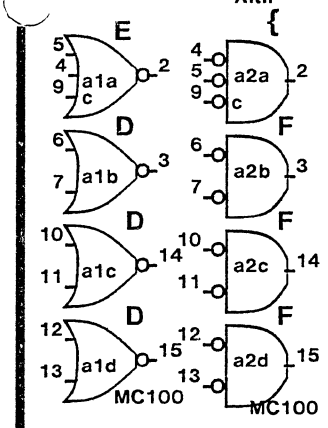
MC100

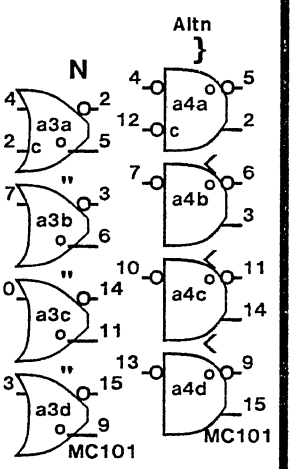
Quad 2-In NOR
with strobe



Tpd = 3.3 est

MC101

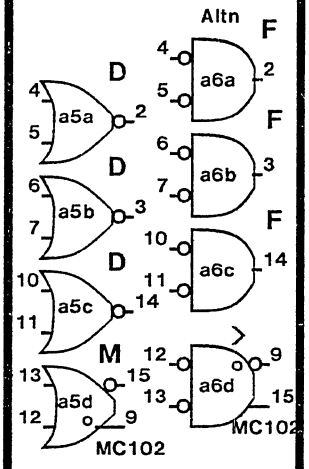
Quad OR/NOR



Tpd = 3.3

MC102

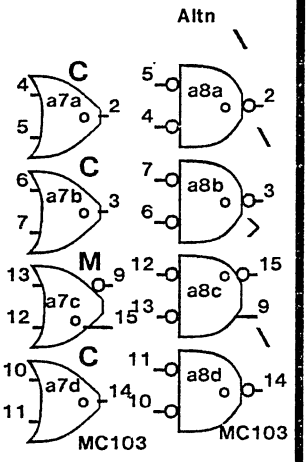
Quad 2-In NOR



Tpd = 3.3

MC103

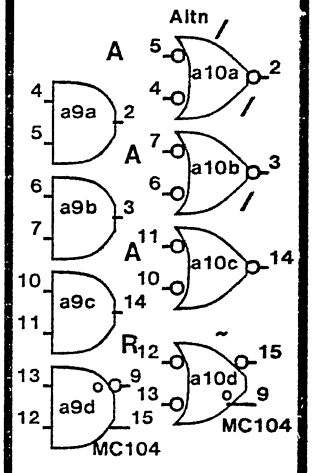
Quad 2-In OR



Tpd = 3.3 est

MC104

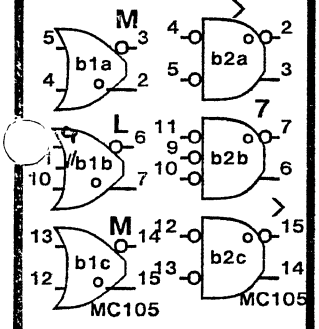
Quad 2-In AND



Tpd = 4.2

MC105

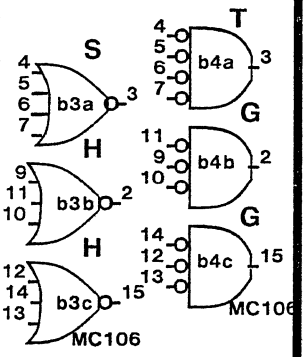
Trip 2-3-2 In
OR/NOR



Tpd = 3.3

MC106

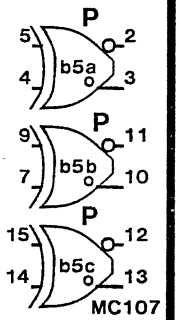
Trip 4-3-3 In
NOR



Tpd = 3.3

MC107

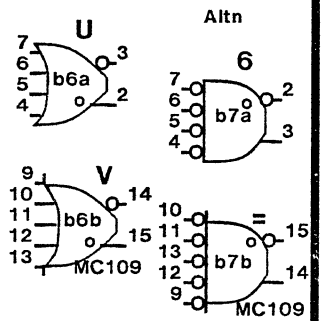
Trip 2-In
Ex-OR
Ex-NOR



Tpd = 4.0

MC109

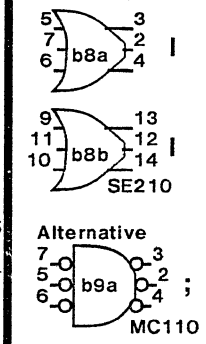
Dual 4-5 In
OR/NOR



Tpd = 3.3

MC110
MC210
SE210
(Selective MC210)

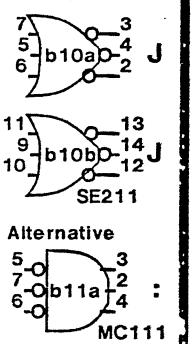
Dual 3-In
3-Out OR



Tpd = 3.8(110)
Tpd = 2.8(210)
Tpd = 1.5(SE) est

MC111
MC211
SE211
(Selective MC211)

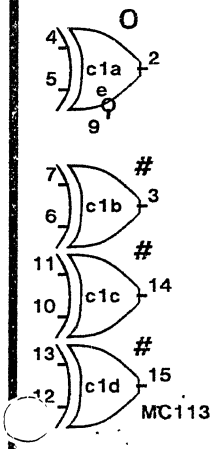
Dual 3-In
3-Out NOR



Tpd = 3.8(111)
Tpd = 2.8(211)
Tpd = 1.5(SE) est

MC113

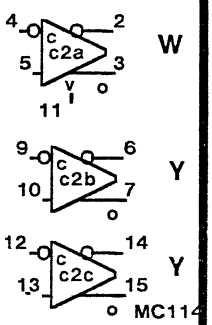
Quad Ex-OR



T(2←4) = 4.5
T(2←9) = 5.1
both EST.

MC114
MC116

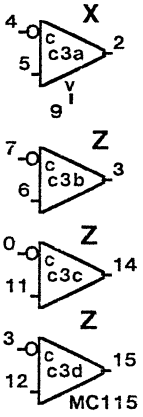
Triple Line
Receiver



Tpd = 4.3(114)
Tpd = 3.6(114)
(Diff. Input)
Tpd = 3.3(116)

MC115

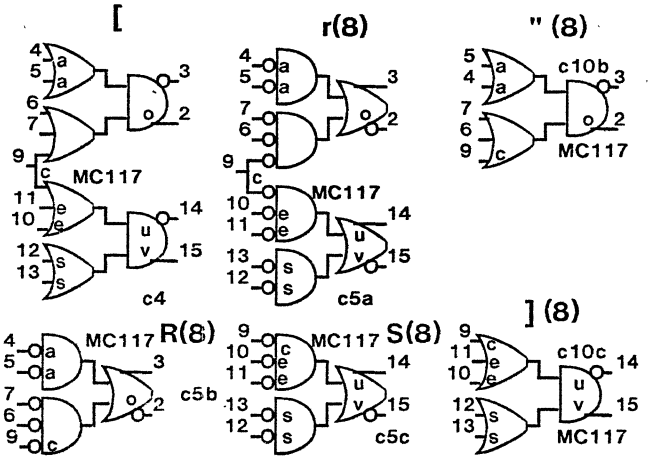
Quad Line
Receiver



Tpd = 3.3

MC117

Dual 2-3 In OR-AND/
OR-AND-INVERT



Tpd = 3.8

Connect only one c pin on bitslice, blob the other c pin

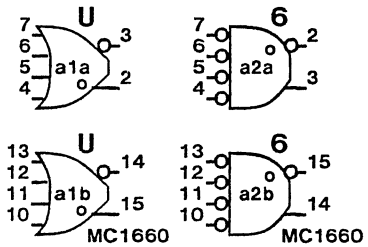
FICAP

[(8)

XEROX SDD	Project	ECL SSI Datasheet	File MC-1.sil	Designer S. T. Chang	Rev B	Date 9/12/78	Page 1

MC1660

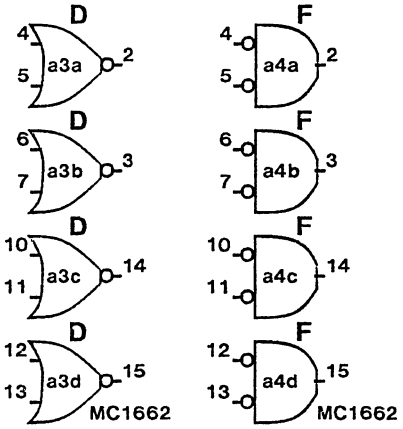
Dual 4 input OR/NOR gate



Tpd = 1.9

MC1662

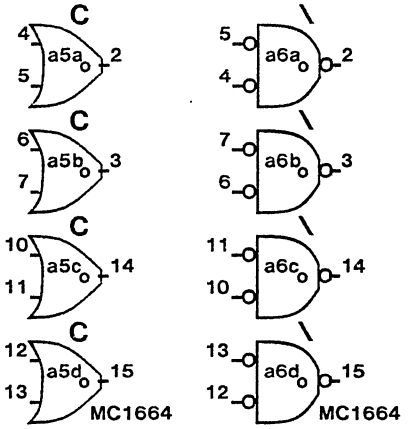
Quad 2 input NOR gate



Tpd = 1.9

MC1664

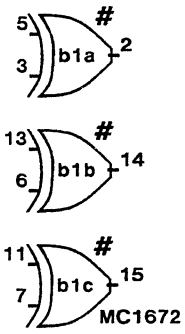
Quad 2 input OR gate



Tpd = 1.9

MC1672

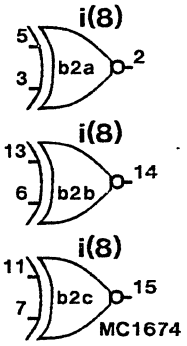
Triple 2 input EXOR gate



Tpd = 2.8

MC1674

Triple 2 inpuEXNOR gate

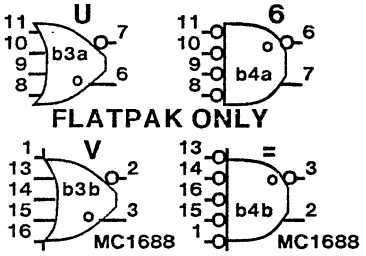


Tpd = 2.8

MC1688

Dual 4/5 input OR/NOR gate

FLATPAK ONLY



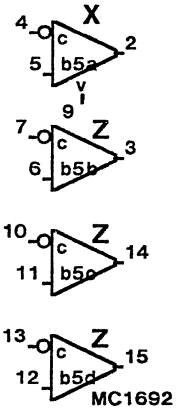
FLATPAK ONLY

FLATPAK ONLY

Tpd = 1.2 est

MC1692

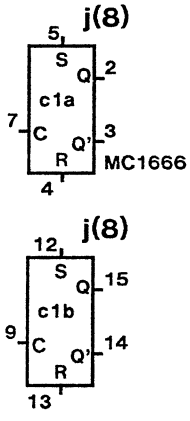
Quad Line Receiver



Tpd = 1.9

MC1666

Dual Clocked R-S Flip-Flop

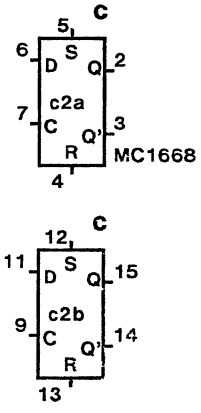


Tpd = 2.8

MC1668

Dual Clocked Latch

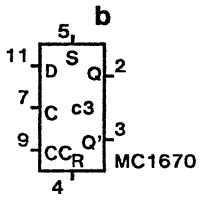
(Q follows D when C is HIGH)



Tpd = 2.8

MC1670

Master-Slave D type Flip-Flop



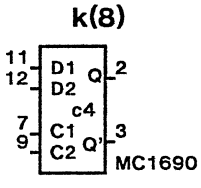
Tpd = 2.9

Tsetup = 0.5 est

Thold = 0.5 est

MC1690

Very Fast D type Flip-Flop



Tpd = 2.3 est

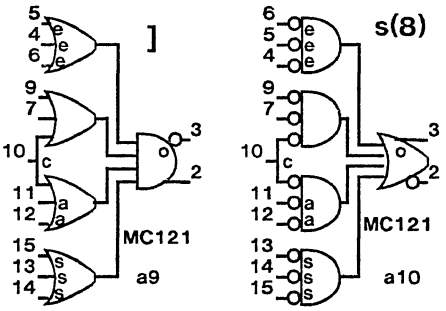
Tsetup = 0.5 est

Thold = 0.5 est

XEROX SDD	Project	File	Designer	Rev	Date	Page
	Datasheet MECL III DATASHEET	MC-10.sil	K. Pier	B	9/10/76	10 end

MC121

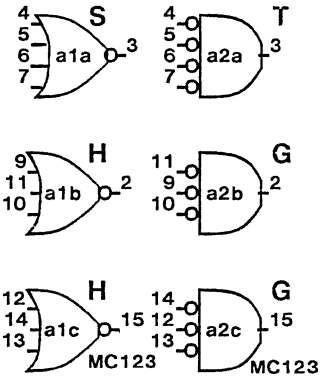
4-wide OR-AND/
OR-AND INVERT



Tpd = 3.8

MC123

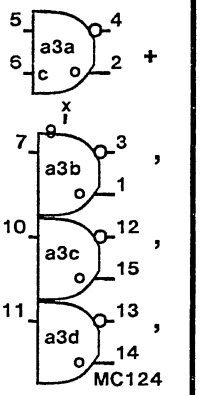
Triple 4-3-3
Bus Driver



Tpd = 3.8

MC124

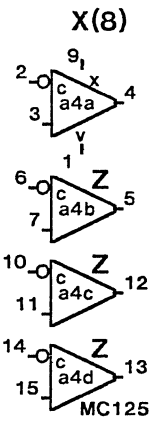
Quad Transl
TTL to ECL



In	Out	Tpd
6+	1+	6
7+	3-	6
6-	1-	6.8
7-	3+	6.8

MC125

Quad Transl
ECL to TTL

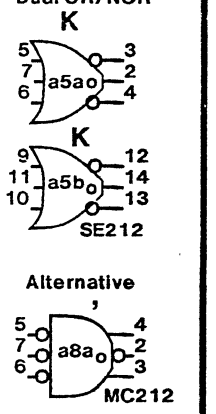


Tpd = 6

MC212
SE212

(Selective MC212)

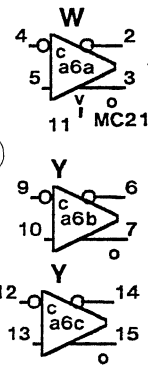
High speed
Dual OR/NOR



Tpd = 2.8(MC212)
Tpd = 1.5(SE212 (est.)

MC216

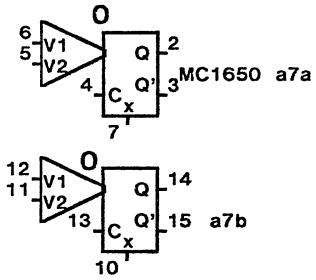
High speed
Line Receiver



Tpd = 2.7(est.)
(Diff. Input)
Tpd = 2.3(est.)

MC1650, MC1651

Dual A/D Comparator



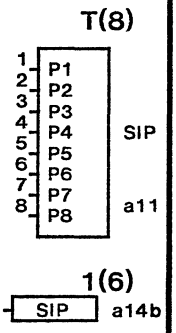
1650 (high impedance inputs)
1651 (low impedance inputs)

C	V1,V2	Qtn+1	Q'tn+1
H	V1>V2	H	L
H	V1<V2	L	H
L	Don'tCare	Qtn	Q'tn

T(2←6) = 5.7 T(2←4) = 5.2

SIP

SIP package



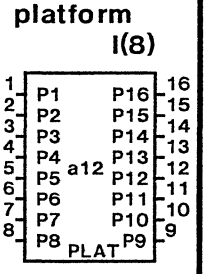
From b to i
for pin# 1 to 8

TERM

automatic
assignment
terminator

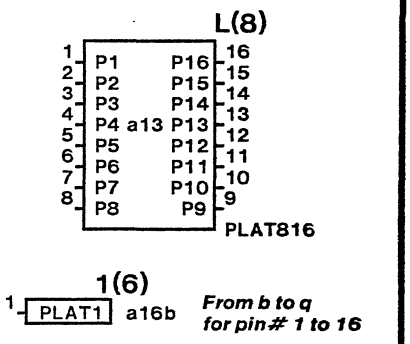
PLAT

Augat
platform



From b to q
for pin# 1 to 16

PLAT's

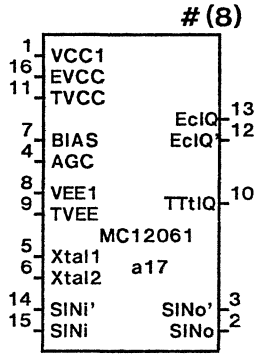


From b to q
for pin# 1 to 16

Platform for trace Cutting

Component name	CUT traces on pins
PLAT1	1
PLAT8	8
PLAT16	16
PLAT18	18
PLAT116	116
PLAT816	816
PLAT1816	1816

MC12061

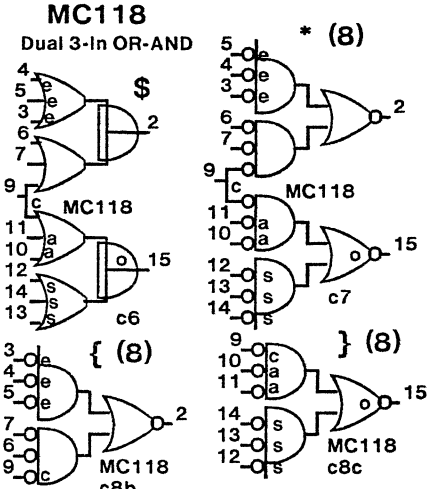


Crystal Oscillator

See page 6-42
of Motorola
Semiconductor
Library Volumn 4

MC118

Dual 3-In OR-AND

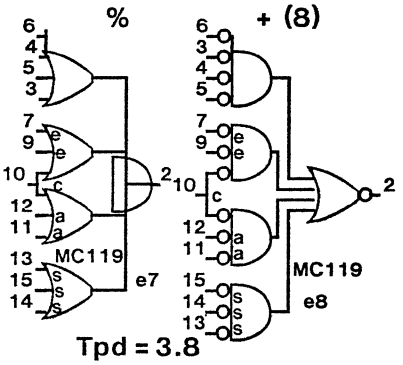


Tpd = 3.8

Connect only one c pin on
bitslice, blob the other c pin

MC119

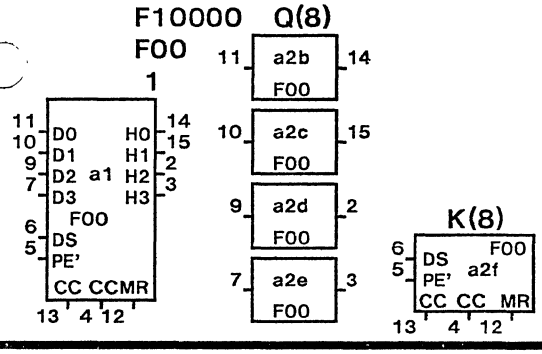
4-Wide 3-3-3



Tpd = 3.8

XEROX SDD	Project	ECL SSI Datasheet	File MC-2.sil	Designer S. T. Chang	Rev C	Date 9/7/78	Page 2

F10000 Q(8) F00 1



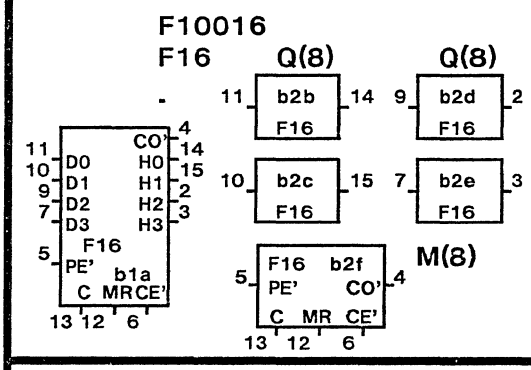
4 bit Shift Register

MR	PE'	CC	CC	MODE
H	X	X	X	reset - all outputs low
L	L	L	↑↑	parallel load
L	L	↑↑	L	parallel load
L	H	↑↑	L	shift left
L	H	L	↑↑	shift left
L	X	H	X	hold
L	X	X	H	hold

Tpd = 5.5
Tw' = 3.8 (clock pulse width)
Ts = 1.7 (data setup)
Th = 1.1 (data hold)
Tse = 6.0 (PE' setup)

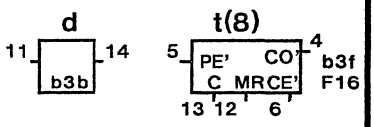
(all times estimates)

F10016 F16 Q(8) Q(8)



4 bit Binary Counter

CE	PE'	MR	CP	FUNCTION
L	L	L	↑↑	parallel load
H	L	L	↑↑	parallel load
L	H	L	↑↑	count
H	H	L	↑↑	hold
X	X	L	/	masters open, slaves hold
X	X	H	X	reset

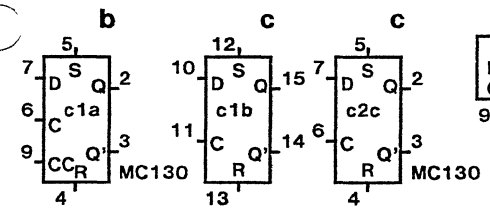


Tpd = 5.5
Tw = 3.5 (clock pulse width)
Ts = 2.2 (data setup)
Th = 1.1 (data hold)
Tse = 2.8 (PE' and CE' setup)

MC130

Dual Latch

obsolete: A(8) c3d CC MC130



D	CC	C	S	R		Qn+1	FUNCTION
L	L	L	X	X	L	Q	follows D
H	L	L	X	X	H	Q	follows D
X	H	X	L	L	Qn		hold
X	X	H	L	L	Qn		hold
X	H	X	H	L	H		set
X	X	H	H	L	H		set
X	H	X	L	H	L		reset
X	X	H	L	H	L		reset
X	H	X	H	H			indeterminate

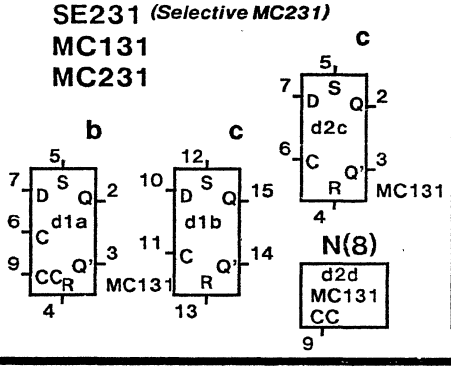
Tpd = 4.1
Ts = 2.8 est
Th = 1.7 est

SE231 (Selective MC231) MC131 MC231

Dual D type Master-Slave Flip-flop

X X X H H indeterminate

obsolete: A(8) d3d CC MC131



D	CC	C	S	R		Qn+1	FUNCTION
X	L	L	L	L	Qn		hold
L	L	↑↑	L	L	L		memory
L	↑↑	L	L	L	L		memory
H	L	↑↑	L	L	H		memory
H	↑↑	L	L	L	H		memory
X	X	X	H	L	H		set
X	X	X	L	H	L		reset
X	X	X	H	H			indeterminate
X	H	X	H	H			indeterminate

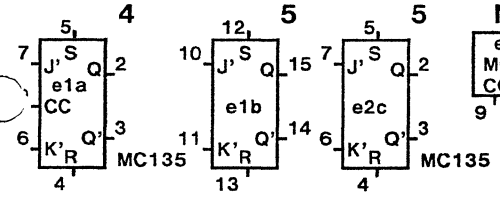
MC131	MC231	SE231
Tpd = 5.0	Tpd = 3.7	Tpd = 2.5
Ts = 2.8	Ts = 1.1	Ts = 1.1
Th = 1.7	Th = 0.8	Th = 0.8

(all times estimates)

MC135

Dual J-K Master Slave Flip-Flop

obsolete: A(8) e3d CC MC135



RS Truth Table

R	S	Qn+1
L	L	Qn
L	H	H
H	L	L
H	H	indet

Clocked JK Truth Table

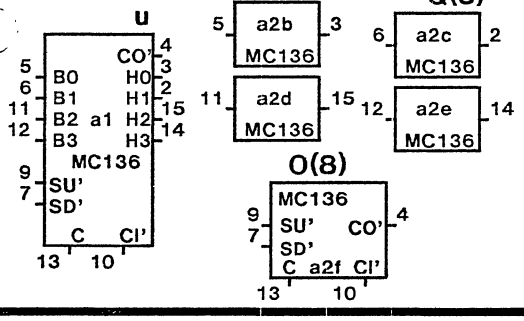
J'	K'	Qn+1
L	L	Qn'
H	L	L
L	H	H
H	H	Qn

clock = ↑↑ on CC

Tpd = 4.6
Trs = 5.2 (R, S to Q)
Ts = 2.8 est
Th = 1.7 est

MC136

Hexadecimal Counter



SU'	SD'	B0	B1	B2	B3	CI'	C	H0	H1	H2	H3	CO'	
L	L	H	H	L	L	X	↑↑	H	H	L	L	L	Load
L	H	X	X	X	X	L	↑↑	H	H	L	H	H	Count Up
L	H	X	X	X	X	L	↑↑	H	H	H	L	H	
L	H	X	X	X	X	L	↑↑	H	H	H	H	L	
L	H	X	X	X	X	H	L	H	H	H	H	H	Hold
L	H	X	X	X	X	H	↑↑	H	H	H	H	H	
H	H	X	X	X	X	X	↑↑	H	H	H	H	H	
L	L	L	L	H	H	X	↑↑	L	L	H	H	L	Load
H	L	X	X	X	X	L	↑↑	L	L	H	L	H	Count Down
H	L	X	X	X	X	L	↑↑	L	L	L	H	H	
H	L	X	X	X	X	L	↑↑	L	L	L	L	L	
H	L	X	X	X	X	L	↑↑	H	H	H	H	H	

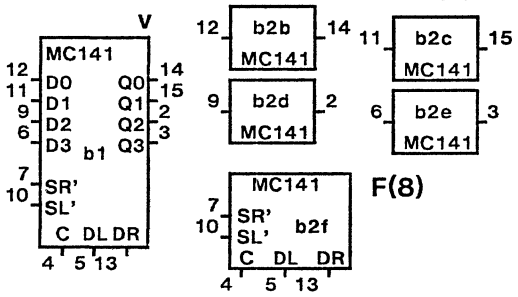
Inputs asumed to vary in sequence from top to bottom

Tpd = 11.5
Tsd = 3.9(data setup)
Tss = 8.3(select setup)
Tsc = 4.1 (CI' setup)
Thc = 3.4 (CI' ld)

(all times estimates)

MC141

4 bit Shift Register



SR'	SL'	MODE	Qi(n+1)
L	L	parallel load	Di(n)
L	H	shift right	Qi-1(n)
H	L	shift left	Qi+1(n)
H	H	Hold	Qi(n)

ALL OUTPUTS EXIST AFTER CLOCK

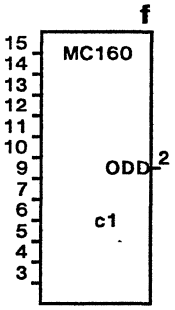
clock = ↑↑ on C

Tpd = 4.2
Tsd = 2.8(data setup)
Tss = 5.5(select setup)
Thd = 1.7(data hold)
Ths = 1.1 (select hold)

(all times estimates)

MC160

12-bit Parity Generator/Checker



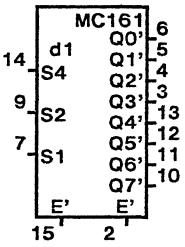
Sum of high inputs	=	*Output*
Even		Low
Odd		High

Tpd = 8.3 est

MC161

8(8)

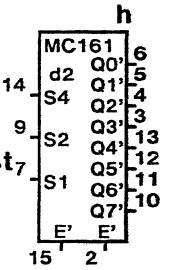
Binary 1 Of 8 decoder - low true outputs



E'	E'	S1	S2	S4	Q0'	Q1'	Q2'	Q3'	Q4'	Q5'	Q6'	Q7'
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

obsolete:

h

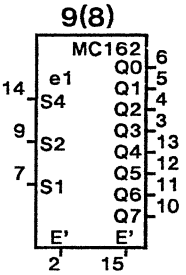


Tpd = 6.6 est

MC162

9(8)

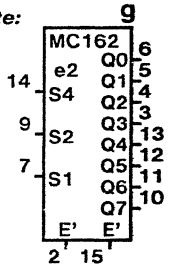
Binary 1 Of 8 decoder - high true outputs



E'	E'	S1	S2	S4	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	L	L	L	L	H	L	L	L	L
L	L	L	L	H	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L

obsolete:

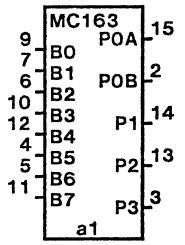
g



Tpd = 6.4

MC163

n



Error Detection/Correction Circuit

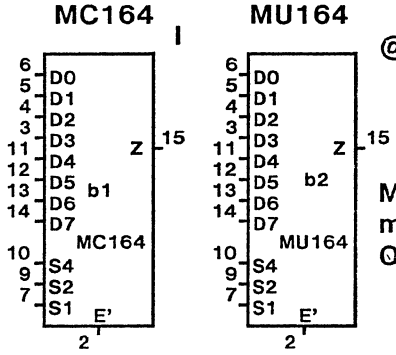
P0A = B1, B2, B4, B7
P0B = B0, B3, B5, B6
P1 = B1, B3, B5, B7
P2 = B2, B3, B5, B7
P3 = B4, B5, B6, B7

(, denotes EXOR)

Tpd = 7.5 est

MC164 / MU164

l



@(8)

Midas multiplexer ONLY

8 line Multiplexer

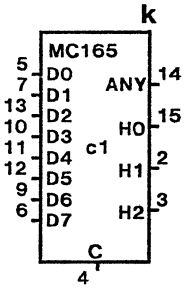
E'	S1	S2	S4	Z
L	L	L	L	D0
L	H	L	L	D1
L	L	H	L	D2
L	H	H	L	D3
L	L	L	H	D4
L	H	L	H	D5
L	L	H	H	D6
L	H	H	H	D7
H	X	X	X	L

Tpdd = 4.8 (data)
Tpds = 6.5 (select)
Tpde = 3.1 (enable)

(all estimates)

MC165

k



8 input Priority Encoder with latch

D0	D1	D2	D3	D4	D5	D6	D7	ANY	H0	H1	H2
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

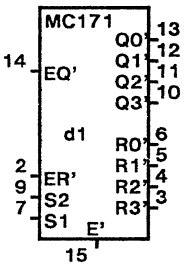
Outputs held when C is high

Tpdd = 16.5 (data)
Tpdc = 5.3 (clock)
Ts = 5.1
Th = 0.0

(all estimates)

MC171

j



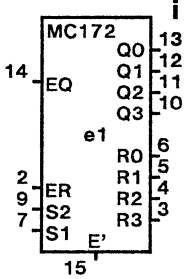
Dual Binary to 1-of-4 Decoder - low true outputs

E'	EQ'	ER'	S1	S2	Q0'	Q1'	Q2'	Q3'	R0'	R1'	R2'	R3'
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	H	L	H	L	H	H	H	L	H	H
L	L	L	L	H	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	L	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H

Tpd = 6.4

MC172

i



Dual Binary to 1-0f-4 Decoder - high true outputs

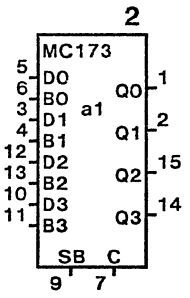
E'	EQ	ER	S1	S2	Q0	Q1	Q2	Q3	R0	R1	R2	R3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	H	L	L	H	L	L	L	H	L	L
L	H	H	L	H	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L

Tpd = 6.4

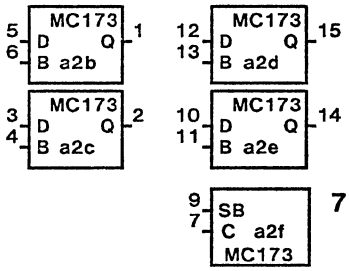
XEROX SDD	Project		File	Designer	Rev	Date	Page
	Datasheet	ECL MSI datasheet	MC-5.sil	K. Pier	A	7/28/76	5

MC173

Quad 2-input Multiplexer/Latch

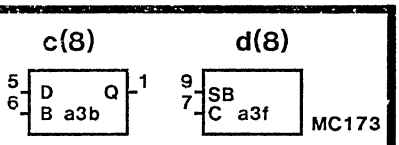


U(8)



SB	C	Qi(n+1)
H	L	Bi(n)
L	L	Di(n)
X	H	Qi(n)

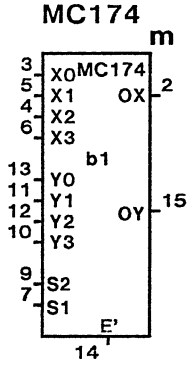
obsolete:



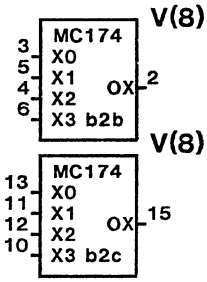
Tpdd = 5.3 (data)
Tpdc = 6.8 (clock)
Tpds = 6.7 (select)
Thd = 2.8 (hold data)
Ths = 1.7 (hold select)

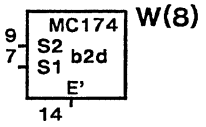
MC174

Dual 4 to 1 Multiplexer



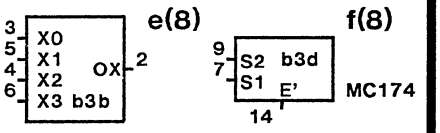
V(8)





E'	S1	S2	OX	OY
H	X	X	L	L
L	L	L	X0	Y0
L	H	L	X1	Y1
L	L	H	X2	Y2
L	H	H	X3	Y3

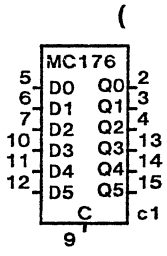
obsolete:



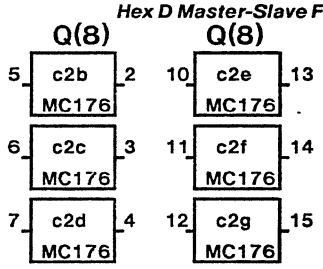
Tpdd = 4.8(data)
Tpde = 3.2(enable)
Tpds = 6.4(select)

MC176

Hex D Master-Slave Flip-Flop



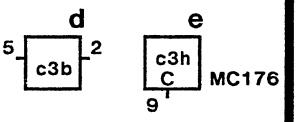
Q(8)



E(8)

C	D	Qi(n+1)
L	X	Qi(n)
↑	L	L
↑	H	H

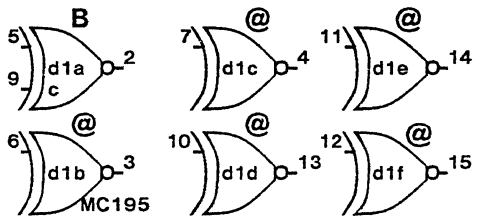
obsolete:



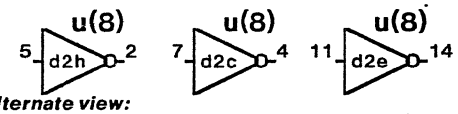
Tpd = 5.0
Ts . = 2.8 est
Th = 1.7 est

MC195

Hex Inverter/Buffer

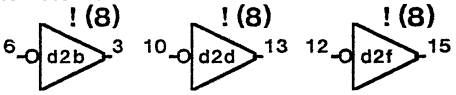


u(8)

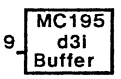


alternate view:

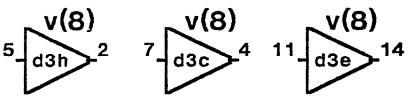
! (8)



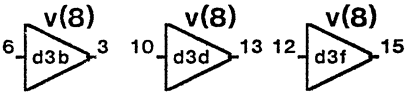
Tpd = 4.2 est



v(8)

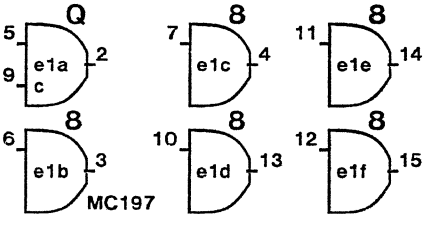


v(8)

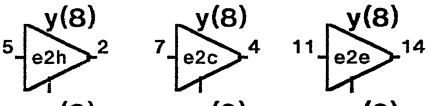


MC197

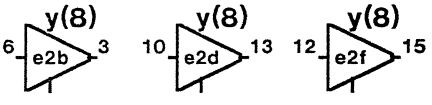
Hex AND gate



y(8)



y(8)

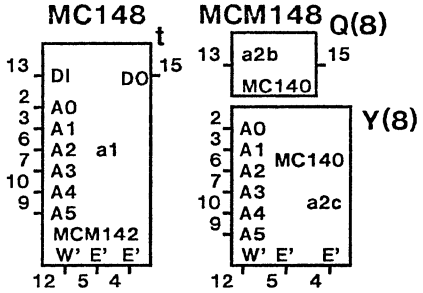


Tpdd = 4.2 (data) est
Tpde = 5.3 (enable) est

XEROX SDD	Project	File	Designer	Rev	Date	Page
	Datasheet ECL MSI datasheet	MC-6.sil	K. Pier	B	2/3/77	6

MC140 MCM140
MC142 MCM142
MC148 MCM148

64 Bit Random Access Memory



Tace = 14(E' access)
Taad = 11(Ai access, MCM142)
Taad = 17(Ai access, MCM140,148)
Tw' = 11 (write pulse width)
Te' = 15 (enable pulse width)

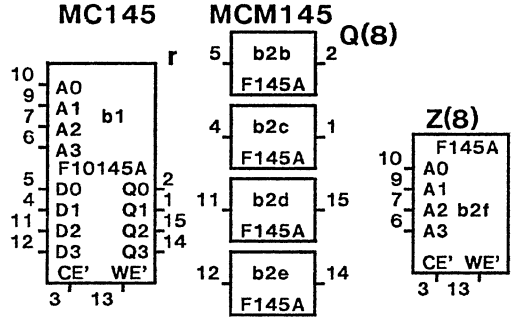
(MCM140 drives 90 ohm loads)

Tsd = 0 (setup times)
Tse = 3.5
Tsa = 5.5

Thd = 3.5 (hold times)
The = 0
Tha = 3.5
(all times estimates)

F145A F10145A
MC145 MCM145

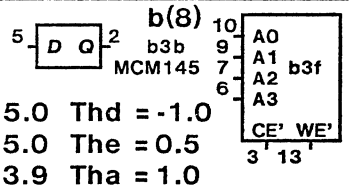
16 x 4 Register File



F10145:
Tace = 6.6(E' access)
Taad = 9.9(Ai access)
Tw' = 4.4(write pulse width)
Te' = 4.4 (enable pulse width)
Twr. = 6.6 (ce,we output recover)

MCM145:
Tace = 10(E' access)
Taad = 15(Ai access)
Tw' = 11 (write pulse width)
Te' = 11 (enable pulse width)

obsolete: a(8) b(8)



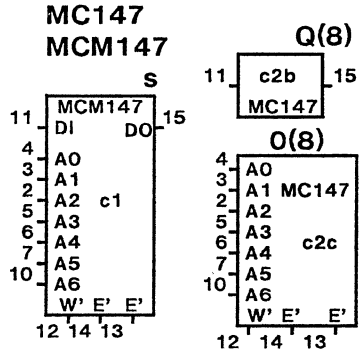
Tsd = 5.0 Thd = -1.0
Tse = 5.0 The = 0.5
Tsa = 3.9 Tha = 1.0

Tsd, Tse relative to ~~end of WE'~~

Tsd = 0 Thd = 5.0
Tse = 5.0 The = 5.0 all est
Tsa = 5.0 Tha = 5.0
Twr = 11.0

MC147
MCM147

128 x 1 bit Random Access Memory



Tace = 8.8(E' access)
Taad = 14(Ai access)
Tw' = 8.8(write pulse width)
Te' = 11 (enable pulse width)

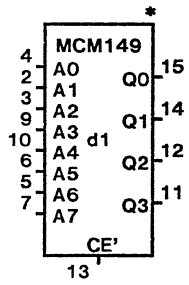
ALL UNUSED INPUTS MUST BE TIED TO VEE

Tsd = 1.0 (setup times)
Tse = 1.0
Tsa = 4.0

Thd = 1.0 (hold times)
The = 1.0
Tha = 3.0
(all times estimates)

MC149 MCM149
MC150 MCM150

256 x 4 bit Programmable ROM

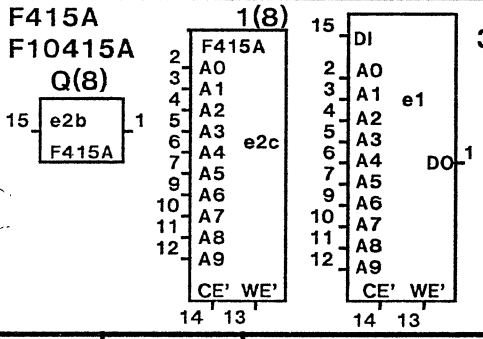


MCM149	MCM150
Tace = 13	Tace = 10.5
Taad = 32	Taad = 30

(all times estimates)

F415A
F10415A

1024 x 1 bit Random Access Memory



Tace = 10(E' access)
Taad = 35(Ai access) *
Tw' = 25 (write pulse width)
Te' = 35 (enable pulse width)

** a 25ns Taad, 20 ns. Tw' part is available*

(all times estimates)

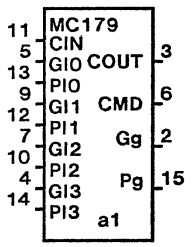
Tsd = 5 (setup times)
Tse = 5
Tsa = 8

Thd = 5 (hold times)
The = 5
Tha = 2

XEROX SDD	Project: Datasheet ECL MSI datasheet	File: MC-7.sil	Designer: K. Pier	Rev: B	Date: 2/14/77	Page: 7

MC179

o



Look Ahead Carry Block

Tpd = 6 est

$Pg = P0 + P1 + P2 + P3$

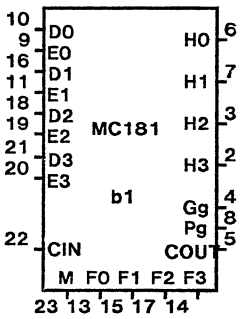
$Gg = (G3 + P2 + P1 + P0)(G2 + P1 + P0)(G1 + P0)G0$

$CMD = (CIN + P3 + P2)(G3 + P2)G2$

$COUT = (CIN + P0 + P1 + P2 + P3)(G3 + P2 + P1 + P0)(G2 + P1 + P0)(G1 + P0)G0$

MC181

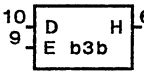
p



4 bit ALU/Function Generator

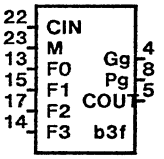
obsolete:

g(8)



MC181

h(8)



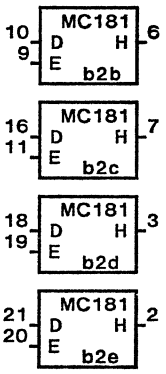
LOGIC FUNCTIONS M is HIGH

ARITHMETIC FUNCTIONS M is LOW CIN is LOW

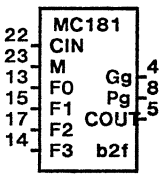
F0	F1	F2	F3	H	H
L	L	L	L	D'	D PLUS 0
L	L	L	H	D' + E'	D PLUS (D AND E')
L	L	H	L	D' + E	D PLUS (D AND E)
L	L	H	H	all 1	D TIMES 2
L	H	L	L	D' AND E'	(D + E) PLUS 0
L	H	L	H	E'	(D + E) PLUS (D AND E')
L	H	H	L	D XNOR E	D PLUS E
L	H	H	H	D + E'	D PLUS (D + E)
H	L	L	L	D' AND E	(D + E') PLUS 0
H	L	L	H	D XOR E	D MINUS E MINUS 1
H	L	H	L	E	(D + E') PLUS (D AND E)
H	L	H	H	D + E	D PLUS (D + E')
H	H	L	L	all 0	MINUS 1 (2s complement)
H	H	L	H	D AND E'	(D AND E') MINUS 1
H	H	H	L	D AND E	(D AND E) MINUS 1
H	H	H	H	D	D MINUS 1

Tpd = 10.8 (max, all functions and carries)

2(8)

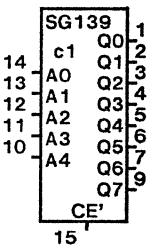


3(8)



SG10139

?

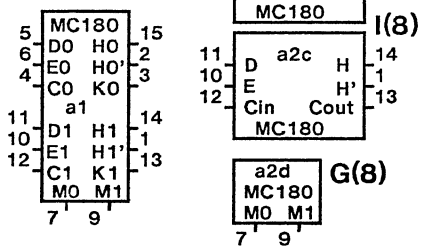


32 x 8 Programmable ROM

Tace = 17.5

Taad = 25 est

MC180

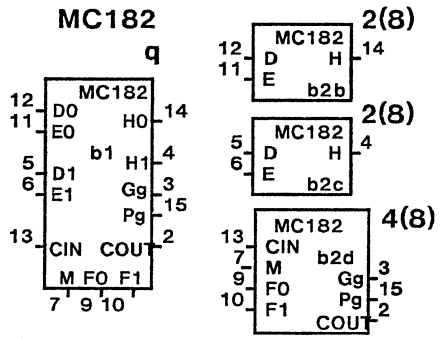


Dual 1 bit Adder/Subtractor

M0	M1	H
H	H	D PLUS E PLUS CARRY
H	L	D MINUS E MINUS CARRY
L	H	E MINUS D MINUS CARRY
L	L	0 MINUS D MINUS E MINUS CARRY

Tpd = 5.8 (all functions)

MC182

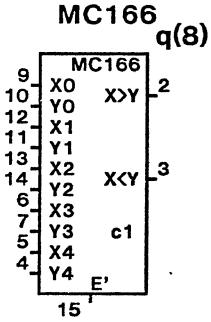


2 bit ALU/Function Generator

		Logic Function M is HIGH	Arithmetic Function M is LOW
FO	F1	H	H
L	L	D XNOR E	D PLUS E PLUS CARRY
L	H	D XOR E	D' PLUS E PLUS CARRY
H	L	D AND E	D PLUS E' PLUS CARRY
H	H	D OR E	D TIMES 2

Tpd = 10.5 est

MC166

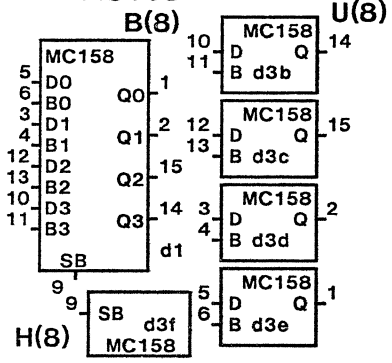


5 bit magnitude comparator

E'	X	Y	X<Y	X>Y
H	x	x	L	L
L	X = Y		L	L
L	X > Y		L	H
L	X < Y		H	L

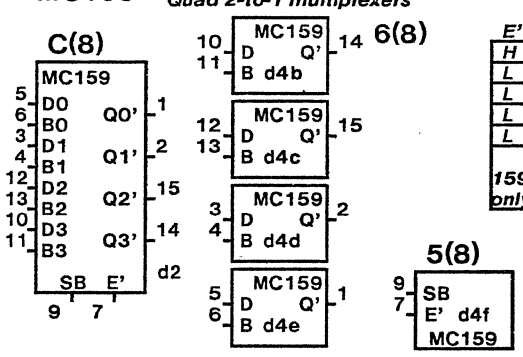
Tpdd = 9.0 est
Tpde = 3.8 est

MC158



MC159

Quad 2-to-1 multiplexers

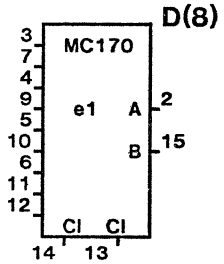


E'	Di	Bi	SB	Qi	Qi'
H	x	x	x		L
L	L	X	L	L	H
L	H	X	L	H	L
L	X	L	H	L	H
L	X	H	H	H	L
159 only				158 only	159 only

MC158	MC159
Tpdd = 3.6	Tpdd = 3.6
Tpds = 5.0	Tpds = 5.0
	Tpde = 5.0

all times est

MC170



9 bit parity circuit with
2 carry inputs

SUM OF PINS 3-12	PIN 2	PIN 15
EVEN	L	?
ODD	H	?
SUM OF ALL INPUTS		
EVEN	?	L
ODD	?	H

TpdA = 6.6
TpdB = 9.9
Tpdcarry = 3.3

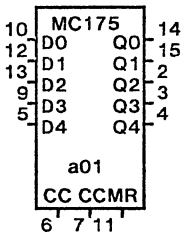
all times est

XEROX SDD	Project	File	Designer	Rev	Date	Page
	Datasheet ECL MSI datasheet	MC-9.sil	K. Pier	E	2/3/77	9

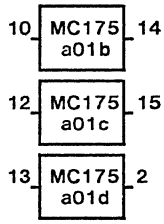
MC175

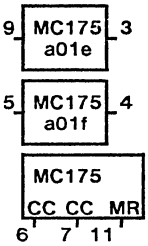
Quint Latch

((8)



Q (8)





) (8)

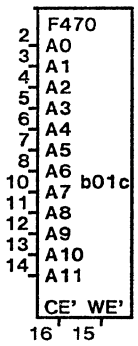
D	CC	CC	MR	Q(n+1)
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Q(n)
X	X	H	L	Q(n)
X	H	X	H	L
X	X	H	H	L

Tpdd	= 3.6	(data)
Tpdc	= 4.4	(clock)
Tpdr	= 4.2	(reset)
Ts	= 3.7	(setup)
Th	= 2.2	(hold)

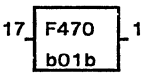
F470

4K x 1 random access memory

$ (8)



Q (8)

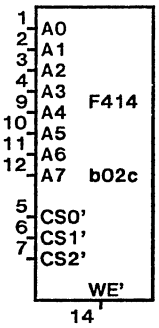


Taad	= 35	A access
Tace	= 15	CE access
Tw'	= 25	write pulse
Tsd	= 5	setup data
Thd	= 5	hold data
Tsa	= 10	setup addr
Tha	= 5	hold addr
Tsce	= 5	setup CE
Thce	= 5	hold CE
Twd	= 15	write disable
Twr	= 20	write recover
Tcer	= 15	CE recover

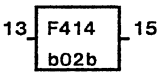
F414

256 x 1 random access memory

~ (8)



Q (8)



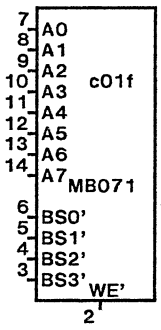
Taad	= 10	A access
Tace	= 6	CE access
Tw'	= 7	write pulse
Tsd	= 1	setup data
Thd	= 2	hold data
Tsa	= 1	setup addr
Tha	= 2	hold addr
Tsce	= 1	setup CE
Thce	= 2	hold CE
Twd	= 8	write disable
Twr	= 10	write recover
Tcer	= 6	CE recover

MB071

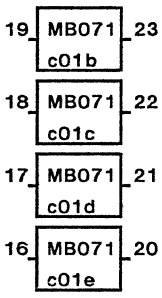
256 x 4 random access memory

QIT package + platform

% (8)



Q (8)



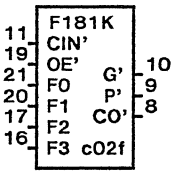
Taad	= 10.0	A access
Tabs	= 4.5	BS access
Tw'	= 8.0	write pulse
Tsd	= 2.0	setup data
Thd	= 2.0	hold data
Tsa	= 2.0	setup addr
Tha	= 2.0	hold addr
Tsbs	= 2.0	setup BS
Thbs	= 2.0	hold BS
Twd	= 5.0	write disable
Twr	= 9.0	write recover
Tbsr	= 4.5	BS recover

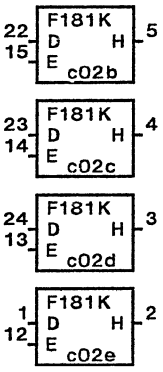
F181K

100K series 4 bit ALU
0.4 wide DIP package

2 (8)

& (8)





Tdh	= 6.5	D to H
Teh	= 6.5	E to H
Tfh	= 6.5	F to H
Tcinh	= 4.7	CIN to H
Tcio	= 3.6	CIN to CO
Tdpg	= 4.1	D to P,G
Tepg	= 4.1	E to P,G
Tfpg	= 4.1	F to P,G
Tdco	= 5.4	D to CO
Teco	= 5.4	E to CO
Tfco	= 5.4	F to CO
Toeh	= 2.1	OE to H