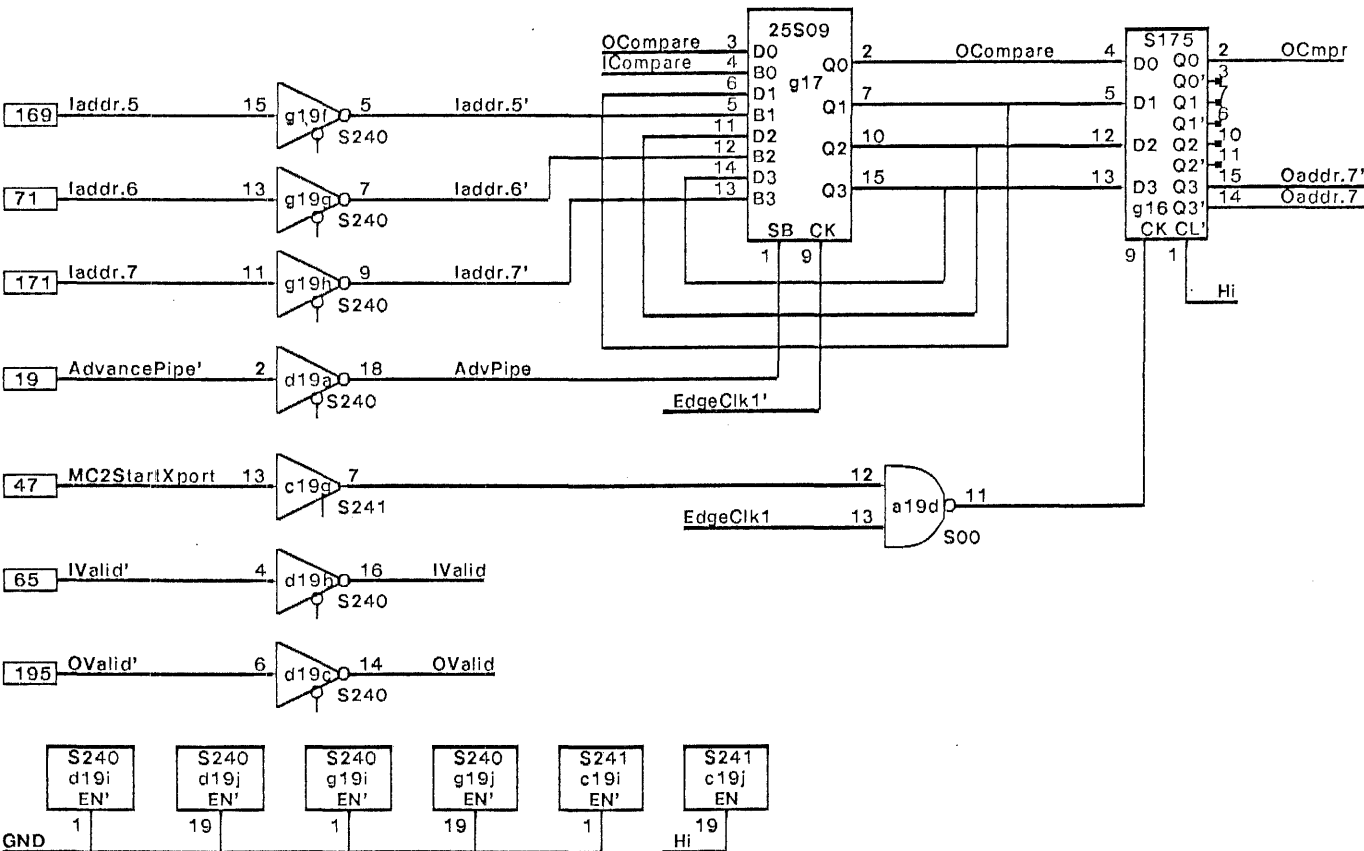
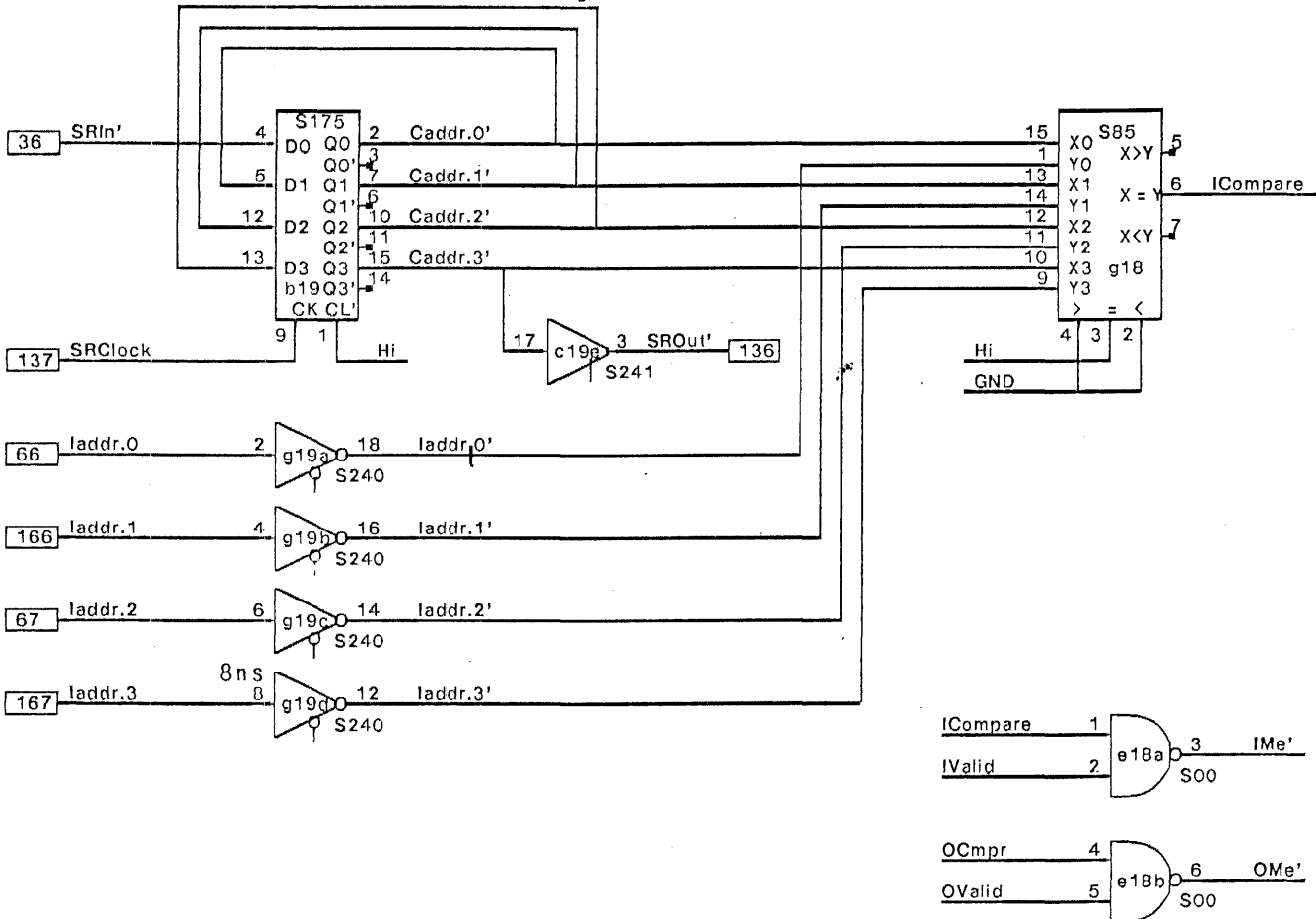
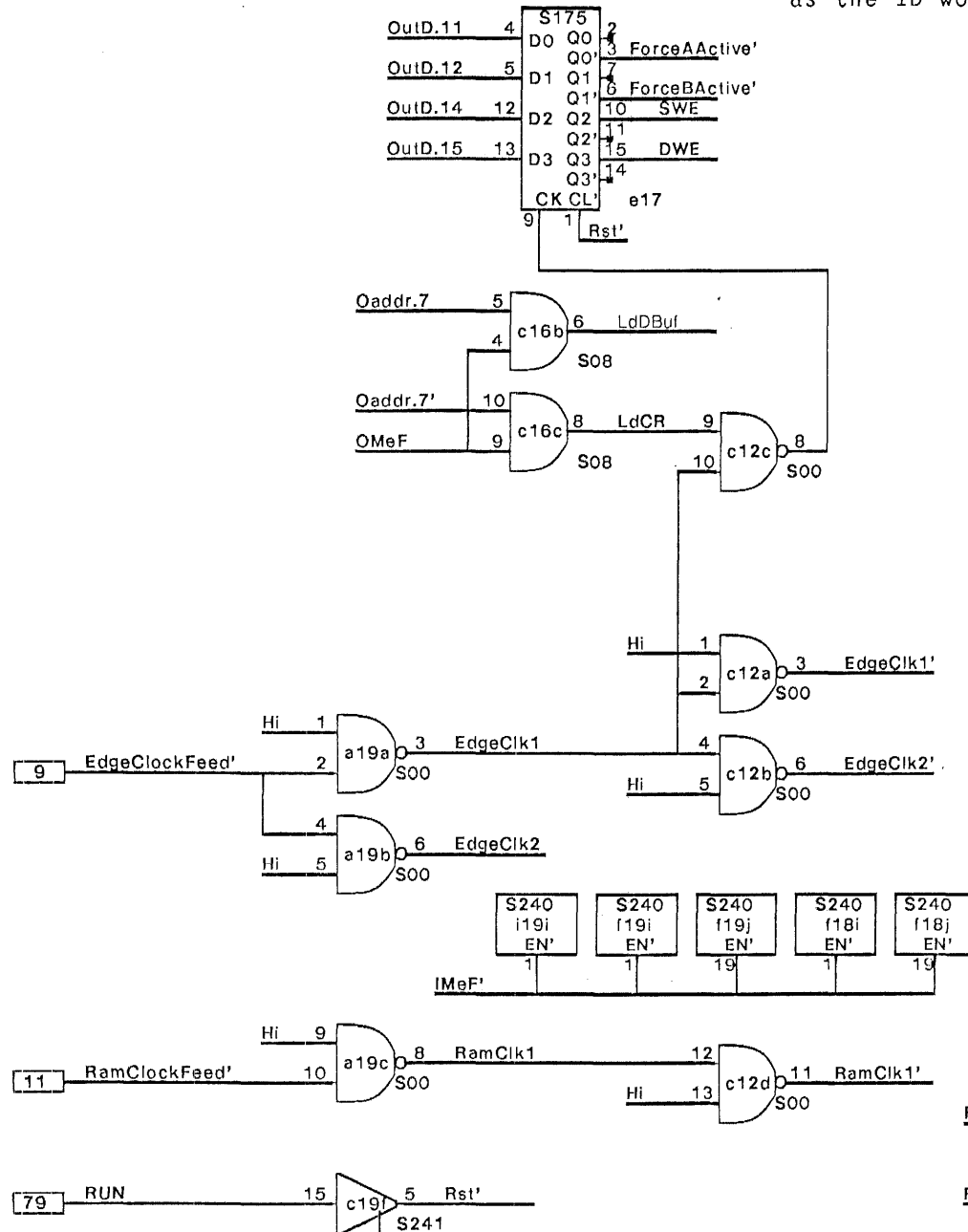
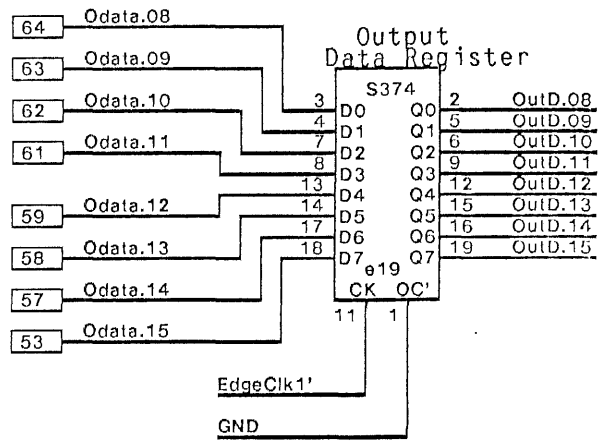
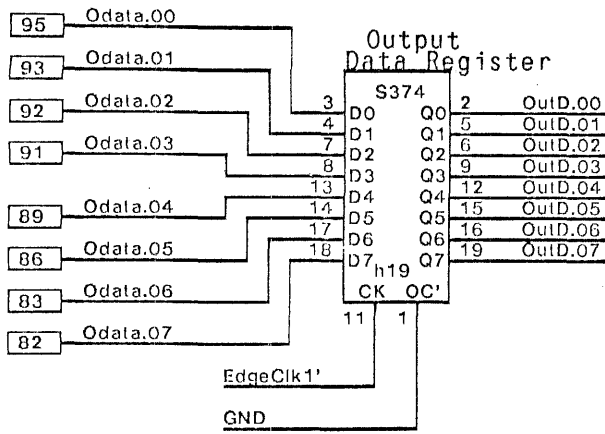
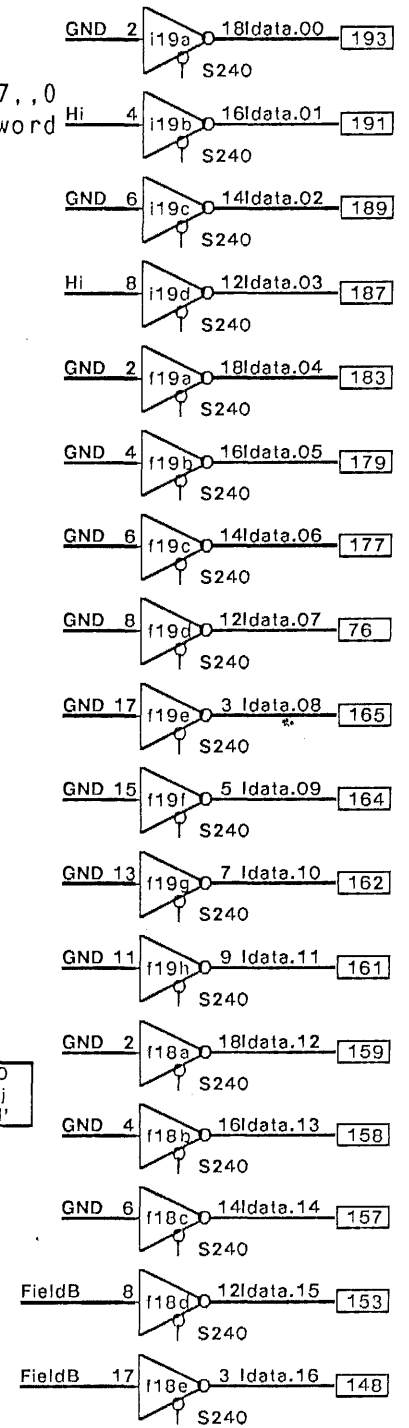


Controller Addressing

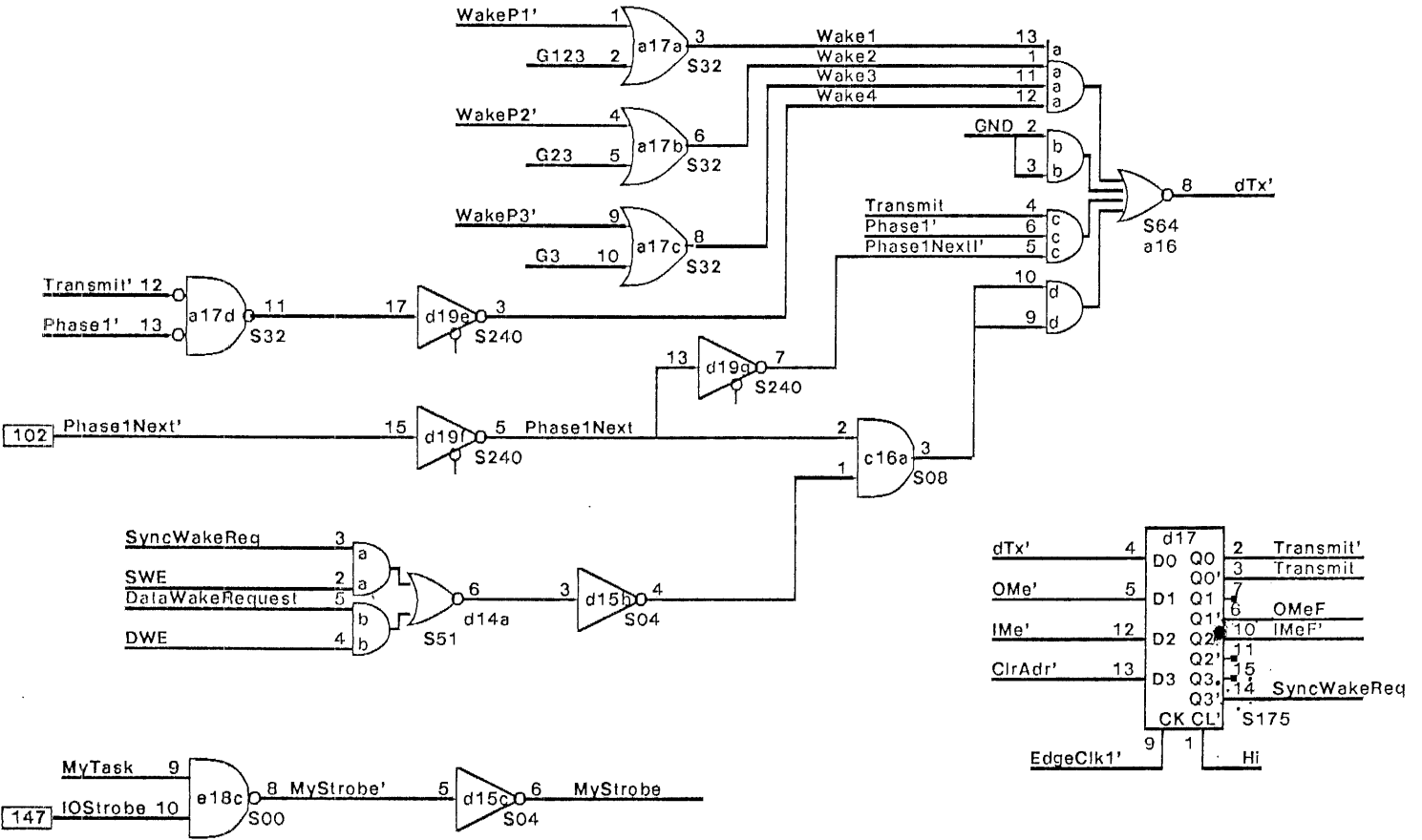
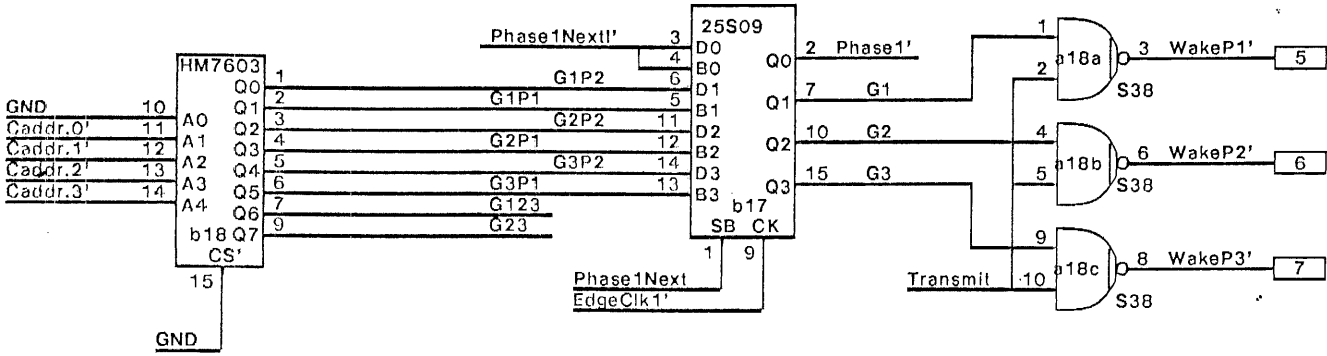




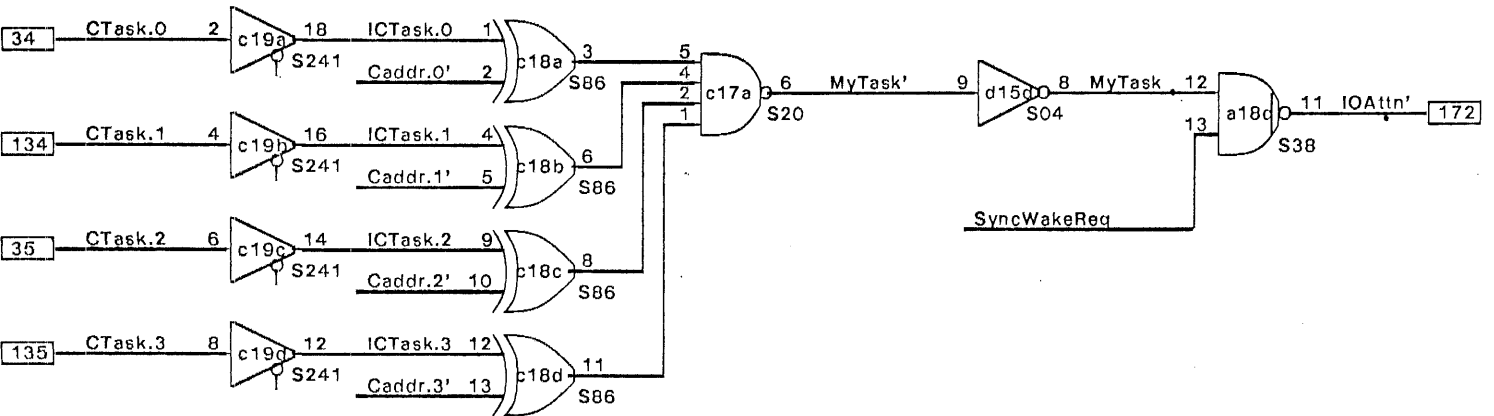
Returns 127,,0  
as the ID word

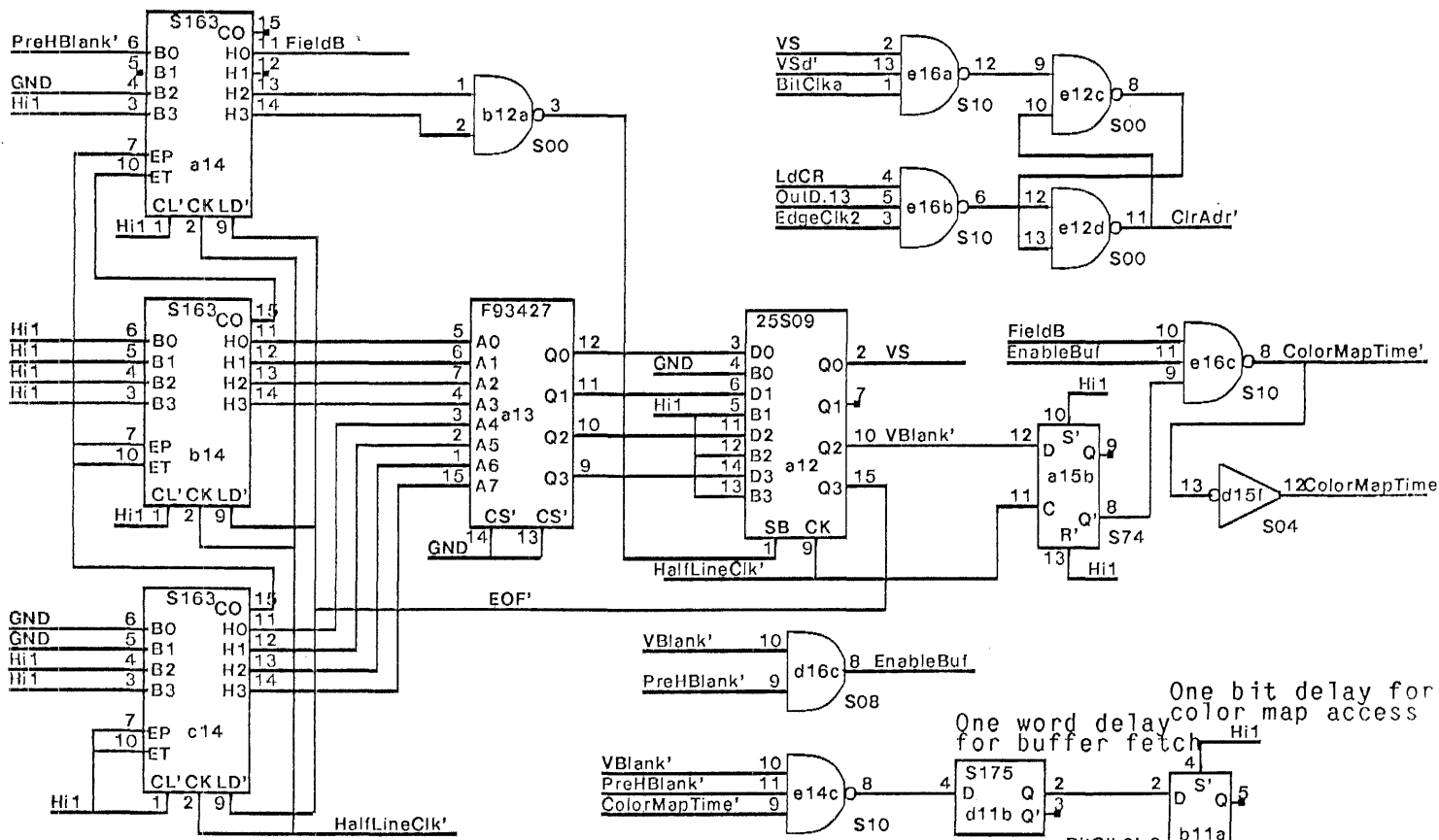


### WakeUp Priority Encoding Logic

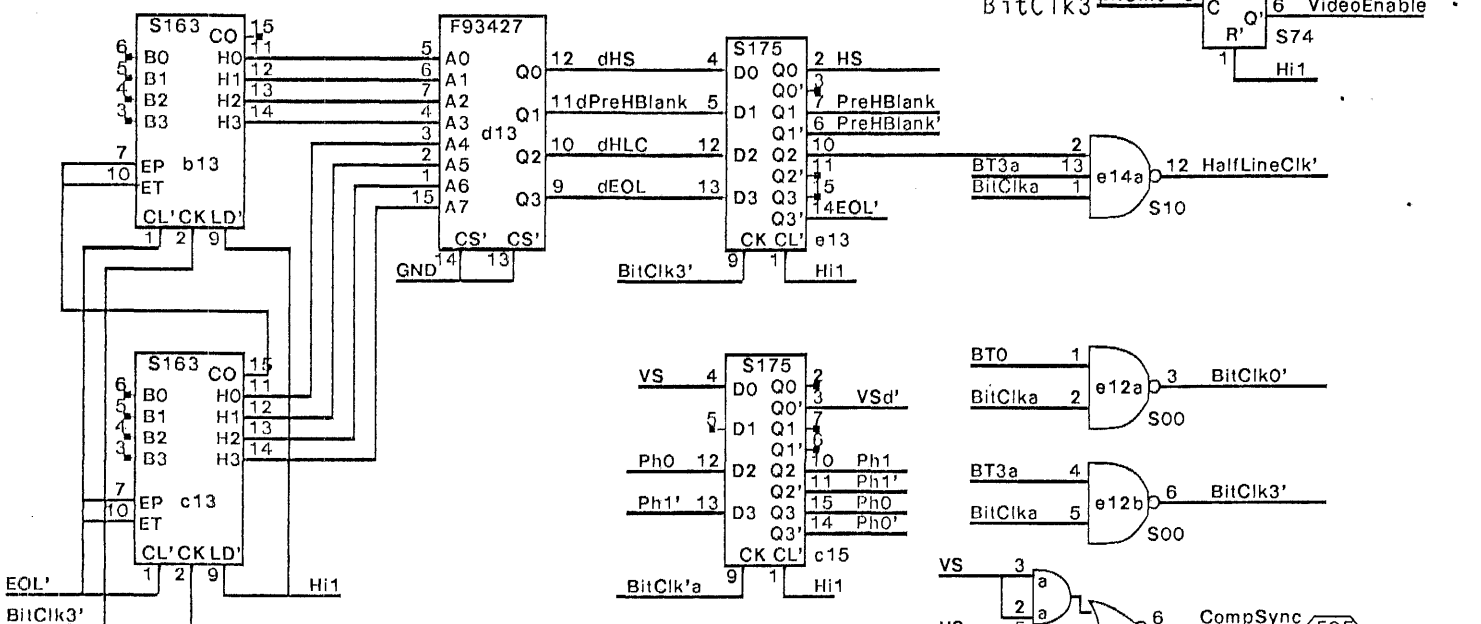


### Current Task Comparator (XOR) IO Attention Logic

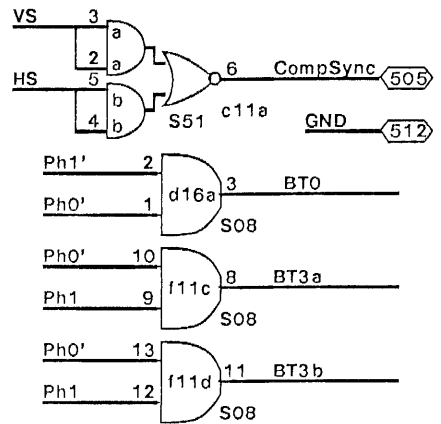
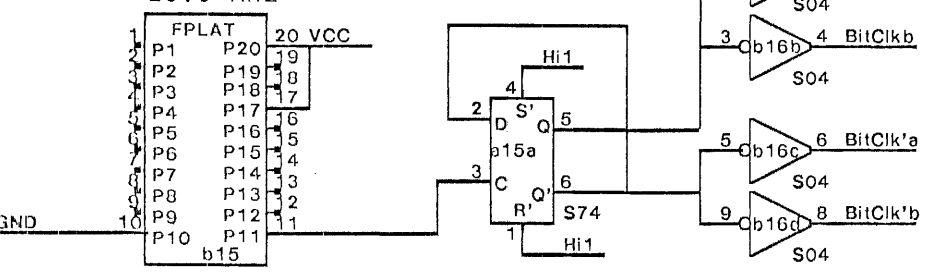




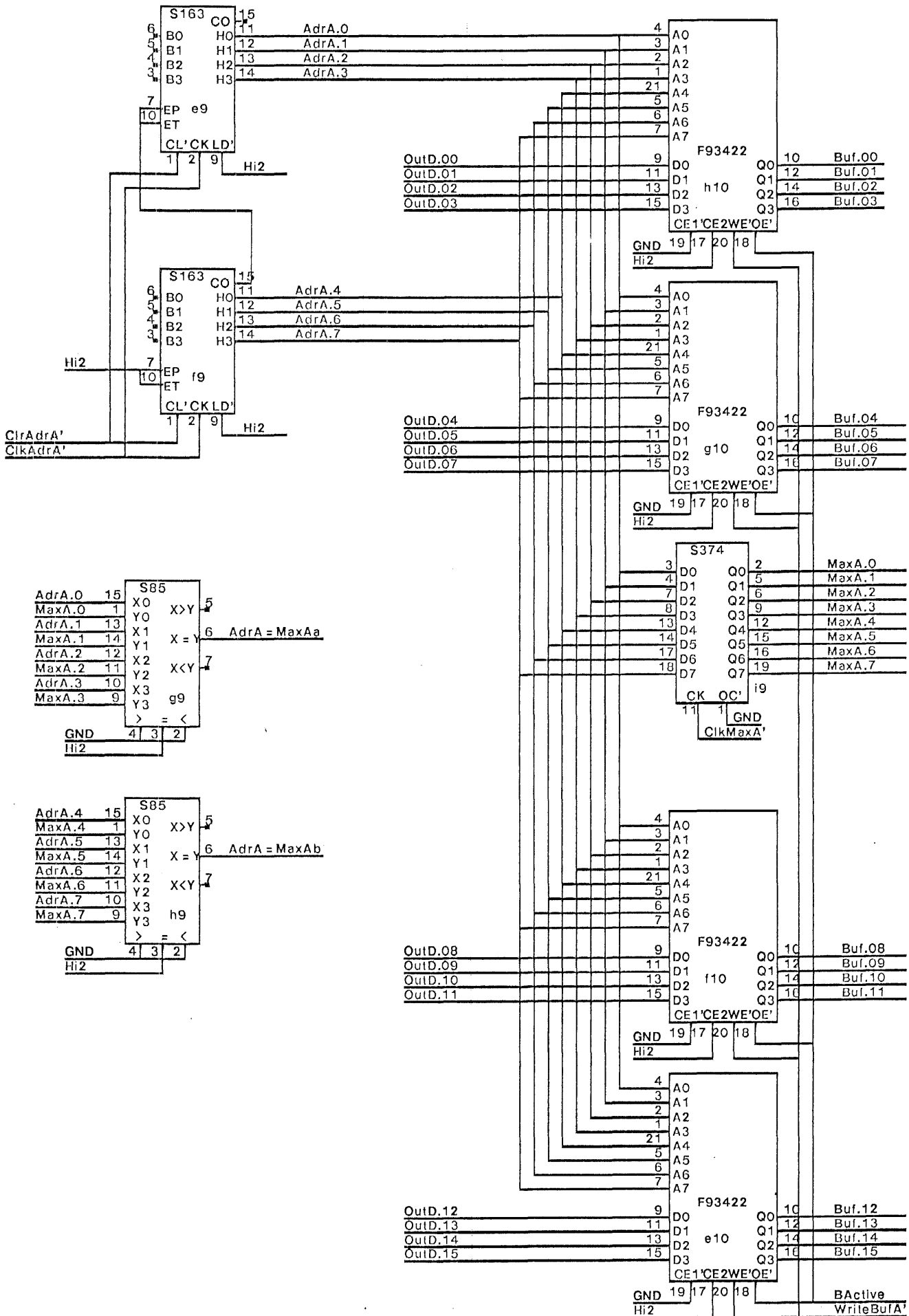
One bit delay for color map access  
 One word delay for buffer fetch

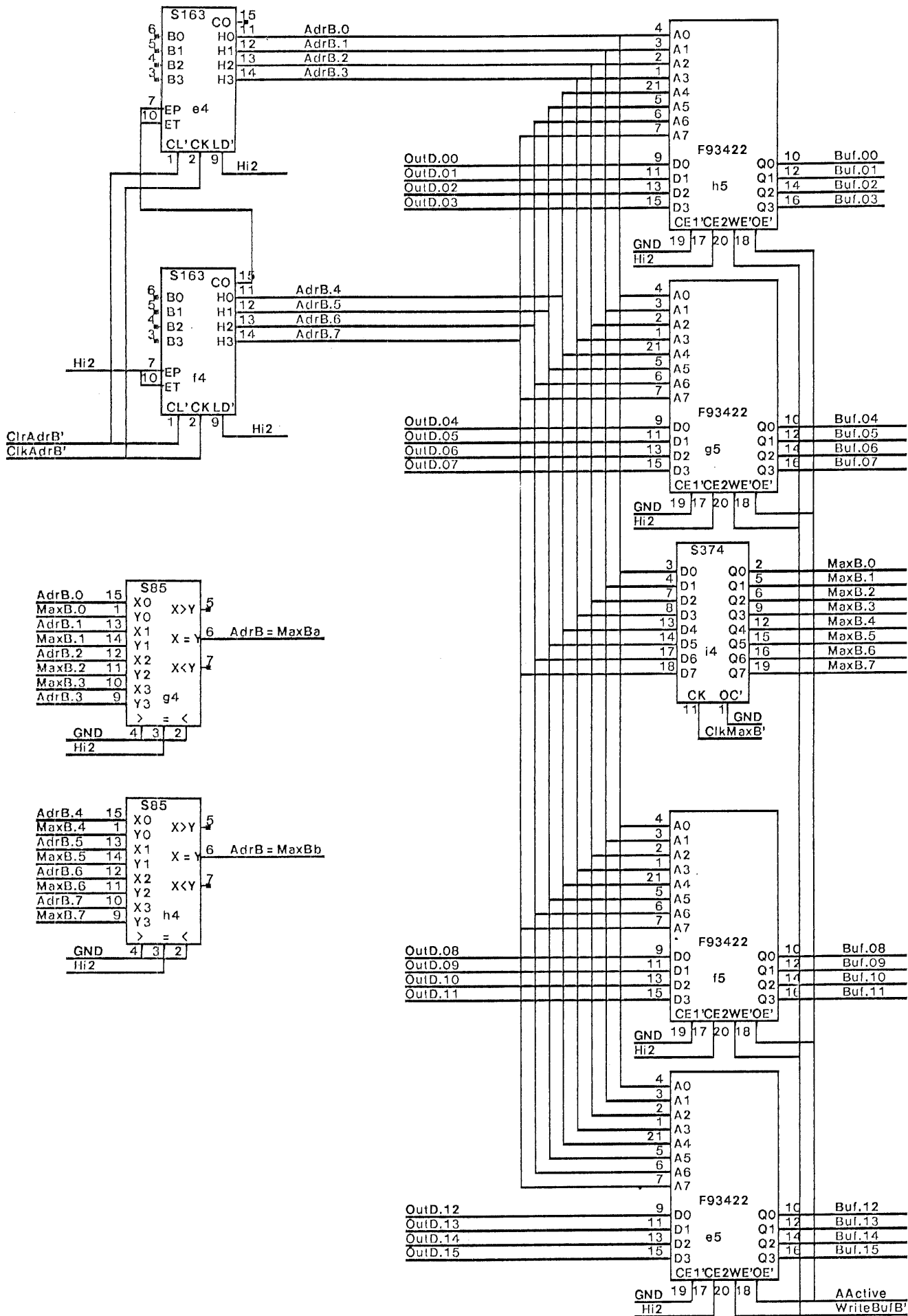


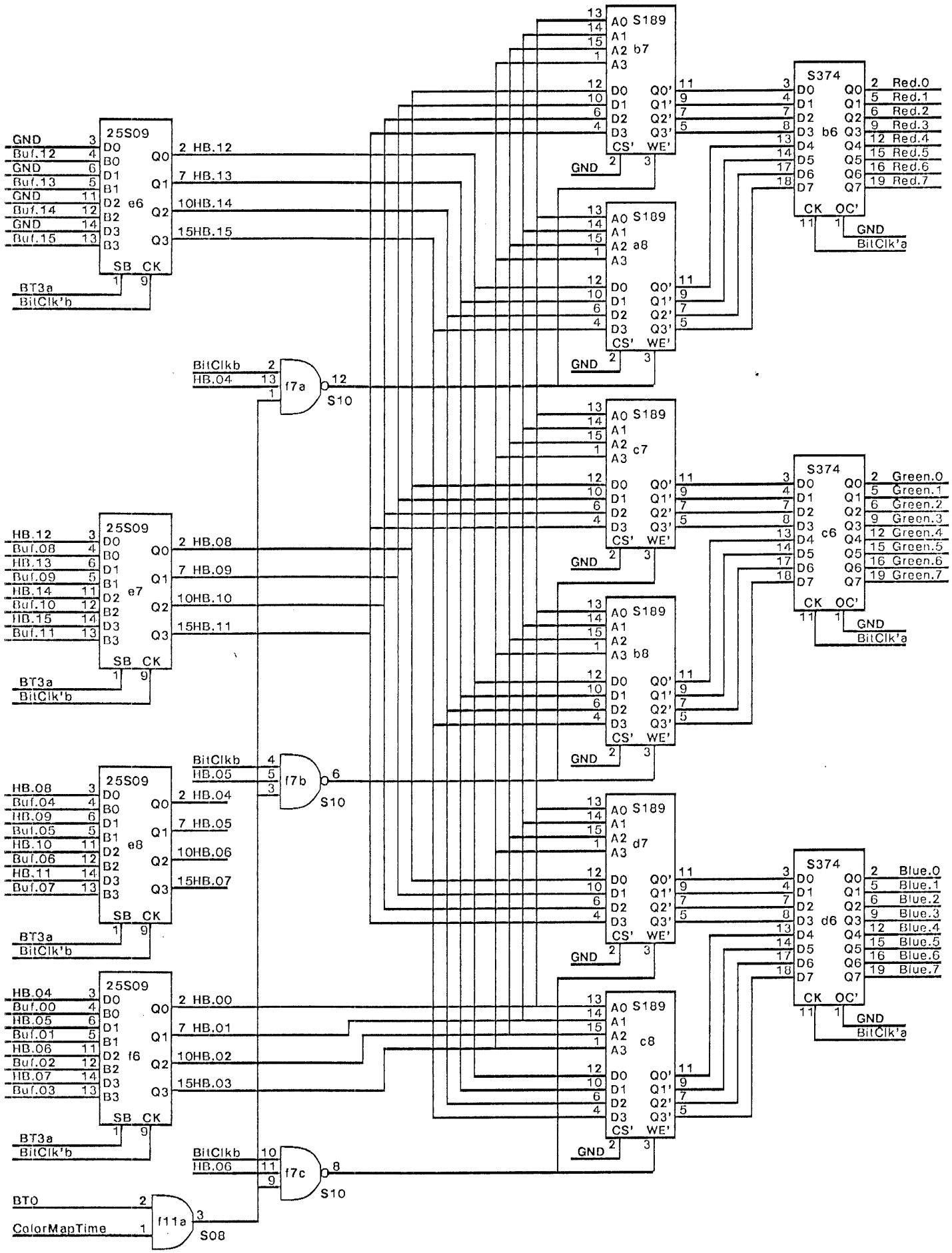
14pin K1100A oscillator  
 25.0 MHz

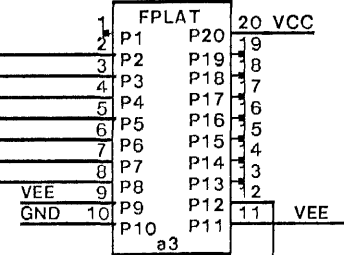
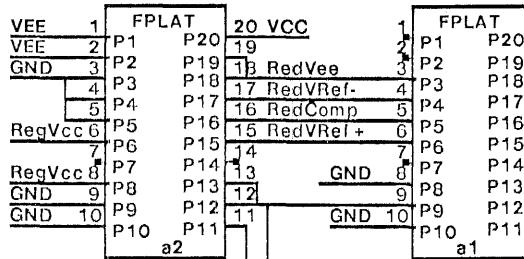
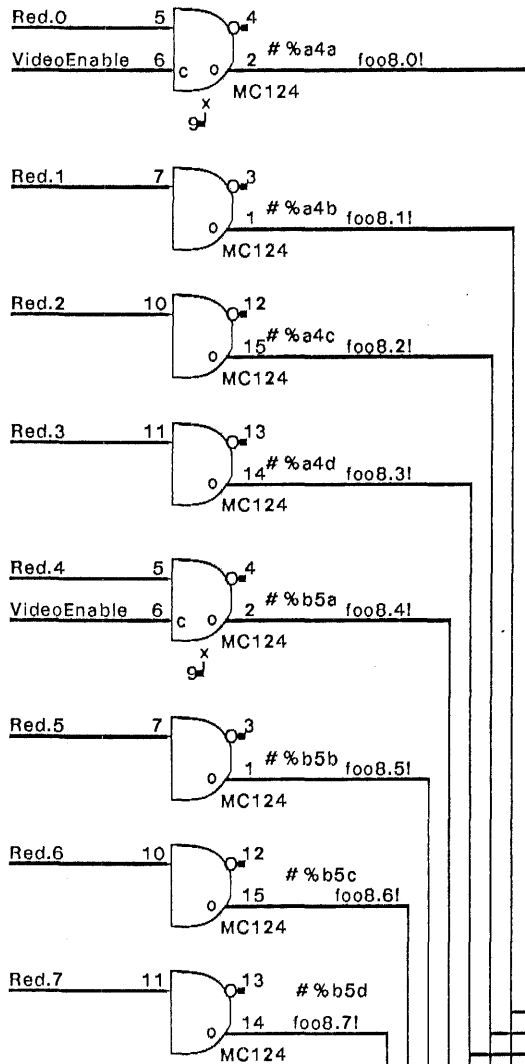
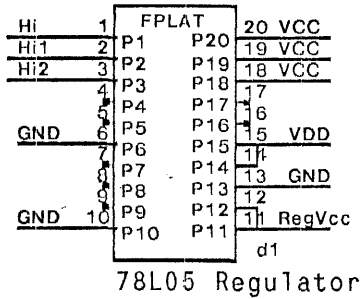






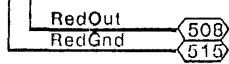


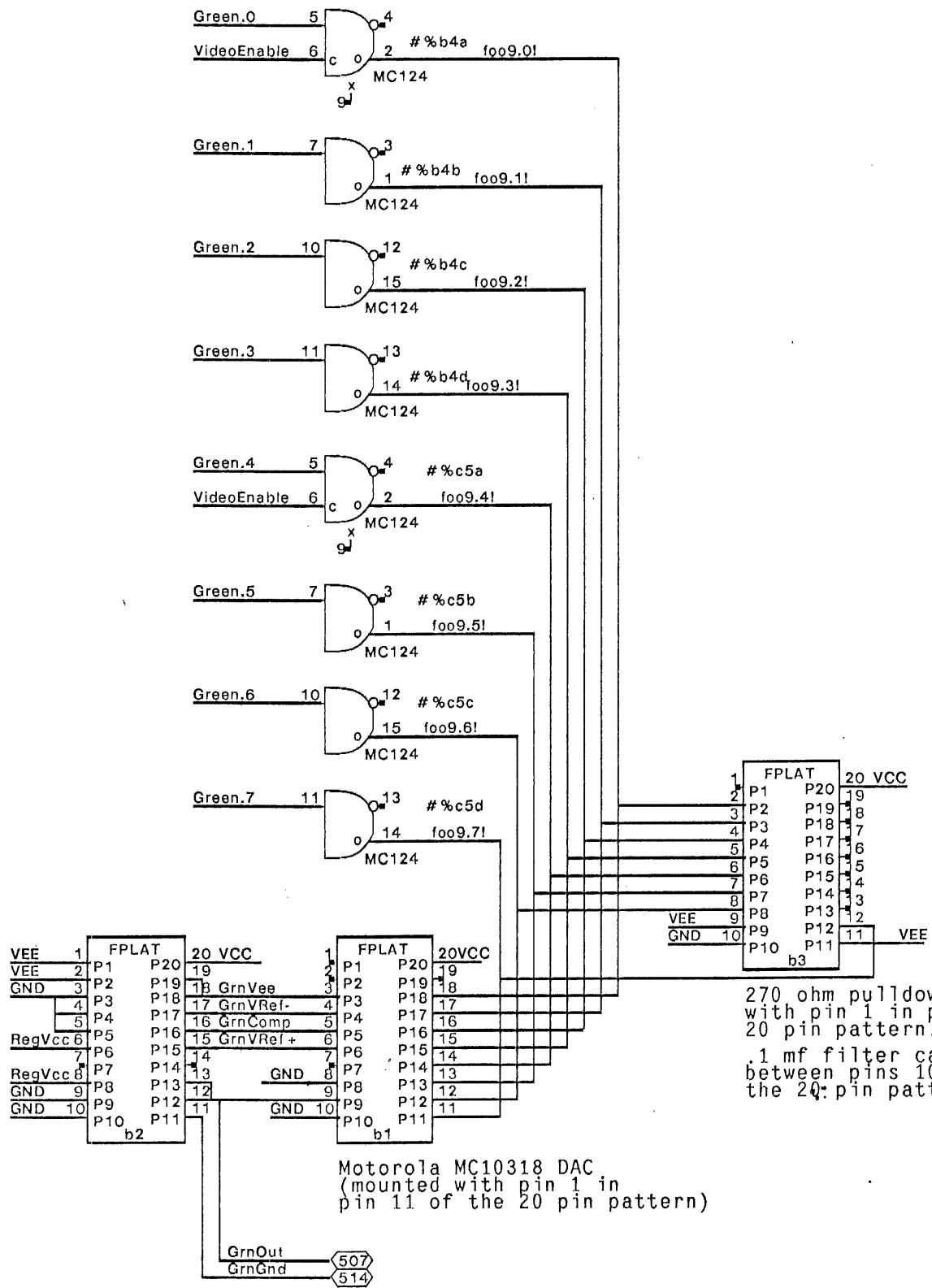




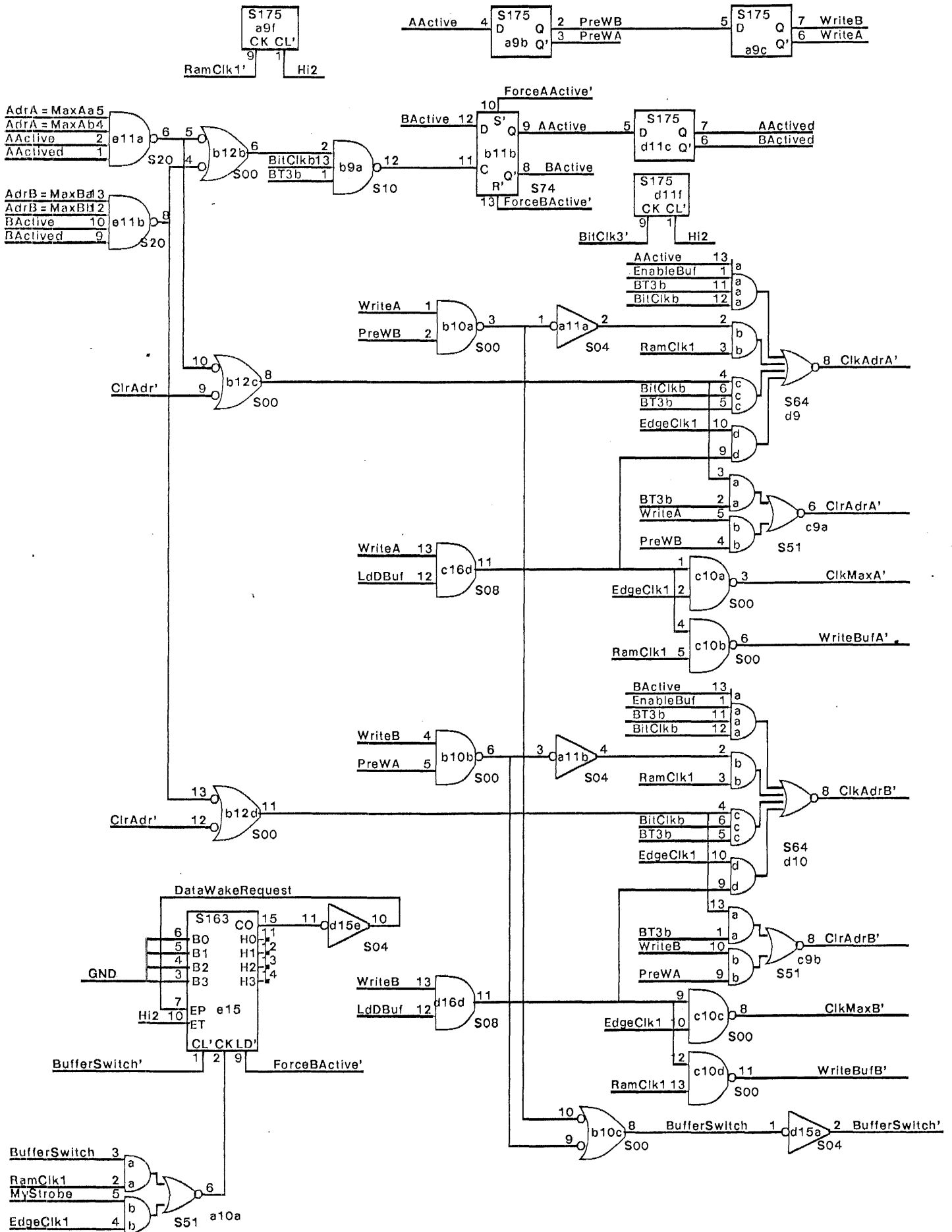
270 ohm pulldowns, mount with pin 1 in pin 12 of 20 pin pattern.  
 .1 mf filter cap. mount between pins 10 and 11 the 20 pin pattern.

Motorola MC10318 DAC (mounted with pin 1 in pin 11 of the 20 pin pattern)





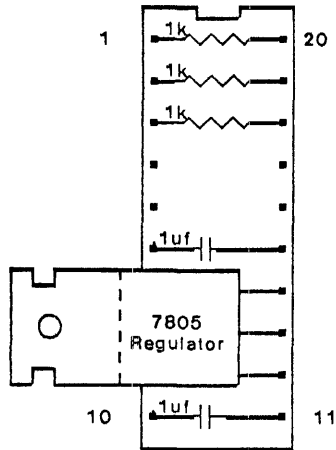




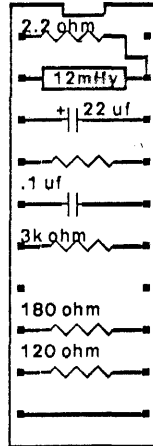
XEROX CSL	Project D0	Sync Generator	File CDC04.sil	Designer Thacker	Rev Ga	Date 9/8/79	Page 01
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Platform d1  
1 required.

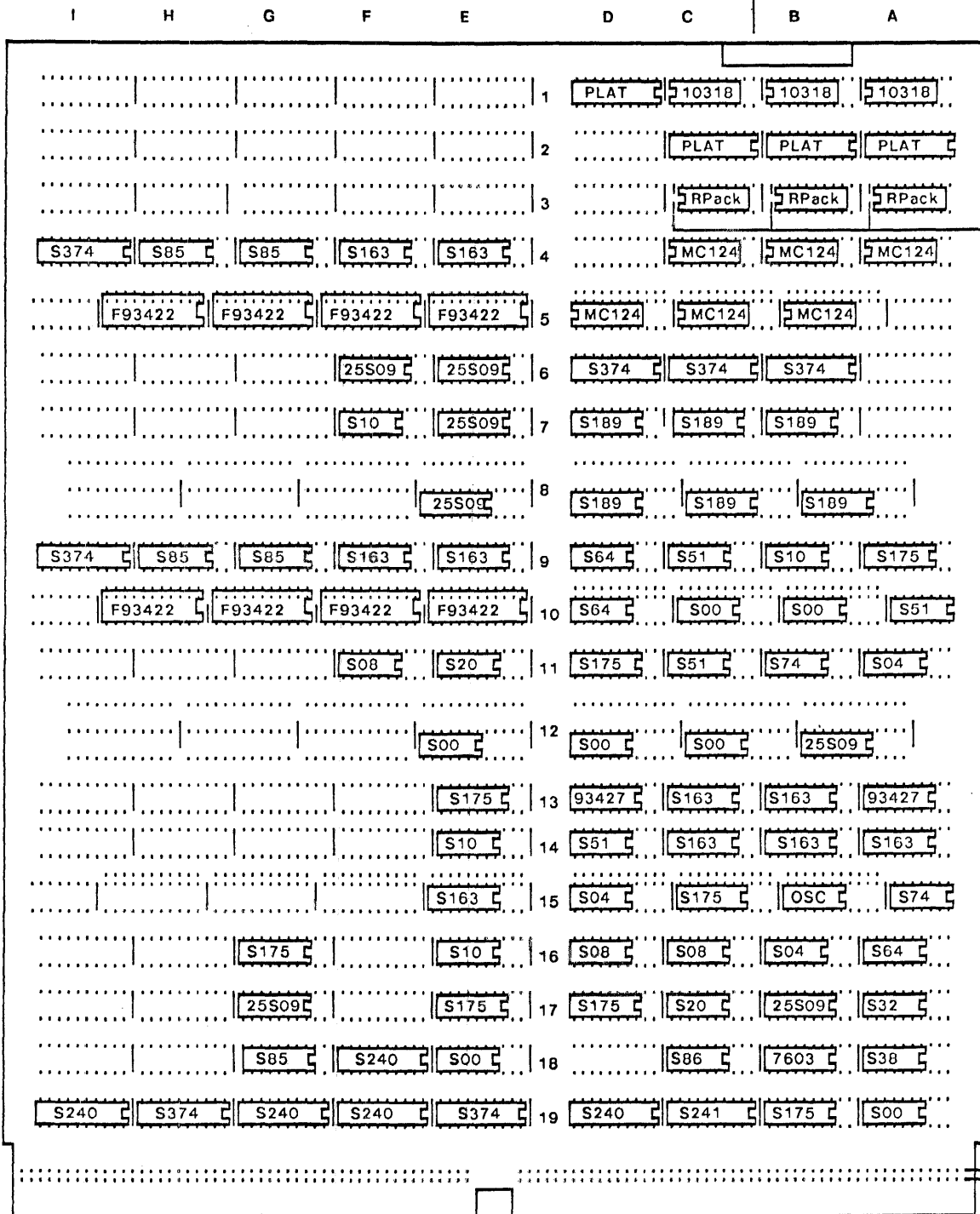


Platform a2, b2, c2  
3 required



Note: remove pins 7,8, and 9 from platform before mounting regulator.

15 Pin FEMALE Connector

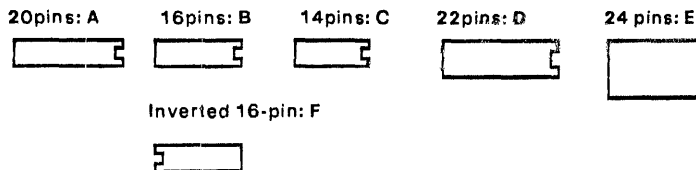


10318 =  
MC10318 DAC

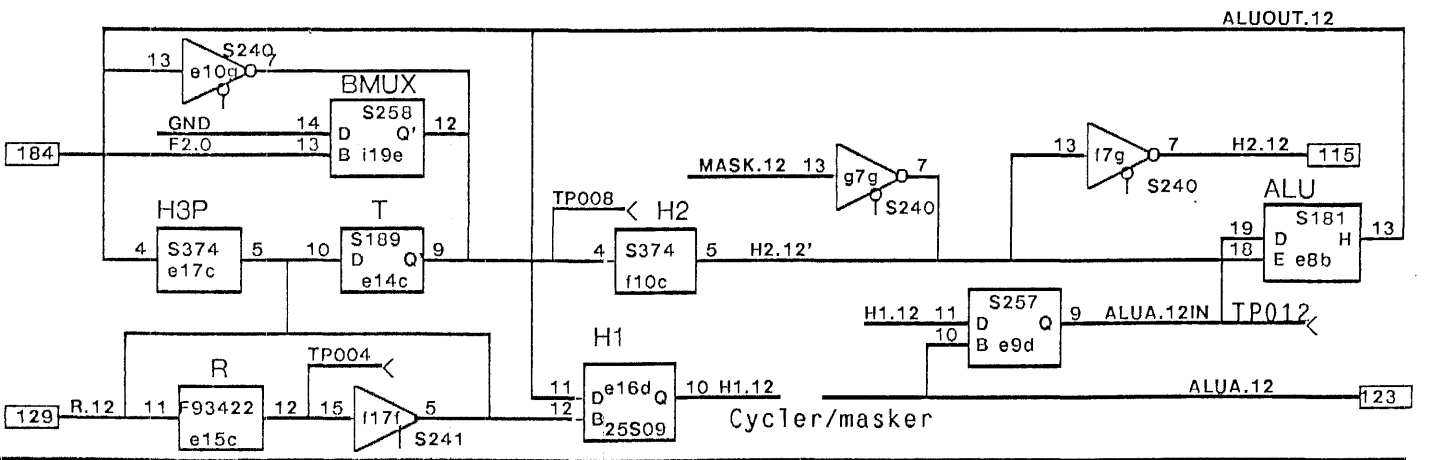
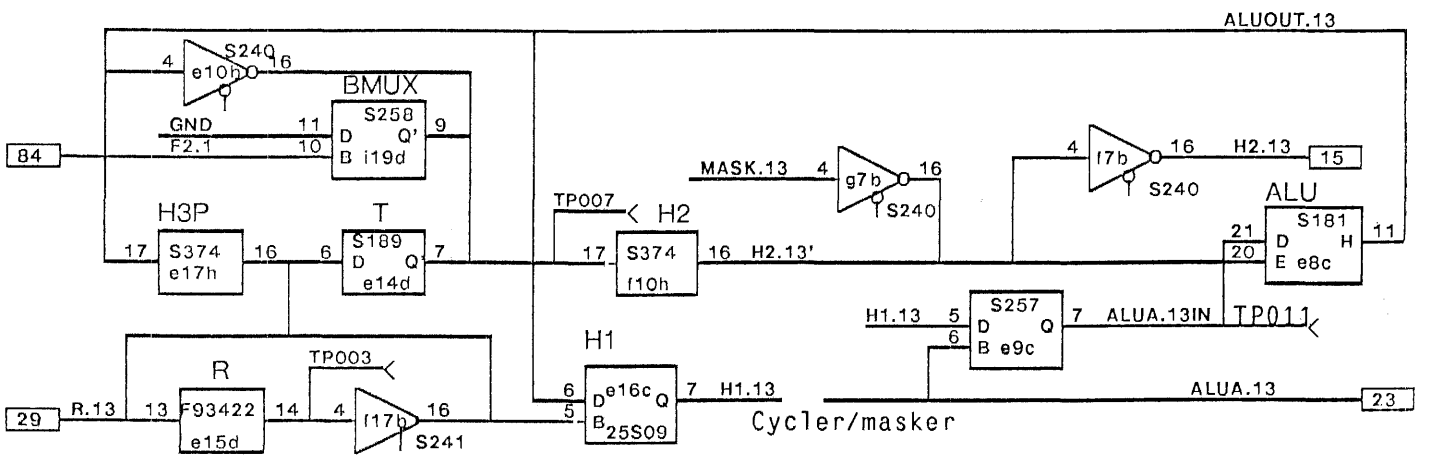
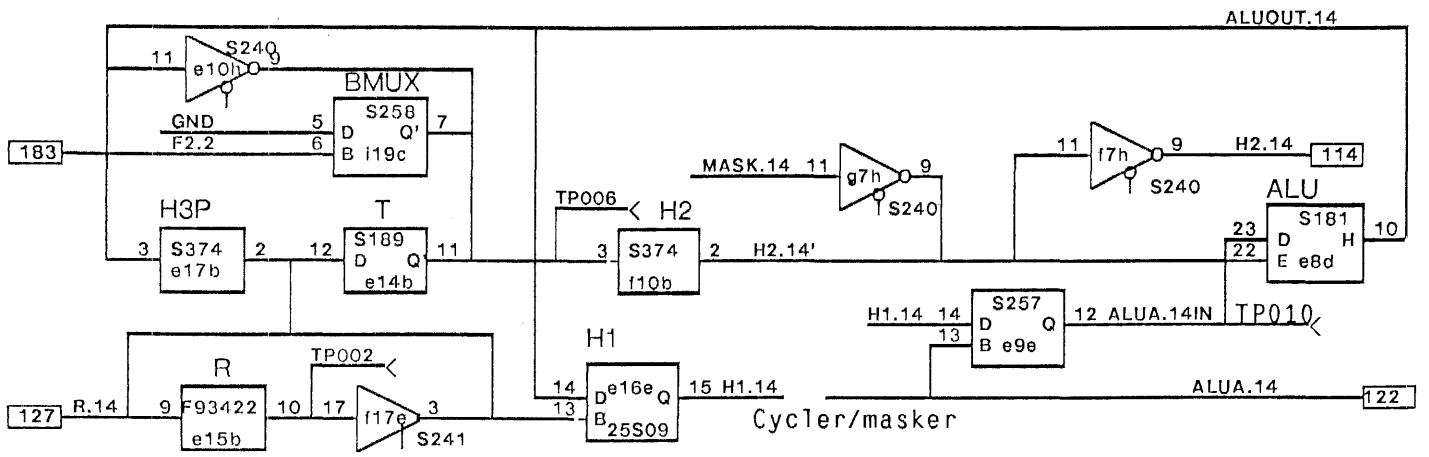
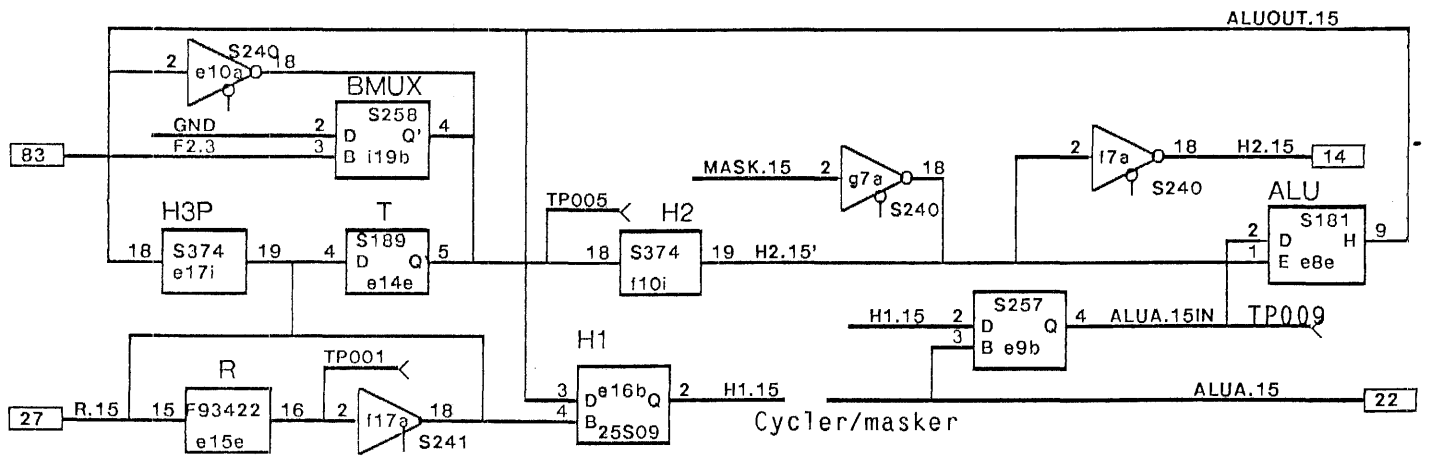
RPack =  
B898-1-R270

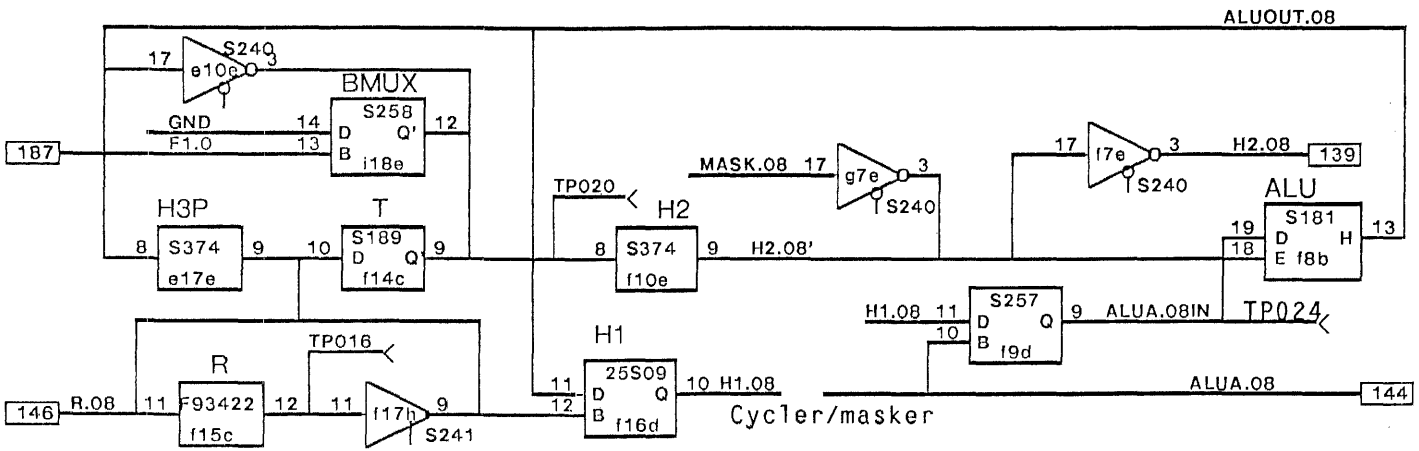
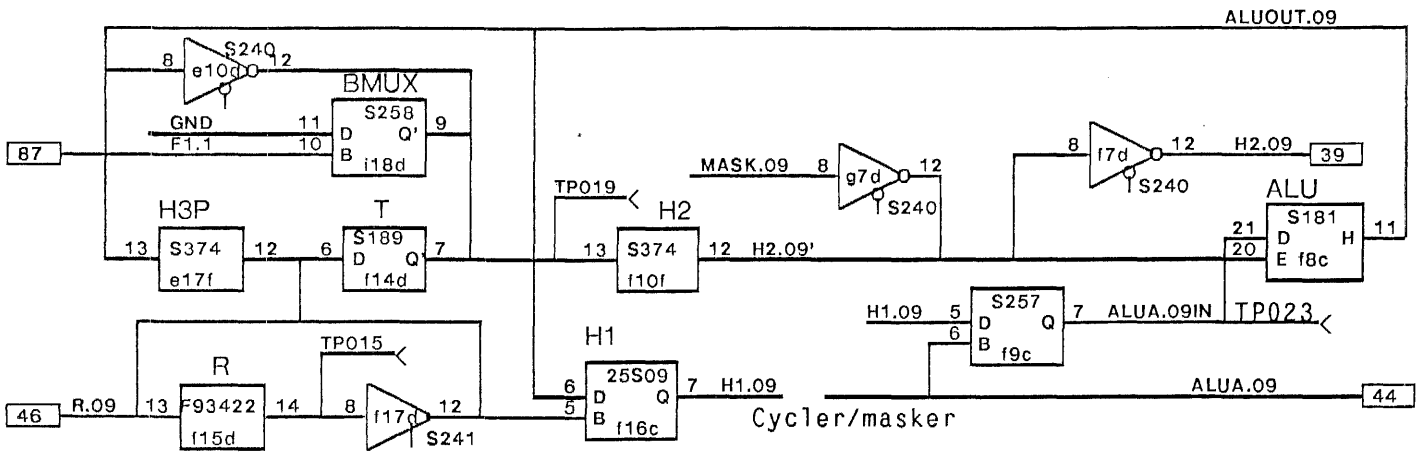
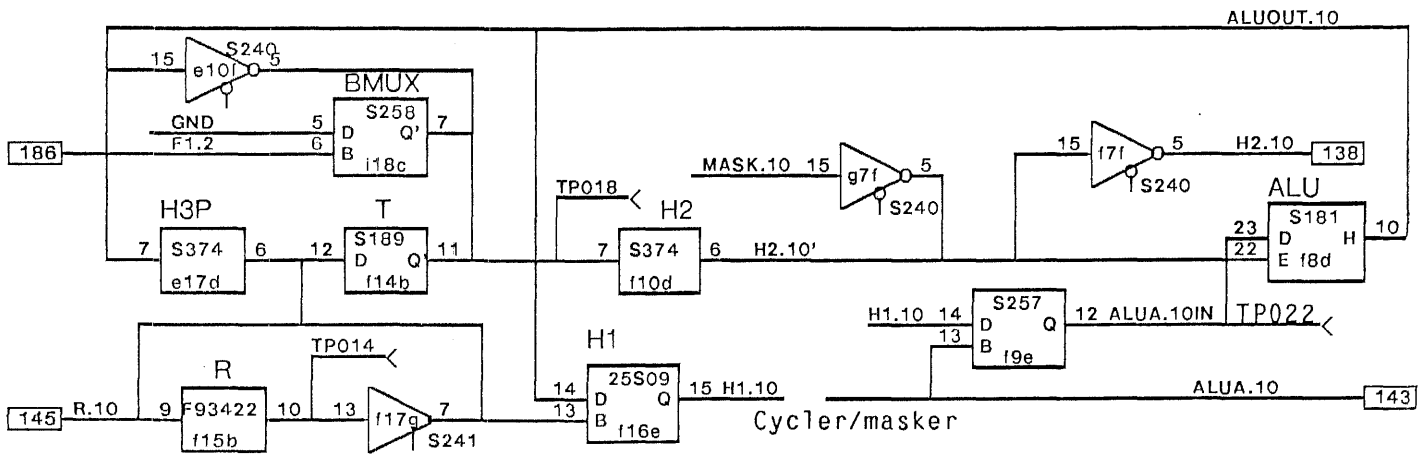
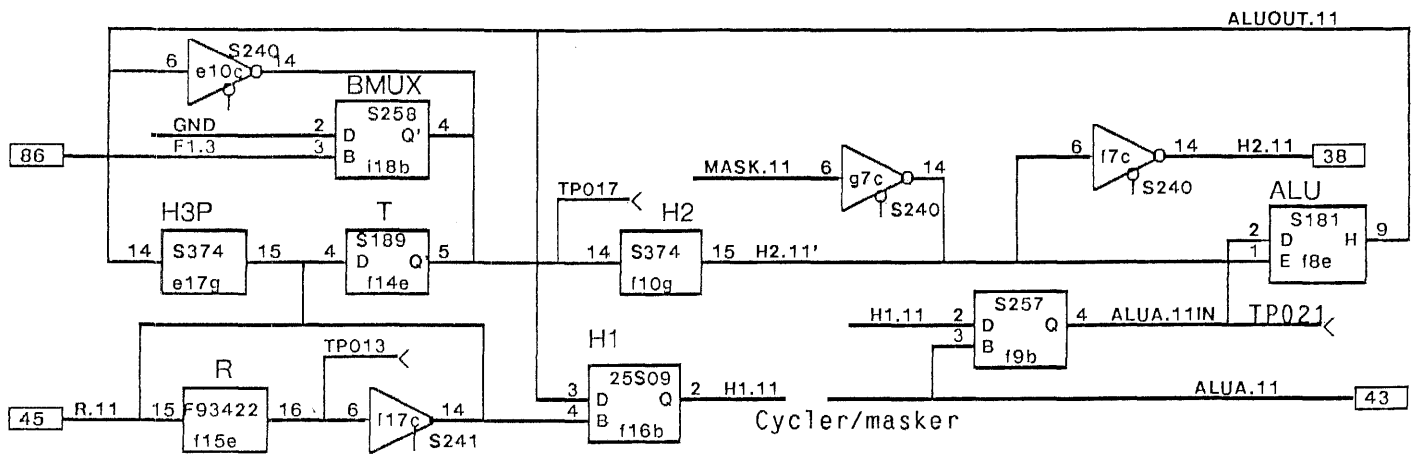
.1uf cap  
3 places

101-200  
1-100



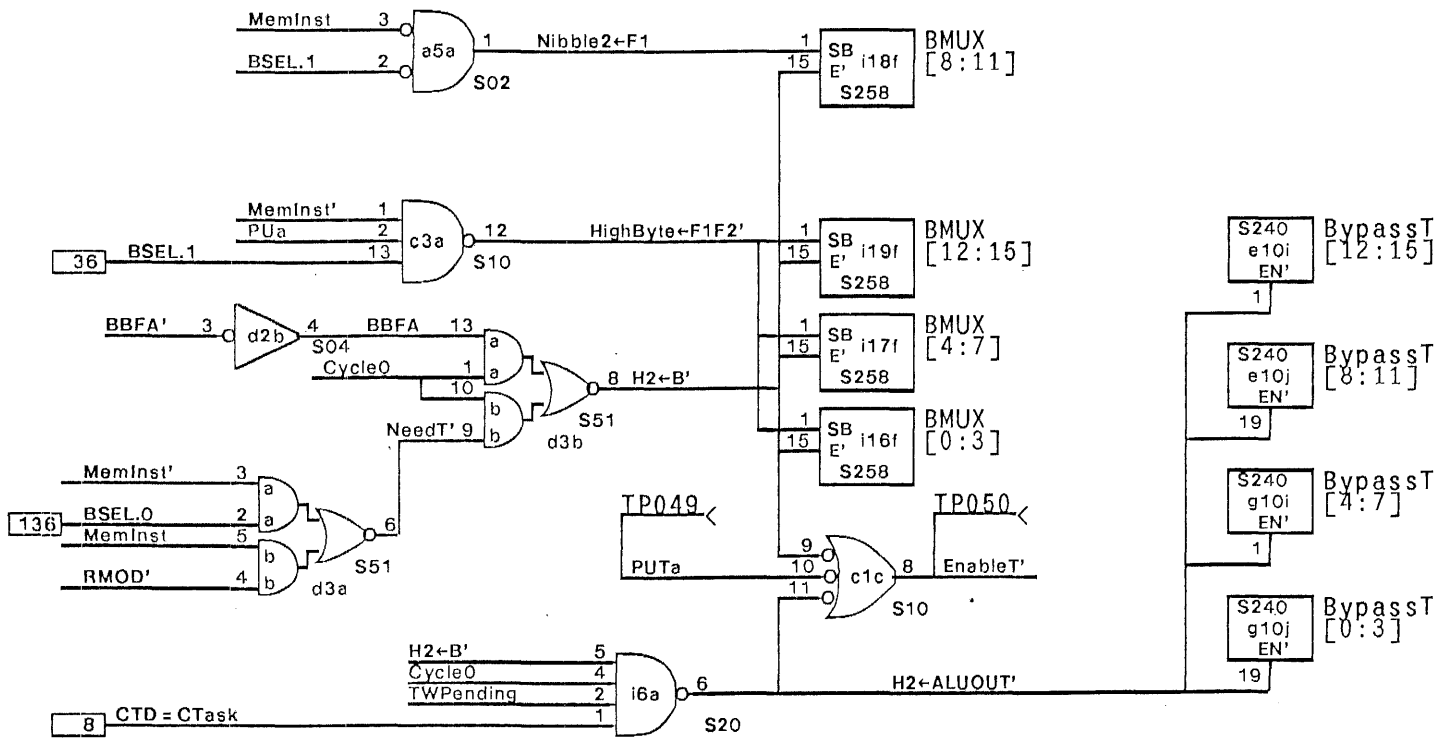
Note: The short vertical lines indicate  
filter capacitor locations.



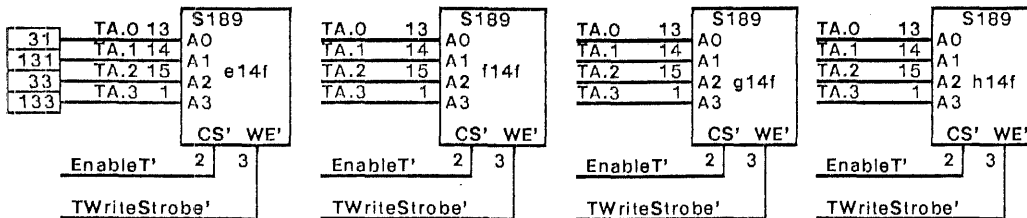




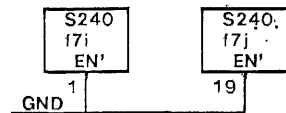


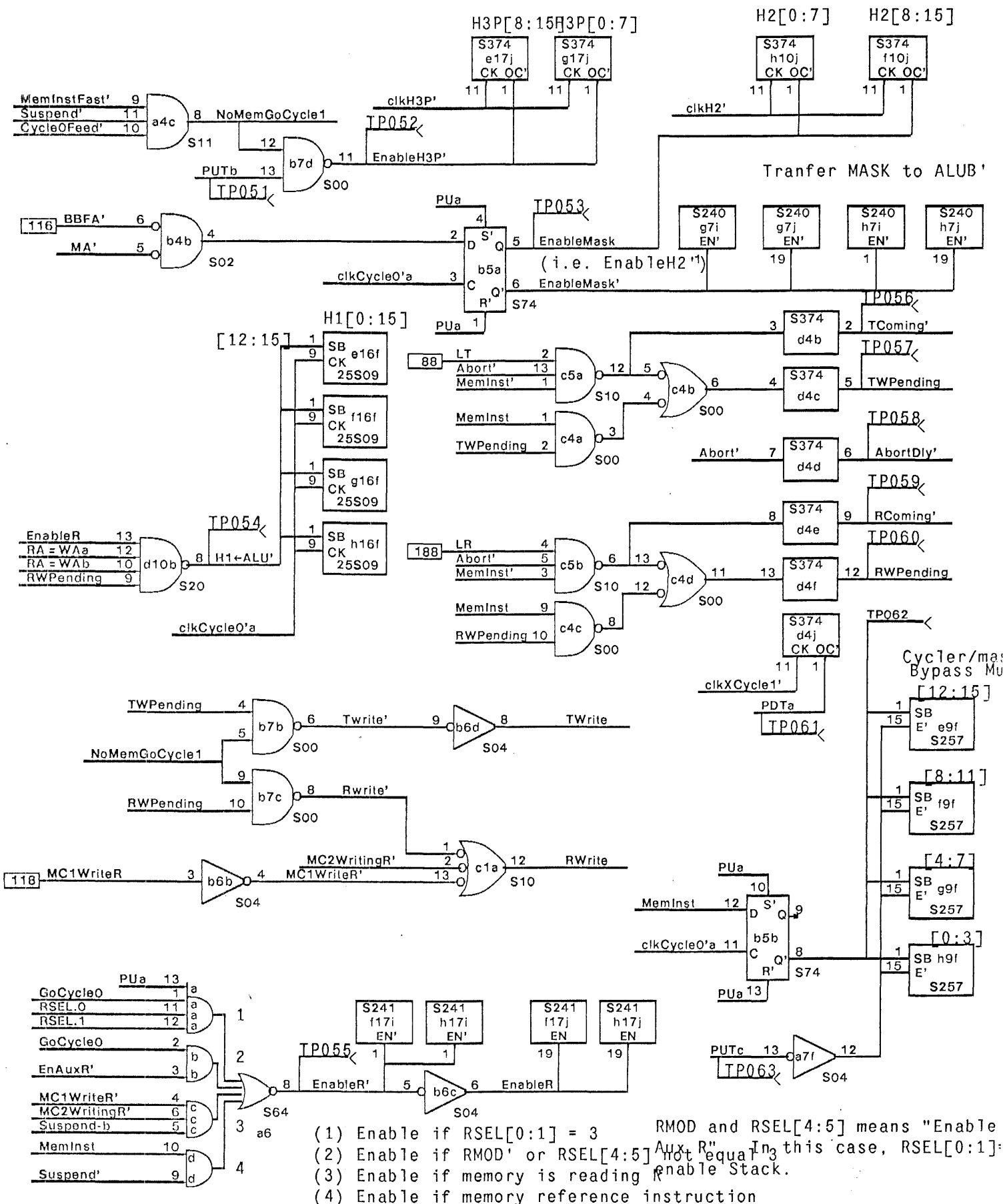


TFILE CONTROL [12:15]    TFILE CONTROL [8:11]    TFILE CONTROL [4:7]    TFILE CONTROL [0:3]

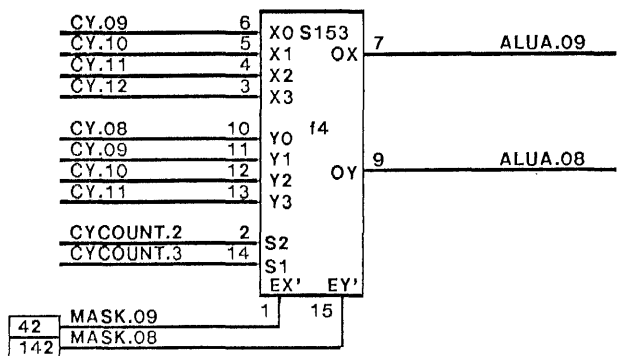
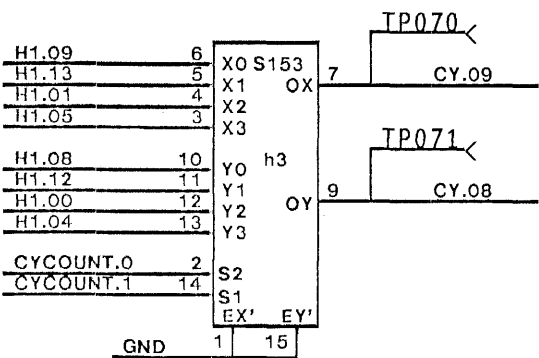
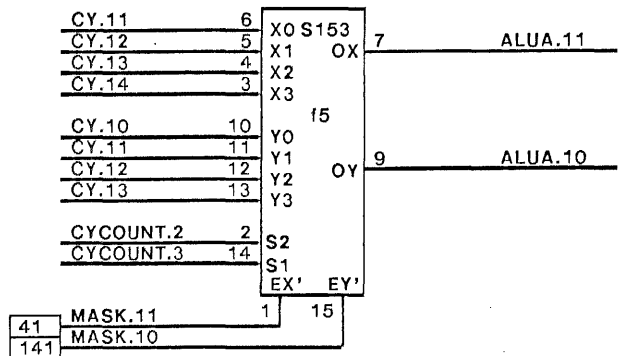
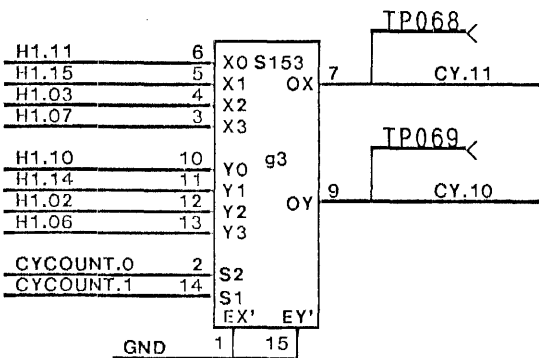
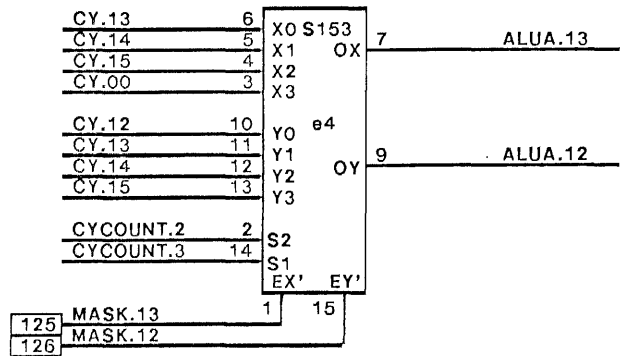
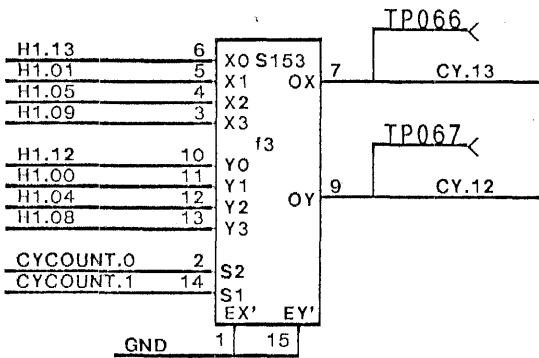
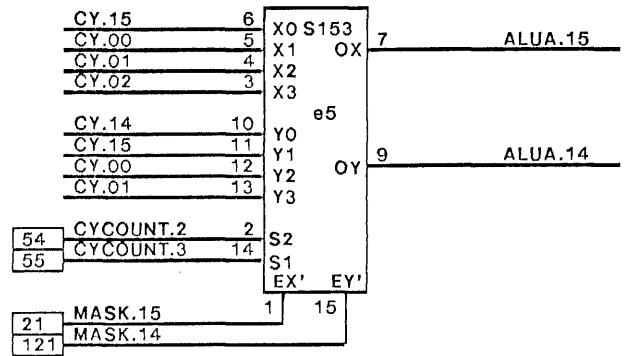
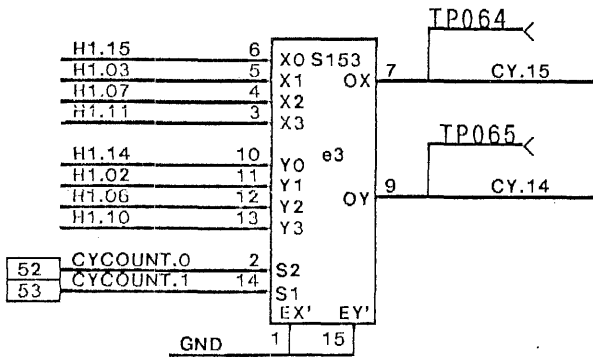


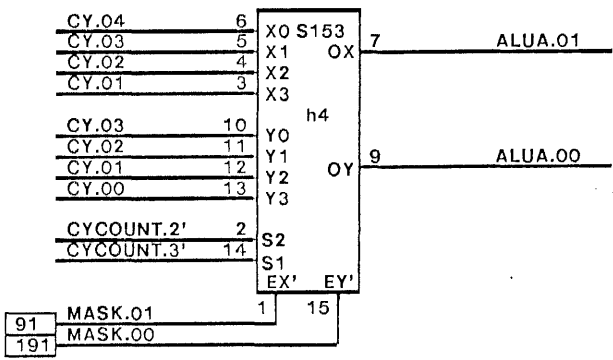
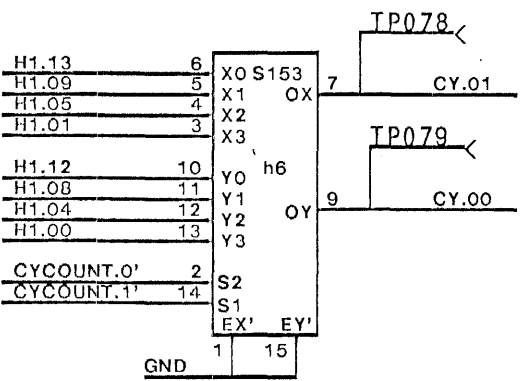
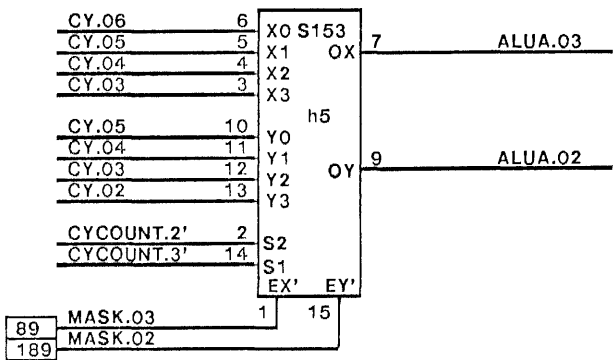
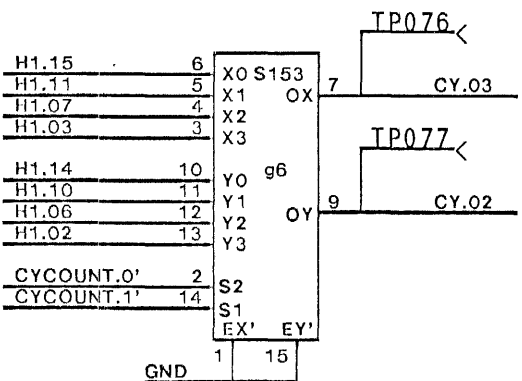
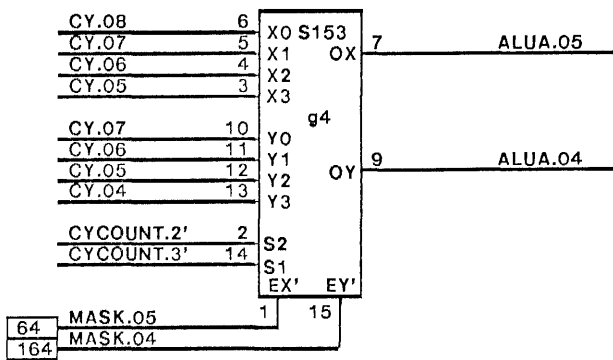
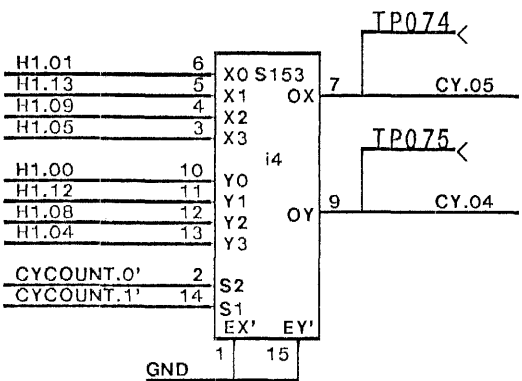
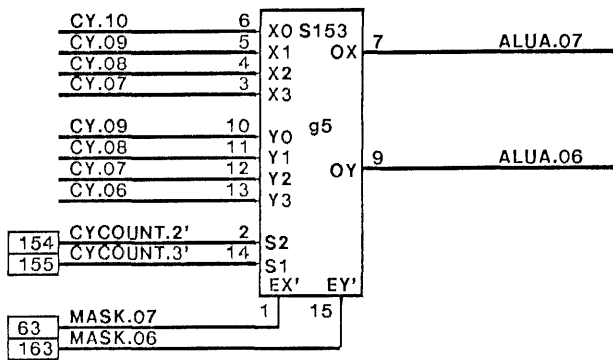
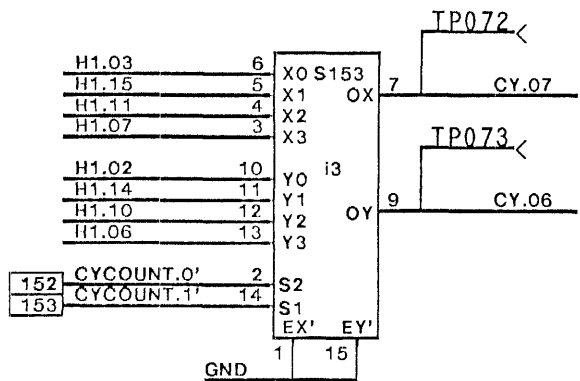
H2.xx Buffer Enables

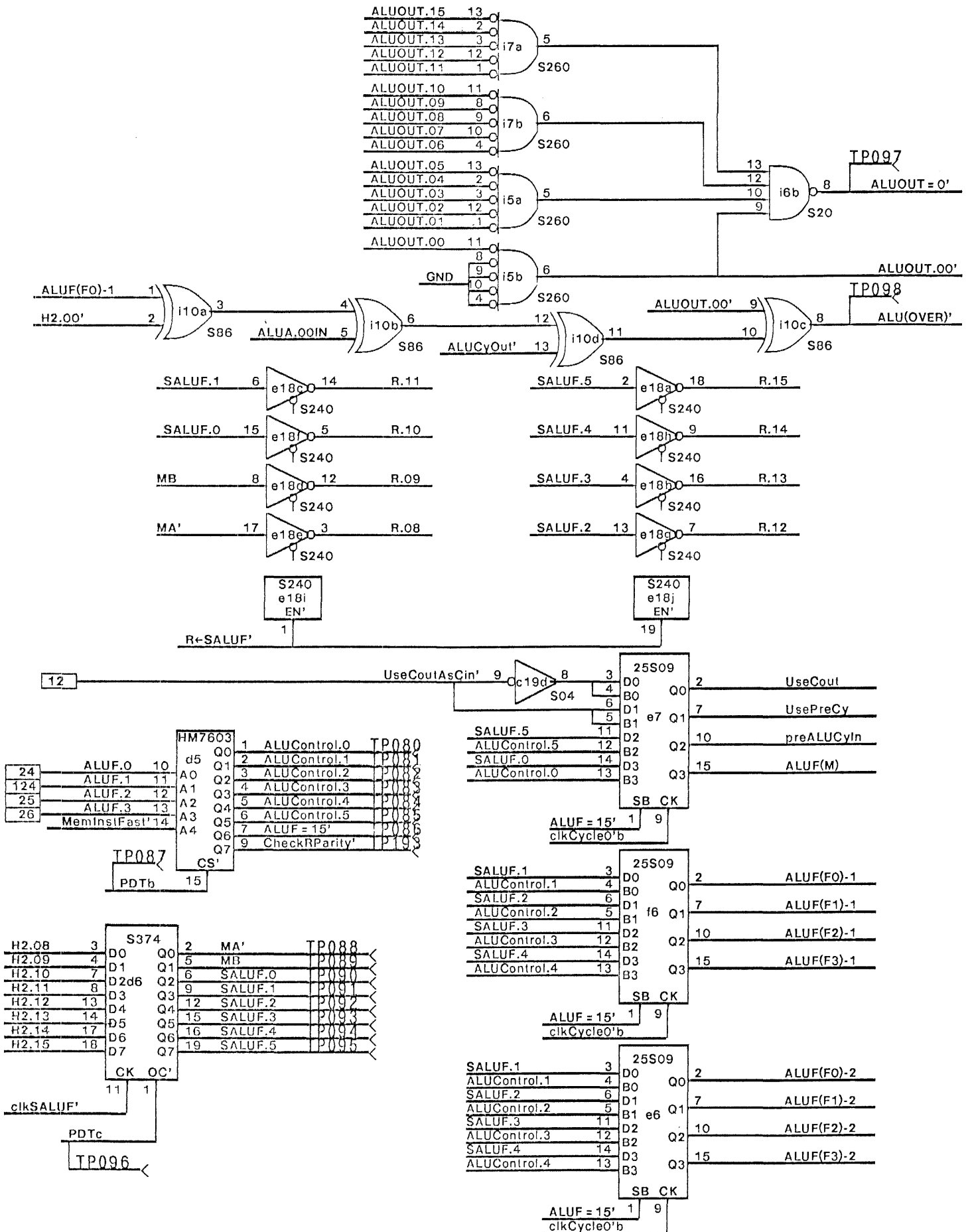


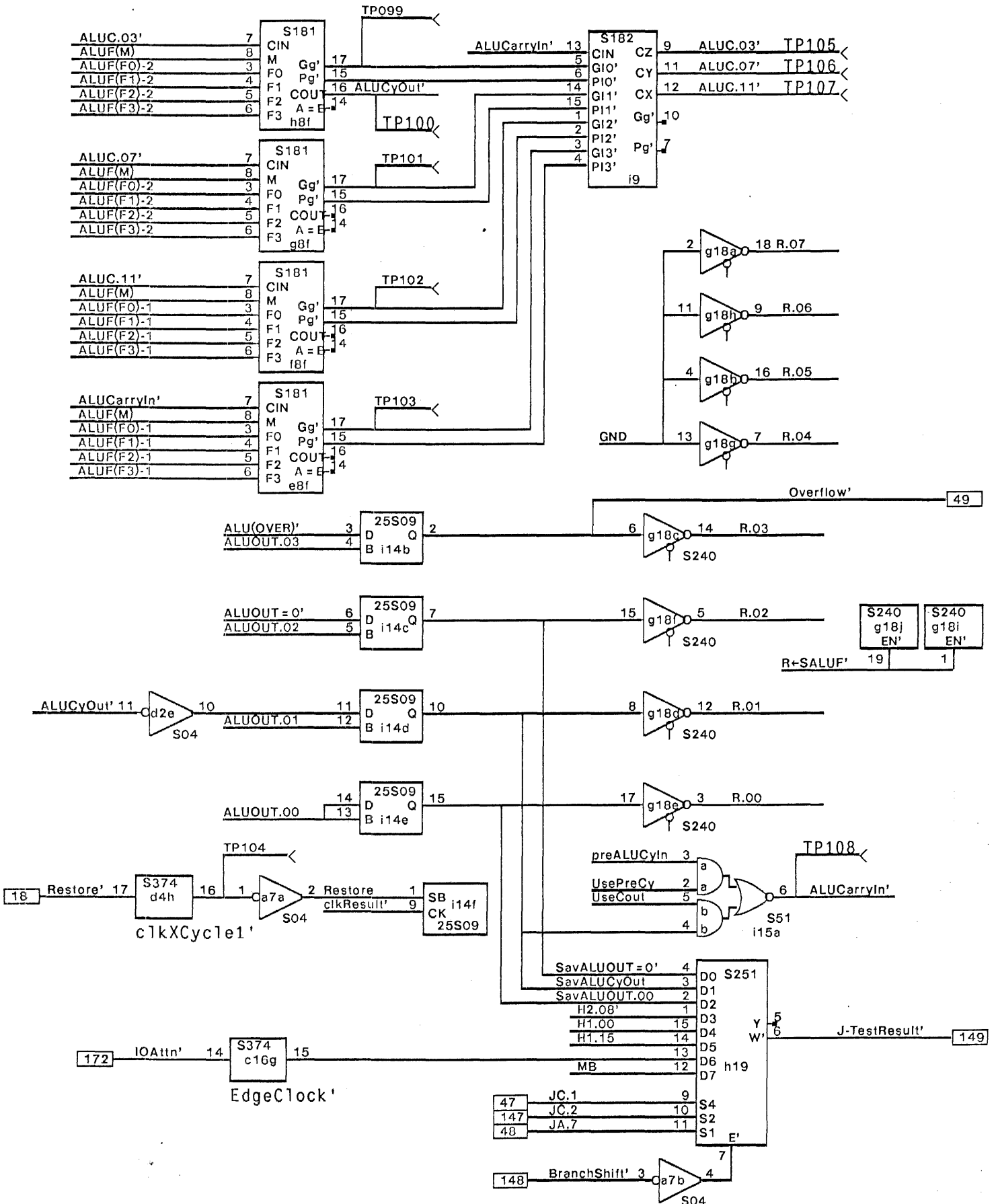


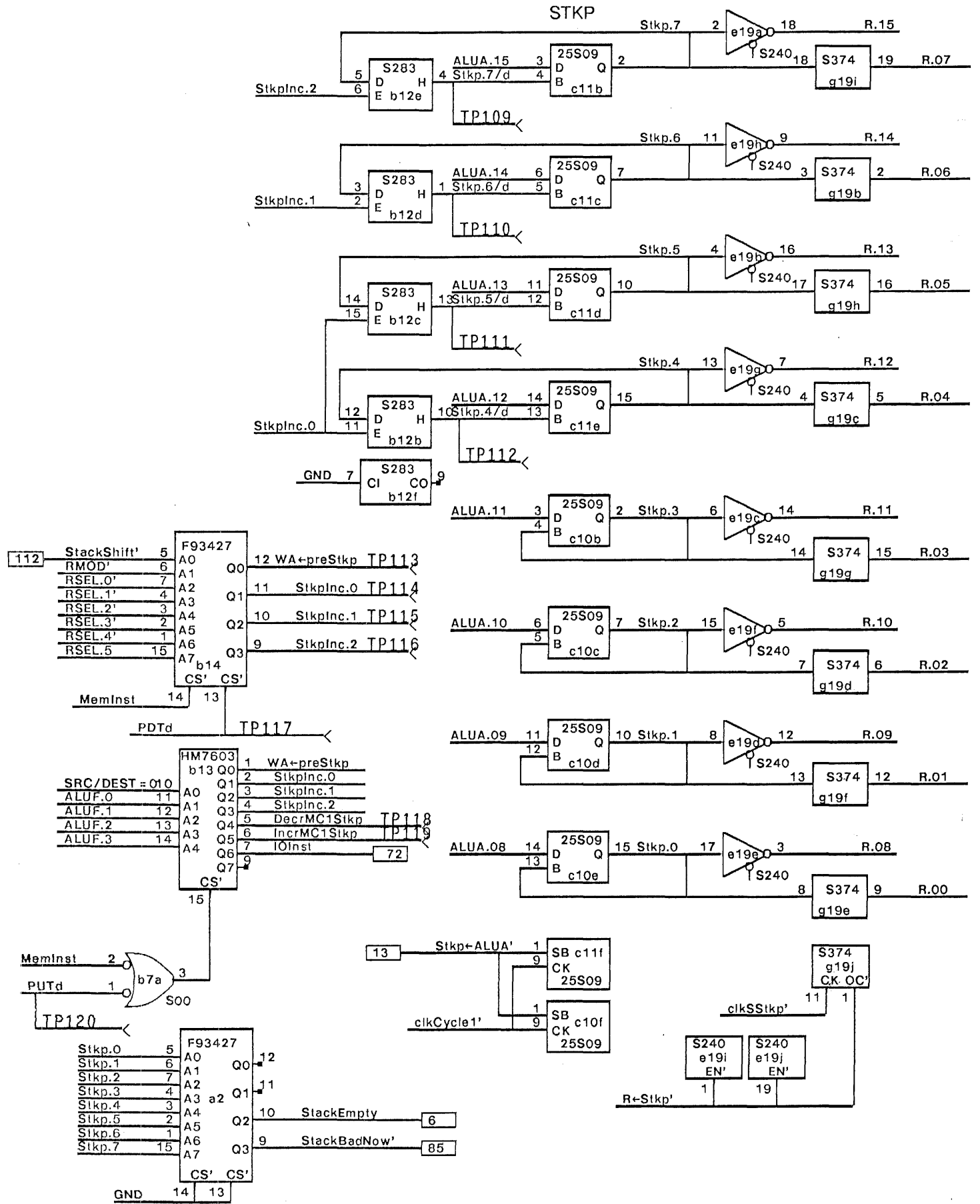




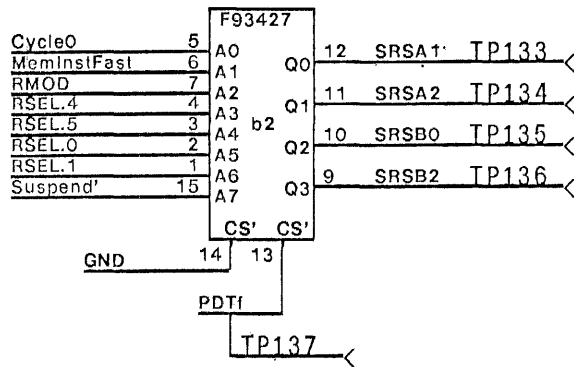
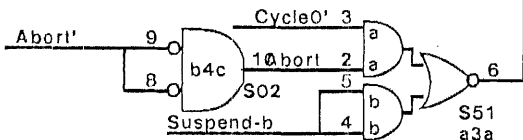
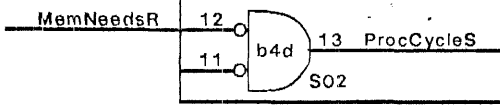
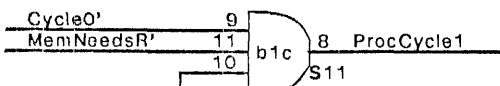
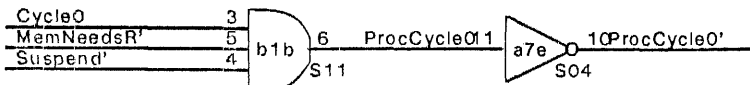
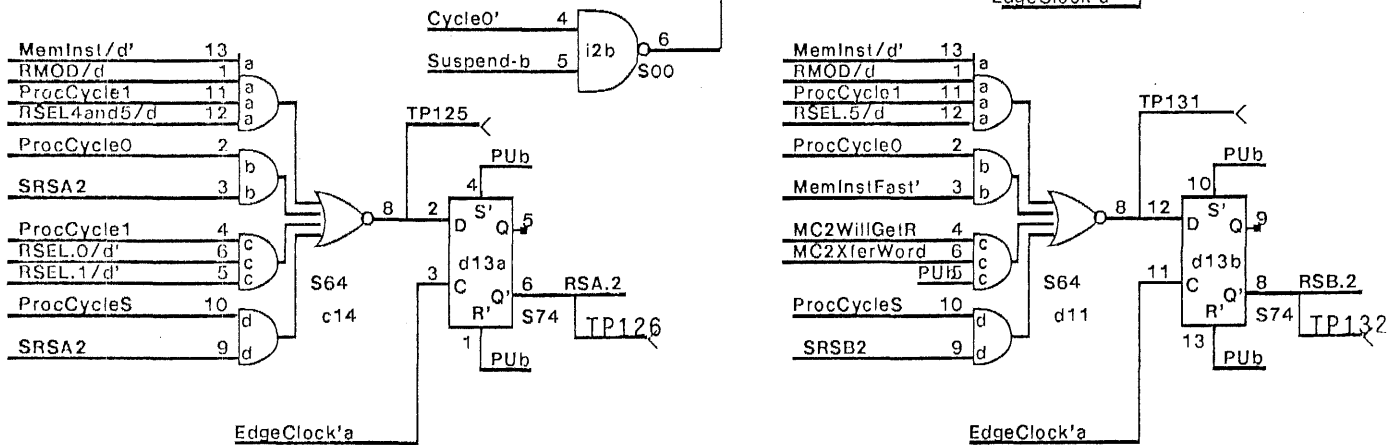
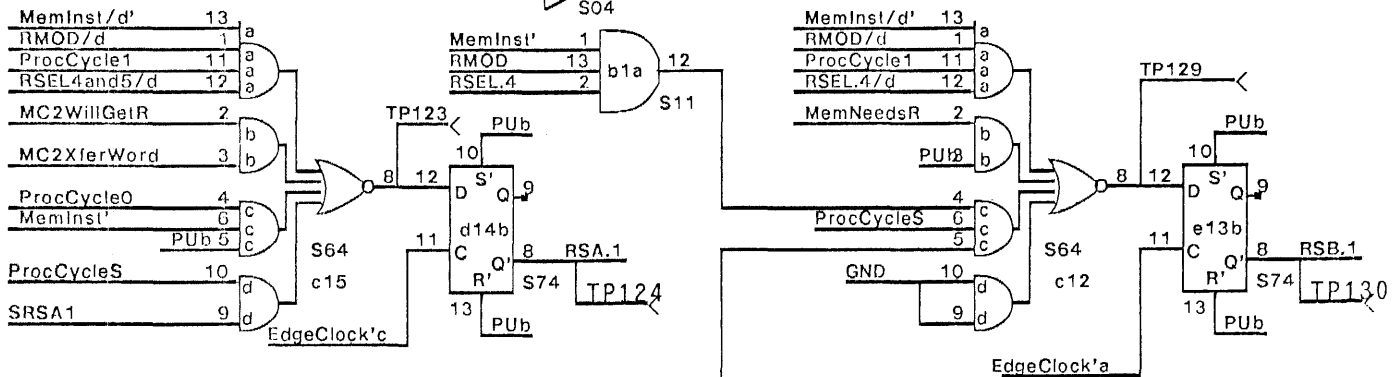
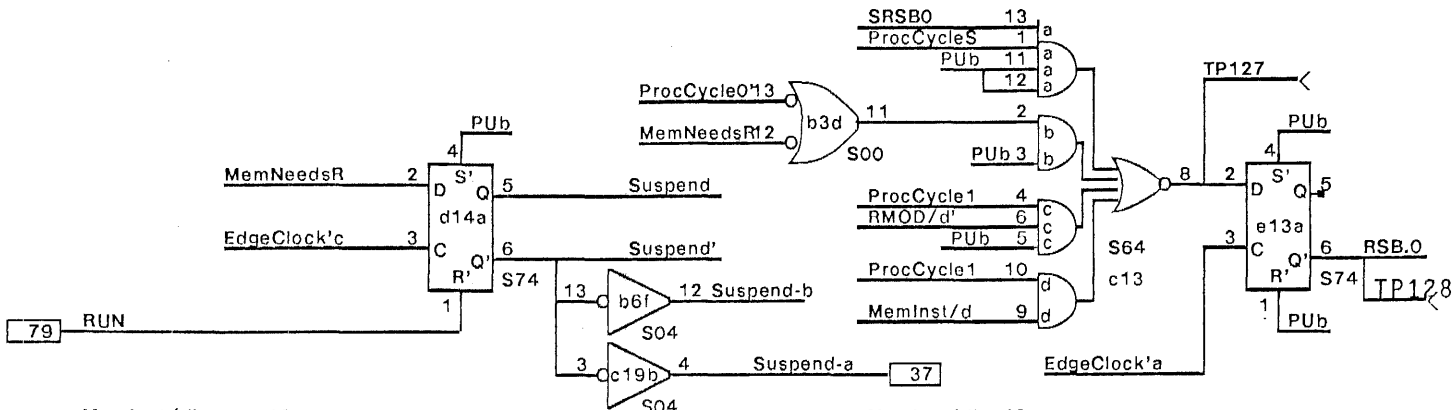


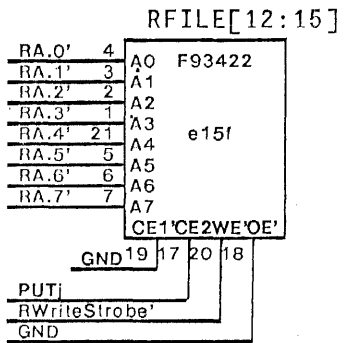
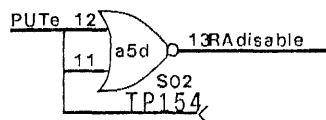
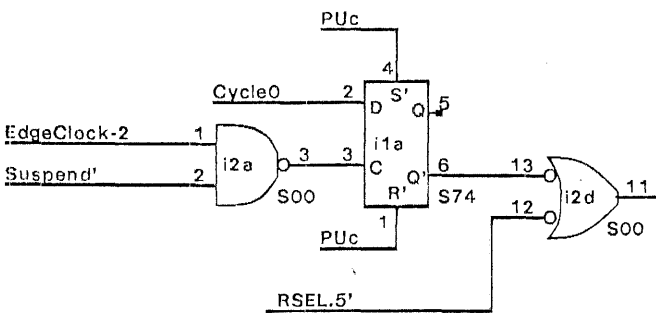
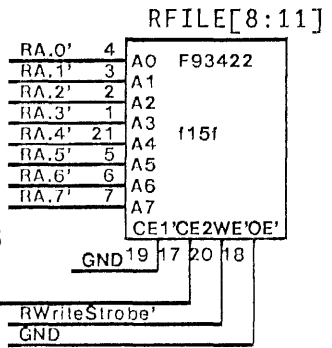
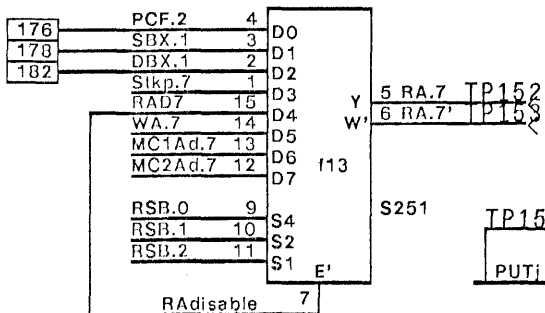
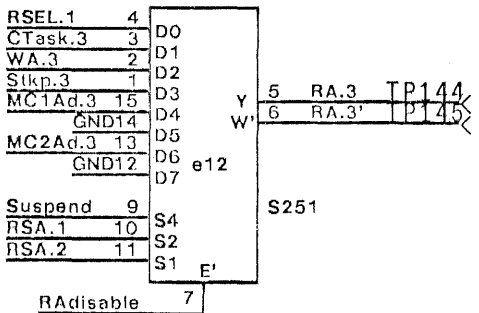
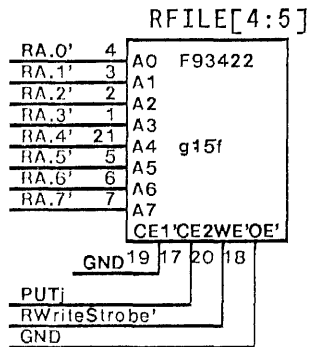
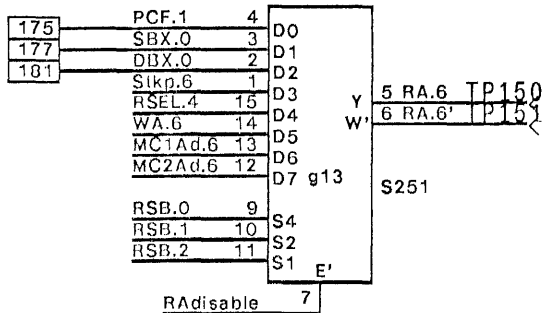
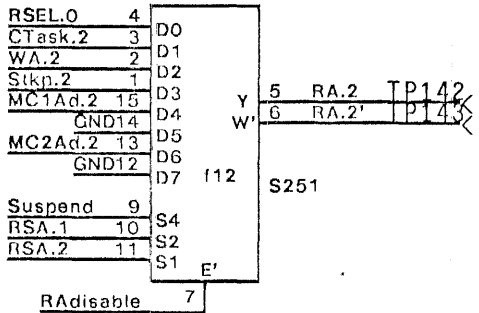
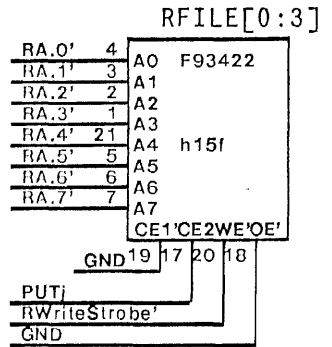
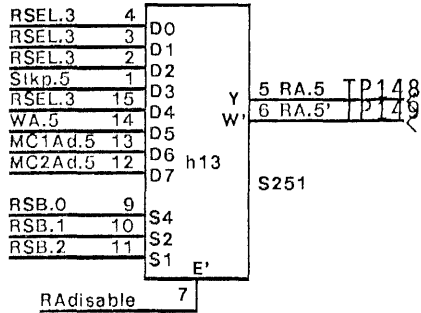
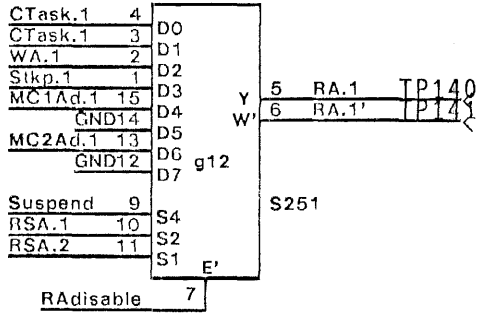
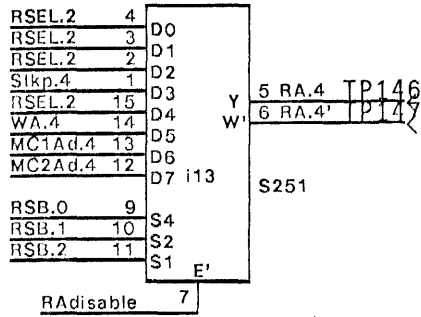
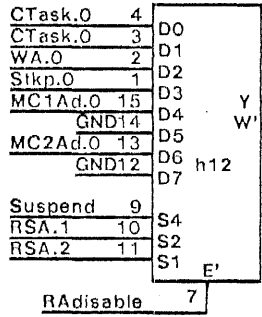




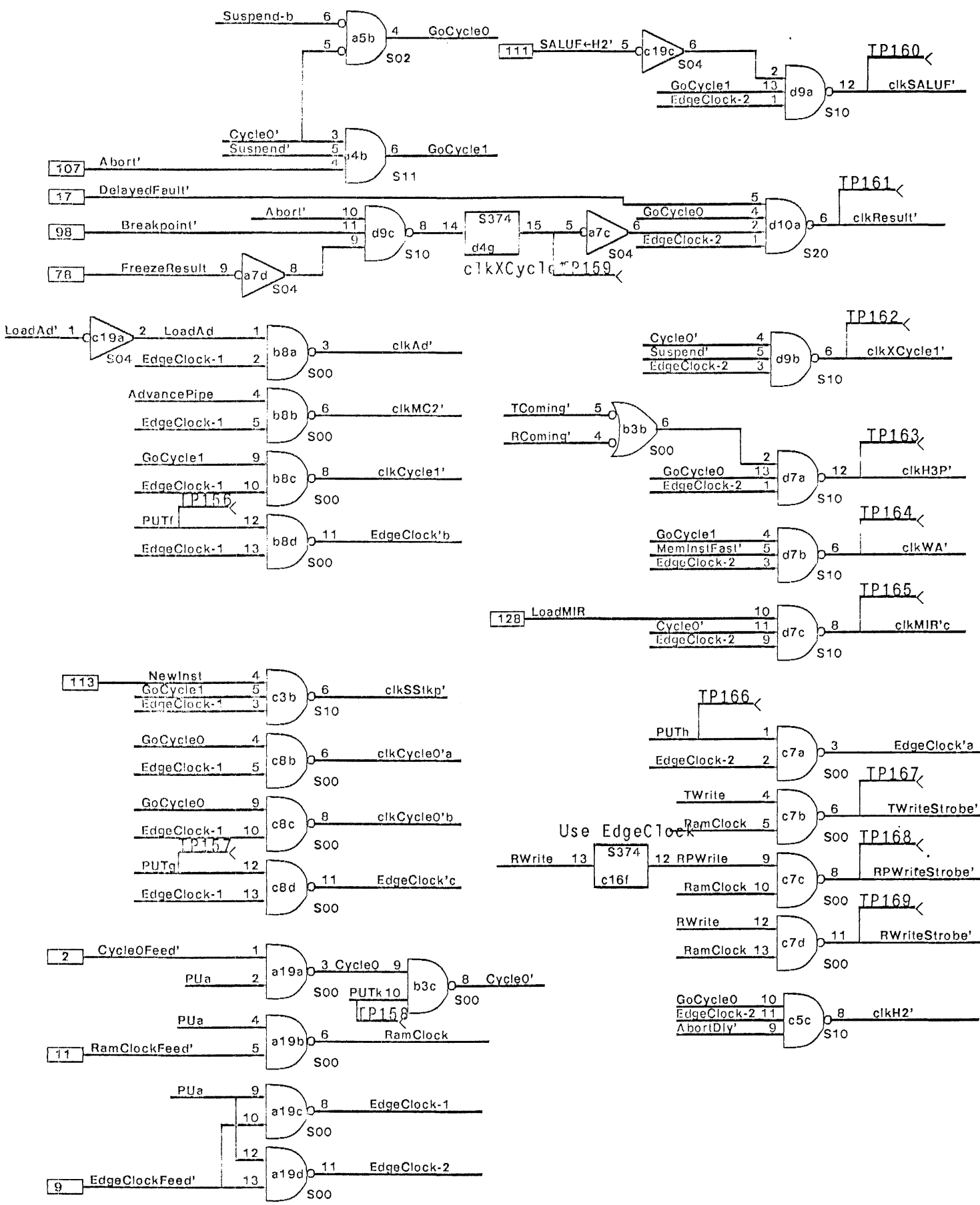


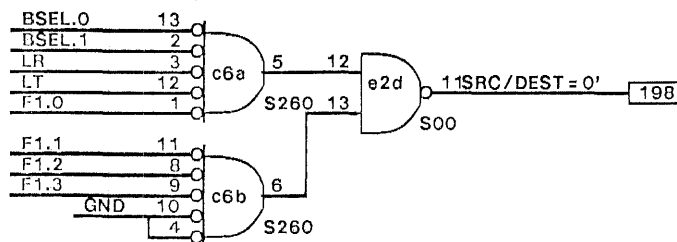
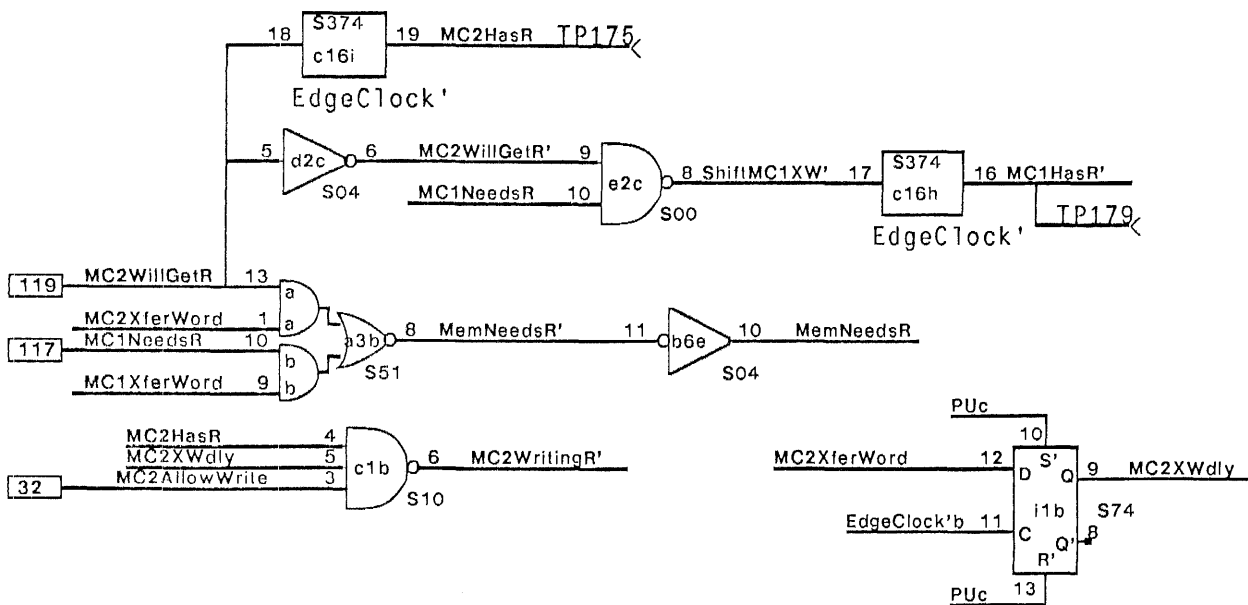
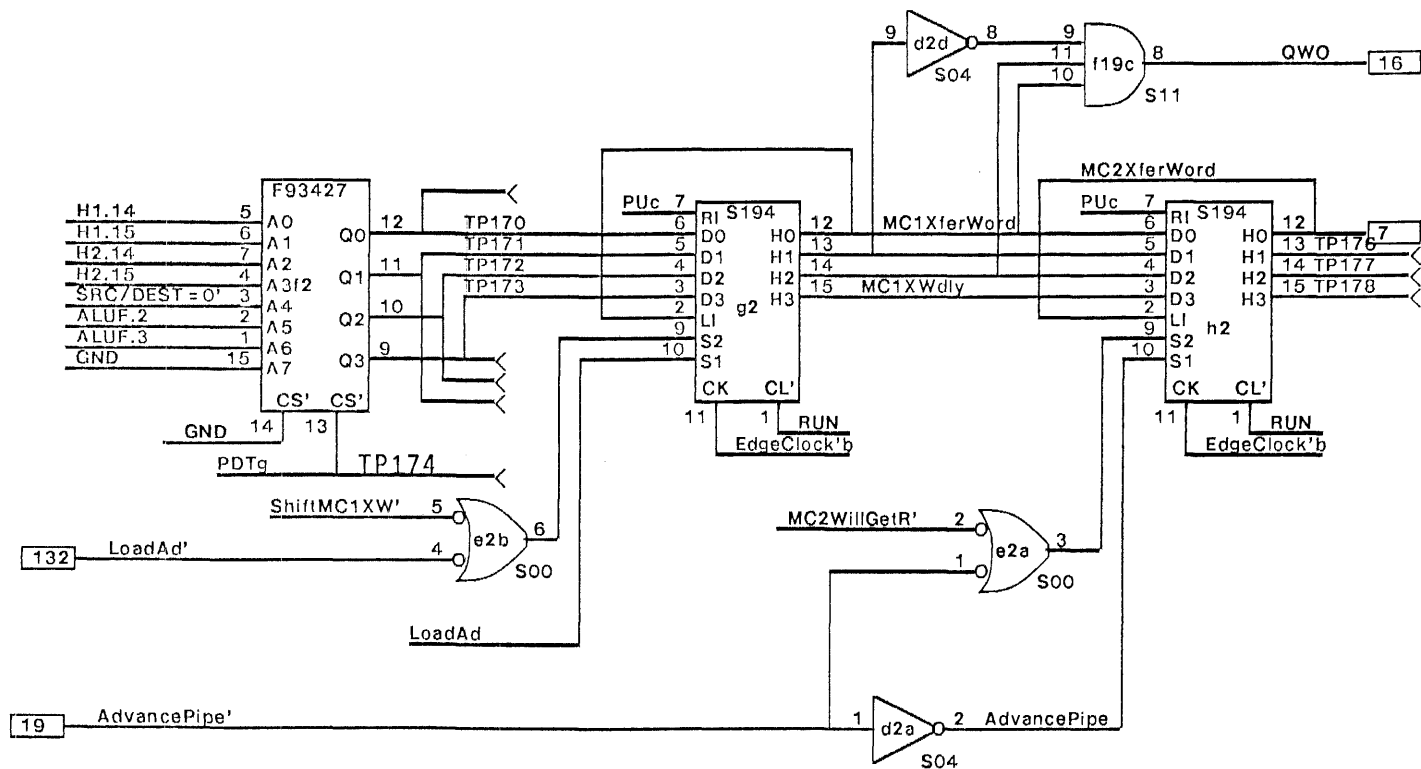


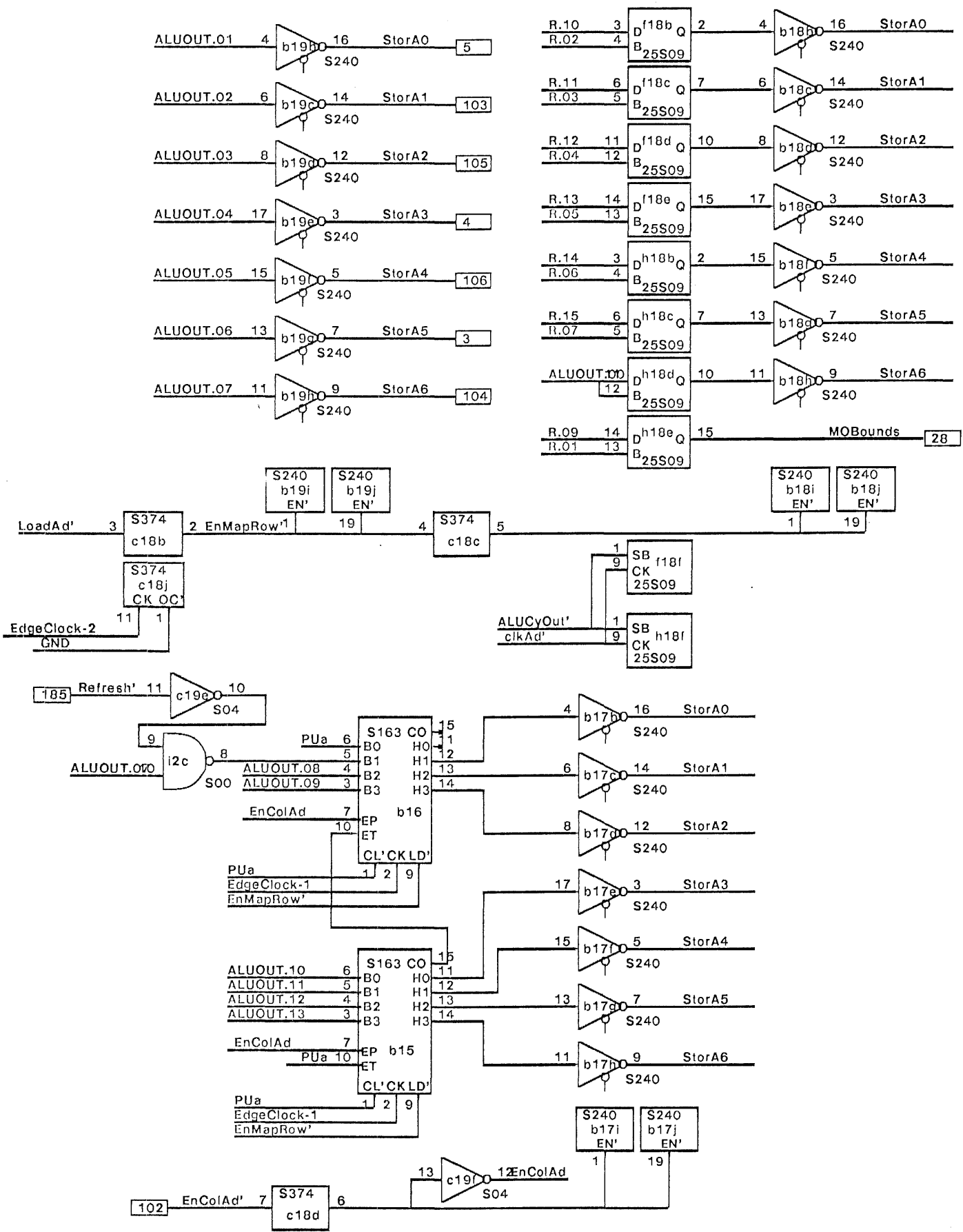


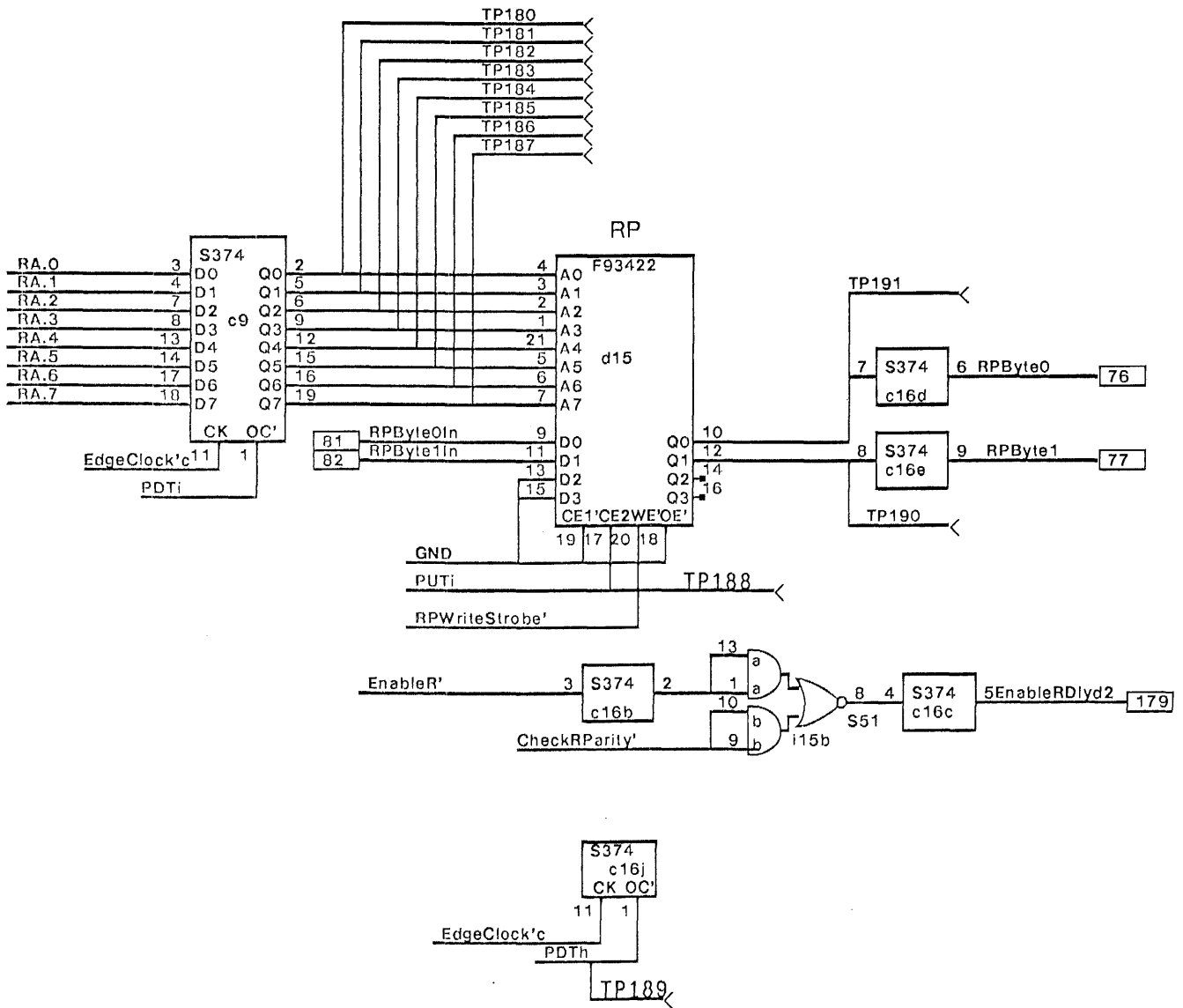


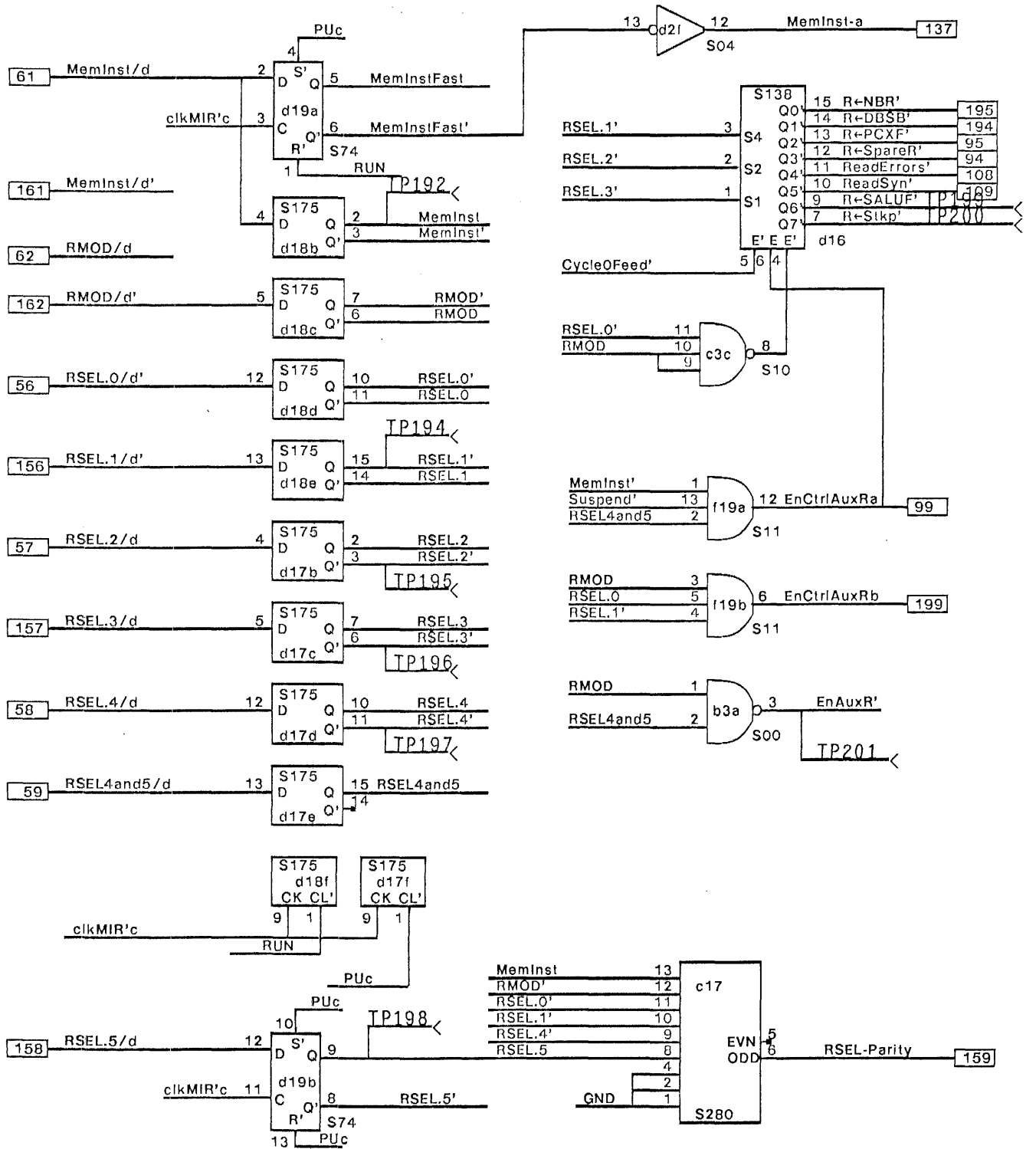


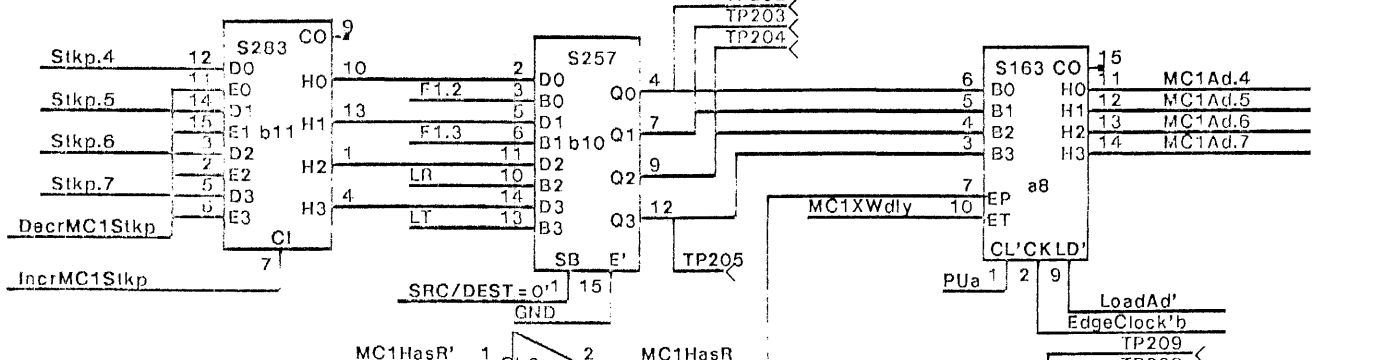
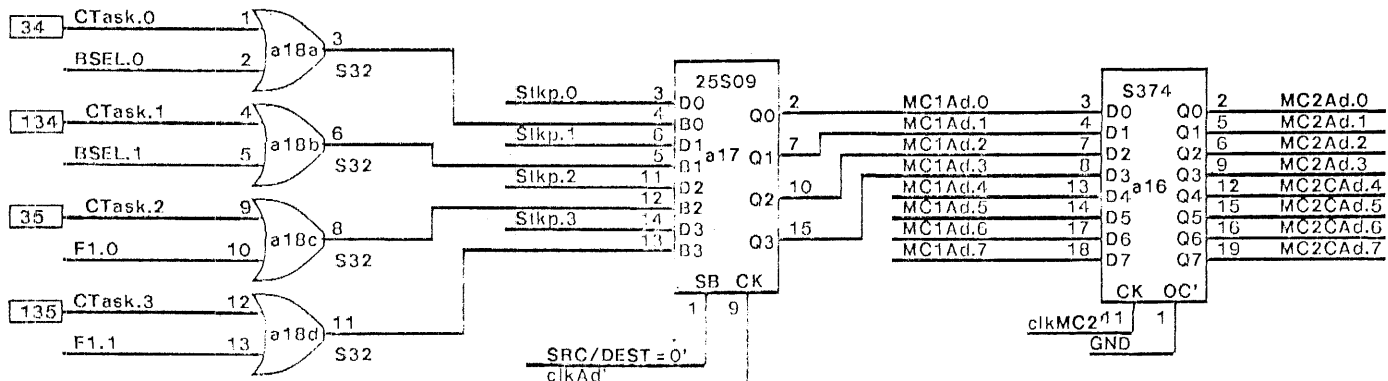




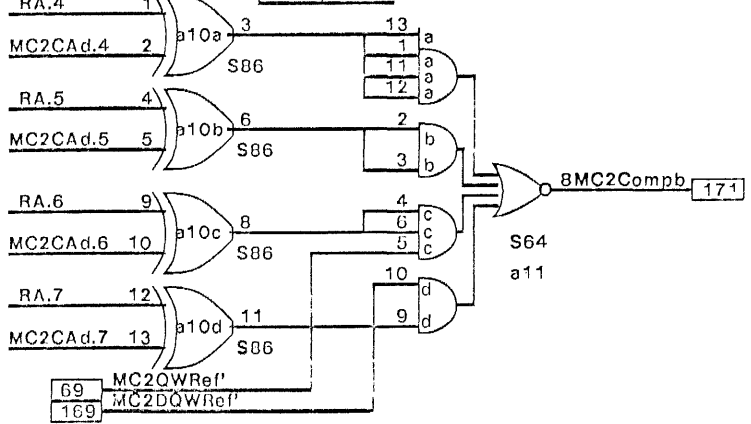
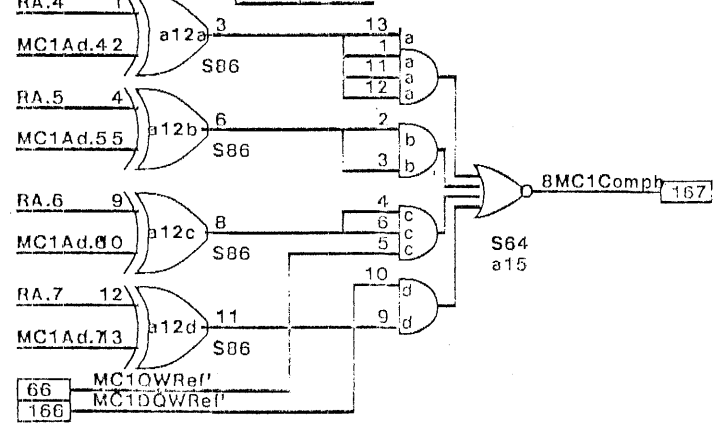
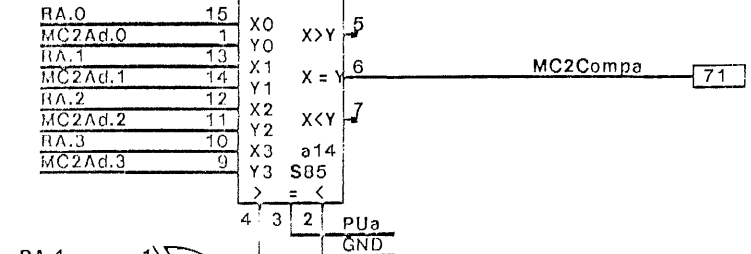
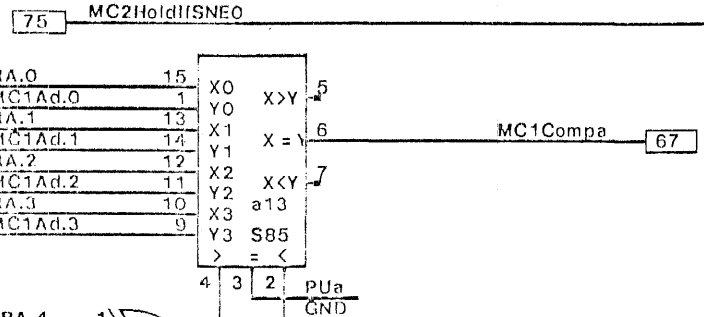
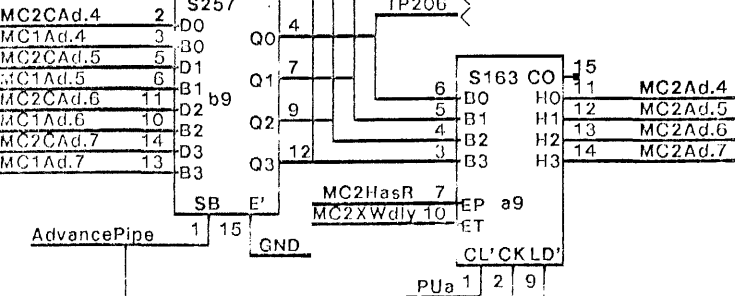
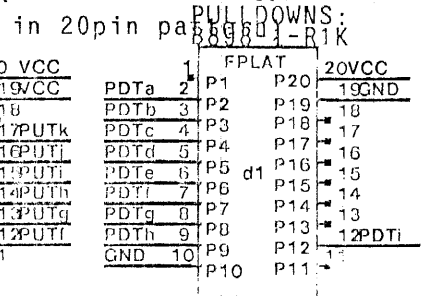
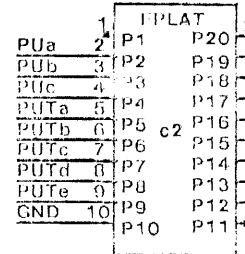


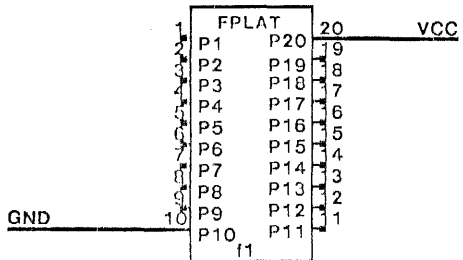
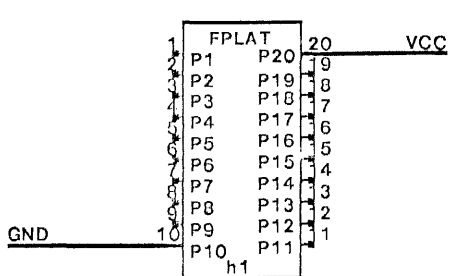
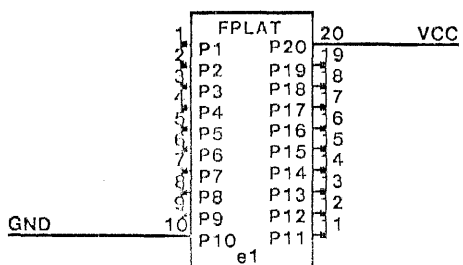
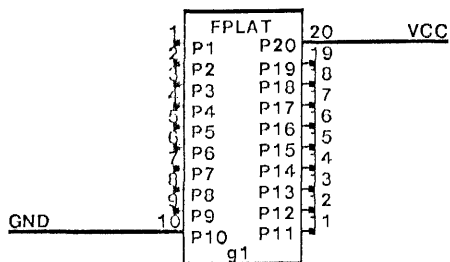
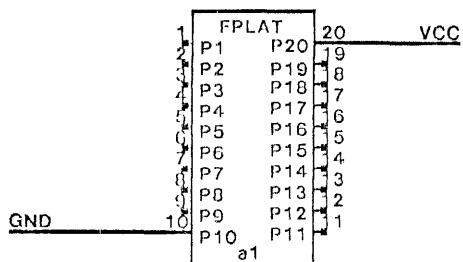






PULLUPS:  
B898-1-R1K  
(centered in 20pin package)





Changes for revision G to H:

- 1) Added clkH2' (pg 6,15).
- 2) Added output CheckRParity' to prom d5 (pg 9) and S51,15b (pg 18) to check parity only when R is read.
- 3) Added (pg 6) gates i2b, a3a, and b4c to correct deficiencies in R address calculation.
- 4) Added signal PUTj (pg 14, 20) for test.
- 5) Added signal PUTk and gate b3c (pg 15,20) for test.
- 6) Added signal PDTi (pg 18,20) for test.

Changes for revision H to I:

- 1) Changed signal named HighByte+F1F2 to HighByte+F1F2' and changed dwg. of gate c3a (pg5).
- 2) Removed sign extension feature for constants in arithmetic operations. Changed signals SignExtendF1F2 to GND (pg 3,4) and removed gate a4a (pg 5).
- 3) Changed clear input of d18 from PUC to RUN (pg 19).
- 4) Eliminated (redundant) signal LoadMC1 (p16). This signal is now LoadAd. Changed gate at c3b (S10) to S00 (e2b).
- 5) I2.15 is now GND, was MemInst' (pg 16).
- 7) Changed ALUA.08In-ALUA.15IN to ALUA.08-ALUA.15 (stkp input, pg 11).
- 8) Added S240's to force R[04:07] to ONE during R←SALUF (pg 10).
- 9) Added test points. If signal was named, t.p is added in italics. If not, signal name is now TPxxx.

Changes for revision I to J (6/26/78)

- 1) Replaced signal Cycle0' with Cycle0Feed' at a4.10 (pg 6)
- 2) Changed PUB to MC2XferWord at c15.3 (pg 13)
- 3) Changed PUB to MC2XferWord at d11.6 (pg 13)
- 4) Generated MC1XWdly at g2.15 - added feedback from g2.12 to g2.2, removed PUC from g2.2 (pg 16)
- 5) Renamed MC1WillGetR' to ShiftMC1XW' (pg 16)
- 6) Generated MemNeedsR' in S51 at a3b rather than in S02 at b4a (pg 16)
- 7) Generated MC2XWdly in S74 at i1b (pg 16)
- 8) a8.10 is now connected to MC1XWdly (was MC1HasR) (pg 20)

Changes for revision J to K (8/29/78)

- 1) Shuffled inputs to decoder d16 and gate c3c, connected d16.5 to Cycle0Feed' (pg 19).
- 2) Changed gate c8a to S10 at c3b to form clkSS1kp' (pg 15).
- 3) Changed a4.2,5,10,13 from MC2Ad.x to MC2CA.d.x to make Raddress interlocking during single errors work properly (pg20).

Changes for revision K to revision L (10/7/78)

- 1) Changed inputs of c14 section b (pg13) from GND to ProcCycle0 and SRSA2. This requires revision E for Prom b2.
- 2) Connected clear inputs of g2 and h2 (pg16) to RUN rather than Puc. (required to initialize XferWord regs. at boot).
- 3) Reversed order of test points TP206-TP209 (pg 20).

Changes for revision L to revision M (12/9/78).

- 1) Changed h19.1 from QWO to H2.0B' (pg 10). Branch on QWO is now done on Control Store.
- 2) Added flip-flop c18d in line EnCoAd' (pg 17). Memory Control rev M is required with this change.
- 3) Added PROM a2 (at revision F) to check Stack overflow (pg 11).
- 4) Removed signal MC1XferWord from E006 to make room for new signal StackEmpty (pg 16).

Note: Revision M = Revision Ga

Current Prom Revisions:

- a2: F
- d5: D
- b14: D
- b13: E
- i2: D
- b2: E

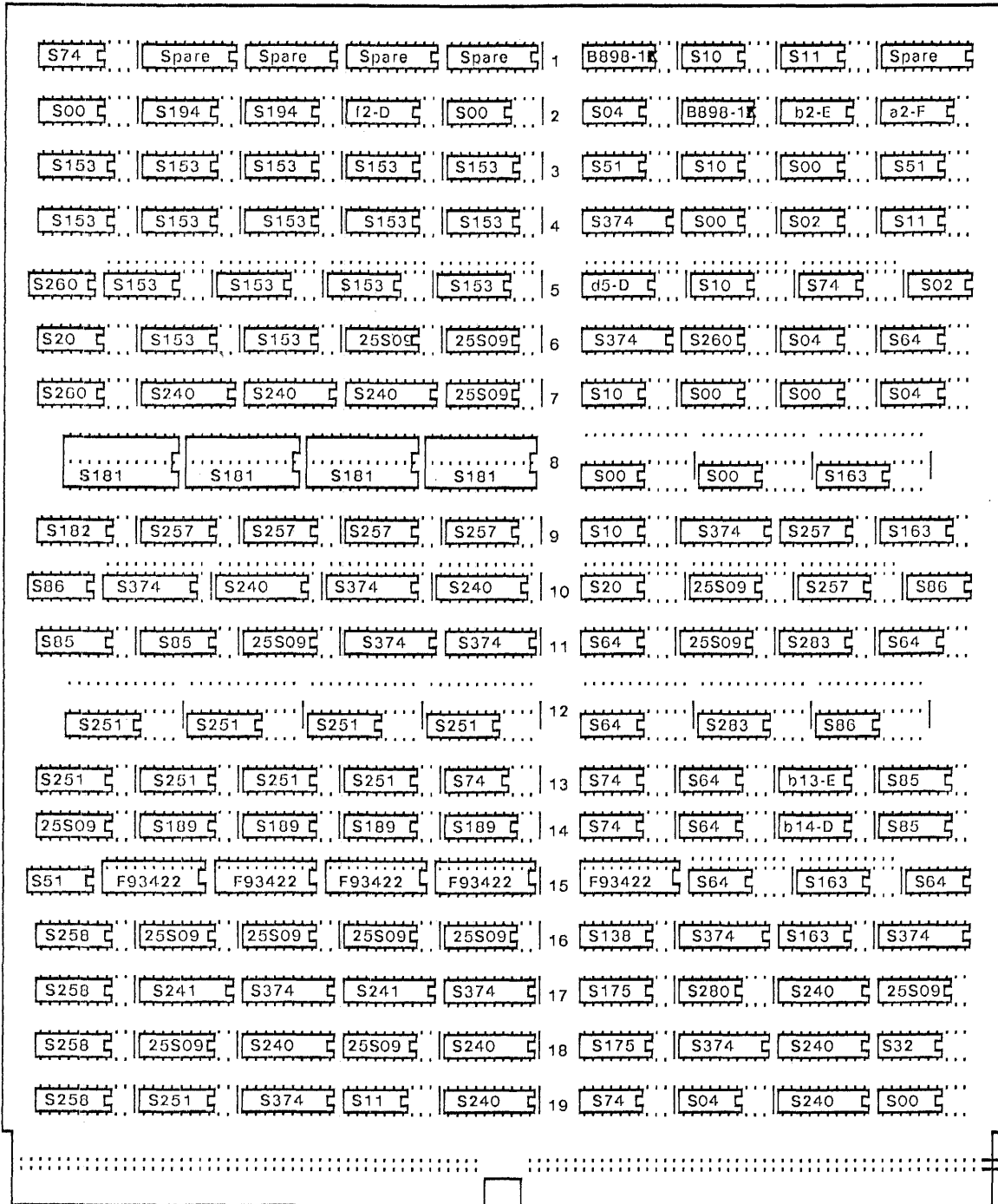
Note: This board contains no platforms. The "Plats" at positions c2 and d1 are Beckman B898-1-R1K resistor networks (15 1K resistors with pin 15 common).

Equivalent networks from other manufacturers may be substituted.

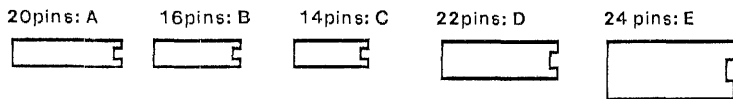
XEROX E00	Project NO	ALU Card CHANGES	File D0aluCHANGES.sjl	Designer Thacker	Rev Ga	Date 2/19/79
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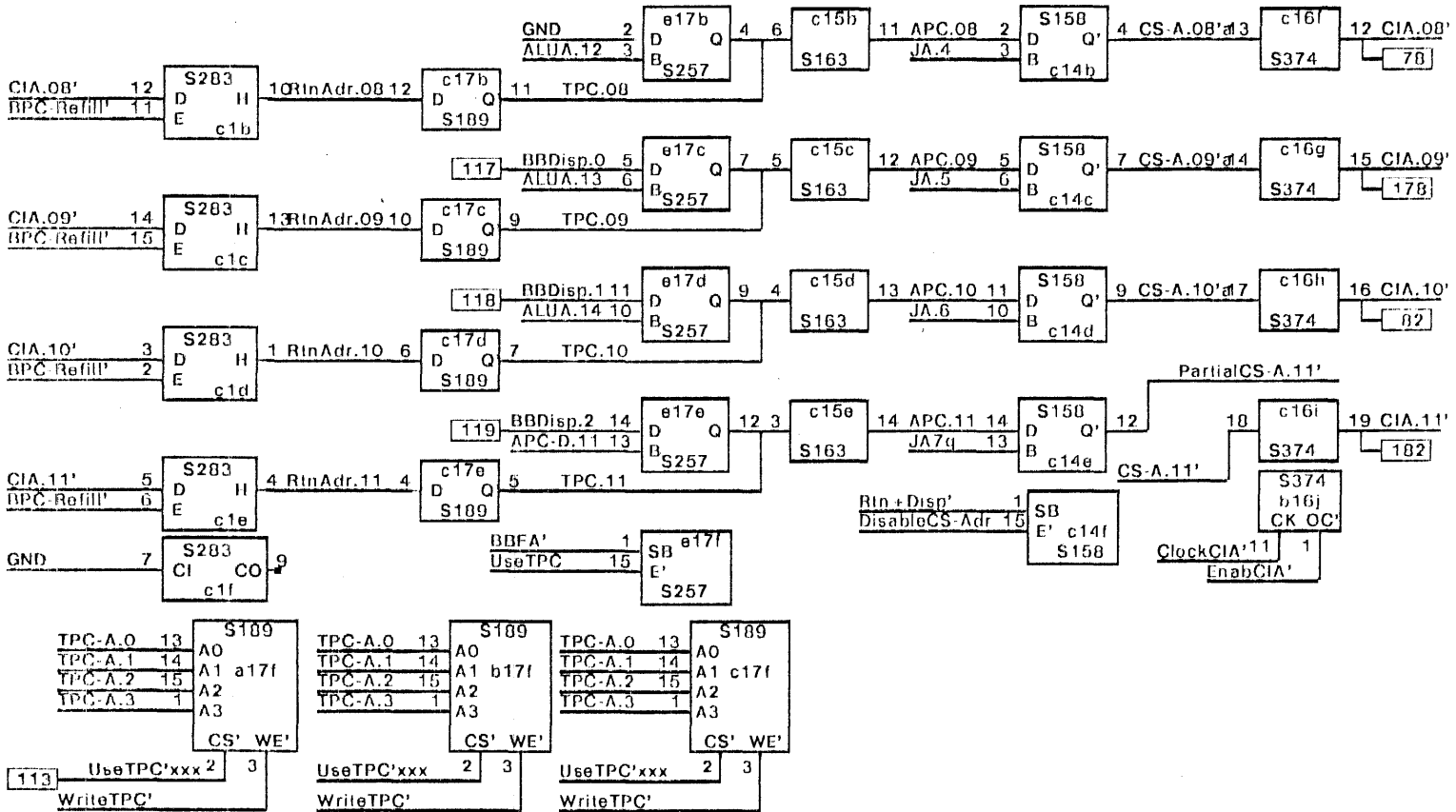
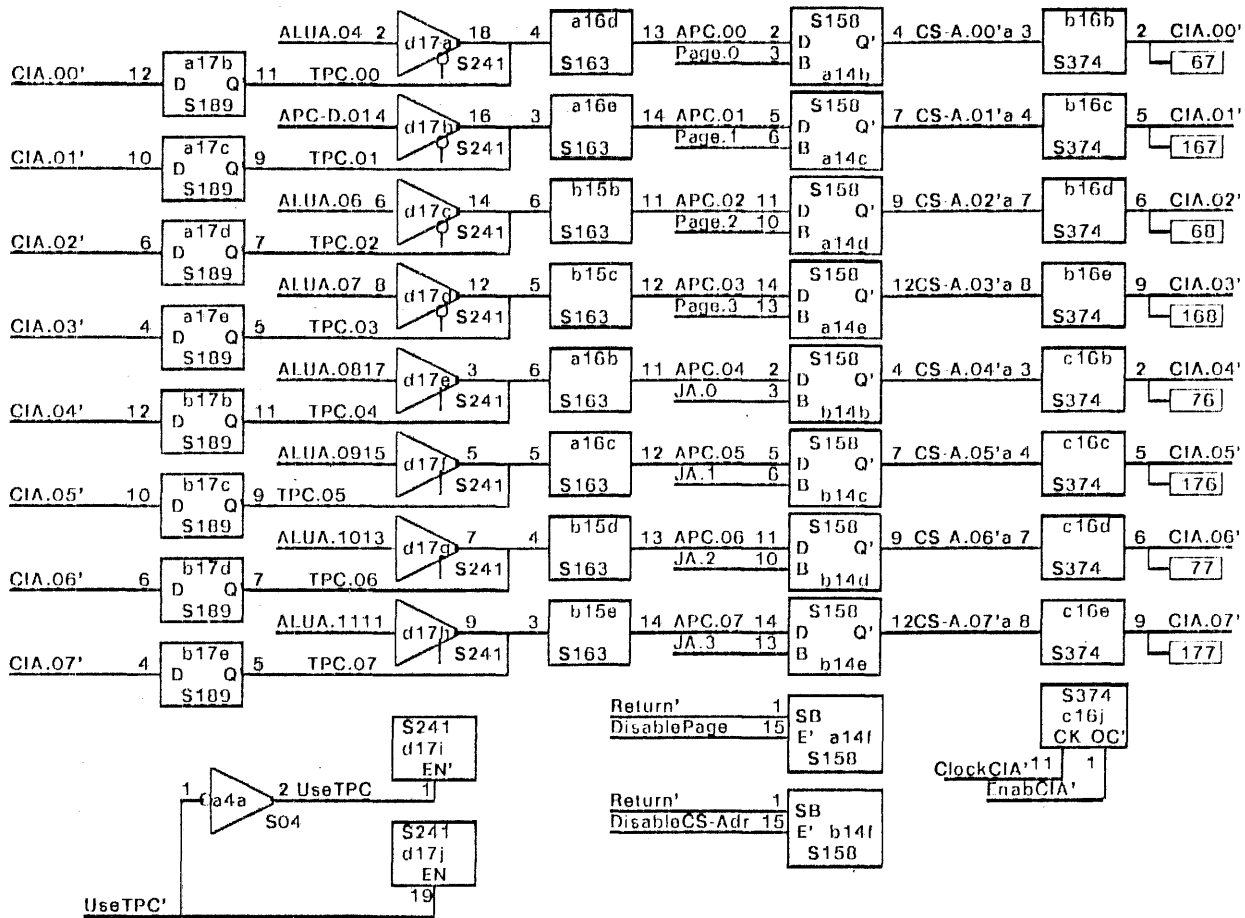
I H G F E D C B A

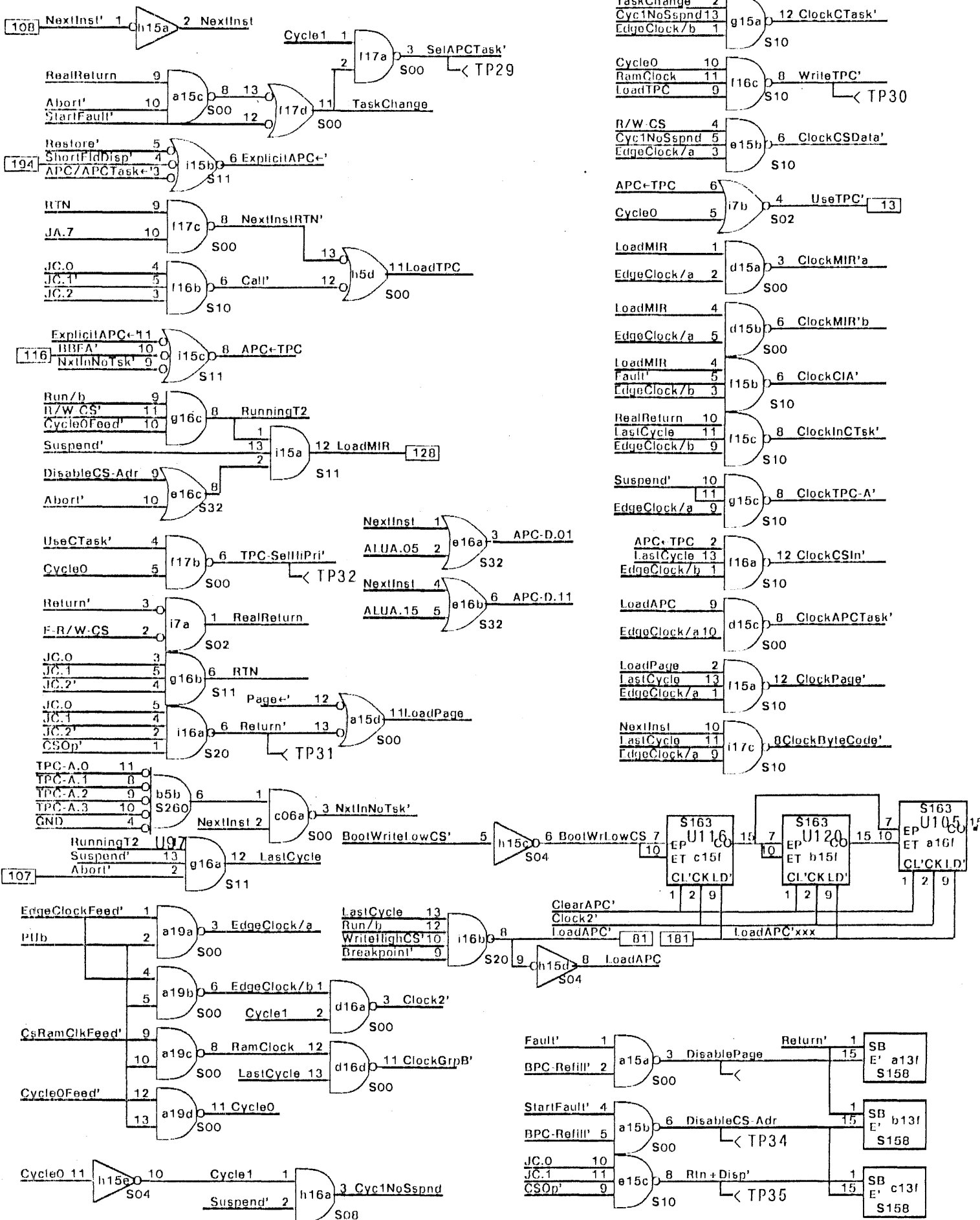


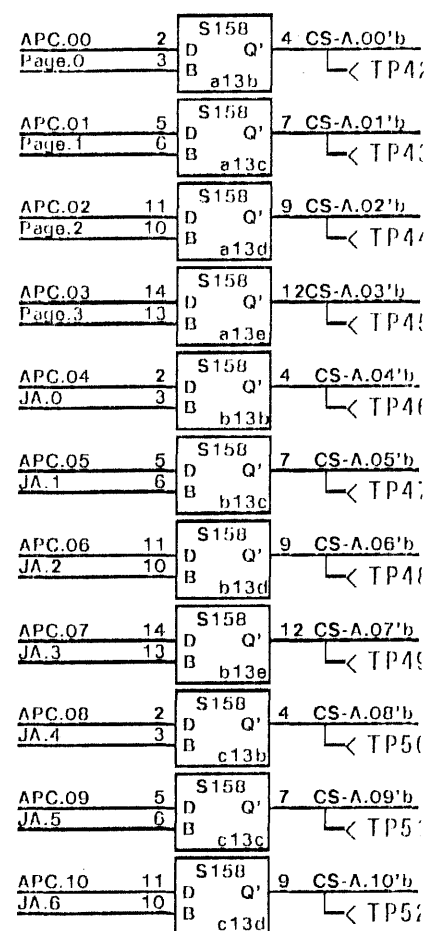
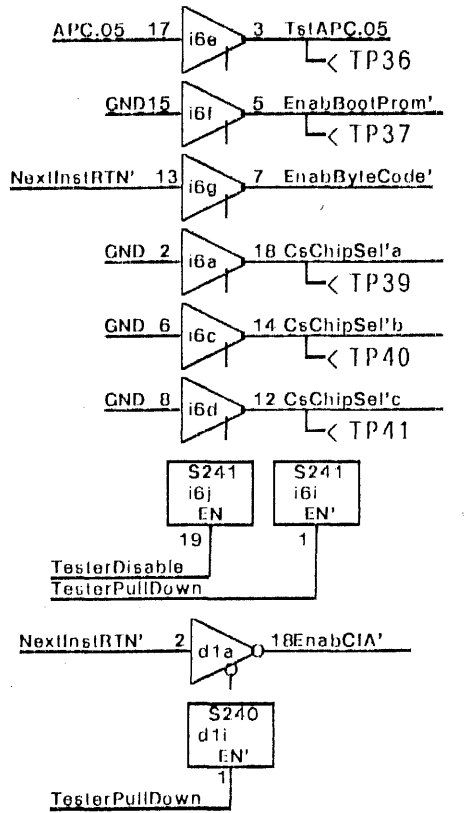
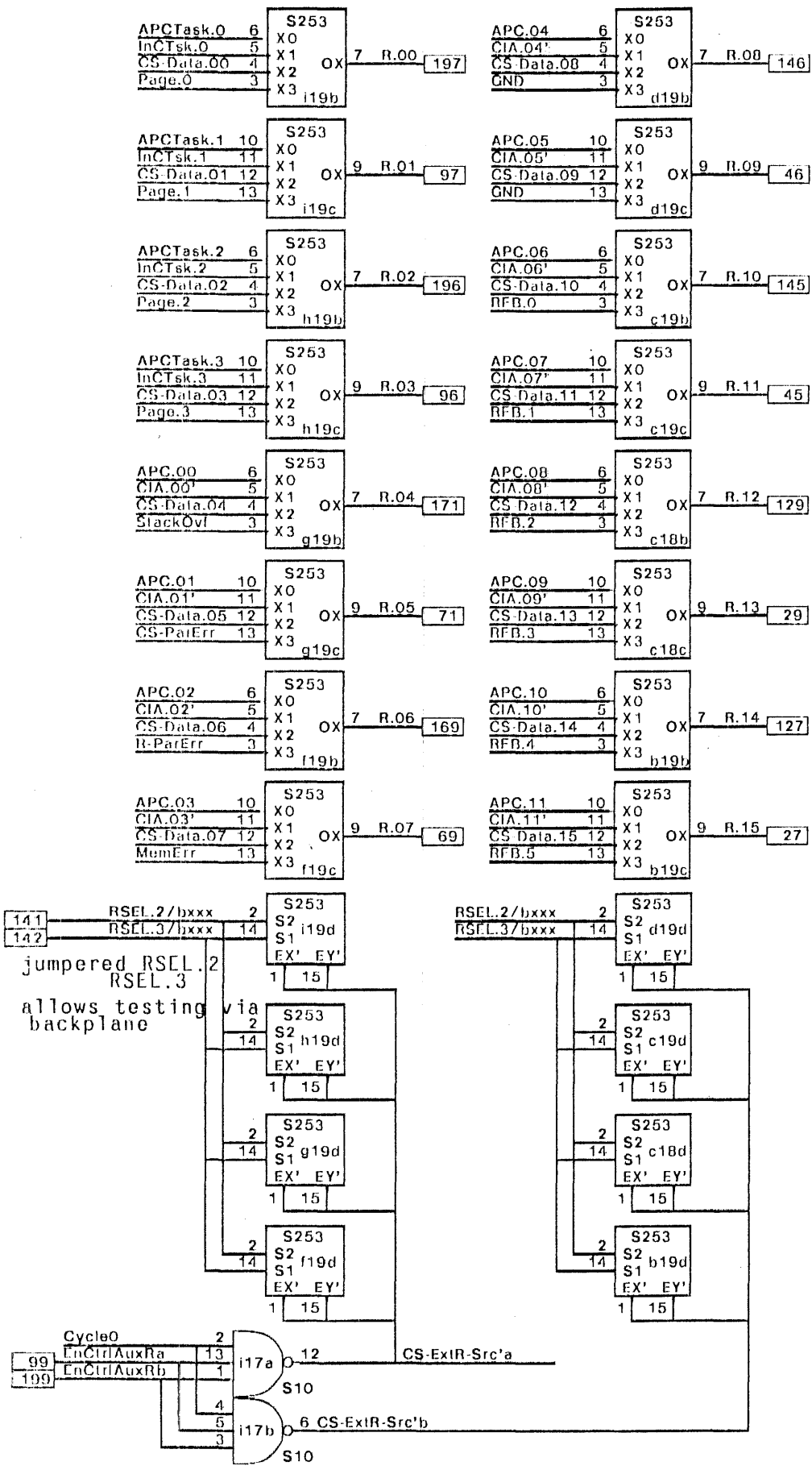
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1-100

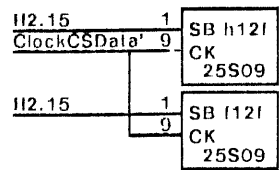
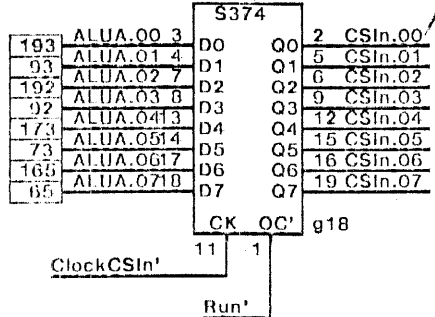
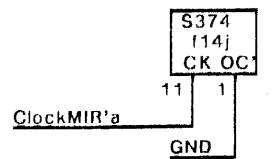
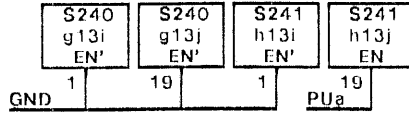
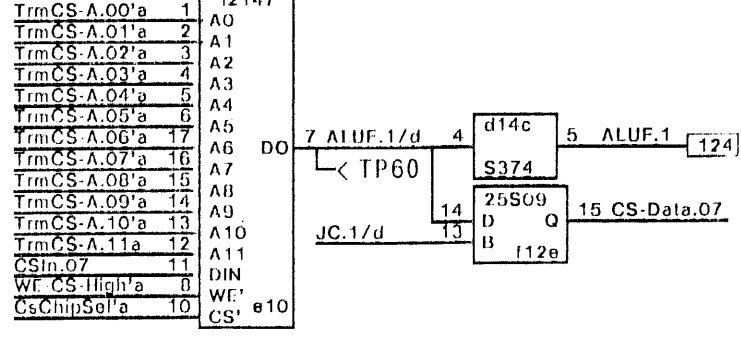
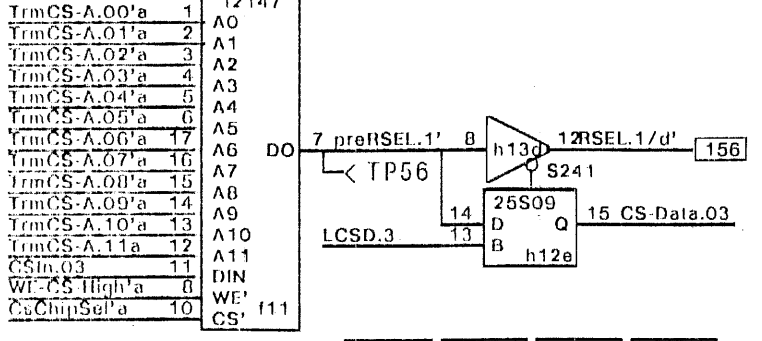
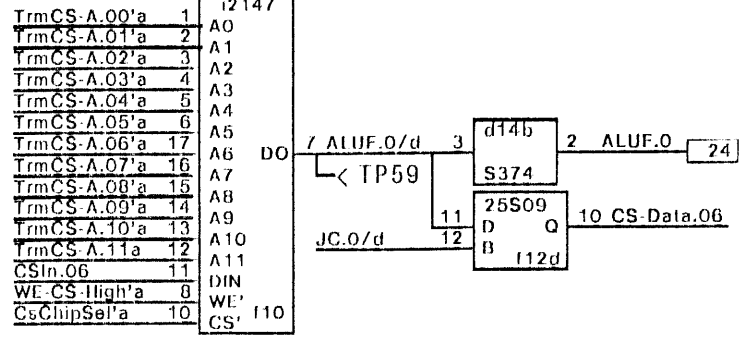
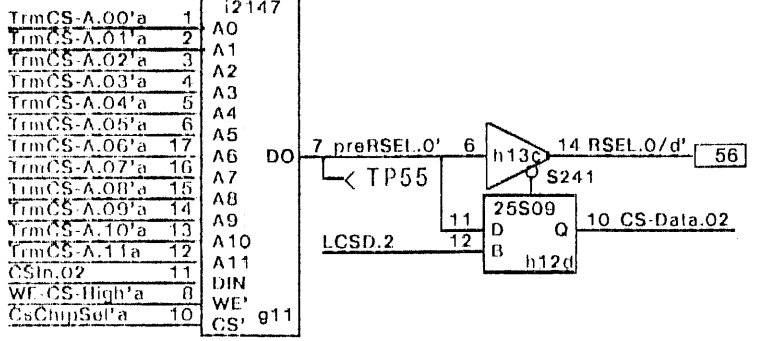
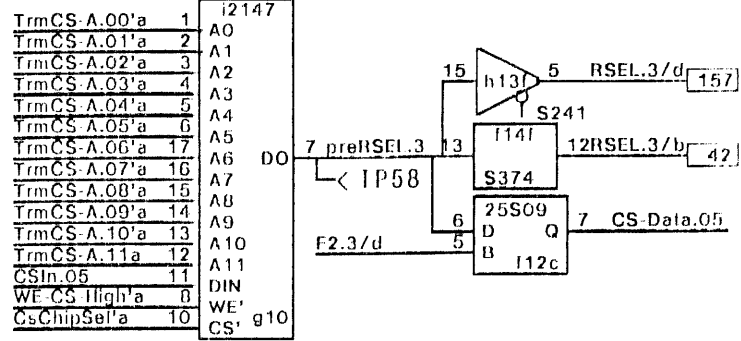
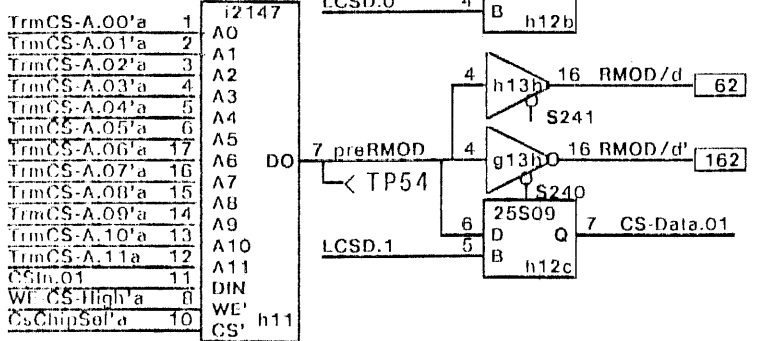
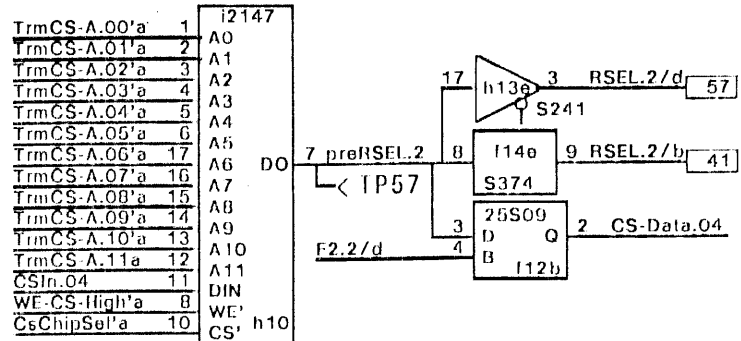
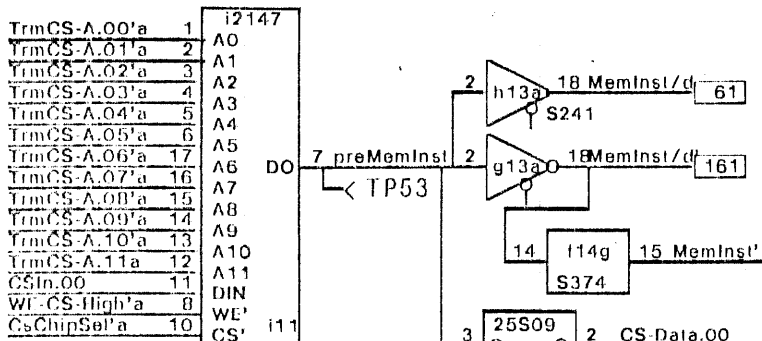


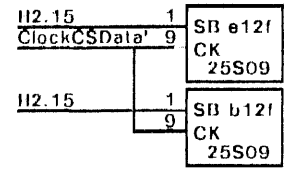
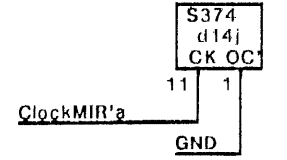
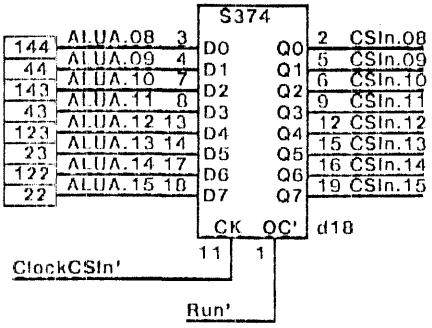
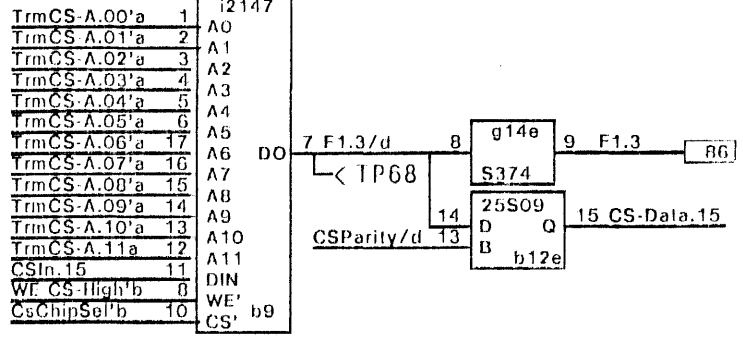
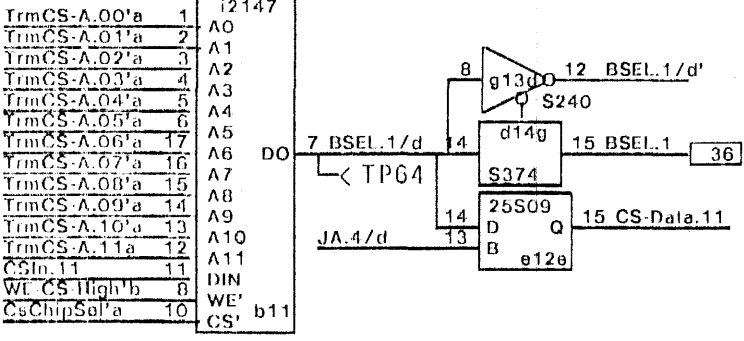
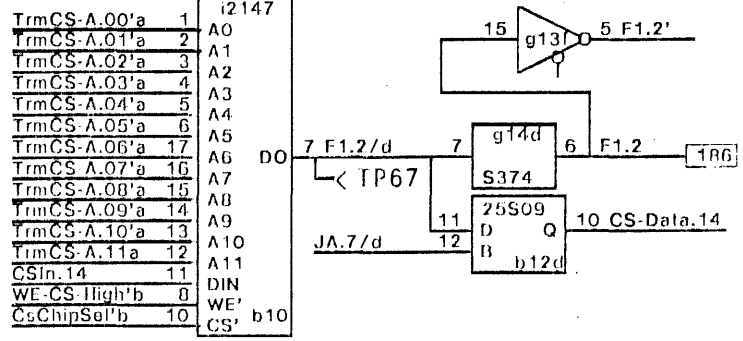
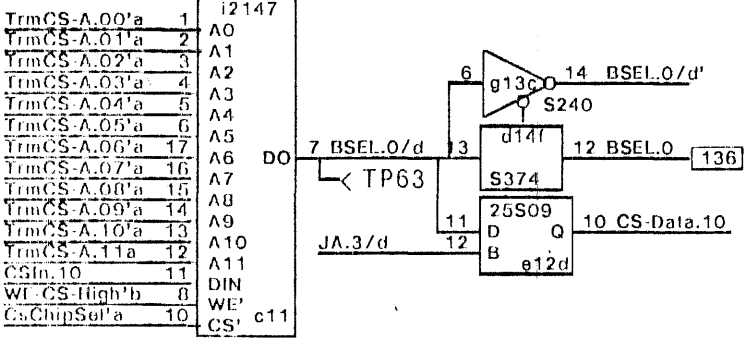
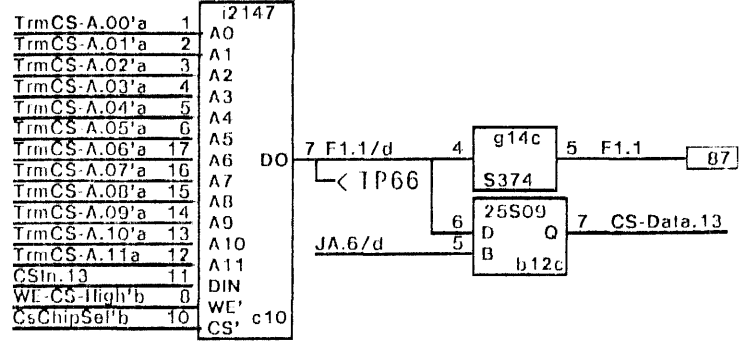
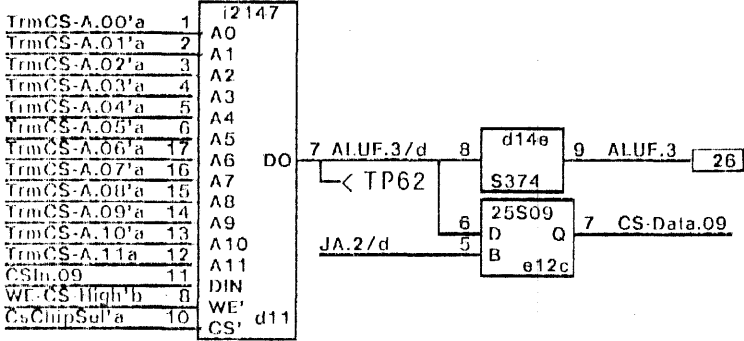
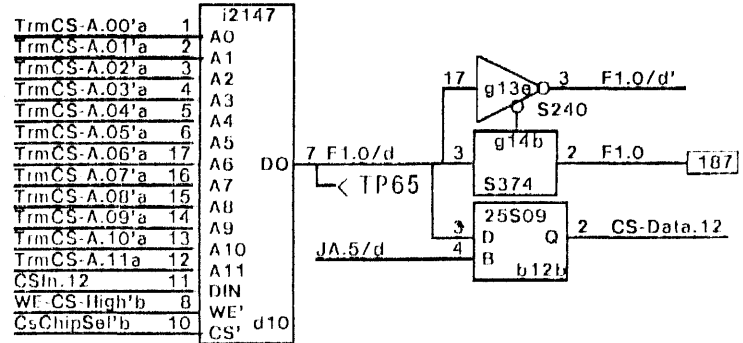
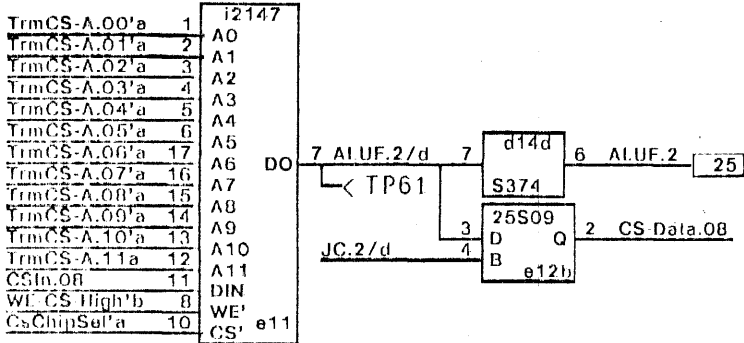
Note: The short vertical lines indicate  
filler capacitor locations.  
(119 Total)

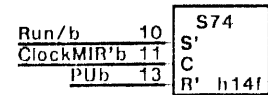
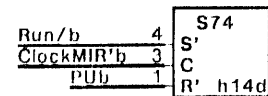
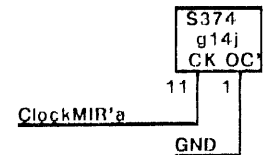
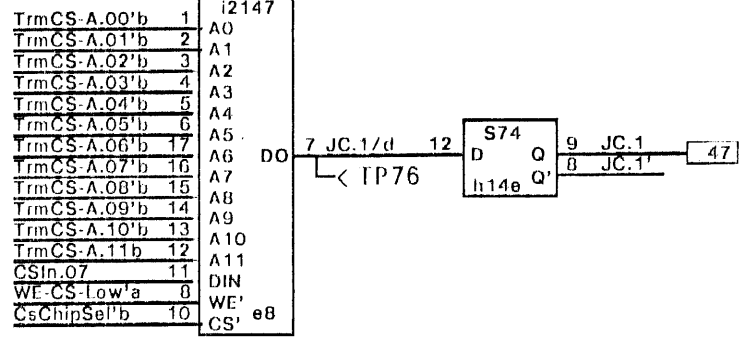
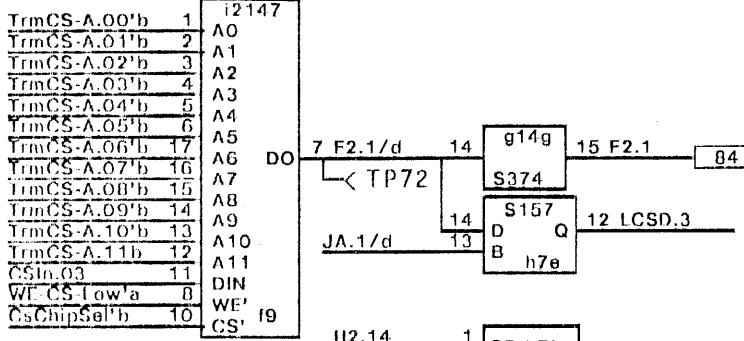
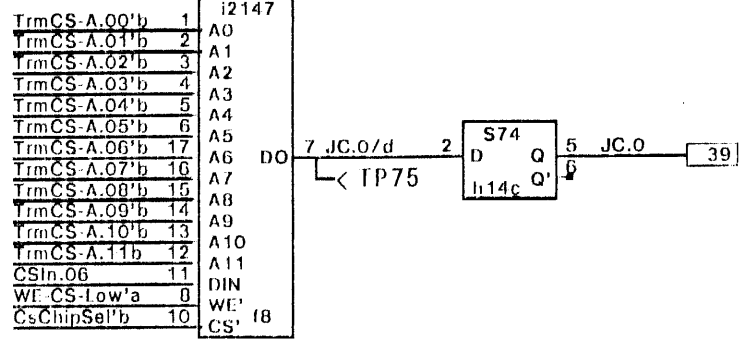
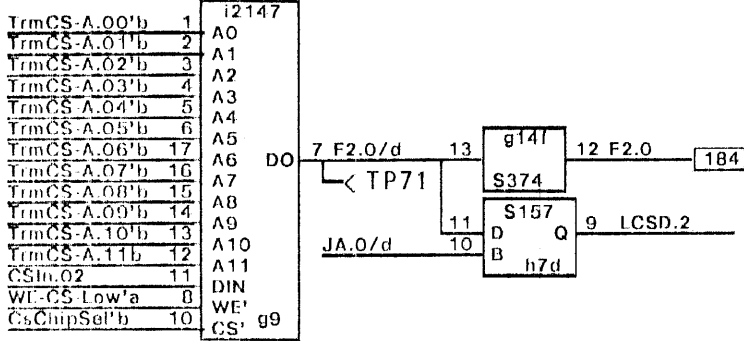
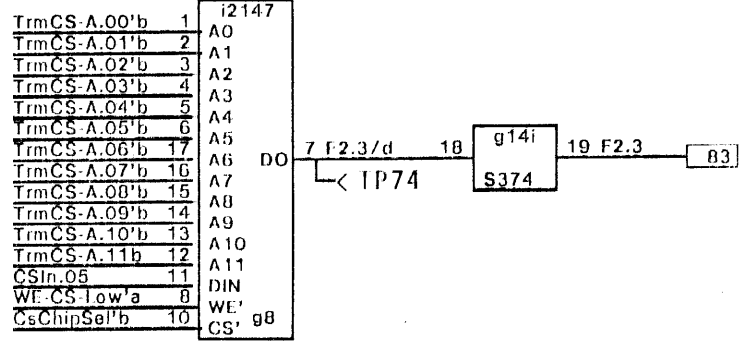
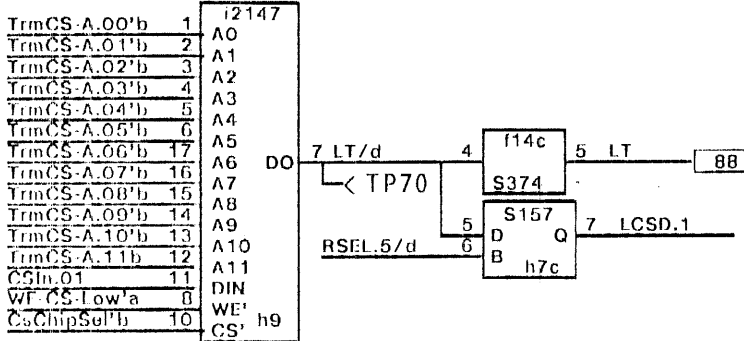
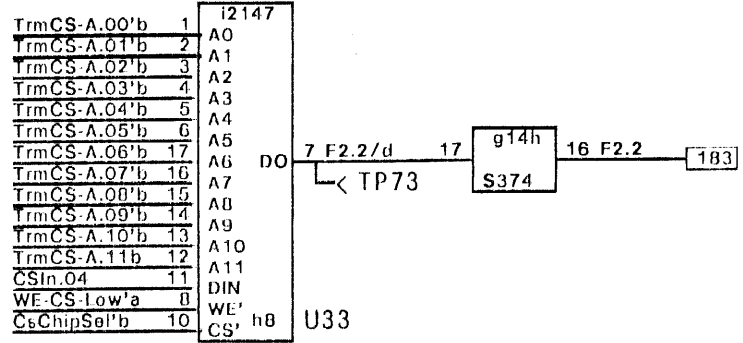
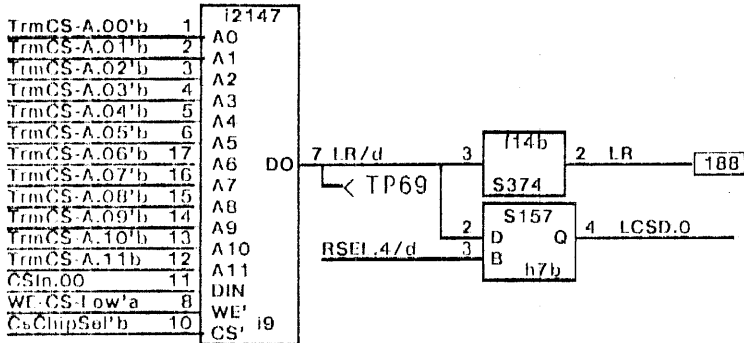






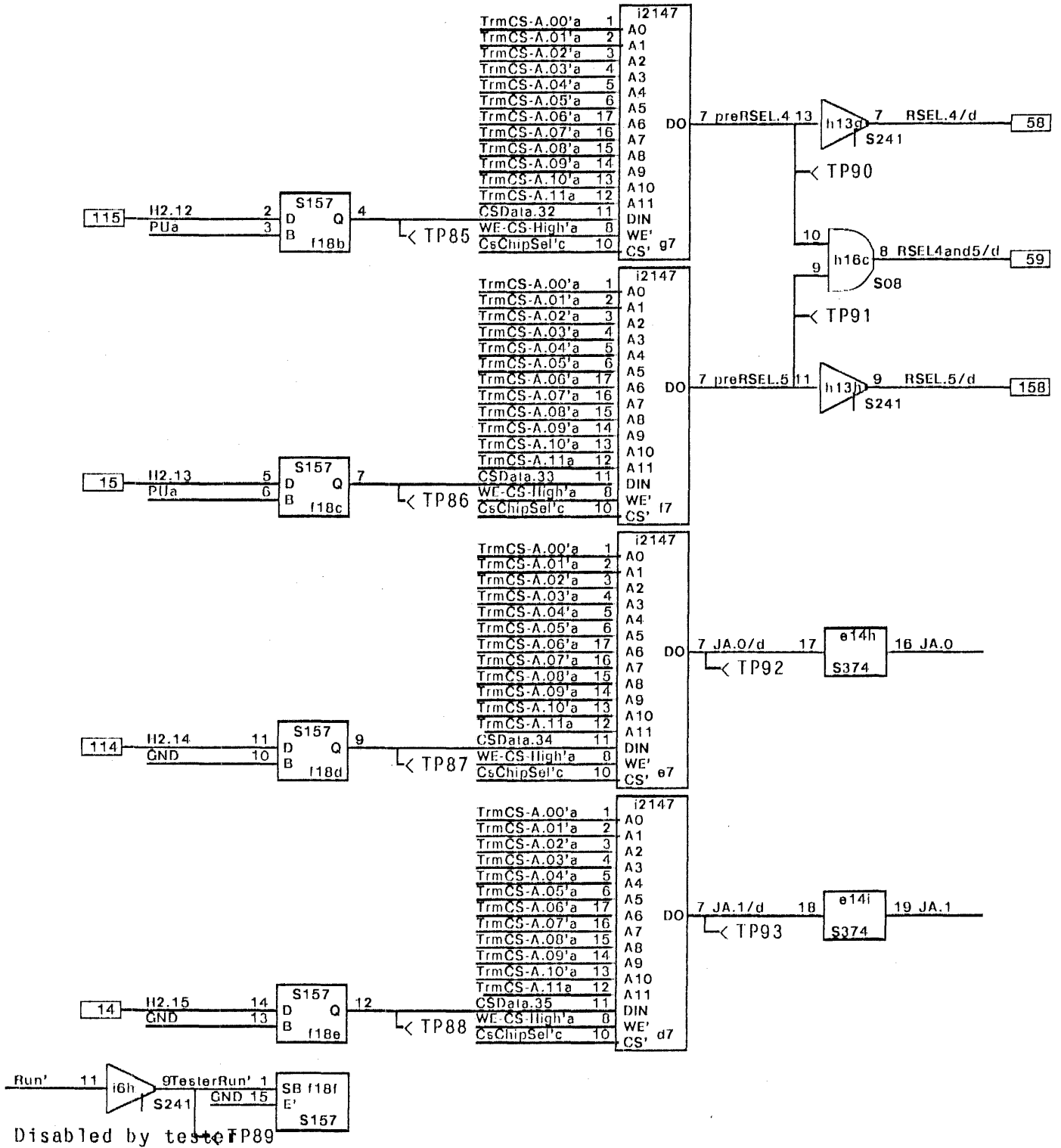




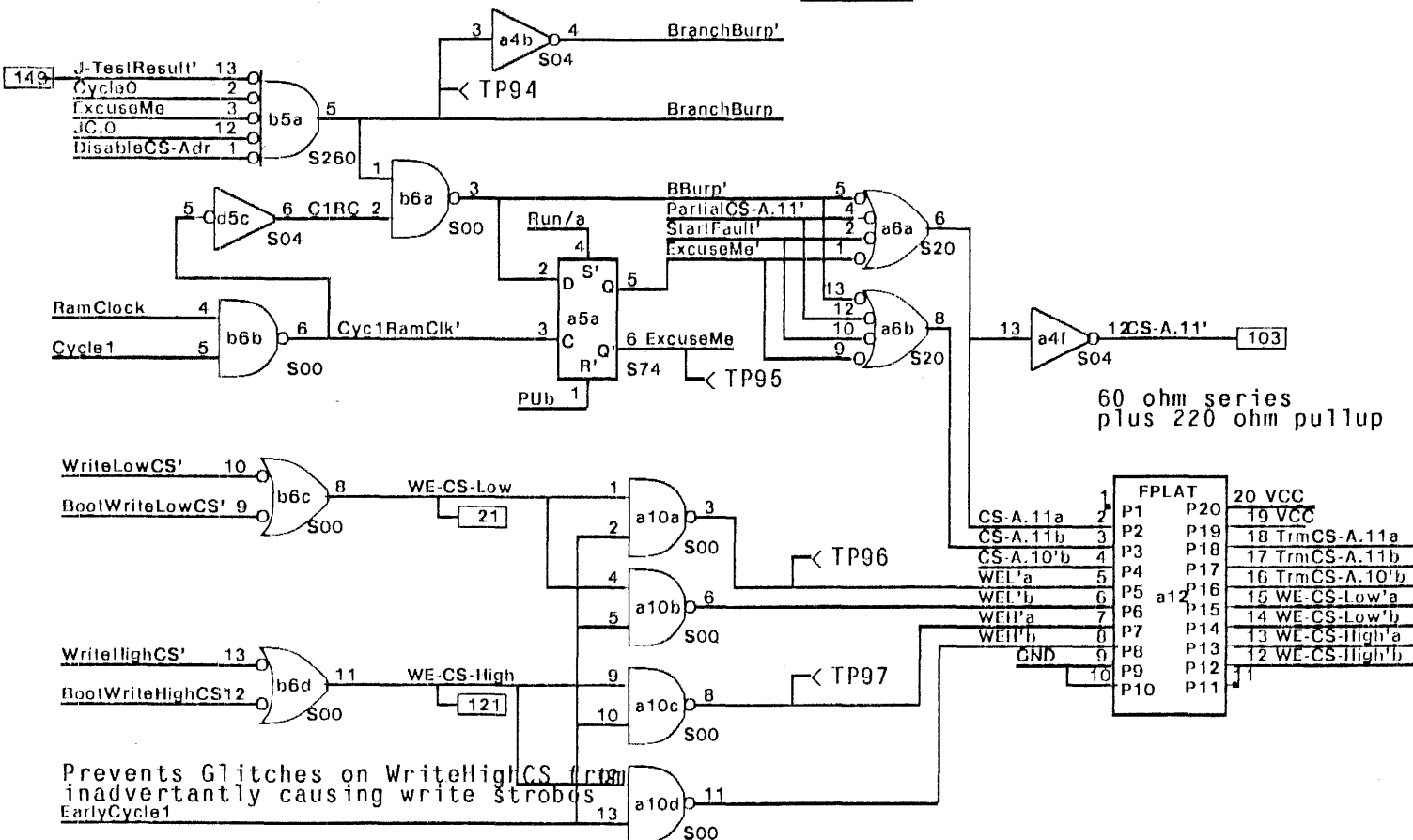
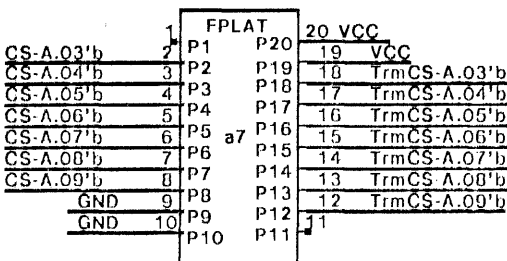
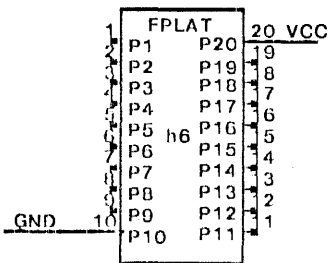
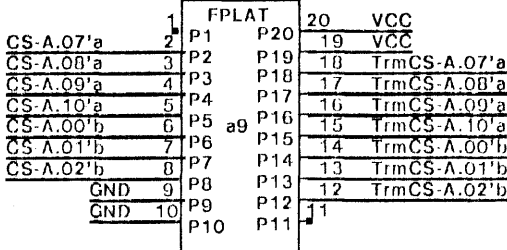
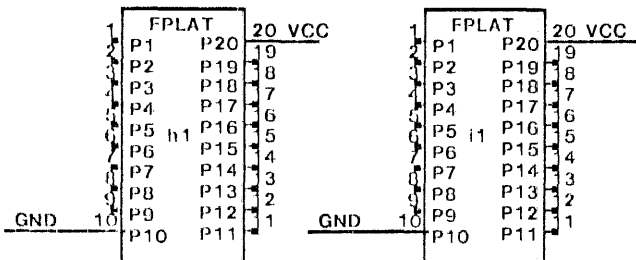
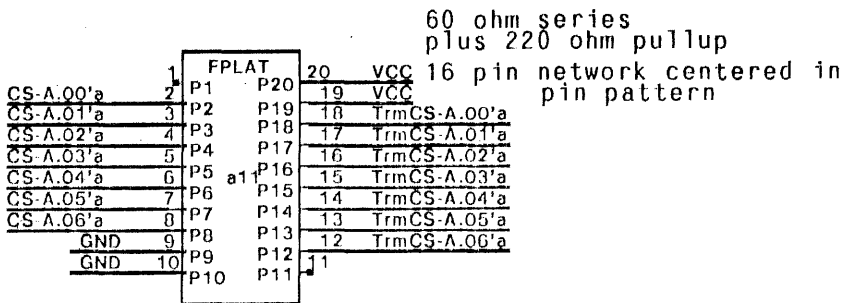
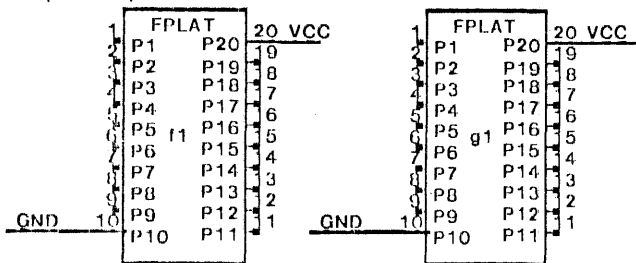




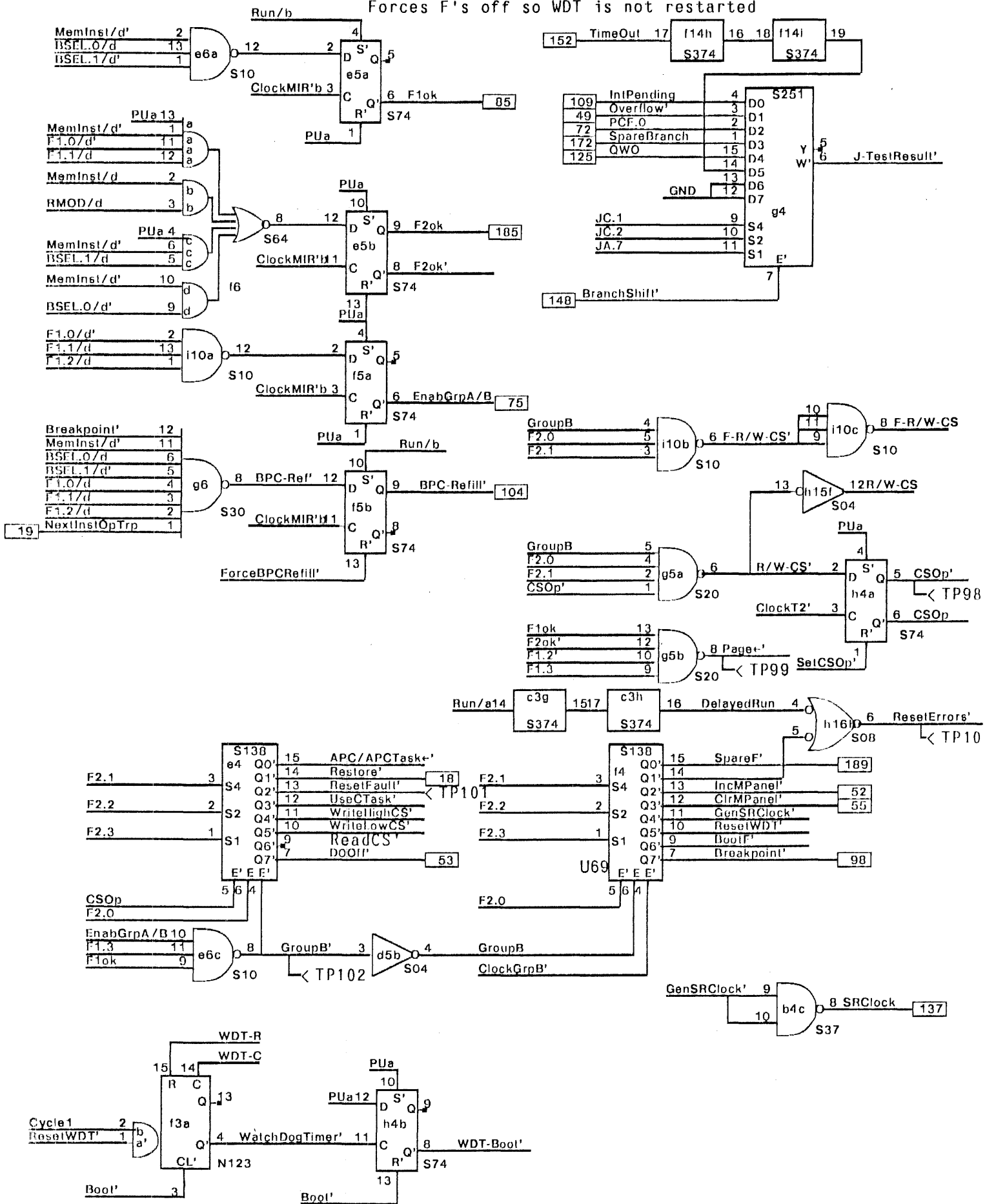




Spare positions

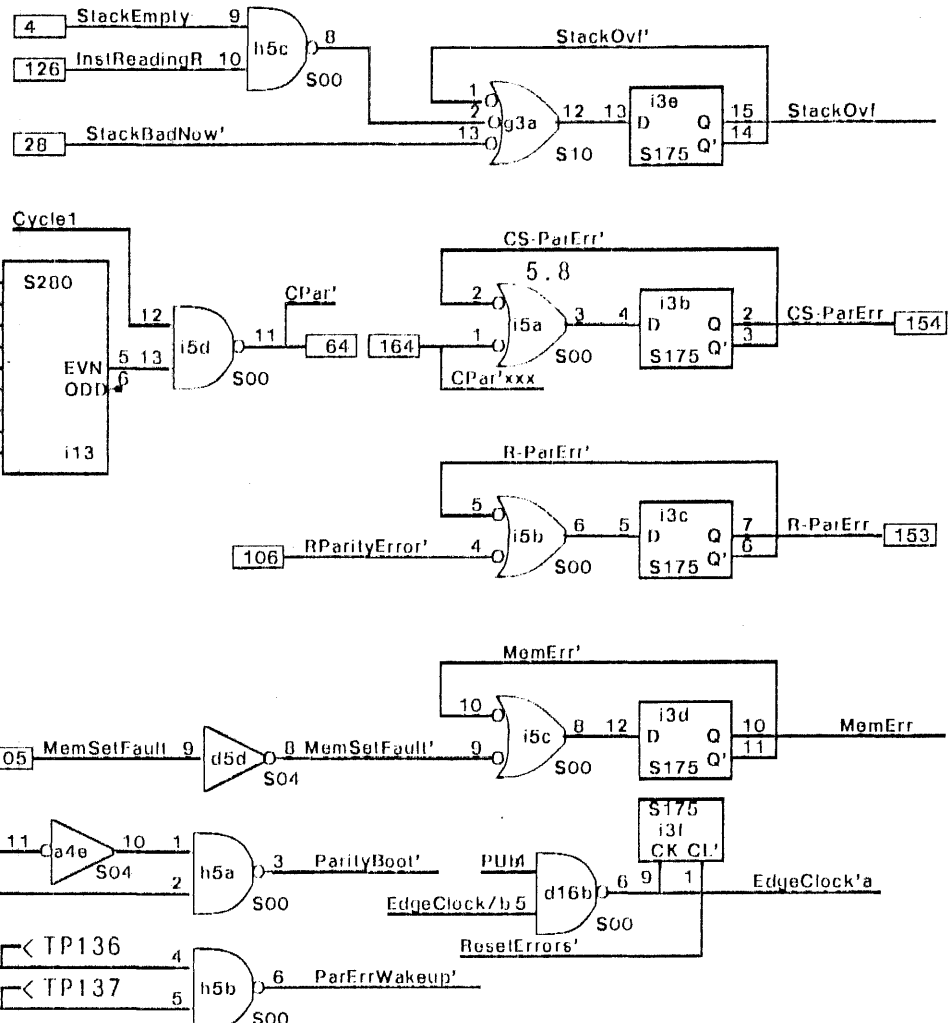
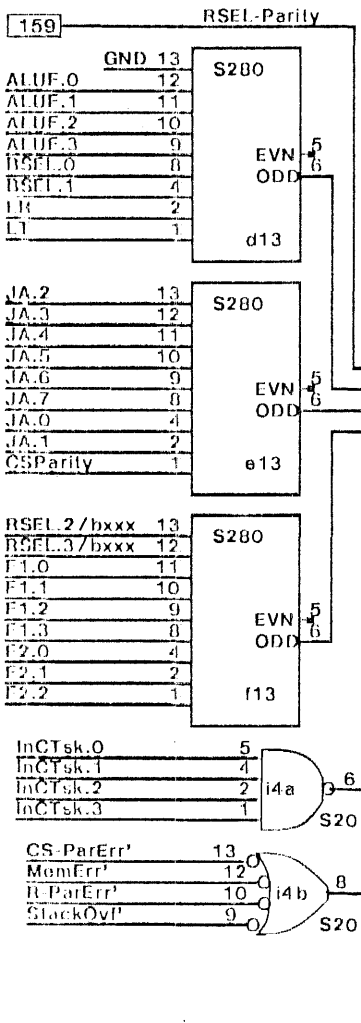
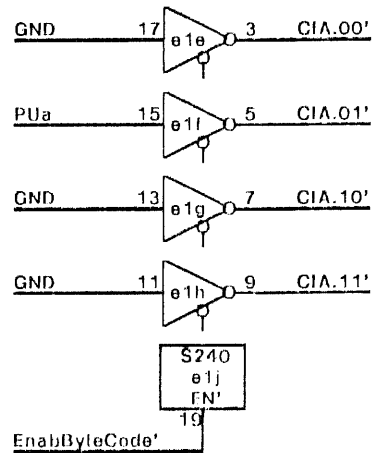
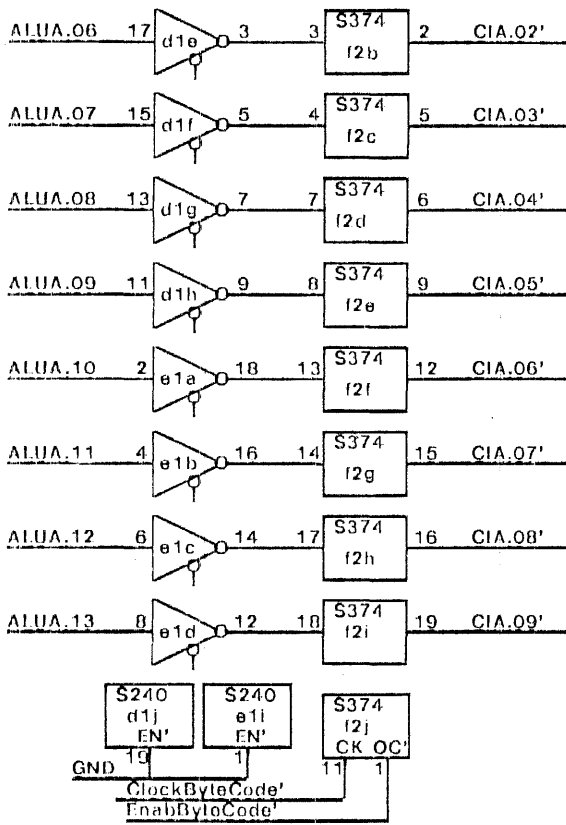


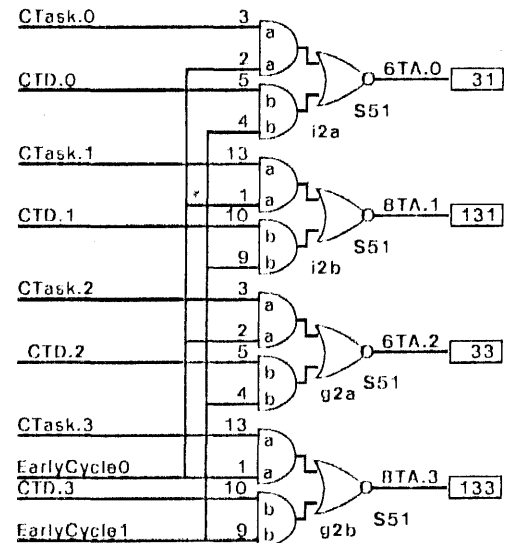
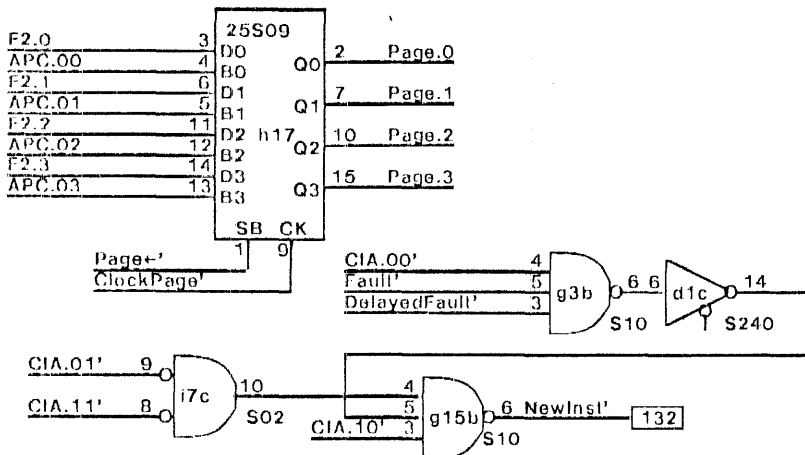
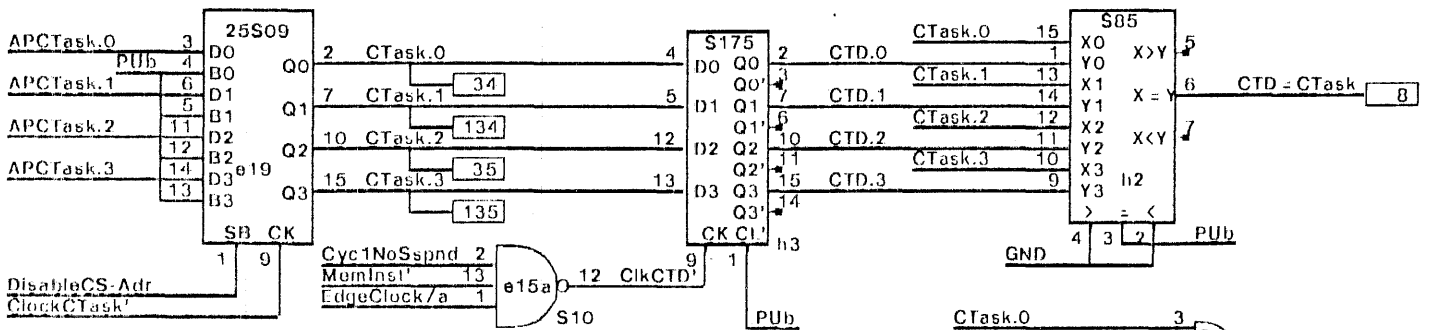
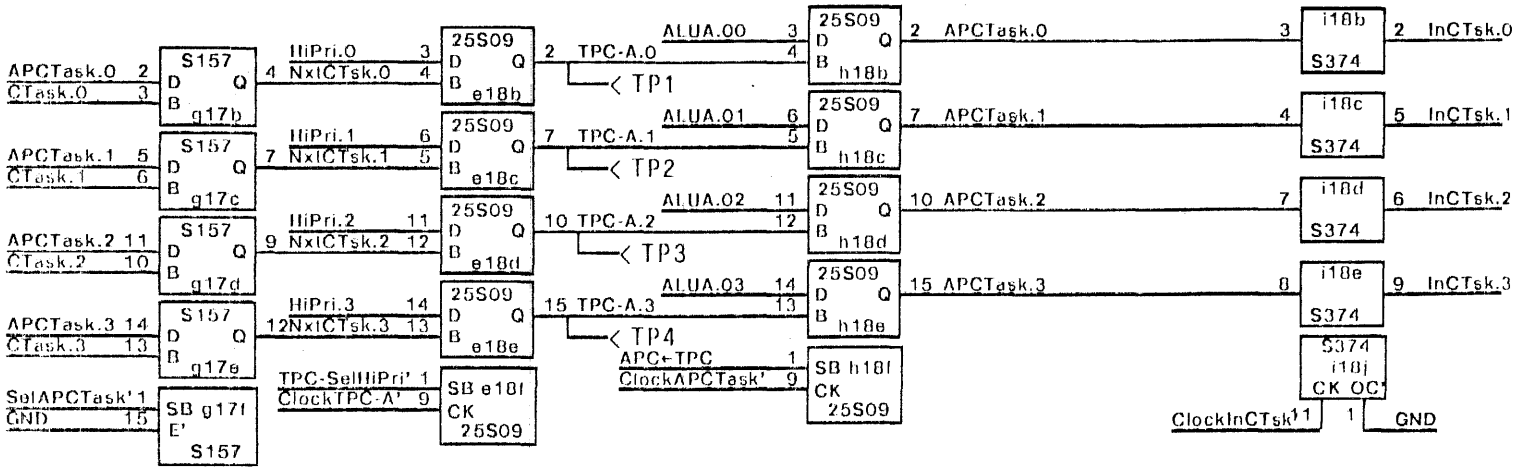
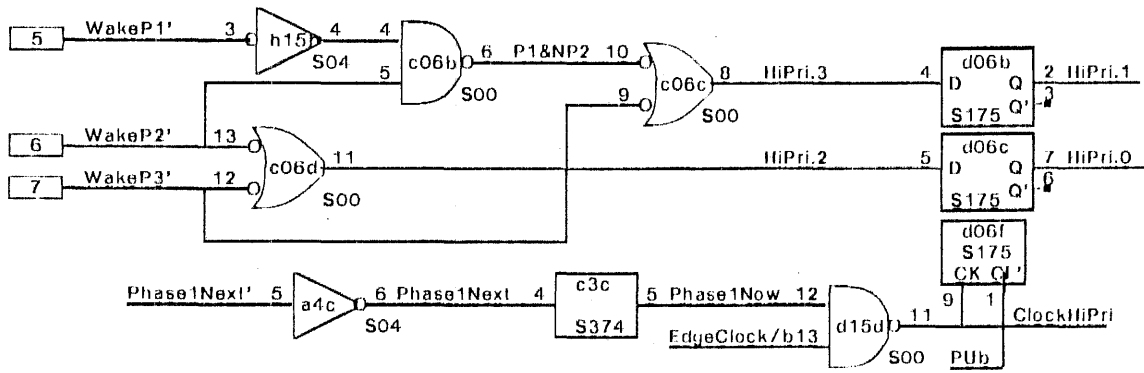
Forces F's off so WDT is not restarted











Rev E to Rev F 3/8/78 Brian Rosen

- 1) The Clock Drivers on page 12 were moved from c1/d1 to a18/b18 to eliminate waveform distortions due to reflections at the connector that caused false clocking on some boards. This necessitated moving the TPC-A multiplexer (page 1) from b18 to g17, and the Wake-up encoder S00 from a18 to c06. The wake-up lines now have long stubs on this board. The HlPri register was also moved up next to the S00 encoder (from e01 to d06).
- 2) The S30 at g6 that makes BPC-Refill' (page 10) had Breakpoint' added to it. This prevents the BPC-Refill trap from occurring when the successor of a breakpointed instruction points to an instruction which has NextInst or Nextop specified.
- 3) The trap location for Fault and BPC refill were reversed by changing the term on CS-A.11 from BPC-Refill' to StartFault' (S20 at a6 on page 9). Faults trap to 1, BPC refill traps to 0. This forces a nextinst/nextop which both BPC refills and Faults to hit the fault handler rather than the BCP handler.
- 4) The EPROM sockets were changed to allow 2716s or 2750s to be plugged in. This removes all dependency on the +12/-5 supplies for booting, and allows a 1k boot program. This change also affected the bit tested to determine end of boot load (from APC.00 to APC.05, thus affecting TstAPC.00 on page 3 and page 11)
- 5) A new Clock was added for the EOM board (ROS printer). This clock, EomClock, is a 35ns (nominal) squarewave, with a clock driver. See page 12.
- 6) Final testability changes were made, they include: a) A new signal, TesterDisable which is an independent pullup resistor on a new plat at e2 (page 11). This signal enables the S241 on page 3 which allows tester control of TstAPC.05, Enable BootProm, EnabCIA. b) another new signal, also an independent pullup (page 11) which allows tester to force CSOp to sel. c) an S51 at b1 now lets the tester turn off the oscillator with a new signal-ExtClockEnab'. This signal is pulled up on the e3 plat instead of ExtClock'. c) the clock generator flip flops can be initialized by the InitClk' signal, which is pulled up on the e2 plat.
- 7) a minor improvement was achieved by eliminating the S32 at d6. Only one section was used (SRData, page 10) and an unused S32 section was available in the e16 S32. d6 is now empty

Rev F to Rev G 4/17/78 Brian Rosen

- 1) The chip enables for the TPC rams (control sections on pages 1 and 2) were run through an S241 controlled by DisableTester to allow tester control of APC inputs
- 2) The Run/a signal was run through another tester controlled S241 gate to allow tester control of the EPROMs (page 11)
- 3) The select input of the data in mux for bits 32:35 of the control store (page 8) was modified to run through another S241 gate to allow tester control of the data input to these 4 RAMs.
- 4) A new pull down resistor was added to the e2 plat (page 11) creating the signal TesterPullDown. This is the control input to the tester S241 (page 3)
- 5) The signal ChipSelect' (an input to all 2147 RAM chips, pages 4:8) was broken up into 3 separate nets, each fed from an S410 gate at i6 (page 3, nets CsChipSel'a, CsChipSel'b, and CsChipSel'c)
- 6) An adder, S283 was added between CIA and the TPC ram inputs (page 1) to make the return address CIA + 1 (carries propagate through 4 bits only). New chip is at c1.
- 7) The clock term for CTD (page 13) needed to have MemInst' as an input. Added a new gate (e15a) to make this term.

Rev G to Rev H 9/8/78 Brian Rosen

- 1) The Abort' term on ClockTPC-A' (g15.11) page 2 is erroneous, it was removed.
- 2) The Cycle1 term on RunningT2 came very late for some qualifier terms. It was changed to CycleOfFeed' thus cutting two gate delays
- 3) The Complement of the actual BranchBurp signal is needed for new clock driver scheme (see note 4 below). Added an inverter to BranchBurp using a4.3 and a4.4 creating BranchBurp'. The signal from b6.3 (page 9) had its name changed to BBurp'
- 4) Clock Drivers (page 12) were changed from S32s to S37s. This changed all inputs on a18, b18 and c5.
- 5) CycleOfFeed' is too late. The S37 that created this signal (page 12) was deleted. CycleOfFeed' now come from a5.8 (this affected the name of the signal at b3.5 (was EarlyCycle1, now CycleOfFeed'))  
This EarlyCycle0 is also used on a10 (page 9) and i2/g2 (page 13). The next revision (I) will remove some of these loads  
For now, they are all CycleOfFeed'

Rev H to Rev I - 11/18/78, C. Thacker

- 1) The register ByteCode is added (f2,d1,e1, pg13). This register holds A1.UA[6:13]' for one cycle following NextInst, so that the bytecode can be written into TPC by the subsequent RETURN. This allows task switches between bytecodes.
- 2) The signal SRData (buffered H2.15) has been deleted. This requires a backplane change (pg 4,5,10).
- 3) The branch logic on pg 10 is changed to add InIPending (in place of Disp999), QWO, and a SpareBranch.
- 4) The signal NxtInNoTsk' is generated in c6a (pg2). This signal is true if a task switch will NOT occur in the RETURN following a NextInst. This signal determines the source of APC data during NextInst.
- 5) The signal NxtInst(RTN) is generated in i17c (pg2). This signal will be asserted by all RETURNs following NextInsts, and will cause ByteCode + 1 rather than CIA + 1 to be written into TPC.
- 6) The function decoder on pg 10 is changed to bring out SpareF', and rename DispCnl' and DispClr' to IncMPanel' and ClrMPanel'
- 7) The generation of RUN(pg11) is different. The feed signal from d4.6 is latched, RUN is generated on platform e2.  
(NOTE: e2 is changed to 18pins). PwrBoot' is generated in e16d.
- 8) CSOP (pg10) is clocked by clockT2' (used to be called ClkFault', pg 12).
- 9) EarlyCycle1 (pg 12) was added to reduce loading on CycleOfFeed'.
- 10) Clk1 is brought to the backplane (E12 -> E112) so that a delay can be inserted to reduce the width of RamClock.
- 11) a5.13 (pg 12) is connected to InitClk' rather than to PUa.
- 12) Stack overflow logic is added on pg 13.
- 13) NewInst (used to be an F) is generated on pg14.
- 14) Added TimeOut branch condition (pg10) and brought R-ParErr and CS-ParErr to the edge connector (pg 13).

Changes to revision Ga (2/18/79 - CT)

- 1) Changed all plats to 20 pins on logic diagrams to cause ROUTE to do no trace cuts.
- 2) Added synchronizer on TimeOut (pg 10)
- 3) Changed D00If' to E53, ClrMPanel' to E55 (pg 10).
- 4) Added spare IC's in positions f1, g1, h1, i1, h6.

Rev Ga to rev Gb (3/8/79 - CT)

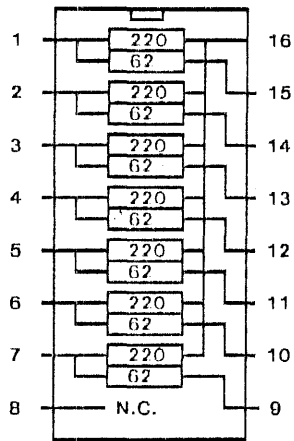
- 1) Added g3b, d1c on pg 14. This change keeps NewInst from occurring when the first microinstruction of a bytecode is aborted.

Rev Gb to rev Gc (7/17/80 - CT) Eliminated signal PwrBoot', changed RFB register clocking (pg 11).

XEROX	Project	Control Board	File	Designer	Rev	Date	Page
EOD	D0	Change History	D0csChanges.si	Rosen	Gc	7/18/80	15



Plats in locations: a7, a9, a11, a12



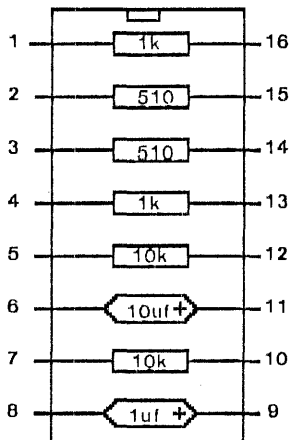
all resistors 1/8 watt

Note: Bourns has made a custom network for this platform.

16 pin platforms plugged into the middle  
of the 20 pin pattern

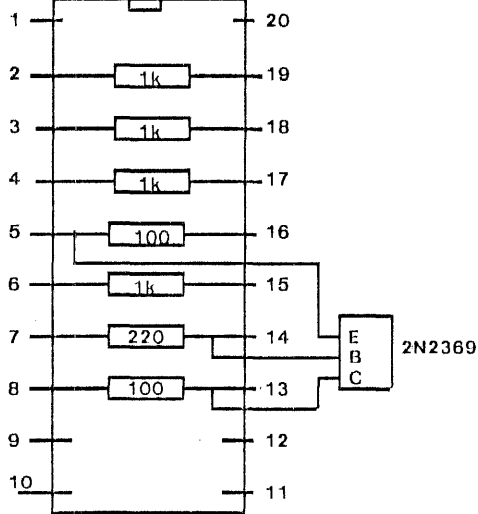
Pin 1 of plat goes in pin 2 of pattern

Plat in location e3



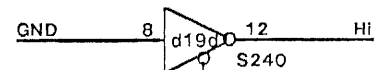
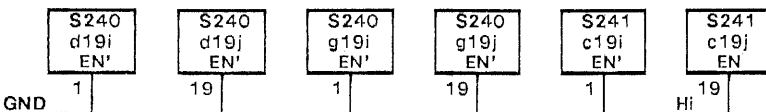
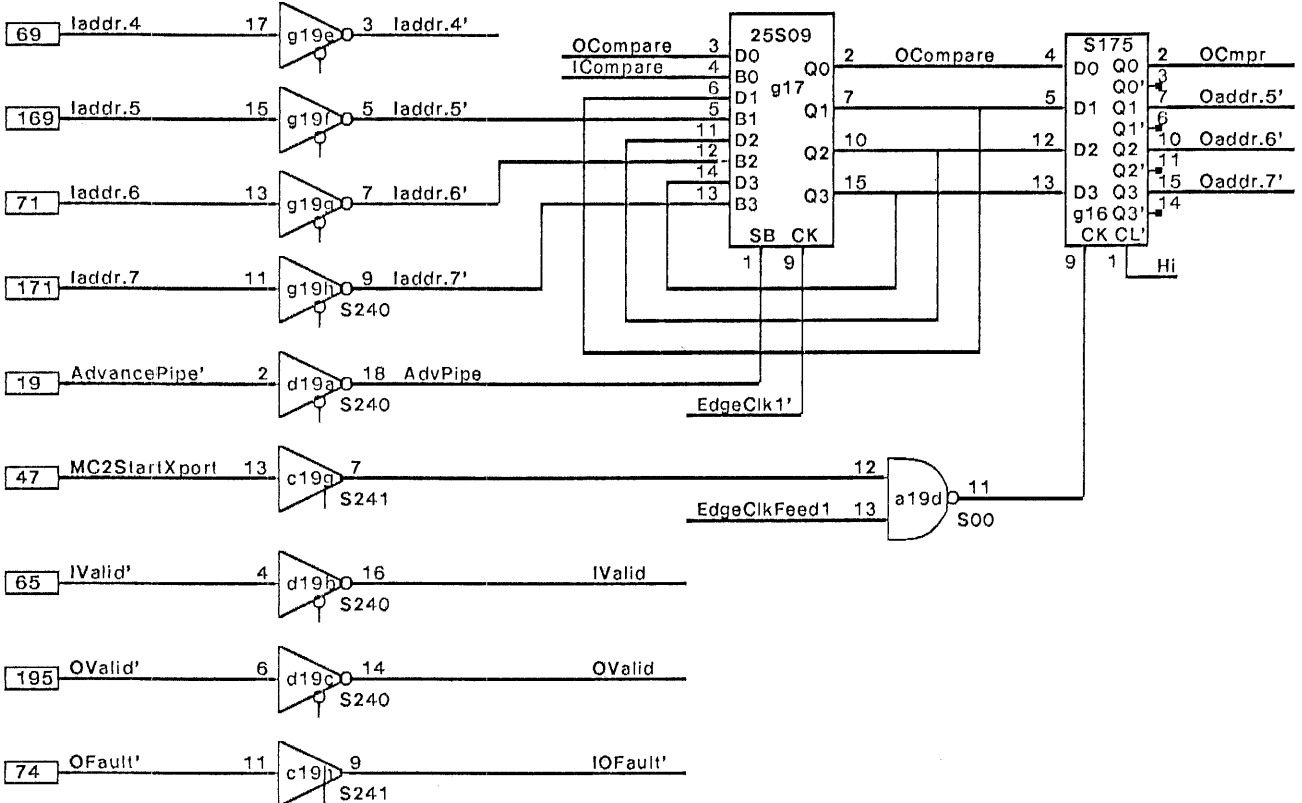
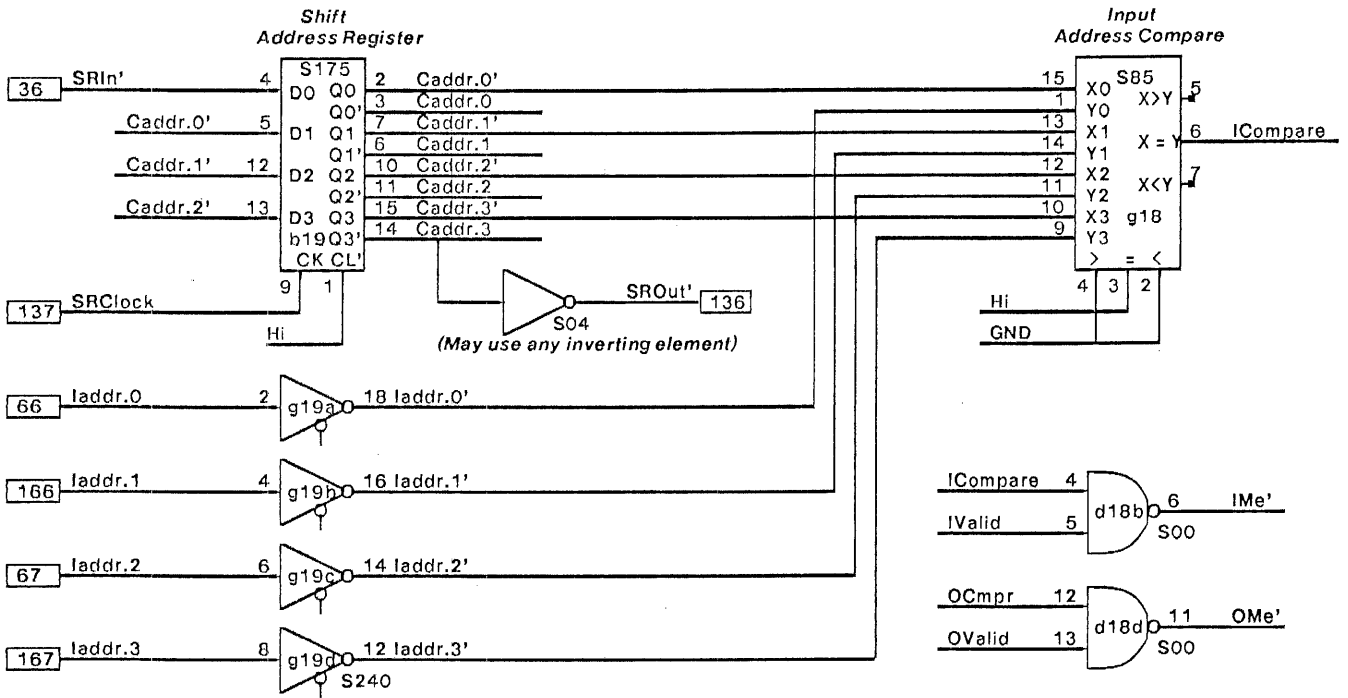
all resistors 1/4 watt  
all capacitors Tantalum

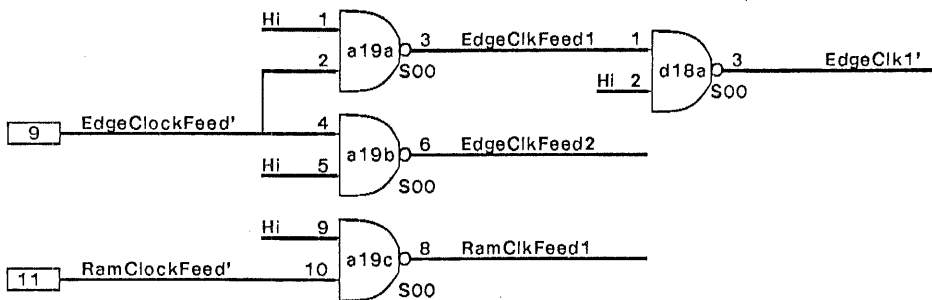
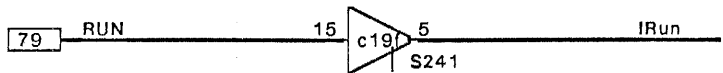
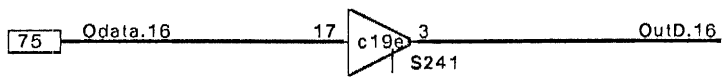
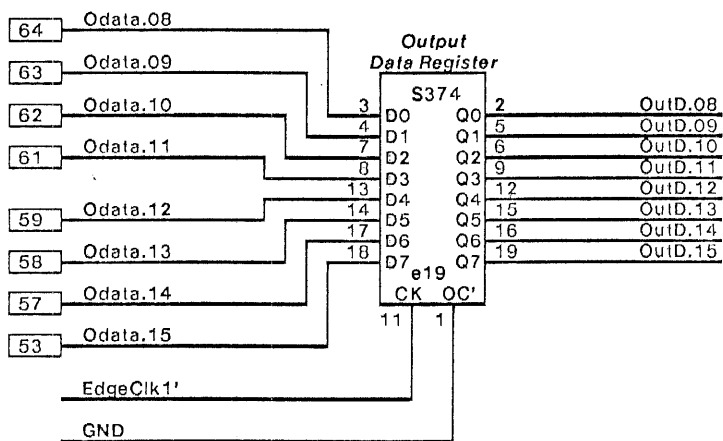
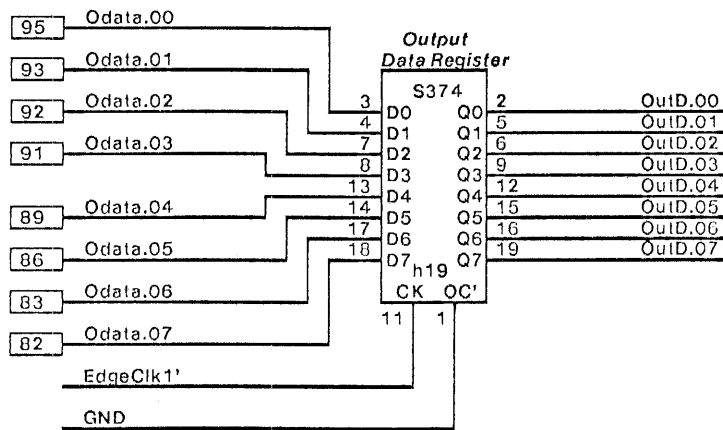
Plat in location e2

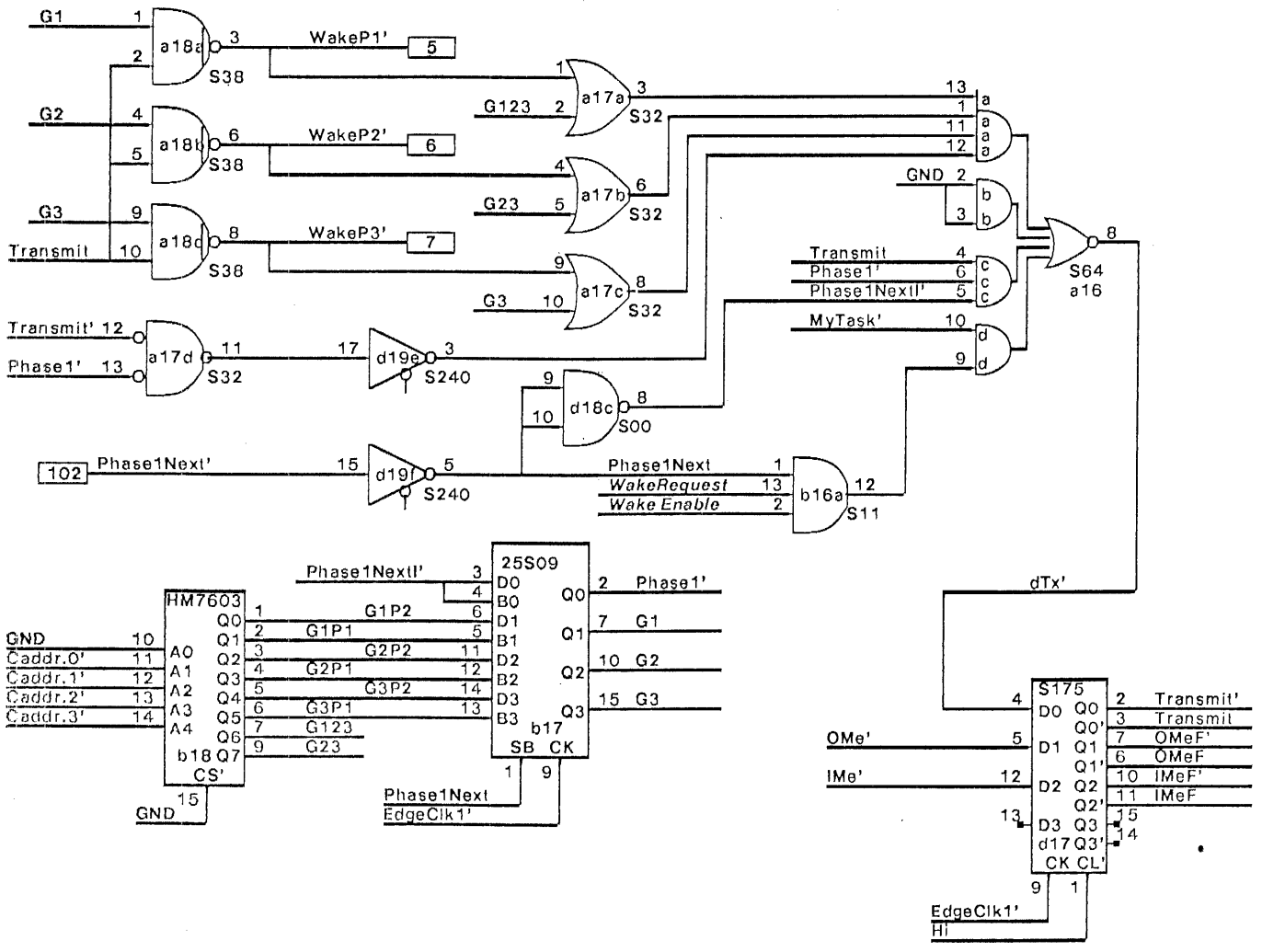


all resistors 1/4 watt

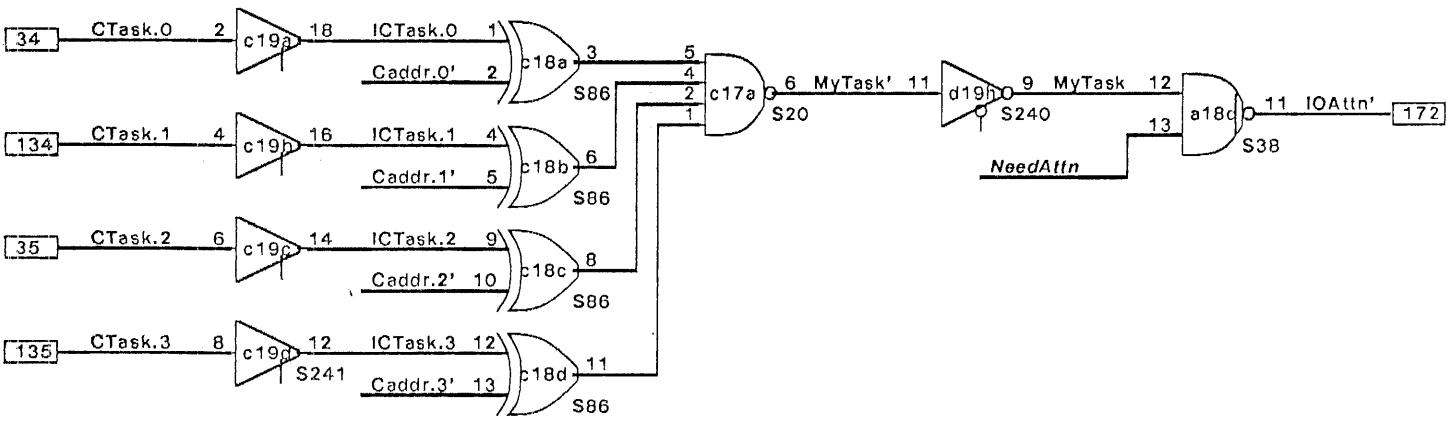


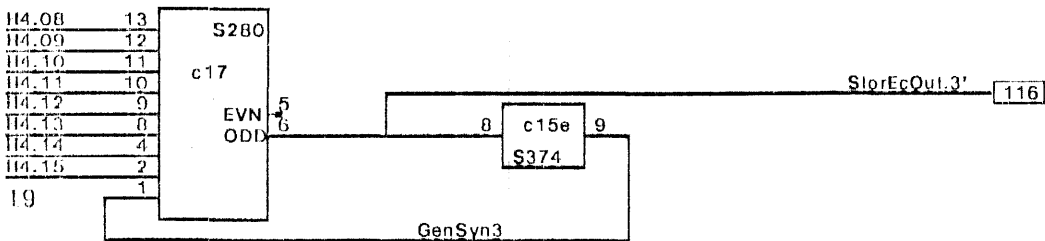
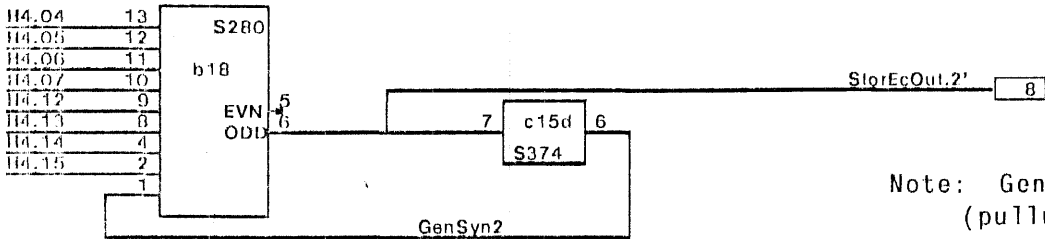
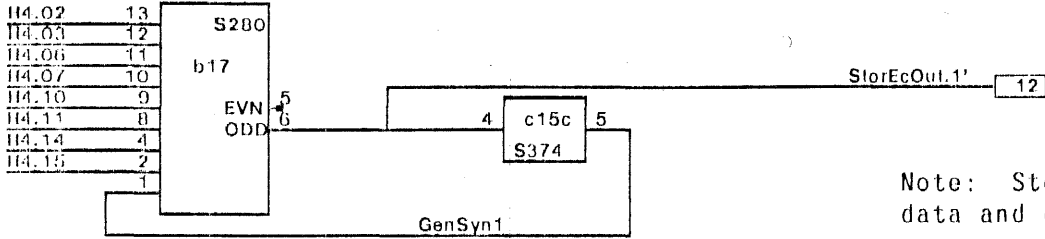
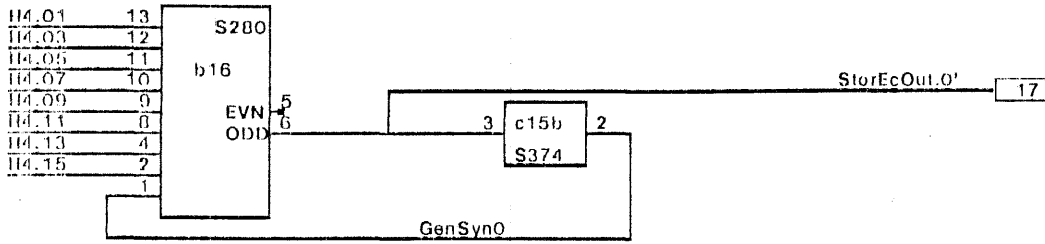






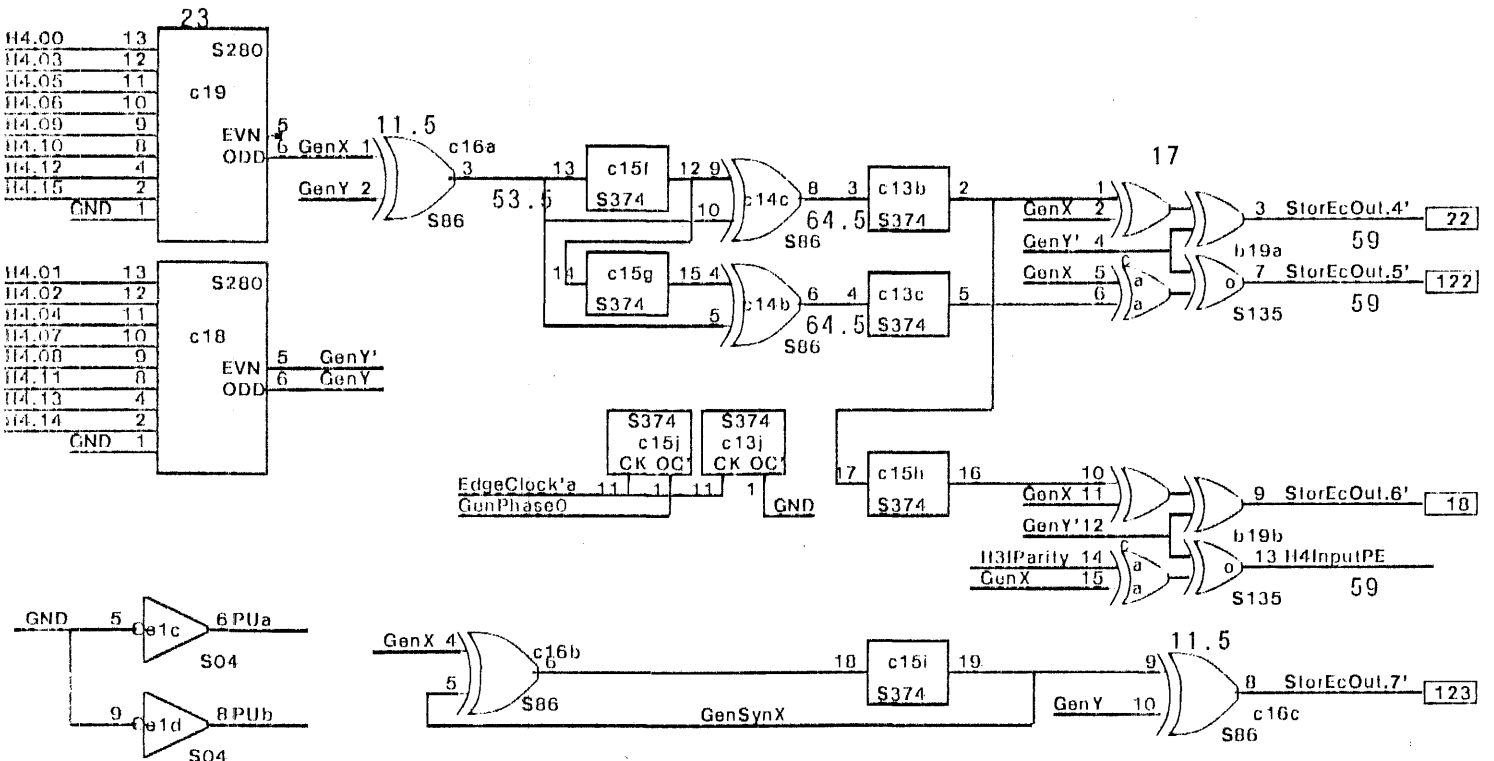
147 IOStrobe

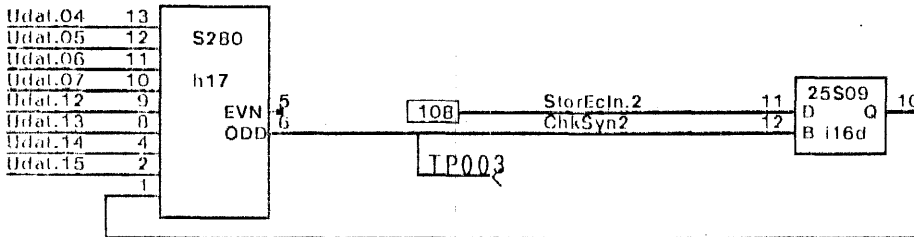
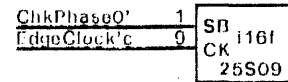
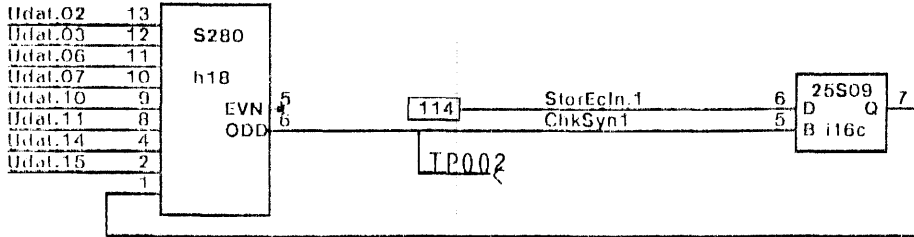
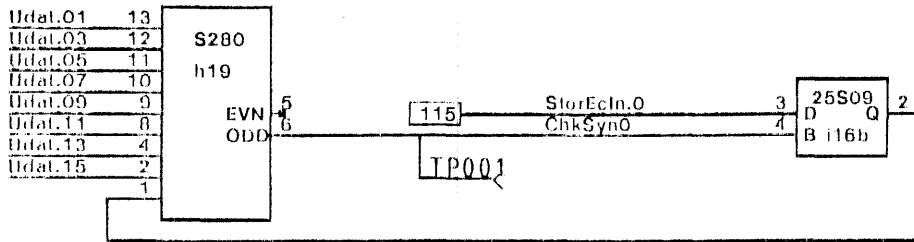




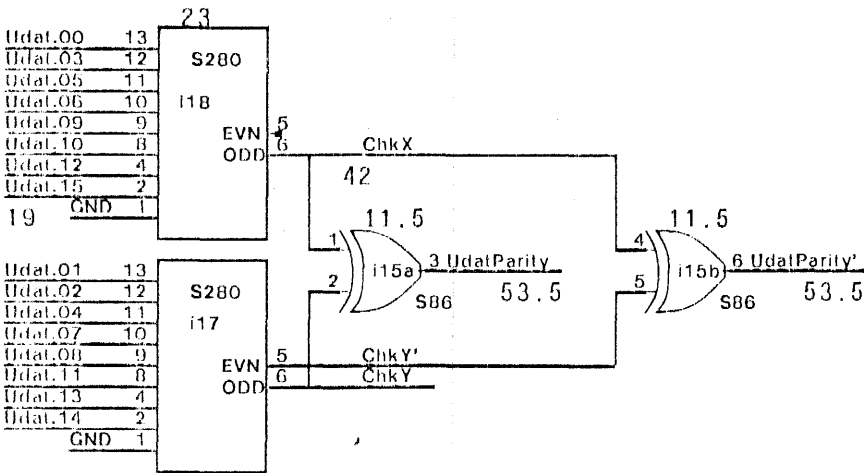
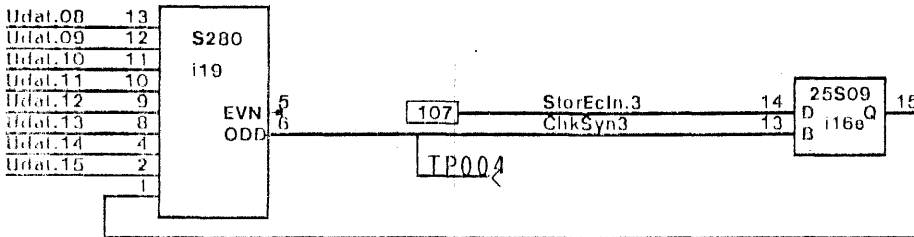
Note: Storage card inverts data and check bits.

Note: GenPhase0 => GenSyn0,1,2,3,X = (pullups on page 12)

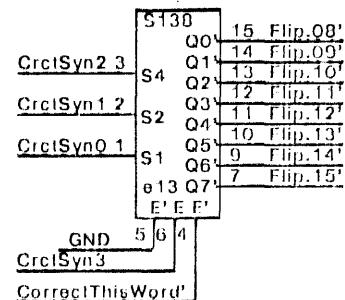
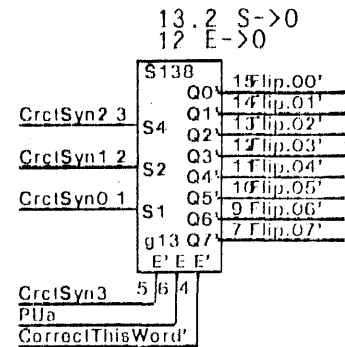


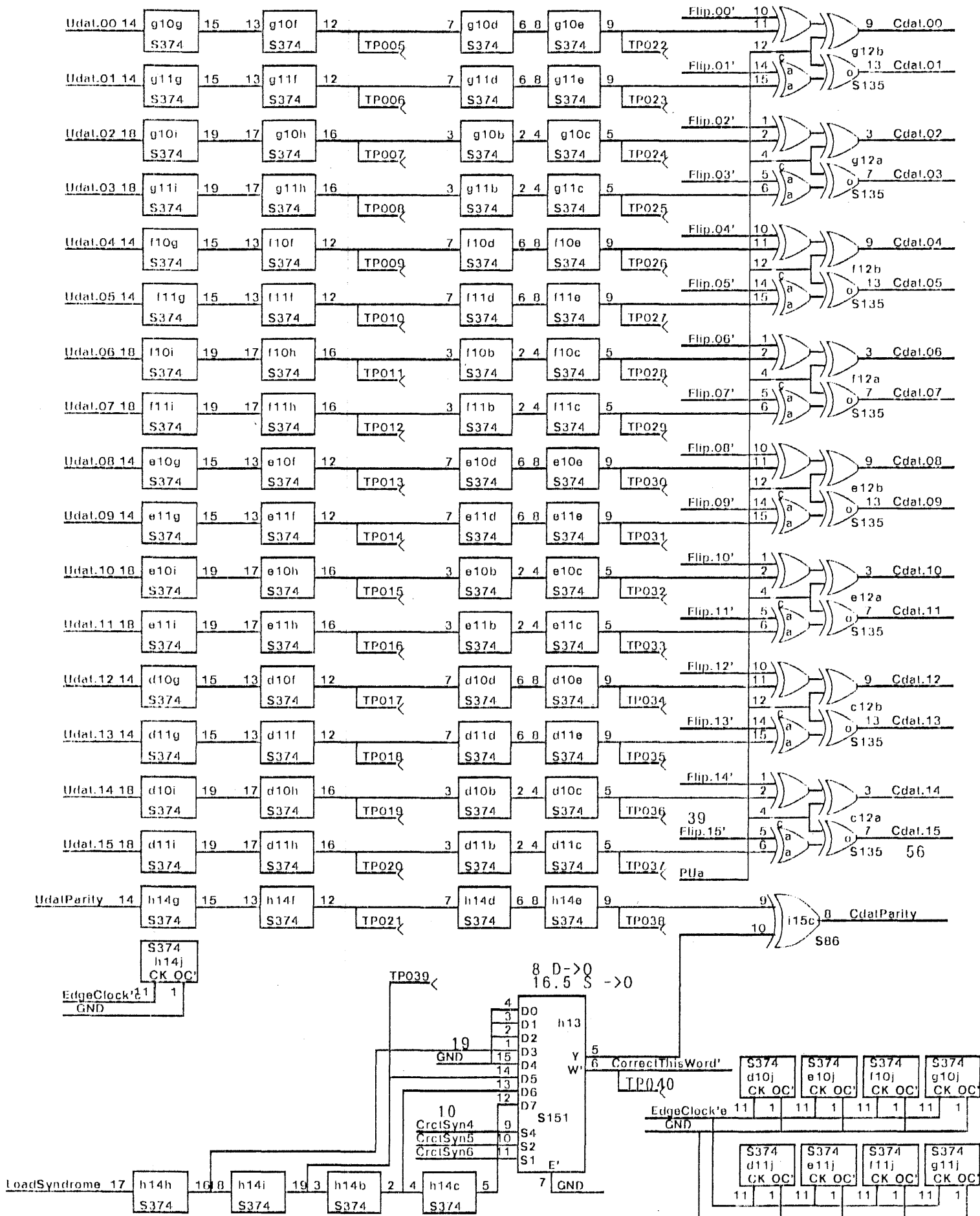


Note: Storage card inverts data and check bits

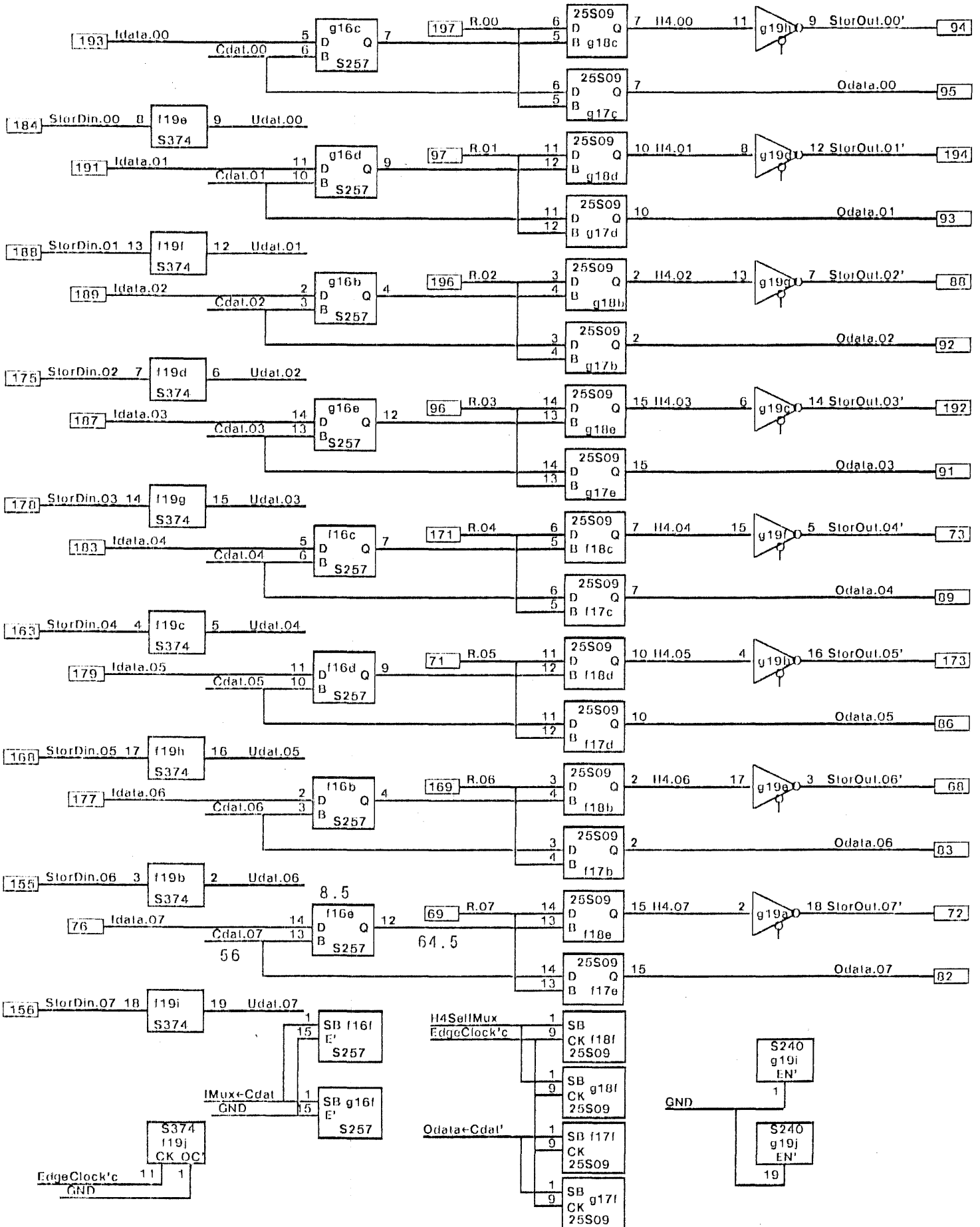


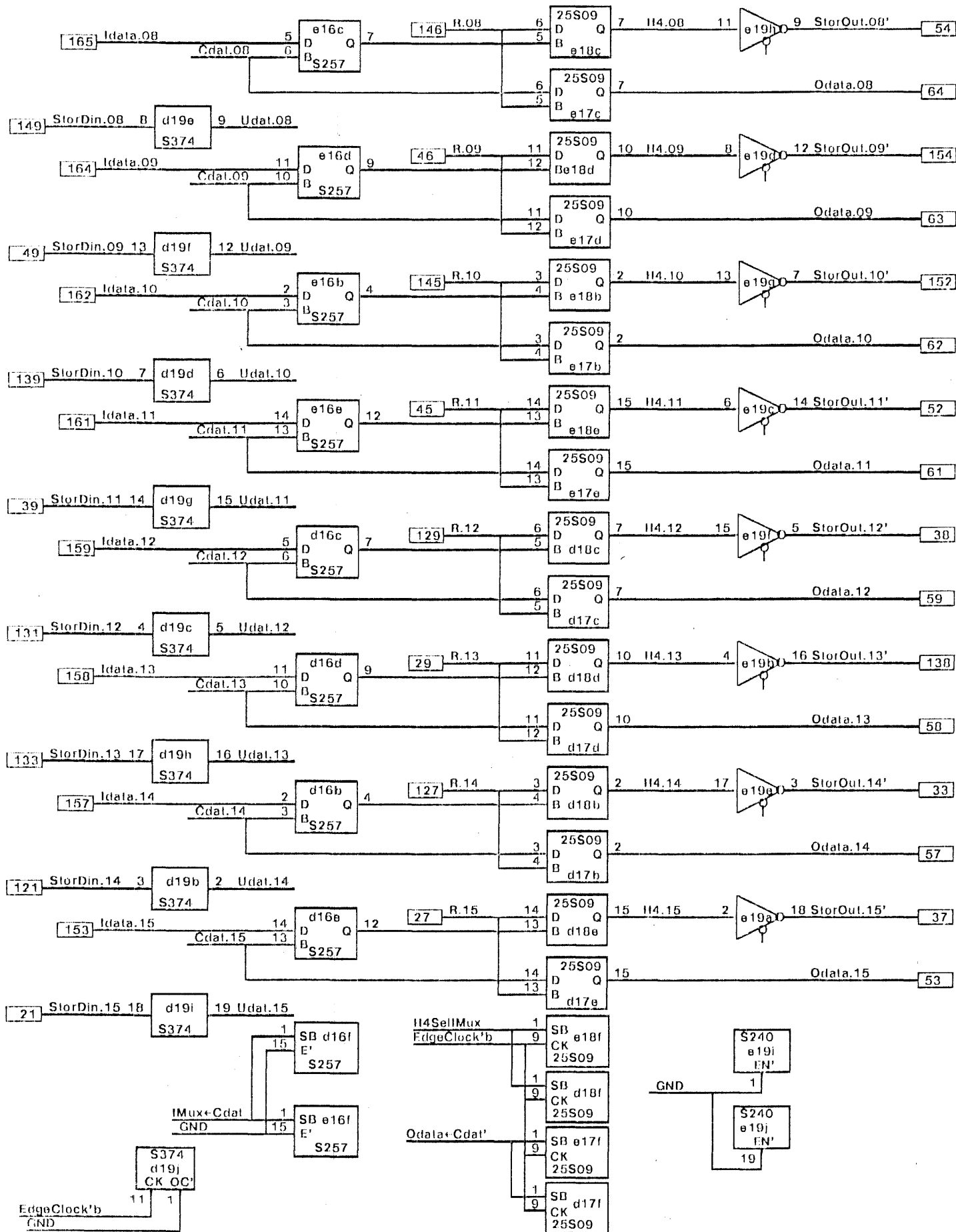
Note: Balance of checker is on pg. 6



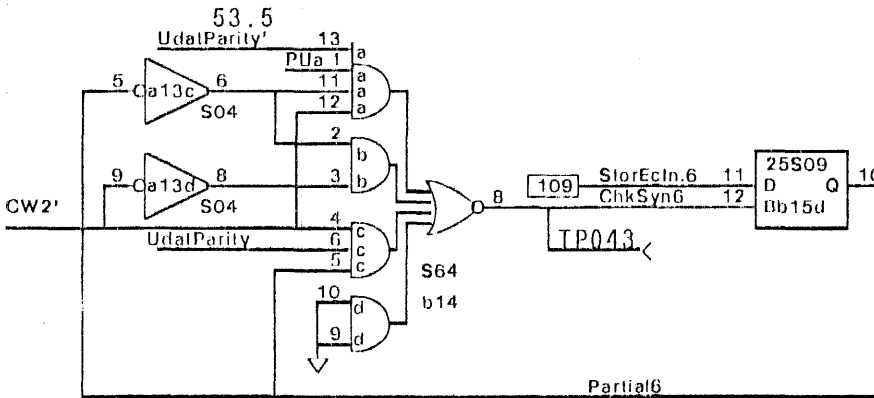
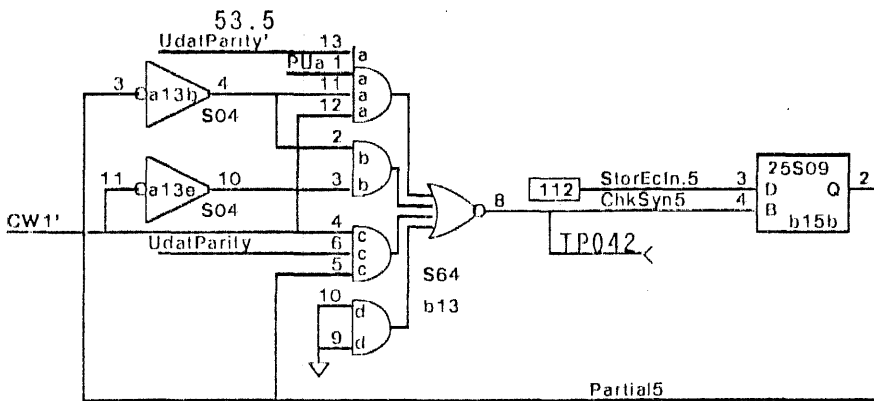
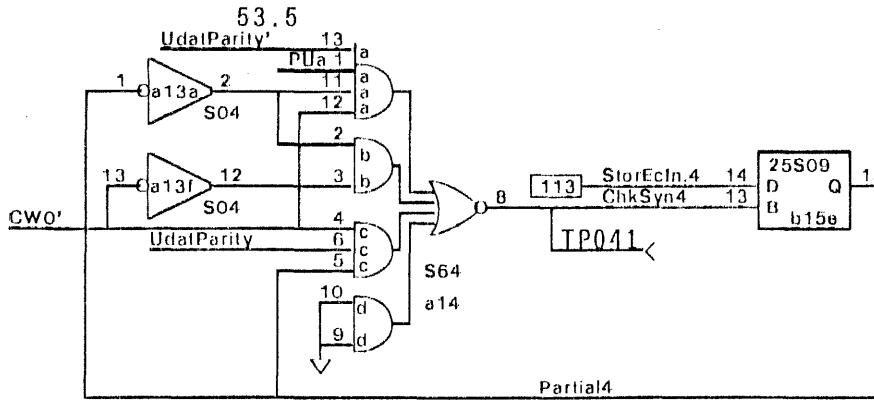








Note: Storage card inverts data and check bits

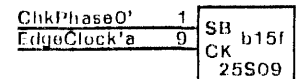
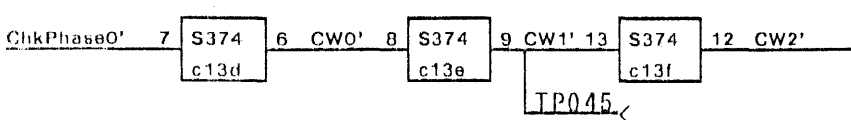
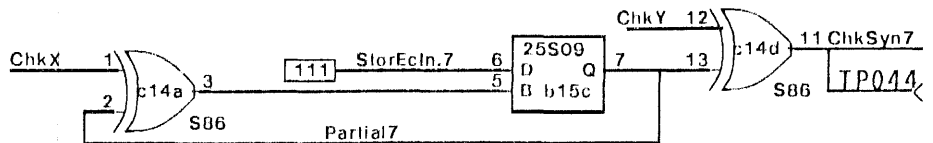


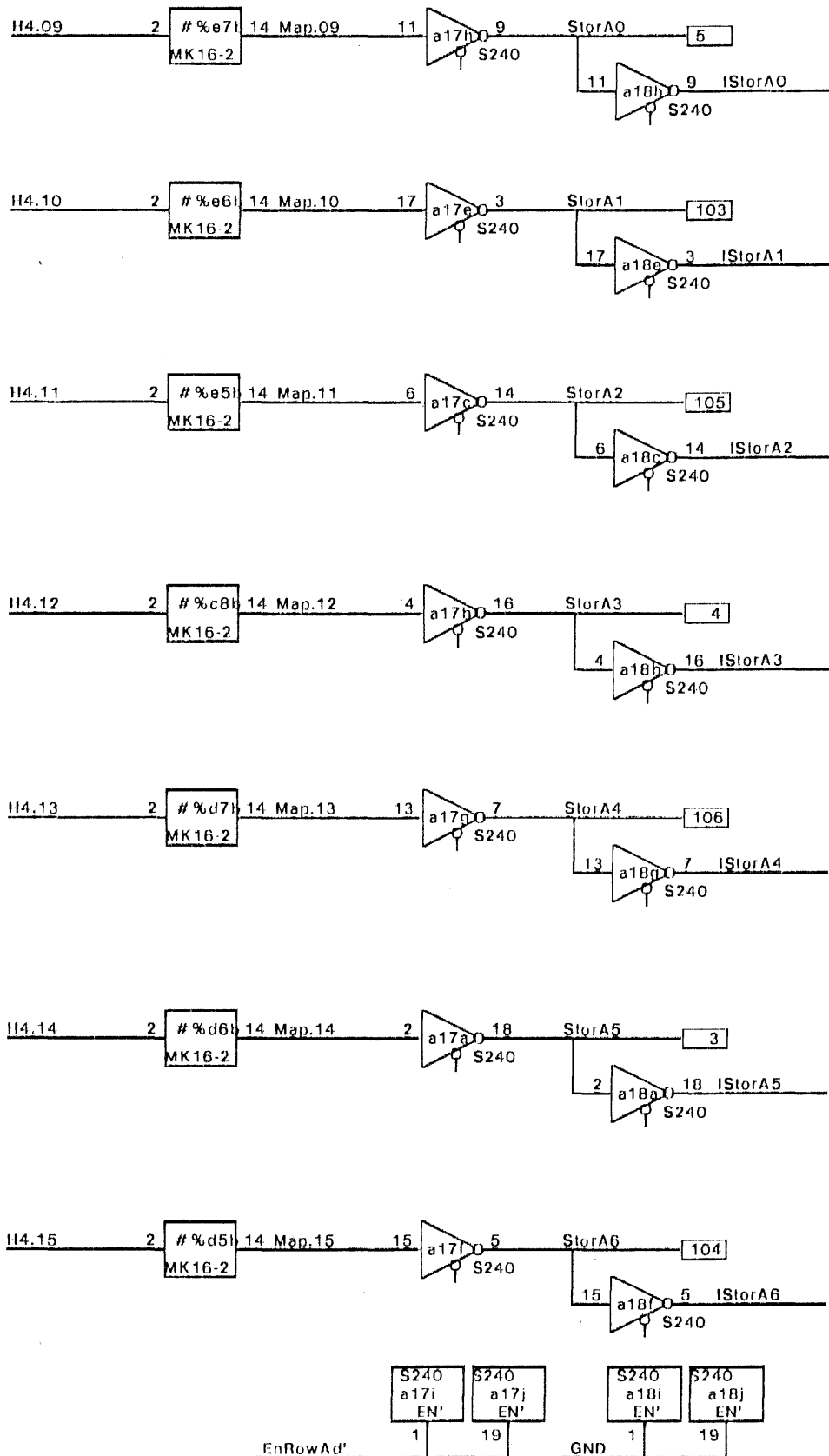
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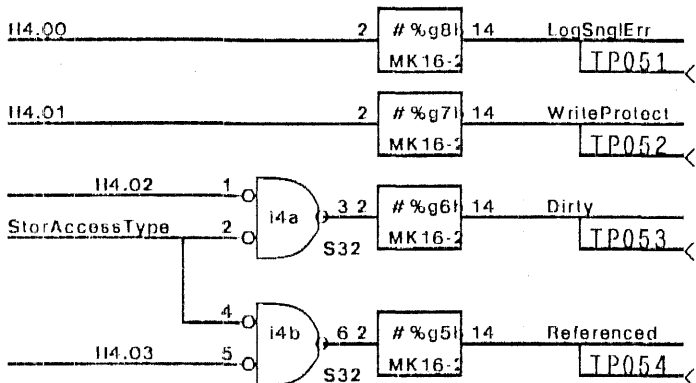
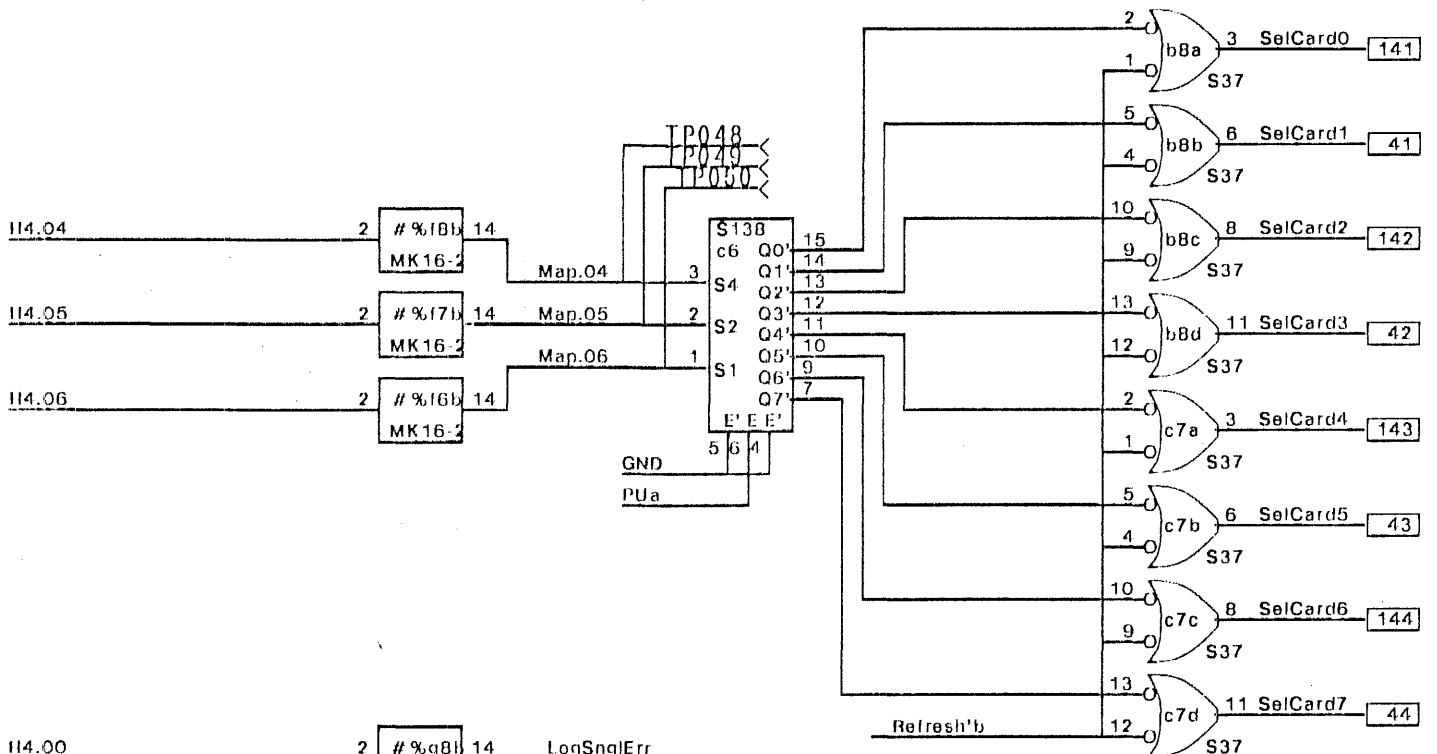
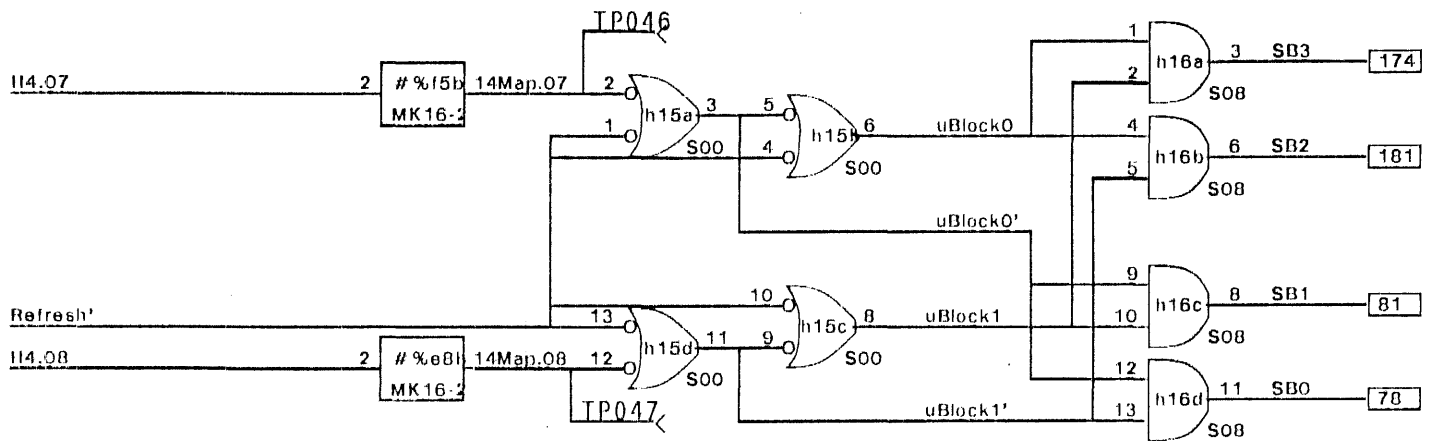
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1	0	1
1	1	0

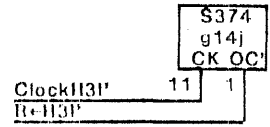
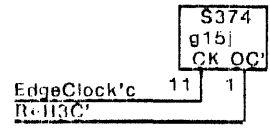
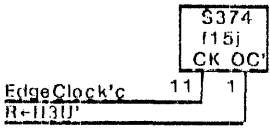
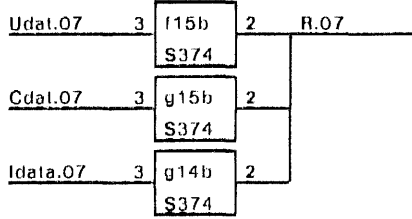
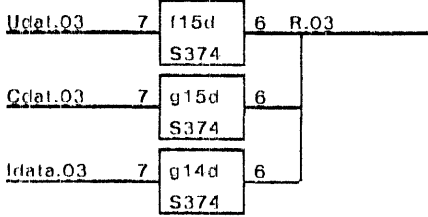
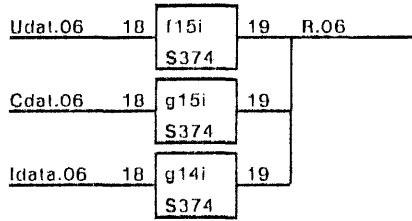
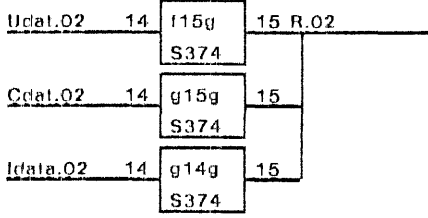
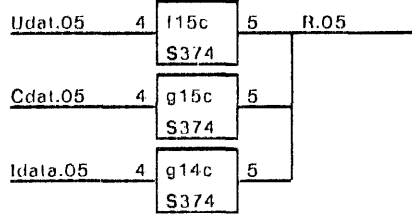
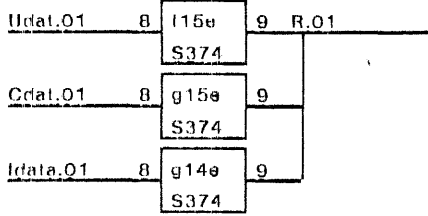
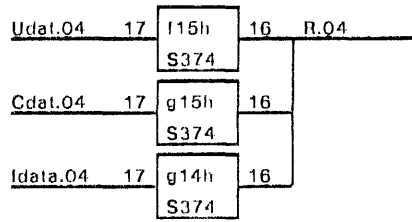
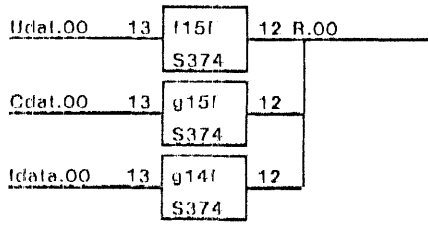
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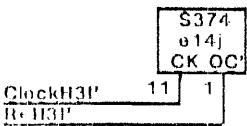
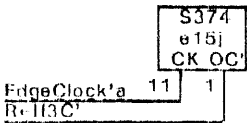
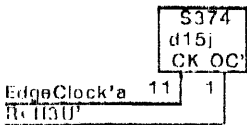
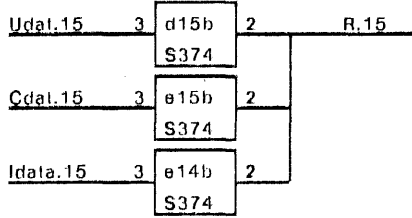
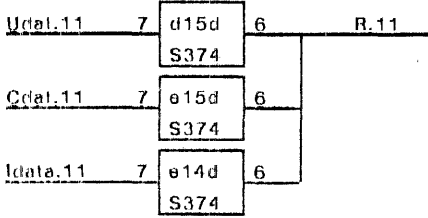
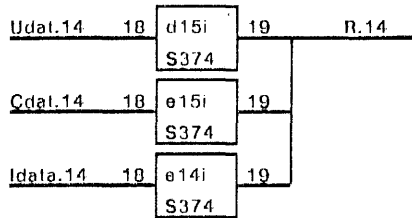
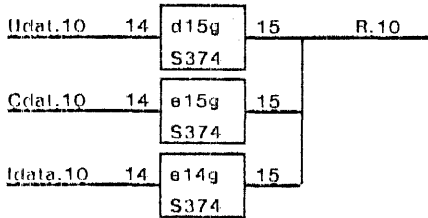
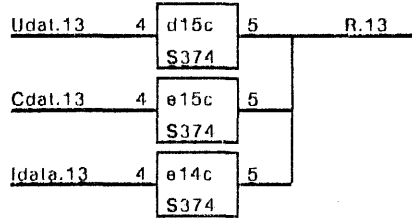
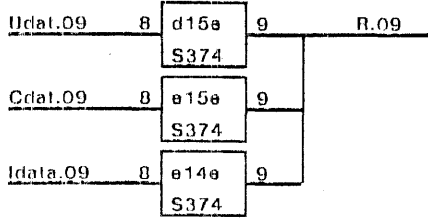
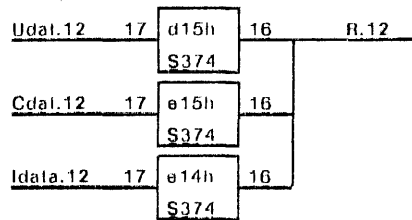
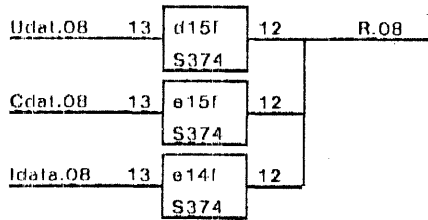
Partial5	ChkSyn5
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1	1



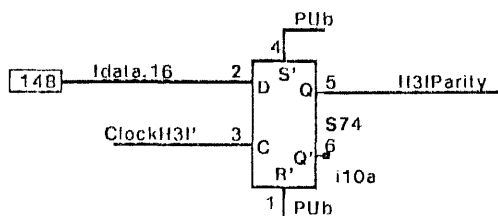
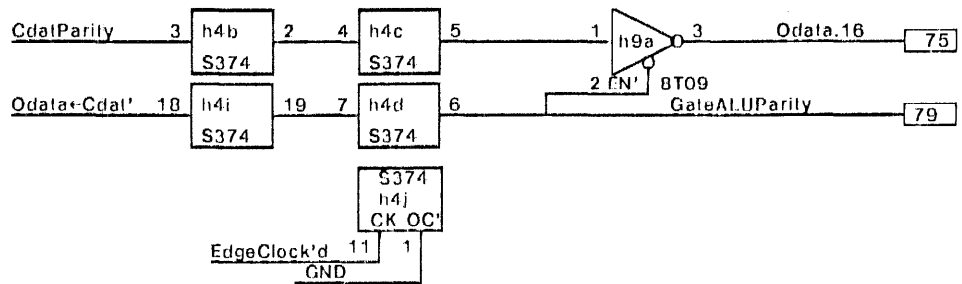


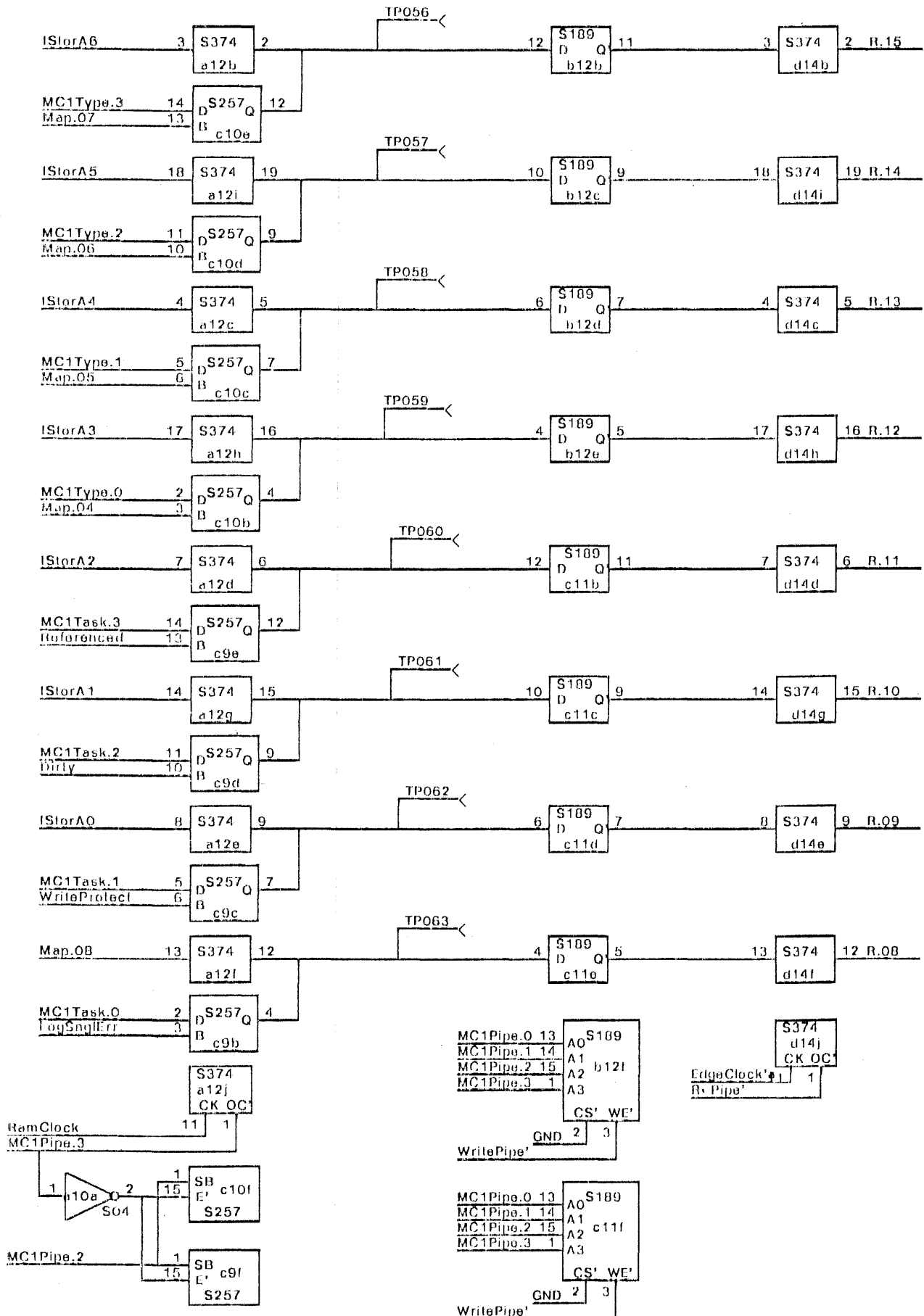




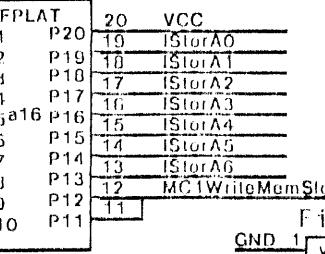
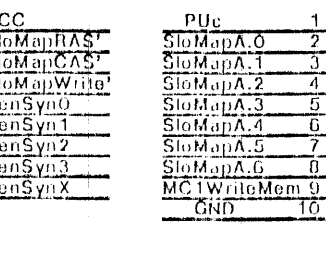
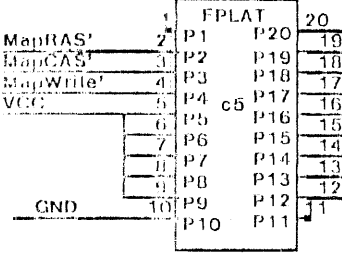
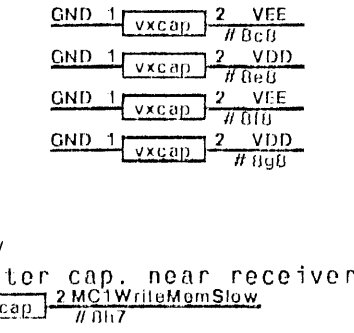
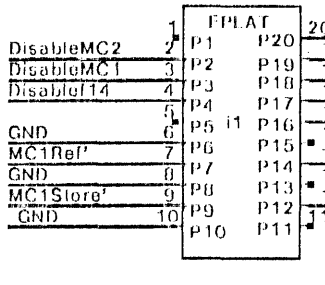
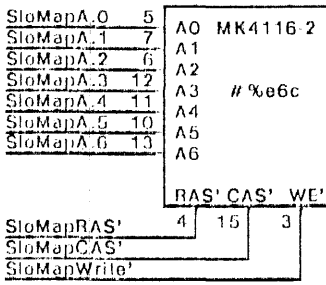
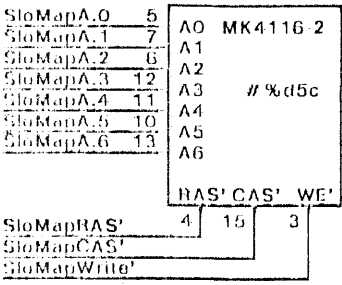
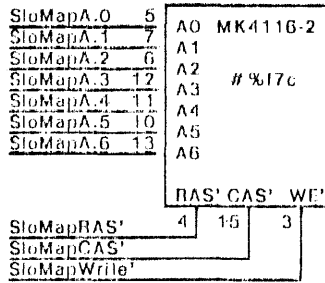
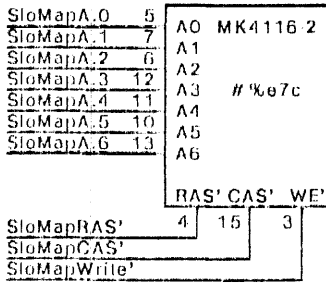
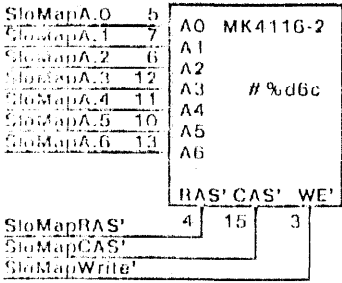
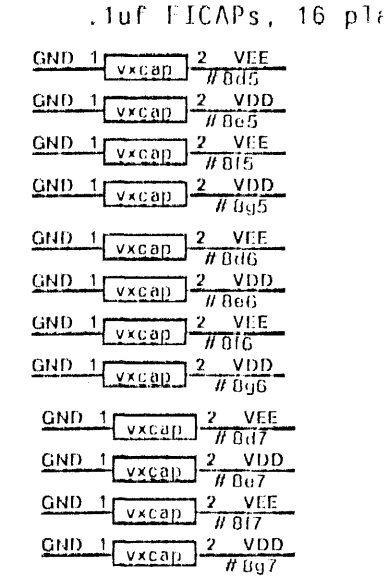
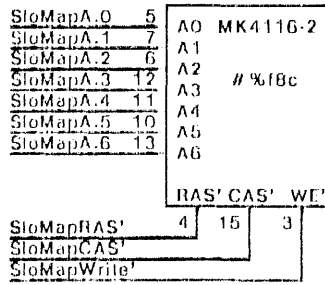
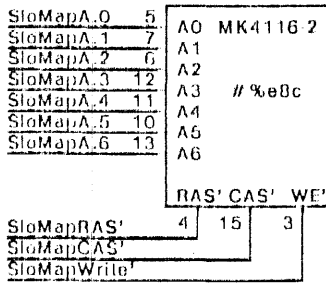
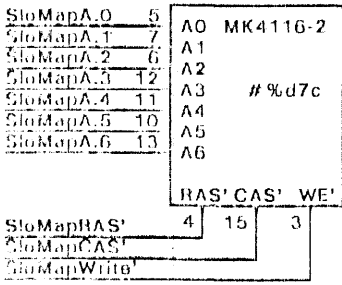
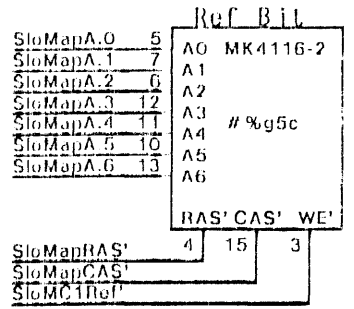
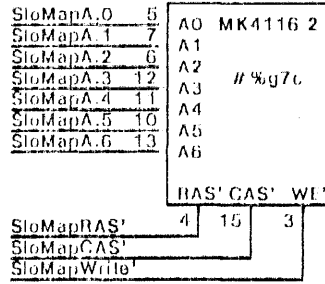
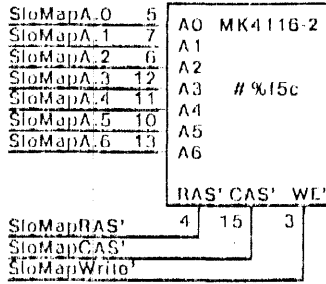
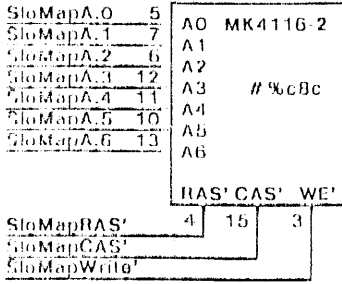
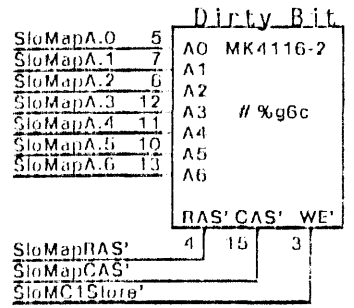
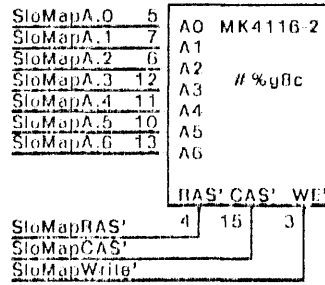
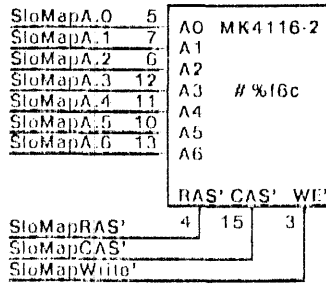
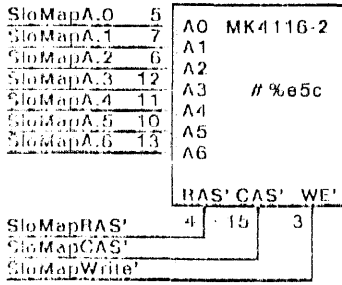


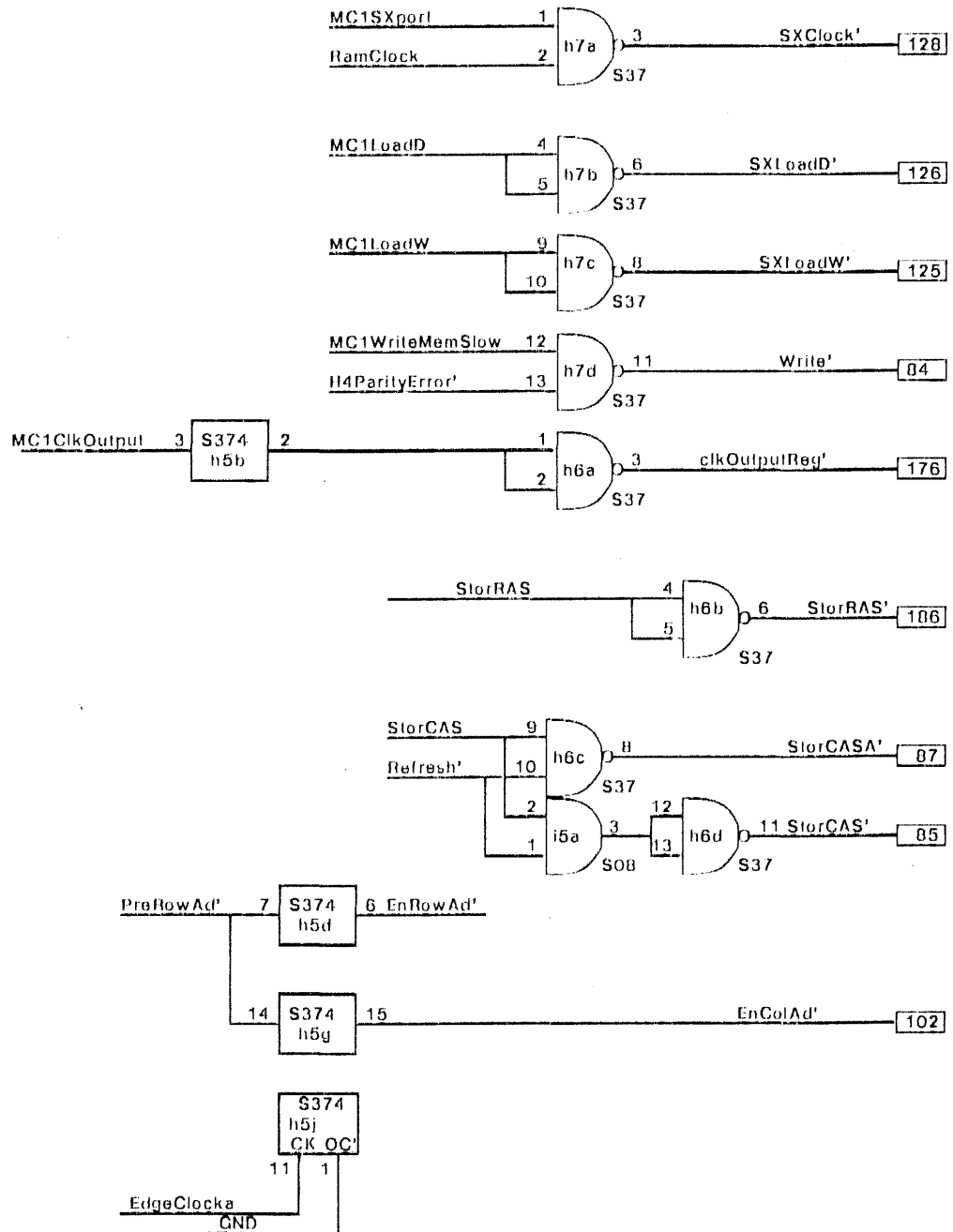
ALU Card supplies parity on OUTPUT

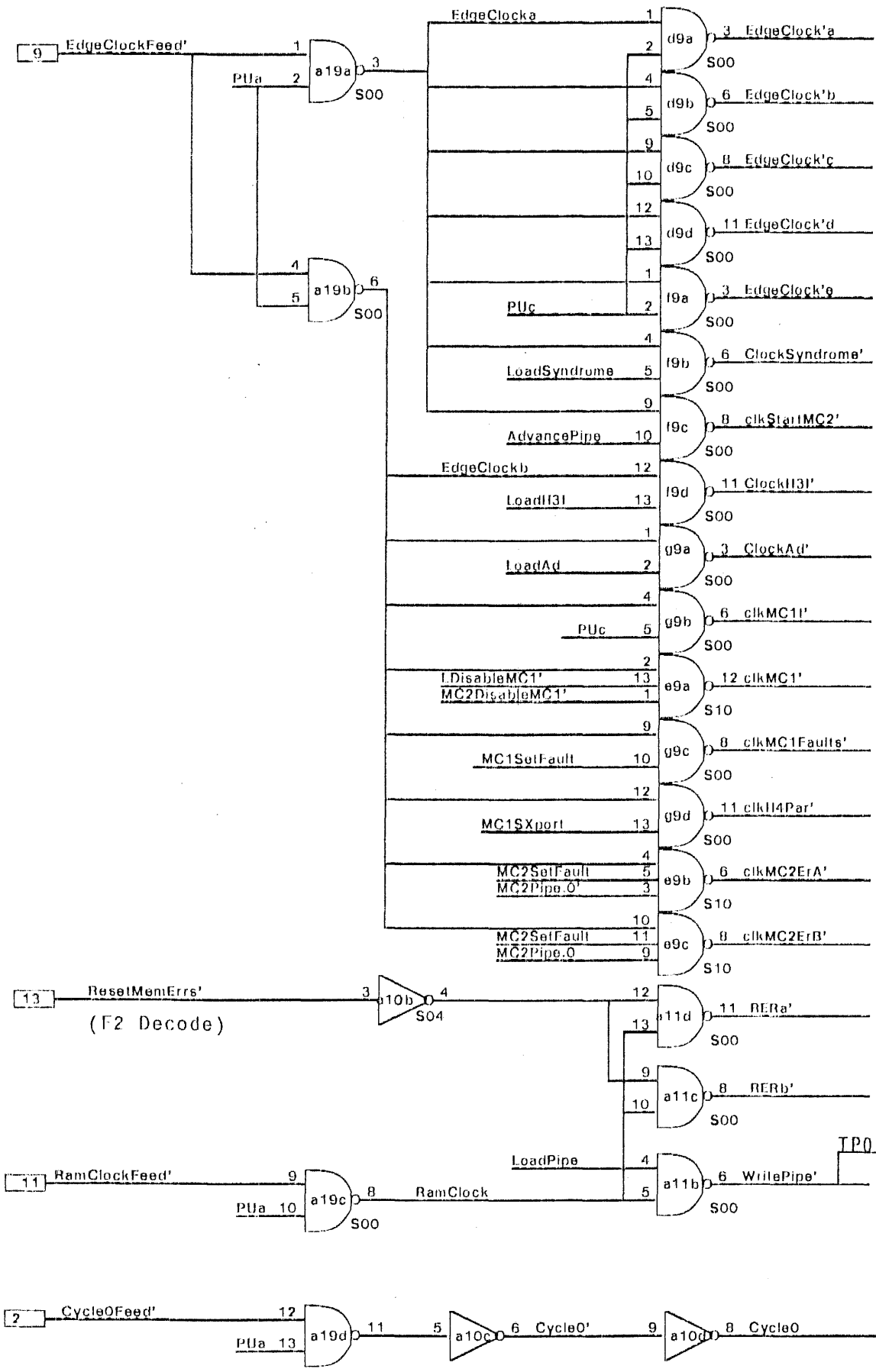




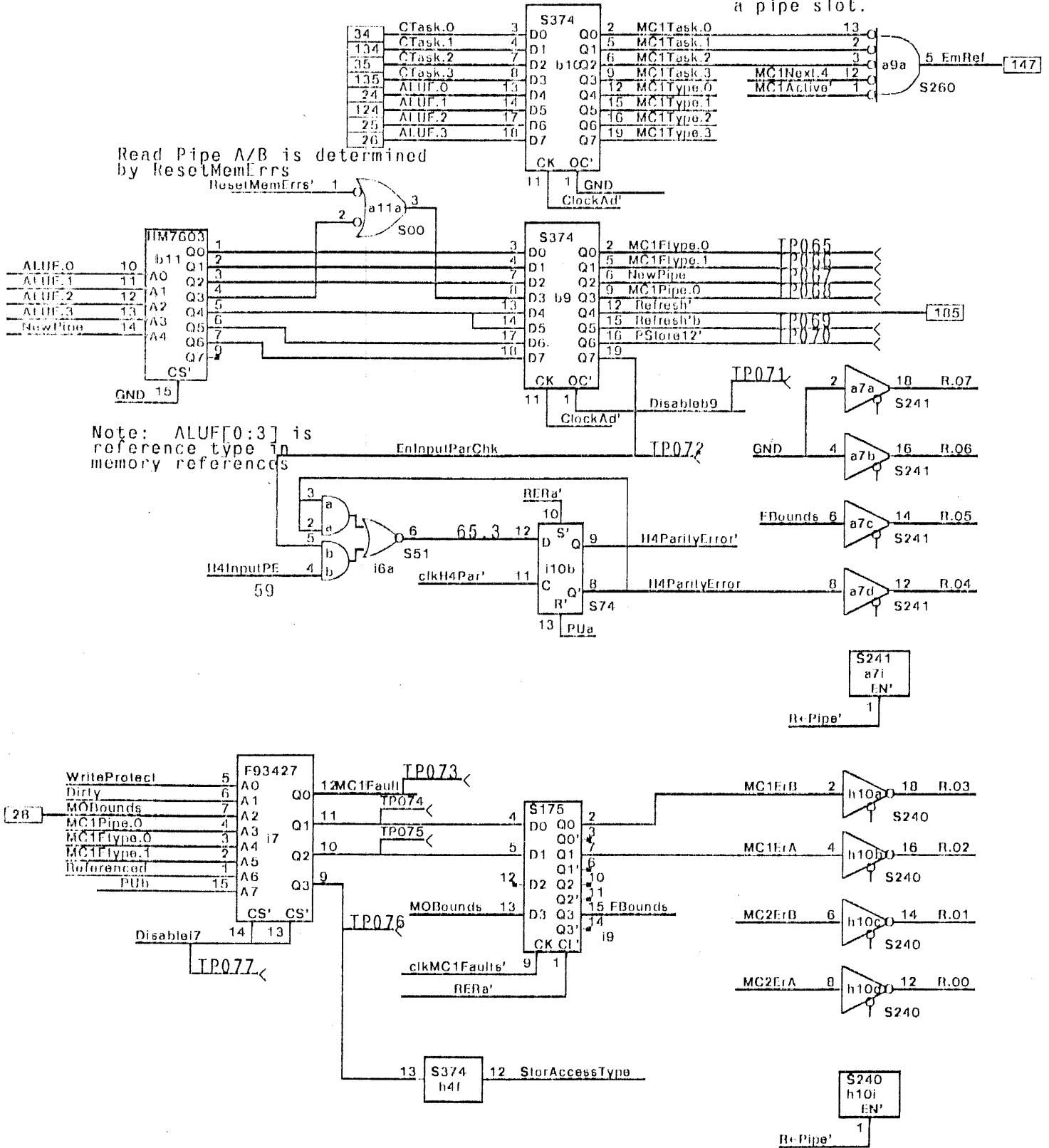


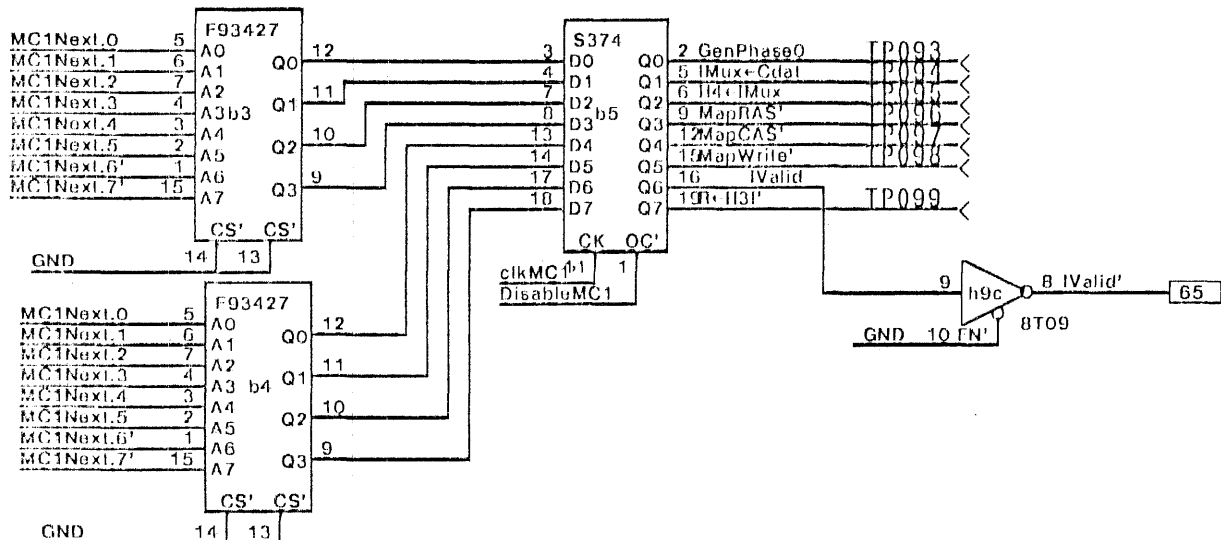
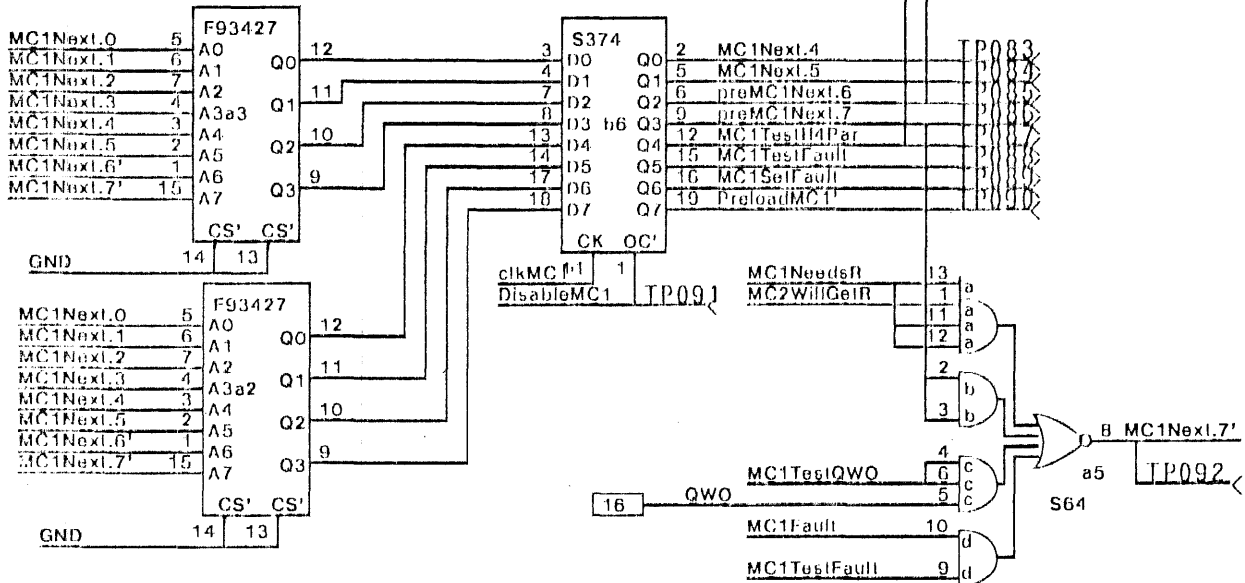
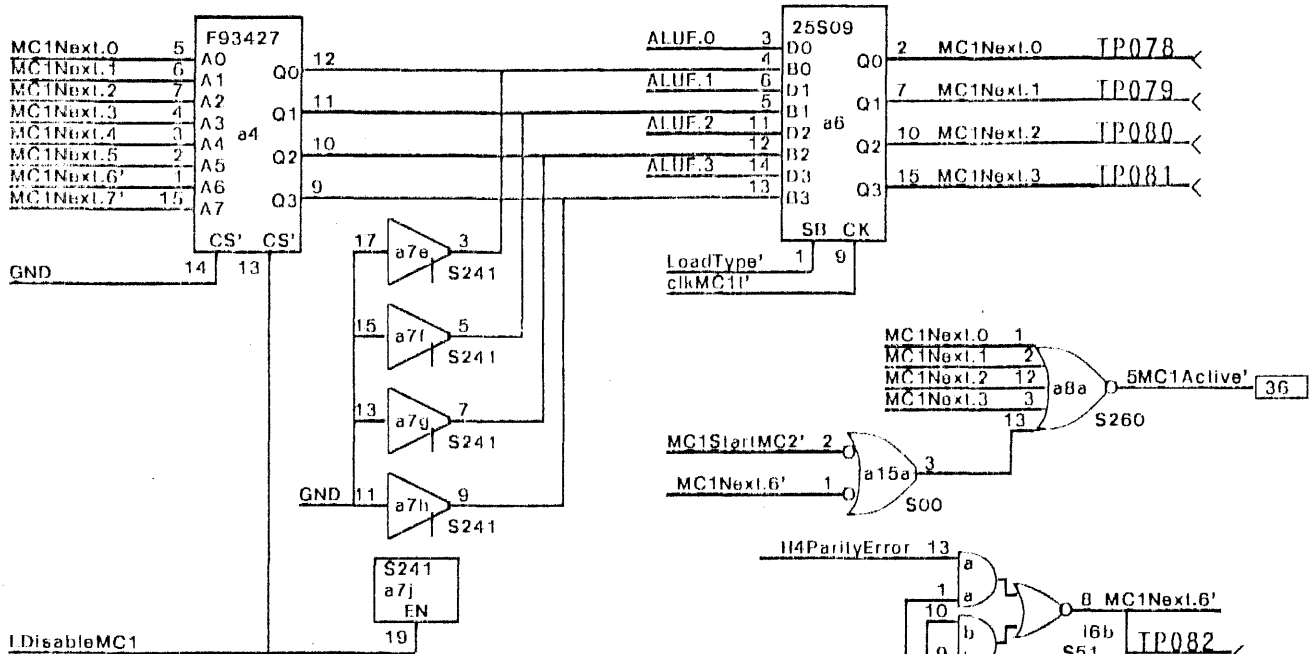


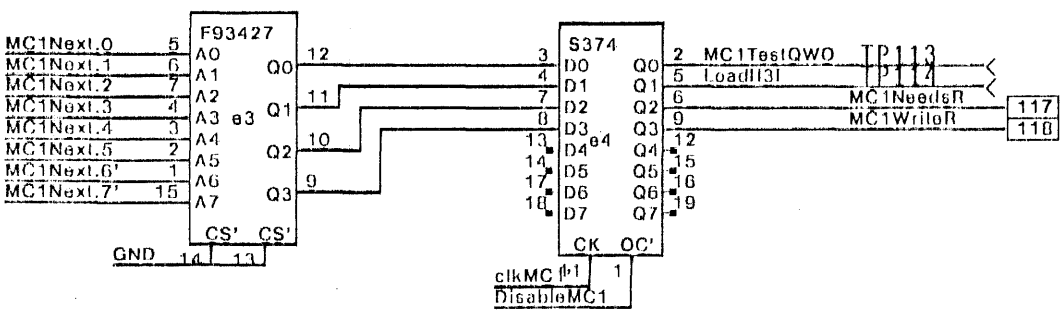
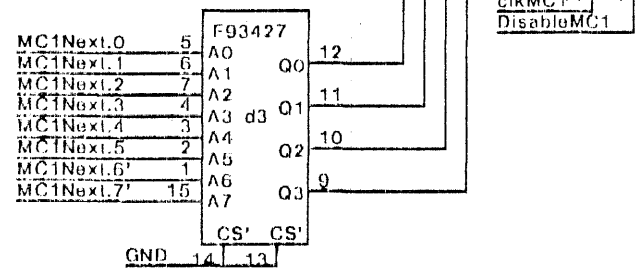
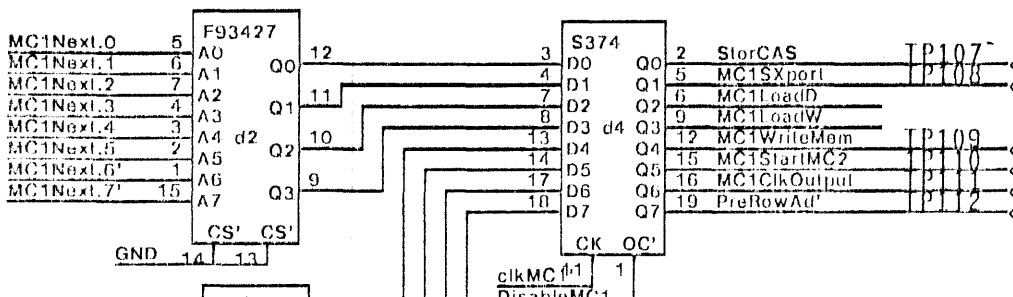
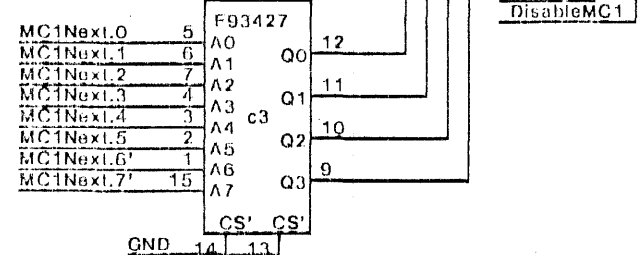
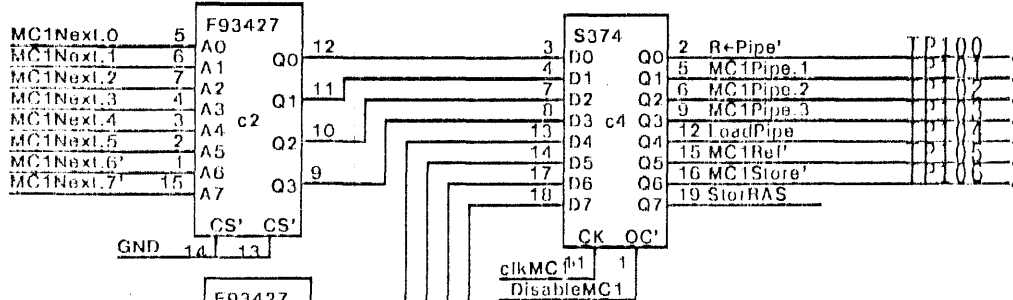


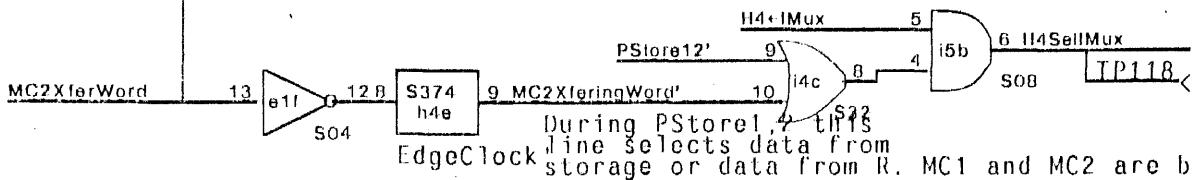
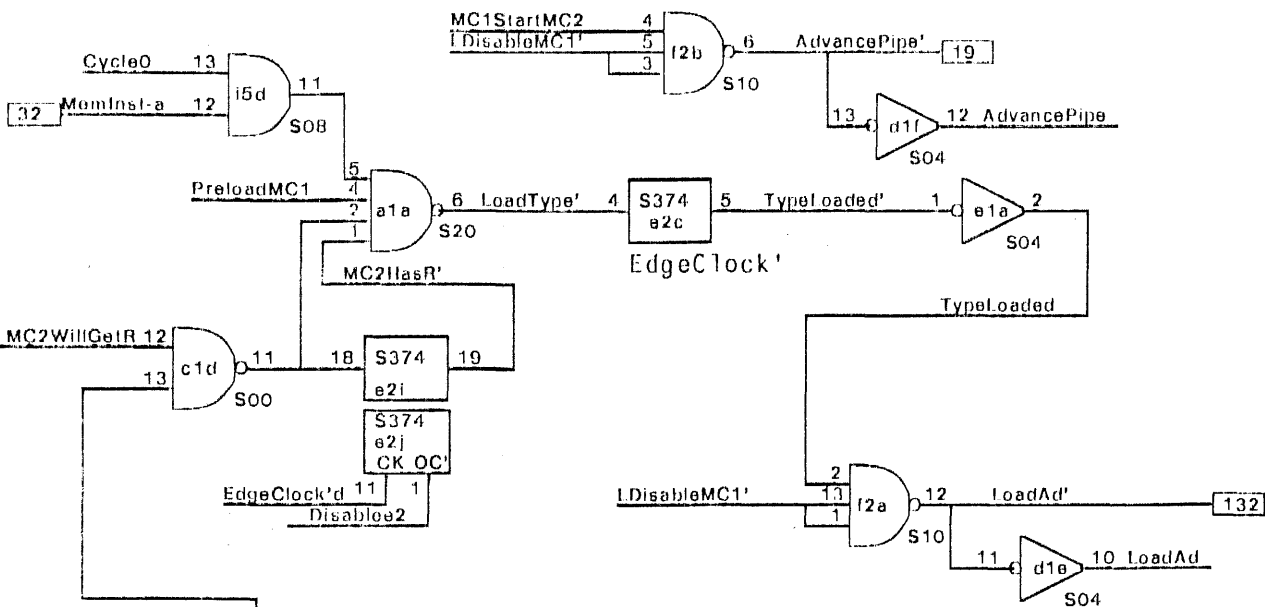
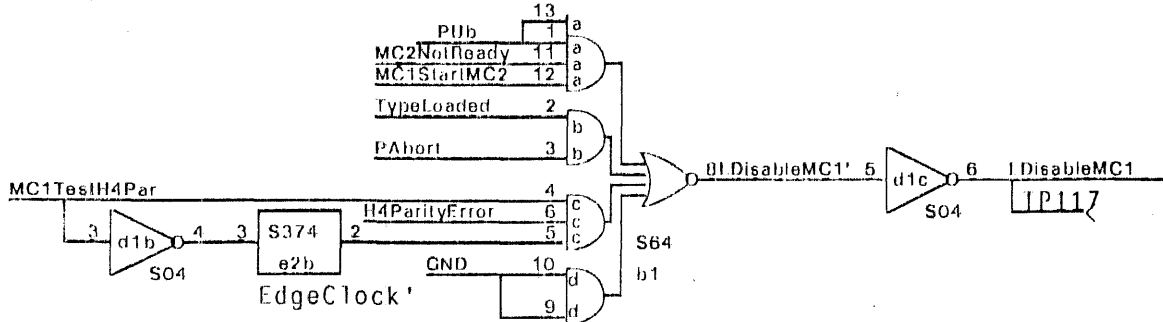
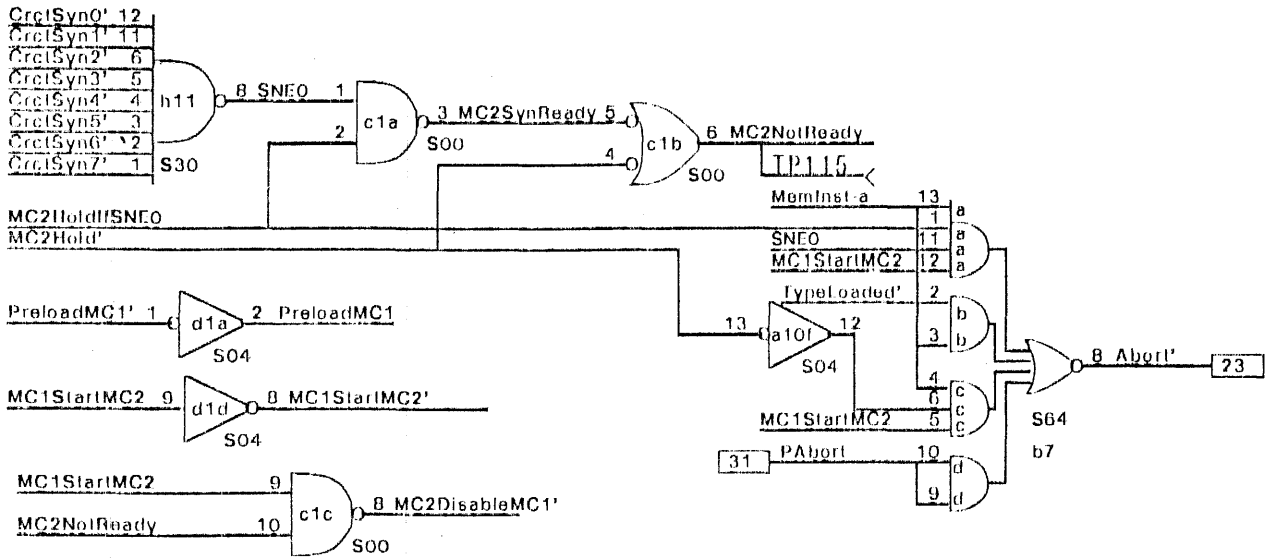


Ftype classifies references according to the types of faults they can cause: Non-memory/Fetch/Store. References are also classified as to whether or not they use a pipe slot.

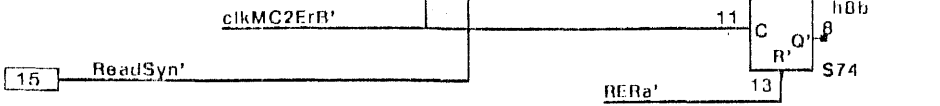
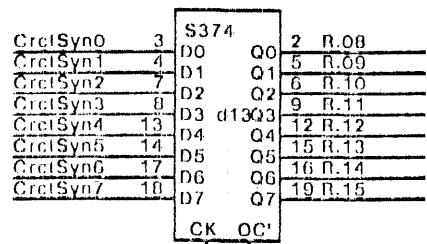
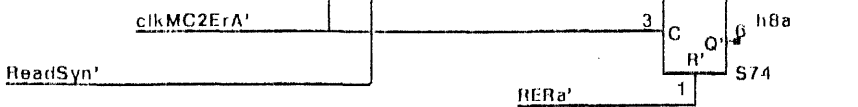
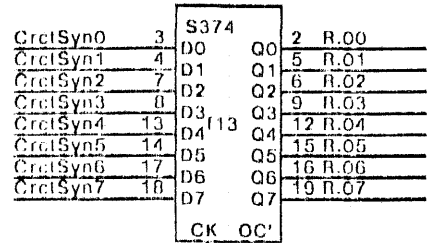
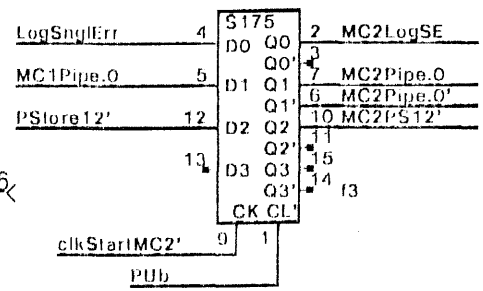
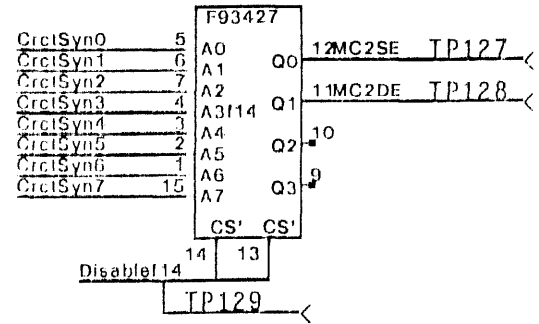
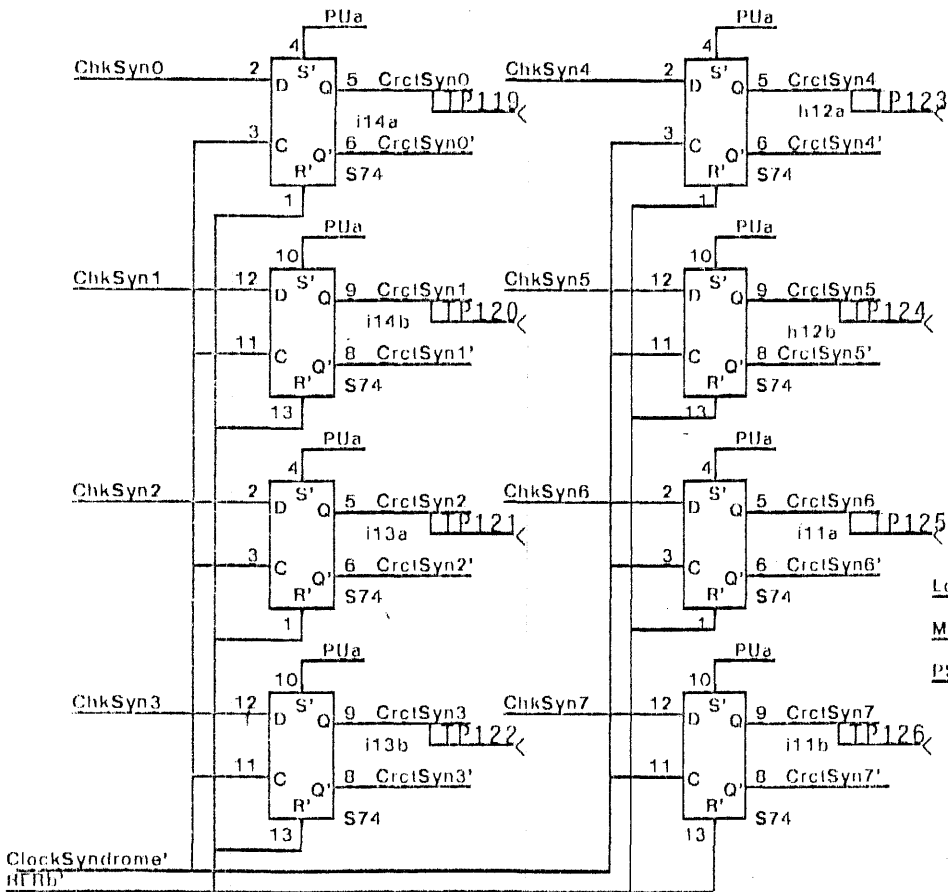




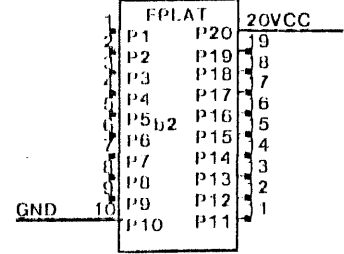




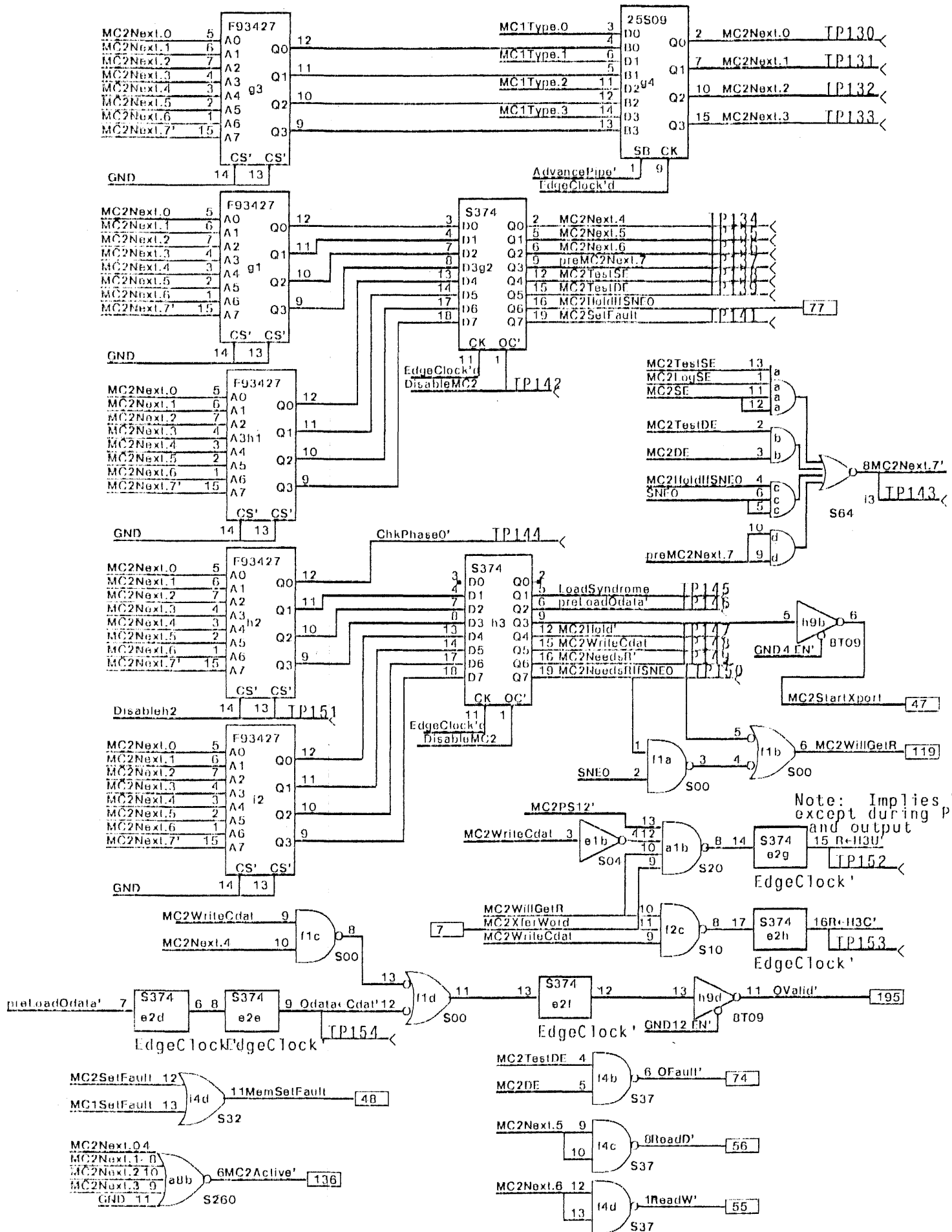
During PStore1, 4, 11, 18  
 EdgeClock line selects data from  
 storage or data from R. MC1 and MC2 are both active.



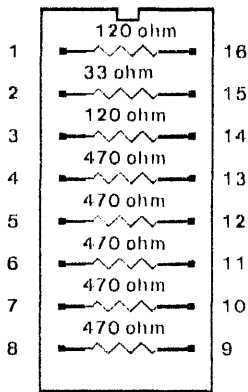
Spare Position



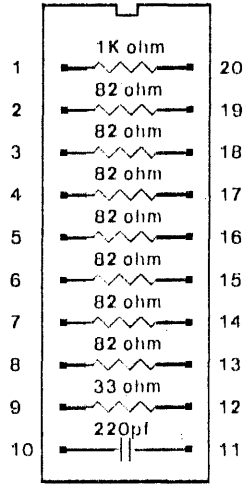




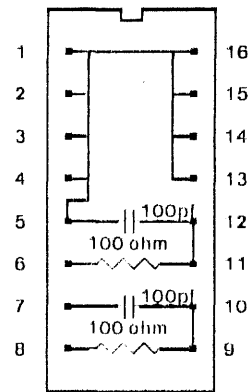
Note: Implies W# except during PS# and output



Position c5

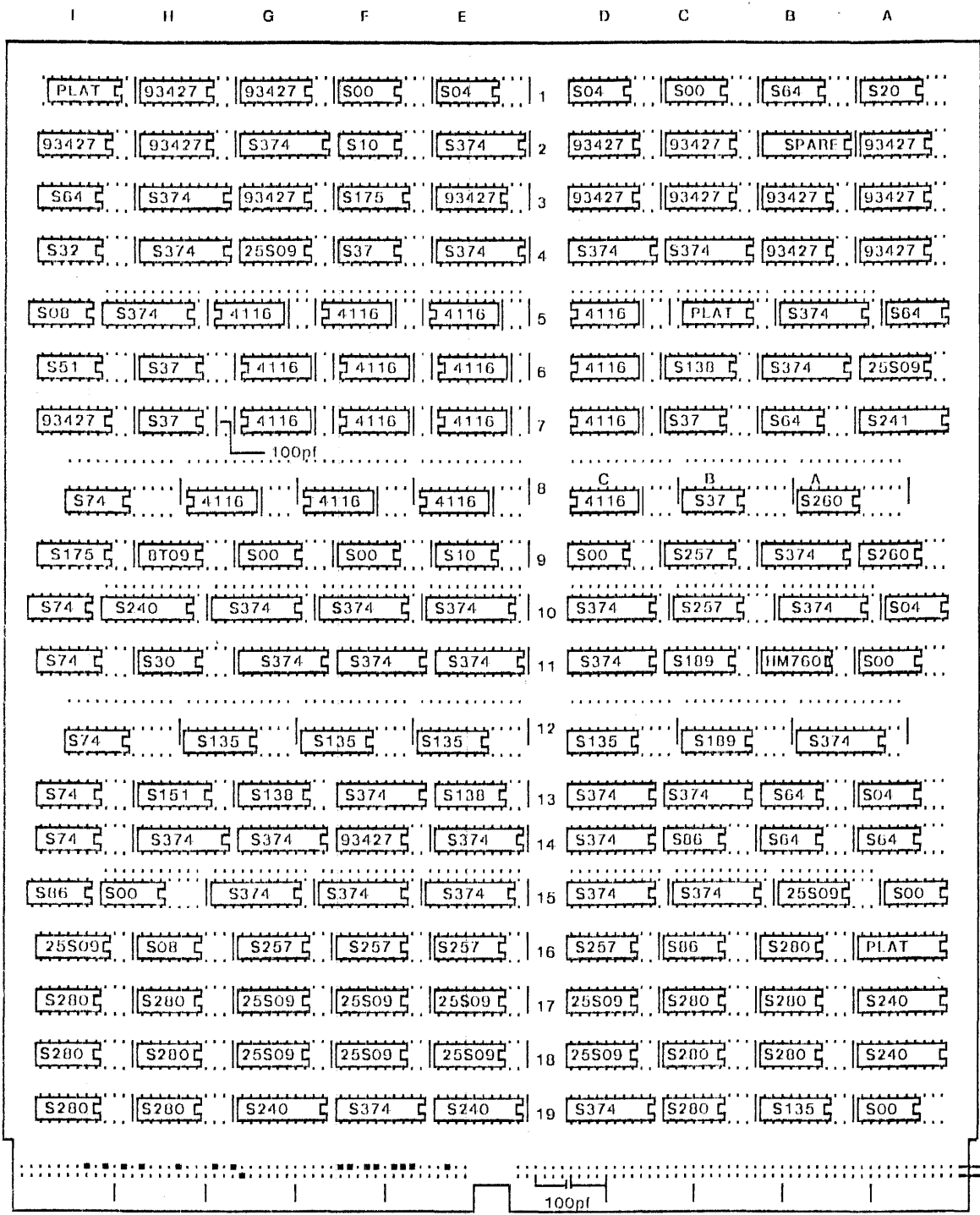


Position a16



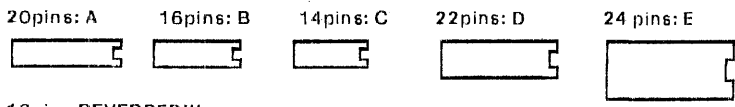
Position i1

XEROX F0D	Project D0	Memory Control PLATFORMS	File DOMemPLATFORMS.sil	Designer Thacker	Rev Gb	Date 7/18/80
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101-200  
1-100

Note: Pinx marked with ■ have 470ohm pullup resistors to +5v.



Note: The short vertical lines indicate filter capacitor locations.

(143 Places)

16 pins REVERSED!!!  
typical of MK4116: F



Changes from Rev E to Rev F:

- 1) Added the signal Disableh2 (pg 20,12) for test
- 2) Removed H4ParityError' from the term that forms Abort' (gate at a15 now free, inverter at e1a moved).

Note: This change deletes IC a15.

Changes from RevF to RevG:

- 1) h11.15 (pg 1) ← GenX, not GenX' (this was wrong in .nl file, ok on dwg.)
- 2) h13.9 ← CrctSyn4, h13.11 ← CrctSyn6 (pg. 3)

Changes from RevG to RevH:

- 1) (pg13) Change c1.13 from RamClock to EdgeClocka
- 2) (pg 13,15) Changed i9 from S74 to S175. Relocated i9's functions to i10. Added MOBounds as R.05 during R+Pipe operation.
- 3) (pg 16) Deleted S04 at a10e. Replaced with S00 a15a, and added MC1StartMC2' as input to MC1Active.
- 4) Added MC2PS12' by replacing i3 (S74) with S175 (pg 19). MC1PS12' is used instead of PStore12' at a1.13 (pg 20).

Changes from RevH to RevI (5/9/78)

- 1) (pg 20) h3.9 was MC2HoldIfSNE0, is now MC2StartXport' after passing through the BT09 at h9b (used as a driver).
- 2) Renamed signal MC2TestSNE0 to MC2HoldIfSNE0 (essentially, these two signals have been coalesced into one).
- 3) Added test points.
- 4) Added comments on Vee bypass and -10V supply changes to D0memplatforms.sil

Changes from Rev I to Rev J (8/12/78 - C. Thacker)

- 1) Renamed signal TP055 GateALUParity, and connected it to E079 (pg 10)
- 2) Latched signal StorAccessType in S374 at h4f (pg 15)
- 3) Removed MC2XferWord and MC1XferWord from a5.11 and a5.12. Connected a5.11 and a5.12 to a5.13 (pg 16). Note that signal MC1XferWord is no longer used on this card, so E006 is free.
- 4) Removed -10V supply components on D0memplatforms.sil

Changes from Rev J to rev K (10/8/78 - C. Thacker)

- 1) Changed h7.12 from MC1WriteMem to MC1WriteMemSlow (pg13). This signal is generated at platform a16 (pg12).
- 2) Changed platform a16 to 20pins to make room for MC1WriteMemSlow (pg12).
- 3) Added capacitors on SloMapRAS' and SloMapWrite' (platform c5, page 12).
- 4) Changed a9.12 from MC1Task.3 to MC1NxtL4 (pg15).
- 5) Changed i7.1 from PUb to Referenced (pg15). This requires changing PROM i7 to revision E.

Changes from Rev K to rev L (11/1/78 - C. Thacker)

- 1) Signal clkOutputReg is now clkOutputReg' by removing S37 at h6a (now free) page 13.
- 2) h10.1 (pg15) was Disableb10, is now GND. Also removed Disableb10 from SPLAT i1 (pg 12).

There are no prom changes in this revision.

Changes from Rev L to rev M (12/9/78 - C. Thacker)

- 1) Changed platforms c5 and i1 - removed capacitors and changed values.
- 2) Changed the generation of clkOutputReg' (pg 13). This signal is now one cycle wide, rather than being a qualified EdgeClock.
- 3) The input to h5g (pg 13) is PreRowAd', not EnRowAd'. This board requires an ALU board of rev M for proper operation.

There are no prom changes in this revision.

Note: Rev M = Rev Ga

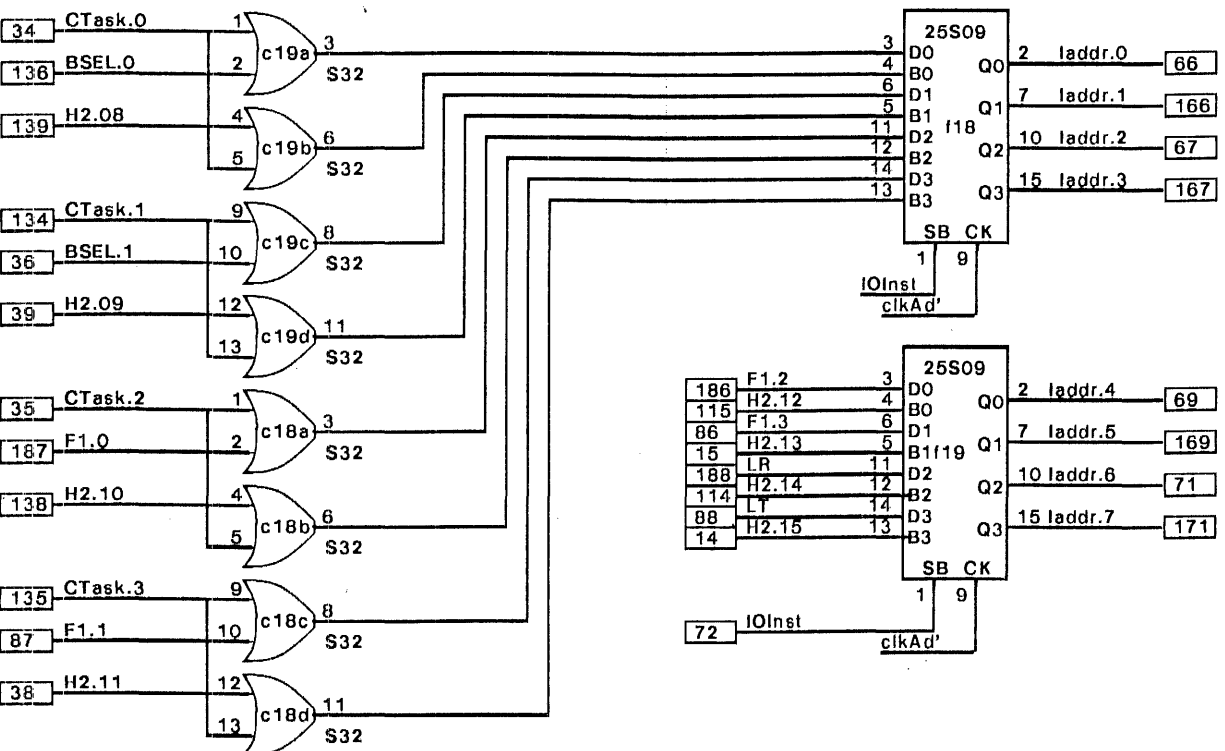
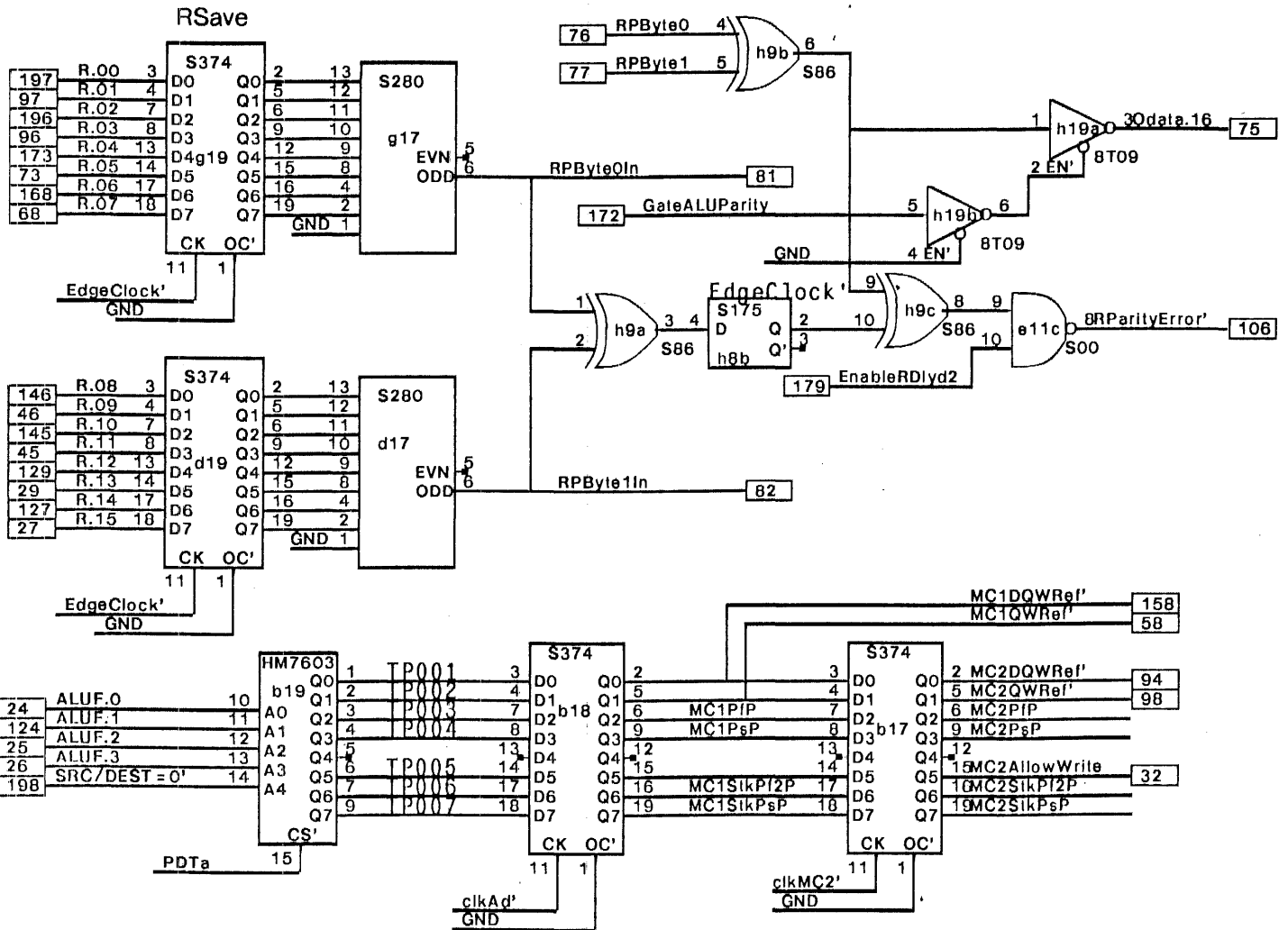
Changes from rev Ga to rev Gb (7/18/80 - CPT).

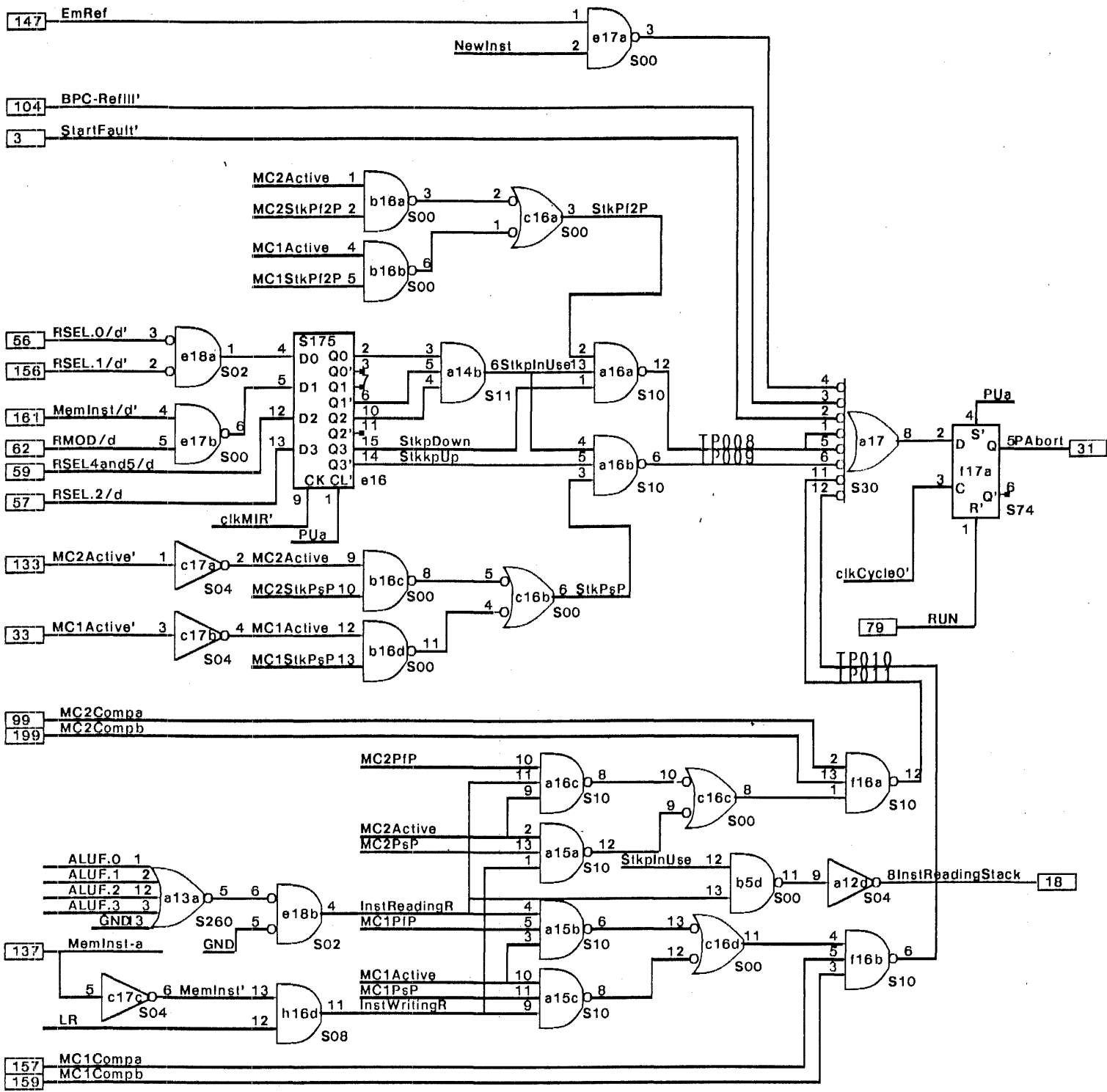
- 1) Added 16 FICAPS for MK4116 chips (VDD and VEE)
- 2) Added glitch suppression capacitor adjacent to h7 (on MC1WriteMemSlow - 100pf).
- 3) Changed interlock logic on page 18.

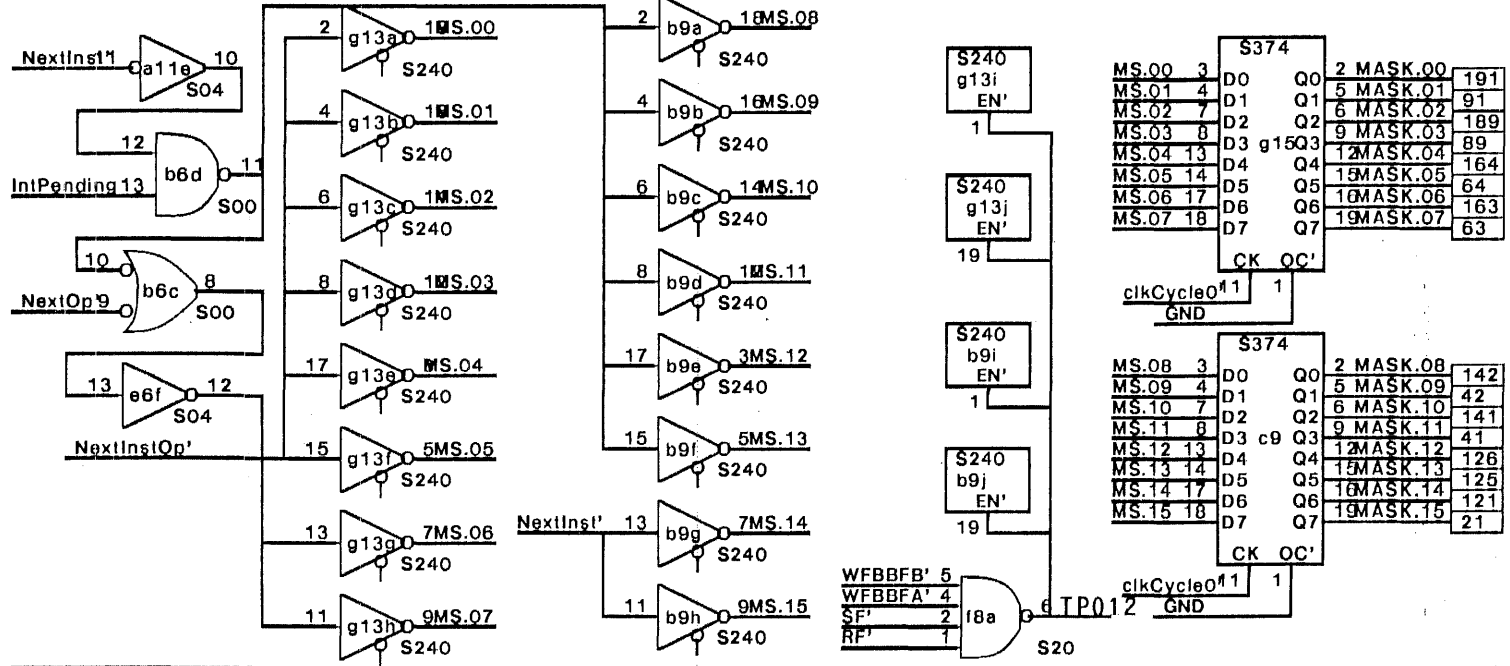
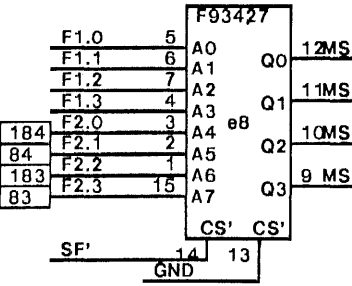
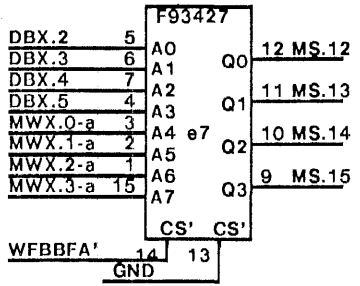
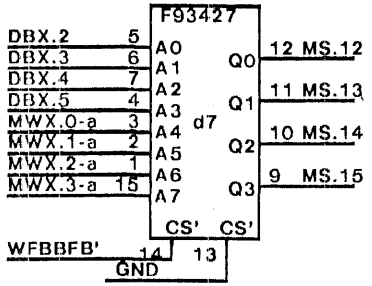
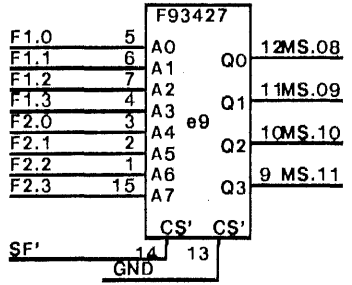
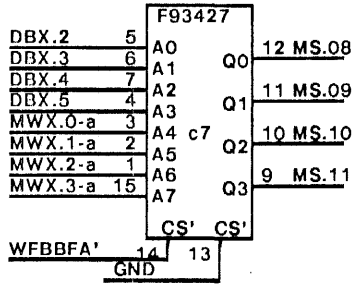
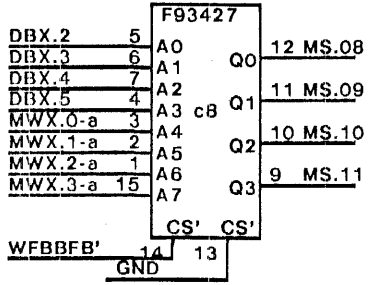
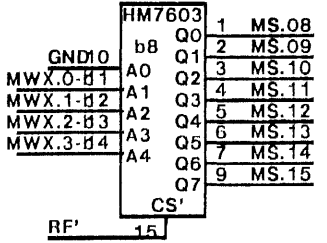
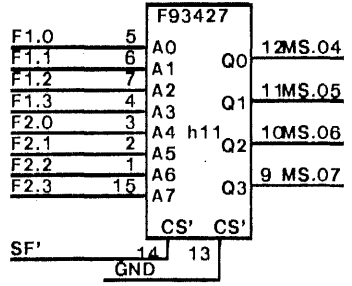
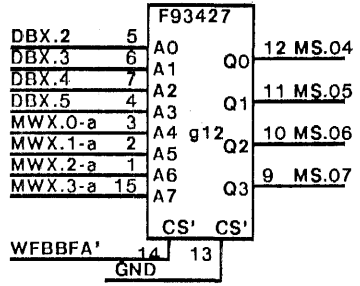
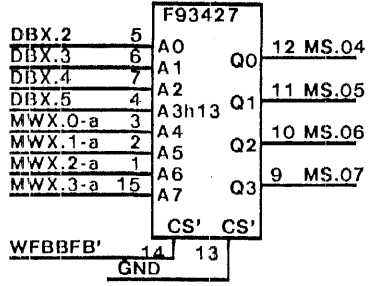
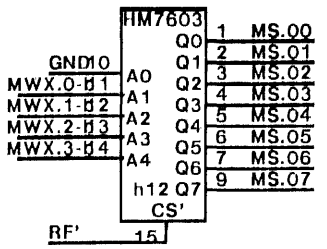
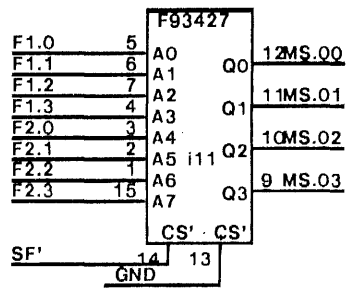
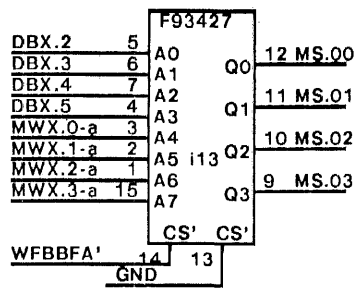
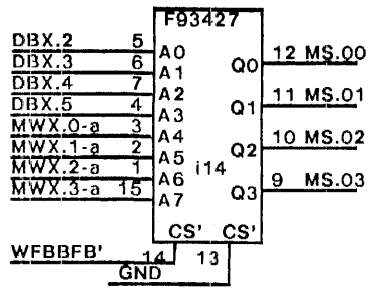
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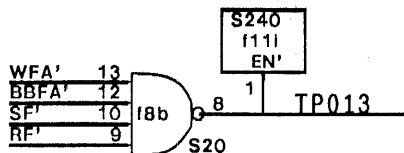
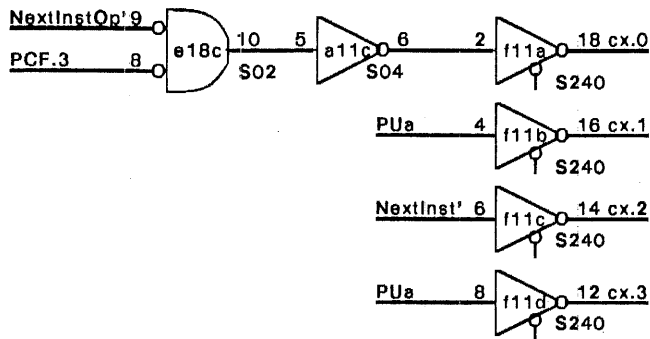
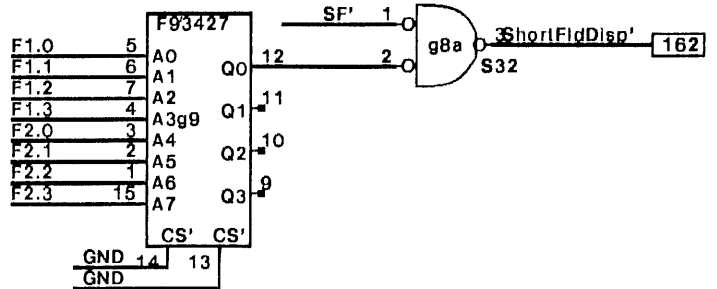
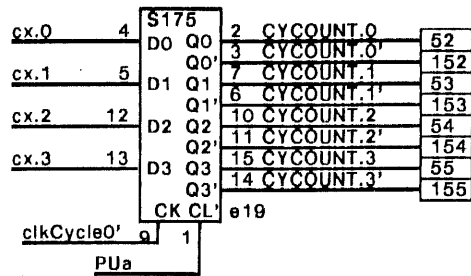
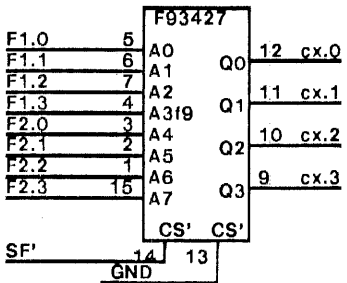
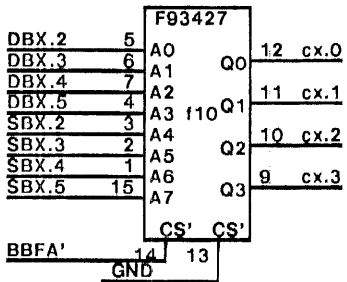
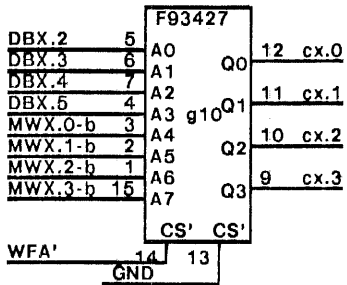
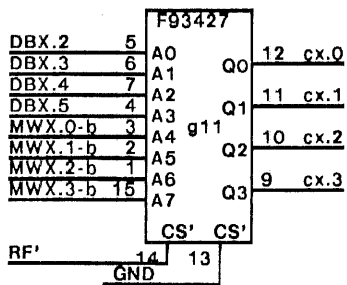
- a4, a3, a2, b3, b4, c2, c3, d2, d3, e3 (MC1 Sequencer): E
- g3, g1, h1, h2, i2 (MC2 Sequencer): D
- i7 (Fault): E
- b11 (Ftype, Pipe): D
- f14 (Single/Double errors)D

XEROX	Project	Memory Control Changes	File	Designer	Rev	Date
EOD	DO		d0memchanges.sil	Thacker	Gb	7/18/80

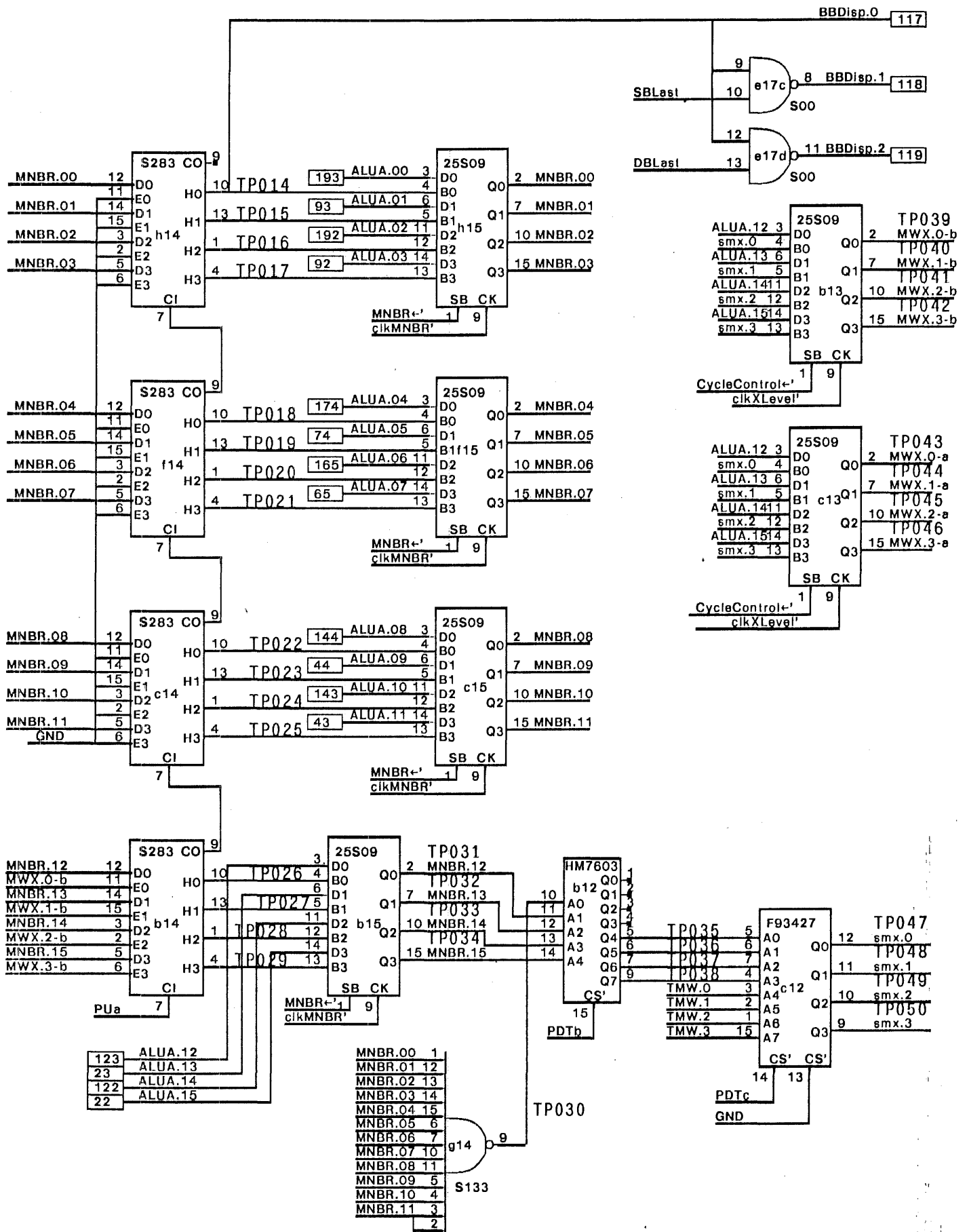


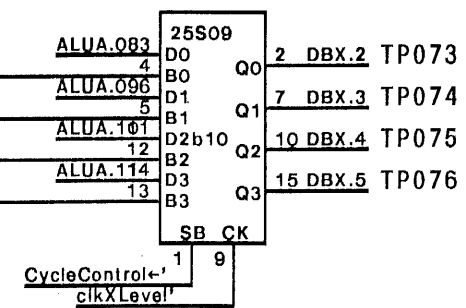
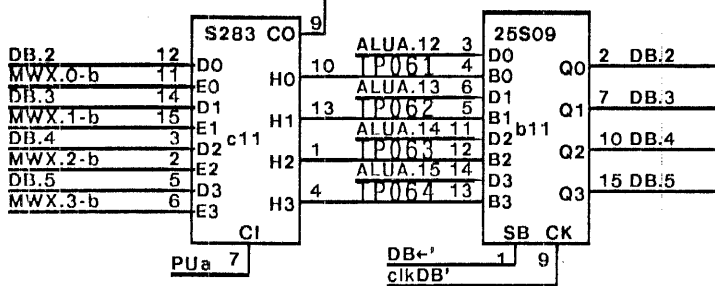
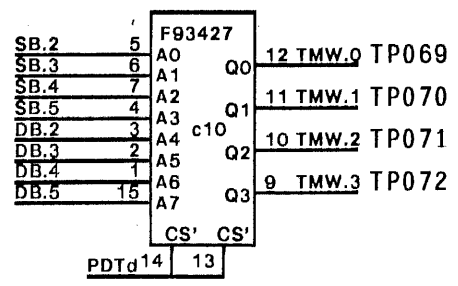
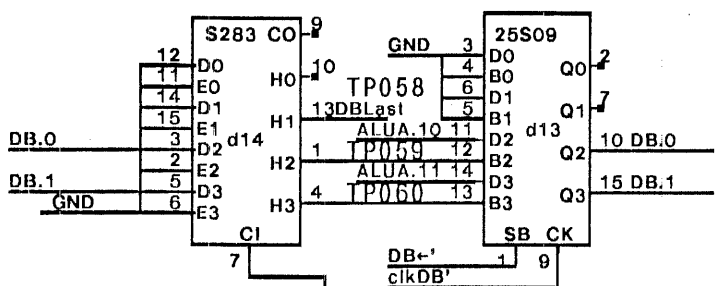
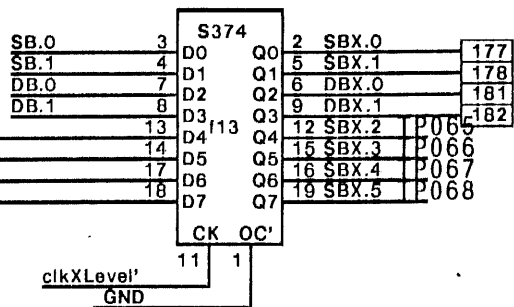
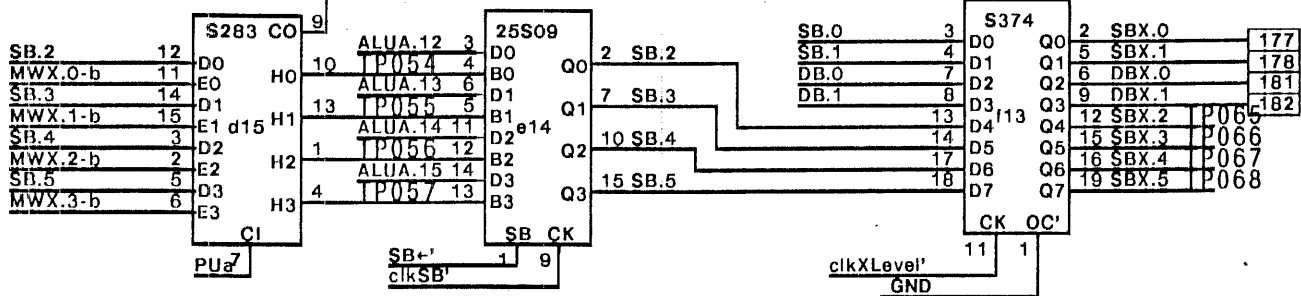
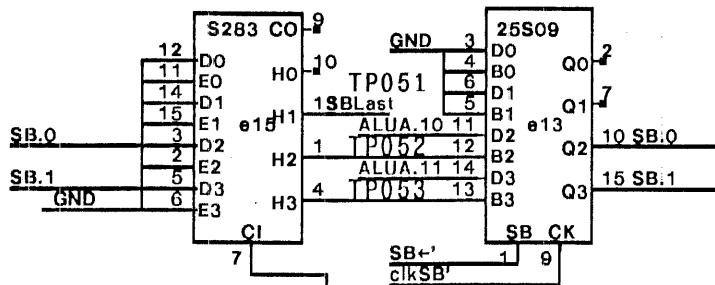


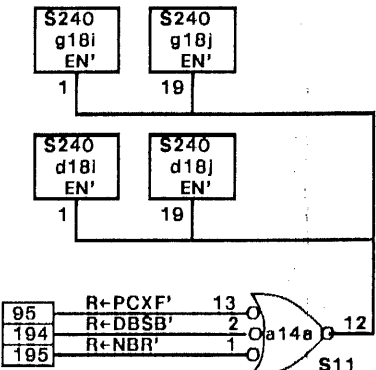
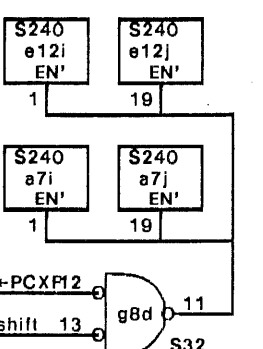
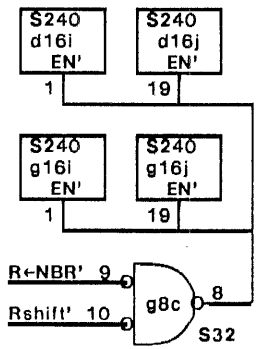
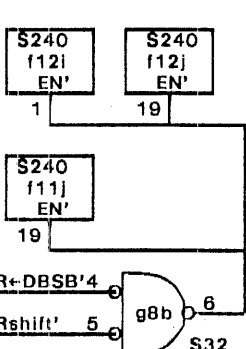
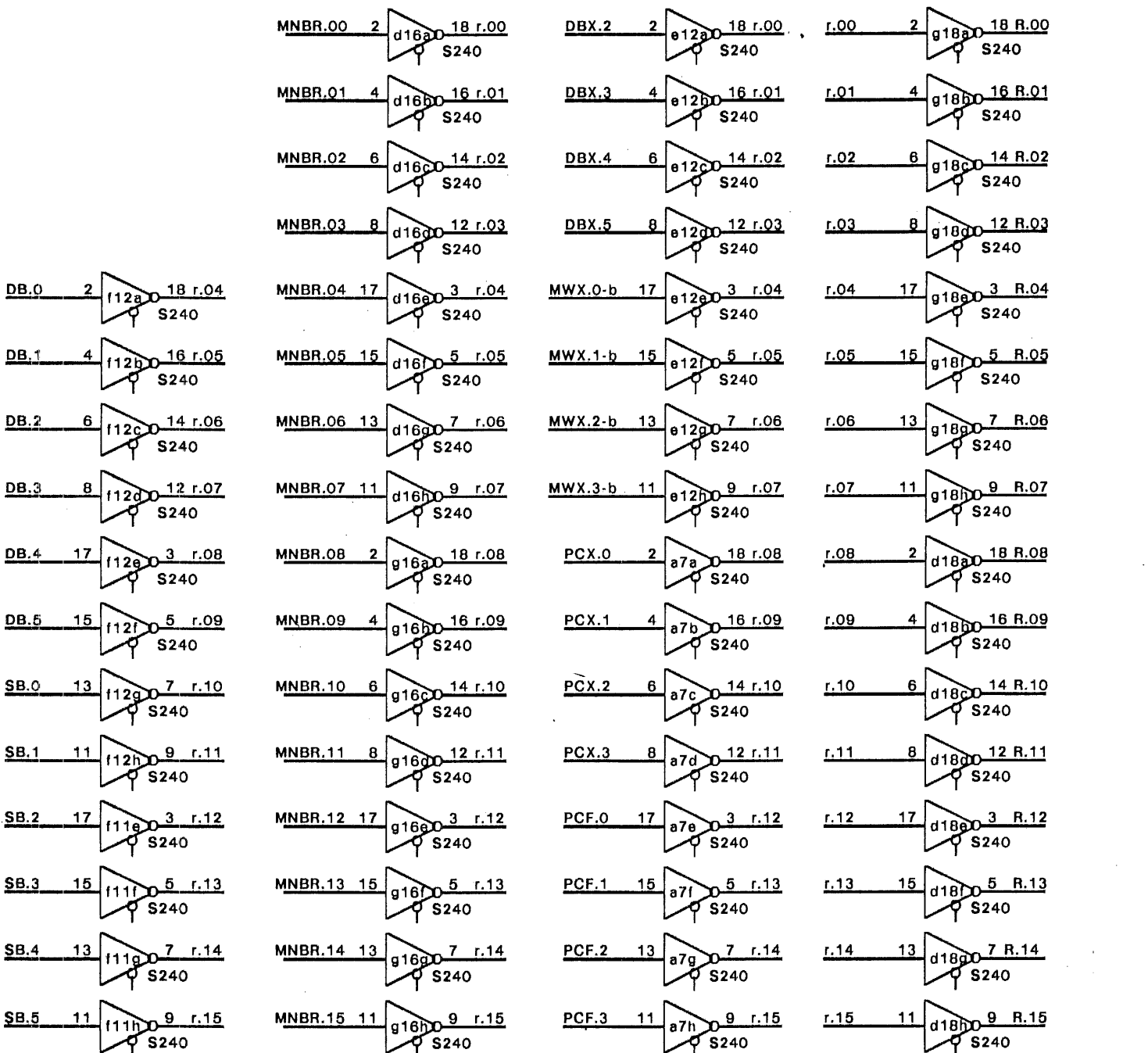


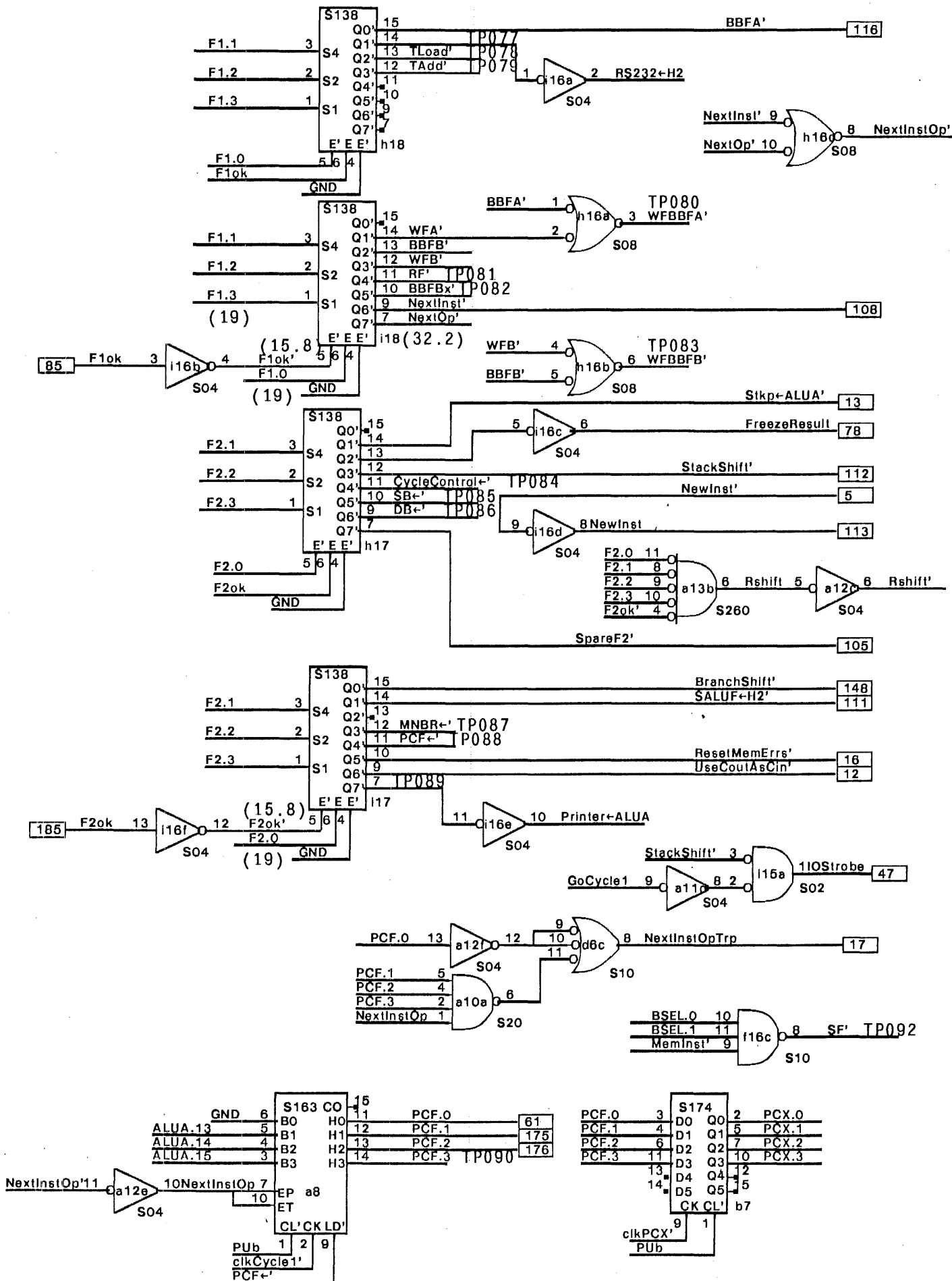


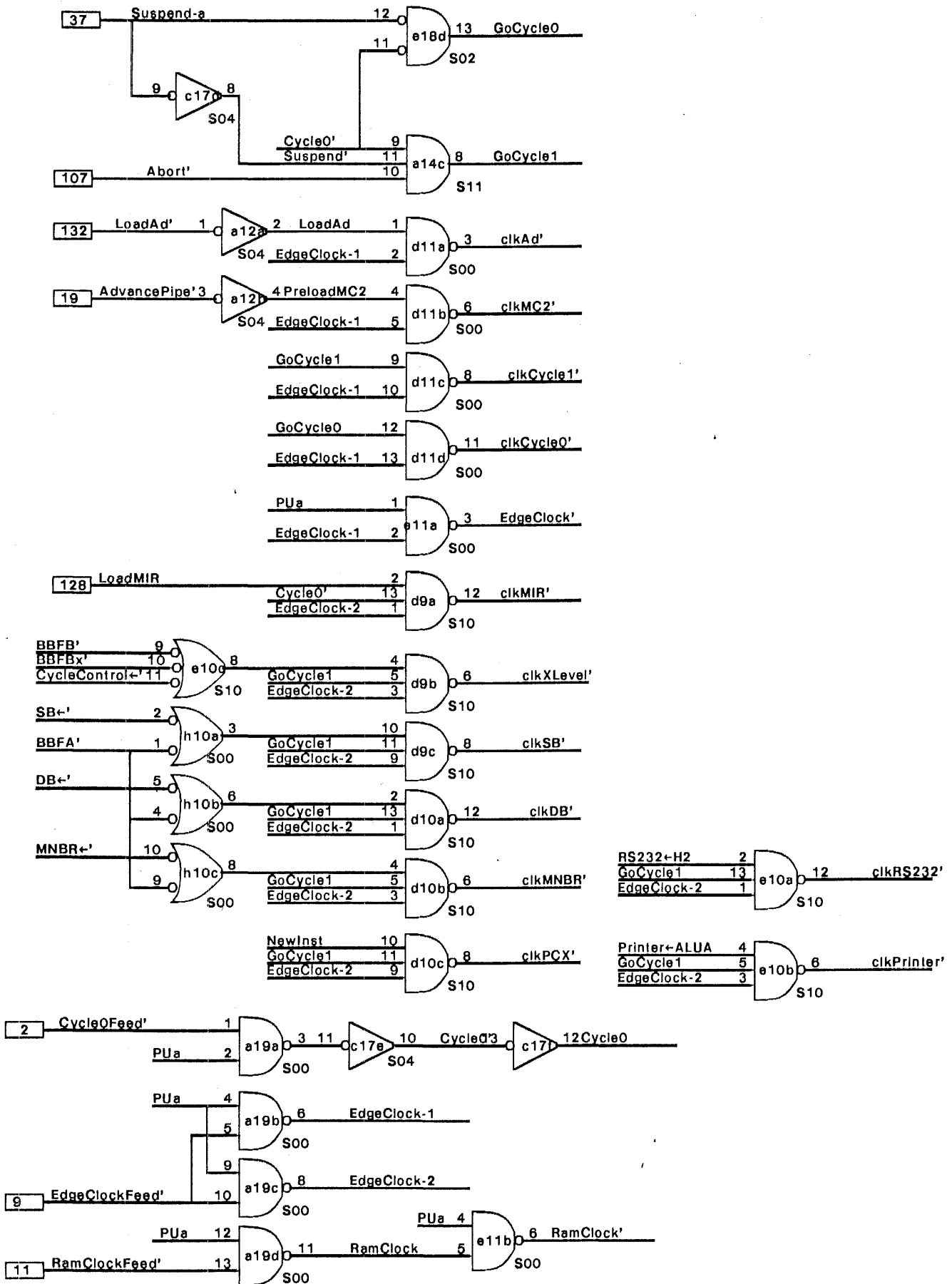


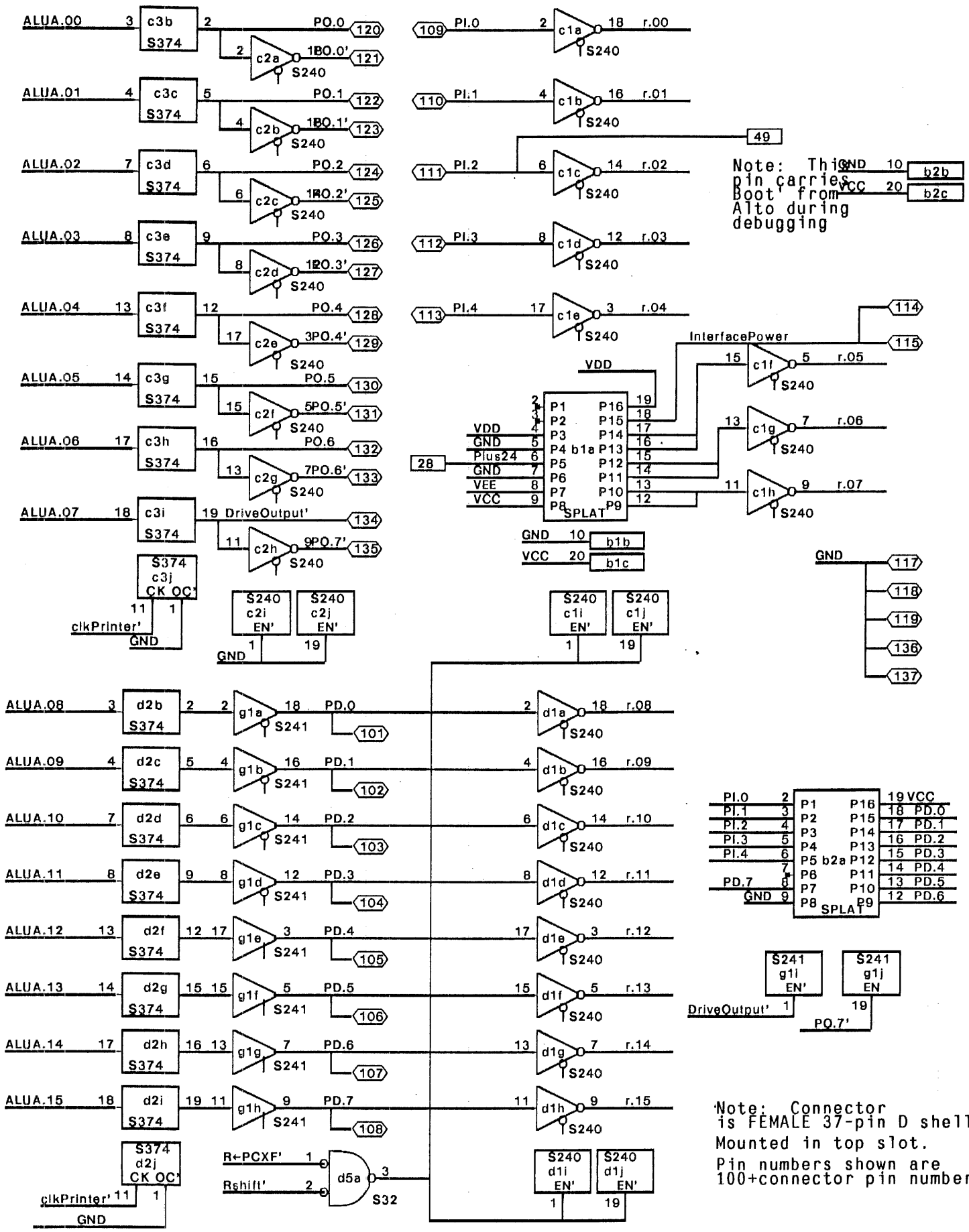


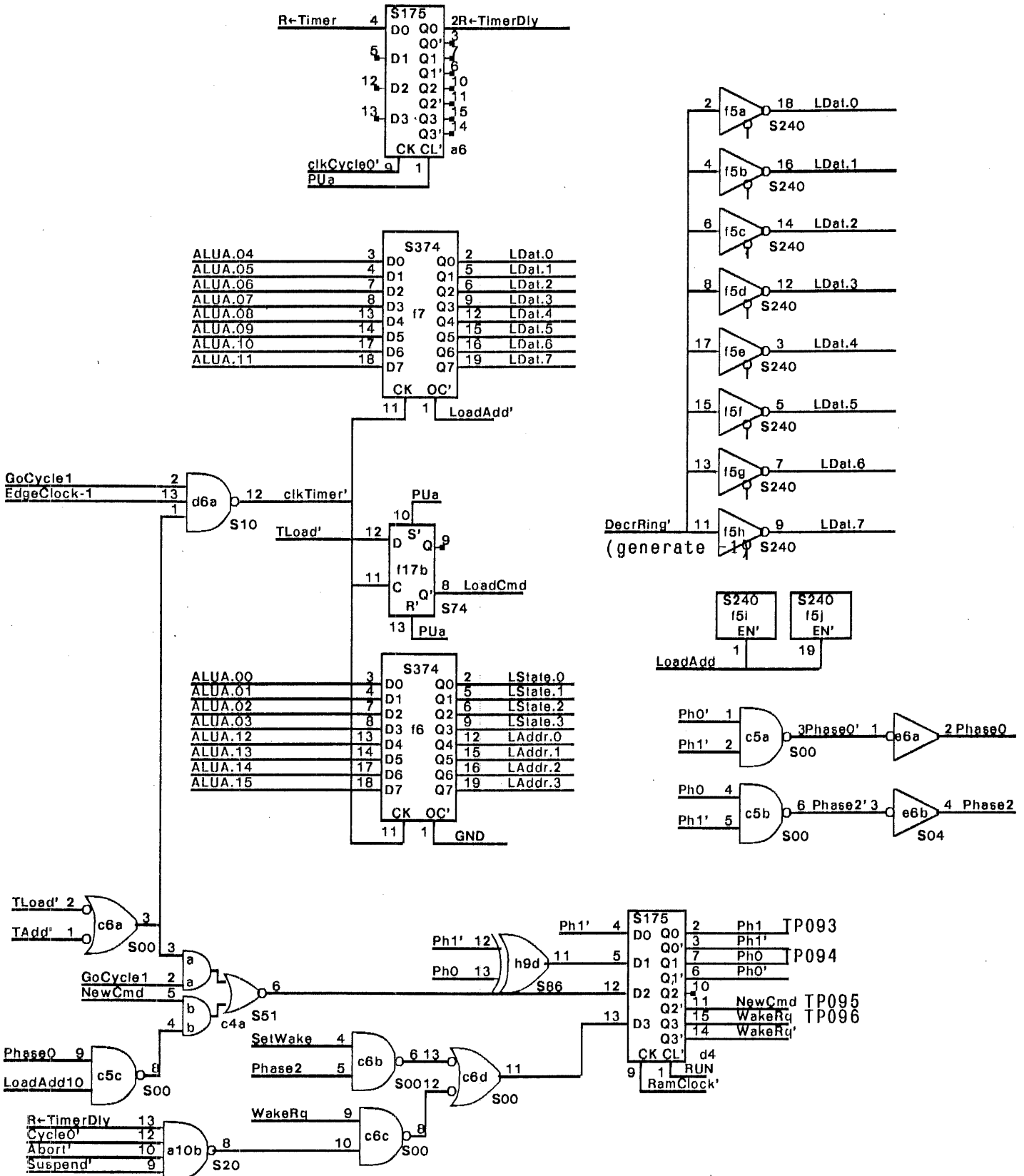




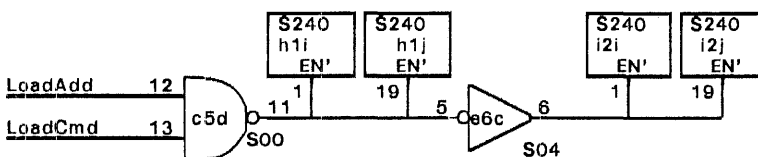
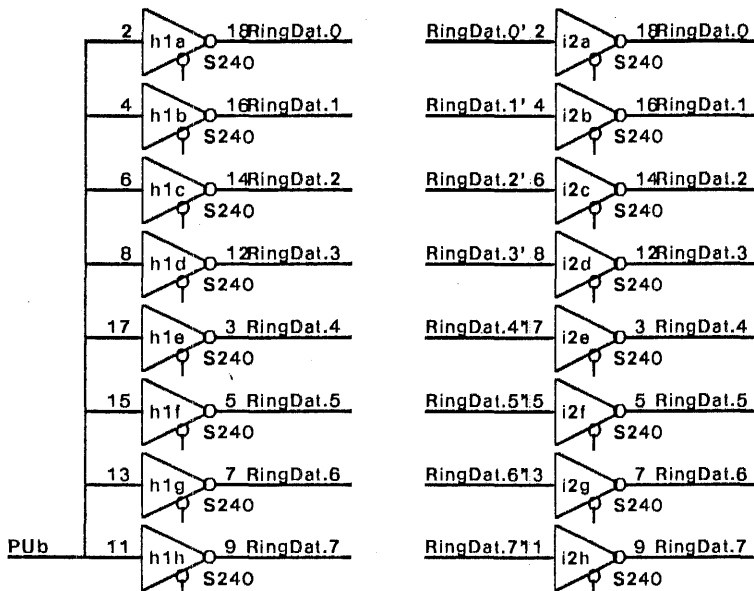
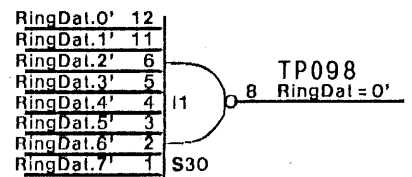
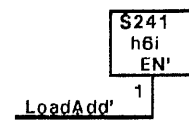
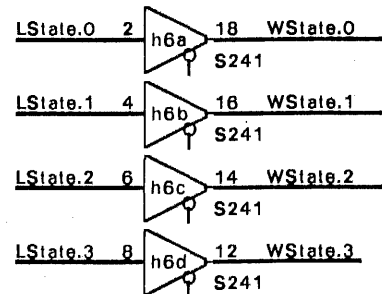
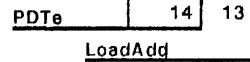
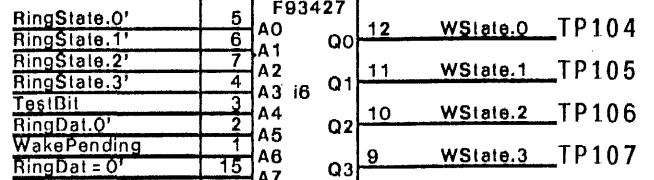
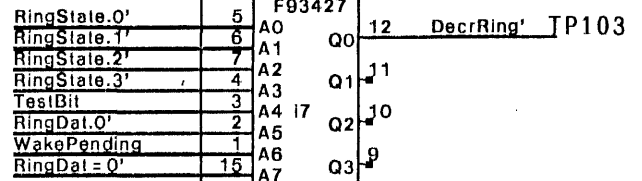
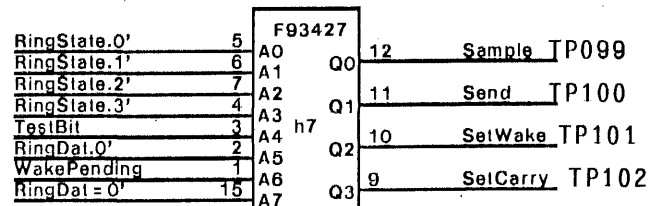
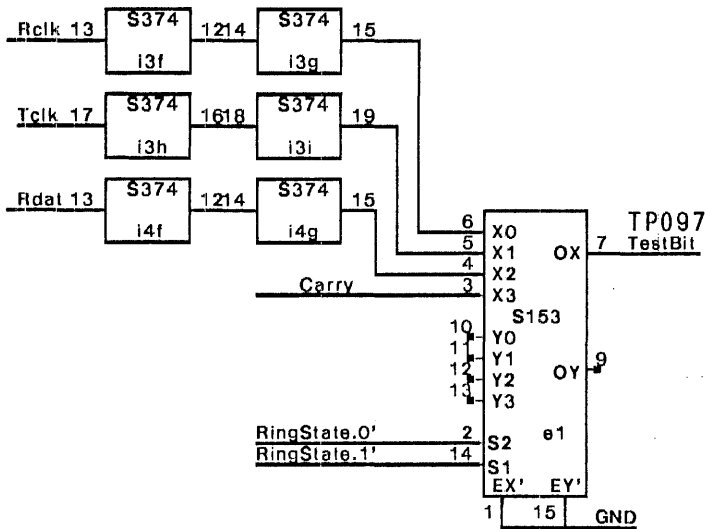




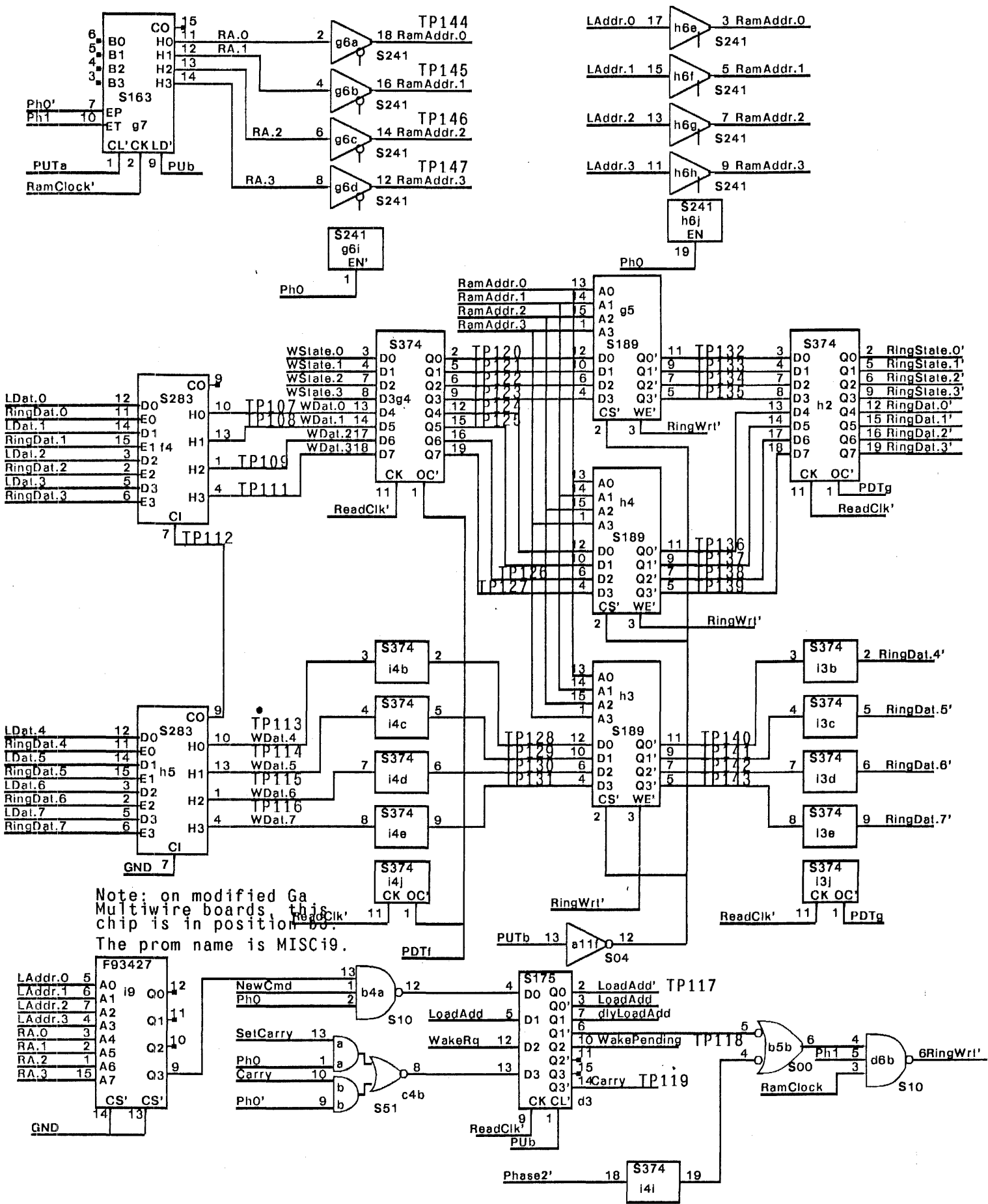




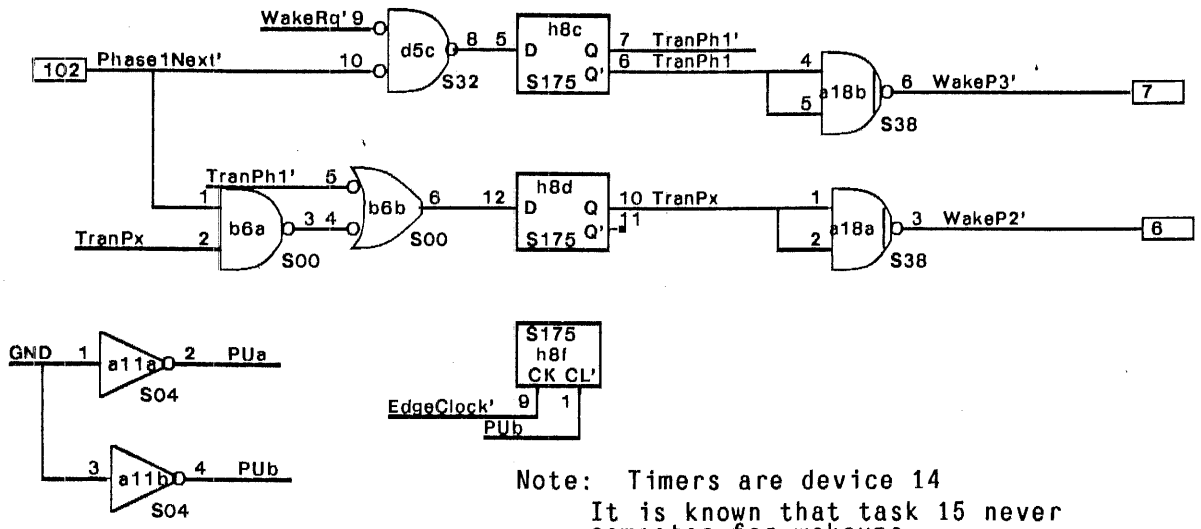
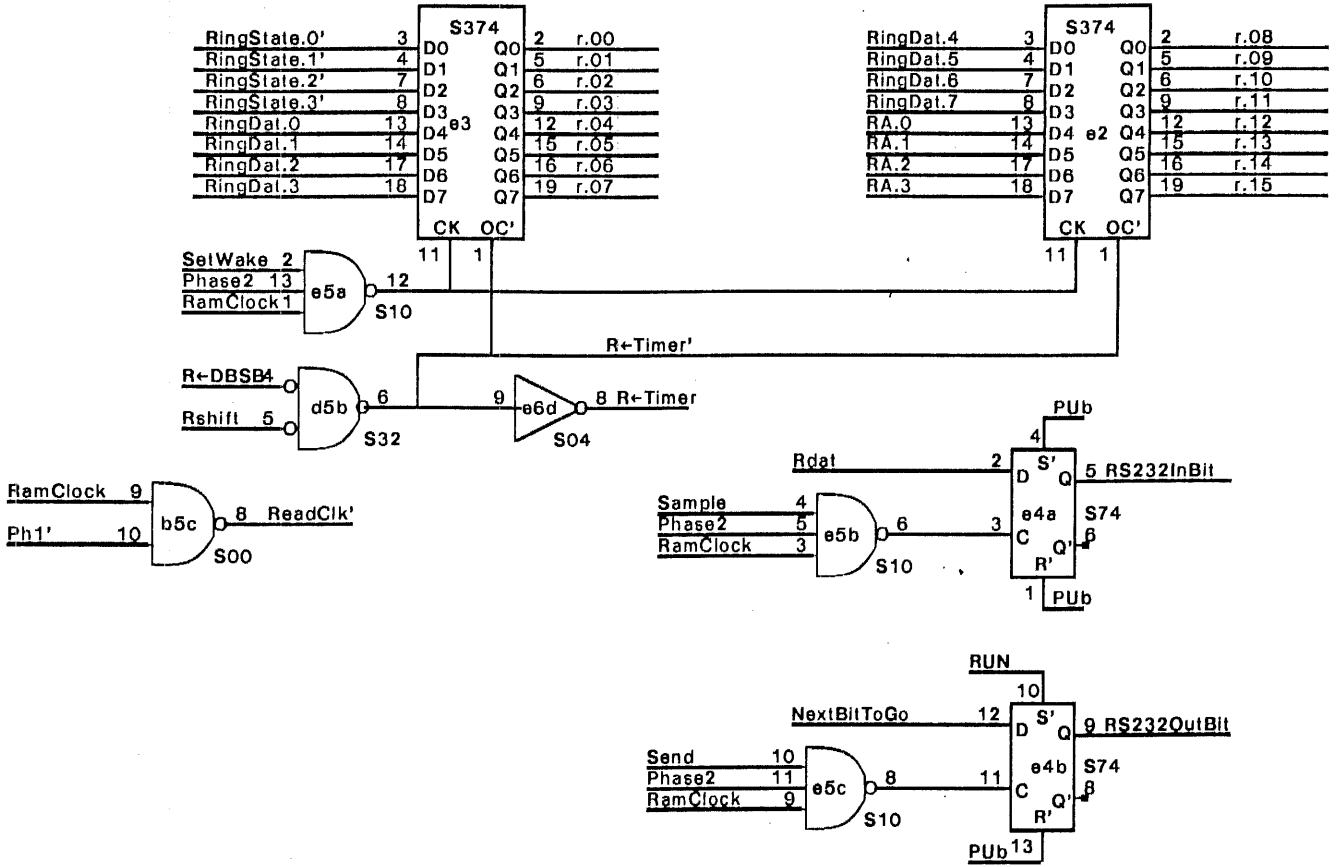
Possible that branch during R←Timer must be disallowed due to BranchBurp



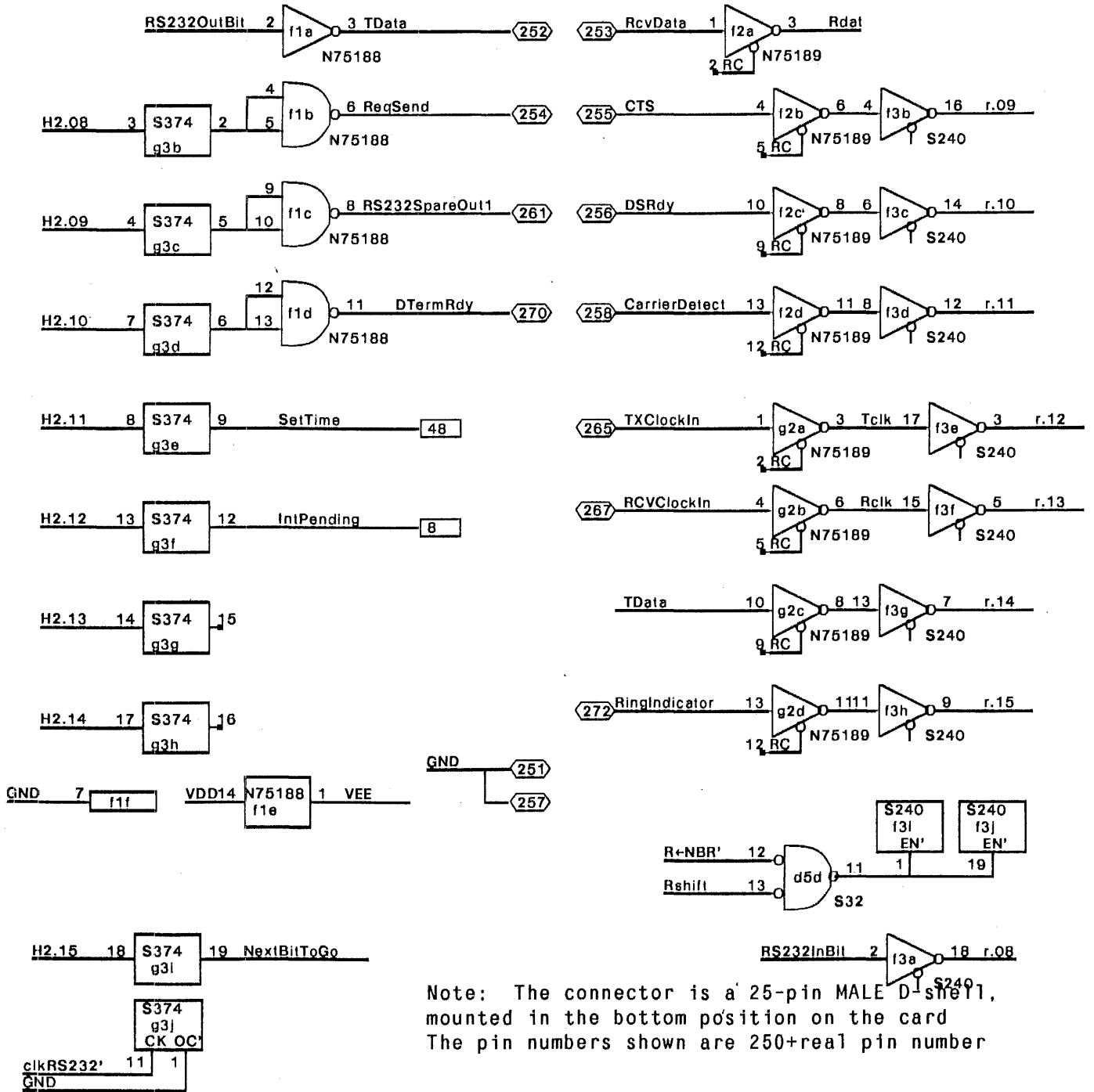




Note: on modified Ga  
Multiwire boards, this  
chip is in position 09.  
The prom name is MISCi9.



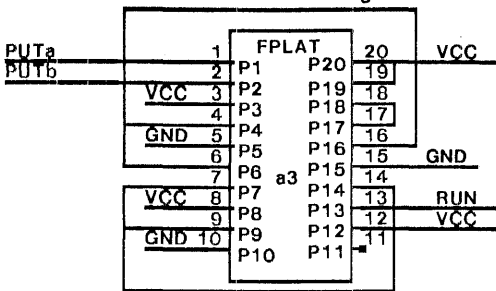
Note: Timers are device 14  
 It is known that task 15 never competes for wakeups.



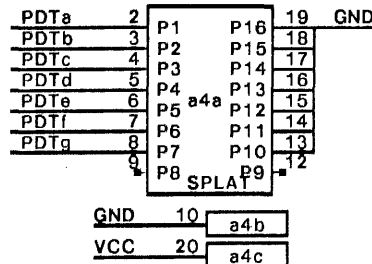
Note: The connector is a 25-pin MALE D-shell, mounted in the bottom position on the card. The pin numbers shown are 250+real pin number.

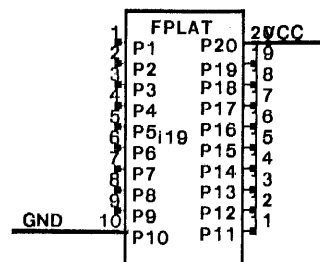
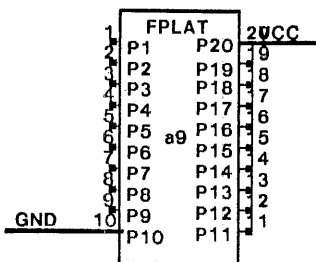
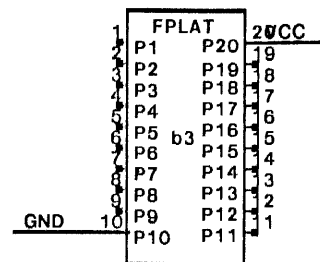
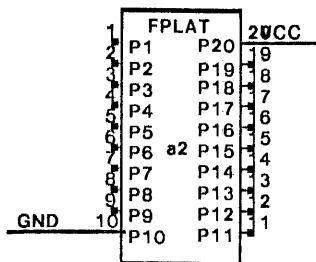
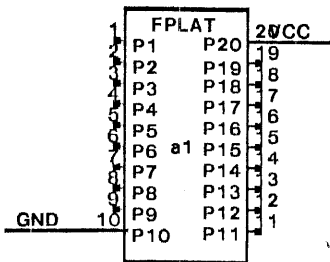
Note for PC Layout: PUTx and PDTx all have independent test

RUN voltage sensor



Test pulldowns (330ohms)





- 1) Added signal GateALUParity and inverter to receive it (Pg 1).
- 2) Deleted signal MC2EnableRP' (Pg 1).

**Changes for rev F to rev G (10/17/78 - C. Thacker)**

- 1) Reduced number of outbound RS232 lines to 4. Looped RS232 data back on R.14. Added SetTime as bit 11 in the output register (goes to E48). Added IntPending as bit 10 of the register. All changes on pg 15.
- 2) Terminated PI.0 - PI.4. Used R bus drivers PI.5-7 for voltage monitors.
- 3) Added a11e, b6d, b6c, e6f on pg 3 to cause IntPending to dispatch to Opcode0 on interrupt.
- 4) Added test pullups and pulldowns.
- 5) Added +5 monitor at a3 (pg 15) to control RUN.

**Changes for rev G to rev H (1/4/79 - C. Thacker)**

- 1) Brought signal InstReadingR to E018 (pg 2).
- 2) h17 pin 7 was NewInst', is now SpareF2, connected to E105
- 3) NewInst' is now connected to E005 rather than to h17.7.  
Note: Control boards with revision <I must have E005 jumpered to E105 on the backplane.
- 4) Removed the time-to-task counter (a9) and freed inverter a12d (pg8).
- 5) Terminated PD.0-7 with splat (R-pack) at b2
- 6) Added InterfacePower signal (short-circuit protected +12V) to Printer Interface connector

**Changes for rev H to rev I (1/18/79 - C.T)**

- 1) Changed layout - g1 is S241, not 75188
- 2) Modified platforms b1, a3.
- 3) (pg 1) b17.1 is GND, not PDTf.
- 4) (pg 10) b1.9 is VCC, not GND
- 5) (pg 10) Added S241 driver for PD.0-PD.7. (note - early etch boards will NOT have this change)
- 6) (pg 12) i6.14 is PDTe, not LoadAdd
- 7) (pg 13) i4.1 is PDTf, not GND

**Changes for rev I to rev J (1/31/79 - CT)**

- 1) Changed E18 from InstReadingR to InstReadingStack (pg2). Corrects a bug in overflow checking

Note: Revision J = Revision Ga

**Changes for revision Ga to revision Gb (10/14/79 by CT). Fixes interval timer inaccuracy.**

Note: This change comes in two flavors: Revision Ga multiwire boards have 2 extra IC's mounted in spare positions b3 (93427) and b4 (74S10). In the Multiwire Gb version, the S10 is in position b4, but the 93427 replaces the S85 in position i9. The logic diagrams show the revision Gb multiwire version of the change. To modify a revision Ga multiwire board, proceed as follows:

In the steps below, pin numbers are those of the chips, not those of the 20 pin sockets used to hold the chips. Chip b4 is mounted with pin 7 in pin 10 of the 20 pin pattern, b3 is mounted with pin 8 in pin 10 of the 20 pin pattern.

All wiring is to be done on the back (non-component) side of the board.

- 1) Add an S10 in position b4 and wire b4.14 to pin 20 of the pattern (Vcc).
- 2) Add a 93427 (programmed) in position b3, and wire b3.16 to pin 20 of the pattern (Vcc).
- 3) Lift pins b5.1, b5.2, and b5.3.
- 4) Remove chip i9 and jumper i9.6 to i9.8
- 5) Add b5.1 to b4.1
- 6) add b5.2 to b4.2
- 7) add b5.3 to b4.12
- 8) add b3.14 to b3.13 to b3.8
- 9) add b3.5 to f6.12
- 10) add b3.6 to f6.15
- 11) add b3.7 to f6.16
- 12) add b3.4 to f6.19
- 13) add b3.3 to e2.13
- 14) add b3.2 to e2.14
- 15) add b3.1 to e2.17
- 16) add b3.15 to e2.18

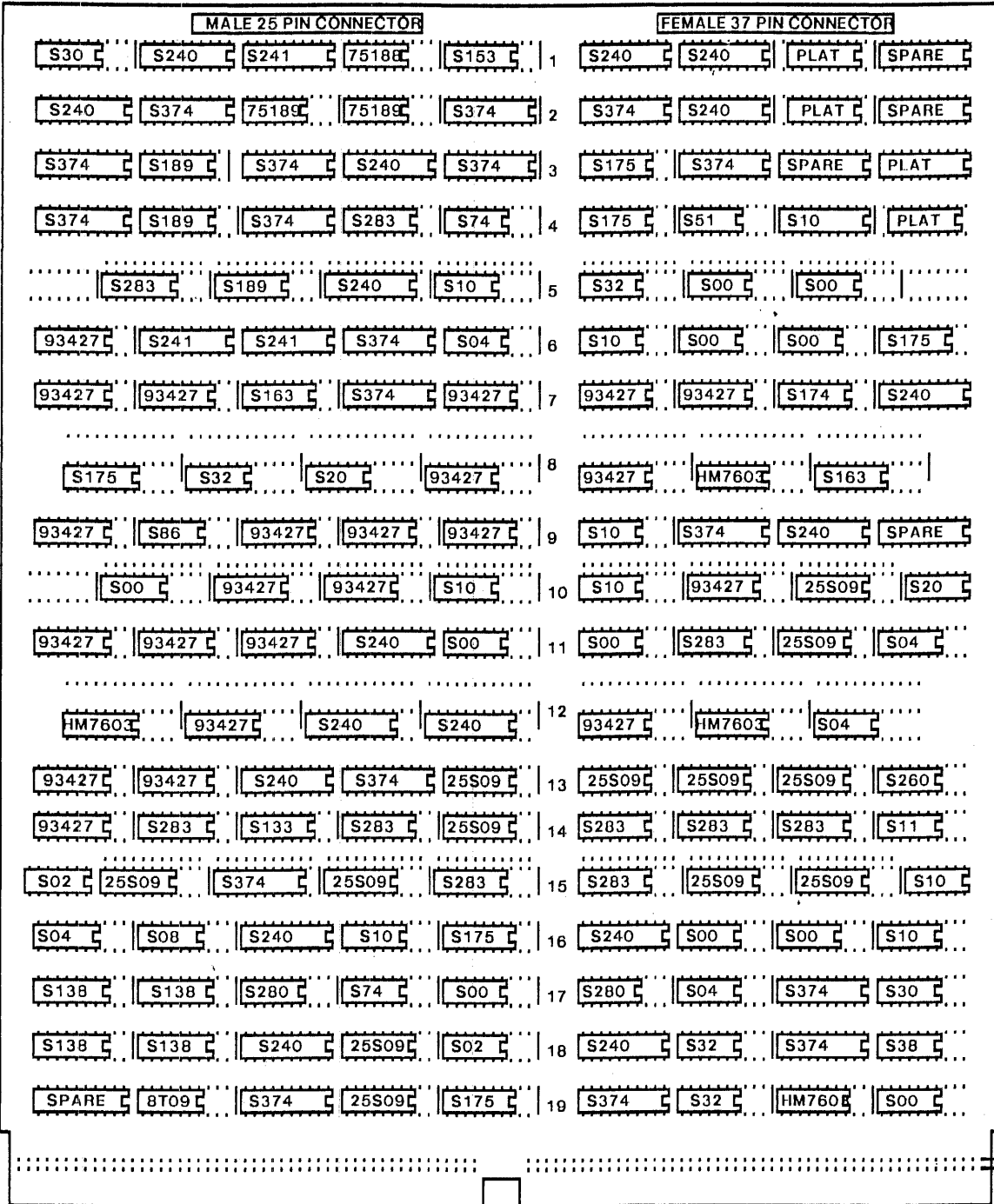
**Changes for revision Gb to Gc (7/17/80 - CPT)**

- 1) e18.5 + gnd (pg. 2) This causes memory reference instructions to interlock when referencing base registers

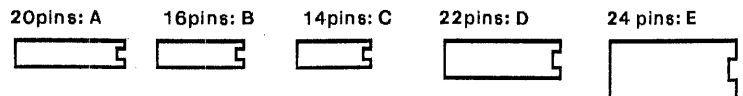
- 17) add b3.9 to b4.13

XEROX PARC/C.S.	Project DO	Title DO MISC board Changes	File DOMISCChanges.s^T	Designer	Rev Gc	Date 7/17/80
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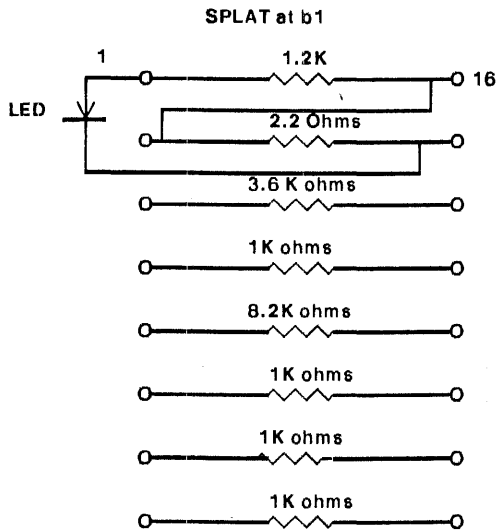
I H G F E D C B A



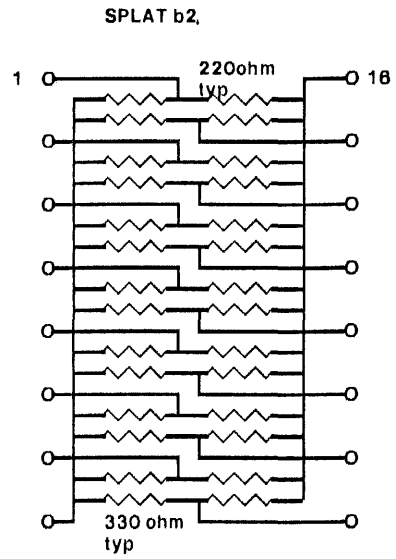
101-200  
1-100



Note: The short vertical lines indicate filter capacitor locations.

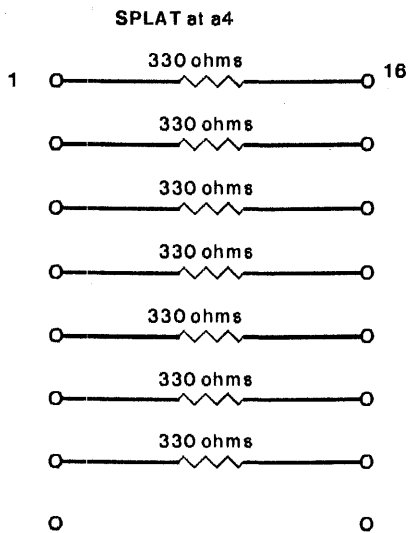


(Page 10)

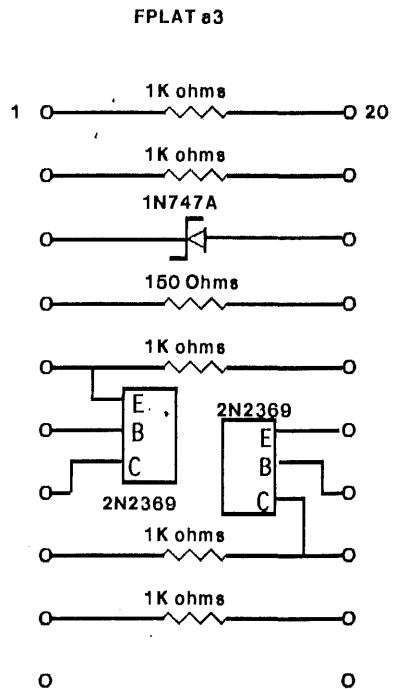


Beckman P/N 898-5-R220/330  
Xerox P/N (7) 703W30491

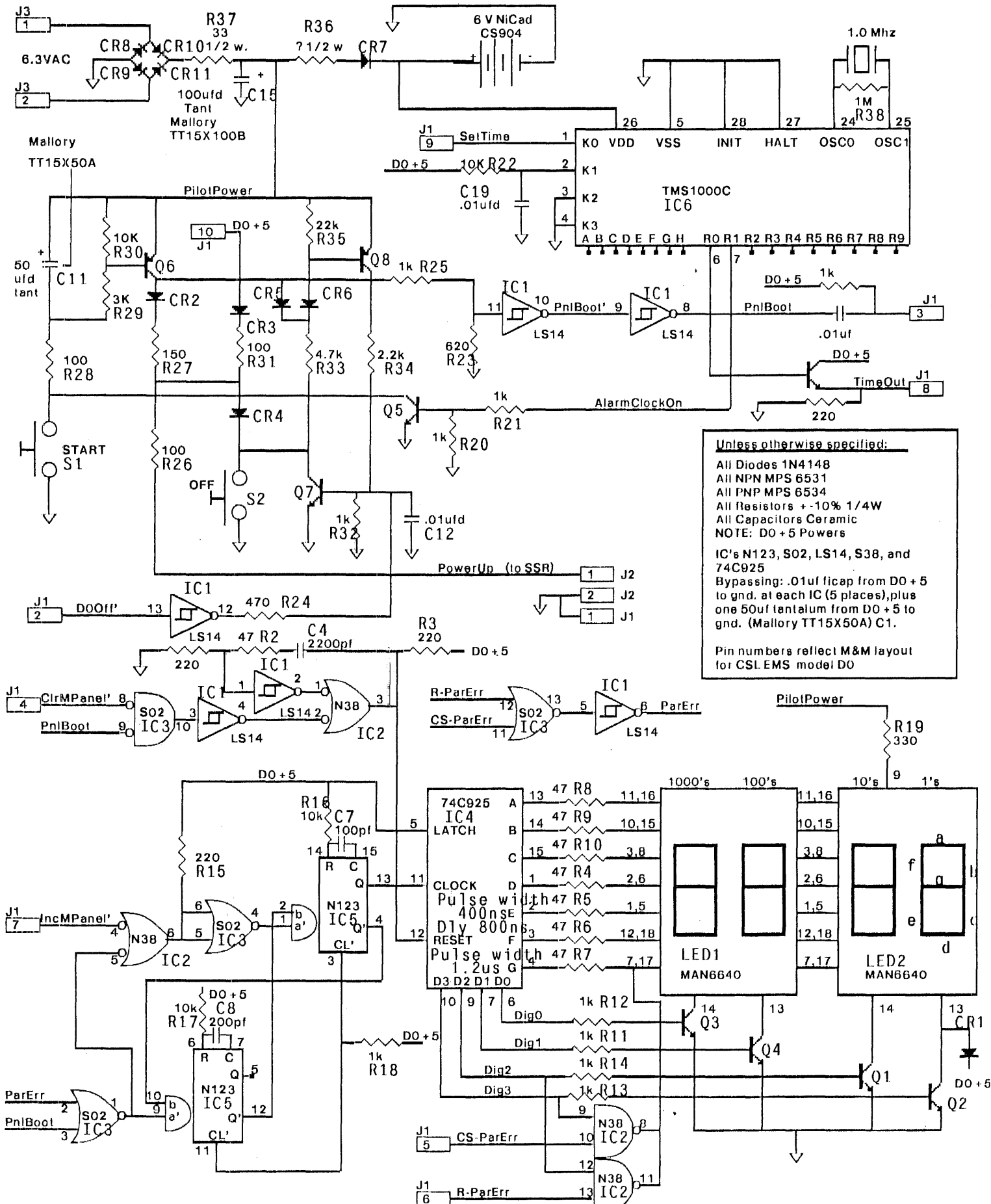
(Page 10)



(Page 15)

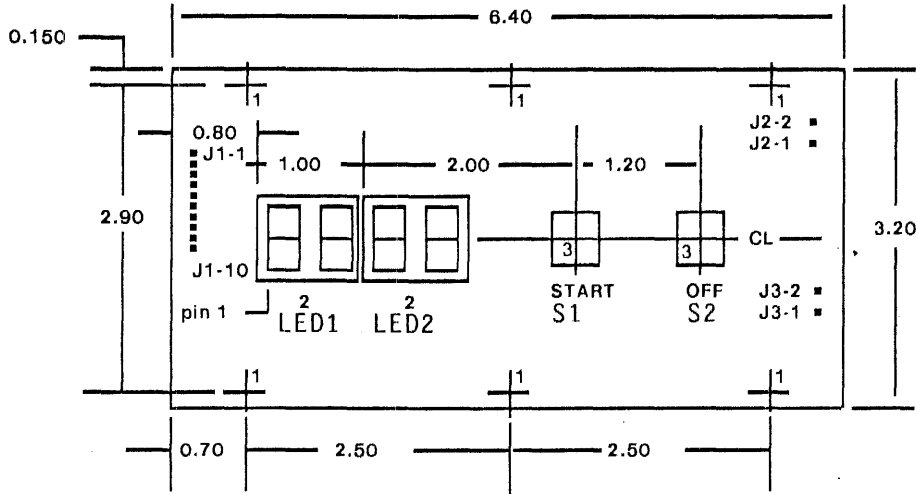
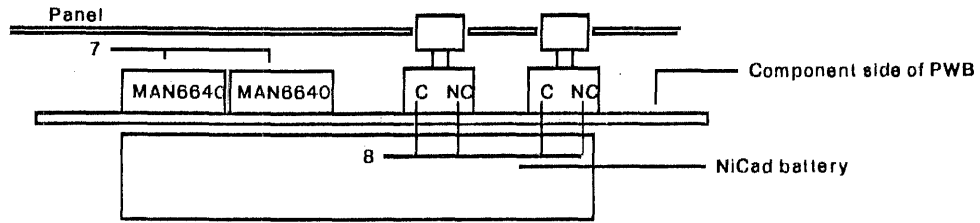


(Page 15)



XEROX E0D	Project D0	Maintainance Panel	File D0mp01.sil	Designer Rosen	Rev Gc	Date 6/11/79	Page 01
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**Notes:**

- 1) Mounting holes .188 dia, 6 places
- 2) 7-segment displays are Monsanto MAN6640. Package is 18 pins, 2 rows on .6 centers. Pin 1 is as shown.
- 3) START and OFF are C&K 8221 Momentary contact buttons with .465 square button.
- 4) J1, J2, and J3 in the schematic are not connectors, but are closely spaced groups of holes suitable for connecting discrete wires.
- 5) The TMS 1000C is a 28-pin DIP. Pin-to-pin spacing is .100, row to row spacing is .600.
- 6) The NiCad battery will be attached to the board with two cable clamps secured to the mounting screws.
- 7) Pin 1 of these LED's is the side containing the marking "MAN6640".
- 8) Note that switches must be oriented with "C" and "NC" as shown.

XEROX EOD	Project D0	Maintenance Panel	File DOMP02.sil	Designer Rosen	Rev Gb	Date 4/27/79	Page 02
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Originally released as rev Ga.

Changes for revision Ga to Gb (4-27-79 CT)

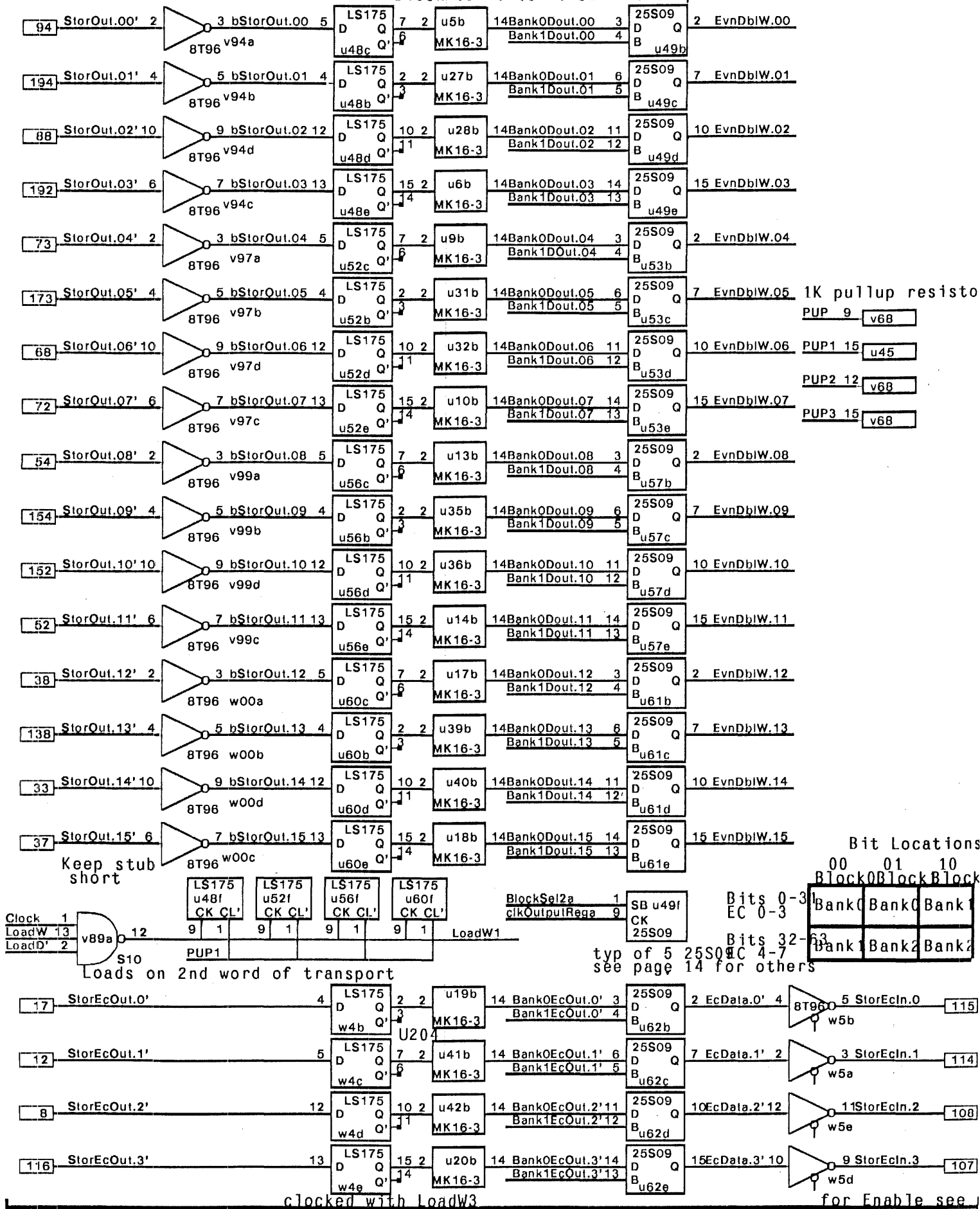
- 1) Changed IC2 from S38 to N38
- 2) Changed C8 from 100 pf to 200pf
- 3) Changed R2 from 470 ohms to 47 ohms (initial loading chart was incorrect).
- 4) Removed components C13, C14, and R39

Changes for revision Gb to Gc (6-11-79 CT)

- 1) Added .01uf cap and 1k resistor in series with PnlBoot. This is the line that boots the machine; this change causes the boot signal to be a negative-going pulse at the end of the ~700ms time delay that starts when the boot button is released.
- 2) Added NPN emitter follower to signal TimeOut to assist the feeble CMOS output of the TMS1000C.

XEROX E0D	Project D0	Maintainance Panel Changes	File D0MPchanges.sil	Designer Rosen	Rev Gc	Date 6/11/79	Page 01
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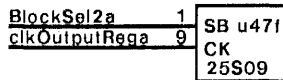
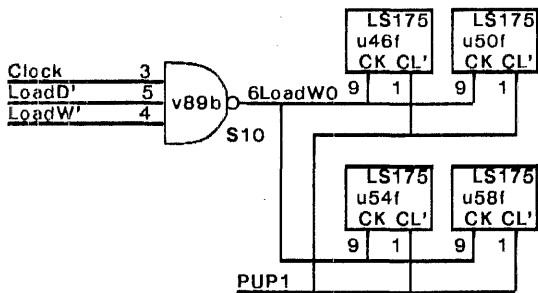
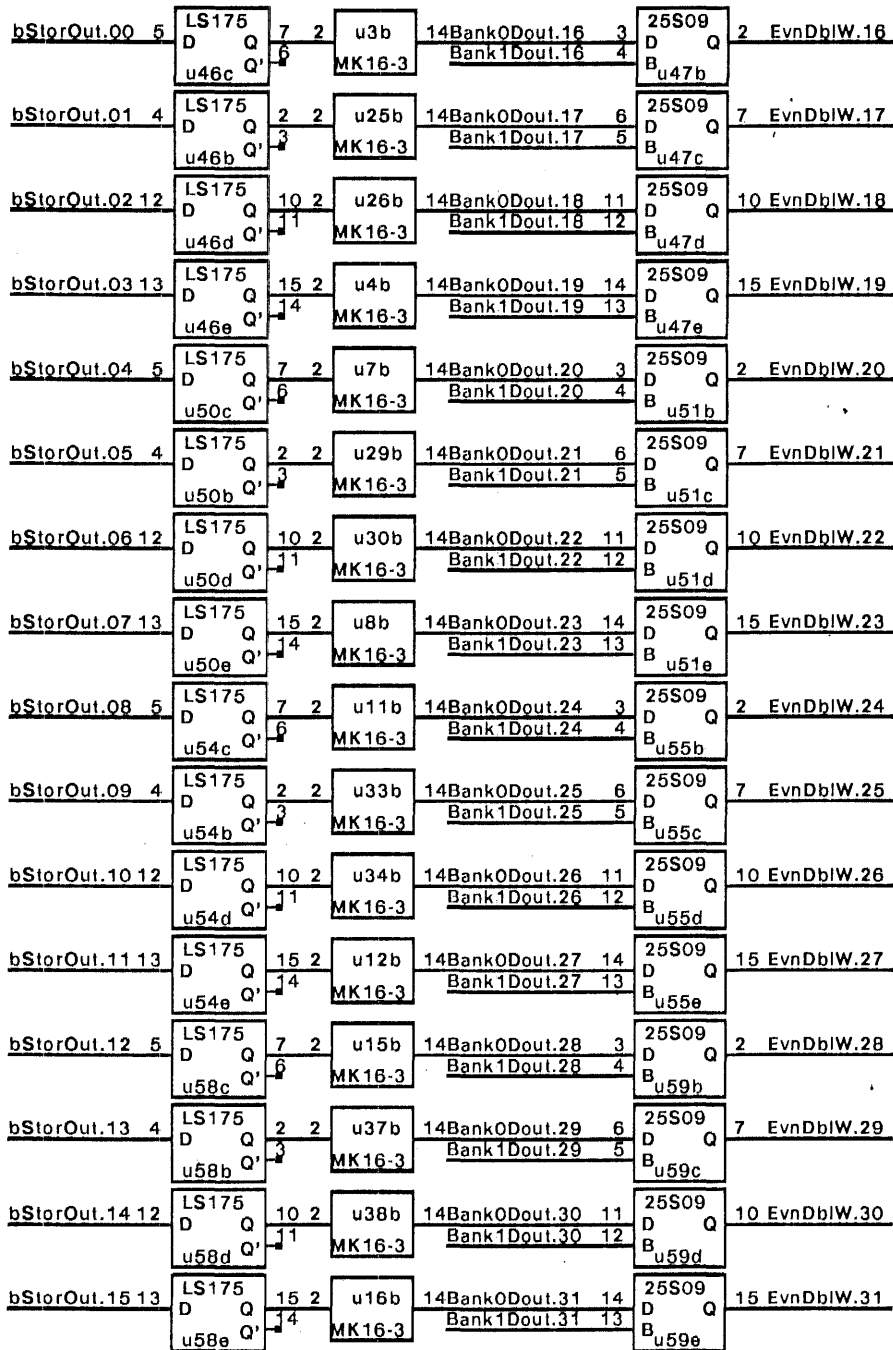
Block 0&1 bits 16-31 5 chips



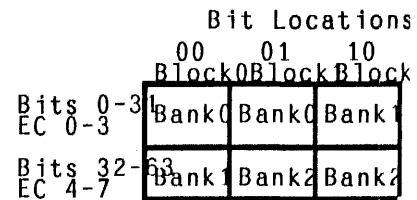
Bit Locations

00	01	10
Block 0	Block 1	Block 2
Bank 0	Bank 1	Bank 2
Bank 0	Bank 1	Bank 2
Bank 0	Bank 1	Bank 2

Block 0&1 bits 0-15

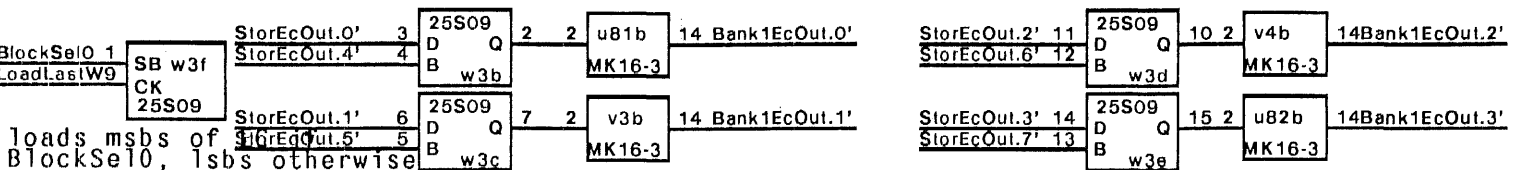
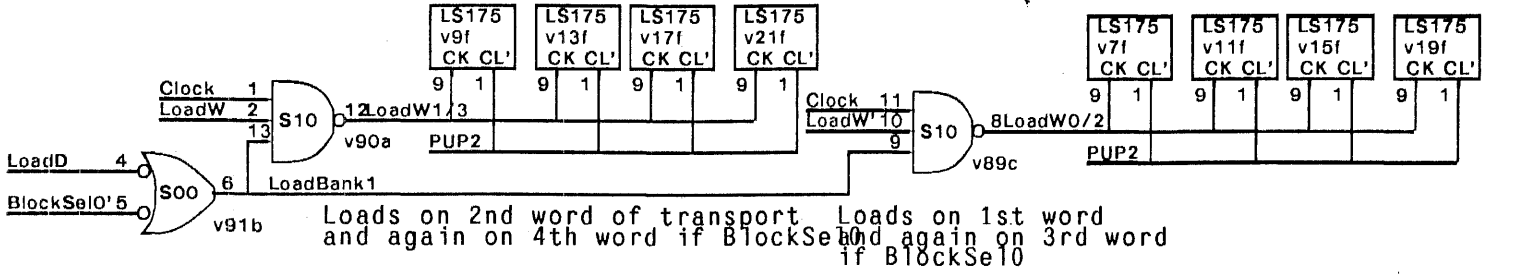
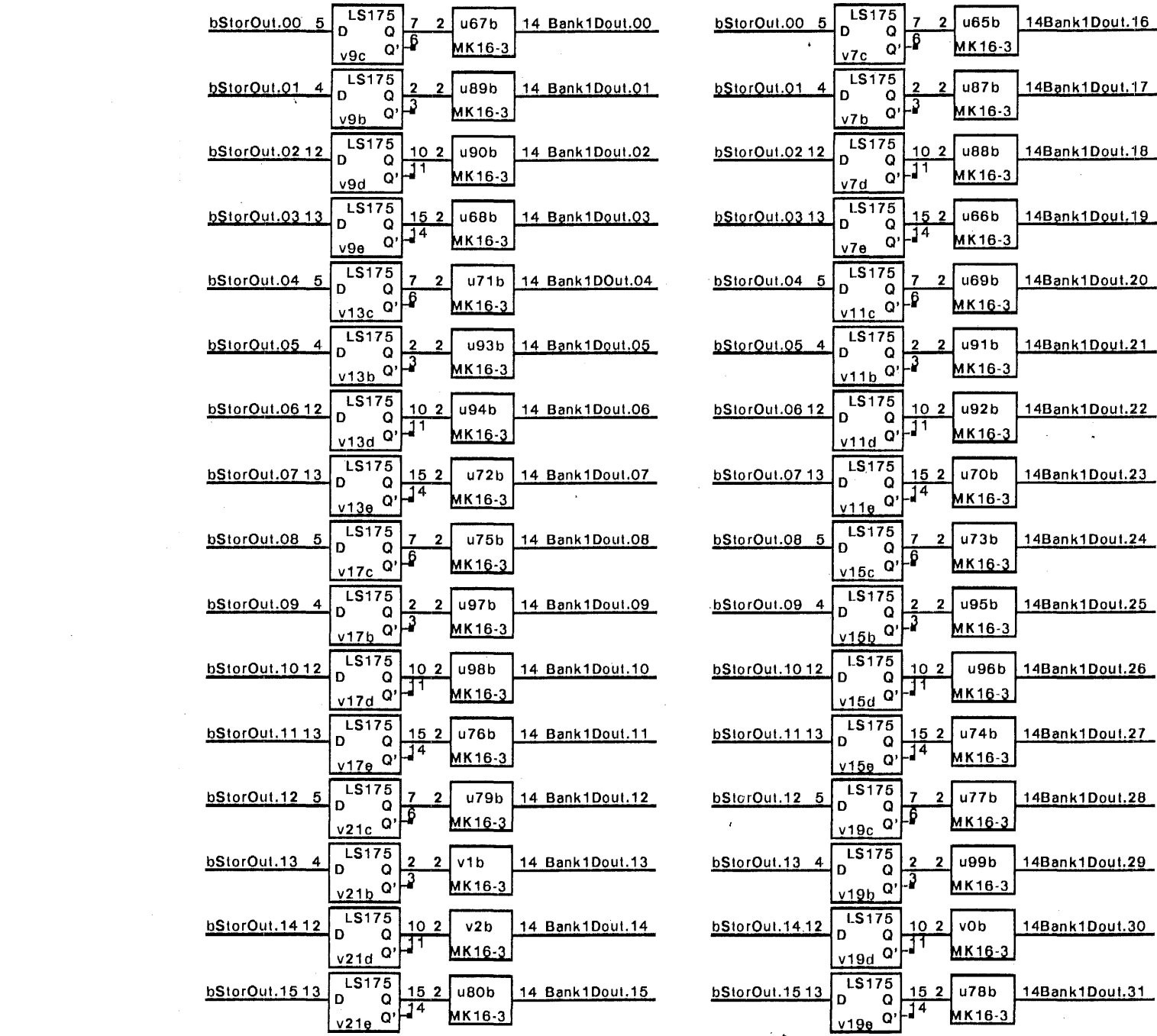


typ of 4 25S09  
see page 14 for others



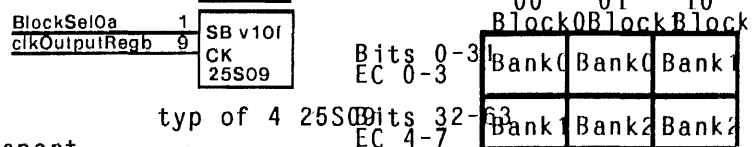
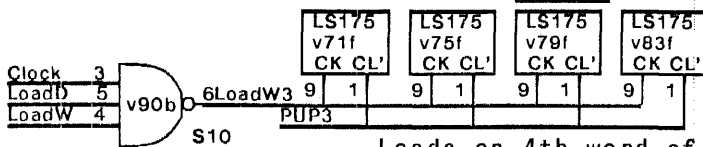
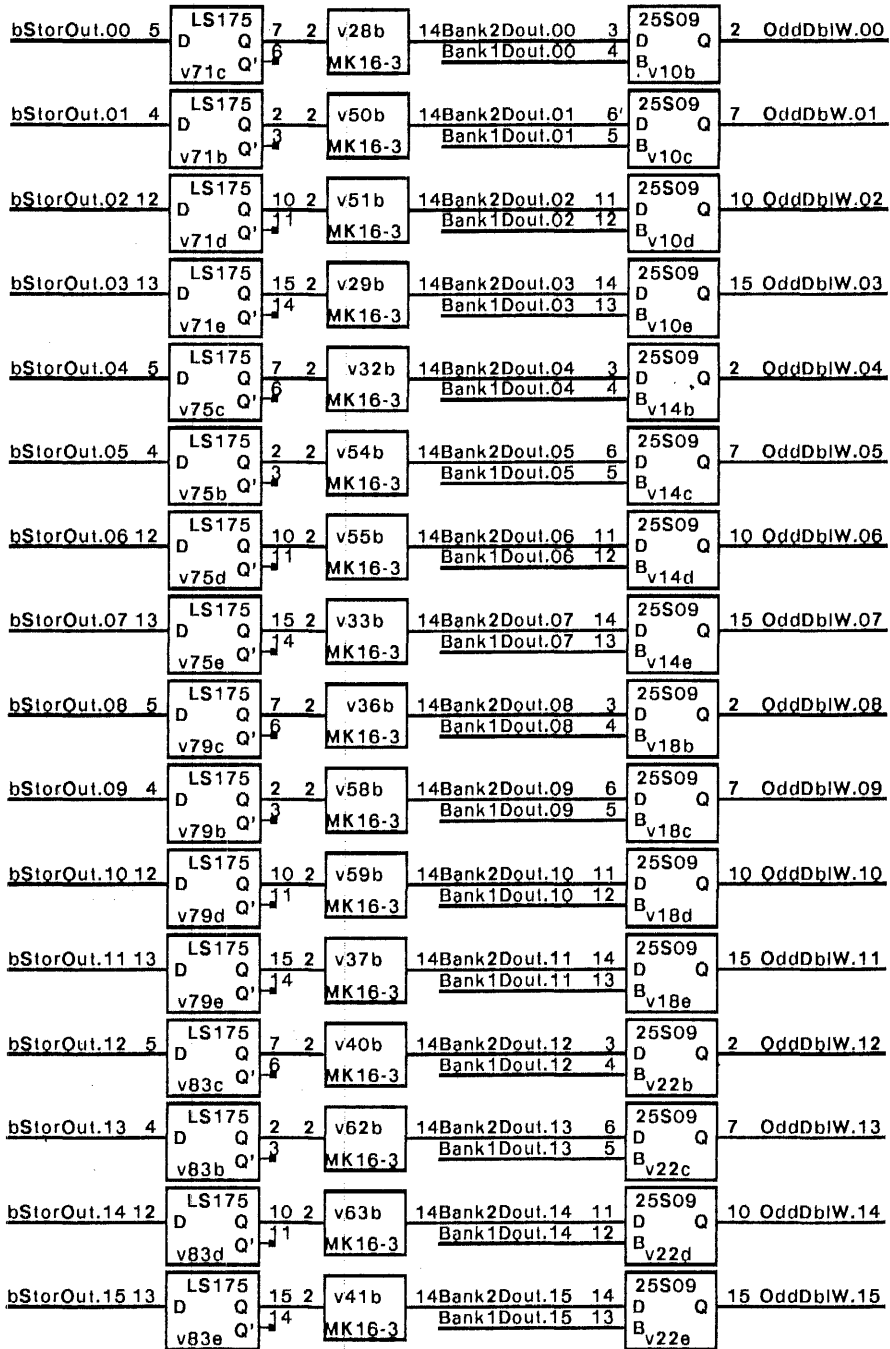
Block 0 bits 48-63  
Block 2 bits 16-31

Block 0 bits 32-4  
Block 2 bits 0-15

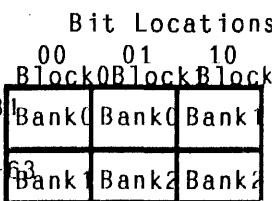
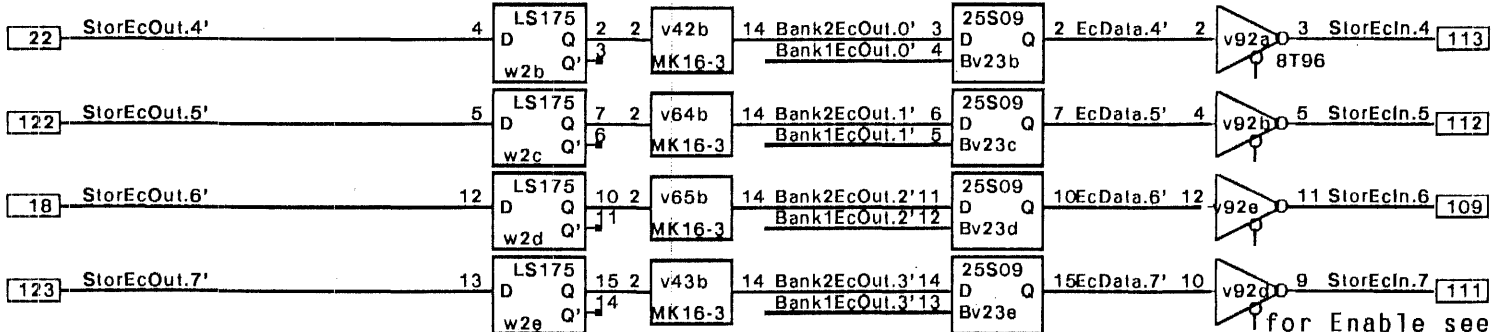


XEROX EOD	Project DO	Storage Card Bank 1	File D0stor03.sil	Designer Rosen	Rev B	Date 1/26/80	Page 03
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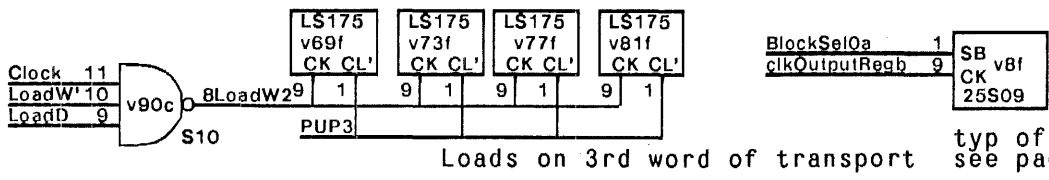
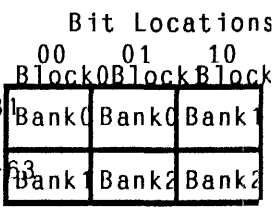
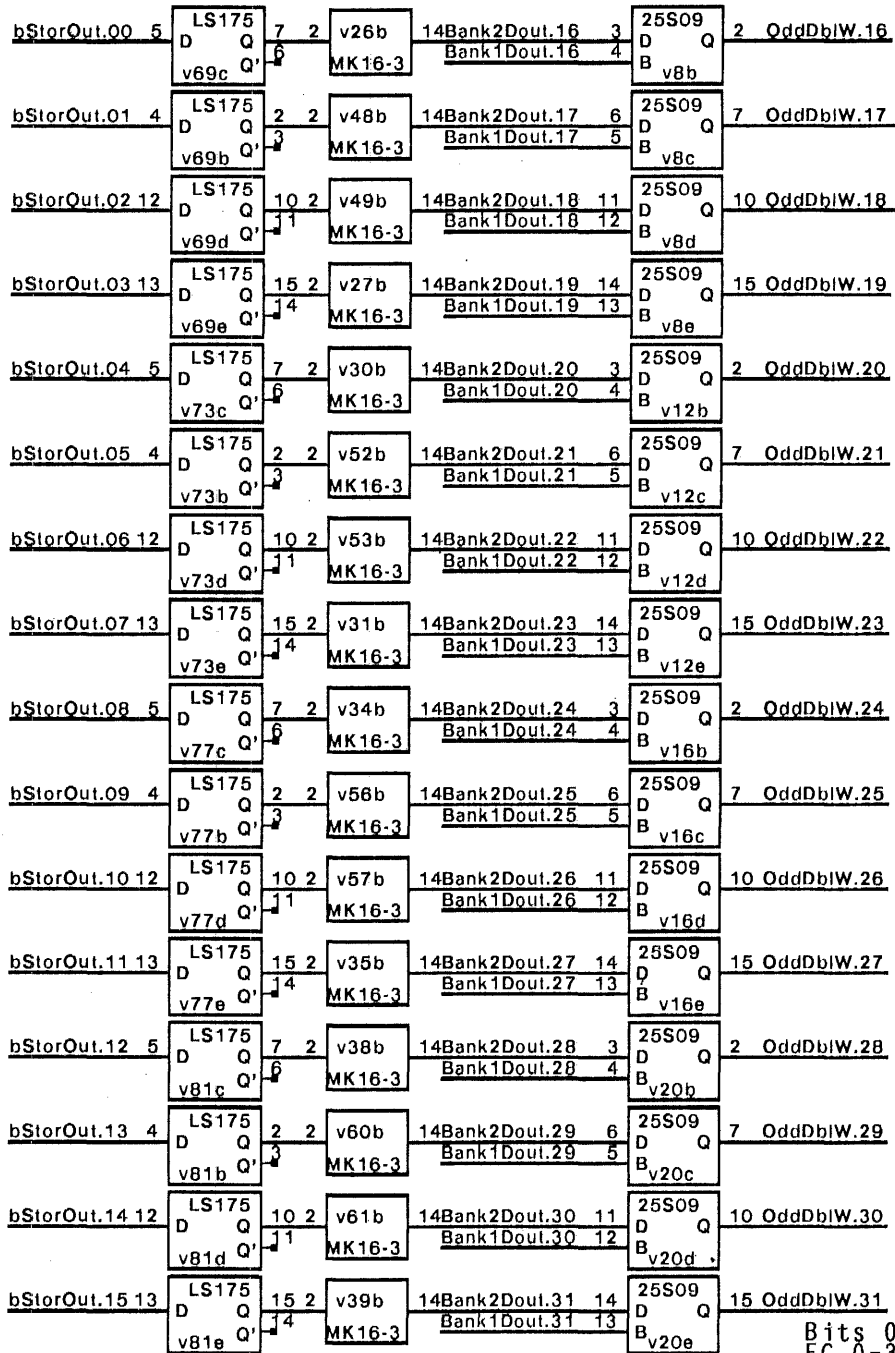
Blocks 1&2 bits 48-63

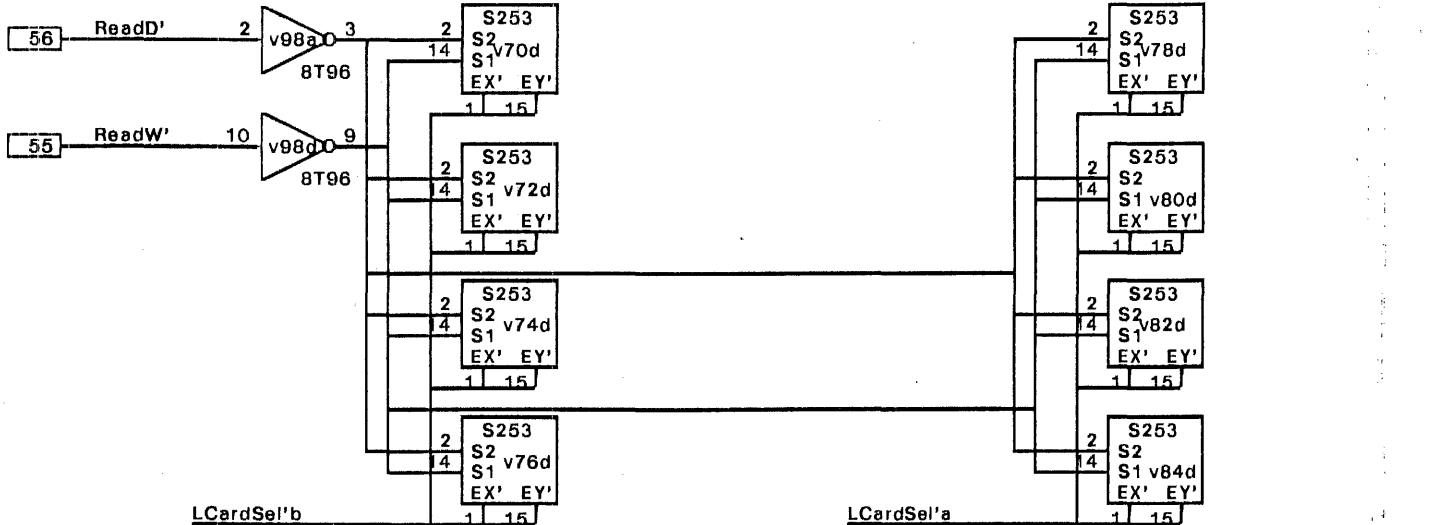
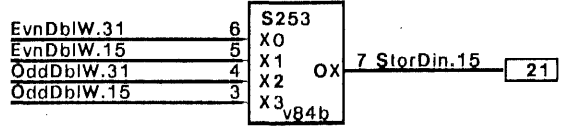
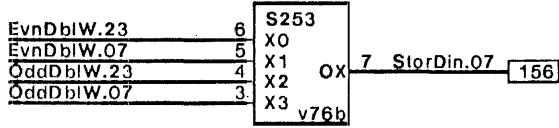
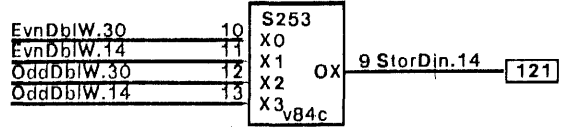
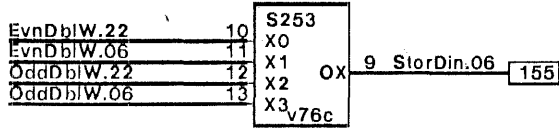
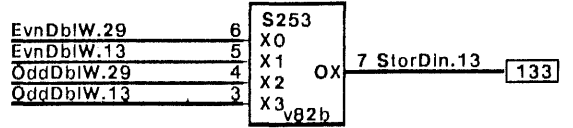
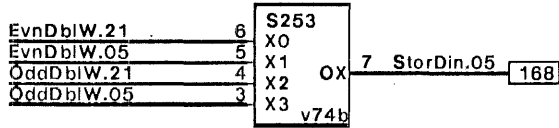
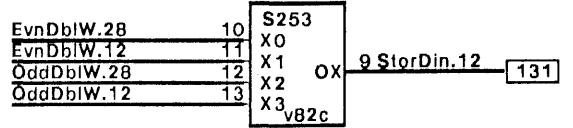
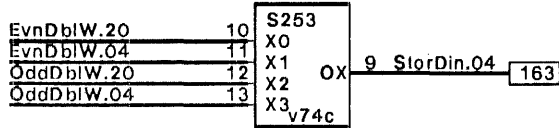
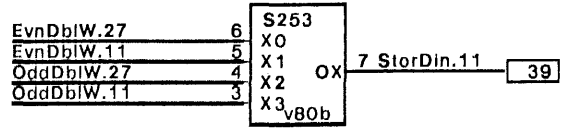
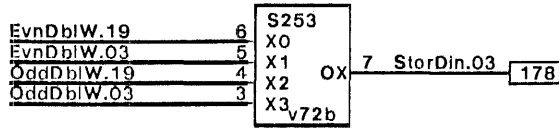
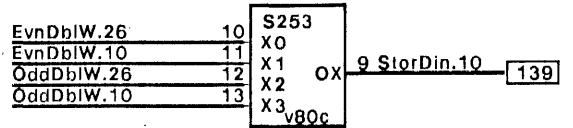
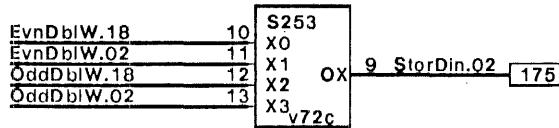
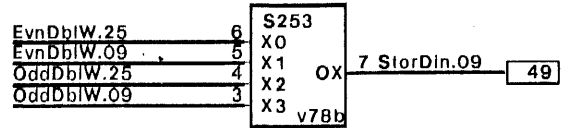
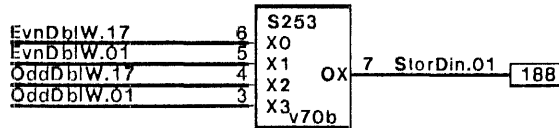
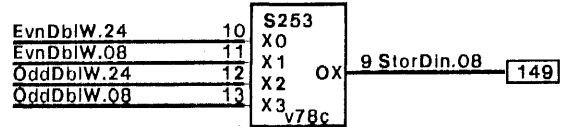
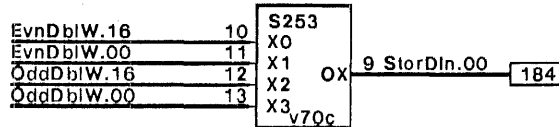


Loads on 4th word of transport  
 Clocked same time as last Data Word see page 14 for others



Blocks 1&2 bits 32-47

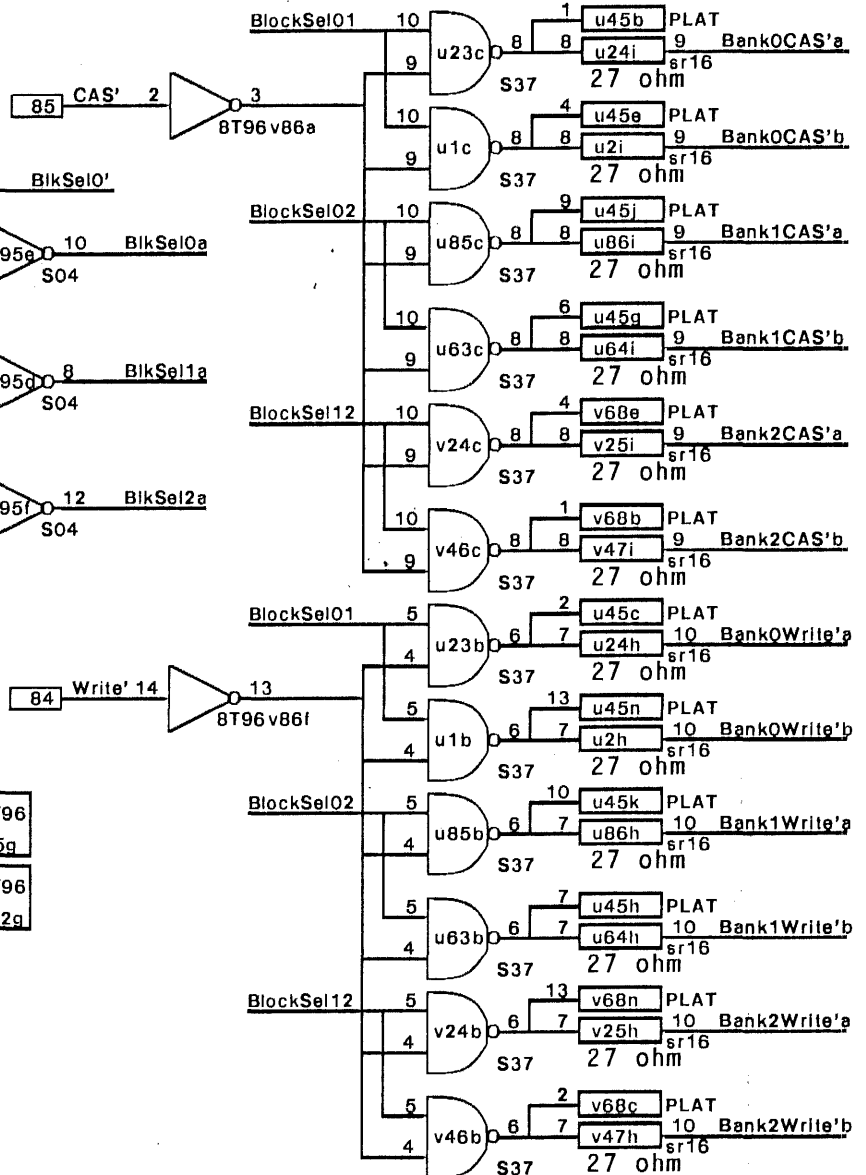
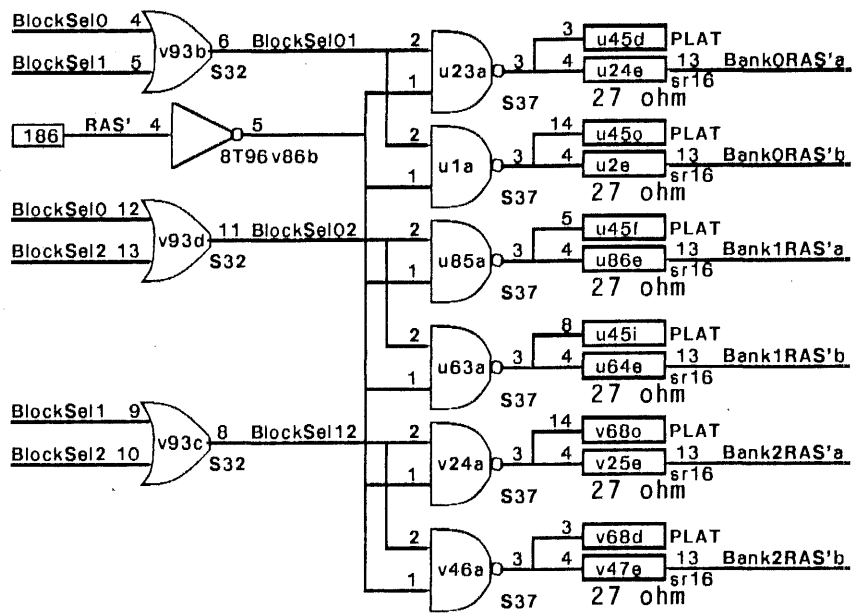
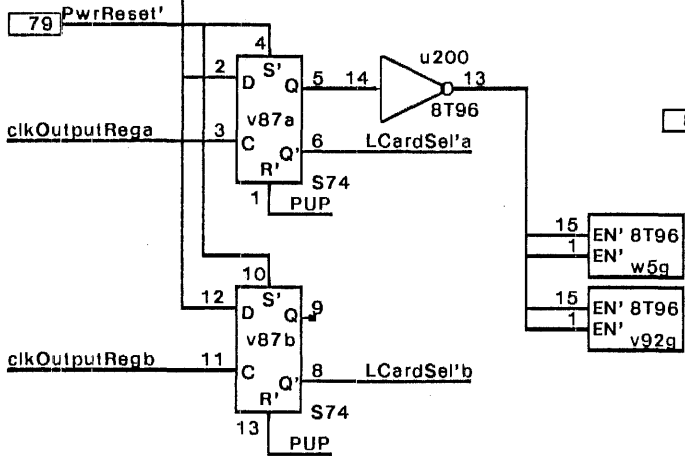
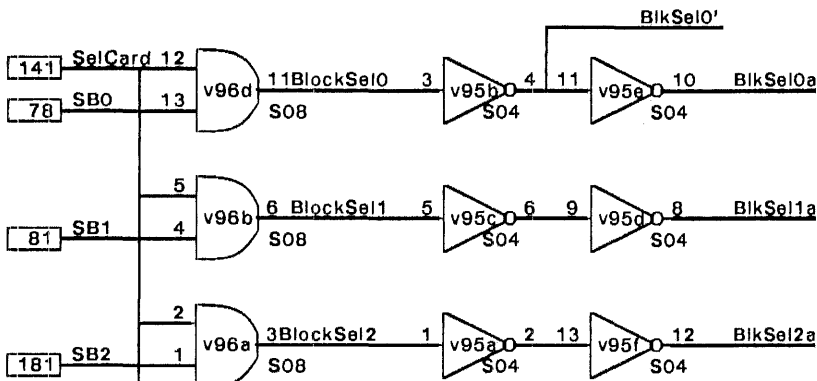
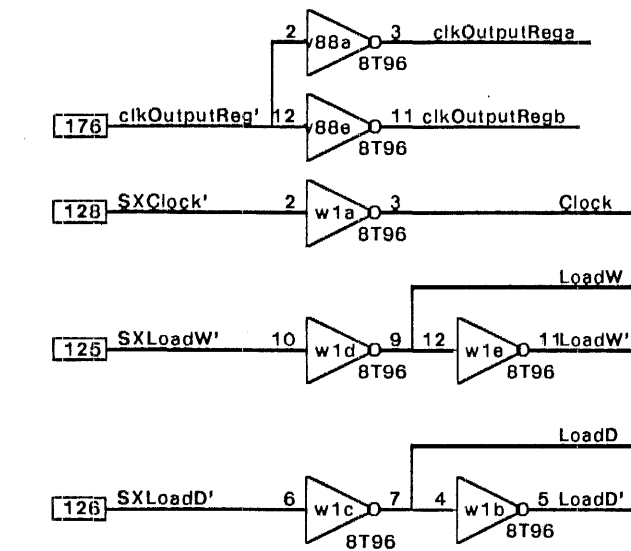


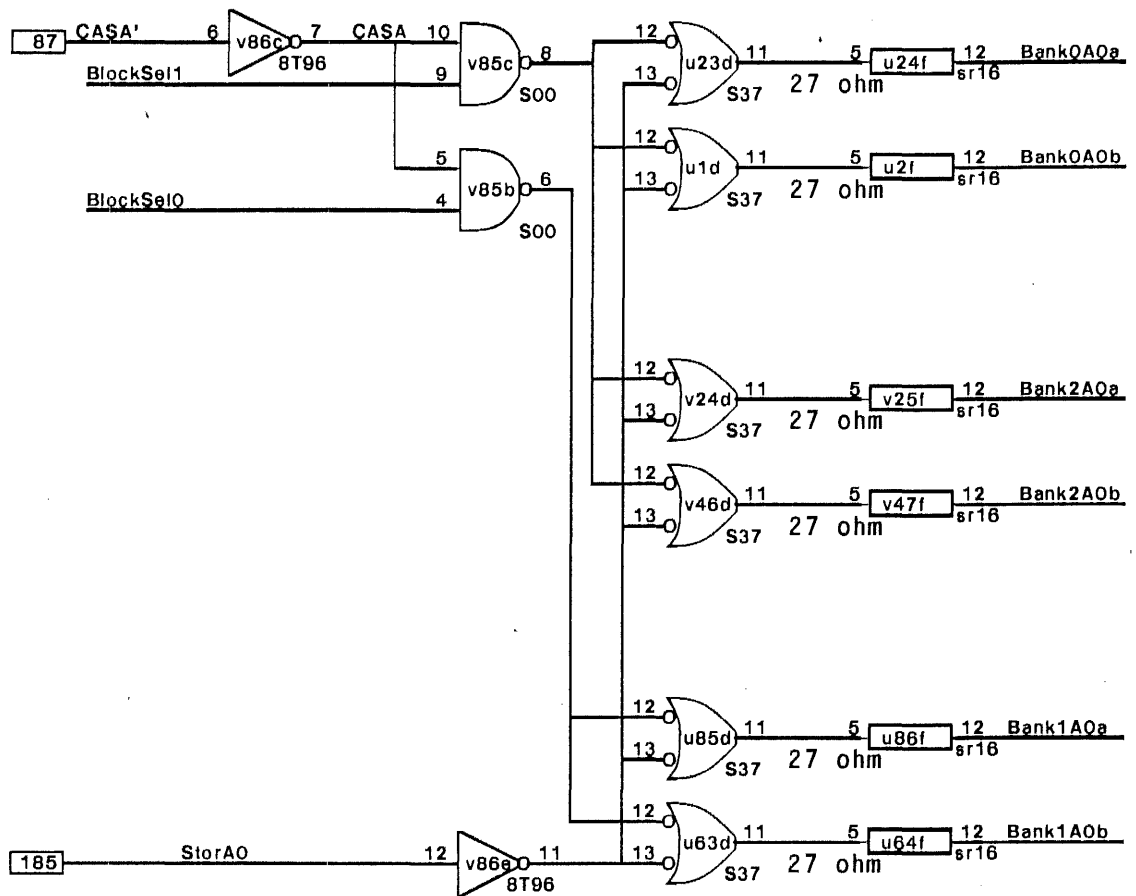


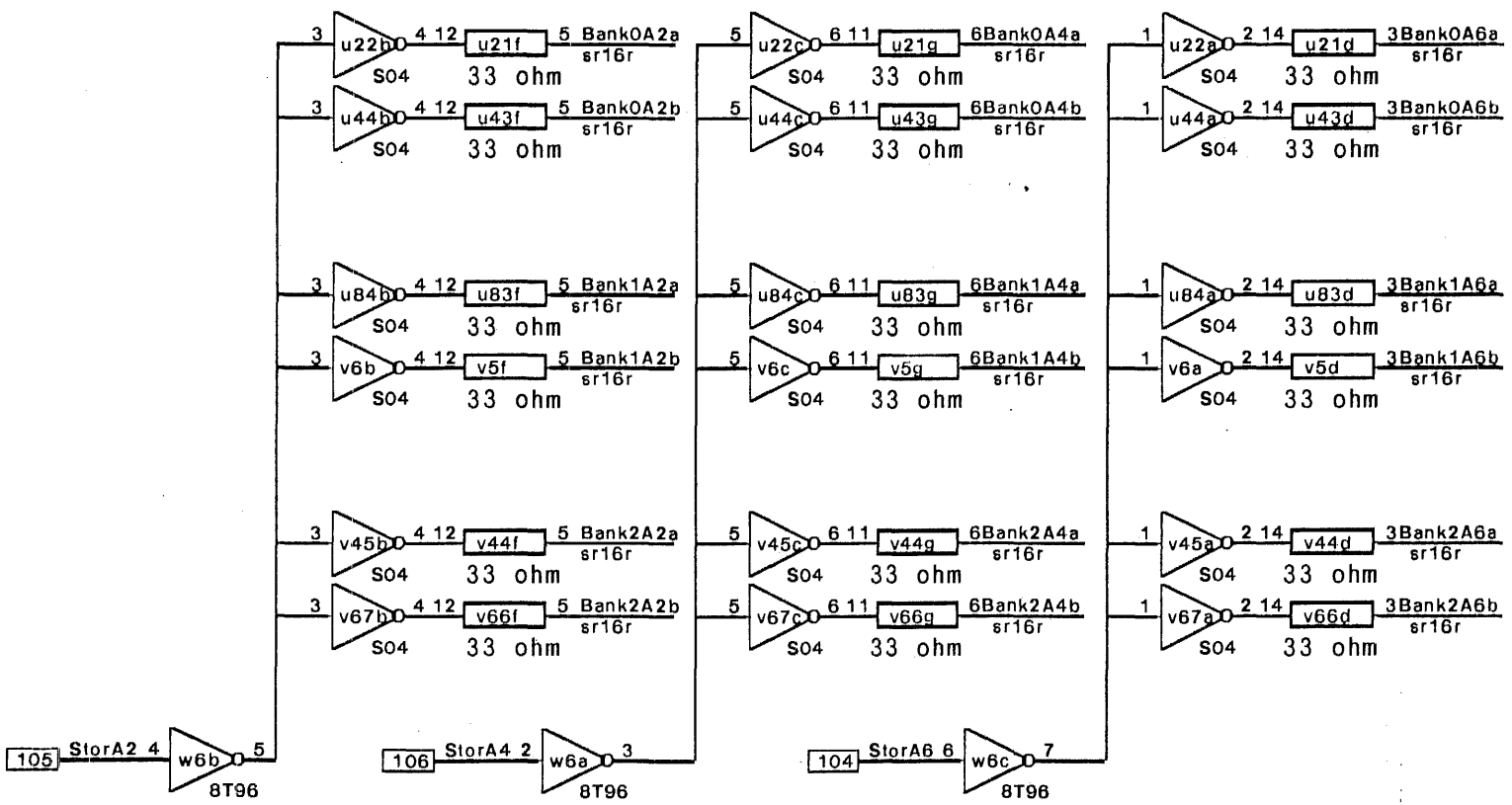
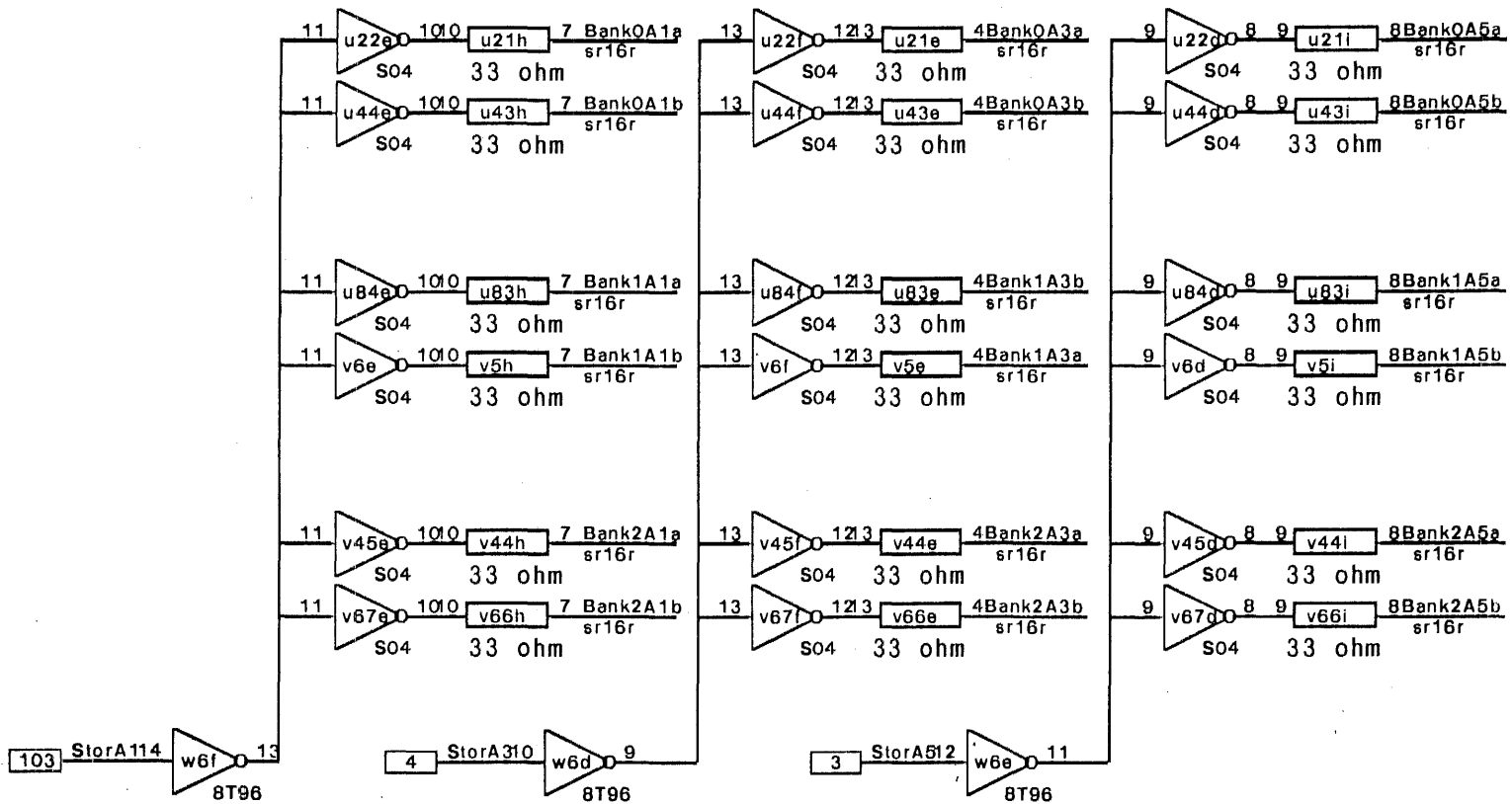


174 SB3  
 Shown for completeness only  
 Not used on 96k storage card

36 SRIn  
 136 SROut  
 Jumper for I/O Boards





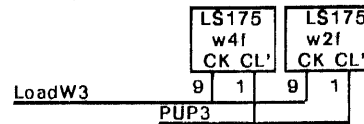
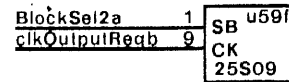
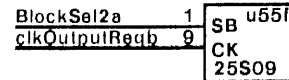
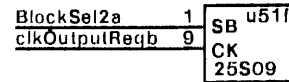
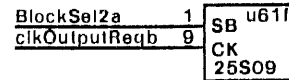
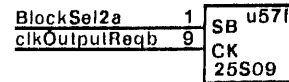
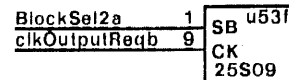
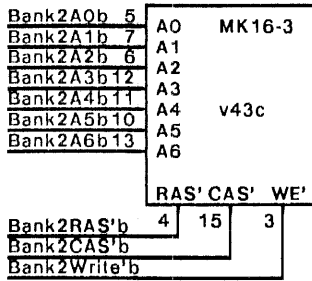
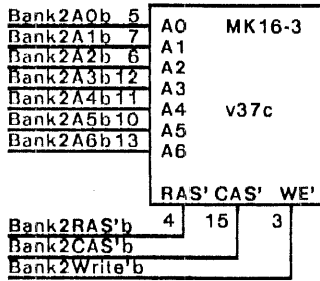
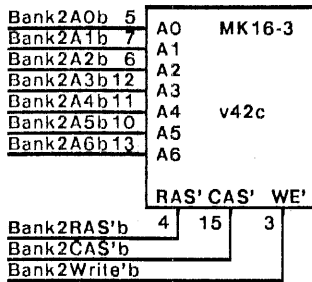
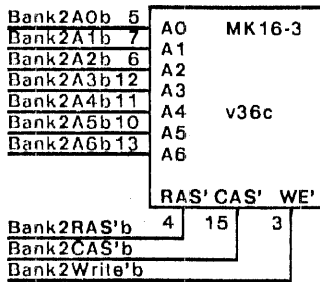
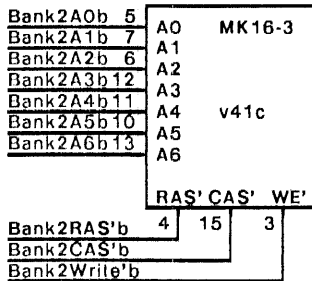
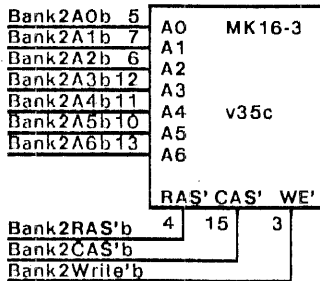
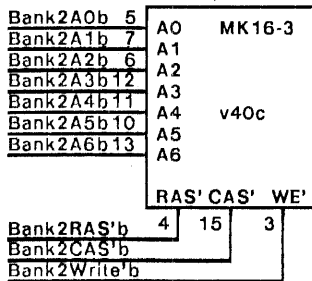
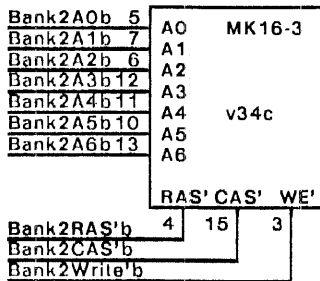
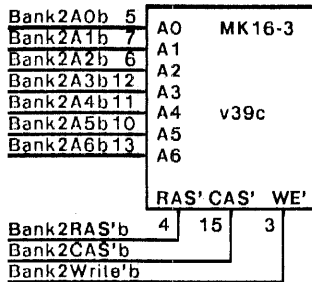
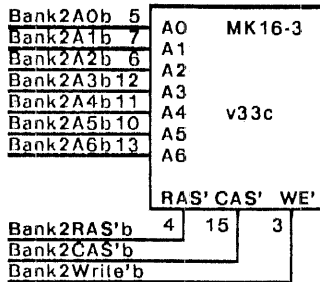
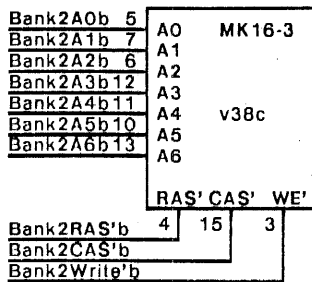
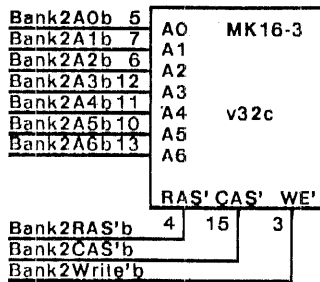




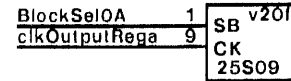
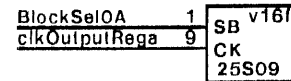
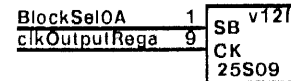
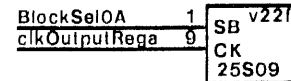
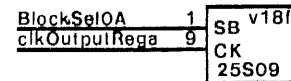
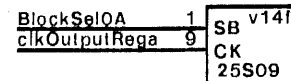




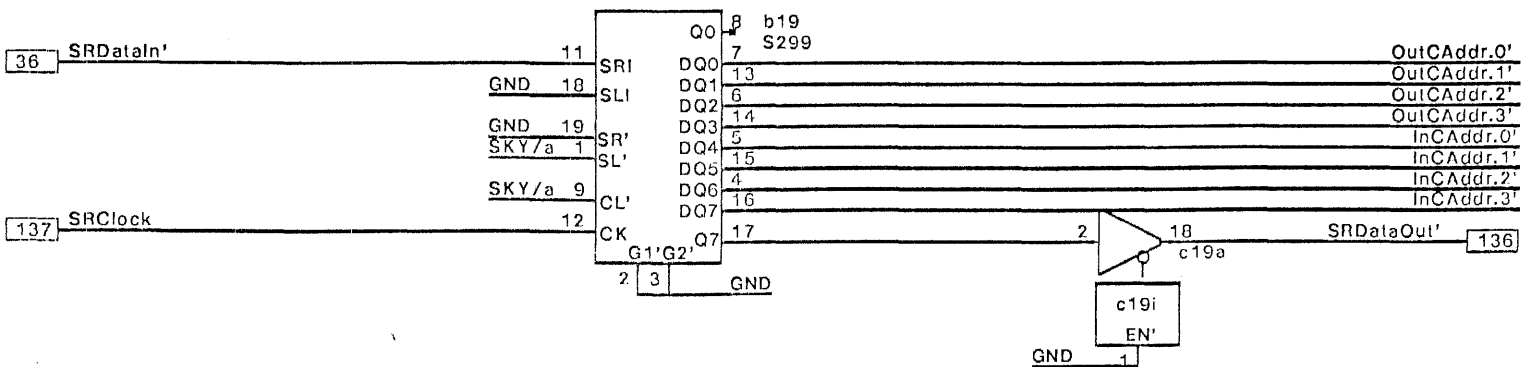
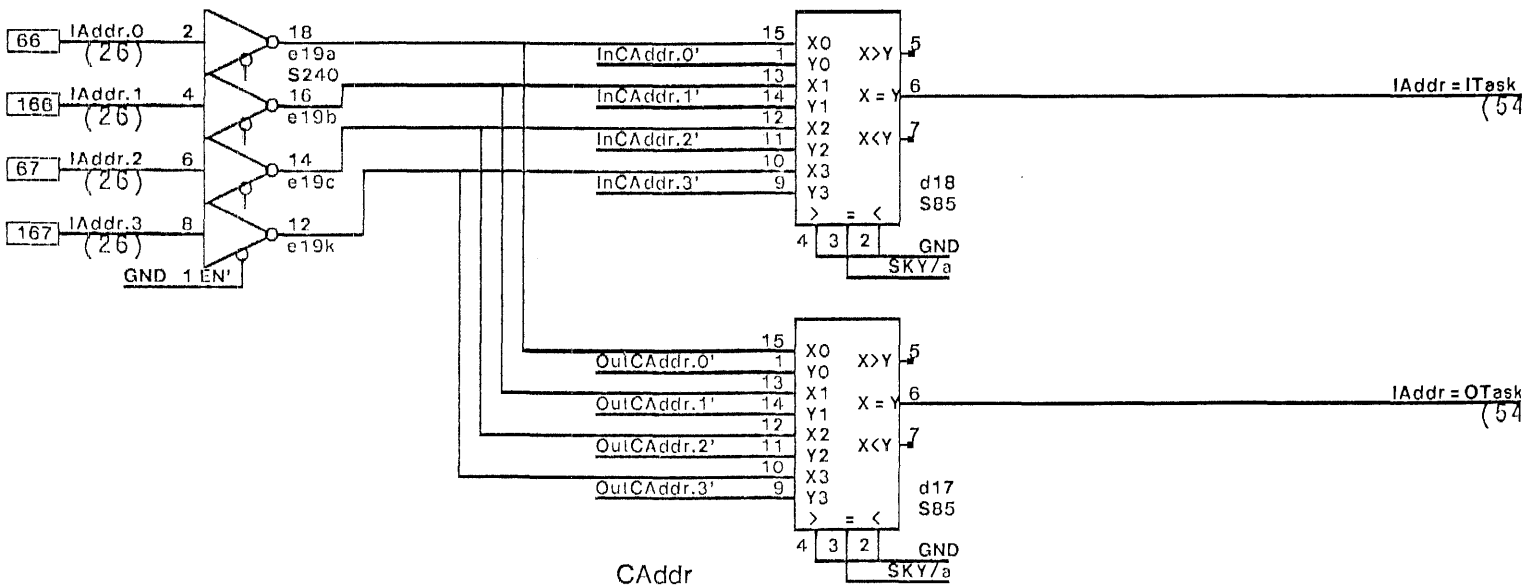
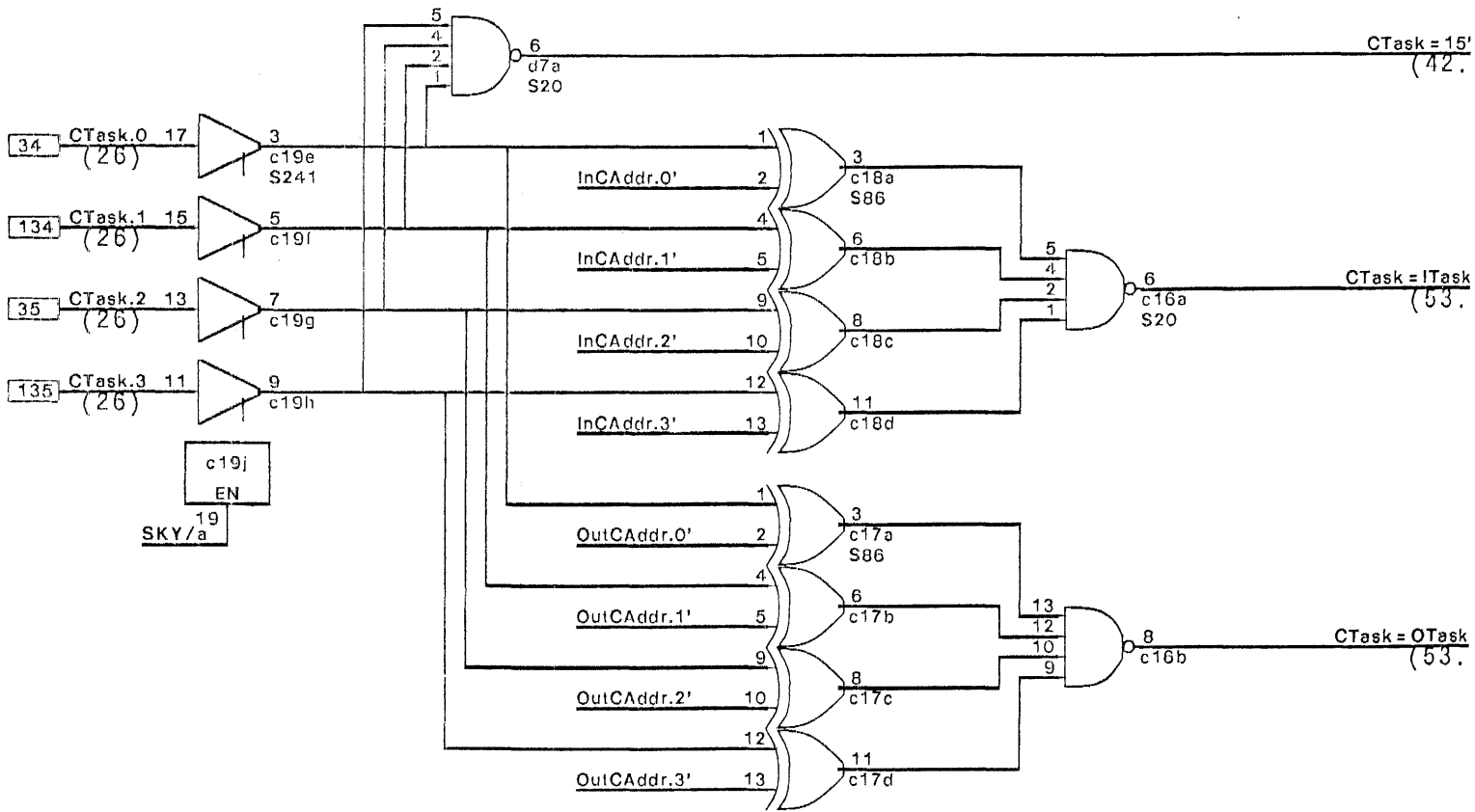


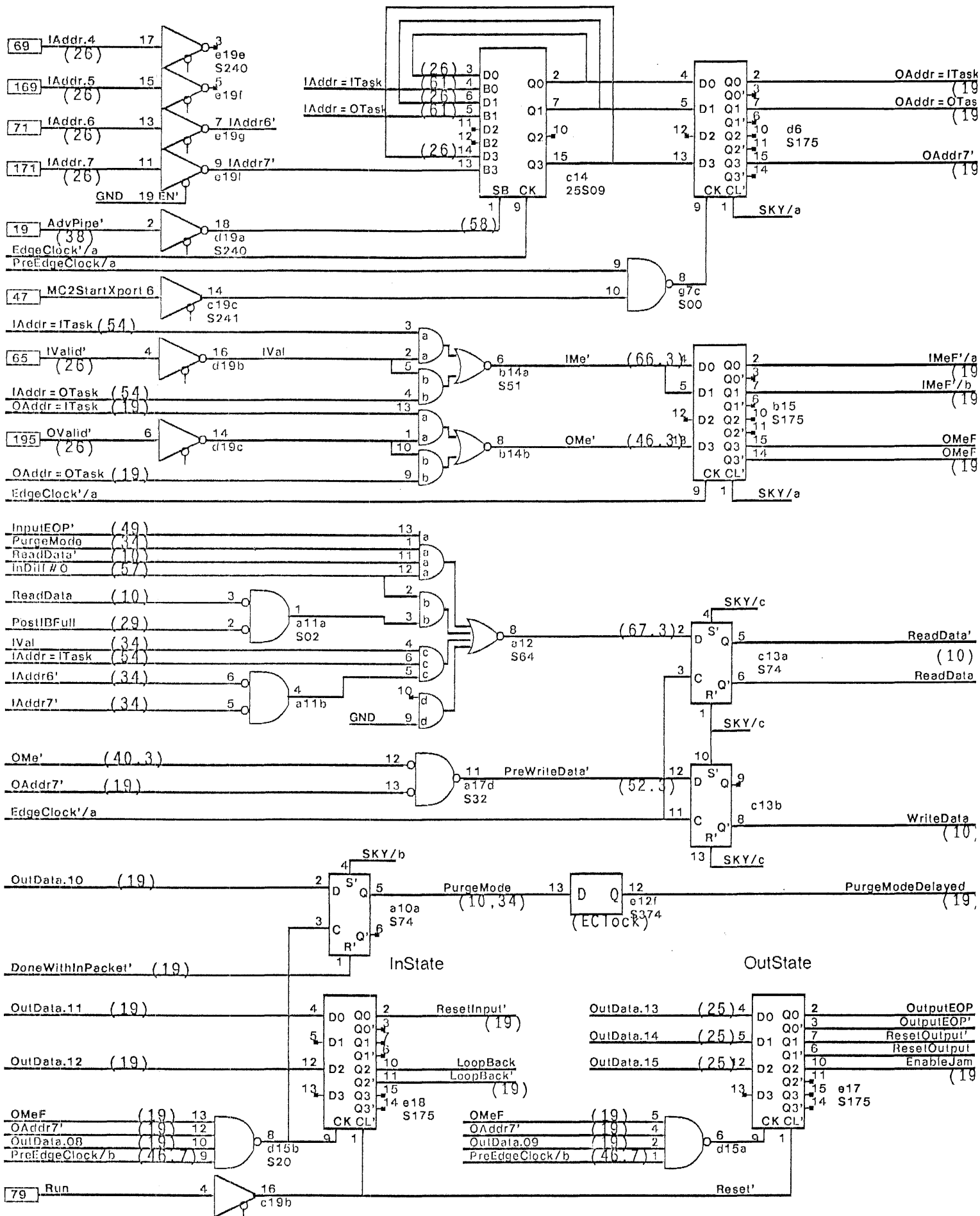


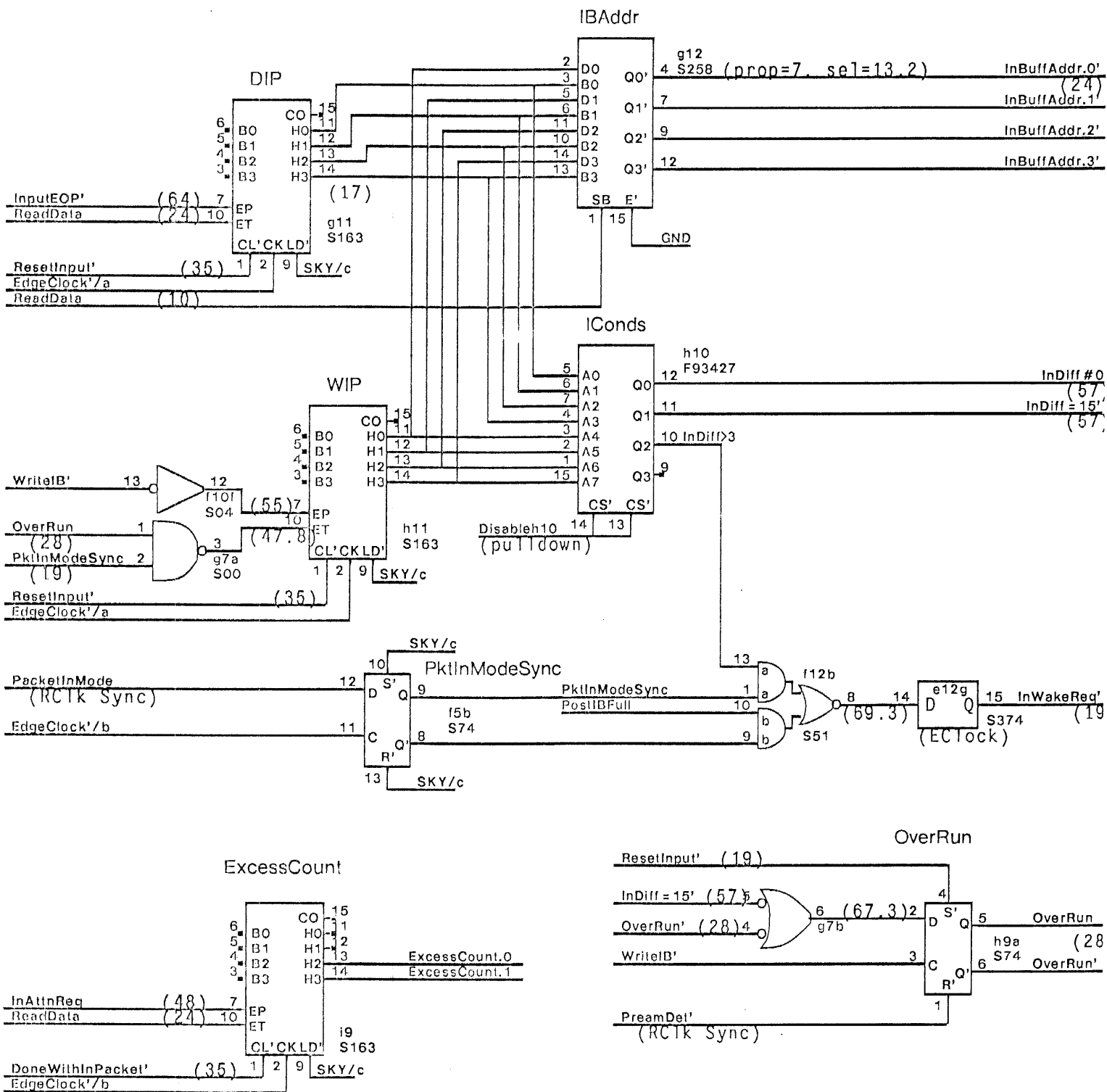
Part of EC input register, which is sha banks 0 and 2

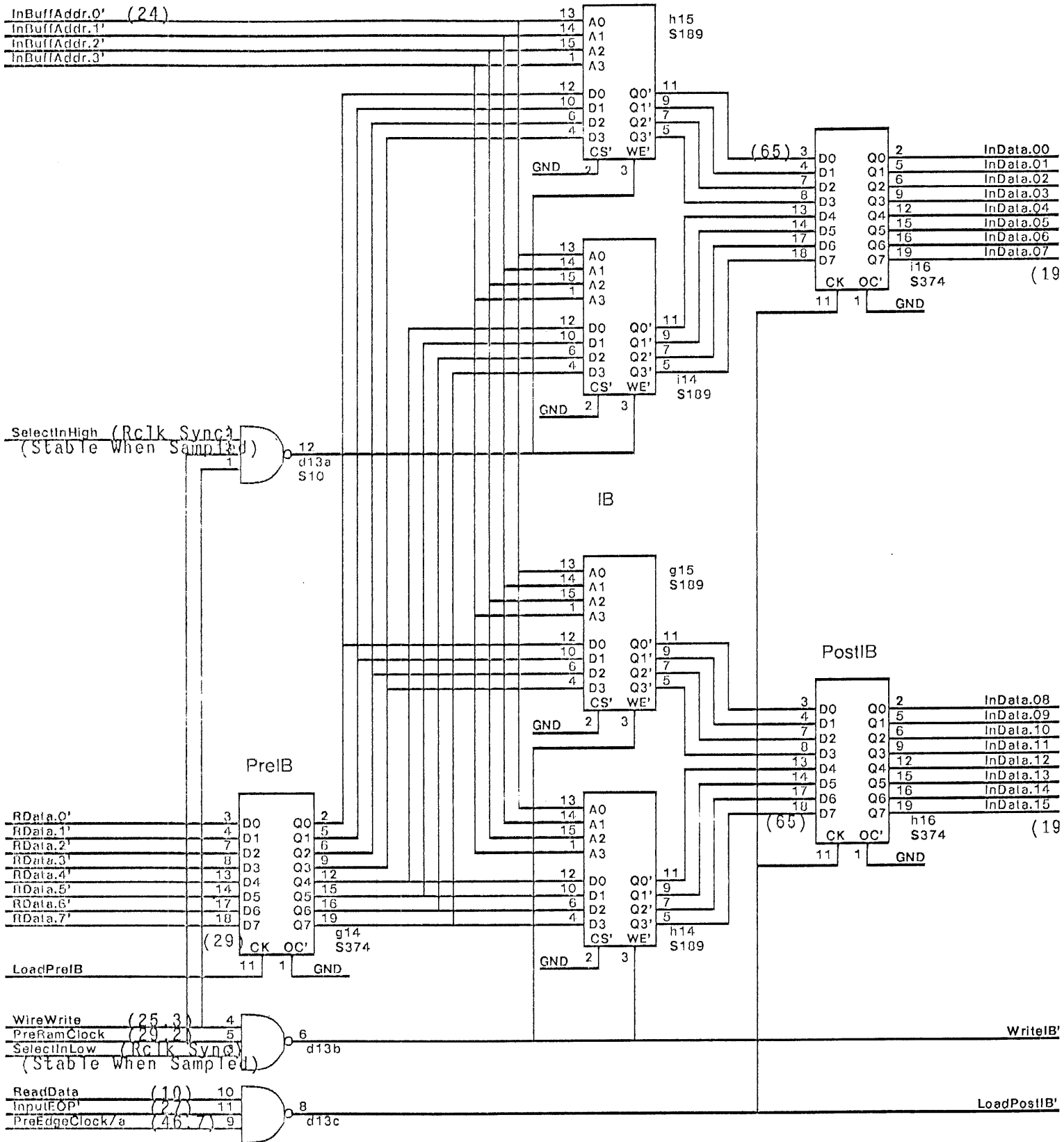


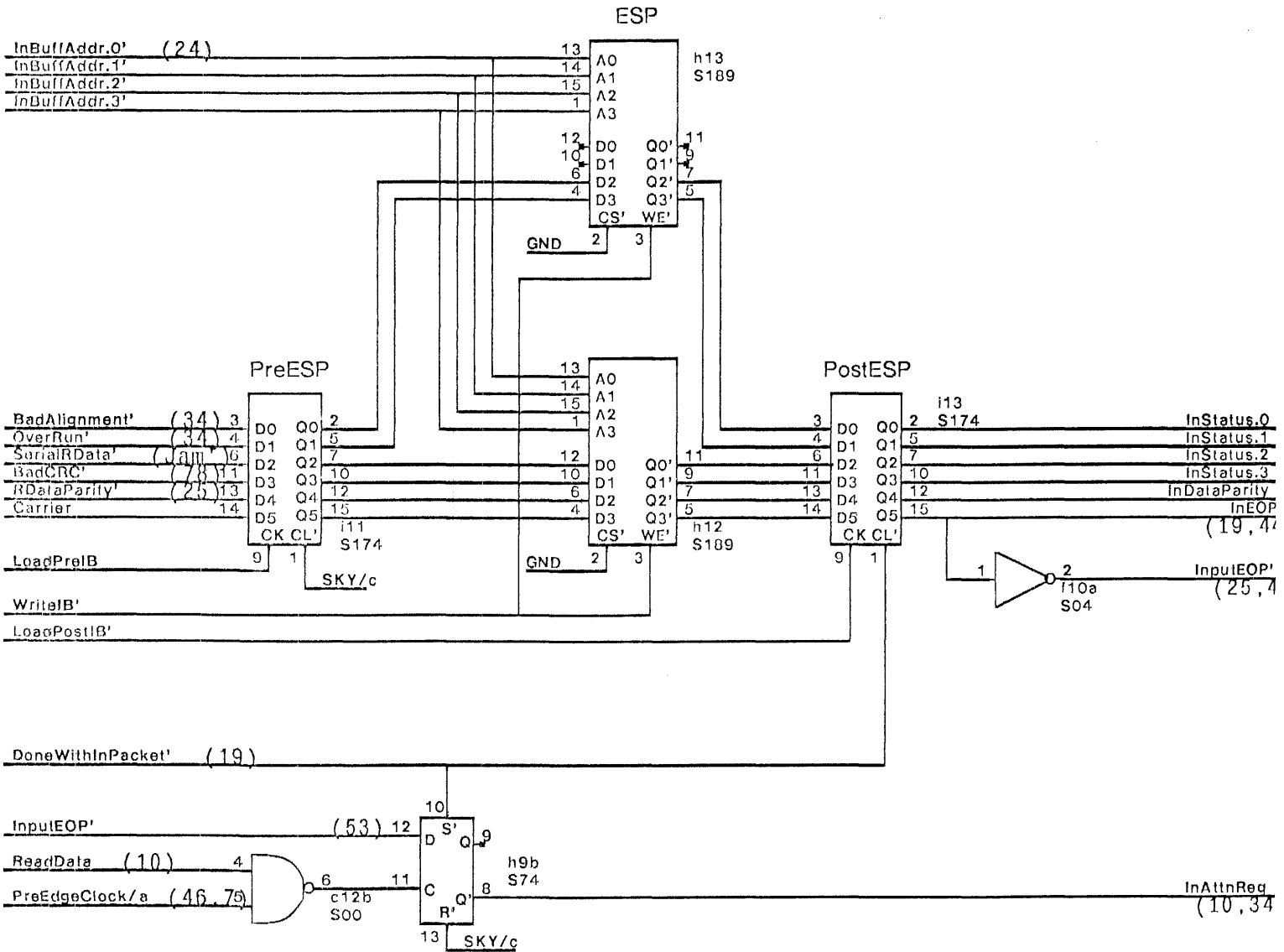


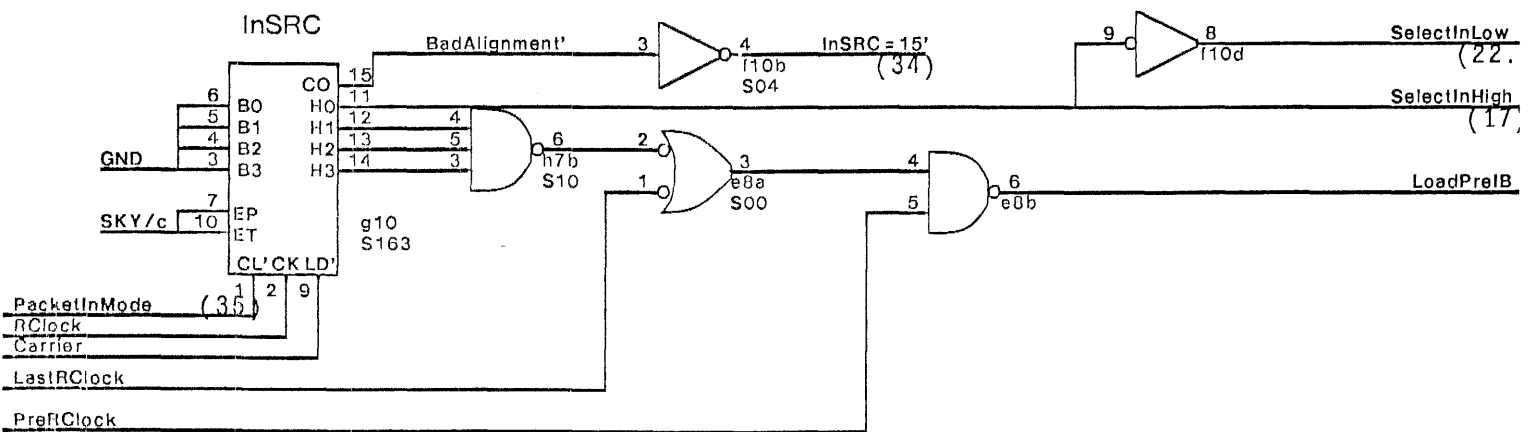
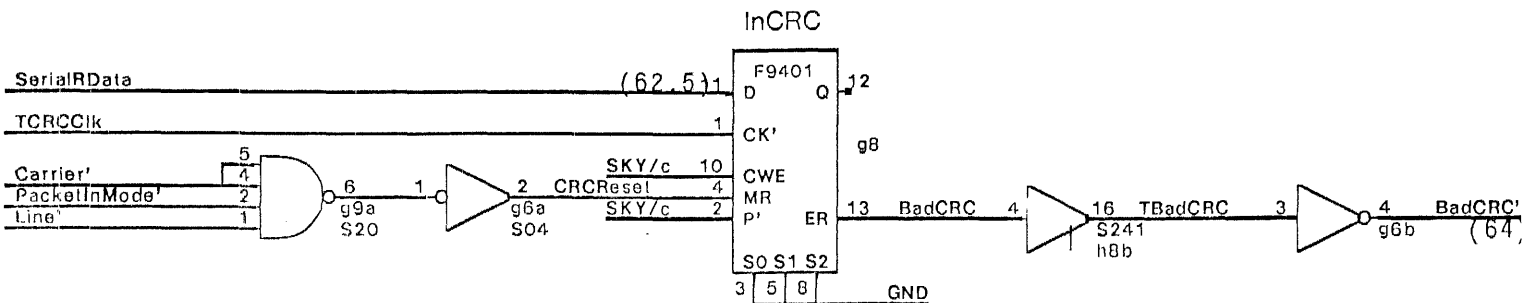
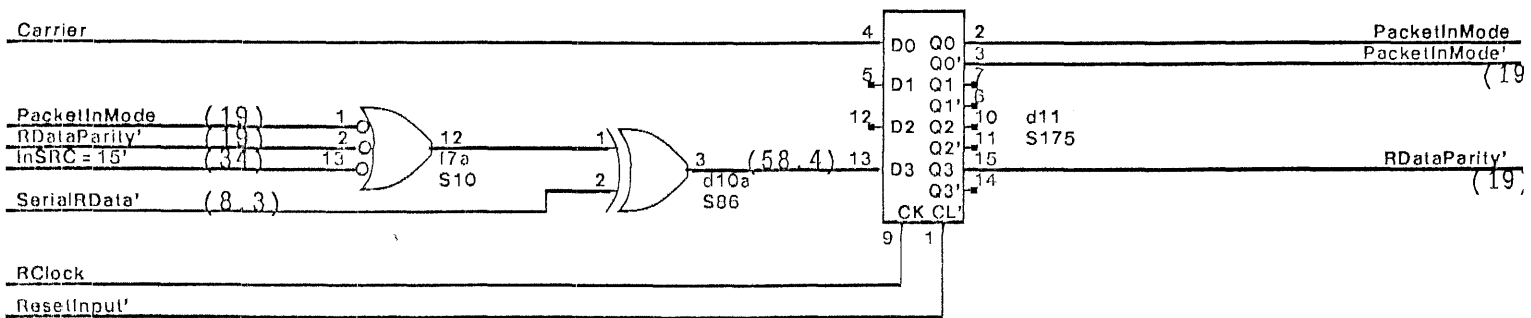
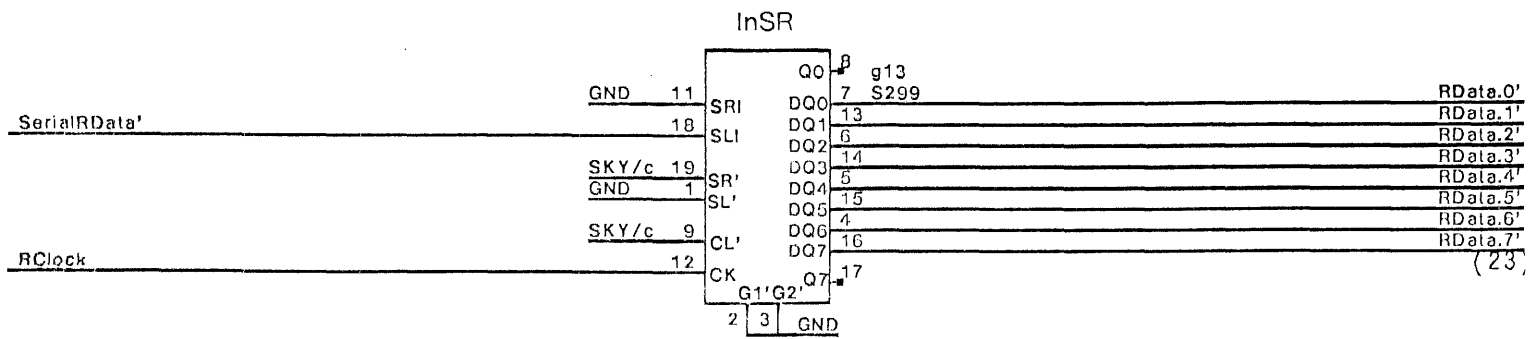


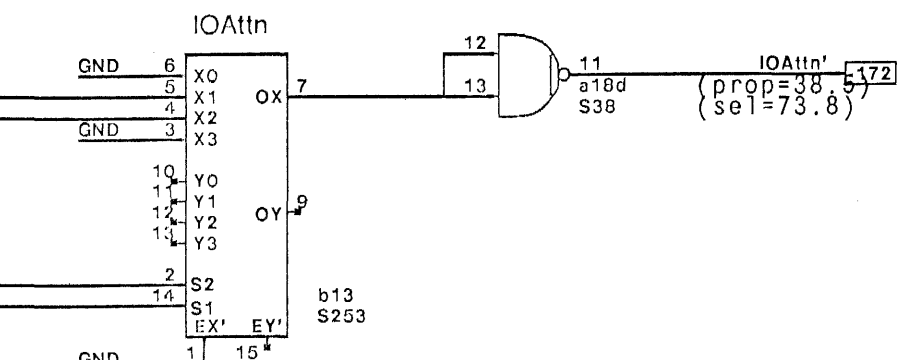
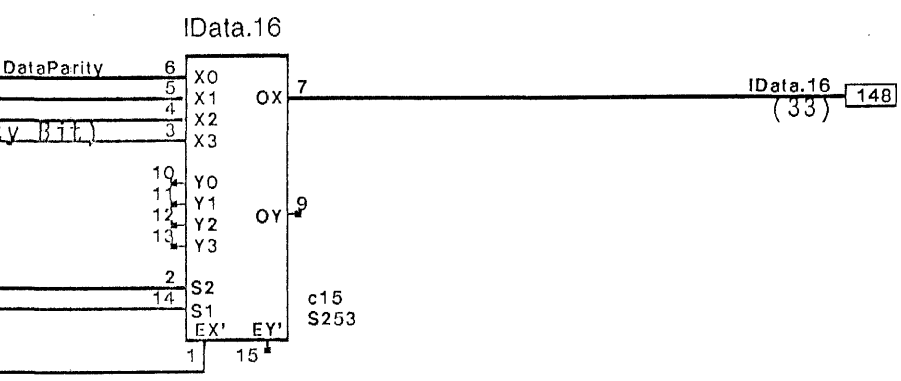
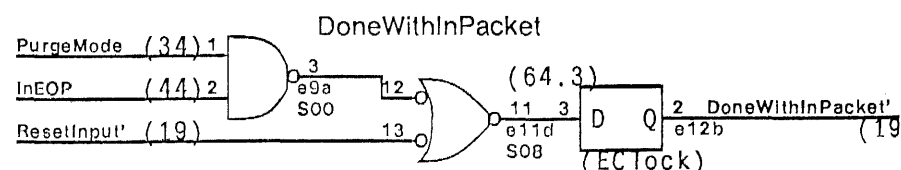
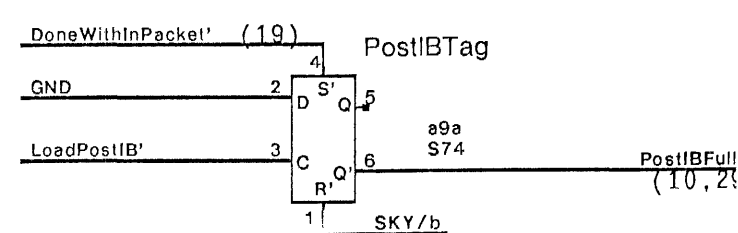
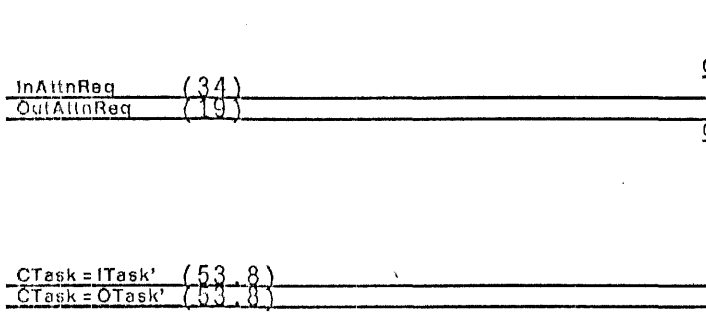
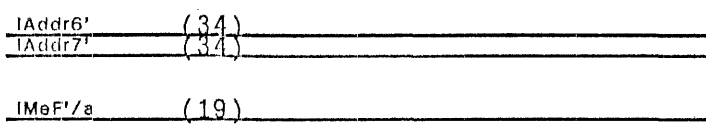
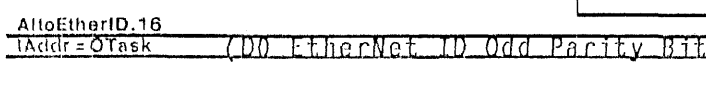
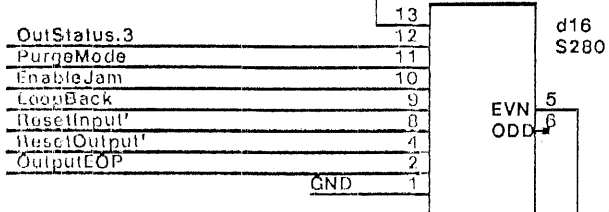
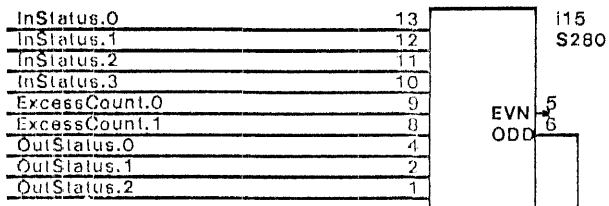
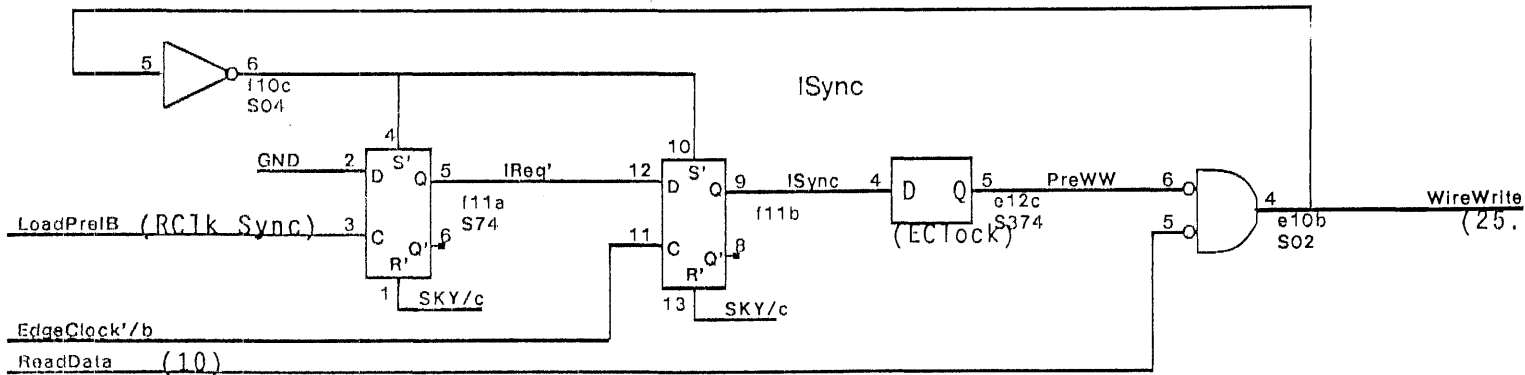


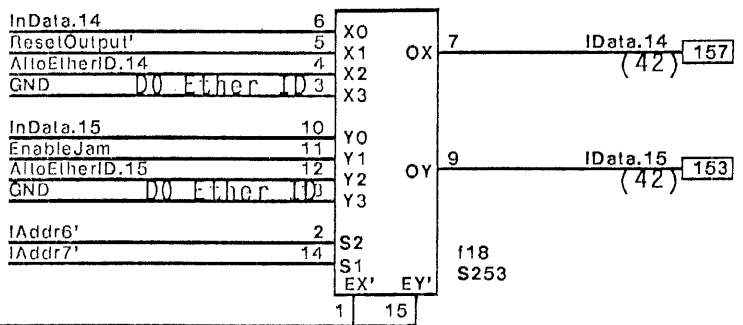
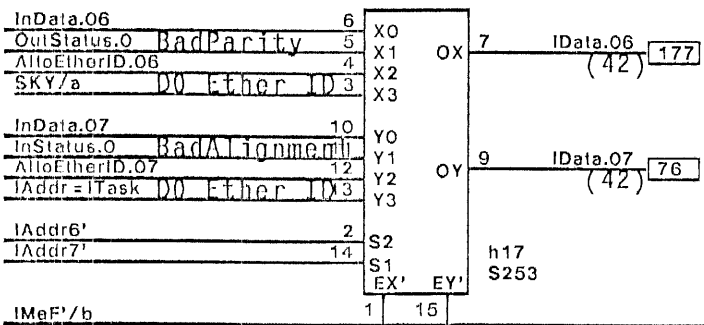
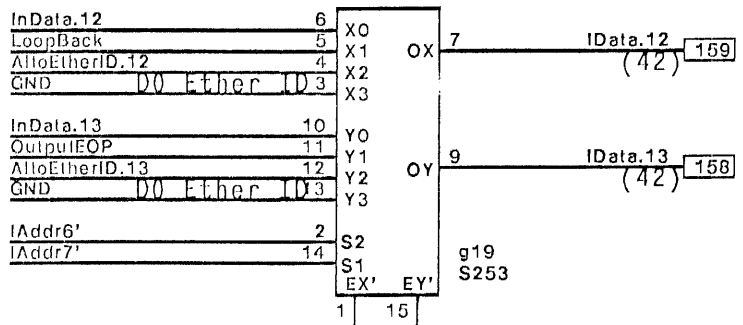
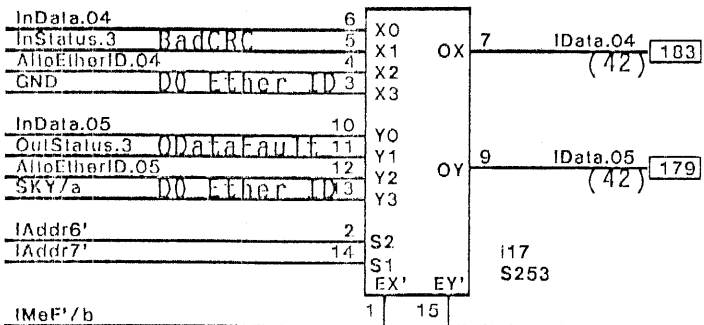
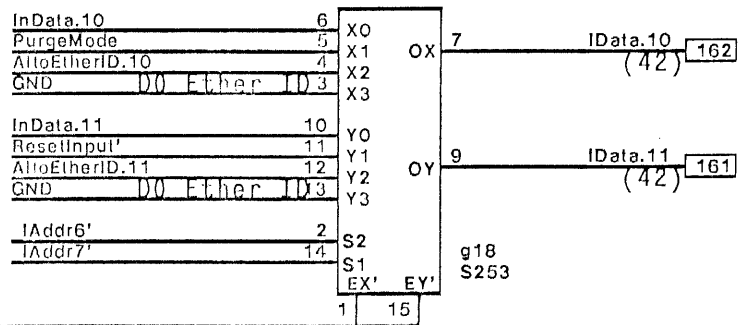
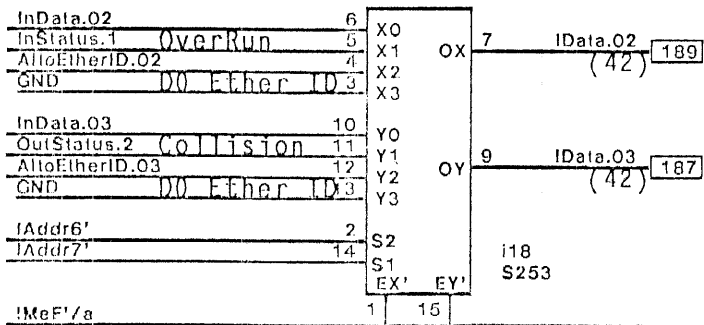
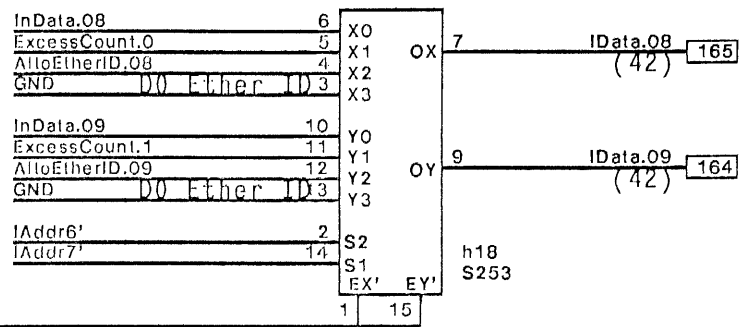
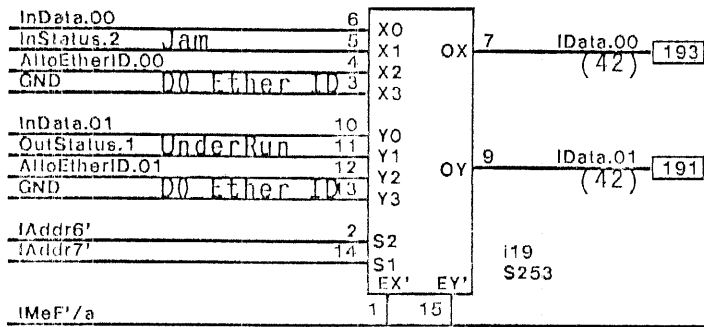








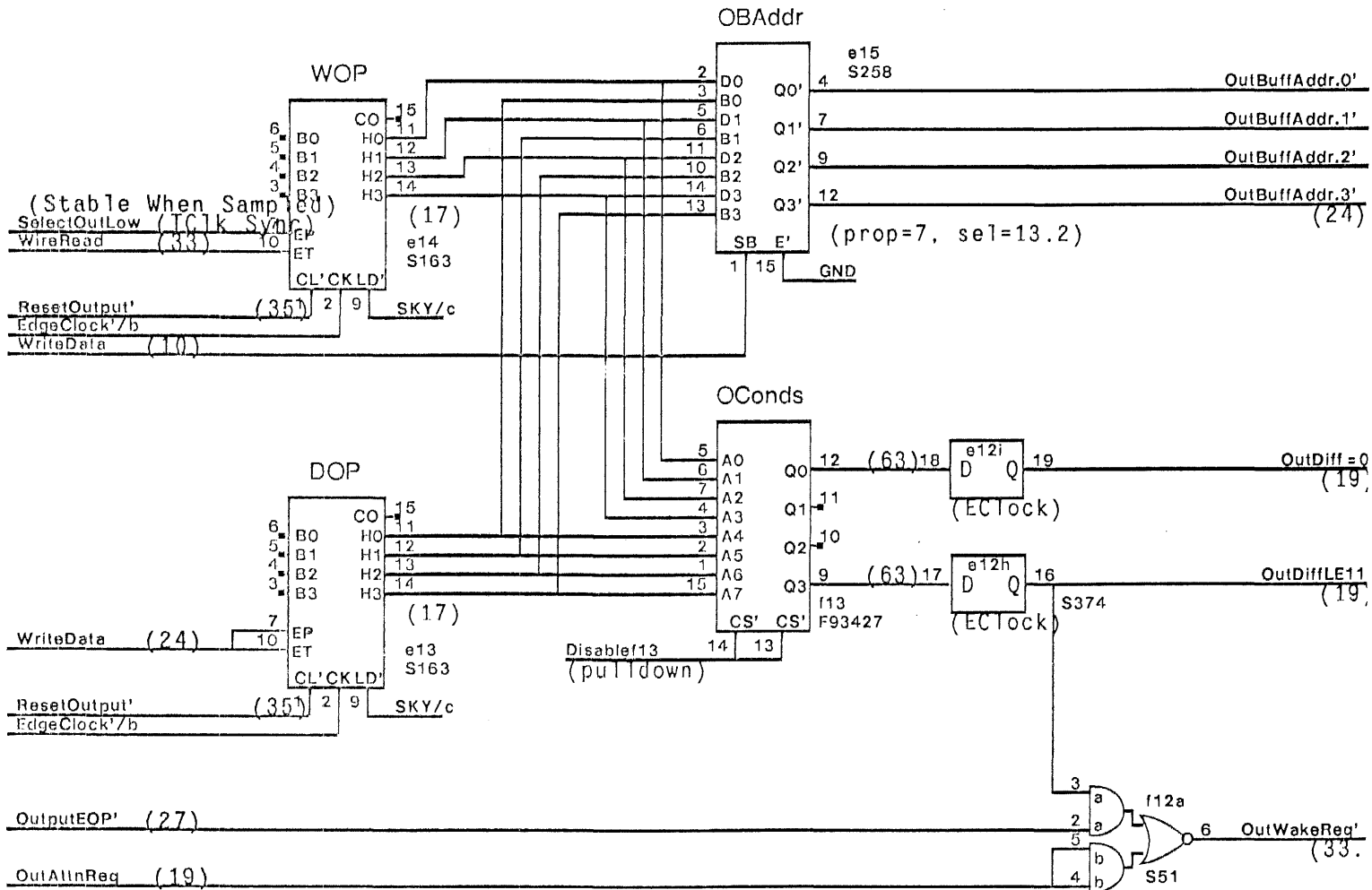


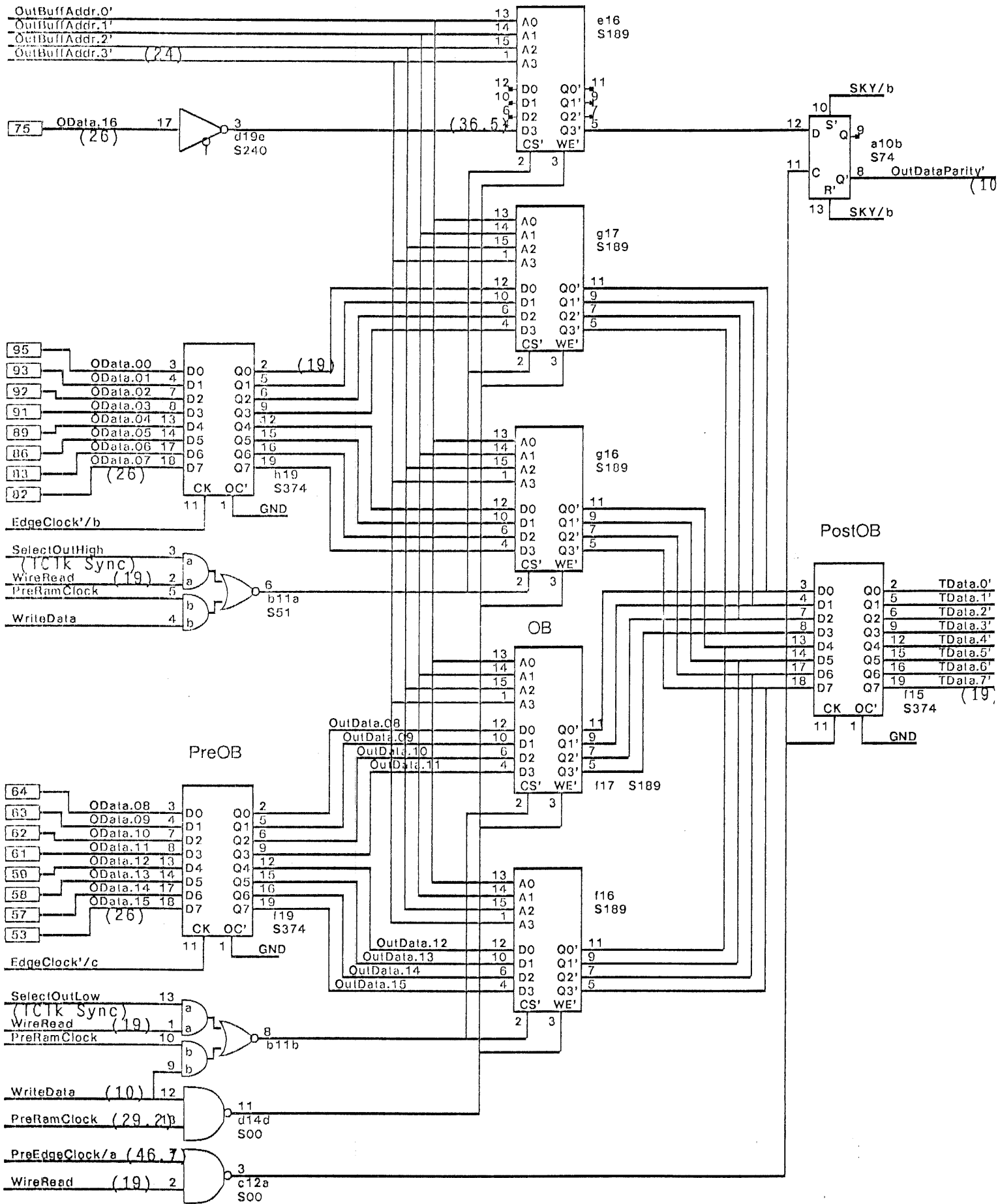


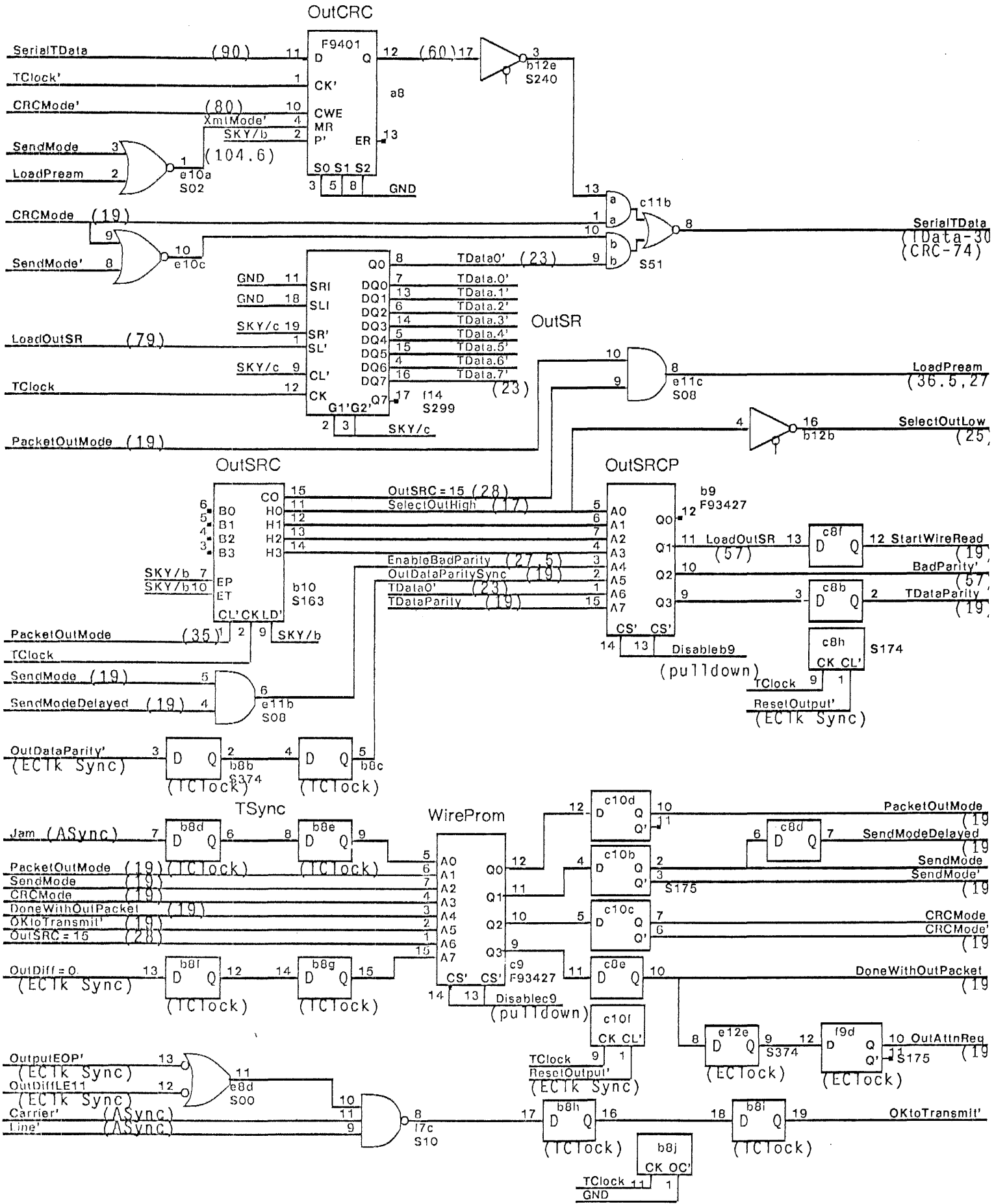
Note: IAddr  
 00 DO Ethernet Device ID high byte = 6 for output and 7 for input. Low byte is always  
 01 Alto EtherNet ID (This simulates the number the Alto EtherNet obtains from the AI  
 10 Status-State  
 11 Input Data  
 Device ID Modifier [0:7] = 00 000 11x Where x = 0 for output and x = 1 for input task.  
 Device ID [8:15] = 00 000 000  
 Thus Output ID = 3000 (octal)  
 Input ID = 3400 (octal)

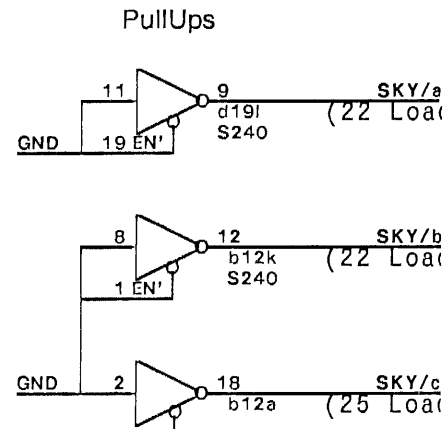
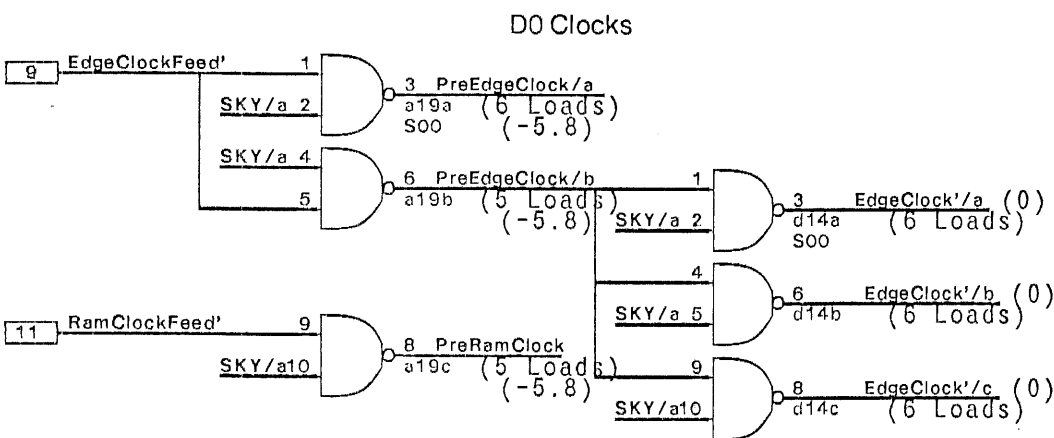
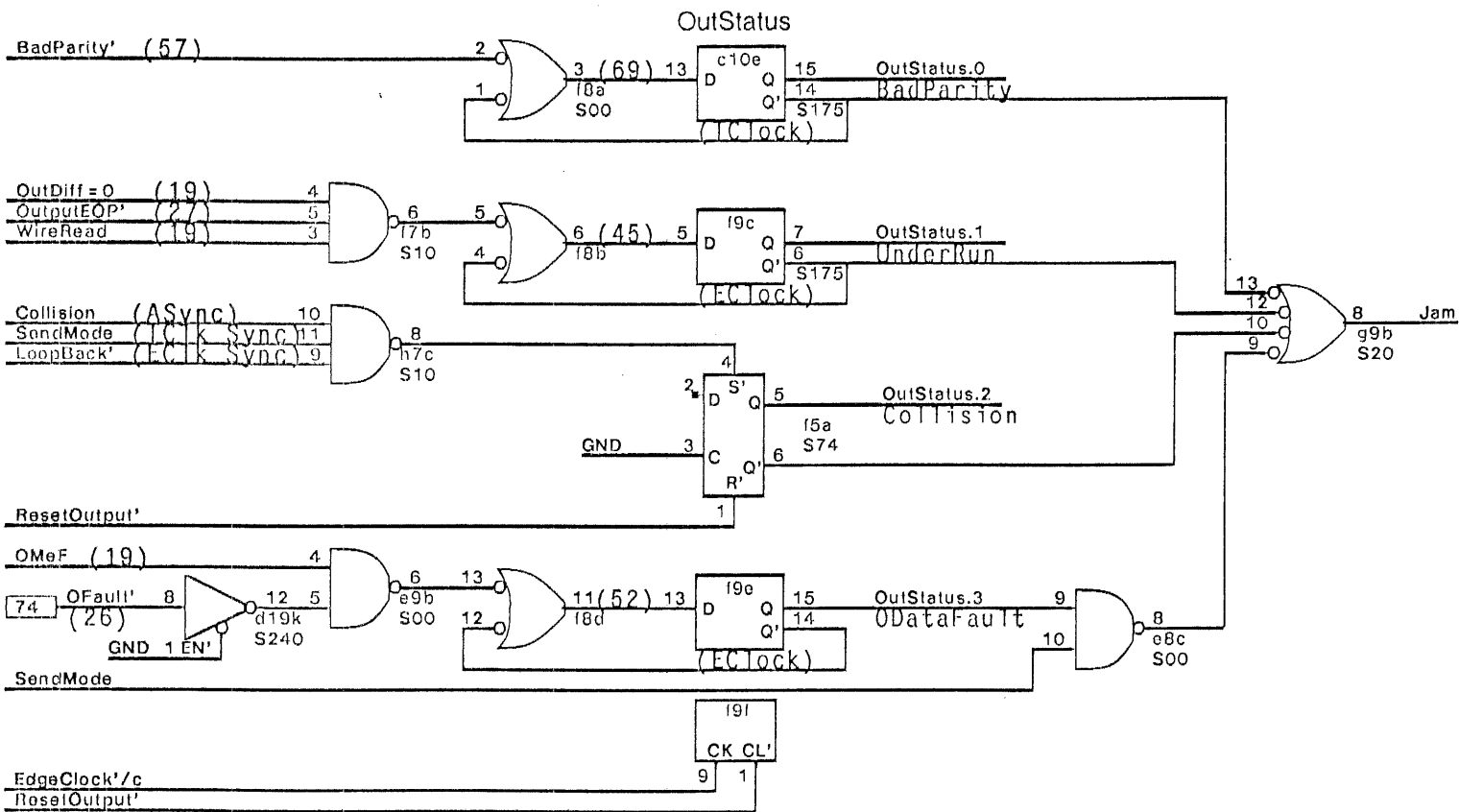
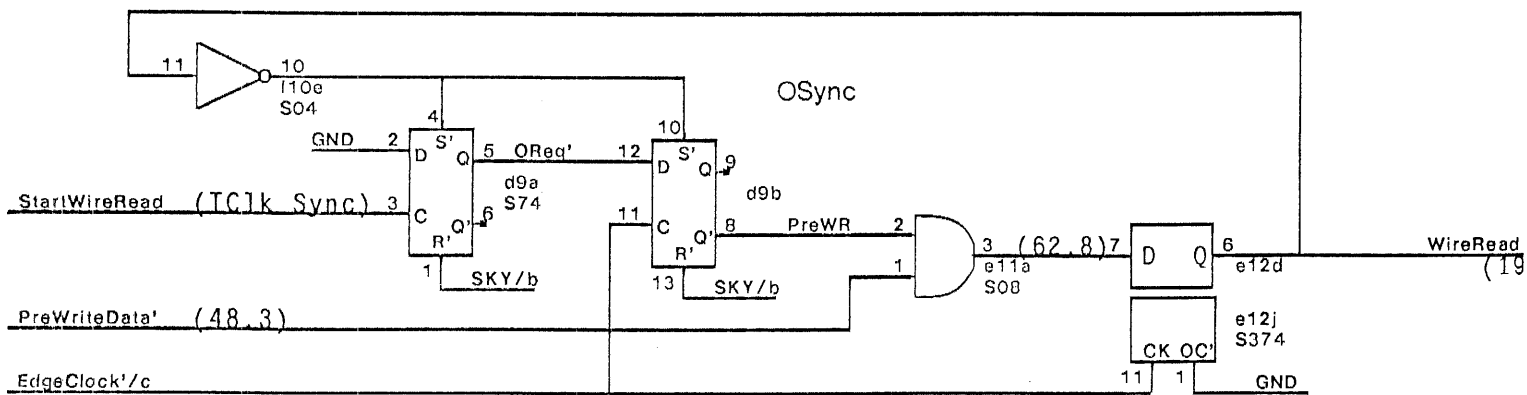
XEROX SDD	Project E Nel	DO Input Bus Drivers	File DOEN08.sil	Designer Garner, Ogus	Rev Ga	Date 4/13/79	Page 08
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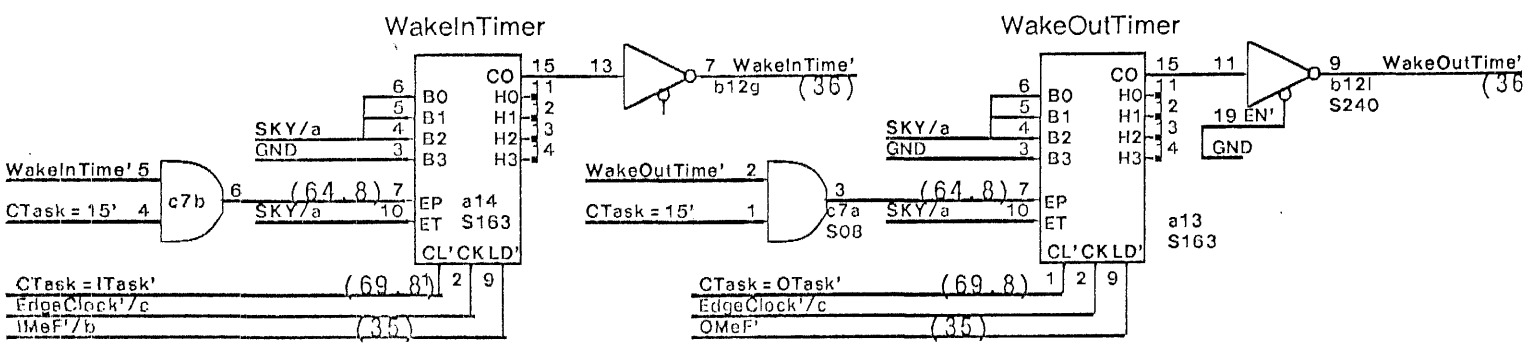
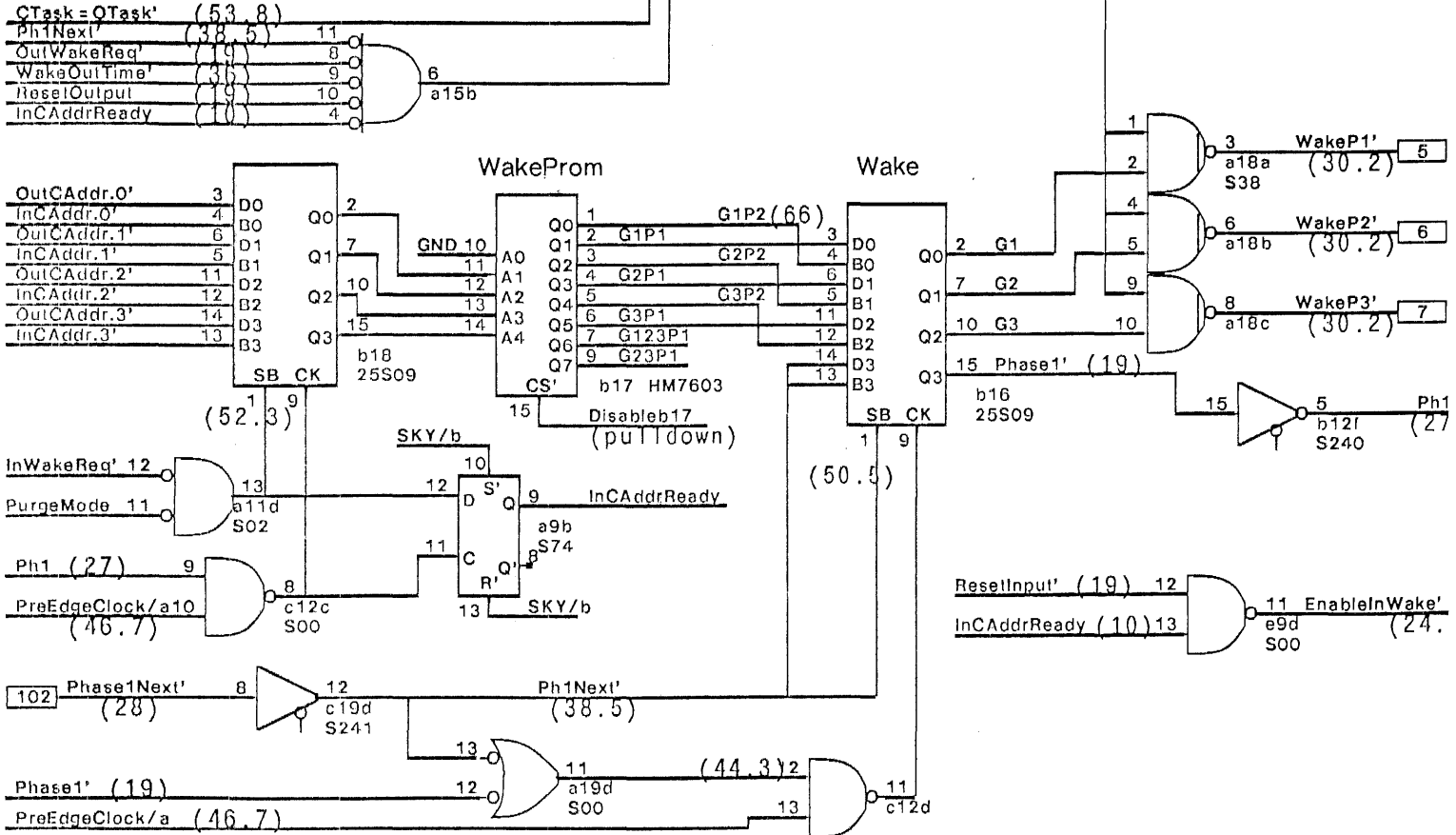
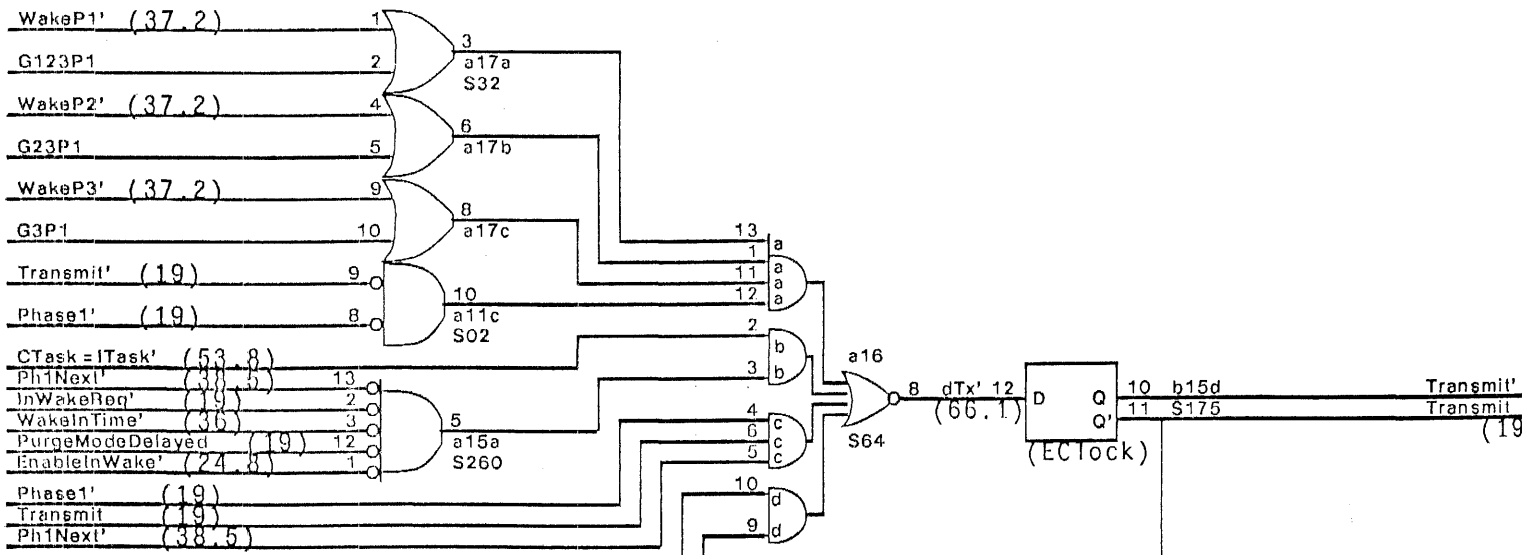


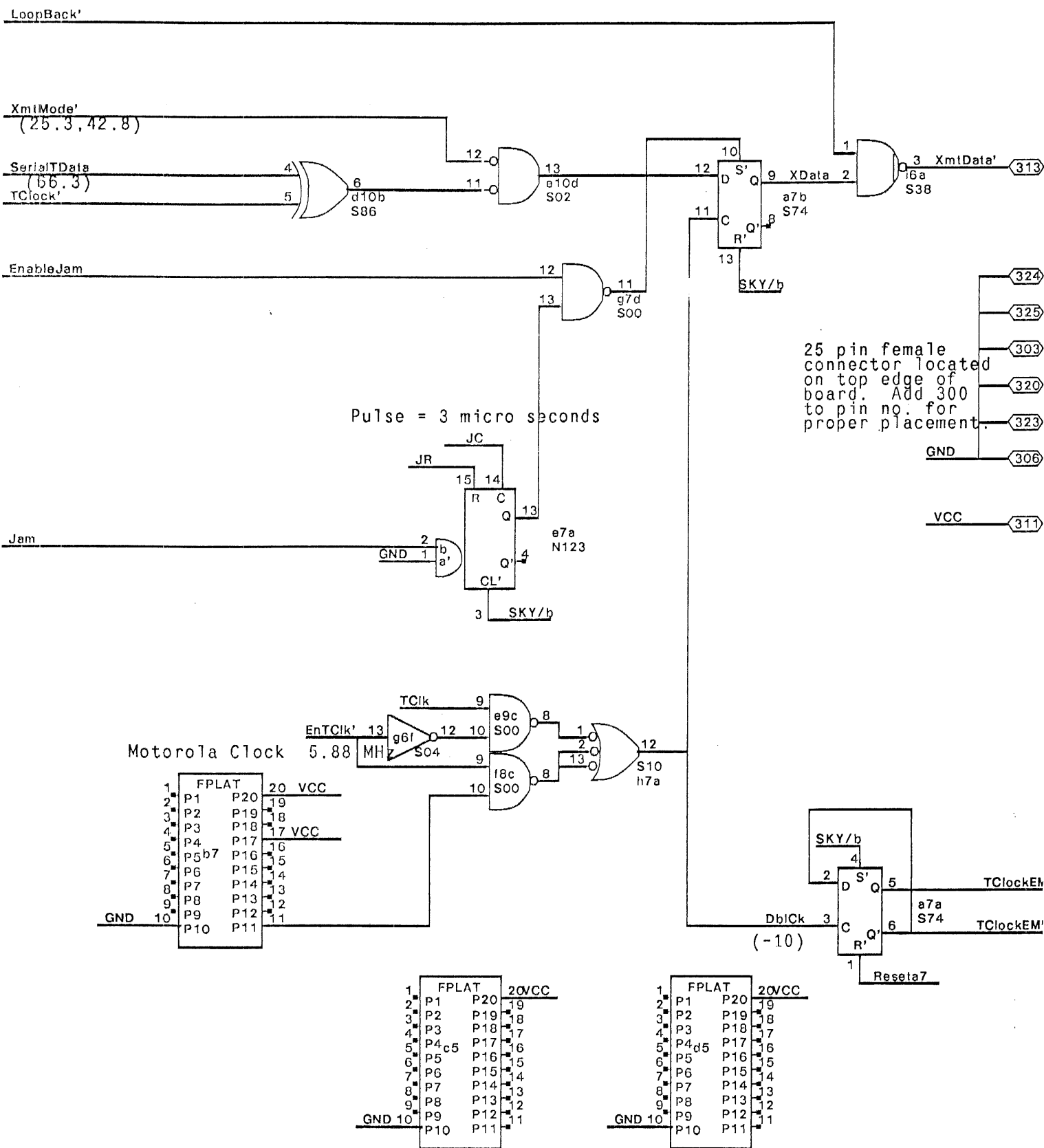




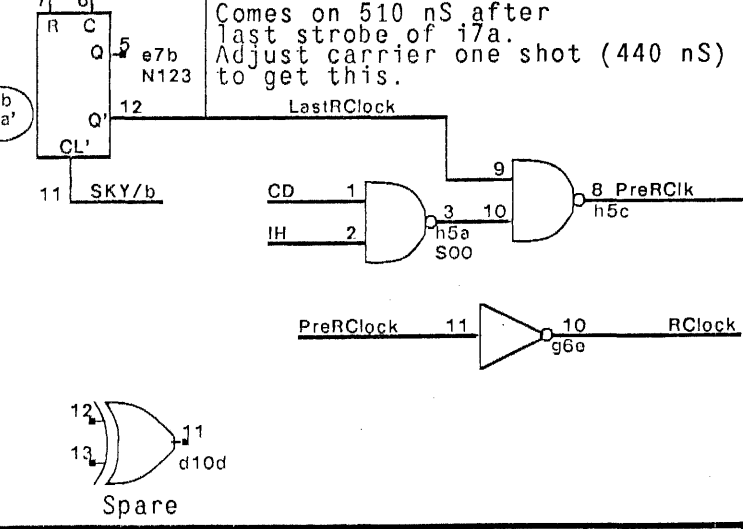
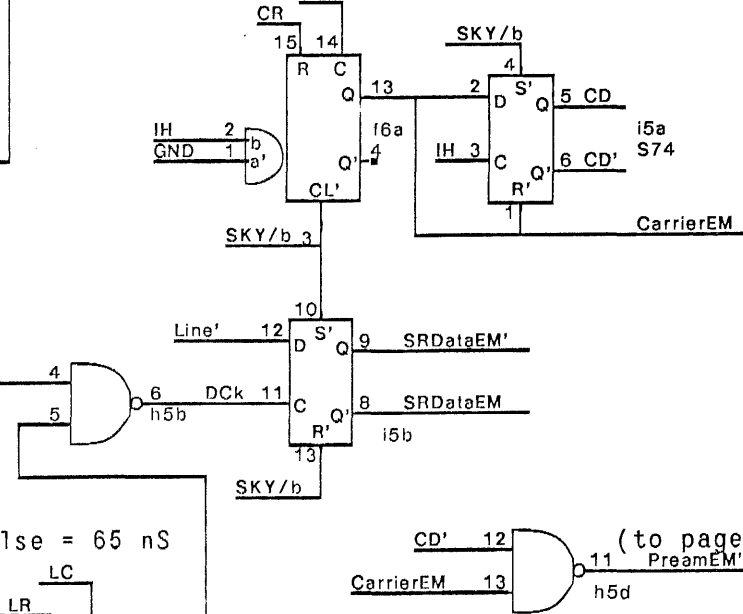
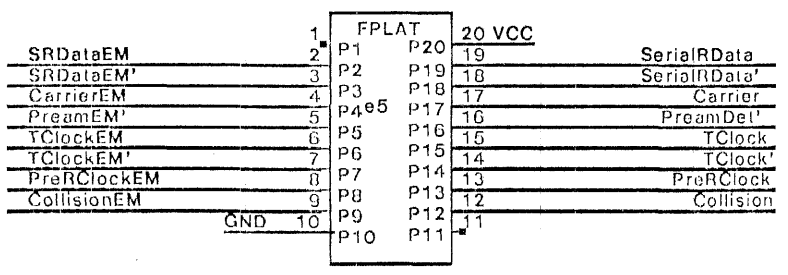
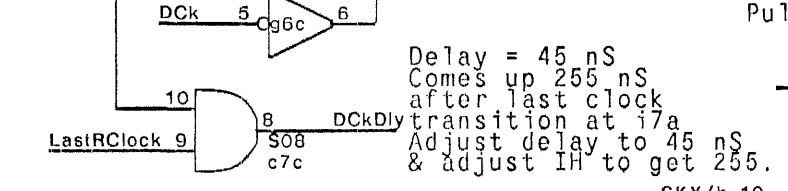
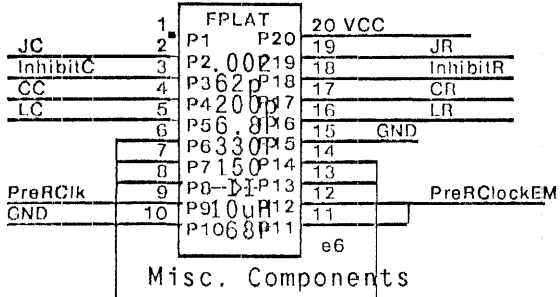
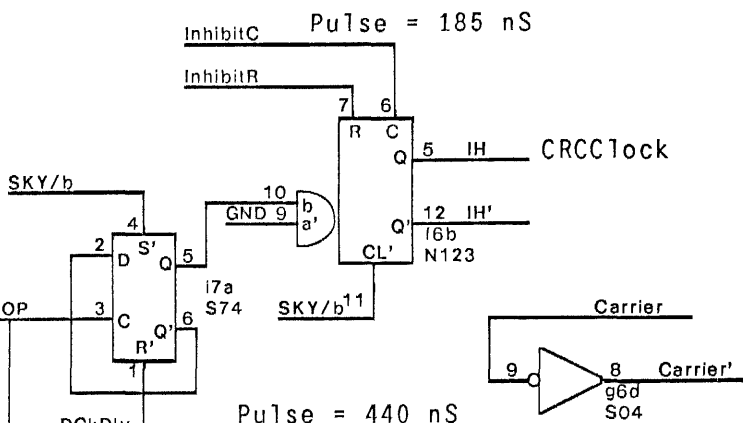
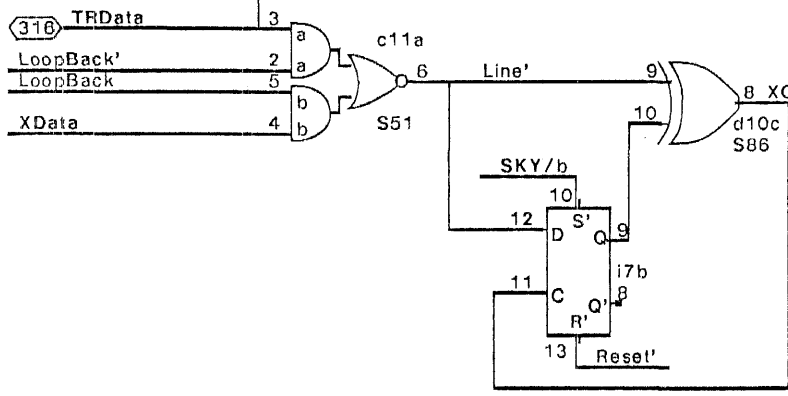
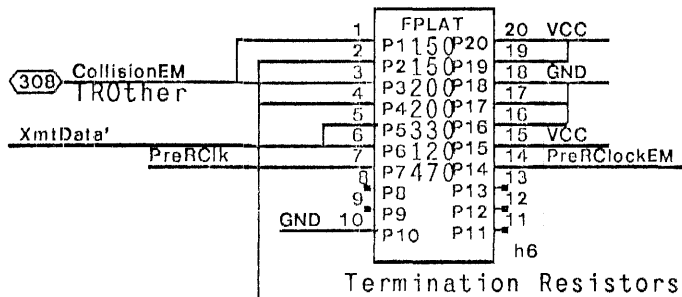


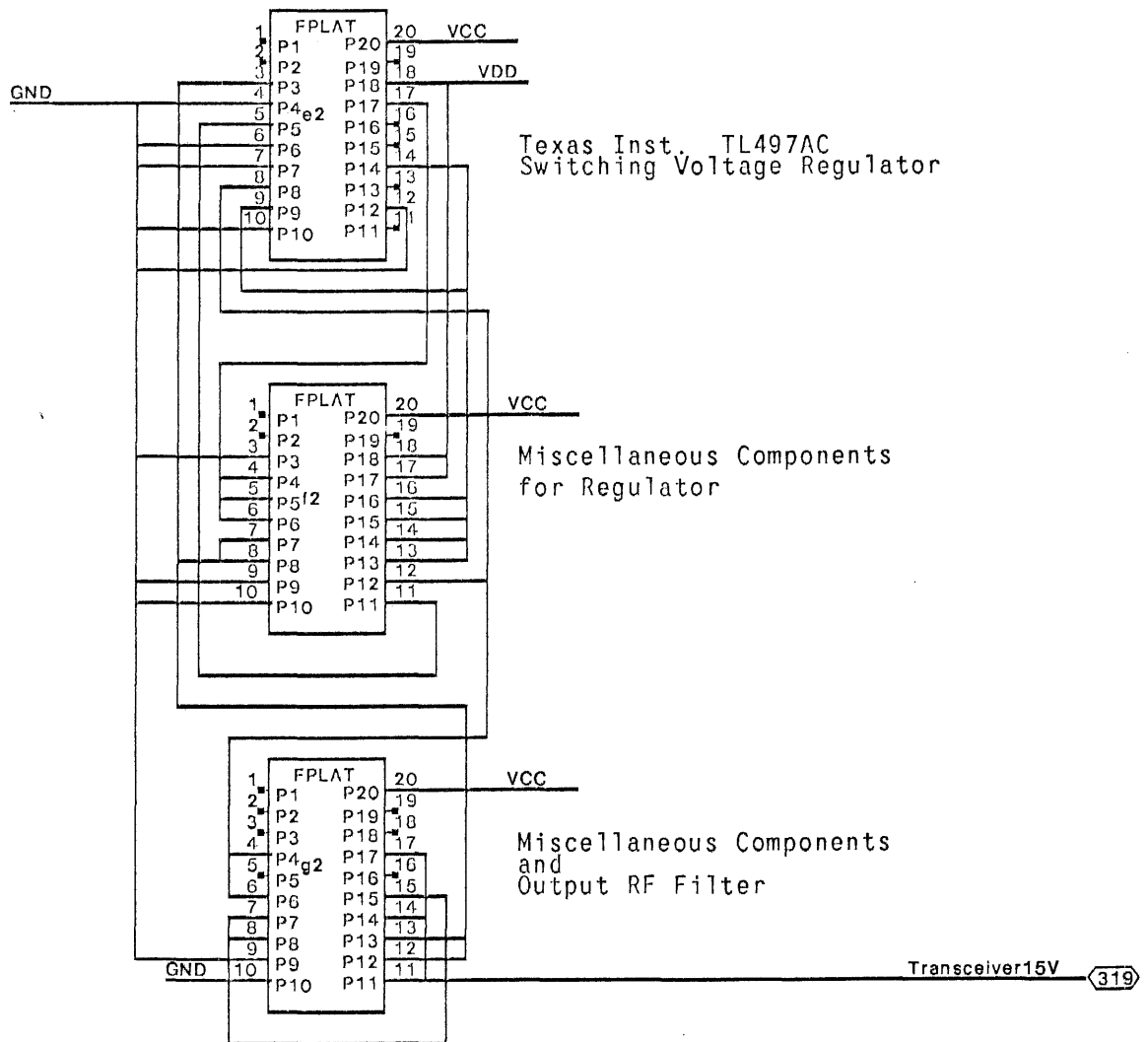




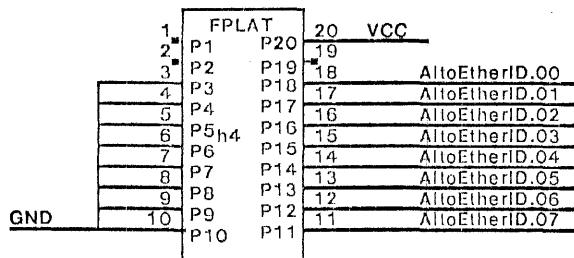


Spare package positions for PC board



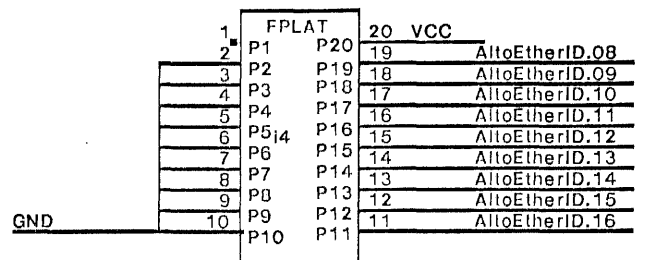


DIP Switches

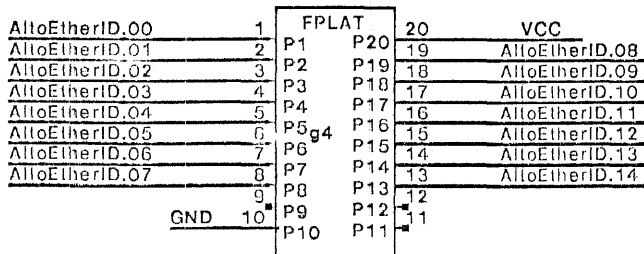


Set these switches to "ON" = logic 0.

DIP Switches

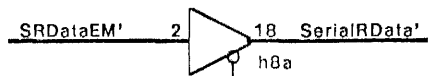
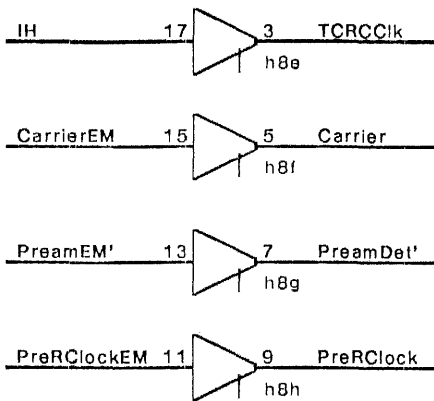


Set these switches to ID number and od  
P2 is MSB of ID number and P9 is LSB.  
Switch ON = 0  
Switch OFF = 1

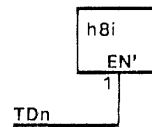
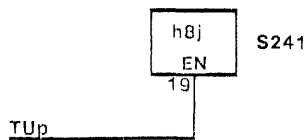
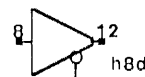


5.1K Pull-up Resistors

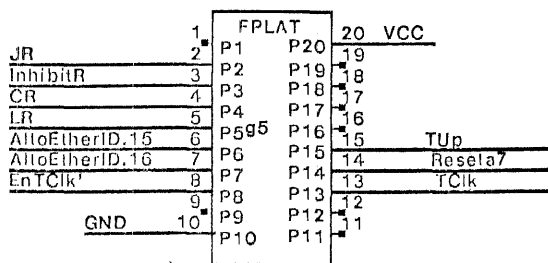




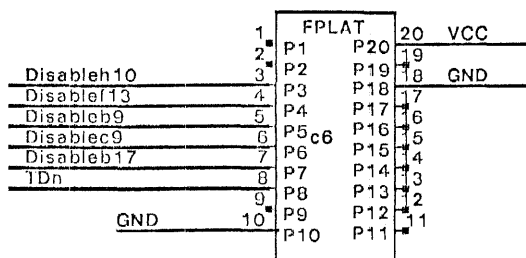
BadCRC on page 6



**Note:** When testing on the D0 Card tester, chip h8 (S241) must be removed as well as the jumper platform e5.



5.1K Pull-up Resistors  
16 pin package



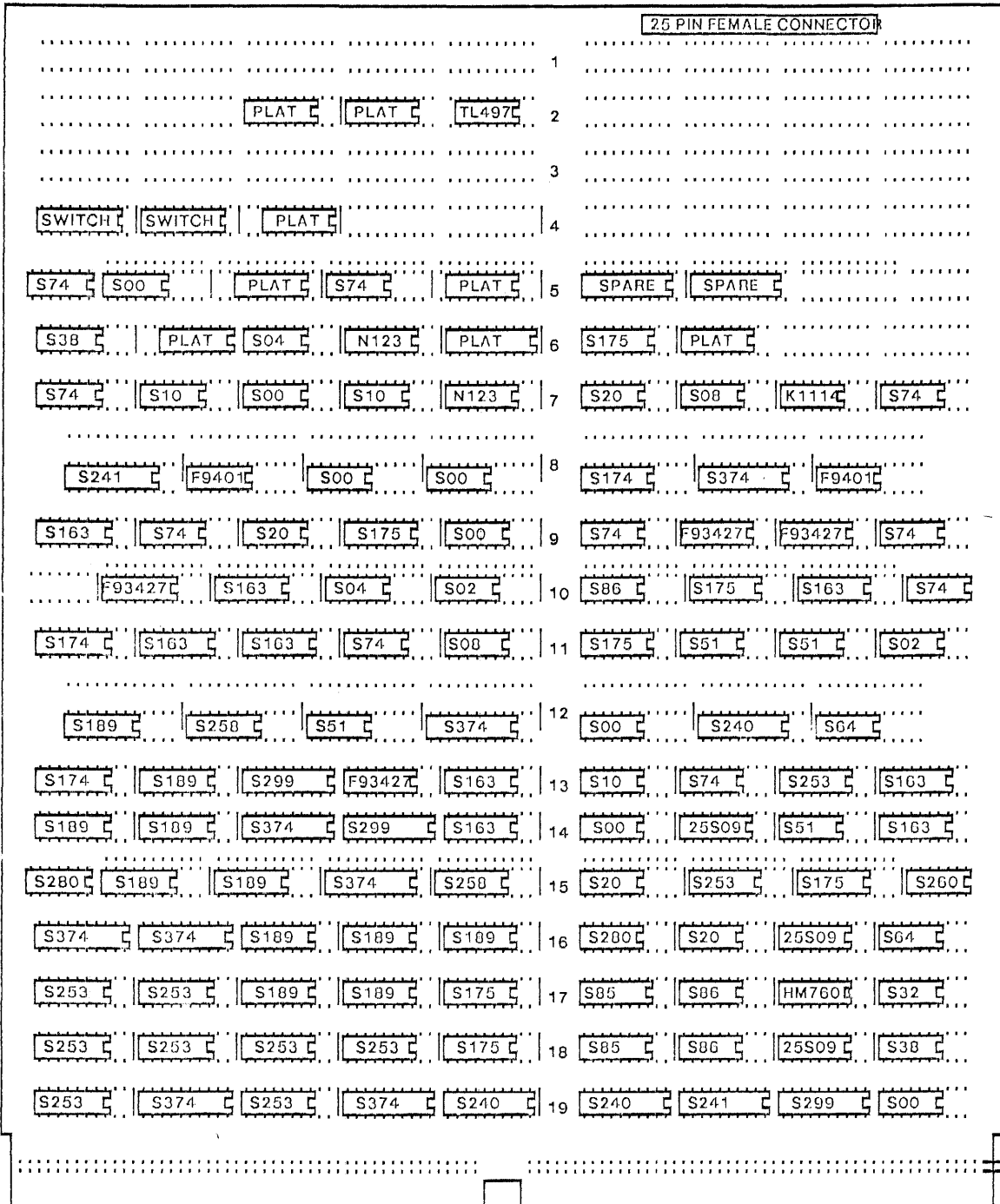
100 ohm pull down resistors  
16 pin package

Revision Ga generated from SDD revision N on 4/12/79 by CT.

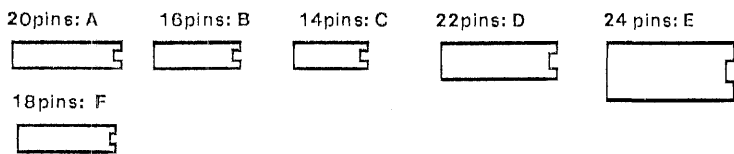
- 1) Renamed DOEn23.sil to DOEn17.sil
  - 2) Added standard files for platforms.
- The following were done to eliminate ROUTE trace cuts:
- 3) Added VCC to clock plat at b7 (p14).
  - 4) moved 470 ohm resistor from plat e6 (1-20) to h6 (7-14), and added VCC to e6 (p15).
  - 5) Coalesced all sections of plat g5 (pg15,16,17) to pg17.
  - 6) Added VCC & GND to plat e5 (pg15).
  - 7) Added GND to plat g4, VCC to h4,i4,g2,f2 (p16).
  - 8) Moved TL497C up one position in pattern e2, added VCC & GND (pg 16).
  - 9) Added VCC, GND to plats c6, g5 (pg 17).

XEROX CSL	Project E Net	Changes	File DOEnChanges.sil	Designer Crane	Rev Ga	Date 4/12/79	Page 1
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I H G F E D C B A



101-200  
1-100



Note: The short vertical lines indicate filter capacitor locations.

MATERIAL LIST

ML	Drawing No.	Rev. N
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Rev.	Drawing Title	<p>These drawings and specifications, and the data contained therein, are the exclusive property of Xerox Corporation and or Rank Xerox, Ltd. issued in strict confidence and shall not, without the prior written permission of Xerox Corporation Rank Xerox, Ltd., be reproduced, copied or used for any purpose whatsoever, except the manufacture of articles for Xerox Corporation or Rank Xerox, Ltd.</p>			
Dwg. No.	<p>D0 Ethernet Controller          (DOENPLO1.sil)          EMS VERSION</p>				
		<table border="1"> <tr> <td>Model No.</td> <td>Date 4/13/79</td> <td>Sheet 1 of 3</td> </tr> </table>	Model No.	Date 4/13/79	Sheet 1 of 3
Model No.	Date 4/13/79	Sheet 1 of 3			

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
	Integrated Circuit	SN74S00	8	
		SN74S02	2	
ML		SN74S04	2	
		SN74S08	2	
		SN74S10	3	
		SN74S20	4	
		SN74S32	1	
		SN74S38	2	
		SN74S51	4	
		SN74S64	2	
		SN74S74	10	
		SN74S85	2	
		SN74S86	3	
	SN74123 TI only		2	This is timing component. Use only Texas Instruments
		SN74S163	9	
		SN74S174	3	
		SN74S175	7	
		SN74S189	11	
		SN74S240	3	
		SN74S241	2	
		SN74S253	10	
		SN74S258	2	
		SN74S260	1	
		SN74S280	2	
		SN74S299	3	
		SN74S374	8	
		AM25S09	3	
	F93427 PROM		4	Bit patterns detailed in Prom listings
	F9401		2	
	Integrated Circuit	HM7603-5 PROM	1	Bit Pattern detailed in Prom listings

ML	Drawing No.	Rev. N
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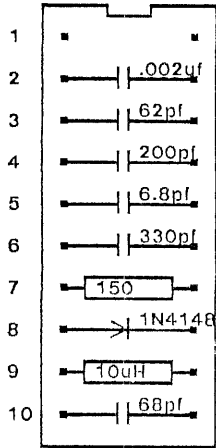
MATERIAL LIST

Rev.	Drawing Title		<p>These drawings and specifications, and the data contained therein, are the exclusive property of Xerox Corporation and or Rank Xerox, Ltd. issued in strict confidence and shall not, without the prior written permission of Xerox Corporation Rank Xerox, Ltd., be reproduced, copied or used for any purpose whatsoever, except the manufacture of articles for Xerox Corporation or Rank Xerox, Ltd.</p>		
Dwg. No.	<p>D0 Ethernet Controller (D0ENPL02.sil) EMS VERSION</p>				
	Model No.	Date	Sheet		
		4/13/79	2 of 3		
Item No.	Drawing Title	Drawing No.	No. Req.	Remarks	
	Integrated Circuit Texas Inst. TL497AC		1	e2	
	Clock package (14 pin) Motorola K1114A or equiv. Clock Frequency = 5.88 MHz		1	b7	
ML	Timing Capacitors NPO Temperature 5% Coefficient	6.8 pF 10V	1	e6 Corning CAC02COG 6R8	
		62 pF 10V	1	e6 Corning CAC02COG 620	
		200 pF 10V	1	e6 Corning CAC02COG 201	
		330 pF 10V	1	e6 Corning CAC02COG 331	
		.002 10V	1	e6 Corning CAC03COG 202	
	Capacitor 10%	10 pF 25V	1	f2	
	Capacitor 10%	68 pF 25V	2	f2 , e6	
	Capacitor 10%	.1 uF 25V	1	g2	
	Capacitor, Tantalum Electrolytic	10 uF 25V	5	f2, g2 2 of these are for board filter caps.	
	Diode	1N4148	2	e6, f2	
	Inductor, non-ferrous core (Nytronics SWD-68)	68 uH 4 ohms or less DC resistance	1	g2 Inductor must not saturate @ 100 mA	
	Inductor, non-ferrous core (Miller 70F254AI)	220 uH 10 ohms or less 250 uH DC resistance	1	f2 Inductor must not saturate @ 300 mA	
	Carbon Composition Resistor .25 Watt 5%	120 ohms	1	h6	
		150 ohms	2	h6	
		200 ohms	2	h6	
		330 ohms	1	h6	
		1K ohm	1	f2	
	Resistor .5 Watt 5%	2.2 ohm	1	f2 Allen Bradley RC20GF2R2J	
	Resistor .25 Watt 1%	150 ohms	1	e6 Allen Bradley RN55D 1500F	
		499 ohm	1	g2 Allen Bradley RN55D 4990F	
		1.21 K ohm	1	g2 Allen Bradley RN55D 1211F	
		13.3 K ohm	1	g2 Allen Bradley RN55D 1332F	
	Resistor Network 16 pin 15 pullup resistors (Allen Bradley 316A512 or equiv.)	5.1K 2%	2	g4 g5 These resistors are used for timing.	
	Resistor Network 16 pin 15 pullup resistors (Allen Bradley 316A101 or equiv.)	100 ohm	1	c6	
	DIP Switch Package 9 SPST switches, 18 pin package		2	h4, i4 CTS 206-9	
	16 pin DIP platform		4	e5, f2, g2, h6 Augat 616-DG5	
	25 pin female D connector (DB25-S) with right angle printed circuit board mount		1	AMP 206584-1	
	Locking posts, nuts, & washers for D Connector (available from Cannon)		2	Cannon D53018	



Platform e6:

Capacitors are 5%, NPO T.C.



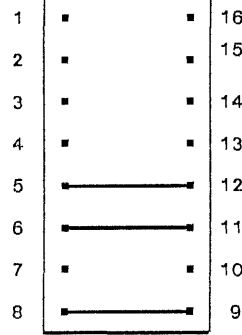
One-shot times:

R	T	Function
5.1k	3uS	Jam
5.1k	185nS	Inhibit
5.1k	440nS	Carrier
5.1k	65nS	LastRClock

Part of 45nS delay. Resistor is 1%

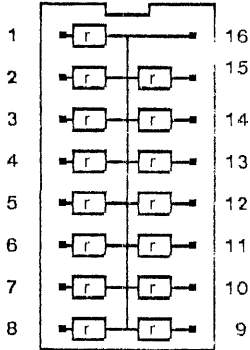
Platform e5:

Jumpers



Platform c6:

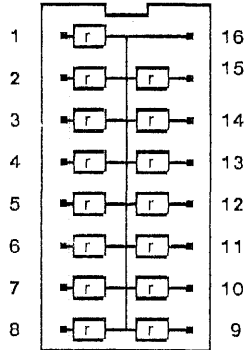
r = 100 ohm  
Allen-Bradley 316A101



Platform g4,

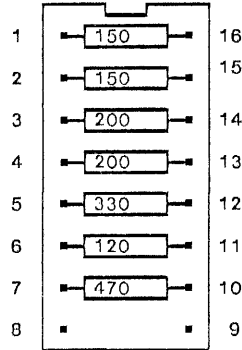
Platform g5:

r = 5.1k, 2%  
Allen-Bradley 316A512



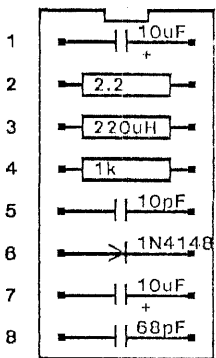
Platform h6:

Termination resistors  
.25 W, 10%



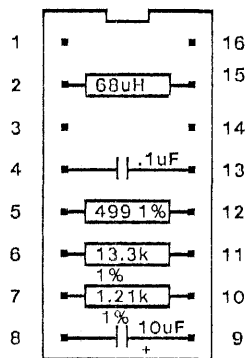
Platform f2:

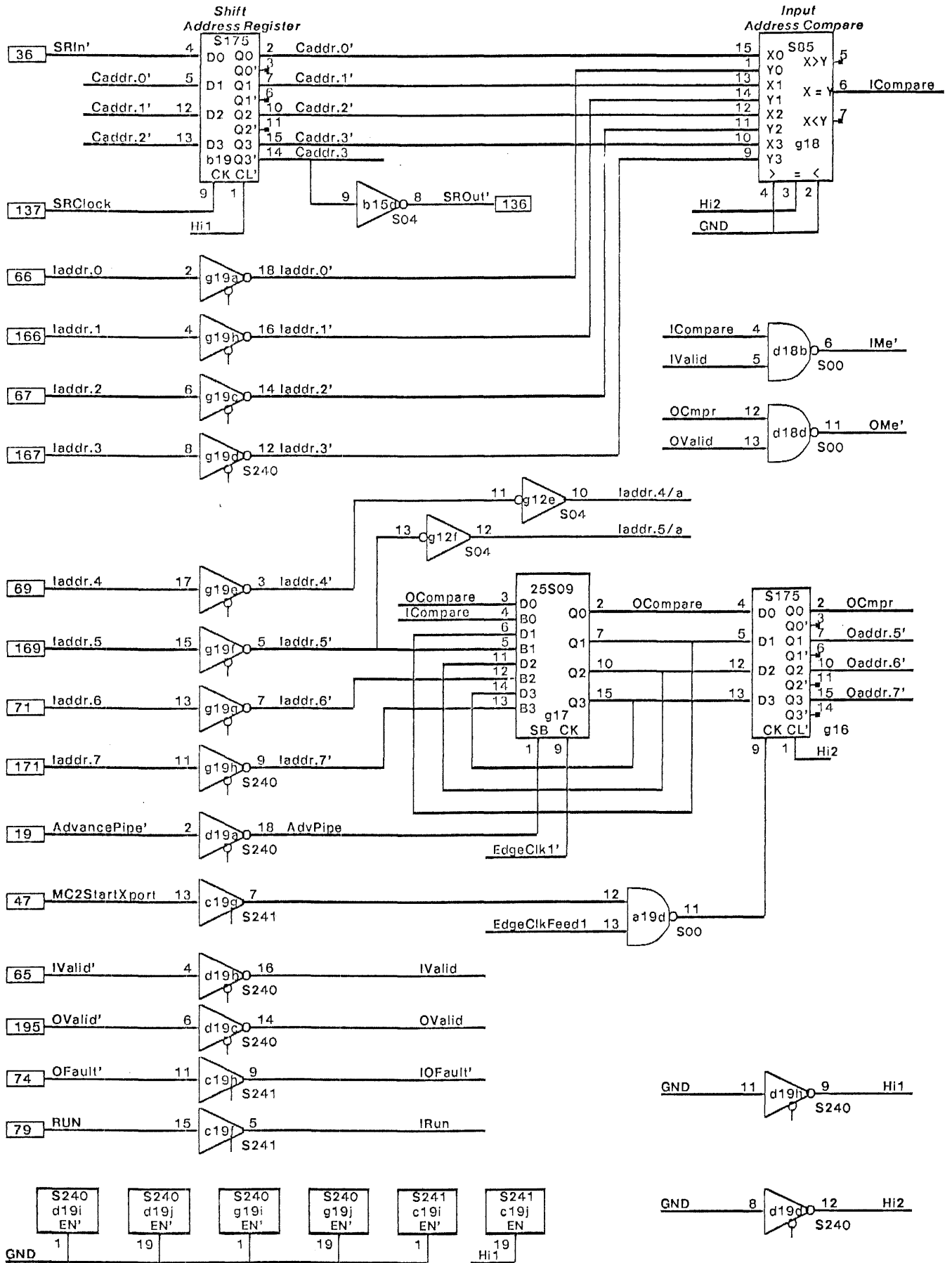
Regulator components



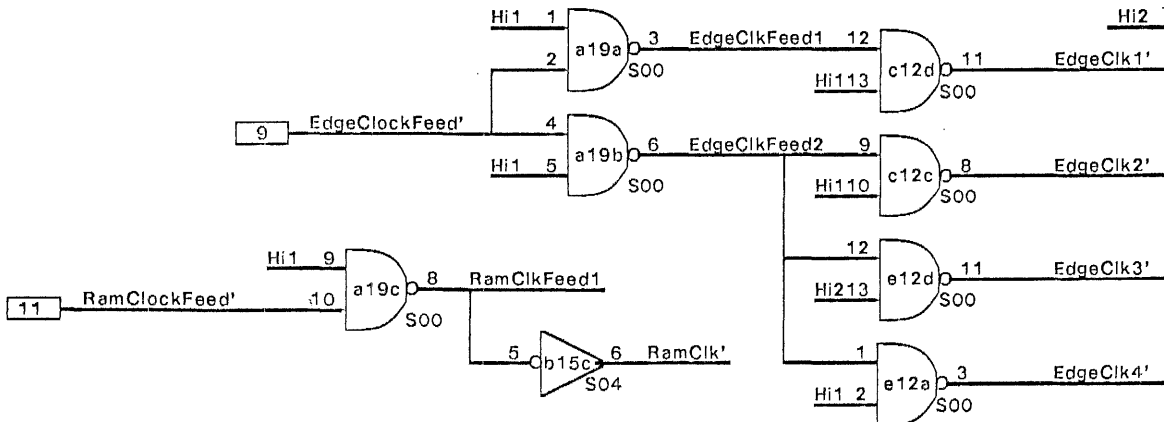
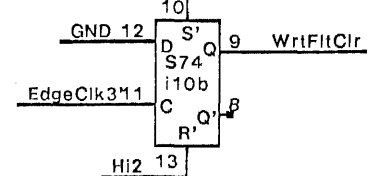
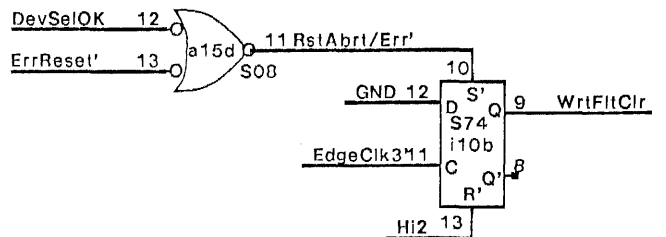
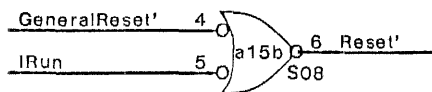
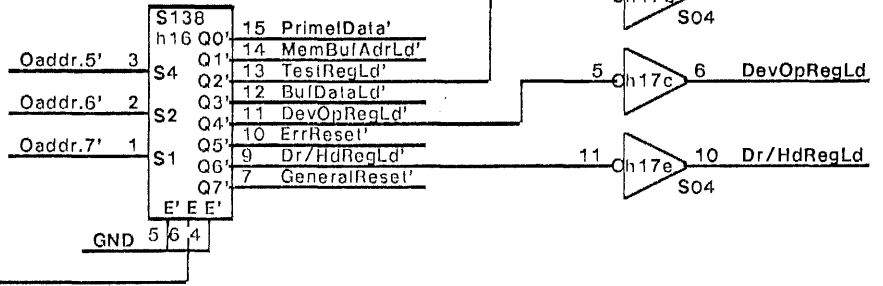
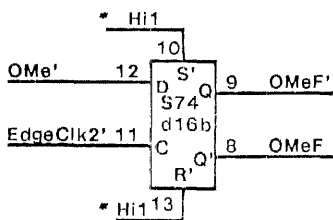
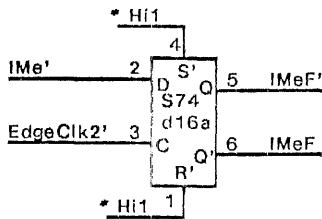
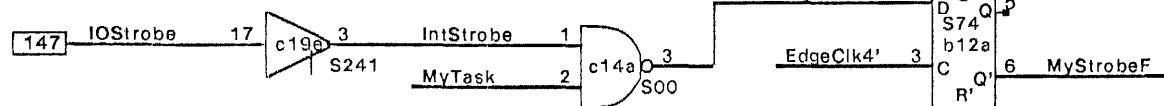
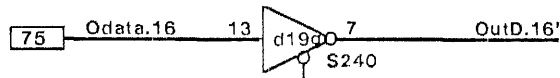
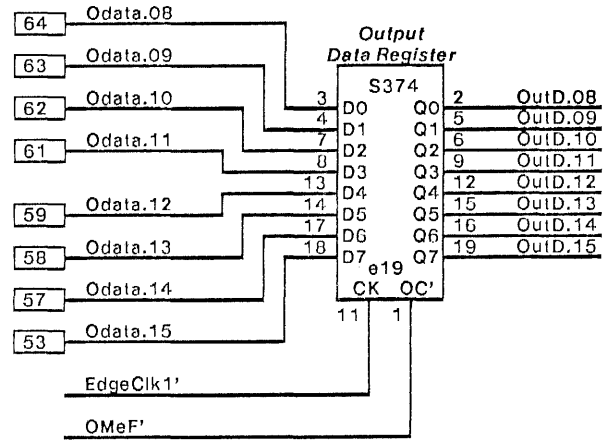
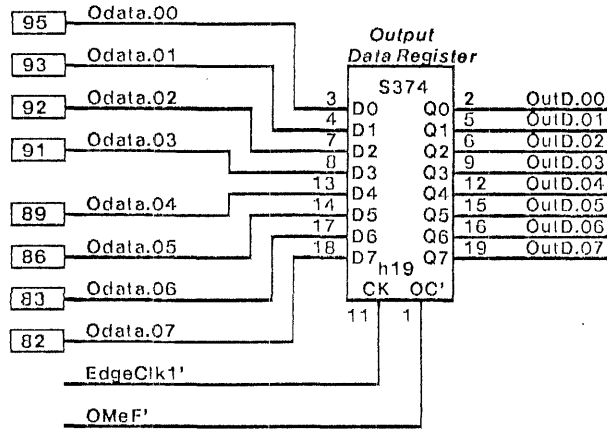
Platform g2:

More regulator



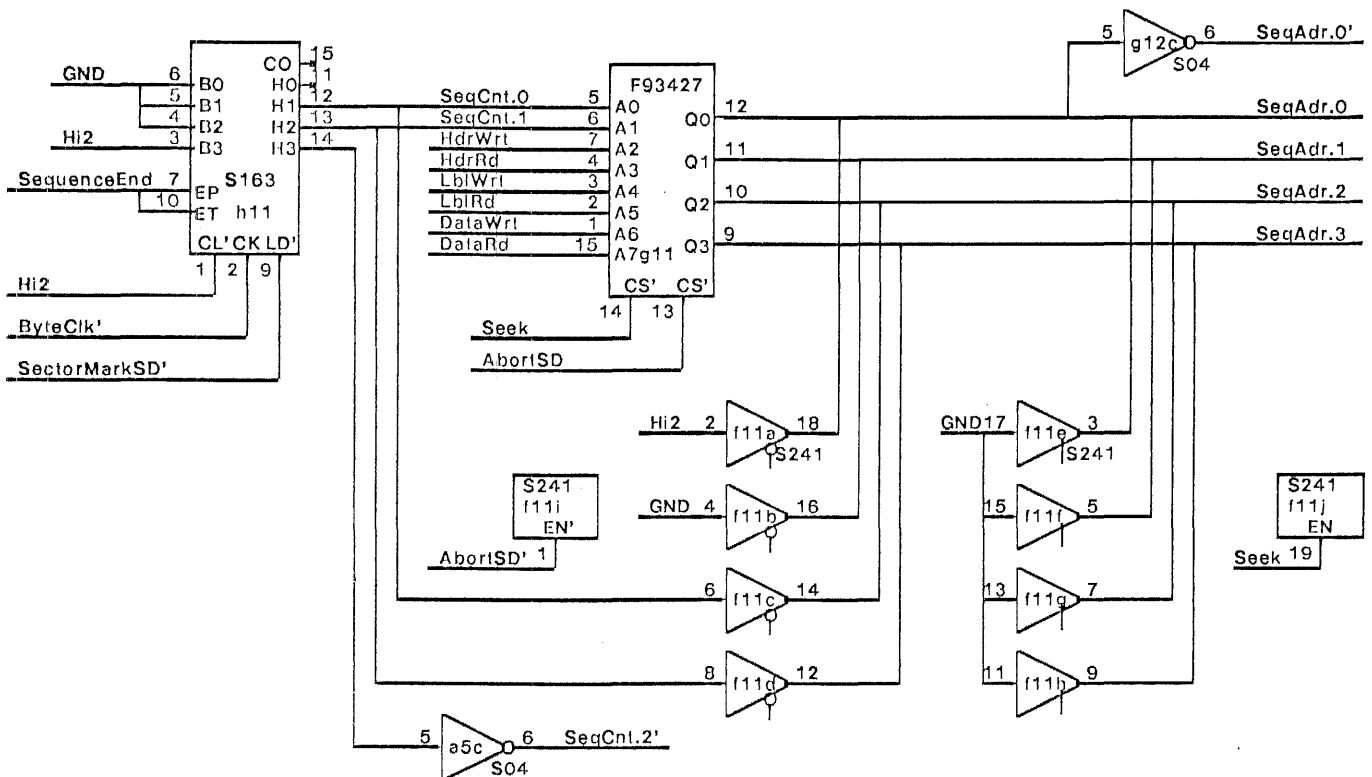
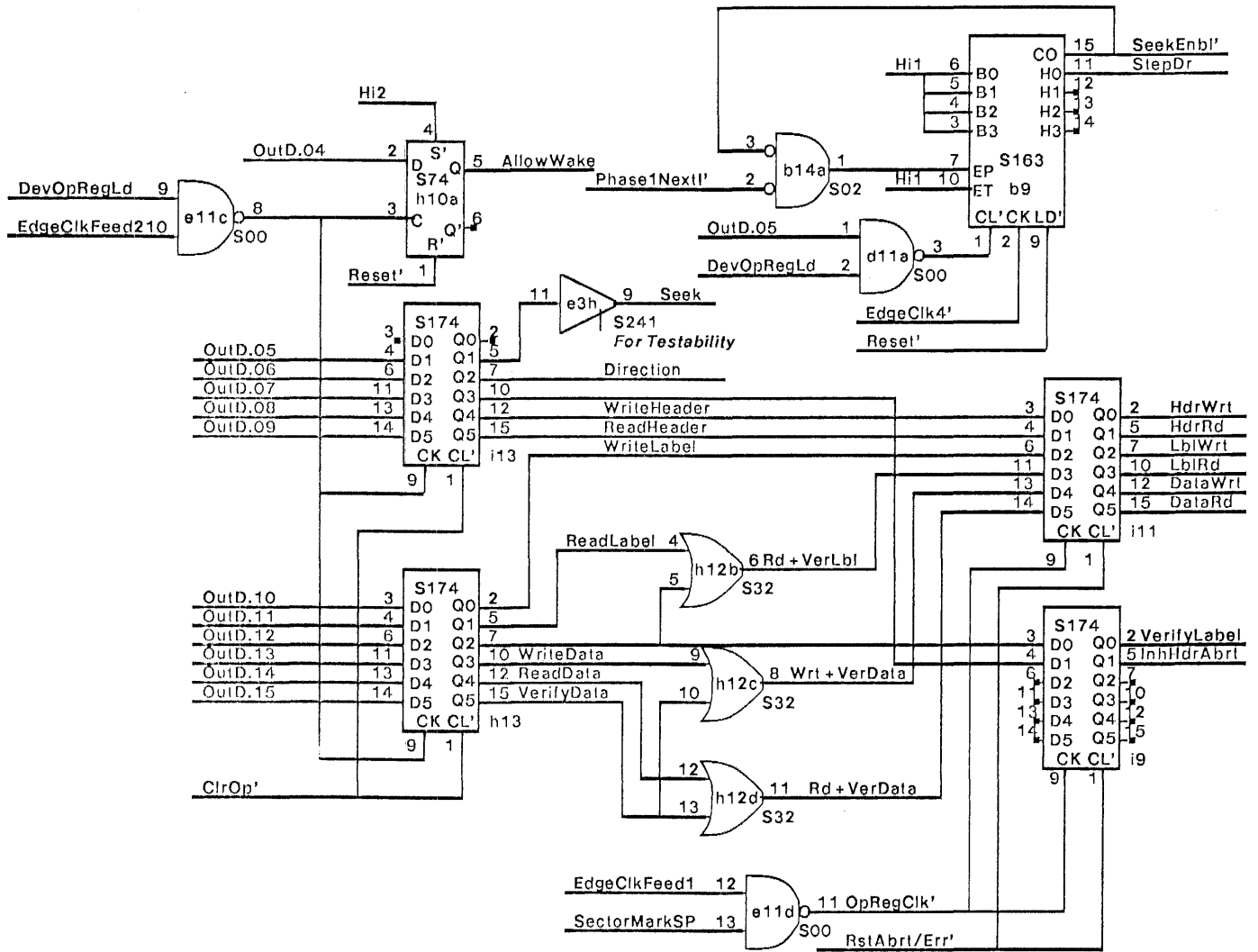


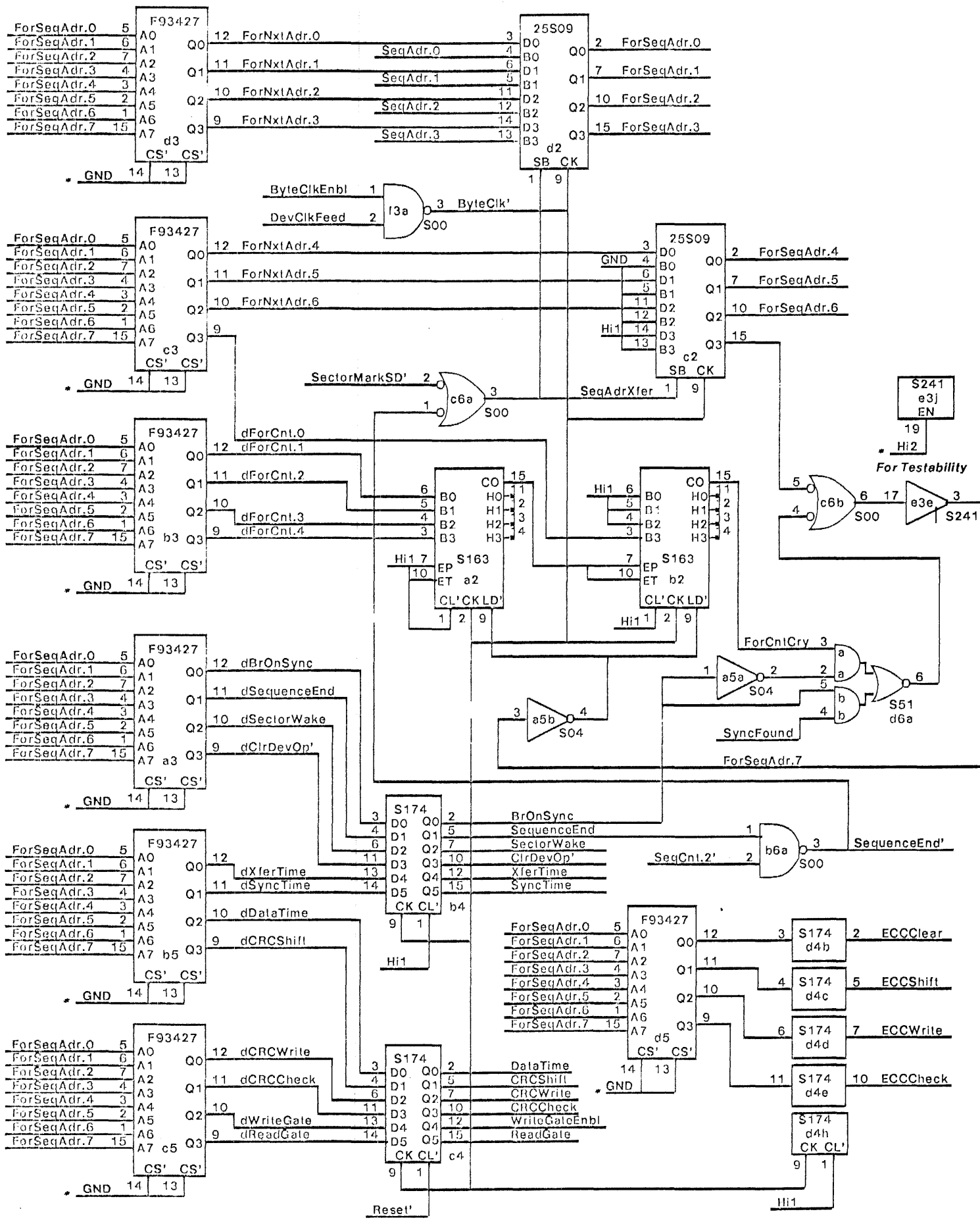




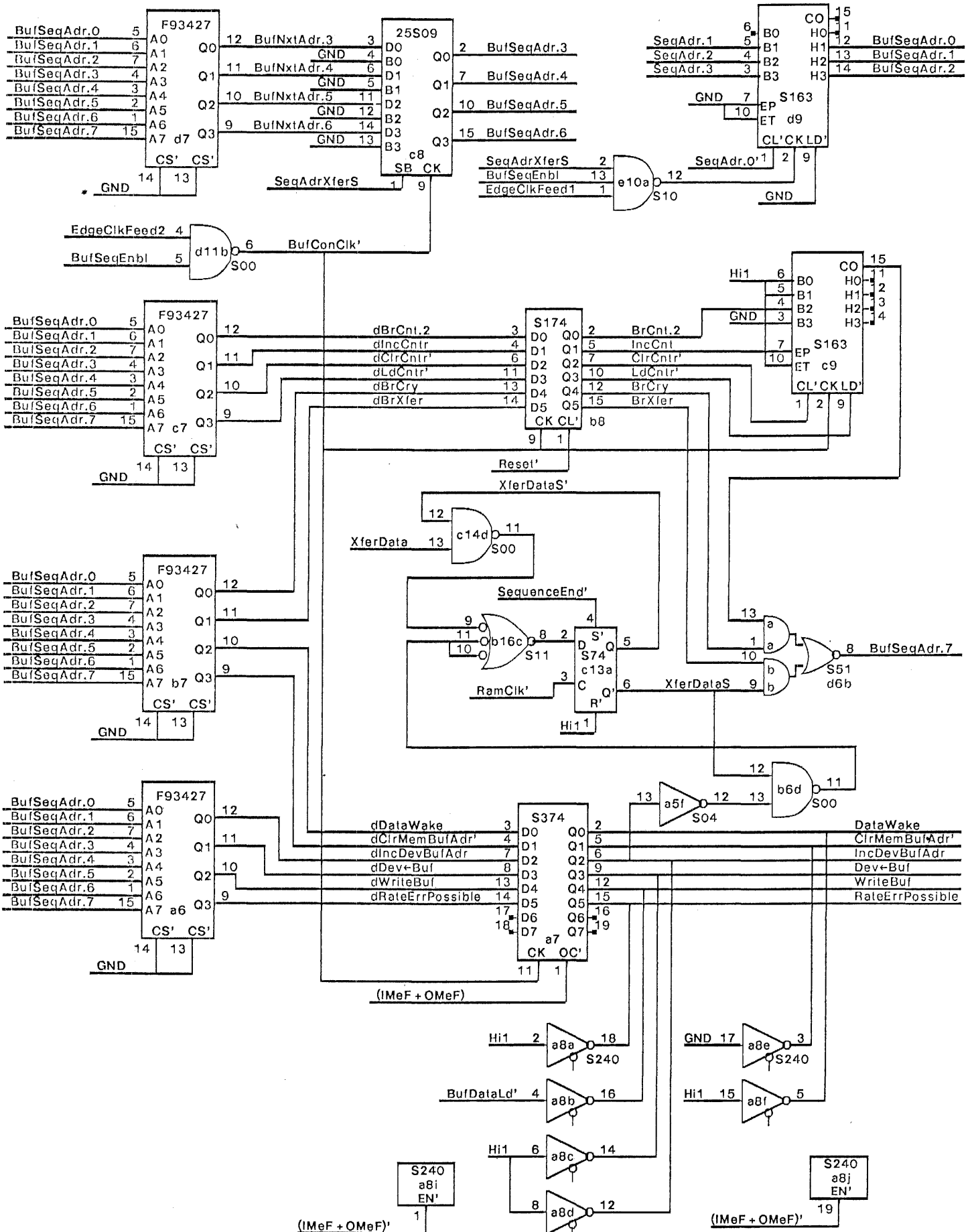
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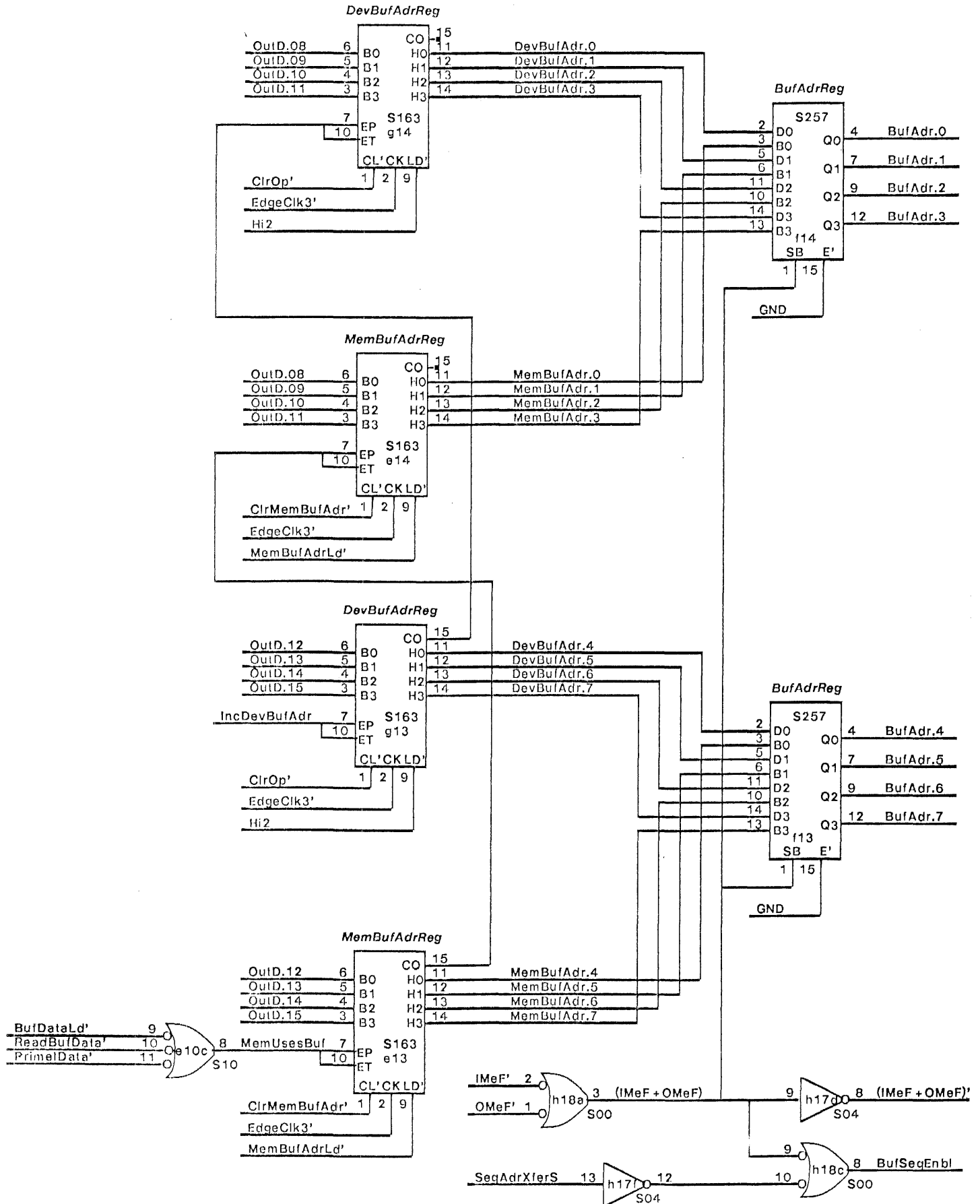




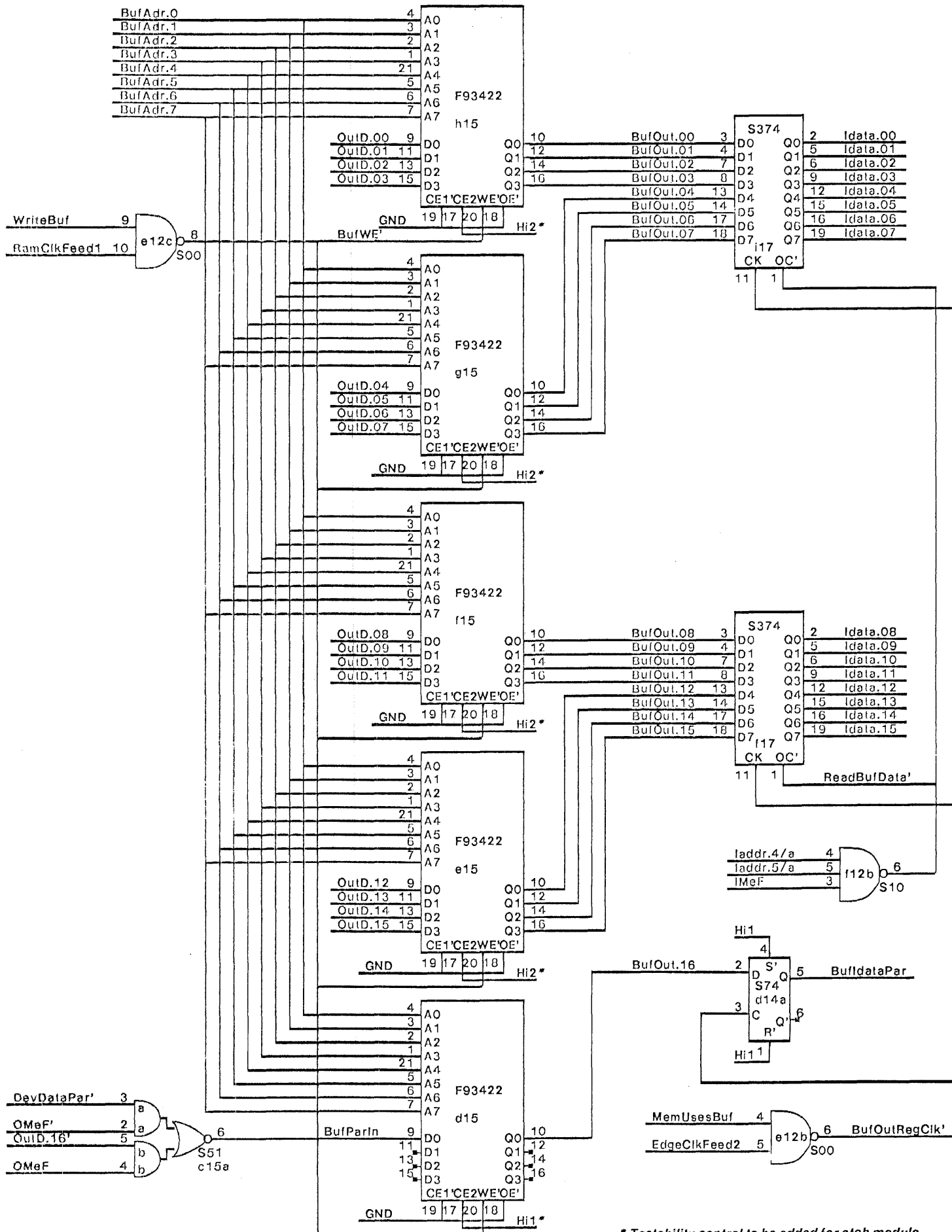
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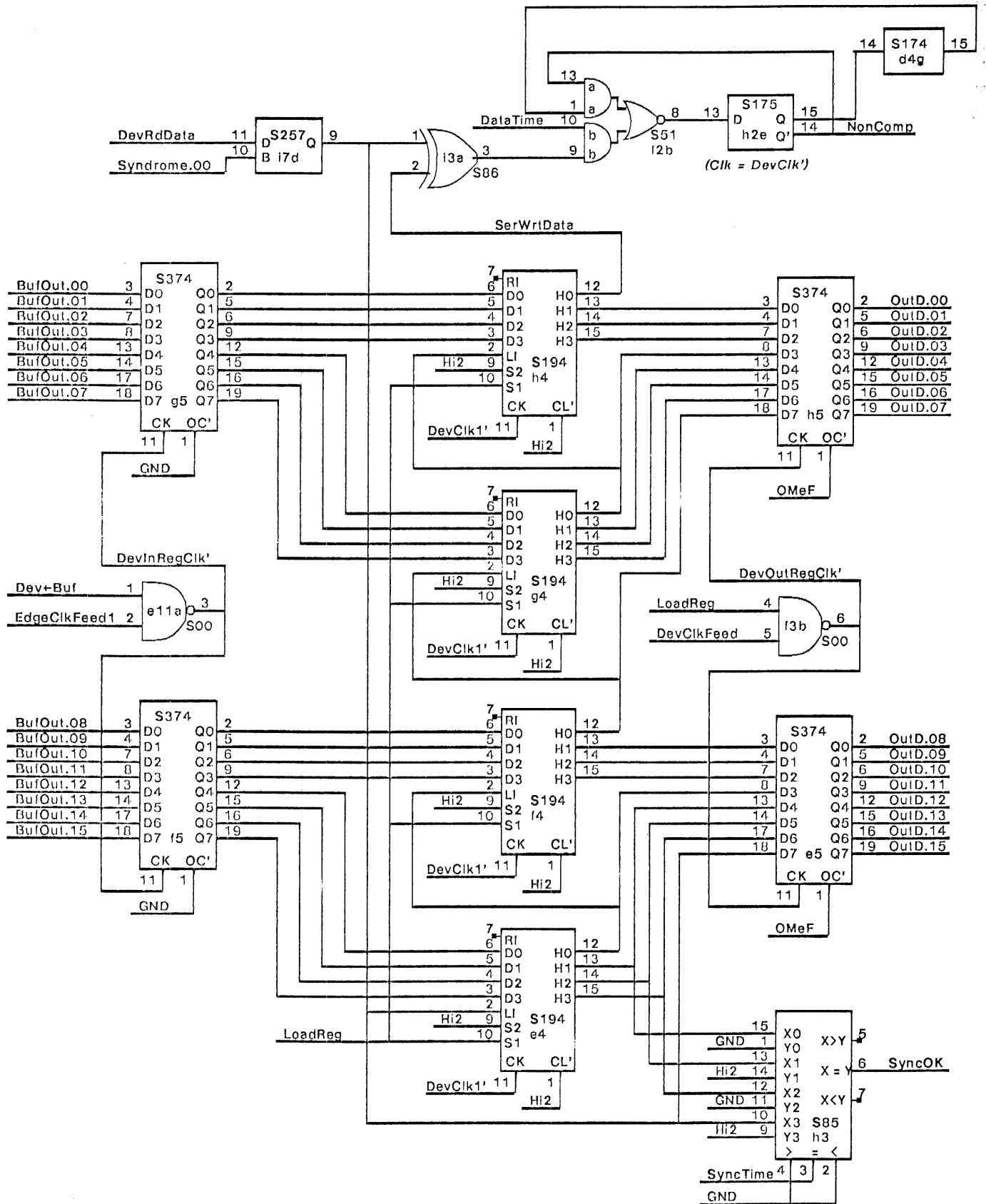
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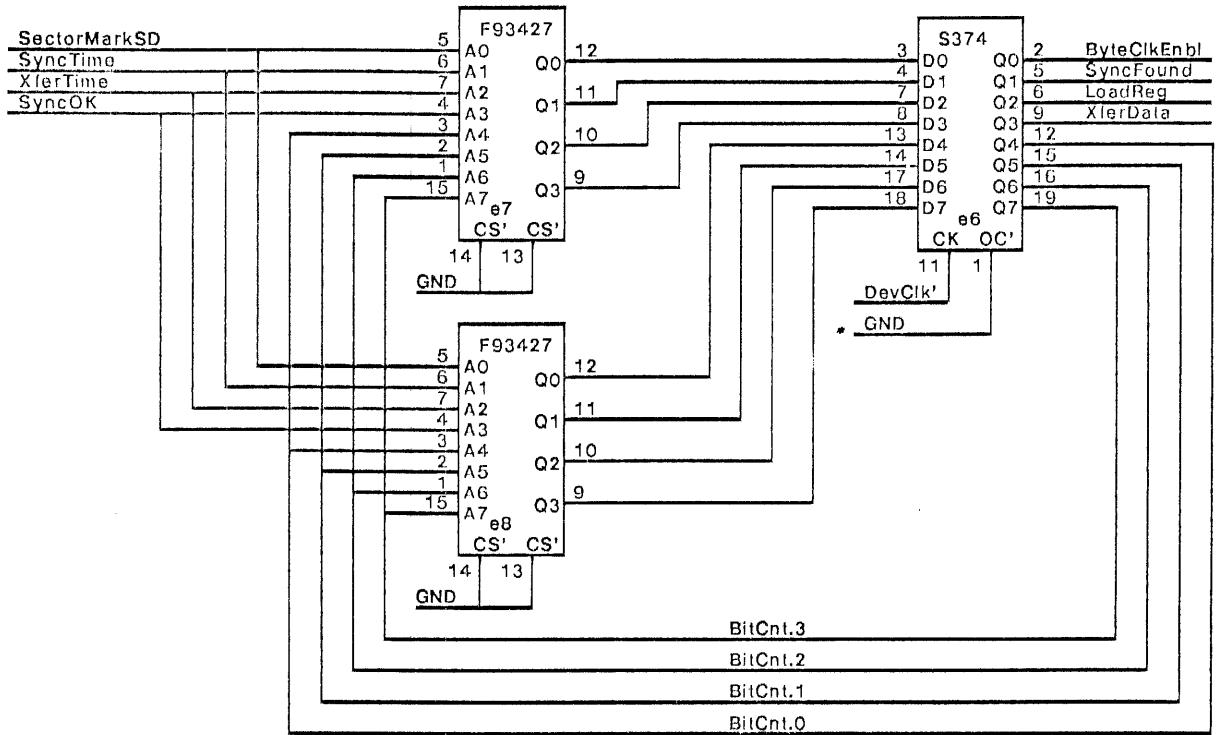
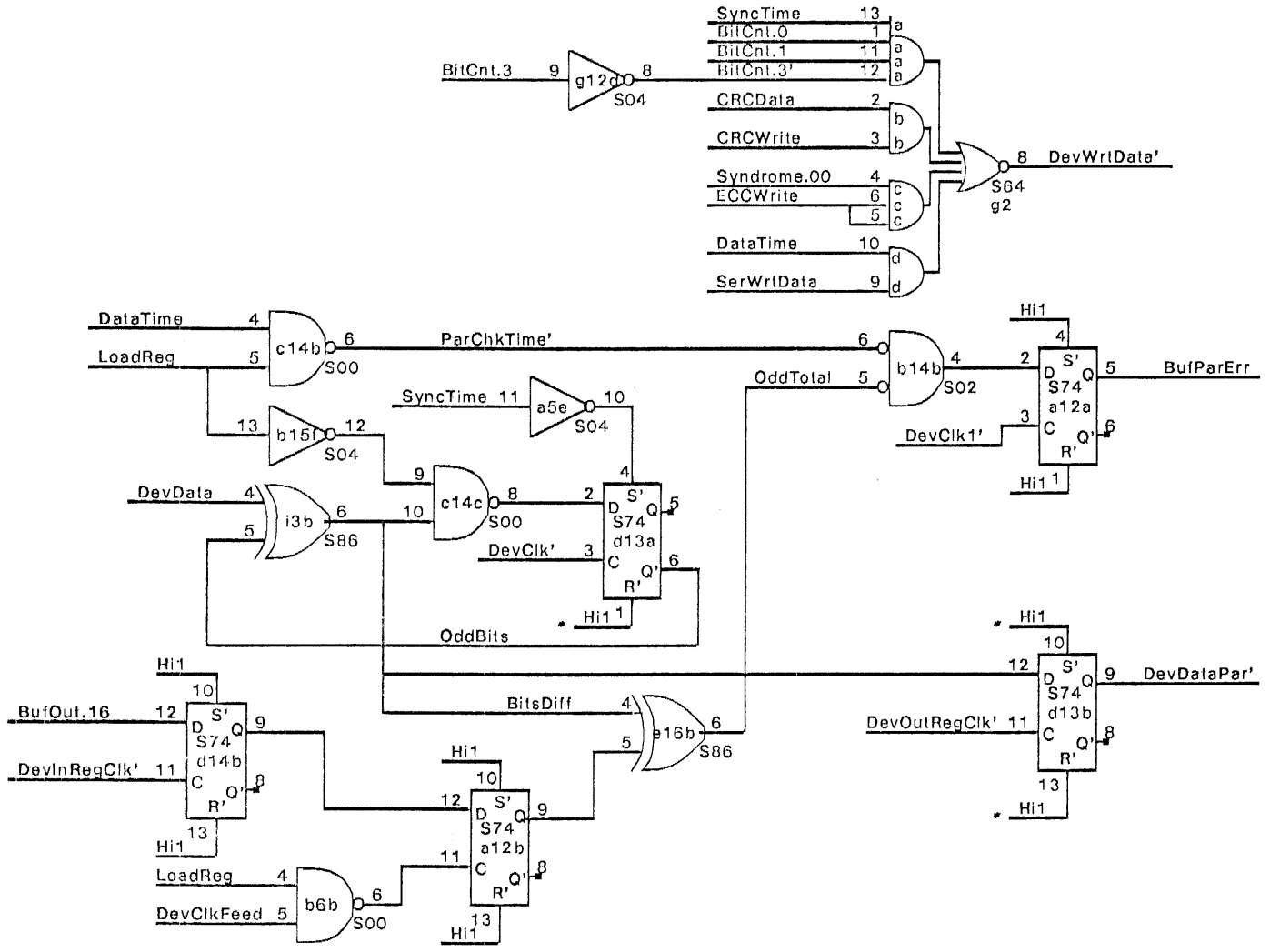
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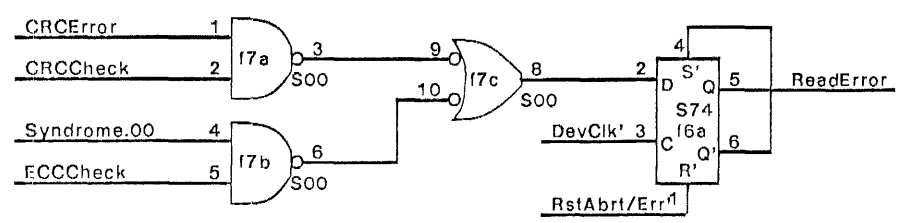
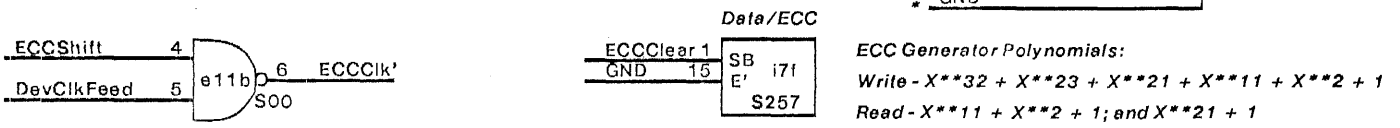
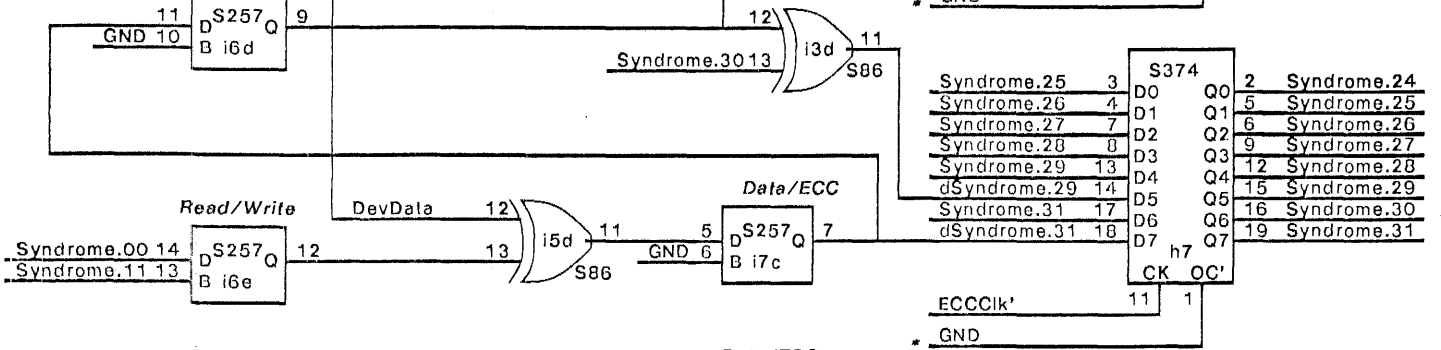
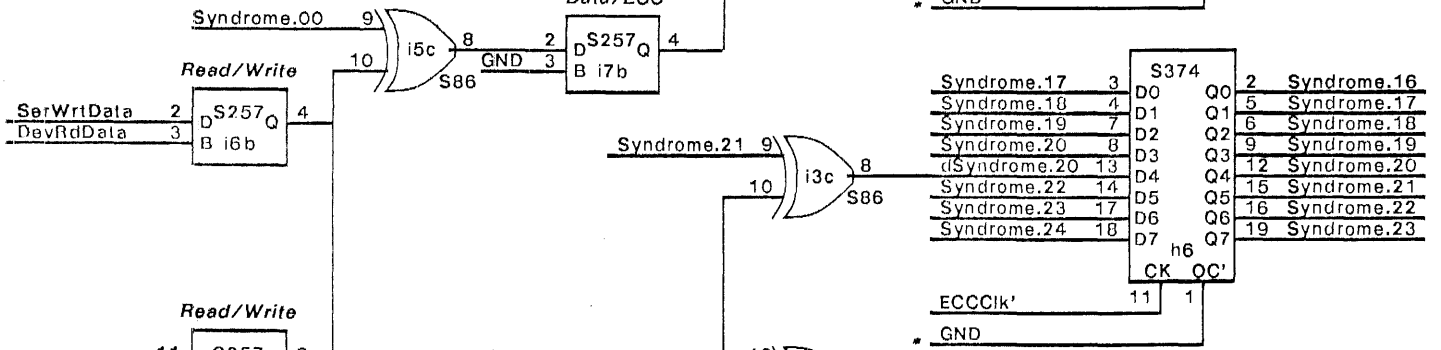
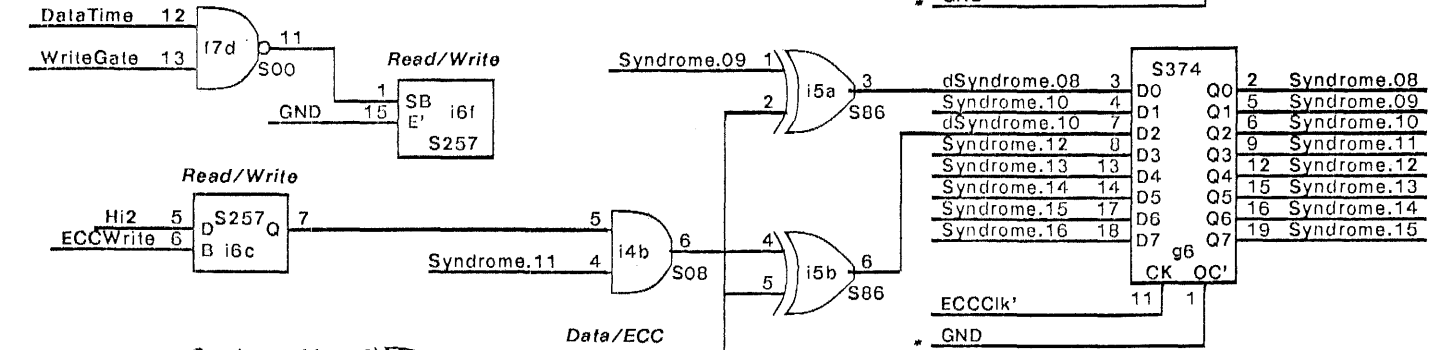
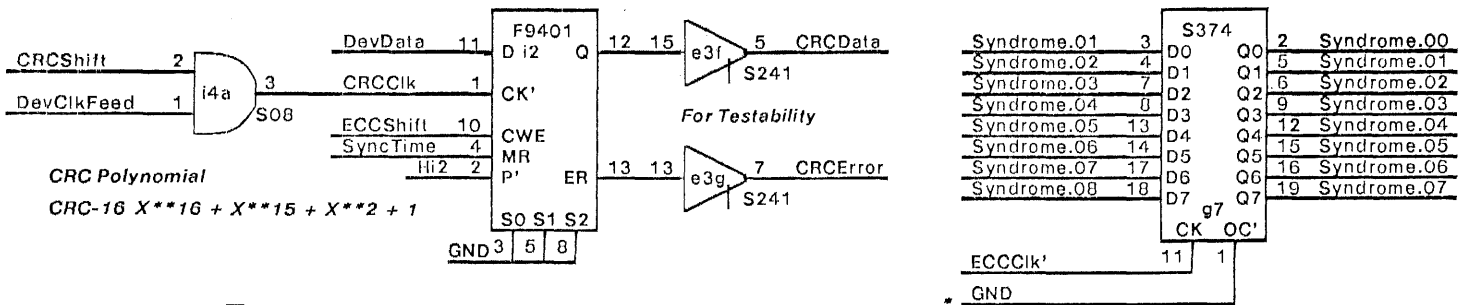
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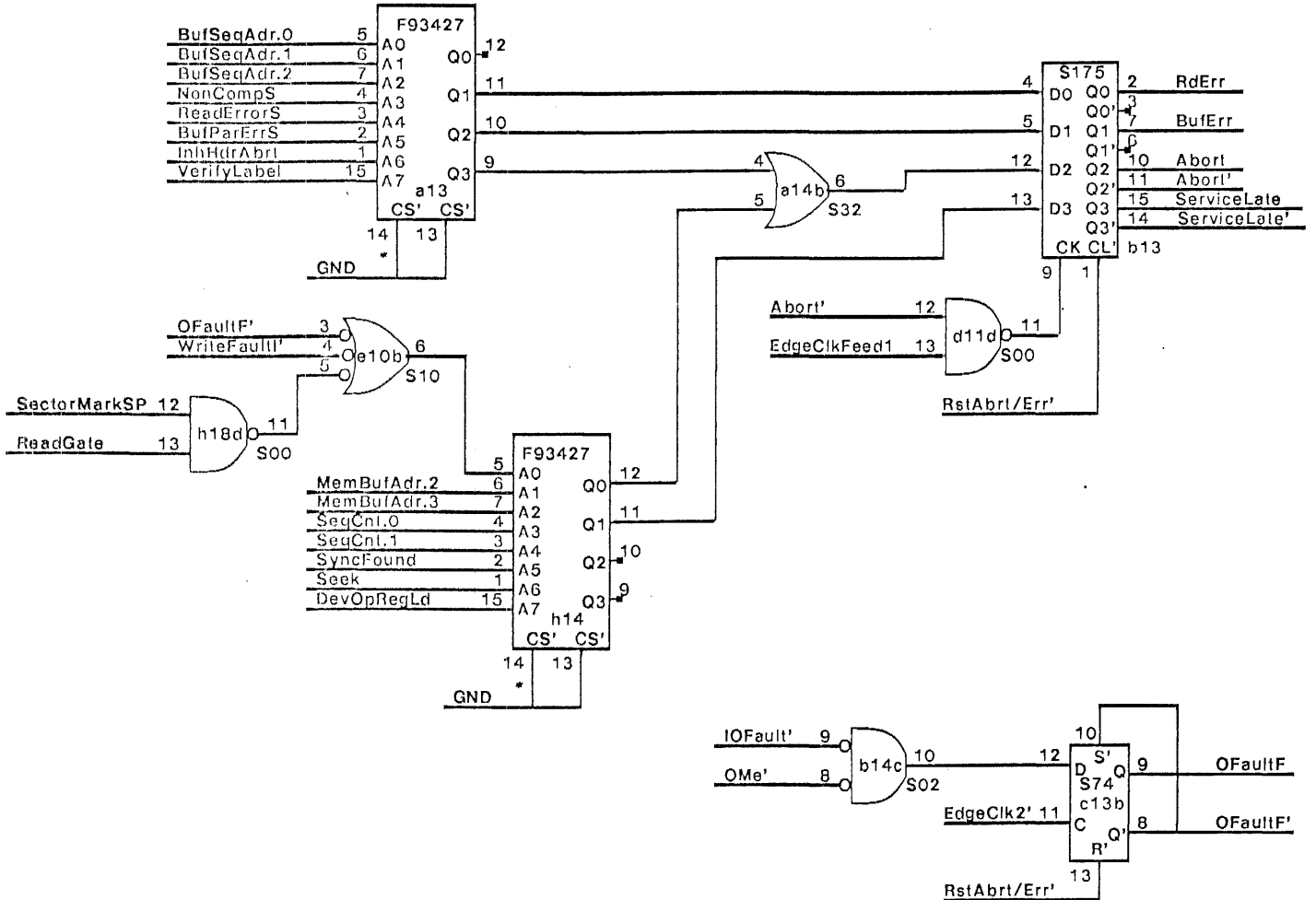
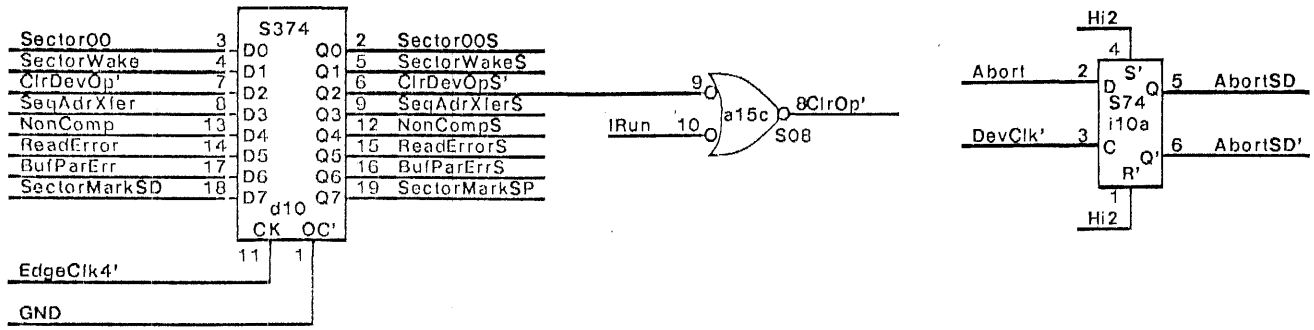




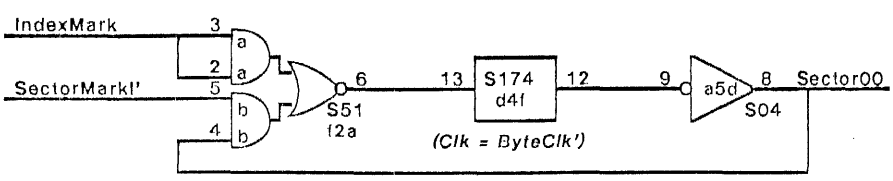
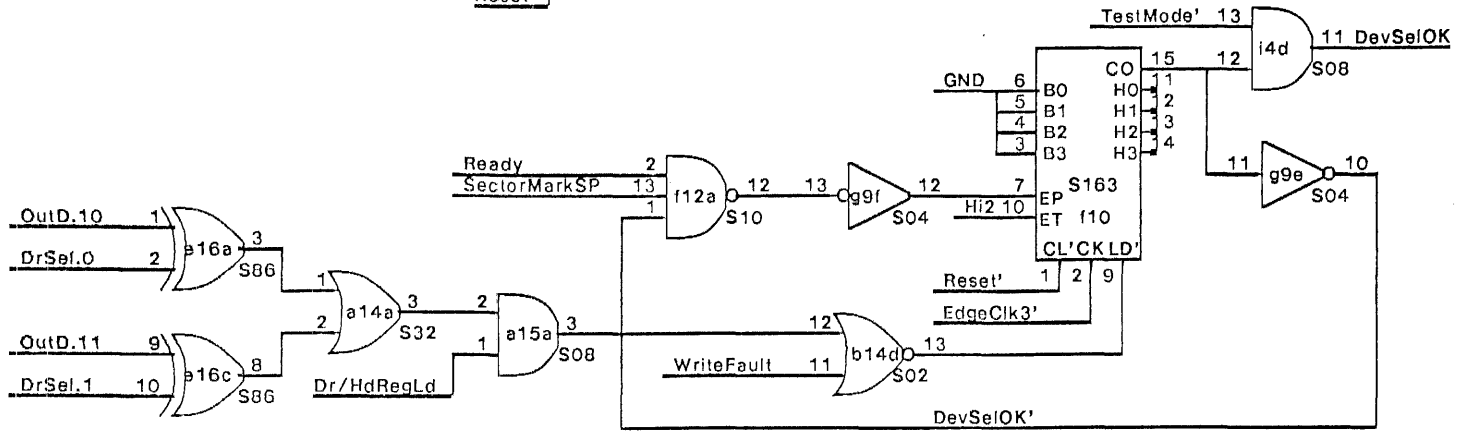
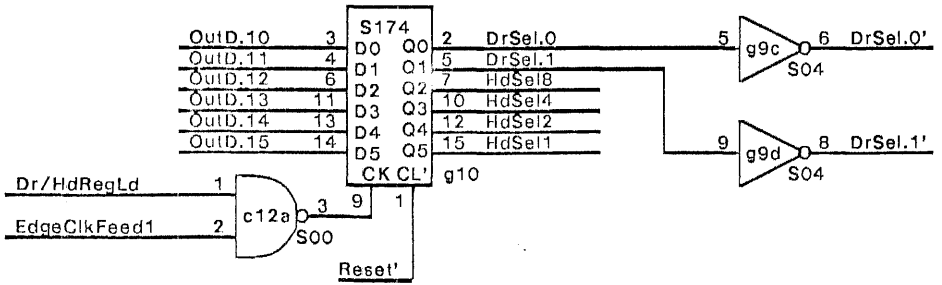
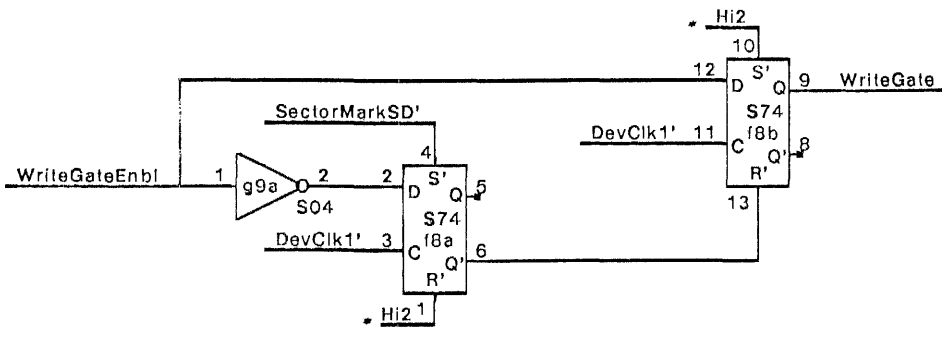
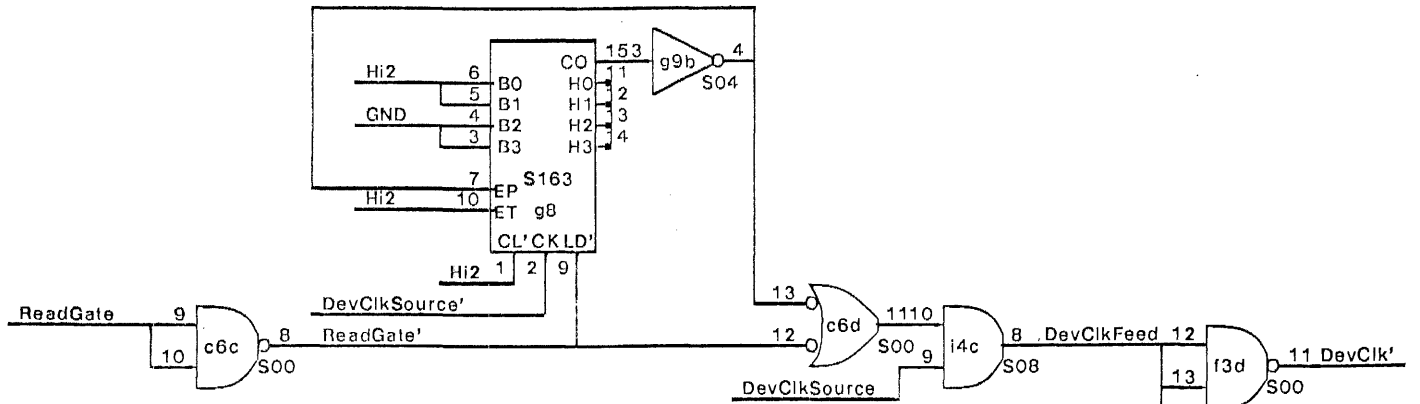
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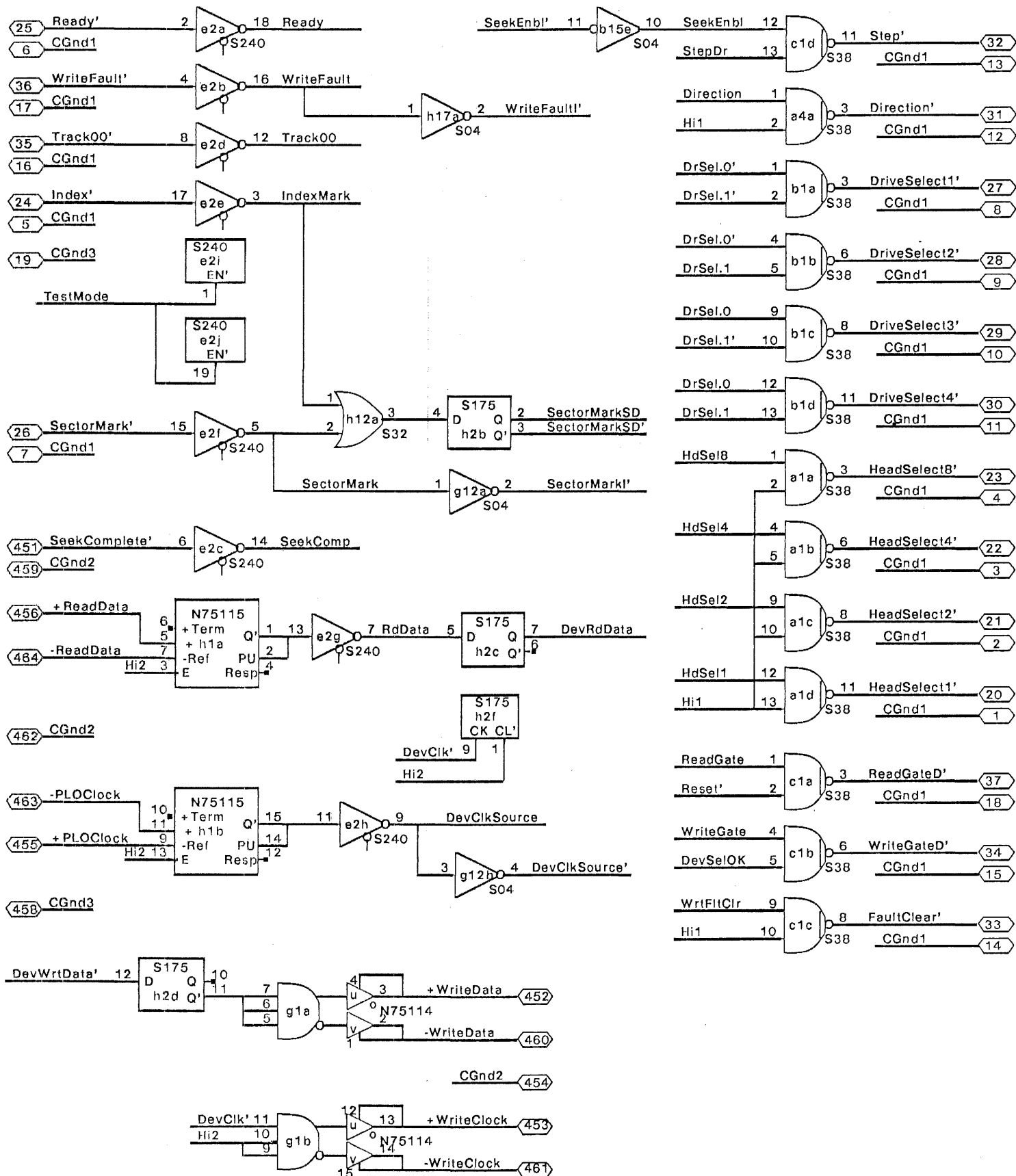
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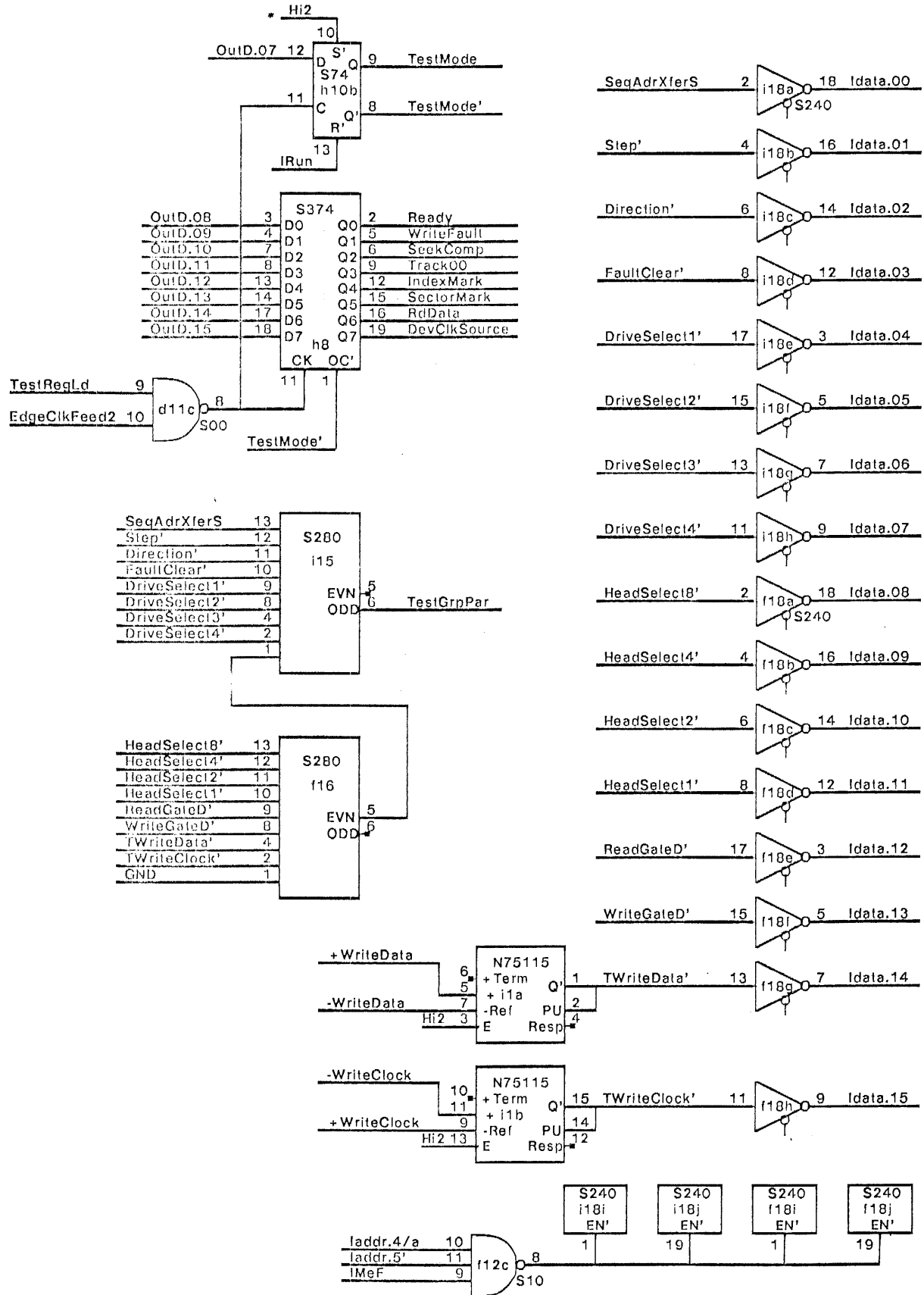


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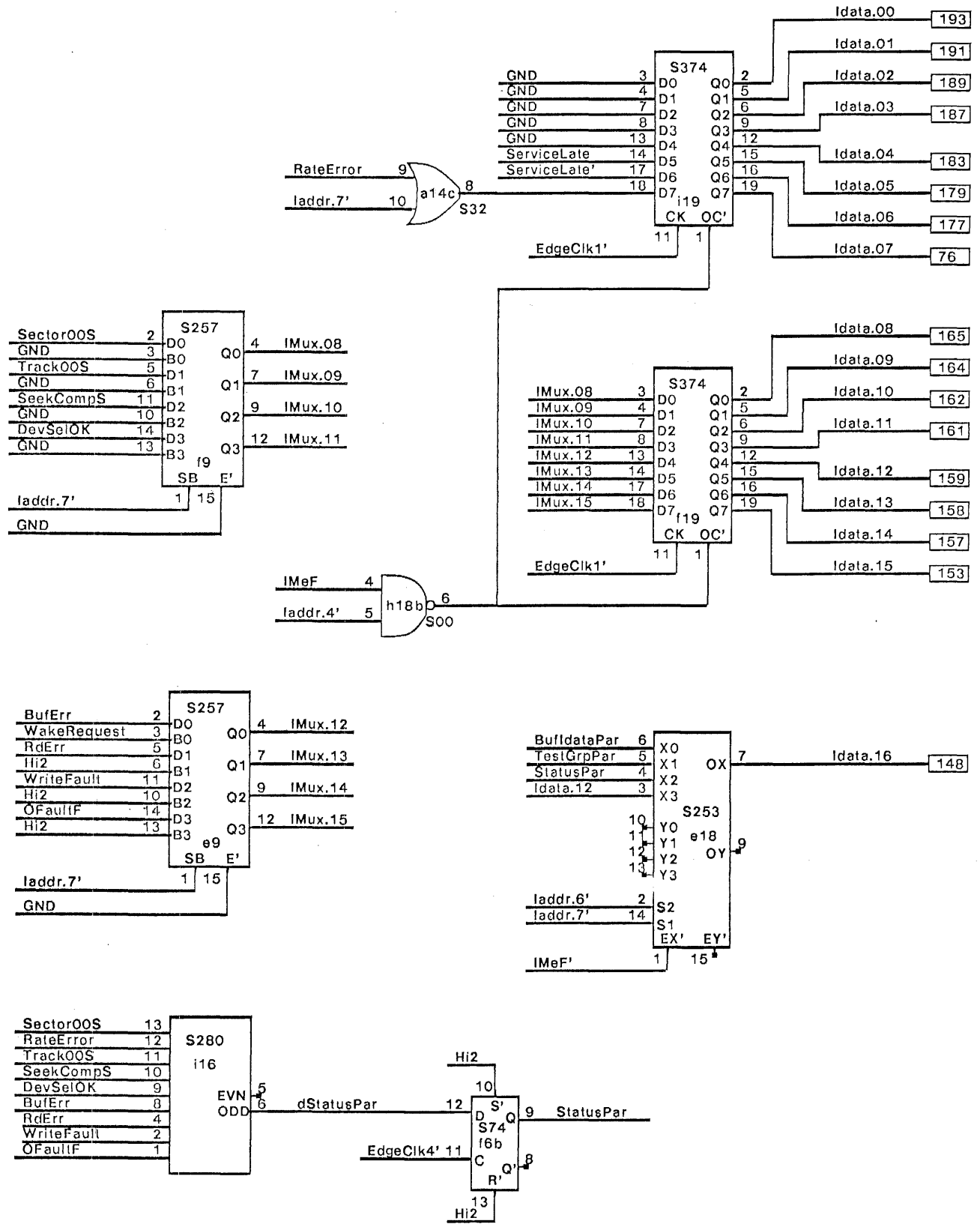


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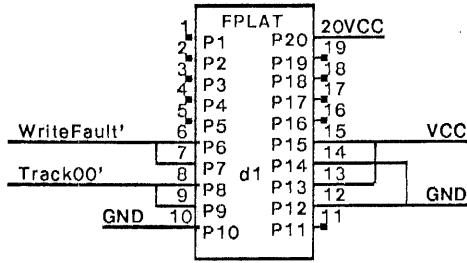


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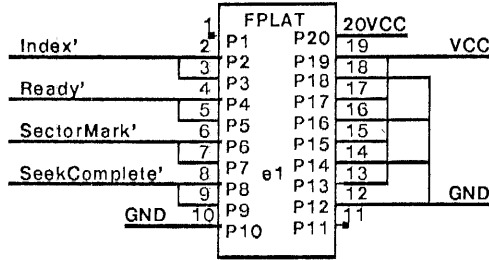


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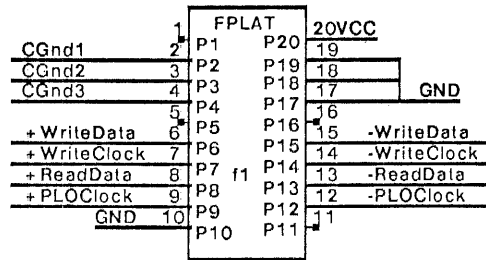
SPLAT A



SPLAT B

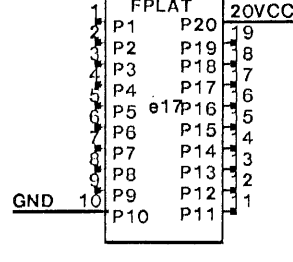
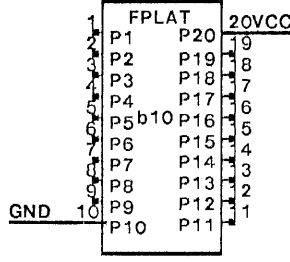
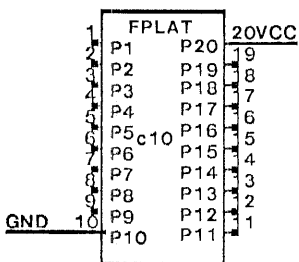
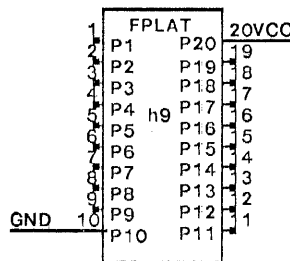
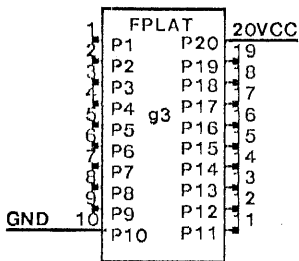


SPLAT C



Note: Splats A, B, and C are 16 pin platforms centered in the 20-pin pattern

Spare Positions (6):





- Rev A: Initial Release
- Rev B: Added SyncTime to Timing Generator PROM address input. Log. Dwg. p. 10.  
 Changed DevSelOK counter load control so that Dr/HdRegLd loads counter only if DrSel[0:1] is changed. Log. Dwg. p. 14.  
 Added Seek counter at b9 to produce seek Step pulse when DevOpReg is loaded with Seek bit (OutD.05). Causes SeqAdr[0:3] to be 0000 when Seek is true. Inhibits Wake-up until Step has been generated. Log. Dwg. p. 2, 3, 4, 5, & 15.  
 Replaced S189 (16 word) buffer with F93422 (256 word) buffer. Log. Dwg. p. 7 & 8.  
 Deleted Wake PROM and Counter; removed XferLate from IOAttn; deleted Flow Control Counter; added Data Wake up/down counter; added 3 wakw count to IOAttn. Log. Dwg. p. 3 & 13.  
 Deleted DRConnect signals and IDWord parity gen. Log. Dwg. p. 14 & 16.  
 Added ability to load DevBufAdrReg & MemBufAdrReg from processor. Log. Dwg. p. 6 & 7.  
 Numerous minor changes in mechanization as a result of above. Log. Dwg. p. all.
- Rev C: Set SectorMarkSP with SectorMarkSD. Log. Dwg. p. 12  
 Removed cross wire of MemBufAdrReg Clear and SectorWakeS strings. Log. Dwg. p. 7.  
 Disabled Seek Counter at max count. Log. Dwg. p. 4.  
 Changed reset of Op Register from Reset' to RstAbrrt/Err'. Log. Dwg. p. 4.  
 Added RateError FF. Log. Dwg. p. 3.  
 Added DataReq to hold term for WakeReqF to override IOStrobe reset. Log. Dwg. p. 3.  
 Added term to Wake Counter enable to prevent incrementing beyond max, or decrementing below 0. Log. Dwg. p. 3.  
 Adds RateError to Status Parity Generator. Log. Dwg. p. 16.  
 Inverted Sync pattern. Log. Dwg. p. 9.  
 Changes DecClkEnable counter clock to DevClkSource'. Log. Dwg. p. 13.  
 Adds SectorMarkI'. Log. Dwg. p. 14.  
 Fixes Testability control. Log. Dwg. p. 5.  
 Fixes ldata Parity select. Log. Dwg. p. 16.  
 Removes 25S09s from BufAdrReg. Replaces them with s257s. Log. Dwg. p. 7.  
 Changes RateError qualifier to DataWrt. Log. Dwg. p. 3.  
 Changed I/O connections to device to reflect etch version with multiple drives. Log. Dwg. p. 14.  
 Made SequenceEnd' true last byte time of SequenceEnd only. Added S00 at b6. Log. Dwg. p. 5.  
 Moved S280 from i14 to i15. Log. Dwg. p. 15
- Rev D: Added one clock delay and DevClk synchronization to parity error logic. Log. Dwg. p. 10.  
 Deleted Abort from Wake Request logic. Log. Dwg. p. 3.  
 Revised DataXferS logic. Log. Dwg. p. 6.  
 Changed BufSeqAdr clock qualifier to SeqAdrXferS. Log. Dwg. p. 6.  
 Devided load on DevClk'. Log. Dwg. various.  
 Added TestMode' qualifier to DevSelOK to prevent writing on device in Test Mode. Log. Dwg. p. 13.  
 Added PrimeIData to BufAdrReg Select. Log. Dwg. p. 6 & 7.  
 Added Write Fault Clear FF. Log. Dwg. p. 2.  
 "Or'ed VerifyLabel with ReadLabel at Op Reg input. Log. Dwg. p. 4.  
 Qualified BufSeqAdr Register Clock with (IMeF + OMeF)'. Log. Dwg. p. 6.  
 Changed data error check to look at Syndrome.00 during ECCCheck. Log. Dwg. p. 11.  
 Changed DevBufAdrReg clear term from SectorWakeS' to ClrDevOpS'. SectorWake cleared too soon. Changed SectorWakeS' to SectorWakeS. Log. Dwg. p. 3, 5, 7, & 12.  
 Added direct set of MyStrobeF by AllowWake to insure Wake-up inhibit. Log. Dwg. p. 2.  
 Removed Reset from S174 @ d4 to prevent "glitch" of Sector00. Log. Dwg. p. 5.  
 Changed reset of XferDataS FF to SequenceEnd'. Log. Dwg. p. 6.  
 Changed latch of NonComp FF to insure at least 2 DevClk times on. Log. Dwg. p. 9.  
 Revised serial parity check/gen logic control. Log. Dwg. p. 10.  
 Added SectorMarkSP "and" ReadGate to Abort set term to indicate missing Sync pattern. Log. Dwg. p. 12.  
 Reversed phase of PLO Clock to increase margin of strobe on read. Log. Dwg. p. 14.
- Rev E: Added SeqAdrXferS' to BufSeqEnbl to insure transfer of Sequence Address even if IMeF or OMeF is true. Log. Dwg. P. 6 & 7.  
 Changed CRC control from DataTime to ECCShift. Log. Dwg. p. 11.  
 Added detection for ServiceLate to indicate Header and Label data not loaded into buffer by Header SyncFound. ServiceLate added as ldata.05 in Status word. Log. Dwg. p. 12 & 16.  
 Changes Reset functions from single Output function with data specified operations to specific Output functions for General Reset and Error Reset to eliminate gate noise on direct reset lines. Log. Dwg. p. 2.  
 Deleted MemUsesBuf and PrimeIData from Buffer Control Sequencer to allow firmware control of MemBufAdrReg. Log. Dwg. p. 6 & 7.  
 Added synchronization of Abort with DevClk (AbortSD) to prevent erroneous setting of Sequencer Address Registers. Log. Dwg. p. 4 & 12.  
 Added RateErrPossible to Buffer Control Sequencer to define actual time when rateerror can occur. Decreased RateError wake-up count from 3 to 2 to insure RateError detection if delay in memory pipe and only 20 words initially loaded in RDC buffer. Log. Dwg. p. 3 & 6.  
 REQUIRES REV B PROMS!!!
- Rev F: Replaced Hi in Status Word with ServiceLate' in order to maintain correct parity. Log. Dwg. p. 12 & 16.  
 Added PrimeIData output function to MemUsesBuf to allow firmware to Prime ldata without parity error  
 Deleted DevBufAdrLd output function. Log. Dwg. p. 2, 6, & 7.  
 Changed AllowWake and WakeReqF control to allow firmware control of AllowWake. Added WakeRequest to IDWord bit 12 for firmware test. This is to facilitate "booting" from the disk. Log. Dwg. p. 2, 3, 4, & 16.
- Rev G: Changed AllowWake so that Odata.04 = 1 sets AllowWake to comply with unpublished convention of setting output registers to zero causing initialization of controllers. Log. Dwg. p. 4.
- Rev Ga: generated from Rev G on 4/11/79 by CPT.  
 1) Redrew splats at d1, e1, f1 as FPLATS to avoid ROUTE trace cuts (pg 17).  
 2) Added spare positions at g3, h9, i9, e17, b10, c10 (pg 17).

Rev Ga: generated from Rev G on 4/11/79 by CPT.

- 1) Redrew splats at d1, e1, f1 as FPLATS to avoid ROUTE trace cuts (pg 17).
- 2) Added spare positions at g3, h9, i9, e17, b10, c10 (pg 17).

Rev Gb: 9/3/79 - CPT

This change is a manual addition to the revision Ga MultiWire board.

1) Lift the following pins:

a15.12  
c16.9  
d10.6  
i13.10  
a13.15

2) Add an S174 IC in position i9, and wire i9.16 to Vcc.

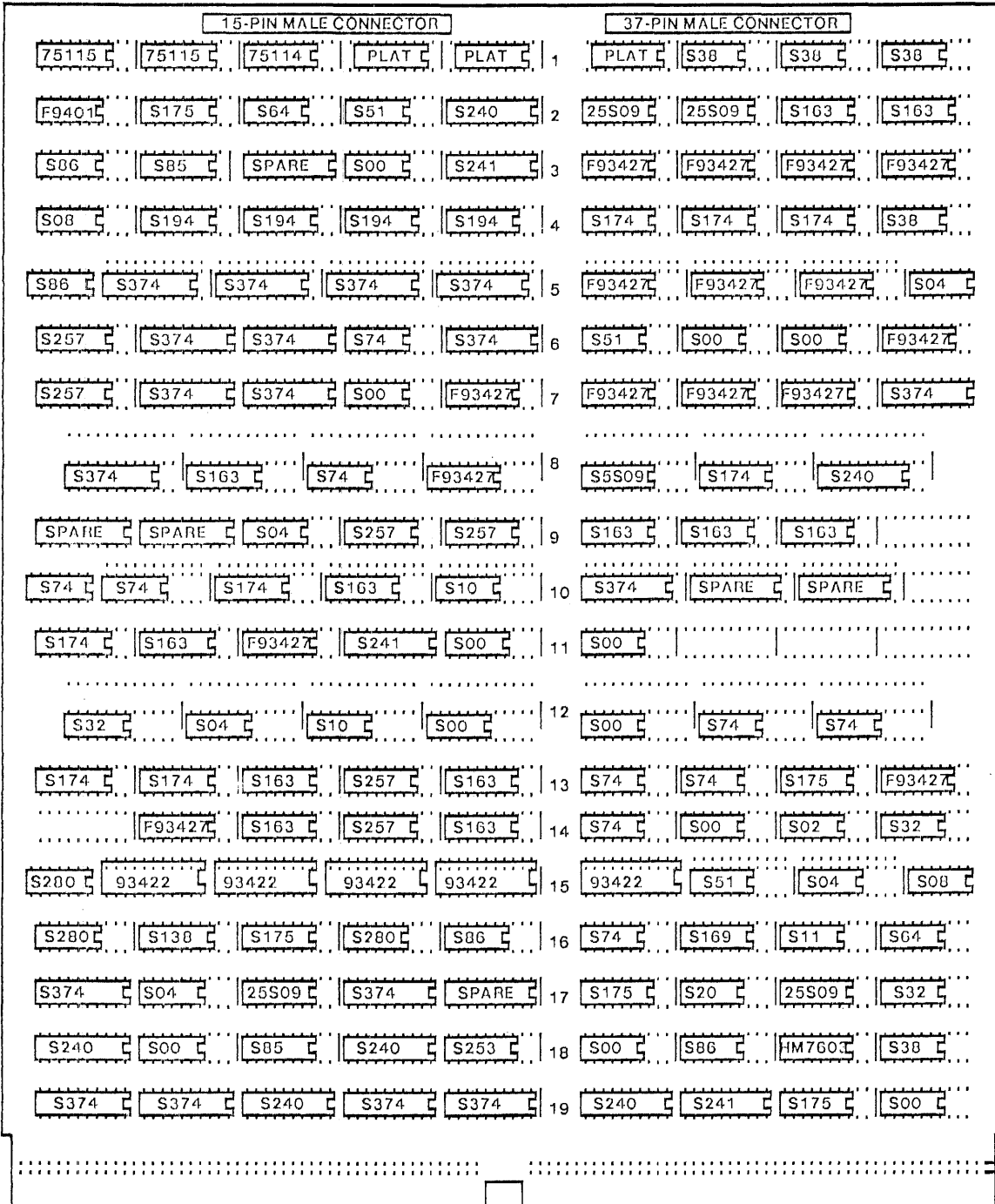
3) Add the following wires:

a15.12 to i16.9 (DevSelOK, pg 2,16)  
c16.9 to a15.11 (RstAbt/Err', pg 3,2)  
d10.6 to a15.9 (ClrDevOpS', pg 12)  
a15.8 to h13.1 (ClrOp', pg 4,7 - new signal name)  
a15.10 to a15.5 (IRun, pg2,12)  
i13.10 to i9.4 (Unnamed signal - was InhHdrAbt, pg 4)  
h13.7 to i9.3 (Unnamed signal - was VerifyLabel, pg 4)  
i11.9 to i9.9 (OpRegClk', pg 4)  
i11.1 to i9.1 (RstAbt/Err', pg 4)  
i9.5 to a13.1 (InhHdrAbt, pg 4,12)  
i9.2 to a13.15 (VerifyLabel, pg 4,12)

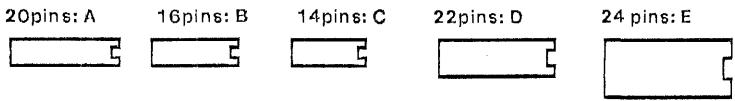
0.

XEROX EOD	Project DO	RDC Logic Changes	File RDCCChanges2.sil	Designer J. F. Cameron	Rev Gb	Date 9/3/79	Page 18
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I H G F E D C B A

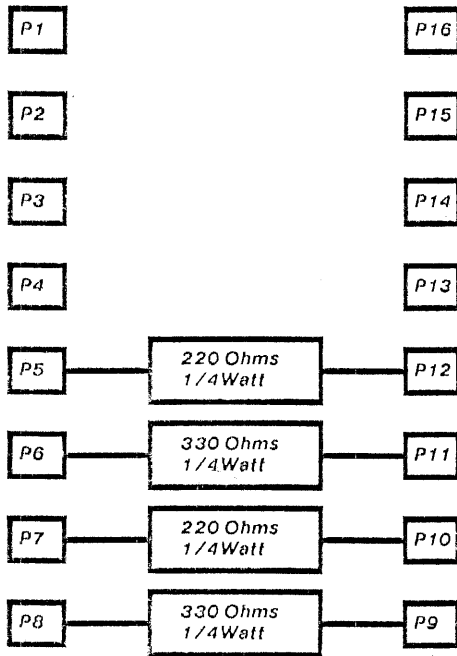


101-200  
1-100

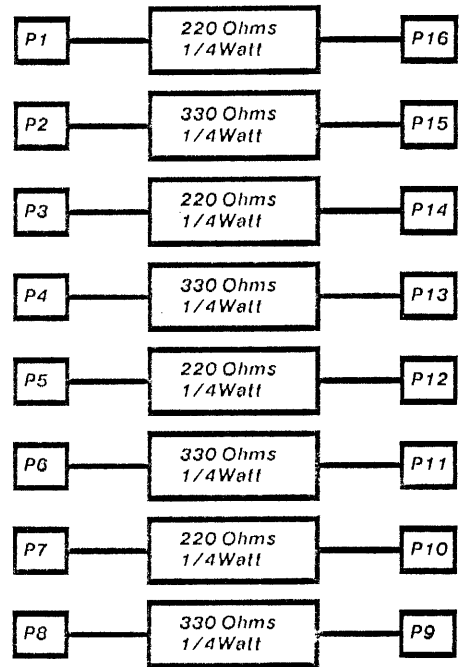


Note: The short vertical lines indicate filter capacitor locations.

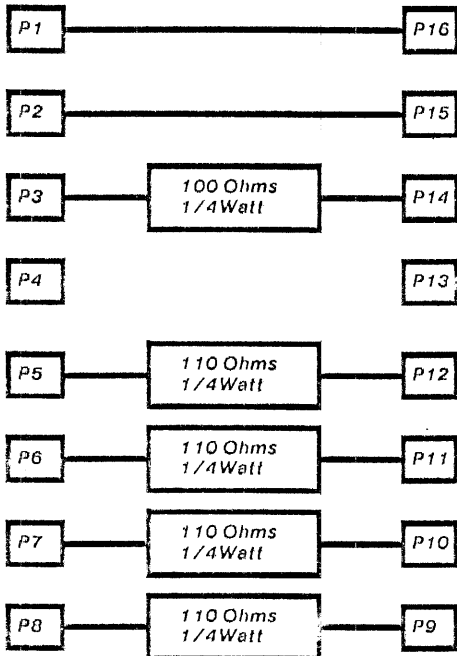
SPLAT A

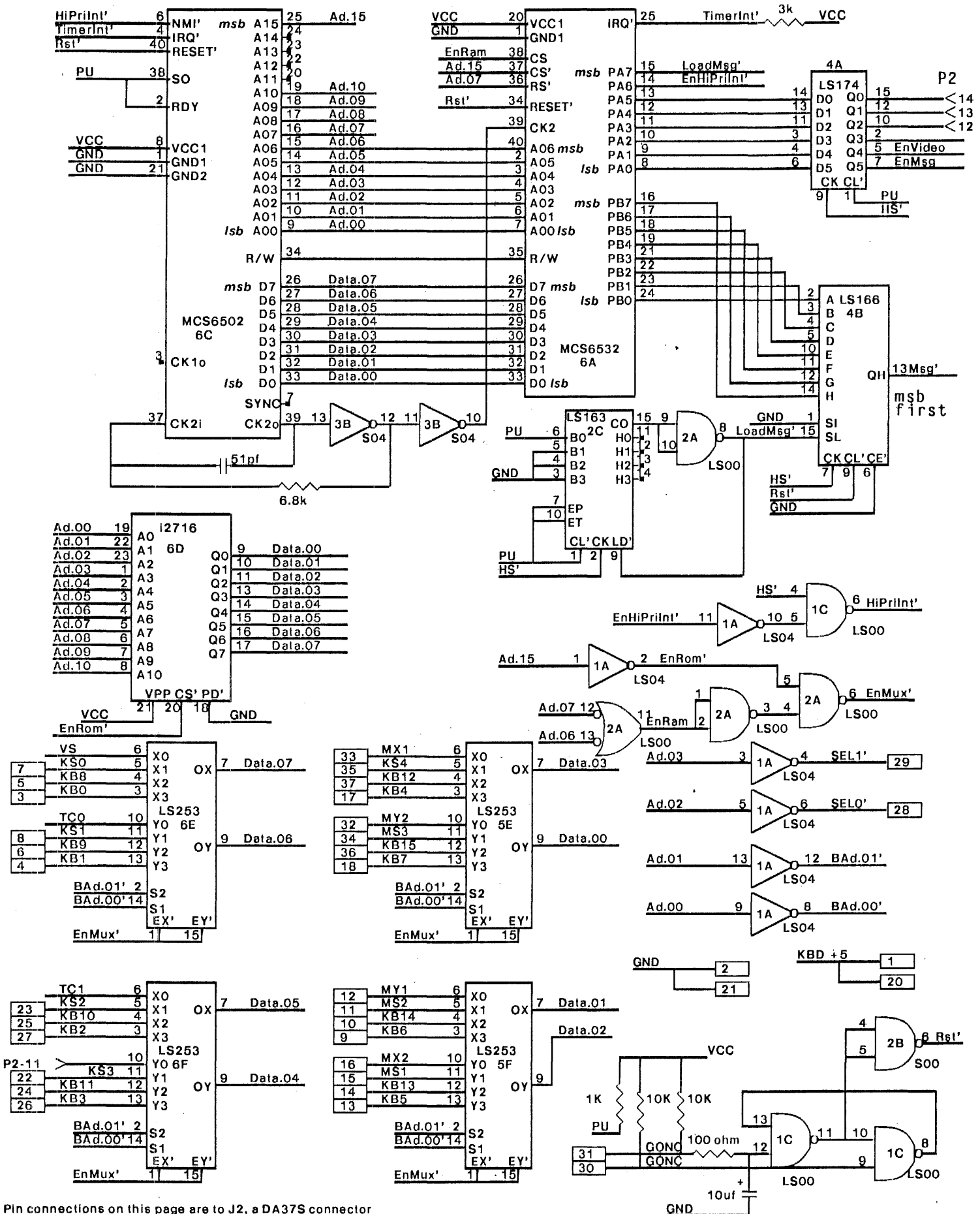


SPLAT B



SPLAT C

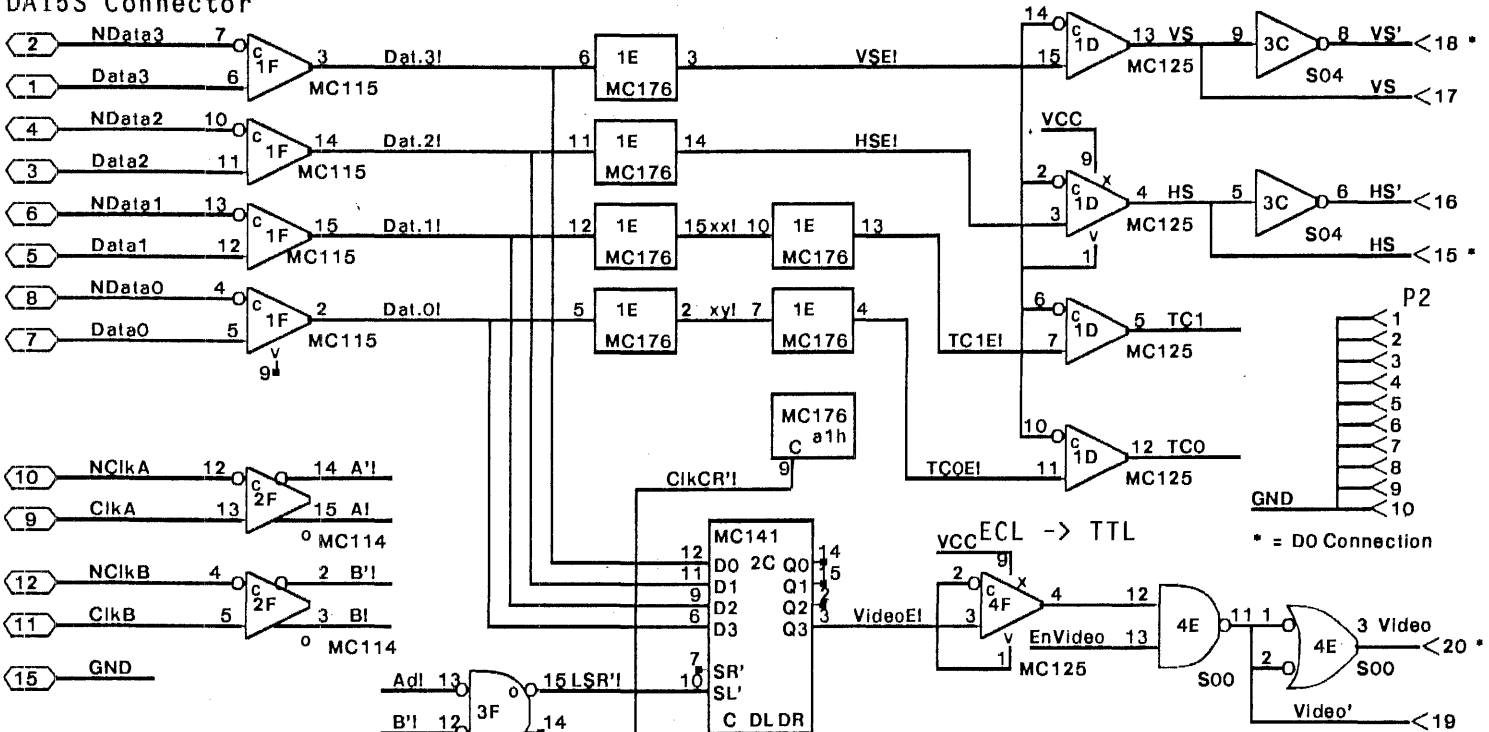




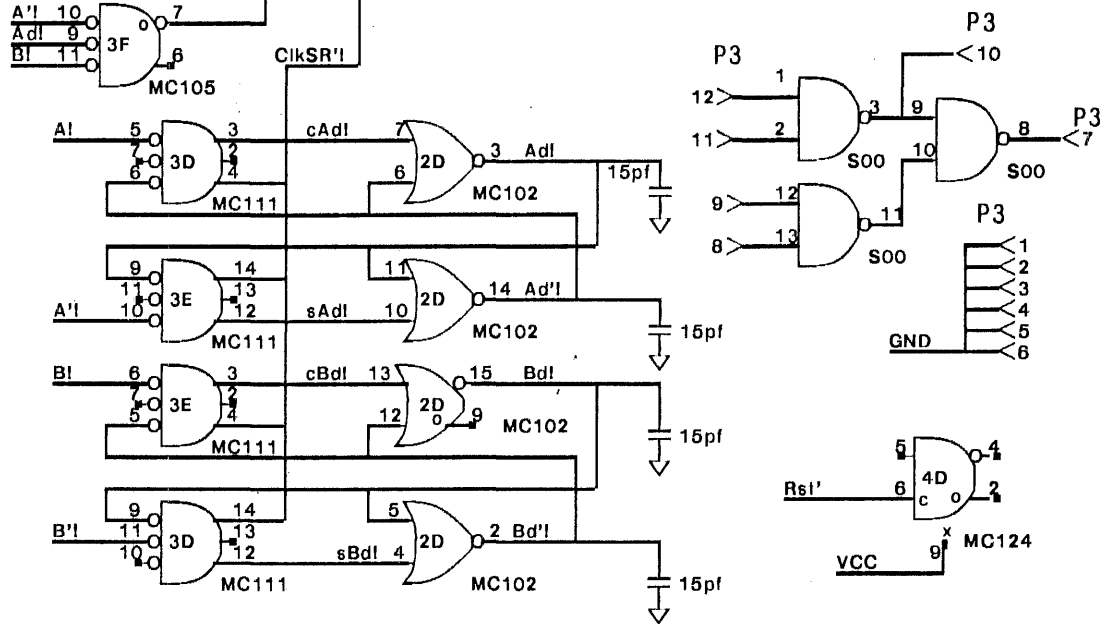
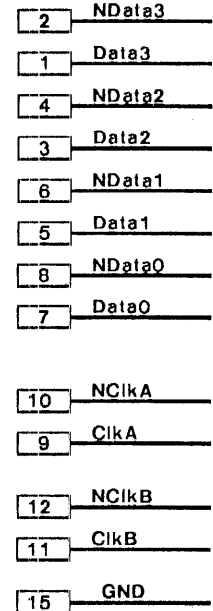
Pin connections on this page are to J2, a DA37S connector

J1  
DA15S Connector

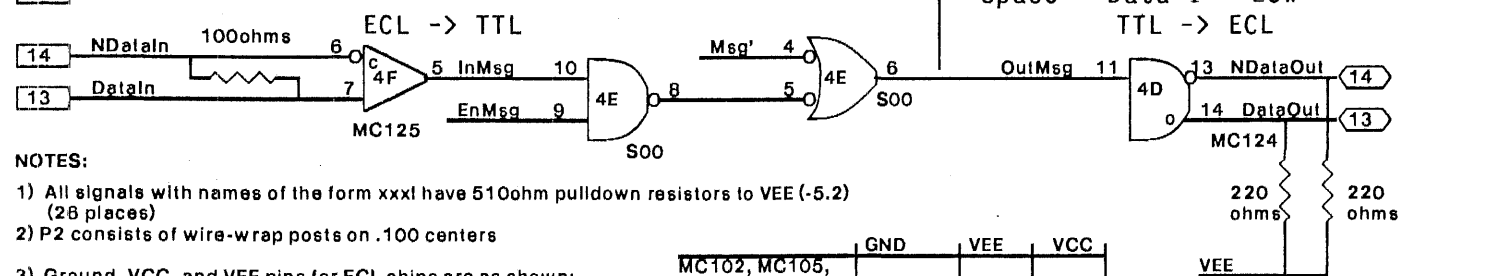
ECL -> TTL P2



P1  
DA15P Connector



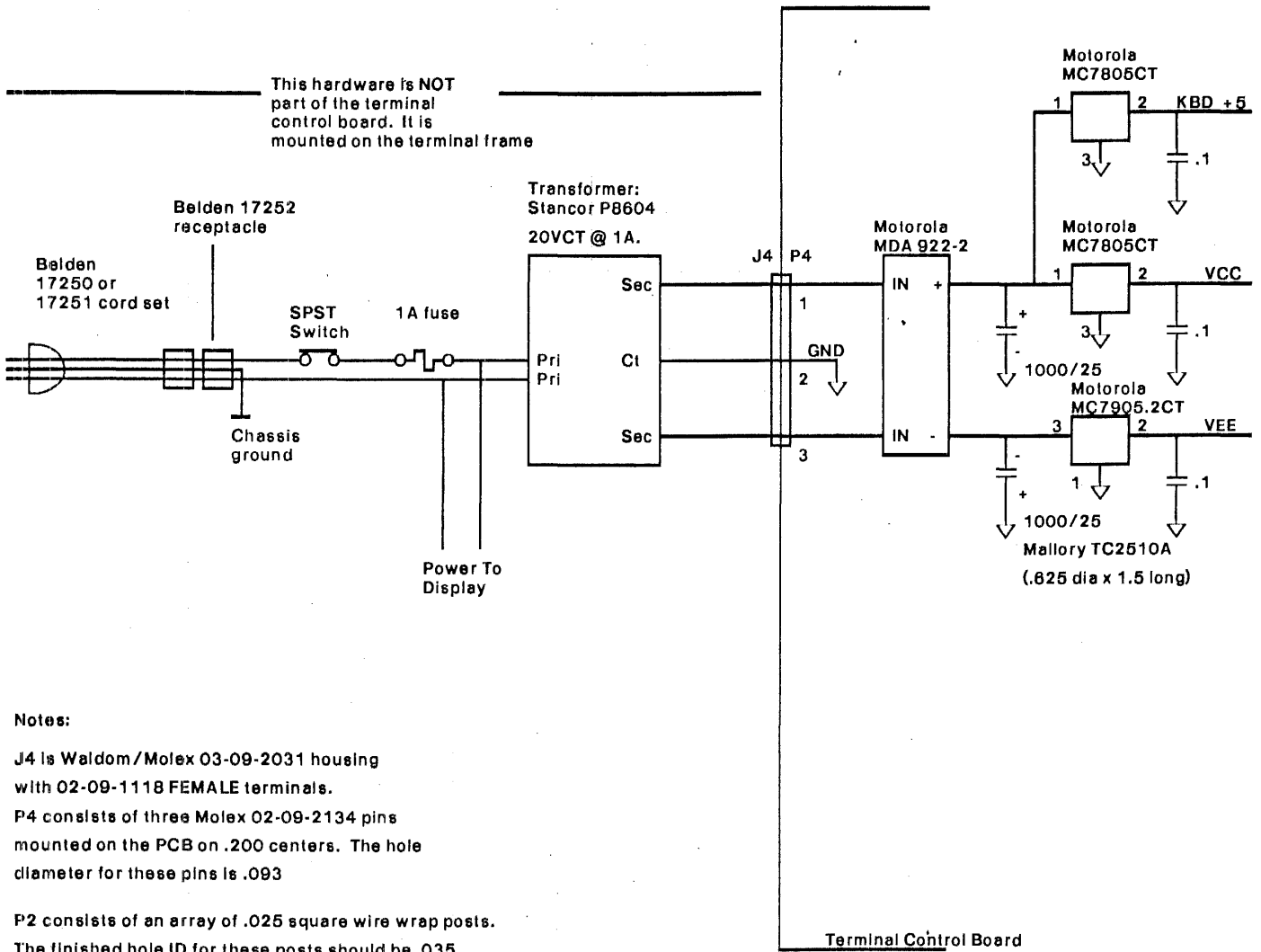
Mark = Data 0 = High (Idle State)  
Space = Data 1 = Low  
TTL -> ECL



NOTES:

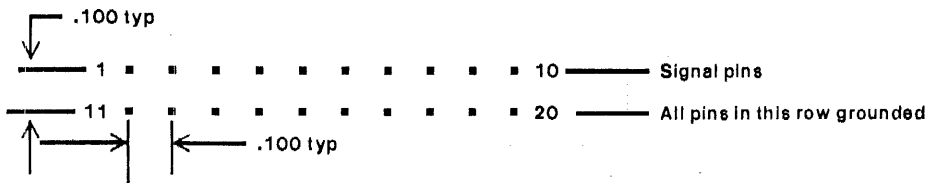
- 1) All signals with names of the form xxxl have 510ohm pulldown resistors to VEE (-5.2) (28 places)
- 2) P2 consists of wire-wrap posts on .100 centers
- 3) Ground, VCC, and VEE pins for ECL chips are as shown:

	GND	VEE	VCC
MC102, MC105, MC114, MC115	1,16	8	-
MC141	1,15,16	8	-
MC111	16	8	9
MC124, MC125	16	8	-
MC173, 176	16	8	-

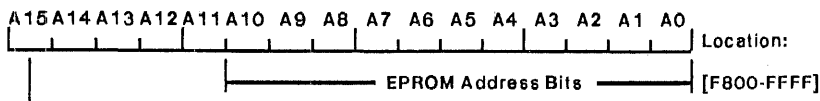


**Notes:**

- 1) J4 is Waldom/Molex 03-09-2031 housing with 02-09-1118 FEMALE terminals. P4 consists of three Molex 02-09-2134 pins mounted on the PCB on .200 centers. The hole diameter for these pins is .093
- 2) P2 consists of an array of .025 square wire wrap posts. The finished hole ID for these posts should be .035. There should be two rows of pins. Only one row is shown on the logic diagrams; all pins in the other row are connected to ground:



- 3) VCC and VEE have one .01uf bypass capacitor per IC package.



1 => Enable EPROM  
 0 => Enable 6532

Ram Address Bits

	RS'	A6	A5	A4	A3	A2	A1	A0	Location	6532 Address Lines
0	X	X	X	X	X	X	X	X	[00-7F]	Ram Address (R/W)
	1	0	X	X	X	0	0	0	[80]	Output Register A (R/W)
	1	0	X	X	X	0	0	1	[81]	DDRA (R/W)
	1	0	X	X	X	0	1	0	[82]	Output Register B (R/W)
	1	0	X	X	X	0	1	1	[83]	DDRB
	1	0	X	X	IE	1	X	0	[84,8C]	Read Timer
	1	0	X	X	X	1	X	1	[85]	Read Interrupt Flag
	1	0	X	0	X	1	ED	ED	[84-87]	Write Edge Detect Control (Data not used)
	1	0	X	1	IE	1	TP	TP	[94-97,9C-9F]	Write Timer
	1	1	X	X	SEL	SEL	MO	M1	[C0-CF]	Read Multiplexer Inputs

IE = Disable (0)/Enable (1) timer interrupt  
 TP = Timer Period: 0 = T, 1 = 8T, 2 = 64T, 3 = 1024T

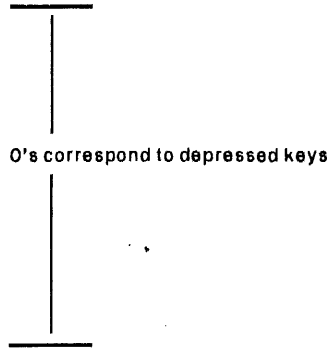
ED = Edge Detect: 0,2 => Disabled  
 1 => Interrupt on PA7 negative edge  
 3 => Interrupt on PA7 positive edge

SELO, SEL1 determine the keyboard word transmitted to the multiplexers

For the Altoll Microswitch keyboard, the bits are as follows:

BIT:

Address:	7	6	5	4	3	2	1	0	
C3	VS	TC0	TC1	0	MX1	MX2	MY1	MY2	
C2	KS0	KS1	KS2	KS3	KS4	MS1	MS2	MS3	
C1	zero	K	-	P	/	\	lf	bs	(KB8-KB15)
C0	5	4	6	E	7	D	U	V	(KB0-KB7)
C9	Z	lshift	.	;	ret	←	del	none	(KB8-KB15)
C8	1	esc	tab	F	ctrl	C	J	B	(KB0-KB7)
C5	X	O	L	,	'	]	spare mid	spare top	(KB8-KB15)
C4	3	2	W	Q	S	A	9	I	(KB0-KB7)
CD	lock	space	[	=	rshift	spare bot	none	none	(KB8-KB15)
CC	R	T	G	Y	H	8	N	M	(KB0-KB7)



These bits end up in Alto memory as follows:

BIT:

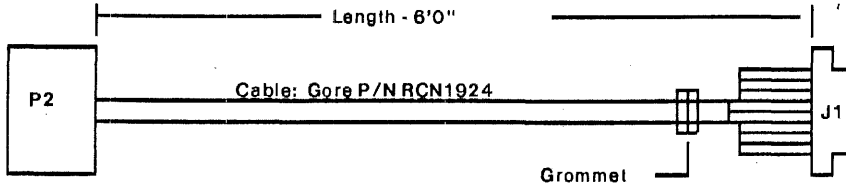
Address:	0	1	2	3	4	5	6	7	8	9	0	11	12	13	14	15
177034	5	4	6	E	7	D	U	V	zero	K	-	P	/	\	lf	bs
177035	3	2	W	Q	S	A	9	I	X	O	L	,	'	]	spare mid	spare top
177036	1	esc	tab	F	ctrl	C	J	B	Z	lshift	.	;	ret	←	del	none
177037	R	T	G	Y	H	8	N	M	lock	space	[	=	rshift	spare bot	none	none
177030									KS0	KS1	KS2	KS3	KS4	MS1	MS2	MS3



37-Pin  
MALE  
D-Shell connector  
With Rear entry Hood  
and Sliding lock retainer

50-Pin  
Card Edge Connector

AMP,P/N 1-583717-1 (Housing)  
AMP P/N 583854-3 or  
583854-5 (Contact - 50 reqd.)  
(contacts are solder cup)



KEYBOARD J1	7-WIRE INTERFACE P1	KEYBOARD J1	7-WIRE INTERFACE P1
1	27 BLU	U	1 W (20 GAUGE-LARGE WIRE)
2	9 Y	N	2 BLK (20 GAUGE-LARGE WIRE)
3	26 Y/BR	B	3 VIO
4	13 Y/R	A	4 Y/BLK
5	14 Y/VIO	8	5 O
6	36 Y/GRY	J	6 Y/GRN
7	24 Y/BLU	14	7 O/BLK
8	5 O	16	8 O/BRN
9	28 GRY	2	9 Y
13	35 O/VIO	F	10 BLK (26 GAUGE-SMALL WIRE)
14	7 O/BLK	25	11 W/BRN
15	22 O/BLU	23	12 W/GRN
16	8 O/BRN	4	13 Y/R
17	31 BLU/BLK	5	14 Y/VIO
23	12 W/GRN	Z	15 W/BLK
24	33 W/YEL	X	16 W/O
25	11 W/BRN	C	17 GRN
A	4 Y/BLK	D	18 Y/O
B	3 VIO	V	20 O/GRN
C	17 GRN	P	21 W/VIO
D	18 Y/O	15	22 O/BLU
E	37 BRN	S	23 O/R
F	10 BLK (26 GAUGE-SMALL WIRE)	7	24 Y/BLU
H	25 R	H	25 R
J	6 Y/GRN	3	26 Y/BR
K	29 W (26 GAUGE-SMALL WIRE)	1	27 BLU
N	2 BLK (20 GAUGE-LARGE WIRE)	9	28 GRY
P	21 W/VIO	K	29 W (26 GAUGE-SMALL WIRE)
S	23 O/R	T	30 BLU/BRN
T	30 BLU/BRN	17	31 BLU/BLK
U	1 W (20 GAUGE-LARGE WIRE)	W	32 W/BLU
V	20 O/GRN	24	33 W/YEL
W	32 W/BLU	Y	34 W/R
X	16 W/O	13	35 O/VIO
Y	34 W/R	6	36 Y/GRY
Z	15 W/BLK	E	37 BRN

NOTES:

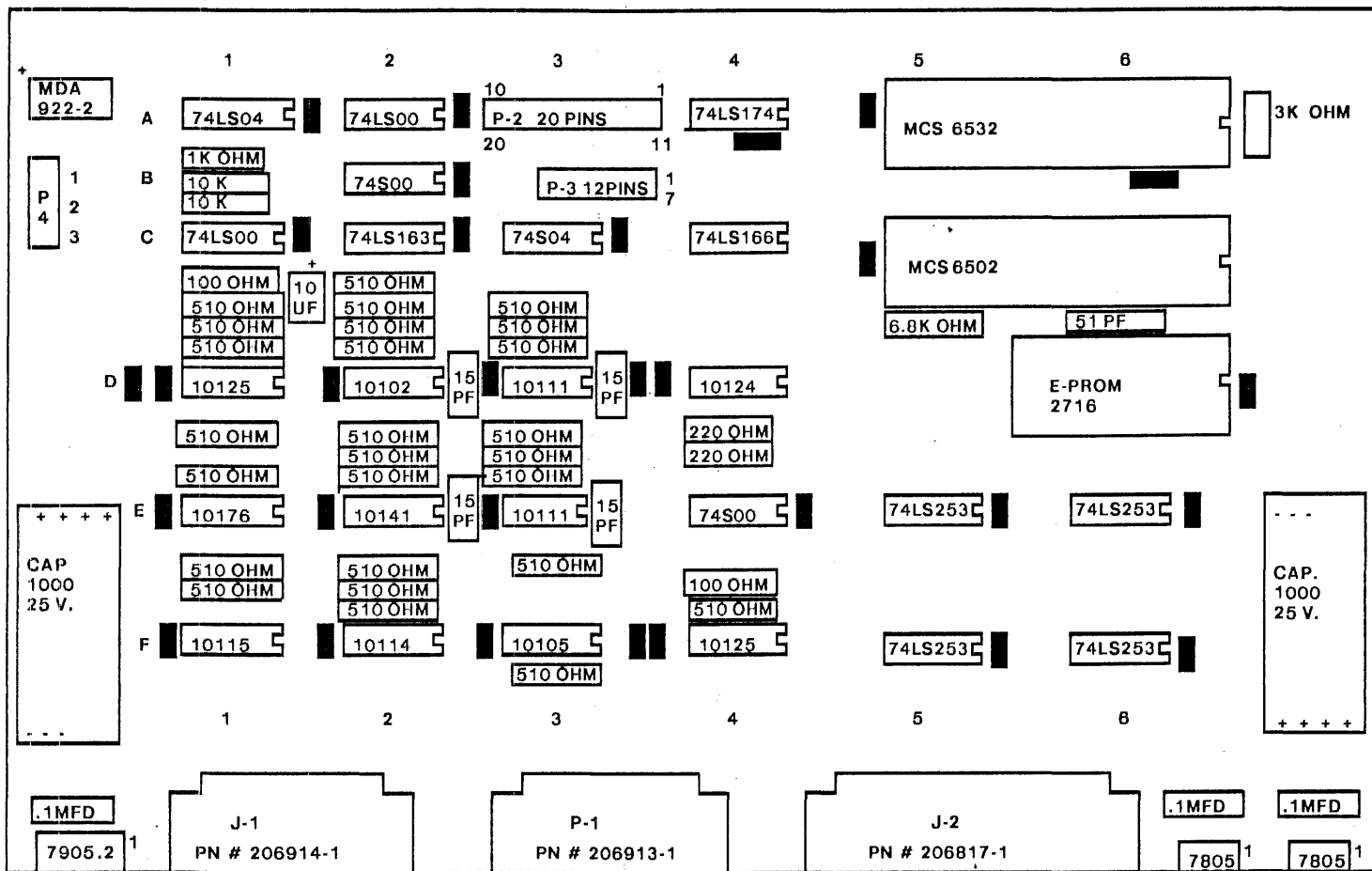
1. CABLE IS 6 FT. LONG +/- 4IN
2. W/GRY WIRE IS CUT OFF
3. O/GRY WIRE IS CUT OFF
4. CABLE IS (GORE PN # RCN1924)

XEROX PARC	Project DO	7-Wire Terminal Interface Keyboard-Terminal Int. Cable	File Terminalcable.sil	Designer Thacker/vest	Rev Gb	Date 12/26/79	Page 1
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Changes to generate revision Gb (8/22/79 by CPT).

- 1) 6c.21 ← Vcc, 6c.18 ← Gnd (EPROM select signals).
  - 2) 2b.3,4,5 ← Gnd, rather than Vcc.
  - 3) 4c.8 ← Rst', rather than PU.
  - 4) 4b.9 ← Rst', rather than PU.
  - 5) Added an additional S00 connected to 6 additional pins of P2.  
This chip provides various flavors of sync via jumpers on P2.
  - 6) Changed the way in which Rst' is generated (added power-up reset).  
Changed 2 1K resistors to 10K, added 100 ohm resistor and 10uf capacitor, added extra S00 section to generate Rst'.
- NOTE: Changes 1-4 will be done to revision A boards via wiring, but 5 and 6 will not be done.  
All changes will be incorporated into the revision B artwork.

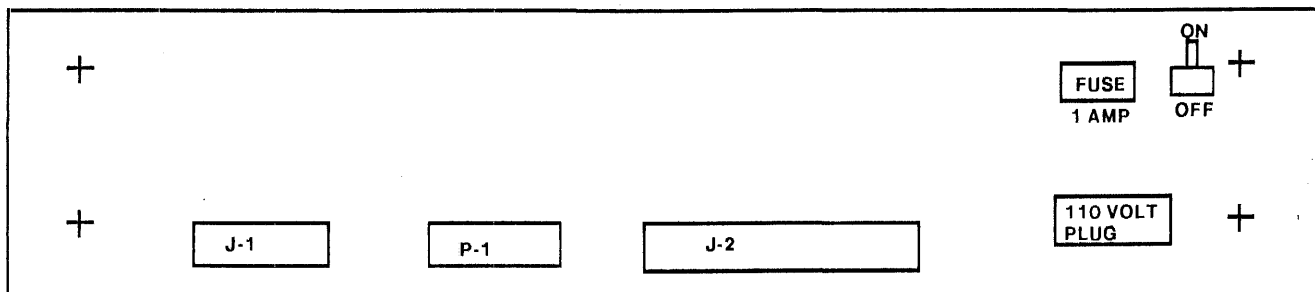
XEROX CSL	Project DO	Terminal Changes	File D0TerminalChanges.sil	Designer Thacker	Rev Gb	Date 8/22/79	Page 01
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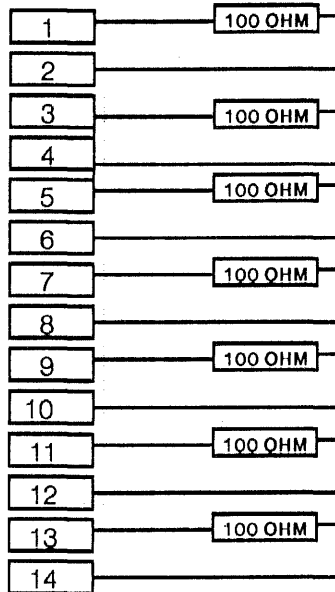
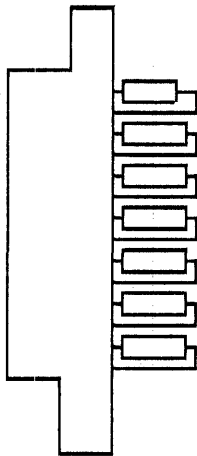


NOTES

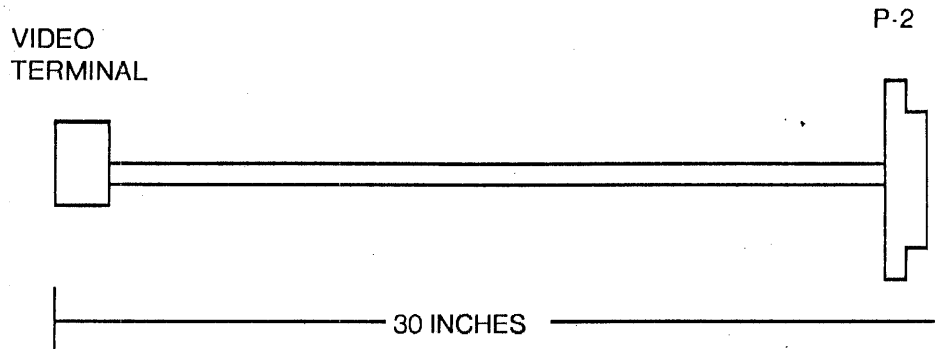
1. [ ] IS A .01 UF CAP.
2. [ ] IS A .01 UF CAP.

BACKPANEL

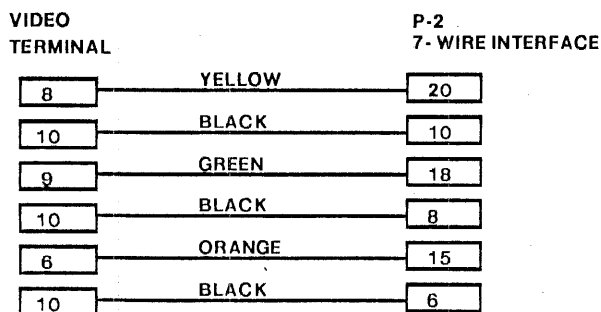




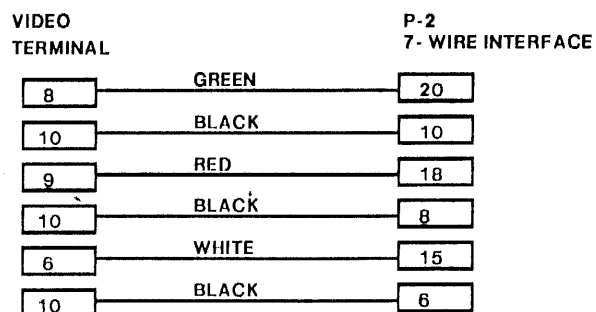
NOTES  
 RESISTORS ARE 100 OHM 1/4 WATT  
 TERMINATOR CONNECTOR IS DA 15S



VIDEO CABLE DO



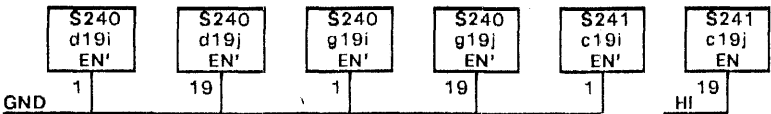
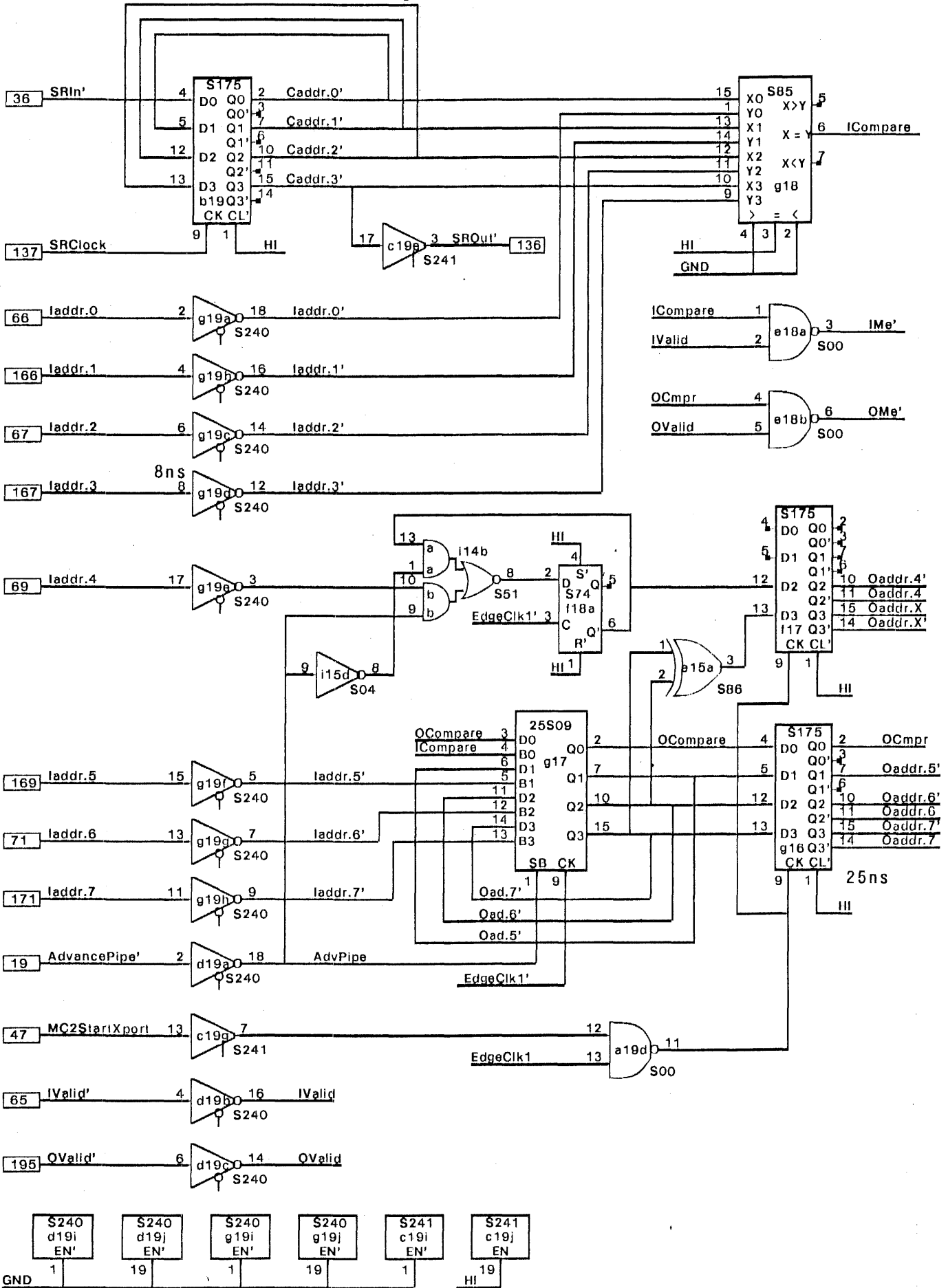
VIDEO CABLE DORADO

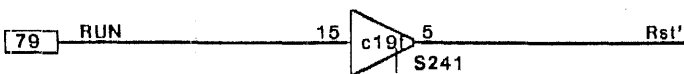
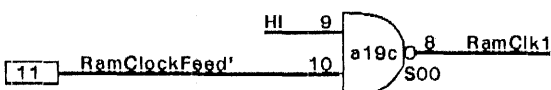
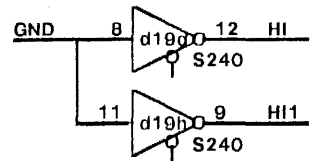
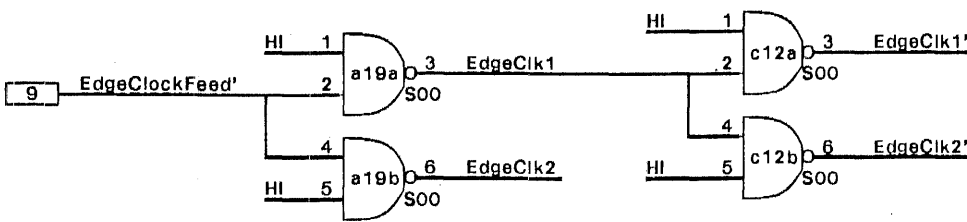
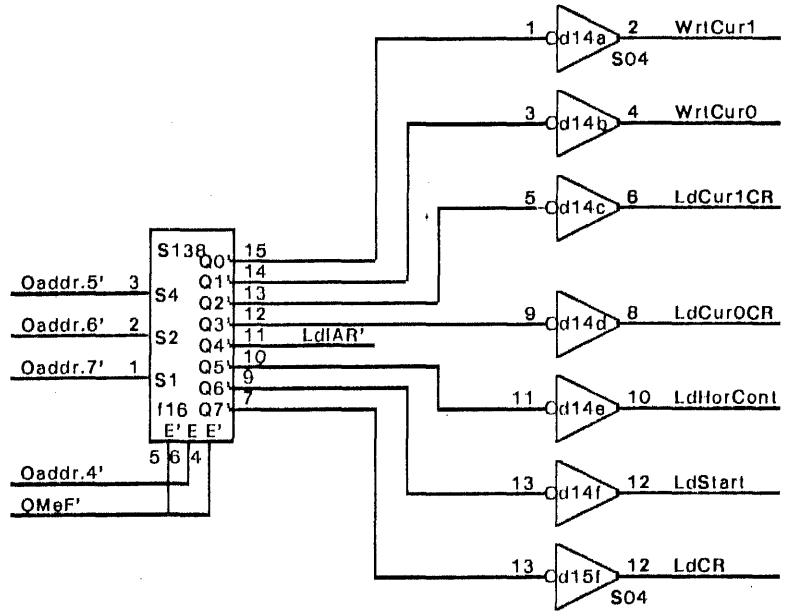
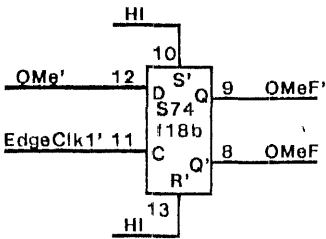
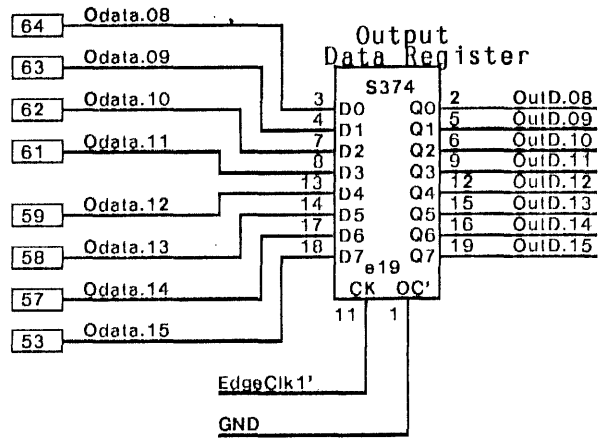
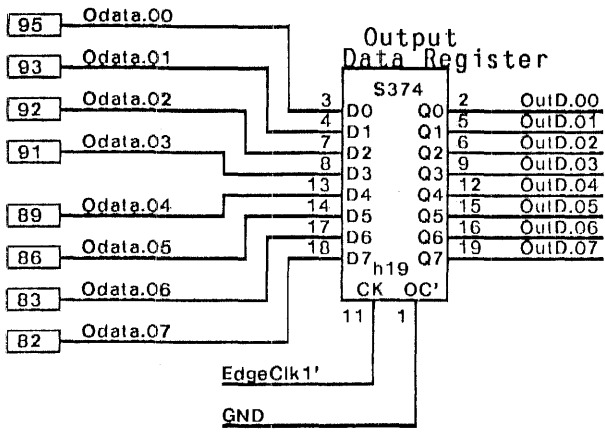


NOTES:

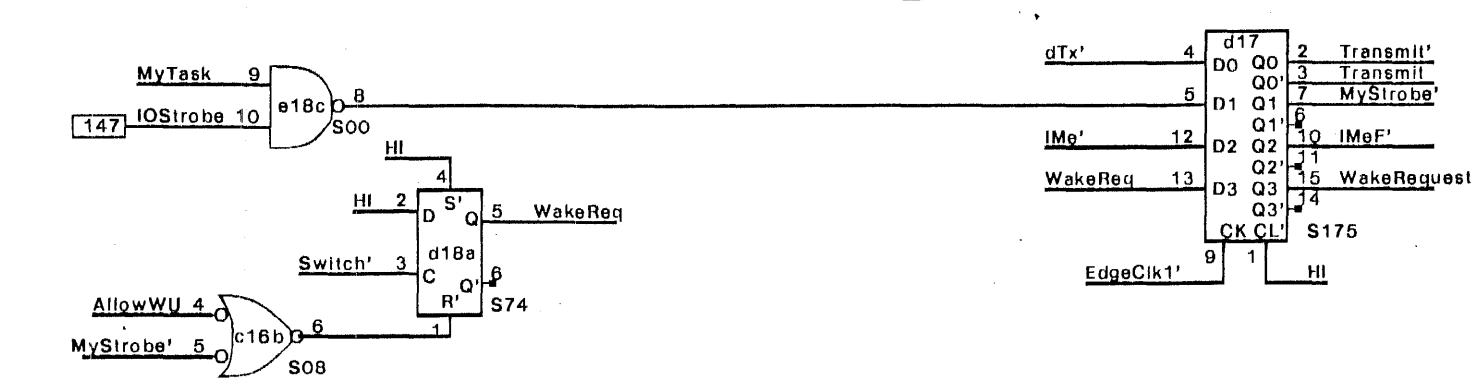
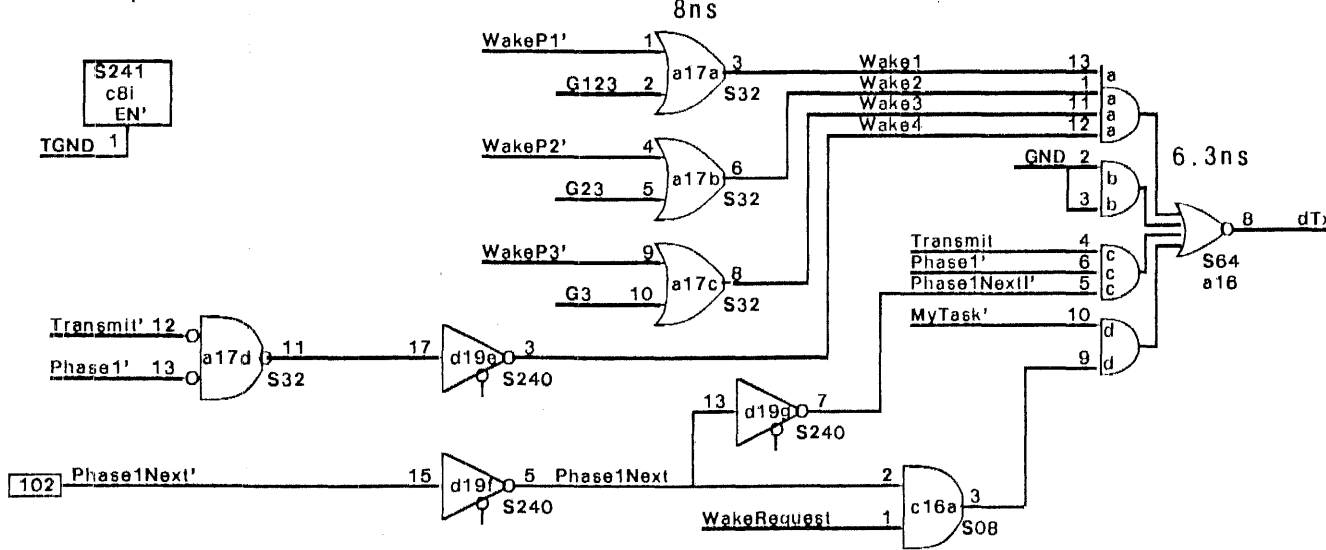
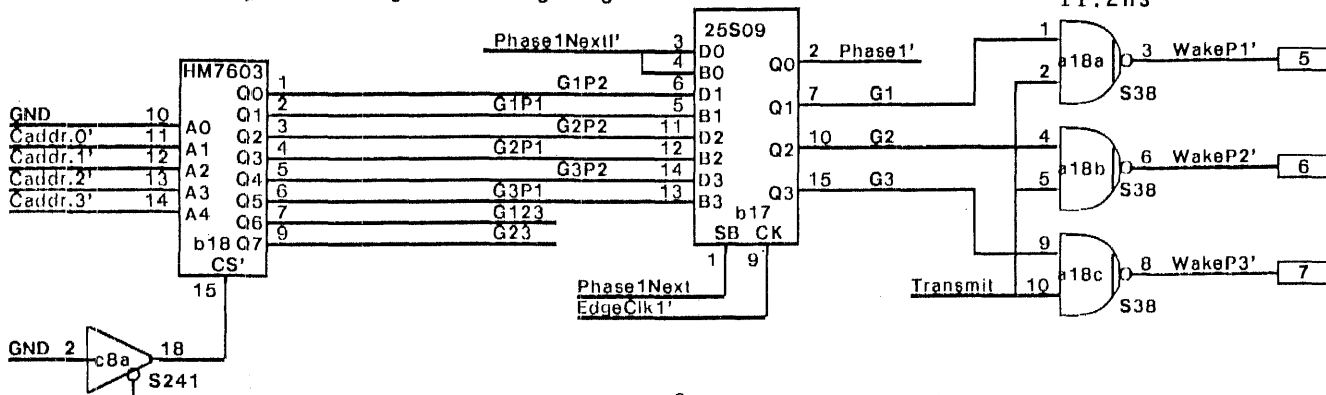
1. WIRE IS 26 AWG TWISTED PAIR
2. TERMINAL CONNECTOR IS AMPHENOL P/N 225-21031-101
3. P-2 CONNECTOR IS AMP 1-87456-6
5. COVER CABLE WITH SHRINK TUBING
6. ADD 100 OHM 1/4 WATT RESISTOR FROM PIN #9 TO PIN #1 ON THE TERMINAL END OF THE CABLE
7. ADD 100 OHM 1/4 WATT RESISTOR FROM PIN #8 TO PIN #1 ON THE TERMINAL END OF THE CABLE
8. ADD 100 OHM 1/4 WATT RESISTOR FROM PIN #6 TO PIN #1 ON THE TERMINAL END OF THE CABLE

### Controller Addressing



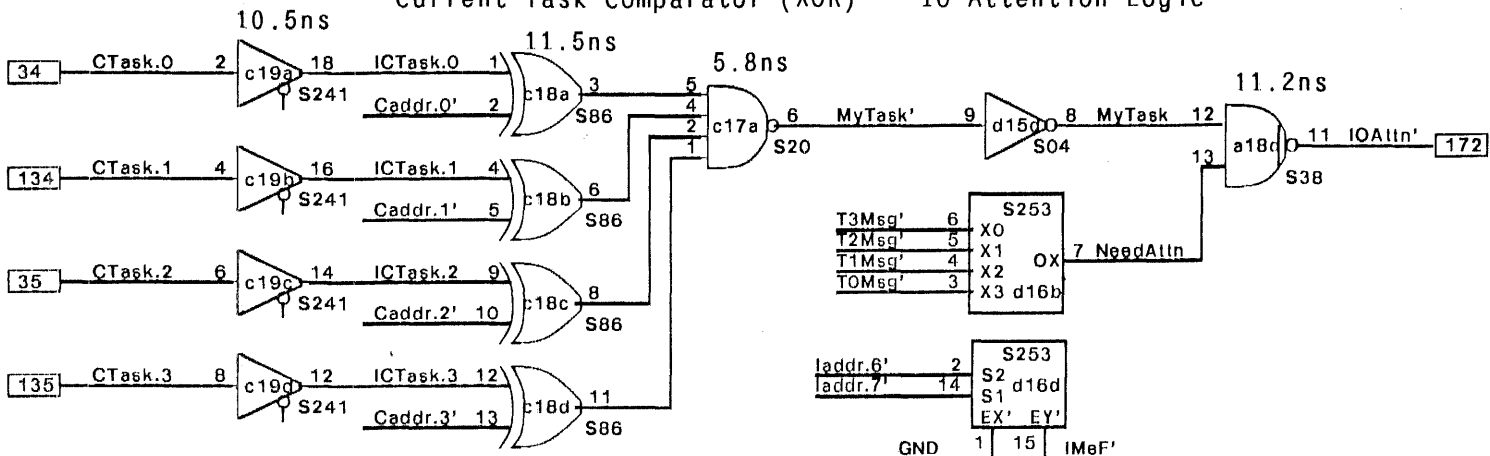


WakeUp Priority Encoding Logic19ns



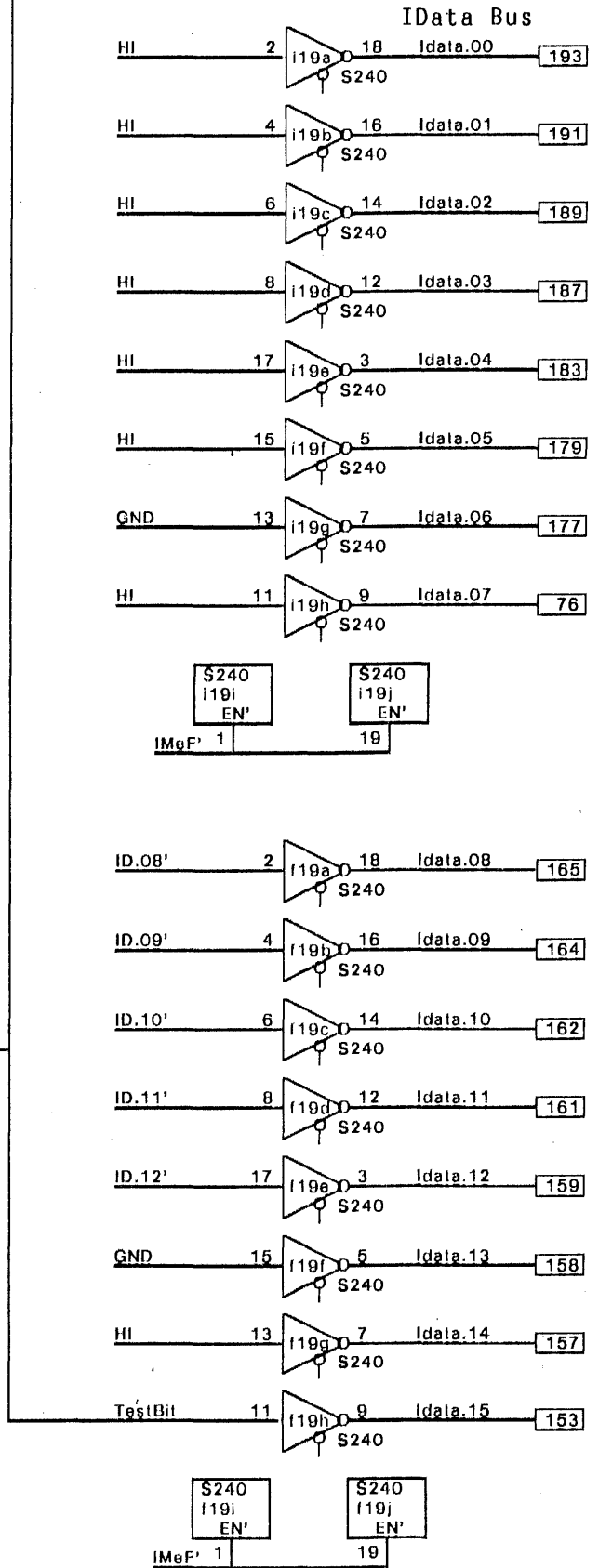
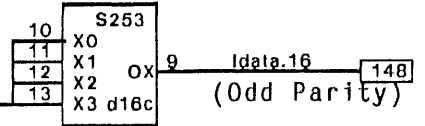
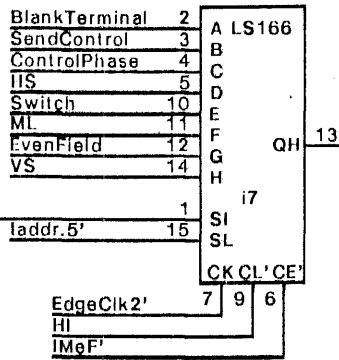
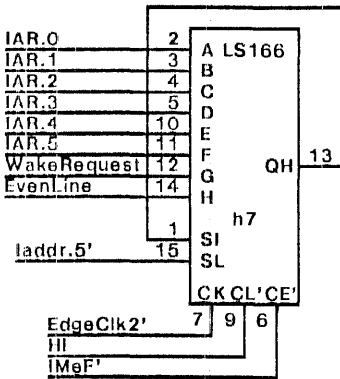
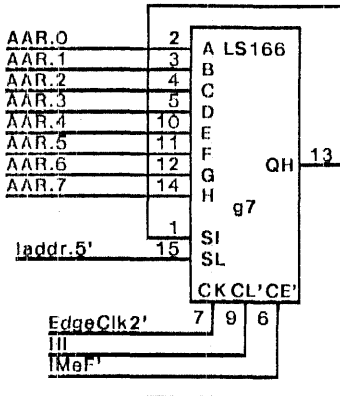
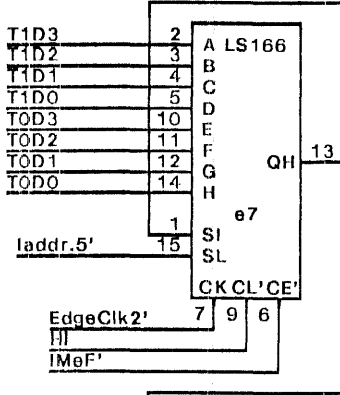
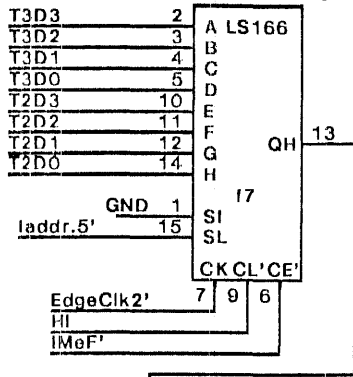
Current Task Comparator (XOR)

IO Attention Logic

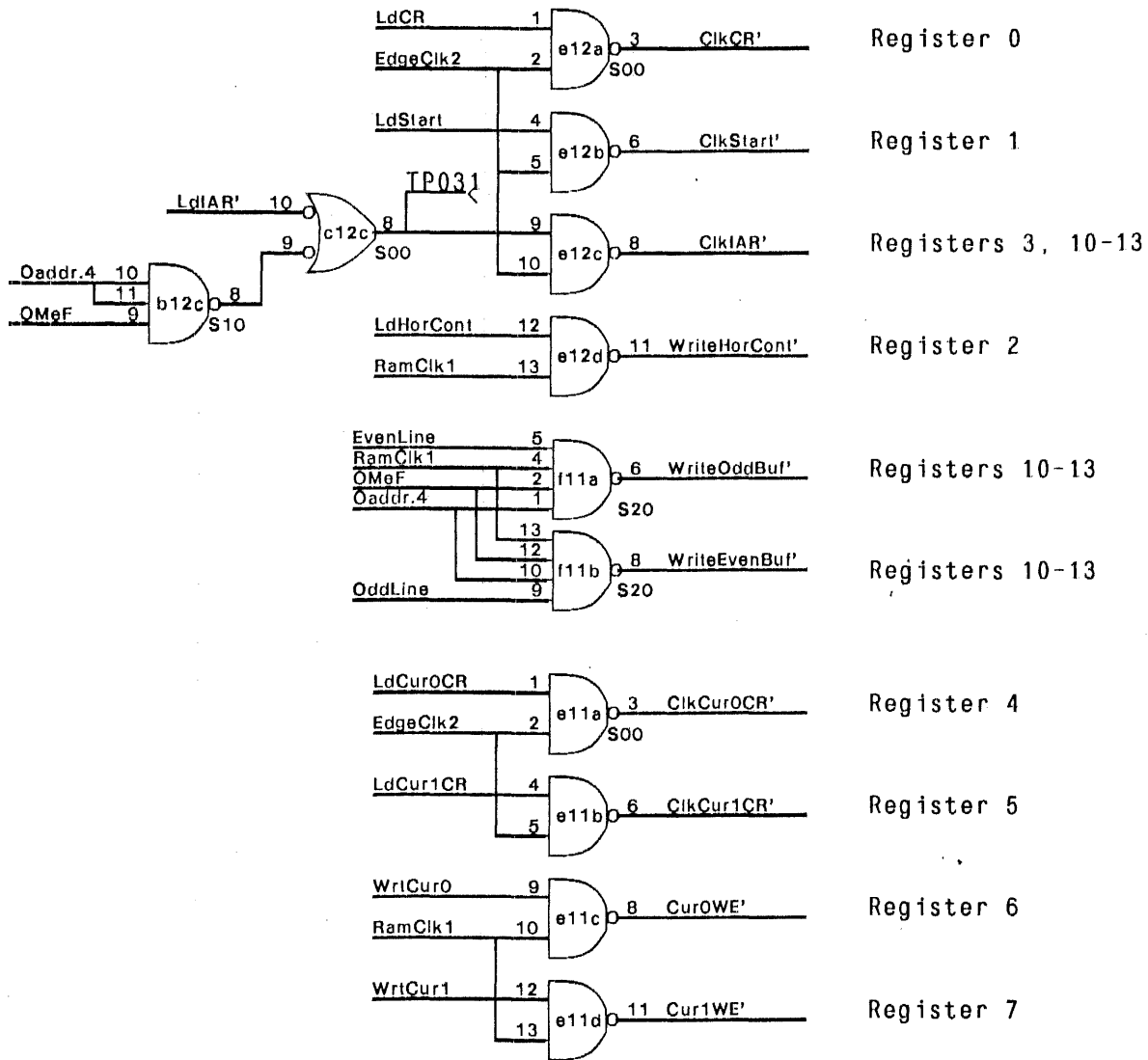




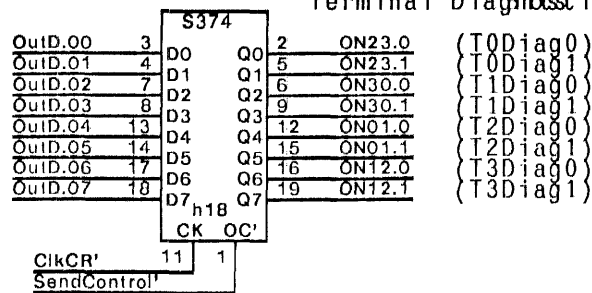
Test Shift Reg.  
(40-bit)



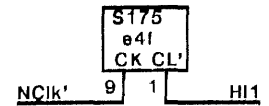
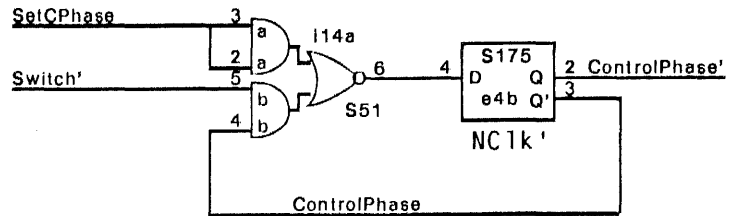
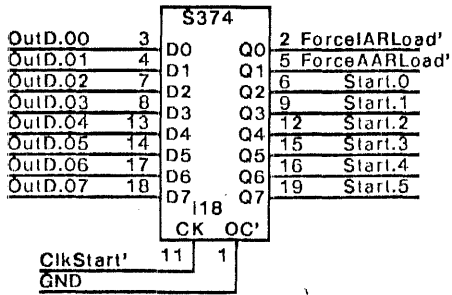
Note: Load: if Input Reg. with address > 4  
Shift: if Input Reg. with address < 4



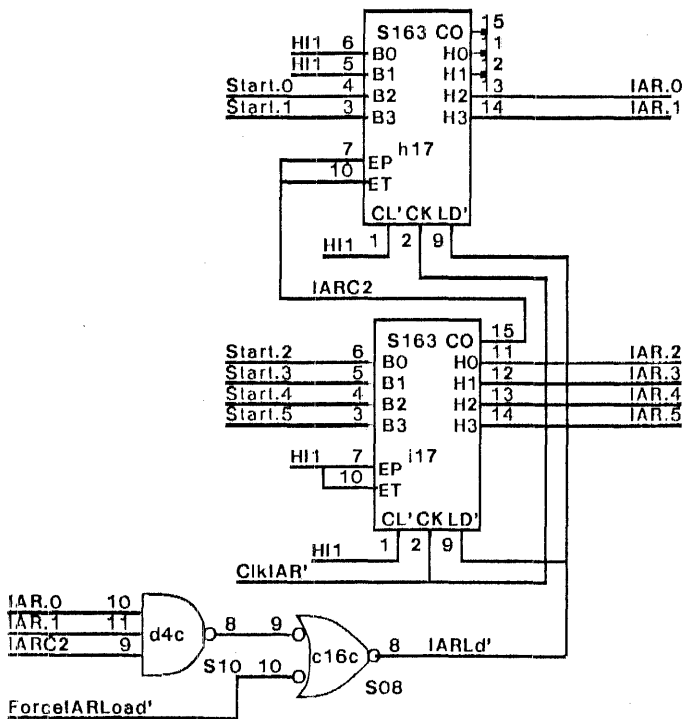
Diagnostic Reg.  
Tri-State  
Terminal Diagnostic



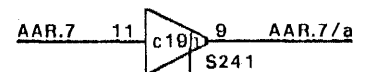
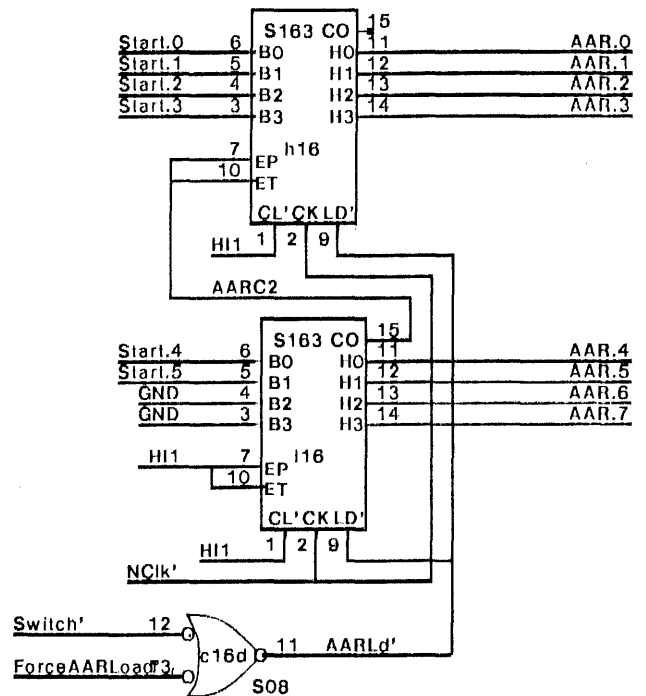
Starting Addr. Reg.



Inactive Addr. Reg.

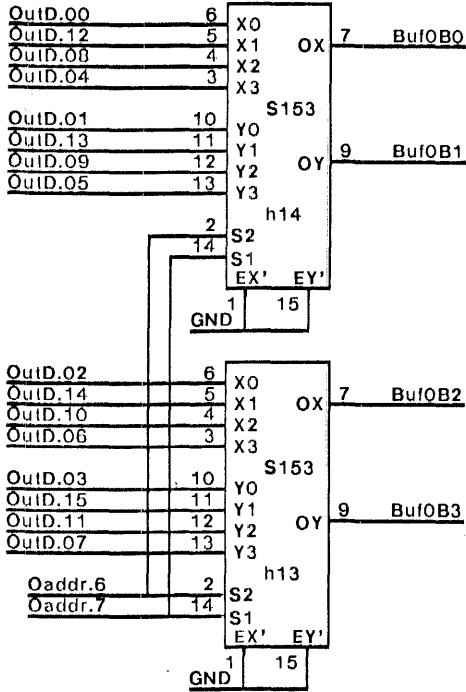


Active Addr. Reg.

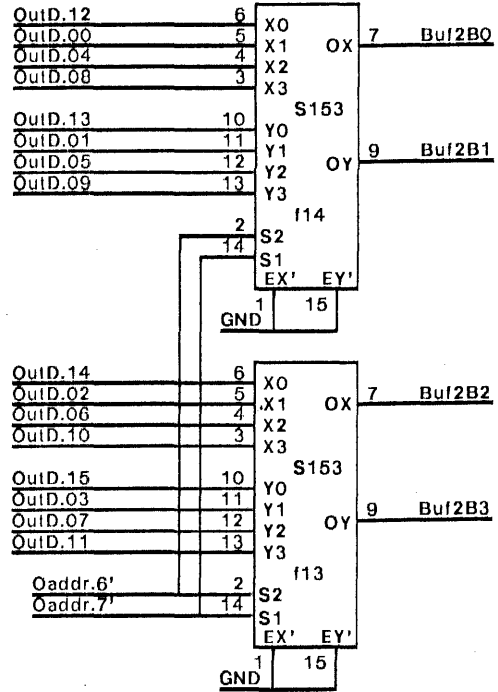




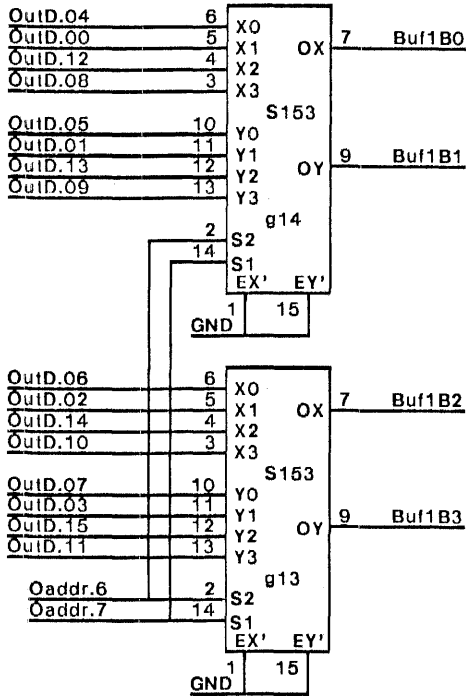
Input Shift Mux  
for Buffer 0



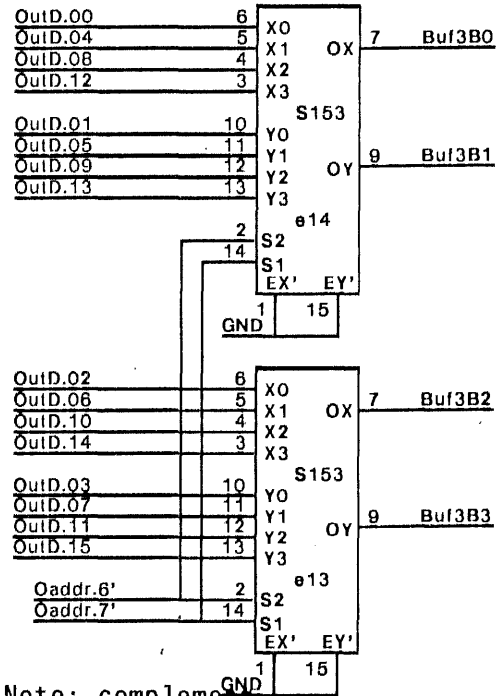
for Buffer 2



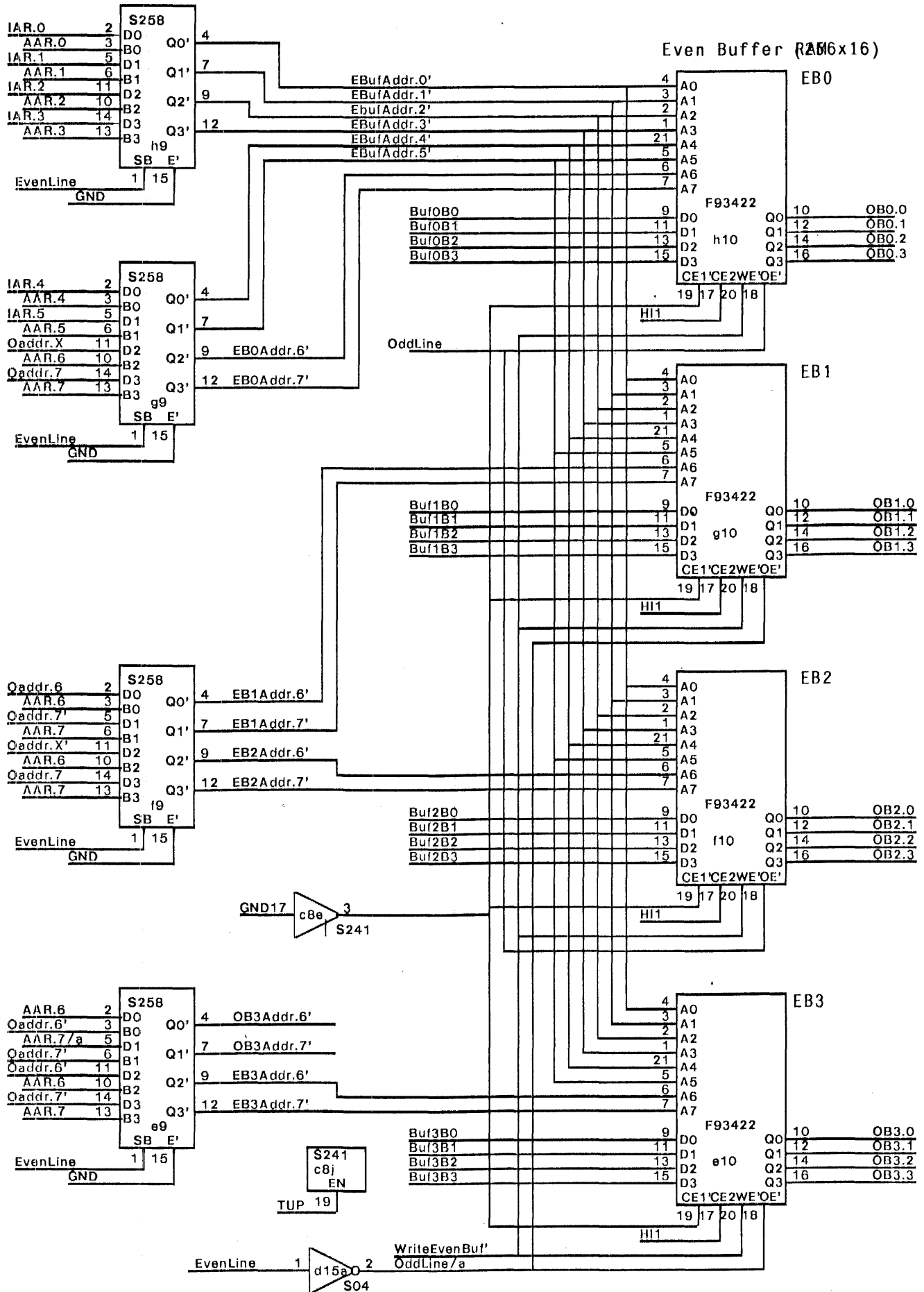
for Buffer 1



for Buffer 3

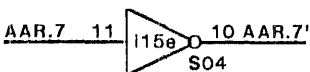
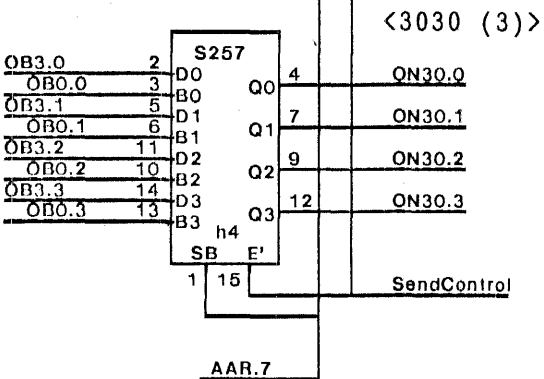
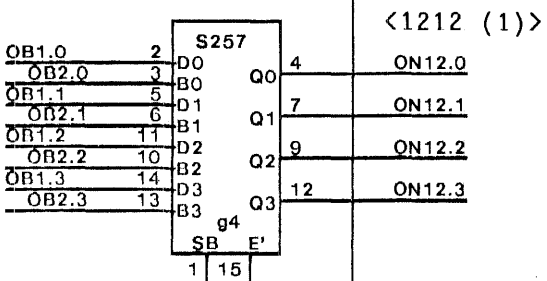
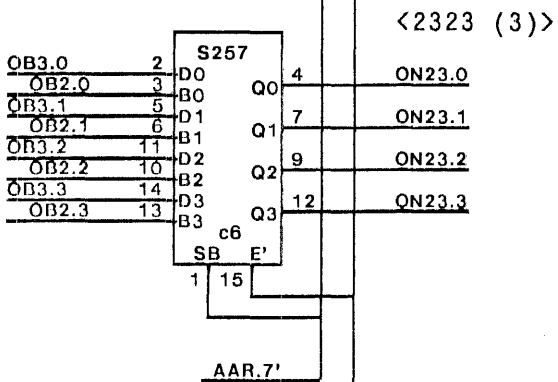
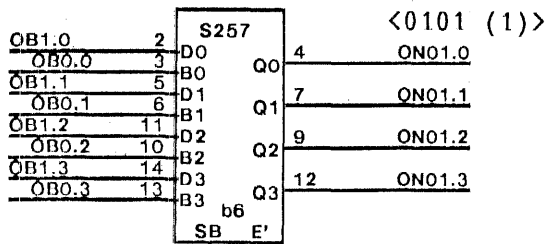


Note: complement  
Oaddr.6,7 lines  
used for better  
load sharing

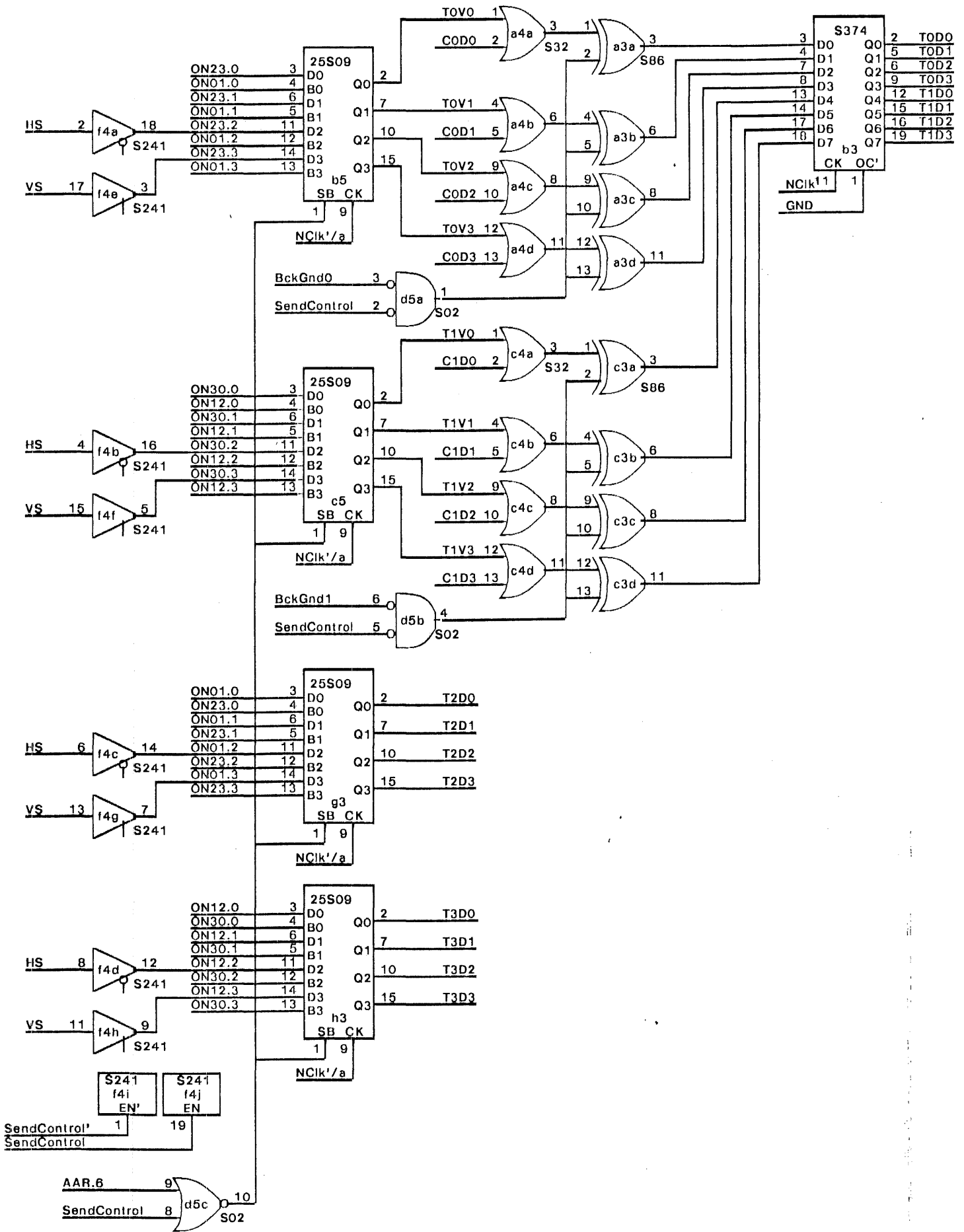


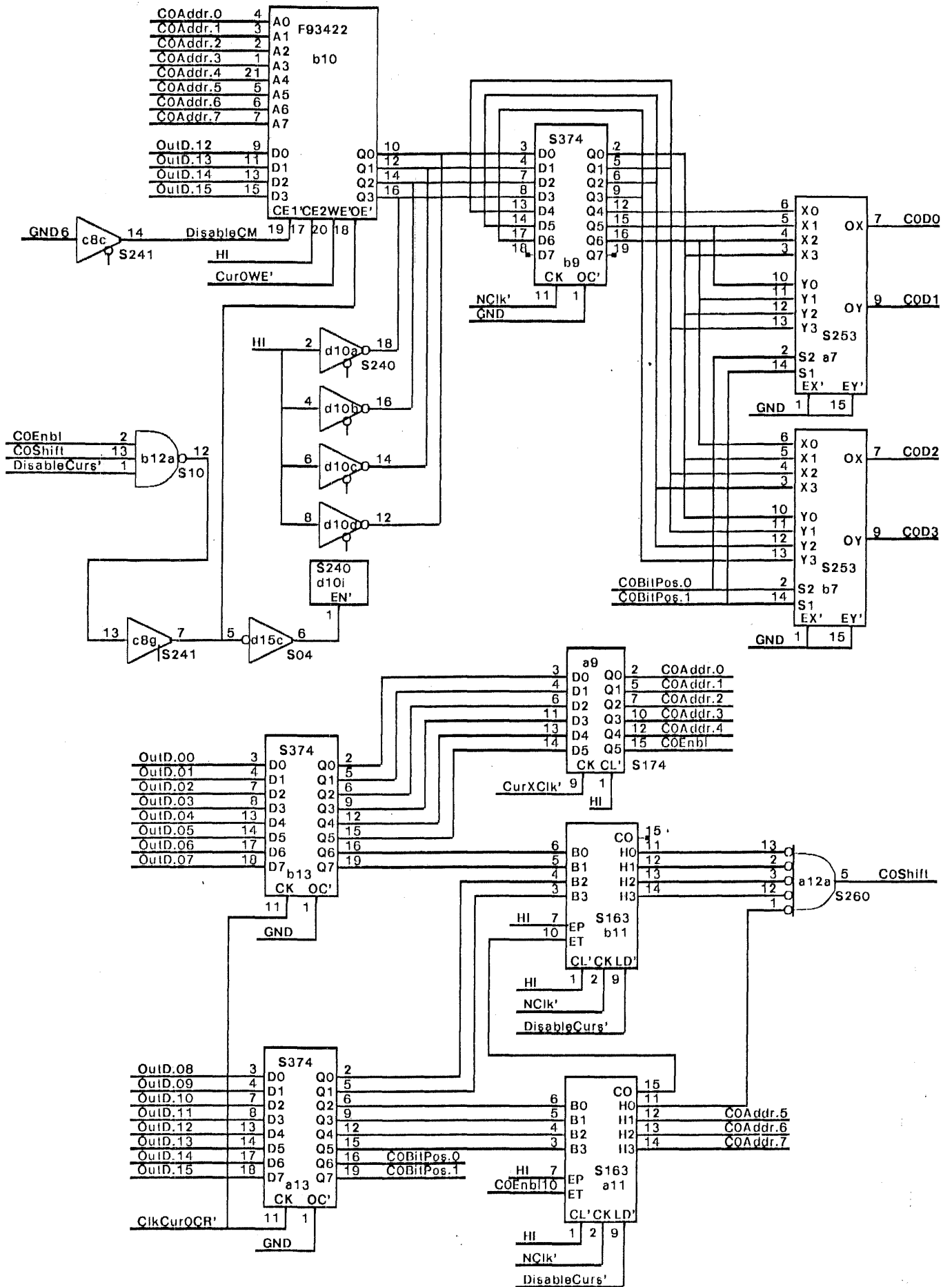


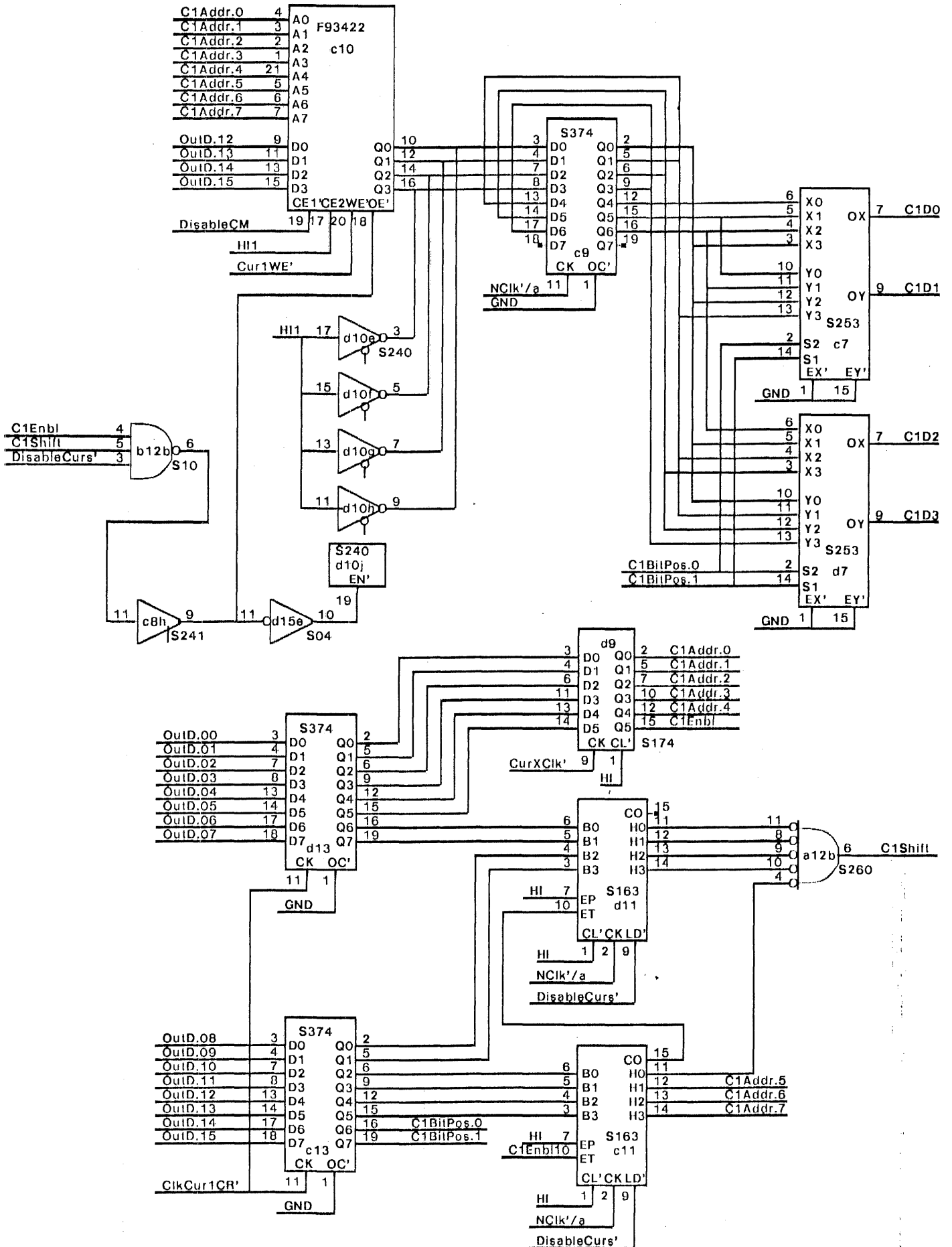
Tri-State

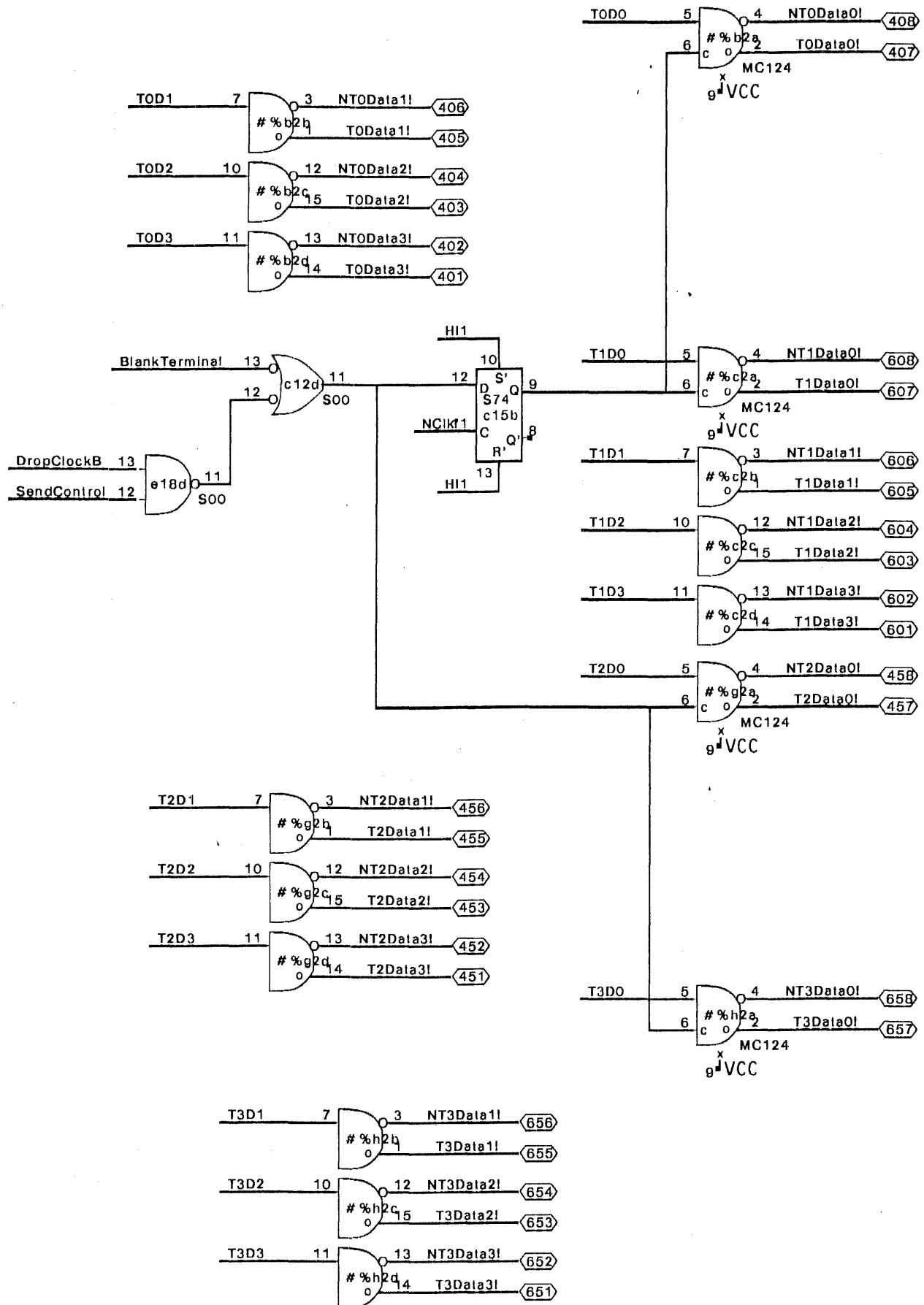




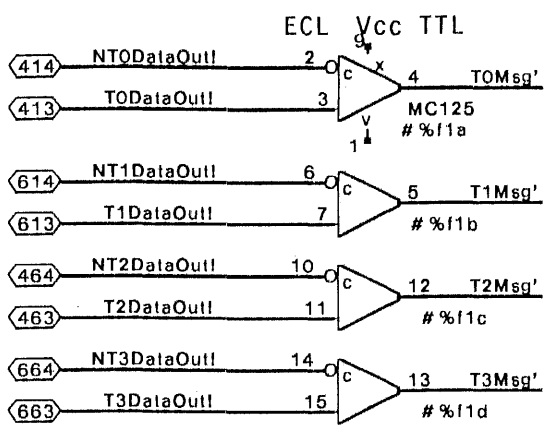
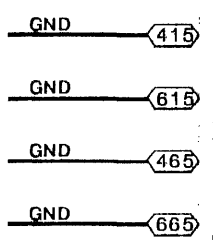
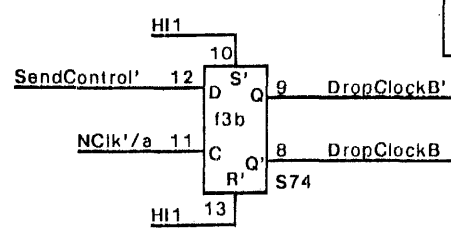
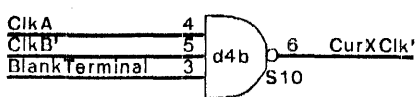
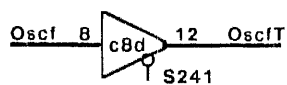
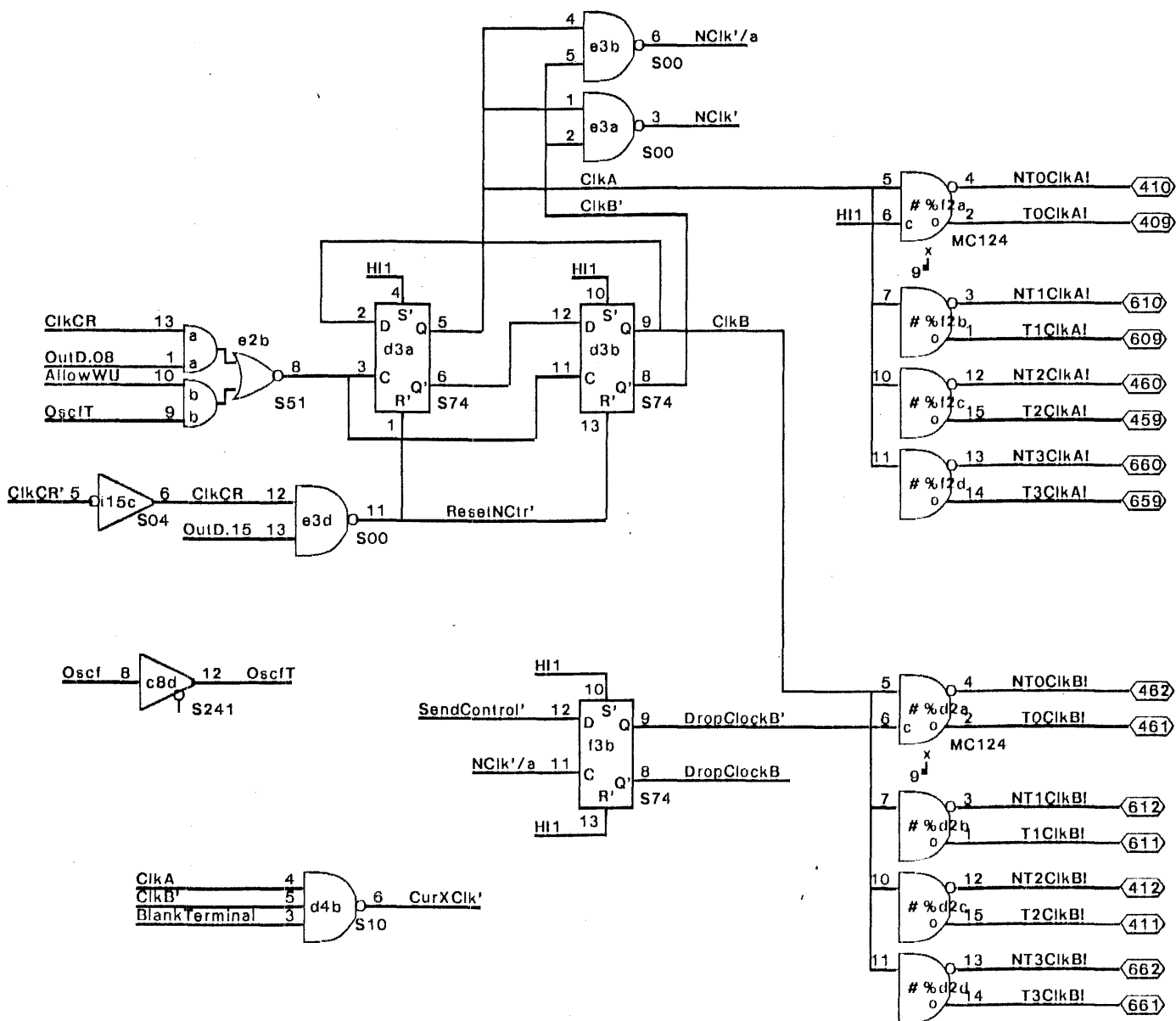




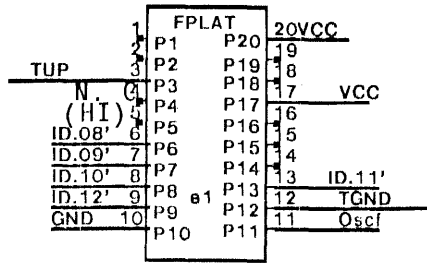




See page 17 for terminators



Oscillator & ID



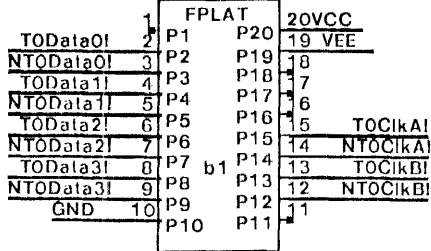
Note: 14-Pin crystal should be installed in this 20-pin platform as follows

Crystal	PLAT
Pin 1: N. C.	P4
7: GND	P10
8: Output	P11
14: +V dc	P17

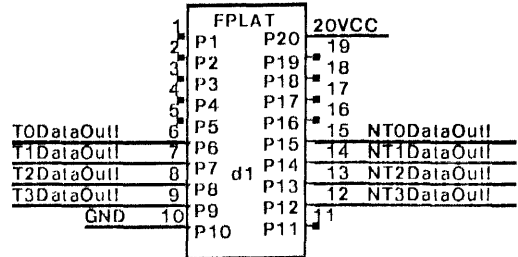
ID Modifier must have even number of p

Note: These platforms are shown as 20 pin units. They are actually 16 pin units with pin 8 of the network inserted into pin 9 of the 20-pin pattern. They are shown as 20 pins so that ROUTE will not try to cut any traces on the

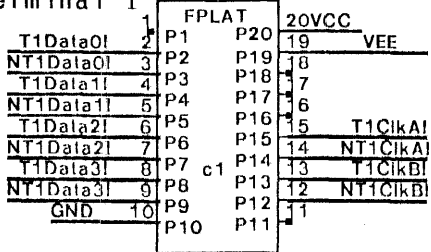
Terminal 0 220 ohm



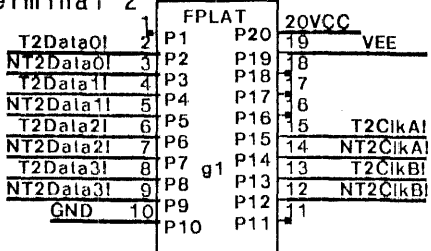
100 ohm



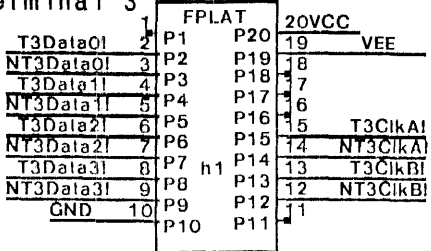
Terminal 1 220 ohm



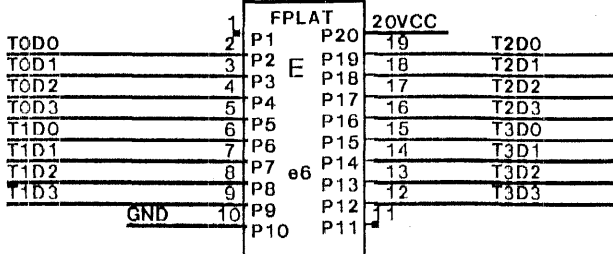
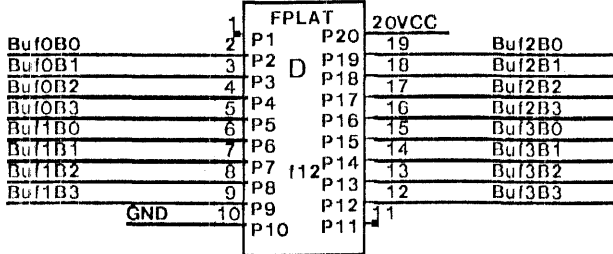
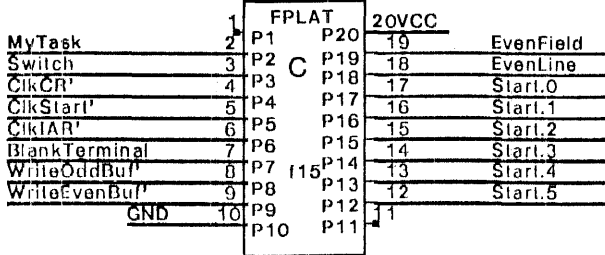
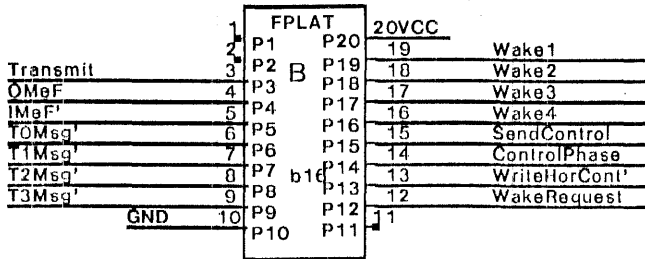
Terminal 2 220 ohm



Terminal 3 220 ohm

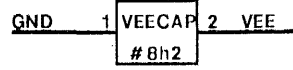
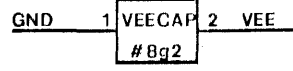
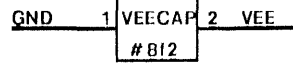
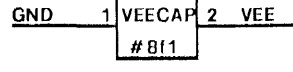
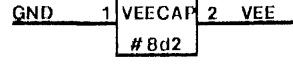
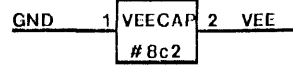
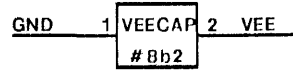


Test Clips:

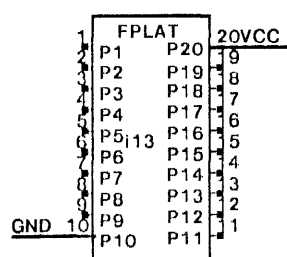
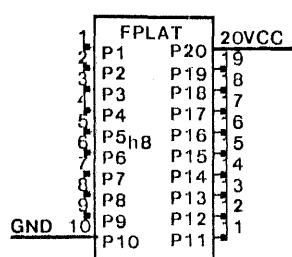
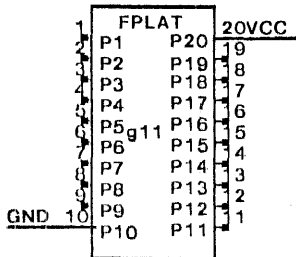
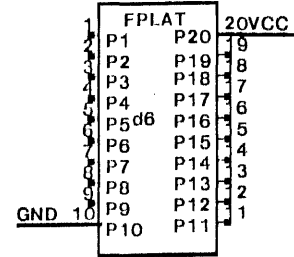
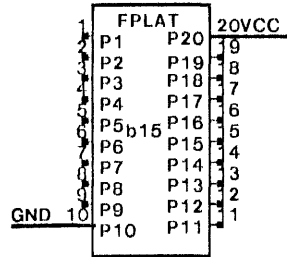
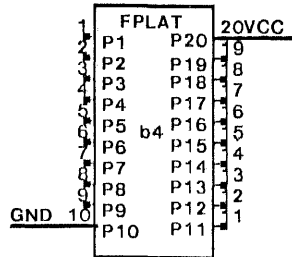
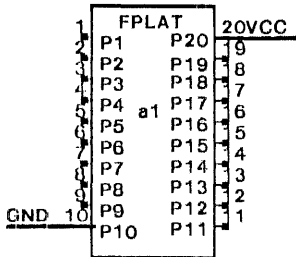


Filter Caps for ECL chips:

These capacitors mount between pins 2 and 19 of a 20 pin pattern due to the offset pr



Spare Positions (for Multiwire):



**Rev C:** Minor changes to logic found necessary during checkout.  
Re-layout to eliminate crossover of connections to I/O connectors.  
Made all I/O connectors male.  
Added hardware cursor to channels 1 & 2.  
All logic pages changed and renumbered.

**Rev D:** Synchronized BckGnd0 and BckGnd1 with Switch. Log. Dwg. p. 7.  
Added SendControl to Background control to maintain proper polarity of Control signals. Log. Dwg. p. 12.  
Changed control gate for Output shift register from S10 to S02. Log. Dwg. p. 6, 12, & 16.  
Changed Blank function in Control register to Unblank so that Rst' results in blanked display. Log. Dwg. p. 7.

**Rev E:** Page 05; OAddr4' input changed to OAddr4.OMeF and S10 gate (b12c) utilized for that .

Page 07; Control Register,PPUnblank changed to PPBlank,EnOsc changed to Allow WU, S74

(c15a) deleted

Sync CR - PUnblank changed to PBlank

S00 (e18d) changed to S02 (d5d).ControlPhase' input changed to ControlPhase.

Inverter (i15f) used instead of S02 (d5d).New wire EnbCurs' added.

Page 13; SendControl' changed to EnbCurs' on the input of S10 (b12a) and load inputs of S163 (b11 and a11). Typo corrected - Output control inputs on b13 and a13 changed from Hi to GND

Page 14; SendControl' changed to EnbCurs' on the input of S10 (b12b) and load inputs of S163 (d11 and c11). Typo corrected - Output control inputs on d13 and c13 changed from Hi to GND

Page 15; SendControl' input on S00 (c12) changed to DropClockB.SendControl,and S00 gate added (e18d)

Page16; NCik gate input changed from ClkB to ClkB'. EnOsc input on S51 changed to Allow WU

DropClockB' signal added on the output of S74 (f3b). S10 gate (d4b) added to produce CurXCik'. Corrected typo - OutD.09 changed to OutD.15 on the input os S51

Page 17; Pullup and pulldown resistors added to the Crystal Plat (also in UTVFCSplats.sil)

Added test chip S241 in loc.c8. Its symbols are scattered on several pages. Added test points on most pages.

**Rev F:** Corrected error made in adding the test points on page 9 and 10. Changed EdgeClock2' to EdgeClock1' (Eich layout-related)on p.2.Changed S166 to LS166 on page 4.Cosmetics on p.17.

**Rev G<sub>a</sub>** created from Rev F by CPT on 3/25/79:

Renamed EnableCurs' to be DisableCurs'

Removed Test points from diagrams.

Reversed ECL chips so that pin 16 (gnd) will be trace-wired.

Made all platforms 20pins so that ROUTE will not do any cuts.

Added spare 20pin positions (for Multiwire) in a1,b4,b15, d6, g11, h8, and i13.

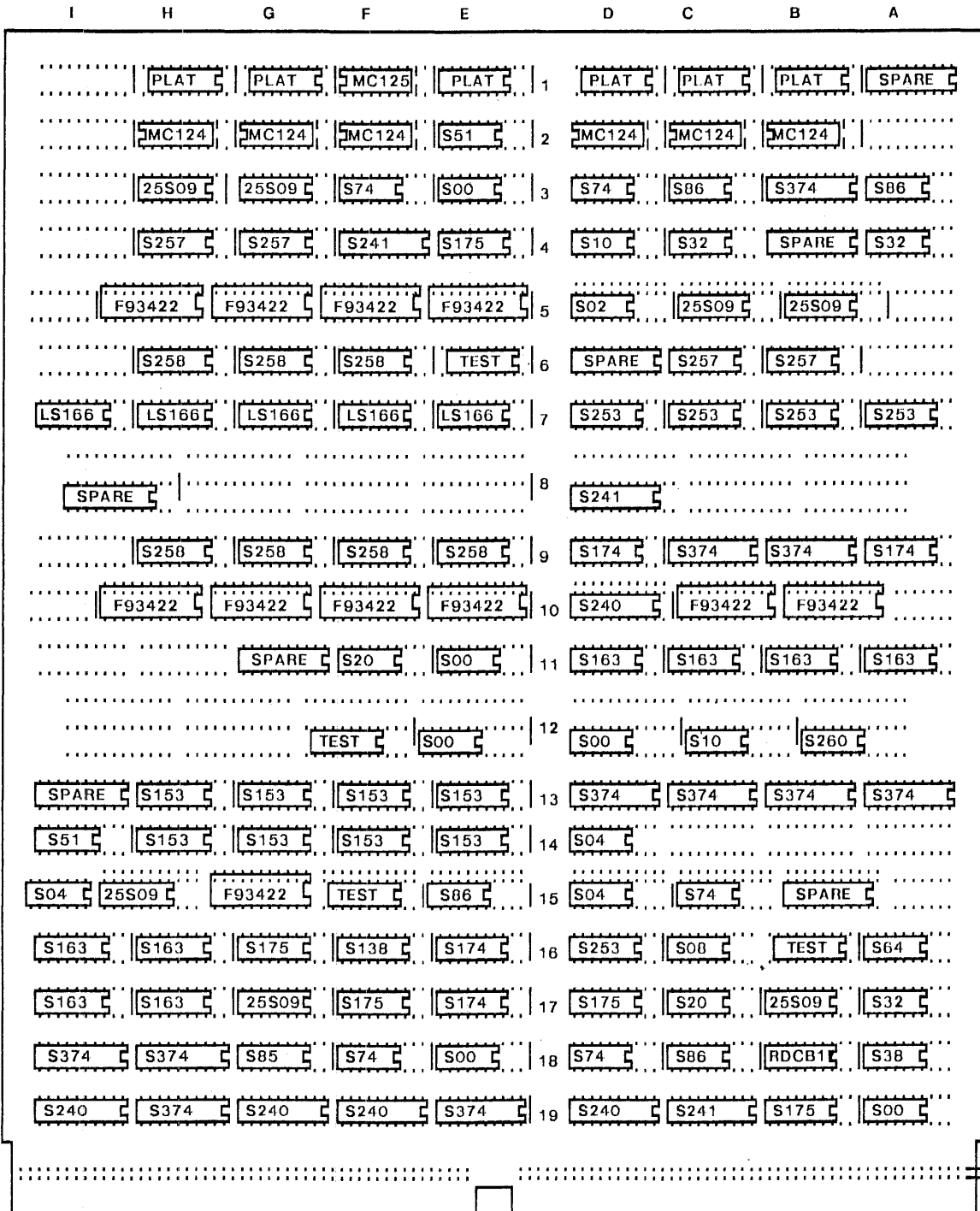
Changes for revision G<sub>b</sub> (7/18/80 - CPT)

1) Connected pin 15 of all 4 terminal connectors to ground (p 16).

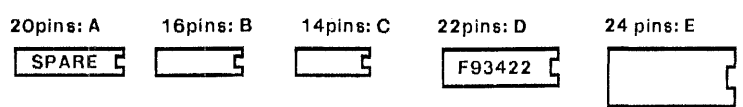
2) Created latched signal MyStrobe' (pg. 3).



Note: The I/O connector area is loaded with 4 15pin MALE D-series connectors.  
 Note: All platforms except e1 have pin 8 of the platform in pin 9 of the pattern.  
 Note REVERSAL of all ECL Chips (MC124, MC125)



101-200  
1-100

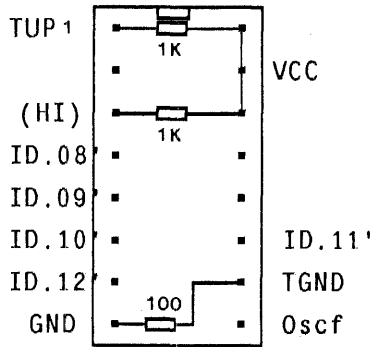


16 pins REVERSED: F  
 Typical of ECL chips

Note: The short vertical lines indicate filter capacitor locations. (103 Total)

Broken vertical lines indicate VEE filter caps for ECL chips. These are mounted from pin 2 or pin 19 of the 20 pin pattern. (7 total)

Platform e1 (oscillator):



Note: The oscillator is mounted on the platform as follows:

Oscillator Pin number	Platform Pin number
1	2
7	8
8	9
14	15

Oscillator is Motorola K1100A series

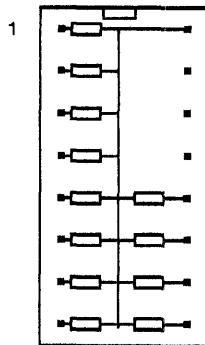
Note: ID.08' - ID.12' are wired to HI (pin 3) or Gnd (pin 8) depending on the oscillator frequency as follows:

Oscillator f:	50mhz	20mhz					
ID.08' (pin 4)	Hi	Hi					
ID.09' (pin 5)	Hi	Hi					
ID.10' (pin 6)	Hi	Gnd					
ID.11' (pin 11)	Gnd	Hi					
ID.12' (pin 7)	Gnd	Gnd					

Platforms b1, c1, g1, h1

Xerox P/N 703W11691 (15 resistors) is acceptable

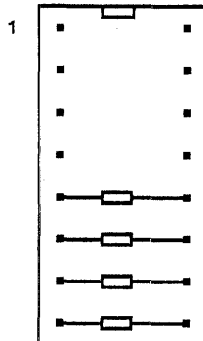
All resistors 220 ohm, 1/4 w.



Platform d1:

Xerox P/N 703W00891 (8 resistors) is acceptable substitute

All resistors 100ohm 1/4 or 1/8 watt, 10%



## Interface to D0 chip tester

.G.T.T. Pgrp . Data .  
1 2 5 8

G -- Go bit (if on, start clocks following this instr.)

TT -- Type of instr:

- 0 -- Other (Pgrp is further decoded, see below)
- 1 -- Load Data into "Enable" reg. for indicated Pgrp
- 2 -- Load Data into "Data A" reg. for indicated Pgrp
- 3 -- Load Data into "Data B" reg. for indicated Pgrp

Pgrp -- Pin Group. Selects (except in "Other" type instrs) the group of 8 pins affected by the instruction.

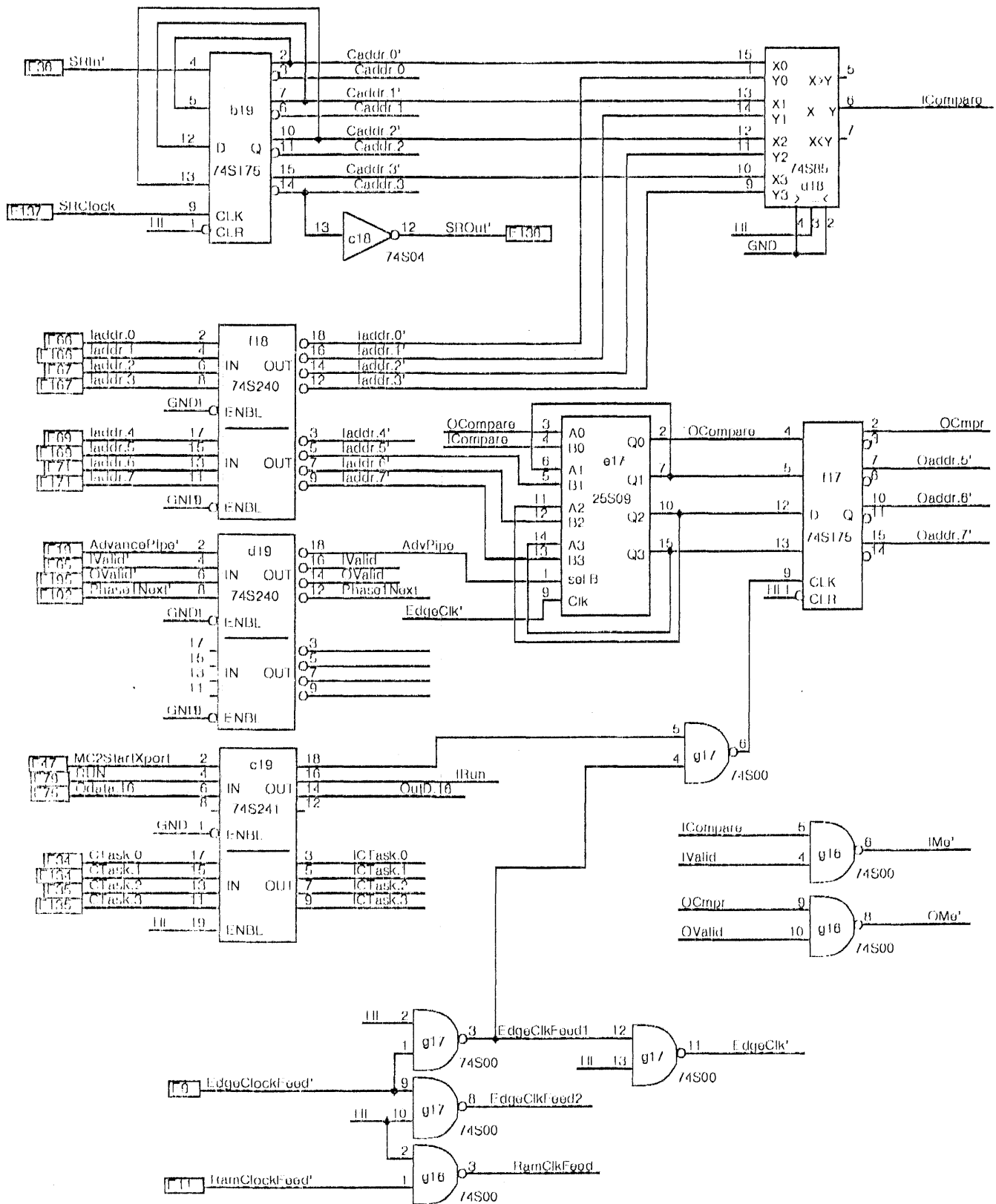
Other group:

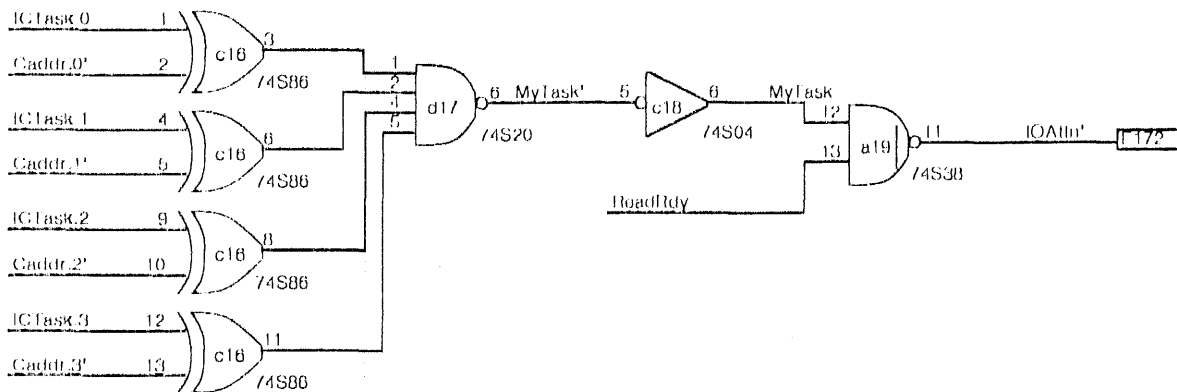
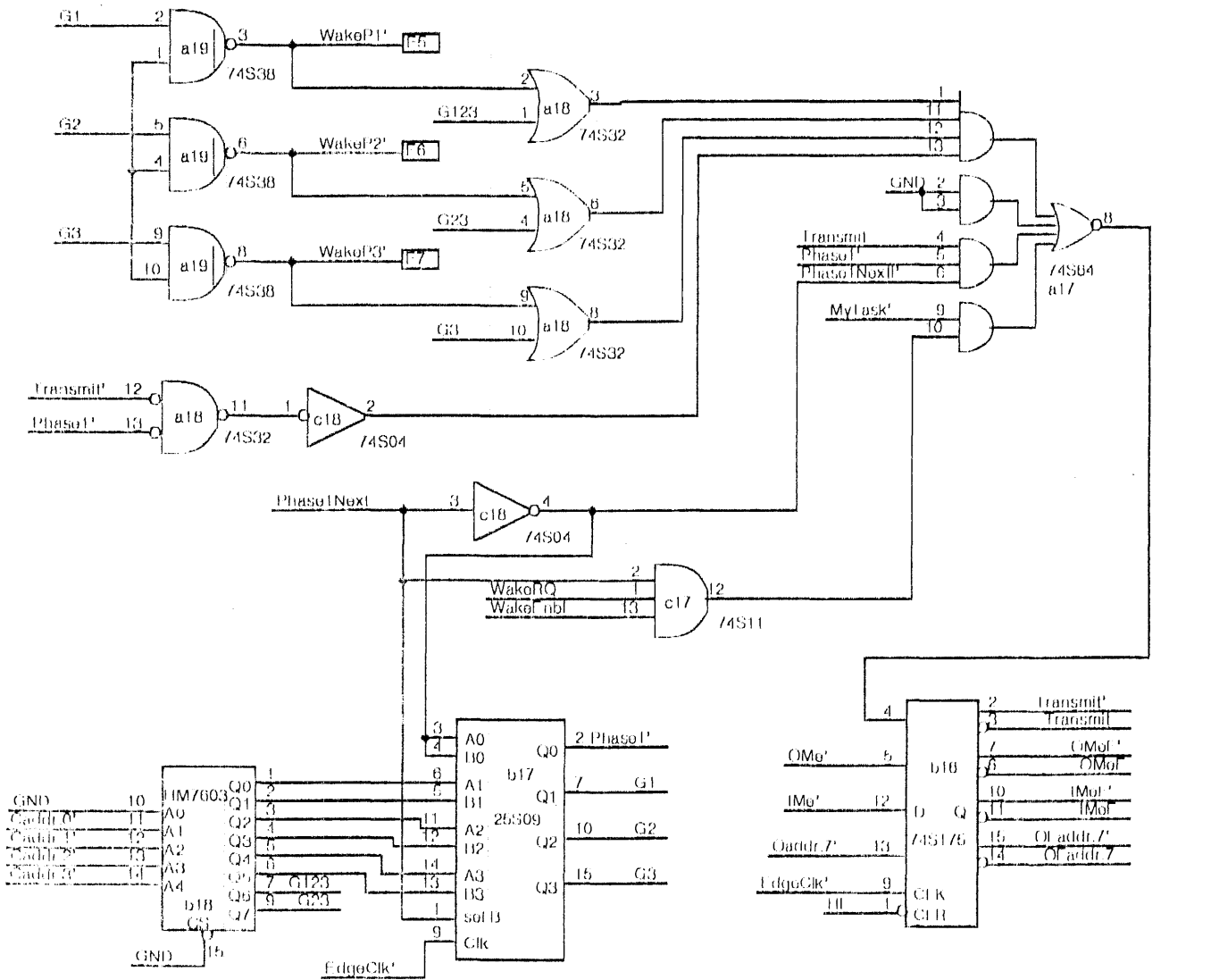
Pgrp: .X.X.I.C.C.

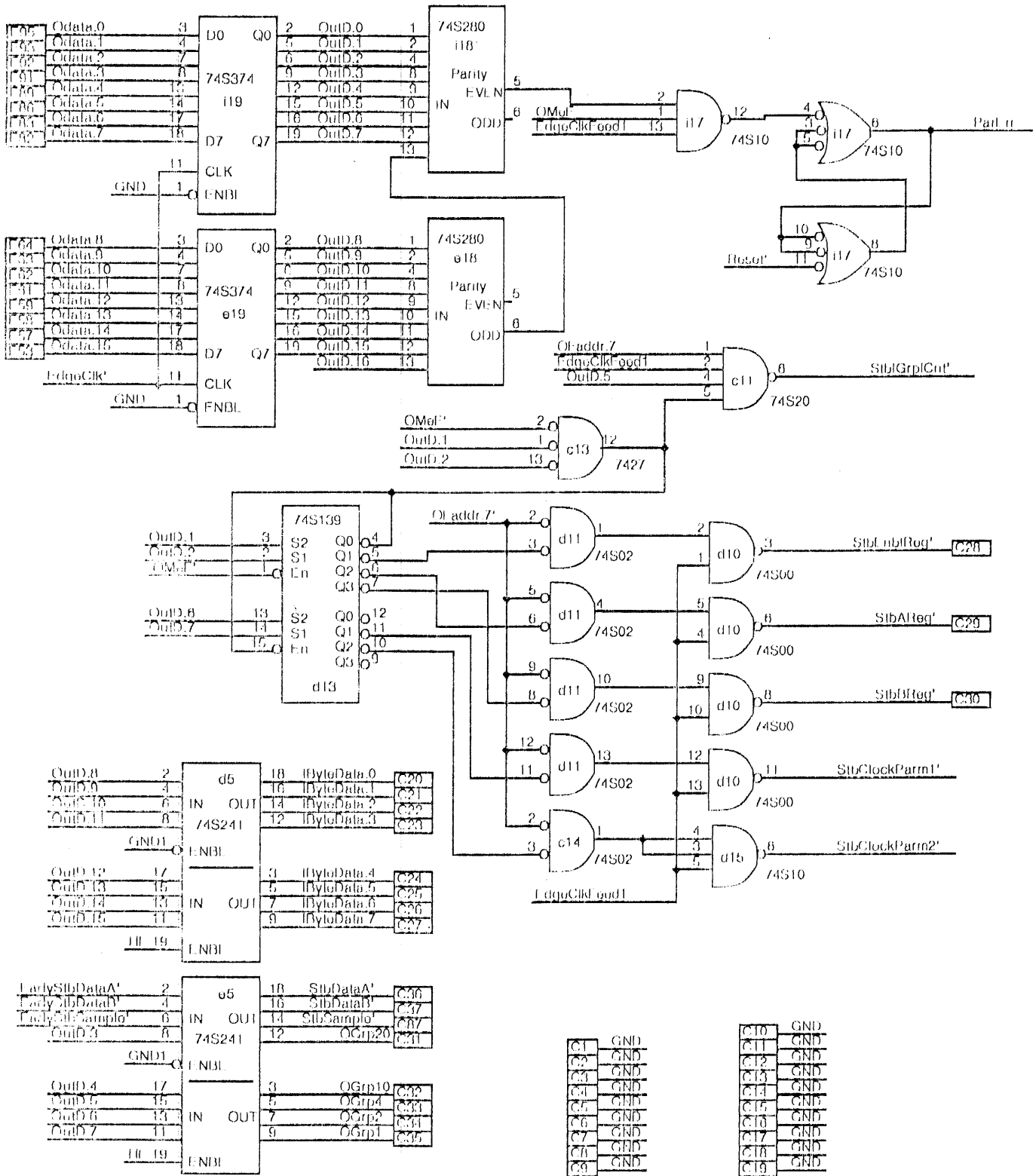
CC -- Clock parameter select:

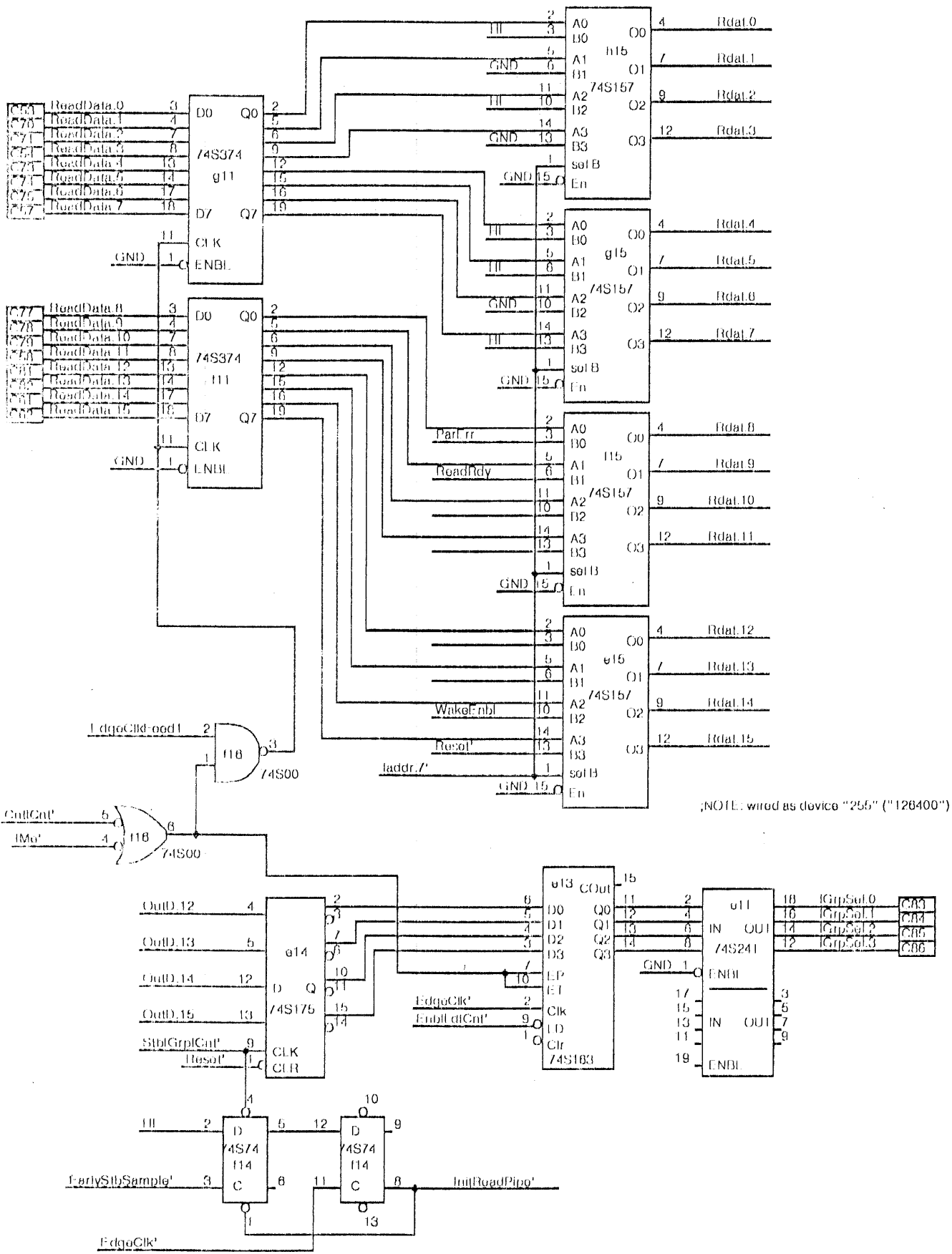
- 0 -- None (nop)
- 1 -- Load Data into clock Parameter Reg. 1
- 2 -- Load Data into clock Parameter Reg. 2
- 3 -- Load Data into clock Parameter Reg. 3

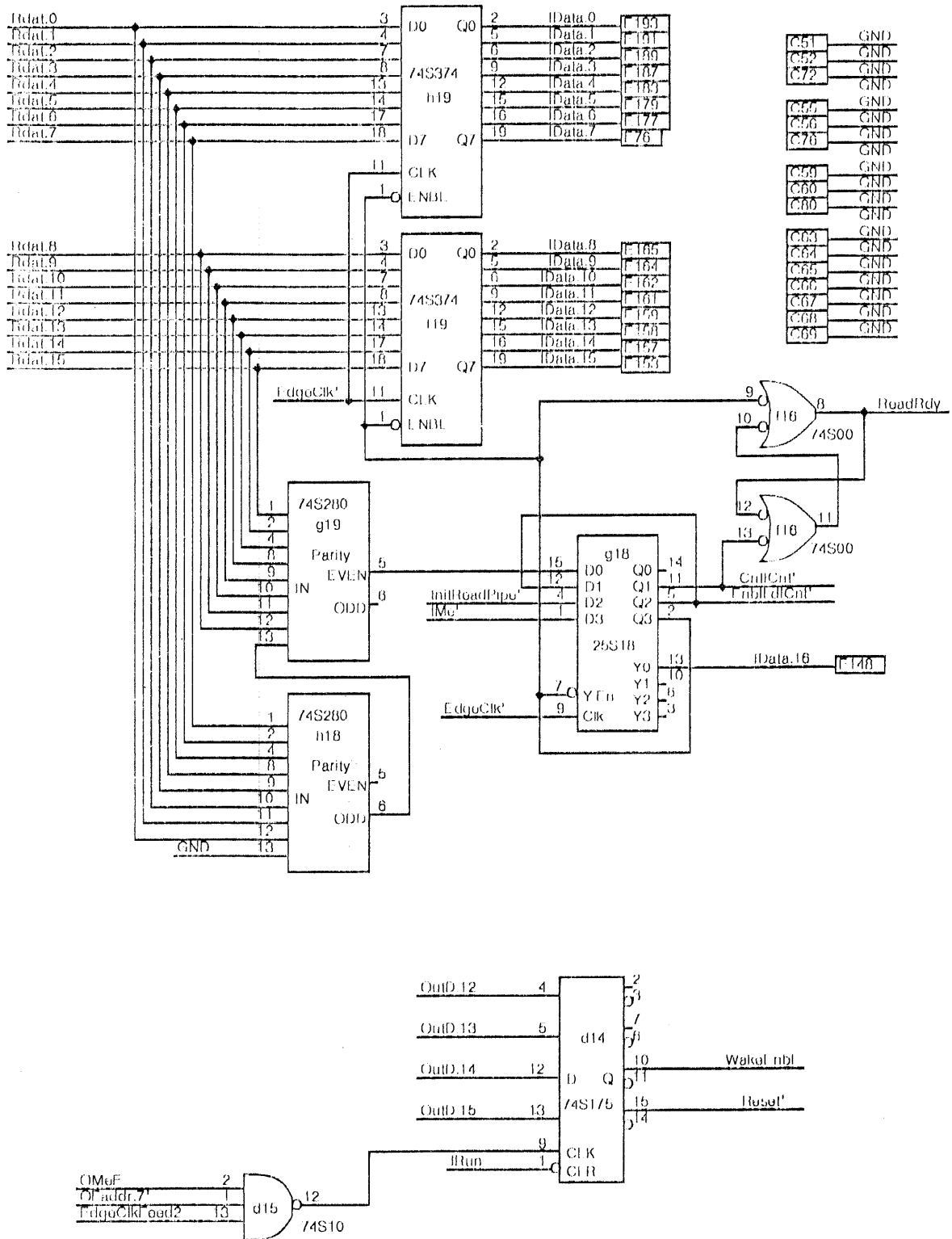
I -- Load Data into Input Group Select Counter



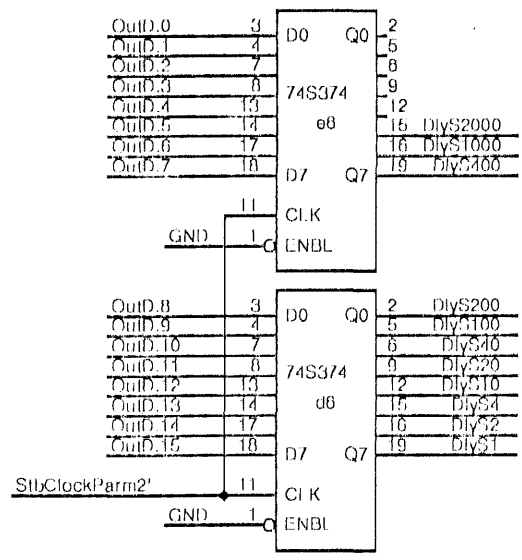
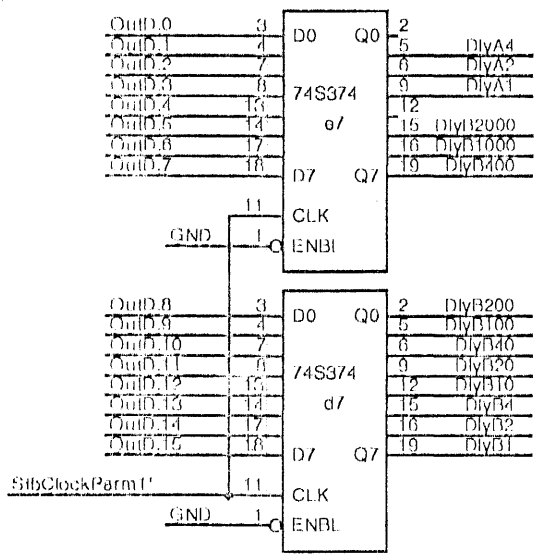
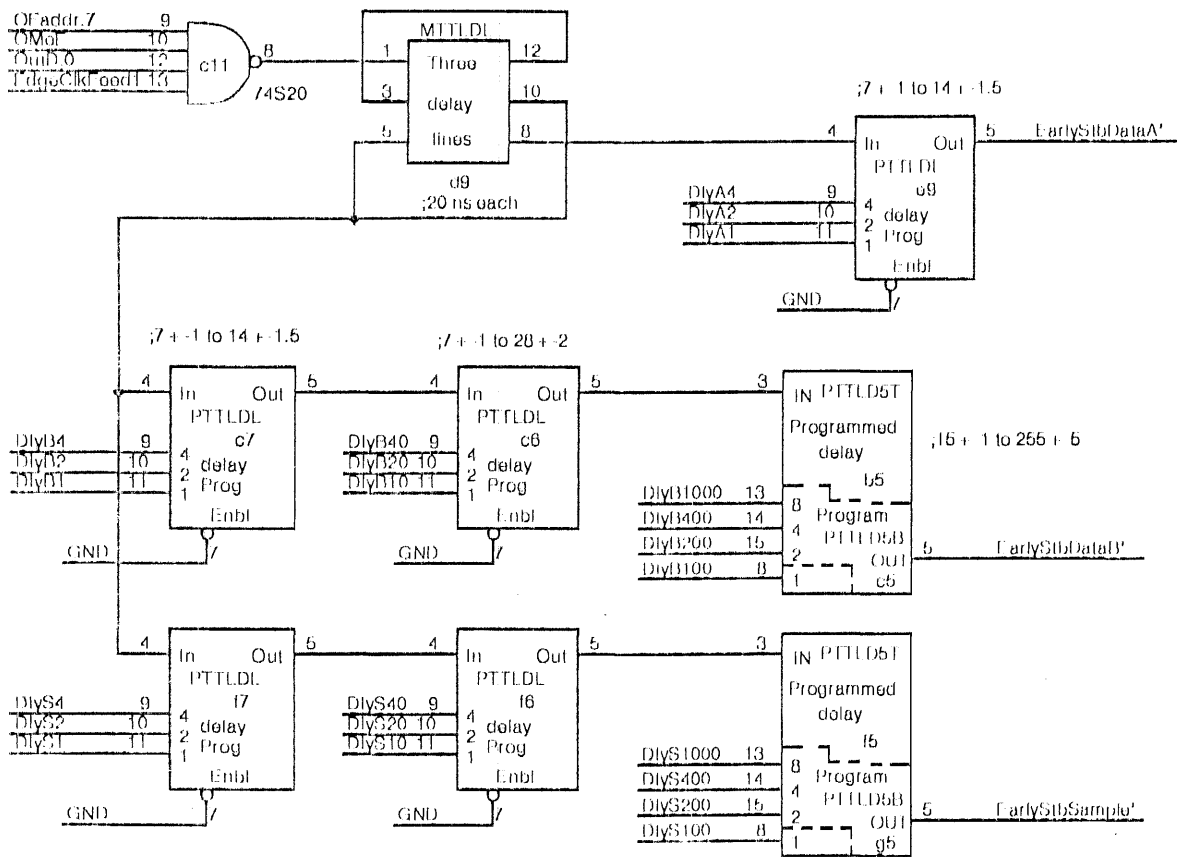




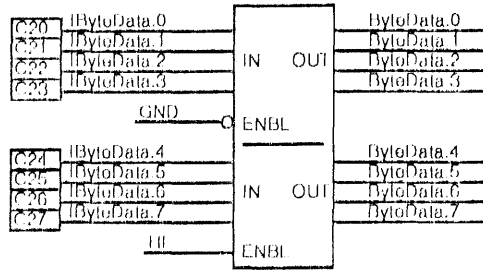




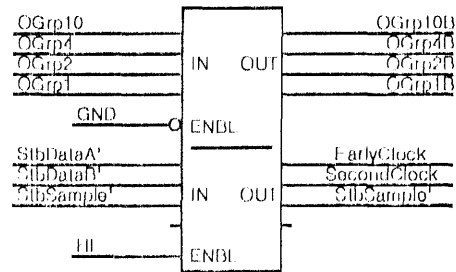




C73	RoadData.0
C76	RoadData.1
C71	RoadData.2
C74	RoadData.3
C73	RoadData.4
C74	RoadData.5
C75	RoadData.6
C77	RoadData.7



C77	RoadData.8
C78	RoadData.9
C79	RoadData.10
C78	RoadData.11
C81	RoadData.12
C82	RoadData.13
C81	RoadData.14
C82	RoadData.15



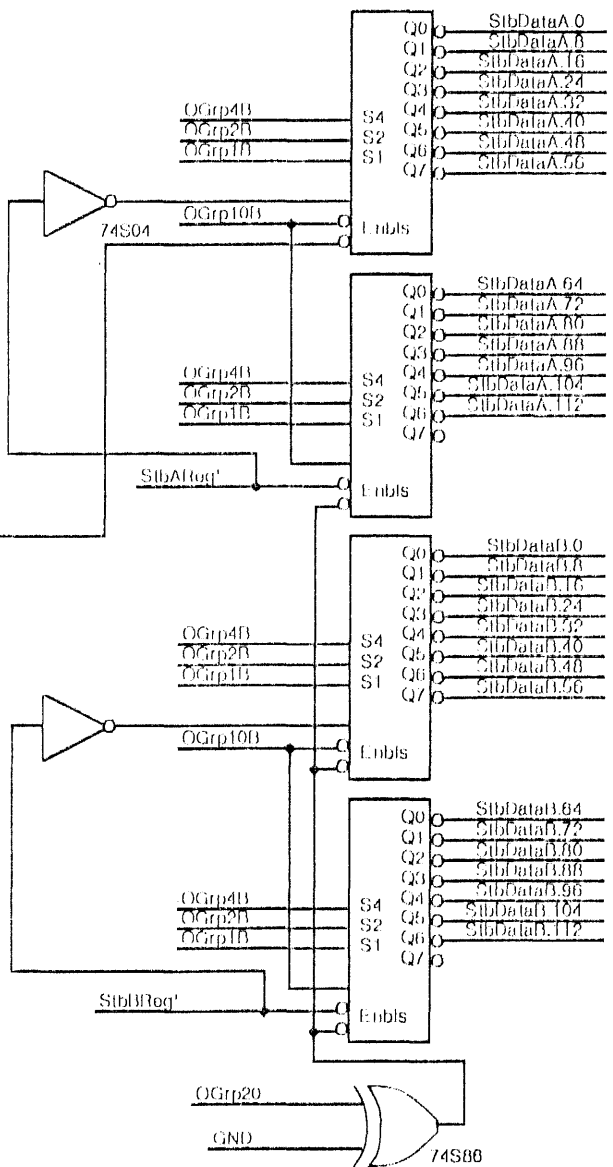
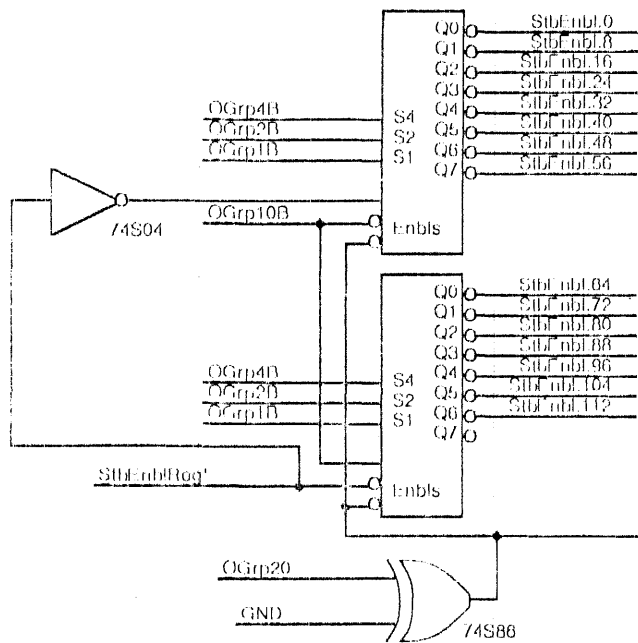
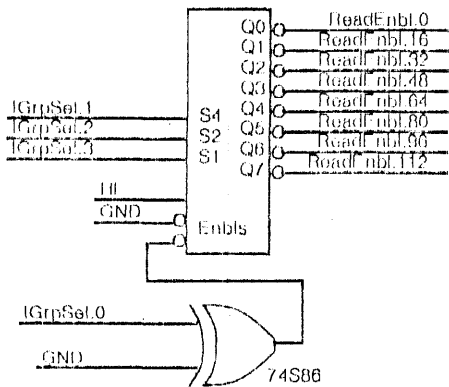
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StbAReq'	C29
StbBReq'	C30

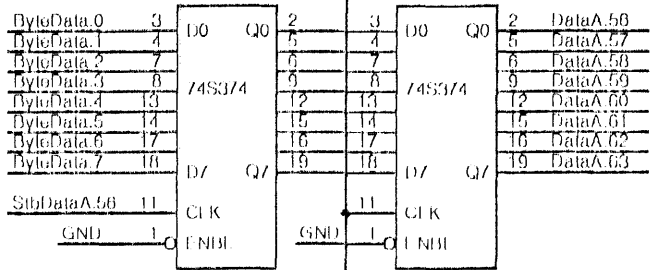
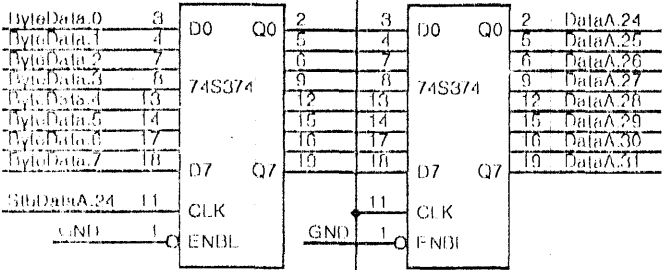
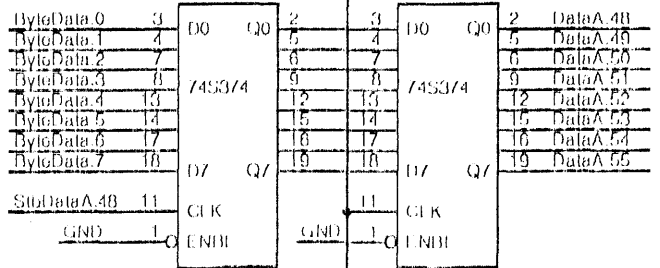
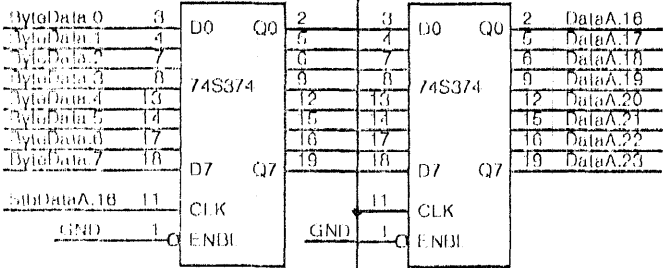
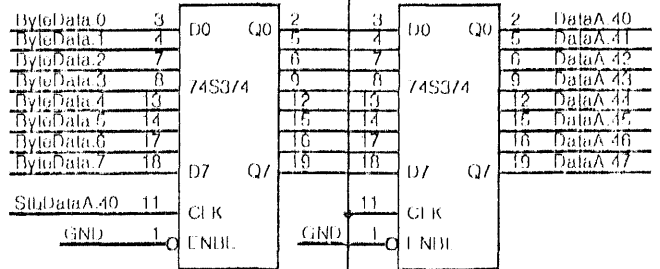
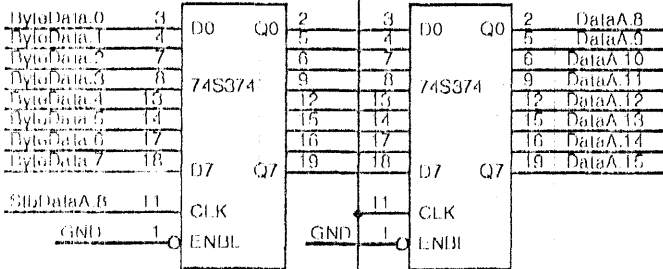
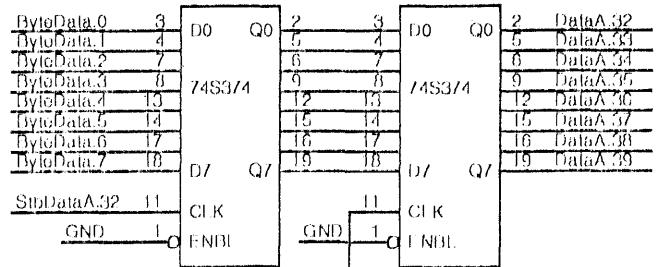
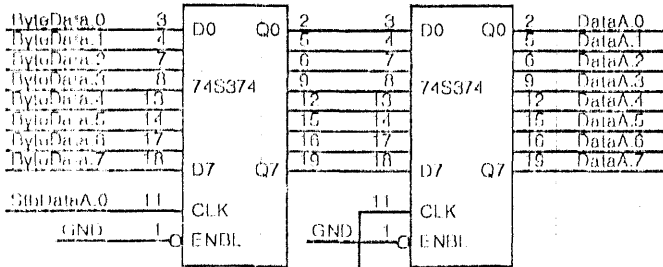
IGrpSel.0	C83
IGrpSel.1	C84
IGrpSel.2	C85
IGrpSel.3	C86

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StbDataB'	C37
StbSample'	C87
OGrp20	C31

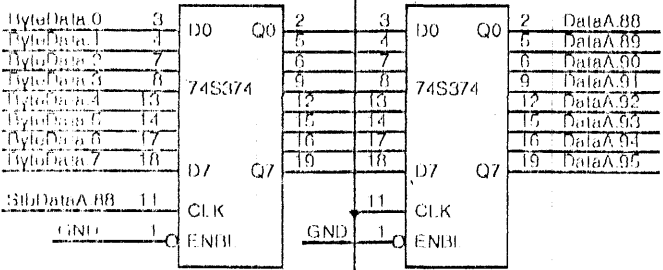
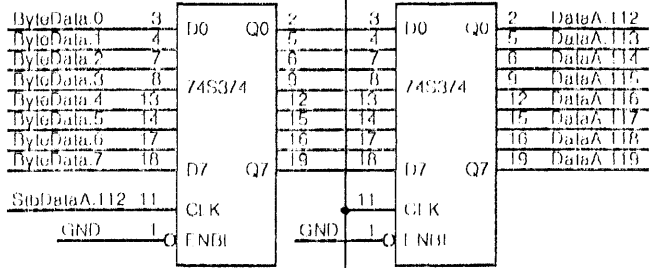
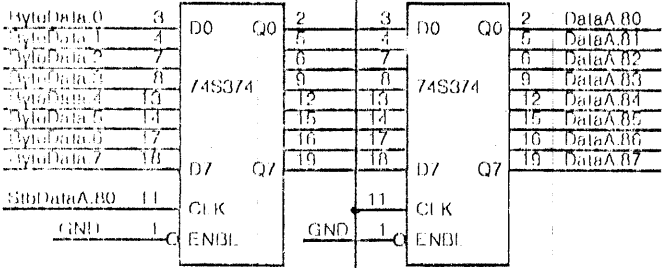
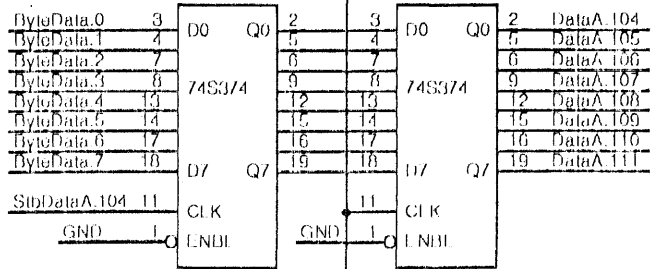
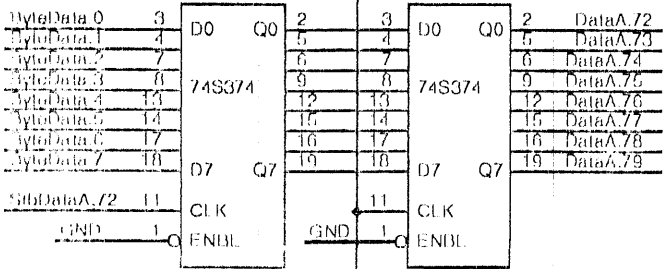
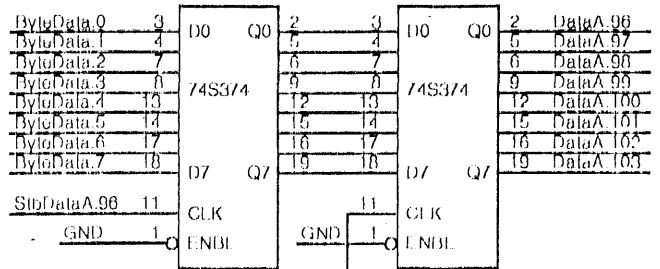
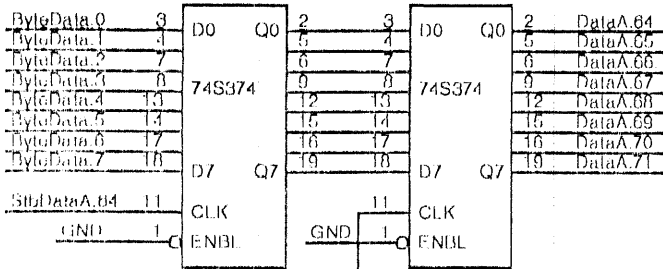
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OGrp2	C34
OGrp1	C35

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C3	GND	C72	GND
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C5	GND	C65	GND
C6	GND	C66	GND
C7	GND	C76	GND
C8	GND		GND
C9	GND	C69	GND
		C60	GND
C10	GND	C80	GND
C11	GND		GND
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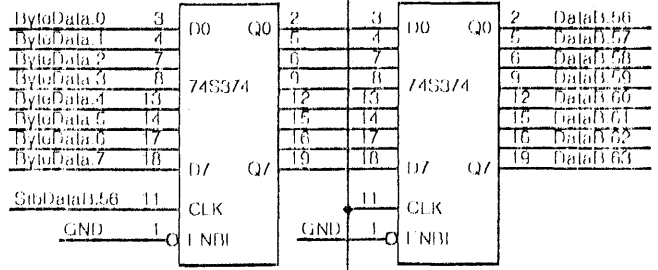
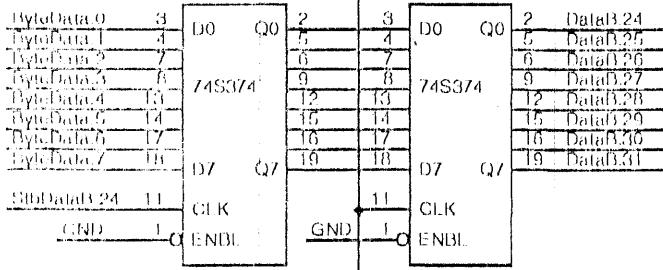
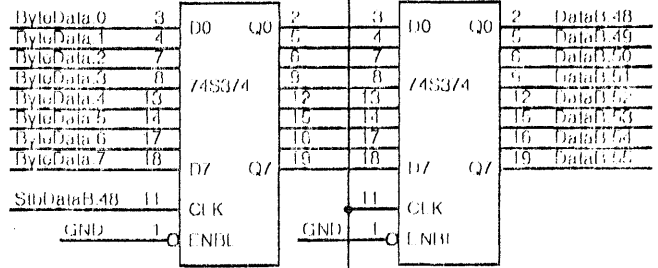
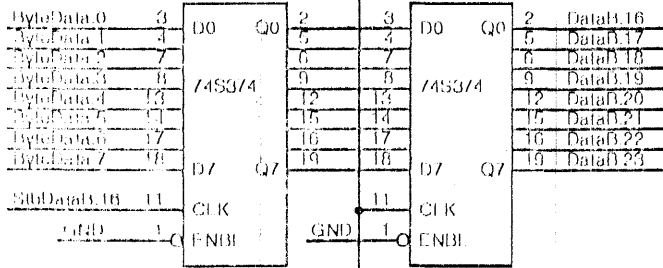
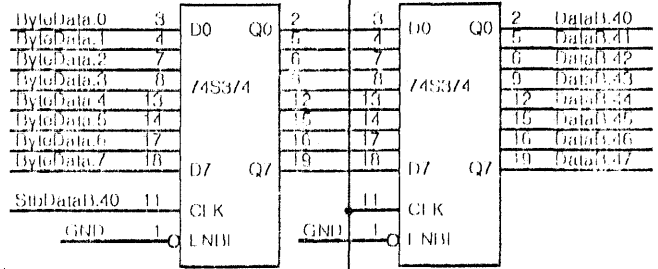
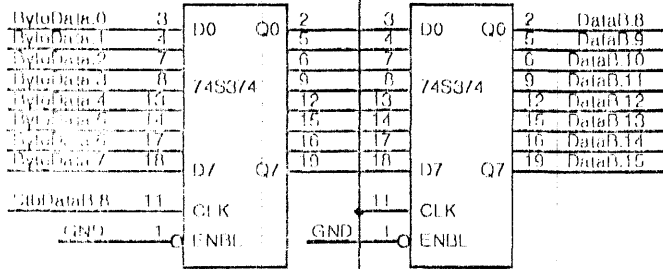
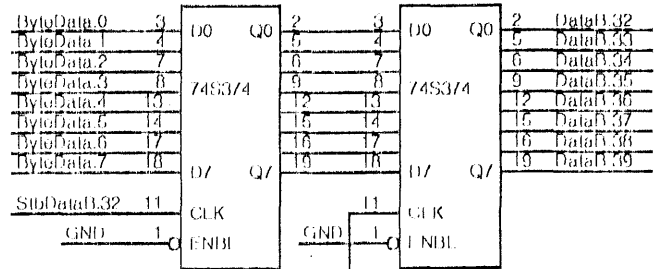
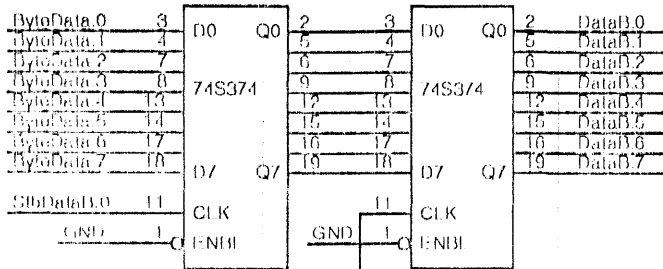




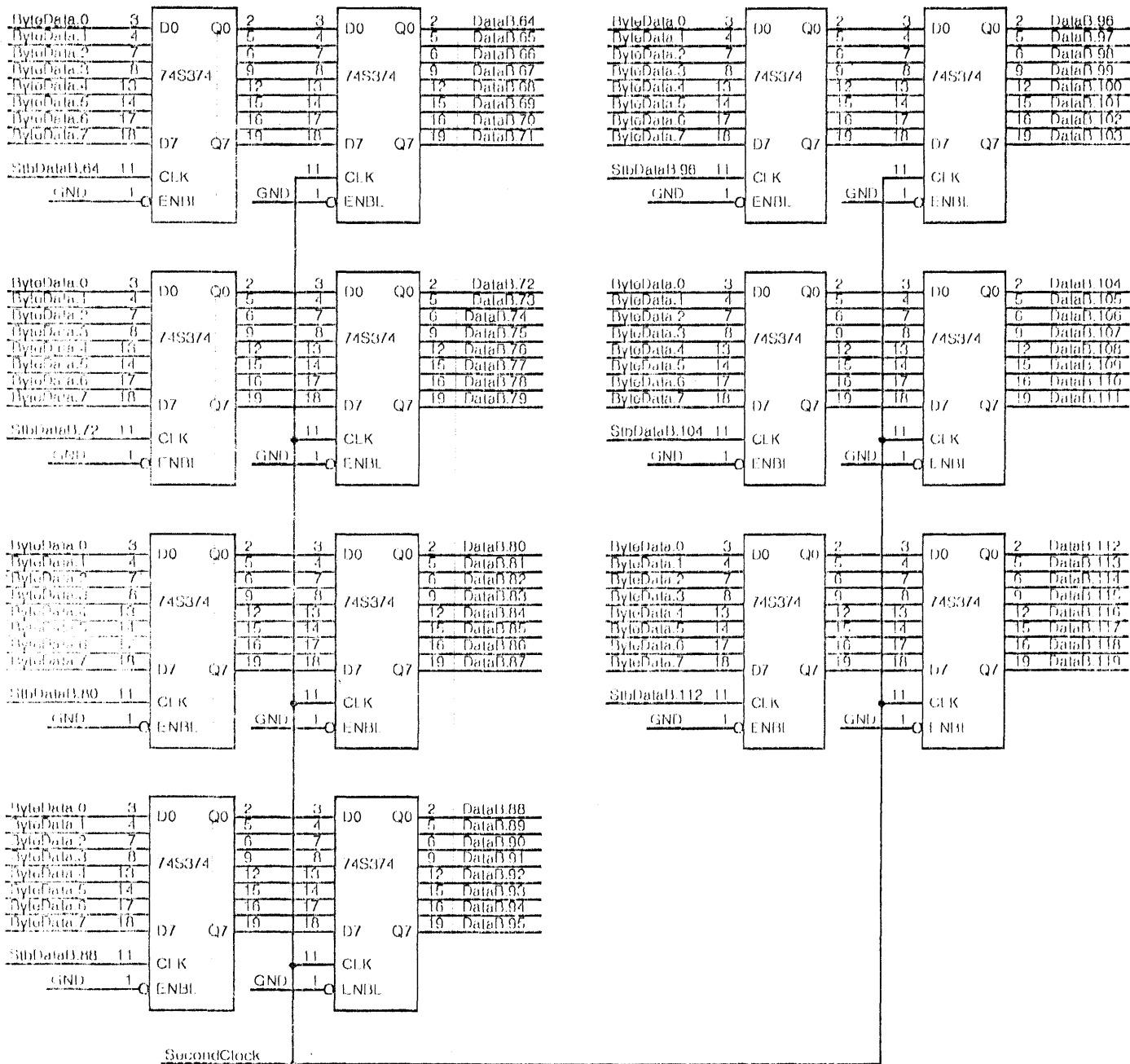
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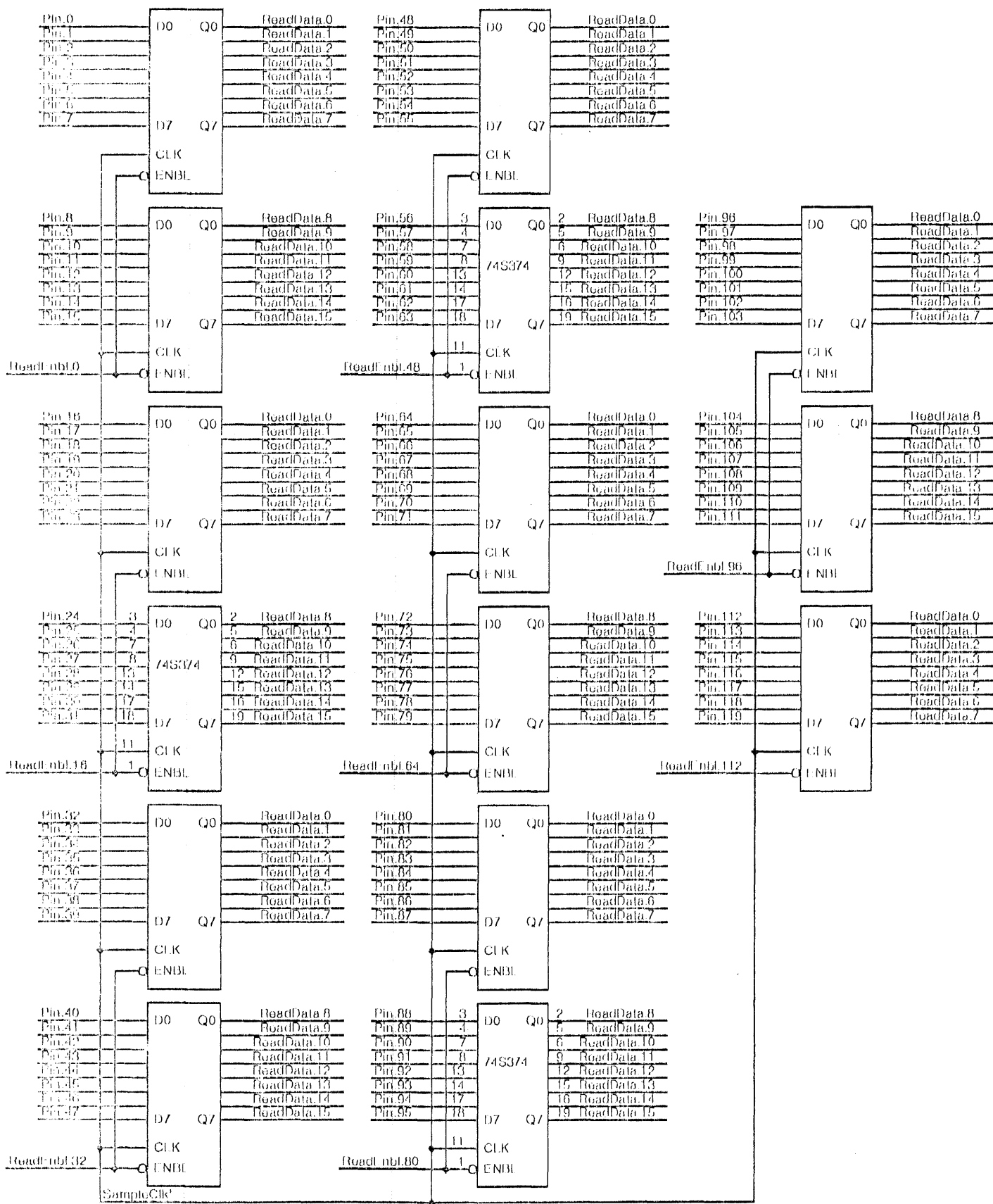


EarlyClock

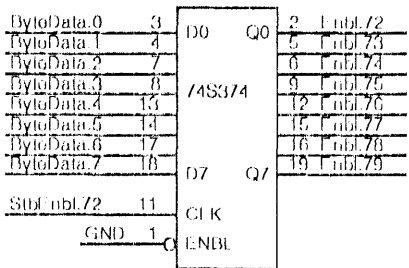
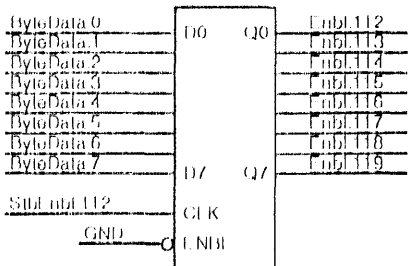
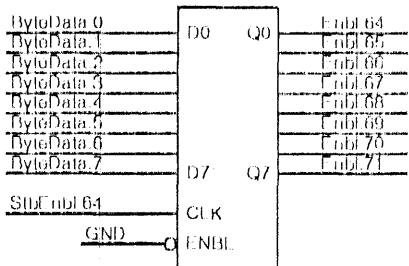
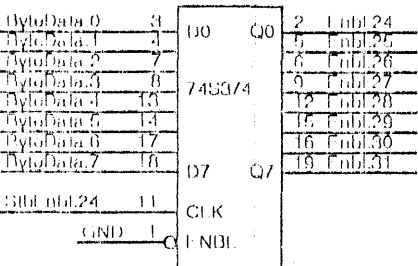
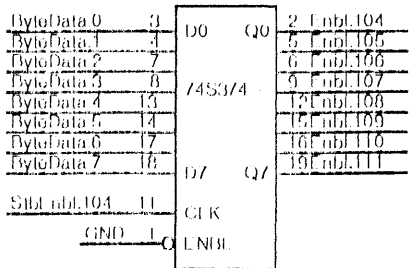
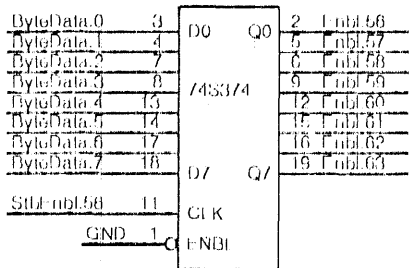
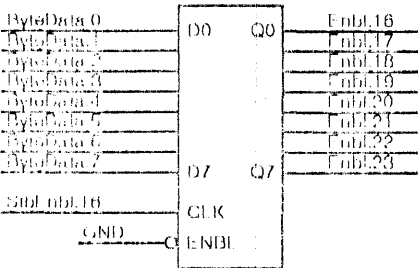
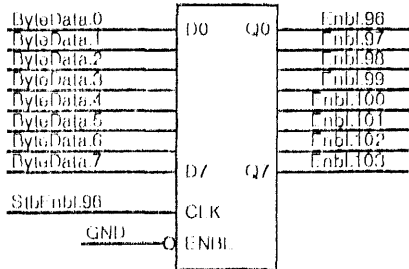
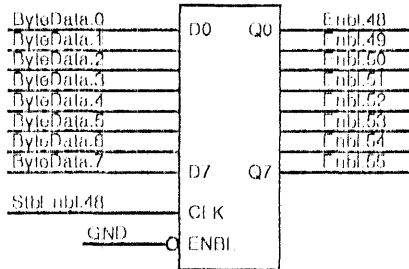
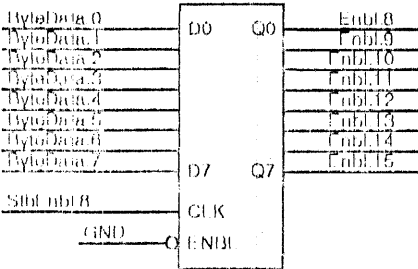
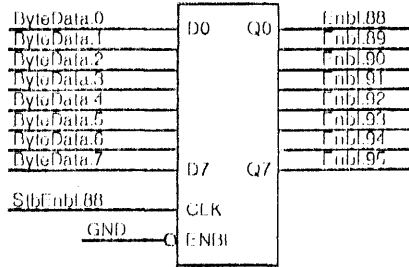
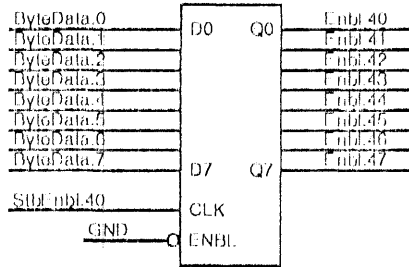
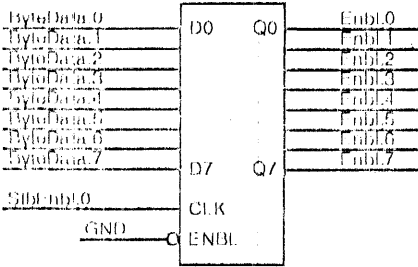
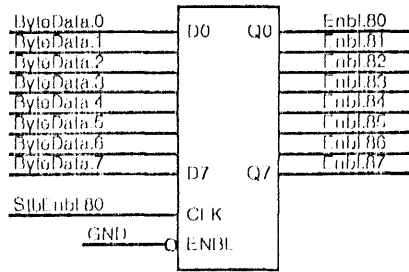
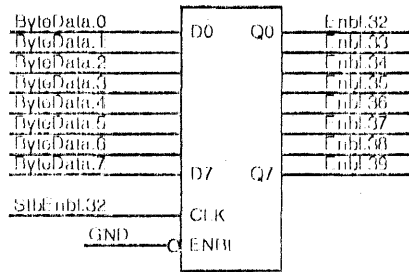


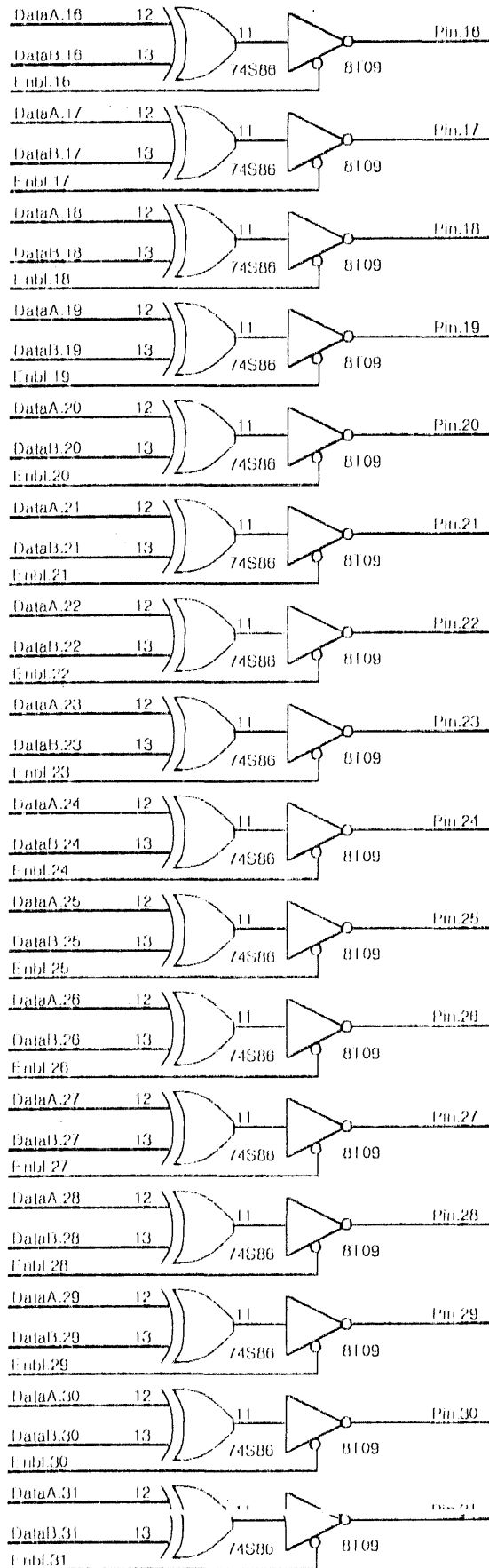
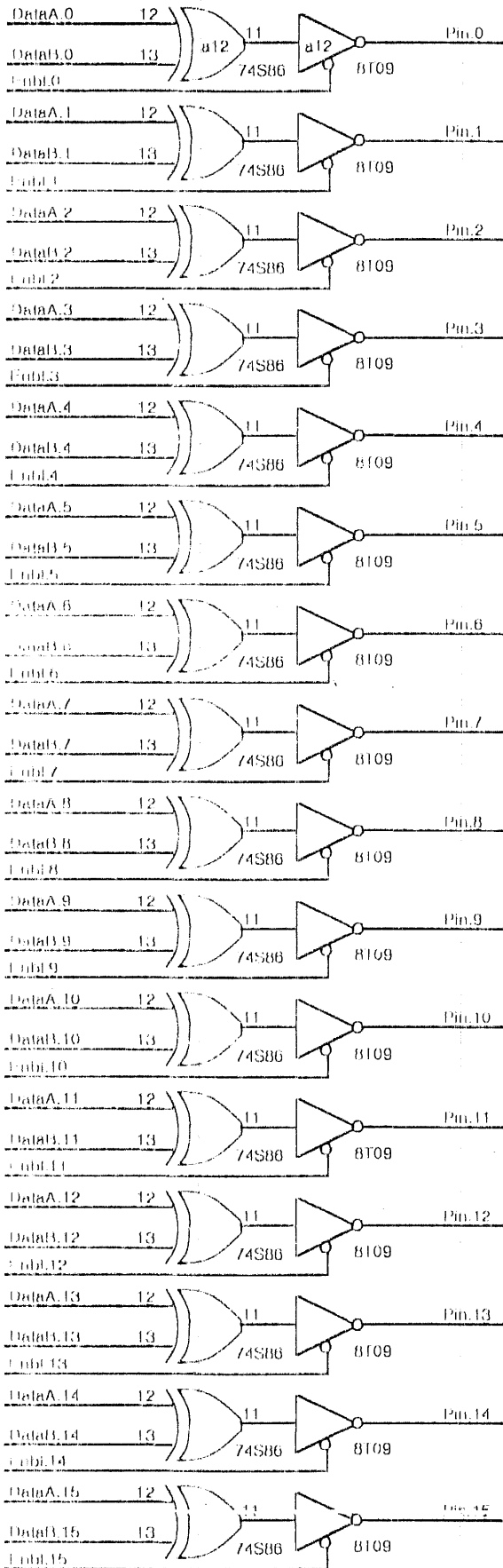
SecondClock

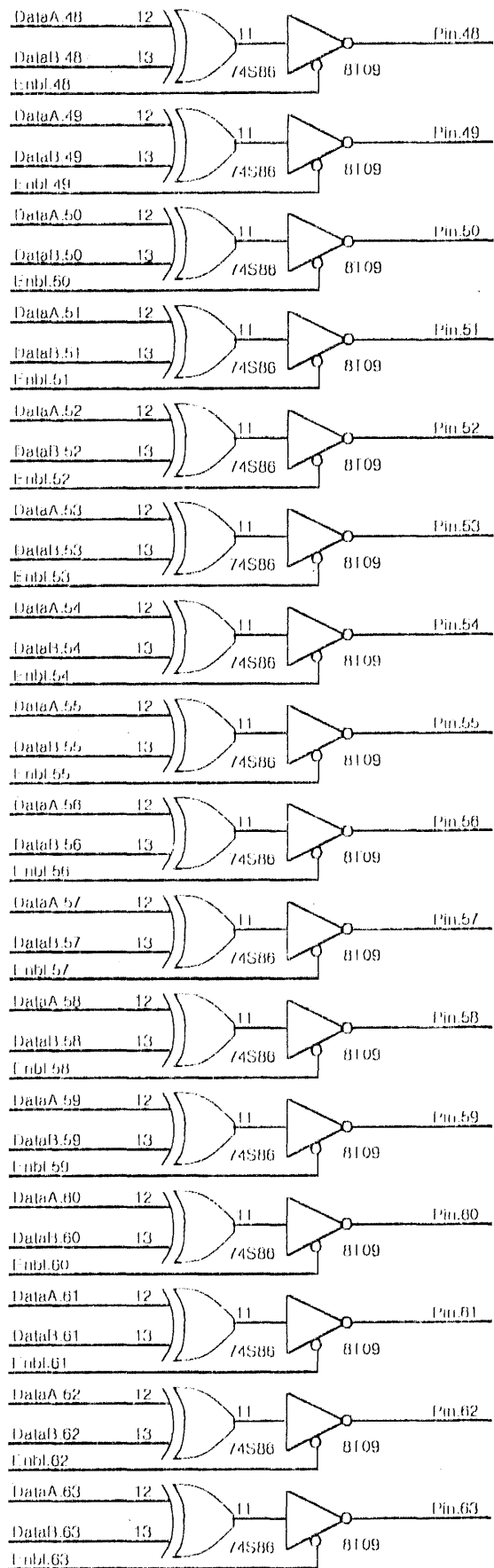
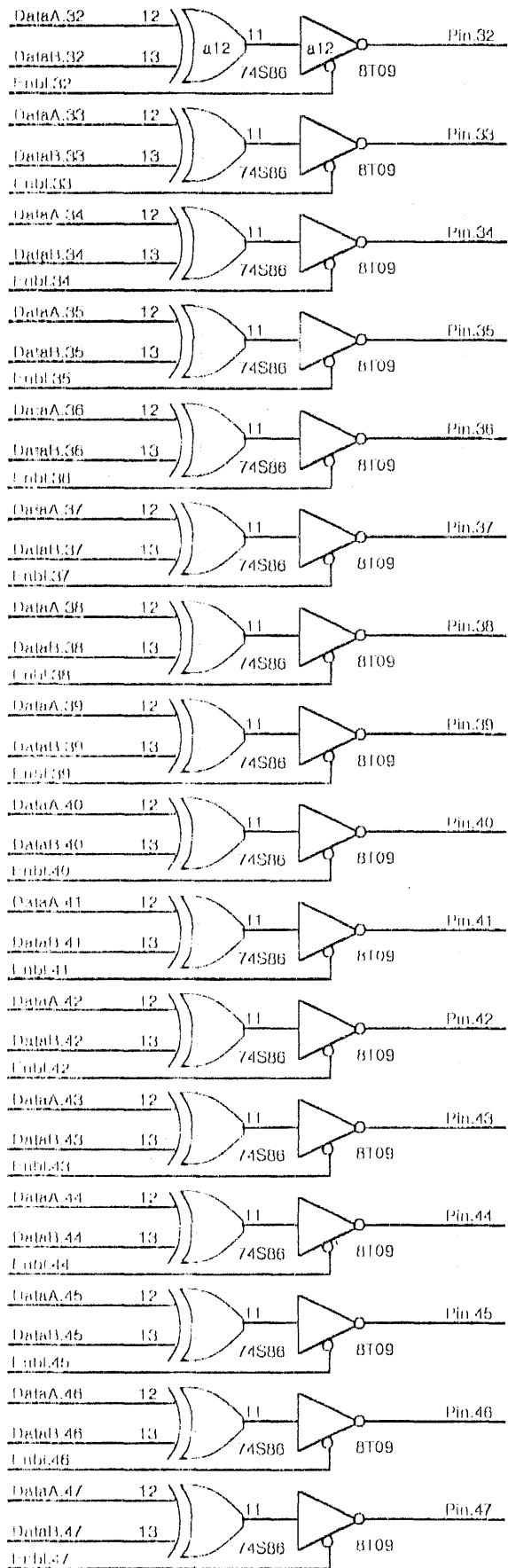


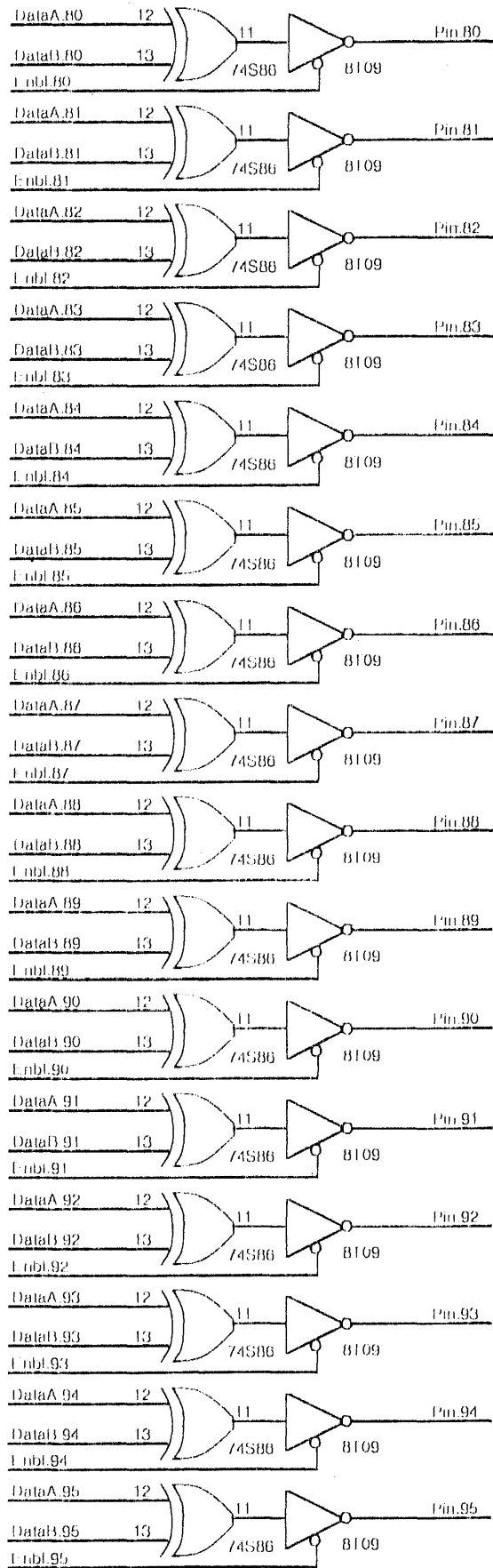
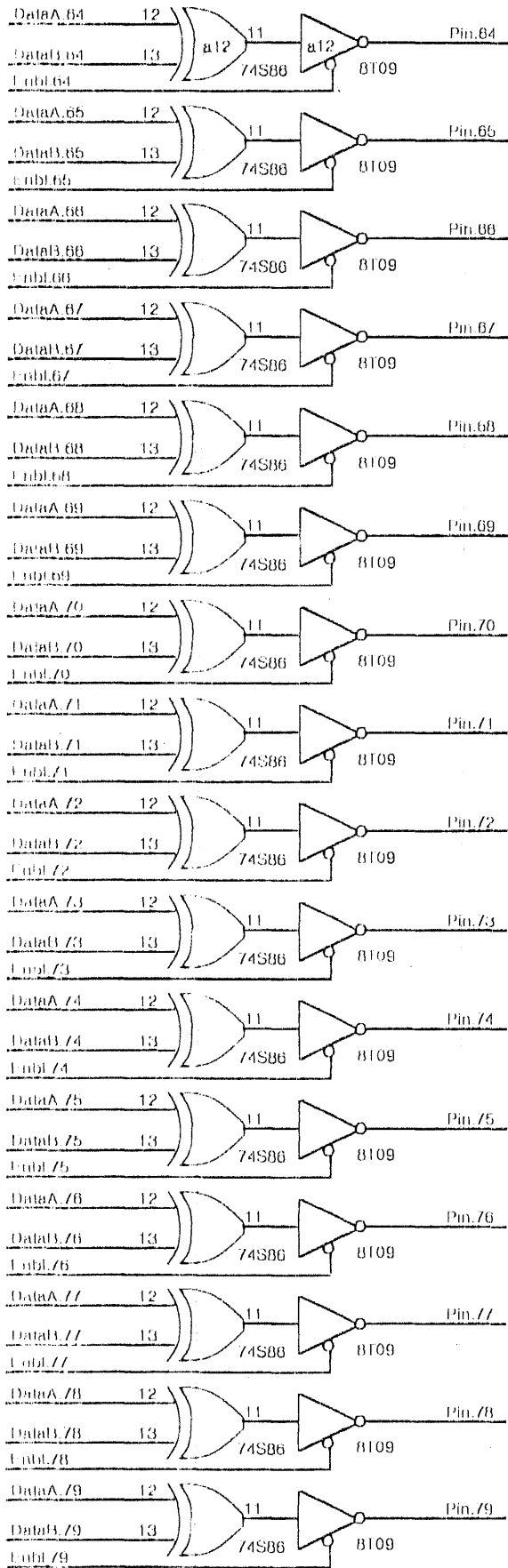


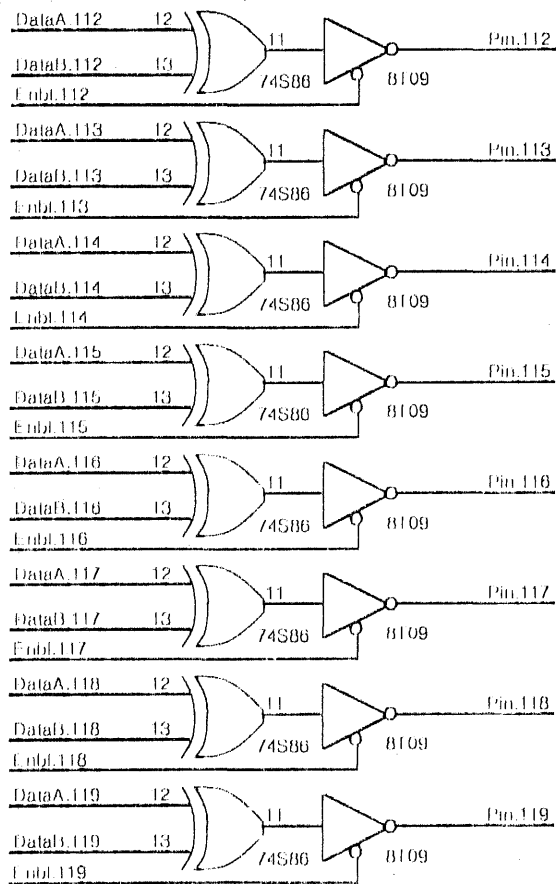
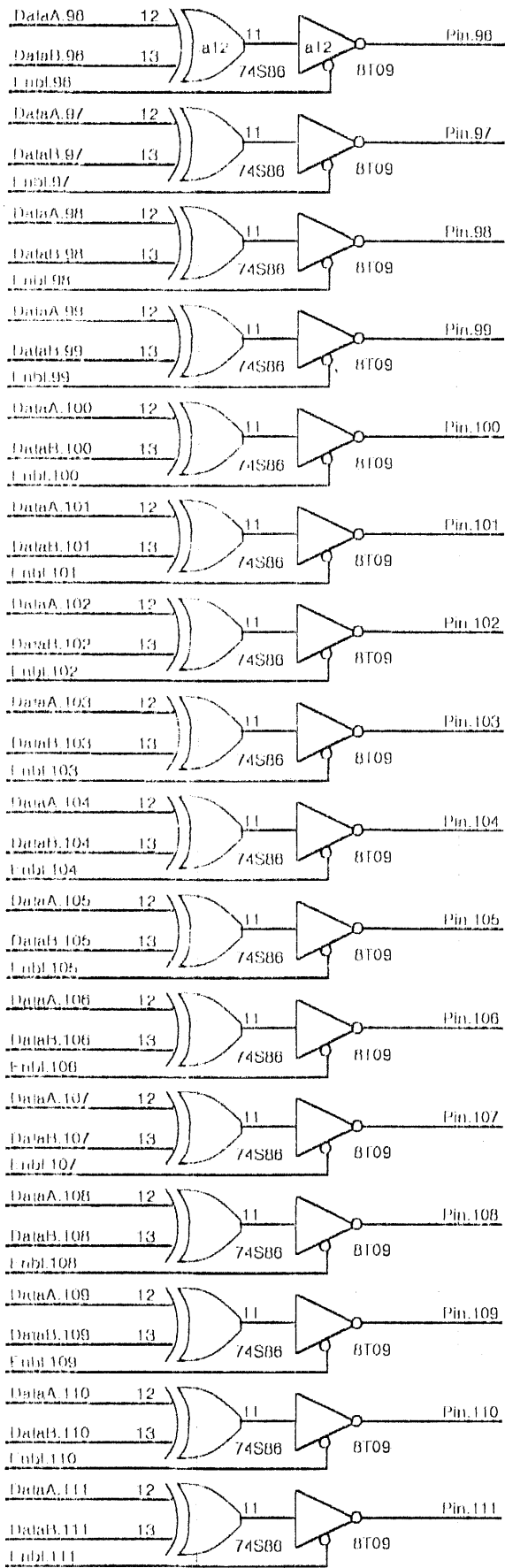












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Pin.60	162	Pin.124	162
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Pin.62	164	Pin.126	164
Pin.63	165	Pin.127	165

Pin Numbers Wrong!

FILE: CTST29

TITLE: Chip tester

Board:  
Ctest-2

Press File Written:15 Oct 80 19:30:56  
LIBRARY: TTI

DATE:15-Oct-80 19:05

Chip Pin Enables  
Chip Pin Catch Reg

Drawn by PARSNIP