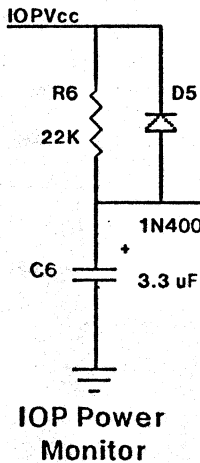
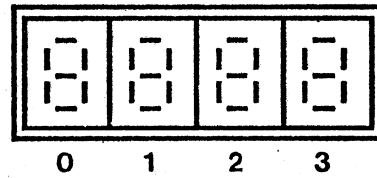
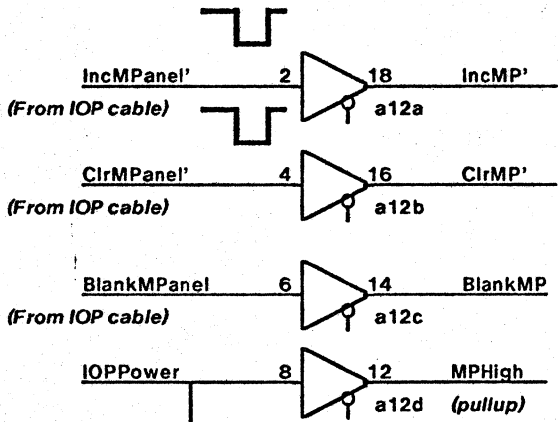
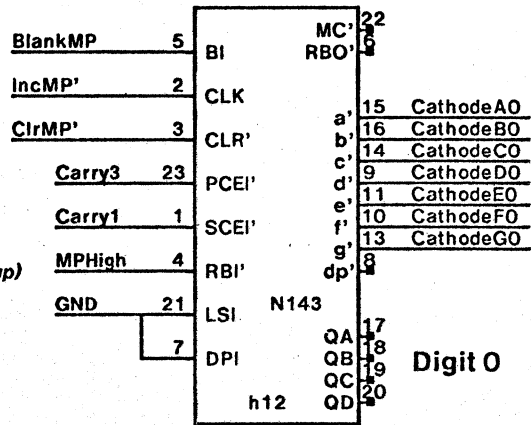
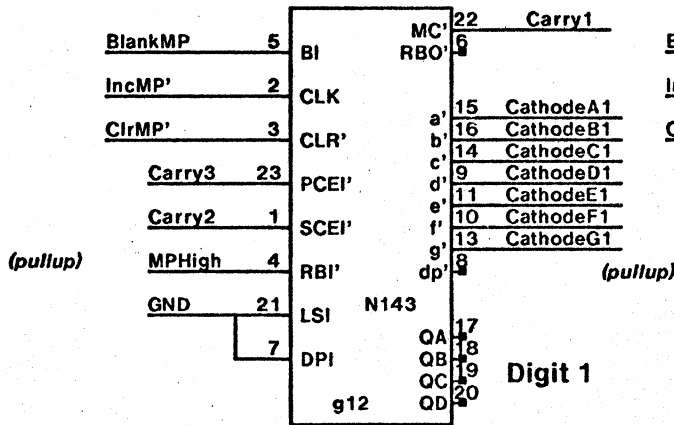
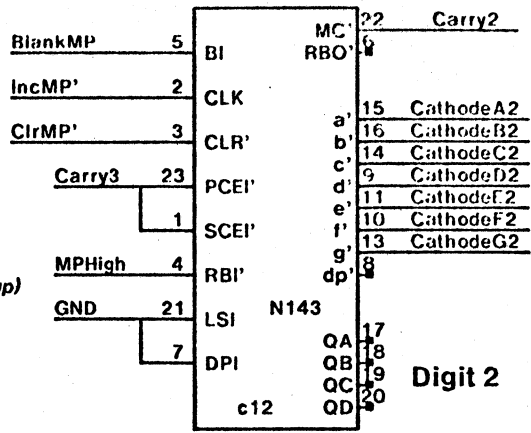
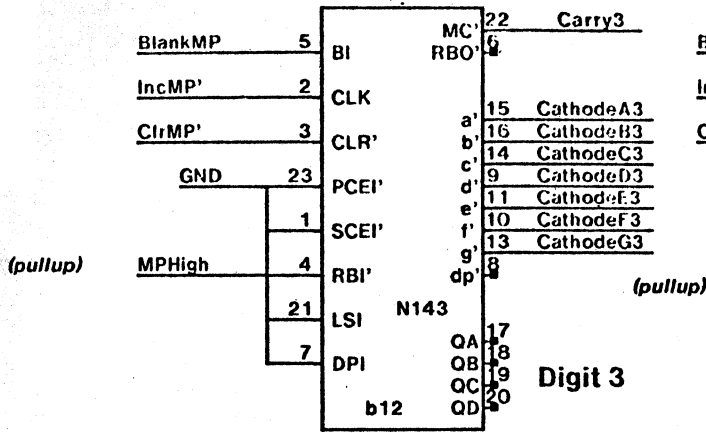
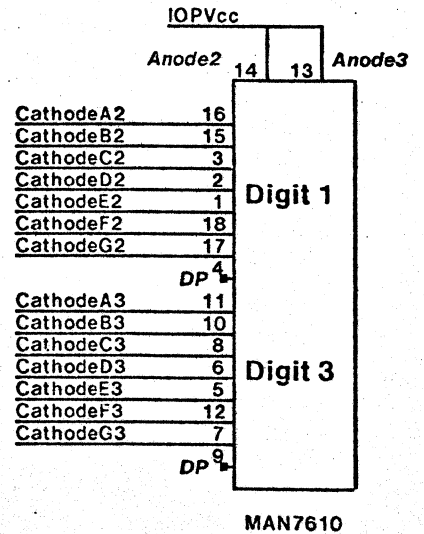
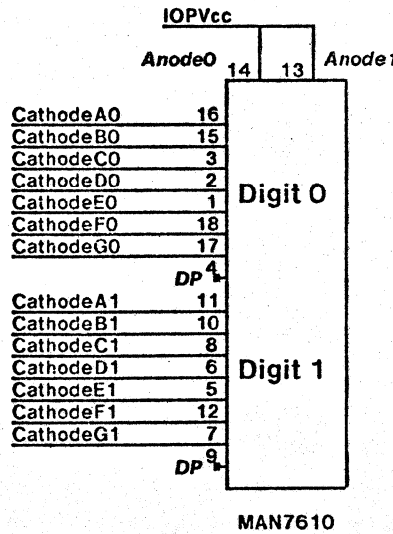


I/O Processor - Maintenance Panel Cable

<u>I/O Processor</u>	<u>Signal Name</u>	<u>Maintenance Panel</u>
1	IncMPanel'	1
2	ClrMPanel'	2
3	BlankMPanel	3
4	PowerFailed'	4
5	SetTime'	5
6	Signal GROUND	6
7	Signal GROUND	7
8	IOPVcc (IOP + 5 V)	8
9	IOPVcc (IOP + 5 V)	9
10	EnMPSignals'	10
11	1HzClk'	11
12	AltBoot'	12
13	BootReset'	13
14	MPVcc (Maintenance Panel + 5 V)	14

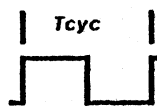
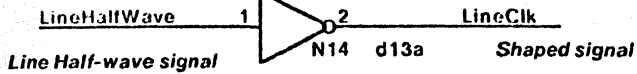


Note: All the logic on this page is powered by the Dandelion +5V (IOPVcc) through the MP-IOP cable. (850 mA max)



**7-Segment Displays (4 digits)
(Monsanto MAN6710, common anode)**

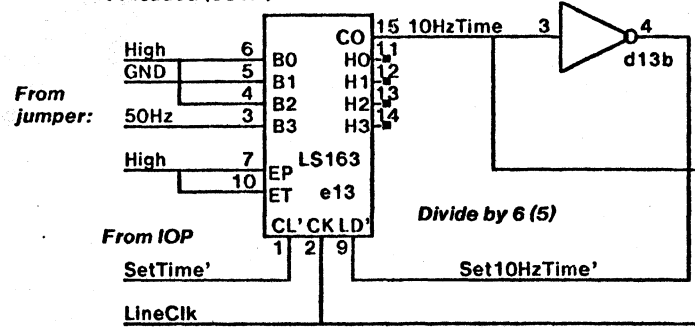
(From page 3)



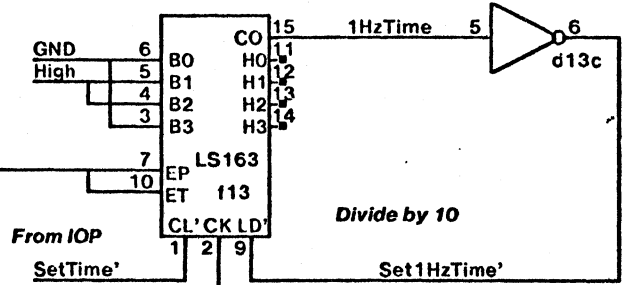
$T_{cyc} = 16.7 \text{ msec (60 Hz)}$
 $T_{cyc} = 20.0 \text{ msec (50 Hz)}$

60/50 Hz divider

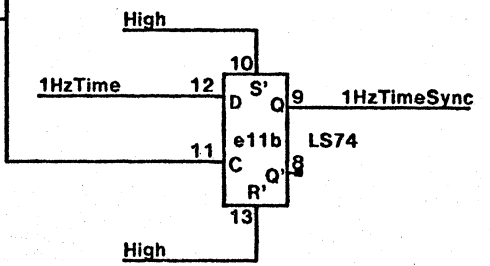
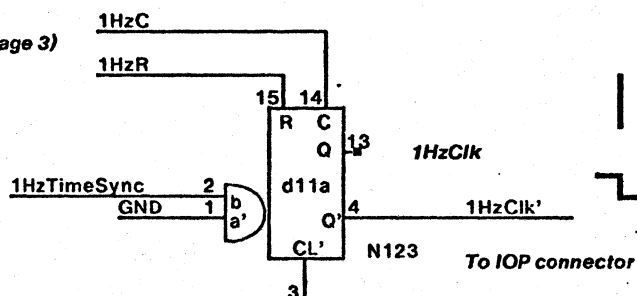
10 loaded (60 Hz)
 11 loaded (50 Hz)



6 loaded

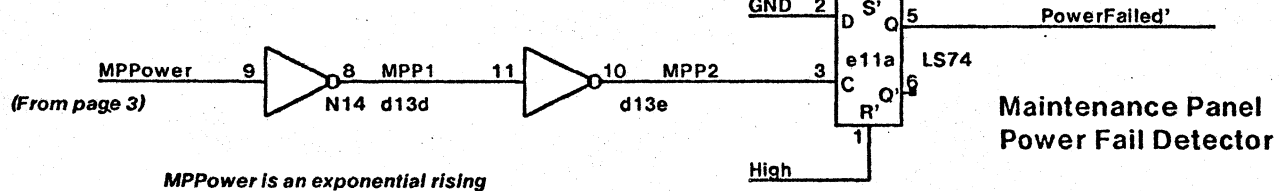


(From page 3)



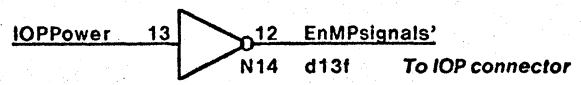
This FF is to ensure that there are no glitches on the input of the 1HzClk one-shot

Note: When SetTime' becomes inactive, there can be a 1HzClk pulse generated if 1HzTime is true.



MPPower is an exponential rising signal when the power comes up. The signal is shaped by the N14 gates and the FF is clocked. PowerFailed is set when the power comes up. This bit can be read by the IOP. The first SetTime will clear the PowerFailed condition.

(From page 1)

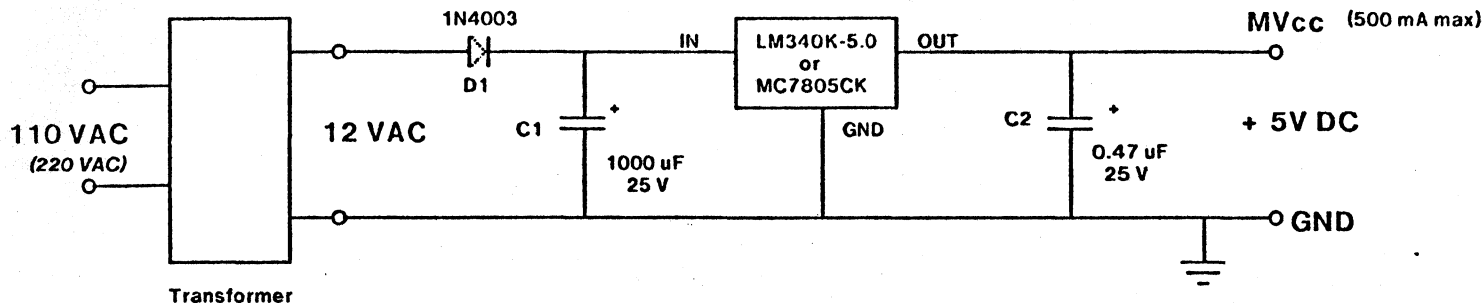


EnMPsignals' is high (inactive) when the IOP power is down, and low (active) when the IOP power is +5V. It is used to enable tristate buffers of signals driving unpowered logic.

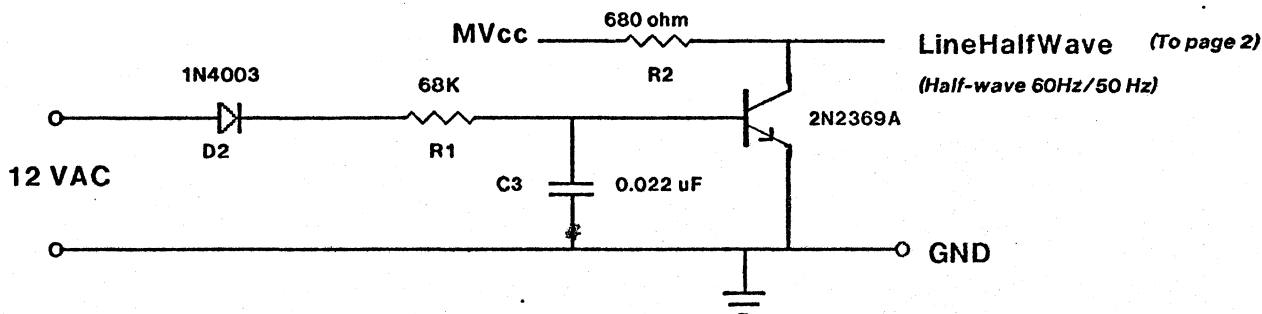
Note: All the logic on this page is powered by the MVcc + 5V supply in the maintenance panel.

XEROX SDD	Project Dandelion	Maintenance Panel 60/50 Hz divider, Power Fail	File DandMP02.sil	Designer Ogus	Rev D	Date 3/17/80	Page 02
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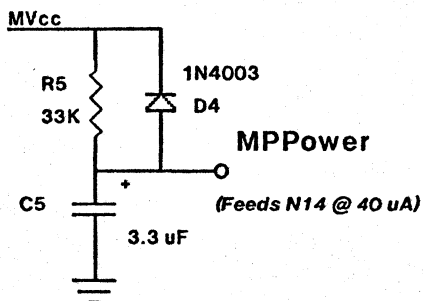
Regulator
TO-3 Metal Can with Heatsink
 Theta (Case-Heatsink) = 0.4 deg. C/W
 Theta (Heatsink-Air) < 16 deg. C/W



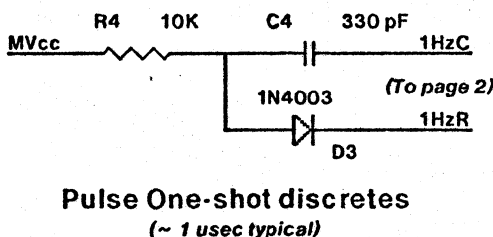
+ 5V DC power supply for Time-Of-Day Clock



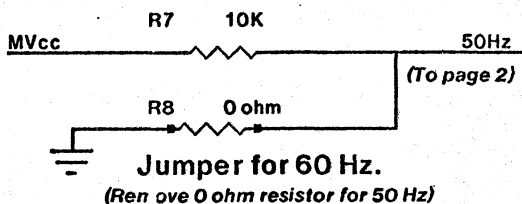
Line Clock for Divider



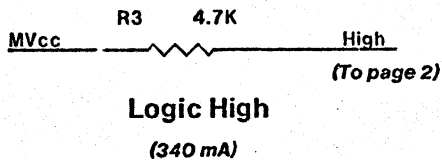
Power-fail time constant
(100 msec)



Pulse One-shot discretes
(~ 1 usec typical)



Jumper for 60 Hz.
(Remove 0 ohm resistor for 50 Hz)

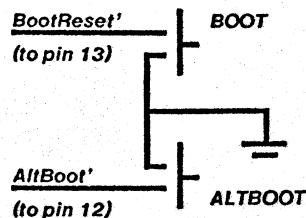


Logic High
(340 mA)

Note: There are two different +5V power supplies on this page. IOPVcc comes from the IOP, and MVcc is generated in the Maintenance Panel.

Page	Signal	Pin
1	IncMPanel'	1
1	CirMPanel'	2
1	BlankMPanel	3
2	PowerFailed'	4
2	SetTime'	5
	GND	6
	GND	7
3	IOPVcc	8
3	IOPVcc	9
2	EnMPsignals'	10
2	1HzClk'	11
3	AltBoot'	12
3	BootReset'	13
3	MVcc	14

I/O Connector to IOP



Boot switches connection

Panel Switches

MATERIAL LIST

ML	Drawing No.	Rev. A
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Rev. No.	Drawing Title	<p>These drawings and specifications, and the data contained therein, are the exclusive property of Xerox Corporation and or Rank Xerox, Ltd. issued in strict confidence and shall not, without the prior written permission of Xerox Corporation Rank Xerox, Ltd., be reproduced, copied or used for any purpose whatsoever, burp, except the manufacture of articles for Xerox Corporation or Rank Xerox, Ltd.</p>
	<p>Dandelion Maintenance Panel Parts list for Revision D <i>(filed on [Iris]<Workstation>IOP>MPParts-D.sil</i></p>	
wg.	Model No.	Date 3/17/80
No.		Sheet 1 of 1

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
	<i>Integrated Circuit</i> 74LS74		1	
	74LS163		2	
ML	74LS244		1	
	7414		1	
	74123		1	
	<i>Integrated Circuit</i> 74143		4	
	<i>7-segment display</i> MAN6710		2	Monsanto Dual-digit display
	<i>IC regulator</i> LM340K-5.0 or MC7805CK		1	+5V 3-terminal regulator TO-3 Metal case
	<i>Heatsink</i> Commercial type for TO-3 case with: Theta (Heatsink-Air) < 16 deg.C/W		1	Mounting: Theta (Case-Sink) < .4 C/W
	<i>Diode</i> Silicon Rectifier 1N4003		5	
	<i>Capacitor</i> C1 1000 uF, 25V		1	
	<i>Capacitor</i> C2 0.47 uF, 25V		1	
	<i>Capacitor</i> C3 0.022 uF, 25V		1	
	<i>Capacitor</i> C4 330 pF		1	
	<i>Capacitor</i> C5, C6 3.3 uF, 25V		2	
	<i>Capacitor</i> .1 uF bypass, 25V		1 per 3 chip positions	
	<i>Resistor</i> R1 68K, 1/4 watt		1	
	<i>Resistor</i> R2 680 ohm, 1/4 watt		1	
	<i>Resistor</i> R3 4.7K, 1/4 watt		1	
	<i>Resistor</i> R4, R7 10K, 1/4 watt		2	
	<i>Resistor</i> R5 33K, 1/4 watt		1	
	<i>Resistor</i> R6 22K, 1/4 watt		1	
	<i>Resistor</i> R8 0 ohms (jumper)			
	<i>Transformer</i> 110 VAC/12 VAC I max (sec) = 500 mA		1	