

ELECTRICAL REF DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QTY
C1,2,11,20,95,	1	702W07301	CAP., 20, 15V	8
112,171,181				
C3 THRU 10,	2	702W07818	CAP., 0.1, 50V	181
12 THRU 19,				
21 THRU 94,				
96 THRU 111,				
113 THRU 170,				
172 THRU 180,				
182 THRU 189				
F1	3	708W11402	FUSE, 10 AMP	1
R1 THRU 7,9,	4	703W27888	RES, 15 OHMS	71
13 THRU 19,22,				
24 THRU 31,34,				
36 THRU 42,44,45,				
48 THRU 55,57,				
60 THRU 63,				
65 THRU 69,				
72 THRU 78,81,82,				
85,88 THRU 96				
R8,10,11,20,21,	5	703W27488	RES, 10 OHMS	24
23,32,33,35,43,				
46,47,56,58,59,				
64,70,71,79,80,				
83,84,86,87				
R12,113,129,132	6	703W32288	RES, 1K OHMS	4
R97 THRU 112,128	7	703W28488	RES, 27 OHMS	17
R114,	8	703P10005	RES, ZERO OHMS	12
117 THRU 124,				
126,130,134				
R136 THRU 145	9	703W30688	RES, 220 OHMS	10
U1 THRU 4,	10	703W01562	IC, MK4164	68
9 THRU 12,				
17 THRU 20,				
25 THRU 28,				
34 THRU 37,				

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TITLE PWB ASSY, MCC-P (256K)	DWG. SIZE A4	DWG. NO. 140S05950	SHEET REV A
	SHEET 1 OF 3		

ELECTRICAL REF DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QTY
42 THRU 45.				
51 THRU 54.				
60 THRU 63.				
68 THRU 71.				
77 THRU 80.				
86 THRU 89.				
94 THRU 97.				
103 THRU 106.				
111 THRU 114.				
120 THRU 123.				
129 THRU 132.				
137 THRU 140				
U33,85,102	11	703W13291	IC, 1KX15	3
U50,59,76,119.	12	733W01634	IC, SN74S241	9
128,145,165,211.				
212				
U146 THRU 154.	13	733W01633	IC, SN74S240	16
156,158,164,182.				
200,202,207				
U155,157	14	733W02136	IC, SN74S37	2
U159,166,179,203	15	733W01638	IC, SN74S280	4
U172,183,192	16	733W01616	IC, SN74S138	3
U161	17	733W01635	IC, SN74S251	1
U162,163,171,177.	18	733W00318	IC, SN74S00	6
184,209				
U167,213	19	733W01606	IC, SN74S10	2
U168	20	733W01648	IC, SN74S86	1
U169,185,193	21	733W01771	IC, SN74S74	3
U170,194,201	22	733W01643	IC, SN74S02	3
U174	23	733W01663	IC, SN74LS393	1
U175,208	24	733W01640	IC, SN74S374	2
U176,210	25	733W00319	IC, SN74S04	2
U178,186	26	744W00001	IC, DELAY LINE	2
U180,181,188,189.	27	733W01636	IC, AM74S253	8
196,197,204,205				

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TITLE PWB ASSY, MCC-P (256K)	DWG. SIZE A4	DWG. NO. 140S05950	SHEET REV A
	SHEET 2 OF 3		

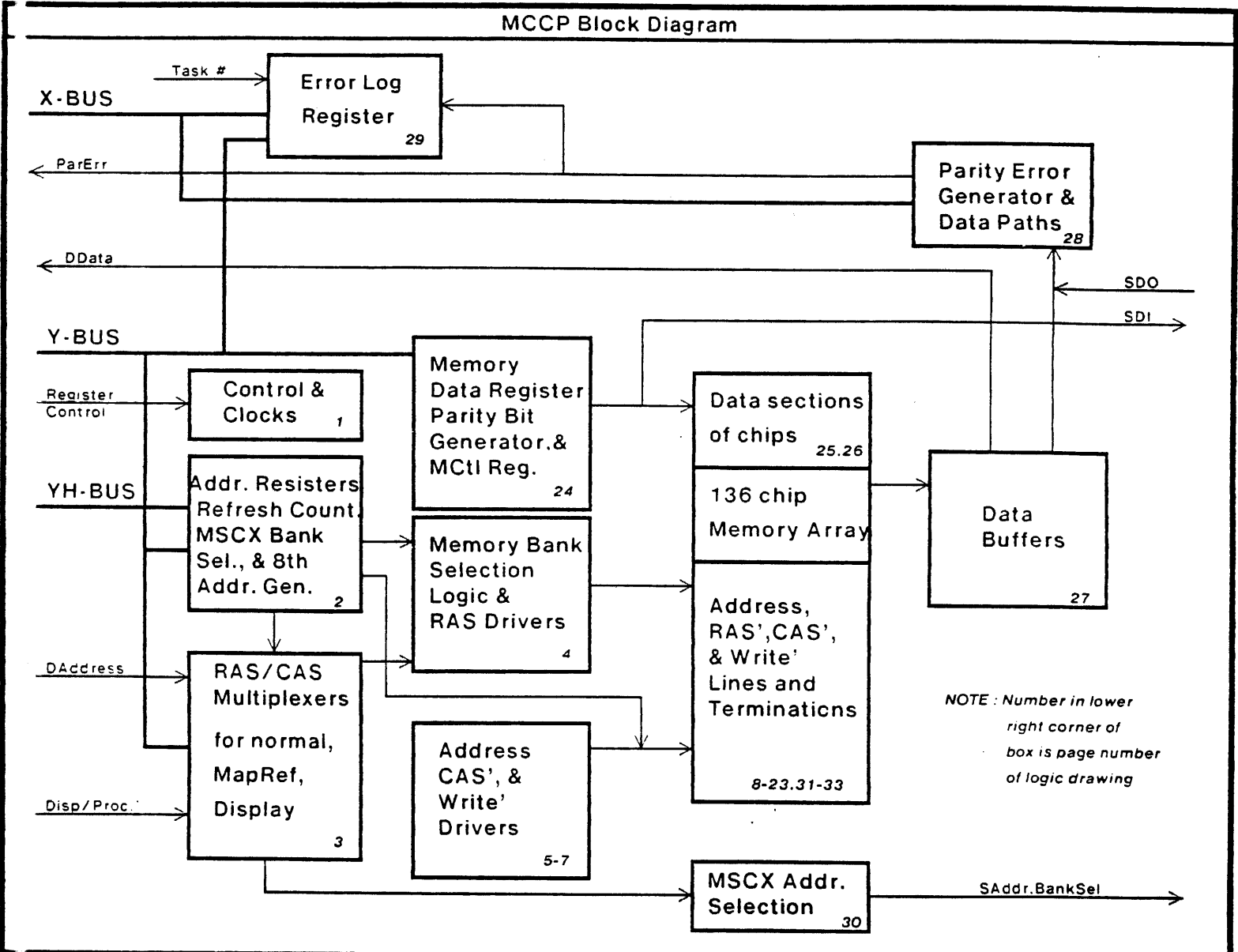
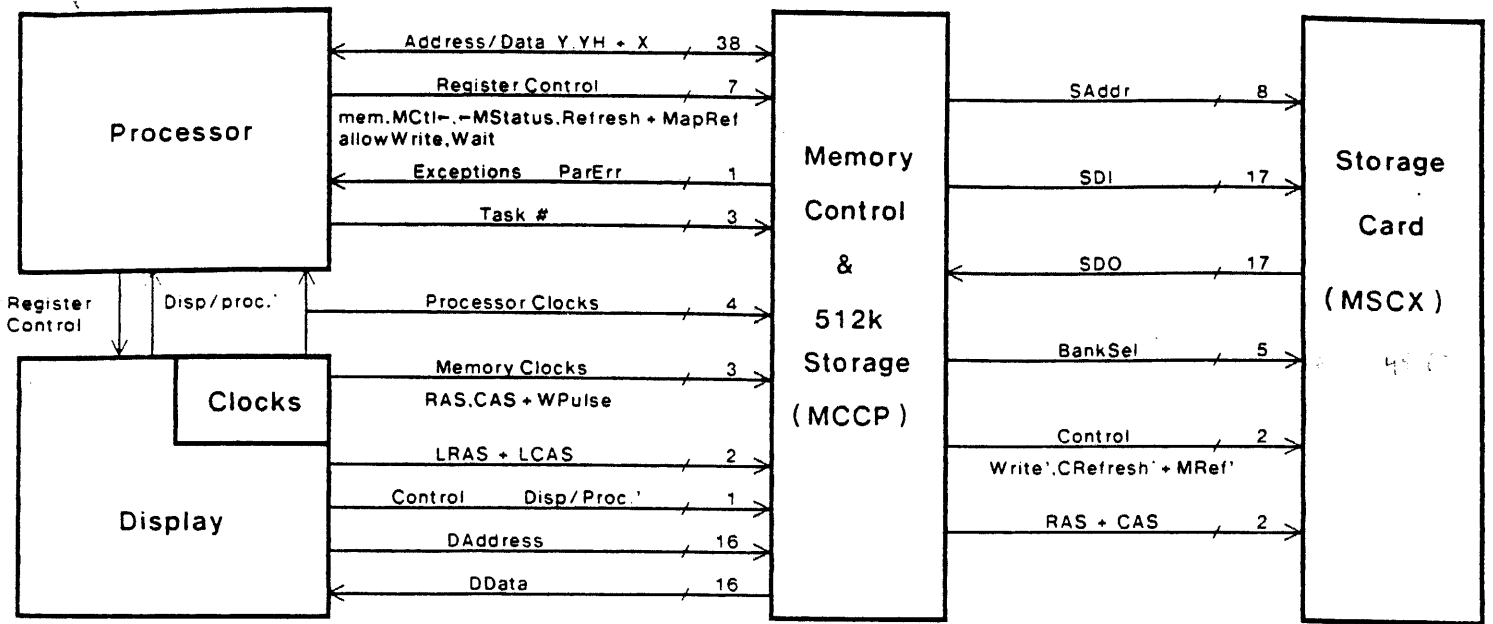
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- 0.4 MEMORY CONTROLLER BLOCK DIAGRAM
- 1. WRITE, CREFRESH', MREF, LDMDR, CYCLE RCV, MDCLK, ←MD'
- 2. ADDRESS SELECT., REFRESH COUNT, CAS RESISTERS
- 3. ADDRESS SELECTION LOGIC, RASDLY, LRASDLY
- 4. MEMORY BANK SELECTION
- 5. MEMORY BANK SELECTION, DRIVERS FOR WRITE' & CAS'
- 6. ADDRESS DRIVERS
- 7. ADDRESS DRIVERS
- 8. ADDRESS, RAS, CAS, WRITE DISPLAY BANK
- 9. ADDRESS, RAS, CAS, WRITE DISPLAY BANK
- 10. MEMORY CONTROL/ BANK B
- 11. MEMORY CONTROL/ BANK B
- 12. MEMORY CONTROL/ BANK C
- 13. MEMORY CONTROL/ BANK C
- 14. MEMORY CONTROL/ BANK D
- 15. MEMORY CONTROL/ BANK D
- 16. MEMORY CONTROL/ BANK E
- 17. MEMORY CONTROL/ BANK E
- 18. MEMORY CONTROL/ BANK F
- 19. MEMORY CONTROL/ BANK F
- 20. MEMORY CONTROL/ BANK G
- 21. MEMORY CONTROL/ BANK G
- 22. MEMORY CONTROL/ BANK H
- 23. MEMORY CONTROL/ BANK H
- 24. MEM. DATA REG., MEM. CTL. REG., PARITY BIT GENERATOR
- 25. WORK STATION MEMORY
- 26. WORK STATION MEMORY
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- 32. DISCRETE RESISTORS
- 33. RESISTOR DIPS, TERMINATIONS
- 34. POWER PINS · FUSES · CAPS
- 35. DISCRETE CAPACITORS
- 36. DISCRETE CAPACITORS
- 37. DISCRETE CAPACITORS

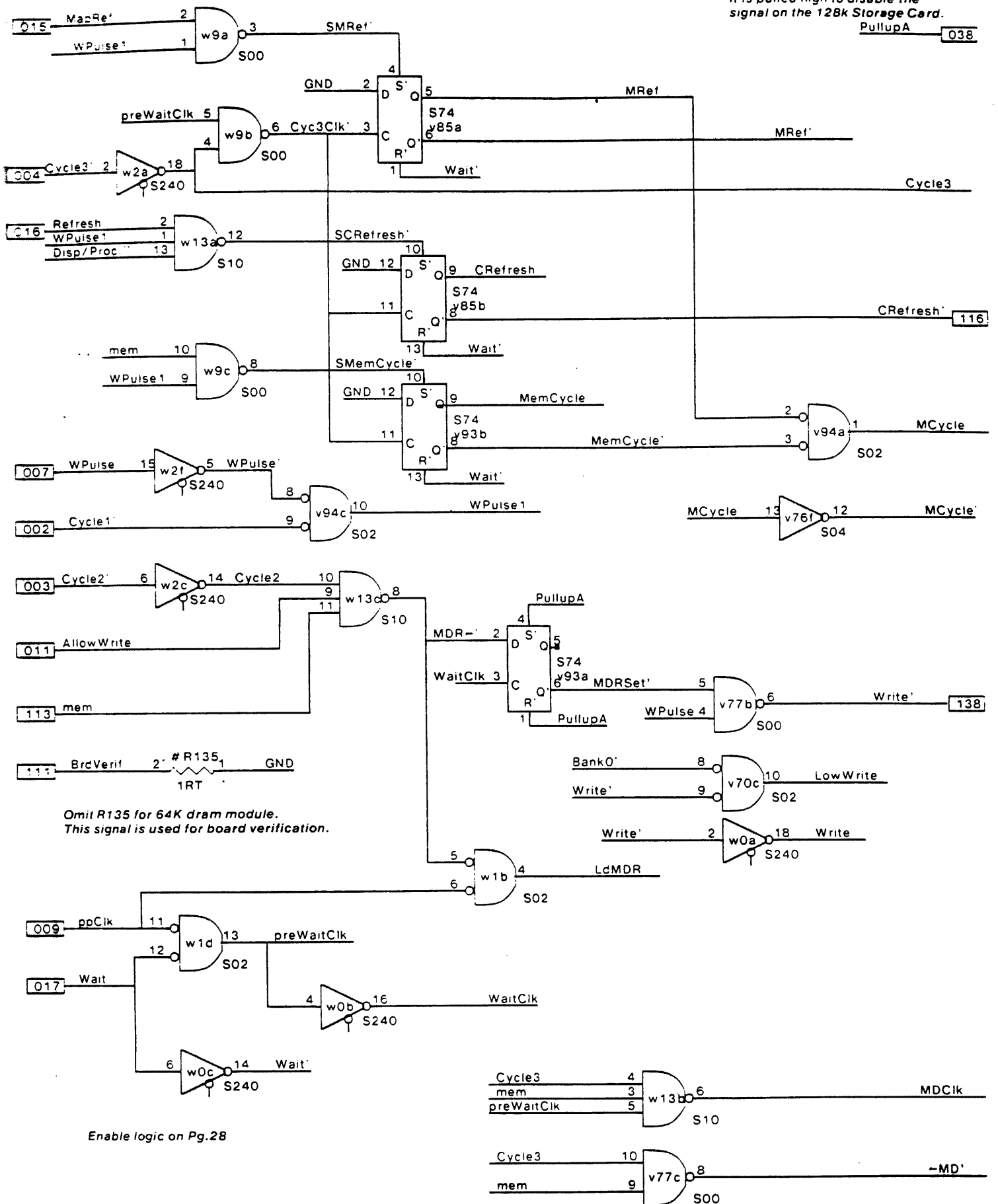
XEROX ED	Project MCCP	Reference Table of Contents	File PMCCP-0.3:sil	Designer S. Ando	Rev A	Date 10/25/83	Page 0.3
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MEMORY SYSTEM



This is MRef' on the Backplane.
It is pulled high to disable the
signal on the 128k Storage Card.

PullupA 038

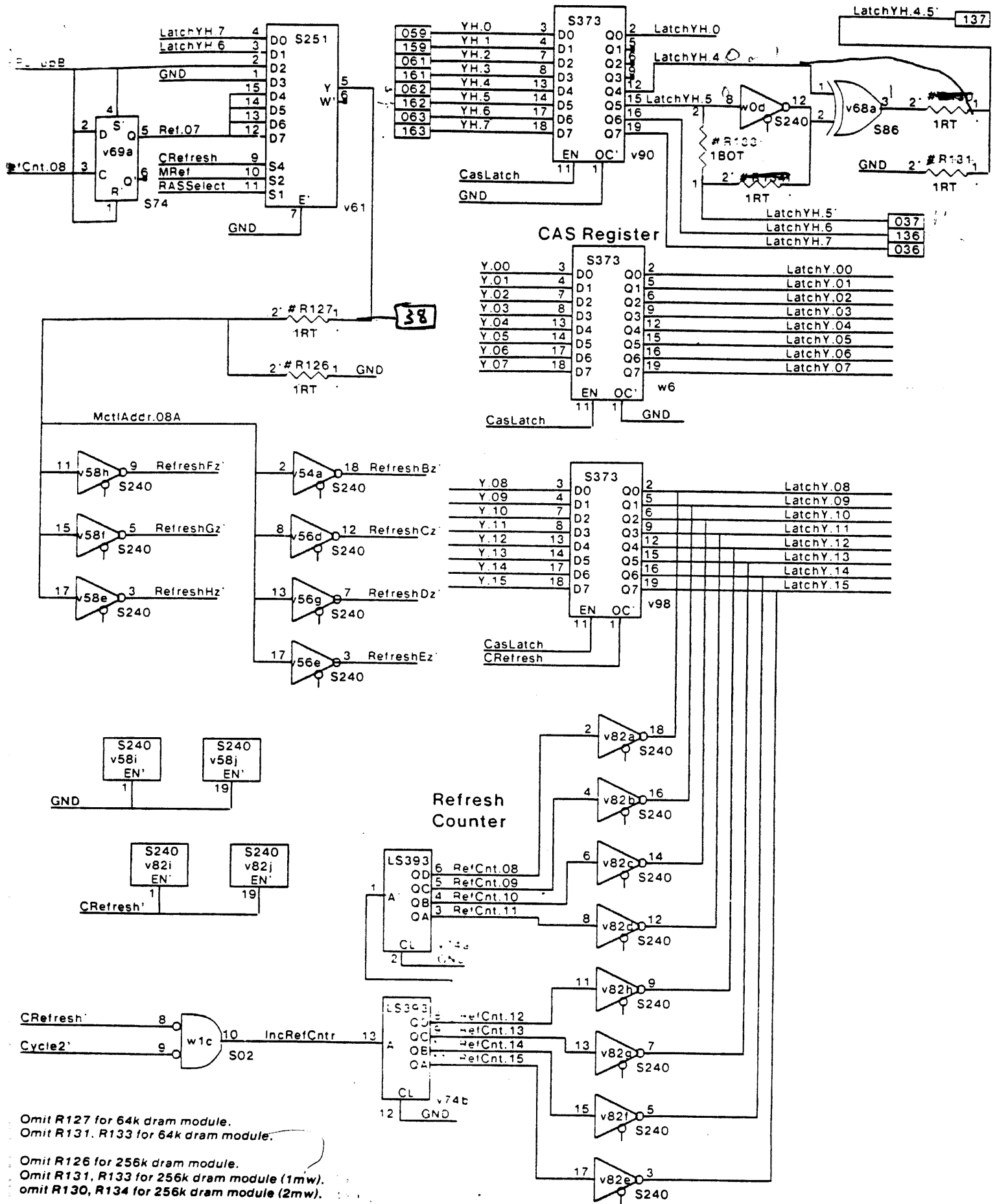


Omit R135 for 64K dram module.
This signal is used for board verification.

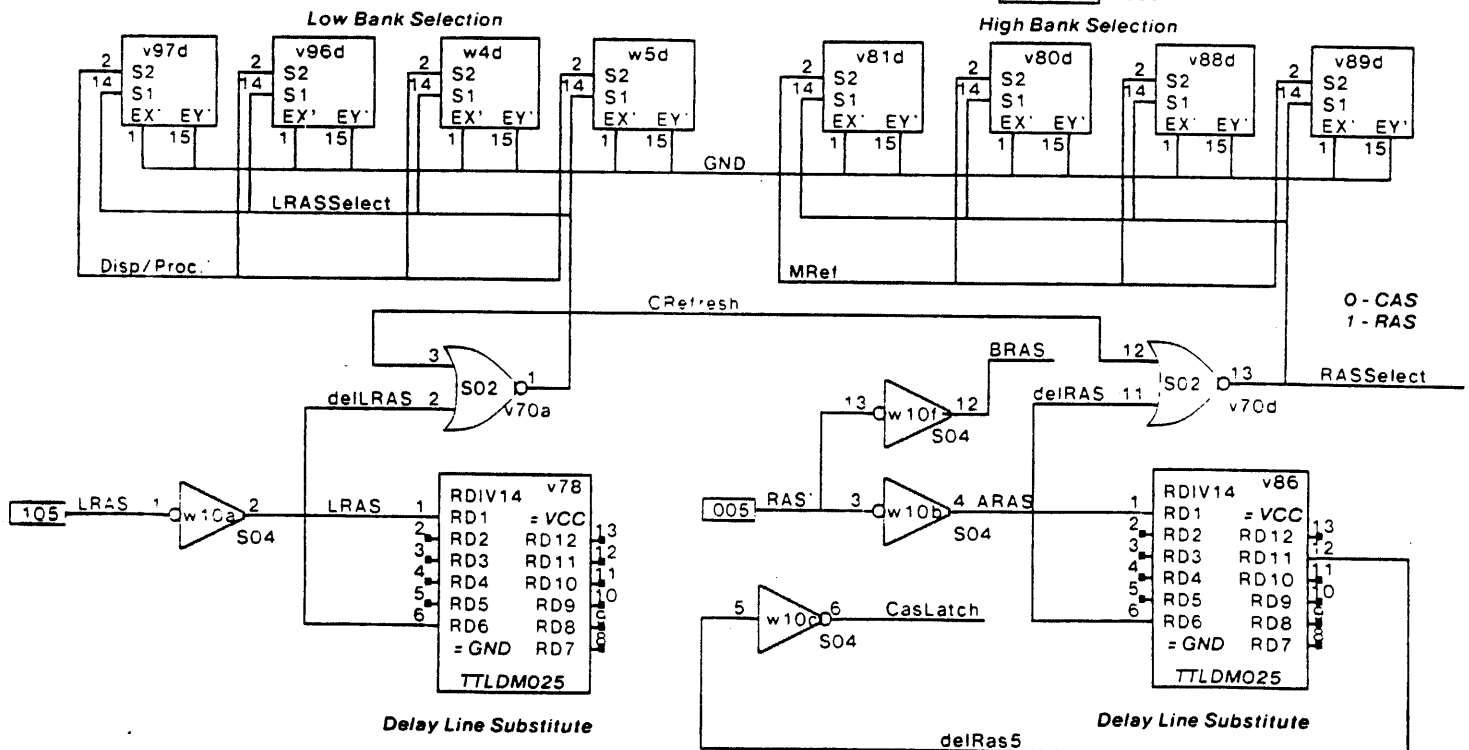
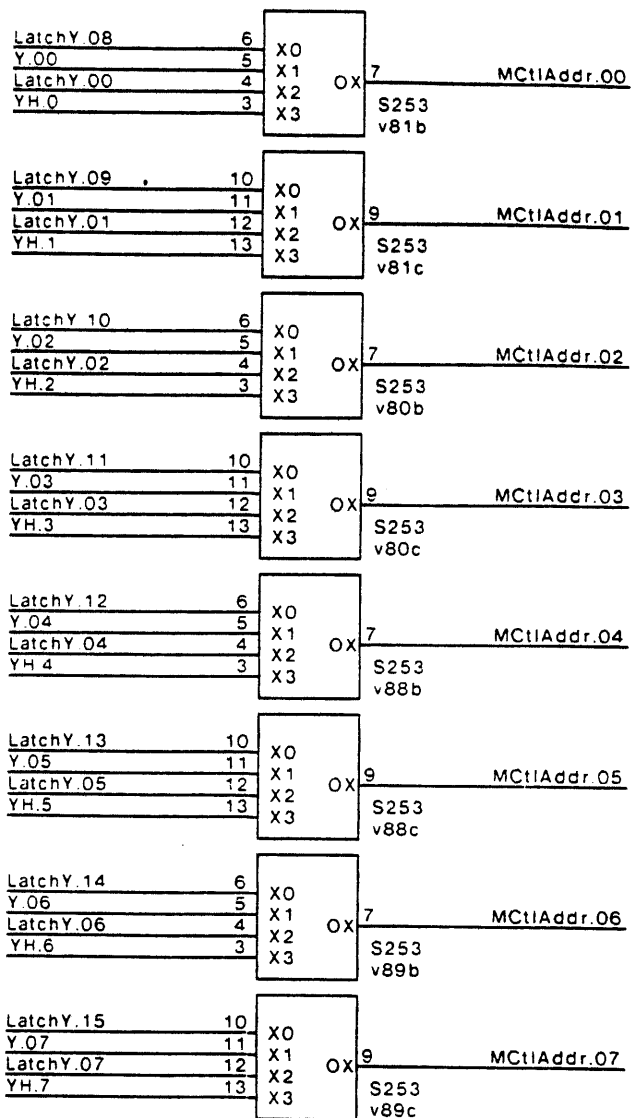
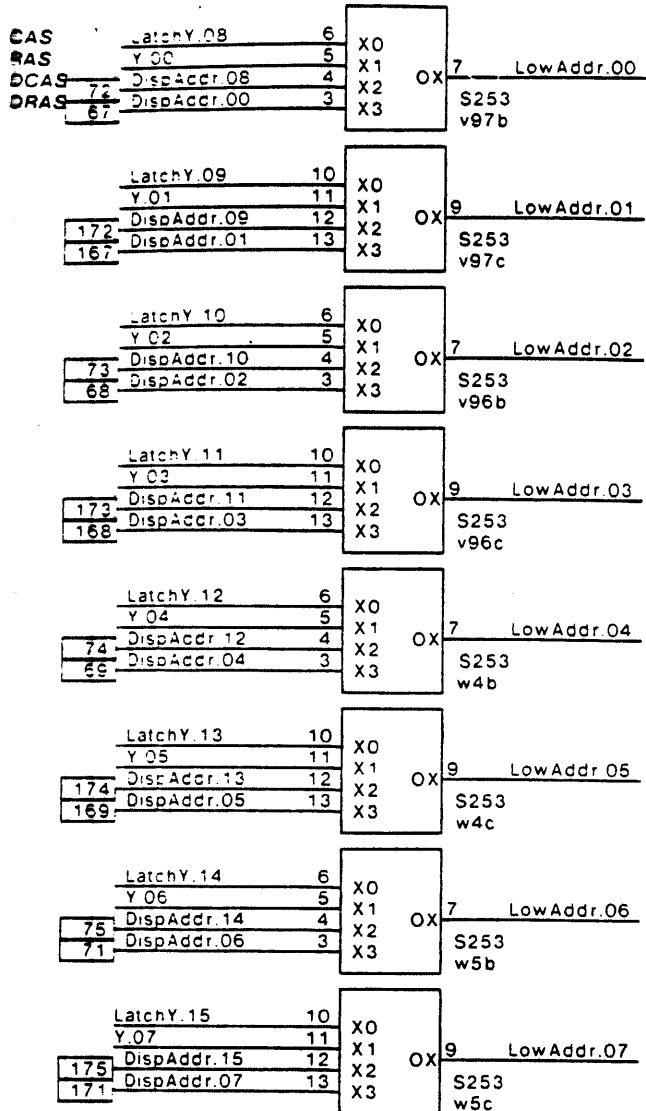
Enable logic on Pg.28

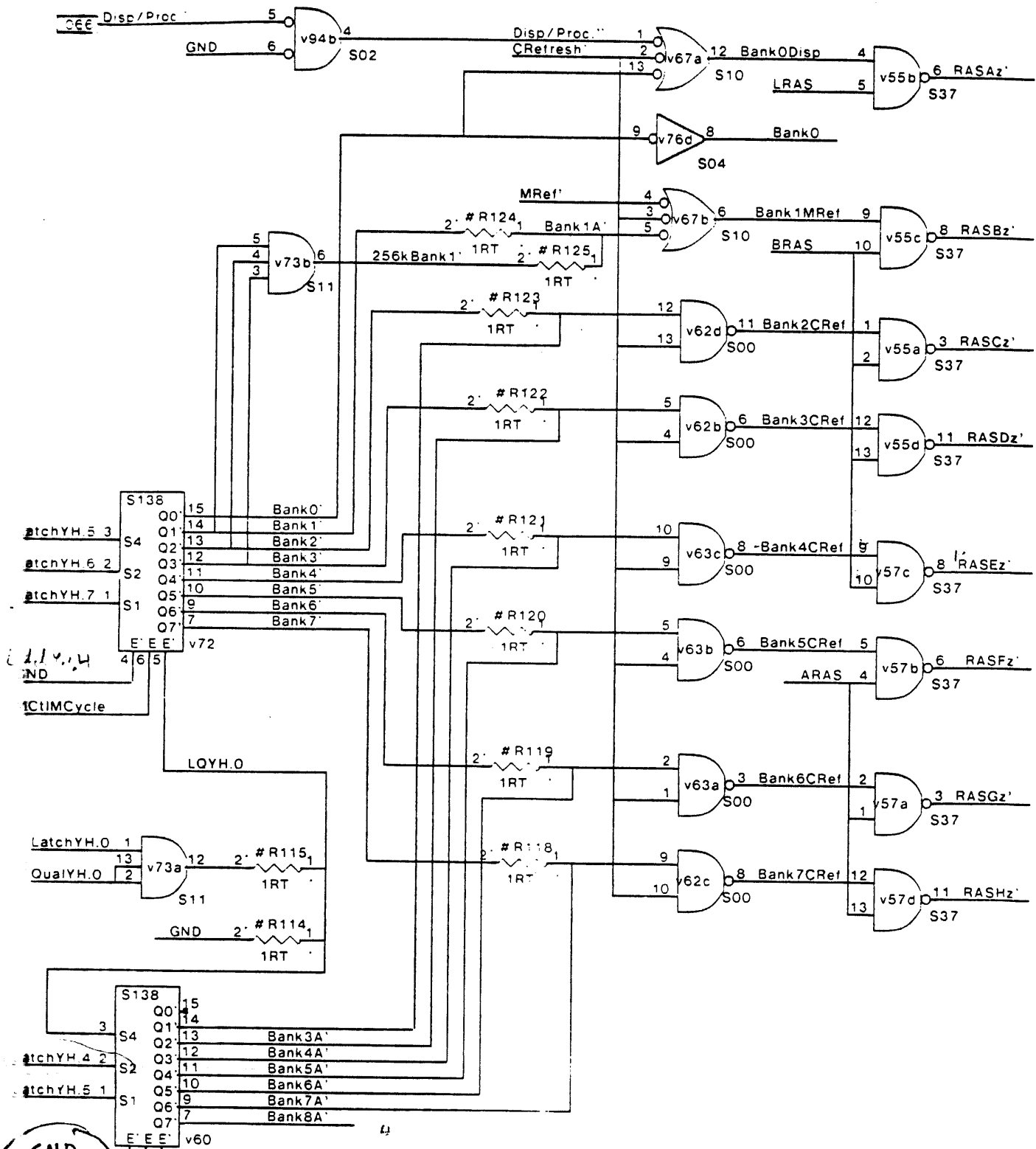
Write, CRefresh', MRef, LdMDR, CycleRcv, MDCIk, ←MD'

XEROX	Project	File	Designer	Rev	Date	Page
ED	MCCP	Write, CRefresh', MRef, LdMDR, CycleRcv, MDCIk, ←MD'	S. Ando	A	8/31/83	1



Address Selection, Refresh Counter & CAS Registers





GND
mCycle
GND
mCycle
mCycle

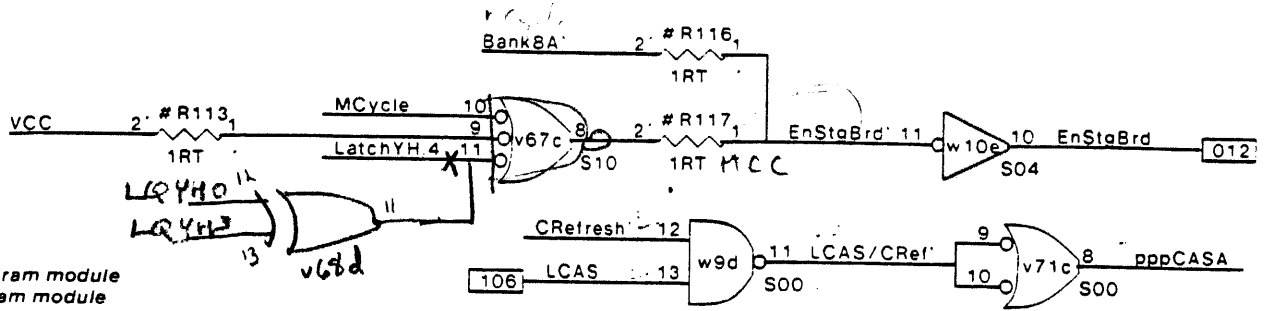
Note: v60 is socketed

Omit R115, R125, u160, and u173 for 64k dram module.

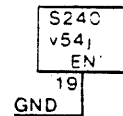
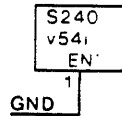
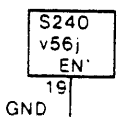
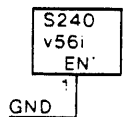
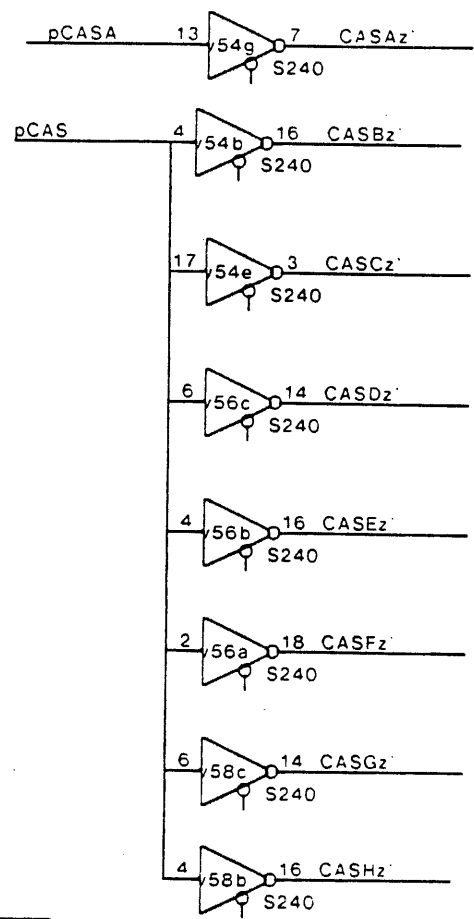
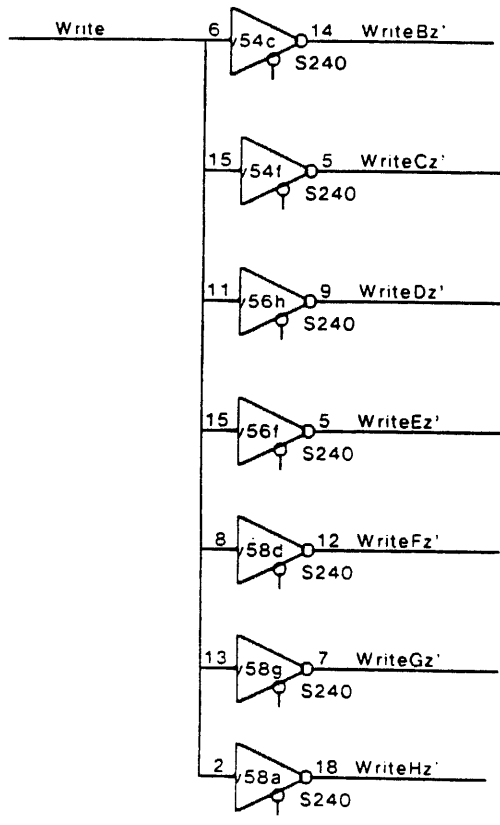
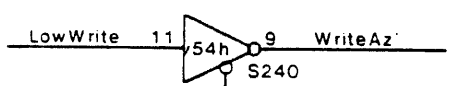
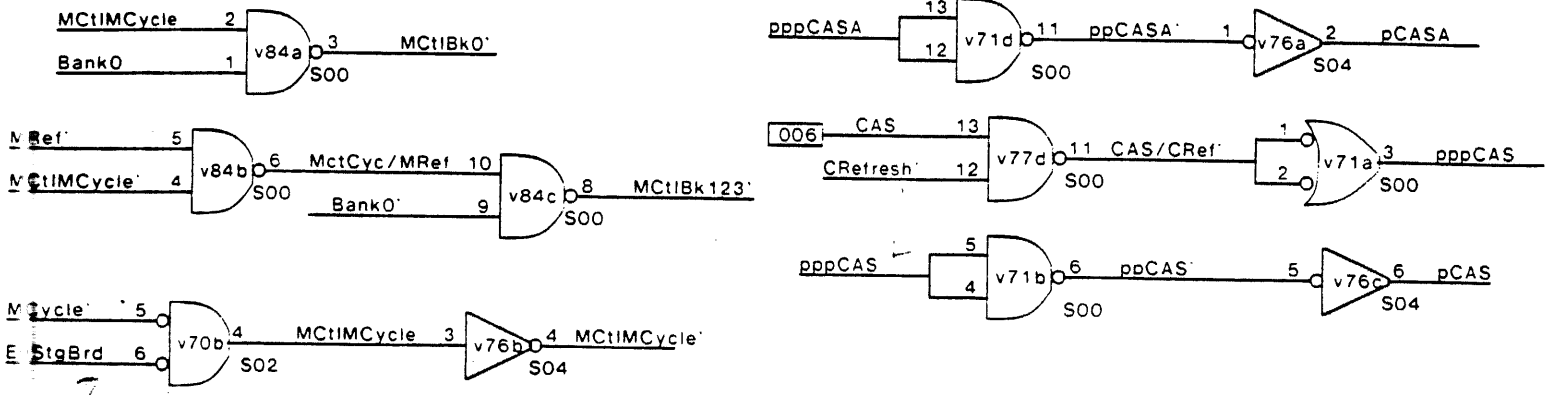
Omit R116, 119, 120, 121, 122, 123, and 124 for 256k dram module.
Omit R115 for 256k dram module (1 mw).
Omit R114 for 256k dram module (2 mw).

Memory Bank Selection

XEROX ED	Project MCCP	Memory Bank Selection	File PMCCP04.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 4
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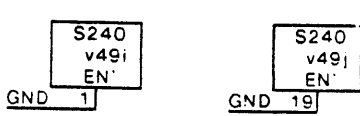
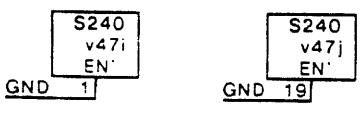
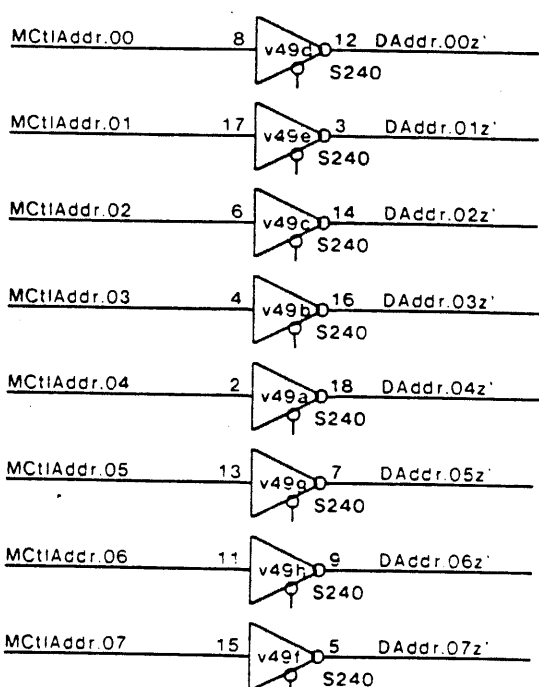
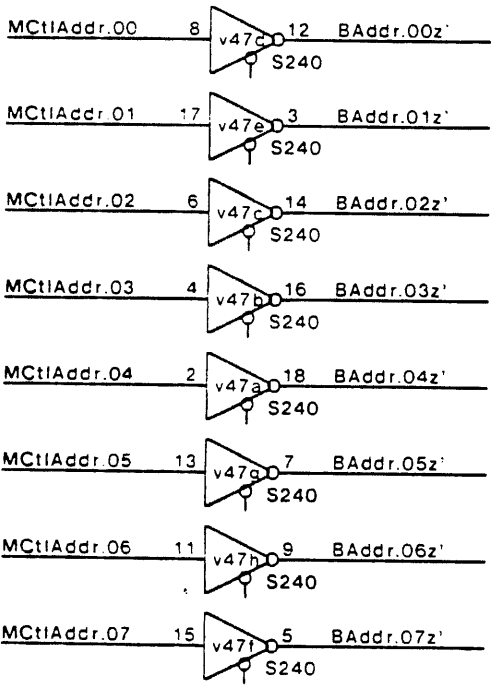
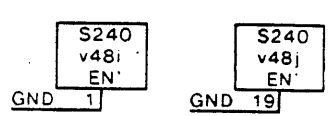
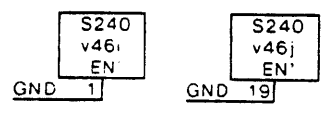
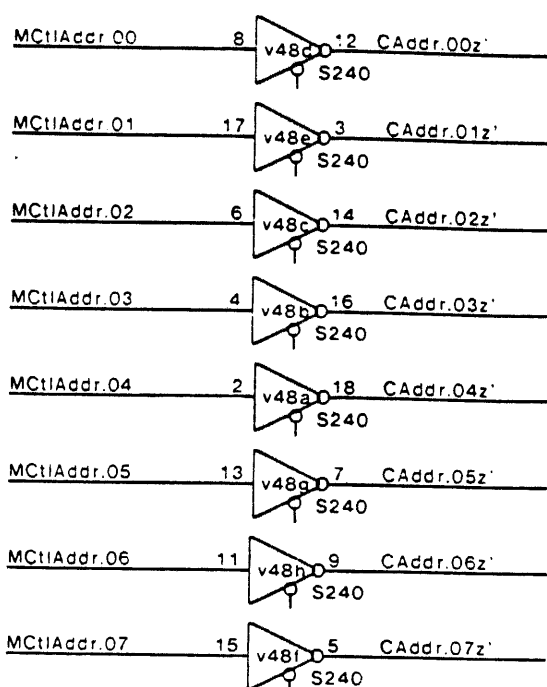
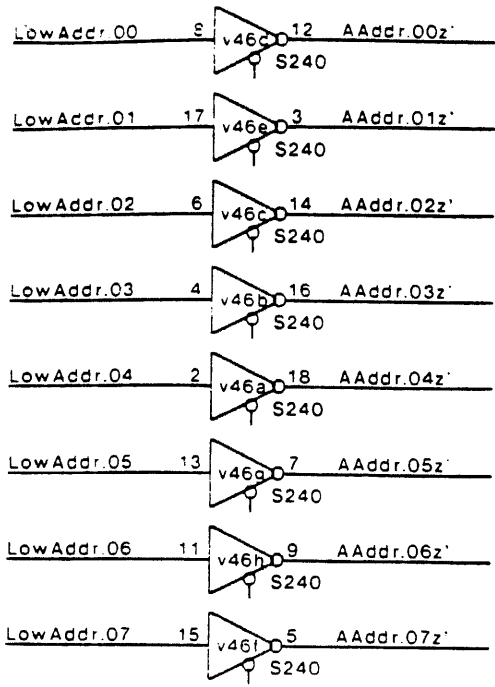


Omit R117 for 256k dram module
Omit R116 for 64k dram module



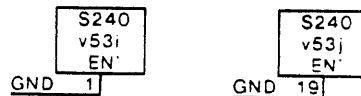
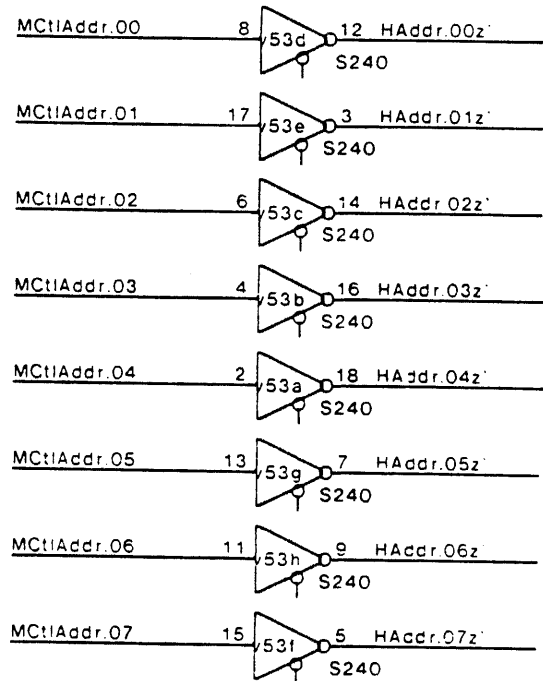
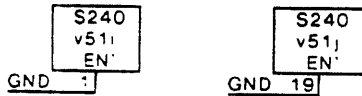
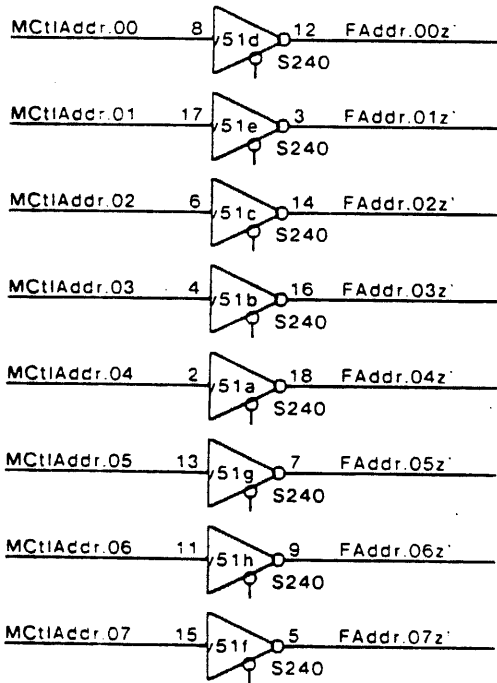
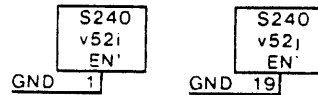
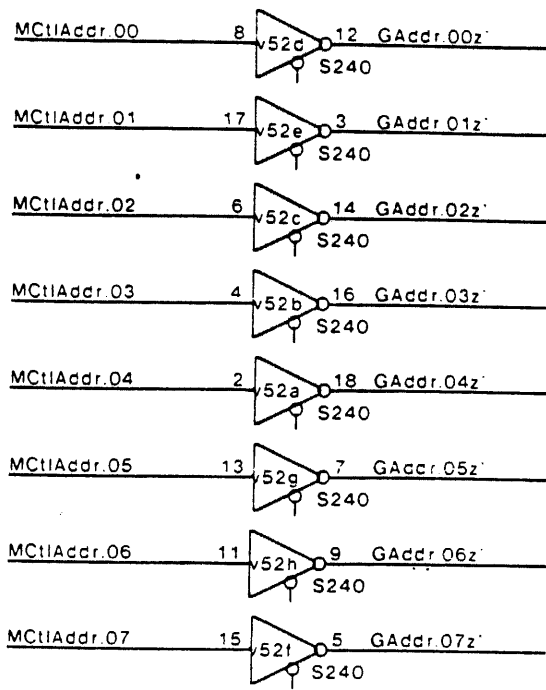
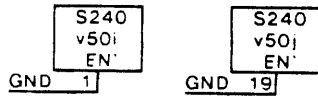
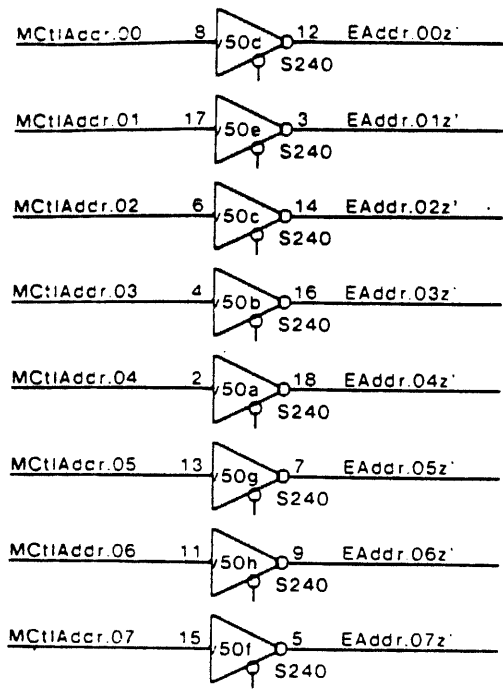
Memory Bank Selection/ Drivers for Write' and CAS'

EROX ED	Project MCCP	Memory Bank Selection Drivers for Write' & CAS'	File PMCCP05.sil	Designer S. Ando	Rev A	Date 10/17/83	Page 5
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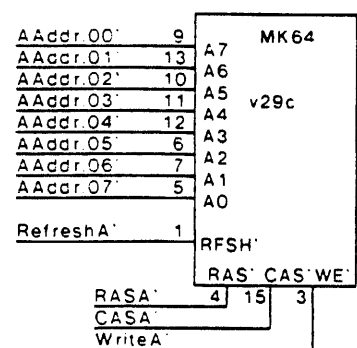
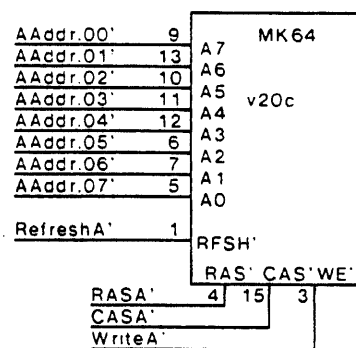
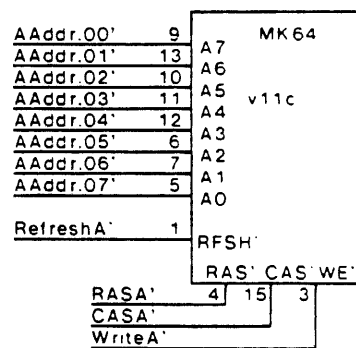
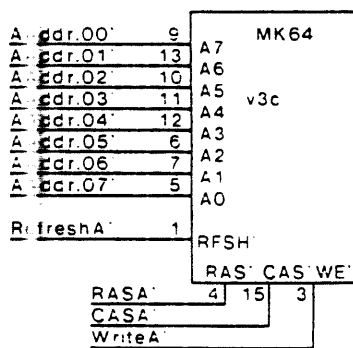
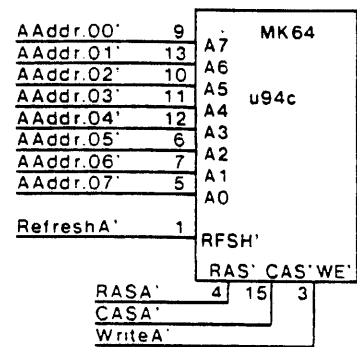
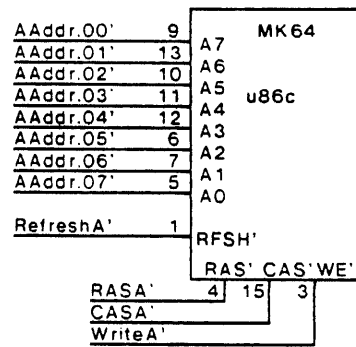
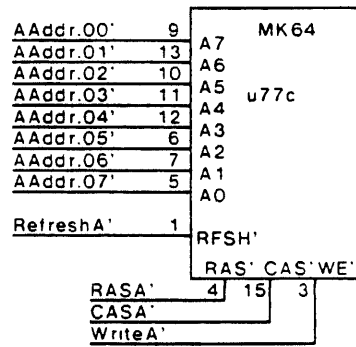
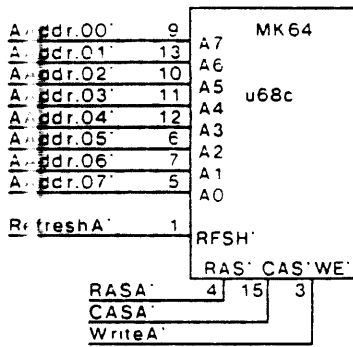
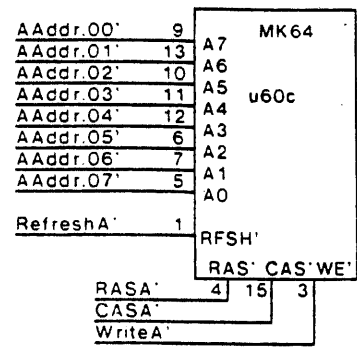
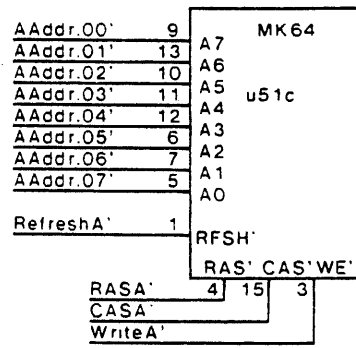
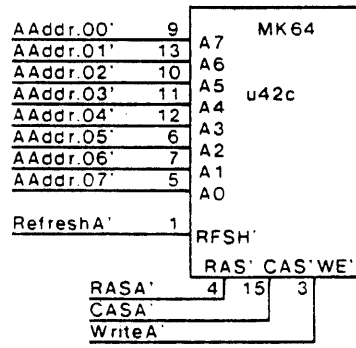
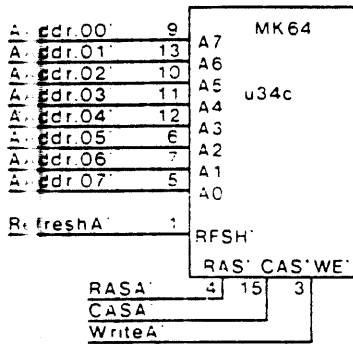
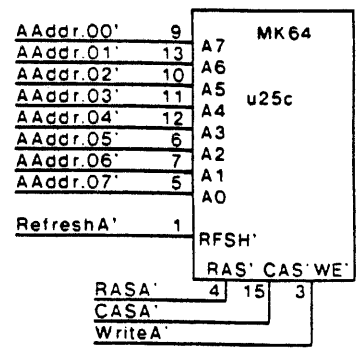
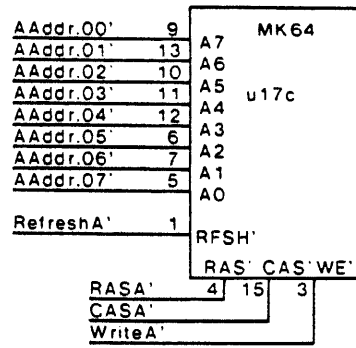
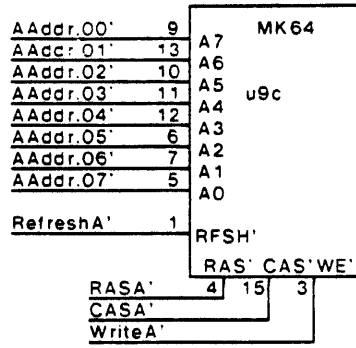
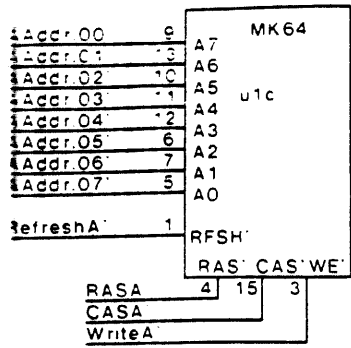
Address Drivers

XEROX ED	Project MCCP	Address Drivers	File PMCCP06.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 6
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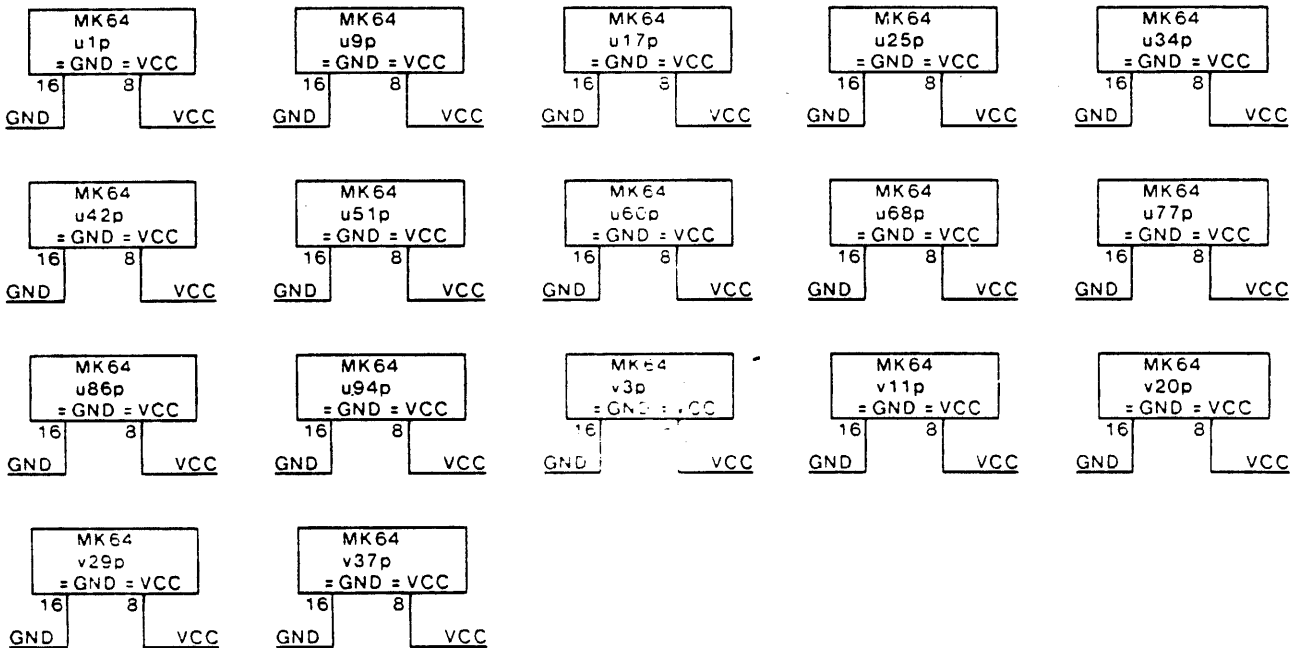
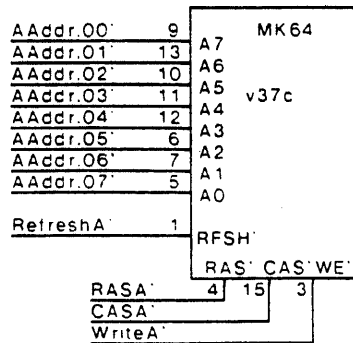
Address Drivers

> EROX ED	Project MCCP	Address Drivers	File PMCCP07.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 7
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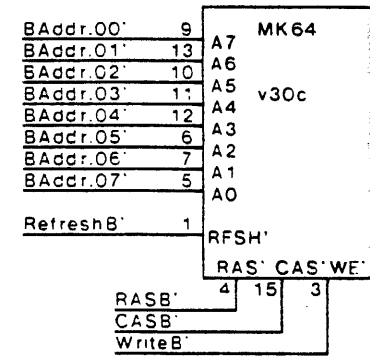
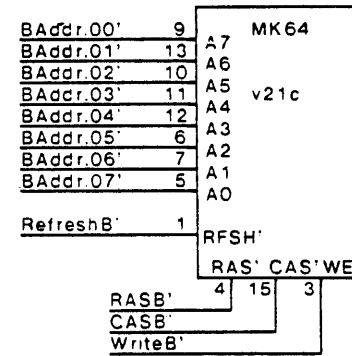
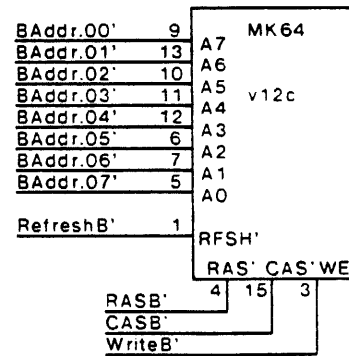
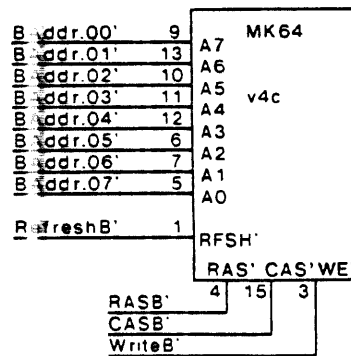
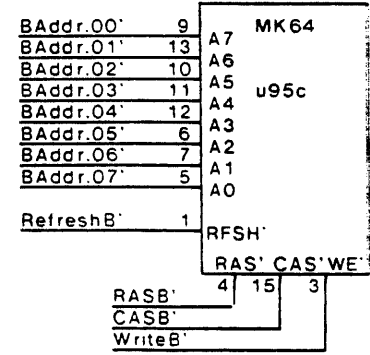
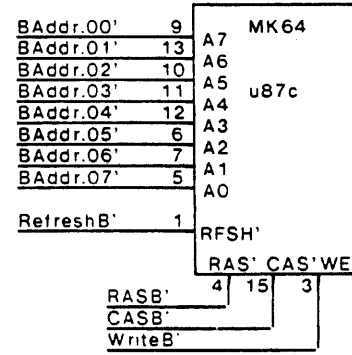
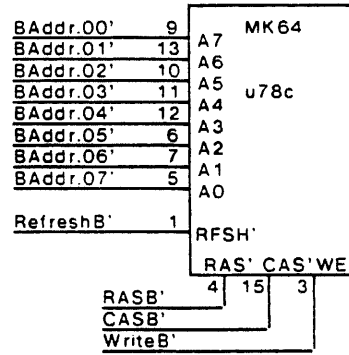
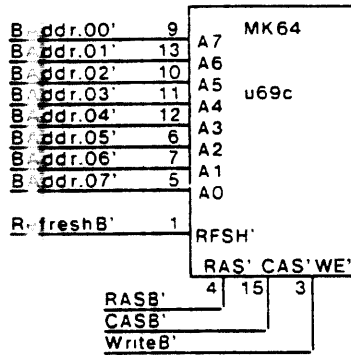
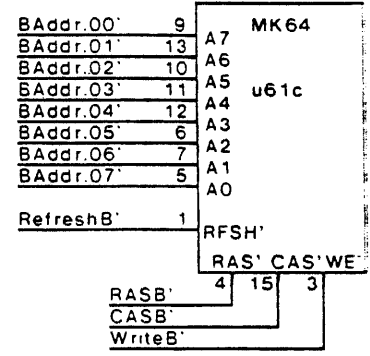
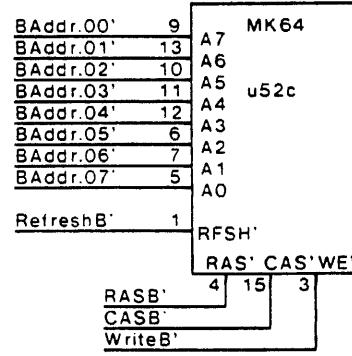
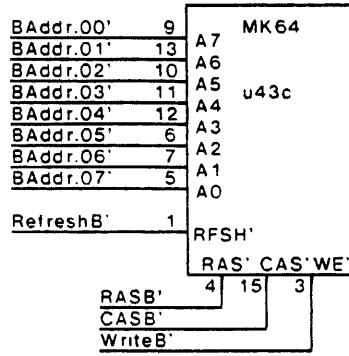
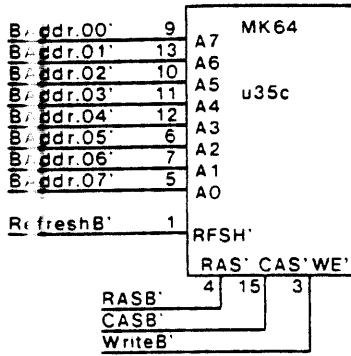
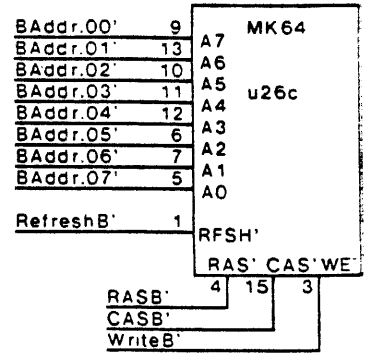
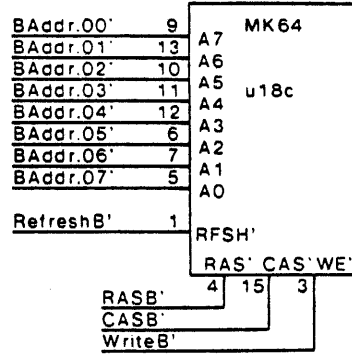
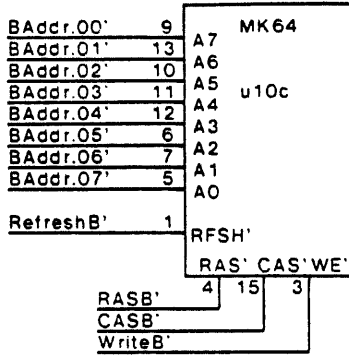
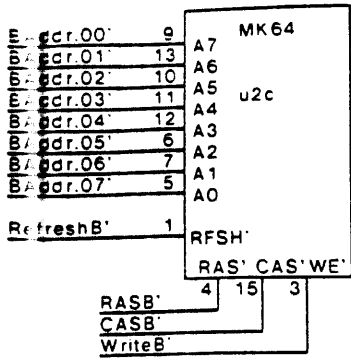
Address,RAS,CAS,Write Display Bank

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ED	MCCP	Address,RAS,CAS,Write Display Bank	PMCCP08.sil	S. Ando	A	8/31/83	8

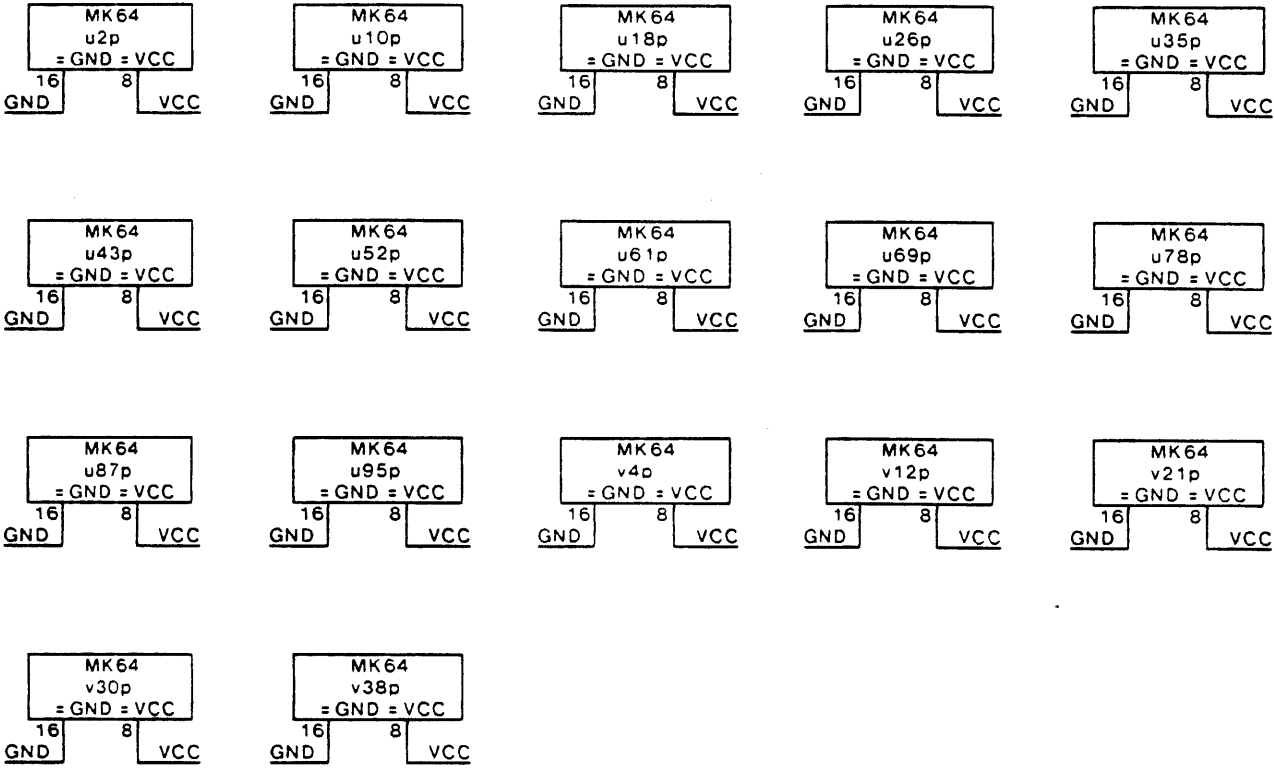
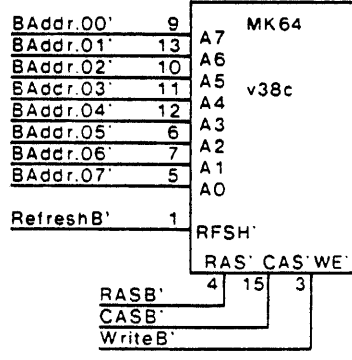


Address.RAS,CAS,Write Display Bank

VEROX ED	Project MCCP	Address.RAS,CAS,Write Display Bank	File PMCCP09.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 9
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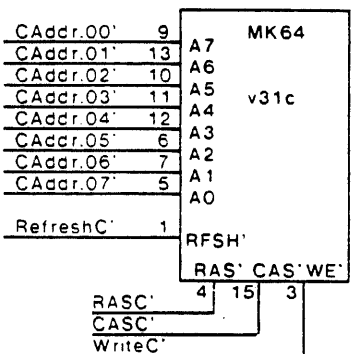
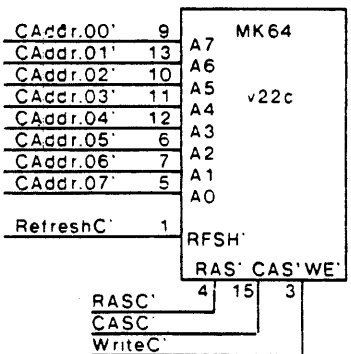
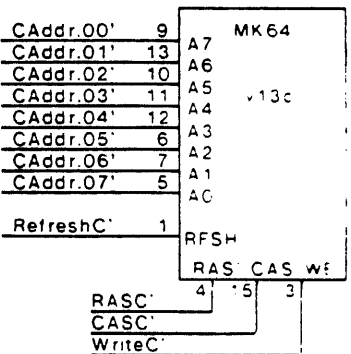
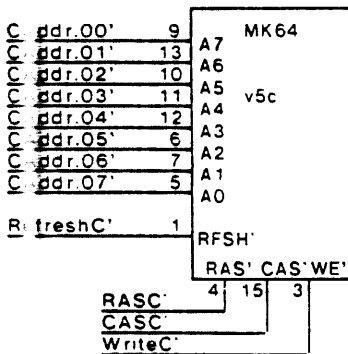
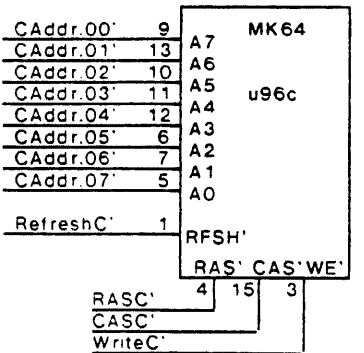
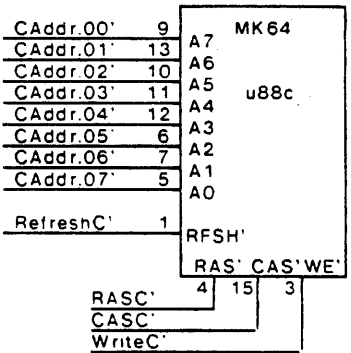
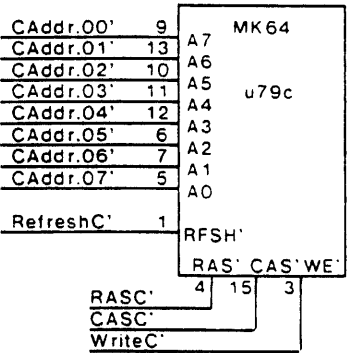
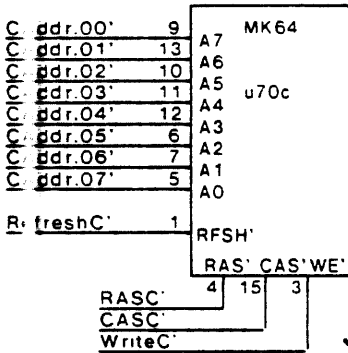
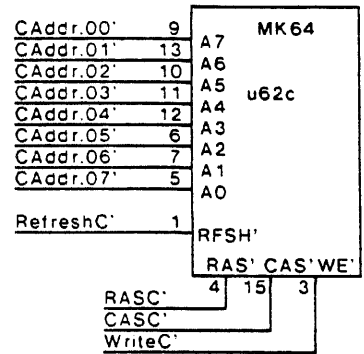
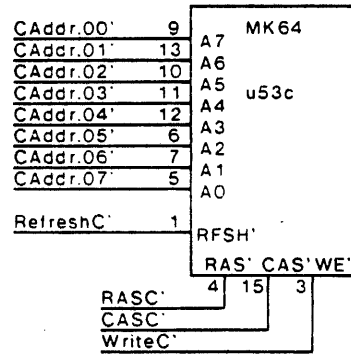
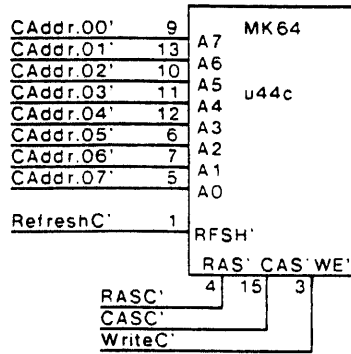
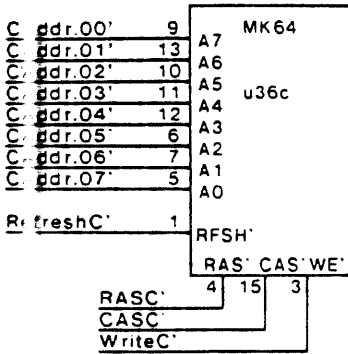
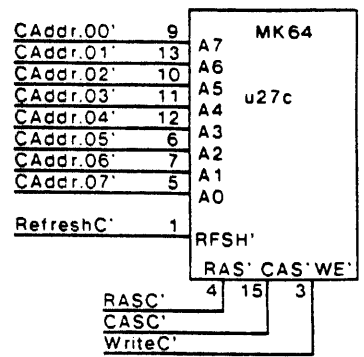
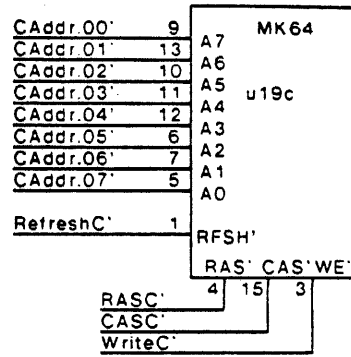
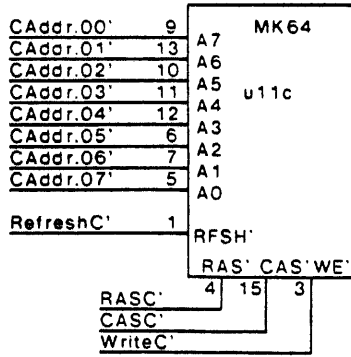
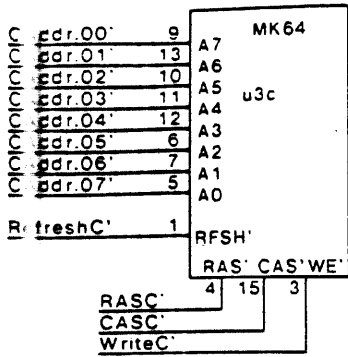


Mem. Control/ Bank B



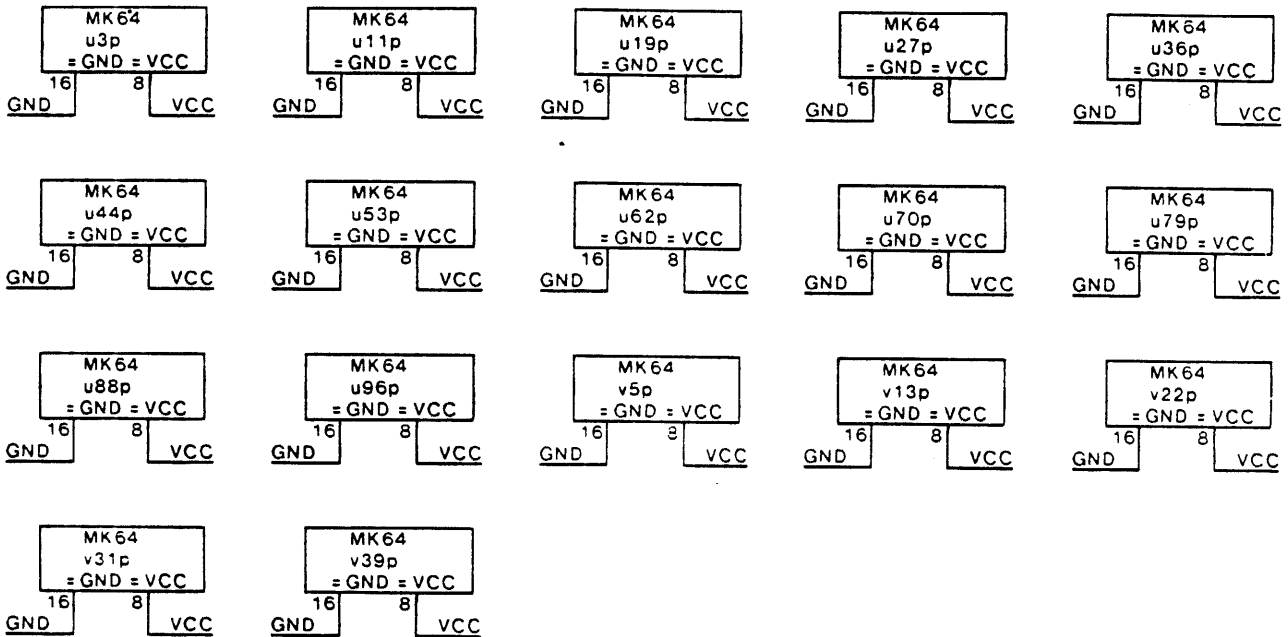
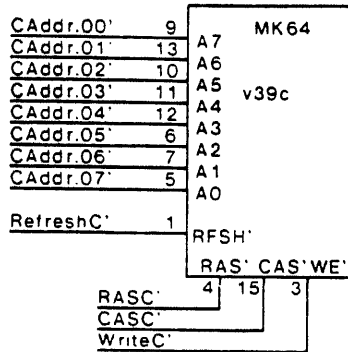
Mem. Control/ Bank B

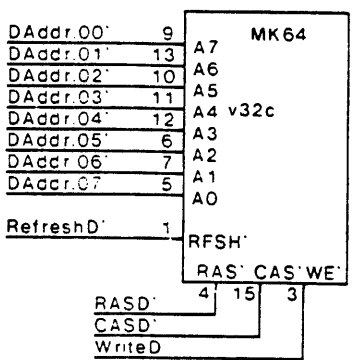
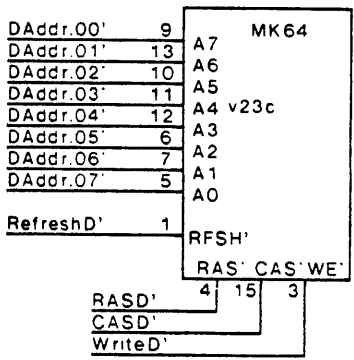
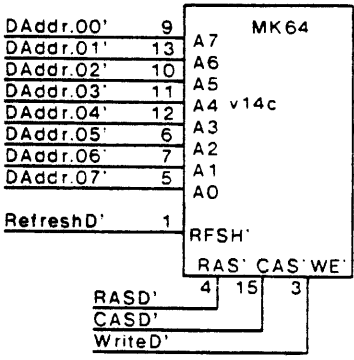
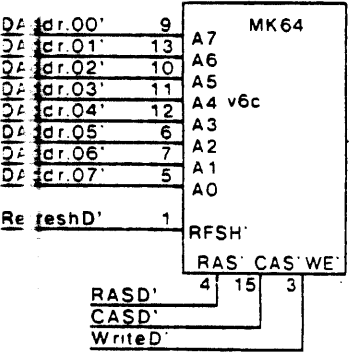
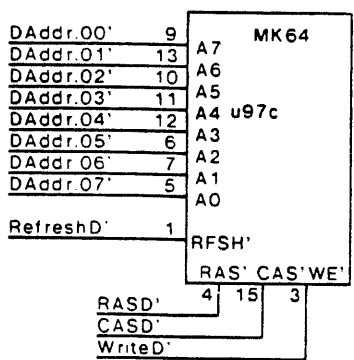
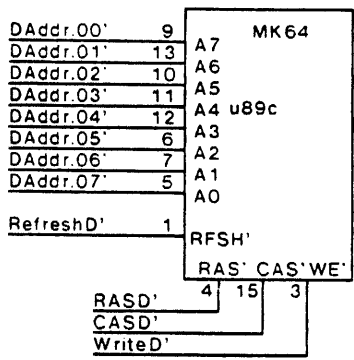
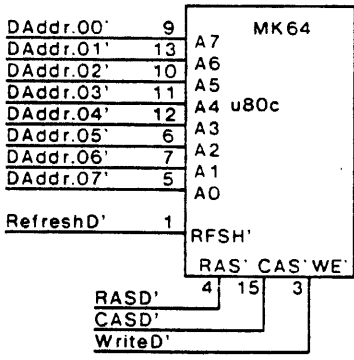
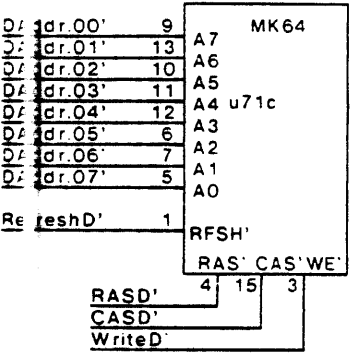
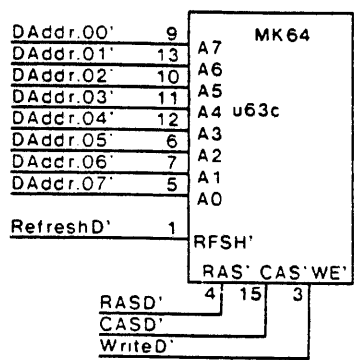
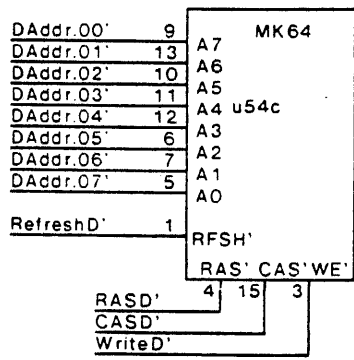
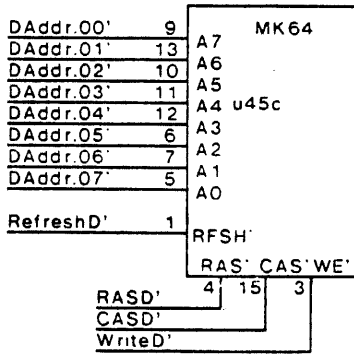
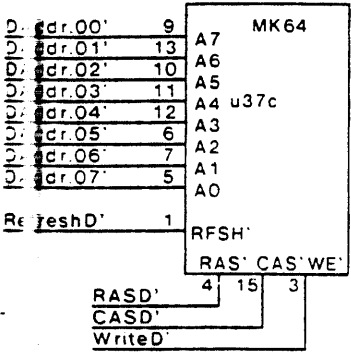
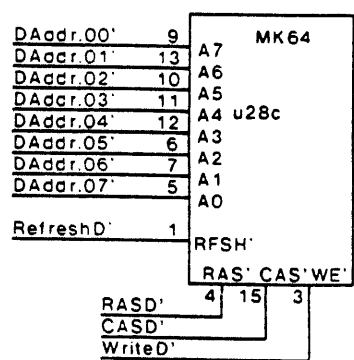
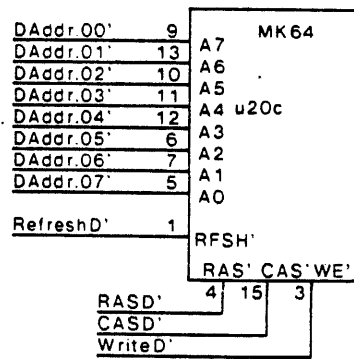
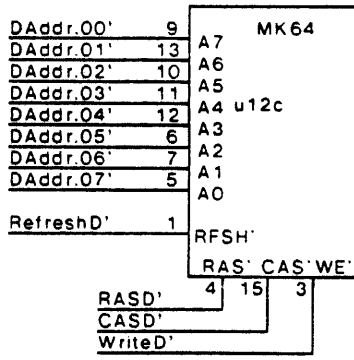
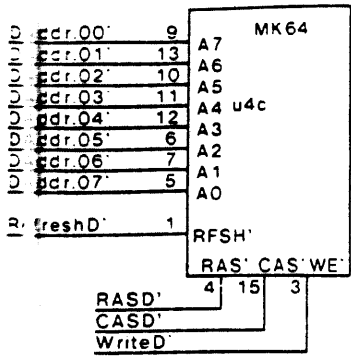
XEROX ED	Project MCCP	Mem. Control/ Bank B	File PMCCP11.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 11
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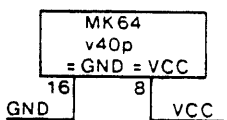
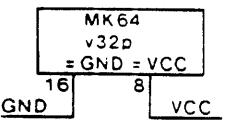
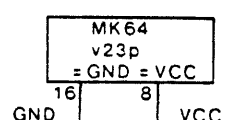
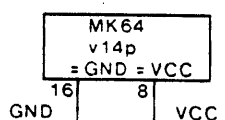
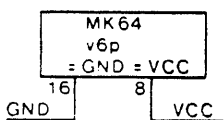
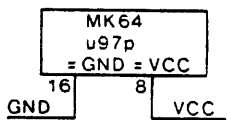
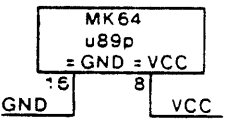
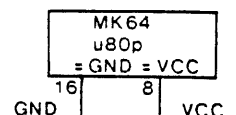
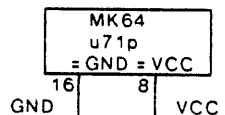
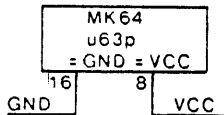
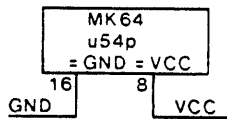
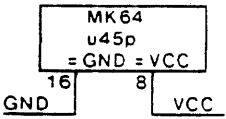
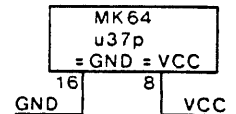
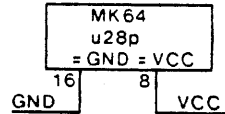
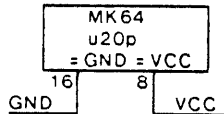
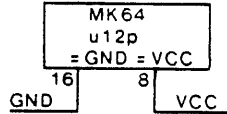
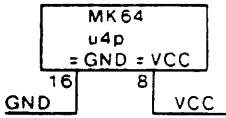
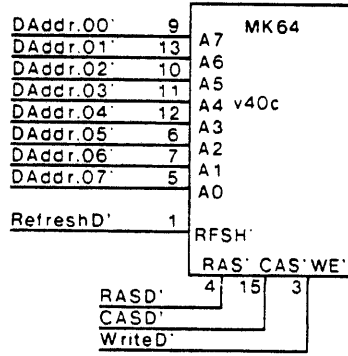


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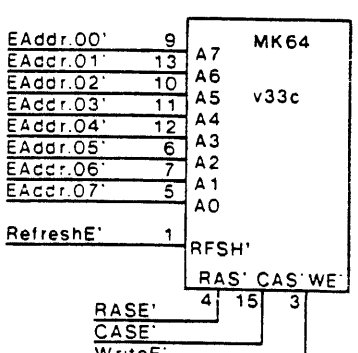
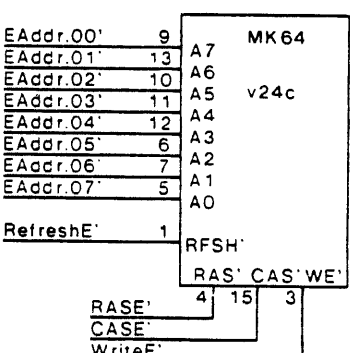
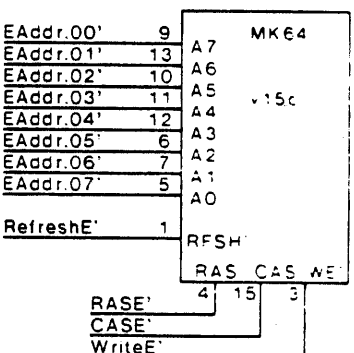
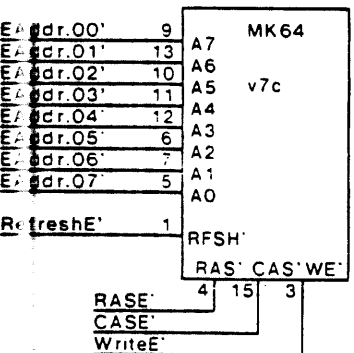
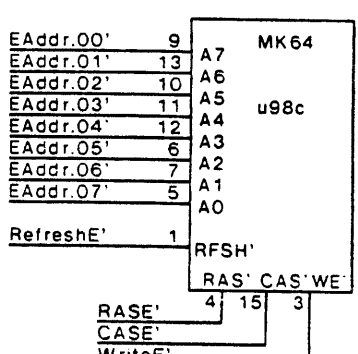
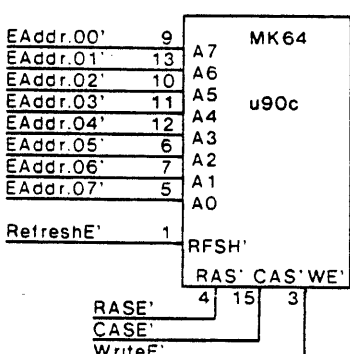
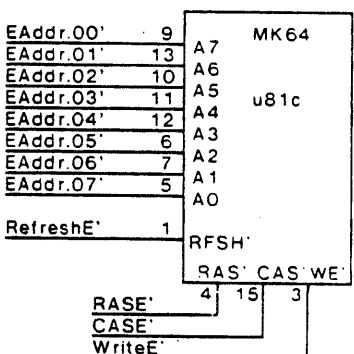
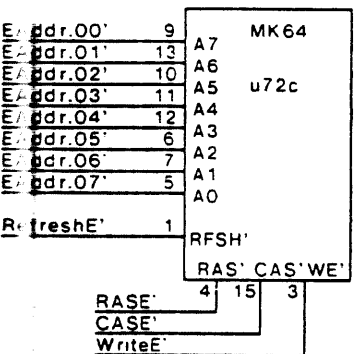
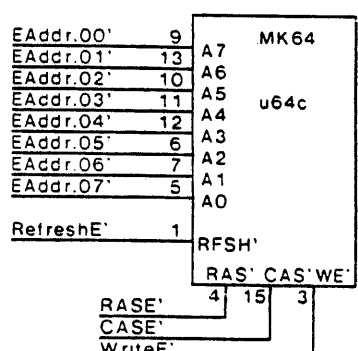
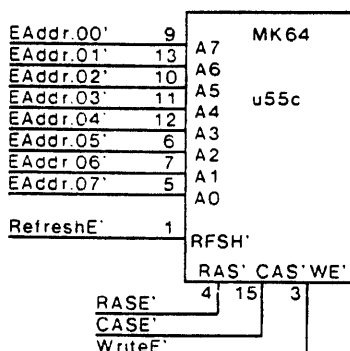
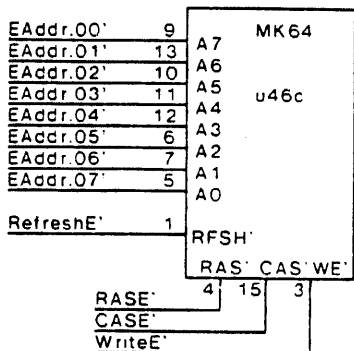
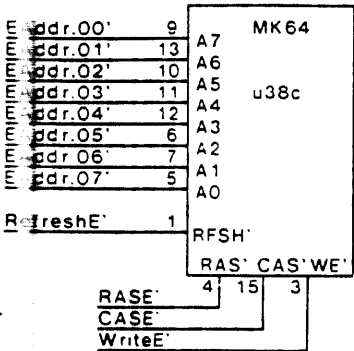
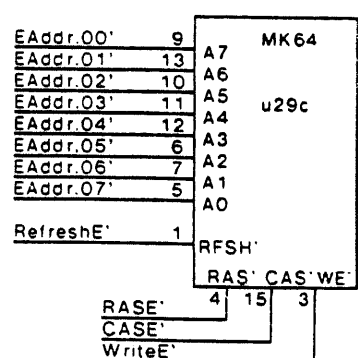
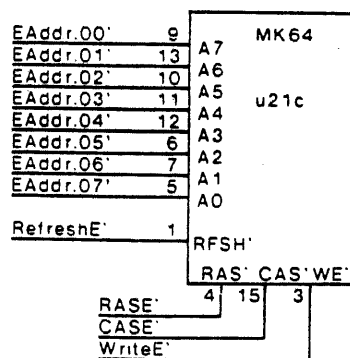
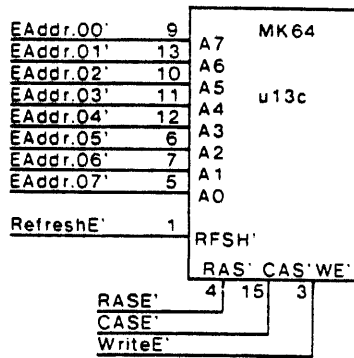
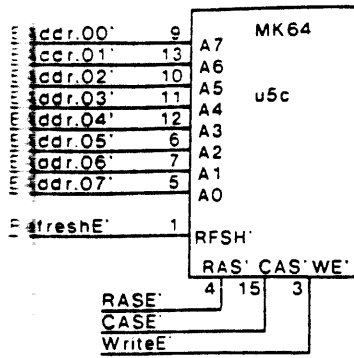
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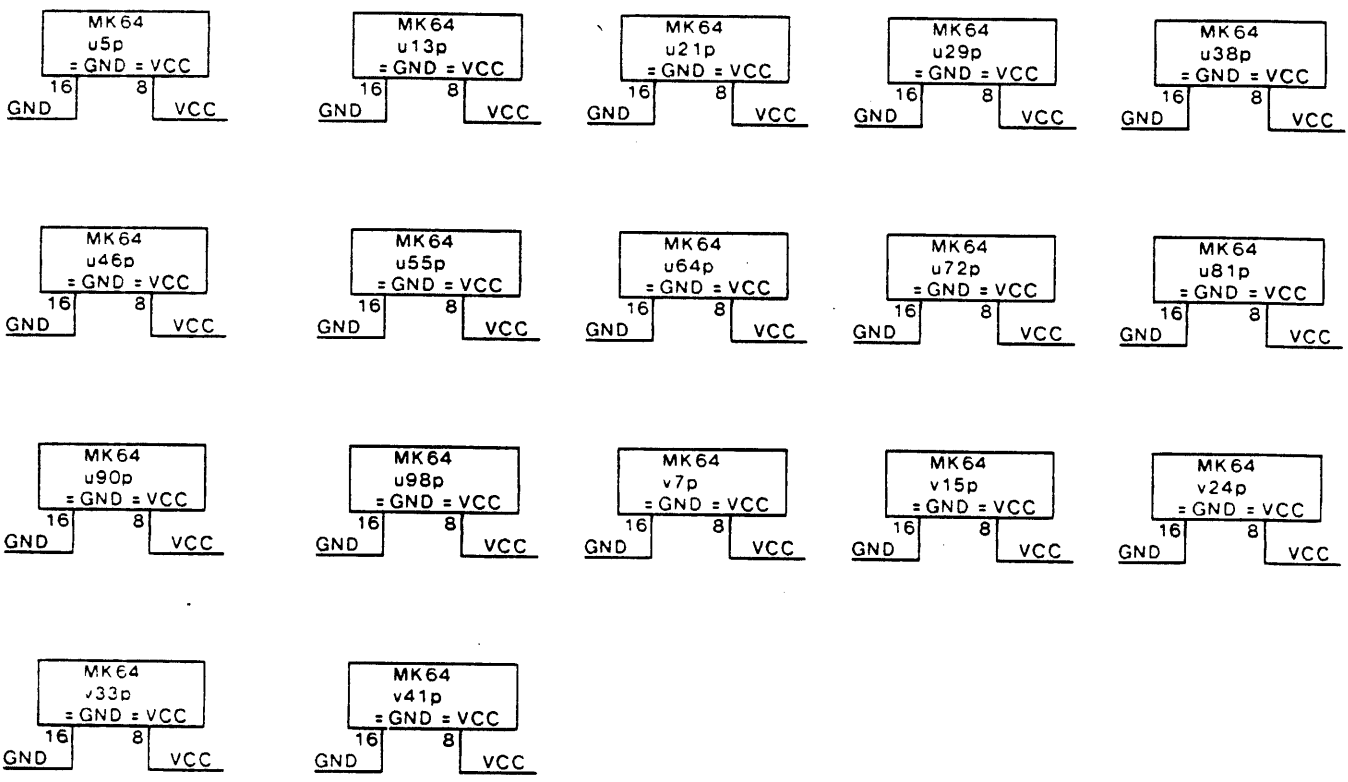
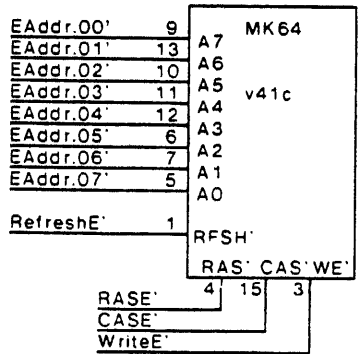


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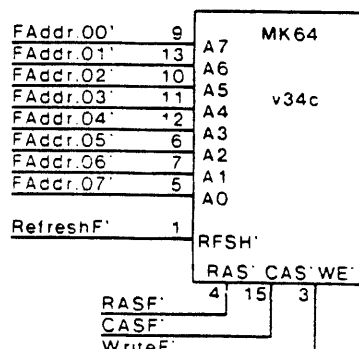
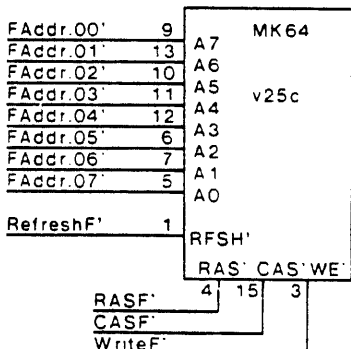
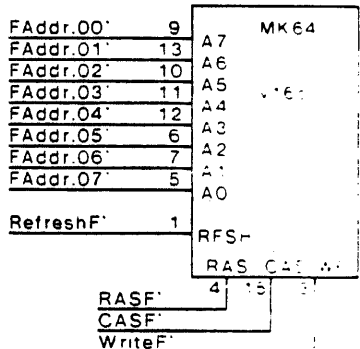
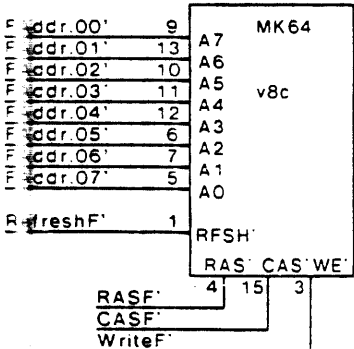
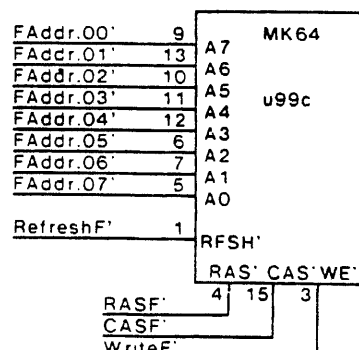
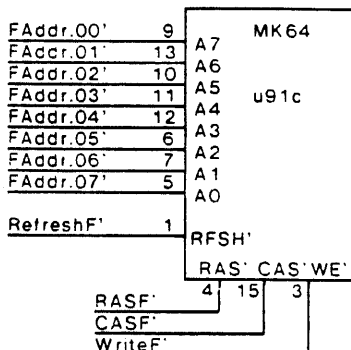
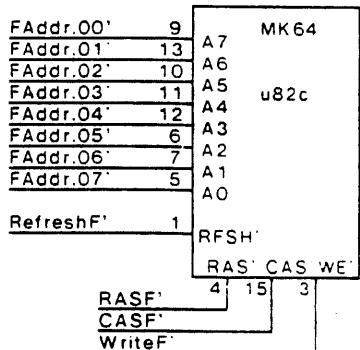
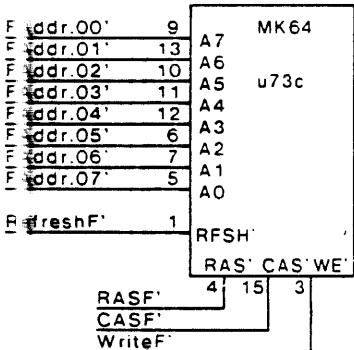
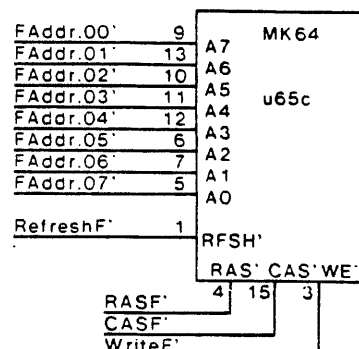
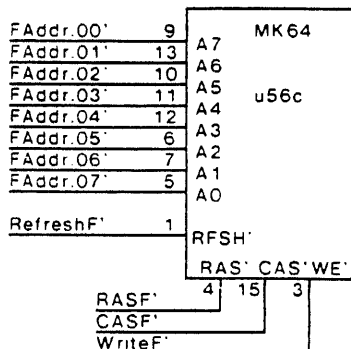
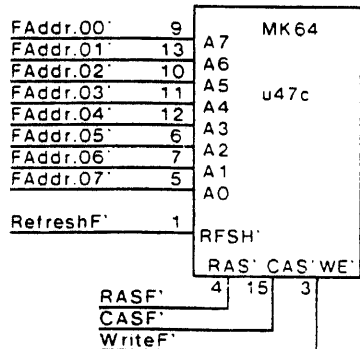
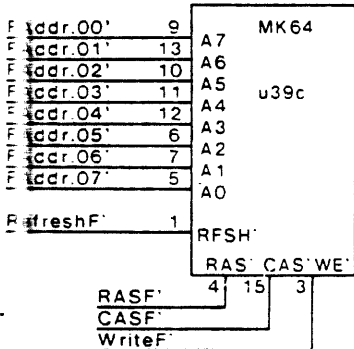
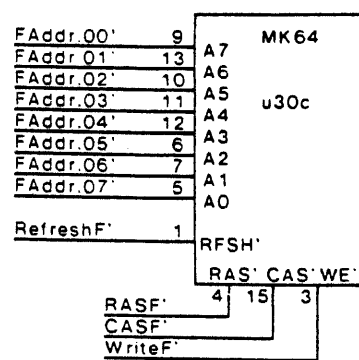
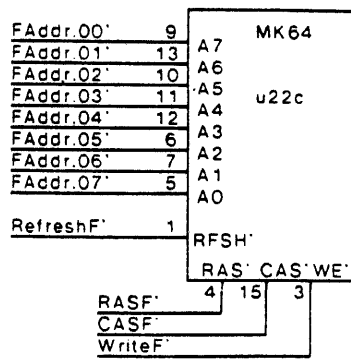
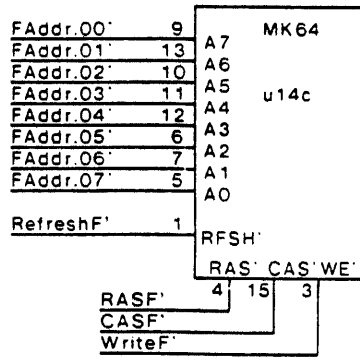
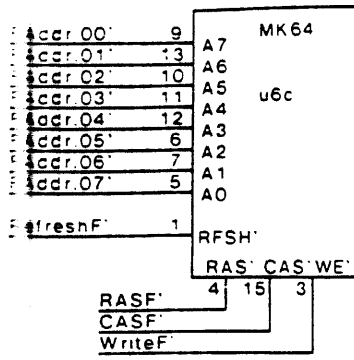


Mem. Control/ Bank E

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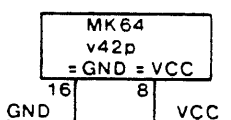
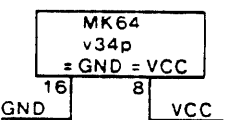
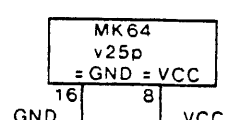
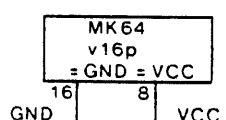
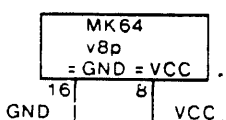
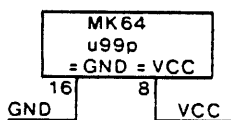
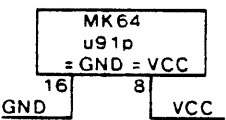
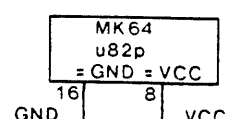
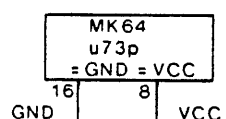
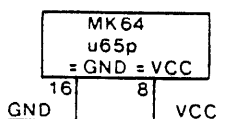
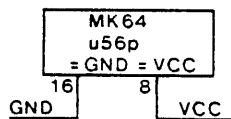
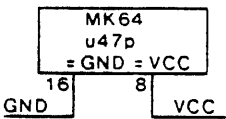
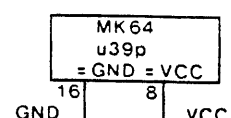
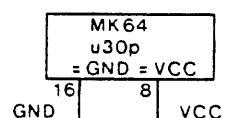
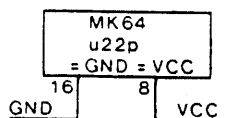
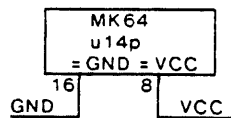
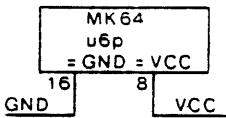
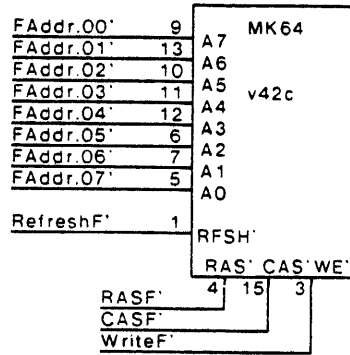


Mem. Control/ Bank E



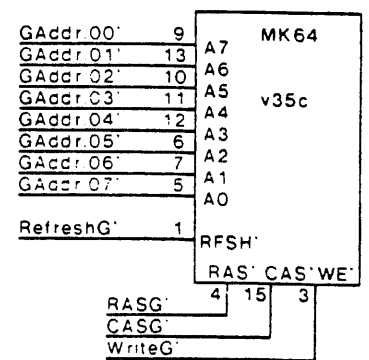
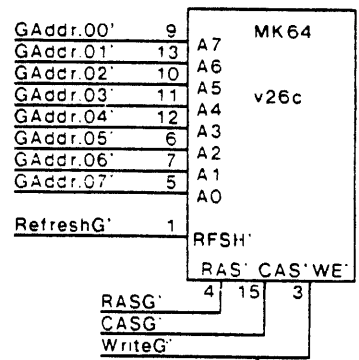
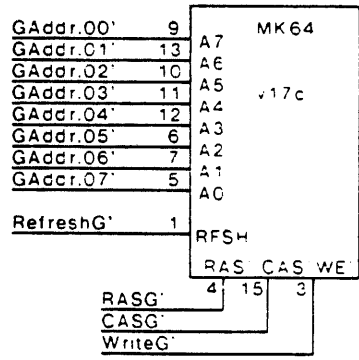
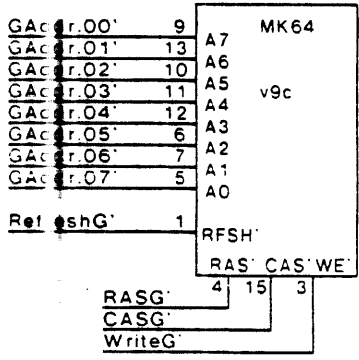
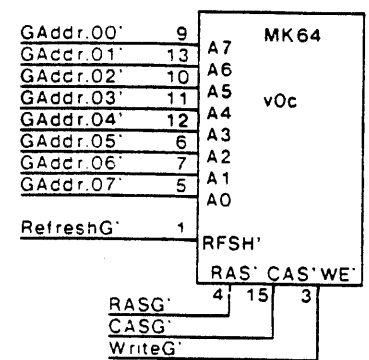
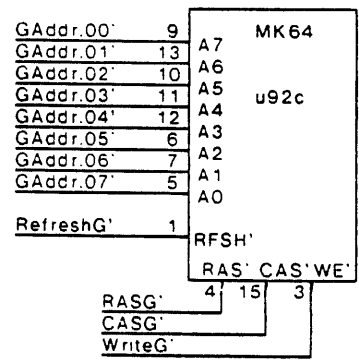
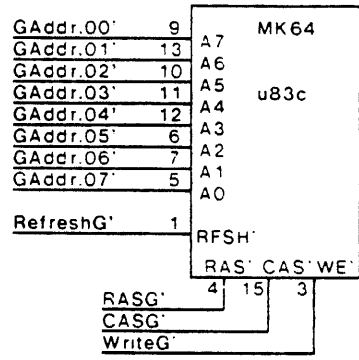
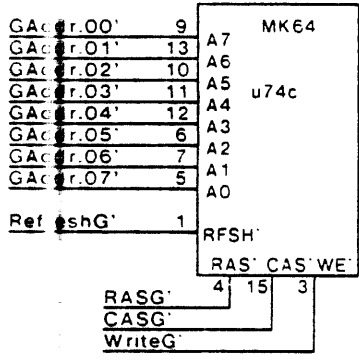
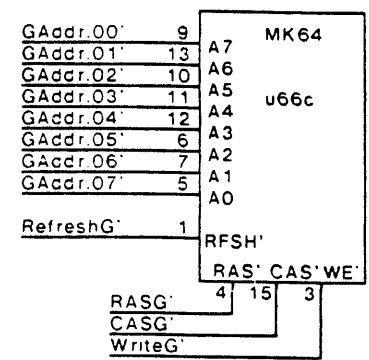
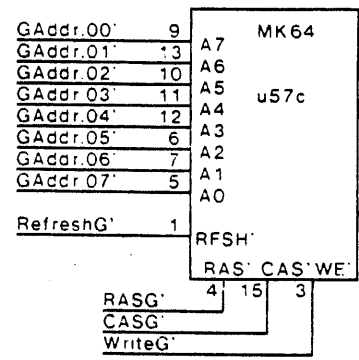
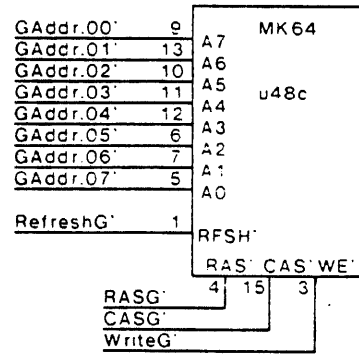
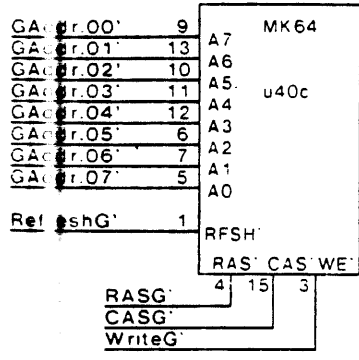
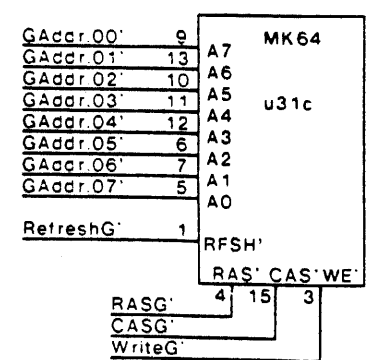
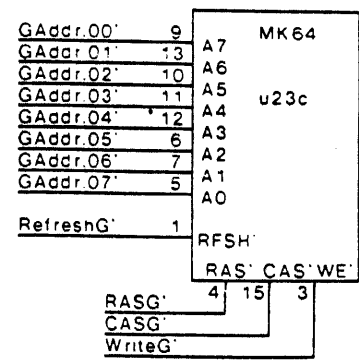
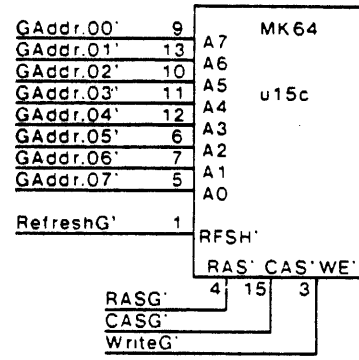
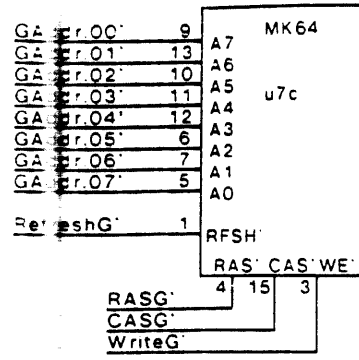
Mem. Control/ Bank F (no dram required for 256k dram module)

XEROX	Project	File	Designer	Rev	Date	Page
ED	MCCP	PMCCP18.sil	S. Ando	A	8/31/83	18



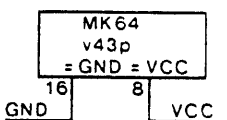
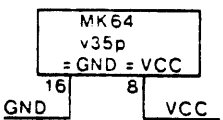
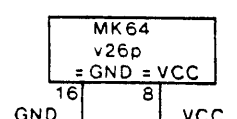
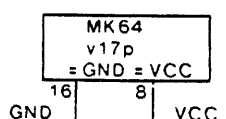
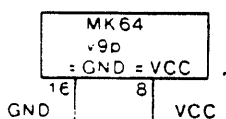
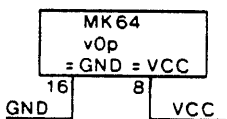
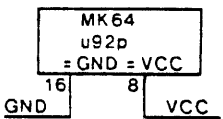
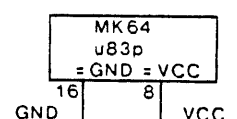
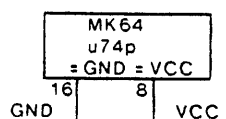
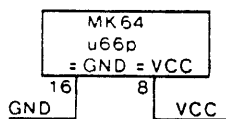
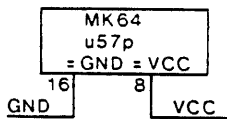
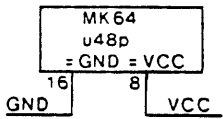
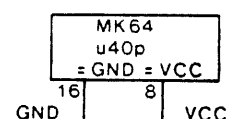
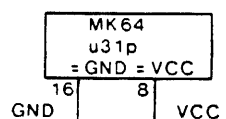
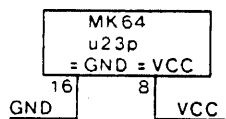
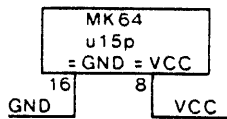
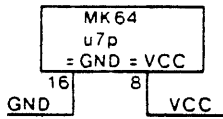
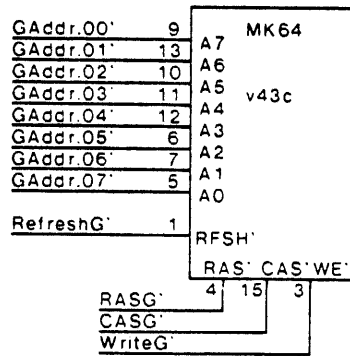
Mem. Control/ Bank F (no dram required for 256k dram module)

XEROX ED	Project MCCP	Mem. Control/ Bank F	File PMCCP19.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 19
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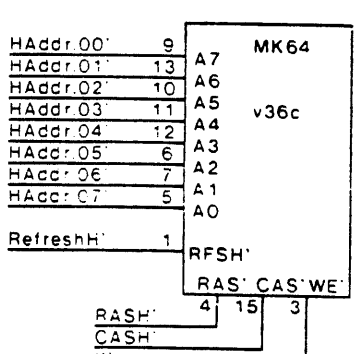
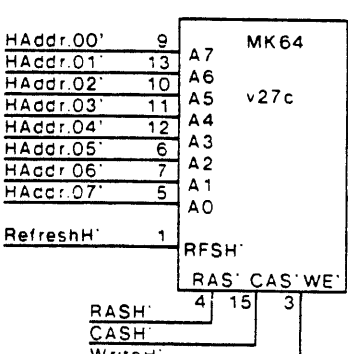
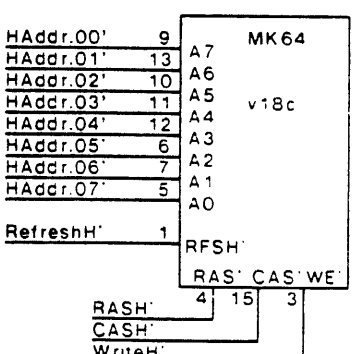
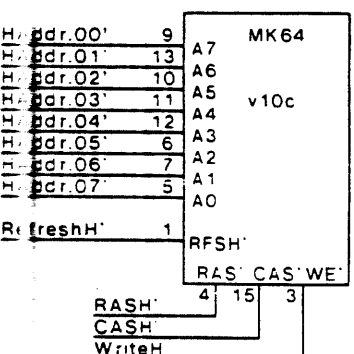
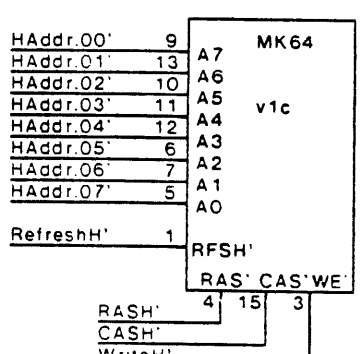
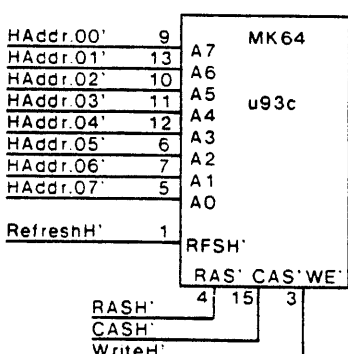
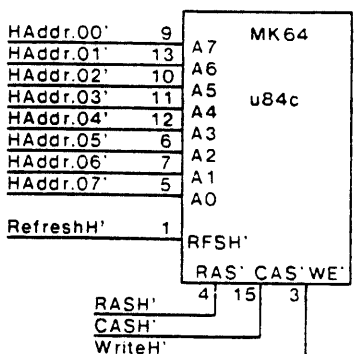
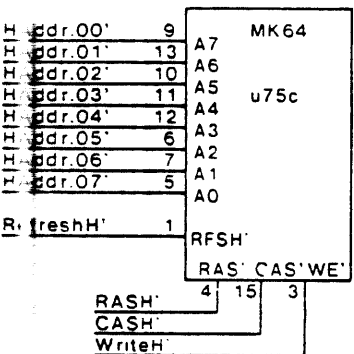
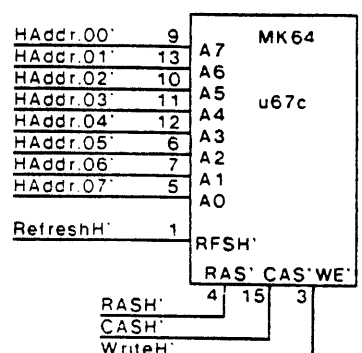
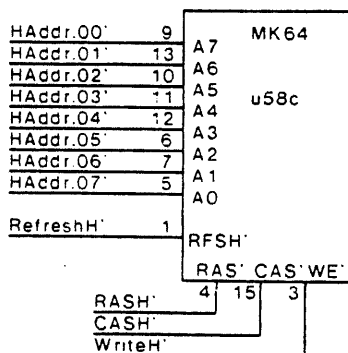
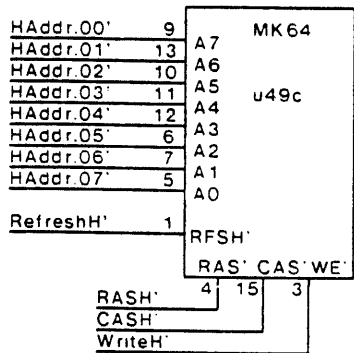
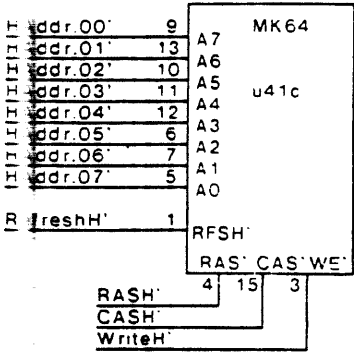
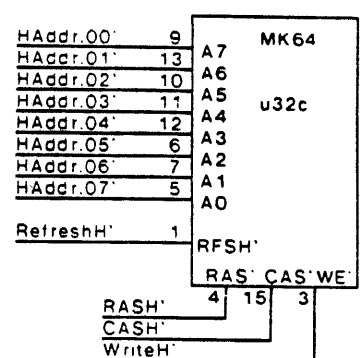
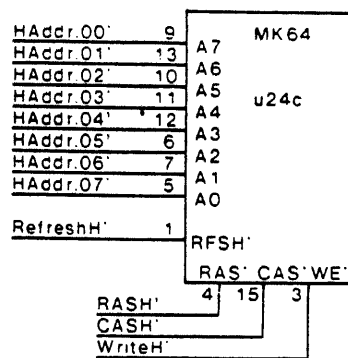
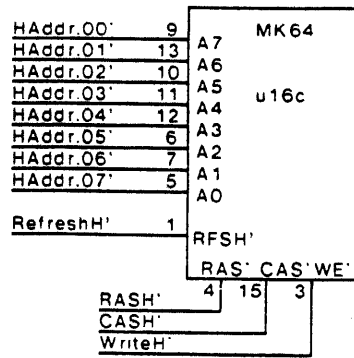
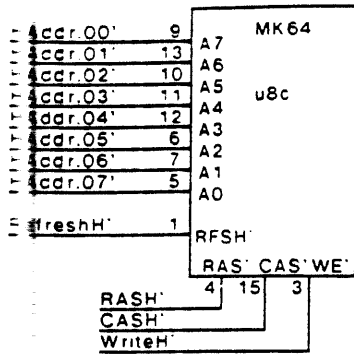
Mem. Control/ Bank G (no dram required for 256k dram module)

XEROX ED	Project MCCP	Mem. Control/ Bank G	File PMCCP20.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 20
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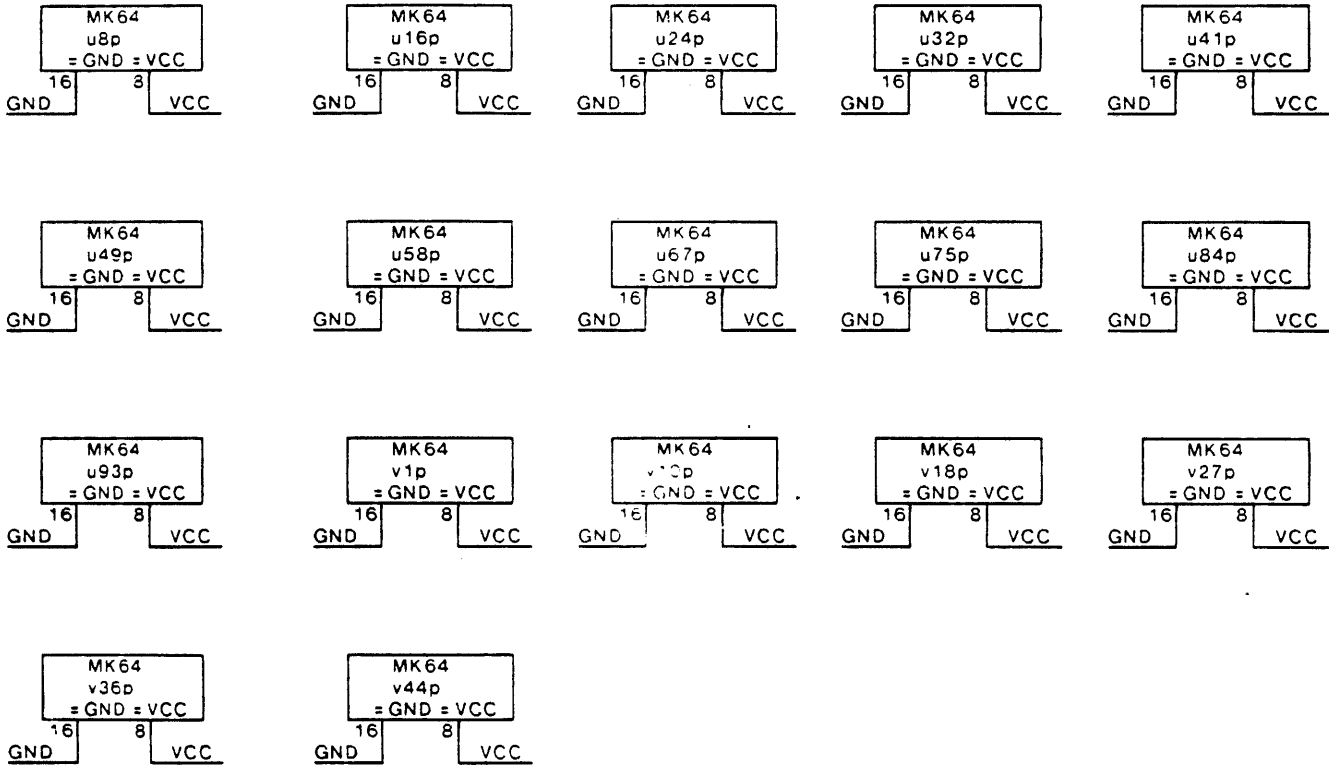
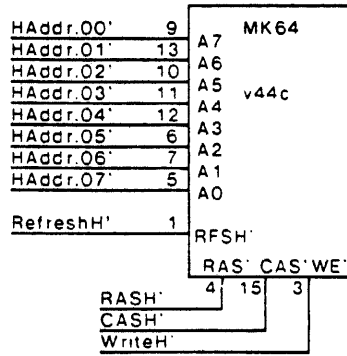
Mem. Control/ Bank G (no dram required for 256k dram module)

XEROX ED	Project MCCP	Mem. Control/ Bank G	File PMCCP21.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 21
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Mem. Control/ Bank H (no dram required for 256k dram module)

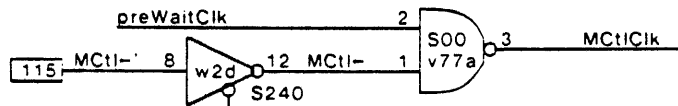
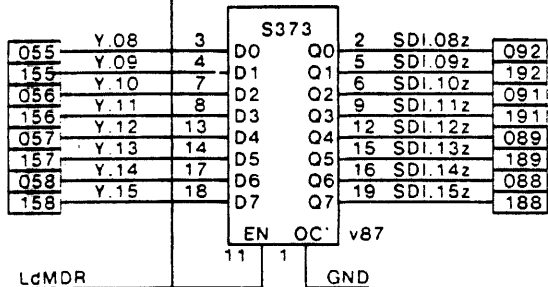
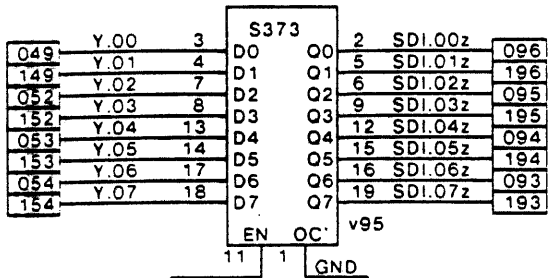
XEROX ED	Project MCCP	File Mem. Control/ Bank H	PMCCP22.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 22
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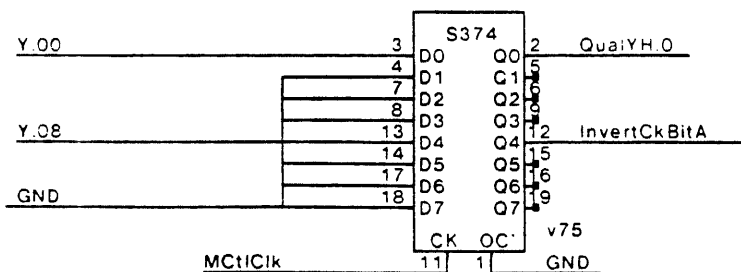
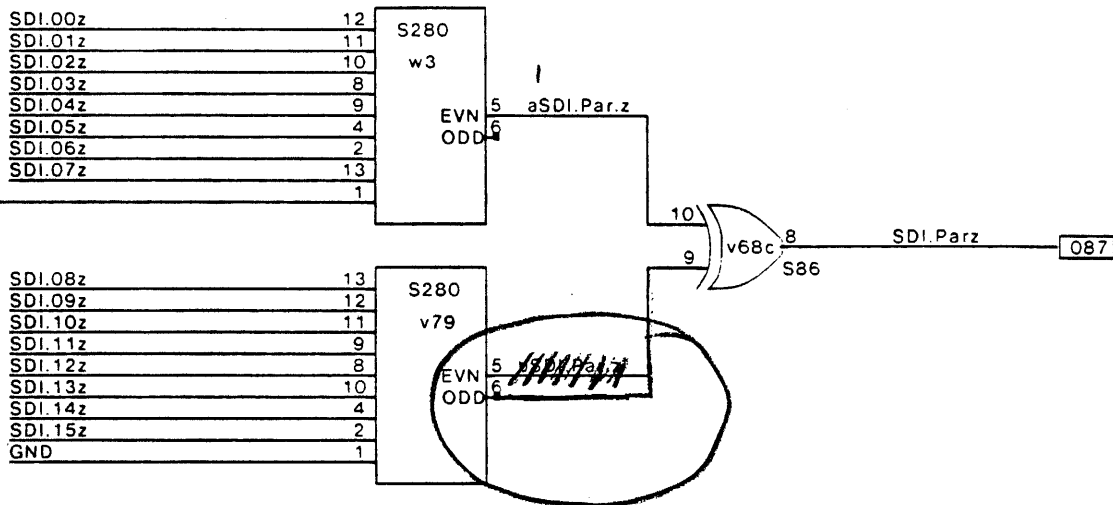
Mem. Control/ Bank H (no dram required for 256k dram module)

XEROX ED	Project MCCP	Mem. Control/ Bank H	File PMCCP23.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 23
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MDR



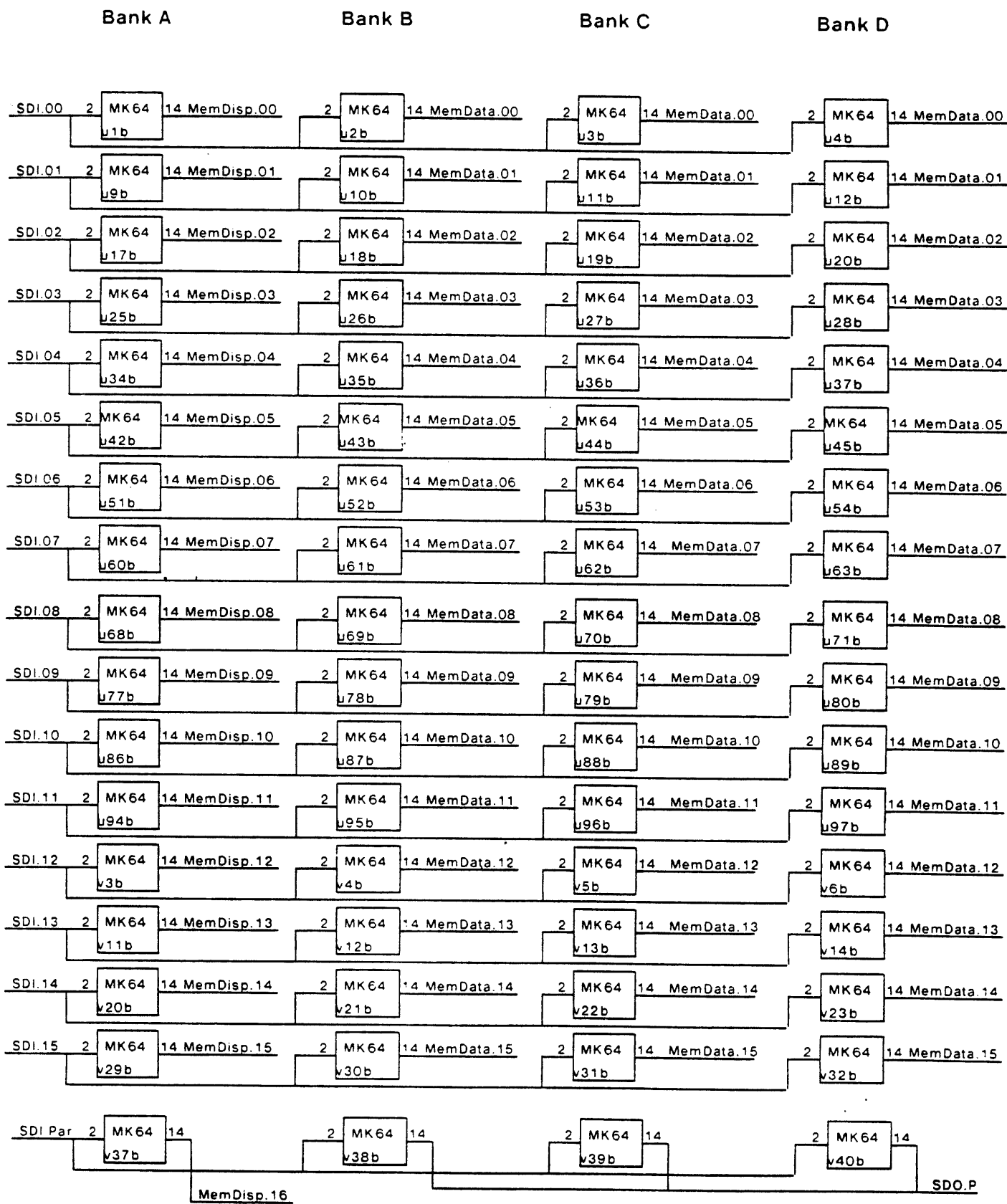
Enable logic on Pg.28



Data bits come from memory data register (MDR)

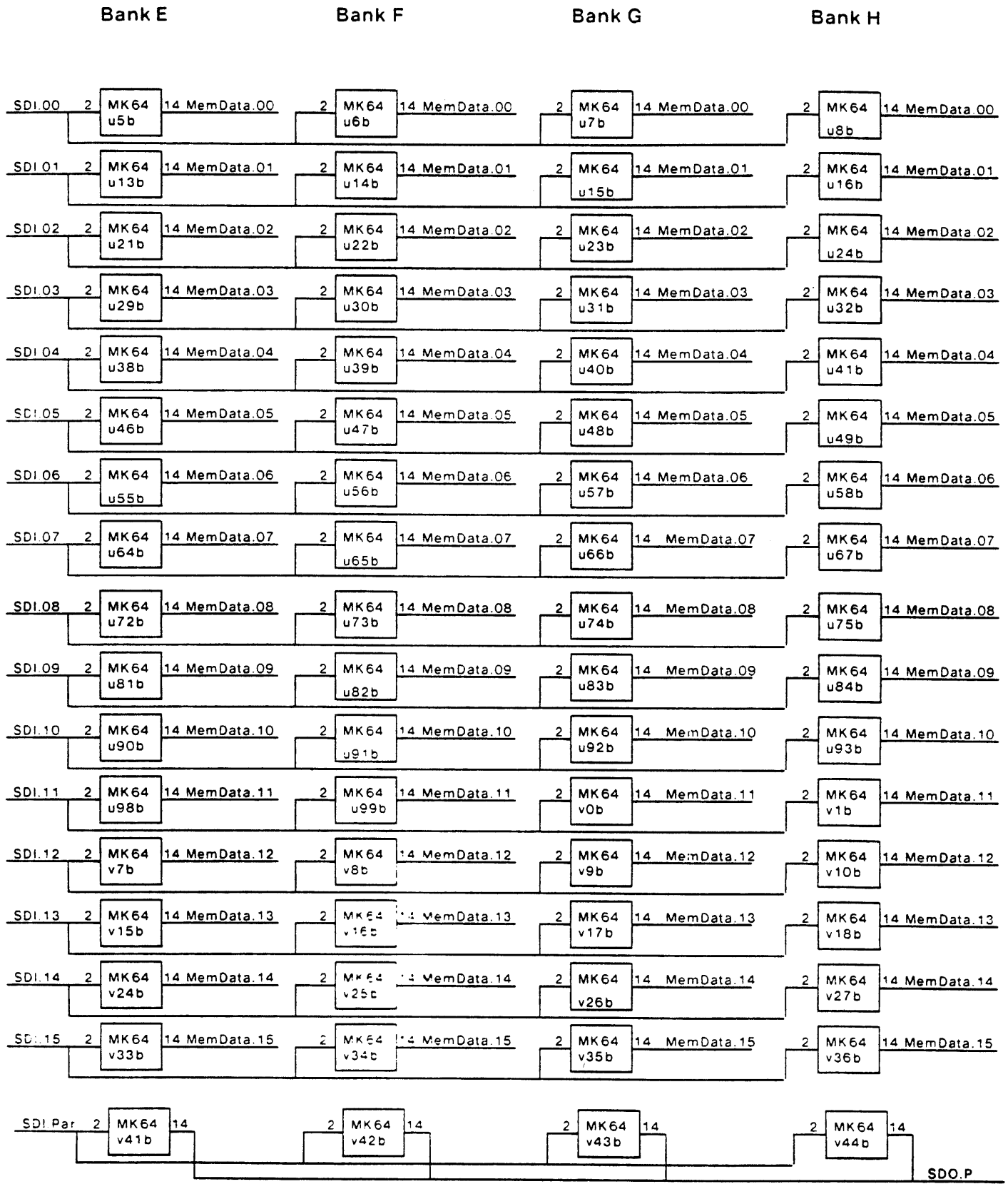
Mem. Data Reg., Mem. Ctl. Reg. & Parity Bit Generator

	Project MCCP	Mem. Data Reg., Mem. Ctl. Reg. & Parity Bit Generator	File PMCCP24.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 24
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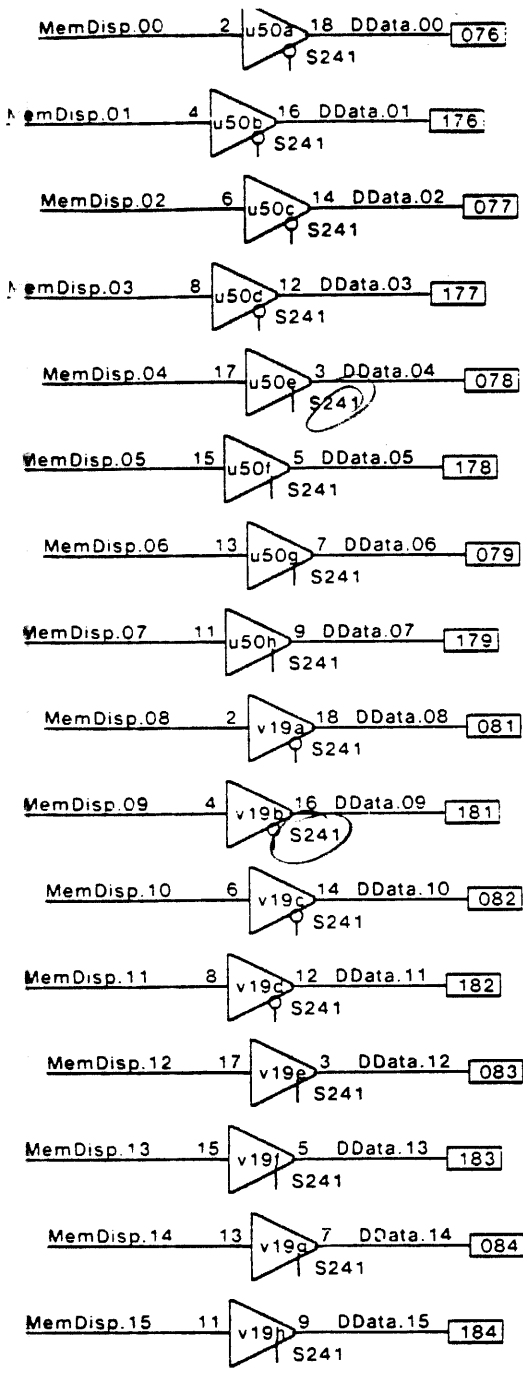


Work Station Memory

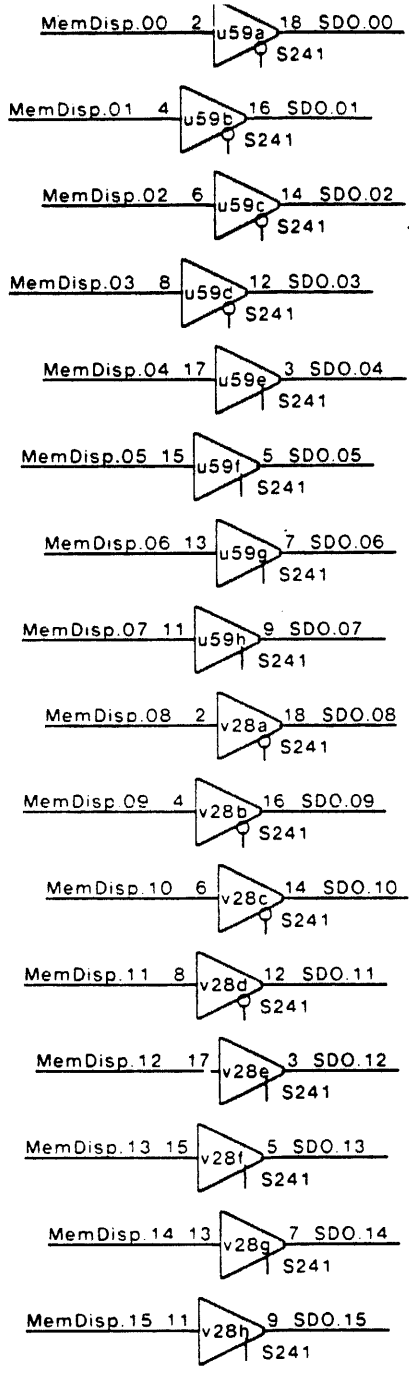
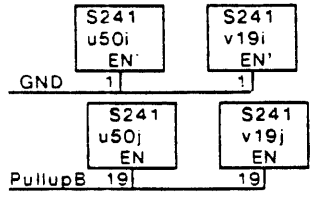
XEROX ED	Project MCCP	Work Station Memory	File PMCCP25.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 25
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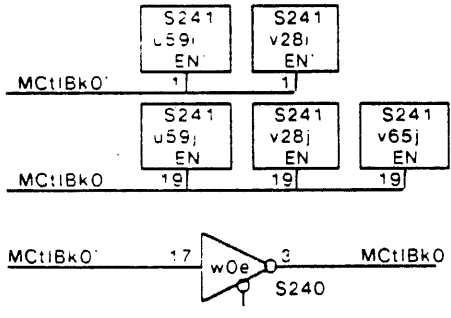
Work Station Memory



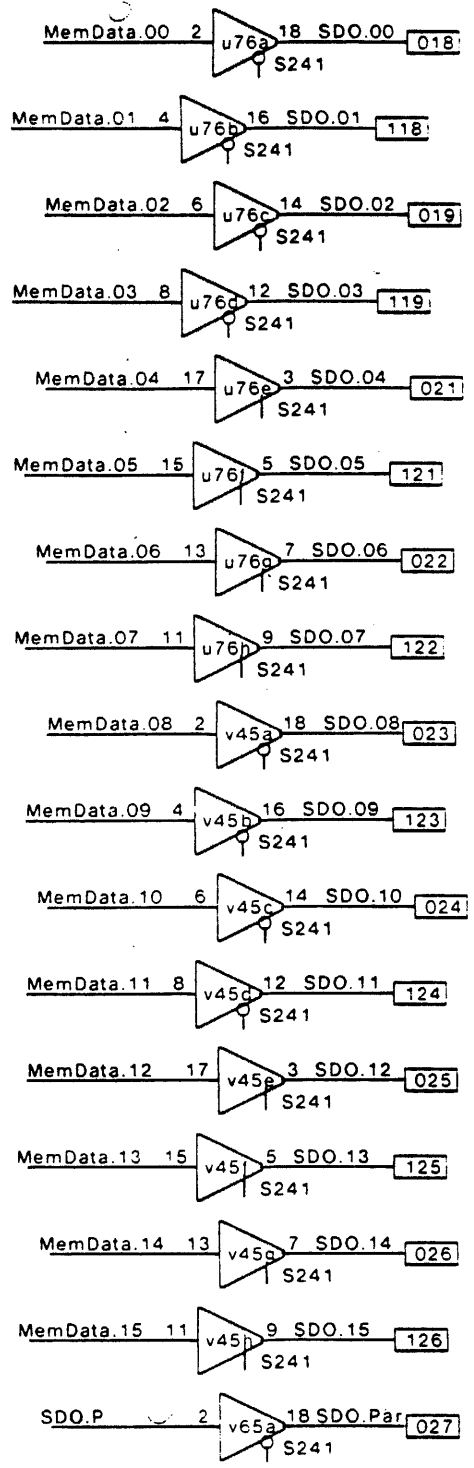
Display Data Buffers



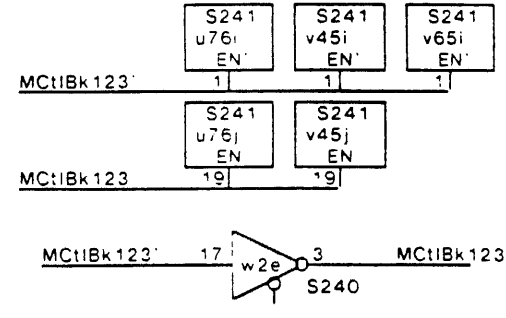
Main Data Buffers



Enable logic on Pg. 28

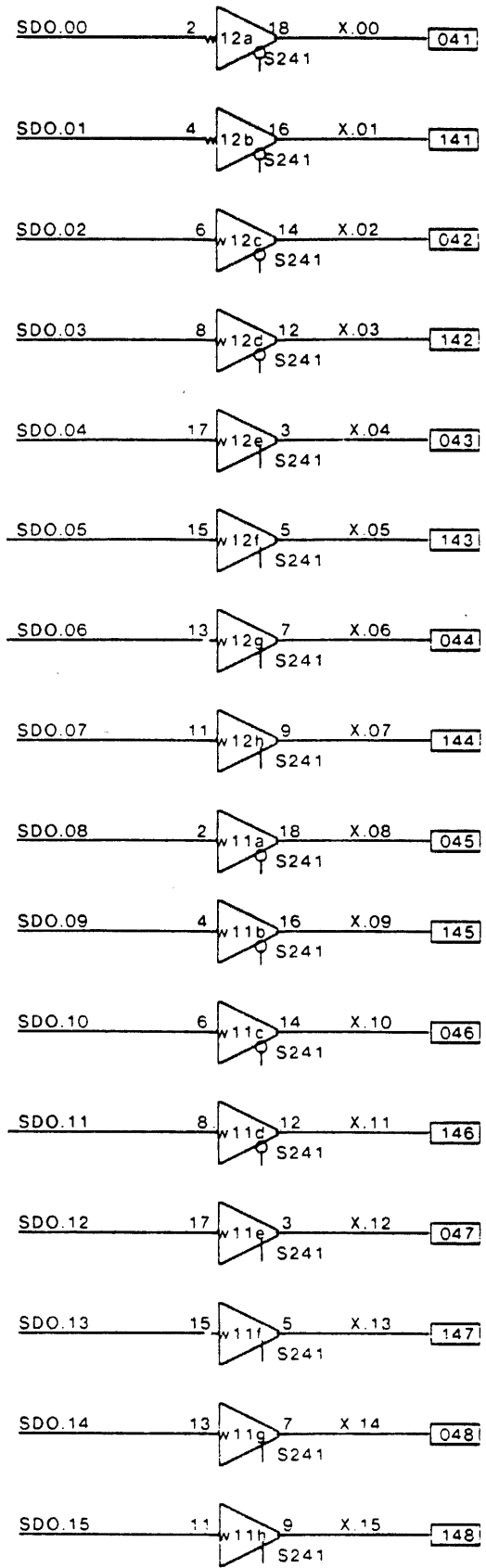
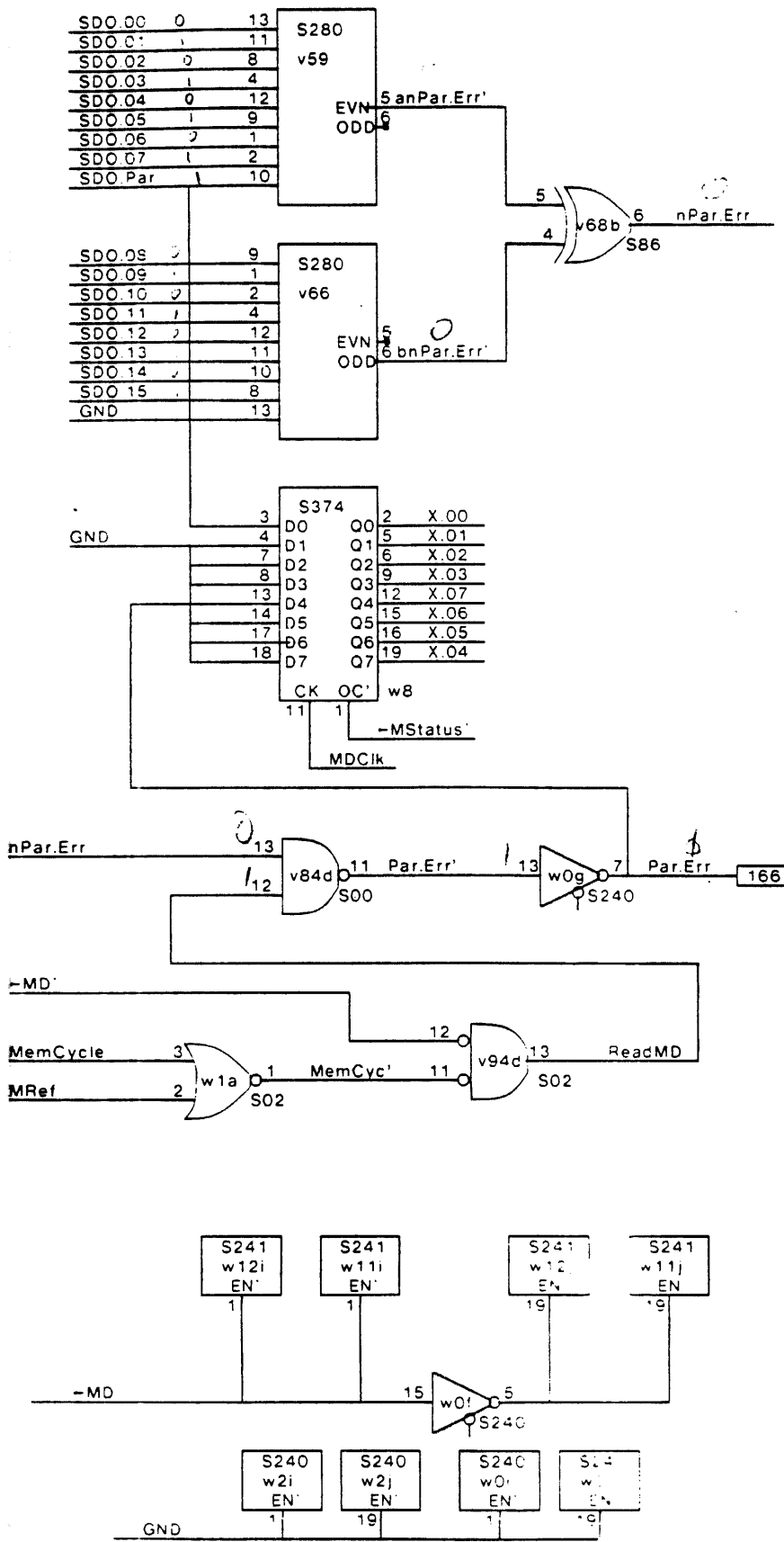


Main Data Buffers



Enable logic on Pg. 28

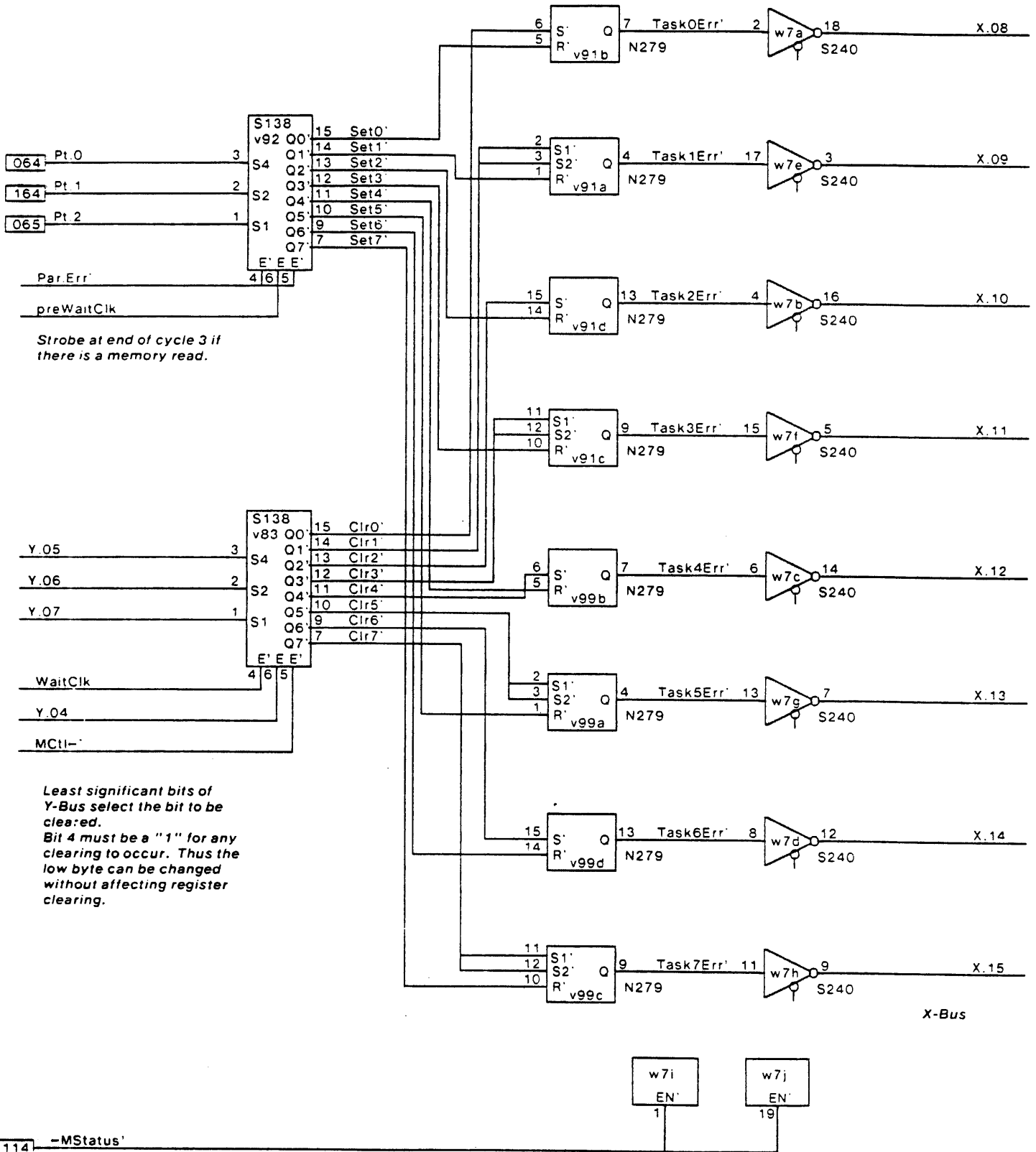
Data Buffers



Parity Error & Data Paths

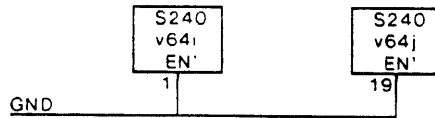
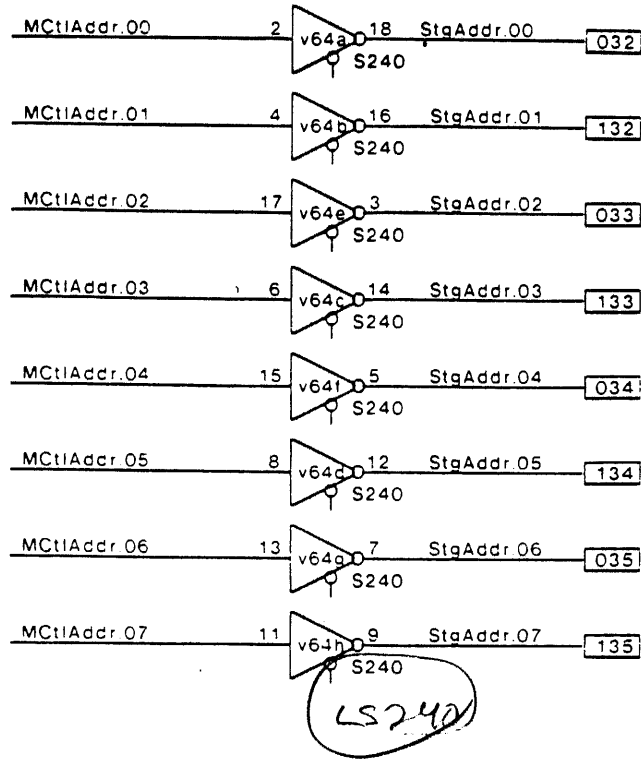
Errors Register

Bit is 1 if there was an error.



Error Log Register

XEROX ED	Project MCCP	Error Log Register	File PMCCP29.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 29
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MSC Address Selection

SDI.00z 2' #R97 1 SDI.00
1RT

SDI.01z 2' #R105 1 SDI.01
1RT

SDI.02z 2' #R106 1 SDI.02
1RT

SDI.03z 2' #R108 1 SDI.03
1RT

SDI.04z 2' #R98 1 SDI.04
1RT

SDI.05z 2' #R109 1 SDI.05
1RT

SDI.06z 2' #R99 1 SDI.06
1RT

SDI.07z 2' #R107 1 SDI.07
1RT

SDI.08z 2' #R112 1 SDI.08
1RT

SDI.09z 2' #R111 1 SDI.09
1RT

SDI.10z 2' #R110 1 SDI.10
1RT

SDI.11z 2' #R100 1 SDI.11
1RT

SDI.12z 2' #R101 1 SDI.12
1RT

SDI.13z 2' #R102 1 SDI.13
1RT

SDI.14z 2' #R103 1 SDI.14
1RT

SDI.15z 2' #R104 1 SDI.15
1RT

SDI.Parz 2' #R128 1 SDI.Par
1RT

VCC 2' #R132 1 PullupA
1RT

VCC 2' #R129 1 PullupB
1RT

VCC 2' #R12 1 RefreshA
1RT

RefreshBz 2' #R24 1 RefreshB
1RT

RefreshCz 2' #R36 1 RefreshC
1RT

RefreshDz 2' #R48 1 RefreshD
1RT

CASAz 2' #R11 1 CASA
1RT

WriteAz 2' #R10 1 WriteA
1RT

AAddr.00z 2' #R1 1 AAddr.00
1RT

RASAz 2' #R8 1 RASA
1RT

AAddr.03z 2' #R5 1 AAddr.03
1RT

AAddr.06z 2' #R2 1 AAddr.06
1RT

AAddr.02z 2' #R3 1 AAddr.02
1RT

AAddr.04z 2' #R7 1 AAddr.04
1RT

AAddr.01z 2' #R9 1 AAddr.01
1RT

AAddr.05z 2' #R4 1 AAddr.05
1RT

AAddr.07z 2' #R6 1 AAddr.07
1RT

CASBz 2' #R23 1 CASB
1RT

WriteBz 2' #R21 1 WriteB
1RT

BAddr.00z 2' #R13 1 BAddr.00
1RT

RASBz 2' #R20 1 RASB
1RT

BAddr.03z 2' #R17 1 BAddr.03
1RT

BAddr.06z 2' #R14 1 BAddr.06
1RT

BAddr.02z 2' #R15 1 BAddr.02
1RT

BAddr.04z 2' #R19 1 BAddr.04
1RT

BAddr.01z 2' #R22 1 BAddr.01
1RT

BAddr.05z 2' #R16 1 BAddr.05
1RT

BAddr.07z 2' #R18 1 BAddr.07
1RT

RefreshEz 2' #R60 1 RefreshE
1RT

RefreshFz 2' #R72 1 RefreshF
1RT

CASCz 2' #R35 1 CASC
1RT

WriteCz 2' #R33 1 WriteC
1RT

CAddr.00z 2' #R25 1 CAddr.00
1RT

RASCz 2' #R32 1 RASC
1RT

CAddr.03z 2' #R29 1 CAddr.03
1RT

CAddr.06z 2' #R26 1 CAddr.06
1RT

CAddr.02z 2' #R27 1 CAddr.02
1RT

CAddr.04z 2' #R31 1 CAddr.04
1RT

CAddr.01z 2' #R34 1 CAddr.01
1RT

CAddr.05z 2' #R28 1 CAddr.05
1RT

CAddr.07z 2' #R30 1 CAddr.07
1RT

CASDz 2' #R47 1 CASD
1RT

WriteDz 2' #R46 1 WriteD
1RT

DAddr.00z 2' #R37 1 DAddr.00
1RT

RASDz 2' #R43 1 RASD
1RT

DAddr.03z 2' #R41 1 DAddr.03
1RT

DAddr.06z 2' #R38 1 DAddr.06
1RT

DAddr.02z 2' #R39 1 DAddr.02
1RT

DAddr.04z 2' #R44 1 DAddr.04
1RT

DAddr.01z 2' #R45 1 DAddr.01
1RT

DAddr.05z 2' #R40 1 DAddr.05
1RT

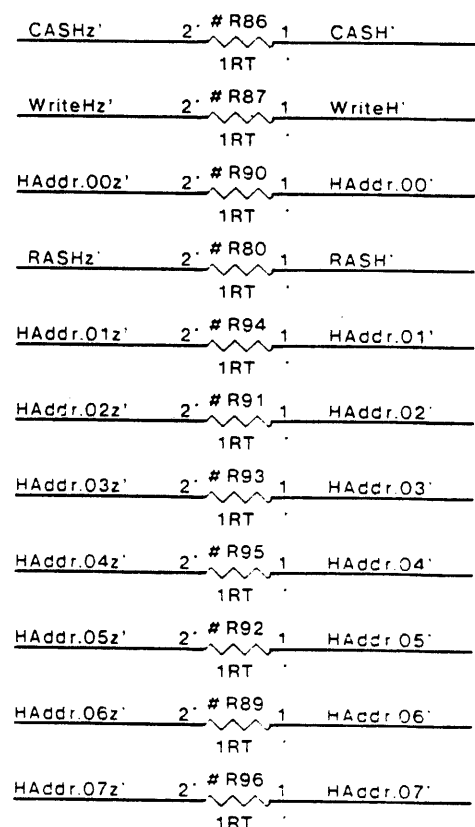
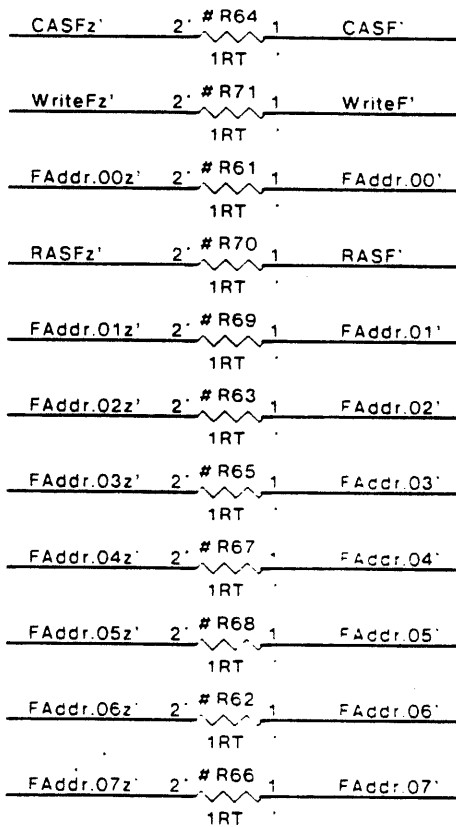
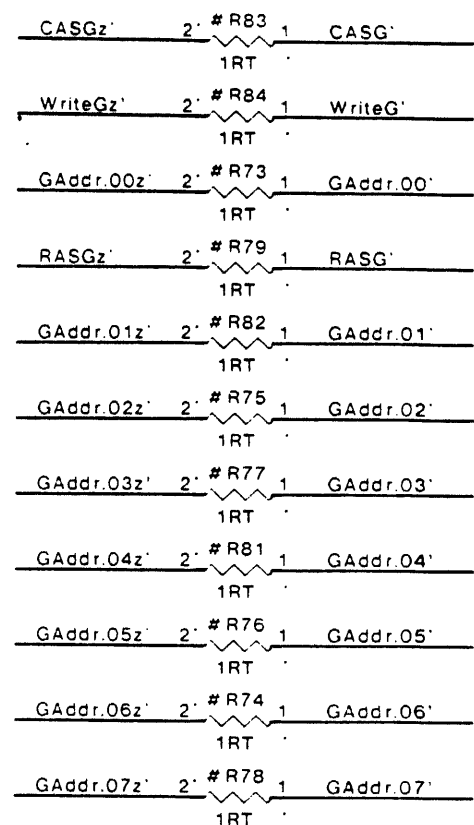
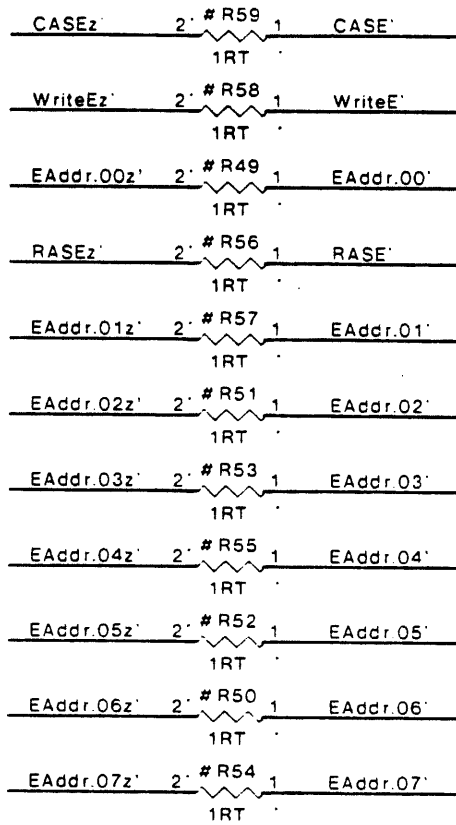
DAddr.07z 2' #R42 1 DAddr.07
1RT

RefreshGz 2' #R85 1 RefreshG
1RT

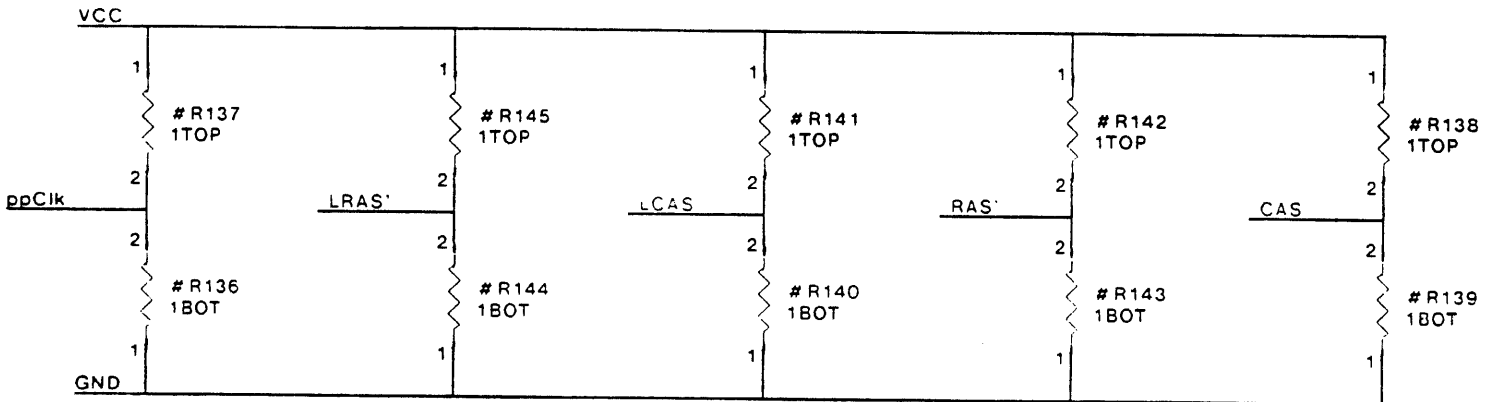
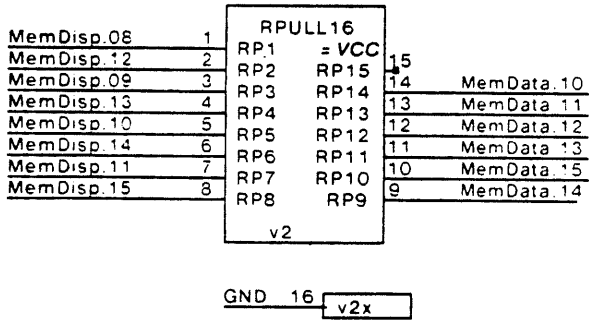
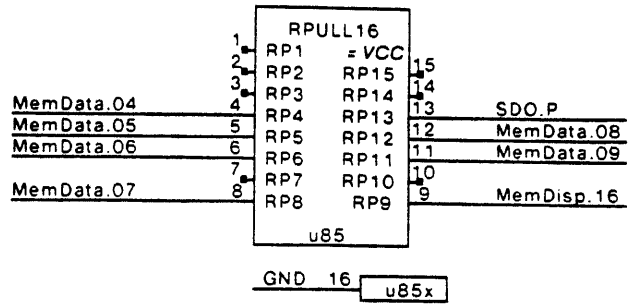
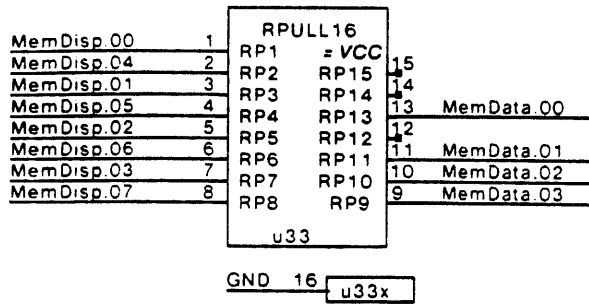
RefreshHz 2' #R88 1 RefreshH
1RT

Discrete Resistors

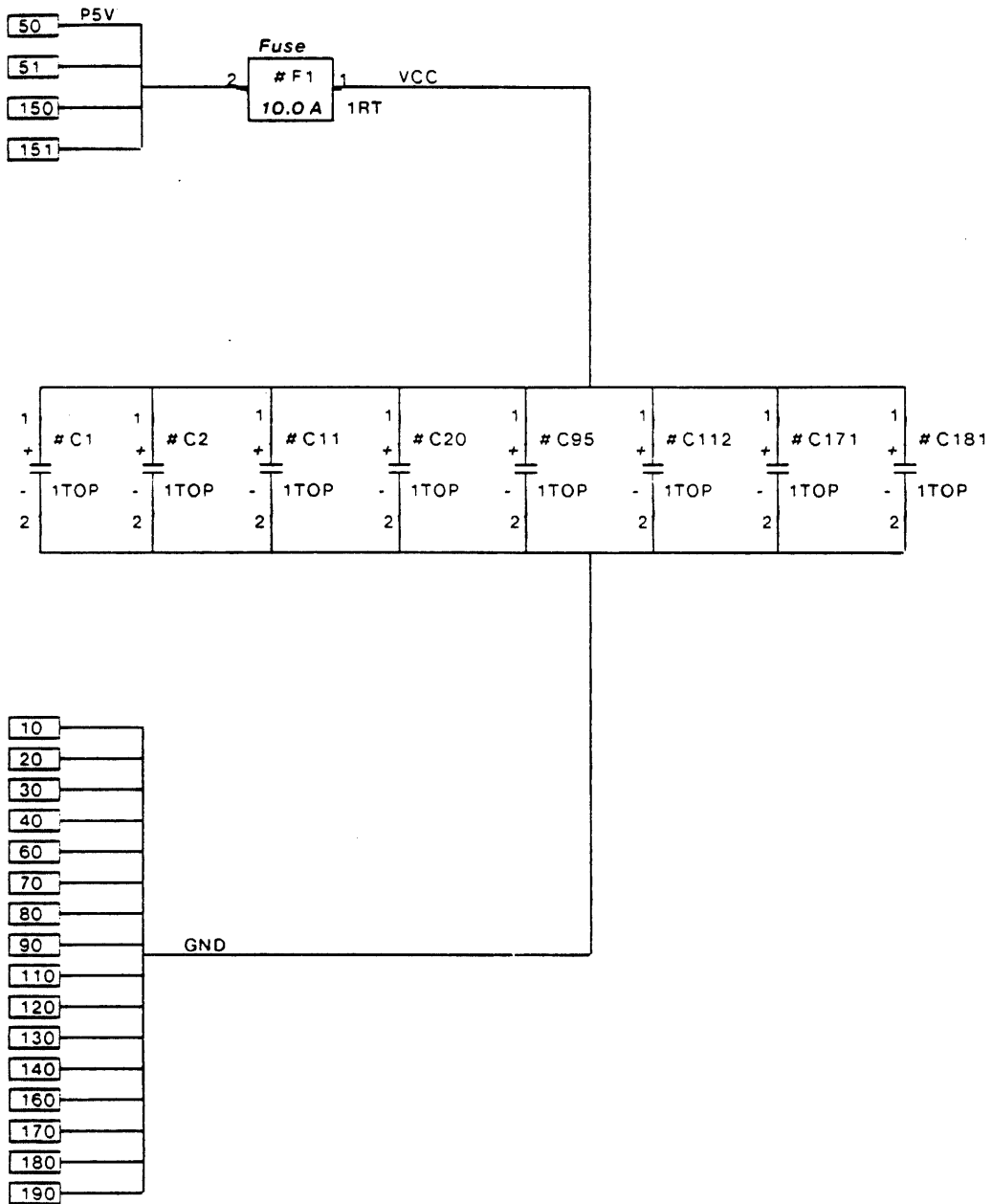
XEROX ED	Project MCCP	Discrete Resistors	File PMCCP31.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 31
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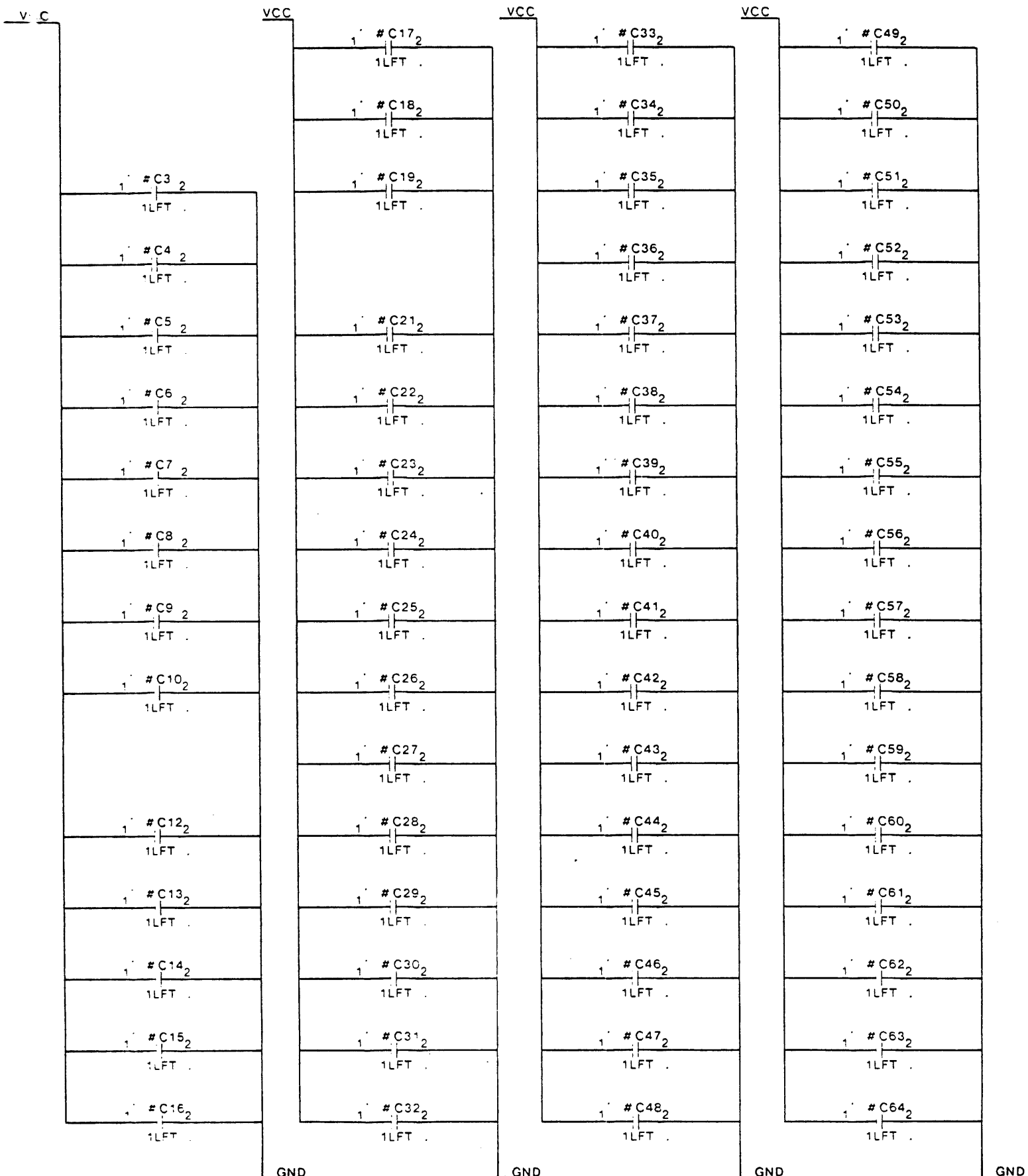
Discrete Resistors



Resistor DIPs, Termination

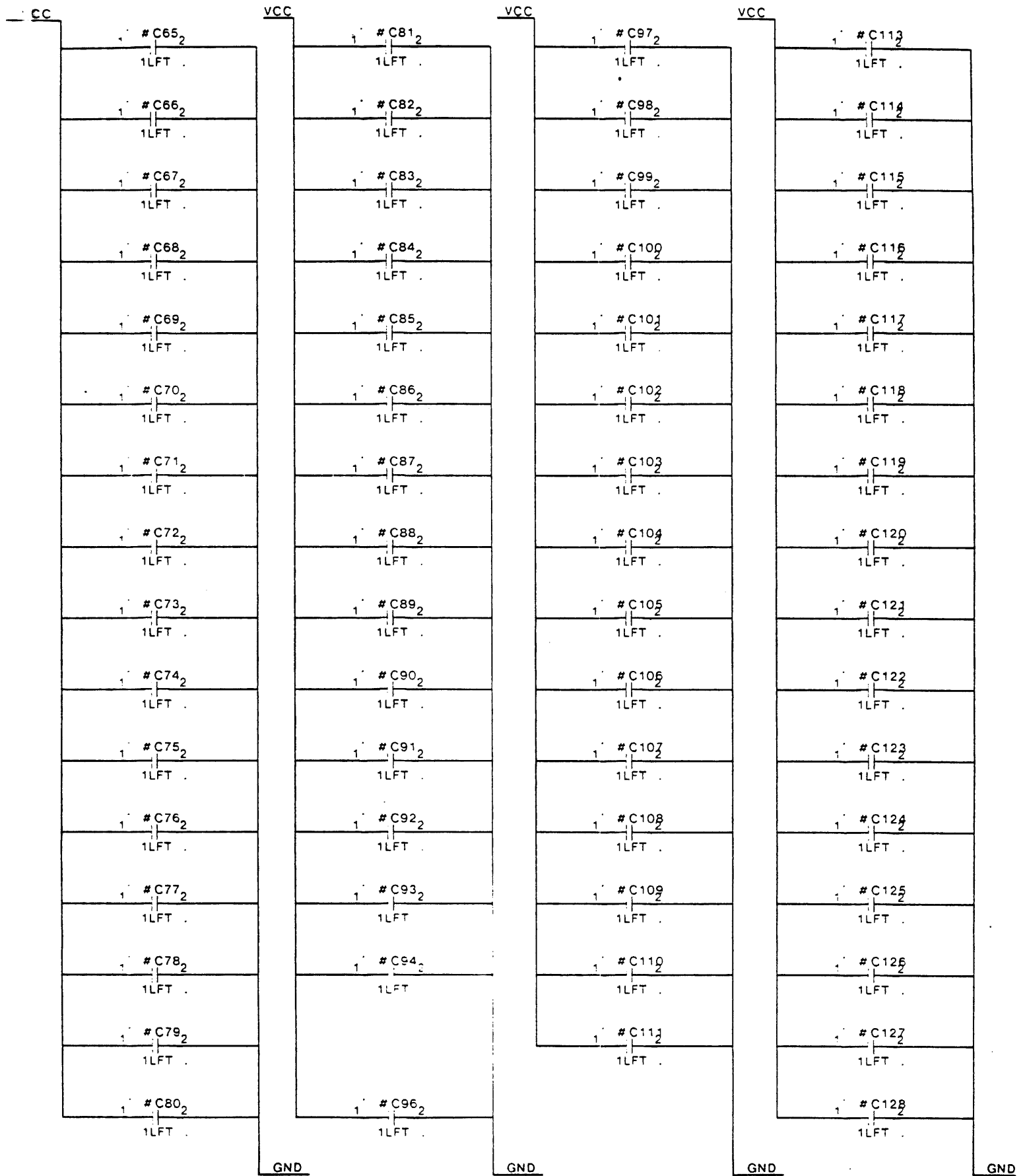


Power Pins - Fuses - Caps



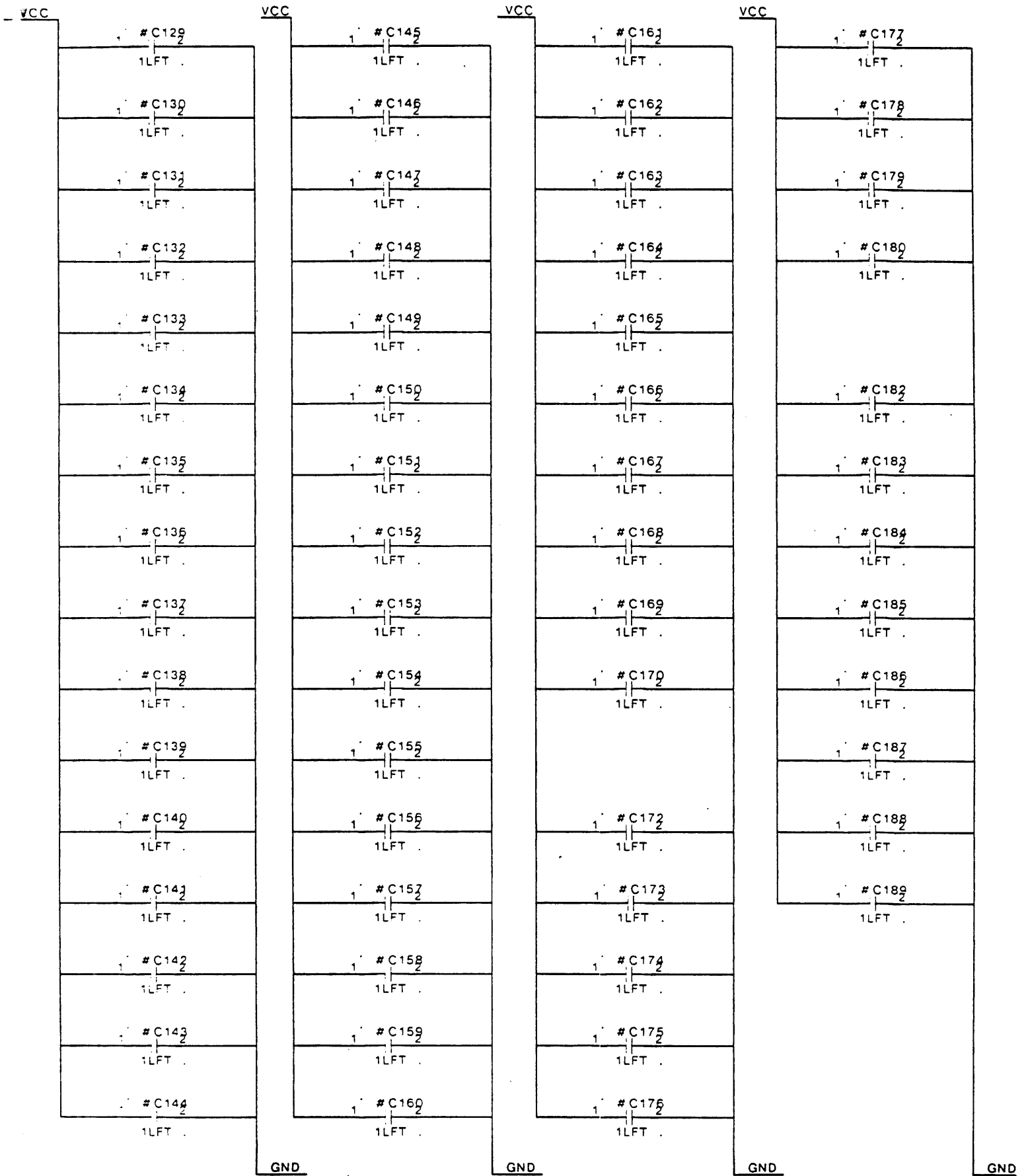
Discrete Capacitors page a

XEROX ED	Project MCCP	Discrete Capacitors	File PMCCP35.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 35
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Discrete Capacitors page b

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ED	MCCP	PMCCP36.sil	S. Ando	A	8/31/83	36



Discrete Capacitors page c

XEROX ED	Project MCCP	Discrete Capacitors	File PMCCP37.sil	Designer S. Ando	Rev A	Date 10/17/83	Page 37
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