9. Keyboard/Mouse Controller and MaintenancePanel TABLE OF CONTENTS

9. Keyboard/Mouse Controller and Maintenance Panel

The keyboard controller supports a low-profile keyboard/mouse interface and a maintenance panel interface. The keyboard interface is an 8251A UART-based controller, an asynchronous serial interface with a data rate of 9600 bps. The IOP communicates through this interface to the keyboard processor.

The keyboard itself contains the mouse controller. The information transferred over the keyboard link contains both keyboard and mouse data.

The maintenance panel displays diagnostic and status information.

9.1 Hardware

Figure 9.1 illustrates the 8251A keyboard controller. Table 9.1 lists the pins and signals and describes their function.

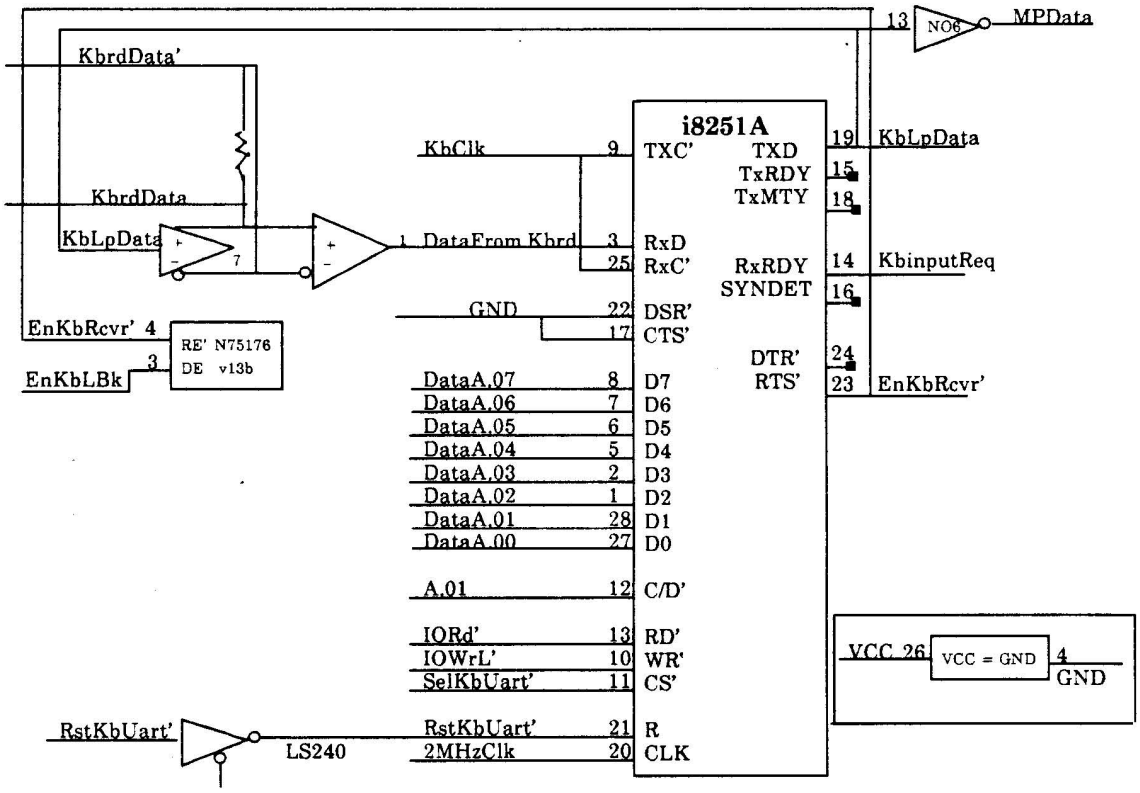

Figure 9.1. 8251A keyboard controller

Table 9.1. 8251A Pins and Signals

Symbol	Pin No.	Connection To	Name and Function
TXC'	9	KbClk	**Transmitter Clock:** The transmitter clock controls the rate at which characters are transmitted. This clock should be 16 times the data transfer rate.
RxD	3	DataFromKbrd	**Receive data:** Data line from the keyboard.
RxC'	25	KbClk	**Receive Clock:** Controls rate at which characters arrive at the 8251 RxD pin. This signal should be 16 times the data transfer rate.
D7	8	DataA.07	**Data 07-00:** Data bus connecting the 8251A to the 80186 for data and command exchange.
D6-4	7-5	Data.A06-04	
D3-2	2-1	Data.A03-02	
D1-0	28-27	Data.A01-00	
C/D'	12	A.01	**Command/Data Select:** Indicates type of access: 0 = data access; 1 = command access.
RD'	13	IORd'	**Read:** Control term indicating a read operation.
WR'	10	IOWrl'	**Write:** Control term indicating a write operation.
CS'	11	SelKbUart'	**Chip Select** or enable.
R	21	RStKbUart	**Reset:** 8251A reset line.
CLK	20	2MHzClk	**Clock:** Input for the 8251A's system clock.
TXD	19	KbLpData	**TxD:** Data line to the Maintenance Panel port.
RxRDY	14	KbinputReq	**INT:** The 8251A's interrupt line for initiating interrupts when a character is received.
RTS'	23	EnKbRcvr'	**RTS':** Control term used to enable the receiver on the keyboard data line.

Pins 15, 16, 18, and 24 are not used. Pins 17 and 22 are not used and are grounded.

9.2 Theory of Operations/Programming Interface

The following subsections explain how the keyboard and mouse controller and maintenance panel operate and describe the registers used for programming the devices.

9.2.1 Keyboard and Mouse Interface

The keyboard/mouse interface uses the receive half of the i8251A interface chip. Keyboard/mouse information is received from the keyboard as a differential signal pair by a 75176A receiver chip. The receiver chip translates the differential signals to a TTL signal and inputs the data to the i8251A via the RxD pin.

The transmit and receive clock is used by the 8251A to transmit and receive characters These clocks are generated by timer 2 of the IOP 8254 timer chip. Refer to Section 8 (RS232C).

9.2.2 Registers

The 8251A has one register with four registers within it, thus appearing as four I/O registers to the 80186. The registers and their addresses are listed in Table 9.2.

Table 9.2. 8257A Registers

Register	Direction	Address
Receive Data Reg	Read	30H
Transmit Data Reg	Write	30H
Status Reg	Read	32H
Command Reg	Write	32H

9.2.2.1. Command Register

After a reset occurs, the 8251A operating mode must be set in the command register. The chip also expects the command register to be used for operation commands.

Figure 9.2 illustrates the initialization process for the 8251A; Figure 9.3 illustrates the bit definitions for the command register during mode initialization. Figure 9.4 illustrates the bit definitions for the command register during normal operation.

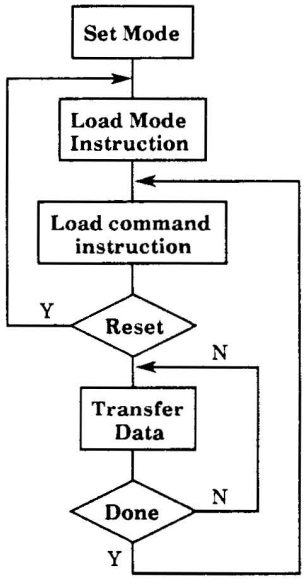

Figure 9.2. 8251A initialization
(From Microsystem Component Handbook, v2, Intel Corporation)

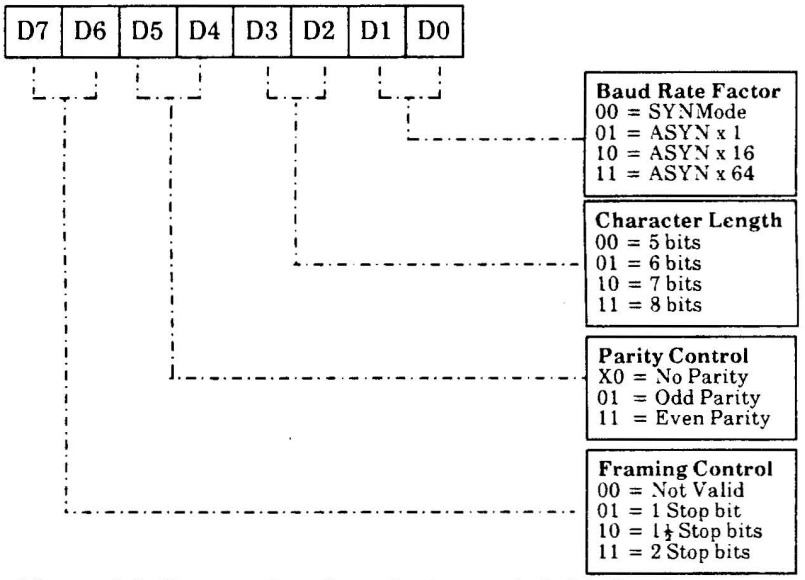

Figure 9.3 Command register during mode initialization
(From Microsystem Components Handbook, v.2, Intel Corporation)

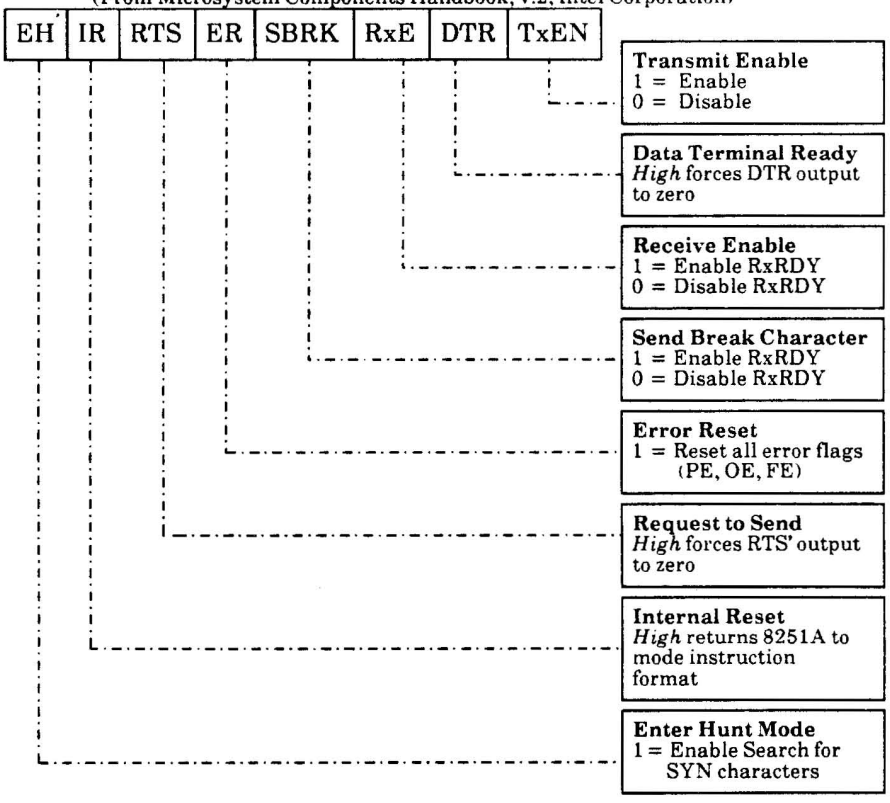

Figure 9.4. Command register during normal operation
(From Microsystem Components Handbook, v.2, Intel Corporation)

9.2.2.2.
Status Register

The 8251A generates an interrupt at level IR3 when a character is received. There is no interrupt generated to indicate that the transmit buffer is empty. Because of this, programs that send information to the maintenance panel must "poll" the status register for the TxE bit going active to indicate a transmit buffer empty condition.

The 8251A may be reset by driving bit 3 of the reset control register (C0H) to a logic 0.

A diagnostic loopback that enables the transmit half of the line driver chip (75176) to drive the receiver may be enabled by driving bit 14 of the reset control register to a logic 1. In this way, the receive logic can be fully tested.

Figure 9.5. illustrates the bit definitions for the status register. This register may be used to obtain the current status of the 8251A.

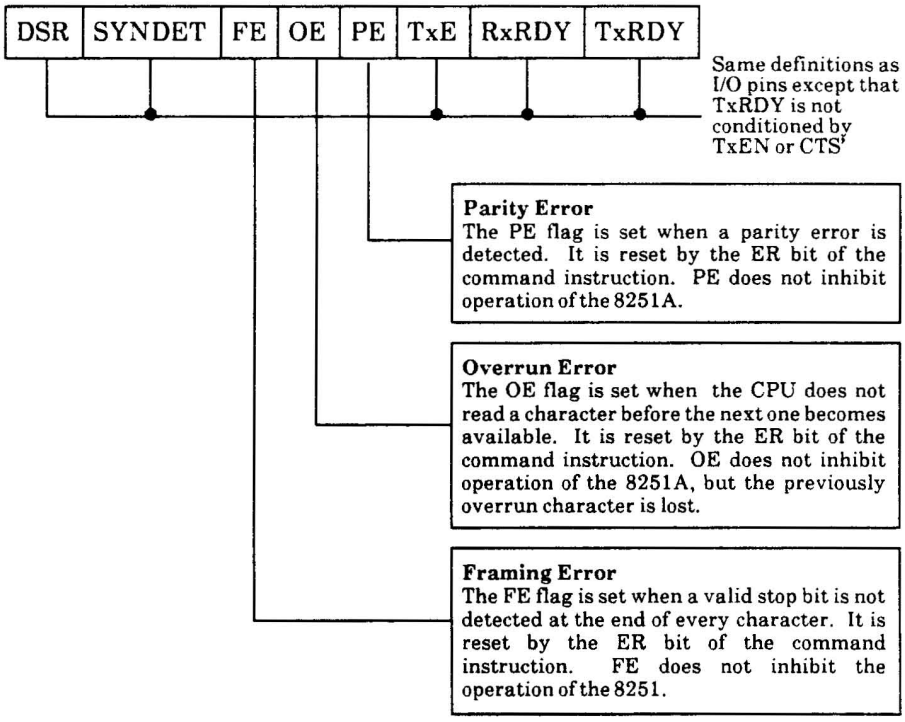

Figure 9.5 Status register
(From Microsystem Components Handbook, v. 2, Intel Corporation)

9.2.3 Maintenance Panel

The maintenance panel (MP) runs at 9600 baud, 1 start bit, 1 stop bit, and no parity bit. Since these variables are the same as the keyboard variables, no differences occur when the i8251A is initialized.

The MP is connected to the transmit data pin (unused by the keyboard) on the i8251A. The MP is also connected to the keyboard reset line, so resetting the keyboard resets the MP board as well.

The MP has an 80-character buffer, but can display only 16 contiguous ASCII characters at a time.

The MP displays twelve preset messages by sending a 1-byte code for the desired message and the hex data for the message arguments. Table 9.3 lists the messages and their respective arguments.

Table 9.3. Maintenance Panel Code Message

Code Message	
Normal Commands	**Special Commands**
00H "Ex Status XXXX"	FB Define Character
01H "Ob Status XXXX"	FC Clear Maintenance Panel display
02H "Ex Data XXXX"	FD Rotate all characters in buffer
03H "Ob Data XXXX"	FE Maintenance Panel Command Literal
04H "To XXXXXX"	FF Maintenance Panel Data Literal
05H "From XXXXXX"	
06H "Test Number XXXX"	
07H "Fault Code XXXX"	
08H "Loc XXXXXX"	
09H "IO Command XXXX"	
0AH "Data XXXX"	
0BH "Status XXXX"	
0CH "Parity Err XXXX"	

The following subsections describe the operations for normal commands and special commands.

9.2.3.1. Normal Commands

If, for example, the desired message is "Status 1234", then the following byte stream is sent by the IOP via the 8251A: 0B,12,34,1B. 0B is sent first to indicate which message is desired; then the arguments, 12 and 34, are sent. The message is terminated with a 1B.

The MP parses 0B and displays the appropriate message and the correct number of argument bytes. The MP stores all characters that are received in a buffer until an escape (esc) character (1BH) is received. The esc character is the signal to the MP to start parsing the message buffer.

Bit 7 modifies the meaning of all the standard messages (00-0C). If the bit is 0, then the maintenance panel clears the display. To clear a message from the display panel before the maintenance panel displays a new message, send 00HHHH1B (where H = any hex character). If the bit is 1, then the maintenance panel appends to the existing display buffer. To append the message to whatever is in the display, send 80HHHH1B. The display then places the new character on the right side of the display, and automatically scrolls the entire message to the left.

All data or argument bytes are sent in hex or binary format. The panel converts the data to ASCII just before it is placed in the display buffer.

9.2.3.2. Special Commands

Command FB defines the bitmap for custom characters. The maintenance panel can display up to four custom characters. All characters are displayed in a 5 x 11 matrix with the cursor being logically ORed with the bottom or 11th line.

To define a character, send the FB command byte followed by the character ID byte (00-03). This command is followed by 11 bytes that define the character's bitmap. Because the bitmap is only 5 bits wide, only the least significant 5 bits are used for the bitmap. The byte string is terminated with a 1BH.

Command FC causes the maintenance panel to clear its display. This command has no parameters.

Command FD causes the display buffer to be rotated or scrolled through the LCD display. This command has no parameters.

Command FE allows the programmer to send commands directly to the display controller. This command always appears as FEXX1B, where XX is the display controller command. Table 9.4 lists the instructions for this command.

Table 9.4 Command Instruction Set

Instruction	Code							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear Display	0	0	0	0	0	0	0	1
Cursor At Home	0	0	0	0	0	0	1	*
Entry Mode Set	0	0	0	0	0	1	I/D	S
Display On/Off Control	0	0	0	0	1	D	C	B
Cursor/Display Shift	0	0	0	1	S/C	R/L	*	*
Function Set	0	0	1	DL	N	F	*	*

Command FF allows the programmer to create his own messages by following the FF with any string of ASCII characters; the message must be completed with an esc (1BH) character. For example, to display the message "A B C", the byte stream FF,41,20,62,20,43,1B must be sent.

All command messages must end in an esc 1BH character to initiate the parsing of a message. Multiple messages may be sent together; for example, 00XXXX81XXXX1B forms the message "Ex Status XXXX Ob Status XXXX" in the buffer. Because the display is only 16 characters long, only the first 16 characters are displayed. To display the rest of the message, the programmer can send an FD command to cause the display buffer to be rotated through the the LCD display.