# 4. Memory

# 4. Memory

The display memory, the system memory, and the expansion memory (option) are included in the memory subsystem.

Memory for Daybreak is packaged in 512 Kbyte blocks. Each of the three memory segments requires a memory controller. Each memory controller includes a refresh controller.

The system and expansion memory has three ports: one for the Mesa processor, one for the I/O subsystem, and one for the Refresh controller. These three devices operate independently except when competing for the same memory segment. Display memory has an additional display controller port. The refresh controller is responsible for refreshing the DRAM chips in its block of real memory.

Each port of the memory subsystem employs a protocol suited to the corresponding device. Each device initiates a memory request whenever necessary. The request results in a memory cycle when the currently active and higher-priority requests have been satisfied.

The memory controller chip receives memory request signals from outside ports (ports A, B, and C), sets priorities, and generates proper control signals to perform memory operations. It also has circuitry to initiate refresh of the dynamic RAMs so that data is maintained.

The memory controller runs four types of cycles:

- display. Display cycles are quadword read. DRAM nibble mode operation allows the display controller to use all the available memory bandwidth.
- IOP bus. Memory cycles are: read word, write word, write high byte, and write low byte.
- Mesa Processor. Memory cycles are: read word and write word.
- Refresh.

## 4.1 Hardware

Memory on the Display Control and Memory (DCM) is 3 x 256 KW, and memory on the Memory Expansion Board (MEB) is 5 x 256 KW. Both are multi-ported memory banks with an internal refresh port. Normal word access cycle time is 312.5 ns/16-bit word; read access cycle time is 718 ns/64-bit nibble.

Figure 4.1 illustrates the memory units .

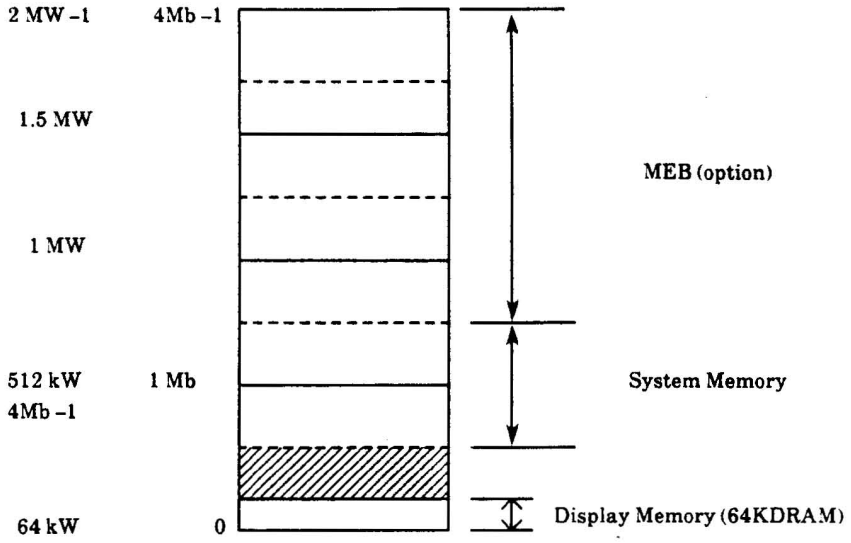


**Figure 4.1.** Memory units

### 4.1.1 Memory on DCM Board

The DCM board contains both display memory and system memory.

The display memory is the first 64 KW of 256 KW real memory contained on the DCM board. Display memory can be 64 KW or 256 kW. It is a 3-ported memory bank with an internal refresh port, controlled by a gate array chip, the Memory Control Chip (MCC).

Figure 4.2 illustrates the pins and signals of the Memory Control Chip (MCC) gate array. Note: Italicized signals are not required for Display memory operation.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DOPE0 | | 1 | P1P68 | P68 | 68 | | PEINT' | |
| ERRCLK" | | 2 | P2 | P67 | 67 | | | |
| DOPE1 | | 3 | P3 | P66 | 66 | | | |
| A/BHEB' | | 4 | P4 | P65 | 65 | | | |
| A/A.00B' | | 5 | P5 | P64 | 64 | | WTHB | |
| A/RESETB1' | | 6 | P6 | P63 | 63 | | WTLB | |
| RFREQDIS' | | 7 | P7 | P62 | 62 | | WRITE | |
| | GND | 8 | P8 | P61 | 61 | VCC | | |
| | VCC | 9 | P9 | P60 | 60 | GND | | |
| | GND | 10 | P10 | P59 | 59 | | DOCLK | |
| *C/A.20* | GND | 11 | P11 | P58 | 58 | | | |
| *B/A.20* | | 12 | P12 | P57 | 57 | | PCEN' | |
| *A/MA.20* | | 13 | P13 | P56 | 56 | | PBEN' | |
| *C/A.191* | | 14 | P14 | P55 | 55 | | PAEN' | |
| *B/A.19* | | 15 | P15 | P54 | 54 | | B/ALEB | |
| *A/MA.19* | | 16 | P16 | P53 | 53 | | B/MEMREFL' | |
| A.20 | | 17 | P17 | P52 | 52 | | REFS2 | REFS2* |
| A.19 | | 18 | P18 | P51 | 51 | GND | *A/PROC'* | REFS2* |
| RAS0T | | 19 | P19 | P50 | 50 | | PBAH' | |
| *RAS1T* | | 20 | P20 | P49 | 49 | | C/MEMREF' | |
| *RAS2T* | | 21 | P21 | P48 | 48 | | A/MEMREF' | |
| *RAS3T* | | 22 | P22 | P47 | 47 | | PAAH' | |
| *CAS1T* | | 23 | P23 | P46 | 46 | | A/MRDBL' | |
| CAS0T | | 24 | P24 | P45 | 45 | | A/MWTBL' | |
| | VCC | 25 | P25 | P44 | 44 | | GND | |
| | GND | 26 | P26 | P43 | 43 | VCC | | |
| | GND | 27 | P27 | P42 | 42 | | RAWCLKB | |
| COLT' | | 28 | P28 | P41 | 41 | GND | *C/NIBBLE'* | |
| ROWT' | | 29 | P29 | P40 | 40 | GND | *C/MRD'* | |
| C/XACK' | | 30 | P30 | P39 | 39 | | HIGH1 *C/MWT'* | |
| B/READYL | | 31 | P31 | P38 | 38 | | B/MRD' | |
| A/READYL | | 32 | P32 | P37 | 37 | | B/MWT' | |
| PCRDEN' | | 33 | P33 | P36 | 36 | | A/ALEB | |
| PBRDEN' | | 34 | P34 | P35 | 35 | | PARDEN' | |

*Refresh Control Signal REFS2 is inserted at MCC pins 51 (A/PROC') and 52 (C/MEMREF") to delay IOP and/or display requests going to the Arbiter during a refresh operation.

**Figure 4.2.** DCM memory controller chip

Table 4.1 describes the signals illustrated in Figure 4.2.

**Table 4.1.** Memory Control Chip (Display) Signal Description

| Signal | Function |
|---|---|
| A/A.00B'<br>A/BHEB' | With A/BHEB' identifies port A memory operation, as follows:<br><br>A/A.00B' / A/BHEB' / Memory Operation<br>0 / 0 / Word<br>0 / 1 / High byte only<br>1 / 0 / Low byte only<br>1 / 1 / Not 1 |
| A.19:20 | With A.21 selects memory location, as follows:<br><br>(A;B/A;C/A) A.21 / (A;B/A;C/A) 20 / 19 / Memory Selected / Remark<br>0 / 0 / 0 / 0 - 255 KW / Display memory<br>0 / 0 / 1 / 256 - 511 KW / Bank 1, system memory<br>0 / 1 / 0 / 512 - 767 KW / Bank 2, system memory<br>0 / 1 / 1 / 768 - 1023 KW / Bank 1, MEB memory<br>1 / 0 / 0 / 1024 - 1279 KW / Bank 2, MEB memory<br>1 / 0 / 1 / 1080 - 1535 KW / Bank 3, MEB memory<br>1 / 1 / 0 / 1536 - 1791 KW / Bank 4, MEB memory<br>1 / 1 / 1 / 1792 - 2047 KW / Bank 5, MEB memory |
| A/ALEB<br>B/ALEB | Address latch enable signal for port A and port B |
| A/MA.19:20<br>B/A.19:20<br>C/A.19:20 | Generate A.19-20, as described above. The prefix identifies the corresponding port. |
| A/MEMREF'<br>B/MEMREFB'<br>C/MEMREF' | Indicate that a memory operation is being requested. The prefix identifies the corresponding port. |
| A/MRDBL'<br>B/MRD'<br>C/MRD' | Memory read operation. The prefix identifies the corresponding port. |
| A/MWTBL'<br>B/MWT'<br>C/MWT' | Memory write operation. The prefix identifies the corresponding port. |
| A/PROC' | Not used. |
| A/READYL<br>B/READYL | Indicates port readiness. |
| A/RESETB1' | General reset. |
| CAS0T<br>CAS1T | CAS (column address strobe) enable for RAM. CAS1T is not used. |
| C/NIBBLE' | Indicates port C nibble mode operation. |
| COLT' | Not used. |
| C/XACK' | Transfer acknowledge for port C. |
| DOCLK | Data Out clock. |

- more -

Table 4.1. Memory Control Chip (Display) Signal Description (continued)

| Signal | Function |
|---|---|
| DOPE0-1 | Data Out parity error for low and high byte. |
| HIGH1 | Input high. |
| LOCK | Not used. |
| PAAH'<br>PBAH' | Indicates valid memory address by the corresponding port. |
| PAEN'<br>PBEN'<br>PCEN' | Identifies the port now being serviced by memory. |
| PARDEN'<br>PBRDEN'<br>PCRDEN' | Enables read operation for corresponding port. |
| PEINT' | Indicates that a parity error was encountered during memory read operation. |
| RAS0T-3T | RAS (row address strobe) enable for RAM. |
| RAWCLKB | System clock. |
| RFREQDIS' | Disables refresh circuit for dynamic RAM. |
| ROWT' | Not used. |
| WRITE | Not used. |
| WTHB<br>WTLB | Enables memory write operation to high and/or low byte. |

### 4.1.2 Memory on MEB

The Memory Expansion Board is a 10.9 inch by 16 inch 165-pin board populated with 256K DRAMs. Figure 4.3 illustrates the board layout.

**Figure 4.3.** Memory Expansion Board (MEB) layout

#### 4.1.2.1 Memory Controller Chip

A 68-pin gate array, MCC, acts as memory controller on the MEB. Figure 4.4 illustrates pins and signals for the MEB memory controller chip (MCC). Refer to the preceding table for description of signals.

| | | | | | | |
|---|---|---|---|---|---|---|
| DOPE0 | | 1 | P1 | P68 | 68 | PEINT'.S |
| ERRCLK' | | 2 | P2 | P67 | 67 | |
| DOPE1 | | 3 | P3 | P66 | 66 | |
| A/BHEB' | | 4 | P4 | P65 | 65 | |
| A/A.00B' | | 5 | P5 | P64 | 64 | WTHB.S |
| A/RESETB2' | | 6 | P6 | P63 | 63 | WTLB.S |
| RFREQDIS' | | 7 | P7 | P62 | 62 | |
| | GND | 8 | P8 | P61 | 61 | VCC |
| | VCC | 9 | P9 | P60 | 60 | GND |
| | GND | 10 | P10 | P59 | 59 | DOCLK |
| | GND | 11 | P11 | P58 | 58 | |
| | GND | 12 | P12 | P57 | 57 | |
| | GND | 13 | P13 | P56 | 56 | PBEN' |
| | GND | 14 | P14 | P55 | 55 | PAEN' |
| | GND | 15 | P15 | P54 | 54 | B/ALEB |
| | GND | 16 | P16 | P53 | 53 | B/MEMREFL' |
| | | 17 | P17 | P52 | 52 | REFS2 |
| | | 18 | P18 | P51 | 51 | REFS2 |
| RASOT' | | 19 | P19 | P50 | 50 | PBAH' |
| | | 20 | P20 | P49 | 49 | HIGH3 |
| | | 21 | P21 | P48 | 48 | A/MEMREF' |
| | | 22 | P22 | P47 | 47 | PAAH' |
| | | 23 | P23 | P46 | 46 | A/MRDB' |
| CASOT | | 24 | P24 | P45 | 45 | A/MWTB' |
| | VCC | 25 | P25 | P44 | 44 | GND |
| | GND | 26 | P26 | P43 | 43 | VCC |
| | GND | 27 | P27 | P42 | 42 | RAWCLKB |
| | | 28 | P28 | P41 | 41 | HIGH3 |
| | | 29 | P29 | P40 | 40 | HIGH3 |
| | | 30 | P30 | P39 | 39 | HIGH3 |
| B/READYL | | 31 | P31 | P38 | 38 | B/MRD' |
| | | 32 | P32 | P37 | 37 | B/MWT' |
| | | 33 | P33 | P36 | 36 | A/ALEB |
| PBRDEN' | | 34 | P34 | P35 | 35 | PARDEN' |

**Figure 4.4.** MEB memory controller chip

### 4.1.2.2 Backplane Interface

Table 4.2 lists the MEB interface to the backplane.

**Table 4.2.** MEB Backplane Pin Assignment (Front View)

Outmost — Inmost

### 1) 80186 Bus

| | | |
|---|---|---|
| Spare-1 J1.001 | GND J1.002 | Spare-2 J1.003 |
| A/AD.07 (bi) J1.004 | A/DT/R' (i) J1.005 | A/AD.15 (bi) J1.006 |
| A/AD.06 (bi) J1.007 | A/DEN' (i) J1.008 | A/AD.14 (bi) J1.009 |
| A/AD.05 (bi) J1.010 | GND J1.011 | A/AD.13 (bi) J1.012 |
| A/AD.04 (bi) J1.013 | A/MemRdy (o) J1.014 | A/AD.12 (bi) J1.015 |
| A/AD.03 (bi) J1.016 | A/ALE' J1.017 | A/AD.11 (bi) J1.018 |
| A/AD.02 (bi) J1.019 | A/IOPMemWr' (i) J1.020 | A/AD.10 (bi) J1.021 |
| A/AD.01 (bi) J1.022 | Spare-3 J1.023 | A/AD.09 (bi) J1.024 |
| A/AD.00 (bi) J1.025 | GND J1.026 | A/AD.08 (bi) J1.027 |
| GND J1.028 | A/CLK (i) J1.029 | VCC J1.030 |

| | | |
|---|---|---|
| J1.031 GND | J1.032 GND | J1.033 GND |
| J1.034 A/AA.19* | J1.035 (i) A/S.2' | J1.036 A/AA.23* |
| J1.037 A/AA.18* | J1.038 (i) A/S.1' | J1.039 A/AA.22* |
| J1.040 A/AA.17* | J1.031 (i) A.S.0' | J1.042 A/AA.21* |
| J1.043 A/AA.16* | J1.044 (i) A/BHE' | J1.045 A/AA.20* |
| J1.046 A/EPROMCs'* | J1.047 GND | J1.048 (i) A/IOR' |
| J1.049 Reserved-0 | J1.050 A/LocRamCS'* | J1.051 Spare-4 |
| J1.052 A/IOPLock'* | J1.053 GND | J1.054 (i) A/IOW' |
| J1.055 A/PCHldToArb | J1.056 (i) A/IOPMemRd' | J1.057 (i) Spare-5 |
| J1.058 -5V | J1.059 -5V | J1.060 -5V |

### 2) MPB-DCM

| | | |
|---|---|---|
| GND J1.061 | GND J1.062 | GND J1.063 |
| A/IORdy* J1.064 | A/MA.23 (i) J1.065 | A/MA.22 (i) J1.066 |
| Spare-7 J1.067 | A/MA.21 (i) J1.068 | A/MA.20 (i) J1.069 |
| SpareID'* J1.070 | A/MA.19 (i) J1.071 | A/MA.18 (i) J1.072 |
| DBRK/DAISY'* J1.073 | A/MA.17 (i) J1.074 | A/AA.16B (i) J1.075 |
| A/PEINT' (o) J1.076 | GND J1.077 | MPB-DCM-spare1 J1.078 |
| A/MEBIntr'* J1.079 | MPB-DCM-spare2 J1.080 | |
| A/VRETINT* J1.082 | | |
| GND J1.085 | GND J1.083 | |
| A/RawCLK (i) J1.088 | MPB-DCM-spare3 J1.086 | |
| | GND J1.089 | |

### 3) Mesa Bus

| | |
|---|---|
| B/MWT' (i) | J1.081 |
| Dawn-Mp-spare1 | J1.084 |
| B/MRD' (i) | J1.087 |
| VCC | J1.090 |

* Not used

- more -

**Table 4.2.** MEB Backplane Pin Assignment (continued)

Outmost

**4) IOP–Mesa**

| | | | | | |
|---|---|---|---|---|---|
| J1.091 | GND | J1.092 | GND | J1.093 | GND |
| J1.094 | A/IOPIntMP'* | J1.095 | CSWREN* | J1.096 (o) | A/MEMS' |
| J1.097 | A/MPIntIOP* | J1.098 | CSLOAD/SHIFT'* | J1.099 (i) | B/Lock' |
| J1.100 | A/IOPRdNIA* | J1.101 | CSBUFFEREN* | J1.102 | B/IOR'* |
| J1.103 | A/Halt'* | J1.104 | CSDATAIN* | J1.105 (i) | B/MemRef' |
| J1.106 | IOP-S-spare1 | J1.107 | CSSHIFTCLK* | J1.108 | B/IOW'* |
| J1.109 | A/ResetMPB'* | J1.110 | CSDATOUT* | J1.111 (o) | B/Rdy |
| J1.112 | VCC | J1.113 | VCC | J1.114 | VCC |
| J1.115 | VCC | J1.116 | VCC | J1.117 (i) | VCC |
| J1.118 | VCC | J1.119 | VCC | J1.120 | VCC |

Inmost

**3) MesaBus (continued)**

| | | | | | |
|---|---|---|---|---|---|
| GND | J1.121 | GND | J1.122 | GND | J1.123 |
| GND | J1.124 | GND | J1.125 | GND | J1.126 |
| GND | J1.127 | GND | J1.128 | GND | J1.129 |
| INTDIS' | J1.130 | B/A.18 (i) | J1.131 | B/ALE' (o) | J1.132 |
| B/A.23 (i) | J1.133 | B/A.17 (i) | J1.134 | Dawn-Mp-spare3 | J1.135 |
| B/A.22 (i) | J1.136 | GND | J1.137 | B/D.11 (bi) | J1.138 |
| B/A.21 (i) | J1.139 | B/D.15 (bi) | J1.140 | B/D.10 (bi) | J1.141 |
| B/A.20 (i) | J1.142 | B/D.14 (bi) | J1.143 | B/D.09 (bi) | J1.144 |
| B/A.19 (i) | J1.145 | B/D.13 (bi) | J1.146 | B/D.08 (bi) | J1.147 |
| -12V | J1.148 | -12V | J1.149 | -12V | J1.150 |

| | | | | | |
|---|---|---|---|---|---|
| J1.151 | GND | J1.152 | GND | J1.153 | GND |
| J1.154 (bi) | B/D.07 | J1.155 (bi) | B/D.12 | J1.156 (bi) | B/D.06 |
| J1.157 (bi) | B/D.05 | J1.158 | GND | J1.159 (bi) | B/D.04 |
| J1.160 (bi) | B/D.03 | J1.161 (i) | A/Reset' | J1.162 (bi) | B/D.02 |
| J1.163 (bi) | B/D.01 | J1.164 | GND | J1.165 (bi) | B/D.00 |

## 4.2 Theory of Operations

The Mesa processor, 80186, display controller, and memory operate at independent speeds. These subsystems are logically joined by the synchronous memory arbiter within the memory controller gate array chip (MCC) on each board. The arbiter grants memory access according to the following priority: refresh, display control, IOP, and Mesa processor. When memory is not busy, the arbiter grants access to the first requesting device. Otherwise, arbitration is performed during the DRAM RAS precharge time.

IOP and Mesa Processor memory requests are initiated by bus transactions. At the 80186 bus port (port A). the memory controller responds to mapped address bits MA23-17 and not to A17-20. At the Mesa bus port (port B), all signals are synchronized with the Mesa processor.

For refresh, the memory controller counts down from the 16 MHz input clock and requests refresh cycles when necessary.

When a memory cycle is granted, the memory controller is started. The memory controller multiplexes the addresses, controls memory timing, delivers data, and starts the IOP arbiter when memory is again available. DRAM strobes are generated from shift registers in the MCC gate array chip.

The memory controller generates and checks byte parity. If the IOP has accessed memory, then a parity error interrupts the IOP. If the Mesa processor has accessed memory, then a parity error traps the Mesa processor.

The MCC synchronously generates RAS, CAS, and other control signals.

The following subsections provide a summary of system memory functions as viewed from the central processor.

### 4.2.1 Read

A read operation is started upon receipt of a MemRef and valid memory address from the selected port. The selected port address is multiplexed to form the Row/Column DRAM address. The RAS/CAS clocks are initiated. Read data is placed on the selected port bus within 250 ns after the start of the cycle.

### 4.2.2 Write

A Write operation is started in the same manner as a Read operation. Write data is multiplexed from the selected port and routed to the DRAM array. Byte parity is generated and sent to the parity DRAMs. The Write operation is completed when the MCC controller issues the 62 ns write clock.

### 4.2.3 Refresh

The memory controller gate arrays contain circuitry for memory refresh. The MCC generates a refresh sycle by issuing a CAS-before-RAS clock sequence. The refresh time circuit within the MCC determines the refresh interval (minimum of 256 cycles in 2 ms). The RAM device contains the refresh address counter and performs the refresh cycle operation.

## 4.3 Programmer Interface

This section describes the memory status registers and typical process timing.

Figure 4.5 illustrates the IOP I/O address map for memory.

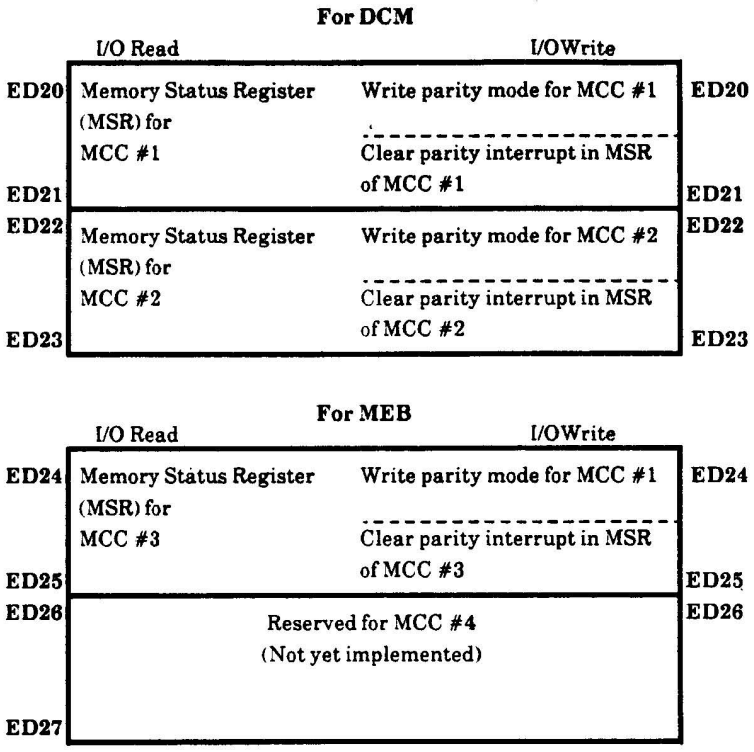


**Figure 4.5.** IOP I/O address map for memory

### 4.3.1 Status Registers

A Memory Control Chip (MCC) controls a unit of memory space. Each MCC has an associated memory status register.

In each unit of memory, the 16-bit, read/write status register, readable at any time by the IOP, logs the following information: Port

A, B, or C selected; the row of 256 Kbit DRAM devices accessed; and the memory page address of a fault.

Figure 4.6 illustrates the register.

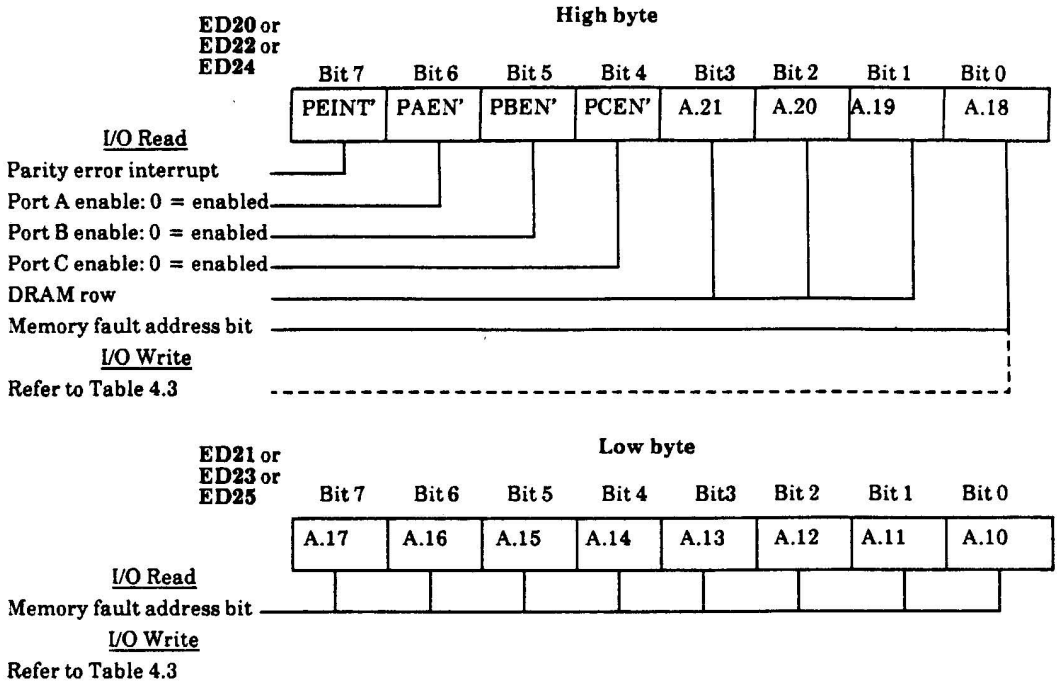


**Figure 4.6.** Memory status register

When a memory error condition is detected, the faulty memory address is logged into the memory status register of the corresponding MCC. The memory status register can be accessed by the I/O read operation.

The I/O write operation has two functions: defining parity mode and clearing parity error interrupts. Table 4.3 lists the address map locations on the MEB for these functions.

**Table 4.3.** I/O Write Operation Locations

| Hex Address | Data bit 0 = | Function |
|---|---|---|
| ED20 | 0 | MCC #1 is odd parity mode |
| | 1 | MCC #1 is even parity mode |
| ED22 | 0 | MCC #2 is odd parity mode |
| | 1 | MCC #2 is even parity mode |
| ED24 | 0 | MCC #3 is odd parity mode |
| | 1 | MCC #3 is even parity mode |
| ED21 | | Clear PEINT' for MCC #1 |
| ED23 | | Clear PEINT' for MCC #2 |
| ED25 | | Clear PEINT' for MCC #3 |

When a parity error is detected, the status register is frozen until read by an IOP status read. Parity defaults to odd parity at system reset. Normal mode parity is odd; special mode parity is even. A special I/O write to a memory bank causes bad parity to be written into memory until changed back to the normal default parity mode. This feature checks the parity checker and the parity-check interrupt to the IOP.

### 4.3.2 Memory Timing

Figure 4.7 illustrates typical processor timing.

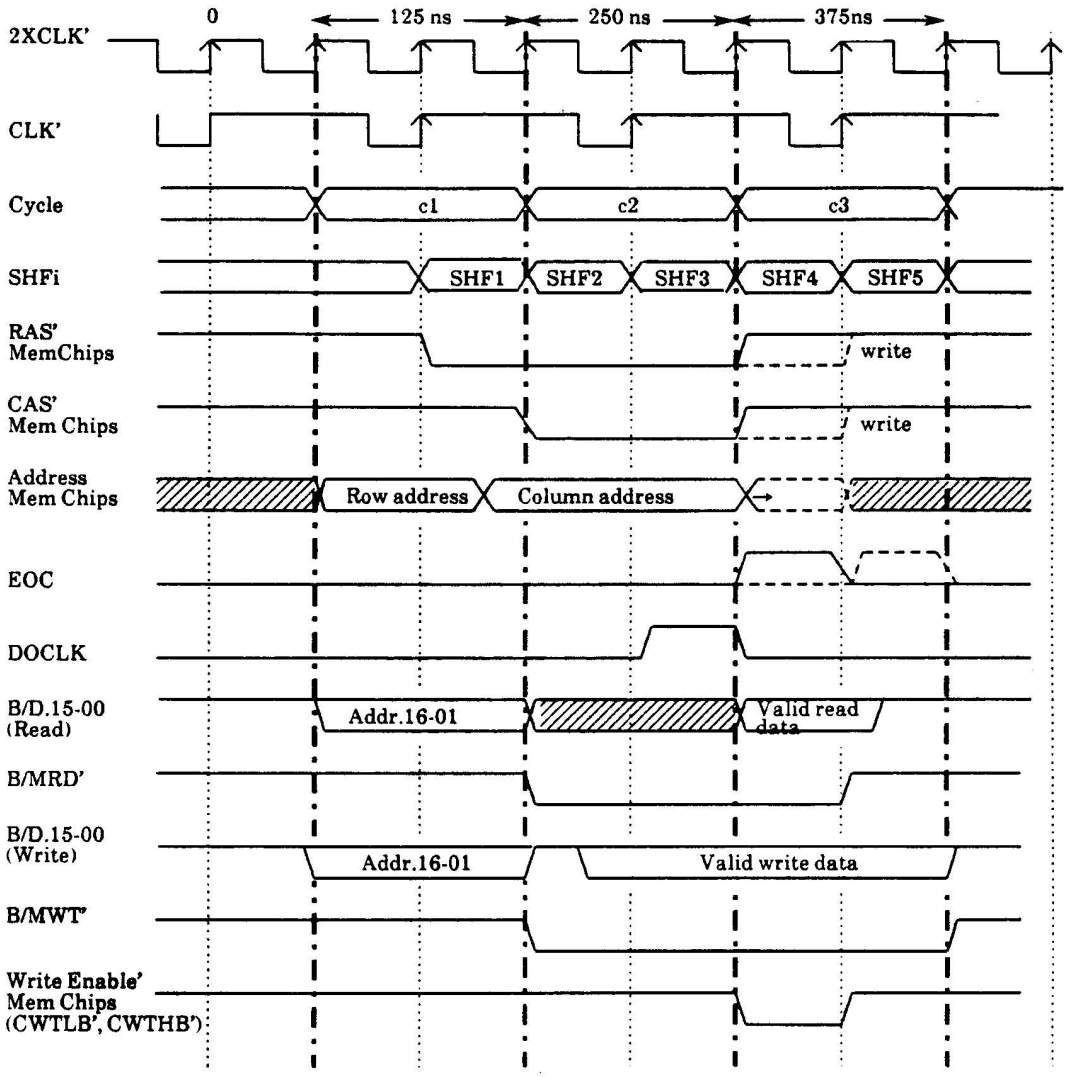


**Figure 4.7.** Memory reference timing

The high order memory address must be valid on the address buses early enough that the proper bank is selected and address lines valid for RAS' (row address strobe). The row address bits are latched in the

DRAM by the RAS' signal. The CAS' (column address strobe) signal occurs 62 ns after the RAS' signal and latches the column address in the memory chips. Data becomes valid at the output of the chips at a maximum of 150 ns after RAS' or 75 ns after CAS', whichever is later.

To be written into memory, data must be supplied within two clocks from RAS'.

## 4.3.3 Functions

Memory functions support full and nibble mode access as well as row and column addressing.

### 4.3.3.1 Full and Nibble Mode Access

The display port supports both full and nibble mode accesses. The full access cycle time is 312 ns; the page mode access time is 687 ns (Quadword). A nibble mode access occurs when the RAS"signal goes low and the CAS' signal cycles several times.

### 4.3.3.2 Row and Column Addressing

Figure 4.8 illustrates how row and column bits are derived from the port address bus.

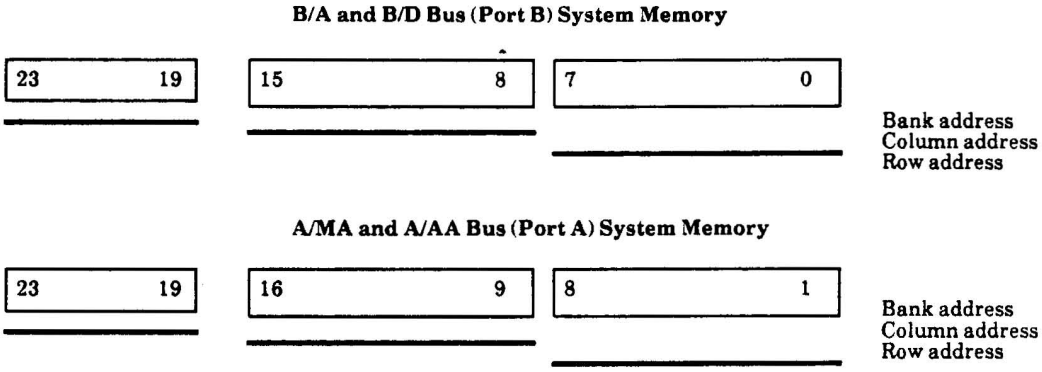


**Figure 4.8.** Row and column addressing