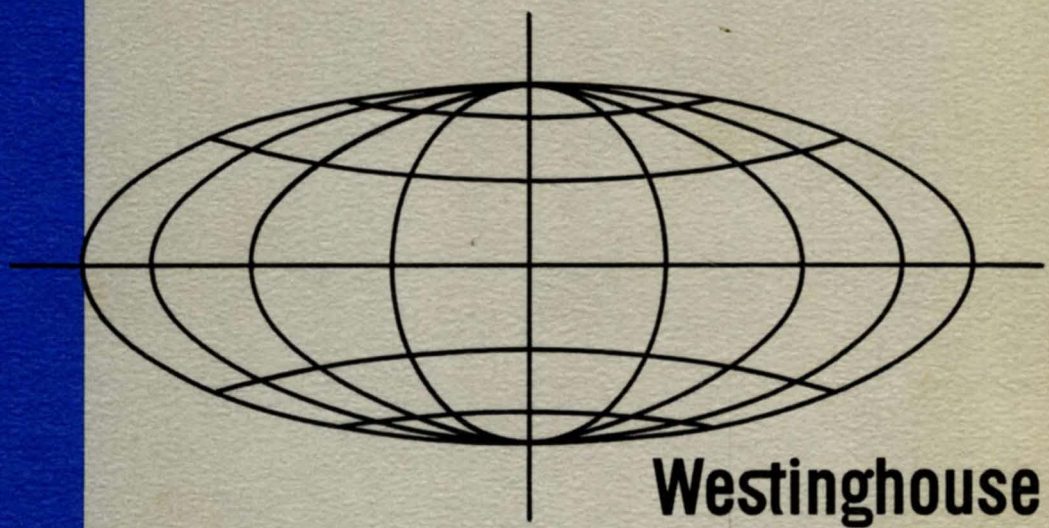
PARALLEL NETWORK PROCESSOR



Westinghouse
DEFENSE AND SPACE CENTER
BALTIMORE, MARYLAND

AEROSPACE DIVISION

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Proposal

for

PARALLEL NETWORK PROCESSOR

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1. INTRODUCTION AND SUMMARY

In response to the stated requirement of the Lawrence Radiation Laboratory for a Parallel Network Processor, Westinghouse Electric Corporation is pleased to submit a proposed program which it is believed will result in filling this requirement in minimum time and with highest performance/cost ratio. This program consists of two phases: a development phase during which all remaining design questions are resolved and each system element fabricated and tested and a production phase which produces sufficient additional, identical units to build the phase 1 system up to operational size.

The basic design of the parallel network computing system known as SOLOMON II was developed by the Westinghouse Electric Corporation under USAF contract AF30(602)3417, Multiple Processing Techniques. Since the completion of this contractual effort Westinghouse has continued the design and development of the Parallel Network Processor (SOLOMON II) System, under corporate sponsorship, resulting in a substantial number of design refinements. As a result the Parallel Network Processor System described in this proposal is a more complete, better defined, and functionally improved machine design than that previously reported in the referenced AF report.

A number of developmental areas still remain in the machine design, but these are well defined, and several reasonable solutions for each are available for final cost-effectiveness determination during phase 1 of the program. Examples of some of the more important design areas that have not yet been resolved are: external interfaces with the SOLOMON II system, diagnostics, maintenance, power distribution and packaging.

Section 2, the technical portion of this proposal concentrates on the design refinements that have been made since the above-cited AF report was prepared. Following a brief basic functional description of the overall system, each major system element is described in detail.

Section 3, Management, presents relevant background and details the proposed Westinghouse phase 1 program.

2. TECHNICAL SECTION

2.1 GENERAL DESCRIPTION OF SOLOMON II

The parallel network of processing elements (PE network) making up the majority of the computation capability of the SOLOMON II system consists of a set of bit-serial arithmetic units controlled by a common source referred to as the network sequence unit (NSU). Each processing element has a unique block of core memory containing 32768 bits referred to as the processing element memory (PEM). The PEM provides bit-serial access in the form of 24-bit words to all PEs simultaneously.

The PEs are arranged in a matrix with a serial data path connecting each PE with the four neighboring PEs. This arrangment provides each PE with access to its own block of memory (referred to as internal memory) and the memories of its four nearest neighbors. The steering of data between PEs and PEM is referred to as data routing. Routing applies only to the reading of data, the PE can write only into its internal memory.

The data paths and the execution of instruction in the PE network are under the control of the NSU and the multimodal status capability of the PE. The NSU supplies the memory address and the control signals for executing all network instructions. The PE mode control determines if the PE is to execute the instruction by comparing the mode value (MV) stored in the PE with program mode control bits from the NSU. The PE mode value capability is provided by a 2-bit (4 state) register in each PE that can be unconditionally set by the NSU, conditionally set on the results of an instruction, stored in PEM, or loaded from PEM. Another condition may also be used to determine if the PE is to execute an instruction. This control is referred to as the "geometric control." Associated with each column and row of the PE network is a control line that must be high for the PEs of that column or row to

execute an instruction. These control lines are referred to as geometric column control and geometric row control, and are connected to two registers (GCR and GRR) which can be modified under a program control. One, both, or neither of these registers can be used to control the PE network on any given instruction. For a PE to execute an instruction GCR, GRR and mode values for that PE must correspond to the selected states in the instruction being executed. When these conditions are satisfied the PE is said to be active and will perform the current instruction. In addition to the data paths between PEs and the PEM mentioned, each PE has a data path to a register that is common to all PEs, a data path that is common to all PEs is a row, and a path that is common to all PEs in a column. These registers are referred to as the "broadcast register" (BR), "L buffer column (LC), and "L buffer row" (LR). BR, LC and LR are two-way data paths controlled by the NSU. The broadcast register functionally is the OR of all the PE accumulators if output is specified, and the source of a common operand for all PEs if input is specified. Transfers between BR and PE are conditional on the PE being active. The LC path is the OR of all PE accumulators of a column of PEs on a one column at a time basis if output is specified, and the source of an operand common to the column if input is specified. The same rules apply for LR transfers in the row direction of the network. Both L buffer transfers are conditional on the PE being active.

The L buffer is a set of registers 24 bits in length that can be loaded bit-serial or word (24 bits) parallel. The number of registers in the L buffer corresponds to one dimension of the PE network. This unit allows data from a parallel memory to be transferred to serial memory.

The word parallel memory in the system is referred to as the program memory (PRM), and is used to store instructions and additional data. The LB-PRM combination allows data to be organized by a conventional sequential processor and transferred to the network. It also allows conventional input-output (I-O) devices to be attached to the system. Only data is transferred between the PRM and the network via the LB. Between the NSU and the PRM is a conventional

sequential control unit referred to as the network control unit (NCU). The NCU is used to process instructions before transferring them to the NSU for execution. The NCU performs functions such as indexing (program modification), input-output control, predecoding of instructions, and loading, storing, and sampling NSU registers.

The set of NSU registers and indicators accessible by the NCU are: BR, GCR, GRR, and the indicator register (IDR). The indicator register is used to test network status; overflow, none, one, or more than one PE active on an instruction and busy conditions in the NSU and PE network.

2.2 SYSTEM DESIGN REFINEMENTS

This paragraph presents refinements in the proposed configuration from that reported in the final report submitted under USAF/RADC Contract AF30(602)3417.

2.2.1 PE-Memory Interface

The PEM system described in the AF report has been reorganized to allow greater flexibility in network size. This alteration has also significantly reduced the electrical problems of transmitting data between the network and the memory. The earlier PEM system required 8 memories for each module of 256 PEs. Each PE was connected to one bit position of eight 256 x 4096 bit memory banks via a collection gate illustrated in figure 2-1.

In the current memory interface design one 256 x 4096 bit memory is connected to 32 PEs via a shift register. The contents of the 256-bit memory read/write register is gated in parallel to a 256-bit shift register. Each PE is assigned an 8-bit segment of the shift register which allows a 1-microsecond memory to supply 32 PEs with data at an 8-mc rate (figure 2-2). This implementation allows a system to be built up of blocks of 32 PEs rather than 256. It also allows the memories to be placed much nearer the PE network which significantly reduces length of the communication path.

The implementation of the L buffer, geometric control registers, and NSU signal driver to the network has been modified to allow these items to be expanded as blocks of 32 PEs are added to a system.

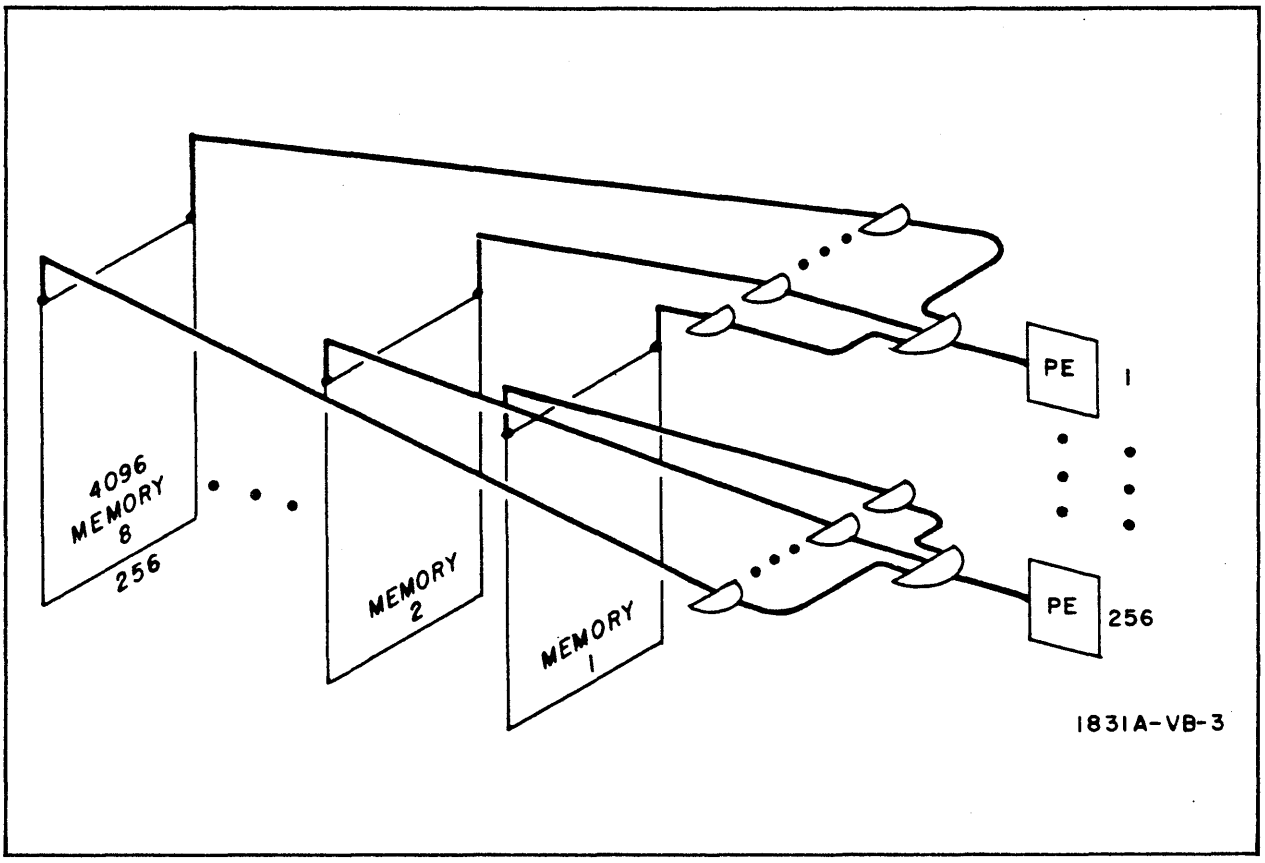


Figure 2-1. PE-PEM Interface for Previous 256-PE Module

2.2.2 PE Design

Since the majority of the components, cost, and complexity in the SOLOMON system is in the PE network, much effort has gone into optimizing and minimizing the PEs themselves. A basic change has been made in the PE design to permit operation with 24-bit words in lieu of 20-bit words as was specified in the AF report. To maintain compatibility with this basic change and to provide a safety factor in circuit requirements and NSU signal distribution tolerances, an 8-mc logic system rate has been chosen. The PE logic design itself has undergone some beneficial evolution due primarily to the ability to modularize the PE network on the basis of 32 rather than 256, and the concurrent PEM design improvements outlined in the preceding paragraph. The algorithms and actual manipulations involved in performing instructions have been slightly modified in several cases to take advantage of the aforementioned

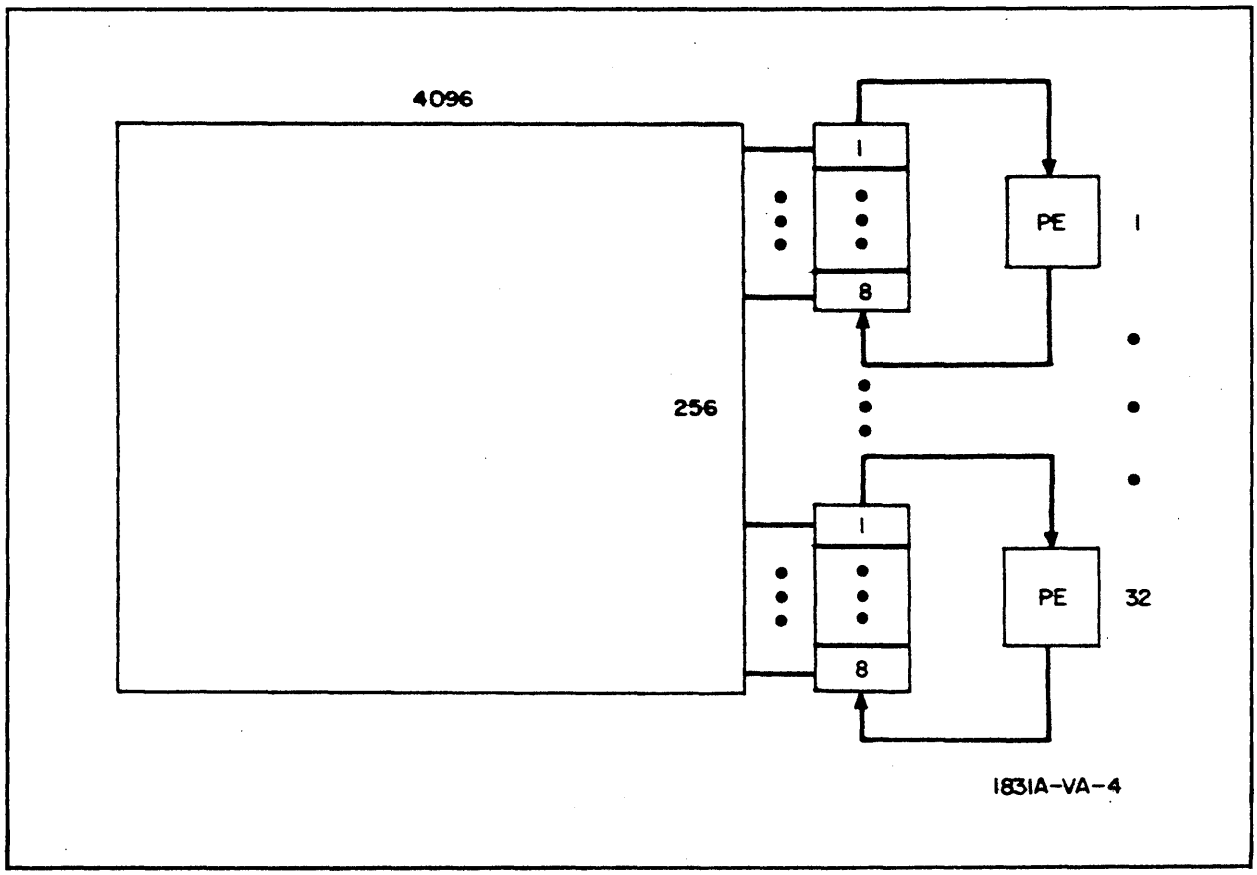


Figure 2-2. PE-PEM Interface for Present 32-PE Module

improvements in the basic PE network structure. Table 2-1 indicates complete instruction operating times (including fetch or storage of operands) for the current SOLOMON II system. In cases where major alogrithm or functional changes have occurred the present system is described in detail for each instruction in the following paragraphs.

2.2.2.1 PE Instructions

Due to the large number of multiply operations in mesh calculations and similar problems, intensive efforts have been made to arrive at an efficient multiply capability. Design studies have shown that a number of adders connected in series is the best way to gain speed in this operation in a basic serial structure. All applicable and promising techniques were analyzed to determine the best cost versus performance ratios.

TABLE 2-1

PE OPERATION TIMES

Command Description	Time (μsec)
Multiply	19.1
Any compare	3.8
Any command that writes into memory	3.8
Divide	84.6
Shifts:	
1. single length left circular $\geq$ 12	12.8
2. single length left circular < 12	6.4
3. single length left algebraic $\geq$ 12	6.5
4. single length left algebraic < 12	3.3
5. single length left logical $\geq$ 12	6.5
6. single length left logical < 12	3.3
7. single length right algebraic $\geq$ 12	6.2
8. single length right algebraic < 12	9.4
9. single length right logical $\geq$ 12	6.2
10. single length right logical < 12	9.4
11. double length left algebraic $\geq$ 12	13.5
12. double length left algebraic < 12	6.8
13. double length left logical $\geq$ 12	13.3
14. double length left logical < 12	6.6
15. double length right algebraic $\geq$ 12	9.8
16. double length right algebraic < 12	16.4
17. double length right logical $\geq$ 12	16.1
18. double length right logical < 12	9.6
All other commands	3.4

Two multiply techniques were selected and evaluated in detail and their cost and speed charted. Scheme A was that scheme used in the 10-mc PE described in the AF report, and Scheme B is described later in this section.

Also, a two-bit multiply scheme for each adder was costed and the speed charted. Table 2-2 shows this cost breakdown with the speeds in the adjacent column. It was finally decided that Scheme B with 6 adders would be used in SOLOMON II. Furthermore, a cost decrease for the system was realized in that the multiplicand could come from memory through four separate accesses and thereby save one of the delay lines in the PE.

TABLE 2-2

SUMMARY CHART-PE MULTIPLY COST/EFFECTIVENESS

Mul Time (μsec)	LOGIC COST FACTOR	Scheme
31.0	430	3 x 1 B
28.6	480	3 x 1 A
25.0	560	4 x 1 B
22.5	640	4 x 1 A
19.1	800	6 x 1 B
17.0	920	6 x 1 A
16.0	1070	8 x 1 B
14.0	1200	4 x 2 A
13.0	1550	6 x 2 B
11.8	1800	6 x 2 A
(for 24 bit words)	(per PE)	(No. of adders times No. of bits at a time)

* Additional Logic cost for the rest of the PE in all schemes is approximately $1200 (cost for PE multiply with 5 adders as in 10 mc AF report system is approximately $680).

After the multiply scheme was decided upon and designed, the basic gates for the add, Boolean mode control, etc, instructions were added. Divide was then designed and finally the shift instruction was added. Here again as in multiply considerable investigation was done to determine how shift would be

implemented. Using scheme 1 as a basis for hardware count, 6 schemes were costed and the corresponding shift times calculated. After careful analysis (summarized in table 2-3) it was decided that scheme 1 would be the most satisfactory solution. Scheme 1 is discussed in more detail below.

TABLE 2-3

SHIFT INSTRUCTION ANALYSIS

Shift Scheme	Extra PE Hardware
1. L shift < 13 3.3 μsec L shift ≥ 13 6.6 μsec R shift < 13 9.8 μsec R shift ≥ 13 6.6 μsec	No hardware
2. L shift < 13 3.3 μsec L shift ≥ 13 3.3 μsec R shift < 13 6.6 μsec R shift ≥ 13 6.6 μsec	2-5 bit delays 1-2 bit delays 2-diode cans
3. L shift < 13 3.3 μsec R shift < 13 4.9 μsec Two commands for shift ≥ 13 μsec	3-5 bit delays 1-2 bit delays 2-diode cans
4. L shift < 13 8.0 μsec L shift ≥ 13 8.0 μsec R shift < 13 8.0 μsec R shift ≥ 13 8.0 μsec Uses 2 fixed memory location	Save: 2 diode cans 1-2 bit delay
5. L shift < 13 3.3 μsec R shift < 13 3.3 + SL Destroy all Q's not in right mode or store all Q's in memory Two commands for shift ≥ 13	No hardware
6. L shift < 13 3.3 μsec R shift < 13 7.3 + μsec Two command for shift ≥ 13 uses 1 fixed memory location	No hardware

2.2.2.2 Add, Subtract, and Boolean Instructions

The processing element receives all its data in the R register. The control signals from the NSU determine which input will be recognized. These include memory inputs from North, South, East, and West neighboring PEs, internal memory, BR, and L-buffer inputs either via row or column.

From the R register data it is then directed to different flip-flops in the PE depending upon the instruction. A load instruction will send data to S_0. The word then goes through S_1 then to P_{25} where it is circulated. The total time for this instruction is 27 bit times or 3.3 microseconds.

A load Q instruction will send this data to Q_{27} then to Q_{25} and circulation in the Q line.

If the instruction is add, R may be chosen as operand 1 in which case it is gated to b_0 or operand 2 may be chosen, in which case it is gated into S_0. At this point it is gated into the adder S_1 where an addition occurs with the other operand. The operand may be the contents of either P or Q. The 24-bit addition occurs in 27 bit times. The reason for this time is that: (1) 24 bit times must be used for data storage itself (P_1 and delay line) and (2) one bit time is used to select the proper operand (S_0 and b_0). This selection not only includes the selection of R, P_1, and Q_1, but also their complements. This permits subtraction, and in addition, the capability exists to do absolute value instruction of P at this level, (3) one bit time to perform the actual addition, or logical operation whichever the case might be (S_1), and (4) one bit time for selection of where the answer will be written. This may be either in P (P_{25}) or Q (Q_{25}). All additions and Booleans are merely single modifications of the above-mentioned operations. The additions and Booleans differ in the PE only in control signals necessary for S_1 and C_1.

It seems appropriate to mention mode control at this point in that it effects these commands as it effects all commands. If the proper mode of the instruction is specified the PE will perform the specified operation and the resultant bits will be circulated in the proper delay line and be ready for another operation at the end of 3.4 microseconds. If, however, the PE is not in the proper mode the EXC flip-flop will not be set. In this state the PE must not alter any of the data within itself. Therefore the result of the computation

must be rejected at (P_{25}) or (Q_{25}) and the old information restored in the delay lines. The information also must stay aligned in time with that data in other PEs which have been modified.

The path for this delay is

$P_1 \rightarrow C_5 \rightarrow C_6 \rightarrow P_{25}$ (27-bit path)

$Q_1 \rightarrow Q_{27} \rightarrow 1\Delta \rightarrow Q_{25}$ (27-bit path)

If an add instruction does not use a memory cell for the address of one operand, it may in fact store one operand (P or Q) in a specified memory cell. Due to the peculiar nature of the memory and its association with the PE it is necessary to increase the time for this class of instructions to 3.8 microseconds. The flip-flop used to write information is b_b and will select either P or Q but not the result of the operation.

The paths for this operation are

P_{EXC}

$P_1 \rightarrow S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_4 \rightarrow S_5 \rightarrow S_6 \rightarrow P_{25}$ or Q_{25}

P_{EXC}

$P_1 \rightarrow R \rightarrow \underline{C_2} \rightarrow C_3 \rightarrow C_4 \rightarrow C_5 \rightarrow C_6 \rightarrow P_{25}$

Q_{EXC} and $\overline{EXC}$

$Q_1 \rightarrow 5\Delta \rightarrow Q_{27} \rightarrow Q_{26}$

Within the logic for the above-mentioned instructions exists the capability to detect overflow. Overflow is detected on all add and subtract instructions. The OF flip-flop is set when overflow occurs and then enacts the program options for handling overflow. They may

a. set the mode flip-flop to the desired states

b. set the mode flip-flops and jump

c. jump

d. do nothing

Another class of instructions is the compare commands. These instructions are similar to the add command except the result of the operation is used to set the PE modes accordingly. This setting of the modes requires extra time since first the set must go to the OF flip-flop so it can control the mode states.

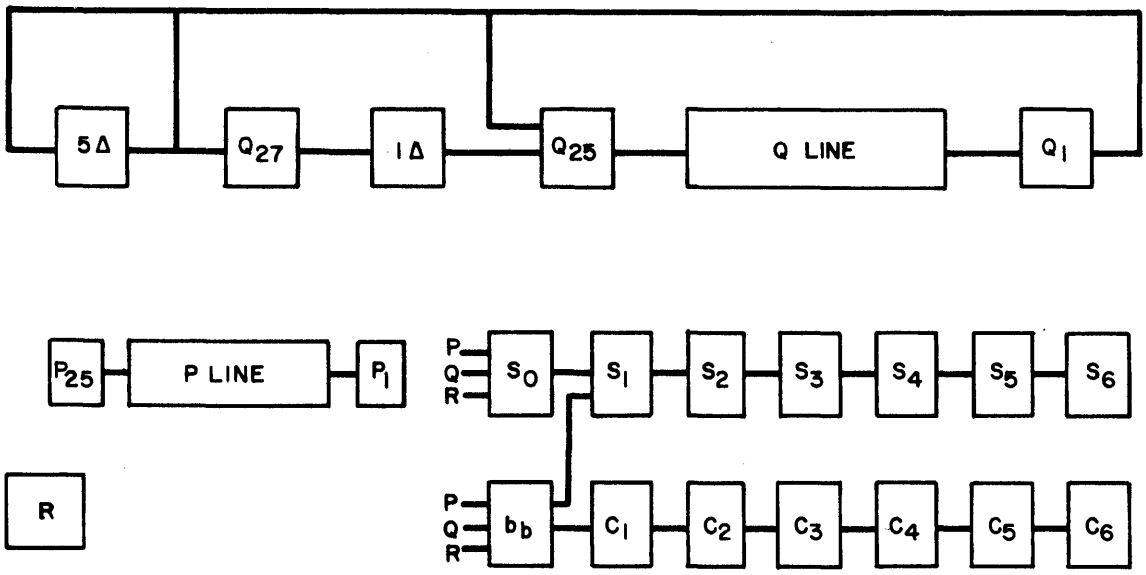
It becomes convenient to choose the same time for this instruction as for a write instruction since the compare commands always require information to be rewritten in the P and Q lines. The data paths are:

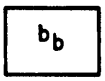
$P_{\overline{EXC}}$ and EXC

$P_1 \rightarrow b_b \rightarrow C_2 \rightarrow C_3 \rightarrow C_4 \rightarrow C_5 \rightarrow C_6 \rightarrow P_{25}$

Q_{EXC} and $\overline{EXC}$

$Q_1 \rightarrow 5\Delta \rightarrow Q_{27} \rightarrow Q_{25}$





b_o - OPERAND

S_o - OPERAND

S_n - $ADDER_n$

C_n - $CARRY_n$

Q_{27}, Q_{25} - Q INPUT SELECT

P_{25} - P INPUT SELECT

b_b - OUTPUT SELECT

R - ROUTING SELECT

2.2.2.3 Multiply Instruction

There is essentially only one multiply instruction. This instruction causes R to be multiplied by Q with a double length product to be stored in P and Q (i.e., R x Q→P, Q). A multiplication of -1 x -1 (an allowable number) produces an incorrect product of -1.

The basic multiply algorithm is shown in figure 2-3. Examples 1, 2, and 3 illustrate the multiplication of two numbers by use of this algorithm.

Figure 2-4 illustrates the logical sequence of the multiply operation with respect to the 6 adders. Basically six multiplier bits at a time are stored in multiply control flip-flops (I_1 - I_6) which perform the function of controlling the corresponding 6 adders. When the multiply control flip-flops are set, the multiplicand bits are transmitted serially to the 6 adders - least significant bit first. On the basis of the corresponding control flip-flop, the adder either adds or does not add the multiplicand to the partial product. Figure 2-5 illustrates the actual sequence for the 4 cycles and figure 2-6 illustrates the operation of each adder and how those bits feed the next successive adder. For example, on the first 6-bit cycle (this refers to 6 multiplier bits) product bits P_{47} - P_{42} are generated (i.e., $P_{47} = A_{33}$, $P_{45} = A_{21} + A_{22} + A_{23}$, etc). Of course, if the corresponding multiplier bit is zero, then the multiplicand is not added (i.e., if M_{21} is zero and M_{22} and M_{23} are 1, then $P_{45} = 0 + A_{22} + A_{23}$) each additional 6-bit cycle will generate 6 product bits and on the fourth cycle the remaining 29 bits are produced.

Figure 2-7 is a block diagram of the system which performs the multiplication. Figures 2-8 and 2-9 refer to the timing necessary to implement the multiply. If the processing element is not in the proper mode, the multiply must not be undertaken and no change should occur on the data within it.

By virtue of the EXC and $\overline{\text{EXC}}$ signals, the mode distinction is made in the PEs.

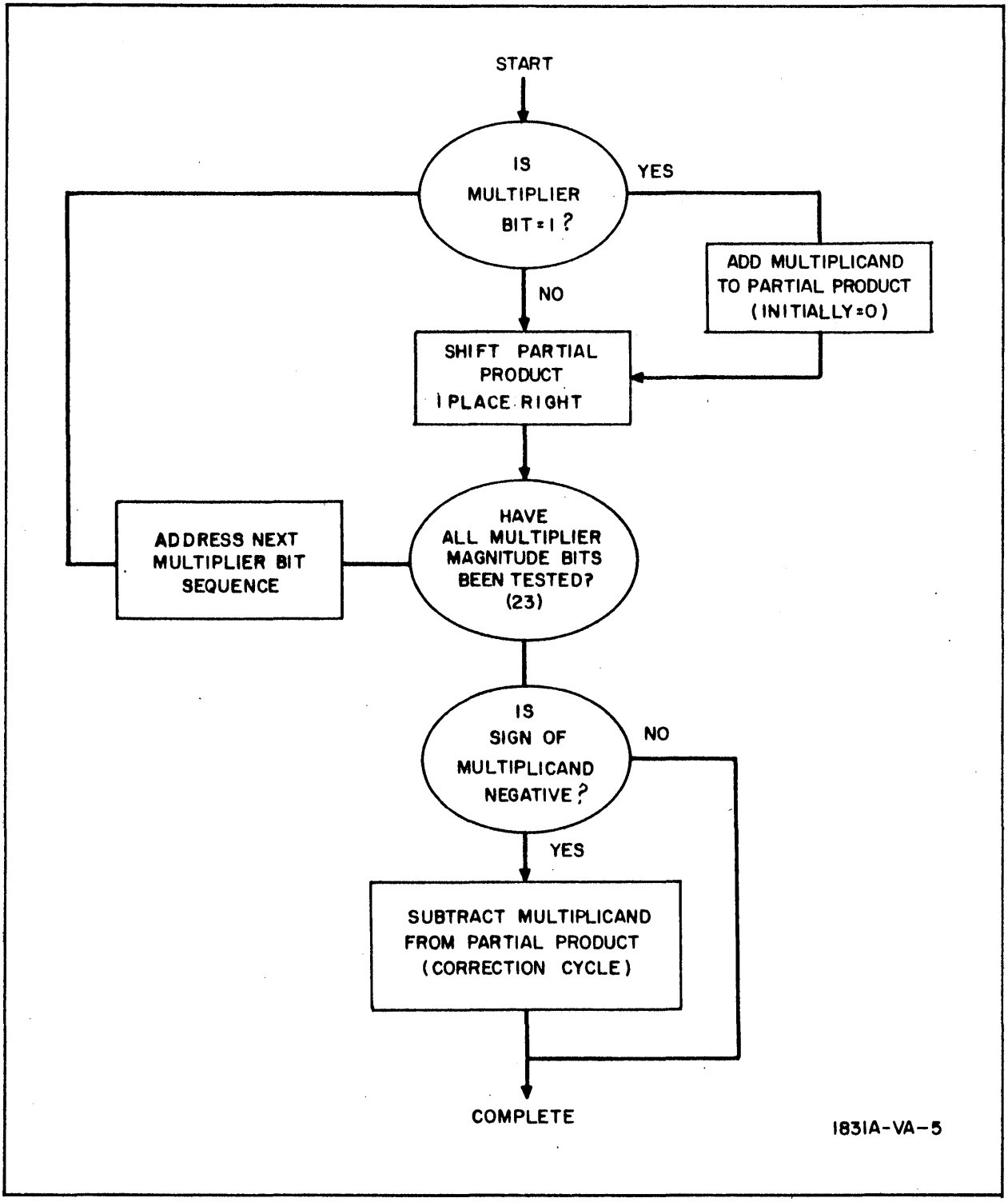


Figure 2-3. Basic Multiply Algorithm

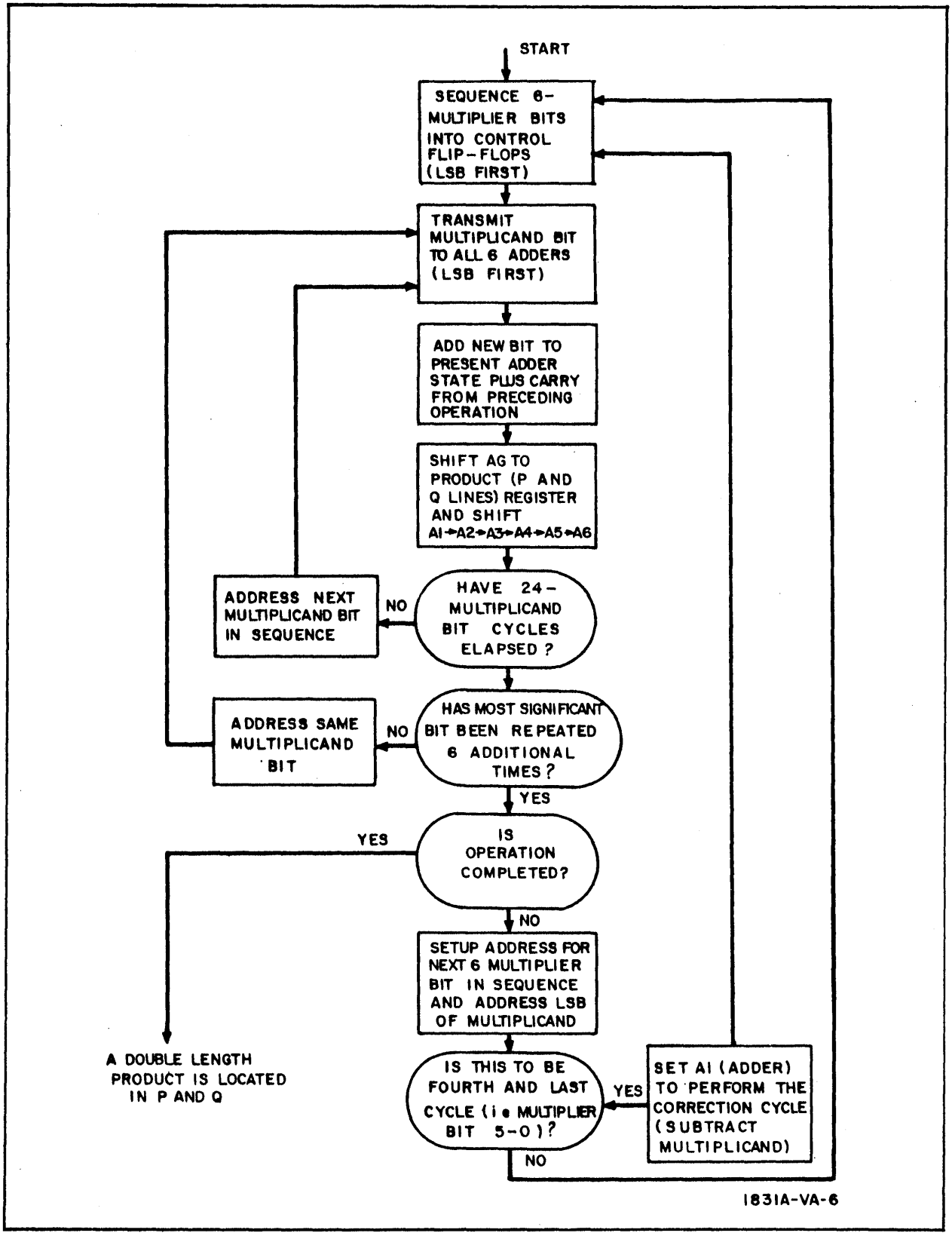


Figure 2-4. Logical Sequence of SOLOMON II Premultiply Scheme

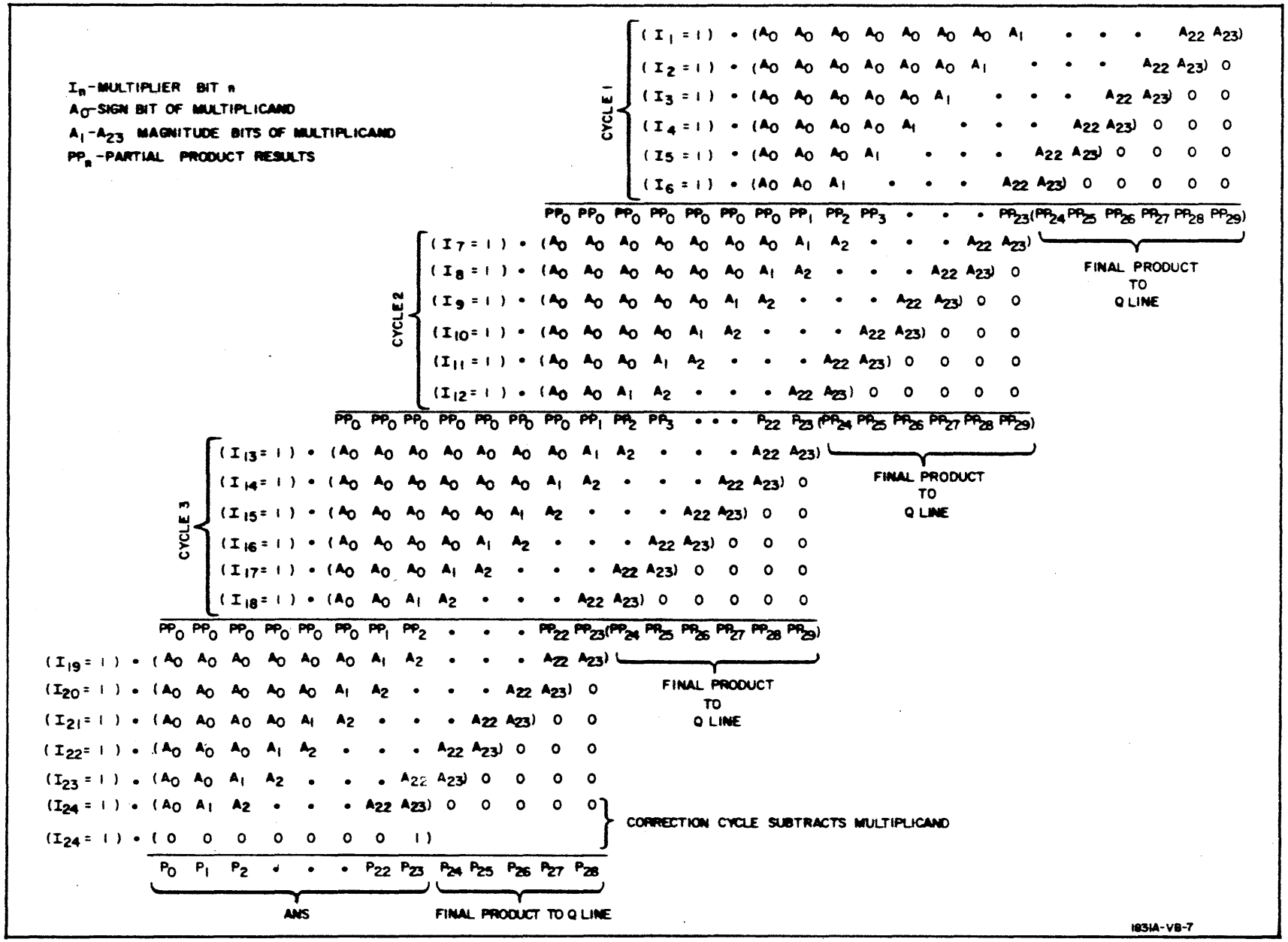


Figure 2-5. SOLOMON PE Logical Representation of Multiply Sequence

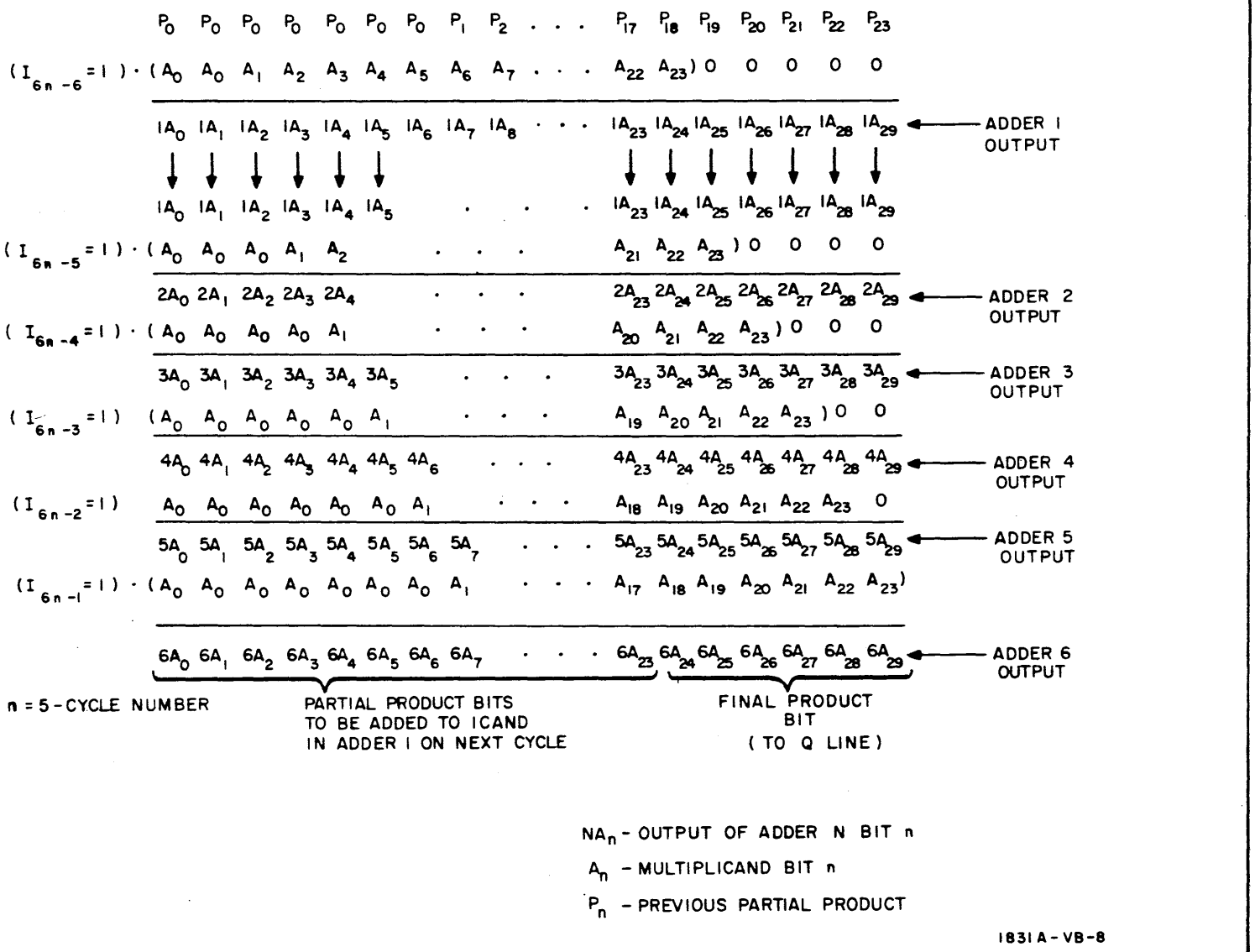


Figure 2-6. SOLOMON PE Multiply Sequence, 1 Cycle

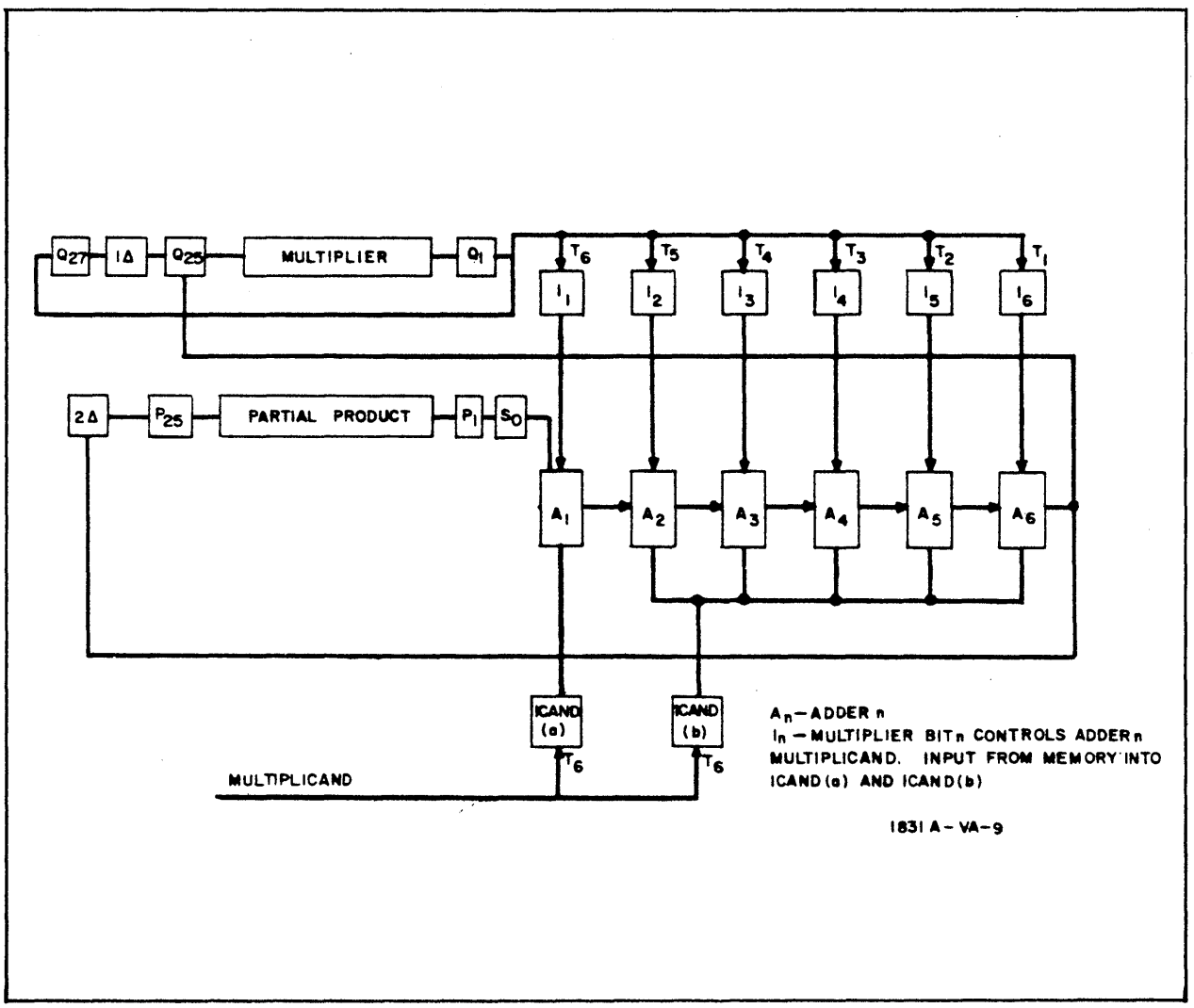


Figure 2-7. SOLOMON II PE Multiply Hardware (Block Diagram)

The nonexecute paths for multiply are:

FOR P

$P_1 \rightarrow P_{25}$ (25-bit path) 3 cycles = 75 bit times

$P_1 \rightarrow b_b \rightarrow P_{25}$ (26-bit path) 3 cycles = 78 bit times

FOR Q

$Q_1 \rightarrow Q_{25}$ (25-bit path)

$Q_1 \rightarrow Q_{27} \rightarrow Q_{25}$ (26-bit path)

Each block in figures 2-8 and 2-9 refers to an operation performed by the element shown in figure 2-7, and the size of the blocks are identical to the

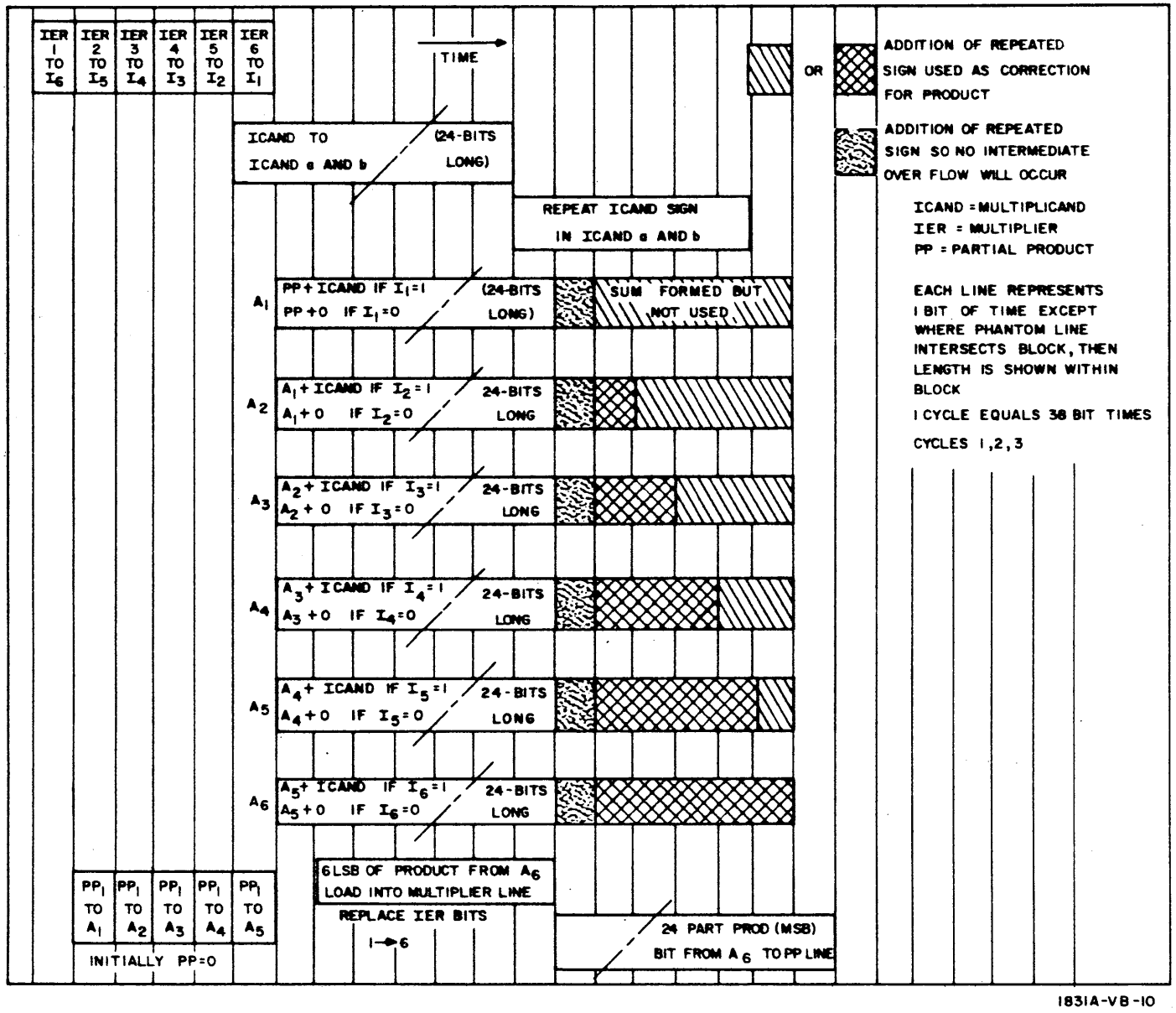


Figure 2-8. Multiply Instruction Timing

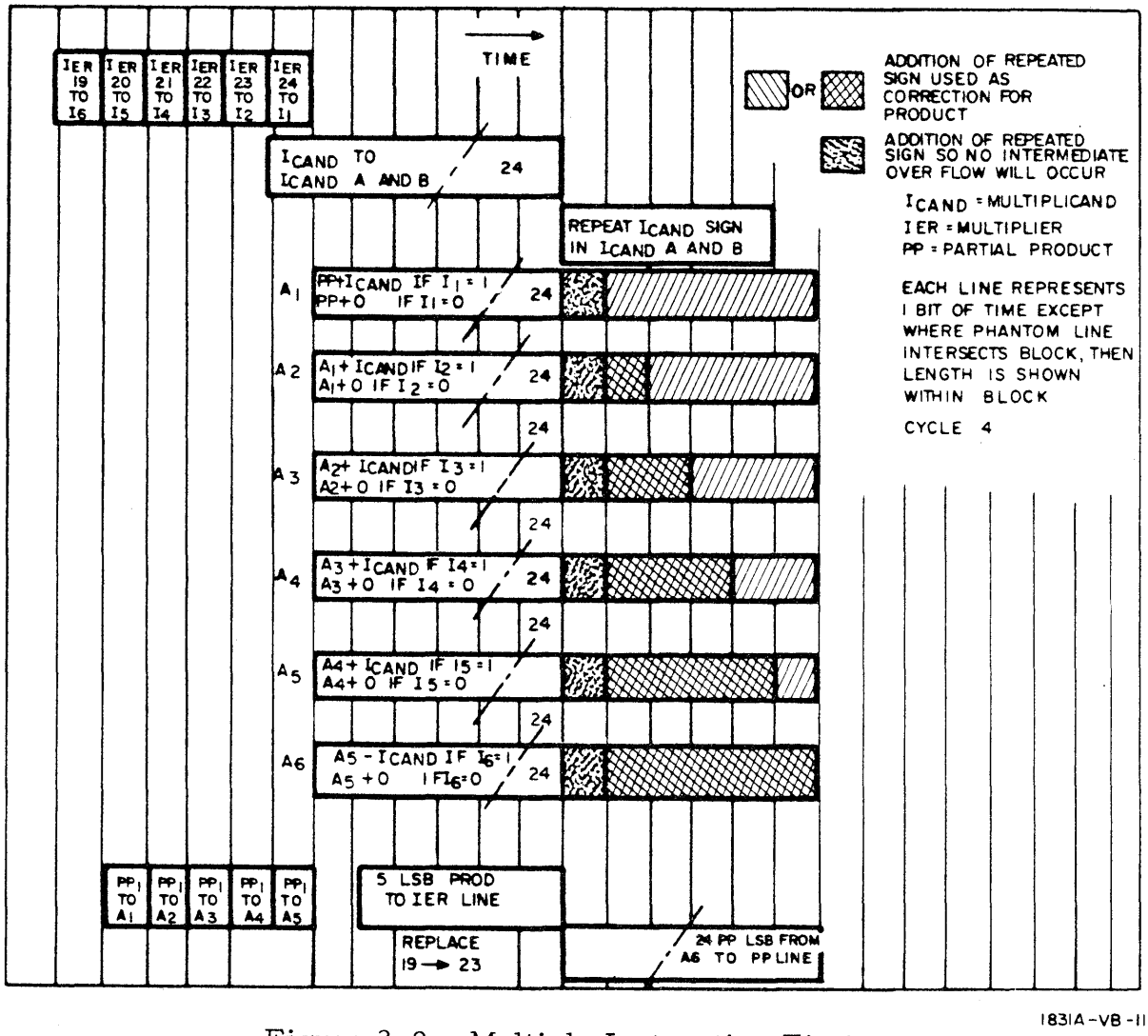


Figure 2-9. Multiply Instruction Timing

length of the operation except where phantom lines cut the blocks. In this case, the number of bit times are specified inside the block. (Note that each vertical line refers to a bit time.) The entire operation requires 153 bit times for completion.

Multiply Examples

Example 1

Multiplicand =						0	0	1	0	0	1	= +9/32
Multiplier =						0	0	1	1	0	1	= +13/32
	0	0	0	0	0	0	0	1	0	0	1	
	0	0	0	0	0	0	0	0	0	0		
	0	0	0	0	0	1	0	0	1			
	0	0	0	0	1	0	0	1				
	0	0	0	0	0	0	0					
	0	0	0	0	0	0						
Product = Sign	0	0	0	0	1	1	1	0	1	0	1	= +117/1024

Example 2

Multiplicand =						0	0	1	0	0	1	= +9/32
Multiplier =						1	0	1	1	0	1	= -19/32
	0	0	0	0	0	0	0	1	0	0	1	Correct cycle, if
	0	0	0	0	0	0	0	0	0	0		sign of multiplier
	0	0	0	0	0	1	0	0	1			is negative subtract
	0	0	0	0	1	0	0	1				multiplicand (i.e.,
	0	0	0	0	0	0	0					2's complement and
	1	1	0	1	1	1						add)
Product =	1	1	1	0	1	0	1	0	1	0	1	= -171/1024

Example 3

Multiplicand =						1	0	1	0	0	1	= -23/32
Multiplier =						0	0	1	1	0	1	= +13/32
	1	1	1	1	1	1	0	1	0	0	1	
	0	0	0	0	0	0	0	0	0	0		
	1	1	1	1	0	1	0	0	1			
	1	1	1	0	1	0	0	1				
	0	0	0	0	0	0	0					
	0	0	0	0	0	0						
Product =	1	1	0	1	1	0	1	0	1	0	1	= -299/1024

Note that sign bit of negative multiplicands is propagated to form final product.

2.2.2.4 Division

Divide within the PE can be performed on either single or double length dividends. The divisor is located in PE memory and its address is specified by R. If a single length divide is specified, the dividend is located in the P register (i.e., the most significant of a double length product). If double length, divide is specified the least significant half of the double length dividend and is contained in the Q register. A single length quotient will be formed in either case with the quotient stored in the P register and the remainder stored in the Q register.

To illustrate in detail the divide operation, the actual divide algorithm is given in figure 2-10 and a block diagram for accomplishing this in the PE is shown in figure 2-11. Figure 2-12 illustrates the overflow tests performed on the operands. By observation of figure 2-10 and the divide examples 1, 2, and 3, one can readily see exactly how division is accomplished in the PEs. Note that in example 2, 5/16 is the dividend and -8/16 is the divisor which yields a quotient of -11/16, while in example 3 with the same absolute values the dividend is negative and the divisor is positive the quotient is -10/16. Obviously then the exact quotient is not obtained in all cases since -10/16 is exact and -11/16 is 1/16 in error. Due to the rather simple nature of the PE, the correction cycles to ensure an exact divide are not implemented. However, in all cases the correct quotient can be obtained by considering the remainder with the quotient. Table 2-4 outlines the possibilities that can exist.

The total time for the divide instruction is 84.6 microseconds. After the initial over flow test the sign of the divisor and the dividend (remainder after first cycle) are compared as shown in example 1 and stored in P sign. This then controls whether the divisor is added or subtracted from the remainder. The P sign value is gated into the Q line in Q_{25} at the appropriate time. This is repeated for the 24 bits with the cycle repeating every 26-bit times. Note that the path is 27 bits (figure 2-11) but that a shift must be affected each time and this is accomplished by using 26-bit times for the repeat time.

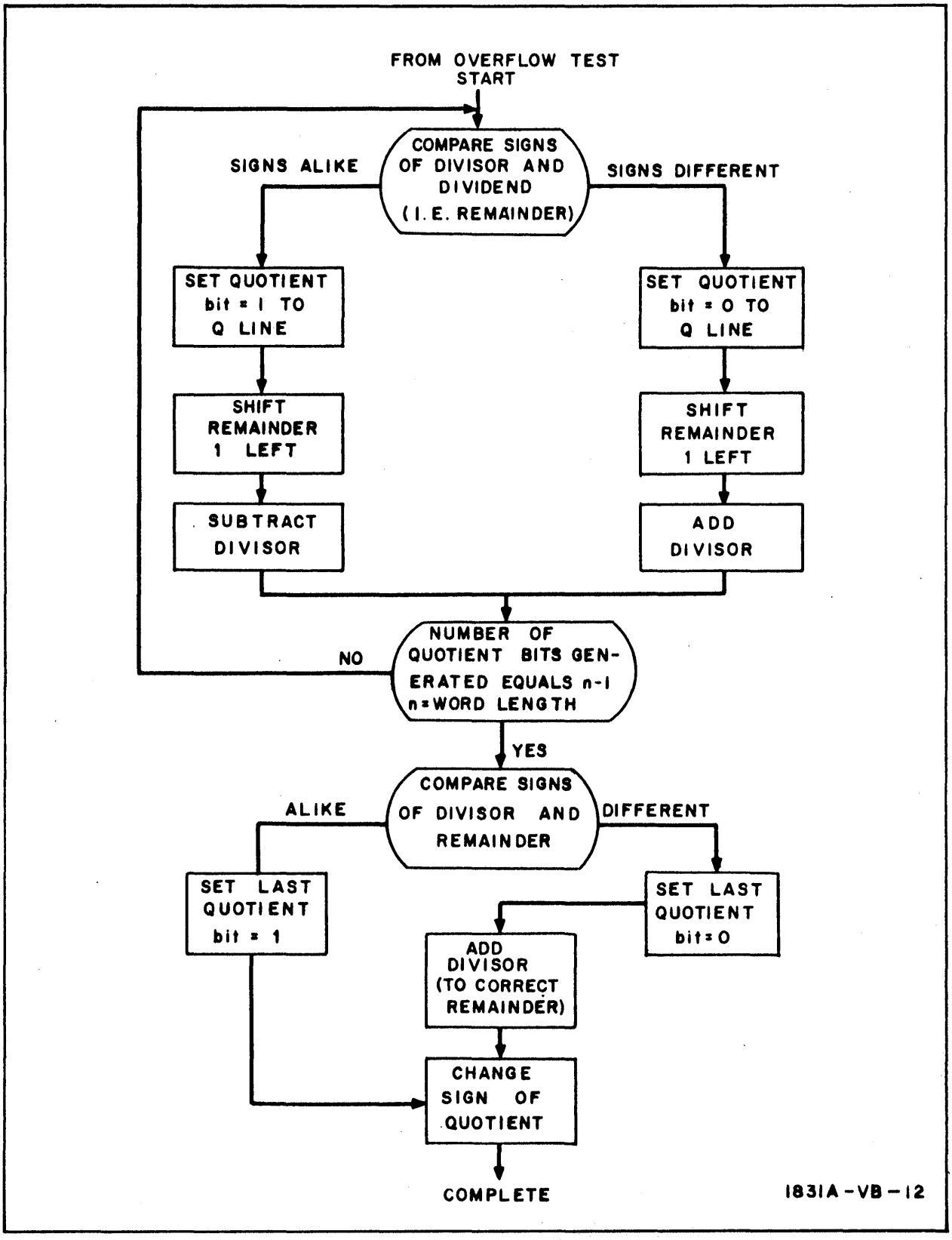


Figure 2-10. Divide Alogrithm

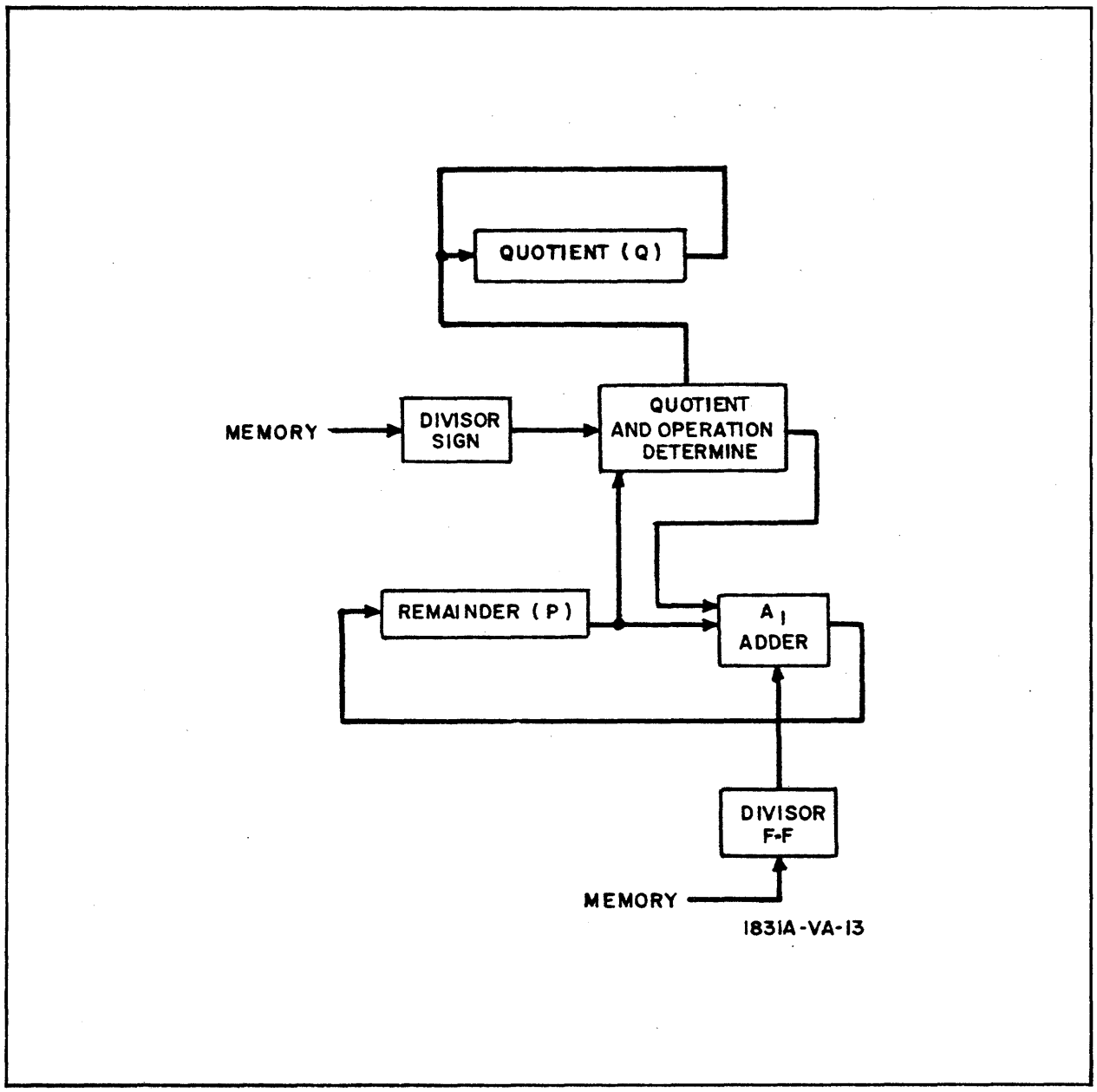


Figure 2-11. PE Divide Hardware (Block Diagram)

The nonexecute paths to keep the operands aligned are:

P $\overline{\text{EXC}}$	Q $\overline{\text{EXC}}$
$P_1 \rightarrow C_5 \rightarrow C_b \rightarrow P_{25}$ (1 time)	$Q_1 \rightarrow Q_{27} \rightarrow \Delta \rightarrow Q_{25}$ (1 time)
$P_1 \rightarrow b_b \rightarrow P_{25}$ (25 times)	$Q_1 \rightarrow Q_{27} \rightarrow Q_{25}$ (25 times)

Divide Examples

Example 1

Dividend = 11111110 = -1/64
Divisor = 01000000 = +1/2

	Operation	Signs Status	Quotient Bits
11111100	Shift	Differ	0
01000000	Add		
00111100		Alike	1
01111000	Shift		
11000000	Subt		
00111000		Alike	1
01110000	Shift		
11000000	Subt		
00110000		Alike	1
01100000	Shift		
11000000	Subt		
00100000		Alike	1
01000000	Shift		
11000000	Subt		
00000000		Alike	1
00000000	Shift		
11000000	Subt		
11000000		Differ	0
10000000	Shift		
01000000	Add		
11000000		Differ	0
01000000	Add		
00000000	Final Remainder		

01111100 Incorrect Quotient
1 Correction Cycle (Change Sign)
11111100 Final Quotient

Example 2

1.1011 -5/16 - Dividend
0.1000 +8/16 - Divisor

```
10110          0
01000
-----
11110

11100          0
01000
-----
00100

01000          1
11000
-----
00000          1

00000          0
11000
-----
11000

11000
01000          Correction Cycle
-----
00000          Corrected Remainder
```

0.0110 Uncorrected Quotient
1.0110 Corrected Quotient
1.0110 = -10/16 with 0/16 Remainder

Example 3

0.0101 5/16 - Dividend
1.1000 -8/16 - Divisor

```
01010          0
11000
-----
00010

00100          0
11000
-----
11100

11000          1
01000
-----
00000

00000          0
11000
-----
11000 Remainder 1
```

0.0101 Uncorrected Quotient
1.0101 Corrected Quotient
1.0101 = -11/16 with -8/16 Remainder

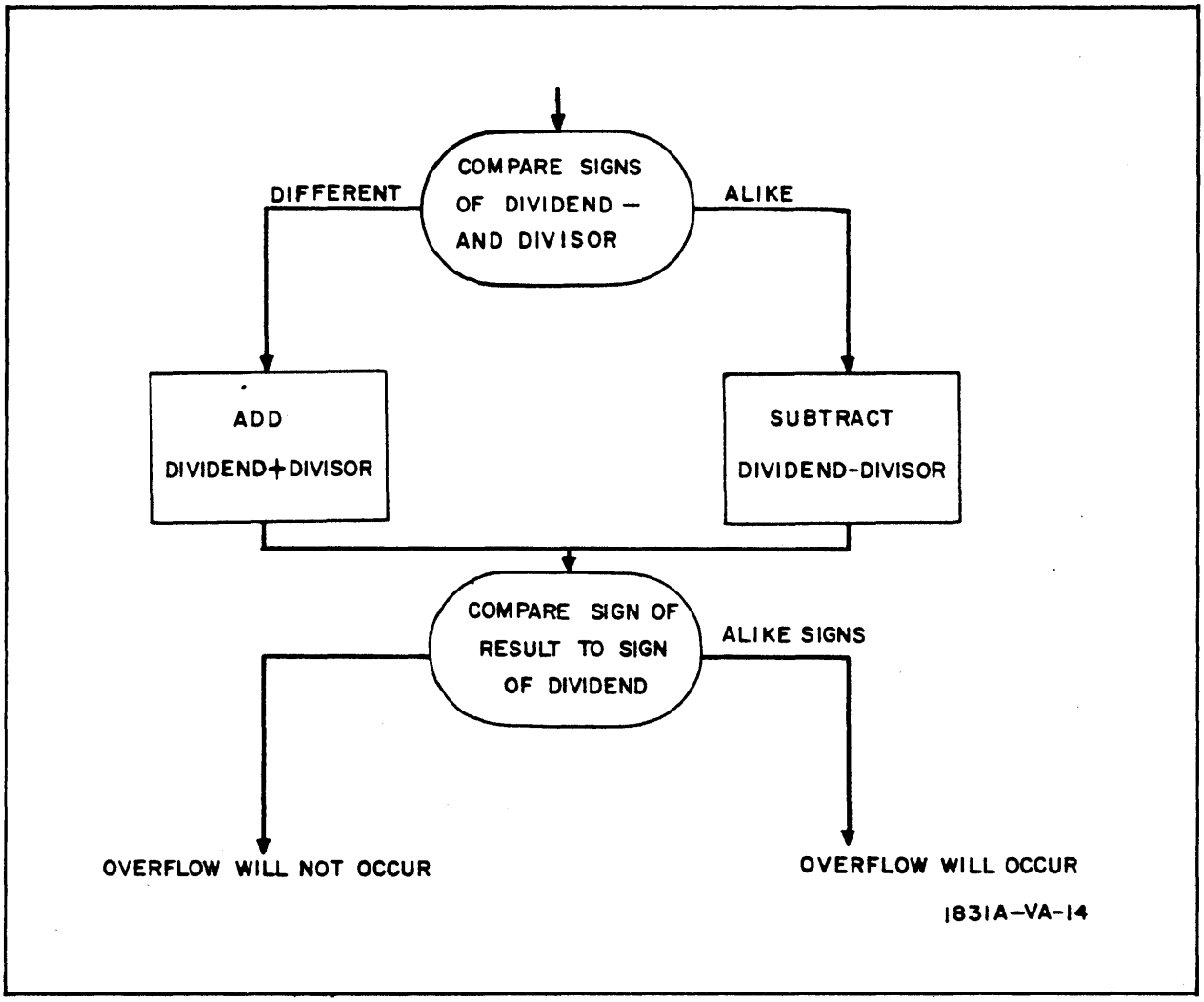


Figure 2-12. Divide Overflow Test

TABLE 2-4

TABULATION OF POSSIBLE DIVISION RESULTS

Divisor Sign	Dividend Sign	Quotient Nature	Quotient	Remainder
-	±	Exact	Exact answer -2^{-23}	Sign and magnitude of = divisor
+	±	Exact	Exact answer	= zero
-	±	Nonexact	Unrounded (magnitude is too large)	= negative
+	±	Nonexact	Unrounded (magnitude is too small)	= positive

2.2.2.5 Shift Instructions

In SOLOMON where some PEs may be operating and some may remain unchanged, all instructions must be of such a length as to have the first bits in all PEs aligned at the conclusion of the instruction. As a result the way chosen to effect a shift is to enter delays into the delay-line loop. The basic time for a left shift is approximately 1-word time and a delay equal to the shift length is added to the delay loop. For a right shift the basic time for the instruction becomes twice the word time and the delay which is added equals 25 minus the shift length. Since the object in designing in the shift was to use as much existing hardware as possible, it was found that only 14 delays could be found without adding extra flip-flops and delay elements. As a result, in order to do a left shift of greater than 13, two passes through the shift paths had to be effected. Similarly, in order to do a right shift of less than 12 two passes had to be made.

These delays are completely dependent on shift length. For shifts that require greater than 13 delays the first pass always is one with 13 delays and the second pass adds the required additional delays.

SOLOMON PEs also have the capability to perform double length shifts both algebraic and logical with P being the most significant and Q the least significant portion of the word.

2.2.3 Network Control Unit Design

The network control unit (NCU) is functionally the same unit described in the AF report. This section will be restricted to supplying more detail concerning the interface and how the NCU functions as a system component.

The NCU and the network are designed to operate concurrently. This feature allows housekeeping required for the network program to be overlapped with execution in the network.

The NSU buffers two instructions to allow the network to operate at maximum rate. Lookahead is required because of the dynamic register in the PEs. At the completion of an instruction, the NSU must have the signal lines for the next instruction high before the end of the switching blank in the PE delay-line registers. If this condition is not met, a complete network cycle is lost, which could approach a 50 percent reduction in performance.

Because of the concurrency between the NCU and NSU and the two instruction buffers in the NSU, all data transferred over the NCU-to-NSU interface must be interlocked to assure that the sequence of the program is not changed. The following description will define the interface.

The network instruction set contains options that allow overflow, the existence of an active PE, and the existence of more than one active PE in the network to be detected. The NCU instruction set contains conditional branch instructions that use these indicators to determine if the branch is to be executed. For the NCU to execute one of these branch instructions, the NSU busy signal must not be present. The broadcast register, geometric row register, and the geometric column register are programmable registers that are loaded from PRM or stored into PRM by the NCU. For the NCU to execute these transfers, the NSU busy signal must not be present.

The transfer of data between the LB and the PRM is controlled by the NCU. The transfer between the LB and the network is controlled by the NSU. To maintain the program sequence, the NCU must know if the NSU is executing or has buffered an LB transfer instruction. The NCU contains a two-stage up-and-down counter which is stepped up each time an LB-network

instruction is sent to the NSU and stepped down each time the NSU completes an LB-network transfer. The NCU will execute an LB-PRM transfer only if the count is zero.

2.2.3.1 Program Memory Interface

In the system configuration proposed, the contents of the PRM are accessed by the NCU and LB only. The NCU instruction word is 48 bits and the data word is 24 bits, corresponding to the NSU 48-bit instruction word and the network 24-bit data word. The path between the NCU and the PRM is 48 bits. The path between the LB and the PRM is 96 bits. The number of bits accessed per memory cycle is 192. The 48-bit instruction formats were selected to allow the PRM to be expanded if desired and the data word from PRM to be a multiple of the 24-bit network data word. The 96-bit path between the LB and the PRM allows data to be transferred between the network and PRM at nearly maximum rate that data can be transferred over the edge of a 32 x 32 PE network. In approximately 3 microseconds, 32 24-bit data words can be transferred between the LB and network. Between the LB and PRM, eight 24-bit words (192 bits) are transferred per memory cycle. Four 1-microsecond memory cycles will transfer 32 data words. A 96-bit path was selected for this communication rather than a 48-bit path to reduce the electrical design problem of the interface. In principle, sufficient time is available to load or read the memory register during the clear or restore portion of memory cycle, but the detailed design of the interface indicates that this implementation is not practical.

The PRM and the PEM are electrically and mechanically the same except for the interface. Both memories use identical electronics and packaging. The only difference is that the PRM accesses 192 bits per cycle and PEM accesses 256 bits. Four PEM's are packaged in the same enclosure for 128 PEs. The PE network is designed to be modular in blocks of 32, which requires the PEM enclosure to be modular. Physically, this memory arrangement allows the PRM to be expanded in increments of 16,000 (48-bit words) to 64,000, within the same physical unit.

The electrical design of the memory allows an additional degree of freedom in expanding the PRM. Additional memory banks can be added to the same interface electronics, or the memories can be independent units that are accessed concurrently. If memory banks are added to make a larger single memory, the hardware required for the digit direction of the memories is shared. Functionally, the memories are tied together at their preamplifiers. If additional memories are to operate independently, a duplicate unit is added including the interface. A brief explanation of the details of the PRM interface will indicate how this is implemented.

Each unit connected to the PRM uses a driver at its interface that is capable of driving as many terminated transmission lines as there are independent memories. The unit decodes the high-order two bits of an address to specify which memory bank is being requested. At each memory bank a memory priority circuit selects the unit to be serviced and gates the address to the memory access circuitry and returns an acknowledgement to the unit. The low-order two bits of the address are decoded at the memory to select the proper 48-bit word. The design that is proposed allows four memories to be connected in this manner to two units. This selection was made to correspond to the estimate of the requirements of an expanded system in the near future. Electrically the interface can be expanded to eight with the same set of drivers. This is the same driver developed for distributing the NSU signals to the network. The number of gates that are practical to package in the interface and the cost of these gates are the limiting factors. The detailed layout of the interface cards has not been attempted, therefore the freedom in expanding the interface, by leaving space for additional cards, beyond the present design cannot be stated.

2.2.3.2 Priority Interrupt

The design of the priority interrupt system has been developed to minimize the complexity of the hardware in the NCU and to allow maximum program control. The current design allows interrupts from four sources to be serviced. Associated with each interrupt source are two memory cells that will be referred to as mail boxes (MB). One MB is used by the programmer

to store a jump instruction to enter the desired service routine, or a No-Op instruction to ignore the interrupt. The other MB, if required, is used by the interrupt source to store information to define the interrupt, if more than one condition can generate the interrupt. Each interrupt source connected to the NCU is assigned a priority determined by the position to which it is wired on the interface. A simple sample and hold network is used to strobe the interrupt lines and select the highest order interrupt. When interrupt is detected, the NCU generates an execute instruction with an address field corresponding to the programmed MB. The sampling network is stopped when an interrupt is recognized and an acknowledgement is returned to the source that is going to be serviced.

If the execute instruction receives No-Op instruction from the MB, the sampling network is released to scan the interrupt lines. If a jump instruction is obtained from the MB, the interrupt lines are not scanned until an unlock interrupt instruction is executed. A lock interrupt instruction that stops the scan of the interrupt lines is available to the programmer. The status of interrupt lines can be sampled under program control by reading the indicator register (IDR) of the NCU, but an acknowledgement to the interrupt source cannot be generated directly by the program. The interrupt unit will be packaged so that it can be expanded by adding additional interface and sample and hold stages.

2.2.3.3 General Purpose Computer or I-O Controller Interface

An input-output system to control peripheral devices is not included in the present SOLOMON II design, but a generalized interface has been designed into the NCU to allow an input-output system or a general purpose computer to be added. The selection of the interface that will be described is a result of an I-O controller designed earlier in the SOLOMON project and the desire to provide a flexible I-O interface for the current system without adding a large amount of hardware to the NCU.

The function of the I-O interface can be illustrated by considering an I-O controller having an independent interface with the PRM that receives

commands that define the function to be executed and the area of memory to be used. Associated with the I-O controller is an MB in the PRM that is used to transfer commands to the I-O controller. The programmer loads the MB with the command (the name command will be used only to refer to the contents of the I-O controller MB) and issues an alert instruction. The alert instruction will result in a signal line being raised to the I-O controller. The I-O controller obtains the MB, and returns a signal to release the NCU. Command completion signals are returned via the priority interrupt system. The second MB associated with the priority system would be used to identify the command completed in a multichannel I-O controller. Afield of the alert instruction is coded to identify the alert line if more than one independent unit is connected to the PRM.

Connecting a commercially available general purpose computer directly to the PRM in this manner cannot be similarly generalized because of the variety of machines that could possibly be used and the lack of specification of a particular machine and detailed information concerning the memory interfaces, interrupt systems, and circuits.

2.2.4 Network Sequencing Unit

The function of the NSU in the proposed system is identical to that previously described. The purpose of the NSU has been outlined in the general description of SOLOMON II in paragraph 2.1 of this proposal.

2.2.4.1 Network Control

The PE network is made up of a matrix of bit-serial arithmetic units with a minimum of control within the PE (detailed description of PE in paragraph 2.2.2). The only control that is unique to the PE is the execute control. If the execute control is not present, the PE ignores the current instruction. The execute control is set by comparing the decoded value of two mode value bits in the PE with four-mode control signals from the NSU. If any bit position agrees within the PE, execute control is set and the PE is said to be active. The mode value (MV) in the active PE, can be unconditional set or conditional

set by the NSU. Overflow options and compare instructions are used to conditional set the MV. The execute control of the PE is also conditional on the state of two other NSU controls, geometric row and geometric column controls, which were previously described. Both of these signals must be high for the PE to be active.

2.2.4.2 Signal Distribution

The signal drive between the NSU and the network has been designed to allow the network to be expanded from 32 PEs to 1024 PEs. The packaging is designed to expand the network in increments of 64 PEs to 1024 PEs (paragraph 2.5). A PE consists of four unique cards. In the PE door, 64 PEs are laid out in eight rows. Within a row, the PE card types are identical, which allows the NSU signals specifically required for a given row to be contained in that row. Each NSU signal required in a row has a driver located at the center of the row that is capable of driving 32 loads. The distance from the driver to any PE is less than 18 inches. The input to the row drivers is supplied by a set of flip-flops at the bottom of the PE door. A clocked flip-flop is used at this point in the NSU drive pyramid to retime the signals and to allow transformer coupling between the NSU and the PE door. In the NSU the signals are input to a clock driver that has an adjustable time delay. The output of the clock driver is three transformers that are capable of driving 8 terminated lines each. One terminated line supplies a control signal for a door of 64 PEs (figure 2-13). As additional doors of PEs are added, the signal drive lines are connected to the output transformers in the NSU.

2.2.5 PE Network Design

The design improvements and refinements in the PEs themselves have been previously described in paragraph 2.2 of this proposal. The arrangement of these PEs into a simultaneously operating network and the interfaces of the PEs to the rest of the system present some unique control requirements. These requirements, where differences exist from the basic earlier SOLOMON II design, are presented in the following paragraphs.

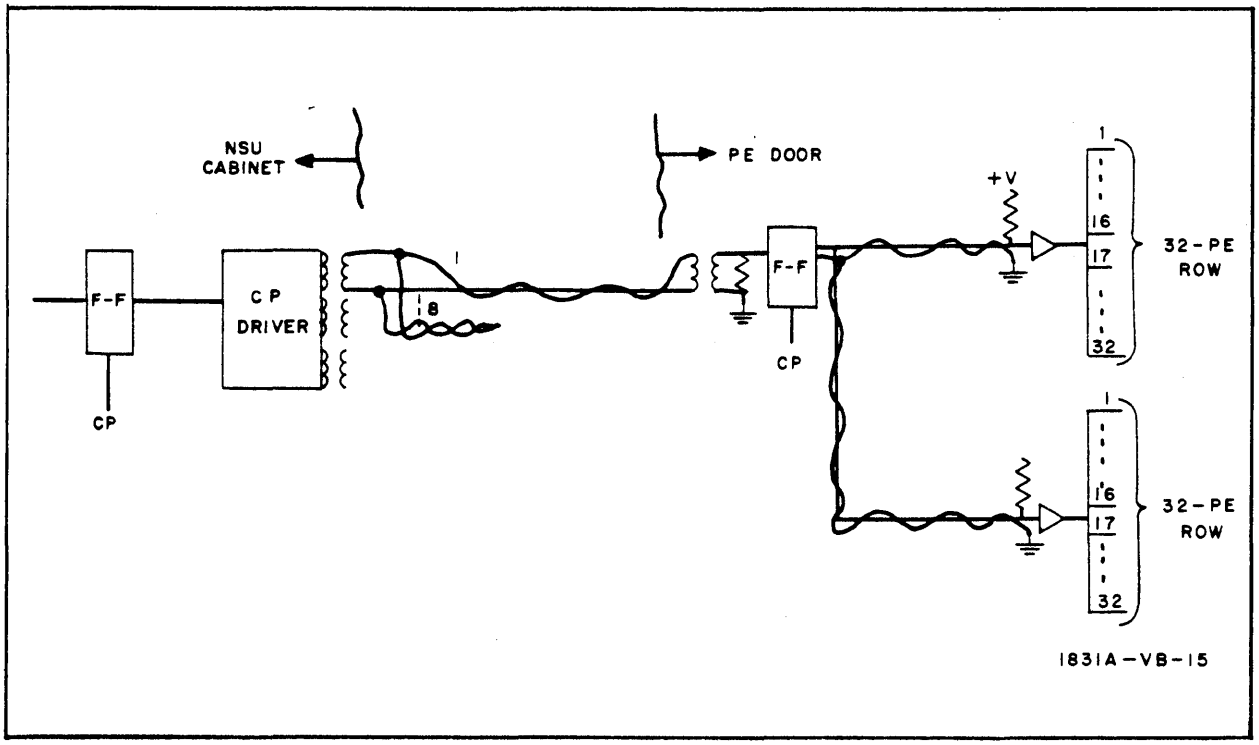


Figure 2-13. PE Network Signal Distribution

2.2.5.1 PE Data Interfaces

Data are transferred bit serial as 24-bit words between the two PE delay-line registers and the PEM, the LB, or the broadcast register. All data path connections are controlled by the NSU and are the same for all PEs.

The PEM is physcially made up of linear select core banks that contain 10^6 bits and can access 256 bits per memory cycle. Each bank is connected to a 32-PE module via an eight-bit shift register (figure 2-2). The shift register allows a 1-microsecond memory to transfer data continuously at an 8-mc bit-serial rate.

Data is transferred between the LB and the network by rows or columns. When writing into the network all active PEs in the same row or column receive the same operand. When reading from the network, the output of all active PEs in a selected row or column are sent to the LB.

The broadcast register is a data source or sink that is common to all active PEs. To write into the network the BR is gated to each of the LB-row

lines. To read, the LB-row lines are all "ORed" at the input of the broadcast register.

2.2.5.2 Indicators

The status of the network can be sampled by testing for overflow or active. Overflow check on arithmetic (paragraph 2.2.2.2) instructions is a programming option that can be used to set an indicator if any active PE overflows. The test for active (paragraph 2.2.4.1) sets one indicator if more than one PE is active and another indicator if only one PE is active.

To test overflow, the overflow flip-flop in each PE is gated to the line used to collect data by rows and the OR gates for loading the broadcast register from the network are opened. If a one is detected, an indicator is set.

To test the active status of the network, the execute flip-flop of the PE's are gated to the lines that collect data by rows and the lines that collect data by columns. The collection lines are gated to a shift register that is used to detect the presence of one or more than one bit set. If more than one bit is detected in either register, only the more than one indicator is set. If only one is detected in either of the registers, the one indicator is set.

A programming option is also available that allows the Execute FF's to be loaded into the Geometric Row and Geometric Col. Register. The same set of lines are used that are necessary to collect the Execute FF's. Both of the Geometric Control registers are programmable.

2.2.6 Console

The console that is proposed is a combination operator's and maintenance console. The ability to load NCU registers, read-write the PRM, to read PEM, and to read PE registers are aids designed to reduce time required to isolate failures. The console typewriter and the PE Mode Value display make up the major portion of the console hardware associated with normal operation.

2.2.6.1 Console Typewriter

The console typewriter is connected to the NCU by a six-bit data path. Input from the typewriter is controlled by the operator. The starting

location is set on the console switch and ENTER TYPEWRITER pushbutton is depressed to initiate a transfer. The characters typed are assembled into 48-bit words by the NCU and are loaded into contiguous memory locations until END OF TRANSFER is depressed by the operator. End of transfer will cause the last group of characters assembled to be loaded into the next memory location. Output to the typewriter is under program control. One 48-bit word is output each time the output instruction is executed.

The PRM can also be loaded from the console by setting the location and the value on a set of console switches and depressing the LOAD MEMORY switch.

2.2.6.2 Single-Step Control

The single-step control is designed to allow the program to be stepped one instruction at a time or one minor cycle of the instruction at a time.

2.2.6.3 Halt Control

A set of halt conditions that can be selected at the console has been provided as a maintenance aid. The NCU can be stopped by the following conditions:

a. Stop if a bit of the NCU's IDR matches its corresponding console switch.

b. Stop when the IC equals the value set in the console switches.

The stop conditions can also be used to generate a branch to a location specified by a set of console switches. This feature allows the operator to cycle on a selected segment of a program when isolating failures.

2.2.6.4 Start Controls

Two basic controls from the console are used to start a program. If the machine has been cleared, initiate is used to set the NCU IC from console switches. If the machine was stopped by a halt instruction or from the console, start is used to initiate the program.

Depressing MASTER CLEAR switch at the console clears all NCU and NSU register and controls. MASTER CLEAR is interlocked with halt, such that it has no effect if the machine is operating.

2.2.6.5 Displays

A complete list of the control to be displayed has not been finalized. The following description will outline the major displays.

The following NCU registers will be displayed:

a. Memory data register (48 bits)
b. Memory address register
c. Instruction register
d. Instruction counter
e. Indicator register
f. Arithmetic registers
g. Selected flip-flops in timing control

The following NSU registers will be displayed:

a. Instruction buffer
b. Broadcast register
c. Geometric control registers
d. Memory address register
e. Selected flip-flops in timing control

Two 32-position rotary switches will be provided to allow one-bit position of the geometric row and the geometric column controls to be selected from the console for displaying the contents of the PE register or the contents of a PRM word or the contents of an LB location. The rotary switches are interlocked with halt. To display a network register, the operator depresses the control corresponding to the register desired and the NSU initiates a timing cycle that gates the contents of the register through the network-broadcast register path to a display register in the NSU. If a word of PRM is desired, the address is set on console switches and the procedure for reading a register is followed. The state of the network is not changed by generating the displays mentioned.

The mode value flip-flops in the PE will be connected directly to console lamps for display. This display will physically be laid out in the same matrix notation manner that the network is labeled.

2.3 MEMORY SYSTEM

The memory system selected for SOLOMON II serves the purpose of both the PEM and PRM as previously defined. Since the AF report was published, certain test programs have verified the selection of the memory system. These tests and their results are briefly described in the following paragraphs.

2.3.1 1-Microsecond Memory Breadboard

Four planes of 30-18 mil cores built by Lockheed Electronics Co. were obtained for test. Each plane consisted of a 32 x 10 section of cores fully wired with loose cores on each line to increase the size to 128 x 64. A 4-wire system was used for each plane. The planes were interconnected so that the read-write lines were 256 cores long. Thus 2 planes formed 32 words of 256 bits each.

2.3.1.1 Test Circuits

The drive system consisted of 12-current drivers; a 12-input LSM transformer, a drive-line selection transformer, and a transistor switch. The switch had a 68-ohm terminating resistor in its collector.

The sense amplifier consisted of 2-differential pairs in series, transformer coupled to a rectifying and output stage.

The digit driver consisted of a voltage switch transformer coupled from a driving stroke gate.

2.3.1.2 Test Results

A 400-milliampere pulse 250-nanoseconds wide was used to interrogate the word lines. Rise and fall times of the pulse was 75-100 nanoseconds. With a full-write pulse so that all 256 cores switched the back-voltage developed by the cores was about 13 volts.

A 180-milliampere one-half write pulse, 400-nanoseconds wide, in conjunction with a 100-milliampere 325-nanoseconds wide digit pulse caused the core to switch to a "1" state.

The digit lines on one of the extra planes were interconnected so that a digit line of 32 x 64 cores or 2048 cores was formed. A sense line parallel to the digit line was also interconnected but in a manner so as to cancel

digit noise. The digit and sense lines thus consisted of 2048 cores plus one plane of 64 cores or a total of 2112 cores.

The noise cancellation achieved was very good. The signal-to-noise ratio was also good.

2.3.1.3 Conclusion

The conclusion from the tests was that all circuits functioned well and that no additional information could be obtained without the use of a full-size stack, since all tests with the small stack were favorable and no problems were encountered in the system design.

It is of interest to note that the existing coincident current memory for the Westinghouse 2402 computer uses access circuitry along one axis similar to that required in the 1-microsecond linear select system. In fact, the only difference other than amplitude of currents, was that the 2402 system requires 128-drive line outputs while the 1-microsecond linear select system requires only 64 outputs. The checkout of the 2402 access circuitry has been completed and its performance is quite satisfactory. The drive system is capable of providing a 350-milliampere current pulse into a core line of 3300 cores terminated in 100 ohms in 40 nanoseconds.

2.3.2 Molecular Sense Amplifiers

The basic package of the molecular sense amplifier consists of 3, 14-lead flat packs built by Texas Instruments to Westinghouse specifications. The molecular sense amplifiers have met or exceeded all specifications. The bandpass of the devices is 5.5-6 mc normally limited in circuit by a transformer. The delay through the molecular sense amplifier is 60 nanoseconds. Common mode rejection appeared to be very good - no detectable offset using Tektronix 545 scope with a 2.0-volt common mode input.

2.4 POWER SYSTEM

In view of the high currents being required at low voltages, all practical power distribution systems involve distributing an ac voltage, either 60 cycles, 400 cycles, or higher frequency, to power supplies located in the various major computing modules.

The choice of primary power to be distributed to the modules depends largely upon the use to which the computer installation is to be directed, and the quality of the primary power that is available at the computer location.

The use to which a computer is directed determines to a large extent how many computer interruptions can be economically or practically tolerated, resulting from power line disturbances. The quality of the power refers to how closely it is regulated, maximum fluctuations, and the duration of the fluctuations. Fluctuations expected range from minor disturbances resulting from switching loads, more serious line variations resulting from heavy load changes on a poorly regulated line to complete line outages lasting from several milliseconds to several hours.

A wide variety of requirements can be met by variations on a basic system where the incoming power is preregulated or improved in quality to a point where the regulators installed in the various computing modules can be quite economically fabricated. In the process of preregulating the power it is advantageous to change the frequency to higher than 60 cycles so that the components in the module power supplies can be smaller, lighter, more efficient, and more economical. In this type system the design of the power supplies in the individual computing modules remains fixed while the preregulator is modified to fit varying requirements.

In the design of past proposed SOLOMON systems, several divisions of Westinghouse, the Lima Division and the Buffalo Division, have participated in the design of power systems to meet the requirements for several different SOLOMON applications. Several outside vendors have also been contacted.

In general the more adverse the requirements, the more complex the system becomes. Systems considered include the following types of regulating systems.

a. No preregulator - module power supply uses raw 60 cycles

b. Brushless rotating frequency changer - with and without flywheel storage preregulator followed by 400 cycle or 2000 cycle input modular power supplies.

c. Constant-voltage transformer-rectifier battery charger and battery with:

(1) dc-to-dc module converters

(2) dc-to-400 or 2000 cycle frequency changers with module regulated power supplies

d. Same as c above with standby diesel engine generator sets.

All systems except c(1) and (a) use the same regulator module in the computer module. The regulator of (a) is of similar nature but must operate over a wider range of input voltages and the components are larger in the rectifier section due to the use of 60 cycles. When the input voltage quality is not good and the system is large, the supply described in (b) becomes the more practical. Systems (c) and (d) are for use where line interruptions are expected but operation interruption is not allowable.

The physical size of a type (b) final regulator used to supply the following power to one door containing 64 PE elements is:

+6 v at 114 amps

+9 at 32 amps

-1.5 at 3 amps

Since the regulation of the high-frequency ac power is good, the power supplies contained in the memory and any auxiliary equipment can be correspondingly small and efficient.

Due to the large number of components and dense packaging the distribution of power has received serious attention. Initial designs indicate that 114 amperes of 6-volts dc power per PE door will be required. With currents

of this magnitude, it requires a conductor of 0.216 square-inch to carry the current with a voltage drop of 10 millivolts per foot.

Since this is a reasonable sized cross section of copper, it is not practical to transmit this over a considerable distance from central power sources. This size conductor yields a 1 percent dc drop for each 6-feet of length.

To maintain the noise on the dc voltage buses within a tolerable level, 3 percent, it is necessary that the characteristic impedance of the bus lines be kept low. Since the characteristic impedance, Z, of a cable is given by:

$$Z = \sqrt{L/C}$$

it is desirable to reduce L. This is obtained by keeping the conductor close to the ground return bus, in this application there is to be 5 mils separation. To further reduce the inductance, the 6 volt bus is laminated; i.e., two strips are paralleled and sandwiched between a ground plane on the main bus inside the cabinet. On the main bus inside the cabinet, capacitors are distributed along the bus to get the impedance sufficiently low, the amount required being approximately 180-microfarad per foot for a bus of the configuration of figure 2-13A.

The most serious problem occurs with the +6 volts, since it is required to have the lowest impedance. The +9 volts requires but 0.92-microfarad per foot and will be an outside conductor having a ground only on one side. The -1.5 volts bus will be identical to the +9 volts.

Figure 2-13A indicates the cross sectional view of the main bus in the door. Similar designs will be used for the branch bus; however, only one conductor will be used for the +6 volts and the dimensions will be smaller.

2.5 PACKAGING

The detailed design of the cabinets has not been completed. An analysis of the signal distribution problem and card count has established the geometry and space requirement. All analysis was made assuming a 1024 network was to be packaged in modules of 64 PEs. The system is modular in increments as small as 32 PEs but the analysis of the packaging indicates that it is more practical to package in modules of 64 PEs.

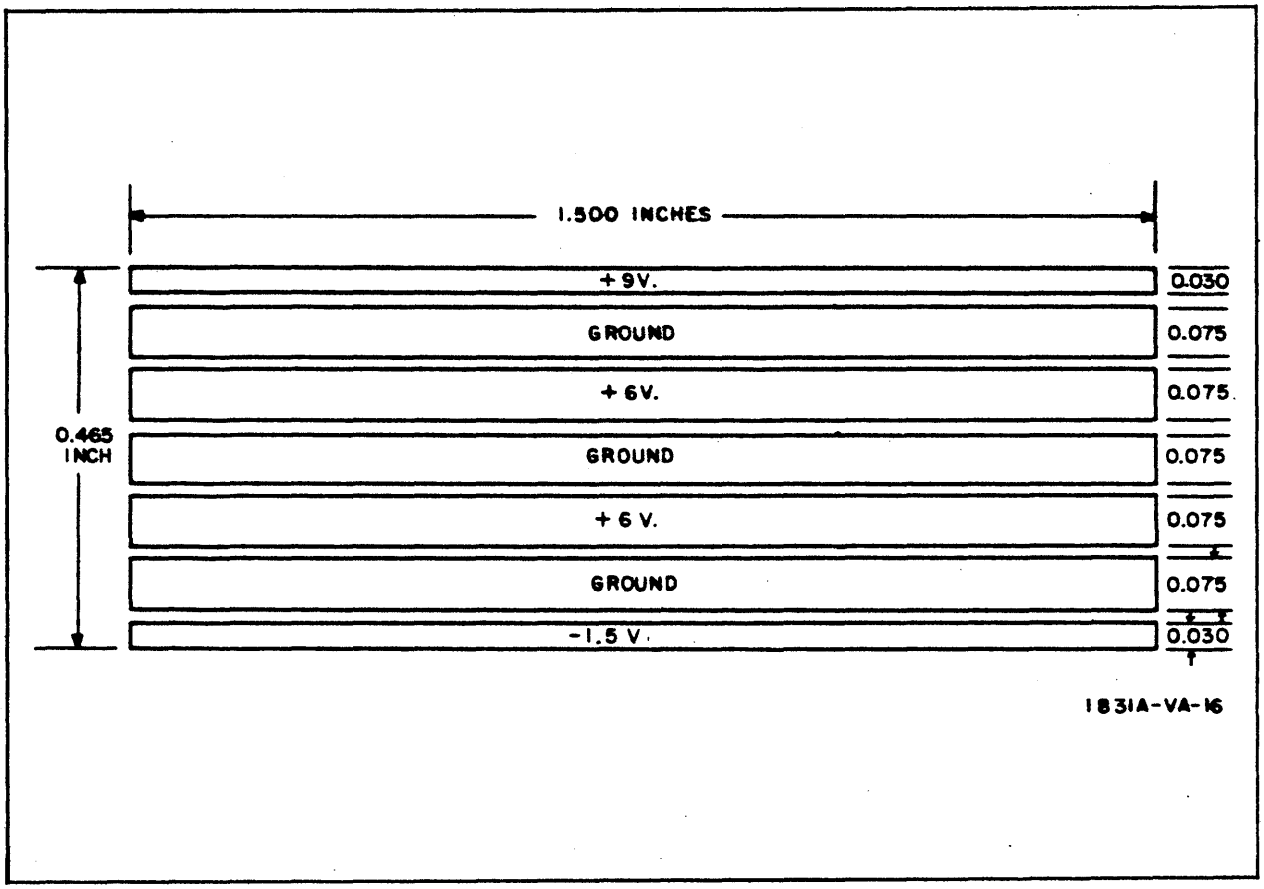


Figure 2-13A. Main Power Bus End View

The distance between the PEM and PEs has the most influence on the gross geometry of a system larger than 256 PEs. Within a 256 network the physical size of the memories dictate the geometry of the enclosures. Four 256 x 4096 memories can be packaged in a 6-foot x 6-foot x 15-inch enclosure (figure 2-14). Because each memory services 32 PEs, the block of 128 PEs associated with the memory enclosure has been packaged in two doors that hinge at opposite ends of the memory enclosure (figure 2-15). Assuming four cards per PE and eight addition card spaces per 32 PE cards and 0.7-inch card centers, 64 PEs can be packaged in 8 rows, 28 inches long. The door will be larger than this to allow for cabling and cabinet structure. A practical dimension for the door appears to be 3 foot x 5 foot x 8 inches. The dimensions of the memory enclosure will be longer than 6 feet to allow for power supplies and

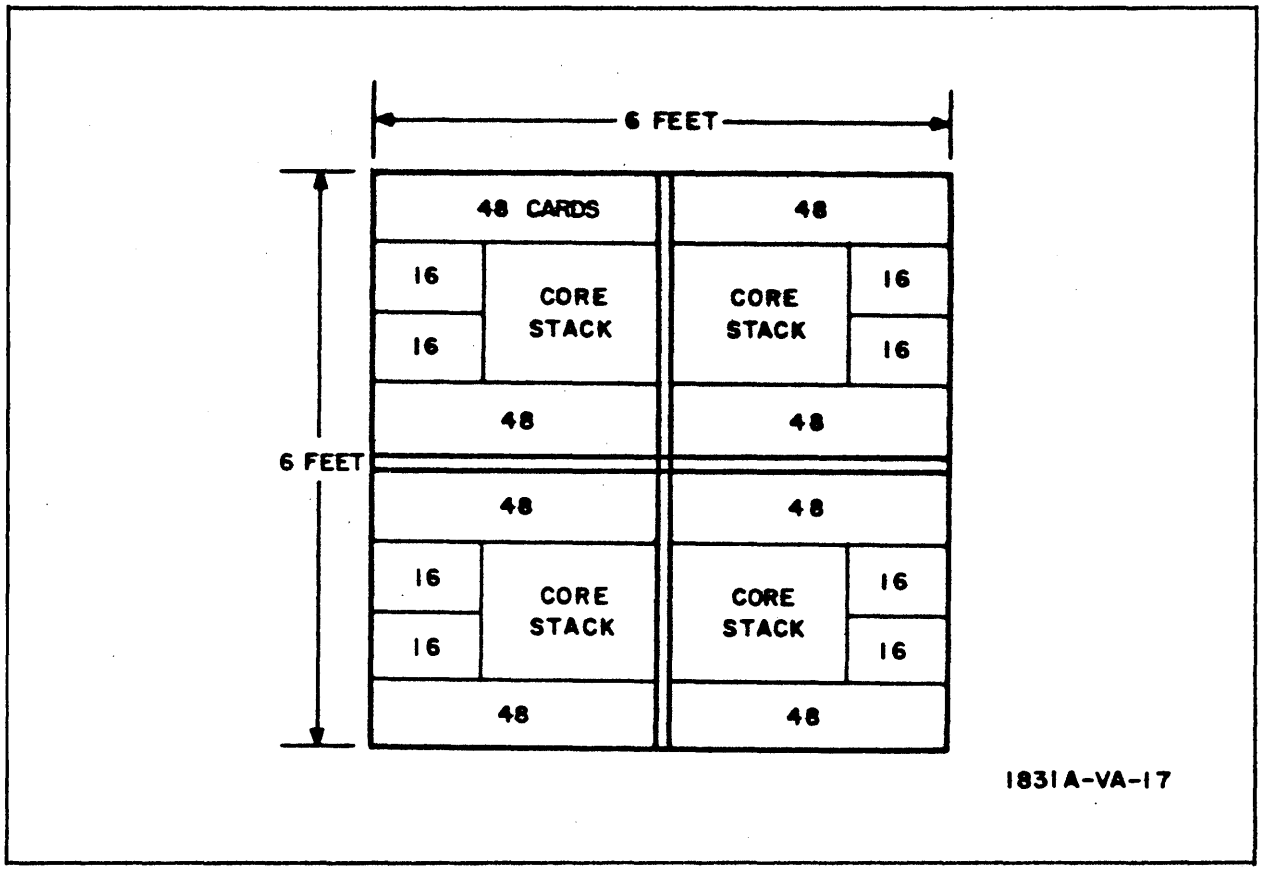


Figure 2-14. Packaging Arrangement

cabling. The power supplies that supply power for the PE doors will be mounted at the edge of the memory enclosure to minimize bus length between the supplies and the load.

A 256-PE network consist of two 128-PE enclosures in line to form a wing approximately 16-feet long. A 1024-PE network consist of four wings positioned as a cross with a 4-foot open center section (figure 2-16).

The cross configuration was selected to assure that no routing line in the sytem would exceed 40 feet and that all cabinets were easily accessible for maintenance. In figure 2-17 the wings have been labeled Q_1 through Q_4 and the routing paths illustrated. All lines between adjacent wings will run diagonally under the floor. Note that there are no routing lines between Q_1 and Q_3 or Q_2 and Q_4. The maximum line length is between the ends of adjacent wings.

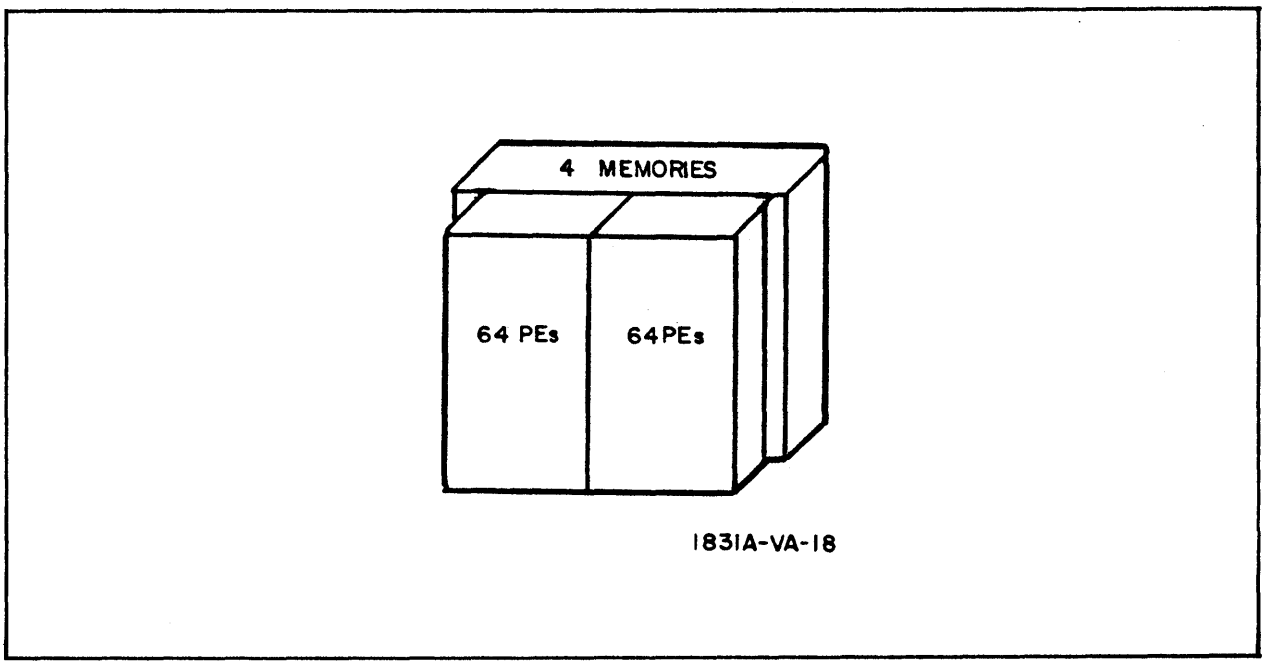


Figure 2-15. Cabinet Arrangement

2.6 RELIABILITY

The SOLOMON II computer system reliability is ensured through the use of silicon integrated circuits at low power levels for logic gates, flip-flops, and memory sense amplifiers, and through the extensive derating of components in the discrete component circuits used as memory drivers and in peripheral and auxiliary electronics. The expected level of reliability for SOLOMON II is shown in tables 2-5 and 2-6, which are mean time between failure (MTBF) figures for 32 PE and for 256 PE SOLOMON II computers respectively. The usual assumption of Poisson distribution of failures is made, i.e.,

$$R = e^{-\lambda(t-t_o)}$$

where

R = reliability = probability, given that the system is operating at time t_o, that the system is operating at time t.

λ = system failure rate in failures/unit time.

e = base of natural logarithms.

Since failures are assumed independent of time, as a result they are assumed independent of each other. Thus the formula equates any single failure to

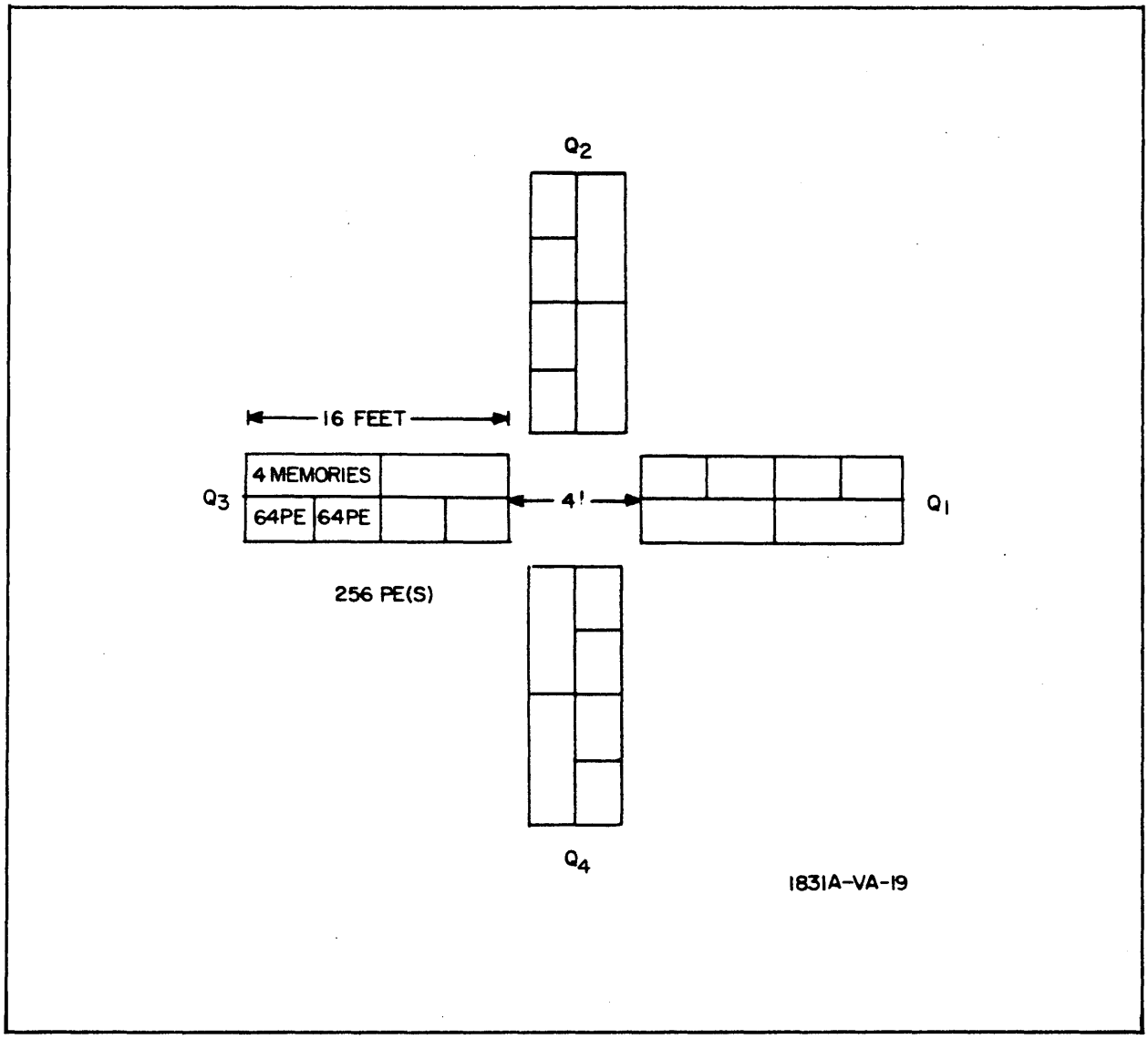


Figure 2-16. System Layout

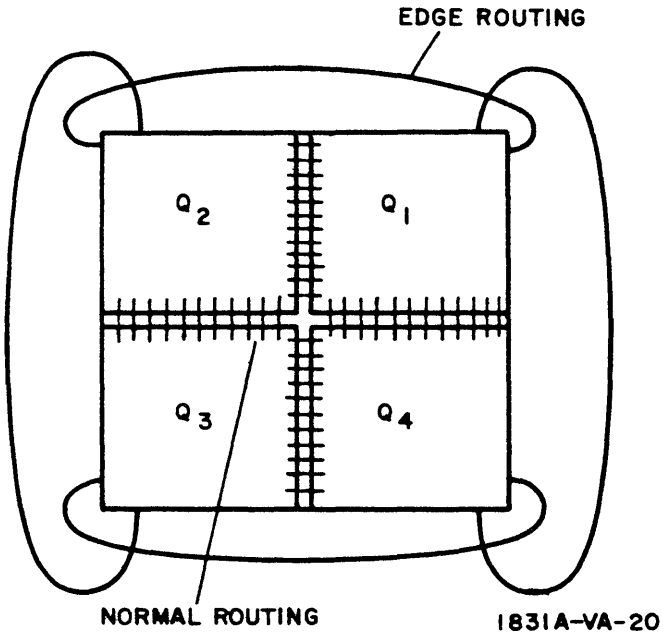


Figure 2-17. Routing Paths

system failure. It should be noted that, due to the SOLOMON II organization, this definition of system failure results in a conservative reliability estimate.

TABLE 2-5

32 PE SOLOMON II RELIABILITY

Component	Quantity	Failure Rate %/1000 hr	Aggregate Failure Rate %/1000 hr
Integrated Circuit (TO-5 can)	25,445	0.001	25.45
Transistor	3,374	0.001	3.37
Diode	26,047	0.0004	10.43
Resistor	5,947	0.0004	2.38
Capacitor	3,163	0.001	3.16
Transformer	1,252	0.001	1.25
Solder Connection	540,000	0.0001	54.00
System Failure Rate			100.04 ≈ 100%/1000 hr
System MTBF			1000 hr

TABLE 2-6

256 PE SOLOMON II RELIABILITY

Component	Quantity	Failure Rate %/1000 hr	Aggregate Failure Rate %/1000 hrs
Integrated Circuit (TO-5 can)	72,399	0.001	72.40
Transistor	11,404	0.001	11.40
Diode	103,017	0.0004	41.20
Resistor	15,369	0.0004	6.15
Capacitor	12,624	0.001	12.62
Transformer	5,634	0.001	5.63
Solder Connection	1,043,000	0.0001	104.30
System Failure Rate			253.70 ≈ 254%/1000 hr
Ststem MTBF			394 hr

It is readily shown that with the assumed failure distribution the system MTBF is the reciprocal of the system failure rate, which in turn is the sum of the component failure rates. The MTBF figures of 1000 hours for the 32-PE system and of 394 hours for the 256-PE system represent the high level of reliability which can be expected when the SOLOMON II computer is implemented with silicon integrated circuits and discrete components which are of uniformly high quality. For this level of reliability, these components must be selected and applied through a high reliability program which follows the machine from parts vendor selection to acceptance of the machine by the customer.

2.7 SOFTWARE

2.7.1 Scope of Work

It is Westinghouse's understanding that L. R. L. plans to develop their own software system for SOLOMON but would welcome cooperation by the manufacturer. Westinghouse desires to cooperate with L. R. L. in the software development and will provide experienced professional personnel for this effort. The combination of L. R. L. s extensive software experience and Westinghouse's detailed knowledge of the SOLOMON System and previous software experience on parallel processors should provide a software package of the highest utility. As part of the SOLOMON project Westinghouse will produce a SOLOMON simulator, a functional assembly system, and diagnostic programs. These programs are necessary to ensure the smooth checkout of the SOLOMON system. The diagnostic programs will be delivered with the system to aid in system maintenance. The simulator and functional assembly system will be available early in the schedule and will provide the flexibility needed to write and check the diagnostic programs. The functional assembly can be used to bootstrap the writing of the SOLOMON assembly system, and therefore, programs do not have to be written in the absolute form.

2.7.2 Diagnostic Programs

Diagnostic programs will be provided as part of the SOLOMON system. These programs, used as part of the maintenance routine, will provide a fast effective method of detecting and locating failures.

The personnel assigned to the diagnostics have had experience of working on diagnostics for the 3 x 3 Parallel Network Computer, the 10 x 10 Iterative Array Computer, and the Westinghouse 2402 Computer. As part of the effort to provide the best possible diagnostics, the logic designers of a unit will provide a specification to the diagnostic programmer on the best methods of checking the designer's unit. The logic designer and diagnostic programmer will form a team and both will benefit from the others work.

The diagnostic programmer will have available to him an assembly system and simulator. The assembly system will be available early in the program and thus provide the diagnostic programmer with ease of programming and the ability to make rapid changes in the program by reassemblying. The simulation program will provide the means of checking the diagnostic programs. It should be noted the programming of the diagnostic routines in assembly language will provide a second benefit of checking the assembly system and programming problems associated with a parallel processor.

2.7.3 Functional Assembly System

Prior to the availability of the SOLOMON system, considerable programming must be performed on the diagnostic programs and various checkout routines. The extent of programming necessitates an assembly system. The functional assembler will be written for an existing computer using its available software. The functional assembler will accept input programs written in SOLOMON assembly language and provide a listing and binary tape to be used as input to the simulator. Thus, the programmers can assemble and execute SOLOMON programs during the manufacturing phase. An obvious use of the functional assembler is the writing of a compiler or assembly system to run on SOLOMON.

The specification for the assembly system is contained in SOLOMON project Technical Memorandum No. 24, SOLOMON II Assembly System.

2.7.4 Simulation Program

Many programs should be written for SOLOMON prior to the availability of the hardware. Some of these are diagnostic programs, checkout routines, and the assembly program. If these can be debugged or at least tested

beforehand, the time required for initial system checkout can be reduced. The simulator will provide a method of debugging these programs in advance.

The characteristics of the simulator are:

a. Any rectangular network from 1 by 1 to any reasonable size can be simulated. The size will be variable at run time. However, large networks will cause large increase in running time since auxiliary storage will be required.

b. The PE memory size will be variable.

c. Snapshot dumps of various registers will be available by using appropriate control cards.

d. The simulator will accept programs directly from the functional simulator.

2.7.5 Documentation

Documentation will be provided for

a. the functional assembly system

b. the simulation program

c. machine reference manual

d. the diagnostic programs.

Preliminary manuals have been written for the assembly system and the machine reference manual. Revised manuals will be available to Lawrence Radiation Laboratory early in the program.

Final manuals provided with the system will be a machine reference manual and documentation for the diagnostic programs. Documentation will consist of manuals, program listing, flow charts, and instructions for running programs.

2.8 GROWTH POTENTIAL

The modularity of the SOLOMON Computer offers a unique growth potential. From the smallest basic system, 32 PEs in a 4 x 8 matrix, the array can be expanded to over a thousand merely by adding proper groups of existing modules.

As an example, the basic system includes 32 PEs in a 4 x 8 matrix, an 8-word L-buffer, and 8-bit geometric row register, a 4-bit geometric column register, the sequencer with drivers for 32 PEs, the network control unit, and a set of peripheral equipment.

This sytem can be expanded in the following ways.

The addition of a PE module of 32 PEs allows a customer to select the number required for most efficient solution of his particular problem. A single addition module, identical to the existing one, plus a memory module and 4-bit column geometric register increases the array to an 8 x 8 matrix.

The system can be expanded, if a problem requires more program memory, by an additional bank of 16,000 words. This expansion is presently limited to 48,000 words. A nearly identical memory module, differing only in interface hardware, can be connected into the system to expand the processing element memory.

Additional speed in I-O operations can be obtained by the addition of a larger L-buffer resulting in an increase in data flow rates into and out of the network. The second buffer will enable the program to load LB_1 and then start transferring data from this L-buffer, while the PE network simultaneously begins loading LB_2 from the program memory to have it ready at the completion of the unloading of LB_1.

Note that this is but a few of the basic configurations which can be built from the basic system modules. This flexibility is an important asset to the SOLOMON system.

3. MANAGEMENT

3.1 SOLOMON EXPERIENCE

Westinghouse has 3-1/2 years of experience in the design, development, and construction of SOLOMON and SOLOMON-like computers to back up the proposed program. At the peak periods of activity as many as 50 professional engineers and mathematicians have been employed full-time on SOLOMON design, applications analyses, and software development. All key personnel of this well trained and highly motivated working force are available for the proposed program. The continuity of the project can be well illustrated by a summary of contractual efforts and company-sponsored efforts leading to the present status of design and knowledge of the machine and its uses.

3.1.1 SOLOMON Program Contracts

Westinghouse has received research and development contracts on SOLOMON and related techniques from the U.S. Air Force, U.S. Army, U.S. Navy, and N.A.S.A. These contractual efforts are summarized in the following paragraphs and in figure 3-1.

3.1.1.1 Contract AF30(602)2724

This contract constituted a major research and development program leading to the design and construction of a small hardware system, and extensive application analyses of the SOLOMON I System. In the program a complete machine design was made, including wiring diagrams, for a full-scale Parallel Network Computing System. An operational machine containing nine processing elements was constructed and has been operated since January 1963. This machine was constructed to demonstrate the logical and electrical feasibility of parallel network computation. In addition 12 separate application analyses for problems of various types drawn from the broad areas of commercial, scientific, and military data processing were performed under the contract. The contract effort began in March 1962 and

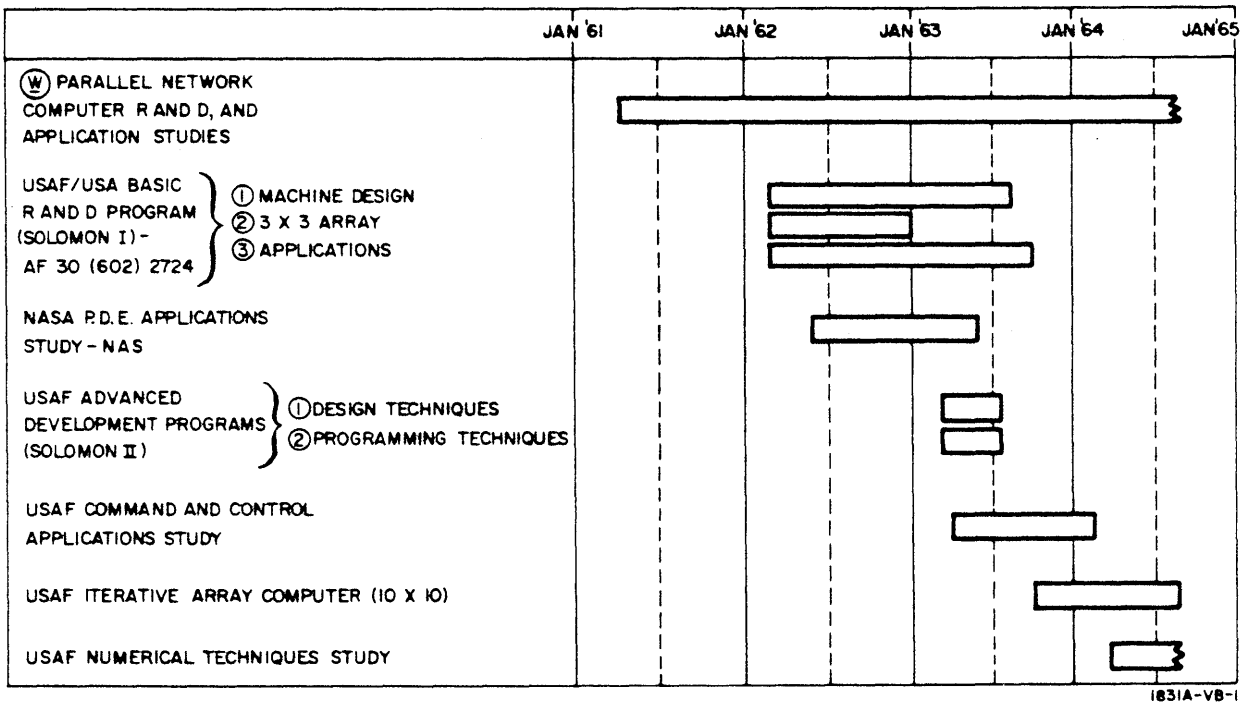


Figure 3-1. Westinghouse - SOLOMON Chronology

was completed in September 1963. Total contract funding was in excess of $400,000. The contract was sponsored by USAF/RADC with financial support from the U.S. Army Signal Corps Laboratories (now Army Electronic Command Research and Development Laboratories).

3.1.1.2 Contract NAS 5-2730

This contract, Numerical Solution of Partial Differential Equations on Parallel Digital Computers was sponsored by the National Aeronautics and Space Agency and was in effect from June 30, 1962 until June 30, 1963. The contract value was approximately $25,000 and represented one man year of effort in the development of techniques for solution of several classes of PDE's on SOLOMON.

3.1.1.3 Contract AF30(602)3417

This contract entitled Multiple Processing Techniques for a Parallel Network Computer resulted in the basic system design of the SOLOMON II machine described by LRL in the July 9, 1964 bidders conference at

Livermore, California. The study, sponsored by USAF/RADC, began in April 1963 and the final report was submitted on April 10, 1964. The final report on this contract has been frequently referenced in the technical portions of this proposal.

3.1.1.4 Contract AF30(602)3146

This study to develop programming techniques for a parallel network computer (SOLOMON) resulted in the assembly of system specifications and language definitions fundamental to the SOLOMON software package. This study which amounted to approximately $100,000 of engineering effort was initiated in April 1963.

3.1.1.5 Contract AF19(628)2846

The analysis performed in this study was oriented toward exploring the applications potential of SOLOMON in USAF Command and Control systems. Three major problem areas were analyzed in detail: communications systems control, information storage and retrieval, and radar data processing. The contract was funded for approximately $70,000 and was in effect from March 1963 until January 1964.

3.1.1.6 Contract AF30(602)3207

The Iterative Array Computer containing 100 PEs was built and delivered to RADC under this contract. The machine contains 3,500 integrated circuit packs identical to those specified for SOLOMON II and has thus served as the test bed for a majority of the SOLOMON II circuitry. In its own right the Iterative Array Computer is a significant computing system in that it is the first large scale parallel network computer. This development has already demonstrated that it will be the vehicle on which much parallel network software and programming reseach will be proven prior to the completion of the first SOLOMON II machine. This program was initiated in September 1963 and the machine was accepted in July 1964 by RADC.

3.1.1.7 Contract AF30(602)3313

This contract entitled Numerical Techniques for Advanced Computers is intended to develop the state of the art in numerical analysis to support

advanced machines such as SOLOMON II. Work began on this $75,000 one-year study in April 1964.

3.1.2 Internally Sponsored SOLOMON Studies

During the design and development of the SOLOMON concept numerous applications studies were performed under corporate sponsorship. The overall list of technical memoranda and project notes is included in this section. In a number of cases the basic research reported in the technical memoranda was to some extent supported by one of the previously mentioned contractual efforts. These memoranda are referenced with a preceding asterisk. It should be noted that numerous hardware studies and experiments leading to the present advanced state of design and development of SOLOMON II have been performed under internal sponsorship.

1. Programmed Multiply and Divide on the SOLOMON Computer (August 1962).
2. SOLOMON Flow Charting Conventions (September 1962).
3. SOLOMON Floating Point Add Subroutine (September 1962).
4. Input-Output Scheme Between the PE Matrix and the Buffer (October 1962).

*5. Simulation of a Communications System (December 1962).

6. Preliminary Signal Designation Format for Experimental Model SOLOMON Drawings.
7. Sorting Techniques on SOLOMON II (April 1963).

*8. Two Theorems and a SOLOMON Solution to a Problem in Nonlinear Threshold Logic (August 1962).

*9. The Use of the SOLOMON Computer for Photo Data Processing Functions (April 1963).

*10. Program Routine for Ephemeris Calculation (April 1963).

*11. Investigation of the Application of the SOLOMON Computer to Certain Linear Programming Problems (January 1963).

*12. A General Nerve Net Simulator (August 1962).

*13. A SOLOMON Program for Solving Systems of Simultaneous Linear Equations (August 1962).

*14. Preliminary Numerical Weather Application Study (June 1963).

15. Preliminary Study of the Reliability and Maintainability of the SOLOMON System (June 1963).

16. An Improved Sorting Routine for the PEs (August 1963).

17. Use of SOLOMON Computer Power Spectral Densities (August 1963).

*18. SOLOMON Assembler System (September 1963).

19. Simulation of a Communications System (Revised) (September 1963).

20. Several Approaches for Using a Bryant Series 4000 Disk as a Temporary Storage Device for the PE Network (October 1963).

*21. Inventory Control (November 1963).

22. Programming Considerations and Examples for SOLOMON II (November 1963).

23. SOLOMON II Reference Manual (November 1963).

24. SOLOMON II Assembly System (November 1963).

25. SOLOMON II Physical Characteristics (November 1963).

*26. The Use of the SOLOMON Computer for Photogrammetric Data Processing (November 1963).

27. Airborne SOLOMON ELINT Signal Processor (November 1963) (SECRET).

28. Satellite Threat Recognition System Feasibility Analysis (SECRET).

*29. SOLOMON II Designers Handbook (November 1963).

30. Study of Application of SOLOMON to a Large Matrix Type Simulation Problem Involving the Diffusion Equation (November 1963).

*31. The Use of SOLOMON for Data Base Analysis and Information Retrieval (December 1963).

32. Optional Table Look-up Feature for SOLOMON II (December 1963).

33. Consideration of SOLOMON for Manned Orbital Reconnaissance Laboratory (January 1964).

34. Study of the Application of the SOLOMON Computing Concept to a Multiplate, Phased, Reflecting Antenna for Use at Centimeter Wavelength (January 1964).

35. Ground Based Satellite Inspection System (January 1964) (SECRET).

36. Application of SOLOMON II to Advanced Sonar Systems (February 1964).

37. Floating Point and Double Precision Subroutines for SOLOMON II (January 1964).

38. Computation of Multiple Target Power Special Densities with a 1024 Processing Element SOLOMON II Computer (March 1964).
39. Mode Status Display for the SOLOMON Computer (March 1964).
40. Application of the SOLOMON Computer to Intelligence Data, Base Maintenance and Manipulation (February 1964).
41. Application of the SOLOMON Computer to the Simulation and Control of Large-Scale Communication Systems (April 1964).
42. The Application of SOLOMON II to Satellite Data Reduction and Analysis (April 1964).
43. Illustration of SOLOMON Application to Digitally Controlled, Phased-Array, Beam-Steering Computations (March 1964).
44. A General Survey of Past and Present Investigation into the Application Parallel Network Computation to Intelligence Data Processing Problems (March 1964).

3.2 PROJECT ORGANIZATION AND PERSONNEL

The SOLOMON II project will be staffed with personnel who represent a major portion of the over 100 man-years of Westinghouse experience on SOLOMON design and development.

The Project Manager with direct responsibility for the SOLOMON II Project is Mr. W.H. Leonard. Mr. Leonard has been associated full-time with the SOLOMON Program since December 1961 in sequential positions of direct line supervisor of the development program, manager of SOLOMON applications, and manager of advanced SOLOMON systems. Mr. Leonard reports directly to Dr. D. L. Slotnick, Manager of Data Management and Communications for the Aerospace Division of Westinghouse Defense and Space Center. Dr. Slotnick is the inventor of the SOLOMON concept and has been personally performing and directing research on parallel network computers since 1953.

The key technological personnel in the proposed development program are the technical directors of hardware and software development. These positions are staffed respectively by Mr. J. R. Hudson and Mr. A. B. Carroll. Mr. Hudson has performed the function of technical director of SOLOMON hardware for over a year and has led the team that developed the proposed SOLOMON II computing system since its inception. Mr. Carroll has been in the position of

technical director of SOLOMON I and later SOLOMON II software development for two years. He has organized and directed the diagnostic procedures, demonstration programs, and software development for the 3 x 3 SOLOMON I Array, the 10 x 10 Iterative Array Computer, and the proposed SOLOMON II system. Messers Hudson and Carroll will report directly to the Project Manager. The technical directors will receive consultation services and support in their specific technology areas as needed from the managers and staffs of the hardware development group under Mr. J. G. Gregory and the software development group under Mr. G. Shapiro. The personnel assigned directly to the SOLOMON II Project are listed in their respective technology areas in the organization chart presented as figure 3-2.

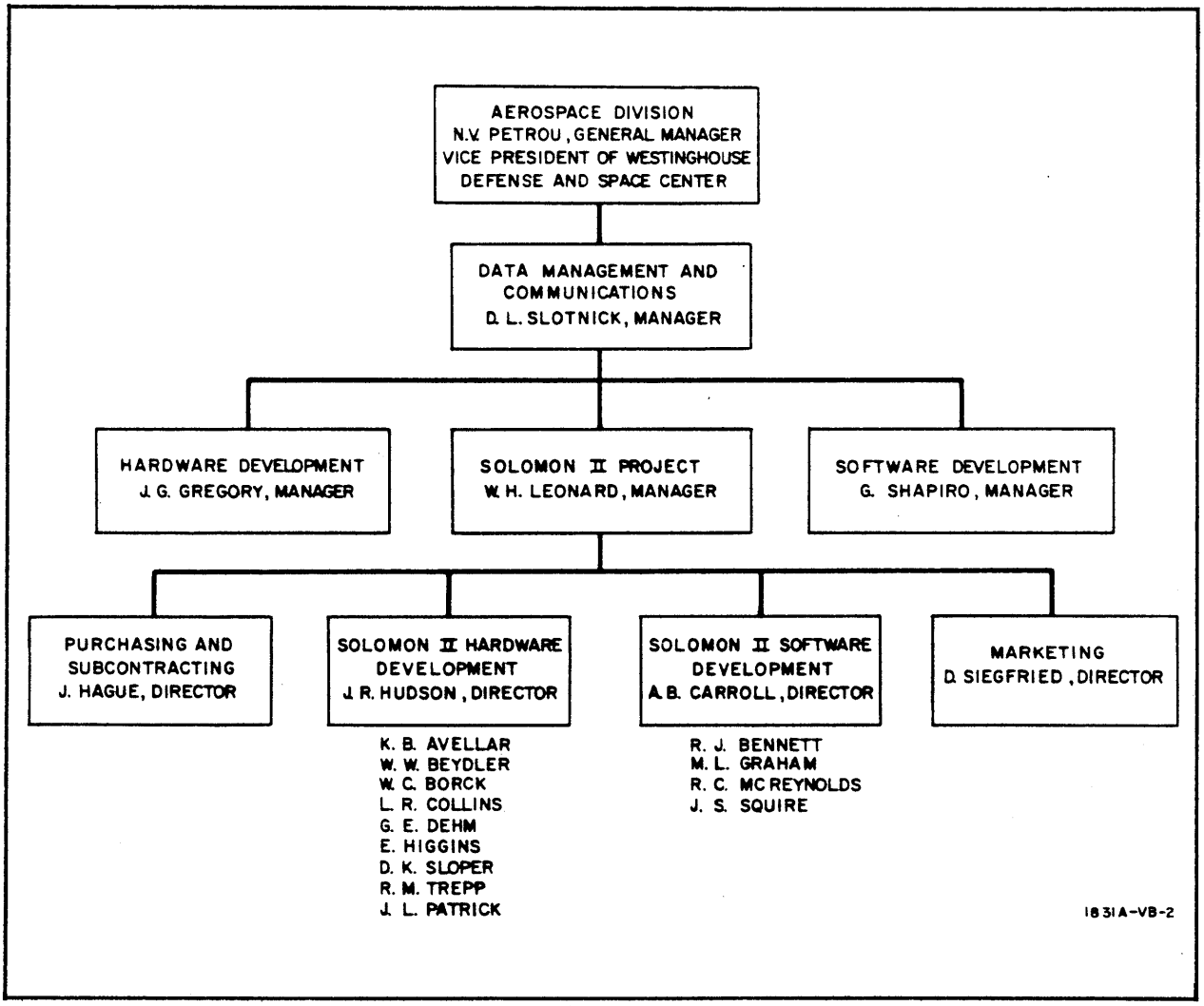


Figure 3-2. SOLOMON II Project Organization

Resumes of all proposed project personnel are included on the following pages. Other experienced SOLOMON personnel will be assigned to the project from the hardware and software development groups as the need arises.

All facilities and capabilities of the Westinghouse Defense and Space Center and the Aerospace Division will be available to the Project as required to ensure its successful completion.

NAME: Daniel L. Slotnick, Manager

EDUCATION: B. A., Columbia College, 1951
M. A., Columbia University, 1952
Ph. D., Applied Mathematics
New York University Institute of Mathematical Sciences, 1956

EXPERIENCE:

1951 - 1952	Columbia University, Department of Mathematics. Research Fellow. Research in the theory of games.
1952 - 1954	Institute for Advanced Study, Electronic Computer Project. Analyst. Analysis, programing, and logic design.
1954 - 1956	New York University Institute of Mathematical Sciences. Research Assistant. Research in celestial mechanics.
1956 - 1957	Princeton University, Nonlinear Mechanics Group. Research Assistant. Consultant in operations research. Research in nonlinear mechanics.
1957 - 1960	International Business Machines Corporation, Research and Advanced Systems Divisions. Advisory Engineer. Chief Engineer on communication-based data processing system for stock brokerage business. Design of scientific computer. Organization and operation of Analysis and Programing Department, Research Division, Scientific Computing Center.
1960 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland.
1960 - 1963	Manager. Control and computing systems, and advanced computing systems and digital techniques. Responsibilities included direction of research on Residue Class Computers as well as design and applications of the SOLOMON Computer.
1963 - 1964	Defense and Space Systems Operations. Responsible for all Computer and data processing work in the Westinghouse Defense and Space Center.
1964 - Present	Aerospace Division, Manager Data Management and communicator.

NAME:	Daniel L. Slotnick (Continued)
PATENTS:	39 disclosures and patents pending in field of digital computers.
PUBLICATIONS:	Ten articles published.
SOCIETIES:	American Mathematical Society Society for Industrial and Applied Mathematics Secretary, Baltimore Chapter Association for Computing Machinery Senior Member, Institute of Electrical and Electronics Engineers

NAME: Karl B. Avellar, Engineer

EDUCATION: B.S.E.E., George Washington University, 1960
M.S.E.E., University of Connecticut, 1963

EXPERIENCE:

1960 - 1962	Norden Division of United Aircraft Corporation, Norwolk, Connecticut. Associate Engineer. Test and development of stable platforms. Design and development of digital angle measuring equipment. System and logic design on FMQ5 weather data processor.
1962 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Associate Engineer. Logic design of SOLOMON computer breadboard. Engineer. System and logic design of SOLOMON computer, particularly in the design of SOLOMON central control.

NAME: William W. Beydler, Senior Engineer

EDUCATION: B.S.E.E., Missouri School of Mines, 1959

EXPERIENCE:

1955 - 1957	U.S. Army, Radar Operator.
1959 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland.
1959	Westinghouse Graduate Student Program.
1959 - 1960	Assistant Engineer, Avionics System Section. Checkout and required redesign of AN/APQ-81 Airborne Data Processor memories from individual circuit boards to complete system.
1960 - 1961	Associate Engineer, Avionics System Section. Checkout and bench test of AN/APQ-81 Data Processing system. Integration of the system with AN/APQ-81 Airborne pulse doppler radar and subsequent rooftop flight test program.
1961 - 1962	Engineer, Computing Systems Section. Responsible for operation and maintenance of AN/APQ-81 Data Processor during successful in-flight test program. FM ranging study for airborne pulse doppler radar including the data processor instruction programming in AN/APQ-81 languages.
1962 - Present	Advanced Data Processing Systems. Memory circuit design for SOLOMON breadboard and memory system checkout. Memory circuit and system design for SOLOMON I computer.

PATENTS: 3 disclosures

SOCIETIES: Institute of Electrical and Electronics Engineers

NAME: W. Carl Borck, Senior Engineer

EDUCATION: B. E. E., Rensselaer Polytechnic Institute, 1960
Graduate Studies in Psychology, Montclair State College

EXPERIENCE:

1960	Westinghouse Electric Corporation, Pittsburgh, Pennsylvania, Graduate Student Program. Assistant Engineer. Worked on automatic digital readout for Franklin Institute analog computer.
1960 - 1963	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Performed logical design of the arithmetic and control units for the family WEDISC computers. Engaged in system conception and techniques used in the Westinghouse microprogrammed computer. Participated in a study of the computer specifications for a series of infrared systems and in ASW applications. Aided in studies to improve computing systems reliability and maintainability. An originator of the logical organization of parallel network computing systems. Responsible for the logical design of a parallel network computing system and the conception of control techniques for increasing programming flexibility. Engaged in the study of applications of parallel network computers. Responsible for design, construction, and testing of the SOLOMON breadboard.
1963 - 1964	Project Engineer responsible for all places on Interative Array (10 x 10) under AF30(602)3207.

PATENTS: Five patents pending in the area of parallel network computers, and computing system
Numerous disclosures in logical and system design techniques

PUBLICATIONS: "Microprogramming Techniques," Paper presented at Digital Techniques Symposium, September 1961.

"Numerical Analysis Considerations for the SOLOMON Computer," coauthor, Proceedings of the Air Force Rome Air Development Center, Westinghouse Electric Corporation. Aerospace Division Workshop, Baltimore, Maryland, October 1962.

NAME:	W. Carl Borck, (Continued)
PUBLICATIONS: (Continued)	"The SOLOMON Computer," coauthor, Proceedings of the Eastern Joint Computer Conference, December 1962.
SOCIETIES:	Institute of Electrical and Electronics Engineers American Management Association American Museum of Natural History Westinghouse Digital Techniques

NAME: Arthur B. Carroll, Fellow Engineer

EDUCATION: B. S. E. E., Pennsylvania State University, 1958
M. S. E. E., University of Michigan, 1962

EXPERIENCE:

1951 - 1953	USAF. Military duties as radar operator and identification clerk.
1958 - 1961	International Business Machines Corporation, Federal Systems Division, Owego, New York. Participated in development and flight testing of experimental and engineering models of the B-70 BNMGS. Assisted in assembling and checking the first prototype digital computer for the Titan Ballistic Missile Guidance System. Responsible for providing diagnostic programs for the B-70 and B-70 Logic Simulation Program.
1961 - 1962	University of Michigan, Graduate Student. Had primary responsibility for maintaining the Michigan Instructional Computer and improving a digital computer (MIC) for laboratory use. Designed core memory system for the MIC breadboard.
1962 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Engineer, Computing Systems. Assisting in development of parallel organized computers for the SOLOMON concept and application studies associated with this program.

PATENTS: Three patent disclosures.

PUBLICATIONS: "The Logical Design of a Holland Machine," A. B. Carroll and W. T. Comfort, University of Michigan, Electrical Engineering Department Internal Report, June 1961.

"Michigan Instructional Computer Core Memory System," A. B. Carroll and R. L. Haken, University of Michigan, Electrical Engineering Department Internal Report, June 1962.

SOCIETIES: Institute of Electrical and Electronics Engineers
Association for Computing Machinery
Eta Kappa Nu

NAME: Loren R. Collins, Fellow Engineer

EDUCATION: B.S.E.E., Illinois Institute of Technology, 1950

EXPERIENCE:

1943 - 1944	U.S. Army Signal Corps. Radar Technician.
1944	U.S. Army Air Corps. Laboratory Technician.
1950 - 1951	University of Chicago, Chicago, Illinois. Electronic Engineer. Designed laboratory instruments for monitoring and control of experiments.
1951 - 1955	Argonne National Laboratory, Electronics Division, Argonne, Illinois. Electronic Engineer. Designed laboratory instruments for monitoring, counting, and control applications. Designed dc amplifiers, pulse amplifiers, counters, coincidence circuits, power supplies, and radiation monitors.
1955 - 1960	Argonne National Laboratory, Applied Mathematics Division, Argonne, Illinois. Electronic Engineer. Designed and checked out logic systems for George, a digital computer. Designed circuits and logic for input-output equipment for George.
1960 - Present	Westinghouse Electric Corporation.
1960 - 1962	New Products Laboratories, Pittsburgh, Pennsylvania. Senior Engineer. Logic design and check-out on Prodac-X. Study and logic design on a small process control computer.
1962 - Present	Aerospace Division, Baltimore, Maryland. Fellow Engineer. Computer Development Section. System and logic design for SOLOMON, including arithmetic unit and data channel design. Supervision of logic design for SOLOMON.

SOCIETIES: Institute of Electrical and Electronics Engineers

NAME: Gerold E. Dehm, Associate Engineer

EDUCATION: B.S.E.E., University of Florida, 1960

EXPERIENCE:

1957 - 1960	U.S. Navy Mine Defense Laboratory, Panama City, Florida (part time). Circuit designer on sonar and mine sweeping equipment.
1960 - 1961	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Engaged in development of high speed logic blocks including monostable and astable multivibrators, Schmitt trigger circuitry, and binary counter circuitry.
1961 - 1962	Engaged in system analysis and feasibility studies of B-70 defense system. Also engaged in development of analog applications to B-70 defense system.
	Feasibility study and preliminary design of Orbiting Astronomical Observatory and ground operational equipment of observatory.
1962 - Present	Logic designer and programmer for prototype model of Orbiting Astronomical Observatory Ground Operational Equipment. Assisted in system coordination and production of prototype model. Logical design for SOLOMON.

PATENTS: Analog High Duty Cycle Radar Detector
Electronic Countermeasures Radar Mode Detector

SOCIETIES: Institute of Electrical and Electronics Engineers

NAME: M. L. Graham, Engineer

EDUCATION: B.S. in Physics, Carnegie Institute of Technology, 1958
Westinghouse Design School, two semesters of graduate study in M.E. at University of Pittsburgh, 1959
Graduate study in mathematics, Aberdeen Proving Ground extension, University of Delaware, 1960-1961
Graduate study in mathematics, University of Maryland, 1962-1963
Numerical Methods for Nuclear Reactor Calculations, University of California, 1963

EXPERIENCE:

1958 - 1960	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Systems design and programming work on a special purpose, high speed airborne digital computer.
1960 - 1961	Ballistic Research Laboratories, Computing Laboratory, Aberdeen Proving Ground, as Lieutenant in the U.S. Army. Analysis and machine language programming of the ORDVAC and EDVAC digital computers for ballistic problems. Work on a general program to fit curves to data including extraneous points.
1962	Served as Maintenance Platoon Leader third echelon ordnance maintenance company in Germany.
1962 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Worked on development studies for a residue class arithmetic computer, including developing algorithms. Performed systems analysis and programming on the SOLOMON design. Work on a device to coordinate and control the simultaneous operation on an arbitrary collection of computers.

PATENTS: Seven patent disclosures, two on the residue class computer, three related to SOLOMON, one on a computer complex control device, and one on a internal control device for computers.

PUBLICATIONS: Several internal reports in the areas mentioned above

SOCIETIES: Association for Computing Machinery
Society of Industrial and Applied Mathematics

NAME: John G. Gregory, Manager

EDUCATION: B. E. E. E., The Johns Hopkins University, 1948

EXPERIENCE:

1948 - 1950	General Electric Company. Test Engineer. Field applications engineer.
1950 - 1952	U.S. Army
1952 - 1962	U.S. Army, Ballistics Research Laboratory. Chief of the Research and Development Section, Computer Research Branch, Aberdeen Proving Grounds, Maryland. Responsible for the development of EDVAC Floating Point Arithmetic Unit, EDVAC Magnetic Tape System. Design and development of BRLESC and BRLESC Off Line Converter, believed to be "the world's fastest operating computer, 1962."
1962 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Director of SOLOMON development.

HONORS: Member BRL Scientific Staff
U.S. Army - Sustained Superior Performance Award, 1960
U.S. Army - Special Act Commendation, 1962
Honorary Journalistic Fraternity

NAME: Edward R. Higgins, Fellow Engineer

EDUCATION: B.S.E.E., Purdue University, 1949

EXPERIENCE:

1945 - 1946	U.S. Navy. Instructor at an aircraft electronics technician school.
1949 - 1951	Public Service Company of Indiana. Power transmission line design engineer.
1951 - 1952	U.S. Navy. Aircraft Electronics Technician. Supervisor of electronics night check crew for AF2S and AF2W aircraft.
1952 - 1955	U.S. Naval Ordnance Plant, Indianapolis, Indiana. Developed and designed voltage reference unit, instrument-type magnetic amplifiers, and associated circuitry for the MK 16 AFCS. Systems engineer responsible for the overall operation of the MK 16 system.
1955 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Senior Engineer. Circuit design and development included the following: magnetic amplifier regulated ac and dc power supplies, overload proof transistor regulated supplies, magnetic amplifier gyro torque drivers, instrument modulators and demodulators, instrument magnetic summing amplifiers, photoelectric shaft to digital encoder drive and sense amplifiers, video amplifiers, complete access circuitry for core, drum, and thin film memory arrays, logic circuits, gates, flip-flops, single shots, etc; supervision of three engineers in developing all circuitry supplied by Westinghouse for the Solomon Breadboard, including complete access circuitry, for a 2-microsecond coincident current core memory, and a line of logic circuits.

PATENTS: "Voltage Regulator" and "Null Detector" U.S. Patents issued.

SOCIETIES: Institute of Electrical and Electronics Engineers

NAME:	William H. Leonard, Manager	
EDUCATION:	B. S., Maryland State College, Frostburg, Maryland, 1952 Graduate Study, University of Maryland, 1955-1956 Advanced Study in Computer Design, American University Washington, D. C., 1958	
EXPERIENCE:	1952 - 1955	US Army, Field Artillery and Corps of Engineers. Various training and operational duties including Engineer Officer's Candidate School (Distinquished Military Graduate) and theatre of operations assignment.
	1955 - 1956	Teaching position in mathematics and science for secondary schools, Prince George's County, Maryland.
	1956 - Present	Westinghouse Defense and Space Center, Baltimore, Maryland.
	1956 - 1963	Aerospace Division, Various computer oriented duties including logical design, specification, systems analysis, and programming for aerospace, shipboard, and ground-based defense systems. Specific responsibilities included systems analysis, technical specification, and test programs for equipment such as AN/APQ-81 data processing subsystem, AN/ALQ-24 (B-70) defense subsystem computers, and the AN/SPG-59 (Typhon) computer complex. Supervision of early phases of SOLOMON computer design and related research and development programs.
	1963 - 1964	Systems Division. Management of computer applications efforts, specification and programming support for SOLOMON and other computer products.
	1964 - Present	Aerospace Division. SOLOMON Project Manager.
PUBLICATIONS:	"Aircraft or Satellite Digital Signal Analysis Technique," Classified Paper Eighth Annual East Coast Conference on Aerospace and Navigation Electronics, October 1961. "Aerospace Digital Computers," Westinghouse Engineer, May 1962.	
SOCIETIES:	Who's Who in American Colleges and Universities (1952)	

NAME: Robert C. McReynolds, Engineer

EDUCATION: B.S., Mathematics, Lincoln Memorial University, 1960
Graduate work, Mathematics, University of Maryland

EXPERIENCE: 1960 - Present Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland. Advanced Data Processing Systems. Participated in system evaluation tests on AN/APQ-81 Data Processor. Responsible for computing system analysis and preliminary design for discrimination radar computer for ballistic defense system. Participated in determining computer requirements for OAO ground support systems. Performed systems and design analysis on original SOLOMON computer concept. Responsible for defining instruction set for SOLOMON. Performed detailed analysis on application of SOLOMON to satellite surveillance problem. Responsible for advanced computer organization studies.

PATENTS: Six patent disclosures pending relating to Military Special Purpose Computers

Eight patent disclosures pending relating to Parallel Network Computers.

PUBLICATIONS: "Numerical Analysis Consideration for the SOLOMON Computer," coauthor, Proceedings of the Air Force Rome Air Development Center, Westinghouse Electric Corporation. Aerospace Division Workshop, Baltimore, Maryland, October 1962.

"The SOLOMON Computer," coauthor, Proceedings of the Fall Joint Computer Conference, December 1962. This paper was chosen as the outstanding paper for FJCC

"On the Use of the SOLOMON Computer," coauthor, Proceedings of the Fall Joint Computer Conference, December 1962.

SOCIETIES: The Institute of Electrical and Electronics Engineers

NAME: John L. Patrick, Senior Engineer

EDUCATION: B.S.E.E., Wayne State University, 1958

EXPERIENCE:

1951 - 1953	U.S. Army Signal Corps, Radar Technician.
1956 - 1957	F.G. DaRozza, Detroit, Michigan. Directed research and development experiments in nonlinear magnetic devices, electronic control systems, and central components.
1957 - 1958	Dongan Electric Manufacturing Company, Detroit, Michigan. Responsible for transformers engineering lab. Conducted open and short circuit test, efficiency test, and heating checks on power (up to 75 kva), machine tool, control, ignition, and gas tube transformers. Directed production test.
1958 - 1959	Chrysler Corporation, Warren, Michigan. Engineer. Designed go-no-go semiautomatic test fixture. Directed "breadboarding" of circuitry for system simulator test equipment; and build-up and installation of test fixture. Trained technicians to use test fixture. Consultant on testing procedure and fixture problems. Responsible for guidance and control system "black boxes," both missile and ground support.
1959 - Present	The Bendix Corporation, Detroit, Michigan. Senior Engineer. Engaged in medium speed digital techniques using solid state AND-OR logic. Worked with core lines, magnetostrictive delay lines, diode gating, and transistor gating. Techniques and problems of integrating and packaging solid state digital logic with hard contact logic and analog circuits. Worked with digital to analog schemes for developing command signals to closed loop servos; closed loop servos using amplitude and phase analog techniques; resolvers, quantizers, Moire scales, Inductosyns, and optical pulse generators for feedback elements in one speed incremental and three speed absolute

NAME: John L. Patrick (Continued)

EXPERIENCE: (Continued)

systems. Designed and developed control schemes using EIA, AIA, and/or JIC standards. Consultant to sales and customer service staff. Advised application engineers on difficult and/or new control applications. Consultant to production test and checkout mechanical design, and manufacturing departments, involving packaging, assembly, hardware, new designs, new concepts. Assistant engineering supervisor for engineering staff of logic designers. Assistant project manager for design and development of a commercial lathe control. Project manager for design and development of a commercial turret drill control. Interpreting and analyzing customer's requirements for continuous path contouring machine tool controls. Developed and incorporated a new system of handling wiring information and various major logic schemes. Responsible for expanding storage capabilities, doubled iteration rate, improved and expanded integrator circuits; designed a self-checking feature that checked 90% of the logic; designed a test panel as an integral part of the system that reduced test and checkout time and user's down time. Responsible for converting logic notes into wiring and packaging instructions for the construction of an engineering prototype. Directed activities of manufacturing, testing, and evaluating the prototype.

PUBLICATIONS: "High Reactance Transformers."

SOCIETIES: Chairman of Student Branch of Institute of Electrical and Electronics Engineers
Member, Engineering College Student Board

NAME: George Shapiro, Manager

EDUCATION: B. A., Brooklyn College, 1947
M. A., The Johns Hopkins University, 1948
Additional Graduate Work and Teaching, The Johns Hopkins University, 1948 - 1951

EXPERIENCE:

1951 - 1955	Aircraft Armaments, Inc., Senior research mathematician. Systems analysis of fire control systems, and preliminary design, radar, missiles, simulators, computers.
1955 - Present	Westinghouse Defense and Space Center, Aerospace Division, Baltimore, Maryland.
1955 - 1962	Missile Seeker Systems Analysis. Statistical detection theory and antijamming problems. Trajectory analysis and space guidance problems for satellite, lunar, and interplanetary flight. Study of modular arithmetic computations.
1962 - Present	Manager of Analysis and Programming Research in the Computer and Data Systems Technology Department. Responsibilities include direction of research and development in numerical analysis, programming languages, software, and computer organization and design techniques.

PUBLICATIONS: Ten articles published

SOCIETIES: Institute of Electrical and Electronics Engineers
American Mathematical Society

NAME: David K. Sloper, Associate Engineer

EDUCATION: A.B., Dartmouth College, 1960
M.S., Thayer School of Engineering, 1961

EXPERIENCE:

1961 - Present	Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland.
1961 - 1962	Graduate Student Program. Engaged in assignments in logical design, programming, etc.
1962 - Present	Associate Engineer. Engaged in design of SOLOMON breadboard model now in operation. Experience in design of SOLOMON central arithmetic unit. Responsible for local design and development of the SOLOMON Processing Elements and Network Sequencer.

PATENTS: Six disclosures
Two disclosure awards
One patent pending
Four disclosures pending

NAME: Jon Stuart Squire, Senior Engineer

EDUCATION: B.S., Electrical Engineering, University of Michigan, 1960
M.S., Electrical Engineering, University of Michigan, 1962
M.S., Mathematics, University of Michigan, 1963

EXPERIENCE:

1960 - 1962	University of Michigan Research Institute, Programmer-Analyst. Development of a Powerful Problem Oriented Language and Translator. The translator produced programs in several compiler languages from a description of an electromechanical system.
1961 - 1963	University of Michigan, Instructor, Department of Mathematics.
1961 - 1963	University of Michigan Research Institute, Assistant Research Engineer. Developed machine organization of a Multiple Processor Computer. Developed a translation algorithm for use in producing code for the Multiple Processor Computer. Determined statistics for concurrent addressibility of information in lattice connected memories by the Multiple Processor Computer.
1963 - Present	Westinghouse Defense and Space Center, Defense and Space Systems Operations, Baltimore, Maryland, Computer and Data Systems Group. SOLOMON software.

PUBLICATIONS: "Iterative Circuit Computers," Coauthor, Computer Organization, Spartan Books, Inc., 1963
"Programming and Design Considerations of a Highly Parallel Computer," Coauthor, Proceedings, SJCC, 1963
"A Translation Algorithm for a Multiple Processor Computer," ACM National Conference, Denver, Colorado, 1963
"An 11 Cryotron Full Adder," IEEE-Transactions, Electronic Computers Correspondence, 1962.

SOCIETIES: Institute of Electrical and Electronic Engineers
IEEE Professional Technical Group on Electronic Computers
Association for Computing Machinery

NAME: Robert M. Trepp, Engineer

EDUCATION: B.S. (Eng), University of Michigan, 1960

EXPERIENCE:

1960 - Present	Westinghouse Electric Corporation
1960 - 1963	Graduate Student Program. Assistant Engineer. Engaged in assignments in sales engineering, electron beam machines, magnetic thin films.
1962 - Present	Aerospace Division, Baltimore, Maryland. Design and development of SOLOMON component circuits. Development of electrical and wiring rules for the SOLOMON Systems. Engaged in design and development of molecular circuits and packages for the SOLOMON System.

PATENTS: Several disclosures pending

NAME: R. James Bennett, Associate Engineer

EDUCATION: B.S. (Mathematics), University of Michigan, 1962
B.S. (Electrical Engineering), University of Michigan, 1962
M.A. (Mathematics), University of Michigan, 1963

EXPERIENCE:

1963 - Present	Westinghouse Electric Corporation
1963	Pittsburgh, Pennsylvania. Graduate Student Training with assignments in Aerospace Division, Lima, Ohio, and in Baltimore Defense and Space Center. Worked on Fourier analysis of several waveforms and completed a FORTRAN program to compute Fourier coefficients on IBM 1620. Worked with EASE Analog Computer.
1963 - Present	Defense and Space Center, Baltimore, Maryland. Associate Engineer. Analysis and programming in FORTRAN and Machine languages for IBM 7094, UNIVAC 1107 and SOLOMON Computers. Developing FORTRAN IV program to design a printed circuit automatically. Developing algorithms for floating point and double precision arithmetic with SOLOMON Computer. Applying SOLOMON Computer techniques to solution of weather prediction problems and to reduction of satellite telemetry data.

3.3 SCHEDULE

This paragraph details the schedules that will be maintained in the performance of this contract. Figure 3-3 shows the overall hardware program breaking down the major units into design and manufacturing tasks. Figure 3-4 shows the software effort during the same period.

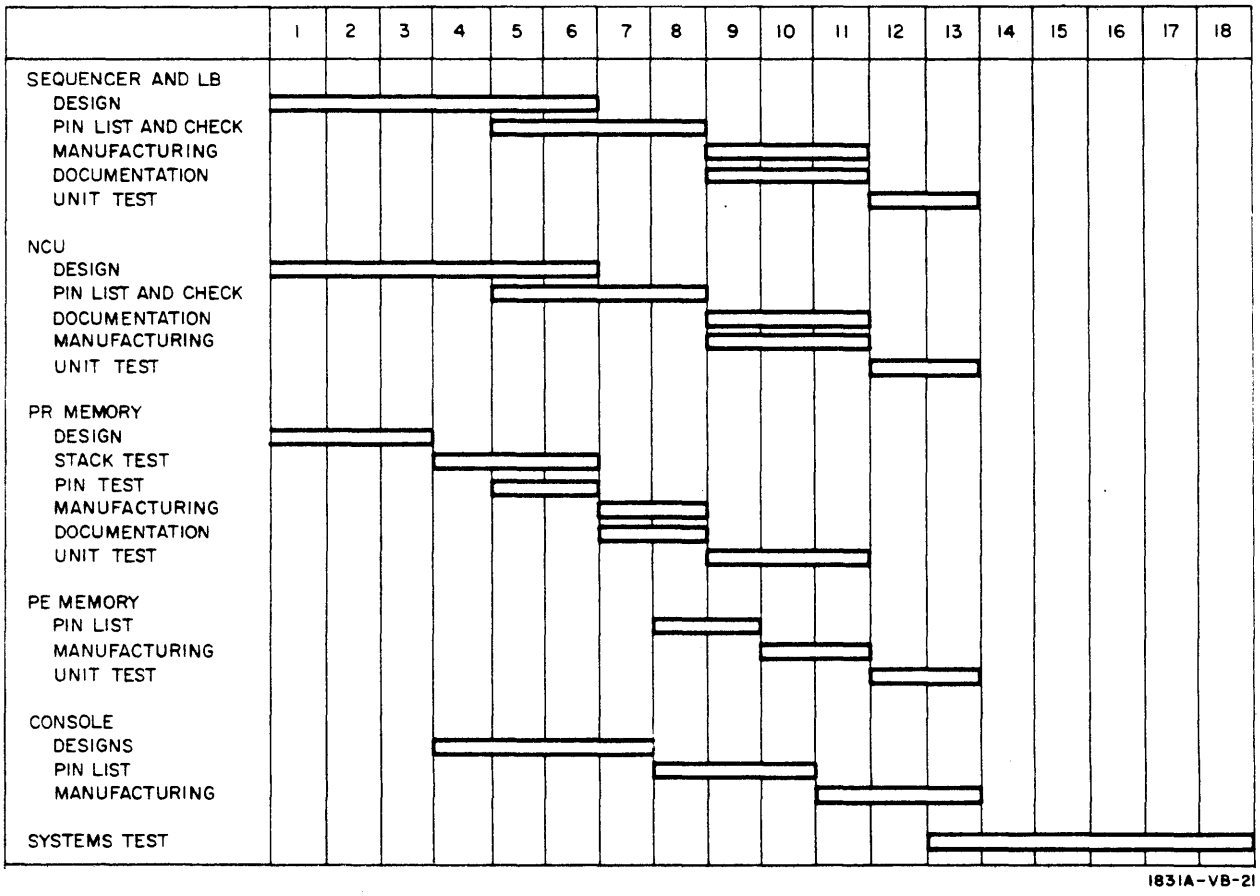


Figure 3-3. SOLOMON II Hardware Schedule

3.3.1 Hardware Milestones

These dates are based on a contract go-ahead as of 1 October 1964.

a. 1 December 1964

(1) Instruction repertoire, format and starting sequencers, completed with 6600 defined.

(2) All circuits finalized and sample tested.

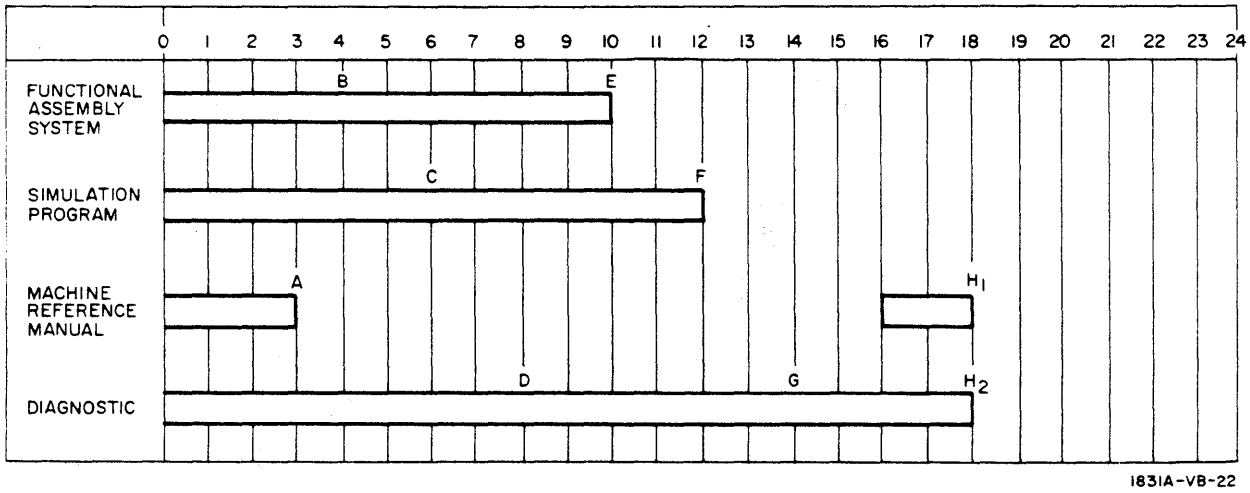


Figure 3-4. SOLOMON II Software Schedule

(3) First PE memory wiring tables started. Stack and components ordered.

(4) PE final version complete and begin manufacturing the first sample units for test.

b. 1 January 1965

Preliminary Programming Manual available.

c. 1 March 1965

(1) L-buffer design complete.

(2) Memory stack test completed.

(3) NCU logic design complete.

(4) Preliminary Sequencer and PE Units tests begin.

(5) Console layout decided upon and design begins.

(6) All parts ordering complete.

d. 1 June 1965

(1) L-buffer wiring tables complete and released to manufacture.

(2) Final PE Memory released to manufacture. Final Program Memory released to manufacture.

(3) All parts and components received for 32 PE System.

(4) NCU wiring tables completed and released to manufacture.

(5) Sequencer finalized and wiring tables begins.

(6) PE design finalized and tested out, and sample batch released for manufacture.

(7) Console design completed, wiring tables started.

(8) Maintenance Manuals started.

e. 1 September 1965

(1) L-buffer complete and test and checkout begins.

(2) Complete Memory and Control Unit; test and checkout begins.

(3) Final Sequencer released for manufacture.

(4) Final PE quantities released for manufacture.

(5) Final Console released for manufacture.

f. 1 November 1965

(1) Assembly of tested subunits into final configuration begins.

(2) Diagnostic test debugging begins.

g. 1 March 1966

(1) System hardware checkout completed.

(2) System turned over for software debugging.

(3) Customer performance tests started

h. 1 April 1966

(1) Machine available.

3.3.2 Programming Milestones

These dates are based on a contract start date of 1 October 1964.

a. 1 January 1965

(1) Preliminary Machine Reference Manual.

b. 1 February 1965

(1) Functional assembly system available for preliminary use.

c. 1 April 1965

(1) Preliminary use of simulator.

d. 1 June 1965

(1) Analysis and coding complete on diagnostic programs. Begin assembly and simulation process to debug programs. Provide feedback to assembly and simulation.

e. 1 July 1965

(1) Functional assembly system available for full use. Remaining effort limited to minor corrections as detected through use.

f. 1 September 1965

(1) Full use of simulator. Remaining effort limited to minor corrections and design changes.

g. 1 December 1965

(1) Begin hardware checkout of diagnostics.

h. 1 April 1966

(1) Final Machine Reference Manual.

(2) Diagnostic checkout complete.

3.4 RELATED EXPERIENCE AND FACILITIES

This paragraph contains descriptions of other related experience as well as the facilities available at the Westinghouse Aerospace Division.

3.4.1 Computer Experience

a. Airborne Radar Data Processor

In this contract, the AN/APQ-81 digital data processor was designed and fabricated for use in an airborne radar system. This is the fastest military airborne data processor currently available and provides multiple track-while-scan capability in the pulse doppler radar system. It is a 1-megacycle parallel-synchronous single-address system of advanced design, which permits reliable operation of its linear selection ferrite core memories up to +85°C with only circulating air for cooling.

b. OAO Ground Operational Equipment

Under NASA Contract NAS 5-814; GAEC P.O. H-94200-c, Westinghouse is developing the control consoles to be used in ground control stations at Goddard Space Flight Center; Rosman, North Carolina; Quito, Ecuador; and Santiago, Chile, for commanding the OAO and retrieving data from its operational life in orbit. Two central control station consoles and three remote station consoles have been delivered to Grumman Aircraft Engineering Corporation as a result of this work. The control consoles provide integration in the ground control stations of the command transmitters, telemetry receivers, general purpose computer, PCM-data handling equipment, and TWX terminal equipment so that a contact with the satellite while over the control stations can be executed automatically in a very short length of time.

The central and remote control consoles are similar in function but the remote consoles are less complicated in mechanization due to the limited decision-making abilities of operations personnel at the remote stations.

c. OAO Mobile Station Control Consoles

Under NASA Contract NAS 5-814; GAEC P.O. I-43250, Westinghouse is also developing the control and integration equipment consoles for use in mobile stations which Grumman Aircraft Engineering Corporation will use to

control the satellite during integration and qualification tests at Grumman, integration tests at GSFC, and prelaunch checkout at Cape Kennedy. The control consoles integrate the operation of a general-purpose computer, command transmitters, telemetry receivers, and PCM-DHE in the mobile station so that the entire station can be operated from a single console while controlling the satellite during the tests. Two consoles have been delivered to Grumman Aircraft Engineering Corporation for this use.

d. Title: S-52/UK-2 International Satellite, Test Stand and Data Reduction Facility

The S-52/UK-2 Test Stand and Data Reduction Facility includes equipment which performs operational tests on the satellite; provides a means of processing the satellite test data rapidly; records the satellite PFM telemetry data on magnetic and oscillographic tape; provides means of preparing the data in a form suitable for direct digital entry and displays selectable data words.

e. Automatic Radar Control and Data Equipment (ARCADE)

The Westinghouse Defense and Space Center is working on the design and fabrication of Automatic Radar Control and Data Equipment (ARCADE) under contract to the White Sands Missile Range, New Mexico.

The ARCADE data processing equipment being fabricated consists of a special-purpose digital computer with a 500-kc clock rate and peripheral equipment to integrate the computer into an AN/FPS-16 radar system.

f. ASW Radar Data Processor

A data processor is being developed on this program to assist the operator by storing and sorting radar data and providing displays with live and/or stored information. The processor consists of a high-speed digital computer and several ancillary equipments for input and output. The system has a storage capacity for 256 12-bit words, with an add time of 2.0 μsec and multiply and divide time, dependent upon word length, with a maximum of 48 μsec. It also has a core memory with nonvolatile storage in case of power failure.

g. AN/GPA-35 Missile Control System

This equipment is a complete ground control system designed and developed to exercise intercept control of the IM-99A and IM-99B Bomarc missiles. This system was designed, developed, produced, installed, and carried through a field evaluation program at Patrick Air Force Base and MacDill Air Force Base. The complete system comprised a Weapon Direction Center, Squadron Operation Center, and a forward Tropospheric Microwave Scatter Link. Some of the salient features of the system included:

(1) Broadband video transmission over 200 miles via scatter link

(2) Multiple loop weapon control using a large scale digital computer as the central real time data processor

(3) Automatic gated video tracking

(4) Frequency and time multiplexed communications

(5) Accurate video combining for display

(6) Automatic operational test

(7) Transmission and maintenance of missile status from multiple bases and squadrons.

h. AN/FPQ-4 Modifications for Synthetic Spectrum

The data processor required for the proposed program is similar in many respects to that already designed, fabricated, and tested by the Westinghouse Electric Corporation for the Synthetic Spectrum modification of the AN/FPQ-4 radar. Westinghouse is currently under contract to implement the same problem as the Target Designation and Acquisition data system. The AN/FPQ-4 Modified for Synthetic Spectrum receives pointing data from a radar site located 100 miles away. The pointing data is transmitted over a telephone data link between the two sites. The Westinghouse computer then computes the data for steering the AN/FPQ-4 antenna with the accuracy necessary for satellite acquisition. This high speed data processor includes the following equipments:

(1) Recording system

(2) Display system

(3) High-speed, 300-channel multiplexer

(4) Digital range tracker

i. Optical Radar Matrix Receiver Data Processor

An optical radar matrix receiver data processor is under development. The system processes data derived from a matrix of sensors. The data processor input unit supplies threshold detection of all sensor outputs and stores a complete image of all returns detected. Two forms of data handling are required of the processor; a high speed interval timing function, and a coordinate tracking function of a selected return in the matrix. Displays include a display of all data appearing in the matrix, the current coordinates of the tracked return, and a display in decimal form of the time interval measurement. The data processor utilizes high frequency digital building blocks for data storage and interval timing functions, analog pulse integrators for background suppression, and beam switching tube decade counters for display of interval timing functions.

j. Modular Arithmetic Techniques

This project is to investigate the potentialities of computation techniques through the use of residue class arithmetic, and to evaluate the feasibility of a modular-arithmetic digital computer. It involves programming, logic design, and system design in addition to basic number theory investigation.

k. Self-Adaptive Computer Techniques

Westinghouse Aerospace Division has been active in research on self-adaptive techniques. Significant programs include company-sponsored military research studies on weighted threshold logic, majority logic, redundancy, and unique computer organizations especially conductive to adaptive programming.

A redundancy demonstration unit has been built, tested, and demonstrated at Aerospace Division. This device consists of three identical adder-subtractors tied together operationally with majority gating techniques so that if any one logical element in any chain fails (provision is made in the demonstrator to induce failure at will) the arithmetic function will not be adversely affected.

In the areas of threshold logic, Westinghouse research programs have produced effective synthesis algorithms and an experimental threshold gate element of highly desirable characteristics. It has been shown in these programs that a single-bit full adder can be mechanized with two threshold gates.

1. Nondestructive Readout Memory Systems

The Aerospace Division has a continuing research and development program in the area of nondestructive readout, random access memory systems. In September of 1961, a 2000-hour reliability test was completed on a 1024 word, random access, NDRO, multiaperture ferrite device, electrically alterable memory. This memory system was designed specifically for read-only usage and was operated at a 0.5 μsec cycle time. Currently, a read-write NDRO memory system is undergoing test in the Aerospace engineering laboratory. This system, designed specifically for Aerospace applications, is capable of storing 512 fifteen-bit words with a 0.6 μsec read cycle time and a 6-μsec clear-write cycle time.

3.4.2 Facilities

3.4.2.1 Westinghouse Defense and Space Center

The Westinghouse Defense and Space Center in Baltimore, Maryland, (figure 3-5) a major unit of the Atomic, Defense and Space Group, is the focal point for military and space systems and equipment development and manufacture for the corporation. Its Aerospace Division directs its basic efforts toward airborne and space projects in the areas of armament control, guidance and navigation, reconnaissance and surveillance, command and control, computer systems, and electronic warfare. Its Surface Division is concerned with land and sea surface-based programs in armament control, surveillance, command and control, communications and electronic equipment in underground defense centers. The Underseas Division is devoted to underwater projects in areas of ordnance, command and control, surveillance, and oceanography. For purposes of coordination of the efforts of all divisions, and other corporate resources as may be required on major systems programs embracing a mix of Defense and Space Center capabilities, the Defense and Space Systems Operations organization has been established as the fourth divisional entity of the Center.

This complex, with its supporting administrative services and logistic and field support operations, occupies over 2,000,000 square feet of engineering, laboratory, manufacturing, and office space, centered principally at Friendship Airport. Over 12,000 persons are employed, including 2500 graduate engineers and scientists.

The Center is currently embarked on an expansion program in which additional operating units devoted to specific product lines which will support the overall systems effort are being established in the surrounding metropolitan area at locations which take best advantage of the professional and skilled labor market.

3.4.2.2 Aerospace Division

The Aerospace Division of Westinghouse Electric Corporation is an integral facility of the Westinghouse Defense and Space Center and a major

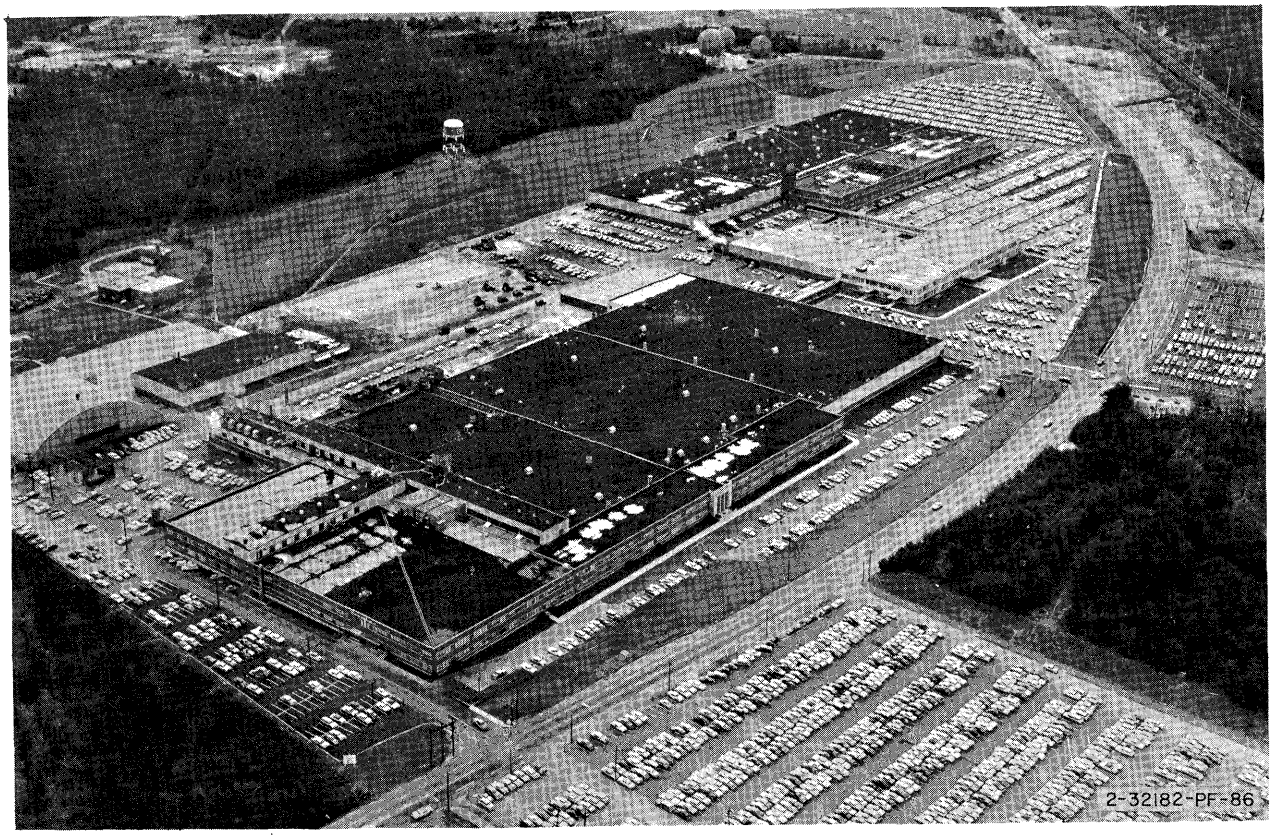


Figure 3-5. Westinghouse Defense and Space Center, Aerospace Division in the Foreground

division of the Westinghouse Atomic, Defense and Space Group. It is unique concentration of talent and facilities devoted exclusively to the development and manufacture of airborne and space electronics systems.

Since its establishment in 1951, the Aerospace Division has continually expanded to meet the growing demands of the aerospace industry. It now amounts to a 37-million-dollar investment of modern engineering and manufacturing facilities and equipment, capable of fulfilling the requirements of the largest aerospace programs. It comprises 876,423 square feet of engineering space, laboratories, test facilities, and reliability and manufacturing areas, allocated as follows:

Engineering	295,021
Manufacturing and product reliability	364,682
Support facilities	136,000
General office area	80,720

The 364,682 square feet of floor space used for manufacturing and product reliability activities can accommodate 4500 workers on a three-shift basis. The facilities, which are among the best in the industry, can produce all types of aerospace electronic systems.

The scope of Aerospace Division activity includes basic and applied research, design, development, and prototype or volume production. It ranges from minor support equipment to major military systems. It covers the spectra of radar, infrared, ultraviolet, and optical techniques and includes applications to aircraft, submarines, missiles, satellites, and spacecraft. In recent years the Aerospace Division has had major programs for pulse and pulse doppler air intercept radar, missile guidance and control, electronic countermeasures, submarine weapons control, satellites and spacecraft, computer systems, and surveillance.

Aerospace Division personnel numbered 3828 as of 23 May 1964. These employees were assigned and classified as follows:

Department	Class	Number	Total
Engineering	Professional	1171	
	Nonprofessional	700	1871
Manufacturing	Production	1210	1210
Product reliability	Production	491	491
Marketing and administration		152	152
Astroelectronics laboratory		104	104
			3828

Although Aerospace is only one of more than 50 Westinghouse divisions, it employs over 10 percent of Westinghouse scientists and engineers. Of these, over 700 have bachelor of science degrees, approximately 140 have master

of science degrees, and 35 have doctor of philosophy degrees. In addition, the professional talent and facilities of other related Westinghouse divisions are available to support Aerospace projects. Through visits and other means of communications, specialized help can be obtained quickly when it is needed.

The management of the Aerospace Division is geared to the dynamic character of the aerospace industry. It combines the skills and talents of the best scientists, engineers, and business administrators available today. This alert, aggressive, and informed management enables the division to study and understand complex military weapon system requirements and to direct research and development effort to meet those needs.

Some of the Aerospace facilities and services are described briefly in the following paragraphs.

a. Computer Development Laboratory

The Computer Development Laboratory was created for the exclusive purpose of developing, manufacturing and fabrication techniques as applied to SOLOMON II and other digital computers. The laboratory has an area of 12,000 square feet which is subdivided as follows: 8000 square feet of floor space is devoted to manufacturing and fabrication techniques, 2000 square feet to development and evaluation of digital circuits, and 2000 square feet for test and checkout.

In the modern plating room, which incorporates a high degree of control and maintains "clean" conditions, printed circuit boards with plated-through holes are fabricated. Holes as small as 0.010 inch in diameter are plated, first with copper, then with a choice of precious and nonprecious metals. At present, printed circuit boards are being plated with nickel, tin-lead, gold, silver and rhodium.

With the aid of a highly controllable etching machine, etching capabilities have been developed to the point where conductor ribbon widths of 0.005 inch are common and 0.001 inch are achieved on 2-ounce copper, double-clad laminates. This is possible because plating growth is on the order of 0.0005 inch.

Printed circuit board assembly techniques are developed to handle molecular electronic devices and "cordwood" modules at low cost and high production rates. The techniques result in a high reliability printed circuit assembly. To keep cost down, assembled printed circuit boards are wave soldered. If package density demands it, electronic assemblies can be resistance-welded or thermal-bonded.

b. Engineering Model Shop

The Model Shop constructs experimental models, prototypes, and production equipment in small numbers for Aerospace Division research and development programs. The total shop area is 16,000 square feet.

The Model Shop has extensive experience in machining tool steel, stainless steels, aluminum, magnesium, copper, brass, titanium, invar, and kovar. It has fabricated precision components such as antenna gimbals and gyroscopes and complete radar systems such as the AN/DPN-34, and AN/DPN-53 pulse and pulse-doppler radars. Modules for the Gemini and UK-2/S-52 satellites and the Pathfinder countermeasures system models were constructed here.

Model Shop personnel, numbering 180, include expert model makers, machinists, sheet metal workers, and assembly and wiring specialists. The 120 technicians average 8 years experience. Wiring specialists average 14 years. Flexible operating procedures permit close working relationships between engineers and craftsmen, facilitating the incorporation of changes necessary for design modifications and equipment experimentation and testing.

The overall floorspace occupied by the Model Shop at present totals 16,000 square feet; however, a standing authorization permits expansion into the Manufacturing Department as required for specific programs.

c. Manufacturing Facilities

Approximately 370,000 square feet of floor space at the Aerospace Division is used for fabrication, assembly, and factory testing. Machinery, tools, and equipment on hand are valued in excess of $4 million. Under a 5-year facilities plan approved by corporate headquarters in 1963, this entire manufacturing area is being improved at a cost of $2.3 million to permit

complete manufacturing environmental control and the addition of a new printed circuit board facility.

The environmental control system for the Aerospace Division building is being constructed to maintain general space conditions at 75°F in both summer and winter, regardless of thermal load fluctuations. Sufficient flexibility is to be incorporated in the system to permit relocation of departments and/or sources of high thermal loads within the plant with a minimum of physical changes to the original installation. Clean rooms furnished with complete environmental control systems will be provided as necessary to meet specific system fabrication requirements. Facilities provided will ensure control of factory environmental conditions necessitated by the quality assurance requirements associated with each contract. A centralized control panel and motor control center will provide means of monitoring temperatures, humidity, and water flow rates at selected points in the distribution system.

d. Solid State Systems Technology Laboratory

Established at the Aerospace Division to support the Westinghouse Defense and Space Center in the design and development of advanced electronic systems, the Solid State Systems Technology Laboratory designs, develops, and fabricates advanced solid state structures, for the purpose of achieving more reliable, smaller, and lighter aerospace systems. By direct contact between device design engineers of the Solid State Systems Technology Laboratory and system design engineers of Molecular Engineering Systems and other Aerospace design groups, the most recent concepts in solid state technology are applied to the design of advanced communication, guidance, detection and computer systems.

3.5 RELIABILITY AND QUALITY ASSURANCE CONTROL

The reliability program at the Aerospace Division of Westinghouse has been developed to a high degree of effectiveness through ten years of application to airborne and space systems. Programs susch as the Rendezvous Radar for the Gemini Spacecraft and the UK-2/S-52 International Satellite have provided Aerospace with detailed knowledge of the problems involved in

designing and developing circuitry and systems for reliability and long life in the space environment where conditions are obviously extreme.

Successful completion of the qualification tests of the UK-2/S-52 satellite at stresses greater than those expected during launch and orbit has proven the reliability of the design, packaging techniques, and in-process manufacturing controls applied to the Westinghouse-built structure and associated electronics. During qualification tests the satellite was in operation for over 1400 hours.

The UK-2/S-52 satellite was designed for a reliability objective of approximately one year in orbit. The realization of such an objective requires careful attention to all phases of design and fabrication. The reliability requirements of the proposed Solomon II equipment will also require careful parts selection and control, design adherence to redundancy and derating requirements, careful manufacturing processes and techniques, elaborate testing of components, and an effective quality assurance program.

3.5.1 Parts Selection and Control

The Aerospace Division provides, as one of its major activities, the means of selecting parts of proven reliability. The primary objective is to ensure that each part is suited to its application. Components engineering specialists, experienced in the different classes of components, are available to a assist the design engineers in this task.

Components engineers investigate new products, analyze failures, advise other departments, and provide liaison with suppliers. They also publish standards, standard parts lists, and preferred parts lists. An engineer will be responsible for assisting the design engineers in the selection of reliable parts to meet the design requirements. He will prepare a "preferred parts list" and give it to each engineer. This standardizes the part types from which selection can be made. Parts on this list have been carefully evaluated through extensive usage on test programs, and their reliability parameters have been accurately determined. Parts that have proved reliable on previous systems will be used wherever practical on the proposed equipment.

3.5.2 Design

It is during the design phase that the inherent level of quality for the proposed equipment will be established, since it is well known that quality must be designed and built into equipment and cannot be inspected into it alone. Thus, sufficient controls must be placed on the program to ensure that the fundamental design principles are upheld. Design engineers for this program will conduct frequent consultations with specialists from the Components, Materials, Standards, Reliability, and Manufacturing Departments. Early in the design phase, the design engineer will supply specific part information concerning application, derating, operating temperatures, etc, to the components specialists who will in turn prepare a system parts list which has all the information necessary for a reliability analysis.

The philosophies, concepts, and designs generated during the design phase become firm requirements in the form of engineering drawings and equipment specifications. This information is then released for fabrication of equipment either within the Aerospace Model Shop or from outside suppliers.

3.5.3 Quality Assurance Program

The basic objective of the Product Reliability Department at Westinghouse Aerospace is to provide the control necessary to convert a reliable design into equipment without degradation of the inherent reliability.

The Product Reliability Department of the Aerospace Division functions under the direction of the Manager of Product Reliability, who is responsible to the Division General Manager for overall quality. This department has the organization and necessary authority to maintain control of quality throughout the Division. It is the prime responsibility of the Product Reliability Department to ensure that production operations and all related efforts are conducted in a manner which will result in a quality product and will assure reliable performance of the end product.

Aerospace's quality control system is based on the requirements of MIL-Q-9858 and MIL-Q-21549. It is maintained to meet the latest quality assurance requirements of applicable Government specifications, including: MIL-G-2550, MIL-E-4158, MIL-E-5400, MIL-E-8189, MIL-W-9411, NASA NPC 200-1, 200-2, and 200-3. Westinghouse realizes that strict compliance to the applicable MIL specs with the associated documentation is necessary on production contracts of long term duration. Where no maintainability or logistics support is required to conform to the applicable MIL-spec, a lesser amount of documentation is proposed at no sacrifice of quality or reliability. Appreciable cost savings are realized by this approach. If the customer desires a complete MIL-spec program, the additional cost can be negotiated.

All the necessary controls to ensure compliance to the required quality will be used in the SOLOMON II program.

The Product Reliability Department prepares various reliability procedures controlling Aerospace operations, including: the quality control manual, product reliability station instructions, and test specifications. These procedures cover inspection, test operations, and documentation (including station records, control tags, and performance data).

The control of supplier reliability is maintained by receiving inspection which has the responsibility of verifying the quantity, quality, and conformance of all purchased materials and parts. Mechanical inspections and electrical tests check items against Westinghouse, military, and vendor drawings, specifications, and instructions. These documents specify the required quality levels.

Items passing electrical and mechanical inspection are sample tested for environmental requirements. Items that fail are entered on a Material Rejection Notice and reviewed by Product Reliability, Engineering, Purchasing, and the customer's representatives for disposition. Rejected items are returned to the supplier. Items accepted with minor discrepancies are formally documented by the Material Review Board procedure with vendor requested to answer with corrective action to prevent future discrepancies.

For each contract, the flow of materials and parts through Receiving, Manufacturing Assembly, and Shipping is studied to determine the location of inspections and tests to ensure maximum reliability. Both in-process (prior to the completion of an operation) and final (at completion of an operation) inspections and tests are performed.

Controls (initiated and monitored by the Product Reliability Department) necessary to produce a product of high reliability are listed as follows:

a. Stock control (identification and protection of parts)

b. Statistical process control (control charts and statistical studies)

c. Manufacturing inspection (of fabrication operations)

d. Control and calibration of tools, gages, and electrical measuring equipment

e. Special processes control (welding, heat-treating, penetrant inspection, plating, painting, embedding of transformers and molded units, printed circuits, soldering, manufacture of hydraulic parts, and packaging).

3.5.4 Reliability Analysis

A reliability analysis is, in essence, a task to develop the ground rules as to what constitutes a failure, how such a failure can occur, what the effect of the failure will be, and when it is most likely to occur. The prediction as to the most likely time of occurrence is a conclusion based on a series of assumptions and approximate data, this data having the form of component part failure rates.

In a typical reliability program at Westinghouse, an informal reliability document is prepared which includes a reliability analysis and prediction, a parts list and numerical tabulation of parts by subsystem and system, and a failure mode (effect of failure) analysis.

3.6 SUBCONTRACTOR SELECTION

3.6.1 RFP Preparation

When the major subcontract areas have been established during the program, bid packages are prepared. To assure timely receipt of subcontractor's proposals, and completely fair proposal evaluation, complete bidder's

packages are prepared in each major subcontract area. A general specification is prepared which becomes a part of all bidder's packages. This specification includes all technical requirements of a general nature applicable to all subcontract requirements, such as engineering data, reports and drawing requirements, spare parts requirements, applicable reliability and quality control requirements, required design reviews, PERT/COST report requirements, etc. The various engineers assigned technical responsibility will prepare technical specifications for their particular requirements. These specifications outline specific technical requirements including test and acceptance procedures for each major subassembly or piece of hardware. Concurrent with the engineering effort, a qualified bidder's list is established in each area. A detailed review of prime terms and conditions will be made with Contract Administration personnel, and a standard contractual format will be prepared for use with all subcontracts. Standard cost breakdown formats will be prepared requiring sufficient detail to assure thorough cost and price evaluation and analysis, fair and accurate comparison of bidders in like areas, and timely and complete cost control. Finally, a formal request for proposal will be prepared in each area detailing all requirements and items to be covered in the proposal, setting forth schedules, establishing reports and control requirements along with instructions for the use of various attachments. In order to establish complete rapport between Westinghouse and subcontractors, pre-bid conferences, technical briefings, and seminars will be conducted. When interface requirements exist between subcontractors, joint seminars will be conducted by Westinghouse to assure optimum integration.

3.6.2 Selection of Bidders

During the past years, Westinghouse has accumulated a wealth of knowledge on subcontractors who are qualified to supply equipment to the Westinghouse Defense and Space Center. New equipment suppliers are added continuously to the qualified lists, but only after a thorough formal technical and administrative evaluation. Moreover, subcontractor organizations proven

inadequate due to substandard performances, inordinate delivery delays, or poor product quality are removed from approved lists and must pass a stringent requalification to be reinstated.

In the selection of a supplier for any given job, proposals are solicited only from those bidders who have been technically and administratively evaluated and are known to be capable of performing the required work. The extent of the evaluation of capabilities is tempered by past experience, the magnitude of the job, and the schedule requirements of a given program. In the evaluation of prospective bidders (and to select those qualified to receive invitations to bid), as a minimum, the following factors will be considered:

(1) Technical Reputation of the Company - A company worth considering has a good reputation with the Government and with the companies who have procured its material or services. The overall reputation is a major factor in analyzing and selecting potential bidders.

(2) Technical Capability - Ability to satisfy the requirements of the basic specifications and depth of technical experience and capability that can be brought to bear on technical problems.

(3) Financial Consideration - Analysis of Dun & Bradstreet Reports or other financial reports containing essential information about business concerns.

(4) Past Performance - The ability of a company to provide materials and services within a reasonable time at a competitive or reasonable price is an important factor in the selection of qualified bidders. If a company has performed in the past, it can be extended an opportunity to bid on future purchases falling within its capabilities.

(5) Manufacturing Capability - Ability to manufacture quality products within the time required to satisfy the needs of the procurement.

(6) Capability to Meet Schedules - Ability to comply with the required or proposed delivery schedule considering all existing commercial and military business commitments.

(7) Geographic Location - When items (1) through (6) are considered approximately equal, consideration will be given to geographic location where this could have a significant effect on time and cost relative to liaison by engineering, manufacturing, and purchasing personnel.

(8) Small Business - The buyer shall give adequate and timely consideration to having a fair portion of small business concerns selected as prospective bidders to the extent practical and consistent with their capabilities.

(9) Distressed Labor Areas - The buyer shall give adequate time and consideration to the placement of concerns on the bidder's list which are located in distressed labor areas, to the extent practical and consistent with their capabilities.

An evaluation and selection report of qualified subcontractors is prepared. Recommendations contained in this report are used as a base by Program Management in making a final subcontractor selection. When necessary, an evaluation team consisting of qualified personnel from Engineering, Manufacturing, and other departments are called together to review the qualifications of subcontractors. Proposals are screened by the members of the evaluation team to eliminate those subcontractors who are obviously unacceptable from a technical standpoint. Upon completion of the preliminary screening, a detailed study of the remaining bids is made, including the technical and management proposal, as well as a complete cost analysis.

Upon completion of the proposal review, the team visits facilities where necessary. During these visits, the proposals are discussed in detail, questions prepared in advance by the team are presented, discussions are held with their management, and surveys of the plants and facilities are made. The evaluation team prepares the evaluation and selection report for presentation to the Program Manager for approval. This report forms the basis for selection or any further investigation that may be required.

3.6.3 Evaluation of Proposals

A program for complete and comprehensive evaluation of proposals by evaluation teams is established. Upon receipt of proposals, technical exhibits will be forwarded to the cognizant engineering personnel for review, while management and cost proposals will be reviewed by the appropriate personnel of the program management organization. Cost and price information in each major area will be charted to facilitate comparison and evaluation. Following this initial review, the members of the review team will meet together for final evaluation and selection. This effort will begin with a report by the technical representatives on those bidders in each major area felt to be best qualified from a technical standpoint. A detailed review of proposals, as well as a complete analysis of costs, will then be made. The following represent some of the non-cost areas to be considered:

(1) Technical Qualification
(2) Manufacturing Capability
(3) Reliability and Quality Control Capability
(4) Purchasing Capability
(5) Management Capability

The detail with which the above and other criteria will be covered depends upon the requirements governing the area in which the subcontractor proposes to participate. Supplemental information will be requested where necessary to clarify information contained in proposals or to cover points previously overlooked.

3.6.4 Selection of Subcontract Type

Where possible, firm fixed price type contracts are used when the specifications contain sufficient information for bidders to quote an accurate price. The Aerospace Division is presently administering cost plus fixed fee, fixed price redeterminable, firm fixed price, and time and material subcontracts. In keeping with recent Department of Defense emphasis on incentive-type contracts, an extensive educational program has been conducted to ensure that all subcontract personnel are prepared to utilize these types of contracts,

whenever the proper circumstances arise. In these circumstances, the incentive areas will be selected to effect the optimum performance of the requirements of the prime contract. In arriving at the best type of subcontract, the following factors are considered:

(1) Type and complexity of items.

(2) The availability and completeness of ordering information such as specifications, work statements, etc.

(3) The degree of competition present.

(4) Availability of pricing data to determine reasonableness of prices and costs.

(5) Problems associated with lack of production experience or instability of design.

(6) Subcontractor's technical and financial capabilities.

(7) Prior experience on the part of Westinghouse and the subcontractor in relation to the item to be procured.

(8) Administrative costs of both buyer and subcontractor.

3.6.5 Negotiation

The Purchasing and Subcontracting Director has the responsibility of negotiating a final contract based on the evaluation and selection report. He will secure the best price, terms, and conditions possible. To fulfill the responsibility he utilizes the services of engineering personnel, cost analysis, the Westinghouse Contract Administrator of the prime contract, and other personnel who can assist him in this effort. Complete contract packages are forwarded to the cognizant Administrative Contracting Officer for approval in accordance with prime contract requirements.

3.6.6 Subcontract Control

a. General Administration

The Purchasing and Subcontracting Director is completely responsible for the administration and control of the subcontract from the time of award until its successful completion and closeout. He is "Westinghouse" to the subcontractor, and as such, is the leader and coordinator in all contacts with the

subcontractor. The Purchasing and Subcontracting Director will require that all reports and correspondence go out and come in through him or his representative, with copies to him. No amendment of any kind can be made to the subcontract unless signed by him. This provides both Westinghouse and the customer with one individual constantly prepared to report on subcontract status. He will make certain that subcontractors having major second tier subcontracting efforts are required to apply the same emphasis on quality, performance, cost control, and delivery as the prime contractor.

The Purchasing and Subcontracting Director will supplement reports with frequent visits to the subcontractor's plant to check progress. He will establish and lead a coordination team that will meet regularly with the subcontractor to review progress and resolve problems. He will be in constant contact with the Westinghouse resident representatives and request their assistance whenever necessary to check progress. Upon completion of the subcontract, he will expedite the final audit and promptly negotiate an equitable settlement and closeout. Westinghouse is well aware that, to a large extent, its performance on a program of this type will only be as good as that of its major subcontractors. For this reason, all necessary steps are taken to assure proper subcontract administration.