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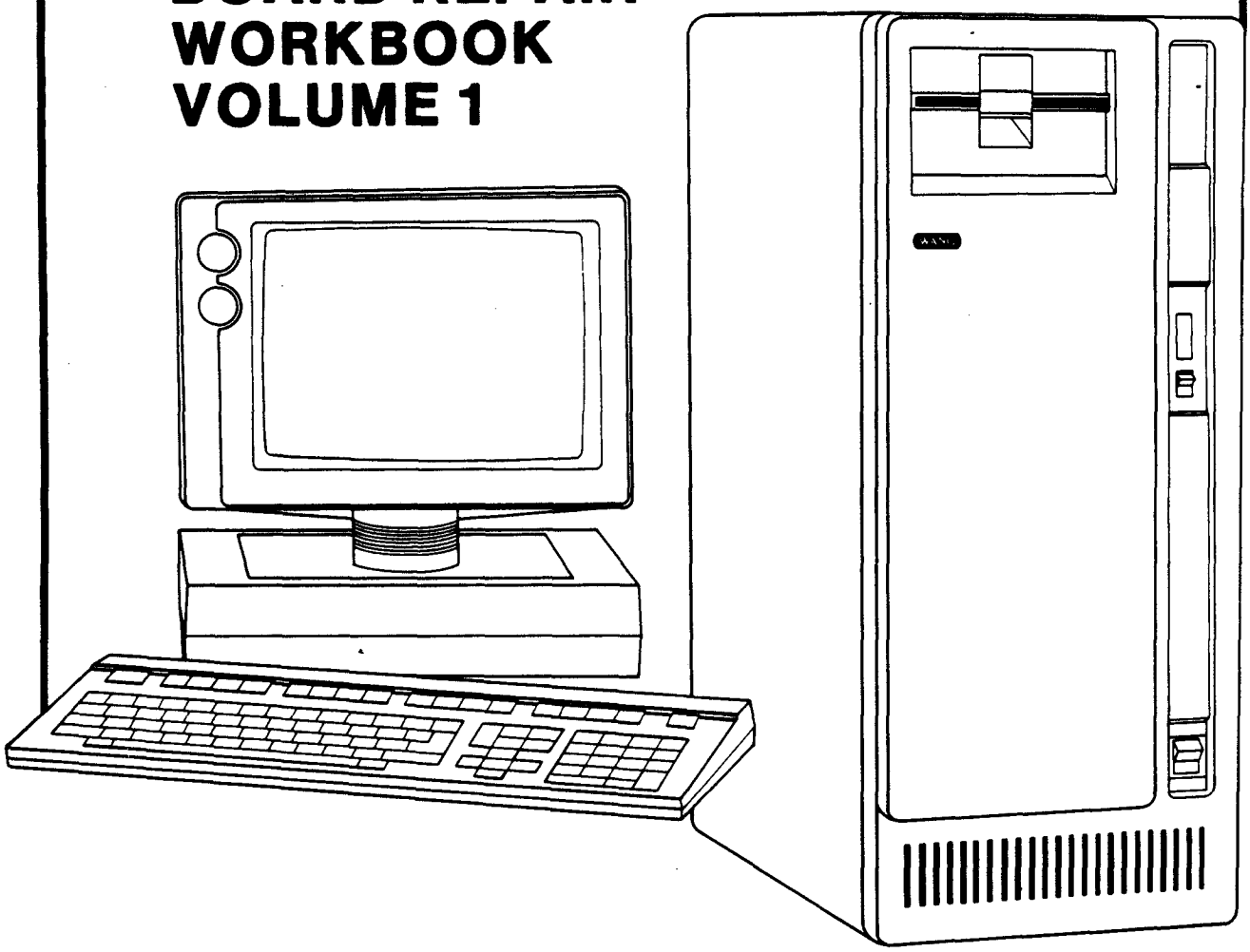
OIS 40/50/60

BOARD REPAIR WORKBOOK VOLUME 1



CUSTOMER ENGINEERING
TRAINING AND DOCUMENTATION

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WANG

CUSTOMER ENGINEERING TRAINING CENTER

OIS 40/50/60
BOARD REPAIR WORKBOOK VOLUME 1

PREFACE

This document is intended to be used for TRAINING PURPOSES only. The material contained in this document, while accurate during the developement of this workbook, may not reflect the latest developments or changes to the OIS 40/50/60 system.

TECHNICAL SUPPORT DOCUMENTS

OIS 50 INTERNAL PRINTER CONTROLLER HARDWARE SPECIFICATIONS HM-60
OIS 40/50 RESOURCE MANAGEMENT UNIT THEORY OF OPERATION 751-0902
OIS 40/50 RESOURCE CONTROL UNIT THEORY OF OPERATION 751-0911
OIS 40/50 IWS FULL MATRIX CONTROLLER SPECIFICATION HM-67
WL-2630 OIS/VS COLLECTIVE GATE ARRAY SPECIFICATION HM-37
OIS-50 INTERNAL WISE SPECIFICATION REVISION 3 HM-85
OFFICE INFORMATION SYSTEMS OIS 40/50/60 741-1267
OIS SYSTEM ADMINISTRATION GUIDE 700-5562E

First Edition - December, 1985

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SECTION I
INTRODUCTION

SECTION 1

OIS 40/50/60 WORKBOOK INTRODUCTION

This board repair workbook is comprized of two volumes. In the first volume the overall system will be covered in general. Then the reader will be presented with theory of operation for the three main circuit boards within the system, the Resource Management Unit (RMU), the Resource Control Unit (RCU), and the Internal Workstation Controller (IWS). Each of these sections will include a detailed description of the circuit board with limited bit chasing. The reader will be referred to Figures and Tables, along with references to the schematics to help him or her understand the operation of the unit. At the end of each section there is a quiz covering the information that was presented. After answering the questions in the quiz the reader can check his or her answers by referring to the answers in Appendix G.

In the second volume the reader will be presented with a detailed description of the theory of operation for the Internal Printer Controller (IPC), and the Internal WISE Controller (IWISE) circuit boards. The organization of the second volume is similar to that of the first as far as type of content and objectives.

Both volumes contain Appendices that provide relitive infromation about the circuit boards within that volume. Also located in the rear of the each volume is a master index that covers both volumes, this should provide the reader with a quick reference to just about any circuit operation.

If after you read this book you have any further questions or are interrested in learning more about the operation of the system, a list of reference books is provided in Appendix A of volume 1.

If while you are reading this workbook you come accross any errors that you feel need correcting, fill out the form provided at the back of the book and subbmit it to you supervisior. This feed back will help us improve the quality of the books that we produce and improve the quality of training that you receive.

1.1 OIS 40/50/60 SYSTEM INTRODUCTION

The OIS 40/50/60 system is a smaller version of the OIS 140 system that is contained in one package. The OIS 50 is capable of supporting up to four non-intelligent workstations and one or two non-intelligent printers. The logic providing the intelligence of these workstations and printers resides within the OIS 50 Master Processor. In addition the system will support up to four OIS 928 type serial devices, including intelligent workstations, image printers, phototypesetters, and telecommunication devices. The OIS 50 may be connected in a network configuration to more powerful Office Information Systems through the use of a Wang Inter-System Exchange Unit (WISE).

The OSI 40 is essentially a subset of the more versitile OIS 50. It was designed to be used as a stand alone system, capable of supporting one non-intelligent workstation along with one non-intelligent printer. As an option the OIS 40 may be configured to support one 928 type serial intelligent workstation or device. Like the OIS 50, it may be connected in an office system network via WISE, and has optional telecommunications capability.

The OIS 60 system represents the latest design in the OIS family of WANG Office Information Systems. In addition to the features of the OIS 40/50 configurations the OIS 60 provides four additional standard 928-type serial data link ports enabling the system to support a total of 12 peripheral devices, eight of these could be workstations. To support the additional ports the Resource Management Unit (RMU) and the Resource Control Unit (RCU) PCA's have been modified. The applicable theory and maintenance information (differences) for each will be covered as the RMU and RCU boards are discussed.

All three system contain an onboard 5 1/4 inch floppy archive drive, and either a 10 Meg or 30 Meg Winchester disk drive. The OIS 40 and 50 contain 10 Meg Winchester drives while the OIS 60 has a 30 Meg Winchester drive. In addition the OIS 60 has a hinged rear panel for easier access to the internal cabling for troubleshooting purposes.

The front panel of each of the units contains a rocker switch used for selecting which drive the unit will IPL from, (i.e. the Winchester or the Floppy). Directly above the IPL switch is located a LED status display. When the system is first powered on the unit will run an onboard BIT diagnostic. If an error is detected during the BIT test the status display will reflect the type of problem found. Refer to Appendix zzz for a complete list of error codes and their meaning.

1.2 SYSTEM OPERATION

In the OIS 40/50/60 system there are six printed circuit board that reside in the Master Processor, they are:

BOARD #	DESCRIPTION	SYSTEM
210-8266-A	Resource Management Unit (RMU)	((OIS 40/50))
210-8490-A	Resource Management Unit (RMU)	((OIS 60))
210-8267-A	Resource Control Unit (RCU)	((OIS 40/50))
210-8267-B	Resource Control Unit (RCU)	((OIS 60))
210-8274-A	Internal Workstation Controller (IWS)	((OIS 40/50/60))
210-8280-A	Internal Printer Controller (IPC)	((OIS 40/50/60))
210-8270-A	Internal WISE Controller (IWISE)	((OIS 40/50/60))
210-8269	OIS 50 Motherboard	((OIS 40/50/60))

The OIS motherboard is designed to hold a total of seven printed circuits boards, two of these boards must be the RMU and RCU boards. These two board contain all the Central Processing Logic for the Master unit. The five remaining slots accommodate the different peripheral controller boards in various combinations. Four of these slot may contain Internal Workstation Controllers (IWS), while the last slot may contain either an Internal WISE Controller (IWISE) or Internal Printer Controller (IPC). Depending on the system configuration, an additional IPC board may be substituted for one of the IWS controllers. FIGURE 1-1 shows a simplified block diagram of the OIS 40/50/60 system depicting the RMU, RCU, IWS,IPC and IWISE controllers, floppy and Winchester storage, and various peripheral devices. The flow of information between the various devices and PC boards occurs on the 50BUS. This bus is comprised of 40 signals representing address, data, select, and control information.

All of the Central Processing Logic for the OIS 40/50/60 is contained on the Resource Management Unit (RMU) and the Resource Control Unit (RCU) circuits boards. The Resource Management Unit (RMU) as its name implies, is responsible for the overall management of system operations. It runs the Operating System code and contains the system's main memory. The Resource Control Unit (RCU) shares the processing burden by controlling some of the more cumbersome tasks. In this way the RCU relieves the RMU of certain time-consuming operations, thus freeing the RMU to concentrate on overall system management. The net result is a system that runs faster and more efficiently than single-processor systems.

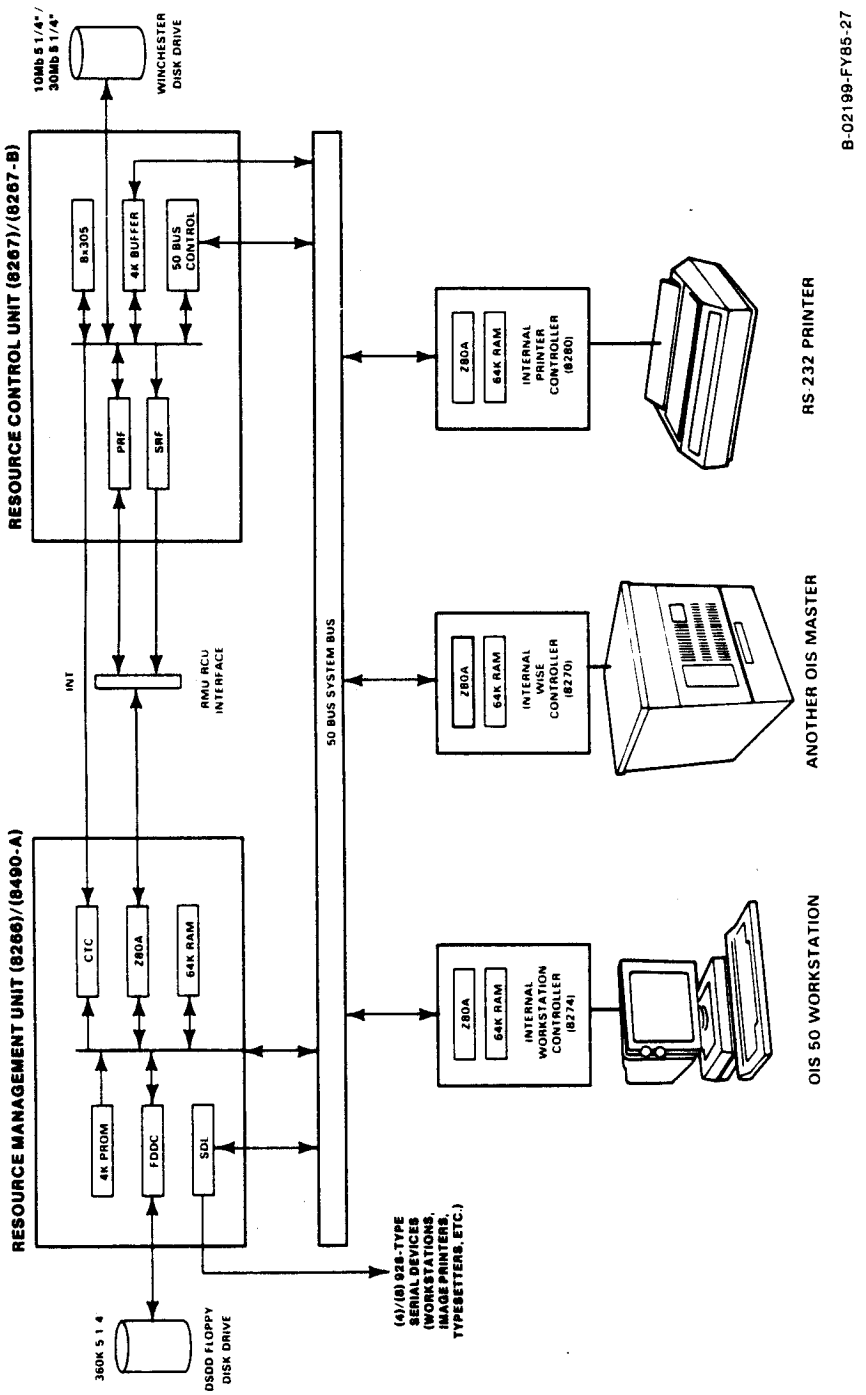


FIGURE 1-1
OIS 40/50/60 Simplified Block Diagram

1.2.1 Resource Management Unit (RMU)

The RMU contains a Z80 microprocessor that executes the system operating code, also on the RMU is located 64K of RAM overlayed by 4K of PROM memory. The RAM functions as main memory for the system, while the PROM contains the BIT power-up diagnostics and bootstrap loader code. The upper 256 bytes of memory is reserved Memory Mapped I/O. A Z80 Counter/Timer Chip (CTC) handles the various interrupts that the Z80 must respond to. The RMU is also responsible for controlling all operation involving the system's mini-floppy disk drive. An LSI Floppy Disk Controller chip (FDDC) resides on the RMU for this purpose. Finally, the RMU also contains all transmit and receive logic for all the external Serial Data Link (SDL) ports that connect the OIS 40/50/60 to 928-type serial peripherals. Although this SDL logic resides on the RMU board the RCU is actually responsible for its control.

1.2.2 Resource Control Unit (RCU)

The RCU board is designed around a Signetics 8X305 Microcontroller chip. It relieves the RMU's Z80 of a good deal of overhead by assuming the processing duties in four main areas:

1. Control and execution of all operations involving the 5 1/4" Winchester Disk Drive.

2. Execution of all block data transfers.

3. Control and arbitration of the 50BUS System Bus.

4. Control and execution of the Serial Data Link (SDL).

The 8X305 Microcontroller is the heart of the RCU board, and operates from instructions stored in firmware. A 4K Data Buffer is located on the RCU, and is involved in any operation that requires the transfer of block data. Logic on the RCU board generates commands and control signals that governs the operation of the 50BUS. Finally, all Serial Data Link (SDL) operations are under direct control of the 8X305 Microcontroller and additional support logic, even though the actual SDL transmit and receive circuitry is on the RMU.

In a multi-processor system such as this, communication between the two microprocessors is an important aspect of the system design. The RMU's Z80A and the RCU's 8X305 Microcontroller communicate with one another through the use of shared memory and interrupt signals. Two special memory areas are present on the RCU board. Both the Z80A and the 8X305 Microcontroller can access these locations. One area is called the Parameter Register File (PRF) while the other is labeled the Status Register File (SRF). When the Z80A of the RMU encounters and instruction that is the responsibility of the RCU, it will instruct the RCU to perform the task. To do this the RMU will write commands and parameter information into the Parameter Register File. The RCU then reads the (PRF) and interprets and executes the commands. When the RCU completes the task it writes status information into the Status Register File. The RMU reads the status information from the (SRF) to determine the outcome of the operation. For lengthy RCU operations such as block transfers the RMU will attend to other management duties while the RCU carries out the operation. When the RCU completes the task it will generate an interrupt to the Z80A indicating that the operation is complete.

As mentioned earlier, the 50BUS is the system's internal bus network comprised of 40 signals representing address, data, select, and control information. All information exchanged between the OIS 40/50/60 Central Processing Logic (RMU, RCU) and the various peripheral controllers (IWS, IPC, IWIS) travel on the 50BUS. The RCU initiates and governs all 50BUS transactions. Via the 50BUS the RCU is able to exchange information with a total of eight logical devices, called 50BUS Devices. Three of these logical devices reside on the RMU board:

1. Main Memory
2. The Floppy disk drive controller
3. The Serial Data Link transmit and receive logic

The remaining five logical devices correspond to the five Motherboard slots which house the various peripheral controller boards (IWS, IPC, IWISE).

A typical 50BUS transaction between the RCU and a 50BUS Device usually involves the transfer of block data. Consider the following example: While running the operating system, the RMU determine that it needs to read a portion of the workstations memory. Since the operation involves use of the 50BUS, and the RCU is responsible for operation of the 50BUS then the RMU instruct the RCU to perform the task and supplies the RCU with the particulars (which IWS, what portion of memory to read from, etc.) by writing to the (PRF). The RMU then goes about doing other housekeeping duties while the RCU performs the task. Using the 50BUS, the RCU selects the desired slave and places the slaves Z80A into a Bus-Request state so a DMA operation can take place. Then the RCU reads the desired slaves memory and transfers it byte for byte into the 4K Data Buffer on the RCU board via the 50BUS. When the operation is complete the RCU notifies the RMU by an interrupt. The RMU will then read the (SRF) to determine the results of the operation.

Three type of peripheral controller boards may be included in an OIS 40/50/60 system. They are; the Internal Workstation Controller (IWS), Internal Printer Controller (IPC), and the Internal WISE Controller (IWISE). Each of these controller boards contain a Z80A microprocessor along with 64K bytes of RAM used as slave memory. The following paragraphs contain a brief description of each board's responsibilities.

1.2.3 The Internal Workstation Controller (IWS)

The OIS 40/50/60 Master is capable of supporting up to four OIS 40/50/60 non-intelligent display terminals. The workstation is termed non-intelligent because the hardware and software that control the logical functions reside within the OIS 40/50/60 Master, on an (IWS) Controller board. The IWS Controller is responsible for providing:

1. The interface signals to the monitor electronics.
2. The interface logic to the serial keyboard.
3. The CRT, font, and main memory storage.
4. Interface logic required to communicate with the 50BUS.

1.2.4 The Internal Printer Controller (IPC)

The Internal Printer Controller (IPC) is designed to control a single RS-232C printer. The IPC receives commands and data from the RCU board via the 50BUS and communicates with the printer through an RS-232C serial interface. It is designed around a Z80A microprocessor running at 4 Mhz, and contains:

1. 50BUS interface logic.
2. RS-232C interface logic.
3. Printer control interface logic.
4. 64K of Dynamic RAM

1.2.5 The Internal WISE Controller (IWISE)

The internal WISE board provides a high speed communication path between the OIS 40/50/60 and any other WANG system that employs the standard 928-type Serial Data Link. The IWISE enables the OIS 40/50/60 to be used as clustered system, providing a communication link to a higher level Master Processor, such as the OIS 145 shown in FIGURE 1-1. Like the other controller devices attached to the 50BUS, the IWISE board depends on a Z80A running at 4 Mhz, and also contains:

1. Serial Data Link protocol logic.
2. 50BUS protocol logic.
3. 64K of Dynamic RAM and memory access arbitration logic.
4. DMA logic.

A complete theory of operation, and detailed circuit description for each of the circuit boards in the OIS 40/50/60 system is discussed in the following sections. Appendix A gives a complete list of all related documents for the OIS 40/50/60 system.

SECTION 1 QUIZ

1) What are the major differences between an OIS 50 and an OIS 60?

2) Name the five PCA assemblies that can reside in the main unit of either of the systems?

3) What two controller circuits reside on the RMU but are primarily controlled by the RCU?

4) In what four main areas does the RCU assume processing duties for the RMU?

5) What two memory areas do the Z80A and the 8X305 use to communicate with each other?

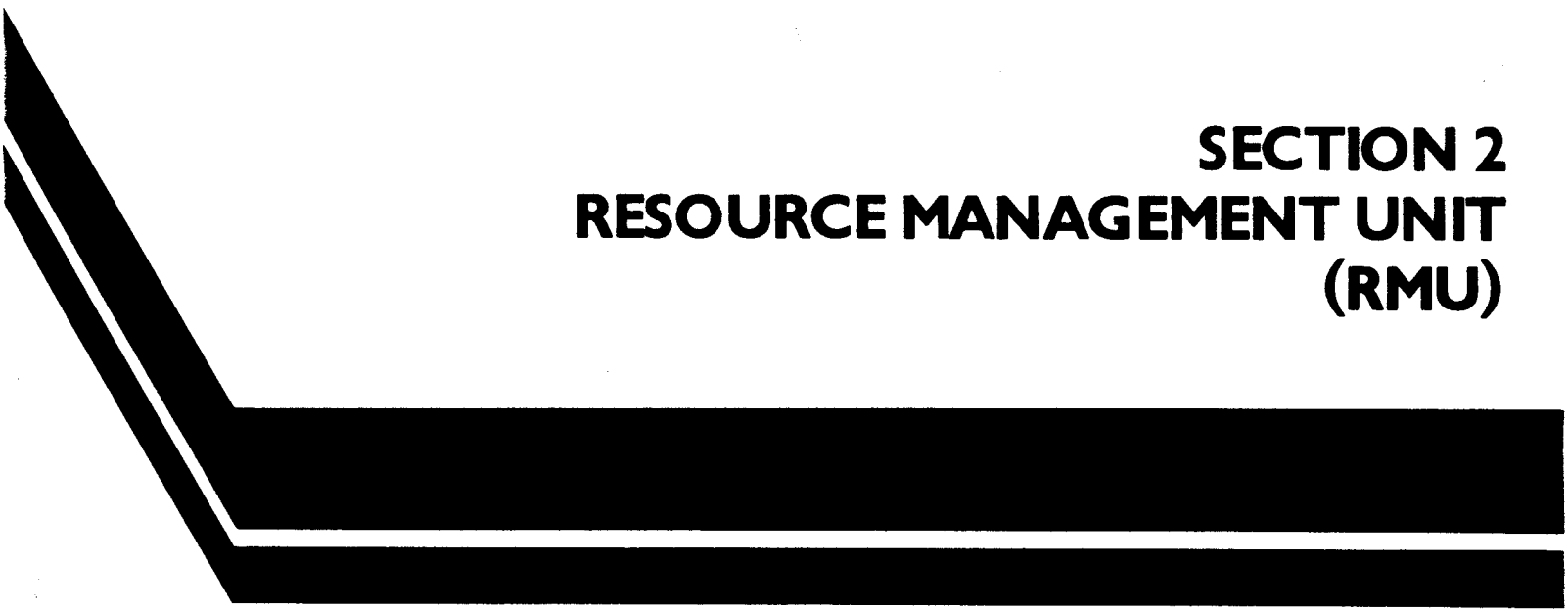
6) Who initiates and governs all 50BUS transactions?

7) What four items is the Internal Workstation Controller (IWS) responsible for?

8) How many printers can be connected to an Internal Printer Controller (IPC)?

9) What type of interface does the Internal WISE Controller (IWISE) require to communicate with other units?

10) Which Appendix contains a listing of reference materials that may be read to provide a better understanding of the OIS 40/50/60 system.



SECTION 2
RESOURCE MANAGEMENT UNIT (RMU)

SECTION 2

Resource Management Unit (RMU)

2.1 Resource Management Unit (RMU)

In this section we will discuss the theory of operation and circuit description for the Resource Management Unit (RMU). In lue of the fact that the RMU can not operate completely by itself, parts of the RCU circuits will also be discussed throughout this section.

While reading this section you should refer to the schematics in Appendix E so that you can follow along with the descriptions given. All circuit components will be referred to by their chip number and schematic location; Example L4 (1B2) indicates chip L4 located on sheet 1 row B column 2. If you are unfamiliar with a pectular type of chip that is being discussed you should refer to either the manufactures specification sheet or to the TTL Data Book by Texas Instruments. A quick reference of all the chips in the OIS 40/50/60 system is located in appendix C, each chip is listed by number and a brief description of its operation in the circuit is given. This Appendix is divided into parts representing each of the circuit boards located in the OIS 40/50/60. I recommend that you turn to Appendix C now and take a quick look at the listings.

Throughout the description of the circuits I will be using mnemonics to describe different signals that are generated. A complete listing of the meaning of these mnemonics are given in Appendix B. Any mnemonics that are active low and are indicated in the schematics by having a bar over the top will be prefixed in this document be an ampersand (&). Some signal have dual functions, such a R/W which when active low indicates a read operation and when active high indicates a write operation. To indicate which part of the mnemonic is active low I will place an additional ampersand next to the portion of the mnemonic that is active low, (i.e. &&R/W will represent the above description whereas R/W&& would indicate the reverse situation).

The 8266 Resource Management Unit used in the OIS 40/50/60 processor-based data processing system contains the 4-MHz Z80A Processor; the Counter Timer Chip, which generates interrupts and acts as a time-of-day clock; and the NEC765 Floppy Disk Controller (FDC), which manages operations involving the system's Floppy Disk Drive (FDD). (The 8X305 Microcontroller, the second processor of the OIS 50 multiprocessor system, is located on the 210-8267 Resource Control Unit board.) FIGURE 2.1-1 is a block diagram of the Resource Management Unit, and FIGURE 2.1-2 illustrates the Resource Management Unit's relation to the OIS 40/50/60 system.

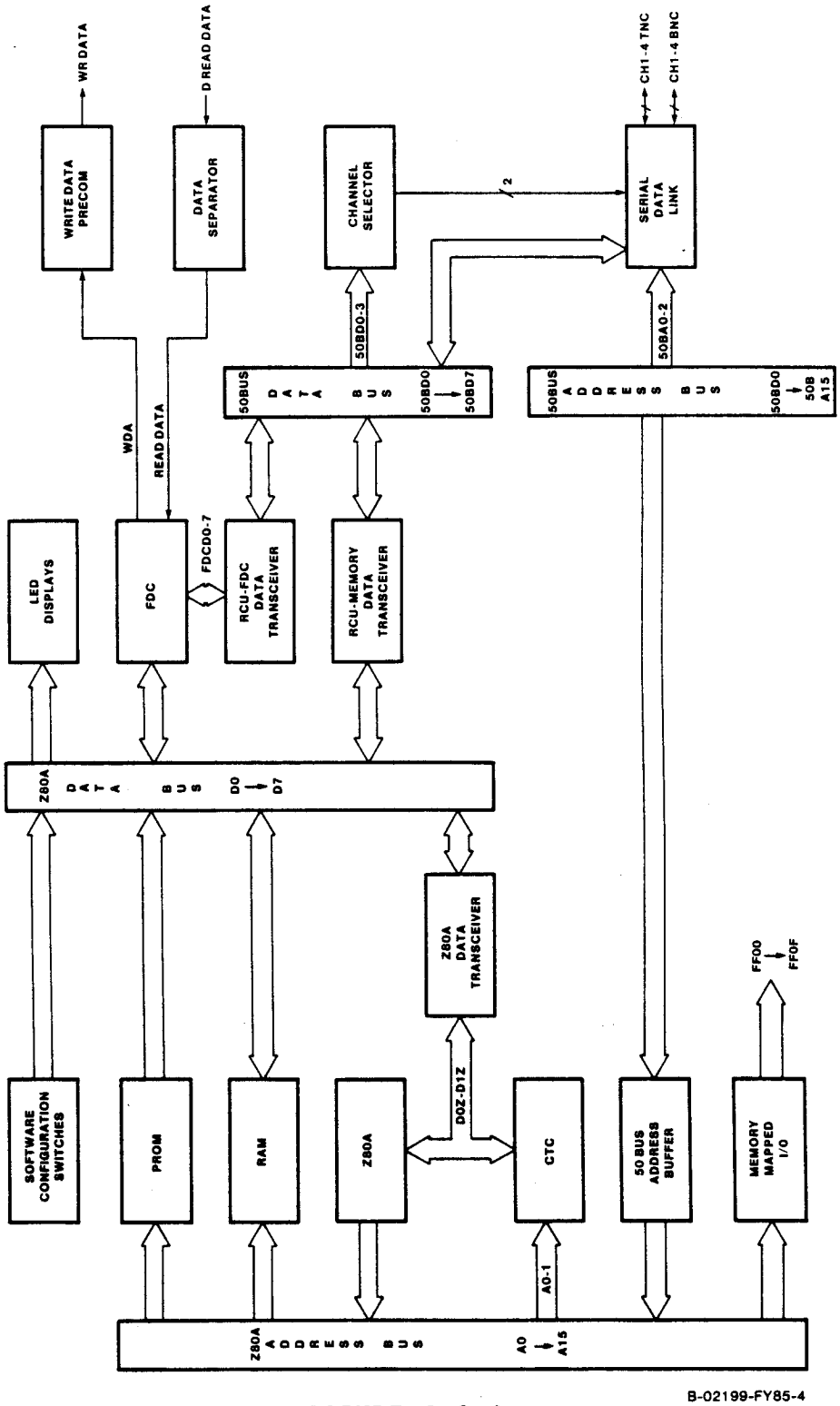


FIGURE 2.1-1
Block Diagram of the Resource Management Unit

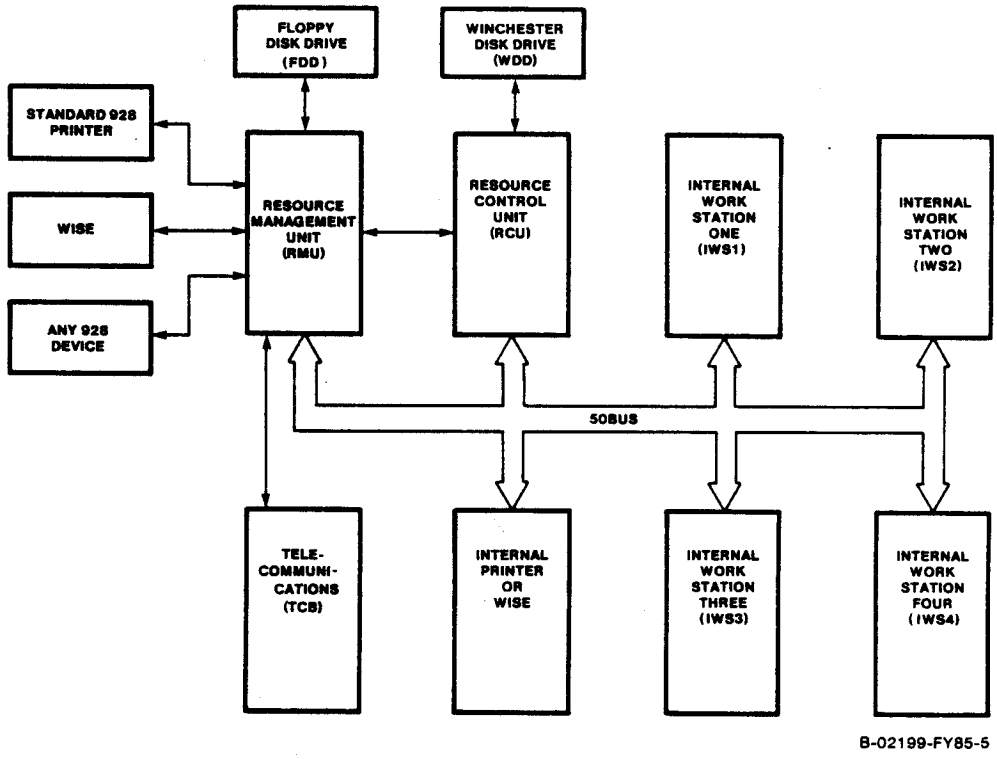


FIGURE 2.1-2
OIS 50 Block Diagram

Memory support for the OIS 40/50/60 is located on the Resource Management Unit (RMU) and is divided among RAM, PROM, and Memory Mapped Input/Output (MMI/O). Sixty-four kilobytes of RAM and 4k bytes of PROM are available for power-up diagnostics and Initial Program Load (IPL). Memory addresses from 1000-FF00 are used as random access memory, with the lower 4k bytes (0000-0FFF) overlayed by PROM. Memory addresses from FF00-FFFF are reserved for MMI/O.

The RMU board also contains serial transmit and receive logic for external Data Link ports 1-4. However, the 8X305 Microcontroller on the Resource Control Unit (RCU) board maintains control of these ports.

RMU-RCU Interaction

RMU-RCU communication involves shared memory, a Command Notification Bit (CNB), and the 8X305 Microcontroller interrupts that assert the Z80A. Two memory areas on the RCU board are shared between the Z80A and the 8X305: the 16-byte Parameter Register File (PRF) and the 12-byte Status Register File (SRF). Both the Z80A and the 8X305 can read from or write to the PRF; they cannot, however, access the PRF simultaneously. Only the Z80A can read the SRF, and only the 8X305 can write to it.

The RCU decodes RMU requests via the Parameter Register File. The Z80A microprocessor in the RMU loads the PRF with the command codes and data that the RCU needs to perform a specific operation. When the Z80A sets the Command Notification Bit, the 8X305 operates on the PRF as needed to complete the command. (Generally, the 8X305 moves the PRF data to its scratchpad RAM and then releases the PRF.) The PRF must be released quickly because the Z80A is suspended (ie, held in a bus request state) while the 8X305 uses the PRF.

PRF byte assignments depend upon the function requested (see Appendix G). Typically, the Z80A issues the FF20 (Command Request) byte and the FF22 (Specify Command) byte to the PRF. The RCU reads the bytes and defines the remaining bytes according to specific command requirements and then returns the FF21 (Command Acknowledge) byte to the PRF for the Z80A to read. To avoid invalid parameter errors, unused or undefined bytes should always be cleared to zero.

To perform a function that involves the RCU, the Z80A loads the command code and necessary data into the PRF. The Z80A then writes to address FF30 to issue the Command Notification Bit that initiates the command. Normally, the 8X305 is polling, waiting for the Command Notification Bit to be set. When the RMU issues a command, the 8X305 can perform one of two routines. If the command is an immediate command, the Z80A is awaiting command completion and the RCU must, therefore, execute the command immediately. If, however, the command is a non-immediate command, the RCU defers the command until it has completed any immediate operation in progress.

Upon receiving an immediate command, the RCU validates the command code, copies the PRF to its scratchpad RAM, completes the requested operation, and releases the RMU. Upon receipt of a non-immediate command, the RCU validates the command code, copies the PRF to its scratch RAM, sets RCU Busy status in the SRF, releases the RMU, completes the requested operation, and issues either an interrupt request or a Control Unit Busy (CUBUSY) signal to the RMU when the operation has been completed.

When the 8X305 Microcontroller performs a 1-byte operation, it does not immediately release the PRF. The Microcontroller holds the Z80A in a suspended state for a maximum of 1 ms (otherwise the lack of dynamic RAM refresh could cause a memory data loss). When the 8X305 releases the Z80A, the data and/or status from the 1-byte operation is immediately available to the Z80A via the SRF.

Status and error information returns to the RMU via the dual-ported SRF. When the 8X305 is busy, RCU Busy status information is set in byte FF10 of the SRF. Status information concerning Data Link block operations resides in SRF bytes FF11 and FF12. SRF bytes FF13-FF15 contain status information about the 1-byte Data Link opera- tions, and bytes FF16-FF1B contain status information concerning the Winchester Disk Drive (WDD).

2.1.1 Controls and Indicators

Two 7-segment displays (L3 and L4, located on the top edge of the RMU board and visible through the front bezel of the OIS 40/50/60 cabinet) indicate various errors. Error codes are displayed to indicate errors detected during power-up diagnostics or system errors (such as operator errors) detected after the operating system has taken control. Inverted data bits /D0-7 drive the LEDs, the data bits are inverted through L8 (1G3) and then supplied to drivers L5 (1G2) (activated by /FF08 write command) and L6 (1G1) (activated by /FF09 write command). L5 drives the L4 (1B2) lower display, and L6 drives the L3 (1B1) upper display.

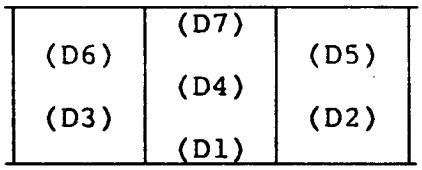
All seven display segments light up momentarily when power is applied to the OIS 40/50/60. The LEDs do not remain on long enough to be seen, however, and their lighted condition can be verified only with a Zebug (to establish that all LEDs are functioning correctly). Power-up LED illumination is created by the trailing edge of the /MR signal as it clocks the L4 and L5 drivers via L26 (1F3) while bits D0-7 are high.

Table 2.1-1 shows the codes used on bits D0-7 to create each hexadecimal symbol on the display. Table 2.1-2 lists the display error codes for power-up diagnostics and the error condition indicated by each symbol. Table 2.1-3 lists the display error codes for system errors and the error condition indicated by each code.

Switch SW2 is a pushbutton Restart Control Switch located on the interior of the OIS 40/50/60 cabinet on the front edge of the RMU board. If the operating system has control, activating SW2 generates a Non-Maskable Interrupt (NMI) to the Z80A. The NMI traps the Z80A to the Master Debugger routine (if the system is configured with the Master Debugger). The Master Debugger routine is used exclusively as a development tool.

Activating the Restart Control Switch during Test 1 (the LED Test) of the power-up diagnostics causes the tests following Test 1 to be skipped and initiates the bootstrap routine. To prevent error message generation, bit 7 of the Software Configuration Switches should be open prior to activating SW2 during Test 1. Activating SW2 with bit 7 open normally allows a smooth transition into the bootstrap routine.

In Table 2.1-2, "fatal*" next to an error indicates that the program cannot "continue on error" (not even when using the special DIP switch settings described in Table 2.1-4). "Fatal**" indicates that the encountered error halts the power-up sequence; however, tests can continue with the use of the DIP switch settings shown in Table 2.1-4. The test number is shown on the upper display, and the error number is shown on the lower display.



(D0) = decimal point

DISPLAY	CODE (HEX, without decimal point)	CODE (HEX, with decimal point
0	EE	EF
1	48	49
2	BA	BB
3	B6	B7
4	74	75
5	D6	D7
6	DE	DF
7	A4	A5
8	FE	FF
9	F4	F5
A	FC	FD
B	4E	4F
C	CA	CB
D	3E	3F
E	DA	DB
F	D8	D9

Table 2.1-1: LED DISPLAY CODES

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES

TEST NUMBER	TEST NAME	ERROR NUMBER
0	LED SEGMENT DISPLAY TEST Visual Feedback for Error Detection	
1	CTC TEST Read/Write Miscompare Down Count Failure	 (fatal**) 1 (fatal**) 2
2	UPPER RAM TEST Data Error (fatal**) Parity Error (fatal**) Parity Status Register Error Non-Maskable Interrupt (NMI) Error	 0-7 P (fatal**) PS (fatal**) P8
3	PRF TEST RCU Busy (loops until ready) RCU Command Response to RMU Command Not Accepted Command Invalid Incomplete Command Accepted None of the Above PRFs Affected	 (fatal*) .d (fatal*) .0 (fatal*) .1 (fatal*) .2 (fatal*) .3 (fatal*) .P

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES (cont.)

4	CTC TEST		
	CTC Not Interrupting (Channels 0-3)	(fatal**)	1
	Incorrect Vector	(fatal**)	2
.4	FDD DEADMAN TIMER TEST		
	No Interrupt (fatal**)	1	
	Incorrect Vector	(fatal**)	2
	Interrupt Not Caused by Deadman Timer	(fatal**)	3
	Floppy Disk Controller Has Interrupt Pending	(fatal**)	4
5	RCU INTERRUPT TEST		
	RCU Busy (loops until ready)	(fatal*)	.d
	RCU Response Bad on Block Write Command	(fatal**)	1
	Vector Error (fatal**)	2	
	No Interrupt Created	(fatal**)	3
.5	WINCHESTER DEADMAN TIMER TEST		
	RCU Busy (loops until ready)	(fatal*)	.d
	No Interrupt Requested	(fatal**)	1
	Vector Error	(fatal**)	2
	Drive Not Selected	(fatal**)	3
	Indexing Stuck Off	(fatal**)	4
	Indexing Stuck On	(fatal**)	5
6	SET SLAVE LIST		
	RCU Busy (loops until ready)	(fatal*)	.d
	RCU Command Response to RMU		
	Command Not Accepted	(fatal*)	.0
	Command Invalid	(fatal*)	.1
	Incomplete Command Accepted	(fatal*)	.2
	None of the Above	(fatal*)	.3
7	MAP SLAVE STATUS		
	RCU Busy (loops until ready)	(fatal*)	.d
	RCU Command Response to RMU		
	Command Not Accepted	(fatal*)	.0
	Command Invalid	(fatal*)	.1
	Incomplete Command Accepted	(fatal*)	.2
	None of the Above	(fatal*)	.3

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES (cont.)

	The following error numbers are displayed for about one second, but do not prevent continuation of testing.		
	1-Byte Data Link Status (DLS) 1-Byte Slave Status (SS) CPE Detected by DLS and SS CPE Detected Only by SS MPE Detected by DLS and SS MPE Detected Only by SS Detected by Data Link Status Received Parity Error No Data Timeout Check Power-Up State If slaves are not available, display error and loop on test.		.4 .5 .6 .7 .8 .9 .P .F
8	SLAVE CONTROL WRITE SECTION RCU Busy (loops until ready) RCU Command Response to RMU Command Not Accepted Command Invalid Incomplete Command Accepted None of the Above	 (fatal*) (fatal*) (fatal*) (fatal*) (fatal*)	 .d .0 .1 .2 .3
	The following error numbers are displayed for about one second, but do not prevent continuation of testing.		
	1-Byte Data Link Status (DLS) 1-Byte Slave Status (SS) CPE Detected by DLS and SS CPE Detected Only by SS MPE Detected by DLS and SS MPE Detected Only by SS Detected by Data Link Status Received Parity Error No Data Timeout Check Power-Up State		 .4 .5 .6 .7 .8 .9 .P
.8	READ SECTION RCU Busy (loops until ready) RCU Command Response to RMU Command Not Accepted Command Invalid Incomplete Command Accepted None of the Above	 (fatal*) (fatal*) (fatal*) (fatal*) (fatal*)	 .d .0 .1 .2 .3

Table 2.1-2: POWER-UP DIAGNOSTIC DISPLAY ERROR CODES (cont.)

	The following error numbers are displayed for about one second, but do not prevent continuation of testing.	
	1-Byte Data Link Status (DLS) 1-Byte Slave Status (SS) CPE Detected by DLS and SS CPE Detected Only by SS MPE Detected by DLS and SS MPE Detected Only by SS Detected by Data Link Status Received Parity Error No Data Timeout Check Power-Up State Compare Data to Correct Data	 .4 .5 .6 .7 .8 .9 .P .E
	If slaves are not available, a loop back to Test 7 is performed until a slave passes the test.	
	COMPARE DATA ERROR Register Contents: H - Data Received C - Data Expected D - XOR Data E - Slave Number L - Low Address	
9	IPL TEST FLOPPY DISK DRIVE I/O Error Addressed Drive Is Not Ready (loops on drive if not ready) WINCHESTER DISK DRIVE I/O Error Addressed Drive Is Not Ready (loops on drive if not ready)	 (fatal*) 1 2 (fatal*) .1 .2
	"UP" is displayed for approximately 1 s after successful completion of all power-up tests. Control then passes to bootstrap program.	

Table 2.1-3: SYSTEM DISPLAY ERROR CODES

Display Error Code (Hex)	Error Condition
FF	Parity
FE	Restart
FD	Software Debugger
FC	Hardware Debugger
FB	I/O Error Reading Master or Volume Label
FA	Illegal PROM Address
F9	Parity and Illegal PROM Address
DC	PROM Revision Levels Not Compatible
DD	No RCU Response
DE	XMM Configured for 64k Master
DF	Data Link Error During I/D Transfer (XMM)
E0	Invalid Volume Label (Hash Code)
E1	Not System Disk
E2	Bad Configuration - Too Little Memory
E3	Bad Configuration - System Disk Excluded
E4	Insufficient Memory for Control Blocks (TCB)
E5	Insufficient Memory for Control Blocks (VCB)
E6	Insufficient Memory for Control Blocks (DCB)
E7	Insufficient Memory for Control Blocks (FCB)
E8	Unsupported Disk Type
E9	Insufficient Memory for Buffers (VAU Map)
EA	Insufficient Memory for Buffers (Catalog)
EB	Incorrect PROM Installed
EC	Unsupported Timer Interval
ED	Cannot Mount System Disk
EE	Invalid SMD/CMD Characteristic Switches
EF	Invalid IPL Sector

IPL Device Select Switch SW1 is a rocker switch located on the OIS 40/50/60 control panel. When read by the /FF04 command, SW1 selects either the Floppy Disk Drive or the Winchester Disk Drive as the system drive for initial program loading. When SW1 is in position 3, D7 is cleared to 0 and the Floppy Disk Drive is selected to IPL the system; when SW1 is in position 1, D7 is set to 1 and the Winchester Disk Drive is used to IPL the system.

SW3 is an 8-bit switch bank used to select various software configurations during the power-up sequence. SW3 switch settings define, via data bits D0-7, which software configurations run on the OIS 40/50/60. Switch settings are passed through the L49 Software Configuration Switch Buffer when the /FF05 command is activated. The SW3 Software Configuration Switches, used only during power-up diagnostics, are sensed in the order listed in Table 2.1-4.

Table 2.1-4: SOFTWARE CONFIGURATION SWITCH SETTINGS

Switch Number	Function
7	Software configuration switch settings are of no significance to the built-in test unless this bit is set (ie, D7 = 1).
0	When cleared (D0 = 0), causes program to loop on power-up diagnostics.
1	When cleared (D1 = 0), causes program to stop on error.
2	When cleared (D2 = 0), causes program to loop on error.
3	When cleared (D3 = 0), causes program to continue on error.
4-6	Ignored by diagnostics.

Power-Up Protection

Power-Up protection circuitry (L131 (2F3-8), composed of four comparators) monitors the 5-V (pin 9), -5-V (pin 4), and 12-V (pin 7) power levels to ensure that the proper voltages are reached before the Z80A is released to place the OIS 40/50/60 into an operative mode. When the voltages are at their correct levels, the active &AUTO RESET signal from L131 pin 13 is deactivated, allowing the Z80A to begin operation. The &AUTO RESET signal is converted into the Master Reset (&MRC) signal and sent to the other boards of the OIS 40/50/60 system. &MRC holds each OIS 40/50/60 board reset until proper voltage levels are reached.

2.1.2 Clock Generation

Y1 generates the 16-MHz base timing signal (CK) from which the clock generation circuitry (L31 (1K2) and L32 (1I3/4), shown in FIGURE 2.1-3) creates all other clock signals used on the RMU board. L32 gate 1 divides the 16-MHz signal to create the 8-MHz 1/2Phi signal that synchronizes the generation of Z80A Data Bus direction control signals and the RAS signal. L32 gate 2 divides the 8-MHz signal to create the 4-MHz Phi-Z and Phi-ZC signals that drive the CTC and the Z80A processors. L31 gate 2 generates the /Phi-A signal used for FDC write timing and for the Z80A wait circuit. FIGURE 2.1-4 illustrates the relationship of the various clocking signals.

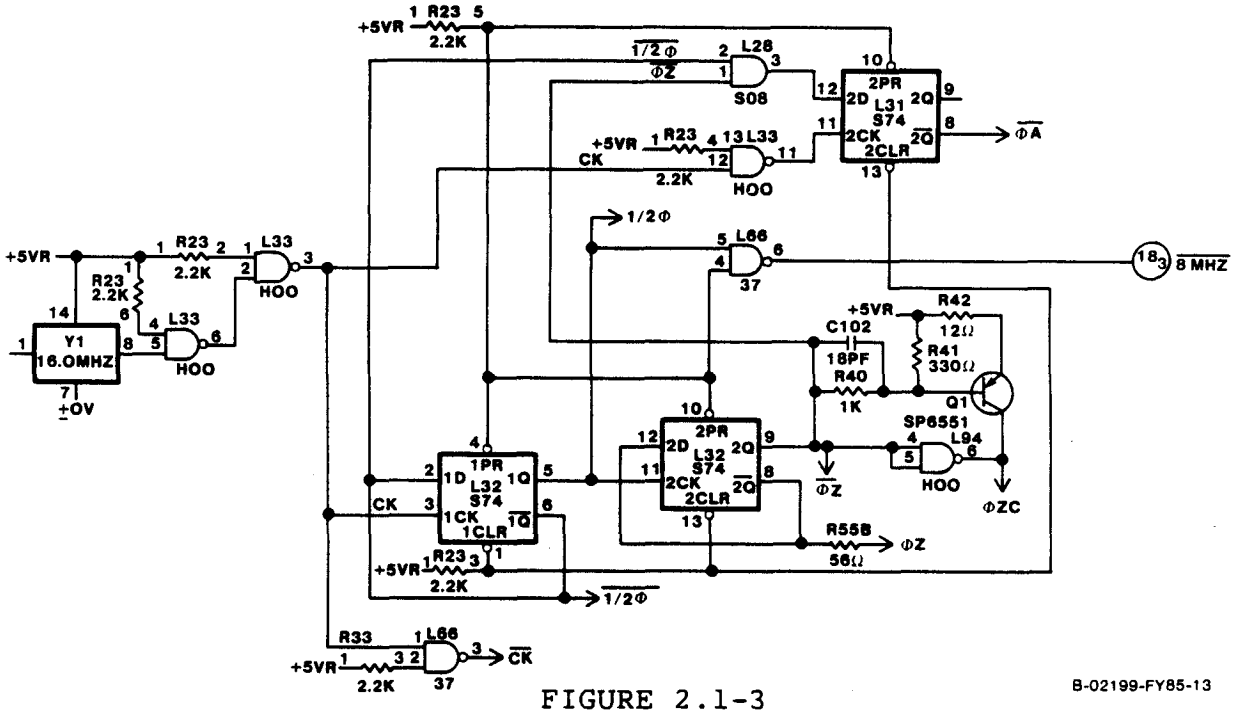


FIGURE 2.1-3
RMU CLOCK LOGIC

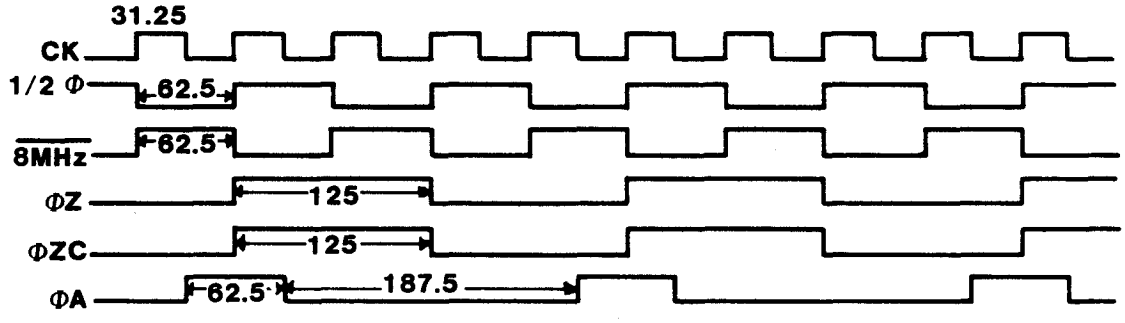


FIGURE 2.1-4
RMU TIMING

2.1.3 Memory Mapped Input/Output

Memory addresses FF00-FFFF are reserved for Memory Mapped I/O (MMI/O) operations. FF00-FF0F are decoded on the RMU board, and FF10-FF40 are decoded on the RCU board. MMI/O Decoder L80 on the RMU board decodes address bits A0-3 into I/O Port Commands /FF00-/FF0F (defined in Table 2.1-5). Address bits A4-15 are decoded through gates L64 (1J10) and L95 (1K11) to enable the MMI/O Decoder L80 (1J/K9). MMI/O Logic is shown in FIGURE 2.1-5.

The RMU MMI/O Decoder is enabled when address bits A8-15 are high and address bits A4-7 are low: A8-15 select a memory mapped operation, and A4-7 enable decoding of the RMU Memory Mapped I/O operation. Address bits A8-15 assert L95 to generate the Port Address (&PORTAD) signal from pin 8. The combination of &PORTAD and the &MREQ signal (which is active for any memory request operation) asserts L63 (1K10) to generate the &MMI/O enabling signal that asserts L80 pin 18. During MMI/O operations BUSAK is low on pin 5 of L63 to gate the &MMI/O signal through. BUSAK is applied at L63 to prevent an incorrect DMA address from generating an MMI/O operation. Low-order address bits A4-7 assert L64 to generate the second MMI/O Decoder enabling signal, which asserts L80 pin 19. If A4-7 are low, ports FF00-FF0F on the RMU board are decoded from A0-3; if A4-7 are high and the &MMI/O signal is active, ports FF10-FF2F on the RCU board are decoded.

During Memory Mapped I/O operations the Wait State Insert Flipflop (L31 (1K6)) generates the PWAIT signal to delay the Z80A by one complete WAIT State. The WAIT state allows time for propagation delays and for ports that have slow response times. PWAIT generation is initiated when the &MMI/O signal asserts L11 (1K6) to generate a signal that asserts L31 pin 2. When L31 is clocked by the /Phi-A signal it generates &PWAIT from pin 6. &PWAIT asserts the Z80A's &WAIT pin to insert the necessary WAIT state. PWAIT from pin 5 is fed back to hold L31 latched for one complete WAIT state.

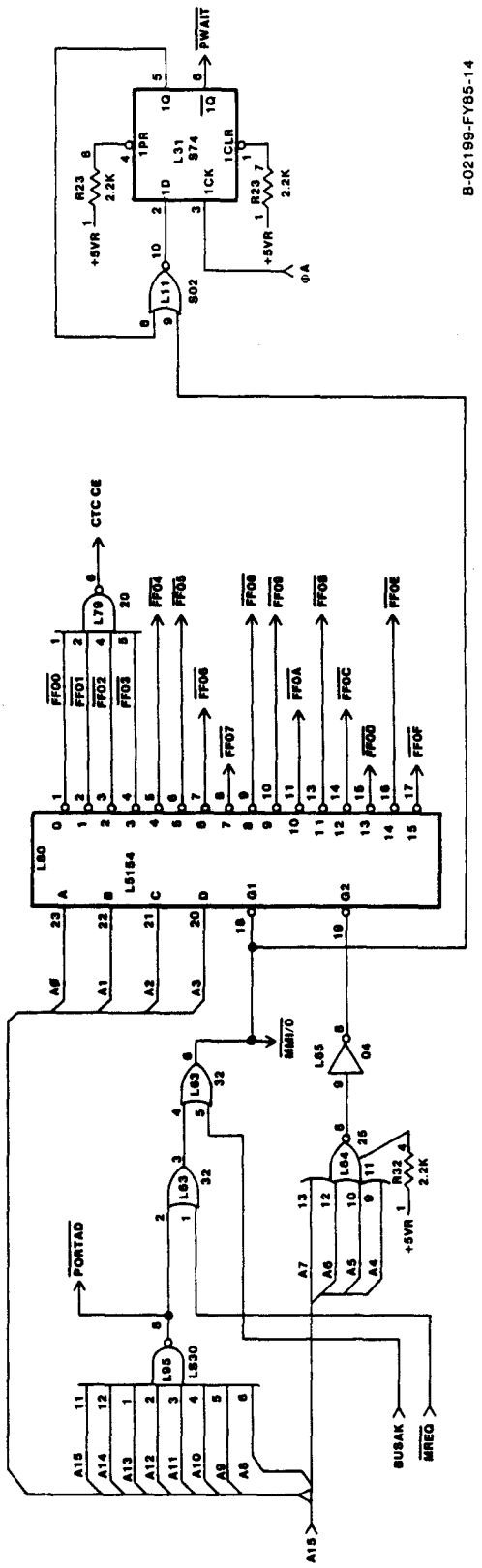


FIGURE 2.1-5
MMI/O Logic

When a command such as &FF0B is issued, it can be used to perform either a read or a write operation. To create individual signals for read and write operations the &FF0B signal is gated with the &RD1 and &WR signals at L108 (1F8), &FF0B asserts pins 9 and 13 of L108. In read operations, &FF0B is gated through L108 by the active &RD1 signal asserting pin 12 to create the &RFF0B signal from pin 11. In write operations, &FF0B is gated through L108 by the active &WR signal asserting pin 10 to create the &WFF0B signal from pin 8.

Table 2.1-5: RMU MEMORY MAPPED I/O COMMANDS

PORT COMMAND	DEFINITION
&FF00-&FF03	Writes Counter Timer Chip channels. Also writes interrupt vector, control word, and time constant assignments as follows: COMMAND CHANNEL &FF00 00 &FF01 01 &FF02 02 &FF03 03 Read CTC internal down counter of one of the four CTC channels.
&FF04	Read IPL Device Select Switch (SW1), which determines Disk Drive to be used for IPL. D7 = 0 - Floppy Disk Drive D7 = 1 - Winchester Disk Drive
&FF05	Read Software Configuration Switches (SW3) to define running software configurations.
&FF06	Read Floppy Disk Controller Status Register.
&FF07	Read Floppy Disk Controller Data Register (&RFF07). Write data to Floppy Disk Controller (&WFF07).

Table 2.1-5: RMU MEMORY MAPPED I/O COMMANDS (cont.)

&FF08	Write lights lower Error LED Display (see Tables 1-1, 1-2, and 1-3).
&FF09	Write lights upper Error LED Display (see Tables 1-1, 1-2, and 1-3).
&FF0A	Write resets Floppy Disk Controller Chip. Two &FF0A writes must be performed to software-specify a 10-us reset pulse. The first &FF0A issued turns the reset pulse on and the second &FF0A turns the pulse off. Reset pulse width must be at least 10 us.
&FF0B	Read Floppy Disk Drive Status Register (/RFF0B). D0 = 1 - File Ready. D1 = 1 - Disk Selected. D2 = 1 - Door Disturbed. (Cleared by &RFF0B when door is closed.) D3 = 1 - Deadman Timer Interrupt Pending. D4 = 0 - DMA Request Pending. D5 = 0 - Interrupt Request Pending. D6 = 0 - Not Used. D7 = 0 - Not Used. Write Floppy Disk Drive Motor Control and Drive Select (&WFF0B) data . D0 = 1 - Turn Floppy Disk Drive Motor On. D1 = 1 - Select Floppy Disk. D6 = 1 - Terminal Count Asserts Floppy Disk Controller. D7 = 1 - DMA Acknowledge Asserts Floppy Disk Controller.
&FF0C	Issued immediately after an FDD operation is sent to the FDC. Write sets the deadman timer and trips a 540-ms timeout that determines whether FDC is "frozen." Timeouts issue a Floppy Interrupt (FINT) signal to the CTC.

Table 2.1-5: RMU MEMORY MAPPED I/O COMMANDS (cont.)

&FF0D	Primarily used in diagnostics. Write controls parity (even or odd) written to memory. D6 = 1 - Prevents a memory error (&ME) from generating an NMI to the Z80A. D7 = 0 - Even Parity. D7 = 1 - Odd Parity.
&FF0E	Reads memory parity bit (&RFF0E). D7 = 1 - Parity Error. Write enables or disables access to diagnostic /IPL PROM (&WFF0E). PROM is mapped into memory locations 0000-0FFF. D7 = 0 - PROM Disabled. D7 = 1 - PROM Enabled.
&FF0F	Write clears RAM Parity Error Bit.

2.2 Z80A CENTRAL PROCESSOR UNIT

The Z80A Central Processor Unit (L114 (1E-J13)) resides on the 8266 Resource Management Unit board. When power is first applied, the active &AUTO RESET signal on L114 pin 26 automatically resets the Z80A. When the voltages are at their correct levels, &AUTO RESET is deactivated to allow the Z80A to begin operation.

Address lines from the Z80A are supplied to the L145 and L130 (1I/J13) Address Bus Drivers. When enabled by the inactive BUSAK signal, L145 and L130 gate the Z80A address lines onto the A0-15 Address Bus. Separate enabling and direction control logic controls Data Transceiver L115 (1G13), which controls the data flow to and from the Z80A. When enabled by an inactive &BUSAK signal, Control Line Driver L96 (1E12) drives the Z80A control signal outputs. Z80A access logic is shown in FIGURE 2.2-1.

2.2.1 Z80A CONTROL LINES

a. &BUSREQ (input)

The Z80A can be halted momentarily by either an active &BUSREQ (Bus Request) or &CMD BUSREQ (Command Bus Request) signal asserting pin 25. Requesting the Z80A bus forces the Z80A to relinquish bus control and, therefore, allows the RCU to gain control of the Z80A Data and Address Buses. The RCU generates two signal to the RMU when it requires the Z80A data and address bus, they are &5ØBSLCTØ and &5ØBUSREQ. These enter at 2K12 and are ORed together to generate &BUSREQ to the Z80A, and &BUSREQ also removes the preclear from L127 (2K10) so that the Z80A can generate a &5Ø BUSAK (bus acknowledge). Once the Z80A receives the bus request it will complete the operation that it is doing and then activate &BUSAK at pin 23 of the Z80A. This signal is then sent to L127 at 2K10 where it is placed on the "D" input. Then on the next phase Z clock L127 will set and generate &5Ø BUSAK to the RCU. When the Z80A activated the &BUSAK on pin 23 it also tristated its data and address bus. The Z80A can also be placed into this type of condition by the &CMDBUSREQ signal. The RCU generates the &CMDBUSREQ signal at 1J14 to directly request the Z80A buses after the Z80A has issued a command to the RCU.

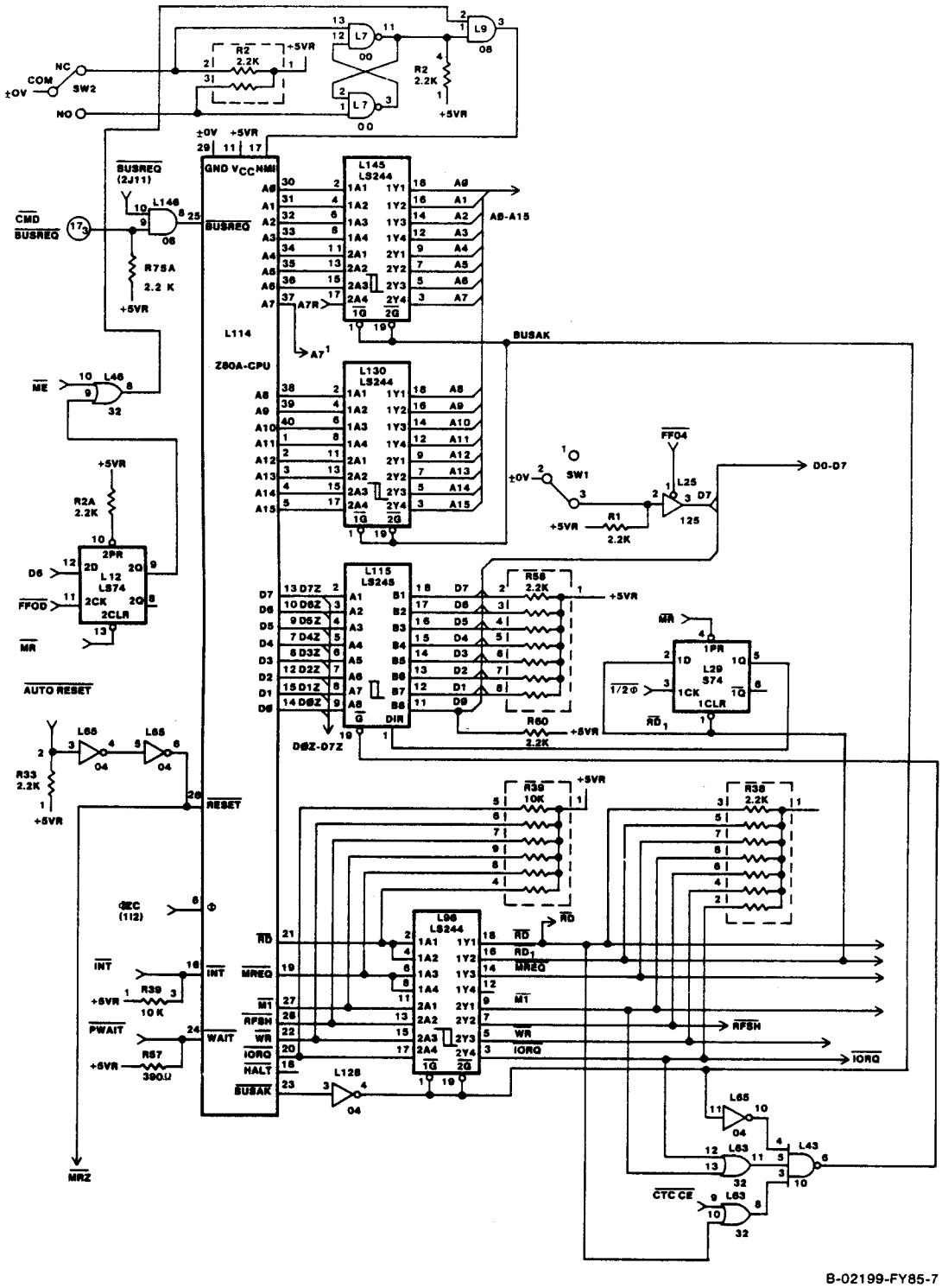


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FIGURE 2.2-1
Z80A Access Logic

b. Interrupts (input)

The Z80A can be interrupted by non-maskable interrupt (NMI) requests arriving on pin 17 or by maskable interrupt requests asserting pin 16. NMIs result either from memory errors or from activation of the Restart Switch. Maskable interrupts are generated by the CTC in response to either active &CUBUSY, &WSKCMP, or &FINT (&DMI) signals, or the programmable time-of-day clock.

1. NON-MASKABLE INTERRUPTS (input)

If during the reading of the RMU's main memory a parity error is detected the &ME will be sent to L46 at (1I14). This will be passed through as long as the system is not doing a MMI/O operation &FF0D with D6 high, (usually done during diagnostics). The active &ME signal will then be placed on pin 17 of the Z80A after it passes through L9 at (1K12).

The other source of nonmaskable interrupt is from SW2 the Restart Switch. Them SW2 located at 1K14 is depressed ground will be placed on the NO contact and force latch L7 (1K13) to place a zero pin 17 of the Z80A after passing through L9 (1K12). When SW2 is released latch L7 will change states and clear the MNI.

When the Z80A receives a NMI request on pin 17 it will ignore the next instruction that it fetches an jump directly to its hardware default address of ØØ66H. At this location there will be a restart routine that will determine where the interrupt came from. This will be discussed in more detail in the section on parity checking.

2. MASKABLE INTERRUPTS (input)

The Z80A receives maskable interrupts on pin 16 from the CTC (Counter Timer Chip) at 3J3. The CTC generates this interrupt in response to either active &CUBUSY, &WSKCMP, or &FINT (&DMI) signals, or the programmable time-of-day clock. When the CTC generates an interrupt to the Z80A it will also place a vector corresponding to the location of the interrupt routine on the Z80A data bus. The Z80A will then jump to this location and perform the required task. A further discussion on the workings of the CTC can be found in the section covering the CTC.

c. WAIT (input)

During Memory Mapped I/O operations, &PWAIT asserts the Z80A's &WAIT pin to delay the Z80A by one complete WAIT state. The &PWAIT signal is generated by L31 (1J6), the Wait State Insert Flipflop, whenever the flipflop is driven by the &MMI/O signal, which is asserted during all MMI/O operations.

d. CONTROL OUTPUTS

Z80A control outputs are supplied to L96 (1E12), the Control Line Driver, when the inactive &BUSAK signal enables the driver. (&BUSAK is inactive when the Z80A has bus control.)

The &RD and &MREQ are the only control signals generated by the RCU during DMA operations. They are generated when the RCU needs to access memory (the Z80A is held inactive until the &50BBUSREQ signal from the RCU is deactivated).

&M1 is active on Z80A pin 27 during op-code fetch cycles. When a memory read or write is about to occur, the &MREQ signal from pin 19 is activated. When a read operation is about to occur, &RD goes active on pin 21, and when a memory or I/O write operation is about to occur, &WR goes active on pin 22. The Input/Output Request (&IORQ) signal from pin 20 is active only during interrupt acknowledge cycles.

The Refresh signal (&RFSH) travels to the Refresh Multiplexer Logic and the Memory Request Logic to generate the RAS-only refresh operation. Pin 28 of the Z80A generates &RFSH during the last two "T" states of an op-code fetch.

During diagnostic operations, the &FFOD command can be asserted on L12 (1H14) pin 11 with D6 = 1 on pin 12 to prevent a memory error from interrupting the Z80A with an NMI. L12 will then generate a high signal from pin 9 that prevents the Memory Error (&ME) signal from being gated through L46 (1I14).

2.2.2 ADDRESS BUS

Address lines from the Z80A are supplied to Address Bus Drivers L145 and L130 (1I/J12). L145 drives the low address byte and L130 drives the high address byte. When the inactive &BUSAK signal asserts pins 1 and 19 of both L145 and L130, the drivers place the addresses onto the A0-15 Address Bus. &BUSAK is inactive while the Z80A has bus control.

L145 does not drive address bit A7 directly from the Z80A. Rather, this bit is sent to the A7 Refresh Bit Multiplexer where it is multiplexed with a synthetic A7 bit used for RAM refresh purposes. The multiplexed result, A7R, is driven by L145 (1J13) as the A7 address bit. (Section 2.4.3 provides a detailed explanation of the refresh operation.)

L129 and L144 located at (2I/K13), are address buffers between the 50BUS and the Z80A's A0-15 Address Bus. The RCU uses these RCU-Memory Address Buffers when it provides an address for a memory access operation. The buffers move the address from the 50BA Bus when the enabling signal, which is generated by L127 (1K10) in response to an RCU bus request, is present. (Sections 2.5.1 and 2.5.2 provide a detailed explanation of the RCU memory access operation.)

2.2.3 DATA BUS

Data lines to and from the Z80A pass through Data Transceiver L115 (1G13), which produces outgoing data or accepts incoming data depending on enable and direction control inputs. When the Data Transceiver is disabled, the CTC has access to the Z80A via the D0Z-D7Z bus. The Data Transceiver is disabled (ie, tristated) when a high signal generated by L43 (pin 6), located at (1F8), asserts L115 pin 19. Only the CTC has access to the Z80A via the D0Z-D7Z Bus when the Data Transceiver is disabled.

Three operations can disable the Data Transceiver. When the Z80A does not have bus control (eg, in a DMA operation) the active &BUSAK signal asserts L43 (1F8) pin 4 to disable the Data Transceiver. While the CTC is being read via the D0Z-D7Z Bus, the CTC Chip Enable (&CTC CE) signal and the &RD signal assert L63 (1F9) pins 9 and 10, respectively. L63 then generates a signal that asserts L43 to disable the transceiver. When the Z80A is in an interrupt-acknowledged service routine, active &IORQ and &M1 signals assert L63 (pins 12 and 13, respectively). L63 then generates a signal that causes L43 to disable the transceiver. The CTC can then access the Z80A via the D0Z-D7Z Bus.

L29 (1G10), the Data Transceiver Control Flipflop, governs the direction of data flow to and from the Z80A. During a read from memory operation, the active &RD1 signal asserts the clear pin (pin 1) of L29, driving the pin 5 output low. (&RD1 is used through L29 to prevent bus contention problems.) The low signal from L29 pin 5 places the transceiver in the read from memory direction (B to A) by asserting pin 1. Write operations are performed when the &RD1 signal is inactive. The inactive &RD1 signal asserts pin 2 of flipflop L29. Then, when clocked by the &1/2Phi clock, L29 issues a high signal from pin 5 to place the transceiver in the write direction (A to B).

L89 (2I10) is a Data Transceiver between the 50BUS and the Z80A's D0-7 Data Bus. During RCU memory access operations, when the necessary enabling and direction control signals are present, the L89 RCU-Memory Data Transceiver moves data to and from the 50BD Bus. The control signals are generated in response to RCU bus request and Read/Write signals. (Sections 2.5.1 and 2.5.2 provide a detailed explanation of the RCU memory access operation.)

2.3. COUNTER TIMER CHIP

The Counter Timer Chip (CTC), L82 (3J3) is a programmable, 4-channel device that generates maskable interrupts and provides a time-of-day clock. The chip has an 8-bit data bus, eight control outputs, and 10 control inputs (including the clock input). Counter Timer Chip interrupts have the highest priority after non-maskable interrupts; therefore, the Enable Interrupt input (pin 13) is held in a high, enabled state at all times. The Counter Timer Chip Data Bus (D0-7Z) provides an all-purpose, free access path between the Z80A and the Counter Timer Chip. To reset the Counter Timer Chip, the Master Reset (&MRZ) signal asserts pin 17. (FIGURE 2.3-3 shows the Counter Timer Chip access logic.)

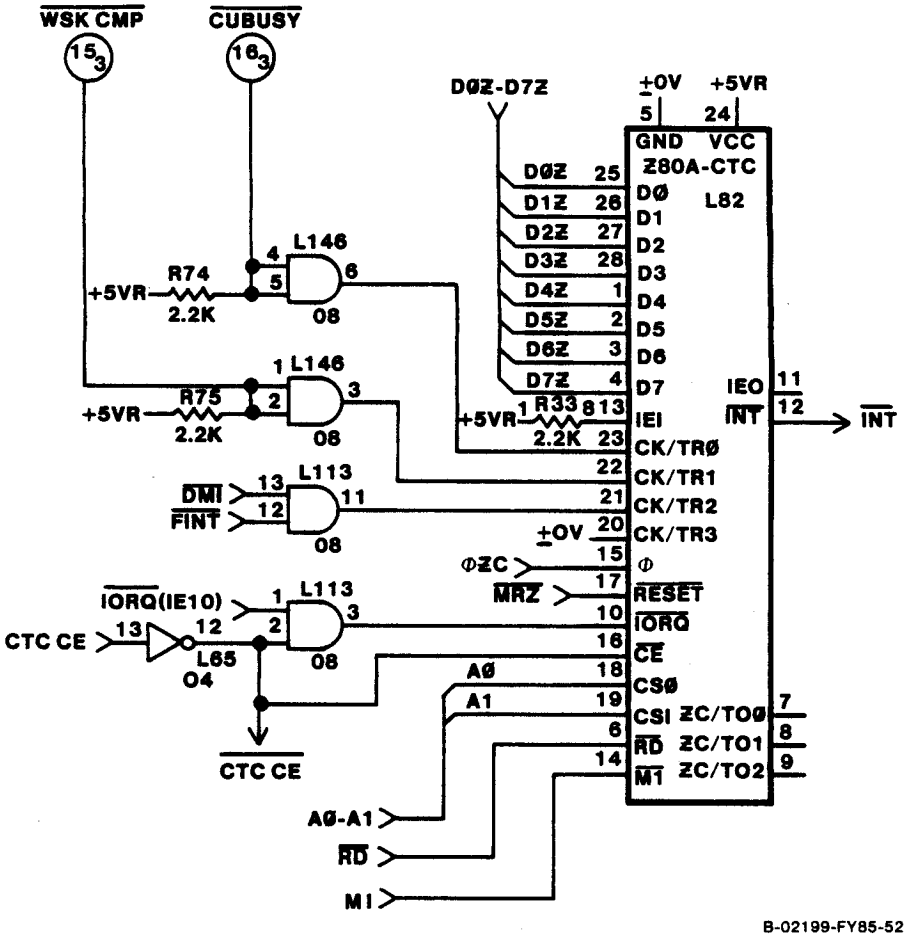

FIGURE 2.3-1
Counter Timer Chip Access Logic

When the Counter Timer Chip issues the Interrupt (&INT) signal from pin 12, it also places a unique vector on the data bus. The CTC-generated vector combines with information programmed in the Z80A Instruction (I) Register to provide a pointer to a table. This table contains a list of interrupt service routine addresses that direct the Z80A to the proper service routine.

CTC channels 0, 1, and 2 are set in the counter mode and are used to prioritize Z80A interrupt requests received by the Counter Timer Chip. Channel 0 generates an interrupt request when the RCU has completed an operation and is, therefore, no longer busy (&CUBUSY, pin 23). Channel 1 generates an interrupt request when the Winchester Disk Drive (WDD)completes a seek operation (&WSKCMP, pin 22), and channel 2 provides interrupt support for Floppy Disk Drive (FDD) functions such as the deadman timer (&DMI, pin 21 via L113 (3J5)) and Floppy Disk Controller Interrupt (&FINT, pin 21 via L113). Channel 3 is programmed to operate in the timer mode for use as a time-of-day clock.

Buffered address bits A0B and A1B (on pins 18 and 19 of L82) provide the channel selection signals to the CTC. A0B and A1B select one of the four CTC channels (channel numbers are coincident with A0B and A1B's hex values) to generate prioritized interrupts. The CTC Chip Enable (&CTC CE) signal asserts L82 pin 16 to enable the CTC for operation. The Z80A issues the &RD, &IORQ, and &M1 control signals to the CTC. &RD is active on pin 6 when a read operation is pending, &IORQ is active on pin 10 during interrupt acknowledge cycles, and &M1 is active on pin 14 during op-code fetch and interrupt acknowledge cycles.

2.4. MEMORY

Memory support for the OIS 40/50/60 processors is divided among RAM, PROM, and Memory Mapped Input/Output (MMI/O). Sixty-four kilobytes of RAM and 4k bytes of PROM are available on the RMU board for power-up diagnostics and Initial Program Load (IPL). Memory addresses from 1000-FF00 are assigned to RAM, with the lower 4k bytes (0000-0FFF) overlayed by PROM for power-up diagnostics and initial bootstrap. Memory addresses from FF00-FFFF are reserved for MMI/O.

The Resource Management Unit provides 64k bytes of RAM (with parity) in nine 64k-bit dynamic memory chips. PROM-resident programs normally overlay memory addresses 0000-0FFF. RAM addresses 0000-0FFF are not normally available but can be accessed under software control (via the MMI/O &FF0E command) following the power-up sequence and during diagnostics. A 2-position switch on the OIS 40/50/60 control panel selects either the Floppy Disk Drive (FDD) or the Winchester Disk Drive (WDD) as the device to be used for initial program loading. After the IPL and diagnostics, RAM can be banked in from 0000-0FFF.

During the power-up routine, memory is loaded with data carrying bad (ie, odd) parity bits. This data will cause a parity error if it is read from memory that has not been initialized (ie, loaded with valid data). The Memory Parity Bit Control Flipflop (L30 (1D3), gate 2Q) controls the parity of the data loaded into memory. Upon receipt of an &FF0D command with D7 = 1, L30 generates signals that cause the gating logic of L26 and L46 (1D1) to issue an odd PARIN signal, loading all bad parity bits upon power up. During normal operation (due to power-up default), L30 allows the even parity bit from L27 into memory.

2.4.1 Z80A and Direct Memory Access Paths

Either the Z80A or the RCU can access RAM via the A0-15 Address Bus and the D0-7 Data Bus as shown in FIGURE 2.4-1 . (The actual memory access circuitry appears in FIGURE 2.4-2.) The Z80A accesses memory directly (through buffers) from its data and address output pins. The RCU gains Z80A bus control for a DMA operation by issuing either an active Command Bus Request (&CMD BUSREQ) or an active 50BUS Bus Request (&50BBUSREQ) signal. The Z80A responds with an active &BUSAK (Bus Acknowledge) signal to release bus control to the RCU.

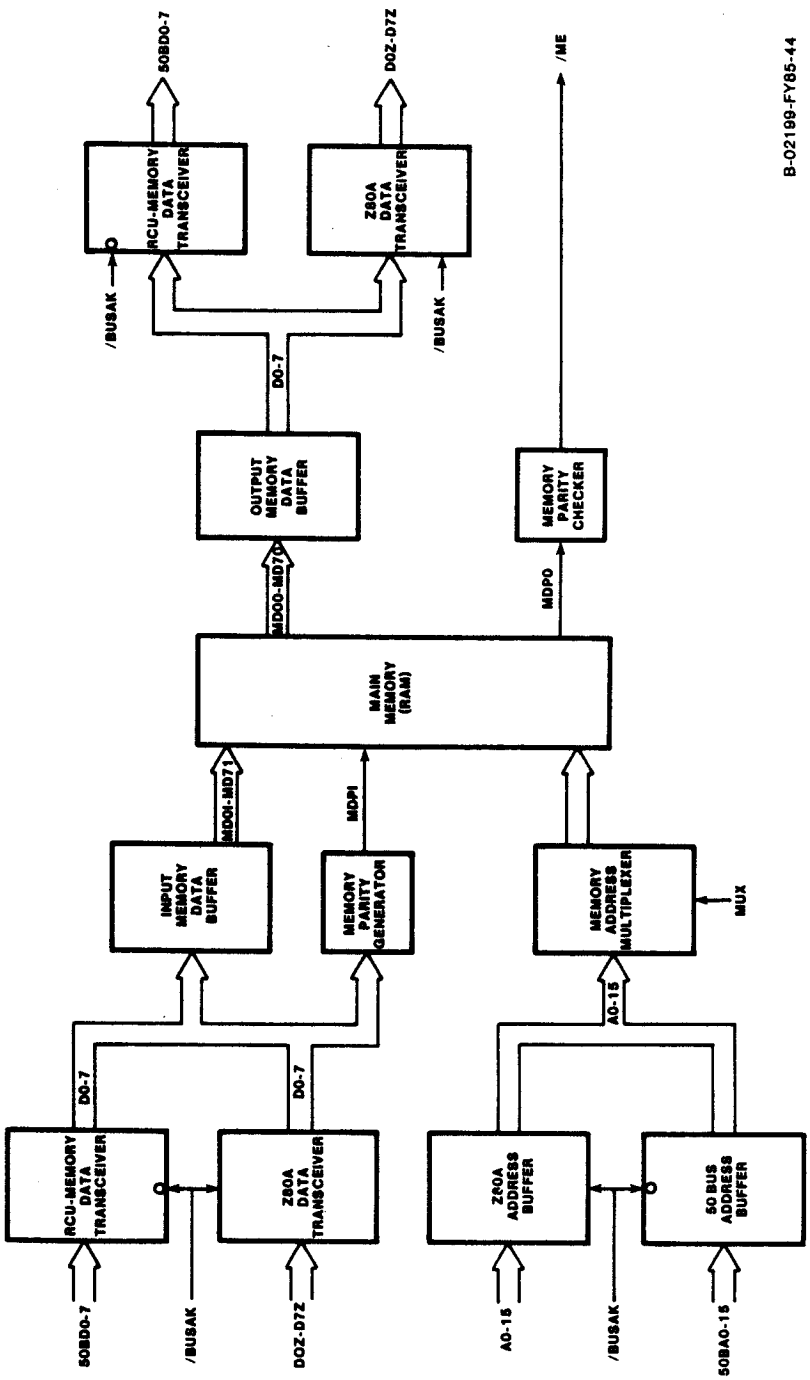

FIGURE 2.4-1
Memory Access Block Diagram

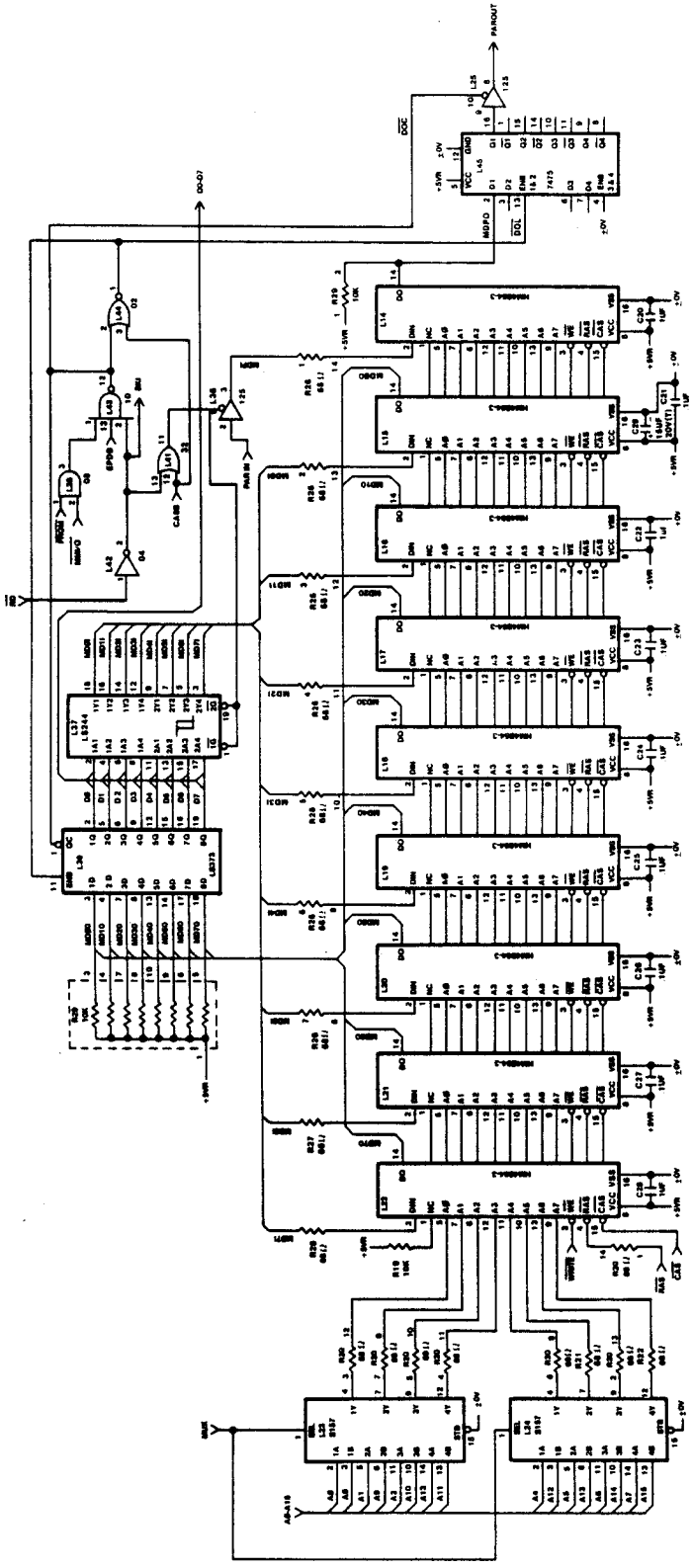

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FIGURE 2.4-2
Memory Access Circuitry

Direct Memory Access (DMA) occurs under RCU control via the D0-7 Data Bus and the A0-15 Address Bus. The RCU initially moves data between the 50BD Bus and the RCU's data buffer. Upon receipt of the proper enabling and direction control signals, RCU-Memory Data Transceiver (L89 (2I10)) moves data between the 50BD Bus and the D0-7 Bus. The RCU sends addresses for read and write operations to the A0-15 Address Bus via the 50BUS Address Bus and Address Buffers L129 and L144. (2I/J13)

When performing a DMA transfer, the RCU-Memory Operation Enabling Flipflop (L127 (2K10)) issues a signal from pin 6 that enables Address Buffers L129 and L144 and Data Transceiver L89 to move data between the RCU and memory via the 50BUS. BUSAK is clocked through L127 by the Phi-Z (8-MHz) clock to generate the &50B BUSAK (50BUS Bus Acknowledge) signal from pin 6. BUSAK is active whenever the RCU has Z80A bus control. &50B BUSAK asserts the enabling pins of the address buffers and data transceiver.

The direction of data flow through RCU-Memory Data Transceiver L89 is controlled by gating the 50BR/W (50BUS Read/Write) signal through L141 (2H13) to create a synthetic &RD (simulated Z80 Read) signal. If the synthetic &RD signal is active, L89 passes data from the D0-7 Bus to the 50BD Bus as the RCU reads the memory.

In a Z80A or DMA memory access, data is buffered from the D0-7 Bus to the MD0I-MD7I (Memory Data Input) Bus by Input Memory Data Buffer L37 (1D9). Outgoing data is buffered from the MD0O-MD7O (Memory Data Output) Bus to the D0-7 Bus by Output Memory Data Latch L39 (1D10).

Upon receipt of a low enabling signal on pins 1 and 19, L37, the Input Memory Data Buffer, allows data to enter memory. L41 (1D8) generates the enabling signal for L37 from pin 11 when it receives inactive &RD and active &CASB (Buffered Column Address Strobe) signals on pins 13 and 12, respectively. RD is inactive during memory write operations, and &CASB is active near the end of memory access operations.

When the main memory is to be read, the Output Memory Data Latch L39 (1D10) receives an active Data Out Control (&DOC) signal on pin 1 and an active Data Out Load (&DOL) signal on pin 11. Gate L43 (1D7) generates the &DOC signal when all of the gate's inputs are high. Generally, L43 generates &DOC when PROM and MMI/O are not being accessed (inactive &PROM and inactive &MMI/O on pins 1 and 2 of L38), the read signal is active (active RD on L43 pin 2), and the processor Data Bus is enabled (active EPDB on L43 pin 13). The &DOC signal generated from L43 pin 12 asserts L44 pin 2 and then is gated with &CASB. If &CASB is active (as it should be at the end of a memory access cycle), L44 generates the &DOL signal. &DOL asserts pin 11 of the Output Memory Data Latch (L39) to send the data from memory to the D0-7 Data Bus. Upon receipt of &DOL and &DOC, the transparent Memory Parity Bit Buffer (L45 (1B6)) creates the PAROUT (Parity Out) signal from the Memory Data Parity Out (MDPO) signal.

2.4.2 Memory Parity Generator/Checker

In Z80A-controlled read and write operations, the Parity Generator/Checker (L27 (1E4)) and its associated circuitry generate and check data parity (see FIGURE 2.4-3). L27 also generates a parity bit during RCU-controlled write operations. However, since the 50BUS does not have the capacity to carry a parity bit, the RCU does not check parity during read operations. The parity bit generated during RCU-controlled write operations is checked when the Z80A reads RCU-generated data.

During memory write operations, the Parity Generator/Checker establishes even parity for RCU or Z80A data entering on the D0-7 Data Bus. L27 issues the even parity bit from pin 5 to assert L26 pin 5 (1C2). Normally, the even parity bit is gated through L26, since the signal on L26 pin 4 is low (pin 4 is high only while running diagnostics). The even parity bit from L26 pin 6 is gated through L46 to create the PARIN (Parity In) signal. PARIN is gated through L36 (1C7) to create the MDIP (Memory Data In Parity) signal that enters RAM via L14 (1B7) pin 2.

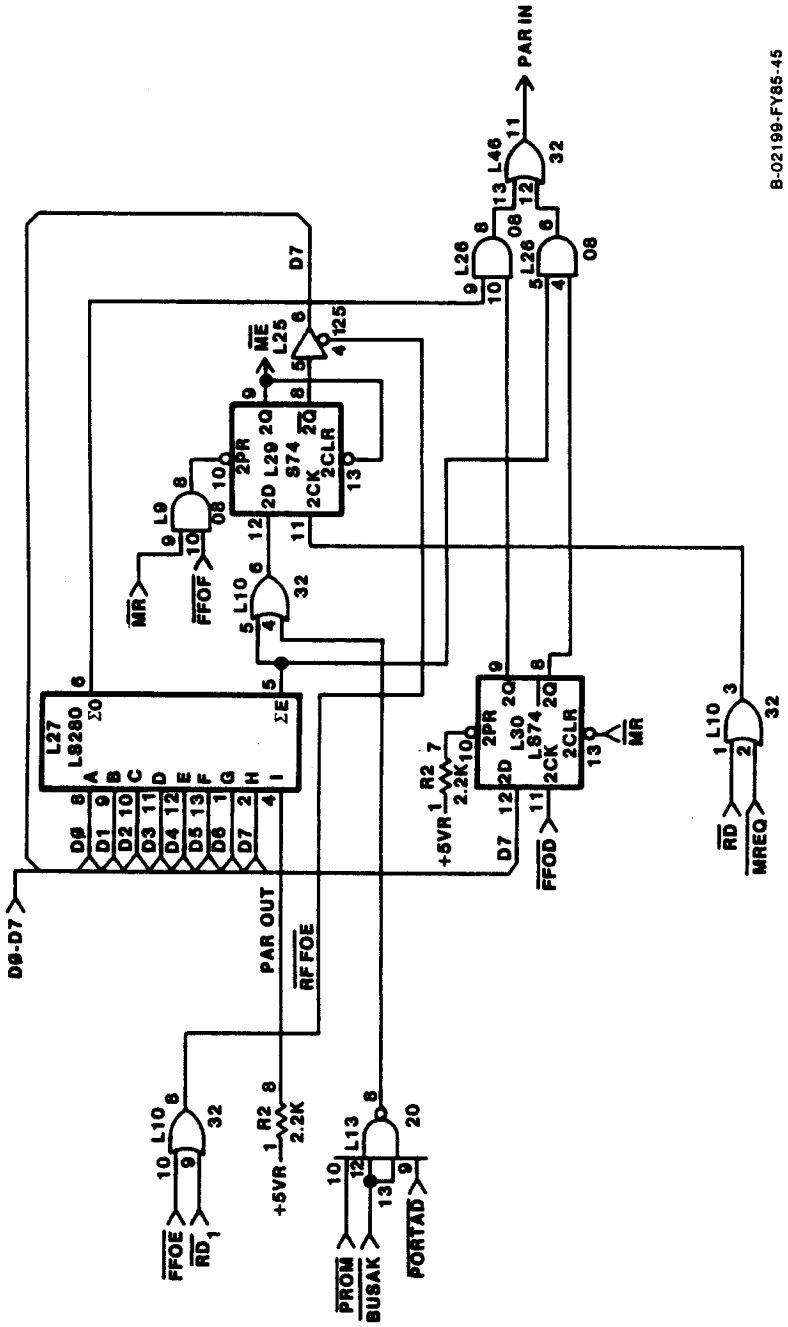

FIGURE 2.4-3
Parity Generator/Checker Logic

L27 also checks data parity in Z80A-controlled memory read operations. MDPO, the parity bit from memory, is issued from L14 pin 14 and used by Parity Buffer L45 to create the PAROUT signal. PAROUT along with data on the D0-7 Bus asserts the inputs of the Parity Generator/Checker (L27). If L27 detects odd parity (ie, an error has occurred), it issues a low signal from pin 5 that drives low pin 12, (via L10, see next paragraph below) of the Memory Parity Error Flipflop (L29). The trailing edge of the &RD signal clocks the low signal on L29 pin 12 through L29 to create the Memory Error (&ME) signal on pin 9. &ME asserts the Z80A to generate a non-maskable interrupt.

Parity can be checked only when the Z80A reads data from memory. Parity is not checked if &PROM (PROM operation), &BUSAK (RCU-controlled DMA operation), or &PORTAD (MMI/O operation) prevents L29 from checking parity bits. When asserted by any of these signals, L13 generates a high signal from pin 8 that prevents generation of the &ME signal by holding L29 pin 12 high.

By issuing the &FF0E command and reading the D7 bit, software can determine whether an NMI was caused by a memory error or the Restart Switch (SW2). &FF0E from L80 (1J9) pin 14 is gated with the &RD signal to create the &RFF0E signal on L10 (1E5) pin 8. &RFF0E asserts L25 pin 4, which allows software to read the ME signal via the D7 bit to determine if a memory error caused the NMI. If ME is inactive, the Restart Switch caused the interrupt; if it is active, a memory error caused the NMI.

Diagnostic routines test the Parity Generator/Checker by issuing the &FF0D command with D7 = 1. In response to &FF0D, L30 (gate 2Q (1D4)) generates signals that cause the gating logic of L26 and L46 to issue an odd PARIN signal, establishing the odd parity bit in memory. As data is retrieved from memory, L27 checks for even parity and detects odd parity. (L27 always checks for even parity.) L29 then generates the Memory Error (&ME) signal.

2.4.3 Memory Refresh

Memory Refresh of the RMU dynamic RAM chips must be completed every 2-4 ms, depending on RAM type. To begin the memory refresh process, the Z80A activates the Z80A Refresh Control (&RFSH) signal at the end of an op-code fetch cycle. At the same time, the Z80A presents to memory the row address of the memory space to be refreshed. (See FIGURE 2.4-4.) The Z80A can provide a 7-bit refresh address, yielding a total of 128 row addresses for refresh. Some of the RMU's 64k-byte RAMs require 256-row address refresh capability. This capability is produced by toggling and multiplexing a synthetic Refresh A7 bit into the A7R bit of the Z80A Address Bus.

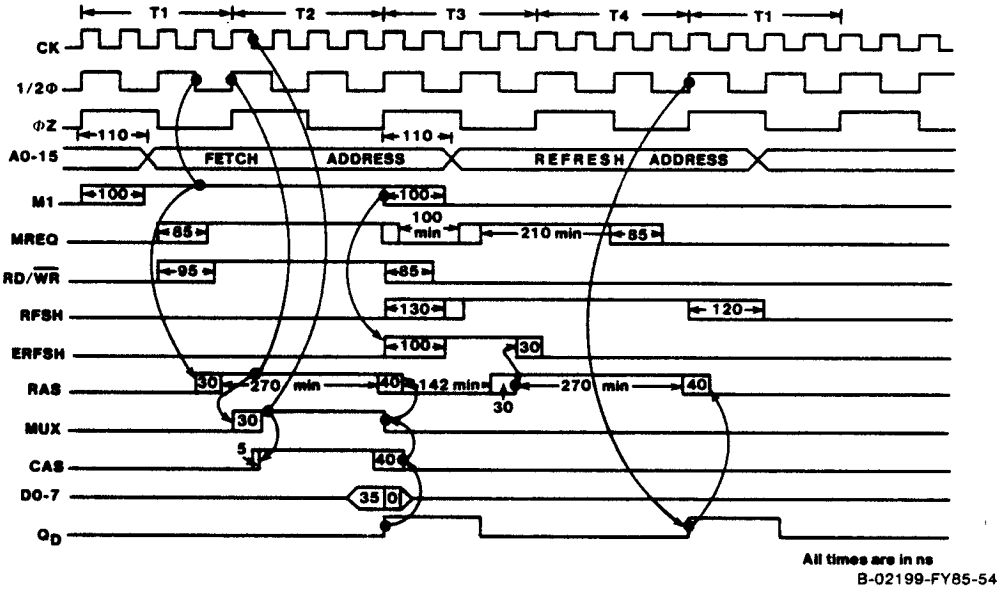

FIGURE 2.4-4
Op-Code Fetch / Memory Refresh Timing Diagram

Z80A refresh memory request logic is centers around the Refresh Request Flipflop (L35 (3J12)), which generates the Early Refresh (&ERFSH) signal. L35 produces &ERFSH at the end of each &M1 op-code fetch cycle as the rising edge of &M1 clocks L35 pin 3. The signal ERFSH from pin 5 asserts the RAS Generating Flipflop (L54 (3K10)) via L51 to begin the RAS generation cycle for refresh (see Section 2.4.4). &ERFSH from pin 6 travels to the L52 (3I11) Refresh A7 Bit Control Flipflop to cause it to select the synthetic Refresh A7 bit needed to perform a RAS-only refresh operation. L35 is cleared when the &RAS signal asserts pin 1.

The Refresh A7 Bit Control Flipflop L52, is preset to select the synthetic Refresh A7 bit during refresh by the active &ERFSH signal. The synthetic Refresh A7 bit is produced by L69 (3I13) and latched by the synthetic Refresh A7 Bit Latch L40 (3I12) during a row address refresh. Active &MREQ and &RFSH signals assert L69 (via L71) to clock the A6 bit through to L40.

In a 256-row refresh operation, the Z80A issues A6 low for the first 128-row refresh and high for the second 128-row refresh. In a 256-row refresh, the high signal from L69 (generated as a result of the high A6 signal) clocks L40 to generate the high A7R bit needed for the second 128-row refresh. Both A7R and A6 are low for the first 128-row refresh and high for the second 128-row refresh. The Refresh A7 Bit Control Flipflop is reset (to feed the A7' bit) at the end of each refresh operation by the rising trailing edge of the &RFSH signal that clocks pin 3.

2.4.4 RAS/CAS Signal Generator

Row Address Strobe (RAS) and Column Address Strobe (CAS) signals strobe data to and from the memory array. (FIGURE 2.4-5 shows the RAS/CAS and WRITE generating logic.) The memory address must be present on the Memory Address Bus prior to RAS or CAS strobe activation. RAS uses the low-order address byte to provide the row location of the data cell to be strobed, and CAS uses the high-order address byte to provide the column location of the data cell to be strobed.

The RAS/CAS generation cycle begins differently in memory data access operations and refresh operations. During a request for memory data transfer, the RAS/CAS cycle is initiated by either an active &M1 (Z80A in Fetch Cycle) signal on L34 (3K12) pin 4, or an active &MREQ (Memory Request) signal on L51 (3K14) pin 1 and an inactive RFSH (Z80A Refresh Control) signal on L51 pin 2. When the active &M1 signal or the active &MREQ and inactive &RFSH signals assert L34 and L51, output pin 6 of L34 generates the Enable Processor Data Bus (EPDB) signal. EPDB clocks L35 (3K12) (gate 2) to initiate the generation of memory data transfer request signals. The Memory Access Operation Pending Latch (L35, gate 2) issues a high signal from pin 9 that asserts pin 12 of L54 (3K10), the RAS Generating Flipflop.

During refresh operations, the Early Refresh (ERFSH) signal is generated at the end of all op-code fetch cycles (ie, when &M1 is active) to begin the RAS-only cycle. ERFSH from L35 pin 5 asserts L54 via L51 to initiate the RAS-generating cycle.

RAS/CAS generation during refresh or memory access begins with a high signal asserting pin 12 of L54, the RAS Generating Flipflop. The &1/2Phi (8-MHz) signal clocks L54's 2Q output to begin the generation of synchronized RAS signals. The &RAS signal from L54 pin 8 proceeds to memory to provide the row address strobe, and RAS from pin 9 travels to the RAS/CAS Timing Shift Register (L53 (3I8)) to begin the RAS/CAS timing chain. RAS from pin 9 also asserts L38 (3K9) pin 10 to begin the MUX-CAS cycle. An inactive &RFSH signal on pin 9 of L38 indicates that the current operation is not a refresh operation. The combination of active RAS on L38 pin 10 and inactive &RFSH on L38 pin 9 causes pin 8 to go high. This high signal asserts pin 2 of MUX Flipflop L50 (3J8) to generate MUX from pin 5 when the 1/2Phi clock signal asserts pin 3.

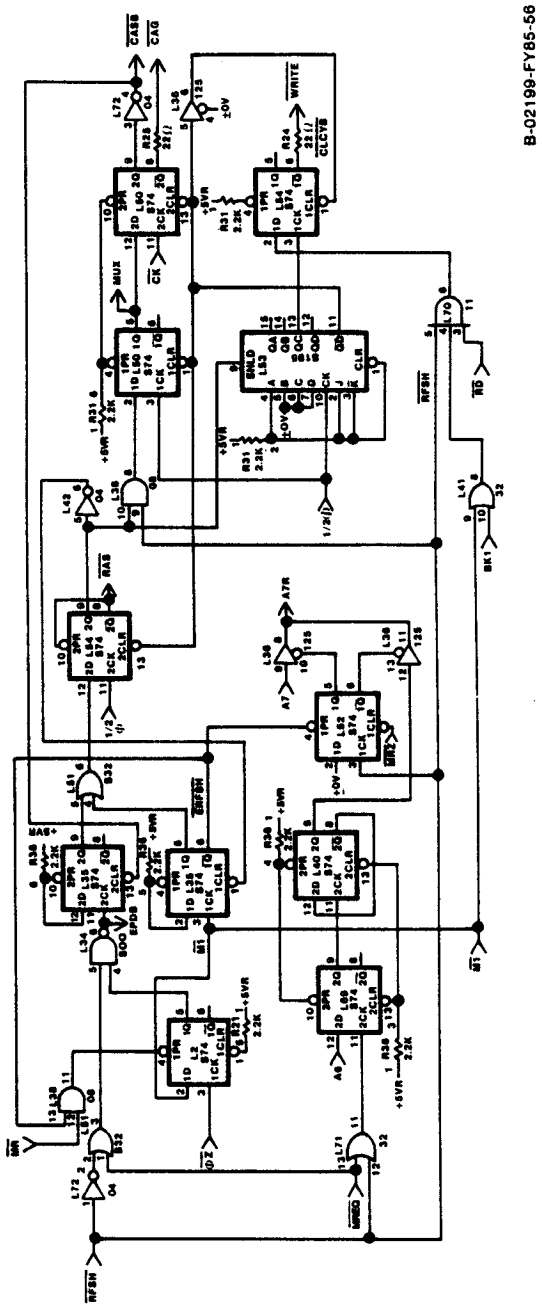

FIGURE 2.4-5
RAS/CAS and WRITE Generating Logic

MUX asserts the Memory Address Multiplexer (L23 and L24 (1A-C14)) to switch to the high-order address containing the column address. MUX also asserts pin 12 of CAS Flipflop L50 to generate CAS signals upon receipt of the &CK 16-MHz clock. &CAS from pin 8 proceeds to memory to provide the Column Address Strobe; it also indicates that the end of the memory access cycle is near. &CASB from L50 pin 9 clears the L35 Operation Pending Flipflop and aids in memory read/write control.

2.4.5 RAS/CAS Timing

RAS/CAS timing logic generates the timing sequence (shown in FIGURE 2.4-6) for memory access operations. The RAS/CAS Timing Shift Register (L53) is preset to 01H. When the RAS signal arrives on pin 9 of L53, it places the Shift Register into the shift mode of operation. The 1/2Phi clock signal on pin 10 of L53 shifts the bit through the register upon the receipt of each clock pulse. After two clock pulses, the QC output generates a high signal that clocks Write Flipflop L54 to generate the &WRITE signal. The &WRITE signal will only be activated if L70 (3H8) has all highs on its inputs, indicating a write operation. Upon the arrival of the third clock pulse at the end of the memory access cycle, the &QD output of L53 goes high on pin 11. The &Qd signal clears the RAS/CAS signal generation logic directly, and then clears the write logic via L36 and the &CLCYB signal.

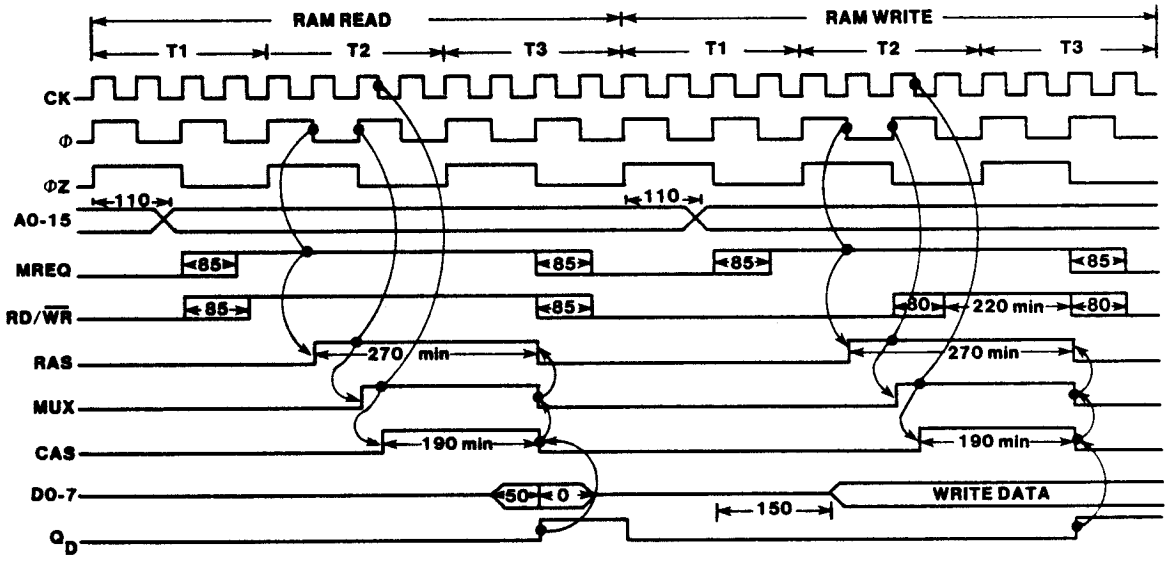

FIGURE 2.4-6
Memory Read Write Timing

2.4.6 Read/Write Signal Generator

During read and write operations, the Read/Write Signal Generator (L54 (3I7)) produces an active or inactive &WRITE signal on pin 6. The &WRITE signal from L54 is low if a write operation is required, and high if a read operation is required. When clocked by the Qc bit from the RAS/CAS Timing Shift Register, the Read/Write Flipflop samples its pin 2 input. If pin 2 is high, L54 generates an active &WRITE signal, and if pin 2 is low, L54 generates an inactive &WRITE signal.

Read/Write signal generation logic monitors the &M1, &RFSH, and &RD (respectively, Z80A in Fetch Cycle, Z80A Refresh Control, and Z80A or 8X305 Memory Read) signals via L54 pin 2 to detect read or write operations. When the inputs of L70 are high, a write operation is pending, and a signal from the output of L70 asserts L54 pin 2. &M1, &RFSH, and &RD are normally inactive during write operations; these signals, therefore, cause the output of L70 to go high to generate the WRITE signal from L54. &M1 and RD are gated into L41 to prevent L54 from generating WRITE during interrupt acknowledge operations when &M1 goes active.

2.4.7 Programmable Read Only Memory

L47 (1H6), a 2732A-2 PROM, contains 4k bytes of power-up (ie, IPL) and diagnostic programs that are addressed by bits A0-11. (FIGURE 2.4-7 diagrams the PROM Access Logic.) PROM-resident programs overlay the lower 4k bytes (0000-0FFFH) of RAM. PROM is enabled to overlay RAM when pins 9 and 10 of L7 (1G6) both are held high. L7 pin 9 normally is held high by a signal from the PROM Diagnostic Control Flipflop (L30 (1E5), gate 1Q). L7 pin 10 is held high by low address bits A12-15 driving the output of L64 (1G6) high. This combination of high signals on the inputs of L7 generates the low enabling signal from pin 8 that asserts the PROM's command enable and output enable pins via L46 (1G6). L46 monitors the &M1 and &MREQ signals (from L9 (1F6)) on its pin 4 input to ensure that either one or both signals are active during PROM access.

Data from the enabled PROM is placed on the D0-7 Bus and then buffered into the D0-7 Data Bus via Data Buffer L48 (1G5). L48's output is enabled when the &RD signal (from L96 (1E12)) and the low PROM enabling signal (from L7) assert L46 pins 1 and 2 to generate the low enabling signal from pin 3. The low signal from L46 pin 3 enables data output from PROM by driving pins 1 and 19 of L48 low.

To make more RAM space available as needed, diagnostic and operating system programs can retain control of the lower 4k bytes of RAM and, therefore, prevent PROM from overlaying the 0000-0FFF RAM space. Applying the &FF0E signal, via L10, to pin 3 of L30 (gate 1Q) with D7 = 0 on pin 2 causes L30 to generate a low signal from pin 5. This low signal asserts pin 9 of L7 to prevent the generation of the PROM enabling signal and, therefore, disabling PROM from the lower 4k bytes of RAM. When PROM is disabled, the lower 4k bytes of RAM are available for diagnostic testing.

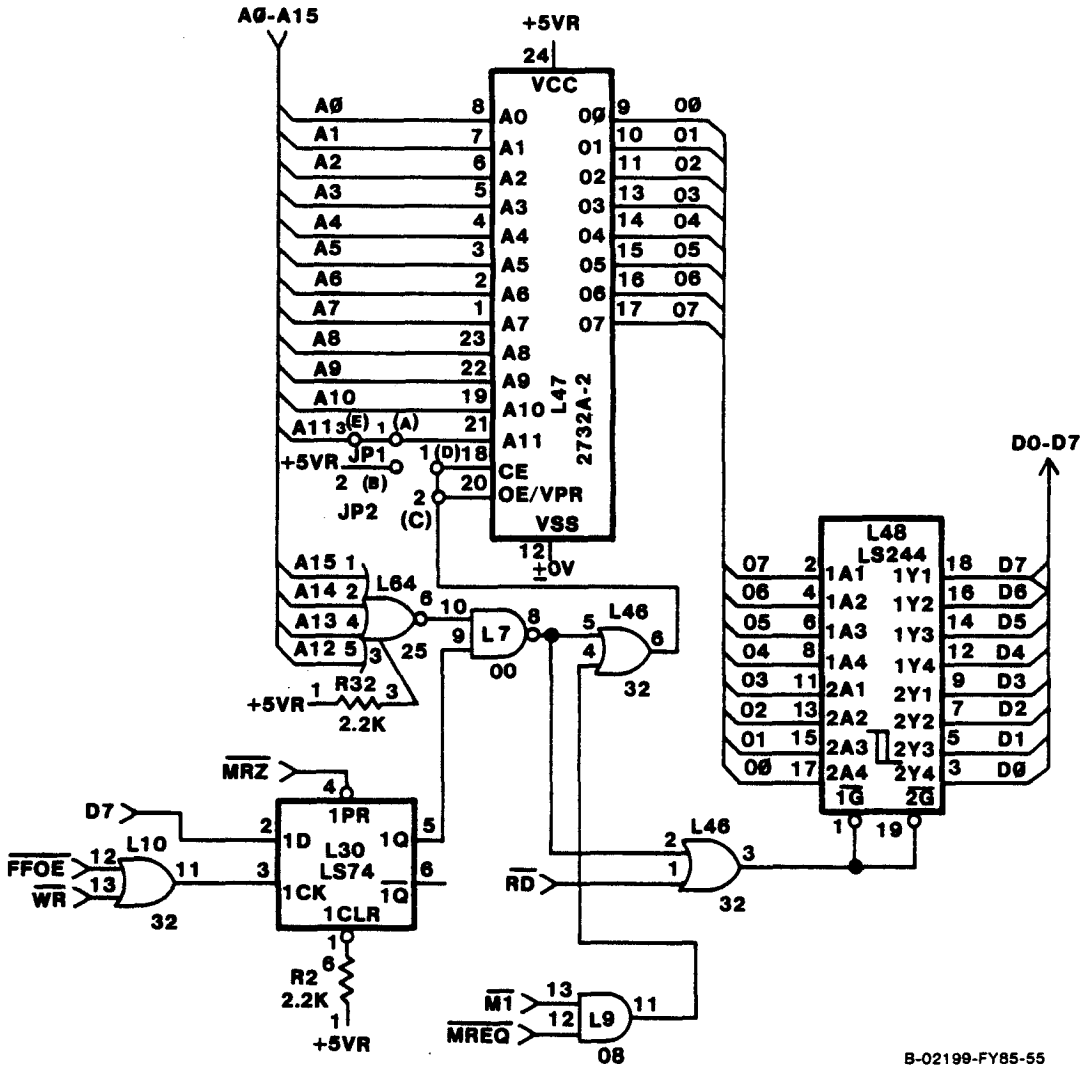

FIGURE 2.4-7
Prom Access Logic

2.5. FLOPPY DISK CONTROLLER

The Resource Management Unit's Floppy Disk Controller can execute ten different commands, each is initiated by a multibyte transfer from the Z80A processor. Command execution can result in a multibyte transfer back to the Z80A processor. Because of this multibyte interchange of information between the Floppy Disk Controller and the Z80A, it is convenient to consider each command as consisting of three phases:

1. Command phase: The Floppy Disk Controller (FDC, L101) receives all the information it needs to perform a particular operation.

2. Execution phase: The FDC performs the operation as instructed by the command.

3. Result phase: After completing the operation, the FDC makes status information available.

The FDC, when used in an OIS 50 system, can execute ten of the 15 available FDC commands: Read Data, Read ID, Read a Track, Specify, Write Data, Format a Track, Seek, Recalibrate, Sense Interrupt Status, and Sense Drive Status. Each of these commands require a multiple byte transfer of commands to specify the operation to be performed. The FDC receives and decodes the command in the command phase and executes it in the execution phase. At the end of the execution phase, the FDC issues an interrupt to the Z80A processor. The FDC must then complete the result phase, by reading all of the FDC internal status registers before the FDC can accept new commands.

2.5.1 Read/Write Operation

During the command phase of Floppy Disk Drive (FDD) operation, data is sent, via the D0-7 Bus, from the Z80A to the FDC Data Transceiver (L87 (2D7)). (FIGURE 2.5-1 shows FDC data access routes, and FIGURE 2.5-2 and 2.5-3 show the FDC access and data path logic.) The command is sent through the Data Transceiver to the Floppy Disk Controller Data (FDCD) Bus and into the FDC. The FDC interprets the command and enters the execution phase to perform the operation.

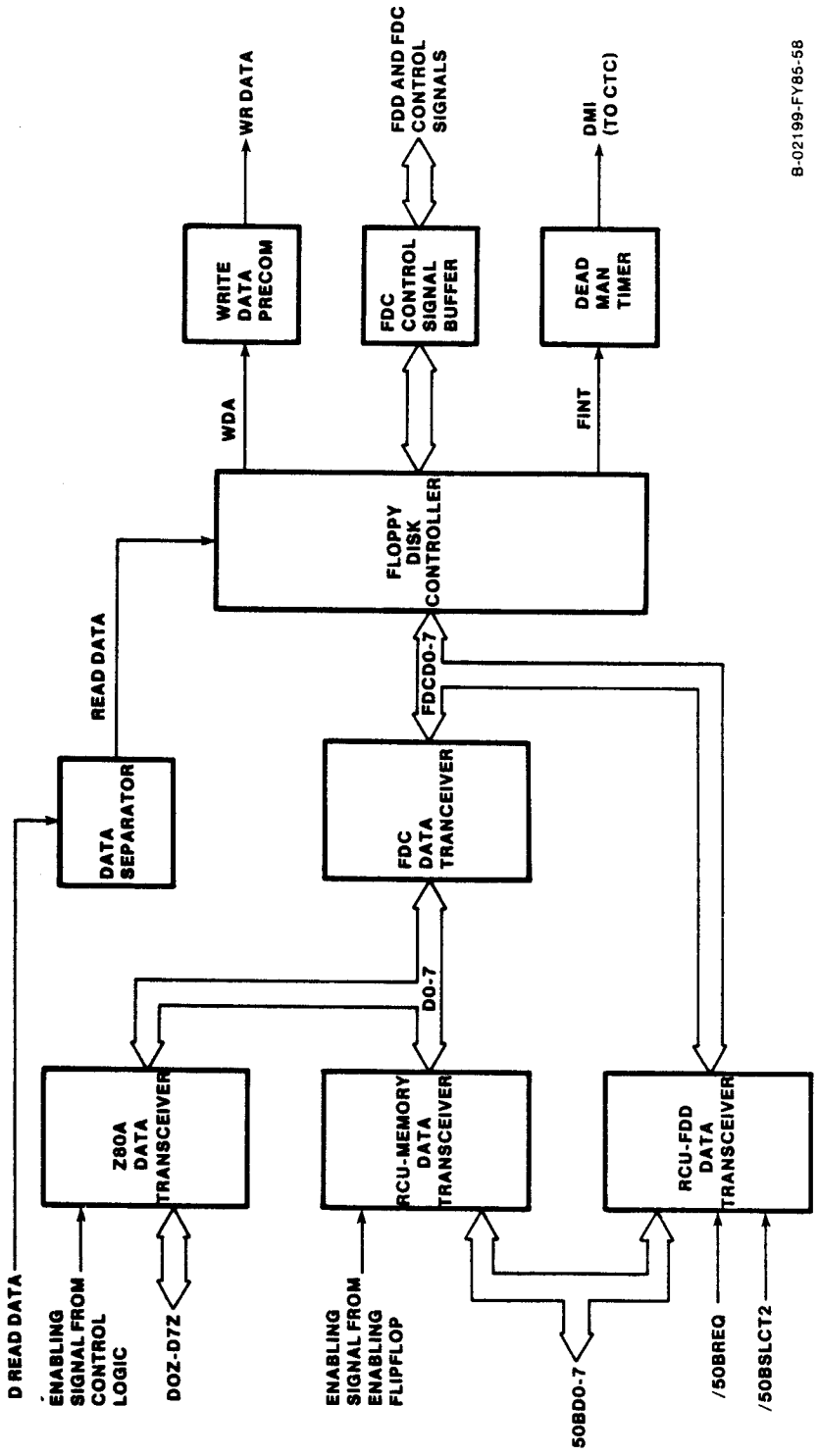

FIGURE 2.5-1
FDC Access Block Diagram

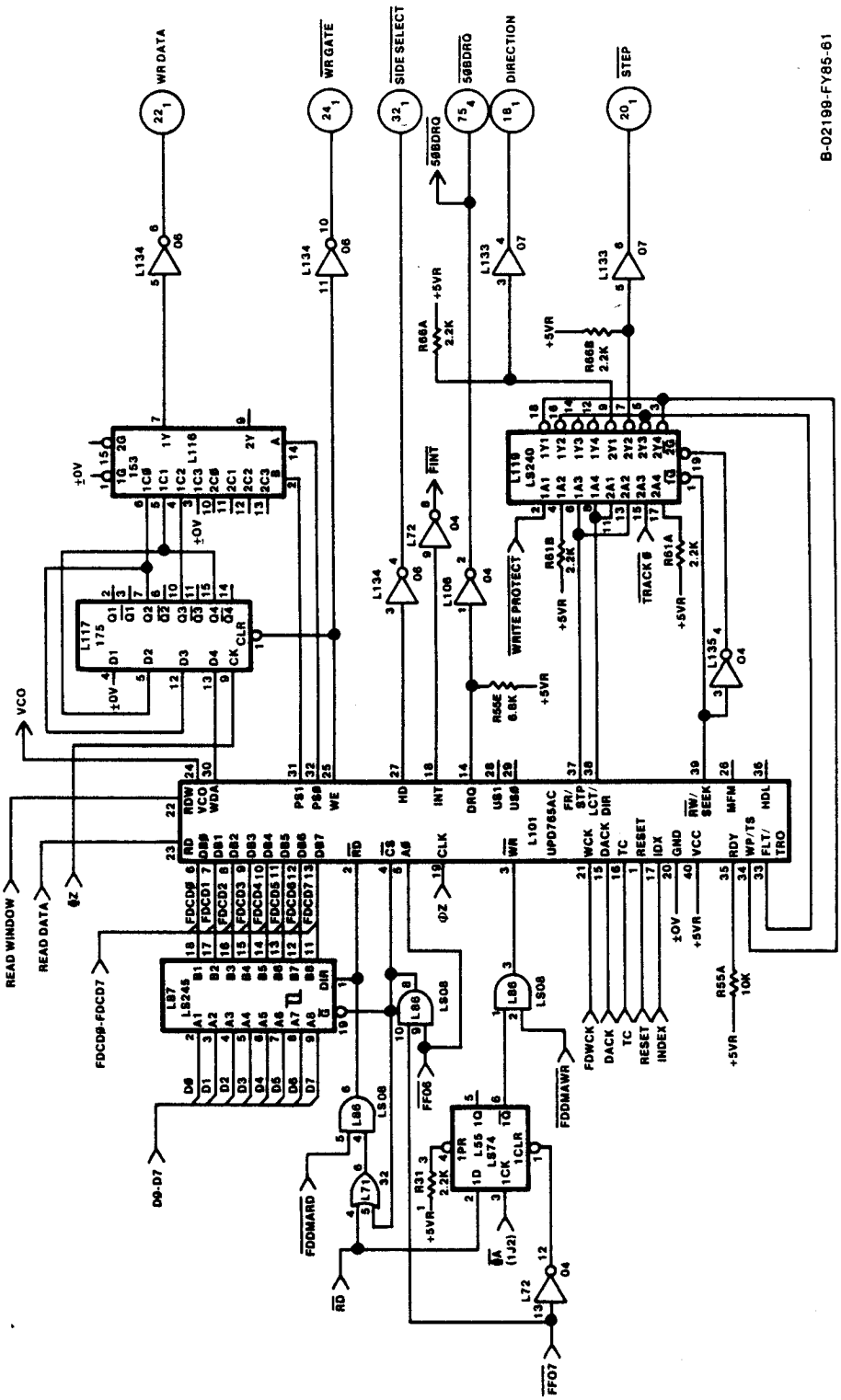

FIGURE 2.5-2
FDC Access Logic

During FDD read operations, control signals allow data to be read from the Floppy Disk Drive. The FDD Controller receives this data on pin 23, assembles it into a parallel format, and sends it, via the FDCD Bus, to the RCU-FDC Data Transceiver (L88 (2H10)). Enabling and direction control signals allow the data to pass through L88 and onto the 50BD (50 Bus Data) Bus. The RCU board then reads the data from the 50BD Bus into its data buffer. The FDD-originated data is written from the RCU back onto the 50BD Bus, and, simultaneously, the data's memory address is written onto the 50Bus Address (50BA) Bus. When the necessary enabling and direction control signals are present, the RCU-Memory Data Transceiver (L89 (2I10)) reads the data from the 50BD Bus onto the D0-7 Bus. At the same time, the RCU-Memory Address Buffers (L129 and L144 (2I-J13)) place the data address onto the A0-15 Bus. The data is then stored in memory at the address provided on the A0-15 Bus. (Section 2.5.2 explains the enabling and control signals used in this operation.)

During FDD write operations, the data to be written to the Floppy Disk Drive is retrieved from memory under RCU control via the D0-7 Data Bus. The RCU provides the data address via the 50BUS Address Bus and Address Buffers L129 and L144. Upon receipt of the proper enabling and direction control signals, the RCU-Memory Data Transceiver (L89) places the data on the 50BD Bus. The RCU reads the data from the 50BD Bus into its data buffer. When the RCU-FDC Data Transceiver (L88) is properly enabled, the data is written from the RCU onto the 50BD Bus and passed through L88 onto the FDCD0-7 Bus. The FDC reads the data from the FDCD Bus, serializes it for transmission, and sends the serial data to the Floppy Disk Drive from pin 30. At the same time, the FDC issues the appropriate control signals from other pins.

2.5.2 Read/Write Enabling

The RCU generates the &50BRW signal to place the DMA operation in either the read or write direction (see FIGURE 2.5-3). During RCU read operations, &&50BR/W is low; the low &&50BR/W signal is gated through L143 (2G12), with &50BSLCT2 and &50BREQ to create the active FDD DMA Read (&FDDMARD) signal. During RCU write operations, &&50BR/W is high; the high &&50BR/W signal asserts L112 (2G12) pin 5 to generate an active FDD DMA Write (&FDDMAWR) signal from pin 6. &FDDMARD and &FDDMAWR assert the appropriate buffers and control logic to control read and write operations.

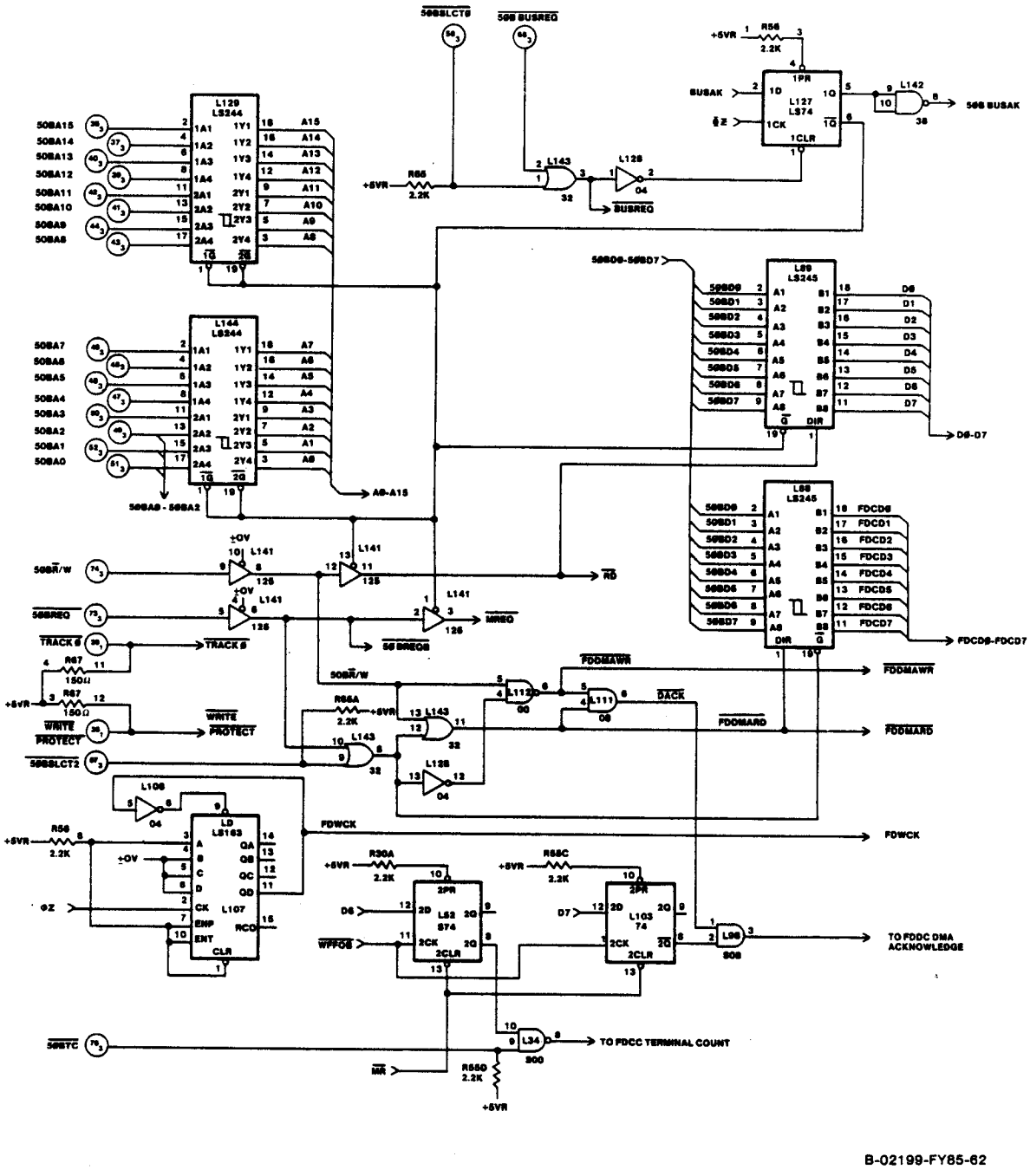

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FIGURE 2.5-3
FDC Data Path Logic

The chip select signal, which is generated by L86 (2C7) pin 8 as a result of the Read FDC Status (&FF06) or Read/Write FDD Data (&FF07) command asserting pins 9 and 10, enables FDC Data Transceiver L87 (2D7). The &RD and &FDDMARD signals control the direction of data flow through L87. If &FDDMARD is active on L86 pin 5 or an active &RD signal is gated onto L86 pin 4 (via L71), L86 generates a low signal from pin 6 that places the transceiver in the read direction. If &RD or &FDDMARD is inactive (high) and the FDC is selected, L87 is placed in the write direction.

L127 (2K10), the RCU-Memory Operation Enabling Flipflop, issues a signal from pin 6 that enables Address Buffers L129 and L144 and Data Transceiver L89 to move data (via the 50 Bus) between the RCU and memory. The BUSAK signal is clocked through L127 by the Phi-Z clock to generate the &50B BUSAK signal from pin 5. (BUSAK is active whenever the RCU has Z80A Bus Control.) &50B BUSAK asserts the enabling pins of the address buffers and data transceiver.

To control the direction of data flow through the RCU-Memory Data Transceiver (L89), the &&50BR/W signal is gated through L141 to create a synthetic &RD (simulated Z80 Read) signal. If the synthetic &RD signal is active, L89 passes data from the D0-7 Bus to the 50BD Bus when memory is read by the RCU.

Gating the RCU-generated &50BREQ (50BUS Byte Request) signal on pin 10 with the &50BSLCT2 (FDD Bus Select) signal on pin 9 creates a low signal from L143 pin 8. This low signal enables L88, the RCU-FDC Data Transceiver. &50BREQ is active whenever the RCU reads or writes a byte of data to the disk, and &50BSLCT2 is active during all FDD operations. The &50BREQ signal from the RCU is interpreted on the RMU board, via L141 (2H13), to create the synthetic &MREQ (Z80A Memory Request) signal.

The direction of data flow through the RCU-FDC Data Transceiver (L88) is controlled by the Floppy Disk Drive DMA Read (&FDDMARD) signal asserting L88 pin 1. When &FDDMARD is active on pin 1, data passes from the FDCD Bus to the 50BD Bus as data is read from the FDD. An inactive &FDDMARD signal places L88 in the opposite (ie, write to the FDD) direction. &FDDMARD is created from L143 pin 11 by the &&50BR/W (50 Bus Read/Write) signal being gated through pin 13 to pin 11. L143 pin 12 monitors the active &50BSLCT2 and &50BREQ signals (via L143 pins 9 and 10) to ensure that the FDD is selected and the RCU is prepared to read or write a byte of data.

2.5.3 Control Signal Generator

The Read-Write/Seek (&&RW/SEEK) signal on pin 39 of the FDC determines the flow of signals through L119 (2B4), the FDC Control Signal Buffer (FIGURE 2.5-2). When the FDC performs a read or write operation, pin 39 is low to allow the 1Y1-1Y4 outputs of L119 to follow the inputs on pins 1A1-1A4. When the FDC performs seek operations, pin 39 is high to allow the 2Y1-2Y4 outputs to follow the inputs on pins 2A1-2A4.

During Floppy Disk Drive read or write operations, L101 pin 39, the FDC, produces a low Read/Write (&RW) signal that enables the 1Y outputs of Control Signal Buffer L119. These outputs generate the signals required for read or write operations to occur. L119 passes the &WRITE PROTECT and Fault (FLT) signals from the FDD to the FDD Controller. The &WRITE PROTECT signal defines, to the FDC, the status of the recording media (ie, write protected or not write protected). The signal from 1Y2 (pin 16) of L119 is held low to create an inactive FLT (Fault) signal. The FDC's FLT input is not used and, therefore, is held inactive during read or write operations.

During Floppy Disk Drive Seek operations, L101 pin 39 produces a high SEEK signal that enables the Control Signal Buffer's 2Y outputs to generate the signals needed to perform a seek operation. L119 passes the &STEP, DIRECTION, TRACK 0, and TWO-SIDED MEDIA signals. &STEP asserts the Floppy Disk Drive to move the head of the drive to another cylinder, and DIRECTION controls the direction in which the drive moves the head when the STEP signal is generated. TRACK 0 signals the FDC that the drive is at Track 0. The TWO-SIDED MEDIA signal is held active on pin 34 of the FDC (since this is the only medium used during seek operations).

The following FDC-generated control signals are not buffered through L119: Floppy Interrupt (FINT), 50BUS DMA Request (50BDRQ), SIDE SELECT, and Write Gate (WR GATE). When the FDC finishes command execution, the FDC (L101, pin 18) sends a Floppy Interrupt to the RMU. L101 pin 14 sends 50BDRQ to the RCU when a byte of data is ready to be transferred. SIDE SELECT is generated by pin 27 and sent to the FDD to select a disk surface to be used in the FDD operation, and WRITE GATE is generated from pin 25 to command the FDD to prepare for a write operation.

2.5.4 Write Data Precompensation

Write data precompensation circuitry (FIGURE 2.5-2) defines the timing sequence of the data pattern to be written onto the Floppy Disk Drive. Data can be written in one of three different timing sequences, early, nominal, or late, to prevent data errors from being created when the data is written. Writing data early means that each data bit is written 250 ns earlier then normally expected. Nominal data is written at the time that it would normally be written, and late data is written 250 ns after it would normally be written on the disk. Writing data at alternate times prevents data crowding and, therefore, prevents frequent data errors as data is read from near the center of the disk.

L117 (2E5), the Write Data Precompensation Sequencer, is enabled during FDD write operations by the WRITE GATE signal from FDC pin 25. When enabled, L117 receives data from the FDC via pin 13 and then transmits that data via pin 15. The data from pin 15 is fed back into pin 5 of L117 and then fed back again from the pin 7 output to the pin 12 input. This feedback cycle creates the 250-ns delay between each data bit as a result of the Phi-Z (4-MHz) clock asserting the clocking pin of L117. Early data is fed from L117 pin 15, nominal data from pin 7, and late data from pin 10.

L116 (2E4), the Write Data Precompensation Data Selector, chooses either early (input pin 5), nominal (input pin 6), or late (input pin 4) data depending on the PS1 and PS0 signals it receives on pins 2 and 14. The data, in the selected timing sequence, is transmitted to the Floppy Disk Drive as the WR DATA signal from L116 pin 7. Table 2.5-1 illustrates the timing sequences selected by the PS0 and PS1 signals from the FDC.

Table 2.5-1: WRITE DATA/PRECOMPENSATION SELECT SIGNALS

PS0	PS1	TIMING SEQUENCE
0	0	Nominal
0	1	Early
1	0	Late

2.5.5 Motor Control

On/off motor control circuitry protects against excessive disk wear if the drive motor is left running continuously (since the heads are loaded when the disk drive door is closed). To turn on the drive motor, the Z80A issues &WFF0B with D0 = 1. In response, Motor Control Flipflop L118 ((2C13) gate 1) issues the MOTOR ON signal to the disk drive. To turn off the drive motor, the Z80A issues &WFF0B with D0 = 0, and L118 responds with the inactive MOTOR ON signal. The FDD motor is shut off automatically under Z80A program control if the FDD is not accessed for 1 s.

The &FF0A MMI/O command asserts L55, the FDC Reset Flipflop, to generate a signal from pin 5 which asserts the reset pin of the NEC765 Floppy Disk Controller. Reset pulse width must be at least 10 us (see Section 2.5.9).

2.5.6 Terminal Count

For Z80A-Floppy Disk Drive DMA operations, Terminal Count and DMA Acknowledge handshaking signals are generated by flipflops L52 and L103, respectively (see FIGURE 2.5-3). The RCU board generates Terminal Count and DMA Acknowledge signals for 8X305-Floppy Disk Drive DMA operations.

During Z80A-Floppy Disk Drive DMA operations, Terminal Count Flipflop L52 provides the active Terminal Count handshaking signal. This signal is sent to the FDC during Z80A DMA data transfers either when all the data has been sent or when all the data has been received by the Z80A. L52 (2F12) generates a high Terminal Count signal from pin 8 upon receipt of the &WFF0B command with D6 = 1. This signal is gated through L34 (2E12) to generate a signal that asserts FDC pin 16. During 8X305-FDD DMA operations, the RCU board provides the Terminal Count signal to FDC pin 16 via the 50 Bus Terminal Count (&50BCT) signal on pin 9 of L34.

2.5.7 DMA Acknowledge

The DMA Acknowledge (&DACK) handshaking signal is used in all Floppy Disk Drive DMA transfers. The RCU returns this signal, on a byte-by-byte basis, in response to a DMA Request from the FDC. During normal DMA operations (8X305-Floppy Disk Drive), L111 (2G11) generates &DACK in response to the RCU-generated &50BREQ signal (as shown in FIGURE 2.5-3). L143 pins 9 and 10 monitor the &50BSLCT2 (50BUS Select Channel 2) and &50BREQ (50BUS Byte Request) signals. &50BSLCT2 is active throughout any FDD operation, and &50BREQ pulses each time a byte is transferred in a DMA operation. As &50BREQ is activated, it is gated through the L143 (2G13) gates into input pin 4 of L111. L111 then generates &DACK upon receipt of the gated &50BREQ signal (since L111 pin 5 is low as a result of the inverted &50BREQ signal asserting L112 pin 4).

During diagnostics the Z80A (rather than the RCU) can perform DMA operations. In this case, the necessary &DACK signal is generated on the RMU board by the Z80A DMA Acknowledge Flipflop (L103, pin 8 (2F11)) in response to the &WFF0B command with D7 = 1. &DACK from L103 pin 8 is gated through L98 to assert pin 15 of the Floppy Disk Controller.

2.5.8 Deadman Timer

Deadman timer logic prevents errors from causing both Floppy Disk Drive operation and Floppy Disk Controller operation to be frozen or "hung". The Z80A, after issuing a command to the FDC, sends the &FF0C signal to the deadman timer to begin a 540-ms timeout period. The deadman timer logic then monitors the FDC for the presence of the &FINT signal. (&FINT normally is sent to the Z80A from the FDC when command execution is completed.) If the active &FINT signal does not assert the deadman timer logic within 540 ms, the deadman timer logic issues a Deadman Interrupt (&DMI) signal to the Z80A. Also, the Z80A can read the status of the DMI signal via FDC Status Register bit D3 (&RFF0B).

After the FDC receives a command during any Floppy Disk Drive operation, L80 (1J9) issues &FF0C to pin 11 of the Deadman Timer 1-Shot (L100, gate 2 (2D12)). If L100 is not cleared by a low signal on pin 13 prior to the 540-ms timeout, it issues a signal that clocks L69 (2D11), the Deadman Timer Flipflop. L69, when clocked, issues the Deadman Interrupt (&DMI) signal from pin 6. &DMI asserts pin 12 of the CTC (via L13), and the CTC, in turn, issues an interrupt to the Z80A. Upon receiving the interrupt, the Z80A executes a routine to determine whether the Floppy Disk Drive or the deadman timer generated the interrupt. The Z80A then proceeds with other routines to correct the error situation or to retry the Floppy Disk command.

Three signals can clear the deadman timer logic to prevent the generation of the &DMI signal. The &FINT (Floppy Interrupt) signal goes active whenever the FDC completes an operation. &FINT asserts L70 (2D13) pin 13 to generate a low signal from pin 12 that clears the deadman timer logic. &MRFD (Master Reset Floppy Disk) also asserts L70 to clear the deadman timer logic. &RFF0B from L108 reads the FDC Status Registers and clears the deadman timer logic via L70.

2.5.9 Floppy Disk Controller Reset

Either the Z80A processor or the &MRFD (Master Reset Floppy Disk) signal can reset the Floppy Disk Controller. The Z80A resets the FDC by issuing &FF0A commands through L80, the Memory Mapped I/O Decoder. L80 (1J9) issues two &FF0A write commands to reset the FDC: the first &FF0A command turns on the Reset Flipflop and the second turns it off. (Reset pulse width must be at least 10 us.) &FF0A asserts pin 11 of the Reset Flipflop (L55 (2E14), gate 2Q) to generate a high signal from pin 9 that is gated through L71 (2E13) to reset the FDC. The active &MRFD signal resets the FDC by asserting pin 1 of the FDC via pin 9 of L71. (&MRFD is generated as a result of the &AUTO RESET signal.)

2.5.10 Floppy Disk Drive and Controller Status

The Z80A uses the &RFF0B command to read the status of the Floppy Disk Drive and Controller. &RFF0B asserts the clock pins of Status Registers L101A (2D9) and L105 (2C11) to clock the Status Byte onto the D0-7 Data Bus. Table 2.5-2 lists and defines the status signals, and FIGURE 2.5-4 illustrates the logic that generates the status signals.

Table 2.5-2: FLOPPY DISK DRIVE STATUS BYTE

BIT	SIGNAL	DEFINITION
D0	True File Ready	Generated by True File Ready 1-Shot (L100, gate 1). Indicates that Floppy Disk Drive is ready to perform an operation (ie, disk is loaded and spinning, FDD door is closed, and FDD is selected).
D1	Select Line	Generated by Floppy Disk Drive Select Flipflop (L118, gate 2). Indicates that Floppy Disk Drive is selected to perform an operation.
D2	Door Disturbed	Generated by Door Disturbed Flipflop (L120, gate 2). Indicates that door to Floppy Disk Drive is open.
D3	Deadman Timer	Generated by Deadman Timer Flipflop L69. Indicates that deadman timer has generated an interrupt.
D4	50BUS Data Request	Generated by Floppy Disk Controller (L101) when FDC makes a DMA request for data. Signal is of primary significance during diagnostic testing of FDC logic.
D5	Floppy Interrupt	Generated by Floppy Disk Controller. Indicates that received command has been executed. Signal is of primary significance during diagnostic testing of FDC logic.
D6	Not Used	
D7	Not Used	

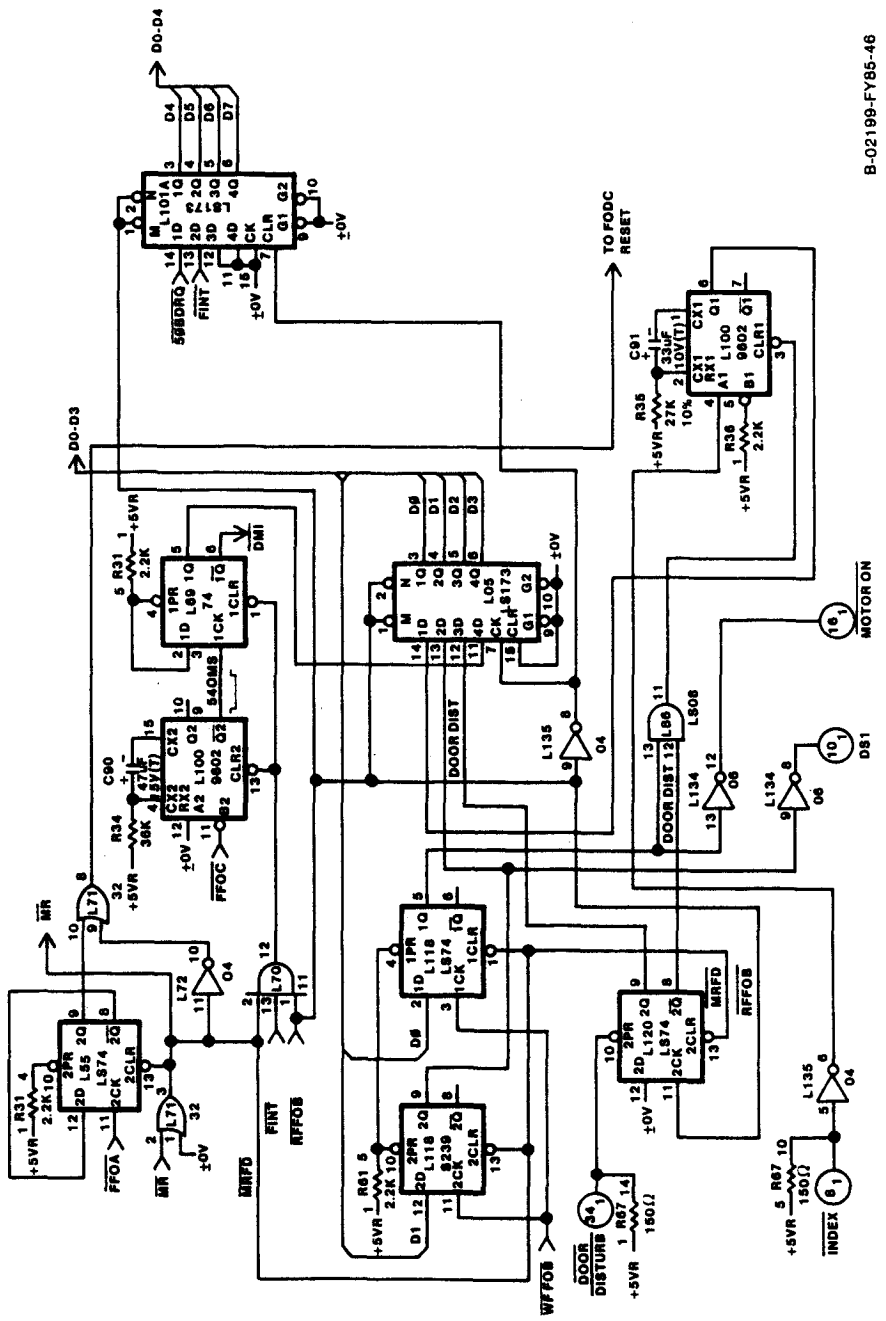

FIGURE 2.5-4
FDC Status Logic

L100 (2A10) (gate 1) generates the True File Ready status signal from pin 6 to indicate that the disk is loaded and spinning, the FDD door is closed, and the FDD is selected. The inactive &DOORDIST signal (door has not been disturbed) and the active MOTOR ON signal (motor is on) assert L86 to generate a high signal from pin 11 that asserts the clear pin of L100. L100 can then generate the True File Ready signal when it receives the INDEX signal from the FDD. The INDEX pulses from the FDD assert pin 4 of L100 when the disk is loaded and spinning. If either the MOTOR ON signal or the &DOORDIST signal on the inputs of L86 changes state, L100 is cleared and the True File Ready signal is deactivated.

The Floppy Disk Drive Select Flipflop (L118 (2C14), gate 2) responds to &WFF0B and D1 by issuing the Disk Select #1 (DS1) signal that controls FDD selection. The Z80A selects the Floppy Disk Drive for operation by issuing the &WFF0B with D1 = 1; &WFF0B with D0 = 0 de-selects the FDD.

L120 (2A13), the Door Disturbed Flipflop, latches the &DOOR DISTURB signal from the FDD to inform the Z80A that the drive door has been opened (even if the door is closed at the time of the Status Read). The Z80A issues the &RFF0B command to read the FDC Status Register. If the door is closed, &RFF0B clears the Door Disturbed Flipflop by clocking a zero through the flipflop.

When a diagnostic routine tests the FDC logic, the Z80A must verify the generation of &50BDREQ (50BUS DMA Request) and &FINT (Floppy Interrupt). &50BDRQ is generated by L101, the Floppy Disk Controller, when L101 makes a DMA request for data. &FINT is generated by the Floppy Disk Controller to indicate that execution of the received command has been completed. Status Register L101A provides &50BDRQ and &FINT to the Z80A via data bits D4 and D5.

2.5.11 Data Recovery

FDD data recovery logic accepts and synchronizes the data signal (D READ DATA) from the Floppy Disk Drive and converts this signal into a form (READ DATA) that the FDC can easily use. (FIGURE 2.5-5 diagrams the data recovery operation.) The data recovery logic recognizes data bits from the FDD only as phase/frequency transitions, which then are converted into a standard digital data stream. Voltage Regulator VR1 provides an isolated 5 V to the data recovery logic (since the recovery logic can operate correctly only in an environment with a minimal amount of electronic noise).

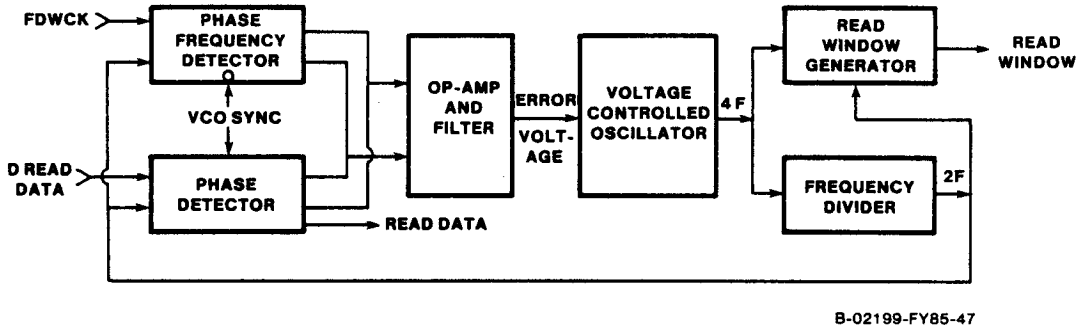

FIGURE 2.5-5
Data Recovery Block Diagram

When the FDD data recovery logic shown in FIGURE 2.5-6 is not reading data, it is locked into use as a free-running frequency generator to hold the recovery logic at the center frequency of operation. The phase locked loop portion of the recovery logic generates a free-running center frequency by locking the phase and frequency of the FDD Write Clock (FDWCK) signal and the VCO-generated feedback signal into the same phase and frequency. (&FDWCK is a 1-MHz signal generated by Floppy Disk Timing Generator L107.)

Phase/Frequency Detector L85 (2J6) detects FDWCK on pin 1 and compares FDWCK's phase and frequency with the phase and frequency of the signal generated by the Voltage Controlled Oscillator (VCO, L83 (2J2)). If the signals' phases and/or frequencies differ, L85 produces error signals on pins 2 and 13. The two L99 gates, sum these signals and send them to Op Amp L84, which creates an error voltage output relative to the signals it receives. The error voltage issued from L84 asserts pin 2 of VCO L83. In response, L83 generates a frequency (from pin 7) that is dependent on the error voltage applied to pin 2. The VCO-generated frequency asserts L97, which then halves the frequency and issues it from pin 5. The frequency from pin 5 again asserts the Phase/Frequency Detector to continue the loop and generate a predictable center frequency until a read operation occurs.

During read operations, the FDC issues a high VCO Synchronizing signal from pin 24. This signal prevents the Phase/Frequency Detector from generating a free-running center frequency by holding pins 11 and 3 of L99 high. The VCO Synchronizing signal drives L103 (2I8) pin 2 high, enabling L103 to receive the D READ DATA signal from the FDD. Data from the FDD can then be accepted, via L103, for conversion into a digital data stream.

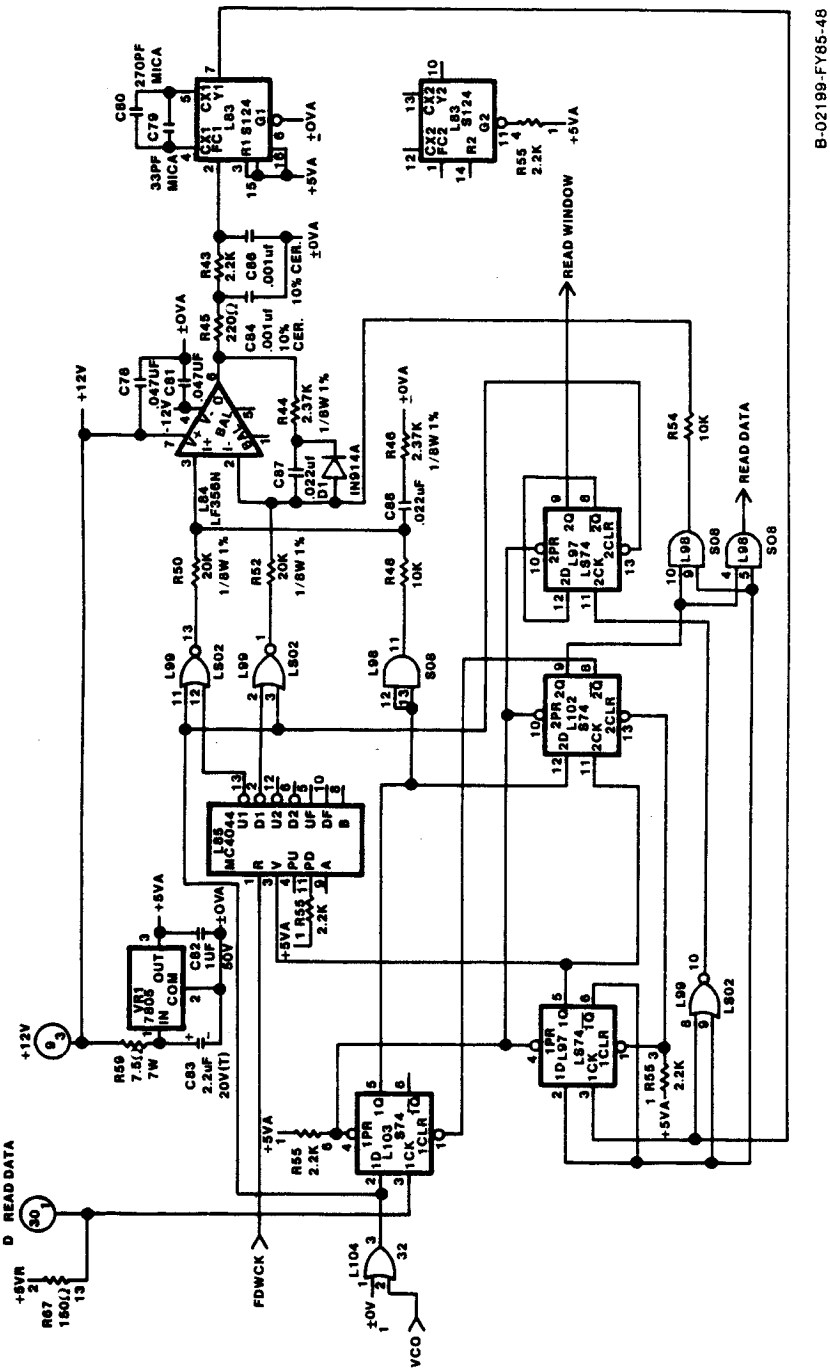

FIGURE 2.5-6
Data Recovery Logic

The data recovery logic recognizes data from the FDD as phase transitions; therefore, during read operations, only the data's phase is significant. L103, when clocked by D READ DATA, issues a signal (from pin 5) containing the phase information the recovery logic needs to convert the FDD data into digital form. The FDD data is gated through L98 (2I5) to assert pin 3 of Op Amp L84. The data also asserts L102 (2H5) pin 12 to generate the READ DATA signal, which is sent to the positive input of the Op Amp. L84 the OP Amp compares the data on its input pins 2 and 3 and issues an error voltage relative to those inputs. This error voltage asserts the VCO, and the VCO, in turn, produces an error frequency that reflects the error voltage. L97 halves the error frequency and transmits it to L102 pin 11 to clock data in.

The synchronized READ DATA signal from L102 pin 9 is fed to the FDC via L98. READ DATA is continually fed back through the loop to reduce the phase error and, therefore, keep the frequency from the VCO within the correct range to separate the data. The FDC reads data when the READ WINDOW signal created by L97 is active (ie, the read window is open).

2.6 SERIAL DATA LINK

2.6.1 Command Decoder

The RCU activates &50BSLCT1 (50BUS Device Select 1) on the 50BUS to select the Serial Data Link I/O ports. Seven commands (see Table 2.6-1) allow the RCU to communicate with a Serial Data Link port on the RMU board. The Serial Data Link Command Decoder (L110 (3G13), see FIGURE 2.6-1) decodes RCU-generated commands from the 50BUS address lines when the Serial Data Link is selected and 50BREQ (50BUS Byte Request) is strobed on pin 6. 50BUS Address Bits 50BA0-2 assert L110 pins 1-3 to select the commands that control the Serial Data Link ports. Appendix D Part 1 describes the 8X305 instruction sequences used to complete the Serial Data Link commands.

During transmit and receive operations, the 8X305 issues the necessary commands and then halts and waits for a response from the Serial Data Link (SDL) logic. After executing a transmit or receive command, the SDL logic deactivates the Clear Halt (&CL HALT) signal to clear the Microcontroller halt. The SDL logic deactivates &CL HALT in response to an active Serial Data Link Byte Request (&BYTE REQ), Serial Data Link Byte Received (&BYTE REC), or &NO DATA signal. In one of the final steps of all SDL operations, the Microcontroller senses SDL Status Register L126 (3G10) to determine which signal cleared the halt state.

A combination of the Channel Select (&CHAN SLCT) signal and the 50BD0-1 Data Bits controls channel selection during SDL receive and transmit operations. (Channels always are selected before the receive or transmit operation is performed.) The Channel Select Flipflops (L125 (3G6-7)) are loaded with the proper channel code via 50BD0-1. &CHAN SLCT then clocks the flipflops to present 50BD0-1 to either the Receive or Transmit Channel Selector. The selected channel number equals the hexadecimal code of 50BD0-1 (eg, hex code 0 selects Channel 0). After the channel is selected, the 8X305 issues instructions and data to begin the receive (1H on 50BA0-3) or transmit (0H on 50BA0-3) operation.

Table 2.6-1: SERIAL DATA LINK COMMANDS

COMMAND	50BA0-2 (HEX)	DEFINITION
&TRANSMIT	0	Transmit (pin 15). Enables Serial Data Link transmit logic.
&RECEIVE	1	Receive (pin 14). Enables Serial Data Link receive logic.
&CHAN SLCT	2	Channel Select (pin 13). Selects channel for upcoming transmit or receive operation. Channels are selected from 50BUS Data Bits 50BD0-3 as follows: 50BD0-3 (Hex) Channel 00 0 01 1 02 2 03 3
&XMIT DATA	3	Transmit Data (pin 12). Moves data from 50BUS Data Bus into Serial Data Link transmit logic.
&RECD DATA	4	Receive Data (pin 11). Moves data from Serial Data Link receive logic onto 50BUS Data Bus.
&STATUS READ	5	Status Read (pin 10). Places Serial Data Link Status Nibble on 50BUS bits 50BD0-4. Data is interpreted as follows: 50BD0 = 0 - Received data byte 50BD1 = 0 - Received data parity error 50BD2 = 0 - Byte requested for transmit 50BD3 = 0 - No data timeout detected
DIAGNOSTIC	6	Diagnostic (pin 9). Allows diagnostic routine from RCU to check Serial Data Link logic on RMU board.
SPARE	7	Not Used (pin 7).

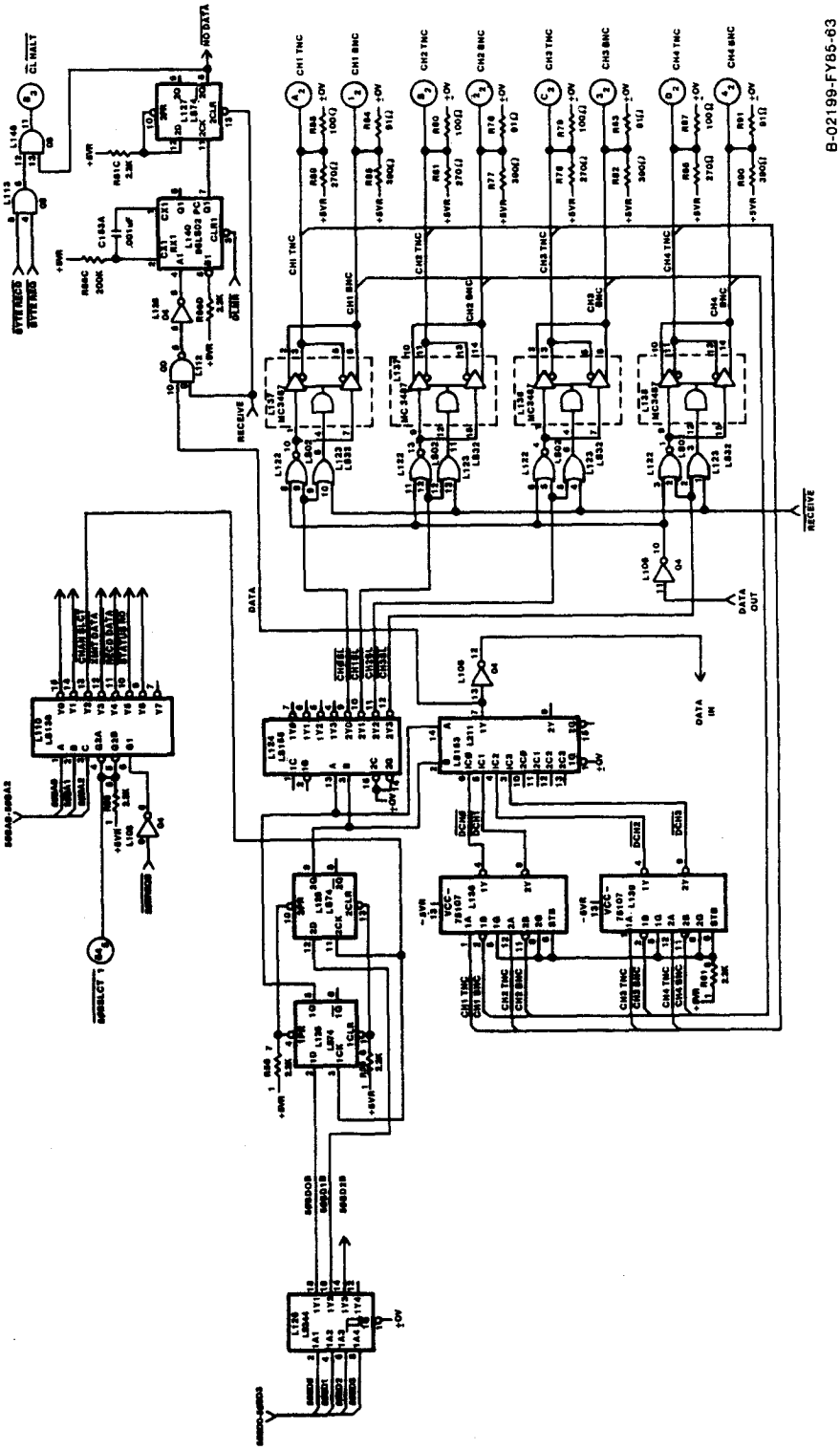

FIGURE 2.6-1
SDL Operation Control Logic

Loopback Control Flipflop L120 (3E9) places the SDL into a loopback mode for diagnostic testing. L110 issues a diagnostic command with 50BD2B = 1, causing L120 to generate the Receive Enable (REC ENB) signal. REC ENB enables the Receive Timing logic, but does not enable the receive logic to accept data from the 50BUS. ENABLE SAMPLE and &RECD DATA enable the SDL receive logic to receive data from the SDL transmit logic. (The loopback capability can be implemented as needed, but is not currently used in any diagnostic routines.)

2.6.2 Receive Operation

Serial Data Link Receive operations are initiated when the 8X305 Microcontroller issues a 1H code on Address Bits 50BA0-3 and &50BSLCT1 (50BUS Device Select 1) and &50BREQ (50BUS Byte Request) are active. In response, Command Decoder L110 issues the Receive signal on pin 14 to assert Receive Latch L109 (gate 2 (3F9)) to hold the receive condition active. L109, in turn, issues RECEIVE to the SDL receive logic to instruct and enable the logic to receive data. RECEIVE from L109 is gated through L108 to create the REC ENB signal. REC ENB deactivates the clear pins of Start Bit Detector L78 (3F13) and Enable Sample Flipflop L91 (3E11), allowing these chips to function when the Start Bit is detected. FIGURE 2.6-2 and 2.6-3 show the SDL Receive Block Diagram and the SDL Receive Logic. FIGURE 2.6-4 illustrates receive operation timing signal interaction.

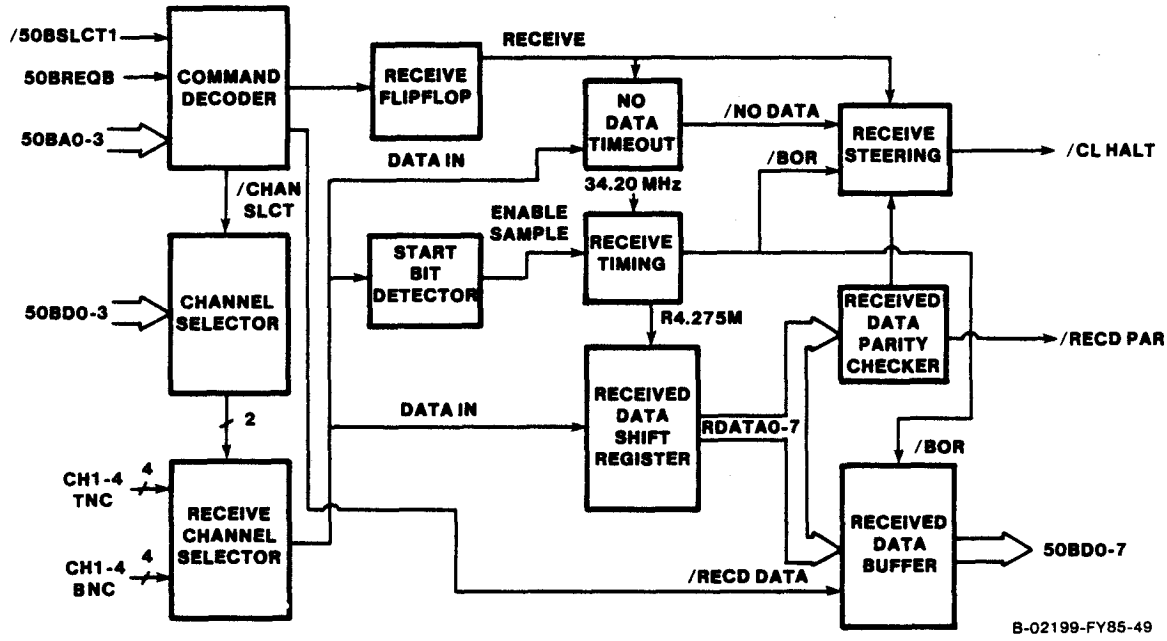

FIGURE 2.6-2
SDL Receive Block Diagram

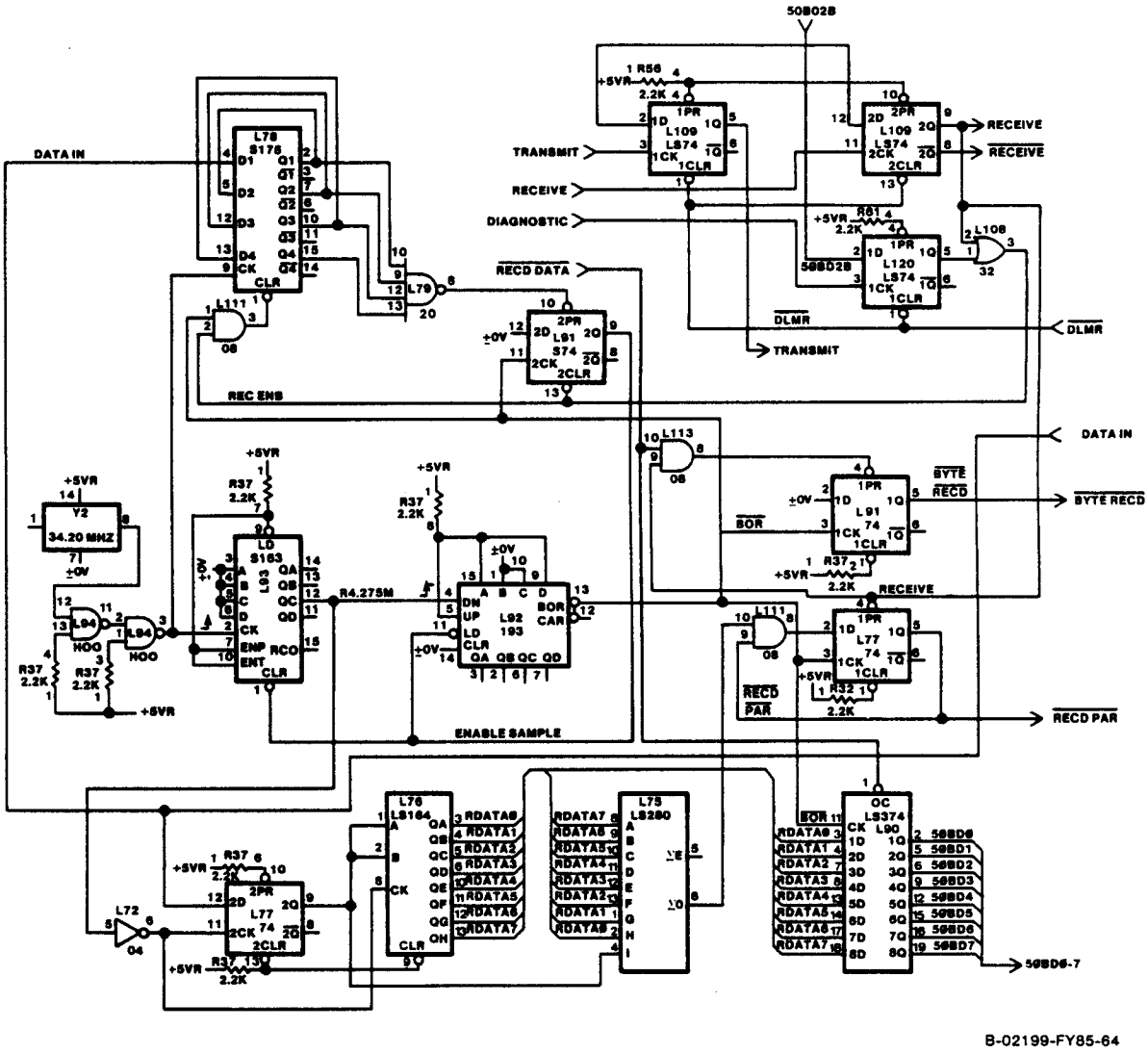

FIGURE 2.6-3
SDL Receive Logic

Data enters the RMU board via Serial Data Link Receivers L136 and L139 (3E-F7). Each 11-bit data word contains a start bit, eight data bits, a parity bit, and a stop bit. Data from the Serial Data Link channels is supplied to Receive Channel Selector L121 (3F6), which selects a data channel according to the signals (on its input pins 2 and 14) from the Channel Select Flipflops (L125). L121 transmits (on pin 7) data from the selected channel as the DATA IN signal.

L78 (3F12), the Start Bit Detector, samples the data stream (DATA IN) from the Receive Channel Selector at a 34.20-MHz rate to detect the Start Bit and to determine that the received word is legal. Upon detecting a legal Start Bit, L78 causes L79 to issue a low signal that presets Enable Sample Flipflop L91 (3E11). When the preset of L91 is held low and the clear pin of L91 is held high by an active REC ENB signal, L91 generates the Enable Sample signal. ENABLE SAMPLE asserts the Receive Shift Frequency Generator (L93 (3C12), pin 1) and the Receive Bit Counter (L92 (3C13), pin 11) to initiate their timing functions.

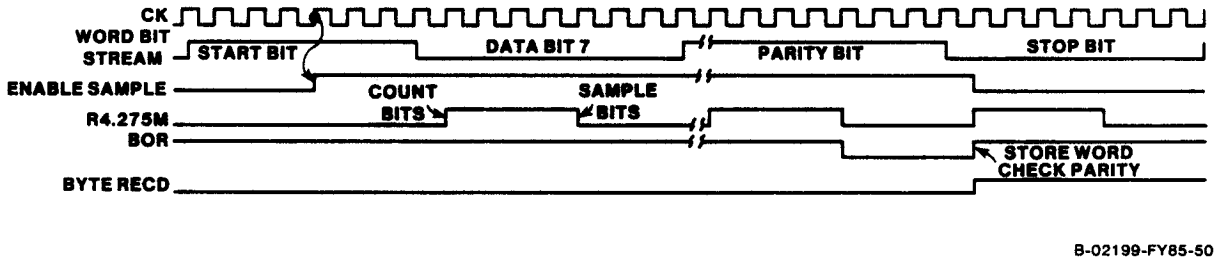

FIGURE 2.6-4
SDL Receive Timing

Serial Received Data Shift Register L76 (3A12) receives (via L77) eight of the 11 bits in a data word, assembles these bits into an 8-bit word, and then places this word onto Data Bus RDATA0-7. L75 (3A11), the 9-bit Serial Received Data Parity Checker, examines the received data's parity bit; if the data has the correct (ie, odd) parity, L75 issues a high signal to Parity Latch L77 (3C9). Upon receipt of the Received Data (&RECD DATA) enabling signal and the Serial Data Link Receive Borrow Strobe (&BOR) clocking signal, Received Data Bus Buffer L90 (3A9) places RDATA0-7 onto the 50BUS.

Receive Shift Frequency Generator L93 and Receive Bit Counter L92 derive the receive logic timing signals from the 34.20-MHz signal generated by SDL Clock Generator Y2. L93 uses the 34.20-MHz signal to generate a 233-ns (4.275-MHz) signal that asserts L77 (3A13) pin 11 to clock data in. L92 counts the nine bits (eight data bits plus a parity bit) contained in each word it receives and generates &BOR upon receipt of each complete word. &BOR then clocks the Receive Parity Flipflop (L77 (3C9)) and the Receive Control Flipflop (L91 (3D9)), causing them to generate the Received Parity (&RECD PAR) and Byte Received (&BYTE RECD) signals. &RECD PAR is fed to the SDL Status Register, and &BYTE RECD clears the &CL HALT (Clear Halt) signal via L113 and L146 (3I2) to inform the Microcontroller that the Serial Data Link has completed the receive operation.

2.6.3 Transmit Operations

Serial Data Link transmit operations are initiated when the 8X305 Microcontroller issues a 0H code on Address Bits 50BA0-3 and &50BSLCT1 (50BUS Device Select 1) and &50BREQ (50BUS Byte Request) are active. Command Decoder L110 responds by issuing the Transmit Data (&XMIT DATA) signal. &XMIT DATA clocks the data to be transmitted from the 50BUS (50BD0-7) onto the TDATA bus via Transmit Data Bus Buffer L74 (3A7). FIGURE 2.6-5 and 2.6-6 show the SDL Transmit Block Diagram and the SDL Transmit Logic. FIGURE 2.6-7 illustrates transmit operation timing signal interaction.

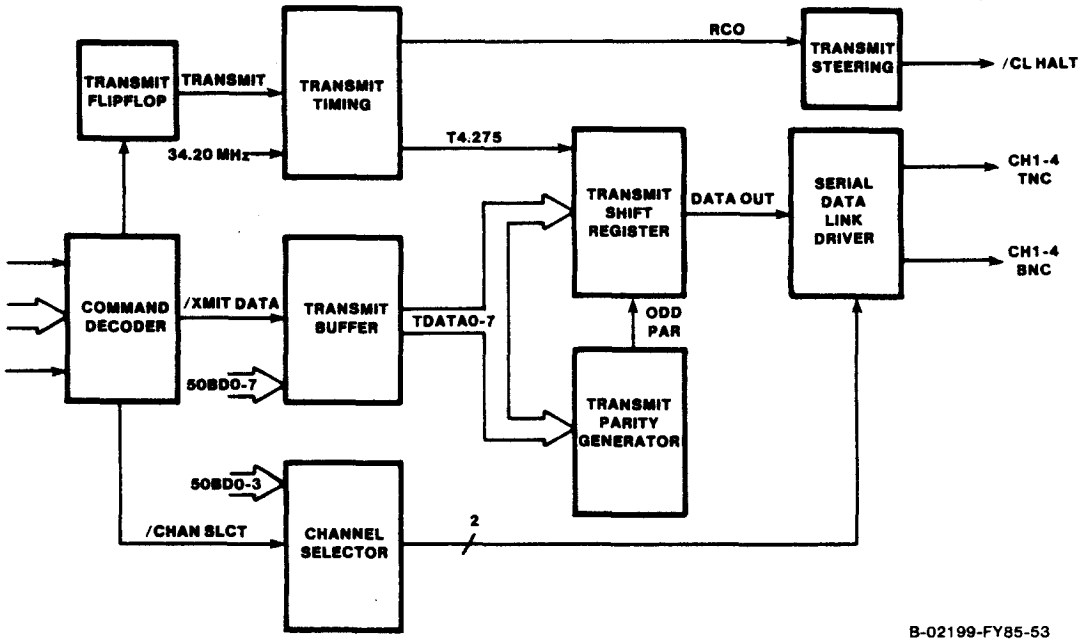

FIGURE 2.6-5
SDL Transmit Block Diagram

After issuing the &XMIT DATA signal, Command Decoder L110 issues the Transmit signal (in response to instructions from the RCU). TRANSMIT from L110 pin 15 asserts Transmit Latch L109 (gate 1 (3F10)) to hold the transmit condition active. L109, in turn, issues TRANSMIT to enable the Serial Data Link transmit logic by deactivating (via L111) the signals that assert the clear pins of L56-59 (3B1-4 and 3C7). When TRANSMIT is activated, the transmit logic begins processing the data that was loaded by &XMIT DATA. Shift Control Flipflop L40 (3C6), which is enabled when the Transmit signal deactivates its preset pin, generates a Shift signal from pin 5 that follows the T4.275 input on L40 pin 3. The Shift signal asserts (via L44) the shift/load pins of the Transmit Shift Registers, L56-58, placing the registers in the shift mode.

Transmit Data Parity Generator L73 (3B5) generates odd parity for received data bits TDATA0-7. Transmit Serial Data Shift Registers L56, L57, and L58 shift the data in response to the 4.275-MHz transmit clock. The serial data stream is shifted to the SDL Drivers (via L56, pin 14) as the DATA OUT signal.

Data is transmitted out of the Serial Data Link logic by gating the DATA OUT signal through one of the four SDL Drivers (two each on L137 and L138). The Channel Select (&CH0-3SL) signals from Transmit Channel Selector L124 enable the driver for transmission.

Transmit Shift Frequency Generator L60 (3C8) and Transmit Bit Counter L59 derive the transmit logic timing signals from the 34.20-MHz signal generated by SDL Clock Generator Y2. After being enabled by the TRANSMIT signal, L60 converts the 34.20-MHz signal into a 233-ns (4.275-MHz) clock signal that is used to shift data out. Shift Control Flipflop L40 generates a signal from pin 6 that asserts L62 to introduce a 233-ns delay in the generation of the &BYTE REQ signal. This delay prevents &BYTE REQ from being generated too early and causing a race condition.

Transmit Bit Counter L59 counts each clock pulse from L60 to count the 11 bits (Start bit, eight Data Bits, Parity Bit, and Stop Bit) contained in each transmitted word. Upon counting the 11th bit, L59 generates the Carry Out (RCO) signal. When clocked by RCO, Byte Request Flipflop L61 (3C3) generates the &BYTE REQ signal to deactivate the Clear Halt (&CL HALT) signal. &BYTE REQ clears the &CL HALT signal via L113 and L146 (3I2) to inform the Microcontroller that the SDL has completed the transmit operation.

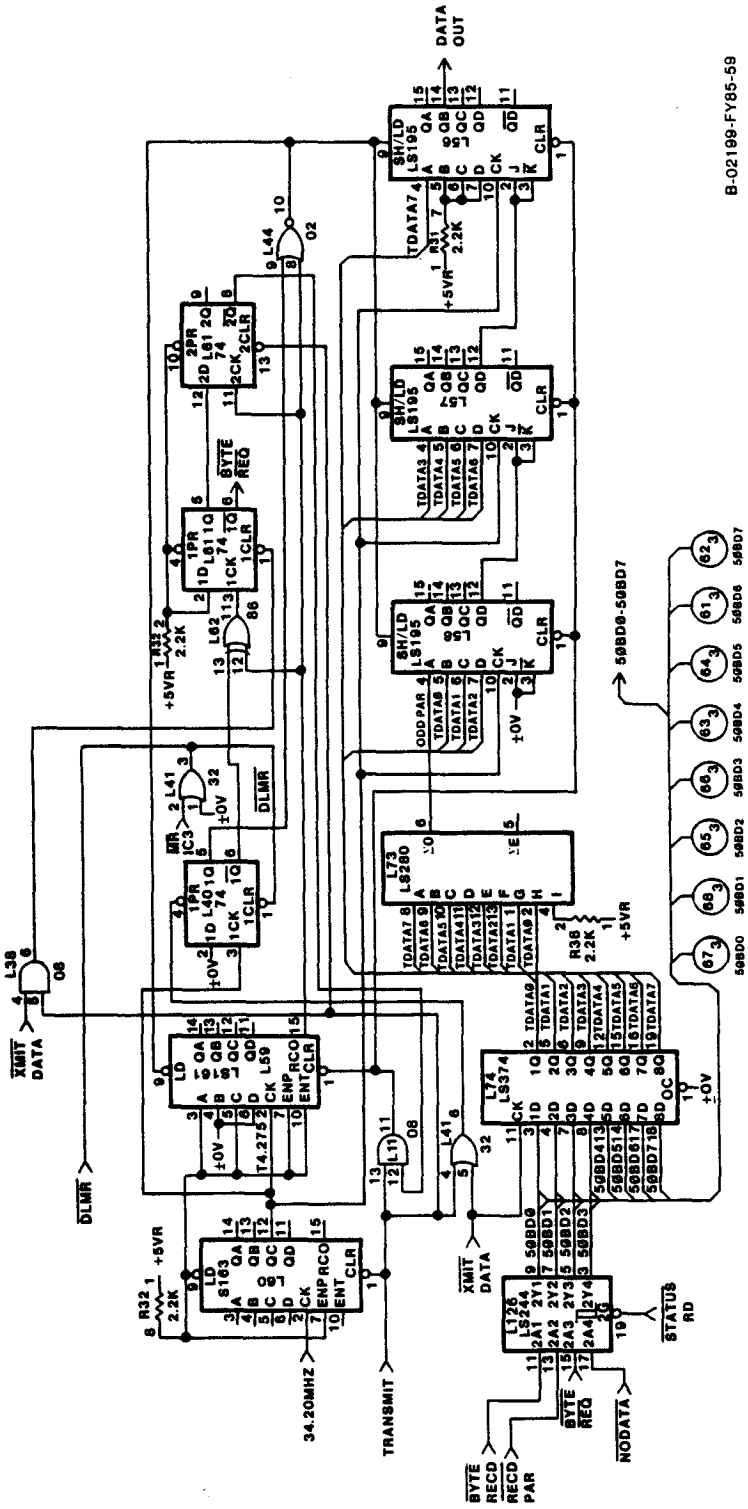

FIGURE 2.6-6
SDL Transmit Logic

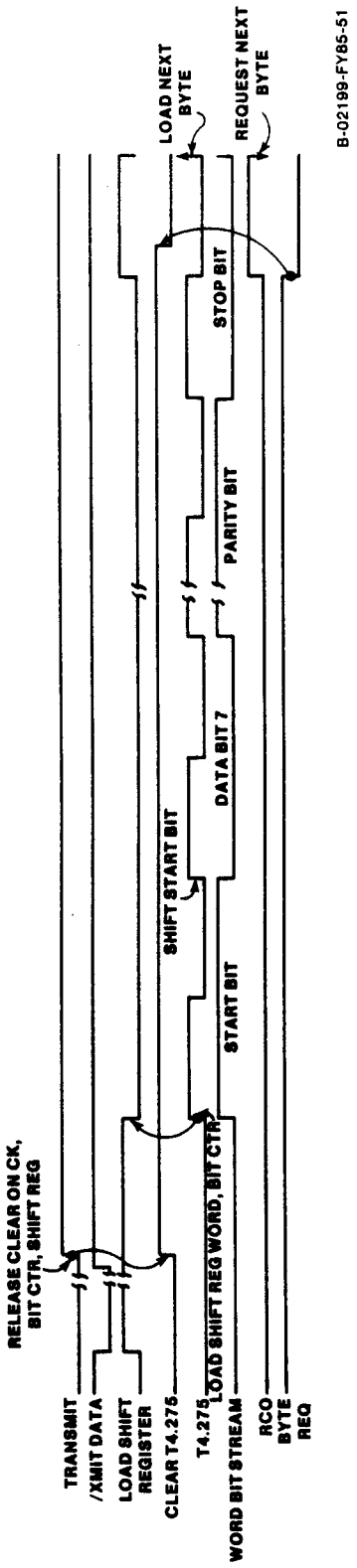

FIGURE 2.6-7
SDL Transmit Timing Diagram

&XMIT DATA clears Byte Request Flipflop L61 via L38 (3D6) as each new byte is loaded into the transmit logic; &XMIT DATA does not clear L61 at the end of the transmit operation, however, because no new bytes are being loaded into the transmit logic. If the Transmit signal is still active, L59 continues to count bits from the Transmit Shift Frequency Generator. When L59 generates the next RCO signal, L61 (3C2) generates a low signal (from pin 8) that clears the Shift Registers (via L111, pin 11 (3B11)) by activating the clear pins of the Shift Registers and the Bit Counter. A continuous data stream of zeros is shifted out of the Shift Registers until TRANSMIT is deactivated. Deactivating the Transmit signal at any time during the transmit operation also causes L111 to generate a signal (from pin 11) that clears the transmit logic.

2.6.4 Status Register

Four status bits and the 50BD0-3 Data Bus report the status of the SDL Transmit or receive logic to the 8X305. The Microcontroller accesses the SDL Status Nibble via SDL Status Register L126 (3A8) and the &STATUS RD command. Table 2.6-2 lists and defines the Status Bits.

Table 2.6-2: SERIAL DATA LINK STATUS BYTE

BIT	SIGNAL	DEFINITION
50BD0	&BYTE RECD	Generated by L91 to indicate that the Serial Data Link has received a data byte. Also clears the 8X305 halt condition.
50BD1	&RECD PAR	Generated by L77. Indicates that the Serial Data Link has received a data byte containing a parity error.
50BD2	&BYTE REQ	Generated by L61 to indicate that the Serial Data Link has transmitted a data byte. Also clears the 8X305 halt condition.
50BD3	&NO DATA	Generated by L127. Indicates that a Serial Data Link Receive operation was commanded, but either no data was received or the data was interrupted.

During receive operations, Receive Parity Flipflop L77 and Byte Received Flipflop L91 generate the Received Parity (&RECD PAR) and Byte Received (&BYTE RECD) signals (see Section 2.6.2). &BYTE RECD functions as a status signal and also deactivates the &CL HALT signal via L113 and L146 (Section 2.6.1). &RECD PAR from L77 functions only as a status signal.

L61 generates the &BYTE REQ signal to indicate that a byte of data is needed for transmission (see Section 2.6.3). &BYTE REQ functions as a status signal and also deactivates the &CL HALT signal via L113 and L146 (Section 2.6.1).

No Data Flipflop L127 (3H1) generates the &NO DATA signal to indicate that an SDL receive operation was commanded and initiated, but either no data was received or the data was interrupted. The No Data Timeout 1-Shot (L140 (3H2)) is activated when RECEIVE is active and DATA is inactive on the inputs of gate L112. L112 then generates a signal that triggers the 1-Shot via L128. If no data is received, the 1-Shot times out for 86 us and generates a signal from pin 7 to clock L127. If the No Data Flipflop is cleared by the inactive Receive signal within 86 us (prior to the clocking signal), it does not generate the &NO DATA signal. If, however, RECEIVE is still active when the clock signal arrives, L127 issues the &NO DATA signal from pin 8 to deactivate the Clear Halt (&CL HALT) signal via L146. Deactivating &CL HALT causes the 8X305 to function as if SDL command execution had proceeded normally. The 8X305 detects the no data condition when it reads SDL Status Register L126 at the completion of the receive command.

This concludes the theory of operation section for the RMU circuit board. Refer to Section 8 for troubleshooting tips for the Resource Management Unit (RMU).

SECTION 2 QUIZ

1) What two ways does the RCU have to inform the RMU that a non-immediate command has been completed?

2) If SW1 is depressed during TESt 1 of the BIT what will happen?

3) What purpose does the AUTO RESET signal provide?

4) Why is the signal PWAIT generated during MMI/O operations?

5) What two way does the RCU have to request the Data and Address busses of the RMU?

6) What are the two sources of Non-Maskable interrupts for the Z80A on the RMU?

7) Which bit of the Address bus is used as a synthetic refresh bit?

8) The PROM enabling flipflop performs what function?

9) What are the three phases of a floppy drive access?

10) If the dead-man timer is not reset after 540 nsec what happens?

11) How many commands are used to communicate between the RCU and the SDL?

12) What do the four bit of the SDL status register indicate?

SECTION 3
RESOURCE CONTROL UNIT (RCU)

SECTION 3

Resource Control Unit (RCU)

3.1.1 GENERAL INFORMATION

The 8267 Resource Control Unit (RCU) used in the OIS 40 and OIS 50 multiprocessor-based data processing systems contains the 4K x 8 Data Buffer, 1K-byte Scratchpad RAM, 16-byte Parameter Register File (PRF), 12-byte Status Register File (SRF), Winchester Disk Drive Interface, 50BUS Interface, and 10-MHz 8X305 Microcontroller. The 4K x 8 Data Buffer on the RCU board is a 4K-byte buffer used as a data storage area during all block data moves between any two boards in the OIS system. Scratchpad RAM is a temporary storage area for tables and program variables. The PRF is used as a common area for data moving between the Resource Management Unit (RMU) and the RCU. Status information sent from the RCU to the RMU uses the Status Register File as a intermediary storage area. The 50BUS is an internal bus that connects all devices within the OIS 50. The 8X305 Microcontroller maintains control over most RCU operations. FIGURE 3.1-1 is a block diagram of the Resource Control Unit.

The Microcontroller generates two control signals, called the Left Bank (LB) and Right Bank (RB) signals, to optimize its data accessing capabilities. By providing left and right bank I/O options, the Microcontroller can access a total of 512 ports. The Microcontroller in the RCU maintains 256 x 8 bytes of Scratchpad RAM on its left bank as a temporary storage area for tables and program variables. The RCU's right bank contains I/O port commands to control major RCU functions.

The RCU's 4K x 8 Data Buffer serves as a temporary storage area for data passing between the RCU and the Winchester or floppy disk drives. The Microcontroller uses 4K x 16 bytes of RCU-resident PROM to store its instruction code. Addresses for PROM-resident instructions are generated by the Microcontroller and sent to the PROM via the XA0-12 bus. XA1, the control bit of the XA0-12 bus, selects high-order (active XA1) or low-order (inactive XA1) PROM.

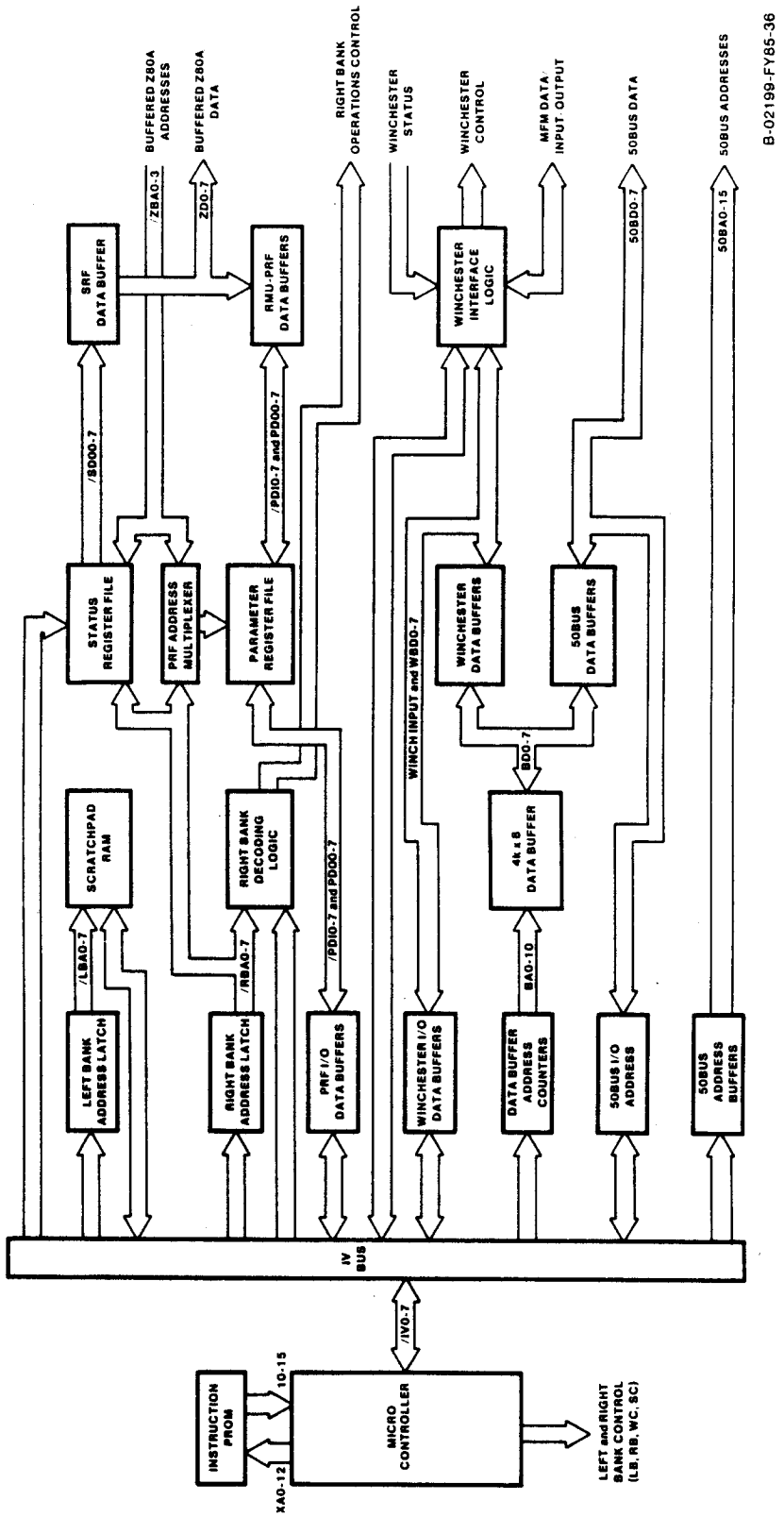

FIGURE 3.1-1
Block Diagram of the Resource Control Unit

During Winchester read/write operations, the Microcontroller controls the Winchester disk drive and loads or empties the 4K x 8 Data Buffer. When the Winchester access operation has been completed, the Microcontroller presents status information (via the Status Register File) and the Control Unit Not Busy (&CUBUSY) interrupt to the Z80A. The Winchester Seek Complete (WSKCMP) interrupt is generated by the Winchester disk drive and sent directly to the Counter Timer Chip (CTC, channel 2) on the RMU board.

3.1.2 RMU-RCU Interaction

RMU-RCU communication involves shared memory, a Command Notification (&CMD) bit, and the 8X305 Microcontroller interrupts that assert the Z80A. Two memory areas on the RCU board are shared between the Z80A and the Microcontroller: the 16-byte Parameter Register File (PRF) and the 12-byte Status Register File (SRF). Both the Z80A and the Microcontroller can read from or write to the PRF; however, they cannot access the PRF simultaneously. Only the Z80A can read the SRF, and only the Microcontroller can write to it.

The RCU receives RMU requests via the Parameter Register File. The Z80A microprocessor on the RMU loads the PRF with the command codes and data that the RCU needs to perform a specific operation. When the Z80A sets the Command Notification bit, the Microcontroller operates on the PRF as needed to complete the command. (Generally, the Microcontroller moves the PRF data to its Scratchpad RAM and then releases the PRF.) The PRF must be released quickly because the Z80A is suspended (ie, held in a bus request state) while the Microcontroller controls the PRF. If the Z80A is suspended for too long a time, the RAM on the RMU board will decay due to the lack of Z80A-generated refresh cycles.

PRF byte assignments depend upon the function requested (see Appendix G). Typically, the Z80A issues the FF20 (Command Request) byte and the FF22 (Specify Command) byte to the PRF. The RCU reads the bytes, defines the remaining bytes according to specific command requirements, and then returns the FF21 (Command Acknowledge) byte to the PRF for the Z80A to read. To avoid invalid parameter errors, unused or undefined bytes should always be cleared to zero.

To perform a function that involves the RCU, the Z80A loads the command request and necessary data into the PRF. The Z80A then writes to address FF30 to issue the Command Notification bit that initiates the command. Normally, the Microcontroller is polling, waiting for the Command Notification bit to be set. When the RMU issues a command, the Microcontroller can perform one of two routines. If the command is an immediate command, the Z80A is awaiting command completion and the RCU must, therefore, execute the command immediately. If, however, the command is a non-immediate command, the RCU releases the Z80A after moving the data from the PRF to the scratchpad. The RCU then executes the command and notifies the Z80A upon completion.

Upon receiving an immediate command, the RCU checks to see that the command code is valid, copies the PRF to its scratchpad RAM, completes the requested operation, and releases the RMU. When the 8X305 Microcontroller performs a 1-byte operation, for example, it does not immediately release the PRF. The Microcontroller holds the Z80A in a suspended state for a maximum of 1 ms (otherwise the lack of dynamic RAM refresh could cause a memory data loss). When the Microcontroller releases the Z80A, the data and/or status information from the 1-byte operation is immediately available to the Z80A via the SRF.

Upon receipt of a non-immediate command, the RCU checks to see that the command code is valid, copies the PRF to its scratch RAM, sets RCU Busy status in the SRF, releases the RMU, completes the requested operation, and issues either an interrupt request or a Control Unit Not Busy (&CUBUSY) signal to the RMU when the operation has been completed.

Status and error information returns to the RMU via the dual-ported SRF. When the Microcontroller is busy, RCU Busy status information is set in byte FF10 of the SRF. Status information concerning Data Link block operations resides in SRF bytes FF11 and FF12. SRF bytes FF13-FF15 contain status information concerning the 1-byte Serial Data Link operations, and bytes FF16-FF1B contain status information concerning the Winchester Disk Drive.

3.1.3 RMU-RCU Interface

The interface between the Resource Control Unit (RCU) and the Resource Management Unit (RMU) resides on the RCU board. FIGURE 3.1-2 shows a block diagram of this interface. Data passing to and from the Z80A on the RMU must pass through L149 (1I10), a data transceiver. The direction of the data flow is determined by the decoding of the MMI/O signals sent from the RMU. Table 3.1-1 lists the MMI/O commands generated by the Z80A. L98 (1J13) decodes the commands by looking at the upper nible of the lower byte of the Z80A port address (A4-7). Looking at Table 3.1-1 you can see that the upper nible of the lower byte only changes from a 1 through a 4, thus selecting the command. The lower nible of the lower byte selects the address in either the (PRF) or (SRF) that the data is to transferred. The upper byte of the port address is always FF for MMI/O operations.

There are three buffers connected to the B side of L149. Two of these buffers are use to transfer data to and from the (PRF), while the other buffer allows the (SRF) to sent data to the Z80A. The selection of these buffers is either from decoding of the Z80A MMI/O signals or form the 8X305 Microcontroller.

The (SRF) is comprized of six LS670's, these are 4-by-4 register files with each containing separate read and write address inputs. When the Z80A wishes to read the status of an operation the address is decoded using L98 (1J13), L99 (1H13) and L103 (1I12). This decoded address is sent to pin 4, 5 and 11 of each of the chips. Pins 4 and 5 select the location within the chip while pin 11 selects the chip for a read operation. The actual chip selection is determined by L103 through address bits BA2-3. L103 also selects the (SRF) data buffer through L86 (1G11) thus allowing the selected data to pass to the data transceiver. The status information in the (SRF) was written into it by the 8X305 Microcontroller. The data was presented to each of the chips from the IV0-7 data bus, while the address was sent to pin 12, 13 and 14. Pins 13 and 14 did the selection of the location within the chip, while pin 12 selected the chip. Chip selection was generated from dacoder L79 (2F6). This information is decoded from the data generated by the 8X305.

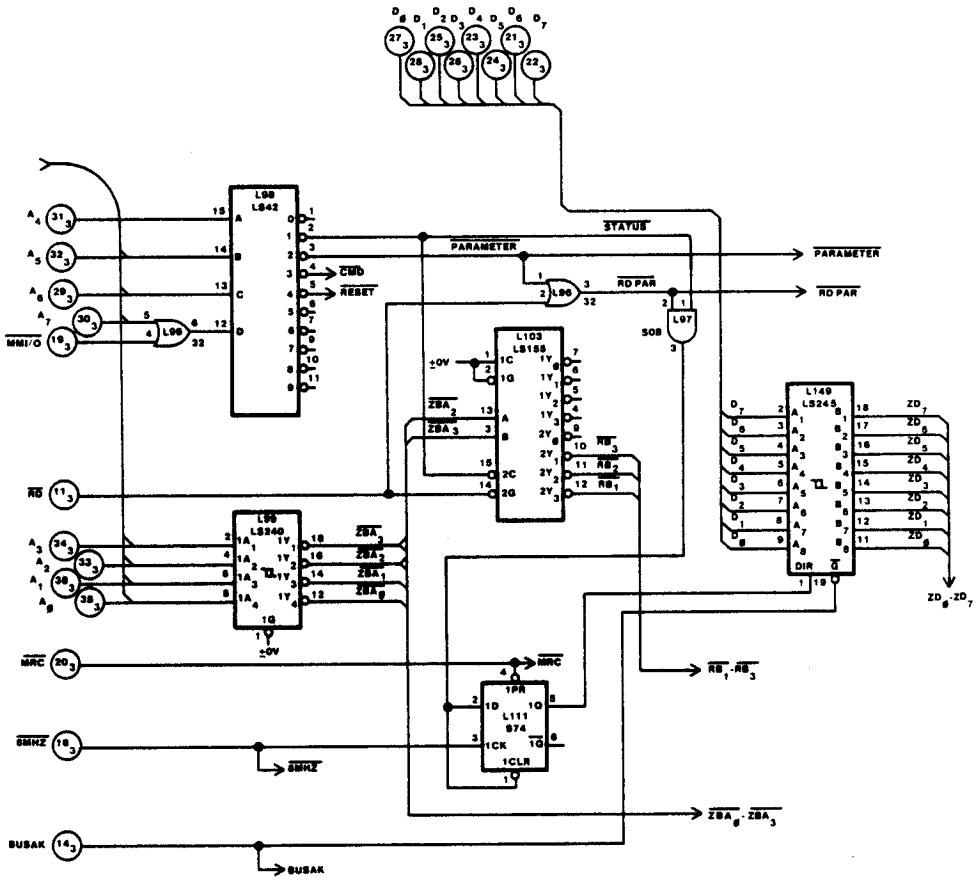

FIGURE 3.1-2
RMU/ RCU Interface Block Diagram

The Parameter Register File can be written to by the Z80A to instruct the RCU to perform an operation. The parameters are passed through the data transceiver and on to the inputs of L116 (1F9) the (PRF) Input Data Buffer. At this time the Z80A generates a write to the paramter register which is decoded by L98 (1J13). L98 will generate &PARAMETER which will enable L116 the (PRF) Input Data Buffer and both L100 and L101 (1B8-10), the (PRF). Since the Z80A is writing to the (PRF) it will also generate &WR, entering at (1A14). &WR is gated with &PARAMETER through L64 (1A11) and L97 (1A10) to activate the write enbale of the (PRF). After all of the parameters are stored in the (PRF) the Z80A will then set the CMD bit, informing the RCU that a command is pending.

The (PRF) can also be read by the Z80A. This is accomplished by the Z80A reading MMI/O loaction FF20-FF2F. The Z80A issues a &RD along with the address within the (PRF) that it wishes to read. The &RD signal is gated with &PARAMETER through L76 (1J12) to generate &RD PAR. &RD PAR has two functions, first it is gated through L97 (1J11) to the Data Direction Control Flipflop. On the next clock pulse from the 8Mhz clock the data transceiver will be placed in the B-to-A mode. The second function of &RD PAR is two fold, first it enables the (PRF) Data Out Buffer and second it enables the (PRF) memory chips by driving pin 2 of L00 and L101 low.

The location within the (PRF) that the data is to be transfered to or from is selected by L102 (1D10). This data selector selects addresses from either the Z80A or the 8X305 Microcontroller. The Z80A address come from the same circuits that generated the address for the (SRF), while the address from the 8X305 Microcontroller are generated by L85 (2G8) (more on this later). L102 receives its select signal from L25 the Command Bus Request Flipflop. This flipflop is normaly in the reset state, thus deactivating CMDBUSREQ causing the select input of L102 to select the A inputs. If this were a write operation to the (PRF) the Z80A would issues a CMD command after all the data had been transferred, thus causing L25 to set causing the RCU to start the its operation.

The Z80A set L25 by issuing FF30-FF3F MMI/O instruction, this forces L98 to activate &CMD. &CMD is placed directly on the preset input of L25 forcing it set. The Q output of L25 will go high activating CMDBUSREQ causing L102 to select the RCU address information. At the same time the &Q output will go low, causing several things to happen. First this low is sent back to the RMU notifing the Z80A that the RCU is performing an operation. Secondly this low is sent to L133 the IV Bus to (PRF) Input Data Bus Buffer. Here it activates L133 allowing the 8X305 the ability to write data into the (PRF) if needed during the operation. Lastly the low on the 2Q output of L25 is sent to L94 (1B7).

Table 3.1-1: Z80A-GENERATED I/O COMMANDS

Z80A Port Address	I/O Command	Function
FF10-FF1F (R)	&STATUS	Read the 12-byte Status Register File. Data located in FF10-FF1B are the result of a previously executed Microcontroller command. FF1C-FF1F are not used.
FF20-FF2F (W/R)	&PARAMETER	Read or write the 16-byte Parameter Register File. The read or write operation is specified by the condition of the Z80A Read Request (&RD) signal from the RMU board.
FF30-FF3F (W)	&CMD	After the Z80A writes to any location in the (PRF) it will set Command Bus Request Flipflop. The &CMD bit generates the Command Bus Request (&CMDBUSREQ) signal to notify the Microcontroller that a command has been loaded in the PRF and the Z80A has surrendered bus control.
FF40-FF4F (W)	&RESET	Accessing any one of the 16 PRF locations generates a Z80A Reset (&RESET) signal that resets the Microcontroller and, therefore, the RCU board.

The 8X305 Microcontroller is normaly in a poling mode of operation, and during this operation it will activate &RD INPUT DATA and &COMMAND. These two signals will activate the trystate input of L94, thus allowing the low on pin 2 to be placed on IV7 of the 8X305 bus. The 8X305 Microcontroller will check this bit, looking for it to be low (which it is). Once the 8X305 find this bit low it will start reading the (PRF) to determine what operation it is to perform.

3.2: 8X305 MICROCONTROLLER

The RCU's 8X305 Microcontroller (see FIGURE 3.2-1 and 3.2-2) controls most of the OIS 50's functions. Instructions for the Microcontroller arrive from the 4K x 16 PROM storage area via the 16-bit I0-15 instruction bus. Addresses for PROM-resident instructions are generated by the Microcontroller's address bus (XA0-12). Designed to operate with a 200-ns instruction execution cycle, the Microcontroller controls a series of peripheral devices attached to it by means of the 8-bit Interface Vector (IV) bus. The IV bus issues signals to Microcontroller Data Transceiver L69 which, in turn, generates the &IV0-7 Interface Vector bus. The Microcontroller does not use typical conventions for bit identification: on all of its buses (I0-15, XA0-12, and IV0-7), a subscript of "0" denotes the most significant bit (MSB) and the highest subscript denotes the least significant bit (LSB). The Microcontroller sends control signals to L38, the Control Signal Decoder, to create the necessary peripherals control signals.

Five control signals generated by the Microcontroller indicate the direction in which the IV bus is being driven and the type of data on the bus. Any one of up to 256 addresses (per bank) can be selected in a single instruction cycle when the Microcontroller places a unique address on the IV bus and asserts the Select Command (SC) signal. Once selected, the address normally remains selected until the SC signal is again asserted with a different address on the IV bus. The direction of data flow is indicated by the Write Command (WC) signal. The WC signal is asserted when data is being placed on the IV bus, and is not asserted when data is read from the IV bus. An IV bus read is indicated when both the SC and WC signals are inactive.

Two control signals, the Left Bank (LB) and Right Bank (RB) signals, optimize the Microcontroller's data accessing capabilities. Either of these signals is asserted concurrently with other control signals based on the contents of the instruction word. The LB and RB signals allow 512 addresses (256 on each bank) to be accessed during a single microcontroller instruction cycle. Timing on the bus is synchronized with the Master Clock (MCLK) signal. Together with the other control signals, MCLK enables access to the IV bus at the correct time in the Microcontroller's instruction cycle. The left bank reads or writes 256 bytes of Scratchpad RAM, and the right bank issues I/O Port commands, which control many OIS 50 functions.

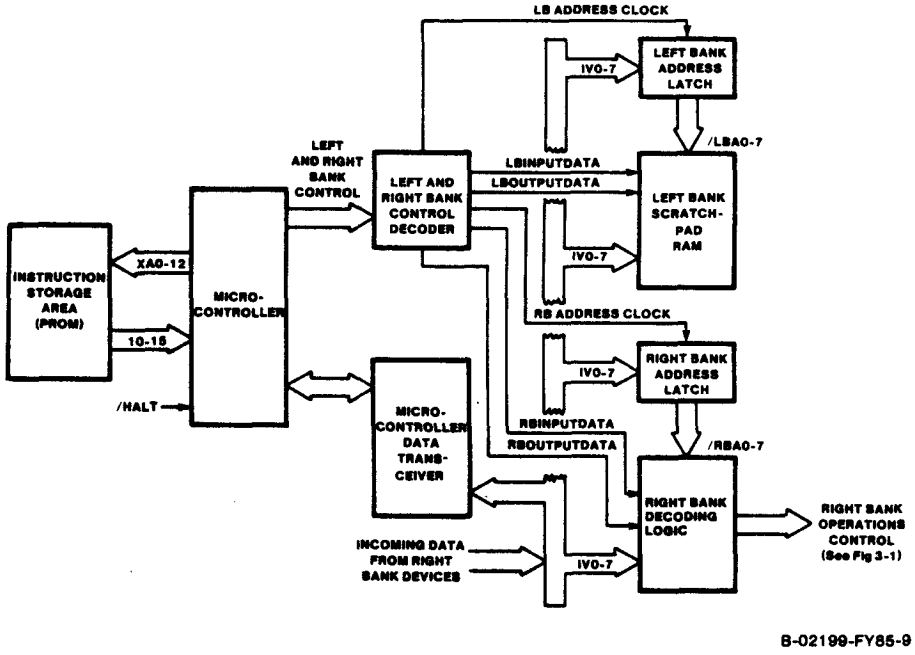

FIGURE 3.2-1

8X305 Microcontroller Block Diagram.

Control Signal Decoder L38 receives four of the five primary control signals as inputs (barring the Master Clock). The signals issued from L38 depend, of course, on the status of the incoming signals. Table 3.2-1 lists the outputs generated by the various input combinations.

The Left Bank Input Data (&LBINPUTDATA) and Right Bank Input Data (&RBINPUTDATA) signals are used throughout the logic to enable either left or right bank read operations. The Left Bank Output Data (&LBOUTPUTDATA) and Right Bank Output Data (&RBOUTPUTDATA) signals enable either left or right bank write operations. The direction of the Microcontroller's Data Transceiver, L69, is controlled by either the active &RBINPUTDATA or the active &LBINPUTDATA signal asserting L69 pin 1 (via L97), depending on which bank has control of the read or write operation.

Table 3.2-1: MICROCONTROLLER CONTROL SIGNAL DECODER

Control Signals Active	Decoder Output Signals Active
WC, &LB	&LBOUTPUTDATA and WC (from pin 6)
SC, &LB	&LBINPUTDATA
SC, WC, &RB	&RBOUTPUTDATA and WC (from pin 10)
SC, &RB	&RBINPUTDATA

If either &RBINPUTDATA or &LBINPUTDATA is active, L97 generates a low signal that asserts pin 1 of Microcontroller Data Transceiver L69 to place the transceiver in the input direction (B-to-A). An inactive &RBINPUTDATA or &LBINPUTDATA signal places the data transceiver in the output direction (A-to-B). &RBOUTPUTDATA is synchronized with the Microcontroller's Master Clock (MCLK) signal at L81 to generate the &RBODMCLK signal. &RBODMCLK is used by all of the right bank decoders to synchronize write operations. &LBOUTPUTDATA is gated with &MCLK at L64 to generate a synchronized signal which asserts the write enable pin of the left bank scratchpad memory.

The Write Command (WC) signal is decoded from Control Signal Decoder L38 for use as an address write control signal for either the left or right bank (whichever is being asserted by the Microcontroller). If the left bank address is being accessed, L38 pin 6 asserts L26 pin 12, driving it low, which allows the &MCLK signal through to the output of L26 pin 13. From L26 pin 13, the left bank &MCLK signal then clocks L68, the Left Bank Address Latch, to store left bank addresses &LBA0-7. &LBA0-7 address 256 bytes of scratchpad RAM. If the right bank is being accessed, L38 pin 10 asserts L26 pin 9, driving it low, which allows the &MCLK signal through to the output of L26 pin 10. From L26 pin 10, the right bank &MCLK signal then clocks Right Bank Address Latch L85 to store right bank addresses &RBA0-7. &RBA0-7 are sent to decoders throughout the right bank circuitry to decode the I/O ports that control the primary RCU functions.

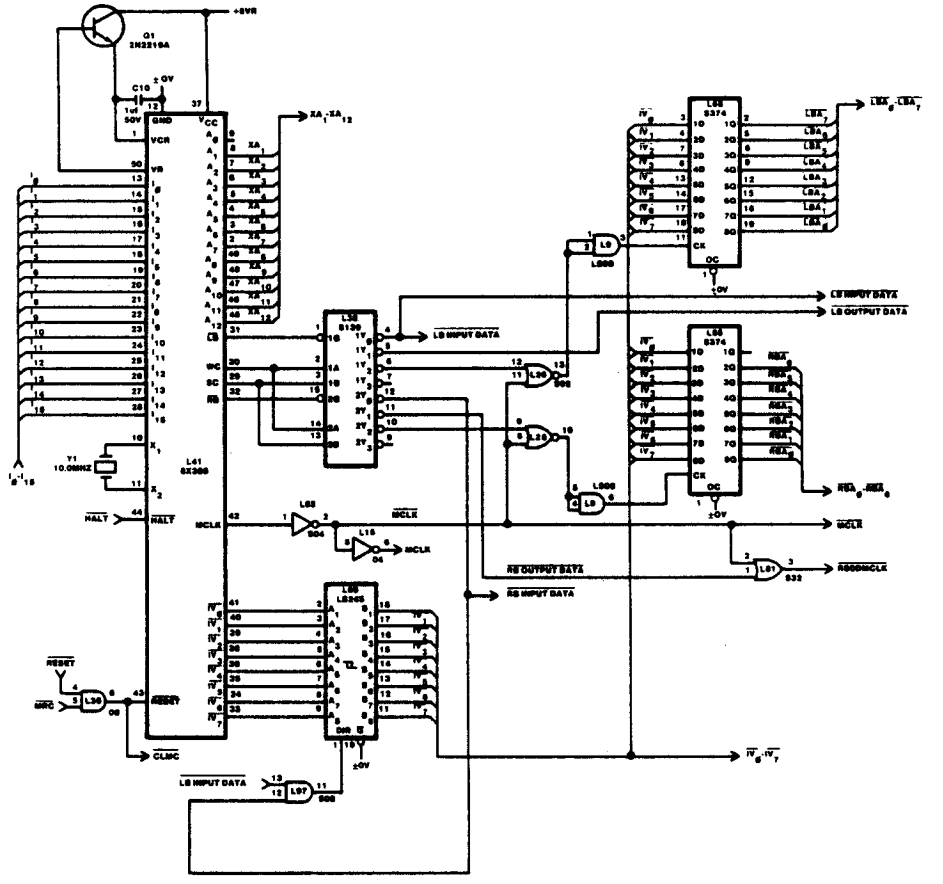

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FIGURE 3.2-2
8X305 Microcontroller Access Logic

3.2.2 Microcontroller Instruction Storage Area

Four 2K x 8 PROMs provide the 4K x 16 storage area needed for the Microcontroller's instructions set. These PROMs are addressed by a 13-bit address generated by the Microcontroller's address bus (XA0-12). The PROM places the 16-bit addressed instruction onto the I0-15 instruction bus, where it is sent to the Microcontroller for execution. L40 and L54 contain the low-order (from 0 to 2k) addressed PROM, as addressed by XA0-12. When accessing low-order PROM, L54 provides the high byte (I0-7) of the 16-bit instruction, and L40 provides the low byte (I8-15). (As explained earlier in this chapter, the Microcontroller uses an atypical convention for bit identification.) L39 and L53 contain high-order addressed PROM, from 2 to 4k, as addressed by XA0-12. When accessing high-order PROM, L53 provides the high byte (I0-7) of the 16-bit instruction, and L39 provides the low byte (I8-15). High or low order PROM is specified by the XA1 bit of the Microcontroller's address bus. Inactive XA1 asserts the low enabling pin 20 of the low-order PROM chips (L40 and L54) to enable these chips when low-order PROM is accessed. High-order PROM is enabled by the active XA1 signal asserting enabling pin 18 of L39 and L53.

3.2.3 Left Bank Scratchpad Memory

The Microcontroller uses 256 x 8 bytes of scratchpad RAM (in two 256 x 4 chips, L66 and L67) on its left bank as a temporary storage area for tables and program variables . Table 3.2-2 displays the memory map configuration of the scratchpad.

Table 3.2-2: SCRATCHPAD MEMORY MAP

Memory Location (Hex)	Memory Contents
00-0F	Parameter Register File data supplied by the RMU. Parameters are typically retrieved and decoded from the scratchpad copy of the PRF, not directly from the PRF. Some diagnostic support routines directly access and decode parameters from the PRF without copying the PRF in the scratchpad.
10-19	Physical to logical slave address mapping table. This table is created by the set slave list command.
1A-23	Hardware select code for each slave type. Slave's physical addresses are used to index this table for select codes. Slave — Physical Address — Select Code Master Memory — 00 — 01 IWS 1 — 01 — 08 IWS 2 — 02 — 10 IWS 3 — 03 — 20 IWS 4 — 04 — 40 IWISE — 05 — 80 Serial Port 1 — 06 — 02 Serial Port 2 — 07 — 02 Serial Port 3 — 08 — 02 Serial Port 4 — 09 — 02
80	Start of variable area which ends at location FF. The variable area is cleared upon power on.

Table 3.2-2: SCRATCHPAD MEMORY MAP (cont.)

80	1-byte cell devoted to serial device status Operations.
81	1-byte cell devoted to the control byte for Winchester operations.
82-83	Working storage used to count the number of headers that have passed since the beginning of the Winchester read or write operation. Currently, this number is only an 8-bit number, with location 83 reserved for expansion.
84-86	ECC syndrome or check bytes from the previous read or diagnostic read operation. The first ECC byte resides at location 84.
87	1-byte flag indicating the condition of the Winchester to slave memory chaining operation.
88-8A	Desired header bytes when chaining a Winchester write to slave read. Location 88 contains a copy of the value of FF24. Location 89 contains a copy of the value of FF25. Location 8A contains a copy of the value of FF26.
8B	1-byte flag indicating an error in a slave memory read operation. Data read is intended to be written to the Winchester.
8C-8F	32-bit count of ECC errors since power on. Byte 8C is the least significant byte. The count is not cleared when the RMU resets the RCU.
90-93	32-bit count of Winchester sector read operations since power on. Byte 90 is the least significant byte. The count is not cleared when the RMU resets the RCU.
94-97	32-bit count of Winchester sector write operations since power on. Byte 94 is the least significant byte. The count is not cleared when the RMU resets the RCU.

Table 3.2-2: SCRATCHPAD MEMORY MAP (cont.)

98-9B	32-bit count of parameter errors since power on. Byte 98 is the least significant byte. The count is not cleared when the RMU resets the RCU. One byte to master memory operations are not counted.
9C-9F	32-bit count of serial receive data parity errors since power on. Byte 9C is the least significant byte. The count is not cleared when the RMU resets the RCU.
A0-A3	32-bit count of header not found errors since power on. Byte A0 is the least significant byte. The count is not cleared when the RMU resets the RCU.
A4-A7	32-bit count of header LRC errors since power on. Byte A4 is the least significant byte. The count is not cleared when the RMU resets the RCU.
A8-AB	32-bit count of RCU resets (by the RMU) since power on. Byte A8 is the least significant byte. The count is not cleared when the RMU resets the RCU.
AC-AF	Not used.
B0	Constant number (96 decimal) initialized at power on. This constant provides three disk revolutions during which the maximum number of headers is examined before declaring that a requested sector cannot be found (i.e. header not found error). Diagnostics may change this value in order to tighten the sector-finding window.
B1-B3	24-bit test pattern, initialized at power on. When reset, the Microcontroller checks for the initialized pattern. If the pattern is present, the Microcontroller executes a reset sequence. If the pattern is absent, the Microcontroller generates the pattern and initiates the power-on sequence.

A primary function of the scratchpad is to act as a temporary storage area for data moving between the Microcontroller and the PRF or SRF. Typically the Microcontroller accepts data from the PRF and places this data into the scratchpad. The Microcontroller accesses data in the scratchpad to perform an RMU-requested operation and then returns the necessary data to the scratchpad. Data from the scratchpad is then read again by the Microcontroller (via a left bank operation) in order to place the data into either the PRF or the SRF (via a right bank operation). PRF- or SRF-based data is available to be read by the the Z80A on the RMU board.

The Microcontroller provides addresses to the scratchpad for the scratchpad access operation via the &IV0-7 bus as shown in FIGURE 3.2-3. Addresses from the &IV bus are buffered through L68, the Left Bank Address Latch, onto the left bank address bus (&LBA0-7). The bit weights of the addressed data on the &IV bus are reversed at the output of L68. Therefore, IV0, which is the most significant bit on the &IV bus, becomes &LBA7, the most significant bit on the &LBA bus. The &LBA addresses from L68 assert the address pins of scratchpad chips L66 and L67. Data to be stored at the &LBA addresses comes into the scratchpad directly from the Microcontroller's &IV bus. Scratchpad chip L67 handles the high-order data nibble (&IV0-3), and L66 handles the low-order nibble (&IV4-7). Data is read from the scratchpad through the Scratchpad Data Output Buffer (L83) and onto the &IV bus.

Under the control of the 8X305 Microcontroller, data is read from the PRF via the right bank and then loaded into the scratchpad on the left bank. Data is drawn from the PRF through the PRF Data Output Buffer (L84), onto the &IV bus, and then to the Microcontroller. The Microcontroller then transfers the data to the scratchpad on the left bank.

Scratchpad data destined for the PRF or SRF is first read from the scratchpad (into the Microcontroller) via Scratchpad Output Buffer L83 when &LBINPUTDATA is active on the buffer's enabling pins. The Microcontroller then writes the outgoing data from the &IV bus to the PRF via L133, the PRF Data Input Buffer. Scratchpad data destined for the SRF is read by the Microcontroller and then written to the SRF directly from the &IV bus. The Microcontroller provides addresses for the PRF and SRF via its right bank ports. Control of PRF Data Input (L133) and Output (L84) Buffers is also maintained by a right bank I/O command.

Scratchpad read and write operations are controlled by the &LBOUTPUTDATA and &LBINPUTDATA signals generated by Control Signal Decoder L38. During a scratchpad write operation, &LBOUTPUTDATA is active on L64 pin 1. Since L64 pin 1 is low, the &MCLK signal from the Microcontroller controls the output of L64 (pin 2), which clocks the Write Enable (&WE) pin (pin 20) of scratchpad chips L66 and L67 to perform a write operation. The Microcontroller reads scratchpad data via Scratchpad Output Buffer L83 and then passes that data to the SRF or PRF by means of a right bank operation. Since the output enable pin of the scratchpad is always enabled, data is read from the scratchpad onto the &IV bus when the enabling pins of Scratchpad Output Buffer L83 are driven low by the active &LBINPUTDATA signal.

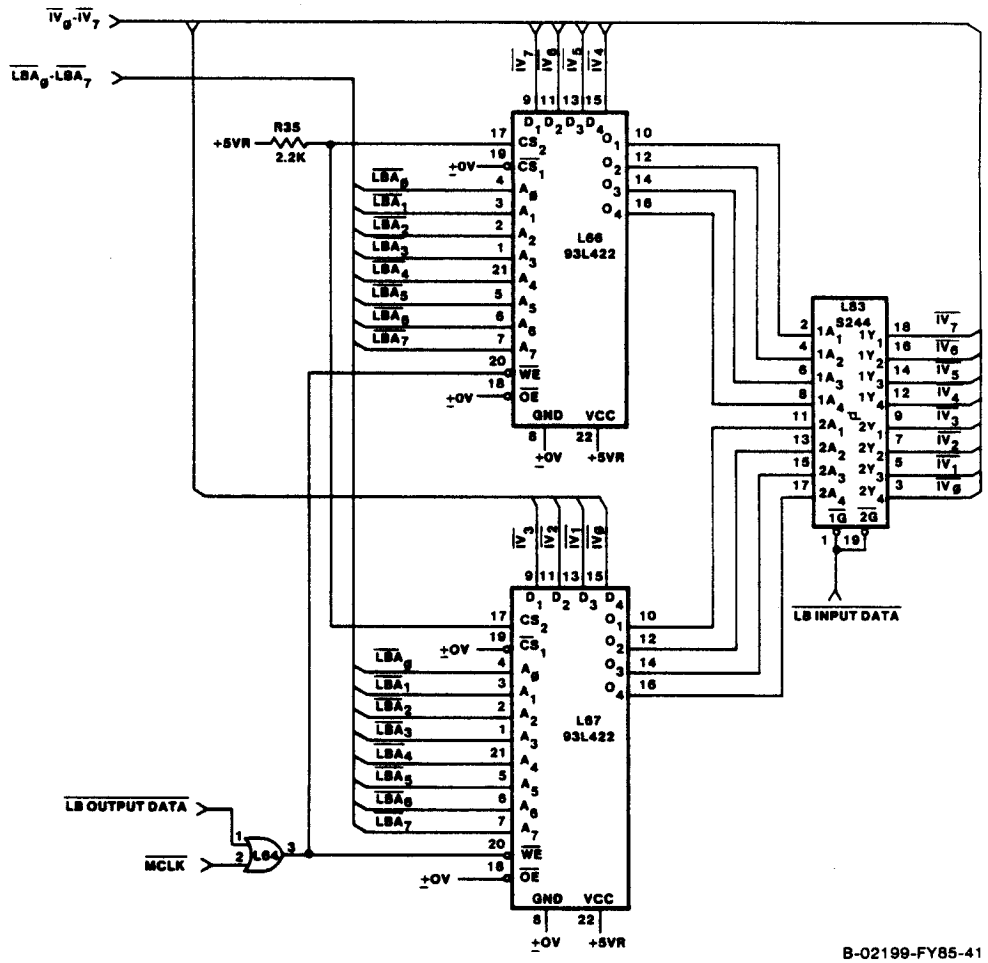

FIGURE 3.2-3
Scratchpad Memory Logic

3.2.4 Right Bank I/O Decoder Operations

The right bank generates I/O port commands which control the primary RCU functions. The right bank controls Status and Parameter Register File access, 4K x 8 Data Buffer access, 50BUS access, Winchester Disk Drive access, the Control Unit Busy interrupt, and reading and clearing the Command Bus Request bit.

The Microcontroller places the addresses of selected right bank ports on the &IV bus via Microcontroller Data Transceiver L69. At the proper time the Microcontroller issues active Right Bank (&RB) and Select Command (&SC) control signals to Control Signal Decoder L38 to select the appropriate right bank port. L38 then issues &RBINPUTDATA from pin 12 and an inverted WC signal from pin 10. The signal from L38 pin 10 drives pin 9 of L26 low, allowing the &MCLK signal to pass through to the output of L26 (pin 10). From L26 pin 10, &MCLK then clocks Right Bank Address Latch L85 to generate right bank addresses &RBA0-7. The bit weights of the &IV bus address on the inputs of L85 are reversed (ie, &IV0, the MSB of the &IV bus, becomes &RBA7, the MSB of the &RBA bus). The &IV address bus is and then issued from L85 as the &RBA address bus. The &RBA0-7 addresses are decoded to create I/O command control signals. There is one primary right bank I/O decoder and seven secondary right bank I/O decoders.

L80, the Right Bank I/O Decoder, decodes addresses &RBA4-6 into seven I/O command groups. Each of these groups enables one of the seven I/O port functions. L80 is always held enabled and, therefore, generates I/O commands when it receives an address on its input pins. Table 3.2-3 lists right bank RCU port addresses, the corresponding command, and the function of that command. In Table 3.2-3 and following tables, "W" indicates that the commands are used for write-only operations, "R" indicates that the commands are used for read-only operations, and "W/R" indicates that the some of the commands in the address range are used for both write and read operations. Each specific right bank command function is broken down in greater detail in Section 3.3

Table 3.2-3: RCU RIGHT BANK I/O DECODER COMMANDS

RCU Port Address (Hex)	I/O Command	Function
00-0B (W)	&STREGFILE	Status Register Functions Strobe. Write status information to the 12-byte Status Register File. Status information is read from the SRF by the RMU.
0C-0F	Not Used	
10-1F (W/R)	&PARREGFILE	Parameter Register File Functions Strobe. Write or read data to or from the 16-byte Parameter Register File. The Parameter Register File passes commands and parameters between the RMU and the RCU.
20 (W/R)	&COMMAND	Command. Write or read the Command Notification (&CMD) bit. The &CMD bit is generated by the RMU to issue a Command Bus Request (&CMDBUSREQ) to the RCU. Writing to 20H clears &CMDBUSREQ. Reading 20H reads the status of the &CMDBUSREQ signal.
21-2F	Not Used	
30-3B (W/R)	&BUFFER	Buffer Memory Functions Strobe. Write or read data to or from the 4K x 8 Data Buffer. The 4K x 8 Data Buffer is used as an interim data storage area during Winchester write or read operations.
34-3F	Not Used	
40-47 (W/R)	&50BUS	50BUS Functions Strobe. Write or read generates 50BUS control signals. These control signals control all 50BUS operations.
48-4F	Not Used	

Table 3.2-3: RCU RIGHT BANK I/O DECODER COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
50-57 (W/R)	&WINCH	Winchester Functions Strobe. Write or read controls Winchester write, read, and format operations.
58-6F	Not Used	
70 (W)	&INTERRUPT	Interrupt Functions Strobe. Write issues the Control Unit Not Busy (&CUBUSY) signal. &CUBUSY notifies the RMU when the Microcontroller has completed an operation.
71-7F	Not Used	

3.3. RIGHT BANK OPERATIONS

The right bank generates I/O port commands, which control the primary RCU functions. The right bank also controls Status and Parameter Register File access, 4K x 8 Data Buffer access, 50BUS access, Winchester disk drive access, issuing the Control Unit Busy interrupt, and reading or clearing the Command Bus Request bit. There is one primary right bank I/O decoder and seven secondary I/O decoders on the right bank, as shown in FIGURE 3.3-1. L80, the Right Bank I/O Decoder, decodes addresses &RBA4-6 into seven I/O functions. Each of the seven functions enables the respective I/O port's command decoder. Table 3.2-3 shows the relationship between the RCU port addresses and the right bank I/O functions. Each specific right bank command function is broken down in greater detail in the following text.

3.3.1 Status Register File Control I/O Commands

When the Microcontroller selects the Status Register File (locations 00-0BH), Right Bank I/O Decoder L80 issues the active Status Register Functions Strobe (&STREGFILE) signal from pin 7. &STREGFILE first is synchronized with &RBODMCLK (&RBODMCLK is the &MCLK signal synchronized with the Right Bank Data Output signal, &RBOUTPUTDATA) at L81. &STREGFILE then enables Status Register File Decoder L79 by asserting L79 pin 1. When enabled, L79 decodes addresses &RBA2-3 into one of three address spaces: Write SRF Bank One, Two, or Three (WB1, WB2, or WB3). Each of these signals asserts enabling pins on two Status Register File chips. The SRF chips must be enabled in pairs since each chip contains half (ie, four bits) of a complete word. Six 4 x 4 Status Register File chips provide twelve SRF bytes. Table 3.3-1 illustrates the relationship of the address bits to the command, and the function of each command.

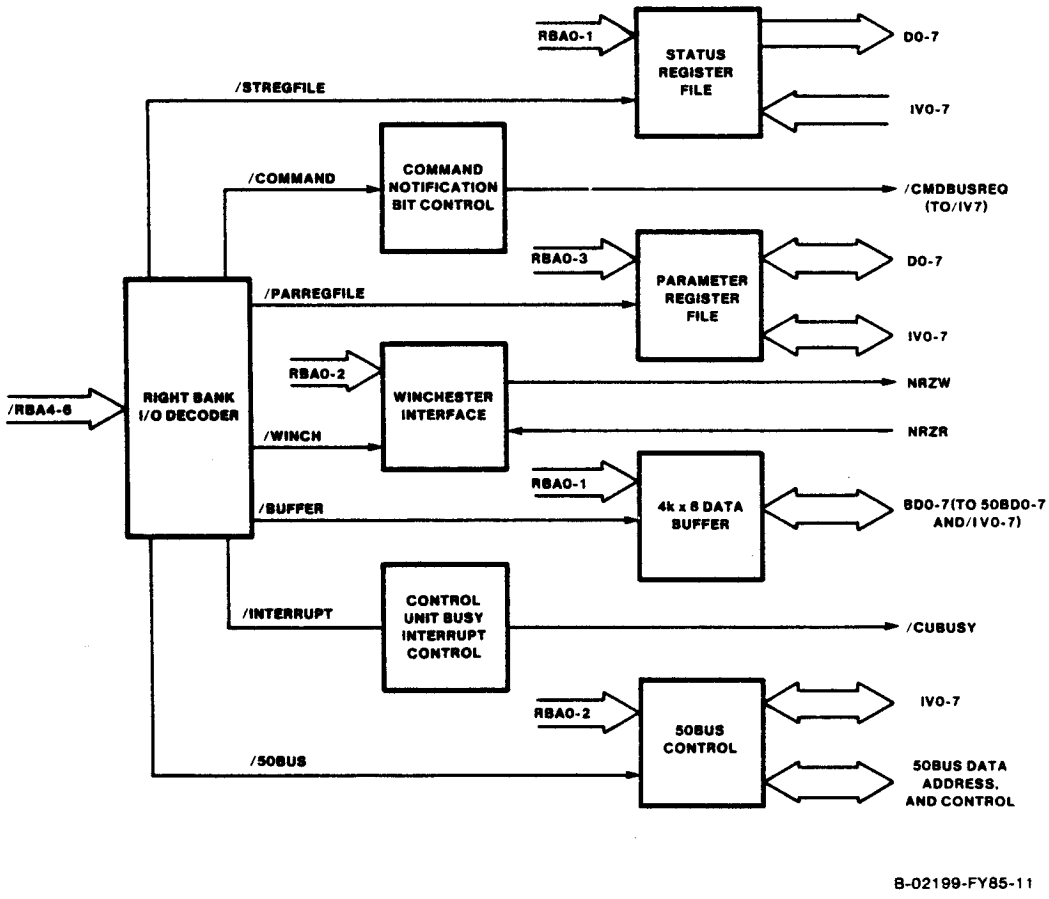

FIGURE 3.3-1
Right Bank Decoding Block Diagram

Table 3.3-1: STATUS REGISTER FILE I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
00-03	WB1 (W)	Write enables data to be written into the L151 and L152 SRF chips.
04-07	WB2 (W)	Write enables data to be written into the L134 and L135 SRF chips.
08-0B	WB3 (W)	Write enables data to be written into the L117 and L118 SRF chips.

3.3.2 Parameter Register File Control I/O Commands

When the Microcontroller writes or reads data to or from the Parameter Register File (locations 10-1FH), Right Bank I/O Decoder L80 issues the Parameter Register File Functions Strobe (&PARREGFILE) signal from pin 9. &PARREGFILE is gated through L97 (pin 5 to pin 6) to assert the select pin of Parameter Register File chips L100 and L101. During PRF write operations, &PARREGFILE asserts L64 pin 9, where it is synchronized with &RBODMCLK on pin 10. The output of L64 is gated through L97 to generate a low signal that instructs the PRF to write data by asserting pin 3 of the PRF chips. During read operations, &RBODMCLK is inactive; therefore, pin 10 of L97 is high. Since the Z80A Write Request (&WR) signal is also inactive, pin 9 of L97 is high, which creates a high signal on the PRF's write pin, placing the PRF in the read direction. At the same time, &PARREGFILE asserts L64 pin 6, allowing the Right Bank Input Data (&RBINPUTDATA) signal to enable PRF Data Output Buffer L84 (via L64 pin 5). PRF read and write operations are explained in detail in Section 3.5. Section 3.5 also provides detailed information about Parameter Register File access.

3.3.3 Command Notification Bit Issuance I/O Command

To clear the Command Notification bit (write port 20H), Right Bank I/O Decoder L80 issues the &COMMAND signal from pin 10. After being synchronized with the active &RBODMCLK signal through L26, &COMMAND asserts the clock pin of Command Bus Request Flipflop L25 as shown in FIGURE 3.3-2. When clocked by the synchronized output from L26 pin 4, L25 deactivates the Command Bus Request (&CMDBUSREQ) signal from pin 8. The inactive &CMDBUSREQ signal is sent to the RMU to release the Z80A from its bus-requested state. The Microcontroller cuts off its access to the PRF by disabling PRF Input Data Buffer L133 with the inactive &CMDBUSREQ signal. At the same time, the inactive CMDBUSREQ signal from L25 pin 9 asserts the select pin of PRF Address Multiplexer L102 to select the Z80A-generated bank address bits (&ZBA0-3) for an impending Z80A-controlled PRF read or write operation.

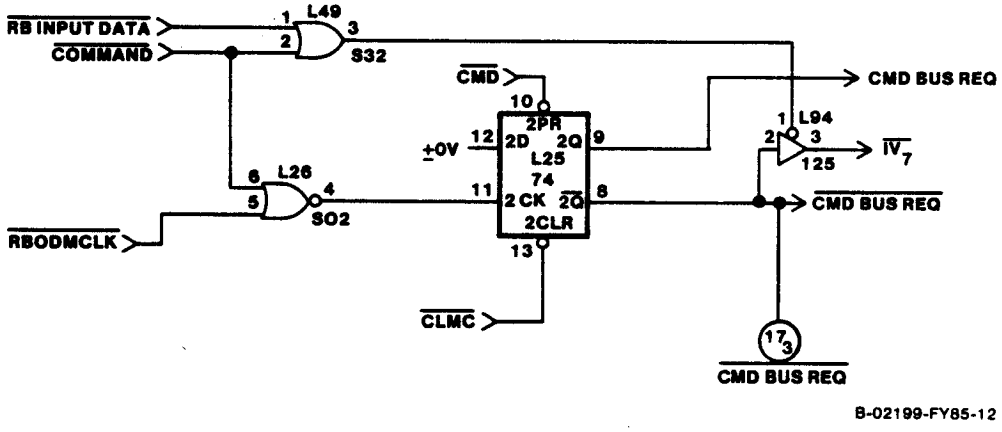

FIGURE 3.3-2
Command Bus Request Bit Control

The Microcontroller reads the status of the CMDBUSREQ signal by reading port 20H. The active &COMMAND signal asserts L94 (via L49), allowing the Microcontroller to read the status of the &CMDBUSREQ signal via the &IV7 bit.

3.3.4 4K x 8 Data Buffer Control I/O Commands

When the Microcontroller commands a 4K x 8 Data Buffer read or write operation (ports 30H-3FH), Right Bank I/O Decoder L80 issues the Buffer Memory Functions Strobe (&BUFFER) signal from pin 11. &BUFFER is synchronized with the active &RBODMCLK signal to generate a low synchronized output from L49 pin 11 which enables 4K x 8 Data Buffer Decoder L77 by asserting pin 1.

When enabled, the 4K x 8 Data Buffer Decoder responds to address bits &RBA0-1 by generating one of four possible I/O commands. Table 3.3-2 shows the relationship of the address bits to the command, and the function of each command. Section 3.4 provides detailed information about 4K x 8 Data Buffer access.

Table 3.3-2: 4K x 8 DATA BUFFER I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
30 (W)	Load Low-Order Address	Write loads low-order address bits from the &IV bus through the 4K x 8 Data Buffer Low-Order Address Counter (L125 and L126) onto Buffer Address Bus bits BA0-7.
31 (W)	Load High-Order Address	Write loads high-order address bits from the &IV bus through the 4K x 8 Data Buffer High-Order Address Counter (L143) onto Buffer Address Bus bits BA8-10. Only four bits are needed; therefore, the low-order nibble (&IV4-7) of the IV bus is used.

Table 3.3-2: 4K x 8 DATA BUFFER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
32 (W)	READ	Write generates the Data Buffer Read (READ) signal which commands a 4K x 8 Data Buffer read operation. Two consecutive writes to port 32H must be performed to read data. The first write turns on the 4K x 8 Data Buffer Read (&BUFFRD) strobe to the Data Buffer, and the second write turns it off (creating a 200-ns duration READ signal).
33 (W)	WRITE	Write generates the Data Buffer Write (WRITE) signal, which commands a 4K x 8 Data Buffer write operation. Two consecutive writes to port 33H must be performed to write data. The first write turns on the 4K x 8 Data Buffer Write (&BUFFWR) strobe to the Data Buffer, and the second write turns it off (creating a 200-ns duration WRITE signal).
34-3F	Not Used	

3.3.5 50BUS Control I/O Commands

When the Microcontroller initiates a 50BUS operation (ports 40-4FH), Right Bank I/O Decoder L80 issues the 50BUS Functions Strobe (&50BUS) signal from pin 12. The &50BUS signal asserts 50BUS Decoders L78 (1G7) and L114 (1F7) (via L81) to enable a 50BUS read or write operation. L78, the 50BUS Read Control Decoder, decodes addresses &RBA0-1 into one of two I/O commands. L114, the 50BUS Write Control Decoder, decodes addresses &RBA0-2 into one of eight 50BUS control commands.

When &RDINPUTDATA is active at L81 pin 9, the &50BUS signal from the Right Bank I/O Decoder is passed through L81 to enable L78, the 50BUS Read Control Decoder. L78 decodes addresses &RBA0-1 into one of two commands. (Table 3.3-3 illustrates the relationship of the address bits to the command, and the function of each command.) When &RBODMCLK is active at L81 pin 12, the &50BUS signal from the Right Bank I/O Decoder is synchronized through L81 to enable L114, the 50BUS Write Control Decoder. L114 decodes addresses &RBA0-2 into one of eight commands. Section 3.4 provides a detailed explanation of the 50BUS Control I/O command functions.

Table 3.3-3: 50BUS I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
40 (R)	&RP40H	Read data from the 50BUS data bus onto the &IV data bus.
40 (W)	&SLAVESLCT	Select a slave on the 50BUS. The relationship of the data on the &IV bus to the device selected is shown below. &IV0-&IV7 — Device Selected 01H — 0 - Master memory 02H — 1 - Serial data link 04H — 2 - FDC DMA 08H — 3 - IWS 10H — 4 - IWS 20H — 5 - IWS 40H — 6 - IWS 80H — 7 - IWISE
41 (R)	Unnamed	Read the status of the 50BUS Acknowledge (&50BBUSAK) and 50BUS DMA Request (&50BDRQ) signals from the 50BUS. If &IV7 (the LSB) is set to 1, &50BBUSAK is active; if &IV6 is set to 1, &50BDRQ is active.

Table 3.3-3: 50BUS I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
41 (W)	&WP41H	Write to load low-order address from the &IV bus onto the 50BUS address bus.
42 (W)	&ADDHIGH	Write to load high-order address from the &IV bus onto the 50BUS address bus.
43 (W)	&WP43H	Write data onto the 50BUS data bus.
44 (W)	&DATA ENABLE	Write selects data path to the 50BUS as follows: IV7 = 1 - Microcontroller data is sent to 50BUS IV6 = 1 - Data from 4K x 8 Data Buffer is sent to the 50BUS
		NOTE: Only one can be selected at a time.
45 (W)	&CNTRL	Write generates both 50BUS Bus Request (&50BBUSREQ) and 50BUS read/write signals as follows: IV1 = 0 - Write operation IV1 = 1 - Read operation IV2 = 0 - Turn off &50BBUSREQ IV2 = 1 - Turn on &50BBUSREQ

Table 3.3-3: 50BUS I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
46 (W)	&SPFUNC	Write generates the following 50BUS signals: Status 50BUS (STATUS50B) IV4 = 1 - Turn on status IV4 = 0 - Turn off status Reset 50BUS Device (RESET50B) IV3 = 1 - Turn on reset IV3 = 0 - Turn off reset Terminal Count (TC) IV5 = 1 - Turn on terminal count IV5 = 0 - Turn off terminal count
47 (W)	&REQ	Write generates the 50BUS Byte Request (&50BREQ) signal.
47-4F	Not Used	

3.3.6 Winchester Control I/O Commands

When the Microcontroller commands a Winchester read or write operation (ports 50-57H), Right Bank I/O Decoder L80 issues the Winchester Functions Strobe (&WINCH) signal from pin 13. &WINCH, after being gated through L35, asserts the Winchester Read and Write Decoders (L78 and L62 (2B4 & 2D4)). During Winchester write operations, the Right Bank Output Data Master Clock (&RBODMCLK) signal is active on L35 pin 12, synchronizing the &WINCH signal through L35 to enable Winchester Write Decoder L62. During Winchester read operations, &RBINPUTDATA is active on L35 pin 5, allowing the &WINCH signal through L35 to enable Winchester Read Decoder L78.

When enabled, Winchester Write Decoder L62 responds to address bits &RBA0-2 by generating one of eight possible I/O write commands. Winchester Read Decoder L78, when enabled, responds to address bits &RBA0-1 by generating one of three possible I/O read commands. (Table 3.3-4 illustrates the relationship of the address bits to the command, and the general function of each command.) Chapter 6 provides a detailed explanation of the Winchester I/O command functions.

Table 3.3-4: WINCHESTER I/O COMMANDS

RCU Port Address (Hex)	I/O Command	Function
50 (R)	&READDSKDATA	Read a byte of data from the Winchester.
50 (W)	&DSKWRITEDATA	Write a byte of data to the Winchester.
51 (R)	&READDSKSTATUS	Read the Winchester status byte. IV7 = 1 - Track 0 has been detected. IV6 = 1 - A write fault has been detected. IV5 = 1 - The Winchester is ready to perform an operation. IV4 = 1 - A command seek operation has been completed. IV3 = 1 - The Winchester has been selected for an operation. IV2 - Unused IV1 - Unused IV0 = 1 - An index mark has been detected (ie, located at the beginning of a track).

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
51 (W)	&WRITEDRPRG	Program the Winchester. Write a control byte to the Winchester and controller. IV7 = 1 - Select a write operation. IV6 = 1 - Select a read operation. IV5 = 1 - Select reduced write current for write precompensation. IV4 = 1 - Select the direction of head movement. IV3 = 1 - Select the drive for a read, write, or seek operation. IV2 - 1 - Select head 2 for read or write operation. IV1 = 1 - Select head 1 for read or write operation. IV0 = 1 - Select head 0 for read or write operation.

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
52 (R)	&READCNTRLSTATUS	Read Winchester controller status. IV7-IV4 - Four switched bits that define Winchester characteristics. IV3 = 1 - Parallel to Serial Converter L141 has sent a byte of data to the Winchester and requires another byte for serialization. IV2 = 1 - Serial to Parallel Converter L107 has assembled a byte of data and requires the host to accept the data byte. IV1 = 1 - The minimum amount of zeros (8 bytes) needed prior to address mark detection has been encountered. IV0 = 1 - An address mark has been detected. The header or data field should follow.

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
52 (W)	&WRITELOGICCNTRL	Write Winchester control signals. IV7, IV2, IV1 - Unused. IV6 = 1 - Enable ECC time. IV5 = 1 - Generate reset. IV4 = 1 - Enable skip (for address mark generation). IV3 = 1 - Enable write gate. IV0 = 1 - Enable write precompensation.
53 (W)	&WRITELOTSC	Write the low-order track step counter with eight bits (&IV7-&IV0).
54 (W)	&WRITEHOTSC	Write the high-order track step counter with four bits (&IV7-&IV4).
55 (W)	&LOADDSKWD	Write to clear byte request from Winchester controller (data irrelevant).
56 (W)	&WP56H	Write to enable or disable the Microcontroller Halt circuit.
57 (W)	Unnamed	Enable or disable data movement. IV7 = 1 - Enable data from 4K x 8 Data Buffer to the Winchester.

Table 3.3-4: WINCHESTER I/O COMMANDS (cont.)

RCU Port Address (Hex)	I/O Command	Function
		IV7 = 0 - Disable data from 4K x 8 Data Buffer to the Winchester. IV6 = 1 - Enable Winchester data to 4K x 8 Data Buffer. IV6 = 0 - Disable Winchester data to 4K x 8 Data Buffer. IV5 = 1 - Enable 50BUS data to 4K x 8 Data Buffer. IV5 = 0 - Disable 50BUS data to 4K x 8 Data Buffer.
58-5F	Not Used	

3.3.7 Interrupt Issuance I/O Command

When the Microcontroller issues an interrupt (port 70H), Right Bank I/O Decoder L80 issues the Interrupt Functions Strobe (&INTERRUPT) signal from pin 15. &INTERRUPT, together with the active &RBODMCLK signal (&RBODMCLK is the &MCLK signal synchronized with the &RBOUTPUTDATA signal), asserts L35 (2E5). Together these signals generate a low output from L35 pin 8 which, via L65, fires Control Unit Not Busy 1-Shot L34 by asserting pin 11. L34's firing issues the Control Unit Not Busy (&CUBUSY) pulse to inform the RMU that the RCU has completed an operation and is no longer busy. When the Microcontroller is hung in a Winchester read or write operation (see Section 3.5.7), a signal from the carry pin of the Dead Man Timer can also assert L34 via L65 to generate the &CUBUSY signal. When interrupted, the Z80A performs interrupt service routines which determine the cause of the active &CUBUSY signal by examining various status bits in the Status Register File.

3.4 4K x 8 DATA BUFFER and 50BUS INTERFACE

3.4.1 4K x 8 Data Buffer

The 4K x 8 Data Buffer on the RCU board serves as a temporary storage area for data passing between the RCU and the Winchester or floppy disk drive (see FIGURE 3.4-1). Two 2K x 8 Static RAM chips (L110 and L109 (1H7 & 1J7)) comprise the 4K x 8 Data Buffer (as shown in FIGURE 3.4-2). Therefore, if data moves between one slave's memory and another slave's memory, the data passes through the 4K x 8 Data Buffer. In addition, if data moves between the RCU and any slave, the data passes through the 4K x 8 Data Buffer.

Addresses are provided to the 4K x 8 Data Buffer by the 4K x 8 Data Buffer Address Counters (L125, L126, and L143 (1H/K8)). The Microcontroller generates the initial address and sends it to the data buffer via the &IV bus. The 11-bit address is then sent into the 4K x 8 Data Buffer via the BA0-10 address bus when the address counter load pins are asserted by signals from the 4K x 8 Data Buffer Decoder (L77). The address is then incremented by either an active &BUFFRD or &BUFFWR signal issued via the L76 flipflops.

Data moves to and from the 4K x 8 Data Buffer via the BD0-7 data bus. Data is moved between the BD0-7 bus and the 50BD0-7 (50BUS Data) bus through the 50BD0-7 to BD0-7 Bus Data Buffer (L127) and the BD0-7 to 50BD0-7 Bus Data Latch (L28). Data moves between the BD0-7 bus and the Winchester via the BD0-7 to WBD0-7 Bus Data Latch (L142) and the Winchester to BD0-7 Bus Data Buffer (L108).

The 4K x 8 Data Buffer Bank Select Flipflop (L93, 1Q output) selects and synchronizes (with the Master Clock, MCLK) the bank select signal which chooses either L109 or L110 for the 4K x 8 Data Buffer read or write operation. The &IV4 signal is forwarded through L143 to the input of L93 to specify L93's output. L109 is selected for the read or write operation if L93 generates an active signal from pin 6 (ie, input &IV4 is inactive). L110 is selected for the read or write operation if L93 generates an active signal from pin 5 (ie, input &IV4 is active).

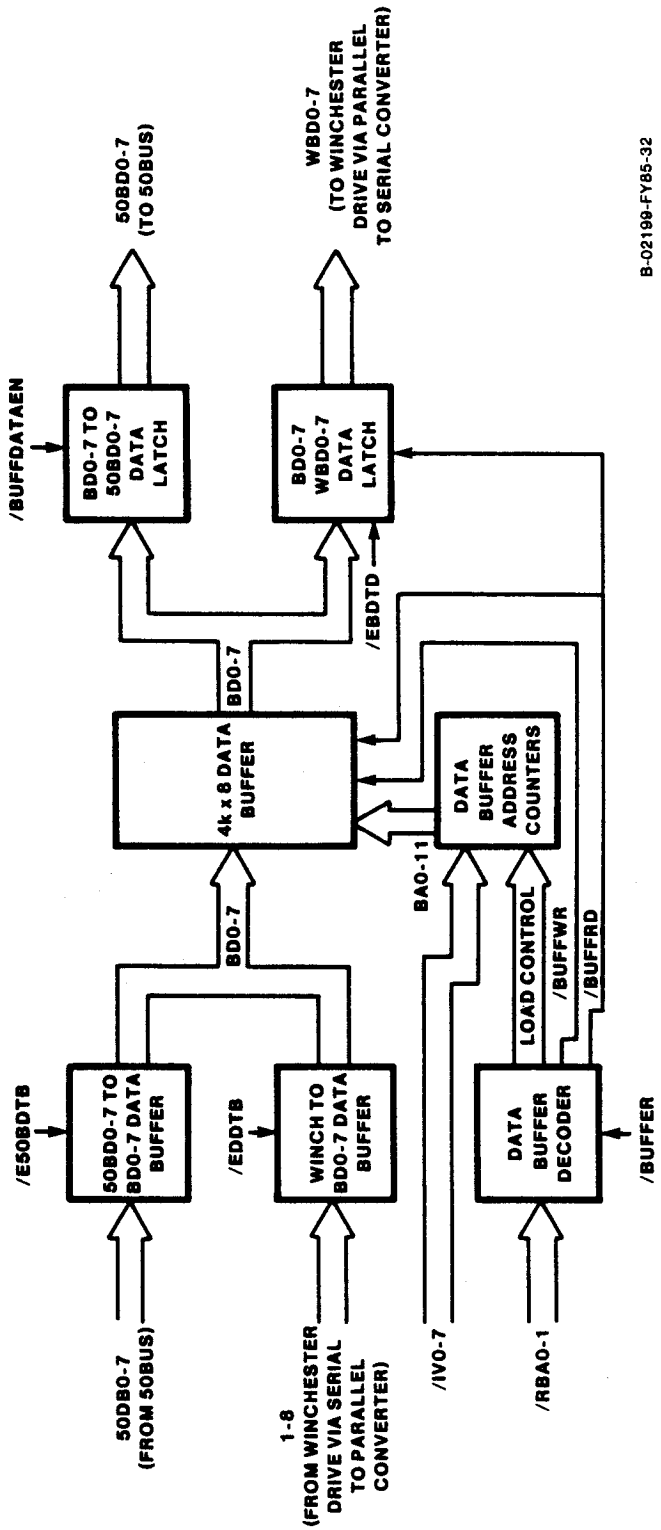

FIGURE 3.4-1
4K x 8 Data Buffer Block Diagram

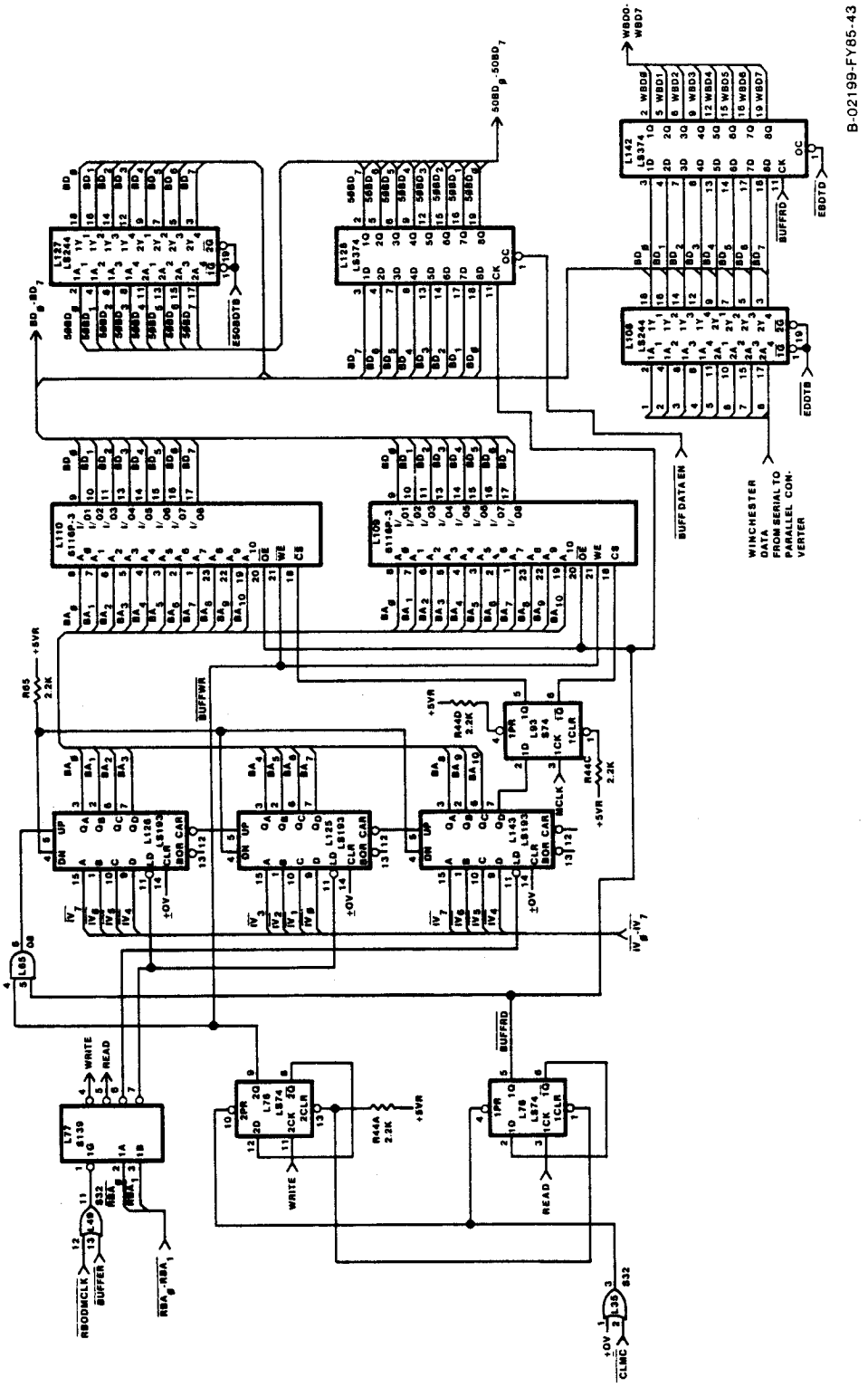

FIGURE 3.4-2
4K x 8 Data Buffer Access Logic

3.4.2 Data Buffer I/O Command Functions

When the Microcontroller commands a 4K x 8 Data Buffer read or write operation (ie, it issues 30-3BH), Right Bank I/O Decoder L80 issues the Buffer Memory Functions Strobe (&BUFFER) signal from pin 11. &BUFFER is synchronized with the active &RBODMCLK (Right Bank Output Data Synchronized with Master Clock) signal to generate a low synchronized output from L49 pin 11 which enables 4K x 8 Data Buffer Decoder L77 by asserting pin 1. When enabled, L77 responds to address bits &RBA0-1 by generating one of four possible I/O commands (see Table 3.3-2).

In response to the 30H write command, 4K x 8 Data Buffer Decoder L77 issues a signal from pin 7 which asserts the load pins of 4K x 8 Data Buffer Low-Order Address Counters L125 and L126 to pass the initial address from the &IV bus onto the &BA0-7 bus outputs. The address counters are incremented to provide additional addresses by the active 4K x 8 Data Buffer Read (&BUFFRD) or 4K x 8 Data Buffer Write (&BUFFWR) signal asserting L126 pin 5 via L65. &BUFFWR and &BUFFRD are latched versions of the active Data Buffer Write (&WRITE) and Data Buffer Read (&READ) signals issued from L77 pins 4 and 5.

In response to the 31H write command, L77 issues a signal from pin 6 that asserts the load pin of 4K x 8 Data Buffer High-Order Address Counter L143 to pass the initial address from the &IV bus onto the &BA8-10 bus outputs. The High-Order Address Counter is incremented to provide additional addresses when the carry signal from Low-Order Address Counter L125 asserts pin 5 of L143.

In response to the 32H write command, 4K x 8 Data Buffer Decoder L77 issues a signal from pin 5 that initiates a data buffer read operation. The Microcontroller actually generates the read strobe to the data buffer by writing to port 32H. Two consecutive port 32H writes are issued to perform a read operation: the first turns the Read signal on, and the second turns it off. This procedure results in an active &BUFFRD strobe of 200-ns duration (200-ns is the lenght of one instruction cycle for the 8X305 Microcontroller). The Read signal from L77 generates the &BUFFRD signal directly through Data Buffer Read Control Flipflop L76 (2H3). READ asserts L76's clock input to latch the &BUFFRD signal active from pin 5. &BUFFRD is turned off 200 ns later when the READ signal is activated again on the clock input of L76.

When activated, &BUFFRD asserts the output enable pins of 4K x 8 Data Buffer chips L109 and L110 to move a byte of data out of the buffer and onto the BD0-7 data bus. For each byte read, &BUFFRD asserts the Data Buffer Address Counter's up-count pin (via L65) to increment the BA0-10 address bits sent to the data buffer. &BUFFRD asserts the clock pins of 4K x 8 data output chips L128 and L142 to clock data off of the BD0-7 data bus and onto either the 50BD0-7 or WBD0-7 data bus (depending on which bus is enabled).

In response to the 33H write command, 4K x 8 Data Buffer Decoder L77 issues the Write signal from pin 4 to initiate a data buffer write operation. The Microcontroller actually generates the write strobe to the data buffer by writing to port 33H. Two consecutive 33H writes are issued to perform the write operation: the first turns the Write signal on, and the second turns it off. This procedure results in an active &BUFFWR strobe (generated by L76 pin 9) of 200-ns duration. The Write signal from L77 generates the &BUFFWR signal directly through Data Buffer Write Control Flipflop L76. WRITE asserts L76's clock input to latch the &BUFFWR signal active from pin 9. &BUFFWR is turned off 200 ns later when the Write signal is activated again on the clock input of L76.

When activated, &BUFFWR asserts the write enable pins of 4K x 8 Data Buffer chips L109 and L110 to write a byte of data into the buffer from the BD0-7 data bus. For each byte written, &BUFFWR asserts the Data Buffer Address Counter's up-count pin (via L65) to increment the BA0-10 address bits sent to the data buffer.

3.4.3 50BUS Interface

The 50BUS is an internal bus which connects all internal and external devices of the OIS 50 system (see FIGURE 3.4-3). The RCU interface to the 50BUS consist of 40 signals generated in four distinct groups. The first group is the 50BUS address bus (50BA0-15), which is generated via 50BUS Address Bus Buffer/Counters L143A, L147, and L148. The second group is the 50BUS data bus (50BD0-7), which is received by the RCU via the 50BD0-7 to &IV0-7 Bus Data Buffer (L129) and transmitted through the &IV0-7 to 50BD0-7 Bus Data Latch (L145). The 4K x 8 Data Buffer receives data from the 50BUS data bus through the 50BD0-7 to BD0-7 Bus Data Buffer (L127) and transmits data to the 50BUS through the BD0-7 to 50BD0-7 Bus Data Latch (L128).

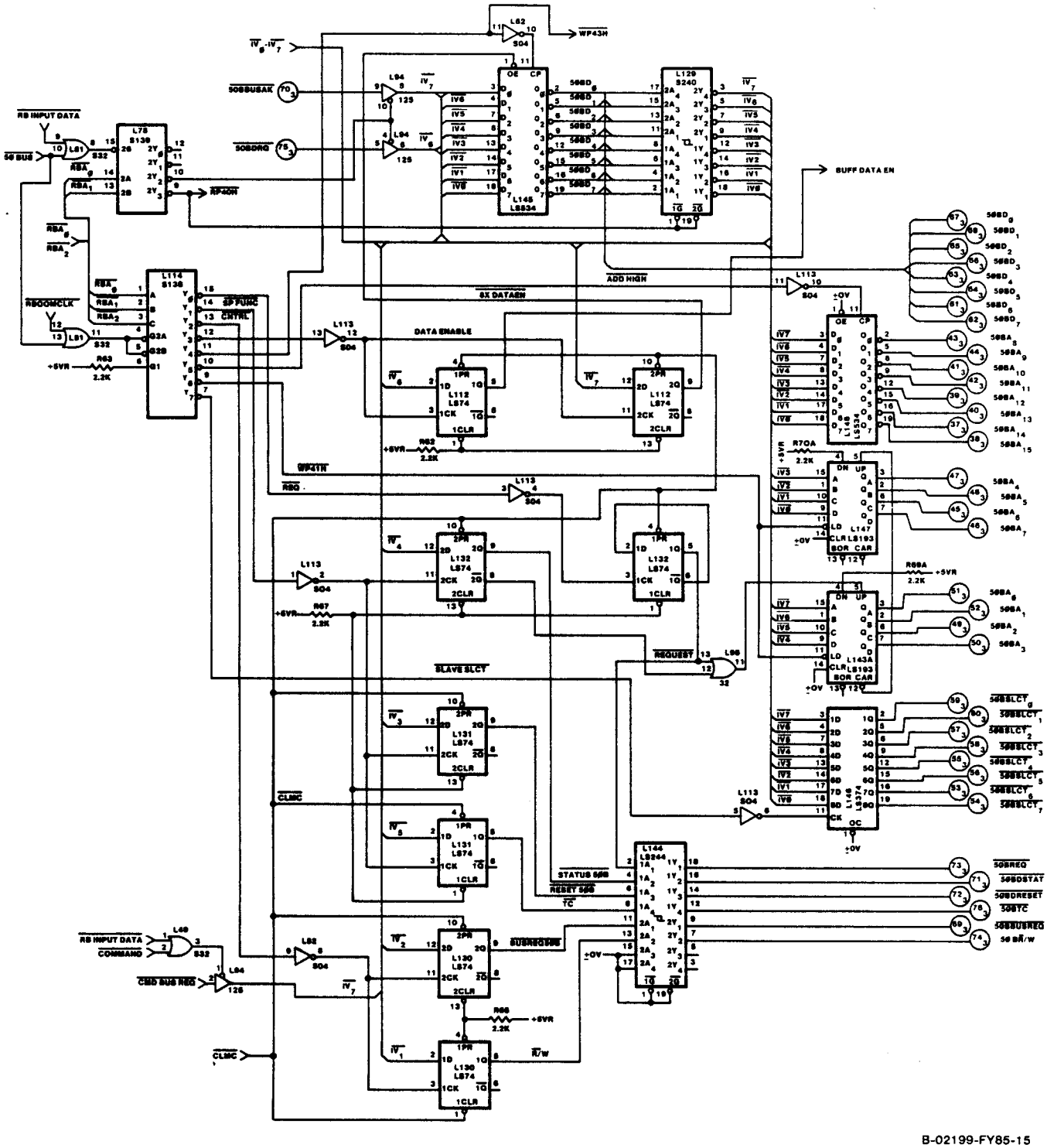

FIGURE 3.4-3
50BUS Control Logic.

The third group contains eight 50BUS select signals (&50BSLCT0-7), which select a device to use the 50BUS for communication. The fourth group consists of eight control signals, six of which are RCU-generated via 50BUS Control Signal Buffer L144. Two control signals, 50BUS Byte Request (&50BREQ) and 50BUS Bus Acknowledge (&50BBUSAK), are generated by the RMU or system devices. &50BREQ is generated by the floppy disk drive to indicate that the 50BUS is transferring a byte to or from the 4K x 8 Data Buffer. &50BBUSAK is generated by the RMU or an internal slave when relinquishing bus control after receiving a 50BUS Bus Request (&50BBUSREQ) signal.

3.4.4 50BUS I/O Command Functions

When the Microcontroller commands a 50BUS operation (ports 40-47H), Right Bank I/O Decoder L80 issues the 50BUS Functions Strobe (&50BUS) signal from pin 12. The active &50BUS signal is first gated through L81; it then asserts either the L78 or L114 (1F7) 50BUS Decoder to enable a 50BUS read or write operation. When the Right Bank Input Data (&RBINPUTDATA) signal is active at L81 pin 9, the &50BUS signal from the Right Bank I/O Decoder is passed through L81 to enable 50BUS Read Control Decoder L78. When &RBODMCLK is active on L81 pin 12, the &50BUS signal from the Right Bank I/O Decoder is passed through L81 to enable the 50BUS Write Control Decoder, L114.

When enabled, 50BUS Read Control Decoder L78 decodes addresses &RBA0-1 to generate one of two 50BUS read commands. 50BUS Write Control Decoder L114, when enabled, decodes addresses &RBA0-2 into one of eight 50BUS write commands. (Table 3.3-3 lists the 50BUS control I/O commands, which are explained in detail in the following text.)

When a Read 50BUS Data command (port 40H) is issued, L78 issues the Read 50BUS Data (&RP40H) signal from pin 9. &RP40H asserts pins 1 and 19 of L129, the 50BD0-7 to &IV0-7 Bus Data Buffer, to move data from the 50BUS onto the IV bus. &RP40H also asserts (via L63) the clock pin on Halt Generator Flipflop L61 to generate the &HALT signal to halt Microcontroller operations. It is necessary to halt the Microcontroller when performing Winchester or Serial Data Link operations to allow the two asynchronous devices (eg, the Microcontroller and the Winchester or the Microcontroller and the Serial Data Link) to be synchronized.

In response to the Slave Select write command (port 40H), L114 issues the Slave Select (&SLAVE SLCT) signal from pin 7. &SLAVE SLCT is first inverted; it then asserts the clock pin of 50BUS Device Select Latch L146. L146, when clocked by &SLAVE SLCT, generates a device select signal (from &50BSLCT0-7) corresponding to the code it receives from the &IV bus.

When the Read 50BUS Status read command (port 41H) is generated, L78 issues a signal from pin 10 that enables the 50BUS DMA Request (&50BDRQ) and 50BUS Bus Acknowledge (&50BBUSAK) signals to be gated onto the &IV bus (bits &IV6 and &IV7, respectively). &50BDRQ is activated by the floppy disk drive when the drive has a byte of data ready to be transferred either to or from buffer memory. &50BBUSAK is activated when a selected slave has surrendered bus control in response to receiving a &50BBUSREQ signal.

The 50BUS Address Low write command (port 41H) causes L114 to issues the Write 50BUS Addresses (&WP41H) signal from pin 9 to place a low-order address byte on the 50BUS address bus (50BA0-7). &WP41H asserts the load pins of 50BUS Low-Order Address Counters L143A and L147 to move the address from the IV bus onto the 50BUS address bus. The counters input address from the &IV bus is inverted in L143A and L147 prior to being placed on the 50BUS. The initial 50BUS address is incremented by each active 50BUS Request (&REQUEST) signal that asserts the up-count pin of L143A (via L96). (The &REQUEST signal and, therefore, the 50BUS Byte Request (&50BREQ) signal are issued once for each byte transferred via the 50BUS.) The active Status Register File Read (STATUS) signal is used at L96 pin 12 to prevent the &REQUEST signal from incrementing the address counters in operations that do not require the address to be incremented (eg, in Serial Data Link operations).

The generation of the 50BUS Address High write command (port 42H) causes L114 to issues the Address High Order (&ADD HIGH) signal from pin 10 to place a high-order address byte on the 50BUS address bus (50BA0-15). &ADD HIGH asserts pin 11 of 50BUS High Address Latch L148 to place the high-order address from the &IV bus onto the 50 BUS address bus. The address from the &IV bus is inverted through L148 prior to being placed on the 50BUS.

In response to the &IV Bus to 50BUS Clock write command (port 43H), L114 issues the Write 50BUS Data (&WP43H) signal from pin 11 to move data from the &IV bus to the 50BUS data bus. By asserting the clock pin of L145, &WP43H moves data from &IV0-7 onto 50BD0-7. L145's output enable pin is asserted by a low signal from the &IV Bus to 50BUS Data Control Flipflop (L112, gate 2Q). L112 generates the 8X305 Data Enable (&8XDATAEN) output enabling signal from pin 9 when clocked by the &DATA ENABLE signal (port 44H command issued) as &IV7 is active on its D input. &WP43H also asserts (via L63) the clock pin of Halt Generator Flipflop L61 to generate the &HALT signal which stops Microcontroller operations (if enabled) for data synchronization purposes. It is necessary to halt the Microcontroller when performing Winchester or Serial Data Link operations to allow the two asynchronous devices (eg, the Microcontroller and the Winchester or the Microcontroller and the Serial Data Link) to be synchronized.

When the &IV Bus or &BD (4K x 8 Data Buffer) Bus to 50BUS Enable write command (port 44H) is issued, L114 issues the &DATA ENABLE signal from pin 12 to enable data from the &IV bus or the &BD0-7 bus onto the 50BUS data bus. To prevent bus contention problems, only one path should be selected at a time. If DATA ENABLE clocks L112 (gate 1Q) while &IV6 is active, L112 generates the Buffer Data Enable (&BUFFDATAEN) signal which asserts the output enable pin of the BD0-7 to 50BD0-7 Bus Data Latch (L128). If DATA ENABLE clocks L112 (gate 2Q) while &IV7 is active, L112 generates the &8XDATAEN signal which asserts the output enable pin of the &IV0-7 to 50BD0-7 Bus Data Latch (L145). The Data Enable Control Flipflops (L112) are cleared, as are most of the 50BUS control flipflops, by the active Controller Master Clear (&CLMC) signal asserting their preset pins.

In response to the 50BUS Control write command (port 45H), L114 issues, from pin 13, the 50BUS Control (&CNTRL) signal which is inverted to clock the 50BUS Control Signal Generating Flipflops (L130, gates 1Q and 2Q). If CNTRL clocks L130 (gate 1Q) while &IV1 is active, L130 generates a low Read/Write (&R/W) signal which passes through L144 to generate the low 50BUS Read or Write (50B&R/W) signal which commands a read operation. If &IV1 is high, L144 commands a write operation (due to the high 50B&R/W signal from L130). If CNTRL clocks L130 (gate 2Q) while &IV2 is active, L130 generates the active 50BUS Bus Request (&BUSREQ50B) signal. &BUSREQ50B passes through L144 to generate the active 50BUS Bus Request (&50BBUSREQ) signal which requests control of a selected device's bus. If &IV2 is inactive (ie, high), &50BBUSREQ is not activated from L144 (due to the inactive &BUSREQ50B signal from L130).

When the 50BUS Special Function write command (port 46H) is generated, L144 issues the Special Function (&SPFUNC) signal from pin 14. &SPFUNC is inverted to clock 50BUS Special Function Flipflops L131 (gates 1Q and 2Q) and L132 (gate 2Q only). If SPFUNC clocks L131 (gate 1Q) while &IV5 is active, L131 generates the active Terminal Count (&TC) signal. &TC passes through L144 to generate the active 50BUS Terminal Count (&50BTC) signal needed to command the terminal count associated with a floppy disk drive operation. If &IV5 is high, &50BTC is turned off in response to an inactive &TC signal from L131. If SPFUNC clocks L131 (gate 2Q) while &IV3 is active, L131 generates the active Reset 50BUS Device (&RESET50B) signal. &RESET50B passes through L144 to generate the active 50BUS Device Reset (&50BDRESET) signal used to reset a selected device on the 50BUS. If &IV3 is high, &50BDRESET is deactivated in response to an inactive &RESET50B signal from L131.

If SPFUNC clocks L132 (gate 2Q) while &IV4 is active, L132 generates the active Status 50BUS (&STATUS50B) signal from pin 9. &STATUS50B passes through L144 to generate the active 50BUS Device Status (&50BDSTAT) signal to request the selected 50BUS device's status. If &IV4 is high, &50BDSTAT is deactivated in response to an inactive &STATUS50B signal from L132. When clocked with &IV4 active, L132 (gate 2Q) issues the Status Register File Read (STATUS) signal from pin 8. During operations involving the Serial Data Link, STATUS is activated at L96 pin 12 to prevent an active 50BUS Request (&REQUEST) signal from incrementing the 50BUS Low-Order Address Counters. STATUS50B performs this function because it is available for use when the counters are not required to increment (ie, after a 50BUS Byte Request, &50BREQ, signal is issued). When STATUS50B prevents the counters from incrementing, its activation does not affect the responses from devices on the 50BUS since they are not selected.

In response to the 50BUS Request write command (port 47H), L114 issues the Request (&REQ) signal from pin 15. &REQ is inverted to clock the 50BUS Request Signal Generating Flipflop (L132, gate 1Q). When clocked, L132 generates the 50BUS Request (&REQUEST) signal from pin 5. &REQUEST passes through L144 to generate the active 50BUS Byte Request (&50BREQ) signal. &REQUEST and, therefore, &50BREQ are issued once for each byte transferred via the 50BUS, or for transmissions or receptions via the RMU board's Serial Data Link logic. The pulse width of the &50BREQ signal varies (under Microcontroller firmware control) according to the type of operation being performed. The active &REQUEST signal also asserts the 50BUS Address Bus Counters to provide an incrementing pulse and, therefore, a new address for each word sent on the 50BUS data bus. The REQUEST signal from pin 6 of L132 is fed back into the D input of L132 to clear the active &REQUEST signal when the next &REQ signal is issued by L144.

3.4.5 Interfacing to a Parallel Device on the 50BUS

Requesting a parallel device restart is similar to requesting a serial device restart. The selected parallel device resets itself upon receiving the leading edge of the 50BUS Device Reset (&50BDRESET) signal (as shown in FIGURE 3.4-4). Holding &50BDRESET active for 6 us provides enough time for the Z80A to ensure that an M1 cycle occurs during the activated &50BDRESET signal.

Requesting parallel device status is similar to requesting serial device status. The selected parallel device loads an 8-bit status byte onto the 50BUS data bus (50BD0-2) upon receiving an active 50BUS Device Status (&50BDSTAT) signal (as shown in FIGURE 3.4-5). When &50BDSTAT is deactivated, the selected device removes its status information from the 50BUS data bus. Prior to issuing a status request to a device the RCU performs a handshaking procedure (displayed in FIGURE 3.4-6).

Requesting parallel device memory access is similar to requesting serial device 1-byte and 256-byte memory access. The RCU first issues a bus request to the selected device by activating the 50BUS Bus Request (&50BBUSREQ) signal (see FIGURE 3.4-7). The RCU waits up to 10 us for the device to return the active 50BUS Bus Acknowledge (&50BBUSAK) handshaking signal. If &50BBUSAK is not received within 10 us, the operation is terminated and a No-Data Time-out is posted to the operating system. If &50BBUSAK is activated within 10 us, the RCU places addresses (&50BA0-15), data (50BD0-7), and the read/write control signal (50BR/W) on the 50BUS and then activates the &50BREQ signal. Upon receiving the active &50BREQ signal, the selected device performs the read or write operation (specified by the state of 50BR/W) using the address and data residing on the 50BUS.

During memory read and write operations the selected parallel device initiates its memory access operations upon receiving the leading edge of the active &50BREQ signal. Data, addresses, and read/write control signals on the 50BUS are held stable when &50BREQ is active. During a memory read operation, data is valid and stable on the 50BUS after 600 ns. Data can be read by the selected device following the 600-ns stabilization period, and can still be read from the 50BUS after &50BREQ is deactivated (see FIGURE 3.4-7). During a memory write operation, &50BREQ is active for 600 ns, during which time data is written into memory by the selected device. From 1-256 bytes can be read or written in this fashion. Individual 1-byte or 256-byte read/write operations are not performed as in Serial Data Link memory access operations. Since the 4K x 8 Data Buffer has a capacity of 4K bytes, up to a 4K-byte memory read/write operation is possible (but not implemented due to operating system limitations).

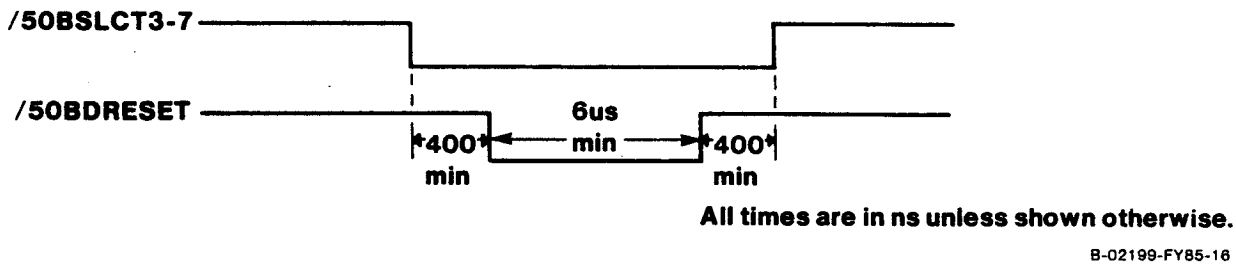

FIGURE 3.4-4
Parallel Device Restart Timing Diagram.

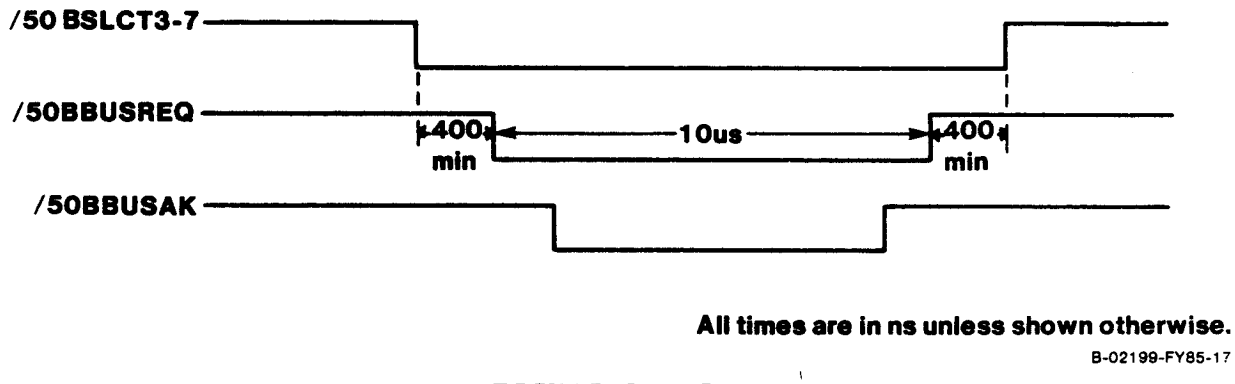

FIGURE 3.4-5
Parallel Device Status Timing Diagram.

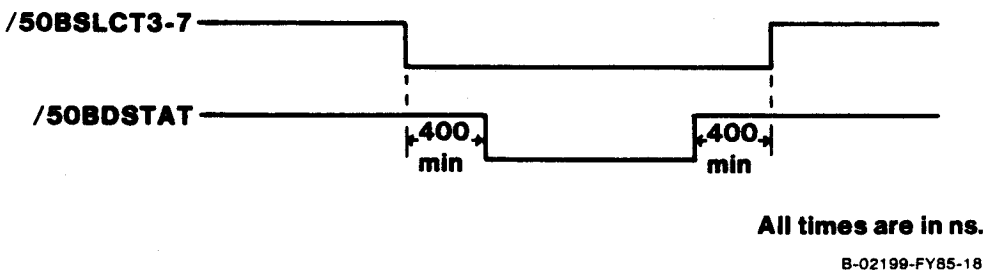

FIGURE 3.4-6
50BUS Handshaking Timing Diagram

Although devices 3-7 are selected in FIGURE 3.4-7, parallel device memory read/write operations also involve reading from and writing to master memory (device 0). Parallel device restart and status operations cannot be performed with master memory. Master memory can be accessed only by implementing 256-byte data transfers; 1-byte operations can not be performed.

FIGURE 3.4-7 (the parallel device memory access operation timing diagram) displays only one &50BREQ signal, indicating that only one byte is being transferred. To perform 256-byte data transfers, &50BSLCT, &50BBUSREQ, and &50BUSAK remain active while &50BREQ is strobed for each of the 256 data bytes (each data byte's corresponding address is provided). FIGURE 3.4-8 shows the pulse width and repetition rate of &50BREQ during various operations. Internal Wang Inter-system Exchange (IWISE) read and write operations use unique timing (due to the nature of the memory arbitration scheme). The RCU determines which timing to use by reading the device select code. Any board residing in the IWISE slot (possibly an Internal Printer Controller, or IPC, board) receives the &50BREQ signal in the IWISE pattern as shown in FIGURE 3.4-8.

3.4.6 Microcontroller Halt Circuit

The Microcontroller Halt Generating Circuit generates an active &HALT signal to temporarily stop Microcontroller operation. &HALT is sampled by the Microcontroller's internal logic at the end of the first internal quarter of each instruction cycle. If the &HALT signal is active when sampled, a halt is immediately executed and the current instruction is terminated. The MCLK signal is not inhibited during a halt operation. The Microcontroller is intentionally halted to synchronize asynchronous operations that occur during data transfers between the Microcontroller and the Winchester or the Serial Data Link.

In response to the Enable Halt Circuit write command (port 56H), Winchester Write Decoder L62 issues the Clock Halt Circuit (&WP56H) signal from pin 14. &WP56H clocks the Halt Enabling Flipflop (L61, 1Q output). Clocking L61 places a low signal on the pin 12 input of L61 (2Q output). This procedure enables L61 (2Q output) to generate the &HALT signal when clocked by either an active Write 50BUS Data (&WP43H) or Read 50BUS Data (&RP40H) signal (via L63), or a combination of active 4K x 8 Data Buffer Read (&BUFFRD) and Winchester Write Gate (&WTG) signals (via L49 and L63).

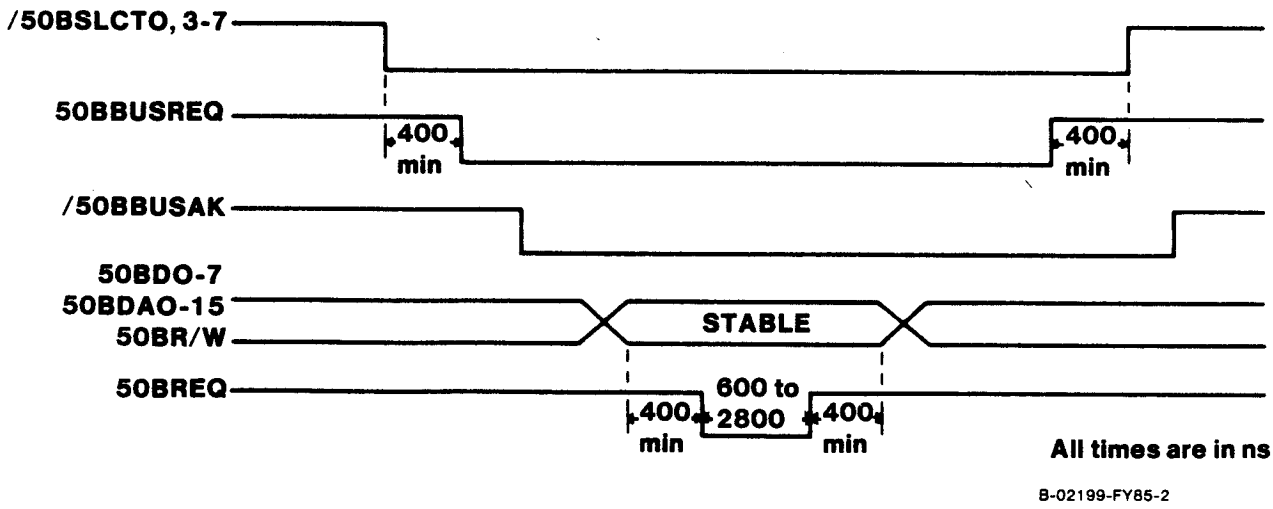

FIGURE 3.4-7
Parallel Device Memory Access Timing Diagram.

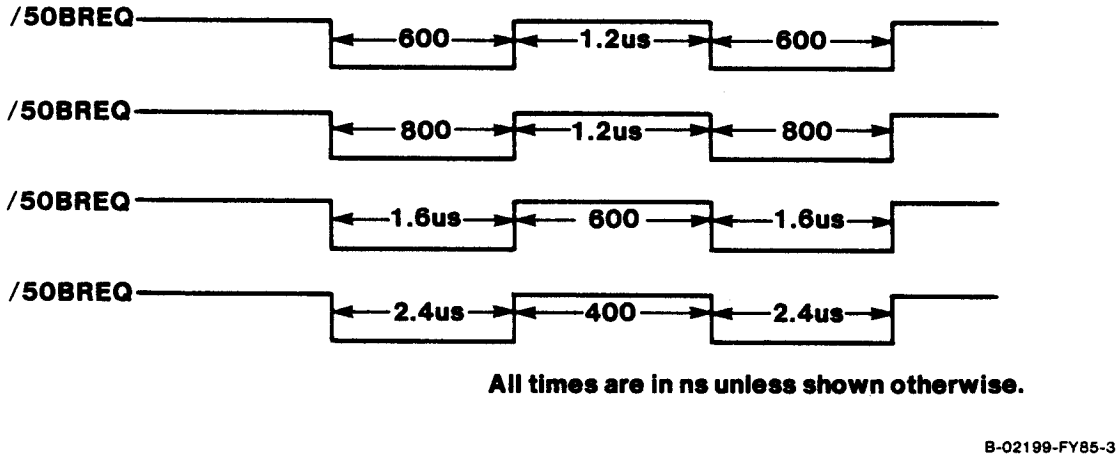

FIGURE 3.4-8
Block Read/Write 50BUS Request Timing Diagram.

&WP43H generates a &HALT signal to synchronize the Microcontroller during all Serial Data Link read and write operations (byte or block writes). &RP40H halts the Microcontroller during all Winchester read operations (ID or data field). The combination of the active &BUFFRD and &WTG signals generates a Halt signal when data is being written to the Winchester (including formatting operations). &HALT can be generated by any of the above signals or signal combinations only when L61 (1Q output) has been clocked by the write to port 56H command (activated &WP56H).

Presetting the L61 Halt Flipflops clears the &HALT signal. The flipflops are preset when the active Byte Done Read (&BDONER), Byte Done Written (&BDONEW), Clear Halt (&CLHALT), or Controller Master Clear (&CLMC) signal asserts the flipflops' preset pins. When a new byte is received from the Winchester during a read operation, &BDONER clears the Halt signal; when a new byte is requested to be transmitted during a Winchester write operation, &BDONEW clears the halt circuit. &CLHALT is generated by the RMU board when the Serial Data Link requires a byte for transmission to, or has received a byte from, a serial device. &CLMC is asserted at L86 to clear the &HALT signal during the power-on sequence.

3.5. WINCHESTER DISK DRIVE INTERFACE

The Winchester disk drive is a 10M-byte drive (30M-byte for the OIS 60) with data formatted on four recording surfaces into 304 cylinders; each cylinder uses four heads and four tracks. Each track contains 32 sectors, and each sector contains 256 bytes of data. The Winchester disk drive device type is read by the Microcontroller via the 4-bit SW1 Winchester Disk Drive Device Type Switches. The SW1 switches are set to 3H for the 10M-byte Winchester device used in OIS 40 and OIS 50 applications. Winchester device status is read from SW1 onto &IV4-7 (IV7 is the least significant bit) via Drive Device Type Buffer L122 when the Read Control Status (&READCNTLSTATUS) signal activates L122's enabling pin. The ST506 Winchester Disk Drive Interface is used in OIS 40 and OIS 50 applications.

3.5.1 Winchester I/O Command Functions

When the Microcontroller commands a Winchester disk drive operation (ie, it issues port 50-5FH), Right Bank I/O Decoder L80 issues the Winchester Functions Strobe (&WINCH) signal from pin 13. The active &WINCH signal is gated through L35 to assert either of the Winchester Decoders (L62 or L78, see FIGURE 3.5-1) in order to enable either a Winchester read or write operation. When the Right Bank Input Data (&RBINPUTDATA) signal is active at L35 pin 5, the &WINCH signal from the Right Bank I/O Decoder is passed through L35 to enable the Winchester Read Decoder, L78. When the &RBODMCLK (Right Bank Output Data synchronized with Master Clock) signal is active at L35 pin 12, the &WINCH signal from the Right Bank I/O Decoder is passed through L35 to enable the Winchester Write Decoder (L62).

When enabled, Winchester Read Decoder L78 decodes addresses &RBA0-1 to generate one of three Winchester read commands; Winchester Write Decoder L62, when enabled, decodes addresses &RBA0-2 to generate one of eight Winchester write commands. Table 3.3-4 lists the Winchester I/O commands (which are explained in detail in the following text).

In response to the Read Disk Data read command (50H), L78 issues the Read Disk Data (&READDSKDATA) signal to enable a byte of data through the Winchester to &IV0-7 Bus Data Buffer (L123, see FIGURE 3.5-2) and to clear the Byte Done Read (BDONER) signal from the Serial to Parallel Converter (L107). The active &READDSKDATA signal asserts 1-Shot L33 (via L3) to generate an active low signal from L33 pin 9. This low signal asserts the &BCLR pin of the Serial to Parallel Converter to clear the BDONER signal in preparation for the next byte.

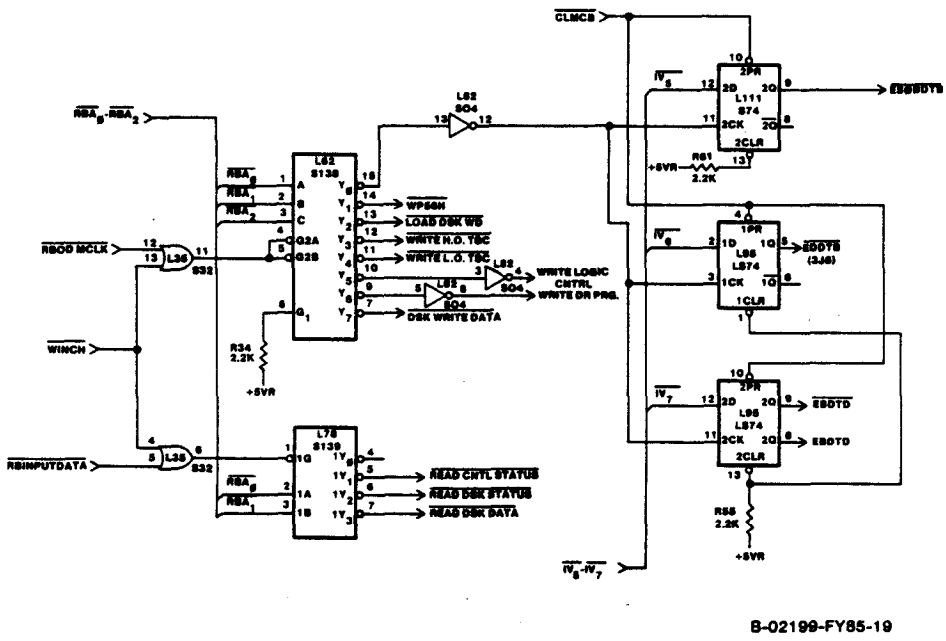

FIGURE 3.5-1
Winchester Interface Control Logic.

In response to the Disk Write Data write command (50H), L62 issues the Disk Write Data (&DSKWRITEDATA) signal, which clocks the &IV0-7 to WBD0-7 Bus Data Buffer (L124, see FIGURE 3.5-2). When L24 (which is enabled by the Enable Data Buffer to Winchester, EBDTD, signal) is clocked, inverted data is moved from the &IV0-7 bus onto the WBD0-7 bus. Data passed to the Winchester from the IV bus usually consists of the information that proceeds and follows the data field in the data format package (see Section 3.5.2).

In response to the Read Disk Status read command (51H), L78 issues the Read Disk Status (&READDSKSTATUS) signal to enable the Winchester Status Signal Buffer (L121). Enabling L121 allows the Microcontroller to read the condition of status signals received directly from the Winchester. Table 3.5-1 illustrates the relationship of the &IV0-7 inputs to the status signals and defines the meaning of each status signal.

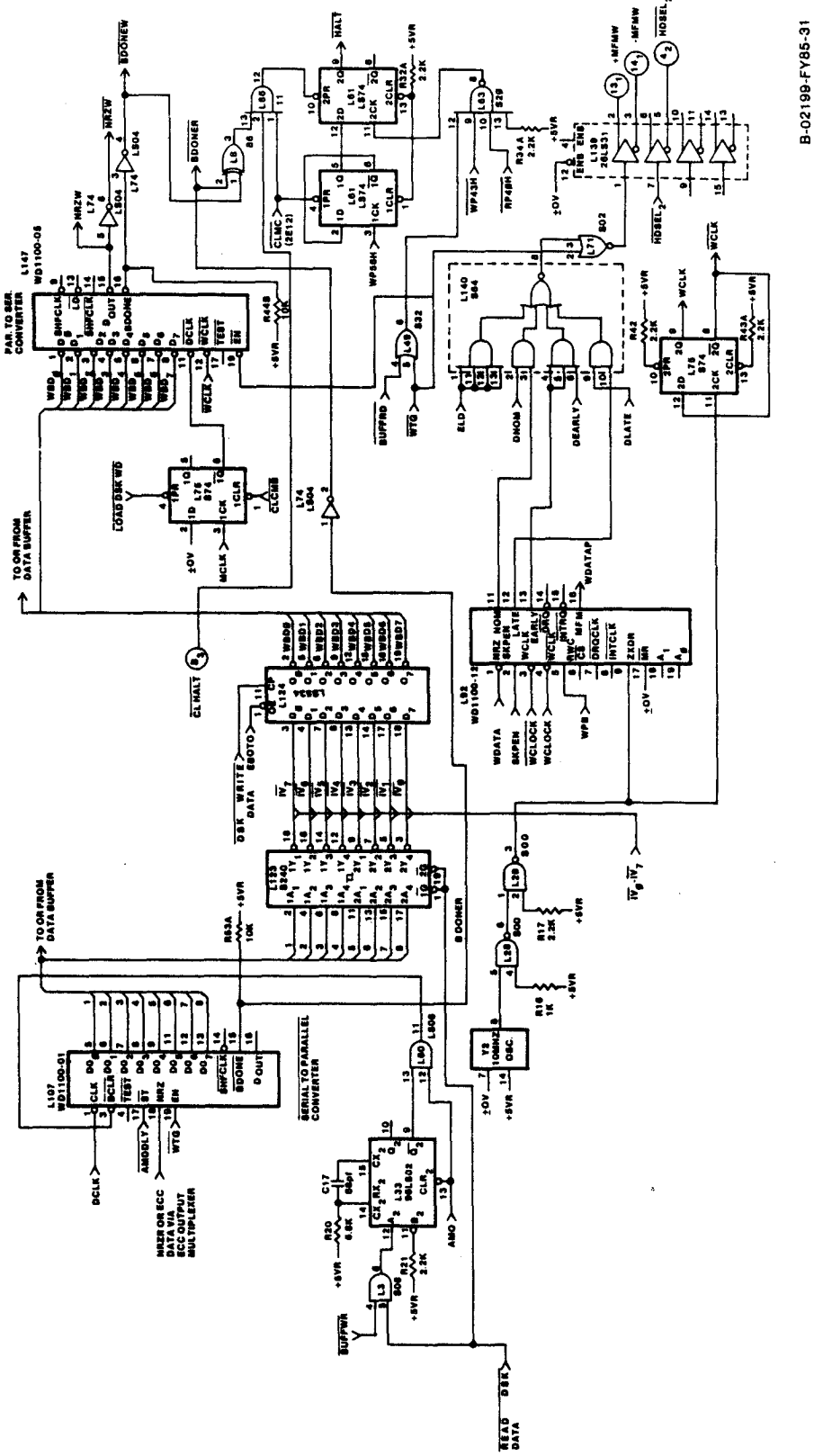

FIGURE 3.5-2
Winchester Interface Logic.

Table 3.5-1: WINCHESTER STATUS BYTE

Bit	Status Signal	Definition
&IV7	&TRACK0	Track 0. Track 0 has been detected. Disk heads are positioned over cylinder 0's outermost data track.
&IV6	&WRITEFAULT	Write Fault. A write fault has been detected. A condition exists that has caused improper writing on the disk. Further writing and stepping is inhibited until the fault is corrected.
&IV5	&READY	Ready. Active &READY in conjunction with active &SEEKCOMPLETE indicates that the Winchester is ready to perform a read, write, or seek operation.
&IV4	&SEEKCOMPLETE	Seek Complete. The commanded seek operation is complete. Indicates that the heads have settled on the destination track.
&IV3	&DRS	Drive Selected. The Winchester has been selected for an operation.
&IV2-&IV1	Unused	
&IV0	&INDEX	Index. An index mark has been detected. (An index mark is located at the beginning of each track.)

In response to the Write Drive Program Signals write command (51H), L62 issues the Write Drive Program Byte (&WRITEDRPRG) signal, which is inverted to clock the Winchester Program Signal Generator (L136). Clocking L136 generates Winchester signals corresponding to the commands received from the IV bus inputs. Table 3.5-2 illustrates the relationship of bits IV0-7 to the program command issued, and the function of each command.

Table 3.5-2: WINCHESTER PROGRAM BYTE

Bit	Command Issued	Function
IV7	DWRITE	Disk Write. Specifies a Winchester write operation.
IV6	DREAD	Disk Read. Specifies a Winchester read operation.
IV5	RWC	Reduce Write Current. Specifies reduced write current for write precompensation purposes within the Winchester.
IV4	DIRECTION	Direction. Specifies the direction of head movement in a seek operation.
IV3	DRVSEL	Drive Selected. Selects the Winchester for a read, write, or seek operation.
IV2	HDSEL2	Head Select 2. Specifies head 2 for read or write operations (not used on the 10M-byte drive).
IV1	HDSEL1	Head Select 1. Specifies head 1 for read or write operation.
IV0	HDSEL0	Head Select 0. Specifies head 0 for read or write operation.

In response to the Read Control Status read command (52H), L78 issues &READCNTLSTATUS to enable Winchester Control Status Signal Buffer L122. Enabling L122 allows the Microcontroller to read the Winchester control status signals and the condition of the SW1 Winchester Device Type Switches. Table 3.5-3 illustrates the relationship of bits &IV0-7 to the control status signals, and defines each status signal.

Table 3.5-3: WINCHESTER CONTROL STATUS BYTE

Bit	Status Signal	Definition
IV7-IV4	Device Type	Defines characteristics and capacity of the Winchester being used.
IV3	&BDONEW	Byte Done Write. The Parallel to Serial Converter has issued a byte of data to the Winchester and, therefore, is prepared to accept another byte for conversion.
IV2	&BDONER	Byte Done Read. The Serial to Parallel Converter has accepted and converted a byte of data from the Winchester and, therefore, is prepared to accept another byte for conversion.
IV1	MINCOUNT	Mincount. The minimum amount of zeros (8 bytes) has been detected in the data stream received from the Winchester. MINCOUNT detection is mandatory before attempts are made to detect the address mark on the disk.
IV0	&AMD	Address Mark Detect. An address mark has been detected in the data stream received from the Winchester. Address mark detection indicates that the ID or data field will follow.

In response to the Write Logic Control Signals write command (52H), L62 issues the Write Logic Control (&WRITELOGICCNTRL) signal. &WRITELOGICCNTRL is inverted to clock Winchester Interface Control Signal Generator L119. When clocked, L119 generates Winchester control signals that correspond to commands received from the IV bus. Table 3.5-4 illustrates the relationship of bits IV0-7 to the program command issued, and the function of each command.

All Winchester interface control signals must be deactivated upon power on. Upon power up, the Buffered Controller Master Clear (&CLMCB) signal is activated to assert the clear pins of Winchester Interface Control Signal Generator L119. The active &CLMCB signal ensures that all signals from L119 are off after the power-up sequence. To provide the Winchester interface with the high IV0-7 signals needed to activate the Winchester control signals, the low-active &IV0-7 bus must be inverted. L120, the IV Bus Inverter, provides the inverted signals needed to turn L119's signals on following a power-up clear operation.

Table 3.5-4: WINCHESTER INTERFACE CONTROL BYTE

Bit	Command Issued	Function
IV7	Unused	
IV6	ECCTIME	ECC Time. Specifies the time at which Control Multiplexer L47 is switched so that the multiplexer can move ECC information rather than data into the read or write data stream.
IV5	SRESET	Software Reset. Specifies a software-commanded reset of the Data Recovery Circuit. SRESET normally is issued after every successful read operation and when certain errors are detected.
IV4	SKPEN	Skip Enable. Enables the creation of the address mark by commanding the MFM Generator to skip the clock pulse needed to create an address mark during format or write operations.
IV3	WTG	Write Gate. Enables the Winchester write circuit so that it can perform a write operation.
IV2-IV1	Unused	
IV0	WPB	Write Precompensation Bit. Enables the MFM Generator to generate write precompensation control signals.

In response to the Write Low-Order Track Step Counter write command (53H), L62 issues the Write Low Order Track Step Counter (&WRITELOTSC) signal which loads Low-Order Track Step Counters L104 and L105 with an initial count from bits IV0-7. The count is decremented as the STEP signal asserts L105's down-count pin. L105 asserts its borrow signal to L104, and L104 asserts its borrow signal to L106 to create a cascaded step counter capable of decrementing from a bit count of 4096 (12 bit).

In response to the Write High-Order Track Step Counter write command (54H), L62 issues the Write High-Order Track Step Counter (&WRITEHOTSC) signal which loads High-Order Track Step Counter L106 with an initial count from bits IV4-7. The High-Order Step Counter is decremented by a borrow signal from L104 asserting the counter's down-count pin. Additional information about the Winchester step logic is contained in Section 3.5.6.

In response to the Load Disk Drive Write Data write command (55H), L62 issues the Load Disk Write Data (&LOADDSKWD) signal. &LOADDSKWD is synchronized (via L75) with the Master Clock (MCLK) to clock Parallel to Serial Converter L141. Clocking L141 loads the data from the WBD0-7 bus into the converter and resets the Byte Done Written (BDONEW) signal. The converter serializes incoming data into the NRZW signal that is issued from L141 pin 15.

In response to the Enable Halt Circuit write command (56H), L62 issues the Clock Halt Circuit (&WP56H) signal, which clocks pin 3 of Halt Enabling Flipflop L61. Clocking L61 places a low signal on the D input (pin 12) of L61, enabling generation of the Halt Microcontroller (HALT) signal when a clock occurs on L61's clock input (pin 11). L61 (pin 9) generates the active &HALT signal when clocked by an active Write 50BUS Data (&WP43H) or Read 50BUS Data (&RP40H) signal (via L63), or when clocked by a combination of active 4K x 8 Data Buffer Read (&BUFFRD) and Winchester Write Gate (&WTG) signals (via L49 and L63). The active &HALT signal places the Microcontroller in a halt state (see Section 3.4.6).

In response to the Enable/Disable Data Movement write command (57H), L62 issues an unnamed signal which clocks the L95 (1Q and 2Q outputs) and L111 (2Q output) Data Control Flipflops. Clocking these flipflops can generate data movement control signal depending on the state of the &IV5-7 inputs. Table 3.5-5 illustrates the relationship of bits IV5-7 to the data movement control signals issued, and the function of each signal.

Table 3.5-5: WINCHESTER DATA MOTION CONTROL BITS

Bit	Command Issued	Function
IV7	&EBDTD	Enable Buffer Data To Disk. Enables BD0-7 to WBD0-7 Bus Data Latch L142 and &IV0-7 to WBD0-7 Bus Data Buffer L124 (the buffers are not enabled simultaneously, but alternately).
IV6	&EDDTB	Enable Disk Data To Buffer. Enables Winchester to BD0-7 Bus Data Buffer L108.
IV5	&E50BDTB	Enable 50BUS Data To Buffer. Enables 50BD0-7 to BD0-7 Bus Data Buffer L127.

3.5.2 Winchester Data Format

The Winchester's track data format is specified by the Microcontroller via the 4K x 8 Data Buffer. When the Microcontroller organizes the Winchester data format (as shown in FIGURE 3.5-3), it does so by creating an image of the desired format in the 4K x 8 Data Buffer and then writing pieces of the image to the Winchester in the necessary quantities. All of the formatting information written to the Winchester originates in the 4K x 8 Data Buffer.

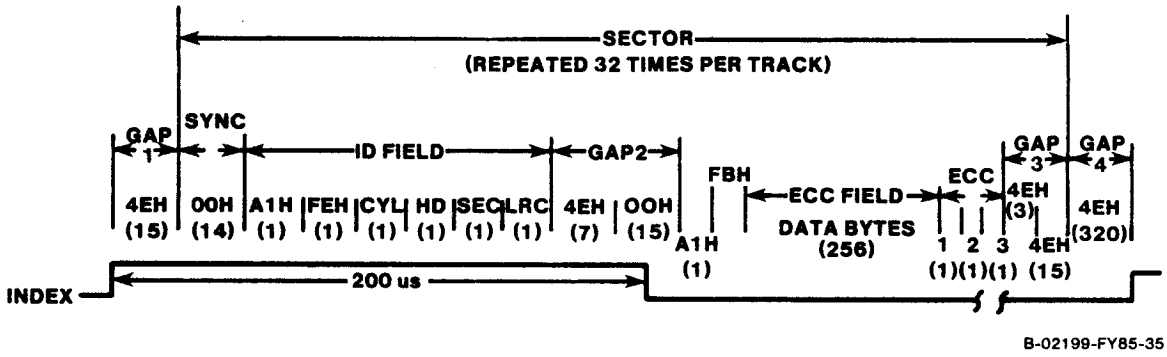

FIGURE 3.5-3
Winchester Disk Data Format.

The Winchester disk is formatted one track at a time. There are 304 cylinders, with four tracks per cylinder, providing a total of 1216 available tracks. Each track contains 32 sectors, each of which contains 256 bytes of data (a total of 8K bytes of data per track). The rising edge of the Winchester-generated INDEX signal marks the location of the beginning of each track. When the Microcontroller detects the leading edge of INDEX, it begins formatting the first sector by writing fifteen 4EH bytes (Gap 1) to act as a write splice area. The first sector physically begins following Gap 1 as the Microcontroller directs 14 bytes of zeros prior to the sector's ID field.

Fourteen bytes of zeros are needed prior to any address mark to set up the hardware which detects the address mark. The hardware looks for an address mark only if 8 bytes of zeros have been detected (Mincount). If 16 bytes of zeros (Maxcount) are detected before an address mark is found, the hardware resets to begin a new zero count. Maxcount is often generated when a data field of zeros is encountered.

An address mark always precedes the ID field and the data field of each sector. The address mark is a unique mark, recognized by the hardware as an A1H byte with a clock bit missing from the MFM data stream. The Microcontroller specifies whether an ID field or a data field will follow the address mark by directing either an FEH (ID field) or FBH (data field) byte after the Address Mark byte. If an FEH byte follows the address mark, an ID field has been detected. If an FBH byte is detected after the address mark, a data field will follow.

Following Gap 1 and 14 bytes of zeros the Microcontroller directs an address mark followed by the FEH byte (to specify the following field as an ID field). The ID field contains the address mark (A1H), the ID field identifier (FEH), three bytes that specify a physical location on the disk (by cylinder, head, and sector), and a Longitudinal Redundancy Check (LRC) byte. The Cylinder (CYL) byte identifies the cylinder that the heads are located above during the read or write operation, and the Head (HD) byte specifies the surface selected. Since there are 304 cylinders, the high-order two bits of the Head byte to help define the cylinder location. The Sector (SEC) byte defines the sector that the heads are above during the read or write operation. The Longitudinal Redundancy Check (LRC) byte is a checksum of the CYL, HD, and SEC bytes used to verify the integrity of the ID field.

The ID field is followed by Gap 2, which contains seven bytes of 4EH (a write splice area needed when the write gate is turned on during write operations), and another 14 bytes of zeros (to set up the Mincount needed for address mark detection). The data field is identified by the address mark and the FBH byte which precede it. During a formatting operation the data field is filled with 256 bytes of zeros followed by the three corresponding Error Check and Correct (ECC) bytes. The data field and the ECC bytes have previously been loaded into the 4K x 8 Data Buffer by the Microcontroller for use in formatting. In a typical write operation the ECC bytes are generated by the ECC Circuitry after the circuitry has examined the data that is being written into the data field.

Gap 3, which follows the ECC bytes, contains three 4EH bytes (a write splice buffer needed when the write gate is turned off during write operations). Gap 3 contains 15 4EH bytes to complete the formatted sector. Formatting continues until all 32 sectors of the track have been formatted. Three hundred twenty 4EH bytes comprise Gap 4, which is written following the last (32nd) sector. Gap 4 compensates for variations in Winchester spindle speed. The rising edge of the INDEX signal terminates formatting of the track.

3.5.3 Winchester Write Operation

Data from the Microcontroller or the 4K x 8 Data Buffer can be written to the Winchester disk drive via the circuitry on the RCU board (see FIGURE 3.5-2 and 3.5-4). All the information sent to the Winchester during a write operation is generated by the Microcontroller (except for the 256-byte data field and the three ECC bytes). Information from the Microcontroller passes through the &IV0-7 to WBD0-7 Bus Data Buffer (L124) and onto the Winchester data bus (WBD0-7). Data field information from the data buffer passes through the BD0-7 to WBD0-7 Bus Data Latch (L142). Section 3.5.1 provides information concerning the generation of the control signals needed to move data through L124 and L142.

Double-buffered Parallel to Serial Converter L141 accepts a new byte of data to be serialized while serializing a second byte held internally. The converter generates the &BDONEW signal from pin 16 when it is prepared to accept another byte of data. Data from the write data bus (WBD0-7) is clocked into L141 by a signal generated by L75 (this signal also deactivates the &BDONEW signal). L75 pin 6 generates the parallel data loading signal when clocked by the MCLK signal after being preset by an active Load Disk Write Data (&LOADDSKWD) signal. The Parallel to Serial Converter utilizes the 5-MHz Write Clock (&WCLK) signal to shift data into a serial NRZW data stream to be issued from pin 15.

To create the WDATA data stream, &NRZW data from the Parallel to Serial Converter is passed through Control Multiplexer L47 (pin 13) when L47's select pin 1 is high. NRZW data is also sent to Control Multiplexer L19 where it is passed onto the ECC Circuit as the Page Data (PGDATA) signal (see Section 3.5.5). All data is examined at the ECC Generator in order to generate three ECC bytes which are placed at the end of the data packet (via pin 14 of Control Multiplexer L47). After all the NRZW data is sent through pin 13 to pin 12 (where it is output as the WDATA signal), L47's select pin is driven low by the Write ECC (&WECC) signal (via L65), allowing three ECC bytes to follow the data (from pin 14 to pin 12).

Data, in the form of the WDATA signal, is sent to MFM Generator L92. The MFM Generator has three functions: converting NRZW data to MFM data, generating write precompensation control signals, and stripping the clock bit from the A1H address mark byte. The Write Data Precompensation (WDATAP) signal is the MFM-encoded result of the WDATA input to the MFM Generator. The MFM Generator creates the early, nominal, and late write precompensation control signals when its write precompensation pin is enabled by the Write Precompensation Bit (WPB) control signal from the Winchester Interface Control Signal Generator (L119).

The WDATAP signal is sent to the Write Precompensation Logic (L90 and L138) to generate the Data Early (DEARLY), Data Nominal (DNOMINAL), Data Late (DLATE), or Extra Late Data (ELD) signals. The ELD signal is used at L140 to prevent a splice condition. One of three MFM-encoded data signals from L138 is gated through L140 and sent to the Winchester (via L139) when any of the early, nominal, or late control signals from L92 is activated. If write precompensation is not selected (ie, WPB is inactive) L92's nominal signal is activated. MFM-encoded data from the RCU is written onto the Winchester under control of the Microcontroller-generated right bank I/O commands.

3.5.4 Winchester Read Operation

MFM-encoded data from the Winchester disk drive is accepted onto the RCU board through MFM Data Receiver L89 when L89 is enabled by the active Drive Select (&DRS) signal. The incoming data stream is sent to the Phase Locked Loop Circuitry, where it is synchronized to a predefined center frequency clock (see Section 3.5.8). Data is passed from the Phase Locked Loop Circuit into the Data Recovery Circuit, where the data and clock pulses are separated (see Section 3.5.9). The Data Recovery Circuit's NRZR data output is sent to Address Mark Detector L29, Control Multiplexer L19, and Control Multiplexer L47. The separated clock signal is generated as the Data Clock (DCLK) signal from pin 12 of the Address Mark Detector. FIGURE 3.5-5 is a block diagram of the data routes during a Winchester read operation, and FIGURE 3.5-2 shows the Winchester Interface Circuit.

After being enabled when the MINCOUNT signal (8 bytes of zeros, see Section 3.5.2) is detected, the Address Mark Detector monitors the NRZR data stream for the A1H address mark. When the address mark is detected the Address Mark Detector generates the Address Mark Detect (AMD) signal, which is delayed by L5 to create the AMD Delayed (AMDDLY) signal. AMDDLY enables the ECC Checker Circuit at the proper time by releasing the clear on the ECC Read Control Shift Register.

The activated ECC Checker Circuit examines the data and the three ECC bytes to verify that all information has been read without error (see Section 3.5.5). Control Multiplexer L47 passes the NRZR data stream, followed by three ECC Syndrome bytes from the ECC Checker, from pin 4 into the Serial to Parallel Converter (L107). If data has been transferred correctly the ECC Syndrome bytes, which are checked by the Microcontroller, will contain all zeros.

L107 converts serial data to parallel form using the separated DCLK signal from the Address Mark Detector (via Control Multiplexer L47) as the shift clock. When properly enabled (write gate off, WTG inactive on pin 3), parallel data from L107 is passed onto an outgoing data bus. The Parallel to Serial Converter generates the active Byte Done Read (BDONER) signal from pin 15 when it has accepted and converted a byte of data from the Winchester and is preparing to accept another byte for conversion. When the next byte of data is read from the Winchester, L33 generates a signal to clear the BDONER signal by asserting L107 pin 3. L33 generates a signal that clears BDONER upon receipt of the necessary control signals (active &BUFFWR or &READDSKDATA, and AMD).

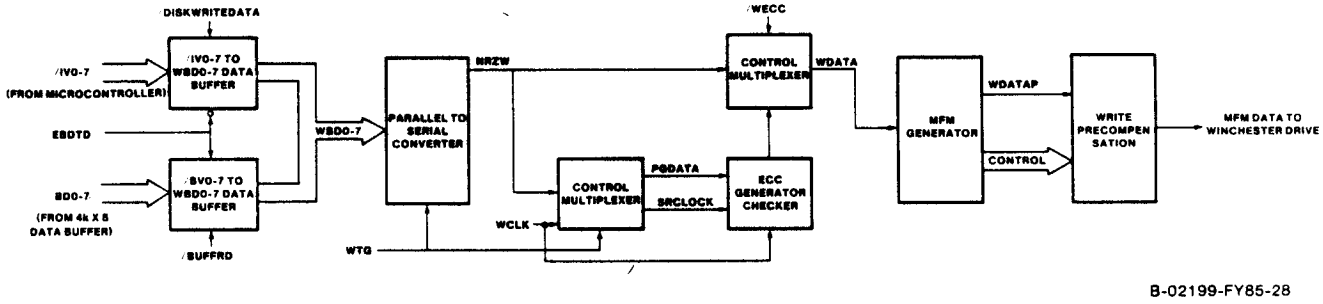

FIGURE 3.5-4
Winchester Write Block Diagram.

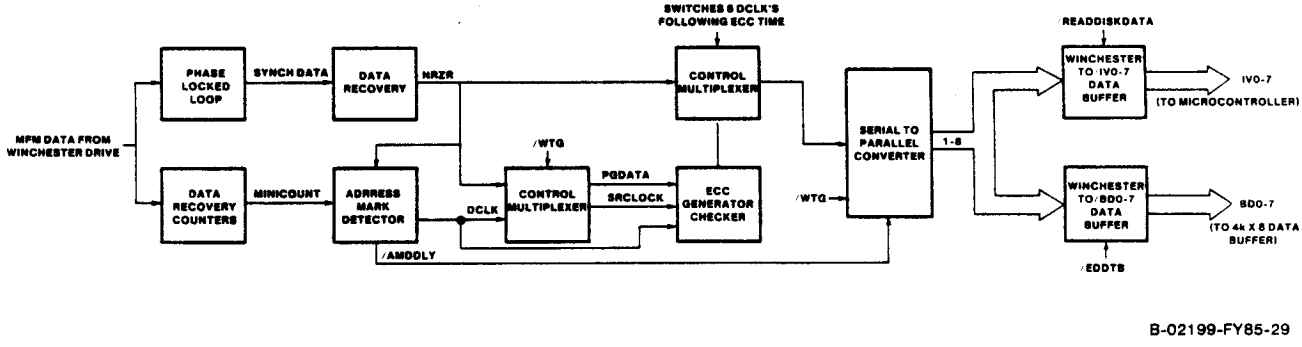

FIGURE 3.5-5
Winchester Read Block Diagram.

Parallel data from L107 can be read onto the BD0-7 bus (via L108) or the &IV0-7 bus (via L123), depending on which control signals are generated. An active &READDSKDATA signal reads Winchester data onto the &IV bus via the Winchester to &IV0-7 Bus Data Buffer (L123). An active Enable Disk Data To Buffer (&EDDTB) signal reads the data onto the BD0-7 bus via the Winchester to BD0-7 Bus Data Buffer (L108). Section 3.5.1 contains information concerning the generation of control signals needed to move data through buffers L108 and L123.

3.5.5 ECC Generator/Checker

ECC hardware on the RCU board (FIGURE 3.5-6) monitors the outgoing (to the Winchester) data stream to generate three Error Check and Correct (ECC) bytes during a write operation; during a read operation, it also checks the data and the ECC bytes. The ECC Syndrome bytes issued by the ECC Circuit during a read operation should contain all zeros. If all zeros are not present, an error has been detected and the Microcontroller initiates several retries to reread the data. If ECC errors are encountered after numerous retries, the Microcontroller passes the data and the ECC bytes to the Z80A on the RMU board. The Z80A performs an error correcting algorithm if the error is less than or equal to an 8-bit burst error. If the error cannot be corrected, the Z80A notifies the slave requesting the read operation of the sector error. If a non-correctable error occurs during an RMU read of primary data from the Winchester (ie, code area, catalog map, vowel map, or alternate vowel map) a fatal system error occurs.

When writing data to the Winchester, the ECC Write Control Shift Register (L23) and associated logic (L8 and L9) monitor the NRZW data stream and the Skip Enable (SKPEN) signal to detect the FBH byte that occurs in the NRZW data stream before the data field (see Section 3.5.2). When FBH is detected, L23 issues a signal from pin 13 to release the clear from the ECC Shift Registers (via L22) so that the shift registers can begin to accept the data field that follows.

During write operations the NRZW data stream from the Serial to Parallel Converter (L141) is routed to pin 5 of Control Multiplexer L19, where it is multiplexed to become the PGDATA signal. PGDATA is routed to the pin 4 input of ECC Parity Generator L46 to serve as the data stream input to the ECC Checker Circuit. The Write Clock (WCLK) signal from the Write Clock Flipflop (L75) asserts the pin 3 input of L19 to become the SRCLOCK signal used as the shift clock for the ECC Shift Registers (L6, L21, and L32). (Due to the active Write Gate (&WTG) select signal, the A inputs are selected to be passed through L19.)

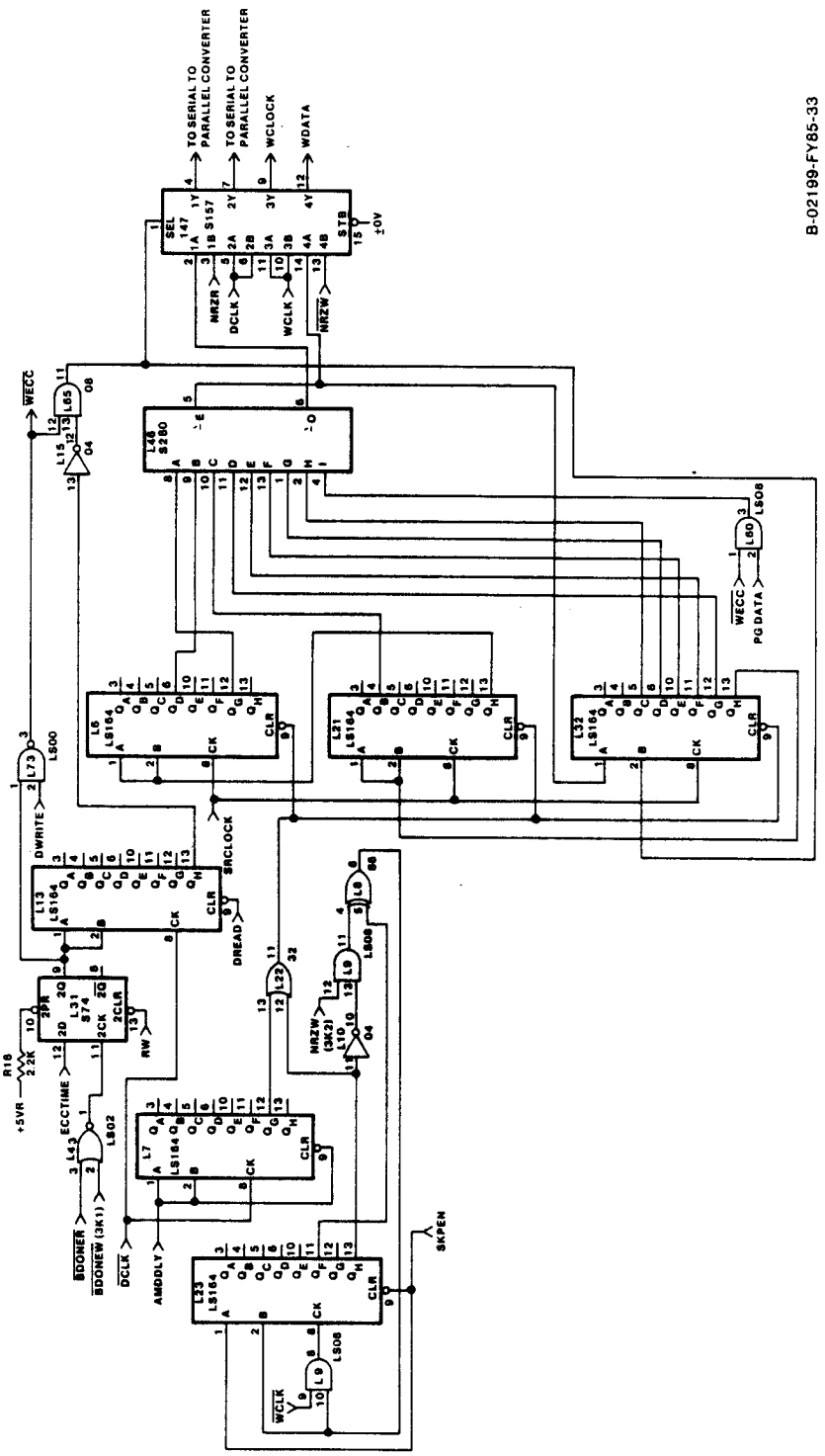

FIGURE 3.5-6
ECC Generator/Checker Logic.

Once the ECC Shift Registers are enabled, each cycle of SRCLOCK causes a data shift, and a unique polynomial is developed based on the value of PGDATA that is entered into the ECC Parity Generator (L46). The ECC Parity Generator, as a result of the summation inputs from the shift registers, serially generates three ECC bytes from pin 5 following the 256-byte data field.

Once the write data field is shifted through the ECC Shift Registers, Control Multiplexer L47 must be selected to forward the ECC bytes from L46 into the outgoing data stream. To initiate this action, the ECC Time Enable (ECCTIME) control signal from the Winchester Interface Control Signal Generator (L119) asserts the pin 12 input of the ECC Output Control Flipflop (L31). As the Byte Done Written (&BDONEW) signal is activated for the 256th data byte written, it clocks flipflop L31 to generate a signal which is gated with the active Drive Write (DWRITE) signal at L73 to create an active Write ECC (&WECC) signal. The activated &WECC signal drives the select pin of the Control Multiplexer low (via L65) to select the ECC circuit's output as the input to the data stream. Once selected, pin 14 of Control Multiplexer L47 passes the three ECC bytes generated by the ECC Circuit into the data stream immediately after the data field.

The low signal asserting the Control Multiplexer's select signal also asserts pin 2 of ECC Shift Register L32, forcing three bytes of zeros through the ECC Shift Registers. Three bytes of 00H must be shifted through the ECC Circuit to force out the ECC bytes for the write data field. The active &WECC signal asserts pin 1 of L60 to prevent any data (PGDATA) from asserting the ECC Parity Generator while the parity generator is producing ECC bytes.

When reading data from the Winchester, the ECC circuit must be enabled to accept and check data at the beginning of the data field that follows the address mark and the FBH byte (see Section 3.5.2). The ECC Read Control Shift Register (L7) monitors the &AMDDLY signal in order to generate a signal to enable the ECC Shift Registers at the proper time. When the address mark is detected, Address Mark Detector L29 generates the active &AMD signal. &AMD is delayed (by one DCLK signal) through Address Mark Delay Flipflop L5 to generate an active &AMDDLY signal. Since the active &AMDDLY signal has been delayed by one DCLK signal, it enables Read Control Shift Register L7 during the second DCLK signal used to read the FBH byte. The enabled Read Control Shift Register shifts through seven DCLK bits (used in reading the FBH byte) before generating an ECC Shift Register enabling signal from pin 12. The high enabling signal from pin 12 asserts the low-cleared pin of the ECC Shift Registers via L22 to prevent the registers from being cleared. The ECC Shift Registers then begin to shift the data field and the ECC field through in order to check for errors.

During read operations the NRZR data stream from the Data Recovery Circuit is routed to pin 6 of Control Multiplexer L19 where it is multiplexed to become the PGDATA signal. PGDATA is routed to the pin 4 input of ECC Parity Generator L46 to serve as the data stream input to the ECC Checker Circuit. The DCLK output from Address Mark Detector L29 is routed to the pin 3 input of L19 where it becomes the SRCLOCK signal used as the shift clock for the ECC Shift Registers (L6, L21, and L32). (The B inputs are selected to be passed through L19 due to the inactive Write Gate (&WTG) select signal.) Once the ECC Shift Registers are enabled, each cycle of SRCLOCK causes a data shift, and a unique polynomial is developed based on the sum of PGDATA that is entered into ECC Parity Generator L46. After the 256-byte data field and three ECC bytes are shifted through, the ECC Parity Generator serially generates three ECC Syndrome bytes from pin 5.

Once the read data field and the ECC bytes are shifted through the ECC Shift Registers, Control Multiplexer L47 must be selected to forward the ECC Syndrome bytes from L46 into the data stream. To initiate this action the ECCTIME control signal from the Winchester Interface Control Signal Generator (L119) asserts pin 12 of the ECC Output Control Flipflop (L31). The Byte Done Read (&BDONER) signal, activated for the 258th byte read (the 2nd ECC byte), clocks flipflop L31 to generate a signal which enables ECC Output Control Shift Register L13. When enabled, L13 shifts once upon encountering each of the last eight &DCLK signals used to read the 256th data byte. The eighth &DCLK signal asserting L13 causes L13 to create a high signal from pin 13 which is inverted to drive Control Multiplexer L47's select pin low. Driving L47 pin 1 low selects the ECC Circuit's output as the input to the data stream (pin 2 to pin 4). Once the Control Multiplexer is selected, pin 4 passes the three ECC Syndrome bytes generated by the ECC Circuit into the data stream immediately after the data field and the three ECC bytes.

The low signal that asserts the Control Multiplexer's select signal also asserts pin 2 of ECC Shift Register L32 to insert three bytes of zeros through the ECC Shift Registers. Three bytes of 00H must be shifted through the ECC Circuit to force out the ECC Syndrome bytes. If no errors are encountered, the ECC Syndrome bytes contain all zeros.

3.5.6 Winchester Step Logic

The Winchester Step Logic shown in FIGURE 3.5-7 generates a 6-us &STEP signal that commands the Winchester heads to move one step in a predefined direction during a track seek operation. Hardware on the RCU board generates the &STEP signal in predefined increments in order to step, or move, the head to the desired track for the read or write operation. The direction of head step motion depends on the status of the &DIRECTION signal generated by the Winchester Disk Drive Program Signal Generator (L136). The Winchester Step Logic is controlled by several right bank I/O control signals.

During each read or write operation the Microcontroller loads an initial step count into Winchester Step Counters L104, L105, and L106. The Low-Order Step Counters (L104 and L105) are loaded first, via IV0-7, when the Write Low-Order Track Step Counter (&WRITELOTSC) signal is activated on pin 11. Following the low-order step count

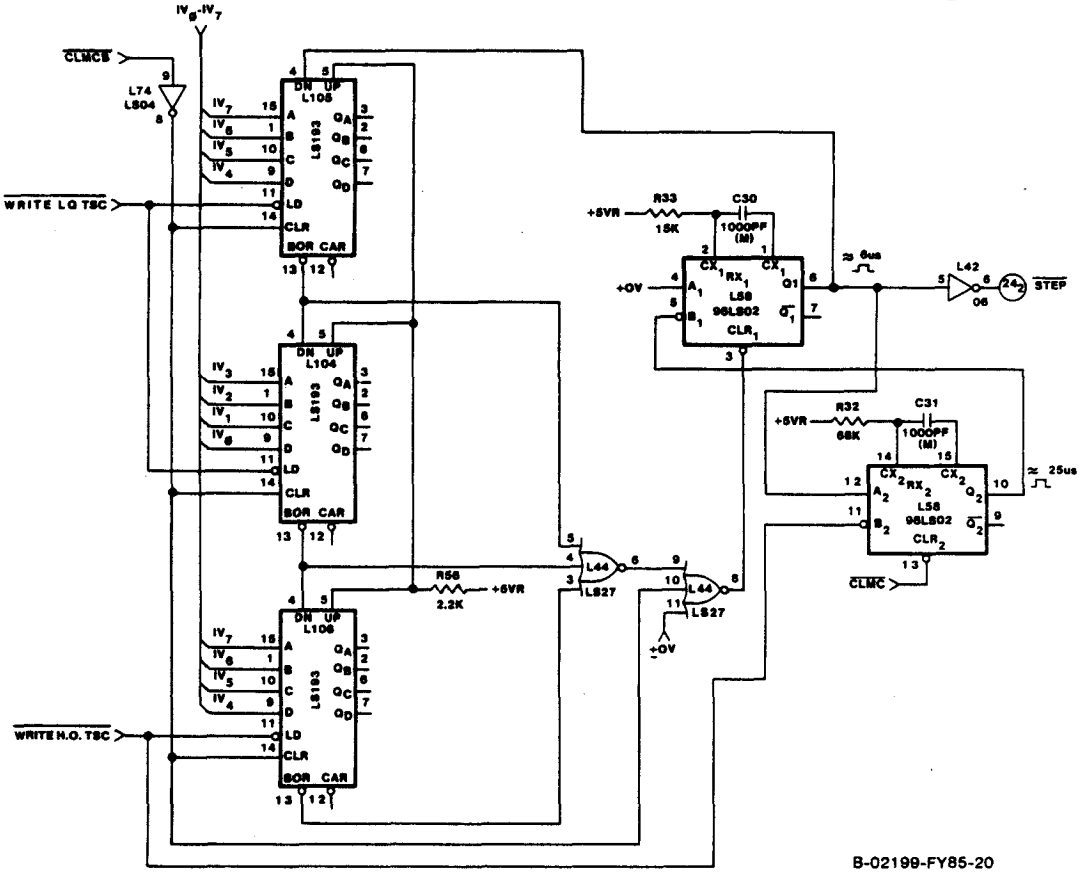

FIGURE 3.5-7
Winchester Step Generating Logic.

loading, the high-order step count is loaded into L106, via IV4-7, upon the arrival of the active Write High-Order Track Step Counter (&WRITEHOTSC) signal on pin 11. The activated &WRITEHOTSC signal also asserts pin 11 of the Step Pulse Rate 1-Shot (L58, Q2 output) to trigger the generation of a 25-us step rate pulse. The step rate pulse asserts the Step 1-Shot (L58, Q1 output) to generate an active 6-us &STEP signal from pin 6 every 25 us. The active &STEP signal regenerates the step rate pulse by asserting L58 (2Q output) pin 12, decrements the Winchester Step Counters by asserting L105 pin 4, and asserts the Winchester to step the head in the proper direction.

Since the three step counters are cascaded, the initial count is decremented as each active &STEP signal asserts the down-count pin of L105. When the counters have decremented to zero, their borrow pins are in the active low state. The low borrow signals are gated at L44 to generate a signal that is passed through L44 to clear Step 1-Shot L58 and prevent additional &STEP signals from being generated.

When the Winchester has completed a seek operation it issues the &SEEKCOMPLETE signal. The Microcontroller reads the &SEEKCOMPLETE signal through the Winchester Status Register (L121) using the &READDSKSTATUS command. The active &SEEKCOMPLETE signal also triggers the Winchester Seek Complete 1-Shot (L34) to fire a 2-us Winchester Seek Complete (&WSKCOMP) signal from pin 7. The active &WSKCOMP signal is sent to the CTC on the RMU board where it generates an interrupt to the Z80A processor, informing the processor that the Winchester seek operation has been completed.

3.5.7 Dead Man Timer

Dead Man Timer Counter L14 monitors the INDEX and Read or Write (RW) signals to ensure that the system is never "hung" during Winchester read or write operations. When a Winchester read or write operation is initiated, the RW signal is activated to turn off L14's clearing signal, allowing L14 to begin counting active Index One Shot (&IOS) signals on pin 5. An &IOS signal is generated as each index mark is detected on the disk. (One index mark should be encountered on each disk revolution.) If RW is not deactivated prior to the detection of 16 active &IOS signals, L14 generates a carry signal from pin 12 that asserts the Control Unit Not Busy 1-Shot (L34) to generate the Control Unit Not Busy (&CUBUSY) interrupt signal.

&CUBUSY is sent to the CTC on the RMU board, where it generates an interrupt to the Z80A. The Z80A, once interrupted, performs a service routine to determine the cause of the interrupt. When the Z80A determines that a dead man interrupt has been generated, it initiates a subroutine to clear the problem.

3.5.8 Phase Locked Loop

The Phase Locked Loop (PLL) Circuit shown in FIGURE 3.5-8 generates a known center frequency clock which is used to synchronize read data during a Winchester read operation. When not in the read mode the circuitry generates a center frequency by feeding back a VCO-generated frequency and comparing that frequency to the WCLK signal (200 ns per bit). When a read operation occurs the PLL Circuit is switched to accept MFM data from the Winchester. The Phase Locked Loop will then track data coming from the Winchester.

Phase/Frequency Detector L87 detects WCLK on pin 1 and compares WCLK's phase and frequency with the phase and frequency of the signal generated by VCO L56. If the signals' phases and/or frequencies differ, L87 produces error signals on pins 2 and 13. The L71 gates sum these signals and send them to Op Amp L55, which creates an error voltage output relative to the signals it receives. The error voltage issued from L55 asserts pin 2 of VCO L56. In response, L56 generates a frequency (from pin 7) that is dependent on the error voltage applied to pin 2. The VCO-generated frequency asserts L57, which then halves the frequency and issues it from pin 9. The frequency from pin 9 again asserts the Phase/Frequency Detector to continue the loop, guaranteeing a predictable center frequency until a read operation occurs.

During read operations, the Microcontroller issues a high Drive Read (DREAD) signal, causing the Phase Locked Loop to accept incoming data from the Winchester drive. The active DREAD signal first asserts pins 11 and 8 of L71 to prevent the Phase/Frequency Detector from issuing error information to L55, the Phase Locked Loop Op Amp. DREAD drives L88 (1Q output) pin 2 high, enabling L88 to generate output signals corresponding to the clocking signals it receives from the MFM-encoded input. Data from L88 (1Q output) is passed to the Phase Locked Loop Circuit via L70 and L88 (2Q output). L88 (2Q output) is enabled by the activated DREAD signal on pin 10.

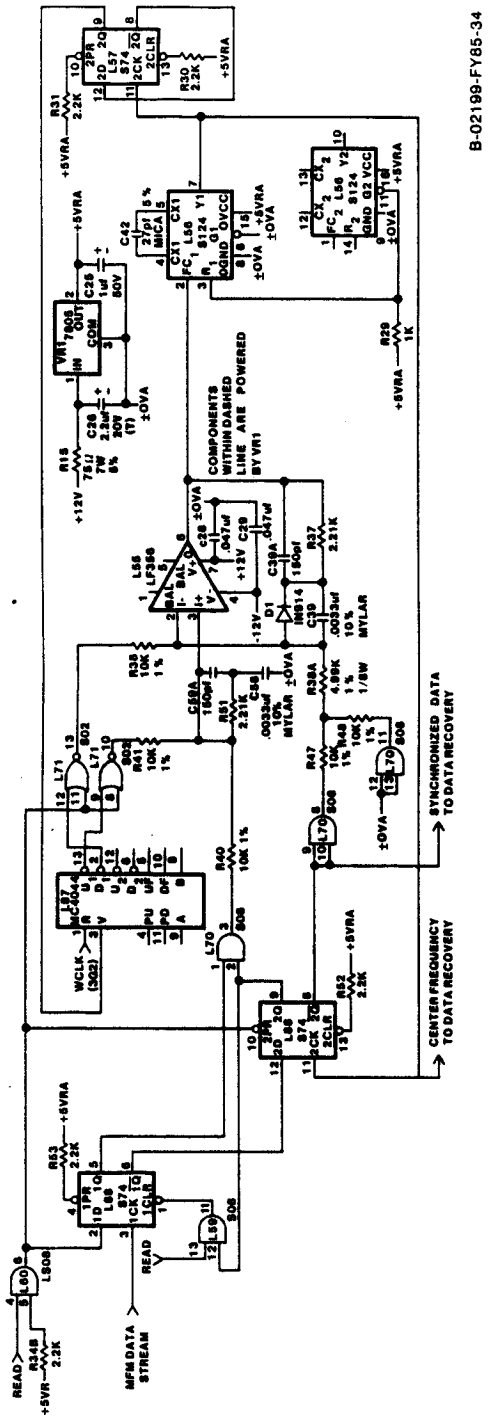

FIGURE 3.5-8
Phase Locked Loop Logic.

Once enabled, L88 (2Q output) generates synchronized data signals by synchronizing incoming data (on pin 12) with the clock frequency being generated by VCO L56 (on pin 11). Synchronized data signals from L88 (2Q output) are continually fed through the PLL to reduce the phase error and, therefore, keep the VCO-generated frequency in the desired range (ie, tracking data from the Winchester). Synchronized data from L88 (2Q output) pin 8 is also forwarded to the Data Recovery Circuit so that the data bits can be separated from the clock bits.

3.5.9 Data Recovery

The Data Recovery Circuit (FIGURE 3.5-9) accepts the synchronized data stream from the Phase Locked Loop Circuit and separates the data bits from the clock bits to generate an NRZR data stream and DCLK signals. The data field of the data packet from the Winchester always follows the address mark and the FBH byte (see Section 3.5.2). The Data Recovery Circuit monitors the data stream for the address mark before allowing the data through to the ECC Circuit. Data is constantly being separated prior to detection of the address mark; however, data is never moved out of the Data Recovery Circuit into the Serial to Parallel Converter until a valid address mark is detected.

An address mark always precedes the ID field and the data field of each formatted sector. The address mark is a unique mark, recognized by the hardware as an A1H byte with a missing clock bit. Either an ID field or a data field will follow the address mark. If an FEH byte follows the address mark, an ID field will follow the FEH byte. If an FBH byte is detected after the address mark, a data field will follow.

The Address Mark Detector (L29) searches for the A1H address mark after detecting the Mincount (eight bytes of zeros) and before the Maxcount (16 bytes of zeros) is reached (see Section 3.5.2). The Data Recovery Counters (L30) receive MFM data on pin 1 to directly count up to 16 bytes of zeros. If eight bytes of zeros are detected, L30 generates a signal from pin 9 that clocks L2 to generate the MINCOUNT signal. MINCOUNT enables Address Mark Detector L29 by asserting pin 9. If 16 bytes of zeros are detected, L30 pin 8 generates a Maxcount signal which indirectly (through L17 and L18) clears the Data Recovery Circuit and the Data Recovery Counters. Following Maxcount detection, the search for the Mincount that must precede address mark detection begins again.

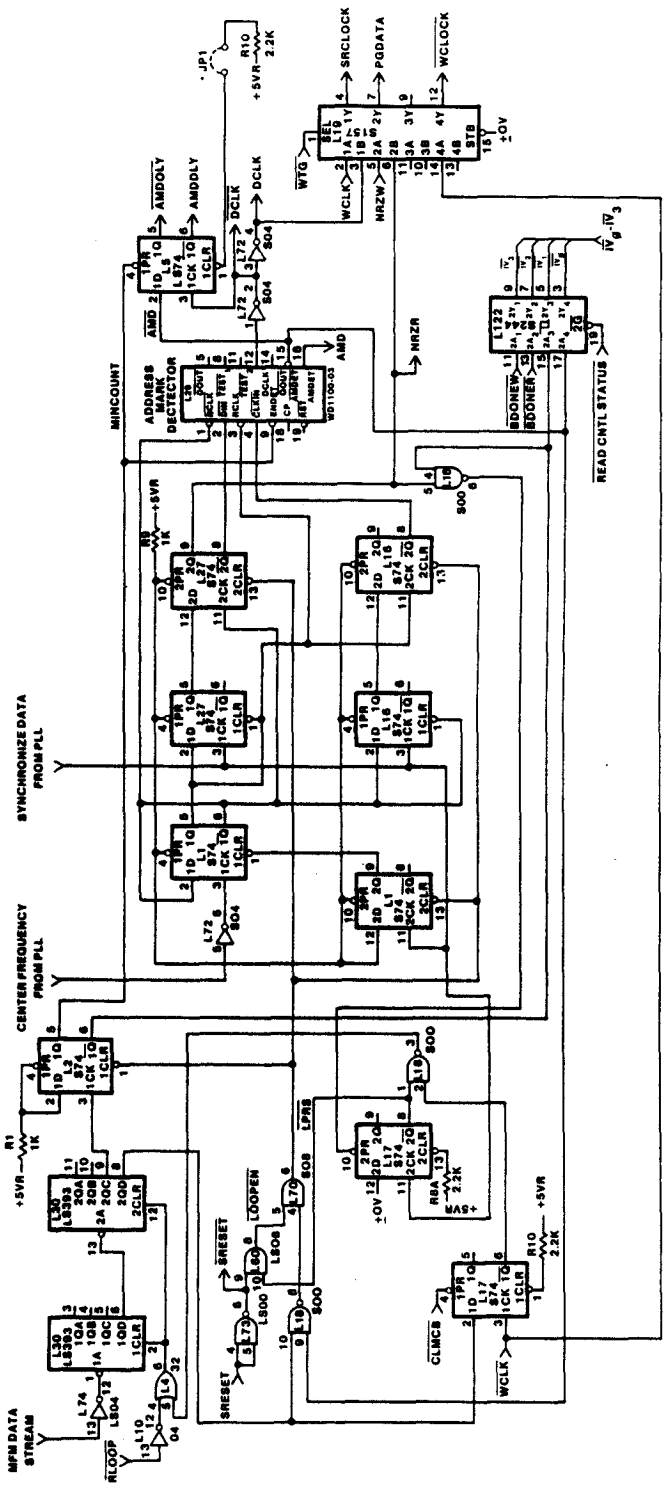

FIGURE 3.5-9
Data Recovery Logic.

Once the Data Recovery Counters (L30) have reached the Mincount of eight bytes of zeros, L2 issues a signal from pin 5 to enable Address Mark Detector L29 by asserting pin 9. Once enabled, L29 monitors the Data Recovery Circuit's NRZR data stream output on pin 2. Utilizing the separated clock bits as the clock input, L29 searches for the A1H bit with the missing clock bit. Upon detecting the address mark, L29 activates the Address Mark Detect (AMD) signals from pins 15 and 16 and the Data Clock (DCLK) signal from pin 12. An active AMD signal indicates that the address mark has been detected. DCLK represents the separated clock bits from the Data Recovery Circuit.

The AMD signal generated by L29 is delayed by L5 to create the Address Mark Detect Delayed (AMDDLY) signals. AMDDLY is used to enable the ECC Checker circuit at the proper time, and &AMDDLY asserts the Start (&ST) pin of the Serial to Parallel Converter to allow the converter to accept serial data. The Data Clock (DCLK) signals generated by L29 are used as clocking signals throughout the ECC Circuit. DCLK is buffered through Control Multiplexer L19 to create the Shift Register Clock (SRCLOCK) signal which is used as the ECC Shift Register clock. L19's read inputs are selected at this point by the inactive Write Gate (&WTG) signal on pin 1. NRZR data from the data separator is passed through Control Multiplexer L19 to become the PGDATA signal, which is used as the ECC Shift Register's data input. NRZR data is also forwarded through Control Multiplexer L47 to Parallel to Serial Converter L107. L47's "B" inputs are selected at this point to pass the NRZR data stream through. Following the data field and the ECC bytes, the Control Multiplexer's "A" inputs are selected so that the ECC Syndrome bytes can be moved out of the ECC Shift Registers and into the Serial to Parallel Converter.

The Microcontroller monitors the status of the Winchester read operation by reading primary status information onto bits &IV0-3 via the Control Status Register (L122, 2Y outputs). The Microcontroller polls the Control Status Register throughout the read operation by issuing the &READCNTLSTATUS signal to L122 pin 19. It reads the status of the &MINCOUNT signal and the &AMD signal through bits &IV1 and &IV0, respectively. By reading these signals periodically the Microcontroller determines what portion of the data stream it is currently reading. If the Microcontroller detects an active &AMD signal, for example, it begins to check for the FEH or FBH byte that should follow to determine whether the ID field or the data field is upcoming. The Microcontroller also monitors the Byte Done Written (&BDONEW) and Byte Done Read (&BDONER) signals via L122 and bits &IV3 and &IV2. The Control Status Register's 1Y outputs are used to read the Winchester disk drive device type, as explained in the beginning of this chapter.

3.5.10 Data Recovery Logic Reset Control

Several conditions clear the Data Recovery Circuit and/or the Data Recovery Counters. Some of these conditions are quite common, and others occur infrequently, during error situations. Two conditions require both the Data Recovery Circuit and the Data Recovery Counters to be cleared. One condition clears only the Data Recovery Circuit; in this case, the Data Recovery Counters are cleared in another manner. Two conditions clear only the Data Recovery Counters.

Two conditions require both the Data Recovery Circuit and the Data Recovery Counters to be cleared. The first of these conditions is detected when separated data is available before the MINCOUNT signal is generated. Gate L18 detects this condition when separated NRZR data on pin 5 and an inactive &MINCOUNT signal on pin 4 combine to generate a low signal from pin 6. This low signal from L18 presets the Load Preset Flipflop (L17, 2Q output) to generate the Loop Reset (&LPRS) signal from pin 8. The active &LPRS signal is gated through L60 and L70 to generate the data recovery clearing signal from L70 pin 6. &LPRS is also gated through L18 and L4 to clear the Data Recovery (Mincount/Maxcount) Counters, resetting them so that they can begin counting zeros again.

The second condition requiring both the Data Recovery Circuit and the Data Recovery Counters to be cleared is the issuance of the Software Reset (SRESET) command. The Microcontroller issues SRESET when certain errors are detected, and at the end of every successful operation. SRESET, when activated from L119 pin 15, asserts L60 pin 9 to generate the Loop Enable (&LOOPEN) signal from pin 8. &LOOPEN is gated through L70 to generate the data recovery clearing signal from pin 6. The Data Recovery Counters are cleared as the active &SRESET signal is gated through L36 to generate the active Read Loop (&RLOOP) signal. &RLOOP clears the counters via L4.

One condition clears only the Data Recovery Circuit; in this case, the active Maxcount signal typically clears the Data Recovery Counters. Hardware generates a Data Recovery Circuit clearing signal if the Maxcount signal is generated prior to the detection of the Address Mark Detect (&AMD) signal. L18 detects this condition since L18 receives the Maxcount and &AMD signals on its inputs (pins 9 and 10). If Maxcount is activated while &AMD is deactivated, L18 generates a low signal from pin 8 that is gated through L70 to generate the Data Recovery Circuit clearing signal from pin 6. The Maxcount signal clears the Data Recovery Counters whenever it is activated.

Two conditions require only the Data Recovery Counters to be cleared. Whenever Maxcount is reached, the Data Recovery Counters must be reset to begin a new count. The active Maxcount signal asserts L17 (1Q output), where it is synchronized with the Write Clock (WCLK) signal. The low output of L17 is gated through L18 and L4 to clear the Data Recovery Counters. The Data Recovery Counters are also reset whenever an INDEX signal is detected, since the synchronizing field of zeros always follows the index mark and Gap 1 (see Section 3.5.2) of the first sector encountered in each track. The active &INDEX signal asserts Index 1-Shot L48 to generate an active 10-us Index One Shot (&IOS) signal. &IOS is gated through L36 to generate the active Reset Loop (&RLOOP) signal. &RLOOP asserts the clear pins of the Data Recovery Counters via L4 to clear the counters so that they can begin counting zeroes.

3.6. STATUS AND PARAMETER REGISTER FILES

Two memory areas on the Resource Control Unit (RCU) board pass data and status information between the Resource Management Unit (RMU) and the RCU: the 16-byte Parameter Register File (PRF) and the 12-byte Status Register File (SRF). Both the Z80A and the Microcontroller can read from or write to the PRF; they cannot, however, access the PRF simultaneously. Only the Z80A can read from the SRF, and only the Microcontroller can write to it.

Typically the Z80A microprocessor in the RMU loads the PRF with the command codes and data that the RCU needs to perform a specific operation (see Appendix D of the RMU Theory of Operation). When the Z80A sets the Command Notification (CMD) bit, the Microcontroller operates on the PRF as needed to complete the command. (Generally, the Microcontroller moves the PRF data to its scratchpad RAM and then releases the PRF.) The Microcontroller completes the command and returns information to the RMU via the PRF or SRF.

Status and error information returns to the RMU via the dual-ported SRF. When the Microcontroller is busy, RCU Busy status information is set in byte FF10 of the SRF. Status information concerning data link block operations resides in SRF bytes FF11 and FF12. SRF bytes FF13-FF15 contain status information about 1-byte data link operations, and bytes FF16-FF1B contain status information about the Winchester disk drive.

3.6.1 SRF-PRF Control

Both the RCU and the RMU can read from or write to the PRF, but no two operations can occur simultaneously. However, only the RCU (ie, the Microcontroller can write to the SRF, and only the RMU (ie, the Z80A processor) can read from the SRF. The Microcontroller controls its operations involving the PRF and the SRF via L80, the Right Bank I/O Decoder. By issuing I/O commands to ports 10-1FH, the Microcontroller can perform PRF read and write operations. The Microcontroller issues I/O commands to ports 00-0BH to perform SRF write operations. (Sections 3-1 and 3-2 contain additional information on issuing the I/O commands that control SRF and PRF data access operations.)

The Z80A maintains control of SRF and PRF data access operations by issuing I/O commands via the Z80A address, data, and control buses. The Z80A issues I/O commands FF10-FF40 for RCU-resident I/O decoded operations. Addresses FF10-FF1F are reserved for reading SRF-resident data. Addresses FF20-FF2F are used to move data to and from the PRF.

3.6.2 Status Register File

The Status Register File is a 12-byte (8-bit words) storage area that uses six 4 x 4 storage devices. As shown in FIGURE 3.6-1 and 3.6-2, the SRF is the common ground for status information passed from the RCU to the RMU. The Microcontroller places status information in the SRF after completing an operation. The RMU then reads the status information from the SRF and uses this information to determine whether the operation was performed successfully. Only the Microcontroller can write to the SRF and only the RMU can read from the SRF.

Status information from the scratchpad memory is read by the Microcontroller and then loaded into the SRF via the &IV bus. The Microcontroller controls writing data into the SRF via SRF Write Bank Decoder L79. When the Microcontroller accesses the SRF, L79 issues the SRF Write Bank (&WB1-3) signals to control bank selection within the SRF (see Table 3.3-1). &WB1 (ports 00-03H) asserts SRF Registers L151 and L152. &WB2 (ports 04-07H) asserts registers L134 and L135, and &WB3 (ports 08-0BH) asserts registers L113 and L117. Addresses of data within the SRF are provided via right bank address bits &RBA0-1.

The RMU requests data from the SRF by issuing one or more of the FF10-FF1B addresses (on A0-5) and asserting the active Memory Mapped Input/Output (&MMI/O) signal to the Z80A I/O Decoder (L98) on the RCU board. Upon receiving an active &MMI/O signal and any address between FF10-FF1B on the A0-7 bus, L98 generates the Status Register File Read (&STATUS) signal from pin 2.

When passed through Z80A Address Bus Buffer L99, Z80A address bits A0-3 generate the Z80A inverted buffered address bits (&ZBA0-3). Read Bank Decoder L103 (when enabled by active Status Register File Read and Z80A Read Request signals) uses ZBA2-3 to generate &RB1-3. &RB1-3 select the particular SRF bank to be read. Each &RB signal (1-3) asserts enabling pins on two SRF chips, thereby enabling a read of an entire 8-bit byte (addressed by &RBA0-1) when &RB1, &RB2, or &RB3 is active.

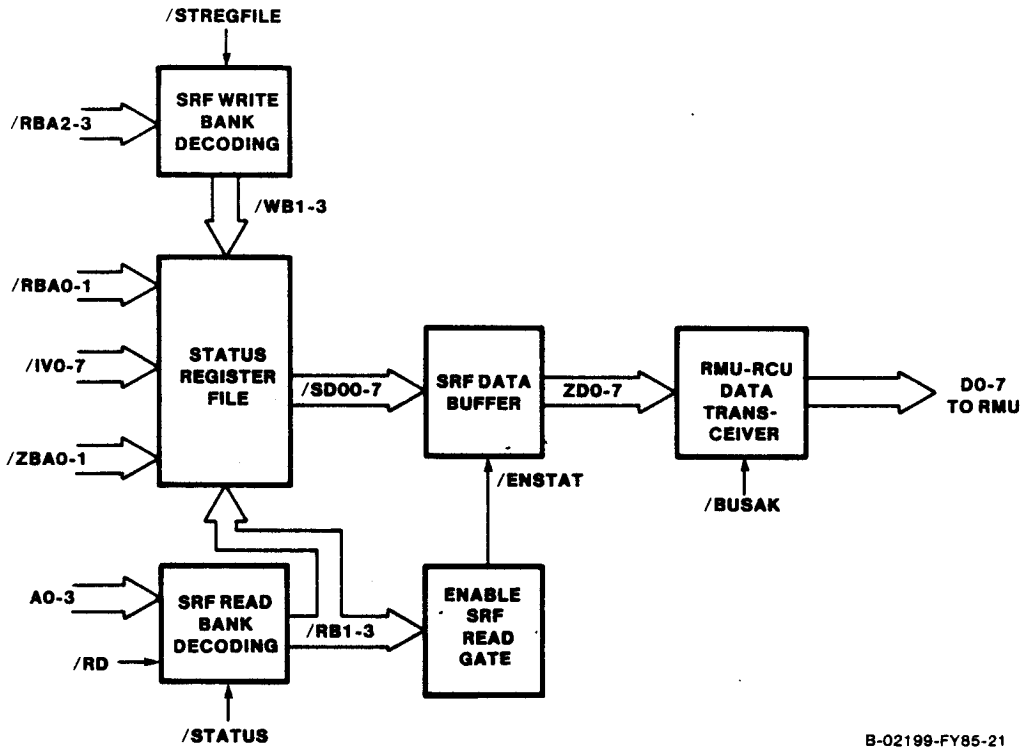

FIGURE 3.6-1
Status Register File Block Diagram.

After an &RB signal has enabled two SRF chips, the data byte is moved out of the SRF via the &SD00-7 bus and passed through the enabled SRF Data Buffer (L150). L150 is enabled to provide output by the Enable SRF Read (&ENSTAT) signal, which is generated whenever any of the &RB1-3 signals is active on the inputs of L86. Data from the SRF can then be passed to the RMU via RMU-RCU Data Transceiver L149 (if the proper enabling and direction control signals have been activated). Control of data movement between the RMU and the RCU relies upon the RMU-RCU data direction control hardware explained in Chapter 1.

3.6.3 Microcontroller Writes to the SRF

The Microcontroller issues control signals and addresses to order the Right Bank I/O Decoder (L80, see Chapter 3) to issue the Status Register Functions Strobe (&STREGFILE) command. For an SRF write operation, SRF Write Bank Decoder L79 is enabled by the &STREGFILE signal from pin 7 of the Right Bank I/O Decoder. &STREGFILE is synchronized with the &RBODMCLK (Right Bank Output Data synchronized with Master Clock) signal at L81 to generate a signal to enable the SRF Decoder. Once enabled, address bits &RBA2-3 determine which of the three Write SRF Bank (&WB1-3) signals is issued. (Table 3.3-1 displays the relationship of the &RBA2-3 addresses supplied to the

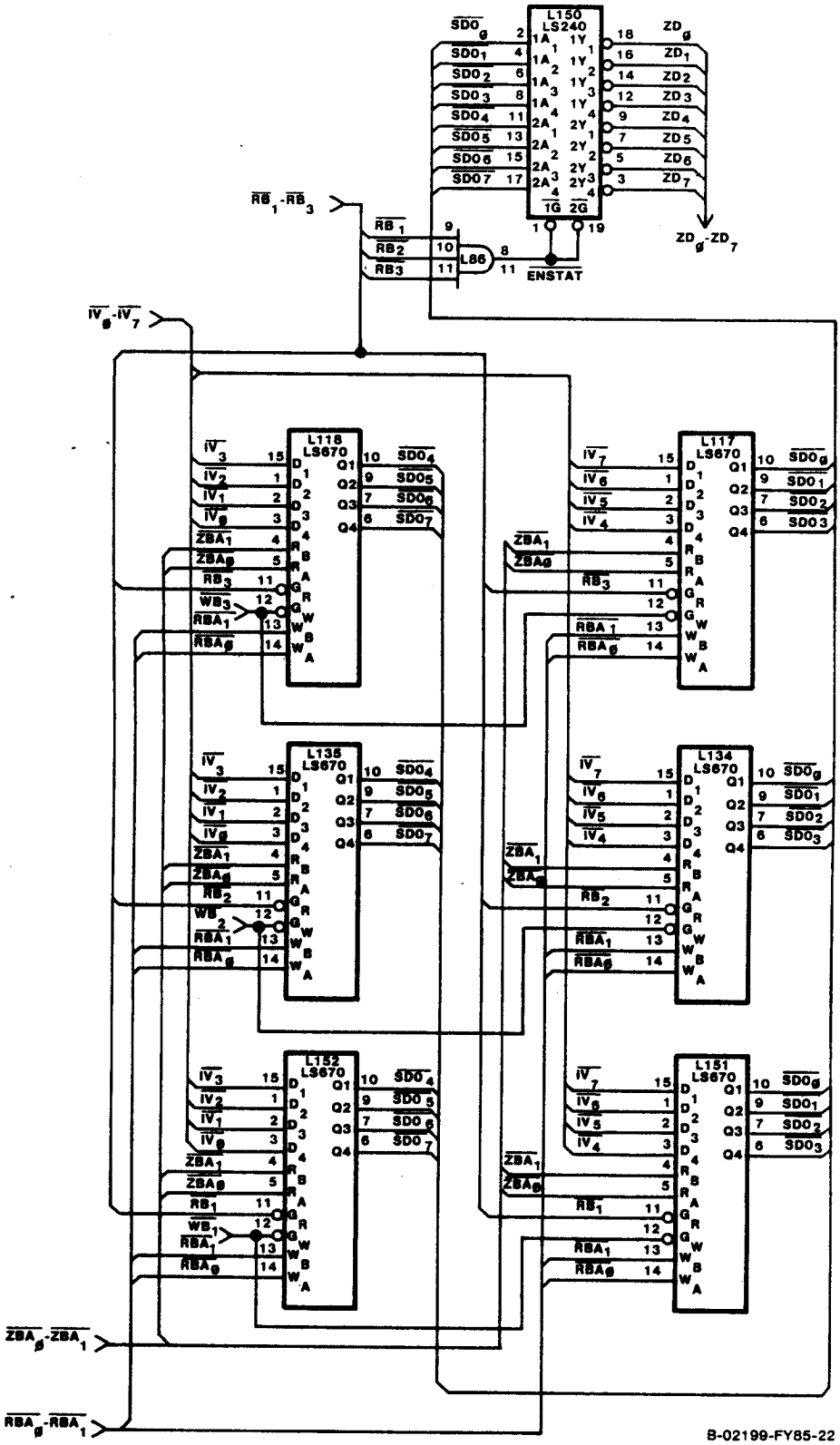

FIGURE 3.6-2
Status Register File Logic

&WB1-3 signals issued.) SRF data addresses are generated by the Microcontroller and then supplied to the SRF from the &IV bus, through L85, via the &RBA bus. Bits &RBA0-1 assert pins 14 and 13 of the SRF chips to specify the Microcontroller-requested address. The Microcontroller-generated address is selected (instead of the Z80A-generated address, which is selected via pins 4 and 5) as the data location when a Write Bank (&WB1-3) signal is activated on pin 12 of any SRF chip.

3.6.4 RMU Reads from the SRF

The RMU reads SRF data via Z80A-generated I/O commands FF10-FF1B, which are carried to the RCU on the Z80A address bus. Z80A address bits assert L98, the Z80A I/O Decoder, and L99, the Z80A Address Bus Buffer, to control SRF read operations. When the RMU issues a command (between FF10-FF1B) to read the SRF, the Z80A I/O Decoder issues the &STATUS command from pin 2 of L98. The &STATUS command and the &RD command enable Read Bank Decoder L103 by asserting its pins 15 and 14. When enabled, L103 uses address bits &ZBA2-3 to generate the Register Bank Enable (&RB1-3) signals.

Each &RB signal (1-3) generated by L103 asserts enabling pins on two SRF chips, thereby enabling a read of an entire 8-bit byte when &RB1, &RB2, or &RB3 is active. Each &RB signal asserts pin 11 of two SRF chips to enable the chips and to select the &ZBA0-1 addresses (instead of the &RBA0-1 addresses) for data retrieval. After the &RB signal has enabled two SRF chips, the addressed data byte is moved out of the SRF via the &SDO0-7 bus and passed through the inverting SRF Data Buffer (L150) onto the ZD0-7 bus. L150 is enabled by the Enable SRF Read (&ENSTAT) signal, which is generated whenever any of the &RB1-3 signals is active on the inputs of L86. Data from the ZD0-7 bus can then be passed to the RMU via RMU-RCU Data Transceiver L149, if proper enabling and direction control signals have been activated (see Chapter 1 for information on RMU-RCU data direction control).

3.6.5 Parameter Register File

The Parameter Register File (PRF) passes data (commands and parameters) between the RMU and the RCU. The Z80A begins an operation by issuing commands to the RCU via the PRF (see FIGURE 3.6-3 and 3.6-4). The Microcontroller reads the data from the PRF and then transfers that data into the scratchpad. The Microcontroller executes the RMU-generated command and returns necessary data to the scratchpad. To transmit the scratchpad data to the SRF or PRF, the Microcontroller first reads the data and then transfers it to either the SRF or PRF.

The 16-word (8-bit words) PRF consists of two 16 x 4 chips (L100 and L101). Data enters the PRF via the Parameter Data In (&PDI0-7) bus and exits the PRF via the Parameter Data Out (&PDO0-7) bus. Addresses are supplied to the PRF via PRF Address Multiplexer L102. Addresses are supplied to the multiplexer by either bits &RBA0-3 (when the Microcontroller has control of the PRF) or bits &ZBA0-3 (when the Z80A has control of the PRF). The RMU accesses PRF data via the L115 (Read Data) and L116 (Write Data) PRF Data Buffers. The Microcontroller access PRF data via the L84 (Read Data) and L133 (Write Data) PRF Data Buffers. The Microcontroller and the Z80A maintain separate read/write control over PRF data access operations.

3.6.6 Microcontroller Accesses the PRF

During a Microcontroller-controlled PRF read or write operation, the Microcontroller issues the appropriate control signals and addresses to cause the Right Bank I/O Decoder to issue the active Parameter Register File Functions Strobe (&PARREGFILE) signal. The active &PARREGFILE signal is gated through L97 (from pin 5 to pin 6) to create a low signal that selects the PRF for operation by asserting the select pin of each PRF chip. &PARREGFILE also proceeds to the PRF direction control logic, where it asserts L64 pin 9 to enable Microcontroller control of the PRF's read/write direction.

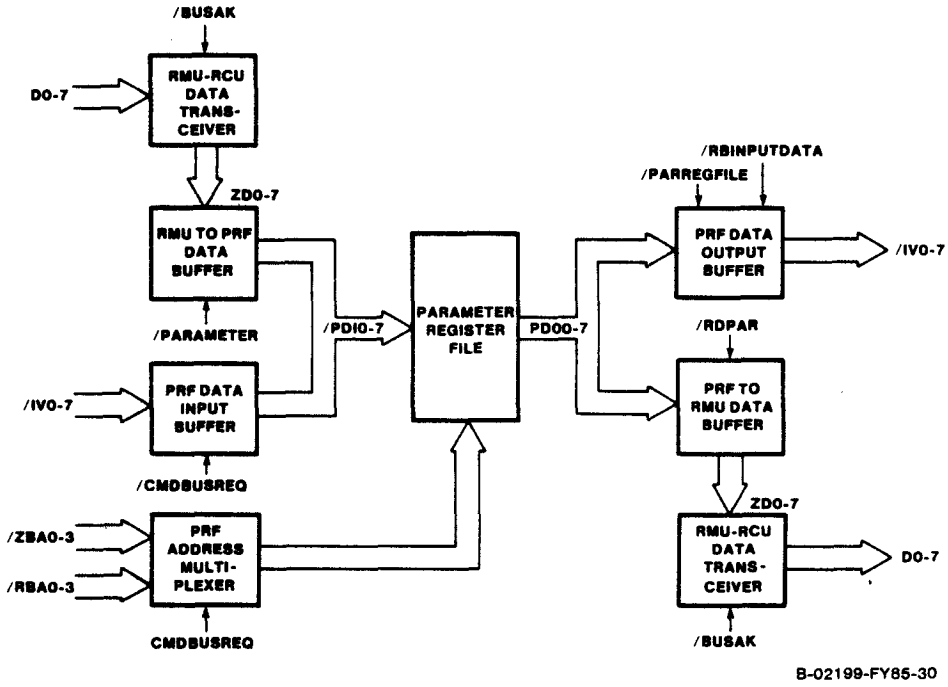

FIGURE 3.6-3
Parameter Register File Block Diagram.

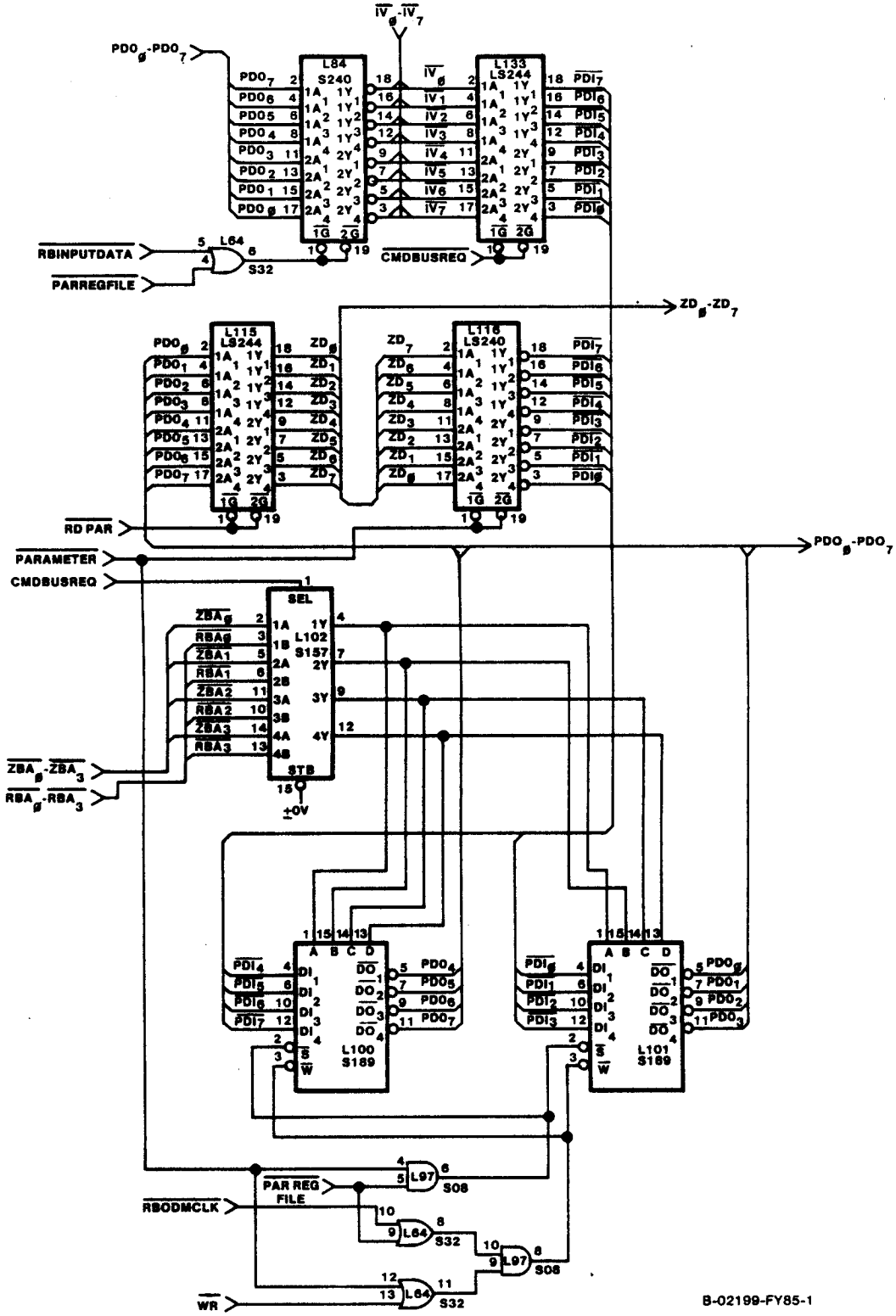

FIGURE 3.6-4
Parameter Register File Logic

The direction of data flow in the PRF is determined by the condition of the &RBODMCLK (&RBOUTPUTDATA synchronized with &MCLK) signal on L64 pin 10. The Microcontroller activates &RBODMCLK during write operations and deactivates it during read operations. Since &PARREGFILE is low on pin 9 of L64, an active &RBODMCLK signal will drive L97 pin 10 low. Since pin 9 of L97 will be high (&WR and &PARAMETER are active at L64 only during Z80A PRF write operations), &RBODMCLK forces the pin 8 output of L97 low. The low output of L97 is directly asserted to the write control pins (pins 3) of the PRF chips (L100 and L101) to specify a write operation. If an inactive &RBODMCLK signal asserts L64 pin 10, &RBODMCLK is gated through L64 and L97 in the same way to drive the PRF's write pins high and, therefore, place the PRF in the read direction.

During Microcontroller-controlled PRF write operations, data sent from the Microcontroller to the PRF is buffered from the &IV bus onto the PRF Data Input (&PDI0-7) bus via L133, the PRF Data Input Buffer. L133 is enabled by an active Command Bus Request (&CMDBUSREQ) signal, which is active whenever the Microcontroller receives a command from the RMU board. The data on the &PDI0-7 bus is sent directly into the PRF and placed in a location determined by the addresses supplied via PRF Address Multiplexer L102. When the Microcontroller is accessing the PRF, the address multiplexer passes the &RBA addresses through (due to the active CMDBUSREQ signal on pin 1). Address bits &RBA0-3 are supplied by the Microcontroller via the &IV bus and Right Bank Address Latch L85.

During Microcontroller-controlled PRF read operations, data sent to the scratchpad or the Microcontroller is moved from the PRF onto the PRF Data Output bus (&PDO0-7, eight bits). The data to be read is addressed the same way as data written to the PRF by the Microcontroller. Data sent out of the PRF on the &PDO0-7 bus travels through PRF Data Output Buffer L84 and onto the &IV bus. L84 is enabled when the &PARREGFILE and Right Bank Input Data (&RBINPUTDATA) signals are active on L64 pins 4 and 5. (&RBINPUTDATA is active whenever the Microcontroller is reading data.) Data from the PRF on the &IV bus is then read into the Microcontroller (via L69); it can then be written into the scratchpad under Microcontroller control.

3.6.7 RMU Accesses the PRF

The hardware which passes data between the RMU and the PRF resides on the RCU board. The Z80A issues commands to the Microcontroller via the Z80A data bus (D0-7). Data on this bus moves between the RMU and RCU boards via RMU-RCU Data Transceiver L149. PRF read or write operation control commands, and the addresses needed for the operations, are sent to the RCU via the Z80A address bus (A0-7). Z80A address bus bits are received on the RCU board by Z80A I/O Decoder L98 and Z80A Address Bus Buffer L99. L98 decodes address bits A4-7 into one of four I/O commands. Address bits A0-3 are passed through L99 to create the Z80A inverted buffered address bus (&ZBA0-3).

Z80A I/O Decoder L98 generates the Parameter Register File Select Read or Write (&PARAMETER) signal from pin 3 to perform any PRF read or write operation. L98 generates &PARAMETER in response to an active &MMI/O signal asserting pin 12 (via L96) and RMU addresses on the A0-7 bus in the FF20-FF2F range. The active &PARAMETER signal is gated with an active or inactive &RD signal at L96 to create either an active or inactive Z80A Read Parameter Register File (&RDPAR) signal from pin 3. During a Z80A-controlled PRF read or write operation, RMU-RCU Data Transceiver L149 is enabled by the inactive Bus Acknowledge signal (BUSAK, which is active only if the Microcontroller has PRF control) on pin 19. The direction of data flow through RMU-RCU Data Transceiver L149 is determined by the state of the &RDPAR signal.

Since the &STATUS signal on L97 pin 1 is high during PRF operations, the condition of the &RDPAR signal determines the output of L97 and, therefore, determines the input of RMU-RCU Data Transceiver Direction Control Flipflop L111. The output on pin 5 of L111 is the synchronized (&8MHZ clock) result of the active or inactive &RDPAR signal that asserts L111's D input. The active &RDPAR signal generates a low signal from L111 to place RMU-RCU Data Transceiver L149 in the read, or B-to-A, direction; an inactive &RDPAR signal generates a high signal from L111, placing L149 in the write, or A-to-B, direction.

The PRF chips' read/write direction is determined by the condition of the Z80A Write Request (&WR) signal when &PARAMETER is active. The active &PARAMETER signal asserts L64 pin 13, allowing the &WR signal to control the output of L64 during PRF read or write operations. During PRF write operations the active &WR signal is gated through L64 to assert pin 9 of L97. Since pin 10 of L97 is high due to an inactive &PARREGFILE signal (which is active only when the Microcontroller accesses the PRF), the active &WR signal drives the output of L97 low. The low output of L97 directly asserts the write control pins (pins 3) of the PRF chips (L100 and L101) to specify a

write operation. If an inactive &WR signal is asserting L64 pin 13, then &WR is gated through L64 and L97 in the same way to drive the PRF's write pins high and, therefore, place the PRF in the read direction.

During an RMU-to-PRF operation (ie, a PRF write operation), data sent to the PRF is placed on the Z80A data bus (D0-7). Data from the RMU is moved to the RCU, and then buffered through the enabled RMU-RCU Data Transceiver (L149) and onto the Z80A buffered data bus (&ZD0-7). Data from the ZD0-7 bus is buffered onto the Parameter Register File Data Input (PDI0-7) bus through the enabled (by the active &PARAMETER signal) RMU to PRF Data Buffer (L116). The data is then placed into the PRF according to the address supplied by Address Multiplexer L102. Due to the inactive Command Bus Request (CMDBUSREQ) signal on pin 1 of L102, address bits &ZBA0-3 are passed to the PRF. Z80A Address Bus Buffer L99 supplies address bits &ZBA0-3 as the inverted, buffered results of Z80A address bits A0-3.

During a PRF-to-RMU operation (ie, a PRF read operation), data sent to the RMU is moved out of the PRF and onto the Parameter Register File Data Output (PDO0-7) bus to assert the inputs of the PRF to RMU Data Buffer (L115). When enabled by the active &RDPAR signal, L115 places the data onto the ZD0-7 bus. Outgoing data from ZD0-7 passes through RMU-RCU Data Transceiver L149 (when the transceiver is properly enabled) and onto the Z80A data bus (D0-7). The data from the PRF is then available to the Z80A on the RMU board.

SECTION 3 QUIZ

1) What is the 4K x 8 data buffer used for?

2) What function does the right bank perform?

3) The SRF and the PRF are used in communicating between what two devices?

4) What six functions are performed when the RCU receives a non-immediate command?

5) What is unconventional about the 8X305 addressing?

6) What does the 8X305 Microcontroller use the 256 x 8 bytes of scratch pad memory for?

7) During what part of the instruction cycle does the 8X305 check for the HALT signal?

8) How does the microcontroller determine what size of Winchester is installed?

9) What information does the microcontroller obtain from the Winchester status register?

10) How many sectors are there per track for a 10 Meg Winchester?

SECTION 4
INTERNAL WORKSTATION CONTROLLER (IWS)

SECTION 4

Internal Workstation Controller (IWS)

The primary responsibility of the Internal Workstation Controller (IWS) is to decode and execute the software that is DMA'ed into its Main memory by the system, react to the information it receives from the keyboard, update the display on the CRT, and the control memory, control the loading of the font memory and provide an interface to the system through the 50BUS.

The major components that make up the IWS are:

1. A 4Mhz Z80A Microprocessor.
2. A 8031 Microprocessor for keyboard control.
3. 64K of Dynamic RAM with parity.
4. 4K X 8 of static RAM for Control storage.
5. 4K X 8 of static RAM for Character storage.
6. Two 4K X 10 banks of static RAM allowing for two soft locatable font stores, capable of supporting a full matrix video scheme.
7. 2632 Collective Gate Array.
8. Differential TTL Video Driver Circuits to interface to the P.C. monitor.
9. Serial Keyboard Interface Logic.
10. Support of Device Type Switches, (Master In07, Slave In07, 08).
11. OIS 40/50/60 Parallel Bus Interface Logic.

FIGURE 4-1 shows a simplified block diagram of the IWS Controller. The logic of the IWS can be divided into six parts:

4.1 The CPU and Support Logic.
4.2 Main Memory and Control Logic.
4.3 Display Memory and Control Logic.
4.4 Display Timing Logic.
4.5 Keyboard Interface Logic.
4.6 OIS 40/50/60 Bus Interface Logic.

As each of the parts of the IWS are described you should refer to the Figures and diagrams that are provided, or you may refer to the schematics in Appendix E.

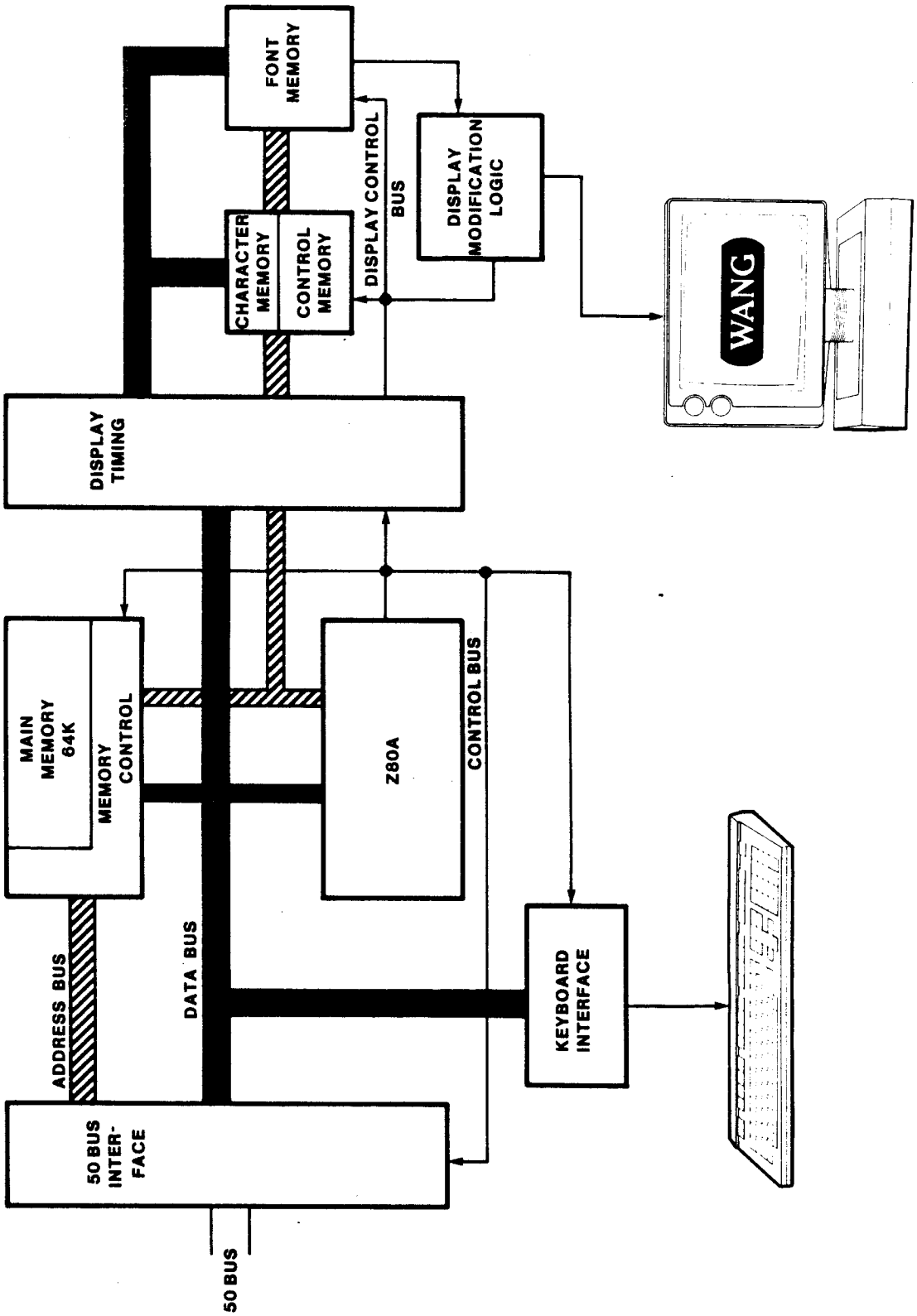

FIGURE 4-1
Internal Workstation Controller (IWS)
Block Diagram

Initialization

When the OIS 40/50/60 CPU enclosure is powered on, the controllers that reside within the CPU box will receive a power on system reset pulse from the Resource Management Unit (RMU). This reset pulse (MRC-n) is distributed over the 50BUS. When a device such as the IWS receives this reset pulse it will force the IWS CPU (Z80A) to be initialized and start executing code from location X'0000'. The data bus through hardware, will be forced to have X'00', which to the Z80A is interpreted as a NOP operation. The zero data value was applied to the data bus by the NOP generator logic. The NOP generator logic essentially holds the character memory output latches cleared, which in turn will force zeros onto the Z80A data bus. Since the Z80A is executing NOP's, which are continuous M1 opcode fetch cycles, the dynamic main memory of the device is constantly being refreshed from the M1 refresh cycle. The output of the NOP generator is passed to the master IN 07 status register, where it is use to inhibit main memory reads, and append the not running status bit.

After the RCU/RMU have determined that the device is in need of IPLing the RCU will down-load a jump to location zero code to the device. This instruction will reside at location zero of the devices main memory. Then the RCU will issue a device restart command the IWS will decode it and generate a controller reset, and disable the NOP generator. The reset controller signal will cause the Z80A to start executing code from location zero, which has the down-loaded jump to zero instruction, thus causing the Z80A to remain in a tight loop. When the NOP generator was disabled it cleared the not running status bit in the master IN 07 register. The RCU can now down-load program code through DMA transfers by the 50BUS. Once the IPL code has been loaded into main memory the RCU will issue another restart command, causing the IWS's Z80A to start executing the new code.

NOP Generation

The NOP (No Operation) opcode of the Z80A consists of Hex 00. The hardware that generates this instruction is quit simple. When power is first applied to the IWS controller board flipflop L152 (3E3) is set. This generates &PWRST (Power Reset) which is sent to the gate array (L2) (2H12). When the gate array receives &PWRST it will generate NR (Not Ready) from pin 31. NR is buffered and inverted by L17 and L18 and then applied to pin 5 of NAND gate L67 (2D7). The resulting high out from L67 will clear the Character Output Latch L35 and L36 (2B-D5). The high that cleared L35 and L36 was also inverted by NOR gate L68 (2C7) which then enabled the M output control pins of L35 and L36. The N output control pins of L35 and L36 are then activated by the inactive BUSAK (Bus acknowledge). BUSAK is only active when the RCU is accessing the IWS Main memory. With both the output control line active L35 and L36 will place all zeros on the data bus for the Z80A to read as a NOP instruction.

4.1 The CPU and Support Logic.

The Z80A and its support logic for the Internal Workstation Controller (IWS) is similar to that of the Resource Management Unit (RMU). Since the IWS and the RMU employ a Z80A and 64K bytes of main memory the overall operation of these parts of the unit are therefore the same. There are a few differences and they will be pointed out as each section is discussed. As for the most part the circuits that are the same will be discussed very briefly so as to not bore you with repeated details. You may want to refer back to the appropriate section of the RMU description if you feel that you need further explanation of a given section.

4.1.1 Clock Generation

Y1 generates the 16-MHz base timing signal (MCK) from which the clock generation circuitry (L43 (1I14) and L15 (1I12/10), shown in FIGURE 4.1-2)) creates all other clock signals used on the IWS board. L16 gates the 16-MHz signal that synchronizes the generation of Z80A Data Bus direction control signals and the RAS signal. L43 gate 1 divides the 16-MHz signal to create the 8-MHz 1/2 Phi-Z and &1/2 Phi-Z signals that drive the RAS and CAS circuits. L15 gates 1&2 generates the &Phi-B signal used for main memory sequencer logic, also L15 gates 1&2 generate the 4 Mhz clock for the Z80A processor. FIGURE 4.1-1 illustrates the relationship of the various clocking signals, while FIGURE 4.1-2 shows the logic involved.

4.1.2 Z80A Control Inputs

4.1.2.1 &BUSRQ

The Z80A on the IWS can be halted momentarily by activating the &ZBUSRQ (Z Bus Request) signal on pin 25 of the processor. &ZBUSRQ is activated be the RCU through the combination of 50BSLCT (50BUS SELECT) and &50BUSRQ (50BUS REQUEST). These two signals are gated through L155 and L153 (3A12) to generate &ZBUSRQ, thus causing the Z80A to suspend its operation and allow the RCU to take control of its busses. Once the Z80A receives a BUSRQ it will complete the operation that is in progress and then suspend its operations. It will then acknowledge the request by activating pin 23 (&BUSAK) causing the Control, Data, and Address Bus Driver to tri-state themselves. After the RCU has completed its operation using the IWS's bus it will remove the request, hence allowing the Z80A to continue its operation.

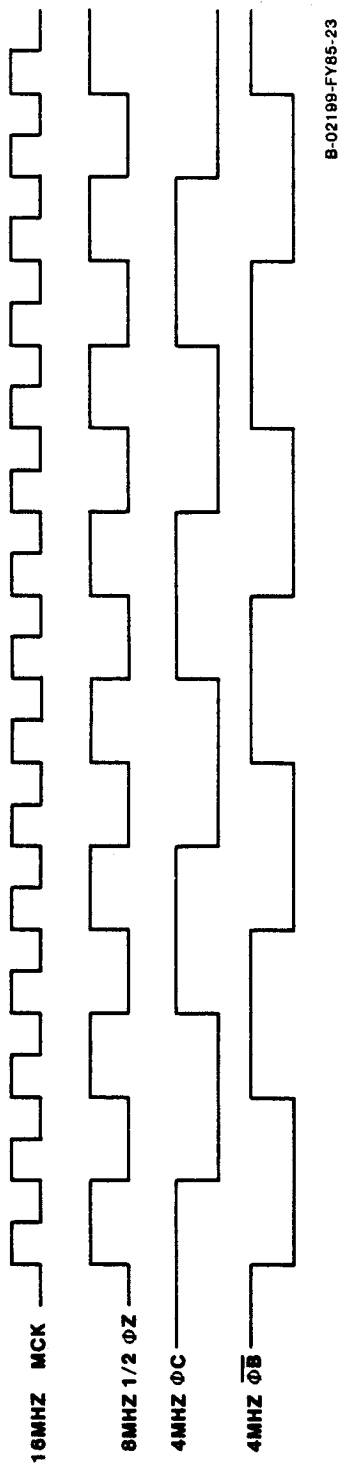

FIGURE 4.1-1
Clock Timing Diagram

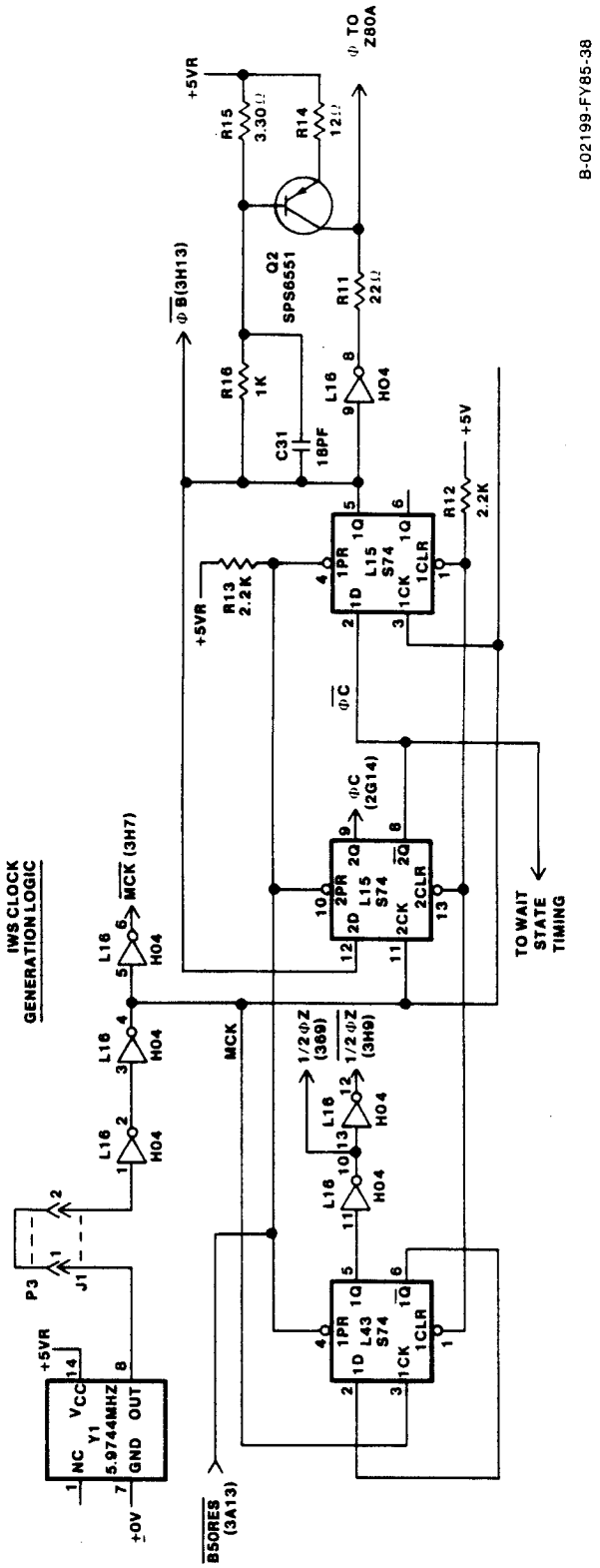

FIGURE 4.1-2
Clock Logic

4.1.2.2 Interrupts

The Z80A can be interrupted by a non-maskable interrupt (NMI) request arriving on pin 17 or by a maskable interrupt asserting pin 16. The only non-maskable interrupt that can be generated is from the parity circuits. Parity is checked on all data transferred to or from main memory. Further information on when and how parity is checked can be found in Section 4.2.3. A maskable interrupt can be requested by the 8031 receiving information from the keyboard. The generation of the keyboard interrupt will be discussed in Section 4.5.?.

4.1.2.3 Wait

Wait states are inserted into the Z80A machine cycle during accesses to the CRT memory or the Font memory. These wait states are added to synchronize the Z80A with the WL2632. The WL2632 is constantly updating the CRT display with information from the CRT memory and Font memory. These wait states are inserted whenever pin 24 of the Z80A is driven low by &CWAIT.

With these conditions in mind let's look at FIGURE 4.1-3 and see what happens. Gate L53 (1G14) pin 6 will go low if BFS (Buffered Font Select) is high at the same time that BA14 and BA15 are high. Also L53 pin 8 will go low if BCOMM (Buffered Command) is high at the same time that BA14 and BA15 are high. If either one of these two output are driven low they will force gate L61 pin 11 (1G14) to drive low. This low is gated with BUSAK (Bus Acknowledge) through L110 to drive the "D" input of L99 (1F13). Then when the Z80A activates &AMREQ (Advance Memory Request) &CWAIT will be generated causing the Z80A to enter into a WAIT condition. The Z80A will remain in this state until the Display Timing logic, consisting of L98 and L99, generates the proper enabling signals, thus synchronizing the Z80A with the Display circuits.

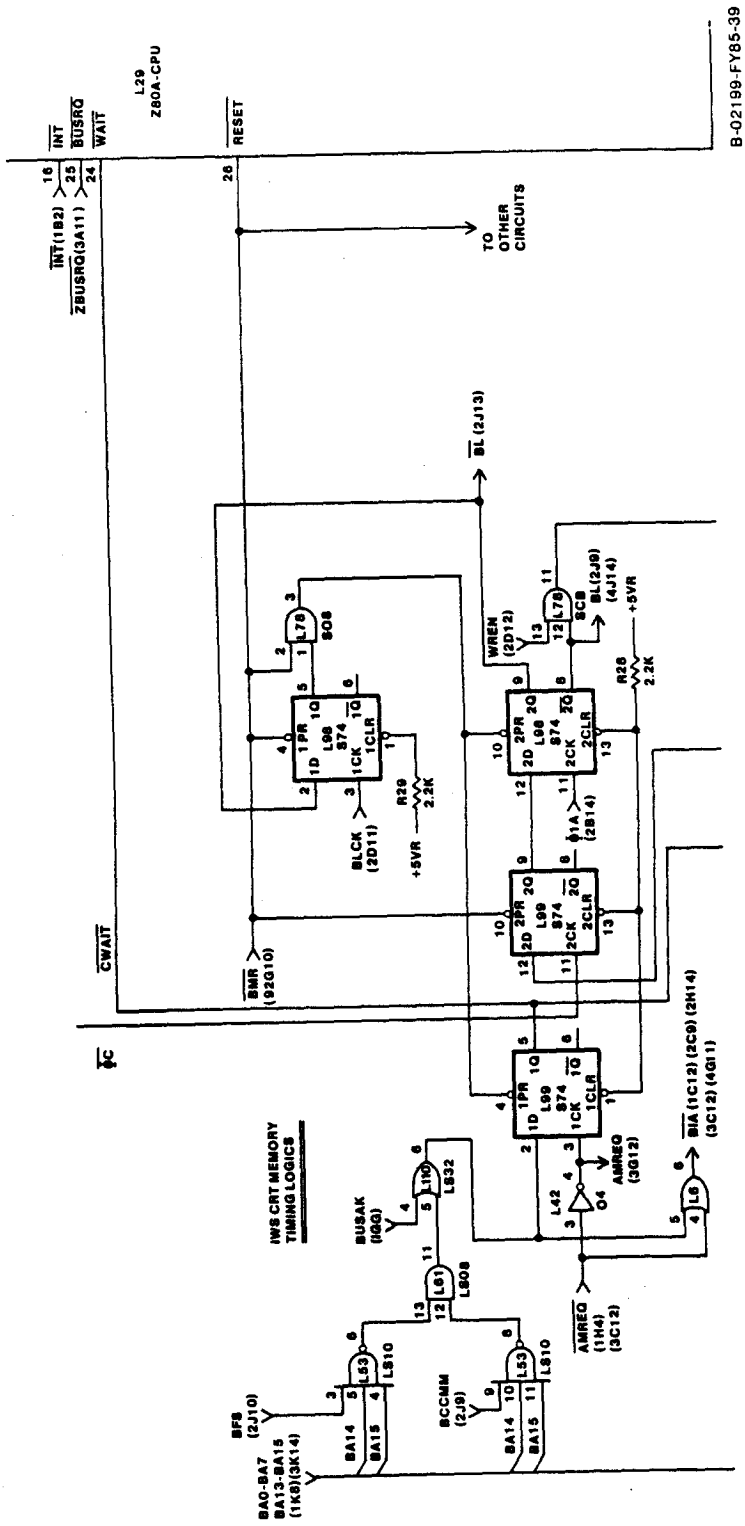

FIGURE 4.1-3
Wait State Timing Logic

4.1.3 Control Outputs

The Z80A control outputs are supplied to L14 (1G6), the Control Line Driver, When the inactive &BUSAK signal enables the driver allowing the control signals to pass onto the Control Bus. The &BUSAK signal is inactive whenever the Z80A has control of the Busses.

When the RCU wishes to transfer information to or from the IWS main memory it will activate the &ZBUSRQ (Z Bus Request) signal. The Z80A will then activate &BUSAK disabling the Bus drives and the Data transceiver. When the Control Bus Drive is deactivated (its output tri-stated) the RCU can then use the BRD (Buffered Read) signal to indicate the direction of travel. This means that &BRD can be generated from two location, one form the Z80A through the Control Bus Driver and two from L156 (3A13) the 50BUS Buffer. When &BRD is low data will be read from memory and when &BRD is high data will be written to memory.

4.1.4 Address Bus

Address lines form the Z80A are supplied to L28 (1J6) and L13 (1I6). L28 drives the lower byte of the address and L13 drives the upper byte. When the inactive &BUSAK signal asserts pins 1 and 19 of L28 the lower byte of the address can be place on the Bus. &BUSAK also asserts the output control pin of L13 to allow it to place the high address on the bus. During I/O operation only the lower byte of the address is placed on the Bus for decoding of the I/O operation, but during a normal read or write operation to any of the memories, both bytes of the address will be placed on the bus by the active &AMREQ signal.

4.1.5 Data Bus

Data line to and from the Z80A pass through L41 (1F6) Data Transceiver, which produces outgoing data or accepts incoming data depending on the the enable and direction control inputs. The direction of travel through L41 is determined by Data Transceiver Control Flipflop L43 (1D8), which insures that the transceiver is stable throughout the transfer operation.

4.1.6 MMI/O Decoders

The Z80A can communicate to other devices through MMI/O locations. Three decoder chips are use to select the device that the Z80A wishes to communicate to. L55 (1J2) and L96 (1D11) decode all the OUT location, while L52 (1H2) decodes all the IN locations. The decoding logic use here is standard in most Z80A based system so a detailed description of its operation is not necessary. Table 4.1.1 give a complete list of each MMI/O location and its use. For further information on the operation of an individual MMI/O operation refer to the appropriate section for that function.

Table 4.1.1 MMI/O COMMANDS

MMI/O LOCATION IN HEX	DESCRIPTION
OUT 0	Sounds Keyboard Clicker
OUT 1	Sounds Keyboard Speaker
OUT 2	Set CRT Horizontal Scroll. Data sent must be in the range of 00H to 50H.
OUT 5	Selects whether the top 16K of memory is CRT, Main RAM memory, or Font memory. Data — Select 00H — CRT Memory 01H — Main Memory 02H — Font Memory
	NOTE: The lower 48K of Main Memory is not affected by this operation.

Table 4.1.1 MMI/O COMMANDS (cont.)

MMI/O LOCATION	DESCRIPTION
OUT 6	Selects Primary Character Set
OUT 7	Selects Secondary Character Set
OUT 9	Selects either Normal or Inverse Video depending on the condition of D7. D7=1 Selects Inverse Video D7=0 Selects Normal Video
OUT E	Diagnostic Parity Checking D0=0 Sets all Memory Writes to Correct Parity D0=1 Set all Memory Writes to Wrong Parity D1=0 Insures that CPU will not stop when a Parity Error occurs. D1=1 Insures that CPU will stop when a Parity Error occurs.
OUT 20	Character Set Selection D0=0 Selects a 256 Character Set for Font Memory. D0=1 Selects a 128 Character Set for Font Memory.
OUT 25	Serial Keyboard Function Control Data can be from 00H to FFH.
IN 0	Keystroke Data; K0 - K6 and Shift K0 - LSB Shift - MSB
IN 7	Switch Bank Used to Define Device Type SW1 - LSB SW8 - MSB
IN 8	Switch Bank Used to Define Device Type SW1 - LSB SW8 - MSB

4.2 Main Memory and Control Logic

The Internal Workstation Controller contains 64K byte of Dynamic RAM that services as Main memory. It also contains three other memories that can be overlaid into the upper 16K area of the Main memory. These other memories can be switched in or out through MMI/O operations. The Main memory is the only memory that the RCU has access to for DMA operation. Once the RCU transfers data into the Main memory then the Z80A can move the data into either the Control, Character or Font memory as needed. The Main memory is the only memory of the four that contains parity, and since it is Dynamic it must also be refreshed so as to retain its integrity. In this section we will discuss addressing, refresh, parity and data transfers for Main memory.

4.2.1 Addressing Main Memory

Addresses for Main memory is done through the row and column technique. The Z80A will place the address of the location that it wishes to direct the information on the address bus through the Address Drivers L28 and L13 (1I/J6). Then the Z80A will activate &MREQ and either the &WR or &RD control signals.

The address on the bus will be placed onto the inputs of the Address Multiplexers L113 & L114 (3I/J14). These multiplexer splits the address into Row addresses and Column addresses where the low byte is the Row address and the high byte is the Column address. The SEL input of the multiplexers are driven by SWMUX. When SWMUX is low the Row address is transferred to the memory chips, and when SWMUX is high the Column address is transferred.

4.2.1.1 RAS/CAS Generation

The RAS/CAS generation circuits for the IWS are similar to those of any other Z80A based device. The general idea is that the RAS (Row address) signal will be developed first, then the SWMUX will change states followed by the generation of CAS. To introduce a little bit of complexity to the circuit the Z80A throws in a refresh cycle at the end of the M1 machine cycle, this refresh cycle also uses part of the RAS/CAS circuits to complete it job. To help you comprehend the sequence of events that are about to take place an example is provided. Refer to FIGURE 4.2-1

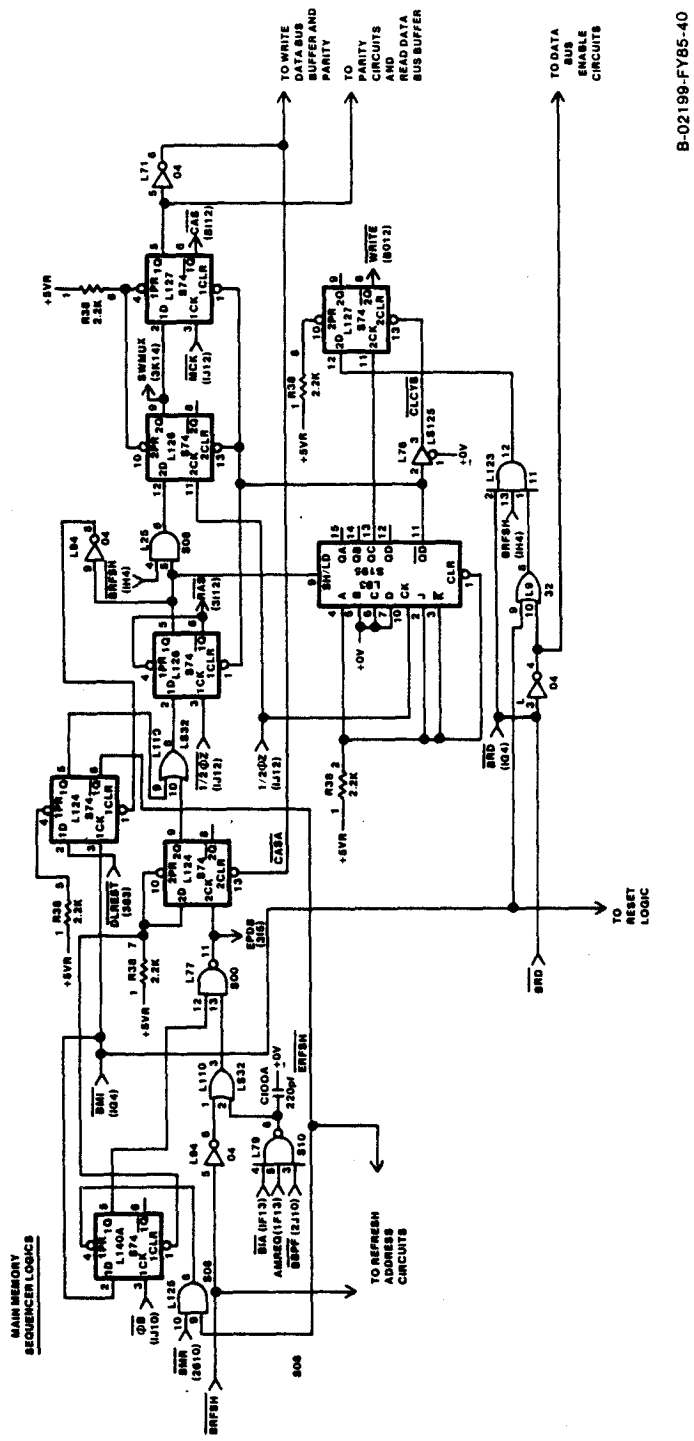

FIGURE 4.2-1
RAS/CAS Generating Logic

Let's take a typical instruction fetch. The Z80A places the address on the bus and activates &BRD, &BM1, and &AMREQ control signals. Active AMREQ will be gated through L73 (3G11) with deactive &BIA (Buffered I/O address) and &BBPF (Buffered Bad Parity Found). The low from L73 pin 6 will then be gates through L110 (1G11) and L77 (1G10) to clock the Memory Access Operation Pending Flipflop L124 gate 2 (1G9). L124 will set, placing a one on the "D" input of the RAS Generation Flipflop L126 gate 1 (1G8). At the next rising edge of &1/2 Phi Z clock L126 gate 1 will set, generating &RAS. On the next rising edge of 1/2 Phi Z clock L126 gate 2 will set, causing SWMUX to switch the address multiplexers from the Row address to the Column address. On the next rising edge of &MCK (16Mhz clock) L127 gate 1 will generate &CAS, thus allowing the Column address to enter the RAM. The generation of CAS will cause &CASA (CAS Acknowledge) to clear the Memory Access Operation Pending Flipflop L124 gate 2 (1G9), hence completing the operation.

At the end of M1 machine cycle the Z80A will generate &BRFSH (Refresh), which will be gated into pin 13 of L77 (3H10). At the same time that the Z80A asserts &BRFSH, it deactivates &BM1. This zero to one transition will clock L124 gate 1 (3H9). The 1D input of L124 will be high, thus the 1Q output will go high causing the RAS flipflop to be set on the next 1/2 Phi Z clock. The deactivation of BM1 also caused a logic 1 to be placed on Pin 12 of L77. Now both pin 12 and pin 13 are high causing a low out, thus preparing flipflop L124 gate 2 for the next memory access. Once the RAS flipflop was set it caused the refresh request flipflop L124 gate 1 to clear. Then on the next 1/2 Phi Z clock the RAS flipflop cleared. &BRFSH disqualified And gate L125 (3H8), thus interrupting the RAS/CAS cycle. Only a RAS cycle is needed for a refresh operation.

4.2.2 Data Transfers

Data transferring to and from Main memory must pass through Data Buffers L142 and L112 (3H2/3). L142 allows data to pass from the memory to the data bus, while L112 allows data to be transferred from the data bus to memory. All data transfers will take place after CAS has been generated. When data is to be read from the Main memory the Z80A will generate &RD and &AMREQ. &AMREQ will start the RAS/CAS cycle and &RD will be gated with EPDB (Enable Parity and Data Bits), that was generated by L77 (3G10) during the RAS/CAS cycle, through L106 (3I5), thus enabling L142's output control and L103 Parity gate.

Once CAS has been generated L127 1Q output will enable L142 thus allowing the data on it inputs to be clocked through to the Data Bus. During a write operation all the above procedure will take place except that this time &BRD will be deactivated, thus causing L112 to be enabled while dis-enabling L142. Also during the write operation L127 2Q will generate &WRITE to write enable the memory chips.

4.2.3 Parity Circuits

The parity checking and generation circuits are only functional on data going to or from Main memory. The Control, Character and Font memories do not have parity checking capabilities. A parity bit is generated for each byte of data written into Main memory and then when that byte is read out the parity is checked, thus insuring memory integrity. FIGURE 4.2-2 shows the parity circuits used in the IWS controller.

During a read operation the parity bit stored in L131 (3J5) is transferred through L128 (3G3) and L103 to generate PARE. L109 (3G2) will be in a tri-state condition so PARE will only be allowed to travel to inverter L75 pin 5 (1B11). L76 (1B11) will also be in a tri-state condition due to gates L77 & L79. PARE will be placed on pin 10 of L77 (1B10), which will be qualified by active &BRD and &AMREQ, thus allowing PARE to pass to pin 4 of L78. Pin 5 of L78 receives its signal from inactive &BFP (Buffered Forced Parity, used to force odd parity during diagnostic operations), hence allowing PARE to be use by L59 (1A12) the Parity Generator/Checker. If odd parity is detected pin 6 of L59 will go high and cause a non-maskable interrupt to occur.

When data is being written into memory, L59 checks the contents of the data bus and developes a parity bit representing even parity, which it send out on pin 5 through now active L76. Pin 6 of L76 generates PARE and sends it L109 (3G2) which is qualified by &PWR (Parity Write). Here it is presented to the input of the parity RAM for storage.

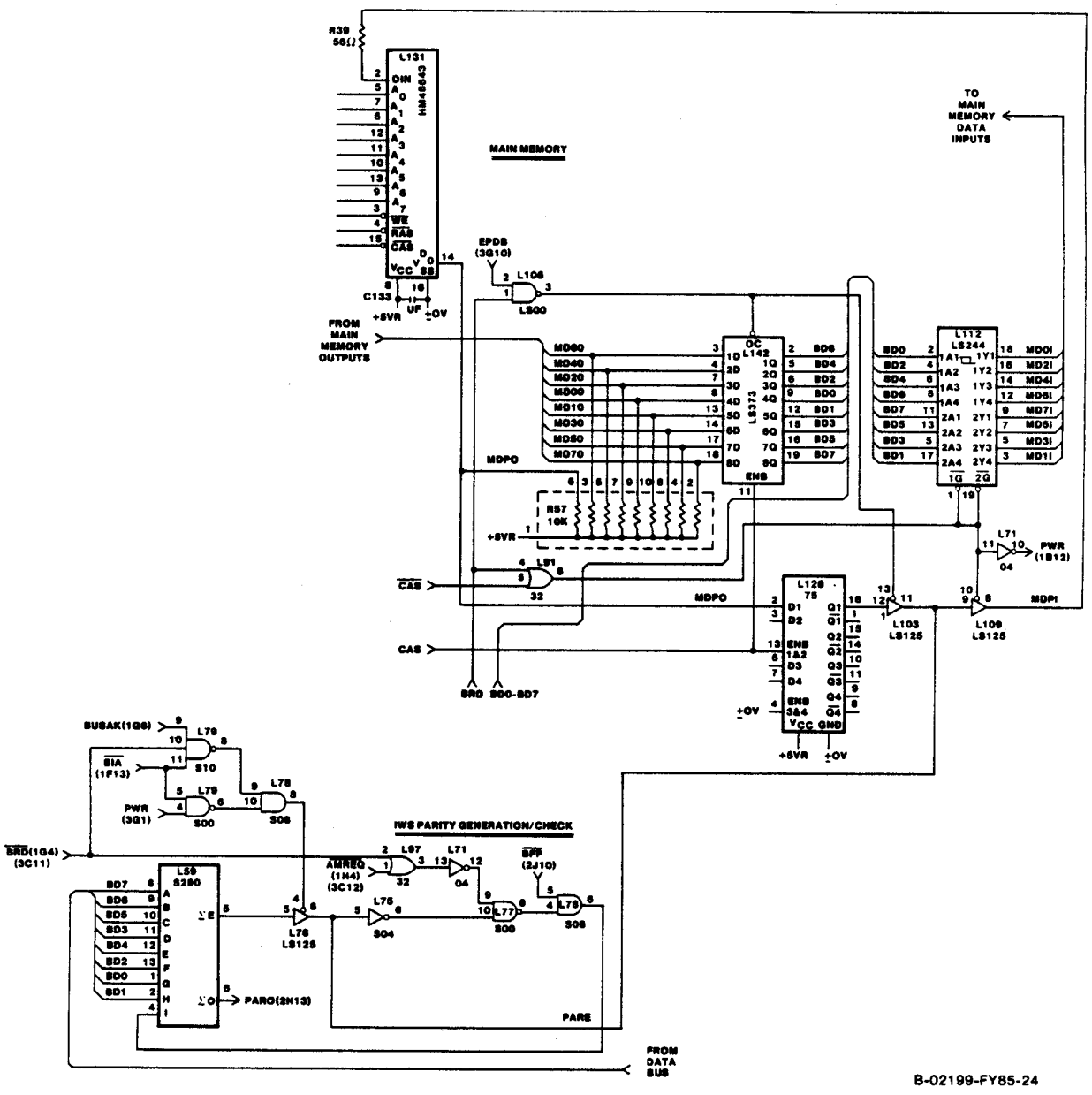

FIGURE 4.2-2
Parity Generating/Checking Logic

4.3 Display Memory and Control Logic

Before we get started let's take a look at the overall picture of how information is displayed on the CRT, and how the IWS controls the different memories associated with this operation. First there are three separate memories located on the IWS board, the Main memory, the CRT memory, and the Font memory.

The Main memory as you know is made up of 64K byte of Dynamic RAM. This memory is addressable by the Z80A directly, and by the RCU through DMA transfers. Both program and data information can be stored in Main memory.

The CRT memory is made up of four 2K x 8 static RAMs, for a total of 8K bytes of memory. This 8K of memory is divided into two separate parts, Control, and Character memory. The Character portion of the CRT memory contains the ASCII code of the character that is to be displayed on the CRT. The location in the Character memory that the ASCII code is stored represents the location that it will be displayed on the CRT. This representation of the location on the CRT screen that the character is to placed is determined by the upper byte of the address representing the row or line of the CRT, while the lower byte of the address represents the column within the row that the character is to be displayed. The ASCII code that is stored in the Character memory will be placed on the address bus of the FONT memory so as to determine what bit pattern should be displayed, (refer to the Font memory section for further information on Font memory addressing).

The Control portion of the CRT memory contains attributes of the character to be displayed. These attributes range from blinking to subscripts. Each attribute will be described later. The location within the Control memory that these attributes are stored will correspond to the location of the character that the attributes are effecting, i.e. if a CRT character is stored at location X700H in the Character memory then the attribute for that character will be stored at X700H in the Control memory. This data stored in the Control memory will be sent to the display modification logic, where it will effect the way the bit pattern is presented to the CRT circuits.

The Font memory is made up of four 2K x 8 and four 4K x 1 static RAMs, for a total of 8K x 10. This memory is also divided into two parts, Primary Font, and Secondary Font memory and each Font (Primary or Secondary) can represent either 128 or 256 characters. The data stored in the Font memory is the bit pattern for each character that is to be displayed on the CRT. When a character is to be displayed on the CRT the Character memory will transfer the ASCII code from the selected location in the character memory to the upper 7 bits of the address input of the Font memory. The lower four bits of the address will be made up of address information supplied by the Display Timing circuits. The combination of these two address inputs will select the proper bit pattern for the character to be displayed. This bit pattern will then be loaded into a parallel to serial shift register to be shifted out to the CRT one bit at a time. As each bit is shifted out to the CRT the attribute control from the control memory will determine how the bit should be displayed, i.e. high or low intensity, inverse or normal etc. Two separate set of fonts may be used by the system, but only one at a time. The selection of these different fonts is under software control.

The CRT memory and the Font memory are only accessible by the Z80A and the display timing and control logic, there is no DMA access to these memory locations.

Since the Z80A of the IWS can only access 64K of memory at any one time, and Main memory has 64K assigned to it already we must switch between Main memory and the other two memories. Only the upper 16K of Main memory is effected by this switching operation. When the Z80A desires to read or write information from or into either the CRT memory or the Font memory it will perform an OUT 05 instruction with the data being either a 0, 1, or 2, depending on which bank of memory is to be used. Table 4.3.1 shows the relationship between the data and the memory effected.

Table 4.3.1

DATA	MEMORY AREA
00	CRT AND 48K of Main Memory
01	All 64K of Main Memory
02	Font Memory and 48K of Main Memory

If either the CRT or the Font memory is selected, then when any access to a location that would of normally resided in the upper 16K of Main memory is performed, that access will be directed to the selected Display memory instead.

Since the Display Timing logic also has access to these two Display memories then we must supply some sort of contention circuits so that both the Z80A and the Display circuits do not try to access them at the same time. This process it controlled by the WL2632 Gate Array, which is the heart of the Display and timing logic and controls when information is sent to the CRT. It also controls when information can be entered into the display memories by the Z80A. When the Z80A tries to access a location within either the CRT or the Font memory the Display circuits will force the Z80A into wait states until they have completed moving data from the Character memory to the Font memory.

Now that you have the overall picture of the operation of the CRT display let's get into the meat of the operation and look at the circuits that make all this happen.

4.3.1 Character/Control Memory

The address of the information that is stored in either the Character memory or the Control memory is derived from the Z80A address bus or the Row/Column circuits of Display Timing. These two sources of address information are sent to a series of multiplexers. These multiplexers L125/126 (2H/I8) & L39/40 (2F/G8) select which set of addresses are presented to the memory chips. Each of the select inputs of these multiplexers are tied to the signal CBL. This signal is made up from two others. The first is BCOMM, which is active high whenever the CRT memory is selected by the Z80A. The second signal is BL, it is derived from the WAIT STATE GENERATOR. BL is generated at the end of the WAIT states so as to synchronize the Z80A with the display circuits. When both of these signals are high then the multiplexers will select the A inputs, (Z80A Address Bus). When the Z80A is not trying to access information in the CRT memory, either BL or BCOMM will be low, forcing the multiplexers to select the B inputs, which come from the display and timing circuits. Once the address is selected and presented to the memory chips the proper chip must be enabled.

Before I discuss how the chip selects are activated let's take a look at where the data stored in these memories comes from and where it may be sent to. For the Control memory the data within it effect the way the character is displayed on the CRT. This information is sent to the display modification circuits, it can also be read by the Z80A if needed. As for the Character memory the information stored within it is normally sent to the Font memory as an address, it too can be read from the Z80A. What I am getting at here is that there are two data busses coming from the CRT memory, one from the Character memory and one from the Control memory. This means that there must be separate buffer that control where and when the data is to be moved. When the Z80A reads the Character memory the data is moved to L35 & L36 (2B-D5) the Character Memory Output Latch. It will then be clocked into the latch, and at the proper time outputed to the Z80A data bus. The timing of this operation will be discussed in the section on CRT timing and control.

If the display circuits are reading the data in the Character memory, they will move the data from the memory chips to L37 (2H2) Character to Font Output Latch. The data will be clocked through L35 at the proper time determined by the Display Timing circuits. When the display circuits read the Character memory they also read the Control memory at the same time. This information is sent to L7 (2F1) the attribute decoder, and to the WL2632. Table 4.3.2 shows which attributes are decoded where, and Table 4.3.3 shows what bits in the attribute control byte control what function.

Table 4.3.2
Display Attribute Decoding

CHIP	ATTRIBUTE
L7. Decoder Chip	Extended Character Set Superscript Subscript Video (Inverse/Normal)
L2 WL2632	Intensity (Normal/High) Blink ON or OFF Cursor ON or OFF Underline

Table 4.3.3
Attribute Control Bits

BIT #	FUNCTION
D7	Intensity (1=high 0=low)
D6	Blink (1=on 0=off)
D5	Cursor (1=on 0=off)
D4	Underline (1=on 0=off)
D3	Extended Character Set (1=yes 0=no)
D2	Superscript (1=on 0=off)
D1	Subscript (1=on 0=off)
D0	Inverse Video (1=inverse 0=normal)

When the Z80A reads the control memory the data is moved to the inputs of L50 the Control Memory Output Latch. Then at the proper time the data is clocked through to the data bus for the Z80A to read. This concludes the reading of data from the CRT memory. Next let's look at how information is written into these memories.

Only the Z80A can write data into the CRT memories so it makes things a lot easier. Two buffers are used to transfer information from the data bus to the correct memory. L51 (2H4) the Character Memory Input Buffer passes data from the data bus to the Character memory when the enable inputs are activated by &WCHAR (Write Character Memory) which is decoded from the display timing and control logic and Z80A address information. L69 (2F4) the Control Memory Input Buffer passes data from the data bus to the Control memory when &WCNTL (Write Control Memory) which is also decoded from the display timing and control circuits and address information from the Z80A. Simple wasn't it.

Now back to the selection of the different memory chips. Because the data in the control memory controls the way a character in the Character memory is displayed, both the Control memory and the Character memory are selected at the same time. The Control memory and the Character memory are subdivided into two parts these parts are labeled upper and lower. Whenever the upper Control memory chip is selected we will also select the upper Character memory chip, and the same thing goes when we select the lower memory. Since the addresses for both the Control memory and the Character memory come from the same place, and we select both the Control memory and the Character memory at the same time we insure that the control byte and the character byte reside at corresponding location in the appropriate memory chip.

4.3.2 Font Memory

The display area on the CRT screen consists of 24 rows and 80 columns of characters. Each character that is displayed on the screen is made up of a 10 x 12 matrix or bit pattern. The character itself occupies an 8 x 8 portion of this matrix while cursor and underline information is displayed in a 10 x 2 areas of the matrix. Two blank dot columns allow for horizontal spacing while two blank lines at the bottom of the matrix allows for vertical spacing. FIGURE 4.3-1 shows the bit pattern of a character.

LINE #	COLUMN #	
	0 1 2 3 4 5 6 7 8 9	
F	0 0 0 0 0 0 0 0 0 0	0 represent blanks and 1 represent the area that the character will reside.
0	0 0 0 0 0 0 0 0 0 0	
1	0 0 1 1 1 1 1 1 1 1	
2	0 0 1 1 1 1 1 1 1 1	
3	0 0 1 1 1 1 1 1 1 1	
4	0 0 1 1 1 1 1 1 1 1	
5	0 0 1 1 1 1 1 1 1 1	
6	0 0 1 1 1 1 1 1 1 1	
7	0 0 1 1 1 1 1 1 1 1	
8	0 0 1 1 1 1 1 1 1 1	
9	0 0 0 0 0 0 0 0 0 0	
A	0 0 0 0 0 0 0 0 0 0	

FIGURE 4.3-1
FONT MATRIX

Each row in the matrix contains 10 bits, bits 2 through 9 resides in the main part of the font memory while the remaining two bits (0 and 1) reside in the secondary part of the Font memory. As each row of the CRT is scanned both parts of the Font memory are accessed simultaneously creating a ten bit word. This word is sent to the parallel to serial shift register and then to the CRT.

Each matrix will occupy 16 locations within the Font memory, and since there are 4096 locations in each of the two Font memories we can calculate that there are 256 matrixes in each, or a total of 512 between the two. To address 4K of memory it requires 12 address lines, the upper 8 lines are supplied by the character memory, (the ASCII code of the display character), which will select the matrix. The remaining four line of the address are supplied by the WL2632. These lower four lines will select the row or line within the matrix. If you refer back to FIGURE 4.3-1 you will see that the line number start at F and proceed to A. This sequence is produced by a counter

within the WL2632 chip, thus making this system compatible with other OIS system displays. These address lines are directed to the Font memory chip through multiplexers L85 (4G13), L104 (4H13), and L100 (4J13) which will select between the Z80A address bus (used for loading font data), and the display memory timing logic.

Only the IWS Z80A can write data into the Font memory, while both the Z80A and the display timing and control logic can read from it. When the Z80A is directed to write data to the Font memory it will first issue an OUT 05 with D=2, thus selecting the Font memory. Then the Z80A will write to a location with in the Font memory addresses by moving the data through L139 (4H7). During this operation the multiplexers L85, L104, and L100 will be selecting the Z80A address bus. The address will be decoded and the data sent to the proper chip. Since the Font memory is 10 bits wide the Z80A will have to perform two writes to complete the operation. When data is write into the secondary part of the Font memory only DB0 and DB1 will be used to transfer data. Reading data form the Font memory, by the Z80A, is also a two step operation, one read from the main part and one read from the secondary part. One point that you should keep in mind when the Z80A is transferring data to or from the Font memory is that the display timing and control logic is constantly using this memory to update the display. So whenever the Z80A wishes to access this memory it will be placed in a WAIT condition until the display circuits have completed there operation.

4.4 Display Timing

To help you understand the display operation let's take a look at what happens during the display of one line of characters on the screen. We will use the top line of the screen as our example.

Each line of characters displayed on the CRT screen requires that the electron beam travel across the screen twelve time, moving down one scan line for each pass. As this beam travels across the screen, dot information is feed to it causing it to either briten the spot on the screen or not. This dot information is generated from the Font memory which in turn receives its information from the CRT memory. When we start, the electron beam is at the upper left hand corner of the screen. A row counter in the WL2632 will be set to 0, indicating that we are at the first row of characters on the screen. Another counter call the Horizontal Scroll Counter is set to zero indicating that we are at the first character in the row. One more counter in the WL2632 called a line counter is also set to zero. This counter indicates that we are on the first line of the the current row. The combination of the Horizontal Scroll counter and the Row counter locate the ASCII code of the character to be displayed in the CRT memory. This code is sent to the Font memory along with the output of the line counter. These two locate in the Font memory the dot pattern for the given character and the given line within that character. This pattern is then dumped into a parallel to serial shift register. A clock pulse is applied to the shift register and the first dot of the first line of the first character is displayed. These clock pulses will continue shifting dots out until all ten dots of the first line of the first character are displayed. At this time the Column counter will be incremented by one. This will cause the CRT memory to move the ASCII code for the second character of the first row into the Font memory, where it will be dumped into the shift register for display. Ten more clock pulses will be applied and the process will again repeat. This process will continue until the Column counter reaches the 80^{th} count. At this time the line counter will be incremented by one and the Column counter will reset to zero. We are no looking at the second line of the first character in the first row. The process of moving the data from the CRT memory to the Font memory to the shift register and then to the screen will repeat. When the line counter finally reaches a count of 13 it will increment the row counter and reset both the Horizontal Scroll counter and itself. This completed the display of the first row of character on the screen.

At the end of each line the electron beam will be returned to the far left of the screen and lowered position. Then when the last character of the last row has been displayed the electron beam will be returned to the upper left hand corner to start the operation again. Now that you understand how data is displayed on the screen let's see what circuits are involved in making this operation happen.

Part of the timing for this operation is controlled by the WL2632 Gate Array. This array generates the row addresses and the line addresses along with several control signals. Table 4.4-1 shows the inputs and outputs of the array that effect the display operation.

Table 4.4-1
WL2632 Display Signals

Signal	Type	Function
R0 - R4	O	Row Address Counter output to the Character/Control memory.
LC0 - LC3	O	Line Counter output to the Font memory.
CCC	O	Column Counter Clear - this signal is used to clear the CRT column counter. It is generated when the row counter reaches counts 0 and 23 with the column timing counter reaching 99.
CCL	O	Column counter load. This signal is used to load the CRT column counter.
DT89	I	This clock is active at the end of each character display. The rising edge of DT89 is used internally by the gate array to generate specific timing relationships.
HS	O	Horizontal Sync. This signal controls when the electron returns to the left side of the screen.

Table 4.4-1
WL2632 Display Signals (cont.)

Signal	Type	Function
VS	O	Vertical Sync. This signal indicates when the electron been returns to the upper left corner of the screen.
PCS	O	Primary Character Set. When this signal is high it indicates that the Primary Character set is selected.
FS	O	Font Select. When this signal is high it indicates that the Font memory is selected by the Z80A.
HIC	O	High Intensity Control. When this signal is low the bit being displayed will be highlighted.
UC	O	Underline Control. When activated causes the character to be underlined.
BC	O	Blanking Control. Forces the screen to blank between characters and during horizontal and vertical retrace time.
CBC	O	Cursor Blinking Control. Controls the blinking of the cursor.
L8, L9	O	Lines 8 & 9. These signals indicate that the display is on the last two lines of the character so that underlining or cursor operation can take place.

External to the gate array we have a ring counter used for counting the dots within the bit pattern that is being displayed. This ring counter, comprised of L33 (2D13) and associated logic, will generate load and clock pulses for the display timing circuits. Also external to the gate array we have a column counter comprised of L72 and L73 (2B6-8). This counter can be loaded with an offset count if more than 80 columns are required in the display. Only 80 columns are visible on the CRT at any one time, thou the screen can be scrolled, so that up to 159 columns can be viewed. This offset is loaded into the column counter when the Z80A generates an OUT 02 instruction.

Referring to the timing diagram in FIGURE 4.4-1 we see the six signal that are developed by the ring counter. Three of these signals, LDT, DT89, and Phi 1A are used to control the timing of the display. The other three are used to control when the Z80A can transfer data to or from the CRT or Font memory. First let's look at the display memory signals.

The best place to start this explanation is when the shift register loads the bit pattern of the current character. This happens when LDT and DT89 are both high and the clock input to the shift register goes low, (Point 1). The shift register, when in the load mode is inhibited from shifting. On the next clock pulse LDT will go low and place the register back in the shift mode. &CK will then clock (shift) the bit pattern through the register and send it to the attribute insertion circuits, where the attribute will be appended to the bit and then sent to the CRT for display.

One clock pulse after LDT went low DT89 will go low, (Point 2). This transition will cause the next character's ASCII code to be read from the Character memory and placed on the address inputs of the Font memory. Then the next time that both DLT and DT89 are high (Point 3) this code will be loaded into the shift register and the process will start all over again. The falling edge of DT89 is also used to increment the column counter L72, and L73 (2B6-8), and generate timing signals inside the WL2632 gate array. From this point on these signals keep repeating themselves forever, at least until the power is turned off.

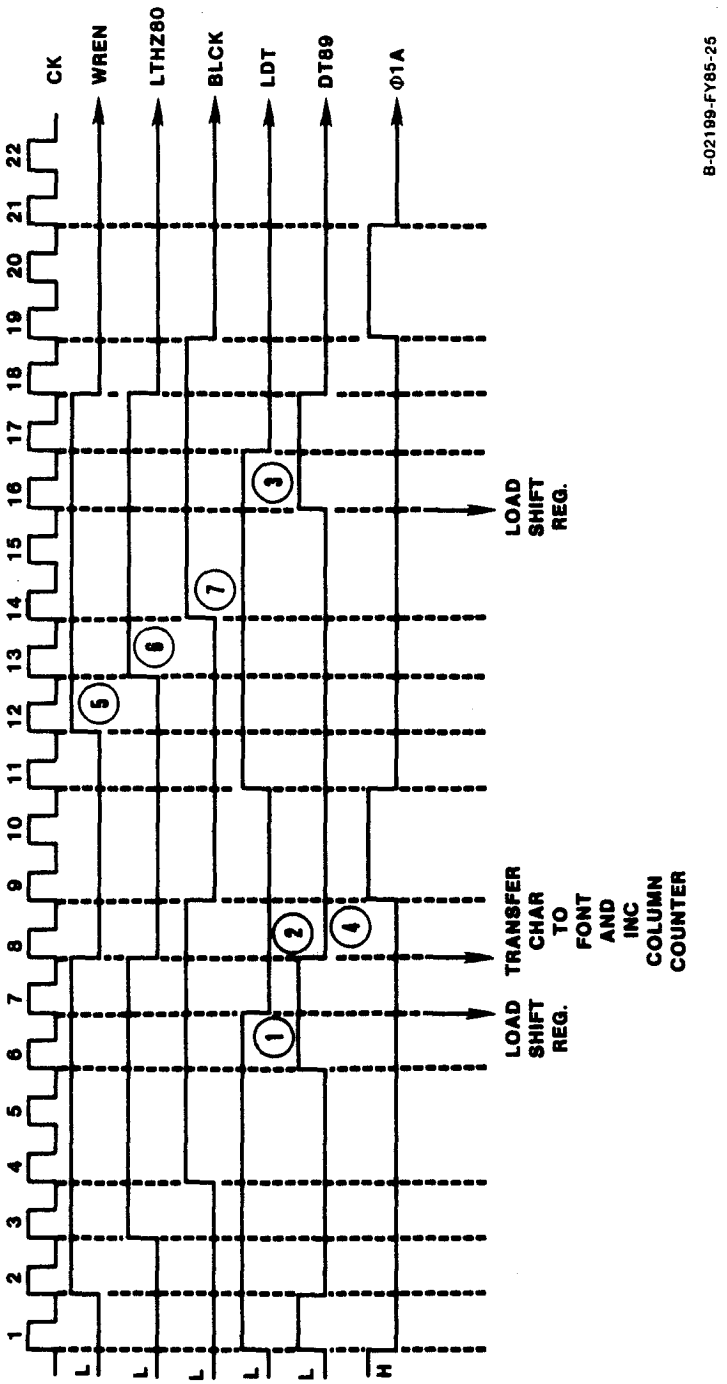

FIGURE 4.4-1
Display Timing

4.4.1 Display Memory Access

There are only certain times that the Z80A can access the display memories, so as to avoid conflict with the display timing logic. We will divided this operation into two section, Access to the CRT memory, and access to the Font memory.

4.4.1.1 Access to the CRT Memory

Before the Z80A can access the CRT memory it must overlay the upper 16K of Main memory with the CRT memory. This is accomplished by doing an OUT 05 instruction with D=0. The gate array will receive the OUT 5 and force BCOMM high and BFS low, indicating CRT memory is selected as an overlay. Next the Z80A will access the location within the CRT memory that it wishes to transfer data to or from. Address bits BA0 - BA12 are sent to the CRT memory address multiplexer where they will be used to select the location within the memory chips.

Address bits BA13 - BA15 are decoded to generate timing and control signal for the transfer. BA13 determines whether the Character memory or the Control memory will be selected. Gate L95 (1E13) pin 6 will generate &WCHAR (Write Character) when BA13 is high and the rest of its inputs are high, these input will be explained soon. Gate L95 (1D13) pin 8 will generate &WCHTL (Write Control) when BA13 is low. Address bits BA14 & BA15 are NANDed with BCOMM at L53 (1G14), these two address lines will be high when the Z80A is accessing the upper 16K of its range. When this happens L53s pin 8 will go low, this low will be ORed with the deactivated BUSAK (Bus Acknowledge) at L110 (1G13), this insures that it is the Z80A that is trying to access the upper part of memory. L110 will place a low on the "1D" input of flip-flop L99, and pin 5 or OR gate L60 (1F13). The Z80A will then activate &AMREQ and clock L99 through inverter L42. Plus it will generate BIA, this is use to indicate to the memory circuits that an address within a switched upper bank of memory has be selected. When L99 was clocked by &AMREQ the 1Q output places the Z80A in a WAIT state. Wait states are inserted here so that the access to the CRT memory can take place without conflicting with the Display circuits. The low from the 1Q output of L99 that placed the Z80A in WAIT states will be passed through L60 pins 10 to 8 (1D11) and placed on the 2D input of L99. This low will be transfers to the 2Q output on the next Phi C clock. Here it will wait until the ring counter generate PHI 1A (Point 4 in FIGURE 4.4-1). When PHi 1A goes high L98 gate 2 (1F11) will set, generating BL (Bank Load), which is ANDed with BCOMM at L61 (2J8). CBL will switch the CRT memory multiplexers from the Display circuits to the Z80A address bus, also CBL will be placed on And gate L21 (2B7) where it will wait for the ring counter to generate LTHZ80 (Load the Z80A), reference point 6 in

FIGURE 4.4-1. At this time data from the Character memory will be place in the Character memory output latch. If the Z80A had indicated that this operation was a read cycle then the output controls of the Character or control memory latches will be enabled.

Shortly after L98 &2Q output went high generating BL the ring counter produced WREN (Write Enable). BL and WREN are ANDed by L78 (1F10) to produce VCW (Video Circuit Write), which is gated with BWE (Buffered Write Enable), deactivated &BFS (Buffered Font Select), and of course BA13 to select either the Character memory or the Control memory to write to. To bring you up to date on what has happen so far let's review; The address of the desired location has been place on the multiplexers inputs, the multiplexers have been switched from the Display circuites to the Z80A address bus, &WCNTL or &WCHAR has write enabled the selected memory chips and respective buffers, and the Z80A has placed the data on the data bus for transfer. The operation is not complete though, for the Z80A is still in a Wait State and can not complete the machine cycle until the WAIT line go high. This will happen when the ring counter generates BLCK (Point 7 in FIGURE 4.4-1). BLCK will clock L98 (1G11) causing the 1Q output to go low which forces L99 gate 1 to set, thus removing the low from the WAIT input to the Z80A.

4.4.1.2 Access to the Font Memory

Z80A access to the Font memory is similar to that of accessing the CRT memory. First the Z80A must overlay the Font memory in the upper 16K of Main Memory instead of the CRT memory. Once again this is done with an OUT 05 instruction with D=2. Now the Z80A can move data from the Main Memory to the Font memory or from the Font memory to the Main Memory. Next the Z80A must select which Font memory it is accessing, primary or secondary. This is done with either an OUT 06 or an OUT 07. The OUT 06 will select the Primary area of the Font memory, while an OUT 07 will select the secondary area. Then the Z80A must select whether there will be 256 characters in the font or 128. This must be done now because if only 128 characters are selected then part of the Font memory is inaccessible to the Z80A or the Display Circuits. Selection of the number of character within a character set is accomplished by generating an OUT 20 instruction, with D=0 or D=1. If D=0 then 256 character per set are selected and if D=1 then 128 are selected.

Once the above selections have been made the Z80A can then access the Font memory. From this point on the operation is the same as for accessing the Character or Control memories. Meaning the the Z80A will once again be places in a WAIT state so that it can be synchronized with the Display circuits.

4.4.2 Display Modification Logic

The Display Modification Logic receive the attribute information from the Control memory for each character displayed on the screen. This information will then determine how the character will be displayed on the screen. Table 4.3.3 shows the different attributes and the appropriate bit within the control word that performs the selected operation. The control word is transferred from the Control memory to the Display modification logic at the trailing edge of DT98, the same time that the Character data is loaded into the shift register. Four bits of the control word are processed through the WL2632 gate array, while the other four bits are latched into L7 (2G1). Table 4.3.2 shows which attributes are controlled by the WL2632 and which are controlled by L7.

4.4.2.1 Normal Display Path

There are two signal lines that drive the CRT display. These two line control the intensity of the electron beam. If both lines are low then the beam will be turned off. When the NV (Normal Video) line is high while the INTN (Intense Video) is low the beam will be turned on at the normal brightness. And finally if both lines are high then the beam will be turned on at the highlighted brightness. Let's now follow the path of a single bit from where it leaves the shift register until it is presented to the CRT. For the first example we will use no attributes, so the dot on the screen will be displayed in its normal brightness and location.

Our display bit will be shifted out of L149 (4K7) on the one to zero transition of the clock. Let's assume that the bit is high, indicating that the spot on the screen should be light. This high will be placed on pin 5 of L116 (4F10), here it is NANDed with the inactive &BC (Blink Control). As long as &BC is inactive L116 will act as an inverter. So in this case the one from the shift register now becomes a zero, and is feed through And gate L115 to the 2D input of flipflop L147 (4F8), also this zero is placed on pin 12 of Nor gate L148 (4E9). The second input to L148 will be high at this time, thus forcing the 1D input of L147 to be low. Now on the next low to high transition of &CK both halves of L147 will assume the appropriate state. Gate 1 of L147 will reset causing the &1Q output to go high, thus forcing L148 pin 4 to output a low onto INTN. Gate 2 of L147 will set causing the &2Q output to go low. This low is inverted by L133 and placed on pin 10 of Exclusive OR L134 (4D11). Pin 9 of L134 will be high causing a low out. This low is placed on pin 8 of Nor gate L148 (4D8). Pin 9 of L148 will be low, as long as we are not scanning row 25 or above on the CRT. Two low to L148 will cause it to

output a high to the CRT circuits. This leaves we with a low on INTN and a high on NV thus producing a dot on the screen displayed at the normal brightness.

4.4.2.2 Intensity Control

Now that the path of flow has been established let's start adding attributes. First we will use high intensity. Bit 7 of the control word determine the intensity of the character. Bit 7 of the control word is detected by the WL2632 gate array. When this bit is high the array will activate the &HIC (High Intensity Control) output on pin 8. This signal will be gated through L20 (2I11) and L66 (2C3) to pin 10 of L115 (4E10). &HIC is then gated through L115 and L132 to L148. Here it qualifies L148 so that the data can act upon the 1D input of L147. Then as L147 is clocked the INTN line will reflect the high intensity condition.

4.4.2.3 Reverse Video

Reverse video can be selected two ways, the entire screen can be reversed or just a single character can be reversed. To reverse the entire screen the Z80A must perform a OUT 9 instruction with D=1. This will cause flipflop 1107 (4B14) gate 2 to set. When an individual character is to be reversed bit 0 of the control word is set. This generates BCRV which is placed on pin 13 of Exclusive OR gate L134 (4B13). The other input of L134 is from flipflop L107. As long as only one of L134s two inputs are high it will output a high. This high is inverted and placed on pin 6 Nor gate L133 (4D11). This low will be gated with the inactive &BC (Blank Control) and placed on pin 9 of Exclusive OR gate L134 (4D11). Pin 10 of L134 is the bit data going to NV. when a zero is on pin 9 of L134 any data presented to pin 10 will be inverted, thus causing the screen to display reverse video.

4.4.2.4 Underline Control

When a character is to be underlined bit 4 of the control word will be set. When this bit is set the gate array will activate pin 6 &UC (Underline Control). This signal is passed through buffer L12 (2I11) to latch L66 (2C2). Then when the character data is transferred to the shift register L66 will generate &UC, and place it on pin 1 of L132 (4E11). Now when the line counter in the gate array reaches line 9 of the current row &BL9 will go low. &BL9 and &UC will force L134 pin 8 to output a low causing L116 pin 8 to go high. This high is gate with the inactive &BC to produce a low from L116 pin 12.

As long as pin 12 of L116 is low data from the shift register can not pass through L115. In fact this low will insure that the dot on the screen that corresponds to this bit is brighten.

4.4.2.5 Cursor Control

To place the cursor on the screen the soft ware will set bit 5 of the control word that corresponds to the location of the cursor. When this bit is set the gate array will activate pin 5 and generate &BCBC (Cursor Blink Control). &BCBC is gated through L66 when the character data is loaded into the shift register. The resulting &CBC then travels to pin 12 of L132 (4E11). Since the cursor is made up of the two bottom line of a character, then whenever &BL8 or &BL9 are active L132 will present a zero to pin 9 of L115 and pin 9 and 10 of L116. L115 will pass the zero on through L132 pins 9 and 10 to L148, here it will act the same as when we did high intensity video, (remember the cursor is also displayed as a highlighted character). Going back to were L132 pin 11 outputed a zero to pins 9 and 10 of L116. The zero here will act the same as it did when we did underlining, forcing the dot to be displayed. The flashing of the cursor is controlled by L19 (2J14) a 555 timer. This timer runs at about a 30 Hz rate. The output of this timer is directed to the gate array where it is use to determine the blinking rate of the cursor. Whenever the output of the timer is high and bit five of the control word is set the cursor will be blanked, and whenever the timer output is low and bit 5 is high the cursor will be displayed.

4.4.2.6 Blink Control

It is possible to have a single character blink. This can be done by setting bit 6 of the control word that corresponds to the character that is to blink. When this bit is set, the gate array will activate pin 7 &BC (Blink Control) at a rate determined by L19 the 555 timer, this works on the same principle as the cursor blinking except that the gate array will now look for bit 6 of the control word to be set. &BC is gated through buffer L20, flipflop L31 (2C4) and latch L66. The resulting &BC signal will be directed to the display modification logic when the character to be blinked is loaded into the shift register. When &BC is active the character will be displayed as a blank.

4.4.2.7 Extended Character Set

We know that the system can switch between a primary and a secondary character set be generating an OUT 06 or OUT 07 instruction. Also we know that the system can have either a 128 byte or 256 byte character set. Sometimes more than 256 bytes for a character set is required, i.e. when using the system in international teletext word processing. If this extended character set is needed the system will first have to load the font memory with the additional font patterns and select a 256 character set, (this is done by the OUT 20 instruction with D=0). Then if a character is to be used from the extended character set that characters control word will have bit 3 set. When the display circuits transfer the ASCII code from the character memory to the font memory address inputs L7 (2G1) will activate CFS on pin 7. CFS will be Exclusive ORed with BPCS (Buffered Primary Character Select) by L134 (4H12). The output of L134 selects either the primary or the secondary Font memory. Normally this Exclusive OR gate will allow BPCS to pass through unaffected because CFS is then low. But when CFS is high L134 will invert the selection and cause the alternate Font memory to be selected. Since this operation is on an individual character basis, it in effect extendes the character set from 256 up to 512.

4.4.2.8 Superscript and Subscript

To either superscript or subscript a character on the CRT screen an offset is applied to the line counter of the display circuits. To help you understand this operation let's look at the way a Font for a character is stored in memory. FIGURE 4.4-2 shows the character matrix and the memory address for each byte within the matrix, and FIGURE 4.4-3 shows how the line counters output corr-risponds to the associated memory address.

The line counter is a 4 bit MOD 12 counter located in the gate array. As each line of a character is displayed the counter is incremented. The output from the counter selects the appropriate address in the matrix for the current line.

When superscript is selected an offset of two is added to the counters output. Normally the first two lines of a character is blank, so when superscript is selected these two lines are not displayed and the first line of the character is displayed in its place. Thus the character is displaced upward by two line.

ADDRESS	LINE COUNT	COLUMN #									
		0	1	2	3	4	5	6	7	8	9
F	LC0	0	0	0	0	0	0	0	0	0	0
0	LC1	0	0	0	0	0	0	0	0	0	0
1	LC2	0	0	1	1	1	1	1	1	1	1
2	LC3	0	0	1	1	1	1	1	1	1	1
3	LC4	0	0	1	1	1	1	1	1	1	1
4	LC5	0	0	1	1	1	1	1	1	1	1
5	LC6	0	0	1	1	1	1	1	1	1	1
6	LC7	0	0	1	1	1	1	1	1	1	1
7	LC8	0	0	1	1	1	1	1	1	1	1
8	LC9	0	0	1	1	1	1	1	1	1	1
9	LC10	0	0	0	0	0	0	0	0	0	0
A	LC11	0	0	0	0	0	0	0	0	0	0
B	X	0	0	0	0	0	0	0	0	0	0
C	X	0	0	0	0	0	0	0	0	0	0
D	X	0	0	0	0	0	0	0	0	0	0
E	X	0	0	0	0	0	0	0	0	0	0

0 represent blanks and 1 represent the area that the character will reside.

FIGURE 4.4-2
FONT MATRIX

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
LC1	LC2	LC3	LC4	LC5	LC6	LC7	LC8	LC9	LC10	LC11	X	X	X	X	LC0

FIGURE 4.4-3
Line Count to Address Relationship

When subscript is selected an offset of 14 is added to the line counter output. When the counter starts with an output of 0 plus the offset of 14 we access location 0D in the matrix. This causes the display to output two extra lines of blanks before it starts displaying the character, thus displacing the character downward by two lines.

The offset for both superscript and subscript is added to the line counters output by adder L44 (4E13). When superscript is selected OR L4 places a one on the B2 input of L44. The output of L44 will then be the sum of the line counter and the offset. If subscript is selected then the B2,B3 and B4 inputs of L44 are brought high, causing the addition of 14 to the line count.

4.5 Keyboard Interface

The keyboard of the IWS is interfaced to the Z80A through an 8031 microprocessor. The Z80A communicates to the 8031 through MMI/O operations and interrupts. When a keystroke has been detected the 8031 will generate an interrupt to the Z80A. Then the Z80A will perform a keyboard interrupt service routine and read the x/y data from the 8031 through an IN00 instruction. The Z80A can transfer data to the keyboard via the 8031 by using one of three OUT instructions. An OUT 00 will generate a click from the keyboard, while and OUT 01 will generate a beep. The Z80A can transfer a byte of data to the keyboard by performing an OUT 25 instruction.

4.5.1 The 8031 Microcontroller

The 8031 is a microprocessor in its own right, but for the purpose of this book and the OIS 40/50/60 system we can think of the 8031 as a sophisticated UART. Its full duplex serial ports allow us to send and receive data to or from the keyboard. The major features of the controller are:

1. 8 Bit CPU
2. On chip Oscillator and clock circuitry
3. 32 I/O lines
4. 64K address space for external data memory
5. 64K address space for external program memory
6. Two 16 bit timers/counters
7. A five source interrupt structure with two priority levels
8. Full duplex serial ports
9. Boolean processor
10. 128 bytes of onboard RAM

Referring to FIGURE 4.5-1 we see a block diagram of the 8031 controller. The four ports, P0-P3, provide the 8031 with a means of communicating with the outside world. Each of these ports are bidirectional, while some of them are multitasked. Along with the four ports are four control line that indicate to external circuitry what operation is taking place.

At power up time the 8031 self-configures itself as a UART by executing instructions in an external EPROM. Port 0 is a multitasked port, it provides the lower byte of the address for the EPROM and also acts as a data bus. Bits 0-3 of port 2 act as the upper part of the address for the EPROM while bits 4-7 are used as control functions. Port 1 is a bidirectional data bus between the 8031 and the Z80A. Finally port 3 serves as I/O port for directing the UART operations.

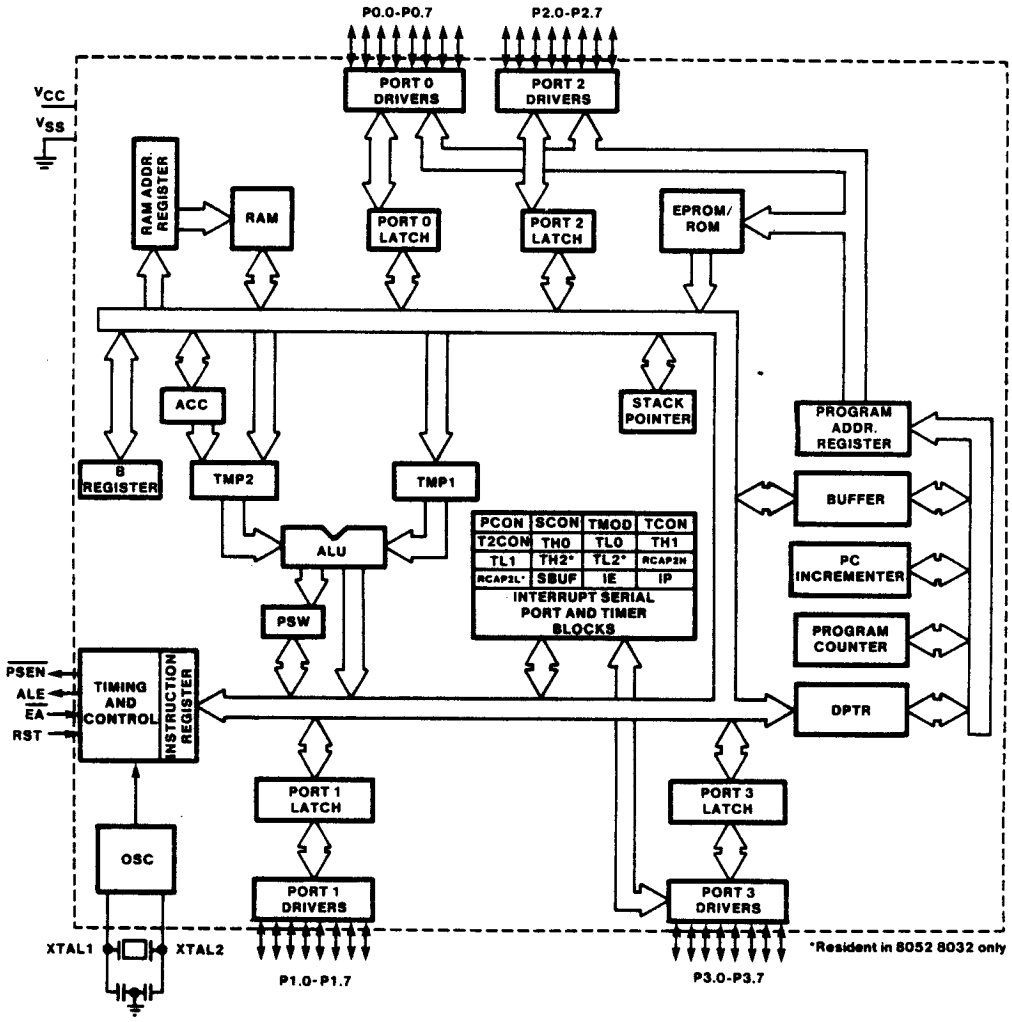

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FIGURE 4.5-1
8031 Block Diagram

4.5.2 Receive Operations

When a key has been depressed on the keyboard the UART within the keyboard will transmit the X/Y code of the key to the 8031 on the IWS controller. This X/Y code will be received by the 8031 through Port 3 bit 0 (P3.0). At this time the 8031 will output to the Z80A an interrupt request through Port 3 bit 7 (P3.7) and flipflop L70 (1B2). When the Z80A receives the interrupt request it will drive both &M1 and &IORQ low, thus generating and acknowledge. The acknowledge signal is decoded by L67 (1E10) and passed to the Keyboard to Data Bus latch (L87 (1D7)) output control pin. When the 8031 generated the interrupt request it placed into this latch a hex C7, which is a RST 0 instruction for the Z80A. Now when the output control of L87 is activated, the RST0 instruction is sent to the Z80A. The Z80A will then jump to the RST0 location and start the keyboard service routine.

The keyboard service routine will generate an IN0 instruction in order to read the X/Y key code. The generation of the IN0 instruction causes the 8031 to clear the interrupt request and place the X/Y key code on the data bus. This is done by activating and interrupt request on the 8031 through Port 3 bit 2 (P3.2). The service routine will then determine what key was depressed and take the appropriate action.

4.5.3 Transmit Operation

There are three items that the 8031 can transmit to the keyboard, beeps, clicks, and data. Both the beep and click commands make use of the timers within the 8031 so they will be discussed first, then the transmitting of a data word to the keyboard will be discussed.

When the software determines that a click or a beep is needed it will generate the appropriate OUT 0 or OUT 1 command. The OUT 0 command will set latch L120 gate 1, (1C7). The low from pin 4 of L120 will cause timer 1 to go into operation. The 8031 detects this timer operation and transmits a click code to the keyboard through Port 1 bit 1, (TXD). To clear the click command latch the 8031 will also generate &CLCIR (Click Clear) signal from Port 2 bit 4 (P2.4). The OUT 1 command sets L120 gate 2 (1B7). This activates timer 2 of the 8031 and causes it to generate a beep code to the keyboard. Once again the 8031 will reset the beep latch by generating a &BPCIR (Beep Clear) signal.

The transmission of a data word to the keyboard is generated by the Z80A performing an OUT 25 instruction. The Z80A will place the data to be transmitted on the data but and activate the OUT 25 I/O line. The OUT 25 signal, decoded by L96 (1C11) clocks the data into the 8031's input data latch and at the same time generates an interrupt to the 8031 through Port 3 bit 2 (P3.2). When the 8031 receives this interrupt it will retrieve the data from the input latch and transmit it to the keyboard through the serial transmit line (TXD). Once the 8031 has transmitted the data to the keyboard it will clear the interrupt pending latch L120 gate 3 (1A7). This is accomplished through the generation of &AFUNCIR (Alternate Function Clear) signal from Port 2 bit 6 (P2.6).

4.5.4 The 8031 Instruction Cycle

As I stated before the 8031 fetches its instruction from an EPROM. This EPROM is only accessible by the 8031 and since it is an EPROM only read operation can be performed. When the 8031 begins an instruction fetch cycle it will place the lower byte of the address on Port 0, and the upper 4 bits of the address on Port 2 bits 0-3. When the 8031 will drive ALE (Address Latch Enable), and &PSEN (Program Store Enable) high, thus latching the address onto the inputs of the EPROM. ALE will then go low followed by &PSEN going low, the 8031 will then read the instruction from the EPROM through Port 0.

4.6 OIS 40/50/60 Bus Interface Logic

The IWS controller interfaces with the RCU board through the 50BUS. This interface allows the RCU to transfer data and instructions to or from the IWS. The RCU has access to the Main memory and the status registers of the IWS, it can also invoke a Restart command to reset the IWS's Z80A.

When the RCU wishes to transfer data to or from the IWS Main memory it will issue a 50BUS Request. When the Z80A receives the bus request it will finish the operation that is in progress and the tri-state its address, data and control bus. Then the Z80A will generate a &BUSAK (Bus Acknowledge), informing the RCU that it may use the IWS's busses. Once the RCU receives the &BUSAK signal it will then place the selected address on the bus and generate the appropriate control signals to transfer the data.

4.6.1 Read operation

To read data from the IWS Main memory the RCU will generate &50SLCT and &50BUSRQ. These two signal are buffered through L156 (3A13) where they are NORed together to generate &ZBUSRQ by L155 and L153 (3A12). Then after the Z80A generates &50B BUSAK the RCU will generated once again a &50 BSLCT along with &50BREQ and 50BR/W. The &BREQ and the &DESLCT are ORed together to enable the 50 Bus Data Buffer L157 (3C13), and generate &AMREQ through now active L76 (3C12). L76 was activated when the Z80A acknowledged the 50BUSRQ signal. The address of the Main memory that the RCU wishes to transfer the data is place on the address bus by 50 Bus Address Bus Buffers L159 and L160 (3D-E13). The direction of travel through the 50 Bus Data Buffer and the Main memory is controlled by the 50BR/W signal, since this is a read operation this signal will be low causing the generation of &BRD by L151 (3C12). Once again L151 was activated by the acknowledge signal from the Z80A.

4.6.2 Write Operation

The write operation is performed in the same manner as the read operation except that the 50BR/W signal is high this time.

4.6.3 Status Information

The RCU can read the status register of the IWS in order to determine the condition of the controller board. Table 4.6-1 list the information that the RCU can obtain.

Table 4.6-1
Status Information

BIT	FUNCTION
0	Not Ready Bit. This bit indicates that the IWS has not been IPLed.
1	Not used. This bit is always high.
2	Parity Error. This bit indicates that a Parity Error has been detected during a transfer to or from Main memory.
3	Power ON. This bit indicates the ON/OFF status of the IWS terminal. When High the terminal is powered ON.
4-7	Defines the type of slave on the bus. For the IWS these bit should indicate a Hex 05.

The RCU can read this information by generating a device select and status signals. The RCU does not have to request the IWS bus to perform this operation.

4.6.4 Block Transfers

A block transfer is performed exactly the way that a one byte transfer is. The only item that must be taken into consideration is that the 64K of Dynamic RAM must be refreshed.

SECTION 4 QUIZ

1) There are several tasks that the Internal Workstation Controller (IWS)must perform, name three of them.

2) During what operation are WAIT states inserted in to the Z80A instruction cycle?

3) Of the four memories located in the IWS board, which one has parity checking?

4) What type of information is contained in the Control portion of the CRT memory?

5) The location that information is stored in the character memory is representative of what?

6) What type of information is stored in the Font memory?

7) Can the RCU down load information directly into the CRT and Font memories?

8) When the Z80A access either the Font memory or the CRT memory, which section of the Main memory is switched out?

9) The four address lines for the Font memory that indicate the row of the font are produced by what?

10) The 8031 Microcontroller performs what function on the IWS board?

SECTION 5
APPENDICES

APPENDIX

A

APPENDIX A:

RELATED DOCUMENTATION

System Installation Guide for VS, 2200, WP/OIS Systems	(729-0907)
Site Prearation Guide	(700-5978)
OIS Supervisor Procedures Manual	(700-5562-C)
OIS Supervisor Quick reference Guide	(700-5741-C)
Documentation Control and Processing Index	(729-0000-B)
TCB-1, DLP64, DLP128 Telecommunication Controllers	(729-0887-B)
Product Maintenance Manual: Wang Daisy Printers	(729-0372-A)
Archive Workstation - Service Information, WPNL #77	(729-0521)
Mag-Card Reader for WPS, WPNL #78	(729-0545)
Model 61/62 Matrix Printer Maintenance Manual	(729-0339)
Model 44, 48 Phototypesetter	(729-0465)
Image Printer Maintenance Manual	(729-0447)
Model 5538 Twin Sheet Feeder (TSF) Installation Manual	(729-0549)
Envelope Feeder (EF) Product Maintenance Manual	(729-0873)
WISE Model 6550-1 PMM	(729-0906)
TCB-1 TC Controller Self Study Workbook	(729-1057)
Advance Function Training Workbook	(700-7018)
Introduction to Wang Office Systems	(700-6944)
OIS Overview	(700-7009)
Glossary Training Workbook	(700-6983)
Glossary Auxiliary Functions	(700-4642-C)
Decision Processing Reference Guide	(700-4614-C)
Column Edit User Manual	(700-5104-C)
Mathpak User Manual	(700-4671-E
Mathpak Applications User Manual	(700-4732-D)
System Security	(700-6865-A)
Corporate Publications Literture Catalogue	(700-7647)
Wang Supply Catalogue	(700-5725-B)
Office Training Guide	(700-4010)
OIS 40/50 Administrator's Guide	(700-8086)

APPENDIX

B

APPENDIX B

OIS 40/50/60 MNWEMONICS

PART 1: RMU SIGNAL MNEMONICS

MNWMONIC	DESCRIPTION
A0-15	RMU Address Bus. Addresses on A0-15 can originate from either the Z80A or the 50BUS.
A7'	Address Bit 7. Z80A Address Bit 7 is separated from the other address bits to meet memory refresh requirements.
A7R	Address Bit 7 Refresh. Z80A Address Bit 7 modified to meet memory refresh requirements.
AUTO RESET	Automatic Reset. Generated by L131. When power is first applied, holds the OIS 50 circuitry in reset state until proper voltage levels are reached.
BOR	Serial Data Link Receive Borrow Strobe. Generated by L92 when the SDL receives a full data byte.
BUSAK	Bus Acknowledge. Generated by Z80A, after it receives a bus request, to relinquish bus control.
BUSREQ	Bus Request. Generated by L143 when the RMU receives 50B BUSREQ and 50BSLCT0. The RCU generates these signals when it requires 50BUS control of the RMU board.
BYTE RECD	Serial Data Link Byte Received. Generated by L91 when the SDL receives a byte of data.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
BYTE REQ	Serial Data Link Byte Request. Generated by L61 when the SDL needs a byte of data to transfer.
CAS	Column Address Strobe. Generated by L50. Strobes a particular column address bit into memory.
CASB	Column Address Strobe Buffered. Generated by L50. Enables memory data and parity in and out of memory.
CHAN SLCT	Channel Select. Generated by L110. Causes the channel selection logic to choose a channel for an SDL receive or transmit operation.
CH0SL-CH3SL	Serial Data Link Transmit Channel Select. Generated by L124. Selects the proper channel for an SDL transmission.
CH1BNC-CH4BNC	BNC Serial Data Link Ports 0-4. BNC connectors for Serial Data Link Ports 1-4.
CH1TNC-CH4TNC	TNC Serial Data Link Ports 0-4. TNC connectors for Serial Data Link Ports 1-4.
CK	16-MHz Clock. Generated by L66 as the basic timing signal from which other RMU-generated timing signals are derived.
CLCYB	Clear Memory Cycle Buffered. Generated by L53. Clears the RAS/CAS logic and signals the end of a memory read or write cycle.
CL HALT	Clear Halt. Generated by L146 to release the 8X305 Microcontroller from a halt state.
CMD BUSREQ	Command Bus Request. Generated by the RCU. Generates a direct bus request to the Z80A after the Z80A has issued a command to the RCU.
CTC CE	CTC Chip Enable. Generated by L80 (MMI/O Decoder) and L79 to enable the CTC Processor.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
CUBUSY	Control Unit Busy. Generated by the RCU to assert the CTC and, therefore, to generate a Z80A interrupt. Indicates that the RCU has completed an operation and is no longer busy.
D0-7	RMU Data Bus. Data on the RMU Data Bus can originate from the Z80A, 50BUS, SWITCH, FDC, RAM, or PROM.
D0Z-D7Z	Z80A Unbuffered Data Bus. Used only by the CTC and the Z80A to provide a clear communication path between the two devices.
DACK	DMA Acknowledge. In response to a DMA Request from the FDC, DACK normally is generated by L111 (on the RMU) when the RCU has bus control. During diagnostics, L103 generates DACK under Z80A control.
DATA	Serial Data Link Received Data. Data that has passed through SDL Multiplexer L121 (from an SDL Channel).
DATA IN	Serial Data Link Received Data. Inverted DATA signal.
DATA OUT	Serial Data Link Transmitted Data. Outgoing SDL data (generated by L56) available for transmission on the inputs of the SDL Drivers.
DCH0-DCH3	Data Channels 0-3. Converted TNC-BNC data generated by L136 and L139 for channels 0-3 of the SDL.
DIRECTION	FDD Head Step Direction. Generated by L119 under FDC control. Tells the FDD which direction the FDD head should step.
DLMR	Data Link Master Reset. Clears the SDL logic. Generated by gating Master Reset signal through L41.
DMI	Dead Man Interrupt. Generated by L69 to indicate an error when the FDC does not complete a command within 540 ms.
DOC	Data Out Control. Generated by L43. Enables memory data onto the Z80A data bus.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
DOL	Data Out Load. Generated by L44 to clock memory read data out of memory into Latches L39 and L45.
DOOR DIST	Door Disturbed. Generated by L120 as a result of the DOOR DISTURB signal.
DOOR DISTURB	Door Disturbed. Generated by the FDD when its Disk Access Door has been opened.
DREADDATA	Disk Read Data. Incoming data from the Floppy Disk Drive.
DS1-4	Drive Select Lines 1-4. L118 generates DS1 to select the Floppy Disk Drive. DS2-DS4 are unused.
ENABLE SAMPLE	Enable Sample. Generated by L91. Enables Data Link Bit Counter to begin counting received data bits.
EPDB	Enable Processor Data Buffer. Generated by L34 to initiate the RAS/CAS generation cycle for a memory data transfer. EPDB also enables memory read data onto the Z80A data bus.
ERFSH	Early Refresh. Generates a Refresh Memory cycle and presets the Refresh A7 Bit Control Flipflop (L52). L52 places either the Synthetic Refresh A7 bit or the A7' bit onto the Address Bus as A7R.
FDCD0-7	Floppy Disk Controller Data Bus. Passes data between 50BD0-7 and D0-7 Data Buses.
FDDMARD	Floppy Disk DMA Read. Generated by L143. Initiates FDD DMA read operations.
FDDMAWR	Floppy Disk DMA Write. Generated by L112 to initiate FDD DMA write operations.
FDWCK	Floppy Disk Write Clock. Generated by L107 as the FDC's write clock. Also synchronizes the data recovery logic.
FF00-FF0F	Memory Mapped Input/Output Commands. Generated by L80 under Z80A control.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
FINT	Floppy Disk Drive Interrupt. Generated by the FDC when the FDC completes command execution.
INDEX	Index. INDEX pulses are generated from the FDD when a disk is loaded and spinning and the drive is selected.
INT	Interrupt. CTC-generated interrupt to the Z80A. The interrupt is accompanied on the data bus by a unique vector which points the Z80A to a service routine.
IORQ	I/O Request. Generated by the Z80A whenever the Z80A makes an I/O operation request.
M1	Machine Cycle. Generated by the Z80A during op-code fetch cycles.
MD0I-MD7I	Memory Data Input Bus. Created as data passes from the D0-7 Data Bus through L37.
MD0O-MD7O	Memory Data Output Bus. Generated by RAM.
MDPI	Memory Data Parity In Bit. Created when the PARIN signal is gated through L56.
MDPO	Memory Data Parity Out Bit. Gated through L45 to generate the PAROUT signal.
ME	Memory Error. Generated by L29 when a parity error is detected in RAM. ME is used to create a non-maskable interrupt to the Z80A.
MMI/O	Memory Mapped Input/Output. Generated by L63. One of two MMI/O enabling signals. MMI/O is active during valid MMI/O requests.
MOTOR ON	Motor On. Generated by L118. Turns the FDD motor on and off.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
MR	Master Reset Buffered. Generated by buffering the MRZ signal through L81. Primarily used on the RMU board.
MRC	Master Reset. Generated by buffering the MRZ signal through L81. Used by all 50BUS-connected boards to indicate that power is up and stable.
MREQ	Memory Request. Generated (via 50BREQ) by the Z80A or the RCU during memory request operations.
MRFD	Master Reset to the Floppy Disk Drive. Generated by buffering the MR signal through L71.
MRZ	Master Reset. Generated by buffering the AUTO RESET signal through L65. Other RMU reset signals are generated directly from this signal.
MUX	Multiplex Memory Address. Generated by L50. Switches the Memory Address Multiplexer from Row Address (low address byte) to column address (high address byte).
NO DATA	No Data. Generated by L127 when a Data Link channel does not respond to a command within 86 us.
ODDPAR	Odd Parity. Serial Data Link Transmit Logic Parity Bit. Generated by L73.
PARIN	Memory Parity Input Bit. Parity bit of data being written into memory. Generated by L46.
PAROUT	Memory Parity Output Bit. Parity bit of data being read from memory. Generated by L45.
PORTAD	Port Address. Generated by L95 to help enable the MMI/O Decoder when the proper address range (high address bits A8-15) is selected for an MMI/O operation.
PROM	PROM Select. Generated by L7 when all conditions are met to select the PROM for operation.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
PWAIT	Processor Wait. Generated by L31. Inserts a single wait state during MMI/O operations.
R4.275M	Receive Serial Data at 4.275 MHz. Clock signal generated by L93. Used to receive serial data.
RAS	Row Address Strobe. Generated by L54. Strobes a particular row address into memory.
RD	Z80A Read Request. Generated (via 50BR/W) by the Z80A or the RCU whenever a read operation is pending.
RD1	Z80A Read Request. Generated by the Z80A whenever the Z80A performs a read operation.
RDATA0-7	Read Data Bits 0-7. Serial Data Link Receive Data Bus. Generated by L76.
READ DATA	Read Data. Serial data stream from the FDD after the data is separated via the data recovery logic.
READ WINDOW	Read Window. Data is read into the FDC when the read window is open (ie, READ WINDOW is active).
RECD DATA	Received Data. Generated by L110. Places SDL received data onto 50BUS.
RECD PAR	Received Parity. Generated by L77 to indicate that the Serial Data Link has received the wrong parity bit along with the received data.
RECEIVE	Receive. Generated by L109. Initiates a Serial Data Link receive operation.
REC ENB	Receive Enable. Generated by L108 to enable the Serial Data Link receive logic.
RFF0B	Read FF0B. Generated by gating the RD1 and FF0B signals at L108. RFF0B reads the FDC Status Register.
RFF0E	Read FF0E. Generated by gating the RD1 and FF0E signals at L10. RFF0E reads the Memory Parity Bit.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
RFSH	Refresh. Generated by the Z80A. Causes the refresh logic to refresh memory.
SIDE SELECT	Side Select. Generated by the FDC. Selects the disk surface to be used in the FDD operation.
STATUS RD	Status Read. Generated by L110 to place the Serial Data Link Status Nibble onto the 50BUS.
STEP	Step. Generated by the FDC. Instructs the FDD to step the head in the direction specified by the DIRECTION signal.
T4.275	Transmit Serial Data at 4.275 MHz. Clock signal generated by L60. Used to transmit serial data.
TDATA0-7	Transmit Data Bits 0-7. Serial Data Link Transmit Data Bus. Generated by L74.
TRACK0	Track Zero. Generated by the FDD. Informs the FDC that the drive is located at Track 0.
TRANSMIT	Transmit. Generated by L109. Initiates a Serial Data Link transmit operation.
VCO	Voltage Controlled Oscillator Enable. Disables the Phase/Frequency Detector from generating a free-running frequency and enables receipt of the D READ DATA signal from the FDD.
WFF0B	Write FF0B. Generated by gating the WR and FF0B signals at L108. WFF0B writes to the FDC Status Register.
WR	Write. Generated by the Z80A whenever the Z80A performs a memory or I/O write operation.
WR DATA	Write Data. Serial data stream issued from the FDC to the FDD (via the write data precompensation circuitry).

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
WR GATE	Write Gate. Generated by the FDC. Places the FDD in the write mode of operation.
WRITE	Write. Generated by L54. Controls read and write operations in RAM.
WRITE PROTECT	Write Protect. Generated by the FDD. Provides the FDC with the FDD disk write protect status.
WSK CMP	Winchester Seek Complete. Generated by the Winchester Disk Drive to assert the CTC and, therefore, to generate a Z80A interrupt. WSK CMP indicates that the Winchester Disk Drive has completed a seek operation.
XMIT DATA	Transmit Data. Generated by L110. Transmits data from the 50BUS to the SDL transmit logic.
IA	Phi-A FDC Write and Z80A WAIT State Synchronization Clock. L31 generates the 8-MHZ Phi-A signal to synchronize the FDC Write signal. Phi-A also synchronizes the insertion of Z80A WAIT states.
IZ	Phi-Z FDC Clock. L32 generates this 4-MHz signal to clock the FDC and to synchronize DMA operations.
IZC	Phi-ZC Z80A and CTC Clock. L32 generates this 4-MHz signal to clock the Z80A and the CTC.
1/2I	1/2Phi Synchronization Clock. L32 generates this 8-MHz signal to synchronize memory access and Z80A Data Bus direction control signal generation.
50BA0-15	50BUS Address Bus. Shared by all boards (except the Telecommunications board) in the OIS 50 system.
50BBUSAK	50BUS Acknowledge. Generated by L127 when the Z80A, after receiving a bus request, relinquishes bus control to the RCU.

PART 1: RMU SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
50BBUSREQ	50BUS Bus Request. Generated by the RCU to request Z80A data and address bus control to perform a DMA operation.
50BD0-7	50BUS Data Bus. Shared by all boards (except the Telecommunications board) in the OIS 50 system.
50BD0-3B	Buffered 50BUS Nibble. Generated by L126 for use in Serial Data Link channel selection.
50BDRQ	50BUS DMA.Request. Generated by the FDC. Requests a DMA data transfer.
50BR/W	50BUS Read or Write. Generated by the RCU board. Indicates that a read or write memory operation is on the 50BUS.
50BREQ	50BUS Byte Request. Generated by the RCU to initiate action on the 50BUS. Devices selected by 50BSLCT0-2 are activated upon receipt of this signal.
50BREQB	Buffered 50BUS Byte Request.
50BSLCT0-2	50BUS Device Select. Generated by the RCU to select a device on the 50BUS (0 = RMU, 1 = Serial Data Link, 2 = Floppy Disk Drive).
50BTC	50BUS Terminal Count. Generated by the RCU. Provides the FDC with the Terminal Count at the end of a data transfer in a DMA operation.
8MHZ	8-MHz RCU Clock. Generated by L66 on the RMU board for use by the RCU board.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
+ MFMRD	+ MFM Read Data. MFM data stream from Winchester.
+ MFMW	+ MFM Write Data. MFM data stream to Winchester.
- MFMRD	- MFM Read Data. MFM data stream from Winchester.
- MFMW	- MFM Write Data. MFM data stream to Winchester.
50BA0-15	50BUS Address Bus. Generated by the 50BUS Address Buffer/Counters (L143A, L147, and L148) from inputs received from the IV bus. 50BUS addresses are passed to all boards (except the Telecommunications board) in the OIS 50 system.
50BBUSAK	50BUS Acknowledge. Generated by the RMU board or a system slave when bus control is relinquished to the RCU.
50BBUSREQ	50BUS Bus Request. Generated by the 50BUS Control Signal Buffer (L144) to request 50BUS control in order to perform a DMA operation.
50BD0-7	50BUS Data Bus. Generated as data is buffered from either the 4K x 8 Data Buffer Bus (via L128) or the IV bus (via L145). 50BUS data is passed to all boards (except the Telecommunications board) in the OIS 50 system.
50BDRESET	50 Bus Device Reset. Generated by the 50BUS Control Signal Buffer (L144) to reset the device that is selected on the 50BUS.
50BDRQ	50BUS DMA Request. Generated by the RMU or a system slave to request 50BUS control in order to perform a DMA operation.
50BDSTAT	50 Bus Device Status. Generated by the 50BUS Control Signal Buffer (L144) to request status information about the device that is selected on the 50BUS.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
50BR/W	50BUS Read or Write. Generated by the 50BUS Control Signal Buffer (L144) to command a read or write operation on the 50BUS.
50BREQ	50BUS Byte Request. Generated by the 50BUS Control Signal Buffer (L144) to initiate action on the 50BUS. The device selected by 50BSLCT0-7 is activated upon receipt of this signal.
50BSLCT0-7	50BUS Device Select. Generated by the 50BUS Device Select Chip (L146) to select a device on the 50BUS (0 = RMU, 1 = Serial Data Link, 2 = Floppy Disk Drive, 3 = IWS1, 4 = IWS2, 5 = IWS3, 6 = IWS4, 7 = IWISE).
50BTC	50BUS Terminal Count. Generated by the 50BUS Control Signal Buffer (L144) to provide the floppy disk controller on the RMU with the Terminal Count at the end of a data transfer during a DMA operation.
50BUS	50BUS Functions Strobe. Generated by the Right Bank Decoder (L80) to enable either a 50BUS read or write operation.
8MHZ	8-MHz Clock. Generated by the RMU board to synchronize data passing between the RMU and the RCU.
8XDATAEN	8X305 Data Enable. Generated by the 50BUS Data Control Flipflop (L112) to pass data from the /IV0-7 bus, through L145, onto the /50BD0-7 bus.
A0-7	Z80A Address Bus. Addresses are received by the RCU-resident Z80A I/O decoder logic in order to move data between the RMU and the RCU, via the PRF or SRF.
ADD HIGH	Address High Order. Generated by the 50BUS Write Control Decoder (L114) to pass addresses from the IV bus, through L148, onto the high-order 50BUS address bus.
AMD	Address Mark Detect. Generated by the Address Mark Detector (L29) when the A1H address mark has been detected.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
AMDDLY	Address Mark Detect Delayed. Generated by L5 as it delays the AMD signal by one DCLK pulse.
BA0-10	4K x 8 Data Buffer Address Bus. Generated by Address Buffer/Counters L125, L126, and L143 from inputs received from the IV bus.
BD0-7	4K x 8 Data Buffer Data Bus. Generated by the 4K x 8 Data Buffer (L109 and L110), BD0-7 is the 4K x 8 Data Buffer's outgoing data bus.
BDONER	Byte Done Read. Generated by the Serial to Parallel Converter (L107) to indicate that a byte of data has been sent and another byte is required to be placed in a parallel form.
BDONEW	Byte Done Written. Generated by the Parallel to Serial Converter (L141) to indicate that a byte of data has been sent to the Winchester and another byte is required for serialization.
BUFFDATAEN	Buffer Data Enable. Generated by L112 to enable the 4K x 8 Data Buffer to 50BUS Data Buffer (L128). Passes data from the BD0-7 bus onto the 50BD0-7 bus.
BUFFER	Buffer Memory Functions Strobe. Generated by Right Bank I/O Decoder L80 to enable either a 4K x 8 Data Buffer read or write operation.
BUFFRD	4K x 8 Data Buffer Read. Generated by the Data Buffer Read Control Flipflop (L76) to place the 4K x 8 Data Buffer in the read mode of operation.
BUFFWR	4K x 8 Data Buffer Write. Generated by the Data Buffer Write Control Flipflop (L76) to place the 4K x 8 Data Buffer in the write mode of operation.
BUSAK	Bus Acknowledge. Generated on the RMU board to disable RMU-RCU Data Transceiver L149. BUSAK is active only if the Microcontroller maintains bus control. Data is never moved between the RMU and the RCU while the Microcontroller has bus control.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
BUSREQ50B	50BUS Bus Request. Generated by the 50BUS Bus Request Signal Generating Flipflop (L130) to request Z80A data and address bus control to perform a DMA operation.
CLHALT	Clear Halt. Generated by the RMU to release the Microcontroller from a halted condition by clearing the halt-generating circuit.
CLMC	Controller Master Clear. CLMC, which is derived from the RESET signal, clears and resets much of the RCU hardware.
CLMCB	Buffered Controller Master Clear. See CLMC.
CMD	Command Notification Bit. Generated by the Z80A I/O Decoder (L98) in response to an RMU command. The CMD bit notifies the RCU that a command has been loaded into the PRF and the Z80A has surrendered bus control.
CMDBUSREQ	Command Bus Request. Generated by the Command Bus Request Flipflop (L125) to generate a request to the RMU after the Z80A has issued a command to the RCU.
CNTRL	50BUS Control. Generated by the 50BUS Write Control Decoder (L114) to cause the active or inactive /R/W and /BUSREQ50B signals to be generated.
COMMAND	Command. Generated by Right Bank I/O Decoder L80 to issue the Command Notification bit. The Command Notification bit is generated to issue a Command Bus Request (/CMDBUSREQ) signal to the RMU.
CUBUSY	Control Unit Not Busy. Generated by the RCU to assert the Counter Timer Chip and, therefore, to generate a Z80A interrupt. CUBUSY indicates that the RCU has completed an operation and is no longer busy.
D0-D7	Z80A Data Bus. Data is passed between the RMU and the RCU via the Z80A data bus and RMU-RCU Data Transceiver L149.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
DATA ENABLE	Data Enable. Generated by the 50BUS Write Control Decoder (L114) to enable data from either the IV bus or the 4K x 8 Data Buffer bus onto the 50BUS data bus.
DCLK	Data Clock. Generated by Address Mark Detector L129. DCLK is the clock signal from the Winchester-generated incoming data stream.
DEARLY	Data Early. Generated by L138 for write precompensation purposes in response to the incoming WDATA serial data stream. DEARLY is written to the Winchester in a 10-ns early format if the control signal from L92 pin 13 is activated.
DIRECTION	Direction. Generated by the Winchester Drive Program Control Signal Generator (L136) to command the direction of head motion for a Winchester seek operation.
DLATE	Data Late. Generated by L138 for write precompensation purposes in response to the incoming WDATA serial data stream. DLATE is written to the Winchester in a 10-ns late format if the control signal from L92 pin 12 is activated.
DNOM	Data Normal. Generated by L138 for write precompensation purposes in response to the incoming WDATA serial data stream. DNOM is written to the Winchester in the standard format when the control signal from L92 pin 11 is activated. DNOM data is written when write precompensation is not needed.
DREAD	Drive Read. Generated by Winchester Drive Program Control Signal Generator (L136) to aid in controlling Control Multiplexer L47 and to allow the phase locked loop to accept data.
DRIVESLCT	Drive Select. Generated by the Winchester to indicate that the Winchester has been selected.
DRS	Buffered Drive Select. Generated by the Write Precompensation Buffer (L90). See DRIVE SLCT.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
DRVSLCT	Drive Select. Generated by the Winchester Drive Program Control Signal Generator (L136) to select the Winchester for an operation.
DSKWRITEDATA	Disk Write Data. Generated by Winchester Write Decoder L62 to move a byte of data from the /IV0-7 bus, through L124, onto the Winchester buffered data bus (WBD0-7).
DWRITE	Drive Write. Generated by Winchester Drive Program Control Signal Generator L136 to aid in controlling Control Multiplexer L47.
DWTG	Drive Write Gate. Generated by buffering the Write Gate (WTG) signal. DWTG is sent to the Winchester to prepare it for the upcoming write to the Winchester operation.
E50BDTB	Enable 50BUS Data To Buffer. Generated by the 50BUS Data to Data Buffer Control Flipflop (L111) to enable the 50BUS to 4K x 8 Data Buffer (L127).
EBDTD	Enable Data Buffer to Winchester. Generated by the Data Buffer to Winchester Data Control Flipflop (L95) to enable the BD0-7 to WBD0-7 Bus Data Latch (L142).
ECCTIME	ECC Time Enable. Generated by the Winchester Interface Control Signal Generator (L119) to enable switching of Control Multiplexer L47 after the data field has been read or written.
EDDTB	Enable Winchester Data To Buffer. Generated by the Winchester to Data Buffer Data Control Flipflop (L95) to enable the Winchester to BD0-7 Bus Data Buffer (L108).
ENSTAT	Enable Status. Generated by L86 to enable the SRF Data Buffer (L150). Data is passed from the SRF Data Out (/SDO0-7) bus onto the Z80A Buffered Data (ZD0-7) bus.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
HALT	Halt Microcontroller. Generated by the Halt Generating Flipflop (L61) to place the Microcontroller in a halt state.
HDSEL0-2	Head select 0-2. Generated by the Winchester Drive Program Control Signal Generator (L136) to select the proper head for a Winchester operation.
I0-15	Microcontroller Instruction Bus. Instructions for the Microcontroller arrive from the PROM instruction storage area via the I0-15 instruction bus.
INDEX	Index. Generated by the Winchester disk drive as each index mark is written to or read from the disk.
INTERRUPT	Interrupt Functions Strobe. Generated by Right Bank I/O Decoder L80 to issue the Control Unit Busy (/CUBUSY) signal. Control Unit Busy notifies the RMU when the Microcontroller is busy performing an operation.
IOS	Index 1-Shot. Generated by Index 1-Shot L48 as each Index signal is read from the Winchester.
IV0-7	Interface Vector Bus. Generated by the Microcontroller (via Microcontroller Data Transceiver L69), the IV bus is the primary internal data bus in the RCU.
LBA0-7	Left Bank Address Bus. Generated by the Left Bank Address Latch (L68) from inputs received from the IV bus. Left bank addresses are used to address 256 bytes of scratchpad RAM.
LBINPUTDATA	Left Bank Input Data. Control signal generated by Control Signal Decoder L38 when the Microcontroller's Left Bank (/LB) signal is active and it's Write Control (/WC) signal is inactive, indicating a scratchpad read.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
LBOUTPUTDATA	Left Bank Output Data. Control signal generated by Control Signal Decoder L38 when the Microcontroller's Left Bank (/LB) and Write Control (/WC) signals are active, indicating a scratchpad write.
LOADDSKWD	Load Disk Write Data. Generated by Winchester Write Decoder L62 to indirectly (via L75) clock data out of the Parallel to Serial Converter.
LOOPEN	Loop Enable. Activated by L60 to reset the Data Recovery Circuit.
LPRS	Loop Reset. Activated by L17 to reset the Data Recovery Circuit and the Data Recovery Counters.
MCLK	Microcontroller Master Clock. Generated by the Microcontroller to synchronize RCU board operations.
MINCOUNT	Minimum Count. Generated by L2 when the Data Recovery Counters have counted the synchronizing field (eight bytes of zeros) that precedes an address mark.
MMI/O	Memory Mapped Input/Output. Generated on the RMU board to act as an enabling signal for the Z80A I/O logic on the RCU board. MMI/O is active during any Z80A memory mapped input/output operation.
MRC	Z80A Master Reset Clear. Generated on the RMU board to indicate that power is up and stable. Used by all 50BUS-connected boards.
NRZR	NRZ data stream read from the Winchester. Generated by flipflop L27 (2Q output), which passes data out of the Data Separator Circuit.
NRZW	NRZ data stream to be written to the Winchester. Generated by Serial to Parallel Converter L141.
PARAMETER	Parameter Register File Select Read or Write. Generated by Z80A I/O Decoder L98 to select a Z80A-controlled PRF read or write operation.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
PARREGFILE	Parameter Register File Functions Strobe. Generated by Right Bank I/O Decoder L80 to select the PRF for a Microcontroller-controlled read or write operation.
PDI0-7	Parameter Register File Data Input Bus. Moves data from either the ZD0-7 bus or the /IV0-7 bus to the PRF.
PDO0-7	Parameter Register File Data Output Bus. Moves data from the PRF to either the ZD0-7 bus or the /IV0-7 bus.
PGDATA	Page Data. Generated by Control Multiplexer L19 (from NRZR or NRZW input) for use as the ECC Shift Register's data input during read and write operations.
R/W	Read/Write. Generated by the 50BUS Read/Write Signal Generating Flipflop (L130) to command a read or write operation on the 50BUS.
RB1-3	SRF Read Bank. Each Read Bank signal (1-3) asserts enabling pins on two SRF chips, thereby enabling a read of an entire 8-bit byte when /RB1, /RB2, or /RB3 is active.
RBA0-7	Right Bank Address Bus. Generated by Right Bank Address Latch L85 from inputs received from the IV bus. Right bank addresses are used to generate I/O commands which control the primary RCU functions.
RBINPUTDATA	Right Bank Input Data. Control signal generated by Control Signal Decoder L38 when the Microcontroller's Right Bank (/RB) signal is active and its Write Control (/WC) signal is inactive, indicating an I/O port read.
RBODMCLK	Right Bank Output Data synchronized with Master Clock. Generated by L81, RBODMCLK is used throughout the RCU to synchronize the movement of data out of the Microcontroller's right bank.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
RBOUTPUTDATA	Right Bank Output Data. Control signal generated by Control Signal Decoder L38 when the Microcontroller's Right Bank (/RB) and Write Control (/WC) signals are active, indicating an I/O port write.
RD	Z80A Read Request. Generated by the Z80A to perform a Z80A-controlled PRF read operation.
RDPAR	Z80A Read Parameter Register File. Generated at L96 when the /PARAMETER signal is gated with the /RD signal. RDPAR controls the direction of RMU-RCU Data Transceiver L149 when the RMU is accessing the PRF.
READ	Data Buffer Read. Generated by the 4K x 8 Data Buffer Decoder (L77) to command a 4K x 8 Data Buffer read operation. Two consecutive writes to port 32H must be performed to read data (creating a READ signal of 200-ns duration).
READCNTLSTATUS	Read Control Status. Generated by the Winchester Read Decoder (L78) to read the Control Status Byte through the Control Status Register (L122).
READDSKDATA	Read Disk Data. Generated by the Winchester Read Decoder (L78) to move a byte of data from the incoming Winchester bus, through L123, onto the /IV0-7 bus.
READDSKSTATUS	Read Disk Status. Generated by the Winchester Read Decoder (L78) to read the Disk Status byte through L121 onto the /IV0-7 bus.
READY	Ready. Generated by the Winchester to indicate that the drive is ready to perform an operation.
REQ	Request. Generated by the 50BUS Write Control Decoder (L114) to generate the active /REQUEST signal which, in turn, generates the /50BREQ signal via L144.
REQUEST	50BUS Request. Generated by the 50BUS Request Signal Generating Flipflop (L132) to activate the /50BREQ signal from L144.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
RESET	Z80A Reset. Generated by the Z80A I/O Decoder (L98) in response to an RMU command. The RESET signal asserts the Microcontroller and other RCU circuitry to reset the RCU board.
RESET50B	Reset 50BUS Device. Generated by L144 to reset various 50BUS devices.
RLOOP	Read Loop. Generated when L36 gates either an active /SRESET or /IOS signal through to reset the Data Recovery Counters.
RP40H	Read 50BUS Data. Generated by the 50BUS Read Control Decoder (L78) to enable the 50BUS to /IV Bus Data Buffer (L129). L129 passes data from the /50BD0-7 bus to the /IV0-7 bus.
RW	Read/Write for Winchester. Generated via L456 when either the DREAD or DWRITE signal is activated. Enables L31 to generate the select signal that controls the Control Multiplexer (L47).
RWC	Reduced Write Current. Generated by the Winchester Drive Program Control Signal Generator (L136) to select reduced write current for write precompensation purposes.
SDO0-7	Status Register File Data Output Bus. Moves data from the SRF onto the buffered Z80A data bus (ZD0-7).
SEEK COMPLETE	Seek Complete. Generated by the Winchester to indicate that it has completed a seek operation.
SKPEN	Skip Enable. Generated by the Winchester Interface Control Signal Generator (L119) to enable MFM Generator L92 to create an address mark during format or write operations.
SLAVE SLCT	Slave Select. Generated by the 50BUS Write Control Decoder (L114) to clock the 50BUS Device Select Chip (L146). When clocked, L146 generates the device select signal (from /50BSLCT0-7) corresponding to the code it receives on the /IV0-7 bus.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
SPFUNC	Special Function. Generated by L114 to clock the Special Function Flipflops (L131 and L132).
SRCLOCK	Shift Register Clock. Generated by Control Multiplexer L19 (from its DCLK or WCLK input) for use as the ECC Shift Register's clock input during read and write operations.
SRESET	Software Reset. Generated by the Winchester Interface Control Signal Generator (L119) to reset the Data Recovery Circuit.
STATUS	Status Register File Read. Generated by the Z80A I/O Decoder (L98) to select a Z80A-controlled SRF read operation.
STATUS50B	Status 50BUS. Generated by the 50BUS Status Signal Generating Flipflop (L132) to assert the 50BUS Control Signal Buffer (L144) and generate the /50BDRESET signal. STATUS50B also prevents the /REQUEST signal from incrementing the 50BUS Address Counters in operations during which they should not be incremented.
STEP	Step. Generated by L57 of the Winchester step logic to command the Winchester heads to move one step in a predefined direction during a track seek operation.
STREGFILE	Status Register Functions Strobe. Generated by Right Bank I/O Decoder L80 to select the SRF for a Microcontroller-controlled write operation.
TC	Terminal Count. Generated by the 50BUS Terminal Count Signal Generating Flipflop (L131) to assert the 50BUS Control Signal Buffer (L144) and generate the /50BTC signal.
TRACK0	Track Zero. Generated by the Winchester to indicate that Track 0 has been detected.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
WB1-3	SRF Write Bank. Each Write Bank signal (1-3) asserts enabling pins on two SRF chips, thereby enabling a write of an entire 8-bit byte when /WB1, /WB2, or /WB3 is active.
WBD0-7	Winchester Buffered Data Bus. Data to be written to the Winchester passes from either the BD0-7 bus or the /IV0-7 bus onto the WBD0-7 bus, and from there to the Parallel to Serial Converter (L141).
WCLK	Write Clock. Generated by the Write Clock Flipflop (L75), WCLK is the write clock for the Winchester write circuitry.
WCLOCK	Winchester Write Clock. Generated by Control Multiplexers L47 and L19 (from their WCLK inputs) to act as the MFM Generator's write clock signal.
WDATA	Write Data. Generated by Control Multiplexer L47 (from an NRZW input) for use as the serial data input to the MFM Generator.
WDATAP	Write Data Precompensation. Generated by MFM Generator L92, WDATAP is the outgoing serial data stream before it is passed through the Write Precompensation Circuit.
WECC	Write ECC. Generated when the Data Buffer Write (WRITE) signal is gated with a high signal from the ECC Output Control Flipflop (L31). WECC drives the select pin of Control Multiplexer L47 low, which selects the ECC Circuit's output as the input to the data stream.
WINCH	Winchester Functions Strobe. Generated by Right Bank I/O Decoder L80 to enable either a Winchester read or write operation.
WP41H	Write 50BUS Addresses. Generated by the 50BUS Write Control Decoder (L114) to load low-order address from the /IV bus onto the 50BUS address bus.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
WP43H	Write 50BUS Data. Generated by the 50BUS Write Control Decoder (L114) to clock the /IV Bus to 50BUS Data Latch (L145). L145 passes data from the /IV0-7 bus to the /50BD0-7 bus.
WP56H	Clock Halt Circuit. Generated by Winchester Write Decoder L62 to clock the Microcontroller Halt Circuit.
WPB	Write Precompensation Bit. Generated by the Winchester Interface Control Signal Generator (L119) to enable the MFM Generator to create write precompensation control signals.
WR	Z80A Write Request. Generated by the Z80A to perform a Z80A-controlled PRF write operation.
WRITE	Data Buffer Write. Generated by the 4K x 8 Data Buffer Decoder (L77) to command a 4K x 8 Data Buffer write operation. Two consecutive writes to port 33H must be performed to write data (creating a WRITE signal of 200-ns duration).
WRITEFAULT	Write Fault. Generated by the Winchester to indicate that a write fault has been detected.
WRITEDRPRG	Write Drive Program Byte. Generated by the Winchester Write Decoder (L62) to clock the Write Drive Program Signal Generator (L136), causing L136 to generate drive programming signals.
WRITEHOTSC	Write High-Order Track Step Counter. Generated by the Winchester Write Decoder (L62) to load the high-order step count into the High-Order Step Counter (L106).
WRITELOGICCNTRL	Write Logic Control Signals. Generated by the Winchester Write Decoder (L62) to clock the Winchester Interface Control Signal Generator (L119), causing L119 to generate write logic (RCU-resident) control signals.

PART 2 : RCU SIGNAL MNEMONICS

MNWEMONIC	DESCRIPTION
WRITELOTSC	Write Low-Order Track Step Counter. Generated by the Winchester Write Decoder (L62) to load the low-order step count into the Low-Order Step Counter (L104 and L105).
WSKCOMP	Winchester Seek Complete. Generated by the Winchester Seek Complete 1-Shot (L34) to initiate a Z80A interrupt.
WTG	Winchester Write Gate. Generated by the Winchester Interface Control Signal Generator (L119) to enable a write to the Winchester operation.
XA0-12	Microcontroller Instruction Address Bus. Provides instruction addresses to the PROM instruction storage area.
ZBA0-3	Z80A Buffered Address Bits. Buffered from Z80A address bits A0-3 by Z80A Address Bus Buffer L99.
ZD0-7	Z80A Buffered Data Bus. Buffered from the Z80A data bus (D0-7) by RMU-RCU Data Transceiver L149.

PART 3: IWS SIGNAL MNEMONICS

MNEWMONIC	DESCRIPTION
AMREQ	Advance Memory Request: This signal is generated by either the IWS Z80A or the 50BUS whenever they require access to memory.
BC	Blanking Control: Force the screen to blank between character and during horizontal and vertical retrace time.
BEPPER	This signal causes the bepper on the keyboard to activate.
BFS	Buffered Font Select: When this signal is active the Font memory is selected to transfer of data.
CBC	Cursor Blinking Control: Causes the cursor to blink.
CCC	Column Counter Clear: This signal is used to clear the column counter. It is generated when the row counter reaches counts 0 and 23 with the coulmn timing counter reaching 99.
CCL	Column Counter Load: This signal is use to load the column counter.
CLICKER	This signal causes the clicker on the keyboard to activate.
DT89	This clock is active at the end of each character display. The rising edge of DT89 is used internally by the gate array to generate specific timing relationships.
HIC	High Intensity Control: When this signal is low the bit being displayed will be highlighted.
HS	Horizontal Sync: This signal controls when the electron beam returns to the left side of the screen.
L8, L9	Line 8 and 9: These signals indicate that the display is on the last two lines of a character so that underlining or cursor operation can take place.
LC0 - LC3	Line Counter output to the Font memory.

PART 3: IWS SIGNAL MNEMONICS (cont.)

MNEWMONIC	DESCRIPTION
LDT	Load Data Time: This signal indicates when data is loaded from the font memory into the parallel to serial shift register.
PCS	Primary Character Set: When this signal is high it indicated the primary character set is selected.
R0 - R4	Row Address Counter output to the Character/Control memory.
SUBSC	Subscript: When this signal is active the character being displayed will be Subscripted.
SUPSC	Superscript: When this signal is active the character being displayed will be Superscripted.
UC	Underline Control: When this signal is active the character being displayed in underlined.
VS	Vertical Sync: This signal indicates when the electron beam return to the upper left hand corner of the screen.
WCHAR	Write Character: When this signal is active the Charcter Memory is accessed for writing data to it.
WCNTL	Write Control: When this signal is active the Control memory is access for a write operation.
WSPO	Workstation Power On: When this signal is high the workstation has been powered on.

APPENDIX

C

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L19	Random Access Memory Chip. (1B10)
L20	Random Access Memory Chip. (1B11)
L21	Random Access Memory Chip. (1B12)
L22	Random Access Memory Chip. (1B12)
L23	Memory Address Multiplexer (Low Byte). Directs the low address byte (A0-7) into memory when the MUX signal is inactive. (1C14)
L24	Memory Address Multiplexer (High Byte). Directs the high address byte (A0-15) into memory when the MUX signal is active. (1A14)
L27	Memory Parity Generater/Checker. During memory write opera- tions, L27 samples data bits D0-7 and places even parity data into memory. During memory read operations, L27 checks memory parity against the even parity established when the word was written. (1E3)
L29	Data Transceiver Control Flipflop (1Q output). Controls the direction of data flow to and from the Z80A. (1G10)
L29	Memory Parity Error Flipflop (2Q output). Generates the Memory Error (/ME) signal which asserts the Z80A to cause an NMI. (1E2)
L30	Diagnostic PROM Control Flipflop (1Q output). Upon receipt of /FF0E with D7 = 0, L30 disables PROM. Disabling PROM prevents it from overlaying the 0000-1000H RAM space during diagnostics. (1E5)
L30	Diagnostic Memory Parity Control Flipflop (2Q output). Upon receipt of /FF0D with D7 = 1, L30 establishes bad parity for memory during memory write operations. (1D4)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L31	Wait State Insert Flipflop (1Q output). Generates PWAIT, causing a single WAIT state to be inserted in Memory Mapped I/O operations. (1K6)
L31	FDC /Phi-A Clock Generating Flipflop (2Q output). Divides an 8-MHz signal to generate the /Phi-A (4-MHz) signal used for FDC Write and Z80A WAIT State Synchronization. (1K2)
L32	1/2Phi Clock Generating Flipflop (1Q output). Divides the Y1-generated 16-MHz signal to create the 1/2Phi (8-MHz) signal which synchronizes the generation of Z80A Data Bus direction control signals and the RAS signal. (1I5)
L32	Phi-Z and Phi-ZC Clock Generating Flipflop (2Q output). Divides an 8-MHz signal to create the Phi-Z and Phi-ZC (4-MHz) signals for use as the Z80A and CTC clocks. (1I3)
L35	Refresh Request Flipflop (1Q output). Generates Early Refresh (/ERFSH) signal upon the arrival of all /M1B op-code fetch signals on its clock inputs. /ERFSH travels to the Refresh A7 Bit Control Flipflop to enable the Synthetic Refresh A7 Bit. (3J12)
L35	Memory Access Operation Pending Flipflop (2Q output). If /MREQ or /M1 is active, L35 generates a high signal to assert the RAS Generating Flipflop and begin the RAS/CAS generation cycle. (3K13)
L37	Input Memory Data Buffer. Buffers data in memory write operations from the D0-7 Bus to the MD0I-MD7I (Memory Data Input) Bus. (1D10)
L39	Output Memory Data Latch. Latches data in memory read opera- tions from the MD0O-MD7O (Memory Data Output) Bus to the D0-7 Bus. (1D10)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L40	Shift Control Flipflop (1Q output). Generates shift signal that places the Transmit Shift Registers in the shift mode. (3C6)
L40	Synthetic Refresh A7 Bit Latch (2Q output). Latches the Synthetic Refresh A7 Bit generated by L69 and presents the bit to the A7 Multiplexer. (3I12)
L45	Memory Parity Bit Buffer. Buffers the Memory Parity Bit in read operations from the Memory Data Parity Output (MDP0) signal into the PAROUT signal. (1A6)
L47	Power-Up Diagnostic PROM. Contains 4k bytes of Power Up (IPL) and Diagnostic Programs that are addressed by Address Bits A0-11. PROM-resident programs overlay the lower 4k bytes of RAM (0000-1000H). (1H6)
L48	PROM Data Buffer. Buffers PROM-resident data (O0-7) onto the Data Bus (D0-7) when PROM is enabled. (1G5)
L49	Software Configuration Switch Buffer. Transmits data from the Software Configuration Switches to the D0-7 Data Bus upon receipt of the /FF05 command. (1H8)
L50	MUX Signal Generator (1Q output). Generates the MUX signal which asserts the Memory Address Multiplexer to switch in the high address byte needed when CAS signals are generated. (3J8)
L50	CAS Signal Generator (2Q output). Generates the CAS signals which proceed to memory to strobe the column address. (3J7)
L52	Refresh A7 Bit Control Flipflop (1Q output). During memory operations, L52 selects either the Synthetic Refresh A7 Bit or the Z80A-generated A7' Bit to be placed on the Z80A Address Bus as the A7R bit. (3I11).

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L52	Diagnostic Terminal Count Flipflop (2Q output). During diagnostics, L52 generates the Terminal Count signal upon receipt of the /WFF0B command with D6 = 1. Normally, the RMU generates the Terminal Count signal under RCU control during Z80A DMA data transfers when the Z80A has either transmitted or received all the data. (2F12)
L53	RAS/CAS Timing Shift Register. Generates signals that initiate creation of the WRITE signal and then clear the RAS/CAS generation logic. (3I8)
L54	Write Signal Generator (1Q output). Generates the Write signal which determines whether a memory read or a memory write operation is performed. (3I11)
L54	RAS Signal Generator (2Q output). Generates RAS signals which proceed to memory to strobe the row address. RAS also initiates the RAS/CAS/WRITE timing and MUX-CAS signal generation cycles. (3K11)
L55	FDC Write Signal Generator (1Q output). Generates WRITE to place the FDC in the write mode of operation. (2C8)
L55	FDC Reset Flipflop (2Q output). Resets the FDC upon receipt of the /FF0A command. Two /FF0A writes must be performed to reset the FDC under Z80A control. The first /FF0A signal turns on the Reset Flipflop and the second turns it off. Reset pulse width must be at least 10 us. (2E13)
L56	Transmit Serial Data Shift Register. Data (including Start, Stop, and Parity Bits) is shifted into serial form by Transmit Serial Data Shift Registers L56, L57, and, L58. (3B1)
L57	Transmit Serial Data Shift Register. See L56. (3B3)
L58	Transmit Serial Data Shift Register See L56. (3B4)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L59	Transmit Bit Counter. Counts the 11 bits (Start Bit, eight Data Bits, Parity Bit, and Stop Bit) contained in each trans- mitted word and generates a Carry Out (RCO) signal upon receipt of each complete word. (3C6)
L60	Transmit Shift Frequency Generator. Generates the 233-ns (4.275-MHz) clock signal that shifts data out. (3C8)
L61	Byte Request Flipflop (1Q output). Generates the Byte Request (/BYTE REQ) signal to indicate that the SDL transmit logic needs another byte of data. (3C4)
L61	Transmit Clear Flipflop (2Q output). Clears the transmit logic at the end of an SDL transmit operation by activating the clear pins of the Shift Registers and the Bit Counter. (3C3)
L69	Dead Man Timer Flipflop (1Q output). Generates the Deadman Interrupt (DMI) signal when the Floppy Disk Drive does not respond to a command within 540 ms after the FDC issues the command. (2D11)
L69	Synthetic Refresh A7 Bit Generator (2Q output). Determines the state of the Synthetic Refresh A7 bit used for 256-Row Address Refresh. (3I13)
L73	Transmit Serial Data Parity Generator. Generates a parity bit (ODDPAR) for transmitted data (TDATA0-7). TDATA0-7 always has odd parity. (3B5)
L74	Transmit Serial Data Bus Buffer. Buffers data transmitted from the 50BUS (bits 50BD0-7) to the TDATA0-7 Bus. (3A7)
L75	Serial Received Data Parity Checker. Checks the parity (odd) of data received via the Serial Data Link logic. (3A11)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L76	Serial Received Data Shift Register. Assembles SDL received data into an 8-bit word to be shifted onto the RDATA0-7 Data Bus. (3A12)
L77	Serial Data Link Receive Parity Flipflop (1Q output). Gener- ates the Received Parity (/RECD PAR) status signal to indi- cate that the received data has bad parity. (3C9)
L77	Serial Data Link Receive Data Latch (2Q output). Uses the 4.275-MHz signal to clock data to the Serial Received Data Shift Register. (3A13)
L78	Serial Data Link Start Bit Detect. Checks for the presence of a Start Bit to determine whether a legal word is present to be received. (3F13)
L80	Memory Mapped I/O Decoder. Decodes Address Bits A0-3 into MMI/O Port commands /FF00-/FF0F. L80 is enabled by signals produced by decoding Address Bits A4-15 through L64 and L95. (1K9)
L82	Z80A Counter Timer Chip (CTC). L82 is a programmable, 4-channel device that provides counting and timing functions for the RMU. It prioritizes and generates maskable inter- rupts and acts as a general purpose event timer. (3K3)
L83	Voltage Controlled Oscillator. Generates a frequency deter- mined by the error voltage applied to its input. (2J2)
L84	Data Recovery Logic Op Amp. Creates an error voltage output determined by the signals it receives on its inputs. (2J4)
L85	Phase/Frequency Detector. Detects FDWCK (FDD Write Clock) and compares its phase and frequency with the phase and frequency of the VCO-generated signal. If the phases and/or frequencies are unequal, L85 issues error signals. (2J6)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L87	FDC Data Transceiver. Buffers the D0-7 Bus to and from the FDC Data (FDCD0-7) Bus. (2D7)
L88	RCU-FDC Data Transceiver. Passes data between the FDC Bus and the 50BD Bus when the necessary enabling and direction control signals are present. (2H10)
L89	RCU-Memory Data Transceiver. Passes data between the 50BD Bus and the D0-7 Bus when the necessary enabling and direc- tion control signals are present. (2J10)
L90	Received Data Buffer. Buffers received data (RDATA0-7) onto the 50BUS upon receipt of the /RECD DATA enabling signal. (3A9)
L91	Serial Data Receive Control Flipflop (1Q output). Generates the /BYTE RECD signal to indicate that the SDL has received a byte of data. (3D9)
L91	Enable Sample Flipflop (2Q output). Generates ENABLE SAMPLE, which asserts the Receive Shift Frequency Generator and the Receive Bit Counter. (3E11)
L92	Serial Data Link Receive Bit Counter. Counts the 9 bits (eight data bits and a Parity Bit) contained in each received word and generates a Carry Out (RCO) signal upon each 9th bit counted. (3C12)
L93	Serial Data Link Receive Shift Frequency Generator. Gener- ates a 233-ns (4.275-MHz) clock signal which shifts data into the Serial Data Link. (3C13)
L96	Control Line Driver. When enabled by the inactive /BUSAK signal, L96 drives the Z80A's control outputs. (1E12)
L97	Data Recovery Logic Frequency Divider (1Q output). Divides the VCO-generated frequency and sends the resulting frequency to the Phase/Frequency Detector. (2H7)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L97	Read Window Signal Generator (2Q output). Generates the READ WINDOW signal. Synchronized data (READ DATA) from the FDD is read into the FDC when the read window is open (ie, READ WINDOW is active). (2H4)
L100	True File Ready 1-Shot (Q1 output). Generates True File Ready Signal to indicate that the Floppy Disk Drive is ready to perform an operation (ie, the disk is loaded and spinning, the disk door is closed, and the drive is selected). (2A10)
L100	Dead Man Timer 1-Shot (Q2 output). Issues the Dead Man Interrupt (DMI) signal if the FDC does not complete a command within 540 ms after receiving the /FF0C command. (2D12)
L101	Floppy Disk Controller (FDC). Executes the commands that control the Floppy Disk Drive.
L101A	Floppy Disk Drive Status Register. When read by the /RFF0B command, L101A provides FDD status information to bits D4-7 of the Data Bus. (2D9)
L102	Read Data Signal Generator (2Q output). Generates the synch- ronized READ DATA signal. Synchronized data (READ DATA) from the FDD is read into the FDC when the read window is open (ie, READ WINDOW is active). (2H5)
L103	Data Recovery Logic Data Acceptance Latch (1Q output). When enabled by the VCO synchronizing signal, L103 accepts data (D READ DATA) from the FDD and passes this data to the data recovery logic. (2I8)
L103	Diagnostic DMA Acknowledge Flipflop (2Q output). During diagnostics, L103 responds to the /WFF0B command with D7 = 1 by generating the DMA Acknowledge (DACK) signal. Normally, the RMU generates DACK under RCU control in response to a DMA Request from the FDC. (2F11)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L105	Floppy Disk Drive Status Register. When read by the /RFF0B command, L105 provides FDD status information to bits D0-3 of the Data Bus. (2C11)
L107	Floppy Disk Drive Write Clock Generator. Generates the Floppy Disk Write Clock (FDWCK) for the Floppy Disk Controller and the data recovery logic. (2F14)
L109	Serial Data Link Transmit Flipflop (1Q output). Issues the Transmit signal, which enables the SDL transmit logic by deactivating the signals asserting the clear pins of L56-59. (3F10)
L109	Serial Data Link Receive Flipflop (2Q output). Issues the Receive signal to the SDL receive logic to instruct and enable the logic to receive data. (3F9)
L110	Serial Data Link Command Decoder. Decodes 50BUS Address Bits 50BA0-2 to yield one of seven Serial Data Link commands. (3G13)
L114	Z80A Processor. The 4-MHz Z80A Processor is the main proces- sor of the Resource Management Unit. (1I13)
L115	Z80A Data Transceiver. Controls data flow to and from the Z80A. Separate enabling and direction control logic controls the Data Transceiver. (1H13)
L116	Write Data/Precompensation Signal Generator. Selects either early, nominal, or late Write Data (WR DATA) signals. (2D4)
L117	Write Data/Precompensation Sequencer. Generates early, nominal, or late WR DATA (Serial Data to the FDD) signals, which are then transmitted to the FDD via Write Data Pre- compensation Signal Generator L116. (2E5)
L118	FDD Motor Control Flipflop (1Q output). Turns the FDD motor on and off. L118 issues MOTOR ON in response to the /WFF0B command with D0 = 1. (2C13)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L118	Floppy Disk Drive Select Flipflop (2Q output). Generates the Disk Select (DSI) signal, in response to the /WFF0B command with D1 = 1, to select the FDD for an operation. (2C14)
L119	FDC Control Signal Buffer. Controls incoming and outgoing FDC control signals. The /RW/SEEK signal from pin 39 of the FDC establishes the operative mode of L119: low /RW/SEEK sets L119 for a read or write operation, and high /RW/SEEK sets L119 for a seek operation. (2B4)
L120	Loopback Control Flipflop (1Q output). Places the SDL in a loopback mode for diagnostic testing. The loopback capabil- ity is not used in any current diagnostic routines but can be implemented when needed. (3E9)
L120	Door Disturbed Flipflop (2Q output). Generates the /DOORDIST signal to indicate that the door to the Floppy Disk Drive has been disturbed (ie, opened). (2A13)
L121	Serial Data Link Receive Channel Selector. Selects one of four channels to receive data. The signals that control channel selection are generated by the channel select logic. (3F6)
L124	Serial Data Link Transmit Channel Selector. Selects one of four channels for data transmission. The signals that con- trol channel selection are generated by the channel select logic. (3G6)
L125	Serial Data Link Channel Select Flipflops. Generates the signals sent to the Receive or Transmit Channel Selector to select the proper channels. (3G8)
L126	Channel Select Data Buffer (1Y output). Buffers the Channel Select Data Nibble into the SDL channel select logic. (3H10)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L126	Serial Data Status Register (2Y output). When commanded by the /STATUS RD command from the SDL Command Decoder, L126 places four status signals onto 50BD0-3 . (3A8)
L127	RCU-Memory Enabling Flipflop (1Q output). Generates a signal from pin 6 that enables Address Buffers L129 and L144 and RCU-Memory Data Transceiver L89 to move data between the RCU and memory via the 50BUS . Also sends 50BBUSACK to the 8X305 Microcontroller (from pin 5). (2K10)
L127	No Data Flipflop (2Q output). Generates the /NO DATA signal to indicate that an SDL receive operation was commanded and initiated, but the data stream was interrupted during the operation. (3H1).
L129	50BUS High Byte Address Buffer. During RCU memory access operations, L129 provides a high address byte from the 50BUS to the Z80A Address Bus. (2K13)
L130	Z80A High Byte Address Buffer. Upon receipt of an inactive BUSAK signal, L130 provides a high address byte from the Z80A high address outputs to the Z80A Address Bus. (1I13)
L131	Power Up Voltage Comparators. When power is first applied, the comparators monitor the 5-V, -5-V, and 12-V levels to ensure that the proper levels are reached before the Z80A is placed in an operative mode. (2F3, 2F5, 2F7, and 2F8)
L136	Serial Data Link Receiver (Channels 1 and 2). Receives four data inputs (TNC-BNC) from the RMU board and converts this data into two distinct serial data channels (/DCH0-1). (3F7)
L137	Serial Data Link Driver. Drives the Serial Data Link Ports for channels 1 and 2. Converts the serial data it receives into a form that can be transmitted on coaxial cables. (3G4)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
L138	Serial Data Link Driver. Drives the Serial Data Link Ports for channels 3 and 4. Converts the serial data it receives into a form that can be transmitted on coaxial cables. (3E4)
L139	Serial Data Link Receiver (Channels 3 and 4). Receives four data inputs (TNC-BNC) from the RMU board and converts this data into two distinct serial data channels (/DCH2-3). (3E7)
L140	No Data Timeout 1-Shot (Q1 output). After an 86-us delay, L140 generates a signal that causes L127 to generate the /NO DATA signal (unless L127 has been cleared previously by the deactivated Receive signal). (3H2)
L144	50BUS Low Byte Address Buffer. During RCU memory access operations, L144 provides a low address byte from the 50BUS to the Z80A Address Bus. (2I13)
L145	Z80A High Byte Address Buffer. Upon receipt of an inactive /BUSAK signal, L145 provides a high address byte from the Z80A high address outputs to the Z80A Address Bus. (1J13)
SW1	IPL Pointer Switch. Determines which disk drive will be used for Initial Program Load (IPL): when D7 = 0, the Floppy Disk Drive is used for IPL, and when D7 = 1, the Winchester Disk Drive is used for IPL. (1I11)
SW2	Restart Control Switch. Activating SW2 when the operating system has control traps the Z80A to the Master Debugger routine (if the system is configured with the Master Debugger). Activating SW2 during Test 1 (LED Test) of the Power-Up Diagnostics causes the succeeding tests to be omitted and the bootstrap routine initiated. (1K14)
SW3	Software Configuration Switches. Eight-bit switch bank used to select various software configurations defined by the switch settings. (1G10)

PART 1: Resource Management Unit (RMU)

CHIP	DESCRIPTION
VR1	Data Recovery Logic Voltage Regulator. Provides an isolated 5 V to the data recovery logic and to all 50BUS-connected boards. (2K7)
VR2	Voltage Regulator. Provides -5 V to the SDL Receivers. (3J2)
Y1	Master Clock Generator. Generates the 16-MHz timing signal (CK) from which all other timing signals are derived. (1J6)
Y2	Serial Data Link Clock Generator. Generates the 34.20-MHz timing signal used in the SDL to generate the receive and transmit clock signals. (3D14)

APPENDIX C: CHIP LIST

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L1	Data Separator Flipflop (1Q output). Part of the Data Recovery Circuit used to help separate data pulses from clock pulses. (3C11)
L1	Data Separator Flipflop (2Q output). Part of the Data Recovery Circuit used to help separate clock pulses from data pulses. (3B11)
L2	Mincount Flipflop. Generates the MINCOUNT signal to enable the Address Mark Detector when the Mincount Counters (L30) have detected eight contiguous bytes of zeros in the incoming data stream. (3D12)
L5	Address Mark Detect Delayed Flipflop. Generates the AMD Delayed (AMDDLY) signal to enable the ECC Checker Circuit by releasing the clear signal on the ECC Read Control Shift Register. (3D7)
L6	ECC Shift Register. Together with L21 and L32, shifts data in order to generate three ECC bytes corresponding to the data written. Also checks this information during a read operation. (3K11)
L7	ECC Read Control Shift Register. Monitors the /AMDDLY signal in order detect the address mark. When the address mark is detected, L7 generates a signal which enables the ECC Shift Registers so that they can accept the data field that follows the address mark and the FBH byte. (3J13)
L13	ECC Output Control Shift Register. Generates a signal that switches the Control Multiplexer to select the ECC Circuit's output as the data stream input. (3K12)
L14	Dead Man Timer. Generates a carry signal that causes a Z80A interrupt if 16 index marks are detected when the Read/Write (RW) signal is active. (2F2)
L16	Data Separator Flipflop (1Q output). Part of the Data Recovery Circuit used to help separate clock pulses from data pulses. (3B10)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L16	Data Separator Flipflop (2Q output). Part of the Data Recovery Circuit used to help separate clock pulses from data pulses. (3B9)
L17	Maxcount Flipflop (1Q output). Generates a Maxcount signal to clear the Data Recovery Counters (via L18 and L4) after they have counted 16 contiguous bytes of zeros. (3B13)
L17	Loop Reset Flipflop (2Q output). Generates the Loop Reset (/LPRS) signal, which clears the Data Recovery Circuit (via L60 and L70). (3B14)
L19	Control Multiplexer. Selects either read or write data and clock inputs to be used as data and clock inputs for the ECC Circuit. (3B6)
L21	ECC Shift Register. Together with L6 and L32, shifts data in order to generate three ECC bytes corresponding to the data written. Also checks this information during a read operation. (3I11)
L23	ECC Write Control Shift Register. Monitors the NRZW and SKPEN signals to detect the FBH byte that precedes the data field. When FBH is detected, L23 generates a signal to enable the ECC Shift Registers so that they can accept the data field following the FBH byte. (3J14)
L25	Command Bus Request Flipflop. Generates the /CMDBUSREQ signal which is sent to the RMU to request bus control. (1A8)
L27	Data Separator Flipflop (1Q output). Part of the Data Recovery Circuit used to help separate data pulses from clock pulses. (3D10)
L27	Data Separator Flipflop (2Q output). Part of the Data Recovery Circuit used to help separate data pulses from clock pulses. (3D9)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L29	Address Mark Detector. Searches for the address mark (A1H with the clock bit missing) in the incoming data stream. Once the address mark is detected, L29 generates the Address Mark Detect (AMD) signals. (3C8)
L30	Data Recovery Counters. Monitor incoming MFM data to count up to 16 contiguous bytes of zeros. If eight contiguous bytes of zeros are counted, the counters generate the MINCOUNT signal. If 16 contiguous bytes of zeros are counted, the counters issue a signal which indicates that the maximum count of zeros has been reached. (3D14)
L31	ECC Output Control Flipflop. Generates a signal that is gated with the WRITE signal to create the active Write ECC (/WECC) signal. /WECC selects the information to be passed through the ECC Output Multiplexer. (3K12)
L32	ECC Shift Register. Together with L6 and L21, L32 shifts data in order to generate three ECC bytes corresponding to the data written. Also checks this information during a read operation. (3H11)
L33	Byte Done Read Clear Flipflop. Generates a signal which asserts the Parallel to Serial Converter to deactivate the BDONER signal. (3I8)
L34	Winchester Seek Complete 1-Shot (Q1 output). Generates the Winchester Seek Complete (/WSKCMP) pulse to inform the RMU that the Winchester has completed a seek operation. (2G3)
L34	Control Unit Not Busy 1-Shot (Q2 output). Generates the Control Unit Not Busy (/CUBUSY) pulse to inform the RMU that the Microcontroller has completed an operation and is no longer busy. (2E4)
L38	Control Signal Decoder. Accepts Microcontroller-generated control signals and decodes them to generate RCU control signals. (2G11)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L39	PROM Chip. 2K x 8 storage device, four of which provide the 2K x 16 storage area for the Microcontroller's instruction set. (2E14)
L40	PROM Chip. See L39. (2J14)
L41	8X305 Microcontroller. Controls many OIS 50 functions. Operating at 200 ns per 16-bit instruction, the Microcontroller controls a series of peripheral devices which are attached to it by means of the 8-bit Interface Vector bus. (2G11)
L46	ECC Parity Generator. As a result of the summation inputs from the ECC Shift Registers, the Parity Generator serially generates three ECC bytes following the 256-byte data field. (3J9)
L47	Control Multiplexer. Selects either data or ECC information as outputs during Winchester read or write operations. (3J8)
L48	Index 1-Shot. Generates an active, 10-us Index 1-Shot (/IOS) signal to indicate that the index mark has been detected on the Winchester disk drive. (3E1)
L53	PROM Chip. See L39. (2C14)
L54	PROM Chip. See L39. (2G14)
L55	Phase Locked Loop Op Amp. Creates an error voltage output relative to the signals it receives on its inputs. (3E9)
L56	Voltage Controlled Oscillator. Generates a frequency determined by the error voltage applied to the input. (3E7)
L57	Phase Locked Loop Frequency Divider. Divides the VCO-generated frequency and sends the resulting frequency to the Phase/Frequency Detector. (3F5)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L58	Step Pulse 1-Shot (Q1 output). Generates the active 6-us /STEP signal that asserts the Winchester to step the head in the proper direction. (3C2)
L58	Step Pulse Rate 1-Shot (Q2 output). Generates a 25-us step rate pulse that asserts the Step Pulse 1-Shot (L58) to generate an active 6-us /STEP signal every 25 us. (3D2)
L61	Halt Enabling Flipflop (1Q output). Enables the Halt Generating Flipflop so that it can generates the /HALT signal to halt the Microcontroller. (3I1)
L61	Halt Generating Flipflop (2Q output). Generates the /HALT signal to halt the Microcontroller. (3I1)
L62	Winchester Write Decoder. Decodes address bits /RBA0-2 into one of eight possible Winchester Write commands. (2D4)
L66	Scratchpad RAM Chip. 256 x 4 storage device, two of which comprise the 256 x 8 Scratchpad RAM. The Microcontroller uses the scratchpad on the left bank as a temporary storage area when accessing either the PRF or SRF. (2J5)
L67	Scratchpad RAM Chip. See L66. (2H5)
L68	Left Bank Address Latch. Passes addresses from the /IV0-7 bus onto the Left Bank Address bus (/LBA0-7). Left bank addresses are used to address the scratchpad. (2I8)
L69	Microcontroller Data Transceiver. Passes data between the Microcontroller and the /IV0-7 bus. (2F10)
L75	Load Disk Write Data Flipflop (1Q output). Generates the signal that loads parallel data into the Parallel to Serial Converter. (3J4)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L75	Write Clock Flipflop (2Q output). Divides the 10-MHz clock input to generate the WCLK signal used to drive a Winchester write operation. (3G3)
L76	Data Buffer Read Control Flipflop (1Q output). Generates the /BUFFRD signal. /BUFFRD places the 4K x 8 Data Buffer in the read mode of operation. (2I3)
L76	Data Buffer Write Control Flipflop (2Q output). Generates the /BUFFWR signal. /BUFFWR places the 4K x 8 Data Buffer in the write mode of operation. (2I1)
L77	4K x 8 Data Buffer Decoder. Decodes address bits /RBA0-1 to generate one of four possible 4K x 8 Data Buffer control commands. (1K10)
L78	Winchester Read Decoder (1Y outputs). Decodes address bits /RBA0-1 to generate one of three possible Winchester read control commands. (2B4)
L78	50BUS Read Control Decoder (2Y outputs). Decodes address bits /RBA0-1 to generate one of two 50BUS read control commands. (1G7)
L79	SRF Write Bank Decoder. Decodes addresses /RBA2-3 to generate one of three SRF write control commands (Write Bank 1, Write Bank 2, or Write Bank 3). Each of these commands asserts enabling pins on two Status Register File chips. (2F6)
L80	Right Bank I/O Decoder. Decodes addresses /RBA4-6 to generate one of seven I/O commands. Each of the seven commands enables one of the seven I/O ports functions. (2E6)
L83	Scratchpad Data Output Buffer. Passes data from the scratchpad onto the /IV0-7 bus. (2J4)
L84	PRF Data Output Buffer. Passes data from the PRF Data Out (PDO0-7) bus onto the /IV0-7 bus. (2C11)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L85	Right Bank Address Latch. Passes addresses from the /IV0-7 bus onto the Right Bank Address (/RBA0-7) bus. Addresses /RBA0-7 are decoded to create I/O command control signals. (2G8)
L87	Phase Locked Loop Phase/Frequency Detector. Detects the Write Clock (WCLK) signal and compares its phase and frequency with the phase and frequency of the VCO-generated signal. If the phases and/or frequencies are unequal, L87 issues error signals. (3F10)
L88	MFM Data Input Flipflop (1Q output). Accepts MFM-encoded data and passes that data onto the Phase Locked Loop circuit. (3E11)
L88	Read Data Signal Generator (2Q output). Uses the center frequency provided by the Phase Locked Loop Circuit to convert the incoming (from the Winchester) data stream into a synchronized data stream. The synchronized data stream is sent to the Data Recovery Circuit where the data and clock pulses are separated. (3F13)
L89	MFM Data Receiver. When enabled by the active Drive Select (/DRS) signal, L89 accepts MFM-encoded data and passes that data onto the MFM Data Input Flipflop. (3F13)
L92	MFM Generator. Accepts and converts NRZW data (WDATA) to MFM data (WDATAP), generates write precompensation control signals, and strips the clock bit from the A1H address mark byte. (3H4)
L93	4K x 8 Data Buffer Bank Select Flipflop. Selects and synchronizes (with MCLK) the bank select signal which chooses either L109 or L110 for a 4K x 8 Data Buffer read or write operation. (1H8)
L90	Write Precompensation Driver. Drives the WDATAP serial data stream into the Write Precompensation Device (L138). Also drives the Winchester's DRIVESLCT signal. (2J2)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L95	Winchester to 4K x 8 Data Buffer Data Control Flipflop (1Q output). Generates the EDDTB signal which enables data to move from the Winchester bus, through L108, onto the 4K x 8 Buffer data bus (BD0-7). (2D1)
L95	4K x 8 Data Buffer to Winchester Data Control Flipflop (2Q output). Generates the EBDTD signal which enables data to move from either the /IV0-7 bus or the BD0-7 bus, through L124 or L142, and onto the Winchester buffered data bus (WBD0-7). (2C1)
L98	Z80A I/O Decoder. Generates one of four I/O command signals in response to RMU-generated MMIO commands. These signals control the Z80A's access to the SRF and PRF on the RCU board. (1J13)
L99	Z80A Address Bus Buffer. Z80A address bits A0-3 are passed through L99 to generate the Z80A inverted buffered address bus (/ZBA0-3). (1H13)
L100	Parameter Register File Chip. 16 x 4 storage device, two of which comprise the 16 x 8 Parameter Register File. (1C10)
L101	Parameter Register File Chip. See L100. (1C8)
L102	PRF Address Multiplexer. Passes addresses from either the Right Bank (/RBA0-3) or the Z80A (/BA0-3) through to the PRF (depending upon the condition of the CMDBUSREQ signal). (1D10)
L103	SRF Read Bank Decoder. Generates one of the Register Bank Enable (/RB1-3) signals to enable a PRF register bank (two chips) upon receipt of RMU-generated commands. (1I12)
L104	Low-Order Step Counter. Together with the High-Order Step Counter, L104 decrements the initial programmed step count as each STEP signal is generated. (3D4)
L105	Low-Order Step Counter. See L104. (3E4)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L106	High-Order Step Counter. Together with the Low-Order Step Counters, decrements the initial programmed step count as each STEP signal is generated. (3C4)
L107	Serial to Parallel Converter. Converts incoming serial data (from Winchester) into a parallel format using the separated DCLK signal from the Address Mark Detector as the shift clock. (3J7)
L108	Winchester to BD0-7 Bus Data Buffer. Passes incoming data (from the Winchester) onto the BD0-7 bus. (3K6)
L109	4K x 8 Data Buffer Chip. 2K x 8 storage device, two of which comprise the 4K x 8 Data Buffer. The 4K x 8 Data Buffer is used as a data storage area during all block data (256-byte) moves between any two boards of the OIS system. (1K7)
L110	4K x 8 Data Buffer Chip. See L109. (1H7)
L111	RMU-RCU Data Buffer Direction Control Flipflop (1Q output). Controls data direction through RMU-RCU Data Transceiver (L149). Direction depends upon the condition of the /RDPAR (Read PRF) or /STATUS signal. (1H12)
L111	50BUS Data to Data Buffer Control Flipflop (2Q output). Generates the Enable 50BUS Data To Buffer (/E50BDTB) signal, which enables data from the 50BUS Buffered Data bus (50BD0-7), through L127, onto the BD0-7 bus. (2E1)
L112	50BUS Data Control Flipflop (1Q output). Generates the Buffer Data Enable (/BUFFDATAEN) signal that enables data from the BD0-7 bus, through L128, onto the 50BD0-7 bus. (1E5)
L112	50BUS Data Control Flipflop (2Q output). Generates the 8X305 Data Enable (/8XDATAEN) signal that enables data from the /IV0-7 bus, through L145, onto the 50BD0-7 bus. (1E4)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L114	50BUS Write Control Decoder. Decodes address bits /RBA0-2 into one of eight 50BUS write control commands. (1F7)
L115	PRF to RMU Data Buffer. Passes data from the PRF Data Out bus (PDO0-7) onto the Z80A buffered data bus (ZD0-7). (1F10)
L116	RMU to PRF Data Buffer. Passes data from the Z80A buffered data bus (ZD0-7) onto the PDI0-7 (PRF Data In) bus. (1F9)
L117	Status Register File Chip. 4-byte x 4-bit storage device, six of which make up the 12-byte x 8-bit Status Register File (SRF). The SRF is used as common ground for status information passed from the RCU to the RMU. (1F11)
L118	Status Register File Chip. See L117. (1F13)
L119	Winchester Interface Control Signal Generator. When clocked by the active /WRITELOGICCNTRL signal, L119 generates Winchester interface control signals that correspond to the command received from the IV0-7 bus. (3G7)
L120	IV Bus Inverter. Provides inverted IV bus signals needed to turn on control signals from L119 following a power-up operation. (3G8)
L121	Winchester Disk Status Signal Buffer. When enabled by the active /READDISKDATA signal, L121 passes the condition of the Winchester Status Signals onto the /IV0-7 bus. (3H12)
L122	Drive Device Type Buffer (1Y output). When enabled by the /READCNTRLSTATUS signal, L122 reads the Winchester device type from SW1 onto the /IV4-7 bus. (3G12)
L122	Control Status Register (2Y outputs). When enabled by the active /READCNTRLSTATUS signal, L122 reads primary status information onto the /IV0-3 bus. (3B8)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L123	Winchester to /IV0-7 Bus Data Buffer. Passes incoming data (from the Winchester) onto the /IV0-7 bus. (3I6)
L124	/IV0-7 to WBD0-7 Bus Data Buffer. Passes outgoing data (to the Winchester) from the /IV0-7 bus onto the WBD0-7 bus. (3I5)
L125	4K x 8 Data Buffer Low-Order Address Counter. Loads low-order initial address bits from /IV0-3 onto BA4-7. Initial addresses are incremented to generate the succeeding addresses. (1I8)
L126	4K x 8 Data Buffer Low-Order Address Counter. Loads low-order initial address bits from /IV4-7 onto BA0-3. Initial addresses are incremented to generate the succeeding addresses. (1K8)
L127	50BD0-7 to BD0-7 Bus Data Buffer. Passes data from the 50BD0-7 bus onto the BD0-7 bus. (1K5)
L128	BD0-7 to 50BD0-7 Bus Data Latch. Passes data from the BD0-7 bus onto the 50BD0-7 bus. (1I5)
L129	50BD0-7 to /IV0-7 Bus Data Buffer. Passes data from the /50BD0-7 bus to the /IV0-7 bus. (1G3)
L130	50BUS Read/Write Signal Generating Flipflop (1Q output). Generates the active /R/W signal if /IV1 is active when L130 is clocked by the active CNTRL signal. (1A5)
L130	50BUS Bus Request Signal Generating Flipflop (2Q output). Generates the active /BUSREQ50B signal if /IV2 is active when L130 is clocked by the active CNTRL signal. (1B5)
L131	50BUS Terminal Count Signal Generating Flipflop (1Q output). Generates the active /TC signal if /IV5 is active on L131's D-input when L131 is clocked by the active SP FUNC signal. (1B5)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L131	50BUS Reset Signal Generating Flipflop (2Q output). Generates the active /RESET50B signal if /IV6 is active on L131's D-input when L131 is clocked by the active SP FUNC signal. (1C5)
L132	50BUS Request Signal Generating Flipflop (1Q output). Generates the active /REQUEST signal when clocked by the active REQ signal. (1D4)
L132	50BUS Status Signal Generating Flipflop (2Q output). Generates the active /STATUS50B signal if /IV4 is active on L132's D-input when L132 is clocked by the active SP FUNC signal. (1D5)
L133	PRF Data Input Buffer. Passes data from the /IV0-7 bus onto the PRF Data In (/PDI0-7) bus. (1G9)
L134	Status Register File Chip. See L117. (1D11)
L135	Status Register File Chip. See L117. (1D13)
L136	Winchester Disk Drive Program Signal Generator. When clocked by the active WRITEDRPRG signal, L136 generates Winchester programming signals corresponding to the command received from the IV0-7 bus. (3F4)
L138	Write Precompensation Device. L38 generates the write precompensation early, nominal, or late data streams from the nominal WDATAP signal it receives as an input. (2K1)
L139	MFM Data Transmitter. Transmits MFM-encoded data upon receipt of that data from the MFM Data Write Gates. (3G1)
L140	MFM Data Write Gates. Gates outgoing (to the Winchester) MFM-encoded data with the proper write precompensation control signals generated by the MFM Generator. (3H3)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L141	Parallel to Serial Converter. Converts outgoing (to the Winchester) parallel data into a serial format using the Write Clock (/WCLK, 1.6 us per byte) signal to shift the data into the NRZW data stream. (3K3)
L142	BD0-7 to WBD0-7 Bus Data Latch. Passes outgoing data (to the Winchester) from the BD0-7 bus onto the WBD0-7 bus. (3K5)
L143	4K x 8 Data Buffer High-Order Address Counter. Loads high-order initial address bits from /IV5-7 onto BA8-10. Initial addresses are incremented to generate the succeeding addresses. (1H8)
L143A	50BUS Low-Order Address Counters. Loads low-order initial addresses from /IV4-7 onto 50BA0-3. Initial addresses are incremented to generate the succeeding addresses. (1D2)
L144	50BUS Control Signal Buffer. Buffers 50BUS control signals onto the 50BUS. (1B4)
L145	/IV0-7 to 50BD0-7 Bus Data Latch. Passes data from the /IV0-7 bus to the /50BD0-7 bus to bring data from the RCU board onto the 50BUS. (1G5)
L146	50BUS Device Select Chip. L146 generates the device select signal (from /50BSLCT0-7) corresponding to the code it receives from the /IV bus. Data from the /IV bus is inverted through L146; for example, device 0 is selected (active /50BSLCT0) if /IV7 is active. (1C2)
L147	50BUS Low-Order Address Counters. Loads low-order initial addresses from /IV0-3 onto 50BA4-7. Initial addresses are incremented to generate the succeeding addresses.(1E2)
L148	50BUS High Address Latch. Loads high-order initial addresses from /IV0-7 onto 50BA8-15. (1F2)

PART 2: Resource Control Unit (RCU)

CHIP	DESCRIPTION
L149	RMU-RCU Data Transceiver. Moves data between the Z80A data bus (D0-7) on the RMU and the Z80A buffered data bus (ZD0-7) on the RCU. (1I10)
L151	Status Register File Chip. See L117. (1C11)
L150	SRF Data Buffer. Passes data from the SRF Data Out bus (/SDO0-7) to the Z80A buffered data bus (ZD0-7). (1H10)
L151	Status Register File Chip. See L117. (1F11)
L152	Status Register File Chip. See L117. (1C13)
SW1	Winchester Disk Drive Device Type Switches. Switches are set to 3H for Winchester disk drive types used in OIS 40 or OIS 50 applications. (3G14)
VR1	Phase Locked Loop Voltage Regulator. Provides an isolated 5 V to the Phase Locked Loop Circuit. (3F7)
Y2	Write Clock Generator. Generates a 10.0-MHz timing signal which is divided by L75 to generate the write clock that drives Winchester write operations. (3H7)

PART 3: IWS SIGNAL CHIP LIST

CHIP	DESCRIPTION
L2	WL2632 Gate Array. This gate array control all of the timing for the display circuits.
L5	Lower Control Memory
L6	Upper Control Memory
L7	Control Character Decoder: This decoder generates control signals for the character being displayed.
L19	Cursor Blinking Timer. This timer control the on and off time of the cursor.
L22	Lower Character Memory
L23	Upper Character Memroy
L25	Column Address Multiplexor: These two chips select
L26	the column address from either the Z80A or the display circuits.
L29	Z80A IWS CPU.
L33	Display Timing Sequence Decoder. These two chips (L33 & L48) generate the timing signals used for loading and clocking data to the display circuits.
L35	Character to Z80A Output Data Buffer
L36	Character to Z80A Output Data Buffer
L37	Character to Display Output Data Buffer
L39	Row Address Multiplexor: These two chipsselect the
L40	Row address from either the Z80A or the display circuits.
L44	Superscript/Subscript Adder: This adder adds an offset to the forn address when either Superscript or Subscript is selected of display.
L48	See L33
L50	Control to Z80A Output Data Buffer

PART 3: IWS SIGNAL CHIP LIST

CHIP	DESCRIPTION
L51	Character Memory Input Data Buffer
L52	In Instruction Decoder
L55	Out Instruction Decoder
L59	Parity Generater/Checker
L63	Font Memory Chip
L64	Font Memory Chip
L65	Font Memory Chip
L69	Control Memory Input Data Buffer
L72	Column Counter: This two chips indicate the
L73	horizontal postion of the character being displayed.
L81	Font Memory Chip
L82	Font Memory Chip
L83	Font Memory Chip
L84	Character Serialization Register: This register in conjuction with L103 and L149 transfer the 10 bit Font memory data into a serial stream of data for the display.
L85	Font Address Multiplexor
L86	8031 Single Component 8-bit Microcomputer. This chip provides the interface between the Z80A and the keyboard.
L87	Keyboard Data Input Buffer
L88	Keyboard Data Output Buffer
L93	Write Delay Timer: This counter insrues that the Write Enable signal is not generated until the end of the CAS cycle.

PART 3: IWS SIGNAL CHIP LIST

CHIP	DESCRIPTION
L96	OUT Instruction Decoder
L100	Font Address Multiplexor
L101	Font Memory Chip
L102	Font Mmeory Chip
L103	See L84
L104	Font Address Multiplexor
L105	IN07 Switch Bank Buffer
L108	Synthetic A7 bit slect flipflop: During refresh this flipflop select the synthetic A7 bit instead of the normal A7 bit.
L108	Synthetic A7 bit generator: This flipflop determines the state of the synthetic A7 bit.
L112	Memory Data Input Buffer
L113	Memory Address Multiplexor
L114	Memory Address Multiplexor
L119	Keyboard Interface Instruction PROM
L124	Early Refresh Flipflop: This flipflop signals the begining of refresh.
L126	RAS Flipflop: When this flipflop is set the RAS cycle is in operation.
L126	SWMUX Flipflop: This flipflop swicth the Memory Address Mulitplexor between the RAS and CAS.
L127	CAS Flipflop: When this flipflopis set the CAS cycle is in operation.
L127	Write Enable Flipflop: During a write operation this flipflop will go set at the end of the CAS cycle.

PART 3: IWS SIGNAL CHIP LIST

CHIP	DESCRIPTION
L129	Dynamic RAM
L130	Dynamic RAM
L131	Parity RAM
L138	IN08 Switch Bank Buffer
L139	Z80A to Font Memory Data Buffer
L140	Font Memory to Z80A Data Bus Buffer
L141	50BUS Status register
L142	Memory Data Output Buffer
L143	Dynamic RAM
L144	Dynamic RAM
L145	Dynamic RAM
L149	See L84
L152	Power On Flipflop: This flipflop indicates the status of the on/off sense for the workstation.
L156	50BUS Control Signal Buffer
L157	50BUS Data Buffer
L159	50BUS Address Buffer Lower
L160	50BUS Address Buffer Upper
L162	Dynamic RAM
L163	Dynamic RAM
L164	Dynamic RAM
Y1	16 Mhz crystal used for Z80A timing and memory timing.
Y2	19.2 Mhz crystal use for display timing.

APPENDIX

D

SECTION 1 QUIZ
ANSWERS

1) See page 1-2

2) See page 1-3

3) See page 1-5

4) See page 1-5

5) See page 1-6

6) See page 1-6

7) See page 1-7

8) See page 1-8

9) See page 1-8

10) See page 1-1

SECTION 2 QUIZ
ANSWERS

1) See page 2-4

2) See page 2-6

3) See page 2-13

4) See page 2-15

5) See page 2-20

6) See page 2-22

7) See page 2-35

8) See page 2-41

9) See page 2-42

10) See page 2-51

11) See page 2-59

12) See page 2-69

SECTION 3 QUIZ
ANSWERS

1) See page 3-1

2) See page 3-1

3) See page 3-3

4) See page 3-4

5) See page 3-9

6) See page 3-13

7) See page 3-48

8) See page 3-51

9) See page 3-54

10) See page 3-60

SECTION 4 QUIZ
ANSWERS

1) See page 4-1

2) See page 4-7

3) See page 4-15

4) See page 4-17

5) See page 4-17

6) See page 4-18

7) See page 4-18

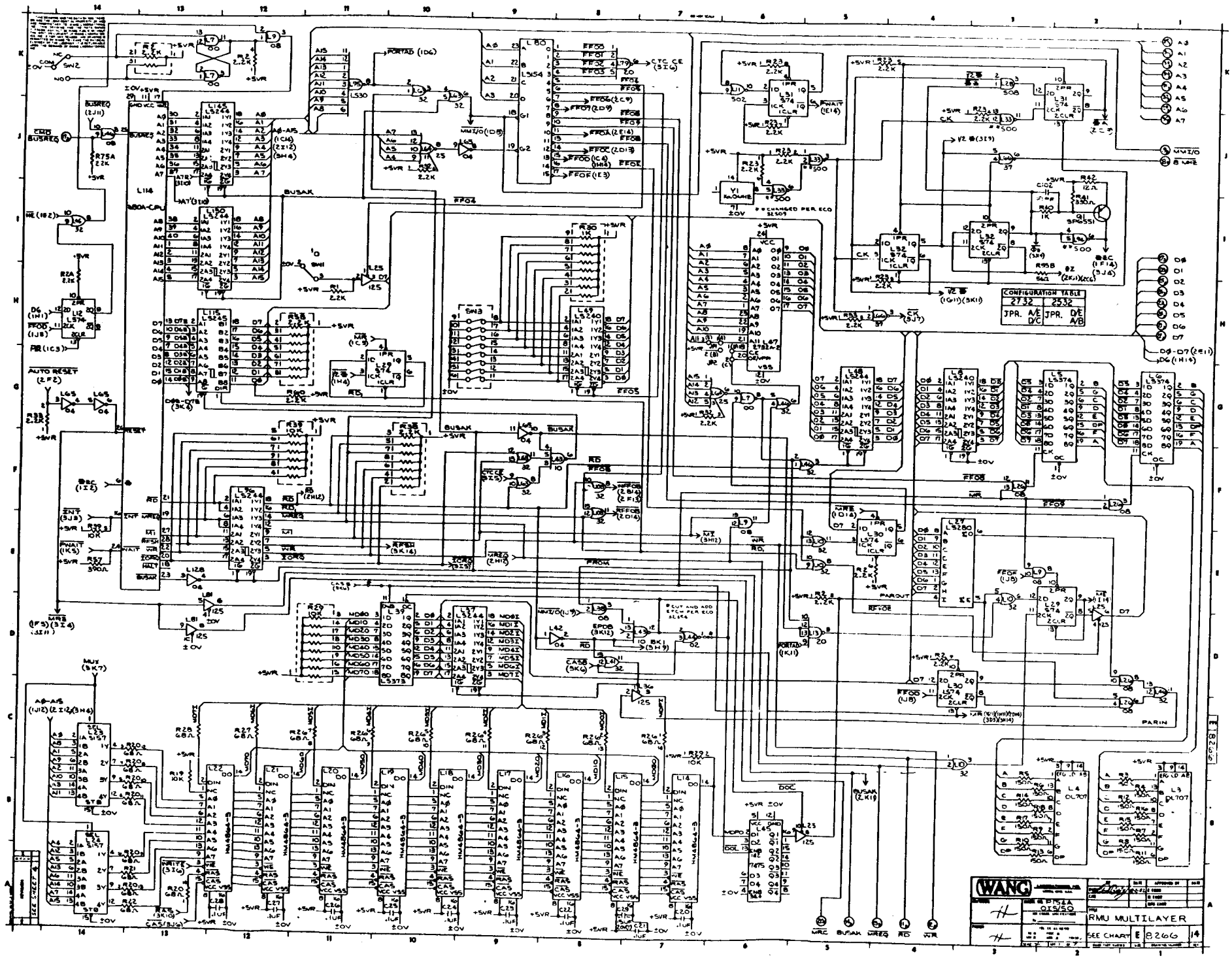
8) See page 4-18

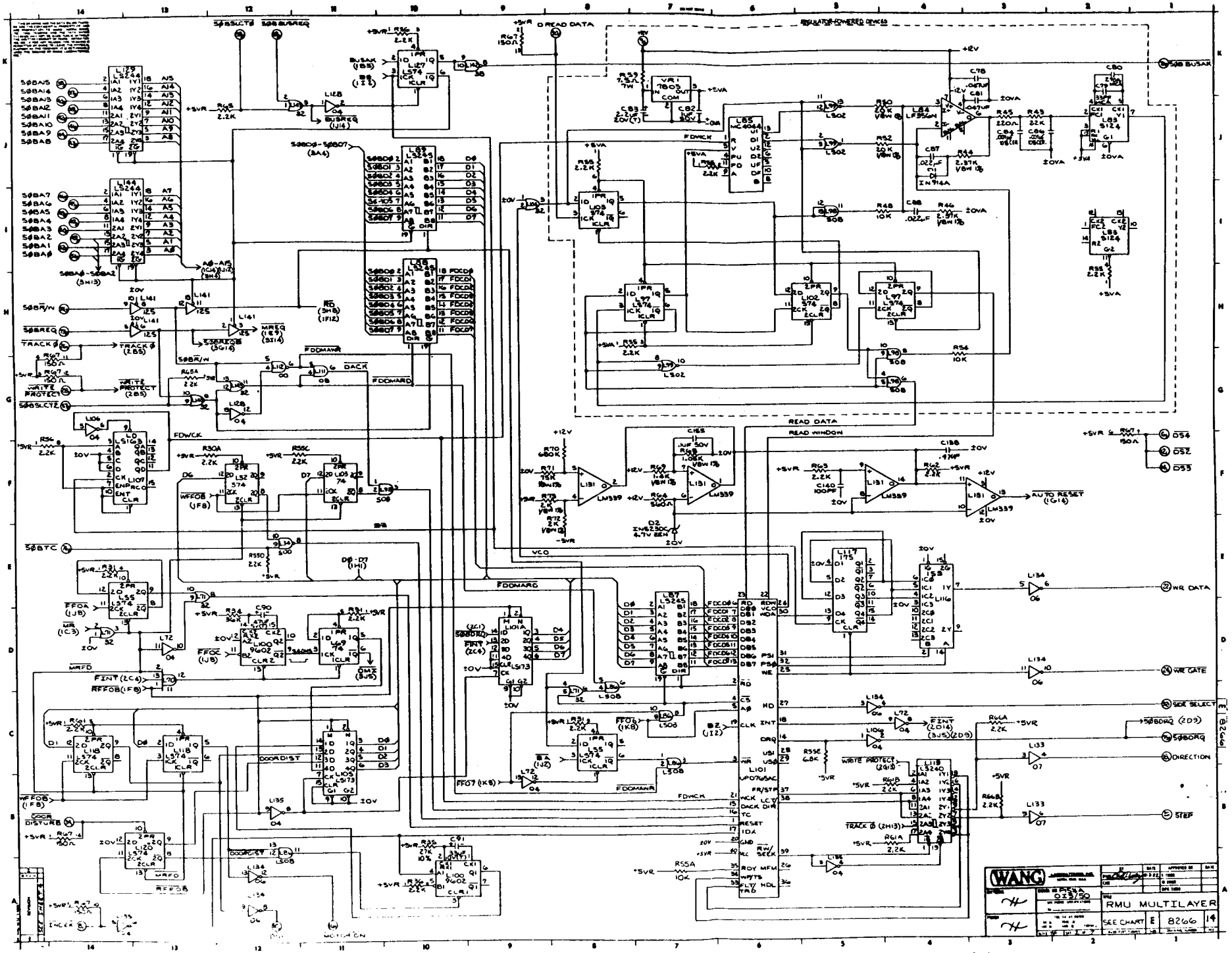
9) See page 4-22

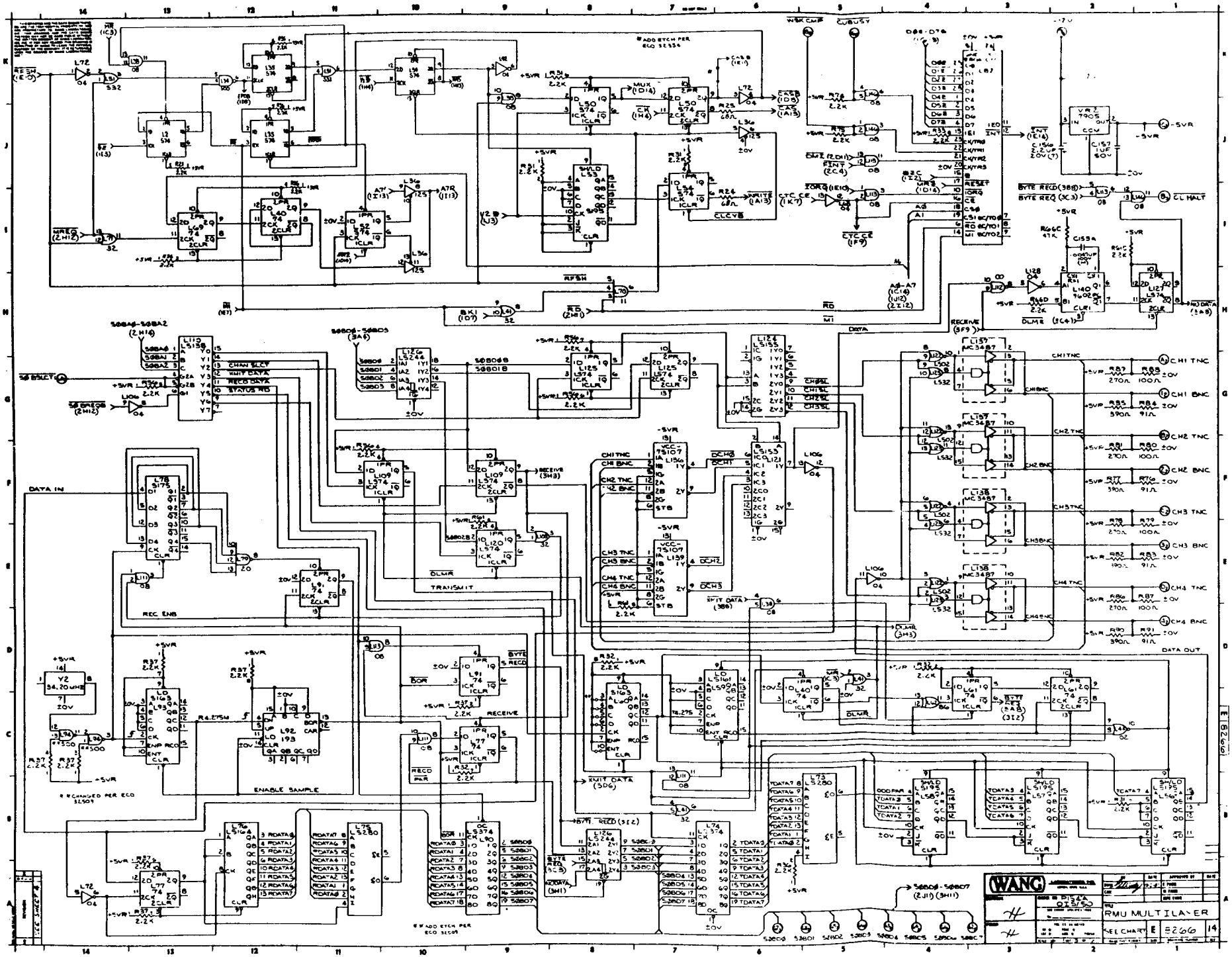
10) See page 4-37

APPENDIX

E

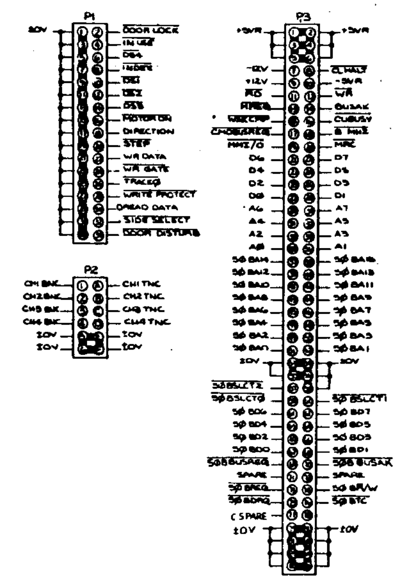

RMU MULTILAYER
WANG
SEE CHART
E 8266
14
CONFIGURATION TABLE
2732
2532
JPR. A/E D/C
JPR. D/E A/B
PARIN
PAROUT
RF-DE
MUX (5K7)
AUTO RESET (2F2)
RESET
BUSAK
BUSREQ
WR
RD
MREQ
IORQ
WAIT
DOC
PORTAB (10C)
MM1/O (10B)
CTC CE (3J6)
FF00
FF01
FF02
FF03
FF04
FF05
FF06
FF07
FF08
FF09
FF0A
FF0B
FF0C
FF0D
FF0E
FF0F
A0-A15
D0-D7
SEE SHEET 2

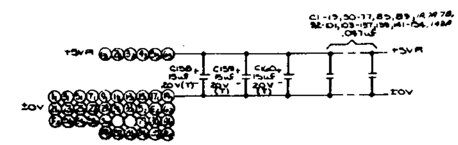

WANG
RMU MULTILAYER
SEE CHART
E 8266 14


WSK CMP
CUBUSY
D00-D07
-5VR
+5VR
+12V
BYTE REQ(38B)
BYTE REQ(3C3)
CL HALT
RESET
RFSH
RD
M1
DATA
RECEIVE (3F9)
CH1 TNC
CH1 BNC
CH2 TNC
CH2 BNC
CH3 TNC
CH3 BNC
CH4 TNC
CH4 BNC
DATA IN
DATA OUT
TRANSMIT
REC ENB
ENABLE SAMPLE
RECEIVE
XMIT DATA (3B6)
XMIT REQ (3E2)
Y2 34.20 MHz
RMU MULTILAYER
WANG
SEE CHART E 82666
14

I.C. TYPE	LOCATION	SPARE
7400	L7	1
	L112	2
74500	L34	1
	L35	1
	L94	1
7402	L44	2
74LS02	L99	1
74S02	L11	3
7404	L42	4
	L65	1
	L106	1
	L128	2
	L135	3
7406	L134	1
7407	L133	4
7408	L9	1
74S08	L28	3
7410	L43	1
7411	L70	1
7420	L13	1
7432	L143	1
	L04	3
	L108	1
74S32	L51	2
7437	L66	2
7438	L142	3
74LS74	L12	1
74S74	L2	1
7475	L46	1
7486	L62	3
74125	L25	1
	L81	2
9602PC	L140	1

MNEMONICS	COOR'D
A0-A7	1K1
BUSAK	1A5
CH1 BNC	3G1
CH2 BNC	3F1
CH3 BNC	3E1
CH4 BNC	3D1
CH1 TNC	3G1
CH2 TNC	3F1
CH3 TNC	3F1
CH4 TNC	3E1
CLHALT	3I1
CMO BUSREQ	1J14
CUBUSY	3K5
D READ DATA	2K8
D0-D7	1H1
DIRECTION	2B1
DOOR DISTURB	2B14
DOOR LOCK	2A12
DS1	2C1
DS2-DS4	2F1
INDEX	2A14
IN USE	2A11
MMI/O	1J1
MOTOR ON	2A11
MRC	1A5
MREQ	1A4
RD	1A4
SIDE SELECT	2C1
STEP	2B1
TRACK0	2H14
WR	1A4
[illegible]R DATA	2E1
WR GATE	2D1
WRITE PROTECT	2G14
WSK CMP	3K5
8MHE	1J1
S0BA0-S0BA7	2I14
S0BA8-S0BA15	2J14
S0B BUSAK	2K1
S0B BUSREQ	2K12
S0BC0-S0BC7	3A5
S0BDRQ	2C1
S0BREQ	2H14
S0BR/W	2H14
S0BSLCT0	2K12
S0BSLCT1	3G14
S0BSLCT2	2G14
S0BTC	2E14
-5VR	3J1
-12V	3K2
+12V	2K7





210 + 209 + 377 OR 378							
210	209	L3, L4		L47	L82	L101	L114
8266A	8266	340-0017		378-9039	377-0371	377-0426	377-0368
8266-B	8266	340-0017		378-9064	377-0371	377-0426	377-0368

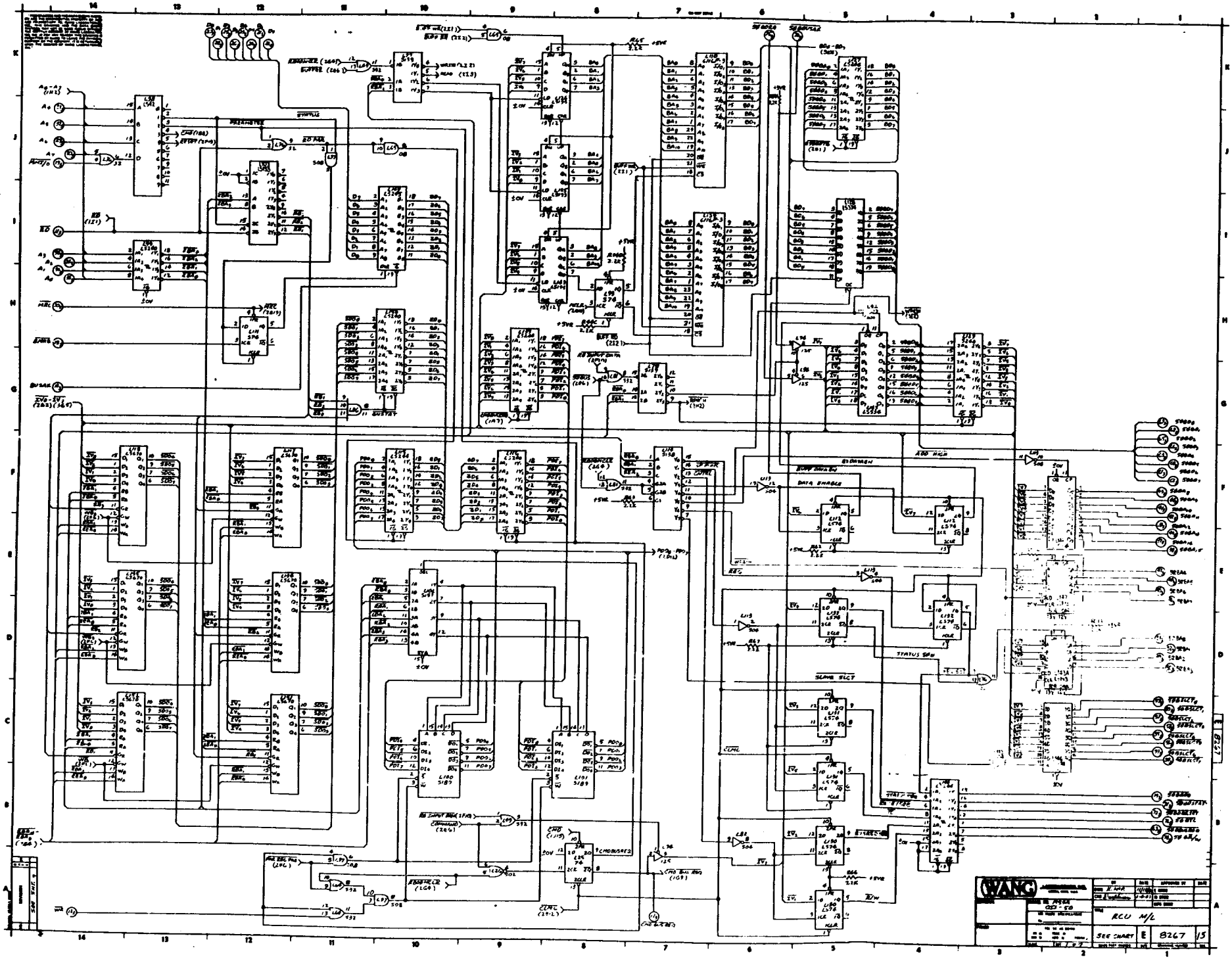
NOTES: 1) ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

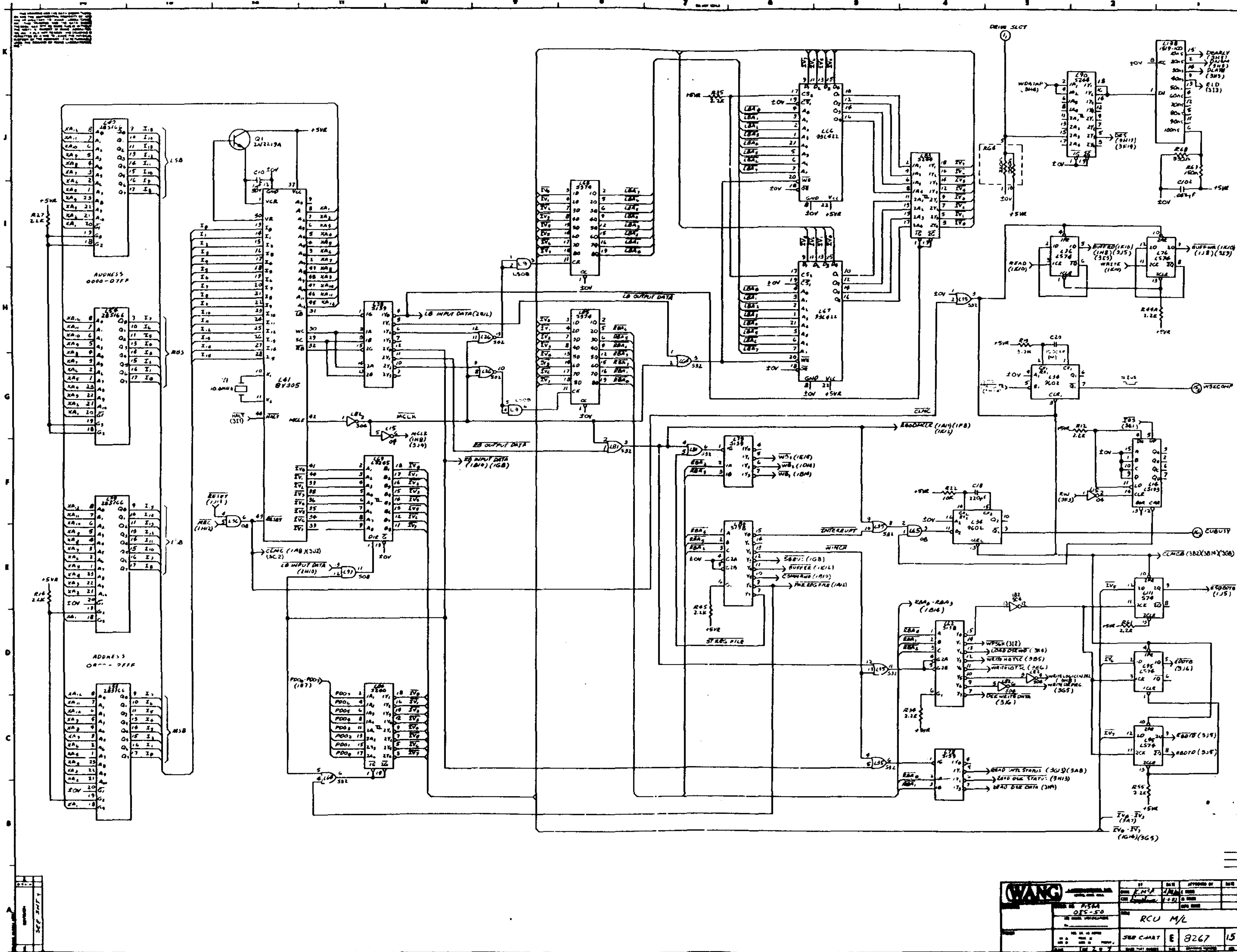
E REV 7

WANG

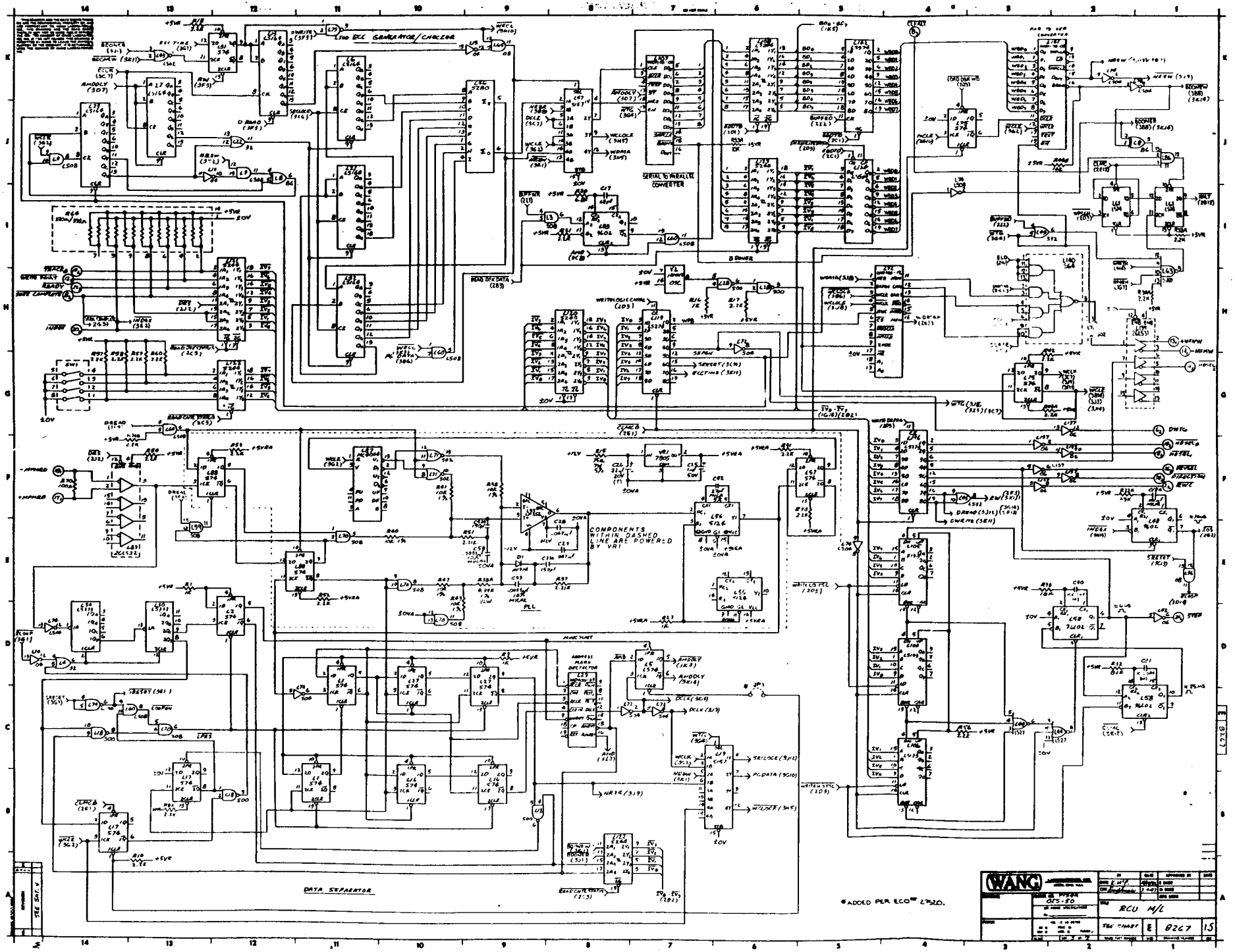
RMU MULTILAYER

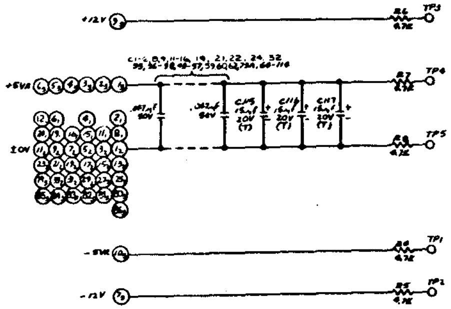
SEE CHART | E | 8266 | 14


WANG
RCU M/L
SEE CHART
E
8267
15



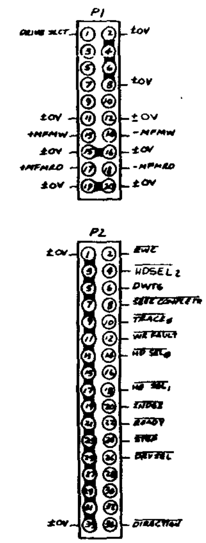
ADDRESS 0000-07FF
LSB
MSB
Q1 2N2219A
L41 8X305
10.0MHZ
HALT (3I1)
RESET
LB INPUT DATA (2H/L)
LB OUTPUT DATA
RB OUTPUT DATA
RB INPUT DATA (1B10) (1G8)
MCLK
L66 93L422
L67 93L422
L90 5244
L138
DRIVE SLCT
WDATAP (3H6)
DES (3H13) (3F19)
ELD (3I3)
BUFFRD (1K10) (1H8) (3J5) (3E5)
BUFFWR (1K10) (1J8) (3I9)
READ (1K10)
WRITE (1K11)
L34 9602
WSKCOMP
CUBUSY
CLMCB (3B2)(3B14)(3G8)
INTERRUPT
WINCH
RESDATA (1A14)(1F8) (1K12)
WB3 (1E14)
WB2 (1D14)
WB1 (1B14)
SBBUS (1G8)
BUFFER (1K12)
COMMAND (1B12)
PRE REG FILE (1A12)
ST REG FILE
RBA0-RBA3 (1B14)
WPSGH (3I2)
LOAD DSKWD (3H4)
WRITE HDTSC (3B5)
WRITELOTSC (3G6)
WRITE DSK DATA (3J6)
READ INTL STATUS (3G13)(3A8)
READ DSK STATUS (3H13)
READ DSK DATA (3H9)
ESQDOTB (1J5)
EDOTB (3J6)
EBOTB (3J9)
EBOTO (3J5)
IV0-IV3 (3A7)
IV0-IV7 (1G14)(3G5)
CLMC (1A8)(3J2) (3C2)
WANG
RCU M/L
SEE CHART
E
8267
15

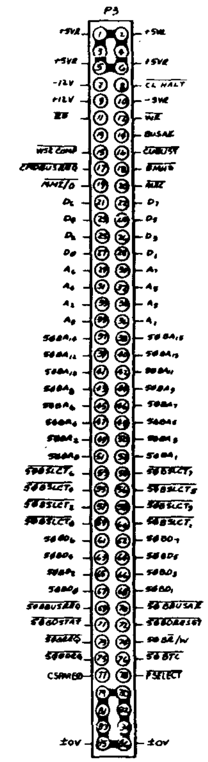

LOW ECC GENERATOR/CHECKER
SERIAL TO PARALLEL CONVERTER
B BUFFER
DATA SEPARATOR
COMPONENTS WITHIN DASHED LINE ARE POWERED BY VR1
PLL
ADDED PER ECO 27320.
WANG
RCU M/L
SHT CHART E 8267 15



TYPE	LOCATION	SPARES
74LS00	L79	2
74S00	L18	1
	L28	2
74LS02	L43	3
74S02	L71	1
7404	L10	4
	L15	5
74LS04	L74	1
74S04	L72	2
	L113	1
7406	L82	5
74S08	L9	3
	L59	2
7411	L86	1
74S10	L63	1
74LS27	L44	1
7432	L6	3
	L22	3
	L96	1
74LS32	L45	3
74S32	L49	1
74S74	L2	1
	L57	1
	L93	1
74LS74	L5	1
7486	L8	2
74125		
	L90	1
74S139	L77	1
	L79	1
74LS240	L99	1
7474	L25	1
7408	L36	2
74S02	L26	1
9602	L33	1
	L48	1

MNEMONICS	COORD
A_8 - A_{15}	1H14
A_0 - A_7	1J14
BUSAK	1G14
CL HALT	3H4
CHKBUSERR	1A7
CLRBUSY	2E1
D_0 - D_7	1K12
DIRECTION	3F1
DRIVE SLCT	2K3
DRVSEL	3F1
DWT6	3F1
HD SEL$_0$	3F1
HD SEL$_1$	3F1
HD SEL$_2$	3G1
INDEX	3H14
+MFMRD	3F14
-MFMRD	3F14
+MFMW	3H1
-MFMW	3H1
MML/O	1J14
MRQ	1H14
RD	1I14
READY	3H14
RWC	3F1
SEEK COMPLETE	3H14
STEP	3D1
TRACK$_0$	3H16
WE	1A16
WR FAULT	3H16
WSR COMP	2G1
BMHB	1H14
560A$_0$ - 560A$_{15}$	1G1
560BUSAK	1K6
560BUSREQ	1B1
560D$_0$ - 560D$_7$	1G1
560RESET	1B1
560CRQ	1K6
5IOSTAT	1B1
560RED	1B1
560R/W	1B1
560SLCT$_0$ - 560SLCT$_3$	1C1
560TC	1B1





	210 = 209 + 377 OR 378							
MODEL	210	209	L39	L40	L53	L54	L41	L66 L67	L109,L110
013-50	8267-A	8267	377-3039	377-3040	377-3058	377-3041	377-0472	377-0384	377-0403
013-60	8267-B	8267	377-3068	377-3069	377-3070	377-3071	377-0472	377-0384	377-0403

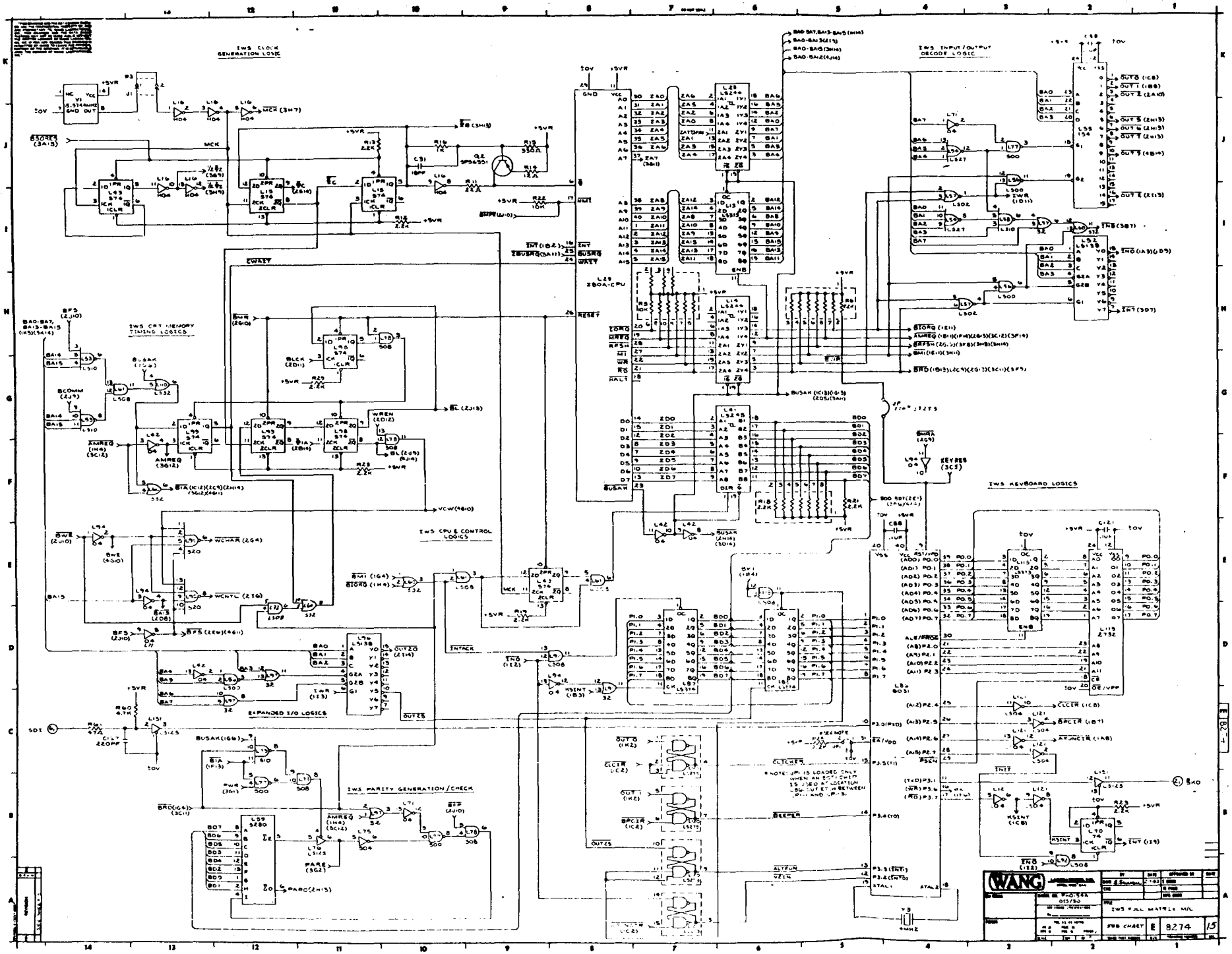
NOTE:
1. ALL RESISTORS UNLESS OTHERWISE SPECIFIED ARE 1/4W 5%.

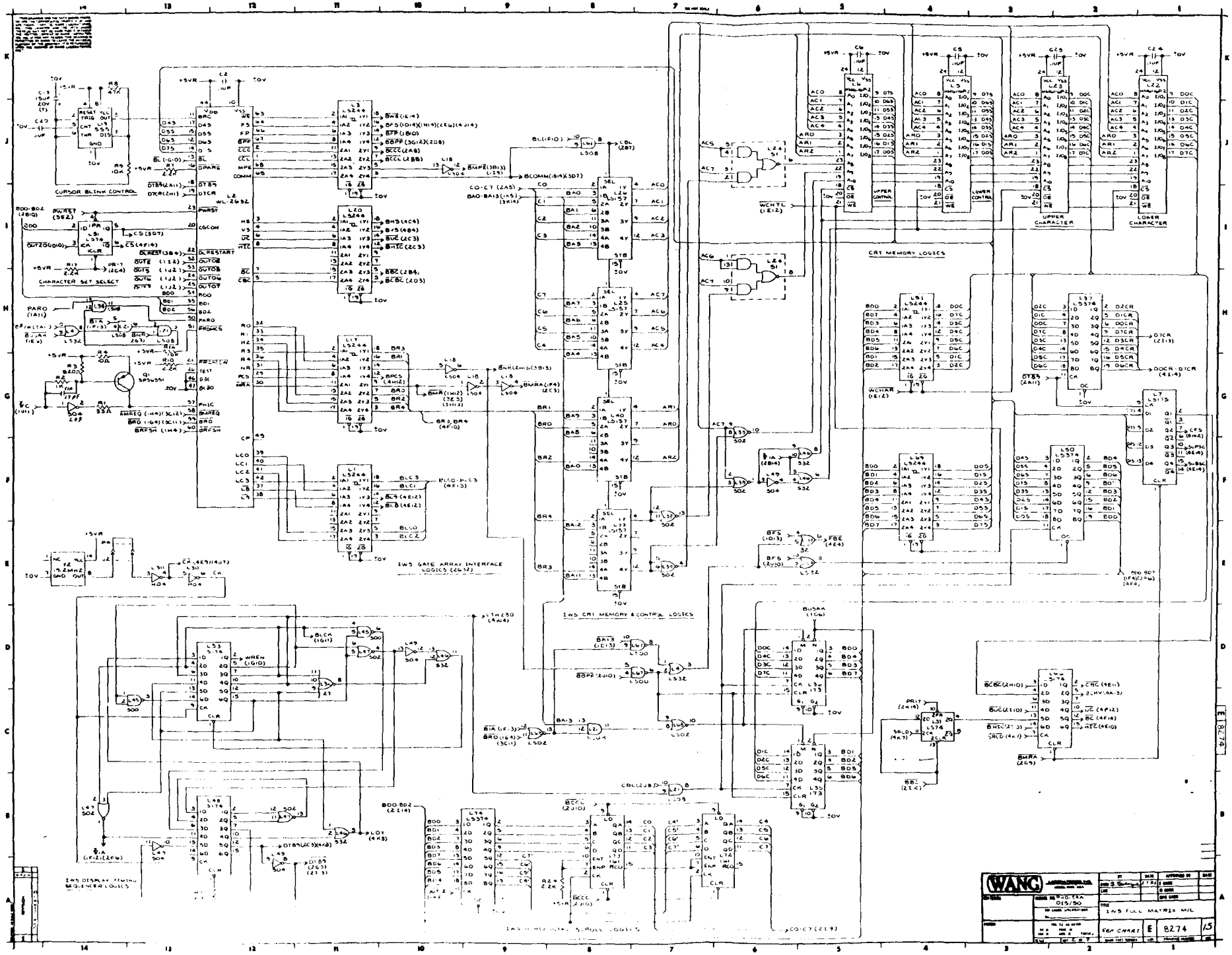
E-REV 5

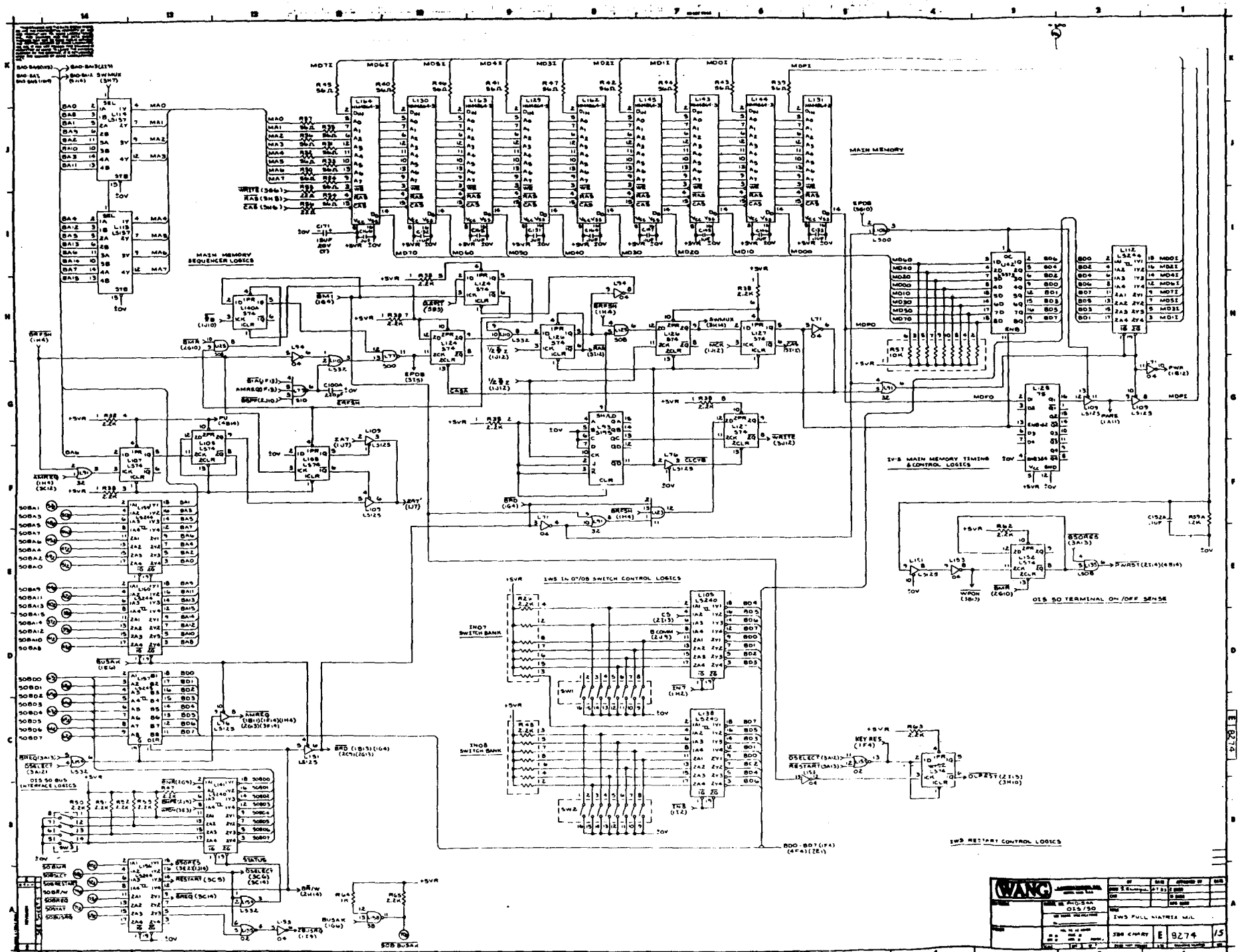
WANG LABORATORIES, INC.

RCU M/L

210-8267 E 8267 15


IWS CLOCK GENERATION LOGIC
IWS CRT MEMORY TIMING LOGICS
IWS CPU & CONTROL LOGICS
EXPANDED I/O LOGICS
IWS PARITY GENERATION/CHECK
IWS INPUT/OUTPUT DECODE LOGIC
IWS KEYBOARD LOGICS
Z80A-CPU
IWS FULL MATRIX M/L
WANG
DWG CHART E 8274 15


CURSOR BLINK CONTROL
CHARACTER SET SELECT
IWS GATE ARRAY INTERFACE LOGICS (2G32)
IWS CRT MEMORY & CONTROL LOGICS
CRT MEMORY LOGICS
UPPER CHARACTER
LOWER CHARACTER
IWS DISPLAY TIMING SEQUENCER LOGICS
IWS HARDWARE SCROLL LOGICS
WANG
IWS FULL MATRIX M/L
FSR CHART E 8274 15


MAIN MEMORY
MAIN MEMORY SEQUENCER LOGICS
IVS MAIN MEMORY TIMING & CONTROL LOGICS
IVS IN 07/08 SWITCH CONTROL LOGICS
IVS RESTART CONTROL LOGICS
015 50 TERMINAL ON/OFF SENSE
015 50 BUS INTERFACE LOGICS
IN07 SWITCH BANK
IN08 SWITCH BANK
WANG
IVS FULL MATRIX M/L
SDB CHART E 9274 15