This Library Memo announces the release and availability of *System 80 Models 8/10/15/20 Processor Programming Reference Manual,* UP-9692 Rev. 2. This manual is a standard library item (SLI). It is part of the standard library provided automatically with the purchase of the product.

The System 80 models 8/10/15/20 are each powerful, flexible data processing systems. These systems feature integrated hardware and the advanced Unisys Operating System/3 (OS/3).

This manual provides detailed programming reference material on the processor complex of the models 8/10/15/20. This includes basic descriptions of the processor components and specific information on operations control, machine check control, and the input/output status tabler.

This revision documents the model 15 processor and these new peripherals: DCP/15, DCP/40, 3200 series magnetic tapes, and the 9246-14B and 9246-25B line printers.

Additional copies may be ordered through your local Unisys representative.

**Destruction Notice:** This revision supersedes and replaces *System 80 Models 8/10/20 Processor Programming Reference Manual,* UP-9692 Rev. 1, released on Library Memo dated September 1987. Please destroy all copies of UP-9692 Rev. 1, all its updates, and all its Library Memos.

# UNISYS

# System 80
# Models 8/10/15/20

# Processor

**Programming
Reference Manual**

# UNISYS

# System 80
# Models 8/10/15/20

# Processor

# Programming
# Reference Manual

# PAGE STATUS SUMMARY
## ISSUE: UP-9692 Rev. 2

| Part/Section | Page Number | Update Level |
|---|---|---|
| Cover | | |
| Title Page/Disclaimer | | |
| PSS | iii | |
| Using This Manual | v, vi | |
| Contents | vii thru xv | |
| 1 | 1 thru 6<br>7/8*<br>9 thru 12<br>13/14*<br>15 thru 86 | |
| 2 | 1 thru 24 | |
| 3 | 1 thru 80 | |
| 4 | 1 thru 33 | |
| 5 | 1 thru 3 | |
| 6 | 1 thru 14 | |
| Appendix A | 1 thru 5 | |
| Index | 1 thru 9 | |
| User Comment Form | | |
| Back Cover | | |

| Part/Section | Page Number | Update Level |
|---|---|---|
| | | |

| Part/Section | Page Number | Update Level |
|---|---|---|
| | | |

* 11 x 17 foldout

# Using This Manual

This manual provides detailed programming information about the processor complex of the System 80 models 8, 10, 15, and 20. This manual is intended for the experienced programmer.

Some sections of this manual contain information that applies only to specific models. These sections include the model designation in their titles. All other information in this manual, unless otherwise indicated, applies to all four System 80 models: 8, 10, 15, and 20.

**Organization of This Manual**

This manual has six sections:

- Section 1. Introduction

    Explains the basic organization and configurations of the processor complex for the models 8/10/15/20.

- Section 2. Processor Components

    Describes the basic functional components that comprise the processor complex of the model 8 and models 10/15/20.

- Section 3. Operations Control

    Describes the basic operations of the processor complex, including data and instruction formats, program status words, and interrupts.

■   Section 4. Machine Check Control

    Describes machine check detection, types, and operations.

■   Section 5. Operations Systems Control

    Briefly describes the system console and the function of the console display.

■   Section 6. Input/Output Status Tabler

    Describes IOST processing, operation, and status handling.

## Related Manuals

The processor complex of the System 80 models 8/10/15/20 is also described in the following manuals:

■   *System 80 Models 8/10/15/20 Processor Complex Controllers Programming Reference Manual, Volume 1: Controllers of Selector Channel and Byte Multiplexer,* UP-9607

■   *System 80 Models 8/10/15/20 Processor Complex Controllers Programming Reference Manual, Volume 2: Controllers and Communications Channels of the I/O Processor,* UP-9732

■   *System 80 Models 8/10/15/20 Processor and Central Peripherals Operating Guide,* UP-9608

# Contents

# 3. OPERATIONS CONTROL

**5. OPERATIONS SYSTEMS CONTROL**

**6. INPUT/OUTPUT STATUS TABLER**

**APPENDIX**

**A.  ABBREVIATIONS AND ACRONYMS**

**INDEX**

**USER COMMENT FORM**

**FIGURES**

## TABLES

# 1. Introduction

## 1.1. PROCESSING SYSTEM

The basic System 80 models 8/10/15/20 processor complex consists of the following equipment:

- System console

- Console display

- Processor cabinet

- I/O cabinet

In addition, the basic system can be expanded by adding an:

- I/O expansion cabinet

Figure 1-1 (model 8) and Figure 1-2 (models 10/15/20) show the basic system with an I/O expansion cabinet.
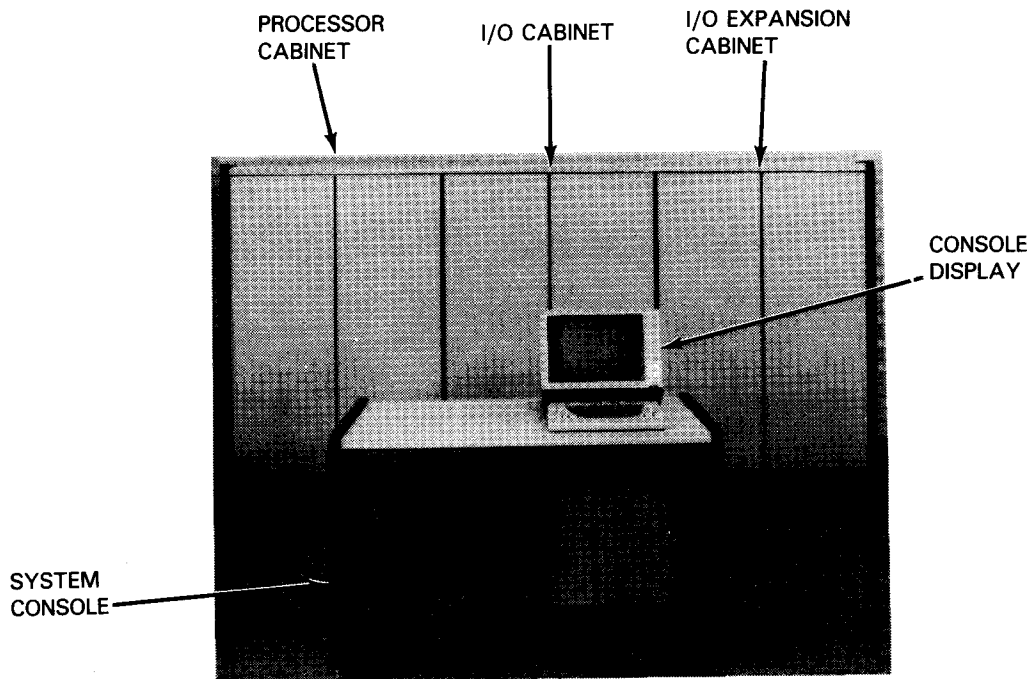
**Figure 1-1. System 80 Model 8 Processor Complex**
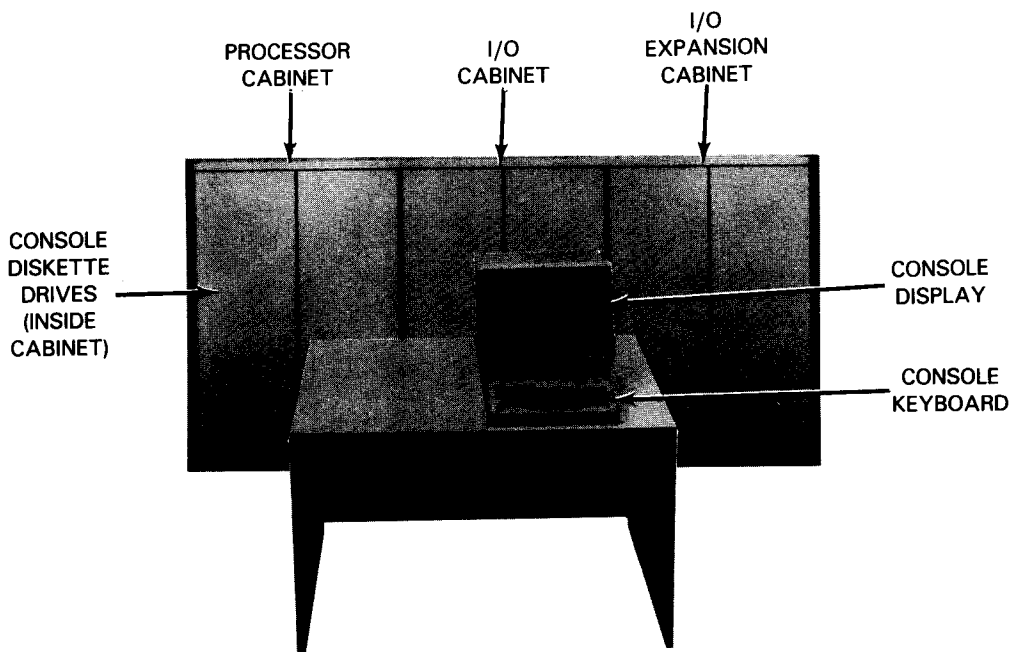


**Figure 1-2. System 80 Models 10/15/20 Processor Complex**

### 1.1.1. Basic Model 8 Processor Complex Structure

Within the basic cabinetry, the model 8 processor complex consists of the following modular components:

■   Central processing unit (CPU)

■   Main storage unit (MSU)

■   I/O channels

■   I/O devices attached to integrated controllers

Figure 1-3 shows the basic organization of these components for the model 8 system.

```
                              ┌──────────────┐
                              │    MAIN      │
                              │   STORAGE    │
                              └──────┬───────┘
        ┌────────────────┬──────────┼──────────┬────────────────┐
  ┌─────────────┐ ┌─────────────┐ ┌─────────────┐ ┌─────────────┐
  │  CENTRAL    │ │   SYSTEM    │ │   CHANNEL   │ │   M-BUS     │
  │ PROCESSING  │ │   CONTROL   │ │ CONTROLLER  │ │  ADAPTER    │
  │    UNIT     │ │  PROCESSOR  │ │             │ │             │
  ├─────────────┤ └─────────────┘ └─────────────┘ └─────────────┘
  │   CONTROL   │
  │   STORAGE   │
  └─────────────┘
  ┌─────────────┐ ┌─────────────┐ ┌─────────────┐
  │    BYTE     │ │ INTEGRATED  │ │    I/O      │
  │ MULTIPLEXER │ │  SELECTOR   │ │MICROPROCESSOR│
  │             │ │  CHANNEL    │ │             │
  └──────┬──────┘ └──────┬──────┘ └──────┬──────┘
```

PRINTERS AND            MAGNETIC TAPE
CARD READERS       AND DISK SUBSYSTEMS
CONSOLE DISPLAY           AND DCPS

```
                    ┌─────────────┐ ┌─────────────┐
                    │ MULTIPLE LINE│ │SHARED DIRECT│
                    │COMMUNICATIONS│ │   MEMORY    │
                    │ MULTIPLEXER  │ │   ACCESS    │
                    │   (MLCM)     │ │   (SDMA)    │
                    └──────┬───────┘ └──────┬──────┘
                                    ┌─────────────┐
                                    │ INTEGRATED  │
   COMMUNICATIONS                   │ PERIPHERAL  │
   LINES AND DEVICES                │ CONTROLLERS │
                                    └──────┬──────┘
```

WORKSTATIONS,
DISKETTE DRIVES,
PRINTERS,
CARD PUNCH AND
READER, AND
MAGNETIC TAPE
DRIVES

**Figure 1-3.  Model 8 System Logical Structure**

## 1.1.2. Basic Models 10/15/20 Processor Complex Structure

Within the basic cabinetry, the models 10/15/20 processor complex consists of the following modular components:

- Basic processing unit (BPU)

- Main storage unit (MSU)

- I/O channels

- I/O devices attached to integrated controllers

Figure 1-4 shows the basic organization of these components for the models 10/15/20 system.
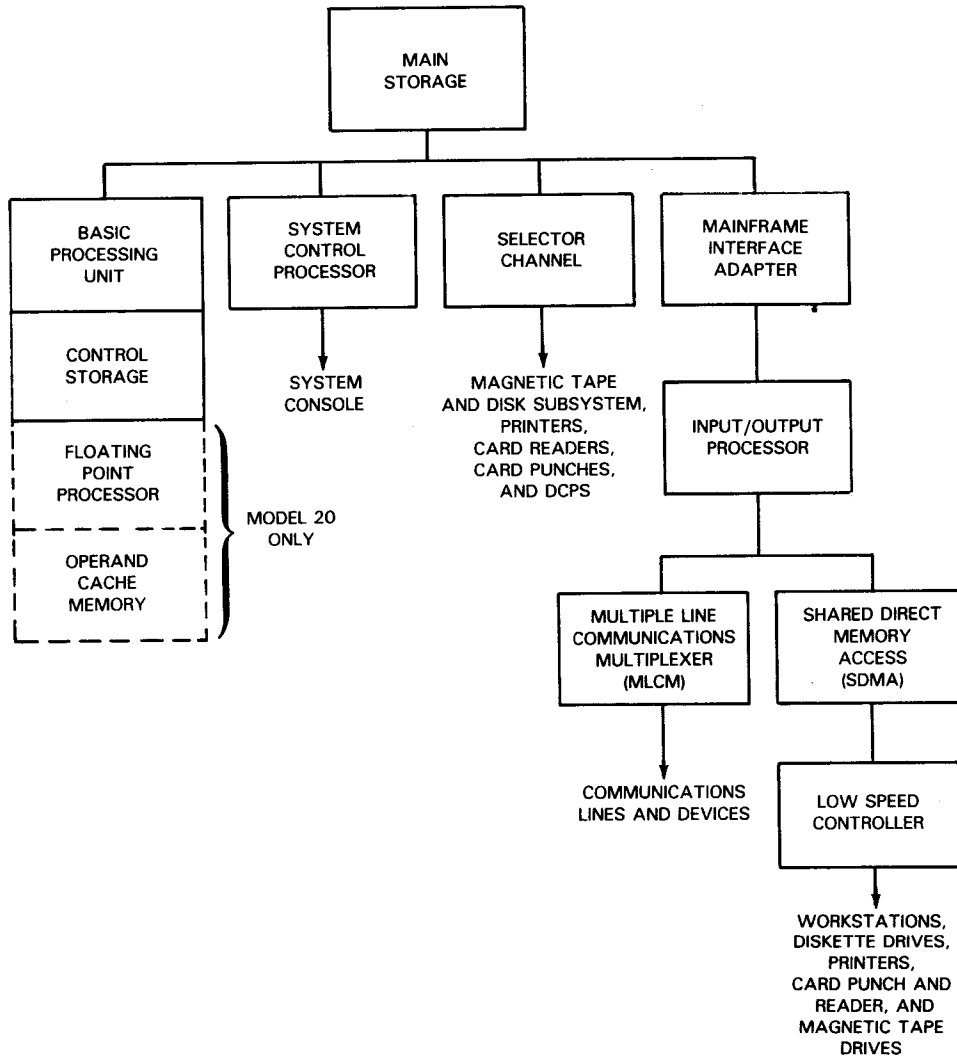
Figure 1-4. Models 10/15/20 System Logical Structure

## 1.2. CONFIGURATIONS

The System 80 models 8/10/15/20 can be configured in a variety of ways to best suit user requirements. Each operating area can be configured separately.

Some configurations are specific to the model 8 or to the models 10/15/20. These configurations are described in separate paragraphs (1.2.1 and 1.2.2 respectively). The configurations of peripheral subsystems common to all models are described in a single paragraph (1.2.3).

### 1.2.1. Model 8 Configurations

Figures 1-5 to 1-9 show configurations specific to the model 8.
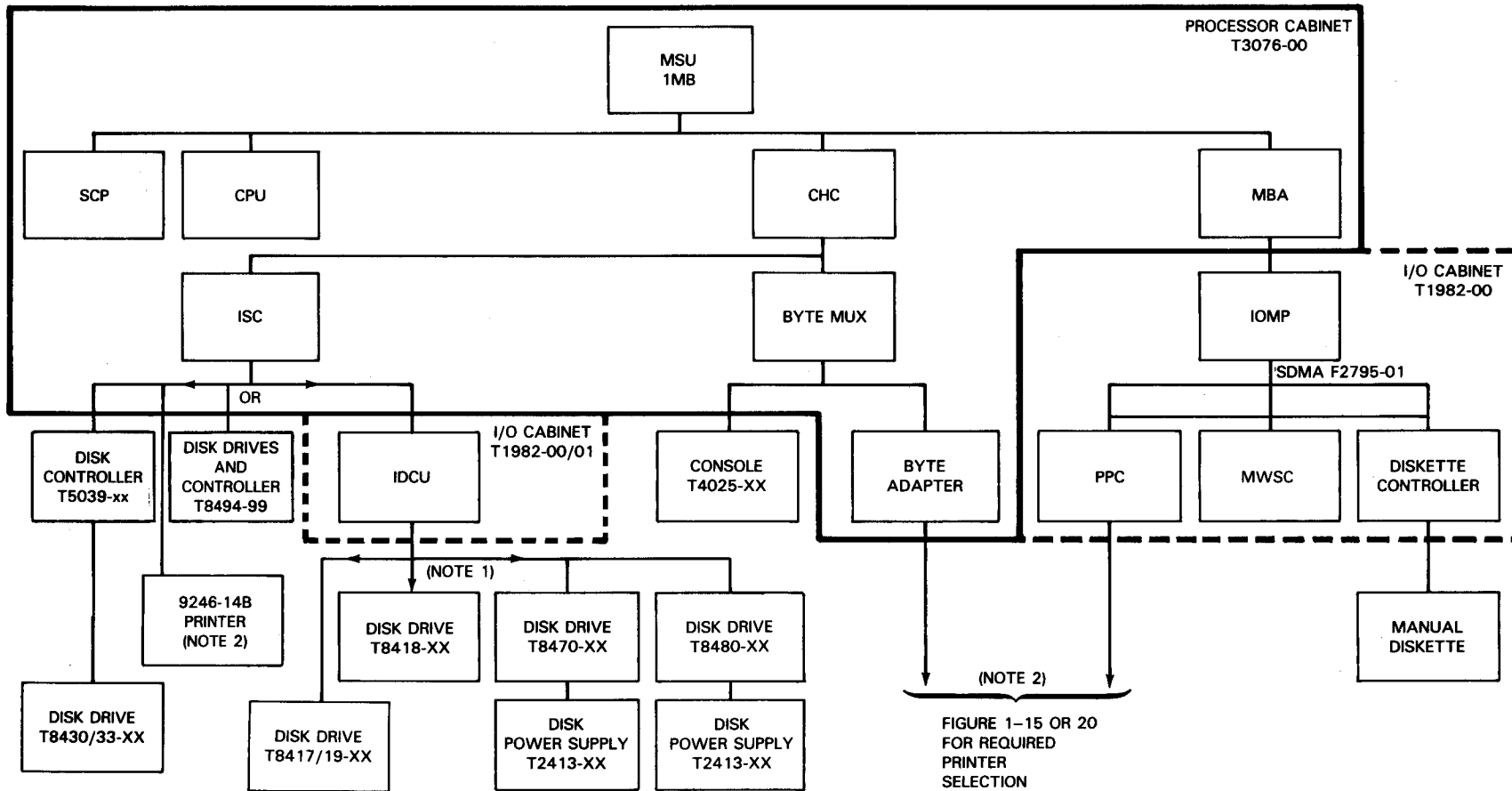
NOTES:

1. Minimum disk configuration 50MB on one drive unless 8418 (high density), 8419, 8430, 8433, 8494 are used. Then a minimum of 2 drives required.

2. Either PPC or byte adapter required if required line printer is not configured on ISC.

**Figure 1-5. Model 8 Minimum Configuration**

PROCESSOR CABINET

| MAIN STORAGE UNIT-1 (MSU) |
| 1 MB |

| CENTRAL PROCESSING UNIT (CPU) |
| CONTROL STORAGE (CS) |

| SYSTEM CONTROL PROCESSOR (SCP) |

| CHANNEL CONTROLLER* (CHC) |

*A MAXIMUM OF 2 CHCs CAN BE CONFIGURED

| BYTE MULTIPLEXER |
| BYTE ADAPTER |

*A MAXIMUM OF 5 ISCs CAN BE CONFIGURED

| INTEGRATED SELECTOR CHANNEL* (ISC) |

| INTEGRATED SELECTOR CHANNEL (ISC) |

| INTEGRATED SELECTOR CHANNEL (ISC) |

| MI |
| MULTIPLE COMMUNICA MULTIPLE. (MLCM |

| SINGLE LIN COMMUNICAT ADAPTEF (SLCA) |

| 0776 PRINTER AND CONTROLLER |

| 0770 ① PRINTER AND CONTROLLER |

| 0716 CARD READER AND CONTROLLER |

| 9246-25B PRINTER AND CONTROLLER |

| SYSTEM CONSOLE |

| 8494 DISK DRIVES AND CONTROLLER |

| 5058 TAPE CONTROLLER |

| UNISERVO 22/24 TAPE DRIVES |

| 5045 TAPE CONTROLLER |

| UNISERVO 10/14 TAPE DRIVES |

| 5017 TAPE CONTROLLER |

| UNISERVO 12/16 TAPE DRIVES (16 MAXIMUM) |

| 0770 PRINTER AND CONTROLLER |

| 5039 DISK CONTROLLER |

| 8430/8433 DISK DRIVES (16 MAXIMUM) |

| 9246-14B PRINTER AND CONTROLLER |

| 5034 TAPE CONTROLLER |

| UNISERVO 12/16/20 TAPE DRIVES (16 MAXIMUM) |

| 5055 TAPE CONTROLLER |

| UNISERVO 22/24/26/28 TAPE DRIVES |

| 9246-25B PRINTER AND CONTROLLER |

| 5039 DISK CONTROLLER |

| 8430 DISK DRIVE |

| 3200 ② SERIES TAPE CONTROLLER |

| 3200 ③ SERIES TAPE DRIVES |

| DCP 15 |

| DCP 40 |

| 8494 DISK DRIVES AND CONTROLLER |

| 8418 DISK DRIVE |

| 8417/8419 DISK DRIVES |

| 8470/8480 DISK DRIVES |

| 8470/8480 DISK DRIVES |

| 8470/8480 DISK DRIVES |

| 8416/8418 DISK DRIVES |

| UNISERVO 10 (TYPE 0871) TAPE DRIVE |

| INTEGRATED DISK CONTROL UNIT (IDCU) |

| INTEGRATED DISK CONTROL UNIT (IDCU) |

| INTEGRATED DISK CONTROL UNIT (IDCU) |

| INTEGRATED DISK CONTROL UNIT (IDCU) |

| DUAL ACCESS |

| INTEGRATED DISK CONTROL UNIT (IDCU) |

| I/O SUBSYSTEM EXPANDER |

| PAPER PERIPHERAL CONTROLLER |

| A [ |

1

LOW TO MED SPEED COMMUNICA LINES

| 0608 CARD PUNCH |

| 0719 CARD READER |

| PRINTER SELECTION |

| UNISERV 22 TAF DRIVE |

LEGEND:

▭ Required for minimum configuration

▭ Optional maximum configuration supported

NOTES:

① T0770-06/07 printer connects only to an integrated selector channel (ISC)

② Where 00 can be 41, 61, or 81

③ Where 00 can be 44, 65, 66, or 88

Figure 1-6.  Model 8 Max

Figure 1-6.  Model 8 Maximum Configuration

(FIGURE 1–9)

MEMORY CONFIGURATION

```
                              ┌─────────────┐
  ┌──────┐  ┌──────┐  ┌──────┐ │             │  ┌──────┐
  │ SCP  │  │ CPU  │  │ CHC* │ │ CHC         │  │ MBA  │
  │      │  │      │  │      │ │ K3960-00    │  │      │
  └──────┘  └──────┘  └──────┘ └─────────────┘  └──────┘
```

BYTE MUX   ISC*   ISC K3962-00   ISC K3962-00   ISC K3962-00   ISC K3962-00

BYTE ADAPTER F3961-00

(FIGURE 1– 8)

*Part of processor cabinet, T3076-00

**Figure 1-7.  Model 8 Maximum Processor Cabinet Configuration**

```
                    ┌─────────────────┐
                    │      BYTE       │
                    │    ADAPTER      │
                    │   F3961-00*     │
                    └─────────────────┘
           ┌───────────────┼───────────────┐
┌───────────────┐ ┌───────────────┐ ┌─────────────────┐
│  PRINTER AND  │ │  PRINTER AND  │ │  CARD READER    │
│  CONTROLLER   │ │  CONTROLLER   │ │ AND CONTROLLER  │
│   T0776-00    │ │   T0770-00    │ │   T0716-00      │
│   THRU -05    │ │   THRU -07    │ │   THRU -07      │
└───────────────┘ └───────────────┘ └─────────────────┘
                      800 LPM
                     1400 LPM
                     2000 LPM
```

*Any combination of 4 peripherals may be connected.

Figure 1-8.  Byte Adapter Configuration

```
                              ┌──────────┐  ┌──────────┐
                              │   MS     │  │   MS     │
                              │  2MB     │  │  1MB     │
                              │ K3959-01 │  │ K3959-00 │
                              └──────────┘  └──────────┘

    ┌──────────┐
    │  MSU     │
    │  1MB     │
    │ (NOTE 2) │
    └──────────┘
                  (NOTE 3)    ┌──────────┐  ┌──────────┐
                              │   MS     │  │   MS     │
                              │  1MB     │  │  1MB     │
                              │ K3959-00 │  │ K3959-00 │
                              └──────────┘  └──────────┘

                              ┌──────────┐  ┌──────────┐
                              │   MS     │  │   MS     │
                              │  2MB     │  │  1MB     │
                              │ K3959-01 │  │ K3959-00 │
                              └──────────┘  └──────────┘

    ┌──────────┐
    │  MSU     │
    │  1MB     │
    │ K3958-00 │
    └──────────┘
    (NOTE 4)
                  (NOTE 3)    ┌──────────┐  ┌──────────┐
                              │   MS     │  │   MS     │
                              │  1MB     │  │  1MB     │
                              │ K3959-00 │  │ K3959-00 │
                              └──────────┘  └──────────┘
```

NOTES:

1.  Memory expansion for each MSU must occur in identical MB increments.

2.  Part of processor cabinet, T3076-00.

3.  Following this path of configuration requires swap-out of one K3959-00 which is replaced with K3959-01 for configuration of 4MB.

4.  When two MSUs are configured, each must contain an equal amount of main storage, that is, configurations of 5MB + 7MB are disallowed.

**Figure 1-9. Model 8 Storage Configuration**

## 1.2.2. Models 10/15/20 Configurations

Figures 1-10 to 1-13 show configurations specific to the models 10/15/20.

**PROCESSOR CABINET T3135-00**

MCU

(NOTE 1)

SCP  BPU  SEL  MIA

**I/O CABINET T1982-04**

IOP

SDMA F2795-01

OR

CONSOLE T4028-XX

DISK CONTROLLER T5039-xx

DISK DRIVES AND CONTROLLER T8494-99

IDCU

**I/O CABINET T1982-04**

9246-14B PRINTER (NOTE 3)

PPC

DISKETTE CONTROLLER

(NOTE 2)

DISK DRIVE T8470-XX

DISK DRIVE T8480-XX

MANUAL DISKETTE

DISK DRIVE T8430/33-XX

DISK DRIVE T8417/19-XX

DISK POWER SUPPLY T2413-XX

DISK POWER SUPPLY T2413-XX

(NOTE 3)

FIGURE 1-15 FOR REQUIRED PRINTER SELECTION

NOTES:

1.  2MB minimum memory for model 10. 4MB minimum memory for models 15 or 20.

2.  Minimum disk configuration 50MB on one drive or at least two drives of the following types: 8419, 8430, 8433, 8494.

3.  PPC required if required line printer is not configured on SEL.

**Figure 1-10. Models 10/15/20 Minumum Configuration**

Figure 1-11. Models 1

**S-BUS**

**L-BUS**

**D MUX**

MAINFRAME INTERFACE
ADAPTER (MIA)

**AS-BUS**

**AL-BUS**

I/O CABINET

INPUT/OUTPUT
PROCESSOR-1
(IOP)

INPUT/OUTPUT
MICROPROCESSOR-2
(IOP)

MULTIPLE LINE
COMMUNICATIONS
MULTIPLEXER
(MLCM)

SHARED DIRECT
MEMORY ACCESS
(SDMA)

MULTIPLE LINE
COMMUNICATIONS
MULTIPLEXER
(MLCM)

SHARED DIRECT
MEMORY ACCESS
(SDMA)

INTEGRATED
DISK CONTROL
UNIT
(IDCU)

SINGLE LINE
COMMUNICATIONS
ADAPTER
(SLCA)

DISKETTE
CONTROLLER

DISKETTE
SELECTION

SINGLE LINE
COMMUNICATIONS
ADAPTER
(SLCA)

DISKETTE
CONTROLLER

DISKETTE
SELECTION

8406
DISKETTE

INTEGRATED
DISK CONTROL
UNIT
(IDCU)

AUTO
DIAL

WORKSTATION
CONTROLLER

SCREEN DEVICE
20D - MODEL 1 OR
40D - MODEL 2
WORKSTATION
OR
SVT 1122
TERMINAL

AUTO
DIAL

WORKSTATION
CONTROLLER

SCREEN
DEVICE

3386
MAGNETIC
STRIPE READER

INTEGRATED
DISK CONTROL
UNIT
(IDCU)

1          14

LOW TO MEDIUM
SPEED
COMMUNICATION
LINES

1          14

LOW TO MEDIUM
SPEED
COMMUNICATION
LINES

I/O
SUBSYSTEM
EXPANDER

UNISERVO 10
(TYPE 0871)
TAPE DRIVE

CHARACTER
PRINTER

CHARACTER
PRINTER

INTEGRATED
DISK CONTROL
UNIT
(IDCU)

3389
MAGNETIC
STRIPE READER

INTEGRATED
TAPE
CONTROLLER

3782
STREAMING
TAPE DRIVE

UNISERVO
22 TAPE
DRIVE

DUAL
ACCESS

8406
DISKETTE

I/O SUBSYSTEM
EXPANDER

REMOTE
PRINTER
INTERFACE

REMOTE
PRINTER
ATTACHMENT

PAPER
PERIPHERAL
CONTROLLER

PRINTER
SELECTION

0608
CARD
PUNCH

PAPER
PERIPHERAL
CONTROLLER

INTEGRATED
TAPE
CONTROLLER

0789
PRINTER

OR

0719 CARD
READER

0608 CARD
PUNCH

0719
CARD
READER

PRINTER
SELECTION

UNISERVO
22 TAPE
DRIVE

3782
STREAMING
TAPE DRIVE

0798
PRINTER

REMOTE
PRINTER
INTERFACE

REMOTE
PRINTER
ATTACHMENT

0789
PRINTER

I/O EXPANSION CABINET

0798
PRINTER

**10/15/20 Maximum Configuration**

1-13/14

MEMORY CONFIGURATION

```
                              ┌──────────────────┐
                              │                  │
              ┌────────┐   ┌────────┐                          ┌────────┐
              │  SCP   │   │  BPU   │                          │  MIA   │
              └────────┘   └────────┘                          └────────┘
                               │
                       ┌───────┴───────┐
                  ┌──────────┐    ┌──────────┐
                  │ FLOATING │    │ OPERAND  │
                  │  POINT   │    │  CACHE   │
                  │PROCESSOR │    │ MEMORY   │
                  │ F8466-00 │    │ F8467-00 │
                  └──────────┘    └──────────┘
                   (NOTE 1)        (NOTE 1)
```

```
  ┌────┬────────┬────────┬────────┬────────┬────────┐
┌──────┐ ┌──────┐ ┌──────┐ ┌──────┐ ┌──────┐ ┌──────┐
│ SEL  │ │ SEL  │ │ SEL  │ │ SEL  │ │ SEL  │ │ SEL  │
│      │ │F4868-│ │F4868-│ │F4868-│ │F4868-│ │F4868-│
│      │ │ 00   │ │ 00   │ │ 00   │ │ 00   │ │ 00   │
└──────┘ └──────┘ └──────┘ └──────┘ └──────┘ └──────┘
(NOTE 2)
```

NOTES:

1.    Model 20 only

2.    Part of processor cabinet T3135-00

Figure 1-12.  Models 10/15/20 Maximum Processor Cabinet Configuration

```
                          ┌──────────────┐
                          │              │
                          │     MCU      │
                          │              │
                          └──────────────┘
                                (NOTE 1)

        ┌──────────────┐                    ┌──────────────┐
        │     BMU      │                    │     BMU      │
        │     2MB      │                    │     4MB      │
        │   F4864-00   │                    │   F4864-01   │
        └──────────────┘                    └──────────────┘
```
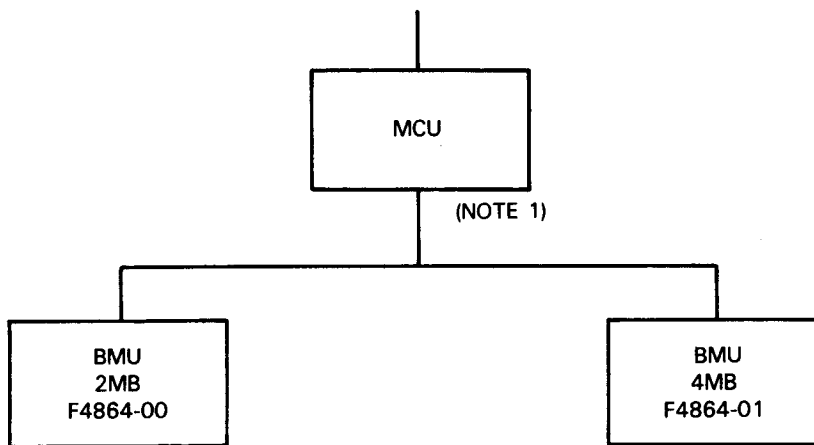
NOTES:

1.  Part of processor cabinet T3135-00

2.  One 2MB memory expansion can occur for model 10. Additional increments
    must be 4MB. All model 15 or 20 increments are 4MB. The maximum
    configurations are 8MB for model 10; 12MB for model 15; 16MB for model
    20.

**Figure 1-13.  Models 10/15/20 Storage Configuration**

### 1.2.3.  Models 8/10/15/20 Configurations

Figures 1-14 to 1-25 show configurations common to the models 8/10/15/20.

ISC1* ISC2*

```
          ┌──────────────────────┐
          │      T5058-00/01      │
          │   TAPE CONTROLLER     │
          └──────────────────────┘
                  U22/24
            ALL FEATURES SUPPORTED

          ┌──────────────────────┐
          │       T8494-99        │
          │    DISK SUBSYSTEM     │
          └──────────────────────┘
            ALL FEATURES SUPPORTED

          ┌──────────────────────┐
          │      T5039-00/01      │
          │    DISK CONTROLLER    │
          └──────────────────────┘
       8430, 8433 DISK DRIVES (16 MAX.)
            ALL FEATURES SUPPORTED

          ┌──────────────────────┐
          │      T5045-04/05      │
          │   TAPE CONTROLLER     │
          └──────────────────────┘
              U10/14 TAPE DRIVES
            ALL FEATURES SUPPORTED

          ┌──────────────────────┐
          │      T5034-00/01      │
          │   TAPE CONTROLLER     │
          └──────────────────────┘
       U12/16/20 TAPE DRIVES (16 MAX.)
            ALL FEATURES SUPPORTED

          ┌──────────────────────┐
          │      T5017-00/01      │
          │   TAPE CONTROLLER     │
          └──────────────────────┘
       U12/16/20 TAPE DRIVES (16 MAX.)
            ALL FEATURES SUPPORTED

          ┌──────────────────────┐
          │    T0716-00 THRU 07   │
          │    CARD READER AND    │
          │      CONTROLLER       │
          └──────────────────────┘

          ┌──────────────────────┐
          │    T0770-02 THRU 07   │
          │ PRINTER AND CONTROLLER│
          └──────────────────────┘
             800/1400/2000 LPM

          ┌──────────────────────┐
          │      T5055-00/01      │
          │   TAPE CONTROLLER     │
          └──────────────────────┘
           U22/24 26/28 TAPE DRIVES

          ┌──────────────────────┐
          │      3200 SERIES      │
          │   TAPE CONTROLLER     │
          └──────────────────────┘
           3200 SERIES TAPE DRIVES
                  (8 Max.)

          ┌──────────────────────┐
          │    T0776-00 THRU 05   │
          │ PRINTER AND CONTROLLER│
          └──────────────────────┘

          ┌──────────────────────┐
          │       9246-14B        │
          │ PRINTER AND CONTROLLER│
          └──────────────────────┘
                  1500 LPM

          ┌──────────────────────┐
          │     DCP 15** OR       │
          │       DCP 40**        │
          └──────────────────────┘
```

* If only freestanding control units are
connected to a selector channel, the
maximum that may be connected is 8.
If freestanding control units are
intermixed with IDCUs, the maximum
is four control units. If only IDCUs are
connected, the maximum is 3.

**Requires a dedicated selector channel (ISC).

DISK CONFIGURATIONS
(Figure 1-23)

Figure 1-14. Selector Channel Configuration

IOMP (MODEL 8)
F3367-01 OR
IOP (MODELS 10/15/20)
F4809-00

| SDMA | MLCM |
|---|---|
| F2795-01 | F2796-01 |

IOMP (MODEL 8)
F3367-01 OR
IOP (MODELS 10/15/20)
F4809-00

| SDMA | MLCM |
|---|---|
| F2795-02 | F2796-02 |

I/O CABINET
T1982-XX
(NOTE 11)

EXPANSION
CABINET
T1982-XX

DISKETTE
CONTROLLER
(NOTES 4,6)
F3427-01

WORKSTATION
CONTROLLER
(NOTES 4,8,10)
F2791-08

WORKSTATION
CONTROLLER
(NOTE 8)
F2791-04

I/O SUBSYSTEM
EXPANDER
(NOTE 10)
F2908-00 (1 MAX.)

INTEGRATED
TAPE
CONTROLLER
F3774-00
(NOTE 10)

PAPER
PERIPHERAL
CONTROLLER
(NOTES 2,4,8)
F2789-02

REMOTE
PRINTER
INTERFACE
(NOTE 9)
F2794-00

SLCA
FEATURES
(FIG. 1–10)

TO
DISKETTES

1  8
WORKSTATION
IN ANY
INTERMIX
T3560 10/11
T3561 10/11

1  8
WORKSTATIONS
IN ANY
INTERMIX
T3560-10/11
T3561-10/11

TAPE DRIVES
T0871-XX

STREAMING
TAPE

CARD
PUNCH
75/160 LPM
80 COL
T0608-03/04/05

READER
FEATURE

F2830-00

ONE PRINTER
OF THE
FOLLOWING:
T0789-00/02
180 LPM
T0789-03/05
300 LPM
T0789-06/07/08
640 LPM
T0776-06/07
1200 LPM
T0798-00/01/02
75 LM
(NOTES 3,5,7)

ONE PRINTER
OF THE
FOLLOWING:
T0789-00/02
180 LPM
T0789-03/05
300 LPM
T0789-06/08
640 LPM
T0798-00
01/02
75 LM
(NOTES 3,5,7)

CARD READER
80 COL
380 CPM
T0719-04/05
14/18
600 LPM
T0719-06/07
15/19

REMOTE
PRINTER
ATTACHMENT
F1955-00/01

PRINTER
75 LPM
T0798-00/01/02
(NOTE 3)

PRINTER
T0789-00 THRU -03 180 LPM
-04/-05 300 LPM
-06 THRU -08 640 LPM
(NOTE 3)

NOTES:

1. Reference configuring system expansion for additional limitations.

2. A maximum of 4 PPCs/IOP.

3. Refer to type and feature description for listing of feature and selections.

4. Each system configuration requires a minimum of one diskette and workstation controller and either a paper peripheral controller or a byte adapter.

5. Maximum aggregate data rate for both line printer connections on paper peripheral controller F2789 must not exceed 1500 LPM.

6. A maximum of two I/O Processors per system.

7. The T0798 printer requires, as a prerequisite, either T0799 or T0776 printer in the system configuration at the host site.

8. A maximum of 15 PPCs and WSC per system with no more than 8 PPCs and 15 WSC if the system printer is configured on the byte adapter or selector channel. Otherwise, the WSC maximum is 14.

9. A maximum of 12 remote printer interfaces per system.

10. A maximum of one per system. I/O subsystem expander may be physically configured with the integrated tape controller, on the same IOP channel, but their operations are mutually exclusive.

11. Model 8 I/O cabinet is T1982-00. Models 10/15/20 use I/O cabinet T1982-00 with F5060-00

**Figure 1-15. I/O Cabinet Configuration**

ISC/SEL

IOMP/IOP

IOMP/IOP

EXPANSION CABINET

(NOTE 9)

IDCU
FEATURES

DISKETTE
CONTROLLER
(NOTE 5)
F3427-01

WORKSTATION
CONTROLLER
(NOTE 6)

F2791-04

I/O SUBSYSTEM
EXPANDER
(NOTE 8)
F2908-01(1 MAX.)

INTEGRATED
TAPE
CONTROLLER
F3774-00
(NOTE 8)

CIU
F2802-01

(NOTE 5)

PAPER
PERIPHERAL
CONTROLLER
(NOTES 2,6)
F2789-02

REMOTE
PRINTER
INTERFACE
(NOTE 7)
F2794-00

SLCA
FEATURES

OR

TO
DISKETTES

1 · · · · · · · 6
WORKSTATIONS
IN ANY INTERMIX
T3560-10/11
T3561-10/11

TAPE DRIVES
T0871-XX

INTEGRATED TAPE
CONFIGURATION

CARD PUNCH
75/160 LPM
80 COL
T0608-03/04/05

READER
FEATURE
F2830-00

ONE PRINTER
OF THE
FOLLOWING
T0789-00/02
180 LPM
T0789-03/05
300 LPM
T0789-06/07/08
640 LPM
T0776-06/07
1200 LPM
T0798-00/01/02
75 LM
(NOTES 3,4)

ONE PRINTER
OF THE
FOLLOWING:
T0789-00/02
180 LPM
T0789-03/05
300 LPM
T0789-06/08
640 LPM
T0798-00/01/02
75 LM

(NOTES 3,4)

CARD READER
80 COL
300 CPM
T0719-04/05
14/18
600 LPM
T0719-06/07
15/19

REMOTE
PRINTER
ATTACHMENT
F1955-00/01

PRINTER
75 LPM
T0798-00/01/02
(NOTE 3)

PRINTER
T0789-00 THRU 03
180 LPM
04/05 300 LPM
06 THRU 09 640 LPM
(NOTE 3)

NOTES:

1. Reference configuring system expansion for additional limitations.

2. A maximum of 4 PPCs/IOP or IOMP.

3. Refer to type and feature description for listing of feature and selections.

4. Maximum aggregate data rate for both line printer connections on paper peripheral controller F2789 must not exceed 1500 LPM.

5. A maximum of two IOMPs or IOPS per system.

6. A maximum of 15 PPCs and WSC per system with no more than 8 PPCs and 15 WSC, if the system printer is configured on the byte adapter or selector channel. Otherwise, the WSC maximum is 14.

7. A maximum of 12 remote printer interfaces per system.

8. A maximum of one per system. I/O subsystem expander may be physically configured with the integrated tape controller on the same SDMA channel, but their operations are mutually exclusive.

9. IDCUs in the expansion cabinet and freestanding controllers may not be connected to the same ISC.

**Figure 1-16. I/O Expansion Cabinet Configuration**

FROM DISKETTE CONTROLLER
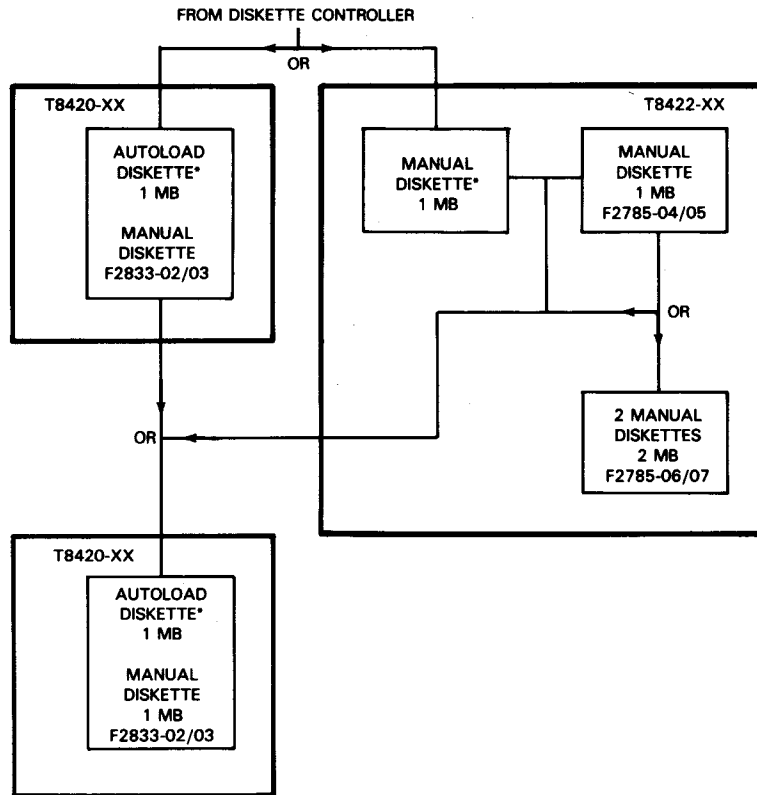


\* A maximum of 4 diskettes, autoload (2 max.) T8420-XX or manual T8422-XX per diskette
controller. A maximum of 4 diskettes per system.

**Figure 1-17.  Diskette Drive Configuration**
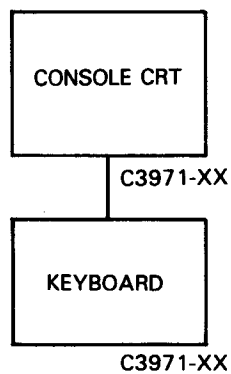


NOTE:

CRT character set and keycaps selection required.

| C397100 | Domestic |
|---------|----------|
| -01 | United Kingdom |
| -02 | Germany |
| -03 | France |
| -04 | Spain (Model 8) |
| -05 | Denmark/Norway |
| -06 | Sweden/Finland |
| -07 | Italy |
| -09 | Spain (Models 10/15/20) |

**Figure 1-18.  Console Display Configuration**
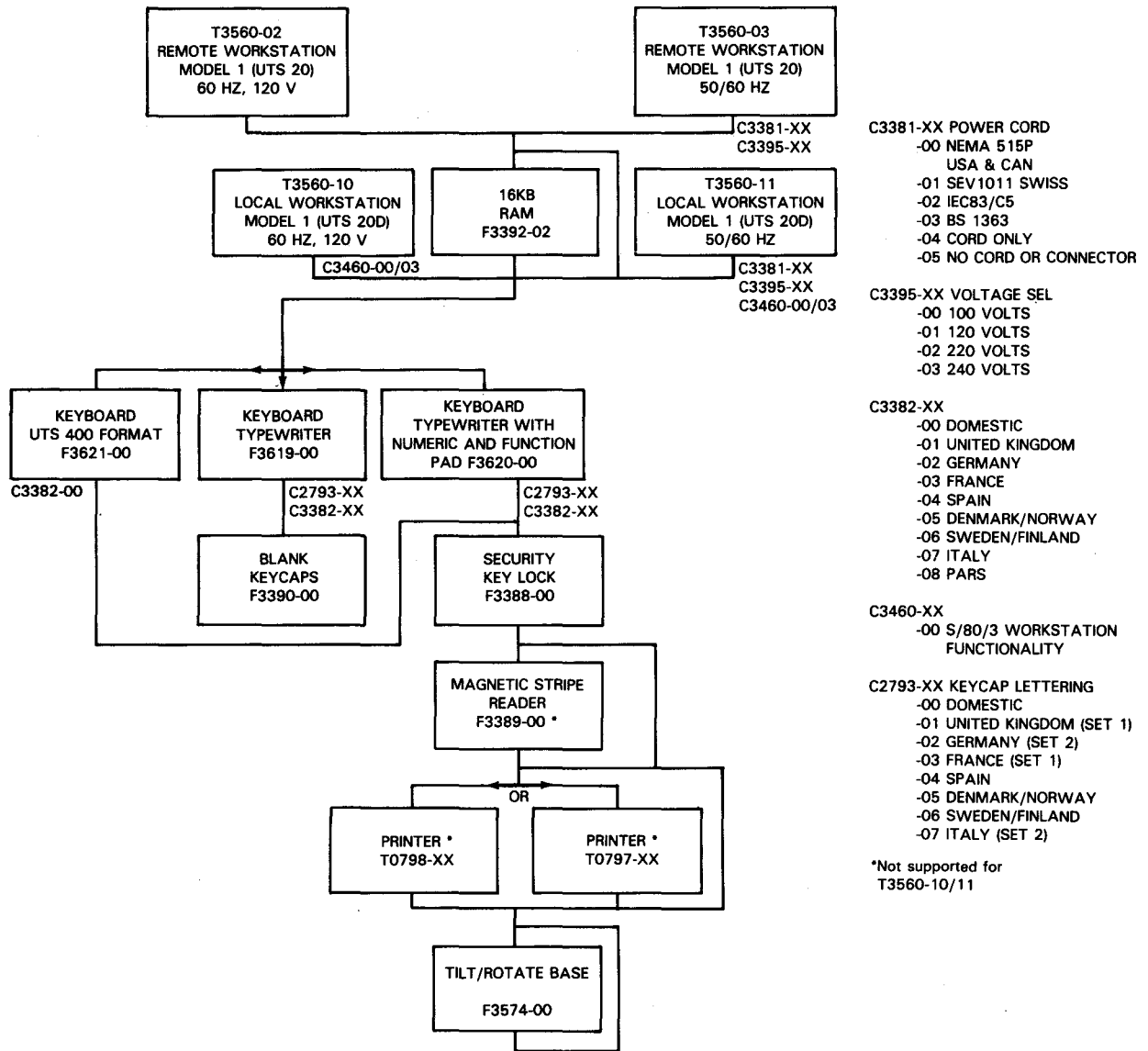
Figure 1-19. Local/Remote Workstation, Model 1, Configuration

**Figure 1-20. Local/Remote Workstation, Model 2, Configuration (part 1 of 2)**

(A)
(FROM PART 1)
BLANK KEY CAPS

```
┌─────────────────────┐
│   MAGNETIC STRIPE   │
│      READER         │
│     F3389-00        │
└─────────────────────┘
```
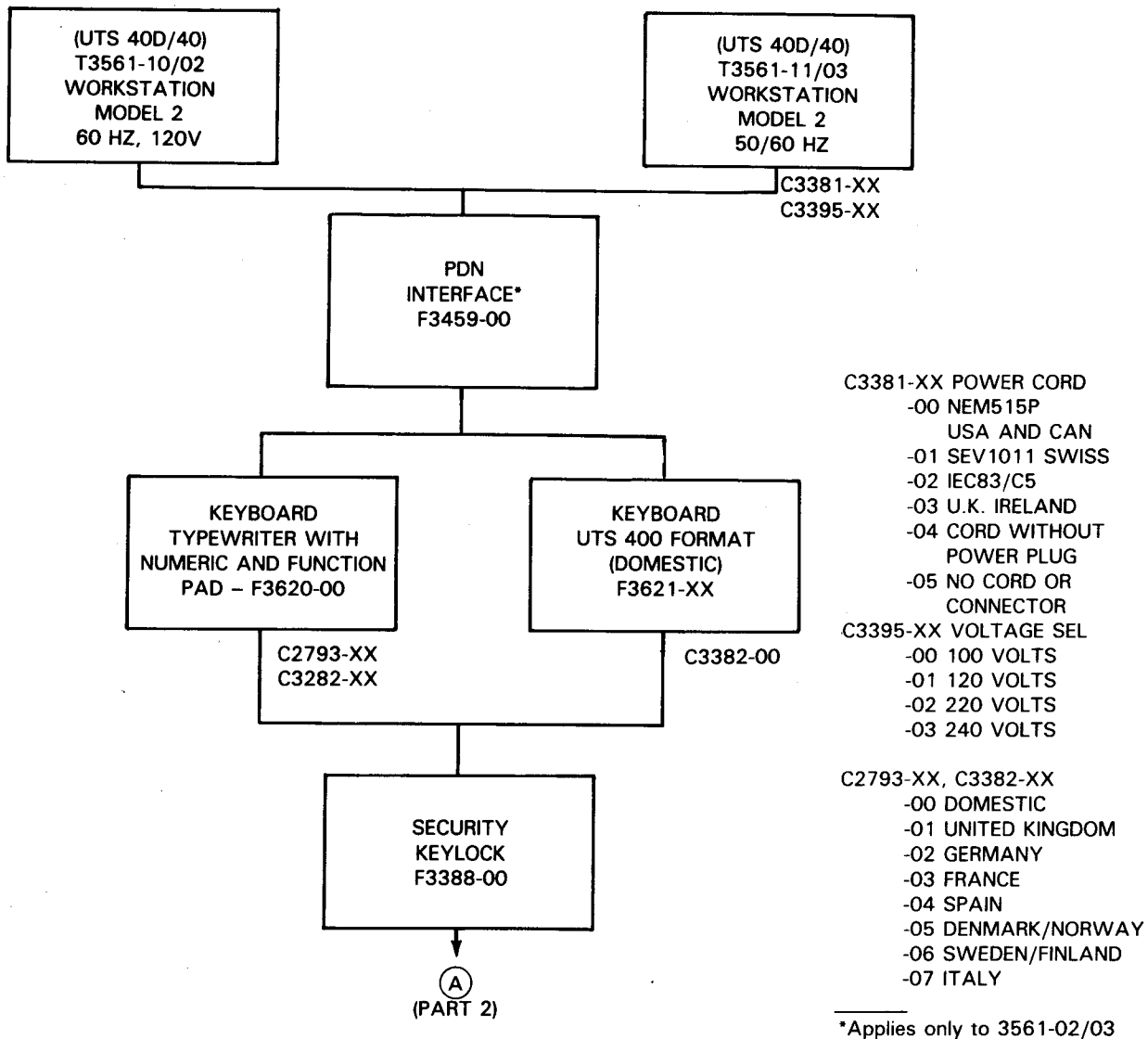
EXPANSION FEATURE 1

F3643-00 8-BIT PERIPHERAL INTERFACE
F3642-00 32KB USER MEMORY
F3642-01 32KB EXPANSION

```
┌──────────────────────────┐
│   EXPANSION FEATURE 1:    │
│     8-BIT PERIPHERAL      │
│    INTERFACE AND/OR       │
│   32KB OF USER MEMORY     │
│ WITH 32KB EXPANSION OPTION│
└──────────────────────────┘
```

EXPANSION FEATURE 2

F3644-00 EXPANSION MODULE
F3644-02 8-BIT PERIPHERAL
            INTERFACE EXPANSION
F3644-03 LOADABLE CHARACTER SET
F3644-01 LIGHT PEN

```
┌──────────────────────────┐
│   EXPANSION FEATURE 2:    │
│    EXPANSION MODULE       │
│    AND/OR LIGHT PEN       │
│ AND/OR LOADABLE CHARACTER │
│           SET             │
│   AND/OR 8-BIT PERIPHERAL │
│   INTERFACE EXPANSION     │
└──────────────────────────┘
```

* Up to 2 printers and 2 diskettes
  may be attached to a workstation
  through the 8-bit peripheral interface.
  These include:

  .0425-XX 132 col. matrix printer
  .0789-00 through -05 300 lpm printer
  .0797-00,-01 80-col. matrix printer
  .0791-00,-01,-02,-03 correspondence
      quality printer
  .8406-04,-05,-06,-07 1 MB diskette

```
┌─────────────────────┐
│                     │
│     PRINTER*        │
│                     │
└─────────────────────┘
```

```
┌─────────────────────┐
│   TILT/ROTATE BASE  │
│     F3574-00        │
└─────────────────────┘
```

Figure 1-20.  Local/Remote Workstation, Model 2, Configuration (part 2 of 2)

```
┌─────────────────────┐      ┌─────────────────────┐      ┌─────────────────────┐
│      SVT 1122       │      │      SVT 1123       │      │      SVT 1124       │
│  LOCAL WORKSTATION  │      │  REMOTE WORKSTATION │      │  REMOTE WORKSTATION │
│      T3612-02       │      │  T3612-00 & F5069-00│      │  T3612-00 & F5069-01│
│   96-264V, 50/60 Hz │      │   96-264V, 50/60 Hz │      │   96-264V, 50/60 Hz │
└─────────────────────┘      └─────────────────────┘      └─────────────────────┘
  C3381-XX                     C3381-XX                          C3381-XX
```

OR

```
┌─────────────────────┐      ┌─────────────────────┐      ┌─────────────────────┐
│    WORKSTATION      │      │      RS232,         │      │     TERMINAL        │
│    CONTROLLER       │      │   CCITT V.24        │      │   MULTIPLEXER       │
│    CONNECTORS       │      │    INTERFACE        │      │    INTERFACE        │
│    F8265-00         │      │    CONNECTION       │      │    CONNECTION       │
│    F8266-XX         │      │    F8201-XX         │      │    F8217-XX         │
└─────────────────────┘      └─────────────────────┘      └─────────────────────┘
```

```
┌─────────────────────┐
│     KEYBOARD        │
│     F4725-XX        │
└─────────────────────┘
```

OR

```
┌──────────────┐  ┌──────────────┐  ┌──────────────┐  ┌──────────────┐
│   MODEL 15   │  │   MODEL 21   │  │   MODEL 25   │  │  MODEL 115   │
│   PRINTER    │  │   PRINTER    │  │   PRINTER    │  │   PRINTER    │
│ T0445-00/01  │  │  T0471-00    │  │ T0425-07/08  │  │  T0472-00    │
│  (NOTE 1)    │  │              │  │  (NOTE 1)    │  │  (NOTE 2)    │
├──────────────┤  ├──────────────┤  ├──────────────┤  ├──────────────┤
│  F8290-XX    │  │  F8290-XX    │  │  F8290-XX    │  │  F8290-XX    │
│  F8291-XX    │  │  F8291-XX    │  │  F8291-XX    │  │  F8291-XX    │
└──────────────┘  └──────────────┘  └──────────────┘  └──────────────┘
```

NOTES:

1. Requires F3860-04 printer interface.

2. Requires F4643-00 printer interface.

Figure 1-21. Local/Remote Workstation, SVT 112X, Configuration

FROM MLCM
OF IOMP/IOP 1 OR 2

| SLCA AUTO DIAL F3794-00/01 | SLCA 9600 BPS SYNC F2788-XX | SLCA 9600 BPS SYNC F2798-XX | SLCA 9600 BPS ASYNC F2799-XX OHM (TTY,DCT 500) | SLCA 56KBPS SYNC F2986-XX BSC NTR |

| RS366 | MICROCODE OHM FUNCT. 4800 BPS FD F2788-02/03 NOTE 1 | MICROCODE NTR F2788-04/05 | MICROCODE NTR BSC, UTS 400 F2798-03 | MICROCODE UDLC F2798-00/02/05 | MICROCODE UTS 400 F2798-06/07 | MICROCODE UDLC F2986-01/02 | MICROCODE BSC F2986-00/03 | MICROCODE NTR F2986-04/05 |

| RS 232 X.21 BIS F2788-02/04 | MIL 108-100 F2788-03/05 | RS 449 X.21 BIS F2798-05/07 | RS 232 F2798-00/06 | X.21 F2798-02/03 | RS 232 X.21 BIS F2799-00 | MIL 188-100 F2799-01 | CCITT Y35 F2986-00/01/05 | RS449 F2986-02/03/04 |

| C3401  C3311 | C3401 | C3590 | C3590 | C3590 | C3401 | C3401 | | |
| C3402 | C3402 | C3591 | C3591 | C3591 | C3402 | C3402 | | |
| C3403 | C3404 | C3592 | C3592 | C3592 | C3403 | C3404 | | |
| | C3406 | | | | C3405 | C3405 | | |
| | C3407 | | | | C3408 | C3409 | | |
| | C3409 | | | | | C3411 | | |
| | C3410 | | | | | | | |

NOTES:

1. CMM emulator provides the same level of support as the 90/30 CA. It operates at 9600 BPS in half duplex and 4800 BPS in full duplex.

2. SLCA selections for F2798-05/06/07 are C3822/C3823/C3824 and SLCA selections for F2798-00 are C3590/C3591/C3592.

3. One auto dial feature supports up to 3 SLCAs. SYNC or ASYNC to 9600 BPS. It replaces one low or medium (L/M) SLCA.

4. A maximum of 14 low- or medium-speed half-duplex SLCAs, 7 high-speed full-duplex SLCAs, or 12 high-speed half-duplex SLCAs configured per I/O processor.
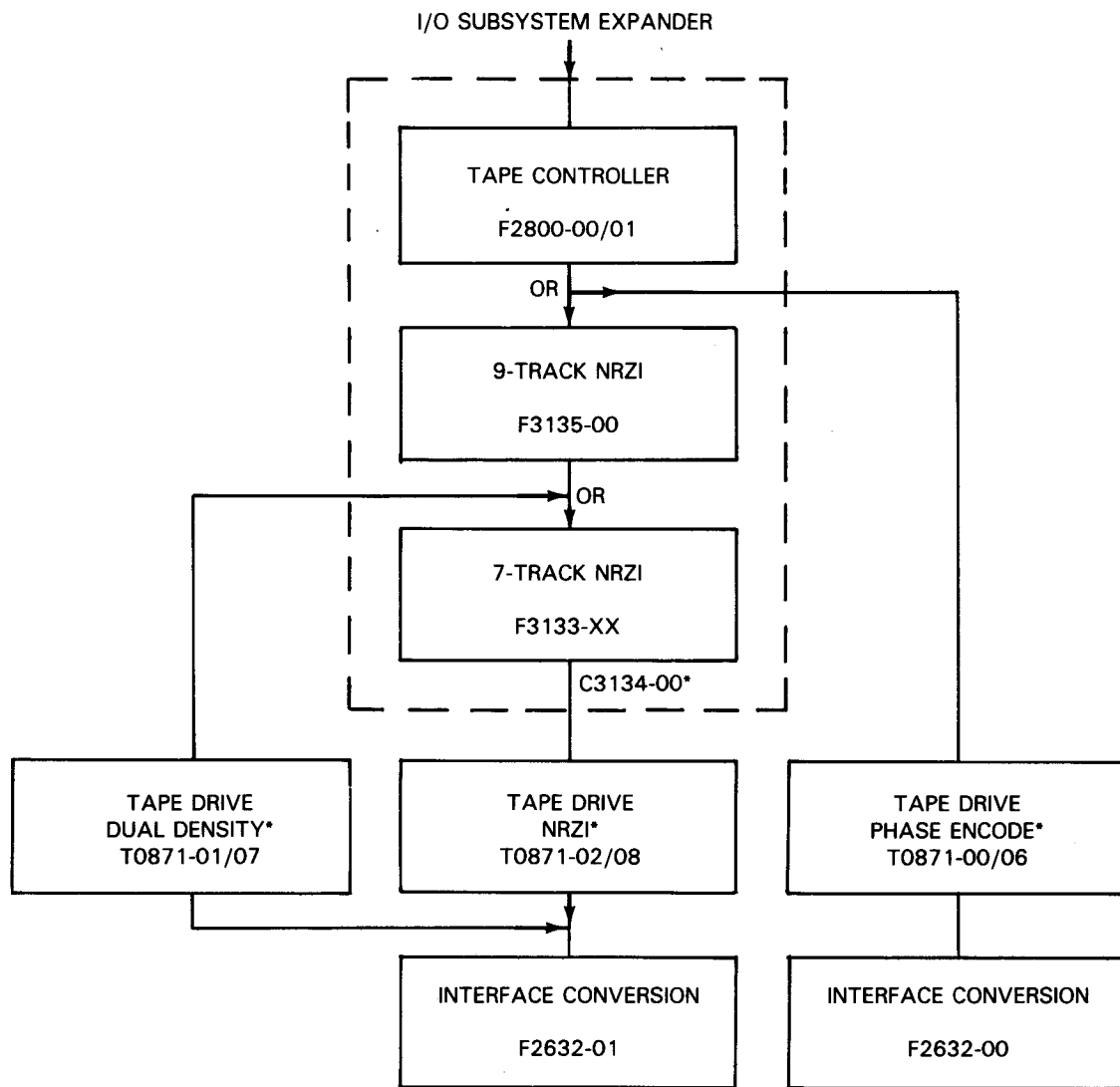
**Figure 1-22.  Systems Communications Configuration**

SELECTOR CHANNEL (NOTE 3)

I/O CABINET OR EXPANSION CABINET
T1982-XX

IDCU (NOTE 10)

IDCU (NOTE 7)

IDCU

IDCU

(NOTES 3, 9)

(NOTES 2, 8)

DUAL ACCESS

FIXED MEDIA DISK CABINET T8417-00/01

(NOTE 4)

T8419-00/01 72.3MB

T8416/18 29/58MB

(NOTE 4)

FIXED MEDIA DISK DRIVE T8470-00/01

HDA 495MB

FIXED MEDIA DISK DRIVE F2834-00/01

FIXED MEDIA DISK DRIVE F2834-00/01

FIXED MEDIA DISK DRIVE F2834-00/01

FIXED MEDIA DISK DRIVE T8470-00/01 T8480-00/01

FIXED MEDIA DISK DRIVE T8470-00/01 T8480-00/01

HDA 118.2MB

(NOTE 11)

HDA 495MB

HDA 495MB

NOTES:

1. Reference system expansion figures for additional limitations.

2. A maximum of 8 drives may be connected in either single or dual access.

3. A maximum of 3 integrated disk control units (IDCUs) can be configured to any selector channel in any combination except where noted. However, a maximum of 6 IDCUs can be configured in the system.

4. Any combination of disk drives may be selected to a maximum of 8.

5. A maximum of 24 disk drives is allowed in any configuration.

6. All IDCUs connected to a selector channel must reside in the same cabinet.

7. A maximum of 1 F3734-00 IDCU and 8 8416/18 disk drives is allowed in any intermix per system. When more than 4 drives are installed, T2408 disk power expansion is required.

8. Disk power expansion T2413 is required for every 8 T8470-XX or T8480-XX disk drives configured.

9. IDCUs residing in expansion cabinet T1982-03 may not be connected with freestanding controllers on the same selector channel.

10. A maximum of 1 F3734-01 IDCU and 8 8417/19 disk drives is allowed in any intermix per system.
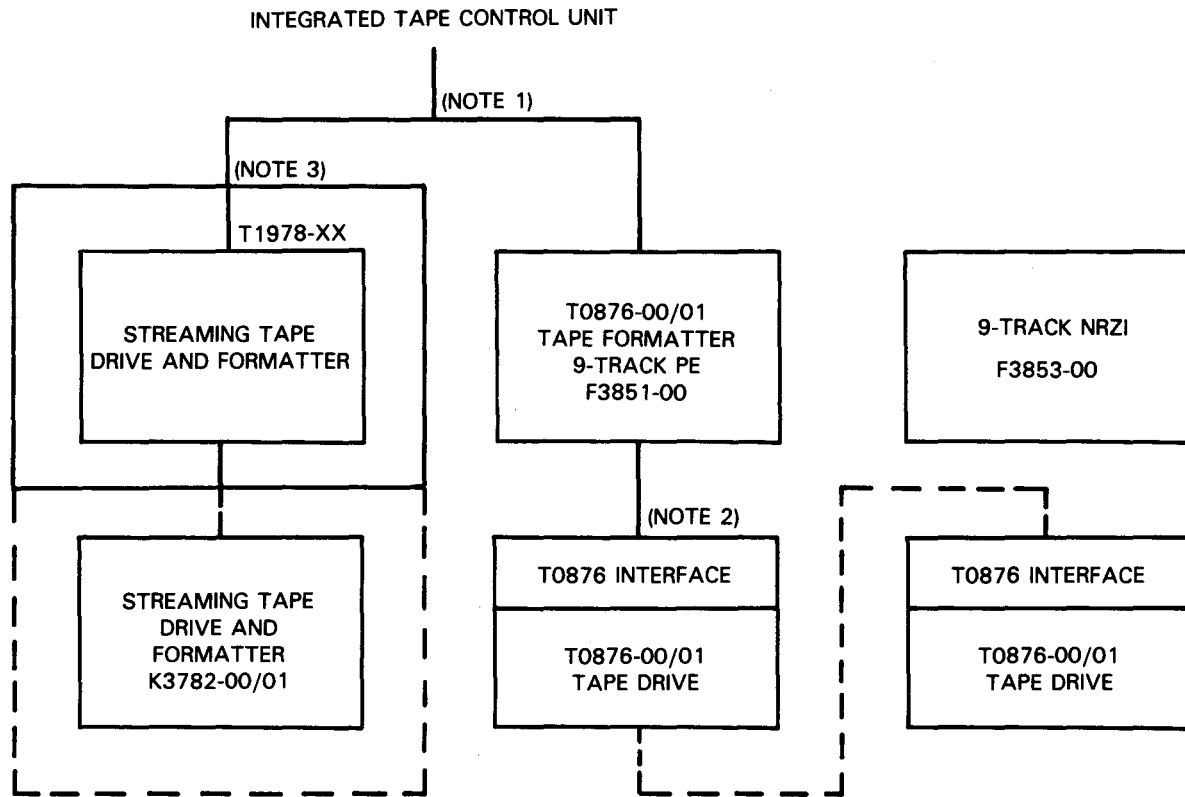
11. One HDA must be selected for each disk drive.

Figure 1-23. Integrated Disk Subsystems Configuration

I/O SUBSYSTEM EXPANDER

```
                    ┌─────────────────────────┐
                    │   TAPE CONTROLLER        │
                    │                          │
                    │   F2800-00/01            │
                    └─────────────────────────┘
                           OR ───────────────────────────┐
                    ┌─────────────────────────┐          │
                    │   9-TRACK NRZI           │          │
                    │                          │          │
                    │   F3135-00               │          │
                    └─────────────────────────┘          │
          ┌─────────────────► OR                          │
          │         ┌─────────────────────────┐          │
          │         │   7-TRACK NRZI           │          │
          │         │                          │          │
          │         │   F3133-XX               │          │
          │         └─────────────────────────┘          │
          │                    C3134-00*                  │
          │                                               │
┌──────────────────┐  ┌──────────────────┐  ┌──────────────────┐
│   TAPE DRIVE     │  │   TAPE DRIVE     │  │   TAPE DRIVE     │
│  DUAL DENSITY*   │  │     NRZI*        │  │  PHASE ENCODE*   │
│   T0871-01/07    │  │   T0871-02/08    │  │   T0871-00/06    │
└──────────────────┘  └──────────────────┘  └──────────────────┘
          └──────────────────►                        │
                      ┌──────────────────┐  ┌──────────────────┐
                      │ INTERFACE        │  │ INTERFACE        │
                      │ CONVERSION       │  │ CONVERSION       │
                      │ F2632-01         │  │ F2632-00         │
                      └──────────────────┘  └──────────────────┘
```

* One tape drive per cabinet. The F2800 controller is located in the first tape cabinet. Up to 8 tape drives T0871-XX in any combination can be supported.

**Figure 1-24.  UNISERVO® 10 Magnetic Tape Subsystem Configuration**

INTEGRATED TAPE CONTROL UNIT

(NOTE 1)

(NOTE 3)

T1978-XX

```
┌─────────────────────────────────┐
│  ┌──────────────────────┐       │
│  │ STREAMING TAPE       │       │
│  │ DRIVE AND FORMATTER  │       │
│  └──────────────────────┘       │
│  ┌──────────────────────┐       │
│  │ STREAMING TAPE       │       │
│  │ DRIVE AND            │       │
│  │ FORMATTER            │       │
│  │ K3782-00/01          │       │
│  └──────────────────────┘       │
└─────────────────────────────────┘
```

T0876-00/01
TAPE FORMATTER
9-TRACK PE
F3851-00

9-TRACK NRZI
F3853-00

(NOTE 2)

T0876 INTERFACE

T0876-00/01
TAPE DRIVE

T0876 INTERFACE

T0876-00/01
TAPE DRIVE

NOTES:

1.    A maximum of 4 tape formatters is allowed with no more than 1 F3851-00.

2.    A maximum of 8 T0876-00/01 tape drives is supported.

3.    A maximum of 2 T1978-XX cabinets is allowed.

**Figure 1-25.  Streaming Magnetic Tape Configuration**

## 1.3. EQUIPMENT TYPES AND OPTIONAL FEATURES

The tables in this section describe the following equipment types and optional features that can be configured in the models 8/10/15/20 processor complex:

- Model 8 processor equipment (Table 1-1)

- Models 10/15/20 processor equipment (Table 1-2)

- I/O cabinet and I/O expansion cabinet equipment (Table 1-3)

- Magnetic disks (Table 1-4)

- Magnetic tapes (Table 1-5)

- Paper peripherals (Table 1-6)

- Workstations and terminals (Table 1-7)

- Ancillary products (Table 1-8)

### Table 1-1. Model 8 Processor Equipment

| Type/Feature | Description |
|---|---|
| Processor Cabinet T3076-00 | A general purpose microprogrammed processor that includes:<br><br>■ Control storage (COS)<br>■ Byte multiplexer<br>■ System control processor<br>■ Power supply and control<br>■ Electronics module for CPU<br>■ Channels and control<br>■ M-bus adapter (MBA)<br>■ Main storage unit (1 MB)<br>■ Channel controller (CHC)<br>■ Integrated selector channel (ISC)<br><br>The T3076-00 processor requires:<br><br>■ Disk drive T8416/8418, T8417/8419, or T8470/8480 and associated controller, or T8430/8433 and associated controller<br><br>■ Byte adapter F3961-00 with printer if paper peripheral controller is not selected in T1982, or printer is not configured in ISC<br><br>■ Console T4025-XX with matching keycap and display character sets per selection from C3971-XX<br><br>■ I/O cabinet T1982-00<br><br>Requires 208/240/381/415 Vac, 50/60 Hz, three-phase power. The system resident disk does not contain system control software, microcode, and online diagnostic. A -2.8 Vdc supply F3964-01 is required when the second MSU, F3958-00 and the second CHC, F3960-00 are added. |
| System Power Expansion F3964-01 | Provides +2.8 Vdc power supply expansion for T3076-00 |
| Main Storage Unit F3958-00 | Provides a main storage unit and 1 MB of main storage. Allows a maximum of 4 MB of main storage. |
| Main Storage F3959-00 | Provides 1 MB of main storage |
| Main Storage F3959-01 | Provides 2 MB of main storage |
| Channel Controller (CHC) F3960-00 | Provides the capability of controlling up to 3 ISC channels, F3962-00, and the resident byte multiplexer, or 2 ISC channels when it is the second CHC configured. Data transfer rate is 4 MB/second. |
| Byte Adapter F3961-00 | A controller that supports up to four low speed peripherals. The controller interfaces to the byte multiplexer and provides a SU00039 interface capability to the associated peripherals. Maximum data is at the rate of 40 kB/s for line printers that operate at 2000 lpm. |
| Integrated Selector Channel (ISC) F3962-00 | An integrated microprogrammed channel that provides support for a maximum of 3 integrated disk control units or 8 freestanding control units in any combination. An integrated selector channel can also support DCP 15s and DCP 40s, but the SEL must be dedicated to only these devices. The channel supports concurrent control operations in the device but only one data transfer at 1.5 MB per second maximum. |

**Table 1-1. Model 8 Processor Equipment (cont)**

| Type/Feature | Description |
|---|---|
| Console Cabinet T4025-00 | Serves for operator system control and consists of a monochromatic CRT display and a typewriter style keyboard. Contains power supply and control, diskette drives for system initialization, and diagnostics. Powered from processor cabinet T3076-00 with 220 Vac, 60 Hz. Requires selection C3971-XX for keycap and display character set. Selections are:<br><br>C3971-00  Domestic<br><br>C3971-01  United Kingdom<br><br>C3971-02  Germany<br><br>C3971-03  France<br><br>C3971-04  Spain<br><br>C3971-05  Denmark/Norway<br><br>C3971-06  Sweden/Finland<br><br>C3971-07  Italy |
| Console Cabinet T4025-01 | Same as T4025-00 except that it is powered from T3076-01, with 220 Vac, 50 Hz. |

**Table 1-2. Models 10/15/20 Processor Equipment**

| Type/Feature | Description |
|---|---|
| Processor Cabinet T3135-00 | A multipurpose microprogrammed pipelined processor that has an instruction cache and control for up to 16 MB of main memory. It also includes:<br><br>■ Basic processing unit (BPU)<br>■ Memory control unit (MCU)<br>■ System control processor (SCP)<br>■ Selector channel (SEL)<br>■ Mainframe interface adapter (MIA)<br>■ Power supply and control electronics module for BPU, channels and control<br>■ Two flexible disk drives for system use<br><br>The T3135-00 processor requires:<br>■ Disk drive types T8417/8419, T8470/8480, or T8494 and associated controller<br>■ Console T4028-00 with matching keycap and display character sets per selection from C3971-XX<br>■ I/O cabinet T1982-04 or T1982-00 with F5060-00<br><br>The T3135-00 processor also requires selection of the following model-dependent features:<br><br>Model 10:<br><br>■ 2 MB basic memory unit F4864-00<br>■ System microcode 10 F4865-00<br><br>Model 15:<br><br>■ 4 MB basic memory unit F4864-01<br>■ System microcode 15 F4865-02<br><br>Model 20:<br><br>■ 4 MB basic memory unit F4864-01<br>■ System microcode 20 F4865-01<br>■ Operand cache F4866-00<br>■ Floating point processor F4867-00<br><br>Requires 208/220/240 Vac, 50/60 Hz, single-phase power. Provides 115 Vac single-phase power to the system console. |
| Basic Memory Unit 2 MB F4864-00 | Provides 2 MB of main storage. (Available only to expand a model 10 from 2MB to 4MB. Otherwise, select F4864-01.) |
| Basic Memory Unit 4 MB F4864-01 | Provides 4 MB of main storage. |
| Operand Cache F4866-00 | Provides an operand cache required for model 20. |
| Floating Point Processor F4867-00 | Provides floating point processor required for model 20. |
| Selector Channel F4868-00 | A microprogrammed selector channel that supports a maximum of 3 integrated disk control units and one freestanding control unit, or 8 freestanding SU00208 control units or DCP/15s and/or DCP/40s. (For SEL-DCP configurations, the SEL must be dedicated to the DCP.) The channel supports concurrent control operations in devices, but only one data transfer at a maximum 2.2 MB/sec rate. |

(continued)

## Table 1-2.  Models 10/15/20 Processor Equipment (cont)

| Type/Feature | Description |
|---|---|
| System Microcode 10 F4865-00 | Provides model 10 system loadable microcode for BPU, SCP, SEL, and IOP. Contained on system diskette. |
| System Microcode 15 F4865-02 | Provides model 15 system loadable microcode for BPU, SCP, SEL, and IOP. Contained on system diskette. |
| System Microcode 20 F4865-01 | Provides model 20 system loadable microcode for BPU, SCP, SEL, and IOP. Contained on system diskette. |
| Console T4028-00 | Serves for operator system control and consists of a monochromatic CRT display, system control panel, and a typewriter style keyboard. Requires selection C3971-XX for keycap and display character set. Powered from processor cabinet T3135-00 with 115 Vac, 50/60 Hz. Selections are:<br><br>C3971-00 Domestic<br><br>C3971-00 United Kingdom<br><br>C3971-02 Germany<br><br>C3971-03 France<br><br>C3971-05 Denmark/Norway<br><br>C3971-06 Sweden/Finland<br><br>C3971-07 Italy<br><br>C3971-09 Spain |

## Table 1-3. I/O Cabinet and Expansion Cabinet Equipment

| Type/Feature | Description |
|---|---|
| **MODEL 8 ONLY** ||
| I/O Cabinet T1982-00 | Cabinet for low speed channels, integrated controllers and expansion capability for I/O and communications. Includes power supply, power control, and an electronics module. Requires 208/240/381/415 Vac, 50/60 Hz, three-phase power. Requires: <br>■ IOMP F3367 with SDMA F2795 <br>■ Diskette controller F3427-01 with diskette drive T8420 or T8422. <br>■ Paper peripheral controller F2789 or byte adapter with line printer if line printer is not configured in ISC <br>■ Workstation controller F2791-08 <br>■ IDCU (integrated disk control unit), F3734-XX with appropriate disk drive if T5039 and 8430/8433 disk drives are not used |
| Expansion Cabinet T1982-03 | Provides a facility to expand the I/O and communications capabilities of the system beyond the I/O cabinet. The expansion includes a power supply, power control, and an electronics module. Requires and interfaces to a second IOMP F3367 in the I/O cabinet T1982-00 except for IDCU expansion. A power supply feature F3964-02, +5 Vdc, is required when more than 8 control units/SLCA/IDCUs are added and an IDCU has a weight of 1. Peripheral power sequencer F3784-XX may be added. Requires 208/240/381/415 Vac, 50/60 Hz, three-phase power. |
| I/O Expansion Cabinet T1982-05 | Provides a facility to expand the I/O and communications capabilities of the system beyond the I/O cabinet. The expansion includes a power supply and electronics module. Requires and interfaces to second IOMP (F3367) in I/O cabinet T1982-00 except for IDCU expansion. <br><br>A +5V power supply feature, F3964-06, is required when the sum of the Current Weight Factors (CWF) of the I/O expansion cabinet modules becomes 16 or more. The CWF for each I/O expansion cabinet module is: <br><br>Module Type    CWF <br>Each IDCU    3 <br>Each CU    1 <br>Each SLCA    1 |
| I/O Power Expansion F3964-06 | Provides +5V power supply expansion for the T1982-05 I/O expansion cabinet. CWF calculation for F3964-05 applies and determines need for power supply expansion. |
| System Power Expansion F3964-02 | Provides +5 Vdc power supply expansion for T1982-00/03. |
| Input-Output Microprocessor (IOMP) F3367-01 | Dual microprogrammed multiplexer processor. It controls concurrent operations over two I/O buses for peripherals and SLCAs (single line communications adapter). SDMA F2795 is required for peripheral controllers, and MLCM F2796 for SLCAs. Requires either F2795 or F2796. |
| Multiple Line Communications Multiplexer (MLCM) F2796-01 | Provides the functionality to attach SLCA to F3367-01. The MLCM supports functions such as buffer pool management, data chaining, and command chaining. Requires first IOMP. |
| Multiple Line Communications Multiplexer F2796-02 | Same as F2796-01 except that it requires a second IOMP. |

(continued)

Table 1-3. I/O Cabinet and Expansion Cabinet Equipment (cont)

| Type/Feature | Description |
|---|---|
| **MODELS 10/15/20 ONLY** | |
| I/O Cabinet T1982-04 | Cabinet for low speed integrated controllers and communications. Includes a power supply, power control, and an electronics module. Requires 208/240 Vac, 3 phase, 60 Hz or 380/415 Vac, 3 phase, 50 Hz.<br><br>Requires:<br><br>■ IOP (F4869-00) with SDMA (F2795-01)<br>■ Diskette controller (F3427-01 with T8420 or T8422 diskette drive)<br>■ Paper peripheral controller (F2789-02) with line printer if line printer is not configured on SEL<br>■ IDCU (F3734-XX) with appropriate disk drives if T5039 or T8430/33 is not used<br><br>A +5V power supply feature, F3964-05, is required when the sum of the current weight factors (CWF) of the I/O cabinet modules becomes 16 or more. The CWF for each I/O cabinet module is:<br><br>Module Type    CWF<br><br>Each IOP      3<br>Each IDCU    3<br>Each CU      1<br>Each SLCA    1<br><br>Peripheral power sequencer F3784-XX may be added. |
| I/O Expansion Cabinet T1982-05 | Provides facility to expand the I/O and communications capabilities of the system beyond the I/O cabinet. The expansion includes power supply, and an electronics module. Requires and interfaces to a second IOP (F4869) in I/O cabinet T1982-04 except for IDCU expansion.<br><br>A +5V power supply feature, F3964-06, is required when the sum of the current weight factors (CWF) of the I/O expansion cabinet modules becomes 16 or more. The CWF for each I/O expansion cabinet module is:<br><br>Module Type    CWF<br><br>Each IDCU    3<br>Each CU      1<br>Each SLCA    1<br><br>Requires 208/240 Vac, 3 phase, 60 Hz or 380/415 Vac, 3 phase, 50 Hz. |
| I/O Cabinet T1982-00 | An I/O cabinet which is part of a System 80 model 8 system. Requires I/O conversion kit F5060-00 and IOP, F4869-00 installation prior to use with models 10/15/20. It is a cabinet for lower speed channels, controllers and expansion capability for I/O and communications. Includes power supply, power control and an electronics module. Requires 208/240/381/415 Vac, 3 phase, 50/60 Hz.<br><br>A +5V power supply feature F3964-02 is required when the current weight factor (CWF) of control units, SLCAs, IOPs and IDCUs exceeds 12. An IDCU has a CWF of 3. All other control units have a CWF of 1.<br><br>Peripheral power sequencer F3784-XX may be added. |

(continued)

Table 1-3. I/O Cabinet and Expansion Cabinet Equipment (cont)

| Type/Feature | Description |
|---|---|
| I/O Cabinet Conversion Kit F5060-00 | Converts a T1982-00 I/O functional equivalent cabinet to a T1982-04 I/O cabinet for use with models 10/20. Provides cables, jumpers, terminators, cable standoffs and necessary instructions to complete a conversion. Required to complete the conversion, but not included with the cabinet conversion kit, is an IOP, F4869-00.<br><br>Converting a T1982-00 I/O cabinet to a T1982-04 equivalent I/O cabinet may require the addition of the +5V power supply expansion feature, F3964-02, after the conversion is complete, although it is not required prior to conversion. If the sum of the current weight factors (CWF) of the converted I/O cabinet modules is 12 or more, F3964-02, is required.<br><br>Module Type    CWF<br><br>Each IOP      3<br>Each IDCU    3<br>Each CU      1<br>Each SLCA    1 |
| I/O Expansion Cabinet T1982-03 | Provides facilities to expand a T1982-04 or converted T1982-00 I/O cabinet. The I/O expansion cabinet includes the necessary power supply and electronics modules. Requires an interface to the second IOP, F4869-00, in the T1982-04 or converted T1982-00 I/O cabinet except for IDCU expansion. Requires 208/240/381/415 Vac, 3 phase, 50/60 Hz.<br><br>A +5V power supply feature, F3964-00, is required when the current weight factor (CWF) of control units, SLCAs and IDCUs exceeds 12. An IDCU has a CWF of 3 and all other control units a CWF of 1. |
| I/O Power Expansion F3964-02 | Provides +5V power supply expansion for a T1982-00 I/O cabinet converted to a T1982-04 I/O cabinet using conversion feature F5060-00. Current weight factor (CWF) calculation determines need for expansion feature as described for F5050-00. |
| I/O Power Expansion F3964-03 | Provides +5V power supply expansion for a T1982-03 I/O expansion cabinet when the current weight factor (CWF) sum becomes 12 or more. Sum the CWF for type and quantity of modules in the I/O expansion cabinet to determine the power supply expansion.<br><br>Module Type    CWF<br><br>Each IDCU    3<br>Each CU      1<br>Each SLCA    1 |
| I/O Power Expansion F3964-05 | Provides +5V power supply expansion for a new (unconverted) T1982-04 I/O cabinet.<br><br>Power supply expansion is required when the sum of current weight factor (CWF) is 16 or more. The total CWF is determined by adding the individual CWFs for each of the modules in the cabinet. The CWF for each module by type is:<br><br>Module Type    CWF<br><br>Each IOP      3<br>Each IDCU    3<br>Each CU      1<br>Each SLCA    1 |

(continued)

## Table 1-3. I/O Cabinet and Expansion Cabinet Equipment (cont)

| Type/Feature | Description |
|---|---|
| I/O Power Expansion F3964-06 | Provides +5V power supply expansion for the T1982-05 I/O expansion cabinet. CWF calculation for F3964-05 applies and determines need for power supply expansion. |
| Input/Output Processor (IOP) F4869-00 | Dual microprogrammed multiplexer processor. It controls concurrent operations over two I/O buses, one for peripherals and one for communications. Requires F2795, SDMA to support peripheral controllers; requires F2796, MLCM to support communications. |
| Multiple Line Communications Multiplexer (MLCM) F2796-03 | Provides the functionality to attach single line communications adapters (SLCAs) to F4869-00. The MLCM supports functions such as buffer pool management, data chaining, and command chaining. Requires first IOP. |
| Multiple Line Communications Multiplexer (MLCM) F2796-04 | Same as F2796-XX except that it requires a second IOP. |
| **MODELS 8/10/15/20** | |
| Shared Direct Memory Access (SDMA) F2795-01 | Provides the functionality to low-performance peripherals. Capability for up to 8 device controller drops and 1 I/O system expander. Enables attachment of any controller compatible with I/O bus. Specific controllers that can be attached include workstations, paper peripheral, remote printer interface, diskette, magnetic tape, ITCU and IDCU. Requires first IOP. |
| Shared Direct Memory Access F2795-02 | Same as F2795-01 except that it requires a second IOP. |
| Diskette Controller F3427-01 | Provides control and interface facilities for configuring 4 diskette drives T8420/8422 in an intermix of manual or autoload. It supports MFM and FM data formats. See configurator for diskette limitations. |
| Integrated Tape Control Unit F3774-00 | Provides an integrated controller for one to four K3782-00 tape drives and one F3851-00 UNISERVO 22 tape formatter with T0876-00/01 tape drives. Supports data rates of 160 kB/s in start/stop mode. |
| Integrated Disk Control Unit (IDCU) F3734-00 | A microprogrammed disk controller and disk adapter supports up to 8 disk devices, consisting of T8416 and T8418 disk drives. |
| IDCU F3734-01 | Same as F3734-00, except that it supports a maximum of 8 F2834 and/or T8419 disk drives and no T8416/8418 disk drives. |
| IDCU F3734-03 | Same as F3734-00, except that it supports a maximum of 8 T8470/8480 disk drives and no T8416/8418 disk drives. |
| T8470 IDCU Conversion Feature F5123-04 | Converts a F3734-02 T8470 IDCU to a F3734-03 T8470/8480 IDCU. |
| Workstation Controller F2791-04 | Provides control and interface facilities for configuring 8 local workstations T3560 or T3561, or T3612-02 in any intermix. Supports CSU capability in workstations. |

(continued)

## Table 1-3. I/O Cabinet and Expansion Cabinet Equipment (cont)

| Type/Feature | Description |
|---|---|
| Workstation Controller F2791-08 (Model 8 Only) | Same as F2791-04, except it applies to model 8 only. |
| Local WSC Conversion Feature F5123-00 | Converts F2791-00 local workstation controller to a F2791-04 workstation controller. |
| Local WSC Conversion Feature F5123-01 | Converts F2791-01 local workstation controller to a F2791-04 workstation controller. |
| Local WSC Conversion Feature F5122-00 | Converts F2791-08 local workstation controller to a F2791-04 workstation controller. |
| Paper Peripheral Controller F2789-02 | Provides control and interface facilities for configuring paper peripheral devices. Allows attachment of printer T0789, a second T0789 printer, or T0798 or T0776 printer, a T0719 card reader, or T0608 card punch/reader. Katakana print bands are excluded from all printers connected to F2789-02. |
| PPC Conversion Feature F5123-02 | Converts a F2789-00 paper peripheral controller to a F2789-02 paper peripheral controller. |
| I/O Subsystem Expander F2908-01 | Provides an interface for tape controller F2800-00/01 located within tape drive T0871-XX. Allows connection of tape drives within 50 feet (15.24 m) of the I/O subsystem expander. |
| I/O Subsystem Expander F2908-02 | Same as F2908-01, except used in T1982-03/05 I/O expansion cabinet. |
| Subsystem Expander Conversion Feature F5123-03 | Converts a F2908-00 I/O subsystem expander to a F2908-01/02 I/O subsystem expander. |
| Line Printer Interface, F2794-00 | Provides control and interface facilities for configuring remotely located printer T0789 or T0798 up to 5000 feet (1524 m) from remote printer interface F2494-00. |
| Peripheral Power Sequencer F3784-00 | Provides dc power sequencing for a maximum of 8 compatible freestanding controllers for System 80, model 8, dc powered peripheral control. |
| Single Line Communications Adapter (SLCA) Synchronous RS-232-C/MIL 188-100 F2788-02 | Provides a communications adapter that is microcoded to support CMM functionality. Provides the same level of support as the 90/30 communications adapter (BSC, NTR, REM-1, U100 and UTS400 protocols, etc.) and operates at 4800 bps full duplex or 9600 bps half duplex for synchronous communications. Requires external clock supplied by modem. Communications interface is compatible with RS-232-C and X.21 BIS. Provides auto answer capability. Provides cable length up to 50 feet (15.24 m) for connection to an external modem. Requires cable selection C3311-00/01 and C3401, C3402, and C3403. Requires F3794-00. |
| SLCA F2788-03 | Same as F2788-02, except has MIL 188-100 communications interface |
| SLCA F2788-04 | Same as F2788-02, except microcode directly supports NTR communications protocols at 9600 bps, full duplex. |

(continued)

## Table 1-3. I/O Cabinet and Expansion Cabinet Equipment (cont)

| Type/Feature | Description |
|---|---|
| SLCA F2788-05 | Same as F2788-04, except has MIL 188-100 communications interface |
| Cable Length C3311-00 | Cable selection for use with modem. Length is specified for 15 to 30 feet (4.57 to 9.14 m) in 5-foot (1.52 m) increments, and from 30 to 50 feet (9.14 to 15.24 m) in 10-foot (3.05 m) increments. Supports NTT modems. |
| Cable Length C3311-01 | Cable selection for use with direct-connect UNISCOPE®U100/200/400/etc. in lengths of 50 feet (15.24 m) only. Applies to F2788-02 only. |
| SLCA Selections for F2788/F2799: | |
| Data Terminal Ready (DTR) C3401-00 | DTR switched (normal selection) |
| DTR C3401-01 | DTR constant |
| Request to Send (RTS) C3402-00 | RTS switched (normal selection) |
| RTS C3402-01 | RTS constant |
| Line Sensitivity (LS) C3403-00 | Low sensitivity (normal selection) |
| LS C3403-01 | High sensitivity |
| Transmit Data (XMD) C3404-00 | Normal XMD (normal selection) |
| XMD C3404-01 | Inverted XMD |
| Clear To Send (CTS) C3405-00 | CTS independent of carrier (normal selection) |
| CTS C3405-01 | CTS dependent on carrier |
| Transmit Clock (XMD) C3406-00 | Standard XMD (normal selection) |
| XMD C3406-01 | Inverted XMD |
| Receive Clock (RC) C3407-00 | RC standard clock (normal selection) |
| RC C3407-01 | RC inverted clock |
| Modem Speed (MS) C3408-00 | MS high speed (normal selection) |
| MS C3408-01 | MS low speed |
| Receive Data (RS) C3409-00 | RS normal (normal selection) |
| RS C3409-01 | RS inverted |

(continued)

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## Table 1-3.  I/O Cabinet and Expansion Cabinet Equipment (cont)

| Type/Feature | Description |
|---|---|
| SLCA Selections for F2788/F2799 (cont): | Communications Line and Modem Rate:<br><br>C3410-00  2400 baud<br>C3410-01  4800 baud<br>C3410-02  9600 baud<br>C3410-03  3600 baud<br>C3410-04  7200 baud<br>C3411-00  50 bits/s<br>C3411-01  75 bits/s<br>C3411-02  110 bits/s<br>C3411-03  134.5 bits/s<br>C3411-04  150 bits/s<br>C3411-05  300 bits/s<br>C3411-06  600 bits/s<br>C3411-07  1200 bits/s<br>C3411-08  1800 bits/s<br>C3411-09  2400 bits/s<br>C3411-10  900 bits/s<br>C3411-11  3600 bits/s<br>C3411-12  4800 bits/s<br>C3411-13  7200 bits/s<br>C3411-14  9600 bits/s |
| SLCA – Low Speed Asynchronous RS-232-C, F2799-00 | Provides a communications adapter the microcode of which implements CMM functionality in support of DCT 500 and TTY protocols. Communications code is ASCII. Operates on a character basis and performs character parity checking. Operates in half-duplex mode at speeds up to 9600 bps with internal clock. Communications interface compatible with RS-232-C and X.21 BIS. Provides automatic answer capability. Automatic dial requires F3794-00. Requires cable selection C3311-00, with specified length. Requires selection of C3401, C3403, C3404, C3405, and C3408. |
| SLCA – Low Speed Asynchronous MIL 188A, F2799-01 | Same as F2799-00, except has MIL 188A communications interface. Requires selections C3401, C3402, C3404, C3405, C3409, and C3411. |
| SLCA – Medium Speed UDLC RS-232-C, and X.21 BIS, F2798-00 | Provides a communications adapter which supports standard UDLC protocols. Operates in synchronous half-duplex mode up to 19.2K bps or full-duplex mode at speeds up to 9600 bps. Requires external clock supplied by modem. Communications interface compatible with RS-232-C and X.21 BIS. Provides automatic answer capability. Requires cable selection C3311-00. Automatic dial requires F3794-00. Provides PDN support for Datapac. |
| SLCA – Medium Speed UDLC X.21 Transpac, F2798-02 | Same as F2798-00, except has X.21 communications interface, with standard 50 feet (15.24 m) of X.21 cable connection. |

(continued)

## Table 1-3. I/O Cabinet and Expansion Cabinet Equipment (cont)

| Type/Feature | Description |
|---|---|
| SLCA Selections for F2798: | |
| C3590-00 | Data terminal ready (DTR) switched (normal selection) |
| C3590-01 | DTR constant |
| C3591-00 | Request to send (RTS) switched (normal selection) |
| C3591-01 | RTS constant |
| C3592-00 | Line sensitivity (LS) low sensitivity (normal selection) |
| C3592-01 | LS high sensitivity |
| SLCA – Medium Speed UNISCOPE, RS-232-C, F2798-06 | Same as F2798-00, except it supports UNISCOPE protocols and requires patch selection C3822, C3823, and C3824. |
| SLCA Selection for F2798-06: | |
| C3822-00 | Data terminal ready (DTR) switched (normal selection) |
| C3822-01 | DTR constant |
| C3823-00 | Request to send (RTS) switched (normal selection) |
| C3823-01 | RTS constant |
| C3824-00 | Line sensitivity (LS) low sensitivity (normal selection) |
| C3824-01 | LS high sensitivity |
| SLCA – High Speed Synchronous UDLC, F2986-01 | Provides a communications adapter that supports UDLC protocols. Operates in synchronous half- or full-duplex modes at speeds of up to 56,000 bps. Has CCITT-V35 interface with standard 50-foot (15.24 m) V.35 interface cable connection. Requires C3825 and C3826. |
| SLCA – High Speed Synchronous NTR, CCITT-V35, F2986-05 | Same as F2986-01, except supports NTR protocols. |
| SLCA Selections for F2986-XX : | |
| C3825-00 | Data terminal ready (DTR) switched (normal selection) |
| C3825-01 | FYT constant |
| C3826-00 | RTS switched (normal selection) |
| C3826-01 | RTS constant |
| SLCA Auto Dial F3794-00 | Provides a communications adapter for three automatic delay interfaces meeting RS-366 interface requirements for both V series or circuit switched public data network. Includes standard 50-foot (15.24 m) RS-366 interface cable connection. |

## Table 1-4. Magnetic Disks

| Type/Feature | Description |
| --- | --- |
| Manual Diskette and Cabinet T8422-02 | Provides a cabinet with one manual diskette drive of one megabyte capacity. An additional 3 drives may be added to provide a total combination of I, 2, or 4 drives. Connects to and requires diskette controller F3427. Operates on 200/208/240 volts, 60 Hz power. |
| Manual Diskette and Cabinet T8422-03 | Same as T8422-02, except operates on 50 Hz power. |
| Manual Diskette F2785-04 | Provides a 1 MB capability manual diskette drive and requires manual diskette cabinet T8422-02. Operates on 60 Hz power. |
| Manual Diskette F2785-05 | Same as F2785-04, except operates on 50 Hz power. Requires T8422-03. |
| Manual Diskettes F2785-06 | Same as F2785-04, except provides 2 manual diskette drives with 1 MB capacity each. Requires F2785-04 as a prerequisite. |
| Manual Diskettes F2785-07 | Same as F2785-06, except operates on 50 Hz power. Requires F2785-05. |
| Autoload Diskette and Cabinet T8420-02 | Provides an autoload diskette and cabinet. Stores up to 20 diskettes in hopper and stacker. Connects to and requires diskette controller F3427. Operates on 208/240 volts, 60 Hz power. |
| Autoload Diskette T8420-03 | Same as T8420-02, except operates on 50 Hz power. |
| Manual Diskette Expansion for Autoload Diskette F2833-02 | Provides addition of a single drive attached to the autoload diskette T8420-02. Operates on 60 Hz power. |
| Manual Diskette Expansion F2833-03 | Same as F2833-02, except operates on 50 Hz power and is for T8420-03. |
| Disk Drive T8416-02 | Provides direct access storage using disk pack F1216-01. Average head positioning time is 30 ms. Average latency time is 10.7 ms. Transfer rate is 625 KB/s. Data capacitly is 36.8 MB (gross), 28.9 MB (net) of removable storage. More than 4 drives requires T2408-00/01 power supply. |
| Disk Drive T8416-03 | Same as T8416-02, except operates on 50 Hz power. |
| Disk Drive T8418-02 | Single disk drive providing 57.9 MB of direct access storage, using removable disk pack F1216-02. Used with appropriate IDCU. More than 4 drives requires T2408-00/01 power supply. |
| Disk Drive T8418-03 | Same as T8418-02, except operates with 50 Hz power. |
| Disk Drive T8418-04 | Same as T8418-02, except stores 28.9 MB. F2198-00 upgrades T8418-04 to T8418-02. |
| Disk Drive T8418-05 | Same as T8418-04, except operates with 50 Hz power. |
| Disk Pack F1216-01 | Removable disk pack provides 28.9 MB for T8416-02/03 disk drive. |
| Disk Pack F1216-02 | Removable disk pack for T8418-XX. Provides 28.9 MB for T8418-04/05 or 57.9 MB for the T8418-02/03. |
| Disk Power Supply Expansion T2408-00 | Provides power expansion for T8416/8418 when more than 4 drives are used. Operates on 60 Hz power. |

(continued)

## Table 1-4. Magnetic Disks (cont)

| Type/Feature | Description |
|---|---|
| Disk Power Supply Expansion T2408-01 | Same as T2408-00, except operates on 50 Hz power. |
| Disk Drive Cabinet T8417–00 | Disk drive cabinet for housing up to three fixed media disk drives F2834-XX. Additional cabinets can provide for disk expansion. Operates on 60 Hz power. |
| Disk Drive Cabinet T8417-01 | Same as T8417-00, except operates on 50 Hz power. |
| Disk drive F2834-00 | Fixed media disk drive. Requires disk drive cabinet T8417-XX and HDA F2787-XX. Operates on 60 Hz power. |
| Disk Drive F2834-01 | Same as F2834-00, except operates on 50 Hz power. |
| HDA F2787-01 | Factory installed head disk assembly, providing 118.2 MB fixed media storage for use with F2834-00/01 disk drives. |
| HDA F2787-03 | Same as F2787-01, except is only used for field replacement. |
| Disk Drive T8419-00 | Provides direct access storage using disk pack F3542-00. Operates on 60 Hz power. |
| Disk Drive T8419-01 | Same as T8419-00, except operates on 50 Hz power. |
| Disk Pack F3542-00 | Removable disk pack provides 72.3 MB for T8419-00/01 disk drives. |
| Disk Controller T5039-00 | Basic control for up to eight T8430/8433 disk drives. May be expanded for up to 16 disk drives via F2047-00. Requires one F2077-00 microprogram in ROM. |
| Disk Controller T5039-01 | Same as T5039-00, except operates on 50 Hz power. |
| Microprogram F2077-00 | Series 9000 microprogram. A set of ROM cards to allow use of T5039 control unit on all Series 9000 units. |
| Disk Drive T8430-XX | Provides a single disk drive using removable media F1230. Average arm positioning time is 27 ms. Transfer rate is 716 KB/s. |
| Disk Drive T8430-YY | Same as T8430-XX, except operates on 50 Hz power. |
| Disk Drive T8433-XX | Provides direct access storage using removable disk pack F1230-00. Average head positioning time is 27 ms. Average latency is 8.33 ms. Transfer rate is 806 KB/s. |
| Disk Drive T8433-YY | Same as T8433-XX, except operates on 50 Hz power. |
| Controller Expansion F2047-00 | Provides capability to attach up to 16 T8430/8433 disk drives to a T5039 controller. |
| Dual Channel F2046-00 | Provides dual channel capability for T5039 control unit. |
| Disk Pack F1223-00 | Removable disk pack for T8433. Provides 200 MB capacity. |
| Disk Pack F1230-00 | Removable disk pack for T8430/8433 disk drives. Provides up to 100 MB for T8430-00/01 and T8433-02/03. |
| Disk Drive Upgrade F2342-00 | Upgrades disk drive T8430-99 to T8433-00. |

(continued)

## Table 1-4. Magnetic Disks (cont)

| Type/Feature | Description |
|---|---|
| Disk Drive T8470-00 | Disk drive cabinet for housing nonremovable media disk storage with a movable head positioner assembly. Requires factory installed HDA without fixed heads, F2717-02. Requires disk power supply. T2413-00/01 required for each 8 drives configured. Operates on 60 Hz power. |
| Disk Drive T8470-01 | Same as T8470-00, except operates on 50 Hz power. |
| HDA F2717-02 | Factory installed head disk assembly, consisting of 9 disks, a movable head/arm assembly with 32 data heads and 1 servo head, for use with T8470-00/01 disk drive. Net capacity is 495 MB on 630 cylinders on 9 disks. Access time is 4 ms mimimum. Transfer rate is 2.1 MB per second at 3600 rpm. Operates on 60 Hz power. |
| Dual Access F2718-00 | Allows T8470 disk drive to interface with 2 IDCUs (integrated disk control units), F3734-03. |
| Disk Power Supply Expansion T2413-00 | Disk power supply for each 8 drives configured. Requires 60 Hz power. |
| Disk Power Supply Expansion T2413-01 | Same as T2413-00, except operates on 50 Hz power, used with T8470-01. |
| Disk Storage Unit T8480-00 | Disk storage unit with 4 nonremovable media disk drives. Each disk drive has a movable head positioner assembly. Requires 4 HDAs without fixed heads, F2717-02. Net capacity is 2732 MB on 2,520 cylinders on 36 disks. Access time is 4 ms minimum. Transfer rate is 2.1 MB/sec at 3600 rpm. Operates on 60 Hz power. |
| Disk Storage Unit T8480-01 | Same as T8480-00, except operates on 50 Hz power. |
| Dual Access F2718-02 | Allows T8480 disk storage unit to interface with 2 IDCUs, F3734-03. |
| Power Supply F2413-XX | Power supply for maximum of two T8480 disk storage units. Requires 60 Hz power. |
| Power Supply F2413-YY | Same as F2413-XX, except operates on 50 Hz power, used with T8480-01. |
| Disk Drive Subsystem T8494-99 | Disk cabinet containing one integrated disk control unit, two 8494 disk drives, and power control. Requires power cord selection, C4630-XX. |
| Power Cord C4630-XX | Provides power cord connecting disk subsystem to power receptacle. Each cord is 12 ft (3.66 m) long:<br><br>C4630-00 NEMA L630P connector with ground pin, 20 amps, 250 Vac maximum<br>C4630-01 MK 9033 BLU connector with ground pin, 35 amps, 250 Vac maximum<br>C4630-02 Power cord with no connector at one end |
| Disk Control Unit Expansion F4958-99 | Provides second disk control unit for T8494-99 disk subsystem. |
| Disk Drive F4959-00 | Provides an additional pair of disk drives for T8494-99 subsystem (each drive is 368 MB). Two disk drives are required for minimum system. System can be expanded by adding pairs of drives to a maximum of eight drives. |
| Channel Expansion F5111-00 | Provides additional channel between integrated controller and host systems. |
| F5152-99 | Provides dual access for first two disk drives. |
| F5152-98 | Provides dual access. One required for each pair of drive expansions (F4959). |
| F4960 | Provides remote power control interface for the subsystem. |

## Table 1-5. Magnetic Tapes

| Type/Feature | Description |
|---|---|
| Tape Controller for UNISERVO 12/16 Tape Drives T5017-00 | Controls up to sixteen 9-track phase encoded, 1600 bpi UNISERVO 12 or 16 tape drives. F0826 provides dual density. |
| Tape Controller T5017-01 | Same as T5017-00, except operates on 50 Hz power. |
| Dual Access F1319-00 | Used on T5017-XX to provide dual access and simultaneous read/read, read/write, write/read, and write/write operation when added to two or more UNISERVO 16 (T0862-04 thru T0862-07) tape drives. |
| Tape Controller for UNISERVO 12/16/20 Tape Drives T5034-00 | UNISERVO 20 control unit, operates on 60 Hz. Has an interface conforming to SU00039 and controls 1 to 16 of 9-track phase encoding (1600 bpi), UNISERVO 20s (T0864-00), UNISERVO 16s (T0862-04), UNISERVO 12s (T0861-00/01), or a mixture of any of these, with at least one UNISERVO 20 drive. Simultaneous read/read, write/read, read/write, or write/write can be accomplished in two or more UNISERVO 20s or 16s, each of which includes F1510-00 or F1319-01, respectively, by adding F1477-00. |
| Tape Controller T5034-01 | Same as T5034-00, except operates on 50 Hz power. |
| Dual Access F1510-00 | Provides for dual access and R/R, R/W, W/R, and W/W operation when added to two or more UNISERVO 20's. Requires two controls (T5034-XX plus F1477-XX). |
| Dual Access F1319-01 | Used with T5034-00/01 for dual access and simultaneous R/R, R/W, W/R, and W/W operation when added to two or more UNISERVO 16 (T0862-04 through -07 only) tape units. |
| Control Module F1477-00 | Provides a second control module with redundant power supply for R/R, R/W, W/R, W/W operation on UNISERVO 20s and 16s in each of which are included dual access device features F1510-00 and F1319-01, respectively. |
| Dual Density Control F0826-00 | Required in T5034 or T5017 to permit controlling dual density tape units (PE/9T NRZI). |
| Dual Channel F1478-00 | Enables a second channel to address the SU00039 interface control unit. |
| UNISERVO 20 Tape Drive T0864-00 | A 9-track phase-encoded tape unit. Transfer rate is 320 kbps at 1600 bpi. Reads forward and backward; writes forward. Requires F1510 for dual access support. |
| UNISERVO 16 Tape Drive T0862-04 | A 9-track phase-encoded tape unit. Transfer rate is 192 kbps at 1600 bpi. Reads forward and backward; writes forward. Requires F1319 for dual access. |
| UNISERVO 16 Tape Drive T0862-00 | A 9-track tape unit utilizing 1600 bpi at 200, 556, and 800 bpi. Reads forward only. Transfer rate is up to 192 KB/s. |
| UNISERVO 16 Tape Drive T0862-02 | A 7-track tape unit using NRZI format at 200, 556, and 800 bpi. Transfer rate is 96 KB/s. |
| UNISERVO 12 Tape Drive T0861-00 | A 9-track master tape unit with logic to service up to 3 T0861-01 slave drives. Uses 9-track 1600 bpi, phase format. Transfer rate is 68.3 KB/s. Reads forward and backward; writes forward. A maximum of 4 masters may be used per subsystem control. Operates on 60 Hz power. |

(continued)

## Table 1-5. Magnetic Tapes (cont)

| Type/Feature | Description |
|---|---|
| UNISERVO 12 Tape Drive T0861-02 | Same as T0861-00, except operates on 50 Hz power. |
| UNISERVO 12 Tape Drive T0861-01 | A 9-track slave drive. Uses 1600 bpi, phase encoded or 800 bpi NRZI. A maximum of 3 tape units per master. Operates on 60 Hz power. |
| UNISERVO 12 Tape Drive T0861-03 | Same as T0861-01, except operates on 50 Hz power. |
| Tape Controller F2800-04 | Provides control and interface facilities for configuring 8 UNISERVO 10 magnetic tape drives T0871-XX in a subsystem. Includes control to write or read from 7- or 9-track tape drives in NRZI or phase-encoded recording format. The controller is located in tape drive T0871-XX cabinet. Requires I/O subsystem expander F2908. Requires C3964-00 if BCD/EBCDIC translation is required. Operates on 100/120 Vac, 50/60 Hz power. |
| Tape Controller F2800-05 | Same as F2800-04, except operates on 200/240 Vac, 50/60 Hz power. |
| UNISERVO 10 Tape Drive with NRZI Format, T0871-02 | Seven track NRZI, half-inch magnetic tape drive. Speed is at 25 ips (63.5 cm) at a recording density of 800, 556, or 200 bpi. Automatic threading for standard reels and for easy-load cartridges. The tape drive connects to the system via F2800-XX controller. It requires F3133 in F2800 tape controller, and F2632-01 in the tape drive. Operates on 100/120 Vac or 208/240 Vac, 60 Hz. |
| UNISERVO 10 Tape Drive, T0871-08 | Same as T0871-02, except it operates on 100/120 Vac or 200/240 Vac, 50 Hz. |
| UNISERVO 10 Tape Drive with Phase Encoding, T0871-00 | Nine track, half-inch magnetic tape drive. Speed is 25 ips (63.5 cm) at a recording density of 1600 bpi phase encoded. Automatic threading for standard reels and for easy-load cartridges. The tape drive connects to the system via a F2800-XX controller. Operates on 100/120 Vac, or 208/240 Vac, 60 Hz. Requires F2632-00. |
| UNISERVO 10 Tape Drive, T0871-06 | Same as T0871-00, except operates on 100/120 Vac or 200/240 Vac, 50 Hz. |
| UNISERVO 10 Tape Drive with Dual Density, T0871-01 | Nine track half-inch magnetic tape drive. Speed is 25 ips (63.5) at a recording density of 1600 bpi phase-encoded mode, or 800 bpi in NRZI mode. Automatic tape threading for standard reels or for easy-load cartridges. The tape drive connects to the system via the F2800-XX controller. Operates on 100/120 Vac or 208/240 Vac, 60 Hz. Requires F2632-01. |
| UNISERVO 10 Tape Drive, T0871-07 | Same as T0871-01, except operates on 100/120 Vac or 200/240 Vac, 50 Hz. |
| Data Conversion C3964-00 | Provides read and write capability in 7-track NRZI mode at recording densities of 200, 556, and 800 bpi, odd or even parity. This selection includes data conversion and BCD/EBCDIC translator C3134-00. |
| Data Conversion C3964-01 | Same as C3964-00, except conversions are in IBM mode. |
| Seven Track Translate C3134-00 | Allows translation to or from BCD on tape for EBCDIC code used in the processor. Seven track NRZI F3133-00 or F3133-01 is a prerequisite. |
| Dual Density F3123-00 | Adds 9-track NRZI to a phase-encoded T0871 tape drive. |

(continued)

## Table 1-5. Magnetic Tapes (cont)

| Type/Feature | Description |
|---|---|
| Interface Conversion F2632-00 | Provides conversion of a 9-track phase-encoded SF02165 interface to a 9-track phase-encoded SH05630 interface. |
| Interface Conversion F2632-01 | Provides conversion of a 9-track phase-encoded or 7-track NRZI SF02165 interface to a 9-track phase-encoded or 7-track NRZI SH05630 interface. |
| Tape Controller T5045-04 | Provides control and housing for two phase-encoded UNISERVO 10 (T0870-00) tape drives; or when F0826-00 is added for 2 dual-density UNISERVO 10 (T0870-00) tape drives; and two 7-track UNISERVO 10 (T0870-02) tape drives. Up to 8 UNISERVO 10 tape drives can be supported, but not intermixed. Can utilize 9-track translator F2627-00/01/02 with selection C2628-XX and 7-track translator F0823-07/08/09. When F2043-00 is present, the controller becomes a UNISERVO 14 controller and cannot be intermixed with a UNISERVO 10 subsystem. Operates on 60 Hz power. |
| Tape Controller T5045-05 | Same as T5045-04, except operates on 50 Hz power and controls UNISERVO 10 (or UNISERVO 14) tape drives that operate on 50 Hz power. |
| UNISERVO 10 Tape Drive T0870-00 | A 9-track, phase-encoded tape drive. The transfer rate is at 40 kB/s at 25 ips with 1600 bpi. |
| UNISERVO 10 Tape Drive T0870-01 | Same as T0870-00, except it also operates at 9 tracks in NRZI mode at 800 bpi. Transfer rate is at 20 kB/s at 25 ips. |
| UNISERVO 10 Tape Drive T0870-02 | Same as T0870-00, except operates in 7 tracks in NRZI at 200, 556, and 800 bpi with transfer rates up to 20 kB/s at 25 ips. |
| UNISERVO 10 Tape Drive T0870-06 | Same as T0870-00, except operates on 50 Hz power. |
| UNISERVO 10 Tape Drive T0870-07 | Same as T0870-01, except operates on 50 Hz power. |
| UNISERVO 10 Tape Drive T0870-08 | Same as T0870-02, except operates at 50 Hz power. |
| UNISERVO 14 Tape Drive T0870-03 | 9-track PE, transfer rate 96 kB/s at 60 ips and 1600 bpi |
| UNISERVO 14 Tape Drive T0870-04 | Same as T0870-03, except also operates in 9-track NRZI mode at 800 bpi. Transfer rate is 48 kB/s at 60 ips. |
| UNISERVO 14 Tape Drive T0870-05 | Same as T0870-03, except operates in 7-track NRZI up to 800 bpi. Transfer rate up to 48 kB/s at 60 ips. |
| UNISERVO 14 Tape Drive T0870-09 | Same as T0870-03, except operates on 220/240 Vac, 50 Hz power. |
| UNISERVO 14 Tape Drive T0870-10 | Same as T0870-04, except operates on 220/240 Vac, 50 Hz power. |
| UNISERVO 14 Tape Drive T0870-11 | Same as T0870-05, except operates on 220/240 Vac, 50 Hz power. |

(continued)

## Table 1-5. Magnetic Tapes (cont)

| Type/Feature | Description |
|---|---|
| Tape Controller for UNISERVO 22/24/26/28 Tape Drives T5055-00 | Provides control and interface for configuring up to 8 T0876 or T0884 magnetic tape drives in any intermix. Basic control provides 9-track, 1600 bpi, phase-encoded, and 9-track, 6250 bpi, GCR mode. Requires 200/208/240 Vac, 60 Hz power. |
| Tape Controller T5055-01 | Same as T5055-00, except operates on 200/220/240 Vac, 50 Hz power. |
| Dual Channel Interface F3738-00 | Enables access of two I/O channels on an alternate basis. |
| Data Translation F3739-00 | Provides ASCII/EBCDIC data translation. |
| 9-Track NRZI F2451-00 | Provides 9-track 800 bpi NRZI operation. |
| 8-Channel MTU Interface F2452-00 | Enables access to MTU numbers 4 through 7. |
| Block Numbering F2453-00 | Provides block numbering mode. |
| Load Device F3927-00 | Provides diskette as load device and maintenance panel for offline maintenance. |
| Load Device F3927-01 | Same as F3927-00, except operates with T5055-01. |
| UNISERVO 22 Tape Drive T0876-00 | Magnetic tape drive capable of operating at 75 ips and provides ANSI compatible operation at 9-track, 1600 bpi or 800 bpi NRZI recording formats. Requires 200/240 Vac, 60 Hz power. |
| UNISERVO 22 Tape Drive T0876-01 | Same as T0876-00, except operates on 200/240 Vac, 50 Hz power. |
| UNISERVO 22 Formatter F3851-00 | Provides phase-encoded format. Installed in first T0876-00/01 tape cabinet. |
| Formatter F3853-00 | Provides 9-track, 800 bpi NRZI format for F3851-00. |
| UNISERVO 22 Interface F3116-00 | Required and installed in each T0876-00/01 tape drive configured to F3851-00. |
| Dual Access F3116-01 | Provides dual acess for UNISERVO 22/24 (T0876-XX) tape drives. |
| UNISERVO 24 Tape Drive T0876-02 | Same as T0876-00, except capable of operating at 125 ips. |
| UNISERVO 24 Tape Drive T0876-03 | Same as T0876-02, except operates on 200/240 Vac, 50 Hz power. |
| UNISERVO 26 Tape Drive T0884-00 | Magnetic tape drive capable of operating at 75 ips and providing ANSI compatible operation on 9 tracks with 1600 bpi and phase encoded/6250 GRC recording formats. Requires 200/240 Vac, 60 Hz power. |
| UNISERVO 26 Tape Drive T0884-01 | Same as T0884-00, except operates on 200/240 Vac, 50 Hz power. |

(continued)

## Table 1-5. Magnetic Tapes (cont)

| Type/Feature | Description |
|---|---|
| UNISERVO 28 Tape Drive T0884-02 | Same as T0884-00, except it is capable of operating at 125 ips. |
| UNISERVO 28 Tape Drive T0884-03 | Same as T0884-02, except operates on 200/240 Vac, 50 Hz power. |
| Dual Access F3737-00 | Provides dual access for UNISERVO 26/28 (T0884-XX) tape drives. |
| Tape Controller for UNISERVO 22/24 Tape Drive T5058-00 | Provides two dual density phase encoded/NRZI 9-track tape drives with control unit. Transfer rates of 120 kB/s and 60 kB/s at recording densities of 1600 or 800 bpi. Tape drives read in forward and backward directions and write in forward direction only. Automatic threading and wraparound cartridge is standard. Up to 8 UNISERVO 22 and/or UNISERVO 24 tape drives may be attached. Operates on 200/240 Vac, 60 Hz power. |
| Tape Controller T5058-01 | Same as T5058-00, except operates on 200/240 Vac, 50 Hz |
| Tape Controller T5058-02 | Provides two additional UNISERVO 22 tape drives which interface to controller in T5058-00. |
| Tape Controller T5058-03 | Same as T5058-02 except 50 Hz. Used with T5058-01. |
| Tape Controller T5058-04 | Provides one additional UNISERVO 22 tape drive which interfaces to controller in T5058-00. |
| Tape Controller T5058-05 | Same as T5058-04 except 50 Hz. Used with T5058-01. |
| Tape Controller T5058-06 | Provides basic control unit and two UNISERVO 24 dual density PE/NRZI 9 track tape drives. Operates at 125 ips with transfer rates of 200kB/s and 100kB/s at recording densities of 1600 bpi/PE and 800 bpi/NRZI. Tape drives read in forward and backward direction and write in forward direction only. Automatic threading and wraparound cartridge standard. Up to 8 T5058-08/09 tape drives may be attached. Operates on 208/240 Vac, 60 Hz. |
| Tape Controller T5058-07 | Same as T5058-06 except 50 Hz. |
| Tape Controller T5058-08 | Provides two additional UNISERVO 24 tape drives which interface to controller in T5058-06. |
| Tape Controller T5058-09 | Same as T5058-08 except 50 Hz. Used with T5058-07. |
| Tape Controller T5058-10 | Provides one additional UNISERVO 24 tape drive which interfaces to controller in T5058-06. |
| Tape Controller T5058-11 | Same as T5058-10 except 50 Hz. Used with T5058-07. |
| Dual Channel F0825-00 | Enables a second SU00039-01 I/O channel SU00039-02 compatible to address the control unit. |
| Dual Access F3820-00 | Adds a second interface to the magnetic tape unit providing dual access capability. |

(continued)

## Table 1-5. Magnetic Tapes (cont)

| Type/Feature | Description |
|---|---|
| 9 Track Translation F2627-00 | Provides the capability to translate data to and from 9-track tape units via one translator. May be expanded to a second translator by the addition of F2627-01. One translator code selection (C2628-XX) is required per F2627-XX feature.<br><br>C2628-00  *ASCII to EBCDIC translator<br>C2628-01  *FD to EBCDIC translator (64 character subset)<br>C2628-02  *FD to ASCII translator (64 character subset) |
| 9 Track Translation F2627-01 | Expands 9 track translation (F2627-00) which is a prerequisite to provide a second translation. One translation code selection (C2628-XX) is required. |
| Freestanding Tape Drive Cabinet T1978-00 | Tape drive for accepting up two K3782-XX tape drives. One additional cabinet may be added to accommodate tape expansion. Operates on 100/120 Vac, 50/60 Hz. |
| Tape Drive Cabinet T1978-01 | Same as T1974-00, except it operates on 208/220/240 Vac, 50/60 Hz. |
| Streaming Tape Drive K3782-00 | Provides magnetic tape drive for dual operation at 100 ips and 25 ips with 9-track, 1600 bpi PE recording. Requires freestanding tape cabinet T1978-00. |
| Streaming Tape Drive K3782-01 | Same as K3782-00, except used in T1978-01. |
| Tape Controller 3241-1 | 75 ips PE/GCR tape subsystem consisting of one controller and one 75 ips master drive. The controller interfaces to a high-speed I/O channel via an SU-212 interface. The subsystem can handle up to eight 75 ips drives maximum. Slave units 2 through 4 can be ordered singly (3244). Additional units 5-8 also require feature 6233, power distribution module. One customer selection kit, CB781 or CB782, must be made. Power requirements are 200/208/240 Vac, 60 Hz, 3 ph, or 220/380/415 Vac, 50 Hz, 3 ph. An order for this subsystem would consist of the following:<br><br>One 3241      Freestanding controller<br>Two CB78X    Cable selection kit |
| Tape Controller 3241-2 | Same as 3241-1 except the controller has a switchable 2-channel interface. Two customer selection kits, CB781 and/or CB782, are required. An order for this subsystem would consist of the following:<br><br>One 3241      Freestanding controller<br>One 6211      2-channel switch<br>Four CB78X   Cable selection kit |
| Tape Controller 3261-1 | 125 ips PE/GCR tape subsystem consisting of one controller and one 125 ips PE/GCR master drive. The controller interfaces to a high-speed I/O channel via an SU-212 interface. Up to seven additional slave drives comprised of any mix of 3266 or 3288 may be configured to this subsystem. Note that feature 6233 is required for configurations of more than four drives. One customer selection kit, CB781 or CB782, is required. Power requirements are identical to those listed for the 3241-1 above. An order for this subsystem would consist of the following:<br><br>One 3261      Freestanding controller<br>Two CB78X    Cable selection kit |

(continued)

## Table 1-5. Magnetic Tapes (cont)

| Type/Feature | Description |
|---|---|
| Tape Controller 3261-2 | Same as 3261-1 except the controller has a switchable 2-channel interface. Two customer selection kits of CB781 and/or CB782 are required. Power requirements are the same as those listed above for the 3241-1. An order for this subsystem would consist of the following:<br><br>One 3261      Freestanding controller<br>One 6211      2-channel switch<br>Four CB78X    Cable selection kit |
| Tape Controller 3281-1 | 200 ips tape subsystem consisting of one controller and a 200 ips PE/GCR master drive. The controller interfaces to a high-speed I/O channel via an SU-212 interface. Up to seven additional slave drives comprised of any mix of 3266 or 3288 may be configured to this subsystem. Note that feature 6233 is required for configurations of greater than four drives. One customer selection kit, CB781 or CB782, is required. Power requirements are identical to those listed for the 3241-1 above. An order for this subsystem would consist of the following:<br><br>One 3281      Freestanding controller<br>Two CB78X    Cable selection kit |
| Tape Controller 3281-2 | Same as 3281-1 except the controller has a switchable 2-channel interface. Two customer selection kits of CB781 and/or CB782 are required. An order for this subsystem would consist of the following:<br><br>One 3281      Freestanding controller<br>One 6211      2-channel switch<br>Four CB78X    Cable selection kit |
| 3244 Tape Drive | Tape Drive - 75 ips PE/GCR slave tape drive |
| 3266 Tape Drive | Tape Drive - 125 ips PE/GCR slave tape drive |
| 3288 Tape Drive | Tape Drive - 200 ips PE/GCR slave tape drive |
| Power Distribution Feature 6233 | Power distribution module required when expanding the number of drives connecting to a controller from 4 to 5. Required for 32X1, 32X2. |
| Cable/Connector Kit CB781 | Cable and connector kit, including two 50-foot I/O cables, bus, and tag terminators. |
| Cable/Connector Kit CB782 | Cable and connector kit, including two 100-foot I/O cables, bus, and tag terminators. |

## Table 1-6. Paper Peripherals

| Type/Feature | Description |
|---|---|
| Line Printer 800 LPM 0770-00 | Printer with built-in controller that interfaces to SU00039 I/O 8-bit compatible interface. Prints with a 48-character set at 800 lpm, using a type cartridge that can be changed by the operator. There are 132 print positions per line, expandable to 160 print positions via a factory installable feature. Vertical spacing is 6 or 8 lines per inch (lpi). Maximum forms advance rate is 50 inches per second (ips). A 48-character print cartridge from F1536-XX is ordered separately. Character sets from F1537-XX, which are greater than 48 characters, require F1534-00. |
| Line Printer T0770-01 | Same as T0770-00, except operates on 50 Hz power. |
| Line Printer T0770-02 | Same as T0770-00, except operates at 1400 lpm and 75 ips. |
| Line Printer T0770-03 | Same as T0770-02, except operates on 50 Hz power. |
| Line Printer T0770-04 | Same as T0770-02, except operates at 2000 lpm and 100 ips. |
| Line Printer T0770-05 | Same as T0770-04, except operates on 50 Hz power. |
| Print Cartridges F1536-XX | Provides a range of different product line 48-character cartridges (for use with T0770-00/05) as follows:<br><br>F1536-00  Business/commercial, 77L font<br>F1536-01  Scientific, 77L font<br>F1536-03  United Kingdom, OCR-B font<br>F1536-04  Denmark/Norway<br>F1536-05  Finland/Sweden OCR-B |
| Print Cartridges F1537-XX | Provides a range of type band cartridges with character sets other than 48 characters. Requires F1534-00. Selection (for use with T0770-00/05) is:<br><br>F1537-00  ASCII, 96 characters<br>F1537-01  Denmark/Norway, 64 characters<br>F1537-02  Finland/Sweden, 64 characters<br>F1537-03  Universal OCR-B (ISO), 128 characters<br>F1537-04  Universal OCR-H14, 128 characters<br>F1537-05  COBOL/FORTRAN, 192 characters, 77L font<br>F1537-06  International, 177 characters<br>F1537-07  Finland/Sweden, 96 characters<br>F1537-08  Katakana, 128 characters<br>F1537-09  Numeric, 24 characters, 77L font<br>F1537-10  Modified, OCR-B, 128 characters<br>F1537-11  Universal, OCR-A, 128 characters<br>F1537-12  Universal, OCR-B (ECMA-11), 128 characters<br>F1537-13  Same as F1537-03, except uses 77L font<br>F1537-14  Modified FORTRAN, 63 characters<br>F1537-15  ASCII, 63 characters<br>F1537-18  Numeric, OCR-B, Japan |
| Character Set Control F1534-00 | Expanded character set control to accommodate print cartridge F1537-XX. |

(continued)

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Line Printer 2000 LPM T0770-06 | Freestanding printer that contains microprocessor-based controller. Prints a 48-character set at 2000 lpm. Prints 136 character positions. Vertical spacing is 6 or 8 lpi. Prints bands can be selected with 64, 96, 128, 192, or 380 characters. Contains remote power sequencing, power stacker with rear door, vacuum cleaner system, and a line counter. Operates on 200/208/230/240 Vac, 50/60 Hz power. |
| Line Printer T0770-07 | Same as T0770-06, except operates on 380/400/415 Vac, 50/60 Hz power. |
| Print Cartridges F4836-XX | Provides a product line of 48-character cartridges for T0770-06/07 printers.<br><br>F4836-00  Business, font 407<br>F4836-01  Scientific, font 407 |
| Print Cartridges F4837-XX | Provides a product line of cartridges with character sets other than 48 characters for T0770-06/07 printers.<br><br>F4837-00  ASCII, OCR-B, 96 characters<br>F4837-02  Finland/Sweden, OCR-B, 64 characters<br>F4837-03  Universal, OCR-B, 128 characters<br>F4837-06  International, OCR-B, 177 characters<br>F4837-07  Finland/Sweden, OCR-B, 96 characters<br>F4837-11  Universal, fonts OCR-A and 407, 128 characters<br>F4837-12  Universal (ECMA), OCR-B 128 characters<br>F4837-14  Modified FORTRAN, font 407, 64 characters<br>F4837-15  Modified ASCII, font 407, 64 characters<br>F4837-19  American Library Assoc., 162 characters<br>F4837-21  Universal, fonts OCR-A and 407, 128 characters<br>F4837-22  ASCII, font 407, 64 characters<br>F4837-23  ASCII, OCR-B, 96 characters<br>F4837-24  Universal (ECMA-11 and ISO), OCR-B, 128 characters |
| Line Printer 2000 LPM 9246-25B | Freestanding buffered line printer capable of 2000 lpm with 48-character set band, connecting to the integrated selector channel; 136 print positions; forms advance rate is 50 ips; vertical spacing is 6 or 8 lines per inch. |
| Print Cartridges F4836-XX | Provides a product line of 48-character cartridges for the 9246-25B printer.<br><br>F4836-00  Business, font 407<br>F4836-01  Scientific, font 407 |
| Print Cartridges F4837-XX | Provides a product line of cartridges with character sets other than 48 characters for the 9246-25B printer.<br><br>F4837-00  ASCII, OCR-B, 96 characters<br>F4837-02  Finland/Sweden, OCR-B, 64 characters<br>F4837-03  Universal, OCR-B, 128 characters<br>F4837-06  International, OCR-B, 177 characters<br>F4837-07  Finland/Sweden, OCR-B, 96 characters<br>F4837-11  Universal, fonts OCR-A and 407, 128 characters<br>F4837-12  Universal (ECMA), OCR-B 128 characters<br>F4837-14  Modified FORTRAN, font 407, 64 characters<br>F4837-15  Modified ASCII, font 407, 64 characters<br>F4837-19  American Library Assoc., 162 characters<br>F4837-21  Universal, fonts OCR-A and 407, 128 characters<br>F4837-22  ASCII, font 407, 64 characters<br>F4837-23  ASCII, OCR-B, 96 characters<br>F4837-24  Universal (ECMA-11 and ISO), OCR-B, 128 characters |

(continued)

### Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Line Printer 760/900/1200 LPM T0776-00 | Prints 48 characters at 760 lpm using an operator changeable type cartridge ordered separately. Prints 136 print positions at 6 or 8 lpi. Forms advance at the rate of 22 ips (maximum). Features available are:<br><br>F2215-XX  Character sets larger than 63 characters<br><br>F2216-00  Character sets having 48/63 characters<br><br>F2217-00  Speed upgrade<br><br>F2245-00  Expanded character set control |
| Line Printer T0776-01 | Same as T0776-00, except operates on 50 Hz power. |
| Line Printer T0776-02 | Same as T0776-00, except operates at 900 lpm. |
| Line Printer T0776-03 | Same as T0776-02, except operates on 50 Hz power. |
| Line Printer T0776-04 | Same as T0776-00, except forms advance at the rate of 50 ips, and prints at the rate of 1200 lpm. Print cartridge is F2216-XX. |
| Line Printer T0776-05 | Same as T0776-04, except operates on 200/220/240 Vac, 50 Hz power. |
| Character Sets F2215-XX | Character sets for T0776-00/05 printer (F2245-00 is a prerequisite) are as follows:<br><br>F2215-05  COBOL/FORTRAN/Business<br>F2215-06  ISO R646<br>F2215-07  Finland/Sweden<br>F2215-11  ANSI-X3, OCR-A<br>F2215-12  OCR-B<br>F2215-13  Unisys 77L<br>F2215-18  Japan, modified OCR-B<br>F2215-20  ASCII<br>F2215-21  OCR-B, ISO<br>F2215-23  OCR-A, full set |
| Character Sets F2216-XX | Character sets for T0776-00/05 printer (F2245-00 is a prerequisite) are as follows:<br><br>F2216-00  48-character set, business/commercial set<br>F2216-01  48-character alphanumeric scientific set<br>F2216-02  48-character alphanumeric, United Kingdom<br>F2216-03  48-character alphanumeric, Denmark/Norway<br>F2216-04  48-character alphanumeric, Finland/Sweden<br>F2216-05  63-character alphanumeric, Denmark/Norway<br>F2216-06  63-character alphanumeric, Finland/Sweden<br>F2216-07  24-character numeric and special symbol set<br>F2216-08  63-character alphanumeric set per 77L, equivalent to T0768 printer selection C1344-03<br>F2216-09  63-character alphanumeric set per 77L, equivalent to T0768 printer selection C1344-01<br>F2216-10  48-character OCR, ANSI requirements<br>F2216-11  64-character ASCII |
| Speed Upgrade F2217-00 | Speed upgrade for T0776-00/05 printer from 760 to 900 lpm. |
| Cartridge Expansion Capability F2245-00 | Provides control to accommodate print cartridges greater than 63 characters used on T0776-00/05 printer. |

(continued)

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Line Printer, 1200 LPM T0776-06 | Provides 1200 lpm for 48 characters with 120 print positions. Prints original and 5 copies at 6 or 8 lpi, which is operator selectable. Can accommodate up to three print band cartridges which are identified by a feature. Attachment to system requires paper peripheral controller F2789. Operates on 100 to 240 Vac, 60 Hz. Requires one print band feature F2346-XX/F2347-XX. |
| Line Printer, T0776-07 | Same as T0776-06, except operates on 50 Hz. |
| Print Band Selection for T0776-06/07 Printer F2346-XX | Character set containing 48 characters for T0776-06/07 printer is as follows:<br><br>F2346-00   Business, 48 characters<br>F2346-01   Scientific, 48 characters<br>F2346-03   United Kingdom, 48 characters<br>F2346-04   Denmark/Norway, 48 characters<br>F2346-05   Finland/Sweden, 48 characters |
| Print Band Selection for T0776-06/07 Printer F2347-XX | Character sets containing more than 48 characters for the T0776-06/07 printer are as follows:<br><br>F2347-01   Denmark/Norway, 64 characters<br>F2347-02   Finland/Sweden, 64 characters<br>F2347-14   Modified FORTRAN 77L, 64 characters<br>F2347-15   Modified ASCII 77L, 64 characters<br>F2347-00   ASCII, 96 characters<br>F2347-07   Finland/Sweden, 96 characters<br>F2347-03   Universal OCR-B (ISO), 128 characters<br>F2347-04   Universal OCR H-14, 128 characters<br>F2347-11   Universal OCR-A, 128 characters<br>F2347-12   Universal OCR-B (ECMA-II), 128 characters<br>F2347-13   Universal 77L, 128 characters<br>F2347-05   COBOL-FORTRAN business, 192 characters<br>F2347-06   International, 348 characters scientific/FORTRAN, 52 characters |
| Print Column Expansion for T0776-XX, F2910-00 | Provides printer column expansion for T0776-XX for expanding up to 136 print positions. |
| Line Printer, 180 LPM T0789-00 | Provides a 180 lpm line printer with 48 characters. Basic printer has 132 print positions. Prints original and five copies at 6 or 8 lpi, which is operator selectable. An acoustic enclosure is provided. Has a print band that can be replaced by the operator. Allows use of three print band types for character selection according to an associated PROM. Attachment to system requires paper peripheral controller F2789 or remote printer interface F2794-00. Contains provisions for attachment of up to 5000 feet (1524 m) of cable by F2794-00. Requires remote printer attachment T1955-XX. Operates on 100/120 Vac, 60 Hz. Requires one print band feature F2865-XX and interface F3572-00. Models 10/20 also require F4107-00. |
| Line Printer T0789-01 | Same as T0789-00, except operates on 100 Vac, 50 Hz. |
| Line Printer T0789-02 | Same as T0789-00, except operates on 220/240 Vac, 50 Hz. |
| Line Printer, 300 LPM T0789-03 | Same as T0789-00, except operates at 300 lpm and requires F3572-01. |

(continued)

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Line Printer T0789-04 | Same as T0789-01, except operates at 300 lpm and requires F3572-01. |
| Line Printer T0789-05 | Same as T0789-02, except operates at 300 lpm and requires F3572-01. |
| Line Printer, 640 LPM, T0789-06 | Provides a 640 lpm printer at 48 characters with 132 print positions. Prints original and five copies at 6 or 8 lpi, which is operator selectable. An acoustic enclosure is provided. Uses removable print bands and can accommodate up to three print band types that are associated with their own PROMs. Attachment to the system requires the paper peripheral controller F2789-02 or remote printer interface F2794, as well as the remote attachment T1955-XX. Operates on 100/120 Vac, 60 Hz. Requires one print band feature F3321-XX, and interface F3572-00. Models 10/20 also require F4107-00. |
| Line Printer T0789-07 | Same as T0789-06, except it operates on 100 Vac, 50 Hz. |
| Line Printer T0789-08 | Same as T0789-06, except it operates on 220/240 Vac, 50 Hz. |
| Print Rate Upgrade for T0789-00/01/02 F2970-00 | Provides a field upgrade of T0789-00/01/02 printers containing F3572-00 to 300 lpm printers. |
| Print Rate Upgrade F2970-01 | Same as F2970-00, except it is used in printer containing F3573-00. |
| Print Band Selection for 0789 Printer | Enables selection of standard print bands as follows: |

| 0789-00/05 | 0789-06/07/08 | Print Band Name |
|---|---|---|
| F2865-01 | F3321-01 | Business, 48 characters |
| F2865-06 | F3321-06 | Scientific, 48 characters |
| F2865-09 | F3321-09 | United Kingdom, 48 characters |
| F2865-10 | F3321-10 | Denmark/Norway, 48 characters |
| F2865-02 | F3321-02 | Finland/Sweden, 48 characters |
| F2865-11 | F3321-11 | Denmark/Norway, 64 characters |
| F2865-03 | F3321-03 | Finland/Sweden, 64 characters |
| F2865-04 | F3321-04 | Modified FORTRAN 77L, 64 characters |
| F2865-00 | F3321-00 | Modified ASCII 77L, 64 characters |
| F2865-05 | F3321-05 | ASCII, 96 characters |
| F2865-12 | F3321-12 | Finland/Sweden, 96 characters |
| F2865-07 | F3321-07 | Universal OCR-B (ISO), 128 characters |
| F2865-13 | F3321-13 | Universal OCR H-14, 128 characters |
| F2865-15 | F3321-15 | Universal OCR-A, 128 characters |
| F2865-08 | F3321-08 | Universal OCR-B (ECMA-II), 128 characters |
| F2865-17 | F3321-17 | Universal 77L, 128 characters |
| F2865-18 | F3321-18 | COBOL-FORTRAN business, 192 characters |

(continued)

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Print Bands F3607-XX | Replacement print band for F2865-XX. |
| Print Bands F3608-XX | Replacement print band for F3321-XX. |
| Panel Connector for T0789-XX Printer F4107-00 (Models 10/20 only) | Contains interface electronics providing panel connector for T0789-XX printer. Contains 6.5 feet of power cord for 60 Hz requirement. |
| Line Printer Interface for T0789-XX, F3572-00 | Provides an interface to connect T0789-00 through -02 printers to the paper peripheral controller F2789 or remote printer attachment T1955. |
| Interface F3572-01 | Same as F3572-00, except used on printers T0789-03 through T0789-05. |
| Interface F3572-02 | Same as F3572-00, except used on printers T0789-06 through T0789-08. |
| Interface F3573-00 | Provides an interface to connect T0789-XX to T3561 workstation via the 8-bit peripheral interface. |
| Interface F3573-01 | Same as F3573-00, except used on printers T0789-03 through T0789-05. |
| Interface F3573-02 | Same as F3573-00, except used on printers T0789-06 through T0789-08. |
| Character Printer at 75 LPM, T0798-00 | Operates at 200 characters per second, 7 x 7 half-space matrix, 132 columns, 6 lines per inch, 10 characters per inch, bidirectional, microprocessor based printer with character set selection and print stand. Attachment to system requires paper peripheral controller F2789 or remote printer interface F2794, as well as remote printer attachment T1955. Printer usage is restricted to not exceed one hour of continuous operation and no more than two hours per eight-hour shift, based on 25 percent duty cycle at 50 percent column density. Operates on 100/120 Vac, 60 Hz single phase power. A line printer is a prerequisite at the host processor site. |
| Character Printer T0798-01 | Same as T0798-00, except operates on 100 Vac, 50 Hz power. |
| Character Printer T0798-02 | Same as T0798-00, except operates on 220/240 Vac, 50 Hz power. |
| 6/8 Lines per Inch F3582-00 | Provides operator control that permits the option of printing either 6 or 8 lines per vertical inch. Without this feature, the printer operates at only 6 lpi. Cannot co-exist with F3584 or F3583. It is installed at the factory only. |
| Nine Wire Printhead F3583-00 | Provides a 9-wire printhead for printing lowercase U.S. ASCII characters with descenders on g, p, j, p, y and —. Requires selection of character set C3588-13. Installed at the factory only. |
| Dual Form Feed F3584-00 | Permits two separate form sets to be loaded simultaneously with independent control. Forms are positioned side by side and are limited in overall usable width. Cannot co-exist with F3582. Installed at the factory only. Requires usage of an 8-bit interface and custom user software control. |
| Document Parting Bar F2648-00 | Permits simple removal of newly printed pages without removing paper from tractors (requires special forms design). |

(continued)

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Compressed Print F3587-00 | Compresses character width to allow printing of 14 characters per inch. This permits printing of 132 columns on 11-inch wide paper. Control is provided allowing operator to switch from 10 to 14 characters per inch. Operates on 60 Hz only. Compressed printing is accomplished at 200 characters per second, but normal printing (10 cpi) rate is reduced to approximately 140 characters per second when this feature is installed. Installed at the factory only. |
| Compressed Print F3587-01 | Same as F3587-00, except operates on 50 Hz power. |
| Paper Peripheral Controller Interface F3581-00 | Provides the necessary signal interfacing to connect the 0798 printer to a paper peripheral controller F2789 or on remote printer interface F2794. Up to 50 feet (15.24 m) of cable is included as requested. When attached to either the paper peripheral controller or remote printer attachment, its usage is restricted to a secondary printer; i.e., a line printer must always be present. |
| 8-Bit UTS 400/UTS 4000 Interface, F3581-03 | Provides the necessary signal interfacing to connect the T0798 printer to an 8-bit UTS 400 terminal, or T3560 workstation. Includes a 10-foot (3.05 m) interconnection cable. Maximum cable length is 200 feet (60.96 m). |
| RS-232 Interface F3581-05 | Provides an RS-232 serial interface to connect printer T0798 to workstation T3560-XX. Printer to be used as a screen copy printer only. |
| Character Selection for T0798-XX Printer C3588-XX | Selections are as follows:<br><br>C3588-00  U.S. ASCII 64 characters<br>C3588-01  U.S. ASCII 96 characters<br>C3588-02  United Kingdom<br>C3588-03  France<br>C3588-04  Germany<br>C3588-05  Italy<br>C3588-06  Sweden/Finland<br>C3588-07  Denmark/Norway<br>C3588-08  Spain<br>C3588-09  Netherlands<br>C3588-10  Germany<br>C3588-11  Spain<br>C3588-13  U.S. ASCII 96 characters with descenders |
| Remote Printer Attachment for T0789 and T0798 Printers, T1955-00 | Provides an interface for remote attachment of a T0789 and T0798 printers; located next to printer. Requires use of remote printer interface F2794-00, and selection from C3660-XX. |
| Remote Printer Attachment, T1955-01 | Same as T1955-00, except operates on 50 Hz. |
| PROM Selection C3600-XX | Provides selection of translator PROM for character support in the remote printer attachment (T1955). |
| Latin Selection C3360-00 | Supports Latin (Western) character set. |
| Character Printer 80 CPS, T0797-00 | Workstation printer, 80-column, 10 characters per inch printer, operates at 80 characters per second, with 9 x 7 half-space dot matrix, friction-fed platen, 6 or 8 lines per inch vertical form spacing, electronic vertical forms control, unidirectional printing. Operates on 100/120 Vac, 50/60 Hz, single phase power. A character set selection (C3566-XX) and interface feature (F3565-XX) are required. |

(continued)

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Character Printer T0797-01 | Same as T0797-00, except operates on 220/240 Vac, 50 Hz single phase. |
| RS-232 Interface F3565-00 | Bit-serial interface with asynchronous data transmission. Complies with CCITTV.24, operating at bit rates from 300 to 9600 baud. Odd/even/no parity check selectable. Cable lengths up to 50 feet (15.24 m) maximum, can be accommodated. |
| 8-Bit UTS 400/UTS 4000 Interface, F3565-02 | An 8-bit plus even parity interface with request/acknowledge and interrupt control. Cable lengths of up to 200 feet (60.96 m) can be accommodated. Provides interface to connect T0797 printer to workstation T3561-XX. |
| Form Feed Tractor for T0797-00/01, F3563-00 | Accommodates sprocketed continuous forms ranging from 3.0 inches (7.62 cm) to 10 inches (25.4 cm) in overall width (edge to edge). |
| Pin Feed Platen for T0797-00/01 F3564-00 | Accommodates sprocketed continuous forms with an overall width of 9.5 inches (24.13 cm). Recommended for special applications where a form must be immediately removed after printing with minimum form wastage. Dimension between centerlines of paper sprocket holes is 9.0 inches (22.86 cm). Not recommended for use with F3563-00. Not customer installable. |
| Character Set Selections for T0797-XX Printer, C3566-XX | Selection can be made from 12 character sets. Only one set can be resident in the printer at one time. Character sets are implemented as removable PROMs and are not customer installable. Selection is as follows:<br><br>C3566-00  ASCII<br>C3566-01  United Kingdom<br>C3566-02  France<br>C3566-03  Germany<br>C3566-04  Italy<br>C3566-05  Sweden/Finland<br>C3566-06  Norway/Denmark<br>C3566-07  Spain<br>C3566-08  Netherlands<br>C3566-09  Germany, modified<br>C3566-10  Spain, modified |
| Character Printer 9246-14B | Freestanding buffered line printer capable of 1500 lpm with 48-character set band, connecting to the integrated selector channel; 136 print positions; forms advance rate is 25 ips. |

<div align="right">(continued)</div>

Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Character Selection for 9246-14B printer F5236-XX or F5235-XX | Selections are as follows:<br><br>F5236-00   48 Char. Business/Commercial (ref F2216-00)<br>F5236-01   48 Char. Alphanumeric/Scientific set<br>F5236-02   48 Char. Alphanumeric set - U.K.<br>F5236-03   48 Char. Alphanumeric set - Denmark/Norway<br>F5236-04   48 Char. Alphanumeric set - Finland/Sweden<br>F5236-05   63 Char. Alphanumeric set - Denmark/Norway<br>F5236-06   63 Char. Alphanumeric set - Finland/Sweden<br>F5236-08   63 Char. Alphanumeric set - 77L (Mod. ASCII)<br>F5236-09   63 Char. Alphanumeric set - 77L (Mod. Fortran)<br>F5236-10   48 Char. Business, Std. OCR, ANSI<br>F5236-11   64 Char. Alphanumeric set, ASCII<br>F5236-12   64 Char. Alphanumeric set - 77L (ASCII - Libra)<br>F5235-00   96 Char. ASCII - ECMA-II<br>F5235-03   128 Char. - Universal OCR-B, ECMA II - ISO<br>F5235-06   384 Char. - ISO R646<br>F5235-07   96 Char. - ECMA - Sweden/Finland<br>F5235-11   128 Char. Universal - 77L/OCR-A<br>F5235-12   128 Char. Universal - ECMA II/OCR-B<br>F5235-13   128 Char. Universal - 77L<br>F5235-20   192 Char. - ECMA II - ASCII<br>F5235-21   127 Char. - ECMA OCR-B, ISO<br>F5235-23   384 Char. - International 177 - ECMA II |
| Reader Conversion F1529-00 | Permits field upgrading of T0716-00 feed rate from 600 cpm to 1000 cpm. |
| Reader Conversion F1529-01 | Same as F1529-00, except upgrades 0716-01 from 600 cpm to 1000 cpm. |
| Reader Conversion F1530-00 | Adds a second translator to translate mode, under program control. Translator selective according to C1485-XX. |
| Reader Translator C1485-XX | Provides an EBCDIC translator for 0716-XX card reader or a second translator for the same card reader if F1530-00 is present, as follows:<br><br>C1485-00   EBCDIC<br><br>C1485-01   ASCII<br><br>C1485-02   Compressed code<br><br>C1485-03   Field code |
| Reader Conversion F1896-00 | Detects end of field (EOF) condition when an empty hopper occurs with EOF button set on T0716 card reader. Used only with 360/1400 emulation. |
| Card Reader, 80 Column 300 CPM, T0719-04 | Provides a tabletop card reader that can read 80 column cards at 300 cpm. Input hopper and output stacker can hold up to 1000 cards each. Attachment to system requires paper peripheral controller F2789. Operates on 120 Vac, 60 Hz. |
| Card Reader, T0719-05 | Same as T0719-04, except operates on 100 Vac, 50 Hz. |
| Card Reader, T0719-06 | Same as T0719-04, except operates at 600 cpm on 120 Vac, 60 Hz. |
| Card Reader, T0719-07 | Same as T0719-04, except operates at 600 cpm on 100 Vac, 50 Hz. |

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Card Reader, T0719-14 | Same as T0719-04, except operates on 220 to 240 Vac, 50 Hz. |
| Card Reader, T0719-15 | Same as T0719-04, except operates at 600 cpm on 220/240 Vac, 50 Hz. |
| Card Reader, T0719-18 | Same as T0719-04, except operates on 100 Vac, 60 Hz. |
| Card Reader, T0719-19 | Same as T0719-04, except operates at 600 cpm on 100 Vac, 60 Hz. |
| 51 or 66 Column Cards, F2324-00 | Permits reading 51- or 66-column cards on T0719-XX. |
| Card Punch, 80 Column 75/160 CPM, T0608-03 | Provides a card punch that can punch 80 column cards from fully punched cards at 75 cpm, to partially punched cards at 160 cpm. Input hopper and primary output stacker hold 700 cards each. Secondary output stacker holds 100 cards. Attachment to system requires paper peripheral controller F2789. Can accommodate reader F2830-00. Operates on 100 to 120 Vac, 60 Hz. |
| Card Punch, T0608-04 | Same as T0608-03, except operates on 100 Vac, 50 Hz. |
| Card Punch, T0608-05 | Same as T0608-03, except operates on 220 to 240 Vac, 50 Hz. |
| Reader for T0608, F2830-00 | Provides card reader capability for card punch T0608-03/04/05. |
| Card Reader, 80 Column T0716-00 | Eighty-column, 600 cpm card reader with a SU00039 interface. Includes transmission or image mode reading under program control. Requires translator C1458-XX. Multiread checking is standard. Input hopper holds 2400 cards. Two output stackers hold 2000 cards. |
| Card Reader, T0716-01 | Same as T0716-00, except it operates on 50 Hz power. |
| Card Reader, T0716-02 | Same as T0716-00, except it operates at the rate of 1000 cpm. |
| Card Reader, T0716-03 | Same as T0716-00, except it operates on 50 Hz power with 1000 cpm. |
| Card Reader, T0716-04 | Same as T0716-00, except it also reads 96-column cards. |
| Card Reader, T0716-05 | Same as T0716-01, except it also reads 96-column cards. |
| Card Reader, T0716-06 | Same as T0716-02, except it also reads 96-column cards. |
| Card Reader, T0716-07 | Same as T0716-03, except it also reads 96-column cards. |

(continued)

## Table 1-6. Paper Peripherals (cont)

| Type/Feature | Description |
|---|---|
| Reader Conversion<br>F1486-XX | Permits field conversion of translation mode from one code to another for T0716-XX card reader, as follows:<br><br>F1486-00   EBCDIC to ASCII<br>F1486-01   Compressed code to ASCII<br>F1486-02   ASCII to EBCDIC<br>F1486-03   Compressed code to EBCDIC<br>F1486-04   ASCII to compressed code<br>F1486-05   EBCDIC to compressed code<br>F1486-06   Permits conversion to field data in place of ASCII, EBCDIC, or compressed code. |
| Reader Conversion<br>F1487-00 | Permits reading 51-column cards for T0716. |
| Reader Conversion<br>F1487-01 | Permits reading 66-column cards for T0716. |
| Reader Conversion<br>F1488-00 | Detects presence of multipunches in rows 1 through 7 when reading a translate mode for T0716. |
| Reader Conversion<br>F1498-00 | Permits the alternate filling of stackers 1 and 2 when operating in stop-on-errors mode. |

## Table 1-7. Workstations and Terminals

| Type/Feature | Description |
|---|---|
| SVT 1120 Terminal<br>T3612-00 | The SVT 1120 editing terminal is UNISCOPE control code compatible and functions similarly to the UTS 20, but provides significant enhancements.<br><br>Connects to system F2788-02/03 SLCA.<br><br>The monitor is a 14-inch CRT with P31 green phosphor. Operator can select a format of 80 or 132 columns by 25 lines. The 25th line is used for status information. Characters are formed using a 7 x 9 dot matrix with 2 dot descenders in 80-column mode and 5 x 7 dot matrix with 2 dot descenders in 132-column mode. The display features a CRT saver for time delay display shut-off and a display intensity control.<br><br>Selectable keyboards supported include: English, United Kingdom, French, German, Italian, Spanish, Danish/Norwegian, and Swedish/Finnish.<br><br>Two menu-driven set-up control pages are provided. One establishes operator-parameters and the other establishes communications configuration parameters. The operator can select control page prompts in Dutch, English, French, Germany, Italian, or Spanish.<br><br>A UTS 20 style control page is provided but is accessible only to the host. A keylock is provided to enable and disable input from the keyboard.<br><br>Synchronous, full-duplex EIA RS-232-C, CCITT V.24 and communications multiplexer interfaces are supported up to 19.2K bps.<br><br>The auxiliary device interface is an asynchronous, full-duplex RS-232 interface that operates at selectable speeds of 2400, 4800, or 9600 bits per second. Printer models 15, 21, 25 and 115 can operate on the auxiliary device interface.<br><br>A universal 99-264 Vac, 50 or 60 Hz power supply is provided.<br><br>Requires power cord selection (C3381-XX), communications interface selection (F8201-XX, or F8202-XX, or F8217-XX, or F8218-XX), and keyboard selection (F4725-XX). An optional printer requires printer cable selection (F8290-XX or F8291-XX). |
| SVT 1120 Power Cord<br>C3381-XX | Provides a detachable power cord for the SVT 1120.<br><br>C3381-00  NEMA 5-15P        C3381-03  BS 1363:1977<br>C3381-01  SEV 1011          C3381-04  Cord without power plug<br>C3381-02  IEC 83/C5         C3381-05  No cord set |
| SVT 1120 Keyboard<br>F2725-XX | Provides a 94-key, low-profile keyboard for the SVT 1120. The keyboard is available with eight different keycap legends.<br><br>F2725-25  United States     F2725-30  Denmark/Norway<br>F2725-26  United Kingdom    F2725-31  Sweden/Finland<br>F2725-27  Germany           F2725-32  Italy<br>F2725-28  France |
| SVT 1120 RS232 Modem Cable (PVC) F8201-XX | Cable used to connect the SVT 1120 to an RS-232 modem. A 20-conductor cable with a 25-pin connector on the DCE end and a 25-socket connector on the DTE end. Both connectors have English screws and the cable has a PVC cover.<br><br>F8201-00  1.0M   3ft    F8201-02  8.0M   26ft<br>F8201-01  3.0M   10ft   F8201-03  16.0M  52ft |

## Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| SVT 1120 Modem Cable (Plenum) F8202-XX | Same as F8201-01 through -03 except cable has a covering that provides fire resistance and low smoke-producing characteristics. |
| SVT 1120 Terminal Multiplexer Cable (PVC) F8217-XX | Cable used to connect the SVT 1120 to a terminal multiplexer. Provides a 20-conductor cable with a 25-pin connector on one end and a 25-socket connector on the other end. The cable has a PVC cover.<br><br>F8217-00  3.0M  10ft   F8217-04  30.5M  100ft<br>F8217-01  7.6M  25ft   F8217-05  45.7M  150ft<br>F8217-02  15.2M  50ft   F8217-06  61.0M  200ft<br>F8217-03  22.9M  75ft   F8217-07  91.4M  300ft |
| SVT 1120 Terminal Multiplexer Cable (Plenum) F8218-XX | Same as F8217-00 through -07 except the cable has a covering that provides fire resistance and low smoke-producing characteristics. |
| SVT 1120 Printer Cable (PVC) F8290-XX | A PVC covered cable used to connect a duplex RS-232 printer to the SVT 1120. It is a one-to-one cable with a 25-pin connector on both ends. The connectors have English screws.<br><br>F8290-00  1.1M  3ft    F8290-04  9.1M  30ft<br>F8290-01  1.5M  5ft    F8290-05  12.2M  40ft<br>F8290-02  3.0M  10ft   F8290-06  15.2M  50ft<br>F8290-03  6.1M  20ft |
| SVT 1120 Printer Cable (Plenum) F8291-XX | Same as F8290-00 through -06 except cable has a covering that provides fire resistance and low smoke-producing characteristics. |
| SVT 1122 Local Workstation T3612-02 | A UTS 20D, model 1 local workstation replacement. Provides the System 80 system mode of operation and connects to the workstation controller (F2791-04). Model 1 (T3560-10/11), model 2 (T3561-10/11) and SVT 1122 local workstations may reside on the same workstation controller. The general characteristics of the local workstation are similar to those identified for the SVT 1120 (T3612-00).<br><br>Requires power cord selection (C3381-XX), keyboard selection (F4725-XX), and workstation controller cable connection (F8265-00).<br><br>Supports auxiliary printers of the following types:<br><br>■  Model 15 (T0445-00/01 with F3860-04 interface and F8290-XX or F8291-XX printer cable).<br><br>■  Model 21 (T0471-00 with F8290-XX or F8291-XX printer cable).<br><br>■  Model 25 (T0425-07/08 with F3860-04 interface and F8290-XX or F8291-XX printer cable).<br><br>■  Model 115 (T0472-00 with F4643-00 interface and F8290-XX or F8291-XX printer cable).<br><br>■  AP1327 (with F5120-00 interface and F8290-XX printer cable).<br><br>■  AP1329 (with F5120-00 interface and F8290-XX printer cable). |

(continued)

## Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| Local Workstation Cable F8265-00 | Used to connect the SVT 1122, UTS 20D, and UTS 40D local workstation to a System 80 models 10/15/20. It is a four-wire cable with a 9-pin male connector on each end. The cable is 15.2m (50 ft.) long. |
| Local Workstation Extension Cable F8266-XX | A cable used to extend cable F8265-00. It is a four-wire cable with a 9-pin female connector on the other end. Up to four extensions can be connected, but the total cable length may not exceed 5000 ft.<br><br>F8266-01   7.6M     25ft<br>F8266-02  15.2M    50ft<br>F8266-03  30.5M   100ft<br>F8266-04  76.2M   250ft<br>F8266-05 152.4M   500ft<br>F8266-06 304.8M  1000ft<br>F8266-07 609.6M  2000ft |
| Local Workstation Extension Cable Kit F8267-XX | Connectors, instructions and, optionally, cable to fabricate a cable to extend cable F2865-00. Connectors included are a 9-pin male connector and a 9-pin female connector.<br><br>F8267-00  kit without cable<br>F8267-01     7.6M     25ft<br>F8267-02    15.2M    50ft<br>F8267-03    30.5M   100ft<br>F8267-04    76.2M   250ft<br>F8267-05   152.4M   500ft<br>F8267-06   304.8M  1000ft<br>F8267-07   609.6M  2000ft<br>F8267-08   762.0M  2500ft<br>F8267-09   794.4M  3000ft<br>F8267-10 1066.8M  3500ft<br>F8267-11 1219.2M  4000ft<br>F8267-12 1371.6M  4500ft<br>F8267-13 1524.0M  5000ft |
| SVT 1123 Remote Workstation F5069-00 | Provides System 80 system mode capability for the SVT 1120 (T3612-00) editing terminal. Provides the characteristics associated with a UTS 20 remote workstation.<br><br>When installed, terminal setup menus are restricted to four languages:<br><br>English<br>German<br>French<br>Italian<br><br>The terminal will identify itself as a SVT 1123 on the last line of the display at the completion of the power-on confidence test when F5069-00 is installed. |
| SVT 1124 Remote Workstation F5069-01 | Same as F5069-00 with the following exceptions:<br><br>■    The four terminal setup languages are:<br><br>English<br>German<br>Spanish<br>Dutch<br><br>■    The terminal identifies itself as a SVT 1124 on the last line of the display at the completion of the power-on confidence test. |

(continued)

## Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| UTS 20 Single Station Model 1 (RS-232-C) Remote Workstation T3560-02 | A freestanding, microprocessor-based, 12-inch (30.48 cm) diagonally measured CRT display screen designed to be located on a desk or counter. Operates on 120 Vac single phase, 60 Hz power. Requires SLCA with RS-232 interface. <br><br> ■ RS-232-C/CCITT V.24/X,21 BIS communications interface. Setup selection of: <br><br>     – Modem connection <br><br>     – Terminal multiplexer <br><br> ■ Auto answer/auto hangup capability <br><br> ■ User setup selectable display format: <br><br>     – 12 lines by 80 columns <br><br>     – 24 lines by 80 columns <br><br> ■ Space for a program cartridge <br><br> ■ Power cord set with NEMA 5-15P interface <br><br> Selection required: <br><br> ■ Latin (Western) alphabet (C3382-XX) with keyboards F3619-00, F3620-00, or F3621-00 <br><br> ■ Keycap usage selection (C2793-XX) with keyboards F3619-00 or F3620-00 <br><br> Feature required: <br><br> ■ Security keylock (F3388-00) <br><br> ■ Katakana/Latin keyboard (F3383-00) with keyboard F3386-00 <br><br> Optional features are one of each: <br><br> ■ Magnetic stripe reader (F3389-00) <br><br> ■ Blank keycaps (F3390-00) <br><br> ■ RAM 16K bytes (F3392-02) <br><br> ■ Tilt/rotate base (F3574-00) |
| UTS 20 Single Station Model 1 Remote Workstation, T3560-03 | Same as T3560-02, except operates on 100/120/220/240 Vac, 50/60 Hz. <br><br> ■ Voltage selection is C3395-XX <br><br> ■ Power cord set selection C3381-XX |

(continued)

## Table 1-7.  Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| UTS 20D Local Workstation, Model 1, T3560-10 | A freestanding, microprocessor-based, 12-inch (30.48 cm) diagonally measured CRT display screen designed to be located on a desk or counter. Operates from a 120 Vac single phase, 60 Hz power source. It provides: <br><br> ■ Interface to workstation controller F2791-XX at distances up to 5000 feet (1524 m). <br><br> ■ 16K bytes RAM memory for system program. <br><br> ■ 4K bytes ROM memory for load and self-test. <br><br> ■ User setup selectable display format: <br><br>   – 12 lines by 80 columns <br><br>   – 24 lines by 80 columns <br><br> ■ Power cord set with NEMA 5-15P plug (C3381-00) <br><br> ■ RS-232-C bit serial peripheral interface <br><br> Selection required on: <br><br> ■ Latin (Western) alphabet (C3382-XX) with keyboard F3619-00, F3620-00 or F3621-00 <br><br> ■ Keycap usage selection (C2793-XX) with keyboard F3619-00 or F3620-00 <br><br> ■ Local workstation functionality (C3460-00) <br><br> Features required are: <br><br> ■ Security keylock (F3388-00) <br><br> Optional features are one each of: <br><br> ■ Blank keycaps (F3390-00) <br><br> ■ Tilt/rotate base (F3574-00) |
| Local Workstation Functionality, C3460-00 | System 80 workstation functionality in 4K ROM. |
| UTS 20D Local Workstation, Model 1, T3560-11 | Same functions as T3560-10, except it operates on 100/120/220/240 Vac, 50/60 Hz. <br><br> Selection required on: <br><br> ■ Voltage cord set selection C3395-XX <br><br> ■ Power cord set selection C3381-XX |

## Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| UTS 40 Single Station Model 2 Remote Workstation, RS-232-C, T3561-02 | A freestanding, microprocessor-based, 12-inch (30.48 m) diagonally measured CRT display screen designed to be located on a desk or counter. Operates from a 120 Vac single phase, 60 Hz power source. Requires SLCA with RS-232 interface. Provides:<br><br>■ User setup selectable formats:<br><br>    – 12 lines by 80 columns<br><br>    – 24 lines by 80 columns<br><br>■ RS-232-C/CCITT V.24/X.21 BIS 9600 bps communications interface with user setup selection:<br><br>    – RS-232-C/CCITT V.24/X.21 modem interface<br><br>    – Terminal multiplexer interface<br><br>■ Auto answer/auto hangup capability<br><br>■ Space for a program cartridge<br><br>■ Power cord set with NEMA 5-15P plug (C3381-00)<br><br>Selection required on:<br><br>■ Latin (Western) alphabet (C3382-XX) with keyboard F3620-00, or F3621-00<br><br>■ Keycap usage selection (C2793-XX) with keyboard F3620-00<br><br>Features required:<br><br>■ Security keylock (F3388-00)<br><br>Optional features are one of:<br><br>■ Keyboard (F3620-00 or F3621-00)<br><br>■ Magnetic stripe reader (F3389-00)<br><br>■ Model 2 display station features F3642, F3643, and F3644<br><br>■ Blank keycaps (F3390-00)<br><br>■ PDN interface (F3459-00)<br><br>■ Tilt/rotate base (F3574-00) |
| UTS 40 Single Station Model 2 Remote Workstation, RS-232-C, T3561-03 | Same as T3561-02 except operates on 100/120/220/240 Vac, 50/60 Hz. Selection required:<br><br>■ Voltage selection C3395-XX<br><br>■ Power cord set selection C3381-XX |

(continued)

Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| UTS 40D Local Workstation Model 2, T3561-10 | A freestanding, microprocessor-based, 12-inch (30.48 cm) diagonally measured CRT display screen designed to be located on a desk or counter. Operates from 120 Vac single phase, 60 Hz power source. It provides:<br><br>■ Attachment to workstation controller, F2791-XX at distances of up to 5000 feet (1500 m)<br><br>■ 32K byte RAM memory for use by system programs<br><br>■ 4K ROM for load and self-test<br><br>■ User setup selectable display format of:<br><br>  — 12 lines by 80 columns<br><br>  — 24 lines by 80 columns<br><br>■ Power cord set with NEMA 5-15P plug (C3381-00)<br><br>Selection required on:<br><br>■ Latin (Western) alphabet (C3382-XX) with keyboard F3620-00, or F3621-00<br><br>■ Keycap usage selection (C2793-XX) with keyboard or F3620-00<br><br>Features required are:<br><br>■ Security keylock (F3388-00)<br><br>Optional features are one of the following:<br><br>■ Keyboard (F3620-00, F3621-00)<br><br>■ Magnetic stripe reader (F3389-00)<br><br>■ Model 2 display station feature (F3642/43/44)<br><br>■ Blank keycaps (F3390-00)<br><br>■ Tilt/rotate base (F3574-00) |
| UTS 40D Local Workstation Model 2, T3561-11 | Same as T3561-10, except operates on 100/120/220/240 Vac, 50/60 Hz.<br><br>Selection required:<br><br>■ Voltage selection C3395-XX<br><br>■ Power cord set selection C3381-XX |
| Latin Alphabet Character Set, C3382-XX | Provides a Latin (Western) alphabet 96-character set for T3560-XX and T3561-XX:<br><br>C3382-00  Domestic (ASCII)       C3382-04  Spain<br><br>C3382-01  United Kingdom (Set 1)  C3382-05  Denmark/Norway<br><br>C3382-02  Germany (Set 2)       C3382-06  Sweden/Finland<br><br>C3382-03  France (Set 1)        C3382-07  Italy (Set 2) |

## Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| Keyboard Model A<br>F3619-XX | Provides a typewriter style keyboard for T3560-XX or T3561-XX workstation. |
| Keyboard Model A<br>F3619-00 | Keyboard in UTS 400 mode. Selection required on national keycaps that must match the character font selection from C3382-XX. |
| National Keycaps UTS 400 Mode, C2793-XX | Provides national keycap lettering for model A keyboard F3916-00 and model B keyboard F3620-00. Selection is from:<br><br>C2793-00  Domestic (ASCII)<br><br>C2793-01  United Kingdom (Set 1)<br><br>C2793-02  Germany (Set 2)<br><br>C2793-03  France (Set 1)<br><br>C2793-04  Spain<br><br>C2793-05  Denmark/Norway<br><br>C2793-06  Sweden/Finland<br><br>C2793-07  Italy (Set 2) |
| Keyboard Model B<br>F3620-XX | Provides a typewriter style keyboard, numeric pad, and a function pad for T3560-XX and T3561-XX workstations. |
| Keyboard Model B<br>F3620-00 | Keyboard in UTS 400 mode. Selection required on national keycaps (C2793-XX) that must match the character font selection from C3382-XX. |
| Keyboard Model D<br>(UTS 400 Compatible Domestic), F3621-XX | Provides a domestic UTS 400 layout with a compatible keyboard for T3560-XX and T3561-XX. Requires character set selection C3382-00. |
| Keyboard Model D<br>F3621-00 | Model D keyboard at UTS 400 mode |
| Security Keylock<br>F3388-00 | Provides a security keylock for T3560-XX or T3561-XX workstations with two functions. One key disables/enables input from the keyboard and magnetic stripe reader. The second key disables/enables the ability to change customer setup variables. |
| Magnetic Stripe Reader<br>F3389-00 | Provides a magnetic stripe reader capable of reading International Air Transport Association (IATA) or American Banking Association (ABA) format for T3560-XX or T3561-XX workstations. |
| Blank Keycaps<br>F3390-00 | Provides a blank keycap for keyboard model A or B (F3619-00/F3620-00). Keyboard model A or B is a prerequisite. |
| Tilt/Rotate Base<br>F3574-00 | Provides a separate base for display stations T3560-XX and T3561-XX that allows the display to be tilted or rotated. |

(continued)

## Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| Model 2 Display Station Features | F3643-00 Eight-bit peripheral interface provides an interface on T3561-XX for use with mode 1 and mode 2 buffered peripherals that conform to specification SR00486. |
| | F3642-00 32K RAM provides parity protected volatile RAM for T3561-XX |
| | F3642-01 32K RAM expansion provides an additional 32K bytes of parity protected volatile RAM for T3561-XX. Feature F3242-00 is a prerequisite. |
| | F3644-00 Expansion module provides expansion that allows addition of an 8-bit peripheral interface expansion (F3644-02), light pen (F3644-01), and loadable character set (F3644-03). |
| | F3644-01 Light pen for T3561-XX. Feature F3644-00 is a prerequisite. |
| | F3644-02 Eight-bit peripheral expansion provides an 8-bit peripheral interface on T3561-XX for use with mode 1 and mode 2 buffered peripherals that conform to interface specification SR00486. Expansion module F3644-00 is a prerequisite. |
| | F3644-03 Loadabale character set provides a 256 characater-loadable generator for T3561-XX. Expansion module F3644-00 is a prerequisite. |
| RAM 16K Bytes F3392-02 | Provides 16K bytes of parity-protected volatile RAM for model 1 workstation T3560-02/03. |
| I/O Cable Selection C3625-XX | Provides selection of I/O cables for T3560-XX and T3561-XX workstations and T1955 remote printer attachment as follows: |
| | C3625-00 Fifty-foot (15.24 m) I/O cable for single workstation and remote printer attachment. |
| | C3625-03 Fifty-foot (15.24 m) I/O cable for single workstation and console workstation. |
| PDN Interface F3459-00 | Provides packet-switched PDN interface support for T3561-02/03 workstations. |
| Voltage Selection C3395-XX | Provides operation voltage selection for T3560-01, T3560-11, T3561-03, and T3561-11 workstations, as follows: |
| | C3395-00 100 Vac |
| | C3395-01 120 Vac |
| | C3395-02 220 Vac |
| | C3395-03 240 Vac |

(continued)

## Table 1-7. Workstations and Terminals (cont)

| Type/Feature | Description |
|---|---|
| Power Cord Set Selection C3381-XX | Provides power cord set selection for T3560-03/11 and T3561-03/11. Each cord set is 6 feet, 7 inches (2.07 m) long. An IEC 320 Vac appliance coupler is provided at the equipment end of the cord. The power plug must be compatible with voltage selection. Power cord set selection is:<br><br>C3381-00  NEMA 5-I5P plug with ground pin, capable of operating with 125 Vac, 15 amperes (maximum) in USA and Canada.<br><br>C3381-01  SEV 1011 plug with ground pin, capable of operating with 250 Vac, 10 amperes (maximum) in Switzerland.<br><br>C3381-02  IEC 83/C5 plug with contact tube and ground side conforming to CEE 7/VII and IEC 83/C5. Operates on 250 Vac, 16 amperes (maximum) in:<br><br>Algeria<br>Austria<br>Belgium<br>Bulgaria<br>Finland<br>France<br>Germany<br>Hungary<br>Iceland<br>Indonesia<br>Iran<br>Malaysia<br>Netherlands<br>Norway<br>Poland<br>Portugal<br>Rumania<br>Spain<br>Sweden<br>Yugoslavia<br><br>C3381-03  United Kingdom/Ireland standard plug with ground pin. Operates on 250 Vac, 13 amperes (maximum). Plug definition to be determined.<br><br>C3381-04  Cord set without power plug. Provides IEC 320/V appliance coupler on equipment end and no plug on the opposite end.<br><br>C3381-05  No cord set.<br><br>C3381-06  NEMA 6-15P plug with ground pin. Operates on 250 Vac, 6 amperes. |

# Table 1-8. Distributed Communications Processor (DCP) Products

| Type/Feature | Description |
|---|---|
| Distributed Communications Processor/15 (DCP/15) K4035-03 | Provides a DCP/15 enclosure that can be mounted in a 19-inch rack. The enclosure includes power supplies, power distribution, cooling, operator panel, a single-port PCA containing the CP and I/O processor and 2MB ECC local storage, and mounting space for fourteen line modules comprised of up to 14 PCAs. One or two K4035-03 DCP/15 enclosures may be mounted in the DCP/15 cabinet, 1986-01.<br><br>Local storage may be expanded to 4MB by adding one storage expansion feature (F4961-00). Requires power supply expansion (F3895-01) for any of the four following configurations: 1) six or more line modules with no F3164-XX, 2) one F3164-XX and two or more other line modules, 3) two F3164-XX, 4) one F1947-03. A maximum of two high-speed loadable LMs may be configured. A maximum of one SU00208 with one F3164-XX may be configured. An integrated 5–1/4-inch flexible disk drive (F4157-00) and a 5–1/4-inch rigid disk drive (F4158-01) may be mounted in the enclosure. Both drives are connected to a disk drive controller (F4232-00), which interfaces a multiple device line module (MDLM) (F3893-00). Both the controller and the MDLM are required when either or both of the disk drives are configured. The enclosure includes an operator control panel and mounting space for the active line indicator panel (F3897-01). A power cord selection (C3381-XX) and voltage selection (C4087-XX) are required. The remote power control feature (F3896-01) may be installed as an option. |
| Voltage Selection C4087-XX | Provides voltage selection for K4035-03.<br><br>C4087-00   100-110v, 50/60 hz<br>C4087-01   110-120v, 50/60 hz<br>C4087-02   200-240v, 50/60 hz |
| DCP/15 Cabinet 1986-01 | A cabinet capable of housing one or two K4035-03 DCP/15 enclosures. The cabinet is 37.5 inches high, 23 inches wide, and 31 inches deep. Requires power cord selection from C3381-14 through 24. |
| Storage Expansion Feature, 2M F4961-00 | Provides K4035-03 with a set of 2M bytes of memory chips that are plugged into the processor board. A maximum of one Storage Expansion Feature is permitted. |
| Integrated Flexible Disk F4157-00 | Provides 1MB of unformatted storage via a 5–1/4-inch flexible disk drive mounted in the K4035-03 enclosure. Requires the multiple device line module (F3893-00), disk drive controller (F4232-00) and a 5–1/4-inch flexible disk medium (F3922-02) containing microprograms and a loader program. |
| Integrated Rigid Disk F4158-01 | Provides 20MB of formatted mass storage via 5–1/4-inch rigid disk drive mounted in the K4035-03 enclosure. Requires the multiple device line module (F3893-00) and the disk drive controller (F4232-00). |
| DCP/15 Microprograms F3922-02 | A flexible disk medium containing DCP/15 primary mode microprograms, microproams for loadable line modules, and a loader program that allows system loading of Telcon software. Used with F4157-00 integrated flexible disk. |
| Multiple Device Line Module F3893-00 | Provides the K4035-03 (DCP/15) with an interface to both the integrated rigid flexible disk drive controller (F4232-00) and the freestanding 8441 mass storage subsystem. Requires the F4232-00 controller when either the integrated flexible disk F4157-00 or the integrated rigid disk F4158-01 is installed. Requires an SCSI I/O cable, F8288-XX, when interfacing to the freestanding 8441 mass storage subsystem. With the selection of both F4232-00 and F8288-XX, the line module may interface both the integrated (F4157-00, F4158-01, and the external 8441 mass storage susbsystem. The line module occupies one DCP I/O port. |
| Disk Drive Controller F4232-00 | Small computer system interface (SCSI) controller which controls the integrated flexible disk drive (F4157-00) and the integrated rigid disk drive (F4158-01) in the K4035-03 DCP/15 system. |

(continued)

## Table 1-8. Distributed Communications Processor (DCP) Products (cont)

| Type/Feature | Description |
|---|---|
| Asynchronous Communication Line Module (EIA/CCITT) F1941-00 | Provides a full-duplex interface to asynchronous data sets operating at data rates of 45.5, 50, 56.8, 74.2, 75, 100, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, or 2400 bps. Operates with Teletypewriter protocol. The interface conforms to EIA RS-232-C and CCITT recommendations V.24 and V.28. The F1941-00 feature does not include the communications interface cable. A cable selection is required from features F8303, F8304, F8305, F8306, or F8200-00. |
| Synchronous Communication Line Module (EIA/CCITT) F1942-00 | Provides a full-duplex interface to synchronous data sets operating at data rates up to 9600 bps. Operates with synchronous UNISCOPE protocol. The interface conforms to EIA RS–232-C and CCITT recommendations V.24 and V.28. An interface cable selection is required from features F8303, F8305, F8244, F8234, F8235 or F8200-00. |
| Medium-Speed Loadable Line Module (RS–232-C) F3163-00 | Provides a full-duplex interface to a synchronous or asynchronous modem with an interface conforming to EIA RS-232-C and CCITT recommendations V.24 and V.28. Also operates with Bell DDS up to 9600 bps. The line module can be loaded with a microprogram for operation with data formats for the following protocols:<br>- Basic asynchronous up to 19,200 bps<br>- Basic synchronous up to 19,200 bps<br>- UDLC up to 19,200 bps<br>- BSC up to 9600 bps<br>- REM1 up to 19,200 bps<br>- 1100 FDX up to 19,200 bps.<br>Basic asynchronous protocol includes ADRD capability for 110, 150, 300, 600, 1200, and 1800 bps, plus the ability to reload the ADRD table for detection of other data rates. A communications interface cable is required and must be selected from F8303, F8304, F8305, F8306, F8307, F8244, F8234, F8235, or F8200-00. |
| Medium Speed Loadable Line Module (X.21) F3163-01 | Provides a full-duplex interface to switched services of Public Data Networks conforming to CCITT recommendation X.21. The line module can be loaded with a microprogram for operation with data formats for the following protocols.<br>- Basic synchronous up to 9600 bps<br>- BSC up to 9600 bps<br>- UDLC up to 9600 bps<br>- 1100 FDX up to 9600 bps<br>A communications interface cable is required and must be selected from feature F8308-XX or F8200-00. |
| High-Speed Loadable Line Module (Bell 303) F3164-00 | Provides full-duplex interface to a Bell System 303 modem. Can be loaded with a microprogram for operation with data formats for the following protocols:<br>- Basic synchronous up to 64K bps.<br>- UDLC up to 64K bps.<br>- BSC up to 64K bps.<br>- REM1 up to 64K bps.<br>- 1100 FDX up to 64K bps.<br>A communications interface cable is required and must be selected from features F8311-XX or F8200-00. Maximum of two F3164-00 with no host channel; maximum of one F3164-00 with one host channel. (F3164-00 must be installed in ports 0-6.) |
| High-Speed Loadable Line Module (V.35) F3164-01 | Provides a full-duplex interface to carrier facilities conforming to CCITT recommendation V.35. Can be loaded with a microprogram for operation with data formats for the following protocols:<br>- Basic synchronous up to 64K bps<br>- UDLC up to 64K bps<br>- BSC up to 64K bps<br>- REM1 up to 64K bps<br>- 1100 FDX up to 64K bps<br>Operates with European V.35 facilities (48K bps) and Bell DDS and DSDS facilities (56K bps). A communications interface cable is required and must be selected from features F8312-XX or F8200-00. Same configuration restrictions as F3164-00. |

(continued)

**Table 1-8. Distributed Communications Processor (DCP) Products (cont)**

| Type/Feature | Description |
|---|---|
| Multiline Sync/Async Line Module F3837-00 | Provides four synchronous or asynchronous, full-duplex interfaces to data sets and/or direct-connect terminals. The interfaces conform to EIA RS–232-C and CCITT recommendations V.24 and V.28. Maximum synchronous data rate on four full-duplex lines operating simultaneously is up to 9600 bps per line. The following asynchronous data rates are supported (rates may be different on each interface): 45.5, 50, 56.8, 74.2, 75, 100, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, 3600, 4800, 7200 or 9600 bps. Alternately, any two interfaces may operate at 19.2K bps synchronous or asynchronous full-duplex if the other two interfaces are not used. Synchronous protocols supported are UNISCOPE and UDLC. Asynchronous protocols supported are TTY, Videotex-Phase II, and UNIX. All protocols except UNISCOPE operate up to 19.2K bps. (Maximum UNISCOPE rate is 9600 bps.) The line module includes ADRD capability for 110, 150, 300, 600, 1200 and 1800 bps, plus the ability to reload the ADRD table for detection of other data rates. For Videotex applications, the line module may be programmed for different transmit speeds on the four RS-232-C/V.24 interfaces, selected from the rates specified above. The receive speed on each interface can be equal to or 1/8 or 1/16 of the transmit speed. The divider (1/8 or 1/16) must be the same on ports 0 and 1, and the same on ports 2 and 3. The line module has echo-plex capability, whereby the LM can automatically retransmit each character it receives. Up to four interface cables are required and must be selected from features F8303, F8304, F8305, F8306, F8307, F8244, F8234, F8235, or F8200-00. |
| Automatic Dialing Line Module F1945-00 | Provides an interface to Bell 801 automatic calling units or automatic calling units conforming to CCITT recommendations V.24 and V.25. Each dialing interface must be associated with a line module for the transfer of data (F1941-00, F1942-00, etc.). A communications interface cable is required and must be selected from features F8313, F8314, or F8200-00. |
| SU00208 Host Interface Line Module F1947-03 | Provides DCP/15 with a SU00208 interface to a host system byte or block multiplexer channel. Occupies 3 PC assemblies and attaches to 2 ports on the DCP/15 L-bus. Requires 1 spare slot for cooling. Maximum of 1 host interface per K4035-03 enclosure. Includes a bulkhead assembly for use in DCP/15 systems. Requires F3895-01 and a cable feature F8316, F8317 or F8200-00. |
| Direct Connect Single Station Line Module F3847-00 | Provides an interface for up to 16 multidropped UTS 4000 Direct Connect Single Stations (DCSS). The line module is loaded with a microprogram for operation with data formats of UDLC protocol. It operates at 250K bits per second over a maximum distance of 5000 feet. The required coaxial cable is available with the UTS 4000 DCSS. To provide resiliency, two DCSS line modules may be connected to the coaxial cable. Only one DCP line module may be active at one time. Each feature includes one line module, a five-foot coaxial adapter cable, T-connector, and two terminators. |
| Power Supply Expansion F3895-01 | Provides K4035-03 DCP/15 with additional +5 volt power. Required for any of the following configurations: 1) six or more line modules with no F3164-XX, 2) one F3164-XX and two or more other line modules, 3) two F3164-XX, 4) one F1947-03, F1946-02, or F4987-01 host interface line module. |
| Active Line Indicators F3897-01 | Provides the capability to monitor up to 14 half/full duplex communication interfaces in K4035-03. Three manual switches control which of the two banks of seven communications lines and which one of the four interfaces on the multiline modules are to be monitored. |

(continued)

**Table 1-8. Distributed Communications Processor (DCP) Products (cont)**

| Type/Feature | Description |
|---|---|
| Power Cord<br>C3381-XX | This selects the power cord required for the K4035-03 DCP/15 system. Selection is from:<br><br>C3381-XX  This selects the power cord required for the K4035-03 DCP/15 system.<br><br>C3381-14  NEMA 5-15P power plug, CEE 22 cabinet plug, 10 amp., Type SJT cable, black. Usage: USA, Canada, Korea, and Japan.<br><br>C3381-15  SEV Type 12 power plug, CEE 22 cabinet plug, 10 amp., black. Usage: Switzerland.<br><br>C3381-16  CEE7/VII power plug, CEE 22 cabinet plug, 10 amp., black. Usage: Austria, Belgium, Finland, France, Germany, Netherlands, Norway, Sweden, generally Portugal and Spain.<br><br>C3381-17  BS 1363 fused power plug, CEE 22 cabinet plug, 10 amp., black. Usage: United Kingdom, Hong Kong, Singapore, Malaysia.<br><br>C3381-18  Cord set without power plug, with CEE 22 cabinet plug, 10 amp., black. Usage: Generally universal. Requires grounded power plug in country used. Not used in USA or Canada.<br><br>C3381-19  Australian power plug, CEE 22 cabinet plug, 10 amp., black. Usage: Australia.<br><br>C3381-20  Danish power plug, CEE 22 cabinet plug, 10 amp., black. Usage: Denmark<br><br>C3381-21  BS 546 power plug, CEE 22 cabinet plug, 10 amp., black. Usage: South Africa and India<br><br>C3381-22  Italian power plug, CEE 22 cabinet plug, 10 amp., black. Usage: Italy.<br><br>C3381-23  Italian heavy duty power plug, with CEE 22 cabinet plug, 10 amp., black. Usage: Italy. |
| RS-232/V.24<br>Modem Cable<br>(2816358)<br>F8303-XX | Provides a cable to connect an RS-232-C/V.24 modem to F1941-00, F1942-00, F3163-00, F3165-01, or F3837-00.<br><br>F8303-00      4.6M      15ft<br>F8303-01      7.6M      25ft<br>F8303-02      12.2M      40ft<br>F8303-03      15.2M      50ft<br>F8303-04      1.8M        6ft |
| Direct Connect<br>Cable (2821423)<br>F8304-XX | Provides a cable for direct connection to an asynchronous terminal with an RS-232-C/V.24, V.28 interface. The terminal cable with its RS-232 connector is used with F8304-XX to provide a total length of up to 300 ft.<br><br>F8304-00      4.6M        15ft<br>F8304-01      7.6M        25ft<br>F8304-02      15.2M      50ft<br>F8304-03      30.5M      100ft<br>F8304-04      61.0M      200ft<br>F8304-05      76.3M      250ft |

(continued)

## Table 1-8. Distributed Communications Processor (DCP) Products (cont)

| Type/Feature | Description |
|---|---|
| Trend Adapter Cable (2824178) F8306-XX | Provides a cable with connector pin 18 (Return to non-data mode) connected to the line module data signaling rate selector driver. Used to connect a trend Telex adapter to the line module.<br><br>F8306-00     4.6M     15ft<br>F8306-01     7.6M     25ft<br>F8306-02     12.2M     40ft<br>F8306-03     15.2M     50ft |
| CCITT Test Loopback Cable (2826449) F8307-XX | Provides a cable to connect to a CCITT modem. The cable is similar to F8303-XX except it is wired according to ISO 2110-1980. This provides compatibility with late Model V series modems including wires for the local loopback, remote loopback, and test indicator signals. Allows loopback support with the proper software, line module and modem.<br><br>F8307-00     4M     13.1ft<br>F8307-01     8M     26.2ft<br>F8307-02     12M     39.4ft<br>F8307-03     16M     52.5ft |
| Direct Connect Cable (2824690) F8244-00 | Provides a 50-foot cable for direct connection to a synchronous Unisys terminal or terminal multiplexer through a U-100 junction box and an external cable. Cable lengths beyond the junction box are limited to 4950 ft. up to 4800 bps or 2450 ft. at 9600 bps. |
| Direct Connect Cable (PVC) (2824691) F8234-XX | Provides a cable with a connector which is suitable for direct connection to a synchronous Unisys terminal or terminal multiplexer.<br><br>F8234-01     4M     13.1ft<br>F8234-02     8M     26.2ft<br>F8234-03     12M     39.4ft<br>F8234-04     16M     52.5ft<br>F8234-05     30.5M     100.0ft |
| Direct Connect Cable (Teflon) F8235-XX | Same cable as F8234-XX except cover is Teflon.<br><br>F8235-01     4M     13.1ft<br>F8235-02     8M     26.2ft<br>F8235-03     12M     39.4ft<br>F8235-04     16M     52.5ft<br>F8235-05     30.5M     100.0ft |
| X.21 Cable (2826034) F8308-XX | Provides a cable for connection to an X.21 standard DCE.<br><br>F8308-00     4.6M     15ft<br>F8308-01     7.6M     25ft<br>F8308-02     12.2M     40ft<br>F8308-03     15.2M     50ft<br>F8308-04     30.5M     100ft<br>F8308-05     45.7M     150ft<br>F8308-06     61.0M     200ft |
| Bell 303 Modem Cable (2824870) F8311-XX | Provides a cable for connection to a Bell System 303 or equivalent modem.<br><br>F8311-00     4.6M     15ft<br>F8311-01     7.6M     25ft<br>F8311-02     12.2M     40ft<br>F8311-03     15.2M     50ft |

(continued)

**Table 1-8. Distributed Communications Processor (DCP) Products (cont)**

| Type/Feature | Description |
|---|---|
| V.35 Modem Cable (2826033) F8312-XX | Provides a cable for connection to a CCITT V.35 standard DCE interface.<br><br>F8312-00    4.6M    15ft<br>F8312-01    7.6M    25ft<br>F8312-02   15.2M   50ft<br>F8312-03   24.4M   80ft<br>F8312-04   30.5M  100ft |
| Bell 801 Dialer Cable (2816359) F8313-XX | Provides a cable for connection to a Bell System 801 dialer or equivalent.<br><br>F8313-00    4.6M    15ft<br>F8313-01    7.6M    25ft<br>F8313-02   12.2M   40ft<br>F8313-03   15.2M   50ft |
| SU00208 LM Cable (4268520) F8316-XX | Provides a cable for connection to a Series 90/70 host system when the SU00208 host interface LM (F1947-03) is configured.<br><br>F8316-00    7.6M    25ft<br>F8316-01   15.2M   50ft<br>F8316-02   30.5M  100ft<br>F8316-03   45.7M  150ft<br>F8316-04   61.0M  200ft |
| SU00208 LM Cable (4268732) F8317-XX | Provides two cables for connection to a Series 90/80 or Series 1100 host system when the SU00208 host interface LM (F1947-03) is configured.<br><br>F8317-00    7.6M    25ft<br>F8317-01   15.2M   50ft<br>F8317-02   30.5M  100ft<br>F8317-03   45.7M  150ft<br>F8317-04   61.0M  200ft |
| SCSI I/O Cable F8288-XX | The SCSI I/O cable is required for connecting the 8441 mass storage subsystem to the DCP/15 system. Cable lengths are as follows:<br><br>F8288-00    0.9M    3ft<br>F8288-01    1.5M    5ft<br>F8288-02    3.0M   10ft<br>F8288-03    6.1M   20ft<br>F8288-04    9.1M   30ft<br>F8288-05   15.2M   50ft |
| Customer- provided Cable F8200-00 | This no-cost feature provides a way for the customer to indicate that he will provide his own cable. |

(continued)

## Table 1-8. Distributed Communications Processor (DCP) Products (cont)

| Type/Feature | Description |
|---|---|
| Distributed Communications Processor/40 (DCP/40) 8596-00 | A communications-oriented processor with a storage controller and 128K bytes of storage housed in a freestanding cabinet. Includes an I/O controller module, a communications line .controller (CLC), line module chassis, maintenance panel, power supplies and power control. A flexible disk and controller (F1939-00/01 or F3139-00/01), a microprogram storage feature (F2923-XX), and a microprogram feature (F1931-XX) must be ordered. Mounting for three additional storage arrays (F1930-00) is provided. With the addition of a storage port expander (F1936-00) and CLC power expansion (F2941-00), three additional CLCs (F1932-00) and line module chassis (F2938-00) can be included in the cabinet. Emulation mode requires F1934-00, one F1935-00 per type II scanner, and one F1950-00 per CLC. Operates over a voltage range from 200 to 240 volts, single phase, 50/60 Hz. |
| Distributed Communications Processor/40 (DCP/40) 8596-01/02 | Same as 8596-00 except the 512K storage array (K1930-01) and associated controller are supported. 8596-01 includes one 512K storage array and storage controller. Up to three K1930-01 storage arrays may be added for a total of 2.0M bytes of storage. The 8596-02 requires F2941-00 for CLC expansion beyond the first CLC. |
| Mass Storage Subsystem For DCP/40 8441-00/01 | Subsystem may be configured with the 5-1/4-inch Winchester disk and the 5-1/4-inch flexible disk. The subsystem interfaces to the multiple device line module in the DCP. This line module needs only one processor when interfacing to an 8441 mass storage subsystem. |
| Direct Communication Module 8610-00 | Freestanding modem replacement device with CSU options for baud rate, mode, duplexing, CTS delay, and test mode for synchronous operation. Synchronous operation between buildings is allowed through isolated lines. Asynchronous operation requires Unisys specified cables. One DCM is required per terminal. Up to 4 DCMs may be connected in multi-drop synchronous. Synchronous baud rates are switch selectable. |
| F4228-00/01 | F4228-00 is the first 28MB disk drive. Same as F4271-00 except it is 28MB of storage. F4228-01 is the second 28MB disk drive. It provides a second 30.24MB (formatted) disk drive expansion for an 8441-00/01 mass storage cabinet. |
| Expansion Cabinet for Distributed Communications Processor/40 1945-00/01 | Freestanding cabinet for expanding DCP/40 systems. Contains a power supply and a power controller. With the addition of F1933-00, accommodates up to four CLCs (F1932-00). Can also accommodate either three storage banks with F2942-00 installed, or a processor and one storage bank with F2940-00/01 installed or two storage banks with F2942-01 installed. The 1945-01 requires F2941-01 for the second through fourth CLC's. |
| Microprogram Storage F2923-02 | Provides the DCP/40 processor with microprogram storage for enhanced mode operation. Mutually exclusive with F2923-00. |
| Work Surface F1928-00 | A freestanding sit/stand work surface that can be used for locating the local console and freestanding flexible disk in a DCP/40 system. Dimensions are 60 inches (153 cm) wide by 30 inches (77 cm) deep by 38 inches (97 cm) high. |
| Storage Controller F1929-00 | Provides four storage access ports and controller for one storage bank of from one to four storage arrays, F1930-00. One storage controller is included in 8596-00 and in F2942-00. |
| Storage Controller F1929-02 | Converts the storage of an 8596-00 to the storage of an 8596-01 with 1.0MB of memory. Feature consists of a storage controller and two 512KB array cards. |

(continued)

## Table 1-8. Distributed Communications Processor (DCP) Products (cont)

| Type/Feature | Description |
|---|---|
| Storage Array 128K Byte F1930-00 | Provides a 128K byte storage array for 8596-00 or 1945-00. One array is included in 8596-00 and additional features are optional in DCP/40 configurations. A maximum of three F1930-00 can be added to 8596-00. Up to eleven F1930-00 can be added to 1945-00. |
| Storage Array 512K Byte K1930-01 | Provides a 512K byte storage array for 8596-01 or 1945-00. A maximum of three K1930-01 can be added to 8596-01. Up to seven K1930-01 can be added to 1945-00. |
| Enhanced Mode Microprograms F1931-02 | Similar to F1931-01 except the DCP/40 processor and CLC microprograms provide for enhanced mode operations per R50237 and contains line module microprograms. The loader program also allows loading from a fixed media disk (8409) or an integrated flexible disk (F3139-XX). Requires microprogram storage feature F2923-02 in the DCP/40 processor. |
| Communication Line Controller F1932-00 | A microcontroller providing for control of up to 16 line module features. Physical mounting for up to four microcontrollers is provided in 8596-00/01 and by F1933-00. |
| Controller Module F1933-00 | Provides mounting space for up to four CLC microcontrollers and a storage port expander. The first CLC and line module chassis (equivalent to F1932-00 and F2938-00) are included. Also includes a cable to local storage and a maintenance panel which can be shared by up to four CLCs mounted in the controller module. Installs in 1945-00. |
| Storage Port Expander F1936-00 | Provides a multiplexed interface to a single local storage access port for up to four requestors. Installation is required in the controller module in F1933-00 in 1945-00 when the number of storage requestors, CLC (F1932-00) or SSA (F1935-00), exceeds a total of two. Installation is required in the processor/storage module in 8596-00 or in F2940-00 in 1945-00 when the number of storage requestors exceeds four. |
| Integrated Flexible Disk and Controller F1939-00 | Provides 256K bytes of storage via a flexible disk drive and control logic installed in the 8596-00/01 cabinet. The control logic occupies one line module position on a CLC L-bus. Cabling between the drive and controller line module is included. Drive operates on 60 Hz power derived from cabinet power. May be installed in 1945-00 after installation of F1932-00 and F2938-00. |
| Integrated Flexible Disk and Controller F1939-01 | Same as F1939-00 except drive operates on 50 Hz. |
| Integrated Flexible Disk and Controller F3139-00 | Similar to F1939-00 except provides 1024K bytes of storage using a double-sided flexible medium with double-density recording. Write protection and single-density capability are provided. |
| Integrated Flexible Disk and Controller F3139-01 | Same as F3139-00 except drive operates on 50 Hz. |
| Asynchronous Communication Line Module (EIA-CCITT) F1941-00 | Provides a full-duplex interface to asynchronous data sets operating at data rates of 45.5, 50, 56.8, 74.2, 75, 100, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, or 2400 bps. The interface conforms to EIA RS-232-C and CCITT recommendations V.24 and V.28. The F1941-00 feature does not include the communications interface cable. The cable is required and must be selected from F8303, F8304, F8305, F8306, or F8200-00. |

(continued)

**Table 1-8. Distributed Communications Processor (DCP) Products (cont)**

| Type/Feature | Description |
|---|---|
| Synchronous Communication Line Module (EIA/CCITT) F1942-00 | Provides a full-duplex interface to synchronous data sets operating at data rates up to 9600 bps. The interface conforms to EIA RS-232-C and CCITT recommendations V.24 and V.23. The F1942-00 feature does not include the communications interface cable. The cable is required and must be selected from F8303, F8305, F8244, F8234, or F8200-00. |
| Medium Speed Loadable Line Module (RS-232-C) F3163-00 | Provides a full-duplex interface to a synchronous or asynchronous modem with an interface conforming to EIA RS-232-C and CCITT recommendations V.24 and V.28. Also operates with Bell DDS up to 9600 bps. The line module can be loaded with a microprogram for operation with data formats for the following protocols:<br>- Basic asynchronous up to 19,200 bps<br>- Basic synchronous up to 19,200 bps<br>- UDLC up to 19,200 bps<br>- BSC up to 9600 bps<br>- REM1 up to 19,200 bps<br>- 1100 FDX up to 19,200 bps<br>The F3163-00 feature does not include the communications interface cable. The cable is required and must be selected from F8303, F8304, F8305, F8306, F8307, F8244, F8234, or F8200-00. |
| Medium Speed Loadable Line Module (X.21) F3163-01 | Provides a full-duplex interface to switched servces of public data networks conforming to CCITT recommendation X.21. The line module can be loaded with a microprogram for operation with data formats for the following protocols:<br>- Basic synchronous up to 9600 bps<br>- BSC up to 9600 bps<br>- UDLC up to 9600 bps<br>- 1100 FDX up to 9600 bps<br>The F3163-00 feature does not include the communications interface cable. The cable is required and must be selected from feature F8308 or F8200-00. |
| High Speed Loadable Line Module (Bell 303) F3164-00 | Provides a full-duplex interface to a Bell System 303 model. Can be loaded with a microprogram for operation with data formats for the following protocols:<br>- Basic synchronous up to 64K bps<br>- UDLC up to 64K bps<br>- BSC up to 64K bps<br>- REM1 up to 64K bps<br>- 1100 FDX up to 64K bps<br>The F3164-00 feature does not include the communications interface cable. The cable is required and must be selected from feature F8311 or F8200-00. |
| High Speed Loadable Line Module (V.35) F3164-00 | Provides a full-duplex interface to carrier facilities conforming to CCITT recommendation V.35. Can be loaded with a microprogram for operation with data formats for the following protocols:<br>- Basic synchronous up to 64K bps<br>- UDLC up to 64K bps<br>- BSC up to 64K bps<br>- REM1 up to 64K bps<br>- 1100 FDX up to 64K bps<br>Operates with European V.35 facilities (48K bps), Bell DDS and SDDS facilities (56 bps). The F3164-01 feature does not include the communications interface cable. The cable is required and must be selected from feature F8312 or F8200-00. |
| Automatic Dialing Line Module F1945-00 | Provides an interface to Bell 801 automatic calling units or automatic calling units conforming to CCITT recommendations V.24 and V.25. Each dialing interface must be associated with a line module for the transfer of data (F1941-00, F1942-00, etc.). NTT Automatic Calling Unit to supported ACUs. The F1945-00 feature does not include the communications interface cable. The cable is required and must be selected from F8313, F8314, or F8200-00. |

(continued)

### Table 1-8. Distributed Communications Processor (DCP) Products (cont)

| Type/Feature | Description |
|---|---|
| SU00208<br>Host Interface<br>Line Module<br>F1947-02 | Provides DCP 20/40 with an SU00208 interface to a host system byte or block multiplexer channel. Occupies three MLP printed circuit assemblies and attaches to two ports on the IOP L-bus. Includes a bulkhead assembly, enable/disable/test switch and online indicator. A selection from C3560-XX is required. Maximum of two host interfaces per 8596-00/01 or 1945-00 cabinet. Maximum of one host interface per 8597-00/01 cabinet. |
| DCP/40<br>Operator Panel<br>C3560-00 | Provides a DCP/40 operator control panel with provisions to mount one SU00039 LM enable/disable/test switch and associated online indicator. Required when one SU00039 LM (F1947-00) is configured in the 8596-00 or 1945-00 cabinet. |
| DCP/40<br>Operator Panel<br>C3560-01 | Provides a DCP/40 operator control panel with provisions to mount two SU00039 LM enable/disable/test switches and associated online indicators. Required when two SU00039 LMS (F1947-00) are configured in the 8596-00 or 1945-00 cabinet. |
| DCP/40<br>Operator Panel<br>C3560-04 | Provides a DCP/40 operator control panel with provisions to mount one SU00208 LM byte/disable/block switch and associated online indicator. Required when one SU00208 LM (F1947-02) is configured in the 8596 or 1945 cabinet. |
| DCP/40<br>Operator Panel<br>C3560-05 | Provides a DCP/40 operator control panel with provisions to mount two SU00208 LM byte/disable/block switches and associated online indicators. Required when two SU00208 LMS (F1947-02) are configured in the 8596 or 1945 cabinet. |
| NEMA Plug<br>C3381-00 | NEMA 5-15P plug with grid pin 15A maximum, 125V (U.S.A., Canada, Korea, Japan). |
| Voltage Selection<br>C3781-00 | Voltage selection 50/60 Hz. Voltage selection for T8543-XX, 115V. |
| Multiline<br>Synchronous<br>Line Module<br>F3837-00 | Provides up to four full-duplex interfaces to data sets and/or direct connect terminals. The interfaces conform to EIA RS-232C and CCITT recommendations V.24 and V.28. UNISCOPE and UDLC protocols are supported. Protocols may not be mixed on the line module. Maximum data rate on four full-duplex lines operating simultaneously is up to 9600 bps per line. The F3837-00 feature does not include any communications interface cables. Up to four cables are required and must be selected from feature F8303-XX, F8305-XX, F8244-00, F8234-XX or F8200-00. |
| Multiline Sync/Async<br>Line Module<br>F3837-03 | Same as F3837-00 except line module storage has been expanded to 512K bytes for support of microcode that requires the large storage capacity. |
| Code Translation<br>Line Module<br>F2013-00 | Provides two code translation tables capable of one-for-one translation between two 8-bit or less codes and one code translation table and logic capable of translating baudot or Katakana codes. One feature can be shared by all CLCs in a system in enhanced mode. |
| Active Line<br>Indicator<br>F1825-05 | Provides a visual display of line activity on up to 16 communication line modules on a single CLC (F1932-00). Mounts on top of the DCP/40 cabinet containing the CLC. |
| Active Line<br>Indicator Switch<br>F3854-00 | Provides the ALI feature (F1825-05) with the capability to manually select one of the four sets of communications interfaces to be monitored when multiline line modules are configured. Mounts in F1825-05 which is required. |

(continued)

## Table 1-8. Distributed Communications Processor (DCP) Products (cont)

| Type/Feature | Description |
|---|---|
| Processor Assembly<br>F2940-00 | The processor assembly includes the DCP/40 processor card complement and back panel. The backpanel supports the processor, storage controller (F1929-00), up to four storage arrays (F1930-00), and a storage port expander (F1936-00). Also includes microprogram storage F2923-02, the processor maintenance panel which mounts inside the cabinet, and an operator's panel which mounts on the front edge of the cabinet top. Installs in 1945-00 for multiprocessor configurations. |
| Processor Assembly<br>F2940-01 | Includes the DCP/40 processor card complement and back panel. The back panel supports the processor, storage controller (F1929-01), up to four storage arrays (K1930-01) and a storage port expander (F1936-00). Also includes microprogram storage (F2923-02), the processor maintenance panel which resides inside the cabinet and an operator panel which mounts on the front edge of the cabinet top. Installs in 1945-00 for multiprocessor configurations. |
| CLC Power Expansion<br>F2941-00 | Provides power for second through fourth CLCs in an 8596 or 1945 cabinet, includes a heavy duty circuit breaker for that cabinet. |
| CLC Power Expansion<br>F2941-01 | Provides power for second through fourth CLCs in an 8596-02 and 1945-01 cabinet. Includes a heavy duty circuit breaker for the cabinet. |
| Storage Expansion<br>Backpanel<br>F2942-00 | Provides a storage-only backpanel with one storage controller and one 128K byte storage array card for mounting in a DCP/40 expansion cabinet (1945-00). One or two additional storage controllers (F1929-00) and up to 11 additional storage array cards (F1930-00) can be added. |
| Storage Expansion<br>Backpanel<br>F2942-01 | Provides a storage-only backpanel with one storage controller and one 512K byte storage array card for mounting in a DCP/40 expansion cabinet (1945-00). One additional storage controller (F1929-01) and up to seven additional storage array cards (F1930-01) can be added. |
| Direct Connect<br>Single Station<br>Line Module<br>F3847-00 | Provides an interface for up to 16 multidropped UTS 4000 direct connect single stations (DCSS). The line module is loaded with a microprogram for operation with data formats of UDLC protocol. It operates at 250K bits per second over a maximum distance of 5000 ft. The required coaxial cable is available with the UTS 4000 DCSS. To provide resiliency, two DCSS line modules may be connected to the coaxial cable. Only one DCP line module may be active at one time. Each feature includes one line module, a five-foot coaxial adapter cable, T-connector, and two terminators. |
| RS-232/V.24<br>Modem Cable<br>(2816358)<br>F8303-XX | Provides a cable to connect an RS-232-C/V.24 modem to F1941-00, F1942-00, F3163-00 or F3165-00.<br><br>F8303-00    4.6M    15ft<br>F8303-01    7.6M    25ft<br>F8303-02    12.2M    40ft<br>F8303-03    15.2M    50ft<br>F8303-04    1.8M    6ft |
| Direct Connect<br>Cable (2821423)<br>F8304-XX | Provides a cable for direct connection to an asynchronous terminal with an RS-232-C/V.24, V.28 interface. The terminal cable with its RS-232 connector is used with F8304-XX to provide a total length of up to 300 ft.<br><br>F8304-00    4.6M    15ft<br>F8304-01    7.6M    25ft<br>F8304-02    15.2M    50ft<br>F8304-03    30.5M    100ft<br>F8304-04    61.0M    200ft<br>F8304-05    76.3M    250ft |

(continued)

**Table 1-8. Distributed Communications Processor (DCP) Products (cont)**

| Type/Feature | Description |
|---|---|
| NTT Modem Cable (2824682) F8305-XX | Provides a cable to connect an NTT modem to F1941-00, F1942-00, F3163-00, or F3165-00. For use in Japan only.<br><br>F8305-00    4.0M    13.1ft<br>F8305-01    8.0M    26.2ft<br>F8305-02    12.0M    39.4ft<br>F8305-03    16.0M    52.5ft<br>F8305-04    30.5M    100.0ft |
| Trend Adapter Cable (2824178) F8306-XX | Provides a cable with connector pin 18 (Return to non-data mode) connected to the line module data signaling rate selector driver. Used to connect a trend telex adapter to the line module.<br><br>F8306-00    4.6M    15ft<br>F8306-01    7.6M    25ft<br>F8306-02    12.2M    40ft<br>F8306-03    15.2M    50ft |
| CCITT Test Loopback Cable (2826449) F8307-XX | Provides a cable to connect to a CCITT modem. The cable is similar to F8303-XX except it is wired according to ISO 2110-1980. This provides compatibility with late model V series modems including wires for the local loopback, remote loopback, and test indicator signals. Allows loopback support with the proper software, line module and modem.<br><br>F8307-00    4.0M    13.1ft<br>F8307-01    8.0M    26.2ft<br>F8307-02    12.0M    39.4ft<br>F8307-03    16.0M    52.5ft |
| X.21 Cable (2826034) F8308-XX | Provides a cable for connection to an X.21 standard DCE.<br><br>F8308-00    4.6M    15ft<br>F8308-01    7.6M    25ft<br>F8308-02    12.2M    40ft<br>F8308-03    15.2M    50ft<br>F8308-04    30.5M    100ft<br>F8308-05    45.7M    150ft<br>F8308-06    61.0M    200ft |
| Direct Connect Cable (2824690) F8244-00 | Provides a 50-foot cable for direct connection to a synchronous Unisys terminal or multiplexer through a U-100 junction box and an external cable. Cable lengths beyond the junction box must be limited to 4950 ft up to 4800 bps or 2450 ft at 9600 bps. |
| Direct Connect Cable (2824691) F8234-XX | Provides a cable with a connector which is suitable for direct connection to a synchronous Unisys terminal or terminal multiplexer.<br><br>F8234-00    4.0M    13.1ft<br>F8234-01    8.0M    26.2ft<br>F8234-02    12.0M    39.4ft<br>F8234-03    16.0M    52.5ft<br>F8234-04    30.5M    100.0ft |
| Bell 303 Modem Cable (2824870) F8311-XX | Provides a cable for direct connection to a Bell System 303 or equivalent modem.<br><br>F8311-00    4.6M    15ft<br>F8311-01    7.6M    25ft<br>F8311-02    12.2M    40ft<br>F8311-03    15.2M    50ft |

(continued)

## Table 1-8. Distributed Communications Processor (DCP) Products (cont)

| Type/Feature | Description |
|---|---|
| V.35 Modem Cable (2826033) F8312-XX | Provides a cable for connection to a CCITT recommendation V.35 standard DCE interface.<br><br>F8312-00 4.6M 15ft<br>F8312-01 7.6M 25ft<br>F8312-02 15.2M 50ft<br>F8312-03 24.4M 80ft<br>F8312-04 30.5M 100ft |
| Bell 801 Dialer Cable (2816359) F8313-XX | Provides a cable for connection to a Bell System 801 dialer or equivalent.<br><br>F8313-00 4.6M 15ft<br>F8313-01 7.6M 25ft<br>F8313-02 12.2M 40ft<br>F8313-03 15.2M 50ft |
| NTT Dialer Cable (6503402) F8314-XX | Provides a cable for connection to an NTT dialer. For use in Japan only.<br><br>F8314-00 5.0M 16.4ft<br>F8314-01 10.0M 32.8ft<br>F8314-02 20.0M 65.6ft<br>F8314-03 30.0M 98.4ft |
| Customer Provided Cable F8200-00 | This no-cost feature provides a way for the customer to indicate that he will provide his own cable. |
| Direct Connect Cable (Teflon) F8235-XX | Same cable as F8234-XX except cover is Teflon.<br><br>F8235-00 15.2M 50.0ft<br>F8235-01 4.0M 13.1ft<br>F8235-02 8.0M 26.2ft<br>F8235-03 12.0M 39.4ft<br>F8235-04 16.0M 52.5ft<br>F8235-05 30.5M 100.0ft |
| SCSI I/F Cable F8288-XX | Used to connect an 8441 mass storage cabinet.<br><br>F8288-00 0.9M 3ft<br>F8288-01 1.7M 5ft<br>F8288-02 3.5M 10ft<br>F8288-03 6.1M 20ft<br>F8288-04 9.0M 30ft<br>F8288-05 15.2M 50ft |
| RS232 Duplex F8290-XX | A PVC covered cable used to connect printers to terminals with duplex RS-232 peripheral interface.<br><br>F8290-00 0.9M 3ft<br>F8290-01 1.7M 5ft<br>F8290-02 3.5M 10ft<br>F8290-03 6.1M 20ft<br>F8290-04 9.0M 30ft<br>F8290-05 12.2M 40ft<br>F8290-06 15.2M 50ft<br>F8290-07* 3.5M 10ft<br>F8290-08* 9.0M 30ft<br>F8290-09* 15.2M 50ft<br>* Same as 02/04/06 except outer jacket is black for certain OEM requirements. |

### Table 1-9. Ancillary Products

| Type/Feature | Description |
|---|---|
| Channel Transfer Switch T2521-00 | Freestanding cabinet containing operator controls for manual switching of four SU00039 subsystem strings, a primary module with a 2 x 1 switch and with power and space for up to 4 x 8 switching. Operates on 60 Hz power. |
| Channel Transfer Switch T2521-01 | Same as T2521-00, except operates on 50 Hz power. |
| Peripheral Table F2919-00 | Table for system peripherals. Can be used for type T3560/3561/3612 workstations or T0719 card reader. |
| 2-By Switch Expansion F2600-00 | Provides expansion of a 2 x 1 by one subsystem string. A maximum of 3 can be used per T2521-00/01. Also, up to 3 can be used with F2601-00. |
| Primary Module 2-By Expansion F2601-00 | Adds a second 2 x 1 primary module and operator control for switching up to 4 additional subsystem strings. Provides expansion beyond 4 switchable subsystem strings, and provides for a fifth subsystem string. |
| Secondary Module 2-By Expansion F2601-01 | Provides a 2 x 1 secondary module for applications requiring independent 2-by switching capability when up to 4 switchable strings can be configured among independent 2-by switches preempts addition of F2602-00. |
| Secondary 4-By Module Expansion F2602-00 | Adds a secondary module expanding capability of a primary 2-by module from 2 to 4 channels. Further expansion beyond one subsystem string requires addition of F2603-00 for each string. A maximum of 3 F2603-00 are allowed with F2602-00. |
| 4-By Switch Expansion F2603-00 | Allows expansion of 4-by switching by one subsystem string. A maximum of 3 is allowed with each F2602-00, which are prerequisites for each F2603-00. |

This section describes the processor components of the System 80 models 8/10/15/20. Subsections 2.1 through 2.8 describe the processor of the model 8. Subsections 2.9 through 2.14 describe the processor of the models 10/15/20.

## 2.1. MODEL 8 PROCESSOR ELEMENTS

The basic elements of the model 8 processor are:

- Central processing unit (CPU)

- Main storage unit (MSU)

- System control processor (SCP)

- Channel controller (CHC)

- D-bus multiplexer channel (D MUX)

- Byte multiplexer channel

- Integrated selector channel (ISC)

## 2.2. MODEL 8 CENTRAL PROCESSING UNIT (CPU)

The central processing unit (CPU) is controlled by an 80-bit microprogram. The unit executes and controls instructions. It also processes interrupts such as input/output interrupts and interval timer interrupts, and provides the input/output status tabler.

The model 8 CPU has the following functions and characteristics:

- Microprogramming

- 256-word register stack

- 173 instructions (including firmware instructions)

- Address relocation

- 6 interrupt levels

- Interval timer

- Input/output status tabler

- Interpretation of instructions by the instruction buffer, and parallel processing of address calculations and execution

- Increased storage bus efficiency (using two storage ports)

- Parity check of all data buses

- Comparison checking by duplexing the principal operating sections

- Enhanced reliabililty by patrol during wait

### 2.2.1. CPU Registers

The CPU has a 256-word register stack. The register stack contains:

- General purpose registers

- Floating-point registers

- Working registers

- Control registers

- Snap registers

Table 2-1 shows the 256-word scratch memory that makes up the register stack.

## Table 2-1. Allocation of Scratch Memory

| Address (Hexadecimal) | Location |
|---|---|
| 00–07 | Shared system area |
| 08–1F | Instruction working register |
| 20–2F | MSU/ED logout area |
| 30–3F | Shared system area |
| 40–6F | CPU logout area |
| 70–7F | Spare |
| 80–8F | Supervisor general register |
| 90–9F | Control register |
| A0–AF | User general register |
| B0–BF | Snap register |
| C0–C7 | Floating-point register |
| C8–CF | AMC instruction area |
| D0–DF | Stack logout area |
| E0–EF | Instruction working register |
| F0–F7 | Spare |
| F8–FF | P-bus microtrap area |

## 2.2.2. General Registers

There are 32 general registers: 16 problem general registers and 16 supervisor general registers, in two sets. The size of each general register (Figure 2-1) is 32 bits (1 full word).
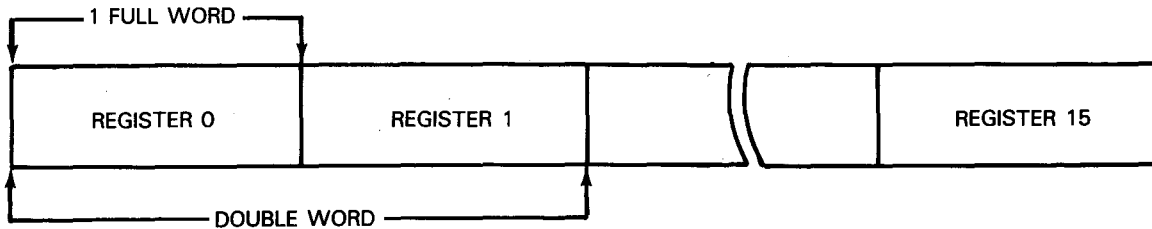


Figure 2-1. General Registers and Register Numbers

The CPU uses one set; either the problem or supervisor general registers, under control of the current program status word (PSW) problem register (PR) bits. Both sets of these general registers are used for indexing, fixed-point and logic operations, and for temporary storage. The registers have their own numbers which are designated to a 4-bit index, (B) basic, and a register field contained in CPU-executed command words.

When using two successive registers as a double-word operand (that is, as one register in an instruction word), the register number should always be an even number. Therefore, a register with an even number can be considered to represent the left half of a double word, and a register with an odd number represents the right half of the double word.

## 2.2.3. Floating-Point Registers

Four floating-point registers are available. Each floating-point register (Figure 2-2) is 64 bits (double word) long. This size permits them to be used for instructions in single-precision format (full word) as well as in double-precision format (double word). In single-precision format, bits 0 to 31 of the double-word registers are used, and the remaining 32 to 63 bits are ignored. The contents of the ignored 32 bits do not change, even after executing single-precision format commands.
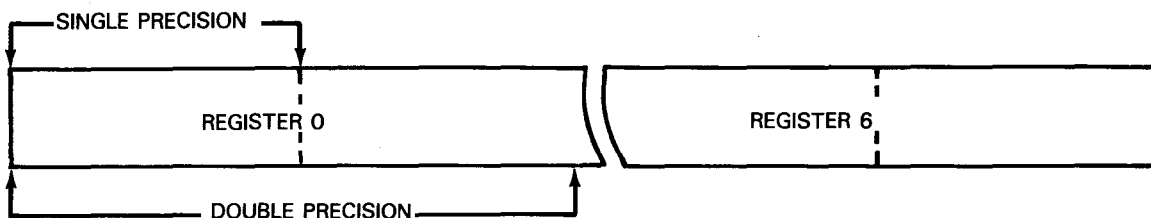


Figure 2-2. Floating-Point Registers and Register Numbers

Floating-point registers are designated by register numbers in 4-bit fields of CPU-executed command words. The operation code (OP code) of the command distinguishes between a general purpose register and a floating-point register. Floating-point registers are numbered 0, 2, 4, and 6, sequentially.

### 2.2.4. Working Registers

Each working register is 32 bits (full word) long. Working registers temporarily store operands and results when executing microinstructions. Because of these conditions, working registers cannot be used in programs.

### 2.2.5. Control Registers

There are 16 full word (32 bits) control registers. Individual control registers have their own intrinsic functions, such as system configuration, machine and channel control, and monitoring. Figure 2-3 shows control register allocations.
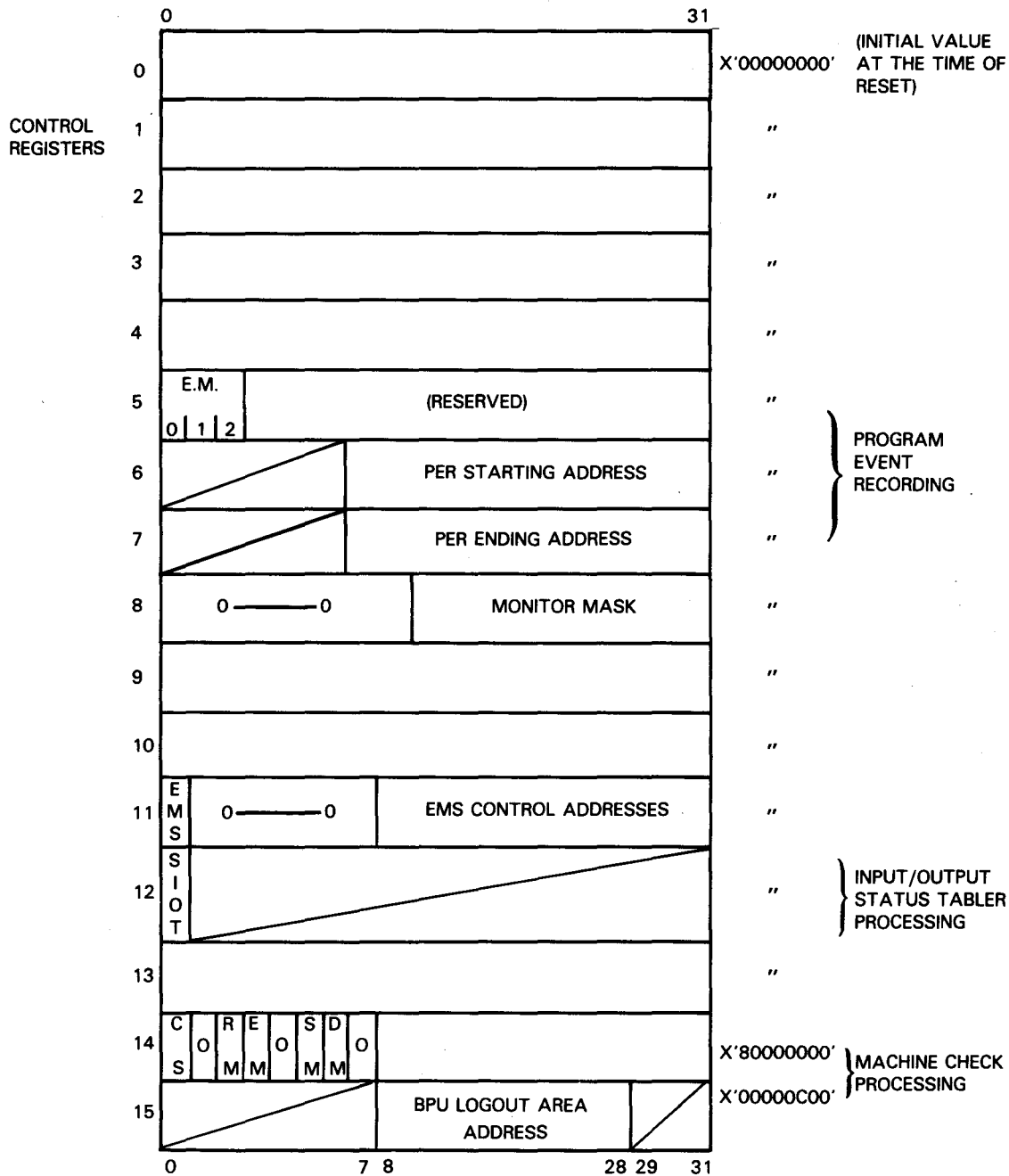
Figure 2-3. Control Register Allocations

LEGEND:

SIOT (SIO trace bit):    When 0 – SIO instruction trace is not performed.
                         When 1 – SIO instruction trace is performed.

EMS                      When 0 – The EMS-STOP state is set up.
                         When 1 – Control is transferred to an EMS control address.

## 2.2.6. Snap Registers

Snap registers save information required for processor maintenance. These registers are loaded by the CPU and are read by a diagnostic program. Figure 2-4 shows the snap register allocations.

| SNAP REGISTERS | 0 | | | 15 | 16 | | 31 | |
|---|---|---|---|---|---|---|---|---|
| 0 | '9 9' | | I2 | | B1 | D1 | | ...HPR COMMAND IMAGE |
| 1 | 0 | 0 | | (B1)+D1 | | | | ...HPR COMMAND OPERAND ADDRESS |
| 2 | | | PSWU | | | | | ...PSW UPPER WORD DURING HPR COMMAND |
| 3 | | | PSWL | | | | | ...PSW LOWER WORD DURING HPR COMMAND |
| 4 | 0 | 0 | L | LAST BRANCH ADDRESS | | | | |
| 5 | 0 | 0 | I | LAST LPSW ADDRESS | | | | |
| 6 | 0 CHC IOP | DVA | CC | 00 | 0 | 0 | 0 | ...LAST SIO (EXCLUDING IOST (DVA=DEVICE ADDRESS) |
| 7 | IT CODE | 0 | 0 | 0 | 0 | IT ADDRESS | | ...LAST IT |
| 8 | 0 | 0 | 0 | 0 | 0 | 0 | 2-ND IT-CODE | ITC FOR INTERRUPT OF PROGRAM EXCEPTION ...ITEM THAT CAUSED PEX MACHINE CHECK INTERRUPT |
| 9 | | | | | | | | |
| 10 | | | | | | | | |
| 11 | | | | | | | | |
| 12 | | | | | | | | (RESERVED) |
| 13 | | | | | | | | |
| 14 | | | | | | | | |
| 15 | | | | | | | | |

Figure 2-4. Snap Register Allocations

## 2.3. MODEL 8 MAIN STORAGE UNIT (MSU)

The main storage unit (MSU) stores commands and data. The basic storage capacity of the MSU is 1 megabyte (MB). It can be expanded in units of one MB up to eight MBs.

The error check and correction (ECC) function automatically corrects 1-bit errors and reports errors of more than 2 bits. Key memories for 6 bits x 512 (for 1 MB) and for 6 bits x 4096 (for 8 MBs) are maintained for storage protection.

Table 2-2 lists the MSU characteristics.

### Table 2-2. MSU Characteristics

| Parameter | Characteristics |
|---|---|
| Memory Blocks | 1,048,576 bytes (1 MB) (minimum) |
| | 2,097,152 bytes (2 MB) |
| | 3,145,728 bytes (3 MB) |
| | 4,194,304 bytes (4 MB) |
| | 6,291,456 bytes (6 MB) |
| | 8,388,608 bytes (8 MB) (maximum) |
| Cycle Time | Four system clock cycles for reading and writing for each 8 bytes (double words) |
| Operating Mode | Nondestructive reading |
| Memory Data Bus | Eight bytes, including one parity bit for each byte is available. Parity bits are supplied to detect errors in the data pass line. |
| Error Checking and Correction (ECC) | Data in main storage consists of 64 bits (8 bytes) of data and an 8-bit ECC code. The ECC code permits a 1-bit error correction and detection of errors larger than two bits. |
| Checking | Storage protection checking is performed. Checking is for write storage protection, or write/read operations. |

### 2.3.1. Addressing MSU

The CPU contains a 24-bit address function capable of addressing up to 16,777,216 bytes.

When reading, main storage transfers eight bytes of information to the CPU or the input/output channel, which selects a specific byte designated in the lower three address bits. When writing, data is written in units of eight bytes, unless partial writing is required.

When the addressing function of the CPU exceeds the storage capacity, an address exception item is generated and a machine check interrupt is raised.

Figure 2-5 illustrates the addressing function.
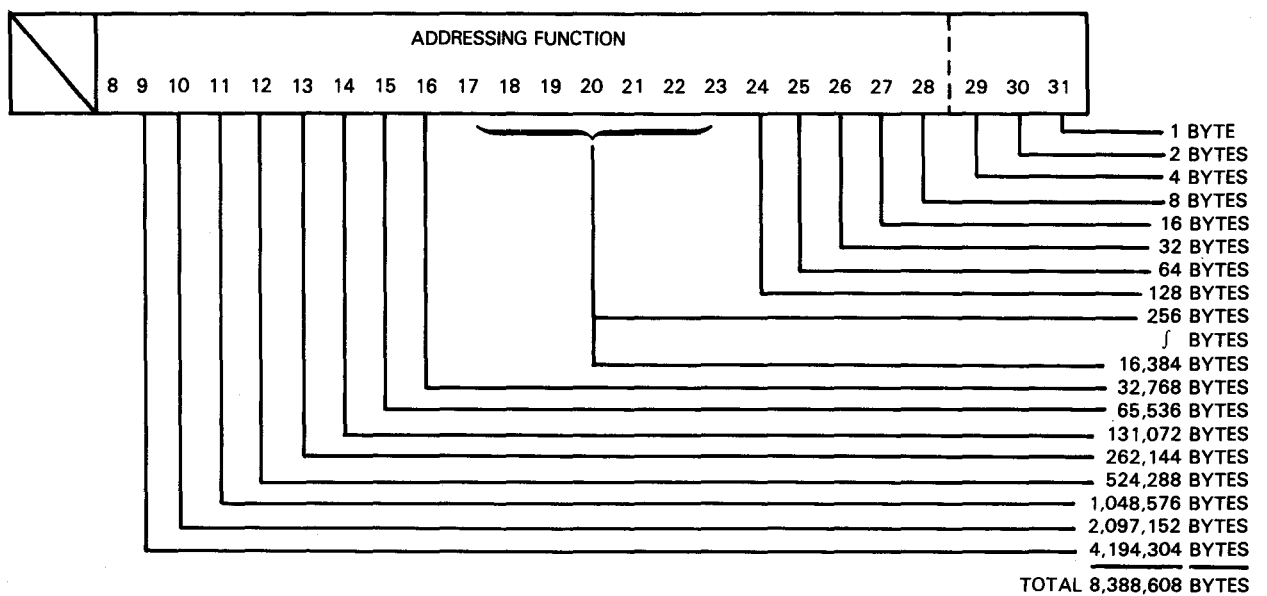


**Figure 2-5. Addressing Function**

### 2.3.2. Main Storage Unit Data Boundary

The main storage data boundary varies depending on the length of the information. Generally, the boundary is on a byte multiple equal to the number of bytes in the information format.

For example:

■    A half-word uses a 2-byte boundary.

■    A full-word uses a 4-byte boundary.

■    A double-word uses an 8-byte boundary.

### 2.3.3. Partial Writing Function

This main storage function allows writing one to eight bytes during a data-write operation. Main storage uses eight mark lines which are CPU or channel supplied with the main storage address.

Each bit corresponds to a byte in the subsequent data transfer. A mark bit equal to 1 allows that byte to be written to memory. When the mark bit is equal to 0, the associated byte in memory retains its original contents.

For example:

Loc 1000 = 123456789ABCDEF0

Execute write with mark bits = E0, data = 112233FFFFFFFFFF

New contents of 1000 are = 112233789ABCDEF0

### 2.3.4. MSU Priority

The MSU and MSU interface are shared by the CPU and I/O channels. Table 2-3 lists the priority for accessing the MSU.

**Table 2-3. MSU Priorities**

| Priority | System Components |
|----------|-------------------|
| 1 | Channel control unit 0 – CHC 0 |
| 2 | Channel control unit 1 – CHC 1 |
| 3 | M bus adapter - MBA |
| 4 | Basic processing unit or input/output status tabler (IOST) |

NOTE:

The byte multiplexer is subpriority to CHC 0, to which it is attached.

### 2.3.5. Storage Protection

Storage protection ensures the safety of supervisor and individual user programs in main storage. Up to 64 programs, including supervisors, are protected.

Contents of main storage are protected from data destruction or erroneous operation when more than one program is being processed. Storage protection is available in units of 2048 bytes (2K) for writing and writing/reading. The CPU and channel control unit provide storage protection for the storage unit reference.

## 2.4. MODEL 8 SYSTEM CONTROL PROCESSOR (SCP)

The system control processor (SCP) is an independent processor that performs basic functions for system operations.

It consists of two sections:

■    A service processor (SVP)

■    A system function section (SF)

Figure 2-6 shows a block diagram of the SCP components.
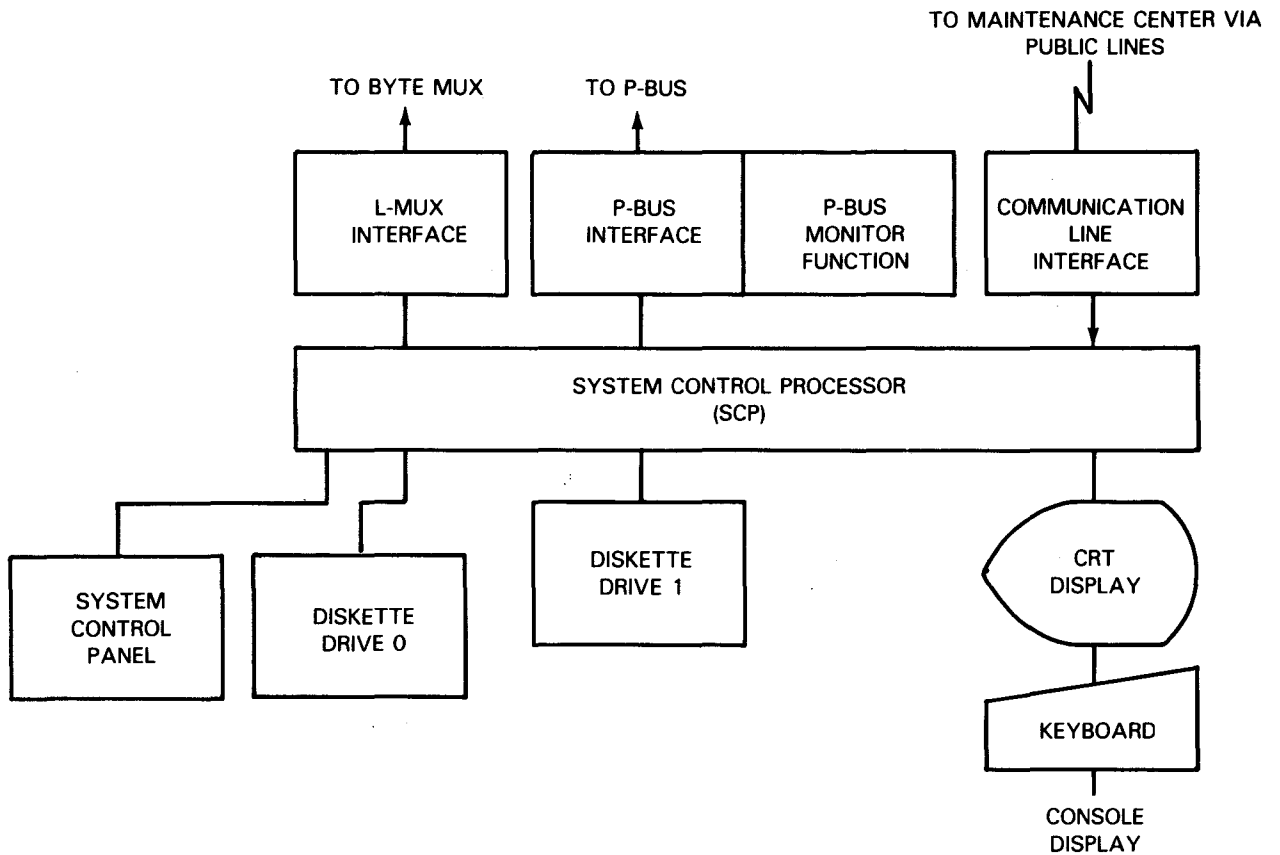
Figure 2-6.  System Control Processing Components

### 2.4.1. Service Processor (SVP)

The service processor (SVP) functions as a maintance panel for each processor and as a console workstation for operator interface.

The major components of the SVP are:

- Byte multiplexer and P-bus interfaces that in turn provide interfaces to mainframe system units and the operating system

- System control panel including switches to turn power on and off and indicator lamps to display system abnormalities

- Console display used for operator interaction

- Console diskette drive to store:

  - CPU and SCP microprograms
  - Diagnostic programs
  - Error information when a system fault occurs
  - IOMP microcode

- Communications line interface connecting to the maintenance center through public telephone lines

### 2.4.2. System Function (SF) Section

The major components of the SF section are:

- M-bus clock generator that generates the system clock and timing to individual processors. The system clock value is 125 ns (+/- 1 ns).

- Time-of-day clock (TOD) storing time with a period up to 143 years. This value is written by the STCK (store clock) and SCK (set clock) instructions.

- Address stop to maintain the CPU in a stop state when it or the channel control unit refers to an absolute address in the MSU. The absolute address is set up by the manual frame.

## 2.5. MODEL 8 CHANNEL CONTROLLER (CHC)

The channel controller (CHC) provides common control of the channel interface section. The CHC connects to the M- and P-buses on one side and the byte multiplexer and integrated selector channels on the other.

The CHC performs functions such as:

- M-bus/P-bus control

- Data buffering

- Channel control

Two CHCs can be configured in a single model 8 system. Each CHC controls up to four channels.

## 2.6. MODEL 8 D-BUS MULTIPLEXER CHANNEL (D MUX)

The D-bus multiplexer channel (D MUX) consists of:

- An M-bus adapter (MBA)

- One or two input/output microprocessors (IOMP)

The IOMP provides the channel connection for the System 80 D-bus controllers (workstations, diskettes, paper peripherals, and tapes) and communications adapters.

The D MUX has an aggregate data rate of 1 MB.

## 2.7. MODEL 8 BYTE MULTIPLEXER CHANNEL

The byte multiplexer channel connects to relatively low-speed input/output devices. It controls up to four subchannels and six controllers. The byte adapter and system console interface connect to the byte multiplexer.

The byte multiplexer has a data transfer rate of up to 70 kilobytes per second. It is controlled by a 16-bit x 3K microprogram.

Only one byte multiplexer can connect to the first CHC.

## 2.8. MODEL 8 INTEGRATED SELECTOR CHANNEL (ISC)

The integrated selector channel (ISC) connects to relatively high-speed input/output devices such as magnetic disk and magnetic tape drives. Because the ISC is operated in selector mode, only one device can operate with the ISC at one time.

The ISC has a data transfer rate of up to 1.5 MB.

As many as three ISCs can connect to the first CHC. One or two ISCs can connect to a second CHC.

## 2.9. MODELS 10/15/20 PROCESSOR ELEMENTS

The basic elements of the models 10/15/20 processor are:

- Basic processing unit (BPU)

- Main storage unit (MSU)

- System control processor (SCP)

- D-bus multiplexer channel (D MUX)

- Selector channel (SEL)

## 2.10. MODELS 10/15/20 BASIC PROCESSING UNIT (BPU)

The basic processing unit (BPU) is controlled by an 80-bit microprogram. The unit executes and controls instructions. It also processes interrupts such as input/output interrupts and interval timer interrupts, and provides the input/output status tabler.

The models 10/15/20 BPU has the following functions and characteristics:

- Microprogramming

- Register stack

- 168 instructions (including firmware instructions)

- Address relocation

- 6 interrupt levels

- Interval timer

- Input/output status tabler

- Parity check of most data buses

- Comparison checking by duplexing the principal operating sections

- Enhanced reliabililty by patrol check during wait state

- Pipeline control

- Micro accelerator (model 15 only)

- Cache memory for instructions (model 20 only)

- Cache memory for operands (model 20 only)

- Floating point processor (model 20 only)

### 2.10.1. BPU Registers

The BPU has a register stack that contains:

- General purpose registers

- Floating-point registers

- Working registers

- Control registers

- Snap registers

### 2.10.2. General Registers

There are 32 general registers: 16 problem general registers and 16 supervisor general registers, in two sets. The size of each general register (Figure 2-7) is 32 bits (1 full word).
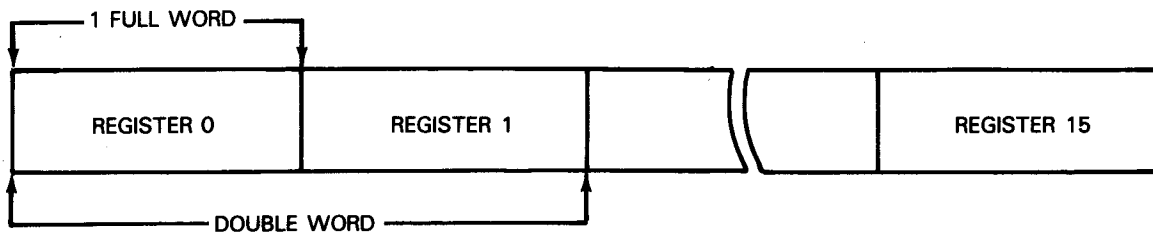


Figure 2-7. General Registers and Register Numbers

The BPU uses one set; either the problem or supervisor general registers, under control of the current program status word (PSW) problem register (PR) bits. Both sets of these general registers are used for indexing, fixed-point and logic operations, and for temporary storage. The registers have their own numbers which are designated to a 4-bit index, (B) base, and a register field contained in BPU-executed command words.

When using two successive registers as a double-word operand (that is, as one register in an instruction word), the register number should always be an even number. Therefore, a register with an even number can be considered to represent the left half of a double word, and a register with an odd number represents the right half of the double word.

### 2.10.3. Floating-Point Registers

Four floating-point registers are available. Each floating-point register (Figure 2-8) is 64 bits (double word) long. This size permits them to be used for instructions in single-precision format (full word) as well as in double-precision format (double word). In single-precision format, bits 0 to 31 of the double-word registers are used, and the remaining 32 to 63 bits are ignored. The contents of the ignored 32 bits do not change, even after executing single-precision format commands.

SINGLE PRECISION

REGISTER 0

REGISTER 6

DOUBLE PRECISION
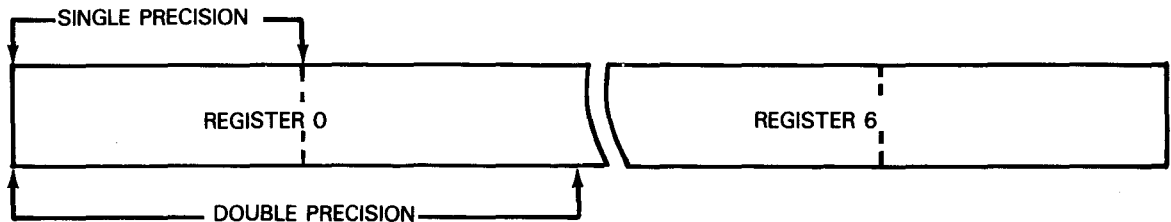
**Figure 2-8. Floating-Point Registers and Register Numbers**

Floating-point registers are designated by register numbers in 4-bit fields of BPU-executed command words. The operation code (OP code) of the command distinguishes between a general purpose register and a floating-point register. Floating-point registers are numbered 0, 2, 4, and 6, sequentially.

### 2.10.4. Working Registers

Each working register is 32 bits (full word) long. Working registers temporarily store operands and results when executing microinstructions. Because of these conditions, working registers cannot be used in programs.

### 2.10.5. Control Registers

There are 16 full word (32 bits) control registers. Individual control registers have their own intrinsic functions, such as system configuration, machine and channel check control, and monitoring. Figure 2-9 shows control register allocations.
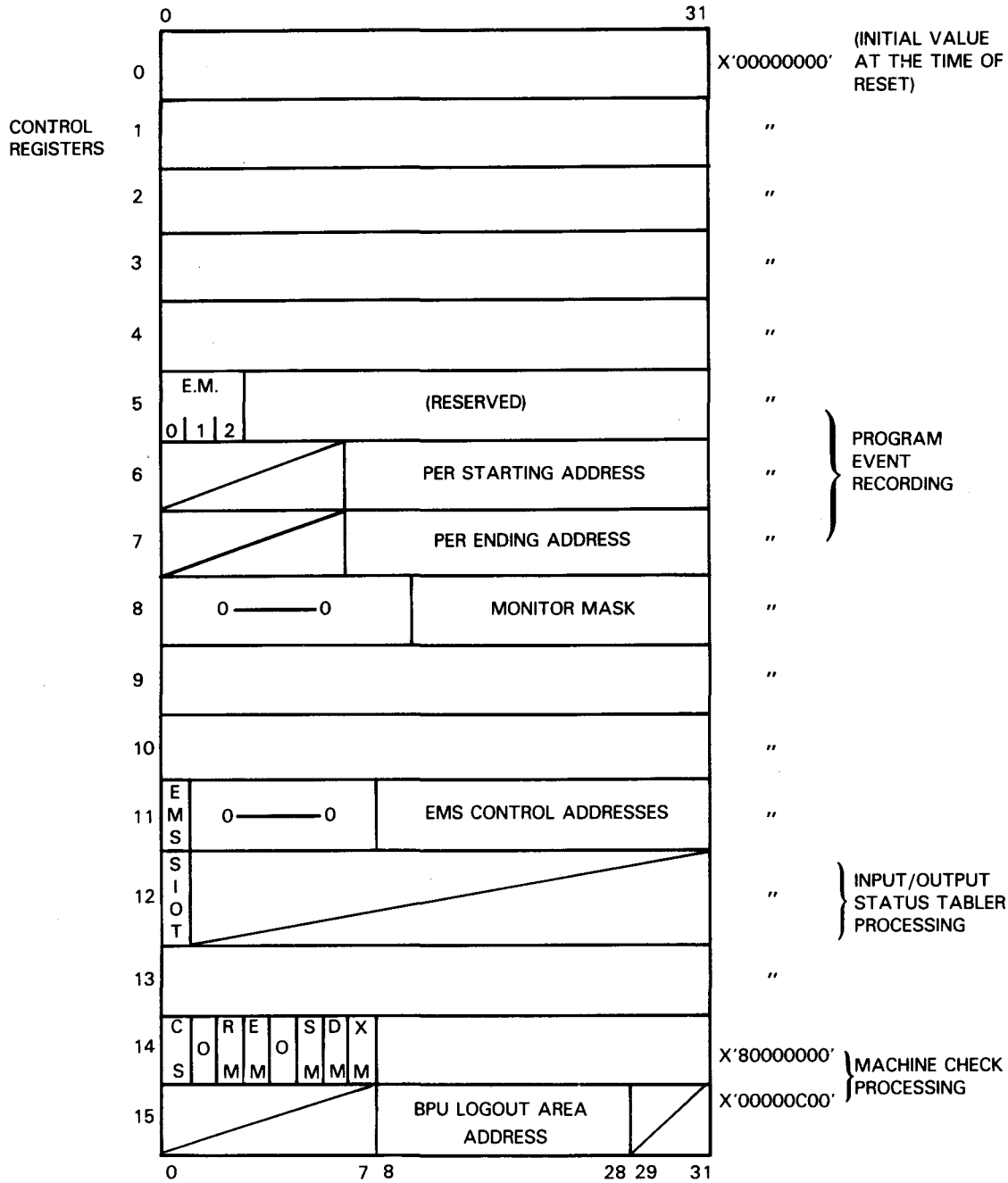
Figure 2-9. Control Register Allocations

LEGEND:

SIOT (SIO trace bit):    When 0 – SIO instruction trace is not performed.
                         When 1 – SIO instruction trace is performed.

EMS                      When 0 – The EMS-STOP state is set up.
                         When 1 – Control is transferred to an EMS control address.

## 2.10.6. Snap Registers

Snap registers save information required for processor maintenance. These registers are loaded by the BPU and are read by a program. Figure 2-10 shows the snap register allocations.
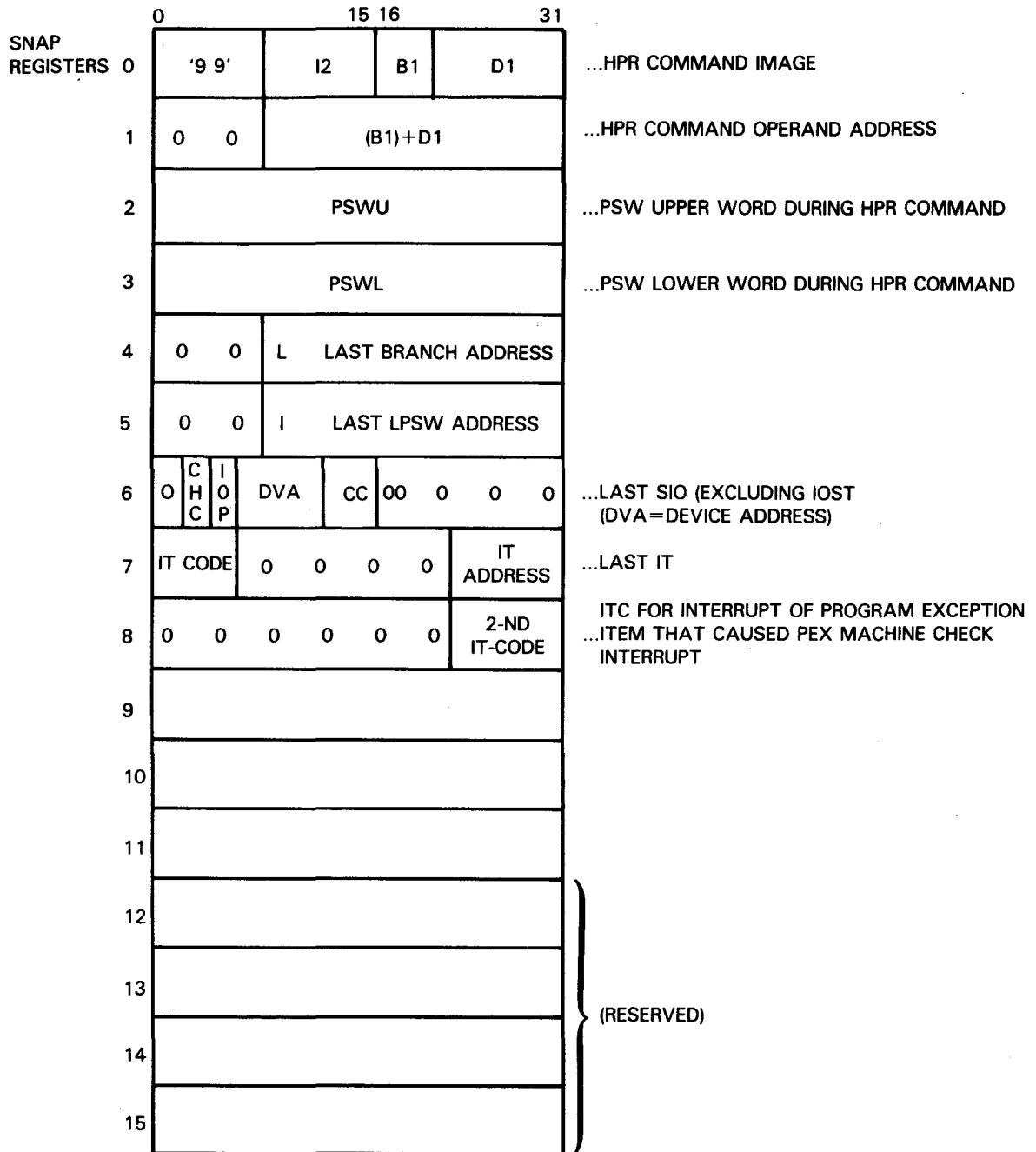


Figure 2-10. Snap Register Allocations

## 2.11. MODELS 10/15/20 MAIN STORAGE UNIT (MSU)

The main storage unit (MSU) stores programs, commands, and data. The MSU comprises a memory control unit (MCU) and one or more basic memory units. The basic storage capacity of the MSU is:

■   2 megabytes (MB) for the model 10

■   4 MB for the models 15 and 20

Storage capacity can be expanded for the models 10/15/20 up to 8 MB, 12 MB, and 16 MB respectively.

The error check and correction (ECC) function automatically corrects 1-bit errors and reports errors of more than 2 bits. Key memories for 8 bits x 512 (for 2 MB) and for 8 bits x 4096 (for 16 MBs) are maintained for storage protection.

Table 2-4 lists the MSU characteristics.

### Table 2-4. MSU Characteristics

| Parameter | Characteristics |
|---|---|
| Memory Blocks | 2,097,152 bytes (2 MB) (minimum) <br><br> 4,194,304 bytes (4 MB) <br><br> 6,291,456 bytes (6 MB) <br><br> 8,388,608 bytes (8 MB) <br><br> 12,582,912 bytes (12 MB) <br><br> 16,777,216 bytes (16 MB) (maximum) |
| Cycle Time | Bytes Transmitted   Read Cycle   Write Cycle <br>   Times   Times <br><br> 4    5 clocks   4 clocks <br> 8    6 clocks   5 clocks <br> 12    7 clocks   6 clocks <br> 16    8 clocks   7 clocks <br><br> Note: One S-bus clock equals 100 nanoseconds. |
| Operating Mode | Nondestructive reading |
| Memory Data Bus | Thirty-two bits including four parity bits are available. Parity bits are supplied to detect errors in the data pass line. |
| Error Checking and Correction (ECC) | Data in main storage consists of 32 bits (4 bytes) of data and a 7-bit ECC code. The ECC code permits a 1-bit error correction and detection of errors larger than two bits. |
| Checking | Storage protection checking is performed. Checking is for store protection, or store/fetch protection. |

### 2.11.1. Addressing MSU

The BPU contains a 24-bit address function capable of addressing up to 16,777,216 bytes (Figure 2-11).

When the addressing function of the BPU exceeds the storage capacity, an address exception item is generated and a machine check interrupt is raised.
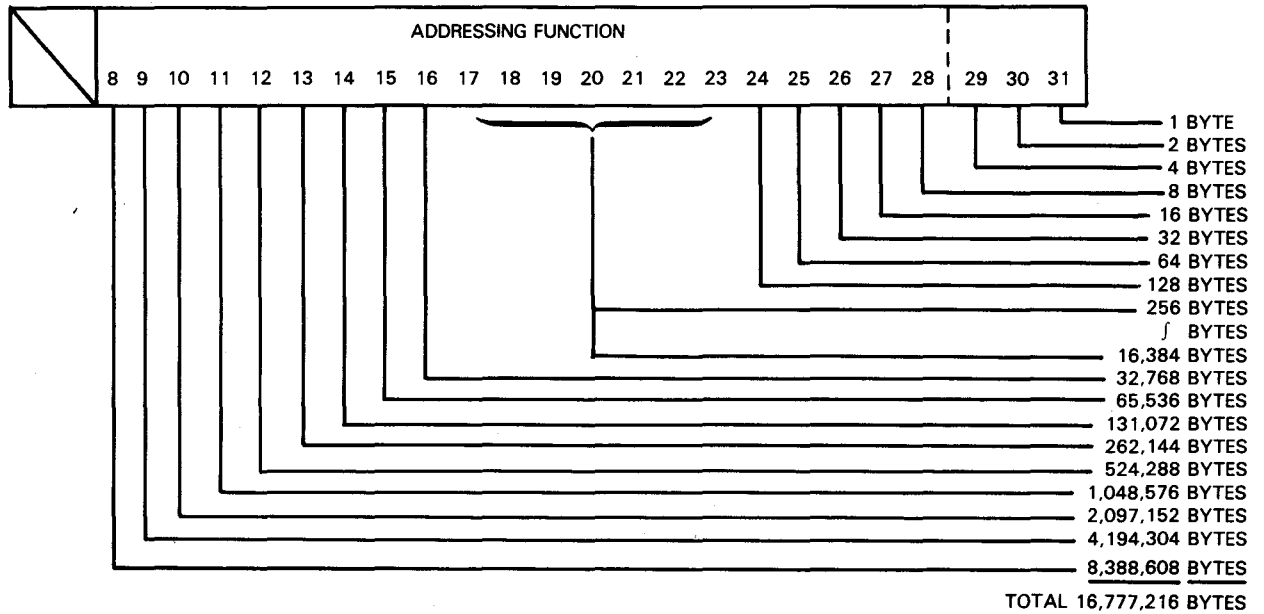


**Figure 2-11. Addressing Function**

### 2.11.2. Main Storage Unit Data Boundary

The main storage data boundary varies depending on the length of the information. Generally, the boundary is on a byte multiple equal to the number of bytes in the information format.

For example:

■ A half-word uses a 2-byte boundary.

■ A full-word uses a 4-byte boundary.

■ A double-word uses an 8-byte boundary.

### 2.11.3. Partial Writing Function

This main storage function allows writing one to four bytes during a data-write operation. Main storage uses four mark lines that are supplied with the main storage address by the BPU or channel control unit.

Each bit corresponds to a byte in the subsequent data transfer. A mark bit equal to 1 allows that byte to be written to memory. When the mark bit is equal to 0, the associated byte in memory retains its original contents.

### 2.11.4. MSU Priority

The MSU and MSU interface are shared by the BPU and channel control units. Table 2-5 lists the priority for accessing the MSU.

**Table 2-5. MSU Priorities**

| Priority | System Components |
|----------|-------------------|
| 1 | Selector channel 1 – SEL1 |
| 2 | Selector channel 2 – SEL2 |
| 3 | Selector channel 3 – SEL3 |
| 4 | Selector channel 4 – SEL4 |
| 5 | Input/Output processor – IOP |
| 6 | Selector channel 5 – SEL5 |
| 7 | Selector channel 6 – SEL6 |
| 8 | Service processor – SVP |
| 9 | Basic processing unit – BPU |

### 2.11.5. Storage Protection

Storage protection ensures the safety of supervisor and individual user programs in main storage. Up to 64 programs, including supervisors, are protected.

Contents of main storage are protected from data destruction or erroneous operation in both single and multiprocessing environments. Storage protection is available in units of 4096 bytes (4K) for writing and writing/reading. The BPU and channel control unit provide storage protection for the storage unit reference.

### 2.12. MODELS 10/15/20 SYSTEM CONTROL PROCESSOR (SCP)

The system control processor (SCP) is an independent processor that performs basic functions for system operations.

The functional component of the SCP is the service processor (SVP). The SVP functions as a maintance panel for each processor and as a console workstation for operator interface.

The major components of the SVP are:

- L-bus interface that in turn provides an interfaces to mainframe system units and the operating system

- System control panel including switches to turn power on and off and indicator lamps to display system abnormalities

- Master console display used for operator interaction

- Diskette drives to store:

  - BPU and SVP microprograms
  - Diagnostic programs
  - Error information when a system fault occurs

- Communications line interface connecting to the maintenance center through public telephone lines

Figure 2-12 shows the componets of the SCP.

TO MAINTENANCE CENTER VIA
PUBLIC LINES

TO S-BUS          TO L-BUS

```
┌──────────┐   ┌──────────┐ ┌──────────┐   ┌──────────────┐
│  S-BUS   │   │  L-BUS   │ │  L-BUS   │   │COMMUNICATION │
│INTERFACE │   │INTERFACE │ │ MONITOR  │   │    LINE      │
│          │   │          │ │ FUNCTION │   │  INTERFACE   │
└──────────┘   └──────────┘ └──────────┘   └──────────────┘

┌──────────────────────────────────────────────────────┐
│            SYSTEM CONTROL PROCESSOR                    │
│                    (SCP)                               │
└──────────────────────────────────────────────────────┘

┌─────────┐ ┌─────────┐   ┌─────────┐        ╭─────────╮
│ SYSTEM  │ │ DISKETTE│   │ DISKETTE│        │   CRT   │
│ CONTROL │ │ DRIVE 0 │   │ DRIVE 1 │        │ DISPLAY │
│  PANEL  │ │         │   │         │        ╰─────────╯
└─────────┘ └─────────┘   └─────────┘        ┌─────────┐
                                             │KEYBOARD │
                                             └─────────┘
```

MASTER CONSOLE
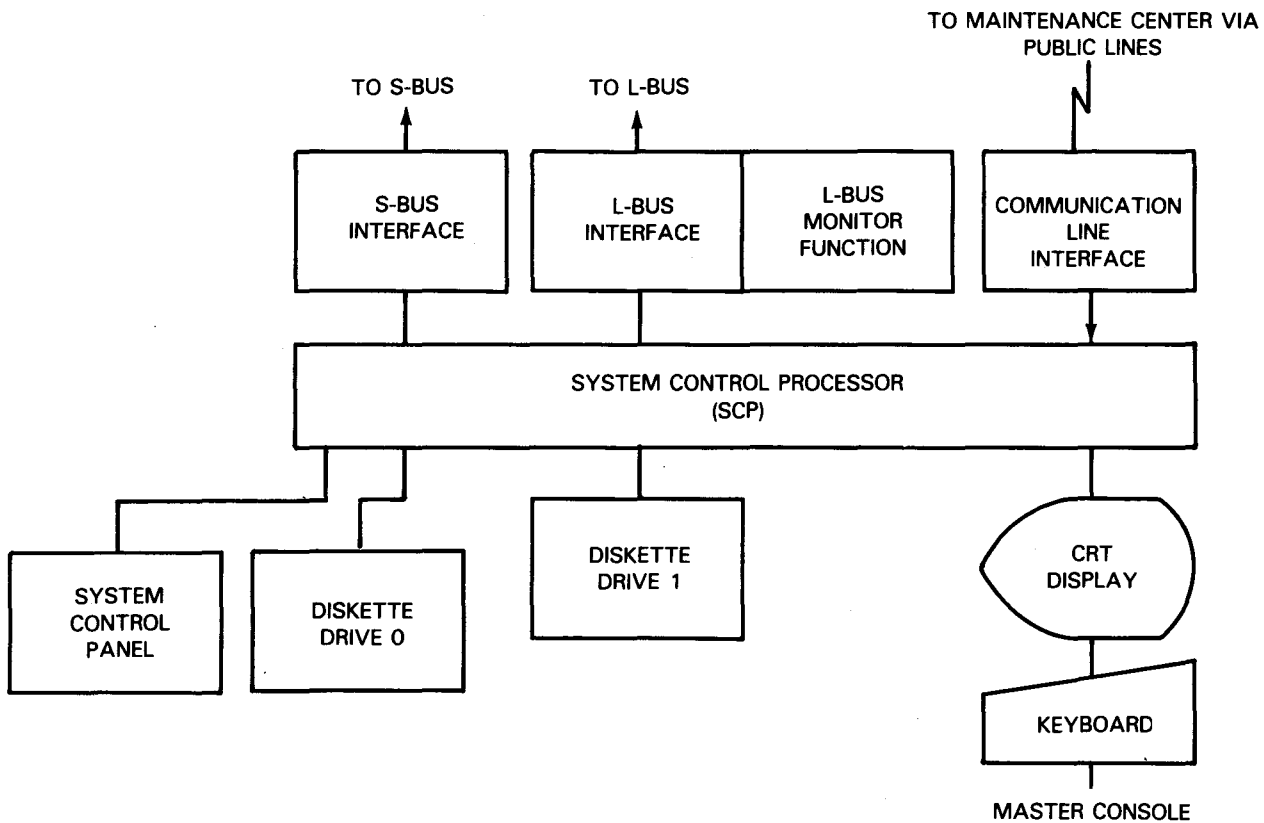
Figure 2-12.  System Control Processing Components

## 2.13.  MODELS 10/15/20 D-BUS MULTIPLEXER CHANNEL (D MUX)

The D-bus multiplexer channel (D MUX) consists of:

■   A mainframe interface adapter (MIA)

■   One or two input/output processors (IOP)

The IOP provides the channel connection for the System 80 D-bus controllers (including workstations, paper peripherals, flexible diskette, and tapes) and communications adapters.

The D MUX has an aggregate data rate of 1 MB.

## 2.14.  MODELS 10/15/20 SELECTOR CHANNEL (SEL)

The selector channel (SEL) connects to relatively high-speed input/output devices such as magnetic disk and magnetic tape drives.

The SEL has a data transfer rate of up to 2.1 MB.

As many as six SELs can connect to a single model 10, 15, or 20 system.

# 3. Operations Control

## 3.1. DATA AND INSTRUCTION FORMATS

### 3.1.1. Information Format

Data and instructions are transferred as information in lengths of 1, 2, 3, or more bytes, with 8 bits (1 byte) per unit. On the model 8, up to 8 bytes of information is transferred in parallel between the MSU and CPU, or between the MSU and input/output channel. On the models 10/15/20, up to 16 bytes are transferred on a single memory access.

Bytes are handled one by one, or in a batch as one field. One half word is a field two continuous bytes long. A double word is a field comprising two words.

Figure 3-1 shows the information format.
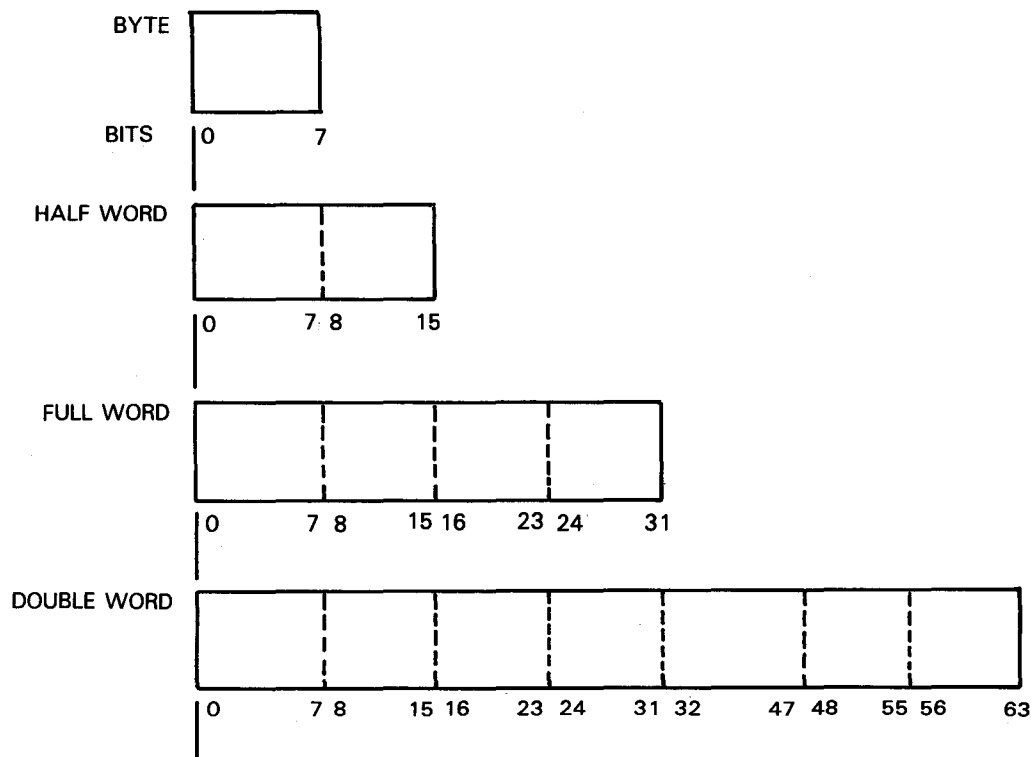


Figure 3-1. Information Format

### 3.1.2. Address Designation Format

Locations of individual bytes in main storage are numbered sequentially beginning with 0. These numbers correspond to the individual information bytes that enter the MSU. When using a series of bytes or one field, reference is made by designating the address of the byte at the left end of the byte group or field.

The number of bytes handled by one field is either:

- Already decided by the operation to be executed

- Designated as part of the instruction

The variable-length operand, in an instruction, is a field that can change the operand length in a byte unit.

### 3.1.3. Information Positioning

Fixed-length fields such as half, full, and double words must be positioned inside the MSU on like boundaries. The boundary for this information is complete when the address is a multiple of the number of bytes that make up the information.

For example, the address of a full word (4 bytes long) in main storage is a multiple of 4. Similarly, multiples of 2 are used for half words (2 bytes) and multiples of 8 are used for double words (8 bytes long).

Addresses in main storage are shown by binary numbers in the processing unit. The complete boundaries for half, full, and double words are shown by binary number, and the bits of the address lower digits are 0, 00, and 000, respectively.

### 3.1.4. Data Format and Operation Processing

The processing unit handles data of various types for:

- Fixed-point numbers

- Floating-point numbers

- Decimal numbers

- Logic information processing

**Fixed-Point Numbers**

Fixed-point numbers are in three formats:

- Half word

- Full word

- Double word

The first bit of fixed-point numbers indicates a code. The remaining bits are integers. When the code bit is 1, the numeral is negative. A negative is expressed in 2s complement form.

Fixed-point operations are performed using the 32 general purpose registers in the processing unit. Fixed-point numbers in the 32 general purpose registers are normally handled as an operand of 32 bits. When half-word numerals are transferred from main storage to general purpose registers, the code bits are expanded towards the left. The bits are generally handled as a full-word operand.

A double-word operand is used in:

■    Multiplication and division instructions of fixed point operations

■    Shift instructions

In this instance, double-word numerals use two general purpose registers which are a pair for even and odd numbers. Addresses of general purpose registers are even numbered. Numerals of the fixed points of half, full, and double words in main storage must be placed at the boundary addresses for information positioning.

Figure 3-2 shows the format of fixed-point numbers.
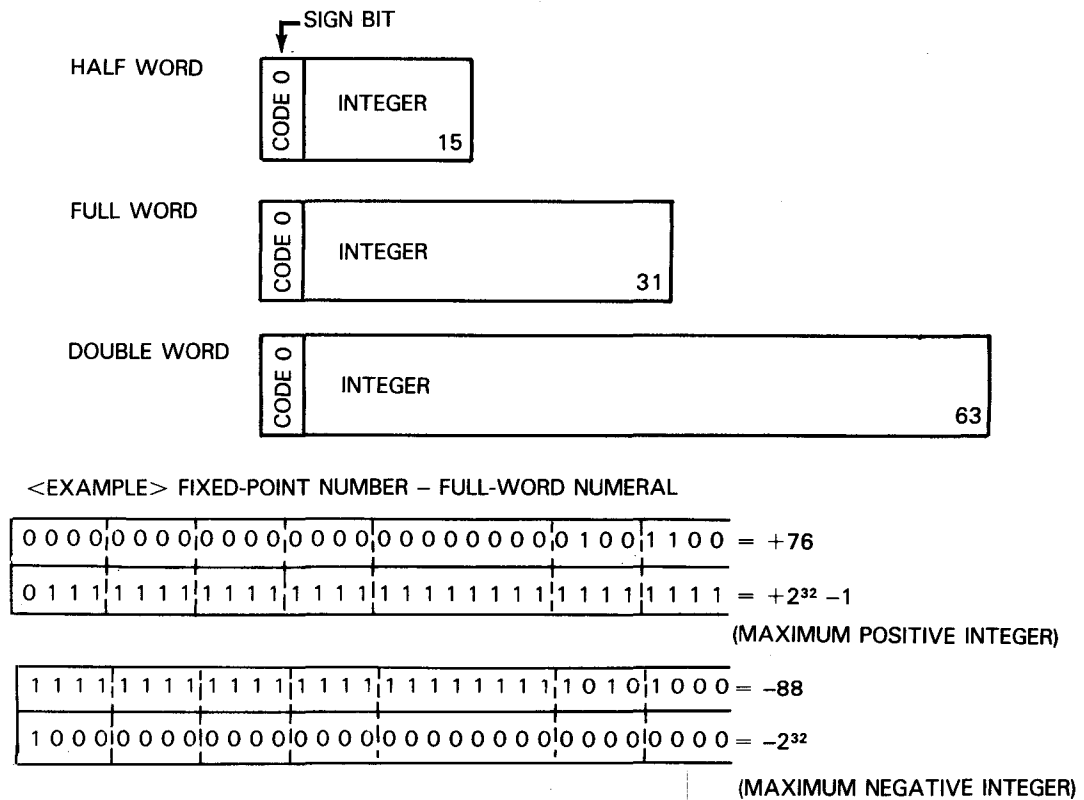


Figure 3-2. Fixed-Point Number Format

## Floating-Point Numbers

Floating-point operations use data lengths in two formats:

- Full word (single precision)

- Double word (double precision)

Both of these formats use floating-point registers in main storage or in the processing unit.

A floating-point number consists of exponent and mantissa sections. The exponent section is expressed by a binary number with 64 added as a bias. The mantissa section is expressed by a hexadecimal number with a decimal point at the left of the uppermost column. The overall value of a floating-point numeral is calculated by raising the numeral, which is obtained by subtracting 64 from the exponent section, to the power of 16. The value of the floating-point number is this product of the numeral and the mantissa.

In both single- and double-precision formats, bit location 0 expresses the code of the mantissa section. Bits 1 to 7 constitute the exponent section. The code is positive when 0 is shown, and negative when 1 is shown. In single precision, bits 8 to 31 are used as the mantissa section. In double precision, bits 8 to 63 are used as the mantissa section.

In floating-point operation instructions, the following are possible:

- Loading to registers for single and double precision

- Storing results of additions, subtractions, divisions, and multiplications

- Code control

In single precision, operating speeds are high and main storage can have a small capacity. However, operation precision is increased with double precision.

Generally, floating-point operations are executed on normalized floating-point numerals (called standard floating-point numbers). In multiplications and divisions, calculaltions are performed on standard floating-point numbers before operation (prenormalization). The results are converted into standard floating-point numbers (postnormalization).

In additions and subtractions, floating-point numbers that are not normalized (called nonstandard floating-point numbers) are also handled. The highest digit (hexadecimal) in the mantissa section of standard floating numerals cannot be 0. Normalizing shifts the mantissa section to the left until the highest digit is no longer 0, and deducts the number of shifts from the exponent section. Normalizing cannot occur when the exponent section is 0.

In order to increase precision, calculations are made to one or more digits as an intermediate result. These are made in single precision for model 8. They are made in single and double precision for models 10/15/20.

This calculation is done when executing instructions for:

- Additions

- Subtractions

- Bisection operations

- Comparisons

- Multiplications of floating-point numerals
  in standard and nonstandard form

This extra digit for precision is called the guard digit.

Figure 3-3 shows the format for floating-point numbers.

SINGLE PRECISION FLOATING-POINT NUMERAL



DOUBLE PRECISION FLOATING-POINT NUMERAL
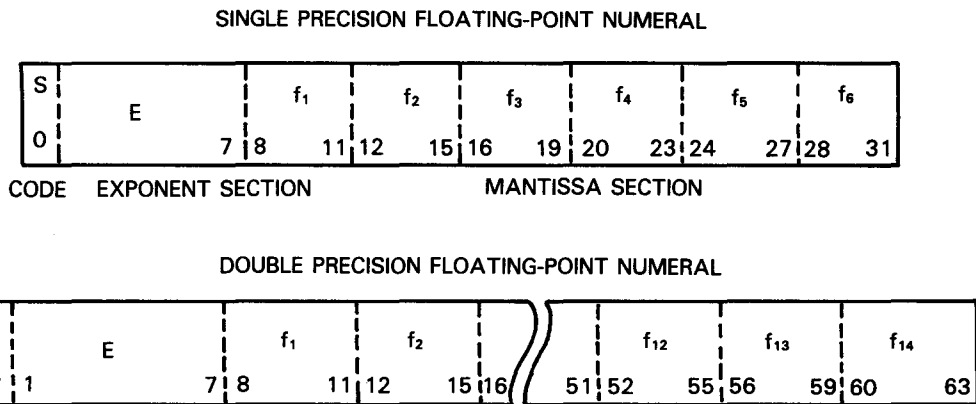


Figure 3-3. Floating-Point Number Format

## Decimal Numbers

Data for decimal number operations has variable lengths. Two format types are used: packed and unpacked. Additions, subtractions, multiplications, and divisions are executed only on data in the packed format. A command to convert decimal numbers in unpacked format into packed format is available.

Bits 0 to 3, in a byte of an unpacked format decimal number, constitute a zone and 1111 is entered into it. Bits 4 to 7 show numeric characters from 0 to 9 in binary decimal numbers. The lowest byte zone is expressed in decimal number code.

For decimal numbers in packed format, two digits each of numeric characters expressed by binary decimal numbers are placed in one byte. However, bits 4 to 7 of the lowest byte show the decimal number code.

Decimal number codes have six combinations:

| Sign | Binary Number |
|------|---------------|
| * + | 1100 |
| * - | 1101 |
| + | 1010 |
| + | 1110 |
| + | 1111 |
| - | 1011 |

The asterisk (*) is a code the processing unit marks on the results of operations.

Figure 3-4 shows the format for decimal numbers.

DECIMAL NUMBERS IN UNPACKED FORMAT
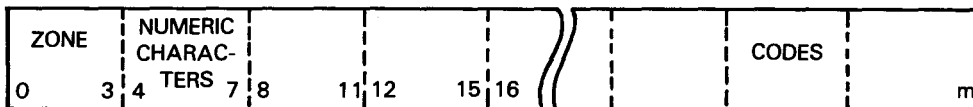


DECIMAL NUMBERS IN PACKED FORMAT
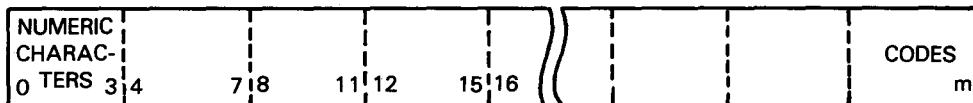


Figure 3-4.  Decimal Number Format

## Logical Operation Data _____

Commands are available for logical operations such as:

■    Comparison

■    Code conversion

■    Edit

■    Bit shifting

■    Bit check

Fixed- and variable-length data are handled in logical operations. Fixed-length data has either 1 or 4 bytes and is processed in general purpose registers. Variable-length data of up to 256 bytes can be processed.

Figure 3-5 shows the format for logical operation data.

FIXED-LENGTH DATA

```
           +-----------------+
BYTE       |     BYTE 0      |
           |                 |
           |0               7|
           +-----------------+
```

```
       +---------+---------+---------+---------+
WORD   | BYTE 0  | BYTE 1  | BYTE 2  | BYTE 3  |
       |0       7|8      15|16     23|24     31|
       +---------+---------+---------+---------+
```

VARIABLE-LENGTH DATA

```
       +---------+---------+---------+---------+
       | BYTE 0  | BYTE 1  | BYTE 2  | BYTE 3  |
       |0       7|8      15|         |2040 2047|
       +---------+---------+---------+---------+
```
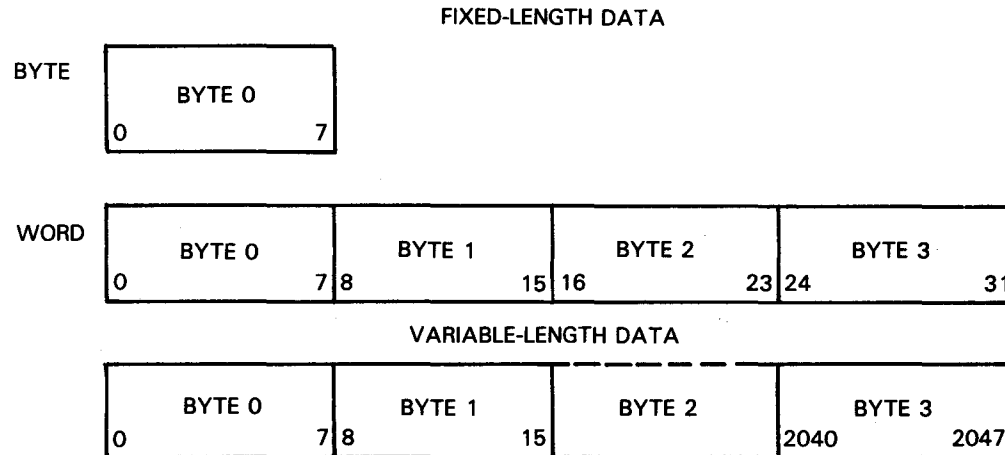
Figure 3-5.  Logical Operation Data Format

### 3.1.5.  Instruction Formats

There are five types of instruction formats used in the processing unit:

■    Register to register  (RR)

■    Register to index storage  (RX)

■    Register to storage  (RS)

■    Storage and immediate operand (SI)

■    Storage to storage  (SS)

Instruction lengths are in 2, 4, or 6 bytes. These instructions must be placed in locations starting with even numbered addresses in main storage.

Figure 3-6 illustrates the instruction formats.
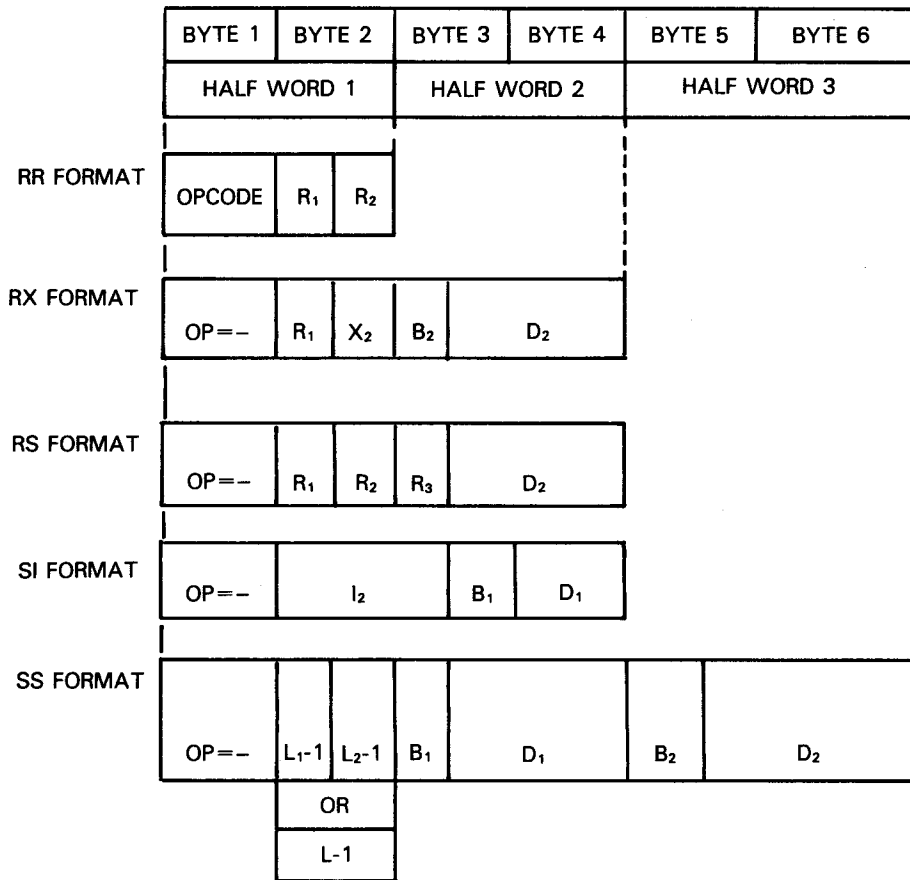


Figure 3-6. Instruction Formats

## Address Generation

An address expressed by an instruction in main storage is determined by the sum of a combination of four components:

1.  B field  (base register)

2.  X2 field  (index register)

3.  D field  (displacement)

4.  Current relocation register  (hardware register)

The B field designates the base address and specifies the designation of any address. The number in the lower 24 bits of the general register designated by the B field of the instruction is the base address. When designation of the B field is 0, the base address is given as 0, regardless of the content of the general register 0.

The X2 field is a component created only by an instruction in RX format. The X2 field is the number in the lower 24 bits of the general register. This field is called an index. When the designation of the X2 field is 0, the address components are given as 0, regardless of the content of general register 0.

The D field is called displacement and is a number in 12 bits contained in the instruction format. This numeral is used in all address calculations.

When producing addresses, base addresses and indexes are handled as positive integers of 24 bits without a code. Displacement is also handled as a positive integer of 12 bits. These three components are added and become a 24-bit binary number.

The value of offset expressed by 24 bits in the current relocation register is added to the hardware. Addresses in main storage are determined by the sum of these four components. These addresses consist of 24 bits. The values of bits 21 to 31 of the current relocation registers are added as 0, and upper overflow is ignored when it occurs.

The final address (absolute address of main storage) is used to:

- Refer to main storage

- Check addressing exception and storage protection exception items

Figure 3-7 shows the absolute address of main storage.

```
BITS 8      21          31

      X X X X X X X X X X X X X X X X X X X X X X X X   =   (B)*

      X X X X X X X X X X X X X X X X X X X X X X X X   =   (X₂)**

      0 0 0 0 0 0 0 0 0 0 0 0 X X X X X X X X X X X X   =   D

  +   X X X X X X X X X X X X X 0 0 0 0 0 0 0 0 0 0 0   =   OFFSET
```

NOTE:

Bits 0 to 7 are ignored.

* (B) expresses the contents of the general purpose registers designated by the B field.

** (X₂) is used only in the RX format.

**Figure 3-7.  Absolute Address of Main Storage**

RR format instructions process data contained in the general purpose registers. These instructions can process:

- A double word maximum data length

- Fixed-point numbers

- Floating-point numbers

- Decimal numbers

RR format instructions are a half word long.

Figure 3-8 shows the RR format.

```
+------------------------+-----------+------------+
|        OP CODE         |  R₁/M₁    |     R₁     |
| 0                    7 | 8     11  | 12      15 |
+------------------------+-----------+------------+
                         |                        |
                         +------------------------+
                         |           I₂           |
                         | 8                   15 |
                         +------------------------+
```

NOTE:

In this instruction format, the same register number can be designated for operands 1 and 2. In some instances, $R_2$ is not used.

LEGEND:

$R_1$ (Bits 8 to 11)
   General register number or floating-point register number designated by operand 1. $M_1$ is designated for a branch instruction. This is a mask.

$R_2$ (Bits 12 to 15)
   General register number or floating-point register number designated by operand 2.

$I_2$ (Bits 8 to 15)
   Shows immediate data of 1 byte.

**Figure 3-8. RR Format**

## RX Format

RX format instructions process data, qualified by an index register, between general registers and main storage.

These instructions can process:

■    A double word maximum data length

■    Fixed-point numbers

■    Floating-point numbers

■    Decimal numbers

RX format instructions are two half words long.

Figure 3-9 shows the RX format.

| OP CODE | $R_1/M_1$ | $X_2$ | $B_2$ | $D_2$ |
|---|---|---|---|---|
| 0          7 | 8       11 | 12     15 | 16       19 | 20                              31 |

LEGEND:

$R_1/M_1$ (Bits 8 to 11)

    General register number or floating-point register number designated by operand 1. $M_1$ is designated in the case of the branching instruction. This represents a mask.

$X_2$ (Bits 12 to 15)

    General register number to give the value of the operand 2 index. When $X_2 = 0$, the index value is 0.

$B_2$ (Bits 16 to 19)

    General register number used to express the operand 2 base address. The base address is 0 when $B_2 = 0$.

$D_2$ (Bits 20 to 31)

    Displacement relative to operand 2.

**Figure 3-9.   RX Format**

## RS Format

RS format instructions:

- Transfer data between registers and main storage

- Shift data.

RS format instructions are two half words long.

Figure 3-10 shows the RS format.

| OP CODE | | R₁ | | R₃ | | B₂ | | D₂ | |
|---|---|---|---|---|---|---|---|---|---|

| OP CODE | R₁ | R₃ | B₂ | D₂ |
|---|---|---|---|---|
| 0      7 | 8     11 | 12     15 | 16     19 | 20                         31 |

LEGEND:

R₁ (Bits 8 to 11)

    General register number designated by operand 1. Alternatively, it is used to designate the head of the boundary of the general purpose register.

R₃ (Bits 12 to 15)

    General register number designated by operand 3. Alternatively, it is used to designate the end of the boundary of the general register.

    This section is not used in a shift instruction.

B₂ (Bits 16 to 19)

    General register number used to express the base address of operand 2.

    The base address is 0 when $B_2 = 0$.

D₂ (Bits 20 to 31)

    Displacement relative to operand 2. In a shift instruction, the value shown in operand 2 shows the number of digits to be shifted.

**Figure 3-10.  RS Format**

## SI Format

SI format instructions execute operations between an 8-bit (1 byte) value (called immediate data) and main storage. SI format instructions are two half words long.

Figure 3-11 shows the SI format.

| OP CODE | | $I_2$ | | $B_1$ | | $D_1$ | |
|---|---|---|---|---|---|---|---|
| 0 | 7 | 8 | 15 | 16 | 19 | 20 | 31 |

LEGEND:

$I_2$ (Bits 8 to 15)

   Expresses immediate data or mask of operand 2.

$B_1$ (Bits 16 to 19)

   General register number used to express the base address for operand 1. The base address is 0 when $B_1$ = 0.

$D_1$ (Bits 20 to 31)

   Displacement relative to operand 1. Operand 1 is used to designate the channel number and equipment number for an input/output instruction.

**Figure 3-11.  SI Format**

## SS Format

SS format instructions execute operations between two operands in main storage. In a logic operation, the operand lengths are assumed to be equal. Their lengths can be 1 to 256 bytes. In decimal operations, operand lengths can be different. Their lengths can be 1 to 16 bytes.

SS format instructions are three half words long.

Figure 3-12 shows the SS format.

LEGEND:

When the OP code (operation code) is an instruction that can be shown by 'FX' (X = 0 to F: hexadecimal number) of a hexadecimal number:

$L_1 - 1$ (Bits 8 to 11)

    Length of operand 1 − 1

$L_2 - 1$ (Bits 12 to 15)

    Length of operand 2 − 1

When the OP code is an instruction, that can be shown by 'DX' (X = 0 to F: hexadecimal number) of a hexadecimal number.

$L - 1$ (Bits 8 to 15)

    Operation is performed assuming the lengths of operands 1 and 2 are equal. Designation of these lengths show the numbers of bytes of data starting with the operand addresses. In TR, TRT, ED, and EDMK instructions, merely the numbers of bytes of data starting with the address of operand 1 are shown.

$B_1$ (Bits 16 to 19)

    General register number used to express the operand 1 base address.

    When $B_1 = 0$, the base address is 0.

$D_1$ (Bits 20 to 31)

    Displacement relative to operand 1.

$B_2$ (Bits 32 to 35)

    General register number used to express the operand 2 base address. The base address is 0 when $B_2 = 0$.

$D_2$ (Bits 36 to 47)

    Displacement relative to operand 2.

**Figure 3-12.  SS Format**

### 3.1.6. Instruction Types

Instructions can be classified depending on the status of the processing unit as either:

- Privileged

- Nonprivileged

**Privileged Instructions** _____

Privileged instructions are executed by the processing unit on a special priority basis. The processing unit must be in supervisor mode to execute privileged instructions.

The processing unit mode is switched by changing the status of the current program status word in the hardware.

The user mode, called problem mode, is switched to the supervisor mode when:

- A supervisor call (SVC) instruction is executed, or

- An interrupt is generated.

All instructions in the system can be used when the processing unit is in supervisor mode.

**Nonprivileged Instructions** _____

Nonprivileged instructions are executed by the processing unit to process ordinary data in problem mode.

Privileged instructions cannot be executed when the processing unit is in problem mode. If the processing unit tries to calculate a privileged instruction when in problem mode:

- Program exception occurs

- An interrupt is generated

The processing unit is switched from supervisor mode to problem mode by executing the load PSW instruction (LPSW). This is a privileged instruction, so the processing unit must be in supervisor mode to execute the LPSW.

**Instruction Word Repertoire** _____

There are:

- General instructions (Table 3-1)

- Floating-point instructions (Table 3-2)

- Decimal instructions (Table 3-3)

- Privileged control and I/O instructions (Table 3-4).

## Table 3-1. General Instruction Set

| Instruction Code | Mnemonic | Type | Op |
|---|---|---|---|
| Add register | AR | RR | 1A |
| Add | A | RX | 5A |
| Add half-word | AH | RX | 4A |
| Add immediate | AI | SI | 9A |
| Add logical | ALR | RR | 1E |
| Add logical | AL | RX | 5E |
| And register | NR | RR | 14 |
| And | N | RX | 54 |
| And immediate | NI | SI | 94 |
| And character | NC | SS | D4 |
| | | | |
| Branch and link | BALR | RR | 05 |
| Branch and link | BAL | RX | 45 |
| Branch on condition | BCR | RR | 07 |
| Branch on condition | BC | RX | 47 |
| Branch on count | BCTR | RR | 06 |
| Branch on count | BCT | RX | 46 |
| Branch on index high | BXH | RS | 86 |
| Branch on index low or equal | BXLE | RX | 87 |
| | | | |
| Compare register | CR | RR | 19 |
| Compare | C | RX | 59 |
| Compare and swap under mask | CSM | RS | 89 |
| Compare half-word | CH | RX | 49 |
| Compare logical | CLR | RR | 15 |
| Compare logical | CL | RX | 55 |
| Compare logical immediate | CLI | SI | 95 |
| Compare logical character | CLC | SS | D5 |
| Compare logical character under mask | CLM | RS | BD |
| Compare logical immediate and skip | CLIS | SS | E1 |
| Compare logical character long | CLCL | RR | 0F |
| Convert to binary | CVB | RX | 4F |
| Convert to decimal | CVD | RX | 4E |
| | | | |
| Divide register | DR | RR | 1D |
| Divide | D | RX | 5D |
| Exclusive OR | XR | RR | 17 |
| Exclusive OR | X | RX | 57 |
| Exclusive OR immediate | XI | SI | 97 |
| Exclusive OR character | XC | SS | D7 |
| Execute | EX | RX | 44 |
| | | | |
| Insert character | IC | RX | 43 |
| Insert characters under mask | ICM | RS | BF |
| | | | |
| Load register | LR | RR | 18 |
| Load | L | RX | 58 |
| Load address | LA | RX | 41 |
| Load and test | LTR | RR | 12 |
| Load complement | LCR | RR | 13 |
| Load half-word | LH | RX | 48 |
| Load multiple | LM | RS | 98 |
| Load negative | LNR | RR | 11 |
| Load positive | LPR | RR | 10 |

(continued)

## Table 3-1. General Instruction Set (cont)

| Instruction Code | Mnemonic | Type | Op |
|---|---|---|---|
| Monitor call | MC | SI | AF |
| Move immediate | MVI | SI | 92 |
| Move character | MVC | SS | D2 |
| Move long | MVCL | RR | 0E |
| Move numerics | MVN | SS | D1 |
| Move with offset | MVO | SS | F1 |
| Move zones | MVZ | SS | D3 |
| Multiply register | MR | RR | 1C |
| Multiply | M | RX | 5C |
| Multiply half-word | MH | RX | 4C |
| | | | |
| OR | OR | RR | 16 |
| OR | O | RX | 56 |
| OR immediate | OI | SI | 96 |
| OR character | OC | SS | D6 |
| | | | |
| Pack | PACK | SS | F2 |
| | | | |
| Set program mask | SPM | RR | 04 |
| Shift left double | SLDA | RS | 8F |
| Shift left double logical | SLDL | RS | 8D |
| Shift left single | SLA | RS | 8B |
| Shift left single logical | SLL | RS | 89 |
| Shift logical | SHL | RS | 9B |
| Shift right double | SRDA | RS | 8E |
| Shift right double logical | SRDL | RS | 8C |
| Shift right single | SRA | RS | 8A |
| Shift right single logical | SRL | RS | 88 |
| Store | ST | RX | 50 |
| Store character | STC | RX | 42 |
| Store character under mask | STCM | RS | BE |
| Store clock | STCK | SI | B205 |
| Store half-word | STH | RX | 40 |
| Store multiple | STM | RX | 90 |
| Subtract register | SR | RR | 1B |
| Subtract | S | RX | 5B |
| Subtract half-word | SH | RX | 4B |
| Subtract logical | SLR | RR | 1F |
| Subtract logical | SL | RX | 5F |
| Supervisor call | SVC | RR | 0A |
| | | | |
| Test and set | RA | SI | 93 |
| Test under mask | TM | SI | 91 |
| Test under mask and skip | TMS | SS | E2 |
| Translate | TR | SS | DC |
| Translate and test | TRT | SS | DD |
| | | | |
| Unpack | UNPK | SS | F3 |

## Table 3-2. Floating-Point Instructions

| Instruction Code | Mnemonic | Type | Op Code |
|---|---|---|---|
| Add normalized (long) | AD | RX | 6A |
| Add normalized (long) | ADR | RR | 2A |
| Add normalized (short) | AE | RX | 7A |
| Add normalized (short) | AER | RR | 3A |
| Add unnormalized (long) | AW | RX | 6E |
| Add unnormalized (long) | AWR | RR | 2E |
| Add unnormalized (short) | AU | RX | 7E |
| Add unnormalized (short) | AUR | RR | 3E |
| | | | |
| Compare (long) | CD | RX | 69 |
| Compare (long) | CDR | RR | 29 |
| Compare (short) | CE | RX | 79 |
| Compare (short) | CER | RR | 39 |
| | | | |
| Divide (long) | DD | RX | 6D |
| Divide (long) | DR | RR | 2D |
| Divide (short) | DE | RX | 7D |
| Divide (short) | DER | RR | 3D |
| Halve (long) | HDR | RR | 24 |
| Halve (short) | HER | RR | 34 |
| | | | |
| Load (long) | LD | RX | 68 |
| Load (long) | LDR | RR | 28 |
| Load (short) | LE | RX | 78 |
| Load (short) | LER | RR | 38 |
| Load and test (long) | LTDR | RR | 22 |
| Load and test (short) | LTER | RR | 32 |
| Load complement (long) | LCDR | RR | 23 |
| Load complement (short) | LCER | TT | 33 |
| Load negative (long) | LNDR | RR | 21 |
| Load negative (short) | LNER | RR | 31 |
| Load positive (long) | LKPR | RR | 20 |
| Load positive (short) | LPER | RR | 30 |
| | | | |
| Multiply (long) | MD | RX | 6C |
| Multiply (long) | MUR | RR | 2C |
| Multiply (short) | ME | RX | 7C |
| Multiply (short) | MER | RR | 3C |
| | | | |
| Store (long) | STD | RX | 60 |
| Store (short) | STE | RX | 70 |
| Subtract normalized (long) | SD | RX | 6B |
| Subtract normalized (long) | SDR | RR | 2B |
| Subtract normalized (short) | SE | RX | 7B |
| Subtract normalized (short) | SER | RR | 3B |
| Subtract unnormalized (long) | SW | RX | 6F |
| Subtract unnormalized (long) | SWR | RR | 2F |
| Subtract unnormalized (short) | SU | RX | 7F |
| Subtract unnormalized (short) | SUR | RR | 3F |

## Table 3-3. Decimal Instructions

| Instruction Code | Mnemonic | Type | Op Code |
|---|---|---|---|
| Add decimal | AP | SS | FA |
| Compare decimal | CP | SS | F9 |
| Divide decimal | DP | SS | FD |
| Edit | ED | SS | DE |
| Edit and mark | EDMK | SS | DF |
| Multiply decimal | MP | SS | FC |
| Shift and round decimal | SRP | SS | FO |
| Subtract decimal | SP | SS | FB |
| Zero and add | ZAP | SS | F8 |

## Table 3-4. Privileged System Control and I/O Instructions

| Instruction | Mnemonic | Type | Op Code |
|---|---|---|---|
| Activate machine check | AMC | SI | 8313 |
| Emergency stop | EMS | SI | 8417 |
| Halt and proceed | HPR | SI | 99 |
| Halt I/O | HIO | SI | 9E |
| Insert storage key | ISK | RR | 09 |
| Load control register | LCTL | RS | B7 |
| Load control store (model 8 only) | LCS | RS | B1 |
| Load PSW | LPSW | S | 82 |
| Longitudinal redudancy check | LRC | S | 830E |
| Read/write sense switch | RSS/WSS | SI | 8316 |
| Reset degradation (model 8 only)/ | RDG/DGC | SI | 8311 |
| Degradation control (models 10/15/20 only) | | | |
| Reset I/O | RIO | SI | 9F |
| Service timer register | STR | RR | 03 |
| Set clock | SCK | SI | B204 |
| Set/reset prioritized | SPIDL | SI | 831C |
| Interrupt device list (model 8 only) | RPIDL | – | – |
| Set storage key | SSK | RR | 08 |
| Set system mask | SSM | SI | 80 |
| Start I/O | SIO | SI | 9C |
| Store control register | STCTL | RS | B6 |
| Store CPU ID | STILDP | SI | B202 |
| Store snap register | STNR | SI | 8315 |
| Store status (model 8 only) | STS | S | 8302 |
| Store UCW (model 8 only) | STUCW | SI | 8314 |
| Supervisor load multiple | SLM | RS | B8 |
| Supervisor store multiple | SSTM | RS | BO |
| Switch list scan | SWLS | S | 830F |
| Translate CCW relative | TCAR | SI | 831D |
| From/to absolute (model 8 only) | TCRA | – | – |

## 3.2. PROCESSING UNIT STATES

There are four processing unit states:

- Stop (STOP)

  In STOP state:

  - The stop-state indicator (STOP) on the system console is lit.

  - Instruction execution, interrupt processing, and input/output status tabler processing are not performed.

  - Data can be transferred between the input/ouput devices and the MSU.

  - The program status word (PSW) and other functions of the processing unit can be changed by means of the console display.

  - The contents of the MSU can be displayed or changed by means of the console display.

- Waiting (WAIT)

  In WAIT state:

  - The PSW wait bit is set to 1.

  - The WAIT indicator on the system console is lit.

  - No instructions are executed.

  - Interrupt processing and I/O status tabler are performed.

- Run (RUN)

  In RUN state:

  - The PSW bit is not set to 1.

  - The RUN indicator on the system console is lit.

  - The charging meter on the model 8 system console operates.

- Check stop (C-STOP)

  In C-STOP state:

  - A machine check condition occurs or a system operation cannot continue due to a machine fault.

  - The C-STOP indicator on the system console is lit.

WAITING and RUN are collectively called operating states. In an operating state, instruction execution, interrupt processing, and I/O status tabler processing are performed:

- According to the internal instruction information, or

- As designated at the console display.

### 3.2.1. Changing Processor Unit States

A change from stop state to an operating state occurs when:

- Start operation is initiated from the system console.

- Initial program load (IPL) is initiated from the console display.

- Automatic IPL is initiated by the system control processor (SCP). (An automatic IPL occurs when power is turned on, as well as for automatic recovery or IPL.)

- An automatic restart occurs due to a momentary power turn-off.

A change from an operating state to stop state occurs when:

- Stop of operation is initiated from the system console.

- An instruction is executed during instruction step mode.

- The required address coincided during address stop mode.

- A halt-and-proceed instruction executed.

- An emergency-stop (EMS) instruction executed.

For these conditions, the stop state is generated after the currently executed instruction is terminated, or when the processing unit is in waiting state. Interrupt is held in abeyance during that time.

The contents of the PSW or the instruction designated by the instruction address of the PSW can be displayed on the console display screen when the processing unit is in stop state. This is done by selecting the manual frame or alter/display frame on the console display keyboard.

When the halt-and-proceed instruction is issued, stop state is generated as if this instruction was not executed.

Execution is restarted from the next instruction when a change is made from stop state to operating state with the operations listed previously for that condition change.

Other hardware stop conditions can also cause a change to stop state. (See Figure 3-13 and Tables 3-5 and 3-6.)

### 3.2.2. Processing Unit Substates

The processing unit states can generally be classified into substates based on the processing unit generating condition. Figure 3-13 and Table 3-5 and 3-6 describe the substates.
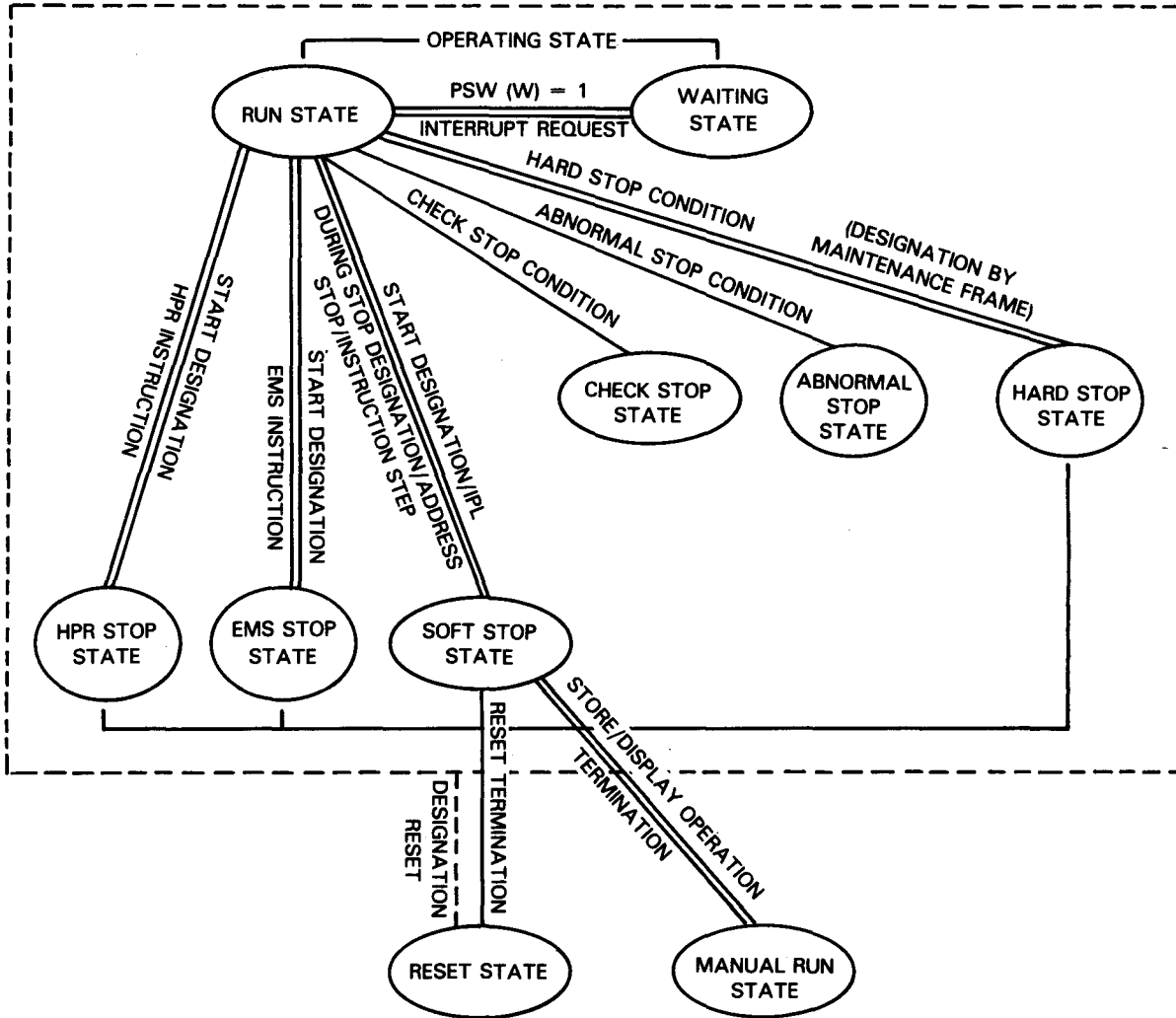


**Figure 3-13. Processing Unit State Transfer**

## Table 3-5. Model 8 CPU Substates

| State | Substate | Generating Condition | Indicator Lit on System Console |
|---|---|---|---|
| Check-STOP | C-stop (check-stop) | 1. Machine check during machine check interrupt processing (CS=1).<br><br>2. By check-stop control switch | C-stop |
| Stop | Hard stop ABN-stop (abnormal stop) | 1. Program exception during machine check interrupt processing.<br><br>2. P-bus interface time-over condition during IIS of machine check interrupt (during FDD log). (See note 1.) | STOP |
|  | M-H stop | 1. Manual operation.<br><br>2. Coincidence of address during microaddress search stop. |  |
|  | S-stop HPR stop | By execution of HPR instruction. |  |
|  | M-stop | 1. Manual operation.<br><br>2. Coincidence of address during the instruction address search stop mode. |  |
|  | EMS stop | By execution of EMS instruction. |  |
| Run | Run | During operation (instruction execution, interrupt, IOST processing). | RUN |
| Waiting | Wait | PSW wait bit is set up. | WAIT |
| Reset-run | M-run | During reset operation. | STOP |

NOTES:

1. Multiple interface time-over condition has occurred by an AIO operation relative to I/O interrupt. (Selected I/O address cannot be assured.)

2. Cycle ROM state, manual run state, etc, are available as hardware states of the CPU, in addition to the foregoing states.

## Table 3-6. Models 10/15/20 Processing Unit Substates

| Status | State | Substate | Generating Condition | Indicator Lit on System Console |
|---|---|---|---|---|
| Check-STOP | | C-stop (check-stop) | 1. Machine check during machine check interrupt processing (CS=1). <br><br> 2. By check-stop control switch (others) | C-stop |
| Stop | S-stop (soft stop) | ABN-stop (abnormal stop) | 1. Program exception during machine check interrupt processing. <br><br> 2. L-bus interface time-over condition during IIS of machine check interrupt. (See note 1.) | STOP |
| | H-stop (hard stop) | M-H stop | 1. Manual operation. <br><br> 2. Coincidence of address during microaddress search stop. | |
| | S-stop (soft stop) | HPR-stop | By execution of HPR instruction. | |
| | | M-stop | 1. Manual operation. <br><br> 2. Coincidence of address during the instruction address search stop mode. | |
| | | EMS-stop | By execution of EMS instruction. | |
| Run | Operating | Run | During operation (instruction execution, interrupt, IOST processing). | RUN |
| Wait | | Wait | PSW wait bit is set up. | WAIT |
| | Reset-run | M-run | 1. During reset operation. <br><br> 2. Manual operation. | STOP |

NOTES:

1. Multiple interface time-over condition has occurred by an AIO operation relative to IOP interrupt. (Selected IOP address cannot be assured.)

2. Cycle ROM state, manual run state, etc, are available as hardware states of the BPU, in addition to the foregoing states.

## 3.3. PROGRAM STATUS WORDS

Program status words (PSWs) have a variety of control fields to define instruction addresses and operating modes. The system has six PSWs for control uses. Each PSW is divided into an old and new PSW. Each old and new PSW consists of a double word. Programs are executed by controlling the current PSW, which consists of a double word stored in the processing unit.

The PSW control field:

■    Shows the storage protection and relocation (SPR) key

■    Holds the program branching status

■    Assists in interrupt analysis

Programs are executed under control of PSWs stored in the processing unit. For this reason, the PSW of the program currently executing is called the current PSW.

All PSWs, or some fields of them, are stored in the current PSW by interruption of a variety of instructions. An entire PSW is accessed when an interrupt occurs, and the current PSW is stored in the old PSW fixed area of main storage. The current PSW is also accessed by executing load PSW instructions.

The eight bits of the system mask in a PSW are partially stored by the set-system-mask (SSM) instruction. The six bits in the program mask field are stored by the set-program-mask (SPM) instruction. Instruction length codes (ILC), condition codes (CC), instruction addresses, etc, are continuously updated in accordance with the sequence of the instruction words to be executed.

When the branch-and-link (BAL) instruction is executed, the contents of the lower 32 bits in the current PSW are stored in the link registers (operand 1 registers).

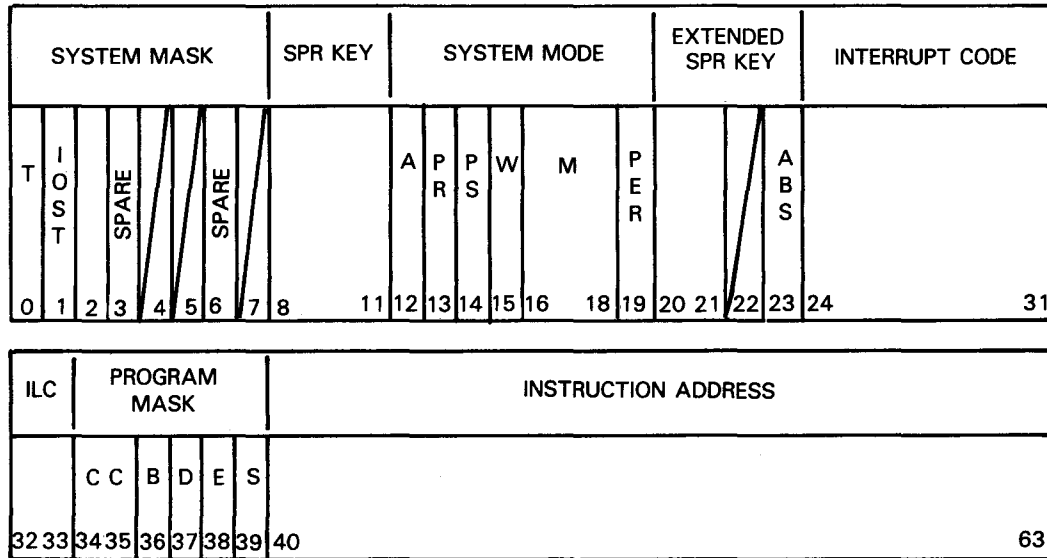The PSW format is made up of a double word (eight bytes). Figure 3-14 illustrates the format.

| SYSTEM MASK | | | | | | | | SPR KEY | SYSTEM MODE | | | | | | | EXTENDED SPR KEY | | | INTERRUPT CODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T | I O S T | | SPARE | | | SPARE | | | | A | P R | P S | W | M | | P E R | | | A B S | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8   11 | 12 | 13 | 14 | 15 | 16   18 | 19 | 20 | 21 | 22 | 23 | 24                    31 |

| ILC | PROGRAM MASK | | | | | INSTRUCTION ADDRESS |
|---|---|---|---|---|---|---|
| | C C | B | D | E | S | |
| 32 33 | 34 35 | 36 | 37 | 38 | 39 | 40                              63 |

Figure 3-14.  PSW Format

### 3.3.1.  System Mask

Of the eight-stage interrupt levels in the processing unit, three interrupt levels are controlled by the system mask bits. When the mask bits corresponding to individual interrupts are set to 1, and all other required conditions are satisfied, interrupts corresponding to the mask bits can occur. Interrupts corresponding to the mask bits cannot occur, however, if the mask bits are set to 0.  Figure 3-15 illustrates the system mask field.
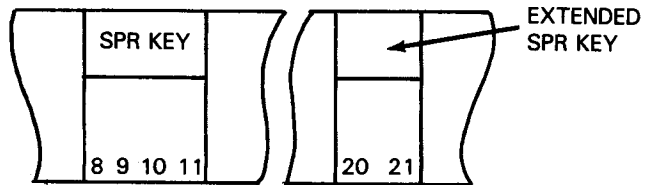
| SYSTEM MASK | | | | |
|---|---|---|---|---|
| T | I O S T | R E S E R V E D 2 | SPARE | |
| 0 | 1 | | | |
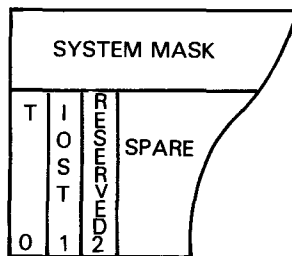
LEGEND:

| | |
|---|---|
| Bit 0 | T is timer interrupt mask. |
| Bits 3, 6 | Spares |
| Bit 1 | IOST is input/output status tabler interrupt mask |
| Bit 2 | Reserved |
| Bits 4, 5 and 7 | Not used |

Figure 3-15.  System Mask Field

### 3.3.2. SPR Keys

SPR keys are required for storage protection and address relocation. Figure 3-16 illustrates the SPR key fields.



LEGEND:

Bits 8 to 11

    Storage keys for storage protection and numbers corresponding to address relocation registers to perform address relocation.
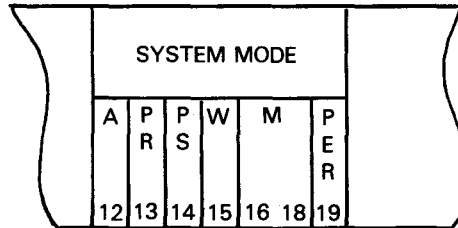
Bits 20 to 21

    Extended SPR keys that will become the upper 2 bits in a 6-bit key.

**Figure 3-16. SPR Keys**

### 3.3.3. System Mode

The system mode field defines a variety of operating modes used in the processing unit. Figure 3-17 illustrates the system mode field.

LEGEND:

Bit 12: A — (ASCII mode)

This bit is always zero since the system operates in EBCDIC mode.

Bit 13: PR (Problem register mode)

The CPU has two sets of 16 general registers. These two sets are called the problem registers and supervisor registers, respectively. The problem register defines which general registers are used by the CPU, and is performed by the PR bit:

PR = 1    Problem mode

PR = 0    Supervisor mode

Bit 14: PS (Problem mode)

The CPU operates in either of two modes; problem or supervisor mode. When operating in supervisor mode, all instructions can be executed. Instructions other than priviledged can be executed while in problem mode. When a priviledged instruction is executed in problem mode, an interrupt request other than a program exception is made. The mode definition is:

PS = 1    Problem mode

PS = 0    Supervisor mode

Bit 15: W (Wait mode)

When bit 15 is 1, the CPU is in waiting status, and no instructions are executed. However, interrupt and IOST processing are performed. Waiting status remains set until the wait bit becomes 0 by an interrupt. Patrolling is performed while waiting for bit 15 to be set to 0.

Bits 16 to 18 — always set to 0.

It should be noted that when a value other than 0 is set in bit 12 and bits 16 to 18 of the PSW, the value is considered as an incorrect PSW and it becomes an interrupt of program exception item in the specification immediately before executing the next instruction. No program execption of the LPSW instruction is obtained even when an incorrect PSW is set. It becomes a program exception item of the new instruction address.

Bit 19: PER (Program event recording)

This mode is used when an interrupt for a program analysis is required before executing individual instructions of the program being executed. The PER mode is:

PER = 1   Execution of PER mode

PER = 0   Execution of ordinary mode

**Figure 3-17. System Mode Fields**

### 3.3.4. Interrupt Code

The interrupt code is used to analyze the interrupt state of software when an interrupt occurs. Figure 3-18 illustrates the interrupt code field.
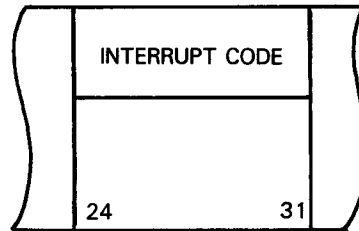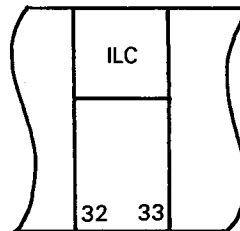


**Figure 3-18. Interrupt Code Field**

### 3.3.5. Instruction Length Code

The instruction length code (ILC) field calculates the instruction address that was stopped or inhibited, together with the address stored in the instruction address field of the PSW. Figure 3-19 illustrates the ILC field.
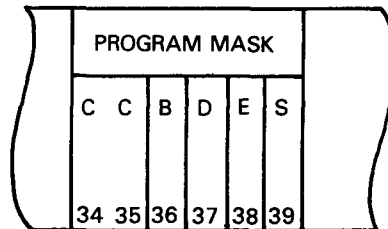


LEGEND:

| Bit | 32 | 33 | | |
|-----|----|----|---|---|
| | 0 | 0 | = | Instruction has been completed. |
| | 0 | 1 | = | 2-byte instruction |
| | 1 | 0 | = | 4-byte instruction |
| | 1 | 1 | = | 6-byte instruction |

**Figure 3-19. Instruction Length Code Field**

### 3.3.6. Program Mask

The program mask includes four types of mask bits to show program exception items. Figure 3-20 illustrates the exception items corresponding to individual mask bits.

```
┌─────────────────────┐
│  PROGRAM MASK       │
├──┬──┬──┬──┬──┬──┤
│C  C │B │D │E │S │
│     │  │  │  │  │
│34 35│36│37│38│39│
└──┴──┴──┴──┴──┴──┘
```

LEGEND:

Bits 34 and 35: CC

A condition code conforming to the results of instruction execution is set in this field. The value of this condition code is checked by various types of branch instructions.

Bit 36: B

Exception item of upper overflow of fixed-point operation.

Bit 37: D

Exception item of upper overflow of decimal number operation.

Bit 38: E

Exception item of lower overflow of exponent in floating-point operation.

Bit 39: S

Exception item of effective numeric character in floating-point operation.

### Figure 3-20. Program Mask Field

### 3.3.7. Instruction Address

The address stored in this field designates the first instruction of the program (relative address) to be executed, when the contents of the new PSW in the system fixed area of main storage are stored in the current PSW of the processing unit. This field is updated whenever various instructions are executed. An updated instruction designates an instruction next to the one executed. This condition is limited, however, to when an interrupt or the branch-and-link instruction is not generated.

When branching is executed, the branch address is stored in the instruction address field of the current PSW. The instruction is executed according to the stored address.

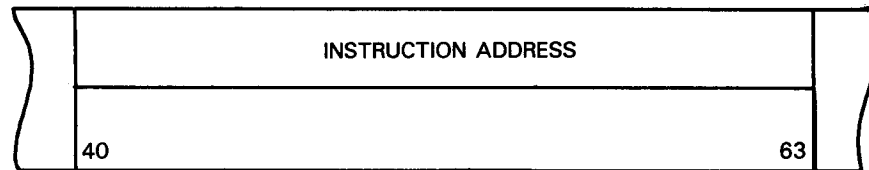Figure 3-21 illustrates the instruction address field.



**Figure 3-21. Instruction Address Field**

## 3.4. ADDRESS RELOCATION

Problem programs don't need to adhere to absolute addresses in main storage in order to be flexible and effective. Regardless of the program purpose or function, program relocation provides a method of relocating programs in main storage. The supervisor can position to any point in main storage providing a 1-byte boundary by adjusting the relocation related to certain programs or data.

There are two methods to determine program addresses:

■    Address generation

This method is used to decide an operand and branch address by an instruction in RS, SI, and SS formats. Addresses are determined by adding a value shown in the D field of the instruction operand to the contents of the general registers designated by the B field. In such instances, addresses are determined by an RX format instruction after adding the contents of the general registers designated in the X2 field.

■    Address relocation

This method adds a relocation value to the address determined by the method described previously, when deciding operand and branch addresses. Instruction addresses and other addresses can be modified by applying this method. Figure 3-22 illustrates the address modifications.
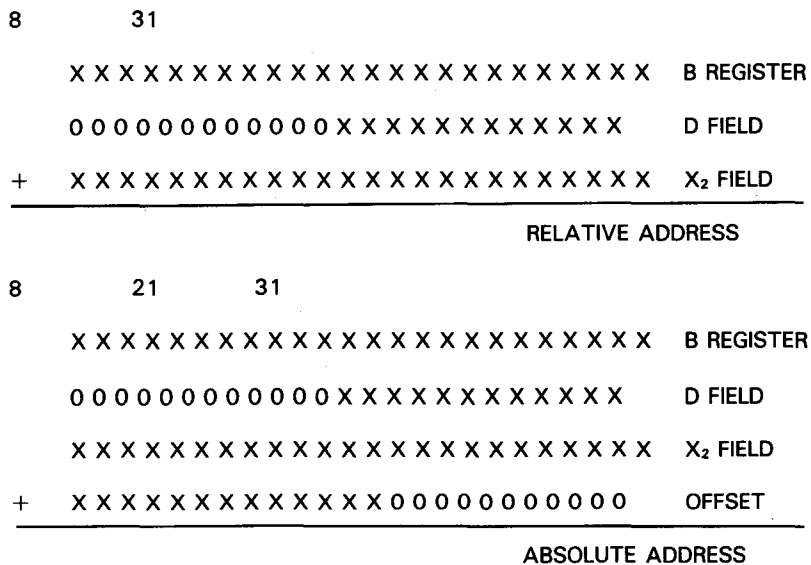
```
8           31

       X X X X X X X X X X X X X X X X X X X X X X X X    B REGISTER

       0 0 0 0 0 0 0 0 0 0 0 0 X X X X X X X X X X X X    D FIELD

+      X X X X X X X X X X X X X X X X X X X X X X X X    X₂ FIELD
      _____
                                        RELATIVE ADDRESS

8           21          31

       X X X X X X X X X X X X X X X X X X X X X X X X    B REGISTER

       0 0 0 0 0 0 0 0 0 0 0 0 X X X X X X X X X X X X    D FIELD

       X X X X X X X X X X X X X X X X X X X X X X X X    X₂ FIELD

+      X X X X X X X X X X X X X 0 0 0 0 0 0 0 0 0 0      OFFSET
      _____
                                        ABSOLUTE ADDRESS
```

Figure 3-22.  Relative Address and Address Modification

### 3.4.1. Absolute and Relative Addresses

Addresses in main storage are determined by both hardware and programs. Addresses produced by hardware are absolute addresses. Absolute addresses are always used when addressing locations in main storage.

Addresses produced and used by programs are relative addresses. That is, they are relative to the program's start address. For example, the addresses referring to instructions and data in an object code program are relative to the program's start address.

The relative addresses do not necessarily have the same values as the absolute addresses used to refer to these locations in main storage.

Relative and absolute addresses are defined as follows:

■ A relative address is an address before modification by address relocation. The address is relocatable.

■ An absolute address cannot be relocated. Addresses produced by hardware or used by the IOST, are absolute addresses. Hardware can refer directly to an absolute address by means of the MSU. All input and output refer to absolute addresses.

An absolute address can be a relocated address after offset is applied to a relative address. This includes instances when absolute addresses have the same values as those of relative addresses after a zero relocation value is applied to the relative addressses.

When the ABS mode of a PSW is set to 1, the relative address becomes an absolute address.

### 3.4.2. Basic Characteristics of Address Relocation

Address relocation is performed by adding a relocation value to the upper 24 bits in main storage. The relocation value is expressed by 24 bits (bits 21 to 31 are added as being 0). Address relocation is calculated when there is no prior relocation. The resultant 24-bit value gives base addresses of relocation in units of 2048 bytes.

Relocation is controlled by the values stored in 64 relocation registers in addresses from 200x to 2FFx in main storage. These registers show hexadecimal numbers and are numbered from 0 to 63. The individual register numbers correspond to storage protection (SPR) and relocation keys. These registers are used by the processing unit. The SPR keys select specific relocation registers.

The processing unit has current relocation registers that store other relocation registers maintained for status in the processing unit. These are located among the 64 relocation registers.

Relocation values stored in relocation registers in main storage can be shifted to the current relocation registers in the processing unit only by:

■  Executing the load PSW instruction, or

■  An interrupt initialization sequence (IIS) of an interrupt start.

### 3.4.3. Current Relocation Register

The contents of relocation registers in main storage that correspond to the SPR keys are loaded in the current relocation register only when the new SPR key is stored in the current PSW. This occurs when the current PSW is changed by either of the following:

■  The interrupt initialization sequence

■  Execution of the load PSW instruction

The new SPR key is then used as a pointer to access the relocation registers. Contents of the relocation register accessed by this pointer is loaded in the current relocation register in the processing unit.

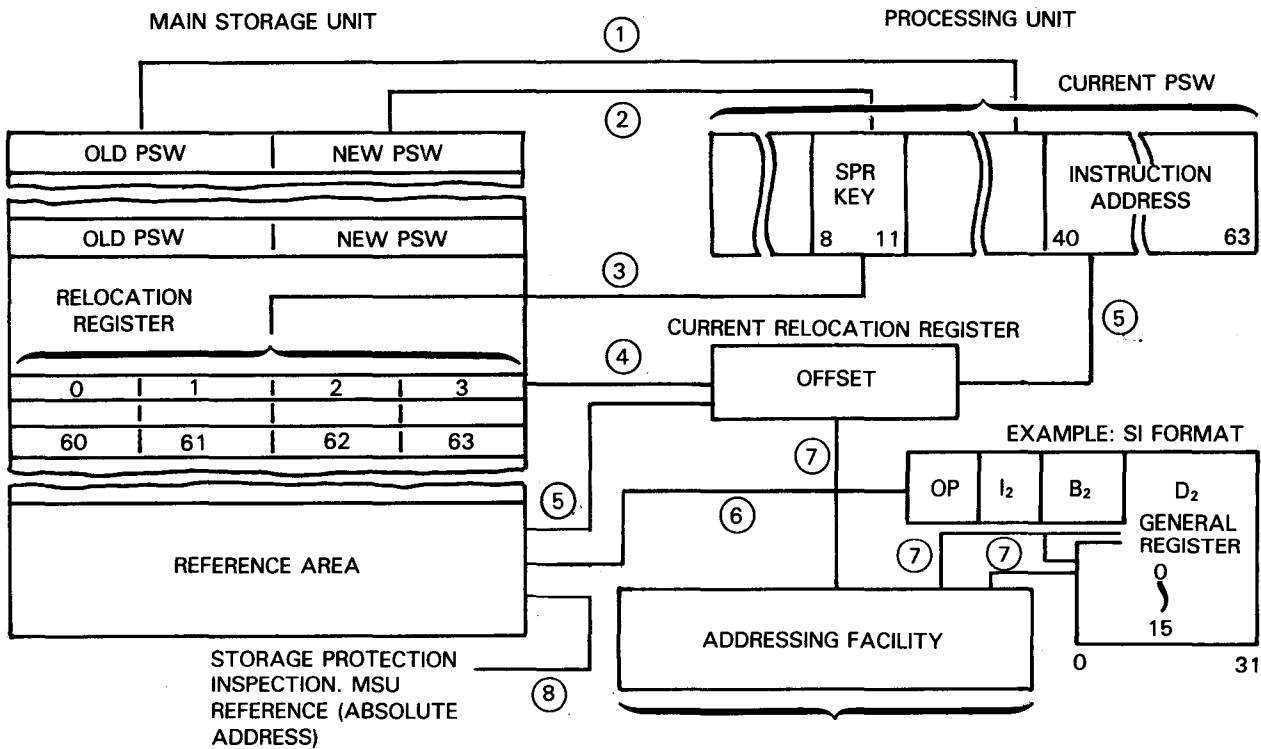Figure 3-23 shows the address relocation structure.



Figure 3-23.  Address Relocation Structure (part 1 of 2)

NOTES:

1.  The interrupt initialization procedure is implemented after the interrupt has been authorized. Contents of the current PSW are stored in the old PSW of the corresponding interrupt level.

2.  Contents of the new PSW in the corresponding interrupt level are placed in the current PSW.

3.  One of the relocation registers in the fixed area of main storage is selected by the new SPR key placed in the current PSW.

4.  The value of the selected relocation register is placed in the current relocation register of the CPU.

5.  During instruction execution, the instruction address is converted into an absolute address, and main storage is referenced.

6.  An instruction word is referred to (for example, instruction word of the SI format). Instruction execution is started.

7.  One of the general registers is selected by the value of the B1 field, and the value contained in the general register selected is added to the addressing facility. The value of the D1 field is added to the addressing facility. Reference address of main storage is produced when the relocation value of the current relocation register is added to the addressing facility, thus becoming an absolute address.

8.  Absolute addresses produced through the addressing facility refers to main storage after receiving storage protection checking.

**Figure 3-23.  Address Relocation Structure (part 2 of 2)**

### 3.4.4.  Relocation of Instruction Addresses

Instruction addresses of the current PSW are relative addresses. Instructions are executed by converting these relative addresses to absolute addresses. Instruction addresses of the current PSW are updated whenever an instruction is executed. The updated instruction address designates the address of the instruction next to the one executed.

In the following instances, however, special instuction addresses are designated:

■   Execution of a Branch Instruction to Cause Branching

The branch address becomes the new instruction address of the new PSW.

■   Execution of IIS

When executing IIS, the instruction address of the current PSW to be substituted is stored in the old PSW. The instruction address of the new PSW corresponding to the interrupt becomes the new instruction address of the current PSW.

■   Execution of Load PSW Instruction

The instruction address of the PSW addressed by operand 1 of the load PSW instruction becomes the new instruction address of the current PSW.

■   Resetting of Current Relocation Register

The PSW is cleared and the zero address becomes a new instruction address when the processing unit is reset. Contents of the relocation register are also cleared to zero.

### 3.4.5. Address Relocation of Operand

The instruction operand addresses are converted from relative addresses to absolute addresses, when necessary, depending on the specific instructions to be executed.

Address relocation does not apply to the operand addresses of all instructions. In the case of the load-address and input/output instructions, operand addresses are not converted from relative to absolute addresses.

Relocation values are added simultaneously with conversion of the instruction operand addresses D + (B). D + (B) + OFFSET = absolute address. In RX format instructions, the content of the index register X2 is added:

- Following D + (B) + OFFSET for model 8

- Before D + (B) + OFFSET for models 10/15/20

### 3.4.6. Address Relocation of Input/Output Channels

Address relocation of input/output channels is not performed. This procedure always designates absolute addresses.

## 3.5. STORAGE PROTECTION

### 3.5.1. Model 8 Storage Protection

**Storage Key and Key Memory** _____

Storage protection is made in units of 2048 bytes (2K). Storage keys are stored in the key memory of main storage.

The number of storage key memories is determined by dividing the capacity of main storage by 2K. For example, when storage capacity is 1 MB, there are 512 storage keys required. When main storage capacity is 8 MB, there are 4096 storage keys required.

Storage keys are set for blocks in units of 2048 bytes by the supervisor. The storage keys are stored in the correct positions of key memory by executing the set-storage-key (SSK) instruction. The insert-storage-key (ISK) instruction is used to read storage keys from key memory. These are two privileged instructions and are executed only when the processing unit is in supervisor mode.

A program storage key is available for every 2048 bytes, and one storage key may be found in more than two key memory positions.

Figure 3-24 illustrates the storage protection and key memory fields.
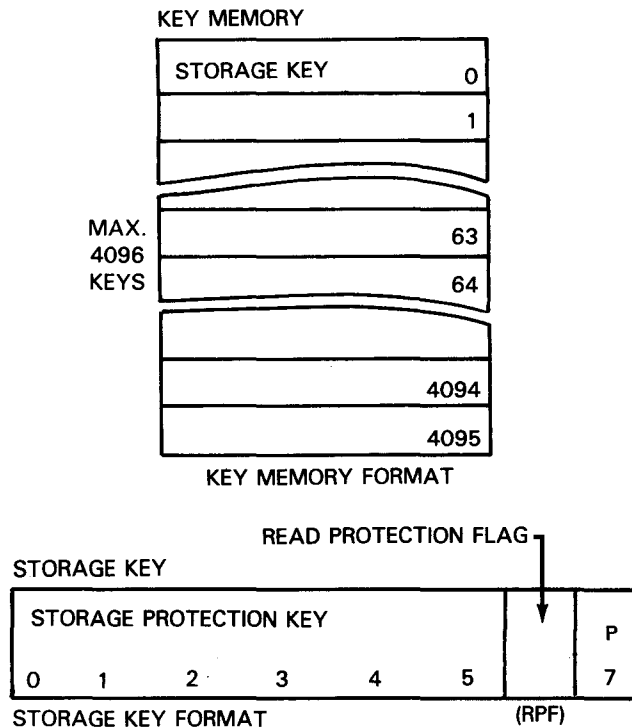


Figure 3-24. Storage Protection and Key Memory Field (part 1 of 2)

LEGEND:

Bits 0 to 5

    A 6-bit code to allocate a 2048-byte block to one of the 64 programs.

Bit 6 (RPF)

    When this bit is 0, writing only is protected. When this bit is 1, there is write/read protection.

Bit 7

    Parity bit. This bit is invisible from software.

**Figure 3-24.  Storage Protection and Key Memory Field (part 2 of 2)**

## Storage Protection and Relocation (SPR) Key

The storage protection facility uses 6-bit storage protection keys to recognize a program or operation that requests access to main storage.

Storage protection inspection uses the key fields in bits 8 to 11, 20, and 21 in the current PSW of the processing unit for reference in main storage. Main storage is accessed by the IOST with a storage protection key allocated by the IOST CW.

Main storage is controlled by a storage protection key allocated to input/output operations by an input/output channel. The storage key is used for:

■    Protection

■    Selection of a relocation register for the system in the fixed area of main storage when relocating addresses

This is called a storage protection and relocation key, or an I/O storage protection key of the current PSW.
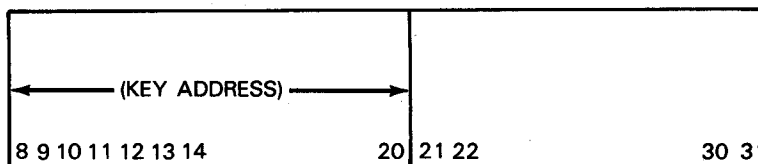
## Key Comparison and Main Storage Access

When the processing unit or input/output channel starts to access main storage:

■    A key memory corresponding to a 2048-bit unit of main storage is selected.

■    The storage key is accessed.

A 24-bit addressing facility is used when the processing unit or input/output channel refers to main storage.

Figure 3-25 illustrates the addressing facility and key addresses.

```
┌──────────────────────────────┬──────────────────────────┐
│                              │                          │
│   ◄──────(KEY ADDRESS)──────► │                          │
│                              │                          │
│ 8 9 10 11 12 13 14        20 │ 21 22              30 31  │
└──────────────────────────────┴──────────────────────────┘
```

NOTES:

1.  Bits 8 to 31 of the addressing facility show the address in the main storage unit to be referenced.

2.  Bits 8 to 20 can show an address in a 2048 byte unit.

**Figure 3-25. Addressing Facility and Key Address**

The system uses bits 8 to 20 as key addresses corresponding to a key memory. A storage key allocated to an address of currently accessed main storage is selected by a key address formed by bits 8 to 20. The key section (upper 6 bits) of the storage key selected from the key memories is compared with the I/O storage protection key or the SPR key of the current PSW. As a result of the comparison, access to main storage is determined as follows:

■   Writing

-   Access is allowed when the storage key is equal to the storage protection key of the current PSW, IOST CW, or of input/output.

-   Access is allowed when the storage protection key of the current PSW, IOST CW, or input/output is zero in a binary number.

-   No access is allowed when the SPR key is not zero and when the storage key is not equal to the SPR key of the current PSW, IOST CW, or input/output.
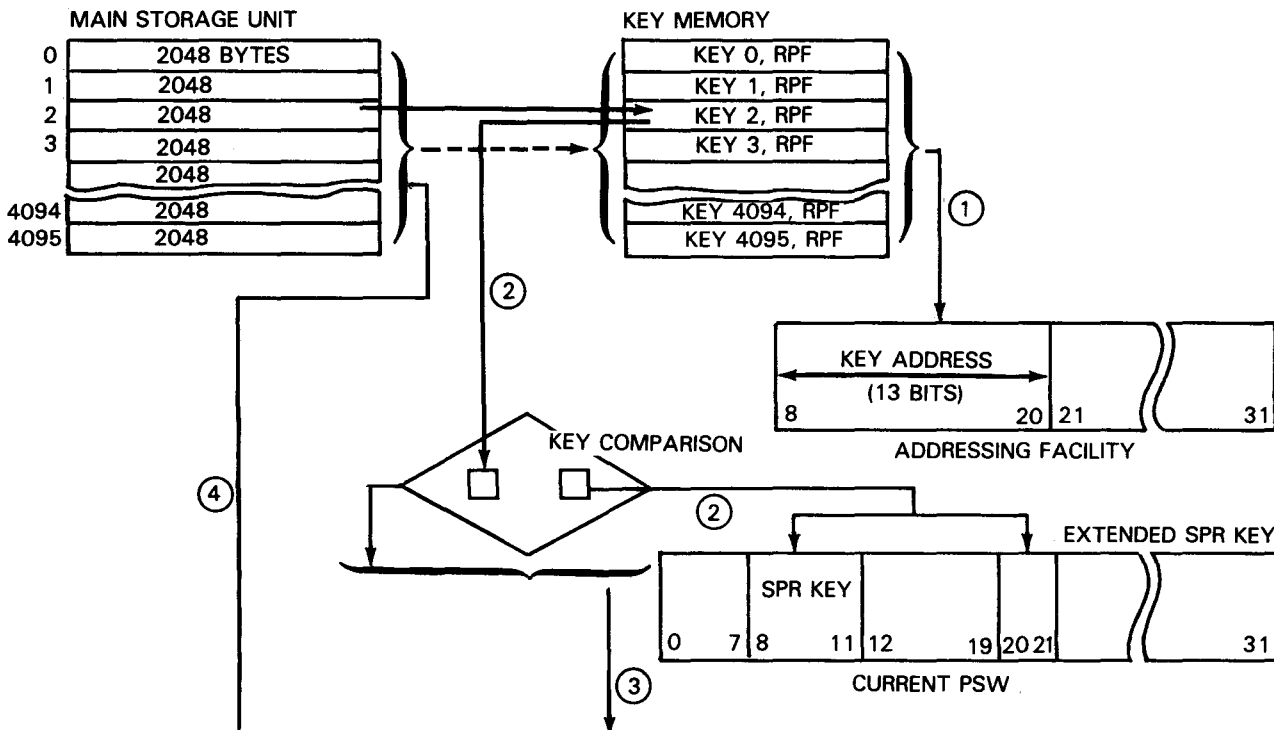
■   Reading

-   Access is allowed when the SPR key is equal to the storage protection key of the current PSW, IOST CW, or input/output.

-   Access is allowed when the SPR key of the current PSW, IOST CW, or input/output is zero.

-   When the SPR key is not zero, and the storage key is not equal to the storage protection key to the current PSW, IOST CW, or input/output, and:

    (1)   When the read protection flag = 0, access is allowed.

    (2)   When the read protection flag = 1, no access is allowed.

As a result of the foregoing comparison, a storage protection exception item occurs when the conditions do not allow access to main storage.

The processing unit protects the original data when reference is for writing. Main storage executes a read cycle when reference is for reading. The processing unit blocks this read data, however. A request for program exception interruption occurs when an exception of storage protection occurs in the referenced program.

Figure 3-26 illustrates the storage protection facility for the model 8.

MAIN STORAGE UNIT

| | |
|---|---|
| 0 | 2048 BYTES |
| 1 | 2048 |
| 2 | 2048 |
| 3 | 2048 |
| | 2048 |
| 4094 | 2048 |
| 4095 | 2048 |

KEY MEMORY

| |
|---|
| KEY 0, RPF |
| KEY 1, RPF |
| KEY 2, RPF |
| KEY 3, RPF |
| |
| KEY 4094, RPF |
| KEY 4095, RPF |

(1)

KEY ADDRESS
(13 BITS)
8    20 | 21    31
ADDRESSING FACILITY

(2)

KEY COMPARISON

(4)

(2)

EXTENDED SPR KEY

| | SPR KEY | | | |
|---|---|---|---|---|
| 0    7 | 8    11 | 12    19 | 20 21 | 31 |

CURRENT PSW

(3)

| COMPARISON RESULTS | RPF FLAG | REFERENCE TO MAIN STORAGE UNIT | |
|---|---|---|---|
| | | READ | WRITE |
| EQ | 1 | POSSIBLE | POSSIBLE |
| EQ | 0 | POSSIBLE | POSSIBLE |
| EQ | 1 | NOT POSSIBLE | NOT POSSIBLE |
| EQ | 0 | POSSIBLE | NOT POSSIBLE |

{ REQUEST FOR INTERRUPT OF STORAGE PROTECTION

CONDITION FOR APPROVAL OF REFERENCE TO
MAIN STORAGE UNIT

NOTES:

1. In the absolute addresses produced by the addressing facility, 11 bits of the addressing facility (that is, bits 10 to 20), act as a key address to select one of up to 4096 storage keys (storage capacity being 8 MB) stored in the key memory.

2. The selected storage key is compared with the SPR key of the current PSW.

3. Following the conditions of 1 and 2, approval of reference to main storage is determined by the conditions illustrated.

4. When reference to main storage is approved or the SPR key in the current PSW is zero, the CPU can refer to main storage. If reference to main storage is not approved, however, memory exception occurs.

**Figure 3-26. Storage Protection Facility**

### 3.5.2. Models 10/15/20 Storage Protection

**Storage Key and Key Memory** _____

Storage protection is performed in units of 4096 bytes (4K). It is determined by dividing main storage by the 8-bit storage key in each unit.

Storage keys are stored in the key memory of main storage. The number of storage key memories is determined by the capacity of main storage. For example, when storage capacity is 1 MB, there are 256 storage keys required. When main storage capacity is 16 MB, there are 4096 storage keys required.

Storage keys are set for blocks in units of 4096 bytes by the supervisor. The storage keys are stored in the correct positions of key memory by executing the set-storage-key (SSK) instruction. The insert-storage-key (ISK) instruction is used to read storage keys from key memory. These are two privileged instructions and are executed only when the processing unit is in supervisor mode.

A program storage key is available for every 4096 bytes, and one storage key may be found in more than two key memory positions.

Figure 3-27 illustrates the storage protection and key memory fields.



Figure 3-27. Storage Protection and Key Memory Field (part 1 of 2)

LEGEND:

Bits 0 to 5

    A 6-bit code to allocate a 4096-byte block to one of the 64 programs.

Bit 6 (RPF)

    When this bit is 0, writing only is protected. When this bit is 1, there is write/read protection.

Bit 7

    Parity bit. This bit is invisible from software.

**Figure 3-27. Storage Protection and Key Memory Field (part 2 of 2)**

## Storage Protection and Relocation (SPR) Key

The storage protection facility uses 6-bit storage protection keys to recognize a program or operation that requests access to main storage.

Storage protection inspection uses the key fields in bits 8 to 11, 20, and 21 in the current PSW of the processing unit for reference in main storage. Main storage is accessed by the IOST with a storage protection key allocated by the IOST CW.

Main storage is controlled by a storage protection key allocated to input/output operations by an input/output channel. The storage key is used for:

■    Protection

■    Selection of a relocation register for the system in the fixed area of main storage when relocating addresses

This is called a storage protection and relocation key, or an I/O storage protection key of the current PSW.

## Key Comparison and Main Storage Access

When the processing unit or input/output channel starts to access main storage:

■    A key memory corresponding to a 4096-bit unit of main storage is selected.

■    The storage key is accessed.

A 24-bit addressing facility is used when the processing unit or input/output channel refers to main storage.

Figure 3-28 illustrates the addressing facility and key addresses.
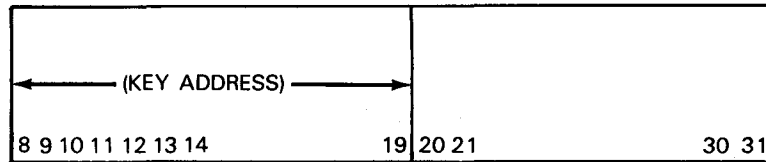
```
┌─────────────────────────────────┬─────────────────────────────┐
│                                 │                             │
│  ←───── (KEY ADDRESS) ─────→    │                             │
│                                 │                             │
│ 8 9 10 11 12 13 14         19│20 21               30 31│
└─────────────────────────────────┴─────────────────────────────┘
```

NOTES:

1.   Bits 8 to 31 of the addressing facility show the address in the main storage unit to be referenced.

2.   Bits 8 to 19 can show an address in a 4096 byte unit.

**Figure 3-28.  Addressing Facility and Key Address**

The system uses bits 8 to 19 as key addresses corresponding to a key memory. A storage key allocated to an address of currently accessed main storage is selected by a key address from among the key memories. The key section (upper 6 bits) of the storage key selected from the key memories is compared with the I/O storage protection key or the SPR key of the current PSW. As a result of the comparison, access to main storage is determined as follows:

■   Writing

-   Access is allowed when the storage key is equal to the storage protection key of the current PSW, IOST CW, or of input/output.

-   Access is allowed when the storage protection key of the current PSW, IOST CW, or input/output is zero in a binary number.

-   No access is allowed when the SPR key is not zero and when the storage key is not equal to the SPR key of the current PSW, IOST CW, or input/output.

■   Reading

-   Access is allowed when the SPR key is equal to the storage protection key of the current PSW, IOST CW, or input/output.

-   Access is allowed when the SPR key of the current PSW, IOST CW, or input/output is zero.

-   When the SPR key is not zero, and the storage key is not equal to the storage protection key to the current PSW, IOST CW, or input/output, and:

    (1)   When the read protection flag = 0, access is allowed.

    (2)   When the read protection flag = 1, no access is allowed.

As a result of the foregoing comparison, a storage protection exception item occurs when the conditions do not allow access to main storage.

The processing unit protects the original data when reference is for writing. Main storage executes a read cycle when reference is for reading. The processing unit blocks this read data, however. A request for program exception interruption occurs when an exception of storage protection occurred in the referenced program.

Figure 3-29 illustrates the storage protection facility for the models 10/15/20.
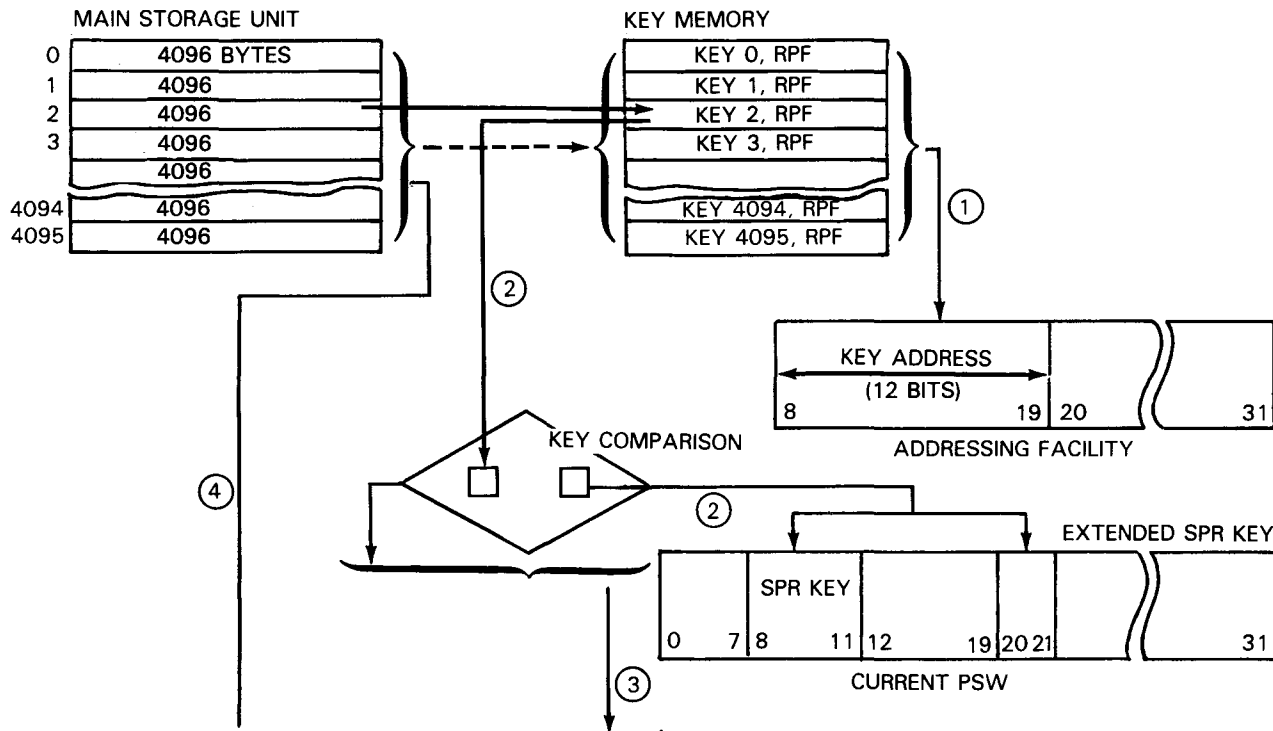
MAIN STORAGE UNIT

| | |
|---|---|
| 0 | 4096 BYTES |
| 1 | 4096 |
| 2 | 4096 |
| 3 | 4096 |
| | 4096 |
| 4094 | 4096 |
| 4095 | 4096 |

KEY MEMORY

KEY 0, RPF
KEY 1, RPF
KEY 2, RPF
KEY 3, RPF
KEY 4094, RPF
KEY 4095, RPF

KEY ADDRESS (12 BITS)
8 ... 19 | 20 ... 31
ADDRESSING FACILITY

KEY COMPARISON

EXTENDED SPR KEY

SPR KEY
0  7 | 8  11 | 12  19 | 20 21 ... 31
CURRENT PSW

CONDITION FOR APPROVAL OF REFERENCE TO MAIN STORAGE UNIT

| COMPARISON RESULTS | RPF FLAG | REFERENCE TO MAIN STORAGE UNIT | |
|---|---|---|---|
| | | READ | WRITE |
| EQ | 1 | POSSIBLE | POSSIBLE |
| EQ | 0 | POSSIBLE | POSSIBLE |
| NOT EQ | 1 | NOT POSSIBLE | NOT POSSIBLE |
| NOT EQ | 0 | POSSIBLE | NOT POSSIBLE |

REQUEST FOR INTERRUPT OF STORAGE PROTECTION

NOTES:

1. In the absolute addresses produced by the addressing facility, 12 bits of the addressing facility (that is, bits 8 to 19), act as a key address to select one of up to 4096 storage keys (storage capacity being 16 MB) stored in the key memory.

2. The selected storage key is compared with the SPR key of the current PSW.

3. Following the conditions of 1 and 2, approval of reference to main storage is determined by the conditions illustrated.

4. When reference to main storage is approved or the SPR key in the current PSW is zero, the processor can refer to main storage. If reference to main storage is not approved, however, memory exception occurs.

**Figure 3-29. Storage Protection Facility**

## 3.6. TIMER

There are two types of timers used in the system:

■ Interval timer (ITR)

■ Time-of-day clock (TOD)

### 3.6.1. Interval Timer

The functions of the interval timer are supplied by the processing unit. The operation is controlled by the interval timer register (ITR). An ITR count is determined by decrementing the ITR after it is turned on by executing a set-timer-register (STR) instruction.

The ITR is decremented by:

■ 2 every 2 ms for model 8

■ 1 every 1 ms for models 10/15/20

**Interval Timer Register** _____

The interval timer register (ITR) hardware in the processing unit is initialized by the STR instruction.

The timer value stored in the ITR is a binary number that provides an interrupt interval from 2 ms to 4.66 hours. An interval timer interrupt request occurs when the ITR count decrements to a negative value. (Also when the count decrements to 0 for model 8 systems.)

The ITR counts continuously after an interrupt request is generated.

The interval timer is on when the system is operating.

Figure 3-30 illustrates the ITR format.

```
┌─────────────────────────────────────┐
│                                      │
│                 ITR                  │
│0                                   23│
└─────────────────────────────────────┘
```
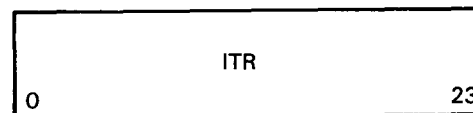
**Figure 3-30. Interval Timer Register Format**

The interval timer is turned off when the system is reset. In off state, the ITR (consisting of 24 bits) is not counted. The timer is turned on by the STR instruction, and counts continuously until turned off by the next STR instruction or by a system reset.

### 3.6.2. Time-of-Day Clock

The time-of-day (TOD) clock counts successive hours and days for a period of 143 years. The clock consists of a two word binary counter. The highest bit of this counter is not a sign bit.

For the model 8, bit 48 is incremented, while bits 49 to 63 are always 0. The clock is incremented every 8 microseconds. Figure 3-31 shows the model 8 TOD clock field.

```
┌──────────────────────────────────────────┐
│                                            │
│                                            │
└──────────────────────────────────────────┘
0                                          31

┌──────────────────────────────────────────┐
│                         │0───────────────0│
└──────────────────────────────────────────┘
32                       48 49             63
```
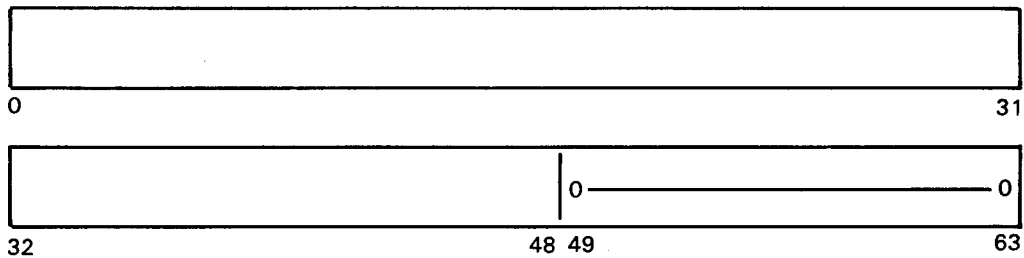
**Figure 3-31.  Model 8 Time-of-Day Clock Field**

For the models 10/15/20, bit 31 is incremented, while bits 32 to 63 are always 0. The clock is incremented every 1.048576 seconds. Figure 3-32 shows the models 10/15/20 TOD clock field.

```
┌──────────────────────────────────────────┐
│                                            │
│                                            │
└──────────────────────────────────────────┘
0                                          31

┌──────────────────────────────────────────┐
│0────────────────────────────────────────0│
└──────────────────────────────────────────┘
32                                         63
```
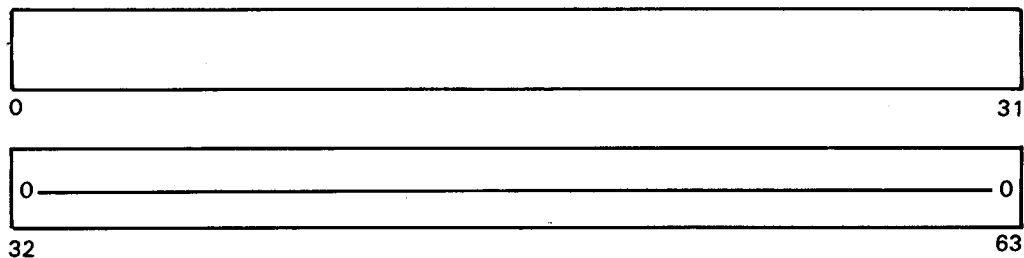
**Figure 3-32.  Models 10/15/20 Time-of-Day Clock Field**

When overflow from bit 0 occurs as a result of calculations, the overflow is ignored and addition from 0 resumes. At this time, neither interrupts nor traps are generated.

Figure 3-33 shows the TOD clock settings.

*NOTE:* *Bit 31 of the TOD clock is added every 1.048576 seconds. In terms of response speed of human operation, the accuracy is sufficient only with the first word. It is difficult to set the TOD clock to an accuracy of 2 microseconds, and the second word of a clock is normally inaccurate as a time element. The second word is used when measuring elapsed time with high accuracy.*

| TOD CLOCK BIT | STEPPING INTERVAL | | | |
|---|---|---|---|---|
| | DAYS | HOURS | MINUTES | SECONDS |
| 47 | | | | 0.000 00 |
| 43 | | | | 0.000 016 |
| | | | | 0.000 256 |
| 39 | | | | 0.004 096 |
| 35 | | | | 0.065 536 |
| 31 | | | | 1.048 576 |
| 27 | | | | 16.777 216 |
| 23 | | | 4 | 28.435 456 |
| 19 | | 1 | 11 | 34.967 296 |
| 15 | | 19 | 5 | 19.476 736 |
| 11 | 12 | 17 | 25 | 11.627 776 |
| 7 | 203 | 14 | 43 | 6.044 416 |
| 3 | 3257 | 19 | 29 | 36.710 656 |

Model 8 only: bits 47, 43, 39, 35

| YEAR | CLOCK | SETTING | | (HEX.) |
|---|---|---|---|---|
| 1900 | 0000 | 0000 | 0000 | 0000 |
| 1976 | 8853 | BAF0 | B400 | 0000 |
| 1980 | 8F80 | 9FD3 | 2200 | 0000 |
| 1984 | 96AD | 84B5 | 9000 | 0000 |
| 1988 | 9DDA | 6997 | FE00 | 0000 |
| 1992 | A507 | 4E7A | 6C00 | 0000 |
| 1996 | AC34 | 335C | DA00 | 0000 |
| 2000 | B361 | 183F | 4800 | 0000 |

| INTERVAL | CLOCK UNITS (HEX.) | | | |
|---|---|---|---|---|
| 1 MICROSECOND | | | | 1000 |
| 1 MILLISECOND | | | 3E | 8000 |
| 1 SECOND | | | F424 | 0000 |
| 1 MINUTE | | 39 | 3870 | 0000 |
| 1 HOUR | | D69 | 3A40 | 0000 |
| 1 DAY | 1 | 41DD | 7600 | 0000 |
| 365 DAYS | 1CA | E8C1 | 3E00 | 0000 |
| 366 DAYS | 1CC | 2A9E | 3400 | 0000 |
| 1,461 DAYS* | 72C | E4E2 | 6E00 | 0000 |

*Number of days in 4 years, including a leap year.

**Figure 3-33. TOD Clock Settings**

The clock operates without causing any effects to the system, and operates normally regardless of whether the processing unit is in an execution, waiting, or in stop state.

The TOD clock continues to operate normally in all instances:

■    When the compute-control instruction is in a step status or in the address-stop designation

■    For a system reset, initial program reset, or power on reset

■    When loading an initial program.

The TOD clock operates even when the processing unit power supply is turned off.

There are three TOD clock statuses:

■    Set status

■    Nonset status

■    Error status

The TOD clock is normally backed up by a battery power supply. When the batteries are discharged, however, a nonset status is set up in which the initial value becomes zero. The set status occurs when the set-clock instruction is normally sent to the clock in the nonset or error status. The machine check trap (timer abnormal) operates and the clock assumes error status when the clock operating condition is abnormal.

The TOD clock can be read by the store-clock instruction, and can be set by the set-clock instruction. Table 3-7 lists the results of the store-clock and set-clock instruction execution as set in the condition codes.

Table 3-7.  Condition Codes to Set Clock and Store Clock Instructions

| Condition Codes After Execution | | Set Clock | Store Clock |
|---|---|---|---|
| CCO | CC1 | | |
| 0 | 0 | TOD clock can be set | Set status |
| 0 | 1 | This condition code is nonexistent | Nonset status |
| 1 | 0 | Error status (models 10/15/20 only) | Error status |
| 1 | 1 | Not installed (model 8 only) | Not installed |

NOTE:

The store-clock instruction stores the value of the TOD clock immediately before executing the instruction.

## 3.7. INTERRUPT

The interrupt function notifies the processing unit that one of the following occurred:

■ A hardware operation is complete. .

■ An exception item is indicated.

■ An unforeseeable event occurred in hardware or software.

When any of these conditions occur, the processing unit takes the appropriate steps to notify the user by way of a program.

### 3.7.1. Interrupt Levels

The following interrupt levels are used in the system:

■ Machine check interrupt

■ Program exception interrupt

■ Supervisor call interrupt

■ Interval timer interrupt

■ Input/output status tabler (IOST) interrupt

■ Program event recording (PER) interrupt

These interrupt requests generate individual status conditions.

**Machine Check Interrupt** _____

The machine check interrupt notifies the operating system that a hardware error is detected. This error could represent an abnormality in main storage, a certain function stop status, blocked ventilating air, or some other cause.

In interrupt requests of individual classes, the interrupt initialization sequence (IIS) is set up by satisfying those individual conditions, and the interrupt processing is performed by software.

Hardware machine check (MC) mask clear status is obtained when MC is reset to 0, and when a machine check interrupt is allowed.

Machine checks that occur in the processing unit during instruction processing, IIS execution, or IOST processing, have the following characteristics:

- Exigent condition machine check is generated when the MC mask is set to 0 and current processing is interrupted. Machine check interrupt IIS is set up immediately at the exigent condition machine check level.

- Repressible condition machine check is generated when the MC mask is 0 and program exception item hardware mask (PX mask) is also 0. Machine check interrupt IIS is set up after executing the instruction at the repressible condition machine check level.

- Dual occurrence of program exception interrupt occurs when the PX mask is already set to 1 after a program exception interrupt has occurred. The interrupt processing of the current program exception is lost and the machine check interrupt IIS is set up instead at the program exception abnormal machine check level.

- Machine check interrupt requests that occur during IOST processing, are in two alarm classes:

  - Interrupt data error (IDE) during IOST processing sets the machine check at completion of instruction execution. In this condition, the MC mask and PX mask are both set to 0 (repressible condition machine check level).

  - During IOST processing, when an addressing exception item or storage protection exception item occurs during IOST CW access, the machine check interrupt IIS is set up after the completion of the instruction execution. The MC and PX masks are both set to 0 (repressible condition machine check level).

The factors for machine check interrupts are classified into these classes and are reported as machine check interrupt codes. Details of factors are reported further by machine check extended logouts.

When a repressible condition machine check occurs simultaneously with other factors, the repressible condition machine check is reported simultaneously with other machine check interrupts.

## Program Exception Interrupt

A program exception interrupt notifies the operating system of various exception items generated by instruction execution. Program exception items are classified in the following 16 classes and are reported as interrupt codes:

1.  Operation

2.  Privileged instructions

3.  EX instruction

4.  Storage protection

5.  Addresses

6.  Specification

7.  Data

8.  Fixed-point overflow

9.  Fixed-point divide

10. Decimal operation overflow

11. Decimal divide

12. Exponent section lower overflow

13. Exponent section upper overflow

14. Significance

15. Floating-point divide

16. Monitor

## Supervisor Call Interrupt

This interrupt is generated when the SVC instruction is executed. When the interrupt occurs, the interrupt decision cannot be controlled by the system mask in the current PSW.

**Interval Timer Interrupt** _____

An interrupt request by the interval timer is generated when the count in the interval
timer of the processing unit goes from:

- A positive value to 0 or to a negative value (model 8)

- 0 to a negative value (models 10/15/20)

The interrupt is permitted when both the:

- T bit of the system mask of the current PSW is set to 1.

- IIS is set up after the instruction is executed by the processing unit.

No interrupt occurs, however, until bit T changes from 1 to 0.

**Input/Output Status Tabler Interrupt** _____

An IOST interrupt request is generated when:

- Operation of the channel or input/output device is completed, or

- An error is detected during operation.

When an IOST interrupt occurs, the interrupt request is permitted when both the:

- IOST bit in the system mask of the current PSW is set to 1.

- IIS is set up after the current instruction is executed.

When this interrupt request is generated, pending status is maintained until the IOST bit
of the current PSW is set to 1 (assuming the IOST bit had been at 0).

**PER Interrupt** _____

An interrupt for program event recording (PER) is generated when the processing unit is
enabled for PER by contents of control registers 5, 6, and 7, and by PSW bit 19 (PER).
Also, one or more specific events must have occurred. Information identifying the event
is stored in main storage location X'1F0' to X'1F7' as part of the interrupt. Refer to 3.14
for further description of PER.

Before an interrupt request is generated and IIS is set up, reference is already made to
one of the following:

- The status of the system mask in the current PSW

- The program mask bit and status of the MC hardware mask

- PX hardware mask

These references determine the decision for an interrupt. When the MC or PX hardware mask is in set status, the interrupt controlled by MC or PX becomes pending or resorts to an unrecoverable error. Otherwise, the interrupt process level is changed. An interrupt occurring when the MC and PX masks are in clear status (and is not controlled by system mask or program mask) is allowed immediately after an interrupt request is generated.

### 3.7.2. Priority of Interrupt Requests

Individual interrupts are related by a pair of PSWs, called old and new PSW, that exist in the system fixed-storage area. Figure 3-34 illustrates the six system interrupt levels.

| BYTE 0 | OLD PSW 7 | 8 NEW PSW F |
|--------|-----------|-------------|
| 02X | INPUT/OUTPUT STATUS TABLER | INPUT/OUTPUT STATUS TABLER |
| 03X | MACHINE CHECK | MACHINE CHECK |
| 04X | PROGRAM EXCEPTION | PROGRAM EXCEPTION |
| 05X | SUPERVISOR CALL | SUPERVISOR CALL |
| 06X | INTERVAL TIMER | INTERVAL TIMER |
| 07X | (RESERVED) | (RESERVED) |
| 08X | PER | PER |
| 09X | (RESERVED) | (RESERVED) |

**Figure 3-34. PSW Position in Main Storage**

Interrupt requests of the IOST and interval timer have current PSW mask bits to control interrupt requests. Interrupt requests of the PER are controlled by the PER bit in the current PSW. Bits B, D, E, and S in the program mask of the current PSW also control masking of specific interrupt conditions on the program exception level.

Program exception interrupts, machine check, and supervisor call level other than those described, do not refer to masks of the current PSW. Also, supervisor calls do not require a mask as they are interrupt requests controlled by programs.

Each of these interrupt levels has a flip-flop corresponding to one or more interrupt requests. When an interrupt flip-flop is set by an interrupt request, interrupt priority to set the interrupt processing sequence is decided by the processing unit. Figure 3-35 shows the interrupt levels.

| Level | Interrupt Level | PSW Address (Hexa-decimal) | Interrupt Sublevel | Hard Priority | Mask | Instruction End Format | Remarks |
|-------|-----------------|----------------------------|--------------------|---------------|------|------------------------|---------|
| 1 | Machine Check Interrupt | 03X | Fault (exigent condition) | 1 | MC=0 | Suppress terminate | 1→MC (Check stop or abnormal stop when 0→P and MC =1 in accordance with corresponding LPSW) |
| | | | Alarm (repressible condition) | 6 | MC=0/ PX=0 | Complete | |
| | | | Program exception abnormality | 2 | MC=0 | Suppress; Terminate; complete | |
| 2 | Program Exception | 04X | Address | 3 | M C = 0 & P X = 0 | Terminate | 1→PX (O→P depending on corresponding LPSW). However, machine check interrupt is immediately set when PX=1 |
| | | | Data | | | Suppress | |
| | | | Decimal division | | | Suppress | |
| | | | Decimal upper overflow | | | Complete | |
| | | | EX instruction | | | Suppress | |
| | | | Exponent upper overflow | | | Complete | |
| | | | Exponent lower overflow | | | Complete | |
| | | | Fixed-point division | | | Suppress-Complete | |
| | | | Monitor | | | Complete | |
| | | | Fixed-point upper overflow | | | Complete | |
| | | | Floating-point division | | | Suppress | |
| | | | Operation | | | Suppress | Abnormal stop status is immediately set when MC=1 (ABN-STOP) |
| | | | Storage protection | | | Terminate | |
| | | | Significance | | | Complete | |
| | | | Specification | | | Suppress | |
| | | | Privileged instruction | | | Suppress | |

Figure 3-35. Interrupt Levels and Factors (part 1 of 2)

| Level | Interrupt Level | PSW Address (Hexa-decimal) | Interrupt Sublevel | Hard Priority | Mask | Instruction End Format | Remarks |
|---|---|---|---|---|---|---|---|
| 3 | Supervisor Call | 05X | | 4 | – | Complete | SVC |
| 4 | Interval Timer | 06X | | 7 | T=1 | Complete | Pending when T=0 |
| 5 | Input/Output Status Tabler | 02X | | 8 | IOST=1 | Complete | PSW pending when IOST=0 |
| 6 | PER Interrupt | 08X | | 5 | PER=1 | Complete | Interrupt is caused at an occurrence of PER |

**Figure 3-35.  Interrupt Levels and Factors (part 2 of 2)**

Hardware priority circuits select which interrupt request is to receive the interrupt initialization sequence for subsequent execution. All interrupt flip-flops are cleared when the interrupt initialization sequence is completed and the request line is searched. Mask bits in the current PSW become effective when all interrupt initialization sequences are completed.

Hardware interrupt requests are selected according to the following priorities:

1.  Exigent machine check interrupt request

2.  Exigent machine check interrupt request for program exception abnormality

3.  Program exception interrupt request

4.  Supervisor call interrupt request

5.  Program event recording interrupt request

6.  Repressible machine check interrupt request

7.  Timer interrupt request

8.  IOST interrupt request

Interrupts between priority ranks 1 and 4 are mutually exclusive. When an interrupt initialization sequence is completed, checks are again made for interrupt requests. Interrupt requests are controlled until the end of an interrupt initialization procedure, according to status of the mask bit in the current PSW. The contents of the final PSW, at IIS completion, determine how the decision is made on which interrupt is selected for

processing. This hardware priority selection method allows faster processing for higher priority interrupts.

Hardware selection of priority for interrupt requests are made when more than one interrupt request is received simultaneously. The order of the IIS is changed according to the mask bit of the current PSW as well as the interrupt requests generated during IIS execution. Occasionally, an interrupt request is generated for more than one reason. Under this condition, the hardware interrupt priority circuit determines which interrupt code should be inserted into the old PSW. Table 3-8 lists the interrupt codes.

## Table 3-8. Interrupt Code List

| Classification | Interrupt Code | Meaning |
|---|---|---|
| Machine check | 0 0 0 0 0 0 0 0 0 | Machine check interrupt has occurred and MCIC could be logged out. |
| | 1 1 1 1 1 1 1 1 | Machine check interrupt has occurred, and addressing exception item has occurred during MCIC logout so that MCIC could not be logged out correctly. |
| Program Exception Item | 0 0 0 0 0 0 0 1 | Operation exception item. Operation other than one normally required was tried. However, operation using overhead function not installed in the CPU was attempted. |
| | 0 0 0 0 0 0 1 0 | Exception item of privileged command. Privileged instruction was attempted while in problem mode. |
| | 0 0 0 0 0 0 1 1 | Execute instruction exception item. Instruction designated by execute instruction was again an execute instruction. |
| | 0 0 0 0 0 1 0 0 | Storage protection exception item. Storage protection exception has occurred. |
| | 0 0 0 0 0 1 0 1 | Addressing exception item. Addressing in program has a value larger than available storage. LCS instruction is excepted (model 8 only). |
| | 0 0 0 0 0 1 1 0 | Specification exception item as follows: <br><br> 1. Boundary error. <br><br> 2. Modifier field designated in STR instruction. <br><br> 3. R1 was odd when an even number + odd registers should be designated. <br><br> 4. When floating-point registers other than 0, 2, 4, and 6 were used. |

(continued)

## Table 3-8. Interrupt Code List (cont)

| Classification | Interrupt Code | Meaning |
|---|---|---|
| Program Exception Item (cont) | | 5. When numbers of digits for multipliers and divisors exceeded 15 in multiplications and divisions of decimal operations. |
| | | 6. When length of operand 1 was shorter or equal to operand 2 in decimal multiplications and divisions. |
| | | 7. Lower 4 bits were not zero in contents determined by R2 field in SSK and ISK instructions. |
| | | 8. Incorrect values were set in PSW. |
| | 0 0 0 0 0 1 1 1 | Data exception items: |
| | | 1. Incorrect codes and numbers in decimal number operations have been designated. |
| | | 2. Operands 1 and 2 in decimal number operations are duplicated in a wrong form. |
| | | 3. Upper section of operand 1 in decimal multiplications does not contain enough 0 digits to insert results. |
| | 0 0 0 0 1 0 0 0 | Fixed-point overflow. Overflow occurred as a result of operations in fixed point additions and subtractions. This interrupt is controlled by bit B of the current PSW. |
| | 0 0 0 0 1 0 0 1 | Fixed-point division exception. Quotient has overflowed into operand 1 in fixed point divisions. Results exceeded 31 bits in CVB instruction. |
| | 0 0 0 0 1 0 1 0 | Decimal operation overflow. Overflow occurred as a result of additions, subtractions, and ZAP in decimal operations. This interrupt is controlled by bit D of bit 37 in the current PSW. |
| | 0 0 0 0 1 0 1 1 | Decimal division exception. Quotient has overflowed in decimal divisions. |
| | 0 0 0 0 1 1 0 0 | Exponent section overflow. Exponent section has exceeded 127 in floating decimal operation. |
| | 0 0 0 0 1 1 0 1 | Lower exponent section overflow. Exponent section has become negative in floating-point .operation. This interrupt is controlled by bit E of bit 38 in current PSW. |
| | 0 0 0 0 1 1 1 0 | Exception item of effective numerical character. Mantissa section was 0 in final results of additions and subtractions of floating-point operations. This interrupt is controlled by bit S of bit 39 in the current PSW. |
| | 0 0 0 0 1 1 1 1 | Floating-point division and zero division. Mantissa section of divisors was 0 in floating-point division. |
| Others | 0 0 0 0 0 0 0 1 | Power off interrupt (model 8 only). |
| | 0 0 0 0 0 0 0 0 | IOST or PER (models 10/15/20 only) interrupt. |
| | 0 1 1 0 0 0 0 0 | Timer interrupt. |
| | I field | SVC interrupt. |
| Program Exception | 0 0 0 1 0 0 0 0 | Monitor interrupt. |

### 3.7.3. Interrupt Initialization Sequence

A PSW expresses the state of a given program in relation to the operating system. The current PSW is stored in the fixed area of the old PSW. This retains the state in which a certain interrupt has occurred while a program was in progress. At the same time, interrupt codes showing applicable interrupt types are stored in bits 24 through 31 of the old PSW according to the interrupt cause. After performing these operations, contents of the new PSW in the fixed area of main storage are transferred to the current PSW to produce a new program status.

When the current PSW is stored in the old PSW, contents of the corresponding new PSW are automatically transferred to the current PSW. This switching between programs is called an interrupt initialization sequence (IIS). Normally, when processing for an applicable interrupt is completed, the contents of the old PSW are stored in the current PSW. This function is executed by the load PSW (LPSW) instruction.

When a particular interrupt occurs that is allowed by the applicable mask of the current PSW, an initialization sequence is processed:

1.  Hardware generates the applicable level of interrupt request.

2.  The executing instruction is controlled in one of the following ways according to the interrupt type:

    ■ End the executing instruction (instruction complete). Results of the applicable instruction are guaranteed.

    ■ Suppress the executing instruction (instruction suppress). Results of the applicable instruction are not produced, and status immediately before executing the instruction is not guaranteed.

    ■ Stop the executing instruction (instruction terminate). Results of the applicable instruction are not guaranteed.

3.  When an IIS is running with a higher priority than the current interrupt, the lower priority interrupt is held pending until the processing for the higher priority interrupt is completed.

4.  The processing unit performs the following functions:

    ■ It stores interrupt codes showing causes for interrupt in bits 24 to 31 of the current PSW. The current PSW transfers its contents to the old PSW corresponding to the applicable interrupt level.

    ■ When the interrupt cause is the IOST, monitor (model 8 only), or timer level (model 8 only), the processing unit clears bits 24 to 31 to 0 of the old PSW corresponding to their respective interrupt levels.

5.  Contents of the new PSW corresponding to the interrupt level are stored in the current PSW. Bits 32 and 33 (ILC) of the current PSW are cleared to 0 by hardware.

6. New relocation values are decided by new relocation keys stored in the current PSW. The contents from the corresponding relocation registers in main storage are placed in the current relocation register.

7. The hardware interrupt priority circuit checks again if there is another request for an interrupt. Depending on the results, one of the following three cases is selected:

   ■ Return to step 3 when the interrupt request line is showing interrupt pending, and is set to 1 in the mask bit corresponding to the interrupt request.

   ■ In the LPSW (I2 = x 01) instruction, the next instruction is executed regardless of the interrupt instruction (except for exigent condition machine check, and program exception interrupt), and whether there is an interrupt request checked upon completing the instruction. When W mode is set to 1 in the PSW that was set in step 5, a waiting status is immediately set up.

   ■ In other instances, program execution is started under control of the current PSW, set as described in step 5, or of the current relocation register as set in step 6.

### 3.7.4. Instruction Execution with Interrupt Initialization

The interrupt initialization sequence is not performed in parallel with an instruction execution. The processing unit processes the IIS after ending the instruction cycle. The IIS starts after the instruction is completed or after forcing termination of a current instruction during execution. The type of interrupt determines the method of starting the IIS:

   ■ Instruction results are guaranteed when the processing unit starts the IIS when instruction execution is completed.

   ■ When the processing unit starts an IIS before an instruction is completed, the instruction becomes inhibited or is stopped. When inhibited, the results are not produced, but the status that existed immediately before instruction execution is guaranteed. The instruction address and instruction length code (ILC) of the current PSW is updated as if the instruction had been executed.

When processing is completed while in machine check interrupt or in program exception interrupt, the instruction address (IA) of the current instruction is inserted in the old PSW. In this case, the ILC of the old PSW is cleared to zero. However, in the SVC instruction, the next instruction address ILC = 01 is inserted in the old PSW.

### 3.7.5. Old PSW during Interrupt

When an interrupt occurs while executing an instruction, the instruction execution address is not cleared during the interrupt. To prevent an ambiguous address, the next address and current instruction ILC are prepared for the old PSW. An interrupt request for machine check, program exception item, supervisor call, or similar occurrence, inserts the address of the instruction word that should have been executed next into the old PSW. Table 3-9 lists the relationships between the ILC and instruction word.

**Table 3-9. Relationship of ILC and Instruction Word during Interrupt**

| ILC | PSW Bits 32 and 33 | Instruction Word Length | Instruction Word Format |
|-----|--------------------|-------------------------|-------------------------|
| 0 | 0 0 | Instruction completed | – |
| 1 | 0 1 | 2 bytes | RR |
| 2 | 1 0 | 4 bytes | RX, RS, SI |
| 3 | 1 1 | 6 bytes | SS |

When the interrupt request is generated, the instruction address results from deducting the ILC from bits 61 and 62 of the old PSW instruction address. If the ILC is other than 0, the instruction was either supressed or terminated. It is identified by the check bit in the interrupt code. Conversely, when the ILC is 0, the instruction was completed and the PSW instruction field shows the address of the instruction word scheduled to be executed next. In the supervisor call interrupt, the ILC remains set to 1, even after its service routine is completed. The address of the instruction scheduled to be executed next enters the instruction address field.

In an example of interrupt processing, assume that an interrupt request for the IOST has occurred (the input/output operation was terminated or an error occurred) while executing a problem program. The following conditions would result:

1.   An IOST interrupt request is made.

2.   Interrupt approval is determined with the interrupt approval condition (interrupt is approved when the IOST bit of the current PSW is 1 and processing is held in abeyance until the IOST bit becomes zero).

3.   The IOST interrupt request is approved and the IOST interrupt initialization sequence is set up when the current instruction completes.

4.   Contents of the current PSW are stored in the old PSW of the IOST level.
     A zero is then inserted in the interrupt code field of the old PSW.

5.   Contents of the new PSW for the IOST level are placed in the current PSW.

6.   The new SPR key in the current PSW selects the relocation register in the system fixed area of main storage.

7.   The selected relocation values of the relocation register are placed in the current relocation register.

8.   The value of this instruction address field becomes the top address in the interrupt analysis routine of the IOST. Interrupt initialization sequence is now ended. At the end of machine check interrupt initialization sequence, the MC hardware mask is set. At the end of the program exception initialization sequence, the PX hardware mask is set. The processing unit checks the next requested interrupt.

9. The IOST interrupt analysis routine by software is set up, starting with the instruction address of the current PSW.

10. Unless an interrupt request permitting an interrupt approval occurs (thus executing an interrupt analysis routine of the IOST by software), the load PSW instruction is issued at the end of this processing. In this case, step 2 is confirmed when an interrupt request is generated while executing this process routine. When the interrupt is approved, the process continues after step 3 is performed. Both old and new PSWs that are to be handled will correspond to their respective interrupt levels. When the interrupt is not allowed, a pending status must be set up or its effectiveness is lost.

11. When the old PSW instruction is issued, contents stored in the old PSW of the IOST level are placed in the current PSW.

12. The SPR key placed in the current PSW selects relocation registers in the system fixed area of main storage.

13. The relocation value of the relocation register is placed in the current relocation register. In case of a machine check interrupt, the MC or PX hardware mask is set at the end of the interrupt initialization procedure, or program exception interrupt will be cleared at the end of this load PSW. Processing of the interrupted problem program is restarted after executing this load PSW instruction.

Figure 3-36 shows a functional diagram of interrupt processing.
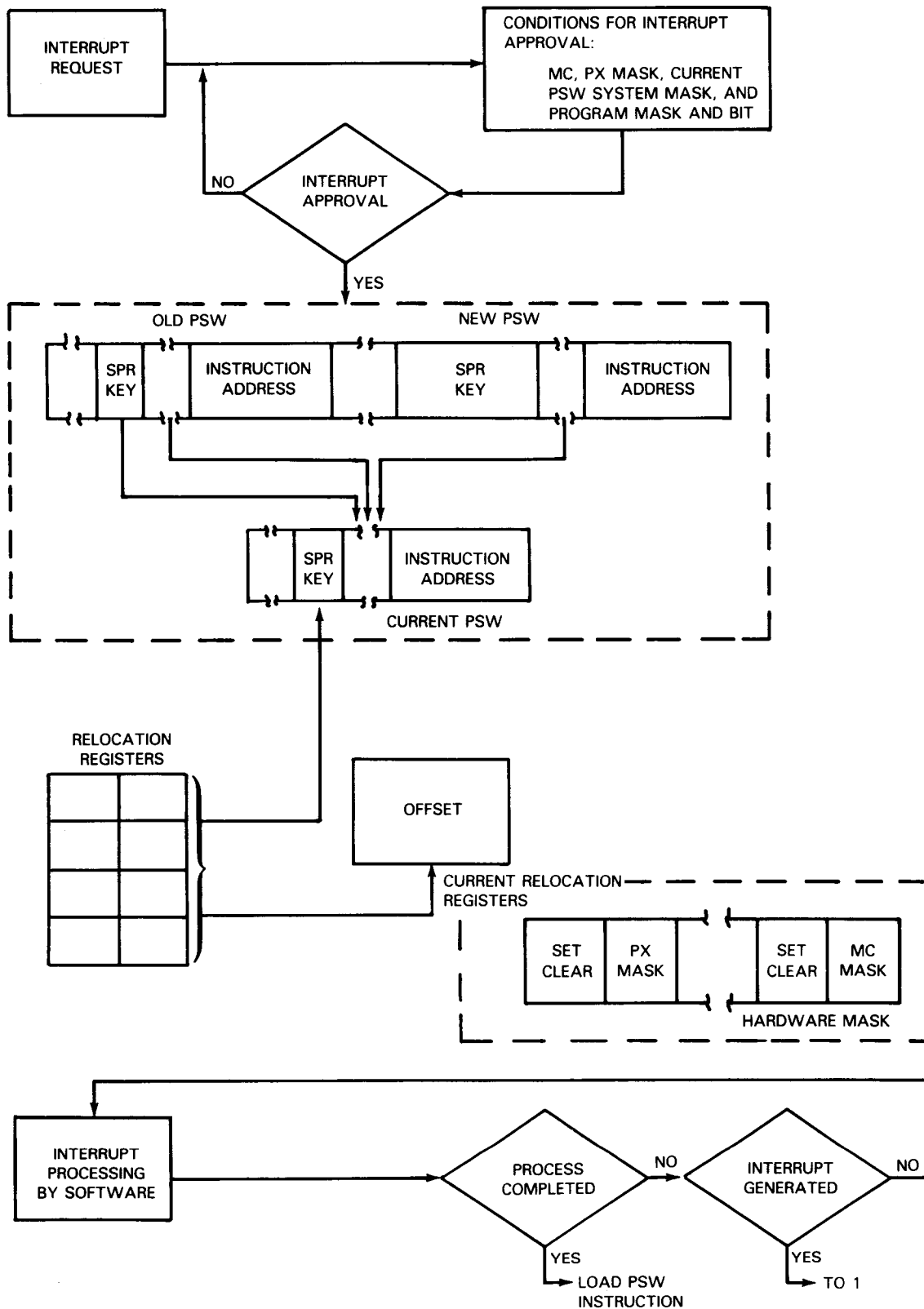
**Figure 3-36. Interrupt Processing Functional Diagram**

## 3.8. RESET

The operator at the console workstation can select the following reset modes:

- System reset

- CPU reset

- Initial program load reset clear

- Initial program load reset normal

- Power-on reset

Table 3-10 lists the reset types.

**Table 3-10. Reset Types**

| Operation | | Reset Type | Sense SW |
|---|---|---|---|
| Reset | System | System reset (main storage validate) | xxxx |
| | CPU | CPU reset (main storage invariable) | xxxx |
| Program Load | Clear | Initial program load reset clear (main storage clear) | 0000 |
| | Normal | Initial program load reset normal (main storage validate) | xx01 |
| Operator Recovery | | Initial program load reset normal (main storage validate) | xx10 |
| POWER ON Switch (when power is turned on) | | Power-on reset | 0000 |
| Automatic IPL | | Initial program reset normal (main storage validate) | xx11 |

NOTE:

xx indicates don't care.

Regardless of the processing unit operating status, all reset modes, as well as resetting, are normal. When in check stop status, reset stop status is cleared by a resetting operation. Table 3-11 presents the relationship between reset operations and reset types.

*NOTE:* *The current PSW, snap register, and current relocation register are saved in main storage fixed area (X'1A0'#'1EF') during system reset and initial program reset normal times.*

## Table 3-11. Relationship between Reset Operation and Reset Types

| Reset Section/Type | Reset | | Initial Program Reset | | Power-on Reset ③ |
|---|---|---|---|---|---|
| | System | CPU | Clear | Normal | |
| BPU status | S | S | L | L | R |
| BPU hardware | C/V | C/V | C/V | C/V | C/V |
| Fixed storage standby | 1A0 to 1EF ④ | – | – | 700 – BFF ⑤ | – |
| PSW | C | C | I① | I② | C |
| General purpose | V | V | C | V | V |
| Floating-point register | V | V | C | V | V |
| Control register | I | I | I | I | I |
| Snap register | C | V | C | C | C |
| Relocation register | C | C | C | C | C |
| Interval timer | V (off) | V (off) | V (off) | V (off) | V (off) |
| Main storage contents | V | U | C | V | C |
| Key storage | V | U | C | V | C |
| I/O relationship | R | U | R | R | R |
| Interrupt in CPU | C | C | C | C | C |

LEGEND:

S = Stop status
L = IPL operation is continuously performed after ending reset operation
R = Performs resetting of I/O system
I = Initial value is set
V = Sets correct check bits, but does not change the contents
C = Clears to 0 and sets correct parity bits
U = Not changed

NOTES:

① IOST mask is set to 1, and remaining bits are cleared to 0.

② MC mask is set to 1 (machine check interrupt inhibit status).

③ Control flags such as check and address stops in individual processors are also cleared.

④ Contents of PSW, RLR, and snap register are saved.

⑤ Contents from 0 to 4FF (hex) in the fixed storage are saved.

## 3.9. WAIT PATROL

When the processing unit is in wait state, it checks the internal registers and part of the operation functions. This is the wait patrol. If an error is found during this patrol, a machine check interrupt of the processing unit is immediately started.

Wait state is cleared when the interrupt is generated and execution state is set up.

## 3.10. INITIAL PROGRAM LOAD

The initial program load (IPL) reads programs from the I/O devices designated when program-load or operator-recovery instructions are selected at the console display.

When an IPL is designated:

1. The processing unit is in load condition. A request for IPL clear or initial program reset normal is sent to the processing unit. Contents 0 to 4FF (hex) in fixed storage are saved in location 700 to BFF (hex).

2. The following values are set in the fixed storage area of main storage:

|  | | | | |
|---|---|---|---|---|
| 0 to 7: | 0200<br>read | 0000<br>data<br>address | 6000<br>CC.SLI | 8000<br>byte<br>count | (CCW) |

|  | | |
|---|---|---|
| A0 to A3: | 00000000 | (CAW) for CHC/SEL |
|  | 0I000XXX | (CAW) for D MUX |

Where:

XXX = channel address specification.

3. The processing unit sends an SIO instruction to the designated I/O device.

4. Program loading is finished and channel end interrupt is returned from the I/O device when condition code is 00 (hex).

5. The IOST mask of the PSW is set to 1 (all others are set to 0).

6. The microprogram version (level) is stored in A4 to A7 (hex) of fixed main storage.

7. Device status of the buffered channel status word (BCSW) is checked, and IIS for IOST interrupt is executed unless the unit check bit is set to 1.

The same PSW normal operation as described previously is performed continuously:

- after turning power on;

- the AUTO IPL switch on the system console is turned on; and

- an automatic IPL is designated. (The I/O device address at that time uses the value designated by the configuration frame.)

If an error is detected while processing an IPL, the values illustrated in Figure 3-37 are stored in the snap registers and a stop state is set up. Contents of snap registers 0 and 1 are shown on the console display screen.
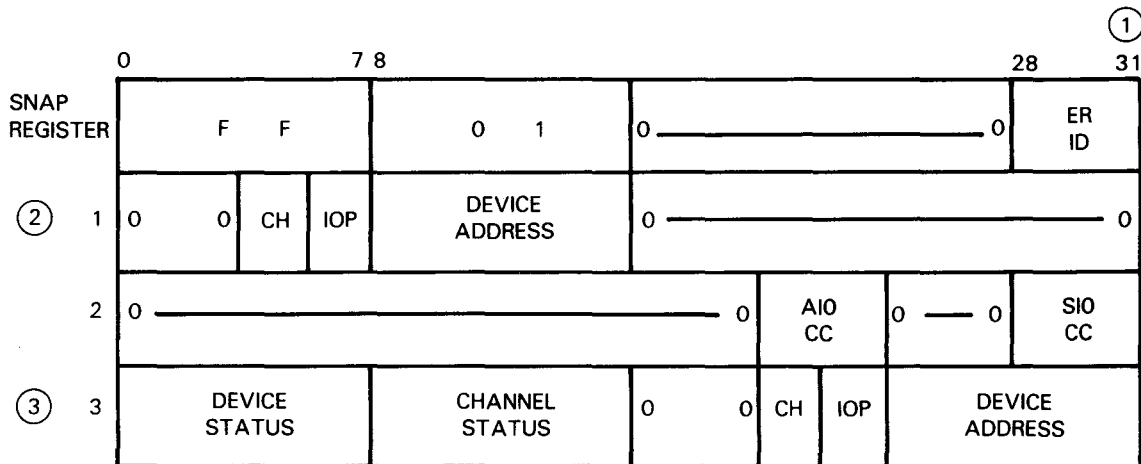


NOTES:

1. ERID: Error identification code

2. Address designated by IPL.

3. Status and address received at the end of IPL operation. When ER-ID is other than 6 ∿ B, 0 is set.

**Figure 3-37. Snap Register Field**

End statuses of the IPL devices are stored in BCSW in the main storage fixed area, when the IPL operation ends. Figure 3-38 shows the format.
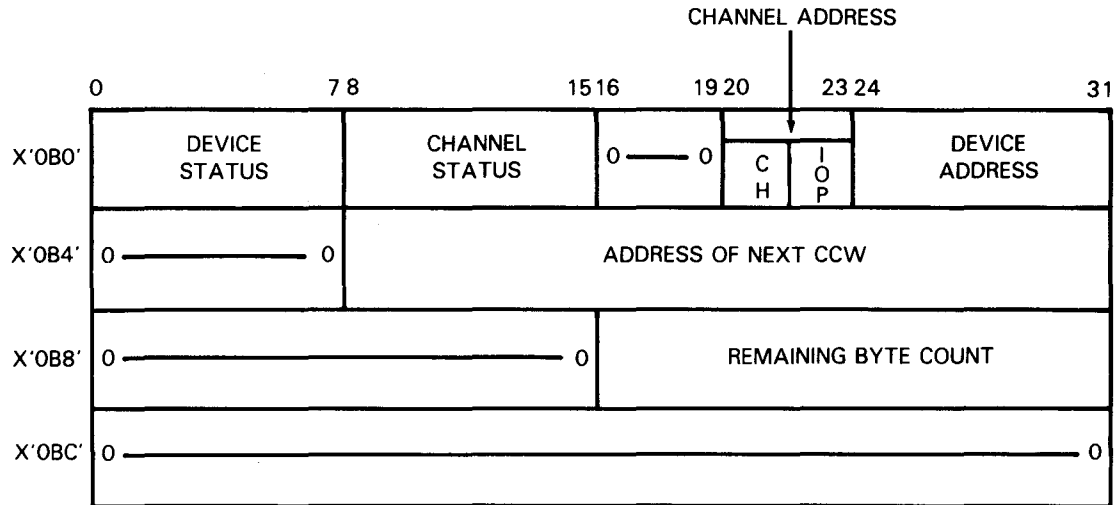


Figure 3-38. IPL End Status Fields

This information in the BCSW has a different format than the IOSTIW of the IOST. The SCP monitors overall time of IPL operation. An error is displayed on the console display screen unless the IPL completes in less than 10 seconds.

The IPL error identification code list is:

| ER-ID | = | 0 | Interface time-over condition is generated in the IPL function. |
|---|---|---|---|
| ER-ID | = | 1 | Interface time-over condition is generated in the SIO relative to the designated device. |
| ER-ID | = | 2 | Condition code of the SIO is not 100 (binary). |
| ER-ID | = | 3 | No interrupt identified in AIO against interrupt. |
| ER-ID | = | 4 | Interface time-over condition is generated in the same AIO. |
| ER-ID | = | 5 | Condition code of the same AIO is not 000X (binary). |
| ER-ID | = | 6 | Unit check status not identified in the status from the designated device. |
| ER-ID | = | 7 | IOST interrupt could not be started. |

| ER-ID | = | 8 | Interface time-over condition is generated in the IPL complete function. |
|-------|---|---|----|
| ER-ID | = | 9 | SCP timer up (10 seconds). |
| ER-ID | = | A | Invalid CH status is detected. |
| ER-ID | = | B | Invalid device status is detected. |

## 3.11. ADDRESS SEARCH STOP FUNCTION

This function can be assigned from the console display keyboard to any arbitrary storage access, including an instruction address or I/O operation.

### 3.11.1. Instruction Address Stop Function

The instruction address stop function assigns both:

- The PSW SPR key

- Leading relative byte address for the command address.

If the addresses coincide with each other during instruction execution, a stop state occurs immediately before executing that instruction. If this function is used, however, processing unit performance is reduced.

### 3.11.2. Arbitrary Address Stop Function

This function assigns the absolute address of a double word boundary for any arbitrary storage access, including I/O operations (that is, the lower 3 bits are ignored). If the address coincides, a stop state occurs after the instruction currently executing is complete.

*NOTE:    When using this function, excessive stop states can occur, as the comparison is made using a double word boundary address. A stop state can also occur because of a deviation in instruction execution timing, as the processing unit accesses commands in advance.*

## 3.12. FIXED AREA IN MAIN STORAGE UNIT

The first 4096 bytes of main storage are used by hardware and the operating system for special purposes. These bytes cannot be used as storage for ordinary data and instructions.

Figure 3-39 shows the format of these bytes.

| | 0  1  2  3 | 4  5  6  7 | 8  9  A  B | C  D  E  F |
|---|---|---|---|---|
| 0 0 X | CCW DURING IPL | | | |
| 0 1 X | IOSTCW 0 to 2 | | | PIAF |
| 0 2 X | IOST | OLD PSW | IOST | NEW PSW |
| 0 3 X | MACHINE INSPECTION | OLD PSW | MACHINE INSPECTION | NEW PSW |
| 0 4 X | PROGRAM EXCEPTION ITEMS | OLD PSW | PROGRAM EXCEPTION ITEMS | NEW PSW |
| 0 5 X | SUPERVISOR CALL | OLD PSW | SUPERVISOR CALL | NEW PSW |
| 0 6 X | INTERVAL TIMER | OLD PSW | INTERVAL TIMER | NEW PSW |
| 0 7 X | (RESERVED) | | (RESERVED) | |
| 0 8 X | PER | OLD PSW | PER | NEW PSW |
| 0 9 X | (RESERVED) | | (RESERVED) | |
| 0 A X | CAW | MICRO VERSION (CPU) | | (MONITOR AREA) |
| 0 B X | BCSW | | | |
| 0 C X | (RESERVED) | | | (RESERVED) |
| 0 D X | (MONITOR AREA) | | | (MONITOR AREA) |
| 0 E X ↓ 1 9 X | (RESERVED) | | | |
| 1 A X | CURRENT PSW SAVE AREA | | CURRENT RELOCATION REGISTER | |
| 1 B X | SNAP REGISTER    0 | 1 | 2 | 3 |
| 1 C X | 4 | 5 | 6 | 7 |
| 1 D X | 8 | 9 | A | B |
| 1 E X | C | D | E | F |
| 1 F X | PER IDENTIFICATION | | MONITOR CALL IDENTIFICATION | |

Figure 3-39. Fixed Areas of Main Storage (part 1 of 2)

| 20X | RELOCATION REGISTER 0 | RELOCATION REGISTER 1 | RELOCATION REGISTER 2 | RELOCATION REGISTER 3 |
|---|---|---|---|---|
| 21X | 4 | 5 | 6 | 7 |
| 22X | 8 | 9 | 10 | 11 |
| 23X | 12 | 13 | 14 | 15 |
| 24X | 16 | 17 | 18 | 19 |
| 25X | 20 | 21 | 22 | 23 |
| 26X | 24 | 25 | 26 | 27 |
| 27X | 28 | 29 | 30 | 31 |
| 28X | 32 | 33 | 34 | 35 |
| 29X | 36 | 37 | 38 | 39 |
| 2AX | 40 | 41 | 42 | 43 |
| 2BX | 44 | 45 | 46 | 47 |
| 2CX | 48 | 49 | 50 | 51 |
| 2DX | 52 | 53 | 54 | 55 |
| 2EX | 56 | 57 | 58 | 59 |
| 2FX | 60 | 61 | 62 | 63 |
| 30X ↓ 3FX | SYSTEM USE AREA | | | |
| 40X ↓ 4FX | SYSTEM USE AREA | | | |

Figure 3-39.  Fixed Areas of Main Storage (part 2 of 2)

## 3.13. FAULT DETECTION/STATUS DETECTION

The system has a variety of status detection functions used by service representatives. Fault state detection and processing protects the entire system or individual devices and ensures system reliability.

When a fault occurs, the SVP or relay panel on the system console processes the fault by one of the following:

■   Lighting an indicator

■   Sounding the alarm

■   Executing the power-off sequence

## 3.14. PROGRAM EVENT RECORDING

Program event recording (PER) assists in debugging programs. It alerts programmers to:

■   Successful execution of a branch instruction

■   Fetching of an instruction from designated main storage locations

■   Alteration of contents of designated main storage locations

The program has control over conditions that are considered events for recording purposes. It can selectively specify one or more events to be monitored. Information concerning a program event is provided through a PER interruption. The cause of the interruption is identified in arguments passed in the low-order main storage location (X'1F0' to X'1F7').

### 3.14.1. Control Register Allocation

Information for controlling PER resides in control registers 5, 6, and 7. Figure 3-40 illustrates these fields.

CONTROL REGISTER 5:

| E.M. | RESERVED |
|---|---|

0    2                                                                   31

CONTROL REGISTER 6:

|   | STARTING ADDRESS |
|---|---|

0               8                                                   31

CONTROL REGISTER 7:

|   | ENDING ADDRESS |
|---|---|

0               8                                                   31
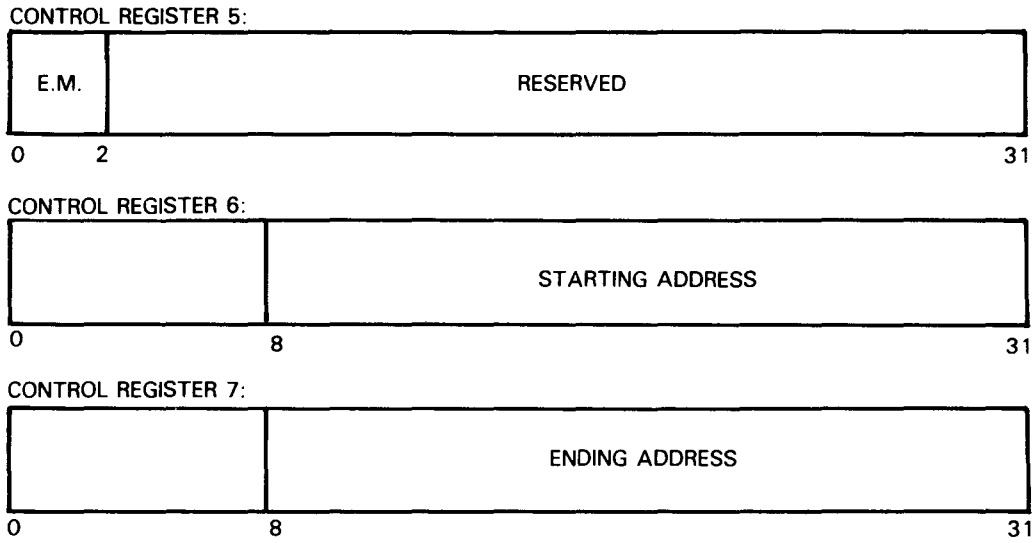
NOTES:

1. PER event mask bits 0 to 2 of control register 5 specify which events are monitored. The bits are assigned as follows:

    Bit 0: successful branching event

    Bit 1: instruction fetching event

    Bit 2: storage alteration event

    Bits 0 to 2, when 1', specify that the corresponding events are monitored. When the bit is 0, the event is not monitored.

2. PER starting address bits 8 to 31 of control register 6 form a logical address that designates the beginning of the monitored main storage area.

3. PER ending address bits 8 to 31 of control register 7 form a logical address that designates the end of the monitored main storage area.

**Figure 3-40. PER Control Fields**

The system operates at a reduced rate when monitoring:

- All program events (model 8), or

- Only instruction fetch (models 10/15/20)

Programs not utilizing PER should disable the facility by setting the PER mask in the PSW to 0. This ensures that processing unit performance is not degraded. Disabling PER by the masks and addresses in control registers 5 to 7 does not necessarily ensure that performance degradation won't occur.

### 3.14.2. Operation

PER is controlled by PSW bit 19. This is the PER mask. When the mask is 0, no program event can cause an interruption. When the mask is 1, a monitored event, as specified by contents of control registers 5, 6, and 7 causes an interruption.

An interruption due to a program event occurs after execution of the instruction responsible for the event. This event does not affect instruction execution, which can be completed, terminated, or suppressed.

A program event condition cannot be kept pending. When the processing unit is disabled for a particular program event at the time the event occurs, either by the mask in the PSW or the masks in control register 5, the interruption condition is lost.

A change in the PER mask in the PSW, or to PER control fields in control registers 5, 6, and 7 affects PER (starting with execution of the instruction that immediately follows).

A PER event causes an interruption if it occurs under all of the following conditions:

- During instruction execution

- When the processing unit is enabled for a PER event

- The processing unit is disabled by the instruction for that particular event.

A program event, when enabled, generates a PER. The old PSW is placed in main storage location X'80' and the new PSW is fetched from main storage location X'88'. Information describing the program event is loaded in main storage location X'1F0' to X'1F7'.

Figure 3-41 illustrates the information format.



MAIN STORAGE X'1F0'

| PER CODE | 0 | 0 |
|---|---|---|
| 0 | 2 3 | 31 |

X'1F4'

| 0 | 0 | PER ADDRESS |
|---|---|---|
| 0 | 7 8 | 31 |
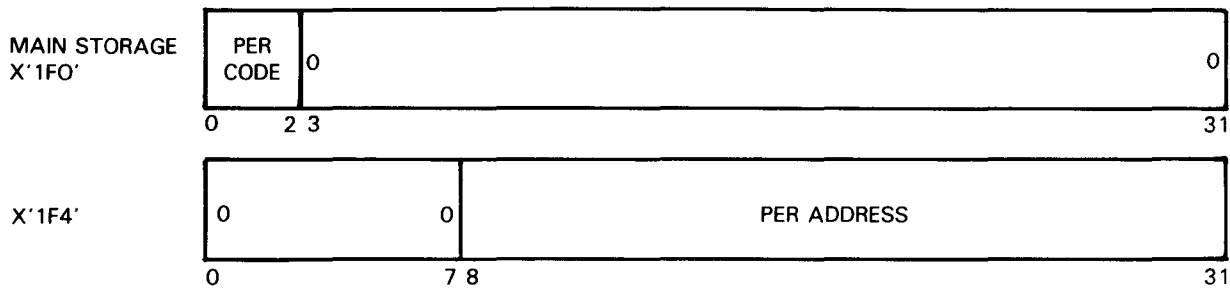
**Figure 3-41. PER Storage Format**

The event causing a program event interruption is identified by a 1 in bit position 0 to 2 of the PER code. The remainder of the bits in the code are set to 0s. The bit position in the PER code for a particular event is the same as the bit position for that event in the PER event mask field. When a PER interruption occurs and more than one designated program has been recognized, all recognized program events are concurrently indicated in the PER code.

The PER address in main storage location X'1F4' to X'1F7' identifies the location of the instruction causing the event. When an instruction is executed through the execute instruction, the address of the location containing the execute instruction is placed in the PER address field. In either case, the address of the next instruction to be executed is placed in the PSW. Zeros are loaded into bit positions 3 to 31 of main storage location X'1F0' to X'1F3' and into bit positions 0 to 7 of main storage location X'1F4' to X'1F7'.

**Interruption Priority**

The program event interruption occurs first when execution of an interruptible instruction is interrupted by:

- An I/O

- An interval timer, or

- A repressible machine check condition

The I/O, interval timer, or repressible machine check interruption is subsequently subject to control of mask bits in the new PSW. Similarly, when the processing unit is placed in stop state during execution of an interruptible instruction, an interruption for the pending PER condition occurs before the stopped state is entered. A PER condition can interrupt instruction execution without an associated asynchronous condition.

Instruction fetching during a supervisor-call instruction causes the PER interruption to occur immediately after the supervisor call interruption.

In the following two conditions, an instruction can cause a PER interruption as well as change the value of bits controlling the occurrence of a PER interruption for that particular event. The original values of the control bits determine whether a PER interrupt occurs:

1.    The instructions LPSW, supervisor-call and monitor-call can cause an instruction fetching event and disable the processing unit for PER interruptions. In addition, a program interruption can be recognized concurrently with a program event. This causes a PER interruption to immediately follow the program interruption PSW swap. In all these cases, the old PSW associated with the program event interruption can indicate that the processing unit was disabled for the interruption.

2.    The load-control instruction can cause an instruction fetching event and change the value of the PER event masks in control register 5, or the addresses in control registers 6 and 7, controlling indication of the instruction fetching event.

When a PER interruption is caused by branching, the PER address identifies the branch instruction (or the execute instruction, as appropriate). The old PSW points to the next instruction to be executed. When the interruption occurs during execution of an interruptible instruction, the PER address and the instruction address in the old PSW are the same.

## Storage Area Designation

Two program events: instruction fetching and storage alteration, involve the designation of an area in main storage. The storage area monitored for the references starts at the location designated by the starting address in control register 6 and extends up to and including the location designated by the ending address in control register 7. The area extends to the right of the starting address. The storage area is always designated by logical addresses.

The set of locations designated for monitoring purposes wraps around at location 16,777,215 (that is, location 0 is considered to follow location 16,777,215). When the starting address is smaller than the ending address, the set of locations designated for monitoring purposes includes:

■    The area from the starting address to the largest address in the system

■    The area from location 0 to (and including) the ending address

When the starting address is equal to the ending address, only the location designated by that address is monitored.

Main storage alteration and instruction fetching monitoring is performed by carrying out the address comparison on all 24 bits of the addresses.

## Successful Branching

Successful branch operation execution causes a PER interruption if bit 0 of the PER event mask field is 1 and the PER mask in the PSW is also 1.

A successful branch occurs when one of the following instructions passes control to the instruction designated by the branch address:

- Branch on condition                         (BC,BCR)

- Branch and link                             (BAL, BALR)

- Branch on count                             (BCT, BCTR)

- Branch on index high                        (BXH)

- Branch on index low or equal                (BXLE)

- Compare logical immediate and skip          (CLIS)

- Test under mask and skip                     (TMS)

The event is identified by setting bit 0 of the PER code to 1.

## Instruction Fetching

Fetching the first byte of an instruction from the main storage area designated by contents of control registers 6 and 7 causes a PER interrupt if both:

- Bit 1 of the PER event mask field is 1.

- The PER mask in the PSW is 1.

A program event is recognized when the processing unit executes an instruction whose initial byte is located within the monitored area. When the instruction is executed by the execute instruction, a program event is recognized when the first byte of the execute instruction or the subject instruction, or both, are located in the monitored area.
The event is identified by setting bit 1 of the PER code to 1.

## Storage Alteration

A PER interrupt occurs when the processing unit stores data in a main storage area designated by contents of control registers 6 and 7 if both:

- Bit 2 of the PER event mask field is 1.

- The PER mask in the PSW is 1.

Contents of main storage are considered altered when the processing unit executes an instruction that stores the whole operand, or part of it, within the monitored area of main storage. An alteration is considered to occur when storing takes place for purposes of indicating protection exceptions.

An arithmetic or movement operation:

- Fetches the operand

- Performs any indicated operation

- Stores the result

This method of storing into main storage constitutes alteration for PER purposes, even if the value stored is the same as the original value.

Implied locations referred by the processing unit during the following are not monitored:

- Interruption processing

- I/O instruction execution

- Machine check logout (including the PSW and logout locations)

These locations are monitored, however, when information is stored there explicitly by an instruction. Monitoring also does not apply to:

- Data storage by a channel

- Alterations made by the set-storage-key instruction (since the key storage area is not considered part of main storage)

The following instructions affect storage alteration as described:

- The store-characters-under-mask instruction does not alter a storage location when the mask is zero.

- The move-long instruction does not alter the storage location when the first operand length is zero.

- The shift-and-round-decimal instruction is always considered to alter the first operand location.

- The compare-and-swap-under-mask instruction is always considered to alter the second operand location.

An event is identified by setting bit 2 of the PER code to 1.

The following 38 instructions can cause a storage alteration event:

| MVCL | MVI | STCK | OC | UNPK |
|------|------|-------|------|------|
| STH | TS | STCTL | XC | ZAP |
| STC | NI | CSM | TR | AP |
| CVD | OI | STCM | ED | SP |
| ST | XI | MVN | EDMK | MP |
| STD | AI | MVC | SRP | DP |
| STE | SSTM | MVZ | MVO | |
| STM | STIDP | NC | PACK | |

## Events Concurrent with Other Interruptions

The following rules govern the indication of program events caused by:

- An instruction that also caused a program exception

- A supervisor call interruption

1. Indication of an instruction fetching event does not depend on whether the execution of the instruction was completed, terminated, suppressed, or nullified. The event, however, is not indicated when addressing or protection exception prohibits access to the instruction.

2. When an operation is complete, the event is indicated regardless of whether any program exception is recognized or not.

3. When instruction execution is terminated, storage alteration is indicated when the event occurs.

4. When a program exception or supervisor-call interruption is indicated concurrently with a program event, the PSW swap for the program or supervisor-call interruption is followed immediately by the PSW swap for the PER interruption. The PER old PSW will be the new PSW from the preceding PSW swap.

5. The PER interruption is delayed until the START key is pressed on the system console when a halt-and-proceed instruction that causes an instruction fetching event is executed.

6. When a repressible machine check is indicated concurrently with a program event:

- The PSW swap for the PER interruption occurs first

- Followed immediately by the PSW swap for the repressible machine check

When an exigent machine check occurs during the execution of an instruction which causing a program event, the program event is ignored and is not indicated.

Table 3-12 summarizes the program events that occur concurrently with other program interruption conditions.

## Table 3-12. Indications of Program Events

| Exception | Ending Type | Branch | Instruction Fetch | Storage Alter |
|---|---|---|---|---|
| Operation | S | – | X | – |
| Privileged operation | S | – | X | – |
| Execute | S | – | X | – |
| Protection |  |  |  |  |
|     Instruction | S | – | – | – |
|     Operand | S or T | – | X | X |
| Addressing |  |  |  |  |
|     Instruction | S | – | – | – |
|     Operand | S or T | – | X | X |
| Specification |  |  |  |  |
|     Odd instruction address | S | – | – | – |
|     Invalid PSW format | C | – | X | – |
|     Other | S | – | X | – |
| Data | S | – | X | – |
| Fixed-point overflow | C | – | X | X |
| Fixed-point divide |  |  |  |  |
|     Division | S | – | X | – |
|     Conversion | C | – | X | – |
| Decimal overflow | C | – | X | X |
| Decimal divide | S | – | X | – |
| Exponent overflow | C | – | X | – |
| Exponent underflow | C | – | X | – |
| Significance | C | – | X | – |
| Floating-point divide | S | – | X | – |
| Monitor | C | – | X | – |

LEGEND:

C = The operation or, in the case of the interruptible instructions, the unit of operation is completed.

S = The operation or, in the case of the interruptible instructions, the unit of operation is suppressed.

T = Execution of the instruction is terminated.

X = The event is indicated along with the exception if the event has occurred; that is, contents of the monitored storage location were changed, or an attempt was made to execute an instruction whose first byte is located in the monitored area.

– = The event is not indicated.

Execution of the move-long (MVCL) and compare-logical-long (CLCL) interruptible instructions can cause an event for instruction fetch. Additionally, MVCL can cause the storage alteration event. Since execution of MVCL and CLCL can be interrupted, a program event can be indicated more than once. It may be necessary, therefore, for a program to remove the redundant event indications from PER data. The following rules govern the indication of the applicable event during execution of these two instructions:

1.   The instruction fetching event is indicated when the instruction is fetched for execution, regardless of whether it is the initial execution or resumption.

2.   The storage alteration event is indicated when the instruction is fetched for execution, regardless of whether it is the initial execution or resumption. No special indication is provided on premature interruptions as to whether the event will occur again upon resumption of the operation. The event for an address match on data storing for a single byte location can be recognized only once in execution of move-long instruction.

A program generally does the following to delete redundant entries in PER data for the MVCL and CLCL instructions, so that only one entry for each complete execution of the instruction is obtained:

1.   Check to see if the PER address is equal to the instruction address in the old PSW, and if the last instruction executed was MVCL and CLCL.

2.   If both conditions are met, delete instruction-fetch events.

3.   If both conditions are met, and the event is storage alteration, delete the event if the count for the destination operand is not zero.

# 4. Machine Check Control

Machine check control lets the system automatically recover from faults through program recovery processing. Diagnostic information obtained during this processing is recorded for maintenance.

## 4.1. MACHINE CHECK DETECTION

Machine checks are reported by machine check interrupts.

Machine check detection is performed during all:

- Processing

- Address relocation

- Control of instructions

- Main storage referencing

Generally, redundancy is provided in each data item and a check is made of previously stored and transferred data. More than one redundancy bit (called a check bit) is added to each data word. The data bit, together with check bits, form the check block.

If a check block contains only one bit, this bit is also the parity bit. A check block having only one bit can only detect errors. A check block having two or more check bits can also correct errors.

A check block consists of check block codes (CBCs), which are correct only if they contain no errors.

## 4.2. RECOVERY FUNCTION

Faults detected by a machine check are automatically corrected and the operation is recovered by one of the following:

- Correction by redundancy

- Processing unit retry

- Degradation (models 15 and 20)

### 4.2.1. Correction by Redundancy

Main storage has a redundancy function called error checking and correction (ECC) that allows for error correction.

When data is supplied from main storage, it is confirmed by the main storage unit (MSU). If an error is detected in a bit, data is rewritten in the MSU. Corrected data is supplied to the processing unit or the input/output processor (IOP). A machine check occurs if an error greater than two bits is detected but not corrected. As a result, the program for processing a machine check interrupt can locate the error address from the fixed logout information.

Figure 4-1 illustrates the save and logout areas of main storage.

| 50X ⟶ 6FX | SYSTEM USE AREA |
|---|---|
| 70X ⟶ BFX | X '000' – X '4FF' SAVE AREA |
| COX ⟶ FFX | (SYSTEM LOGOUT AREA) |
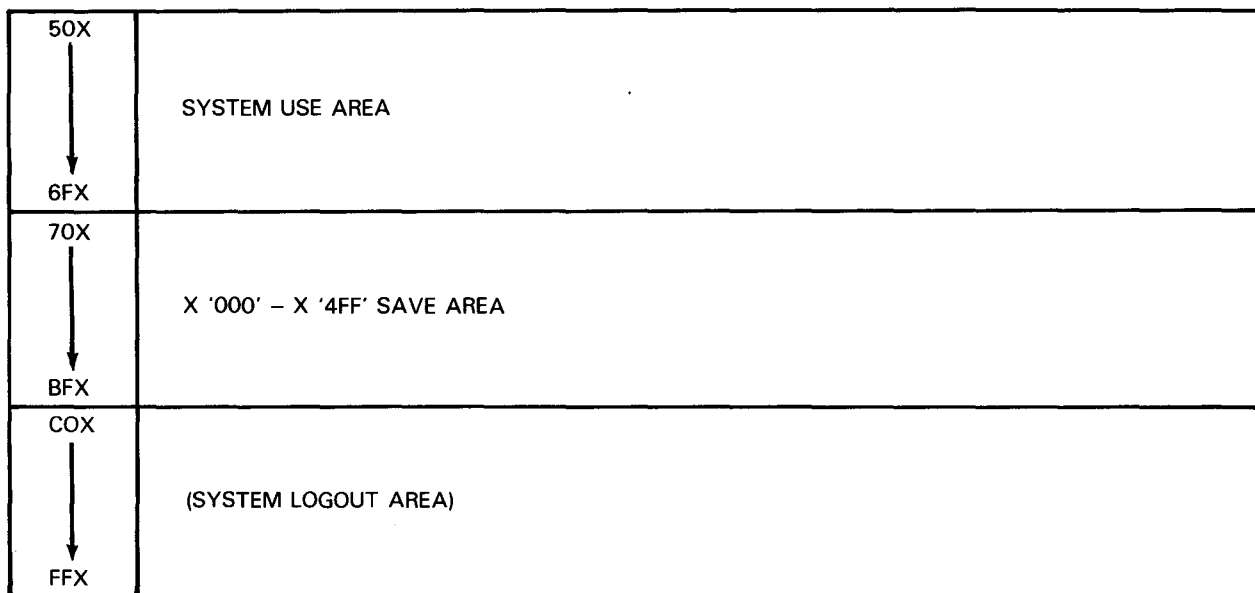
**Figure 4-1. Main Storage Save and Logout Areas**

### 4.2.2. Processing Unit Retry

The processing unit stores information when executing each instruction. If an error occurs during instruction execution, the processing unit reexecutes the instruction according to this stored information. The processing unit will try to reexecute the instruction up to 15 times.

If a normal state is regained as a result of a successful retry, a machine check interrupt occurs as a recording error repressible condition. If an error continues after 16 tries, it is considered a permanent error and the retry is unsuccessful.

If a retry cannot be performed when the error occurs (contents of the required registers and storage are updated), the retry is considered impossible. If a retry is unsuccessful or impossible, a machine check interrupt exigent condition occurs and recovery must be performed by the program.

### 4.2.3. Degradation (Models 15 and 20)

Degradation occurs when an error disables one of the following models 15 and 20 components:

- Micro accelerator (Model 15 only)

- Instruction cache (Model 20 only)

- Operand cache (Model 20 only)

- Floating point processor (Model 20 only)

These components can be disabled by either the hardware or software.

**Hardware Disabling**

The hardware can automatically disable the component when it detects an error. When it does:

- Machine check interrupt is reported as a degradation condition.

- This condition is considered an exigent condition machine check.

- BPU processing is incorrect at the time the degradation occurred.

**Software Disabling**

Whenever an error is detected in one of the components, the hardware automatically replaces the check block (the error data) with a correct check block. The recovery result is reported as a repressible condition machine check interrupt.

However, this error could be detected again in later processing. The software disables the component if the error count exceeds the permitted limit. The software disables the component by executing a degradation control instruction (DGC). The error is no longer detected in this degraded condition.

**Resetting the Component** _____

The degradation state is normally reset by one of these reset operations:

■    System reset

■    BPU reset

■    IPL-CLEAR

■    IPL-normal

■    Power on reset

The reset can fail, however, if the component is improperly installed or if it fails the power on confidence test.

## 4.3. MACHINE CHECK CONTROL

A machine check occurs only as a result of a machine malfunction. It does not occur from data errors in programs or instructions. However, a program exception item that occurs while the program exception (PX) mask bit is 1 results in a machine check. Machine checks from data or instructions are avoided by writing the correct check block code (CBC) in various registers, storage key, and main storage unit when a power-on reset or other reset is performed.

A machine check indicates whether an operation is adversely affected by an incorrect CBC or if there is another factor prohibiting normal operation. An incorrect CBC requires that the entire block be replaced. If an incorrect CBC is detected during input/output operations, a machine check interrupt occurs and the input/output operation is terminated.

Depending on the machine check location, automatic recovery is sometimes performed by hardware, or the interrupt is sent out as an exigent condition to permit processing by software.

A machine check is indicated by one of the following:

- A machine check interrupt

- IOST machine check interrupt

- A processing unit check stop

*NOTE:*    *A machine check does not occur if an MSU, input/output processor, or input/output device is assigned but not installed. A machine check is indicated, however, by a program exception interrupt or condition code.*

### 4.3.1. Incorrect CBC Control of Main Storage

The check block is made up of data bits and the check bit.

- Model 8

  The model 8 main storage check block is eight bytes long. Data in main storage is comprised of 64 bits of data and 8 bits of ECC code. Figure 4-2 shows the data format used by the model 8.

INSIDE MAIN STORAGE

8-BYTE PORTION (72 BITS)                8-BYTE PORTION (72 BITS)

| 64-BIT DATA | 8-BIT ECC CODE | 64-BIT DATA | 8-BIT ECC CODE |
|---|---|---|---|

OUTSIDE MAIN STORAGE

8-BYTE PORTION (72 BITS)                8-BYTE PORTION (72 BITS)

| | P (1) | | 8-BIT DATA | P (1) | 8-BIT DATA | P (1) | | | 8-BIT DATA | P (1) |
|---|---|---|---|---|---|---|---|---|---|---|
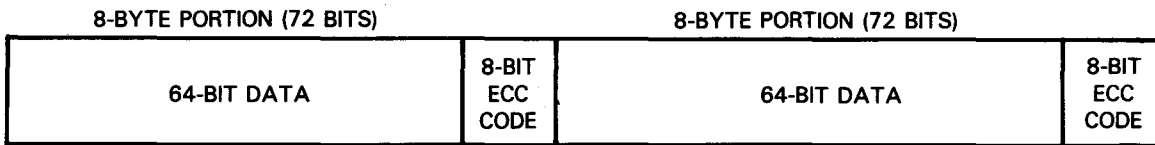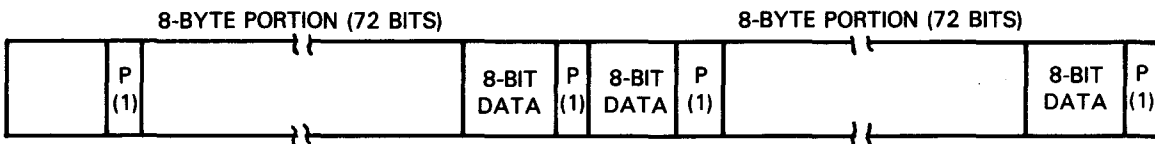
LEGEND:

P = Parity bit (1 bit)

**Figure 4-2. Data Format Used in and out of Main Storage on Model 8**

■    Models 10/15/20

The models 10/15/20 main storage check block is four bytes long. Data in main storage is comprised of 32 bits of data and 7 bits of ECC code. Figure 4-3 shows the data format used by the models 10/15/20.

INSIDE MAIN STORAGE

4-BYTE PORTION (39 BITS)                4-BYTE PORTION (39 BITS)

| 32-BIT DATA | 7-BIT ECC CODE | 32-BIT DATA | 7-BIT ECC CODE |
|---|---|---|---|

OUTSIDE MAIN STORAGE

4-BYTE PORTION (36 BITS)                4-BYTE PORTION (36 BITS)

| 8-BIT DATA | P (1) | | 8-BIT DATA | P (1) | 8-BIT DATA | P (1) | | | 8-BIT DATA | P (1) |
|---|---|---|---|---|---|---|---|---|---|---|
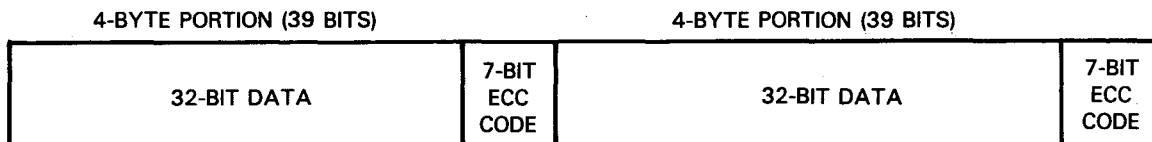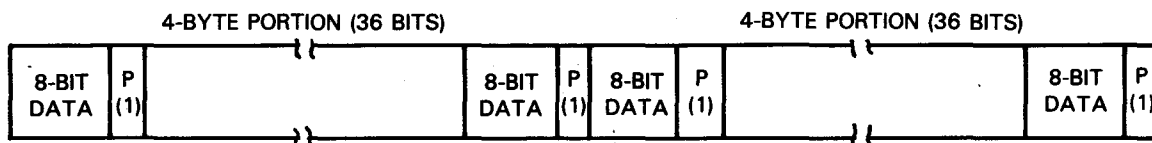
LEGEND:

P = Parity bit (1 bit)

**Figure 4-3. Data Format Used in and out of Main Storage on Models 10/15/20**

If the CBC is correct, data from main storage has one parity bit added to each eight bits. When storing part of a block containing incorrect CBC, data in the block, including the check bit, remains with the error and the new data is not stored. Contents in the block are changed only when the entire block is stored in a single store operation.

An incorrect CBC in main storage cannot be corrected. The particular block with the incorrect CBC must be stored again.

This method of correcting CBC, called memory validation, is done by:

■ Program

■ I/O operation, or

■ Resetting the system with a CLEAR command at the system console

The store-multiple (STM) and the supervisor-store-multiple (SSTM) instructions are used in memory validation by program. This is possible, however, only when the address indicated in the second operand is within the 8-byte (model 8) or 4-byte (models 10/15/20) boundary.

### 4.3.2. Incorrect CBC Control of Key Storage

Key storage consists of a check block of 8 bits including:

■ Six storage key bits

■ One read protection flag (RPF) bit

■ One parity bit

Figure 4-4 is the key storage format.

| KEY<br>(6) | RPF<br>(1) | P<br>(1) |
|---|---|---|
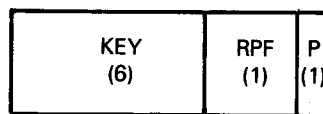
LEGEND:

KEY      Storage key
RPF      Read protection flag
P        Parity bit

**Figure 4-4. Key Storage Format**

If storing and fetching are performed when the SPR key is 0, normal operations are performed even if the storage key has an incorrect CBC.

With the SPR key on 0, storage is referenced by both:

■    An I/O operation during initial program load (IPL)

■    An operation from the store/display frame at the system console

A storage key with an incorrect CBC is corrected by the set-storage-key (SSK) instruction.

Table 4-1 lists the operations performed with an incorrect CBC in the storage key.

**Table 4-1.  Control of Key Storage with Incorrect CBC**

| Type of Reference | Key Storage Operation with Incorrect CBC |
|---|---|
| Set-storage-key instruction | Completed, corrected |
| Insert-storage-key instruction | PD, uncorrected |
| Fetch operation (nonzero SPR key) | MC, uncorrected |
| Store operation (nonzero SPR key) | MC, uncorrected |
| Fetch operation (SPR key zero) | Completed, uncorrected |
| Store operation (SPR key zero) | Completed, uncorrected |

LEGEND:

Completed      Instruction execution is completed normally. Machine check interrupt does not occur.

PD             If an incorrect CBC is still detected after 16 retries, or instruction processing damage interrupt occurs. If a retry is successful, a machine check interrupt repressible condition (SR = 1, KE = 1) occurs.

MC             BPU detects as PD. For I/O, ED (IED, IEDS = 10) is reported to BPU. Contents of storage are not changed.

Corrected      New storage key and read protection flag are set and CBC is corrected.

Uncorrected    Key storage remains as is, and the incorrect CBC remains.

### 4.3.3. Incorrect CBC Control of Registers

Incorrect CBC control affects the processing unit register stack (general register, control register, floating-point register, etc). If an incorrect CBC is detected in any of these registers, the contents of the registers are stored in the logout area while the machine check interrupt is processed. Double machine check does not occur for incorrect CBCs detected during a store operation for this interrupt. If an incorrect CBC is present in stored information, however, it is indicated by the machine check interrupt code (validity bit). A register with an incorrect CBC is corrected while processing the machine check interrupt.

A machine check interrupt occurs even if an incorrect CBC is detected in an unused portion of a register. This occurs during execution of an instruction that refers to this portion of the register (that is, load half word).

In addition, the program is not required to correct an incorrect register CBC. It is corrected while processing the machine check interrupt function.

## 4.4. CHECK STOP STATE

A check stop state occurs if an error in the processing unit prevents operation from continuing. Execution of all instructions, interrupts, and I/O operations is stopped if a check stop state occurs. The CHECK STOP indicator on the system console lights to inform the operator of a check stop state. The processing unit reset function releases check stop state.

The following processing unit errors cause a check stop state:

■  An exigent condition machine check occurs under either of the following conditions while control register 14 check stop control bit is 1:

  -  Processing unit is suppressing a machine check interrupt; machine check (MC) mask bit is 1. (Machine check interrupt is being processed.)

  -  During IIS of an exigent condition machine check interrupt or during storing of machine check interrupt code (MCIC) or logout information.

■  Control register 14 check stop control bit is 0. If any exigent condition machine check occurs during an exigent condition machine check interrupt (during the IIS or logout operation), then machine check interrupt has occurred again. The machine check persists, even after repeatedly processing this operation up to 31 times.

■  Any exigent condition or repressible condition machine check occurs while a check stop mode is set from the system console.


## 4.5. ABNORMAL STOP STATE

An abnormal stop state occurs when a program exception prevents operation from continuing in the processing unit. Execution of all instructions, interrupts, and I/O operations is stopped if an abnormal stop state occurs. The STOP indicator on the system console lights to inform the operator of the abnormal stop state. A reset operation releases the abnormal stop state.

An abnormal stop state occurs when:

■  A program exception interrupt request is made while the MC hardware mask bit is set to 1 (during machine check interrupt processing).

■  An error occurs on the I/O interface during machine check interrupt IIS.

## 4.6. TYPES OF MACHINE CHECKS

There are three types of machine checks:

- Exigent condition

  Occurs when an error remains even after retry and hardware recovery processing are performed, or when a retry cannot be made. The instruction currently executing, interrupt initialization, and IOST are all discontinued and a machine check interrupt occurs.

- Repressible condition

  Indicates completion of recovery of a temporary error by hardware, or an abnormal state that does not directly affect execution of instructions. A machine check interrupt occurs when the current instruction execution is completed.

- Program exception

  Occurs when a program exception interrupt is repeated during the processing of same (that is, program exception (PX) mask bit is set to 1). The instruction currently executing is terminated, completed, or suppressed, and a machine check interrupt is raised immediately.

### 4.6.1. Exigent Conditions

The types of exigent condition machine checks are:

- System damage

- Instruction processing damage

- Degradation (models 15 and 20)

**System Damage** _____

System damage (SD) is an unrecoverable damage independent of instruction processing by the processing unit (that is, independent of the instruction indicated by the old PSW instruction address stored when the machine check interrupt occurred). This condition is indicated by machine check interrupt code (MCIC) SD bit (bit 0).

System damage occurs when:

- It is impossible to identify the damage location, or

- An error is detected by hardware when the processing unit is in interrupt initialization, IOST, or in wait state.

System damage cannot be recovered by programming.

## Instruction Processing Damage

Instruction processing damage (PD) is damage that accompanies instruction execution (that is, by the instruction indicated by the old PSW instruction address when the machine check interrupt occurs). This condition is indicated in the MCIC PD bit (1 bit).

Instruction processing damage can be:

- Processing unit error (retry impossible, retry unsuccessful)

- Storage 2-bit error

- Key storage error

- I/O interface error (interface parity error: IPR)

- Time-out on the instruction stall timer

If the retry is possible at the time of error in the processing unit, the corresponding instruction is retried. If retry is impossible or unsuccessful after attempting the instruction 16 times, an instruction processing damage machine check interrupt occurs. If an error is detected by the processing unit on the I/O interface, an instruction processing damage machine check interrupt occurs immediately.

Time-out on the instruction stall timer occurs when time for execution of the instruction is surpassed. The timer begins operation when instruction execution starts, but if the instruction is not completed within 4 milliseconds, an instruction processing damage machine check interrupt occurs.

The MCIC backup bit (bit 7) is set to 1 to indicate that:

- Damage recovery information for this interrupt is stored.

- Retry of the instruction is possible.

The validity bits TCV and LOV are set to 1.

The specific type of error in the instruction processing damages listed is indicated by the machine check code. In a storage 2-bit error and key storage error, the actual address in main storage is indicated by the machine check interrupt code.

**Degradation**

This exigent condition machine check applies only to models 15 and 20.

During a degradation condition (DG), BPU processing is incorrect and the failing component is disabled.

If machine check interruption occurs, degradation, as well as one of the following, is indicated in the MCIC:

■   System damage (SD)

■   Instruction processing damage (PD)

The errors that cause a degradation condition are:

■   Micro accelerator error (MAE)

    If detected during instruction execution, both DG and PD are reported and bit 14 (MAE) of the MCIC is set to 1.

■   Instruction cache error (ICE)

    If detected during instruction execution, both DG and PD are reported and bit 14 (ICE) of the MCIC is set to 1.

■   Operand cache error (OCE)

    If detected during instruction execution, both DG and PD are reported and bit 15 (OCE) of the MCIC is set to 1.

    If detected during processing other than instruction execution, both DG and SD are reported and bit 15 (OCE) of the MCIC is set to 1.

■   Floating point processor error (FPE)

    If detected during execution of floating point instructions and certain general instructions, both DG and PD are reported and bit 17 (FPE) of the MCIC is set to 1.

### 4.6.2.  Repressible Conditions

There are three types of repressible condition machine checks:

■   System recovery

■   External damage

■   Warning

## System Recovery

System recovery (SR) occurs as a result of either of these two conditions:

- Successful instruction retry (SR = 1, SC = 0)

  If the SR bit is 1 and SC bit (bit 10) is 0, then the instruction retry was unsuccessful and operation is continuing normally.

- Storage 1-bit error (SP = 1, SC = 0)

  If the SR bit and SC bit are set to 1, a 1-bit error occurred in storage. If the 1-bit error in storage occurs during an I/O operation, the operation is normally completed independently of the I/O interrupt, but a system recovery machine check interrupt also occurs. The physical address is reported to FMA (bits 40 to 63) of MCIC at the time the 1-bit error occurs. In addition, a 1-bit error machine check interrupt request can be controlled by the SM bit (bit 5; storage 1-bit error mask) of control register 14, with the interrupt request made only when the SM bit is 1.

## External Damage

External damage (ED) occurs when an error occurs during an I/O operation or in the TOD clock, or abnormal state occurs during IOST by the processing unit and damage is indicated by the MCIC ED bit (bit 4). The four error conditions are:

- I/O operation error (ED = 1, IED = 1)

  If the ED bit and the IED bit (bit 25) are both set to 1, then a 2-bit storage error (SE bit = 1), key storage error (KE bit = 1), or a channel hardware error is indicated. A machine check interrupt is used for collecting logout information. Recovery cannot be performed by programming, but is done through the I/O interrupt processing function.

  In addition, the channel address (CH address, IOP address) and storage address where the error occurred are reported to MCIC CHA (bits 32 to 35) and to FMA.

- Time-out on interface stall timer (ED = 1, IOT = 1, IED = 1)

  If the ED bit, IOT bit (bit 19), and IED bit are all set to 1, then a time-out at the I/O interface stall timer occurred during I/O instruction, control instruction, or IOST processing.

  A time-out is approximately 4 ms long.

  Channel address and I/O functions executing at time-out are reported to MCIC, CHA, and FMA, respectively.

- TOD clock error (ED = 1, TED = 1)

  If the ED bit and the TED bit (bit 24) are both set to 1, then an error in the TOD clock is indicated.

- IOST abnormal (ED = 1, IOST = 1, CWE = 0/1)

    If the D bit and IOST BIT (bit 22) are set to 1, and CWE bit (bit 21) is 0, then an error is indicated in main storage during BCSW readout or during IOSTIW readout/write of IOST processing. When the IOSTSW IDE is also 1, the start of an IOST interrupt is indicated. In this case, machine check interrupt is used for collecting logout information. Recovery by program is not performed. Recovery is done by the IOST interrupt. The storage address where the error occurred is reported to MCIC FMA.

    If the ED bit, IOST bit, and CWE bit are all set to 1, then an address exception or storage protection exception in IOSTCW, that occurs during IOST processing, is indicated.

In external damage, the first three conditions can be controlled by using control register 14 EM bit (bit 3) (an interrupt request authorization is obtained when EM = 1).

Warning _____

A cooling device abnormality causes a warning (W) indication. This warning, indicated by the W bit (bit 6) set to 1, occurs when there is an abnormal state in the computer cabinet cooling device (for example, the fan is obstructed or defective).

### 4.6.3. Program Exception

A program exception machine check interrupt occurs only as a result of a program error. The PEX bit (bit 3) is 1.

A program exception machine check interrupt request occurs when any program exception is repeated during program exception interrupt processing (that is, the PX mask bit is set to 1). Both the final interrupt code and interrupt address are reported to snap register 7 in information that was logged out during machine check interrupt. The code for cause of the second program exception interrupt is then reported to snap register 8.

## 4.7. SUBCLASS MASK OF REPRESSIBLE CONDITION MACHINE CHECKS

Software can prevent a machine check interrupt when a repressible condition occurs. This control is provided by the subclass mask bits found in control register 14. These bits correspond to specific repressible conditions.

When a bit is 0, the repressible condition is held or pending. During this time:

■   The machine check interrupt does not occur.

■   The associated logout is not executed.

When a bit is set to 1, the repressible condition is not held:

■   The machine check interrupt occurs.

■   The associated logout is executed.

The initial value of these bits is 0.

Figure 4-5 shows the format of control register 14.

CONTROL REGISTER 14
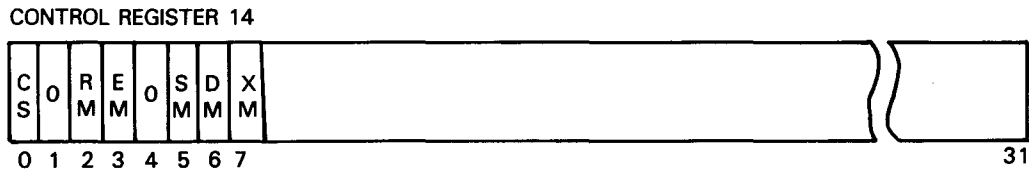


**Figure 4-5.  Control Register 14 Format**

The definitions of the significant bits in this register are:

■   Bit 0 - Check stop control bit (CS)

    Not used as a subclass mask bit.

■   Bit 2 - System recovery bit (RM)

    Controls system recovery interruption conditions except 1 bit memory error correction conditions, micro accelerator errors (MAE), and cache repressible machine checks (OCE, ICE).

■   Bit 3 - External damage bit (EM)

    Controls external damage interruption conditions except input/output status tabler abnormal conditions.

- Bit 5 - Memory 1-bit error correction bit (SM)

   Controls 1-bit memory error correction conditions for system recovery interrupts.

- Bit 6 - Degradation bit (DM)

   Only used with models 15 and 20. Controls degradation conditions.

- Bit 7 - Cache repressible machine check bit (XM)

   Only used with model 20. Controls cache repressible machine checks.

Subclass masks are not used with warning conditions or exigent conditions.

Table 4-2 summarizes the relationship of the subclass masks and the various types of machine checks.

Table 4-2. Machine Check Subclasses and Subclass Masks

| Machine Check Subclass | Subclass Mask |
|---|---|
| System damage (SD) | None |
| Instructions processing damage (PD) | None |
| System recovery (SR) | |
| ■  All except SC, OCE, MAE, and ICE | RM |
| ■  Cache repressible condition (OCE, MAE, and ICE) | XM |
| ■  Memory 1 bit error correction (SC) | SM |
| Program exception (PEX) | None |
| External damage (ED) | |
| ■  All except IOST | EM |
| ■  IOST abnormality (IOST) | None |
| Degradation (DG) | DM |
| Warning (WG) | None |

## 4.8. MACHINE CHECK INTERRUPT OPERATION

If a machine check interrupt is raised, and the interrupt is not suppressed, interrupt initialization is started. During this execution, the code showing details of the cause is stored as a machine check interrupt code (MCIC) in the logout area.

The interrupt control bits are the machine check hardware mask (MC) and program exception hardware mask (PX). These bits control machine check interrupt in the following manner:

- The MC mask is set to 1 after a machine check interrupt is accepted, and at the end of interrupt initialization. It is set to 0 when the corresponding interrupt processing routine load program status word (LPSW) instruction completes execution.

- The PX mask is set to 1 after a program exception interrupt is accepted, and at the end of interrupt initialization. It is set to 0 when the corresponding interrupt processing routine LPSW instruction completes execution.

- An exigent condition machine check interrupt occurs when the MC mask is 0. If the MC mask is 1, a check stop state occurs when control register 14 CS bit is set to 1. If the CS bit is 0, the corresponding machine check interrupt is deferred.

  The deferred interrupt is performed when the corresponding MC mask is cleared by an LPSW instruction. If the previously deferred interrupt is an exigent condition machine check, then delayed (D) machine check interrupt is requested.

- A repressible condition machine check interrupt occurs when both the MC mask and PX mask are 0. If the MC or PX mask is 1, the interrupt is deferred. It is possible to control the repressible condition machine check interrupt by the control register 14 subclass mask bit.

If a system damage machine check occurs during a repressible condition interrupt, both conditions are reported simultaneously. If a repressible condition machine check occurs during processing of a repressible condition machine check interrupt, both conditions are reported simultaneously.

If a deferred repressible condition exists and a different repressible condition machine check interrupt occurs:

- The deferred condition is reported at the same time.

- The deferment is released.

Also, if the control register subclass is set to 1, an interrupt occurs as long as the corresponding repressible condition is already deferred. The D bit is not raised for a repressible condition interrupt.

A machine check interrupt occurs even when the processing unit is in wait or execute state. If instructions are executing in step mode, machine check is performed the same as for a normal state. Tables 4-3 and 4-4 list the machine check interrupt operations used by the model 8 and models 10/15/20, respectively.

## Table 4-3. Model 8 Machine Check Interrupt Operations

| MCM | PXM | Control Register CS | Cause of Occurrence | Processing | Remarks |
|---|---|---|---|---|---|
| 0 | 0 | – | Exigent condition machine check | Exigent condition | During ordinary instruction processing |
|  | 1 |  |  |  | Machine check during program exception interrupt processing |
| 1 | – | CS = 1 | Exigent condition machine check | Check stop | – |
| 1 | – | CS = 0 | Exigent condition machine check | Deferment | Repressible condition machine check interrupt occurs when MCM becomes 0 (D bit = 1). |
| 0 | 0 | Corresponding Subclass mask = 0 Corresponding subclass mask = 1 | Repressible condition machine check | Deferment

Repressible condition machine check interrupt | – |
| 0 | 1 | – | Repressible condition machine check | Deferment | Repressible condition machine check interrupt occurs when the deferment condition is released. |
| 0 | 1 | – | Program exception | Exigent condition machine check interrupt. | – |

## Table 4-4. Models 10/15/20 Machine Check Interrupt Operations

| Cause of Occcurrence | MCM | PXM | Control Register CS | System Control | Multiple MCK | |
|---|---|---|---|---|---|---|
| | | | | | Exigent | Repressible |
| Exigent condition machine check | 0 | – | – | Exigent condition machine check interrupt | Check stop | See Note 1 |
| | 1 | – | 0 | Deferment (See note 3) | – | – |
| | 1 | – | 1 | Check stop | – | – |
| Repressible condition machine check | 0 | 0 | Corresponding subclass mask = 0 | Deferment | – | – |
| | | | Corresponding subclass mask = 1 | Repressible condition machine check interrupt | System damage MCK | See Note 2 |
| | | 1 | – | Deferment | – | – |
| | 1 | – | – | Deferment | – | – |
| Program exception | 0 | 1 | – | Exigent condition machine check interrupt. | – | – |
| | 1 | – | – | Abnormal stop | – | – |

NOTES:

1.    The system recovery (SR) condition may be reported in the same MCIC. A warning (WG) or external damage (ED) condition may be held pending.

2.    All repressible conditions are reported in the same MCIC.

3.    System integrity may be lost.

## 4.9. LOGOUT

Information logout is performed in a logout area assigned at the time of a machine check by control register 15. The first logout of repeated machine checks is stored through an instruction retry.

If the MC mask is 1, or control register 14 subclass is 0, an interrupt does not occur and logout is not performed. If a subclass machine check occurs during interrupt deferment, both causes are reported to the interrupt code. The logout, however, refers to the subsequent machine check. If the interrupt deferment is released, an interrupt occurs and logout is performed.

Machine check logout for the system is performed in the system logout area indicated by control register 15, and is stored in the formats illustrated in Figure 4-6 (model 8) and Figure 4-7 (models 10/15/20).

The machine check interrupt code validity and the validity of logout contents other than this code, are respectively indicated by the machine check interrupt code. The initial value of the contents of the control register is X'C00'.

CONTROL
REGISTER 15 | SYSTEM LOGOUT AREA ADDRESSES (ABSOLUTE ADDRESSES) |

(HEXADECIMAL
BYTE DISPLAY)

| Address Range | Description |
|---|---|
| 000 ～ 007 | MACHINE CHECK INTERRUPT CODE (8 BYTES) |
| 008 ～ 00F | PSW LOGOUT AREA (8 BYTES) |
| 010 ～ 017 | UNUSED |
| | UNUSED |
| 018 ～ 01F | TOD CLOCK LOGOUT AREA (8 BYTES) |
| 020 ～ 05F | GENERAL REGISTER LOGOUT AREA FOR SUPERVISOR (64 BYTES) |
| 060 ～ 09F | GENERAL REGISTER LOGOUT AREA FOR USER (64 BYTES) |
| 0A0 ～ 0BF | FLOATING-POINT REGISTER LOGOUT AREA (32 BYTES) |
| 0C0 ～ 0FF | CONTROL REGISTER LOGOUT AREA (64 BYTES) |
| 100 ～ 13F | SNAP REGISTER LOGOUT AREA (64 BYTES) |
| 140 ～ 16F | MMU LOGOUT AREA (48 BYTES) |
| 170 ～ 17F | EXTERNAL DAMAGE INFORMATION LOGOUT AREA (16 BYTES) |
| 180 ～ 1BF | (48 BYTES = 0) (UNUSED) |
| 18F ～ 3FF | EXPANDED BPU LOGOUT AREA (576 BYTES) |

NOTES:

1. Control register 15 (indicates logout area leading byte address). Logout area: 1024 bytes (256 words) (Initial value: X'C00')

2. The same logout is performed by STOP E status instruction, and also by manual frame status operation.

**Figure 4-6. Model 8 System Logout Format (part 1 of 3)**

Figure 4-6. Model 8 System Logout Format (part 2 of 3)

Logout address format (bits 0 7 8 ... 28 31): LOGOUT ADDRESS

**(000)** (0 — 31)

| Addr | Content | | |
|---|---|---|---|
| 000 | MCICU | | |
| 004 | MCICL | | |
| 008 | PSWU | | |
| 00C | PSWL | | |
| 010 | 0 | | |
| 014 | 0 | | |
| 018 | TODU | | |
| 01C | TODL | | |
| 020 | SUPER GR | C | (SM-X'80') |
| 024 | | 1 | 81 |
| 028 | | 2 | 82 |
| 02C | | 3 | 83 |
| 030 | | 4 | 84 |
| 034 | | 5 | 85 |
| 038 | | 6 | 86 |
| 03C | | 7 | 87 |
| 040 | | 8 | 88 |
| 044 | | 9 | 89 |
| 048 | | 10 | 8A |
| 04C | | 11 | 8B |
| 050 | | 12 | 8C |
| 054 | | 13 | 8D |
| 058 | | 14 | 8E |
| 05C | | 15 | 8F |
| 060 | PROBLEM GR | 0 | (SM-X'A0') |
| 064 | | 1 | A1 |
| 068 | | 2 | A2 |
| 06C | | 3 | A3 |
| 070 | | 4 | A4 |
| 074 | | 5 | A5 |
| 078 | | 6 | A6 |
| 07C | | 7 | A7 |

**(080)**

| Addr | Content | | |
|---|---|---|---|
| 080 | PROBLEM GR | 8 | A8 |
| 084 | | 9 | A9 |
| 088 | | 10 | AA |
| 08C | | 11 | AB |
| 090 | | 12 | AC |
| 094 | | 13 | AD |
| 098 | | 14 | AE |
| 09C | | 15 | AF |
| 0A0 | FR | 0 | (SM-X'C0') |
| 0A4 | | 1 | C1 |
| 0A8 | | 2 | C2 |
| 0AC | | 3 | C3 |
| 0B0 | | 4 | C4 |
| 0B4 | | 5 | C5 |
| 0B8 | | 6 | C6 |
| 0BC | | 7 | C7 |
| 0C0 | CR | 0 | (SM-X'90') |
| 0C4 | (CONTROL) | 1 | 91 |
| 0C8 | | 2 | 92 |
| 0CC | | 3 | 93 |
| 0D0 | | 4 | 94 |
| 0D4 | | 5 | 95 |
| 0D8 | | 6 | 96 |
| 0DC | | 7 | 97 |
| 0E0 | | 8 | 98 |
| 0E4 | | 9 | 99 |
| 0E8 | | 10 | 9A |
| 0EC | | 11 | 9B |
| 0F0 | | 12 | 9C |
| 0F4 | | 13 | 9D |
| 0F8 | | 14 | 9E |
| 0FC | | 15 | 9F |

**(100)**

| Addr | Content | | |
|---|---|---|---|
| 100 | SR | 0 | (SM-X'B0') |
| 104 | (SNAP) | 1 | B1 |
| 108 | | 2 | B2 |
| 10C | | 3 | B3 |
| 110 | | 4 | B4 |
| 114 | | 5 | B5 |
| 118 | | 6 | B6 |
| 11C | | 7 | B7 |
| 120 | | 8 | B8 |
| 124 | | 9 | B9 |
| 128 | | 10 | BA |
| 12C | | 11 | BB |
| 130 | | 12 | BC |
| 134 | | 13 | BD |
| 138 | | 14 | BE |
| 13C | | 15 | BF |
| 140 | MMULOG | OU | (SM-X'20') |
| 144 | | 0L | 21 |
| 148 | | 1U | 22 |
| 14C | | 1L | 23 |
| 150 | | 2U | 24 |
| 154 | | 2L | 25 |
| 158 | | 3U | 26 |
| 15C | | 3L | 27 |
| 160 | | 4U | 28 |
| 164 | | 4L | 29 |
| 168 | | 5U | 2A |
| 16C | | 5L | 2B |
| 170 | ED MCICU | | 2C |
| 174 | ED MCICL | | 2D |
| 178 | ED ERO | | 2E |
| 17C | ED ER1 | | 2F |

**(110)**

| Addr | Col1 | Col2 | Col3 | Col4 | Col5 | Col6 |
|---|---|---|---|---|---|---|
| 180 | | | | | | |
| 184 | | | | | | |
| 188 | | | | | | |
| 18C | | | | | | |
| 190 | | | | | | |
| 194 | | | | | | |
| 198 | | | | | | |
| 19C | | | | | | |
| 1A0 | | | | | | |
| 1A4 | | | | | | |
| 1A8 | | | | | | |
| 1AC | | | | | | |
| 1B0 | | | | | | |
| 1B4 | | | | | | |
| 1B8 | | | | | | |
| 1BC | | | | | | |
| 1C0 | BPU-MCIC — (SM-X'40') | | | | | |
| 1C4 | CPU ID | | | MCIC | | B0/B1 |
| 1C8 | | | | MCIC | | B2/B3 |
| 1CC | | | | | ER0 B0 | ER1 B0 |
| 1D0 | | | | | B1 | B1 |
| 1D4 | | | | | B2 | B2 |
| 1D8 | | | | | B3 | B3 |
| 1DC | | | | | CN | ER2 B0 |
| 1E0 | ZR | | | | | |
| 1E4 | CA 0–13 | P | | 0 | | ER2 B0 |
| 1E8 | CAB | P | | 0 | | ER2 B0 |
| 1EC | CAC | P | | 0 0 | | ER2 B0 |
| 1F0 | RA | P | | 0 0 | | ER2 B0 |
| 1F4 | AS | P | | 0 0 | | ER2 B0 |
| 1F8 | 0 SP D | DC | | 0 0 | | ER2 B0 |
| 1FC | FF DC | | | 0 0 | | ER2 B0 |

Figure 4-6. Model 8 System Logout Format (part 3 of 3)

| (200) | | (280) | | (300) | | (380) | |
|---|---|---|---|---|---|---|---|
| 200 | IA  (SM-X'50') | 280 | SM-X '00' | 300 | SM-X '30' | 380 | SM-X 'E0' |
| 204 | AR | 284 | 01 | 304 | 31 | 384 | E1 |
| 208 | BR | 288 | 02 | 308 | 32 | 388 | E2 |
| 20C | CR | 28C | 03 | 30C | 33 | 38C | E3 |
| 210 | JR | 290 | 04 | 310 | 34 | 390 | E4 |
| 214 | HR | 294 | 05 | 314 | 35 | 394 | E5 |
| 218 | MU | 298 | 06 | 318 | 36 | 398 | E6 |
| 21C | ML | 29C | 07 | 31C | 37 | 39C | E7 |
| 220 | IR | 2A0 | 08 | 320 | 38 | 3A0 | E8 |
| 224 | IBU | 2A4 | 09 | 324 | 39 | 3A4 | E9 |
| 228 | IBL | 2A8 | 0A | 328 | 3A | 3A8 | EA |
| 22C | TU | 2AC | 0B | 32C | 3B | 3AC | EB |
| 230 | TL | 2B0 | 0C | 330 | 3C | 3B0 | EC |
| 234 | FG | 2B4 | 0D | 334 | 3D | 3B4 | ED |
| 238 | SU 00 \| SU B1 \| 00 \| 0 \| 0 | 2B8 | 0E | 338 | 3E | 3B8 | EE |
| 23C | SL B \| 00 \| SL B2 \| 0 \| 0 | 2BC | 0F | 33C | 3F | 3BC | EF |
| 240 | EP \| JR B1 \| JR B2 \| JR B3 | 2C0 | 10 | 340 | STK  +0  (SM-X'D0') | 3C0 | SM-X 'F0' |
| 244 | CUCL \| JR B1 \| JR B2 \| JR B3 | 2C4 | 11 | 344 | +1  D1 | 3C4 | F1 |
| 248 | JR B0 \| JR B1 \| JR B2 \| 0 \| B U | 2C8 | 12 | 348 | +2  D2 | 3C8 | F2 |
| 24C | JR B0 \| JR B1 \| JR B2 \| 0 \| B L | 2CC | 13 | 34C | +3  D3 | 3CC | F3 |
| 250 | 0 \| 0 \| RTE \| 0 | 2D0 | 14 | 350 | +4  D4 | 3D0 | F4 |
| 254 | 0 \| 0 \| CN B2 \| 0 \| 0 | 2D4 | 15 | 354 | +5  D5 | 3D4 | F5 |
| 258 | — | 2D8 | 16 | 358 | +6  D6 | 3D8 | F6 |
| 25C | — | 2DC | 17 | 35C | +7  D7 | 3DC | F7 |
| 260 | TU B0 \| MA | 2E0 | 18 | 360 | +8  D8 | 3E0 | F8 |
| 264 | TU B0 \| RLR \| MK | 2E4 | 19 | 364 | +9  D9 | 3E4 | F9 |
| 268 | MA | 2E8 | 1A | 368 | +10  DA | 3E8 | FA |
| 26C | RLR \| MK | 2EC | 1B | 36C | +11  DB | 3EC | FB |
| 270 | MA | 2F0 | 1C | 370 | +12  DC | 3F0 | FC |
| 274 | OF \| RLR \| MK | 2F4 | 1D | 374 | +13  DD | 3F4 | FD |
| 278 | IRB | 2F8 | 1E | 378 | +14  DE | 3F8 | FE |
| 27C | PF \| PD | 2FC | 1F | 37C | +15  DF | 3FC | FF |

CONTROL REGISTER 15 | SYSTEM LOGOUT AREA ADDRESSES (ABSOLUTE ADDRESSES)

(HEXADECIMAL BYTE DISPLAY)

| | | |
|---|---|---|
| 000 ~ 007 | MACHINE CHECK INTERRUPT CODE (8 BYTES) |
| 008 ~ 00F | PSW LOGOUT AREA (8 BYTES) |
| 010 ~ 017 | RESERVED (8 BYTES) |
| 018 ~ 01F | TOD CLOCK LOGOUT AREA (8 BYTES) |
| 020 ~ 05F | GENERAL REGISTER LOGOUT AREA FOR SUPERVISOR (64 BYTES) |
| 060 ~ 09F | GENERAL REGISTER LOGOUT AREA FOR USER (64 BYTES) |
| 0A0 ~ 0BF | FLOATING-POINT REGISTER LOGOUT AREA (32 BYTES) |
| 0C0 ~ 0FF | CONTROL REGISTER LOGOUT AREA (64 BYTES) |
| 100 ~ 13F | SNAP REGISTER LOGOUT AREA (64 BYTES) |
| 140 ~ 14F | MMU LOGOUT AREA (16 BYTES) |
| 150 ~ 16F | RESERVED (32 BYTES) |
| 170 ~ 17F | EXTERNAL DAMAGE INFORMATION LOGOUT AREA (16 BYTES) |
| 180 ~ 18F | INSTRUCTION CACHE MEMORY LOGOUT AREA (16 BYTES) OR MICRO ACCELERATOR LOGOUT AREA (16 BYTES) - MODEL 15 ONLY |
| 190 ~ 19F | OPERAND CACHE MEMORY LOGOUT AREA (16 BYTES) |
| 1A0 ~ 1AF | FLOATING-POINT PROCESSOR LOGOUT AREA (16 BYTES) |
| 1B0 ~ 1BF | RESERVED (16 BYTES) |
| 1C0 ~ 3FF | EXPANDED BPU LOGOUT AREA (576 BYTES) |

**Figure 4-7. Models 10/15/20 System Logout Format**

## 4.10. MACHINE CHECK INTERRUPT CODE

The machine check interrupt code (MCIC) is stored in the two leading words of the system logout area. The cause of machine check interrupt is indicated in bits 0 to 5. One of these bits is always set to 1 when the interrupt occurs. If machine check occurs simultaneously for multiple causes, more than one bit can be occasionally set to 1.

The MCIC also indicates:

- Additional details on causes of machine check

- Location of the error

- Time of occurrence

- Logout validity

Figure 4-8 shows the format of the MCIC.

| SUBCLASS | | | | | | | | | TIM-ING | | ERROR RELATED TO MEMORY | | | | ERROR RELATED TO CPU | | | | | | AREA CODE | | | | | | | VALIDITY | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S D | P D | S R | P E X | E D | D G | W | B | D | S E | S C | D E | K E | 0 | I C E or M A E | O C E | P T E | C E / F P E | I P R | I O T | 0 | C W E | I O S T | 0 | T E D | I E D | IEDS | T C V | L O V | 0 | I L V |
| 0 | | | | 4 | | | | 8 | | | | 12 | | | | 16 | | | | 20 | | | | 24 | | 26 | | 28 | | | 31 |

| CHA | | 0 | 0 | 0 | 0 | FMA |
|---|---|---|---|---|---|---|
| CH | IOP | | | | | |
| 32 | 33 | 34 | 35 | 36 | 39 | 40 ... 63 |
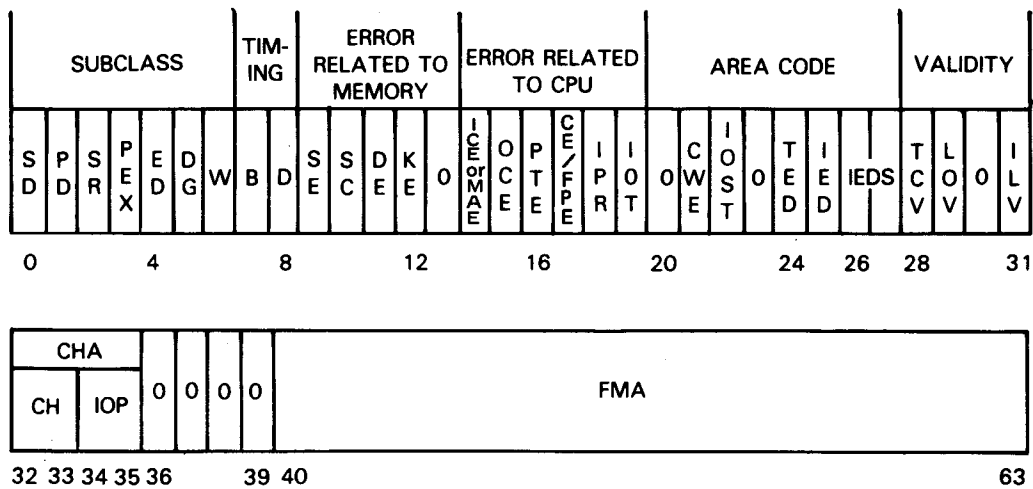
Figure 4-8. Machine Check Interrupt Code Format

The bits in this format are defined in the following paragraphs.

### 4.10.1. Subclasses

The subclasses of machine check interrupts are:

- System damage (SD)

  Occurs when an error is found and:

  - The processing unit is in an IOST, interrupt, processing, or waiting state.

  - There is an indication that continuation of subsequent program execution is not guaranteed.

- Instruction processing damage (PD)

  Indicates that an error occurs during instruction execution. The backup bit (bit B) indicates whether retry by program is possible. That is, if bit B is 1, information concerning general registers and contents of the old PSW (in which machine check interrupt was stored) is accurately preserved. PD also occurs at a timeout of the stall timer during instruction execution (except in IOT).

- System recovery (SR)

  Indicates whether an instruction retry is successful, or if there is a 1-bit storage error

- Program exception (PEX)

  Indicates that a program exception item occurs during processing of a program exception interrupt (PX mask bit = 1)

- External damage (ED)

  Indicates that an abnormal state occurs during I/O operations, IOST processing, or in SCP

- Warning (W)

  Indicates an environmental abnormality

- Degradation (DG)

  Used only on models 15 and 20. It indicates that the micro accelerator (model 15), or, for model 20, the instruction cache, operand cache, or floating point processor is disabled and system performance is degraded.

### 4.10.2. Timing of Machine Check Interrupt

These interrupts are:

- Backup (B)

    When set to 1, a retry is possible. It indicates that the information used for program retry was stored after the unsuccessful retry instruction processing damage.

- Delayed (D)

    If the exigent condition check interrupt is deferred when the MC mask is set from 1 to 0 by an LPSW instruction, then an interrupt occurs after execution of the LPSW instruction. The D bit is 1 if this occurs.

### 4.10.3. Errors Related to Storage

These errors are:

- Storage 2-bit error (SE)

    Indicates the exigent condition machine check or external damage machine check is due to a main storage 2-bit error

- Storage 1-bit error (SC)

    Indicates a 1-bit error occurs in main storage during system recovery

- Storage control error (DE)

    Indicates the exigent condition machine check or external damage machine check is due to the main storage control circuit

- Key storage error (KE)

    Indicates the exigent condition machine check or external damage machine check is due to a key storage error

### 4.10.4. Errors Related to Processing Unit

The errors related to the processing unit are:

- Micro accelerator error (MAE)

    Used only with model 15. Indicates an error was detected in the micro accelerator memory. If reported with DG = 1, the micro accelerator is disabled.

- Instruction cache error (ICE)

    Used only with model 20. Indicates an error was detected in the instruction cache memory. If reported with DG = 1, the instruction cache is disabled.

- Operand cache error (OCE)

  Used only with model 20. Indicates an error was detected in the operand cache memory. If reported with DG = 1, the operand cache is disabled.

- Patrol error (PTE)

  Indicates the exigent condition machine check is an error during wait patrol.

- High-speed buffer storage error (CE)

  Used only with model 8. Indicates the exigent condition or system recovery is an error in high speed buffer storage.

- Floating point processor error (FPE)

  Used only with model 20. Indicates an error was detected in the floating point processor. If reported with DG = 1, the floating point processor is disabled.

- Interface parity error (IPR)

  Indicates the processing unit detected an error on the interface during execution of an I/O instruction, control instruction, or IOST processing

- Time-out on interface stall timer (IOT)

  Indicates the stall timer went to time-out (4 ms) during execution of the I/O instruction, store UCW instruction, or IOST processing

### 4.10.5. Area Codes

The area codes in machine check interrupt mode are:

- IOSTCW abnormality (CWE)

  Indicates an addressing exception or storage protection exception occurs during access of IOSTCW

- IOST abnormality (IOST)

  Indicates an exigent condition or repressible condition machine check occurs during IOST processing

- TOD abnormality (TED)

  Indicates an abnormality exists in the TOD clock due to external damage (ED)

- Input/output external damage (IED)

  Indicates an error occurs during I/O operation due to external damage (ED). The error location is indicated on IEDS.

- I/O External damage subarea code (IEDS)

  Indicates the location of the error causing the IED is indicated by code

## 4.10.6. Validity Bits

The validity bits of the machine check interrupt code indicate that logout was performed correctly.

- TCV

  When set to 1, indicates that the logout of the MCIC was made normally

- LOV

  When set to 1, indicates that logout of the system/expansion processing unit following the MCIC is correct

- ILV

  Indicates external damage validity together with an external damage condition

## 4.10.7. CH, IOP Address

The address of the CH and IOP under operation is indicated in event of input/output external damage.

## 4.10.8. Failing Memory Address

The failing memory address (FMA) indicates the corresponding actual address in main storage when a storage related error occurs. When an interface stall timer timeout (IOT) is detected by BP, 16 bits including the I/O interface function code are entered in place of FMA.

## 4.11. MACHINE CHECK AND CONTROL REGISTER

Control register 15 is used to assign the actual address of the system input area.

Figure 4-9 shows the format of the control register 15.

CONTROL REGISTER 15

| X | SYSTEM LOGOUT AREA ADDRESS (INITIAL·VALUE X'C00') | X |
|---|---|---|

0              7 8                                           28 29   31
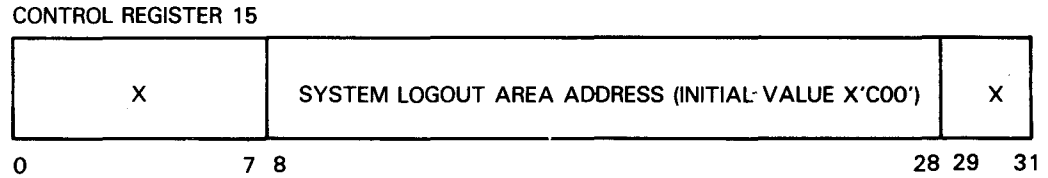
NOTE:

Bytes 0–7 and bits 29–31 are neglected.

**Figure 4-9. Control Register 15 Format**

In addition, there are control mask bits that determine:

■ Whether any machine check interrupt occurred

■ Whether any logout is to be made in control register 14

Figure 4-10 shows the format of control register 14.

CONTROL REGISTER 14

| C S | 0 | R M | E M | 0 | S M | D M | X M | |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 31 |
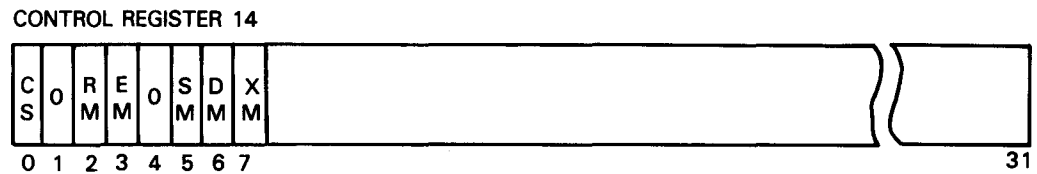
**Figure 4-10. Control Register 14 Format**

The definitions of the significant control register bits are:

- Check stop control bit (CS)

  This bit is used to determine if a check stop should be made after an exigent condition machine check, where either of the following conditions exists:

  - The processing unit is suppressing the machine check interrupt (MC mask).

  - Exigent condition machine check interrupt ILS is being processed, or machine check interrupt code and logout information are being stored.

  If the CS bit is 1, a check stop occurs when either of the above conditions occurs. If the CS bit is 0, processing is continued independently from the machine check. If the exigent condition is repeated 31 times during processing, however, a check stop is made without using the CS bit.

- Machine check subclass mask

  The mask bits are:

  - System recovery mask (RM)

  - External damage mask (EM)

  - Degradation mask (DM)

  - Cache repressible machine check mask (XM)

  Interrupts are controlled by these mask bits as well as with the MC mask. If an interrupt is deferred with a subclass mask of 0, no reporting is made, even if a machine check interrupt for another repressible condition occurs. The interrupt makes the report at the time the corresponding mask is released.

- Storage 1 bit error mask (SM)

  The SM bit controls a 1-bit error machine check interrupt. If SM is 1, a storage 1-bit error causes a system recovery interrupt. If the SM bit is 0, no interrupt or deferment occurs.

Table 4-5 lists and defines the machine check and control mask bits.

#### Table 4-5. Machine Check and Control Mask Bits

| Bit | Function | Control Register | Bit Position | Initial Value |
|-----|----------|------------------|--------------|---------------|
| CS | Check stop control | 14 | 0 | 1 |
| RM | System recovery mask | 14 | 2 | 0 |
| EM | External damage mask | 14 | 3 | 0 |
| SM | Storage 1-bit error mask | 14 | 5 | 0 |
| DM | Degradation mask (models 15 and 20 only) | 14 | 6 | 0 |
| XM | Cache repressible machine check mask (model 20 only) | 14 | 7 | 0 |

# 5. Operations Systems Control

## 5.1. SYSTEM CONSOLE CONTROL

The system consoles for the model 8 and models 10/15/20 (Figures 5-1 and 5-2) are used for operation control and maintenance functions for the processing system. Operating procedures are provided in the *System 80 Models 8/10/15/20 Processor and Central Peripherals Operating Guide*, UP-9608.

The following basic components comprise the system console:

- System control processor (SCP)

- System control panel

  Used to turn system power on and off and to display system status

- Console display and keyboard

  Provides the operator with a display screen for system operations

- Console diskette drive

  Used for:

  - Initial microprogram load (IMPL) for the processing unit, D MUX, SCP, and SEL (models 10/15/20 only)

  - Initial program load (IPL) for storage of diagnostic microprograms or as a logout area for exigent conditions that occur within the processing system
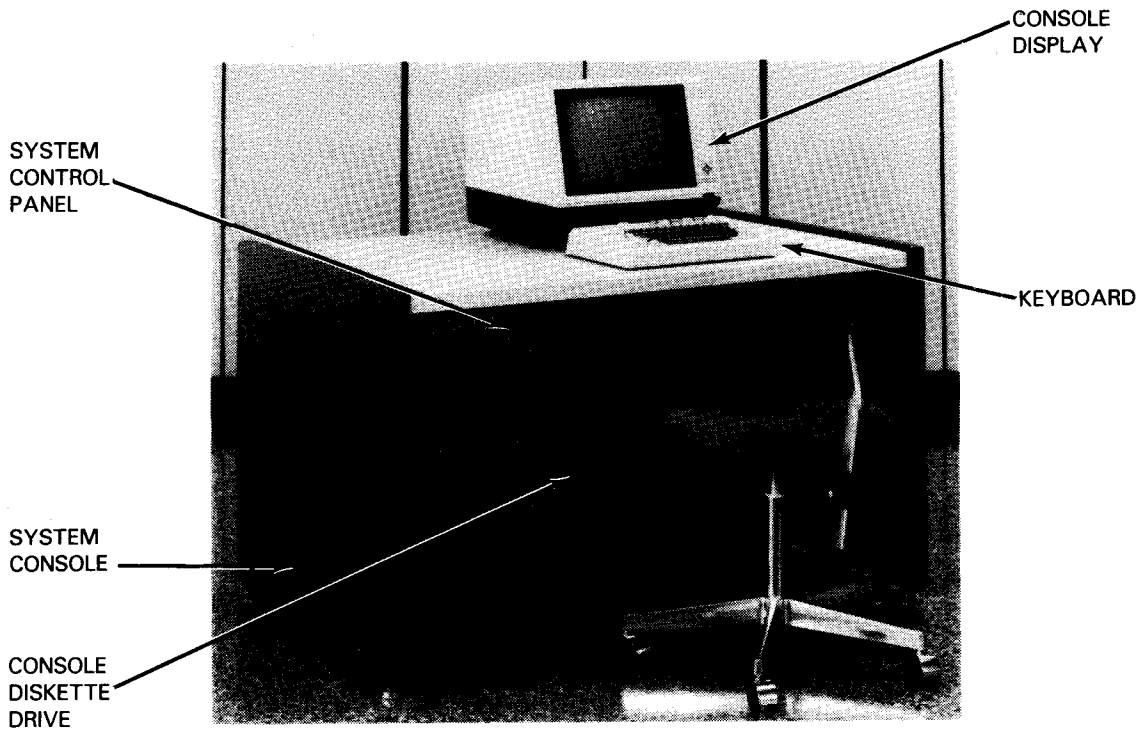
**Figure 5-1.** Model 8 System Console
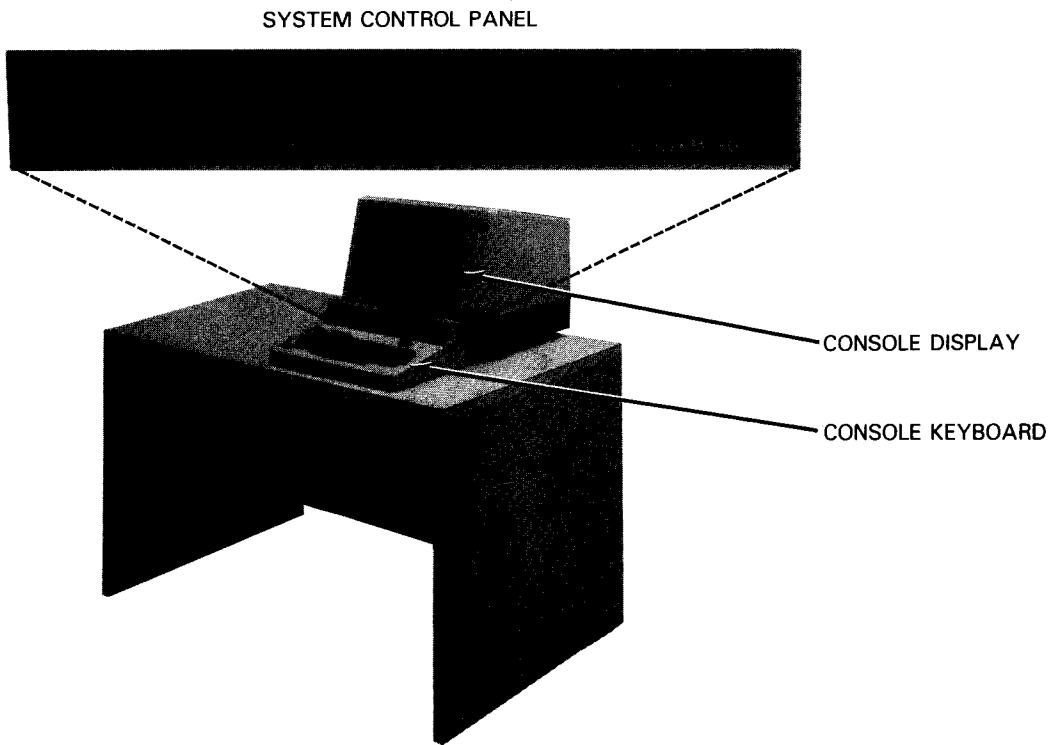


**Figure 5-2.** Models 10/15/20 System Console

## 5.2. CONSOLE DISPLAY FUNCTIONS

The console display and keyboard are different from workstations used throughout the system since their capability extends to system operation and maintenance control.

The functions are:

- Operator console        Under control of the software

- System control        Starts and stops the processing system, changes the configuration, initiates IPL and IMPL, etc.

- System supervision        Collects error information requested from the MSU, processing unit, CHC, IOP, and SCP.

- Maintenance console        Maintenance and diagnostic functions for each component of the processing system.

- System automatic recovery        Performs automatic recovery from IPL after a check stop state in the system.

- Remote maintenance        Allows remote maintenance from the maintenance center.

# 6. Input/Output Status Tabler

## 6.1. INPUT/OUTPUT STATUS TABLER (IOST) OPERATIONS

The IOST instructs and monitors status transfers between the main storage unit and I/O channels. The IOST has a basic processing unit priority for the use of the main storage unit. The IOST receives status on the channel, subchannel, and I/O devices, and stores this information in the status tabler area of the main storage unit.

The IOST has characteristics similar to the I/O channel and is controlled by the SIO instruction. Since the IOST uses low addresses in main storage, it requires a storage protection key of zero. In this manner, the IOST informs the processing unit of operation completions and abnormalities that occur during operation of the:

■   Channel

■   Subsystem

■   Control unit

■   Devices connected to the I/O channel

Interrupt requests from respective I/O devices are simplified and become more effective by leaving status tabling to the IOST. This reduces the load of the supervisor for interrupt processing.

## 6.2. STATUS HANDLING

The IOST receives status from all channels, subchannels, and subsystems, and stores the status in the tabling area of main storage. Status tabling is performed as if the I/O channel were handling data.

Status tabling is controlled by the I/O status tabler control word (IOSTCW) received from software.

The IOSTCW:

- Fetches status from the buffered channel status word (BCSW), which is also in the fixed area of main storage

- Stores the status in the tabling area to make it an IOST interrupt request

### 6.2.1. Buffered Channel Status Word

The buffered channel status word (BCSW) is located at addresses 0B0 to 0BF (hex) in the MSU, which is an area for temporary storage of channel status.

### 6.2.2. I/O Status Tabler Control Word

The I/O status tabler control word (IOSTCW), which consists of full words, is located at addresses 010 to 01B (hex) in the fixed area of main storage. The IOSTCW controls operation of the IOST by indicating the position in the status table where the next I/O status tabler interrupt word (IOSTIW) is to be stored. The IOSTCW also links the two separate areas of main storage for the status table, or obtains software approval for a wraparound.

Before starting up the system, software sets the parameters required for the IOSTCW. The IOST can replace the filed IOSTCW to increase the effective use of the tabling area.

Figure 6-1 illustrates the IOSTCW format.

| 0 | ACTIVE COUNT | 0 | REPLACEMENT COUNT |
|---|---|---|---|

0　1　2　　　　　　　　　　　　　　　　　15　16　17　18　　　　　　　　　　　　　　　　31

| ←KEY→ | 0 0 | ADDRESS | |
|---|---|---|---|
| | | FIXED | ACTIVE |

32　　　37 38 39 40　　　　　　48　　　　　　　　　　　　　　　63

| REPLACEMENT ADDRESS | IOSTSW | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | CHANNEL ADDRESS | | | | | | | | |
| | 0 | I O S T | 0 | CH. NO. | ←0→ | I W E | I D E | C T O | C B W | S T F |

64　　　　　　　　　　　　79 80　81 82 83 84　　　　87 88　　　90 91 92 93 94 95
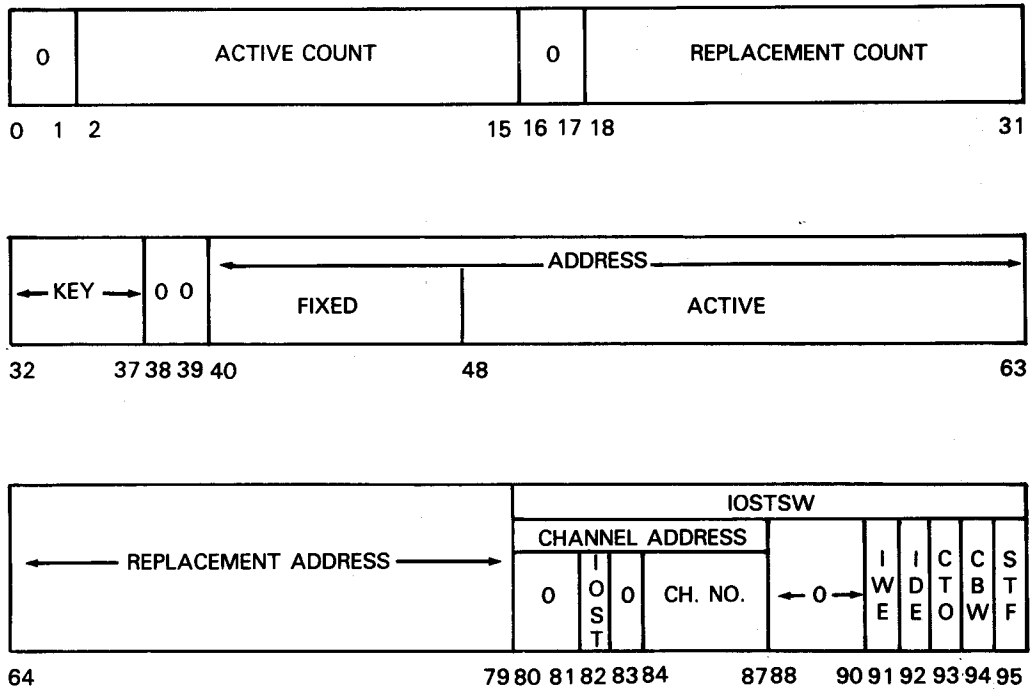
Figure 6-1.  IOSTCW Format

The definitions of bits in the IOSTCW format are:

- **Bits 2 to 15 - Active count**

  This shows the number of words remaining in the status tabler. Each time a status word is stored in the status table by the IOST, 1 is deducted from this count. The maximum count is 16,383 words. In this case, 0 is set to the active count field.

- **Bits 18 to 31 - Replacement count**

  This is the value replacing the active count field when the active count is reduced to 0.

- **Bits 32 to 37 - Key**

  This is a storage protection key used by IOST to access the status table. The IOST address is always an absolute address.

- **Bits 40 to 63 - Address**

  Contains the absolute address of the word (4 bytes) indicating the position of the status table in main storage where the next IOSTIW is to be stored. Contents of this field point to the first byte of the status table. The address must be on the full word boundary; otherwise, the IWE bit is set and causes an IOST interrupt. Following the interrupt, IOST assumes a temporarily suspended status.

■ Bits 40 to 47 - Fixed address

The address indicating the position of the status table is shown by bits 40 to 63. To improve control efficiency of status tabling, the address shown by these 24 bits is divided into a fixed field and active field. The value of this fixed field does not change even if the address of the active field exceeds the maximum value. At this time, the value of the active address field (bits 48 to 63) remains unchanged.

■ Bits 48 to 63 - Active address

Each time IOSTIW is stored in the status table, a count of 4 is added to this address. The active address is then replaced when the active count is reduced to 0.

■ Bits 64 to 79 - Replacement address

This address is stored in the active part (bits 48 to 63) of the address field when the active count is reduced to 0.

■ Bits 80 to 95 - I/O status tabler service word (IOSTSW)

These bits store the error state if the error occurs while the IOST is storing status in the status table.

■ Bits 80 to 87 - Channel address

This is the channel address selected during occurrence of an error.

■ Bit 91 - Interrupt word error (IWE)

Indicates one of the following:

- An error in storage protects the exception items

- An error in address exception items was detected by IOST when IOSTIW was written into, or read from, the status table or BCSW (readout only)

■ Bit 92 - Interrupt data error (IDE)

Indicates an address check error or data parity check error was detected by IOST when the IOSTIW was written into, or read out from, the status table or BCSW (readout only).

■ Bit 93 - Channel time out (CTO)

Set when the channel selected fails to store status within a prescribed time.

- Bit 94 - Channel buffer word error (CBW)

  Indicates an address exception item, storage protect exception item, address check, or write bus check was selected by the selected channel when IOSTIW was written in the BCSW (address 0B0 to 0BF (hex) of main storage).

- Bit 95 - Status table full (STF)

  Set to 0 to indicate STF when the V bit of IOSTIW is detected as 0. IOST is where the IOSTIW is to be stored.

### 6.2.3. I/O Status Tabler Interrupt Word

The channel can store status in up to a maximum of four full words when the IOST permits it to send status to the status table.

The I/O channel writes the three to four full IOSTIW words in the buffered channel status word (BCSW) at address 0B0 to 0BF (hex) in main storage. The status is then stored in the channel or the subchannel is cleared.

**IOSTIW for CHC (Model 8) or SVP and SEL (Models 10/15/20)** _____

Figure 6-2 shows the IOSTIW format for the CHC, SVP, or SEL.

| V | C | S | O | CH. NO. | DEVICE ADDRESS | DEVICE STATUS | CHANNEL STATUS |
|---|---|---|---|---------|----------------|---------------|----------------|

0  1  2  3  4      7 8                15 16            23 24                        31

| V | C | ← 0 → | ← NEXT CCW ADDRESS → |
|---|---|-------|----------------------|

32 33 34      39 40                                                            63

| V | C | ← 0 → | ← REMAINING BYTE COUNT → |
|---|---|-------|--------------------------|

64 65 66              79 80                                                   95
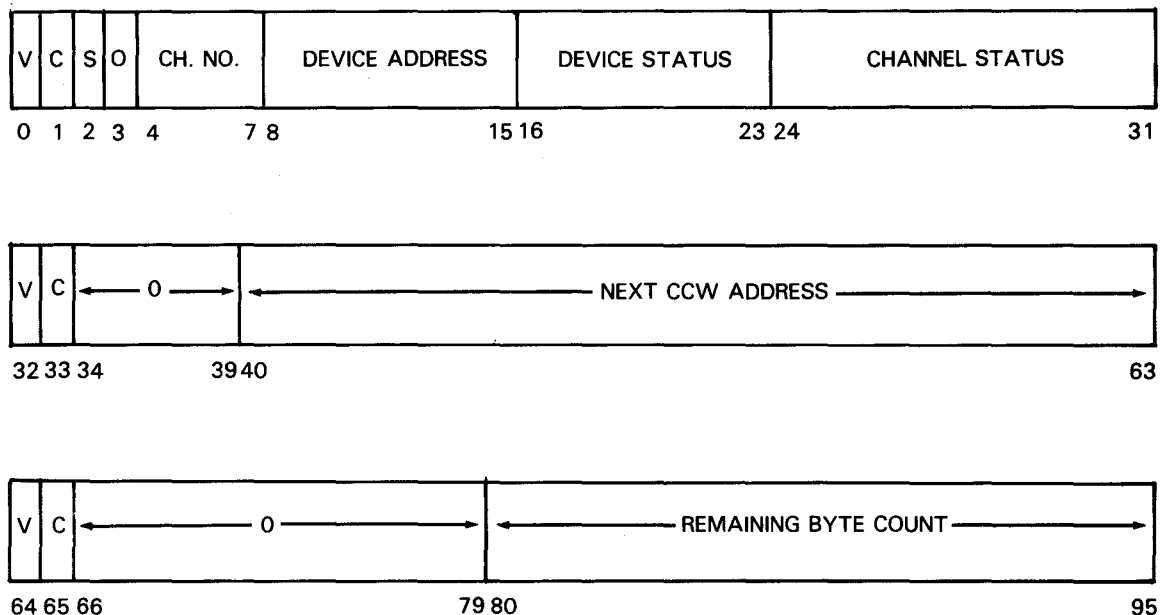
Figure 6-2. IOSTIW Format for CHC, SVP, and SEL

The definition of the bits in this format are:

■   Bits 0, 32, and 64 - Validation (V)

These bits are set to 0 to indicate to the status table that status information is new. These bits are set before storing the IOSTIW into the BCSW. After the status processing is completed, these bits are set to 1 by software so that processing completion can be validated.

■   Bits 1, 33, 65 - Continuation (C)

Indicates the length of the IOSTIW. When continuing to the next full word, these bits are set to 1 by the channel. They are set to 0 when the last full word is to be sent. Settings are:

-   Bits 1 and 33 are always 1.

-   Bit 65 is always 0.

■   Bit 2 - SIO trace bit (S)

When set to 1, the SIO trace is IOSTIW (only one word).

■   Bits 4 to 7 - Channel number (CH. NO.)

Indicates the channel sending status.

■   Bits 8 to 15 - Device address

Indicates the address of the device or subsystem sending status.

■   Bits 16 to 23 - Device status

Indicates the status of the device or subsystem.

■   Bits 24 to 31 - Channel status

Indicates the status set by the channel. This field is set to 0 only when device status is sent by the channel.

■   Bits 34 to 39 - Set to 0.

■   Bits 40 to 63 - Next CCW address

Indicates the address of the next CCW to be executed.

■   Bits 66 to 79 - Set to 0.

■   Bits 80 to 95 - Remaining byte count

Indicates the value of the byte count.

Figure 6-3 shows the IOSTIW format for the D MUX.

```
| V | C | S | 0 | CH. NO. | DEVICE ADDRESS |←──────────── 0 ────────────→|
 0   1   2   3 4         7 8              15 16                           31

| V | C |←─0─→| C | D | I |←──────────── ELEMENT ADDRESS ──────────────→|
                 H
 32 33 34    36 37 38 39 40                                            63

| V | C | 0 |←──────────────────────────────────────────────────→| 0
 64 65 66                                                           95
```
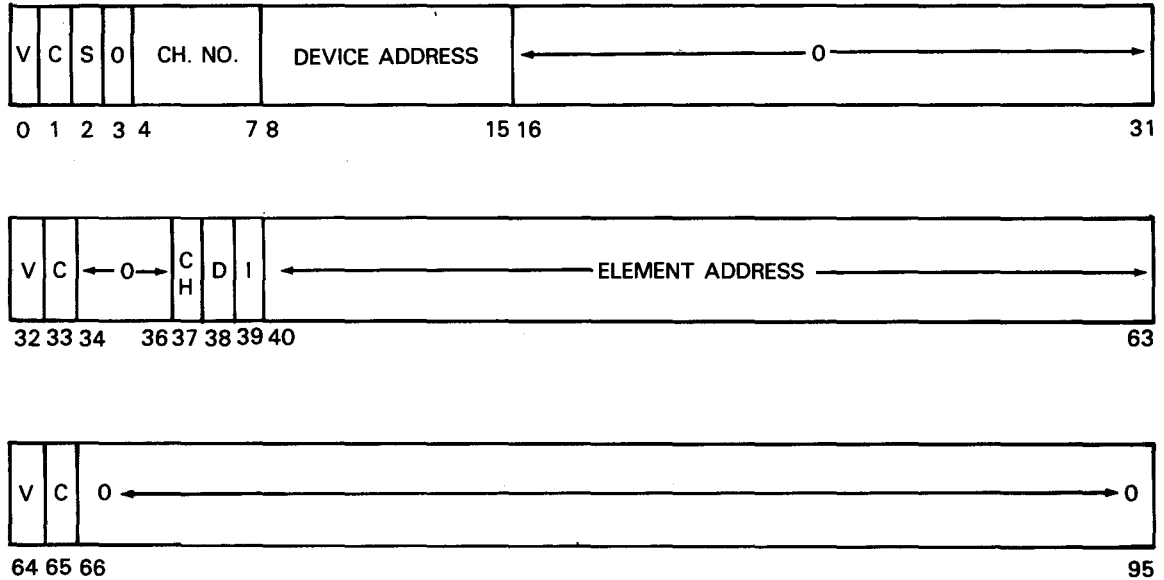
**Figure 6-3.  IOSTIW Format for D MUX**

The definitions of bits in this format are:

- Bits 0, 32, and 64 - Validation (V)

  These bits are set to 0 to indicate to the status table that status information is new. These bits are set before storing the IOSTIW into the BCSW. After the status processing is completed, these bits are set to 1 by software so that processing completion can be validated.

- Bits 1, 33, 65 - Continuation (C)

  - Bits 1 and 33 are always 1.

  - Bit 65 is always 0.

- Bit 2 - SIO trace bit (S)

  When set to 1, the SIO trace is IOSTIW (only one word).

- Bits 4 to 7 - Channel number (CH NO)

  Indicates the number of channels sending status.

- Bits 8 to 15 - Device address

  Indicates the address of the device or subsystem sending status.

- Bits 16 to 31 - Set to 0.

- Bits 34 to 36 - Set to 0.

- Bit 37 - Channel (CH)

  When set to 1, the element address references the CHCB.

- Bit 38 - DVCB (D)

  When set to 1, the element address references the DVCB.

- Bit 39 - IORB (I)

  When set to 1, the element address references the IORB.

- Bits 40 to 63 - Element address

  This is the absolute address of the system control element defined by the CH, D, or I bit.

- Bits 66 to 95 - Set to 0.

## 6.3. PROCESSING THE IOST

Operation of the IOST and I/O channel includes one of the following processes:

- The IOST sets the condition code (CC) at the end of the operation designated by an SIO and HIO instruction

- A procedure for machine check interrupt of the IOST

- Tabling process of the I/O channel IOSTIW

- Entering a suspended state when the IOST is about to store the corresponding information in the IOSTSW

### 6.3.1. Start I/O Instruction to IOST

An SIO instruction issued to the IOST cancels any suspended state. In the IOSTIW format used for the SIO instruction, bits 24 to 31 are set to 0, and no device address allocation is made.

The condition code set by the IOST in response to the SIO instruction, indicates if the IOST is in a suspended state:

CC = 00 (binary)    The IOST is in suspended state. The issued SIO instruction clears the suspended state and the IOST returns to normal operation.

CC = 11 (binary)    The IOST is not in suspended state. The issued SIO instruction is rejected and the IOST continues normal operation.

### 6.3.2. IOST Machine Check Interrupt

The IOST machine check level interrupt request is made by the IOST when certain hardware errors occur. In response to this interrupt request, the processing unit performs the machine check level interrupt initializing sequence.

The conditions that cause the interrupt, and the processing unit actions that result from these conditions, are:

1. An address or data parity error detected (during IOST processing) in main storage while, during IOST processing, read out was performed on the BCSW, or while read out or write of IOSTIW was performed on the status table field.

   As a result of this condition:

   - IOST machine check is initiated. At this time, external damage (ED) and IOST are reported to the machine check interrupt code (MCIC).

   - An IOST interrupt is then initiated and interrupt data error (IDE) is reported to IOSTSW.

2.   Exigent machine check occurs during IOST processing (except condition 1).

As a result of this condition:

■    IOST machine check is initiated. At this time, system damage (SD), ED, and IOST are reported to the MCIC.

■    There are conditions where the content of the IOSTCW of the status table being processed is not guaranteed. This depends upon the cause and timing of the machine check.

3.   An address exception or storage protection exception occurs during IOST processing when IOSTCW read out or write is performed.

As a result of this condition:

■    IOST machine check is initiated. At this time, ED, control word exception (CWE), and IOST are reported.

■    IOST interrupt is then initiated.

NOTES:   1.   Conditions 1 and 3 are repressible levels. Condition 2 is an exigent level.

2.   The IOST machine check interrupts in conditions 1, 2, and 3 are accepted for MCM = 0 only. External damage (ED) is raised (control register 15, bit 3: external damage mask), but interrupt request cannot be controlled by EM.

3.   In condition 2, the IOST interrupt request, which had been held, is now cleared.

When an IOST machine check level interrupt request is made, the IOST:

■    Assumes a suspended state

■    Inhibits status tabling requests from the channel

Processing of status tabling is resumed when the suspended state is canceled by an SIO instruction to IOST.

### 6.3.3.  Tabling for Normal I/O Status Tabler

Each channel sends status independently to the BCSW at address 0B0 to 0BF (hex) in main storage, and requests that status be stored in the BCSW. Device or channel status formed during I/O operation is processed by the channel making a status request. The channel starts the tabling processing procedure by making the status service request (SSR).

The IOST decides which channel status is stored in BCSW according to its own priority level.

Table 6-1 lists the priority level of status requests for the IOST that are assigned to each channel.

Table 6-1. IOST Status Request Priorities

| Priority Level | Channel | Channel Address |
|---|---|---|
| 1 | CHC | 00 (0) |
| 2 | CHC 1 (/BMX) | 01 (1) |
| 3 | (BMX) | 10 (2) |
| 4 | DMUX | 11 (3) |

When the channel completes status transfer to the BSCW, the channel issues a request for status tabler servicing to the IOST. The I/O channel then returns to the data transfer processing procedure.

After receiving a status servicing request for the channel, the IOST suspends the processing unit on the command boundary. It then fetches IOSTIW from BCSW and transfers it to the status table shown in the IOSTCW.

After tabling the IOSTIW, the IOST issues an IOST interrupt to the processing unit. Acceptance of the IOST interrupt request is decided by the system mask IOST bit of the present program status word.

While the IOST bit is 0, the interrupt is pending. Even while the interrupt is pending, however, the IOST continues tabling status by receiving status tabling requests from each channel while accepting the processing unit on the command boundary.

After the IOST interrupt request is accepted, the processing unit begins the I/O status level interrupt initializing sequence.

After status from the channel is correctly stored in the status table, the IOST again examines status requests from other channels. After a channel has stored status in the BCSW once, it can issue the next status request. The IOST continues to receive status requests and to select the specified channel according to the priority level.

### 6.3.4. IOST Timer

The IOST timer detects stops in the IOST operation that are caused by a hardware error in the IOST or channel. The channel selected by the IOST must complete storing status in the BCSW within 4 milliseconds.

If status storing is not completed within that time limitation, the IOST timer:

- Reverts to timeout

- Sends an interrupt selective reset (ISR) to the respective channel

When the ISR signal is sent to the I/O channel, the channel is disconnected from the IOST. The IOST then writes the information (channel number CTO bit) required for the IOSTCWs. IOSTSW and tabling operation suspends. The I/O channel in which this error occurs must not send the same status to the IOST again.

### 6.3.5. IOST Suspended State

The IOST enters a suspended state for tabling operations when:

- Certain IOST errors occur during status tabling,

- Certain errors occur before the channel completes storing status in the BCSW, or

- An IOST machine check occurs.

In a suspended state, the IOST:

- Inhibits status requests arising in succession from the selected channel and other channels

- Stores the cause of error in the IOSTSW

- Makes an IOST level interrupt request

The error detected by the channel is shown to the IOST as BCSW servicing error (BCSWSE). The IOST stores the channel number concerned in the IOSTSW and sets the CSW bit. The IOST holds the state until an SIO instruction is issued to cancel this suspended state.

In case of a time-out error, the IOST stores the channel number in the IOSTSW and sets the CTO bit. The error detected by the IOST during status tabling is shown by either of the IDE, IWE, STF bits of the IOSTSW. The channel number stored in the IOSTSW is the currently selected channel number. The IOST is in the suspended state and remains so until it is canceled by an SIO instruction.

When the suspended state is canceled, the IOST and channel return to normal status processing. Status tabling control by the IOSTCW parameters is performed for up to 16,383 full words with three full words as a maximum unit.

### 6.3.6. SIO Instruction Trace

SIO instruction trace is performed when:

- Bit 0 of the control register 12 (SIO trace bit) is 1

- Channel/device address is not ICP

The device address and condition code during execution of the SIO instruction are stored as a 1-word IOSTIW in the IOST under control of IOSTCW when the SIO instruction is designated. No IOST interrupt is initiated for storing this IOSTIW.

Figure 6-4 illustrates the IOSTIW format used during tracing of an SIO instruction.



Figure 6-4. IOSTIW Format for Tracing SIO Instruction

If an interface-time-over (IOT) occurs during SIO instruction execution, a 3-word IOSTIW is formed in the processing unit and stored in the IOST to initiate an IOST interrupt.

Figure 6-5 illustrates the format for the 3-word IOSTIW.



Figure 6-5. IOST Words for IOT

### 6.3.7. Halt I/O Instruction

When a halt I/O instruction (HIO) is issued to the IOST, it enters the suspended state.

The suspended state is cancelled by either of the following:

- An SIO instruction to the IOST

- Resetting the processing unit

When the suspended state is cancelled, bits 24 to 31 of the HIO instruction are set to 0, and no device address allocation is made.

The IOST responds to the HIO instruction with a condition code:

| | |
|---|---|
| CC = 00 (binary) | Indicates the IOST is in normal state. The HIO instruction resets the normal state and the I/O tabler enters suspended state. |
| CC = 11 (binary) | Indicates the IOST in not in normal state. The HIO instruction issued is rejected and the IOST remains in suspended state. |

# Appendix A. Abbreviations and Acronyms

**A**

| | |
|---|---|
| ANSI | American National Standards Institute |
| ASCII | American National Standard Coded for Information Interchange |

**B**

| | |
|---|---|
| BCSW | buffered channel status word |
| BCSWSE | buffer channel status word error |
| BMU | basic memory unit |
| B-MUX | byte multiplexer |
| BSC | binary synchronous |
| BPI | bits per inch |
| BPS | bits per second |
| BPU | basic processing unit |

**C**

| | |
|---|---|
| CA | communications adapter |
| CBC | check block code |
| CBW | channel buffer word |
| CC | condition code |
| CE | high speed buffer storage error |
| CHC | channel controller |
| CMM | communications multiplexer |
| COS | control storage |
| CPM | cards per minute |
| CPU | central processing unit |
| CRT | cathode ray tube |
| CS | check stop |
| CTO | channel time out |
| CTS | clear to send |
| CW | control word |
| CWE | control word exception |

**D**

| | |
|---|---|
| D | delayed machine check interrupt, divide, displacement field |
| DCP | distributed communications processor |
| DCT | data communications terminal |
| DE | storage control error |
| DM | degradation mask |
| DTR | data terminal ready |
| DVCB | device control block |

**E**

| | |
|---|---|
| EBCDIC | Extended Binary Coded Decimal Interchange Code |
| ECC | error check and correction |
| ED | edit or external damage |
| EDMK | edit and mark |
| EM | external damage mask |
| EMS | emergency stop |
| EOF | end of field |
| ERID | error identification code |
| EX | execute |

**F**

| | |
|---|---|
| FM | frequency modulated |
| FMA | failing memory address |

**H**

| | |
|---|---|
| HDA | head disk assembly |
| HZ | hertz |

**I**

| | |
|---|---|
| IDCU | integrated disk control unit |
| IDE | interrupt data error |
| IED | input/output external damage |
| IEDS | I/O external damage subarea code |
| IIS | interrupt initialization sequence |
| ILC | instruction length code |
| IMPL | initial microprogram load |
| I/O | input/output |
| IOMP | input/output microprocessor |
| IOP | input/output processor |
| IORB | input/output request block |
| IOST | input/output status tabler |
| IOSTCW | input/output status tabler control word |
| IOSTIW | input/output status tabler interrupt word |
| IOSTSW | input/output status tabler service word |
| IOT | interface stall timer timeout |

**I**

| | |
|---|---|
| IPL | initial program load |
| IPR | interface parity error |
| IPS | inches per second |
| ISC | integrated selector channel |
| ISO | International Organization for Standardization |
| ISR | interrupt selective reset |
| ITR | interval timer register |
| IWE | interrupt word error |

**K**

| | |
|---|---|
| KB | kilobyte |
| KBPS | thousand (kilo) bits per second |
| KE | key storage error |

**L**

| | |
|---|---|
| LPI | lines per inch |
| LPM | lines per minute |
| LS | line sensitivity |

**M**

| | |
|---|---|
| M | meter |
| MB | megabyte |
| MBA | M-bus adapter |
| MC | monitor call, machine check, machine clear |
| MCIC | machine check interrupt code |
| MCU | memory control unit |
| MFM | modulated frequency modulation |
| MIA | mainframe interface adapter |
| MS | milliseconds, modem speed, main storage |
| MSU | main storage unit |
| MWSC | maintenance workstation controller |

**O**

| | |
|---|---|
| OCR | optical character reader |
| OP | operation |

**P**

| | | |
|---|---|---|
| PCA | peripheral channel adapter |
| PD | processing damage |
| PDN | public data network |
| PE | phase encoded |
| PER | program event recording |
| PEX | program exception |
| PPC | paper peripheral controller |
| PR | problem register |
| PROM | programmable read-only memory |
| PSW | program status word |
| PTE | patrol error |
| PX | program exception |
| PXM | program exception hardware mask |

**R**

| | |
|---|---|
| RAM | random access memory |
| ROM | read only memory |
| RPM | rotations per minute |

**S**

| | |
|---|---|
| SCP | system control processor |
| SD | system damage |
| SDMA | shared direct memory access |
| SE | storage 2-bit error |
| SEL | selector channel |
| SLCA | single line communications adapter |
| STR | service timer register |
| SV | system function of service processor |
| SVP | service processor |

**T**

| | |
|---|---|
| TOD | time-of-day clock |
| TTY | teletypewriter equipment |

**U**

| | |
|---|---|
| USASCII | see ASCII |
| UTS | universal terminal system |

**V**

| | |
|---|---|
| V | validate |
| Vac | volts - alternating current |
| Vdc | volts - direct current |

**W**

| | |
|---|---|
| W | warning |
| W/R | simultaneous write/read |
| WSS | write sense switch |
| W/W | simultaneous write/write |

**X**

| | |
|---|---|
| XMC | transmit clock |
| XMD | transmit data |

# Index

## A

Abnormal stop state  4-10

Absolute address
  address relocation  3-33
  main storage  3-9

Active address, IOSTCW  6-4

Active count, IOSTCW  6-3

Address
  absolute and relative  3-33
  IOSTCW  6-3

Address designation format  3-2

Address generation  3-8

Address relocation
  absolute and relative addresses  3-33
  basic characteristics  3-33
  current relocation register  3-34
  description  3-32
  input/output channels  3-36
  operand  3-36
  relocation of instuction address  3-35

Address search stop function  3-68

Addressing facility and key address
  model 8  3-39
  models 10/15/20  3-43

Addressing function
  model 8  2-9
  models 10/15/20  2-21

Ancillary products  1-86

Arbitrary address stop function  3-68

Area codes  4-29

Automatic recovery, system  5-3

## B

Basic processing unit (BPU), models 10/15/20
  description  2-15
  registers  2-16

Branching, PER  3-76

Buffered channel status word  6-2

Byte adapter configuration  1-10

Byte multiplexer channel, model 8  2-13

# K

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