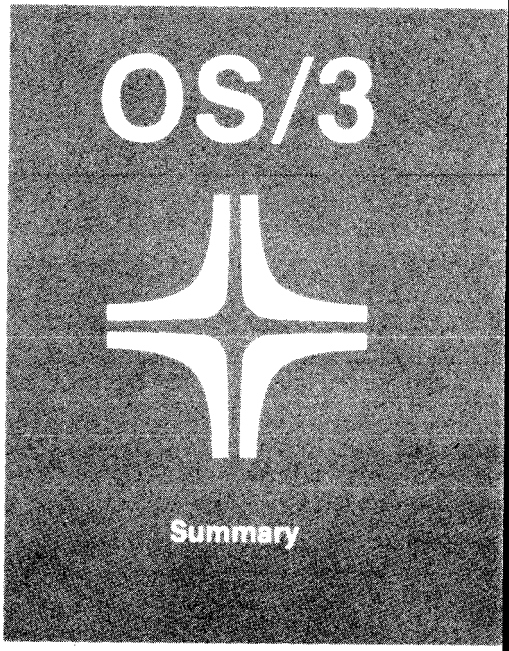
Hardware and Software



Environment: System 80

90/30 version is UP-8203

UP-8868
Rev. 1

SPERRY UNIVAC

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Preface

This document is one in a series designed to describe the hardware and software of the SPERRY UNIVAC System 80 and the Operating System/3 (OS/3). This particular summary is a quick-reference manual for use in detecting hardware errors and in analyzing dumps. It is not necessary to understand the content of this manual to successfully use System 80.

This manual consists of tables and figures abstracted from other OS/3 publications. The information presented is limited to facts; no introductory information or examples of use are provided. The descriptive information for the subjects summarized in this manual is contained in the System 80 processor programmer reference, UP-8881 (current version), the I/O integrated controllers programmer reference, UP-8742 (current version), the OS/3 assembler user guide, UP-8913 (current version), and the supervisor macroinstructions user guide/programmer reference, UP-8832 (current version).

The manual is divided into the following sections:

- Section 1. General

  Contains information of a general nature, including EBCDIC and ASCII character sets, tables for conversion, and a table for hexadecimal-decimal conversion.

- Section 2. Machine Code

  Contains information about the formats and functions of the general machine instructions. Instructions are listed by machine code and instruction name.

- Section 3. Supervisor

  Contains OS/3 supervisor related information such as the program status word (PSW) format, the control register format, the layout for low-order main storage, the input formats for the monitor and trace functions, and a summary of the system debugging aids.

- Section 4. PIOCS

  Contains information primarily related to the OS/3 physical input/output control system, including the peripheral device addresses, command codes, status byte definitions, and I/O sense data byte definitions. This information cannot be used by a programmer for developing programs with physical I/O level interface.

- Appendixes

  Contain the powers of 2 and powers of 16 tables for convenience and quick reference.

Contents

Statement Conventions

Capital letters, parentheses, and punctuation marks	Must be coded exactly as shown
Lowercase letters and terms	Represent information supplied by the programmer
Braces { }	Necessary entries from which one must be chosen
Brackets [ ]	Optional entries
Ellipsis . . .	Indefinite number of entries
Shading ▒▒	Default option
Underlining ___	Only the underlined portion of the entry need be specified.

1.2. ASCII CHARACTER CODES

(American Standard Code for Information Interchange)

ASCII Character Codes

	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	'	p
1	SOH	DC1	! ①	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w

8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	¦
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^①	n	~
F	SI	US	/	?	O	—	o	DEL

② ③ ④

NOTES:

Some graphic, card code, and hexadecimal assignments may differ depending upon the device, language, application, or installation policy.

① The following optional graphics can be substituted in the character set:

¬ for ^

| for ¦

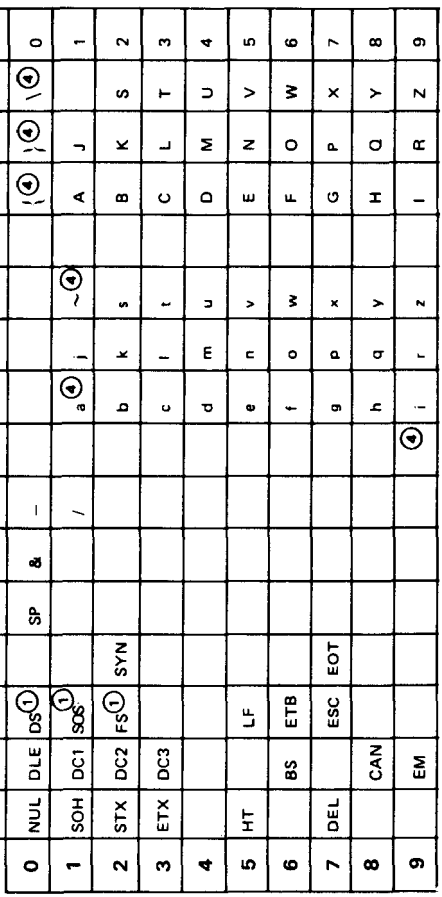
② Sixty-three printable character set

③ Graphics available by use of the type 0768-02 printer, which prints a 94-character set (DEL is not a graphic).

④ Ninety-four printable character set.

1.3. EBCDIC CHARACTER CODES

(Extended Binary Coded Decimal Interchange Code)



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NUL	DLE	DS(1)		SP	&	-						!(4)	!(4)	\(4)	0
1	SOH	DC1	SOS(1)				/		a(4)	j	~(4)		A	J		1
2	STX	DC2	FS(1)	SYN					b	k	s		B	K	S	2
3	ETX	DC3							c	l	t		C	L	T	3
4									d	m	u		D	M	U	4
5	HT		LF						e	n	v		E	N	V	5
6		BS	ETB						f	o	w		F	O	W	6
7	DEL		ESC	EOT					g	p	x		G	P	X	7
8		CAN							h	q	y		H	Q	Y	8
9		EM						(4)	i	r	z		I	R	Z	9

EBCDIC Character Codes

A					[¢	]⑤	;③	:								
B	VT				.	$	,	#								
C	FF	FS⑤		DC4⑥	<	*	%	@								
D	CR	GS⑤	ENQ	NAK	(	)	—	'								
E	SO⑤	RS⑤	ACK		+	;	>	=								
F	SI⑤	US⑤	BEL	SUB	!②⑤	¬②	?	"								

NOTES:

Some graphic, card code, and hexadecimal assignments may differ depending upon the device, language, application, or installation policy.

① DS, SOS, FS are the control characters for the EDIT instruction and have been assigned for ASCII mode processing so as not to conflict with the corresponding character positions previously assigned in the EBCDIC chart. As these characters are not outside the range as defined in ANSI X3.4 – 1968, they must not appear in external storage media, such as ANSI standard tapes. This presents no difficulty due to the nature of the EDIT instruction.

② The following optional graphics can be substituted in the character set:

^ for ¬ | for ¦

③ For 63-character printers, the following substitution is made:

\ for ¦

④ The lowercase alphabet and indicated graphics are introduced by use of the type 0768–02 printer, which prints a 94-character set.

⑤ The following substitutions are made for the UTS 400 handler:

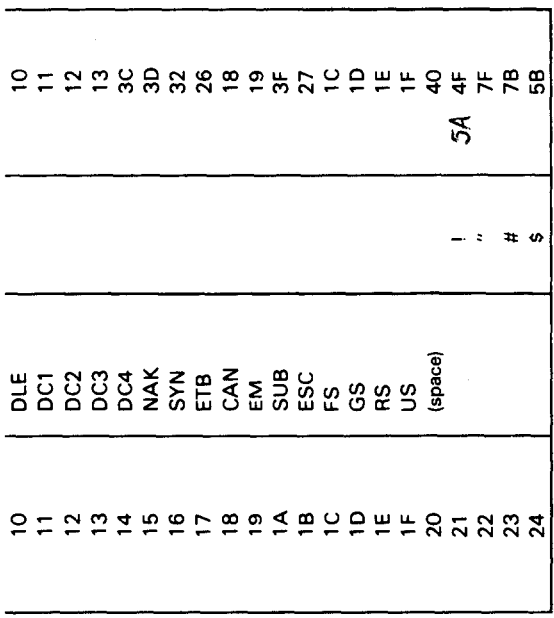
SPROT	(start protected) for SO	FCC	(field control character) for US
EPROT	(end protected) for SI	MW	(message writing) for BEL
SB	(start blink) for FS	]	for ¦
EB	(end blink) for GS	¦	for]
SOE	(start of entry) for RS		

⑥ DC4 for the UTS 400 handler

Hexadecimal Character Codes

ASCII Hexadecimal	Control Character	Symbol	EBCDIC Hexadecimal
00	NUL		00
01	SOH		01
02	STX		02
03	ETX		03
04	EOT		37
05	ENQ		2D
06	ACK		2E
07	BEL		2F
08	BS		16
09	HT		05
0A	LF		25
0B	VT		0B
0C	FF		0C
0D	CR		0D
0E	SO		0E
0F	SI		0F

HEXADECIMAL CONVERSION TABLE FOR DUMP ANALYSIS (cont)



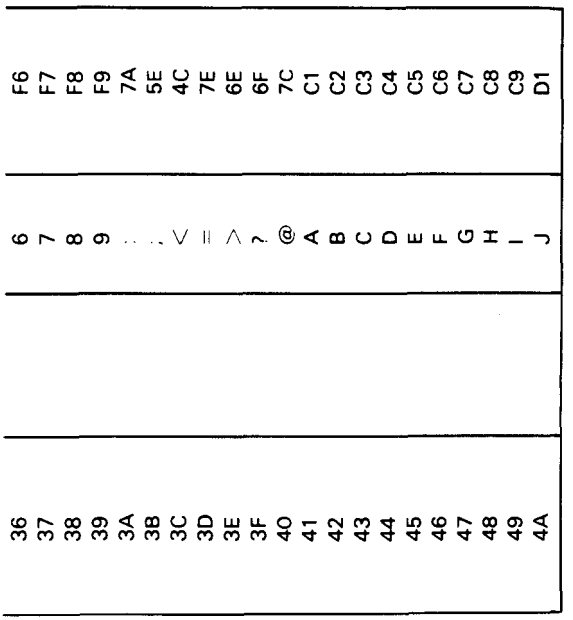
10	DLE			10
11	DC1			11
12	DC2			12
13	DC3			13
14	DC4			3C
15	NAK			3D
16	SYN			32
17	ETB			26
18	CAN			18
19	EM			19
1A	SUB			3F
1B	ESC			27
1C	FS			1C
1D	GS			1D
1E	RS			1E
1F	US			1F
20	(space)			40
21		!		4F
22		"		7F
23		#		7B
24		$		5B

5A

Hexadecimal Character Codes (cont)

ASCII Hexadecimal	Control Character	Symbol	EBCDIC Hexadecimal
25		%	6C
26		&	50
27		'	7D
28		(	4D
29		)	5D
2A		*	5C
2B		+	4E
2C		,	6B
2D		-	60
2E		.	4B
2F		/	61
30		0	F0
31		1	F1
32		2	F2
33		3	F3
34		4	F4
35		5	F5

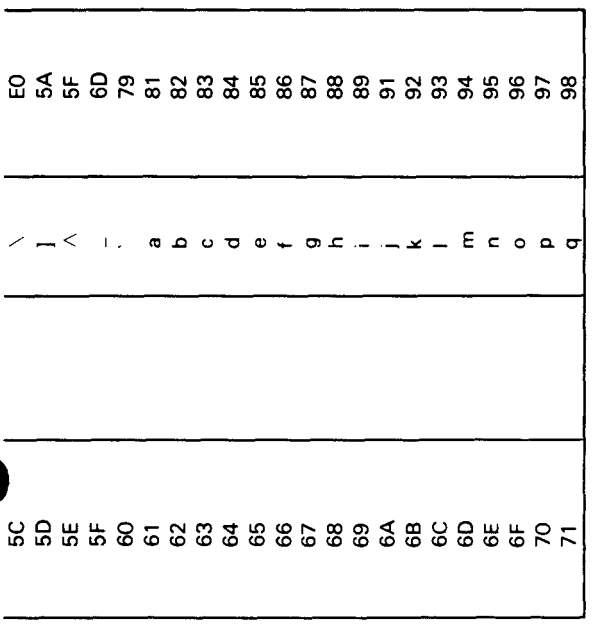
HEXADECIMAL CONVERSION TABLE FOR DUMP ANALYSIS (cont)



Hexadecimal Character Codes (cont)

ASCII Hexadecimal	Control Character	Symbol	EBCDIC Hexadecimal
4B		K	D2
4C		L	D3
4D		M	D4
4E		N	D5
4F		O	D6
50		P	D7
51		Q	D8
52		R	D9
53		S	E2
54		T	E3
55		U	E4
56		V	E5
57		W	E6
58		X	E7
59		Y	E8
5A		Z	E9
5B		[	4A

HEXADECIMAL CONVERSION TABLE FOR DUMP ANALYSIS (cont)



Hexadecimal Character Codes (cont)

ASCII Hexadecimal	Control Character	Symbol	EBCDIC Hexadecimal
72		r	99
73		s	A2
74		t	A3
75		u	A4
76		v	A5
77		w	A6
78		x	A7
79		y	A8
7A		z	A9
7B			C0
7C			4F 6A
7D			D0
7E			A1
7F	DEL		07*
80	ISR		20*
81	SSB		21*
82	FSB		22*

*For edit mask conversion only.

Character Conversion Table

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
Letters						
A	A	12–1	41	65	C1	193
B	B	12–2	42	66	C2	194
C	C	12–3	43	67	C3	195
D	D	12–4	44	68	C4	196
E	E	12–5	45	69	C5	197
F	F	12–6	46	70	C6	198
G	G	12–7	47	71	C7	199
H	H	12–8	48	72	C8	200

Character Conversion Table (cont)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
I	I	12—9	49	73	C9	201
J	J	11—1	4A	74	D1	209
K	K	11—2	4B	75	D2	210
L	L	11—3	4C	76	D3	211
M	M	11—4	4D	77	D4	212
N	N	11—5	4E	78	D5	213
O	O	11—6	4F	79	D6	214
P	P	11—7	50	80	D7	215

CHARACTER CONVERSION TABLE (cont)

Q	Q	11-8	51	81	D8	216
R	R	11-9	52	82	D9	217
S	S	0-2	53	83	E2	226
T	T	0-3	54	84	E3	227
U	U	0-4	55	85	E4	228
V	V	0-5	56	86	E5	229
W	W	0-6	57	87	E6	230
X	X	0-7	58	88	E7	231
Y	Y	0-8	59	89	E8	232
Z	Z	0-9	5A	90	E9	233

Character Conversion Table (cont)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
a	a	12–0–1	61	97	81	129
b	b	12–0–2	62	98	82	130
c	c	12–0–3	63	99	83	131
d	d	12–0–4	64	100	84	132
e	e	12–0–5	65	101	85	133
f	f	12–0–6	66	102	86	134
g	g	12–0–7	67	103	87	135
h	h	12–0–8	68	104	88	136
i	i	12–0–9	69	105	89	137

j	j	12—11—1	6A	106	91	145
k	k	12—11—2	6B	107	92	146
l	l	12—11—3	6C	108	93	147
m	m	12—11—4	6D	109	94	148
n	n	12—11—5	6E	110	95	149
o	o	12—11—6	6F	111	96	150
p	p	12—11—7	70	112	97	151
q	q	12—11—8	71	113	98	152
r	r	12—11—9	72	114	99	153

Character Conversion Table (cont)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
s	s	11—0—2	73	115	A2	162
t	t	11—0—3	74	116	A3	163
u	u	11—0—4	75	117	A4	164
v	v	11—0—5	76	118	A5	165
w	w	11—0—6	77	119	A6	166
x	x	11—0—7	78	120	A7	167
y	y	11—0—8	79	121	A8	168
z	z	11—0—9	7A	122	A9	169

CHARACTER CONVERSION TABLE (cont)

Numerals						
0	0	0	30	48	F0	240
1	1	1	31	49	F1	241
2	2	2	32	50	F2	242
3	3	3	33	51	F3	243
4	4	4	34	52	F4	244
5	5	5	35	53	F5	245
6	6	6	36	54	F6	246
7	7	7	37	55	F7	247

Character Conversion Table (cont)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
8	8	8	38	56	F8	248
9	9	9	39	57	F9	249
Symbols						
Exclamation point	!	11-2-8 12-8-7	21	33	4F 5A	90 79
Quotation mark, dieresis	"	8-7	22	34	7F	127
Number sign, pound sign	#	8-3	23	35	7B	123
Dollar sign	$	11-8-3	24	36	5B	91
Percent sign	%	0-8-4	25	37	6C	108
Ampersand	&	12	26	38	50	80

Apostrophe, acute accent	'	8–5	27	39	7D	125
Opening parenthesis	(	12–8–5	28	40	4D	77
Closing parenthesis	)	11–8–5	29	41	5D	93
Asterisk	*	11–8–4	2A	42	5C	92
Plus sign	+	12–8–6	2B	43	4E	78
Comma, cedilla	,	0–8–3	2C	44	6B	107
Minus sign, hyphen	–	11	2D	45	60	96
Period, decimal point	.	12–8–3	2E	46	4B	75
Slash, virgule, solidus	/	0–1	2F	47	61	97
Colon	:	8–2	3A	58	7A	122

Character Conversion Table (cont)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
Semicolon	;	11-8-6	3B	59	5E	94
Less than	<	12-8-4	3C	60	4C	76
Equal sign	=	8 6	3D	61	7E	126
Greater than	>	0 8 6	3E	62	6E	110
Question mark	?	0 8-7	3F	63	6F	111
Commercial at symbol	@	8 4	40	64	7C	124
Opening bracket	[	12 8 2	5B	91	4A	74
Closing bracket	]	11 8-2	5D	93	5A	90
Reverse slash	\	0-8 2	5C	92	E0	224

Circumflex	^	11—8—7	5E	94	5F	95
Underline	—	0—8—5	5F	95	6D	109
Grave accent	`	8—1	60	96	79	121
Opening brace	{	12—0	7B	123	C0	192
Closing brace	}	11—0	7D	125	D0	208
Vertical line	|	12—11 12-7-8	7C	124	4F 6A	79 106
Overline, tilde	~	11—0—1	7E	126	A1	161

Character Conversion Table (cont)

Character	Card Punches	ASCII		EBCDIC	
		Hexadecimal	Decimal	Hexadecimal	Decimal
Nonprintable Characters					
ACK (acknowledge)	0—9—8—6	06	6	2E	46
BEL (bell)	0—9—8—7	07	7	2F	47
BS (backspace)	11—9—6	08	8	16	22
CAN (cancel)	11—9—8	18	24	18	24
CR (carriage return)	12—9—8—5	0D	13	0D	13
DC1 (device control 1)	11—9—1	11	17	11	17
DC2 (device control 2)	11—9—2	12	18	12	18
DC3 (device control 3)	11—9—3	13	19	13	19

DC4 (device control 4)	9-8-4	14	20	3C	60
DEL (delete)	12-9-7	7F	127	07	7
DLE (data link escape)	12-11-9-8-1	10	16	10	16
DS (digit select)	11-0-9-8-1	80	128	20	32
EM (end of medium)	11-9-8-1	19	25	19	25
ENQ (enquiry)	0-9-8-5	05	5	2D	45
EOT (end of transmission)	9-7	04	4	37	55
ESC (escape)	0-9-7	1B	27	27	39
ETB (end of transmission block)	0-9-6	17	23	26	38

Character Conversion Table (cont)

Character	Card Punches	ASCII		EBCDIC	
		Hexadecimal	Decimal	Hexadecimal	Decimal
ETX (end of text)	12–9–3	03	3	03	3
FF (form feed)	12–9–8–4	0C	12	0C	12
FS (file separator)	11–9–8–4	1C	28	1C	28
FS (field separator)	0–9–2	82	130	22	34
GS (group separator)	11–9–8–5	1D	29	1D	29
HT (horizontal tabulation)	12–9–5	09	9	05	5
LF (line feed)	0–9–5	0A	10	25	37
NAK (negative acknowledge)	9–8–5	15	21	3D	61
NUL (null)	12–0–9–8–1	00	0	00	0

CHARACTER CONVERSION TABLE (cont)

RS (record separator)	11-9-8-6	1E	30	1E	30
SI (shift in)	12-9-8-7	0F	15	0F	15
SO (shift out)	12-9-8-6	0E	14	0E	14
SOH (start of heading)	12-9-1	01	1	01	1
SOS (significance start)	0-9-1	81	129	21	33
SP (space)		20	32	40	64
STX (start of text)	12-9-2	02	2	02	2
SUB (substitute)	9-8-7	1A	26	3F	63
SYN (synchronous idle)	9-2	16	22	32	50
US (unit separator)	11-9-8-7	1F	31	1F	31
VT (vertical tabulation)	12-9-8-3	0B	11	0B	11

1.6. HEXADECIMAL-DECIMAL CONVERSION TABLE

Hexadecimal-Decimal Conversion Table

Hexadecimal to Decimal:

Working from right to left with the hexadecimal digits to be converted, select the decimal number from the digit position column corresponding to each hexadecimal digit. Add the selected decimal numbers to complete the conversion.

Decimal to Hexadecimal

1. Select the highest decimal number from the table that is less than the decimal number to be converted.
2. Subtract this number from the number to be converted.
3. Note the corresponding hexadecimal digit, its digit position, and the difference.
4. Substitute the difference for the decimal number to be converted and repeat steps 1 and 2 until a zero difference is obtained.
5. Include a 0 for each unused digit position.

The resulting hexadecimal number is the conversion.

Hexadecimal Digit Positions											
6		5		4		3		2		1	
Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15

Hexadecimal Addition and Subtraction Table

+	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10
2	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11
3	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12
4	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13
5	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14
6	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15
7	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16
8	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17
9	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18
A	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19
B	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A
C	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

1.8. SIGN CONVENTIONS

Sign Conventions

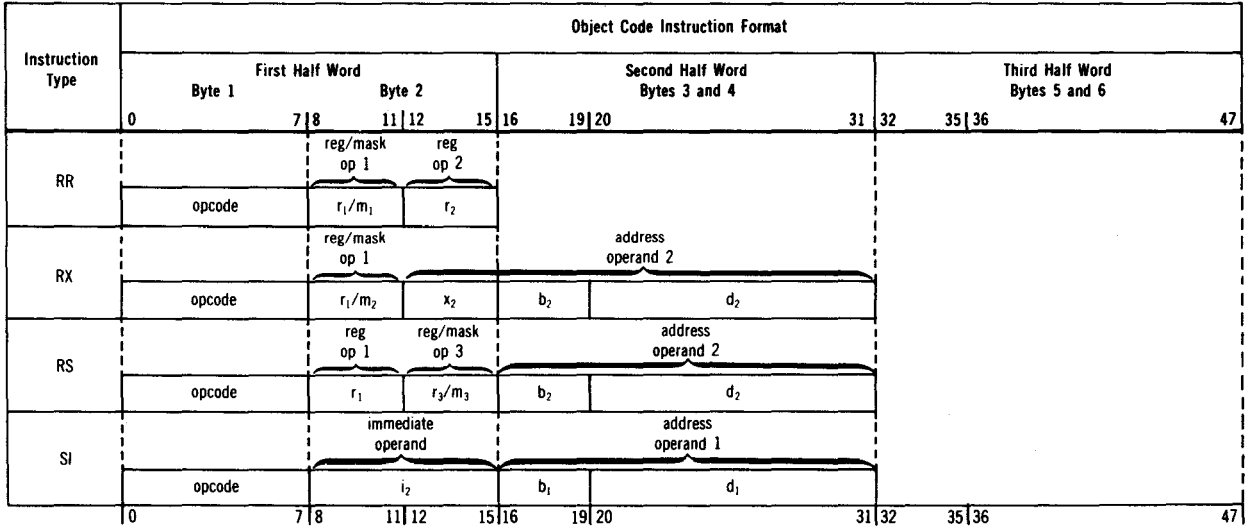
Hexadecimal Representation		Binary Representation	Sign	
Generation	Digit		Value	Mode
External	A	1010	Positive	ASCII
	B	1011	Negative	
Processor	C	1100	Positive	EBCDIC
	D	1101	Negative	
External	E	1110	Positive	
	F	1111	Positive	

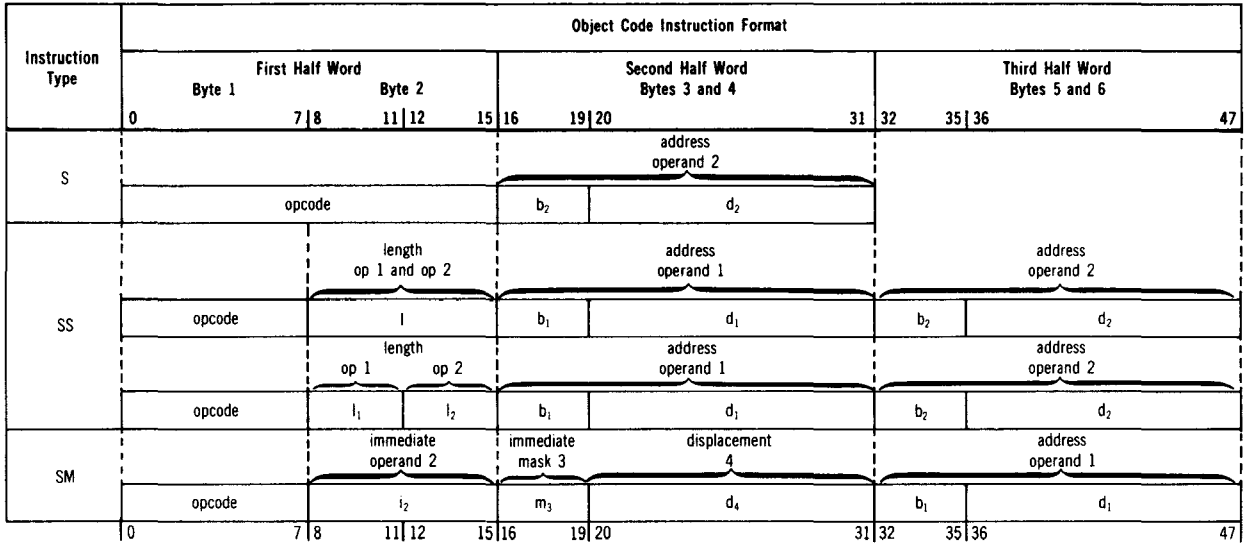
1.9. LINKAGE REGISTER CONVENTIONS

Linkage Register Conventions

Register	Contents
0	Reserved for system use
1	Parameter/list register
2-12	Free registers
13	Save area register
14	Return address register
15	Entry point register

2.1.1. Instruction Formats




Object Code Instruction Format
Instruction Type
First Half Word
Byte 1
Byte 2
Second Half Word
Bytes 3 and 4
Third Half Word
Bytes 5 and 6
0 7 8 11 12 15 16 19 20 31 32 35 36 47
S
address operand 2
opcode
b2
d2
SS
length op 1 and op 2
address operand 1
address operand 2
opcode
l
b1
d1
b2
d2
length op 1
op 2
address operand 1
address operand 2
opcode
l1
l2
b1
d1
b2
d2
SM
immediate operand 2
immediate mask 3
displacement 4
address operand 1
opcode
i2
m3
d4
b1
d1
0 7 8 11 12 15 16 19 20 31 32 35 36 47

Characters	Meaning
OPCODE	The application instruction operation code.
r_1	The number of the general register containing operand 1
r_2	The number of the general register containing operand 2
r_3	The number of the general register containing operand 3
x_2	The number of the general register containing an index number for operand 2 of the RX instruction
i_2	The immediate data used as operand 2 of an SI instruction
l	The length of the operands as stated in object code*
l_1	The length of operand 1 as stated in object code*
l_2	The length of operand 2 as stated in object code*
b_1	The number of the general register containing the base address for operand 1
b_2	The number of the general register containing the base address for operand 2
d_1	The displacement for the base address of operand 1
d_2	The displacement for the base address of operand 2
d_4	The displacement used as operand 4 of an SM instruction
m_1	The mask used as operand 1
m_3	The mask used as operand 3
op_1	Operand 1
op_2	Operand 2
op_3	Operand 3

*Always one less than actual length.

2.1.2.1. **Instructions by Machine Code**

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
03	Service timer register	RR	(privileged)		PR, SP	25
04	Set program mask	RR	$PSW_{34-39} \leftarrow R1_{2-7}$	18		
05	Branch and link	RR	$R1 \leftarrow c(PSW)_{32-39}$; $\rightarrow c(R2)$			1
06	Branch on count	RR	$R1 \leftarrow c(R1) - 1$; $\rightarrow c(R2)$ if $c(R1) \neq 0$			
07	Branch on condition	RR	$\rightarrow c(R2)$ if (M1) cc = 1			
08	Set storage key	RR	(privileged; featured)		AC, OP, PR, SP	
09	Insert storage key	RR	(privileged; featured)		AC, OP, PR, SP	
0A	Supervisor call	RR	SVC interrupt; $(\text{old SVC PSW})_{24-31} \leftarrow I1$	19		
0B	Get IORB	RR	(privileged)	AC, PR	25	
0C	Put IORB	RR	(privileged)	AC, PR		
0E	Move characters long	RR	$c(R1) \leftarrow c(c(R2))$	1	AC, SP	2
0F	Compare logical long	RR		2	AC, SP	2
10	Load positive	RR	$R1 \leftarrow \lvert c(R2) \rvert$	3	XO	

11	Load negative	RR	R1←−c|(R2)|	4		
12	Load and test	RR	R1←c(R2)	5		
13	Load complement	RR	R1←−c(R2)	6	XO	
14	AND	RR	R1←c(R1) AND c(R2)	7		
15	Compare logical	RR		2		
16	OR	RR	R1←c(R1) OR c(R2)	7		
17	Exclusive OR	RR	R1←c(R1) XOR c(R2)	7		
18	Load	RR	R1←c(R2)			
19	Compare	RR		2		
1A	Add	RR	R1←c(R1) + c(R2)	6	XO	
1B	Subtract	RR	R1←c(R1) — c(R2)	6	XO	
1C	Multiply	RR	[R1,R1 + 1]←c(R1 + 1) x c(R2)		SP	
1D	Divide	RR	R1←Remainder of [c(R1),c(R1 + 1)] /c(R2); R1 + 1←Quotient of [c(R1),c(R1 + 1)] /c(R2)		SP, XD	

Instructions by Machine Code (cont)

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
1E	Add logical	RR	R1←c(R1) + c(R2)	8		
1F	Subtract logical	RR	R1←c(R1) — c(R2)	16		
20	Load positive, long	RR	FPR1←|c(FPR2)|	15	SP	3, 4
21	Load negative, long	RR	FPR1← — |c(FPR2)|	4	SP	3, 4
22	Load and test, long	RR	FPR1←c(FPR2)	5	SP	3, 4
23	Load complement, long	RR	FPR1← — c(FPR2)	5	SP	3, 4
24	Halve, long	RR	FPR1←c(FPR2)/2		SP, EU	3, 4
28	Load, long	RR	FPR1←c(FPR2)		SP	3, 4
29	Compare, long	RR		2	SP	3, 4
2A	Add normalized, long	RR	FPR1←c(FPR1) + c(FPR2)	5	SP, EO, EU, SG	3, 4
2B	Subtract normalized, long	RR	FPR1←c(FPR1) — c(FPR2)	5	SP, EO, EU, SG	3, 4
2C	Multiply, long	RR	FPR1←c(FPR1) x c(FPR2)		SP, EO, EU	3, 4

2D	Divide, long	RR	FPR1←c(FPR1)/c(FPR2)		SP, EO, EU, FD	3, 4
2E	Add unnormalized, long	RR	FPR1←c(FPR1) + c(FPR2)	5	SP, EO, SG	3, 4, 5
2F	Subtract unnormalized, long	RR	FPR1←c(FPR1) — c(FPR2)	5	SP, EO, SG	3, 4, 5
30	Load positive, short	RR	FPR1←|c(FPR2)|	15	SP	3
31	Load negative, short	RR	FPR1←|c(FPR2) — |	4	SP	3
32	Load and test, short	RR	FPR1←c(FPR2)	5	SP	3
33	Load complement, short	RR	FPR1← — c(FPR2)	5	SP	3
34	Halve, short	RR	FPR1←c(FPR2)/2		SP, EU	3
38	Load, short	RR	FPR1←c(FPR2)		SP	3
39	Compare, short	RR		2	SP	3
3A	Add normalized, short	RR	FPR1←c(FPR1) + c(FPR2)	5	SP, EO, EU, SG	3
3B	Subtract normalized, short	RR	FPR1←c(FPR1) — c(FPR2)	5	SP, EO, EU, SG	3
3C	Multiply, short	RR	FPR1←c(FPR1) x c(FPR2)		SP, EO, EU	3
3D	Divide, short	RR	FPR1←c(FPR1)/c(FPR2)		SP, EO, EU, FD	3

Instructions by Machine Code (cont)

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
3E	Add unnormalized, short	RR	FPR1←c(FPR1) + c(FPR2)	5	SP, EO, SG	3, 5
3F	Subtract unnormalized, short	RR	FPR1←c(FPR1) — c(FPR2)	5	SP, EO, SG	3, 5
40	Store half word	RX	$S2_{0-15}$←$c(R1)_{16-31}$		AC, SP	
41	Load address	RX	$R1_{8-31}$←S2; $R1_{0-7}$←0			
42	Store character	RX	$S2_{0-7}$←$c(R1)_{24-31}$		AC	
43	Insert character	RX	$R1_{24-31}$←$c(S2)_{0-7}$		AC	
44	Execute	RX	Execute subject instruction at S2, modified by $c(R1)_{24-31}$	20	AC, SP, EX	6
45	Branch and link	RX	R1←$c(PSW)_{32-63}$; →S2			
46	Branch on count	RX	R1←c(R1)—1; →S2 if c(R1)≠0			
47	Branch on condition	RX	→S2 if $(M1)_{CC}$=1			
48	Load half word	RX	$R1_{16-31}$←$c(S2)_{0-15}$; $R1_{0-15}$←$c(S2)_0$		AC, SP	

49	Compare half word	RX		2	AC, SP	7
4A	Add half word	RX	R1←c(R1) + $c(S2)_{0-15}$	6	AC, SP, XO	7
4B	Subtract half word	RX	R1←c(R1) — $c(S2)_{0-15}$	6	AC, SP, XO	7
4C	Multiply half word	RX	R1←$(c(R1) \times c(S2)_{0-15})_{16-47}$		AC, SP	7
4E	Convert to decimal	RX	$S2_{0-63}$ (packed decimal)←c(R1) (binary)		AC, SP	
4F	Convert to binary	RX	R1(binary)←$c(S2)_{0-63}$ (packed decimal)		AC, SP, DT, XD	
50	Store	RX	S2←c(R1)		AC, SP	
51	Load directive address	RX	(privileged)		AC, PR, SP	
54	AND	RX	R1←c(R1) AND c(S2)	7	AC, SP	
55	Compare logical	RX		2	AC, SP	
56	OR	RX	R1←c(R1) OR c(S2)	7	AC, SP	
57	Exclusive OR	RX	R1←c(R1) XOR c(S2)	7	AC, SP	
58	Load	RX	R1←c(S2)		AC, SP	
59	Compare	RX		2	AC, SP	

Instructions by Machine Code (cont)

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
5A	Add	RX	R1←c(R1) + c(S2)	6	AC, SP, XO	
5B	Subtract	RX	R1←c(R1) — c(S2)	6	AC, SP, XO	
5C	Multiply	RX	[R1,R1 + 1] ← c(R1 + 1) x c(S2)		AC, SP	
5D	Divide	RX	R1 Remainder of [c(R1),c(R1 + 1)] /c(S2); R1 + 1←Quotient of [c(R1),c(R1 + 1)] /c(S2)		AC, SP, XD	
5E	Add logical	RX	R1←c(R1) + c(S2)	8	AC, SP	
5F	Subtract logical	RX	R1←c(R1) — c(S2)	16	AC, SP	
60	Store, long	RX	S2←c(FPR1)		AC, SP	3, 4
61	Load I/O address	RX	(privileged)		PR, SP	
68	Load, long	RX	FPR1←c(S2)		AC, SP	3, 4
69	Compare, long	RX		2	AC, SP	3, 4

6A	Add normalized, long	RX	FPR1←c(FPR1) + c(S2)	5	AC, SP, EU, EO, SG	3, 4
6B	Subtract normalized, long	RX	FPR1←c(FPR1) — c(S2)	5	AC, SP, EU, EO, SG	3, 4
6C	Multiply, long	RX	FPR1←c(FPR1) x c(S2)		AC, SP, EU, EO	3, 4
6D	Divide, long	RX	FPR1←c(FPR1)/c(S2)		AC, SP, EU, EO, FD	3, 4
6E	Add unnormalized, long	RX	FPR1←c(FPR1) + c(S2)	5	AC, SP, EO, SG	3, 4, 5
6F	Subtract unnormalized, long	RX	FPR1←c(FPR1) — c(S2)	5	AC, SP, EO, SG	3, 4, 5
70	Store, short	RX	S2←c(FPR1)		AC, SP	3
78	Load, short	RX	FPR1←c(S2)		AC, SP	3
79	Compare, short	RX		2	AC, SP	3
7A	Add normalized, short	RX	FPR1←c(FPR1) + c(S2)	5	AC, SP, EU, EO, SG	3
7B	Subtract normalized, short	RX	FPR1←c(FPR1) — c(S2)	5	AC, SP, EU, EO, SG	3
7C	Multiply, short	RX	FPR1←c(FPR1) x c(S2)		AC, SP, EU, EO	3
7D	Divide, short	RX	FPR1←c(FPR1)/c(S2)		AC, SP, EU, EO, FD	3
7E	Add unnormalized, short	RX	FPR1←c(FPR1) + c(S2)	5	AC, SP, EO, SG	3, 5

Instructions by Machine Code (cont)

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
7F	Subtract unnormalized, short	RX	FPR1←c(FPR1) — c(S2)	5	AC, SP, EO, SG	3, 5
80	Set system mask	S	(privileged)		AC, PR	
81	Move I/O	RS	(privileged)		AC, PR, SP	25
82	Load PSW	S	(privileged)		AC, PR, SP	25
8300	Execute diagnose	S	(privileged)		AC, EX, PR, SP	25
8301	Reset	S	(privileged)		OP, PR, SP	25
8302	Store status	S	(privileged)		AC, OP, PR, SP	
8303	Initial program load	S	(privileged)		PR	
830E	Longitudinal redundancy check	S	(privileged)		AC, PR, SP	25
830F	Switch list scan	S	(privileged)		PR, SP	25
86	Branch on index high	RS	R1←c(R1) + c(R3); if R3 is odd, →S2 if c(R1)>c(R3); if R3 is even, →S2 if c(R1)>c(R3 + 1)			

87	Branch on index low or equal	RS	R1←c(R1) + c(R3); if R3 is odd, →S2 if c(R1)≤c(R3); if R3 is even, →S2 if c(R1)≤c(R3+1)			
88	Shift right single logical	RS	Right shift $(R1)_{0-31}$, fill with 0's			8
89	Shift left single logical	RS	Left shift $(R1)_{0-31}$, fill with 0's			8
8A	Shift right single	RS	Right shift $(R1)_{1-31}$, fill with $c(R1)_0$	5		8
8B	Shift left single	RS	Left shift $(R1)_{1-31}$, fill with 0's	6	XO	8
8C	Shift right double logical	RS	Right shift $[R1,R1 + 1]_{0-63}$, fill with 0's		SP	8
8D	Shift left double logical	RS	Left shift $[R1,R1 + 1]_{0-63}$, fill with 0's		SP	8
8E	Shift right double	RS	Right shift $[R1,R1 + 1]_{1-63}$, fill with $c(R1)_0$	5	SP	8
8F	Shift left double	RS	Left shift $[R1,R1 + 1]_{1-63}$, fill with 0's	6	SP, XO	8
90	Store multiple	RS	S2,...←c(R1),c(R1 + 1),...,c(R3)		AC, SP	9
91	Test under mask	SI		9	AC	
92	Move immediate	SI	$S1_{0-7}$←I2		AC	

Instructions by Machine Code (cont)

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
93	Test and set	S	$S1_{0-7}$←X'FF'	10	AC	
94	AND immediate	SI	$S1_{0-7}$←c(S1)$_{0-7}$AND I2	7	AC	
95	Compare logical immediate	SI		2	AC	
96	OR immediate	SI	$S1_{0-7}$←c(S1)$_{0-7}$ OR I2	7	AC	
97	Exclusive OR immediate	SI	$S1_{0-7}$←c(S1)$_{0-7}$ XOR I2	7	AC	
98	Load multiple	RS	R1, R1 + 1,...,R3←c(S2)		AC, SP	9
99	Halt and proceed	SI	(privileged)		PR	
9A	Add immediate	SI	$S1_{0-15}$←$S1_{0-15}$ + I2	6	AC, SP, XO	10
9B	Shift logical	RS	Shift R1 or [R1,R1 + 1] according to M3 bits	11	SP	8, 11
9C02	Start device	S	(privileged)		AC, PR, SP	25
9DX2	Clear device	RS	(privileged)		AC, PR, SP	25

9E01	Halt device	S	(privileged)		AC, PR	25
9F02	Clear channel	S	(privileged)		AC, PR, SP	25
9F03	Load channel register	S	(privileged)		AC, PR, SP	25
A2	Store relocation register	RS	(privileged)		AC, PR, SP	
A3	Load relocation register	RS	(privileged)		AC, PR, SP	
B0	Supervisor store multiple	RS	(privileged)		AC, PR, SP	
B6	Store control	RS	(privileged)		AC, PR, SP	
B7	Load control	RS	(privileged)		AC, PR, SP	
B8	Supervisor load multiple	RS	(privileged)		AC, PR, SP	

Instructions by Machine Code (cont)

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
B9	Compare and swap under mask	RS	Compares c(S2) and c(R1 + 1) masked by c(R1); if comparands are equal, S2 (masked by c(R3)) ←c(R3 + 1)	2	AC, SP	12
BD	Compare logical characters under mask	RS		2	AC	13
BE	Store characters under mask	RS	S2←c(R1) under M3 mask		AC	13
BF	Insert characters under mask	RS	R1 (under M3 mask)←c(S2)	12	AC	13
D1	Move numerics	SS	S1←c(S2)		AC	14, 15
D2	Move	SS	S1←c(S2)		AC	14
D3	Move zones	SS	S1←c(S2)		AC	14, 16
D4	AND	SS	S1←c(S1) AND c(S2)	7	AC	14

D5	Compare logical	SS		2	AC	14
D6	OR	SS	S1←c(S1) OR c(S2)	7	AC	14
D7	Exclusive OR	SS	S1←c(S1) XOR c(S2)	7	AC	14
DC	Translate	SS	S1←c(S2)		AC	14, 17
DD	Translate and test	SS	Register 1_{8-31}←address of nonzero result byte Register 2_{24-31}←nonzero result byte	14	AC	14, 18
DE	Edit	SS	S1←c(S2)	17	AC, DT	19
DF	Edit and mark	SS	S1←c(S2); Register 1_{8-31}←address of first significant digit	17	AC, DT	19
E0	Enqueue I/O	SS	(privileged)		AC, PR, SP	25
E1	Compare logical immediate and skip	SM	→(PSW_{40-63} + D4) if condition code and M3 mask permit	13	AC, SP	20
E2	Test under mask and skip	SM	→(PSW_{40-63} + D4) if condition code and M3 mask permit	9	AC, SP	20

Instructions by Machine Code (cont)

Machine Code	Instruction Name	Type	Action*	CC Setting**	Exceptions†	Notes††
F0	Shift and round decimal	SS	c(S1) shifted right or left, rounded by factor I3	6	AC, DT, DO	8, 21
F1	Move with offset	SS	S1←c(S2)		AC	22, 23
F2	Pack	SS	S1(packed decimal)←c(S2) (zoned decimal)		AC	22
F3	Unpack	SS	S1(zoned decimal)←c(S2) (packed decimal)		AC	22
F8	Zero and add	SS	S1←packed decimal 0; S1←c(S1) + c(S2)	6	AC, DT, DO	22
F9	Compare decimal	SS		2	AC, DT	22
FA	Add decimal	SS	S1←c(S1) + c(S2)	6	AC, DT, DO	22
FB	Subtract decimal	SS	S1←c(S1) — c(S2)	6	AC, DT, DO	22
FC	Multiply decimal	SS	S1←c(S1) x c(S2)		AC, SP, DT	22
FD	Divide decimal	SS	S1←[quotient of c(S1)/c(S2), remainder of c(S1)/c(S2)]		AC, SP, DT, DD	22, 24

*The meaning of the abbreviations in this column are:

R1	the number of the general register used as operand 1
R2	the number of the general register used as operand 2
R3	the number of the general register used as operand 3
S1	the main storage address used as operand 1
S2	the main storage address used as operand 2
FPR1	the number of the floating-point register used as operand 1
FPR2	the number of the floating-point register used as operand 2
M1	the 4-bit mask used as operand 1
$(Mn)_{cc}$	the operand n mask bit corresponding to the current condition code, 0 to 3
M3	the 4-bit mask used as operand 3

Instructions by Machine Code (cont)

I1	the 8-bit immediate data used as the SVC instruction operand, bits 8—15 of the instruction
I2	the 8-bit immediate data used as operand 2
D4	the 12-bit binary displacement used as operand 4 of SM-type instructions
c(operand)	the contents of the specified operand; for example, S2 specifies the main storage address of operand 2 while c(S2) specifies the contents of operand 2.
operand $_{m[-n]}$	specifies that bit m of the operand is acted upon; if n is also specified, only bits m to n inclusive are acted upon. Bits are numbered left to right starting with 0.
[operand 1, operand 2]	concatenation of operands 1 and 2
[Rn,Rn+1]	the even-odd register pair addressed by register n.
PSW	program status word
←	replacement operator; signifies the replacement of data at the left operand with the right operand
→	branch; signifies that program control passes to the right operand location.

All operands are 32 bits long unless otherwise noted.

**The CC settings are:

1.	Op1 length = Op2 length	Op1 length < Op2 length	Op1 length > Op2 length	Destructive overlap; no move performed
2.	Op1 = Op2	Op1 < Op2	Op1 > Op2	
3.	Result = 0		Result > 0	Overflow
4.	Result = 0	Result < 0		
5.	Result = 0	Result < 0	Result > 0	
6.	Result = 0	Result < 0	Result > 0	Overflow
7.	Result = 0	Result ≠ 0		
8.	Result = 0, no carry	Result ≠ 0, no carry	Result = 0, carry	Result ≠ 0, carry

Instructions by Machine Code (cont)

9.	All selected bits = 0 or c(I2) = 0	Selected bits are mixed, some 0 and some 1		All selected bits = 1
10.	$c(S2)_0 = 0$	$c(S2)_0 = 1$		
11.	Result = 0, all 0's shifted out	Result = 0, 1 or more 1's shifted out	Result ≠ 0, all 0's shifted out	Result ≠ 0, 1 or more 1's shifted out
12.	All inserted bits = 0 or c(M3) = 0	High-order inserted bit = 1	High-order inserted bit = 0 but not all inserted bits are 0's	
13.	Op2 = Op3	Op2 < Op3	Op2 > Op3	
14.	All result bytes = 0	Result byte ≠ 0 and is not last byte of op1	Result byte ≠ 0 and is last byte of op1	
15.	Result = 0		Result > 0	
16.		Result ≠ 0, no carry	Result = 0, carry	Result ≠ 0, carry

17. Last field examined = 0 | Last field examined ≠ 0, and plus sign is not detected | Last field examined > 0

18. Set = to bit positions 2 and 3 of the first operand

19. Set = to bit positions 34 and 35 of the supervisor call new PSW (unchanged in the old PSW)

20. Condition code may be set by the subject instruction

†Exception codes, in parentheses, are those contained in program status word (PSW) bits 24—31.

AC access (protection (04) or addressing (05))

DT data (07)

DD decimal divide (0B)

DO decimal overflow (0A)

EX execute (03)

Instructions by Machine Code (cont)

EO exponent overflow (0C)

EU exponent underflow (0D)

XD fixed-point divide (09)

XO fixed-point overflow (08)

FD floating-point divide (0F)

OP operation (01)

PR privileged operation (02)

SG significance (0E)

SP specification (06)

††The explanations for this column are:

1. No branch is taken if R2 = 0.

2. Operands 1 and 2 both are even-odd register pairs. $c(R1+1)_{8-31}$ is the length of operand 1, $c(R2+1)_{8-31}$ is the length of operand 2, and $c(R2+1)_{0-7}$ is the pad byte.

3. Operands are in floating-point form and normalized except where noted.

4. Operands are 64 bits long.

5. Normalization is not performed on result.

6. Before subject instruction is executed, an OR operation using specified R1 bits is performed on bits 8—15 of the instruction.

7. Before the operation begins, the half-word operand is expanded to 32 bits by propagating $c(S2)_0$ through the high-order 16 bit positions.

8. Length of shift is given by low-order six bits of S2.

9. If R1 > R3, registers wrap around: ...,15,0,... IF R1 = R3, only that register is used. Main storage operand addresses the leftmost byte of main storage used. Length of operand is 4 bytes if R1 = R3, 4 x (R3 — R1 + 1) bytes if R3 > R1, or 4 x (R3 — R1 + 17) bytes if R3 < R1.

10. Prior to addition, the immediate operand is expaned to 16 bits, $(I2)_0$ being propagated through the high-order 8 bits.

11. Bits 12—15 in the instruction govern the shift as follows:

Bit 12: 0	discard bits shifted out; 1	circular shift
Bit 13: 0	shift left; 1	shift right

Instructions by Machine Code (cont)

Bit 14: 0	shift single register; 1	shift even-odd register pair
Bit 15: 0	shift in 0's; 1	shift in 1's

12. R1 and R3 contain 32-bit masks. For $_m$ = bit positions 0—31, c(R1+1) takes part in the comparison only if c(R1) $_m$ = 1, and c(R3+1) $_m$ replaces c(S2) $_m$ only if c(R3) $_m$=1.

13. The 4 bit mask contained in M3 determines which bytes of R1 take part in the operation. For n = mask bits 0 to 3, $c(R1)_{8n}$ — $_{(8n+7)}$ takes part if M3 $_n$ = 1 but is masked out if M3 $_n$ = 0. Main storage bytes are contiguous.

14. The operand length minus 1 is given by bits 8—15 of the instruction.

15. Only the low-order 4 bits of each operand 2 byte are moved.

16. Only the high-order 4 bits of each operand 2 byte are moved.

17. Each byte of S1 is replaced by a byte addressed by S2 so that S1 ← $c(S2 + c(S1))_{0-7}$.

18. The instruction scans S1 until it finds a nonzero byte or until it has scanned all of S1.

19. Operand 2, which must be in packed format, is unpacked and edited under control of operand 1, the pattern, whose length is given in bits 8—15 of the instruction. See 2.1.3 for edit instruction settings.

20. Branch to PSW + D4 only if $c(M3)_{CC} = 1$; M3 is bits 16—19 of the instruction.

21. The low-order 4 bits of c(S1) are left unchanged and 0's are shifted in. The direction of the shift is determined by S2; the high-order bit of the 6-bit shift length in S2 is set to 0 for a left shift, or to 1 for a right shift.

22. The operand 1 length minus 1 is given by bits 8—11 of the instruction, the operand 2 length minus 1 given by bits 12—15.

23. The S2 bytes are shifted left one half byte when placed in S1, thus leaving the rightmost half byte of S1 unchanged.

24. The remainder occupies the rightmost bytes of the operand 1 result and is equal in length to the S2 divisor. The quotient occupies the rest of operand 1.

25. This privileged instruction has possible condition code settings that are not described in this summary due to their complexity. Refer to the assembler user guide, UP-8913 (current version), for further information.

2.1.2.2. **Instructions by Instruction Name**

Instruction Name	Machine Code	Mnemonic
Add	1A	AR
Add	5A	A
Add decimal	FA	AP
Add half word	4A	AH
Add immediate	9A	AI
Add logical	1E	ALR
Add logical	5E	AL
Add normalized, long	2A	ADR

Add normalized, long	6A	AD
Add normalized, short	3A	AER
Add normalized, short	7A	AE
Add unnormalized, long	2E	AWR
Add unnormalized, long	6E	AW
Add unnormalized, short	3E	AUR
Add unnormalized, short	7E	AU
AND	14	NR
AND	54	N
AND	94	NI
AND	D4	NC

Instructions by Instruction Name (cont)

Instruction Name	Machine Code	Mnemonic
Branch and link	05	BALR
Branch and link	45	BAL
Branch on condition	07	BCR
Branch on condition	47	BC
Branch on count	06	BCTR
Branch on count	46	BCT
Branch on index high	86	BXH
Branch on index low or equal	87	BXLE
Clear channel—privileged	9F02	CLRCH

Clear device—privileged	9DX2	CLRDV
Compare	19	CR
Compare	59	C
Compare and swap under mask	B9	CSM
Compare decimal	F9	CP
Compare half word	49	CH
Compare logical	15	CLR
Compare logical	55	CL
Compare logical	95	CLI
Compare logical	D5	CLC
Compare logical characters under mask	BD	CLM

Instructions by Instruction Name (cont)

Instruction Name	Machine Code	Mnemonic
Compare logical immediate and skip	E1	CLIS
Compare logical characters long	0F	CLCL
Compare long	29	CDR
Compare long	69	CD
Compare, short	39	CER
Compare, short	79	CE
Convert to binary	4F	CVB
Convert to decimal	4E	CVD

Divide	1D	DR
Divide	5D	D
Divide decimal	FD	DP
Divide, long	2D	DDR
Divide, long	6D	DD
Divide, short	3D	DER
Divide, short	7D	DE
Edit	DE	ED
Edit and mark	DF	EDMK
Enqueue I/O — privileged	E0	EIO

Instructions by Instruction Name (cont)

Instruction Name	Machine Code	Mnemonic
Exclusive OR	17	XR
Exclusive OR	57	X
Exclusive OR	97	XI
Exclusive OR	D7	XC
Execute	44	EX
Execute diagnose — privileged	8300	EXD
GET IORB — privileged	0B	GRB
Halt and proceed — privileged	99	HPR
Halt device — privileged	9E01	HDV
Halve, long	24	HDR

Halve, short	34	HER
Initial program load — privileged	8303	IPL
Insert character	43	IC
Insert characters under mask	BF	ICM
Insert storage key — privileged	09	ISK*
Load	18	LR
Load	58	L
Load address	41	LA
Load and test	12	LTR
Load and test, long	22	LTDR
Load and test, short	32	LTER
Load channel register — privileged	9F03	LCHR

Instructions by Instruction Name (cont)

Instruction Name	Machine Code	Mnemonic
Load complement	13	LCR
Load complement, long	23	LCDR
Load complement, short	33	LCER
Load control — privileged	B7	LCTL
Load directive address — privileged	51	LDA
Load half word	48	LH
Load I/O address — privileged	61	LIA
Load, long	28	LDR
Load, long	68	LD

Load multiple	98	LM
Load negative	11	LNR
Load negative, long	21	LNDR
Load negative, short	31	LNER
Load positive	10	LPR
Load positive, long	20	LPDR
Load positive, short	30	LPER
Load PSW — privileged	82	LPSW
Load relocation register — privileged	A3	LRR
Load, short	38	LER
Load, short	78	LE

Instructions by Instruction Name (cont)

Instruction Name	Machine Code	Mnemonic
Longitudinal redundancy check — privileged	830E	LRC
Move	92	MVI
Move	D2	MVC
Move I/O — privileged	81	MIO
Move characters long	0E	MVCL
Move numerics	D1	MVN
Move with offset	F1	MVO
Move zones	D3	MVZ

Multiply	1C	MR
Multiply	5C	M
Multiply decimal	FC	MP
Multiply half word	4C	MH
Multiply, long	2C	MDR
Multiply, long	6C	MD
Multiply, short	3C	MER
Multiply, short	7C	ME
OR	16	OR
OR	56	O
OR	96	OI

Instructions by Instruction Name (cont)

Instruction Name	Machine Code	Mnemonic
OR	D6	OC
Pack	F2	PACK
Put IORB — Privileged	0C	PRB
Reset — privileged	8301	RESET
Service timer register — privileged	03	STR
Set program mask	04	SPM
Set storage key — privileged	08	SSK*
Set system mask — privileged	80	SSM
Shift and round decimal	F0	SRP
Shift left double	8F	SLDA

Shift left double logical	8D	SLDL
Shift left single	8B	SLA
Shift left single logical	89	SLL
Shift logical	9B	SHL
Shift right double	8E	SRDA
Shift right double logical	8C	SRDL
Shift right single	8A	SRA
Shift right single logical	88	SRL
Start device — privileged	9C02	SDV
Store	50	ST

Instructions by Instruction Name (cont)

Instruction Name	Machine Code	Mnemonic
Store character	42	STC
Store characters under mask	BE	STCM
Store control — privileged	B6	STCTL
Store half word	40	STH
Store, long	60	STD
Store multiple	90	STM
Store relocation register — privileged	A2	STRR
Store, short	70	STE
Store status — privileged	8302	STS

Instructions by Instruction Name (cont)

Subtract	1B	SR
Subtract	5B	S
Subtract decimal	FB	SP
Subtract half word	4B	SH
Subtract logical	1F	SLR
Subtract logical	5F	SL
Subtract normalized, long	2B	SDR
Subtract normalized, long	6B	SD
Subtract normalized, short	3B	SER
Subtract normalized, short	7B	SE
Subtract unnormalized, long	2F	SWR

2.1.2.2. **Instructions by Instruction Name (cont)**

Instruction Name	Machine Code	Mnemonic
Subtract unnormalized, long	6F	SW
Subtract unnormalized, short	3F	SUR
Subtract unnormalized, short	7F	SU
Supervisor call	0A	SVC
Supervisor load multiple — privileged	B8	SLM
Supervisor store multiple — privileged	B0	SSTM
Switch list scan — privileged	830F	SWLS
Test and set	93	TS
Test under mask	91	TM
Test under mask and skip	E2	TMS

Translate	DC	TR
Translate and test	DD	TRT
Unpack	F3	UNPK
Zero and add	F8	ZAP

*Added as a feature.

Edit Instruction Settings

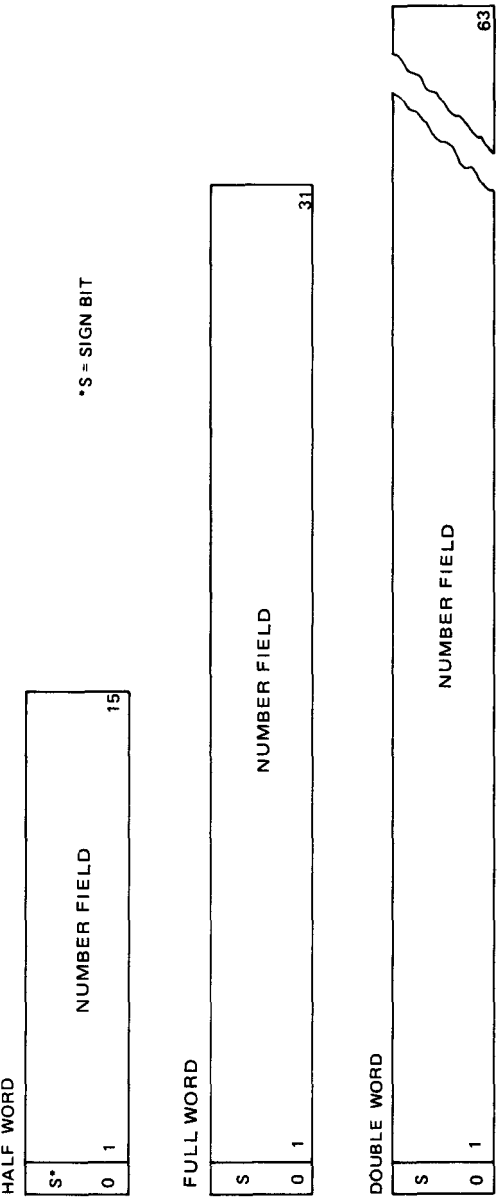
Mask (Operand 1) Character	EBCDIC/ASCII	S Switch Status	Data (Operand 2) Character	Resulting (Operand 1) Character	Resulting S Switch Status
Fill character	Any	Off	Not examined	Remains same	Off
Digit select byte	20	On	Nonzero	Digit	On*
		On	Zero	Digit	On*
		Off	Nonzero	Digit	On*
		Off	Zero	Fill character	Off
Significance start byte	21	On	Nonzero	Digit	On*
		On	Zero	Digit	On*
		Off	Nonzero	Digit	On*
		Off	Zero	Fill character	On*

Mark (Operand 1) Character	EBCDIC/ASCII	S Switch Status	Data (Operand 2) Character	Resulting (Operand 1) Character	Resulting S Switch Status
Message character	Any except 20, 21 22	On	Not examined	Message character	On*
		Off	Not examined	Fill character	Off*
Field separator byte	22	On	Not examined	Fill character	Off
		Off	Not examined	Fill character	Off

*Sign detection (examined simultaneously with operand 2 digit) affects the S switch as follows:

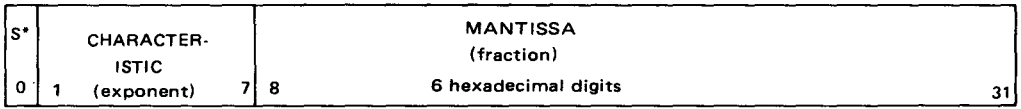
A plus or minus sign detected as most significant digit causes data exception.
A plus sign detected as a least significant digit causes S switch to be turned off.
A minus sign has no effect on the S switch.

Fixed-Point Numbers

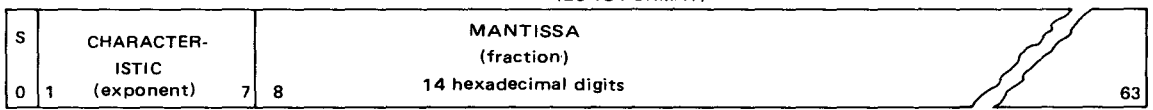


Floating-Point Numbers

FULL WORD (SHORT FORMAT)



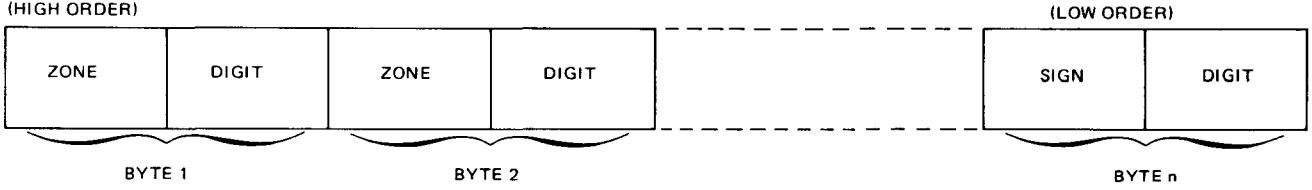
DOUBLE WORD (LONG FORMAT)



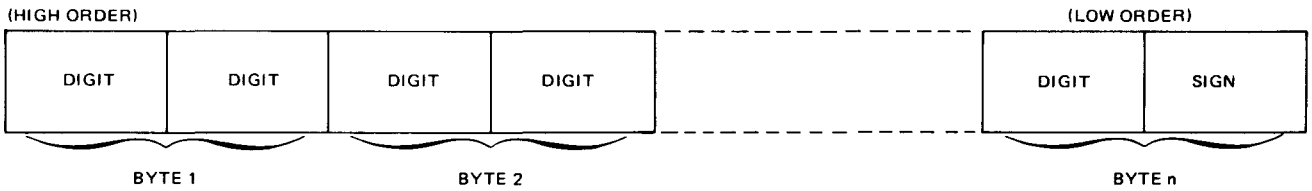
*S = SIGN BIT

Decimal Numbers

UNPACKED NUMBERS

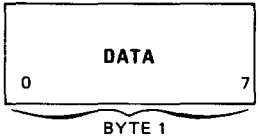


PACKED NUMBERS

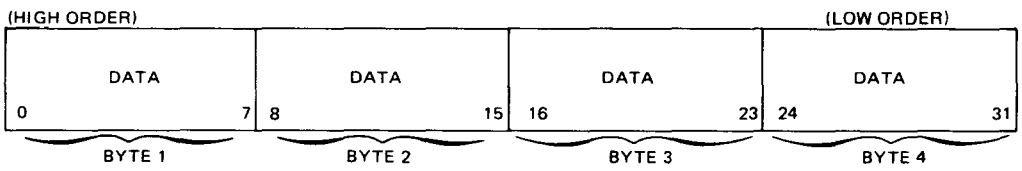


Logical Information

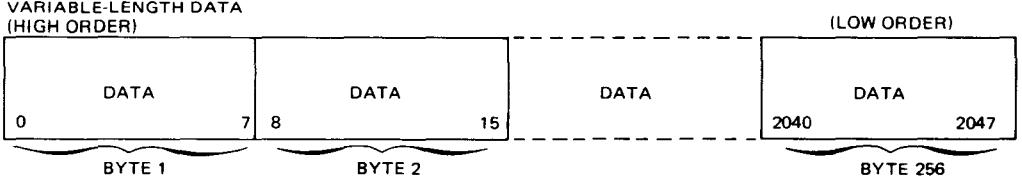
FIXED-LENGTH DATA



FULL WORD

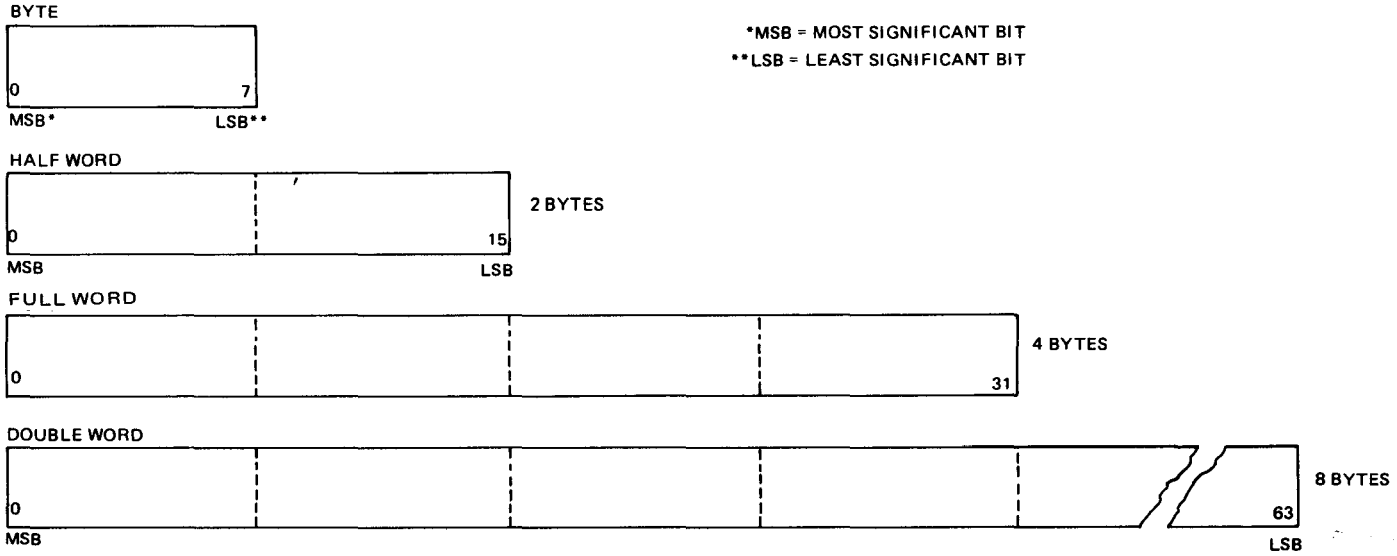


VARIABLE-LENGTH DATA



2.2.2. Data Boundary Alignments

Data Boundary Alignments



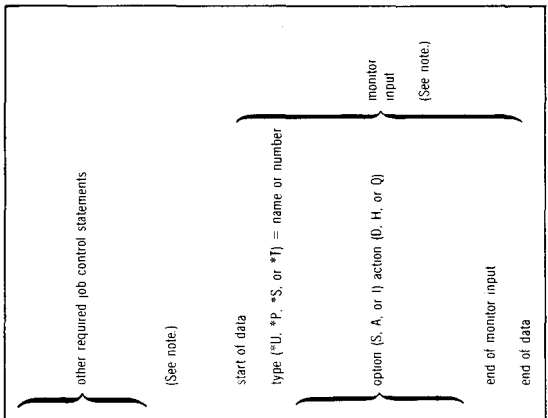
To align data or instructions on a double-word, full-word, or half-word main storage boundaries, use the following directive formats:

```
LABEL     OPERATION     OPERAND                    COMMENTS
1         10            16                         72                80
          CNOP          0,4    0 BYTE OFFSET FROM FULL-WORD BOUNDARY
          CNOP          2,4    2 BYTE OFFSET FROM FULL-WORD BOUNDARY
          CNOP          0,8    0 BYTE OFFSET FROM DOUBLE-WORD BOUNDARY
          CNOP          2,8    2 BYTE OFFSET FROM DOUBLE-WORD BOUNDARY
          CNOP          4,8    4 BYTE OFFSET FROM DOUBLE-WORD BOUNDARY
          CNOP          6,8    6 BYTE OFFSET FROM DOUBLE-WORD BOUNDARY
```

3.1. MONITOR AND TRACE

3.1.1. Control Stream Format for a Job To Be Monitored from the Start of the Program

Control Stream Format for a Job to be Monitored from the Start of the Program



Control Stream Format for a Job to be Monitored from the Start of the Program (cont)

Control Stream Format for a Job to be Monitored from the Start of the Program (cont)

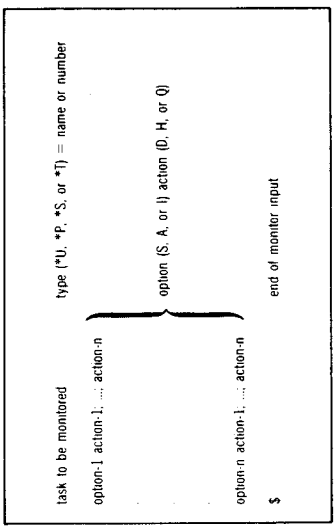
```
// PARAM...        (PARAM cards, if any)
/$                 start of data
                   }
                   } user program data cards
/*                 end of data
/&                 end of job input
// FIN             end of card input
```

NOTE:

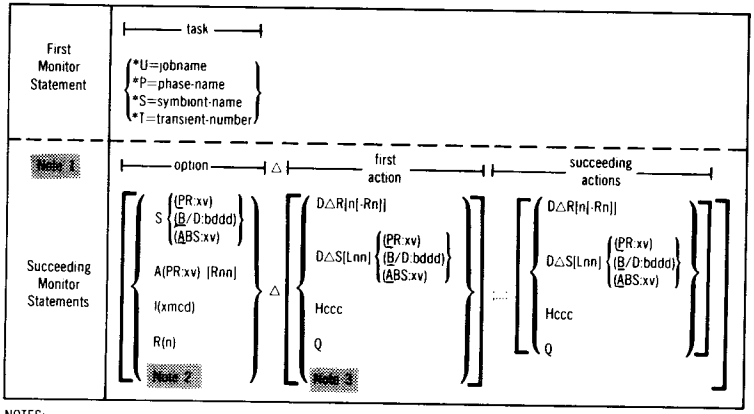
The TRACE entry is required if monitor input is entered via the job control stream.

3.1.2. Monitor Input Format for Input by the Operator After Program Execution Has Begun

Monitor Input Format for Input by the Operator After Program Execution has Begun



Statement Formats for Monitor Input



NOTES:

1. The first action is separated from the option by a blank space, and any succeeding actions are separated from the previous action by a semicolon.
2. If no option is specified, the monitor routine assumes a default option (each instruction is interrupted) and default display. (See 3.1.4.)
3. If no action is specified, the monitor routine produces a default display.

3.1.4. Summary of Actions and Program Information Printed

Summary of Actions and Program Information Printed

Program Information Printed	Action				
	Display Register (D R)	Display Storage (D S)	Default Display	Halt (H)	Quit (Q)
Job name*	x	x	x	x	x
TCB address*	x	x	x	x	x
Program base address*	x	x	x	x	x
PSW contents	x	x	x	x	x
Next instruction to execute	x	x	x	x	x
Option causing this printout	x	x	x	x	x
Contents of specified registers	x				

Summary of Actions and Program Information Printed (cont)

Program Information Printed	Action				
	Display Register (D R)	Display Storage (D S)	Default Display	Halt (H)	Quit (Q)
Contents of specified storage		x			
Contents of changed registers			x		
Contents of referenced storage			x		
HALT message				x	

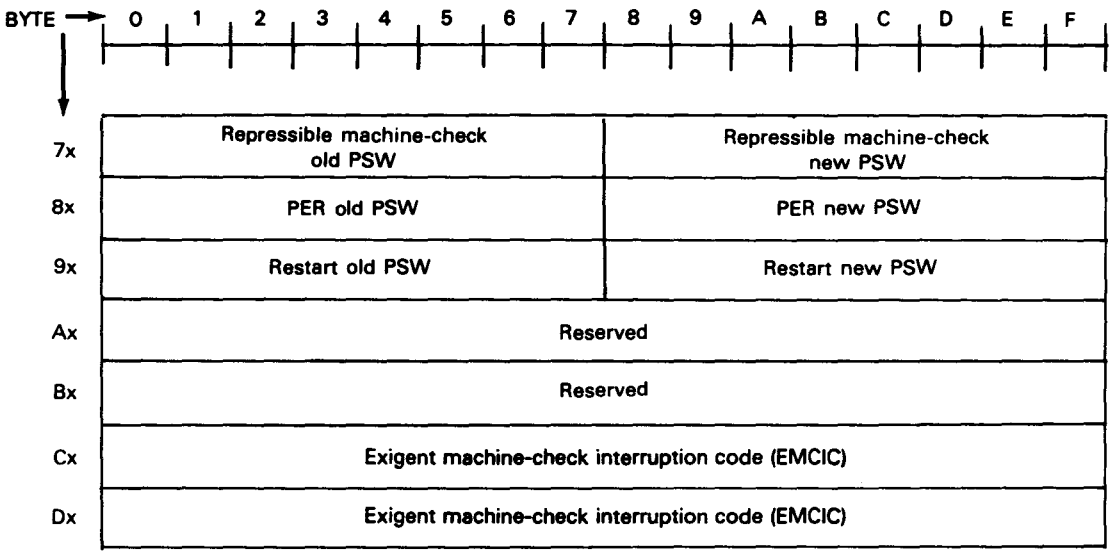
*These items are included only for the first option that causes a printout.

Low-Order Main Storage Layout

BYTE →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x	Software defined												IPL device address		Software defined	
1x	CXPW				monitor class		monitor code		Reserved							
2x	I/O old PSW								I/O new PSW							
3x	Exigent machine-check old PSW								Exigent machine-check new PSW							
4x	Program old PSW								Program new PSW							
5x	Supervisor-call old PSW								Supervisor-call new PSW							
6x	External old PSW								External new PSW							

LOW-ORDER MAIN STORAGE LAYOUT (cont)

Low-Order Main Storage Layout (cont)



Ex	Registers for PER		
Fx	PER interruption register save area	Exigent machine-check save area	Repressible machine—check save area

LEGEND:

CXPW	Channel index pointer word
PER	Program event recording
PSW	Program status word

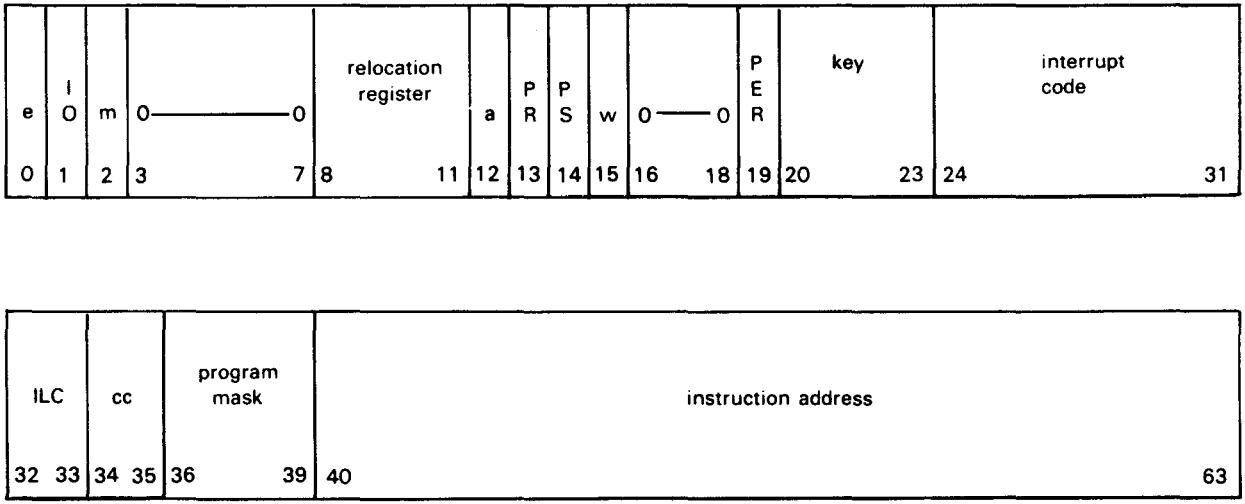
Program Status Word (PSW) Format

NEW PSW

e	I O	m	0 —— 0	relocation register	a	P R	P S	w	0 —— 0	P E R	key	r1	r2
0	1	2	3 7	8 11	12	13	14	15	16 18	19	20 23	24 27	28 31

ILC 0 — 0	cc	program mask	instruction address
32 33	34 35	36 39	40 63

OLD PSW


e
I O
m
0——0
relocation register
a
P R
P S
w
0——0
P E R
key
interrupt code
0 1 2 3 7 8 11 12 13 14 15 16 18 19 20 23 24 31
ILC
cc
program mask
instruction address
32 33 34 35 36 39 40 63

Program Status Word (PSW) Field Interpretation

Bits*	Field Name	Description
0	External mask (e)	Controls whether the CPU is enabled for interruption by an external interruption request. When the bit is 1, interruptions are permitted.
1	I/O mask (IO)	Controls whether the CPU is enabled for I/O interruptions. When the bit is 1, interruptions are permitted.
2	Repressible machine check mask (m)	Controls whether the CPU is enabled for repressible machine check interruptions. When this bit is 1, interruptions are permitted.
3—7	Reserved	Must be zero. The CPU will force these bits to zero when loaded regardless of their state in the new PSW. Stored as zeros in the old PSW.
8—11	Relocation register	The processor relocation key selects 1 of 16 keys and relocation registers which apply to all program-visible CPU references while this PSW is used as the current PSW.

12	ASCII mode (a)	The CPU operates in either ASCII or EBCDIC mode as specified by this bit: a = 1 ASCII mode a = 0 EBCDIC mode Certain CPU instructions interpret or generate code-sensitive characters in either ASCII or EBCDIC. The unpack, edit, and edit-and-mark instructions generate code-sensitive zones as follows: ASCII zone = 3_{16} EBCDIC zone = F_{16} The edit instructions detect the following code-sensitive control characters:

	ASCII	EBCDIC
Digit select	80_{16}	20_{16}
Significant start	81_{16}	21_{16}
Field separator	82_{16}	22_{16}

Program Status Word (PSW) Field Interpretation (cont)

Bits*	Field Name	Description
13	Problem register mode (PR)	The CPU provides 2 sets of 16 general registers: 1. Problem general registers 2. Supervisor general registers This bit selects which set is used in executing an instruction as follows: 1 = problem general registers 0 = supervisor general registers
14	Problem state (PS)	The CPU may operate in one of two states as selected by this bit: 1 = problem mode 0 = supervisor mode When operating in supervisor mode, all implemented instructions may be executed; however when operating in problem mode, only nonprivileged instructions may be executed and attempts to execute privileged instructions will result in a program interruption.

15	Wait state (w)	When 1, the CPU is in the wait state. When zero, the CPU is in the running state.
16—18	Reserved	Must be zero. The CPU will force these bits to zero when loaded regardless of their state in the new PSW. Stored as zeros in the old PSW.
19	Program event recording (PER)	When this bit is 1, a PER interruption is enabled.
20—23	Key	When set to 0, no PER interruption is allowed. Refer to bits 8—11.
24—27 (new PSW)	Service routine register (r1)	Specifies a general register pair for passing the address of the I/O service routine when a clear-channel instruction is executed or when an I/O interruption occurs; specifies the PER argument passing registers for a PER interruption.
24—31 (old PSW)	Interruption code	When the old PSW is stored on a program, external, I/O, machine check, and supervisor-call interruption, this field identifies the cause of the interruption. For other interruptions, zeros are stored in this field in the old PSW. See condition code settings 2.1.2.1 for exception codes contained in bits 24—31.

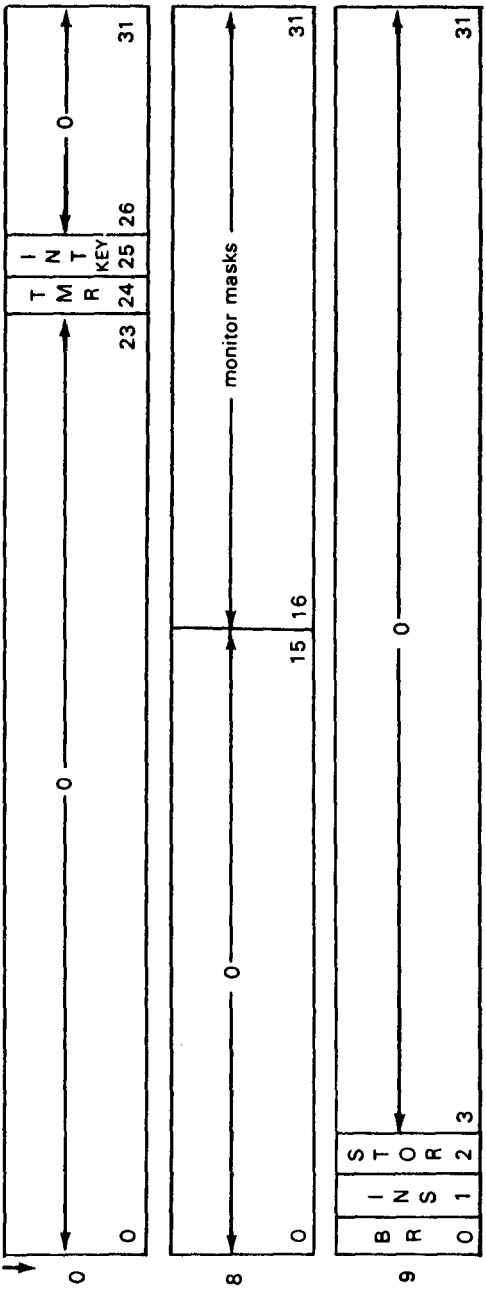
Program Status Word (PSW) Field Interpretation (cont)

Bits*	Field Name	Description
28—31 (new PSW)	Register select (r2)	Specifies a general register pair for argument passing when an I/O interruption occurs or when a clear-channel instruction is executed.
32—33 (new PSW)	Instruction length code (ILC)	This field is forced to zero by CPU when a new PSW is introduced.
32—33 (old PSW)	Instruction length code (ILC)	The code in this field indicates the length of the last interpreted instruction when a program or supervisor-call interruption occurs or when a branch-and-link instruction is executed.
34—35 (new PSW)	Condition code (cc)	This field is the two bits of condition code that is loaded as part of the new PSW.
34—35 (old PSW)	Condition code (cc)	This field, two bits of condition code, is updated by execution of many instructions to reflect the result of the operation.
36—39	Program mask	This field provides the four program mask bits, each of which is associated with a program exception as follows:

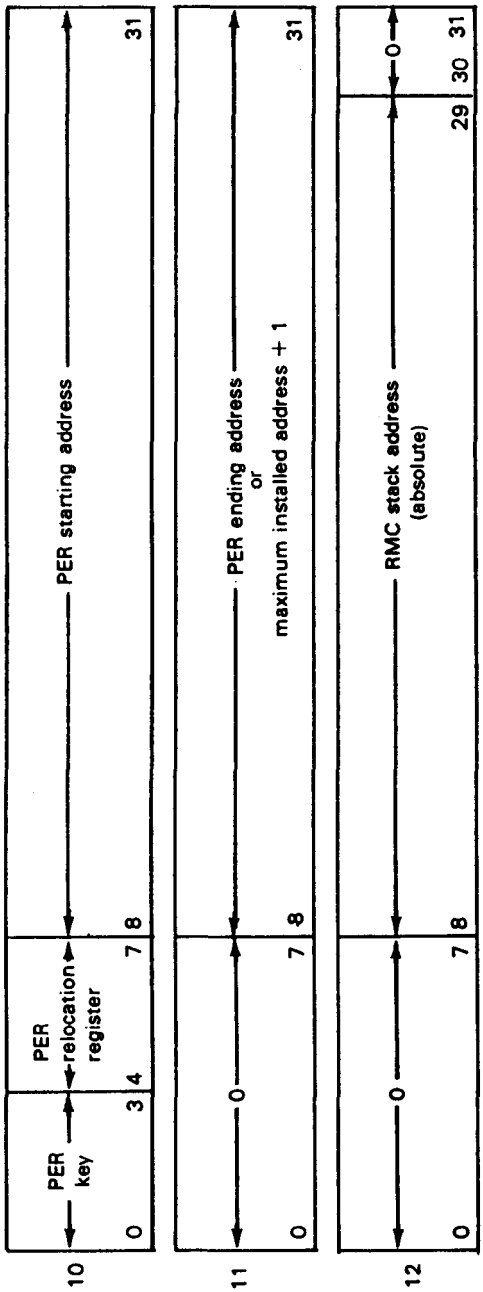
		Program Mask Bit / Program Exception 36 Fixed-point overflow 37 Decimal overflow 38 Exponent underflow 39 Significance When the mask bit is 1, the exception results in an interruption. When the mask bit is zero, no interruption occurs. The significance-mask bit also determines the manner in which floating-point addition and subtraction are completed. NOTE: The floating-point instruction set is a feature; bits 38 and 39 have no effect when the feature is not installed.
40—63	Instruction Address	These 24 bits form the instruction address (logical address). This address designates the location of the leftmost byte of the next instruction.

*Bits specified are for the old PSW and new PSW unless otherwise indicated.

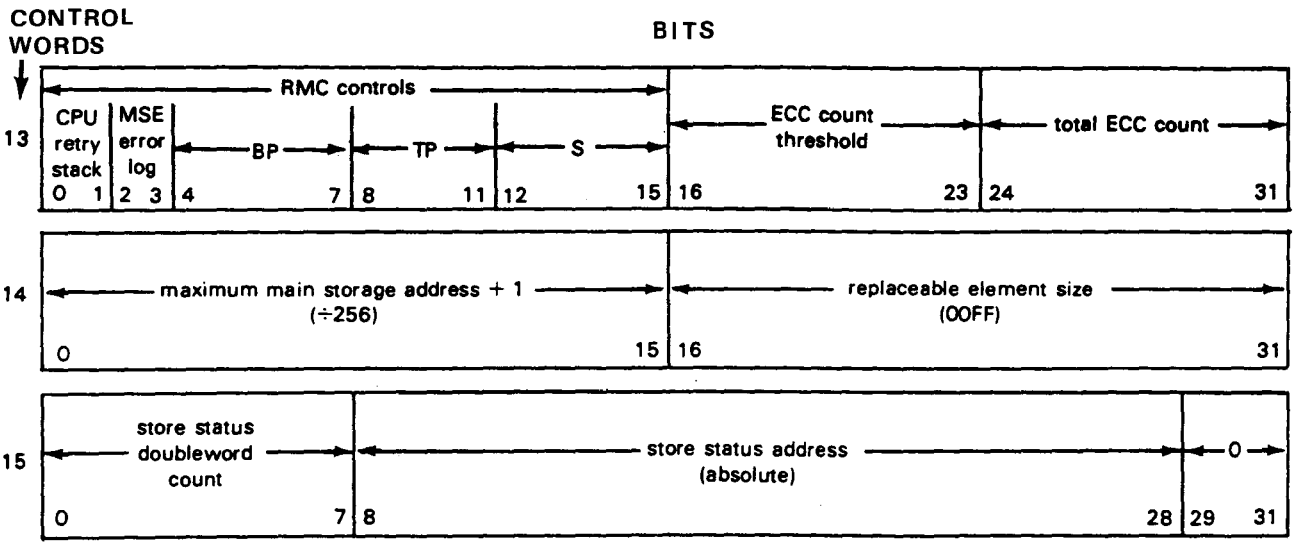
3.4. CONTROL REGISTER FORMAT



Control Register Format


10
PER key
PER relocation register
PER starting address
0
3
4
7
8
31
11
0
PER ending address or maximum installed address + 1
0
7
8
31
12
0
RMC stack address (absolute)
0
7
8
29
30
31

Control Register Format (cont)



LEGEND:

BP	Bottom pointer	MSE	Main storage error	STOR	Storage
BR	Branch	PER	Program event record	TMR	Timer
ECC	Error correction code	RMC	Repressible machine check	TP	Top pointer
INS	Instruction	S	Storage (instruction format)		
INT	Interrupt key				

Control Register Field Assignments

Word	Bits	Field Name	Association	Initial Value
0	0—23	Not used (all zeros)	—	—
	24	Interval timer mask	Interval timer	0
	25	Interrupt key mask	Interrupt key	1
	26—31	Not used (all zeros)	—	—
8	0—15	Not used (all zeros)	—	—
	16—31	Monitor masks	Monitoring	0
9	0	Successful branch event mask	PER	0
	1	Instruction fetch event mask	PER	0
	2	Storage alteration event mask	PER	0
	3—31	Not used (zero)	—	0

10	0—3	PER key	PER	0
	4—7	PER relocation register	PER	0
	8—31	PER starting address	PER	0
11	0—7	Not used (zero)	—	0
	8—31	PER ending address	PER	Maximum installed address+1
12	0—7	Not used (zero)	—	0
	8—29	Repressible machine check absolute address (word boundary)	RMC and ECC logging	0
	30—36	Not used (zero)	—	—

Control Register Field Assignments (cont)

Word	Bits	Field Name	Association	Initial Value
13	0—15	RMC stack controls	RMC and ECC logging	0
	16—23	ECC threshold count	ECC logging	0
	24—31	Total ECC count	ECC logging	0
14	0—15	Maximum main storage address + 1 ÷ 256	ECC logging	Correction 11 ÷ 256
	16—31	Replaceable Element size	ECC logging	$00FF_{16}$
15	0—7	Store status double-word count	Store status and exigent MC	00_{16}
	8—28	Store status absolute address (doubleword boundary)	Store status and exigent MC	0
	28—31	Not used (zero)	—	0

Obtaining a System Dump (SYSDUMP)

You get a system dump with two steps:

1. Main storage write to the YDUMP file
2. SYSDUMP listing from the YDUMP file

In this situation:	You call the main storage write step with:	What happens next:
To get a SYSDUMP with the console workstation	SYSDUMP command	Job SYSDMPxx. This job is automatically scheduled to print SYSDUMP listing.
To get a SYSDUMP within a job	// OPTION SYSDUMP job control statement	This job runs module SYSDMP. It allows the system to run under your job but does no scheduling.

When a system error occurs, the main storage write step (SE 15 message displayed) is called automatically, followed by SYSDMPxx (where xx is the SYSDMP number).

Obtaining a System Dump after an HPR (SYSDUMPO)

To get a system dump after an HPR:

- For Models 3 through 6:
  Perform an IPL on the system according to directions in the operations handbook, taking care not to press FUNCTION and RESTART keys.
- For Model 8:
  Press ESCAPE key on console; then press M. Select L in menu and transmit. Press U and transmit. Do an IPL on the system.

IPL automatically schedules SYSDMPxx and run statement RV SYSDUMPO. At this point, you may enter the following parameters:

```
[,,DO=(ALL     )[,V=(VSN     )][,P=did]]
      (DUMP    )    ((VSN,A))
      (TRANSLATED)
      (JOBS    )
      (SAVE    )
      (RESTORE )
      (NONE    )
```

NOTES:

1. The options and suboptions of the DO= parameter allow for a more specific dump. For a more detailed description of the run statement, see the DUMP ANALYSIS user guide/programmer reference, UP-9980 (current version).
2. If the command is entered without a DO= parameter entry, the following message is displayed:

   SDØ1 DUMP OPTION(ALL,NONE,DUMP,TRANSLATED,JOBS,RESTORE,SAVE)

   An option can be entered at this time, or, by leaving it blank, a default of ALL is assumed and a complete system dump is produced.

Obtaining a Job Dump or EOJ Dump

Job Dump:

```
// OPTION JOBDUMP
```

or

```
// OPTION ABRDUMP (abbreviated JOBDUMP)
```

EOJ Dump:

```
// OPTION DUMP
```

Summary of System Debugging Aids

Function	Use	Console Command	Results
Pseudo monitor*	To identify the routine changing a particular byte	SET HA,PM,address [,job-name]	HPR code 99130202 (Press START to continue.)
Resident monitor*	To identify the instruction changing a particular byte	SET HA,RM,address [,job-name]	HPR code 99130404 (Press START to continue.)
Verify bytes 0—B*	To identify the routine destroying low-order storage	Included in supervisor debug option	HPR code 99130303 (Press RUN to continue.)
History tables*	To provide some recent history in SYSDUMPs	Included in supervisor debug option	Continuous updating of resident tables
Halt on transient load	To halt if and when a particular transient is loaded	SET HA,TL,hex-id	HPR code 990C0C (Press START to continue.)
Halt on transient call*	To halt if and when a particular transient is called	SET HA,TC,hex-id	HPR code 990C0D (Press START to continue.)
Halt on transient exit*	To halt if and when a particular transient is exited	SET HA,TE,hex-id	HPR code 990C0E (Press START to continue.)

Halt on shared code call*	To halt if and when certain (or all) shared code modules are called	SE HA,SC[,{module-name / prefix.}]	HPR code 991D01 (Press START to continue.)
Halt on shared code return*	To halt if and when certain (or all) shared code modules return	SE HA,SR[,{module-name / prefix.}]	HPR code 991D02 (Press START to continue.)
Halt on shared code return with error*	To halt if and when certain (or all) shared code modules return with error	SE HA,SE[,{module-name / prefix.}]	HPR code 991D03 (Press START to continue.)
Pause on shared code call*	To pause a task if and when certain (or all) shared code modules are called	SE PA,SC[,{module-name / prefix.}]	SE25 console message (Enter 'C' to continue.)
Pause on shared code return*	To pause a task if and when certain (or all) shared code modules return	SE PA,SR[,{module-name / prefix.}]	SE25 console message (Enter 'C' to continue.)
Pause on shared code return with error*	To pause a task if and when certain (or all) shared code modules return with error	SE PA,SE[,{module-name / prefix.}]	SE25 console message (Enter 'C' to continue.)

Summary of System Debugging Aids (cont)

Function	Use	Console Command	Results
Halt on symbiont load	To halt if and when a particular symbiont (or symbiont phase) is loaded	SET HA.SY,idnn	HPR code 997C (Press START to continue.)
PIOCS debug option	To identify checksum errors or internal PIOCS problems	SET DE.IO	HPR code 990F
Transient debug option	To halt on transient errors (100—1FF)	SET DE.TR	HPR code 99080800
Loader debug option	To halt on loader errors (52—5F)	SET DE.LD	HPR code 991500 (Press RUN to continue.)
Shared code debug option	To halt on error during execution of shared code	SET DE.SC	HPR code 990809 (Press RESTART to take a SYSDUMP and continue.) HPR 99130A when dynamic buffer pool links are destroyed.
Dynamic buffer debug option*	To halt on dynamic buffer overflow	SET DE.DB	HPR code 99130D

Screen format coordinator input/output debug option	To take a snapshot dump of all input and output buffer blocks when using the screen format coordinator	SET DE,INO	Writes snapshot dump to job log
Screen format coordinator format/input/output debug option	To take a snapshot dump of the format block; the input buffer (on input operations); the output buffer (on output operations) blocks; and, if errors occur, the screen format coordinator blocks	SET DE,FS	Writes snapshot dump to job log or system printer

*Supervisor debug option required at IPL

Summary of System Debugging Aids (cont)

Function	Use	Console Command	Results
Screen format coordinator input/output debug option	To take diagnostic snapshot if screen format coordinator error occurs	SE DE,SF	Causes snapshot to be taken
Reset pause option	To reset all SE PA commands	SE PA,OFF	None
Reset halts	To reset all SE HA commands	SE HA,OFF	None
Reset debug option	To reset all SE DE commands	SE DE,OFF	None

4.1. I/O CHANNEL NUMBER ASSIGNMENT

I/O Channel Number Assignment

Channel 1 =	Direct memory access channel (DMA)
Channel 2 =	Multiple line communications multiplexor channel (MLCM)
Channel 3 =	Shared direct memory access channel (SMDA)

4.2. DEVICE ADDRESSES FOR SYSTEM 80 DEVICES

Device Addresses

Device Type	Device Address
System 80 console workstation	310①
Any System 80 workstation	311—318
Any additional System 80 workstation	341—343, 351—353
Any 8420/8422 diskette	320—323①
Any additional 8420/8422 diskette	341—343, 351—353
Any 8417/8419 disk	100—107①
0789/0776 printer	330①
Additional 0789/0776 printer	331, 340—341
Any 0789/0798 remote printer	340, 350
0719 card reader	332

DEVICE ADDRESSES FOR SYSTEM 80 DEVICES (cont)

Additional 0719 card reader	333, 342—343
0608 card punch	333
Additional 0608 card punch	343
Any UNISERVO 10 magnetic tape	370—371②
SLCA 0	280—282
SLCA 1	290—292
SLCA 2	2A0—2A2
SLCA 3	2B0—2B2
SLCA 4	2C0—2C2
SLCA 5	2D0—2D2
SLCA 6	2E0—2E2
SLCA 7	2F0—2F2

① These device addresses must be configured with the associated device type. All other device addresses are suggestions. Any address within the proper channel can be used. For further information on using device addresses, refer to the system installation user guide/programmer reference, UP-8839 (current version).

② Default device address

4.3. COMMAND CODES FOR SYSTEM 80 DEVICES

4.3.1. Command Codes for 8417/8419 Disk

Device	Command	Operation Code
8417/8419 disk	Seek	07
	Recalibrate	17
	Format write	01
	Write data	05
	Search/read equal	22
	Search/read high or equal	32
	Read ID	0E
	Read data	02
	Diagnostic	12

	Sense	04
	Reset unsafe	33

4.3.2. Command Codes for Single Line Communications Adapter (SLCA)

Device	Command	Operation Code
Single line communications adapter (SLCA)	NO-OP	03
	Sense	04
	Load memory address	0D
	Load RAM	05
	Read memory	06

4.3.3. Command Codes for System 80 Workstation/Console Workstation

Device	Command	Operation Code
System 80 workstation/ console workstation	System message write	01
	Diagnostic write	81
	Command write	21
	User write	09
	System message read	02
	Diagnostic read	82
	Command read	22
	User read	0A
	No-op	03

	Enter work area mode	23
	Enter system response mode	43
	Sense	04
	Workstation reset	0B
	Read event	32
	Message waiting	07
	Load RAM	05

4.3.4. Command Codes for 8420/8422 Diskette

Device	Command	Operation Code
8420/8422 diskette	Sense	04
	Feed	23
	Format write	11
	Load track/side/sector	31
	Data set open	21
	Data set close	51
	Read	06
	Write	01
	Write control	41
	Diagnostic read subsystem area	66

COMMAND CODES FOR SYSTEM 80 DEVICES (cont)

	Diagnostic read subsystem buffer	76
	Read volume ID	56
	Diagnostic write enable	63
	Read control	46
	Diagnostic write subsystem buffer	71
	Recover	13
	Initial load	02
	Unload	33
	Nooperation	03
	Format read	16
	Load physical track	61

4.3.5. Command Codes for 0776/0789 Printer

Device	Command	Operation Code
0776/0789 printer	Load vertical format buffer	43
	Print advance	X1, X9*
	Advance	X7, XF *
	Sense	04
	No-op	03

	Read vertical format buffer	12
	Unprintable character data check disable	73
	Unprintable character data check enable	7B
	Diagnostic write data buffer	75
	Diagnostic read data buffer	76
	Diagnostic write enable	63

*X equals the modifier VFB detail bits. For an explanation of these modifier bits see the I/O controllers programmer reference, UP—8742 (current version).

4.3.6. Command Codes for 0789/0798 Remote Printer

Device	Command	Operation Code
0789 remote printer	Load memory address	0D
	Read memory	16
	Load-RAM	05
	Load vertical format buffer	43
	Print advance	X1, X9*
	Advance	X7, XF*
	Sense	04
	No-op	03
	Read vertical format buffer	12

	Unprintable character data check disable	73
	Unprintable characters data check enable	7B
	Diagnostic write data buffer	75
	Diagnostic read data buffer	76
	Diagnostic write enable	63

*X equals the modifier VFB detail bits. For an explanation of these modifier bits see the I/O controllers programmer reference, UP—8742 (current version).

4.3.7. Command Codes for 0719 Card Reader

Device	Command	Operation Code
0719 card reader	Read translate mode	02
	Read image mode	06
	Sense	04
	No-op	03
	Diagnostic write data buffer	71
	Diagnostic read data buffer	76
	Diagnostic write enable	63

4.3.8. Command Codes for 0608 Card Punch

Device	Command	Operation Code
0608 card punch	Read translate mode	02
	Read image mode	06
	Punch translate mode	01
	Punch image mode	05
	Sense	04
	No-op	03
	Flush last card from wait station	23
	Diagnostic write data buffer	71
	Diagnostic read data buffer	76
	Diagnostic write enable	63

4.3.9. Command Codes for UNISERVO 10 Magnetic Tape Type 0871

Device	Command	Operation Code
UNISERVO 10 Magnetic Tape Type 0871	Write	01
	Sense	04
	Read	02 or 12
	Read backward	0C or 1C
	Rewind	07
	Rewind with interlock	0F
	Erase	17
	Write tape mark	1F
	Backspace block	27

	Backspace file	2F
	Forward space block	37
	Forward space file	3F
	No operation	03
	Request tie	1B
	Set low threshold	5B
	Set 1600 BPI	C3
	Set 800 BPI	CB
	Set monitor	8B
	Set simulate	4B
	Reset simulate	0B

4.4.1. Status Byte Format for 8417/8419 Disk

Bit	Condition Which Sets Bits	Meaning
0	Attention	Indicates an unsolicited interrupt took place in the controller. This bit can only be presented to the processor through the interrupt process after a load-channel-register has been received.
1	Status modifier	Indicates an error in an ID field has been recovered for a record other than the first of a series being processed.
2	—	Not used; always set to zero.
3	Busy	Indicates the I/O device is presently doing a seek operation or that the controller is attempting to present status.
4	Channel end	Presented when a data transfer or control transfer is completed and the controller has no more need of the channel and will not appear busy after presentation as a result of the command for which it is presented. It may or may not be presented with device end.
5	Device end	Presented when the device has finished executing a command. It may be presented when the controller has finished. It will be presented with channel end or delayed as a result of an overlapping seek command. This status is similar to attention (bit 0) except the interrupt is solicited and asynchronous.

6	Unit check	Indicates that an abnormal condition was detected by the controller. It is normally indicative of an error condition, although operations like no-record-found are not software errors, but construed as hardware errors.
7	Unit exception	Always set to zero for the DMA channel.

4.5.1. Status Byte Format for Single Line Communications Adapter (SLCA)

Bit	Condition Which Sets Bits	Meaning
0	Attention	Function is feature dependent. Usually set to zero.
1	Status modifier	Indicates successful error retry information is contained in sense bytes.
2	Control unit end	Indicates to the MLCM that the SLCA can accept another command for this port for a terminal other than the one which presented this control unit end status. (This bit is not seen by software).
3	Busy	Indicates that a command has addressed a device which is currently executing a command.
4	Channel end	Set along with device end.
5	Device end	Indicates that an outstanding command has completed for a given device. Device end is always accompanied by channel end.
6	Unit check	Indicates that the SLCA has encountered an error during the execution of a command or a command sequence and that one or more sense bits are set.
7	Unit exception	Function is feature dependent. Usually set to zero.

4.6.1. Status Byte Format for System 80 Workstation/Console Workstation

Bit	Condition Which Sets Bits	Meaning
0	Attention	Indicates any of the following occurred: ■ operator activated TRANSMIT key; ■ an implied transmit function (DC1 or ESC DC1) was contained in a write command; ■ operator activated any one of 23 function keys; ■ operator activated a mode change request from workstation mode to system mode or vice versa; ■ a RAM parity error occurred at the device; or ■ a power on condition occurred at the device.

Status Byte Format for System 80 Workstation/Console Workstation (cont)

Bit	Condition Which Sets Bits	Meaning
1	Status modifier	When set along with bit 0 (attention) indicates attention item merged with a successful error recovery. When set along with bit 4 (channel end) and bit 5 (device end), indicates the workstation controller (WSC) had to evoke an error recovery procedure in order to complete the outstanding command and the procedure was successful. When set along with bit 4 (channel end), bit 5 (device end), and bit 6 (unit check), indicates error recovery procedure evoked was unsuccessful.
2	—	Not used; always set to zero.
3	Busy	When set, indicates that a command has addressed a device that is currently executing a command.
4	Channel end	When set with bit 5 (device end), indicates WSC has successfully executed an outstanding command.
5	Device end	Indicates the termination of the execution of a command. It is always set along with bit 4 (channel end), or bits 4 (channel end) and 6 (unit check).

6	Unit check	When set, indicates the workstation controller (WSC) has encountered an error condition in response to or during a command sequence; that is, the command cannot be executed. When set along with bit 4 (channel end) and bit 5 (device end), indicates some condition exists that prevented a successful command completion at the device or workstation controller (WSC). Unit check implies that at least one bit in sense byte 0 is set to a 1.
7	—	Not used; always set to zero.

4.6.2. Status Byte Format for 8420/8422 Diskette

Bit	Condition Which Sets Bits	Meaning
0	Attention	Indicates that the device addressed is in the run state. When set with busy (bit 3), it indicates that a command was addressed to a diskette drive that is in the run state and is currently executing a command. When set with status modifier (bit 1) it indicates the device addressed is busy in the run state and has initiated a successful automatic retry.

Status Byte Format for 8420/8422 Diskette (cont)

Bit	Condition Which Sets Bits	Meaning
0	Attention (cont)	When set with status modifier (bit 1) and busy (bit 3) it indicates the device addressed is busy, is in the run state, and has completed a successful automatic retry.
1	Status modifier	Is never set by itself. See the meaning for the following bits: ■ Attention (bit 0); ■ Control unit end (bit 2); ■ Busy (bit 3); ■ Channel end (bit 4); and ■ Unit check (bit 6)
2	Control unit end	Indicates the diskette controller successfully completed a command chain and the controller presented control unit busy status to the channel during the execution of this command.

		When set with status modifier (bit 1), it indicates a successful automatic retry at the completion of a command chain and that the controller presented control unit busy status to the channel during the execution of this command.
3	Busy	Indicates a command has addressed a diskette drive that is currently executing a command. When set with status modifier (bit 1) it indicates that a command was sent to the diskette controller while currently executing a nonfeed command for any other diskette drive (control unit busy). When set with both the status modifier (bit 1) and control unit end (bit 2) it indicates a command was sent to the diskette controller while it was executing a nonfeed command for another diskette drive and when the diskette controller had completed a command chain and presented control unit busy status to the channel. When set with any of the folloing combinations it indicates that an addressed device was attempting to present status when addressed by the system. These combinations indicate the failure of the device handling software to wait for an interrupt: ■ Channel end (bit 4) and device end (bit 5); ■ Status modifier (bit 1), channel end (bit 4), and device end (bit 5);

Status Byte Format for 8420/8422 Diskette (cont)

Bit	Condition Which Sets Bits	Meaning
3	Busy (cont)	■ Channel end (bit 4), device end (bit 5), and unit exception (bit 7); ■ Status modifier (bit 1), channel end (bit 4), device end (bit 5), and unit exception (bit 7); ■ Channel end (bit 4), device end (bit 5), and unit check (bit 6); ■ Status modifier (bit 1), channel end (bit 4), device end (bit 5) and unit check (bit 6): ■ Channel end (bit 4), device end (bit 5), unit check (bit 6) and unit exception (bit 7); and ■ Status modifier (bit 1), channel end (bit 4), device end (bit 5), unit check (bit 6) and unit exception (bit 7).
4	Channel end	When set with device end (bit 5), it indicates that the diskette controller has sucessfully executed an outstanding command that was not preceded by a control unit busy status presentation or that it did not require any automatic retry.

		When set with status modifier (bit 1) and device end (bit 5), it indicates that the diskette controller has successfully completed a command that required an automatic retry. When set with device end (bit 5) and unit exception (bit 7) it indicates that the diskette has encountered the end of volume (EOV). When set with status modifier (bit 1), device end (bit 5), and unit exception (bit 7), it indicates the diskette has the EOV record during the execution of a read or write command and an automatic retry operation occurred. When set with device end (bit 5) and unit check (bit 6) it indicates that the diskette controller has accepted a command and has encountered an error condition during command execution. When set with status modifier (bit 1), device end (bit 5), and unit check (bit 6), it indicates that the diskette controller has accepted a command, an automatic retry operation occurred, and an error condition was encountered during command execution. When set with device end (bit 5), unit check (bit 6), and unit exception (bit 7), it indicates that the diskette controller has accepted a command, the EOV record was encountered, an automatic retry operation occurred, and an error condition was encountered during command execution.

Status Byte Format for 8420/8422 Diskette (cont)

Bit	Condition Which Sets Bits	Meaning
5	Device end	Is never set by itself. See the meaning for the following bits: ■ Busy (bit 3); and ■ Channel end (bit 4).
6	Unit check	Indicates that the diskette controller has encountered an error condition in response to or during a command sequence. (Command cannot be executed.) When set with status modifier (bit 1) it indicates the diskette encountered a nonrecoverable error in response to or during a command sequence and a successful automatic retry was initiated.
7	Unit exception	Is never set by itself. See the meaning for the following bits: ■ Busy (bit 3); and ■ Channel end (bit 4).

4.6.3. Status Byte Format for 0776/0789 Printer

Bit	Condition Which Sets Bits	Meaning
0	Attention	Specifies transition from stop state to run state.
1	Status modifier	Set along with channel-end/device-end whenever the paper peripheral controller (PPC) had to evoke at least one error recovery procedure in order to complete the outstanding command. When status-modifier bit is set without bit 6 (unit check) set, this implies that with error recovery, the command was completed successufully. Autosense follows.
2	—	Not used; always set to zero.
3	Busy	Indicates the device cannot execute the command because it is executing a previously issued command.
4	Channel end	Set concurrently with bit 5 (device end) by the PPC.
5	Device end	Specifies the completion of a command initiated by the channel and readiness to accept a new command.
6	Unit check	Specifies at least one bit is set in sense byte 0, 1, 2, 3, or 4. Autosense follows.
7	Unit exception	Presented with channel end/device end of either a print-advance or advance command and indicates a forms overflow condition. Paper advance is performed and paper stops at position designated by the command detail bits.

4.6.4. Status Byte Format for 0789/0798 Remote Printer

Bit	Condition Which Sets Bits	Meaning
0	Attention	Indicates transition from stop state to run state.
1	Status modifier	Set whenever the subsystem had to perform at least one error-recovery procedure in order to complete the outstanding command. Status modifier set without unit check implies that with error recovery, the command was completed. Autosense follows.
2	—	Not used; always set to zero.
3	Busy	Indicates that the device cannot execute the command because it is executing a previously issued command.
4	Channel end	Indicates that the subsystem is ready to accept a new command.
5	Device end	Indicates the completion of a command initiated by the channel.
6	Unit check	Specifies that at least one bit is set in sense byte 0. Autosense follows.
7	Unit exception	Presented with device end of either a print-advance or advance command and indicates a form-overflow condition. Paper advance is performed and paper stops at position designated by the command detail bits.

4.6.5. Status Byte Format for 0719 Card Reader

Bit	Condition Which Sets Bits	Meaning
0	Attention	Indicates transition from stop state to run state.
1	Status modifier	Set along with channel end/device end whenever the paper peripheral controller (PPC) invokes at least one error recovery procedure in order to complete the outstanding command. Status modifier set without unit check implies that, with error recovery, the command was completed. Autosense follows.
2	—	Not used; always set to zero.
3	Busy	Indicates that the device cannot execute the command due to executing a previously issued command.
4	Channel end	Set concurrently with device end by the PPC.
5	Device end	Specifies completion of command by the PPC and readiness to accept a new command.
6	Unit check	Specifies that at least one bit is set in sense byte 0, 1, or 2. Autosense follows.
7	—	Not used; always set to zero.

4 6 6. Status Byte Format for 0608 Card Punch

Bit	Condition Which Sets Bits	Meaning
0	Attention	Indicates transition from stop state to run state.
1	Status modifier	Set along with channel end/device end whenever the PPC calls at least one recovery procedure in order to complete the outstanding command. When the status modifier bit is set without the unit check being set, it implies that with error recovery, the command was completed successfully. Autosense follows.
2	—	Not used; always set to zero.
3	Busy	Indicates that the device cannot execute the command because it is executing a previously issued command.
4	Channel end	Set concurrently with the device end by the PPC.
5	Device end	Specifies command completion by PPC.
6	Unit check	Indicates at least one bit is set in sense byte 0, 1, or 2. Autosense follows.
7	—	Not used; always set to zero.

4.6.7. Status Byte Format for UNISERVO 10 Magnetic Tape Type 0871

Bit	Condition Which Sets Bits	Meaning
0	Attention	Indicates tape unit is ready for operation. Operator intervention (e.g., load new tape) is required. This status is unsolicited and not the result of any previous channel action.
1	Status modifier	Presented with the busy bit to indicate the controller is busy. Also may be presented with device end bit to indicate successful recovery from error.
2	Control unit end	Presented when an operation having control unit busy is complete.
3	Busy	Presented: ■ With status modifier bit to indicate controller is busy. ■ To indicate tape drive is busy executing a command.
4	—	Not used; always set to zero.

Status Byte Format for UNISERVO 10 Magnetic Tape Type 0871 (cont)

Bit	Condition Which Sets Bits	Meaning
5	Device end	Indicates that: ■ An operation is complete at the controller level. When errors are detected before tape motion is initiated, device end is not presented with error status. Data transfer operations aborted while still in progress (e.g., due to equipment check) cause device end to be sent with unit check. ■ A rewind, as well as other operations, have completed at the tape drive. If control terminates unsuccessfully in the tape drive, device end bit is presented with unit check and control unit end.
6	Unit check	Sets bit when any of the following occurs: ■ A bit in sense byte 0 was set because of the current operation. If the error codition was detected before tape motion begins, unit check is presented without normal ending status end; ■ A rewind operation terminated unsuccessfully. Device-end bit is presented with unit check. ■ A read-backward, backspace-block, or backspace-file operation is attempted when tape is positioned at load point;

		■ A rewind with interlock was completed at the controller level; i.e., when the tape drive becomes nonready, device end is presented, and control unit end is presented if the operation is initiated; ■ The selected tape drive is busy; i.e., ready and rewinding. End status is not presented with unit check. When a rewind tape drive is selected the tape drive is busy until the device end associated with the end of rewind is accepted by the channel; or ■ Presented with device-end to indicate an error was unrecovered.
7	Unit exception	Presented with device-end bit when: ■ A write, write-tape-mark, or erase operation is performed in the end-of-tape area; or ■ A tape mark is sensed during a read, read-backward, forward-space-block, or backspace-block operation.

4.7.1. I/O Sense Data Byte Definitions for 8417/8419 Disk

Bit Position	Bit Designation	Definition
		Sense Data Byte 0
0	Command reject	Indicates an illegal command code occurred. It could be a write command to a file-protected device, unassigned command codes, a write command with programmed offset, or out-of-bounds command parameters (invalid address).
1	Intervention required	Indicates that some manual intervention is required to make the device availbale to the system. It can be set with either stop-state or device-not-present and stop-state.
2	Output parity check	Indicates data transferred contains wrong parity at the time it was to be written onto the disk.
3	Equipment check	Indicates a serious malfunction occurred within the subsystem. If set alone, it indicates that the direct memory access (DMA) control logic contains an error. When set with device check, it indicates a serious problem within the device. When set with seek incomplete, it indicates the device, after having been issued a seek instruction, did not complete that movement within the required period of time. When set with unselected status, it indicates that one of the status lines between the controller and device was active when no devices were selected. When set with

		track overrun, it indicates that a problem exists relative to the rotational speed or sensing of the disk drive. When set with no clocks, it indicates too much time elapsed with no data or clocks being supplied by the device.
4	Data check	Specifies a abnormal pattern exists in the error correction code (ECC) bytes of the control unit. It can be set with the ID field check or data field check, together with either sync region or ECC check. These combinations of sense bits determine the location and nature of the error. When set with record number miscompare, it indicates positioning control errors, and is set with these bits only in the absence of an ECC error in the ID field.
5	Overrun	Indicates that either data was not accepted or data was not provided fast enough to satisfy the demands of the device. This condition normally indicates a problem in the controller data separation hardware.
6	Stop State	Indicates that the drive has no power applied and is not available for use. If a drive is not connected to the system but addressed, the same indication results.
7	Device check	Indicates that a device is unsafe due to loss of DC voltage, disk speed below 80% of normal, write oscillator not synchronous with servo track, or no write transitions when the write gate is active and address mark is not active, a seek failed to complete within 230 milliseconds, or a guard band was detected.

I/O Sense Data Byte Definitions for 8417/8419 Disk (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 1
0	ID field check	Indicates the pertinent sense bits set during the processing of an ID field. This bit is used primarily for diagnostic purposes and serves in isolating problems.
1	Track overrun	Indicates an operating device encounters an index mark when it is oriented on an ID or data field, or the gap between the two.
2	Cylinder end	Indicates an attempt was made to increment the head number beyond the actual heads of the drive. When set with no record found, it indicates a search/read was unsuccessful.
3	Device type	Specifies the type of device selected by given address. When set, indicates a removable media disk drive.
4	No record found	Indicates, when set alone, that two revolutions of index passed without satisfying the search argument. When set with sync region error, it indicates no address mark was detected on the disk surface. It also can indicate the record number in the ICW exceeds the highest record number

		written on the track, for example 60. With multitrack search/read commands, this bit is set with cylinder end, indicating that the search argument could not exceed the cylinder head limit.
5	File protect	Indicates that the selected device is unavailable for write operations. Data can be read from the file but any attempt to write will cause unit check status and command reject to be set.
6	Sync region error	Indicates either an error in gap data, gap detection hardware, or address mark write hardware.
7	Data field check	Indicates an error occurred when processing the data field. This bit is mainly used for diagnostic purposes.
Sense Data Byte 2		
0	Seek incomplete	Indicates a failure occurred within the device so that it was unable to complete accessor movement within a predetermined time interval.
1	Write protect/ offset unsafe	Indicates that a write has been attempted with the head offset active or write protect in the device. This implies either a malfunction in the execution of the nonoffset implied seek or write status verification or a device malfunction.

I/O Sense Data Byte Definitions for 8417/8419 Disk (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 2 (cont)
2	Head cylinder miscompare	Specifies a positioning error. For read-data and write-data commands, this indicator denotes that the head and cylinder information recovered from the disk surface does not compare with that provided by the ICW. This bit may be set with flag byte miscompare. It is not set with read-ID commands or if there is an ECC parity error for the ID field.
3	Record number miscompare	Sets bit with data check to indicate that the record number as read from the disk is not the one expected. (The record number reported in sense byte 4 will be for the expected record.) It indicates that one or more records could have been skipped or that some hardware failure occurred when the address mark or ID field was written.
4	Flag byte miscompare	Indicates that the flag information read from the disk does not compare with that of the software. Occurs when encountering a defective or alternate track location. This bit is set only if there is not ECC parity error at the end of the ID field. Although some bits within the flag byte have no definition, they are compared during read operations and must compare exactly. The occurrence of a flag miscompare causes the operation to terminate immediately.

5	Unselected status	Indicates that one or more of the device status lines were active when no device was selected. When set with equipment check, it indicates an interface failure between the controller and device.
6	ECC check	Set with data check and either ID field check or data field check to indicate that a nonzero residue existed in the ECC register of the control after the field was read. When set with equipment check, it indicates a failure within the ECC hardware during a write operation.
7	No clocks	Set with equipment check to indicate that no clock pulses have been detected for a period of 1 millesecond while the controller was active.
Sense Data Byte 3		
0	Device not present	Indicates that the addressed device is not present in the system.
1	Fixed heads	Indicates that the 60 fixed heads are installed within the drive. If this signal is not present when the command attempts to address the heads, cylinder, head, or record capacity exceeded and command reject are also set.
2	Cylinder addressing feature	Indicates the cylinder addressing feature has been installed on an 8417 disk. This feature permits cylinder 0 through 560 to be addressed.

I/O Sense Data Byte Definitions for 8417/8419 Disk (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 3 (cont)		
3	Cylinder, head or record capacity exceeded	Indicates an attempt was made to select a cylinder or head or record address that exceeded the valid limits for the particular features configured. It is set along with command reject.
4	Index passed	Indicates that the index has been passed once during a search/read command to allow a proper start.
5	Low found	Indicates a low condition has been satisfied during a search/read operation prior to the sector on which the error was detected.
6	Search satisfied	Indicates that the search portion of a search/read command has been satisfied on the record specified, even though an error has been detected.
Sense Data Byte 4		
0—7	Record number	Contains the number of the track record that the associated sense information applies.

Sense Data Byte 5		
0—7	Physical read number	Contains the number of the device head selected at the time that the sense information applies.
Sense Data Byte 6		
0—7	Device status byte	Permits device status to be presented when both head select and device bus bit 7 are set. Each is defined as follows:

Bit	Name	Definition
0	PLO sync unsafe	PLO synchronization loss due to missing servo data.
1	Speed unsafe	Disk speed less than 80% of normal. Head positioned over landing zone.
2	Guard band detected	Guard band 1 or 2 detected during a seek or when access ready is active.
3	DC power unsafe	DC power loss or out of tolerance.

I/O Sense Data Byte Definitions for 8417/8419 Disk (cont)

Bit Position	Bit Designation	Definition		
Sense Data Byte 6 (cont)				
0—7 (cont)	Device status byte	Bit	Name	Definition
		4	PLO unsafe	Indicates loss of synchronization of the PLO during a write operation.
		5	Seek too long	Seek operation exceeded 230 milliseconds.
		6	Write unsafe	Indicates one or more of the following: 1. Both read and write gates are active 2. Multiple leads selected 3. No write current or no transitions detected with write gate active 4. Write current exceeds maximum

		7	Write current unsafe	Write current not a proper level
Sense Data Byte 7				
—	Undefined	—		
Sense Data Byte 8				
0—7	ECC displacement	Indicates the displacement in bytes from the beginning of the data field to the beginning of the error field to be corrected with the error pattern bytes.		
Sense Data Byte 9				
0—7	First pattern byte	Indicates error pattern is to be used with ECC displacement.		
Sense Data Byte 10				
0—7	Second pattern byte	Indicates error pattern byte to be used with ECC displacement.		

I/O Sense Data Byte Definitions for 8417/8419 Disk (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 11		
—	Undefined	—

4.7.1.1. Summary of I/O Sense Data Bytes for 8417/8419 Disk

Bit	0	1	2	3	4	5	6	7
Sense Data Byte 0	Command reject	Intervention required	Output parity check	Equipment check	Data check	Overrun	Stop state	Device check
1	ID field check	Track overrun	Cylinder end	Device type	No record found	File protect	Sync region error	Data field check

I/O SENSE DATA BYTE DEFINITIONS FOR DMA DEVICES (cont)

2	Seek incomplete	Write protect/ offset unsafe	Head/cylinder miscompare	Record number miscompare	Flag byte miscompare	Unselected status	ECC check	No clocks
3	Device not present	Fixed heads	Cylinder addressing feature	Cylinder, head or record capacity exceeded	Index passed	Low found	Search satisfied	N/A
4	Record number							
5	Physical head number							
6	PLO sync unsafe	Speed unsafe	Guard band undetected	DC power unsafe	PLO unsafe	Seek too long	Write unsafe	Write current unsafe

Summary of I/O Sense Data Bytes for 8417/8419 Disk (cont)

Sense Data Byte	Bit 0 1 2 3 4 5 6 7
7	Not defined
8	ECC displacement
9	1st pattern byte
10	2nd pattern byte
11	Not defined

4.8.1. I/O Sense Data Byte Definitions for Single Line Communications Adapter (SLCA)

Bit Position	Bit Designation	Definition
Sense Data Byte 0		
0	Command reject	Sets bit if an invalid command is issued to the SLCA or a command sequence error occurs. See sense byte 1 bit 5 for details. Unit check status is set.
1	Intervention required	Not used; always set to zero
2	Bus out check	Sets bit if a byte is received by the SLCA on the D-bus with a parity error.
3	Equipment check	Sets bit if a parity error is detected by the SLCA during internal data manipulation in the SLCA. See sense byte 1 bits 0 and 1 for further details.
4	Data check	Function is feature dependent.
5	Overrun	Function is feature dependent.

I/O Sense Data Byte Definitions for Single Line Communications Adapter (SLCA) (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 0 (cont)		
6	Bus in check	Sets bit if a byte is received by the MCLM over the D-bus with a parity error.
7	Program alert	Sets bit if a command is issued to an invalid device address or if sense byte 1, bits 2, 3, 5, or 6 are set. Set the description of these bits in sense byte 1 for further details.
Sense Data Byte 1		
0	PIU parity error	Sets bit if a parity error is detected on the SLCA's internal data bus and not on the D-bus while the SLCA is performing a read or write operation with its PIU. Will be set in conjunction with sense byte 0, bit 3.
1	RAM parity error	Sets bit if a parity error is detected by the SLCA while reading a byte from its RAM. Will be set in conjunction with sense byte 0, bit 3.

2	MEM address error	The RAM address for a load RAM command exceeds RAM limits or the associated byte count would cause the address to exceed these limits, or the address for a load memory address command is not within the boundary of the RAM. Will be set in conjunction with sense byte 0, bit 7.
3	Check sum error	The check sum for a load RAM command does not equal the sum generated by the SLCA. Will be set in conjunction with sense byte 0, bit 7 if this error is on the check sum for one of the load RAM records. Will be set in conjunction with sense byte 0, bit 7 and sense byte 1, bit 6 if this error is on the overall check sum in the end record.
4	RAM not loaded	Sets bit if the SLCA's RAM is not yet flagged as executable.
5	Sequence error	Sets bit if any of the following occurs: ■ A read memory command is not immediately preceded by a load memory access command. Set in conjunction with sense byte 0, bit 0.

I/O Sense Data Byte Definitions for Single Line Communications Adapter (SLCA) (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 1 (cont)
5 (cont)	Sequence error	■ A text or end record is received via load RAM command prior to the initialization of a valid load RAM sequence by reception of a valid start record. Set in conjunction with sense byte 0 bit 7.
6	Load RAM record error	Sets bit in conjunction with sense byte 0 bit 1 if a load RAM command results in the SLCA receiving any of the following: ■ A record with a format control character other than the three specified (hex 10, 20, or 40). ■ A text record with a number of valid bytes less than 8 (0008_{16}) or greater than 128 (0080_{16}). ■ A termination from the MLCM before receiving a full 128 byte record. Sets bit in conjunction with sense byte 0 bit 7 and sense byte 1 bit 3 if there is an error detected on the overall check sum contained in the end record.

7	Asynchronous feature	Sets bit if the asynchronous feature is installed in the SLCA.

4.8.1.1. **Summary of I/O Sense Data Bytes for Single Line Communications Adapter (SLCA)**

Bit	0	1	2	3	4	5	6	7
Sense Data Byte 0	Command reject	Intervention required	Bus out check	Equipment check	Data check	Overrun	Bus in check	Program alert
1	PIU parity error	RAM parity error	MEM address error	Check sum error	RAM not loaded	Sequence error	Load RAM record error	Asynchronous feature

4.9.1. I/O Sense Data Byte Definitions for System 80 Workstation/Console Workstation

Bit Position	Bit Designation	Definition
		Sense Data Byte 0
0	Command reject	Sets bit to indicate that an invalid command was issued. Bit is set with program alert if either a user read was issued to the workstation in system mode or a system message read was issued to the workstation in workstation mode.
1	Intervention required	Sets bit to indicate a device is not ready. Bit is set with program alert when an invalid device address is received (out-of-range device).
2	Bus out check	Sets bit to indicate a parity error occurred on the D-bus while receiving a byte of data from the channel.
3	Equipment check	Sets bit to indicate one or more of the following: ■ a parity error occurred within the workstation controller due to microcode; ■ a RAM parity error occurred at the workstation;

		■ power on occurred at workstation; ■ a nonrecoverable programmable interface unit (PIU) error occurred at workstation; or ■ a check sum error occurred during a load RAM command.
4	Data check	Sets bit to indicate that an unsuccessful data transmission occurred between the workstation controller and the workstation in either direction.
5	—	Not used; always set to zero.
6	Bus in check	Sets bit to indicate a parity error occurred on the D-bus while sending a byte of data to the channel.
7	Program alert	Sets bit to indicate one or more of the following: ■ a user write command was issued in system mode; ■ operator pressed unlock key while command was outstanding;

I/O Sense Data Byte Definitions for System 80 Workstation/Console Workstation (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
7 (cont)	Program alert	■ workstation reports an out-of-bounds vector address during a load RAM command; ■ message waiting command was issued in system mode; or ■ load RAM command was issued in system mode. Bit is set with intervention if an invalid device address was received (out-of-range). Bit is set with command reject if a user read command was issued to the workstation in system mode or if a system message read was issued to the workstation in workstation mode.
		Sense Data Byte 1
0	Invalid device address	Sets bit to indicate that a portion of the DA/FC byte was invalid during a command.

1	WS not ready	Sets bit if the workstation does not respond when a workstation reset message results from D-bus reset; or if the workstation controller gets no response from the workstation during a command (other than sense or NO-OP).
2	—	Not used; always set to zero.
3	Interrupt active	Sets bit if the operator pressed the unlock key at the workstation while a command is outstanding for the workstation.
4	Load error	Bit is set with equipment check if the workstation reports a text record check sum error during a load RAM command. Bit is set with program alert if the workstation reports a RAM vector address (contained in the initial record) that exceeds the RAM limits.
5	—	Not used; always set to zero.
6	—	Not used; always set to zero.
7	Invalid command at WS	Sets bit to indicate that a user write command was sent to the workstation in system mode.

I/O Sense Data Byte Definitions for System 80 Workstation/Console Workstation (cont)

Bit Position	Bit Designation	Definition
	Sense Data Byte 2	
0	WSC microcode error	Sets bit to indicate a parity error was detected in the workstation controller during RAM access.
1	NRE PIU error	Sets bit to indicate a nonrecoverable D-bus error occurred related to the PIU device.
2	Power on	Sets bit to indicate that the workstation successfully completed power on and the associated confidence test.
3	RAM parity error	Sets bit to indicate that the workstation reported a parity error.
4	Transmit	Sets bit to indicate that the transmit key on the workstation has been depressed since the last command.
5	Function code ready	Sets bit to indicate that the operator pressed either the message waiting key or one of the function keys.

6	Mode change request	Sets bit to indicate that the operator requested the system to change the mode of the workstation from workstation mode to system mode or vice versa.
7	System mode	Sets bit to 1 when the workstation is in system mode. Sets bit to 0 when the workstation is in workstation mode.
Sense Data Byte 3		
0—7		A binary count of the number of times communication errors were dectected by the workstation controller (WSC) on the workstation controller/workstation interface since the last command.
Sense Data Byte 4		
0—7		A binary count of the number of times communication errors were detected by the workstation at the workstation/workstation controller interface since the last command.
Sense Data Byte 5		
0—7		A binary count of the number of times keyboard parity errors occurred at the workstation/keyboard interface since the last command.

4.9.1.1. Summary of I/O Sense Data Bytes for System 80 Workstation/Console Workstation

Sense Byte	Bit 0	1	2	3	4	5	6	7
0	Command reject	Intervention required	Bus out check	Equipment check	Data check	N/A	Bus in check	Program alert
1	Invalid device	WS not ready	N/A	Interrupt active	Load error	N/A	N/A	Invalid command at WS
2	WSC micro-code error	NRE PIU error	Power on	RAM parity error at WS	Transmit	Function code ready	Mode change request	System mode
3	Workstation controller detected communication error log counter.							
4	Workstation detected communication error log counter.							

5	Keyboard error log counter.

4.9.2. I/O Sense Data Byte Definitions for 8420/8422 Diskette

Bit Position	Bit Designation	Definition
Sense Data Byte 0		
0	Command reject	Sets bit if: ■ an invalid command code is issued; ■ a valid command code is issued to a feature not installed; or ■ an invalid sequence of commands was received.

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
1	Intervention required	Sets bit if: ■ an invalid device address is presented; ■ addressed drive is not installed; ■ addressed drive is in stop state; ■ a manual feed is in progress; ■ an interlock condition exists; ■ the autoloader is not at home position; ■ stacker is full or the hopper empty;

		■ a malfunction occurred during the unload or feed cycles; ■ no index pulses occurred during execution; or ■ drive became not ready during command execution.
2	Bus out check	Sets bit if a parity retry or error was detected on the transfer of a byte of data to the diskette controller.
3	Equipment check	Sets bit if: ■ a PROM parity retry occurred; ■ a diskette controller parity error occurred; ■ no index pulses occurred during execution; ■ no track 0 detected during recalibrate; ■ no disk sense signal occurred during command execution; or ■ an autoloader time out/hang occurred.

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
4	Data check	Sets bit when any of the following occurs: ■ read check error; ■ no data separator lock error; ■ ID CRC error; ■ track mismatch error; ■ side mismatch error; ■ sector mismatch error; ■ record length mismatch error;

		■ data CRC error; ■ control record error; ■ end-of-volume record error; or ■ illegal media.
5	—	Not used; always set to zero.
6	Bus in check	Sets bit if a parity retry or error was detected on the transfer of a byte of data from the subsystem.
7	Program alert	Sets bit if: ■ media (disk) is write protected; ■ data set label is not found or is invalid; ■ device is in the wrong operation mode; ■ not enough parameter bytes are transmitted;

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 0 (cont)		
7 (cont)	Program alert	■ side 2 is specified when a 1-sided diskette is installed; ■ a RAM parity error exists; ■ hexadecimal FF is specified in first parameter byte; ■ EOD record over-read; or ■ an invalid device address is specified.
Sense Data Byte 1		
0	Illegal media	Sets bit if: ■ ID feed track-byte is not 00 through 4C or FF;

		■ ID field side byte is not 00 or 01; ■ ID field sector byte is not 01 through 1A; ■ ID field length byte is not 00 through 02; or ■ the data AM was not detected or was invalid.
1	Invalid mode	Sets bit if device is in wrong operating mode.
2	Invalid sequence	Sets bit if: ■ diagnostic write command was not enabled; ■ not enough parameter bytes were transmitted; ■ hexadecimal FF was specified in first parameter byte; or ■ EOD record was over-read.

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 1 (cont)
3	Invalid parameter	Sets bit if: ■ illegal parameter byte was transmitted; ■ invalid device address was presented; ■ side 2 was specified on 1-sided diskette; ■ hexadecimal FF was specified in first parameter byte; or ■ invalid command code was issued.
4	Not installed	Sets bit if: ■ invalid device address was presented;

		■ address drive was not installed; or ■ feature was not installed.
5	Parity error	Sets bit if: ■ bus-in parity retry or error occurs; ■ bus-out parity retry or error occurs; ■ PROM parity error occurs; or ■ subsystem parity error occurs;
6	Stop state error	Sets bit if: ■ the addressed drive is in the stop state; ■ the addressed drive became not ready during command execution; or ■ the addressed drive never became ready during feed command.

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 1 (cont)
7	Interlock error	Sets bit when the interlock switch is tripped on addressed drive.
		Sense Data Byte 2
0	No data separator lock error	Sets bit if: ■ disk read circuits could not lock onto data from the diskette; or ■ no disk service-signal occurred after once having locked on.
1	Side error	Sets bit if: ■ a side mismatch occurred in ID field read; or ■ side 2 was specified when a 1-sided diskette was installed.

2	Track error	Sets bit if: ■ a track mismatch occurred in ID field read; or ■ no track 0 was detected during recalibrate.
3	Record length error	Sets bit if a record length mismatch occurred in ID.
4	Sector error	Sets bit if: ■ a sector mismatch occurred in field read; or ■ the sector specified is greater than the number of sectors on the cylinder.
5	ID CRC	Sets bit if an ID field CRC error occurred.
6	Data CRC	Sets bit if data field CRC error occurred.
7	Retry	Sets bit if: ■ a repositioning of the R/W head occurred;

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 2 (cont)		
		■ a reread of the ID or data field occurred; or ■ a retry of a parity error occurred.
Sense Data Byte 3		
0	DSL not found	Sets bit if the data set label was not found.
1	DSL invalid	Sets bit if the data set label was invalid.
2	Control AM	Sets bit if a record that was read was preceded by a control address mark.
3	DSL WP error	Sets bit if the data set label has a write protect indication.
4	Disk parity error	Sets bit if a parity error occurred within the disk logic during writes to the disk.

5	EOD/EOE	Sets bit if: ■ end of data (EOD): In DSM, the last valid record of the last or only volume of a file has been read. In DAM, the last sector of the diskette has been read. ■ end of extent (EOE): In DSM, the last valid record of the last or only volume of a file has been written. In DAM, the last sector of the diskette has been written.
6	Read check	Sets bit if a CRC error occurred while read checking a data field after a write command.
7	HWP	Sets bit if the diskette is hardware write protected.
Sense Data Byte 4		
0	Autoloader unload fault	Sets bit if a malfunction occurred during the unload portion of the cycle.
1	Autoloader feed fault	Sets bit if a malfunction occurred during the feed portion of the cycle.
2	Autoloader stacker full	Sets bit if the output stacker is full.

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 4 (cont)		
3	Autoloader hopper empty	Sets bit if the input hopper is empty.
4	Autoloader hang	Sets bit if a mechanism malfunction timeout occurred during operation.
5	Autoloader busy	Sets bit if a manual feed switch operation is in progress.
6	Autoloader jam	Sets bit if a diskette is jammed in the feed path.
7	Data late	Sets bit if a byte of data was lost due to the subsystem failing to respond in time.
Sense Data Byte 5		

<table>
<tr><td>0, 1, 2</td><td>Mode bits</td><td>Indicates the current operation mode of the addressed device as follows:
<table>
<tr><th>Mode bits</th><th>0</th><th>1</th><th>2</th><th></th><th>Mode</th></tr>
<tr><td></td><td>0</td><td>0</td><td>0</td><td>=</td><td>Format label</td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td>=</td><td>Data set label — R at BOE</td></tr>
<tr><td></td><td>1</td><td>0</td><td>1</td><td>=</td><td>Data set label — R/W at BOE</td></tr>
<tr><td></td><td>1</td><td>1</td><td>0</td><td>=</td><td>Data set label — R/W at EOD</td></tr>
</table></td></tr>
<tr><td>3</td><td>H autoloader installed</td><td>Indicate an autoloader mechanism is installed on the addressed drive when bit is set to 1.</td></tr>
<tr><td>4</td><td>Two-sided</td><td>Indicates type of diskette installed. When bit is set to 0, a 1-sided diskette is installed. When bit is set to 1, a 2-sided diskette is installed.</td></tr>
<tr><td>5*</td><td>H MFM density</td><td>Indicates the recording density on the diskette. When bit is set to 0, recording density is single density. When bit is set to 1, recording density is double density.</td></tr>
<tr><td>6*</td><td>FM density</td><td>Indicates the recording density on the diskette. When bit is set to 0, recording density is FM. When bit is set to 1, recording density is FM.</td></tr>
</table>

I/O Sense Data Byte Definitions for 8420/8422 Diskette (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 5 (cont)		
7	HWP	Indicates that installed diskette contains hardware write protect notch.
Sense Data Byte 6		
0—7	Track Address	Indicates the current track address in binary (bit 0 is MSB)
Sense Data Byte 7		
0	L side 0	Indicates the current side address. When bit is set to 0, side 0 is the current side. When bit is set to 1, side 1 is the current side.
1—7	Sector address	Indicates the current sector address in binary (bit 1 MSB).

*Bits 5 and 6 of sense byte 5 are not valid until after the first media related command has been executed on the addressed drive. If bit 5 and 6 are both 0, the recording density is not known.

4.9.2.1. Summary of I/O Sense Data Bytes for 8420/8422 Diskette

Sense Byte \ Bit	0	1	2	3	4	5	6	7
0	Command reject	Intervention required	Bus out check	Equipment check	Data check	Not used	Bus in check	Program alert
1	Illegal media	Invalid mode	Invalid sequence	Invalid parameter	Not installed	Parity error	Stop state error	Interlock error
2	No data separator lock error	Side error	Track error	Record length error	Sector error	ID CRC	Data CRC	Retry
3	DSL not found	DSL not valid	Control AM	DSL WP error	Disk parity error	EOD/EOE	Read check	HWP
4	Autoloader unload fault	Autoloader feed fault	Autoloader stacker full	Autoloader hopper empty	Autoloader hang	Autoloader busy	Autoloader jam	Data late

Summary of I/O Sense Data Bytes for 8420/8422 Diskette (cont)

Sense Byte \ Bit	0	1	2	3	4	5	6	7
5	Mode bit 0	Mode bit 1	Mode bit 2	H autoloader installed	Two-sided	H MFM density	FM density	HWP
6	The current track address.							
7	L side zero	The current sector address.						

4.9.3. I/O Sense Data Byte Definitions for 0776/0789 Printer

Bit Position	Bit Designation	Definition
		Sense Data Byte 0
0	Command reject	Sets bit when invalid command is issued. Unit check status is set and no action is initiated by the PPC.
1	Intervention required	Sets bit if a condition is detected that requires manual intervention, if an out-of range address is detected, or if a feature that was called for was not installed.
2	Bus out check	Sets bit when a parity error is received during a D-bus data transfer on controller inbound data.
3	Equipment check	Sets bit when any of the following error conditions are detected within the PPC or device: ■ a parity error detected when reading VFB; ■ device check; ■ nonrecoverable PIU error;

I/O Sense Data Byte Definitions for 0776/0789 Printer (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
3 (cont)	Equipment check	■ PPC parity error; ■ a print or advance command exceeded the maximum time allowed; ■ paper feed motor motion error; ■ forms runaway; ■ temperature error; ■ actuator error; ■ printer RAM parity error; or ■ band error.

4	Data check	Sets bit when one of the following conditions is present, unless suppressed by the data check disable command: ■ an unprintable character received by printer; or ■ data parity occurred on data transferred to printer on each of four tries.
5	—	Not used; always set to zero.
6	Bus in check	Sets bit when bus parity error is received during a D-bus data transfer on controller outbound data.
7	Program alert	Sets bit when an out of range device address is presented to the PPC during command initiation or when a VFB sequence error or VFB check occurs.
Sense Data Byte 1		
0	Forms out	Sets bit when forms low indication is present and last form moved the paper to or past home paper position. Printer indicates not ready condition.

I/O Sense Data Byte Definitions for 0776/0789 Printer (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 1 (cont)		
1	Forms low	Sets bit when bottom edge of last form passed form detector switch. Printer remains ready until controller declares a paper-out condition. Unit check status is generated when condition is first detected.
2	VFB check	Sets bit when an advance command is issued and the skip code specified by D, E, and F bits (A=1) is not present in the VFB. No paper advance takes place.
3	Forms check	Sets bit when a forms runaway, jam, tear condition, or stacker full occurs.
4	Unprintable characters	Sets bit when one or more nonprintable characters were transmitted to printer. These characters are printed as a space, if enabled.
5	VFB parity error	Set if a parity error is detected when reading the VFB.

6	Stop state	Sets bit when printer is in stop state. Printer may enter stop state by way of stop switch or on error condition.
7	Printer parity error	Sets bit when one or more parity errors occur on the data transferred to printer on each of four tries.
Sense Data Byte 2		
0	Bit 1 print band sense	Used in conjunction with bit 2 to identify which print band is mounted on the printer.
1	Vertical format buffer sequence error	Sets bit if a print-advance or advance command was received after power-on system reset or if operator initialized the VFB and no load-VFB command was issued.
2	Bit 2 print band sense	Used in conjunction with bit 0 to identify which print band is mounted on the printer.
3	6/8 line spacing	Specifies 8 lines per inch
4	Nonrecoverable PIU error	Sets bit if a nonrecoverable D-bus error occurred related to the PIU device.

I/O Sense Data Byte Definitions for 0776/0789 Printer (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 2 (cont)
5	Printer time-out	Sets bit if one of the following is present: ■ printer not installed; ■ printer offline; ■ printer power off; or ■ no response from printer.
6	PPC parity error	Sets bit when a parity error occurs in the PPC during data transfer.
7	Device check	Sets bit when printer detects hardware malfunction or a not-ready condition during printing or advancing paper.

Sense Data Byte 3		
0	—	Not used; always set to zero.
1	—	Not used; always set to zero.
2	Invalid sequence	Sets bit if the diagnostic write enable command has not preceded all other diagnostic write commands.
3	—	Not used; always set to zero.
4	—	Not used; always set to zero.
5	—	Not used; always set to zero.
6	—	Not used; always set to zero.
7	—	Not used; always set to zero.

I/O Sense Data Byte Definitions for 0776/0789 Printer (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 4
0	Stacker forms check	Sets bit when the forms stacker is full.
1	Forms jam	Sets bit when the paper has stopped moving while a line advance operation is being performed.
2	Paper feed motor motion error	Sets bit when the acceleration or deceleration of the paper is too slow.
3	Forms runaway	Sets bit when the form has been continuously advanced for an excessive period of time.
4	Temperature error	Sets bit when an abnormal temperature condition exists at the device.
5	Actuator error	Sets bit when either an open or short circuit exists in one of the print hammer actuators.
6	Printer RAM parity error	Sets bit when the printer has detected a parity error while reading its RAM.

7	Band error	Sets bit when the printer has failed to detect a sprocket signal, has detected an extra sprocket signal, or has failed to detect a font mark.

4.9.3.1. Summary of I/O Sense Data Bytes for 0776/0789 Printer

Sense Data Byte	Bit 0	1	2	3	4	5	6	7
0	Command reject	Intervention required	Bus out check	Equipment check	Data check	—	Bus in check	Program alert
1	Forms out	Forms low	VFB check	Forms check	Unprintable characters	VFB parity error	Stop state	Printer parity error
2	Bit 1 print band sense	VFB sequence error	Bit 2 print band sense	6/8 line spacing	Nonrecoverable PIU error	Printer time-out	PPC parity error	Device check

Summary of I/O Sense Data Bytes for 0776/0789 (cont)

Bit	0	1	2	3	4	5	6	7
Sense Data Byte 3	—	—	Invalid sequence	—	—	—	—	—
4	Stacker forms check	Forms jam	Paper feed motor motion error	Forms runaway	Temperature error	Actuator error	Printer RAM parity error	Band error

4.9.4. I/O Sense Data Byte Definitions for 0789/0798 Remote Printer

Bit Position	Bit Designation	Definition
		Sense Data Byte 0
0	Command reject	Set when either an invalid command or an invalid sequence of commands is issued. Also set if the contents of the RPI RAM are nonexecutable or a command is outside the basic set. Unit check status results, and no action is initiated by the subsystem.

1	Intervention required	Set when a condition is detected that requires manual intervention.
2	Bus out check	Set when a bus parity error is detected.
3	Equipment check	Set when any of the following conditions are detected: ■ parity error detected in the RPI, RPA, or by the printer; ■ print or advance operation exceeds time allotted; ■ error detected in a message on the cable; ■ forms jam; ■ paper feed motor motion error; ■ forms runaway; ■ temperature error; ■ actuator error; or ■ band error.

I/O Sense Data Byte Definitions for 0789/0798 Remote Printer (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
4	Data check	Set when any of the following conditions are present: ■ unprintable character received; or ■ check sum error detected.
5	—	Not used, set to 0.
6	Bus in check	A bus parity error received during a D-bus data transfer on controller outbound data.
7	Program alert	Set to indicate a possible programming error was detected as indicated by: ■ VFB check; ■ VFB sequence error;

		■ out-of-range address; ■ memory address error; ■ load RAM sequence error; ■ load RAM record error; ■ check sum error; or ■ invalid device address.
Sense Data Byte 1		
0	PIU parity error	When set, indicates a parity error detected on the RPI internal data bus while performing a read or write operation with its PIU. Is set in conjunction with sense byte 0, bit 3.
1	RPI RAM parity error	When set, indicates a parity error detected by the RPI while reading a byte from its RAM. Is set in conjunction with sense byte 0, bit 3.

I/O Sense Data Byte Definitions for 0789/0798 Remote Printer (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 1 (cont)
2	MEM address error	When set, indicates the RAM address for the load RAM command exceeds: ■ RAM limits; ■ associated byte count would cause the address to exceed these limits; or ■ address for a load memory command is not within the boundary of the RAM. Is set in conjunction with sense byte 0, bit 7.
3	Check sum error	When set, indicates the check sum for a load RAM command does not equal the sum generated by the RPI. Is set in conjunction with sense byte 0, bit 7 if this error is on the check sum for one of the load RAM records. Is set in conjunction with sense byte 0, bit 7 and sense byte 1, bit 6 if this error is on the overall check sum in the end record.

4	RPI RAM not loaded	When set, indicates the RPI RAM is not yet flagged as executable.
5	Sequence error	Set to one if: ■ read memory command is not immediately preceded by a load-memory address command. Is set in conjunction with sense byte 0, bit 0; or ■ text record is received by way of the load RAM command prior to the initiation of a valid load RAM sequence by reception of a valid start record. Is set in conjunction with sense byte 0, bit 7.
6	Load RAM record error	When set in conjunction with sense byte 0, bit 7, indicates a load RAM command resulted in the RPI receiving: ■ a record with a format control character other than the three specified: 10_{16}, 20_{16}, or 40_{16}; ■ a text record with a number of valid bytes having a value less than 8 (0008_{16}) or greater than 128 (0080_{16}); or ■ a termination from the channel before receiving a full 128-byte record. When set in conjunction with sense byte 0, bit 7 and sense byte 1, bit 3, an error is detected on the overall check sum contained in the end record.

I/O Sense Data Byte Definitions for 0789/0798 Remote Printer (cont)

Sense Data Byte 1 (cont)		
7	RPI feature	Always set to 1.
Sense Data Byte 2		
0	Forms out	When set, indicates forms low and the last form advanced the paper to or past the home paper position. Printer not ready status.
1	Forms low	When set, indicates bottom edge of last form passed the form detecter switch. Printer remains ready until controller declares a forms out condition. Unit check status is displayed when this condition is initially detected.
2	VFB check	When set, indicates an advance command was issued and the skip code specified by the D, E, and F bits (A=1) is not present in the VFB. Paper advance is inhibited.
3	Forms check	A printer forms runaway timeout condition was detected by the RPA.
4	Unprintable characters	When set, indicates that one or more unprintable characters were detected in the line buffer of the printer. The unprintable characters reprinted as a space.

5	—	Always set to 0.
6	Printer not ready	When set, indicates an inactive level is detected on the printer ready line from the printer.
7	Printer parity error	When set, indicates printer reported a parity error in data being received from the RPA.
Sense Data Byte 3		
0	Bit 1 print band sense	Identifies print band mounted on the printer. Is set in conjunction with sense byte 3, bit 2.
1	Vertical format buffer sequence error	When set, indicates a print-advance or advance command was received after either power-on, system reset, or operator initialization of the VFB and no load VFB command was issued.
2	Bit 2 print band sense	Identifies print band mounted on the printer. Is set in conjunction with sense byte 3, bit 0.
3	6/8 line spacing	When set, indicates 6/8 lpi switch is set to the 8 lpi position.
4	—	Always set to 0.

I/O Sense Data Byte Definitions for 0789/0798 Remote Printer (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 3 (cont)
5	Printer time-out	When set, indicates printer did not complete either a print or a form advance operation in less than 8 seconds after having acknowledged the command.
6	—	Always set to 0.
7	Device check	When set, indicates the printer reported a hardware malfunction or a not-ready condition during printing or advancing paper.
		Sense Data Byte 4
0	RPA power-on	When set, indicates the RPA successfully completed its power-on-confidence test.
1	RPA message error	When set, indicates the RPI detected an error in a message from the RPA.
2	Invalid diagnostic sequence	When set, indicates a diagnostic write data buffer command that did not immediately follow a diagnostic write enable command was received from the channel.

3	RPI message error	When set, indicates the RPA reported an error in a message from the RPI.
4	No response from RPA	When set, indicates the RPI received no response while transmitting to the RPA.
5	Unrecoverable RPA message error	When set, indicates the RPI detected an error in four successive message transmissions from the RPA.
6	Unrecoverable RPI message error	When set, indicates the RPA reported an error in four successive message transmissions from the RPI.
7	—	Always set to 0.
Sense Data Byte 5		
0	Stacker forms check	When set, indicates that the forms pullout stacker is full.
1	Forms jam	When set, indicates that the paper forms stopped moving during a line advance operation.
2	Paper feed motor error	When set, indicates starting and stopping of the paper forms is too slow.

I/O Sense Data Byte Definitions for 0789/0798 Remote Printer (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 5 (cont)		
3	Forms runaway	When set, indicates paper forms have been advanced for an excessive period of time.
4	Temperature error	When set, indicates an abnormal temperature condition exists at the device.
5	Actuator error	When set, indicates either an open or short circuit exists in one of the print hammer actuators.
6	Printer RAM parity error	When set, indicates that the printer detected a parity error while reading its RAM.
7	Band error	When set, indicates the printer failed to detect a sprocket signal, detected an extra sprocket signal, or failed to detect a font mark.

Sense Data Byte 6		
0	Unrecoverable printer parity error	When set, indicates the printer reported a parity error in data received from the RPA during each of four successive transfers of the same print line.
1	Printer power-off	When set, indicates an inactive level was detected on the power signal line from the printer.
2	RPA RAM parity error	When set, indicates a parity error was detected by the RPA while reading a byte from its RAM.
3	No response from printer	When set, indicates printer did not acknowledge a command or data transfer from the RPA within one millisecond.
4 through 7	—	Always set to 0.

I/O Sense Data Byte Definitions for 0789/0798 Remote Printer (cont)

Bit Position	Bit Designation	Definition
	Sense Data Byte 7	
0	—	Always set to 0.
1	Command sequence number	Most significant bit.
2 through 6	Command sequence numbers	Intermediate bits.
7	Command sequence number	Least significant unit.

4.9.4.1. Summary of I/O Sense Data Bytes for 0789/0798 Remote Printer

Bit	0	1	2	3	4	5	6	7
Sense Data Byte 0	Command reject	Intervention required	Bus out check	Equipment check	Data check	—	Bus in check	Program alert
1	PIU parity error	RPI RAM parity error	MEM address error	Check sum error	RPI RAM not loaded	Sequence error	Load RAM record error	RPI feature
2	Forms out	Forms low	VFB check	Forms check	Unprintable characters	—	Printer not ready	Printer parity error
3	Bit 1 print band sense	VFB sequence error	Bit 2 print band sense	6/8 line spacing	—	Printer time-out	—	Device check

4	RPA power-on	RPA message error	Invalid diagnostic sequence	RPI message error	No response from RPA	Unrecoverable RPA message error	Unrecoverable RPI message error	—
5	Stacker forms check	Forms jam	Paper feed motor error	Forms runaway	Temperature error	Actuator error	Printer RAM parity error	Band error
6	Unrecoverable printer parity error	Printer power-off	RPA RAM parity error	No response from printer	—	—	—	—
7	—	Command sequence number (MSB)	Command sequence numbers					Command sequence number (LSB)

4.9.5. I/O Sense Data Byte Definitions for 0719 Card Reader

Bit Position	Bit Designation	Definition
		Sense Data Byte 0
0	Command reject	Sets bit when an invalid command is issued. Unit check is also set, and no action is initiated by the PPC.
1	Intervention required	Sets bit when a condition is detected that requires manual intervention, such as: ■ Hopper empty ■ Stacker full ■ Not ready — Power off — Initial power-up clear

I/O Sense Data Byte Definitions for 0719 Card Reader (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
1 (cont)		— Door interlock open — Offline — STOP switch activated ■ Input check.
2	Bus out check	Sets bit when a bus parity error is received during D-bus transfer on controller inbound data.
3	Equipment check	Sets bit on PPC RAM data store parity error, such as PPC parity error, card operation not completed in maximum time, or nonrecoverable PIU error.

4	Data check	Sets bit on an incorrect parity from device, device read check, device input check, or multiple punch error.
5	Overrun	Not used; always set to zero.
6	Bus in check	Sets bit when a bus parity error is received during a D-bus transfer on controller outbound data.
7	Program alert	Sets bit when an out-of-range device address is presented to the PPC during command sequence.
	Sense Data Byte 1	
0	Device not ready	Sets bit if the device is offline, power is off, interlock is open, feature not installed or STOP switch is depressed.
1	Stacker full	Sets bit when stacker is full.
2	Hopper empty	Sets bit when hopper is empty.
3	Input check	Sets bit if device detects a misfeed or mispick condition.
4	—	Not used; always set to zero.

I/O Sense Data Byte Definitions for 0719 Card Reader (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 1 (cont)		
5	Read check	Sets bit if device detects an error at read station.
6	Stop state	Sets bit if device is in stop state. It may be entered by stop or device error.
7	Parity check	Sets bit for parity error from device.
Sense Data Byte 2		
0	Multiple punch	Sets bit if the device detects more than one hole punched in columns 1 through 7.
1	—	Not used; always set to zero.

2	Invalid sequence	Sets bit if the diagnostic-write-enable command has not preceded all other diagnostic write commands.
3	—	Not used; always set to zero.
4	Nonrecoverable PIU error	Sets bit if a nonrecoverable error occurs related to the PIU device.
5	—	Not used; always set to zero.
6	PPC RAM parity error	Set if a parity error occurred in the PPC during a data transfer.
7	—	Not used; always set to zero.

4.9.5.1. Summary of I/O Sense Data Bytes for 0719 Card Reader

Sense Data Byte	Bit 0	1	2	3	4	5	6	7
0	Command reject	Intervention required	Bus out check	Equipment check	Data check	—	Bus in check	Program alert
1	Device not ready	Stacker full	Hopper empty	Input check	—	Read check	Stop state	Parity check
2	Multiple punch	—	Invalid sequence	—	Nonrecoverable PIU error	—	PPC RAM parity error	—

4.9.6. I/O Sense Data Byte Definitions for 0608 Card Punch

Bit Position	Bit Designation	Definition
		Sense Data Byte 0
0	Command reject	Sets bit when an invalid command or command sequence is issued. Unit check status is set and no action is initiated by the PPC.
1	Intervention required	Sets bit when any of the following conditions (that require manual intervention) occurs: ■ Hopper empty ■ Stacker full ■ Not ready — Power off — Initial power up clear — Door interlock open

I/O Sense Data Byte Definitions for 0608 Card Punch (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
		— Offline — STOP switch pressed ■ Input check ■ Output check
2	Bus out check	Sets bit when a bus parity error is received during D-bus data transfer on controller inbound data.
3	Equipment check	Sets bit when error conditions such as PPC parity error, card operation not completed in specified time, or nonrecoverable PIU error are detected within the PPC or device.

4	Data check	Sets bit on incorrect parity from device, device read-check, device input check, device output-check, device not ready, or multiple punch error.
5	—	Not used; always set to zero.
6	Bus in check	Sets bit when a bus parity error is received during D-bus transfer on PPC outbound data.
7	Program alert	Set when a read image command is issued to a 96-column reader, or an out-of-range device address is presented to PPC during command sequence.
Sense Data Byte 1		
0	Device not ready	Sets bit when device is offline, power is off, interlock is open, a feature is not installed that was called for, or STOP switch was depressed.
1	Stacker full	Sets bit if the stacker is full.
2	Hopper empty	Sets bit if the hopper is empty.
3	Input check	Sets bit if the device detects misfeed or mispick condition.

I/O Sense Data Byte Definitions for 0608 Card Punch (cont)

Bit Position	Bit Designation	Definition
Sense Data Byte 1 (cont)		
4	Output check	Sets bit if the device detects an output check error.
5	Read check	Sets bit if the device detects an error at the read station.
6	Stop state	Sets bit if the device is in stop state. It may be entered by way of stop or device error.
7	Parity check	Sets bit on parity check from device.
Sense Data Byte 2		
0	Multiple punch	Sets bit if the device detects more than one hole punched in columns 1 through 7.
1	96 column card reader	Set if 96-column card reader feature is installed.

2	Invalid sequence	Sets bit if the diagnostic write enable command has not preceded other diagnostic write commands.
3	—	Not used; always set to zero.
4	Nonrecoverable PIU error	Sets bit if a nonrecoverable D-bus error occurs related to the PIU device.
5	—	Not used; always set to zero.
6	PPC RAM parity error	Sets bit if parity error occurred in the PPC during a data transfer.
7	—	Not used; always set to zero.

4.9.6.1. **Summary of I/O Sense Data Bytes for 0608 Card Punch**

Sense Data Byte	Bit 0	1	2	3	4	5	6	7
0	Command reject	Intervention required	Bus out check	Equipment check	Data check	—	Bus in check	Program alert
1	Device not ready	Stacker full	Hopper empty	Input check	Output check	Read check	Stop state	Parity check
2	Multiple punch	96-column reader	Invalid sequence	—	Nonrecoverable PIU error	—	PPC RAM parity error	—

4.9.7. I/O Sense Data Byte Definitions for UNISERVO 10 Magnetic Tape Type 0871

Bit Position	Bit Designation	Definition
		Sense Data Byte 0
0	Command reject	Sets bit when: ■ a write, a write tape mark, or erase command was attempted on a file protected tape unit; ■ a backward type command was attempted when the tape was already at load point (sense byte 0, bit 7 and sense byte 1, bit 4 are set); ■ an invalid command is transmitted to the controller (this condition is not set if a bus out check occurred on a command transfer); or ■ the tape unit incompatibility bit was set (sense byte 1, bit 7).
1	Intervention required	Sets bit when tape unit status A is inactive; i.e., a nonexistent or nonready tape unit was selected on other than a sense command (bit 1 of sense byte 1 is not set).
2	Bus out check	Sets bit when even parity appears on the BUS OUT signal for data or command transfers. During write operations, if this condition is set on a data transfer, the operation is terminated and the error byte is not written on tape.

I/O Sense Data Byte Definitions for UNISERVO 10 Magnetic Tape Type 0871 (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 0 (cont)
3	Equipment check	Sets bit when an equipment check condition occurred; i.e., bits 0, 1, or 5 of sense byte 4 have been set.
4	Data check	Sets bit when a data check condition occurred; i.e., bit 0 of sense byte 1 or bits 0, 1, 2, 3, and 4 of sense byte 3 have been set.
5	Overrun	Sets bit when service is requested on the I/O interface, but data cannot be transferred due to a late response from the channel. If this occurs on the first data transfer of a write operation, word count zero is also set in conjunction with overrun (but not set on request-tie or sense commands).
6	Bus in check	Sets bit when the controller receives the outbound control flag for parity error.

7	Program alert	Sets bit when: ■ a command was issued while the tape was rewinding (sense byte 1, bits 1 and 2 are set); or ■ a backward type command was attempted when the tape was already at load point (sense byte 0, bit 0 and sense byte 1, bit 4 are set).
Sense Data Byte 1		
0	Noise	Sets bit if: ■ During reading or read checking a block of data, a data dropout occurs (i.e., all tracks inactive) that is less than 64 frame times in length (1.6 ms at 25 ips/635 mmps). End of block is set and postamble detected is not set. ■ During erase operations, data (or noise due to tape defect) was detected on read check while the tape was being erased. ■ During a read operation, a block consisting of less than 12 bytes is detected.

I/O Sense Data Byte Definitions for UNISERVO 10 Magnetic Tape Type 0871 (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 1 (cont)
1	Tape unit status A	Available condition: 0 = nonexistent (offline) 1 = available Other condition: 0 = rewinding to interlock 1 = rewinding to load point

<table>
<tr><td>2</td><td>Tape unit status B</td><td>Indicates not ready or rewinding
<table><tr><th>Status A</th><th>Status B</th><th>Tape Drive Status</th><th>Bit Set</th></tr><tr><td>0</td><td>0</td><td>Nonexistent or offline</td><td>Unit check</td></tr><tr><td>0</td><td>1</td><td>Not ready rewinding to interlock</td><td>Unit check</td></tr><tr><td>1</td><td>0</td><td>Available</td><td>—</td></tr><tr><td>1</td><td>1</td><td>Busy, i.e., rewinding</td><td>Unit check</td></tr></table></td></tr>
<tr><td>3</td><td>7-track</td><td>Normally zero</td></tr>
<tr><td>4</td><td>Load point</td><td>Indicates tape positioned at load point</td></tr>
<tr><td>5</td><td>End of tape</td><td>Indicates tape positioned at end-of-tape area</td></tr>
</table>

I/O Sense Data Byte Definitions for UNISERVO 10 Magnetic Tape Type 0871 (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 1 (cont)
6	File protect	Indicates tape not using write enable ring
7	Tape unit incompatible	Indicates: 1. Tape unit is selected on any command requiring tape motion and any of the following conditions occur: ■ Addressed tape drive is 7-track mode but indicated PE mode. ■ Addressed tape drive is PE but indicating 7-track mode. ■ Addressed tape drive is 9-track mode and failed to reset to 1600 bpi (630 bpcm) mode (for load point only).

		2. Tape drive is selected for a read operation from load point but tape unit is 9-track mode and failed to set to 800 bpi (315 bpcm) when the tape is written in 800 bpi NRZI mode. NOTE: In case of item 1, no tape motion occurs as a result of attempted operation. In case of item 2, the condition detected after the first read operation is initiated. If a read command is to be attempted a second time, a rewind command should be executed first in order to reposition the tape. 3. GCR ID burst is detected on read operation.
Sense Data Byte 2		
0—7	Track in error	Not used; always set to zero for phase encoded (PE). Used in nonreturn zero inverted NRZI.
Sense Data Byte 3		
0	Read/write VRC/RVRC	Indicates a vertical redundancy check occurred on a data frame on a write, read, or read-backward operation.

I/O Sense Data Byte Definitions for UNISERVO 10 Magnetic Tape Type 0871 (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 3 (cont)
1	Multiple dead track check/LRC	Indicates a marginal signal occurred in more than one track on a read or read-backward operation (uncorrectable).
2	Skew	Indicates excessive skew occurs during a write, read, or read-backward operation (deskew register overflow).
3	Postamble check/CRC	Indicates postamble following the data is not read correctly or is recognized before the actual end of data (early stop sentinal).
4	Dead track check/write VRC	Indicates any of the following: ■ At least one track has a marginal signal during write or write-tape mark operations that causes sense byte 0, bit 4 to set unit check.

		■ A marginal signal is present in only one track during read or read-backward operation (correctable error). This bit is not set if a multiple track error occurs (see bit 1). If I=1 in the read command code and this bit is set, unit check will be set. If this bit is set and I=0 is in the read command, however, unit check will not set. In either case, data is correct. ■ A tape mark was not properly detected on the read check of a write-tape-mark operation.
5	Tape unit 1600 bpi	Indicates the tape drive is set for 1600 bpi (630 bpcm) mode.
6	Backward	Indicates the tape drive is set for backward tape motion.
7	—	Not used; always set to zero.
Sense Data Byte 4		
0	Runaway check	Indicates: ■ While read checking recorded data during write or write-tape-mark operations, the end-of-block mark was not detected within 12.7 milliseconds after writing was terminated. ■ During any read operation, data is not detected within 13 seconds.

I/O Sense Data Byte Definitions for UNISERVO 10 Magnetic Tape Type 0871 (cont)

Bit Position	Bit Designation	Definition
		Sense Data Byte 4 (cont)
1	Tape motion fault	Indicates: ■ Tape drive failed to respond to a start command. Tape motion may or may not have started. ■ Tape motion stopped independently of the controller during an operation requiring tape movement. This condition is detected if a backward operation is executed into load point.
2	Speed check	Indicates excessive speed variation occurred during a write operation.
3	Data bus parity error	Indicates a parity error exists on the data bus during storage read.
4	Translate error	Not used; always set to zero.
5	—	Not used; always set to zero.

6	Tape fault	Indicates end of block was detected sooner than expected during write or write-tape-mark operation. False end of block can occur if a data dropout (all tracks) is longer than 1.6 milliseconds.
7	COS parity error	Indicates a parity error occurred in the control store, read-only memory (ROM).

*These bits reflect the current state of the selected tape unit. For example, if a nonready condition is detected and the operation is aborted early, the tape-unit-available bit will be reset and the intervention-required bit will become set in sense bytes 1 and 0, respectively. Between the time that operation was aborted and the sense command was executed, if the tape drive became ready, then the sense data returned to the channel indicates that intervention is required, and tape-unit-available bits are set.

4.9.7.1. Summary of I/O Sense Data Bytes for UNISERVO 10 Magnetic Tape Type 0871

Sense Data Byte	Bit 0	1	2	3	4	5	6	7
0	Command reject	Intervention required	Bus out check	Equipment check	Data check	Overrun	Bus in check	Program alert
1	Noise	Tape unit status A	Tape unit status B	7-track	Load point	End of tape	File protect	Tape unit incompatible
2	Track in error.							
3	Read/write VRC/RVRC	Multiple dead track check/LRC	Skew	Postamble check/CRC	Dead track check/write VRC	Tape unit 1600 bpi	Backward	—
4	Runaway check	Tape motion fault	Speed check	Data bus parity error	Translate error	—	Tape fault	COS parity error

APPENDIX A. POWERS OF 2 TABLE

Powers of 2 Table

2^n	n	2^{-n}						
1	0	1.0						
2	1	0.5						
4	2	0.25						
8	3	0.125						
16	4	0.062	5					
32	5	0.031	25					
64	6	0.015	625					
128	7	0.007	812	5				
256	8	0.003	906	25				
512	9	0.001	953	125				
1 024	10	0.000	976	562	5			
2 048	11	0.000	488	281	25			
4 096	12	0.000	244	140	625			
8 192	13	0.000	122	070	312	5		
16 384	14	0.000	061	035	156	25		
32 768	15	0.000	030	517	578	125		
65 536	16	0.000	015	258	789	062	5	
131 072	17	0.000	007	629	394	531	25	
262 144	18	0.000	003	814	697	265	625	
524 288	19	0.000	001	907	348	632	812	5

Powers of 2 Table (cont)

2^n	n	2^{-n}
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5

APPENDIX B. POWERS OF 16 TABLE

Powers of 16 Table

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

These powers of 16 are especially useful in determining the value of floating-point numbers.