SPERRY UNIVAC
COMPUTER SYSTEMS

PUBLICATIONS UPDATE

90/30 System

Integrated Peripheral Channel

Programmer Reference

UP-8041 Rev. 1–A

This Library Memo announces the release and availability of Updating Package A to "SPERRY UNIVAC 90/30 System Integrated Peripheral Channel Programmer Reference", UP-8041 Rev. 1.

This update includes corrections to the table of subsystem commands and codes, the description of the print band motor control, and the print cartridge character sets.

Copies of Updating Package A are now available for requisitioning. Either the updating package alone or the complete manual with the updating package may be requisitioned by your local Sperry Univac Representative. To receive the updating package alone, order UP-8041 Rev. 1–A. To receive the complete manual, order UP-8041 Rev. 1.

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Mailing Lists BZ, CZ and MZ	Mailing Lists 75 and 76 (Package A to UP-8041 Rev. 1, 9 pages plus Memo)	Library Memo
		RELEASE DATE: January, 1980

SPERRY UNIVAC
90/30 System
Integrated Peripheral Channel

Programmer Reference

SPERRY UNIVAC
COMPUTER SYSTEMS

UP-8041 Rev. 1

SPERRY UNIVAC 90/30 System

Integrated Peripheral Channel

Programmer Reference

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1. Introduction

1.1. GENERAL

This manual contains information required to program peripheral subsystems integrated with the SPERRY UNIVAC 90/30 System (Figure 1—1) through the integrated peripheral channel (IPC). Information is centered on IPC functions to describe transfer of data and commands between the 90/30 system (processor) main storage and the integrated peripheral subsystems.

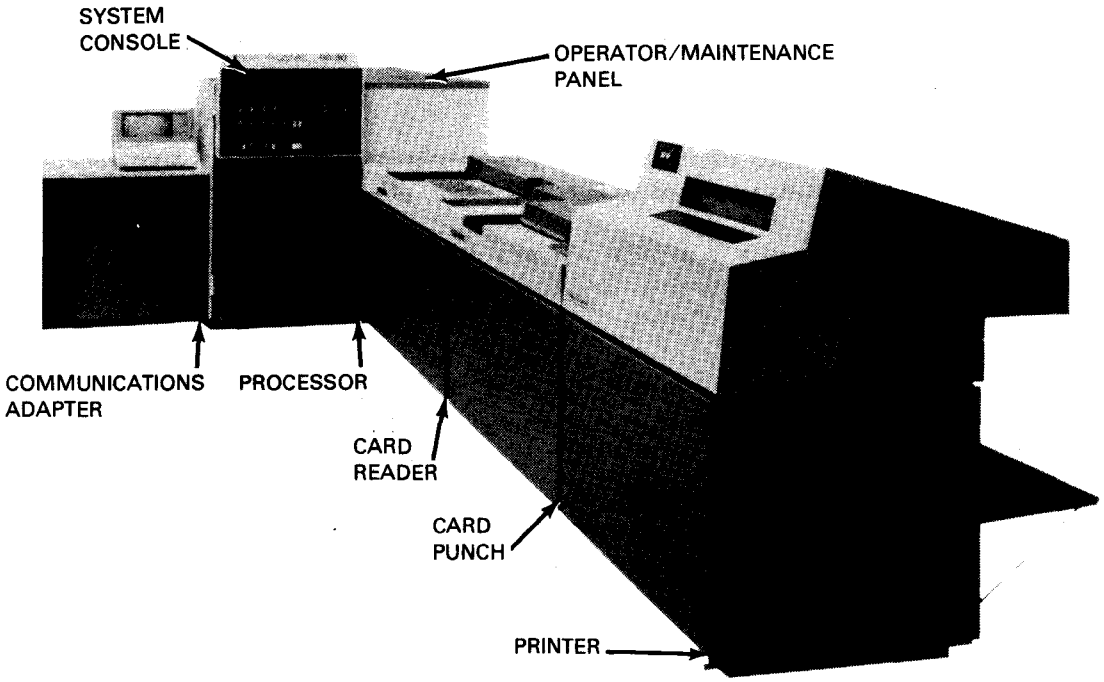


Figure 1—1. 90/30 System With Integrated Peripheral Devices

The IPC serves as a processor I/O channel that interfaces, controls, and coordinates all information transfers between processor main storage and specific peripheral subsystems integrated with the processor. These peripheral subsystems (Figure 1—1) are:

- UNISCOPE 100 Display Terminal (system console)
- SPERRY UNIVAC 0717 Card Reader Subsystem
- SPERRY UNIVAC 0605 Card Punch Subsystem
- SPERRY UNIVAC 0773 Printer Subsystem
- SPERRY UNIVAC Communications Adapter
- SPERRY UNIVAC 8413 Diskette Subsystem

Depending on the processor configuration, a diskette subsystem may or may not be included.

Control functions for each of the foregoing subsystems are developed in the IPC. The processor initiates an instruction to the IPC which results in a command transfer or information interchange between the processor main storage and a specific peripheral subsystem.

Any or all of the integrated peripheal subsystems can operate simulataneously through the processor interface, via the IPC. When simultaneous operation is required, the IPC performs time division multiplexer functions to permit multiple subsystem interfacing with the processor.

The IPC can maintain information transfers between the processor and peripheral subsystems at the rate of 50,000 bytes per second, unless precluded by interface activity of a higher priority I/O channel.

Information in Sections 4 through 9 includes separate descriptions and programming information for each integrated peripheral subsystem. Operating instructions for the same peripheral subsystems are included in current versions of the following documents:

- UNISCOPE 100 operator (reference) UP-7788, and programmer reference, UP-7807;
- 0717 card reader operator reference, UP-8089;
- 0605 card punch operator reference, UP-8088;
- 0773 printer operator reference, UP-8086; and
- 8413 diskette operator reference, UP-8490.

Additional procesor information is available in the current versions of the following documents:

- OS/3 operator handbook, UP-8072; and
- 90/30 system processor manual, UP-8052.

2. IPC Description

2.1. GENERAL

The integrated peripheral channel (IPC) is contained within the 90/30 system processor cabinet, and is powered by the processor power supplies. The IPC, which is one of the processor I/O channels, operates in half-duplex mode to transfer commands, data, status, and sense information between the processor and integrated peripheral subsystems.

2.2. CHARACTERISTICS

Basic characteristics of the IPC are listed in Table 2—1. Characteristics of each of the integrated peripheral subsystems (Figure 1—1) are listed in Sections 4 through 9, with further descriptions for each subsystem.

Table 2—1. IPC Characteristics

Parameter	Characteristic
Operating mode	Half duplex
Data transfer methods	■ Transparent (no change) ■ Translate to: — EBCDIC for processor — ASCII for peripheral device — extended card code for peripheral device
Device and buffer control word addresses	16 addresses for devices and 16 addresses for buffer control word, as follows: ■ 4 for peripheral devices ■ 12 for line adapters
Byte transfer rate	50k bytes per second
Subchannels	32

2.3. CONFIGURATION

The IPC, besides being an I/O channel of the processor, contains control logic for operating the associated integrated peripheral subsystem. Figure 2—1 illustrates the IPC configuration relationship with the processor.

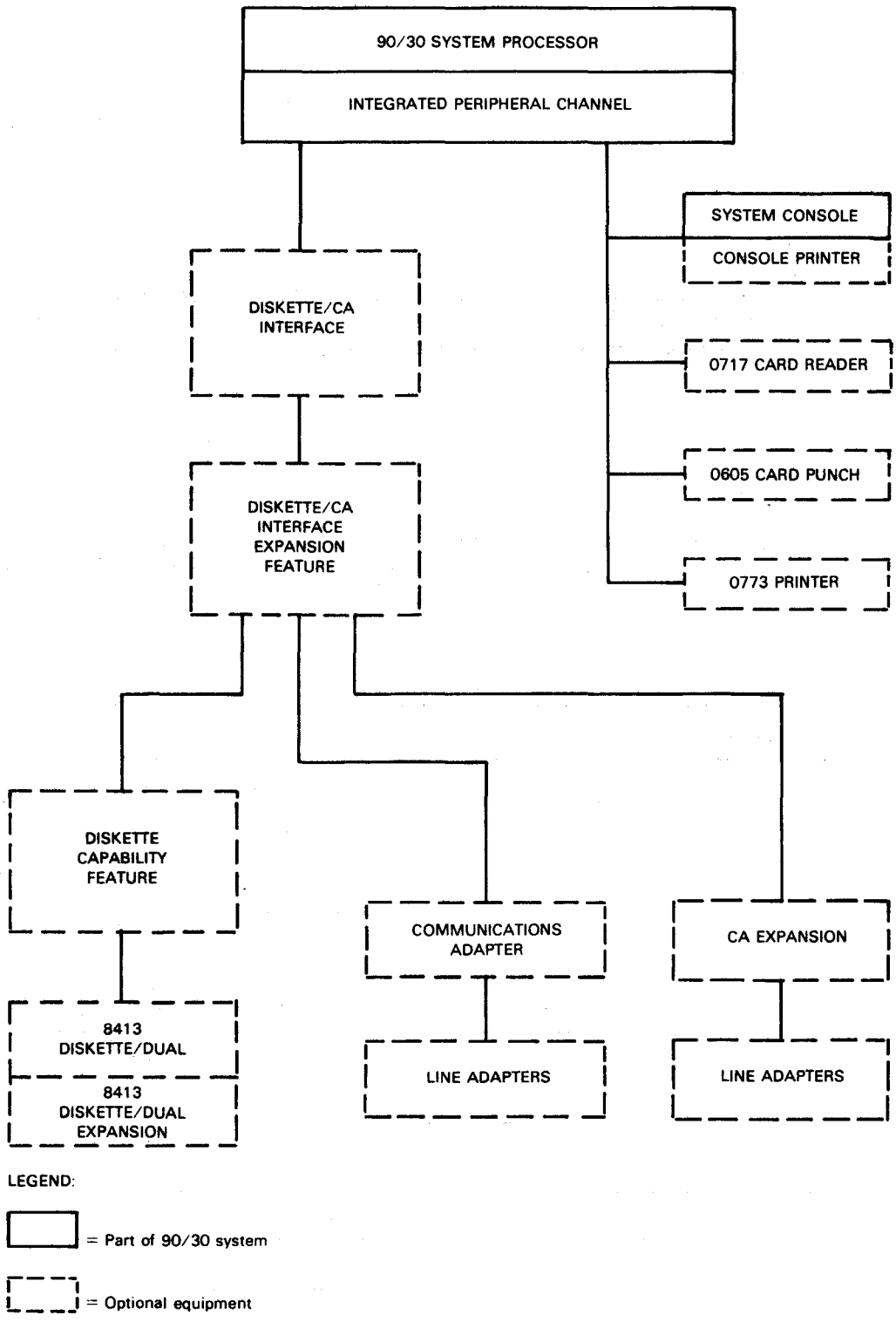


Figure 2—1. Configuration of Integrated Peripheral Devices Used With Integrated Peripheral Channel

The communications adapter feature (D/CA) is the interface to the processor, through the IPC, for diskette and communications subsystems. The D/CA interfaces the communications adapter, and provides multiplexed communications capabilities and availability of up to 12 full-duplex communications line adapters with the D/CA expansion feature.

The diskette capability feature allows up to four diskette drives for operating with flexible (floppy) diskettes that are used on industry-compatible product lines. The diskette subsystem allows the card reader and card punch to be dropped from the system for cardless operation.

Controls for each of the peripheral subsystems illustrated in Figure 2—1 are described in subsequent paragraphs.

2.4. IPC COMPONENTS

The IPC consists of printed circuit boards and logic circuits required to perform all normal I/O channel functions as well as unique control functions for the integrated peripheral subsystems. The control functions include data collection, data distribution, data buffering, storage addressing, buffer control word (BCW) maintenance, and other similar tasks. For the purpose of this description, therefore, components of the IPC are considered control sections for each integrated peripheral subsystem.

The IPC and control sections are integral parts of the processor complex. When a peripheral subsystem is attached to the appropriate control section, both the control and subsystem become part of the processor complex (Figure 2—2). All peripheral subsystems, except the system console (Figure 1—1), may be disconnected from the processor complex. The system console is required for operation of the processor.

2.4.1. IPC Subchannels

Up to 32 subchannels may be included in the IPC for operation of peripheral subsystems. A control section is included with each subchannel to control the subsystem attached to that subchannel. This is a permanent condition; therefore, references to subchannels are conceptually indistinguishable from controls.

Five subchannels (and controls) are used for integration of the system console, card reader, card punch, printer, and diskette subsystems. Low-end communications devices are accommodated with 24 subchannels (and controls) through 2 communications adapters. Six line adapters for each communications adapter, each operating in full-duplex mode, connect to the 24 subchannels for attachment of 12 communications subsystems.

The subchannels are divided into two groups: dedicated and nondedicated. Dedicated subchannels cannot be shared and are used with the card reader, card punch, printer, diskette subsystem and system console. Card punch and card reader controls are connected to a common section in addition to their own unique control sections.

Nondedicated subchannels are used with the communications adapter. In this configuration, communications devices may be selected to operate on any subchannel, depending on priority considerations.

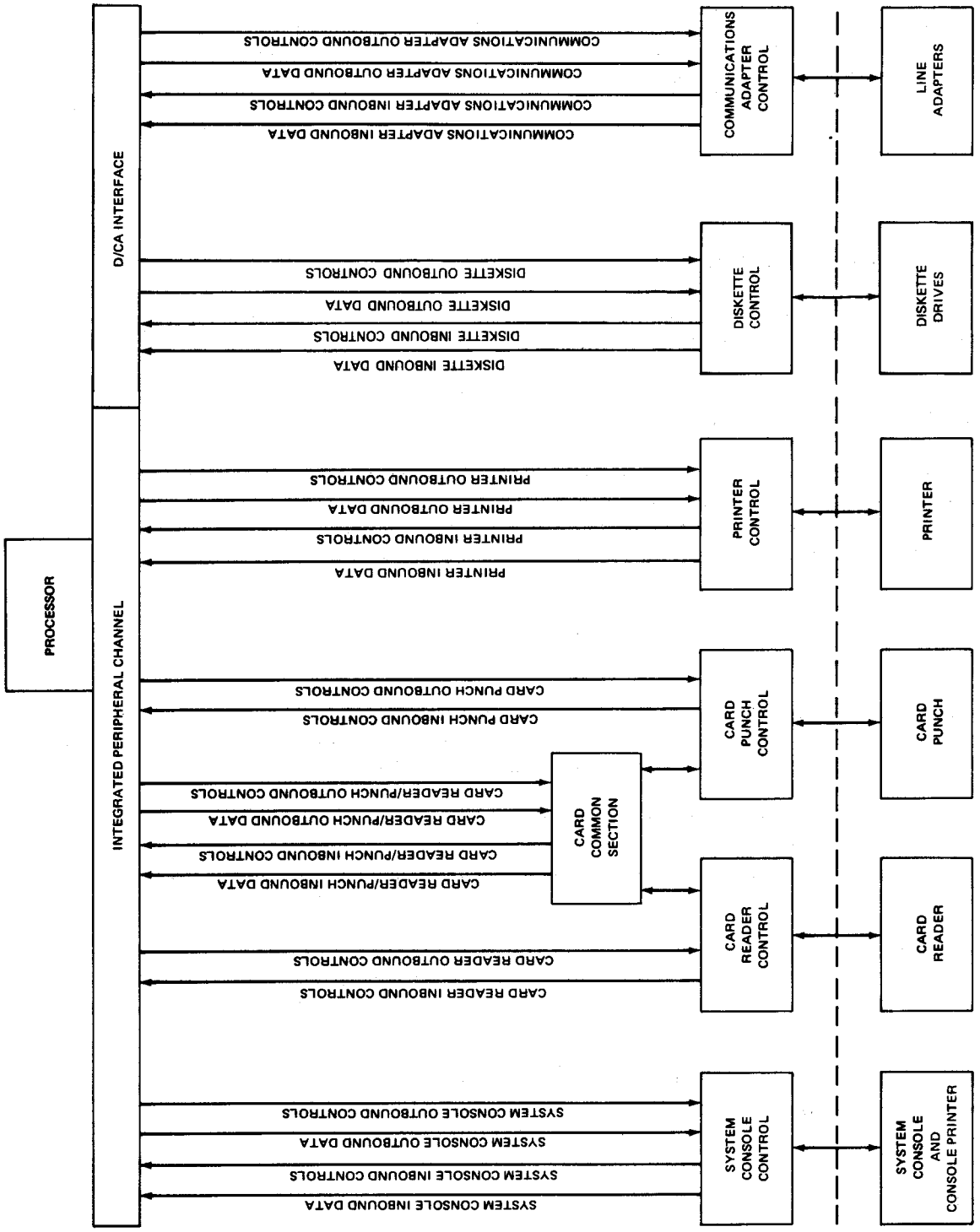


Figure 2—2. IPC Control Interface

2.4.2. System Console Control

The system console is an integral part of the processor complex and is the main interface for operating the processor system. The console control is designed to operate with the UNISCOPE 100 Display Terminal. The console is configured with an alphanumeric typewriter keyboard. Included are the uppercase protected format character generator, protected screen format and the 90/30 U—100 interface.

The system console control also can accommodate addition of the console printer, through an auxiliary interface. The console printer must be equipped with ASCII typewheel C1232—02. Additional information on the console printer is available in the UNISCOPE 100 console printer manual, UP-7939 (current version).

Functional interface between the system console and the IPC is afforded by the console control for transfer of data and status during console or console printer operations. Data decoding for formatting displays on the console, as well as data transfer to the console printer, is controlled by the auxiliary interface. Control functions normally performed by the console (i.e., cursor, editing, and text control) requiring code sequences or control data pass through the console control without interruption or change.

The ASCII code used for data in the system console is translated to EBCDIC in the console control before the data is transferred to the processor. Data from the processor (in EBCDIC) is translated back to ASCII through the console control. Read and write commands (Section 4) select the code translator.

An 8-bit path between the IPC and system console control permits command codes and data to be transferred from the IPC to the console control. Data, status, and sense information is supplied over the same path from the console control to the IPC.

A single device address is recognized by the system console control for the console and console printer. A write command transfers data from the console buffer to the console printer.

All main storage accesses, buffer control word (BCW) manipulations, input/output status tabler interrupt word (IOSTIW) presentation, and status sequences required for the system console control are performed by the IPC. Data chaining for the system console may be specified by the processor.

Additional information concerning the system console and console printer is provided in Section 4 and in the UNISCOPE 100 printer manual, UP-7939 (current version).

2.4.3. Card Reader Control

The card reader control is a functional path to the processor for the SPERRY UNIVAC 0717 Card Reader Subsystem. The card reader control, through the IPC, permits card reading operations and transfer of data and status from the card reader to the IPC. All accesses of the processor main storage, manipulations of the BCW, and presentations of the IOSTIW are performed by the IPC for operation of the card reader control.

During operation of the card reader, two 8-bit paths allow data transfers between the IPC and card reader control. Command codes originating at the processor are supplied to the reader control by the IPC over one 8-bit path. (The IPC control determines that the command is intended for the card reader control.) The second 8-bit path originates at the card reader control, and supplies data, status, or sense information for the IPC.

The card reader control uses a 12-bit data path to read or check data read in the card reader. Two 12-photocell read stations in the card reader provide data read from cards or data read that is to be checked. The card reader control selects the read station.

The processor sends a device address recognized only by the card reader control to initiate card reader operation. The card reader control uses only active BCW fields (Section 3).

Additional information concerning the card reader and card reader control is provided in Section 5.

2.4.4. Card Punch Control

The punch control is a functional path to the processor for the SPERRY UNIVAC 0605 Card Punch Subsystem. The card punch control, through the IPC, permits card punch and card read (with read feature) operations to be controlled, and data and status information to be transferred between the card punch and IPC.

Command codes and data from the IPC are supplied through the 8-bit path to the card punch control. Sense information, status, and data (when the read station feature is included) are supplied from the card punch control to the IPC over the same 8-bit data path.

The processor sends a device address recognized only by the card punch control to initiate card punch or card read operations. The IPC buffer control word (Section 3) controls all concurrent output (punch) and input (read) data transfers between the card punch and processor.

Additional information concerning the card punch and card punch control is provided in Section 6.

2.4.5. Printer Control

The printer control is a functional path from the processor for the SPERRY UNIVAC 0773 Printer Subsystem. The printer control, through the IPC, synchronizes the printer during operations for various type fonts, and permits forms advancing by program control.

The printer control contains storage buffers that store data and control signals for forms movement. Data is transferred to or from the buffers by commands initiated at the processor.

There are 256 locations for buffer storage available in the printer control for the 0773 printer. These accommodate the load code buffer (64 locations), vertical format buffer for forms movement control (48 locations), and the print line buffer for printing data (144 locations). The load code buffer can be expanded to an additional 256 locations with the expanded character set.

Processor main storage accesses, BCW manipulations, IOSTIW presentations, and status sequences required for operation of the printer control are performed by the IPC.

An 8-bit data (plus parity) path is provided between the printer control and the IPC. Command codes and data from the IPC are supplied to the printer control over the path. Sense information, status, and data from the printer control are supplied to the IPC over the same path.

The processor sends a device address recognized only by the printer control to initiate operations. The printer control uses only active fields of the IPC buffer control word (Section 3) to control operation of the printer and perform data transfers between the printer and processor.

Additional information concerning the printer control and printer is provided in Section 7.

2.4.6. Communications Adapter Control

The integrated communications adapter (CA) control includes a diskette/communications adapter (D/CA) that is required to interface the CA with the processor communications front end. Both features are combined for connecting 6 full-duplex or 12 half-duplex line adapters to the CA. An additional 6 full-duplex or 12 half-duplex line adapters may be configured by including the D/CA expansion feature.

The D/CA feature is the interface and control in the IPC that permits use of the CA. The latter controls and coordinates data transfers between the attachment and the line adapters.

A multiplexer module is included in the CA for communications line control, buffering, control character recognition, and other functions necessary for operation. Line adapters in the CA interface the modems, telegraph lines, and automatic dialers.

The CA controls communications lines, which may be private, switched network, telegraph, or other lines of common carriers in the United States and Europe. Control is maintained for line speeds of up to 56 kilobits per second.

Additional information concerning the CA is provided in Section 8.

2.4.7. Diskette Control

The diskette compatibility feature provides diskette control as a functional path to the processor for the SPERRY UNIVAC 8413 Diskette Subsystem. Each subsystem contains two diskette drives, for a total of four diskette drives available on the system. The flexible diskette control (FDC), located within the processor cabinet, engages the start-I/O, data transfer, and status sequences, which are similar to those used for the CA (2.4.6). Data, commands, and device addresses are sent from the IPC to the FDC, then to the diskette. All data is transferred in EBCDIC code.

Additional information on the FDC and diskette subsystem is presented in Section 9.

2.5. OPERATING SEQUENCES

As an I/O channel in the processor, the IPC coordinates all information transfers between the processor main storage and the pertinent integrated peripheral device control. This task requires the IPC to perform three major transfer sequences that initiate, sustain, and conclude I/O activity. The sequences are start input/output (SIO), data transfer, and status. Additional information on operating sequences is included in Sections 4 through 9 for each integrated peripheral subsystem.

2.5.1. Start I/O

When the processor presents a device address to the IPC, it issues an SIO signal to all integrated peripheral controls to initiate a start I/O sequence (Figure 2—3). The processor then issues a connect signal to the addressed control to inform the control that an SIO sequence is in progress. The SIO sequence connects the pertinent control to the IPC, fetches the command code, and generates an appropriate condition code that is returned to the processor. Connection is made when a device address is presented to the IPC when the sequence begins. The device address (Table 3—3) corresponds to one of 32 devices attached to the IPC. They are identified by a 5-bit device address code.

The connect signal is a probe to examine the state of the integrated device and its control. The CA and its associated communications peripheral are examined for presence, and any other integrated peripheral (through the IPC) is examined for presence and availability.

If the connected control is not operational, or if the integrated peripheral is not available because of pending device status or it is actively servicing a previous command, the IPC generates the appropriate condition code. This prevents the IPC from accessing a command from the processor main storage, and no information is exchanged during this sequence. The control clears the connect signal then clears the busy signal.

If the connected control is not busy and is prepared to accept a command, the IPC attempts a buffer control word (BCW) retrieval from the processor main storage by initiating the BCW with the device address, then accessing main storage. If no error occurs, the command in the BCW is issued to the pertinent peripheral control. The control interprets the command, then presents a device status byte which also contains a command acceptance or rejection indication for all remaining peripheral controls.

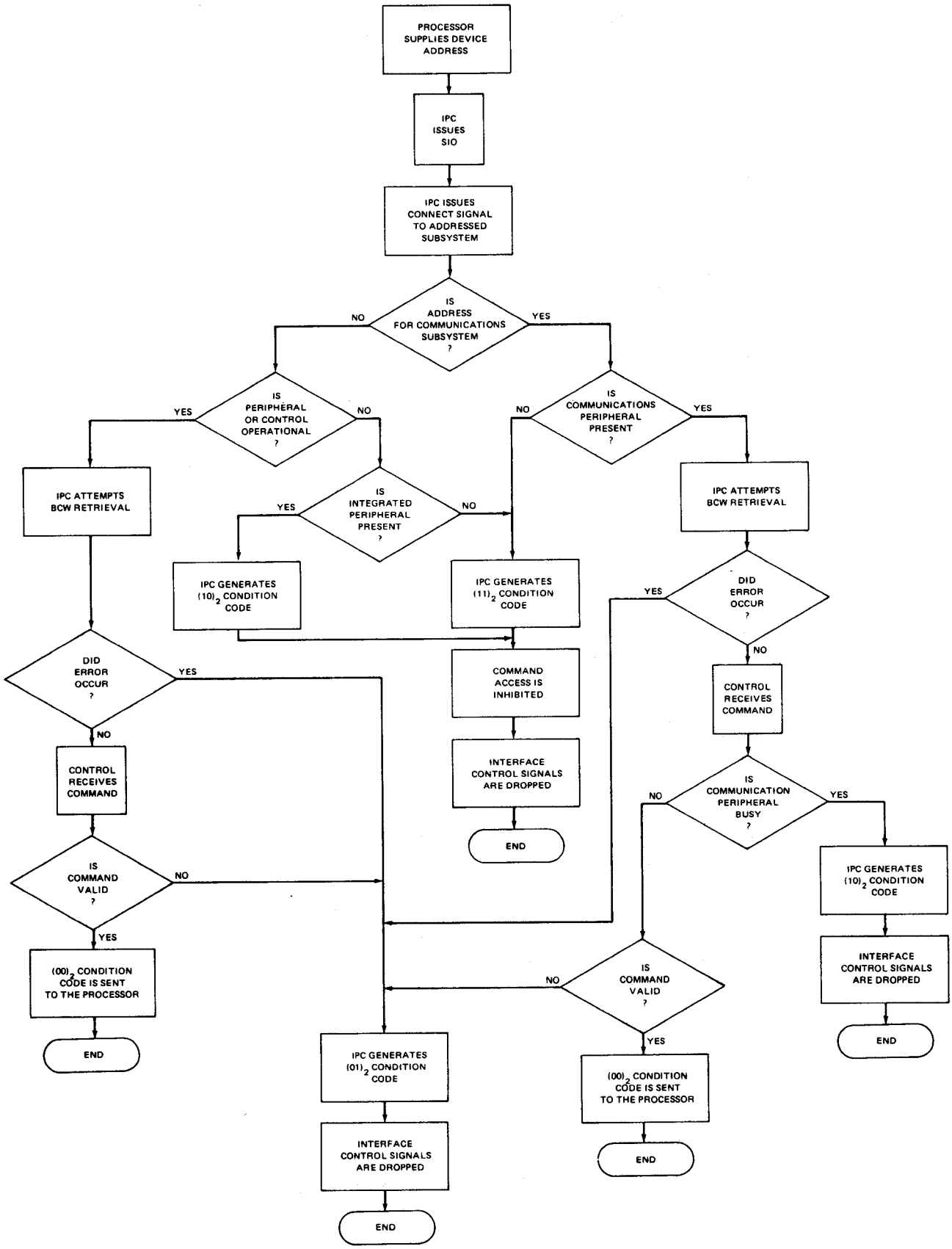


Figure 2—3. SIO Sequence

The status byte also causes the CA to present a busy indication when it is not available to receive commands. This indication is unique to the CA and must not be used by other controls associated with the IPC. The busy indication is mutually exclusive with the command rejection indication presented by must not be used by other controls associated with the IPC. The busy indication is mutually exclusive with the command rejection indication presented by controls used with the system console, card reader, card punch, printer, and diskette subsystem.

The busy indication sends a unique condition code $(10)_2$ to the processor, which prevents generation of an interrupt word (IOSTIW) upon conclusion of the SIO sequence. The command rejection indication also generates a unique condition code $(01)_2$ to the processor, and also generates an IOSTIW upon conclusion of the SIO sequence. If both the busy and command rejection indications appear, the IPC presents a nonoperational condition code $(11)_2$ to the processor. An accepted command generates still another condition code $(00)_2$, which is returned to the processor at the end of the SIO sequence. The SIO condition codes and their resulting actions are listed in Table 2—2.

Table 2—2. SIO Condition Codes

Condition Code	Peripheral Control State	Peripheral Subsystem State	Command Disposition	Interrupt Disposition	Destination of Status Byte in IOSTIW
00	Available	Run	Accepted	Stored*	Integrated peripheral**
01	Available	Stop	Rejected†	Stored*	Integrated peripheral
10††	Busy	—	Rejected	Not Stored	—
11	Not operational	—	Rejected	Not stored	—

* Interrupt word is stored in the buffer control status word (BCSW) via a status sequence after leaving the SIO sequence.

** Interrupt word normally contains device status and it is stored upon completion of the operation.

† Sense command is not rejected by the integrated peripheral control when the associated peripheral subsystem is in the stop state.

†† Addressed integrated peripheral control is also considered busy if there is a pending status condition in the subchannel or control.

The $(01)_2$ condition code can be generated for error conditions, in addition to the stop conditions listed in Table 2—2 for a particular peripheral subsystem. The code, however, always implies a command rejection and subsequent generation of an interrupt word. The IPC stores the IOSTIW after leaving the current SIO sequence. Error conditions implied by the code are as follows (subsystem state is immaterial):

$(01)_2$ Error Condition Code	Detection Source	Location of IOSTIW Status Byte
Invalid command	Peripheral control	Peripheral subsystem
Protection exception on command reference	IPC	Processor channel
Address check on command	IPC	Processor channel
Storage parity check on command reference	IPC	Processor channel
Addressing exception on command reference	IPC	Processor channel

2.5.2. Data Transfer

A data transfer sequence (Figure 2—4) is initiated when an integrated peripheral control issues a data request. After the IPC establishes priority for the control, it sends a connect signal to the control indicating that the control must participate in a data transfer sequence.

The data transfer sequence transfers data, including sense information, and parameter bytes to and from the associated peripheral control. The IPC performs both input and output sequences, where data flow is defined with respect to processor main storage. The direction of data flow and the amount of data to be transferred are defined by the control. The IPC generates the BCW address to retrieve the fields as required. The C and T bit settings in the BCW determine what action is to occur.

An input signal from the control indicates that data is to flow from the control to main storage (2.5.2.1). Absence of the input signal indicates data is to flow from main storage to the control (2.5.2.2).

The IPC transfers one, two, or four data bytes during one data transfer sequence. These transfers are defined as byte, half-word, and word-transfer sequences. Presence of a TAKE-2 signal indicates that two data bytes (a half word) are to be transferred during an input or output sequence. A TAKE-4 signal indicates that four bytes (a full word) are to be transferred during an output sequence. Absence of either signal indicates that a single-byte transfer is to take place. The direction of flow and the amount of data transfer that can be made during each transfer sequence for each integrated peripheral subsystem are listed in Table 2—3.

Table 2—3. Data Transfer Direction and Quantity per Sequence

Integrated Peripheral	Input			Output		
	Byte	Half Word	Full Word	Byte	Half Word	Full Word
System console	X	—	—	X	—	—
Card reader	X	X	—	—	—	—
Printer	—	X	—	—	X	—
Diskette	X	—	X	X	—	X
Card punch:						
Without read	—	X	—	—	X	X
With read	X	X	—	—	X	X
Communications adapter	X	—	—	X	—	—

Upon establishing a connection with the required peripheral control, the IPC generates a buffer control word (BCW) address, and retrieves the required bytes. All controlling parameters of the IPC BCW, and information supplied by the control, are retained by the IPC during the entire transfer sequence. The IPC updates the main storage address upon completion of a transfer.

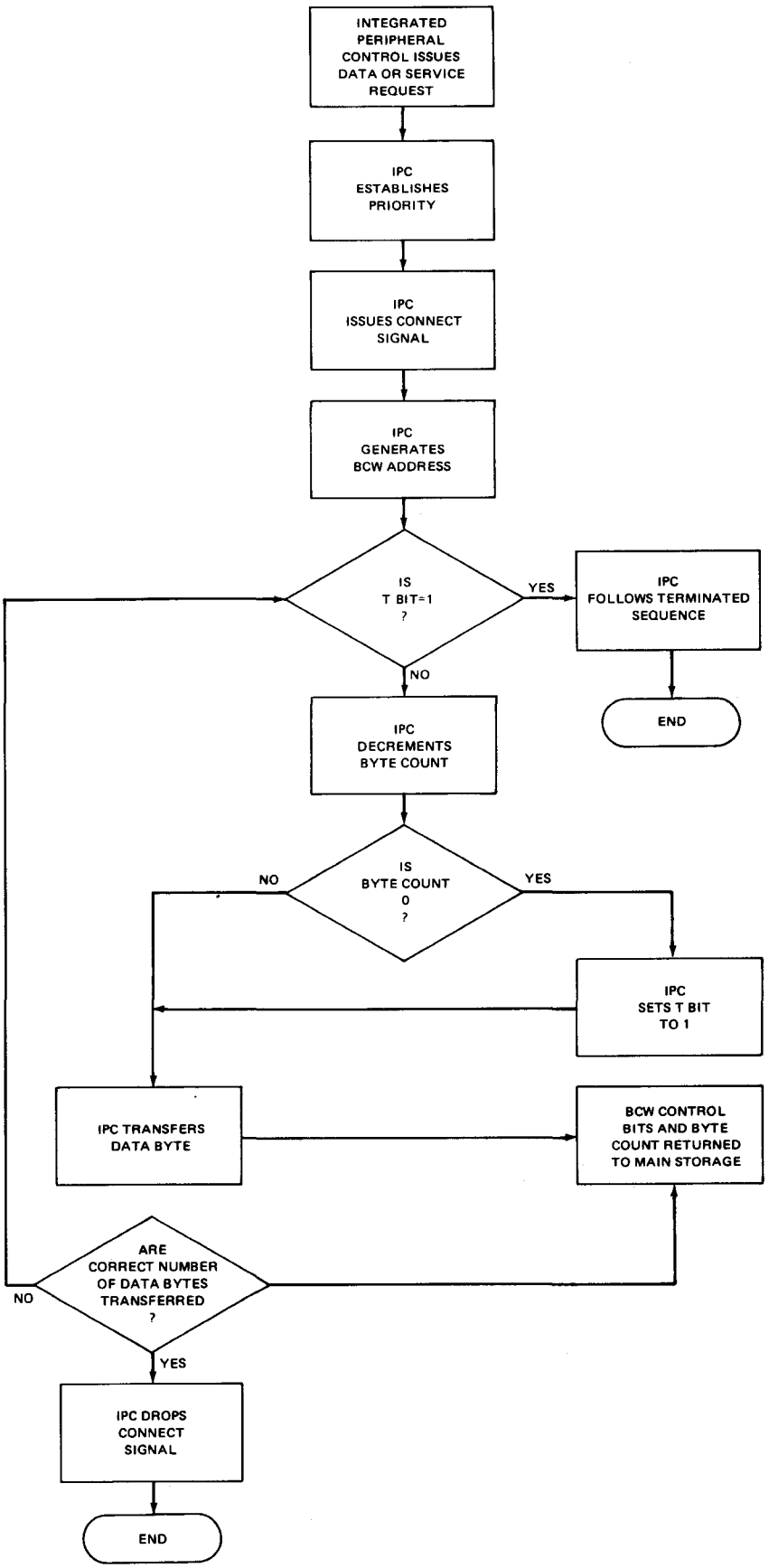


Figure 2—4. Data Transfer Sequence

The IPC responds to all data requests in one of two ways: it performs the data transfer operation, or it terminates the peripheral control. The C and T bit settings of the BCW, or any detected error conditions, determine which course subsequent action is to take.

If a data transfer is to take place, the IPC decrements the byte count and examines the count after each decrement. If the count reaches zero after a single decrement cycle, the IPC sets the T bit to 1 for a normal termination setting and the current data request is honored. All control bits in the BCW and the modified byte count are returned to main storage after decrementing is complete.

The IPC now retrieves main storage BCW information requiring two main storage accesses. The IPC performs the actual data transfer when all addressing is assembled. The new address field is then restored in the BCW.

Note that the restoration cycle normally requires one main storage cycle. Sometimes, however, the address update causes a carry bit to propagate across the half-word boundary of the address field, and requires an additional main storage cycle. At worst, the additional main storage access can occur only during one data transfer sequence for a given command.

Errors that may occur during a data transfer sequence include: storage parity checks, address checks, protection exceptions, and addressing exceptions. An error in any main storage reference associated with a data transfer sequence results in an I/O interrupt. An interrupt word (IOSTIW) is stored by the IPC, which notifies the control that an error has been detected by the channel. This causes the control to suspend further data requests.

After an error, the control may present status, depending on the type of error condition. If the error occurred during actual data fetch/storage operation, the IPC attempts to restore the updated BCW. However, if errors occur during BCW restoration, the resultant BCW state is indeterminate.

2.5.2.1. Input Transfer Sequence

When all addressing information is assembled, the IPC transfers the first data byte in the half word from the peripheral control or in the full word from the FDC (Figure 2—5). The IPC samples the first byte to determine that it is valid, then issues the first INPUT BYTE ACKNOWLEDGE signal. The control then clears the input data bus and SERVICE REQUEST signals, and the IPC waits for the second SERVICE REQUEST signal from the control. The second SERVICE REQUEST signal does not require new priority, but merely indicates that the second byte is present on the input data bus.

A very small delay (4 microseconds) occurs between the first INPUT BYTE ACKNOWLEDGE signal and the second SERVICE REQUEST signal. The second data byte is sampled by the IPC before it assembles the half word (two bytes) and transfers it to the processor main storage.

After the input transfer sequence is successfully completed, the IPC issues a second INPUT BYTE ACKNOWLEDGE signal to the control. The control then clears the interface, and the IPC simultaneously clears the connect and second INPUT BYTE ACKNOWLEDGE signals. The IPC now updates the main storage address.

A 1-byte transfer from a peripheral subsystem begins after the initial exchange of priority and direction of information. The IPC accepts the byte, which must be validated after a signal. Subsequent data transfer sequences are the same as a full-word or half-word transfer, except only a single-byte transfer is made.

For all data transfers, data from the system console, card reader, and card punch is presented without parity. Data from the printer and diskette subsystem is presented with odd parity. The IPC does not check parity of the FDC.

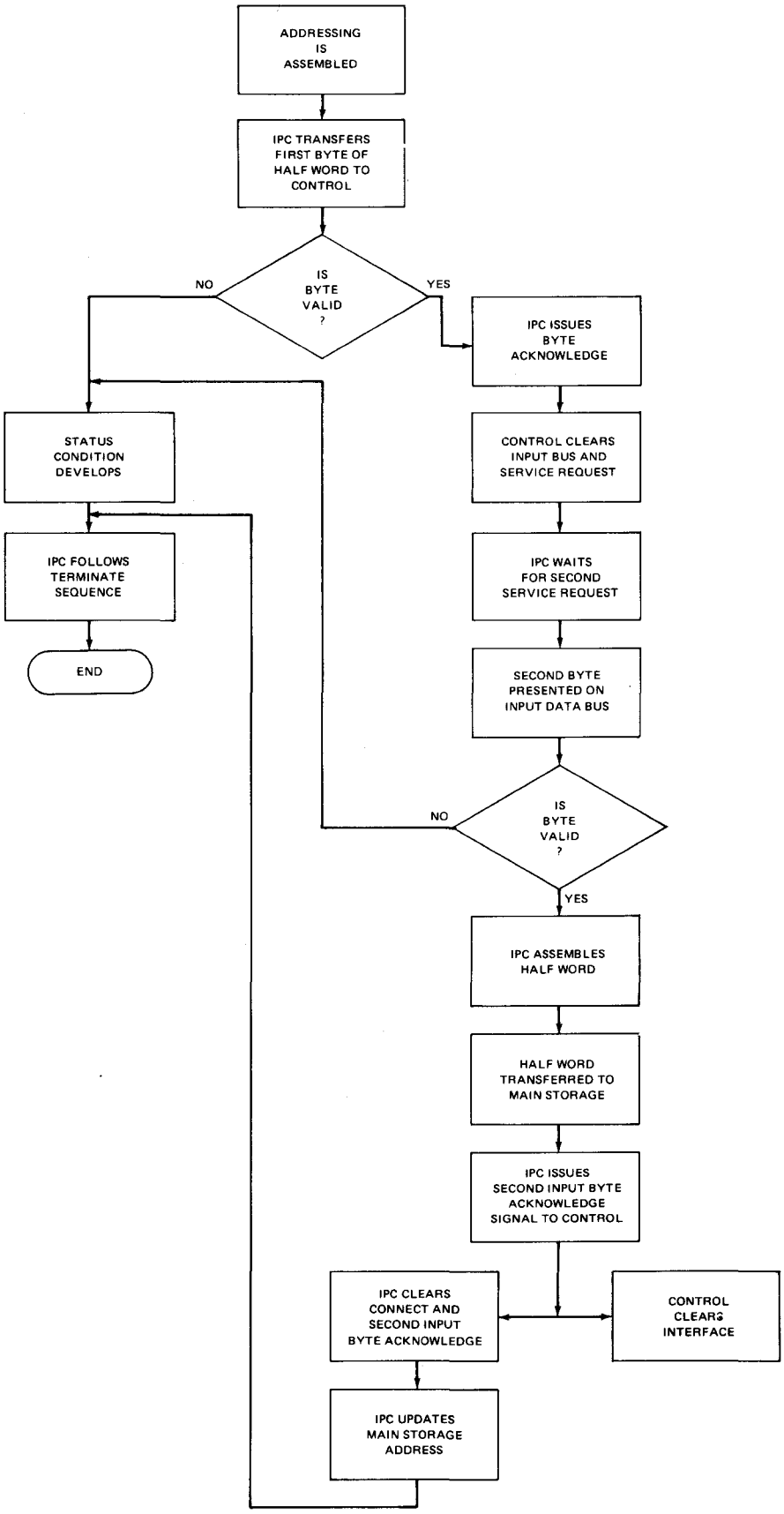


Figure 2—5. Half-Word Transfer to Main Storage

2.5.2.2. Output Transfer Sequence

An output sequence is defined by absence of the input signal in a data request from an integrated peripheral control. The IPC responds to the particular control with a connect signal and control responds with a TAKE-2 or TAKE-4 signal. A TAKE-2 signal indicates a half-word transfer (two bytes), and a TAKE-4 signal indicates a full-word transfer (four bytes). Absence of both these signals indicates a single-byte transfer. All lines must be valid before a transfer can take place.

In a half-word transfer, the IPC accesses the required half word after initial exchange of priority and direction information. The first byte with odd parity is presented on the output data bus, and the IPC indicates its validity by issuing a DATA AVAILABLE signal, which causes the control to clear its SERVICE REQUEST signal.

The IPC now waits (less than a microsecond) for the control to reactivate the SERVICE REQUEST signal and indicate that the control is ready for the second byte. The IPC then presents the second data byte and issues another DATA AVAILABLE signal. The control then clears the second SERVICE REQUEST and TAKE-2 signals, while the IPC is simultaneously clearing the connect and second DATA AVAILABLE signals.

In a full-word data transfer, the basic priority and information exchanges are as for the half-word data transfer. Each data byte with odd parity is presented to the control with a DATA AVAILABLE signal. After each DATA AVAILABLE signal, the control clears the current SERVICE REQUEST signal and reissues a new SERVICE REQUEST signal when it is ready to accept another byte. The final DATA AVAILABLE signal causes the control to clear its SERVICE REQUEST and TAKE-4 signals. The IPC simultaneously clears the connect and fourth DATA AVAILABLE signals.

A 1-byte transfer to a peripheral subsystem begins after an initial exchange of priority and direction information. The IPC accesses the required data byte, and the byte with odd parity is presented on the output data bus. The IPC indicates its validity by issuing a DATA AVAILABLE signal, which causes the control to clear its service request line. The IPC then clears the connect and DATA AVAILABLE signals.

2.5.2.3. Terminate Sequences

The IPC updates the main storage address after a data transfer operation is complete, and the new address is restored in the BCW. The restoration cycle normally requires only one main storage cycle; however, when the address update causes a carry bit to propagate across the half-word boundary of the address field, an additional cycle is required. The additional main storage access can occur only during one data transfer sequence for a given command (3.2).

For an input terminate sequence, the IPC sustitutes the TERMINATE signal for the last input byte ACKNOWLEDGE signal. The TERMINATE signal can occur at any time during an appropriate data transfer sequence.

Termination of data transfer occurs when the IPC detects any of the following conditions:

- The terminate bit (34=1) and chaining bit (32=0) of the appropriate BCW specify termination.
- The terminate bit (50) when chaining due to terminate bit (34) and chaining bit (32) being set.
- A buffer wraparound error condition occurs, which is indicated if the F bit (64) of the BCW is a zero when chaining is attempted due to terminate bit (34) and chaining bit (32) being set.
- A channel status condition develops during the current sequence.

Some data loss may occur as a result of the terminate sequence. The peripheral control clears the interface with a TERMINATE signal in the same manner used to clear the input byte ACKNOWLEDGE signal. With a TERMINATE signal, the associated control is required to terminate the current command.

An output terminate sequence requires the same conditions as an input terminate sequence. Because the termination occurs at any time during the sequence, data may or may not be transferred.

2.5.2.4. Errors During Transfer

Various errors, including storage parity checks, address checks, protection exceptions, and addressing exceptions, can occur during a data transfer sequence. If an error is detected in any main storage reference associated with a data transfer sequence, an I/O interrupt results (3.5).

When an error is detected by the channel, the IPC notifies the associated control that an error has occurred, which causes the control to suspend further data requests. The control may then present status (2.5.3), depending on the type of error condition.

The IPC attempts to restore the updated BCW if an error occurred during the actual data fetch or storage operation. If, however, an error occurs during BCW restoration, the resultant BCW state depends on the status condition (2.5.3).

2.5.2.5. Data Chaining Sequence

The data chaining sequence (Figure 2—6) presents a special condition during data transfer, and is used only with sequences for the diskette subsystem, communications adapter, or the system console. Normal data transfer sequences (2.5.2 through 2.5.2.4) are followed if data chaining is specified with a 1 in the C bit of the BCW, provided the active buffer byte count has not decremented to zero.

When the active (A) fields of the BCW (3.4) are depleted, the C and T bits equal 1, and the IPC uses the replacement (R) fields for current data transfer. The IPC, however, tests the flag (F) bit at the BCW before the replacement fields can be accessed.

If the F bit equals 1, the IPC completes the data transfer under control of the R fields. Subsequently, these R fields are updated and stored in the corresponding active (A) fields of the BCW. The IPC sets the F bit of the BCW to 0 if the replacement operation is completed successfully.

The IPC stores the IOSTIW (for buffer termination) only if the C bit in the R field equals 1. This interrupt notifies the software that new replacement fields are required for the data chaining sequence.

If the F bit equals zero when replacement fields are required, the IPC does not perform a data transfer. The IPC assumes that software did not establish new control parameters; therefore, the IPC terminates the control and sets the C bit in the active fields to 0 for the associated peripheral control. This is, effectively, a buffer wraparound error condition (2.5.2.3), which suspends activity between the IPC and the associated control.

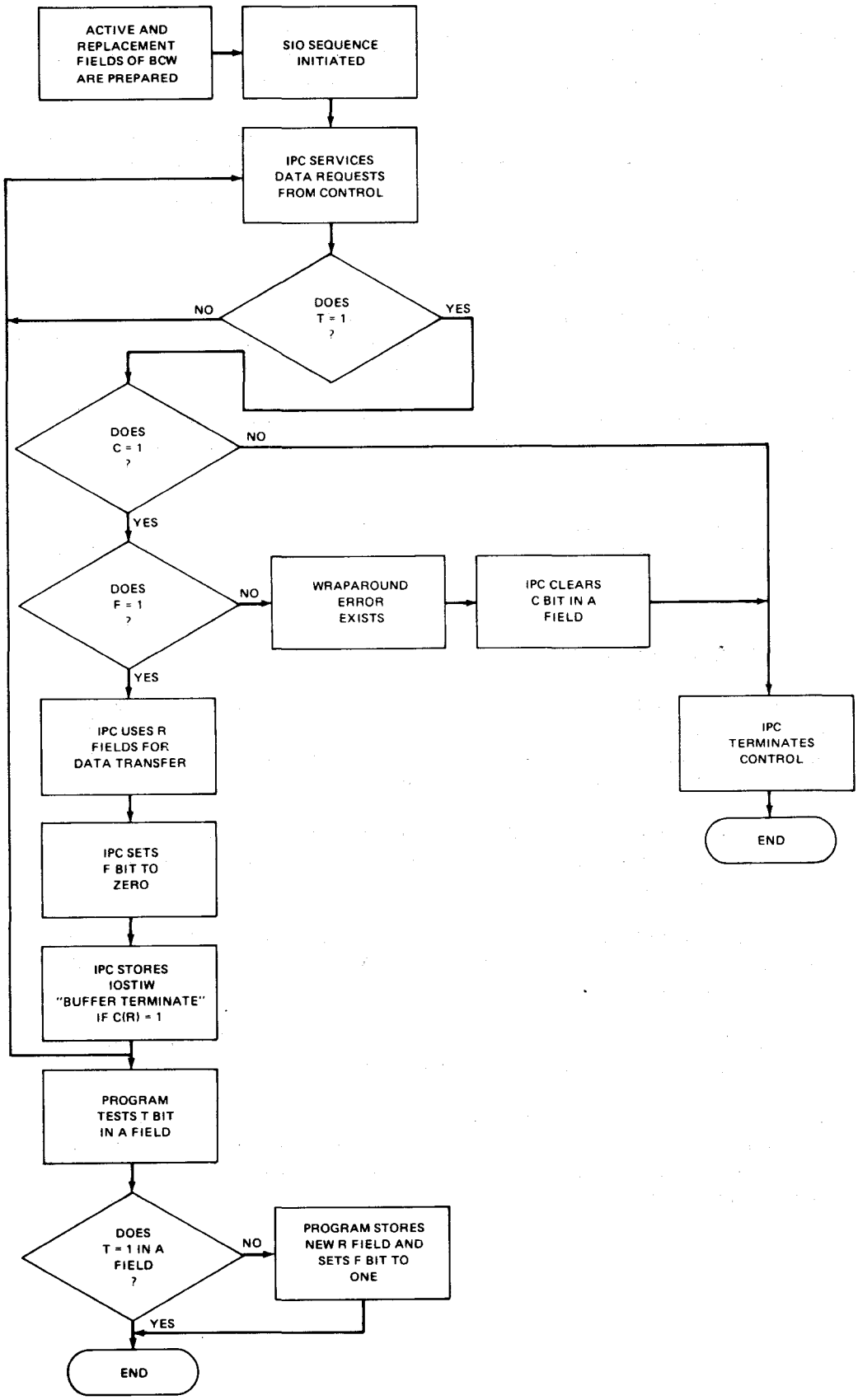


Figure 2—6. Data Chaining Sequence

2.5.3. Channel and Device Status

The IPC presents channel and device status with an interrupt word (IOSTIW). Channel status is stacked by the subsystem control. Each presents its status byte to the input/output status tabler (IOST) by separate status sequences.

The status sequence is entered in response to a status request from a peripheral control or the IPC. A number of reasons may cause a control to request status, depending on the function of the control design. Generally, status requests are generated to indicate completion of a command execution, error conditions, or any unusual condition.

The IPC generates a status request when channel status develops during an SIO or data transfer sequence. The IPC and its associated controls stack status and present the status byte in the form of an IOSTIW to the IOST as a result of the status sequence.

When a status request is received, the IPC acknowledges the signal by raising a connect signal to that control. Subsequent operation is similar to the input transfer sequence (2.5.2.1), except that the specific control must participate in a status sequence instead of a data transfer sequence. The IPC issues the input byte ACKNOWLEDGE signal during all status sequences. Signals are cleared in the same manner as for an input transfer sequence. Although the IPC generates an odd parity for all status bytes, it does not check the parity.

The IOSTIW is stored in the first four bytes of the buffered channel status word (BCSW) in fixed locations of low-order main storage (OEO_{16} through $OE3_{16}$). The IOST in the processor provides control for IPC storage of the IOSTIW. Status generated by the FDC, however, is stored in the device status field of the IOSTIW.

If an error occurs when storing the IOSTIW, the IPC generates a buffered channel status word service error (BCSWSE) indication to the IOST. The IPC attempts to store both half words of its IOSTIW in this condition, but either or both half words may be in an indeterminate state. Thus, the IOSTIW state depends on whether an error exists and when it occurred. The IPC does not generate another IOSTIW to compensate for the IOSTIW encountering the error condition.

If an error occurs when storing a buffer terminate during a buffer terminate interrupt, eventual depletion of the byte count to zero terminates the control because the flag (F) bit of the associated BCW equals zero (3.4). The IPC then generates a BCSWSE, as previously described.

2.5.3.1. Channel Status Registers in IPC

Two identical registers are located in the IPC which hold the I/O channel status until the status is stored into an IOSTIW. Each register comprises a device (subchannel) address field and channel status field.

Two separate subchannel status conditions can be staked simultaneously by the IPC in the channel status registers. If either register contains pending status, the IPC does not accept the SIO instructions. Instead, with this condition, the IPC presents a 10_2 condition code (Table 2—2) in response to an SIO instruction.

The IPC honors an SIO instruction as soon as the register contents are stored as an IOSTIW. When one register is holding status, a pending status condition exists which represents a channel-busy state with all subchannels busy. If both registers contain pending status, the IPC does not honor data transfer requests and rejects SIO instructions.

Pending status in both registers may result in secondary error conditions (e.g., an overrun) in integrated peripheral controls waiting for data service. This is a locked-out condition, from which the IPC normally recovers when pending status conditions are relieved.

2.6. PRIORITIES FOR SEQUENCES AND CONTROLS

All IPC operations are derived from two priority networks and certain interface control lines. One priority network determines the operating sequence (start I/O, data transfer, or status) that is to be performed, and the second priority network determines the peripheral control where the operating sequence is to be performed.

2.6.1. Sequence Priorities

The sequence priority network determines the sequence that the IPC should enter. The network receives inputs from the SIO line from the processor, and the status service request and service request lines from the integrated peripheral controls. These lines result in SIO, status, and data transfer sequences, respectively.

Timing for operating sequences of the IPC originates from an internal sequence counter that is driven by a clock in the processor. Unique starting points are provided for each of three sequences: start I/O (2.5.1), data transfer (2.5.2), and status (2.5.3).

Each sequence is entered in response to certain requests from the processor or peripheral controls. When a single request is presented, it is honored on a first-come, first-served basis. When multiple requests are made, the priority network determines which sequence receives priority.

Sequences are normally executed with the following order of priorities:

1. Status sequence
2. Data transfer sequence
3. Start I/O sequence

The status sequence always receives the highest priority. However, when data transfer and start I/O requests are received simultaneously, the start I/O sequence is not deferred by more than one data transfer sequence.

2.6.2. Controls Priorities

The controls priorities network resolves conflicts when servicing integrated peripheral controls during status, sense, and data transfer sequences. This network determines which control is granted priority for either of the sequences.

Inputs to the controls priorities network are the service request and status request control lines. Outputs from the network are gated to form connect signals to respective peripheral controls. Control priority for the diskette subsystem and communication adapter are identical because the same path is taken for all transfers for these systems.

Control priority depends on the type of sequence in progress. The priority for each integrated peripheral device in the status, sense, and data transfer sequence are listed in Table 2—4.

Table 2—4. Subsystem Priorities During Status and Data Transfer Sequences

Priority	Subsystem Priority in Status Sequence	Subsystem Priority in Data Transfer Sequence
1	IPC	Card punch without reading
2	Communications adapter* or diskette subsystem	Card reader
3	Card punch	Card punch read station
4	Card reader	Communications adapter or diskette subsystem
5	Printer	Printer
6	System console	System console

*With a dual communications adapter, CA1 has priority over CA2, but CA1 does not lock out CA2.

2.7. SUBSYSTEM STOP/RUN MODES

Each integrated peripheral subsystem may reside in either the run or stop state, as viewed from the subchannel or peripheral control. Status is generated when the operator changes from stop state to run state.The stop-to-run

generated status words are asynchronous and do not depend on prior initiation of any I/O operation. Run and stop states may be considered as device-online and device-offline, respectively. Thus, individual subsystems may be placed offline or unavailable for programming control.

Under certain error conditions, the stop state is automatically entered via a subsystem control. The control, however, is always available to the program except during execution of an I/O operation to its related subsystem. The integrated peripheral control cannot be switched offline by the operator in the same manner as a freestanding subsystem can be switched offline to a multiplexer or selector channel.

2.7.1. Stop Mode

A stop state occurs when all commands other than the sense command are rejected, and UNIT CHECK status is presented by the peripheral subsystem. The card reader, card punch, or printer peripheral control may enter the stop state because of operator action (pressing the STOP switch), or because of a condition in the peripheral subsystem causing automatic entry into the stop state. These conditions are described for each peripheral device in Sections 4 through 9.

The stop state causes an affected subchannel to be unavailable for system use, and access by programming is inhibited. Essentially, the peripheral device may be considered offline.

Automatic entry of an integrated card reader, card punch, printer, or diskette subsystem into the stop state is always synchronous where possible. An operation may be completed by a peripheral control, and status is presented to the IPC before the stop state becomes enabled. The unit check status bit is set with the device end bit. Finally, a sense command indicates the stop state and additional conditions which caused that state.

A unit check status with device end does not occur for the command in progress when the STOP switch is pressed by the operator to initiate a stop state. Instead, the stop state is entered after status is accepted by the IPC.

An integrated peripheral control for the card reader, card punch, printer, or diskette subsystem in a stop state (STOP indicator lit) will accept only sense commands from the IPC. All other commands are rejected and a unit check status is presented.

The system console and communications adapter do not enter stop or run mode under conditions described for the card reader, card punch, printer, or diskette subsystems. Operating conditions for entering stop or run mode for the system console and communications adapter are described in Sections 4 and 8, respectively.

2.7.2. Run Mode

A run state occurs when an integrated peripheral device is available for use in the system. An integrated peripheral control whose subsystem is in the run state (RUN indicator lit) accepts all commands supplied from the IPC, except when the following conditions are present:

- The integrated peripheral control is active because its associated subsystem is busy executing a previously issued command.
- A pending status condition exists because the control is holding status that resulted from a program or operator action.

2.7.3. Conditions Resulting From Switch/Indicator Settings

Specific subsystem states result from switch operations and indicator conditions on the integrated peripheral subsystems. These conditions are:

- RUN switch/indicator

  Pressing the RUN switch when the subsystem is in stop state (STOP indicator lit and RUN indicator extinguished) and the control is inactive initiates the following sequence:

  1. Releasing the RUN switch clears all check conditions except those requiring operator intervention (e.g., stacker full, forms low, etc.).
  2. If all check conditions are cleared, the RUN indicator is lit and the STOP indicator is extinguished.
  3. The attention status is generated, which notifies the program that the control is ready to accept commands.

  No action from the control is initiated if the RUN switch is pressed and released while the subsystem is in the run state.

  If the subsystem is in the stop state and the RUN switch is pressed and released, but all check conditions are not cleared, the following conditions result:

  — Attention status is not generated.

  — Some of the check conditions may be cleared.

  — The subsystem remains in the stop state.

  When the RUN indicator is lit, the STOP indicator is extinguished and the subsystem with its associated control is in the run state.

- SYSTEM RESET switch

  Pressing the SYSTEM RESET switch, issuing a DIAG system reset instruction, or initiating a power-on sequence causes an integrated peripheral subsystem to enter or to be initially placed in the run state.

  Releasing the SYSTEM RESET switch causes the integrated peripheral subsystem to remain in the run state unless outstanding check conditions are present. The subsystem remains in the stop state in the presence of check conditions, and no status is generated due to the effect of the reset.

- STOP switch/indicator

  Pressing the STOP switch when an integrated peripheral subsystem is in the run state places the subsystem and its associated control in the stop state as long as it is not executing a command or holding pending status. The RUN indicator is extinguished.

  Pressing and holding the STOP switch while the subsystem is in the stop state provides a lamp test by lighting all the indicators on the subsystem operator panel.

- DEVICE CHECK indicator

  A lit DEVICE CHECK indicator informs the operator that error conditions occurred which set the device check sense bit. These conditions are unique with each subsystem. A DEVICE CHECK indicator is provided for each subsystem on the system operator/maintenance panel.

  An early warning temperature condition detected in a subsystem also causes the DEVICE CHECK indicator to light. The integrated peripheral control does not take action with this detection, except that an indication of the condition is presented to the processor.

No operator controls are included on the diskette subsystem. Therefore, the above conditions do not apply for that subsystem. All operations are controlled by system programming and by the FDC.

3. Programming

3.1. GENERAL

This section provides information for programming the integrated peripheral channel (IPC) with the 90/30 system processor. Codes and word structures are presented, with definitions for each word and code. Additional information for programming each integrated peripheral subsystem is presented in Sections 4 through 9.

3.2. INFORMATION CODES

Information codes are contained in data transfer codes, command codes, status codes, and sense codes. Each type of code is discussed in subsequent paragraphs.

3.2.1. Data Transfer Codes

The IPC is transparent to all command, data, sense, and status information. However, the integrated system console, card reader, and card punch controls require data code conversion, which is accomplished by translators in each control. The translator types and the controls using them are listed in Table 3—1. The card punch shares its translators with the card reader on a time-sharing basis. The printer and diskette subsystem operate with EBCDIC code and, therefore, do not require translations.

Table 3—1. Code Translator for Integrated Controls

Code Translator	Integrated Peripheral Control
EBCDIC to ASCII	All individual controls
ASCII to EBCDIC	All individual controls
EBCDIC to extended card code	All individual controls
Extended card code to EBCDIC	Card reader and card punch

Transparent data transfers are made with no alteration of information bytes, and the type of code is determined by the user. Operations with translated data, however, require conversion from the source to the destination code, and are translated by the 90/30 system translators. All translated data that is to be transferred through main storage is first converted to EBCDIC. Data sent to integrated controls is converted to ASCII or extended card code if translation is required (Table 3—1).

Each integrated control has specific buffering capabilities that vary with device needs and characteristics. This requires the IPC to send or receive a variable amount of data during a given transfer sequence. Table 3—2 lists the requirements for each control in each data transfer sequence. Listed are:

- the number of main storage accesses typically required for data transfer squences;
- direction of data flow;
- allowed data codes; and
- amount of data transferred during the sequence.

The processor data direction column in Table 3—2 defines the direction of data flow with respect to main storage. The data transferred per sequence column defines the amount of data transferred for one data transfer sequence.

Table 3–2. Transfer Requirements for Integrated Controls

Integrated Subsystem Control	Main Storage Accesses*			Processor Data Direction	Data Code	Data Transferred per Sequence
	a	b	c			
Printer	6	1	–	Output	Transparent	Half word
	6	1	–	Input	Transparent	Half word
Card reader:						
Sense command and image mode	6	1	–	Input	Transparent	Half word
Translate mode	6	1	–	Input	Extended card code	Byte
Card punch:						
Image mode	7	1	–	Output	Transparent	Word
Translate mode	6	1	–	Output	Extended card code	Half word
Sense command	6	1	–	Input	Transparent	Half word
Card punch (read station):						
Sense command and read, image mode	6	1	–	Input	Transparent	Half word
Read, translate mode	6	1	–	Input	Extended card code	Byte
System console	6	1	3	Output	ASCII	Byte
	6	1	3	Input	ASCII	Byte
Communications adapter	6	1	3	Output	Transparent	Byte
	6	1	3	Input	Transparent	Byte
Diskette subsystem	7	1	3	Output	Transparent	Word
	7	1	3	Input	Transparent	Word
	6	1	3	Output	Transparent	Byte
	6	1	3	Input	Transparent	Byte

*The number of main storage accesses required for each data transfer sequence is as follows:

a = typical number of access cycles

b = additional cycles that may be required during BCW update (only once during the command)

c = additional cycles required for BCW replacement operation during a chaining sequence

3.2.2. Command Codes

The IPC transfers command codes from the processor to all integrated peripheral controls as transparent data (Table 3—2). The significance of each command code is defined for each integrated peripheral subsystem in Sections 4 through 9.

3.2.3. Status Codes

Status information concerning an integrated peripheral control is transferred to main storage by the IPC. This is transparent data for the IPC, and is transferred by the IPC to main storage under control of the I/O status tabler (IOST). The processor receives the status information as contained in the I/O status tabler interrupt word (IOSTIW) (3.5). Significance of the status fields is described for each integrated peripheral subsystem in Sections 4 through 9.

3.3. IPC ADDRESSES

The IPC is addressed by its own unique channel number 0. The integrated peripheral subsystems operating from the IPC, via their respective controls, have individual addresses assigned to them. In addition, each line adapter (LA), operating from the integrated communications adapter, has an address. Each of these, plus the buffer control word (BCW) used to store the addresses, are described in subsequent paragraphs.

3.3.1. Integrated Subsystem Addresses

The integrated peripheral controls connected to the IPC are identified by 8-bit address fields corresponding to bits 24 through 31 of the start-I/O (SIO) instruction. Bits 24 through 26 are ignored by the IPC; therefore, these bits are unassigned and must be set to 0.

Bits 27 through 31 of the SIO define one of 32 devices interfacing the IPC. Four addresses are assigned to the integrated peripheral controls, four to the diskette subsystems, and the remaining 24 addresses are assigned to two CAs each of which can accommodate up to 12 line adapters. Table 3—3 lists the integrated subsystem addresses and line adapters associated with the CAs.

3.3.2. BCW Addresses for IPC Subsystems

Each integrated peripheral subsystem address (Table 3—3) is related to a fixed location of low-order main storage. These locations are reserved for command and control parameters for the subsystem addresses.

Each subsystem address uses four BCWs labeled BCW0 through BCW3. The hexadecimal half-word storage addresses for these BCWs are listed in Table 3—4.

3.3.3. Buffered Channel Status Word Address

The buffered channel status word (BCSW) stores status of the IPC or any of its associated controls for presentation to the I/O status tabler (IOST) and entry into a status table. The IPC stores two half words of this status information into low-order main storage locations $(0E0)_{16}$ and $(0E2)_{16}$.

Table 3—3. Integrated Subsystem Addresses

Integrated Subsystem	Address (SIO Bits)							
	24	25	26	27	28	29	30	31
System console	0	0	0	0	0	0	0	0
Card reader	0	0	0	0	0	0	0	1
Printer	0	0	0	0	0	0	1	0
Card punch	0	0	0	0	0	0	1	1
Communications adapter 1:								
LA–0	0	0	0	0	0	1	0	0
LA–6	0	0	0	0	0	1	0	1
LA–1	0	0	0	0	0	1	1	0
LA–7	0	0	0	0	0	1	1	1
LA–2	0	0	0	0	1	0	0	0
LA–8	0	0	0	0	1	0	0	1
LA–3	0	0	0	0	1	0	1	0
LA–9	0	0	0	0	1	0	1	1
LA–4	0	0	0	0	1	1	0	0
LA–10	0	0	0	0	1	1	0	1
LA–5	0	0	0	0	1	1	1	0
LA–11	0	0	0	0	1	1	1	1
Diskette drive:								
0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	0	1	0	0	1	0
3	0	0	0	1	0	0	1	1
Communications adapter 2:								
LA–0	0	0	0	1	0	1	0	0
LA–6	0	0	0	1	0	1	0	1
LA–1	0	0	0	1	0	1	1	0
LA–7	0	0	0	1	0	1	1	1
LA–2	0	0	0	1	1	0	0	0
LA–8	0	0	0	1	1	0	0	1
LA–3	0	0	0	1	1	0	1	0
LA–9	0	0	0	1	1	0	1	1
LA–4	0	0	0	1	1	1	0	0
LA–10	0	0	0	1	1	1	0	1
LA–5	0	0	0	1	1	1	1	0
LA–11	0	0	0	1	1	1	1	1

Table 3—4. BCW Storage Addresses for IPC Subsystems (Part 1 of 2)

Integrated Subsystem	Hexadecimal Half-Word Storage Address Prefix			
System console	0	1	0	X_{16}
Card reader	0	1	1	X_{16}
Printer	0	1	2	X_{16}
Card punch	0	1	3	X_{16}
Communications adapter 1:				
LA–0	0	1	4	X_{16}
LA–6	0	1	5	X_{16}
LA–1	0	1	6	X_{16}
LA–7	0	1	7	X_{16}

Table 3—4. BCW Storage Addresses for IPC Subsystems (Part 2 of 2)

Integrated Subsystem	Hexadecimal Half-Word Storage Address Prefix			
Communications adapter 1 (cont):				
LA–2	0	1	8	X_{16}
LA–8	0	1	9	X_{16}
LA–3	0	1	A	X_{16}
LA–9	0	1	B	X_{16}
LA–4	0	1	C	X_{16}
LA–10	0	1	D	X_{16}
LA–5	0	1	E	X_{16}
LA–11	0	1	F	X_{16}
Diskette drive:				
0	0	3	0	X_{16}
1	0	3	1	X_{16}
2	0	3	2	X_{16}
3	0	3	3	X_{16}
Communications adapter 2:				
LA–0	0	3	4	X_{16}
LA–6	0	3	5	X_{16}
LA–1	0	3	6	X_{16}
LA–7	0	3	7	X_{16}
LA–2	0	3	8	X_{16}
LA–8	0	3	9	X_{16}
LA–3	0	3	A	X_{16}
LA–9	0	3	B	X_{16}
LA–4	0	3	C	X_{16}
LA–10	0	3	D	X_{16}
LA–5	0	3	E	X_{16}
LA–11	0	3	F	X_{16}

3.4. IPC BUFFER CONTROL WORD

The system software controls I/O activity of the IPC and the integrated peripheral subsystem controls through preparation of an appropriate BCW and initiation of an SIO instruction. The BCW contains control information required for all I/O operations, including parameters used by the IPC for main storage accesses and control of individual peripheral subsystems.

Each BCW consists of four words residing in fixed locations of low-order main storage. The command, data address, I/O storage protection key, byte count, and control information is supplied to the IPC by the BCW. The IPC accesses the BCW each time a request is received from an integrated peripheral control. Current contents of the BCW control the transfer of data. The BCW is updated by the IPC, and appropriate parameters are restored for each data transfer sequence during the I/O operation.

The BCW must be prepared by the software prior to the initiation of all I/O activity. The key, address, and count fields of any BCW must not be altered by the software until the current I/O operation is complete. However, the software may alter the command code field while an I/O operation is in progress. In addition, the software may issue commands to a control during a current I/O operation, provided the new command does not necessitate use of the BCW key, address, and count fields. BCW control flags may be altered by the software to terminate a given I/O operation. Software must be aware of the attendant risks of such actions.

The BCW consists of two sections or fields: the active (A) and replacement (R) fields. Each section comprises five information bytes, which are similar for both sections.

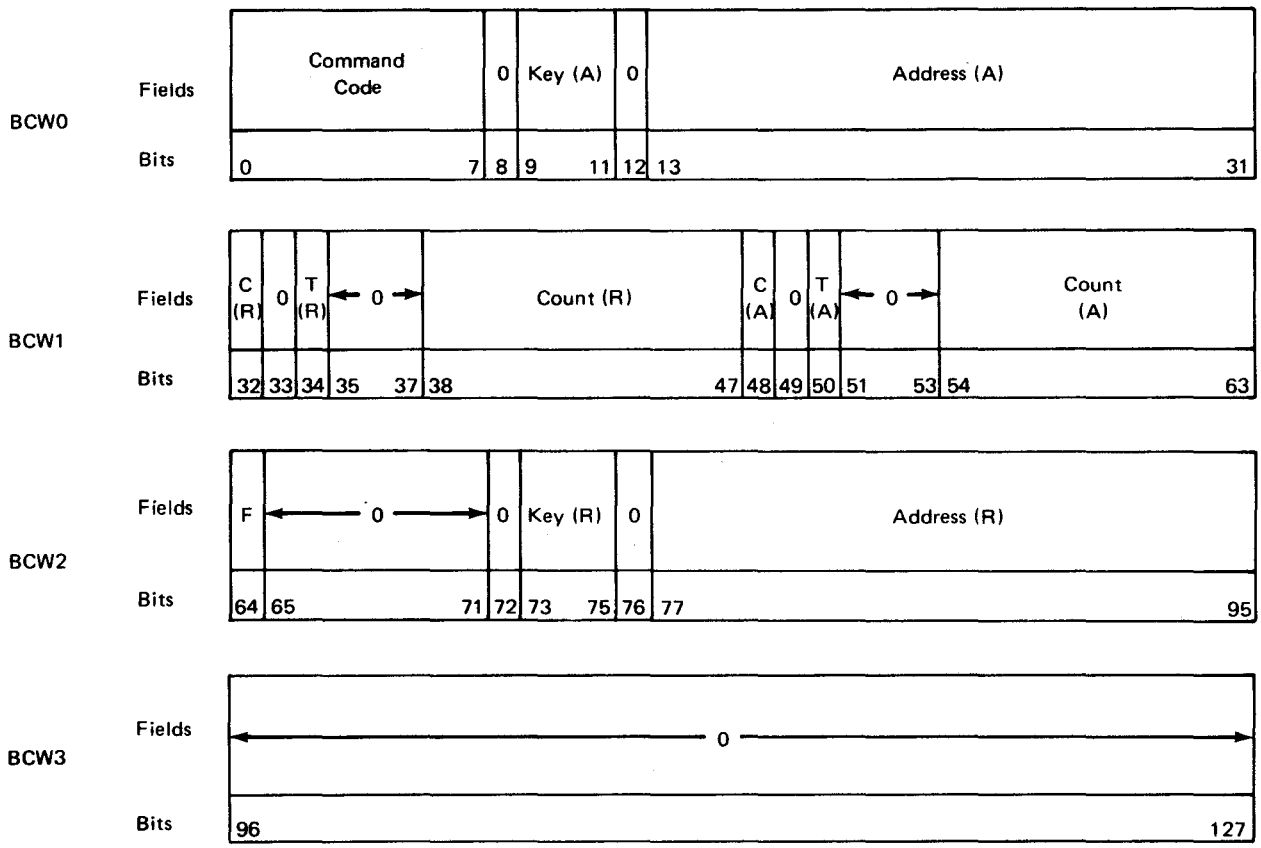
Active fields of the BCW furnish information required for control of a single data buffer area. The A field is used for all data transfers until filled or depleted. After the IPC detects that the A field count reaches 0, use of that buffer area ceases, and the IPC terminates the control during a subsequent data request or replaces the A field with the appropriate R field. If the control stops requesting data prior to termination by the IPC, the A field is not exhausted. Termination is only for operations with a single buffer. Replacement of the A field with an R field occurs during data chaining operations.

Replacement fields are used in conjunction with data chaining operations, which require assignment of two buffer areas in main storage. Replacement fields identify the second buffer area, which is automatically accessed by the IPC when data chaining is specified by software and the active buffer is filled or depleted.

The integrated card punch requires two buffer areas to implement the read and punch operations. Punch operations are controlled by parameters of the A fields, and read operations (of the card punch) utilize R fields. A data chaining operation cannot be specified for the card punch because both the A and R fields are used during normal operations.

Data chaining can be specified only for the system console and communications adapters. Data chaining is useful when the communications attachment feature is included to provide 24 additional subchannels, required by line adapters (LA), and interface for the communications adapter.

Formats of the four IPC buffer control words are illustrated in Figure 3—1. The bits of the BCW are defined in Table 3—5.



NOTE:

Refer to Table 3–5 for field definitions.

Figure 3—1. IPC Buffer Control Words

Table 3–5. IPC Buffer Control Word Fields (Part 1 of 3)

<table>
<tr><th>Field</th><th>Definition</th></tr>
<tr><td>Command code
(bits 0–7)</td><td>This field, accessed by the IPC during the start-I/O instruction, contains a command code that is sent to the addressed integrated peripheral control for interpretation and execution. The commands are described for applicable integrated peripheral subsystems in Sections 4 through 9.</td></tr>
<tr><td>Zero
(bit 8)</td><td>This bit is unassigned and must be set to 0.</td></tr>
<tr><td>Key (A) and (R)
(bits 9–11 and 73–75)</td><td>Each key is a 3-bit field containing the I/O storage protection key which is presented to the main storage interface during each data transfer sequence.

The IPC does not modify the key field during data transfer sequences. Addresses generated internally by the IPC (i.e., references to low-order main storage) are presented to the main storage interface with a key field equal to 0.</td></tr>
<tr><td>Zero
(bit 12)</td><td>This bit is unassigned and must be set to 0.</td></tr>
<tr><td>Address (A) and (R)
(bits 13–31 and 77–95)</td><td>The IPC can reference any byte in main storage during data transfer sequences with either of these 19-bit fields. The first 18 most significant bits of this field are presented by the IPC to main storage for data references. The address is updated by the IPC during each data transfer(3.3).

Data transfers are made on a byte or half-word basis. Addresses must start on the half-word boundary for all half-word transfers. The IPC accesses the half word specified by address bits 13–30 or 77–94 when a half-word transfer sequence is specified (Table 3–2).

The IPC uses the least significant bit for all byte-oriented transfer sequences. The operation for this type of operation can start on any byte boundary. During byte-oriented transfer sequences, the least significant bit has the following significance:
<table>
<tr><th>Bit 32 or 95</th><th>Significance</th></tr>
<tr><td>0</td><td>Most significant byte of the addressed half word is specified.</td></tr>
<tr><td>1</td><td>Least significant byte of the addressed half word is specified. Refer to Tables 3–6 and 3–7 for final values for A.</td></tr>
</table></td></tr>
<tr><td>Zero
(bits 33 and 35–37)</td><td>These bits are unassigned and must be set to 0.</td></tr>
<tr><td>Count
(A) and (R)
(bits 38–47 and 54–63)</td><td>This 10-bit field contains the byte count required for all data transfer operations. The IPC updates the count during each data transfer sequence. Before the actual transfer occurs, the count is decremented by 1, 2, or 4.

An initial count of 0 provides a maximum information transfer of 1024 bytes, provided T (bit 34 or 50) equals 0. The data buffer is depleted after the count decrements to 0. The count dos not wrap around. The count fields must be divisible by 1, 2, or 4, as dictated by the type of operation specified by the addressed device and command table (Table 3–2). The T bit is set to 1 by the IPC after the count reaches 0.

Count fields must be divisible by 1, 2, or 4, depending on the type of operation specified by the addressed subsystem and the command (Table 3–2).</td></tr>
</table>

Table 3–5. IPC Buffer Control Word Fields (Part 2 of 3)

<table>
<tr><th>Field</th><th colspan="3">Definition</th></tr>
<tr><td>Count
(A) and (R)
(bits 38–47 and 54–63)
(cont)</td><td colspan="3">If an odd byte count is furnished for a half-word data transfer sequence, the IPC transfers half words for each sequence. During the final sequence, a half word is transferred for a given command although a byte is specified by the count. The final half word includes one data byte and one byte containing zeros, with data on the most significance byte and zeros in the least significant byte (Tables 3–6 and 3–7).

If an odd byte count is furnished for a word data transfer sequence, the IPC transfers words for each sequence. A word is transferred during the final sequence for a given command although one, two, or three bytes were specified by the count.</td></tr>
<tr><td>C
(A) and (R)
(bits 32 and 48)</td><td colspan="3">When set to 1, this bit specifies data chaining operation. The C bit is used during data transfer sequences with the system console or communications adapter.</td></tr>
<tr><td>Zero
(bit 49)</td><td colspan="3">This bit is unassigned and must be set to 0.</td></tr>
<tr><td>T
(A) and (R)
(bits 34 and 50)</td><td colspan="3">This single control bit is used in conjunction with the C (A) bit as follows:
<table>
<tr><th colspan="2">Field</th><th>Definition</th></tr>
<tr><th>C</th><th>T</th><th>Meaning</th></tr>
<tr><td>0</td><td>0</td><td>Use (A) fields for current data transfer sequence. (This requires normal initial setting without data chaining.)</td></tr>
<tr><td>0</td><td>1</td><td>Terminate the peripheral control (normal terminate setting).</td></tr>
<tr><td>1</td><td>0</td><td>Use (A) fields for current data transfer sequence. (This requires normal initial setting for [A] and [R] fields with data chaining.)</td></tr>
<tr><td>1</td><td>1</td><td>Normally generated by the IPC during data chaining operations to indicate that (A) fields are depleted. A replacement operation is required; however, if the communications adapter or system console is assigned, and the initial setting for both C (A) and T (A) bits is 1, then one of the following conditions associated with the flag (F) bit applies:
<table>
<tr><th>If:</th><th>Then:</th></tr>
<tr><td>F=0</td><td>Terminate with buffer wraparound error.</td></tr>
<tr><td>F=1
C(R)=X
T(R)=1</td><td>Terminate in normal manner.</td></tr>
<tr><td>F=1
C(R)=0
T(R)=0</td><td>Terminate in normal manner. No data chaining is included.</td></tr>
<tr><td>F=1
C(R)=1
T(R)=0</td><td>Terminate in normal manner. Data chaining is included.</td></tr>
</table></td></tr>
</table></td></tr>
</table>

Table 3–5. IPC Buffer Control Word Fields (Part 3 of 3)

Field	Definition
T (A) and (R) (bits 34–50) (cont)	The IPC tests the T(A) bit prior to actual data transfer or updating the BCW. If T(A) equals 1, the IPC terminates the data transfer or performs a replacement operation (if specified by the C[A] and F bits). If T(A) equals 0, the IPC proceeds with the current data transfer sequence, and existing (A) parameters control the sequence. The IPC decrements the count (A) field prior to actual transfer of data. If the count decrements to zero, the IPC sets the T(A) bit to 1 and restores the entire updated BCW half word to main storage. A subsequent data request from the associated peripheral control results in either termination or replacement, as specified in software by defining the C(A) bit.
Zero (bits 51–53)	These bits are unassigned and must be set to 0.
F (bit 64)	This single control bit is used exclusively for data chaining replacement operations. The flag F bit indicates to the IPC that current contents of the (R) fields are valid for a replacement operation. Thus, when the IPC determines that a replacement operation is required (i.e., C[A] =T[A] =1), the IPC accesses and tests the F bit.
	If the F bit equals 1 when replacement is required, the IPC performs the replacement and all (R) field parameters are transferred into the appropriate (A) field positions. When the operation is complete, the IPC sets the F bit to equal 0 in main storage, which indicates that the current (R) fields are loaded into corresponding (A) fields. A buffer terminate I/O interrupt operation informs the software that the replacement operation has transpired. Software establishes new (R) parameters to continue data chaining operations. This operation is generated only when the current C(R) bit is 1. If the bit is 0 when the (R) fields are moved into the (A) fields, the buffer terminate interrupt instruction is not given. With this condition, the (A) fields are no longer in a data chaining mode; therefore, operations commence with normal data transfer and termination. When the IPC determines that a replacement is required, but the F bit equals 0 (wraparound error), the IPC does not perform the replacement operation. Instead, the IPC terminates the associated peripheral control, and sets the C(A) bit in the associated BCW to 0. The IPC does not generate an interrupt for this condition; the reset C(A) bit indicates the data chaining sequence is terminated. Software response to the buffer terminate operation is as follows: 1. Insert the next C(R), T(R), count (R), and low-order half word of address (R). 2. Test the T(A) bit. a. If T(A) equals 1, a buffer wraparound error occurred. (This is the only indication of a buffer wraparound error.) b. If T(A) equals 0, the high-order word of the address, including the key and F control bit, must be inserted within one character time of the T(A) test.
Zero (bits 65–72, 76, 96–127)	These bits are unassigned and must be set to 0.

Table 3—6. Use of BCW With IPC in Half-Word Mode

BCW Values (A)			Data Buffer Area			Zero Bytes Inserted
Initial		Final ① Address	Start I/O	End		
Address	Count			Input	Output	
2N	2M	2N+2M	2N	2N+2M–1	2N+2M–1	0
2N	2M+1	2N+2M+1	2N	2N+2M+1 ②	2N+2M ③	1
2N+1	2M	2N+2M+1	2N	2N+2M–1	2N+2M–1	0
2N+1	2M+1	2N+2M+2	2N	2N+2M+1 ②	2N+2M ③	1

NOTES:

① These values require that the final byte count (A) equals zero.

② An all-zero byte is contained in the least significant byte position of this address.

③ The last true data byte is taken from this location. The IPC inserts all-zero bytes and sends them to the peripheral subsystem.

Table 3—7. Use of BCW With IPC in Word Mode

BCW Initial Values		BCW Final Values ①	Data Buffer Area			Number of Inserted "Zero" Bytes	
			Start	End			
Address (A)	Count (A)	Address (A)	Input/ Output	Input	Output	Input	Output
2N	4M	2N+4M	2N	2N+4M–1 ②	2N+4M–1	0	0
2N	4M+1	2N+4M+1	2N	2N+4M+1 ②	2N+4M ③	1	3
2N	4M+2	2N+4M+2	2N	2N+4M+1 ②	2N+4M+1 ③	0	2
2N	4M+3	2N+4M+3	2N	2N+4M+3 ②	2N+4M+2 ③	1	1
2N+1	4M	2N+4M+1	2N	2N+4M–1 ②	2N+4M–1	0	0
2N+1	4M+1	2N+4M+2	2N	2N+4M+1 ②	2N+4M ③	1	3
2N+1	4M+2	2N+4M+3	2N	2N+4M+1 ②	2N+4M+1 ③	0	2
2N+1	4M+3	2N+4M+4	2N	2N+4M+3 ②	2N+4M+2 ③	1	1

NOTES:

① It is assumed that the final byte count (A) equals zero.

② This address contains an all-zeros byte in the least significant byte position.

③ This is the location from which the last "true" data byte is taken. Bytes containing all zeros are automatically inserted by the hardware and they are sent to the subsystem.

3.5. IOST INTERRUPT WORD

The I/O status tabler interrupt word (IOSTIW) provides the IPC with a means of presenting status of its associated peripheral subsystems and subchannels. Each peripheral control stacks its subsystem status, and the IPC stacks its channel status (2.5.3).

The IOSTIW is stored in fixed locations of low-order main storage ($0E0_{16}$ through $0E3_{16}$), in the first four bytes of the buffered channel status word (BCSW). The processor I/O status tabler (IOST) provides control for the IPC to store the IOSTIW.

If an error occurs during storage of the IOSTIW, the IPC generates a BCSW service error (BCSWSE) indication to the IOST. The IPC attempts to store both half words of its IOSTIW; but either or both half words may be in an indeterminate state. The IOSTIW state is a function of the error and when the error occurred. The IPC does not generate another IOSTIW for the interrupt that encountered the error condition.

If an error occurs while a buffer terminate interrupt is being stored, the byte count depletion to zero terminates the peripheral control because the F bit of the associated BCW equals zero. The IPC will have generated a BCSWSE as described previously.

The IOSTIW is prepared by the IPC and stored in the BCSW for each IPC and/or control status request. The IPC IOSTIW format is as follows (bits are defined in Tables 3—8, 3—9, and 3—10):

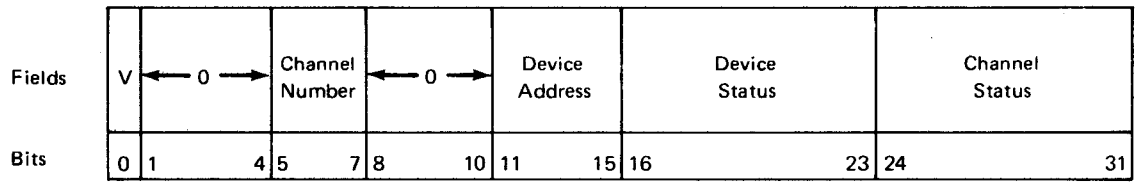


Table 3—8. IOSTIW Fields

Field	Definition
V (bit 0)	This single bit is used by the IOST for control functions. The bit is set to 0 when the IPC stores the IOSTIW.
Zero (bits 1–4)	These bits are unassigned and must be set to 0.
Channel Number (bits 5–7)	This 3-bit field identifies the channel presenting status. The IPC channel is number 0.
Zero (bits 8–10)	These bits are unassigned and must be set to 0.
Device Address (bits 11–15)	This 5-bit field identifies the channel and/or peripheral subsystem to which the channel or peripheral subsystem status pertains.
Device Status (bits 16–23)	This 8-bit field identifies either successful completion or error conditions detected at the peripheral control or subsystem level. The field bits and their significance are listed in Table 3–9.
Channel Status (bits 24–31)	This 8-bit field identifies certain error conditions and the buffer terminate condition used with data chaining sequences. The processor or IPC detects the error conditions. The field bits and their significance are listed in Table 3–10.

Table 3—9. Device Status Bits of IOSTIW

Bit	Designation	Significance
16	Attention	Indicates the operator initiated a transition from stop to run state. The condition is asynchronous and independent of operations initiated by programming.
17–20	–	These bits are set to 0.
21	Device end	Indicates completion of a previously initiated command by the subsystem, and readiness to accept a new command. If the device end bit is presented without the unit check bit, the command is successfully completed.
22	Unit check	An unusual condition is detected at the subsystem level. If presented with the device end bit, the condition occurred during execution of the current command. If presented without the device end bit, the command was rejected during the SIO sequence, prior to initiation of the current command.
23	Unit exception	An unusual condition occurred when an operation was initiated. This indication does not necessarily represent an error condition, but may be presented as a result of an SIO sequence, or upon completion of the operation.

Table 3—10. Channel Status Bits of IOSTIW

Bit	Designation	Significance
24–26	–	These bits are set to 0.
27	Invalid address	Indicates a protection exception or an addressing exception condition occurred during any main storage access, except IOSTIW references.
28	Channel data check	Indicates a storage parity check has been detected when fetching or storing data in main storage during a data transfer sequence.
29	–	This bit is set to 0.
30	Channel control check	Indicates an address check occurred during an IPC operation with main storage, except IOSTIW references. The bit is set if a storage parity check was detected during a fetch or storage of the BCW. The bit is set in conjunction with an invalid address if a protection exception or an addressing exception occurred during the BCW fetch or restoration.
31	Buffer terminate	Indicates the IPC performed the replacement operation required for data chaining operations. Software restores new replacement parameters in the BCW(R) fields.

3.6. CHANNEL STATUS REGISTERS

Two identical registers are included in the IPC to hold channel status until it is stored as an IOSTIW. Each register comprises the device (subchannel) address and the status fields. If each register contains a pending status, the IPC does not accept the SIO instruction, but responds to the SIO by presenting condition code 10_2.

The IPC honors an SIO instruction as soon as the contents of the register are stored in the IOSTIW. If one register is holding status for a pending status, the condition represents a channel busy state indicating all channels are busy.

If both registers contain pending status, the IPC does not honor data requests and it rejects the SIO instruction. The latter condition may cause secondary error indications in the integrated controls waiting for data service (e.g., an overrun indication). This is a locked-out condition and the IPC recovers when the pending status conditions are relieved.

4. System Console and Console Printer

4.1. GENERAL

This section provides information on the UNISCOPE 100 Display Terminal (system console) used with the 90/30 system processor. The system console control (2.4.2) is located in the processor main frame with the integrated peripheral channel (IPC).

Additional information on the system console is available in the UNISCOPE 100 programmer reference manual, UP-7807 (current version). If the SPERRY UNIVAC Console Printer is included with the system, additional information on the console printer can be found in the UNISCOPE 100 console printer manual, UP-7939 (current version).

The system console (Figure 4—1) uses one subchannel of the IPC, and it is designed for direct operator interaction with the processor via the IPC. As such, the system console is basic to the processor complex and cannot be separated from the processor.

As a buffered device with 1024 storage locations, the system console accepts data from the keyboard or the system console control, displays the data, and transfers the data from the buffer to the console printer or IPC. Data transfers can be initiated by the control or control codes transferred as part of the data. Data entered into the system console buffer is displayed on the screen in a 16 line by 64 characters per line format providing a total display of 1024 characters. Displayable characters consist of the 64-character (including space) ASCII set (hexadecimal codes 20 through 5F) plus certain control characters.

The protected format capability provides a means of protecting selected data from operator alteration. The format or data on any portion of the system console screen may be protected while certain unprotected areas are left for operator data entry. Protected areas of the display are defined as all data transferred to the system console between the shift-out (SO) and shift-in (SI) codes.

A hard copy of the data displayed on the system console is provided by the auxiliary interface feature (4.2.5) and the console printer (4.2.3). Under either operator or processor control, selected data displayed on the system console screen can be printed. Once initiated, a print sequence is under control of the system console. Data transfers are from the system console to the console printer.

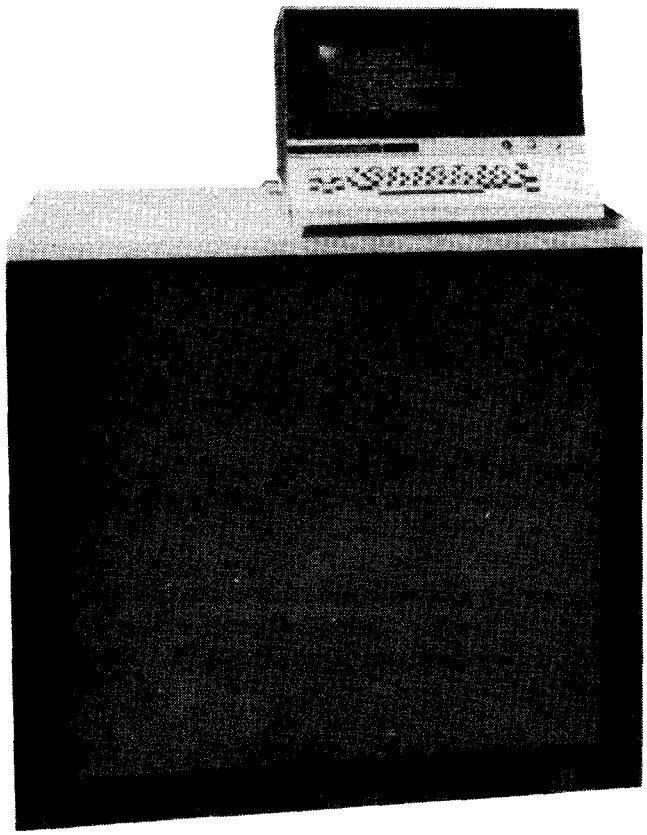


Figure 4—1. 90/30 System Console

4.2. SUBSYSTEM DESCRIPTION

The subsystem description is divided into two parts to cover the system console and the console printer.

4.2.1. System Console

4.2.1.1. Display Screen

The display screen is a cathode-ray tube (CRT) with a viewing surface 5 inches high and 10 inches wide. Spacing between characters is consistent from one end of the screen to the other, and the size and shape do not change relative to the character position on the screen. The character style (uppercase alphanumeric) and size produce maximum legibility and readability. Flicker-free presentation is obtained by regenerating the displayed images 60 times each second (50 times for 50 Hz models).

4.2.1.2. Display Storage

The display storage affords a maximum capacity of 1024 seven-bit characters. It contains a processor-type storage area that provides the same reliability, speed, and random access that are built into the processor.

4.2.1.3. System Console Control Operation

The system console control provides the logical interface between the system console with the 90/30 UNISCOPE 100 interface feature, and the IPC for the transfer of data and status information resulting from system console or console printer operations. The system console provides all decoding of the data required to format information to be displayed on the screen as well as to transfer data to the console printer under control of the auxiliary interface feature. Additional information on the system console control is provided in 2.4.2.

4.2.1.4. Translation Codes

Keyboard translation code from EBCDIC to ASCII is given in Table 4—1.

Table 4—1. System Console Codes and Sequences

Function	Code From Processor	Code to Processor	Hex Code ASCII	Hex Code EBCDIC
Erase display	ESCM	–	1B, 4D	27, D4
Erase unprotected display	ESCa	–	1B, 61	27, 81
Erase to end of line	ESCb	–	1B, 62	27, 82
Delete – in line	ESCc	–	1B, 63	27, 83
Delete – in display	ESCC	–	1B, 43	27, C3
Insert – in line	ESCd	–	1B, 64	27, 84
Insert – in display	ESCD	–	1B, 44	27, C4
Cursor to home	ESCe	–	1B, 65	27, 85
Scan up	ESCf	–	1B, 66	27, 86
Scan left	ESCg	–	1B, 67	27, 87
Scan right	ESCh	–	1B, 68	27, 88
Scan down	ESCi	–	1B, 69	27, 89
Insert line	ESCj	–	1B, 6A	27, 91
Delete line	ESCk	–	1B, 6B	27, 92
Erase field	ESCK	–	1B, 4B	27, D2
Tab	HT	HT	09	05
Tab set	ESCHT	–	1B, 09	27, 05
Transmit unprotected display	DC1	–	11	11
Transmit display	ESCDC1	–	1B, 11	27, 11
Print	DC2	–	12	12
Print transparent	ESCDC2	–	1B, 12	27, 12
Line feed	LF	LF	0A	25
Cursor position	VT	VT	0B	0B
Form feed	FF	FF	0C	0C
Carriage return	CR	CR	0D	0D
Shift out (start protected field)	SO	–	0E	0E
Shift in (end protected field)	SI	SI	0F	0F
Lock keyboard	DC4	–	14	3C
Skip protected data	–	SUB	1A	3F
Code extension	ESC	ESC	1B	27
Start blink field	FS	FS	1C	1C
End blink field	GS	GS	1D	1D
Start of entry (SOE)	RS	RS	1E	1E
Character erase (space)	SP	SP	20	40

NOTE:

The escape (ESC) code used in the sequences required for the console is intended to provide code extension at the console. The ESC code itself is a prefix affecting the interpretation of a limited number of contiguous characters (4.2.1.7).

4.2.1.5. Keyboard and Control Switches

The operator console is the main area of control for the 90/30 systems operator. The operator console consists of a UNISCOPE 100 Display Terminal mounted on top of a floor cabinet. The operator console includes a display screen with two indicators, two switch/indicators, one rotary control, and a keyboard for entering data and information. Figure 4—2 shows the operator console, and Table 4—2 describes the keyboard controls and indicators.

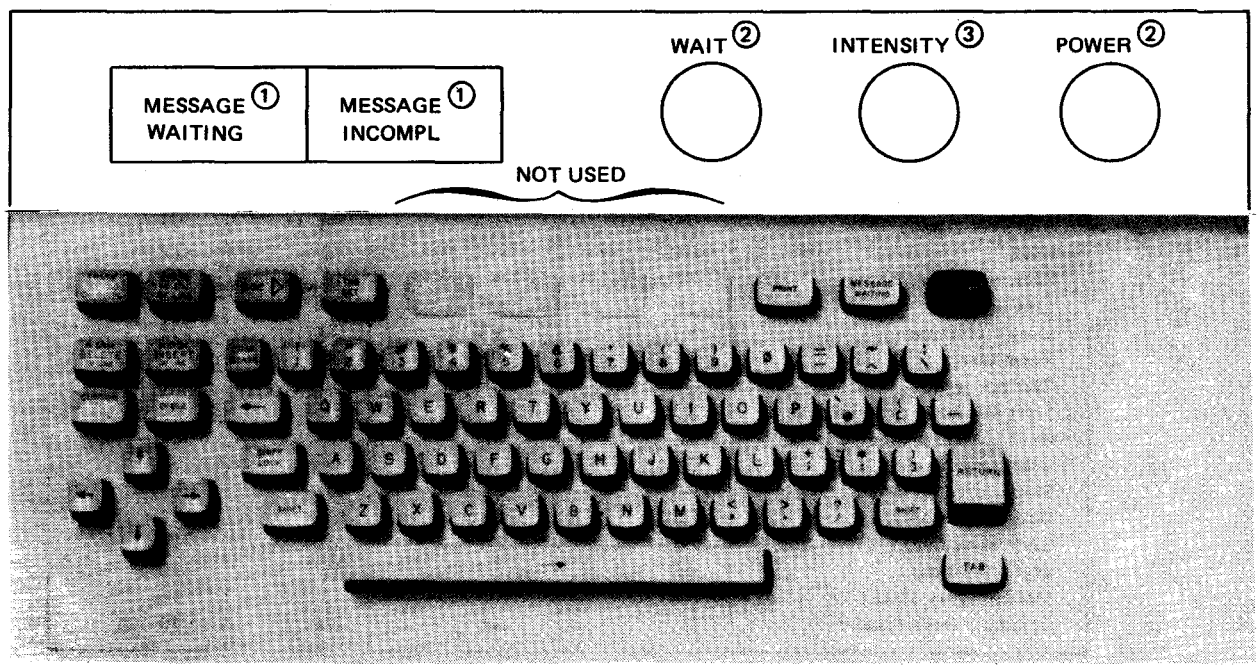
4.2.1.6. Display Control and Indicator Panel

The display controls and indicators (Figure 4—2) are located above the keyboard. The functions of these controls and indicators are given in Table 4—2.

4.2.1.7. Cursor, Editing, and Text Control

Special codes and sequences or keyboard functions are required to perform editing, cursor positioning, and text transfers at the console. The codes and sequences must be included in the data (text) transferred from the processor to the console. The keyboard functions are available to the operator whenever the keyboard is unlocked (WAIT indicator extinguished). The console control remains transparent to all codes and sequences. The console decodes the sequences and performs the specified operations.

The functions described in Table 4—2 apply regardless of the source (keyboard or processor), and when displayed, the codes are entered in the console buffer and require a character position on the screen. Not all codes are required for operation of the console; however, they are included for information purposes.



NOTES:

① Indicators

② Switch/indicators

③ Rotary control

Figure 4—2. System Console Keyboard (Uppercase With Alphanumeric Keys)

Table 4–2. Operator Console Keyboard Controls and Indicators (Part 1 of 3)

Name	Function
WAIT switch/indicator	This indicator lights when the keyboard is locked. The keyboard, except for the MESSAGE WAITING key, is locked whenever the TRANSMIT key is pressed or an input data transfer is occurring on the screen (in which case the control unit unlocks the keyboard at the end of the transfer). The keyboard automatically unlocks after a system reset. When pressed, the switch manually unlocks the keyboard and provides a master clear for the system console. It is advisable not to use this switch when online as it interferes with normal activity and can interrupt transmission or print activity causing loss of data.
INTENSITY control	This control adjusts the brightness of the screen display and should be adjusted for a clear image and not for maximum brightness.
POWER switch/indicator	This switch/indicator controls and indicates power on/off operation of the terminal (push for on, push again for off, as indicated by the backlighted push switch).
MESSAGE INCOMPL indicator	This indicator is turned on by an early termination of a read command. It is reset when the control accepts another command (other than a sense command).
MESSAGE WAIT indicator	This indicator lights during the time a text message is being received by the terminal. It is extinguished when all checks for the message have been satisfied. If the indicator remains lit, the operator should not depend on the displayed data which may contain an error. Normally, the processor program is aware of the error condition and will automatically resend the data.
Keyboard	
Typewriter keys	These keys are arranged in standard typewriter fashion and include alphanumeric and symbolic functions. These are the keys for message composition to the processor. As a key is pressed, the character (uppercase alphanumeric depending on the SHIFT key) is displayed on the screen at the cursor position.
Message Control Keys	
SOE ▷	This is the start-of-entry key which places the start-of-entry symbol on the screen at a position corresponding with the cursor. The location of this symbol on the screen designates the starting point of the message to be transmitted to the processor. The cursor determines the end of message. Automatic carriage return is employed following the last character of each line (nonsignificant space codes are suppressed). If more than one start-of-entry symbol happens to be entered upon the screen, transmission starts at the start-of-entry symbol closest to the cursor and continues until the cursor is reached. If the start-of-entry symbol is not inserted, all data on the screen from the beginning of the display to the cursor is transmitted.
TRANSMIT	Pressing this key alerts the processor that the input message (located between the start-of-entry symbol and cursor, or from beginning of display if no start-of-entry symbol is present) is to be transmitted. Pressing this key locks the keyboard, except for the MESSAGE WAITING key, until a read command is received from the processor. The processor can lock the system console keyboard by transmitting a lock character in the return message.
MESSAGE WAITING	Pressing this key alerts the processor that the operator wishes to enter a message on the screen. The processor must unlock the system console keyboard to permit operator data entry.

Table 4–2. Operator Console Keyboard Controls and Indicators (Part 2 of 3)

Name	Function
Message Control Keys (cont)	
PRINT	Pressing this key causes data presented on the display between the ▷ and the ¬ to be transferred to an output device such as a console printer. It also permits the transfer of data from an input device on the auxiliary interface to be displayed on the console screen.
Cursor Control Keys	
Cursor symbol ¬	The cursor symbol, small right angle (¬), is always present in the screen display and indicates the location where the next keyboard-generated character will be displayed. When in a blank space, the cursor is displayed; however, when in a position already occupied, the character and cursor blink alternately. When in the eighth character position from the end of a line, an audible alarm is momentarily sounded.
Scan forward →	If this key is pressed momentarily, it causes the cursor to move forward (to the right) one position. If the key is pressed and held, the cursor moves forward approximately 10 character positions per second.
Scan backward ←	If this key is pressed momentarily, it causes the cursor to move backward (to the left) one position. If the key is pressed and held, the cursor moves backward approximately 10 character positions per second.
Scan upward ↑	If this key is pressed momentarily, it causes the cursor to move up one line. If the key is pressed and held, the cursor moves upward approximately 10 lines per second.
Scan downward ↓	If this key is pressed momentarily, it causes the cursor to move down one line. If the key is pressed and held, the cursor moves downward approximately 10 lines per second. Space bar and back space cause a single space each time pressed. The space bar provides the same result as the scan forward key. The backspace key provides the same result as the scan backward key.
CYCLE	Pressing this key causes the next alphanumeric or symbolic character (chosen by the operator) to be repeated at a rate of about 10 cycles per second. This key operates with all keys except the ERASE, DELETE, INSERT, SHIFT, SHIFT-LOCK, PRINT, MESSAGE WAITING, TRANSMIT, and CURSOR TO HOME keys. Repetition continues as long as the CYCLE key and typewriter keys are held pressed.
CURSOR TO HOME	Pressing this key causes the cursor to move to the first character position on the screen (upper left-hand corner).
RETURN	Pressing this key moves the cursor to the first character position of the next line.
TAB SET	Pressing this key sets the tab code by inserting a tab character in storage. The position corresponds to the position of the cursor.
TAB	Pressing this key moves the cursor ahead to a position on the screen one space beyond that which was set by the TAB SET key. If no tab was set, the cursor will stop at the home position.

Table 4–2. Operator Console Keyboard Controls and Indicators (Part 3 of 3)

Name	Function
Editing Control Keys	
CHAR ERASE	Pressing this key replaces a character at the cursor position with a space.
ERASE TO END OF LINE	Pressing this key replaces all characters from and including the cursor to the end of the line with spaces.
ERASE TO END OF DISPL	Pressing this key replaces all characters from and including the cursor to the end of the display with spaces.
IN DISPL INSERT INLINE	Lowercase operation of this key causes all the characters in the line from and including the cursor position to move right one position. A space is inserted in the cursor position, and if a character is moved out of the last position of the line, it is discarded. Uppercase operation of this key causes all the characters in the display from and including the cursor position to move right one position. A space is inserted in the cursor position, and if a character is moved out of the last position of the display, it is discarded.
IN DISPL DELETE IN LINE	Lowercase operation of this key causes the characters in the line to the right of the cursor to shift left one position. The original character at the cursor position is deleted, and a space is inserted into the last character position in the cursor line. This key is pressed once for each character to be deleted. Uppercase operation of this key (SHIFT key pressed) causes all characters from the cursor to the end of the display to shift to the left, and a space is inserted in the last position in the display. (Characters in the first position of each line are moved to the last position of the previous line.) In protected format use, this key limits the code sequence to one unprotected field rather than to the end of the line or of the display. This permits the operator to shift several lines within one protected field, but does not allow the shifting of more than one unprotected field at a time.
Alarm	
Sonalert Audio	An audible alarm is provided that is activated when any of the following conditions occur: ■ sounds once at the eighth character position from the end of line; ■ sounds once when the cursor moves to the last line; and ■ sounds repeatedly when an early warning temperature fault is detected in the 90/30 system.

NOTE:

The four special function keys (F1, F2, F3, F4) provided with the keyboard are suppressed in the 90/30 system console.

4.2.2. Auxiliary Interface Feature

The auxiliary interface feature provides control logic and interface circuits required to transfer data, addressing, and console printer status information between the system console and console printer. Operator of the console printer may be controlled by the processor or operator.

The auxiliary interface used by the console printer is a bit-parallel, character-serial, request/acknowledge type. Output signal coding is 7-bit ASCII. Parity is not checked in the console printer.

The system console houses the auxiliary interface that permits half-duplex data flow between the console printer and the system console. Under automatic selection, both input and output buses are used by the console printer to exchange, in addition to data, the information required for selection and status reporting.

Processor-initiated print sequences (write command and DC2 code as the last data byte transferred) result in console printer status being presented to the console control. Console printer status from the auxiliary interface causes ending status to be presented at the completion of the print sequence from the console buffer, or clearing of the auxiliary interface by the system console control if data transfers cannot proceed. The equipment check (SB0,3) sense bit is set in this case.

4.2.2.1. Processor-Initiated Print Sequence

A write command (C modifier bit set) issued to the system console control followed by the DC2 code as the last data byte transferred initiates a print sequence at the console. The keyboard is locked during the write command and after completion of the print sequence unless the unlock keyboard (B modifier bit) is set in the write command. The system console control is busy until completion of the print sequence.

The system console control jams an address of $(75)_{16}$ to the auxiliary interface to select the console printer when the write command is issued. After detection of the DC2 or ESCDC2 codes by the auxiliary interface, the text data printed is the data (protected and unprotected) contained between the SOE symbol and the cursor. Text data to the console printer may include the line feed (LF) and form feed (FF) codes to provide proper formatting of the printed output.

During the print sequence, the console control monitors the auxiliary interface for status information pertaining to the print sequences. A 1-second timer monitors data transfers on the auxiliary interface after detection of the DC2 or ESCDC2 code. Should the timer expire, indicating no data transfers are in progress, the print time-out (SB1,6) sense bit is set.

Should an error occur, the system console control terminates the auxiliary interface print sequence and presents unit check and device end status. The equipment check (SB0,3) and/or intervention required (SB0,1) sense bit is set. Error-free completion of the print sequence results in device end status.

4.2.2.2. Operator-Initiated Print Sequences

Print sequences may be initiated by the operator when the keyboard is unlocked (by a write command modifier bit or the operator pressing the MESSAGE WAITING key) and the operator manually selects the console printer. Pressing the PRINT key causes the printing of data (protected and unprotected) between the SOE symbol (▷) and the cursor. The keyboard is locked when the PRINT key is pressed and unlocked after completion of the print sequence.

4.2.2.3. Print Transparent Sequence

The print transparent sequence (ESCDC2) is analogous to the print (DC2) code except that for the ESCDC2, the carriage return (CR) code is not inserted at the end of each display line transferred to the console printer. With no CR codes in the data, the console printer prints continuously until the right limit switch is reached before performing a line feed. The print transparent sequence is disregarded by the console if the auxiliary interface feature is not installed.

NOTE:

This function is not available from the keyboard.

4.2.2.4. Line Feed Code

The line feed code (LF) performs no function in the system console and is stored in the system console buffer as a nondisplayable code. On a print sequence, the LF code is transferred from the system console to the console printer. The LF code causes a carriage return and advances the form one line at the console printer. The CR code normally inserted by the system console performs a function identical to the LF code.

NOTE:

This function is not available from the keyboard.

4.2.2.5. Form Feed Code

The form feed code (FF) performs no function in the system console and is stored in the console buffer as a nondisplayable code. On a print sequence, the FF code is transferred from the system console to the console printer. The FF code causes a carriage return and a paper advance to four lines beyond the next form perforations (when the form size is 11 inches and loaded between the block pins).

NOTE:

This function is not available from the keyboard.

4.2.2.6. Text Format

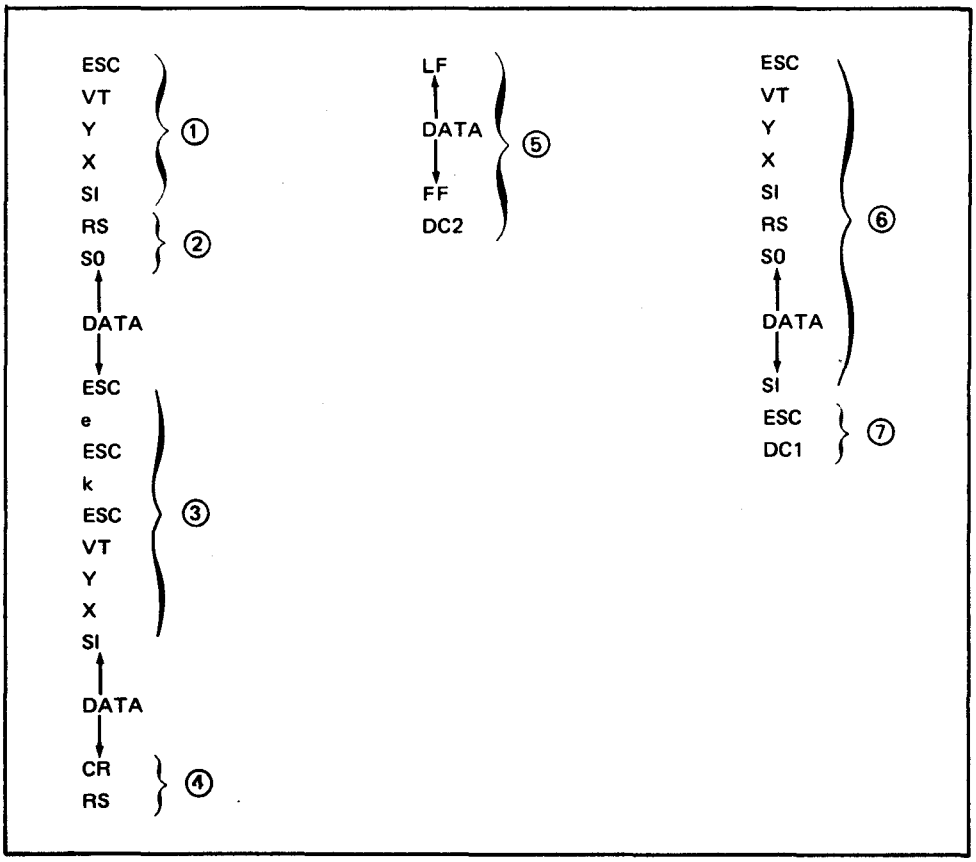
Several formats of text between the processor and the console are shown in Figures 4—3 and 4—4. In data transfers from the processor to the system console, the text is placed on the screen starting at the position of the cursor. If the cursor is not repositioned between data transfers, the text received from the processor follows the text already displayed on the screen. The text starts at the cursor position and moves to the right across the screen and supersedes character by character any prior text displayed.

A carriage return code (CR) in the text causes the next character to be placed at the beginning of the next line without spacing to the end of the line. If the end of the screen is reached, the next character is placed at the home position of the screen. Carriage return codes used before the end of the line do not effect any data to the end of the line when the carriage return is executed.

The erase-to-end-of-line sequence (ESCb) may be used before a carriage return code to erase all of the remaining data on that line. The erase-unprotected-display (ESCa) or erase-display (ESCM) sequence may be used to clear the remainder of the screen before or after the text transfer.

All data intended for display at the system console must be included in the text portion of a properly formatted message. Within the text portion of a message, the SO and SI codes are used to identify protected and unprotected fields. As each data byte is received from the processor keyboard, it is identified in the buffer as a protected or unprotected code. Only unprotected data may be entered from the keyboard; either protected or unprotected data may be entered from the processor. Any number of protected or unprotected data fields may be included in a single text message from the processor.

In the case of both protected and unprotected data, the code sequences from the processor (displayable characters, nondisplayable characters, FS, SOE, tab set) are stored except where there is an intervening cursor control sequence (cursor positioning sequence, tab, carriage return, cursor-to-home). If a cursor control sequence is detected, the same type of storage (protected and unprotected) begins at the new cursor location as had been specified before the cursor control sequence. The locations skipped by the cursor control sequence are not altered.



NOTES:

① Cursor positioning sequence

② SOE symbol start protected field

③ Display rolling and end protected field

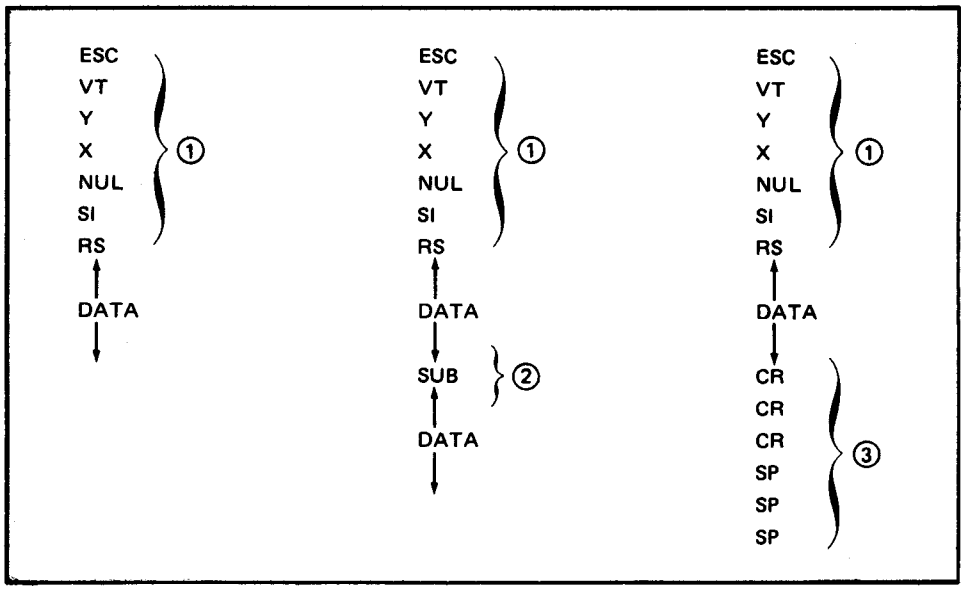
④ SOE symbol positioned for operator data entry

⑤ Printer form control function with text and initiate print sequence code

⑥ Protected text to system console

⑦ Transmit display (or DC1 if data is not protected)

Figure 4—3. Text Format, Processor to System Console



NOTES:

① SOE address and SOE code (RS)

② Skip over protected field

③ Cursor positioned three lines and three positions after last data character

Figure 4—4. Text Format, System Console to Processor

Data transferred from the processor is stored at the specified locations in the system console regardless if the locations are occupied by protected or unprotected data. At completion of data transfer from the processor, the cursor may have been positioned over a protected location permitting alteration of that location from the keyboard. Keyboard alteration of a protected location can be prevented if the cursor is positioned over an unprotected location before permitting operator data entry.

Data transfers initiated by the operator (TRANSMIT key) when the keyboard is unlocked consist of unprotected data only. If the SOE symbol had been entered from the processor or by the operator (SOE key), data is transferred from the SOE up to and including the cursor position. The SOE address and code is the first seven data bytes (Figure 4—4) transferred to the processor. All nonsignificant spaces after the cursor to the end of a line are suppressed; all spaces preceding the cursor are included in the data transfer. When the last character is entered by the operator, the cursor moves to the right one position. The text transferred to the processor includes the data character under the cursor or a CR code if no significant data follows the cursor position.

By including the address of the SOE character at the beginning of the data transferred to the processor along with spaces out to the cursor (Figure 4—4), data transfers from the system console allow software to determine the location of the last operator entry on the screen.

If the SOE (▷) symbol is not on the screen and the TRANSMIT key is pressed, the data sent to the processor is:

ESC VT SP SP NUL SI

followed by all characters preceding and including the cursor position.

If the screen is blank with only the cursor visible, and the TRANSMIT key is pressed, the data sent to the processor is:

ESC VT SP SP NUL SI

followed by n—1 carriage return (CR) codes (n=line position of the cursor).

A space (SP) code for each position between the cursor and the left end of the line that the cursor is on is also sent. If the SOE (▷) symbol is located under the cursor when the TRANSMIT key is pressed, the following data is sent to the processor:

ESC VT Y X NUL SI RS

where Y and X are the coordinates of the SOE code.

4.2.3. Console Printer

The console printer, shown in Figure 4—5, consists of a SPERRY UNIVAC 0769 Incremental Printer, a printer control assembly, power supplies, and the freestanding cabinet which includes the top cover assembly.

Figure 4—5. Console Printer

4.2.3.1. Incremental Printer

The primary operating component of the console printer is the incremental printer. It sits on four rubber-insulated shock mounts on top of the console printer chassis. The incremental printer includes a printing system, carriage, paper feed system, printer drive system, and printer control circuits.

- Printing System

  The printing system consists of the print wheel, ink roll, actuator hammer, code wheel, and reluctance head.

  1. Print Wheel

     A set of 63 characters is arranged around the circumference of the print wheel in a pattern that forms one turn of a helix. Only one character print set is permitted. The characters are sequenced so that the corresponding binary codes are in ascending order, eliminating the need for using a hardware translator with the console printer. Each character is offset slightly from the preceding one, forming the helical pattern. This offset compensates for the continual carriage movement during printing, so that each character is printed in the proper columnar position on the page.

  2. Inking Roll

     A single ink-impregnated roller applies ink directly to the raised characters on the print wheel. The standard color is black, but green, red, and violet inking rolls are available. The inking roll is mounted under a hinged-covered housing in front of the print wheel. It is in constant contact with the surface of the print wheel, supplying the rotating print wheel with ink.

  3. Actuator Hammer

     The print hammer, mounted in the print actuator carriage, is positioned directly behind the print wheel. When the print actuator is energized, the print hammer is thrust against the reverse side of the paper, causing the character on the contacted portion of the print wheel to be printed.

  4. Code wheel and Reluctance Head

     Timing of the printing operation is controlled by the print sprocket signal, which is derived from a 65-tooth code wheel mounted on the left end of the print-wheel shaft. The first 63 cycles of the print sprocket signal directly represent the 63 printable characters on the print wheel; the last two teeth are used for timing.

  5. Carriage

     The carriage of the incremental printer is in two parts, the print-wheel carriage and the print actuator carriage. A braided steel cable, running over two fixed pulleys, connects the two so that their movements are in precise relationship. During printing operations, the carriage pawl solenoid is energized so that the carriage pawl engages the rotating carriage lead screw; this causes the print actuator carriage to be driven from left to right. As the print actuator carriage moves, the print-wheel carriage is drawn along by the steel cable. A spring attached to the print-wheel carriage by a cord-and-pulley arrangement is extended as the carriage moves to the right. When a carriage return is dictated, this spring pulls the carriage back to the initial position. A spring-loaded pawl on the print actuator carriage engages a rack to prevent the carriage from returning prematurely. A solenoid withdraws the pawl from the rack teeth to permit the carriage return. When the carriage is at rest, an index mark on the front of the print-wheel carriage aligns with a bar graduated in column positions to show the columnar position of the carriage.

6. Paper Feed System

   Paper is fed through a slot in the cabinet of the console printer, up through the two paper drive tractors of the printer, and out through a slot in the rear of the top cover assembly. A spring-loaded plate on each tractor holds the paper onto the teeth of the tractor sprocket belts. During paper loading, these plates swing aside to permit easy access to the sprocket belts. Both tractors are driven by a splined shaft coupled through a clutch to a belt-driven pulley. Ordinarily, the tractor drive shaft is prevented from turning by a spring-loaded pawl that engages a stepped phenolic collar on the right end of the shaft; but when paper advance is required, a solenoid is energized that withdraws the pawl and permits the shaft to rotate.

7. Printer Drive System

   The printer drive system includes an electric motor, the print-wheel shaft, the tractor drive shaft and clutch, and the carriage lead screw.

8. Printer Control Circuits

   The electronic circuitry used to control the incremental printer is on a printed circuit board located on the underside of the printer mechanism.

4.2.3.2. Printer Control Assembly

A printer control assembly consists of a printed circuit board containing the logic circuits which form the request/acknowledge interface controlling the operation of the console printer.

4.2.3.3. Internal Power Supplies

Three power supply assemblies are contained in the console printer cabinet which supply the various dc voltages required to operate the console printer electronic circuitry.

4.2.3.4. Top Cover Assembly

Although primarily a part of the console printer cabinetry, the top cover assembly contains functioning parts: a small blower, two cover lamps, the cover interlock switch, the operator's panel, and a wiring harness. The blower exhausts air from the interior of the console printer to prevent temperature buildup. The two cover lamps, located on either side of the access cover, illuminate the incremental printer. As a safety feature, the access cover is equipped with an interlock switch that opens when the access cover is raised, removing ac power from the incremental printer and the blower. The interlock switch also connects the solenoid and actuator drivers of the incremental printer to ground when the access cover is raised. This prevents printer operation during paper loading or printer servicing.

4.2.3.5. Operator Panel

The console printer operator panel has three indicators and two switches.

Figure 4—6 illustrates the operator panel, and Table 4—3 describes the controls and indicators.

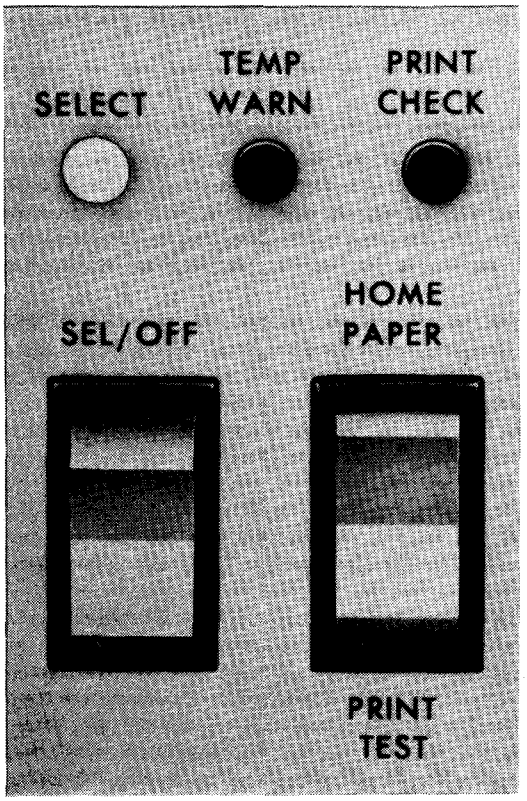


Figure 4—6. Console Printer Operator Panel

Table 4—3. Console Printer Controls and Indicators (Part 1 of 2)

Name	Function
SELECT indicator	The SELECT indicator lights when the console printer is selected as the output device (by either system or manual action). It is turned off when the console printer selection is terminated.
SEL/OFF switch	The SEL/OFF switch is a momentary-contact switch. When the switch is activated, a signal produced is applied to the input of the printer control assembly. As a result, the console printer is selected if it was clear and terminated if it was selected. The switch also produces a CR/LF signal.
TEMP WARN indicator	When internal temperature of the console printer rises to 140(±5)°F (60°C), a thermostatic switch mounted on the pan under the incremental printer closes, causing the TEMP WARN indicator to light. The console printer does not shut down automatically with a high temperature condition; it is the responsibility of the operator to take corrective action upon receiving the indication.
PRINT CHECK indicator	The PRINT CHECK indicator lights and printing stops if the printer is out of paper or if the print actuator fuse, the paper feed solenoid fuse, or the +43-volt dc power supply fuse burns out.

Table 4—3. Console Printer Controls and Indicators (Part 2 of 2)

Name	Function
HOME PAPER/PRINT TEST switch	The HOME PAPER/PRINT TEST switch is a momentary-contact rocker switch that functions only while held at one position or the other. In the HOME PAPER position, the switch signals the incremental printer to advance paper from one form to the top of the next form; this operation continues as long as the switch is held. When the switch is released, the paper advances to the fourth line of the next form and stops. With the switch pressed momentarily to the PRINT TEST position, the console printer prints a complete row of the E character. This operation also continues as long as the switch is held, with carriage return and line feed operations occurring automatically at the end of each line. When the switch is released from the PRINT TEST position, the printer completes the line being printed, performs a line feed and carriage return, and then stops. The PRINT TEST function is disabled when the console printer is selected.
Power panel	The power panel (Figure 4—7) is located at the rear of the console printer, near the left side. Mounted on the panel is a 10-ampere, press-to-reset type circuit breaker and the power ON/OFF rocker switch. The circuit breaker interrupts ac power when overloads occur.
Phasing control	The phasing control (Figure 4—8) is a short lever mounted on the left front side of the incremental printer. This control is easily reached through the access cover in the top cover assembly. Movement of the phasing control varies the position of the reluctance head relative to the code wheel, causing a phase shift in the print sprocket signal and, in turn, changing the time relationship between the print wheel position and application of the print signal to the print actuator. A change in the print hammer impact time results to avoid clipping the top or bottom from the printed characters. Because impact time is a function of form thickness, the phasing control must be adjusted whenever pack thickness is changed.
Paper positioning knob	To facilitate the positioning of preruled forms, a paper positioning knob (Figure 4—8) on the right side of the console printer is provided for the operator to manually adjust the vertical position of the paper. The spring-loaded knob must be pulled outward to engage it with the tractor drive shaft.

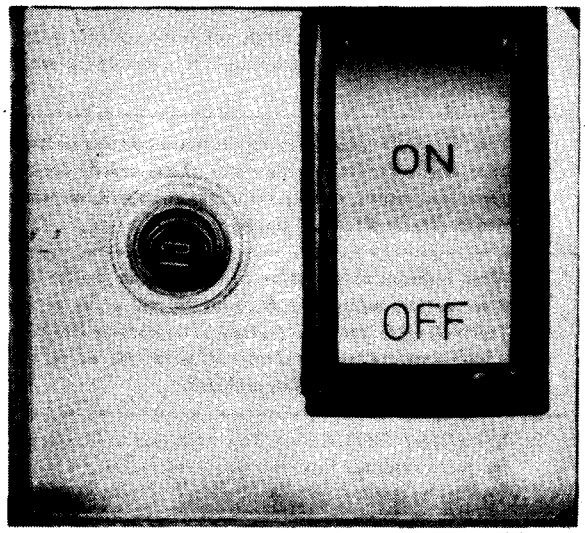


Figure 4—7. Console Printer Power Panel

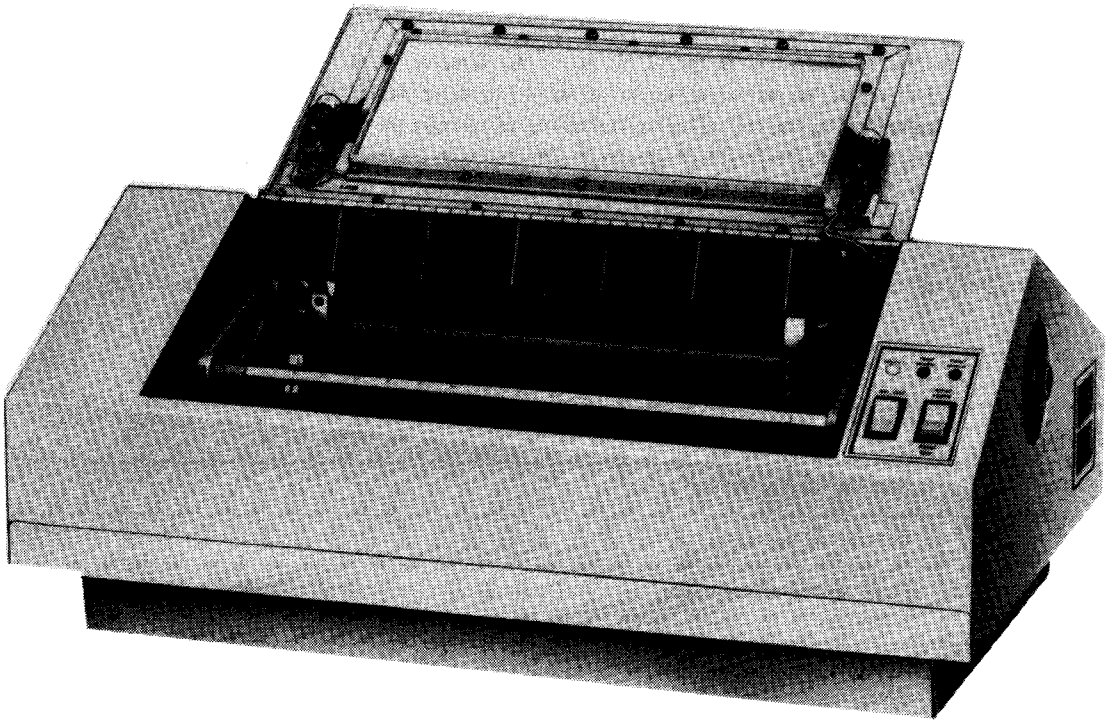


Figure 4—8. Location of Phasing Control and Paper Positioning Knob

4.3. PROGRAMMING

4.3.1. Commands

The command codes listed in Table 4—4 may be issued to the system console control by the processor to initiate data transfers or to interrogate the control about the system console or console printer status. Command codes not listed in Table 4—4 are rejected by the control and result in unit check status being presented to the IPC.

Table 4—4. System Console Commands

Command	Bit							
	0	1	2	3	4	5	6	7
Read	A	X	X	X	X	F	1	0
Write	A	B	C	X	X	F	0	1
Sense	X	X	X	X	0	1	0	0

LEGEND:

X = Bit is ignored by the control.

A, B, C, and F = Modifier bits

4.3.1.1. Read Command

The read command is used to transfer data from the system console to the processor. The read command is normally issued in response to the attention status. Pressing the MESSAGE WAITING key causes the attention status to be transferred to the IPC. The read command causes all data between the SOE(▷) and the cursor to be transferred to main storage when the operator presses the TRANSMIT key. The system console control is busy from the time the read command is accepted, until completion of the data transfer from the system console, and the ending status is presented and accepted by the IPC.

Interpretation of the read command depends on the definition of the modifier bits (A,F) listed in Table 4—5.

Table 4—5. Read Command Modifier Bits

Modifier Bit	Meaning
A=0	Normal read operation.
A=1	Diagnostic use only.
F=0	Read in translate mode. The ASCII-to-EBCDIC translator is enabled, and all data transferred to the processor is in EBCDIC code.
F=1	Read in ASCII mode. The ASCII-to-EBCDIC translator is bypassed and all data to the processor is in ASCII code.

Successful completion of the read command is indicated by device end status presented to the IPC. Any error detected during operation is indicated by unit check and device end status at the conclusion of the operation. The keyboard remains locked (WAIT indicator lit) at completion of the read command. Early termination results in unit check and device end status being presented; the overrun (SB0,5) sense bit (Table 4—8) is set as an indication of early termination.

A read command which is issued after the PRINT key has been pressed by the operator is not executed. The command is rejected with unit check status; the command reject (SB0,0) and the operator print (SR1,2) sense bits are set.

A read command which is issued when the WAIT switch is depressed is not executed. The command is rejected with unit check status; the command reject (SB0,0) and wait active (SB1,3) sense bits are set. The WAIT switch being pressed during the execution of the read command causes immediate termination of the data transfers. Unit check and device end status are presented to the IPC; the overrun (SB0,5) and wait active (SB1,3) sense bits are set.

On a read command, data transfers from the system console buffer may be directed through the ASCII-to-EBCDIC translator provided by the system console control. When translation is not specified by the read command modifier bit, the system console control inserts a 0 in the b_8 position of all ASCII data transferred to the IPC. When ASCII-to-EBCDIC translation is specified, the 7-bit ASCII data from the console is translated to EBCDIC 8-bit codes.

If a data check error is detected, the system console control terminates data transfers with unit check and device end status presented to the IPC. The byte causing the data check error is not transferred to the system console buffer.

On accepting the read command, the following action is initiated by the system console control when transferring read data:

1. Decode the read command.

2. Check if a print operation is in progress to the console printer; if so, the command is rejected.

3. When the TRANSMIT key is pressed, initiate data transfers to the IPC. The data transferred is ASCII or EBCDIC, depending on the modifier bit of the read command.

4. Generate ending status when the transmit indication goes inactive.

5. Maintain the keyboard in a locked state (WAIT indicator lit).

4.3.1.2. Write Command

The write command is used to transfer data from the processor to the system console and console printer. Data to the system console must contain the cursor addressing, display editing, and print control information.

To initiate a print sequence, data transfers on a write command must include the DC2 (12_{16}) code as the last data byte transferred to the system console buffer. The system console control is considered busy until completion of the data transfer to the system console or completion of the print operation (if specified), and until the status byte is presented and accepted by the IPC.

Interpretation of the write command depends on the modifier bits (A, B, C, F), listed in Table 4—6.

Table 4—6. Write Command Modifier Bits

Modifier Bit	Meaning
A=0	Normal write operation.
A=1	Diagnostic use only.
B=0	Locks keyboard at completion of the write sequence. Only the MESSAGE WAITING key is available to the operator.
B=1	Unlocks keyboard at the completion of the write sequence. Operator data entry is allowed. Overrides the DC4 (lock keyboard) code.
C=0	Data transfer is to system console only. No print sequence is to be initiated.
C=1	Data transfer is to the system console and console printer. A DC2 (12_{16}) code must be the last data byte transferred to the system console. The print sequence is initiated by the system console on receipt of the DC2 code.
F=0	Write in translate mode. The EBCDIC-to-ASCII translator is enabled; all EBCDIC data from the processor is translated to ASCII, required by the system console.
F=1	Write in ASCII mode. The EBCDIC-to-ASCII translator is bypassed; all data from the processor must be ASCII, required for the system console.

Successful completion of the data transfer to the system console and console printer (if a print operation is specified) is indicated by device end status presented to the IPC. Any error indication from the auxiliary interface feature also causes a hardware termination of the print sequence.

A write command issued before the TRANSMIT key has been pressed by the operator is executed; no indication is given if operator data entry had been initiated.

A write command issued after the TRANSMIT key has been pressed by the operator is not executed. The command is rejected with unit check status.

A write command issued after the previous data transfer contained a transmit-unprotected-display (DC1) code or the transmit-display (ESCDC1) sequence is rejected with unit check status. The command reject (SB0,0) and transmit active (SB1,4) sense bits are set (Table 4—8).

A write command issued after the PRINT key has been pressed by the operator is not executed. The command is rejected with unit check status; the command reject (SB0,0) and wait active (SB1,3) sense bits are set. The WAIT switch being pressed during execution of the write command causes immediate termination of all data transfers. Unit check and device end status are presented to the IPC; the overrun (SB0,5) and wait active (SB1,3) sense bits are set.

On a write command, data transfers to the system console buffer may be ASCII or EBCDIC. For EBCDIC data transfers, the write command modifier bit selects the EBCDIC-to-ASCII translator. Valid EBCDIC codes translate with the ASCII b_8 bit position set to 0. Invalid EBCDIC codes translate with the b_8 bit set to 1, resulting in a data check (SB0,4) sense bit (Table 4—8) indication.

If ASCII data transfers are specified by the write modifier bit and a data byte contains the b_8 bit set to 1, the data check sense bit is set. If a data check error is detected, the system console control terminates data transfers with unit check and device end status presented to the IPC. The byte causing the data check errror is not transferred to the system console buffer.

On accepting a write command, the following action is initiated by the system console control to perform write data transfers:

1. Decode the write command.

2. Check if a print operation is in progress in the console printer; if so, the command is rejected.

3. Check if the TRANSMIT key is pressed on the system console; if so, the command is rejected.

4. Lock the keyboard (WAIT indicator lit).

5. Activate the auxiliary interface by addressing the console printer, if a print sequence is specified by the write modifier bit.

6. Enable the EBCDIC-to-ASCII translator, depending on the modifier bit of the write command.

7. Request data from the IPC and transfer the data to the system console buffer.

8. At completion of data transfers, monitor the auxiliary interface for completion of the print sequence (if specified) or error indications.

9. The keyboard remains locked unless the write command modifier bit specifies unlocking the keyboard.

4.3.1.3. Sense Command

The sense command is used to interrogate the system console control, and transfer sense information to main storage that reflects unusual conditions detected during the last operation and the current state of the system console and console printer. The command is executed regardless of the state of the device, and may be issued independently, or as a response to unit check status.

Some sense indications may be cleared upon acceptance of a command other than sense (e.g., command reject). Failure to issue the sense command as a response to unit check status may result in loss of the condition.

The system console control transfers two sense bytes to main storage as a result of the sense command. The control probes the auxiliary interface feature and console printer for status before transfer of the sense bytes. The first sense byte contains summary information. Detailed information of the device and control is indicated in the second sense byte. The system console control terminates and presents device end status to the IPC upon successful transfer of the second sense byte.

4.3.2. Status Byte

The status byte supplies information pertaining to the state of the system console control. The status byte is presented to the IPC and stored as an IOSTIW (input/output status table interrupt word) in the BCSW (buffered channel status word) field (3.5) for any of the following conditions:

- as a unit check response to an SIO sequence;
- at completion of a command; and
- if an attention condition is detected.

The status register in the system console control is cleared when the IPC accepts the status byte. Status generated during the SIO sequence causes the IPC to return the appropriate condition code to the processor and if the command was rejected, a subsequent status sequence causes the IPC to store an IOSTIW. The status bits and their meaning are listed in Table 4—7.

Table 4—7. System Console Status Byte

Bit Position	Designation	Definition
0	Attention	Presented each time the operator presses the MESSAGE WAITING key on the system console. Attention status generated during any command sequence will not be presented with ending status for the command but is presented as a separate status sequence. The system console control remains busy until the status is accepted by the IPC.
1	N/A	Set to 0 by the system console control.
2	N/A	Set to 0 by the system console control.
3	N/A	Set to 0 by the system console control.
4	N/A	Set to 0 by the system console control.
5	Device end	Indicates completion of a command initiated by the IPC and readiness to accept a new command.
6	Unit check	Bit set in sense byte 0.
7	N/A	Set to 0 by the system console control.

4.3.3. Sense Data Bytes

Sense indications presented by the system console control are:

- Device conditions (e.g., intervention required, equipment check)

  Presented each time a sense command is issued until the condition is cleared by the operator. No other command is executed under these conditions and will cause unit check status if issued.

- Command reject, data check and overrun indications

  May be cleared if a command other than sense is issued as a response to unit check status.

Table 4—8 presents the name and position of the bits in sense byte 0, and Table 4—9 describes sense byte 1.

Table 4—8. System Console Sense Byte 0

Bit Position	Designation	Definition
0 (SB0,0)	Command reject	Set if an invalid command is issued, or the wait active (SB1,3) or operator print (SB1,2) sense bits are set when a read or write command is issued. Also set if the transmit active (SB1,4) sense bit is set when a write command is issued.
1 (SB0,1)	Intervention required	Set if the system console power is off (SB1,0); console printer no response (SB1,1) or equipment check (SB,3) sense bit is set.
2 (SB0,2)	Bus out check	Set to 0 (not used).
3 (SB0,3)	Equipment check	Set if a fuse fault, print test, interlock, or out-of-paper condition is detected during a write command with the C modifier bit set. Also set if a print time-out (SB1,6) is detected. Always 0 if the auxiliary interface feature is not installed.
4 (SB0,4)	Data check	Set if bit position b_8 of the ASCII bit label code is set to 1. (See 4.2.2.8.)
5 (SB0,5)	Overrun	An early termination of a read command occurred or the WAIT switch was pressed during execution of a read or write command.
6 (SB0,6)	N/A	Set to 0 by the system console control.
7 (SB0,7)	N/A	Set to 0 by the system console control.

Table 4—9. System Console Sense Byte 1

Bit Position	Designation	Definition
(SB1,0) Console	Power off	Set if the system console power has not sequenced up.
1 (SB1,1)	COP no response	Set if the auxiliary interface cannot perform print sequences due to the console printer being in a power-off state or is nonexistent. Always 0 if auxiliary interface feature is not installed.
2 (SB1,2)	Operator print	Set if the auxiliary interface indicates a print sequence is in progress. Always 0 if auxiliary interface feature is not installed.
3 (SB1,3)	Wait active	Set if the operator presses the WAIT switch, or power is turned on at the system console.
4 (SB1,4)	Transmit active	Set if the operator presses the TRANSMIT key or the text data contained a DC1 code.
5 (SB1,5)	Auxiliary interface feature	Set if the auxiliary interface feature is installed; otherwise always 0.
6 (SB1,6)	Print time-out	Set if the 1-second interface timer expired during a print sequence.
7 (SB1,7)	N/A	Set to 0 by the system console control.

5. Card Reader

5.1. GENERAL

This section contains information for operating and programming the SPERRY UNIVAC 0717 Card Reader Subsystem. The card reader (Figure 5—1) is designed for integration in the 90/30 system processor both operationally and mechanically. Even though it is a freestanding unit, it is dependent entirely on the card reader control located in the processor. The card reader control (2.4.3), in turn, responds to instructions from the integrated peripheral channel (IPC).

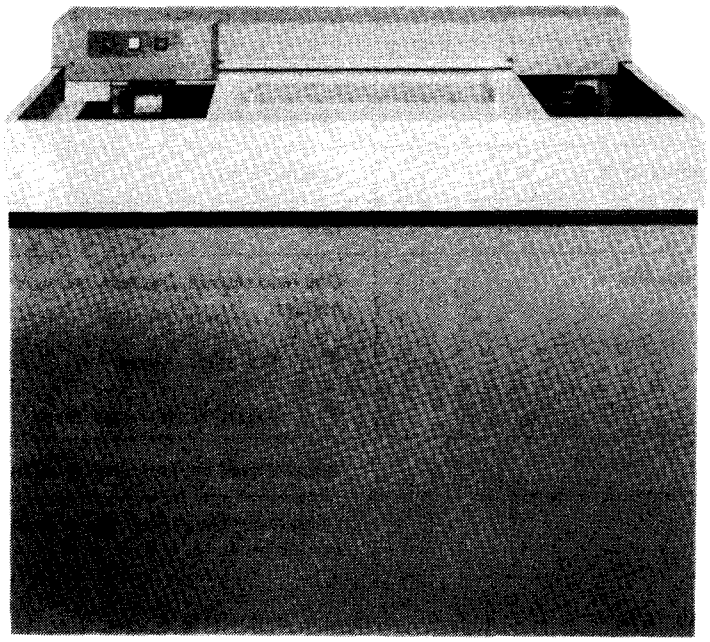


Figure 5—1. 0717 Card Reader Subsystem

5.2. SUBSYSTEM DESCRIPTION

The card reader is an 80-column reader capable of reading 500 standard-thickness cards per minute in a column-by-column manner. It contains two read stations, a primary station (read station 1) to read the data, and a secondary station (read station 2) to checkread the data. One output stacker with a capacity of 2000 cards and one input hopper with a capacity of 2400 cards, and validity checking are part of the basic device. Feature additions provide 51- or 66-column short card read capability.

Control of the feed mechanism is on a demand basis and reading is column serial. When each feed command is received, a single card is fed. Once fed, a card is committed to be read and stacked. The card proceeds at constant speed in the transport.

Card orientation in the hopper is conventional file mode; ascending order front-to-back when decks are placed in a face-forward position. The arrangement of the hopper and stacker permits sustained operation at maximum rate by a single operator.

The basic characteristics of the card reader are listed in Table 5—1.

Table 5—1. Card Reader Characteristics

Item	Characteristic
Number of card columns read	80, 66, or 51
Number of cards read per minute, maximum	500
Output stacker capacity, maximum	2000 cards (standard thickness)*
Input hopper capacity, maximum	2400 cards (standard thickness)*
Feed mechanism control mode	Demand basis
Method of reading cards	Column, serial
Number of cards fed per command	One
Read check capability	One read station, 2 stacks each with 12 photosensitive devices: ■ first stack — read ■ second stack — read check
Feeding	Vacuum feed actuator with friction drum
Transport	Cards transported past read station to the stacker using double flat belts

*Standard card thickness = 0.007±0.0004 inches; 0,178±0,010 mm

5.2.1. Configuration

The card reader consists of a single unit containing the necessary components to operate with an 8-bit byte-oriented 90/30 system processor. The card reader is connected to the processor through the IPC and appropriate interface hardware. Figure 5—2 illustrates the functional arrangement of the card reader and processor. The operational features of the card reader are listed and described in Table 5—2. Major components of the card reader are illustrated in Figure 5—2.

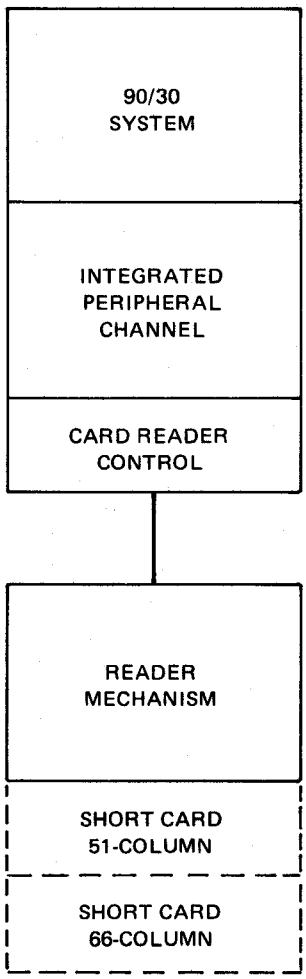


Figure 5—2. Card Reader Configuration

Table 5—2. Card Reader Type and Optional Features

Item	Description
Card reader	80-column, 500 cards per minute. Multiread checking: 0717—00: 60 Hz operation 0717—01: 50 Hz operation
Short card 51-column feature	Permits reading of 51-column cards. Logic required is located in the associated integrated control unit in the processor.
Short card 66-column feature	Permits reading of 66-column cards. Logic required is located in the associated integrated control unit in the processor.

The card reader operates online through the IPC and I/O interface to the processor. The basic components comprising the card reader are: the hopper, read stations, transport, stacker, interface, control panels, and power distribution.

5.2.2. Hopper

The hopper holds up to 2400 standard-thickness punched cards that are to be read, with a feed mechanism capability of feeding a maximum of 500 cards per minute.

5.2.3. Read Station

The read station is located immediately adjacent to the hopper and contains two columns of phototransistors activated by a lamp. These phototransistors and read sprockets supply electrical signals accurately related to the columnar position of the card at the read station.

5.2.4. Transport

The punched cards are transported from the hopper past the read station to the stacker using flat double belts. The physical speed and arrangement of the transport permit as many as three 80-column or five 51-column cards in the transport area simultaneously. The transport contains detectors which permit positioning tests to assure proper movement of the punched card through the transporting system. Logical tests and restoring actions taken in case of a malfunction in this area are determined in the card reader control unit.

The operation of the drive train (motor and belts) is directly controlled by the card reader control; the vacuum pumps and reader lamps are indirectly controlled by the same card reader control signal. The card positioning test, indicating a card jam in the transport, causes immediate power removal from the drive motor.

5.2.5. Stacker

One stacker is provided to receive the read punched cards with a capacity of 200 standard-thickness cards. Card stacking is controlled by a timed carousel stacker.

5.2.6. Card Reader Control

The card reader control provides the functional capabilities to perform card read operations and to transfer data and status information to the IPC. The IPC performs all main storage accesses, buffer control word (BCW) manipulations, input/output status table interrupt word (IOSTIW) presentations, and status sequences required for the operation of the card reader (Figure 5—3). An 8-bit data path is provided between the IPC and card reader control. Command codes are sent from the IPC to the card reader control; data, status, and sense information is sent from the card reader control to the IPC.

The card reader control responds to one device (card reader) address. Only the active BCW fields are used for card reader control.

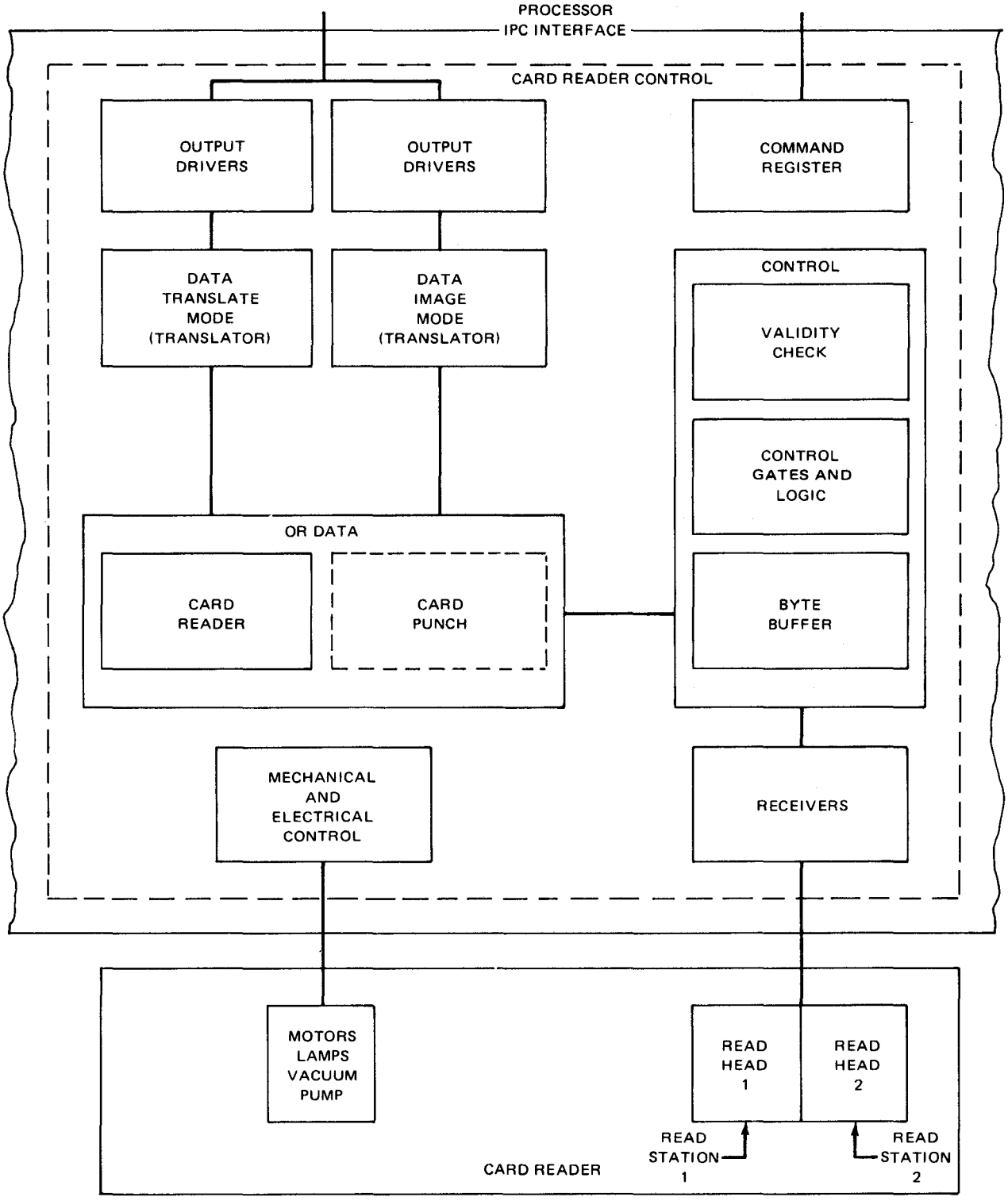


Figure 5—3. Card Reader Control, Block Diagram

5.2.7. Control Panels

Two control panels are provided for the operation and maintenance of the card reader. One is located on the card reader and contains two control switch/indicators and one control switch; the other panel is located on the processor operator/maintenance panel and contains six indicators.

5.2.7.1. Card Reader Control Panel

The card reader control panel, located in the upper left corner of the card reader, contains the RUN and STOP switch/indicators and the FEED switch.

Table 5—3 lists and describes the card reader control panel switch/indicators.

Table 5—3. Card Reader Control Panel Switch/Indicators

Switch/Indicator	Description
RUN switch/indicator	When pressed and released, all error conditions are cleared (provided necessary corrective action has been performed) and the reader is in the run state. RUN indicator lights and STOP indicator extinguishes.
STOP switch/indicator	Pressing this switch places the reader in the stop state; the STOP indicator remains lit after release of pushbutton. RUN indicator is off during the stop state. Pressing this switch when reader is in the stop state serves as a lamp test for the reader control panel indictors.
FEED switch	When pressed and released, provides a method of feeding one card at a time through the card reader during the stop state. It provides an integrity test of the card path. If the switch is pressed and held, cards feed continuously until the switch is released.

5.2.7.2. Processor Operator/Maintenance Panel Indicators for Card Reader

The card reader is provided with six indicators located on the processor operator/maintenance panel for card reader operation and maintenance. Table 5—4 lists and describes these indicators.

Table 5—4. Processor Operator/Maintenance Panel Indicators for Card Reader

Indicator	Description
TRANSFER CHECK	Indicates a transfer check (SB1,4).
FEED CHECK	Indicates an equipment check (SB0,3).
HOPPER	Indicates a card from the hopper failed to reach the read station after the card reader control made several attempts to feed. If card fails to feed, the motors shut off immediately. Intervention is required, (SB0,1) is set, and the stop state is initiated.
READ	Indicates a column 0 error (SB1,0), compare error (SB1,2), resync error (SB1,3), or an overrun error (SB0,5). The card causing the sense indication will be the last card in the stacker. This indicator also lights in combination with FEED CHECK when equipment check (SB0,3) is set due to a card being slowed or stopped in the read station (SB0,3, condition 1, refer to Table 5—10).
VALIDITY	Indicates a validity check (SB1,1); the card causing the sense indication is the last card in the stacker.
DEVICE CHECK	Indicates an error condition that has set the device check sense bit (SB0,7). An early warning temperature condition detected in the card reader also lights this indicator.

5.2.8. Power Distribution

The card reader operates as a slave input peripheral device to the processor. As a result, all ac and dc power is distributed and controlled by the processor. Power is applied to the card reader through the power interface cable in proper sequence from the processor, IPC, and card reader control.

5.2.9. Stop Conditions

The card reader goes into the stop state if any of the following conditions occur:

- Stacker-full switch (normally open)

  This switch detects when the stacker is overfilled.

- Interlock switch (normally open)

  Two interlock switches detect when the mechanism cover or front panels are not properly closed.

- Overheat thermostat (normally open)

  A vacuum pump thermostat and a read lamp thermostat are ambient temperature sensors and indicate any overheating conditions. If overheating occurs during operation, the card reader halts (stop state).

5.3. PROGRAMMING

5.3.1. Data Transfer Rate

To maintain the maximum card throughput rate of 500 cards per minute (5.2), response time cannot exceed 3 milliseconds. The response time is defined from the time of status generation in the card reader control until the next command to feed a card (read command) is received by the card reader control.

The time between successive data requests is approximately 700 microseconds (based on a column read time). However, the time to respond to a data request must be less than 600 microseconds. Failure to meet this requirement produces an overrun condition and data transfers terminate immediately. Status is presented at the normal ending point for the operation, and the stop state is entered when the status is accepted by the IPC.

5.3.2. Data Transfer Operations

All data transfer operations performed by the IPC may be classified as transparent or translated types. Transparent data operations result in no alteration of information bytes. The code for this type of data is determined by the user. Translated data operations require conversion from a source code to a destination code. All code conversions are performed by hardware translators. Translated data transferred to main storage is converted to the EBCDIC code.

The card reader translator required for code conversion is the extended-card-code to EBCDIC. The translator is time-shared by the card reader control and card punch control.

The card reader control has specific buffering capabilities. The amount of buffering is provided by the IPC, and the IPC either furnishes or accepts a variable amount of data during a given data transfer sequence.

A brief summary of the card reader control needs for each data transfer is as follows:

Requirement	Sense Command/ Image Mode	Translate Mode
Typical number of main storage accesses	6	6
Additional cycles which may be required during BCW update (can occur only once during a command)	1	1
Data direction	Input to control	Input to control
Data code	Transparent	EBCDIC code
Data transferred per one IPC data transfer sequence	Two bytes (half word)	One byte

On accepting the read command, the card reader control initiates the following steps (Figure 5—4):

1. Start card movement by feeding a card from the hopper.
2. Read a card column at read station 1 and transfer the data to a register in the reader control.
3. Check read the card column at read station 2.
4. Transfer the data to main storage by way of the IPC.
5. Continue steps 2 through 4 until all card columns have been read.
6. Direct the card from read station through the long or short card transport path (dependent upon stacker timing) to the stacker. No wait station is provided in the card reader; card motion is continuous once initiated.
7. When data transfers for the card have been completed, the card reader control generates end status and presents it by way of the IPC.

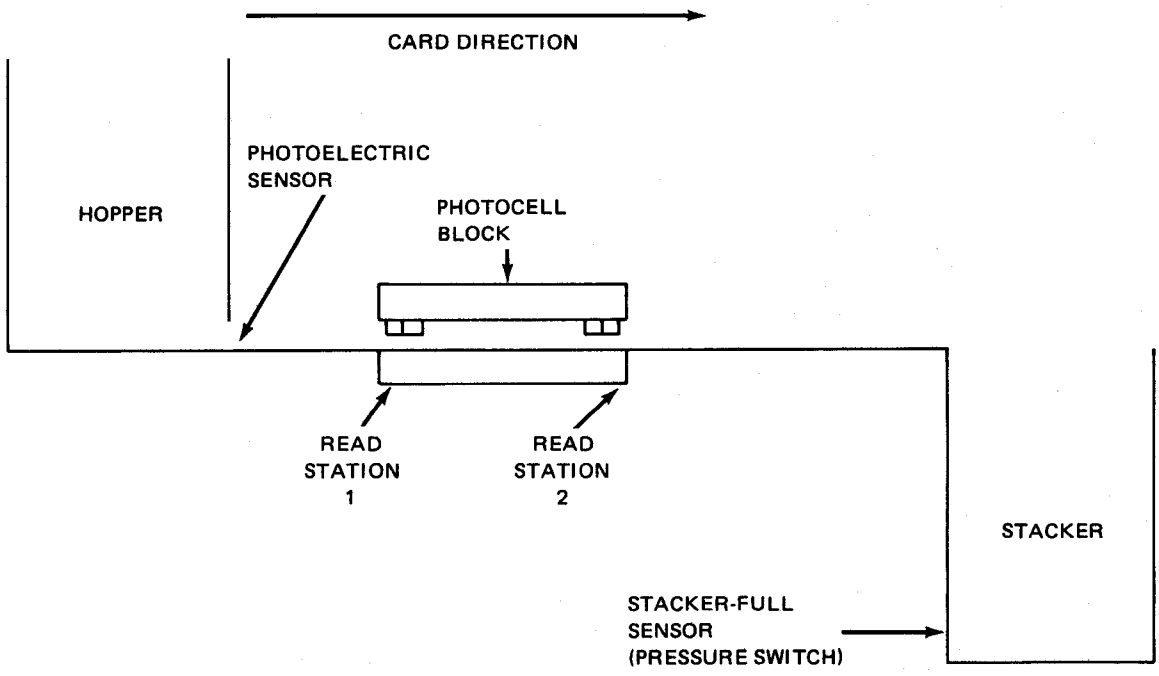


Figure 5—4. Card Path Through Card Reader

When the card reader control has data available for transfer to the IPC, service is requested from the IPC. The IPC services card reader control data requests on a priority basis. One column is read at a time resulting in the transfer of one or two bytes of data based on whether translate mode or image mode is specified in the read command.

5.3.2.1. Translate Mode Data Format

In translate mode, each column read results in the transfer of one byte of data to the IPC. Translation of the card data is made from extended card code to EBCDIC code, as listed in Table 5—5.

Table 5—5. Extended Card Code to Hexadecimal Translation (Part 1 of 2)

Extended Card Code ③	Hexadecimal ① Card Zones ②							
	Blank	12	11	0	12–11–0	12–11	12–0	11–0
Blank	40	50	60	F0	70	6A	C0	D0
1	F1	C1	D1	61	B1	91	81	A1
2	F2	C2	D2	E2	B2	92	82	A2
3	F3	C3	D3	E3	B3	93	83	A3
4	F4	C4	D4	E4	B4	94	84	A4
5	F5	C5	D5	E5	B5	95	85	A5
6	F6	C6	D6	E6	B6	96	86	A6

Table 5–5. Extended Card Code to Hexadecimal Translation (Part 2 of 2)

Extended Card Code ③	Hexadecimal ①							
	Card Zones ②							
	Blank	12	11	0	12–11–0	12–11	12–0	11–0
7	F7	C7	D7	E7	B7	97	87	A7
8	F8	C8	D8	E8	B8	98	88	A8
9	F9	C9	D9	E9	B9	99	89	A9
1–8	79	49	59	69	B0	90	80	A0
2–8	7A	4A	5A	E0	BA	9A	8A	AA
3–8	7B	4B	5B	6B	BB	9B	8B	AB
4–8	7C	4C	5C	6C	BC	9C	8C	AC
5–8	7D	4D	5D	6D	BD	9D	8D	AD
6–8	7E	4E	5E	6E	BE	9E	8E	AE
7–8	7F	4F	5F	6F	BF	9F	8F	AF
1–9	31	01	11	21	71	51	41	E1
2–9	32	02	12	22	72	52	42	62
3–9	33	03	13	23	73	53	43	63
4–9	34	04	14	24	74	54	44	64
5–9	35	05	15	25	75	55	45	65
6–9	36	06	16	26	76	56	46	66
7–9	37	07	17	27	77	57	47	67
8–9	38	08	18	28	78	58	48	68
1–8–9	39	09	19	29	30	10	00	20
2–8–9	3A	0A	1A	2A	FA	DA	CA	EA
3–8–9	3B	0B	1B	2B	FB	DB	CB	EB
4–8–9	3C	0C	1C	2C	FC	DC	CC	EC
5–8–9	3D	0D	1D	2D	FD	DD	CD	ED
6–8–9	3E	0E	1E	2E	FE	DE	CE	EE
7–8–9	3F	0F	1F	2F	FF	DF	CF	EF

NOTES:

① Hexadecimal equivalents for zone and digit combinations not listed are not valid.

② Zones are rows 12, 11, 0.

③ Digits are rows 1, 2, 3, 4, 5, 6, 7, 8, and 9.

5.3.2.2. Image Mode Data Formats

In image mode, each column read results in the transfer of two bytes of data to the IPC. The following restrictions apply to the half-word transfers:

- The count (A) field, bits 54 through 63 of BCW1, must contain an even count. If an odd count is initially placed in this field, the main storage location corresponding to the last byte transferred plus one is cleared to 0's by the IPC (starting address + byte count + 1).
- The main storage address must start on a half-word boundary. If the address does not start on a half-word boundary, data is stored starting at main storage location (starting address —1) nearest the lower half-word boundary.
- The first byte (rows 12, 11, 0, 1, 2, and 3) is always stored in the most significant half of the half word.
- The second byte (rows 4, 5, 6, 7, 8, and 9) is always stored in the least significant half of the half word.

The 8-bit bytes transferred to the IPC contain the two most significant bits set to zero. The six least significant bits of two adjacent bytes contain one column from the card (Figure 5—5). Data transfers to the IPC start from column 1.

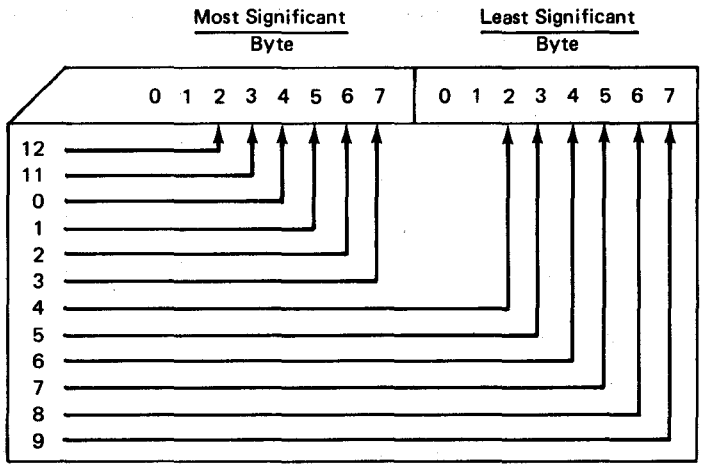


Figure 5—5. Image Mode Byte Formats on Card

5.3.3. Card Reader Commands

Command codes may be issued to the card reader control by the processor to initiate data transfers or interrogate the card reader control about device conditions. See Table 5—6.

Table 5—6. Card Reader Commands

Command	Bits (BCW0)							
	0	1	2	3	4	5	6	7
Read	A	B	X	D	E	F	1	0
Sense	X	X	X	X	0	1	0	0

LEGEND:

X = Bit is disregarded by card reader control

D, E, F = Modifier bits

A = Modifier bit for diagnostic use only; normal operation of the card reader should not be predicated on the use of this bit

B = Normal read operation; when set to 1, selects read station 2 only

Command codes not specified in Table 5—6 are rejected by the card reader control and result in unit check status being presented to the IPC. The card read control and card reader do not go active.

5.3.3.1. Card Reader Read Command

The read command is used to initiate feeding and reading a card. The card reader control is considered busy from the time the command is accepted until the status byte is presented and accepted by the IPC. Interpretation of the read command depends on the definitions of modifier bits A, B, D, E, F (Table 5—7).

Table 5—7. Card Reader Read Command Modifier Bits

Modifier Bit	Definition
A = 0	Normal read operation
A = 1	Diagnostic
B = 0	Normal read operation
B = 1	Select read station 2 only, inhibit compare error (SB1,2).
D = X and E = 0	Eighty-column read. Normal mode for standard size 80-column punch cards.
D = 0 and E = 1	Short card (51-column) read. Permits reading of 51-column card; feature must be installed.
D = 1 and E = 1	Short card (66-column) read. Permits reading of 66-column card; feature must be installed.
F = 0	Read in translate mode. The extended card code to EBCDIC translator is selected.
F = 1	Read in image mode.

Successful completion of the read command is indicated by device end status being presented to the IPC. Any error detected during the read operation is indicated by unit check and device end status.

The read command is executed by the card reader control when the device is in the run state. A read command issued when the device is in the stop state does not initiate an operation; rather a unit check status is presented. Early termination of data transfers initiated by the read command may be specified by the T bit (bit 50 of BCW1) set to 1 (Table 3—5) or count (A) field decremented to zero. Either termination results in normal ending status being presented; no special indication of early termination is indicated. Early termination (T bit set to 1 initially) can be used to feed a card without data transfer.

5.3.3.2. Card Reader Sense Command

The sense command is used to interrogate the card reader control and store data in main storage indicating unusual conditions detected during the last operation and the current state of the card reader. The command is executed regardless of the state of the card reader (run or stop) and may be issued independently or as a response to unit check status. With the card reader in the run state, some sense indications may be cleared upon acceptance of a command other than the sense command (such as command reject). Failure to issue the sense command as a response to a status indication can result in the loss of the sense condition.

The card reader control transfers two sense bytes to main storage as a result of the sense command. The first sense byte contains summary information with detailed information of the card reader. Control is indicated in the second sense byte. The control terminates and presents device end status to the IPC upon successful transfer of the second sense byte.

If the sense command is issued with the BCW count (A) field set to 1, the card reader control transfers two sense bytes; however, only the first sense byte is stored. If the sense command is issued and the BCWT (A) bit is set to 1, no sense bytes are transferred. In either case, normal ending status is presented to the IPC. Unit check status is never set with device end status for a sense command.

5.3.4. Card Reader Status Byte

The status byte presents information pertaining to the state of the card reader control. The status byte is presented to the IPC and stored as an I/O status table interrupt word (IOSTIW) in the buffered channel status word (BCSW) fields (3.5).

- as a unit check response to a start I/O (SIO) sequence;
- at the completion of a command; or
- if an attention condition is detected.

The status register in the card reader control is cleared when the IPC accepts the status byte. Status generated during an SIO sequence causes the IPC to return the appropriate condition code to the processor, and if the command was rejected, a subsequent status sequence causes the IPC to store an IOSTIW.

The status bits and their interpretations are listed in Table 5—8.

Table 5—8. Card Reader Status Byte

Bit Position	Designation	Interpretation
0	Attention	Indicates transition from stop state to run state.
1	–	Set to 0 by card reader control.
2	–	Set to 0 by card reader control.
3	–	Set to 0 by card reader control.
4	–	Set to 0 by card reader control.
5	Device end	Indicates the completion of a command initiated by the IPC and readiness to accept a new command.
6	Unit check	Indicates at least one bit is set in sense byte 0.
7	–	Set to 0 by the card reader control.

5.3.5. Card Reader Sense Data Bytes

Sense indications presented by the card reader control are divided into two categories:

1. Card reader conditions (i.e., intervention required, equipment check) which result in the stop state (Figure 5—6) are presented each time a sense command is issued until the condition is cleared by the operator. No other command is executed under these conditions; unit check status results if other than a sense command is issued.

2. The command reject indication which may be cleared if a command other than sense is issued in response to unit check status.

Table 5—9 lists the name and position of the bits in each sense and status byte. The status and sense bits and associated switch/indicators are summarized in Figure 5—6.

The interpretation of the sense bits and the conditions that set them are listed in Table 5—10.

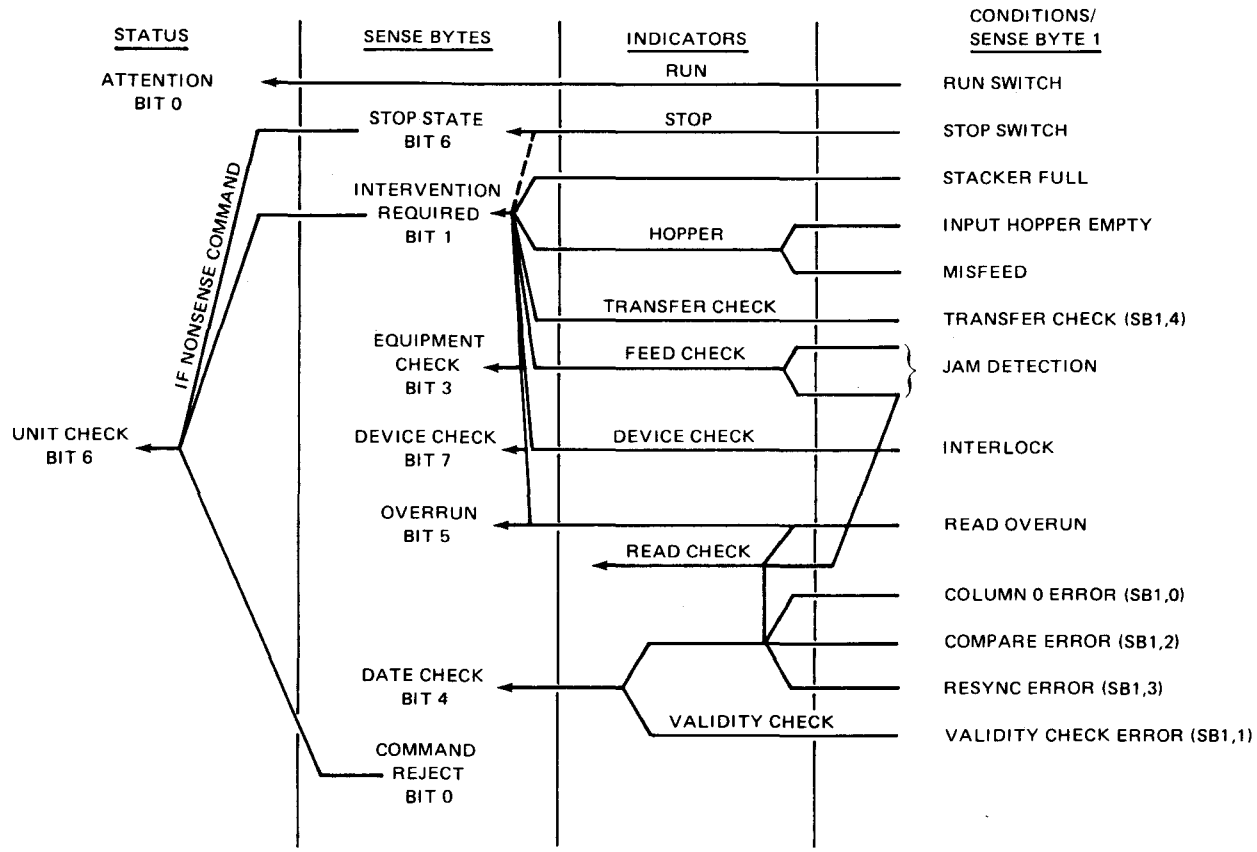


Figure 5—6. Summary of Card Reader Status and Sense Bytes

Table 5—9. Card Reader Status and Sense Byte Summary

Commands	Bit	Status	Sense 0	Sense 1	Switches	Indicators
0 1 2 3 4 5 6 7	0	Attention	Command reject	Column 0 error	RUN	RUN
Sense: X X X X 0 1 0 0	1	Not used	Intervention required	Validity check error	STOP FEED	STOP READ CHECK
Read: A B X D E F 1 0	2	Not used	Not used	Compare error		FEED CHECK HOPPER
	3	Not used	Equipment check	Resync error		TRANSFER CHECK
	4	Not used	Data check	Transfer check		DEVICE CHECK
	5	Device end	Overrun	Not used		VALIDITY CHECK
	6	Unit check	Stop state	Feature: 51-col.		
	7	Not used	Device check	Feature: 66-col.		

Table 5–10. Sense Bit Interpretations (Part 1 of 2)

Bit Position	Designation	Interpretation
		Sense Byte 0 (SB0)
0 (SB0,0)	Command reject	Set to 1 if an invalid command is issued. Invalid command codes are any codes not listed in Table 5–6. Unit check status is set to 1 and card reader control does not go active.
1 (SB0,1)	Intervention required	Set to 1 if a condition is detected that requires manual intervention (Figure 5–5).
2 (SB0,2)	Bus out check	Not used and is set to 0 by the card reader control.
3 (SB0,3)	Equipment check	Set to 1 if a card transport error has occurred (card jam). The following conditions cause this error: 1. The read station photocells remain covered, indicating that a card has slowed or stopped in the read station. 2. A card covers the gate photocell and does not pass within the prescribed time count. The motors are turned off immediately and the stop state entered.
4 (SB0,4)	Data check	Set to 1 if any of the following conditions are detected: ■ Column 0 error (SB1,0) ■ Validity check error (SB1,1) ■ Compare error (SB1,2) ■ Resync error (SB1,3)
5 (SB0,5)	Overrun	Set to 1 if an overrun condition on data transfer is detected.
6 (SB0,6)	Stop state	Set to 1 if the card reader in in the stop state. The card reader may enter the stop state by way of the STOP switch or an error condition (Figure 5–5).
7 (SB0,7)	Device check	Set to 1 if the card reader detects an interlock active. If device check occurs during a command, the command is terminated immediately.
		Sense Byte 1
0 (SB1,0)	Column 0 error	Set to 1 if all 12 read amplifiers are not off midway between the leading edge of a card and column 1.
1 (SB1,1)	Validity check error	Set to 1 if the command specified translate and the card reader control detected multiple punches in rows 1 through 7 for any individual column.
2 (SB1,2)	Compare error	Set to 1 if for any given column the data read in read station 1 does not compare when read in station 2.

Table 5–10. Sense Bit Interpretations (Part 2 of 2)

Bit Position	Designation	Interpretation
	Sense Byte 1 (cont)	
3 (SB1,3)	Resync error	Set to 1 if the card reader control does not detect a punch hole after the read strobe has been synchronized. A read strobe is performed on every column. A resync is performed only when the leading edge of a hole is detected. If a resync occurs, a check is made to verify if the hole still exists (properly centered). The error occurs when the hole does not register properly.
4 (SB1,4)	Transfer check	Set to 1 if a card is fed from the hopper and detected by the read station photocells or the card path sensor when a feed was not issued by the card reader control. The motors are turned off immediately and the stop state entered. No status indication is presented to the IPC until the next SIO sequence to the card reader control.
5 (SB1,5)	NA	Set to 0 by the card reader control.
6 (SB1,6)	51-column feature	Set to 1 if feature is installed; otherwise 0.
7 (SB1,7)	66-column feature	Set to 1 if feature is installed; otherwise 0.

5.3.6. Card Reader Motor Control

The card reader control turns off the reader motors when cards are not being processed.

If a feed order is given to the card reader by way of the FEED switch or a read command, a 3-second delay is initiated. The delay inhibits activation of the card feed actuator coil until the motors are up to speed and an adequate vacuum level has been produced.

Issuing a feed order to the device also initiates a 15-second delay. If 15 seconds elapse between feed orders, the reader motors turn off. The card reader motors turn off after 15 seconds when the STOP switch/indicator is pressed or an error condition causes the card reader to enter the stop state. An equipment check (SB0,3), device check (SB0,7) or transfer check (SB1,4) causes the motor to turn off immediately without the 15-second delay.

5.3.7. Card Reader Card Feed

All cards (80-, 66-, or 51-column) are placed in the hopper with cards facing away from operator towards reader, and with column 1 leading and row 9 down. No initial feeding is required because no wait station is provided in the card reader.

When a card feed is activated, a card is separated from the deck and fed from the hopper to read station 1 where it is read, through read station 2 where it is read-checked, and finally to the stacker (Figure 5—4).

5.3.7.1. Manual Card Feed

A FEED switch is provided for manual feeding of cards through the card reader.

5.3.7.2. Program Controlled Card Feed

Program controlled card feed occurs when a read command is accepted by the card reader control. If an error occurs during execution of the command, the error card is either the last card in the output stacker or somewhere in the card transport path as a result of a card jam. Card reader motors are turned off automatically either immediately or after a 15-second delay.

5.3.8. Error Recovery

When an abnormal condition occurs, the card reader stops, an indicator on the card reader control panel lights, and the appropriate bits in the status and sense data bytes are set.

By observing which indicator lights on the processor operator/maintenance panel and the status presented, action can be taken to recover from erroneous programming or faulty operation. Figure 5—6 lists a summary of the status and sense bytes that result in setting the unit check bit (bit 6 of the status byte).

5.3.8.1. Unit Check

When bit 6 of the status byte is set, any one of the sense byte bits has been set (5.3.4). Recovery procedures can be accomplished by determining the reason why the particular bit of the sense byte was set.

6. Card Punch

6.1. GENERAL

This section contains information for programming the byte-oriented SPERRY UNIVAC 0605 Card Punch Subsystem.

To program the card punch, which is integrated in the 90/30 system processor, reference should also be made to available supplemental information listed in program libraries. Operating information for the card punch is included in the card punch operator manual, UP-8088 (current version). Information on the card punch control is included in 2.4.2.

The card punch has an input capacity of 700 standard Electrical Accounting Machine (EAM)* thickness cards and an output capacity of 600 cards and a reject stacker with a 100 card capacity. It is located close to the processor to provide maximum accessibility and convenience for the system operator (Figure 6—1).

The card punch provides the processor with a unit that operates at a speed of 75 cards per minute (cpm) when punching a full 80 columns, or 160 cpm when punching is limited to the first 28 card columns.

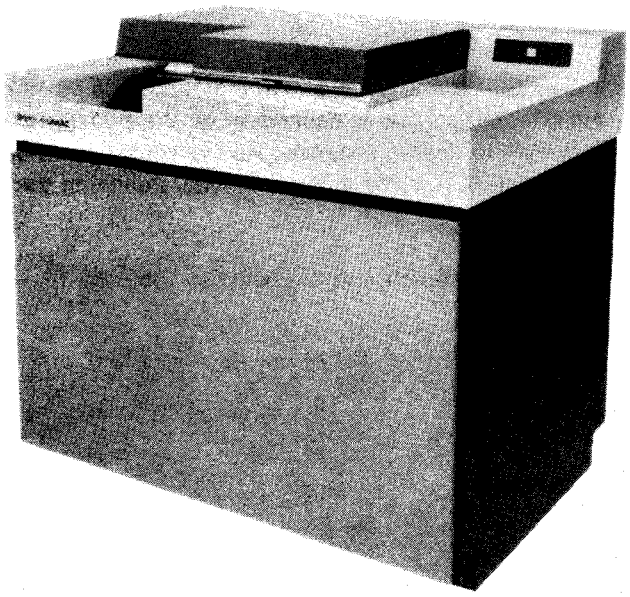


Figure 6—1. 0605 Card Punch Subsystem

*Standard card thickness = 0.007±0.0004 inches; 0.178±0.010mm

The card punch performs the following:

- receives control signals and punching data from the integrated peripheral channel (IPC);
- notifies the interface of operating conditions within the card punch unit;
- sends data read from standard EAM cards from the card read station to the IPC if the read feature is installed; and
- controls the reading of data from standard EAM cards in the addressed punch unit (if optional read station is installed).

The IPC performs the following:

- receives and interprets command information from the processor;
- transmits data to an addressed card punch unit and makes it available to the processor; and
- maintains accurate data control.

6.2. SUBSYSTEM DESCRIPTION

The card punch is an 80-column, column-oriented unit capable of feeding, punching, and checking standard EAM cards at the rate of 75 to 160 cpm (cards per minute). The card punch, together with its associated control functions, provides a complete set of status information upon termination of each command.

A translation process is performed by the card punch to prepare for either image or compressed code mode prior to punching. A read station option is available which enables the card punch to read cards prior to punching. Data is read serially, column by column, as the card passes through the read station.

6.2.1. Characteristics

The card punch mechanism is an 80-column serial punch that feeds and punches cards in 2-column increments at the rate of 75 to 160 cpm. The punch rate is dependent on the number of columns punched in each card. During punching, cards are checked to ensure accuracy. An incorrectly punched card is rejected and supplied to the reject stacker if the B bit is selected in the command code. Punching translation is provided in either the image mode or translate mode.

The performance characteristics of the punch unit are listed in Table 6—1.

Table 6—1. Card Punch Subsystem Characteristics

Parameter	Characteristics
Punch speed	75 cpm (full 80 columns) 160 cpm (punch first 28 columns) 120 columns per second through punch station
Card punch code	Image or compressed
Punch cycle time	16.6 milliseconds for every two columns punched
Card stock	Standard EAM 80-column cards
Punching mode	2-column serial translator or image mode
Checking mode	Punch motion check
Feeding mode	Column serial, on demand
Hopper capacity	700 cards
Stacker capacity	600 cards (primary stacker) 100 cards (reject stacker)
Card read feature	Allows reading of punched cards.
Read rate	160 cpm (provided no punching, or punching only the first 28 card columns)

6.2.2. Configuration

Figure 6—2 shows the system configuration, which contains an IPC and the card punch, including the read/punch option. The card punch utilizes the card punch control in the IPC. The control combines all signals and data to achieve coherent system integration between the subsystem and processor.

The basic components and optional read/punch feature are listed in Table 6—2.

Figure 6—2. Integrated Peripheral Channel and Card Punch

Table 6—2. Basic Components for the Card Punch

Unit	Description
Card punch	The card punch is an 80-column card punching device capable of punching 75 cpm. The card punch control is located in the IPC. The card punch is designed for operator intervention, and is placed close to the processor for ease of operation.
Read station	The read station is an optional feature that is either factory or field installed. It permits standard EAM cards to be read prior to punching at the rate of 160 cpm, provided that punching is confined to the first 28 card columns.

6.2.3. Card Punch Components

The card punch components consist of two card punch controls in the processor cabinet and a card punch. The IPC is a processor component which acts as a punch control, and for the purposes of this document it is considered to be a control.

When instructed to do so through the IPC, the card punch control causes the card punch to perform punching (or read/punching if the read option is installed) on standard EAM card stock. Prior to operation, the card punch must be primed by pressing the FEED switch on the control panel (Figure 6—3) while the punch is in the stop state. This causes one card to be picked from the hopper and placed in the advance station, which then advances the card to the punch mechanism. Subsequent card movement is now under program control. Upon receipt of a write command from the processor, the card at the punch station (where data is stored in odd-even punch buffers) is punched two columns at a time (one odd column, one even column). Cards are fed from the punch station to the stackers by a pinch roll located directly to the left of the punch station. Refer to Figure 6—4 for punched card format.

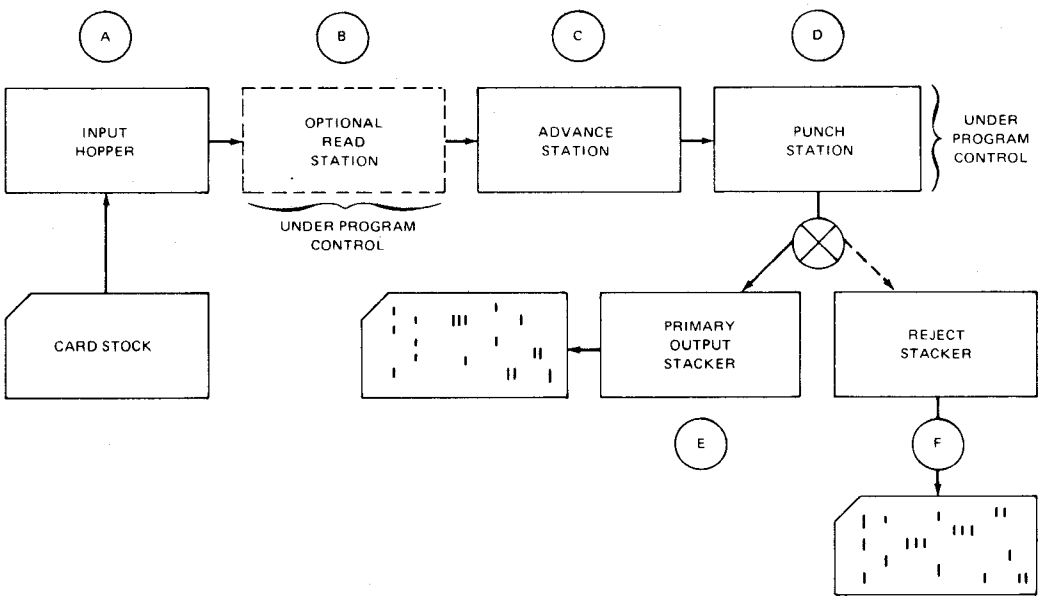
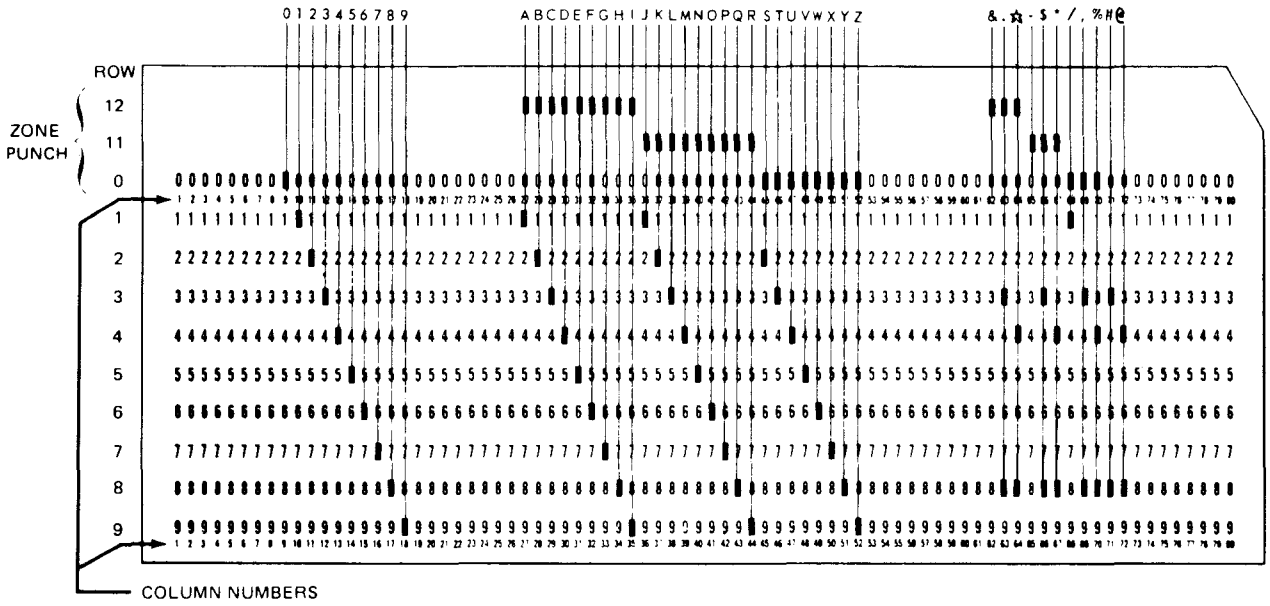


Figure 6—3. Card Punch, Block Diagram



NOTES:

1. The standard EAM punched card has 12 horizontal rows and 80 vertical columns. One character can be punched into each column. The maximum number of characters that can be punched into an EAM card is 80.

2. Each numeric, alphabetic, and special character can be represented in expanded card code by one, two, or three holes punched in a column as shown in the EAM card. This EAM card is shown only in compressed card code.

3. A zone punch (12, 11, or 0) is included in the punched-hole code of each alphabetic and special character.

Figure 6—4. Punch Card Format

6.2.3.1. Hopper

The hopper (Figure 6—3) has a capacity of 700 standard EAM cards. It is positioned so as to be easily accessible by the operator. Cards are placed in the hopper with the print side (face) to the front and row 9 at the bottom. They are then transferred from the hopper to the advance station by means of a feed roll. Once in the advance station, the cards face front with column 1 to the left.

6.2.3.2. Optional Read Station

Cards are passed through the read station (Figure 6—3) as they are transferred from the hopper. As the card enters the read station, it is "sprocketed" from its own leading edge (i.e., a pulse generated by the card serves as the timing mark for reading the card). Data is read in serial form, column by column, as the card passes through the read station. The read rate is approximately 160 cpm. On read/punch commands, the rate is 160 cpm, provided that punching is confined to the first 28 columns. The read data transfer rate is 1 column every 1.5 milliseconds.

6.2.3.3. Advance (Wait) Station

The advance station (Figure 6—3) is idle except when required to advance the card through the punch station. The card is advanced in 2-column increments by a card pushing mechanism, which consists of spring steel pusher blades attached to an oscillating platform. The advance rate is approximately 120 columns/second.

6.2.3.4. Punch Station

The punch station (Figure 6—3) contains 2 columns of 12 punches each (1 punch for each of the 12 positions per card column). As each card is fed from the advance station, it is registered for punching in columns 1 and 2 (i.e., it is accurately positioned relative to an internal reference point). It is then advanced under the punch die in 2-column increments by oscillating pusher blades located with the advance station mechanism.

6.2.3.5. Primary Stacker

The primary stacker (Figure 6—3) has a capacity of 600 standard EAM cards and is equipped with a follower block that rides in a slot in the base of the stacker. Cards are fed into the primary stacker face forward, with row 9 at the bottom. The primary stacker is equipped with a stacker-full detection device. The primary stacker is also equipped with a follower block misposition sensor which is activated if the follower block is not properly positioned by an operator. This prevents card spills during punching operations.

The primary stacker is automatically activated when stacking is required. Cards are fed from the punch station to the stackers by means of a pinch roll. The pinch roll enables the cards to be ejected from the advance mechanism through the punch station to either the primary or reject stackers when as few as 28 columns are punched.

6.2.3.6. Reject Stacker

The reject stacker (Figure 6—3) has a capacity of 100 standard EAM thickness cards and is also equipped with a stacker-full detection device (6.2.3.5). The reject stacker is selected by simply energizing the reject stacker select gate. The reject stacker can also be selected by a combination of a command bit being set and a punch check or punch overrun.

6.2.3.7. Image Mode Punching

Punching cards in the image mode permits the punching of two bytes of binary data represented on each column of the 80-column card (Figures 6—5 and 6—6). To punch two bytes on one column, the two most significant bits of each data byte received from the IPC are disregarded. The remaining least significant six bits of each byte are punched on half of a column. For example, data byte 1 would be represented on the lower half of a column, and data byte 0 would be represented on the upper half of the same column. Thus, 80 columns of a punched card can represent a total of 160 bytes of binary data. A card punched in the image mode contains a one-to-one representation of binary data (that is, a punch represents a binary 1 and no punch represents a binary 0).

If the prepunch read feature is used, one column of data read is assembled from two 6-bit bytes into two 8-bit bytes. To present a complete 8-bit byte, zeros are added to bits 0 and 1.

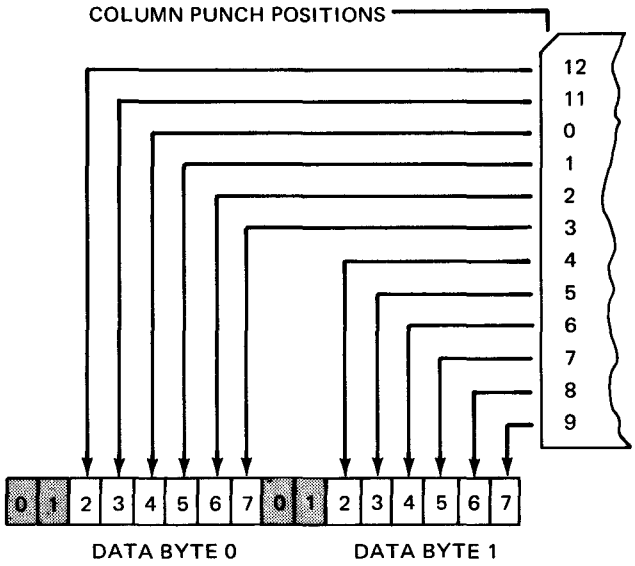


Figure 6—5. Image Mode Translation (Binary Column)

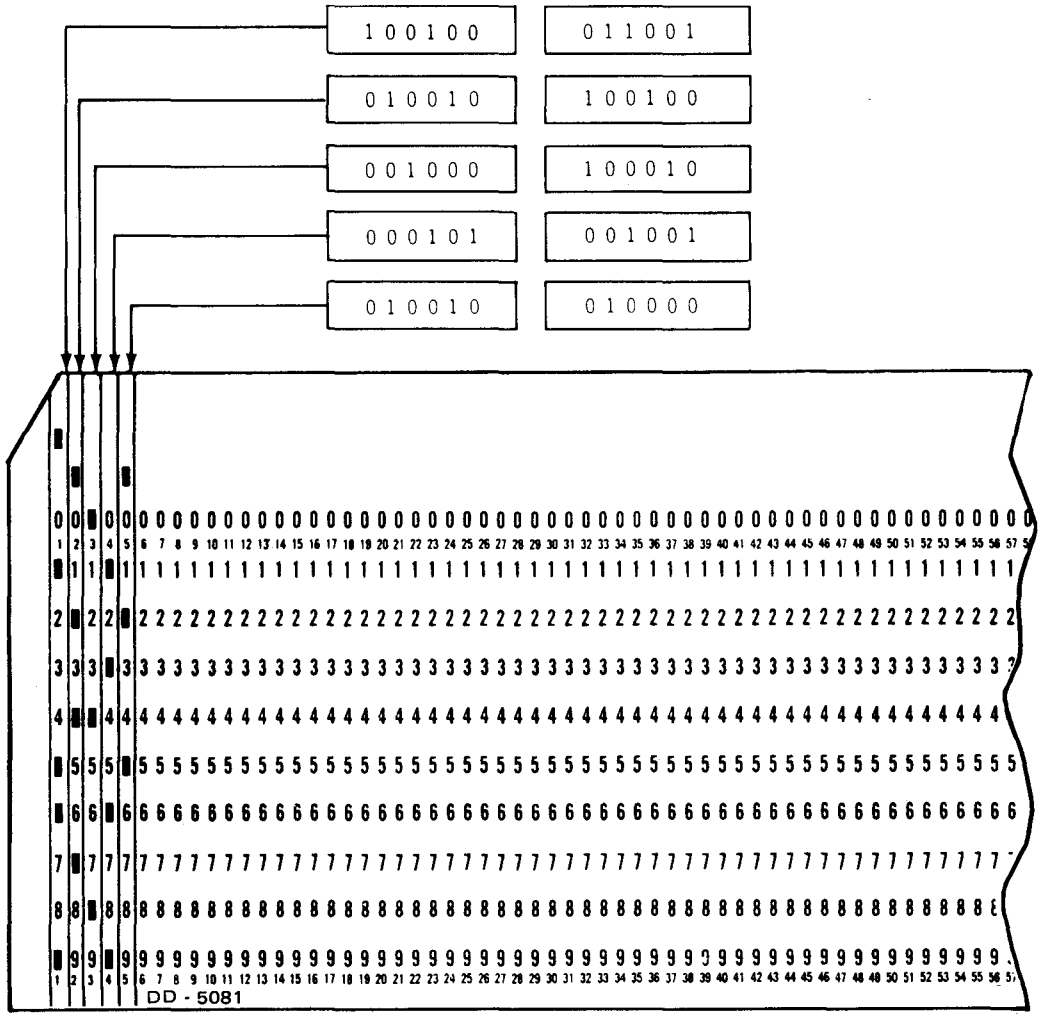


Figure 6—6. Relationship of Data Bytes to Card Punches (Image Mode)

6.2.3.8. Accuracy Control

As a card is punched, it is checked to ensure accuracy. Incorrectly punched cards are rejected, and the correct data is punched on the following blank card. Again, a card is rejected only if the B command bit is set to 1, otherwise the stop state results. The card is only repunched if the program tells the punch to punch a card and then the program must provide the punch with the same data as before.

Because the serial punch is an integral part of the processor, the control circuitry and indicators are located on the processor maintenance panel.

6.2.4. Card Punch Control

The card punch control, connected between the IPC and punch device, controls and monitors the operation of the serial punch mechanism.

1. Data is transferred in Hollerith code from the processor main storage by way of the IPC to the card punch control. The transferred data is punched on a card fed from the wait-and-advance station. To ensure that the card is punched correctly, the punch control receives and interprets signals from the punch check unit as the card is being punched.

2. At the completion of the punch operation, the card punch control transfers the punched card to either the normal stacker or the reject stacker.

3. If the read/punch option is installed and cards are to be read, a card is fed through the read station to the wait-and-advance station. As the card passes through the read station, data is read in either the image mode or the translate mode and applied to the card punch control which transfers the data by way of the IPC to the assigned processor main storage area.

4. The card just read is now located in the wait-and-advance station and will be punched if so instructed by the next command.

5. The previously stated process is repeated for each command.

The card punch control, comprised of control logic and data paths, is designed to perform the following functions:

- supply signals which prepare the punch mechanism for punch or read/punch operations;
- synchronize the flow of data to and from the punch mechanism; and
- detect and interpret signals, both normal and abnormal, from the punch mechanism.

When the serial punch is conditioned for a punch operation, and a card has been advanced to the wait station so it is ready to enter the punch station on command from the processor, the card punch control initiates and controls operations.

6.3. PROGRAMMING

The card punch control provides the card punch subsystem with the ability to perform the punch/read operations. It also transfers data and status information between the card punch unit and the IPC.

The IPC performs all main storage accesses, buffer control word (BCW) manipulations, I/O presentation, and status sequences required for the operation of the card punch control.

The card punch control responds to one device address for both punch and read operations. To allow concurrent output data transfers (punch) and input data transfers (read), the active fields of the BCW control the punch operations, and the replacement fields of the BCW control the read operations. When sense data is to be presented, the active fields of the BCW must be used to specify the byte count, main storage address, and termination. An 8-bit data path is provided between the IPC and the card punch. Command codes and data are sent from the IPC to the card punch control. Status, sense, and data (read station feature) information is sent from the card punch control to the IPC.

6.3.1. Data Transfer Rate

Response time extends from the time of status generation in the card punch control until the next control to feed a card is received by the card punch control. To maintain maximum throughput (Table 6—3), the response time cannot exceed 3 milliseconds.

Table 6—3. Card Punch Throughput Rate

Operation	Columns	Rate (cpm)
Punching	29–80	Varies between 75 and 160 cpm, depending on the number of columns punched
Punching	1–28	160 cpm
Reading	1–80	160 cpm

NOTES:

1. The rates in Table 6—3 are maximum values. Read operations may occur concurrently with punching operations while utilizing the maximum values. To maintain the 160 cpm rate while reading, only 28 card columns may be punched.

2. The time between successive data requests when punching cards is approximately 16.6 milliseconds for every two columns punched. However, the time to respond to the punch data request must be less than 400 microseconds.

3. The time between successive data requests is approximately 1.4 milliseconds for every card column read. However, the time to respond to the read data request must be less than 1.18 milliseconds. Failure to meet the response times produces an overrun condition for the specified operation and terminates data transfers immediately. If both reading and punching are specified, only the operation for which the overrun occurs is terminated; the other operation proceeds to normal completion. Status is presented at the normal ending point, and the card punch control enters a stop condition when the status is accepted by the IPC.

6.3.2. Data Transfers

Once the card punch control command is accepted by the card punch, the following action is initiated by the card punch control:

1. Decode the command.
2. Start card movement inside the advance (wait) station.
3. Request data from the IPC and punch a card (if punching is specified) or initiate transport of a card to the stacker (read operation only).
4. Feed the next card located with the hopper (card n + 1).
5. Read card n + 1 (if reading is specified and read feature is installed). Data requests for punching and reading may overlap cards n and n + 1 if both operations are specified.
6. Card n is transported to the stacker; card n + 1 remains at the advance station until the next control command is executed.
7. When the trailing edge of card n + 1 is detected at the read station and punching is complete on card n, the card punch control generates the required status signal and transmits it to the processor via the IPC.

When the card punch control has data available for transfer to the IPC or requires data for punching, service is requested from the IPC.

The IPC services the data requests on a priority basis. Two card columns are punched at a time requiring the access of two or four bytes of data from the IPC, based on whether the translate mode or image mode (respectively) of punching is specified.

One card column is read at a time resulting in the transfer of one or two bytes of data to the IPC, based on whether the translate mode or image mode of reading is specified.

6.3.2.1. Translate Mode Punch Data Format

When the translate mode is specified, the following restrictions apply.

1. The byte count must be even.
2. The main storage address must start on a half-word boundary.
3. The first column is punched from the byte contained in the most significant half of the half word.
4. The next column is punched from the byte contained in the least significant half of the half word.

Translation for the punch operation is EBCDIC to extended card code.

6.3.2.2. Translate Mode Read Data Format

In translate mode, each card column read results in the transfer of one byte of data to the IPC. Translation of the card data is extended card code to EBCDIC.

6.3.2.3. Image Mode Punch Data Format

When utilizing the image mode, each byte received from the IPC will have the two most significant bits stripped off the card punch control. Two card columns are punched at one time; therefore four bytes of data must be transferred from the IPC. The following restrictions apply to the word transfers:

1. The byte count must be even.

2. The main storage address must start on a half-word boundary.

3. The top half of the column is punched from the byte contained in the most significant half of the half word.

4. The lower half of the column is punched from the byte contained in the least significant half of the half word.

Each card column punched appears as shown in Figure 6—7.

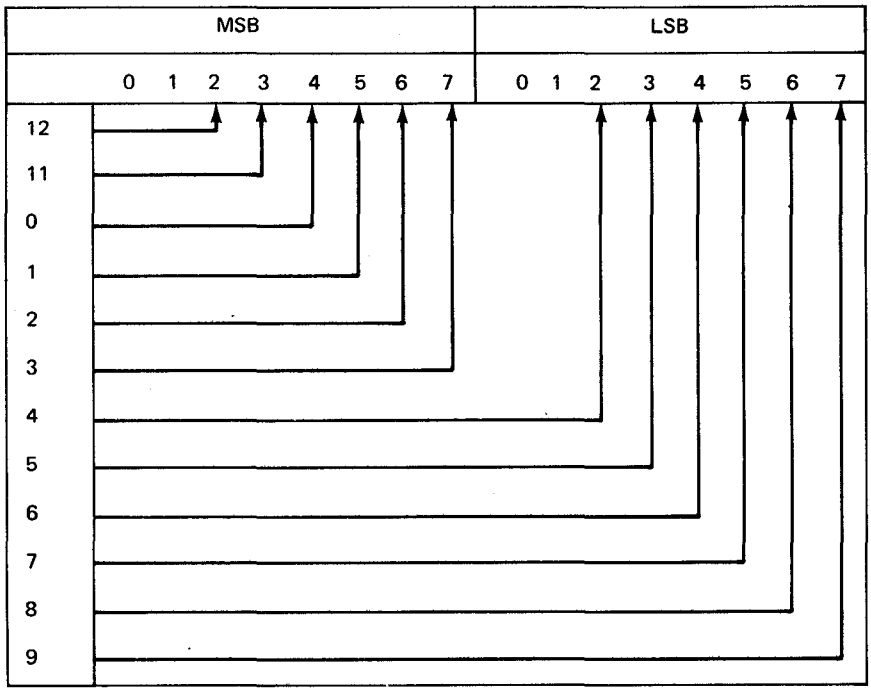


Figure 6—7. Image Mode Byte Contents

6.3.2.4. Image Mode Read Data Format

When utilizing the image mode of reading cards, each card column results in the transfer of two bytes of data to the IPC. The following restrictions apply to the half-word transfers:

1. The byte count must be even.
2. The main storage address must start on a half-word boundary.
3. The first byte (rows 12, 11, 0, 1, 2, and 3) is always stored in the most significant half of the half word.
4. The second byte (rows 4, 5, 6, 7, 8, and 9) is always stored in the least significant half of the half word.

The 8-bit bytes transferred to the IPC have the two most significant bits padded with 0's. The six least significant bits of the two adjacent bytes contain one column from the card (Figure 6—7).

6.3.3. Card Punch Commands

The command codes listed in Table 6—4 may be issued to the card punch control by the processor to initiate data transfers or to interrogate the control about the card punch status.

Table 6—4. Card Punch Commands

Bit / Command	0	1	2	3	4	5	6	7
Control	A	B	X	X	E	F	R	P
Sense	X	X	X	X	0	1	0	0

LEGEND:

X = Bit is ignored by the subsystem control.

A, B, F, R, P = Modifier bits

E = A modifier bit and is used for diagnostic testing only; normal operation of the card punch is dependent on the use of this modifier bit. This bit is ignored if P = 0.

Command codes that are not specified in Table 6—4 are rejected by the card punch control, and result in unit check status being presented to the IPC. The card punch does not become active.

6.3.3.1. Control Command

The control command is used to initiate the feeding, punching, or reading of a card. The card punch control becomes busy to any other interrogation from the time the control command is accepted, until the status byte is presented and accepted by the IPC.

Interpretation of the control command depends on the definition of the modifier bits as indicated in Table 6—5.

Table 6–5. Card Punch Modifier Bits

Definition Number	Modifier Bit	Definition
1	A=0	Normal punch/read operation.
2	A=1	Diagnostic use only.
3	B=0	Stop on error.
4	B=1	Sort errors and remain in run state.
5	E=0	Normal punch operation.
6	E=1	Select reject stacker.
7	F=1	Punch or read in translate mode.
8	F=1	Punch or read in image mode.
9	P=0 R=0	Invalid code.
10	P=0 R=1	A read operation is specified with no punch operation.
11	P=1 R=0	A punch operation is specified with no read operation.
12	P=1 R=1	A punch and read operation is specified.

Definition of modifier bits listed in Table 6—5:

1. Normal punch/read operation (self-explanatory).

2. Diagnostic use only (self-explanatory).

3. Stop on error. A specified operation in which conditions causing a unit check status to be presented at the completion of the command cause automatic entry into the stop state.

4. Sort errors and remain in run state. A unit check status, generated by a punch overrun (SB0,5) or punch check (SB1,4), is presented upon completion of the command. The card leaving the punch station is routed to the reject stacker. This particular mode applies to punch operations only. All read errors cause operation in the stop on error mode (B-bit ignored).

5. Normal punch operation (self-explanatory).

6. Select reject stacker. Terminates data transfers and ejects the card based on the punch data (diagnostic mode only).

7. Punch or read in translate mode. The extended card code EBCDIC translator has been selected. Refer to Table 6—6.

8. Punch or read in image mode (self-explanatory).

9. Invalid code. This results in a command reject.

10. A read operation is specified with no punch operation. This code is invalid if the read station feature is not installed. This results in a command reject.

11. A punch operation is specified with no read operation (self-explanatory).

12. A punch and read operation is specified. This code is invalid if the read station feature is not installed. This results in a command reject.

Successful completion of the control command is indicated by device end status presented to the IPC. Any error detected during the specified operation is indicated by unit check and device end status.

The control command is executed by the card punch control when the device is in the run state. A control command issued when the device is in the stop state does not initiate an operation and unit check status is presented to the processor.

Early termination of punch/read operations may be specified via the BCW T bit set to 1, or the byte count has decremented to 0. Read or punch operations may be terminated independently via the active (punch) or replacement (read) fields of the BCW. Early termination results in normal ending status being presented, and may be used to feed a card without a data transfer (T bit set in the BCW).

Table 6–6. Extended Card Code Hexadecimal Translation (Part 1 of 2)

No.	Zones							
	Blank	12	11	0	12–11–0	12–11	12–0	11–0
Blank	40	50	60	F0	70	6A	C0	D0
1	F1	C1	D1	61	B1	91	81	A1
2	F2	C2	D2	E2	B2	92	82	A2
3	F3	C3	D3	E3	B3	93	83	A3
4	F4	C4	D4	E4	B4	94	84	A4
5	F5	C5	D5	E5	B5	95	85	A5
6	F6	C6	D6	E6	B6	96	86	A6
7	F7	C7	D7	E7	B7	97	87	A7
8	F8	C8	D8	E8	B8	98	88	A8
9	F9	C9	D9	E9	B9	99	89	A9
18	79	49	59	69	B0	90	80	A0
28	7A	4A	5A	E0	BA	9A	8A	AA
38	7B	4B	5B	6B	BB	9B	8B	AB
48	7C	4C	5C	6C	BC	9C	8C	AC
58	7D	4D	5D	6D	BD	9D	8D	AD
68	7E	4E	5E	6E	BE	9E	8E	AE
78	7F	4F	5F	6F	BF	9F	8F	AF
19	31	01	11	21	71	51	41	E1
29	32	02	12	22	72	52	42	62
39	33	03	13	23	73	53	43	63
49	34	04	14	24	74	54	44	64
59	35	05	15	25	75	55	45	65
69	36	06	16	26	76	56	46	66
79	37	07	17	27	77	57	47	67
89	38	08	18	28	78	58	48	68
189	39	09	19	29	30	10	00	20
289	3A	0A	1A	2A	FA	DA	CA	EA
389	3B	0B	1B	2B	FB	DB	CB	EB

Table 6–6. Extended Card Code Hexadecimal Translation (Part 2 of 2)

No.	Zones							
	Blank	12	11	0	12–11–0	12–11	12–0	11–0
489	3C	0C	1C	2C	FC	DC	CC	EC
589	3D	0D	1D	2D	FD	DD	CD	ED
689	3E	0E	1E	2E	FE	DE	DE	EE
789	3F	0F	1F	2F	FF	DF	CF	EF

NOTE:

Hexadecimal equivalents for zone and digit combinations not listed in Table 6—6 are not valid, and produce a validity check error if detected during a read in translate mode.

Zones are rows 12, 11, 0. Digits are rows 1, 2, 3, 4, 5, 6, 7, 8, and 9.

6.3.3.2. Sense Command

The sense command is used to interrogate the card punch control, and to store data in main storage which reflects unusual conditions detected during the last operation. The command is executed regardless of the state of the card punch and may be issued independently or as a response to unit check status. With the device in the run state, some sense indications may be cleared upon acceptance of a command other than sense. Failure to issue the sense command as a response to a status indication may result in the loss of the condition within the card punch. As a result of the sense command, the card punch control transfers two sense bytes to main storage. The first one contains summary information; the second contains detailed information of the device and control indicated. The control is terminated and presents device end status to the IPC upon successful transfer of the second sense byte.

If the sense command is issued with the BCW count (A) set to 1, the control transfers two sense bytes, but only the first sense byte is stored. If the sense command is issued with the BCW T (A) bit set to 1, no sense bytes are transferred. In either case, normal ending status is presented to the IPC. Unit check status is never set with device end for a sense command. The replacement fields of the BCW are ignored during sense data transfers.

6.3.4. Card Punch Status

The status byte, which supplies information pertaining to the state of the card punch control, is presented to the IPC, and is stored as an I/O status table interrupt word (IOSTIW) in the buffered channel status word (BCSW) field (3, 5):

- as a unit check in response to the start-I/O instruction (SIO) sequence;
- at the completion of a command; or
- if an attention condition is detected.

The status register in the card punch control is cleared when the IPC accepts the status byte. Status generated during the SIO sequence causes the IPC to return the appropriate condition code to the processor and, if the command was rejected, a subsequent status sequence causes the IPC to store an IOSTIW. The status bits and their meaning are listed in Table 6—7.

Table 6—7. Card Punch Status Byte

Bit Position	Designation	Definitions
0	Attention	Indicates transition from the stop state to the run state.
1	N/A	Set to 0 by the card punch.
2	N/A	Set to 0 by the card punch.
3	N/A	Set to 0 by the card punch.
4	N/A	Set to 0 by the card punch.
5	Device end	Indicates the completion of a command initiated by the IPC and readiness to accept a new command.
6	Unit check	Indicates at least one bit is set in sense byte 0.
7	N/A	Set to 0 by the card punch.

6.3.5. Card Punch Sense Data Bytes

The card punch employs two sense data bytes to indicate the operating conditions that occur when punching cards. These bytes are listed in Table 6—8.

Table 6–8. Card Punch Sense Data Bytes (Part 1 of 2)

Bit Position	Designation	Definition
		Byte 0
0	Command reject	Set to 1 if an invalid command is issued, see 6.3.3.1. Unit check status set and control not active.
1	Intervention required	Set to 1 if a condition is detected requiring manual intervention.
2	N/A	Set to 0 by the control.
3	Equipment check	Set to 1 if a card transport error has been detected. Following conditions cause card transport error: a. The advance wait station light sensor indicated a lit condition prior to feeding the card from the advance station to the punch station; b. A card was fed through the read station, but leading edge failed to be detected by the pre-punch sensor; c. A card was pushed through the punch station, but leading edge of card failed to be detected by the post punch light sensor after the card was pushed 34 columns; d. The eject card rollers were activated to transport a card to the output stacker but the post light sensor did not switch from dark to light within 250 milliseconds; e. A card is in the read station for more than 150 milliseconds or any read station sensor is dark at column 84; f. A card was fed from the advance station through the punch station, but the prepunch sensor did not switch from dark to light after the fifth punch on the card.
4	Data check	Set to 1 if any of the following conditions exist: a. Column 0 error (SB1,0) b. Validity check error (SB1,1) c. Strobe error (SB1,2) d. Punch error (SB1,4)
5	Overrun	Set to 1 if an overrun condition on punch or read data transfers is detected. Data transfers for the current operation are terminated.
6	Stop state	Set to 1 if the subsystem is in the stop state. The subsystem may enter this state by way of the stop switch, or an error condition such as specified under data check error conditions.
7	Device check	Set to 1 if the subsystem has detected an interlock active. If device check occurs during a command, the command is immediately terminated.

Table 6–8. Card Punch Sense Data Bytes (Part 2 of 2)

Bit Position	Designation	Definition
Byte 1		
0	Column 0 error	Set to 1 if read station feature is installed and any one of the 12 read stations detect a punch between the leading edge of a card and column 1.
1	Validity check error	Set to 1 if, when in translate mode, more than one punch per column is present in rows 1 through 7.
2	Strobe error	Set to 1 if the read station feature is installed and a strobe signal detected incorrect data.
3	Misfeed error	Set to 1 if a card failed to feed from the card reader input hopper.
4	Punch check error	Set to 1 if a mismatch occurs during the punch cycle, when the punch check performs an accuracy check.
5	N/A	Set to 0 by the control.
6	Read station feature	Set to 1 if feature is installed, otherwise set to 0 by the control.
7	N/A	Set to 0 by the control.

7. Printer

7.1. GENERAL

This section contains information for programming the SPERRY UNIVAC 0773 Printer Subsystem (0773 printer). Information on the printer control is included in 2.4.5. To program the printer, which is integrated in the 90/30 system processor, reference should also be made to available supplemental information listed in program libraries for the 90/30 system.

The 0773 printer (Figure 7—1) provides the processing system with a medium speed online output. Line printing is accomplished with an operator-replaceable print band cartridge. All printer control elements are connected through a special interface to the processor. The printer operates at throughput rates of approximately 110 to 680 lines per minute (lpm), depending on the type font cartridge specified. The minimum rate for a standard 48-character set is 500 lpm.

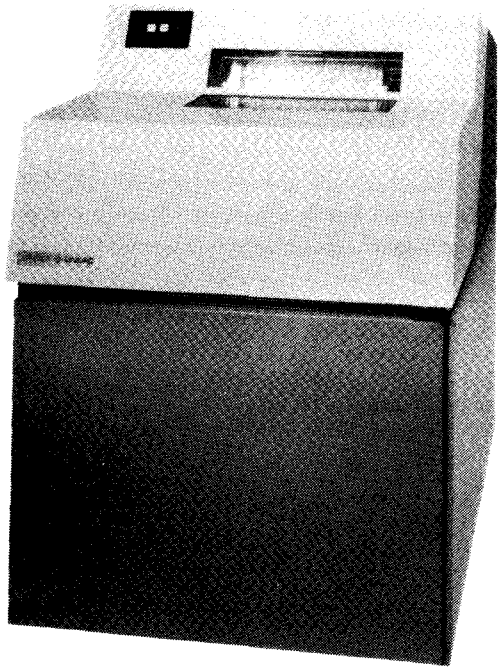


Figure 7—1. 0773 Printer

Besides these functional capabilities, other areas of interest to the programmer include:

- printing is from a metallic print band moving continuously in a horizontal direction;
- vertical format buffer loaded by program and capable of being reset by the operator;
- program identification, according to the number of characters, of the print band;
- form overflow* indication; and
- operation checking capabilities which include:
  - parity check
  - invalid command check
  - load code buffer check
  - vertical format buffer check
  - forms low check
  - forms out check
  - ribbon condition check
  - device check
  - print actuator check
  - print overrun check

7.2. SUBSYSTEM DESCRIPTION

The printer is an integrated unit designed for use specifically with a 90/30 processor. The printer is intended for electronic integration into a 90/30 system but is removable from the system. The printer prints alphanumeric data and responds to a 10-command repertoire to permit a versatile combination of functions.

7.2.1. Characteristics

The characteristics for the printer are listed in Table 7—1.

*Form overflow is not an error condition, but a code loaded with the vertical format buffer (VFB), which, when detected while advancing forms by line count, produces unit exception status, signaling the program that the end of the page has been reached so that the page number and similar information can be printed before reaching the home paper position.

Table 7—1. Printer Characteristics

Item	Characteristics
Minimum specified printing rate (single line spacing)	48-character set 500 lpm 64-character set 400 lpm 48/16-character set* 400/670 lpm 85-character 310 lpm 128-character set 217 lpm 96- (16—16) character set* 217/500 lpm 256-character set 114 lpm
Forms advance time in milliseconds (maximum)	6 lpi (2.36 lines per cm) / 8 lpi (3.15 lines per cm) single line 16.0 / 14.2 double line 23.6 / 19.9 triple line 31.2 / 25.6 n+1 line 16.0 + 7.6n / 14.2 + 5.7n Indicated times for multiline advances correspond to a normal forms advance (slew) rate of 22 inches (558.8 mm) per second.
Horizontal print spacing	10 print positions per inch (2.54 mm per print position)
Vertical line spacing	Either 6 lpi (4.23 mm per line) or 8 lpi (3.17 mm per line), as determined by the operator.
Number of characters	Standard 48- or 64-character set, with 5 sets on a 240-character band; or up to 256 characters with expanded character set control feature; 48-character set band repeats 5 times resulting in 240 characters; 64-character set band repeats 4 times resulting in 256 characters. Expanded character bands contain 256 characters and require optional feature.
Ribbon feed	Bidirectional, self-reversing; ribbon removable without rewinding
Ribbon	Fabric and plastic film ribbons: 13.25 inches (336.5 mm) wide for 120 columns 14.50 inches (367.3 mm) wide for 132 columns 15.75 inches (400.0 mm) wide for 144 columns
Codes	EBCDIC, ASCII, or any 8-bit code
Forms	Continuous single-part and multipart (up to six parts or up to 0.018 inch (0.456 mm) thick) with standard edge sprocket holes. Printer can also accept continuously sprocketed, 1-part card stock forms of weights typically used for punch cards, postcards, or offset masters. Form widths from 4.0 inches (101.60 mm) to 18.75 inches (476.2 mm) and lengths up to 24 inches (609.6 mm) can be accommodated. Forms longer than 17 inches (431.8 mm) can be run with casework door open, but noise level increases with door open.
Print positions	120 or 132 print positions, and 144 print positions (optional features required for all except 120 positions)

*The "16" array is commonly a numeric subset. Extra 16 arrays are included in the 96/16—16 arrangement to make up the total number of 256 characters in a band.

7.2.2. Configuration

The printer subsystem consists of a single unit equipped with the necessary components to operate with the 90/30 processor. The printer is electronically connected to the processor through an integrated peripheral channel (IPC) and appropriate interface hardware. Figure 7—2 illustrates the functional arrangement of the printer and processor. Figure 7—3 illustrates the printer configuration. The printer types and optional features are listed and described in Table 7—2.

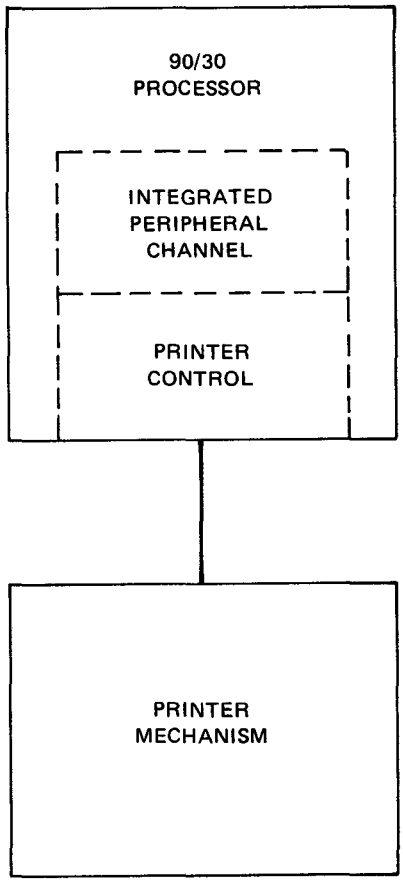


Figure 7—2. Printer Functional Arrangement

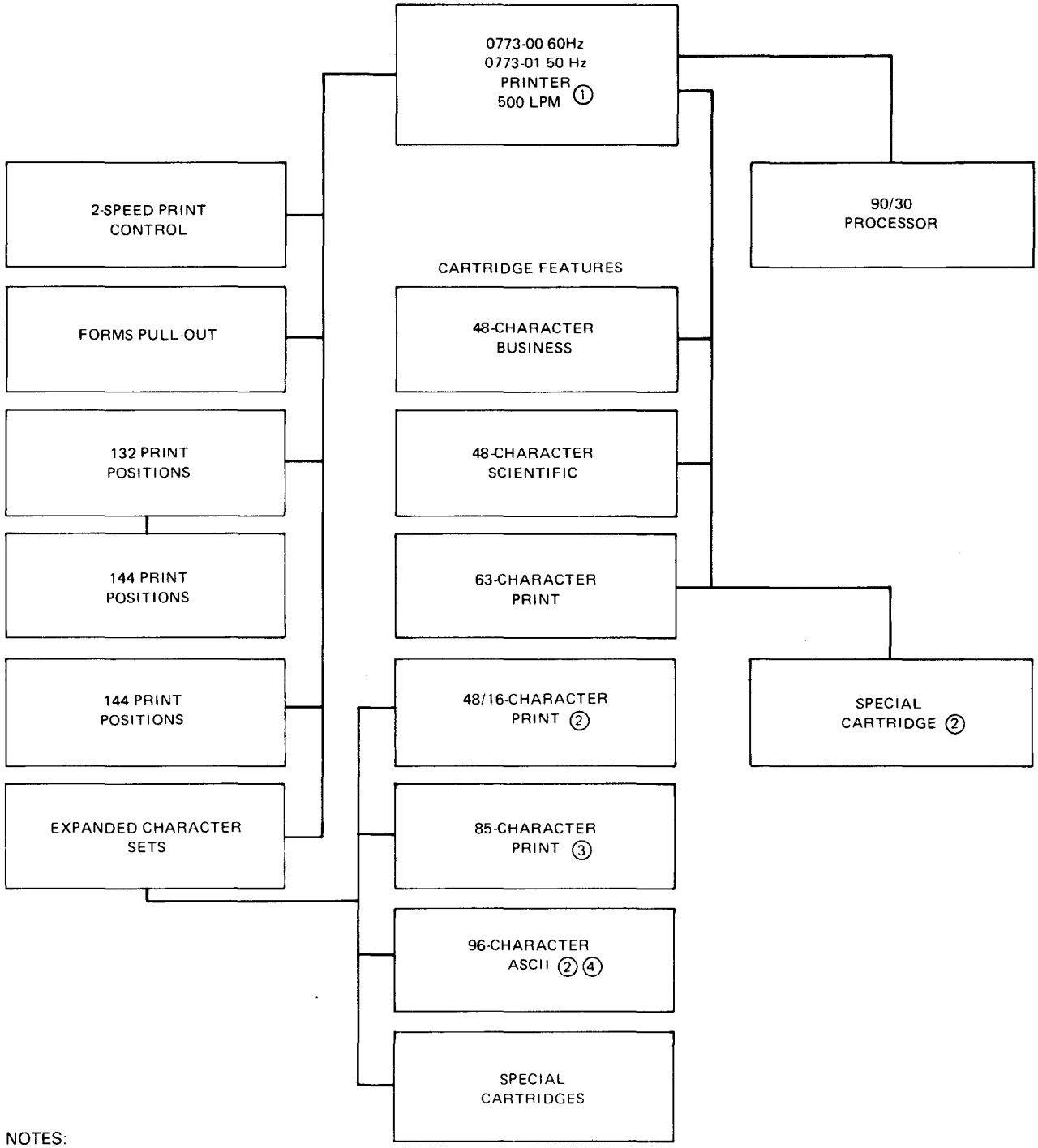
7.2.2.1. Print Font Styles

Standard character fonts for the eight print cartridges listed in Table 7—2 comply, in general, with the font specified for OCR—B characters or 77L font styles. Appendix B lists the characters for each cartridge type, as well as the loading sequence.

7.2.2.2. Print Character Sets

Characters in each print band used on the printer must be loaded by program in proper sequence. The character sets for each print cartridge included in Table 7—2 are listed in Appendix B in the same sequence in which the character codes must be entered into the load code buffer.

The character symbol shapes illustrated in Appendix B do not necessarily conform with actual printed shapes, but are provided only for informational purposes.



NOTES:

① 48-character font

② Expanded character set feature is a prerequisite.

③ 85-character print cartridge provides a faster print rate than 96-character print cartridge.

④ 96-character ASCII is a 128-character set in a 96/16—16 arrangement.

Figure 7—3. Printer Configuration With Optional Features

Table 7—2. Printer Type and Optional Features (Part 1 of 2)

Item	Description
Printer	Prints a 48-character set at 500 lpm, single spaced, with an operator-changeable print cartridge. There are 120 print positions per line, expandable to 132 print positions with feature (factory installed) and up to 144 print positions with feature (factory or field installed). Vertical spacing is 6 lpi (4.23 mm per line) or 8 lpi (3.17 mm per line). Maximum forms advance (slew) rate is 22 inches per second (558.8 cm per sec). A minimum of one print cartridge feature must be ordered. Additional type cartridges are available on a feature or special order basis. Type 0773—00 operates on 60Hz power. Type 0773—01 operates on 50Hz power.
2-speed print control	Provides capability to print at approximately half speed to optimize for unusually demanding requirements (such as multilith masters).
132 print positions	Provides additional print positions by expanding the standard 120 print positions to 132 print positions. Factory or field installable.
144 print positions	Provides additional print positions by expanding from 132 print positions to 144 print positions. The 132 print position feature is a prerequisite. Factory or field installable.
144 print positions	Provides additional print positions by expanding from 120 print positions to 144 print positions. Factory or field installable.
Expanded character sets	Provides for type cartridges containing character set arrays greater than 64.
Business cartridge	Contains one 48-character alphanumeric business set. Font style is 77L.
Scientific cartridge	Contains one 48-character alphanumeric scientific set. Font style is 77L.
63-character print cartridge	Contains a 63-character alphanumeric set compatible with the 9200/9300 series as an additional cartridge. One character is repeated in each set to make a full set of 64 characters. Font style is 77L.
Special cartridges	Custom type cartridges may be ordered. In addition, the following are available: ■ OCR—A Print Cartridge (48 characters) ■ United Kingdom Cartridge (48 characters) ■ Norwegian-Danish Cartridge (48 characters) ■ Swedish-Finnish Cartridge (48 characters) ■ Norwegian-Danish Cartridge (64 characters); one character is repeated in each set to make a full set of 64 characters. ■ Swedish-Finnish Cartridge (64 characters); one character is repeated in each set to make a full set of 64 characters. ■ Katakana (63 characters) ■ 48/16 numeric ■ H—14 (63 characters) ■ OCR—B ISO (63 characters) ■ OCR—B (63 characters) ECMA—11 (63 characters) ■ OCR—A (63 characters) ECMA—11 ■ Business Portuguese (46 characters) ■ Business Spanish (46 characters)

Table 7—2. Printer Type and Optional Features (Part 2 of 2)

Item	Description
85-character print cartridge	Contains an 85-character uppercase/lowercase alphanumeric set with one redundant character. Nominal print rate is 310 lpm. Font style is OCR—B.
96-character ASCII cartridge	Contains the 96-character ASCII set including redundant characters. Nominal print rate is 217/500 lpm. 96/16 Finland/Sweden 128 Japan Katakana
Special cartridges	Custom type cartridge may be ordered. These special cartridge features are made according to a users need.
Forms pull-out	Provides for power assisted forms output stacking rollers.

7.2.3. Printer Control

The basic components comprising the printer are the intimate electronics and logic section, and the print mechanism. A minimum of logic circuitry is included in the printer. Most control functions are performed in the printer control (2.4.5).

Operation of the printer is governed by the printer control (Figure 7—4). The printer control (located in the processor) accepts commands from the processor or requests data for printing or storing. Once a command is accepted, the printer control is busy and cannot accept further commands until the command being executed is complete. Semiconductor type storage is used for buffering print data (print line buffer), character coding (load code buffer), and forms advance control codes (vertical format buffer). Status and sense bytes are supplied by the printer control to the processor.

Printer control also provides the functional characteristics for the device to synchronize print operations for the various type fonts and to advance forms under program control.

Functions of printer control are to:

- provide storage (buffers) for printing and forms control; and
- transfer data to and from the buffers on command.

A total of 256 buffer storage locations (each 10 bits including parity) is provided for use as follows:

- print line buffer: 144 locations;
- vertical format buffer: 48 locations; and
- basic load buffer: 64 locations.

An expanded load code buffer (256 locations) is provided with the expanded character set feature which also expands the VFB to 64 buffer storage locations and allows using 24-inch long forms spaced at 8 lpi.

The printer control is connected to the processor via the integrated peripheral channel (IPC) and interface hardware. An 8-bit data path (plus parity) is provided between the IPC and printer control. Command codes and data are sent from the IPC to printer control. Status, sense, and data information (buffer contents) are sent from printer control to the IPC.

The printer control includes the following logic circuitry:

- A channel interface logic circuit generates control signals for interfacing and storing status and sense bytes, and for receiving data and decoding received commands.
- An execution data path controls printing or interaction between the print line and load code buffers.
- A timing and synchronization control circuit provides timing control for the printer.
- Vertical format logic contains a buffer, the data path, and control for vertical formatting of forms and detection of forms movement errors.
- Print mechanism interface logic directly controls various portions of the print mechanism.

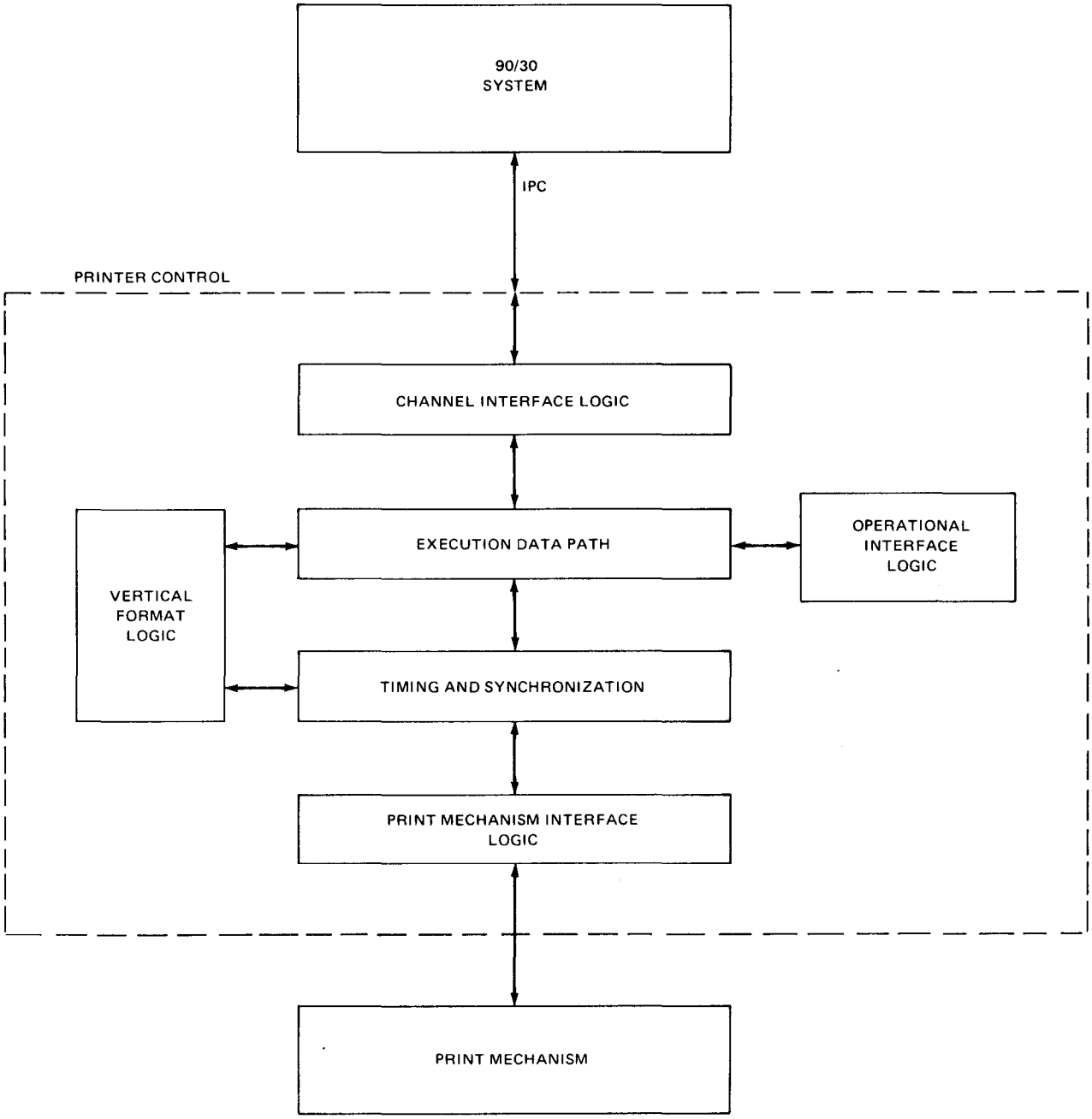


Figure 7—4. Printer Control Circuitry

7.2.3.1. Print Line Buffer

The print line buffer has 120 locations for a complete print line. The print line buffer is loaded via the print-advance or load-print-line-buffer command. An entire print line is loaded before printing. The print line buffer codes are compared to the load code buffer codes for matching. When a match occurs, a print operation takes place. The print line buffer can be expanded to 132 or 144 locations (Figure 7—5). Each column number corresponds to a storage location assigned to the print line buffer as listed in Table 7—3. Each location contains 10 bits: one odd parity bit, one printed bit, and eight bits for each character code.

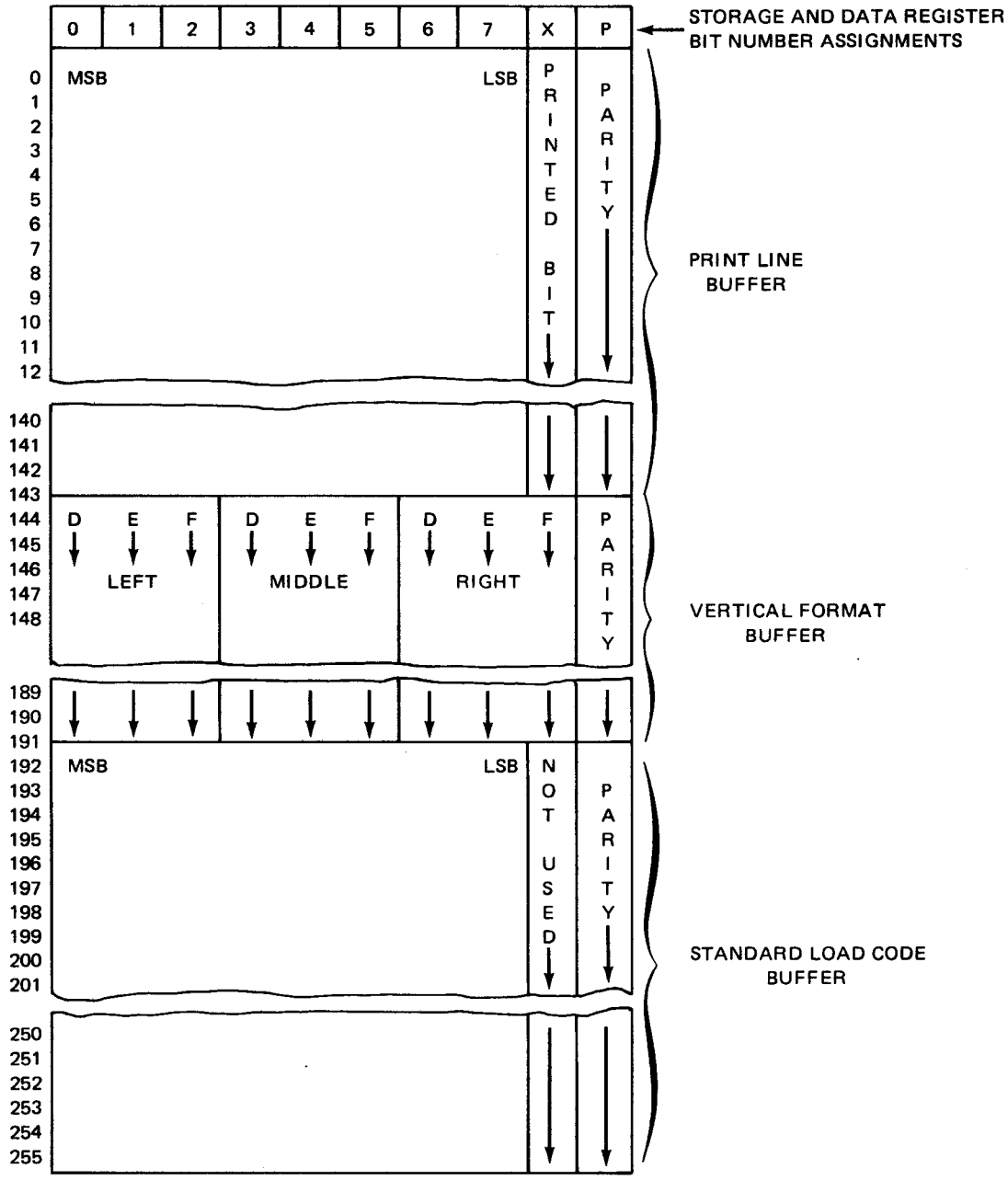


Figure 7—5. Printer Standard Storage Map

Odd buffer locations are printed first. These numbers refer to locations in the buffer; location 0 = column 1 in printer, location 1 = column 2 in printer, etc.

Printing a line begins as soon as the print line buffer is loaded with data and the previous forms advance is complete. Print operation is independent of the position of type characters. The print band moves continuously in a horizontal direction, scanning print positions. Printer control synchronizes timing of print hammer firing to print the correct character in the desired column.

The print band has raised timing marks for each character position, so that the position of the print band can be related to the selected print position. Printing a selected character occurs when the character on the print band arrives at the selected print position. (This position is relative to its position in the print line buffer.)

When even columns for a line are printed, a font mark initializes a band character counter. The printer control then begins comparing every fourth character in the load code buffer (LCB) with every tenth character in the print line buffer (PLB). The comparison begins with the first character in the LCB after a space and the 144th character in the PLB. However, th printer has a maximum of 136 print positions, so all remaining positions are zero-filled to avoid printing these locations.

When a match of characters is found, printing of the first character of the LCB occurs; and comparison begins for the second character. This sequence continues until all even columns selected for printing are printed.

Upon completion of printing for even columns and recovery of actuators, the printer control prepares for printing odd columns. The odd columns are printed with the same method used for even columns. After the form has advanced to the next line for printing, the printer control returns to even columns and the process is repeated.

A "printed bit" is reserved within the PLB for each character. This bit is set when the character is printed and inhibits further comparisons of this PLB location with the LCB. The nonprinting character (space) loaded in the PLB sets the "printed bit" in the corresponding buffer position prior to print scans. A space is not required on a band because all space codes are automatically skipped. A hardware space-fill sequence clears the PLB to space codes when the LCB command transfers data for less than the maximum print line. This ensures that the remaining line positions are cleared to space codes.

When a comparison for all odd PLB positions (even printer columns) is complete (printed bit set in each position), printing of the even PLB (odd printer columns) positions begins. Provision is made to detect whether a print cycle is completed in the maximum allowable time. When a comparison for all even PLB positions is complete, printing of the line is terminated and any forms advance specified takes place.

7.2.3.2. Load Code Buffer

The basic LCB stores up to sixty-four 10-bit character codes corresponding to character arrays on the print band; codes must be loaded in the appropriate sequence before printing can commence (Figure 7—6). The LCB allows any code to be assigned to the character set on the band because comparison with the corresponding code on the PLB results in printing of the selected character. Any 48- or 64-character band (that has identically repeated fonts) can be accommodated by the standard LCB.

The 48-character set is repeated five times around the band, and the 64-character set is repeated four times. The maximum capacity of a band is 240 characters for the 48-character set and 256 characters for the 64-character band.

The expanded LCB is provided with the expanded character set control feature. The characters may be arranged in any array of 256 different print characters on the print band. The band may contain repeated arrays or arrays of different characters, or high usage characters may repeat within an array. Two hundred and fifty-six character codes must be loaded in the proper sequence before printing may be initiated.

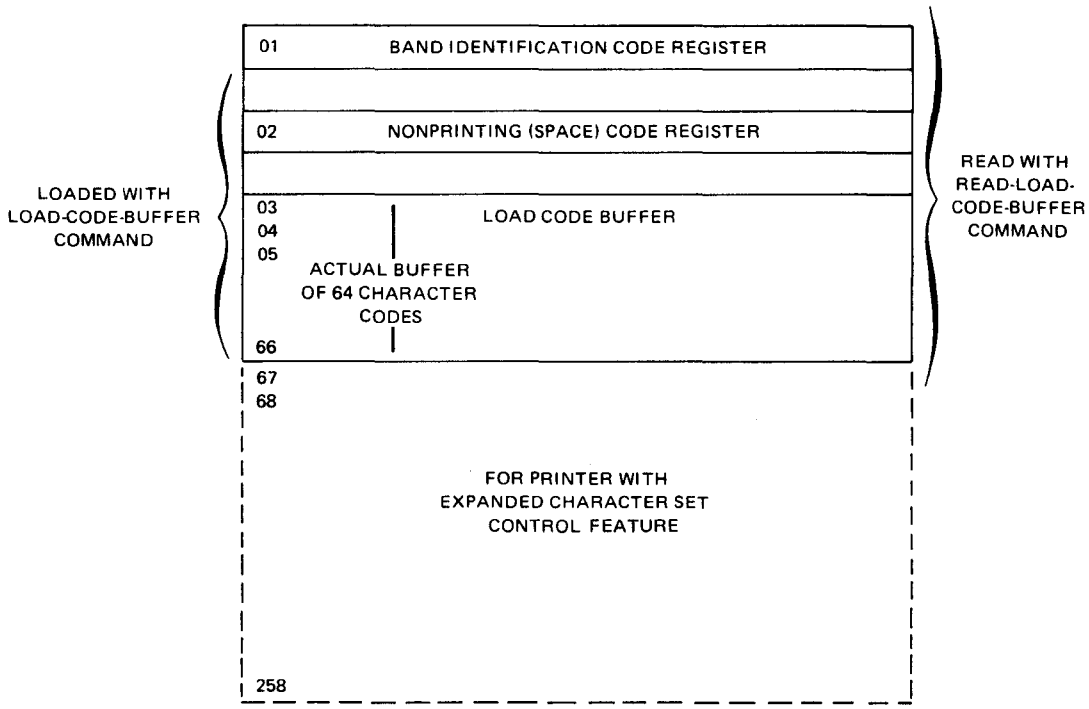


Figure 7—6. Load Code Buffer Array

The relationship between the sequence of characters on a band (or within an array) and the loading of an appropriate buffer by the LCB command is as follows:

1. The first byte loaded is the band identification code (Table 7—3). If no LCB command is issued after initial power turn on, and a print or advance command is issued, printer control sets unit check status and load code request (SB1,7); the program is notified that the character sequence code is not loaded, and the command is rejected.

   Bit 0 of the byte that specifies the character sequence code is reserved for selection of the overrun mode.

   Considerations are:

   - The condition that sets overrun (SB0,5) occurs if a character code is found in the PLB that has no corresponding code in the LCB. If S=0 (Table 7—3), all printable characters will be printed, unit check is set with device end status, and the forms advance operation for this command is not executed.
   - If S=1, unit check is not set and the forms advance operation is executed as if no unusual condition occurred.
   - If the no-match condition occurs, overrun (SB0,5) is set and can be interrogated via the sense command, regardless of the setting of the S bit.

2. The second byte loaded is the nonprinting space (blank) code.

3. The third byte loaded must be the first character after the font mark that identifies the start of each array on the band (Table 7—4).

4. The fourth through fiftieth bytes loaded correspond to the remaining 47 characters of the 48-character band.

5. The fifty-first through fifty-fourth bytes loaded provide a character dualing capability for the 48-character bands. Each of the four locations can be loaded with a unique character code that corresponds to the characters listed in Table 7—4. The forty-first, forty-second, forty-sixth, and forty-ninth bytes have a correspondence to these same characters; therefore, the capability is provided to have either of two character codes correspond to a particular character in the array. Each of the four characters, however, appears only once per array. For example, the forty-first and fifty-first locations are said to be dualed. This follows for the three additional pairs.

6. The fourth through sixty-sixth bytes correspond to the remaining 63 characters of the 64-character band. The sixty-sixth byte corresponds to the additional character provided at the end of each array. Although the type set consists of 63 unique characters, each array contains 64 character positions that are repeated four times with four font marks on the band.

7. The fourth through two hundred fifty-eighth bytes correspond to the remaining 255 characters of the 256-character band. The 256-character array is considered as one continuous array with one font mark.

These seven relationships between the buffer and character sequences on bands allow the printer control to execute the print command similarly regardless of the band installed. Also, the basic 48- or 64-character bands may be accommodated when the expanded character sets feature is installed. This precludes special handling when the basic or expanded LCB is installed.

Table 7–3. Character Sequence Codes

Band	Bits							
	0	1	2	3	4	5	6	7
48-character ①	S	X	X	X	X	1	0	0
64-character ②	S	X	X	X	X	0	1	0
Expanded character ③	S	X	X	X	X	0	0	1

NOTES:

① Print band consists of 48 characters that are repeated to have five identical fonts around the band.

② Print band consists of 64 characters that are repeated to have four identical fonts around the band.

③ Print band consists of more than 64 characters (requiring expanded character set control feature) arranged around the band for a total of 256 characters.

A map of the print line buffer and load code buffer is illustrated in Figure 7—7.

Table 7—4 lists the character sequences for the three basic band selections as well as the general sequence for an expanded character set band.

Table 7—4. Load Code Buffer Character Sequences (Part 1 of 3)

Load Code Character Sequence	48-Character Business Set	48-Character Scientific Set	63-Character or 9200/9300 Compatible 64-Character Set	256 Expanded Character Set
1.	Character sequence code			
2.	Nonprinting space (blank) code		0 (second zero)	
3.*	Z	Z	Z	
4.	Y	Y	Y	
5.	X	X	X	
6.	W	W	W	Character
7.	V	V	V	sequences
8.	U	U	U	found
9.	T	T	T	in
10.	S	S	S	Appendix B
11.	R	R	R	
12.	Q	Q	Q	
13.	P	P	P	
14.	O	O	O	
15.	N	N	N	
16.	M	M	M	
17.	L	L	L	
18.	K	K	K	
19.	J	J	J	
20.	I	I	I	
21.	H	H	H	
22.	G	G	G	
23.	F	F	F	
24.	E	E	E	
25.	D	D	D	

Table 7–4. Load Code Buffer Character Sequences (Part 2 of 3)

Load Code Character Sequence	48-Character Business Set	48-Character Scientific Set	63-Character or 9200/9300 Compatible 64-Character Set	256 Expanded Character Set
26.	C	C	C	
27.	B	B	B	
28.	A	A	A	
29.	9	9	9	
30.	8	8	8	
31.	7	7	7	
32.	6	6	6	
33.	5	5	5	
34.	4	4	4	
35.	3	3	3	
36.	2	2	2	
37.	1	1	1	
38.	0	0	0	
39.	-	-	-	
40.	/	/	/	
41.	@	' (apostrophe)	@	
42.	#	=	#	
43.	$	$	$	
44.	, (comma)	, (comma)	, (comma)	
45.	+	+	+	
46.	' (apostrophe)	)	' (apostrophe)	
47.	*	*	*	
48.	%	(	%	
49.	&	&	&	
50.	.	.	.	
51.**	@	' (apostrophe)	:	
52.**	#	=	| (vertical line)	
53.**	' (apostrophe)	)	"	

Table 7–4. Load Code Buffer Character Sequences (Part 3 of 3)

Load Code Character Sequence	48-Character Business Set	48-Character Scientific Set	63-Character or 9200/9300 Compatible 64-Character Set	256 Expanded Character Set
54.**	%	(	!	
55.	N/A	N/A	¾	
56.	N/A	N/A	– (underline)	
57.	N/A	N/A	(	
58.	N/A	N/A	=	
59.	N/A	N/A	Γ	
60.	N/A	N/A	;	
61.	N/A	N/A	\	
62.	N/A	N/A	¢	
63.	N/A	N/A	)	
64.	N/A	N/A	½	
65.	N/A	N/A	¾	
66.	N/A	N/A	0	

* First character after font mark.

**Dualed character positions. (Characters shown in this table represent those printed for codes loaded in the sequence presented.)

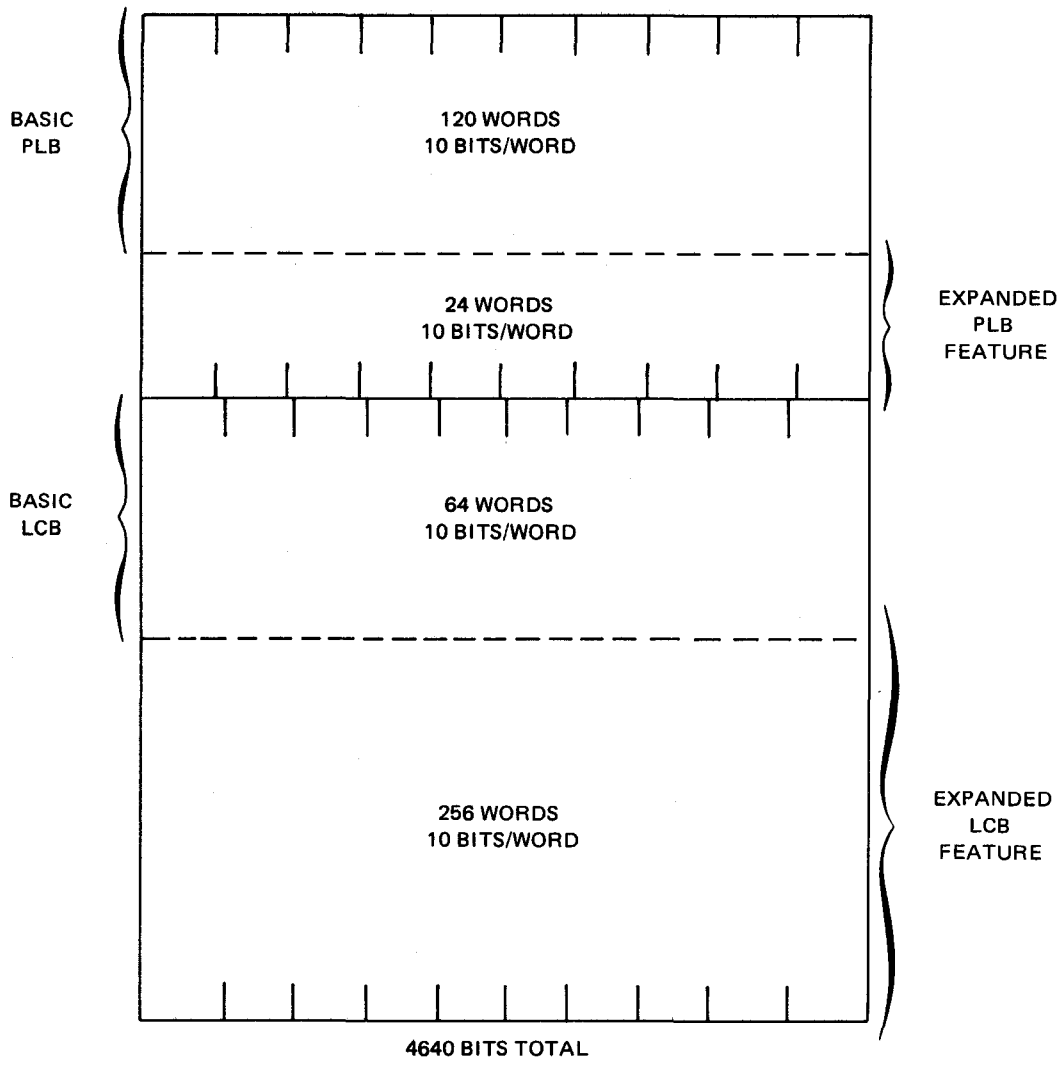


Figure 7—7. Print Line Buffer and Load Code Buffer Map

7.2.3.3. Vertical Format Buffer

The vertical format buffer (VFB) stores the vertical format for paper advance, and skip codes for forms advance, line spacing, and length of forms.

The VFB accommodates up to 144 skip/stop positions (48 positions with 3 stop positions of 3 bits each), equivalent to a 24-inch (609.6 mm) form at 6 lines per inch (4.23 mm per line), and an 18-inch (457.2 mm) form at 8 lines per inch (3.17 mm per line). If the expanded character set control feature is installed, the VFB is expanded to 64 locations, which can provide up to 192 stop positions and accommodate form sizes up to 24 inches at 8 lines per inch (3.17 mm per line). Forms may be advanced, with one command, from 1 to 15 lines, or they may be skipped to line positions specified by a program loaded in the buffer. Selected codes are loaded in the buffer in positions corresponding to stop positions desired on the form (Figure 7—8).

The VFB is initially synchronized with the home position of the form by the operator; the operator aligns the form by pressing and holding the STOP switch, then pressing the HOME switch. The VFB location corresponding to the current print line is kept in synchronization with the movement of the paper by the VFB address register. Once synchronized, the VFB must be loaded (via the load-VFB command) with the appropriate print form information. Print form information must include the home paper code and may also include forms overflow, end of forms, and stop codes. If a command is received specifying print-advance or advance, and the VFB is not loaded, the command is rejected with unit check status, and vertical format request sense bit (SB1,6) is set.

The 3-bit code loaded via the load-VFB command consists of the three least significant bits (LSB) for each byte transferred via the command. The data byte sequences required to load the VFB and the data byte sequences transferred to main storage when a read-VFB command is executed are listed in Table 7—5.

The interpretation of modifier bits DEF of the line bit register (Figure 7—8) is as follows:

Modifier Bits	Interpretation
DEF	
000	Filler code
001	Forms overflow
010	Program selectable codes; these codes are compared to DEF bits specified in the advance and print-advance commands.
011	
100	
101	
110	
111	Home paper or end of forms code

The first position in the VFB is reserved for the home paper code (111) which must be loaded first. The end of forms code (111), identical to the home paper code, designates the end of the VFB. The number of contiguous positions between home paper and end of forms codes is determined by the program and normally corresponds to the length of the form being printed. When printer control detects the end of forms code in the VFB, or the last location of the VFB is reached without detecting the end of forms code, the VFB address register is cleared to the home paper position.

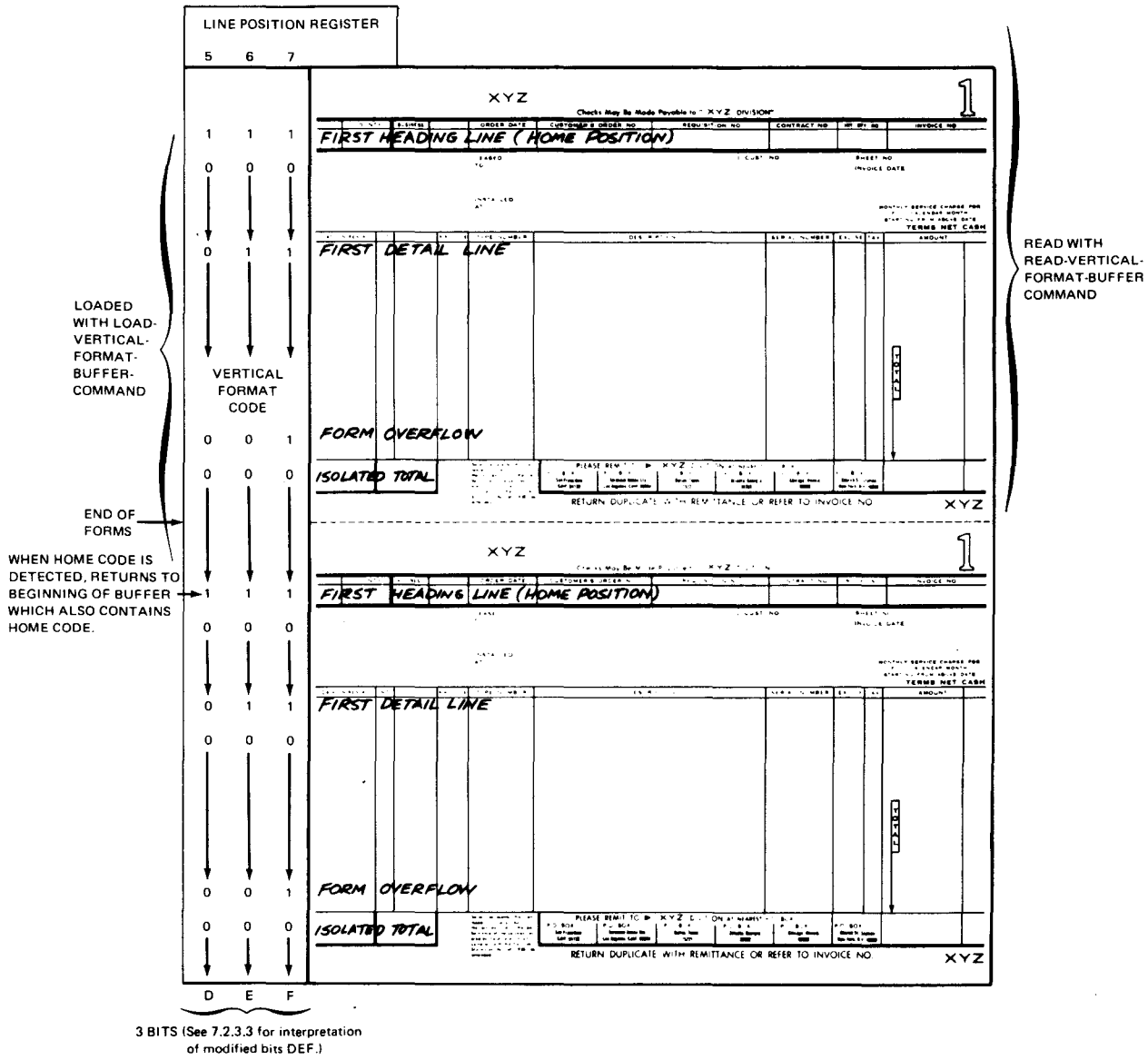


Figure 7—8. Vertical Format Buffer and Form Relationship

Table 7—5. VFB Data Byte Sequences

VFB Location	Command																
	Load VFB Bits									Read VFB Bits							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	Notes
1	X	X	X	X	X	1	1	1	0	0	0	0	0	1	1	1	1
2	X	X	X	X	X	D	E	F	0	0	0	0	0	D	E	F	2
3	X	X	X	X	X	D	E	F	0	0	0	0	0	D	E	F	2
n	X	X	X	X	X	1	1	1	0	0	0	0	0	1	1	1	3
143	X	X	X	X	X	D	E	F	0	0	0	0	0	D	E	F	2,4
144	X	X	X	X	X	D	E	F	0	0	0	0	0	D	E	F	2,4,5
n+1	X	X	X	X	X	D	E	F	0	0	0	0	0	D	E	F	2,4,6
191	X	X	X	X	X	D	E	F	0	0	0	0	0	D	E	F	2,4,6
192	X	X	X	X	X	1	1	1	0	0	0	0	0	1	1	1	2,4,5,6,7,8

LEGEND:

X = Bit is ignored.

D, E, F = Detail bits (7.2.3.3 and Figure 7—8)

NOTES:

1. Home paper code (111_2) must be loaded for the command detailed bits to specify an advance to the home paper position.
2. These bits are compared with the DEF bits of the print-advance, or advance command when program controlled line skip is specified. Form advancing stops when the bits compare.
3. End of forms code (111_2) when detected before the last location in the VFB is reached, it clears the VFB address register to the home paper position and advances the form to the corresponding position.
4. If end of forms code is present before maximum VFB location (144 or 192), these codes are ignored by the hardware.
5. Last location in VFB. After this location is reached, the VFB address register is cleared to the home paper position on the next form advance.
6. Expanded VFB; provided when the expanded character set control feature is installed.
7. Maximum expanded VFB. After this location is reached, the VFB address is cleared to the home paper position on the next form advance.
8. To initiate paper advance under program control via skip codes or line count, and to detect and recover from forms low/out of forms conditions, refer to 7.2.4.1.

7.2.3.4. Character Dualing

Character dualing capability in the printer control is always in effect for 48-character print bands; therefore, 52 characters must always be loaded in the load code buffer. If the capability is not required, or must be inhibited, the four locations corresponding to the dualed character positions (i.e., bytes 51 through 54) should be loaded with the space code or the code that is loaded in the dual character positions. In either of these 2 (nondualing) cases, only 48 character codes (plus space) are valid, and nonmatching codes cause the overrun bit (SB0,5) to set.

Character dualing enables software to handle either the business or scientific 48-character print band with a single load of the load code buffer. This is because the four different positions on the arrays correspond with the four dualed locations in the load code buffer. For example, if the 48-character business cartridge code set is a basis for loading the load code buffer, then codes for the fifty-first through fifty-fourth locations can correspond with the apostrophe, equal sign, right parenthesis, and left parenthesis of the scientific set. The load code buffer is loaded with 52 unique characters. If the installed cartridge matches the code set in use (48 characters), code-to-character correspondence will be correct.

This method of loading the load code buffer can also be used when only one 48-character band is available but print runs are made with either code set. In this case, code-to-character correspondence will be incorrect when the code set in use does not match the band in use (i.e., @ is printed for ', # is printed for =, etc.).

A general application of dualing is where a code set to be applied is greater than 48 characters and the only available band is either of the two 48-character bands. With dualing, the code set to be applied can be extended to 52 character codes; however, only 48 characters can be printed. Dualing does not affect the throughput rate.

Handling code sets greater than 52 characters with the 48-character bands is possible only if S bit equals 1 in the character sequence code (Table 7—3). In these cases, codes beyond those stored in the load code buffer are interpreted as space (blank) codes.

7.2.3.5. Data Transfer Rate

The 300 lines per minute (lpm) printing is based on printing 48-character sets (plus space) with single line advance via successive print-advance commands. The actual throughput rate depends on the operating mode of the printer (print-advance and advance commands, or only print-advance command), and on the number of different characters to be printed on a line. The data transfer rate is therefore controlled by the following parameters:

1. The print rate, as explained under 7.2.4.3.

2. Selection of forms printing at 6 lpi (2.36 lpcm) or 8 lpi (3.15 lpcm), and the number of lines advanced per command. The time required is as follows:

   6 lpi= 16 + 7.6 (n—1) ms
   8 lpi= 14.2 + 5.7 (n—1) ms
   $n \neq 0$

   where n is number of lines to be advanced.

3. Characters to be printed within the selected font. Even columns can be printed within 1 ms in the most favorable case, or within 47.0 ms in the worst case. With the additional recovery time of 10 ms, and an equal time to print the odd columns, the print time for a line varies between 12 and 104 ms.

4. Frequency of print-advance and advance commands. To achieve the specified rates, the commands must be issued and the print line buffer loaded prior to the end of the previous line advance. The following restrictions apply to the printer control and are effective only if the time for printing is significantly less than the worst case, as stated above:

   a. Start of consecutive print operations occurs more often than 83 ms apart.

   b. Start of consecutive line advances occurs more often than 70 ms apart.

   Commands are accepted and held in the printer control, but are not executed until the delays in restrictions a and b (above) have elapsed. The delays permit rated lpm speeds to be achieved, and conform to the duty cycle safety limitations for the printer.

5. Loading of the print line buffer. Printing cannot begin until the print line buffer has been loaded. Data requests for loading the buffer are limited by the buffer cycle time, internal printer control timing, activity on the IPC by other subsystems, and activity on channels having higher priority than the IPC. This rate can approach the maximum data rate attainable by the IPC under optimum conditions.

7.2.3.6. Print Band Synchronization

The print band uses sprockets etched along its entire length for obtaining timing synchronization (Figure 7—9). As the print band moves, a sprocket pulse is detected by a magnetic head and supplied to a print sprocket counter. This counter tracks characters on the print band and determines which characters will align with the print hammers during the next sprocket pulse. This permits the proper load code location to be addressed during a print operation.

If the print sprocket counter has reached 0 and the once-per-font sprocket (called the font mark, Figure 7—9) has not occurred, a synchronization error exists. The error is also caused if the font mark occurs at any time except when the sprocket counter has reached 0. However, these errors are not reported in sense commands unless they occur during printing. In that case, printing is aborted, the PRINT CHECK indicator is lit, and a band-check error is indicated.

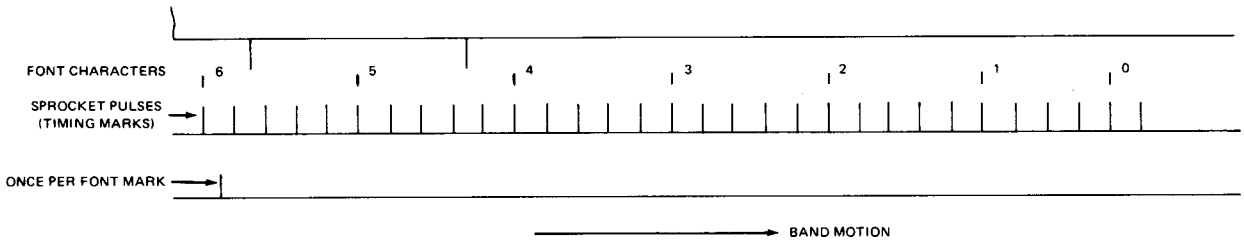


Figure 7—9. Print Band Synchronization

7.2.3.7. Print Band Identification

The print band is identified by counting the sprocket pulses between detection of font marks (Figure 7—9) and compared to data contained in the first byte transferred during the load-code-buffer command read-in. Thus, the load code contains the print band identification that must compare with the sprocket pulse count of the band in use. Identification is made only when the print band motor is on.

If the wrong band is installed (i.e., the codes mismatch), the command is aborted, the PRINT CHECK indicator lights, and a band-check error is indicated.

7.2.3.8. Print Band Motor Control

Printer control turns off the print band motor when the printer is not in use. If a print-advance command is given and the band motor is not running, a 5-second delay is initiated to inhibit printing until the band motor is up to speed. Issuing a print-advance command also initiates a 5-minute (minimum) time-out delay. That is, if no printing occurs during this 5-minute period, the band motor is turned off.

7.2.4. Printer Mechanism

The printer mechanism comprises a print carriage assembly, interchangeable print cartridge, ribbon feed mechanism, print hammer/actuator assembly, and forms transport mechanism.

The printer mechanism is used to print data and advance forms. The print band (print cartridge) contains etched characters, timing marks, and synchronization. The print band moves horizontally at a constant speed in front of print hammers. The print hammers impact the rear of a forms pack forcing the forms pack into contact with an inked ribbon and the moving print band. Printing occurs asynchronously (not dependent on initial position of print band) when a selected character lines up with a selected column position.

7.2.4.1. Print Carriage Assembly

The print carriage assembly, located immediately in front of the forms, is capable of swinging out to permit clear access to forms and facilitate ribbon changing. The print carriage assembly includes the print band cartridge and the ribbon feed mechanism.

7.2.4.2. Print Cartridge

The print cartridge (Figure 7—10) contains a print band, with its associated pulleys, and magnetic heads that initiate timing and synchronism control (7.2.3.6, 7.2.3.7, 7.2.3.8). The cartridge assembly is housed in its own integral cartridge cover to prevent damage to the print band.

A nameplate on the cartridge cover identifies the print band. A variety of print cartridges is available to meet most customer requirements. Additional special print cartridges are under consideration.

Each print band contains characters grouped in repeating arrays. For example, a 48-character set is repeated five times on the band and the 64-character set is repeated four times. The maximum capacity of a print band is 240 characters for the 48-character set and 256 characters for the 64-character set (plus spaces).

The expanded character set control feature (Table 7—2) allows use of 256 character bands with the characters arranged in any array. The print band may contain repeated arrays or arrays of different characters, or high usage characters may repeat within an array.

A font mark at the beginning of each character set on the band is used to initiate comparisons against data in the print line buffer.

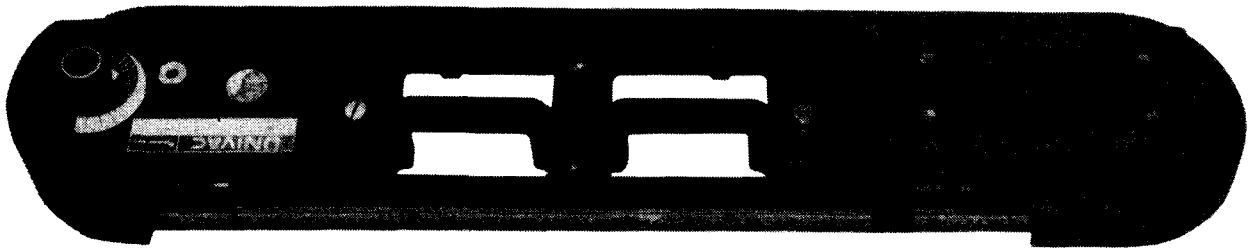


Figure 7—10. Print Cartridge

Print bands contain raised font-set characters, font marks, and timing marks (Figure 7—11) around their continuous periphery. Font characters on the print band are positioned approximately 0.250 inch (6.35 mm) apart.

The print band moves continuously in a horizontal direction past the print hammers. One hammer covers two columns. The printer operates in a dual cycle mode: even and odd. During one cycle, the hammers print the even columns (odd print line buffer addresses); in the next cycle (after a hammer recovery delay of 10 ms), the hammers print in the odd column (even buffer addresses), completing the line.

The print band column numbers begin with 1, whereas the memory buffer location numbers begin with 0. Thus, band column 1 is in buffer location 0, band column 2 in buffer location 1, band column 3 in buffer location 2, etc.

Print cartridges may be replaced by the operator when required. However, print bands are replaced within the print cartridge only by the Sperry Univac customer engineer.

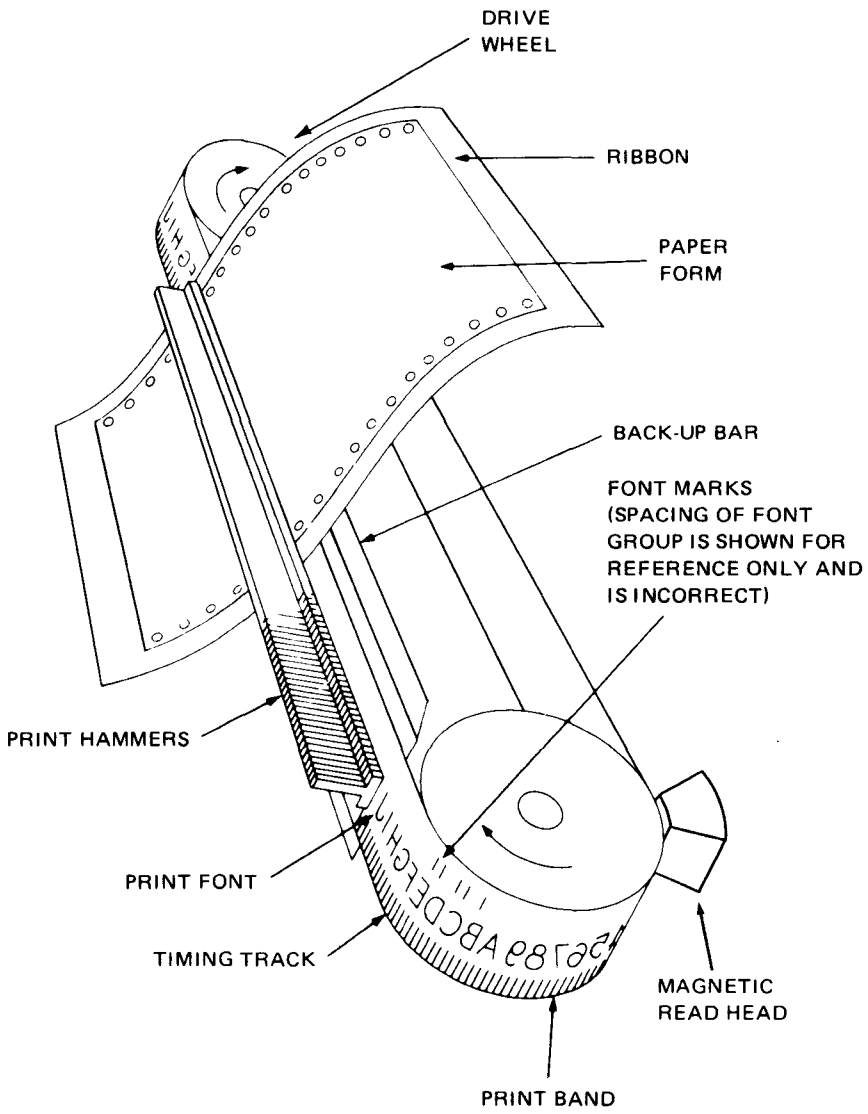


Figure 7—11. Print Function, Schematic Diagram

7.2.4.3. Print Rate

The print band scans the print positions and the form advances one line (for single line spacing) in 16.0 ms. With a 48-character print band, a complete line is printed and forms advanced in 120 ms (maximum).

Line printing begins as soon as the print line buffer has been filled and the form has advanced from the previous line, regardless of the print band position. Printing continues until all characters for the line have been printed, which is recognized by an end-of-print detector.

Table 7—6 lists the nominal print rates for the various print cartridge arrangements, assuming single line spacing.

Table 7—6. Print Rates

Length of Array	Arrays per Band	Minimum Specified Print Rate (lpm)
48	5	500
64	4	400
48/16*	4	400/670
85	3 (plus 1 character)	310
128	2	217
96/(16–16)*	2	217/500
256	1	114

*The smaller array appearing in the middle of and between the larger array can be printed at the higher indicated throughput rate. The "16" is commonly a numeric subset. Extra "16" arrays are included in the 96/16—16 arrangements to make up the 256 total number of characters in a band.

7.2.4.4. Ribbon Feed Mechanism

The entire ribbon feed and ribbon drive mechanism is contained on the carriage assembly (7.2.4.1). The ribbon drive mechanism causes the print ribbon to wind in either direction, and contains a reversing bar at each end to reverse direction upon sensing that either spool supply is exhausted.

Design of the ribbon feed mechanism facilitates ribbon removal by the operator. The ribbon may be removed completely from both spool drives without winding to the end when ribbon replacement is required. If the print band is to be replaced, or maintenance is required on the carriage assembly, only a single spool need be removed from a spool drive and the ribbon temporarily held on the opposite side of the carriage assembly. This permits access to replace the print cartridge.

7.2.4.5. Print Hammer/Actuator Assembly

The print hammer/actuator assembly is located behind the paper forms on the front of the printer. One print hammer with an electromechanical actuator is provided for every two print positions. A standard print hammer/actuator is equipped with 60 hammers and associated actuators. When a print command is received for a particular hammer, the actuator propels the hammer behind the paper form which pushes the form against a raised character font on the print band. As the print band continuously moves in front of the form, the proper hammers are actuated the instant a desired character is in proper print position. Ribbon passes between the paper form and print band (Figure 7—11).

7.2.4.6. Forms Transport Mechanism

The forms transport mechanism contains two sets of form tractors that feed forms from a supply container in the lower front of the printer to a forms shelf in the rear. Forms are moved under printer control according to a programmed vertical format buffer.

The two sets of form tractors are manually adjustable for form widths from 4.0 inches (101.6 mm) through 18.75 inches (467.2 mm), and for margin placement. It is possible to adjust the tractors to print a full line of 144 characters (14.4 inches, 36.57 mm) anywhere within the print area of a form 17.20 inches (43.69 cm) wide. When using a form 18.75 inches (47.62 cm) wide, line adjustments of 1.50 inches (3.81 cm) to the left and 0.25 inch (6.35 mm) to the right, around the center of a 14.37 inch (36.49 cm) form are used. Column 1 position is fixed at a location approximately 7.2 inches (18.28 cm) left of center of the print head.

Vertical forms tension is adjustable by an operator control, and does not vary with changes in paper stock weight. The lower set of tractors draws paper up from a supply container and passes the paper to the upper set of tractors after printing is complete. Printed forms pass over guides and to the forms shelf where they are refolded and stacked.

Forms movement is controlled during operation by the vertical format buffer, which is loaded by the program. Forms may be advanced (with a single command) from 1 to 15 lines, or they may be skipped to line positions specified by the program loaded in the vertical format buffer. The forms and vertical format buffer advance simultaneously so that print lines are controlled for each form.

An end-of-paper detection device generates a warning signal to indicate that approximately 6 inches (15.24 cm) of paper remains below the print line. A switch on the right lower tractor detects the absence of forms in the lower tractors (i.e., end of forms) and a switch in the top left tractor detects whether the forms are torn (or missing) at the print line.

7.2.4.7. Forms Advance Rate

Forms are advanced at specific rates. Table 7—7 lists the line advance rates when using 6 lpi (2.36 lpcm) or 8 lpi (3.15 lpcm) spacing. The minimum time required between start of execution of consecutive advance commands is 70.0 ms.

Table 7—7. Line Advance Rate

Lines Advanced	Maximum Time (milliseconds)	
	6 lpi	8 lpi
1	16.0	14.2
2	23.6	19.9
3	31.2	25.6
n+1	16.0 + 7.6n*	14.2 +5.7n

*n = total lines to be advanced

NOTE:

Forms advance slew rate = 22 inches (55.8 cm) per second

7.2.5. Operating Sequences

The programmer should be familiar with the sequence of operations in the printer, beginning with printing, and continuing into forms advance.

A typical printer control operating sequence is as follows:

1. Decode the print-advance command (command n).
2. Load the print line buffer (space fill if less than the maximum number of characters is specified via buffer control word).
3. Scan to print all even columns (1 to 47 ms for 48-character band).
4. Delay 10±0.5 ms to recover after all even columns are printed; the same print hammers are used to print odd columns.

5. Scan to print all odd columns after the delay expires (1 to 47 ms for 48-character band).

6. Initiate a request to the processor to store status and await the next command (command n+1).

7. Simultaneously perform the paper advance for command n and the delay to recover print hammers (10±0.5 ms) before beginning printing portion of command n+1.

The first print-advance command (command n) loads the print line buffer, prints the line, and advances the paper. The status is presented after the printing is completed. It is assumed that the program responds and issues the next print-advance command (command n+1). Printer control loads the print line buffer for command n+1 before the advance for command n is completed and is ready to start the next print cycle. All subsequent cycles are overlapped in a similar manner.

Printer control is considered busy from the time a command is accepted until status is stored (at completion of the print operation before paper advance). After status is accepted by the processor, printer control can accept the next command.

The following restrictions apply to all data transfers between the processor and printer control for the print line buffer, load code buffer, vertical format buffer, and sense data transfers:

1. The count (A) must contain an even count.

2. The main storage address, address (A), must start on a half-word boundary.

3. The first byte transferred is in the most significant half of the half word.

4. The second byte transferred is in the least significant half of the half word.

7.2.5.1. Printer Line Feed and Paper Advance

During the paper advance operation, forms are advanced by the forms tractors and a driving motor. Printer commands contain either line feed information ("A" detail bit set to 0 in print-advance or advance command) or indicate a skip to a specific line position on the form ("A" detail bit set to 1), Table 7—8.

A manual paper advance capability is provided via the HOME and LINE SPACE switches.

7.2.5.2 Program Controlled Paper Advance

To initiate paper advance under program control, the operator must synchronize the form with the vertical format buffer (VFB) (in the STOP state). Note that on initial power-up, the printer is in the run state, provided forms are loaded and no other error conditions are present. The following procedure is followed upon initial power-on, or when a change of forms is required:

1. Load the paper in the printer and advance the paper to the home position using the LINE SPACE switch.

2. Initialize the VFB to the home position by pressing the HOME switch while pressing and holding the STOP switch. No forms advance is initiated by this procedure.

3. Press the RUN switch to enter the run state (if no error conditions persist). Attention status is presented to the IPC and the program must respond with the load-vertical-format-buffer command before initiating an advance operation. The program and form are now synchronized.

The VFB provides the capability for skipping to program selected line positions. There is no mechanical indication that the form is or is not in the proper position. All program initiated skips are relative to the VFB only. Once an error (initial synchronization, or during printing operations) on advance occurs, the error can be detected only by visual inspection of the form. Manual intervention is required to correct the condition.

7.2.5.3. Paper Advance via Skip Codes

When an advance or print-advance command specifies paper advance via skip codes (A = 1), printer control steps through the VFB and searches for the next VFB position containing the code excluding the current position. The search function is performed during the delay after all the even columns are printed. If a match exists between the command D, E, F bits (Table 7—9) and the D, E, F bits of the VFB (Table 7—5), the advance is initiated when all printing is completed. If a match does not exist, printing is completed but no paper advance occurs. Unit check and device end status are presented to the processor. The sense bytes specify the particular error condition; therefore, a forms runaway condition caused by the program is not possible. If the program specifies a skip to end of forms, it is treated as a skip to home position.

7.2.5.4. Paper Advance via Line Count

When the advance or print-advance command specifies paper advance via line count (A = 0), printer control steps through the VFB in search of the forms overflow code (001) while decrementing the line count. If forms overflow is not detected before the line count is decremented to 0, the specified paper advance is initiated at completion of the printing operation. The VFB address register is kept in synchronism with movement of the printer.

If a forms overflow is detected before the count is depleted or if the count is depleted at the forms overflow position in the VFB, the advance stops after the forms have advanced the number of lines specified by the command. Unit exception and device end status are presented to the processor.

7.2.5.5. Detection and Recovery of Forms Low or Out of Forms Conditions

Out-of-forms detection capability is provided by printer control generating a forms low indication (SB1,1) when 6 inches (15.24 cm) of paper remains below the print line. This condition occurs only if the form is advancing and, therefore, status and sense information cannot be presented until completion of the operation. If a long skip is specified, it is possible to advance the form past the upper tractor; this condition requires operator recovery and resynchronization of the form with the VFB. Forms out (SB1,0) and forms low (SB1,1) bits are set.

If the form stops advancing before the detection of the end of forms code 111 in the VFB, the printer enters the stop state and the OUT OF FORMS indicator lights. The indicator remains lit until the condition is cleared by the operator. Sense data indicates the forms low condition (SB1,1). Because overlapping of commands is allowed, it is possible that the next command may be issued to printer control. Unit check and device end status are presented to the processor and the printer enters the STOP state. A print or advance command is not executed and must be issued by the program when the error condition is cleared. The following conditions apply to the forms low condition:

- If a command was not issued when forms low condition was detected, the printer enters the stop state immediately. The next command (other than sense) is rejected with unit check status.
- After a command is issued, the detection of forms low (due to a previous command) generates unit check and device end status and places the printer in the stop state.

- The operator may overlay the form with a new supply to clear the forms condition. Pressing the RUN switch after loading new forms resumes normal operation.

  If prenumbered forms are used and printing to the end of the form must be accomplished, the operator may press the RUN switch when the FORMS LOW indicator is lit without loading new forms. Subsequent commands are executed normally until the VFB address register is cleared to the home paper position. The printer reenters the stop state when the command that caused the advance to or past the home paper position is executed. No further commands to print or advance are accepted until the forms supply is replenished.

If the printer is returned to the run state and a command is issued which may advance the form after the forms low condition is detected, the following conditions apply:

- If the advance is to the end of the form, the advance is performed and the stop state is entered. If the advance is past the end of the form (as specified by the A, C, D, E, and F bits), the form advance is performed as specified and the stop state is entered.

- Because overlapping of commands is allowed, the next print or advance command may have already been issued to printer control; the advance portion of this command is not executed, and unit check and device end status are presented to the IPC. The advance portion of the commmand must be reissued by the program when the error condition is cleared.

- When the sense command is issued, the sense data includes both forms low (SB1,1), and forms out (SB1,0) indications.

- If the advance has moved the form out of the upper tractors, no overlay is possible and resynchronization of the form and the VFB must be performed by the operator.

7.2.5.6. Parity Checks

Parity error parameters are as follows:

SB0,1 and SB1,7	RUN,PARITY CHECK indicators lit.	→ LCB parity error during read-LCB command.
SB0,1 and SB1,5	RUN,PARITY CHECK indicators lit.	→ PLB parity error during read-PLB command.
SB0,1;SB0,6; and SB1,7	STOP,PARITY CHECK indicators lit.	→ LCB parity error during print advance or diagnostic print.
SB0,1;SB0,6; and SB1,5	STOP,PARITY CHECK indicators lit.	→ PLB parity error during print advance or diagnostic print.
SB0,4 and SB1,6	RUN indicator lit.	→ VFB parity error during print-advance, advance, or read-VFB commands.

- PLB and LCB Parity Errors

  PLB and LCB parity errors cause immediate termination. If they occur during read (PLB or LCB) commands, they remain in the RUN state. During print commands, the print command must be retried (overprint on previously printed characters will occur). No advance takes place on commands with error.

- VFB Parity Errors

  VFB parity errors cause immediate termination on read-VFB commands but remains in the RUN state. During print-advance or advance commands, no advance occurs (printing is completed), and it remains in the run state.

7.2.6. Operator Control Panel and Indicator Panel

The 0773 printer operator control panel is illustrated in Figure 7—12. The switch/indicators are described in Table 7—8.

Indicators associated with the printer are located on the processor operator/maintenance panel. The indicators are illustrated in Figure 7—13 and also described in Table 7—8.

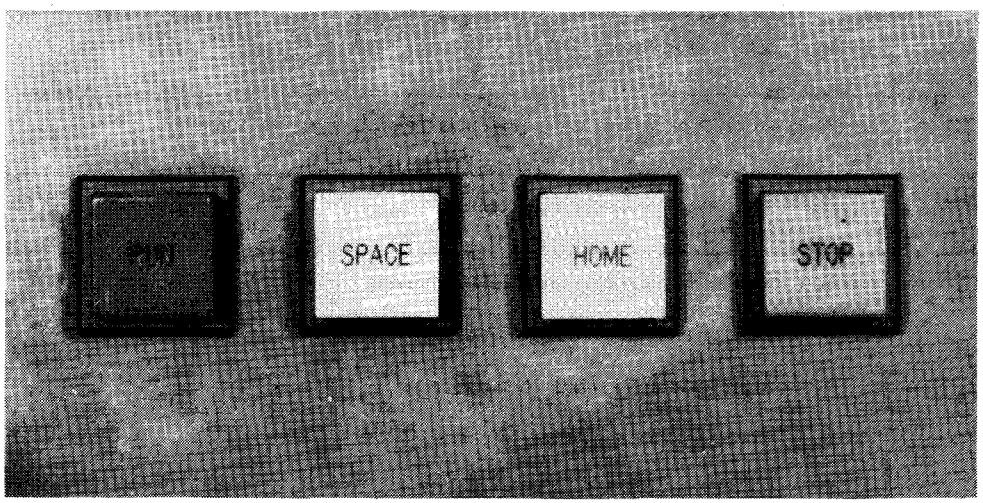


Figure 7—12. Printer Control Panel

Table 7—8. Printer Controls and Indicators

Switch/Indicator	Function
RUN switch/indicator	Places printer online to processor provided no check conditions exist and the STOP switch/indicator is lit.
STOP switch/indicator	Places printer offline if RUN switch/indicator is lit. When held pressed, allows lamp test for all switch/indicators.
HOME switch/indicator	Causes forms to advance under program control. When lit, indicates forms are in the home position.
LINE SPACE switch	Causes forms to be stepped forward at a steady rate as long as switch is held depressed. Momentarily pressing switch causes forms to advance a single line at either 6 lpi (2.36 lpcm) or 8 lpi (3.15 lpcm), according to setting of line selection switch.
OUT OF FORMS indicator	Printer is out of forms or less than 6 inches of forms remain. Extinguishes when forms are loaded.
FORMS CHECK indicator	Form is torn or jammed.
PRINT CHECK indicator	Fault exists in print hammer actuator or in print band operation.
PARITY CHECK indicator	Parity error detected by printer control.
DEVICE CHECK indicator	This indicator lights when one of the following conditions is present: ■ Lack of air flow through printer ■ Print band drive motor inoperative ■ Print carriage not locked in place ■ Internal printer temperature too high

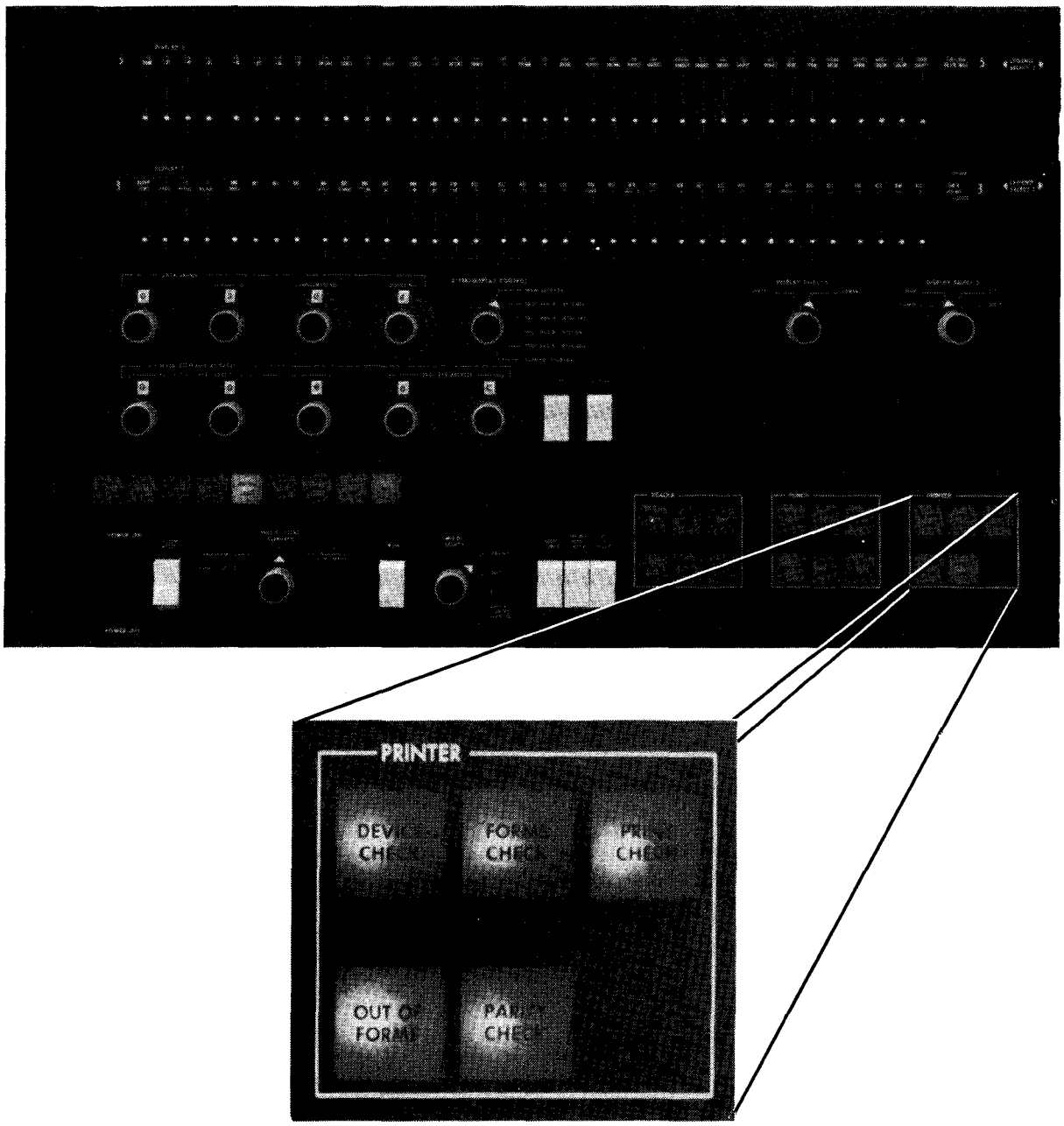


Figure 7—13. Processor Operator/Maintenance Panel Showing Printer Error/Fault Indicators

7.3. PROGRAMMING

This section provides programming reference information for the printer. In particular, information is concerned with processing the printer subsystem command bytes, status bytes, and sense data bytes. Information on error recovery is also presented.

7.3.1. Commands

The printer recognizes as valid the commands listed in Table 7—9 and described in 7.3.1.1 through 7.3.1.10. The command codes may be issued to printer control to provide format information, initiate forms movement, transfer data, or interrogate printer control about printer conditions. Each command is checked for parity and validity before being accepted in the printer control. Status signals generated in response to the commands are described in 7.3.2.

If a command is invalid or incorrect, it is rejected by printer control, and a unit check status is returned to the IPC with the command reject bit (0) set in sense byte 0. Printer control is considered busy from the time a command is accepted until the status byte is presented and stored by the IPC.

Table 7—9. Printer Commands

Command	Bits							
	0	1	2	3	4	5	6	7
Load Vertical Format Buffer	0	1	1	0	0	0	1	1
Load Code Buffer	1	1	1	1	1	0	1	1
Print-Advance	A	C	D	E	F	0	0	1
Advance	A	C	D	E	F	1	1	1
Load Print Line Buffer*	1	1	1	0	0	0	1	1
Read Print Line Buffer*	X	X	X	0	0	0	1	0
Read Load Code Buffer*	X	X	X	0	1	0	1	0
Read Vertical Format Buffer*	A	X	X	1	0	0	1	0
Diagnostic*	X	X	X	X	X	1	0	1
Sense	X	X	X	X	0	1	0	0

*These commands are normally for diagnostic use only; normal operation of the printer should not be predicated on the use of these commands.

LEGEND:

X = Bit is ignored by the printer control.

A, C, D, E, F = Modified/detail bits

7.3.1.1. Load Vertical Format Buffer

This command loads the vertical format buffer (VFB) with the stop codes for the appropriate line conditions. Eight-bit bytes received from the processor contain the stop codes for the VFB in the three least significant bits of each byte (Table 7—5).

Data bytes are loaded sequentially until either the buffer count word (BCW) count (A) is exhausted or the last VFB position is loaded. The maximum byte count is 144 bytes. Device end status is returned after successful completion of the load operation. The program must load the proper sequence and number of bytes to provide forms control required for the print operation to be performed.

The printer control will find the remaining VFB locations with zeros if the data transferred from the IPC is less than the size of the installed VFB.

7.3.1.2. Load Code Buffer

This command loads the band identification code, the space code, and the load code buffer with codes assigned to each successive character on the print band (Table 7—4). Both the band identification code (first byte transferred) and the space code (second byte transferred) are stored in hard registers external to the load code buffer. If the expanded character set feature is not installed, either 52 or 64 bytes can be loaded in the basic buffer for the appropriate type band; with the feature installed, 52, 64, or 256 bytes, can be loaded in the expanded load code buffer.

If the expanded character set feature is not installed and the byte count in the BCW is greater than 66, printer control terminates data requests after the sixty-sixth byte has been transferred.

Device end status is returned after successful completion of the load operation. The program must load the appropriate codes for the print band in use.

7.3.1.3. Print-Advance

The print-advance command initiates the transfer of data characters for one print line into the print line buffer. The print line buffer may be loaded while the paper advance initiated by a previous command is in progress. The maximum byte count specified should correspond to the number of print positions available (120, 132, 144). Loading of the print line buffer continues sequentially until 120, 132, or 144 characters have been transferred or early termination occurs (BCW count (A) decremented to 0 or T bit set). Upon loading the buffer (120, 132, 144) or when early termination occurs, printer control (if applicable) space fills the remaining print line buffer locations through the 144th position. Once all 144 positions of the print line buffer are loaded or space filled, the printer control initiates the printing of the data.

Printing of the data transferred by the print-advance command (command n+1) occurs when the paper advance from the previous command (command n) is completed. Successful completion of the printing is indicated by device end status being presented to the processor for command n. An error detected during the paper advance from command n inhibits printing of the data loaded in the print line buffer and is indicated by unit check and device end status for command n+1; the printer enters the stop state.

Paper advancing specified by the print-advance command is initiated after completion of printing and transfer of device end status (if no error occurs). The A, C, D, E, and F detail bits of the print-advance command specify two modes of paper advance:

- If A = 0, the C, D, E, and F bits specify a line advance from 0 to 15 lines. Note that the specified line advance should not cause the VFB address (synchronized with paper advance) to pass through the location containing the end-of-forms code more than once, since it will only be reported as unit exception status once.

- If A = 1, the D, E, and F bits are interpreted as skip codes, which are compared with the stop codes in the vertical format buffer. The C bit is ignored when A = 1.

The eight codes are assigned to home paper/end of forms, forms overflow, five unique skip codes which may be used multiple times per form, and the filler code, which is ignored. The detail bit interpretation is summarized in Table 7—10.

7.3.1.4. Advance

The advance command is used to initiate forms advance operations on the printer with no print operation being performed. The A, C, D, E and F detail bits (Table 7—10) of the advance command specify the mode of paper advance (7.3.1.3).

Device end status is presented by printer control after the VFB scan and at initiation of a paper advance to allow overlapping of the next command. Any error detected during the forms advance is indicated by unit check and device end status being presented when the next command is issued by the processor.

Table 7—10. Command Detail Bit Interpretation

A = 0	Detail Bits				A = 1
Advance Lines	**C**	**D**	**E**	**F**	**Interpretation**
0	0	0	0	0	Filler code*
1	0	0	0	1	Forms overflow
2	0	0	1	0	
3	0	0	1	1	Program selectable
4	0	1	0	0	Skip codes
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	Home paper/end of forms
8	1	0	0	0	Filler code*
9	1	0	0	1	Forms overflow
10	1	0	1	0	
11	1	0	1	1	Program selectable
12	1	1	0	0	Skip codes
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	Home paper/end of forms

*This code should not normally be specified in the command. If A = 1 and DEF = 000, paper advances to a position corresponding to the next position in the vertical format buffer containing the filler code.

7.3.1.5. Load Print Line Buffer

The load-print-line-buffer command initiates the transfer of data characters for one print line into the print line buffer as in the print-advance command. At the completion of the data transfer sequence, no printing operation or paper advance is initiated.

Successful completion of the command is indicated by device end status. If the command has been executed during a paper advance from a previous command and an error is detected on the paper advance, unit check and device end status are presented.

7.3.1.6. Read Print Line Buffer

The read-print-line-buffer command initiates transfer of the print line buffer contents to main storage. Unloading the buffer continues sequentially until 144 bytes have been transferred or until the processor indicates the end of data transfers (early termination).

Device end status indicates a successful completion of the command. If the command is executed during a paper advance from a previous command and an error is detected on the advance, unit check and device end status are presented.

7.3.1.7. Read Load Code Buffer

The read-load-code buffer command initiates transfer of the band identification code and space code, followed by the contents of the load code buffer, to main storage. The load code buffer is unloaded sequentially until 66 bytes (258 bytes with expanded character set feature) have been transferred or the processor indicates end of data transfers (early termination). The first byte transferred is the band identification code; bits 1—4 are set to 0 (Table 7—3).

Device end status is returned on successful completion of the command. If the command is executed during the paper advance from a previous command and an error is detected on the advance, unit check and device end status are presented.

7.3.1.8. Read Vertical Format Buffer

If A equals 0, the read-vertical-format-buffer command initiates transfer of the VFB contents to main storage. The VFB is unloaded sequentially beginning at the home paper location. Unloading continues until 144 (192 bytes if feature is installed) bytes have been transferred or the IPC indicates end of data transfers (early termination). Bits 0—4 of each transferred byte are set to 0 (Table 7—5).

If A = 1, the read-vertical-format-buffer command initiates transfer of the print line buffer (PLB) contents (Table 7—11), followed by contents of the VFB (Table 7—5).

Table 7—11. Print Line Buffer Byte Formats

PLB Location	Bits							
	0	1	2	3	4	5	6	7
1	0	0	0	0	0	0	1	2
1	0	0	0	0	0	3	4	5
1	0	0	0	0	0	6	7	P
2	0	0	0	0	0	0	1	2
2	0	0	0	0	0	3	4	5
2	0	0	0	0	0	6	7	P
•								
•								
•								
144	0	0	0	0	0	0	1	2
144	0	0	0	0	0	3	4	5
144	0	0	0	0	0	6	7	P

LEGEND:

P = Printed bit

The format of the data transferred from the PLB is indicated in Table 7—11. The maximum number of bytes depends on the VFB size. If the expanded character set feature is not installed, up to 576 bytes can be transferred. If the feature is installed, up to 624 bytes can be transferred. The VFB data format is identical to the read-vertical-format-buffer command when A = 0 (Table 7—5).

The variation of the read-vertical-format-buffer command permits software verification of the "printed" bit position in the print line buffer (7.2.3.1), which otherwise is not available. Device end status is returned when the command is successfully completed. If the command is executed during the paper advance from a previous command and an error is detected on the advance, unit check and device end status are presented.

7.3.1.9. Diagnostic

The diagnostic command initiates transfer of data characters for one print line into the print line buffer and is then followed by printing of the data transferred. Unlike the print-advance command, the diagnostic command does not initiate a line feed. Upon completion of this command, device end status is presented to the IPC. This command is provided for diagnostic use only; normal printer operation should not be predicated on the use of this command.

7.3.1.10. Sense

The sense command is used to interrogate printer control and store data in main storage which reflects unusual conditions detected during the last operation, and the current state of the printer. The sense command is executed regardless of the state of the printer (i.e., run/stop) and may be issued independently or as a response to unit check status. When the printer is in the run state, some sense indications may be cleared upon acceptance of a command other than the sense command. Failure to issue the sense command as a response to a status indication may result in a loss of the condition.

Printer control transfers two sense bytes to main storage as a result of the sense command. The first sense byte may contain summary information, with detailed information of the printer and printer control indicated in the second sense byte. Upon successful completion of the second sense byte, printer control terminates the condition and presents device end status to the IPC.

If the sense command is issued with the buffer control word (BCW) count (A) set to 1, printer control transfers two sense bytes; however, only the first sense byte is stored. If the sense command is issued with the BCW T bit set to 1, no sense bytes are transferred. Normal ending status is presented to the processor in either case. Unit check status is never set with device end status as a sense command.

7.3.2. Status Byte

The status byte supplies information pertaining to the state of the printer control. The status byte is presented to the IPC and stored as an IOSTIW (input/output status table interrupt word) in the buffered channel status word (BCSW) fields (3.5) when any of the following conditions are present:

1. As a unit check response to the start I/O (SIO) sequence
2. At the completion of a command
3. If an attention condition is detected

The status register in printer control is cleared when the IPC accepts the status byte. Status presented during an SIO sequence causes the appropriate condition code to be returned to the IPC and, if the command was rejected, subsequent status sequence causes the IPC to store an IOSTIW. The status bits and their meaning are listed in Table 7—12.

Table 7—12. Status Bit Designations (Part 1 of 2)

Bit Position	Designation	Interpretation
0	Attention	Indicates transition from the stop state to run state.
1	N/A	Set to 0 by printer control.
2	N/A	Set to 0 by printer control.
3	N/A	Set to 0 by printer control.
4	N/A	Set to 0 by printer control.
5	Device end	Indicates completion of a command initiated by the processor and readiness to accept a new command.

Table 7—12. Status Bit Designations (Part 2 of 2)

Bit Position	Designation	Interpretation
6	Unit check	Indicates at least one bit is set in sense byte 0 or 1.
7	Unit exception	Presented with device end status of either a print-advance or advance command and indicates a forms overflow condition. The paper advance is performed and the paper advances the number of positions specified by the command.

7.3.3. Sense Data Bytes

Sense data bytes presented by printer control are comprised in two categories:

1. Printer conditions (e.g., intervention required, equipment check) that result in the printer entering the stop state (Figure 7—14), and that are presented each time a sense command is issued until the condition is cleared by the operator. Under these conditions, no command can be executed and, if issued, causes unit check status to be presented.

2. Error indications (e.g., command reject), which may be cleared if a command other than sense is issued as a response to unit check status.

The name and position of the bits in each sense and status byte are listed in Table 7—13. Status and sense bits and associated indicators/switches are summarized in Figure 7—14.

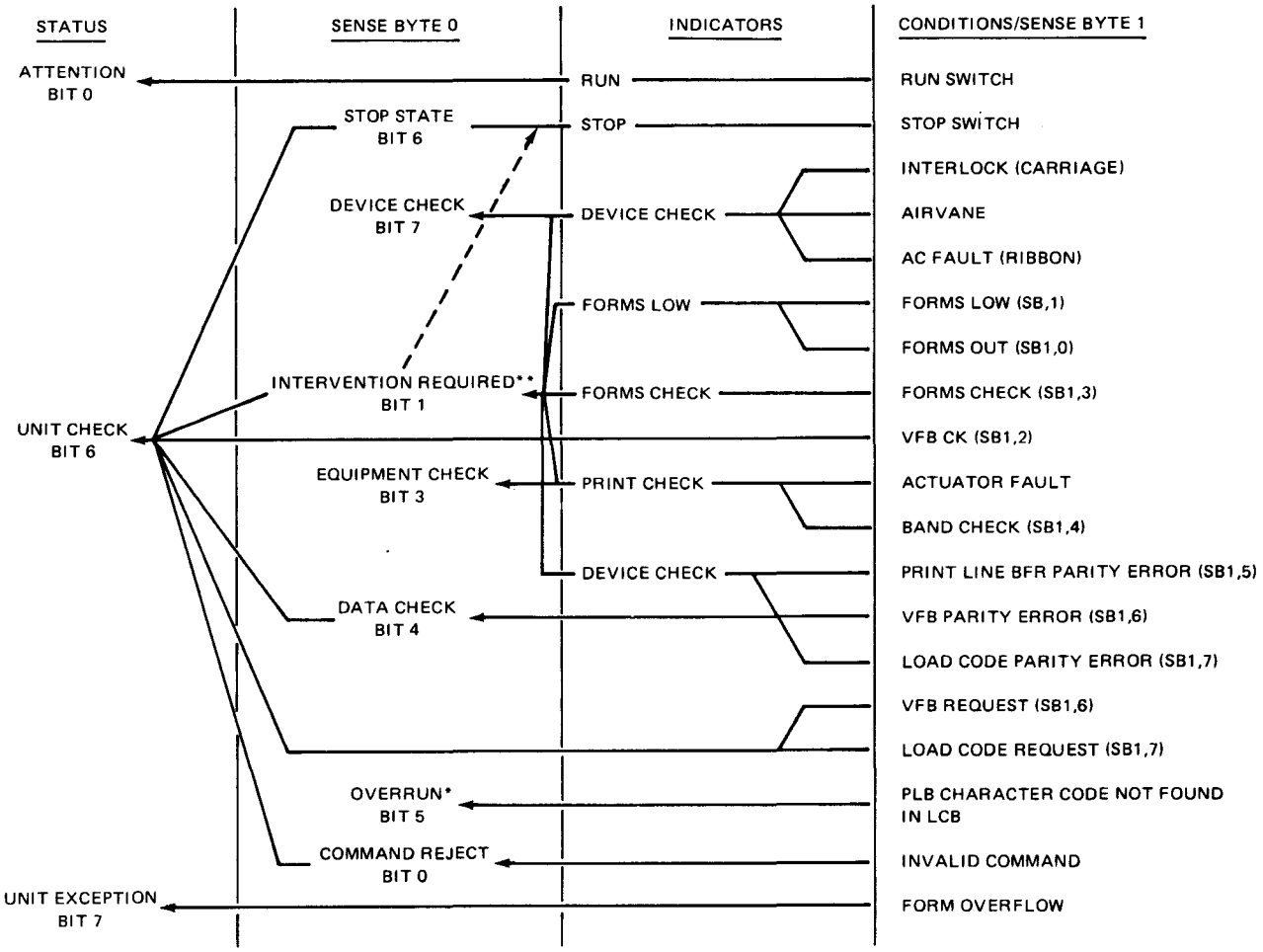
The meaning of the sense bits and the conditions under which they are set are listed in Tables 7—14 and 7—15.

Table 7—13. Printer Status and Sense Summary (Part 1 of 2)

Commands 01234567	Bit	Status	Sense 0	Sense 1	Operator	
					Switches	Indicators
Sense: XXXX0100	0	Attention	Command reject	Forms out	RUN STOP	RUN STOP
Diagnostic: XXXXX101	1	–	Intervention required	Forms low	HOME LINE SPACE	DEVICE CHECK
Print-advance: ACDEF001	2	–	–	VFB check	–	PRINT CHECK
Advance: ACDEF111	3	–	Equipment check	Forms check		OUT OF FORMS
Load PLB: 11100011	4	–	Data check	Band check		FORMS CHECK

Table 7—13. Printer Status and Sense Summary (Part 2 of 2)

Commands 01234567	Bit	Status	Sense 0	Sense 1	Operator	
					Switches	Indicators
Load Code BFR: 11111011	5	Device End	Overrun	Print line BFR Parity error		PARITY CHECK
Load VFB: 01100011	6	Unit check	Stop state	Vertical format request or parity error		
Read PLB: XXX00010	7	Unit exception	Device check	Load code request or parity error		
Read LCB: XXX01010						
Read VFB: AXX10010						



*Overrun may be inhibited from setting unit check (if bit 0 of the band identification code is set to 1).
**Parity errors on read-print-line-buffer or read-load-code-buffer commands do not cause entry into stop state.

Figure 7—14. Sense and Status Byte Summary

Table 7—14. Sense Data Byte 0 Bit Designations

Bit Position	Designation	Interpretation
0 (SB0,0)	Command reject	This sense bit indicates a command reject. Invalid command codes are any codes not listed in Table 7—12. This bit is generated during an SIO sequence whenever output of the command register is not decoded as a valid command. Unit check status is set and printer control becomes active.
1 (SB0,1)	Intervention required	This sense bit indicates that an operator intervention is required (Figure 7—12).
2 (SB0,2)	Bus out check	Not used, set to 0.
3 (SB0,3)	Equipment check	This sense bit indicates a print check. It is set if an actuator circuit check or band check (SB1,4) error is detected and also if either fuse check or latch check is detected.
4 (SB0,4)	Data check	This sense bit indicates a parity error detected in the vertical-format-buffer (SB1,6).
5 (SB0,5)	Overrun	This sense bit indicates an overrun condition. It is generated when there is one or more unprintable characters in the print line buffer; no matching code is found in the code buffer.
6 (SB0,6)	STOP state	This sense bit indicates that the printer is in the stop state. The printer enters the stop state via the STOP switch or an error condition (Figure 7—14).
7 (SB0,7)	Device check	This sense bit indicates a device check is required. It is generated when one of the following errors occurs and causes printer control to enter the STOP state: ■ Blower or ribbon check ■ Interlock active If device check status occurs during a print or advance command, the command is immediately terminated.

Table 7—15. Sense Data Byte 1 Bit Designations

Bit Position	Designation	Interpretation
0 (SB1,0)	Forms out	This sense bit indicates that the printer is out of paper. It is generated when an advance to or past home paper position has occurred after a forms low indication. Setting this bit causes entry into the stop mode and cannot be cleared until paper has been loaded in the printer.
1 (SB1,1)	Forms low	This sense bit is set if less than 6 inches of paper remains in the paper supply. The lower tractors may no longer contain paper. Setting this bit causes entry into the stop state; the run mode can be reentered until a forms out (SB1,0) is generated. Unit check status is only generated when this condition (forms low) is first detected.
2 (SB1,2)	VFB check	This sense bit indicates a paper runaway was detected during an advance setup sequence. It is set if an advance command is issued and the skip code, specified by the C, D, E, and F bits (A = 1), is not present in the vertical format buffer. No paper advance takes place.
3 (SB1,3)	Forms check	This sense bit indicates a forms check. It is set if any individual paper advance exceeds 1.1 seconds or a forms jam condition was detected.
4 (SB1,4)	Band check	This sense bit is set if no timing marks are detected within 1 millisecond, or an incorrect number of timing marks is detected between two font marks. Detection of timing marks begins 5 seconds after power is applied to the print band motor.
5 (SB1,5)	Print line buffer parity error	This sense bit is set if a parity error is detected when reading the print line buffer or during a print setup sequence.
6 (SB1,6)	Vertical format request/parity error	This sense bit is set if one of the following conditions is present: a. A parity error is detected when accessing the vertical format buffer. b. A print-advance or advance command was received after power turn on, system reset, or operator initialization of VFB, and no load-vertical-format-buffer command was issued.
7 (SB1,7)	Load code request/ parity error	This sense bit is set if one of the following conditions is present: a. A parity error is detected when accessing the load code buffer. b. A print-advance or diagnostic command was received after power turn on, system reset, or operator initialization of VFB, and no load-code-buffer command was issued.

7.3.4. Programming Considerations

The various application capabilities of the printer require that software be developed to fully utilize the printer capabilities. The following program requirements, described in subsequent paragraphs, must be considered in developing the appropriate software:

- Initiating print sequence
- Use of load code with expanded character set feature
- Print band motor speed recovery time
- Status byte considerations
- Error recovery

7.3.4.1. Printer Initialization

Before printing can be initiated following a power-up sequence, the program must issue the load-code-buffer and load-vertical-format commands. The printer control section can differentiate between a normal stop-to-run transition and a stop-to-run transition following a power-up sequence. With a normal stop-to-run transition, the printer presents status with attention (bit 0) set. However, following a power-up sequence printer control presents no status.

The LCB must be loaded before printing can commence, and the VFB must be loaded before a forms advance can take place. If the program attempts either of these operations without preloading as required, status is presented with the unit check (bit 6) set.

NOTE:

Before issuing either a load-vertical-format-buffer or load-code-buffer command, the operator must synchronize the forms with the VFB by performing the procedure specified in 7.2.5.2.

7.3.4.2. Print Band Speed Recovery Times

A print-advance command causes the print band to initiate movement if it is stopped. However, printing does not begin until after five seconds so that the print band may reach proper speed. This condition causes the device end bit to occur seconds later than it normally would. The print band motor automatically turns off if no printing has occurred for about seven minutes.

7.3.4.3. Status Byte Considerations

Status bytes present the IPC with information on status of the printer as well as on certain conditions of the last operation. To assist in understanding functions and uses of status bytes, the programmer should note the times that status is presented (7.3.2) and the conditions causing the unit check bit and/or unit exception bit to be set (Table 7—12). Error recovery/procedures from unit check and unit exception are described in 7.3.5.

7.3.5. Error Recovery

Operating status of the printer is supplied to the IPC so the programmer can monitor conditions at the printer and take proper action to terminate the operation, continue with other operations, or recover from erroneous programming or faulty operation. Figure 7—15 illustrates the areas affected by set bits of the status bytes and the procedure to be followed if recovery of operation is required. Subsequent paragraphs and flowcharts describe the recovery procedures. It should be noted that Figures 7—15 through 7—18 are flowcharts specifying in logical order various errors that may occur within the 90/30 integrated printer control and the 0773 printer, along with the resulting indications to software and the operator. The flowcharts also give the actions that should be taken by software and/or the operator in response to these error conditions.

7.3.5.1. Unit Exception

When bit 7 (unit exception) of the status byte is set, a forms overflow condition is detected (Table 7—12). Figure 7—15 provides a guide for further refinement of this information.

7.3.5.2. Unit Check

Unit check (bit 6) of the status byte is set when any sense bit of sense data byte 0, or any sense bit of sense data byte 1, is set. Recommended error recovery for a unit check condition is illustrated in Figure 7—15.

7.3.5.2.1. Intervention Required

When set, bit 1 of sense data byte 0 indicates that intervention is required to recover while in unit check condition. Figure 7—16 illustrates recommended recovery.

7.3.5.2.2. Equipment Check

When set, bit 3 of sense data byte 0 indicates an equipment check condition is present during a unit check condition. Figure 7—17 illustrates recommended recovery.

7.3.5.2.3. Buffer Errors

When set, bit 5 of sense byte 0 indicates an overrun, and one or more character codes in the PLB have no corresponding code in the LCB.

When set, bit 5 of sense byte 1 indicates that a parity error was detected while the printer control was accessing the print line buffer. Figure 7—18 illustrates the recommended recovery. When set, bit 2 of sense byte 1 indicates that the skip code of a print-advance or advance command was not located in the VFB. When set, bit 6 of sense byte 1 indicates that a print-advance or advance command was issued to the printer control before a load VFB command was received after power turn on, system reset, operator initialization of the VFB or data check, provided bit 4 of sense byte 0 is not set. If set (bit 4 of sense byte 0), a parity error was detected while the printer control was accessing the VFB. When set, bit 7 of sense byte 1 indicates that a parity error was detected while the printer control was accessing the LCB, or that a diagnostic print or print-advance command was issued to the printer control before a load LCB command was received after power turn on, system reset, or operator initialization of the VFB. Figure 7—18 illustrates recommended recovery.

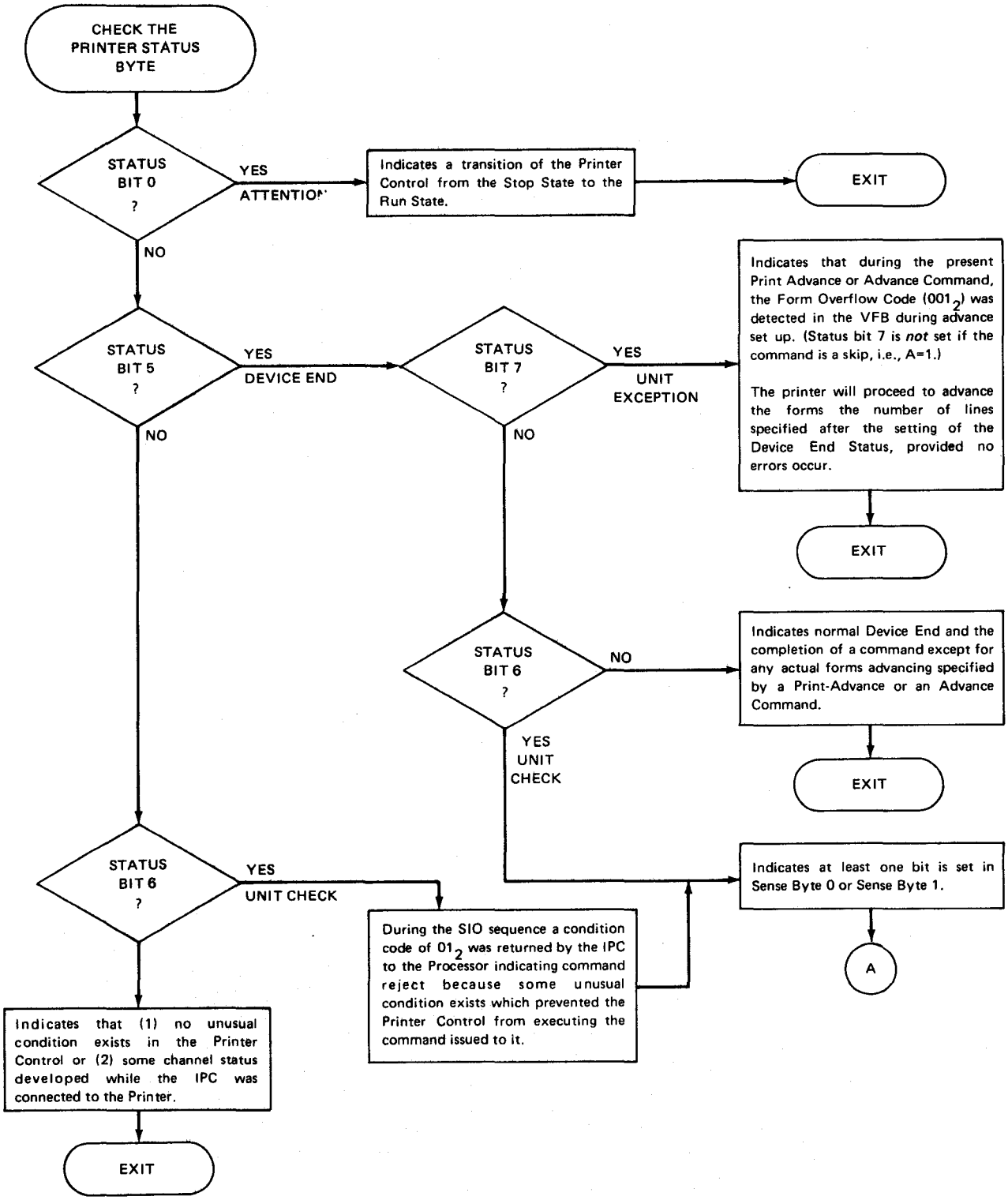


Figure 7—15. Conditions Indicated by Status Byte

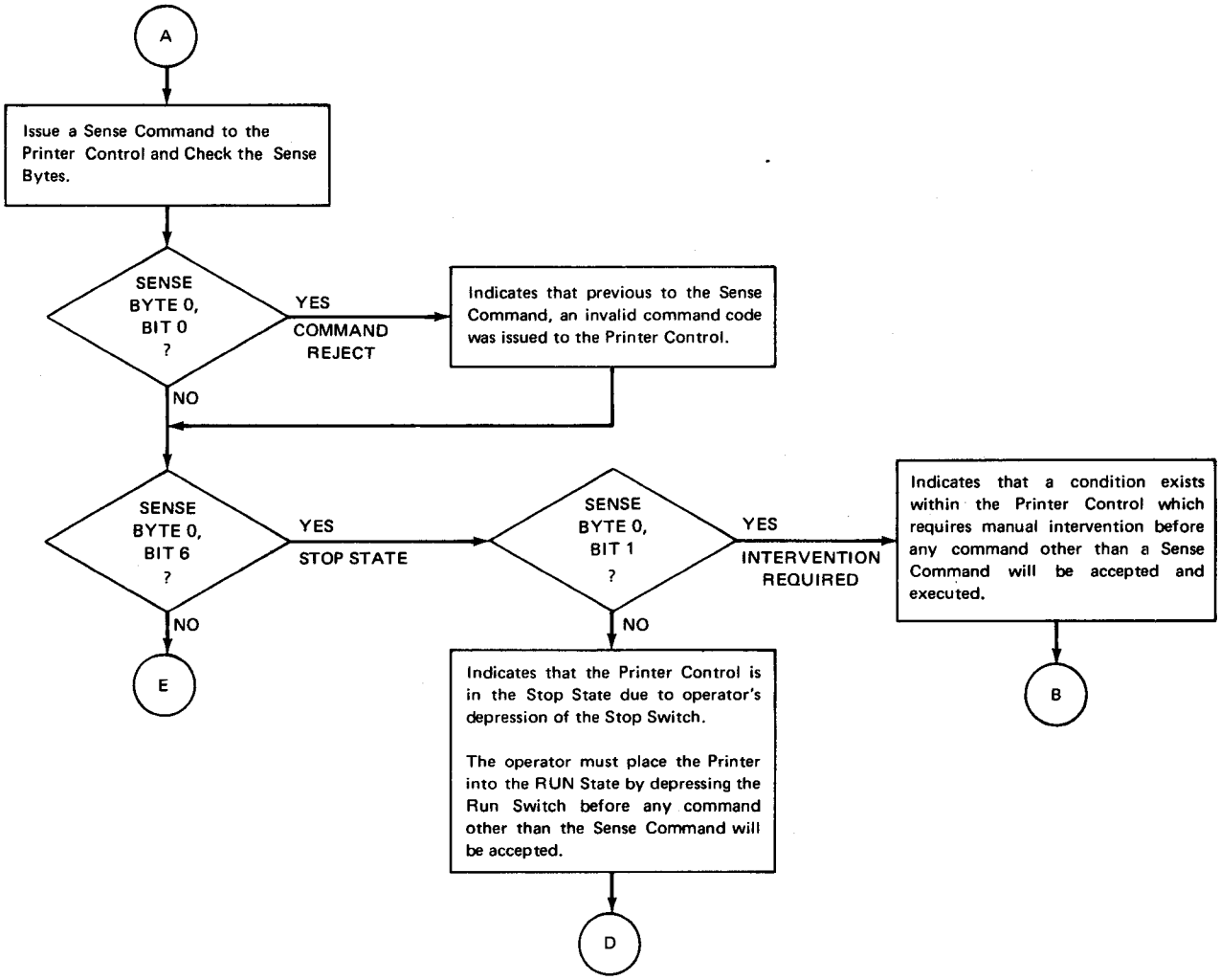


Figure 7—16. Intervention Required Error Recovery Flowchart

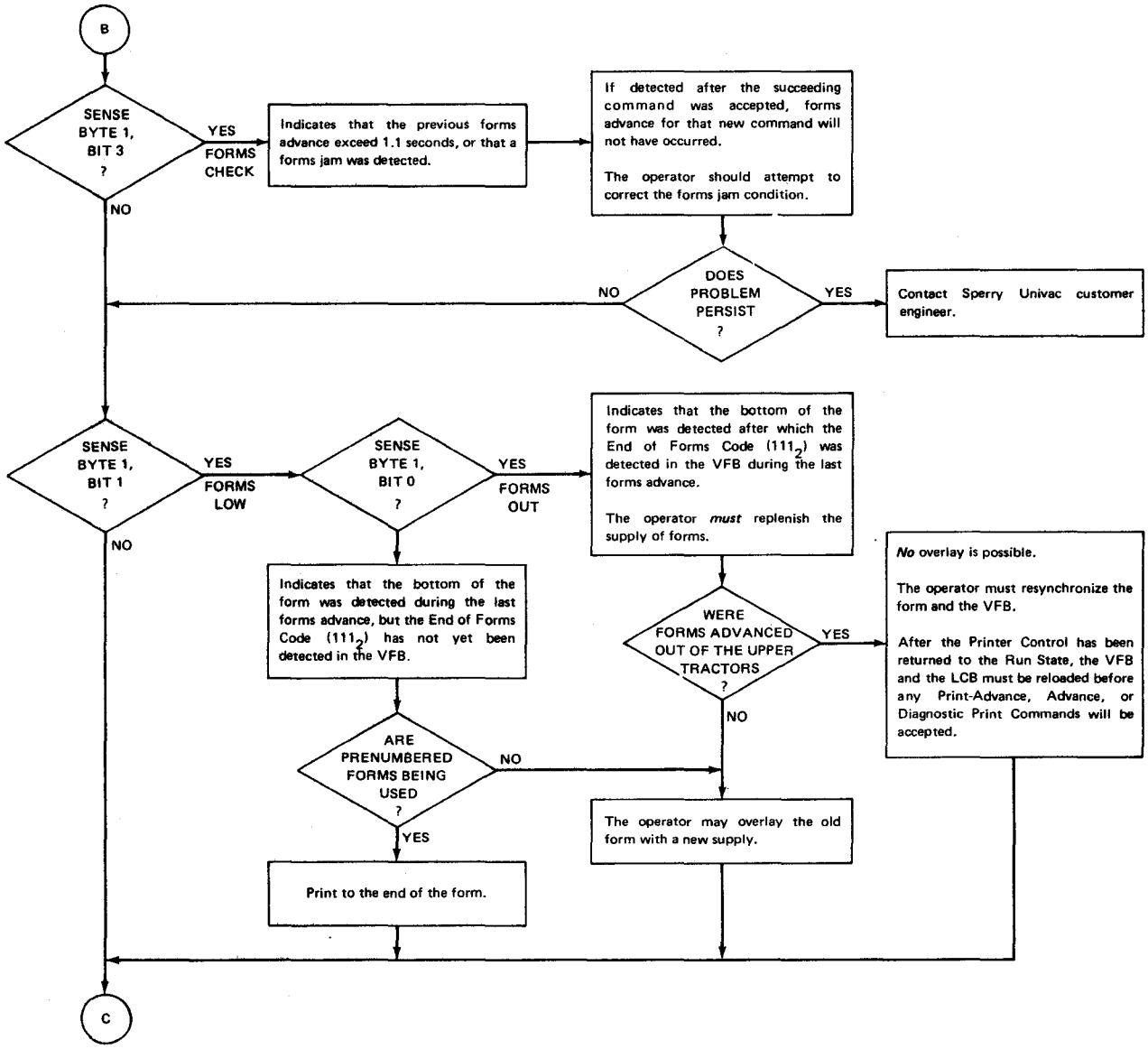


Figure 7—17. Equipment Check Error Recovery Flowchart (Part 1 of 2)

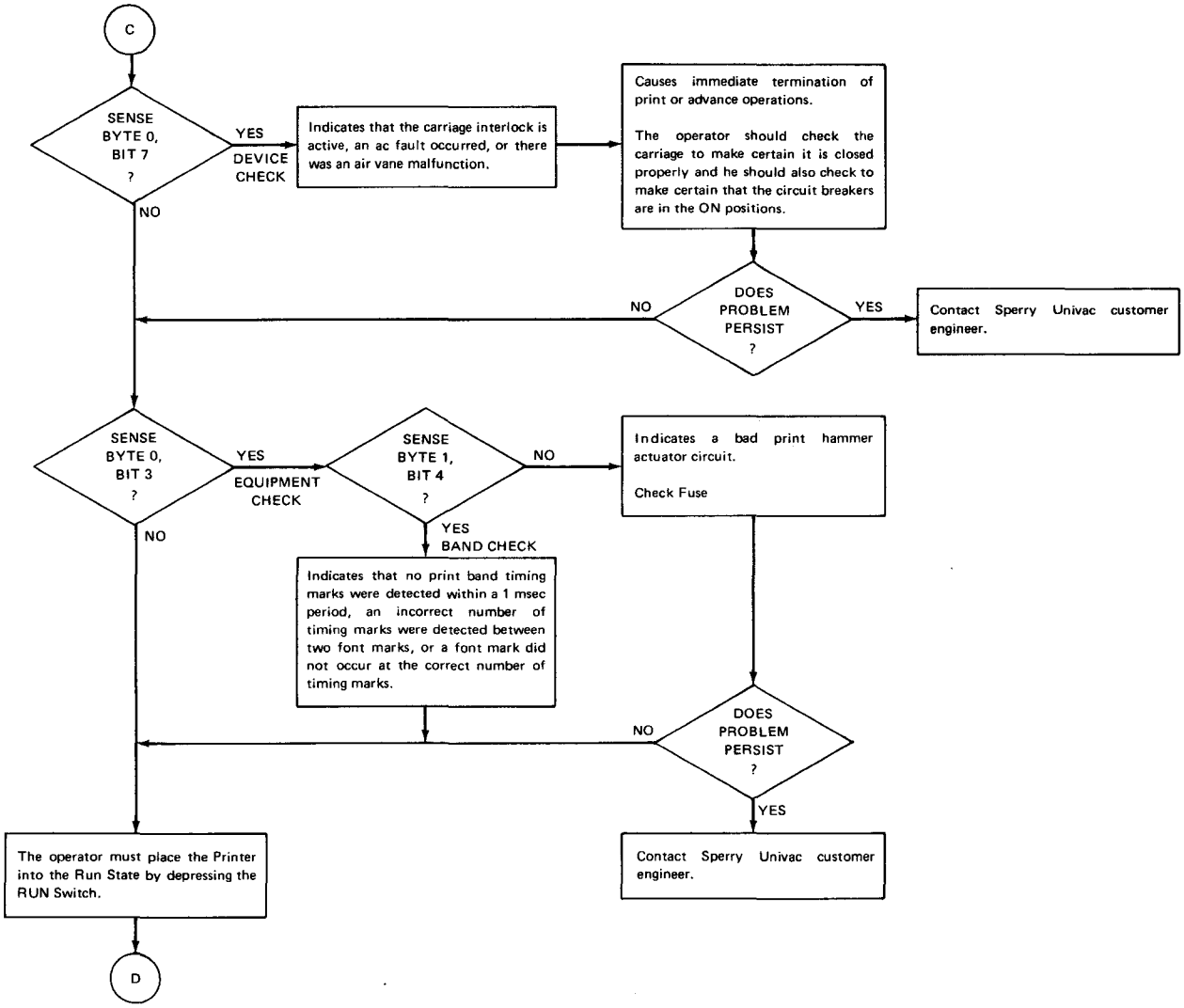
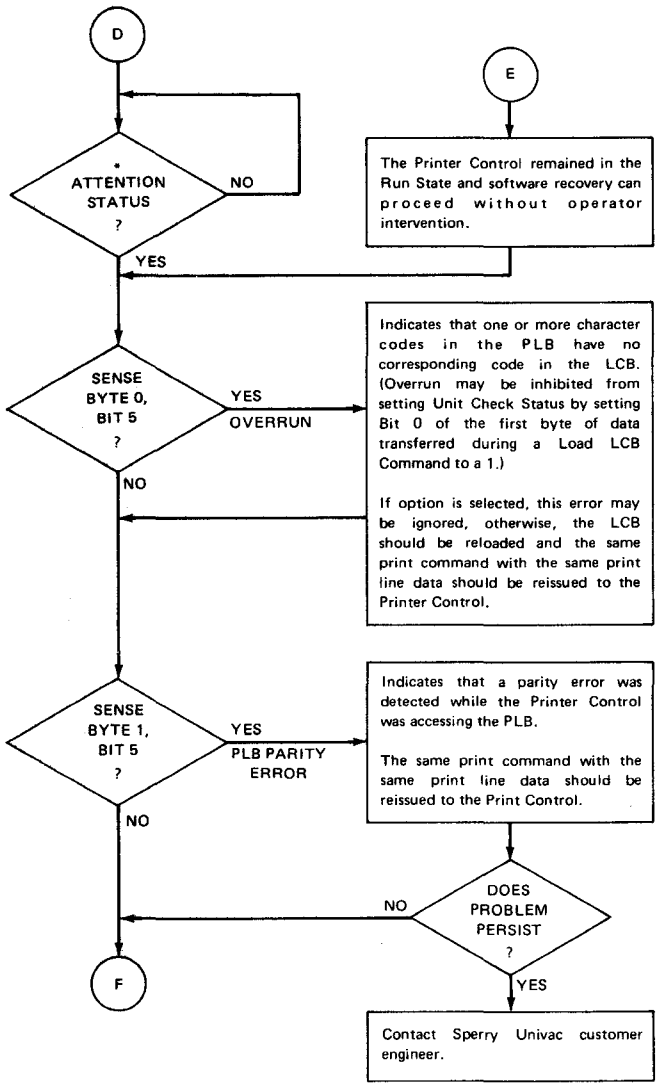


Figure 7—17. Equipment Check Error Recovery Flowchart (Part 2 of 2)



*All the Sense Bits should be processed before having the operator place the Printer Control back into the Run State, however, software recovery cannot continue beyond this point until the Attention Status for the Stop-to-Run transition is received indicating that the Printer Control is ready to accept and execute commands issued to it.

Figure 7—18. Buffer Error Recovery Flowchart (Part 1 of 2)

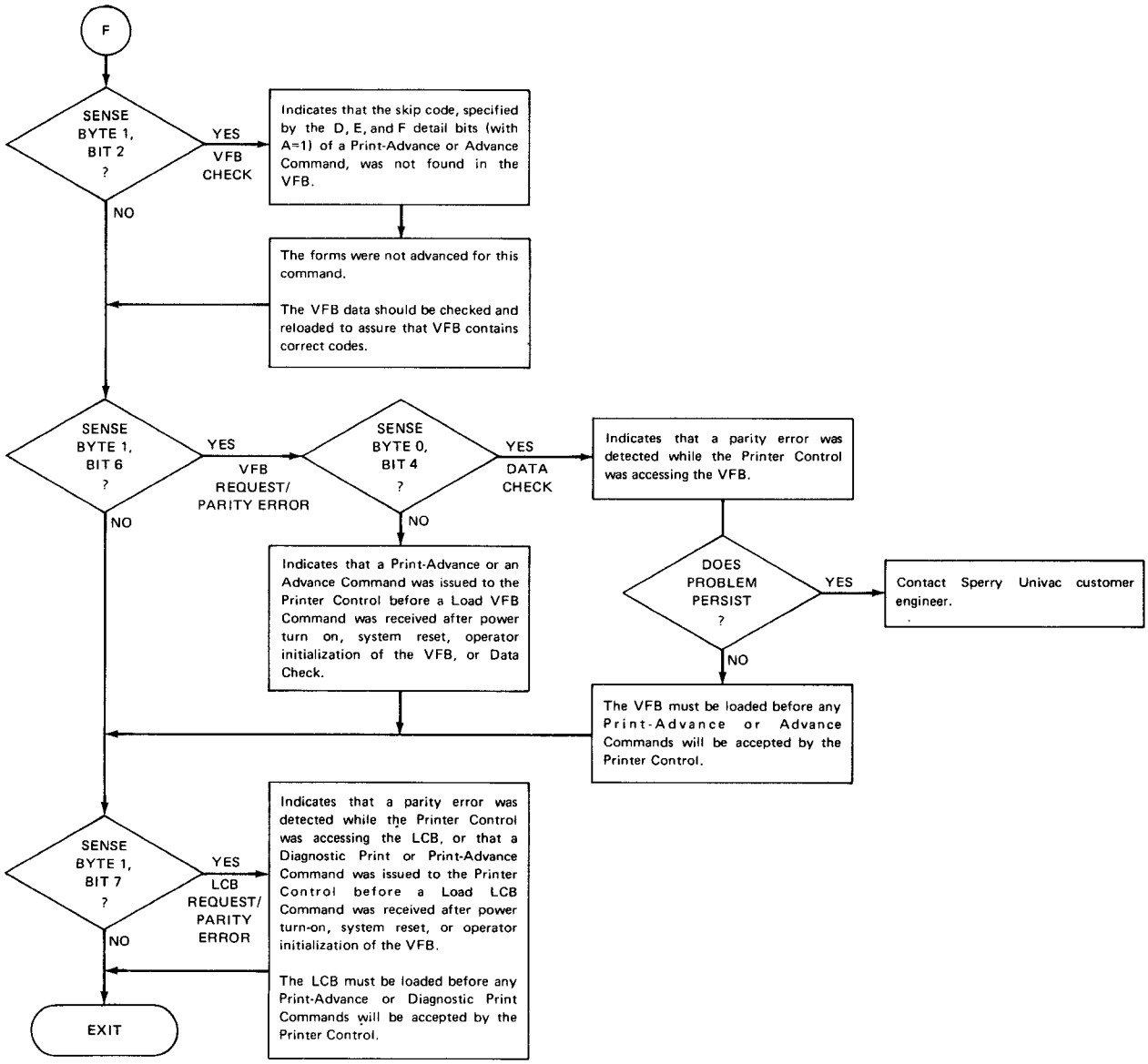


Figure 7—18. Buffer Error Recovery Flowchart (Part 2 of 2)

8. Communications Adapter

8.1. GENERAL

The communications adapter (CA) is basically a control unit that interfaces with the 90/30 processor IPC through the diskette/communications adapter interface (D/CA) feature. The CA provides the processor with a communications capability for controlling up to 12 half-duplex or 6 full-duplex communications lines. In dual configuration, up to 24 half-duplex or 12 full-duplex lines can be controlled. These lines may be private communications lines, switched network lines, telegraph lines, or lines for other common carriers in the United States or Europe. Line speeds of up to 56K bytes per second are accommodated.

8.2. SUBSYSTEM DESCRIPTION

The ICA is composed of three basic parts. These are:

- interface to the D/CA;
- communications multiplexer module (CMM); and
- up to 12 communications line adapters (LA).

The CA performs the tasks required to interface between the processor IPC and a communications line. These tasks include staticizing/serializing characters, synchronization, asynchronous timing control, parity checking and generation, and detection of control characters. Line adapters provide the interface between the CA and modems, telegraph lines, and automatic calling units.

8.2.1. Characteristics

The CA characteristics are listed in Table 8—1.

Table 8—1. CA Characteristics

Item	Characteristic
Data rate (aggregate with no diskette attached)	Up to 37.8K bytes per second, based on LA speeds of up to 56K bytes per second
Data rate (aggregate with diskette)	Up to 32.8K bytes per second
Power requirements (derived from processor)	+5 volts (±6%), 30 amperes —12 volts (±5%), 2 amperes 220 Vac, 50/60 Hz, for cooling fan
Number of commands	21 commands in operational command repertory, and 5 additional commands for diagnostics
Communications lines accommodated	Half duplex: Single configuration: 12 Dual configuration: 24 Full duplex: Single configuration: 6 Dual configuration: 12

8.2.2. Configuration

The CA consists of a single unit equipped with all necessary components to operate with the 90/30 processor through the D/CA. The CA is located in the console stand abutting the processor cabinet, and is electronically connected to the processor through the IPC and appropriate interface hardware. Figure 8—1 illustrates the functional arrangement of the CA and processor. Figure 8—2 illustrates the CA configuration. The CA optional features are listed and described in Table 8—2.

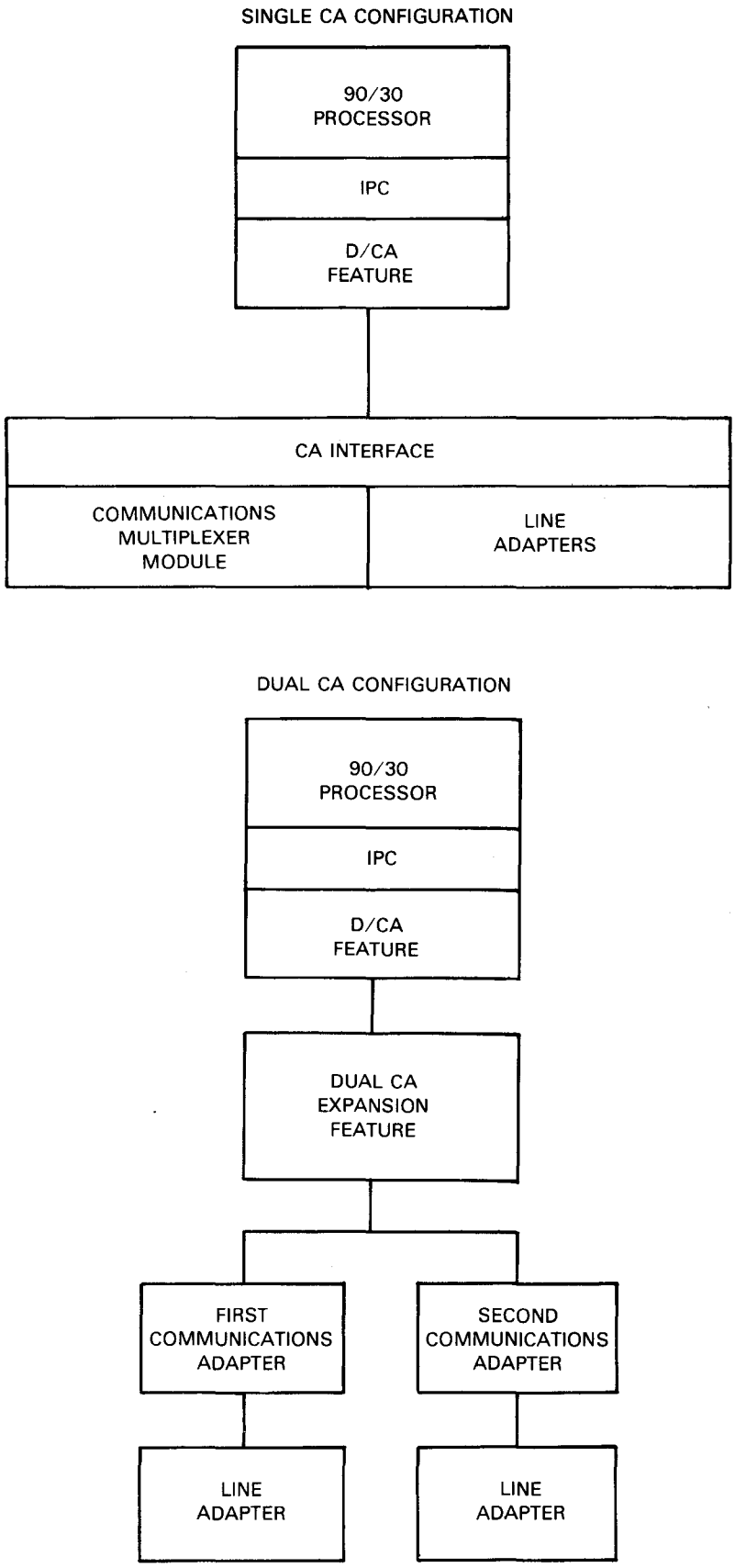
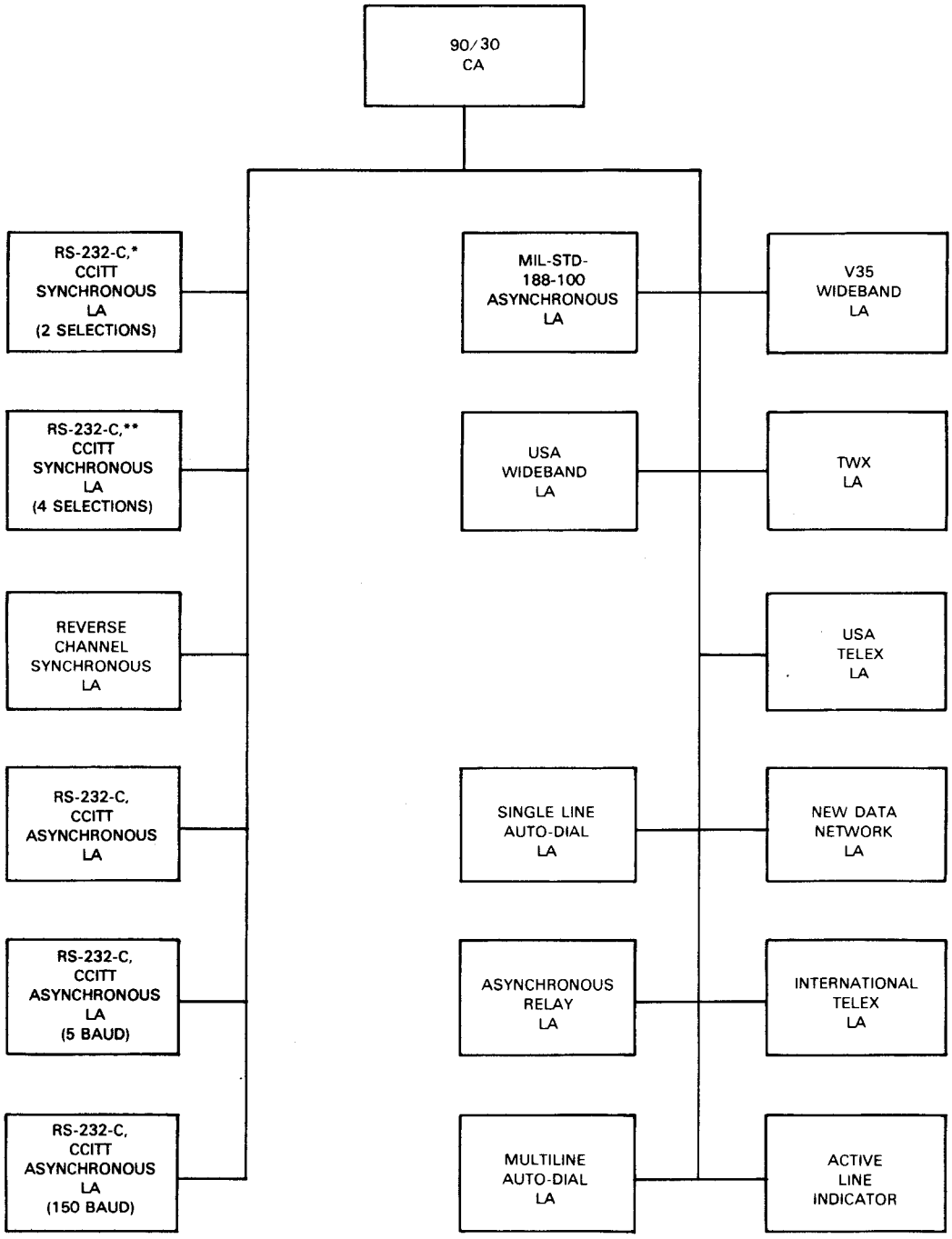


Figure 8—1. CA Functional Arrangement



*Selections:
Modem or DCM cable
Direct connection cable

**Selections:
Normal MIL
Inverse data
Inverse clock
Inverse data and clock

Figure 8—2. CA Configuration of Optional Features

Table 8—2. CA Type and Optional Features (Part 1 of 2)

Item	Description
90/30 Communications Adapter (single configuration)	Includes basic CA with location for 12 line adapters comprised of 6 full-duplex or 12 half-duplex. Used for single 90/30 CA configuration, or as the first CA in a 90/30 dual CA configuration. Requires diskette/communications attachment (D/CA) feature in the processor.
90/30 Communications Adapter (dual configuration)	Same as CA for single configuration except used as the second CA in a dual 90/30 CA configuration. Requires D/CA, first D/CA and second D/CA features.
RS-232-C, CCITT Synchronous LA Feature	Provides full duplex interface to synchronous data sets conforming to RS-232-C and CCITT Recommendations U24 and U28 for data communications. Provides two cable selections: ■ Cable, Modem, or DCM — Provides normal cable in lengths up to 50 feet. ■ Cable, Direct Connection — Provides a UNISCOPE Terminal Multiplexer with direct connection cable in lengths up to 50 feet for connection to the junction box.
RS-232-C, CCITT Synchronous LA Feature	Same as synchronous CA for 2 selections except permits exact compliance with MIL-STD-188-100 Low Level Interface Specifications. Control line polarity is in accordance with RS-232-C. Provides four cable connections: ■ Normal Military Standard — Standard offering with normal MIL-STD-188-100 polarity. ■ Inverse Data — Inverse data polarity with normal (RS-232-C) clock polarity. ■ Inverse Clock — Normal data polarity with inverse clock polarity. ■ Inverse Data and Clock — Inverse data polarity with inverse clock polarity.
Reverse Channel Synchronous LA Feature	Same as synchronous LA for 2 selections, except also provides reverse channel with up to 150 baud asynchronous operation. Requires two parts.
RS-232-C, CCITT Asynchronous LA Feature	Provides full duplex interface to asynchronous data sets conforming to RS-232-C and CCITT Recommendations U24 and U28.
RS-232-C, CCITT Asynchronous LA (5 baud) Feature	Same as asynchronous LA (above) but also provides reverse channel of up to 5 baud 202 type.
RS—232-C, CCITT Asynchronous LA (150 baud) Feature	Same as asynchronous LA (above) but also provides reverse channel with up to 150 baud asynchronous operation. Requires two parts.
MIL-STD-188 100 Asynchronous LA Feature	Same as asynchronous LA (above) except permits exact compliance with MIL-STD-188-100 low level interface. Control line polarity is according to RS-232-C. Selections permitted: ■ Normal Military Standard — Normal MIL-STD-188-100 polarity for data. ■ Inverse Data — Inverse data polarity; according to RS-232-C polarity.
U.S. Wideband LA Feature	Provides synchronous full-duplex interface to the 301B2 data set or to Bell Telephone 303 data set. The LA has a maximum data rate of 56K bps.
Single Line Auto-Dial LA Feature	Provides the interface to both rotary or touch tone auto dialing units. Requires LA location for each dialing unit.
Asynchronous Relay LA Feature	Provides asynchronous full duplex interface optionally compatible with either 20-75 MA neutral or 10-40 MA polar telegraph line.

Table 8—2. CA Type and Optional Features (Part 2 of 2)

Item	Description
Multi-Line Auto Dial LA Feature	Same as single-line auto dial LA (above), except permits interface to two auto dialers from a single line adapter position.
V35 Wideband LA Feature	Same as U.S. Wideband LA (above), except interface conforms to V35 requirements.
TWX LA Feature	Allows interface to domestic TWX network.
U.S. Telex LA LA Feature	Allows interface to Western Union Telex network in the U.S.
New Data Network LA Feature	Reserved for future LA development for interfacing new data networks.
International Telex	Allows interface to international Telex lines.
Active Line Indicator Feature	Provides a display panel to display line activity on up to 12 half-duplex or 6 full-duplex communications lines.

8.2.2.1. Single CA

The single CA configuration supports 6 full-duplex or 12 half-duplex communications lines. These lines are identified within the IPC by device addresses 04_{16} through $0F_{16}$, inclusive.

Software controls the communications lines through use of 12 IPC buffer control words (BCW). These BCWs reside in main storage locations 00140_{16} through $001FF_{16}$, inclusive.

The maximum CA data throughput accommodated by the IPC is 37.8K bps. This rate is achieved when the CA accommodates two full-duplex lines operating at 56K baud. All lines have an 8-bit character length for those applications.

8.2.2.2. Dual CA

The dual CA configuration supports 12 full-duplex or 24 half-duplex communications lines. The communications lines within the CA are identified by device addresses 14_{16} through $1F_{16}$, inclusive. Device addresses 10_{16} through 13_{16} are used for diskette drives.

A nonoperational condition code (11_2) is presented to the processor when an SIO instruction addresses a CA that is not present.

Software controls the communications lines in the dual CA configuration through use of 24 BCWs for CA number 1 reside in main storage locations 00140_{16} through $001FF_{16}$, inclusive. BCWs for CA number 2 reside in main storage locations 00340_{16} through $003FF_{16}$ inclusive.

The maximum throughput accommodated by the IPC for dual CA configuration is 34.6K bps. Combined throughput of both CAs must not exceed this value.

The diskette/communications attachment (D/CA) feature is shared by CA. During SIO sequences, bit 27 of the IPC device address is examined. If this bit is zero, the sequence addresses CA number 1, if the bit is 1, the CA addresses CA number 2. The device address sent to the CAs consist of bits 28 through 31 of the IPC device address. Bit 27 is not sent to the CAs.

Data transfers and status sequences are allocated to the CAs on a priority basis. Separate, but identical priority networks exist for each sequence. Status requests and data service requests are treated separately. Each CA is served on a first-come-first-served basis, when no conflict exists.

When a contention situation arises, the priority networks resolve the conflict. Normally, CA number 1 has priority over CA number 2. This rule is waived when CA number 2 has an outstanding data service request when CA number 1 is granted a data transfer sequence. When this arises, the next data transfer sequence allocated is given to CA number 2. Thus CA number 1 cannot lockout CA number 2.

The same mechanism is used for status sequencing. This priority scheme results in a restriction that communications lines operating at speeds over 9.6K bps must be connected to CA number 1.

During all data transfer and status sequences the CAs send a four bit device address. These bits correspond to bits 28 through 31 of the IPC device address. Bit 27 of the IPC device address is furnished by the dual CA feature. If CA number 1 is assigned, bit 27 is zero. If CA number 2 is assigned, bit 27 is one.

8.2.3. Line Adapters

Line adapters convert signal levels into logic levels, and vice versa. Each LA transfers data one bit at a time to or from the communications multiplexer module (CMM) via multiplexer ports. The CA transfers data one character at a time to or from the processor through the IPC. The CA interface logic performs all required functions to interface the CMM to the D/CA feature and the IPC.

Interface to communications equipment such as modems, telegraph lines, and automatic dialers is provided by the LAs. One LA is required for each communications channel. Two LAs are required for automatic dialing; one for the modem, and one for the automatic calling unit.

The LAs are plug-in modules that can be plugged into any adapter position in the CA. Each LA module contains input and output sections that operate independently. One LA module interfaces with either a full-duplex or half-duplex line.

An LA used to simultaneously transmit and receive data (full-duplex operation) requires access to two CMM ports. There are 12 CMM ports in the CA.

An asynchronous LA transmits and receives asynchronous start-stop characters. Transmit/receive timing is controlled by the CMM. Asynchronous LAs may be used for half- or full-duplex mode. Full-duplex mode requires two CMM ports.

A synchronous LA transmits and receives synchronous data, with timing supplied by the modems. The synchronous LAs can transmit and receive data up to 20K bytes per second. Synchronous LAs can operate in either full- or half-duplex mode; full-duplex requires two CMM ports.

8.2.4. Communications Multiplexer Module

The CMM provides the following functions:

- Assemble data bits from LAs into characters.
- Disassemble characters from the processor to appropriate LAs into serial bit form.
- Initiate transfer of assembled character to and from the processor through the IPC.
- Automatically establish character synchronization on synchronous input lines.

- Provide 16 asynchronous timing rates selectable by software.
- Activate and deactivate communications lines commanded by software.
- Generate and check character parity; odd, even, or no parity is selected by software.
- Generate and check block parity; odd or even parity is selected by software.
- Generate and check cyclic redundancy check (CRC) characters.
- Control character detection; control characters are specified by software.
- Automatic insertion and detection of SYN or DLE SYN characters.
- Hardware aids for diagnostics.

8.2.4.1. M Register and Line Control Registers

The main (M) register contains the port control word for each line when that line is scanned. The port control word consists of the character assembly/disassembly field, character input/output buffer field, character size field, asynchronous timing countdown, line speed selection field, line control flags, status field, interval timers, block check character (BCC) field, CRC field, and parity control.

The control word resides in the line control register when not in the M register. Pertinent machine control logic is keyed from contents of the M register. Line parameters and commands for each port are written into the word for that port when it resides in the register stack. Other fields in the word are used as working areas by the CMM when executing commands.

Software locates control words in the control character detect table in the required order, and also performs any required bit transposition of data characters.

The port control word contains a field that counts down from the major cycle clock to derive asynchronous clock rates (as defined by another field). The rates are listed in Table 8—3.

Table 8—3. CMM Asynchronous Clock Rates per Second

45.45	150
50	200
56.88	300
74.20	600
75	1050
100	1200
110	1800
134.5	2400

A field of the control word is used to define character lengths. Allowable lengths are 5, 6, 7, and 8 bits, exclusive of parity. Eight bits plus parity is not allowed.

A field of the control word is used to define the following line characteristics:

- Synchronous input with a specific start character
- Synchronous input with any good parity non-SYN code as the start character
- Synchronous output with a 4-SYN character preamble
- Synchronous output with a 2-pad + 2-SYN character preamble
- Asynchronous output, stop element = 1 unit interval
- Asynchronous output, stop element = 1.5 unit interval
- Asynchronous output, stop element = 2 unit interval

8.2.4.2. Control Character Detection

The port control word contains a field that allows selection of any of four character sets. Four control character detect tables are available and loaded by software.

Code functions recognized by the CMM are listed in Table 8—4.

Table 8—4. Code Functions Recognized by CMM

ASCII Defined Characters	Function
SYN, DLE SYN	Synchronization/sync idle
SOH, STX, EOT, DLE, ENQ, ACK, NAK	Specified synchronous start
SOH, STX, DLE SOH, DLE STX	LRC or CRC start
ETX, ETB, ITB, DLE ETX, DLE ETB, DLE ITB	LRC or CRC end
ETX, ETB, EOT, ENQ, DLE, ACK, NAK, DLE ENQ	Look for SYN-at-end and generate status. Look-for-sync is delayed until the last character of a sequence is received.
DLE EOT	Disconnect

NOTE:

The program load code may use any bit pattern to represent these functions. A no-operations reference (no-op) may be loaded when a particular function is not required.

8.2.4.3. Parity Generation and Checking

Error control combinations are selected by the program. Standard conventions, as well as those required for binary synchronous communication (BSC) and Sperry Univac nonstandard conventions, are included.

Block check character (BCC) computation for a control interpretation table parameter specifies: "Message End Character included/excluded in Summation".

CRC computation in either BSC or ASCII transparent mode uses the following conventions:

1. CRC generation begins with the first appearance in a message or transmission block of either TSOH or TSTX.

2. CRC generation stops by appearance of TETB, TETX, or TITB.

3. The following characters are included in CRC generation:

Sequence	Characters in CRC Accumulation	
	Yes	No
TSYN	—	DLE SYN
TSOH	—	DLE SOH
TSTX*	—	DLE STX
TSTX**	STX	DLE
TSTS***	DLE STX	—
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	DLE (one)	DLE (the other)
TITB	ITB	DLE
TENQ	ENQ	DLE

*If not preceded within the same block by transparent heading information. This could be with no heading for nontransparent heading.

**If preceded within same block by transparent heading information (American National Standards Institute standards). However, transparent headings must be handled by the CA as separate transmission blocks terminated by DLE ETB.

***If preceded by ITB CRC when operating BSC.

Polynomial codes selected for parity checking and generation are:

1. $X^{16} + X^{15} + X^2 + 1$ (CRC—16)

2. $X^{16} + X^{12} + X^5 + 1$ (CCITT)

3. 16-degree strap selected

4. $X^{12} + X^{11} + X^3 + X^2 + X + 1$ (CRC—12)

The polynomial used by the cyclic redundancy check (CRC) is stored in the CMM.

An input operation is not terminated when a character parity error is detected. The status byte with unit-check and device-end bits set is transferred after the message-end character is received.

The LRC and CRC accumulation is always located after the message-end character.

Character parity bits are stripped by the CA. In transparent ASCII version of BSC, all eight character bits are treated as data bits.

8.2.4.4. Timers

The CA contains the necessary timers to properly interface communications services. This includes modem interface timing requirements, BSC sync insertion, and timing required for extended received spacing signals.

Specific extended spacing conditions that are timed are: break, disconnect, and open line. Table 8—5 lists the CA timers with a brief description of each.

Table 8—5. CA Timers

Name	Function
Break	Any steady spacing input signal lasting from 180 msec to 750 msec. Unit-check status is presented and break sense bit is set.
Disconnect	Any steady spacing input signal lasting from 750 msec to 3 seconds. The CA disconnects from the line, presents unit-check-device-end-status, and the disconnect sense bit is set.
Open line	A steady spacing input signal longer than 3 seconds. Unit-check status is presented and the open-line sense bit is set.
Space to mark	Any steady spacing signal longer than 180 msec and terminated by a space to mark a transition. Unit-check status is presented and the space-to-mark sense bit is set. This timing may be coincidental with other CA timer sense bits.
BSC sync insertion	Character sequences SYN SYN or DLE SYN are inserted in BSC operations once each second. A timer and mechanism to perform the insertion is implemented in the CA. Characters are not inserted between ETB, ETX, ITB, DLE ITB, DLE ETB, or DLE ETX and the next following BCC. They are not inserted between DLE and any following character of a DLE sequence.
Line procedure	Provides up to 34 seconds for timing response and receive or connection time. Time out generates unit-check status, and the line-procedure-timer sense bit is set.
Modem interface	Assures that the request-to-send and data-terminal-ready modem interface signals, when turned off, will remain off for at least 50 msec or until the input end-of-message is detected. Actual CCM timer may vary from 51 to 68 msec. The timer is started by any command causing request-to-send or data-terminal-ready to turn off, even if the signal is strapped to a continuous *on* state in the LA. The timer can be stopped by any command that turns off the port (e.g., send mark), thus providing software with the capability of overriding the timer; however, software must assume responsibility if this is done, and for meeting interface timing requirements of nonsupported modems. If a single software timer is used for timing the data-terminal-ready-off state for all supported modems, at least 4 seconds duration is recommended.

8.2.5. Transparent Operation

Transparent operation allows data to be transferred to a remote station without restrictions on binary format of data. The transparent operation requires the CA to insert a DLE character when a character within the data has the same bit configurations as the DLE character.

The transmitter must know how to permit transmission of a true DLE ending sequence without inserting a DLE character that breaks the ending sequence, thus making it unrecognizable to the receiving station. The CA accomplishes this with the LAST BYTE signal from the IPC, as described in subsequent paragraphs.

8.2.5.1. Transparent-Output Mode

The CA enters transparent-output mode when it receives the 2-character sequence DLE STX or DLE SOH (where control interpretation bit 9=1 for STX or SOH). While in the transparent-output mode, the CA performs the following functions:

1. The CA ceases to respond for all control characters except DLE.

2. Upon decoding a DLE control character in the data stream, the CA inhibits it from inclusion in the BCC accumulation, and it transmits the DLE on the following conditions:

    a. If the next character received from the IPC is not accompanied by the LAST BYTE signal, the CA generates a second DLE to form the DLE DLE sequence and includes it in the BCC accumulation. After the inserted DLE is transmitted, the CA transmits the character received from the IPC. This requires a transparent heading to be sent as a separate transmission block that is terminated by DLE ETB. Characters DLE STX are treated as a data sequence, and the DLE is duplicated without the LAST BYTE signal.

    b. If the next character from the IPC is accompanied by the LAST BYTE signal, the CA does not generate a second DLE but transmits the character received from the IPC. This should be an ending character and is included in the BCC accumulation.

3. The CA inserts DLE SYN characters in the data stream as a time fill when data is not available from the IPC. The time fill DLE SYN is not included in the BCC accumulation.

8.2.5.2. Transparent-Input Mode

The CA enters transparent-input mode upon receipt of the 2-character sequence DLE STX or DLE SOH. While in this mode, the CA operates as follows:

1. The CA ceases to recognize all control characters except DLE.

2. Upon decoding DLE, the CA remembers detection of DLE, inhibits its inclusion in the BCC accumulation, deletes DLE from the data stream, and examines, the next received character. If the next character is:

    a. One of the ending characters ETX, ETB, or ENQ, the CA performs a normal ending as though the characters were received in a normal text transmission.

    b. Another DLE character, the CA treats it as a transparent data character; i.e., it is included in the BCC accumulation and transferred to the IPC. The CA then returns to transparent operation, where it acts only on the DLE character.

c. A SYN character, the character is deleted from the data stream and from BCC accumulation. The CA returns to transparent operation.

d. An ITB character, it indicates that the following characters are the BCC. Transparent mode is reset, but the CA remains in input mode and begins accummulating a new BCC. To reenter transparent mode, DLE STX must be received. Both the DLE and STX characters are included in the new BCC accumulation.

8.3. PROGRAMMING

This section contains programming reference information for the CA. In particular, information is directed toward processing the CA command bytes, status bytes, and sense data bytes.

8.3.1. Commands

The CA recognizes as valid the commands listed in Table 8—6, and described in 8.3.1.1 through 8.3.1.2.1. The upper two bits (bits 6 and 7) of all command codes are ignored by the CA, unless noted otherwise.

Table 8—6. CA Commands (Part 1 of 3)

Command	Hex	Bits							
		0	1	2	3	4	5	6	7
No-op	00	0	0	0	0	0	0	0	0
Enable data output	01	0	0	0	0	0	0	0	1
	or								
	41	0	1	0	0	0	0	0	1
Enable data output with automatic turnaround	81	1	0	0	0	0	0	0	1
	or								
	C1	1	1	0	0	0	0	0	1
Dial	05	0	0	0	0	0	1	0	1
Send space	11	0	0	0	1	0	0	0	1
Send mark	0D	0	0	0	0	1	1	0	1
Send idle	09	0	0	0	0	1	0	0	1
Enable data input	02	0	0	0	0	0	0	1	0
New sync	0A	0	0	0	0	1	0	1	0
Look for sync	06	0	0	0	0	0	1	1	0
Turn off	03	0	0	0	0	0	0	1	1
Clear active	0E	0	0	0	0	1	1	1	0
Disconnect	13	0	0	0	1	0	0	1	1
Sense	04	0	0	0	0	0	1	0	0

Table 8—6. CA Commands (Part 2 of 3)

Command	Hex	Bits							
		0	1	2	3	4	5	6	7
Set busy	1F	0	0	0	1	1	1	1	1
LA clear	0F	0	0	0	0	1	1	1	1
Enable data set ready monitor	17	0	0	0	1	0	1	1	1
Set full duplex	1B	0	0	0	1	1	0	1	1
Load control bytes:									
Byte 1, 2, 3, 4	15	0	0	0	1	0	1	0	1
Byte 2, 3, 4	55	0	1	0	1	0	1	0	1
Byte 3, 4	95	1	0	0	1	0	1	0	1
Byte 4	D5	1	1	0	1	0	1	0	1
Load control character detect table:									
Table 1	19	0	0	0	1	1	0	0	1
Table 2	59	0	1	0	1	1	0	0	1
Table 3	99	1	0	0	1	1	0	0	1
Table 4	D9	1	1	0	1	1	0	0	1
Load control interpretation table:									
Table 1	1D	0	0	0	1	1	1	0	1
Table 2	5D	0	0	0	1	1	1	0	1
Table 3	9D	1	0	0	1	1	1	0	1
Table 4	DD	1	1	0	1	1	1	0	1
LA test (diagnostic)	0B	0	0	0	0	1	0	1	1
Modem test (diagnostic)	07	0	0	0	0	0	1	1	1
Read port control word (diagnostic)	16	0	0	0	1	0	1	0	0
Read control character detect table:									
Table 1	1A	0	0	0	1	1	0	1	0
Table 2	5A	0	1	0	1	1	0	1	0
Table 3	9A	1	0	0	1	1	0	1	0
Table 4	DA	1	1	0	1	1	0	1	0

Table 8—6. CA Commands (Part 3 of 3)

Command	Hex	Bits							
		0	1	2	3	4	5	6	7
Read control interpretation table:									
Table 1	1E	0	0	0	1	1	1	1	0
Table 2	5E	0	1	0	1	1	1	1	0
Table 3	9E	1	0	0	1	1	1	1	0
Table 4	DE	1	1	1	0	1	1	1	0

8.3.1.1. No-Op

The no-op command causes no operation to occur in the CA. Sense bytes are not cleared. If a deferred unit-check status condition (8.3.2) exists, a status request is generated.

Command hexadecimal codes also interpreted as no-op commands are:

40, 80, CO, 4E, 8E, CE, 12, 52, 92, and D2.

8.3.1.2. Enable Data Output

This command initiates the output data sequence. The command turns on the data-terminal-ready and request-to-send sequences. This command terminates the command functions (hexadecimal):

11, 0D, 09, 02 (half duplex), 06, 03, 0F, 13, and 1F.

8.3.1.3. Enable Data Output With Automatic Turnaround

This command performs the same functions as the enable-data-output command, and also clears the request-to-send sequence and switches the port automatically from output to input mode upon detection of the message-end bit.

When using BSC line discipline or when the message is followed by a CRC character, the CRC or LRC is followed by a PAD character before the automatic turnaround is initiated and message-end status is reported.

Software issues an enable-data-input command (8.3.1.8) in response to device-end status presented after automatic turnaround. This restores the port to an active state.

During the time between an output end-of-message status and the enable-data-input command, the port is in idle state and an overrun or input data error may occur. This status is reported at the end of the next message after the port is placed in active state.

8.3.1.4. Dial

The dial command turns on the CALL REQUEST signal to the ACU each time ACU raises the PRESENT NEXT DIGIT signal, it causes the CA to request output data that is treated as a dial digit. No CCD table access is made for dial digits.

An enable-data-output, enable-data-input, or turn-off command must be sent to the associated data set LA before data-set status or abandon-call-and-retry request is returned from the ACU. Failure to do this results in disconnection of the dialed call.

The dial command is terminated by the LA-clear command (8.3.1.16).

8.3.1.5. Send Space

This command causes the LA to send a continuous spacing signal until the command is terminated by any of the following hexadecimal command codes:

01, 0D, 09, 02, 03, 0F, or 13.

A timed spacing signal is normally used to stop a remote transmitter (break) or disconnect a remote terminal equipped with a modem recognizing the long spacing signal (disconnect). Recommended time for a break signal is 600 msec, and for a disconnect, 2 seconds. However, specific terminal and modem requirements may vary from these time values.

8.3.1.6. Send Mark

The send-mark command causes the LA to send a continuous MARK signal until terminated by any of the following hexadecimal command codes:

01, 11, 09, 02, 03, 0F, or 13.

The send-mark command precludes data and status transfers for the addressed port; therefore, it cannot be used in conjunction with the CA internal hardware timers.

8.3.1.7. Send Idle

The send-idle command causes continuous transmission of the SYN character if transmission is synchronous, or continuous MARK signal if asynchronous, until terminated. The command is terminated by program time-out and any of the following hexadecimal command codes:

01, 11, 0D, 02, 03, 0F, or 13.

8.3.1.8. Enable Data Input

This command starts an input data sequence when input data is available. The command turns on the DATA TERMINAL READY signal and sets the LA to input mode. If synchronous mode (control byte 4) is used and the port is not yet set to input because of a previous enable-data-input command, the look-for-sync function is initiated. This command terminates the following command functions:

01 (half duplex only), 11, 0D, 09, 03, 0F, 13, and 1F.

8.3.1.9. New Sync

The new-sync command is used to quench the receive clock of a synchronous modem, and causes fast resynchronization with a newly turned-on remote transmitter. This command is normally used for multiple-parity connections. The command is self-terminating.

8.3.1.10. Look for Sync

This command nullifies character synchronization and sets the addressed port to an inactive state so that data transfers are halted, and it begins searching for two contiguous sync characters.

The command must be followed by an enable-data-input command (for a half-duplex port) or a disconnect command (for a full-duplex port) to proceed with input data. Input data flow to the processor ceases until resynchronization is achieved; then the CA automatically reverts to normal data input.

Normally, this command is needed only during recovery procedures because character synchronization occurs automatically upon acceptance of an enable-data-input command (if the port is turned off or set to output), and after detection of an input ending character.

If this command is sent to a port engaged in output, it will place the port in an inactive state and cause a spacing signal to be sent.

8.3.1.11. Turn-Off

The turn-off command causes termination of an output data sequence after any pending data request is serviced. The data-terminal-ready function is not turned off; but if it is off, it will be turned on. A request to send is also turned off.

This command terminates the following command functions:

01, 11, 09, 06, 13, and 1F.

8.3.1.12. Clear Active

This command sets the addressed port to an inactive state so that input or output data transfers are halted. No LA/modem interface signals are affected by this command, and the sense bytes are not cleared. This command is accepted even if the CA has an input or output data request pending from the CMM.

8.3.1.13. Disconnect

The disconnect command terminates a call. The DATA TERMINAL READY and REQUEST TO SEND signals are turned off.

8.3.1.14. Sense

The sense command detects an unusual condition in the CA. The CA then sends a unit-check status byte, and the processor replies with a sense command requiring the CA to return two sense bytes (assuming a byte count of 2).

It should be noted that command code 44 causes sense byte 1 to be transferred, and command code 84 causes an all-zero byte to be transferred to the IPC first. Command code C4 causes the port control word to be transferred to the IPC until the byte count goes to zero. Also, if command code 04 is received, the command toggles down to 44 after the first byte is transferred, to an 84 after the second byte to a C4 after the third byte, then remains at C4 until the LAST BYTE signal is received from the IPC. Transfer of the port control word may start at any byte position within the word.

The C4 command is not rejected if the byte counter is busy, and it resets the counter to a not-busy state upon command termination.

The following commands may be useful for diagnostics:

44, 84, and C4.

8.3.1.15. Set Busy

This command causes a data set equipped with a suitable interface lead to appear busy to incoming dialed calls, but does not set the port to an inactive state. The command is terminated by any at the following command codes:

01, 11, 0D, 09, 02, 03, 0B, 0F, 17, or 1B.

8.3.1.16. LA Clear

The LA-clear command switches the LA back to normal operation after an LA test or modem test operation. The command sets the LA to half-duplex mode, and new incoming calls can be recognized.

This command clears the status and sense bits associated with the addressed port, including the automatic adapter port. The command clears the CALL REQUEST signal if sent to a dial adapter, and places the dial adapter in an inactive state.

8.3.1.17. Enable Data Set Ready Monitor

This command causes the data-set-read monitor in the LA to be enabled. The command need only be issued after a data-set-ready condition (sense byte 1, bit 6) has been detected so that the monitor is again in effect.

8.3.1.18. Set Full Duplex

This command is used to set an LA into full-duplex mode. All CAs are set to half-duplex mode by the MASTER CLEAR signal.

8.3.1.19. Load Control Bytes

This command transfers to the CA all control bytes listed in Table 8—8 (8.3.3), and is terminated by the LAST BYTE signal from the IPC.

Any combination of control bytes can be loaded by varying the byte count and command code. For example, use command code 95 and a byte count of 1 to load control byte 3. A byte count of 2 loads control bytes 3 and 4. Loading port control byte 1 with zeros in the lower half of the byte is the same as issuing an LA-clear command (8.3.1.16).

If the byte count is greater than the value required to load control byte 4, this command degenerates into a sense command for the remainder of the byte count.

8.3.1.20. Load Control Character Detect Table

This command transfers to the CA the specific control codes to be placed in a control character detect table.

Each active port in the CA, except ports used for dialing, references one of four tables in the CA for detection of control characters. The table to be used by a specific port is specified by bits 0 and 1 of control byte 2 (Table 8—8, 8.3.3). The tables are loaded at system initialization time with a load-control-character-detect-table command. Up to 256 five-bit control codes are loaded into each table with each command. The tables are cleared to all zeros when system power is turned on (master clear).

A pseudo-device (port) address must accompany this command. The addressed port is issued an LA-clear command by the CA before transfer of table data.

8.3.1.21. Load Control Interpretation Table

This command transfers to the CA specific control interpretation codes to be placed in a control interpretation table.

There are four of these tables located in the CA. The table used by a port is specified by bits 0 and 1 of control byte 3 (Table 8—8, 8.3.3). There are 16 twelve-bit words in each table, each bit position producing a single function. When a word is accessed, multiple functions (whose corresponding bits are set to 1) may be initiated. The tables are not cleared when system power is turned on, nor by master clear function.

8.3.1.22. LA Test

This diagnostic command terminates the connection between the LA and data set or communications line. The command causes the output signal to be looped back to the input for testing by the processor.

This command requires two CMM ports and sets the LA to full-duplex mode. Upon completion of the test, an LA-clear command must be issued to reset the LA.

8.3.1.23. Modem Test

This diagnostic command causes the U.S.A. wideband LA feature to exercise a local test on the associated modem. The command places the modem in a loopback test mode for testing all local (onsite) hardware, including the modems (provided modems have turnaround capabilities).

The command requires two CMM ports and it sets the LA to full-duplex mode. Upon completion of the test, the LA-clear command must be issued to reset the LA.

8.3.1.24. Read Port Control Word

This diagnostic command causes the CA to transfer the control word associated with the addressed port (device address) to the processor.

When the command is issued, the 24 bytes of the port control word are read in the following order:

Byte	Contents
1	EDC counter/output flag assembly/disassembly bits 10, 09, and 00
2	Assembly/disassembly bits 08—01
3	Storage bits 07—00
4	Break timer bits 07—00
5	Same as byte 3
6	Request byte bits 07—00
7	Same as byte 6
8	Write enables
9	Timer bits 03—00/flag bits 02—00, and DLE flag
10	CRC/LRC; after device-end status, all 0's are returned if no error was detected.
11	Control byte 2
12	Sense byte 0
13	Same as byte 11
14	Control byte 1
15	Same as byte 14
16	Write enables
17	Message control flag D—A/line on, async counter, port select inhibit 01, 00 flags
18	CRC/async counter
19	Control byte 3
20	Sense byte 1
21	Same as byte 19
22	Control byte 4
23	Same as byte 22

Byte	Contents
24	Write enables
25—32	All zero bytes

The command then returns to byte 1 and is terminated upon receipt of the LAST BYTE signal from the IPC.

8.3.1.25. Read Control Character Detect Table

This diagnostic command causes the CA to transfer control codes residing in the control character detect table to the processor. Read out begins with the code at address 00 and progresses to address FF. Up to 256 bytes are transferred. A port address must be specified with this command. The addressed port is issued on LA-clear command by the CA before transfer of table data.

The command is terminated by receipt of the LAST BYTE signal from the IPC.

8.3.1.26. Read Control Interpretation Table

This diagnostic command causes the CA to transfer codes residing in the control interpretation table to the processor. Conditions for use and clearing are the same as for the read-control-character-detected-table command (8.3.1.25).

8.3.2. Command Processing

The start input/output (SIO) instruction sequence initiates processing commands received by the CA from the IPC (Figure 8—3). After the SIO instruction sequence is complete, the IPC sets a condition code to indicate what action the ICA has taken in response to a command code. The actions and condition codes are as follows:

Condition Code	CA Action
00_2	Command accepted by CA
01_2	Command rejected by CA
10_2	CA busy
11_2	CA not available because in offline condition

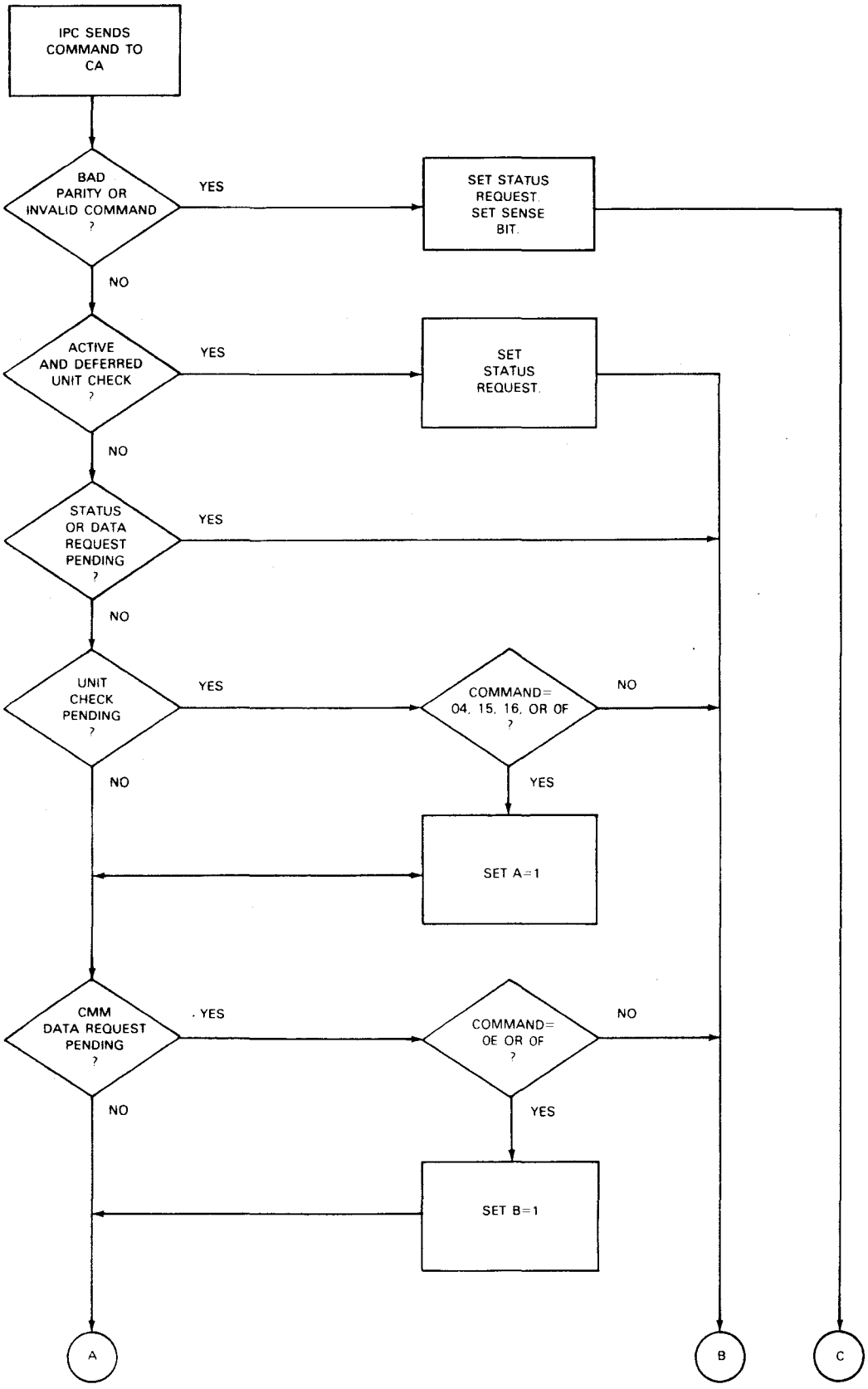
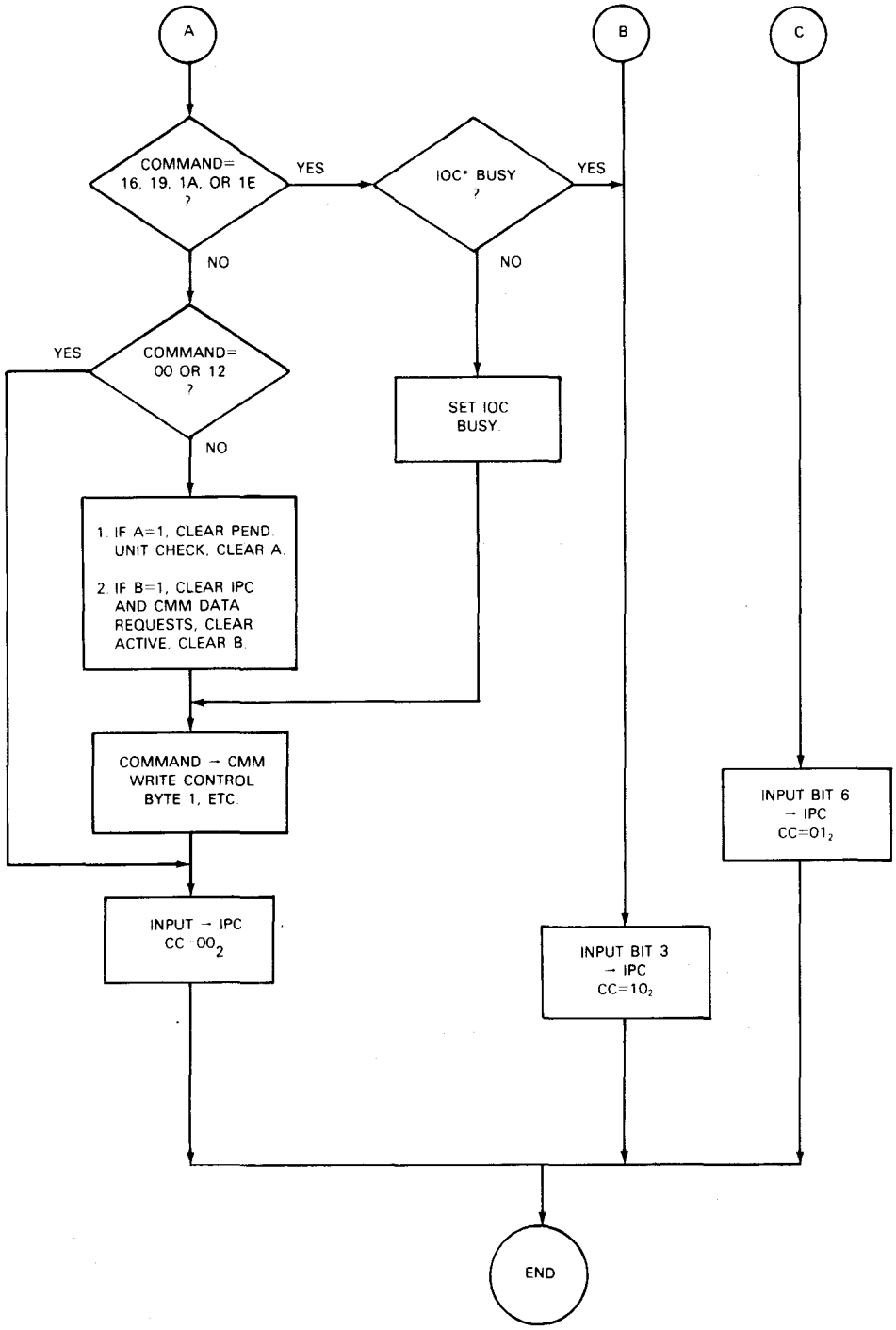


Figure 8–3. CA Operation During SIO Sequence (Part 1 of 2)



*IOC is common to all ports. Other conditions refer to addressed port only.

Figure 8—3. CA Operation During SIO Sequence (Part 2 of 2)

8.3.2.1. Command-Rejected Condition Code

When the IPC sets condition code to 01_2, it indicates the CA has rejected the command because of incorrect parity in the command code, an invalid CA command code was used, or because the addressed port has no LA attached.

A status byte with unit-check status and a sense byte with the command reject bit set are presented to the IPC for an invalid command code or for a missing LA. Unit-check and bus-out-check bits are set if parity is incorrect in the command code.

A few early processors allow commands to be accepted by ports not having LAs attached. However, no input or output data transfers can occur with this condition, and software is designed to detect the condition by time-out, loopback test, or similar methods.

Invalid CA commands are listed in Table 8—7.

Table 8—7. Invalid CA Commands

Command Bits							
7	6	5	4	3	2	1	0
X	X	X	X	1	0	0	0
X	X	X	X	1	1	0	0
X	X	X	1	0	0	0	0
X	X	X	1	0	1	0	0
X	X	1	X	X	X	X	X

LEGEND:

X = don't care bit

8.3.2.2. Busy Condition Code

The busy condition code does not cause a status request by itself. A sequence of events following the busy condition code are required for a status request. Any of the following conditions that exist at the time of an SIO sequence will cause a busy condition code:

- The previous command to the addressed port has not been sent to the LA, because CMM port scan delays (approximately 15 microseconds) or modem interface time delays (51 to 68) microseconds after request-to-send or data-terminal-ready events are turned off) are occuring when the commands are not accepted.

  Certain commands (00, 40, 80, C0, 12, 52, 92, D2, 0E, 4E, 8E, and CE) are accepted even though the busy condition exists due to scan delays. Other commands (04, 44, 84, C4, 15, 55, 95, D5, 16, 56, 96, D6, 0F, 4F, 8F, and CF) are always accepted. Commands 0D, 0F, 19, 1A, 1D, 1E, and 1F will stop the modem interface time delay.

- The addressed CA port is actively passing data, and a deferred unit-check bit (e.g., VRC error or overrun condition) exists. Data flow is automatically stopped (command termination), and a status request is initiated.

- A status request or IPC/CA interface data request is pending.
- An outstanding unit-check status exists for which no sense command has been received. Exceptions are the LA-clear (0F), sense (04, 44, 84, or C4), load-control-bytes (15, 55, 95, and D5), and read-port-control-word (16) commands. These four commands clear the outstanding unit-check conditions, set the 00_2 condition code, and perform command functions in the normal manner.
- A CMM data request (message data) is pending. Exceptions are the clear-active (0E) and LA-clear (0F) commands, which perform functions in the normal manner.
- Certain commands (16, 19, 59, 99, D9, 1A, 5A, 9A, DA, 1D, 5D, 9D, DD, 1E, SE, 9E, and DE) use a common byte counter in the CA. If the counter is already in use, the commands are not accepted.

8.3.3. Command Termination

After a command is accepted, and depending on which command is accepted, status may or may not be returned upon command termination. Table 8—8 lists the command termination condition for each of six groups of commands.

Table 8—8. Command Termination Conditions (Part 1 of 2)

Command Group	Termination Condition
SIO commands requiring no data transfers: 03, 06, 07, 0A, 0B, 0D, 0E, 0F, 11,17,1B, and 1F.	These commands are performed upon being accepted, and no status is returned. Commands 09 and 13 also fall in this category except that send-idle (09) causes one data request to be made if the port is in an offline state before the command, and disconnect (13) may be issued to the input port of a full duplex pair to enable data input.
No-op commands: 00, 40, 80, C0, 4E, 8E, CE, 12, 52, 92, and D2.	The no-op commands do not return status.
Normal data SIO commands: 01, 02, and 05	These commands require data transfer from/to the processor. An end-condition of some type must be recognized by the CA before status is returned. This could be a recognized end-of-message character, line procedure time-out, or an abandon-call-and-retry from a dial adapter. If the buffer count goes to zero (last byte) or a TERMINATE signal occurs from the IPC before detection of one of the above conditions, the CA inhibits further data transfers from that port until a new SIO is received. Device-end status is returned. If an IPC bus parity error occurs, the CA inhibits further data transfers to the address port, reports unit-check status, and sets the bus-out-check sense bit. After receipt of the sense command, a new SIO command must be received by the CA to restart data transfer.
Sense command: 04	Causes data requests to continue until the buffer count goes to 0 (last byte). Only the first two bytes are sense information. Normally, the programmer should set up a 2-character buffer. Device-end status is returned after the last byte or TERMINATE signal is received from the IPC.
Read-port-control-word command: 16	Causes the 24-byte port control word or any portion of it (depending on the byte count) to be transferred to the IPC. The command terminates when the last byte or TERMINATE signal is received by the IPC. Device-end status is returned. This command is used for diagnostics only.

Table 8—8. Command Termination Conditions (Part 2 of 2)

Command Group	Termination Condition
Load and read table commands: 19, 59, 99, D9, 1A, 5A, 9A, DA, 1D, 5D, 9D, DD, 1E, 5E, 9E, and DE.	These commands use a port address during data transfers. When the SIO is accepted, the port is placed in a cleared state. Data requests are generated until the buffer count goes to zero. Following a last byte or TERMINATE signal from the IPC, device-end status is returned. If an IPC bus parity error occurs, the CA inhibits further data transfers, reports unit-check status, and sets the bus-out-check sense bit. After receipt of the sense command, a new SIO command must be received by the CA to restart data transfer. A new load/read table command causes the CA to begin loading or reading the specified table at address 00.
Load control byte commands: 15, 55, 95, D5	Cause data requests to be generated that continue until the buffer goes to zero. Only the first four requests cause control bytes to be loaded. Normally, a 4-character buffer (or less) should be set up by the programmer. The command terminates by receipt of the last byte or TERMINATE signal. The CA returns device-end status. If an IPC bus parity occurs, the CA inhibits any further data transfers, reports unit-check status, and sets the bus-out-check sense bit. After the sense command is received, a new SIO command must be received by the CA to restart data transfer.

8.3.4. Control Bytes

The four load control bytes listed in Table 8—8 are transferred to the CA with a load control byte command. Each active port in the CA requires a set of four control bytes that are loaded at system initialization time or as required for diagnostics and timers.

The four control bytes are cleared to all 0's by the MASTER CLEAR signal. The control bytes should be loaded with 0's, except that bit 6 of byte 4 must equal 1 when a dial adapter is connected to a port. Table 8—9 lists the four control byte formats and bit functions.

8.3.5. Line Procedure Timer

The line procedure timer provides software with the means of timing intervals for line control or device control. A timer is stopped or started by loading control byte 4 (Table 8—9) and controlling the active state of the port. Bit 7 of control byte 4 selects the proper timing range (Tables 8—10 and 8—11).

The timer is started when bits 0 through 3 of control byte 4 are loaded with a binary number equal to or greater than 0010, and the port is in an active state. The timer is stopped by setting bits 0 through 3 to 0000, or by placing the port in an inactive state (clear-active command, 8.3.1.12).

The timer is reset to its initial timing value and continues timing in any of the following circumstances:

- Receipt of a start character
- Receipt of an end character (including ITB)
- Receipt of any character in asynchronous mode
- When the timer expires

Table 8—9. Control Byte Formats (Part 1 of 4)

Byte 1

0 1	2 3	4 7
Characteristics	**Modifiers**	**Command Functions**

Characteristics – 0-1 synchronous:

0 Input (specific start characters)

1 Input (any non-SYN start)

0 Output (2 pads + 2 SYNs). This preamble precedes the first message after enabling data output. If contiguous output messages are sent (e.g., on a full duplex-output port), the preamble preceding the second and following messages are as follows:

Parity Function	4 SYN Option	2 Pad – 2 SYN Option
0 through A	PSSS	PPSS
B through F	PSSSS	PSPSS

1 Output (4 SYNs)

Characteristics – 0-1 asynchronous:

00 Not used

01 Output (1 stop element)

10 Output (1.5 stop elements)

11 Output (2 stop elements)

Modifiers – 2-3:

Bits 2 and 3 must be 0; these positions are used internal to CA.

Command Functions – 4-7:

Bits 4 through 7 must be 0; these positions are used internal to CA.

Byte 2

0 1	2 3	4 7
Control Detect Table Select	**Character Length**	**Asynchronous Line Speed**

Control Detect Table Select – 0-1:

Bit 0	Bit 1	Control Detect Table
0	0	Table 1
0	1	Table 2
1	0	Table 3
1	1	Table 4

Table 8—9. Control Byte Formats (Part 2 of 4)

Byte 2 (cont)

Character Length – 2-3:

Bit 2	Bit 3	Character Length
0	0	5 bits per character
0	1	6 bits per character
1	0	7 bits per character
1	1	8 bits per character

Asynchronous Line Speed – 4-7:

Bit 4	Bit 5	Bit 6	Bit 7	Asynchronous Speed (bps)
0	0	0	0	45.45
0	0	0	1	50
0	0	1	0	56.8
0	0	1	1	74.2
0	1	0	0	75
0	1	0	1	100
0	1	1	0	110
0	1	1	1	134.5
1	0	0	0	150
1	0	0	1	200
1	0	1	0	300
1	0	1	1	600
1	1	0	0	1050
1	1	0	1	1200
1	1	1	0	1800
1	1	1	1	2400

Byte 3

0 – 1	2	3	4 – 7
Control Interpretation Table Select	Not Used	Include/Exclude Start Character	Parity Functions

Control Interpretation Table Select – 0-1:

Bit 0	Bit 1	Control Interpretation Table
0	0	Table 1
0	1	Table 2
1	0	Table 3
1	1	Table 4

Include/Exclude Start Character – 3:

Bit 3 = 0 Start character is not included in the BCC. (Bit 8 of CI table set to 1 also excludes start character from BCC.)

Bit 3 = 1 Start character is included in BCC (unless CI bit 8 equals 1 for the start character).

Table 8–9. Control Byte Formats (Part 3 of 4)

Byte 3 (cont)

Parity Functions – 4-7:

Bit				Parity Functions					
4	5	6	7	VRC	Control Character	LRC	LRC Character Parity	CRC①	Application
0	0	0	0						No parity check
0	0	0	1	Odd	Even				CTMC/DCS compatible
0	0	1	0	Odd	Even				CTMC/DCS compatible
0	0	1	1	Even	Even				CTMC/DCS compatible
0	1	0	0	Even	Odd				CTMC/DCS compatible
0	1	0	1	Even	Even	Even	Even		Async std*
0	1	1	0						Spare
0	1	1	1						Spare
1	0	0	0②	Odd	Even	Even	Even		1004 (DLT-1/3)
1	0	0	1	Odd	Odd	Even	Odd		Sync std*
1	0	1	0	Odd	Odd	Even	Even		U–300
1	0	1	1	Odd	Odd	Even	Odd		BSC-ASCII nontransparent
1	1	0	0③	Odd	Odd			#1	BSC-ASCII transparent
1	1	0	1					#1, 4④	BSC-EBCDIC or 6-bit code
1	1	1	0					#2	CCITT
1	1	1	1					#3	Selectable CRC

NOTES:

① CRC #1 $X^{16} + X^{15} + X^2 + 1$ (CRC–16)

#2 $X^{16} + X^{12} + X^5 + 1$ (CCITT)

#3 16-bit strap selected (RPQ)

#4 $X^{12} + X^{11} + X^3 + X^2 + X + 1$ (CRC–12)

② Parity option 8 is intended specifically for use with the 1004 and NTR procedures that utilize a mixture of odd and even character parity. Use of this parity option for other procedures should not be attempted.

③ A 7-bit character size must be specified when parity function 1100^2 is used. A 6- or 8-bit character size must be specified when parity function 1101^2 is used. An 8-bit character size must be specified when parity function 1110^2 is used.

④ Use of CRC #1 or #4 is determined by character length set in port control byte 2.

*American National Standard Institute

Table 8—9. Control Byte Formats (Part 4 of 4)

Byte 4

0 — 3	4	5	6	7
Timer Value	**SYN/ASYN**	**D/T SELECT**	**SYN/ASYN**	**Timer Range**

Timer Value – 0–3:

Bits 0	1	2	3	Diagnostic Control	Timer Value
0	0	0	0	Normal asynchronous back-back (do not use)	Refer to 8.3.5.
0	0	0	1	↓	↓
.	.	.	.		
.	.	.	.		
1	1	1	1		

SYN/ASYN – 4, 6:

Bits 4	6	SYN/ASYN Function
0	0	Asynchronous transmission is specified.
0	1	Synchronous transmission is specified.
1	0	Synchronous LA with synchronous control byte parameters. Used with IBM equipment having capability of 2400 bps.
1	1	Reserved for future use.

D/T Select – 5:

Bit 5=0 Bits 0–3 specify line procedure timer value (8.3.5).

Bit 5=1 Internal diagnostic control. Bits 0–3 must be set to 0000 (asynchronous use only).

Timer Range – 7:

Bit 7=0 High timer range (Table 8–11)

Bit 7=1 Low timer range (Table 8–10)

The line procedure timer is useful in operations on a switched network by facilitating disconnection in event of a wrong number or other connection not resulting in data transfer. It also facilitates disconnection when data transmission stops because DLE EOT was not recognized, or because of problems with a remote terminal or communications network.

The timer may be used to time the sending of break signals or other similar devices by its ability to restart upon detection of synchronizing sequences. It is also useful in BSC to time the 3-second receive interval required for these sequences.

Timer discipline is dependent and is usually defined in documentation specified by protocol.

Table 8–10. Low Timer Range

Control Byte 4, Bits				Elapsed Time (seconds)	
0	1	2	3	Maximum	Minimum
0	0	0	0	Timer stopped	
0	0	0	1	Timer stopped	
0	0	1	0	0.142	0.071
0	0	1	1	0.213	0.142
0	1	0	0	0.284	0.213
0	1	0	1	0.355	0.284
0	1	1	0	0.426	0.355
0	1	1	1	0.710	0.426
1	0	0	0	0.994	0.710
1	0	0	1	1.278	0.994
1	0	1	0	1.562	1.278
1	0	1	1	1.846	1.562
1	1	0	0	2.130	1.846
1	1	0	1	2.414	2.130
1	1	1	0	2.698	2.414
1	1	1	1	3.834	2.698

NOTE:

Control byte 4, bit 7=1 for this timer range only. The timer resets when a SYN character is sent or received, in addition to the reset conditions described in 8.3.5.

Table 8–11. High Timer Range

Control Byte 4, Bit				Elapsed Time (seconds)	
0	1	2	3	Maximum	Minimum
0	0	0	0	Timer stopped	
0	0	0	1	Timer stopped	
0	0	1	0	4.544	2.272
0	0	1	1	6.816	4.544
0	1	0	0	9.088	6.816
0	1	0	1	11.360	9.088
0	1	1	0	13.632	11.360
0	1	1	1	15.904	13.632
1	0	0	0	18.176	15.904
1	0	0	1	20.448	18.176
1	0	1	0	22.720	20.448
1	0	1	1	24.992	22.720
1	1	0	0	27.264	24.992
1	1	0	1	29.536	27.264
1	1	1	0	31.808	29.536
1	1	1	1	34.080	31.808

NOTE:

Control byte 4, bit 7=0 for this timer range only. The timer resets under same conditions for resetting low timer.

8.3.6. Status Byte

The status byte supplies to the IPC information pertaining to the state of the CA. Status is stored in the IOSTIW device status field. The status register in the CA is cleared when the IPC accepts a status byte.

A CA port exists in either the active or idle state. Status presentations to the IPC are made in accordance with the following rules under each state:

- Active state

  The following commands place the addressed CA port in active state:

  — Enable-data-output (01)

  — Enable-data-input (02)

  — Dial (0J)

  — Send-idle (09)

  — Send-space (11)

  — Disconnect (13)

  In active state the CA generates data requests as required. When the CA encounters any condition warranting status presentation, it inhibits subsequent data requests and places the port into idle state when the presentation is made. The commands: turn-off (03), LA-clear (0F), look-for-sync (06), and clear-active (0E), place the port into idle state.

- Idle state

  When a port resides in idle state, it will not generate status except for the following selected events:

  — Ring indicator/data set status

  — Break

  — Data set ready off

  — Bus-out check (SIO sequence)

  — Command reject (invalid command)

  — Disconnect

  — Open line

  — Space to mark

  Any of the above conditions causes a single unit-check status presentation to be made, and the CA sets a port flag inhibiting subsequent status requests. In addition, the flag signifies that the next command must be a sense, LA-clear, read-port-control-word, or load-control-byte command. In normal operation, the next command is a sense command causing transfer of sense bytes to the IPC. Sense bytes may contain multiple bit settings that occurred since the original unit-check presentation. The four commands just cited clear the flag that inhibits status presentations.

  If the next command after a unit-check status presentation is not a sense, LA-clear, read-port-control-word, or load-control-byte command, the command is not accepted by the CA, and the busy condition code (10_2) is set.

  If an overrun or data error occurs while the port is in idle state, the condition is flagged and status is reported after the port is returned to active state, and another status condition or SIO occurs. A master-clear or LA-clear command to the port while in idle state will clear the flag and cause the overrun or data-error status to be lost.

Status bits and their meanings are listed in Table 8—12. A summary of status conditions is shown in Figure 8—4.

Table 8—12. Status Byte

Bit	Designation	Interpretation
0—4	—	Set to zero by the CA.
5	Device end	Completion of a previously initiated command. Successful completion is indicated if device-end status is presented without unit-check status.
6	Unit check	An unusual condition has occurred, and at least one sense bit has been set.
7	—	Set to 0 by the CA.

8.3.7. Sense Bytes

Sense bytes are cleared upon acceptance of any command except sense, read-port-control-word, load-control-bytes, clear-active, or no-op. The master clear command also clears the sense bytes.

The sense bits for each sense byte are listed in Table 8—13, together with the conditions that set the bits. Also, see Figure 8—4 for a summary of sense bits.

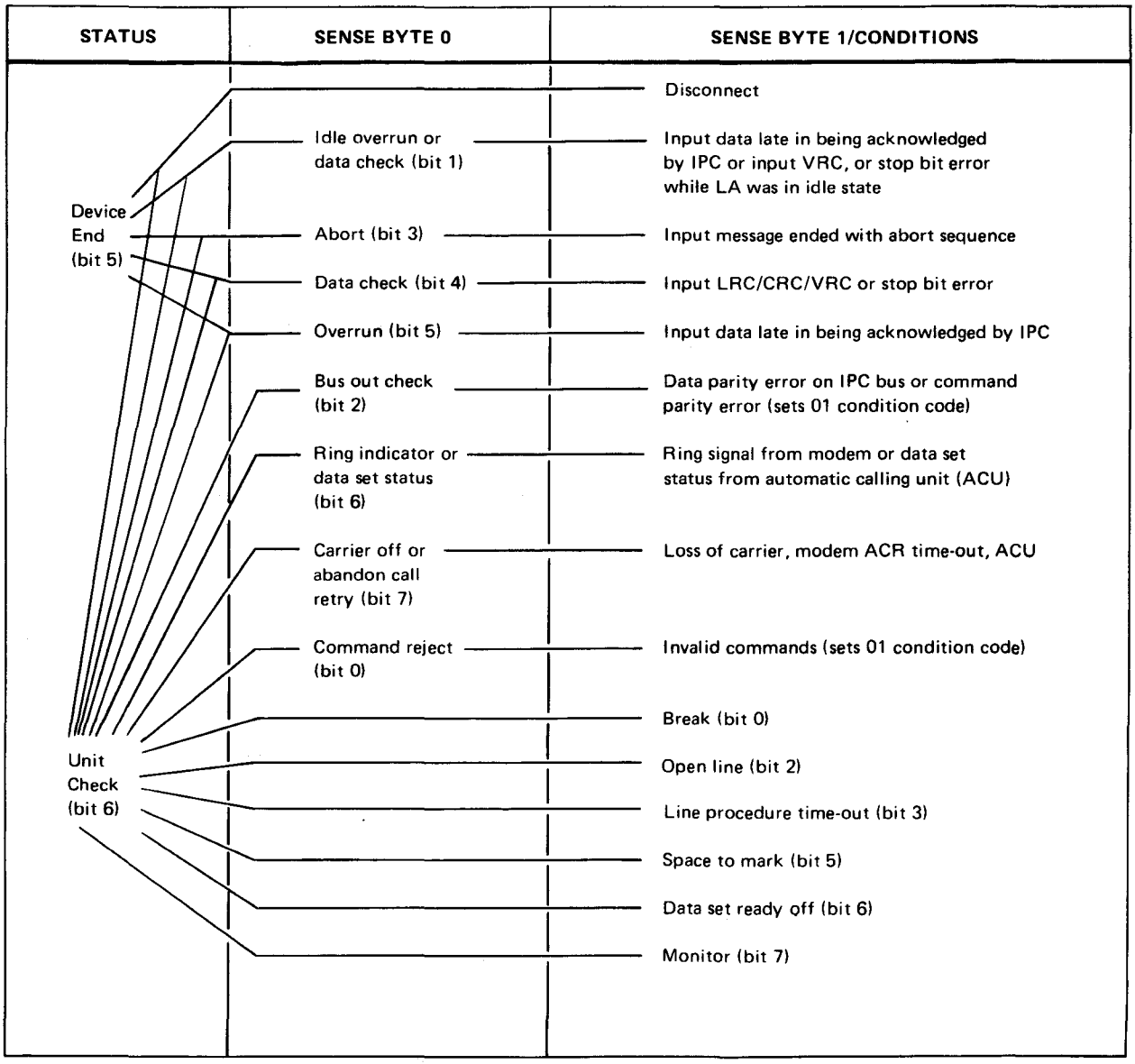


Figure 8—4. Summary of Status and Sense Conditions

Table 8—13. Sense Bytes (Part 1 of 2)

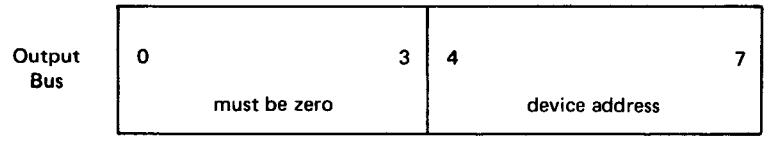
Bit	Designation	Interpretation
		Sense Byte 0
0	Command reject	A valid command was presented to the CA. Condition code 01_2 is set.
1	Idle overrun or idle check	An input data overrun or an input data error occurred while the port was in an inactive state. This bit is set if a break, disconnect, or open line condition occurs while the port is inactive.
2	Bus out check	a. A parity error was detected on a command code. Unit-check bit is set. Condition code 01_2 is set; or b. A data parity error on data was received from the IPC. Output data transfer on the affected port is halted immediately on detection of the error. The CA time fills in with SYNs (nontransparent synchronous), or marking (asynchronous) until a new command is received.
3	Abort	An input message ended with an abort sequence (a character with CI bit 5=1, preceded by a start character). Unit-check bit and device-end bit are set.
4	Data check	An input LRC/CRC error, character parity error, or a missing stop bit error (asynchronous) has occurred on an input block, message, or supervisory sequence. Unit-check bit and device-end bit are set upon termination. Data-check bit is set for break, disconnect, or open line conditions if the port is active.
5	Overrun	Input data was late in being acknowledged by the IPC. Unit-check and device-end check bits are set upon termination.
6	Ring indicator or data set status	A ringing signal is being received from a modem, or a dialed connection has been successfully established by an automatic calling unit. The LA ring inhibit flip-flop must be cleared with an LA-clear command before ring status can be reported again. An enable-data-input, enable-data-output, or turn-off command should be sent to the CA in order to turn on data-terminal-ready sequence for a modem, or an LA-clear command should be sent to clear a call request to an automatic calling unit (ACU).
7	Carrier off or abandon call and retry	Loss of a carrier on a modem-equipped LA, or a connection was not established after a dial command.
		Sense Byte 1
0	Break	Reception of a spacing signal for at least 180 and less than 250 microseconds duration from a terminal. The signal is normally used to stop transmission. Break, disconnect, and open line are mutually exclusive.
1	Disconnect	The communications line has been disconnected via reception of either a DLE EOT or a space signal of at least 750 microseconds and less than 3 seconds. Unit-check and device-end bits are set. Break, disconnect, and open line are mutually exclusive.
2	Open Line	Reception of a spacing signal for at least 3 seconds, usually indicating an open telegraph line. Break, disconnect, and open line are mutually exclusive.
3	Line procedure time-out	The line procedure timer has run out.
4	–	Set to 0 by the CA.

Table 8—13. Sense Bytes (Part 2 of 2)

Bit	Designation	Interpretation
		Sense Byte 1 (cont)
5	Space to mark	Occurs when the space-to-mark transition occurs, provided the spacing exceeds 180 microseconds duration. Used primarily for flagging the end of an idle period when following European TELEX procedures. NOTE: The space-to-mark sense bit is set concurrently with the break and disconnect sense bits. The space-to-mark bit may be set at some indeterminate point in time relative to the open-line indication. Break, disconnect, and open line are mutually exclusive.
6	Data set ready off	The data-set-ready bit has turned off, but data-terminal-ready bit is still on. Software should interrogate the terminal to ensure proper terminal identity when this condition occurs. Also, an enable-DSR-monitor command or LA-clear command must be issued so that the DSR monitor is again in effect. If the DSR monitor is not in effect, no data can be transferred.
7	Monitor	A monitor character has been detected. Normally used to indicate that an illegal character was detected in an output message. Transmission is automatically stopped until a new command is received. If an error occurs on a BCC following ITB, this bit becomes set.

8.3.8. LA Device Addresses

The device address for LAs is analogous to the CMM port address. The device address received from the IPC is encoded and formatted as follows:



The LA device addresses are listed in Table 8—14.

Table 8—14. Line Adapter Device Addresses (Part 1 of 2)

LA Number	Device or Port Address (hexadecimal)
LA—0	4
LA—1	6
LA—2	8

Table 8—14. Line Adapter Device Addresses (Part 2 of 2)

LA Number	Device or Port Address (hexadecimal)
LA—3	A
LA—4	C
LA—5	E
LA—6	5
LA—7	7
LA—8	9
LA—9	B
LA—10	D
LA—11	F

8.3.9. Full-Duplex Operation

Only one pair of full-duplex lines are used in the 90/30 system. Operating an LA in full-duplex mode requires that the following rules are observed:

1. Two CMM ports are required. Full duplex port pairs are any one of the following:
   - 4 and 5
   - 6 and 7
   - 8 and 9
   - A and B
   - C and D
   - E and F
2. The output port is defined as the port coincident with the active LA (only one LA is required for FD). For example, if the LA is plugged into position LA—0, port 4 is output and port 5 is input. If the LA is plugged into position LA—6, port 5 is output and port 4 is input.
3. A set full-duplex, LA-test, or modem-test command will set the LA into full-duplex mode. If an LA is present at the associated port, a disconnect command must be sent to that LA so that the CMM port becomes available for input data from the LA coincident with the output port.
4. The LA can be set to half-duplex mode with an LA-clear command to the output port, or it is automatically set to half-duplex by the MASTER CLEAR signal. The load-CC-table, load-CI-table, read-CC-table, and read-CI-table commands also set the LA to half-duplex mode.

5. When full-duplex mode is set, data input is automatically enabled on the adjacent port. Input data is transferred to the processor using the input port buffer control words. Status associated with input is presented using the input port address. If unit-check status is presented on the input port, a sense command must be issued to the input port to determine the cause of the status.

6. A disconnect command must be issued to the input port to place it in an active state. Whenever status is presented for a data transfer, the port is placed in an idle state, and another disconnect command must be issued to return the input port to an active state.

7. For full-duplex synchronous operation, if a look-for-sync command is required, it should be issued to the input port. This places the input port in an active state and stops service requests from that port so that recovery procedures may be executed. The look-for-sync command may be followed by a disconnect command to the input port to place the port in an active state and continue data input. The look-for-sync command should not be issued to the output port, because it will terminate any output data transfer in process at that time.

8. Unless the CA is configured as a remote station on a full-duplex multipoint network, the modem or LA should be strapped for continuous carrier operation.

An example of full-duplex operation using the above rules follows:

1. Initiate full-duplex operation.

Commands		Applicable	
Output Port	Input Port	Rules	Comments
0F	0F	1, 2, 4	To clear any previous functions.
1B			
	13	3	Required to disconnect the LA connected to the input port.

2. Send output after full-duplex mode is set.

Commands to Output Port	Comments
01	
04	If unit-check status is presented on the output port.

3. Receive input after full-duplex mode is set.

Commands to Input Port	Applicable Rules	Comments
04	5	If unit-check status is presented to input port.
13	6	Required to reenable the input port.

4. Send output with memory interruption.

Commands to Output Port	Comments
01	
09	Interrupts output with idle-state fill.
01	
04	If unit-check status is presented on the output port.

8.3.10. I/O Error Detection and Recovery

The CA detects errors that occur in a communications environment external to the CA (e.g., modems and transmission lines) through use of character parity or block check character and interval timers, as applicable to the remote terminal communications discipline.

Errors occurring internal to the CA or in the communications between the CA and processor are detected through use of byte parity as follows:

- Input data transfer errors are detected by the processor.
- Output data transfer errors are detected by the CA. Output transmission is halted and the CA presents status.
- Command error is detected by the CA, which causes a command-rejected condition code to be returned to the IPC.

Logic in the CA protects against the loss of status information by inadvertent clearing when an SIO sequence is issued for two conditions:

1. If a unit-check status has been deferred (e.g., awaiting the end of a message) or if status is pending, any SIO is rejected by the CA with a condition code of 10, and status is returned.
2. If a unit-check status is pending, any further unit-check bits are stored but no status request is made. All SIOs except sense, LA-clear, load-control-bytes, and read-port-control-word are rejected with a condition code of 10.

Recovery from any error, whether in the communications environment or internal to the CA, must be accomplished by software.

9. Diskette

9.1. GENERAL

The SPERRY UNIVAC 8413 Diskette Subsystem is a microprogrammed controller with diskette drives capable of interfacing the IPC through the diskette/CA interface (D/CA) feature. The subsystem (Figure 9—1) provides I/O capability for reading and writing with flexible (floppy) diskettes used on industry compatible product lines. The subsystem can replace the card reader and card punch in a cardless version of the 90/30 processing system.

This section contains information on operating characteristics required for programming the subsystem. To program the subsystem, which is integrated in the 90/30 system, reference should also be made to available supplemental information listed in program libraries for the 90/30 system. Information on the diskette subsystem control is included in 2.4.6.

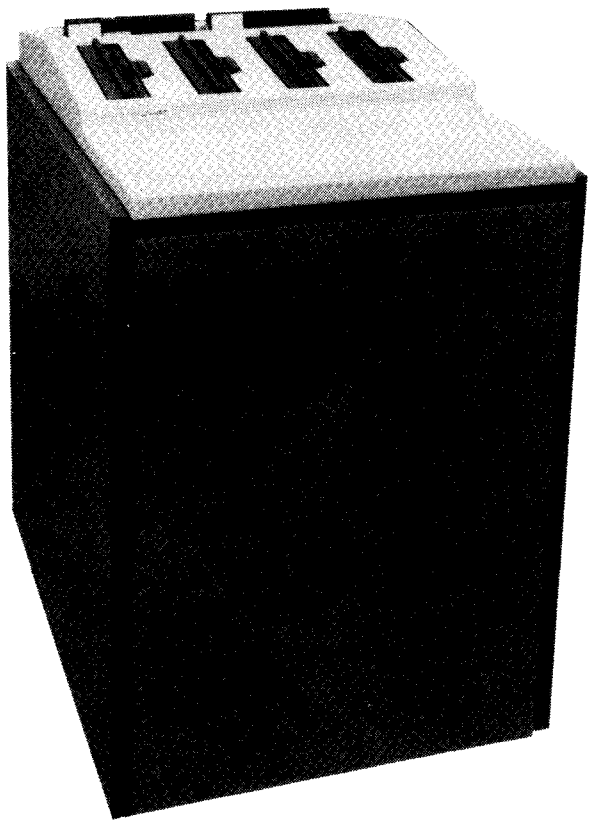


Figure 9—1. 8413 Diskette Subsystem

9.2. SUBSYSTEM DESCRIPTION

The subsystem is a buffered device that supports nonconcurrent read/write operations on all of its diskette drives. The basic subsystem has two drives; two additional drives can be added with special features. The subsystem reads at the rate of 1500 records per minute, and writes at the rate of 850 records per minute. The recording method and records format allows use with industry compatible equipment.

9.2.1. Characteristics

The subsystem characteristics are listed in Table 9—1.

Table 9—1. Diskette Subsystem Characteristics

Item	Characteristic
Read rate	1500 records per minute
Write rate	850 records per minute
Number of drives	2 standard, plus 2 with optional feature
Number of record buffers	6 buffers
Bytes per buffer	128 bytes
Diskette rotation rate	167 milliseconds per revolution
Data transfer rate	128 bytes in not less than 6 milliseconds
Diskette recording tracks	77 tracks, each having 26 sectors
Diskette recording capability	242,944 bytes
AC line voltages (nominal)	220V @ 60 Hz 220V @ 50 Hz
DC voltages	+5 V, 15 A +24 V, 1.7 A —12 V, 0.8 A
Heat dissipation	1129 Btu/hr

9.2.2. Configuration

The subsystem consists of a single unit having a flexible diskette controller (FDC), two diskette drives, and a +5 volt power supply. The diskette operates through the D/CA feature and IPC to the multiplexer channel of the processor. Figure 9—2 illustrates the functional arrangement of the subsystem and processor. The subsystem types and optional features are listed and described in Table 9—2.

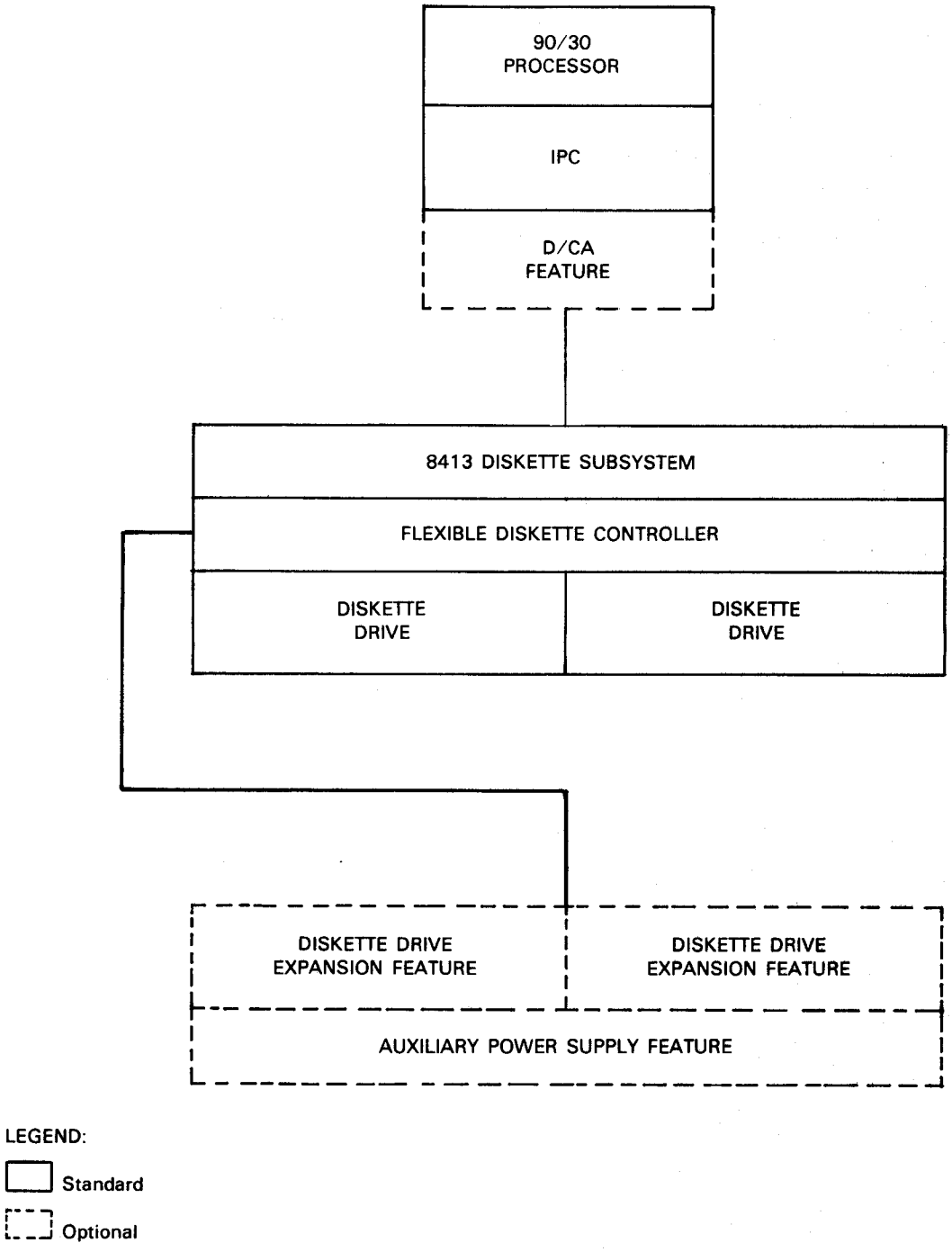


Figure 9—2. Diskette Subsystem Configuration With Optional Features

Table 9—2. Diskette Subsystem Types and Optional Features

Item	Description
8413 diskette subsystem, 60 Hz	An integrated peripheral subsystem of the 90/30 system that can replace the card punch and card reader in the system. The subsystem is basically composed of two diskette drive mechanisms, a microprocessor controller, and device and interface control logic. The diskette drives read and write at byte frequency-modulated (FM) density. The subsystem interfaces with the IPC. Operates on 220 Vac (line-to-line, single phase) at 60 Hz.
8413 diskette subsystem, 50 Hz	Same as 8413 diskette subsystem, 60 Hz, except operates on 220 Vac (line-to-neutral) at 50 Hz.
8413 diskette subsystem expansion feature, 60 Hz	Provides two additional diskette drive mechanisms for the subsystem. Reading and writing are at FM density, as on the basic subsystem. Operates on 220 Vac (line-to-line, single phase) at 60 Hz.
8413 diskette subsystem expansion feature, 50 Hz	Same as 8413 diskette subsystem expansion feature, 60 Hz, except operates on 220 Vac (single phase line-to-line) at 50 Hz.
8413 diskette subsystem power supply feature	Auxiliary power supply required on subsystem when configuration of the processor system cannot supply +5 Vdc to the subsystem. Operates on 220 Vac (line-to-line, single phase) at 60 Hz; 220 Vac (line-to-line, single phase) at 50 Hz; or 220 Vac (line-to-neutral) at 50 Hz.

9.2.3. Intelligent Operations

The subsystem has control logic (FDC) and related mechanisms (diskette drives). Control logic includes a microprocessor controller, processor-to-device interface logic, processor-to-IPC interface logic, and various data path components including buffer storage for the subsystem. The FDC controls the diskette drives, recording or retrieval of data, and detection of error conditions. Data set labels (DSL) are not generated by the FDC, however.

The FDC is microprogrammed to automatically perform certain operating sequences that do not require commands to be issued by software. When a commonly used command, such as read, is issued, the FDC initiates the sequence and the "intelligent" FDC fetches the data set label, interprets and checks the parameters, directs the data position, and performs the read operation. Some intelligent operations that the FDC is programmed to perform are listed in Table 9—3.

Table 9—3. Subsystem Intelligent Operations

Power-up diagnostics
Check data set label (DSL) parameter
Read check after write operation
Position heads according to DSL parameters
Retry positioning errors
Look ahead of read operation
Retry read errors
Perform read command sequences
Open a file on a read command
Skip deleted data sets and records
Blank sectors up to the logical record length
Validate commands according to DSL parameters
Detect an end-of-data according to DSL parameters
Skip over bad tracks

The FDC and IPC perform start input/output (SIO), data transfer, and status sequences similar to those performed by the CA (8.3.2). Data transfer sequences include the IPC byte mode (as in the CA) and word mode (as in the card punch). Word mode imposes certain restrictions on the address and count fields of the buffer control word (BCW), and is further described in 2.4.

9.2.4. Diskette Drive Mechanism

The flexible diskette drive mechanism allows direct access storage by utilizing a removable and interchangeable diskette storage medium. The diskette consists of a single flexible magnetic disk enclosed in a jacket.

A diskette drive accepts one diskette at a time. Only one side of the diskette is used to read or write. Read and write operations are performed on a single drive at a time, and not concurrently. The FDC implements time sharing when more than one diskette drive is to operate at any given time.

9.2.5. Diskette Media

The diskette contains 77 recording tracks with 26 sectors in each track (Figure 9—3). A track is a ring location on the diskette on which the read/write head is positioned during rotation of the diskette. Thus, the read/write head moves to 77 different radial positions on the diskette to reach 77 tracks. Tracks are numbered 00 through 76, with track 00 located at the outermost edge of the diskette.

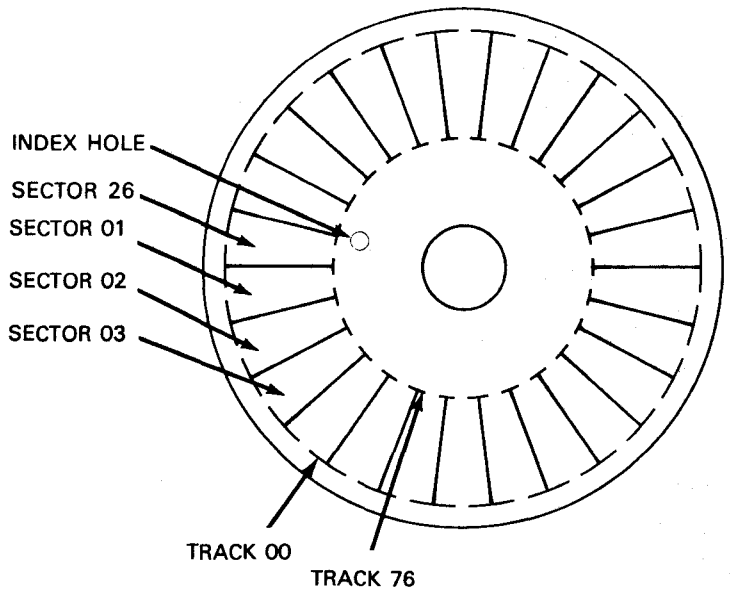


Figure 9—3. Diskette Sectors

Each track is divided into 26 evenly spaced portions called sectors. However, a sector must contain a complete record; therefore, the number of sectors on a track may vary according to the number of bytes required for the record.

The diskette uses a fixed format to form sectors electronically (Figure 9—4). Each sector contains an identification (ID) field and data field. Information on sync bytes and track or sector addresses are included in the ID field. Gaps separate the ID field from the data field and from the track index start/end point.

The format for each sector in a track may be in numerical order according to any one of 13 arrangements. The numerical order of the sectors around the track can be specified during the diskette subsystem initialization procedure. Table 9—4 lists the diskette sector sequences.

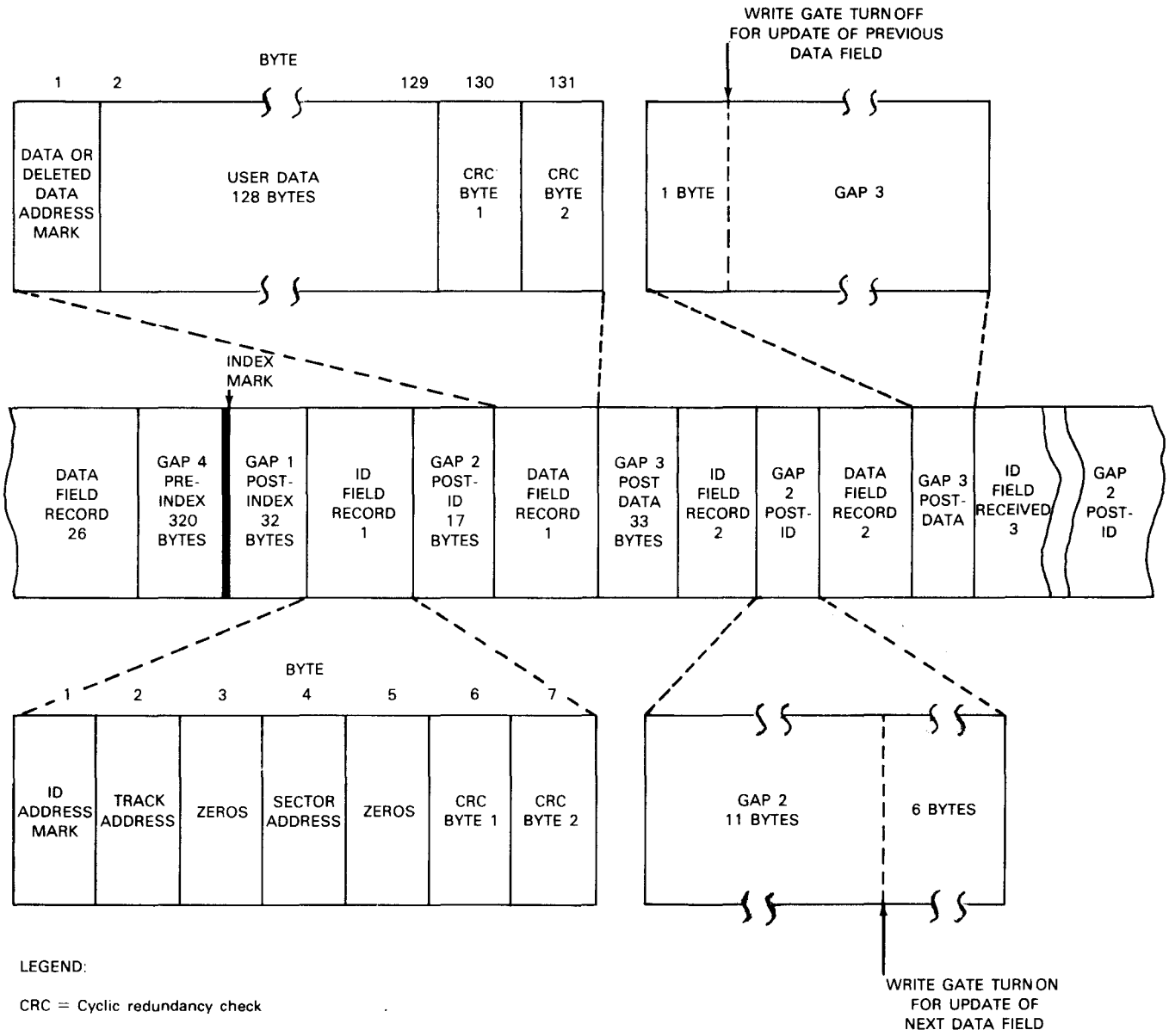


Figure 9—4. Diskette Track Format

Tracks 01 through 73 of the diskette can store up to 242,944 bytes of data. Track 74 is also a data track, but it is recommended that this track remain unused. Track 00 is the index track, which contains information on contents and volume of the diskette, and identification of the diskette's user. The index track also identifies each data set* on the diskette by including the names and addresses of data set extents (9.2.5.1). Table 9—5 lists the index track sectors and functions and the sector position in which each sector is initialized. The last two tracks (75 and 76) are replacement or alternate tracks that may be used to replace defective tracks.

The diskette is formatted in the same manner as industry-compatible diskettes for all read and write operations. However, an industry-compatible formatted diskette cannot be initialized by the FDC. Initialization can be accomplished offline by prior arrangement with the diskette supplier.

**Data set refers to a record group on the diskette; it is not to be confused with a data set or modem used in communications.*

Table 9—4. Diskette Sector Sequences

Track Physical Record Sequence	Record Number of Sector Address (Selected Sequence)											
	02	03	04	05	06	07	08	09	10	11	12	13
1	1	1	1	1	1	1	1	1	1	1	1	1
2	3	4	5	6	7	8	9	10	11	12	13	14
3	5	7	9	11	13	15	17	19	21	23	25	2
4	7	10	13	16	19	22	25	2	2	2	2	15
5	9	13	17	21	25	2	2	11	12	13	14	3
6	11	16	21	26	2	9	10	20	22	24	26	16
7	13	19	25	2	8	16	18	3	3	3	3	4
8	15	22	2	7	14	23	26	12	13	14	15	17
9	17	25	6	12	20	3	3	21	23	25	4	5
10	19	2	10	17	26	10	11	4	4	4	16	18
11	21	5	14	22	3	17	19	13	14	15	5	6
12	23	8	18	3	9	24	4	22	24	26	17	19
13	25	11	22	8	15	4	12	5	5	5	6	7
14	2	14	26	13	21	11	20	14	15	16	18	20
15	4	17	3	18	4	18	5	23	25	6	7	8
16	6	20	7	23	10	25	13	6	6	17	19	21
17	8	23	11	4	16	5	21	15	16	7	8	9
18	10	26	15	9	22	12	6	24	26	18	20	22
19	12	3	19	14	5	19	14	7	7	8	9	10
20	14	6	23	19	11	26	22	16	17	19	21	23
21	16	9	4	24	17	6	7	25	8	9	10	11
22	18	12	8	5	23	13	15	8	18	20	22	24
23	20	15	12	10	6	20	23	17	9	10	11	12
24	22	18	16	15	12	7	8	26	19	21	23	25
25	24	21	20	20	18	14	16	9	10	11	12	13
26	26	24	24	25	24	21	24	18	20	22	24	26

Table 9–5. Index Track Sectors (Part 1 of 2)

Sector	Position	Initialized (hexadecimal)	Function
1	1–80	40	Reserved
	81–128	00	Reserved
2	1–80	40	Reserved
	81–128	00	Reserved
3	1–80	40	Reserved for system scratch
	81–128	00	Reserved for system scratch
4	1–80	40	Reserved
	81–128	00	Reserved
5	1–5	Character ERMAP	ERMAP label indicates an error map record.
	6	40	Blank separator
	7, 8	40	Blank for no defective tracks; otherwise, contains first defective track number
	9	40	Blank for no defective tracks; otherwise, contains 0 for one or more defective tracks
	10	40	Blank separator
	11, 12	40	Blank for no defective tracks; otherwise, contains the number of the second defective physical track if one or more defective tracks exist
	13	40	Blank for one or no defective tracks; otherwise, contains 0 for more than one defective track
	15–22	40	Reserved
	23	40	Indicates at least one defective record exists if the position contains a D. Defective records are contained in data of any data set extent of this volume. Defective records are handled by an alternate physical record method. A blank indicates that no defective records exist.
	24	40 for 128-byte sector, C2 for 256-byte sector	This position is an error directory indicator. If blank, no specification was made on format or location for an alternate physical record location. If it contains a B, contents of the defective physical records were relocated to the ERROSET data set and recorded in the error directory in discontinuous binary format 0thr. If it contains a C, contents of the defective physical records were relocated to the ERRORSET data set and recorded in the error directory in character decimal format Δtthrr, indicating track, head, and record numbers.
	25–72	40 for 128-byte sector, 00 for 256-byte sector	These positions are the error directory containing addresses of physical records with one or more errors. Up to 12 addresses of relocated physical records can be included in discontinuous binary format (0thr), or up to 8 addresses in character decimal format (Δtthrr). The ERRORSET data set contains the relocated records in the same sequence in which addresses are located in the error directory. If sector position 24 contains a B, unused positions of this directory are filled with 0's. If position 24 contains a C, unused positions are left blank.
	78–80	40	Reserved
	81–128	00	Padded with 0's
6	1–80	40	Reserved
	81–128	00	Reserved

Table 9–5. Index Track Sectors (Part 2 of 2)

Sector	Position	Initialized (hexadecimal)	Function
7	1–4	Character VOL1	Identifies the volume label. This sector uses several fields to identify the diskette owner, the type of security, sequence of extents, and record lengths.
	5–10	Character IBMIRD	This field is the volume identifier and contains the same serial number contained on the diskette permanent label. The first character of this identification must be located in position 5 of the field, and all unused positions are left blank, with no blanks contained between characters. When initialized, the value in the field is usually part of the initialization procedure.
	11	40	This field indicates the volume's accessibility. If access to the diskette can be made, the field is blank. Further qualifications are required if a character is indicated, before access to the diskette is to be made beyond this position.
	12–37	40	Reserved
	38–51	40	Owner identification field (not used in some subsystems)
	52–71	40	Reserved
	72	40	This position is the volume surface indicator. The position should be blank to indicate that the diskette uses only one recording surface.
	73	40	This position is the extent arrangement indicator. A character P indicates that extents must be contiguous, beginning at track 1, head 0, sector 1; data set labels must begin at track 0, head 0, sector 8 and in the same sequence as the described extents. All spaces not allocated must follow the last data set of the volume, if P character is indicated; and extents in unused created space must be rearranged so that space is eliminated. A blank in position 73 indicates that extents, data set labels, or unallocated space can be arranged without specific constraints.
	74	40	This position indicates special requirements. A character R indicates some data set recordings were made that are logically nonsequential. If no special requirements are needed to access data, the position is left blank.
	75	40	Reserved
	76	40 for 128-byte sector, F1 for 256-byte sector	This position indicates the physical length of records in tracks 1 through 76. A blank in position 76 indicates 128 bytes, a 1 indicates 256 bytes, and a 2 indicates 512 bytes.
	77, 78	40	This position contains the physical record sequence code of the sector. A blank or numeric characters 1 through 13 indicate the sector physical sequence. If the sectors are physically sequential, a blank or 1 is indicated. When not used to indicate the sequence code, the field is used to increment to the next physical sector. A value can be specified as part of the initialization procedure.
	79	40	Reserved
	80	Character W	This position indicates the label statement version. When a character W is indicated, industry-compatible standard labels are used.
	81–128	00	Padded with binary 0's
8–26	–	–	These sectors permit the programmer to record data set labels reflecting the recorded data sets on tracks 1 through 74. Sectors 9 through 26 are indicated as deleted records during initialization (Table 9–6).

Records are written on and read from specified locations on the diskette identified by addresses. Determination of this location requires the track number, head number, and record number. The address format is as follows:

tthhss

where:

tt
Is the track number, which a physical record is written on or read from.

hh
Is the head number, normally indicated by 00 to indicate that only one head is used.

ss
Is the sector number, which a physical record is written on or read from.

9.2.5.1. Checking Data Set Labels

Diskettes recognized by the FDC use industry-compatible format for the data set labels. To be compatible with this format, the labels must be prepared by software so that certain fields conform with specific rules to meet the compatibility requirement (9.2.5.2). The FDC checks certain fields of the data set label to determine the extent, bypass indicator, write-protect indicator, and record length.

- Extent

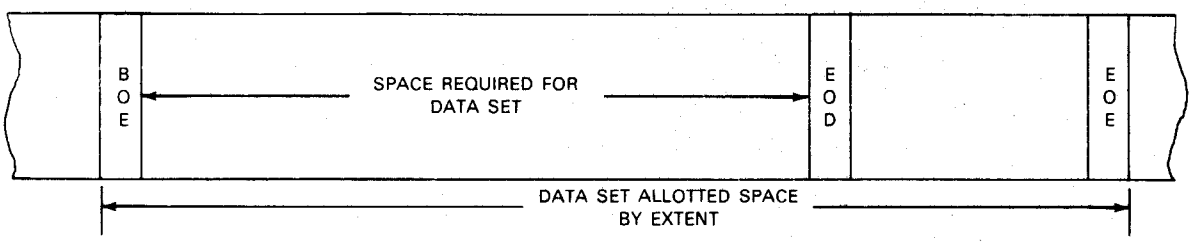
  An extent is the maximum space a data set is permitted to occupy. The beginning-of-extent (BOE) address indicates the beginning of the space the extent may occupy. The BOE restrictions are:

  1. BOE cannot be on less than track 01 and sector 01.
  2. The sector number cannot equal 00 or be greater than 26.
  3. Position 31 of the BOE must contain a 0.

  The end-of-extent (EOE) address indicates the end of the space the extent may occupy. The EOE restrictions are:

  1. EOE cannot be greater than track 74 and sector 26.
  2. The sector number cannot equal 00 or be greater than 26.
  3. Position 37 of the EOE must contain a 0.

  All the space allotted by the BOE and EOE addresses cannot be used by a data set. This requires an end-of-data (EOD) address to identify the next unused area within the extent or to indicate that data was included up to the EOE address. For example:



Restrictions on EOD are:

1. EOD cannot be greater than the EOE plus 1 or cannot be less than the BOE.
2. EOD cannot be greater than track 75 and sector 01.
3. The sector number cannot equal 00 or be greater than 26.
4. Position 77 must contain a 0.

- Bypass Indicator

  During the write, write deleted, read, and read deleted commands, if position 41 of the data set label contains a B character, the FDC sets the invalid data set label sense bit and presents device-end and unit-check status to the IPC. In this case, the data set label was to be bypassed but was referenced by the command, thus setting the sense bit. The FDC does not search for the next valid data set label. Recovery of the error is a function of software.

- Write-Protect Indicator

  Position 43 of each data set label referenced by a write or write-deleted command is checked by the FDC. If postion 43 contains a character P in EBCDIC, the FDC sets the write-protect-check sense bit and presents device-end and unit-check status to the IPC.

- Record Length

  Positions 23 through 27 of the data set label are checked for a range of 00001 to 00128 (or △△001 to △△128) by the FDC. If the checked value is not in this range, the FDC sets the invalid data set label sense bit and presents device-end and unit-check status to the IPC.

An exception found to any of the preceding fields causes the FDC to declare that a data set is invalid. These checks are a subset to checks made by industry-compatible equipment, and it is assumed that software performs the necessary checks for the following error conditions in the data set label:

1. The addressed sector is 00 or greater than 26.
2. A record length of 0 or more than 128 bytes was requested.
3. The record address has a third character that is not 0 for the BOE, EOE, or EOD.
4. A BOE address indicates less than track 01, sector 01.
5. In the header 1 field, number 1 is not indicated in position 4.
6. A request is made for an EOE address greater than track 74, sector 26.
7. The BOE address is higher than the EOE address.
8. The EOD address is higher than track 75, sector 01.
9. The EOD address is higher than the EOE plus 1 address.
10. Track 00, sectors 1 through 7, is displayed as the last record read.
11. A deleted record was requested.

All of the foregoing conditions are checked if a search, verify, enter, or update is attempted on the index track. An incorrect data set label error indication is made if any of the foregoing errors is detected.

Error conditions 1 through 4 and 6 through 9 cause an incorrect data set label error indication when header 1 record in sectors 08 through 26 is read.

All data set labels are read during execution of read and write commands. If an error occurs in the diskette during a command execution, the track zero sense bit (SB3/1) determines if the error occurred when reading the data set label or during execution of the command on related data tracks.

9.2.5.2. Deleted Data Set Labels

Deleted data set labels or any deleted records are identified by a deleted address mark that precedes the sector data field. Deleted data set labels are transferred to the IPC by the read-index-delete command, and device-end and unit-exception status are presented by the FDC. In addition, the FDC sets the deleted data set label address mark bit.

If the FDC encounters a deleted data set label while executing a read or read-deleted command, the FDC skips over that label and proceeds to the next valid data set label. When the FDC executes a read command, deleted data set records are not transferred to the IPC, and no special status presentation is made.

The read-deleted command, however, transfers both deleted and nondeleted data set records to the IPC. In this case, when deleted data set records are transferred, the FDC presents device-end and unit-exception status to the IPC as normal ending status and sets the deleted data address mark sense bit.

9.2.5.3. Data Set Label Compatibility Requirements

Valid data set labels must be prepared by software on an industry-compatible data station before writing data sets. A system using the FDC generates all fields of the data set label. These fields conform to the requirements specified in 9.2.5.1.

Table 9—6 lists and describes the field layout of sectors 8 through 26 of the index track, which comprises the data set labels. These fields are laid out to conform with industry-compatible standards and to assure interchangeability of diskettes. Table 9—7 summarizes the contents of diskette data.

Table 9–6. Data Set Label Field Layout (Part 1 of 3)

Field Position	Field Name	Function
1–4	Header 1	This is a required field. This data set label uses identifier HDR1 to be valid. Sector 08 of the index track (00) is the only sector having this identifier. Sectors 9 through 26 contain identifier DDR1, and the identifier is deleted from positions 1 through 4. The deleted identifier can be modified to a valid HDR1 identifier so that more data sets can be identified on one diskette. To modify the identifier, issue the appropriate commands to obtain the index header position and write in the new identifier for the record to be written.
5	–	Reserved
6–13	Data set name	This is an optional field. This field allows a descriptive name to be assigned to a data set. The name DATA is contained in data set label sector 08 when the diskette is initialized. DATA 09 through DATA 26 are names given to sectors 09 through 26, respectively. A data set name in these sectors can be modified with the appropriate commands.
14–22	–	Reserved

Table 9–6. Data Set Label Field Layout (Part 2 of 3)

Field Position	Field Name	Function
23–27	Record	This is a required field. The field indicates the length of records to be inserted in the data set. A record length is included in the field during initialization. The record length field is from 00001 to 00128 and can be modified to any value from 1 to 128, with appropriate commands.
28	–	Reserved
29–33	BOE	This is a required field. The field indicates the address of the first sector of the data set. The BOE format is: ttOss where: tt Is the track number in positions 29 and 30 of the field. 0 Indicates position 31, which must be 0. ss Is the track number in positions 32 and 33. The address used for BOE must be 01001 or greater.
34	–	Reserved
35–39	EOF	This is a required field. This field indicates the address of the last sector of the data set. The field uses the same format as the BOE field, except that tt is in positions 35 and 36, and ss is in positions 38 and 39. An address larger than 74026 cannot be used; if so, a data set label error occurs. Also, track 74 should not be used for data, because the track is reserved.
40	–	Reserved
41	Bypass data set	This field is used with communications; it allows data and programs to be stored on the same diskette. If the field contains character B, the FDC bypasses the data, and the data set is not converted for tape use. The field must be left blank to convert the data set for tape. During communications, transmissions bypass a data set having a B in the bypass data set field. However, a data set field containing B in a receiving location allows data to be received and written into a data set defined by a data set label.
42	Accessibility	This field controls access to a data set and cannot be modified. Any character in the field prevents accessibility to the diskette or processing of the data set. The field must be blank to process the data set.
43	Write protection	Records written on the diskette are controlled by this field. A character P in the field prevents data from being written on the diskette. If the field is blank, records can be written or read.
44	Interchange indicator	This field must remain blank to allow the data set to be used for information interchange.
45	Multivolume indicator	This field must contain the character C if data is continued to another diskette for a multivolume data set. If the field is blank, the data set is contained entirely on this diskette. If more than two diskettes are required for the data set, the last diskette on which the data set is recorded must contain an L in this field.

Table 9–6. Data Set Label Field Layout (Part 3 of 3)

Field Position	Field Name	Function
46, 47	Volume sequence	This is an optional field. The field is used for multivolume data sets, requiring more than one diskette, to specify the volume sequence. Volume numbers must be in sequential order, up to a maximum of 99, if required.
48–53	Data creation date	This is an optional field. The field is used to record the data on which the recorded data was originated, with the format: yymmdd where: yy Indicates year. mm Indicates month. dd Indicates day.
54–66	–	Reserved
67–72	Expiration date	This is an optional field. The field is used to record the date on which the recorded date set expires. The same format is used as for the data creation date field.
73	Verify indicator	A character V in this field indicates that the last record of the data set has been verified. If the data set was verified (V in the field) and later changed, the FDC replaces the V with blank.
74	–	Reserved
75–79	EOD	This is a required field. This field contains the next sector address of the data set, following the final data record. The final data record of the data set is the EOD address minus 1. The EOD address must be equal to the BOE address when a data set label is created. Each time a record is advanced, the FDC updates the EOD address to keep track of where the next record can be written. When returning to index, the EOD is modified by the operator to the updated EOD.
80	–	Reserved

Table 9–7. Diskette Contents

Track	Sector	Position	Content
00 (index)	01–02	–	80 blanks
	03	1	Reserved for write test
		2–80	Blanks
	04	–	80 blanks
	05 (bad track information)	1–5	Error map (ERMAP)
		6	Blank
		7, 8	First bad track number
		9	Zero
		10	Blank
		11, 12	Second bad track number
		13	Zero
		14–80	Blanks
	06	–	80 blanks
	07 (volume label information)	1–4	Volume number (VOL1)
		5–10	6-character volume name
		11	Accessibility bit. Any character indicates the diskette is not accessible. Blank indicates the diskette is accessible.
		12–76	Blanks
		77, 78	Sector sequence number
		79	Blank
		80	Character W
	08	–	First data set label (Table 9–6).
	09–26	–	Additional data set labels (Table 9–6).
01–73	01–26	–	Data tracks where information is recorded
74	–	–	Not used
75–76	01–26	–	Spare tracks used for data when replacing a defective track in 01 through 73.

9.2.6. Operating Sequences

The operating sequences between the IPC and FDC include the start I/O (SIO), data transfer, and status sequences. These have been explained for the system level in 2.5.1, 2.5.2, and 2.5.3, respectively, and are also applicable with the FDC. This section describes additional characteristics of these sequences, plus other operating sequences applicable to the FDC.

9.2.6.1. SIO Sequence With FDC Condition Codes

The condition codes described for the IPC in 2.5.1 are also applicable for the FDC. Conditions in the FDC that generate four possible condition codes are:

1. Command accepted condition code (00_2)

   This condition code results from FDC and diskette drive availability, valid command parity, and a legal command code. Commands that are accepted, however, may produce device-end or unit-check status presentations without data transfers after the command accepted condition code is presented. This can occur because of a variety of error conditions that may arise during execution of the command.

2. Command rejected condition code (01_2)

   This condition code occurs when the command is invalid because of a bad parity or because the command code is illegal, or when the IPC detects a channel error during the SIO sequence. The condition code also occurs when the read, read-deleted, read-index, read-index-deleted, write-index, write-index-deleted, write, write-deleted, load-track, and load-sector-address commands address a diskette drive that is in stop state, or if the commands address diskette drives 2 or 3 but those drives are not installed.

3. Busy condition code (10_2)

   This condition code results when the SIO instruction is executed if the following conditions exist:

   a. A pending channel status condition is present in the IPC for any integrated control unit, including the FDC.

   b. A pending device status condition is present in the FDC for any diskette drive.

   c. A command was issued to the FDC while it was executing a previous command for any diskette drive.

4. Not operational condition code (11_2)

   This condition code occurs when the FDC is not present for an SIO sequence, or when the FDC does not recognize the address presented during the same sequence. The condition code also occurs when a power-on diagnostic test is in progress or if a power-on diagnostic error condition exists. The condition code also occurs if the FDC detected a control store parity error.

9.2.6.2. Data Transfer Sequences

The FDC transfers data and sense bytes between the IPC and FDC in byte mode or word mode of operation. No restriction is imposed on the byte count or on addressing when using byte mode. However, in word mode, an address must begin at the half-word boundary, and byte counts must be divisible by 4. If the address does not begin at the half-word boundary, the IPC stores or accesses data to or from main storage locations as listed in Table 3—6. All word transfers by the IPC begin at the most significant byte of the main storage location.

Usually, the programmer specifies the number of bytes to be transferred with the FDC command. In some cases, however, the byte count is larger than or equal to the amount of information to be transferred; therefore, the byte count is not exhausted during execution of the command. In these cases, the FDC terminates an operation before the byte count is exhausted when:

1. The sense command byte is greater than 6.

2. The load-track-and-sector-address command byte is greater than 2.

3. Read-index and write-index command byte counts are each greater than 128.

4. Read and read-deleted commands encounter an EOD condition before byte count depletion.

5. Write and write-deleted commands encounter an EOE condition before byte count depletion.

The FDC transfers sense, load-track-and-sector address commands in byte mode. The read-index, write-index-deleted, write-index, diagnostic-read, and diagnostic-write commands are transferred in word mode.

Normally, the FDC transfers the read, read-deleted, write, and write-deleted commands in word mode. However, when a record boundary is approached, the FDC transfers one, two, or three bytes residing at the boundary with byte mode. This eliminates zero-byte insertions by the IPC if the byte count is greater than or equal to the record length.

If the byte count is less than the record length during read, read-deleted, read-index, write, write-deleted, write-index, and write-index-deleted commands, the IPC and FDC perform a 1-word mode data transfer sequence that causes the IPC to insert one, two, or three bytes, each containing eight 0's.

During write operations, the zero byte is written on the diskette. During read operations, the zero byte is sent to main storage. During write operations, if the byte count is less than the record length, the IPC fills the logical record with EBCDIC space characters (40_{16}). The space characters may be immediately preceded by a zero byte or other characters, with the IPC forming a valid parity for the byte.

Rules imposed on the byte count are indicated in Table 3—6 for IPC word mode. No zero byte insertions are made in word mode if the byte count is wholly divisible by 4, or if the byte count is equal to or greater than the actual amount of data to be transferred by the FDC.

The word mode data transfer sequence is initiated by the FDC when it generates the TAKE-4 signal in the interface, after the IPC indicates that the FDC is connected to the IPC bus. The FDC word mode sequence is the same as that used for the card punch word mode sequence, except that a device address is sent to the IPC at the beginning of the sequence. Device address transfer timing is the same as for the ICA data transfer sequence.

9.2.6.3. Data Tranfer Rates

The subsystem provides an 8-bit data path plus parity bit to the IPC. The IPC sends data, commands, and device addresses to the FDC. The FDC sends data, status, sense information, and device addresses to the IPC.

All data is transferred in one of two forms:

1. Data written on or read from the diskette is in EBCDIC.

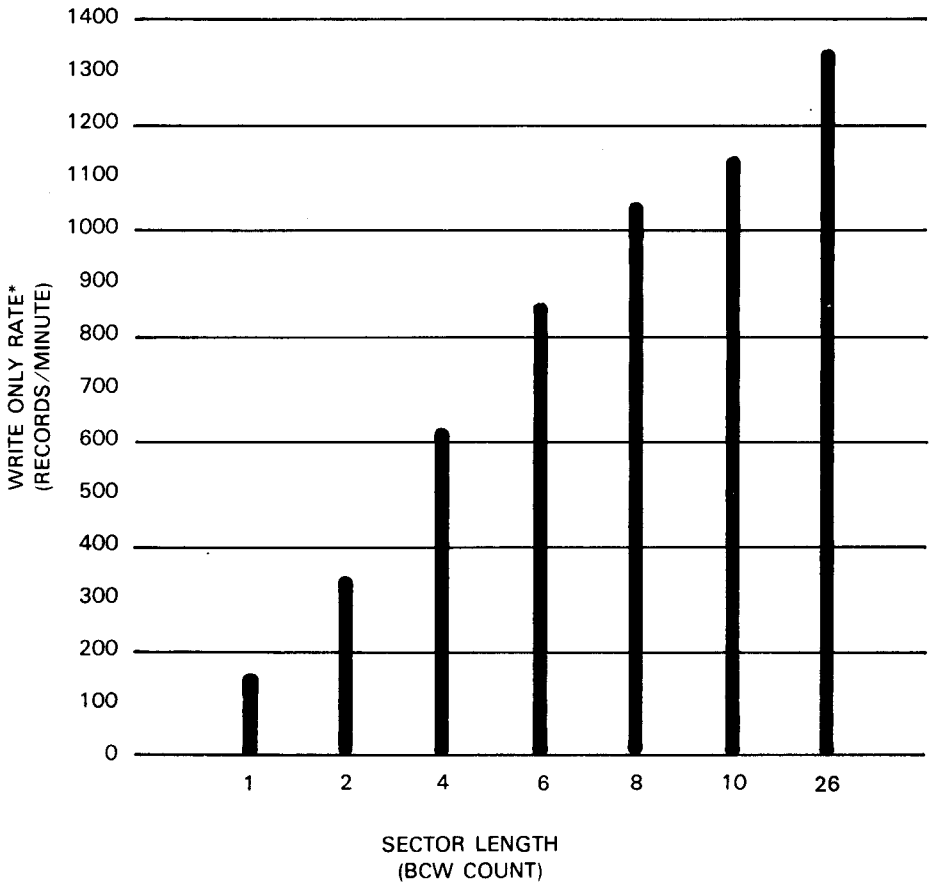
2. All other data is in binary code.

Six record buffers in the FDC provide data transfer. Each buffer can hold a maximum of 128 bytes. The buffers allow:

- A read data rate of 1560 records per minute, provided the user can accept a block of six records during one revolution of the diskette (approximately 167 milliseconds).
- A write data rate of 850 records per minute, provided the user supplies a block of six records during one revolution of the diskette.

The subsystem is capable of reading at a rate of approximately 2340 records per minute under ideal conditions. This assumes that the user can accept data on a track basis. However, the IPC can not maintain the FDC data request rates. Also, the processing system must support the bandwidth needed by the IPC for that type of application. Under the same ideal environment, data can be written at the rate of 1340 records per minute. Ideal data transfer rates require that data chaining be implemented if the diskette track contains more than 1024 bytes. Figure 9—5 illustrates typical timing write-only operations for various sector lengths.

The FDC requires at least 6 milliseconds to transfer 128 bytes to or from the IPC, regardless of the operating mode or contention experienced at the main storage interface. This includes requests for a sense command.



*Time required to write a complete diskette using various BCW counts

Figure 9—5. Examples of Copy Operation Timings

9.2.6.4. Status Sequences

Status sequences in the IPC generate an I/O status tabular interrupt word (IOSTIW), provided no errors are encountered. This word is stored in the I/O status tabular (IOST) buffer control status word (BCSW). Status generated by the FDC is stored in the device status field of the IOSTIW, with no parity check made by the IPC.

The status byte supplies information to the IPC concerning the state of the diskette subsystem. The status byte is presented to the IPC:

- after an SIO sequence in which the command was rejected because of a command parity error or an invalid command, or because the diskette drive was not ready to accept a command;
- when a command is completed; or
- when a transition is made from stop to run state.

The status byte is cleared when the IPC responds to the status byte presentation.

9.2.6.5. Command Modes and Sequences

The FDC can operate in either direct access mode (DAM) or data set mode (DSM). When power is turned on, the FDC is placed in DSM mode if a diskette is loaded into the diskette drive or the load-track-sector (LTS) command is issued with command code 21_{16} (track equals zero and a valid number is used for the sector number register).

The FDC can operate only in DAM when the LTS command is issued with command code 31. While in DAM, the FDC rejects the LTS command in code 21_{16}, as well as the read-index (RI), read-index-deleted (RID), write-index (WI), and write-index-deleted (WID), commands. However, the diagnostic-read (DR), diagnostic-write (DW), and sense commands can operate.

The read (R), read-deleted (RD), write (W), and write-deleted (WD) commands will increment the TAR-SAR registers before executing these commands, unless the command is the first of this set after an LTS command with code 31_{16}. This allows the FDC to be positioned to a particular track-sector of from 00—01 to 76—26. The positional track-sector is processed first by the commands, then causes automatic increment of the TAR-SAR registers for each R, RD, W, and WD command in a string of commands not using the LTS 31_{16} command. In all other operations, these commands function as defined in 9.3.2.

In DSM operation, all commands are valid, and all commands are executed by the FDC on an individual basis. However, it is possible to cause certain command sequences that automatically read sequential data set labels or data sets. Commands appearing in these sequences will increment the appropriate SNR by 1. The two basic sequences that usually increment the SNR automatically are the RI or RID and R or RD sequences.

A string of RI and RID commands may be issued to read a group of sequential sectors on the index track. The FDC initializes the appropriate SNR to sector 8 when a diskette is loaded into the diskette drive.

Software issues RI commands after the diskette is loaded, thereby causing the FDC to read successive sectors of the index track. If this process is not preceded by the LTS 21_{16} command, with track 0 specified, up to 19 sectors may be read. If the process is preceded by the LTS 21_{16} command, the FDC begins executing RI commands at the sector specified by the LTS command.

The SNR is incremented by one for each RI command in the string. If SNR overflows (SNR value is greater than 26), the FDC does not execute the associated RI command. Instead, the FDC presents device-end and unit-check status to the IPC and sets the sector-number-check sense bit.

Any LTS 21_{16} command issued that specifies track 0 will start a new RI command string.

A command other than an LTS 21_{16} or LTS 31_{16} command in a string of RI or RID commands does not affect the rules for incrementing the SNR. The R and RD command sequences also increment the appropriate SNR if the command is received when an end-of-data condition exists for a data set. The incremented SNR value is then used to access the next sector, having a data set label, from the index track.

This next sector is checked for data errors and data set validity (9.2.5.1). If a valid data set label is accessed, the FDC executes the R command. If an invalid data set label is accessed, as determined by the FDC, the command is not executed. Instead, the unit-check and device-end status is presented to the IPC, and the invalid-data-set-label sense bit is set.

Software may read a string of sequential data sets by issuing a string of R commands.

9.2.7. Controls and Indicators

The diskette subsystem is designed so that all operations are under control of the software and FDC logic; therefore, no operator controls are required. The operator needs only to properly install the diskette and close the door of the diskette drive. No physical damage will result to the medium if the diskette is removed while the drive is operating. However, data integrity may be affected if a write operation is in progress when the diskette is removed.

An indicator in the latch push bar of each diskette drive is lit while that drive is reading, writing, or seeking. This indicator may remind the operator to avoid removing the diskette while the indicator is lit. Additional information on subsystem operation is contained in the 8413 subsystem operator reference, UP-8490 (current version).

9.3. PROGRAMMING

This section contains programming information for the diskette subsystem. In particular, information is directed toward processing subsystem commands, status byte, and sense data bytes.

Operation and control of the FDC is dependent on system software. On that basis, it is assumed that software complies with the requirements stated in Sections 2 and 3. It is also assumed that software is totally responsible for generating valid data set labels.

9.3.1. Initiating Operations

Operations with the FDC begin when any diskette drive in the subsystem changes from stop state to run state. This transition causes an attention interrupt sequence to supply the attention status to the IPC and initiate operation. Entering the run state occurs when the operator places a diskette in a drive and closes the door. After two revolutions of the diskette, attention status is presented to the IPC with the diskette drive device address included.

An attention interrupt is not generated if the subsystem is powered up with a diskette already installed in a diskette drive. Subsystem design requires the diskette door to be closed after a diskette is inserted and power has been applied. Attention status is delayed until after power-on diagnostic tests (9.3.7.1) are completed. Once operation is initiated, commands (9.3.2) can be made and executed.

9.3.2. Commands

The commands that can be issued by the processor to the FDC are listed in Table 9—8. Any codes other than those listed in Table 9—8 are rejected, and the unit-check status is returned to the processor. Each command is described in subsequent paragraphs.

Table 9—8. Subsystem Commands and Codes

Command Name	Mnemonic	Code (hexadecimal)	Transfer Mode	Bytes Transferred (maximum)
Load track and sector	LTS	21/31	Byte	2
Read index	RI	12	Word	128
Read index deleted	RID	52	Word	128
Write index	WI	11	Word	128
Write index deleted	WID	51	Word	128
Read	R	02	Byte and word	–
Read deleted	RD	42	Byte and word	–
Write	W	01	Byte and word	–
Write deleted	WD	41	Byte and word	–
Diagnostic read	DR	82–F2*	Word	–
Diagnostic write	DW	81–F1*	Word	–
Sense	Sense	X4**	Byte	6

*Any hexadecimal value within the stated ranges will execute the command.
**Any hexadecimal value may be used for the first digit; the second value (4_{16}) is the significant value for the sense command.

9.3.2.1. Load Track Sector

Command codes 21_{16} or 31_{16} can be used for this command to transfer up to two bytes to the FDC. If the buffer control word (BCW) byte count equals 1, only one byte is transferred.

- Command Code 21_{16}

  Code 21_{16} is a multipurpose command that transfers track and sector addresses or a sector number to an addressed diskette drive. The diskette drive address is specified by the device address in the SIO sequence.

  Software can control three hardware registers in the diskette drive via the load track sector commands. These registers are the track (TAR) and sector (SAR) address registers that contain positioning parameters, and the sector number register (SNR) that contains the index track sector number. The latter number is used to reference data set labels residing on the diskette index track.

  The first byte accessed by the FDC via the 21_{16} command is always treated as a track address. The second byte is always treated as a sector address or sector number. Both bytes must contain valid binary track and sector values; that is, the track address value must be greater than or equal to 0 and be less than 75, and the sector address/number must be greater than 0 and less than 27. If either value is invalid, the FDC does not alter the current TAR, SAR, or SNR values, and it presents device end and unit check status to the IPC.

If the BCW byte count equals 2 or more, and the bytes are valid and accessed without error, the FDC decodes the track address. A track address of 0 causes the second byte to be transferred to the appropriate SNR and present a normal ending status. If the track address is not 0, the bytes are transferred to the appropriate TAR and SAR, provided those register addresses are within range of the current data set label. If the sector specified by the TAR and SAR is not within bounds of the data set label, the FDC does not alter TAR and SAR, but instead presents device-end and unit-check status to the IPC. If no error is encountered by the command, the same presentation is made to the IPC after the command is executed.

If the BCW byte count equals 1, and the bytes are valid and accessed without error, the FDC decodes the track address in the same manner described above for a BCW count of 2 or more, except that no data is transferred to the SNR and normal ending status is presented. Also, a nonzero track address causes the address to be transferred to the appropriate TAR, provided this TAR and the previous unchanged SAR are within the current data set label range. Otherwise, device-end and unit-check status is presented to the IPC.

The FDC may be preconditioned with a 21_{16} command by addressing specific sectors on the index track or sector within a data set. This preconditioning is useful for normal read and write operations as well as for error recovery. When a diskette is loaded into a diskette drive, the FDC forces the SNR in the drive to sector 8. Thus, operations commence with the data set label contained in sector 8, unless software changes the SNR.

After power is turned on or a diskette drive door is closed, the FDC accepts only an LTS 21_{16} command having a track value of 0. Detection of a value of 1 through 74 causes a device-end and unit-check status to be sent to the IPC, with command reject and track and sector address check sense bits set.

- Command Code 31_{16}

Command code 31_{16} operates in a manner similar to command code 21_{16}. The FDC accesses one or two bytes from the IPC. The first byte is the track address and must have a binary value of 0 to 76. The second byte is the sector address and it must be within 1 and 26. If either byte is invalid, the FDC does not alter any hardware registers, and it presents device-end and unit-check status to the IPC. If the BCW byte count is 2 or more, and the bytes are valid and accessed without error, the FDC transfers the bytes to the TAR and SAR, respectively.

The 31_{16} command cannot alter the SNR, but it can set the FDC to DAM (9.2.6.5). The FDC is not concerned with data set boundaries when the 31_{16} command is executed. If the byte count is 1, and the byte is valid and accessed without error, the FDC transfers the byte to the appropriate TAR. Again, the FDC does not alter the SNR, and it sets the FDC to DAM.

The track address may reference any track on the diskette. If the 31_{16} command is successfully executed, the FDC presents device-end status to the IPC. If errors are encountered, the FDC presents device-end and unit check status.

The SNR, TAR, and SAR include a parity bit that is checked by the FDC when the values used by those registers are used again during subsequent operations. Also, the value in the registers is included in the sense bytes to provide necessary positional and data set information required during error recovery.

9.3.2.2. Read Index

The RI command transfers index track sector data from the diskette to the IPC. However, no index track sector data preceded by a deleted address mark is transferred by the FDC. The FDC skips over such records, and it does not indicate that it encountered such records during execution of the RI command. Otherwise, the command is executed in the same manner as the RID command (9.3.2.3).

If an RI command is issued with a BCW byte count of 0, the FDC presents device end with no data transfers. The SNR is incremented with this condition.

9.3.2.3. Read Index Deleted

The RID command causes the FDC to access one sector from the diskette index track and transfer that sector to the IPC if no errors are encountered. The sector is not transferred, however, until it has been entirely accessed and checked for valid cyclic redundancy checks (CRC). If the CRC is incorrect, the FDC rereads the sector until the CRC is corrected or until the retry count (12) is exhausted.

If the retry count is exhausted before correcting the CRC, no data is transferred to the IPC by the FDC. The erroneous data is located in a hardware record buffer that can be accessed by issuing a diagnostic-read command. The specific record address is contained in sense information.

If the CRC is correct, data is transferred to the IPC by the FDC until one of the following events occurs:

1. Self-termination

   The FDC transfers up to 128 bytes to the IPC.

2. Byte count control

   The FDC transfers the number of bytes specified by the byte count in the BCW. The IPC inserts 1, 2, or 3 zero bytes if the byte count is not wholly divisible by 4.

3. The IPC detects an error.

4. The FDC detects an error.

Events 1 and 2 are normal cases, with the FDC presenting device-end status to the IPC. Device-end and unit-exception status is presented if retries were required or if a deleted data set label was encountered. Either event will set the appropriate sense bits.

Event 3 is a channel error where the IPC presents error status to the I/O status tabular (IOST). The FDC presents some type of ending status for this event.

Event 4 results in device-end and unit-check status because the FDC detected an error during execution of the command. If the error involves a bad CRC, SNR, etc., no data is transferred. If the diskette drive goes into stop state, the FDC presents device-end and unit-check status, and data can be transferred for this condition.

The sector transferred to the IPC by the RID command is addressed by contents in the SNR of the appropriate diskette drive. The SNR may be loaded by the appropriate LTS command, or software may issue the RID command directly. The FDC forces the appropriate SNR to a value of 8 whenever the diskette is loaded into that particular diskette drive.

A string of RID commands causes the FDC to read successive index track sectors, beginning at sector 8, if software has not preconditioned the SNR. Software may specify the starting point by issuing the appropriate LTS command. Also, a string of RID commands may be issued to access some number of index track sectors, beginning with and including the specified starting point.

The FDC transfers sectors regardless of information content. If the index track sector is a deleted record, the data is transferred to the IPC, and the FDC presents device-end and unit-exception status to the IPC. Also, the deleted-data-address-mark sense bit is set.

The FDC reads index track sectors as long as the SNR contains a valid sector number. If the sector number is invalid, the FDC does not execute the command, but presents device-end and unit-check status to the IPC. Additional information on reading a string of index track sectors is described in 9.2.6.5.

If an RID command is issued when BCW byte count equals 0, the FDC presents device-end status with no data transfers. In addition, the SNR value is incremented.

9.3.2.4. Write Index

The WI command allows the FDC to access data from the IPC, and write the data on a sector of the index track. The sector receiving the data is specified by an appropriate SNR. An invalid sector number in the SNR prevents the FDC from writing data on the diskette. Instead, the FDC presents device-end and unit-check status to the IPC, and it sets the command-reject and SN-check sense bits.

If the BCW byte count is 0 or the T bit of the BCW is set, no data is sent to the FDC when the WI command is issued. The sector is not written and the data field remains unchanged. In this case, the FDC terminates the command with device-end status, and the SNR remains unchanged.

Up to 128 bytes can be transferred to the FDC with the WI command. After transfer, the FDC writes the data on the appropriate sector of the index track. Information content of the data is not tested during execution of the command.

The FDC computes CRC for the associated data while it is being written on the diskette surface. After data and CRC are written, the FDC reads the data and computes a new CRC. The new CRC includes the recorded CRC in the computation.

If the new CRC equals 0 when all recorded data and its CRC are read, the data is considered correct, and the FCD presents device-end status to the IPC. If the new CRC does not equal 0, an error occurred, and the FDC presents device-end and unit check status to the IPC, as well as setting the CRC-check sense bit.

The WI command may be preceded by an LTS command to precondition the SNR, or the WI command may be issued directly by software. If no preconditioning occurs, the FDC writes the sector specified by the last value in the SNR. The WI command does not increment SNR; therefore, software must load SNR before each WI command if a string of data set labels are to be written.

9.3.2.5. Write Index Deleted

The WID command allows the FDC to access data from the IPC and write the data on a sector of the index track. This data is preceded by a special code written on the address-mark field.

The sector is completely rewritten when the WID command is issued, and the previous data in the sector is destroyed. If the sector data is to be deleted, but original data is to be retained, the sector must be first read, then the same data is to be reissued for the WID command.

If the BCW byte count equals 0 or the T bit of the BCW is set when the WID command is issued, no data is sent to the FDC. In this event, the sector is not written, the address mark and data field remain unchanged, and the FDC terminates the command with a device-end status.

The WID command functions are identical to the WI command, except that the deleted address mark is written for the WID command.

9.3.2.6. Read

The read command allows the data set to be transferred from the diskette to the IPC. However, any records preceded by a delete-address mark are not transferred. The FDC skips over such records without indicating that they were encountered during execution of the R command.

When an R command is sent to an initialized diskette drive, the FDC accesses one sector from the index track of the diskette. This is the sector that correlates with contents of the appropriate SNR. After reading the referenced index track sector, the FDC analyzes contents in that sector to determine if it has a valid data set label.

When the FDC determines that the read sector represents a valid data set label, the FDC executes the command. If the sector does not contain a valid label, the FDC sets the invalid-data-set-label-check sense bit and presents device-end and unit-check status to the IPC. The criteria for a valid data set label are described in 9.2.5.1.

A valid label allows the FDC to execute the R command currently in the data set defined by the data set label. All track and sector addresses, record length, and other data set parameters are derived by the FDC from the data set label.

The FDC automatically seeks the beginning of the data set and recovers the first record from the diskette. While data is being read, the FDC computes a CRC based on data and the CRC stored on the diskette. The entire record is recovered and stored on a hardware record buffer by the FDC.

If the computed CRC equals 0, the FDC initiates data transfers to the IPC, generally in word mode. Byte mode transfers are made for bytes located at the boundary of records whose lengths are odd or not wholly divisible by 4.

While checked data is being transferred to the IPC, the FDC continues reading new data and storing it in other FDC hardware record buffers. The amount of data transferred to the IPC during a given R command is determined by the following conditions:

1. The value contained in the byte count field of the BCW

2. Size of the data set

3. Error conditions detected by the IPC or FDC

Exhausting the BCW byte count during an R command causes the FDC to stop transferring data to the IPC. If the byte count reaches 0 before an entire record is transferred, the FDC stops at the specified position, and residual bytes in the record are discarded. Sending another R command to the FDC when the byte count reaches 0 will cause transfers to begin at the first position of the next sequential logical record. This assumes that software has not issued any WI, WID, RI, RID, or LTS commands.

When the byte count of the BCW goes to 0, the FDC presents device-end status to the IPC if the end-of-data (EOD) record has not yet been transferred. If the EOD coincides with depletion of the byte count, the FDC presents device-end and unit-exception status to the IPC, and it sets the EOD/EOE sense bit.

Condition 2, just cited, is a case where the FDC encounters the EOD during the current R command and the byte count is not exhausted. The FDC, in this case, transfers the last record, presents device-end and unit-exception status to the IPC, and sets the EOD/EOE sense bit.

Error conditions detected by the IPC cause an error status to be generated by the IPC and a termination sequence in the FDC. The IPC presents a terminating signal, and the FDC presents an ending status to the IPC.

The FDC may encounter CRC errors during a given R command, causing the FDC to reread the record containing the error. The FDC rereads the record 12 times before declaring the data unrecoverable. If the retry is successful, the FDC resumes data transfers to the IPC. If the retry count is exhausted but the error continues to appear, all data transfers are halted by the FDC, and the data-check, CRC-check, and retry sense bits are set. Sense bytes contain contents of the SNR and the track and sector addresses where the current R command began. This information supplied by the FDC provides software with a basis for initiating a retry. The track and sector addresses point to the beginning of the current data block that software may wish to retrieve.

Multidata set volumes and multivolume data sets may be read by the FDC. Appropriate LTS and RI commands give software capabilities for searching for a specific data set label. In addition, the FDC automatically initializes a specific SNR to sector 8 so that software may issue an R command without preconditioning the SNR. In this case, the FDC accesses sector 8 of the index track and determines if the sector contains a valid, non-deleted data set label.

Valid data set labels result in data transfers, while invalid labels result in a device-end and unit-check status presentation to the IPC. If the data set label is deleted, the FDC accesses sectors from the index track until it finds a valid data set label, exhausts the data set label capacity of the diskette, or encounters an invalid data set label.

Assuming that a data set has been successfully read, the FDC automatically advances to the next index track sector for each R command issued while in DSM, provided the command is not preceded by appropriate LTS, RI, RID, WI, or WID commands. Thus, an uninterrupted string of R commands may result in transfer of consecutive nondeleted data sets to the IPC. If the SNR is incremented to a value greater than 26, the FDC responds to an R command with device-end and unit-check status, and no data transfer occurs.

Multivolume data sets cause the FDC to respond to an R command in the normal manner provided the data set resides in the current volume. When the FDC reaches the EOD for the current volume and the data set is continued on another volume, it presents device-end and unit-exception status to the IPC after the EOD record is transferred to the IPC. The FDC also sets the end-of-volume sense bit for this case. However, if the EOD coincides with the last volume of the data set, the FDC presents device-end and unit-exception status, and sets the EOD/EOE sense bit.

If the R command is issued when the BCW byte count equals 0, the FDC presents device-end status with no data transfers. This condition also causes the TAR/SAR values to be incremented.

If an R command is issued and the data set is empty (EOD = BOE), the FDC presents device-end and unit-exception status, and the EOD/EOE sense bit is set. No data transfers are made with this condition.

An LTS command that sets the TAR/SAR values beyond the EOD value when an R command is issued will cause the FDC to terminate the command with device-end and unit-check status, and set the end-of-volume sense bit.

9.3.2.7. Read Deleted

The RD command transfers deleted data set records to the IPC after the records are checked. No records are skipped when the FDC executes the RD command. If deleted data set records are encountered, the FDC presents device-end and unit-check status to the IPC, and sets the deleted-data-address-mark sense bit.

Operation of the RD command is closely similar to operation of the R command (9.3.2.6), except the RD command transfers deleted data set records to the IPC.

Issuing an RD command when BCW byte count equals 0 causes the FDC to present device-end status, and no data transfers are made. In addition, the TAR/SAR values are incremented.

An RD command issued when the data set is empty (EOD = BOE) causes the FDC to present device-end and unit-exception status, and set the EOD/EOE sense bit. No data transfers are made with this condition.

Issuing an RD command when an LTS command has set the TAR/SAR values beyond the EOD value will cause the FDC to terminate the command. Device-end and unit-check status is presented, and the end-of-volume sense bit is set.

9.3.2.8. Write

The W command transfers data in a data set from the IPC to the diskette. A W command issued to an initialized diskette drive causes the FDC to access a sector from the index track of the diskette that correlates with contents of the appropriate SNR. After reading the referenced index track sector, the FDC analyzes contents of the sector to determine if it is a valid data set label (9.2.5.1).

The FDC executes the W command if it determines that it has read a valid data set label. If the data set label is invalid, or if the data set is "write- protected", the FDC sets the appropriate invalid-data-set-label, write-protect-check, or hardware-write-protect sense bit, and presents device-end and unit-check status to the IPC.

A valid data set allows the current W command on the data set defined by the data set label to be executed. The FDC derives from the data set label all parameters on track and sector addresses, record length, and other data set information.

The FDC accesses data from the IPC while searching for the first physical sector of the data set. The FDC then stores this data record (or less) on a hardware record buffer before the actual writing operation. The FDC computes a CRC while data is being written on the diskette.

The amount of data accessed before writing is governed by the record length field of the data set or by the byte count field of the BCW. If the byte count does not go to 0 before reaching the record length, an entire record is accessed, stored in the record buffer, and ultimately written on the appropriate physical sector of the data set.

Data set records may contain up to 128 bytes of data. A physical sector includes address information and the CRC. If a data set label record field is less than 128 bytes long, the FDC fills the unused positions of the sector data portion with 0's.

The CRC is computed on an entire sector of 128 bytes. If a byte count reaches 0 before the record length is reached, and it is not wholly divisible by 4, the specified number of bytes are accessed from the IPC and the required 0's are inserted. All remaining positions within the defined record are loaded with blanks (40_{16}).

CRC calculations include 128 bytes of the physical sector. For example:

1. Record length equals 80 bytes.

2. BCW byte count equals 57 bytes.

The FDC accesses 57 bytes from the IPC. In this case, the FDC forms an 80-byte record consisting of the 57 bytes plus 3 zero bytes and 20 space characters. The FDC also writes zero bytes in the remaining 48 positions of the sector that are outside the actual record.

The FDC accesses additional data from the IPC while a given record is being written on the diskette. Writing continues in this manner until the byte count in the BCW is depleted, the EOE record is encountered, or a track boundary is reached. Each condition causes the FDC to read-check all data written since the previous read-check operation. Thus, with maximum throughput, the FDC can write and read-check 26 data records before processing continues or before presenting status to the IPC.

Four status conditions can occur during data access:

1. Device-end status is presented if the byte count in the BCW was exhausted during the current W command before EOE is encountered, and no read-check errors were detected during execution of the command.

2. Device-end and unit-exception status is presented, the EOD/EOE sense bit is set if the EOE was written, no errors were detected, and another volume is not required.

3. Device-end and unit-exception status is presented and the end-of-volume sense bit is set if another volume is required for a multivolume data set.

4. Device-end and unit-check status is presented along with the CRC-check sense bit (SB1/7) being set if the read-check operation results in a CRC error.

The read-check operation requires reading of a particular record. The FDC computes the CRC as the record is read. If the computed CRC equals 0, the FDC continues processing data, or it presents the normal ending status, as described above. If the CRC does not equal 0, the FDC sets the appropriate sense bit and presents unit-check and device-end status.

Sense bits contain error indicators, contents of the SNR (data set label pointer), and track and sector addresses of where the current W command began. This provides software with physical information to initiate a retry. Track and sector addresses point to the beginning of the data block that was not successfully written.

The FDC supports writing multidata set volumes and multivolume data sets. The LTS, RI, RID, WI, and WID commands give software the ability to search the index track and write new or modified data set labels. Software must assume responsibility for preparing and writing all fields in every data set label.

The FDC is initialized to index sector 8. Write operations may begin at this point, provided this sector contains a valid data set label. The FDC does not increment SNR after completion of W, WD, WI, or WID commands. Thus, software must precondition the appropriate SNR if a string of data sets are to be written.

Multivolume data set labels must indicate that a multivolume data set is being written. When the FDC reaches the end of a volume (last sector or EOE), the FDC presents device-end and unit exception status to the IPC, and sets the end-of-volume sense bit. If EOE coincides with the last volume of the data set, the FDC presents device-end and unit-exception status and sets the EOD/EOE sense bit.

If no data is sent to the FDC (BCW byte count = 0 or T bit in BCW is set) when the W command is issued, the sector is not written and the data field remains unchanged. The FDC terminates this command with device-end status, and the TAR/SAR values remain unchanged.

If the SNR is pointing to an index track sector containing a deleted data set label when a W command is issued, the FDC presents device-end and unit-check status, and the invalid-data-set-label sense bit is set. No writing occurs for this condition.

After writing the final record of a data set, the FDC presents device-end and unit-exception status, and either EOD/EOE sense bit or the end-of-volume sense bit is set. If another W command is issued to the same data set, the FDC presents device-end and unit-check status, and no writing will take place.

9.3.2.9. Write Deleted

The WD command allows the FDC to access data from the IPC and write the data on a sector of the data set. The command also writes a special code in the address-mark field preceding the accessed data.

The sector is completely rewritten when the WD command is issued, and previous data in the sector is destroyed. If deletion of the sector and retaining of the original data is desired, the sector must first be read, then the same data reissued for the WD command.

If BCW byte count equals 0 (or T bit of the BCW is set) when the WD command is issued, no data is sent to the FDC. With this condition, the sector is not written, and the address mark and data field remain unchanged. The FDC terminates the command with device-end status.

The WD command is identical to the W command (9.3.2.8), except for writing the deleted-address-mark.

9.3.2.10. Diagnostic Read

The FDC contains a 1024-byte read and write memory (RAM) composed of six record buffers of 128 bytes each, and a 256-byte working register. Eight DR commands allow transfer of RAM data to the IPC. The starting RAM location is specified by DR individual command codes listed in Table 9—9.

Table 9—9. DR and DW Command Codes

Command (hexadecimal)		RAM Starting Address (hexadecimal)	Function
DR	DW		
82	81	3FF	Record buffer 0
92	91	37F	Record buffer 1
A2	A1	2FF	Record buffer 2
B2	B1	27F	Record buffer 3
C2	C1	1FF	Record buffer 4
D2	D1	17F	Record buffer 5
E2	E1	0FF	FDC working registers
F2	F1	07F	FDC working registers

Any DR command transfers the number of bytes specified by the BCW byte count field. The FDC begins all data transfers at the RAM locations specified by individual DR command codes (Table 9—9).

Software may read any number of bytes. If the byte count is greater than 768 for a diagnostic command sent to the record buffer area ($82—D2_{16}$), the command will wrap around within that record buffer area only. If the byte count is greater than 256 for a working-area register area (E2, $F2_{16}$), the command will wrap around within that working area only. If the byte count is not wholly divisible by 4, the IPC inserts zero bytes into main storage. When a byte is transferred, the FDC decrements the RAM address.

The FDC transfers data to the IPC until one of the following events occur:

1. The byte count is depleted.

2. An error is detected by the IPC or FDC.

The first event causes presentation of device-end status. The second event results in a status presentation if a channel error occurred. The FDC presents an ending status, consisting of device-end or device-end and unit-check, when the second event occurs.

The FDC executes the DR command regardless of the state of the associated diskette drive. The DR commands do not alter the subsystem operating mode.

9.3.2.11. Diagnostic Write

Eight DW commands are provided (Table 9—9). Six codes transfer data from the IPC to pertinent record buffers in the FDC. The E1 command code transfers data from the IPC to the 256-byte working register area. The F1 command code serves as an enable for the E1 command.

The starting FDC RAM addresses for the six write buffer command codes are listed in Table 9—9. These six codes are not self-terminating; i.e., the byte count in the BCW specifies the amount of data transferred. If the byte count is higher than 768, the command causes data to wrap around within the record buffer area of the RAM. These codes do not alter the working register area of the RAM.

The E1 command is a special write code that allows writing in the diskette parameter list (DPL) area of the RAM. This data can completely change the characteristics of the subsystem, and thereby raise integrity questions.

The F1 command enables the DPL diagnostic write and E1 command functions as the actual DW command. Any command issued between the F1 and E1 sequence will remove the enabled condition.

Each time software issues an F1-E1 sequence (in that order), the number of bytes specified in the BCW is written into DPL area of the RAM, beginning at location OFF. If the E1 command is issued without a preceding F1 command, E1 is rejected. F1 is a no-op command in all respects except for enabling E1. This greatly reduces inadvertent use of the E1 command and possible disruption of subsystem integrity.

A valid F1-E1 sequence transfers an arbitrary number of bytes into the working register area of the RAM. If the byte count is larger the 256, the command wraps around within the RAM area instead of in the buffer area.

A DW command presents the same ending status as the DR command (9.3.2.10). In addition, the FDC executes a DW command regardless of the state of the associated diskette drive.

The DR and DW commands do not alter the operating mode of the subsystem.

It should be noted that execution of the F1-E1 sequence may alter future operations of subsystem commands. Therefore, the subsystem should be reinitialized if the F1-E1 sequence is executed.

9.3.2.12. Sense

The sense command is used for test, diagnostic, and error recovery. Software may specify any or all of six sense bytes available in the FDC. The sense command causes byte mode transfers.

The sense command may terminate for any of the following reasons:

1. All six sense bytes are successfully transferred to the IPC.
2. The byte count in the BCW is depleted before the maximum number of sense bytes are transferred.
3. An error occurred in the device or channel.

Conditions 1 and 2 cause device-end presentation to the IPC. Condition 3 results in IPC channel error status and ending status from the FDC.

If the FDC detects a parity error during execution of a sense command, the FDC presents device-end and unit-check status. A parity error during execution of the sense command causes the FDC parity-error sense bit (SB2/2) to be overlaid. Normally, the sense bits are not overlaid.

The FDC executes the sense command regardless of the state of the associated diskette drive. The command does not alter the subsystem operating mode.

The sense command does not clear the sense byte of the device addressed by the command, unlike all other commands of the repertoire. Additional information on sense bytes is presented in 9.3.4.

9.3.3. Status Byte

Table 9—10 lists and describes each bit of the status byte.

Table 9—10. Status Byte ***(Part 1 of 2)***

Designation	Bit	Function
Attention	0	Indicates that the diskette drive has made a transition from stop to run state. Run state is entered after the diskette is inserted, the diskette drive door is closed, and two revolutions of the diskette are detected.
—	1	Not used, set to 0.
—	2	Not used, set to 0.
—	3	Not used, set to 0.
—	4	Not used, set to 0.
Device end	5	Indicates completion of a previously initiated command by the FDC, and availability to execute a new command. Successful completion of a command is indicated by device-end bit set without unit-check bit (6) being set.
Unit check	6	Indicates an unusual condition at the subsystem level was detected during execution of the current command if unit-check bit is presented with device-end bit (5). If unit-check is presented alone, indicates command was rejected during SIO sequence.

Table 9—10. Status Byte (Part 2 of 2)

Designation	Bit	Function
Unit exception	7	Indicates an abnormal condition occurred during operation. The condition is not necessarily an error, and does not affect validity of the data transferred. The sense bytes should be interrogated to define the condition. Unit-exception is always set with another sense bit. The following conditions cause unit-exception to be presented with device-end status: 1. FDC encountered EOD/EOE condition while executing RD, R, WD, or W commands. 2. FDC encountered an end-of-volume condition while reading or writing a multivolume data set. 3. An R, RD, RID, RI command or seek operation resulted in automatic error recovery during a read operation. 4. FDC encountered a deleted record during execution of RID or RD command.

9.3.4. Sense Bytes

Sense bytes are sent by the FDC to the IPC in response to a sense command (9.3.2.12) from the system. Sense bytes contain error and operational information concerning the last command (except sense command) issued to the FDC. Error information in the sense byte is cleared when the next command (except sense) is accepted.

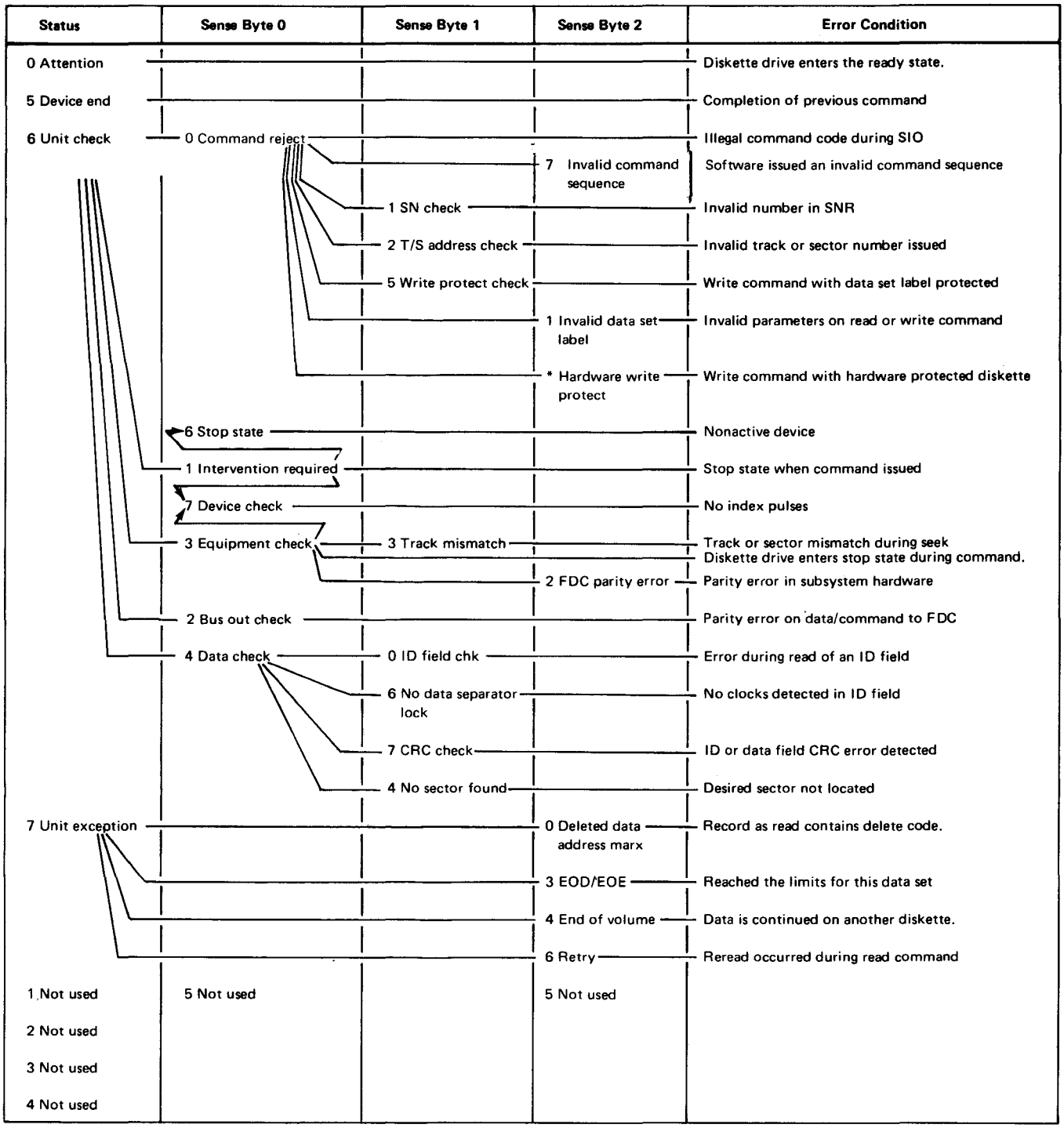
When power is turned on, all sense bytes, except bits 0, 1, and 2 of sense byte 2, are cleared to 0's. These three uncleared bits remain set to indicate hardware conditions.

Sense byte 0 summarizes detected error conditions that are further defined in sense bytes 1 and 2. Sense bytes 3, 4, and 5 provide operational data, such as track and sector locations.

Table 9—11 summarizes all bits of the status byte and sense bytes. Table 9—12 lists and describes the sense byte bits. Figure 9—6 summarizes the relationship of status bits, sense bits, and error conditions.

Table 9—11. Summary of Status and Sense Bits

Byte	Bits							
	0	1	2	3	4	5	6	7
Status	Attention	Not used	Not used	Not used	Not used	Device end	Unit check	Unit exception
Sense 0	Command reject	Inter-vention required	Bus out check	Equipment check	Data check	Not used	Stop state	Device check
Sense 1	ID field check	SN check	Track sector address check	Track mismatch	No sector found	Write protect check	No data separator check	CRC check
Sense 2	Deleted data address mark	Invalid data set label	FDC parity error	EOD/ EOE	End of volume	Not used	Retry	Invalid command sequence
Sense 3	Direct access mode	Feature installed	Hardware write protect	SNR 0	SNR 1	SNR 2	SNR 3	SNR 4
Sense 4	Not used	Track address 0	Track address 1	Track address 2	Track address 3	Track address 4	Track address 5	Track address 6
Sense 5	Not used	Not used	Not used	Sector address 0	Sector address 1	Sector address 2	Sector address 3	Sector address 4



*The hardware write protect bit is in sense byte 3, bit 2.

Figure 9—6. Error Conditions Indicated by Status and Sense Bits

Table 9–12. Sense Bit Meanings (Part 1 of 4)

Bit	Meaning
	Sense Byte 0
0 Command reject	Sets for any of the following reasons: 1. Illegal command code is detected during SIO sequence. Illegal command also causes 01_2 condition code (9.2.6.1) and unit check status (Table 9–10). 2. Error condition detected during execution of a legal command code. Specific errors set individual sense bits as well as command reject bit. The error conditions cause device-end and unit-check status presentation to the IPC. The FDC sets the command reject sense bit when any of the following sense bits are also set: ■ SN check (SB1, bit 1) ■ Track or sector address check (SB1, bit 2) ■ Write protect check (SB1, bit 5) ■ Invalid data set label (SB2, bit 1) ■ Hardware write protect (SB3, bit 2) 3. A DW (E1) command was issued without an enabling (F1) command immediately preceding it. This error condition results in a device-end and unit-check status to the IPC. 4. While in DAM (SB4, bit 0 is set), the following commands were issued: RI, RID, WI, WID, LTS 21 with track 0, or LTS 21 with track 0 but no sector number specified. This error causes device-end with unit-check status presentation to the IPC. 5. An SIO sequence that caused the FDC to reject all commands except sense, DR, or DW because the addressed diskette drive was in stop state or is not installed. This causes condition code (01_2), unit-check status, stop state (SB0, bit 6), and intervention required (SB0, bit 1) bits to be set.
1 Intervention required	Set by FDC to indicate that an RI, RID, R, RD, WI, WID, W, WD, or LTS command was issued to a diskette drive that was in stop state (SB0, bit 6). This bit is also set when the FDC sets the device-check sense bit (SB0, bit 7). When intervention-required bit is set, the FDC presents device-end and unit-check status to the IPC.
2 Bus out check	This bit is set when: 1. An incorrect parity in a command byte is detected during an SIO sequence. 2. A parity error is detected during an outbound data transfer. Upon completion of the take-4 sequence, the FDC presents device-end and unit-check status to the IPC.
3 Equipment check	This bit is set when: 1. The diskette drive enters stop state (SB0, bit 6) while an RI, RID, R, RD, WI, WID, W, WD, or LTS command is being executed in that diskette drive. 2. The FDC sets the device-check (SB0, bit 7) sense bit. 3. The FDC sets the track-mismatch (SB1, bit 3) sense bit because a retry was unsuccessful. 4. The FDC sets the FDC parity error (SB2, bit 2) sense bit. For each of these errors, the FDC terminates the current command and presents device-end and unit-check status. For item 3, the FDC also sets unit-exception status.

Table 9–12. Sense Bit Meanings (Part 2 of 4)

Bit	Meaning
	Sense Byte 0 (cont)
4 Data check	This bit is set for various data errors related to the diskette or diskette drive. If a retry is unsuccessful, the same errors will also set the following sense bits: 1. ID field check (SB1, bit 0) 2. No data separator lock (SB1, bit 6) 3. CRC check (SB1, bit 7) 4. No sector found (SB1, bit 4) For each of these error conditions, the IPC terminates the current command and presents device-end, unit-check and unit-exception status to the IPC.
5	Not used; always set to 0.
6 Stop state	This bit is set when the addressed diskette drive is not ready for a command. A diskette drive is ready when the DRIVE SELECT signal is true, a diskette is inserted, the diskette door is closed, and two index pulses have been detected. The diskette drive is not ready if the diskette door is open or the DRIVE SELECT signal is inactive. If the diskette drive is not in use, the stop-state setting does not occur for any status presentations. When stop-state causes command-reject or equipment-check setting, the device-end and unit-check status is also presented to the IPC.
7 Device check	This bit is set when the FDC is executing the RI, RID, R, RD, WI, WID, W, or WD command but no index pulse is detected. With this condition, the FDC terminates the command and presents device-end and unit-check status to the IPC. In addition, the equipment-check and intervention-required sense bits are set when the device-check bit is set.
	Sense Byte 1
0 Field check	This bit is set when the FDC detects an error in the ID field of any sector while read and write operations are being performed. The ID field includes address marks, track and sector identification, and CRC bytes that precede each data record. This sense bit is set when the FDC cannot read the ID field for a required sector. The errors may be caused by a CRC check, or a no-data-separator lock condition. The FDC attempts 12 retries on a given ID field before declaring an error condition. Device-end and unit-check status is presented whenever the ID field check sense bit is set and retry is unsuccessful.
1 SN check	This bit is set when the FDC encounters an invalid sector number during execution of any command that references a sector number register (SNR). One of 26 sectors on the index track of the diskette must be addressed by the SNR. If contents of the addressed SNR equal 0 or if the addressed value is higher than 26, the SN-check sense bit becomes set. Detection of the error causes termination of the command, the command-reject sense bit (SB0, bit 0) is set, and device-end and unit-check status is presented to the IPC.
2 Track or sector address check	This bit is set when software loads a track and/or sector address that is outside the range permitted for the diskette or data set described by the current data set label (9.3.2.1). When this bit is set, the FDC also sets the command-reject sense bit (SB0, bit 0), terminates the current command, and presents device-end and unit-check status to the IPC.
3 Track mismatch	An incorrect track encountered during seek operation causes the FDC to set this bit. If a retry is successful, the FDC sets the equipment-check sense bit (SB0, bit 3), and device-end and unit-exception status. If the retry is unsuccessful, the FDC sets this bit as well as the equipment-check sense bit, and device-end, unit-check, and unit-exception status.

Table 9–12. Sense Bit Meanings (Part 3 of 4)

Bit	Meaning
	Sense Byte 1 (cont)
4 No sector found	Detection of two index pulses without locating a specified sector causes the FDC to set this bit. If retry is successful, the FDC sets this bit and presents device-end and unit-exception status. If retry is unsuccessful, the FDC sets this bit as well as data check sense bit (SB0, bit 4), and presents device-end, unit-check, and unit-exception status.
5 Write protect check	Issuing a W or WD command while the associated data set label's write-protected position contains a P character or while a hard-write-protected diskette is mounted in the diskette drive causes the FDC to set this bit. The error also causes the command-reject sense bit (SB0, bit 0) to be set and terminate the command, and device-end and unit-check status is presented by the IPC.
6 No data separator lock	A no-clocks condition encountered in the ID field of any sector addressed by the current command while processing an RI, RID, WI, WID, R, RD, W, or WD command causes the FDC to set this bit. The ID-field-check sense bit (SB1, bit 0) is also set, the current command is terminated, and device-end and unit-check status is presented.
7 CRC check	A CRC error detected during an RI, RID, WI, WID, R, RD, W, or WD command causes the FDC to set this bit. The CRC may pertain to the data record or ID field of the associated sector. If the CRC error pertains to the ID field, the FDC also sets the ID-field-check sense bit (SB1, bit 0). When CRC-check sense bit is set but a retry is unsuccessful, the data-check sense bit (SB0, bit 4) is also set, the current command is terminated, and device-end, unit-check, and unit-exception status is presented to the IPC.
	Sense Byte 2
0 Deleted data address mark	A deleted record encountered during execution of an RID or RD command causes the FDC to set this bit. The deleted record, consisting of a data set label or record in the data set, is transferred to the IPC. Device-end and unit-exception status is presented to the IPC as an ending status. That is, the FDC does not terminate data transfers after it transfers a deleted record to the IPC. Status is presented after all bytes specified by the command are transferred to the IPC.
1 Invalid data set label	An invalid data set label encountered during execution of an R, RD, W, or WD command causes this bit to be set. (Refer to 9.2.5.1 for criteria of an invalid data set label.) The FDC also sets command-reject sense bit (SB0, bit 0), terminates the current command, and presents device-end and unit-check status to the IPC.
2 FDC parity error	Detection of a read-only-memory (ROM) or read-and-write-memory (RAM) parity error causes any of the following conditions: ■ A RAM parity error occurring during execution of a command causes this bit to be set, and device-end and unit-exception status is presented. ■ A recoverable ROM parity error during execution of a command causes this bit to be set, and device-end and unit-check status is presented. ■ A nonrecoverable ROM parity error during a command causes either device-end and unit-check status or only unit-check status to be presented. Sense bits cannot be set with this type of error. If a subsequent command is required, it is presented with the not-operational condition code (11_2).
3 EOD/ EOE	Encountering an EOD record during R and RD commands or an EOE record during W and WD commands causes the FDC to set this bit. The EOD/EOE record is transferred to or from the IPC, and subsequently the FDC presents device-end and unit-exception status to the IPC.
4 End of volume	An EOD/EOE condition encountered while the FDC is reading or writing a multivolume data set when another volume is required causes the FDC to set this bit. The EOD/EOE sense bit (SB2, bit 3) is not set when this bit is set. The FDC presents device-end and unit-exception to the IPC as ending status.

Table 9–12. Sense Bit Meanings (Part 4 of 4)

Bit	Meaning
Sense Byte 2 (cont)	
5	Not used, always set to 0.
6 Retry	When the FDC rereads a data set label or data set record during an RI, R, RID, or RD command, this bit is set. The bit is also set if the FDC is to reinitialize an implied seek operation because a track mismatch condition is detected. If a retry is successful, the FDC presents device-end and unit-exception status upon normal completion of the command. If a retry is unsuccessful, the command is terminated and device-end, unit-check, and unit-exception status are presented to the IPC.
7 Invalid command sequence	This sense bit indicates that software has issued an illegal command sequence to the subsystem. Device end and unit check status will be presented. The command reject sense bit (SB0/0) will also be set. The following invalid command sequences can occur: 1. A read command is issued when TAR and SAR values are equal to or greater than the EOD value. 2. An LTS 21 with a track value of 1–74 was issued after a power-up or door closure condition.
Sense Byte 3	
0 Direct access mode	This sense bit is set when the control unit is in direct access mode. When this bit is inactive, the control unit is in data set mode.
1 Feature installed	This bit is self-setting when the diskette expansion feature is installed to add diskette drive 2 and diskette drive 3 to the subsystem. No status presentation is made when this bit is set. The bit may be tested by addressing any diskette drive.
2 Hardware write protect	Detection of an uncovered diskette write-protect hole causes this bit to be set by the FDC. If a W, WD, WI, or WID command addresses a diskette that is hardware-write protected, regardless of the command sequence, the sense bit is set and the command is terminated. In addition, the command-reject (SB0, bit 0) and write-protect-check (SB1, bit 5) sense bits are set, and device-end and unit-check status is presented to the IPC.
3–7 Sector number register	The five sector number register bits 0 through 4 (SNR0 through SNR4) of the sector number register (SNR) addressed by the sense command are stored in the corresponding bit positions of sense byte 3. SNR0 is the highest-order bit. The SNR is used as a pointer to a specific sector of the index track.
Sense Byte 4	
0	Not used, always set to 0.
1–7 Track access register	The seven track access register bits 0 through 6 (TA0 through TA6) of the track address register (TAR) addressed by the sense command are stored in the corresponding bit positions of sense byte 4. TA0 is the high-order bit. TA0 through TA6 reference the track where a given R, RD, W, or WD command began. These seven bits are loaded when an LTS 21 with TT=0 is issued, or when an R or W command is executed.
Sense Byte 5	
0–2	Not used, always set to 0.
3–7 Sector address register	The five sector address register bits 0 through 4 (SA0 through SA4) of the sector address register (SAR) addressed by the sense command are stored in the corresponding bit positions of sense byte 5. SA0 is the high-order bit. SA0 through SA4 reference the sector where a given R, RD, W, or WD command began. These five bits are loaded when an LTS 21 command with TT=0 is issued or when an R or W command is executed.

9.3.5. Device Addressing

The four diskette drives are uniquely specified during SIO, data transfer, and status sequences by an 8-bit device address. The addresses are presented by the IPL to the FDC without parity checks; also, the IPC does not check parity of the device address presented by the FDC.

Device address assignments for diskettes are as follows:

Diskette Number	Device Address (hexadecimal)
0	10
1	11
2	12
3	13

Diskette numbers 0 and 1 are included with the FDC in the basic subsystem. Diskettes 2 and 3 are installed as part of the subsystem expansion feature.

9.3.6. System Initialization With Diskettes

Initial load of control storage (ILCL) and initial program load (IPL) system operations are supported by the FDC and require the use of two diskettes. Either or both operations may be performed with any operational diskette drive. Detailed procedures for performing the ILCL and IPL are described under initial program load procedures in the 90/30 operations handbook for operators, UP-8511 (current version).

9.3.7. Diagnostics

The subsystem can be tested by using diagnostic programs written to activate the FDC and diskette drives. The LTS, sense, diagnostic-write, and diagnostic-read commands may be used to validate the FDC data path control logic. These commands test the IPC-FDC interface, FDC hardware record buffers, sector number registers, and track and sector address registers.

The diskette drive may be tested by using a diskette to perform read and write operations. Diskettes having data sets with known data patterns may be tested by reading the diskette to determine the FDC's ability to recover data.

Data sets having a variety of data set labels may be written and read on another diskette to perform comprehensive tests of the FDC. Various data set label options may be selected to perform these tests.

A test program can also include such FDC functions as detection of an invalid data set label, incrementing an SNR, and other similar operations. The FDC command repertoire may be included in developing comprehensive test and diagnostic programs.

9.3.7.1. Power-On Diagnostics

Upon initial application of power to the subsystem, the operator must avoid any operations for at least 1 second. This waiting period allows the FDC to execute a resident diagnostic microprogram that always follows a system reset. If system reset is reactivated by a switch on the processor operator/maintenance panel, the microprogram is restarted from the beginning by the FDC.

When the resident diagnostic microprogram has completed, an FDC flag is set so that subsequent activation of the system reset does not retrigger the resident diagnostic microprogram. Reactivation of the microprogram occurs only when the subsystem performs another power-on sequence. Failure to wait at least 1 second to execute a command after system reset causes the FDC to present condition code 11_2.

If the resident diagnostic microprogram detects an error that does not correct itself after several repeats of the portion of the test that detects the error, all processing is halted and the FDC "hangs up" (suspends operation). The test that failed is encoded and displayed on a printed-circuit board for use by the Sperry Univac customer engineer.

Attempting to operate the subsystem after the resident diagnostic program detects an error will cause the FDC to supply condition code 11_2 to the IPC. This condition code is displayed on the processor operator/maintenance panel.

9.3.7.2. Malfunction Timer

The FDC contains a 10-second timer that prevents the subsystem from "hanging" the channel in the event of a subsystem malfunction. A microprogram in the subsystem continually resets the timer for a 10-second wait.

If a malfunction occurs in the subsystem while a command is being processed, the 10-second time period will elapse and cause a device-end and unit-check status to be supplied to the IPC. If the FDC was not active, however, unit-check status is presented at the next SIO operation.

9.3.8. Error Detection

The subsystem provides required error logging information by presenting status and detailed sense error conditions to the IPC. Error logging is a responsibility of system software.

9.3.8.1. Error Types

Three types of errors are detected by the subsystem:

- Seek errors

  The diskette drive has a maximum seek error rate of one wrong track in 10^6 seeks. A seek is the positioning of the access head in the diskette drive to a specified location.

- Recording errors

  Diskette errors are detected by two CRC bytes that are appended to the data and ID fields in each sector. The particular error detection code is a "fire" code that detects all error bursts of 16 bits or less. The probability of not detecting an error is 1 in 2^{15} for a burst of 17 bits, and 1 in 2^{16} for a burst greater than 17 bits. The CRC bytes also detect two error bursts in the same field, each having a length of 2 bits or less.

  The diskette error rate does not exceed one nonrecoverable error in 10^{12} bits, or one recoverable error in 10^8 bits.

- Thru checking

  Internal parity circuits detect single bit errors in the subsystem. Parity checks are provided on all read operations from the FDC's ROMs. Parity checking and generation is provided on all read/write operations involving use of FDC's RAMs.

9.3.8.2. Automatic Retry

Upon detecting an error, the subsystem executes retries on either of two levels:

1. Retries are executed on certain medium-mechanism-related errors. These retries are controlled by microprograms in the FDC.

   If a data CRC error is detected, the FDC automatically retries 12 times to complete the operation before indicating an error condition to the IPC. The FDC also automatically retries for each of the following errors:

   a. No data separator lock

   b. Bad tracks

   c. Address mark CRC error

   d. Track mismatch

   e. No sector found

   Three direct retries are made first, then three retries of a special procedure are made if the error persists. The microprogrammed procedure for errors a and b is a head jog. The microprogrammed procedure for errors c, d, and e is to recalibrate and step out.

   The subsystem may require a maximum of 3 seconds to execute these retry procedures.

2. System software can execute retries on command from the processor when predetermined errors are detected on the channel.

Appendix A. ASCII, EBCDIC, and Punched Card Codes

Table A—1. ASCII Character Codes

		Bit Positions 7, 6, 5							
		000	001	010	011	100	101	110	111
Bit Positions 4, 3, 2, 1	0000	NUL	DLE	SP	0	@	P	`	p
	0001	SOH	DC1	! ①	1	A	Q	a	q
	0010	STX	DC2	"	2	B	R	b	r
	0011	ETX	DC3	=	3	C	S	c	s
	0100	EOT	DC4	$	4	D	T	d	t
	0101	ENQ	NAK	%	5	E	U	e	u
	0110	ACK	SYN	&	6	F	V	f	v
	0111	BEL	ETB	'	7	G	W	g	w
	1000	BS	CAN	(	8	H	X	h	x
	1001	HT	EM	)	9	I	Y	i	y
	1010	LF	SUB	*	:	J	Z	j	z
	1011	VT	ESC	+	;	K	[	k	{
	1100	FF	FS	,	<	L	\	l	| ②
	1101	CR	GS	–	=	M	]	m	}
	1110	SO	RS	.	>	N	^ ①	n	~
	1111	SI	US	/	?	O	_	o	DEL

③ ④ ⑤

NOTES:

ASCII bits are numbered from the left in descending numerical sequence: 7 6 5 4 3 2 1

① The following optional graphics can be substituted in the character set:

¬ for ^

② For 64-character printers, the following substitution is made:

\ for |

③ Sixty-four printable character set.

④ Graphics available by use of the type 0768-02 printer which prints a 94-character set (DEL is not a graphic).

⑤ Ninety-four printable character set.

Table A—2. EBCDIC Character Codes

Bit Positions 4, 5, 6, 7	Bit Positions 0, 1, 2, 3															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	NUL	DLE	DS①		SP	&	–						¦④	¦④	\④	0
0001	SOH	DC1	SOS①				/		a④	j	~④		A	J		1
0010	STX	DC2	FS①	SYN					b	k	s		B	K	S	2
0011	ETX	DC3							c	l	t		C	L	T	3
0100									d	m	u		D	M	U	4
0101	HT		LF						e	n	v		E	N	V	5
0110		BS	ETB						f	o	w		F	O	W	6
0111	DEL		ESC	EOT					g	p	x		G	P	X	7
1000		CAN							h	q	y		H	Q	Y	8
1001		EM						·④	i	r	z		I	R	Z	9
1010					[	]	¦③	:								
1011	VT				.	$	,	=								
1100	FF	FS		DC4	<	*	%	@								
1101	CR	GS	ENQ	NAK	(	)	—	'								
1110	SO	RS	ACK		+	;	>	≠								
1111	SI	US	BEL	SUB	¦②	¬②	?	"								

NOTES:

EBCDIC bits are numbered from the left in ascending numerical order: 0 1 2 3 4 5 6 7

① DS, SOS, FS are the control characters for the EDIT instruction and have been assigned for ASCII mode processing so as not to conflict with the corresponding character position previously assigned in the EBCDIC chart. As these characters are not outside the range as defined in American National Standards Institute, X3.4—1968, they must not appear in external storage media, such as American National Standards Institute standard tapes. This presents no difficulty due to the nature of the EDIT instruction.

② The following optional graphics can be substituted in the character set:

¢, for [
! for]

③ For 64-character printers, the following substitution is made:

\ for |

④ The lowercase alphabet and indicated graphics are introduced by use of the 0768—02 printer, which prints a 94-character set.

Table A–3. Punched Card, ASCII, and EBCDIC Codes (Part 1 of 5)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
Letters						
A	A	12–1	41	65	C1	193
B	B	12–2	42	66	C2	194
C	C	12–3	43	67	C3	195
D	D	12–4	44	68	C4	196
E	E	12–5	45	69	C5	197
F	F	12–6	46	70	C6	198
G	G	12–7	47	71	C7	199
H	H	12–8	48	72	C8	200
I	I	12–9	49	73	C9	201
J	J	11–1	4A	74	D1	209
K	K	11–2	4B	75	D2	210
L	L	11–3	4C	76	D3	211
M	M	11–4	4D	77	D4	212
N	N	11–5	4E	78	D5	213
O	O	11–6	4F	79	D6	214
P	P	11–7	50	80	D7	215
Q	Q	11–8	51	81	D8	216
R	R	11–9	52	82	D9	217
S	S	0–2	53	83	E2	226
T	T	0–3	54	84	E3	227
U	U	0–4	55	85	E4	228
V	V	0–5	56	86	E5	229
W	W	0–6	57	87	E6	230
X	X	0–7	58	88	E7	231
Y	Y	0–8	59	89	E8	232
Z	Z	0–9	5A	90	E9	233
a	a	12–0–1	61	97	81	129
b	b	12–0–2	62	98	82	130
c	c	12–0–3	63	99	83	131

Table A–3. Punched Card, ASCII, and EBCDIC Codes (Part 2 of 5)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
d	d	12–0–4	64	100	84	132
e	e	12–0–5	65	101	85	133
f	f	12–0–6	66	102	86	134
g	g	12–0–7	67	103	87	135
h	h	12–0–8	68	104	88	136
i	i	12–0–9	69	105	89	137
j	j	12–11–1	6A	106	91	145
k	k	12–11–2	6B	107	92	146
l	l	12–11–3	6C	108	93	147
m	m	12–11–4	6D	109	94	148
n	n	12–11–5	6E	110	95	149
o	o	12–11–6	6F	111	96	150
p	p	12–11–7	70	112	97	151
q	q	12–11–8	71	113	98	152
r	r	12–11–9	72	114	99	153
s	s	11–0–2	73	115	A2	162
t	t	11–0–3	74	116	A3	163
u	u	11–0–4	75	117	A4	164
v	v	11–0–5	76	118	A5	165
w	w	11–0–6	77	119	A6	166
x	x	11–0–7	78	120	A7	167
y	y	11–0–8	79	121	A8	168
z	z	11–0–9	7A	122	A9	169
Numerals						
0	0	0	30	48	F0	240
1	1	1	31	49	F1	241
2	2	2	32	50	F2	242
3	3	3	33	51	F3	243
4	4	4	34	52	F4	244
5	5	5	35	53	F5	245
6	6	6	36	54	F6	246

Table A–3. Punched Card, ASCII, and EBCDIC Codes (Part 3 of 5)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
7	7	7	37	55	F7	247
8	8	8	38	56	F8	248
9	9	9	39	57	F9	249
Symbols						
Exclamation point	!	12–8–7	21	33	4F	79
Quotation mark, dieresis	"	8–7	22	34	7F	127
Number sign, pound sign	#	8–3	23	35	7B	123
Dollar sign	$	11–8–3	24	36	5B	91
Percent sign	%	0–8–4	25	37	6C	108
Ampersand	&	12	26	38	50	80
Apostrophe, acute accent	'	8–5	27	39	7D	125
Opening parenthesis	(	12–8–5	28	40	4D	77
Closing parenthesis	)	11–8–5	29	41	5D	93
Asterisk	*	11–8–4	2A	42	5C	92
Plus sign	+	12–8–6	2B	43	4E	78
Comma, cedilla	,	0–8–3	2C	44	6B	107
Minus sign, hyphen	–	11	2D	45	60	96
Period, decimal point	.	12–8–3	2E	46	4B	75
Slash, virgule, solidus	/	0–1	2F	47	61	97
Colon	:	8–2	3A	58	7A	122
Semicolon	;	11–8–6	3B	59	5E	94
Less than	<	12–8–4	3C	60	4C	76
Equal sign	=	8–6	3D	61	7E	126
Greater than	>	0–8–6	3E	62	6E	110
Question mark	?	0–8–7	3F	63	6F	111
Commercial at symbol	@	8–4	40	64	7C	124
Opening bracket	[	12–8–2	5B	91	4A	74
Closing bracket	]	11–8–2	5D	93	5A	90
Reverse slash	\	0–8–2	5C	92	E0	224
Circumflex	^	11–8–7	5E	94	5F	95

Table A–3. Punched Card, ASCII, and EBCDIC Codes (Part 4 of 5)

Character	Printed Symbol	Card Punches	ASCII		EBCDIC	
			Hexadecimal	Decimal	Hexadecimal	Decimal
Underline	—	0–8–5	5F	95	6D	109
Grave accent	`	8–1	60	96	79	121
Opening brace	{	12–0	7B	123	C0	192
Closing brace	}	11–0	7D	125	D0	208
Vertical line	|	12–11	7C	124	6A	106
Overline, tilde	~	11–0–1	7E	126	A1	161

Character	Card Punches	ASCII		EBCDIC	
		Hexadecimal	Decimal	Hexadecimal	Decimal
Nonprintable Characters					
ACK (Acknowledge)	0–9–8–6	06	6	2E	46
BEL (Bell)	0–9–8–7	07	7	2F	47
BS (Backspace)	11–9–6	08	8	16	22
CAN (Cancel)	11–9–8	18	24	18	24
CR (Carriage return)	12–9–8–5	0D	13	0D	13
DC1 (Device control 1)	11–9–1	11	17	11	17
DC2 (Device control 2)	11–9–2	12	18	12	18
DC3 (Device control 3)	11–9–3	13	19	13	19
DC4 (Device control 4)	9–8–4	14	20	3C	60
DEL (Delete)	12–9–7	7F	127	07	7
DLE (Data link escape)	12–11–9–8–1	10	16	10	16
DS (Digit select)	11–0–9–8–1	80	128	20	32
EM (End of medium)	11–9–8–1	19	25	19	25
ENQ (Enquiry)	0–9–8–5	05	5	2D	45
EOT (End of transmission)	9–7	04	4	37	55
ESC (Escape)	0–9–7	1B	27	27	39
ETB (End of transmission block)	0–9–6	17	23	26	38
ETX (End of text)	12–9–3	03	3	03	3
FF (Form feed)	12–9–8–4	0C	12	0C	12
FS (File separator)	11–9–8–4	1C	28	1C	28

Table A–3. Punched Card, ASCII, and EBCDIC Codes (Part 5 of 5)

Character	Card Punches	ASCII		EBCDIC	
		Hexadecimal	Decimal	Hexadecimal	Decimal
FS (Field separator)	0–9–2	82	130	22	34
GS (Group separator)	11–9–8–5	1D	29	1D	29
HT (Horizontal tabulation)	12–9–5	09	9	05	5
LF (Line feed)	0–9–5	0A	10	25	37
NAK (Negative acknowledge)	9–8–5	15	21	3D	61
NUL (Null)	12–0–9–8–1	00	0	00	0
RS (Record separator)	11–9–8–6	1E	30	1E	30
SI (Shift in)	12–9–8–7	0F	15	0F	15
SO (Shift out)	12–9–8–6	0E	14	0E	14
SOH (Start of heading)	12–9–1	01	1	01	1
SOS (Significance start)	0–9–1	81	129	21	33
SP (Space)		20	32	40	64
STX (Start of text)	12–9–2	02	2	02	2
SUB (Substitute)	9–8–7	1A	26	3F	63
SYN (Synchronous idle)	9–2	16	22	32	50
US (Unit separator)	11–9–8–7	1F	31	1F	31
VT (Vertical tabulation)	12–9–8–3	0B	11	0B	11

Appendix B. Print Cartridge Character Sets

Tables B—1 through B—21 list the character symbols appearing in each optional feature print cartridge used on the 0773 or 0778 printer. The characters must be loaded by program into the load code buffer in the sequence they appear in the tables. The programmer assigns a separate code from sets such as ASCII, EBCDIC, or Fieldata to each different character on the print band.

The tables also provide useful information on array size, which can be applied to estimating minimum print rates (7.2.4.3). Additional information on the print cartridge is presented in Table 7—2 and Table 7—3.

Print character symbols listed in the tables are for information purposes and are not necessarily the same shape or form as those on the print bands.

Table B—18 lists the character sequence for 85-character feature print band requiring expanded load code buffer feature. A total of 256 characters plus the space code and band identification must be loaded. Hexadecimal codes are not assigned since these are assigned by the customer.

Table B–1. 48-Character Standard Business Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	@	Commercial At	1
40	#	Number Sign	1
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus	1
44	'	Apostrophe	1
45	*	Asterisk	1
46	%	Percent Sign	1
47	&	Ampersand	1
48	.	Period	1
		Array Size	**48**

Table B–2. 48-Character Standard Scientific Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	'	Apostrophe	2
40	=	Equal Sign	2
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus Sign	1
44	)	Right Parenthesis	2
45	*	Asterisk	1
46	(	Left Parenthesis	2
47	&	Ampersand	1
48	.	Period	1
		Array Size	**48**

Table B—3. 64-Character Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	2
37	–	Hyphen (Minus)	1
38	/	Slash (Solidus)	1
39	@	Commercial At	1
40	#	Number Sign	1
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus	1
44	'	Apostrophe	1
45	*	Asterisk	1
46	%	Percent Sign	1
47	&	Ampersand	1
48	.	Period	1
49	:	Colon	1
50	|	Vertical Bar	1
51	"	Quotation	1
52	!	Exclamation	1
53	?	Question	1
54	_	Underline	1
55	(	Left Parenthesis	1
56	=	Equal Sign	1
57	¬	Logical NOT	1
58	;	Semicolon	1
59	\	Reverse Slash	1
60	¢	Cent Sign	1
61	)	Right Parenthesis	1
62	>	Greater Than	1
63	<	Less Than	1
64	0	Numeric Zero	2
		Array Size	**64**

Table B—4. 48-Character Business Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	@	Commercial At	1
40	#	Number Sign	1
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus	1
44	<	Less Than	1
45	*	Asterisk	1
46	%	Percent Sign	1
47	&	Ampersand	1
48	.	Period	1
		Array Size	**48**

Table B—5. United Kingdom Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	@	Commercial At	1
40	£	Pound Sign	1
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus	1
44	'	Apostrophe	1
45	*	Asterisk	1
46	%	Percent Sign	1
47	&	Ampersand	1
48	.	Period	1
		Array Size	**48**

Table B—6. Denmark — Norway Print Cartridge

Symbol Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	Ø	Uppercase O with Slant	1
40	Å	Uppercase A with Circle	1
41	Ü	Uppercase U with Diaeresis	1
42	,	Comma	1
43	+	Plus	1
44	É	Uppercase E with Acute Accent	1
45	*	Asterisk	1
46	Æ	Uppercase AE Diphthong	1
47	&	Ampersand	1
48	.	Period	1
		Array Size	**48**

Table B—7. Finland—Sweden Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	Ö	Uppercase O with Diaeresis	1
40	Å	Uppercase A with Circle	1
41	Ü	Uppercase U with Diaeresis	1
42	,	Comma	1
43	+	Plus	1
44	É	Uppercase E with Acute Accent	1
45	*	Asterisk	1
46	Ä	Uppercase A with Diaeresis	1
47	&	Ampersand	1
48	.	Period	1
		Array Size	**64**

Table B—8. Denmark—Norway 63-Character Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols Per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	2
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	Ø	Uppercase O with Slant	1
40	#	Number Sign	1
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus Sign	1
44	'	Apostrophe	1
45	*	Asterisk	1
46	%	Percent Sign	1
47	&	Ampersand	1
48	.	Period	1
49	:	Colon	1
50	Å	Uppercase A with Circle	1
51	"	Quotation	1
52	!	Exclamation	1
53	?	Question	1
54	_	Underline	1
55	(	Left Parenthesis	1
56	=	Equal Sign	1
57	Ü	Uppercase U with Diaeresis	1
58	;	Semicolon	1
59	É	Uppercase E with Acute Accent	1
60	Æ	Uppercase AE Diphthong	1
61	)	Right Parenthesis	1
62	>	Greater Than	1
63	<	Less Than	1
64	0	Zero	2
		Array Size	**64**

Table B–9. Finland–Sweden 63-Character Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols Per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	2
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	Ö	Uppercase O with Diaeresis	1
40	#	Number Sign	1
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus	1
44	'	Apostrophe	1
45	*	Asterisk	1
46	%	Percent	1
47	&	Ampersand	1
48	.	Period	1
49	:	Colon	1
50	Å	Uppercase A with Circle	1
51	"	Quote	1
52	!	Exclamation	1
53	?	Question	1
54	—	Discontinuous Underline	1
55	(	Left Parenthesis	1
56	=	Equal Sign	1
57	Ü	Uppercase U with Diaeresis	1
58	;	Semicolon	1
59	É	Uppercase E with Acute Accent	1
60	Ä	Uppercase A with Diaeresis	1
61	)	Right Parenthesis	1
62	>	Greater Than	1
63	<	Less Than	1
64	0	Numeric Zero	2
		Array Size	**64**

Table B—10. Japan—Katakana 63-Character Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	ト	Katakana Capital Letter	1
2	ヤ	Katakana Capital Letter	1
3	シ	Katakana Capital Letter	1
4	ア	Katakana Capital Letter	1
5	キ	Katakana Capital Letter	1
6	チ	Katakana Capital Letter	1
7	オ	Katakana Capital Letter	1
8	セ	Katakana Capital Letter	1
9	エ	Katakana Capital Letter	1
10	フ	Katakana Capital Letter	1
11	ﾟ	Katakana Capital Letter	1
12	ワ	Katakana Capital Letter	1
13	ノ	Katakana Capital Letter	1
14	リ	Katakana Capital Letter	1
15	ラ	Katakana Capital Letter	1
16	ニ	Katakana Capital Letter	1
17	ナ	Katakana Capital Letter	1
18	ヨ	Katakana Capital Letter	1
19	ン	Katakana Capital Letter	1
20	カ	Katakana Capital Letter	1
21	ス	Katakana Capital Letter	1
22	ウ	Katakana Capital Letter	1
23	イ	Katakana Capital Letter	1
24	ハ	Katakana Capital Letter	1
25	マ	Katakana Capital Letter	1
26	タ	Katakana Capital Letter	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	3
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	レ	Katakana Capital Letter	1
40	ケ	Katakana Capital Letter	1
41	¥	Yen Sign	1
42	,	Comma	1
43	ツ	Katakana Capital Letter	1
44	ミ	Katakana Capital Letter	1
45	*	Asterisk	1
46	メ	Katakana Capital Letter	1
47	テ	Katakana Capital Letter	1
48	.	Period	1
49	モ	Katakana Capital Letter	1
50	ヌ	Katakana Capital Letter	1
51	ホ	Katakana Capital Letter	1
52	ク	Katakana Capital Letter	1
53	ソ	Katakana Capital Letter	1
54	ロ	Katakana Capital Letter	1
55	ネ	Katakana Capital Letter	1
56	サ	Katakana Capital Letter	1
57	ヒ	Katakana Capital Letter	1
58	ユ	Katakana Capital Letter	1
59	ヘ	Katakana Capital Letter	1
60	ル	Katakana Capital Letter	1
61	ム	Katakana Capital Letter	1
62	0	Numeric Zero	3
63	コ	Katakana Capital Letter	1
64	0	Numeric Zero	3
		Array Size	**64**

Table B—11. 48/16 Alphanumeric Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase P	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	0	Numeric Zero	3
18	9	Numeric Nine	2
19	8	Numeric Eight	2
20	7	Numeric Seven	2
21	6	Numeric Six	2
22	5	Numeric Five	2
23	4	Numeric Four	2
24	3	Numeric Three	2
25	2	Numeric Two	2
26	1	Numeric One	2
27	,	Comma	2
28	<	Less Than	1
29	*	Asterisk	2
30	–	Hyphen (Minus)	2
31	.	Period	2
32	J	Uppercase J	1

Loading Sequence	Symbol	Symbol Description	Symbols per Array
33	I	Uppercase I	1
34	H	Uppercase H	1
35	G	Uppercase G	1
36	F	Uppercase F	1
37	E	Uppercase E	1
38	D	Uppercase D	1
39	C	Uppercase C	1
40	B	Uppercase B	1
41	A	Uppercase A	1
42	0	Numeric Zero	3
43	@	Commercial At	1
44	#	Number Sign	1
45	$	Dollar Sign	1
46	'	Apostrophe	1
47	%	Percent Sign	1
48	&	Ampersand	1
49	9	Numeric Nine	2
50	8	Numeric Eight	2
51	7	Numeric Seven	2
52	6	Numeric Six	2
53	5	Numeric Five	2
54	4	Numeric Four	2
55	3	Numeric Three	2
56	2	Numeric Two	2
57	1	Numeric One	2
58	/	Slant (Solidus)	1
59	,	Comma	2
60	+	Plus	1
61	*	Asterisk	2
62	0	Numeric Zero	3
63	–	Hyphen (Minus)	2
64	.	Period	2
		Array Size	**64**

Table B—12. Universal OCR H—14 Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	0	Numeric Zero	2
18	9	Numeric Nine	2
19	8	Numeric Eight	2
20	7	Numeric Seven	2
21	6	Numeric Six	2
22	5	Numeric Five	2
23	4	Numeric Four	2
24	3	Numeric Three	2
25	2	Numeric Two	2
26	1	Numeric One	2
27	,	Comma	2
28	<	Less Than	1
29	*	Asterisk	2
30	–	Hyphen (Minus)	1
31	.	Period	2
32	J	Uppercase J	1
33	I	Uppercase I	1
34	H	Uppercase H	1
35	G	Uppercase G	1
36	F	Uppercase F	1
37	E	Uppercase E	1
38	D	Uppercase D	1
39	C	Uppercase C	1
40	B	Uppercase B	1
41	A	Uppercase A	1
42	0	Numeric Zero	3
43	@	Commercial At	1
44	#	Number Sign	1
45	$	Dollar Sign	1
46	'	Apostrophe	1
47	%	Percent Sign	1
48	&	Ampersand	1
49	9	Numeric Nine	2
50	8	Numeric Eight	2
51	7	Numeric Seven	2
52	6	Numeric Six	2
53	5	Numeric Five	2
54	4	Numeric Four	2
55	3	Numeric Three	2
56	2	Numeric Two	2
57	1	Numeric One	2
58	/	Slant (Solidus)	1
59	,	Comma	2
60	+	Plus	1
61	*	Asterisk	2
62	0	Numeric Zero	3
63	\	Reverse Slant (Reverse Solidus)	1
64	.	Period	2
		Array Size	**64**

Table B—13. Universal OCR—B (ISO) Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	0	Numeric Zero	2
18	9	Numeric Nine	2
19	8	Numeric Eight	2
20	7	Numeric Seven	2
21	6	Numeric Six	2
22	5	Numeric Five	2
23	4	Numeric Four	2
24	3	Numeric Three	2
25	2	Numeric Two	2
26	1	Numeric One	2
27	,	Comma	2
28	<	Less Than	1
29	*	Asterisk	2
30	–	Minus	1
31	.	Period	2
32	J	Uppercase J	1
33	I	Uppercase I	1
34	H	Uppercase H	1
35	G	Uppercase G	1
36	F	Uppercase F	1
37	E	Uppercase E	1
38	D	Uppercase D	1
39	C	Uppercase C	1
40	B	Uppercase B	1
41	A	Uppercase A	1
42	0	Numeric Zero	3
43	@	Commercial At	1
44	#	Number Sign	1
45	$	Dollar Sign	1
46	'	Apostrophe	1
47	%	Percent Sign	1
48	&	Ampersand	1
49	9	Numeric Nine	2
50	8	Numeric Eight	2
51	7	Numeric Seven	2
52	6	Numeric Six	2
53	5	Numeric Five	2
54	4	Numeric Four	2
55	3	Numeric Three	2
56	2	Numeric Two	2
57	1	Numeric One	2
58	/	Slant (Solidus)	1
59	,	Comma	2
60	+	Plus	1
61	*	Asterisk	2
62	0	Numeric Zero	3
63	>	Greater Than	1
64	.	Period	2
		Array Size	**64**

Table B—14. Universal OCR—B (ECMA—11) Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	0	Numeric Zero	2
18	9	Numeric Nine	2
19	8	Numeric Eight	2
20	7	Numeric Seven	2
21	6	Numeric Six	2
22	5	Numeric Five	2
23	4	Numeric Four	2
24	3	Numeric Three	2
25	2	Numeric Two	2
26	1	Numeric One	2
27	,	Comma	2
28	<	Less Than	1
29	*	Asterisk	2
30	–	Minus	1
31	.	Period	2
32	J	Uppercase J	1
33	I	Uppercase I	1
34	H	Uppercase H	1
35	G	Uppercase G	1
36	F	Uppercase F	1
37	E	Uppercase E	1
38	D	Uppercase D	1
39	C	Uppercase C	1
40	B	Uppercase B	1
41	A	Uppercase A	1
42	0	Numeric Zero	3
43	@	Commercial At	1
44	#	Number Sign	1
45	$	Dollar Sign	1
46	'	Apostrophe	1
47	%	Percent Sign	1
48	&	Ampersand	1
49	9	Numeric Nine	2
50	8	Numeric Eight	2
51	7	Numeric Seven	2
52	6	Numeric Six	2
53	5	Numeric Five	2
54	4	Numeric Four	2
55	3	Numeric Three	2
56	2	Numeric Two	2
57	1	Numeric One	2
58	/	Slant (Solidus)	1
59	,	Comma	2
60	+	Plus	1
61	*	Asterisk	2
62	0	Numeric Zero	3
63	>	Greater Than	1
64	.	Period	2
		Array Size	**64**

Table B—15. Universal OCR—A (ECMA—11) Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	0	Numeric Zero	2
18	9	Numeric Nine	2
19	8	Numeric Eight	2
20	7	Numeric Seven	2
21	6	Numeric Six	2
22	5	Numeric Five	2
23	4	Numeric Four	2
24	3	Numeric Three	2
25	2	Numeric Two	2
26	1	Numeric One	2
27	,	Comma	2
28	<	Less Than	1
29	*	Asterisk	2
30	–	Minus	1
31	.	Period	2
32	J	Uppercase J	1
33	I	Uppercase I	1
34	H	Uppercase H	1
35	G	Uppercase G	1
36	F	Uppercase F	1
37	E	Uppercase E	1
38	D	Uppercase D	1
39	C	Uppercase C	1
40	B	Uppercase B	1
41	A	Uppercase A	1
42	0	Numeric Zero	3
43	@	Commercial At	1
44	#	Number Sign	1
45	$	Dollar Sign	1
46	'	Apostrophe	1
47	%	Percent Sign	1
48	&	Ampersand	1
49	9	Numeric Nine	2
50	8	Numeric Eight	2
51	7	Numeric Seven	2
52	6	Numeric Six	2
53	5	Numeric Five	2
54	4	Numeric Four	2
55	3	Numeric Three	2
56	2	Numeric Two	2
57	1	Numeric One	2
58	/	Slant (Solidus)	1
59	,	Comma	2
60	+	Plus	1
61	⅄	Fork	2
62	0	Numeric Zero	3
63	⊐	Hook	1
64	⊐	Chair	2
		Array Size	**64**

Table B—16. Portuguese Print Catridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	/	Slant (Solidus)	1
39	§	Section	1
40	Õ	Uppercase O with Tilde	1
41	$	Dollar Sign	1
42	,	Comma	1
43	+	Plus	1
44	ç	Lowercase C with Cedilla	1
45	*	Asterisk	1
46	%	Percent Sign	1
47	Ã	Uppercase A with Tilde	1
48	.	Period	1
		Array Size	**48**

Table B—17. Spanish Print Cartridge

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	Z	Uppercase Z	1
2	Y	Uppercase Y	1
3	X	Uppercase X	1
4	W	Uppercase W	1
5	V	Uppercase V	1
6	U	Uppercase U	1
7	T	Uppercase T	1
8	S	Uppercase S	1
9	R	Uppercase R	1
10	Q	Uppercase Q	1
11	P	Uppercase P	1
12	O	Uppercase O	1
13	N	Uppercase N	1
14	M	Uppercase M	1
15	L	Uppercase L	1
16	K	Uppercase K	1
17	J	Uppercase J	1
18	I	Uppercase I	1
19	H	Uppercase H	1
20	G	Uppercase G	1
21	F	Uppercase F	1
22	E	Uppercase E	1
23	D	Uppercase D	1
24	C	Uppercase C	1
25	B	Uppercase B	1
26	A	Uppercase A	1
27	9	Numeric Nine	1
28	8	Numeric Eight	1
29	7	Numeric Seven	1
30	6	Numeric Six	1
31	5	Numeric Five	1
32	4	Numeric Four	1
33	3	Numeric Three	1
34	2	Numeric Two	1
35	1	Numeric One	1
36	0	Numeric Zero	1
37	–	Hyphen (Minus)	1
38	Ñ	Uppercase N with Tilde	1
39	@	Commercial At	1
40	#	Number Sign	1
41	Pt	Pt Sign	1
42	,	Comma	1
43	+	Plus	1
44	<	Less Than	1
45	*	Asterisk	1
46	%	Percent Sign	1
47	&	Ampersand	1
48	.	Period	1
		Array Size	**48**

Table B—18. 85-Character Abbreviated ASCII Print Cartridge (Part 1 of 4)

Loading Sequence	Symbol	Symbol Description	Symbols Per Array	Loading Sequence	Symbol	Symbol Description	Symbols Per Array
1	c	Lowercase c	3	33	O	Uppercase O	3
2	b	Lowercase b	3	34	N	Uppercase N	3
3	a	Lowercase a	3	35	M	Uppercase M	3
4	[	Left Square Bracket	2	36	L	Uppercase L	3
5	]	Right Square Bracket	2	37	K	Uppercase K	3
6	\	Reverse Slant (Reverse Solidus)	2	38	J	Uppercase J	3
7	^	Circumflex	2	39	I	Uppercase I	3
8	_	Underline	2	40	H	Uppercase H	3
9	:	Colon	2	41	G	Uppercase G	3
10	;	Semicolon	2	42	F	Uppercase F	3
11	=	Equal Sign	2	43	E	Uppercase E	3
12	>	Greater Than	2	44	D	Uppercase D	3
13	?	Question	2	45	C	Uppercase C	3
14	0	Numeric Zero	5	46	B	Uppercase B	3
15	,	Comma	3	47	A	Uppercase A	3
16	+	Plus	3	48	9	Numeric Nine	3
17	<	Less Than	3	49	8	Numeric Eight	3
18	*	Asterisk	3	50	7	Numeric Seven	3
19	%	Percent Sign	3	51	6	Numeric Six	3
20	&	Ampersand	3	52	5	Numeric Five	3
21	.	Period	3	53	4	Numeric Four	3
22	Z	Uppercase Z	3	54	3	Numeric Three	3
23	Y	Uppercase Y	3	55	2	Numeric Two	3
24	X	Uppercase X	3	56	1	Numeric One	3
25	W	Uppercase W	3	57	0	Numeric Zero	5
26	V	Uppercase V	3	58	–	Hyphen (Minus)	3
27	U	Uppercase U	3	59	/	Slant (Solidus)	3
28	T	Uppercase T	3	60	@	Commercial At	3
29	S	Uppercase S	3	61	#	Number Sign	3
30	R	Uppercase R	3	62	$	Dollar Sign	3
31	Q	Uppercase Q	3	63	z	Lowercase z	3
32	P	Uppercase P	3	64	y	Lowercase y	3

Table B—18. 85-Character Abbreviated ASCII Print Cartridge (Part 2 of 4)

Loading Sequence	Symbol	Symbol Description	Symbols Per Array
65	x	Lowercase x	3
66	w	Lowercase w	3
67	v	Lowercase v	3
68	u	Lowercase u	3
69	t	Lowercase t	3
70	s	Lowercase s	3
71	r	Lowercase r	3
72	q	Lowercase q	3
73	p	Lowercase p	3
74	o	Lowercase o	3
75	n	Lowercase n	3
76	m	Lowercase m	3
77	l	Lowercase l	3
78	k	Lowercase k	3
79	j	Lowercase j	3
80	i	Lowercase i	3
81	h	Lowercase h	3
82	g	Lowercase g	3
83	f	Lowercase f	3
84	e	Lowercase e	3
85	d	Lowercase d	3
86	c	Lowercase c	3
87	b	Lowercase b	3
88	a	Lowercase a	3
89	!	Exclamation	2
90	"	Quotation	2
91	'	Apostrophe	2
92	(	Left Parenthesis	2
93	)	Right Parenthesis	2
94	:	Colon	2
95	;	Semicolon	2
96	=	Equal Sign	2
97	>	Greater Than	2
98	?	Question	2
99	0	Number Zero	5
100	,	Comma	3
101	+	Plus	3
102	<	Less Than	3
103	*	Asterisk	3
104	%	Percent Sign	3
105	&	Ampersand	3
106	.	Period	3
107	Z	Uppercase Z	3
108	Y	Uppercase Y	3
109	X	Uppercase X	3
110	W	Uppercase W	3
111	V	Uppercase V	3
112	U	Uppercase U	3
113	T	Uppercase T	3
114	S	Uppercase S	3
115	R	Uppercase R	3
116	Q	Uppercase Q	3
117	P	Uppercase P	3
118	O	Uppercase O	3
119	N	Uppercase N	3
120	M	Uppercase M	3
121	L	Uppercase L	3
122	K	Uppercase K	3
123	J	Uppercase J	3
124	I	Uppercase I	3
125	H	Uppercase H	3
126	G	Uppercase G	3
127	F	Uppercase F	3
128	E	Uppercase E	3

Table B—18. 85-Character Abbreviated ASCII Print Cartridge (Part 3 of 4)

Loading Sequence	Symbol	Symbol Description	Symbols Per Array
129	D	Uppercase D	3
130	C	Uppercase C	3
131	B	Uppercase B	3
132	A	Uppercase A	3
133	9	Numeric Nine	3
134	8	Numeric Eight	3
135	7	Numeric Seven	3
136	6	Numeric Six	3
137	5	Numeric Five	3
138	4	Numeric Four	3
139	3	Numeric Three	3
140	2	Numeric Two	3
141	1	Numeric One	3
142	0	Numeric Zero	3
143	–	Hyphen (Minus)	3
144	/	Slant (Solidus)	3
145	@	Commercial At	3
146	#	Number Sign	3
147	$	Dollar Sign	3
148	z	Lowercase z	3
149	y	Lowercase y	3
150	x	Lowercase x	3
151	w	Lowercase w	3
152	v	Lowercase v	3
153	u	Lowercase u	3
154	t	Lowercase t	3
155	s	Lowercase s	3
156	r	Lowercase r	3
157	q	Lowercase q	3
158	p	Lowercase p	3
159	o	Lowercase o	3
160	n	Lowercase n	3
161	m	Lowercase m	3
162	l	Lowercase l	3
163	k	Lowercase k	3
164	j	Lowercase j	3
165	i	Lowercase i	3
166	h	Lowercase h	3
167	g	Lowercase g	3
168	f	Lowercase f	3
169	e	Lowercase e	3
170	d	Lowercase d	3
171	c	Lowercase c	3
172	b	Lowercase b	3
173	a	Lowercase a	3
174	!	Exclamation	2
175	"	Quotation	2
176	'	Apostrophe	2
177	(	Left Parenthesis	2
178	)	Right Parenthesis	2
179	[	Left Square Bracket	2
180	]	Right Square Bracket	2
181	\	Reverse Slant (Reverse Solidus)	2
182	^	Circumflex	2
183	_	Underline	2
184	¤	International Currency Sign	1
185	,	Comma	3
186	+	Plus	3
187	<	Less Than	3
188	*	Asterisk	3
189	%	Percent Sign	3
190	&	Ampersand	3
191	.	Period	3
192	£	Pound Sterling Sign	1

Table B—18. 85-Character Abbreviated ASCII Print Cartridge (Part 4 of 4)

Loading Sequence	Symbol	Symbol Description	Symbols Per Array
193	Z	Uppercase Z	3
194	Y	Uppercase Y	3
195	X	Uppercase X	3
196	W	Uppercase W	3
197	V	Uppercase V	3
198	U	Uppercase U	3
199	T	Uppercase T	3
200	S	Uppercase S	3
201	R	Uppercase R	3
202	Q	Uppercase Q	3
203	P	Uppercase P	3
204	O	Uppercase O	3
205	N	Uppercase N	3
206	M	Uppercase M	3
207	L	Uppercase L	3
208	K	Uppercase K	3
209	J	Uppercase J	3
210	I	Uppercase I	3
211	H	Uppercase H	3
212	G	Uppercase G	3
213	F	Uppercase F	3
214	E	Uppercase E	3
215	D	Uppercase D	3
216	C	Uppercase C	3
217	B	Uppercase B	3
218	A	Uppercase A	3
219	9	Numeric Nine	3
220	8	Numeric Eight	3
221	7	Numeric Seven	3
222	6	Numeric Six	3
223	5	Numeric Five	3
224	4	Numeric Four	3
225	3	Numeric Three	3
226	2	Numeric Two	3
227	1	Numeric One	3
228	0	Numeric Zero	5
229	–	Hyphen (Minus)	3
230	/	Slant (Solidus)	3
231	@	Commercial At	3
232	#	Number Sign	3
233	$	Dollar Sign	3
234	z	Lowercase z	3
235	y	Lowercase y	3
236	x	Lowercase x	3
237	w	Lowercase w	3
238	v	Lowercase v	3
239	u	Lowercase u	3
240	t	Lowercase t	3
241	s	Lowercase s	3
242	r	Lowercase r	3
243	q	Lowercase q	3
244	p	Lowercase p	3
245	o	Lowercase o	3
246	n	Lowercase n	3
247	m	Lowercase m	3
248	l	Lowercase l	3
249	k	Lowercase k	3
250	j	Lowercase j	3
251	i	Lowercase i	3
252	h	Lowercase h	3
253	g	Lowercase g	3
254	f	Lowercase f	3
255	e	Lowercase e	3
256	d	Lowercase d	3
		Array Size	256

Table B—19. Full ASCII Print Cartridge (Part 1 of 2)

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	f	Lowercase f	1
2	e	Lowercase e	1
3	d	Lowercase d	1
4	c	Lowercase c	1
5	b	Lowercase b	1
6	a	Lowercase a	1
7	9	Numeric Nine	3
8	8	Numeric Eight	3
9	7	Numeric Seven	3
10	6	Numeric Six	3
11	5	Numeric Five	3
12	4	Numeric Four	3
13	3	Numeric Three	3
14	2	Numeric Two	3
15	1	Numeric One	3
16	,	Comma	3
17	'	Apostrophe	1
18	*	Asterisk	3
19	–	Hyphen (Minus)	3
20	/	Slant (Solidus)	3
21	&	Ampersand	1
22	.	Period	3
23	!	Exclamation	1
24	|	Vertical Line	1
25	0	Numeric Zero	4
26	"	Quotation	1
27	#	Number Sign	1
28	$	Dollar Sign	1
29	%	Percent Sign	1
30	(	Left Parenthesis	1
31	)	Right Parenthesis	1
32	:	Colon	1
33	;	Semicolon	1
34	=	Equal Sign	1
35	>	Greater Sign	1
36	?	Question	1
37	@	Commercial At	1
38	[	Left Square Bracket	1
39	+	Plus	2
40	]	Right Square Bracket	1
41	¤	International Currency Sign	1
42	^	Circumflex	1
43	¬	Logical Not	1
44	_	Discontinuous Underline	1
45	`	Grave Accent	1
46	~	Tilde (Overline)	1
47	9	Numeric Nine	3
48	8	Numeric Eight	3
49	7	Numeric Seven	3
50	6	Numeric Six	3
51	5	Numeric Five	3
52	4	Numeric Four	3
53	3	Numeric Three	3
54	2	Numeric Two	3
55	1	Numeric One	3
56	0	Numeric Zero	4
57	\	Reverse Slant (Reverse Solidus)	1
58	,	Comma	3
59	/	Slant (Solidus)	3
60	{	Left Brace Bracket	1
61	*	Asterisk	3
62	–	Hyphen (Minus)	3
63	}	Right Brace Bracket	1
64	.	Period	3

Table B—19. Full ASCII Print Cartridge (Part 2 of 2)

Loading Sequence	Symbol	Symbol Description	Symbols per Array
65	Z	Uppercase Z	1
66	Y	Uppercase Y	1
67	X	Uppercase X	1
68	W	Uppercase W	1
69	V	Uppercase V	1
70	U	Uppercase U	1
71	T	Uppercase T	1
72	S	Uppercase S	1
73	R	Uppercase R	1
74	Q	Uppercase Q	1
75	P	Uppercase P	1
76	O	Uppercase O	1
77	N	Uppercase N	1
78	M	Uppercase M	1
79	L	Uppercase L	1
80	K	Uppercase K	1
81	J	Uppercase J	1
82	I	Uppercase I	1
83	H	Uppercase H	1
84	G	Uppercase G	1
85	F	Uppercase F	1
86	E	Uppercase E	1
87	D	Uppercase D	1
88	C	Uppercase C	1
89	B	Uppercase B	1
90	A	Uppercase A	1
91	0	Numeric Zero	3
92	9	Numeric Nine	3
93	8	Numeric Eight	3
94	7	Numeric Seven	3
95	6	Numeric Six	3
96	5	Numeric Five	3
97	4	Numeric Four	3
98	3	Numeric Three	3
99	2	Numeric Two	3
100	1	Numeric One	3
101	,	Comma	3
102	+	Plus	2
103	<	Less Than	1
104	*	Asterisk	3
105	–	Hyphen (Minus)	3
106	/	Slant (Solidus)	3
107	.	Period	3
108	z	Lowercase z	1
109	y	Lowercase y	1
110	x	Lowercase x	1
111	w	Lowercase w	1
112	v	Lowercase v	1
113	u	Lowercase u	1
114	t	Lowercase t	1
115	s	Lowercase s	1
116	r	Lowercase r	1
117	q	Lowercase q	1
118	p	Lowercase p	1
119	o	Lowercase o	1
120	n	Lowercase n	1
121	0	Numeric Zero	4
122	m	Lowercase m	1
123	l	Lowercase l	1
124	k	Lowercase k	1
125	j	Lowercase j	1
126	i	Lowercase i	1
127	h	Lowercase h	1
128	g	Lowercase g	1
		Array Size	**128**

Table B—20. 96/16 Finland—Sweden Print Cartridge (Part 1 of 2)

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	e	Lowercase e	1
2	d	Lowercase d	1
3	c	Lowercase c	1
4	b	Lowercase b	1
5	a	Lowercase a	1
6	¤	International Currency Symbol	1
7	9	Numeric Nine	2
8	8	Numeric Eight	2
9	7	Numeric Seven	3
10	6	Numeric Six	3
11	5	Numeric Five	3
12	4	Numeric Four	3
13	3	Numeric Three	3
14	2	Numeric Two	3
15	1	Numeric One	3
16	*	Asterisk	3
17	+	Plus	3
18	,	Comma	3
19	–	Hyphen (Minus)	3
20	.	Period	3
21	/	Slant (Solidus)	3
22	?	Question	1
23	!	Exclamation	1
24	"	Quote	1
25	=	Equals Sign	1
26	$	Dollar Sign	1
27	%	Percent	1
28	&	Ampersand	1
29	'	Apostrophe	1
30	(	Left Parenthesis	1
31	)	Right Parenthesis	1
32	0	Numeric Zero	4
33	>	Greater Than	1
34	=	Equal Sign	2
35	<	Less Than	1
36	;	Semicolon	1
37	:	Colon	1
38	Ü	Uppercase U with Diaeresis	1
39	Å	Uppercase A with Circle	1
40	Ö	Uppercase O with Diaeresis	1
41	Ä	Uppercase A with Diaeresis	1
42	É	Uppercase E with Acute Accent	1
43	ü	Lowercase u with Diaeresis	1
44	ä	Lowercase a with Diaeresis	1
45	ö	Lowercase o with Diaeresis	1
46	ä	Lowercase a with Diaeresis	1
47	è	Lowercase e with Grave Accent	1
48	_	Discontinuous Underline	1
49	9	Numeric Nine	3
50	8	Numeric Eight	3
51	7	Numeric Seven	3
52	6	Numeric Six	3
53	5	Numeric Five	3
54	4	Numeric Four	3
55	3	Numeric Three	3
56	2	Numeric Two	3
57	1	Numeric One	3
58	*	Asterisk	3
59	+	Plus	3
60	,	Comma	3
61	–	Hyphen (Minus)	3
62	.	Period	3
63	/	Slant (Solidus)	3
64	0	Numeric Zero	4

Table B—20. 96/16 Finland—Sweden Print Cartridge (Part 2 of 2)

Loading Sequence	Symbol	Symbol Description	Symbols per Array
65	Z	Uppercase Z	1
66	Y	Uppercase Y	1
67	X	Uppercase X	1
68	W	Uppercase W	1
69	V	Uppercase V	1
70	U	Uppercase U	1
71	T	Uppercase T	1
72	S	Uppercase S	1
73	R	Uppercase R	1
74	Q	Uppercase Q	1
75	P	Uppercase P	1
76	O	Uppercase O	1
77	N	Uppercase N	1
78	M	Uppercase M	1
79	L	Uppercase L	1
80	K	Uppercase K	1
81	J	Uppercase J	1
82	I	Uppercase I	1
83	H	Uppercase H	1
84	G	Uppercase G	1
85	F	Uppercase F	1
86	E	Uppercase E	1
87	D	Uppercase D	1
88	C	Uppercase C	1
89	B	Uppercase B	1
90	A	Uppercase A	1
91	0	Numeric 0	4
92	9	Numeric Nine	2
93	8	Numeric Eight	2
94	7	Numeric Seven	2
95	6	Numeric Six	2
96	5	Numeric Five	2
97	4	Numeric Four	1
98	3	Numeric Three	1
99	2	Numeric Two	1
100	1	Numeric One	1
101	*	Asterisk	3
102	+	Plus	3
103	,	Comma	3
104	–	Hyphen (Minus)	3
105	.	Period	3
106	/	Slant (Solidus)	3
107	z	Lowercase z	1
108	y	Lowercase y	1
109	x	Lowercase x	1
110	w	Lowercase w	1
111	v	Lowercase v	1
112	u	Lowercase u	1
113	t	Lowercase t	1
114	s	Lowercase s	1
115	r	Lowercase r	1
116	q	Lowercase q	1
117	p	Lowercase p	1
118	o	Lowercase o	1
119	n	Lowercase n	1
120	m	Lowercase m	1
121	l	Lowercase l	1
122	k	Lowercase k	1
123	j	Lowercase j	1
124	i	Lowercase i	1
125	h	Lowercase h	1
126	g	Lowercase g	1
127	f	Lowercase f	1
128	0	Numeric Zero	4
		Array Size	**128**

Table B—21. Japan—Katakana 128-Character Print Cartridge (Part 1 of 2)

Loading Sequence	Symbol	Symbol Description	Symbols per Array
1	ト	Katakana Capital Letter	1
2	ナ	Katakana Capital Letter	1
3	ニ	Katakana Capital Letter	1
4	ヌ	Katakana Capital Letter	1
5	ネ	Katakana Capital Letter	1
6	ノ	Katakana Capital Letter	1
7	ハ	Katakana Capital Letter	1
8	ヒ	Katakana Capital Letter	1
9	フ	Katakana Capital Letter	1
10	ヘ	Katakana Capital Letter	1
11	ホ	Katakana Capital Letter	1
12	マ	Katakana Capital Letter	1
13	ミ	Katakana Capital Letter	1
14	ム	Katakana Capital Letter	1
15	メ	Katakana Capital Letter	1
16	モ	Katakana Capital Letter	1
17	ヤ	Katakana Capital Letter	1
18	ユ	Katakana Capital Letter	1
19	ヨ	Katakana Capital Letter	1
20	ラ	Katakana Capital Letter	1
21	リ	Katakana Capital Letter	1
22	ル	Katakana Capital Letter	1
23	レ	Katakana Capital Letter	1
24	ロ	Katakana Capital Letter	1
25	ワ	Katakana Capital Letter	1
26	ン	Katakana Capital Letter	1
27	゜	Katakana Capital Letter	1
28	0	Numeric Zero	4
29	9	Numeric Nine	4
30	8	Numeric Eight	4
31	7	Numeric Seven	4
32	6	Numeric Six	4
33	5	Numeric Five	2
34	4	Numeric Four	2
35	3	Numeric Three	2
36	2	Numeric Two	2
37	1	Numeric One	2
38	,	Comma	1
39	'	Apostrophe	1
40	|	Vertical Line	1
41	–	Hyphen (Minus)	2
42	\	Reverse Slant (Reverse Solidus)	1
43	.	Period	2
44	_	Discontinuous Underline	1
45	•	Katakana Symbol	1
46	]	Right Square Bracket	1
47	[	Left Square Bracket	1
48	>	Greater Than	1
49	Δ	Delta	1
50	!	Exclamation	1
51	#	Number Sign	1
52	$	Dollar Sign	1
53	%	Percent Sign	1
54	&	Ampersand	1
55	¬	Logical Not	1
56	(	Left Parenthesis	1
57	)	Right Parenthesis	1
58	:	Colon	1
59	;	Semicolon	1
60	=	Equal Sign	1
61	0	Numeric Zero	4
62	@	Commercial At	1
63	?	Question	1
64	¢	Cent Sign	1

Table B—21. Japan—Katakana 12-Character Print Cartridge (Part 2 of 2)

Loading Sequence	Symbol	Symbol Description	Symbols per Array
65	Z	Uppercase Z	1
66	Y	Uppercase Y	1
67	X	Uppercase X	1
68	W	Uppercase W	1
69	V	Uppercase V	1
70	U	Uppercase U	1
71	T	Uppercase T	1
72	S	Uppercase S	1
73	R	Uppercase R	1
74	Q	Uppercase Q	1
75	P	Uppercase P	1
76	O	Uppercase O	1
77	N	Uppercase N	1
78	M	Uppercase M	1
79	L	Uppercase L	1
80	K	Uppercase K	1
81	J	Uppercase J	1
82	I	Uppercase I	1
83	H	Uppercase H	1
84	G	Uppercase G	1
85	F	Uppercase F	1
86	E	Uppercase E	1
87	D	Uppercase D	1
88	C	Uppercase C	1
89	B	Uppercase B	1
90	A	Uppercase A	1
91	0	Numeric Zero	4
92	9	Numeric Nine	2
93	8	Numeric Eight	2
94	7	Numeric Seven	2
95	6	Numeric Six	2
96	5	Numeric Five	2
97	4	Numeric Four	2
98	3	Numeric Three	2
99	2	Numeric Two	2
100	1	Numeric One	2
101	,	Comma	2
102	+	Plus	1
103	<	Less Than	1
104	*	Asterisk	1
105	–	Hyphen (Minus)	1
106	/	Slant (Solidus)	1
107	.	Period	1
108	¥	Yen Sign	1
109	ｱ	Katakana Capital Letter	1
110	ｲ	Katakana Capital Letter	1
111	ｳ	Katakana Capital Letter	1
112	ｴ	Katakana Capital Letter	1
113	ｵ	Katakana Capital Letter	1
114	ｶ	Katakana Capital Letter	1
115	ｷ	Katakana Capital Letter	1
116	ｸ	Katakana Capital Letter	1
117	ｹ	Katakana Capital Letter	1
118	ｺ	Katakana Capital Letter	1
119	ｻ	Katakana Capital Letter	1
120	ｼ	Katakana Capital Letter	1
121	ｽ	Katakana Capital Letter	1
122	ｾ	Katakana Capital Letter	1
123	0	Numeric Zero	4
124	ｿ	Katakana Capital Letter	1
125	ﾀ	Katakana Capital Letter	1
126	ﾁ	Katakana Capital Letter	1
127	ﾂ	Katakana Capital Letter	1
128	ﾃ	Katakana Capital Letter	1
		Array Size	**128**

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