CONUS 24

DIGITAL COMPUTER

GENERAL DESCRIPTION

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Prepared By:

Government Marketing Planning
St. Paul, Minnesota

Date:

September 10, 1064

COMPANY CONFIDENTIAL

CONUS 24 COMPUTER

GENERAL DESCRIPTION

I. INTRODUCTION

The CONUS 24 Computer is a small general purpose, stored program, real-time digital processor. It uses binary notation, is word organized, and operates with two's complement additive arithmetic. Input/output data transfers are buffered, and the computer also includes a communications multiplexer interface for buffered operations with communications devices. All memory locations are directly addressable and may be used for storage of data or instructions.

The CONUS 24 Computer may be operated in any office type environment, and it does not require any special preparations for installation. The physical and functional characteristics of the CONUS 24 are described in the following sections of this manual.

II. PHYSICAL CHARACTERISTICS

The CONUS 24 Computer, including all logic, memory, input/output channels, power supplies, and operator panel, is mounted in a single cabinet approximately 50 inches by 25 inches and 48 inches in height. Thus, the computer requires slightly over eight square feet of floor area. All wiring (power and peripheral data cables) may be brought out through the side of the cabinet at the floor level or through the bottom of the cabinet if the computer is to be used where a false floor is required or desired for other equipments.

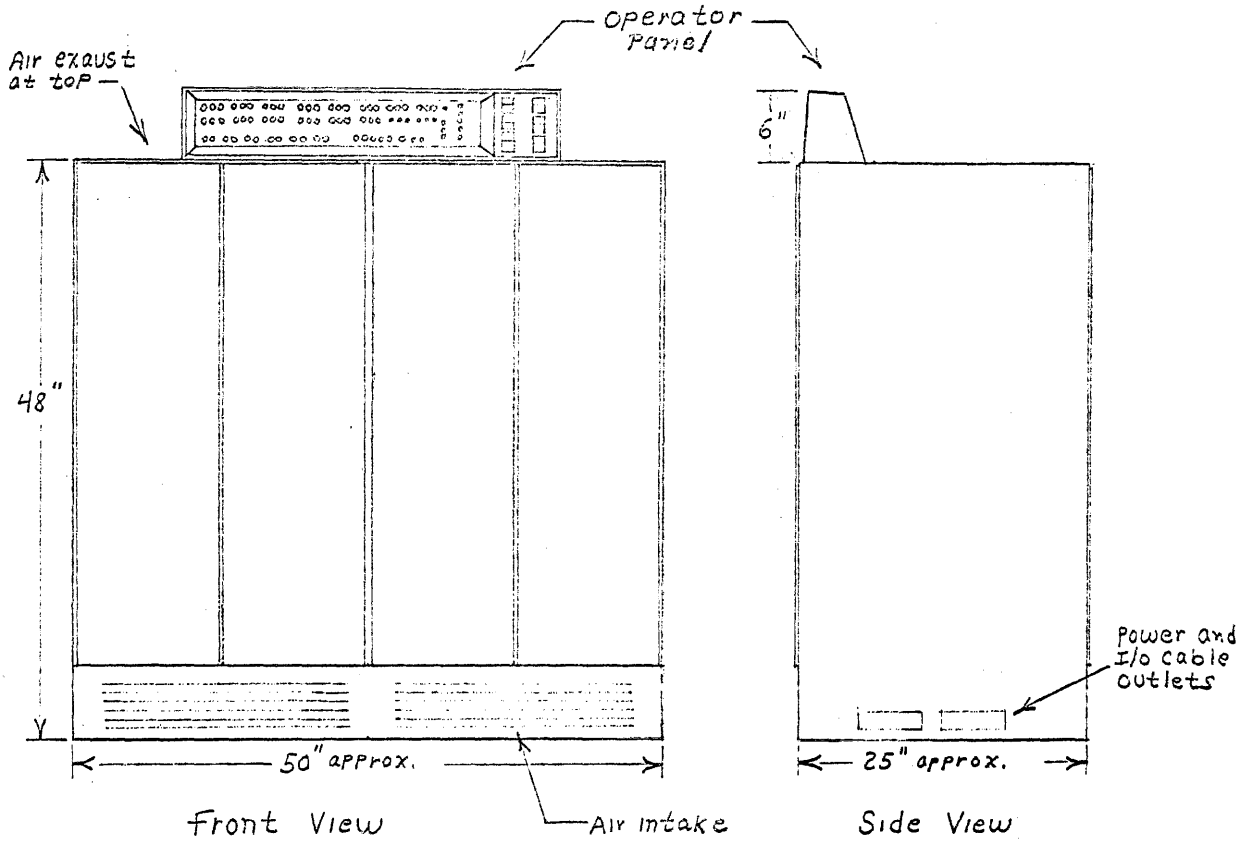
Figure 1 is a diagram of the CONUS 24 Computer. The CONUS 24 Computer uses forced room air for cooling and dissipates from 1,000 watts to 2,000 watts, depending upon the memory size and number of input/output channels included. The front and rear doors of the computer cabinet are hinged at the sides and swing open to allow easy access to the blower, air filter, power supply, logic, and memory.

The operator panel is at a convenient height for use by an adult person, the center of the controls being approximately 51 inches from the floor. The operator panel indicators and controls are displayed on a black background, and the center portion of the panel is recessed slightly so that the neon indicators may be seen easily in high ambient light areas.

The CONUS 24 Computer requires between 1,000 and 2,000 watts of 105-125 volt AC single phase electrical power for operation. The exact power requirements depend upon the memory and input/output options selected. The CONUS 24 Computer will operate satisfactorily without any special provisions for heating or cooling in any environment suitable for office personnel.

FIGURE 1

CONUS 24 COMPUTER



III. FUNCTIONAL DESCRIPTION

The CONUS 24 Computer has a minimum memory size of 4,096 - 24 bit words, expandable in 4,096 word increments to a maximum of 32,768 words. Figure 2 shows the relationships between word and eight bit characters in terms of the memory sizes offered.

FIGURE 2
MEMORY OPTIONS

Function Unit Size	Minimum Size Offered	Incremental Size Offered	Maximum Size Offered
18 Bit Word	4,096	4,096	32,768
8 Level Character	12,288	12,288	98,304

Memory modules may be added to an existing installation as a field modification.

Input/Output

The minimum size CONUS 24 Computer contains, as standard features, three input and three output (a total of six) fully buffered general purpose high speed channels, each capable of transmitting up to 24 bits or three, eight level characters in parallel. The maximum input or output rate allowable with any peripheral device depends on system constraints such as the number of peripheral devices which must operate concurrently. The maximum computer buffered data transfer rate, input or output, can exceed 100,000, 24 bit words per second or over 300,000, eight level characters per second. Normally, with concurrent processing and input/output, the average data transfer rate will be much lower.

The number of buffer control words is not limited by the number of input/output channels. The minimum size CONUS 24 Computer Input/Output section contains fourteen address lines such that communications type peripheral equipments may specify the buffer control word addresses to be used. This feature permits automatic sorting and buffering of communications data between the CONUS 24 Computer memory and the communications facilities by use of the UNIVAC Standard Communications Subsystem.

An additional set of six high speed channels (three for input and three for output) including an additional set of address lines may be ordered as optional equipment and can be installed in a CONUS 24 Computer in the field.

Instruction Operation

The average instruction execution time of the CONUS 24 Computer depends on the individual program being run. The instruction times, including all memory references vary from a minimum of 4.8 microseconds to a maximum of 14.4 microseconds. An average of 9.6 microseconds per instruction may be expected with most programs.

Figure 3 is a simplified block diagram of the CONUS 24 Computer. The registers are identified by capital letters. Note that the A Register (Accumulator) and the P Register (Program Address Register) are contained in core memory. The following description of the functions of each of the registers will aid in understanding the operation of the CONUS 24 Computer.

Description of Registers

S - Storage Address Register. The S Register is fifteen bits in length and is used to hold the address of the particular memory location being accessed during the memory read/write cycle. This register is displayed on the operator panel and its contents may be manually altered except when the computer is operating at high speed.

Z - Memory Data Register. The Z Register is twenty-four bits in length and, in general, is used to receive and hold the data read out of the memory cell whose address is held in the S Register. The Z or data register is displayed on the operator panel and its contents may be altered manually except when the Computer is operating at high speed.

X - Auxiliary Register. The X Register is twenty-four bits in length and is used as an auxiliary arithmetic register and data register. During memory write operations, the contents of the X register are automatically added to the contents of the Z Register and this sum is stored at the address indicated by the S Register.

F - Function Register. The F Register is eight bits in length. It is used to indicate the instruction being executed and it holds the operation or function code and designators while being decoded and executed. The F Register is displayed on the operator panel to aid in program debugging.

C - Output Register. The C Register is twenty-four bits in length and is used to hold data which is to be transmitted to peripheral devices so that the computer can proceed with other operations simultaneously with the transmission of data to slower speed peripheral devices. This register is provided because many peripherals cannot accept data during the short memory reference time when it is offered.

A - Accumulator Register. The A register is twenty-four bits in length and is contained in core memory at address zero. The A Register is explicitly addressable by most instructions by setting Y = 1. The A Register is implicitly addressed and automatically accessed by those instructions which specify its use.

P - Program Address Register. The P Register is a twenty-four bit register which is contained in core memory at address zero. The P Register holds the address of the next instruction to be executed, and it may be explicitly addressed in most instructions by setting Y = 0. The P Register is accessed automatically during the operation of the computer for the purposes of incrementing and obtaining the addresses of instructions to be executed.

Other Functions

Other functions shown in the block diagram include the input/output priority network and the operation of the adder.

Adder - The adder is a parallel, two's complement twenty-four bit device which adds two twenty-four bit numbers (the contents of Z and X) and provides a twenty-four bit sum which is placed in memory at the location whose address is contained in the S Register. Functionally, the adder operates between the read and write cycle such that during every memory reference, the sum of the contents of the Z Register and the contents of the X Register are placed in memory during the write or last half of the read/write memory cycle.

Input/Output Priority - The I/O Priority network determines the next input/output function to be performed and insures that all requested I/O operations are noted and processed in an orderly manner.

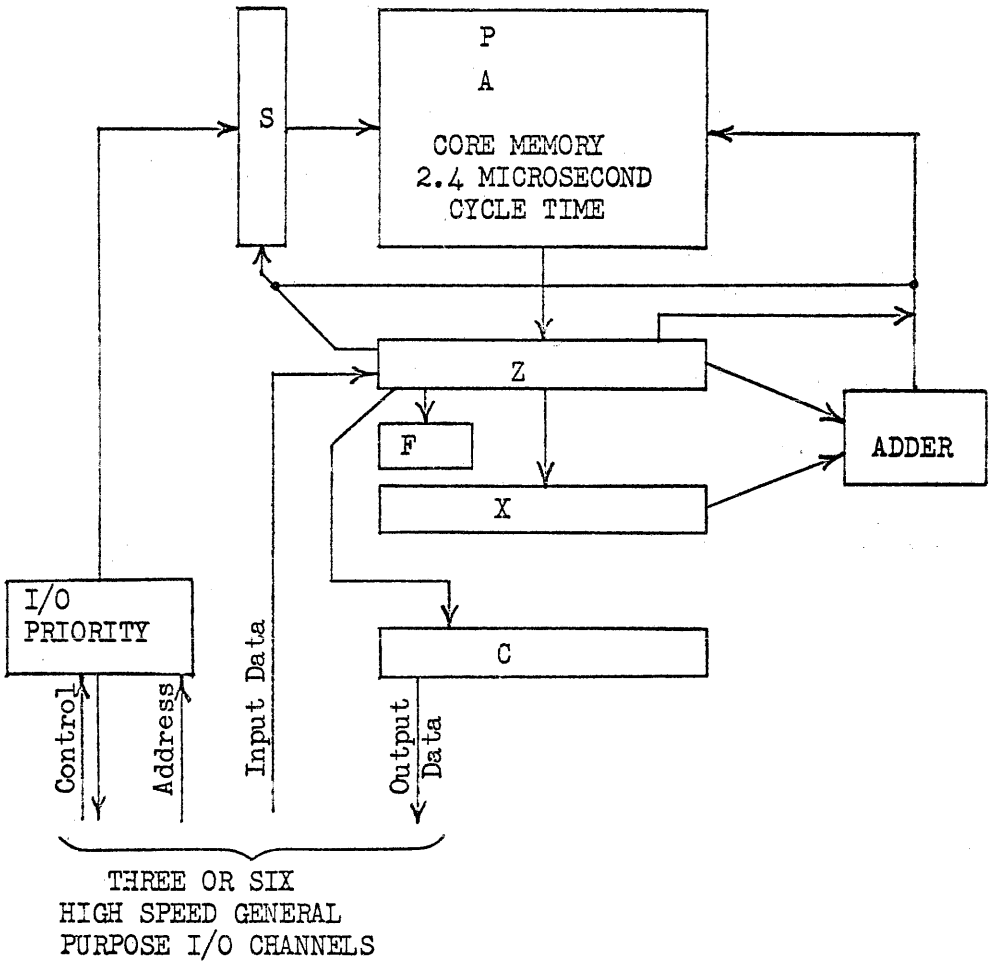
General Theory of Instruction Operation

The accessing and execution of instructions are in the form of successive sequences which are wired into the computer. Each sequence normally involves a memory reference (read/write cycle) and the duration of a sequence normally coincides with the duration of the memory cycle. The following description applies to most of the instructions.

Instructions normally begin with a P sequence. This sequence extracts the address of the instruction from the P Register and increments the address as it is being restored to the P Register. The P sequence, then, consists of one memory read/write cycle. During the read portion of the cycle, the contents of memory location Zero is read into the Z Register. A binary one is automatically placed into the X Register. The sum of the contents of Z and X is then restored to memory at address zero during the write portion of the P cycle.

FIGURE 3

CONUS 24 COMPUTER
SIMPLIFIED BLOCK DIAGRAM



The next sequence is the I, or Instruction sequence which extracts the instruction, restores it to memory, and decodes the function code in the instruction. The I cycle begins by taking the address obtained in the P cycle and placing this address into the S Register. The instruction at this address is then extracted and restored to memory. During the last half of the I sequence, the F Register is loaded with the function or operation portion of the instruction, and the operation called for is decoded. In the case of a JUMP instruction, the next instruction may then begin, as the address of the next instruction is contained in the y portion of the jump instruction. The shortest instructions, JUMP, SKIP, and some I/O instructions which contain only a P and I sequence are two memory cycles in length.

If the B designator in the instruction is set to a value other than zero, the next sequence in the instruction cycle will be a B sequence. The B sequence causes the contents of the appropriate index register to be read and restored to memory. The sum of the contents of the twenty-four bit index register and the fifteen bit address portion of the instruction is placed in the S Register at the end of this sequence. This value becomes the new operand address.

If the i designator in the instruction is set to one, the next sequence in order of execution is the indirect (N) sequence. This sequence places the fifteen bit address portion of the instruction (or the address obtained in the B sequence) into the S Register. The data at this address is then read from memory and restored to memory. This data becomes the effective operand address unless the binary position in this word corresponding to the i designator is set to a one. If the new i designator in this word is set to a one, the B and Indirect (N) sequences are repeated according to the B and i designator settings in this new word. When the i designator is found to be zero, the B and N sequences are terminated.

The next sequence in the instruction cycle may be either an A sequence or a Y sequence. If the contents of the accumulator are to be placed at a storage location, the A Register is accessed to obtain the Accumulator contents, and then the Y sequence is used to place this data at the address Y. If the instruction is, for example, LOAD CONSTANT, only an A sequence is required, because the constant is contained in the instruction. If the instruction is, for example, INCREMENT Y, an A sequence is not required because the contents of the Accumulator will not be needed unless the program has set Y = 1 in this particular instruction in which case the contents of the Accumulator will be incremented.

In summary, the sequences are as follows:

P - Determines the address of the next instruction.

I - Calls the instruction from memory.

B - Adds the index register contents to the instruction address to obtain the operand address.

N - Uses the operand address to obtain the effective address of the operand.

Y - Extracts and modifies the operand.

A - Extracts and modifies the A Register.

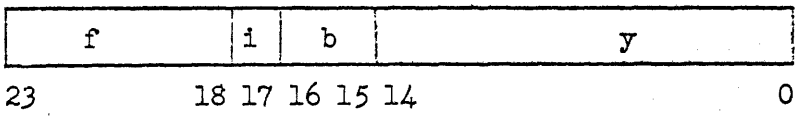
The P and I sequences are always used. The B and N sequences are used if the corresponding designators are set and can be repeated. The Y and A sequences are used as necessary. The average number of sequences of memory cycles used in an average instruction would be approximately three to four.

IV. PROGRAMMING CHARACTERISTICS

The CONUS 24 Computer instructions are twenty-four binary digits in length and each instruction is contained in a single word in the computer memory. The instructions consist of a six bit function code which defines the operation to be performed, a one bit indirect addressing designator, a two bit index register designator, and a fifteen bit operand address designator. Figure 4 shows the instruction word format.

FIGURE 4

INSTRUCTION WORD FORMAT



f = function or operation code - 6 bits.
i = indirect addressing designator - 1 bit.
b = index register (one of three) designator - 2 bits.
y = operand address designator - 15 bits.

The CONUS 24 Computer instructions are as shown in Table 5.

TABLE 5

CONUS 24 INSTRUCTION REPERTOIRE

NAME	OPERATION	NORMAL EXECUTION TIME IN MICROSECONDS
STOP	Computer stops	4.8
STORE STATUS	Store all designators at y	7.2
LOAD STATUS	Load all designators from y	7.2
EXECUTE REMOTE	$(P_{0-15}) \rightarrow Y_{0-15}$, Execute Y + 1	7.2
EXECUTE	$(P_{0-15}) \rightarrow Y_{0-15}$, Y P	7.2
MASK SKIP	Sense Y, Conditional Skip NI	4.8 - 7.2
JUMP	$Y \rightarrow P$	4.8
LOCKOUT	$Y_0 \rightarrow$ Lock Designator	4.8
ADD	$(A) + (Y) \rightarrow A$	9.6
SUBTRACT	$(A) - (Y) \rightarrow A$	9.6
AND	$(A) \odot (Y) \rightarrow A$	9.6
EXCL. DR	$(A) \bar{\oplus} (Y) \rightarrow A$	9.6
STORE B	$(B)_b \rightarrow Y$	9.6
LOAD B	$(Y) \rightarrow B_b$	9.6
LOAD A	$(Y) \rightarrow A$	9.6
LOAD CHAR. 1	$(Y_{0...7}) \rightarrow A_{0...7}$	9.6
LOAD CHAR. 2	$(Y_{8-15}) \rightarrow A_{0-7}$	9.6
LOAD CHAR. 3	$(Y_{16-23}) \rightarrow A_{0-7}$	9.6
STORE A	$(A) \rightarrow Y$	9.6
STORE CHAR. 1	$(A_{0...7}) \rightarrow Y_{0...7}$	9.6
STORE CHAR. 2	$(A_{0...7}) \rightarrow Y_{8-15}$	9.6
STORE CHAR. 3	$(A_{0...7}) \rightarrow Y_{16-23}$	9.6

NAME	OPERATION	NORMAL EXECUTION TIME IN MICROSECONDS
INCREMENT	(Y) + 1⟶Y	7.2
LOAD CONSTANT	Y⟶A	7.2
INDEX SKIP	(Y) - 1⟶Y, Skip NI if $(Y)_f < 0$	7.2 - NS 9.6 - S
STORE ADDRESS	$(A_{0...15})$⟶$Y_{0...15}$	9.6
CHARACTER SHIFT	(Y) Left Circular 8 bits	7.2
SHIFT RIGHT	(A) Right open Y bits, y = 0...7 only	4.8 + K (2.4)
SHIFT LEFT	(A) Left open Y birs, y = 0...7 only	4.8 + K (2.4)
PARITY	Set designators	7.2
ESCAPE	Interrupt to Y	4.8
ACTIVATE I/O	Activate Channel Y	4.8
EXTERNAL FUNCTION	(A)⟶Channel Y	7.2
STORE REMOTE	ESI or Channel Y data⟶A	7.2

The use of indirect addressing adds 2.4 microseconds to each instruction execution time per each indirect cycle executed. The use of the index registers adds 2.4 microseconds to each instruction execution time per each indexing cycle used.

The instruction repertoire for the CONUS 24 Computer has been designed to allow easy programming of basic arithmetic, logical, and business decision operations. By storing each instruction in a 24 bit word, optimum use of the storage for instructions is realized, as there are no wasted bit positions. The use of eight level characters for alpha and numeric information provides compatibility with all common computer character codes. The ability of the CONUS 24 Computer to address characters in groups of three (three 8 level characters per word) provides very fast operation. Note that certain instructions are provided for operating on single characters in each group of three.

The CONUS 24 Computer can directly address 32,768 words of storage and allow indirect addressing and indexing even with its short instruction. This ability makes software much easier to write, faster, and does not introduce a great number of programming restrictions. Since all instructions are short, and since the status of the designators may be stored and loaded with a single pair of instructions, the handling of real-time interrupts can be extremely rapid, and interrupts need not be deferred for long times. This allows the CONUS 24 Computer to handle real-time operations extremely fast.

The CONUS 24 Computer instruction repertoire was designed using statistical "frequency of use" tables compiled from business, real-time, and information retrieval and storage programs in use on various other computers. Single, double, and triple address computers were studied as well as decimal and binary types of machines. The CONUS 24 Computer, for its functional size, represents an optimum solution for batch business, real-time, and information storage and retrieval problems. Instructions which are very seldom used or needed may be programmed easily using the basic instructions provided.

Input and Output

The basic CONUS 24 Computer contains three general purpose high speed input channels and three general purpose high speed output channels. In addition, a set of address lines is provided for multiplexing a number of peripherals on to one of the high speed channel input and output pairs.

Input/output data transfers are normally carried on by the memory of the CONUS 24 Computer and the peripheral device in such a way that the computer program is not logically interrupted. The input/output logic operates by temporarily suspending the program for three memory cycles during which time one twenty-four bit word is transferred to or from the peripheral device and the CONUS 24 memory. Three memory cycles are necessary for this operation because the CONUS 24 Computer memory and I/O logic also monitors and controls

the number of words to be transferred, the memory addresses involved, and the conditions under which the transfer of data is automatically stopped. No provisions need be made in the writing of programs for individual buffered I/O word transfers. They have no effect upon the program logic except to slow the running of the program slightly and to interrupt the program after the proper number of words have been transferred.

The rate of data word transfers between peripheral equipments and the CONUS 24 Computer are governed by the transfer rate of the peripheral devices if they are slower than the CONUS 24 Computer and by the CONUS 24 Computer if they are faster.

All of the CONUS 24 input and output channels may be active concurrently. Through the use of the address lines provided and a communications multiplexer, the number of active input and output data word buffers is limited only by the number of peripheral devices which are required and the total data transfer rate which the CONUS 24 Computer can handle from all of the peripheral devices combined.

Buffer Control Words

The CONUS 24 Computer contains in memory, two twenty-four bit words for each buffer operation to be established. These words are loaded initially by the program. They are then placed under control of the input/output logic for the duration of the time during which the transfers will take place. The first location in memory associated with a buffered transfer initially holds the count of the total number of data words to be transferred. The second location, one address above the first location, holds the address of the memory cell into which the first data word is to be placed (input), or the address of where the first output data word is to be obtained from (output). The word count is decremented and the data address is incremented automatically during each data transfer by the input/output logic. When the count reaches zero, a monitor interrupt is generated to inform the program that the number of words called for has been transferred. At the same time, the input/output logic also deactivates the channel. The procedure to initiate a buffered transfer of N words is as follows:

1. The program loads the count location for the desired channel with the number of words N.

2. The program loads the address location for the same channel with the first data storage address to be involved in the data transfer.

3. The program executes an EXTERNAL FUNCTION instruction which directs the peripheral device to begin operation.

4. The program executes an ACTIVATE I/O instruction which transfers control of the buffer control words to the input/output logic of the channel involved. The actual transfer of data words to or from the CONUS 24 Computer and the peripheral device then proceeds logically independent of the program. When all of the words have been transferred, a monitor interrupt will occur. This monitor interrupt will cause the computer to execute an instruction in a memory location permanently associated with the channel through which the data transfers took place. This has the effect of logically interrupting the program. Interrupts may be locked out by use of the LOCKOUT instruction which is normally used only when transferring control from one program to another under executive program control.

The buffered sequence for the transfer of a single word to or from the CONUS 24 Computer and a peripheral device is as follows:

1. The peripheral device sends the request to the computer.

2. The computer suspends the execution of the next instruction temporarily for the next three memory cycles.

3. The count is read out of memory, and restored to memory decremented during the write portion of the same memory cycle. If the count restored to memory is zero, the logic for generating a monitor interrupt is activated. The transfer, however, continues in either case.

4. The data address is read out of memory and restored to memory incremented. This data address, before incrementation, is saved for the next memory cycle.

5. The data presented by the peripheral device is placed in memory at the data address (input), or the data at the address in memory is sent to the peripheral device (output). This data transfer cycle is the third and last memory reference in the buffered sequence.

6. The program automatically resumes where it was suspended and the next instruction is executed, etc.

The program will continue to run without any suspension or time interruption until the next request is received from a peripheral device.

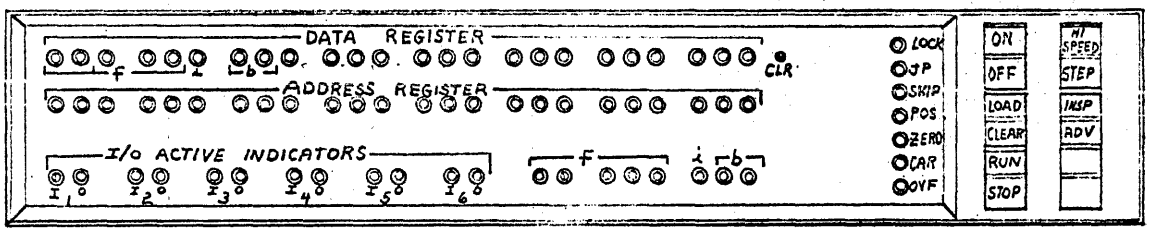
VI. OPERATOR PANEL

The operator panel mounted on the CONUS 24 Computer is used to start and stop the computer, enter a limited amount of information, display the contents of any memory location, aid in program debugging, and facilitate maintenance if it should ever be required.

The layout of the operator panel is shown in Figure 6.

FIGURE 6

OPERATOR PANEL



Power is applied to the CONUS 24 Computer by depressing the ON switch. The switch lights when power is applied. If the OFF switch is depressed, the ON switch will become dark and power is removed. The procedure to start the CONUS 24 Computer, high speed, is as follows: 1) With the computer on, depress the CLEAR switch which master clears the computer. 2) Depress the HI SPEED switch which readies the computer for high speed operation. 3) Depress the LOAD switch. Depressing the LOAD switch conditions the computer to accept a program starting address. The JP (Jump) designator will light when the LOAD switch is depressed. This indicates that the computer is prepared to jump to the address which is manually inserted into the Data Register. 4) Enter the starting address of the program into the Data Register. If a mistake is made, the register may be cleared by means of the small clear button to the right of the register. Finally, depress the RUN switch. The computer will indicate a stop by extinguishing the RUN indicator and lighting the STOP indicator.

In order to inspect any memory location and enter data or instructions directly into the CONUS 24 Memory, the CLEAR switch should be depressed and the INSPECT switch should also be depressed.

Next, the LOAD switch should be depressed. This will prepare the computer to accept the first address to be inspected. The address to be inspected should then be loaded into the Data Register. When the RUN switch is depressed, the manually inserted address will be transferred to the Address Register, and the information at that address in core memory will be displayed in the Data Register. This information may be cleared out by means of the small clear button to the right of the data register, and new information may be entered into this memory location by depressing the appropriate bit position indicator switches.

In order to inspect the next consecutive address, the ADVANCE switch should be depressed. The computer will then automatically increment the address displayed in the Address Register by one and will display the contents of this new memory location in the Data Register.

If a different address, not in sequence, is to be inspected, the STOP, CLEAR, and LOAD switches should be depressed again. The new address may then be entered into the Data Register, and the computer may be started as before.

Step operation allows slow speed operation of a program in such a way that one instruction is executed each time that the ADVANCE switch is depressed. The CONUS 24 Computer should be placed into the STEP mode in order to operate at slow speed. This is accomplished by depressing the CLEAR switch, followed by depressing STEP switch. The Load switch should then be depressed, and the starting address is entered into the Data Register. The computer is then started by depressing the RUN switch. Each time that the ADVANCE switch is depressed, the CONUS 24 Computer will execute one instruction. The Data Register and Address Register will display the results of the last memory reference in the instruction just executed. The function code will be displayed in the Function Register, and the appropriate designator settings will also be displayed.

If peripheral devices are active and an I/O data transfer takes place following the instruction in the STEP mode, the last memory reference of the input or output transfer, data and address will be displayed in the Data and Address Registers, respectively.

If the switches on the Operator Panel are not depressed in the correct sequence, or if they are depressed accidentally during high speed operation, no harm will result to the electrical components. Some of the program or data stored in memory may be destroyed, however, and it may be necessary to reload the mutilated information either manually or via the bootstrap program and data stored in a peripheral device such as a card reader.

The following indicators, in addition to the Data and Address (Z and S) Registers are displayed on the operator console.

LOCK - indicates if the I/O Interrupt Lockout is set.

JP - indicates if a jump instruction has been executed or if the computer is conditioned to accept a starting address.

SKIP - The skip indicator indicates if a skip instruction has been executed, and the skip will be performed.

POS - the positive designator is set during certain instructions and is sensed by the SKIP instruction.

ZERO - the zero designator is set during certain instructions and is sensed by the SKIP instruction.

CAR - the carry designator is set during certain instructions when an adder carry occurs and it is sensed by use of the SKIP instruction.

OVF - the overflow designator is set during certain arithmetic instructions when adder overflow occurs. It is sensed by use of the SKIP instruction.

I - six I designators are displayed in the six channel model of the CONUS 24 Computer (three in the three channel model). These designators indicate if the corresponding input channel is in an active status.

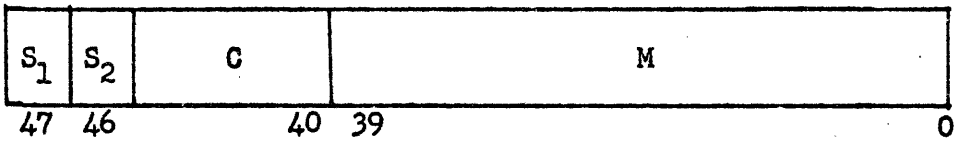
O - six O designators are displayed in the six channel model of the CONUS 24 Computer (three in the three channel model). This designator is lit if the corresponding output channel is in an active status.

The neon indicators on the recessed portion of the Operator Panel indicate correctly only when they are set to one state over a long period of time or when the computer is in the INSPECT or STEP modes or when the computer is stopped. When the computer is operating at high speed, indications normally change at a rate too high for the neon indicators or eye to follow, and any indications during high speed operation are normally not useful. Possible exceptions are the I/O active indicators which are associated with channels on which very slow speed peripherals are being operated.

CONUS 24 FLOATING POINT

Assuming a 48 bit optional arithmetic section, the following floating point package will be applicable.

Word Format



Where

M (Mantissa) = 40 bits

C (Characteristic) = 6 bits

S_1 (Sign of Mantissa) = 1 bit

S_2 (Sign of Characteristic) = 1 bit

The basic algorithm for floating point is identical to that used presently in the 1107 with the exception of renormalization. The renormalization portion of the Floating Point algorithm will be variable according to a variable characteristic base (2,4,16,256) as designated by the programmer, i.e. renormalize the mantissa in groups of 1,2,4,8 respectively.

If X is the mantissa and § is the base, X is normalized if the following holds:

$$1/\S \leq X < 1$$

Given the floating point format as described above the following numerical ranges (N) are possible:

base 2	$2^{-63} \leq N \leq 2^{63}$	$\approx$ $10^{-21} \leq N \leq 10^{21}$
base 4	$2^{-126} \leq N \leq 2^{126}$	$\approx$ $10^{-42} \leq N \leq 10^{42}$
base 16	$2^{-252} \leq N \leq 2^{252}$	$\approx$ $10^{-84} \leq N \leq 10^{84}$
base 256	$2^{-504} \leq N \leq 2^{504}$	$\approx$ $10^{-168} \leq N \leq 10^{168}$

Implimentation of the variable base will be accomplished by a 3 bit (binary) base register which may be set by the programmer with a special instruction. The register will be used by the hardware to determine the appropriate scaling proceedure at the completion of each floating point arithmetic instruction. The cost of incorporating this feature is in the neighborhood of $300 to $400.

The feature is justified from both an applications and a marketing standpoint. From an application standpoint there are two basic advantages of variable base floating point over fixed base floating point. 1) Increased significance when dealing with small numbers. 2) Ability to handle large numbers. And obviously there are no disadvantages, in that the identical results can be achieved by using the same base.* From the marketing standpoint we need only say, "We offer everything that the IBM 360 offers [floating point to the base 16] and more."

*See Appendix for a more rigorous analysis of application advantages.

The following is an initial list of instructions to be available with the optional 48 bit arithmetic section.

1. Fixed Point Add
   The contents of memory (48 bits) are added to the accumulator (2's complement arithmetic)
2. Fixed Point Subtract
3. Fixed Point Multiply
   Two 48 bit vectors into 96 bit result
4. Fixed Point Divide
   A 48 bit vector into a 96 bit vector resulting in a 48 bit quotient and a 48 bit remainder.
5. Floating Point Add
6. Floating Point Subtract
7. Floating Point Multiply
8. Floating Point Divide
9. Floating Pack (to be defined)
10. Floating Unpack (to be defined)
11. Jump if A = 0 Fixed Point .
12. Jump if $A < 0$ " "
13. Jump if $0 \leq A$ " "
14. Skip if $A < Y$ " "
15. Skip if A = Y " "
16. Skip if $Y \leq A$ " "

In addition to these instructions, others will be considered according to their merit.