THE ERA 1103

COMPUTER SYSTEM

(TYPE 2300C1)

VOLUME ONE

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SECTION 1

GENERAL DESCRIPTION

1. GENERAL.

The ERA 1103 equipment is a general-purpose digital computer for applications requiring large storage capacity, high operating speed, and great programming versatility. Its internal memory consists of 16,384 registers of magnetic drum storage, 1024 registers of magnetic core storage, and the A and Q registers. Each register is individually addressed and directly accessible. Supplementary storage of 262,144 words is provided by four magnetic tape units. Information is transmitted to and from the tapes in blocks of a fixed number of words each.

The computer performs 44 different input-output, arithmetic, and logical operations. It is fully automatic in that the sequence of operations is determined by a program of internally stored instructions capable of self modification. To attain high computing speed, the computer operates in the parallel mode, i.e. all digits of a number are operated upon simultaneously. Internal arithmetic operations are in the binary system. The basic word size is 36 binary digits, or "bits". A word may be an instruction, a number, or an arbitrarily coded quantity.

The basic systems used for input and output in the ERA 1103 computer employ a Ferranti photoelectric tape reader, a typewriter, and a high speed punch, respectively. However, communication with a variety of optional external equipment is possible by use of an 8-bit register (IOA) and a 36-bit register (IOB) in connection with appropriate external equipment instructions. These registers, together with the basic output registers, TWR and HPR, are arranged to permit simultaneous use of several external output or input-output units, and to allow computation to proceed while such terminal equipment is operating.

The basic computer weighs approximately 33,600 pounds, and occupies a space, including working space, of 26 by 60 feet. The power service required is 220 vac, 3 phase; the power factor is 0.9 inductive with a power consumption of 42 kw. The equipment contains approximately 4700 vacuum tubes, 6000 crystal diodes, and 150 relays and consists of six large air-cooled cabinets containing electronic circuits, a photoelectric tape reader, an electric typewriter, a high-speed tape punch, two motor generator sets, and an air conditioning cabinet.

2. GLOSSARY OF ABBREVIATIONS AND TERMS USED IN THIS SECTION

A	The 72-bit Accumulator (A_{71}, A_{70}, ... A_0)
(A)	The 72-bit word in A.
A_L	The left hand (most significant) 36 bits of A.
(A_L)	The 36-bit word in A_L.

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A_R	The right-hand (lease significant) 36 bits of A
(A_R)	The 36-bit word in A_R
AIK	The Angular Index Counter
$\longrightarrow$	(Arrow) Transmit, such as $A_R \rightarrow X$
AR	A ten-stage Address Register, used to store a Magnetic Core address during a reading or writing operation.
ARAC	The Arithmetic Register Access Control
ASC	The Arithmetic Sequence Control
Bit	Binary digit
BK	Block counter
CI	The Current Instruction
Core	A small toroid of Ferrite capable of storing a binary digit (bit) equal to "1" or "0", depending upon the direction of remnant magnetization of the toroid.
CRC	The Clock Rate Control
CSS	The Clock Source Selector
CTC	The Command Timing Circuits
D(Q)	A 72-bit word whose right-hand 36 bits are the contents of Q and whose left-hand 36 bits are all alike and equal to the left-most bit of the contents of Q.
D(u)	A 72-bit word whose right-hand 36 bits are the contents of u and whose left-hand 36 bits are all alike and equal to the left-most bit of the contents of u.
D(v)	A 72-bit word whose right-hand 36 bits are the contents of v and whose left-hand 36 bits are all alike and equal to the left-most bit of the contents of v.
F_1	A Fixed Address 00000 (or 40001 depending on a switch setting)
F_2	A Fixed Address 00001
HPC	The High-Speed Punch Control
HPR	The High-Speed Punch Register
I/D	Inhibit/Disturb, a term used to describe circuits which control the selective writing of information in cores.

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Instruction	A word, represented by $i_{35}, i_{34}, \ldots i_0$, which causes the computer to perform one or more of its operations. It consists of an operation code and, usually, two execution addresses.
IOA	An in-out register of 8 bits
IOB	An in-out register of 36 bits
IR	Magnetic Core Input register, a 36-stage register that serves as a transfer register between X and the cores.
j	A one-digit octal number (u_{14}, u_{13}, u_{12})
k	The Shift Count ($v_6, v_5, \ldots, v_0$)
LK	A Line Counter
L(Q) (u)	A 72-bit word whose left-hand 36 bits are zeros and each of whose right-hand 36 bits is given by the bit-by-bit product of the corresponding bits of Q and u.
L(Q)'(v)	A 72-bit word whose left-hand 36 bits are zeros and each of whose right-hand 36 bits is given by the bit-by-bit product of the corresponding bits of v and the Complement of Q.
MC	A prefix denoting "Magnetic Core", used to designate signals belonging to the Magnetic Core Storage System.
MCR	The Main Control Register, a part of PCR
MCS	The Magnetic Core Storage System
MCT	The Main Control Translator
MD	The Magnetic Drum Storage System
MDAC	The Magnetic Drum Storage Access Control.
MP	A MAIN PULSE, usually followed by a numeral
MPD	The Main Pulse Distributor
MT	The Magnetic Tape Storage System
MTI	The Magnetic Tape Storage Input Register
MTO	The Magnetic Tape Storage Output Register
MTSC	The Magnetic Tape Storage Sequence Control
n	a four-digit octal number ($u_{11}, u_{10}, \ldots, u_0$)

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NI	The Next Instruction
Operand	A word on which an operation is performed.
Operation Code	That six-bit part of an instruction, represented by $i_{35}, i_{34} \ldots i_{30}$, designating the operation to be performed.
PAK	The Program Address Counter
( )	(Parentheses) Denotes "the content of"
PCR	The Program Control Registers, MCR, UAK, VAK.
PDC	The Pulse Distributor Control
'	(Prime) Denotes "the complement of" such as Q', X', etc.
Q	The 36-bit Q-Register ($Q_{35}, Q_{34}, \ldots, Q_0$)
(Q)	The 36-bit word in Q
RSC	The Repeat Sequence Control
S(u)	A 72-bit word whose right-hand 36 bits are the contents of u and whose left-hand 36 bits are all zeros.
SAR	The Storage Address Register
SCC	The Storage Class Control
SCP	Supervisory Control Panel
SCT	The Storage Class Translator
SKC	The Shift Counter Control
TWR	The Typewriter Register
u	The first execution address ($i_{29}, i_{28} \ldots, i_{15}$)
(u)	The content of u
UAK	The U-Address Counter, a part of PCR
v	The second execution address ($i_{14}, i_{13}, \ldots, i_0$)
(v)	The content of v
VAK	The V-Address Counter, a part of PCR
WK	The Word Counter

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w The v-address portion of a Repeat instruction

X The X-Register (X_{35}, X_{34}, ..., X_0)

y The address of the current instruction.

3. PURPOSE AND BASIC PRINCIPLES.

The ERA 1103 equipment is used to perform a wide variety of large-scale calculations. It solves, at an extremely high rate of speed, any problem which can be presented to it as a series of instructions which order the performance of arithmetic and logical operations upon stored operands. The system is also adaptable to many special purpose applications, including simulation and control in real time.

The series of instructions and operands, called a program, is initially entered into the storage systems in a coded form which the computer interprets. A system of two-address logic is employed; an instruction word consists of a 6-bit operation code and two 15-bit execution addresses. The operation code specifies which of the 44 possible operations is to be performed. The functions of the execution addresses are different for the various types of instructions, but, in general, they specify registers in the memory from which operands are to be obtained or in which results are to be stored. During the performance of a program, instructions are removed, one at a time, from storage in the order in which they are required. Each instruction orders a specified operation to be performed upon the operands stored at the execution addresses. The intermediate and final results of the computations are either stored or presented to the output equipment. The final instruction of the program either stops the computer or initiates the performance of a new program.

The computer employs a "1's" complement system of notation in which the left-most bit of a number is the sign bit of that number and the binary point is considered to be to the right of the lowest order bit. Thus, if the left-most bit of a number is "0", the number is said to be positive; if it is a "1", the number is said to be negative. In the "1's" complement system, a negative number can be obtained by complementing all the bits (including the sign bit) of the corresponding positive number. In the single length, or 36-bit, registers, integers from $1-2^{35}$ up to $2^{35}-1$ may be represented; in the double length Accumulator (72 stages) integers from $1-2^{71}$ up to $2^{71}-1$ may be represented. In "1's" complement notation, each of these integers has a unique representation with the exception of zero; zero has both a negative and positive notation; however, due to the nature of the arithmetic operations in the ERA 1103, a negative zero can not be generated.

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Integers not lying in the above range as well as fractional quantities that may occur in certain problems can also be handled by suitably scaling such quantities so that the resulting quantity can be represented by machine numbers. This scaling can either be accomplished using the Scale Factor instruction or by using suitable "floating point" routines.

4. REPERTOIRE OF INSTRUCTIONS.

The complete list of instructions which the computer performs is presented below. The instructions are arranged in 11 groups, according to their basic characteristics. In each listing a code representing the instruction is enclosed in parentheses after the name of the instruction. The operation code portion is designated by a two-number combination and the execution addresses by the letters u and v. In some cases u is replaced by the conditioning factors j and n, as in the Repeat instruction; and v is replaced either by the repeat termination address w, or in shifting operations by the factor k. Table 1-1 shows the entire repertoire of instructions arranged by their octal code number. Unit's digits of the operation code are arranged horizontally, eight's digits vertically. In Table 1-1 the operation code portion of each instruction is also represented by letters suggesting the name and function of the instruction.

a. SEQUENCED INSTRUCTIONS.

(1) MULTIPLY (71uv): Form in A the 72-bit product of (u) and (v), leaving in Q the multiplier (u).

(2) MULTIPLY ADD (72uv): Add to (A) the 72-bit product of (u) and (v), leaving in Q the multiplier (u).

(3) DIVIDE (73uv): Divide the 72-bit number (A) by (u), putting the quotient in Q, and leaving in A a non-negative remainder R. Then replace (v) by (Q). The quotient and remainder are defined by: $(A)_i = (u) \cdot (Q) + R$, where $0 \leq R < |(u)|$. Here $(A)_i$ denotes the initial contents of A.

(4) SCALE FACTOR (74uv): Replace (A) with D(u). Then left circular shift (A) by 36 places. Then continue to shift (A) until $A_{34} \neq A_{35}$. Then replace the right-hand 15 bits of (v) with the number of left circular shifts, k, which would be necessary to return (A) to its original position. If (A) is all ones or zeros, k = 37. If u is the address of the Accumulator, (A) is left unchanged in the first step, instead of being replaced by $D(A_R)$.

(5) REPEAT (75jnw): This instruction calls for the next instruction, which will be called NIuv, to be executed n times, its "u" and "v" addresses being modified or not according to the value of j. Normally n executions are made and the program is continued by the execution of the instruction stored at a fixed MC address F_1. The steps carried out are:

(a) Replace the right-hand 15 bits of (F_1) with the address w.

*(b) Execute NIuv, the next instruction in the program n times.

* See Repeat Sequence Control, Page 19, this Section.

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TABLE 1-1. REPERTOIRE OF INSTRUCTIONS, ERA 1103 COMPUTER

3^1 \ 3^0	0	1	2	3	4	5	6	7
0								
1		TPuv	TMuv	TNuv	IP--	TUuv	TVuv	EFv
2		RAuv		RSuv				CCuv
3		SPuk	SAuk	SNuk	SSuk	ATuv	STuv	RJuv
4		IJuv	TJuv	EJuv	QJuv	MJjv	SJuv	ZJuv
5		QTuv	QAuv	QSuv	LAuk	LQuk	MSjv	FS
6		PRv		PUjv	RMjnv	WMjnv	AMjn	BMjn
7		MPuv	MAuv	DVuv	SFuv	RPjnw	ERjv	EWjv

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(c) If j = 0, do not change u and v.

If j = 1, add one to v after each execution.

If j = 2, add one to u after each execution.

If j = 3, add one to u and v after each execution.

*(d) On completing n executions, take (F_1) as the next instruction.

*(e) If the repeated instruction is a jump of stop instruction, the occurrence of a jump or stop terminates the repetition. In addition, if NIuv is a Threshold Jump or an Equality Jump, and the jump to address v occurs, (Q) is replaced by the quantity j, (n-r), where r is the number of executions that have taken place.

b. TRANSMISSIVE INSTRUCTIONS.

(1) TRANSMIT POSITIVE (11uv): Replace (v) with (u).

(2) TRANSMIT NEGATIVE (13uv): Replace (v) with the complement of (u).

(3) TRANSMIT MAGNITUDE (12uv): Replace (v) with the absolute magnitude of (u).

(4) TRANSMIT U-ADDRESS (15uv): Replace the 15 bits of (v), designated by v_{15} through v_{29}, with the corresponding bits of (u), leaving the remaining 21 bits of (v) undisturbed.

(5) TRANSMIT V-ADDRESS (16uv): Replace the right-hand 15 bits of (v) designated by v_0 through v_{14}, with the corresponding bits of (u), leaving the remaining 21 bits of (v) undisturbed.

(6) ADD AND TRANSMIT (35uv): Add D(u) to (A). Then replace (v) with (A_R).

(7) SUBTRACT AND TRANSMIT (36uv): Subtract D(u) from (A). Then replace (v) with (A_R).

c. Q-CONTROLLED INSTRUCTIONS

(1) Q-CONTROLLED TRANSMIT (51uv): Form in A the number L(Q)(u). Then replace (v) by (A_R).

(2) Q-CONTROLLED ADD (52uv): Add to (A) the number L(Q)(u). Then replace (v) by (A_R).

(3) Q-CONTROLLED SUBSTITUTE (53uv): Form in A the quantity L(Q)(u) plus L(Q)'(v). Then replace (v) with (A_R). The effect is to replace selected bits of (v) with the corresponding bits of (u) in those places corresponding to 1's in Q.

* See Repeat Sequence Control, Page 19, this Section.

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d. REPLACE INSTRUCTIONS.

(1) REPLACE ADD (21uv): Form in A the sum of D(u) and D(v). Then replace (u) with (A_R).

(2) REPLACE SUBTRACT (23uv): Form in A the difference D(u) minus D(v). Then replace (u) with (A_R).

(3) CONTROLLED COMPLEMENT (27uv): Replace (A_R) with (u) leaving (A_L) undisturbed. Then complement those bits of (A_R) that correspond to ones in (v). Then replace (u) with (A_R).

(4) LEFT SHIFT IN A (54uk): Replace (A) with D(u). Then left circular shift (A) by k places. Then replace (u) with (A_R). If u is the address of the Accumulator, the first step is omitted, so that the initial content of A is shifted.

(5) LEFT SHIFT IN Q (55uk): Replace (Q) with (u). Then left circular shift (Q) by k places. Then replace (u) with (Q).

e. SPLIT INSTRUCTIONS.

(1) SPLIT POSITIVE ENTRY (31uk): Form S(u) in A. Then left circular shift (A) by k places.

(2) SPLIT NEGATIVE ENTRY (33uk): Form in A the complement of S(u). Then left circular shift (A) by k places.

(3) SPLIT ADD (32uk): Add S(u) to (A). Then left circular shift (A) by k places.

(4) SPLIT SUBTRACT (34uk): Subtract S(u) from (A). Then left circular shift (A) by k places.

f. TWO-WAY CONDITIONAL JUMP INSTRUCTIONS.

(1) SIGN JUMP (46uv): If $A_{71} = 1$, take (u) as NI. If $A_{71} = 0$, take (v) as NI.

(2) ZERO JUMP (47uv): If (A) is not zero, take (u) as NI. If (A) is zero, take (v) as NI.

(3) Q-JUMP (44uv): If $Q_{35} = 1$, take (u) as NI. If $Q_{35} = 0$, take (v) as NI. Then, in either case, left circular shift (Q) by one place.

g. ONE-WAY CONDITIONAL JUMP INSTRUCTIONS.

(1) INDEX JUMP (41uv): Form in A the difference D(u) minus 1. Then if $A_{71} = 1$, continue the present sequence of instructions; if $A_{71} = 0$, replace (u) with (A_R) and take (v) as NI.

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(2) THRESHOLD JUMP (42uv): If D(u) is greater than (A), take (v) as NI; if not, continue the present sequence. In either case, leave (A) in its initial state.

(3) EQUALITY JUMP (43uv): If S(u) equals (A), take (v) as NI; if not, continue the present sequence. In either case leave (A) in its initial state.

h. ONE-WAY UNCONDITIONAL JUMP INSTRUCTIONS.

(1) MANUALLY SELECTIVE JUMP (45jv): If the number j is zero, take (v) as NI. If j is 1, 2 or 3, and the correspondingly numbered MJ selecting switch is set to "jump", take (v) as NI; if this switch is not set to "jump", continue the present sequence.

(2) RETURN JUMP (37uv): Let y represent the address from which CI was obtained. Replace the right-hand 15 bits of (u) with the quantity y plus 1. Then take (v) as NI.

(3) INTERPRET (14--): Let Y represent the address from which CI was obtained. Replace the right-hand 15 bits of (F_1) with the quantity Y plus 1. Then take (F_2) as NI.

i. MAGNETIC TAPE STORAGE INSTRUCTIONS.

(1) ADVANCE MAGNETIC TAPE (66jn-): Move the magnetic tape of MT unit j in the forward direction by n blocks. (Note: One block consists of 32 words.)

(2) BACK MAGNETIC TAPE (67jn-): Move the magnetic tape of MT unit j in the backward direction by n blocks.

(3) READ MAGNETIC TAPE (64jnv): Read n blocks from MT unit j (running forward) to 32 n consecutive addresses in MC starting with v.

(4) WRITE MAGNETIC TAPE (65jnv): From 32 n consecutive addresses in MC, starting with v, write n blocks on MT unit j (running forward).

j. STOP INSTRUCTIONS.

(1) MANUALLY SELECTIVE STOP (56jv): If j = 0, stop computer operation and provide suitable indication. If j = 1, 2, or 3 and the correspondingly numbered MS selecting switch is set to "stop", stop computer operation and provide suitable indication. Whether or not a stop occurs, (v) is NI.

(2) FINAL STOP (57--): Stop computer operation and provide suitable indication.

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k. EXTERNAL EQUIPMENT INSTRUCTIONS.

(1) EXTERNAL FUNCTION (17-v): As designated by (v) select a unit of external equipment and cause it to perform a function.

(2) EXTERNAL READ (76jv): If j = 0, replace the right-hand 8 bits of (v) with (IOA); if j = 1, replace (v) with (IOB).

(3) EXTERNAL WRITE (77jv): If j = 0, replace (IOA) with the right-hand 8 bits of (v); if j = 1, replace (IOB) with (v). Cause the previously selected unit to respond to the information in IOA or IOB.

(4) PRINT (61-v): Replace (TWR) with the right-hand 6 bits of (v). Cause the typewriter to perform the operation specified by the 6-bit code.

(5) PUNCH (63jv): Replace (HPR) with the right-hand 6 bits of (v). Cause the punch to respond to (HPR). If j = 0, omit seventh level hole; if j = 1, include seventh level hole.

5. GENERAL THEORY OF OPERATION.

a. GENERAL. - The computer is divided into five basic sections as follows:

(1) INPUT. - Effects insertion of data into the Storage Section.

(2) STORAGE. - Stores information within the computer.

(3) ARITHMETIC. - Performs digital manipulations to accomplish arithmetic and logical operations.

(4) OUTPUT. - Delivers the results of a computation to external devices.

(5) CONTROL. - Interprets the program and directs its execution.

The general features of each of the above systems and the manner in which each system functions with the others in the solution of a program is discussed in the following subparagraphs.

b. PRINCIPAL MULTIPURPOSE REGISTERS. - The X-Register, the Q-Register, and the Accumulator each perform several different functions. These registers collectively are generally referred to as the "arithmetic registers"; however, each has additional functions not associated with arithmetic functions. Brief descriptions of the registers and their functions are given in the following subparagraphs.

(1) X-REGISTER. - The X-Register, X, is a 36-bit flip-flop register which can be complemented. It has two functions:

(a) As an "exchange register", X handles nearly all internal transmissions of words between various sections of the computer.

(b) As an "arithmetic register", X holds the addend, subtrahend, multiplicand, and divisor in the corresponding arithmetic operations.

(2) Q-REGISTER. - The Q-Register, Q, is a 36-bit flip-flop register with shifting properties. It has three functions:

(a) As a "storage register", Q provides storage for a single 36-bit word. It is individually addressed; its address is 1---- (only the first octal digit is of significance).

(b) As an "assembly register", Q is capable of receiving several bits at a time and by shifting can ultimately assemble a 36-bit word. In conjunction with Magnetic Tape Storage, Q assembles a word, two bits at a time during a reading operation, and disassembles a word, two bits at a time during a writing operation.

(c) As an "Arithmetic register", Q holds the multiplier, quotient, and logical multiplier in the corresponding arithmetic operations.

(3) ACCUMULATOR. - The Accumulator, A, is a 72-bit flip-flop register with shifting properties. This register is subtractive in nature. A is logically divided into two halves termed A_R (A-right)and A_L (A-left). The transmissive link to X is from A_R only, although the algebraic sign is carried by A_L. A has two functions:

(a) As a "storage register", A provides storage for a single 36-bit word (in A_R). It is individually addressed; its address is 2----(only the first octal digit is of significance).

(b) As an "arithmetic register", A holds the sum, difference, product, and dividend (and remainder) in the corresponding arithmetic operations. In addition, products may be accumulated up to 72 bits through a combination of multiplication and addition.

c. INPUT SECTION

(1) PUNCHED PAPER TAPE. - The program of instructions and operands is presented to the computer via standard seven level perforated paper tape. The "1" digits are represented by holes in the tape, the "0" digits by the absence of holes. Six of the tape levels store data; the seventh stores loading codes which direct the insertion of the data into storage. Since a single frame of holes across the tape stores six data bits, each word is stored in six-bit segments in six consecutive frames on the tape.

(2) THE TAPE READER. - A photoelectric tape reader is used to transform the data on the perforated paper tape into corresponding patterns of pulses which are then sent to the computer. The output of the reader, for any one frame, consists of six bits of data and may or may not contain a seventh-level hole. A feed pulse, generated each time a frame is read, transfers the contents of that frame to the computer for eventual assembly into a word and separation of the seventh-level (providing it is present) from the data. After three seventh-level holes have been read the computer generates a three bit loading code. The spacing of the seventh-level holes (in frame counts) determines the code.

(3) OPTIONAL INPUT. - Through the use of the input-output registers, IOA and IOB, a great variety of optional input mechanisms operating basically under their own control may transmit data to the computer. These registers communicate directly with the X-Register, and are involved in input operations only as directed by a control program.

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d. STORAGE SECTION. - The principal function of the Storage Section, or computer memory, is to provide the Arithmetic and Control Sections with the operands and instructions required during the execution of a program. A secondary function of the section is to provide temporary storage for the intermediate and final results of the computations.

The Storage Section is composed of four classes of uniquely addressed storage locations (Magnetic Drum Storage, Magnetic Core Storage, the Accumulator, and the Q-Register) and the Magnetic Tape Storage System. Individual addresses are used to identify the storage positions of the four storage classes MD, MC, A, and Q. A total of 17,410 15-bit addresses is assigned to these classes, as follows:

Storage Class	Addresses in Octal Notation
MC	00000-01777
Q	1----
A	2----
MD (Group 4)	40000-47777
MD (Group 5)	50000-57777
MD (Group 6)	60000-67777
MD (Group 7)	70000-77777

Addresses 02000-07777 and 30000-37777 are not used and result in a fault if included in a program. Words are stored on magnetic tape in blocks of 32 words each. The words in the blocksare not individually addressed, but the blocks are located by their relative positions on the tape as specified by a "block count". The magnetic tape system (four magnetic tape units) can store up to 262,144 words.

A storage reference to MD, MC, A or Q is made on the basis of the 15-bit storage address held in the Storage Address Register, SAR, at the time of the reference. The address held in SAR is interpreted by the Storage Class Translator and Storage Class Control. The proper one of the four addressed classes is then selected and the necessary signals are sent to the proper locating circuit. The proper locating circuit then locates the specific storage position called for by (SAR). Reference is made to the four magnetic tape units by programmed instructions which select the proper tape unit, and specify the number of blocks to be involved in the MT operation.

(1) STORAGE ADDRESS REGISTER. - The Storage Address Register (SAR) holds the 15-bit storage address during any storage reference other than a reference to the Magnetic Tape Storage System. SAR receives addresses from PAK, UAK, and VAK and communicates with Storage Class Control, MD, MC, the X-Register and PAK.

(2) STORAGE CLASS CONTROL. - The Storage Class Control (SCC) and its translator (SCT) determine the class of storage referenced by translating the higher-order three bits of the address in SAR. Thus it may determine that MD, MC, A, or Q is being referenced.

(3) MAGNETIC DRUM STORAGE SYSTEM. - The Magnetic Drum Storage System is a medium access speed storage medium consisting of a magnetic drum, a locating circuit, and reading and writing circuits. The system stores, in parallel, 16,384 words in four groups of 4096 words each. The maximum access time is approximately 34 milliseconds, the time taken in one drum revolution. The drum addresses are 40000 through 77777.

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(a) MAGNETIC DRUM. - The magnetic drum is a precision aluminum cylinder 17 inches in diameter and 12 inches long. Its surface is coated with a magnetizable iron oxide. A housing in which the magnetic heads are mounted covers the surface of the drum. The magnetic heads which read and write on the drum's surface have their gaps about 0.002 inch from the surface and provide non-contact recording of the digital data. At one end of the drum a soft steel band containing the milled Timing Track and Mark Track is affixed. The timing notches are spaced 80 to the linear inch and the mark notch (one only) corresponds to one of the timing notches. The mark notch denotes the electrical beginning of the Timing Track. The data heads are arranged in a spiral fashion to permit an axial spacing of 16 to the inch.

(b) LOCATING CIRCUIT. - The MD Locating Circuit is composed of the Group Detector and Group Selector, the Angular Index Counter (AIK), the Angular Coincidence Detector, and the Location Control unit. It is the function of these circuits to identify the referenced group (one of four) and then to select the proper angular address (one of 4096). An interchangeable Address Interlace Chassis (4-, 8-, 16-, 32-, and 64-interlace patterns may be chosen) is interposed between the Angular Coincidence Detector and the lower-order 12 stages of SAR for the purpose of selecting proper time intervals between consecutive MD storage references (to accommodate inter-reference sequences) rather than having to wait a full drum revolution between references.

(c) ACCESS CONTROL. - The MD Access Control (MDAC) provides 125 kc TIMING PULSES to the Location Control and determines whether a reading or writing operation is ordered; it reacts accordingly on receipt of a COINCIDENCE PULSE from the Angular Coincidence Detector and sends a RESUME signal to the Control Section at the completion of the storage reference.

(4) MAGNETIC CORE STORAGE SYSTEM. - The Magnetic Core Storage System is a non-volatile rapid-access storage medium consisting of 36 magnetic core matrices, an address selection system, a 36-bit input register, and an access control. The system stores 1024 36-bit words in parallel and has an access time of 10 microseconds.

(a) MAGNETIC CORE MATRICES. - Each matrix consists of 1024 cores wired in a 32 by 32 array so that the wires all lie in the same plane. The cores are held in position by the wires which are terminated on a square printed-circuit frame. Each core is a small toroid of material exhibiting a nearly rectangular hysteresis loop. Five wires pass through each core: a horizontal X wire, a vertical Y wire, a diagonal S wire, a horizontal I_1 wire, and a vertical I_2 wire. Each core thus wired, forms a bi-stable device which can store a "1" or a "0" depending on the direction of magnetization.

(b) ADDRESS SELECTION. - The circuits used in address selection consists of the address Register, the Read/Write Pulse Generators, and the Read/Write Enable Generators. These circuits select a particular pair of X and Y wires so that reading or writing is executed at a particular coordinate location.

(c) INPUT REGISTER. - The 36-stage Magnetic Core Input Register acts both as an input register and restoration register. During a writing operation a 36-bit word from the X-Register is transmitted to the Input Register from which the word is entered into the Magnetic Core Storage at the address specified by SAR. During a reading operation, the word being transferred from a MCS address to the X-Register is held temporarily in the Input Register so that the information at the reference address can be rewritten.

(d) ACCESS CONTROL. - The Magnetic Core Access Control receives INITIATE READ MC or INITIATE WRITE MC signals from the Control Section of the computer. Upon receipt of such a signal, the Access Control generates a sequence of operations to effect the incoming command. These sequences control the reading, writing and restoration operations within the Magnetic Core Storage System.

(5) REGISTER STORAGE. - In many programs it is convenient to use the Q-Register and the Accumulator as one-word storage media. SAR through SCC and the Arithmetic Registers Access Control (ARAC) can select A or Q as a storage register if the u-address or v-address of an instruction so dictates. Q has the address 1---- and A the address 2----. The right-hand four octal digits in each case are immaterial since only the left-hand octal digit designates the respective register.

(6) MAGNETIC TAPE STORAGE SYSTEM. - The Magnetic Tape Storage System does not have each word individually addressed as in the foregoing discussions on MD, MC, Q, and A. Rather, the words are stored in blocks of 32, and one or more of four program instructions must be used to read or write a block (note that at least 32 words must be read or written during a Magnetic Tape Storage reference). The addressing procedure involves a "block count" to arrive at the proper block followed by a reading or writing sequence in which the information in one or more blocks may be transferred. The system consists of four magnetic tape units, a locating circuit, and a sequence control.

(a) MAGNETIC TAPE UNITS. - The storage medium in this system is magnetic tape. The tape is divided into six tracks: two carry timing marks which generate LINE PULSES, two carry one bit and the last two carry a second bit. Each mark is carried twice in non-adjacent tracks so that a flaw in the tape does not obliterate data. Because of the redundant nature of bit storage, 18 lines of tape (a line is an area at right angles to the length of the tape) are necessary to accommodate one 36-bit word. Since each block contains 32 words, 576 lines are needed in each block. The lines are spaced 100 to the inch and between blocks there is a short blank space containing no data or timing marks.

The tape transport units hold about 1200 feet of tape and a complete scan takes approximately five minutes. Each tape holds 2048 blocks of words or 65,536 words. The four units, then, store 262,144 words. The tapes are driven at 45.5 inches per second being held on counter-revolving reels which share the same axis. The tapes can be stopped from full speed within the interblock space.

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(b) LOCATING CIRCUIT. - Each tape unit has an associated locating circuit consisting of a Line Counter (LK), a Word Counter (WK), a Block Counter (BK), and asociated control stages. LK and WK are additive counters, and BK is a subtractive counter. LK counts LINE PULSES as the tape moves, and, when

it reaches a decimal count of 18, an end-carry signal advances WK by one. An end carry signal from WK, after reaching a count of 32 (decimal), subtracts one from BK. When the count in BK reaches zero, a signal is issued which stops the tape and indicates this action to the Control Section. Therefore, to locate a specific block, a "block count" is entered in BK such that, when reduced to zero by the movement of the tape, the desired block is located and a reading or writing operation can be initiated. Similarly, during a reading or writing operation, the number of referenced blocks are specified and the tape is stopped when the block count is exhausted.

(c) SEQUENCE CONTROL. - The Magnetic Tape Sequence Control (MTSC) synchronizes the reading and writing operations of the selected MT unit with that of the computer. During the reading sequence MTSC directs the reading from each line (two bits) into Q and then shifts Q twice. This is executed 18 times at which time the word is assembled in Q and a transfer from Q to MC is effected. During writing operations MTSC controls a similar sequence which transfers the word from MC to Q and disassembles the word by writing from Q and shifting Q two-bits at a time. The writing and shifting is executed 18 times thus placing the word in MT storage. Note that MTSC is not involved in tape positioning instructions.

(d) INSTRUCTIONS. - Four program instructions relate to the operation of the Magnetic Tape Storage System; these are: Advance Magnetic Tape (66jn-), Back Magnetic Tape (67jn-), Read Magnetic Tape (64jnv), and Write Magnetic Tape (65jnv). The first two are used to position the tape starting from a known position. The "j" selects one of the four units (OMT, 1MT, 2MT, or 3MT). The "n" designates the number of blocks which the tape is to be advanced or backed. The second two instructions are used for reading and writing. The "j" again designates the tape unit. The "n" designates the number of blocks to be read from or written into. The "v" designates the starting address in MC to which or from which the information is to be transferred.

e. ARITHMETIC SECTION. - The Arithmetic Section performs the arithmetic operations of addition, subtraction, multiplication, and division as well as some strictly logical operations such as shifting, logical addition (bit-by-bit addition), and logical multiplication (bit-by-bit multiplication). The section contains the X-Register, Q-Register, Accumulator, the Shift Counter and its control, and the Arithmetic Sequence Control.

(1) X-REGISTER. - As an arithmetic register, X holds the addend, subtrahend, multiplicand, and divisor in the corresponding arithmetic operations. In addition, during a logical multiplication, X may be considered as holding the multiplier; the actual bit-by-bit multiplication is carried out by a transmission from Q, $Q' \rightarrow X'$.

(2) Q-REGISTER. - As an arithmetic register, Q holds the multiplier and quotient in the corresponding arithmetic operations. During a logical multiplication, Q may be considered as holding the multiplicand during the transmission $Q' \rightarrow X'$. The shifting property of Q is utilized in both multiplication and division.

(3) ACCUMULATOR. - As an arithmetic register, A holds the sum, difference, and product in the corresponding arithmetic operations. In the division operation, A initially holds the dividend, and at the completion of the division

operation A holds the non-negative remainder R. The shifting property of A is utilized in multiplication, division, and in the scale factor operation. The Accumulator is basically subtractive; an operand in being transferred from X to A is automatically complemented and subtracted. During a transfer from X to A the modulus is converted from $2^{36}-1$ to $2^{72}-1$ except in "split" operations.

(4) SHIFT COUNTER. - The Shift Counter, SK, used to keep track of the number of shifts in arithmetic operations. Physically, SK is the seven lower-order stages of SAR (since SAR is not used as an address register during an arithmetic sequence, SAR is free to perform this second function). Associated with SK is the Shift Counter Control, SKC, which governs its sequence.

(5) ARITHMETIC SEQUENCE CONTROL. - The Arithmetic Sequence Control, ASC, controls the operations of the Arithmetic Section upon command from the Control Section. ASC generates sequences of subcommands, each subsequence being dependent on the command received from the Control Section. At the end of the subsequence, control is returned to the Control Section.

f. OUTPUT SECTION. - The basic output devices of the ERA 1103 Computer are an electric typewriter and a high-speed tape punch. In addition, optional output equipment may be employed using the input-output registers IOA and IOB. The two basic devices are connected to the computer by the basic Output System in such a manner that a 6-bit character held in X may be recorded either by the typewriter (when a PRINT instruction is called for) or by the high-speed punch (when a PUNCH instruction occurs). Under program control, optional output devices may be connected to the computer and receive data via the input-output registers IOA and IOB.

(1) TYPEWRITER. - The Typewriter Register (TWR) receives from X and temporarily stores each 6-bit character during its recording. The Typewriter Control (TWC) receives the order to PRINT from the Control System, translates the 6-bit character held in TWR, and activates the proper one of 50 different typewriter operations.

(2) HIGH SPEED PUNCH. - The High Speed Punch Register (HPR) receives from X and temporarily stores each 6-bit character during its recording in the punch mode. It also stores the factor "j" which controls the punching of a seventh-level hole. The High Speed Punch Control (HPC) receives the order to punch and directs the transfer of the character onto a single line of tape. If "j" = 1, HPC also directs the punching of a seventh-level hole.

(3) OPTIONAL OUTPUT. - By the use of a programmed sequence of instructions, output data from the computer can be sent to a variety of suitable output devices via IOA and IOB.

g. CONTROL SECTION. - The Control Section exerts the directing influence over the activities of the computer by controlling the timing of the various operations of the computer. The Control Section receives the instructions which the computer is to carry out; interprets them, and directs their execution upon the operands specified. The computer must be manually started, but can stop automatically or be manually stopped. Besides being automatically controlled by a program of instructions, it can be manually controlled from the Supervisory Control Panel which contains all the necessary controls and indicators for manually operating (and maintaining) the equipment.

(1) MASTER CLOCK. - All the activities which take place within the computer, except for certain ones in the magnetic tape and output sections, are synchronized by a central timing system, called the Master Clock. During NORMAL computer operation, the clock generates 500 kc CLOCK PULSES based on TIMING PULSES from the Magnetic Drum Storage System and, after exerting certain controlling influences over them, supplies them to circuits throughout the computer. During TEST operations, a 500 kc oscillator may be used instead of the drum as the basic source of timing pulses.

The principal circuits of the master clock system, and the functions they serve, are as follows:

(a) TEST OSCILLATOR. - Generates a continuous series of timing pulses at a rate of 500 kc.

(b) CLOCK SOURCE SELECTOR (CSS). - Selects either the MD system or the TEST OSCILLATOR, depending upon manual selections made by the operator, as the source of timing pulses for the clock.

(c) CLOCK RATE CONTROL (CRC). - Controls the rate at which pulses leave the clock. During test operations, CRC permits the operator to select any of six different pulse rates. During NORMAL operation, it automatically selects the 500 kc pulses from the MD System.

(d) PULSE DISTRIBUTOR CONTROL (PDC). - Starts and stops the flow of CLOCK pulses from CRC to the Main Pulse Distributor in response to signals received from other sections of the computer.

(2) MAIN PULSE DISTRIBUTOR. - The Main Pulse Distributor, MPD, receives CLOCK pulses from PDC and distributes them, in successive cycles of from four to eight pulses, to the Command Timing Circuits. The distributor supplies each of the pulses cyclicly on its eight output lines. In an eight pulse cycle, all the output lines are used and the pulses are designated, in the order of their generation, MP0 through MP7. The selection of a particular cycle is made on the basis of the operation code held in the Main Control Register, MCR. Each code selects the cycle which will permit its performance in the least possible time.

(3) PROGRAM ADDRESS COUNTER. - The Program Address Counter, PAK, is a 15-stage additive counter which is used to generate successive addresses at which the instructions of the computer's program can be found. During computation, the address in PAK is referred to each time an instruction word is to be obtained from the computer memory; PAK can thus be thought of as guiding the computer through the instructions of the program being run. The starting address of a computation may be manually inserted into PAK before the START button is pushed; if this is done, computation will begin by picking up the instruction stored at that address. If PAK is not manually preset, it will automatically be set to either MD address 40000 or MC address 00000 depending on other starting selections that are made. Once computation is started, PAK then generates consecutive addresses at which succeeding instructions in the program can be found. If a jump instruction appears in the program and its execution calls for a jump to be made, the following events occur: (1) the jump address (i.e., an address to which the Control Section must now refer in extracting the next instruction) is inserted into PAK; (2) the Control Section picks up the next instruction from the jump address specified by PAK and advances PAK by one; and (3) thereafter,

PAK generates consecutive addresses, starting from the jump address, until another jump occurs or until a stop instruction appears.

(4) PROGRAM CONTROL REGISTERS. - The Program Control Registers, PCR, receive each instruction and temporarily store it during its execution. The registers consist of the Main Control Register, MCR, the U-Address Counter, UAK, and the V-Address Counter, VAK. Each instruction sent to PCR consists of a 6-bit operation code, which is stored in MCR; a 15-bit u-address portion, which is stored in UAK; and a 15-bit v-address portion, which is stored in VAK. Each instruction is obtained from some 36-bit storage location as specified by PAK.

(5) MAIN CONTROL TRANSLATOR. - The Main Control Translator, MCT, is composed of a principal and an auxiliary translator. Its principal translator receives a 6-bit operation code from MCR and produces a single prime operation code enable on one of its 44 output lines. Its auxiliary translator receives enables from the principal translator, from MCR, and from various other circuits in the computer, and produces composite or conditional enables. Output enables from both translators in MCT are utilized throughout the Control Section, but mainly in the Command Timing Circuits, CTC, and the Main Pulse Distributor, MPD. In CTC, the MCT enables are used in the selection of the sequence of commands which are needed to execute the instruction currently in MCR. In MPD, the MCT enables are used in the selection of the MAIN PULSE, MP, cycle required for the operation.

(6) COMMAND TIMING CIRCUITS. - The Command Timing Circuits, CTC, combine each operation enable, from the Main Control Translator, with the corresponding MP cycle, from MPD, to produce a discrete sequence of commands which executes the specified operation. CTC receives two or more of the pulses MP0 through MP5, and MP6 and MP7, along with each operation enable. It distributes pulses MP0 through MP5 as commands which execute the operation. It reads the succeeding instruction from storage into X on MP6, then transfers the instruction from X into PCR on MP7.

(7) REPEAT SEQUENCE CONTROL. - When a Repeat Instruction (75jnw) is executed, a repeat sequence is set up in the Repeat Sequence Control, RSC. The controlling functions of this repeat sequence depend on the values of "n" and "j" in the Repeat Instruction and the nature of the instruction following the Repeat. In general, the RSC sequence (1) notifies Control that a repeat operation is in progress; (2) causes additional commands to be generated on MP5 during the execution of the repeated instruction (these commands determine whether another execution of the instruction should be carried out and therefore, the usual MP 6 omitted, or they determine that the repeat operation should be terminated); and (3) initiates the Repeat Termination routines. (RSC may be rendered inoperative by certain jump and stop instructions.) The nature of the repeat operation and the specific functioning of RSC is outlined in the following paragraph.

During the execution of the Repeat Instruction, the right-hand 15-bits of (F_1) are replaced by "w"; the instruction to be repeated is transmitted to PCR (and its operation code held there until the repeat operation is terminated); the factor "jn" is stored in PAK; PAK is then complemented, and a repeat sequence is initiated in RSC. The RSC sequence then tests to see if the "n" of the

Repeat Instruction is zero or not. If n = 0, the RSC sequence is immediately terminated, and no execution of the instruction in PCR is carried out; rather Control is directed to go to F_1 for the NI. If n ≠ 0, the RSC sequence advances MPD to 7, SAR is cleared, MPD advances and the instruction in PCR is executed. Whether it is then repeated or not depends on the value of n and the nature of the instruction itself. If the execution of an instruction does not create a condition which can terminate the repeat sequence (as a jump or stop), RSC advances PAK and tests the new value of "n". If n ≠ 0, RSC advances the execution addresses of the instruction as specified by the initial value of "j" in the 75 jnw instruction:

If j = 0, RSC does not advance the "u" or "v" address

If j = 1, RSC advances the "v" address by one

If j = 2, RSC advances the "u" address by one

If j = 3, RSC advances both the "v" and "u" addresses by one.

RSC also sets MPD to 7 (omits MP 6, thereby retaining the instruction to be repeated in PCR). On MP 7, SAR is cleared; MPD then advances, and another execution of the instruction is carried out. This procedure continues until "n" executions have been made, or until some condition arises in the execution of the instruction which terminates the repeat sequence. The manner in which the repeat sequences of the various instructions are terminated is shown on the table on Page B-98, APPENDIX B.

6. APPENDIX A.

Each instruction in the Computer's repertoire is also listed in APPENDIX A, CONTENT OF REGISTERS, at the end of this volume. This appendix explains the effect, that the execution of each instruction has on the content of the A and Q Registers and the MD and MC Storage Locations, for various types of storage class selections that may be chosen as each instruction's execution addresses.

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SECTION 2

OPERATION

1. GENERAL.

The total operation of the ERA 1103 Computer System is not performed by one person but by a group operating as a team. Generally, three types of persons are involved; these are: operators, maintenance personnel, and programmers. The maintenance personnel are responsible for turning on the power, performing the routine maintenance tests, isolating and correcting machine malfunctions, and shutting down the equipment. The operator is responsible for operating the system (after application of power) from the Supervisory Control Panel, preparing the external equipment for operation, and changing tapes in the Magnetic Tape Storage System. The operator's control of the system via the Supervisory Control Panel is usually in the NORMAL mode. The programmer may operate the system from the Supervisory Control Panel in the course of "debugging" a program. In doing so, it will be necessary to use the TEST mode as well as the NORMAL mode. The following paragraphs cover the total operation in the normal order starting with the system completely shut down. All referenced plates are in Volume 6.

2. TURNING ON THE EQUIPMENT.

a. MAIN POWER DISCONNECT. - Check to see that the DRUM DRIVE MOTOR switch (Plate 5-19) and the BLOWER DRIVE MOTOR switch (Plate 5-24) are set to the ON position. Then set the MAIN POWER DISCONNECT switch (Plate 2-1) to the ON position. The drum and blower motors will start.

b. MAIN POWER SUPPLY. - The following step-by-step procedure applies power to all sections except the Magnetic Core Storage System. The controls referred to are mounted on the MAIN POWER CONTROL PANEL (Plate 2-2).

STEP 1. Turn the SEQUENCE LIMITING switch to the OPERATE position.

STEP 2. Press the NORMAL ON-OFF button. The power application cycle timer starts running immediately and the TIMER ON indicator lights. The remaining POWER SEQUENCE indicators (INIT. SEQ., LOW HEATER, FULL HEATER, BIAS, and POS. VOLTAGES) are successively illuminated as shown in the following table.

Indicator	Time
TIMER ON	0 sec.
INIT. SEQ.	24 sec.
LOW HEATER*	34 sec.
FULL HEATER	2 min., 34 sec.
BIAS	2 min., 54 sec.
POS. VOLTAGES	3 min., 14 sec.

*The HEATER HOURS meter starts running at this time.

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At the end of the power application cycle, the TIMER ON indicator is extinguished but the other indicators remain illuminated. During the cycle the VOLTAGE FAULT indicators (-80, -25, -15, and +5) should be disregarded.

STEP 3. Press the CLEAR POWER SUPPLY FAULT button if any voltage fault indicators remain on after the POS. VOLTAGES indicator is illuminated. Failure to extinguish indicates an actual malfunction.

STEP 4. Check the 220 VAC on all three phases and the 110 VAC by turning the A-C VOLTAGE switch to each position. PHASE A, PHASE B, and PHASE C should read 220 VAC, and 110 A-C should read 110 VAC.

STEP 5. Check the d-c voltages at each position of the D-C VOLTAGE switch. The meter must read ±5 percent of the indicated voltage.

In the event the power application cycle timer is at the POS. VOLTAGES end of the cycle (due to a previous emergency stop or a manual shut-down via the SEQUENCE LIMITING switch), it is necessary either to go through an automatic shut-down cycle and then a turn-on cycle or to go through a manual turn-on using the SEQUENCE LIMITING switch.

c. MAGNETIC CORE POWER SUPPLY. - The procedure for turning on the MC Power Supply for normal operation is described below. The controls used in this procedure are mounted on the MC power panel (see Plate 2-3).

STEP 1. Turn the sequence limiting switch to OPERATE.

STEP 2. Press the NORMAL ON-OFF button. The timer will start running and the TIMER ON indicator will glow. The remaining power sequence indicators on the MC power control panel will then illuminate in a definite timed sequence which is shown in the chart listed below. The times shown are the approximate elapsed times after the NORMAL ON-OFF button is pressed. Disregard any voltage fault indications until the operate indicator glows.

Indicator	Time
TIMER ON	0 sec
INIT. SEQ.	24 sec
LOW HEATER	34 sec
FULL HEATER	2 min 34 sec
BIAS	2 min 54 sec
POS. VOLTAGE	3 min 14 sec
OPERATE	3 min 34 sec

STEP 3. Turn the A.C. VOLTAGES switch to each of its positions. At each switch position the A.C. VOLTAGES meter should indicate the voltages labelled at the switch position.

STEP 4. Turn the D.C. VOLTAGES switch to each of its positions. At each switch position the D.C. VOLTAGES meter should read between ±5 per cent of the voltage labelled at the switch position.

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d. MANUAL OPERATION OF POWER SUPPLIES. - Under certain conditions it is desirable to turn on the Main Power Supply or MC Power Supply manually, i.e., to step through the power sequence manually not using the timer. The procedure is as follows.

STEP 1. -Turn the sequence limiting switch to OFF.

STEP 2. Press the NORMAL ON-OFF button. The timer will start running and the TIMER ON indicator will glow. After 24 seconds the INIT. SEQ. indicator will glow. Although the timer is running, it will not start the power sequence with the sequence limiting switch in the OFF position.

STEP 3. Turn the sequence limiting switch to the right through its marked positions and allow the sequence limiting switch to rest at each of its positions the prescribed amount of time. Minimum times are listed.

At Position	Allow
LOW HEATER	10 sec
FULL HEATER	2 min
BIAS	20 sec
POS. VOLTAGE	20 sec
OPERATE	20 sec

STEP 4. Perform Steps 3 and 4 of Paragraph c above.

e. WARM-UP TIME. - After completing the turn on procedure outlined above, allow the equipment to warm up at least 30 minutes before computation is initiated.

3. PREPARATION OF MT UNITS.

a. TAPE THREADING PROCEDURE. - A Magnetic Tape Unit is shown in Plate 2-4. The numerical call-outs in this photograph identify the various components and controls referred to in the following step-by-step procedure.

STEP 1. Set the STANDBY (1) and POWER (2) switches to their "down" positions. Turn the SELECTOR switch (3) to either one of the S (Stop) positions.

STEP 2. Remove the two empty tape reels (4). The outer tape reel is removed by depressing the outer spring loaded finger (5) and pulling the reel out. Remove the inner tape reel by depressing both inner and outer spring loaded fingers and pulling the reel out.

STEP 3. Both inner and outer tape reels are identical and hence are interchangeable. Position one of the reels so that the opening in its reel flange is visible from the front. The reel's threading pin (6) is then also visible. Loop a prepared tape (see Paragraph 2, Section 3, Volume I) around the reel by turning the reel clockwise. Be sure that the magnetic (dull) side of the tape is outermost. Also make certain that the tape is securely fastened to the reel before starting to completely fill the reel. When this reel, which is to be used as the inner reel, is filled, the tape should be hanging free from its left side.

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STEP 4. Depress both inner and outer spring loaded fingers, and mount the filled inner reel onto the hub (7) so that the reel's front face (the one showing the threading pin) is visible. When the inner reel is in position over the inner portion of the hub, move the reel counter-clockwise until it locks over the hub. Releasing the inner spring loaded finger completes the locking action of the hub to the inner reel.

STEP 5. Mount the empty outer reel on the hub in the same manner, i.e., so that its threading pin is visible from the front.

STEP 6. Attach the tape to the empty outer reel by securing the free end of the tape to the outer reel's threading pin in the same manner as was done in loading the inner reel, magnetic side out. Be sure that the tape is not twisted while being looped from one reel to the other.

STEP 7. Turn the outer reel counter-clockwise and wind the tape around it until the tape is securely fastened to the reel.

STEP 8. Having thus firmly attached the tape to each reel, pull out approximately three feet of the tape from the inner reel. The loose tape should then form a loop which hangs downward from the left side of the inner reel and downward from the right side of the outer reel, dull side out.

STEP 9. Thread the tape coming off the outer reel on fixed idlers (8), (9), and (10). Slide the carrier (11) and arm (12) to the left as far as they will go. Slip the tape between carrier idlers (13) and (15) and fixed idler (14). Then loop the tape over the capstan (16) so that the tape's magnetic side (dull) is uppermost. Thread the tape under the magnetic head (17) and over fixed idler (18).

STEP 10. Move the carrier (11) slowly to the extreme right until carrier idlers (19) and (20) extend beyond fixed idlers (21), (22), and (23). Be sure to keep the tape on the idlers which were threaded in Step 9. Thread the tape down between idlers (19 , (20), (21), (22), and (23). Place the tape over the wiper pad (24) and under the lead-in fixed idler (25). (Several folded layers of clean lens tissue should be clamped on the wiper pad.)

STEP 11. Move the carrier to the center of the track by turning the outer reel counter-clockwise while applying a slight clockwise force to the inner reel. This removes all tape slack in the tape handling mechanism.

STEP 12. Carefully examine all points of contact between the tape and idlers to be sure the tape is properly seated in its correct position and does not rub on any of the idler rims.

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b. PROCEDURE FOR AUTOMATIC OPERATION. - After a magnetic tape unit is threaded, the following step-by-step procedure using the MT Unit's manual controls is carried out. The tape is run through the unit several times using its manual controls to insure the unit's proper operation in its automatic mode under

computer control. (In the following procedure "call out" numbers in parentheses are placed after each of the MT unit controls mentioned. These controls can be located on Plate 2-4.)

STEP 1. Set the POWER switch (2) to its "up" position. The POWER ON indicator (26) will glow. Allow the unit to warm up for one minute.

STEP 2. Position the carrier (11) to the center of its track as described in STEP 11 of the threading procedure, subparagraph 3a(1).

STEP 3. Holding the tape reels firmly, set the STANDBY switch (1) to its "up" position.

STEP 4. Slowly release pressure on the reels and allow them to reach their equilibrium positions, thus absorbing any slack in the tape.

STEP 5. Turn the SELECTOR switch (3) to F (Forward). Allow the tape to almost empty from the inner reel onto the outer reel and then turn the SELECTOR switch (3) to either S (Stop) position.

WARNING

STOP THE TAPE'S MOVEMENT BEFORE ALL OF IT HAS EMPTIED ONTO THE OUTER REEL, OTHERWISE THE TAPE WILL BE TORN FROM THE INNER REEL.

STEP 6. Turn the SELECTOR switch (3) to R (Reverse). Allow the tape to almost empty from the outer reel onto the inner reel and then turn the SELECTOR switch (3) to either S (Stop) position.

WARNING

STOP THE TAPE'S MOVEMENT BEFORE ALL OF IT HAS EMPTIED ONTO THE INNER REEL, OTHERWISE THE TAPE WILL BE TORN FROM THE OUTER REEL.

STEP 7. Repeat Steps 5 and 6, leaving the tape so that a portion of its leader is under the reading heads. (The length of the leader varies but it is always at least 10 feet long.)

STEP 8. Allow the magnetic tape unit to warm up for 30 minutes before automatic operation is initiated.

STEP 9. For automatic control of a magnetic tape unit by the computer, turn the SELECTOR switch (3) to A (Automatic).

c. PROCEDURE FOR INITIALLY POSITIONING TAPE. - Before Computation which involves using the Magnetic Tape Storage System is initiated, the magnetic tape in each unit that is to be used must be properly positioned with respect to the unit's head assembly; i.e., the starting point on the tape in each unit must be located beneath the unit's head assembly. A properly prepared tape has the following spacings and arrangement of blocks:

(a) Leader - blank space, at least 10 feet long.

(b) First Error Block - a space in which 580 LINE PULSES are inserted.

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(c) Forward Starting Position - a long blank space between the Error Block and the first Data Block.

(d) Storage Area, subdivided as follows:

1st Data Block
INTERBLOCK SPACE
2nd Data Block
INTERBLOCK SPACE
3rd Data Block

INTERBLOCK SPACE
2040th Data Block

Each Data Block contains 576 LINE pulses and can store 32 36-bit words, and each INTERBLOCK SPACE is a blank space about 3/4" long.

(e) Reverse Starting Position - a long blank space between the last Data Block and the Second Error Block.

(f) Second Error Block - a space in which 580 LINE pulses are stored.

(g) Trailer - blank space, at least 10 feet long.

The objective of the following procedure is to position a tape so that a portion of its Forward Starting Position is under an MT Unit's head assembly. Controls on both the Supervisory Control Panel, SCP, and the MT Unit whose tape is being positioned are employed. All SCP controls, lights and indicators are shown on Plate 5-2 unless otherwise specified. Wherever possible the group in which a particular control on the SCP can be found is also mentioned. MT Unit controls are each identified by call-out numbers in parenthesis, and are shown on Plate 2-4.

	ACTION	EFFECT
STEP 1.	If the NORMAL lights on the SCP, Plate 5-3, are illuminated, push the RELEASE NORMAL button No action is required if TEST has been selected or if no OPERATION MODE Group selection has been made.	NORMAL lights go out; ADVANCE, BACK & STOP buttons on SCP can then be used to manually operate MT Unit.

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	ACTION	EFFECT
STEP 2.	On the MT Unit whose tape is being positioned, make sure that the STANDBY (1) switch is in the "up" position and the SELECTOR (3) switch is set to A (Automatic).	MT Unit properly set for manual control from SCP.
STEP 3.	On the SCP, set the correct MT Unit (0, 1, 2, 3) STOP DISCONNECT switch to the "up" position.	Any missing or extra LINE pulses read from the MT Unit's tape will not stop the tape but will indicate the error; i.e., the MT Unit's (upper) MISSED LP indicator on the SCP will light if an error occurs but tape drive will not stop.
STEP 4.	On the SCP, press the ADVANCE button corresponding to the MT Unit (0, 1, 2, 3) whose tape is being positioned.	Top row of BLOCK COUNTER indicators all light* and the MT Unit's tape is advanced (i.e., tape moves off the inner reel, passes under the head assembly, and winds on the outer reel).
	After the ADVANCE button is pressed, carefully watch the MT Unit's LINE, WORD & BLOCK COUNTER indicators on the SCP.	No activity in these indicators (other than that mentioned above for the BLOCK COUNTER indicators) will be noted until the tape leader has passed under the Unit's head assembly and the Error Block begins to move under the heads. To determine that the Error Block is being read, note the following: a. LINE & WORD COUNTER indicators - top and bottom indicators quickly flash; b. Right-most pair of BLOCK COUNTER indicators-top light goes off, bottom light comes on; c. MISSED LP indicators - top indicator (of pair corresponding to MT Unit) comes on, bottom indicator goes off. This change occurs almost simultaneously with b.

*Only if the MT Unit's BLOCK COUNTER originally contained all zeros; if some other value than zero is stored, the count is merely reduced by one.

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	ACTION	EFFECT
		d. Then, no further change in the activity of these indicators.
	As soon as possible after the activity of the indicators ceases, press the STOP (0, 1, 2, 3) button corresponding to the MT Unit whose tape is being positioned.	Tape movement will stop, and a portion of the blank space between the Error Block and the first Data Block will be beneath the head assembly. The tape is now in its forward starting position.
STEP 5.	On the SCP, return the STOP DISCONNECT switch (set in STEP 3) to its "down" position.	Any missing or extra LINE PULSE read from the Tape will stop the tape and cause a B FAULT. This is shown on the SCP by the lighting of the B FAULT indicator in the A/B FAULT GROUP and the lighting of the MISSING LP indicator.
STEP 6.	On the SCP press the white button associated with the LINE, WORD, & BLOCK COUNTER indicators that have been used.	Counters all set to Zero
STEP 7.	On the SCP, press the white button beneath the MISSED LP indicator that was used to detect Error Block	Top MISSED LP indicator goes out, bottom indicator comes on, and the error condition is removed from the MT Unit's circuitry.

The MT Unit is now completely ready for use in the forward direction under the computer control. The above procedure can also be used to position the tape's Reverse Starting Position under the head assembly if the tape's trailer rather than its leader is initially positioned under the head assembly and the BACK instead of ADVANCE button is pressed in STEP 4.

4. PREPARATION OF INPUT AND OUTPUT DEVICES

a. PHOTOELECTRIC TAPE READER. - The step-by-step procedure for properly loading the Ferranti Photoelectric Tape Reader is listed below. (Refer to plate 2-5, and Figure 2-1.)

STEP 1. Load the tape reel holder with a properly prepared, prewound tape in the following manner:

a. Snap open the hinged member of the reel holder.

b. Place the reel of tape over the spindle on the reel holder such that the tape levels, reading away from you, are in the order 7-6-1-2-feed holes-3-4-5 and the tape feeds from the top of the reel.

c. Snap closed the hinged member of the reel holder.

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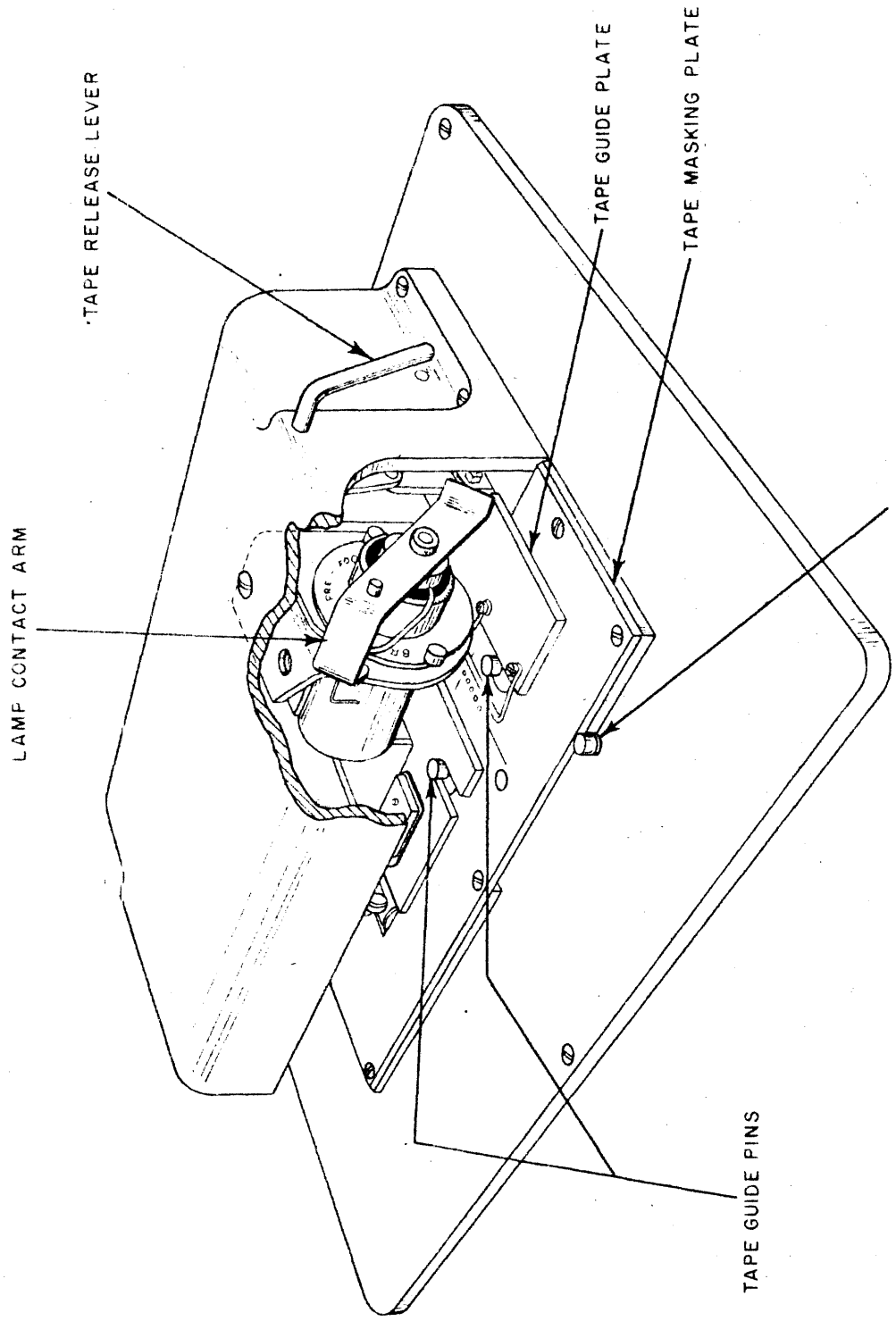

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Figure 2-1. Ferranti Reader Tape Guide Mechanism

STEP 2. Thread the tape through the tape feed mechanism as follows:

NOTE

THE TAPE GUIDE PIN ADJUSTING LEVER SHOULD BE IN THE EXTREME RIGHT-HAND POSITION WITH THE LOCATING PIN ENGAGED IN THE HOLE BENEATH THE TAPE MASKING PLATE. THIS POSITIONS THE TAPE GUIDE PINS FOR A SEVEN-LEVEL TAPE.

a. Turn the tape release lever counter-clockwise to raise the tape guide plate.

b. Allowing approximately 12 inches of leader, thread the tape between the tape masking plate and the tape guide plate and between the tape guide pins, then through the friction drive mechanism. If the tape has been inserted right-side-up, a pair of lines parallel to the direction of tape travel engraved on either side of the feed holes in the masking plate will align with the sides of the feed holes on the tape.

c. Hold the tape in its proper position and rotate the tape release lever fully clockwise to lower the tape guide plate into its normal position.

d. Feed the tape through the reader by hand to bring the first tape frame into reading position. An engraved line on the masking plate marks the reading position.

The Tape Reader is now ready for operation from the Supervisory Control Panel.

b. HIGH SPEED PUNCH. - The threading of the punched tape is illustrated in Plates 5-28 and 5-29. The motor is turned on by setting the toggle switch to the "up" position (Plate 5-28). These two items prepare the punch for operation.

c. OUTPUT TYPEWRITER. - Preparation of the typewriter for operation consists of inserting paper and setting the OFF-ON switch to the ON position (Plate 5-31).

d. OPTIONAL INPUT AND OUTPUT DEVICES. - The preparation for operation of these devices is covered in the individual instruction manuals supplied with the devices.

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5. COMPUTATION

a. GENERAL. - The system is usually operated in the NORMAL mode; however, maintenance personnel and occasionally programmers use the TEST mode exclusively. The NORMAL mode of operation is presented in full, but the TEST mode, being far more complicated, is given only in a general way; a more complete coverage is given in Volume 3, MAINTENANCE.

b. NORMAL MODE OF OPERATION.

(1) BASIC SELECTIONS. - A group of basic selections are made on the Supervisory Control Panel (Plate 5-3) prior to actual operation; these are:

(a) NORMAL. - This selection automatically selects the DRUM as a clock source and HIGH SPEED as a clock rate.

(b) One of the "start" selections, i.e., MD START, or MT START. These are discussed in subparagraph b. (4) below.

(c) One or more, or none, of the manually selective jump selections according to the instructions accompanying the program.

(d) One or more, or none, of the manually selective stop selections according to the instructions accompanying the program.

(e) The contents of the Program Address Counter, PAK, may or may not be altered according to conditions existing in the program.

(f) START. - This selection is made after all basic selections have been made and any other selections or procedures involved have been carried out.

(2) ABNORMAL CONDITIONS AND FAULTS. - The computer cannot be put into operation in the NORMAL mode if an ABNORMAL CONDITION exists (Plate 5-5). All disconnect switches must be in the "down" position. Furthermore, the selection of an ABNORMAL CONDITION after operation has been initiated will result in a fault and cause the computer to stop. In general, if a fault condition arises, the computer is prevented from running, if not yet started; or stopped, if already in operation. However, one fault-producing interlock may be by-passed: this is the low temperature interlock circuit. A key switch in TEST GROUP (Plate 5-5) termed BY-PASS TEMPERATURE INTERLOCK can be used to by-pass the interlock circuit in emergency cases where it is mandatory to complete a program despite an overheating condition (the high temperature interlock circuit still protects the equipment from damage by immediate removal of all power should the temperature condition warrant). For the correction of faults and resumption of operation see subparagraph 5 d below.

(3) PUNCHED TAPE LOADING. - The Ferranti Reader requires a program for its operation. This program, called the Ferranti Loading Routine, is normally stored at the first block of MT Unit 0 although it may be stored on the drum or on one of the other tape units. The latter two storage locations, however, have disadvantages. In the case of drum storage the routine may inadvertenly be erased and, should the routine be stored on a tape unit other

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than MT Unit 0, a greater number of selections must be made at the Supervisory Control Panel before starting.

The step-by-step procedure for loading into the computer a bioctal coded tape containing seventh-level loading instructions (assuming that the Ferranti Loading Routine as given on pages 5-88, 5-89, and 5-90 of Volume 3 has been previously stored on block 1 of MT Unit 0) is as follows:

STEP 1. Position MT Unit 0 to the beginning as described in subparagraph 3c above.

STEP 2. Place the tape in the tape reader and prepare the tape reader as described in subparagraph 4a above.

STEP 3. Select MT START.

STEP 4. Push the START button on the Supervisory Control Panel.

The Ferranti Loading Routine will then be transferred into Rapid Access Storage starting with address 00000. After this has been done the computer will automatically take address 00000 for its next command. The tape reader will start and the tape in the reader will be loaded into the computer.

Tapes other than those coded in bioctal with seventh-level coding may be loaded into the computer by using a suitable Ferranti loading routine. (See Figure 4-14, Volume 2 for Ferranti Reader timing with respect to the computer.)

(4) COMPUTATION. - Computation can be initiated in two different ways: an MD START or an MT START. Both starts have some preliminary steps in common. The controls are located on the Supervisory Control Panel (Plates 5-2, 5-3, and 5-5 in Volume 6) unless otherwise indicated.

STEP 1. Set the F_1 switch (Plate 5-5) to 00000 position unless the instructions accompanying the program call for a 40001 setting.

STEP 2. Check that all ABNORMAL CONDITION switches are in the "down" position and that the BY-PASS TEMPERATURE INTERLOCK key switch is in the "off" position.

STEP 3. Prepare those external devices to be used by the program as described in subparagraphs 4b, 4c, and 4d above.

STEP 4. Prepare those Magnetic Tape units which will be used, as described in paragraph 3 above. Prepare for "automatic" operation.

STEP 5. Press the NORMAL button. The NORMAL indicators in OPERATING GROUP and OPERATION MODE GROUP, the DRUM indicator in CLOCK SOURCE GROUP, and the HIGH SPEED indicator in OPERATING RATE GROUP will illuminate.

STEP 6. Press those SELECT JUMP buttons called for in the program's instructions. The associated SELECTIVE JUMPS indicators will illuminate.

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STEP 7. Press those SELECT STOP buttons called for in the program's instructions. The associated indicators (immediately above SELECT STOP buttons) will illuminate.

After these preliminary steps, the selection of MD START or MT START can be made. The following effects will be noted for each selection:

MD START

MD START indicator (START SELECTION GROUP) is illuminated.
READY indicator (OPERATING GROUP) is illuminated.
PROGRAM ADDRESS COUNTER is set to octal 40000.
MAIN PULSE DISTRIBUTOR is set to 6.

MT START

MT START indicator (START SELECTION GROUP) is illuminated.
READY indicator (OPERATING GROUP) is illuminated.
PROGRAM ADDRESS COUNTER is set to octal 00000.
MAIN PULSE DISTRIBUTOR is set to 0.
"U" ADDRESS COUNTER is set to octal 00001.
MCR (Main Control Register) is set to octal 64.

If the instructions accompanying the program call for a setting of the PROGRAM ADDRESS COUNTER other than that obtained automatically, press the "clear" (white) button and enter the binary value by pressing the "set" (black) buttons.

At this point, the system is ready for operation. Press the START button (OPERATING GROUP) which illuminates the OPERATING indicator and initiates the computation.

c. TEST MODE OF OPERATION. - In the TEST mode the number of optional selections that can be made are so numerous that only a general procedure will be given in this section. (Maintenance, Volume 3, contains a thorough treatment of the optional selections and the consequence of each.) The Magnetic Tape units and the external equipment are prepared as in the NORMAL mode, described previously.

After making the desired optional test selections, the following step-by-step procedure is followed (specific test procedures may introduce minor deviations from the procedure below):

STEP 1. Press the TEST button. The associated TEST indicator in OPERATION MODE GROUP is illuminated.

STEP 2. Press the DRUM button or the OSC (oscillator) button. The associated indicator is illuminated. (Note that DRUM is not automatically selected as in the NORMAL mode.)

STEP 3. Select the desired clock rate in OPERATING RATE GROUP. (Note that HIGH SPEED selection is not automatically made as in the NORMAL mode.)

STEP 4. Select the desired manual jumps (SELECTIVE JUMPS GROUP) and manual stops (SELECTIVE STOPS GROUP).

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STEP 5. Select one of the "starts": MD START, or MT START. The MASTER CLEAR signal is produced at this point after which any desired flip-flop may be changed. (The X-REGISTER and the Magnetic Tape counters are not cleared by the MASTER CLEAR signal).

STEP 6. Press the START button. If HIGH SPEED, AUTOMATIC STEP CLOCK, or AUTOMATIC STEP OPERATION was selected in STEP 3, the operation starts immediately. If MANUAL STEP CLOCK, MANUAL STEP DISTRIBUTOR, or MANUAL STEP OPERATION was selected in STEP 3, the START selection merely lights the OPERATING indicator; each step of the operation must be initiated by pressing the STEP button (OPERATING GROUP).

While in the TEST mode, the accidental or intentional pressing of any "set" button (except those associated with the PROGRAM ADDRESS COUNTER) will alter the state of the associated flip-flop.

d. RESTORATION OF OPERATION AFTER STOPS. - The computer ceases operation at the occurrence of a programmed Manually Selective Stop, a FORCE STOP, an emergency stop, or a fault condition. The stops by classes are discussed in subparagraphs (1) through (4) below, together with the steps necessary to resume operation.

(1) PROGRAMMED STOPS.

(a) MANUALLY SELECTIVE STOP - The Manually Selective Stop instruction, 56jv, stops the computer operation if the programmed j (0, 1, 2, or 3) agrees with the selection made on the Supervisory Control Panel (no button selection is provided for j = 0; the computer will always stop in this case). Whether or not a stop occurs at the execution of this instruction, the next instruction will be taken from the v-address. When a stop occurs the OPERATING indicator is extinguished and the appropriate SELECTIVE STOP indicator (red) is illuminated. To resume operation, press the START button. During the stop, any stop or jump selections may be changed.

(b) FINAL STOP. - The Final Stop instruction, 57--, indicates the end of the program and all selections are dropped except NORMAL or TEST and those selections automatically made by the NORMAL selection. Also the SELECT STOP indicators and SELECTIVE JUMP indicators, if illuminated, will remain. To resume operation, a new program must be initiated, or the previous program can be altered and re-run.

(2) FORCE STOP. - An unscheduled stop of the computer can be effected by pressing the FORCE STOP button. The OPERATING indicator is extinguished and the FORCE STOP indicator is illuminated. After the condition which prompted the stop has been corrected, operation is resumed by pressing the START button.

(3) EMERGENCY STOPS.

(a) MANUAL EMERGENCY STOP. - In cases of extreme emergency, such as a fire, pressing either EMERGENCY STOP button (one is located on the Main Power Supply Panel and one on the Magnetic Core Power Supply Panel) removes all

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voltages from the equipment except that to the power application cycle timer circuits of the two power supplies. Since all power is removed, a program in process is halted and cannot be immediately resumed. To resume operation after correction of the fault, it is necessary to return both cycle timers (Main Power and Magnetic Core) to their starting positions by pressing the respective NORMAL ON-OFF buttons. Then each NORMAL ON-OFF button must be pressed again to apply power. After the proper warm-up interval, the operating selections on the Supervisory Control Panel can be re-made and the operation resumed. It should be noted that such a stop could destroy information or could render some circuits inoperative; it may be well to perform routine maintenance to insure proper operation and then reload the program and data into the system.

(b) AUTOMATIC EMERGENCY STOPS. - The high temperature thermostats, cabinet door interlocks and sail switches in the cooling cabinet are in the same circuit as the EMERGENCY STOP buttons. Therefore, a temperature condition in excess of 120°F at any point, improper bypassing of door interlocks, or failure of the air blower causes the same condition as pressing an EMERGENCY STOP button. For resumption of operation see subparagraph (a) immediately above.

The cabinet door interlocks are bypassed in the following manner. Press the interlock by-pass button mounted on the frame adjacent to the door handle. While pressing the interlock by-pass button, open the door and pull out the interlock plunger located near the upper corner of the door opening. This plunger switch is in a neutral position after opening the door which would open the interlock circuit if the by-pass switch were not held in. After pulling out the plunger, the interlock by-pass switch can be released. To close the door, press (and hold in) the interlock by-pass button on the frame, close the door fully, and release the interlock by-pass button.

(4) FAULT CONDITIONS

(a) A FAULT. - An A Fault results in a stop which manifests itself much like a manually Selective Stop or a Force Stop in that the OPERATING indicator is extinguished and the A FAULT indicator is illuminated rather than a SELECTIVE STOP or FORCE STOP indicator. In addition, the READY indicator is extinguished. The specific fault is indicated by the illumination of one of the following indicators (FAULT INDICATORS GROUP, Plate 5-5):

DIVIDE
SCC (Storage Class Control)
PRINT
TEMP. (Low Temperature - 100°F)
WATER
OVERFLOW (only possible on Multiply Add instruction, 72uv)
ABNORMAL CONDITION - Group X (only if operating in NORMAL mode)

The A Fault does not drop other operating selections so that after correcting the fault, operation can be resumed.

Generally, a DIVIDE, SCC, PRINT, or OVERFLOW indication is derived from a program error. First check the appropriate instructions or operands, and, if these are correct, an actual machine malfunction is the cause and must be

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isolated and corrected. A TEMP. indication is the result of a high air temperature at some point. The high air temperature is indicated by the illumination of one of the amber indicators mounted above the cabinet doors. Corrective measures should be applied immediately unless the urgency for problem results dictates that the BY-PASS TEMPERATURE INTERLOCK key switch should be turned and thus the problem can be continued despite the over-temperature condition. A WATER indication necessitates correcting a water pressure fault (over- or under-pressure condition) before the program can be resumed. An ABNORMAL CONDITION indication usually occurs at the outset of a NORMAL mode of operation unless a Test Disconnect switch has been accidently or intentionally set to the "up" position after operation has been initiated. Movement of the switch to its "down" position will correct the condition. In the correction of some A Faults it is necessary to remake basic selections; in this event, it is mandatory to record the contents of all the principal registers, counters, and the MAIN PULSE DISTRIBUTOR if the operation is to be resumed from the point of the fault. Then, after correction of the fault, the contents of the registers, counters, and MPD must be inserted manually before resuming operation.

After correction of the A Fault, press the CLEAR A FAULT button which in turn illuminates the READY indicator. Finally, press the START button; the OPERATING indicator is illuminated and the operation is resumed.

(b) B FAULT. - A B Fault results in a stop which manifests itself much like a Final Stop in that most selections are dropped. Only the NORMAL or TEST selections and those selections automatically made by the NORMAL selection remain in effect. In addition, the B FAULT indicator and one of the indicators in FAULT INDICATOR GROUP listed below are illuminated.

MCT (Main Control Translator)
VOLTAGE
IO (Input-Output)
MISSING FP (Missing Feed Pulse)
MISSING LP (Missing Line Pulse)

In addition to the above, an external equipment fault may be indicated, in which case the fault indicators shown on Plate 5-4 will be illuminated. These are:

EXTERNAL (in combination with one of the following)
IOA1 READ
IOB1 READ
IOA2 READ
IOB2 READ

Generally, an MCT or IO indication is due to a program error in which case the program in storage or the input tape should be checked for accuracy. If no errors are thus discovered, a machine malfunction is indicated and must be corrected.

A MISSING FP, MISSING LP, or a VOLTAGE indication necessitates corrective maintenance. The MISSING LP may be due to a magnetic tape breakage when operating in the NORMAL mode; such a condition is accompanied by an excessive hum

caused by the high rotational speed of the tape reels. In the case of magnetic tape breakage the STANDBY and POWER switches of the MT unit involved should be immediately set to the "down" (off) position to avoid overheating the tape drive motors. If a tape break occurs under conditions that do not stop the equipment, the FORCE STOP button should be pressed and then the STANDBY and POWER switches set to the "down" position. In either case a new tape must be inserted and the problem re-run from the beginning.

An EXTERNAL fault together with one of the four READ faults indicates that the external equipment is not ready to transmit information to the computer. Such a condition can result from either a program timing consideration or an actual malfunction of the external equipment. In either case corrective action must be taken.

Since many operating selections are dropped at the occurrence of a B Fault, the computation must be started anew. If the contents of any addresses have been altered by the instructions during execution of that part of a program which was completed before the fault, it would be well to re-load the computer before initiating computation.

6. TURNING OFF THE EQUIPMENT.

a. MAGNETIC TAPE UNITS. - The Magnetic Tape Units should be shut down before removing power from the computer. Proceed as follows:

STEP 1. Turn the selector switch to one of the S (Stop) positions.

STEP 2. Set the STANDBY switch to the "down" position.

STEP 3. Set the POWER switch to the "down" position. The POWER indicator is extinguished.

b. EXTERNAL UNITS. - It is recommended that external devices be turned off before removing power from the system.

c. POWER SUPPLY. - Both the Main Power Supply and the Magnetic Core Supply are turned off in the following manner. Press the NORMAL ON-OFF button. The power application cycle timer goes through its automatic shutdown sequence. After approximately two minutes all POWER SEQUENCE indicators will be extinguished. The HEATER HOURS meter stops when the LOW FILAMENT indicator is extinguished.

d. MAIN POWER DISCONNECT. - Set the MAIN POWER DISCONNECT switch to the OFF position. This completes the system shutdown.

SECTION 3

PREPARATION OF TAPES

1. GENERAL

This section describes (1) the basic principles of entering encoded information on paper tapes used for transfer of input data into the computer via a photoelectric tape reader, and (2) methods of writing a timing track on a magnetic tape for use as the storage medium in the Magnetic Tape Storage System.

2. PRINCIPLES OF PUNCHED TAPE PREPARATION

Punched paper tape is a prime input medium for the ERA 1103 Computer System. Standard teletype seven-level tape or equivalent is used. In each tape frame a six-bit portion of a 36-bit word is punched in six tape levels in bioctal code, and one bit of the loading instruction is punched in the seventh level. The following subparagraphs explain the general principles of the tape coding rather than presenting an operating procedure for the Tape Preparation Equipment. The detailed procedure for preparing input tapes using the ERA Tape Preparation Equipment is given in the separate "Tape Preparation Equipment" volume of this series.

a. TAPE NOMENCLATURE. - The following terms are applied to punched paper tapes:

(1) LEVEL. - A tape level is a row of positions parallel to the length of the tape. In a tape moving from left to right the rows are identified, from top to bottom, as follows: 7-6-1-2-sprocket hole-3-4-5. Since the sprocket hole position is not considered a level, the levels are correspondingly numbered 7-6-1-2-3-4-5 with the sprocket hole intervening between levels 2 and 3.

(2) FRAME. - A tape frame is a single column of seven levels and a sprocket hole perpendicular to the length of the tape. The frame position is defined by the sprocket hole.

(3) WORD. - A tape word is a group of six consecutive frames containing an orderly arrangement of 36 bits in levels 6-1-2-3-4-5 and a seventh level pattern embracing the same six frames and the last frame of the previous word.

(4) IDENTITY OF BITS. - A binary "1" is represented as a punched hole, and a binary "0" is represented by the absence of a punched hole.

b. FORM OF ENCODED INFORMATION. - The information encoded on the tape falls into several categories: program instructions, operands, and loading instructions. These are explained in the following subparagraphs.

(1) PROGRAM INSTRUCTIONS. - A program instruction is a 36-bit word composed of three parts: a 6-bit operation code, a 15 bit u-address (this may be replaced by the operators j and n), and a 15-bit v-address (this may be replaced

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by the operator k or the repeat termination address w). An instruction usually is represented in octal notation wherein 12 octal digits represent the 36 bits. As an example of an instruction consider the following:

71 00123 01004

This octal notation would appear in binary as follows:

Operation code u-address v-address

111,001,000,000,001,010,011,000,001,000,000,100

The program instruction is contained in six frames in levels 6-1-2-3-4-5 and is positioned as follows: the first frame contains the two-digit (six-bit) operation code. The second, third, and first half of the fourth frame (levels 6-1-2) contain the u-address. The second half of the fourth frame (levels 3-4-5) and the fifth and sixth frames contain the v-address. The various levels within a frame hold the following octal and binary values: levels 6-1-2 hold the higher order octal digit and the binary coefficients 2^2, 2^1, and 2^0 respectively; levels 3-4-5 hold the lower order octal digit and the binary coefficients 2^2, 2^1, and 2^0 respectively.

(2) OPERANDS. - An operand is a 36-bit combination usually used to express a numerical value with its algebraic sign. As such, the left most bit (2^{35}) is the sign bit, and the remaining 35 bits (2^{34}, 2^{33}, ... 2^0) comprise the number. The operand word is contained in six frames in levels 6-1-2-3-4-5 and is positioned as follows: the bits are arranged in descending powers of 2 with 2^{35} in the level 6 of the first frame and ending with 2^0 in level 5 of the sixth frame.

(3) LOADING INSTRUCTIONS. - There are four loading instructions; these are: Assemble Data, Enter Data, Insert Address, and Check Address. These four instructions are encoded in the seventh level. The code occupies seven frames; six of the frames correspond with the current word and one frame is the last frame of the previous word. The six frames of the current word are identified by the letters A-B-C-D-E-F with A being the first frame and F being the sixth. The F frame of the previous word is termed F' when considered as part of the code concerning the current word. Of the seven letters embracing the code only F, C, D, and F' are used in the loading instruction code. The following table shows the possible combinations of these four frames together with the octal instruction code produced and the resulting loading instruction.

Frame Combination	Octal Code	Loading Instruction
None, F, or F'	00	Assemble Data
F and F'	01	Enter Data
C, C and F, or C and F'	02	Assemble Data
F, C, and F'	03	Insert Address
D	04	Assemble Data
F, D, and F'	05	Check Address

During the assembly of a 36-bit word, six bits at a time, the loading instruction frames are continuously monitored to evaluate the code contained. In actual tape reading, each of the first five frames read produce an Assemble Data

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instruction; however, the sixth frame produces one of the other instructions. Should an Enter Data instruction be recognized, the assembled word is stored. If an Insert Address instruction is recognized, the v-address portion of the assembled word is inserted as the first loading address and the following word (containing an Enter Data instruction) is stored at that address. If a Check Address instruction is recognized, the current address is compared with the v-address portion of the assembled word. If the addresses agree, the loading continues (if an ERA Tape Reader is employed, the next word must contain an Insert Address instruction because the checking procedure destroys the current address in PAK). If the addresses do not agree, the loading operation is stopped. Check Address words are placed periodically in long input tapes to make sure the loading is correctly done.

c. SAMPLE PUNCHED TAPE. - Figure 3-1 shows a sample of tape containing words with all types of data and loading instructions. The sample tape begins with a blank leader (note that just before the first word an F' seventh-level hole is punched), followed by an Insert Address word, a program instruction and two operand words (each with an Enter Data instruction), a Check Address word, and a blank trailer. Note that the check address word contains the address of the word that would normally occupy this position, not the address of the preceding operand word. The leader and trailer should each be at least 12 inches long.

3. MAGNETIC TAPE PREPARATION

a. GENERAL. - One-half inch magnetic plastic recording tape is the basic storage medium of the Magnetic Tape Storage System. Minnesota Mining No. 109A will give satisfactory performance. The tape must be wound, magnetic (or dull) surface out, on reels which are supplied with the equipment. Approximately 1200 feet of tape can be stored on a single reel. The MT System requires four such tapes for full scale operation, one for each of the four magnetic tape units.

b. NOMENCLATURE. - The following terms are used in the tape preparation procedure given in subparagraph d below.

(1) CELL. - A cell is a rectangular area (approximately 0.05 x 0.01 inches) of the magnetic surface of the tape. The cell provides storage for either a binary digit (bit) or a timing signal. The entire area of the cell is magnetized to saturation in one of its two possible polarities to represent "0" bit. To store either a "1" bit or a timing signal in the cell, the cell is magnetized to saturation in the opposite polarity.

(2) CHANNEL. - A channel is a column of cells parallel to the length of the tape. The tape is divided into six channels, each approximately 0.08 inches wide. The channels are numbered consecutively 1-2-3-4-5-6. When the tape is threaded on a magnetic tape unit, the channel nearest the front plate of the outer reel is channel 6; the channel nearest the back plate of the outer reel is channel 1.

(3) LINE. - A line is a row of cells (one in each channel) which is approximately perpendicular to the length of the tape. The line density is 100 per inch. Each line contains six cells, which provide duplicate storage for two bits of a word and a timing signal called a LINE pulse. The lower-order bit

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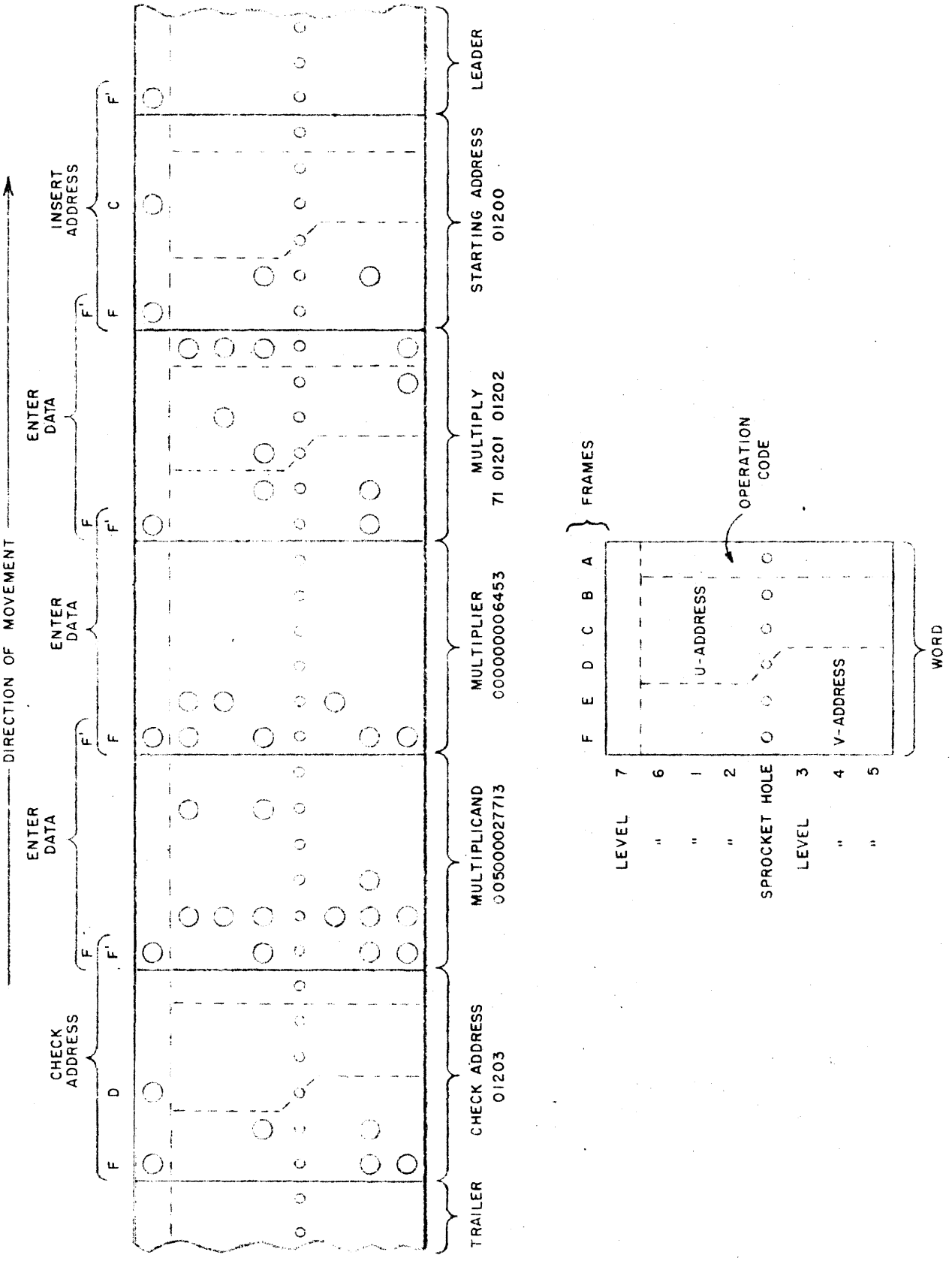

Figure 3-1. Sample Punched Tape.

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occupies channels 2 and 5; the higher-order bit occupies channels 3 and 6. The LINE pulse occupies channels 1 and 4.

(4) WORD. - A word is a group of eighteen consecutive lines. The word thus consists of 36 binary bits and 18 consecutive LINE pulses each recorded twice.

(5) DATA BLOCK - A Data Block is a group of 32 consecutive words. The words follow each other so that within a Data Block no blank portion of tape separates adjacent words. Data Blocks thus contain 576 consecutive lines.

(6) INTERBLOCK SPACE. - An interblock space is a section of blank tape which separates adjacent blocks of words. The interblock space is equivalent to 72 lines.

(7) TAPE ERRORS. - A tape is erroneous if more or less than 576 pulses are present in either of the LINE pulse channels of any Data Block. When the equipment is in operation, the counting of the 576th LINE pulse conditions an error detection circuit that searches for additional LINE pulses for a distance equivalent to 72 lines. If an interblock space is present after the 576th LINE pulse, no fault is detected. If less than 576 LINE pulses are read from a block, the error detection circuit is not conditioned until additional LINE pulses are read from the succeeding block. When the 576th LINE pulse is read the error detection circuit is conditioned, and the next LINE pulse will cause a MISSING LP FAULT. A MISSING LP FAULT is also produced if more than 576 LINE pulse signals are read from the same block. In this case, the reading of an extra LINE pulse during what should be the interblock period causes the error detection circuitry to register the fault condition.

The tape itself may produce a MISSING LP FAULT even though the LINE pulses have been properly written on channels 1 and 4; i.e., tape defects may hinder the reading of LINE pulses or produce spurious signals which are read as LINE pulses.

(8) ERROR BLOCK. - An Error Block is one which contains 580 LINE PULSES. One Error Block is written on each end of a prepared tape. The Error Block on each end of the tape is separated from the Data Blocks by a relatively long space (about 35 feet) which contains no LINE pulses. The Error Blocks cause the tape drive to be stopped when either end of the tape is approached. That is, when a reference is made inadvertently to the MT System to advance or back a particular tape to the point where one of the tape's Error Blocks pass under the magnetic heads, the Error Detection circuits generate the signal STOP MT UNIT J (where J equals 0, 1, 2, or 3) which stops the rotation of the tape reels.

(9) LEADER AND TRAILER. - The first and last ten to fifteen feet of a tape is blank to provide a leader and trailer. The leader and trailer are used to fasten the tape to the reels of each magnetic tape unit. Either the leader or trailer can also provide the extra tape required for threading the tape-handling mechanism once the tape is securely attached to the tape reels.

(10) CONTENTS OF TAPE. - A properly prepared tape contains the following arrangement of blank spaces and areas on which LINE pulses are stored:

(a) Blank Space of about 20 feet (Leader)

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(b) Block of 580 LINE pulses (First Error Block)

(c) Blank Space of about 35 feet (Forward Starting Position)

(d) 2048 blocks each storing exactly 576 LINE pulses, and separated from each other by interblock spaces equivalent to 72 lines.

(e) Blank Space of about 35 feet (Reverse Starting Position)

(f) Block of 580 LINE pulses (Second Error Block)

(g) Blank Space of about 20 feet (Trailer)

c. TAPE INSPECTION. - Only inspected tapes should be used. The method of inspecting magnetic tape is described in detail in Volume III, Section 5, Paragraph 5.

d. PREPARATION PROCEDURE. - To prepare a blank reel of magnetic tape for use in the MT System, it is necessary to duplicate on Channels 1 and 4 on the blank tape the sequence of LINE pulses stored on Channels 1 and 4 of a master tape supplied with the equipment. The following magnetic tape preparation procedure thus causes the LINE PULSES read from consecutive lines on the master tape to be written into corresponding lines and channels on a blank tape. This regeneration may be accomplished in either of two ways: a tape in MT Unit 1, 2, or 3 may be prepared from a master tape in MT Unit 0, or a tape in MT Unit 0, 2 or 3 may be prepared from a master tape in MT Unit 1. To prepare the tapes using either MT Unit 0 or MT Unit 1 for the master tape, it is necessary to alter the contents of jacks J70141 through J70144 and jacks J70151 through J70154 as shown in Table 3-1 below. The second column of the table, headed NORMAL CHASSIS, lists the chassis normally plugged into the jacks. The third column, headed PREP. 1 CHASSIS, lists the units plugged into the jacks to prepare tapes if the master reel is placed in MT Unit 0. The fourth column, headed PREP. 2 CHASSIS, lists the units plugged into the jacks to prepare tapes if the master reel is placed in MT Unit 1. In both cases, a special tape preparation chassis, the 72300 unit, is used.

As an example of how tapes are prepared, a procedure is given below which describes the method of preparing a tape in MT Unit 3 from a master tape in MT Unit 0. All referenced Plates are in Volume 6.

STEP 1. - At Supervisory Control Panel, if the NORMAL light in START SELECTION GROUP is lit, press the START SELECTION GROUP RELEASE button (See Plate 5-3).

STEP 2. - Remove DC power from the Magnetic Tape Cabinet by setting the SEQUENCE LIMITING switch on the Main Power Control Panel (rear of 80000 Cabinet) to the BIAS position (See Plate 2-2).

STEP 3. - Insert chassis into jacks J70141 through J70144 and J70151 through J70154, as shown in the PREP. 1 CHASSIS column of Table 3-1 below.

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Step 4. - Restore power to the Magnetic Tape Cabinet by resetting the SEQUENCE LIMITING switch to the OPERATE position.

Step 5. - Load the master tape onto MT Unit 0 and the blank tape onto MT Unit 3, and run the tapes through the units several times. This procedure is given in Paragraph 3 of Section 2 in this volume.

Step 6. - Position the tape in MT Unit 3 so that about 20 feet (about 1/4 inch thickness) of tape is on the outer take-up reel.

Step 7. - On the MT Unit 0 panel, set the SELECTOR switch to "A", (Automatic), and set the STANDBY switch to the "up" position (see Plate 2-4).

WARNING

WHEN SETTING THE STANDBY SWITCH TO THE "UP" POSITION, HOLD THE TAPE REELS AND RELEASE THEM SLOWLY SO THAT THE TAPE SLACK IS TAKEN UP SLOWLY.

Step 8. - At the Supervisory Control Panel, set the STOP DISCONNECT 0 switch to the "up" position (see Plate 5-2).

Step 9. - Press the ADVANCE 0 button and observe the OLK, OWK, and OBK counter indicators. When these indicators count, press the STOP 0 button.

Step 10. - Clear the MISSED LP 0 flip-flop. Press the BACK 0 button and observe the OBK, OWK, and OLK counter indicators; stop counting when the dead space between the error and data blocks is reached. After about 10 seconds, the counter indicators flash and MISSED LP 0 indicates "1". At this time, press the STOP 0 button. This leaves the MT Unit in the proper starting position for tape preparation, i.e. with a portion of the tape leader under the head assembly in MT Unit 0.

NOTE

THE NEXT THREE STEPS MUST BE EXECUTED QUICKLY. FOR THIS REASON, THESE STEPS SHOULD BE MEMORIZED. IT IS ADVISABLE TO HAVE AN ASSISTANT AT THE SUPERVISORY CONTROL PANEL.

Step 11. - At the Magnetic Tape Cabinet, set the MT Unit 3 SELECTOR switch to "F" (Forward), then the MT Unit 0 SELECTOR switch to "F" (see Plate 2-4).

Step 12. - At the Supervisory Control Panel, observe the OBK, OWK, and OLK indicators. After they flash, the first error block has

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passed. During the 10-second dead space, clear the MISSED LP 0 flip-flop and the OBK, OWK, and OLK counters.

Step 13.- About five minutes later, when the second dead space is reached, the counters will cease and no further indicator activity will be observed. About 10 seconds later, the counter indicators will flash and the MISSED LP 0 flip-flop will indicate "1". At this time, immediately stop the tapes by setting the SELECTOR switches on the MT Unit 0 and MT Unit 3 panels both to the "S" (Stop) position.

To check the prepared tape, set the MT Unit 3 SELECTOR switch to "A" (Automatic) and position the newly prepared tape so that its reverse starting position is under the head assembly in MT Unit 3, as described in Section 2, Paragraph 3. Clear 3WK and 3LK, set $3BK_{11}$ to "1", and press the REVERSE 3 button. If the tape has been incorrectly prepared an error will be detected and the MISSED LP 3 "1" indicator will glow. If there is no error, the tape will stop because of first error block. Position the tape to the forward starting position and repeat the test using the above procedure but pressing the ADVANCE 3 rather than the REVERSE 3 button.

Tapes are prepared from a master reel in MT Unit 1 exactly as for MT Unit 0 except that the chassis are inserted as shown in the column headed PREP. 2 CHASSIS Table 3-1, and the master reel is placed in MT Unit 1. After the first error block has been passed and before the first word block is reached, the 1 MT counters and the 1 MT ERROR flip-flop are cleared and $1BK_{11}$ is set to "1".

TABLE 3-1

INSERTION OF CHASSIS FOR TAPE PREPARATION

CABINET JACK	NORMAL CHASSIS	PREP. 1 CHASSIS	PREP. 2 CHASSIS
J70141	72200	72300	Blank
J70142	72200	Blank	72300
J70143	72200	Blank	Blank
J70144	72200	Blank	Blank
J70151	71500	71500	72200
J70152	71500	72200	71500
J70153	71500	72200	72200
J70154	71500	72200	72200

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APPENDIX A

CONTENT OF REGISTERS

1. GENERAL.

This appendix, Content of Registers, shows, in tabular form and at the completion of the execution of each instruction, the contents of memory locations, the Q-Register, and the Accumulator. The instruction tables are listed in the numerical order of their octal operation codes. The left column, STORAGE CLASS SELECTION, lists the class of storage chosen for the u-address and v-address. The remainder of the table lists the final contents of the memory locations, A, and Q for all cases of storage class selections. Those instructions which do not result in changes contain no tables but, instead, have notes covering these exceptions. A series of dashes in any table position indicates that the memory location or register is not involved in the execution of the instruction. An SCC table entry indicates that an SCC Fault occurs causing the computer to stop.

2. DEFINITION OF SYMBOLS.

A	The 72-bit Accumulator
A_R	The right-hand 36 bits of A
A_L	The left-hand 36 bits of A
Q	The 36-bit Q-Register
MD	Magnetic Drum Storage (16,384 36-bit words)
MC	Magnetic Core Storage (1024 36-bit words)
MT	Magnetic Tape Storage (262,144 36-bit words)
u	The first execution address (i_{29}, i_{28}, ..., i_{15})
v	The second execution address (i_{14}, i_{13}, ..., i_0)
$.2^k$	Left circular shift k places
( )	(Parentheses) Denotes "the content of"
$( )_i$	The "initial content of"
$( )_f$	The "final content of"
( )'	(Prime) The "complement of the content of"

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$\|(\ )\|$	The absolute value of the expression
j	A one digit octal number (u_{14}, u_{13}, u_{12})
n	A four digit octal number (u_{11}, u_{10}, ..., u_0)
D( )	A double extension of the contents of the parentheses
S( )	A single extension of the contents of the parentheses
L(Q)(u)	The bit-by-bit product of (u) and (Q)
L(Q)'(v)	The bit-by-bit product of (v) and the complement of (Q)
$\oplus$	Denotes a bit-by-bit sum without carries.

Instruction: TRANSMIT POSITIVE (TPuv)	Operation Code: 11
Function: Replace (v) with (u).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	(u)	- - -	- - -
	A	No Change	- - -	D(u)	- - -
	Q	No Change	- ---	- - -	(u)
A	MC or MD	- - -	(A_R)	No Change	- - -
	A	- - -	- - -	$D(A_R)_i$	- - -
	Q	- - -	- - -	No Change	(A_R)
Q	MC or MD	- - -	(Q)	- - -	No Change
	A	- - -	- - -	D(Q)	No Change
	Q	- - -	- - -	- - -	No Change

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Instruction: TRANSMIT MAGNITUDE (TMuv)	Operation Code: 12
Function: Replace (v) with the absolute magnitude of (u).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$\lvert(u)\rvert$	- - -	- - -
	A	No Change	- - -	$D\lvert(u)\rvert$	- - -
	Q	No Change	- - -	- - -	$\lvert(u)\rvert$
A	MC or MD	- - -	$\lvert(A_R)\rvert$	No Change	- - -
	A	- - -	- - -	$D\lvert(A_R)_i\rvert$	- - -
	Q	- - -	- - -	No Change	$\lvert(A_R)\rvert$
Q	MC or MD	- - -	$\lvert(Q)\rvert$	- - -	No Change
	A	- - -	- - -	$D\lvert(Q)\rvert$	No Change
	Q	- - -	- - -	- - -	$\lvert(Q)_i\rvert$

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Instruction: TRANSMIT NEGATIVE (TNuv)	Operation Code: 13
Function: Replace (v) with the complement of (u).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$(u)'$	- - -	- - -
	A	No Change	- - -	$D(u)'$	- - -
	Q	No Change	- - -	- - -	$(u)'$
A	MC or MD	- - -	$(A_R)'$	No Change	- - -
	A	- ---	- - -	$D(A_R)_i'$	- - -
	Q	- - -	- - -	No Change	$(A_R)'$
Q	MC or MD	- - -	$(Q)'$	- - -	No Change
	A	- - -	- - -	$D(Q)'$	No Change
	Q	- - -	- - -	- - -	$(Q)_i'$

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Instruction: INTERPRET (IP--)	Operation Code: 14

Function: Let Y represent the address from which CI was obtained. Replace the right-hand 15 bits of (F_1) with the quantity Y + 1. Then take (F_2) as the next instruction.

F_1 and F_2 are MC addresses 00000 and 00001 respectively.

The right-hand 30 bits of (Y) are unaffected by this operation. The contents of A and Q are left unchanged.

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Instruction: TRANSMIT U-ADDRESS(TUuv)	Operation Code: 15

Function: Replace the 15 bits of (v) designated v_{15} through v_{29} with the corresponding bits of (u). The remaining 21 bits of (v) are not to be disturbed.

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$(v_{0-14})_i$; (u_{15-29}); $(v_{30-35})_i$	- - -	- - -
	A	SCC FAULT			
	Q				
A	MC or MD	- - - -	$(v_{0-14})_i$; (A_{15-29}); $(v_{30-35})_i$	No Change	- - -
	A	SCC FAULT			
	Q				
Q	MC or MD	- - -	$(v_{0-14})_i$; (Q_{15-29}); $(v_{30-35})_i$	- - - -	No Change
	A	SCC FAULT			
	Q				

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Instruction: TRANSMIT V-ADDRESS (TVuv)	Operation Code: 16

Function: Replace the right-hand 15 bits of (v), v_0 through v_{14}, with the corresponding bits of (u). The remaining 21 bits of (v) are are not be disturbed.

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	(u_{0-14}) $(v_{15-35})_i$	- - -	- - -
	A	SCC FAULT			
	Q				
A	MC or MD	- - -	(A_{0-14}) $(v_{15-35})_i$	No Change	- - -
	A	SCC FAULT			
	Q				
Q	MC or MD	- - -	(Q_{0-14}) $(v_{15-35})_i$	- - -	No Change
	A	SCC FAULT			
	Q				

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Instruction: EXTERNAL FUNCTION (EF-v)	Operation Code: 17
Function: Select a unit of external equipment and perform the function designated by (v). (No Change in Content of Registers)	

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Instruction: REPLACE ADD (RAuv)	Operation Code: 21
Function: Form in A the sum of D(u) and D(v). Then replace (u) with (A_R).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	$(A_R)_f$	No Change	$D(u)_i+D(v)$	- - -
	A	$(A_R)_f$	- - -	$2D(u)$	- - -
	Q	$(A_R)_f$	- - -	$D(u)_i+D(Q)$	No Change
A	MC or MD	- - -	No Change	$D(A_R)_i+D(v)$	- - -
	A	- - -	- - -	$2D(A_R)_i$	- - -
	Q	- - -	- - -	$D(A_R)_i+D(Q)$	No Change
Q	MC or MD	- - -	No Change	$D(Q)_i+D(v)$	$(A_R)_f$
	A	- - -	- - -	$2D(Q)$	$(A_R)_f$
	Q	- - -	- - -	$2D(Q)_i$	$(A_R)_f$

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Instruction: REPLACE SUBTRACT (RSuv)	Operation Code: 23
Function: Form in A the difference D(u) minus D(v). Then replace (u) with (A_R).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	$(A_R)_f$	No Change	$D(u)_i - D(v)$	- - -
	A	0	- - -	0	- - -
	Q	$(A_R)_f$	- - -	$D(u)_i - D(Q)$	No Change
A	MC or MD	- - -	No Change	$D(A_R)_i - D(v)$	- - -
	A	- - -	- - -	0	- - -
	Q	- - -	- - -	$D(A_R)_i - D(Q)$	No Change
Q	MC or MD	- - -	No Change	$D(Q)_i - D(v)$	$(A_R)_f$
	A	- - -	- - -	0	0
	Q	- - -	- - -	0	0

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Instruction: CONTROLLED COMPLEMENT (CCuv)	Operation Code: 27
Function: Replace (A_R) with (u) leaving (A_L) undisturbed. Then complement those bits of (A_R) that correspond to ones in (v) Then replace (u) with (A_R)	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed				
		$(MC)_f$ or $(MD)_f$				
u	v	u	v	$(A_L)_f$	$(A_R)_f$	$(Q)_f$
MC or MD	MC or MD	$(A_R)_f$	No Change	No Change	$(u)_i \oplus (v)$	- - -
	A	$(A_R)_f$	- - -	No Change	Zero	- - -
	Q	$(A_R)_f$	- - -	No Change	$(u)_i \oplus (Q)$	No Change
A	MC or MD	- - -	No Change	No Change	$(A_R)_i \oplus (v)$	- - -
	A	- - -	- - -	No Change	Zero	- - -
	Q	- - -	- - -	No Change	$(A_R)_i \oplus (Q)$	No Change
Q	MC or MD	- - -	No Change	No Change	$(Q)_i \oplus (v)$	$(A_R)_f$
	A	- - -	- - -	No Change	Zero	Zero
	Q	- - -	- - -	No Change	Zero	$(A_R)_f$

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Instruction: SPLIT POSITIVE ENTRY (SPuk)	Operation Code: 31
Function: Form S(u) in A. Then left circular shift (A) by k places.	

Storage Class Selection for u	Content of Registers and Storage Positions after Operation is Executed.		
	$(MC)_f$ or $(MD)_f$	$(A)_f$	$(Q)_f$
MC or MD	No Change	$S(u) \cdot 2^k$	- - -
A	- - -	$S(A_R)_i \cdot 2^k$	- - -
Q	- - -	$S(Q) \cdot 2^k$	No Change

Instruction: SPLIT ADD (SAuk)	Operation Code: 32
Function: Add S(u) to A. Then left circular shift (A) by k places	

Storage Class Selection for u	Content of Registers and Storage Positions after Operation is Executed.		
	$(MC)_f$ or $(MD)_f$	$(A)_f$	$(Q)_f$
MC or MD	No Change	$\left[(A)_i + S(u)\right] \cdot 2^k$	- - -
A	- - -	$\left[(A)_i + S(A_R)_i\right] \cdot 2^k$	- - -
Q	- - -	$\left[(A)_i + S(Q)\right] \cdot 2^k$	No Change

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Instruction: SPLIT NEGATIVE ENTRY (SNuk)	Operation Code: 33
Function: Form in A the complement of S(u). Then left circular shift (A) by k places.	

Storage Class Selection for u	Content of Registers and Storage Positions after Operation is Executed.		
	$(MC)_f$ or $(MD)_f$	$(A)_f$	$(Q)_f$
MC or MD	No Change	$S(u)' \cdot 2^k$	- - -
A	- - -	$S(A_R)_i' \cdot 2^k$	- - -
Q	- - -	$S(Q)' \cdot 2^k$	No Change

Instruction: SPLIT SUBTRACT (SSuk)	Operation Code: 34
Function: Subtract S(u) from A. Then left circular shift (A) by k places.	

Storage Class Selection for u	Content of Registers and Storage Positions after Operation is Executed.		
	$(MC)_f$ or $(MD)_f$	$(A)_f$	$(Q)_f$
MC or MD	No Change	$\left[(A)_i - S(u)\right] \cdot 2^k$	- - -
A	- - -	$\left[(A)_i - S(A_R)_i\right] \cdot 2^k$	- - -
Q	- - -	$\left[(A)_i - S(Q)\right] \cdot 2^k$	No Change

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Instruction: ADD AND TRANSMIT (ATuv)	Operation Code: 35

Function: Add D(u) to (A). Then replace (v) with (A_R)

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$(A_R)_f$	$(A)_i+D(u)$	- - -
	A	No Change	- - -	$(A)_i+D(u)$	- - -
	Q	No Change	- - -	$(A)_i+D(u)$	$(A_R)_f$
A	MC or MD	- - -	$(A_R)_f$	$(A)_i+D(A_R)_i$	- - -
	A	- - -	- - -	$(A)_i+D(A_R)_i$	- - -
	Q	- - -	- - -	$(A)_i+D(A_R)_i$	$(A_R)_f$
Q	MC or MD	- - -	$(A_R)_f$	$(A)_i+D(Q)$	No Change
	A	- - -	- - -	$(A)_i+D(Q)$	No Change
	Q	- - -	- - -	$(A)_i+D(Q)_i$	$(A_R)_f$

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Instruction: SUBTRACT AND TRANSMIT (STuv)	Operation Code: 36
Function: Subtract D(u) from (A). Then replace (v) with (A_R).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_i$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$(A_R)_f$	$(A)_i - D(u)$	- - -
	A	No Change	- - -	$(A)_i - D(u)$	- - -
	Q	No Change	- - -	$(A)_i - D(u)$	$(A_R)_f$
A	MC or MD	- - -	$(A_R)_f$	$(A)_i - D(A_R)_i$	- - -
	A	- - -	- - -	$(A)_i - D(A_R)_i$	- - -
	Q	- - -	- - -	$(A)_i - D(A_R)_i$	$(A_R)_f$
Q	MC or MD	- - -	$(A_R)_f$	$(A)_i - D(Q)$	No Change
	A	- - -	- - -	$(A)_i - D(Q)$	No Change
	Q	- - -	- - -*	$(A)_i - D(Q)_i$	$(A_R)_f$

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Instruction: RETURN JUMP (RJuv)	Operation Code: 37

Function: Let y represent the address from which CI was obtained. Replace the right-hand 15 bits of (u) with quantity y plus 1. Then take (v) as NI.
(If both u and v refer to MC or MD there is no change in contents of A and Q. If u is Q or A, an SCC FAULT occurs. Also see page A-23.)

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Instruction: INDEX JUMP (IJuv)	Operation Code: 41
Function: Form in A the difference D(u) minus 1. If A_{71} is then 1, continue with the present sequence of instructions; if A_{71} is 0, replace (u) with (A_R) and take (v) as the next instruction.	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
FOR A_{71} = 1					
MC or MD	MC or MD	No Change	No Change	D(u)-1	- - -
	A*	No Change	- - -	D(u)-1	- - -
	Q*	No Change	- - -	D(u)-1	No Change
A	MC or MD	- - -	No Change	$(A)_i$-1	- - -
	A*	- - -	- - -	$(A)_i$-1	- - -
	Q*	- - -	- - -	$(A)_i$-1	No Change
Q	MC or MD	- - -	No Change	D(Q)-1	No Change
	A*	- - -	- - -	D(Q)-1	No Change
	Q*	- - -	- - -	D(Q)-1	No Change

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INDEX JUMP (IJuv) continued

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
FOR $A_{71} = 0$					
MC or MD	MC or MD	$(u)_{i-1}$	No Change	$D(u)_{i-1}$	- - -
	A*	$(u)_{i-1}$	- - -	$D(u)_{i-1}$	- - -
	Q*	$(u)_{i-1}$	- - -	$D(u)_{i-1}$	No Change
A	MC or MD	- - -	No Change	$(A)_{i-1}$	- - -
	A*	- - -	- - -	$(A)_{i-1}$	- - -
	Q*	- - -	- - -	$(A)_{i-1}$	No Change
Q	MC or MD	- - -	No Change	$D(Q)_{i-1}$	$(Q)_{i-1}$
	A*	- - -	- - -	$D(Q)_{i-1}$	$(Q)_{i-1}$
	Q*	- - -	- - -	$D(Q)_{i-1}$	$(Q)_{i-1}$

* see page A-23

PX 71871

Instruction:	THRESHOLD JUMP (TJuv)	Operation Code: 42
Function:	Subtract (u) from (A). If A_{71} is then 1, take (v) as the next instruction; if A_{71} is 0, continue with the present sequence of instructions. Then, in either case, restore (A) to its initial state. (No change in Content of Registers or Storage Positions except for those special cases outlined on pages A-23 and A-35.)	

Instruction:	EQUALITY JUMP (EJuv)	Operation Code: 43
Function:	Subtract (u) from (A). If (A) is then zero, take (v) as the next instruction; if (A) is not zero, continue with the present sequence of instructions. In either case restore (A) to its initial state. (No Change in Content of Registers or Storage Positions except for those special cases outlined on pages A-23 and A-35.)	

PX 71871

Instruction: Q-JUMP (QJuv)	Operation Code: 44
Function: If Q_{35} is 1, take (u) as the next instruction; if Q_{35} is 0, take (v) as the next instruction. Then, in either case, left circular shift (Q) by 1 place.	

Storage Class Selection		Content of Registers and Storage Position after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	No Change	- - -	$(Q)_i \cdot 2$
	A*	No Change	- - -	No Change	$(Q)_i \cdot 2$
	Q*	No Change	- - -	- - -	$(Q)_i \cdot 2$
A	MC or MD	- - -	No Change	No Change	$(Q)_i \cdot 2$
	A*	- - -	- - -	No Change	$(Q)_i \cdot 2$
	Q*	- - -	- - -	No Change	$(Q)_i \cdot 2$
Q	MC or MD	- - -	No Change	- - -	$(Q)_i \cdot 2$
	A*	- - -	- - -	No Change	$(Q)_i \cdot 2$
	Q*	- - -	- - -	- - -	$(Q)_i \cdot 2$

* see page A-23

PX 71671

Instruction:	MANUALLY SELECTIVE JUMP (MJjv)	Operation Code: 45
Function:	If the number j (given by u_{13} u_{12}) is 0, take (v) as the next instruction. If j is 1, 2 or 3 and the correspondingly numbered manual jump-selecting switch is set to "jump", take (v) as the next instruction; otherwise if this switch is not set to "jump", continue with the present sequence of instruction. (No Change in Content of Registers or Storage Positions and see page A-23.)	

Instruction:	SIGN JUMP (SJuv)	Operation Code: 46
Function:	If A_{71} is 1, take (u) as the next instruction; if A_{71} is 0, take (v) as the next instruction (No Change in Content of Registers or Storage Positions and see page A-23.)	

Instruction:	ZERO JUMP (ZJuv)	Operation Code: 47
Function:	If (A) <u>is not</u> zero, take (u) as the next instruction; if (A) <u>is</u> zero, take (v) as the next instruction. In either case leave (A) in its initial state. (No Changes in Content of Registers or Storage Positions and see page A-23.)	

PX 71871

Notes Concerning the Jump Instructions

1. If v refers to A, an SCC FAULT occurs.
2. If v refers to Q, no fault occurs, and Control obtains the NI from (Q). If the (Q) is a legal instruction it will be executed in the normal manner. Unless (Q) is a jump instruction, however, the following will occur: (1) PAK will be advanced and the (Q) will be taken as NI; (2) Control will be directed to Q again after executing the (Q), PAK will be advanced, and (Q) executed again. This process will continue until a FORCE stop is made. PAK advances from 10000 to 11777 and then starts over from 10000, each time, of course, referencing Q as the address of NI.
3. The above remarks also apply to u for the two way jump instruction, QJ, SJ, and ZJ.

Instructions: Q-CONTROLLED TRANSMIT (QTuv)	Operation Code: 51
Function: Form in A the number L(Q)(u). Then replace (v) by (A_R).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$ See Storage Class Selection		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$(A_R)_f$	L(Q)(u)	No Change
	A	No Change	- - -	L(Q)(u)	No Change
	Q	No Change	- - -	L(Q)(u)	$(A_R)_f$
A	MC or MD	- - -	$(A_R)_f$	L(Q) $(A_R)_i$	No Change
	A	- - -	- - -	L(Q) $(A_R)_i$	No Change
	Q	- - -	- - -	L(Q) $(A_R)_i$	$(A_R)_f$
Q	MC or MD	- - -	(Q)	S(Q)	No Change
	A	- - -	- - -	S(Q)	No Change
	Q	- - -	- - -	S(Q)	No Change

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Instruction: Q-CONTROLLED ADD(QAuv)	Operation Code: 52
Function: Add to (A) the number L(Q)(u). Then replace (v) by (A_R).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$ See Storage Class Selection		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$(A_R)_f$	$(A)_i + L(Q)(u)$	No Change
	A	No Change	- - -	$(A)_i + L(Q)(u)$	No Change
	Q	No Change	- - -	$(A)_i + L(Q)(u)$	$(A_R)_f$
A	MC or MD	- - -	$(A_R)_f$	$(A)_i + L(Q)(A_R)_i$	No Change
	A	- - -	- - -	$(A)_i + L(Q)(A_R)_i$	No Change
	Q	- - -	- - -	$(A)_i + L(Q)(A_R)_i$	$(A_R)_f$
Q	MC or MD	- - -	$(A_R)_f$	$(A)_i + S(Q)$	No Change
	A	- - -	- - -	$(A)_i + S(Q)$	No Change
	Q	- - -	- - -	$(A)_i + S(Q)$	$(A_R)_f$

PA 71171

Instruction:	Q-CONTROLLED SUBSTITUTE (QSuv)	Operation Code: 53
Function:	Form in A the quantity $L(Q)(u)+L(Q)'(v)$; then replace (v) with A_R. (The effect of this is to replace the digits of (v) with the digits of (u) where there are 1's in Q.)	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$(A_R)_f$	$L(Q)(u)+L(Q)'(v)$	No Change
	A	No Change	- - -	$L(Q)(u)$	No Change
	Q	No Change	- - -	$L(Q)(u)+S(Q)'$	$(A_R)_f$
A	MC or MD	- - -	$(A_R)_f$	$L(Q)(A_R)_i+L(Q)'(v)$	No Change
	A	- - -	- - -	$L(Q)(A_R)_i$	No Change
	Q	- - -	- - -	$L(Q)(A_R)_i+S(Q)'$	$(A_R)_f$
Q	MC or MD	- - -	$(A_R)_f$	$S(Q)+L(Q)'(v)$	No Change
	A	- - -	- - -	$S(Q)$	No Change
	Q	- - -	- - -	$2^{36}-1$	$2^{36}-1$

PX 71671

Instruction: LEFT SHIFT IN A (LAuk)	Operation Code: 54
Function: Replace (A) with D(u); then left circular shift (A) by k places; then replace (u) with (A_R).	

Storage Class Selection for u	Content of Registers and Storage Positions after Operation is Executed.		
	$(MC)_f$ or $(MD)_f$	$(A)_f$	$(Q)_f$
MC or MD	$(A_R)_f$	$D(u)_i \cdot 2^k$	- - -
A	- - -	$(A)_i \cdot 2^k$	- - -
Q	- - -	$D(Q)_i \cdot 2^k$	$(A_R)_f$

Instruction: LEFT SHIFT IN Q (LQuk)	Operation Code: 55
Function: Replace (Q) with (u); then left circular shift (Q) by k places; then replace (u) with (Q).	

Storage Class Selection for u	Content of Registers and Storage Positions after Operation is Executed.		
	$(MC)_f$ or $(MD)_f$	$(A)_f$	$(Q)_f$
MC or MD	$(u)_i \cdot 2^k$	- - -	$(u)_i \cdot 2^k$
A	- - -	$D(Q)_f$	$(A_R)_i \cdot 2^k$
Q	- - -	- - -	$(Q)_i \cdot 2^k$

PX 71871

Instruction: MANUALLY SELECTIVE STOP (MSjv)	Operation Code: 56
Function: If the number j (given by u_{14}, u_{13}, u_{12}) is 0, stop the computer operation and provide suitable indication. If j is 1, 2, or 3 and the correspondingly numbered manual stop selecting switch is set to "stop", stop the computer operation and provide suitable indication. Whether or not a stop occurs, take (v) as the next instruction. (No Change in Content of Registers or Storage Positions.)	

Instruction: FINAL STOP (FS--)	Operation Code: 57
Function: Stop computer operation and provide suitable indication. (No Change in Content of Registers or Storage Positions.)	

PX 71871

Instruction: PRINT (PR-v)	Operation Code: 61
Function: Replace (TWR) with the right-hand 6 bits of (v). Cause the electric typewriter to print the character to which this code corresponds. (No Change in Content of Registers or Storage Positions.)	

Instruction: PUNCH (PUjv)	Operation Code: 63
Function: Replace (HPR) with the right-hand 6 bits of (v). Cause the punch to respond to (HPR). If j = 0, omit seventh level hole; if j = 1, include seventh level hole. (No Change in Content of Registers or Storage Positions.)	

Instruction: READ MAGNETIC TAPE (RMjnv)	Operation Code: 64
Function: Read n blocks from magnetic tape j (running forward) to 32 n consecutive addresses in MC, starting with v. (No Change in Final Content of Registers. MC Storage Locations modified as explained in Function. Q Register used during data transmissions.)	

Instruction: WRITE MAGNETIC TAPE (WMjnv)	Operation Code: 65
Function: Write on magnetic tape j (running forward) n blocks from 32 n consecutive addresses in MC, starting with v. (No Change in Final Content of Registers or MC Storage Positions. Q Register used during data transmissions.)	

Instruction: ADVANCE MAGNETIC TAPE (AMjn-)	Operation Code: 66
Function: Move magnetic tape j in the forward direction by n blocks. (No Change in Content of Registers or Storage Positions.)	

Instruction: BACK MAGNETIC TAPE (BMjn-)	Operation Code: 67
Function: Move magnetic tape j in the reverse direction by n blocks. (No Change in Content of Registers or Storage Positions.)	

PX 71071

Instruction: MULTIPLY (MPuv)	Operation Code: 71
Function: Form in A the 72-bit product of (u) and (v), leaving in Q the multiplier (u).	

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	No Change	$(u) \cdot (v)$	(u)
	A	No Change	- - -	0	(u)
	Q	No Change	- - -	$(u)_i^2$	(u)
A	MC or MD	- - -	No Change	$(A_R)_i \cdot (v)$	$(A_R)_i$
	A	- - -	- - -	0	$(A_R)_i$
	Q	- - -	- - -	$(AR)_i^2$	$(AR)_i$
Q	MC or MD	- - -	No Change	$(Q) \cdot (v)$	No Change
	A	- - -	- - -	0	No Change
	Q	- - -	- - -	$(Q)^2$	No Change

PA 71071

Instruction: MULTIPLY ADD (MAuv)	Operation Code: 72

Function: Add to (A) the 72-bit product of (u) and (v), leaving in Q the multiplier (u).

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	No Change	$(A)_i + (u) \cdot (v)$	(u)
	A	No Change	- - -	$(A)_i + (u) \cdot (A_L)_i$	(u)
	Q	No Change	- - -	$(A)_i + (u)^2$	(u)
A	MC or MMD	- - -	No Change	$(A)_i + (A_R)_i \cdot (v)$	$(A_R)_i$
	A	- - -	- - -	$(A)_i + (A_R)_i \cdot (A_L)_i$	$(A_R)_i$
	Q	- - -	- - -	$(A)_i + (A_R)_i^2$	$(A_R)_i$
Q	MC or MD	- - -	No Change	$(A)_i + (Q) \cdot (v)$	No Change
	A	- - -	- - -	$(A)_i + (Q) \cdot (A_L)_i$	No Change
	Q	- - -	- - -	$(A)_i + (Q)^2$	No Change

PX 71871

Instruction: DIVIDE (DVuv)	Operation Code: 73

Function: Divide the 72-bit number in (A) by (u), putting the quotient in Q and leaving in A a non-negative remainder, R. Then replace (v) by (Q). The quotient and remainder are defined by:

$(A)_i = (u) \cdot (Q) + R$ where $0 \leq R < |(u)|$.

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.			
		$(MC)_f$ or $(MD)_f$		$(A)_f$	$(Q)_f$
u	v	u	v		
MC or MD	MC or MD	No Change	$\left[(A)_i - R\right]/(u)$	R	$\left[(A)_i - R\right]/(u)$
	A	No Change	- - -	$D(Q)_f$	$\left[(A)_i - R\right]/(u)$
	Q	No Change	- - -	R	$\left[(A)_i - R\right]/(u)$
A	MC or MD	- - -	$\left[(A)_i - R\right]/(A_R)_i$	R	$\left[(A)_i - R\right]/(A_R)_i$
	A	- - -	- - -	$D(Q)_f$	$\left[(A)_i - R\right]/(A_R)_i$
	Q	- - -	- - -	R	$\left[(A)_i - R\right]/(A_R)_i$
Q	MC or MD	- - -	$\left[(A)_i - R\right]/(Q)_i$	R	$\left[(A)_i - R\right]/(Q)_i$
	A	- - -	- - -	$D(Q)_f$	$\left[(A)_i - R\right]/(Q)_i$
	Q	- - -	- - -	R	$\left[(A)_i - R\right]/(Q)_i$

PX 71671

Instruction:	SCALE FACTOR (SFuv)	Operation Code: 74

Function: Replace (A) with D(u) unless u is A. Then left circular shift (A) 36 places and continue shifting until $A_{35} \neq A_{34}$. Replace the right-hand 15 bits of (v) with the number of left shifts, k, necessary to return the final contents of A or $(A)_f$ to the original position. The range of k if u is A is $0 \leq k \leq 71$; if u is MC, MD, or Q, k may be 0 or $37 \leq k \leq 71$. Effectively, the initial contents of A or $(A)_i$, which may be D(u) or D(Q) after the above replacement, is positioned in A_R (with the sign bit represented by A_{35} and the most significant bit by A_{34}) so that $(A)_f = (A)_i \cdot 2^s$.

If $0 \leq k \leq 36$, the Scale Factor, $s = -k$;

if $37 \leq k \leq 71$, $s = 72 - k$. Note that for $0 < k \leq 36$, this positioning scales $(A)_i$ "down"; for $37 < k \leq 71$, $(A)_i$ is scaled "up". If $k = 0$, $(A)_i$ was properly positioned before any shifting operations; if $k = 37$, $(A)_i$ is all ones or zero.

Storage Class Selection		Content of Registers and Storage Positions after Operation is Executed.				
		$(MC)_f$ or $(MD)_f$			$(A)_f$	$(Q)_f$
u	v	u	v_{15-35}	v_{0-14}		
MC or MD	MC or MD	No Change	No Change	k	$D(u) \cdot 2^{72-k}$	---
	A, Q	SCC FAULT				
A	MC or MD	No Change	No Change	k	$(A)_i \cdot 2^{72-k}$, $37 \leq k \leq 71$ $(A)_i \cdot 2^{-k}$, $0 \leq k \leq 36$	---
	A, Q	SCC FAULT				
Q	MC or MD	- - -	- - -	k	$D(Q) \cdot 2^{72-k}$	No Change
	A, Q	SCC FAULT				

PX 7 8271

Instruction: REPEAT (RPjnw)	Operation Code: 75
Function: Execute the following instruction n times modifying the u- and v-addresses of the instruction to be repeated according to the value of j. Afterward, continue the program by the execution of the instruction at F_1 whose v-address is replaced by w. (No change in registers or storage positions except the v-address of F_1 which is replaced by w.)	

Notes:
1. If the repeated instruction is a Threshold Jump (42uv) or an Equality Jump (43uv) and a jump occurs, the quantity j(n-r) from PAK is sent to the Q-Register thus altering its contents.
2. If the n of the Repeat instruction is a zero, the Normal Repeat Termination is executed immediately and the next instruction taken from F_1.

Instruction: EXTERNAL READ (ERjv)	Operation Code: 76
Function: If j = 0, replace the right-hand 8 bits of (v) with (IOA); if j = 1, replace (v) with (IOB). If the external unit utilizes step-by-step operation, advance one step. (No change in registers except as indicated by function above.)	

Instruction: EXTERNAL WRITE (EWjv)	Operation Code: 77
Function: If j = 0, replace (IOA) with the right-hand 8 bits of (v); if j = 1, replace (IOB) with (v). Cause the previously selected unit to respond to the information in IOA or IOB. (No change in contents of registers.)	

PX 71871