THE ERA 1103

COMPUTER SYSTEM

(TYPE 2300C1)

VOLUME TWO

SECTION 4. THEORY OF OPERATION

PX 71871

Remington Rand

ENGINEERING RESEARCH ASSOCIATES DIVISION

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SECTION 4

THEORY OF OPERATION

1. GENERAL

This section discusses the logical operation of the various sections of the ERA 1103 Computer System and those systems which serve as adjuncts to the logical circuitry such as power supplies, power distribution, protective interlocks, and the air cooling system. The emphasis of explanations is placed on "what" each circuit does logically rather than "how" each circuit operates electrically in the accomplisnment of its function. This approach is taken because of the relatively simple electronic principles involved. The system, generally, is built of a great number of similar circuits and stages which are adequately explained in the early paragraphs of this section; thus, a general treatment of computer circuits is given which applies to most of the systems within the equipment. Where unique circuits are encountered, their operation is described at the point of use rather than in the general theory paragraphs.

The system is composed of four major logical sections: the Storage Section, the Arithmetic Section, the Input and Output Section, and the Control Section. Each of these sections is further divided into logical systems which are the subjects of the principal subparagraphs. Each portion of the system is covered by block diagrams beginning with a system block diagram and then going to block diagrams of the system. The block diagrams show only the "decision elements" of the circuits; the strictly signal manipulating stages, such as amplifiers, inverters, pulse transformer, etc., are omitted so that the functions of the circuits are clearly defined. The electronic diagrams which include all components are of two types: the "schematic diagrams" which are basic electrical drawings of physical entities such as chassis and rack units, and the "unit signal diagrams" which are schematic diagrams to which signal names and source and destination information have been added. A schematic diagram is included of each "chassis type", whereas a unit signal diagram is included for each "chassis position" in the system.

The information presented in this section covers only the computer proper and several of its standard input and output devices. Information on optional peripheral equipment can be found in appropriately titled volumes supplied with such devices and includes sufficient information to explain their operation as part of the system.

2. GLOSSARY OF ABBREVIATIONS AND TERMS

A	The 72-bit Accumulator (A_{71}, A_{70}, ..., A_0)
A_L	The left-hand (most significant) 36 bits of A

A_R	The right-hand (least significant) 36 bits of A
AIK	The Angular Index Counter
$\longrightarrow$	(Arrow) Transmit, such as $A_R \rightarrow X$
AR	A ten-stage Address Register, used to store a Magnetic Core address during a reading or writing operation.
ARAC	The Arithmetic Register Access Control
ASC	The Arithmetic Sequence Control
Bit	Binary digit
Core	A small toroid of Ferrite capable of storing a binary digit (bit) equal to "1" or "0", depending upon the direction of remnant magnetization of the toroid.
CRC	The Clock Rate Control
CSS	The Clock Source Selector
CTC	The Command Timing Circuits
D(Q)	A 72-bit word whose right-hand 36 bits are the content of Q and whose left-hand 36 bits are all alike and equal to the left-most bit of the content of Q.
D(u)	A 72-bit word whose right-hand 36 bits are the contents of u and whose left-hand 36 bits are all alike and equal to the left-most bit of the content of u.
F_1	A Fixed Address 00000 (or 40001 depending on a switch setting)
F_2	A Fixed Address 00001
HPC	The High-Speed Punch Control
HPR	The High-Speed Punch Register
I/D	Inhibit/Disturb, a term used to describe circuits which control the selective writing of information in cores.
IR	Magnetic Core Input Register, a 36-stage register that serves as a transfer register between X and the cores.
j	A one-digit octal number (u_{14}, u_{13}, u_{12})
k	The Shift Count (v_6, v_5, ..., v_0)

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L(Q)(u)	A 72-bit word whose left-hand 36 bits are zeros and each of whose right-hand 36 bits is given by the bit-by-bit product of the corresponding bits of Q and u.
L(Q)'(v)	A 72-bit word whose left-hand 36 bits are zeros and each of whose right-hand 36 bits is given by the bit-by-bit product of the corresponding bits of v and the complement of Q.
Matrix	A printed-circuit frame containing 1024 magnetic cores held in a 32 x 32 array by wires threaded through the cores.
MC	A prefix denoting "Magnetic Core", used to designate signals belonging to the Magnetic Core Storage System.
MCAC	Magnetic Core Access Control. A flip-flop control circuit that produces sequences for execution of reading and writing operations in the Magnetic Core Storage System.
MCP	Magnetic Core Pulse, usually followed by a number, such as MCP-1, MCP-2, etc. Basic timing pulse used in the Magnetic Core Access Control.
MCPD	Magnetic Core Pulse Distributor, a three-stage binary counter and distributor that distributes a sequence of five MCP's.
MCR	The Main Control Register, a part of PCR.
MCS	An abbreviation for the Magnetic Core Storage System. This abbreviation followed by a subscript number denotes a particular stage (digit) of MCS. For example: MCS_0 represents the digit which stores the lowest-order bits (2^0), and MCS_{35} represents the digit which stores the highest-order bits (2^{35}).
MCT	The Main Control Translator
MD	The Magnetic Drum Storage System
MDAC	The Magnetic Drum Storage Access Control
MP	A MAIN PULSE, usually followed by a numeral
MPD	The Main Pulse Distributor
MT	The Magnetic Tape Storage System
MTI	The Magnetic Tape Storage Input Register
MTO	The Magnetic Tape Storage Output Register
MTSC	The Magnetic Tape Storage Sequence Control
n	A four-digit octal number (u_{11}, u_{10}, ..., u_0)

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PAK	The Program Address Counter
( )	(Parentheses) Denotes "the content of"
PCR	The Program Control Registers, MCR, UAK, and VAK
PDC	The Pulse Distributor Control
'	(Prime) Denotes "the complement of" such as Q', X', etc.
Q	The 36-bit Q-Register (Q_{35}, Q_{34}, ..., Q_0)
RSC	The Repeat Sequence Control
S(u)	A 72-bit word whose right-hand 36 bits are the content of u and whose left-hand 36 bits are all zeros
SAR	The Storage Address Register
SCC	The Storage Class Control
SCT	The Storage Class Translator
SK	The Shift Counter (SAR_6, SAR_5, ..., SAR_0)
SKC	The Shift Counter Control
TWC	The Typewriter Control
TWR	The Typewriter Register
u	The first execution address (i_{29}, i_{28}, ..., i_{15})
UAK	The U-Address Counter, a part of PCR
v	The second execution address (i_{14}, i_{13}, ..., i_0)
VAK	The V-Address Counter, a part of PCR
w	The v-address portion of a Repeat instruction
X	The X-Register (X_{35}, X_{34}, ..., X_0)
y	The address of the current instruction

3. BLOCK DIAGRAMS

Two types of block diagrams are included in this instruction book. The Block Diagram, ERA 1103 Computer System, in Envelope #1 of Volume 7 is a "higher level" type of block diagram composed of block symbols which represent each

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principle circuit of the computer. The other block diagrams are of the "stage level" type, each composed of block symbols which represent the logical circuits or stages of a particular system of the computer.

The purpose of the Block Diagram, ERA Computer System, is to show each principle circuit of the computer and its relation to the other circuits. On this diagram, the principle sections of the computer are shown as follows: the Storage Section consisting of the Magnetic Drum, Magnetic Core, and Magnetic Tape Storage System is in the top half of the diagram; the Control Section is in the lower left corner; the Arithmetic Section consisting of principle multipurpose registers (X, Q, and A) and various control circuits is in the lower center portion of the drawing; and the Input and Output Section consisting of IOA, IOB, the Photoelectric Tape Reader, the Typewriter System, and the High-Speed Punch System is in the lower right-hand corner.

The purpose of the other block diagrams is to show the operations occurring in each of the principle circuits of the computer system. In these diagrams, each stage or subcircuit that performs a function is assigned a symbol called a "block symbol". If a stage does not perform a function, it is omitted. For example, such stages or subcircuits as inverters, pulse transformer, DC restorers, etc. which merely perform signal manipulation and have no logical purpose are not included in block diagrams. Similarly, if an amplifier is used only to amplify a signal, it is not shown on a block diagram; however, where an amplifier's screen grid bias level is controlled to permit that stage to serve as a gate as well as an amplifier, then the amplifier is represented since it performs a logical operations. It should be emphasized that logical elements on the Block Diagrams (particularly, AND, OR and NOT circuits) are represented on the basis of "what" they do. An analysis of their circuitry on a schematic-type drawing is essential in many cases to an understanding of actually "how" they operate. One or more block diagrams of this type have been made for each system of the computer, depending upon the complexity of the system.

"Stage level" block diagrams are the basic references for this entire section. As the text for each system is read, the system's block diagram (Volume 7) should be at hand and should be studied in conjunction with the text. After each of the principle sections of the computer is studied, the section should be located on the Block Diagram, ERA 1103 Computer System, so that the overall function of the section can be reviewed in relation to the other sections of the computer.

4. UNIT SIGNAL DIAGRAMS AND UNIT CHASSIS SCHEMATIC DIAGRAMS

The ERA 1103 computer is constructed out of a large number of unit chassis of the 74-pin plug-in type and of the 19-inch relay rack mounting type. Although over 400 unit chassis are used, there are only about 85 distinct types of units. This is because one chassis type may be used more than once where circuit similarities exist. In those cases where there are more than one of the same type used, the unit chassis are interchangeable as to their place in the equipment; i.e. chassis of the same type (same unit chassis construction) may be used for various similar functions.

To show how these chassis are interconnected, unit signal diagrams are provided. Essentially a unit signal diagram is the schematic diagram of a unit chassis associated with a particular physical location within the equipment. Thus where two or more identically constructed unit chassis are employed for different applications (as for different stages of a register), their unit signal diagrams will be exactly the same schematically, but will differ in regard to signal designation, inputs and outputs utilized, and origin and destination of signals. Thus, unit signal diagrams are used as circuit diagrams. Each is a schematic of a particular unit chassis, and it shows how that chassis is associated with the rest of the equipment. It is marked to show the sources and destinations of all voltages and signals employed in the chassis. A set of unit signal diagrams is provided for each major section of the equipment. These diagrams are in Volumes 8 through 14, grouped as shown in Table 4-1 below.

TABLE 4-1

LIST OF UNIT SIGNAL DIAGRAMS

Volume	Unit Signal Diagram Sets	Symbol Series
8	Operator's Table	
	Relay Panel	26100
	Photoelectric Tape Reader Power Supply	26200
	High Speed Punch	26300
	Typewriter	26400
	Photoelectric Tape Reader	26700
	Supervisory Control Cabinet	
	Supervisory Control Panel	40000
	Address Monitor	41000
9	Arithmetic Cabinet	10000
10	Control Cabinet	30000
11	Magnetic Core Storage Cabinet	
	Magnetic Core Storage System	55000
	Magnetic Core Storage Power Supply	55000
12	Magnetic Drum Storage Cabinet	60000
13	Magnetic Tape Storage Cabinet	70000
14	Main Power Supply	80000
	Motor-Generator Assembly	88000
	Blower Cabinet	90000

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In the Arithmetic Cabinet, Control Cabinet, Magnetic Core Storage System, Magnetic Drum Storage Cabinet, and Magnetic Tape Storage Cabinet sets, the drawings are arranged consecutively by the symbol series numbers of the 74-pin jacks which mount the chassis. In all other sets, the drawings are arranged consecutively by unit symbol series number or by physical location in the cabinet.

The unit schematic diagrams are found in Volume 15. These are to be used in conjunction with the test procedures explained in the separate ERA 1103 Test Equipment Manual, supplied with the ERA 1103 Test Equipment.

3. DIAGRAM SYMBOLS

a. GENERAL - To conserve space on each of the three kinds of diagrams, block-type symbols are used where possible. Unit signal diagrams and unit chassis schematic diagrams employ special "shorthand symbols" to represent six "standard" circuits, which are used a great number of times throughout the computer. Block diagrams, on the other hand, are composed entirely of block symbols. The symbols used on the block diagrams are different from those used on schematic diagrams. Each symbol by its size, shape, inputs, outputs, and other identifying information represents a particular circuit or a particular logical element. The following subparagraphs explain the basis on which the symbols were chosen, illustrate the various symbols for each type of diagram, and explain what each symbol represents.

b. TUBE ELEMENT CONNECTIONS. - Symbols for the various tube element connections are shown in Figure 4-1. These symbols are used on all three types of diagrams and should be memorized by maintenance personnel.

c. SHORTHAND SCHEMATIC SYMBOLS. - The specific symbols used on schematic and unit signal diagrams are discussed in the following subparagraphs. If a stage or subcircuit is used repeatedly throughout the equipment and is identical wherever it appears, it is called a "standard stage." All standard stages of the same type are identical electrically; e.g., two standard stage flip-flops receiving identical input signals will, theoretically, produce identical outputs. Each of the principal standard stages explained below in detail will always be found represented by its respective "shorthand schematic symbol" when it appears on a schematic-type diagram.

The principal standard stages are flip-flops, cathode followers, inverters, gates, amplifiers, and pulse transformers.

1. FLIP-FLOP - The Eccles-Jordan trigger circuit, or flip-flop, is a form of multivibrator employing direct coupling between the plates and grids of two tubes. The standard flip-flop stage circuit employed in this equipment utilizes a 5963 twin triode tube. A flip-flop circuit is not a free-running multivibrator; rather it is a circuit possessing two stable conditions of equilibrium. For example, in Figure 4-2 below, one condition of equilibrium exists if the triode in side "A" of the flip-flop tube is conducting and the triode in side "B" is cut off, and the other condition of equilibrium exists if the triode in side "A" is cut off and side "B" is conducting. Regardless of which of these two states the flip-flop is in, it will remain in the current state until some external impulse causes it to reverse its state. After such a reversal, the flip-flop will remain in the second state until another external

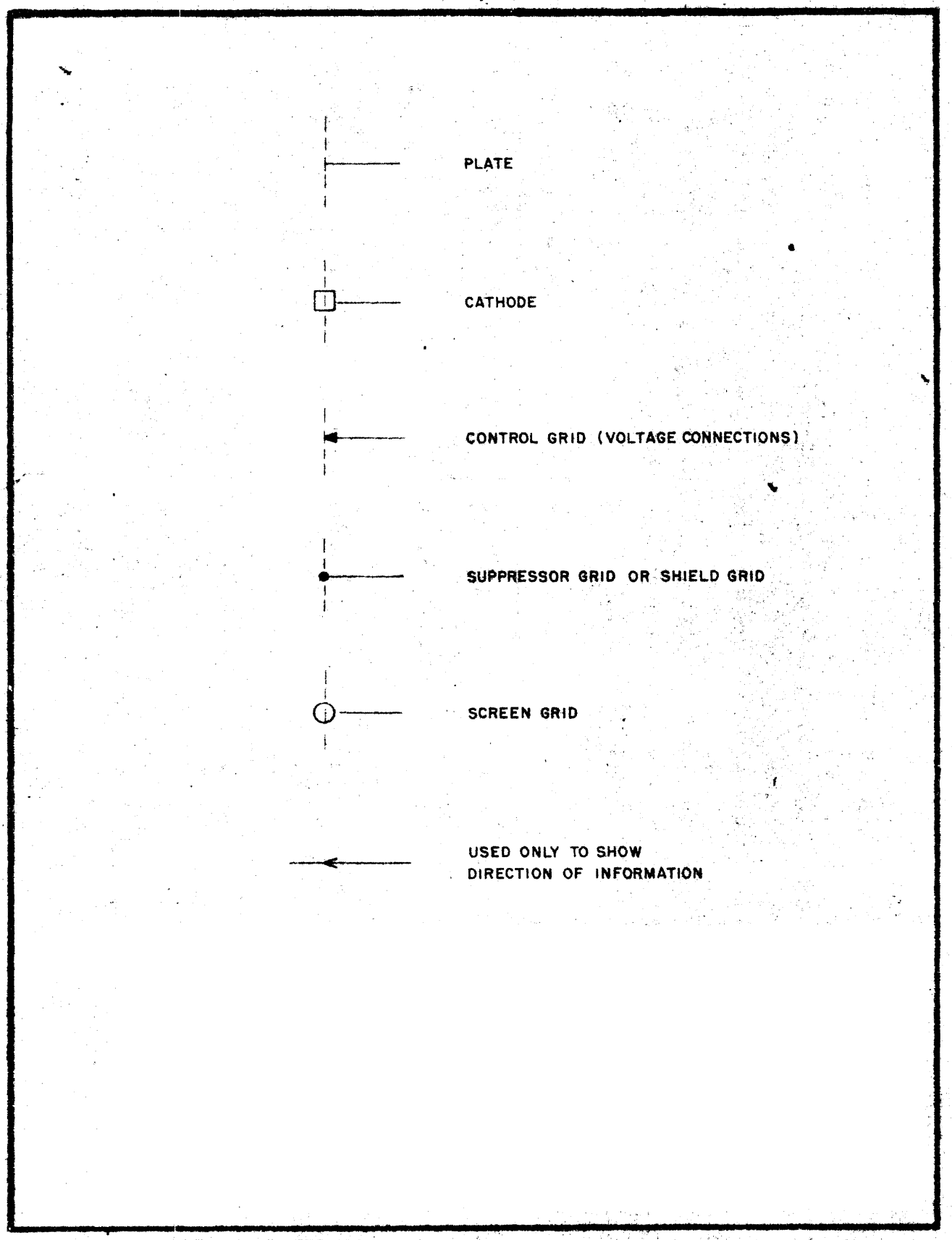

Figure 4-1. Tube Element Connections.

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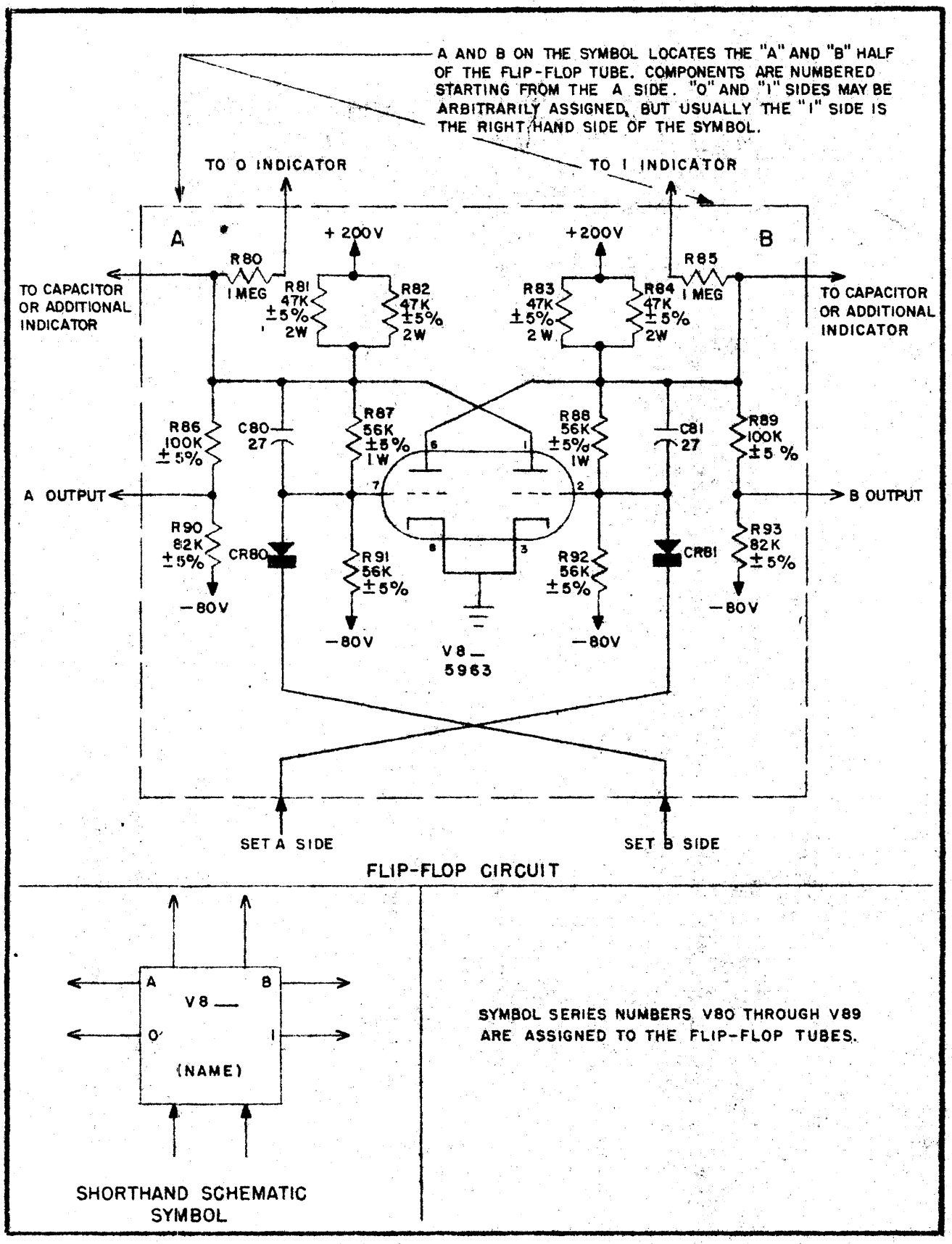

Figure 4-2. STANDARD flip-flop Stage.

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impulse is applied to revert the flip-flop to its first state. The term "flip-flop" is derived from this property of "flopping" from state to state.

Since the circuitry in both halves of the flip-flop is identical, it would seem that equal plate current should flow through the triode in each half when plate voltage is applied; however, slight unbalances will always be present. This unbalance will cause a greater plate current to flow in one of the tube's twin triodes when plate voltage as applied. If the greater plate current flows in the triode in side "A", a proportionally larger voltage drop will occur across plate resistors R83 and R84 in side "B"; therefore, the voltage at the plate of the triode in side "A" will be lower than that at the plate of the triode in side "B". The lower plate potential at the triode in side "A" will be applied to the grid of the triode in side "B" through the voltage divider consisting of R88 and R92. The decreasing potential at this grid will cause a further decrease in the plate current of the triode in side "B". The decrease of current in side "B" will cause a corresponding rise in its plate voltage. This rise in plate voltage will be applied to the grid of the triode in side "A" through the voltage divider consisting of R87 and R91. These incremental changes will continue until a state of equilibrium is reached, at which time the triode in side "B" will be cut off and the triode in side "A" will be fully conducting.

To reverse the state of equilibrium, a negative-going pulse is applied through CR80 to the grid of the triode in side "A". The increase in bias on the grid of this triode causes a drop in its plate current. The drop in plate current causes a rise in plate voltage, which is applied to the grid of the triode in side "B" through the voltage divider consisting of R88 and R92; therefore, the rise in plate voltage causes the triode in side "B" to start to conduct. This triode, when conducting, has a low plate voltage which is applied to the grid of the triode in side "A" through the voltage divider consisting of R87 and R91. The reduced voltage at the grid of the triode in side "A" drives that tube closer to cut-off and the triode in side "B" to heavier conduction. The process continues until the triode in side "A" cuts off and that in side "B" fully conducts. This condition represents the second state of equilibrium.

The shorthand schematic symbol for the standard flip-flop stage is also shown on Figure 4-2. Usually the "A" side of the flip-flop is called the "0" state and the "B" side is called the "1" state. The input line on the "0" side of the flip-flop symbol indicates an input signal to set the flip-flop to "0"; the input line to the "1" side indicates a similar input to set the flip-flop to "1". When the flip-flop is in the "1" state, the "1" output shown on the "1" side of the symbol is positive, and when in the "0" state the output on the "0" side is positive.

It is sometimes desirable to simply reverse the state of a flip-flop by an input signal. This is done by applying a "trigger" signal simultaneously to both input lines through isolation crystals outside the flip-flop circuit. The sample circuit shown in Figure 4-8 includes a trigger input line, connected to

CR05 and CR06. A negative COMPLEMENT X pulse on this line is received, through the crystals, by both sides of the flip-flop. The signal has no direct effect on the non-conducting triode, but proceeds to cut off the conducting triode. As a result, the state of the flip-flop is reversed, in the manner described above.

2. CATHODE FOLLOWER. - The standard cathode follower stage is essentially an impedance-matching or impedance-lowering device which is capable of producing power gain. A triode vacuum tube (1/2 5963) is employed, with the plate tied to +150 vdc and the cathode tied through a resistance to -80 vdc. The output is taken across the cathode resistor. The circuit for this stage and its shorthand schematic symbol are given in Figure 4-3. The particular side, A or B, of the 5963 tube used is included in the tube's symbol series number.

3. INVERTER. - The standard inverter circuit stage and its shorthand schematic symbol are shown in Figure 4-4. This circuit is used to reverse the polarity of the input signal. A single triode (1/2 5963) is employed, and the particular side, A or B, of the 5963 tube is included in the inverter's symbol series number.

4. GATE. - The standard gate circuit stage shown in Figure 4-5 is a pentode (7AK7) which permits the passage of signal pulses applied to the control grid when an enabling voltage is present coincidentally on the suppressor grid. The screen grid is connected to +100 vdc if no screen grid connection is shown. The shorthand schematic symbol of this stage is also given in Figure 4-5.

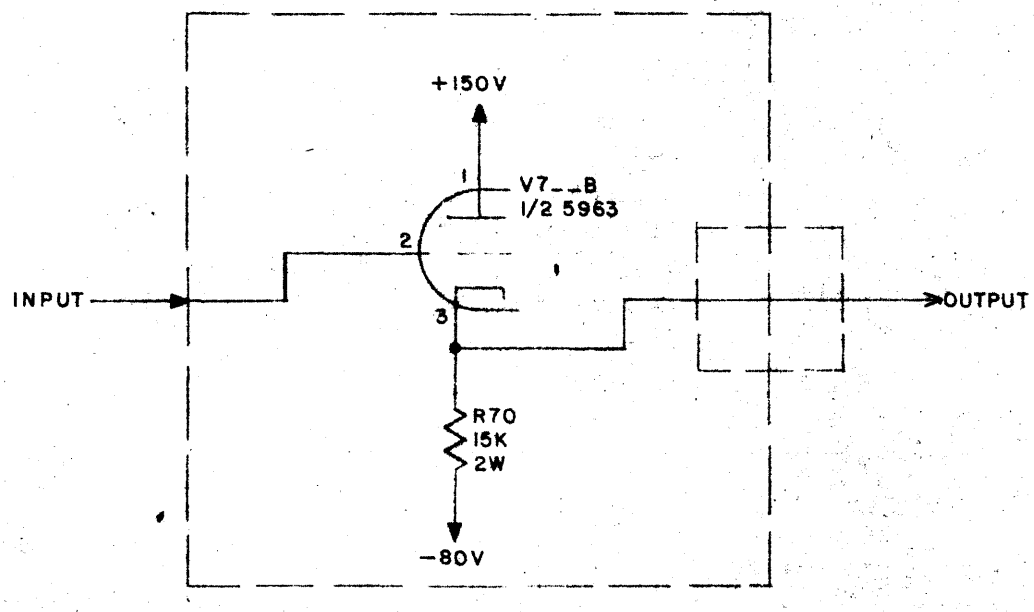
5. AMPLIFIER. - The standard amplifier stage shown in Figure 4-6 uses a 6AN5 tube. This type of amplifier is used to produce voltage gain. As shown in Figure 4-6 if the shorthand schematic symbol for this type of amplifier does not show a screen grid connection, the screen grid is connected to +80 vdc.

6. PULSE TRANSFORMERS. - Standard pulse transformer stages are used primarily for impedance matching and phase inversion. Transformer number and winding ratios as well as the shorthand schematic symbols for each type used are shown in Figure 4-7.

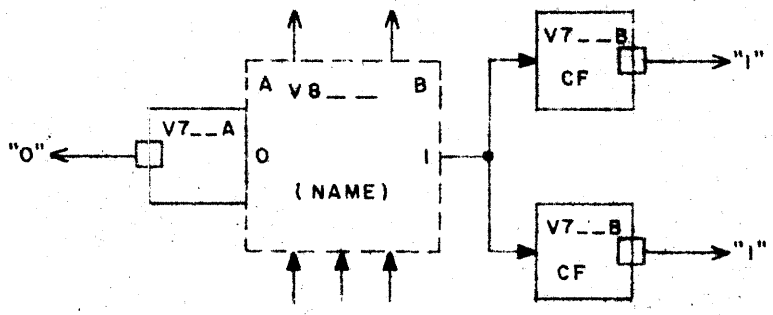
7. SUMMARY. - To illustrate how some of these shorthand schematic symbols are used, a portion of a typical schematic-type diagram is shown in Figure 4-8.

d. BLOCK SYMBOLS. - Each "block symbol" on a block diagram represents some circuit which functions as a logical element of a system, i.e., contributes in some way to "what" the system is doing. Block symbols are assigned to various circuits, therefore, on the basis of logical function. Usually different circuits performing the same functions are represented by the same block symbol. Where possible, each block symbol is identified by a tube symbol series and unit jack number so that the actual circuitry it represents can be found in the unit signal diagrams.

Figure 4-9 illustrates the block symbols used on the block diagrams of this book. Each symbol contains some type of abbreviation as G, A, FF, etc., which identifies the stage it represents. Some also contain supplemental information such as a name, which further identifies its function on the block diagram; e.g. the block symbol for Clock Pulse Distributor, Stage I flip-flop is



CATHODE FOLLOWER CIRCUIT



SHORTHAND SCHEMATIC SYMBOL *

SYMBOL SERIES NUMBERS V70 THROUGH V79 AND V90 THROUGH V99 FOLLOWED BY "A" OR "B", ARE ASSIGNED TO THE CATHODE FOLLOWER AND INVERTER TUBES.

* WHEN MORE THAN ONE CATHODE FOLLOWER IS USED ON A SINGLE FLIP-FLOP OUTPUT, THE CATHODE FOLLOWER SYMBOLS ARE SHOWN DETACHED FROM THE FLIP-FLOP BLOCK ON SCHEMATIC-TYPE DIAGRAMS

Figure 4-3 STANDARD Cathode Follower STAGE

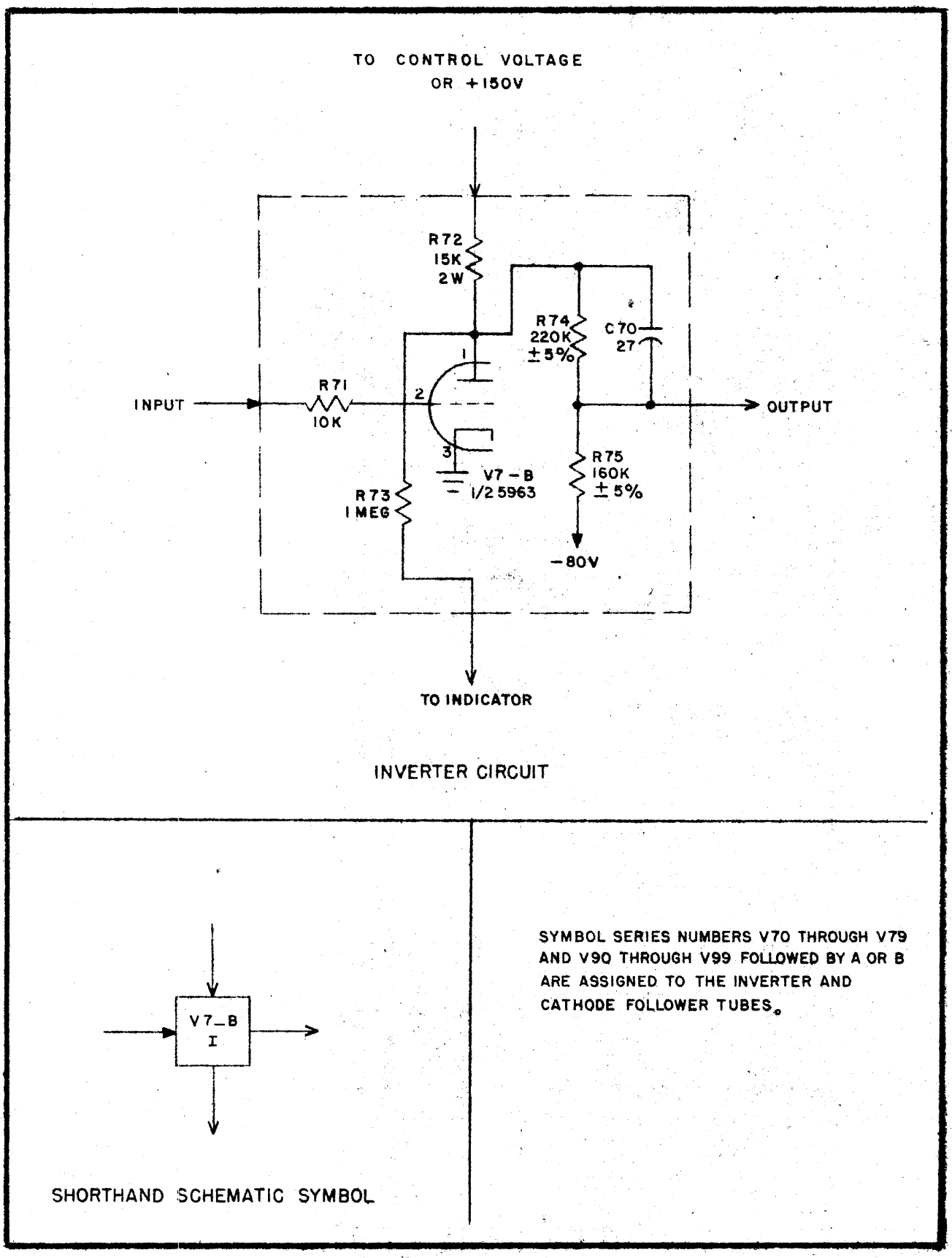


Figure 4-4. STANDARD Inverter Stage

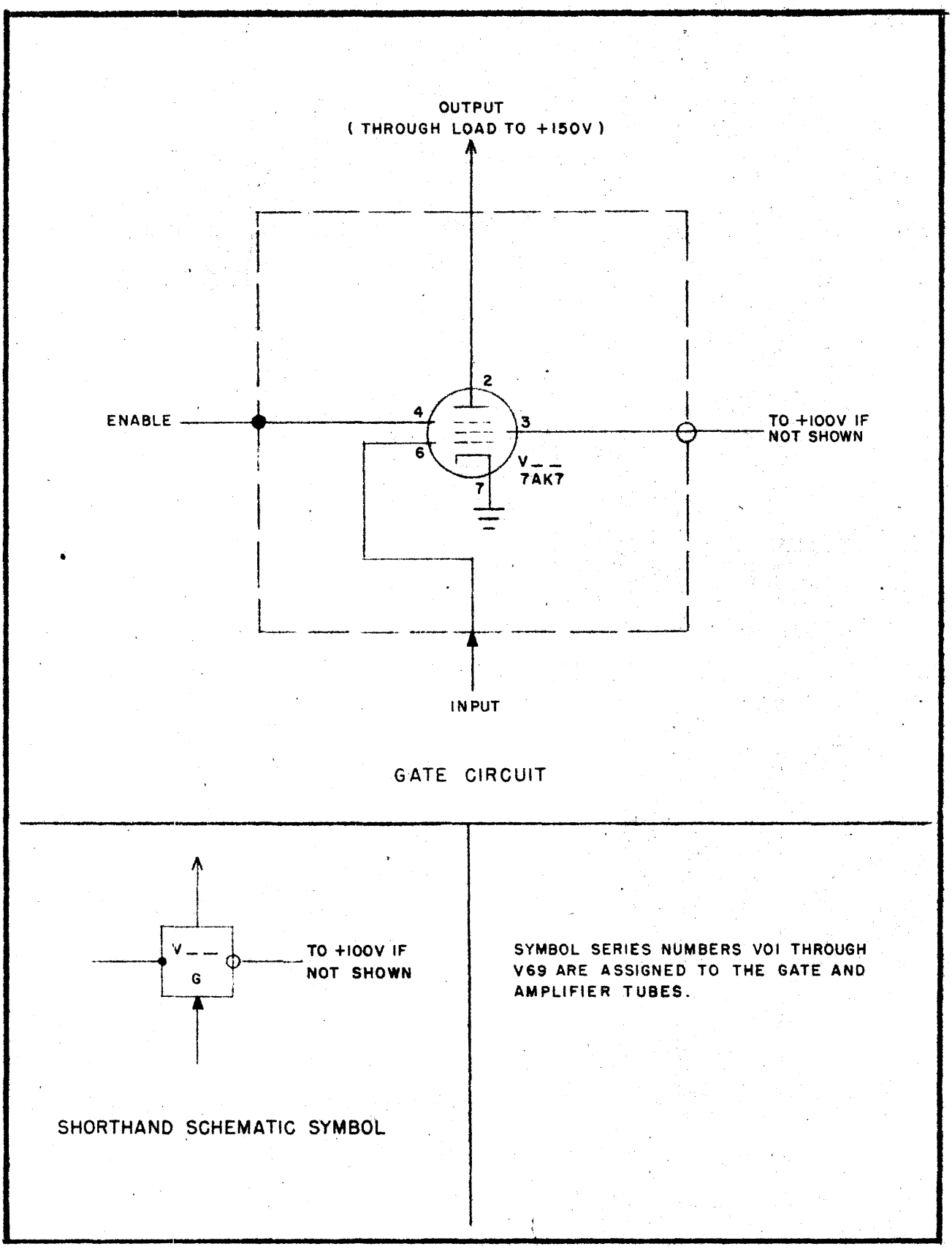


Figure 4-5. STANDARD Gate Stage

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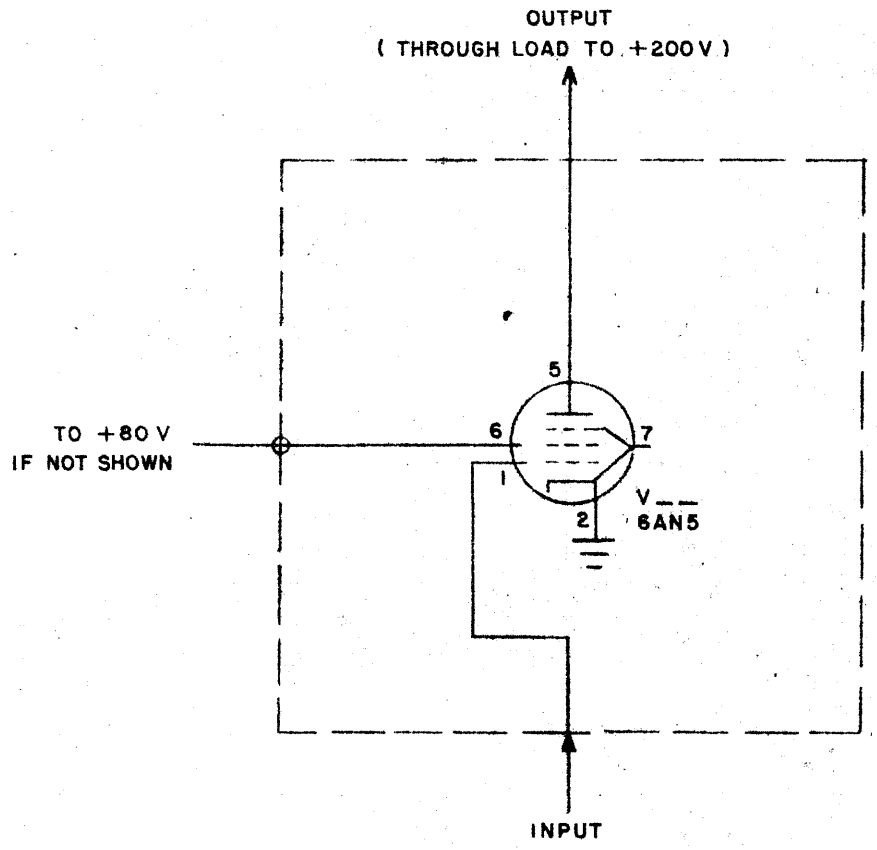
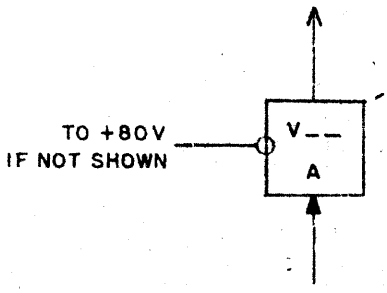


AMPLIFIER CIRCUIT



SHORTHAND SCHEMATIC SYMBOL

SYMBOL SERIES NUMBERS V01 THROUGH V69 ARE ASSIGNED TO THE AMPLIFIER AND GATE TUBES.

Figure 4-6. STANDARD Amplifier Stage

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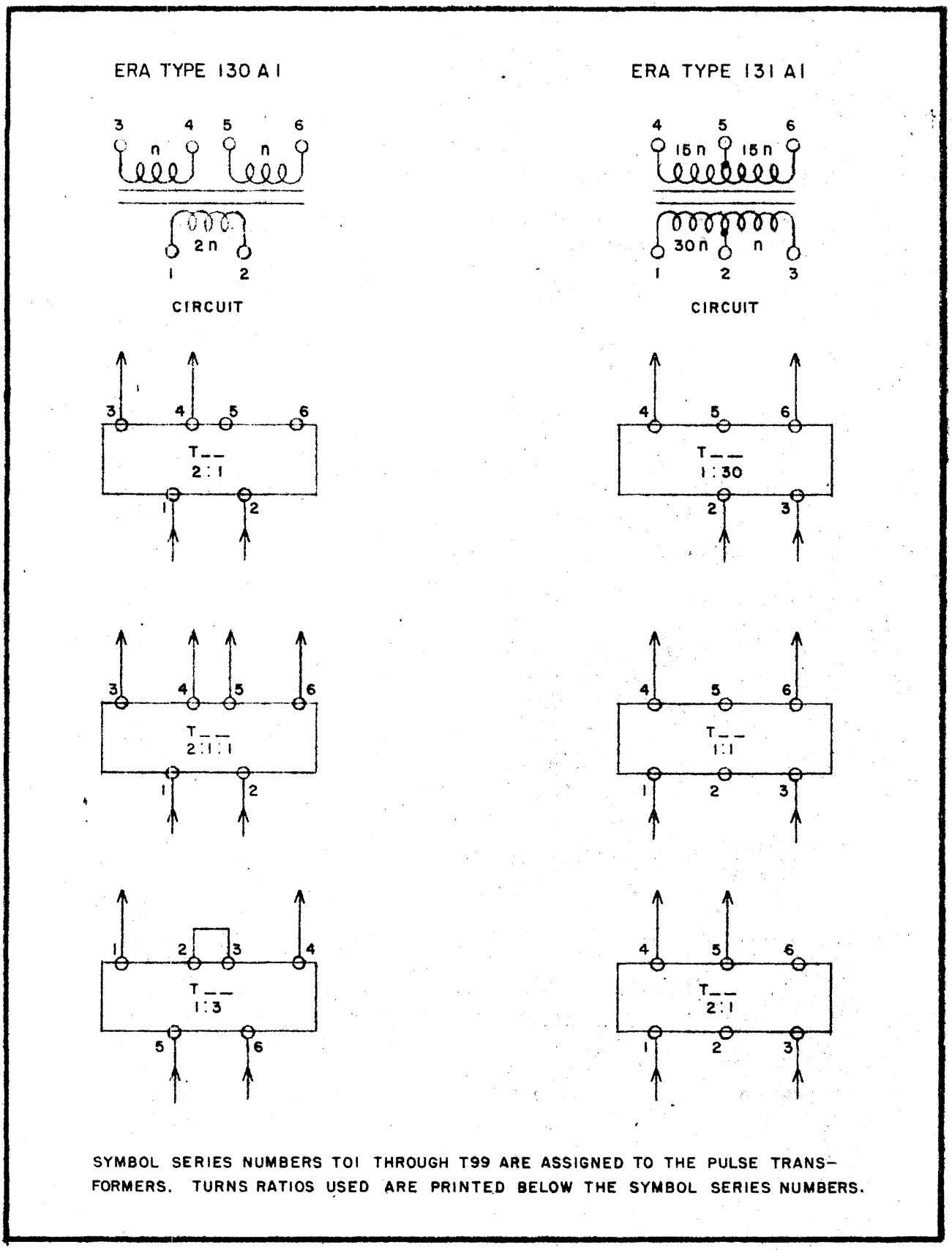

SYMBOL SERIES NUMBERS T01 THROUGH T99 ARE ASSIGNED TO THE PULSE TRANSFORMERS. TURNS RATIOS USED ARE PRINTED BELOW THE SYMBOL SERIES NUMBERS.

Figure 4-7. STANDARD Pulse Transformer Stages

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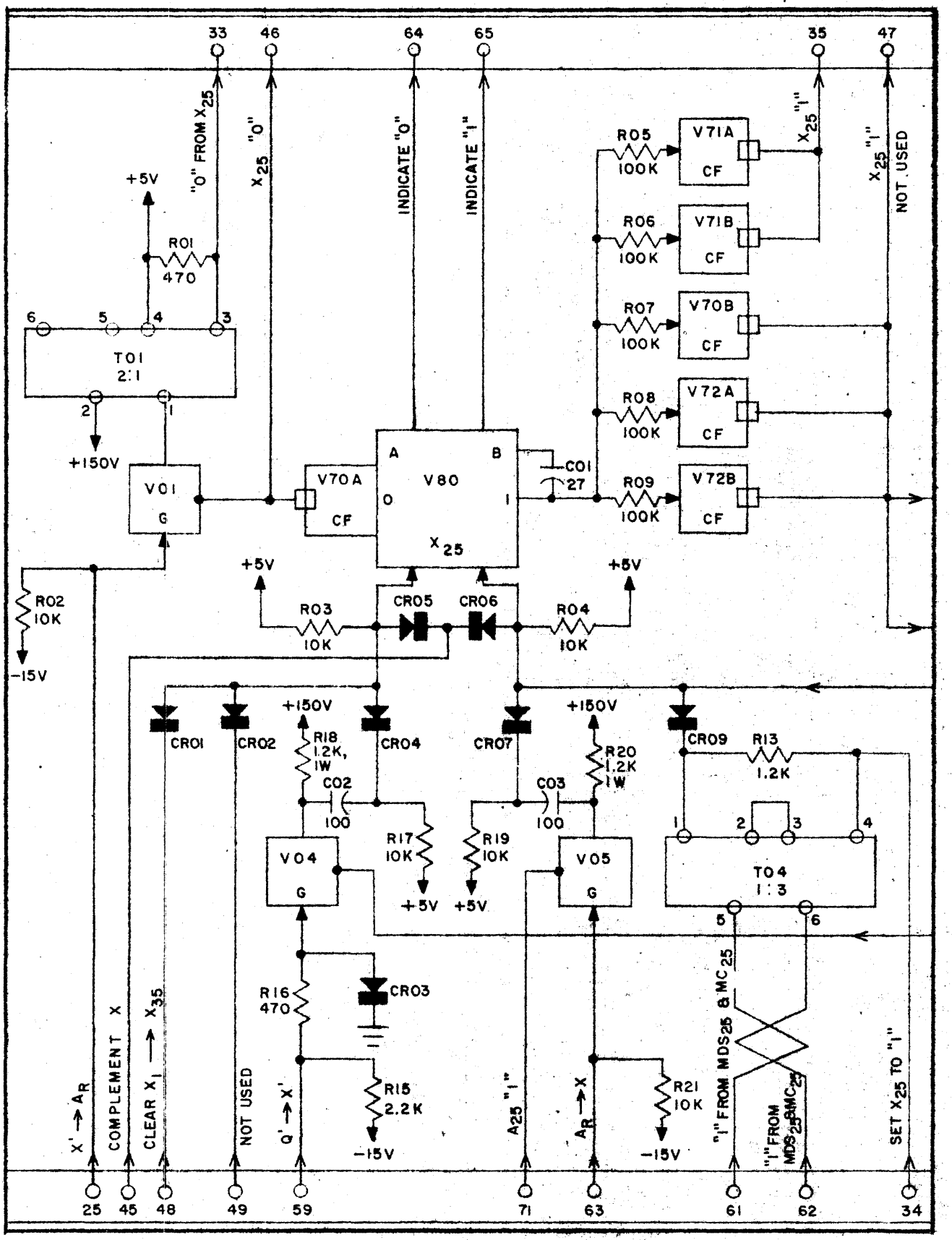

Figure 4-8. Portion of a Typical Schematic-Type Diagram (with signal origins and destinations omitted.)

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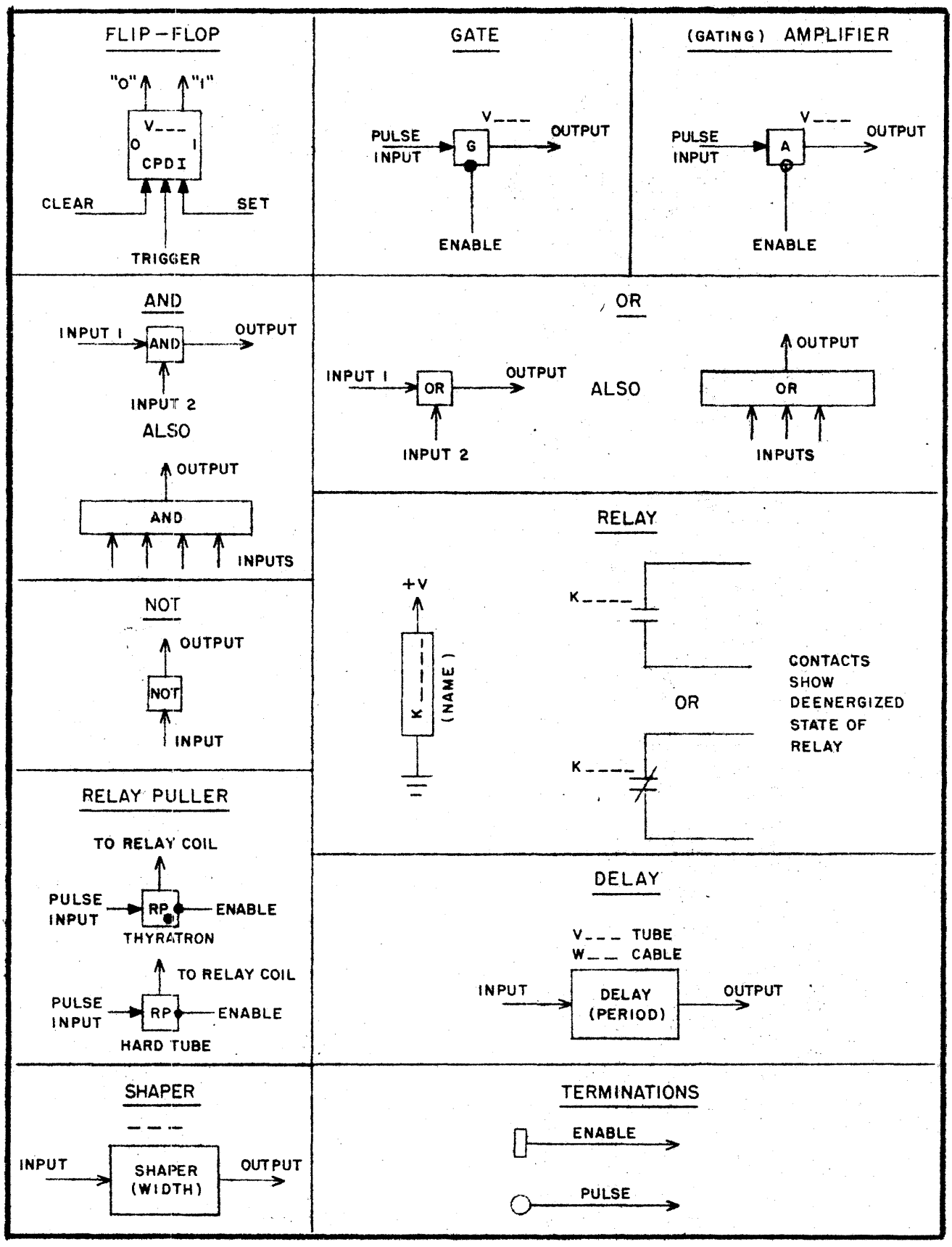

Figure 4-9. Block Symbols.

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identified by the label "CPD-1" on the block symbol.

In the following paragraphs comments are made concerning each block symbol to acquaint the reader with its use on block diagrams.

1. FLIP-FLOP. - A flip-flop is a logical element which is used to store a binary "0" or "1" digit of a count or computer word, or is used in a control circuit to register control conditions. All flip-flops are assigned a specific name which suggests their function in a particular system.

2. GATE. - Gates are used to control the path computer signals take throughout the equipment. A gate transmits an input signal when it simultaneously receives an enable. The screen grid may be used as a second control element but if it is not used in this manner, it is connected permanently to +100 vdc.

3. AMPLIFIER. - If an amplifier does not perform a logical function, it is left off of the block diagrams. However, the screen grid of many amplifiers are connected through a "disconnect" switch to +80 vdc, so that the amplifier functions like a gate. Where this feature is used, the amplifier is shown on the block diagram.

4. "AND" and "OR" CIRCUITS. - An "AND" circuit is a crystal coincidence circuit; that is, an output will be produced only when signals are present on all input lines simultaneously. An "OR" circuit produces an output when a signal is received from any one or more inputs.

5. "NOT" CIRCUIT. - The "NOT" circuit produces an output signal whenever there is not a signal from the preceding stage; that is, it is an inverter which produces a positive output only when the input goes negative. Under certain conditions, if an "OR" circuit is followed by a "NOT" circuit, the two function together as an "AND" circuit.

6. RELAYS AND RELAY PULLERS. - Relays function in general as electromechanical switches. Relay pullers are tubes which, when conducting, energize relay coils. If a dot is present in the block symbol, the relay puller is a gas-filled tube (thyratron), and if no dot is present, it is a hard (vacuum) tube.

7. SHAPERS AND DELAYS. - As their names imply, these circuits are used to shape and delay pulses. Where they are included on block diagrams, the block symbol often contains additional information; e.g., for shapers, pulse width; for delays, the amount of the delay and the type of element used to effect the delay.

8. TERMINAL SYMBOLS. - The terminal symbols denote whether input and output lines are enables or pulses on block diagrams. In general, a pulse is a short-duration signal and an enable is a signal of relatively longer duration.

9. SUMMARY. - Figure 4-10 illustrates the block diagram representation of the circuits shown in schematic form in Figure 4-8.

Stages such as inverters, cathode followers, etc., are not useful in explaining the logical function of a system and therefore are not used on block diagrams.

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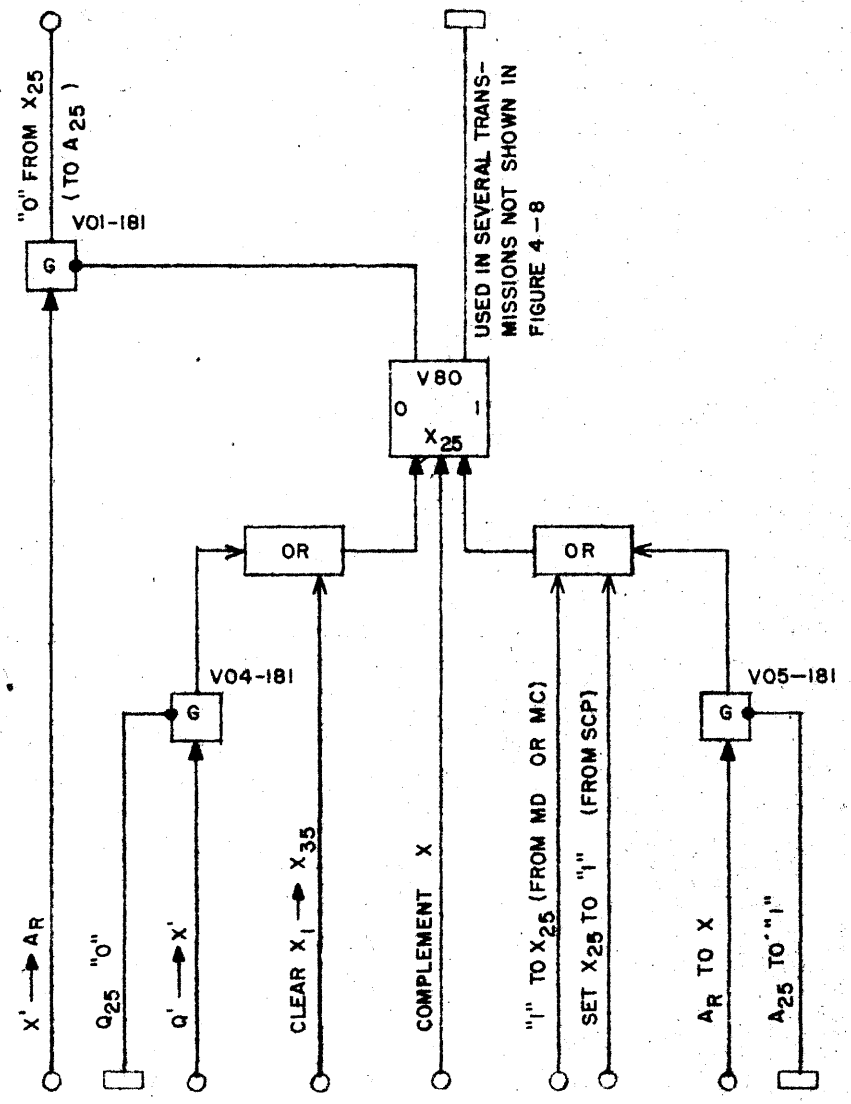

THE PURPOSE OF THIS DIAGRAM IS TO ILLUSTRATE (1) WHICH CIRCUITS OF FIGURE 4-8 PERFORM LOGIC AND THEREFORE WOULD BE INCLUDED ON A BLOCK DIAGRAM; AND (2) HOW THESE LOGICAL CIRCUITS ARE REPRESENTED BY BLOCK SYMBOLS.

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Figure 4-10. Block Diagram Representation of Figure 4-8.

6. STORAGE SECTION

a. GENERAL - The principle function of the Storage Section, or computer memory, is to provide the Control, Arithmetic, and Input-Output sections of the computer with the operands and instructions they require during computation. A secondary function of the computer memory is to provide temporary storage for the intermediate and final results of computations.

The Storage Section is composed of both "internal" and "external" storage. The internal storage consists of four "classes" of storage locations: magnetic drum (MD), Magnetic Core storage (MC), Q-register (Q), and Accumulator (A). Each storage position of internal storage is individually addressed. By insertion of the proper address into the Storage Address Register, any of the internal storage address locations can be made directly available for reading or writing. The external storage consists of four magnetic tape units, 0 MT, 1 MT, 2 MT, and 3 MT. Information in external storage is available only through the use of programmed computer instructions.

The principal characteristics of each of the storage systems are outlined in Table 4-1 below.

In the following subparagraphs, the Storage Address Register (SAR), the Storage Class Translator (SCT), and the Storage Class Control (SCC) circuits, which function in all references to the internal storage systems, are described first; the operation of the internal storage systems involving MD, MC, Q and A storage locations is then described; and finally the operation of the external storage system, MT, is explained.

b. STORAGE ADDRESS REGISTER - The Storage Address Register, SAR, is a 15-stage flip-flop register whose lower-order seven stages can operate as a subtractive counter. (See Block Diagram, Address Registers, Envelope *3, Volume 7.) As a 15-stage flip-flop register SAR has two principal functions: (1) SAR is the exchange register for transmissions to and from the Program Address Counter, PAK, and for transmissions from the U-Address Counter, UAK, and the V-Address Counter, VAK; (2) SAR provides temporary storage for a 15-bit storage address during internal storage references. These two functions of SAR are discussed in the following subparagraphs. The function of the seven lower-order stages of SAR as a subtractive counter, the Shift Counter (SK), are discussed in the paragraph which explains the Arithmetic Section of the computer.

(1) OPERATION AS AN EXCHANGE REGISTER. - Each of the 15 flip-flops in SAR has gate-controlled inputs to its "1" side. A set of gates in the "1" output circuits of PAK, another set of gates in the "1" output circuits of UAK, and a third set in the "1" output circuits of VAK are respectively sampled by the signals PAK→SAR, UAK→SAR, and VAK→SAR to achieve the corresponding transmissions into SAR. Generally, when transmissions from PAK, UAK, or VAK are to be carried out, the flip-flops in SAR have all been previously set to their "0" state. If SAR does not initially contain all "0's", the transmission from PAK, UAK, or VAK will possibly set SAR to some value other than (PAK), (UAK), or (VAK). The special cases where this can occur are noted in the subparagraph which discusses SK.

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TABLE 4-1

PRINCIPAL CHARACTERISTICS OF EACH STORAGE CLASS

CLASS	STORAGE MEDIUM	STORAGE CAPACITY (36-bit words)	MAXIMUM ACCESS TIME	STORAGE REFERENCE PROCEDURE
MD	Non-Volatile: Polarized areas on surface of continuously rotating magnetizable surface.	16,384 words individually addressed.	34 milliseconds.	Highest-order three bits in SAR equal to 4,5,6, or 7 determines drum group 4,5,6 or 7. Lowest order 12 bits determines angular position on drum.
MC	Non-volatile: magnetized "cores" of permanent magnet material	1024 words, individually addressed.	8 microseconds.	Highest-order six bits in SAR equal to 00 or 01 (octal) determines MC. Lowest-order 10 bits determines specific MC address.
Q	Volatile: flip-flop register.	One word.	Two microseconds.	Highest-order three bits in SAR equal to 1 (octal) determines Q.
A	Volatile: flip-flop register.	One word.	Six microseconds.	Highest-order three bits in SAR equal to 2 (octal) determines A
MT	Non-Volatile: Polarized areas on surface of magnetic tape.	262,144 words (four tapes of 65,536 words each). On each tape, words grouped in blocks of 32 words each.	About five minutes; transfer rate of about 222 words per minute.	Words not individually addressed. Words located by block position. Blocks accessible through programmed Advance, Back, Read, & Write MT instructions.

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In the following example it is assumed SAR is clear before transmission takes place: gates in the "1" output circuits of PAK, UAK, or VAK are sampled by the signal PAK→SAR, UAK→SAR, or VAK→SAR; those gates enabled by "1" output enables from PAK, UAK, or VAK, then transmit a signal to the "1" input signal line of the corresponding stage of SAR and set the flip-flop in that stage to "1"; the effect is to change "0's" to "1's" in appropriate stages of SAR, so that if SAR was initially cleared to all "0's", (SAR) becomes equal to (PAK), (UAK), or (VAK), depending on which transmission signal is received. It is important to note that in these transmissions only "1's" are transmitted.

SAR can transmit information to both X and PAK. When one set of gates in the "1" output circuits of SAR are sampled by the signal SAR→X, those gates enabled by "1" outputs from SAR transmit a pulse to the "1" input signal line of the corresponding stage in the 15 lower-order stages of X. When the other set of gates in the "1" output circuits of SAR are sampled by the signal SAR→PAK, a similar transmission to PAK occurs.

(2) OPERATION AS AN ADDRESS REGISTER. - The usual manner in which storage addresses for internal storage references are inserted into SAR is by transmission of an address from PAK, UAK, or VAK into SAR, in the manner described in the previous subparagraph.

Another manner in which addresses are inserted into SAR is by special Command Timing Circuit (CTC) signals which set or clear SAR flip-flops. During one Command Timing Sequence, signals are initiated to change (SAR) to register either the first MC address, 00000, or the second MD address, 40001. If the F_1 switch on the Supervisory Control Panel (See Block Diagram, CTC, Envelope #4, Volume 7) is set to MC, a CLEAR SAR signal from CTC clears all SAR flip-flops to "0". However, if this switch is set to the MD position, SAR_{14} and SAR_0 are set to "1" and SAR_1 through SAR_{13} are cleared to "0" so that the address 40001 is in SAR.

The signal CLEAR SAR is also produced, either by an INTERNAL STORAGE RESUME signal received from the Pulse Distributor Control after each MD, MC, Q, and most A references, or by a CLEAR SAR signal issued directly by the Arithmetic Register Access Control. This is done to prepare SAR for receipt of the next address.

The possible addresses that can be formed by a 15-bit number and hence can be inserted into SAR are shown in octal notation in Table 4-2 below. Note that some possible addresses are not assigned to any of the four storage classes. These unassigned addresses, if inserted into SAR, will produce an SCC Fault and stop computer operation.

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TABLE 4 - 2
ASSIGNMENT OF ADDRESSES

ADDRESSES	ASSIGNED TO
00000-01777	MC Storage Addresses
02000-07777	Unassigned
1----	Q-Register Address (first digit only is significant; the other digits may be assigned any value.)
2----	Accumulator Address (first digit only is significant; the other digits may be assigned any value.)
30000-37777	Unassigned
40000-47777	MD, Group 4 Addresses
50000-57777	MD, Group 5 Addresses
60000-67777	MD, Group 6 Addresses
70000-77777	MD, Group 7 Addresses

The storage addresses assigned to each storage class form a closed consecutive set; i.e., each address of each class may be used to generate the next address of the set; the last address of each set can be used to generate the first address of the set.

This "closed loop" operation is explained in the text for UAK, VAK, and PAK.

When an internal storage reference operation is initiated, the "0" and "1" outputs of SAR are employed to determine not only which storage class (MD, MC, Q, or A) is involved, but, in the case of MD and MC, which specific storage location in the selected class is desired. The "0" and "1" outputs of the five higher-order stages of SAR are used to initiate a reading or writing operation in the proper storage system. If the referenced address belongs to the MD storage class, SAR stages SAR_0 through SAR_{14} are used in the MD system to locate the specific MD address desired. If the referenced address belongs to the MC storage class, SAR stages SAR_0 through SAR_9 are used in the MC system to locate the specific MC address desired. If the referenced address belongs to the Q or A class, the lower-order bits are ignored because Q and A both store only one word.

After an internal storage reference has been completed, the CLEAR SAR signal prepares SAR for the receipt of new data, as described previously in this subparagraph.

c. STORAGE CLASS TRANSLATOR. - The Storage Class Translator (SCT), shown on the Block Diagram, Storage Class Control, Envelope #2, Volume 7, is a group of "AND" circuits which interpret the contents of the five highest-order bits of the address held in SAR and produce storage class enables for the Storage Class Control (SCC), the Arithmetic Register Access Control (ARAC), and the Fault Detector.

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The storage class enables produced by SCT for the various possible combinations of bits in the higher-order stages of SAR are listed in Table 4-3 below. The Storage Class Translator does not receive outputs from the 10 lower-order stages of SAR.

TABLE 4-3

STORAGE CLASS TRANSLATION

SAR STAGE					ADDRESS	RESULTING STORAGE
14	13	12	11	10	RANGE SPECIFIED (Octal)	CLASS ENABLE
0	0	0	0	0	00000 - 01777	MC
0	0	1	-	-	10000 - 17777	Q
0	1	0	-	-	20000 - 27777	A
1	-	-	-	-	40000 - 77777	MD
"1" in any stage, SAR_{10}-SAR_{14}					02000 - 77777	NOT MC

The SCT enables MC, Q, A, and MD are used in SCC during SCC sequences to direct INITIATE READ and INITIATE WRITE commands from the Command Timing Circuits (CTC) to the proper internal storage system, and are used in the Arithmetic Register Access Control to control the clearing of A during certain instructions.

All five SCT enables (MC, Q, A, MD, and NOT MC) are sent to the Fault Detector where they are used to detect erroneous storage class references.

d. STORAGE CLASS CONTROL. - The Storage Class Control (SCC), shown on the Block Diagram of the Storage Class Control, Envelope #2, Volume 7, consists basically of the following four flip-flops: Initiate Read, Initiate Write 0-35, Initiate Write 0-14, and Initiate Write 15-29. Each of these has a series of gates associated with its "1" output circuit. The basic purpose of SCC is to carry out short sequences which initiate reading or writing operations in the storage class referenced by SAR.

SCC performs an SCC Initiate Read Sequence for MC, Q, A, or MD after its Initiate Read flip-flop is set to "1" by an INITIATE READ signal from CTC. The sequence initiates a reading operation in a particular storage system, depending on the type of SCT enables (MC, MD, Q, or A) present on the gates associated with the "1" output circuit of the Initiate Read flip-flop. Similarly, SCC performs one of the three writing operations after an INITIATE WRITE 0-35, INITIATE WRITE 0-14, or INITIATE WRITE 15-29 signal from CTC sets the Initiate Write 0-35, Initiate Write 0-14, or Initiate Write 15-29 flip-flop in SCC to "1". An Initiate Write Sequence initiates a writing operation in one storage system, depending on the SCT enables which are present on the gates associated with the "1" output circuit of these flip-flops.

(1) SCC INITIATE READ SEQUENCES. - SCC executes the following four SCC Initiate Read sequences: SCC Initiate Read MD, SCC Initiate Read MC, SCC Initiate Read A, and SCC Initiate Read Q. These sequences are listed in tabular form in Appendix B, Page B-58, Volume 2. Each sequence is begun by the INITIATE READ signal from CTC. The particular sequence executed for any given

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internal storage reference depends on which of the gates associated with the "1" output of the Initiate Read flip-flop are enabled by SCT.

As an example of how all SCC Initiate Read sequences are executed, the sequence is described below for the case where an MD address is held in SAR. (See Block Diagram, SCC, Envelope #2, Volume 7.) An MD address held in SAR causes SCT to enable the following gates in SCC: V07-30153, V02-30153, V06-30123, V06-30143, and V05-30153. When an INITIATE READ signal is produced by CTC, the SCC Initiate Read flip-flop V80-30143 is set to "1", and gate V08-30143 is thus enabled. The next CONTROLLED CLOCK PULSE that is produced passes through gate V08-30143, clears the Initiate Read flip-flop, samples gates V04-30143, V09-30143, V05-30143, V06-30143, and V05-30153, and is sent to the Fault Detector. Gates V06-30143 and V05-30153, enabled by the MD enable, issue INITIATE READ MD and INITIATE MD REFERENCE signals to initiate a reading operation in the MD system.

In a manner similar to that described above, INITIATE READ MC, INITIATE READ A, and INITIATE READ Q signals are produced for MC and ARAC when MC, A, or Q addresses, respectively, are in SAR.

(2) SCC INITIATE WRITE SEQUENCES. - There are six possible SCC Initiate Write sequences for MD and MC, as follows: SCC Initiate Write MD (0-35), SCC Initiate Write MD (0-14), SCC Initiate Write MD (15-29), SCC Initiate Write MC (0-35), SCC Initiate Write MC (0-14), and SCC Initiate Write MC (15-29). The 0-35 sequences initiate the writing of 36-bit words in MC and MD locations, and the 0-14 and 15-29 sequences initiate writing operations in only the v-address and u-address portions of storage locations, respectively. For example, these "partial writes" are used in execution of the Insert u Address (15uv) and Insert v Address (16uv) instructions, to alter execution addresses in a programmed routine.

No partial writing operations can be used in Q and A. For this reason, only two SCC Initiate Write sequences are possible for Q and A, as follows: SCC Initiate Write Q and SCC Initiate Write A.

Each SCC Initiate Write sequence is executed in a manner similar to the SCC Initiate Read MD sequence described in the previous subparagraph. The specific steps are described in detail in Appendix B, Pages B-59 through B-61 in this volume.

It should be particularly noted that SCC does not initiate any partial read operations in any of the internal storage systems, and that the SCC initiates partial writing operations only in MD and MC.

The following outline of events summarizes the basic functions of SAR, SCT, and SCC during internal storage references:

(1) A 15-bit storage address is held in SAR during every internal storage reference.

(2) Outputs from the five higher-order stages of SAR are translated by SCT to select MD, MC, or Register Storage as the memory system which is to function.

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(3) One of the SCC Initiate Read or SCC Initiate Write sequences is performed which initiates the desired operation in the storage system of the selected storage class.

(4) If MD or MC is involved, the output of lower-order stages of SAR are also used to determine the particular MD or MC location referenced.

(5) When the desired operation has been carried out in the exact memory location specified, SAR is cleared and thus prepared for use in another storage reference.

e. MAGNETIC DRUM STORAGE SYSTEM. - The Magnetic Drum Storage System (MD) provides the 1103 Computer System with a non-volatile, medium-access storage memory. Each of the 16,384 36-bit storage locations in MD is individually addressed and is available for reading or writing once each drum revolution. Storage addresses 40000 through 77777 (octal) are assigned to MD.

The MD Storage System (See Block Diagram, Magnetic Drum Storage System, Envelope #2, Volume 7) is composed of four principal parts, as follows: (1) the Magnetic Drum Assembly which includes the storage medium, a coated surface on a continuously rotating aluminum cylinder (known as the magnetic drum) which receives computer words during writing and makes them available for reading once during each revolution of the drum, and the transducing elements, dual-purpose magnetic reading-and-writing heads which transfer data to and from the storage positions with which they are associated; (2) the Clock Pulse Distributor (CPD) which receives 500 kc signals from the Timing Pulse Multiplier circuit when the drum is used as the basic clock source, and issues timing signals CP-0, CP-1, and CP-3 to the MD system; (3) the Magnetic Drum Locating Circuits which function primarily to notify the MD Access Control when a referenced storage location has been located and positioned for reading or writing; and (4) the Magnetic Drum Access Control which directs the transfer of words into or out of the drum when the referenced storage location is properly positioned.

(1) MAGNETIC DRUM ASSEMBLY. - The Magnetic Drum Assembly consists of two principal elements: the rotating cylinder (or drum), and the magnetic reading and writing heads.

The cast-aluminum drum (see Plate 5-17, Volume 6) is 17 inches in diameter and 11.875" long. It is taper-fitted and locked to a steel shaft which in turn is mounted on a cast-aluminum base and driven at 1725 rpm by a 220 vac, 3 phase, 3/4 hp motor. The machined drum surface is coated with magnetic iron oxide, except at one end where it is encircled by a narrow soft steel band. A cast aluminum head-mounting bracket fits over the top of the drum and fastens to the supporting base.

The head-mounting bracket contains inserts which receive the magnetic heads. Details of the magnetic head assembly are shown in Plate 5-20, Volume 6. These inserts are arranged for space considerations so that the heads are mounted in the bracket in a spiral fashion. A lateral spacing of 1/16" between adjacent heads is maintained by means of the spiral arrangement.

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The mechanical "setting" of each head is accomplished by a differential thread principle. When a head is properly set, its core-gap is approximately 0.002 inch from the drum surface.

Once the head has been set, the head cable is connected by fitting the five-conductor plug of the head cable into the head barrel and tightening the coupling flange firmly. The entire MD Assembly is shown installed in Plate 5-19, Volume 6.

(2) PRINCIPLES OF MAGNETIC DRUM STORAGE. -- Each magnetic head contains a single winding on a ferrite core. In writing, a current pulse of a given polarity is sent through the winding, setting up a magnetic field. The pulse polarity governs whether a "0" or a "1" is to be written. The flux of the magmetic field fringing around the gap of the core magnetizes to saturation that portion of the drum surface under the gap at that instant. The polarity of the magnetized area agrees with the pulse polarity applied to the head winding, and thereby can be later distinguished as a "0" or a "1" during reading operations. Amplifiers in the reading circuits receive signals from areas storing "0's" as well as from those storing "1's", but produce outputs only when "1's" are read.

The narrow band on the coated storage surface of the drum which passes beneath one head as the drum revolves is called a "track". Tracks on this surface exist only in concept, i.e., the coated surface is not physically divided, but can be thought of as discreet narrow bands, one for each head. However, the two tracks on the soft steel band on the end of the drum exist physically. The outer track, or "timing track", is uniformly knurled with V-shaped notches which are spaced 80 per circular inch. The inner track is called the "mark track" and it contains a single "zero index" notch. These two permanent tracks are used for control purposes. Unlike the other heads, the heads associated with the two permanent tracks perform only reading operations.

Provision is made for three read heads (one for the timing track, one for the mark track, and one spare), and 175 read-write heads (including 31 spares) for the tracks on the coated surface; 144 of the read write heads and their associated tracks are divided into 4 groups of 36, called Group 4, Group 5, Group 6, and Group 7.

Each group of read-write heads has 36 sets of reading and writing circuits, each of which is associated with one of the 36 heads of the group. In every reading or writing operation sequence, one part of the operation selects which group of heads is to read or write; another part selects the angular position of the drum at which these heads are to function.

The timing track and mark track are used in connection with the angular position selection. The timing track notches, spaced 80 per circular inch, are used to identify discreet angular positions of the drum; i.e. when the timing track head senses a notch, it produces a TIMING PULSE signal. The TIMING PULSES are produced at a rate of 125 kc. Each TIMING PULSE results in a signal which notifies MD Location Control that an angular position will presently be correctly positioned for reading or writing. The single notch on the mark track is called a zero index notch because it marks the effective beginning of the timing track. It establishes a reference point during each drum revolution from which angular positions are counted. The first 4096 notches read from the timing track after the zero index notch on the mark track is read define the

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4096 usable angular positions of the drum. All other positions, i.e., those between angular position 4095 and angular position 0, are called the "dead space" on the drum.

Since there are 4096 angular positions of the drum at which each of the four groups can read or write, there are a total of 16,384 locations, or storage addresses, available. Each MD storage address is uniquely defined by specifying what group of heads writes into it or reads from it, and at which angular position of the drum it is located.

The portion of each track that is positioned beneath one magnetic head during one angular position of the drum is called a "cell". It is convenient to think of each of the 36 heads of a group as writing into or reading from one cell beneath it at discreet angular positions of the drum.

The return-to-neutral method of recording is employed; i.e., all the cells of the drum are initially unmagnetized. During writing operations both the "0's" and "1's" of the word to be stored are written; during reading only the "1's" are read to X.

(3) CLOCK PULSE DISTRIBUTOR. - The Clock Pulse Distributor (CPD) uses 500 kc CLOCK PULSES to produce CP-0, CP-1, and CP-3 pulses for controlling the MD operations.

The 500 kc CLOCK PULSES are developed by the Timing Pulse Multiplier circuit, shown in the lower right corner of the Block Diagram, MD Storage System. When manual selections are made so that the drum is used as the basic source of CLOCK PULSES, the 125 kc TIMING PULSES from the drum timing track are recirculated through this circuit. Each TIMING PULSE entering the circuit is delayed by two microseconds, then fed back into the circuit. As a result, the output of this circuit is a sequence of 500 kc MD CLOCK PULSES. These pulses are used not only in the MD Storage System, but also in the Clock Pulse Distributor as a basic source of computer clock pulses.

For convenience the operation of the Timing Pulse Multiplier and the Clock Pulse Distributor are best described together. The Timing Pulse Multiplier and the Clock Pulse Distributor consist of two flip-flops (CPD I and CPD II), a two microsecond delay circuit W01-60054, six gates, and several coincidence circuits. Initially, CPD I and CPD II are set to "0", and the recirculation gate V02-60054 is enabled. When the drum is selected as the clock source, a MULTIPLIER ENABLE is supplied to gate V03-60054, from the normally-closed contacts of the Select Osc relay, K30018. The first TIMING PULSE to enter the Multiplier through gate V03-60064 will emerge after a two microsecond delay as an MD CLOCK PULSE. This MD CLOCK PULSE is then sent externally to the Clock Rate Control (CRC), a part of the Master Clock System. Within the Multiplier and Distributor each MD CLOCK PULSE is used to probe Distributor gates V04-60073, V05-60073, and V07-60073, to advance the Distributor flip-flops, and to probe the recirculation gate V02-60054. The first MD CLOCK PULSE, issued two microseconds after a TIMING PULSE, finds Distributor gate V04-60073 enabled and produces CP-0. It also triggers CPD II to "1", and passes through the recirculation gate V02-60054. (It does not change CPD I since gate V01-60054 is not yet enabled.) After a two microsecond delay, this first MD CLOCK PULSE is issued again to CRC by the delay circuit as another MD CLOCK PULSE. This second MD CLOCK PULSE finds Distributor

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gate V06-60073 enabled and produces CP-1. It passes through gate V01-60054 (enabled since CPD II is a "1"), triggers CPD II back to "0", and triggers CPD I to a "1". It recirculates, and two microseconds later it emerges as the third MD CLOCK PULSE. This third MD CLOCK PULSE is sent externally to CRC as were the other two, but internally it finds all three Distributor gates and gate V01-60054 disabled, so it merely triggers CPD II to a "1" and is recirculated. After a two microsecond delay it emerges as the fourth MD CLOCK PULSE. Like the others, this fourth MD CLOCK PULSE is sent externally to CRC. Internally it finds Distributor gate V07-60073 enabled and passes through as CP-3. Since CPD II and CPD I were both set to "1" by the previous MD CLOCK PULSE, gate V02-60054 is disabled during CP-3, so that the fourth MD CLOCK PULSE is not recirculated. Its only function in the Distributor is to trigger both CPD II and CPD I to "0". At the same time that CP-3 is produced, another TIMING PULSE arrives from the drum and the above sequence is repeated. As a result of the above operations, the Master Clock System receives 500 kc MD CLOCK PULSES and the MD Access Control receives CP-0, CP-1, and CP-3 signals. The numerals 0, 1, and 3 after the letters "CP" signify the relative time of occurrence of these pulses in 500 kc CLOCK PULSE periods: i.e., CP-0 and CP-1 are separated by two microseconds, and CP-1 and CP-3 are separated by four microseconds.

(4) MAGNETIC DRUM LOCATING CIRCUITS. - These circuits are used in each MD reference to find the MD storage location specified by (SAR), and to generate the proper signals for reading or writing when the drum is positioned in that location. These circuits are shown in the lower left quarter of the Block Diagram of the MD Storage System.

The complete storage address of a particular location in MD is specified by a 15-bit number. The three higher-order bits specify the group number, which may be 4, 5, 6, or 7. The 12 lower-order bits specify one of the 4096 angular positions of the drum. At the time a storage reference is made, a 15-bit storage address is held in the Storage Address Register, SAR. One part of the MD Locating Circuit is a Group Selection Circuit which performs the group selection specified by the group bits of the storage address. The other part of the MD Locating Circuit searches for the angular position specified by the storage address, and generates a COINCIDENCE PULSE when the correct angular location is properly positioned for reading or writing.

The Group Selection circuit is composed of a group detector, a group selector, and a group translator. The group detector is composed of four gates and several coincidence circuits. Gates V05-30203 and V06-30203 receive an INITIATE MD REFERENCE signal from SCC during every MD reference. If the group which is to function in the current MD reference is the same group that functioned during the last MD reference (i.e., if SAR_{12} and SAR_{13} = GS_1 and GS_2), these gates are disabled and the group detector does not initiate any change in group selection. But if the current address in SAR specifies a group different from the group which last functioned in an MD reference, either gate V05-30203, or gate V06-30203, or both will be enabled and their outputs will trigger group selector flip-flops GS_1 and GS_2 to register the correct group selection. The outputs of the GS_1 and GS_2 flip-flops are combined in coincidence circuits in the group translator. Depending on which group is selected, a GROUP 4, GROUP 5, GROUP 6, or GROUP 7 enable is produced. Each of these enables is sent to gates in the reading and writing circuits of the group of heads to which it corresponds. For example, if a GROUP 4 enable is produced, it enables gates in the reading

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and writing circuits of each head in Group 4. Once selected, a particular GROUP enable is present until a new group selection is made.

If a change in the group selection is required for a reading operation, it is necessary to delay reading by about 32 microseconds to allow the circuitry to recover from transients introduced by the group switching operation. No corresponding problem exists for the writing operation. When a read reference is made to MD, gates V01-30203 and V04-30203 in the Group Detector are pulsed by the INITIATE READ MD signal from SCC. If the currently referenced group of heads is the same as the last group which functioned, gate V01-30203 will be enabled and the SCC signal will produce an INITIATE READ signal for MDAC. If a switching of groups is required in the current MD reference, gate V04-30203 will be enabled and the SCC signal will produce an INITIATE DELAYED READ signal for MDAC. This latter signal sets the Initiate Delayed Read flip-flop in MDAC to "1". The "1" output of this flip-flop initiates a delay of approximately 32 microseconds, and thereby prevents any attempt to probe for coincidence (and hence read) until the reading amplifiers have had a chance to recover from the transients generated by switching heads. If an INITIATE READ signal is produced, the above delay is not initiated.

The remainder of the MD locating circuits are the Address Interlace Chassis, an Angular Coincidence Detector, an Angular Index Counter (AIK), and a Location Control circuit. (See Block Diagram and Figure 4-11.) These function to select the angular position on the drum which is referenced by lower-order 12-bits of the storage address held in SAR. The Address Interlace Chassis, depending on its wiring arrangement, translates the 12 angular position bits of address in SAR in such a manner that if addresses with consecutive angular positions are inserted into SAR, they become coincident with every fourth, eighth, sixteenth, thirty-second, or sixty-fourth angular position on the drum, rather than with physically adjacent angular positions. The Angular Coincidence Detector compares the count in AIK (a 12-stage binary counter) with the interlaced count from SAR. Location Control consists of three flip-flops (Preset, Advance AIK, and Coincidence Lockout) and their associated gates. Location Control regulates the advance of AIK and the probing of the Angular Coincidence Detector.

In every MD reference, the 12 lower-order bits in SAR are connected through the Address Interlace Chassis to the Angular Coincidence Detector. As the drum rotates, TIMING PULSES from the timing track head are produced which identify or define each successive angular position of the drum. Each of these TIMING PULSES results in a signal which causes the Angular Index Counter (AIK) to advance by one, so that AIK maintains a count which indicates the angular position of the drum to be properly positioned next for reading or writing. When, during reading or writing operations, the angular position of the drum indicated by (AIK) matches the referenced angular position from the Address Interlace chassis a COINCIDENCE PROBE signal detects this condition and the Coincidence Detector generates a COINCIDENCE PULSE for MDAC. The COINCIDENCE PULSE results in the referenced reading or writing operation being performed in exactly the referenced angular location.

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Five types of Address Interlace Chassis are provided with the 1103 system: one chassis each for 4, 8, 16, 32, and 64-interlaces. However, only one of these is inserted into the equipment at any one time. Each, in effect, alters the angular position of consecutive storage addresses from Computer Control in

such a manner that they will be coincident with different sequences of angular positions on the drum. For example, the 4-interlace Address Interlace Chassis will translate the angular positions specified in consecutive storage addresses received from SAR so that they are coincident with every fourth angular position on the drum, rather than with the physically consecutive angular positions. If the 8-interlace Address Interlace Chassis is used, then coincidence is obtained from every eighth angular position on the drum and so on. A spare Address Interlace chassis is also provided which can be wired to make angular positions of consecutive addresses in Computer Control coincident with the consecutive, or physically adjacent, angular positions on the drum. In summary, Address Interlace Chassis function to assign an order or sequence to the angular positions on the drum which are to be coincident with consecutively numbered angular positions from Computer Control.

The usefulness of interlace may be seen by the following example. If instructions involving a series of readings from consecutive MD addresses are to be executed, and each transmission in the series can be accomplished in less time than is required for four angular positions to pass beneath the heads but more time than for one angular position to pass (32 microseconds), the employment of the 4-interlace Address Interlace chassis will cause the data to be transmitted to every fourth storage location, even though the SAR-specified locations are consecutive. The computer can thus accomplish its transmissions without waiting a full drum revolution period between consecutive reading operations. Of course, changing the Address Interlace Chassis results in the changing of the assignment of addresses on the drum, so that the drum must be reloaded each time the interlace is changed. The interlace does not affect the outputs of SAR_{12}, SAR_{13}, and SAR_{14}, and therefore does not affect the selection of the MD group in any way.

Figure 4-11 below shows how the Address Interlace Chassis alters consecutive storage addresses from SAR to effect a 4-interlace. In Figure 4-11, the MD address 40001 is inserted in SAR. Note that although address 40001 is numerically the second Group 4 angular position of the drum, the interlace causes 40001 to be coincident with the fifth angular position around the drum (AIK = 4). This is because the 4-interlace Address Interlace Chassis effectively shifts the lower-order 12 bits of the SAR address to the left by two bits, which corresponds to a binary multiplication of four. In a similar manner, the 8-interlace chassis shifts these bits to the left by three ($2^3 = 8$), the 16-interlace shifts the bits by 4 ($2^4 = 16$), etc.

(5) MAGNETIC DRUM ACCESS CONTROL. - The Magnetic Drum Access Control (MDAC) directs the MDAC Locating Sequence, and performs MDAC Read and MDAC Write Sequences when read or write references are made to MD.

(a) MDAC LOCATING SEQUENCE - The MDAC Locating Sequence is executed when no reading or writing references are being made to the drum. This sequence keeps track of which angular position of the moving drum is next to be properly positioned for reading or writing. The MDAC Locating sequence described below is shown in tabular form in Appendix B of this volume.

Once per drum revolution the zero index notch is read from the mark track and gate V11-60064 is momentarily enabled. A TIMING PULSE from the timing track head probes this gate while it is enabled and produces a MARK PULSE. Each

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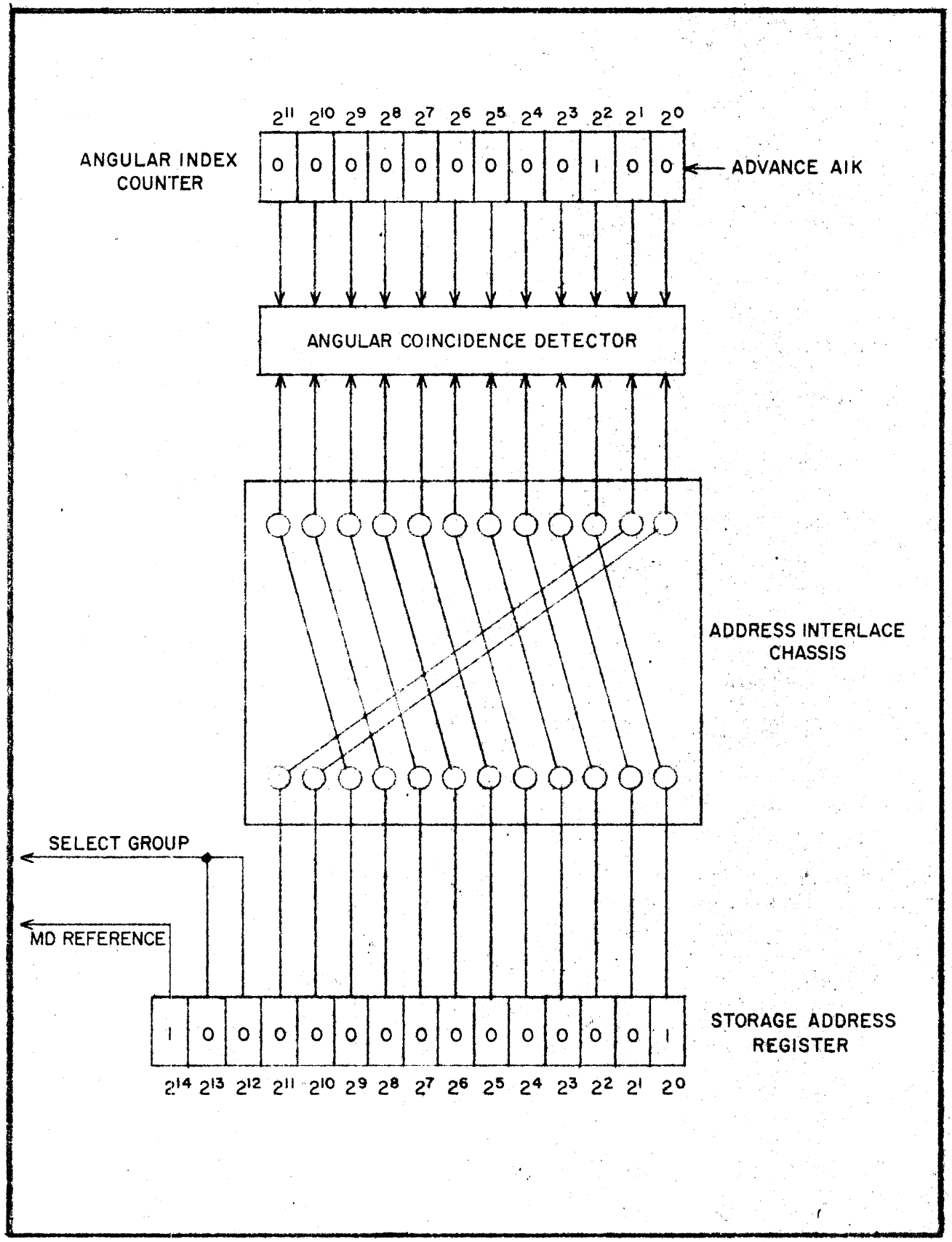

Figure 4-11. MD Locating Circuits

MARK PULSE initiates the MDAC Locating Sequence to count each of the next 4096 consecutive angular positions of the drum, and thereby assign a number to each position, as follows: the first, zero; the next, one; etc. to the last, 4095. After 4096 consecutive angular positions have been counted in AIK, the MDAC Locating Sequence effectively ceases until another MARK PULSE is read. It then begins all over again.

Each MARK PULSE sets the Preset flip-flop V81-60063 in Location Control to "1". The next CP-0 issued by the Clock Pulse Distributor passes through gate V04-60063, sets AIK to all ones, clears the Preset flip-flop, and sets the Coincidence Lockout flip-flop to a "1". The same CP-0 also clears the Advance AIK flip-flop. The next CP-0 to occur clears the Advance AIK flip-flop and advances AIK from all "1's" to all "0's" producing an AIK END CARRY signal which triggers the Coincidence Lockout flip-flop from "1" to "0". Subsequent CP-0's each clear the Advance AIK flip-flop and advance AIK one count. AIK can advance from zero to 4095. When AIK stores the count 4095, each stage contains a "1". The next CP-0 advances AIK to all "0's" and results in an AIK END CARRY signal which triggers the Coincidence Lockout flip-flop back to a "1". This marks the effective end of the MDAC Locating Sequence. AIK continues to be advanced by subsequent CP-0's, but its count is meaningless until a MARK PULSE is produced which indicates that the dead space on the drum has passed and that the above sequence is to begin again. This sequence for locating is slightly different during reading and writing. When a read reference is made, the receipt of the INITIATE READ MD signal eventually results in the enabling of gates V04-60053 and V06-60053. When this condition is set up, the read sequence is superimposed on the locating sequence so that CP-0's continue to advance AIK, and, during the AIK counts 0 through 4095, which follow a MARK PULSE, each CP-0 produces a COINCIDENCE PROBE until coincidence is obtained. These operations are explained in the MDAC Read Sequence below. When a write reference is made, the particular INITIATE WRITE MD command that is received results in the enabling of gates V01-60073 and V03-60073. CP-0 will advance AIK and clear the Advance AIK flip-flop to "0" as in the MDAC Locating Sequence, until the first CP-1 which occurs after V01-60073 and V03-60073 are enabled. This first CP-1 also advances AIK and sets the Advance AIK flip-flop back to "1". Thus, the AIK count is moved ahead by two instead of one during the first CP cycle of an MDAC Write Sequence, and thereafter AIK is advanced by CP-1 until the writing operation is completed. When writing is completed the MDAC Locating Sequence resumes and AIK is advanced by CP-0 again. The double advance of AIK upon receipt of an INITIATE WRITE MD signal is explained in the MDAC Write Sequence below.

(b) MDAC READ SEQUENCE. - When a reading operation from the drum is to be executed, an MDAC Read Sequence is initiated to locate the MD address at which the word to be read is stored, and to read the contents of that address (36-bits) into X. The signals INITIATE MD REFERENCE and INITIATE READ MD are sent from SCC to the Group Detector. The INITIATE MD REFERENCE signal and the group bits of the referenced storage address (SAR_{12} and SAR_{13}) initiate the proper group selection; the INITIATE READ MD signal initiates the MDAC Read Sequence. The angular position bits of the referenced storage address (SAR_0 through SAR_{11}) are connected through the Address Interlace Chassis to the Angular Coincidence Detector, so that when the referenced storage address is located, a COINCIDENCE PULSE is generated and the selected group of heads functions. Each of the 36 heads which reads a "1" transmits a "1" to its corresponding stage in X. ("0's" are not transmitted to X.)

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If the group being referenced (as specified by bits SAR 12-13) is the same as that which last functioned, gates V05-30203 and V06-30203 will be disabled. If the currently referenced group is different from the last group that functioned, either or both of these gates will be enabled and their outputs will trigger the Group Selector (V80-60071 and V81-60071) to select the presently desired group. Outputs of this Group Selector are sent to coincidence circuits where a GROUP 4, GROUP 5, GROUP 6 or GROUP 7 enable is produced. Each of these latter outputs enable 36 gates in the reading and writing circuits of the group of heads to which they correspond. Since only one GROUP enable can be produced, only its corresponding group of heads will function during reading.

The INITIATE READ MD signal probes gates V01-30203 and V04-30203. If no switching between groups of heads is called for only gate V01-30203 will be enabled and the INITIATE READ MD signal will produce an INITIATE READ signal for MDAC. If a switching of group enables is required, only gate V04-30203 will be enabled and the INITIATE READ MD signal will produce an INITIATE DELAYED READ signal for MDAC. In either case the INITIATE READ MD signal from SCC begins the MDAC Read Sequence which is shown in tabular form in Appendix B of this Volume, and explained below.

If the currently referenced group of heads is different from the last to function, the resulting INITIATE DELAYED READ signal sets both the Initiate Read and Initiate Delayed Read flip-flops to "1". The "1" output of the Initiate Read flip-flop enables gates V06-60053 and V07-60063. The "1" output of the Initiate Delayed Read flip-flop enables gate V07-60053. The next CP-0 to occur passes through V07-60053 to clear the Initiate Delayed Read flip-flop to "0", and to set the Read Lockout flip-flops V80-60053, V81-60053, and V82-60053 to "1", "0", and "0" respectively. (This registers a binary count of 100 in these flip-flops.) No further CP-0's get through V07-60053; however, as explained before in the MDAC Locating Sequence, they continue to advance AIK. The next four CP-1's to occur pass through V05-053 to set the Read Lockout flip-flops to 101, 110, 111, and 000 (binary) in that order. When each flip-flop is set to 0, gate V05-60053 is disabled and subsequent CP-1's have no effect on the Read Lockout flip-flops. Gate V04-60053 however, becomes enabled. Because gate V06-60053 is also enabled by the "1" output of the Initiate Read flip-flop, the next CP-0 to occur and all succeeding CP-0's which occur while the usable area of the drum is passing under the magnetic heads become COINCIDENCE PROBES. The delay is the only difference between an MDAC Read Sequence begun by an INITIATE DELAYED READ signal and that begun by the INITIATE READ signal. The delay disables gate V04-60053 and prevents any attempt to make a coincidence probe after switching group enables, since this latter action causes transients which may interfere with the reading operation. The delay in effect provides the reading amplifiers with time to recover from these transients before attempting to read data from the drum.

If no switching of groups is required, the INITIATE READ MD signal from SCC produces an INITIATE READ signal in the Group Detector. This signal merely sets the Initiate Read flip-flop to its "1" state. When the next CP-0 occurs, gates V06-60053 and V04-60053 are both enabled, and CP-0, in addition to advancing AIK by one as in the MDAC Locating Sequence also generates a COINCIDENCE PROBE which effectively compares (AIK) with the interlaced storage address held in SAR before CP-0 advances AIK. A CP-0 is produced for each angular position of the drum, and this comparison continues until the desired angular location is

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about to be positioned under the magnetic heads. When the count in AIK equals the interlaced count from SAR, the COINCIDENCE PROBE on CP-0 results in a COINCIDENCE pulse (and AIK is then advanced). The COINCIDENCE pulse passes through gate V07-60063 and produces a READ pulse which probes 36 Read to X gates. These Read gates are the transfer gates for MD read operations and they are common to the reading circuits of all four groups. When the READ pulse occurs, signifying that the desired angular position has been found, the heads (in the selected group) that are reading a "1" from the cell beneath them enable their corresponding Read to X gate. A signal "1" to X_n from each such Read to X gate is transmitted to the proper stage in X.

The READ pulse also clears the Initiate Read flip-flop and produces an MD RESUME signal which is sent to PDC. When the Initiate Read flip-flop is cleared to "0", the MDAC Locating Sequence resumes and CP-0 no longer produces a COINCIDENCE PROBE.

It is important to note that during the MD Read Sequence, a locating sequence occurs similar to the basic MD Locating Sequence described in subparagraph (a) above. However, in the modified sequence for reading, CP-0's not only continue to advance AIK, but also produce COINCIDENCE PROBE signals during AIK counts 0 through 4095 following a MARK PULSE. Each CP-0, however, probes for coincidence before it can actually effect the advancing of AIK by one. Therefore, during any CP-0, it is the <u>previous</u> CP-0 which corresponds to the angular position under the reading heads. This introduces a difference of one angular position in the assigning of addresses to the drum, but it is of no consequence because a similar difference exists for the writing operation.

(c) MDAC WRITE SEQUENCES. - Because the execution of some instructions requires that only the u-address or v-address portion of a word be altered, three writing sequences are used in the MD Storage System as follows: the MDAC Write (0-35) Sequence, the MDAC Write (0-14) Sequence, and the MDAC Write (15-29) Sequence. These sequences, though different in the number of bits they cause to be stored, are nevertheless similar in that each locates the storage address at which the writing is to be done and executes the transmission from X to MD when the referenced address is located. The following discussion describes only the MDAC Write (0-35) Sequence. Similar explanations apply to the other write sequences. The sequence described below as well as the MDAC Write (0-14) and MDAC Write (15-29) sequences can be found in tabular form in Appendix B, of this Volume.

When all 36 bits of a word stored in X are to be written on the drum, the INITIATE WRITE MD (0-35) signal is sent to MDAC from SCC to initiate the MDAC Write (0-35) SEQUENCE. At the same time the INITIATE MD REFERENCE signal is produced, and this signal, together with the group bits of the referenced storage address (SAR_{12} and SAR_{13}), is sent to the Group Detector in the MD Locating Circuit. Also, at this time the interlaced angular position bits of the referenced storage address (SAR_0 through SAR_{11}) are available to the Angular Coincidence Detector. When the referenced storage address has been located, the 36 bits in X are written on the drum and the MDAC Write (0-35) Sequence is terminated.

If the group of heads being referenced is the same as that which last functioned, the Group Detector does not change the group selection. If the currently referenced group is different from the last group to function, either or both

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of gates V05-30203 and V06-30203 are enabled and their outputs will trigger the Group Selector to make the new selection. The outputs of the Group Selector are then sent to coincidence circuits in the Group Translator. The group translator circuits produce a single enable (either GROUP 4, GROUP 5, GROUP 6, or GROUP 7) which is sent to input gates in the writing circuits of the selected group of heads.

The INITIATE WRITE MD (0-35) signal from SCC occurs simultaneously with one of the CP pulses. Although this SCC signal is used by MDAC to initiate the MDAC Write (0-35) Sequence, this sequence is actually started only on a CP-0. Hence, if the INITIATE WRITE MD (0-35) signal occurs at the same time as CP-0, the writing sequence begins immediately; if it occurs at any other time, the writing sequence is begun on the next CP-0. In any event, the INITIATE WRITE MD (0-35) signal sets the Initiate Write flip-flop V82-60074 to "1", and the "1" output of this flip-flop is used to enable gates V01-60073, V03-60073, V03-60074, V02-60074, V01-60074, and V04-60074. If the useable portion of the drum is passing beneath the heads, the first CP-0 of the sequence advances AIK and clears the Advance AIK flip-flop just as is done in the basic MDAC Locating Sequence, described in subparagraph (a). Two microseconds later, CP-1 passes through gate V01-60073, sets the Advance AIK flip-flop to "1", and also advances AIK. The count in AIK is thus increased by two, rather than one, during the first CP cycle of an MDAC Write Sequence, and from this time on, the advancing of AIK is done by CP-1's instead of CP-0's. This is because each CP-1 sets the Advance AIK flip-flop back to "1" to prevent the next CP-0 from advancing AIK. Also, because gate V03-60073 is enabled and V06-053 is disabled, COINCIDENCE PROBE signals are produced on CP-3 instead of CP-0, as is done for reading. The reason for the difference in timing is explained in detail in a subsequent paragraph.

Subsequent cycles of CP's repeat the action of this last described cycle until coincidence is detected. The latter occurs on CP-3 when the count in AIK matches the interlaced count from SAR, and a COINCIDENCE PULSE is generated by the Coincidence Detector in the MD Locating Circuit. The COINCIDENCE PULSE passes through gate V04-60074 and enters a delay circuit, W02-60074. After 1.1 microseconds, it emerges from the delay circuit and sets the Write flip-flop V83-60074 to a "1". The next CP-0 produces a pulse which produces MD RESUME to PDC. This pulse, delayed by 1.1 microsecond, clears the Write flip-flop to "0". Therefore, the "1" enable from this flip-flop lasts about 2 microseconds. This enable, applied to gate V07-60074, is used as a two microsecond MD WRITING PULSE which probes gates V03-60074, V02-60074, and V01-60074. Since these gates are enabled by the "1" output of the Initiate Write flip-flop, WRITE 30-35, WRITE 15-29, and WRITE 0-14 signals are produced for the MD writing circuits.

There are 36 writing circuits in each of the four groups of heads; one circuit for each head in the group. The writing circuit for each head consists essentially of an input gate and two Write gates (Write "1" and Write "0"). The input gates associated with a particular group of heads are enabled by the group translator circuits of the Group Selector when the corresponding group is selected to write. Each of the 36 Write "1" gates in a group is enabled if the corresponding stage of X contains a "1"; each of the 36 Write "0" gates of the group is enabled if the corresponding stage of X contains a "0" (due to the "NOT" circuits in the 36 X input lines). When the WRITE 30-35, WRITE 15-29, WRITE 0-14 signals from gates V01-60074, V02-60074, and V03-60074 pass through the input gate in

each head's writing circuit, they probe the Write gates; WRITE "1" or WRITE "0" signals are produced in each head winding. If the stage in X to which a head corresponds stores a "1", a "1" is written on the drum; if a stage in X stores a "0", its corresponding head writes a "0".

The CP-0 which passes through V07-60074 enters the delay circuit W01-60074, produces the MD RESUME signal, sets the Read Lockout flip-flops to 011, and after the 1.1 microseconds delay, clears the Write flip-flop. As a result, the next CP-1 passes through gate V02-60053 (enabled by Read Lockout flip-flops I and II) and clears the Initiate Write (0-35) flip-flop. It also passes through gate V05-60053 (enabled by Read Lockout flip-flops II and III) to set the Read Lockout flip-flops to read 100, and through gate V01-60073 to advance AIK and set the Advance AIK flip-flop to "1".

In the next CP cycle the double advance of AIK during the first CP cycle of this sequence is compensated for and the true AIK count restored. CP-3 is blocked since gate V03-60073 is disabled at the time it occurs. CP-0 merely sets the Advance AIK flip-flop to "0". CP-1 and CP-3 are blocked in Location Control and thus AIK is not advanced during this CP cycle. However, this CP-1 passes through gate V05-60053 and sets the Read Lockout flip-flops to 101. The MDAC LOCATING SEQUENCE resumes and AIK is subsequently advanced on CP-0. CP-1 continues to pass through gate V05-60053 until the Read Lockout flip-flops are set to 000. After a writing operation no reading operation can thus be performed until each Read Lockout stores a "0". This provides time for the reading amplifiers to recover from the transients produced during the writing operation.

In the MDAC Read Sequence, discussed in Subparagraph (b) above, the correspondence between angular positions on the drum and the count in AIK was defined. Coincidence is detected in that sequence on CP-0, and the reading circuits are sampled shortly after the SAR-specified angular position begins to move beneath the heads. Because writing must be accomplished in the same relative position, the double advance of AIK at the start of a writing operation, the coincidence on CP-3 for writing operations, and the subsequent 1.1 microsecond delay (initiated after CP-3) before the Write "0" or Write "1" gates are probed, provide a delayed writing operation and allow reading and writing to be performed at the same spot. That is, although AIK is producing coincidence on CP-3 during writing operations just before the specified location is positioned, the correct angular position is under the heads by the time the actual writing is done.

The MDAC Write (0-14) and MDAC Write (15-29) sequences are both similar to the MDAC Write (0-35) sequence. However, during the (0-14) sequence, gates V03-074 and V02-074 are disabled so that writing occurs only in bits 0 through 14 of the referenced drum address. A similar situation occurs during the (15-29) sequence, i.e., gates V03-074 and V01-074 are disabled so that writing occurs only in bits 15 through 29.

f. MAGNETIC CORE STORAGE SYSTEM. - The Magnetic Core Storage System consists of 36 Magnetic Core matrices and their control circuits. Each core matrix consists of 1024 toroidal cores and their control wires. The following Block Diagrams should be referenced while reading this section: System, envelope 1; Magnetic Core Storage System, envelope 2; and MCS Address Location System, envelope 6 . All of these Block Diagrams are found in Volume 7.

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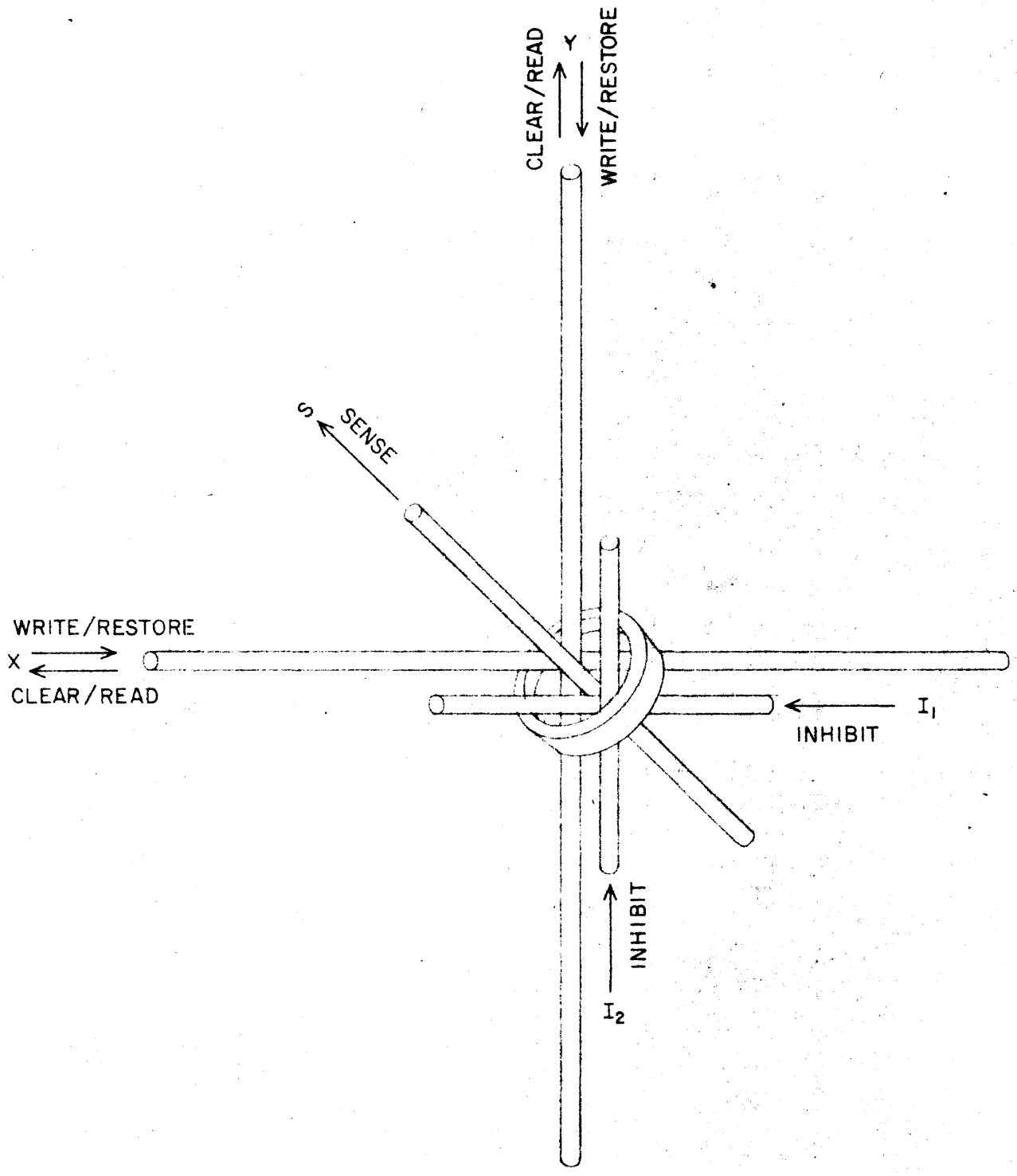

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Figure 4-12. Typical Magnetic Core and Control Wires. Arrows Indicate Direction of Current Flow During Reading or Writing

Each core is a small toroid of a material possessing an almost rectangular hysteresis loop. Five wires pass through each core as shown in Figure 4-12: a horizontal X wire, a vertical Y wire, a diagonal S wire, a horizontal I_1 wire, and a vertical I_2 wire. The core is a bistable device capable of storing a "1" or a "0", depending upon the direction of remnant magnetization in the core. In general, the "1" state is produced in a core when the resultant magnetizing force of coincident current pulses on the X, Y and I wires is of one polarity through the core, and the "0" state is produced when the resultant magnetizing force of coincident current pulses on these wires is of the opposite polarity through the core.

Reading or writing is accomplished by a sequence of current pulses through the wires. Graphs and hysteresis loops showing the specific pulse sequences for reading or writing both a "1" and a "0" are shown in Figures 4-13 through 4-18.

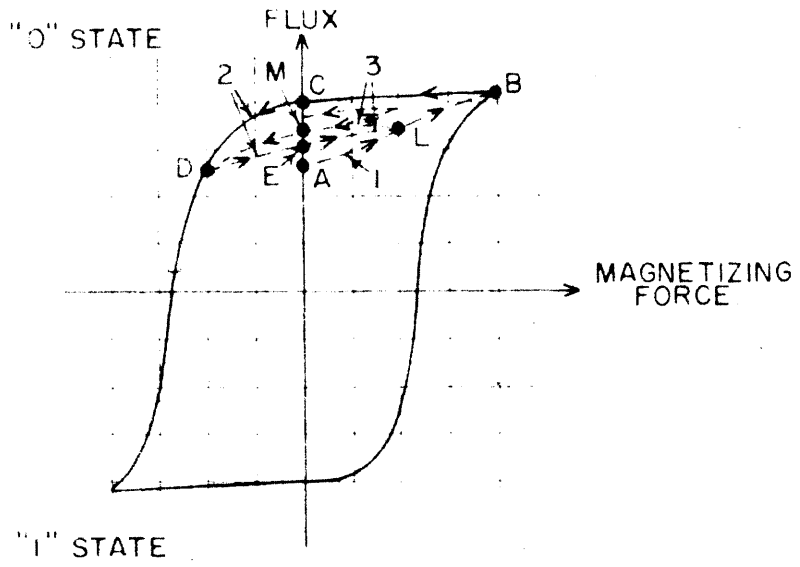
The writing of information in a single core is accomplished in three steps, as shown on Figures 4-13 through 4-16. These may be designated as the "clear", the "write", and the "disturb" steps.

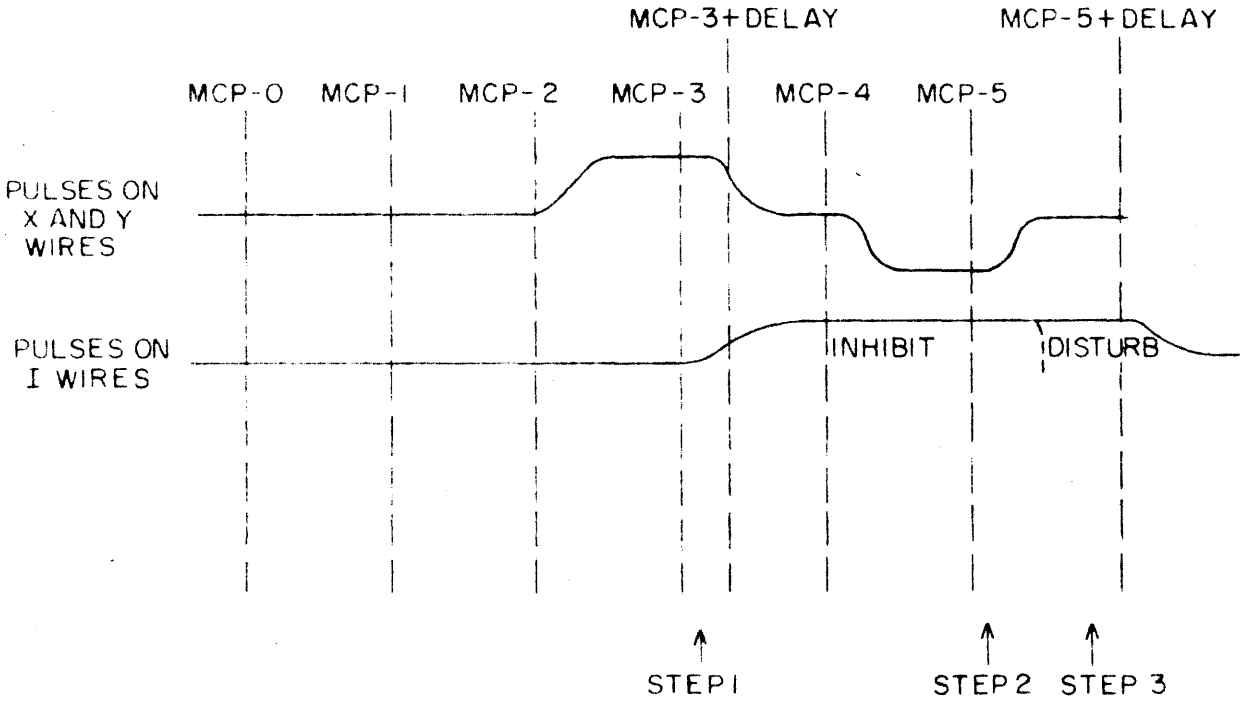
Step 1. - The "clear" step is executed by two coincident current pulses on the X and Y wires. The amplitude of these pulses is such that the combined effect of both pulses is sufficient to force the core from the "1" to the "0" state if the core is initially in the "1" state, but the occurrence of a pulse on only one of these wires does not change the state of the core. This choice of amplitude provides an "and" logic function that is used to select one particular core during writing, as explained in subparagraph (4) below, MC ADDRESS SELECTION SYSTEM.

Step 2. - After the "clear" step has forced the core to "0", the "write" step is executed which either leaves the core in the "0" state or forces the core to the "1" state. If a "1" is to be written, two simultaneous pulses of polarity opposite to the "clear" pulses are applied to the X and Y wires to force the core to the "1" state. These pulses are also of an amplitude such that both must be present simultaneously to change the state of the core. If a "0" is to be left in the core, the two coincident current pulses are applied to the X and Y wires, but their effect upon the core is cancelled by the presence of an INHIBIT pulse of opposite polarity on the I_1 and I_2 wires, occurring simulta with the X and Y pulses. The amplitude of the conditionally present INHIBIT pulse is equal to about one-half the sum of the amplitudes of the pulses used on the X and Y wires. A pulse of this value cancels the effect of the X and Y magnetizing force sufficiently to prevent the writing of a "1".

Step 3. - The third or "disturb" step is executed by a DISTURB pulse applied to the I_1 and I_2 wires. If a core was in the "1" state, the DISTURB pulse alters the state of the core along a minor hysteresis loop so that the flux "settles" to a standard "1" value which is fairly stable in the presence of positive "half-pulses" produced during references to other cores in the system.

PX 71871





STEPS (See illustrations above)

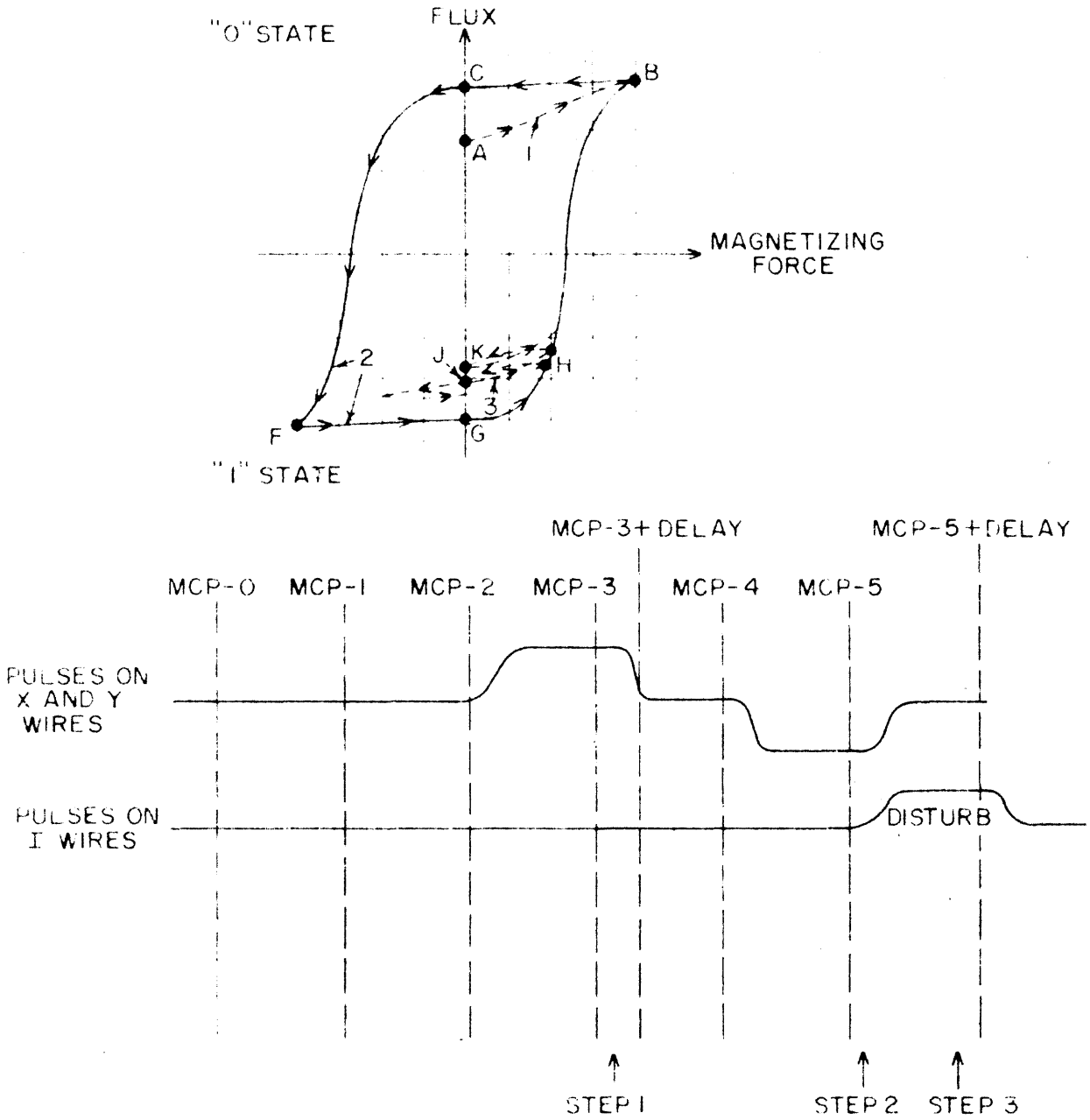
Step 1 - (CLEAR) X and Y "CLEAR" pulses shift core state from A to B to C.

Step 2 - (WRITE) Inhibit pulse on I wire cancels X or Y "WRITE" pulses so that core state is shifted from C to D to E.

Step 3 - (DISTURB) "DISTURB" pulse on I wire shifts core state from E to L to M, along a minor hysteresis loop. (Additional series of "half-pulses" of both polarities leave state of core between points A and C.)

Figure 4-13. Writing a "0" When the Core Was In the "0" State

PX 71871



STEPS (See illustrations above)

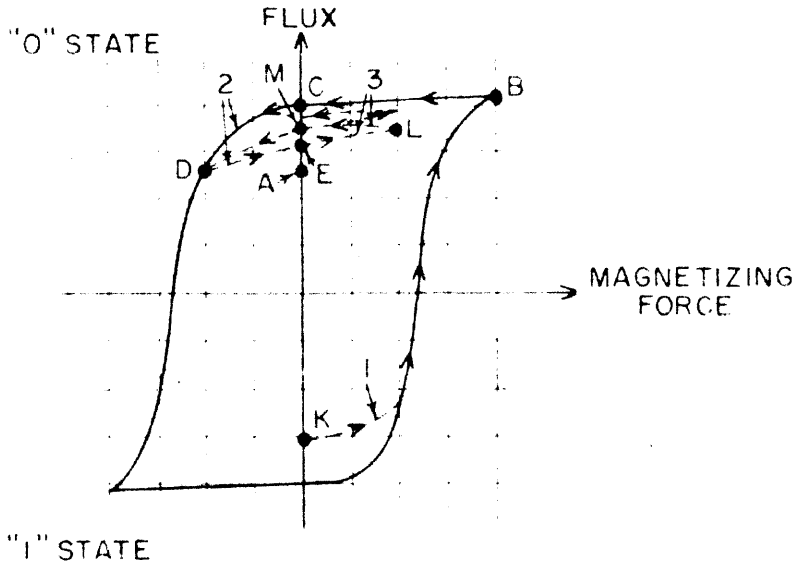
Step 1 - (CLEAR) X and Y "CLEAR" pulses shift core state from A to B to C

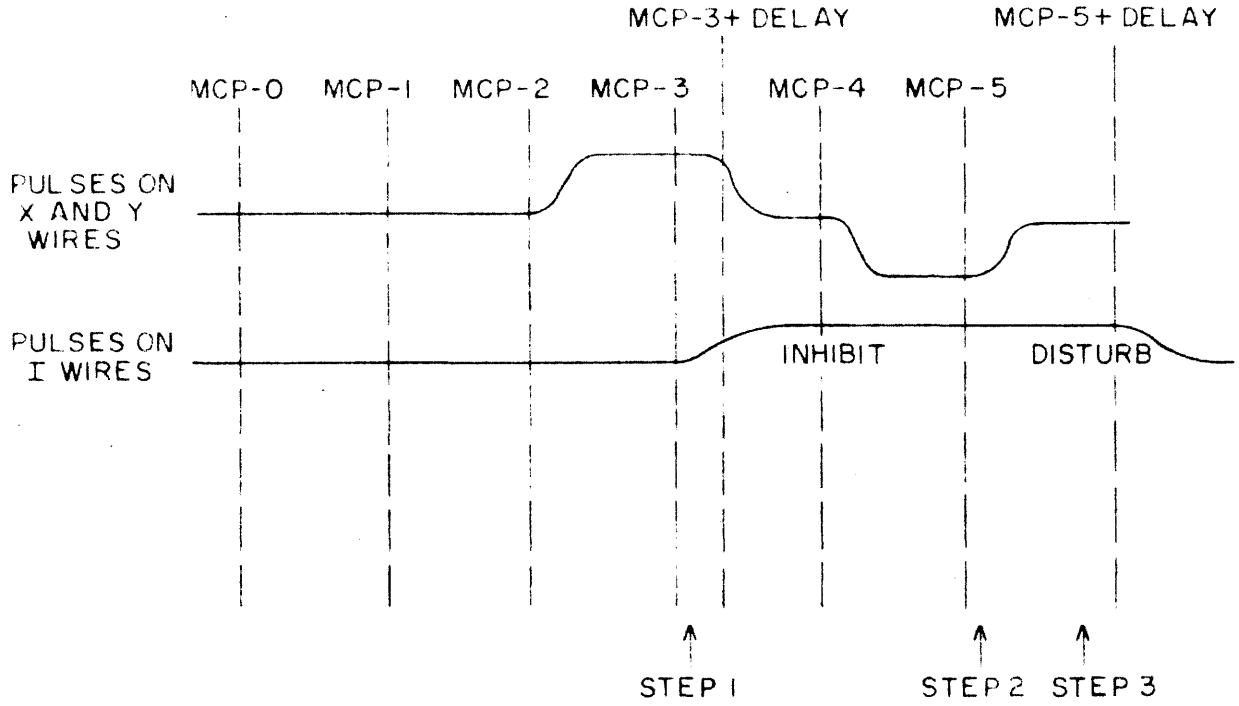
Step 2 - (WRITE) X and Y "WRITE" pulses shift core state from C to F to G

Step 3 - (DISTURB) "DISTURB" pulse on I wire shifts core state from G to H to J along minor hysteresis loop (Additional series of "half-pulses" of both polarities shift core along a minor loop and leave the state of the core between K and G.)

Figure 4-14. Writing a "1" When The Core Was In The "0" State

71871





STEPS (See illustrations above)

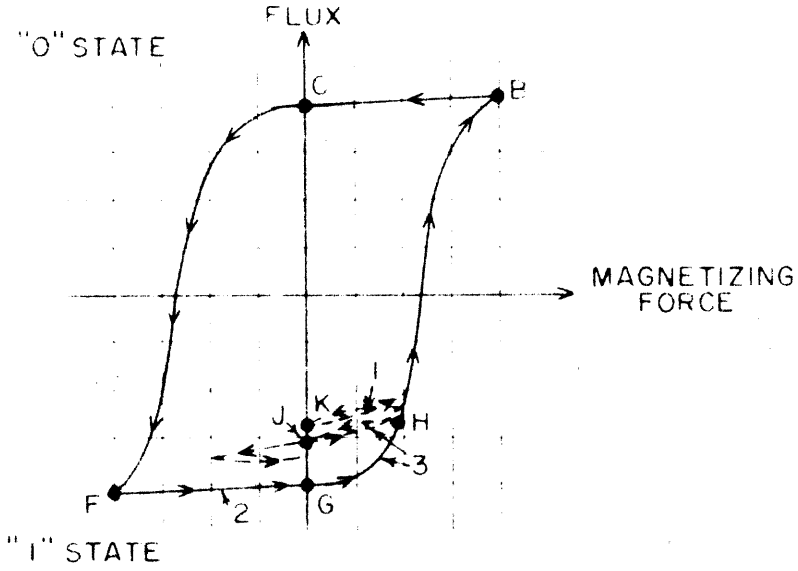
Step 1 - (CLEAR) X and Y "CLEAR" pulses shift core state from K to B to C

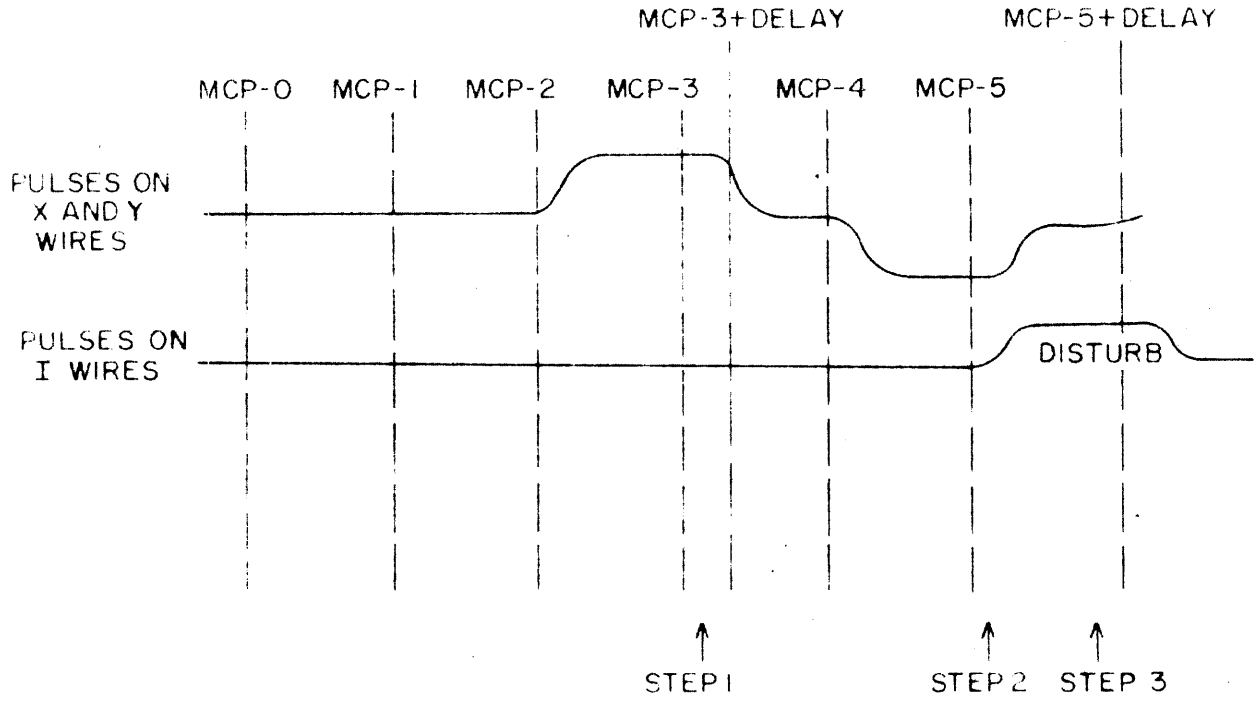
Step 2 - (WRITE) Inhibit pulse on I wire cancels X or Y "WRITE" pulses so that core is shifted from C to D to E along a minor loop

Step 3 - (DISTURB) "DISTURB" pulse on I wire shifts core state from E to L to M. (Additional series of "half-pulses" of both polarities leave the state of the core between A and C.)

Figure 4-15. Writing a "0" When The Core Was In The "1" State

PX71871





STEPS (See illustrations above)

Step 1 - (CLEAR) X and Y "CLEAR" pulses shift core state from K to B to C.

Step 2 - (WRITE) X and Y "WRITE" pulses shift core state from C TO F TO G.

Step 3 - (DISTURB) "DISTURB" pulse on I wire shifts core state from G to H to J along a minor hysteresis loop. (Additional series of "half-pulses" of both polarities shift state of core along a minor loop and leave it between K and G.)

Figure 4-16. Writing a "1" When The Core Was In the "1" State

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The reading of information from a single core is also accomplished in three steps, as shown on Figures 4-17 and 4-18. These may be designated as the "read" the "restore", and the "disturb" steps.

Step 1. - The "read" step is similar to the first step of writing in that it is executed by two coincident current pulses on the X and Y wires. If the core was initially in the "1" state the resulting flux change occurring when the core is forced from "1" to "0" produces a SENSE voltage pulse on the S wire. Therefore, during this step the reading of a "1" is represented by the presence of a SENSE pulse, and the reading of a "0" is represented by the absence of a SENSE pulse on the S wire. Because the first or "read" step destroys the presence of a "1", it is necessary to restore the "1" so that repeated readings may be made from the core. This is accomplished by the second or "restore" step.

Step 2. - The "restore" step is similar to the second step of writing. If a "1" was read from the core, the restoring of the "1" is accomplished by two coincident pulses of polarity opposite to the "read" step pulses on the X and Y wires. These pulses are also present on X and Y if a "0" was read. Their effect upon the core is cancelled by the presence of an INHIBIT pulse on the I_1 and I_2 wires, and the core is left in the "0" state.

Step 3. - The third or "disturb" step is identical to the third step of the writing sequence.

(1) GENERAL SEQUENCES OF OPERATION. - So that the functions of the various circuits of the Magnetic Core Storage System may be more clearly understood, the sequences of operations occurring in the system are explained below. The specific steps producing the sequences are explained more fully in subparagraph (7), MAGNETIC CORE ACCESS CONTROL below..

Four different sequences are produced, one for reading and three for writing. An MCS Read Sequence transmits the contents of an SAR-specified magnetic core address to X, and an MCS Write Sequence transmits the contents of X into an SAR-specified magnetic core address. MCS Write 0-14 and an MCS Write 15-29 sequences provide means of writing in only the u or v portions of storage addresses, respectively.

When a reference is made to the Magnetic Core Storage System, an INITIATE READ MCS, INITIATE WRITE MCS, INITIATE WRITE MCS (0-14), or INITIATE WRITE MCS (15-29) signal from the Storage Class Control initiates one of the four sequences by setting the Magnetic Core Pulse Distributor and Magnetic Core Access Control flip-flops. The particular settings of these flip-flops determines the type of sequence that is performed.

The MCS Write and MCS Read sequences are similar in that many of the operations used in reading are identical to operations used in writing. During the first half of either an MCS Write or a Read sequence, simultaneous CLEAR/READ

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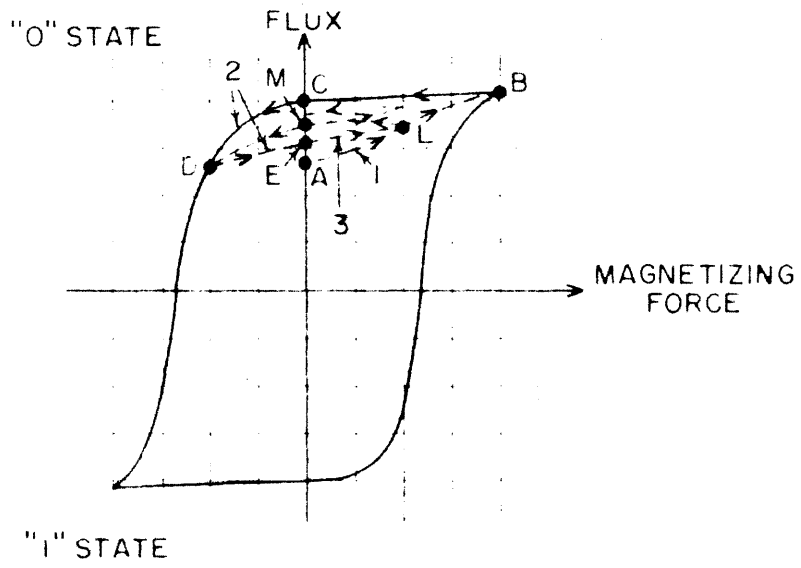

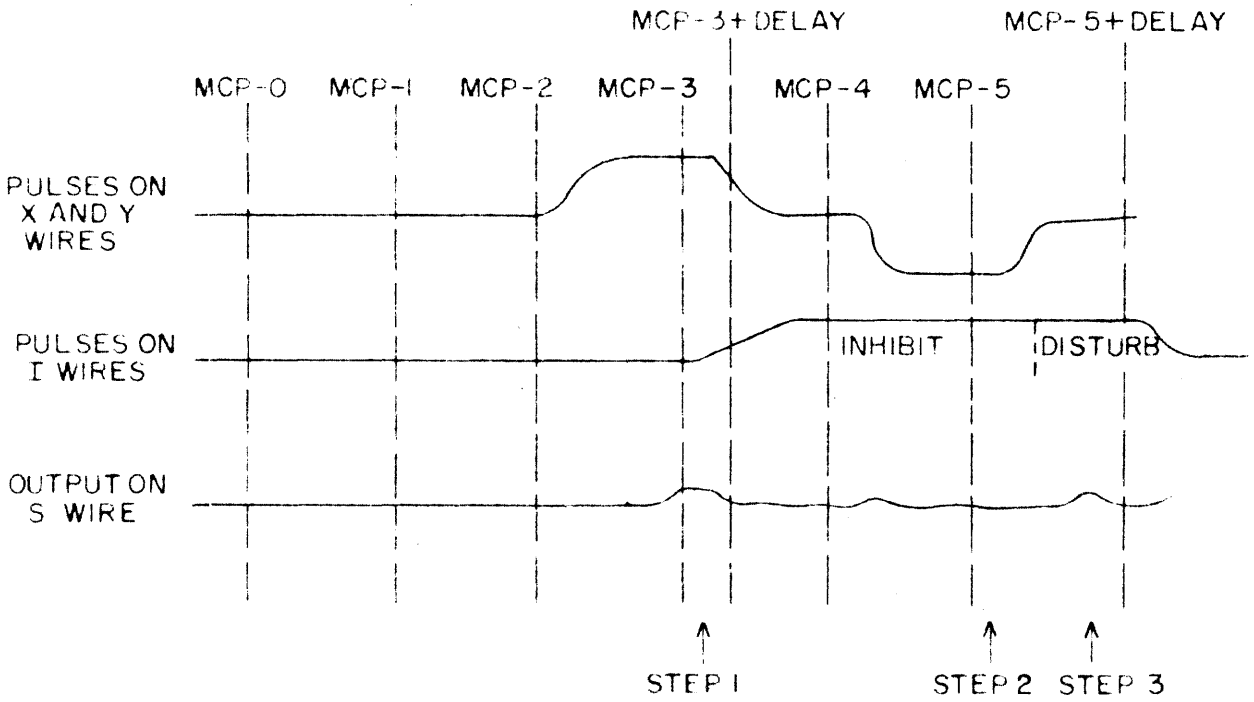

STEPS (See illustrations above)

Step 1 - (READ) X and Y "READ" pulses shift core state from A to L to B to C; no appreciable output is produced on the S wire.

Step 2 - (RESTORE) Inhibit pulse on I wire cancels X or Y "RESTORE" pulses so that core state is shifted from C to D to E.

Step 3 - (DISTURB) "DISTURB" pulse on I wire shifts core state from E to L to M along a minor hysteresis loop. (Additional series of "half-pulses" of both polarities leave the state of the core between A and C)

Figure 4-17. Reading a Core In The "0" State

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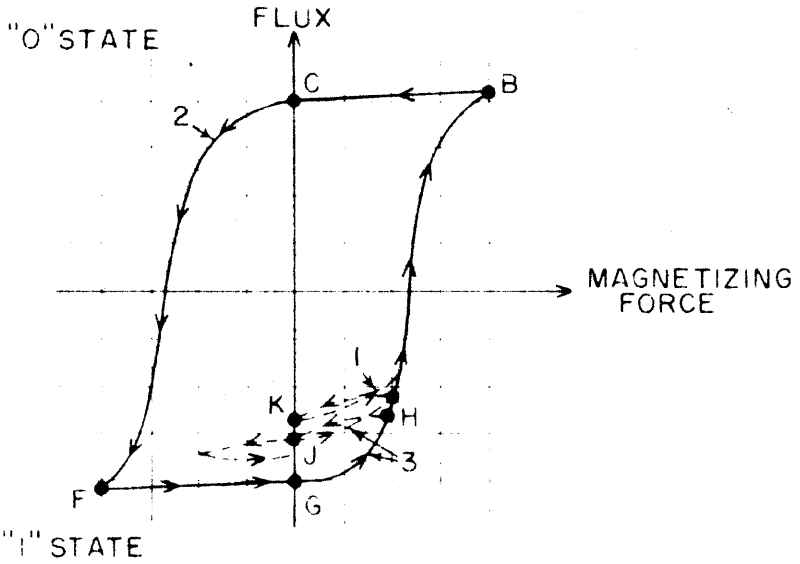

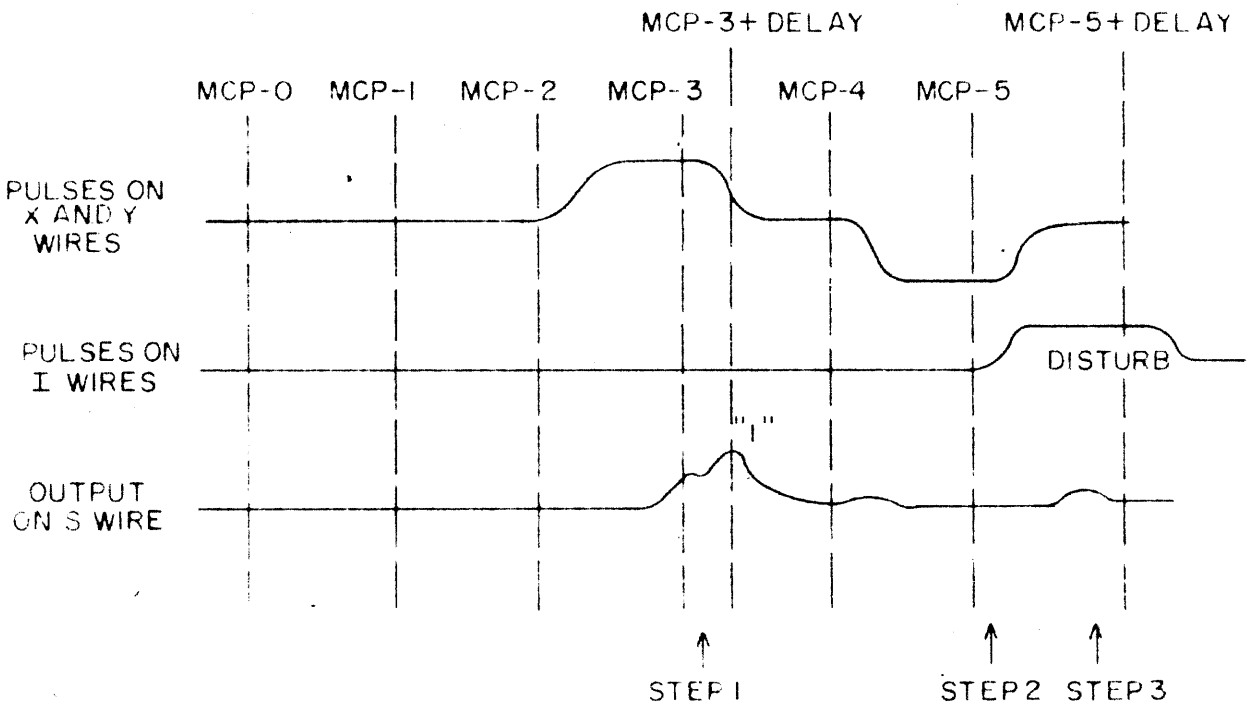

STEPS (See illustrations above)

Step 1 - (READ) X and Y "READ" pulses shift core state from K to B to C, and a "1" output is produced on the S wire.

Step 2 - (RESTORE) X and Y (RESTORE) pulses shift core state from C to F to G.

Step 3 - (DISTURB) "DISTURB" pulse on I wire shifts core state from G to H to J along a minor hysteresis loop. (Additional series of "half-pulses" of both polarities shift core along a minor loop and leave state of core between K and G.)

Figure 4-18. Reading a Core In The "1" State

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current pulses are sent to one X wire circuit and one Y wire circuit. During the last half of either a Write or Read sequence, WRITE/RESTORE current pulses, sent to the same X and Y wires, conditionally write or restore ones in the cores, depending upon the presence or absence of INHIBIT pulses on the I wires. For all sequences, a DISTURB pulse is present on the I wires after writing or restoring has been completed.

The CLEAR/READ and WRITE/RESTORE pulses for the X and Y wires are produced by current generators. When any of the four MCS sequences is initiated, the contents of the lower-order 10 stages of SAR is transmitted to an Address Register (AR). During the Write or Read sequences, a READ ENABLE, WRITE ENABLE, READ PULSE, and WRITE PULSE formed by the Magnetic Core Access Control are combined in the current generators with the outputs of the Address Register to form the CLEAR/READ and WRITE/RESTORE pulses.

The INHIBIT AND DISTURB pulses for the I wires are produced by Digit Control circuits. Each of the 36 matrices is controlled by one of these circuits during writing or restoring. If a "0" is to be left in the selected core, a "0" enable from an Input-Restore flip-flop allows an INHIBIT-DISTURB ENABLE to pass as a current pulse to the I wire. This pulse is of slightly longer duration than the WRITE/RESTORE pulse. The portion of the enable which exists during the WRITE/RESTORE pulse inhibits the writing of a "1", and the remaining portion performs the "disturb" function. If a "1" is to be written or restored in the selected core, only the final DISTURB portion of this enable is applied to the I wire.

(2) MAGNETIC CORE MATRICES. - Each matrix consists of 1024 magnetic cores and their control wires, positioned in a 32-by-32 array so that the wires all lie in the same plane. The cores are held in position by the wires, which are soldered to a square printed-circuit frame. A typical magnetic core matrix is shown in Plate 5-13.

In each matrix, all 1024 cores transmit to and receive information from the same stage of the X register. This system arrangement is economical in that it permits the 1024 cores to share common S and I wires. Furthermore, the 32-by-32 square arrangement requires only 32 X wires and 32 Y wires for 1024 cores. The circuit of the X, Y, S, and I wires is shown on the Unit Signal Diagram, 55500, found in the set of unit signal diagrams for the Magnetic Core (55000) cabinet. This diagram illustrates that there are 32 X wires, 32 Y wires, one diagonal S wire which passes through each core once, and one I wire which passes through each core twice.

The path of the sense winding is chosen so that the effects of signals from unselected cores are subtractive rather than additive. The diagonal S Wire passes back and forth over each X or Y wire an even number of times so that transients produced in the sense winding by pulses on the X and Y wires tend to cancel each other.

When writing (or reading) is to be performed in a particular core address, a Magnetic Core Write (or Read) sequence produced by the Magnetic Core Access Control first sends CLEAR/READ pulses simultaneously to one of the 32 X wires and to one of the 32 Y wires. In the core located at the junction of these two lines, the additive effect of both pulses performs the first step of writing

(or reading) by forcing the core to the "0" state. On the pulsed X and Y wires, 62 other cores each receive only a single pulse (called a "half-pulse" because it is of one-half the amplitude required to change the state of a core), and therefore are not affected.

Next, a WRITE/RESTORE pulse of the opposite polarity on the same X and Y wires attempts to force the selected core to the "1" state. If the core is to be left in the "0" state, an INHIBIT-DISTURB pulse is sent to the matrix I wire to inhibit the writing of a "1". The INHIBIT-DISTURB pulse starts before the WRITE/RESTORE pulse and lasts until two microseconds after the WRITE/RESTORE pulse. The last two microseconds of this pulse perform step 3 of writing or reading.

If the core is to be left in the "1" state, a DISTURB pulse is sent to the matrix I wire instead of an INHIBIT-DISTURB pulse. The DISTURB pulse starts when the WRITE/RESTORE pulse ends, and lasts two microseconds. This two-microsecond pulse performs step 3 of writing or reading.

During the first step of a reading sequence, when a "1" is changed to a "0", the pulse induced on the diagonal S wire is rectified and amplified to form a positive SENSE pulse which indicates that a "1" is being read. Although pulses may be induced on the S wire during a writing sequence, these are not utilized by the system.

(3) MAGNETIC CORE MATRIX ASSEMBLY. - The Magnetic Core Matrix Assembly consists of a vertical stack of 36 matrices, mounted in the 55000 cabinet. This assembly is shown in Plate 5-12, Volume 6.

Vertical jumpers on the matrix connectors provide 64 series paths through the X and Y wires for the X and Y current pulses. This includes 32 paths for wires X_0 through X_{31}, and 32 paths for wires Y_0 through Y_{31}. The 32 Y inputs are connected to the bottom right and bottom left edges of the stack, and the 32 X inputs are connected to the bottom front and bottom rear of the stack. At the top end of the stack, the 64 series X and Y circuits are connected to terminating resistors mounted above the stack.

For each matrix, two wires provide connection for the I matrix wire and two wires provide connection for the S matrix wire. The electrical connections to these terminals and to the 64 X and Y circuits are tabulated in the Unit Signal Diagram, 55500, found in the set of unit signal diagrams for the Magnetic Core (55000) Cabinet.

(4) MC ADDRESS SELECTION SYSTEM. - The circuits used in address selection are shown on the Block Diagram, Magnetic Core Address Selection System. These consist of the Address Register, the Read/Write Pulse Generators, the Read/Write Enable Generaters, and the X and Y Drivers. These circuits distribute CLEAR/READ and WRITE/RESTORE current pulses to the matrix assembly X and Y wires so that reading or writing is executed in one particular core address.

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When a write or a read reference is made to the Magnetic Core Storage System, circuits of the 1103 equipment Control System transmit the contents of SAR stages 0 through 9 to the 10-stage Magnetic Core Address Register (AR). During each MCS Read or Write sequence, the Read/Write Pulse Generators and Read/Write Enable Generators combine the AR enables with the READ ENABLE, WRITE ENABLE, READ pulse and WRITE pulse from the Magnetic Core Access Control. The resulting signals operate the X and Y Drivers which send positive and negative current pulses to the X and Y wires.

(a) READ OR CLEAR PORTION OF CYCLE. - During the first step in an MCS Write or Read Sequence, the lower-order five stages of AR designated as AR_0 through AR_4 provide enables for generating the X wire pulses. The enables from AR_3 and AR_4 and a READ ENABLE from MCAC combine in the crystal AND circuits of the Read/Write Enable Generators to form one of the following four READ enables: READ 00XXX, READ 01XXX, READ 10XXX, or READ 11XXX. The enables from AR_0, AR_1, and AR_2 and a READ PULSE (the first pulse to arrive on the READ/WRITE pulse line from MCAC) are combined by the Read/Write Pulse Generators to form one of the following eight READ pulses: READ XX000, READ XX001, READ XX010, READ XX011, READ XX100, READ XX101, READ XX110, or READ XX111.

The X Drivers produce one of 32 CLEAR/READ current pulses, i.e., READ X 0, READ X 1, READ X 2, etc., depending upon the particular READ pulse produced by the Read/Write Pulse Generators and the particular READ enable produced by the Read/Write enable generator. This is accomplished because the driver tubes are connected in an array that permits the use of "and" logic in the selection of each driver tube. For example, only one of the 64 X Drivers produces READ X 13, and this driver is connected so that it will only produce READ X 13 when a READ 01XXX enable is present on the grid, AND a READ XX101 pulse is present on the cathode. The circuit used to produce the CLEAR/READ and WRITE/RESTORE pulses for each matrix wire consists of a duo-triode, connected in "push-pull" fashion to an output transformer. Only one half is used to produce the CLEAR/READ pulse, and the other half is used to produce the WRITE/RESTORE pulse. Because of the manner in which the triodes are connected, the signal on the output line of the transformer is either a CLEAR/READ pulse (during the first step in a cycle), or a WRITE/RESTORE pulse of the opposite polarity (during the second step of a cycle).

It should be noted that the combination of the "1" and "0" bits in the names READ 01XXX and READ XX101 forms 01101, the binary equivalent of 13. This number corresponds to the number designation of the X wires that receive the current pulse, i.e., the X 13 wire of each matrix receives the READ X 13 pulse.

The other portions of the MC Address Selection System, consisting of AR_5 through AR_9, the Y Drivers, and the remaining Read/Write pulse and enable generators, function in a manner similar to the X half, described above. During the first step in an MCS Write or Read Sequence, the contents of AR_5 through AR_9 provide enables for generating one of 32 CLEAR/READ current pulses, i.e., READ Y 0, READ Y 1, READ Y 2, etc.

In each core matrix, the receipt of one of the 32 CLEAR/READ current pulses for X and one of the 32 CLEAR/READ pulses for Y clears (or reads) one of the 1024 positioned in one of the 1024 intersections of the X and Y wires. In this

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manner, each of the 1024 possible values in AR directs reading operations to one core in each of the 36 matrices. The values in AR represent 10-bit addresses obtained from SAR, and therefore, the MC Address Selection System provides access to 1024 addresses each having 36 bits.

(b) WRITE OR RESTORE PORTION OF CYCLE. - During the second step in an MCS Write or Read sequence, the Address Selection System functions in a manner similar to that described in the preceding subparagraph, except that the presence of a WRITE ENABLE from MCAC causes the Read/Write Enable Generators to produce WRITE enables designated as WRITE 00XXX, WRITE 01XXX, WRITE 11XXX, etc.

The X Drivers produce one of 32 WRITE/RESTORE pulses, i.e., WRITE X 0, WRITE X 1, WRITE X 2, etc., depending upon the particular pulses and enables produced in the circuitry. Similarly, the Y Drivers also produce one of 32 WRITE/RESTORE pulses, i.e., WRITE Y 0, WRITE Y 1, WRITE Y 2, etc. Because of the manner in which the triodes are connected to the output transformer, the WRITE/RESTORE pulse is of opposite polarity to the CLEAR/READ pulse, in the secondary winding of the transformer.

(5) DIGIT CONTROL CIRCUITS. - A Digit Control circuit is associated with each of the 36 magnetic core matrices. Each of these is essentially one stage of a 36-stage Input Register, which serves as a temporary storage medium for the bits of a word written into or read from a core address.

(a) OPERATION DURING A WRITE SEQUENCE. - During an MCS Write Sequence, the Digit Control Circuits function as a 36-bit input register which stores "0" or "1" bits while they are being written in one core address.

At the beginning of the sequence, MCP-1 clears all 36 stages to "0". During the remainder of the sequence, the particular operations performed in each Digit Control circuit depends upon the type of writing operation being executed, and whether a "1" or a "0" is to be written.

If a partial write sequence is initiated, writing will occur in only 15 of the Digit Control circuits, and the remaining circuits will execute operations similar to the Read sequence operations, except that the absence of an MCS→X pulse from MCAC prevents "1" pulses from being transmitted to X. If the initiating signal is INITIATE WRITE MCS 0-14, only Digit Control circuits 0 through 14 execute writing operations, and if the initiating signal is INITIATE WRITE MCS 15-29, writing is executed only by circuits 15 through 29. If INITIATE WRITE MCS is received, writing occurs in all 36 circuits. The operation of Digit Control circuit 0 is explained below.

If writing is to be executed in stage 0 and a "1" is present in X_0, IR_0 is first cleared. Next, the "clear" step in the sequence serves only to clear the selected core of Matrix 0 to "0". At the beginning of the "write" step, a WRITE MCS 0-14 pulse from MCAC passes through gate V05-251 to set IR_0 to "1". The WRITE X and WRITE Y current pulses from the MC Address Selection System force the core to the "1" state. The "disturb" step is similar to the "disturb" step of the Read sequence, and is produced by the simultaneous presence of the ENABLE INHIBIT-DISTURB and DISTURB enables from MCAC.

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If writing is to be executed and a "0" is in X_0, IR_0 is first cleared. Next, the "clear" step clears the core to "0". However, the absence of a "1" enable from X_0 leaves gate V05-251 disabled so that at the beginning of the "write" step the WRITE MCS 0-14 pulse fails to set IR_0 to "1". The "0" enable from IR_0 enables V06-251 so that the ENABLE INHIBIT DISTURB signal produces an INHIBIT current on the matrix I wire; the writing of a "1" is inhibited, and thus the core is left in the "0" state. The "disturb" step is produced during the last portion of ENABLE INHIBIT-DISTURB when the DISTURB pulse is received from MCAC.

The above operations are similar for each of the other circuits 1 through 35 if writing is being executed in those stages. Digit Control Circuits which are to function for writing receive one of the following signals from MCAC: WRITE MCS 0-14, WRITE MCS 15-29, or WRITE MCS 30-35. Circuits which are not writing receive one of the following signals instead: RESTORE MCS 0-14, RESTORE MCS 15-29, or RESTORE MCS 30-35.

(b) OPERATION DURING A READ SEQUENCE. - During an MCS Read sequence, the Digit control circuits function as a 36-bit restoration register, which restores the information destroyed by the reading operation.

At the beginning of the sequence, MCP-1 clears all 36 flip-flop stages to "0". During the remainder of the sequence, the particular operations performed in each Digit Control circuit depends upon whether or not a "1" is read from the associated matrix. Because each Digit Control circuit is similar electrically to any of the 35 other circuits, only the functioning of Digit Control circuit 0 (IR_0) is explained below.

If a "1" is present in the selected address of Matrix 0, a SENSE signal is received from the matrix SENSE wire during the first "read" step of the sequence. This signal enables two gates. Gate V03-251 passes an MCS $\rightarrow$ X pulse received from MCAC at this time, to produce a "1" from MCS_0 pulse which sets stage 0 of the X register to "1". Gate V04-251 passes a RESTORE MCS 0-14 pulse, which is received simultaneously with the SENSE pulse, to set IR_0 to "1". During the second or "restore" step of the sequence, the selected core of Matrix 0 is reset to "1", and as a result the "1" read from the core is restored. During the third or "disturb" step, a third gate, V06-251, is enabled by a DISTURB enable from MCAC and pulsed by an ENABLE INHIBIT-DISTURB signal also from MCAC. The resulting DISTURB pulse, applied to the matrix I wire, standardizes the residual flux in the cores.

If a "0" is present in Matrix 0, no SENSE signal is received. As a result, IR_0 will remain in the "0" state and no signal will be sent to the X register. During the second or "restore" step of the sequence the "0" enable from IR_0 enables gate V06-251 so that the ENABLE INHIBIT-DISTURB signal from MCAC produces an INHIBIT current on the I wire of the matrix, and as a result the writing of a "1" in the core is inhibited. The core remains in the "0" state. During the "disturb" step the DISTURB pulse from MCAC is applied to V06-251; however, V06-251 is already enabled, because of the OR circuit and the "0" in IR_0. The final portion of the ENABLE INHIBIT-DISTURB signal from MCAC passes through the gate to form a DISTURB pulse, which is applied to the I wire of the matrix.

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The above operations are similar for Digit Control circuits 1 through 35. During the "restore" step circuits 0 through 14 receive RESTORE MCS 0-14, circuits 15 through 29 receive RESTORE MCS 15-29, and circuits 30 through 35 receive RESTORE MCS 30-35.

(6) MAGNETIC CORE PULSE DISTRIBUTOR. - The Magnetic Core Pulse Distributor is a three-stage binary counter which distributes CLOCK PULSES as a series of magnetic core control pulses, MCP-1 through MCP-5. Preceding these, control pulse MCP-0 is produced when INITIATE READ MCS or any of the three INITIATE WRITE MCS signals is received from SCC. This pulse sets the count in the MCPD flip-flops to the binary value 001. The resulting MCPD enables cause the next CLOCK PULSE to be distributed as MCP-1. This MCP-1 pulse advances the count in MCPD to 010 and the next CLOCK PULSE is distributed as MCP-2. Similar operations occur for MCP-3 and MCP-4. The last pulse, MCP-5, clears all three MCPD flip-flops to "0" and no additional pulses are produced until the next read or write reference is made to Magnetic Core Storage.

Two delay circuits produce two additional distributor pulses. Delay W01-194 produces a delayed MCP-3 pulse (MCP-3+ delay) which occurs between MCP-3 and MCP-4, and delay W02-194 produces a delayed MCP-5 (MCP5 + delay) which occurs two microseconds after MCP-5.

(7) MAGNETIC CORE ACCESS CONTROL. - During each sequence of six MCP's, the MCAC circuits produce signals for operating the Address Location System, the Address Monitor, and the Digit Control Circuits. The sequences are presented in tabular form in Appendix B, under the MCAC heading.

The current generators, which produce the CLEAR/READ and WRITE/RESTORE current pulses for the matrix X and Y wires, are operated by a READ ENABLE, a WRITE ENABLE, a READ PULSE, and a WRITE PULSE. During the first half of either a read or a write sequence, the read enable is started when MCP-0 sets the Enable Read flip-flop to "1", and is terminated when MCP-3 clears this flip-flop. During the last half of the sequence, the WRITE ENABLE is started when MCP-3 sets the Enable Write flip-flop to "1", and is terminated by MCP-5. The Read/Write I and II flip-flops are set and cleared in a manner so that their combined "1" and "0" outputs produce two enables of short duration, one starting at MCP-2 called the READ pulse, and one starting at MCP-4 called the WRITE pulse. In the Address Location System, these pulses are used to operate drivers which produce the CLEAR/READ and RESTORE/WRITE current pulses for the matrices.

The Address Monitor, which provides a visual indication of the address to which a reference is being made, is controlled partially by MONITOR GRID PULSES produced by the Monitor Intensity flip-flop. During either an MCS read or an MCS Write sequence, MCP-1 sets the Monitor Intensity flip-flop to "1" and MCP-5 clears this flip-flop to "0". The resulting eight-microsecond MONITOR GRID PULSE increases the intensity of the cathode ray beam so that the address being referenced is represented on the Address Monitor screen as a bright spot.

The Digit Control Circuits, which control the writing or restoring of "1's" and "0's" in core matrices, are operated by the INHIBIT-DISTURB ENABLE, the DISTURB signal, and by combinations of MCS→X, RESTORE MCS 0-14, RESTORE MCS 15-29, RESTORE MCS 30-35, WRITE MCS 0-14, WRITE MCS 15-29, and WRITE MCS 30-35.

During either a read or a write sequence, the INHIBIT-DISTURB ENABLE is started when MCP-3 sets the Enable I/D flip-flop to "1", and is terminated by delayed MCP-5. The resulting enable, which is started coincidently with the WRITE ENABLE, is conditionally gated in the Digit Control circuits to inhibit the writing of a "1". The DISTURB signal is started when MCP-5 clears the Disturb II flip-flop to "0" and is terminated when delayed MCP-5 clears the Disturb I flip-flop. This signal operates in the digit control circuit so that the last two microseconds of the INHIBIT-DISTURB ENABLE is always applied to the I wires of the matrices, regardless of whether a "1" or a "0" is being written. It is this portion of the INHIBIT-DISTURB ENABLE which disturbs the cores to make them assume a standard flux valve.

The combinations of other signals used to operate the Digit Control Circuits depends upon the type of initiating signal received from SCC. If an INITIATE READ MCS signal has been received, the Read to X flip-flop will be in the "1" state, and delayed MCP-3 produces an MCS → X signal which transmits the 36-bit word read from the cores to the X register. If an INITIATE WRITE 0-14 signal has been received, the W/R 0-14 flip-flop will be in the "1" state, and MCP-3 will produce a WRITE MCS 0-14 signal to matrices 0 through 14. If an INITIATE WRITE 15-29 signal has been received, the W/R 15-29 flip-flop will be in the "1" state so that MCP-3 produces WRITE 15-29. If INITIATE WRITE MCS has been received, WRITE MCS 0-14, WRITE MCS 15-29, and WRITE MCS 30-35 will be sent to the 36 Digit Control circuits. In all four sequences, Digit Control circuits which do not receive one of these three types of WRITE signals on MCP-3 receive a correspondingly numbered RESTORE MCS 0-14, RESTORE MCS 15-29, or RESTORE MCS 30-35 signal on delayed MCP-3. These WRITE and RESTORE signals cause the Digit Control circuits either to write or restore "1"s or "0"s in the cores.

(8) ADDRESS MONITOR. - The Address Monitor, a five-inch cathode ray tube mounted at the top of the S$_0$ Control Panel, provides an indication in one of 1024 positions each time a read or a write reference is executed in the 1024-address rapid access storage system.

g. STORAGE IN Q AND A. - The Q-register and Accumulator are individually addressed, and each provides rapid-access storage for one computer word. The Q-register is assigned address 1----, and the Accumulator is assigned address 2---- (the lowest four octal digits are of no significance).

Access to these registers is controlled by the Arithmetic Register Access Control (ARAC). The execution of ARAC Read and Write sequences control transmissions to and from Q and A when the u and/or v address portions of an instruction word contain either a Q or A address. ARAC has the additional function of controlling the clearing of A during the execution of those instructions which require that information obtained from internal storage locations be transmitted to A from X as a result of an arithmetic rather than a storage operation.

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The u-address portion of an instruction word is the Q or A address if it is desired that an operation be performed on an operand already present in Q or A. In such a case the internal storage reference operation involves an SCC Initiate Read Q or an SCC Initiate Read A sequence which sends an INITIATE READ Q or an INITIATE READ A signal to ARAC. Depending on the instruction being executed, ARAC then executes the appropriate ARAC Read sequence for the register referenced.

If it is desired to retain the results of an operation performed in Q or A, the v-address portion of an instruction word is either the Q or A address. In such a case the internal storage reference operation involves an SCC Initiate Write Q or an Initiate Write A sequence which sends an INITIATE WRITE Q or INITIATE WRITE A signal to ARAC. Depending on the instruction being executed, ARAC then carries out the appropriate ARAC Write sequence for the register referenced.

During the execution of certain instructions, an operand, which was obtained from an internal storage location and transmitted to X, is inserted into A by an arithmetic operation rather than by an internal storage reference involving A. During the execution of these instructions, ARAC appropriately clears A to prepare A for the arithmetic operation which transmits data from X into A.

(1) STORAGE PROPERTIES OF Q AND A. - The Q-Register, Q, is a 36-stage flip-flop shifting register which can store a single 36-bit computer word. Q is assigned the octal address 1----. When Q is used as a storage register, its shifting property is not utilized. If Q is referenced by the u-address portion of an instruction word, one of the ARAC Read sequences for a Q reference is executed. Each ARAC Read sequence for a Q reference complements X and executes the transmission $Q^{\circ} \rightarrow X^{\circ}$. In the execution of some instructions where Q is referenced by the u-address portion of the instruction, A_R is cleared during the ARAC Read sequence; in the execution of other instructions, both A_R and A_L are cleared; and in the execution of still other instructions, neither A_R nor A_L is cleared. When Q is referenced by the v-address portion of an instruction word, an ARAC Write sequence for a Q reference is executed. This sequence clears Q and transmits the "1°s" stored in X to corresponding stages in Q. The content of A is not affected in any way.

As a storage register the Accumulator, A, is a 72 stage subtractive flip-flop register. During all transmissions into A in storage references, A acts as a 72-stage subtractive register; during all transmissions out of A, however, only the right-most 36 stages of A, A_R, are involved and A_R functions much the same as any flip-flop storage register. Depending on the instruction being executed, the bits of A involved in storage references can be either a single length (36-bit) word or a double length (72-bit) word. A is assigned the octal address 2----. The only restriction placed on A as a storage location is that it cannot be referenced to pick up the next instruction of a program.

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When A is referenced by the u-address portion of an instruction word, one of the ARAC Read sequences for an A reference is executed. The particular ARAC Read sequence carried out depends on the instruction being executed. Some instructions whose u-address references A require that (A_R) be transmitted to X. In such cases, an ARAC Read A sequence for an A reference is produced which

simply carries out the transmission $A_R \rightarrow X$. That is, X is cleared and gates in the "1" output circuits of A_R are sampled by the $A_R \rightarrow X$ signal from ARAC; those gates enabled by "1" outputs from their associated stage in A_R set their associated stage in X to "1". It should be noted that only the 36-bit word stored in A_R is transmitted. In other instructions wherein the u-address references A, the instruction requires that (A) be retained in A. In the execution of these instructions, the ARAC Read sequence for an A reference produced does not affect (A) in any way. Such instructions can thus reference (A) as a double length word. After some ARAC Read sequences, A is cleared; after others, only A_R is cleared; and after some, neither A_R nor A_L is cleared.

When A is referenced by the v-address portion of an instruction word, one of the ARAC Write sequences for an A reference is executed. During the execution of those instructions which require that a 36-bit operand be stored in A from X, an ARAC Write sequence is produced which clears both A_R and A_L and carries out an Add X to A sequence. The latter sequence transmits (X) to A by effectively adding D(X) to A, where D(X) is a double-length number whose right-hand 36-bits are equal to (X) and whose left hand 36-bits are the same as the leftmost (sign) bit of the word stored in X. During the execution of other instructions which require that (A) be retained in A, an ARAC Write sequence is executed which suppresses the writing operation and leaves (A) undisturbed. These latter instructions can reference (A) as a double length word.

(2) ARITHMETIC REGISTER ACCESS CONTROL. - The Arithmetic Register Access Control, ARAC, has the following functions: it produces the appropriate ARAC sequence during internal storage references to Q and A so that the required transmission, if any, is carried out; it produces an ARAC RESUME signal for PDC when the ARAC sequence being executed is completed; and it controls the clearing of A during the execution of certain instructions so that A is properly prepared for subsequent receipt of data. ARAC is shown on the Block Diagram, Arithmetic Register Access Control, in Envelope #2 of Volume 7.

The particular ARAC sequence carried out by ARAC during an internal storage reference to Q or A depends not only on which signal is received from SCC (INITIATE READ Q, INITIATE READ A, INITIATE WRITE Q, or INITIATE WRITE A), but also which instruction is being executed. The following sub-paragraphs describe the ARAC sequences. These sequences can be found in tabular form in Appendix B, Pages B-71 through B-76 of this volume.

(a) ARAC READ SEQUENCES. - When either Q or A is referenced by the u-address portion of an instruction word, one of the Read sequences is carried out. The particular sequence executed depends on which instruction is in program control. As an example of how all ARAC Read sequences are initiated and executed, the ARAC Read Sequence, Instruction 27 (Q Reference) is described in detail. The other ARAC Read sequences are then discussed in comparison to this sequence.

1. ARAC READ SEQUENCE, INSTRUCTION 27. - The first internal storage reference in the execution of the Controlled Complement (27uv) instruction requires that an operand be transmitted from address u into the 36 lower-order stages of A, A_R, and that the 36 higher-order stages of A, A_L, remain unchanged in the process.

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a. Q REFERENCE. - On MP 0, during the execution of a 27uv instruction, ARAC receives an INITIATE CLEAR A signal from CTC. Simultaneously, in other sections of the machine, X is cleared, (UAK) → SAR and INITIATE READ signals are sent to SCC, and MPD is stopped. (See APPENDIX B, Page B-15, Volume 2.) In ARAC the INITIATE CLEAR A signal sets the Clear A flip-flop, V81-30133, to "1". In SCC, the INITIATE READ signal sets the Initiate Read flip-flop to "1". As in all internal storage references, SCT translates the five higher-order bits of the address held in SAR and supplies Q-reference enables for SCC, ARAC, and the Fault Detector. The first CONTROLLED CLOCK PULSE to occur after MP 0 passes through gates V08-30133 and V07-30133 in ARAC, clears the Clear A flip-flop, and is sent as a CLEAR A_R signal to A. (A_L is not cleared since gate V06-30133 in ARAC is not enabled during the 27uv instruction.) In SCC the same CONTROLLED CLOCK PULSE produces an SCC INITIATE READ Q sequence which clears the Initiate Read flip-flop in SCC, and sends an INITIATE READ Q signal to ARAC. In ARAC this latter signal sets the Read Q flip-flop V82-30133 to "1" and continues on to X as a COMPLEMENT X signal. The next CONTROLLED CLOCK PULSE to occur passes through gate V11-30133 in ARAC, clears the Read Q flip-flop, achieves the Q' → X' transmission, and passes on to PDC as an ARAC RESUME signal. The contents of Q are thus transmitted to X.

b. A REFERENCE. - The same preliminary operations are performed on MP 0 as during a Q reference. Also in ARAC when the first CONTROLLED CLOCK PULSE occurs, A_R is cleared in the same manner as during a Q reference, except that gate V07-30133 is enabled by the NOT MCT 41, 54, or 74 circuit rather than by a Q reference enable. In SCC, however, the first CONTROLLED CLOCK PULSE produces an Initiate Read A sequence which issues an INITIATE READ A signal to ARAC. In ARAC this latter signal passes through gate V03-30143 (also enabled by the NOT 41, 54, or 74 circuit) and is sent to A as an $A_R \rightarrow X$ signal and to PDC as an ARAC RESUME signal. The contents of A_R are thus transmitted to X, and A_L is left undisturbed.

c. MD and MC REFERENCES. - When MD and MC storage references are made during the execution of the 27uv instruction, ARAC receives the INITIATE CLEAR A signal from CTC on MP 0 and merely clears A_R. (During these references gate V07-30133 is enabled by an MD or MC reference enable from SCT.)

2. ARAC READ SEQUENCE, INSTRUCTION 41, 54, or 74. The Index Jump (41uv), Left Shift A (54uk) and Scale Factor (74uv) Instructions all require that the operand read from address u to X be ultimately inserted into A. The transmissions from the u address to X for Q and A references involve the ARAC Read sequences outlined below. The transmissions from the u-address to X for MD and MC references involve ARAC only in the preparation of A for subsequent receipt of the u-address operand.

a. Q REFERENCE. - The ARAC READ sequence for a Q reference for the 41 uv, 54 uv, and 74 uv instructions is exactly the same as for the 27 uv instruction except that both A_R and A_L are cleared. The contents of Q are transmitted to X by the usual COMPLEMENT X and Q' → X' signals, and an ARAC RESUME signal is sent to PDC.

b. A REFERENCE. - When the u-address portion of instructions 41 uv, 54 uv, and 74 uv reference A, the resulting ARAC Read sequence suppresses the usual clearing of A and the transmission $A_R \rightarrow X$. That is, the

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contents of A are left undisturbed. The INITIATE CLEAR A signal on MP 0 sets the Clear A flip-flop. The next CONTROLLED CLOCK PULSE in ARAC merely clears the Clear A flip-flop. The INITIATE READ A signal from SCC passes through gate V02-30143 and is issued to PDC as an ARAC RESUME.

c. MD or MC REFERENCES. - ARAC functions merely to clear both A_R and A_L.

3. ARAC READ SEQUENCE, INSTRUCTION 21, 23, 31, 33, 51, 53, or 71. - The execution of these instructions requires that an operand be obtained from the u-address and transmitted into X for subsequent insertion into A_R. If Q or A are referenced by the u-address, the ARAC Read sequences outlined below are carried out. If MD or MC are referenced by the u-address, ARAC functions merely to clear A_R and A_L.

a. Q REFERENCE. - The same operations carried out as for 41 uv, 54 uv, and 74 uv instructions: X is complemented, the transmission $Q' \rightarrow X'$ is achieved, and A_R and A_L are cleared.

b. A REFERENCE. - The ARAC Read Sequence for instructions 21 uv, 23 uv, 31 uv, 33 uv, 51 uv, and 71 uv does not suppress the clearing of A nor the transmission $A_R \rightarrow X$. The ARAC Read sequence for these instructions is carried out in exactly the same manner as that for the 27 uv instruction, except that both A_R and A_L are cleared after the transmission $A_R \rightarrow X$. The accumulator is thus left prepared for the re-insertion of the operand originally stored in A_R. These instructions, therefore, involve only a 36-bit operand.

c. MD or MC REFERENCES. - ARAC functions merely to clear A_R and A_L.

4. ARAC READ SEQUENCE, OTHER INSTRUCTIONS. - Other instructions than those listed above do not produce the INITIATE CLEAR A signal on MP 0. Except for the fact that A is not cleared, ARAC Read sequences for both Q and A References during other instructions are basically the same as those listed above for instructions 21, 23, 31, 33, 51, 53, and 71. ARAC does not clear A if MD or MC references are made by the u-address portion of any of these other instructions.

(b) ARAC WRITE SEQUENCES. - Not all instructions have a v-address portion which references a writing operation. All instructions which call for a writing operation, however, should specify a full 36-bit writing operation if they reference Q or A. When Q is referenced by the execution address of an instruction word, an ARAC Write Sequence for a Q reference is carried out, and if A is referenced by the execution address of an instruction word, one of two possible ARAC Write sequences for an A reference is executed depending on the instruction in program control.

1. ARAC WRITE SEQUENCE, ANY INSTRUCTION, Q REFERENCE. - If Q is referenced, SCT supplies ARAC, SCC, and the Fault Control with Q reference enables. SCC carries out the SCC Initiate Write Q sequence and issues an INITIATE WRITE Q signal to ARAC. The latter signal sets the Write A or Q flip-flop V80-30133 in ARAC to "1" and passes on to Q as a CLEAR Q signal. In ARAC, the next CONTROLLED CLOCK PULSE to occur clears the Write A or Q flip-flop, passes

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through gate V02-30133, and is issued to X as an X→Q signal and to PDC as an ARAC RESUME signal. The contents of X are thus written in Q. If the instruction's v-address references Q, this sequence is carried out regardless of the instruction being executed.

2. ARAC WRITE SEQUENCE, INSTRUCTIONS 11, 12, 13, 55, 73, or 76, A REFERENCE. - If A is referenced, SCT supplies ARAC, SCC, and the Fault Control with A reference enables. SCC carries out the SCC Initiate Write A sequence and issues an INITIATE WRITE A signal to ARAC. The latter signal passes through gate V02-30123 in ARAC, sets the Write A or Q flip-flop, passes through gate V07-30133 (enabled by the NOT 41, 54, or 74 circuit), and clears both A_R and A_L. In ARAC, the next CONTROLLED CLOCK PULSE to occur clears the Write A or Q flip-flop, passes through gate V03-30133 and is issued to ASC as an ADD X TO A signal and to SAR and MCT as a CLEAR SAR signal. Upon completion of the ASC Add X to A sequence, the quantity D(X) is held in A, and PDC is sent an ASC RESUME signal. An examination of the above instructions which use this ARAC Write sequence will indicate that the operand being written is generally not in A prior to the writing operation, and therefore, to store the operand in A, a writing operation must be carried out.

3. ARAC WRITE SEQUENCE, OTHER INSTRUCTIONS, A REFERENCE. - The other instructions which specify a writing operation each call for a transmission which stores (A_R) at the v execution address. The MP which produces the INITIATE WRITE (0-35) signal also produces in most cases an A_R→X signal. X then holds the 36-bit operand to be written by the time the internal storage reference is well under way. If MD, MC, or Q are referenced by the v-address portion of the instruction, an MDAC, MCAC, or ARAC Write (Q Reference) sequence, respectively, is carried out to transmit (X) to the referenced MD, MC, or Q location. However, if A is referenced, (X) is not re-inserted into A. The INITIATE WRITE A signal produced by SCC during instructions other than 11, 12, 13, 55, 73, or 76 merely passes through gate V03-30123 and is issued to PDC as an ARAC RESUME signal. Thus, the writing operation from X is by-passed, because A_R already holds the operand to be written.

h. MAGNETIC TAPE STORAGE SYSTEM. - The Magnetic Tape Storage System, MT, is the principal external storage system of the computer. MT is a binary, magnetic, non-volatile, relatively slow-access storage system of large capacity. Computer words are stored serially on the magnetic tape storage medium, two bits on each line and eighteen lines per word. Words are stored in 32-word groups called blocks. MT information is available from MT and can be recorded in MT only through the proper use of the four MT instructions: Advance Magnetic Tape (66jn-), Back Magnetic Tape (67jn-), Read Magnetic Tape (64jnv), and Write Magnetic Tape (65jnv). The value of "j" (0, 1, 2, 3) in these instructions specifies that the magnetic tape in one of the four separate storage units, 0 MT, 1 MT, 2 MT, or 3 MT, is to be involved in the MT operation. The value of "n" (where $0 \leq n \leq 2047$) specifies the number of blocks of data on the j-selected tape to be involved in the advancing, backing, reading, or writing operation. The value of "v" in the 64jnv and 65jnv instructions represents the starting MC address in the reading or writing operation. From one to 32 blocks can be written onto a selected tape from MC or read from a selected tape into MC in a single reference operation. In general, positioning operations precede reading or writing operations. A particular block or group of consecutive blocks to be written into or read from are located by moving the tape a specified number of

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blocks, in either the forward or reverse direction, from a known starting position. While the location of the desired blocks may require up to a maximum of a little over 5 minutes (the time required to scan an entire magnetic tape), the rate of transfer of words into or out of the blocks is rapid, taking place at approximately 222 words per second.

The MT system is composed of the following principal parts: four magnetic tape storage subsystems designated by jMT, each of which contains a Raytheon Magnetic Tape Handling Unit, designated MT Unit j, and associated locating and error detection circuitry; a pair of two-bit, flip-flop, buffer storage registers called the Magnetic Tape Input register (MTI) and the Magnetic Tape Output register (MTO), which are shared at separate times by all four jMT storage elements, and are used in storing information on the tape and reading information from the tape; and the Magnetic Tape Sequence Control (MTSC) which synchronizes MT reading and writing operations with the operation of the rest of the computer and executes the various subsequences which perform MT reading and writing operations.

(1) PRINCIPLES OF MAGNETIC TAPE STORAGE. - Information is stored in MT in binary form, as magnetized areas on the surface of magnetic tape. The magnetized areas represent "0's" or "1's" depending on their polarity. The return-to-zero method of recording is used in which the entire magnetic surface of the tape is first polarized in one direction to represent a "0", and then individual areas are given an opposite polarity where it is desired that a "1" be stored. In MT reading operations only "1's" are sensed; in MT writing operations, the area to be written on is first erased (made to store a "0") and then left in that condition or oppositely polarized, depending on whether a "0" or "1", respectively, is to be written.

For locating purposes, the magnetic tape can be thought of as being divided longitudinally into six parallel channels or tracks each approximately 0.025 inch wide, and transversely into lines spaced 100 to the inch. Each line can thus be regarded as containing six minute areas, called "cells", one in each track. These cells store MT data.

Certain cells of the tape may contain blemishes which cannot be magnetized to either polarity. Consequently, any information written into these "cells" is lost. Since the blemishes occur relatively infrequently, and since they rarely occupy more than one cell area, the loss of information due to them is practically eliminated by storing each bit of information in two non-adjacent cells of the same line. Accordingly, two pairs of non-adjacent cells in each line of tape are used to provide duplicate storage for two binary digits of data and the third pair of non-adjacent cells is used to store a timing or control bit. Eighteen lines can thus store a computer word as well as the control bits required to manipulate that word, two-bits at a time. Words are stored successively on the tape in 32-word groups called "data blocks". Data blocks contain 576 lines. Between each data block there is a blank space in which no data is stored.

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When a blank space on the tape is beneath the tape's magnetic head assembly no effect is produced. When the lines of a block pass under the head assembly, however, one of three basically different MT operations can be executed: positioning, reading, or writing. The particular operation carried out depends on

which of the following program instruction is in program control: Advance Magnetic Tape (66jn-), Back Magnetic Tape (67jn-), Read Magnetic Tape (64jnv), or Write Magnetic Tape (65jnv).

If either the 66jn- instruction or 67jn- instruction is in program control, a positioning operation is carried out. The value "j" (0, 1, 2, or 3) in these instructions specifies which of the four is to be positioned, and the value "n" specifies how many blocks that tape is to be moved in a forward or reverse direction from a known starting position. When the instruction sequence is executed, the value "j" is used to initiate the positioning operation in MT Unit "j", and the value "n" is inserted in the Block Counter associated with MT Unit "j". As the tape moves under the heads, the control bits stored on each line are read and LINE PULSE (LP's) are produced. Each LINE PULSE is sent to the selected MT Unit's Line Counter (j LK) and advances the Line Counter by one count. When 18 lines have been read, the Line Counter is cleared and a WORD PULSE (WP) is produced which advances the MT Unit's Word Counter (j WK) by one. When the Word Counter has been advanced to 32 it is cleared and a BLOCK PULSE (BP) is produced which subtracts 1 from the value "n" stored in a the Block Counter (j BK). When the count stored in the Block Counter is reduced to zero, tape movement stops. The tape is left positioned "n" blocks from the starting position so that part of the interblock space after the nth block is under the head assembly. If the 64jnv instruction is in program control, an MT reading operation is carried out; if a 65jnv instruction is in program control, a writing operation is carried out. In reading and writing operations the values of "j" and "n" are used the same as in the positioning operation, and the counting activities of the LINE, WORD, and BLOCK PULSES are the same. However, during reading and writing a Counter Pulse Control Circuit allows LINE PULSES and WORD PULSES to function also in the Magnetic Tape Sequence Control (MTSC), and to trigger various portions of the reading and writing operations. The Counter Pulse Control also puts the MT Unit's reading and writing circuits in communication with MTO (reading operation) or MTI (writing operation). Thus, as the selected tape moves, the lines, words and blocks are counted and the reading or writing is accomplished line-by-line until the desired number of blocks have been read or written.

During the reading operation, as each line of tape is read, the two data bits on each line of tape are transmitted to MTO, the transmission MTO$\rightarrow Q_{0-1}$ is achieved, and Q is shifted two places to the left. After 18 lines are thus read, the word assembled in Q is sent to the MC address specified by the v portion of the 65jnv instruction, the v-address is advanced by one, and Q is cleared. This process continues until all "n" blocks specified by the 64jnv instruction are read. Since the capacity of MC is 1024, up to 32 blocks may be read in any reading operation.

As soon as the signal is received which initiates an MT writing operation, a word is stored in Q from the v-address specified by 65jnv instruction, the v-address is advanced by one, Q is left-circularly shifted two places (since highest order bits are always written and read first), the transmission $Q_{0-1} \rightarrow$ MTI is achieved, and an ERASE BIAS is applied to the head assembly. When the first LINE PULSE is produced, (MTI) is written on the first line of the first block, Q is shifted two places to the left and the new (Q_{0-1}) is transmitted to MTI. The next sixteen LINE PULSES produce the same effect as the first LINE PULSE. When the 18th LINE PULSE is produced, a WORD PULSE is generated. The 18th LINE PULSE effects the writing of the 18th pair of bits of the word stored in Q.

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The WORD PULSE effects the clearing of Q, the transmission to Q of the word stored at MC address v + 1, the subsequent shifting of Q two places to the left and the insertion of (Q_{0-1}) into MTI. The 19th LINE PULSE starts the writing operation of the new word. The above process continues until all "n" blocks of words specified by the 65jnv instruction have been written.

(2) MT STORAGE SUBSYSTEMS. - Each of the four jMT storage subsystems has the following principal parts: a Magnetic Tape Unit (designated MT Unit j) which contains a tape drive mechanism with manual as well as automatic controls, a magnetic head assembly, and a magnetic recording tape; a Locating Circuit consisting of a set of three counters (Line Counter, Word Counter, and Block Counter) and a Counter Pulse Control (jKPC flip-flop and associated gates); a Zero Move Circuit which consists basically of a pair of gates used at the start of MT operations to prevent tape movement when none is specified; and an Error Detection Circuit, consisting of an Error flip-flop and associated circuitry, which prevents further MT operation if an error is detected. The purpose of each of these component parts is discussed below.

(a) MAGNETIC TAPE UNITS. - Each Magnetic Tape Unit contains a tape drive mechanism, a six-channel magnetic head assembly, and 1200 feet of one-half inch magnetic recording tape.

The tape-drive mechanism consists of a continuously rotating tape-drive motor connected to a drive capstan by a clutch and brake assembly, a tape-slack absorber mechanism, and two reel motors which operate the take-up and rewind tape reels.

The magnetic head assembly consists of six read-write heads so arranged to permit writing or reading operations to be performed simultaneously in six channels or "tracks" on the magnetic tape.

The magnetic tape is wound onto the tape-drive mechanism so that as one reel unwinds tape, the other winds it, and vice versa. In passing from one reel to the other, the tape passes across the magnetic head assembly and through the slack absorber mechanism.

A selector switch in the MT Unit permits the motion of the tape to be controlled either manually or automatically. By setting this switch to the F, R, or S position the maintenance personnel may drive the tape forward (F) or reverse (R), or stop the tape (S). If this switch is set to position A, the motion of the tape is controlled automatically by the signals ADVANCE, BACK, and STOP produced in the control circuitry associated with the MT Unit. The ADVANCE signal energizes a "forward" clutch and a "forward" brake which cause the capstan to rotate counter-clockwise so that the tape is accelerated from 0 to 45.5 inches per second in the forward direction. The BACK signal causes the capstan to rotate clockwise so that the tape is accelerated from 0 to 45.5 inches per second in the reverse direction. At a speed of 45.5 inches per second, approximately 222 36-bit words can be written on or read from the tape. The STOP signal energizes "forward" and "reverse" brakes so that the capstan stops rotating.

The slack-absorber mechanism is an assembly of fixed and moveable spools

that holds a long loop or "reserve" of tape. This "reserve" of tape serves as a shock absorber during starting and stopping when the movement of the drive capstan produces tape acceleration that must overcome the inertia of the take-up and rewind reels. During acceleration, the movement of the slack-absorber carriage mechanism operates a servo mechanism that produces the error signal used in operating the tape reel motors.

The tape reel motors are controlled by the error signal from the servo system so that the reserve of tape contained in the slack-absorber mechanism is maintained at the proper length. Any displacement of the slack-absorber carriage, detected by the servo input, operates the reel drive motors so that tape is wound on or off of the reels until the slack-absorber carriage is returned to its proper position.

Only inspected and properly prepared magnetic tapes can be used in the MT units. The method of inspecting magnetic tapes is discussed in Volume 3, Section 5. A properly prepared tape has the following spacings and arrangement of blocks:

a. Leader - blank space, at least 10 feet long;

b. First Error Block - a space in which 580 pairs of control bits (used to produce LP's) are stored.

c. Forward Starting Position - a rather long blank space between the first Error Block and first Data Block.

d. Storage Area, subdivided as follows:

1st Data Block
Interblock Space
2nd data Block
Interblock Space
3rd Data Block

(etc.)

Interblock Space
2048th Data Block

Each Data Block contains 576 lines on each of which are stored a pair of control bits used to produce LP's.
Each Interblock Space is a blank space about 3/4" long.

e. Reverse Starting Position - a rather long blank space between the last Data Block and the second Error Block;

f. Second Error Block - a space in which 580 pairs of control bits (used to produce LP's) are stored;

g. Trailer - blank space, at least 10 feet long.

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The method of properly preparing a magnetic tape is presented in Volume 1, Section 3. The manner in which tape is threaded in each MT Unit and the way in which tape in an MT Unit is properly positioned for use under automatic control by the computer are described in Volume 1, Section 2.

It should be noted that each magnetic tape has 2048 Data Blocks. Each tape can, therefore, store 65, 536 36-bit words, and the entire capacity of MT is 262,144 36-bit words.

(b) LOCATING CIRCUIT. - Each storage subsystem (jMT) has a locating circuit associated with its tape handling unit, MT Unit j. Each locating circuit has two basic parts: a set of three counters (Line Counter (jLK), Word Counter (jWk), and Block Counter (jBK), and a Counter Pulse Control Circuit.

The three counters are connected in series and their collective function is to count the blocks which pass under the head assembly as the tape moves, and to stop tape movement when the specified number of blocks have passed. The Line Counter, a modulo 18 additive counter composed of five flip-flops, counts the LP's produced as the control bits stored on each line of tape are read. Each time the Line Counter reaches the count of 18 (LK = 18), it generates an end-carry pulse called a WORD PULSE (WP). The WP resets the Line Counter to zero and advances the Word Counter by one. The Word Counter, a modulo 32 additive counter composed of five flip-flops, generates an end-carry pulse, called a BLOCK PULSE (BP), each time it reaches the count of 32 (WK = 32). The BP resets the Word Counter to zero and subtracts a single count from the Block Counter. The Block Counter, a modulo 2048 subtractive counter composed of 12 flip-flops, is initially set to the number of blocks, n, which the tape must be moved. The first BP which enters the Block Counter after the block count has been reduced to zero (BK = 0) sets the BK to $2^{12} - 1$ and leaves the Block Counter as a STOP pulse.

The Counter Pulse Control Circuit in each jMT is composed of a Counter Pulse Control flip-flop (jKPC) and its associated control gates. During positioning operations (advancing or backing the tape) the jKPC flip-flop is set to "0". In such operations, the LP's, PW's, and BP's produced as the tape in MT Unit j moves are used simply for counting purposes to effect the proper positioning. During reading and writing operations, however, the jKPC flip-flop is set to "1" and its "1" output is used to enable a set of control gates which pass LP's, WP's, and STOP signals to MTSC. During the writing operation the "1" output enable of jKPC is also combined in a coincidence circuit with the "1" output enable of the MTSC Write flip-flop to create the ERASE BIAS used in the writing operation and used to gate the WRITE signal from MTSC which triggers the transmission of the "1's" stored in MT I to the head assembly's writing circuits.

(c) ZERO MOVE CIRCUIT - The Zero Move Circuit of each jMT storage subsystem consists of two gates in the BACK and ADVANCE signal lines that are enabled only when $jBK_{11} = 0$. This circuit prevents the tape from being backed or advanced when the number of blocks, "n", the tape is to be backed or advanced is equal to zero.

As explained above, each BK is a subtractive counter of modulo 2048. Stages bk_0 through bk_{10} are used to store values of n from 0 to 2047. Stage BK_{11} is always zero (and therefore the Advance and Back gates of the Zero-Move Circuit

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are enabled) unless the value of n originally inserted into BK equals zero. When advancing or backing of the tape is called for, a BACK BK signal is always produced prior to the actual start of tape movement. If the value "n" stored in BK is 0, the BACK BK signal sets BK to all "1's". The resulting END BORROW from BK produces a STOP signal which stops the MT unit if it is not already stopped. At this time, because BK_{11} is set to "1", the ADVANCE or BACK signal which normally initiates tape movement is blocked by the disabled Zero Move gates. The MT Unit therefore remains stopped.

(d) ERROR DETECTION CIRCUIT. - The Error Detection Circuit in each jMT storage element consists of a 500 microsecond shaper, a gate, and the j Error flip-flop. In NORMAL operation this circuit stops tape drive, and registers a B-Fault called MISSING LP (hence stops the computer) if more or less than 576 LP's are produced when a block on the tape passes under the head assembly.

A BP is produced simultaneously with each 576th LP. If the proper number of LP's are produced per block, a BP is generated simultaneously with the last LP read from each block. If more than 576 LP's are produced from a block, a BP is produced before the last line of the block passes under the head assembly. If less than 576 LP's are produced from a block, a BP is not produced until one or more lines of the next block pass under the head assembly. The Error Detection Circuit functions, each time a BP is produced, to check that the proper number of LP's are produced from each block.

Besides being used to subtract one from the Block Counter, each BP is shaped and used momentarily to enable a gate in the "1" input circuit of the j Error flip-flop. If exactly 576 LP's were produced from a tape block, no LP's will be produced during the interblock period when the 3/4-inch blank space passes under the head assembly. The input gate of the j Error flip-flop is enabled for approximately 500 microseconds, but its enable is dropped by the time an LP is produced from the first line of the next block.

If less than 576 LP's are produced from a tape block, one or more lines of the next block are read before a BP is produced. The first LP to be produced after the gate in the "1" input circuit of the j Error flip-flop is enabled by the shaped BP will pass through that gate, stop tape drive, and set the j Error flip-flop to "1". The "1" output of the j Error flip-flop energizes the Missing Line Pulse relay, K30076, and a B Fault is registered which stops the computer.

Similar detection occurs if more than 576 LP's are produced by a tape block. The BP produced with the 576th LP enables the gate in the "1" input circuit of the j Error flip-flop. The first LP to occur after the error flip-flop gate is enabled stops tape drive and registers a B Fault, which stops the computer.

A pair of Error Blocks each containing 580 dual control bits is intentionally stored on each tape, one preceding the first Data Block and one following the last Data Block. The purpose of these Error Blocks is to stop tape drive if an attempt is made to run the tape too far in either the forward or reverse direction. When an Error Block is read, the error detection is the same as that described above for cases where too many LP's are produced by a tape block.

Before another storage reference to jMT can be made and operation resumed, the MT unit's counters must be manually cleared and the tape re-positioned past

the Error Block in the direction of the Data Blocks. The next MT operation must then call for a movement of tape in a direction opposite to that causing the Error Block to be read.

(3) MAGNETIC TAPE INPUT REGISTER. - The Magnetic Tape Input Register (MTI) is a two-stage flip-flop register which is used during MT writing operations. MTI functions to temporarily store the successive two-bit portions of words that are to be written on the magnetic tape. For every 36-bit computer word stored in MT the following events involving MTI occur 18 times: MTI is cleared; Q is shifted two places to the left; the "1's" stored in Q_0 and Q_1 are transmitted to MTI_0 and MTI_1; respectively; and the MTI "1" outputs, together with a WRITE signal from MTSC, are applied to the writing circuits of the proper MT Unit j. If "1's" are stored in MTI_0 and MTI_1 they are appropriately recorded on the tape. MTI is thus a buffer storage register between Q and the writing circuits of the tape units. Exact details concerning the transmissions in and out of MTI are given below under MT Writing Sequence.

(4) MAGNETIC TAPE OUTPUT REGISTER. - The Magnetic Tape Output Register (MTO) is a two stage flip-flop register which is used during MT reading operations. MTO functions to temporarily store each two-bit portion read from lines on the magnetic tape. For every 36-bit computer word read from the tape the following events involving MTO occur 18 times: MTO is cleared; the "1's" sensed by the selected MT Unit's reading from the two data bits stored on a line of the tape are sent to MTO the transmission $MTO_{0-1} \rightarrow Q_{0-1}$ is carried out; and Q is shifted two places to the left. MTO is thus the buffer storage register between the reading circuits of the tape units and the Q-Register. Exact details concerning the transmissions in and out of MTO are given below under the Reading Sequence.

(5) MAGNETIC TAPE SEQUENCE CONTROL. - The Magnetic Tape Sequence Control (MTSC) functions primarily in the execution of MT Reading and Writing sequences. Since these sequences produce signals which direct the activities of elements external to the MT system (as Q, VAK, etc.), MTSC also functions to coordinate MT activity with that of the central computer. Upon receipt of an INITIATE READ j MT signal from CTC, MTSC is prepared for a reading operation; upon receipt of an INITIATE WRITE jMT signal from CTC, MTSC is prepared for a writing operation. During both of these operations each LP produced is set to MTSC to trigger a short subsequence which assembles two bits of data from the tape in Q (during reading) or writes two bits of data from Q onto a line of tape (during writing). As every 18th LP is produced, a WP is generated. Both are sent to MTSC; the LP effects the disposition of the last two-bit portion of a 36-bit word and the WP prepares MTSC so that the word assembled in Q is set to MC and Q is cleared (during reading), or so that the word just written from Q is cleared out and a new word assembled in Q (during writing). When all "n" blocks to be read or written into have passed under the head assembly, tape drive stops, and the jMT RESUME signal produced clears the reading or writing condition out of MTSC.

The principal components of MTSC are the following: the Synchronizing Unit (two flip-flops, SUI and SUII, two gates, and a 40 microsecond delay circuit) which effects the switchover from the LP timing pulses which control MT to CONTROLLED CLOCK PULSES; the Read and Write flip-flops which are set, respectively, by INITIATE READ jMT and INITIATE WRITE jMT signals from CTC, to allow their corresponding MT operation to be carried out; the Recycle Read I, Recycle Read II, and Recycle Write flip-flops, which function to issue signals which

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transmit MT information assembled in Q into MC, or issue signals which transmit successive words into Q after each word has been written; and the MTSC flip-flops, which function in the production of signals which shift Q, control the transmissions between MTO and Q_{0-1}, MTI and Q_{0-1}, and control the transmission between X and Q. In the following subparagraph, the specific function of each of the above mentioned MTSC components is discussed in detail.

(6) MT SEQUENCES. - There are four sequences of MT operations, as follows: the MT Reading Sequence, the MT Writing Sequence, the MT Advance Sequence, and the MT Back Sequence. These sequences are performed in the execution of the following four corresponding computer instructions: Read Magnetic Tape (64 jnv), Write Magnetic Tape (65 jnv), Advance Magnetic Tape (66 jn-) and Back Magnetic Tape (67 jn-).

During the Read Magnetic Tape instruction (64 jnv), an INITIATE READ j MT signal from CTC initiates an MT Reading Sequence which transmits the data from n consecutive blocks on the tape in MT Unit j into consecutive addresses in MC, beginning with the MC address v. Reading is performed with the tape travelling in the forward direction. During the Write Magnetic Tape instruction (67 jnv), an INITIATE WRITE j MT signal from CTC initiates an MT Writing Sequence which transmits the contents of 32 n consecutive MC addresses, beginning with MC address v, onto n blocks on the tape in MT Unit j. During writing, the tape moves in the forward direction. During the Advance Tape instruction (66 jn-), an INITIATE ADVANCE j MT signal initiates an MT Advance Sequence which advances the tape in MT Unit j by n blocks. During the Back Tape instruction (67 jn-), an INITIATE BACK j MT signal initiates an MT Back Sequence which backs the tape in MT unit j by n blocks.

The following sub-paragraphs discuss each of the four sequences of operations of the Magnetic Tape Storage System. For simplicity, only the details concerning MT Unit 0 are presented. Exactly the same operations would be performed, however, if any of the other units were referenced. Each of the MT sequences of operations is shown in tabular form in Appendix B, Pages B-78 through B-80, Volume 2.

(a) MT READING SEQUENCE. - By the time an INITIATE READ j MT signal is received from CTC, Q and the 0 counters (0 LK, 0 WK, 0 BK) have been cleared and the initial value of n has been stored in 0 BK. The INITIATE READ 0 MT signal then backs 0 BK by one count, sets the 0 KPC and Read flip-flops, V82-70162 and V83-70243 respectively, to "1", clears the Recycle Read I flip-flop, V81-70243, and after a 5 millisecond delay, probes gate V02-70171.

If the "n" stored in 0 BK does not equal zero, advancing of the tape in MT Unit 0 is initiated. Approximately 14 milliseconds after the INITIATE READ j MT signal is received from CTC, the first LP is generated. Successive LP's are then produced at a rate of approximately 4.5 kc. Each LP advances 0 LK, samples the Error Detection gate V13-70151, and passes through gate V05-70162 which is enabled by the "1" output of the 0 KPC flip-flop. The gated LP clears MTO_0 and MTO_1, and enters the 40 microsecond delay circuit, V02-70232. Approximately 15 microseconds after the LP is produced, the two bits of data stored on the first line of the tape are transmitted to MTO. (Actually only "1's" are read from the tape and passed by gates V09-70142 and V04-70141 to the "1" input signal lines of MTO_1 and MTO_0, respectively.) The 40 microsecond delay circuit

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prevents initiation of each reading subsequence until the reading gates V09-70142 and V04-70141 have transmitted the data bits to MTO. MTO is thus loaded by the time the gated LP is issued by V80-70232 and the gated LP sets the SU I flip-flop, V80-70232 to "1". When SU I is set to "1" its output is combined with the "0" output of the SU II flip-flop, V81-70232, and gate V03-70232 is enabled. The next CONTROLLED CLOCK PULSE to occur sets the SU II flip-flop to "1", disables gate V03-70232 and enables gate V04-70232. The next CONTROLLED CLOCK PULSE passes through gate V04-70232 as a SYNCHRONIZED CLOCK PULSE which clears both SU I and SU II to "0" and samples gates V10-70242 and V05-70232 in the "1" output circuits, respectively, of the Read and Write flip-flops. Gate V10-70242 passes the SYNCHRONIZED CLOCK PULSE and initiates a reading subsequence involving the MTSC-2, MTSC-3, and MTSC-4 flip-flops (V80-70243, V80-70232, and V83-70233, respectively). The reading subsequence for the first 17 LP's merely clears X, shifts Q left two places, inserts (MTO) into Q_{0-1}, and clears MTO. When the 18th 0 LP is produced, a 0 WP is generated simultaneously, signifying that the last two-bit portion of a word is about to be read from the tape. The 0 WP advances 0 WK, clears 0 LK, passes through gate V17-70164, sets the Recycle Read I flip-flop V81-70243 to "1", and clears the Recycle Write flip-flop, V80-70242. The 18th LP produces the same effect as the other LP's, and completes the assembly of a 36-bit word in Q. During every 18th reading subsequence, however, gate V04-70243 is enabled by the "1" output of the Recycle Read I flip-flop. When sampled by the pulse,which sends the last two-bit portion of the word being read from MTO to Q, gate V04-70243 issues a signal which complements X, achieves the transmission VAK → SAR, advances VAK, clears the Recycle Read I flip-flop and sets the Recycle Read II flip-flop. The next CONTROLLED CLOCK PULSE passes through gate V06-70233, clears the Recycle Read II flip-flop, achieves the transmission Q'→X', and produces an INITIATE WRITE signal which ultimately stores the word in MC. In exactly this same manner, successive words are read from the tape, assembled in Q, and transmitted to MC. At the end of each tape block (32 words) a 0 BP is produced. Each 0 BP clears 0 WK and backs 0 BK by one count. When 0 BK has backed to zero, n-1 blocks have been read. When n blocks have been read, the last 0 BP produces a STOP pulse. After a 2 millisecond delay, this STOP pulse stops tape drive in MTU 0; after a 10 millisecond delay, it passes through gate V06-70162, clears the Read, Write and 0 KPC flip-flops, and is transmitted to PDC as a 0 MT RESUME signal.

(b) MT WRITING SEQUENCE. - By the time an INITIATE WRITE 0 MT signal is received from CTC, the MT unit 0 counters have been cleared and the initial value of "n" has been stored in 0 BK. The INITIATE WRITE j MT signal then backs 0 BK by one count, sets the 0 KPC, Write, Recycle Write, and MTSC-1 flip-flops to "1", and, after a 5 millisecond delay, probes gate V02-70171. The INITIATE WRITE signal is also used to clear Q, transmit (VAK) to SAR, advance VAK, and produce an INITIATE READ signal which reads the contents of MC address v into X. Meanwhile the "1" outputs of the 0 KPC and Write flip-flops are combined in an AND circuit and an ERASE BIAS supplied for the head assembly in MT Unit 0. Also, if the "n" stored in 0 BK does not equal zero, advancing of the tape in MT Unit 0 is initiated.

The first CONTROLLED CLOCK PULSE to be produced, after the reading operation from MC to X is completed, passes through gate V03-70233 (enabled by "1" output of MTSC-1), clears X, transmits (X) to Q, clears MTSC-1 and sets MTSC-2. The next CONTROLLED CLOCK PULSE to appear thereafter will pass through gate V03-70243, clear MTSC-2, shift Q left one place, and set MTSC-3. The first

CONTROLLED CLOCK PULSE to appear after gate V06-70232 has been enabled by MTSC-3 will shift Q left another position, clear MTSC-3, and set MTSC-4. When gate V07-70233 has been enabled by MTSC-4 the next CONTROLLED CLOCK PULSE to appear will pass through gates V07-70233 and V08-70242, clear MTSC-4 and effect the $Q_{0-1} \rightarrow$ MTI transmission.

Approximately 14 milliseconds after the signal INITIATE WRITE j MT is received from CTC, the first LP is generated. Each 0 LP advances 0 LK, and passes through gate V05-70162 to MTSC. In MTSC, each 0 LP enters a delay circuit and passes through gate V04-70233, producing a WRITE signal. The WRITE signal is applied to AND circuits in the "1" outputs of MTI_0 and MTI_1. If either or both MTI_0 and MTI_1 store a "1" the writing circuits in MT Unit 0 appropriately store a "1" on the tape. If neither MTI_0 or MTI_1 stores a "1", the writing circuits do not receive an input. However, a "0" is effectively written since the ERASE BIAS, which is applied to the tape prior writing, removes previously stored data. A 40-microsecond delay circuit prevents the clearing of MTI until the 18-microsecond WRITE signal has effected the MTI→MT Unit 0 transmission. After the delay period has elapsed, 0 LP operates the SU flip-flops as described above under MT Reading Sequence. The resulting SYNCHRONIZED CLOCK PULSE initiates a writing subsequence involving the Recycle Write flip-flop and all four MTSC flip-flops. This subsequence transmits (X) to Q, clears X, shifts Q left two places, and transmits (Q_{0-1}) to MTI. (Since at this point X contains all "0's", the X→Q transmission is meaningless.) The writing subsequence for each of the next 16 0 LP's effects the writing of the contents of MTI onto a line on the tape, shifts Q two places to the left, and transmits Q_{0-1} to MTI. (X is also cleared, and the X→Q signal produced, but these have no effect during this time.) When the 18th 0 LP is produced, a 0 WP is generated, signifying that the last two-bit portion of the word stored in Q is about to be written on the tape. The 0 WP signal advances 0 WK, clears 0 LK, passes through gate V17-70164, clears the Recycle Write flip-flop, and sets the Recycle Read I flip-flop. The writing subsequence produced by the 18th 0 LP writes the final two-bit portion of the word on the tape, resets the Recycle Write flip-flop to "1", sets MTSC-1 to "1", and issues signals which clear Q, transmits (VAK) to SAR, advances VAK and produces an INITIATE READ MT sequence which inserts the contents of address v + 1 into X. After the reading of the contents of V+1 to X, the new word in X is processed by a Sequence similar to the one described above. When n blocks have been completed, the last 0 BP produces a STOP pulse which, after a 10 millisecond delay, stops MT Unit 0, clears the 0 KPC, Read, and Write flip-flops, and produces 0 MT RESUME.

(c) MT ADVANCE SEQUENCE. - When an INITIATE ADVANCE 0 MT signal is received, the value "n" stored in 0 BK is backed by one count, and the 0 KPC flip-flop is cleared. Providing $n \neq 0$, an ADVANCE signal is also produced which starts the tape in MT Unit 0 moving in the forward direction. Each 0 LP read from the tape operates the MT Unit 0 counters. When 0 BK has been backed to zero, the tape has been advanced by n-1 blocks. After the next block has passed beneath the reading head, the last 0 BP produces a STOP signal that stops MT Unit 0 and sends a 0 MT RESUME signal to PDC.

(d) MT BACK SEQUENCE - The INITIATE BACK 0 MT command produces the same effect as the INITIATE ADVANCE 0 MT command except that a BACK (rather than an ADVANCE) signal is produced which starts the tape in MT Unit 0 moving in the reverse direction. Subsequent operations are similar to operations described above for the 0 MT Advance Sequence.

7. ARITHMETIC SECTION

a. GENERAL. - The Arithmetic Section is composed of the following principle parts: the X-register (X); the Q-register (Q); the Accumulator (A); the Shift Counter (SK); the Shift Count Translator (SKT); and the Arithmetic Sequence Control (ASC).

Although the X-register, the Q-register, and the Accumulator are generally referred to as "arithmetic registers" because of their functions during arithmetic operations, each of these registers is used for a multitude of purposes, not all associated with arithmetic operations. These auxilliary uses are discussed briefly in the subparagraphs on X, Q, and A.

The Arithmetic Section uses special procedures derived from the fundamental processes of ones complement binary arithmetic to perform all the arithmetic and logical operations involved in the execution of the ERA 1103 Computer System's repertoire of instructions. Fundamentally, the Arithmetic Section executes five basically different unit operations, as follows: addition, in which a number in X is added to a number in A; shifting, in which numbers in A or Q or both are appropriately shifted one place to the left, with the bit in highest order stage being transferred to the lowest-order stage (sometimes this is accomplished to multiply a number in A or Q (by two); complementing of X, in which a number stored in X is multiplied by minus one; subtracting of one from A, in which a signal is generated which reduces the number held in A by one; and bit-by-bit multiplication, in which corresponding bits of X and Q are multiplied together and the bit-by-bit product stored in X.

These unit operations are employed separately to form an arithmetic or logical sequence, or they are integrated in various combinations with one another to form more complex sequences of operations. Separately and in combinations, they are used to form eleven distinct logical and arithmetic sequences, each initiated by a signal from the Command Timing Circuits (CTC) and carried out by one of the eleven sequence generating circuits in ASC. Each CTC signal which initiates a logical or arithmetic sequence of operations also stops the Main Pulse Distributor (MPD). CONTROLLED CLOCK PULSES then time the initiated sequence in the appropriate ASC sequence generating circuit. Upon completion of the logical or arithmetic operation, the sequence generating circuit issues an ASC RESUME signal which allows MPD to advance.

b. X-REGISTER. The X-Register, or X, is so-called because of its function as the central exchange register of the computer. It is a 36-stage flip-flop register which can be complemented. As an "exchange register" X handles nearly all internal transmissions of words between various sections of the computer. As an "arithmetic register" X holds the addend, subtrahend, multiplicand, and divisor during arithmetic operations. The X-register is shown on the Block Diagram, Arithmetic Registers, in Envelope #1 of Volume 7.

(1) BASIC PROPERTIES OF X. - The storage element of each of the 36 stages of X is the standard flip-flop. Each flip-flop has gate and manually controlled input circuits to its "0" and "1" sides, and each flip-flop supplies output enables for several gates in its "0" and "1" output circuits.

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Besides the "0" and "1" inputs to each stage of X, a trigger input is provided for each stage. When the signal COMPLEMENT X is sent to X, this signal is applied to both the "0" and "1" input of each stage of X. The effect is to reverse the state of each flip-flop in X regardless of what each flip-flop previously stored. Of the three arithmetic registers, only X can be complemented.

(a) TRANSMISSIONS TO X. - For transmissions to X, except for transmissions from Q, X is prepared for the receipt of an operand by the signal CLEAR X which clears each flip-flop in X to "0". The operand is then inserted into X by an internal storage reference (reading) operation in which "1's" are transmitted from the referenced storage location into X. For transmissions to X from Q, X is prepared for the receipt of an operand by the signals CLEAR X and COMPLEMENT X which, in turn, clear X to all "0's" and then set X to all "1's". When the transmission $Q^0 \rightarrow X^0$ occurs, "0's" stored in Q are sent to X, and appropriate stages of X are changed from "1" to "0". This method of transmission from Q to X is the opposite of the usual method of clearing a register and then transmitting "1's". This seemingly unorthodox method ($Q^0 \rightarrow X^0$) is used in place of $Q \rightarrow X$ for component economy; i.e., the $Q^0 \rightarrow X^0$ signal is also used to form in X the bit-by-bit product of X and Q.

The X-register receives operands one or more times during each instruction as part of the execution of the instruction; since X is always cleared on MP 0 a number left in X as a result of one instruction is not available from X during the next instruction.

The "0" and "1" outputs of stage X_{35} are used by various circuits in ASC to determine the specific steps executed in logical and arithmetic sequences.

(b) COMPLEMENT X - The basic unit operation of complementing X is accomplished when the signal COMPLEMENT X is applied as a trigger input to each flip-flop in X. The COMPLEMENT X signal reverses the state of each flip-flop regardless of what it previously stored. Since one's complement notation is employed in the ERA 1103, the effect is to multiply the contents of X by minus one.

(2) OPERATION AS THE CENTRAL EXCHANGE REGISTER. - As a central exchange register, X is involved in almost all internal transmissions of data. With some circuits of the computer, X can communicate in two-way type of transmissions (such as X→MD and MD→X), while in transmissions involving other circuits of the computer the information flow is in one direction only (such as X→PCR or SAR→X). Some transmissions involve 36 bits; others involve a fewer number of bits. In some cases "0's" are transmitted; in other cases "1's" are transmitted. Although only "0's" or "1's" are transmitted, provision is made that the register receiving the information is properly cleared or set to all "1's" or the circuit design is such that the transmission is correctly achieved. The following listing summarizes the various transmissions in which X is involved as the central exchange register:

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TWO-WAY TRANSMISSIONS	ONE-WAY TRANSMISSIONS
X↔MD	X→PCR
X↔MC	X→HPR
X↔A	X→TWR
X↔Q	X→jBK (Block Counter)
X↔IOA	SAR→X
X↔IOB	

Deatils concerning the signals which trigger each of the above transmissions, the number of bits involved in each transmission, and the kind of bits("0's" or "1's") transmitted are presented in those subparagraphs which describe the circuit with which X communicates. For example, the transmissions X→MD and MD→X are discussed in the subparagraph which described the MD system.

(3) OPERATION AS AN ARITHMETIC REGISTER. - As an arithmetic register X holds the addend, subtrahend, multiplicand and divisor in the corresponding arithmetic operations. In logical addition and logical multiplication X holds the logical addend and the logical multiplicand.

c. Q-REGISTER. - The Q-Register, or Q, is so-called because it holds the quotient during division. It is a 36-stage flip-flop register which can be left circularly shifted. As a "storage register", " is addressed and provides a single rapid-access storage location for one 36-bit computer word. Its address is 1---- (only the first octal digit is of significance). As an "assembly register", Q is capable of receiving two bits at a time and shifting these to the left to assemble a 36-bit word as is done in the MT Reading operation. During the MT Writing operation, 36-bit words are disassembled by a similar operation in Q. As an "arithmetic register", Q performs shifting operations and holds the multiplier, quotient, and logical multiplier during arithmetic operations. The Q-register is shown on the Block Diagram, Arithmetic Registers, in Envelope #1 of Volume 7.

(1) BASIC PROPERTIES OF Q. - The Q-register has 36 stages each consisting of a standard flip-flop and its associated input and output circuits. Interconnections between the stages provide Q with left circular shift properties. The "0" and "1" input circuit of each of the 35 left-most stages include gates enabled by the "0" and "1" circuits of the stage immediately to the right, and the input circuits of the right-most stage, Q_0, includes gates enabled by the outputs of Q_{35}.

In addition to the inputs mentioned above for the shifting operation, Q has inputs for transmitting data to and from Q and inputs for use during special arithmetic sequences.

(a) TRANSMISSIONS TO AND FROM Q. - For transmitting the contents of X to Q, Q is first cleared by a CLEAR Q signal, then the receipt of the X→Q signal transmits "1" inputs to all stages of Q which correspond to stages in X storing a "1". During the divide operation, the receipt of SET Q_0 to 1 from Arithmetic Sequence Control sets the Q_0 flip-flop to "1". During MT Reading operations, "1's" read from magnetic tape are stored in the Magnetic Tape

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Output Register; when the signal MTO→Q_{0-1} is produced, the "1's" stored in the two-stage MTO will be transmitted to Q_0 and Q_1.

Outputs of Q are used for transmitting data to X for special circuits of the Arithmetic Sequence Control and for transmission of data to the Magnetic Tape Storage System. For transmitting the contents of Q to X, X is set to contain all ones, then the receipt of $Q^0 \rightarrow X^0$ causes those stages in X, which correspond to stages in Q storing a "0", to be cleared to "0". Stages Q_0, Q_1 and Q_{35} each supply both a "0" and a "1" output enable for the Arithmetic Sequence Control. The "1" output enables from stages Q_0 and Q_1 are used to enable gates in the "1" input circuits of MTO.

(b) SHIFTING. - The basic unit operation of shifting can be performed in Q. Numbers stored in Q can be left circularly-shifted one place by the signal QL 1 (shift Q left one place). This signal causes the bits in stages Q_0 through Q_{34} to be shifted to the left by one place, and the contents of Q_{35} to be shifted to Q_0.

(c) BIT-BY-BIT-MULTIPLICATION. - The signal $Q^0 \rightarrow X^0$ is employed for the basic operation of bit-by-bit multiplication. A number is inserted into X, and the $Q^0 \rightarrow X^0$ signal is produced. Where "0's" are stored in Q, the corresponding stage of X is cleared to "0". Where "1's" are stored in Q, the corresponding stage of X is left undisturbed. The effect for each set of corresponding stages is that a "0" in Q times either a "0" or "1" in X, leaves a "0" stored in X, and that a "1" in Q, times either a "0" or "1" stored in X, leaves X undisturbed.

(2) OPERATION AS A STORAGE REGISTER. - As a storage register, Q is the addressed storage location 1---- (only the first octal digit is significant). Q can provide rapid access storage for any 36-bit computer word. As a storage register, Q communicates only with X.

Information is transmitted from X to Q by clearing Q (setting each of its flip-flops to "0") and then sampling gates in the "1" output circuits of X ("1" input circuits of Q) with the signal X→Q. Those gates which are enabled by "1" outputs from X will transmit signals to the "1" input signal lines of the corresponding stages in Q. The word stored in X is thus transmitted to Q by changing "0's" to "1's" in the appropriate stages of Q.

Information is transmitted out of Q to X in storage references by first clearing X, then complementing X (setting each flip-flop to "1"), and then sampling the gates in the "0" output circuits of Q ("0" input circuits of X) with the signal, $Q^0 \rightarrow X^0$. Those gates enabled by "0" outputs from Q will transmit signals to the "0" input signal line of the corresponding stage in X. The word stored in Q is thus transmitted to X by changing "1's" to "0's" in the appropriate stages of X.

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(3) OPERATION AS AN ASSEMBLY REGISTER. - During MT Reading operations, Q assembles 36-bit words, two bits at a time. As each pair of bits is read from a line on the magnetic tape, they are stored in the Magnetic Tape Output Register, MTO. When the signal MTO Q_{0-1} is produced it samples the gates in the "1" output circuits of MTO. The gate or gates enabled by "1" outputs from MTO_0 and MTO_1 transmit signals to the corresponding "1" input signal lines of Q_0 and Q_1. Q is then shifted two places to the left. This process is re-

peated 18 times until the complete 36-bit word is present in Q.

During MT writing operations, a 36-bit word is stored in Q from X. Q is then shifted two places to the left, putting the two most significant bits of the word initially stored in Q in Q_1 and Q_0. Gates in the "1" output circuits of Q_1 and Q_0 ("1" input circuits of MTO_0 and MTO_1) are sampled by the $Q_{0-1}\rightarrow$ MTI signal. The gate or gates which are enabled by "1" outputs from Q_0 and Q_1 transmit signals to "1" input signal lines of MTI_0 and MTI_1, respectively. The two bits in MTI are then written on a line of tape, and Q is shifted left two places. The process continues until the entire 36-bit word in Q has been written on the magnetic tape. A new word is then inserted into Q from X, and the disassembly operation described above is repeated.

(4) OPERATION AS AN ARITHMETIC REGISTER. - Q holds the multiplier during multiplication and stores the quotient while it is being formed during division. In all logical operations except the Controlled Complement instruction, (Q) is the controlling factor of the operation.

d. ACCUMULATOR. - The Accumulator, or A, is so-called because the results of many arithmetic operations are formed by "accumulation" in A. It is a 72-stage flip-flop subtractive accumulator-register with shifting properties. It has two halves, termed A_R (A-right) and A_L (A-left). Only the 36-stage A_R portion communicates directly with X. As a storage register, A is addressed and provides a single rapid-access storage location for either the single-extension (36 bits) or double-extension (72 bits) equivalent of one computer word. Its address is 2---- (only the first octal digit is of significance). As an "arithmetic register", A performs shifting and accumulating operations and holds the sum, difference, product, and dividend (remainder) during arithmetic operations. In additions and multiplications, sums and products may be accumulated up to 72 bits.

(1) BASIC PROPERTIES OF A. - The properties of A may summarized as follows: (1) A is a subtractive register, i.e., information transmitted into A in a storage operation or as part of an arithmetic or logical operation is subtracted from what A already stores; (2) A is a left circular shifting register, i.e., the "0" and "1" outputs of the flip-flop in each stage of A enable gates in the corresponding "0" and "1" input signal lines of the next stage of A, and the "0" and "1" outputs of stage A_{71} enable gates in the "0" and "1" input signal lines, respectively, of stage A_0. When these gates in the "0" and "1" input circuits of each stage of A are sampled by a AL1 (SHIFT A LEFT 1) signal, the bit stored in each stage of A is moved one stage to the left, and the bit in A_{71} is transmitted to A_0; and (3) A is a double-length register and can be used to register 72 bits in arithmetic and certain storage operations. The Accumulator is shown on the Block Diagram, Arithmetic Registers, in Envelope #1 of Volume 7.

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(a) TRANSMISSIONS TO AND FROM A. - All numbers inserted into A, either for storage purposes or for arithmetic reasons, are inserted into A exclusively from X, by the basic addition process. In all such transmissions from X, a 36-bit number is added to A; in most cases, the value added is automatically converted from the modulus of X ($2^{36} - 1$) to the modulus of A ($2^{72} - 1$) in the process.

(b) SHIFTING. - The basic unit operation of shifting can be performed in A. A number stored in A can be left circularly-shifted one place by the signal AL_1 (shift A left one place). This signal causes the bits in stages A_0 through A_{70} to be shifted to the left by one place and the contents of A_{71} to be shifted to A_0. The use of this property is discussed in subparagraph e, SHIFT CONTROL CIRCUITRY. The shifting of A is always under the control of AS

As in the case of Q and X, the "0" and "1" output enables of certain stages of A are used by the Arithmetic Sequence Control in directing certain steps in various ASC sequences of operations.

(c) ADDITION. - The basic unit operation of addition is perhaps the most important operation of the Arithmetic Section. There are two factors, however, which tend to complicate the comprehension of addition: one is the subtractive nature of the Accumulator, and the other is the double length of the Accumulator. The apparently contradictory facts that A is subtractive and that a fundamental operation of the computer is addition can be reconciled by examining the rules of binary subtraction and the nature of the $X^1 \rightarrow A_R$ transmission which inserts a number into A. The difficulty of inserting 36-bit numbers from X into the 72-stage A can be obviated by examining the nature and purpose of the higher-order 36-bits of double length extension numbers.

A binary subtraction table is given in Table 4-4 below:

TABLE 4-4

BINARY SUBTRACTION TABLE

1 - 0 = 1
1 - 1 = 0
0 - 0 = 0
0 - 1 = 1, with a borrow required from the next higher-order bit.

An examination of Table 4-4 shows that "0" subtracted from either a "0" or a "1" does not alter the "0" or the "1" in any way; and a "1" subtracted from a "0" or a "1" in each case reverses the value of the bit, and in the case of "1" subtracted from "0", initiates a borrow from the next higher-order bit. If the above binary subtraction table is applied to X and a subtractive A, rules for subtraction can be formulated as follows: (1) if no subtractive "1" signal is received from a stage in X, the state of the corresponding A_R flip-flop, whether "0" or "1", is not changed; (2) if a subtractive "1" signal is received from a stage in X, the state of the corresponding A_R flip-flop is reversed, and if the state of an A_R flip-flop is changed from "0" to "1", a borrow is initiated from the next higher order stage of A_R.

The first step in addition is actually a bit-by-bit subtraction, performed by application of the rules described above. The $X^1 \rightarrow A_R$ signal samples a gate in the "0" output circuit of each stage of X. Those gates enabled by "0" outputs from X send a "0" (subtractive) signal to their associated stage in A_R. Gates associated with stages in X which store a "1" do not issue a signal.

Because the "0" side of each X stage is used instead of the "1" side, it is apparent that the signal $X' \rightarrow A_R$ effectively subtracts the complement of X, not the actual contents of X, from A. Since in one's complement binary notation the complement of a number is the negative of that number, the net result initiated by $X' \rightarrow A_R$ can be expressed by the following equation:

$$A - (-X) = A + X$$

This equation implies that even though A is subtractive, the overall operation initiated by $X' \rightarrow A_R$ is additive.

In ordinary addition, the 72-bit extension of a 36-bit number is added to A. That is, if the left-hand bit of X is equal to "0", the number in X is positive, and therefore the 72-bit extension of this number would contain 36 "0's" on the left end. These 36 additional bits propagate the "sign bit" from the 2^{35} position to the 2^{71} position. When the quantity in X is positive, the problem of adding these 36 imaginary "0's" is resolved by sending an A_L INPUT signal to A_L. This signal effectively subtracts 36 "1's" from the left half of A, which is the equivalent of adding 36 "0's" to the left half of A.

The second step in addition is the generation of borrows which complete the numerical subtraction and correct the algebraic sign of the result. A "borrow" in a subtractive counter or accumulator is similar to a "carry" in an additive counter or accumulator, except that a "borrow" is used to "back" a stage by one count and a "carry" is used to "advance" a stage by one count. This "borrow" feature is what makes A subtractive rather than additive.

The "1" and "0" outputs of each Accumulator stage, are used to enable transfer gates, shift gates, "borrow" gates, and "rapid-borrow" gates. In A_R the "borrow" gate in each stage is enabled when the stage stores a "1" and the corresponding stage of X stores a "0". In A_L, the "borrow" gate in each stage is enabled when the associated stage stores a "1". The "rapid borrow" gate in each stage of both A_R and A_L is enabled when the stage with which it is associated stores a "0".

The first CONTROLLED CLOCK PULSE to be produced after the occurrence of the signal $X' \rightarrow A_R$ (and the signal A_L INPUT, if $X_{35} = 1$) generates an A_R PROBE signal (and an A_L PROBE signal if an A_L INPUT was produced). In A_R, the A_R PROBE signal samples the "borrow" gate associated with each stage. In every stage where the flip-flop was changed from "0" to "1" by the $X' \rightarrow A_R$ signal and the corresponding stage in X is a "0", a BORROW signal is produced. The BORROW signal indicates that a "1" was subtracted from a "0", and that a "1" must therefore be subtracted from the next higher order stage. Each BORROW signal produced enters the next higher-order stage of A and performs two functions: (1) it probes the "rapid borrow" gate in that next stage, and (2) it reverses the state of the flip-flop in that next stage.

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In those cases where the BORROW signal triggers the flip-flop in the next stage from "0" to "1", another borrow becomes necessary. This latter borrow is actually produced before the flip-flop changes state, since the BORROW signal probes the flip-flop's "rapid borrow" gate before reversing the state of the flip-flop. If the flip-flop stored a "0", the BORROW signal

passes through the "rapid borrow" gate as a RAPID BORROW signal. Each RAPID BORROW signal produced is then sent to the next higher-order stage and functions therein the same as a BORROW signal, in that it probes that stage's rapid borrow gate and triggers the flip-flop in that stage.

Simultaneously, in A_L, if an A_L INPUT is produced, all the "borrow" gates in A_L stages are sampled by the A_L PROBE signal. BORROW and RAPID BORROW signals are produced, and they function exactly the same in A_L as those in A_R. Borrows produced from stage A_{71} are sent to stage A_0. When all the borrows are achieved, the subtraction of the complement of the double length extension of the number in X from A is completed; i.e., the double-length extension of the number held in X is added to A.

The above discussion of the basic unit operation of addition can be summarized by the following rules:

Rule 1. A bit in an Accumulator stage is changed from "0" to "1" or from "1" to "0" (complemented) only if the corresponding bit in the X-Register is "0".

Rule 2. A "borrow" from the next higher-order stage is necessary if a bit in an Accumulator stage is changed from "0" to "1", as a result of Rule 1.

Rule 3. A "rapid-borrow" from the next higher-order stage is necessary if any borrow changes the bit in an Accumulator stage from "0" to "1".

An example of the application of these rules is given below. In this example, a positive number in X, equal to +5, is added to zero in A. For simplicity, a word length of only four bits is used, and X is considered to be a double-length register.

	(A_L)	(A_R)	(X_L)	(X_R)
1. Initial Conditions:	0000	0000	0000	0101

2. Following Rule 1, change each stage of the Accumulator which corresponds to a stage of X which stores a "0":

(A_L)	(A_R)
1111	1010

Note that this partial sum appears negative, since $A_7 = 1$

3. Following Rules 2 and 3, indicate a "borrow" by a slanted solid arrow ↙ from the next higher stage if an Accumulator stage is changed from "0" to "1", and indicate a "rapid-borrow" by a horizontal broken arrow ←- - if any borrow changes the bit in an Accumulator stage from "0" to "1"

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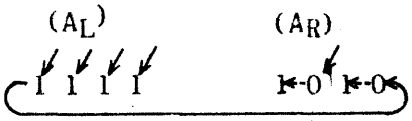

4. The final result after all borrows are completed is as follows:

(A_L)	(A_R)	(X_L)	(X_R)
0000	0101	0000	0101

This result is the sum of (X) and (A): 5 + 0. It is a double-length number and it is positive, since $A_7 = 0$.

The basic unit operation of addition described above is for "ordinary" addition; i.e., an addition operation where the left-most bit of X (stage X_{35}) is used to register the algebraic sign of the number. In "split" addition, the content of X is considered to be positive; the left-most bit is not used as a sign bit. For this reason, the A_L INPUT signal is always used in "split" addition. The "controlled complement" operation is a variation of addition where only the bit-by-bit sum (no borrows) of X and A_R is formed. For this operation, X is initially complemented then $X' \rightarrow A_R$ performs the addition. The A_L INPUT, A_R PROBE, and A_L PROBE signals are omitted.

Ordinary subtraction and split subtraction are similar to ordinary addition and split addition respectively, except that the contents of X is initially complemented. The total results can be expressed by the following equation:

$$A - \left[-X_f\right] = A - \left[- (-X_i) \right] = A - X_i$$

where A = number in A

X_i = number in X before complementing X

X_f = number in X after complementing X

(d) SUBTRACT 1 FROM A. - The basic operation of subtracting one from A differs from an addition operation, which would add minus one to A from X, in that it does not employ X. When the CTC signal SUBTRACT 1 FROM A is generated, it is used in a ASC sequence which produces an ARTIFICIAL A END BORROW signal. The ARTIFICIAL A END BORROW signal is sent to the Accumulator stage A_0 where it functions exactly the same as any regular borrow signal, in that it samples the rapid borrow gate of A_0 and triggers the A_0 flip-flop, etc. The content of A is thus reduced by one count in a manner quite distinct from the basic addition process employing X.

(2) OPERATION AS A STORAGE REGISTER. - A is the addressed storage location 2---- (only the first octal digit is significant). The (A) involved in a storage reference can be either a single or double length number, depending on the instruction being executed; in general, however, only a single length, or 36-bit word, stored in A_R is involved. In the paragraph which des-

scribes the Storage Section of the computer, the use of A as a storage register is thoroughly explained.

Usually, transmissions into A for storage purposes are 36-bit transmissions from X to A_R, and the sign bit of the transmitted word is propagated throughout A_L so that the number is ultimately stored in A as a 72-bit or double length number. In such transmissions, A is cleared and an arithmetic subsequence, ADD X TO A, is executed.

Transmissions out of A are produced by the signal $A_R \rightarrow X$. All 36-bits in A_R are effectively transmitted to X by first clearing X and then transmitting "1's" to those stages of X that correspond to stages in A_R which store a "1". The signal $A_R \rightarrow X$ samples gates in the "1" output circuits of the stages in A_R. Those gates enabled by "1" outputs from A_R send a "1" input signal to the corresponding stage of X.

(3) OPERATION AS AN ARITHMETIC REGISTER. - A is the basic arithmetic register. It forms the sum in additon (logical or arithmetic), the difference in subtraction, the product in multiplication (logical or arithmetic), and holds the dividend (initially) and the remainder (finally) in division. Although A is a subtractive register the basic operation of the computer is addition. A is made functionally additive by providing automatic complementing of a number during its transmission from X. Subtraction is performed by complementing the number before the transmission and automatic complementing take place. As an accumulator, A has double precision properties and the capacity to handle double length numbers. Details of the function A in arithmetic and logical operations are presented in the paragraph which describes the Arithmetic Section of the computer.

e. SHIFT CONTROL CIRCUITRY (SK, SKT, & SKC). - Shifting operations controlled by the Arithmetic Section involve the following shift control circuits: the Shift Counter (SK), the Shift Count Translator (SKT), and the Shift Counter Control (SKC). It should be noted that these circuits function only in shifting operations controlled by the Arithmetic Section. The following subparagraphs describe each of the shift control circuits in detail and outline a few of the applications of shifting as an arithmetic operation.

(1) SHIFT COUNTER - Since a storage reference requiring the use of SAR as an address register is never made during the shifting operation part of an instruction, the seven lower-order stages of SAR are used as a subtractive counter, called the Shift Counter. (See Block Diagram of Storage Address Register, Envelope #3, Volume 7.) During shifting operations which are part of ASC sequences, SK functions to store the number of left shifts (usually denoted as "k") which are to be performed involving either Q or A, or both Q and A. Upon receipt of a BACK SK signal from SKC, which signifies that one shifting operation has been carried out, the value of the shift count k is reduced by one count. The various values held in SK during the succeeding steps of shift operations are continually evaluated by the Shift Count Translator (SKT). SKT enables the Shift Counter Control (SKC) to regulate ASC sequences which involve shifting operations depending on which of the following conditions are detected: SK = 0, SK $\neq$ 0, SK = 1, SK = 38.

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The setting of SK to the initial shift count k is frequently accomplished automatically, either as an integral part of an ASC sequence of operations, or as part of the execution of an instruction. In such cases SK is made to store a shift value of 36 or 71 (decimal) when the corresponding signals SET SK TO 36 and SET SK TO 71, respectively, are produced. SK, however, can be set to any desired shift count k, during the execution of those instructions whose v-address portion specifies a programmed number of shifts. During the execution of such instructions, SAR is cleared, then the desired value k is inserted into SK by the transmission VAK → SAR.

Each time a shifting operation is performed in A or Q, the BACK SK signal is applied to the SAR_0 through SAR_6 flip-flops. The shifting operation terminates when the value held in SK is the critical value for the particular sequence being executed. In most cases, this critical value is reached when SK contains all "0's". The fact that SAR stages SAR_0 through SAR_6 hold all "0's" does not necessarily imply that the higher order stages of SAR are also "0's". For example, during instructions 31 uk, 32 uk, 33 uk, 34 uk, 54 uk, and 55 uk; if, at the time the transmission VAK→SAR occurs, the v-address portion of any of these instructions contains any "1's" in stages VAK_7 through VAK_{14}, the "1's" are transmitted to the corresponding higher-order stages of SAR. After the shifting operation is completed, even though the SK portion of SAR is backed to "0", any "1's" in the higher-order stages of SAR are still retained. If SAR is not left cleared after a shifting operation, it is possible that the next transmission into SAR (as PAK → SAR) will lead to a program error. On the other hand, by proper choice of values for the higher-order bits of the v-address portion of the instruction words mentioned above, it is possible that the above described feature, concerning the partial clearing of SAR after shifting operations, can prove quite useful.

(2) SHIFT COUNT TRANSLATOR - The Shift Count Translator (SKT), shown on the Block Diagram of Shift Counter Control, Envelope #2, Volume 7, receives the "0" and "1" output enables from SK stages SK_0 through SK_6 and translates these outputs into one of four enables for the Shift Counter Control: SK = 0, SK ≠ 0, SK = 1, and SK = 38. These SKT outputs specify the current condition of SK and are used to enable control gates in the Shift Counter Control (SKC).

(3) SHIFT COUNTER CONTROL. - The Shift Counter Control (SKC) is shown on the Block Diagram, Shift Counter Control, Envelope #2, Volume 7. It is a collection of gates and "OR" circuit which control the initiation of certain shifting operations, the backing of SK after each Arithmetic Section shifting operation, and the termination of all Arithmetic Section shifting operations. During some sequences of operations which involve shifting, SKC merely supplies the following SKT control enables to ASC: SK = 0 and SK ≠ 0. However, during the ASC/SKC sequences Shift Q, Shift A, Scale Factor, Multiply, and Divide, SKC not only supplies control enables but also produces signals which direct control over ASC.

(4) BASIC SHIFTING OPERATION. - The basic unit operation of shifting in A or Q is best described by an example. For example, in the ASC/SKC Multiply sequence, the product is formed in A by alternately conditionally adding Q to A, and shifting Q left by one place. An initial k value of 36 is inserted in SK by the SET SK TO 36 signal. After each shift in Q, a BACK SK signal backs

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SK by one count. When SK is reduced to the critical value of zero, the alternate adding and shifting sequence is terminated.

f. ARITHMETIC SEQUENCE CONTROL (ASC). - The Arithmetic Sequence Control is a collection of eleven sequence generating circuits. Each of these circuits directs the execution of one arithmetic sequence. The Overall Block Diagram of the Arithmetic Sequence Control, in Envelope #3 of Volume 7, shows the entire ASC system.

A study of the overall block diagram reveals that many of the gates and flip-flops are shared by several of the circuits — a feature which makes it difficult to recognize the individual sequence generating circuits. For this reason, selected portions of ASC and SKC have been redrawn for each of the eleven arithmetic sequences. These block diagrams are on two sheets, called Block Diagram, Parts of ASC, and Block Diagram, Divide Portion of ASC, both in Envelope #3 of Volume 7.

Most of the eleven arithmetic sequences are produced in circuits located entirely in the Arithmetic Sequence Control; these are called "ASC Sequences". A few of the sequences are executed in both ASC and SKC; these are called "ASC/SKC sequences".

Each sequence is performed in the following manner: (1) CTC sends an initiating command to ASC or SKC, and stops MPD; (2) the initiated sequence is carried out under the influence of CONTROLLED CLOCK PULSES; then (3) when the sequence is completed, ASC sends an ASC RESUME signal to the Master Clock System, which signifies that MPD may be advanced.

At the top of the Overall Block Diagram, Arithmetic Sequence Control, are shown a number of flip-flops which act together somewhat like a pulse distributor, in that they produce sequences of "probes" which carry out the various operations in ASC. When one of these flip-flops is set to "1", the next CONTROLLED CLOCK PULSE produces the corresponding probe signal (A_R PROBE, B PROBE, etc.), which clears the flip-flop to "0".

(1) ASC ADD X TO A SEQUENCE. - The diagram for this sequence is shown in the upper left corner of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. A timing chart for this sequence is on Page B-7 of Appendix B, in this volume.

The Add X to A sequence adds the double-length (72-bit) extension of a 36-bit addend D (u) stored in X to a 72-bit augend stored in A. The resulting 72-bit sum is left in A, and the original contents of X are left undisturbed.

When the signal ADD X TO A is received, the following sequence of probes is generated in ASC:

Step 1. $X' \rightarrow A_R$ (and A_L INPUT if X is positive).

Step 2. A_R PROBE (and A_L PROBE if X is positive).

Step 3. B PROBE, which produces ASC RESUME because the Extend Sequence flip-flop is in the "0" state.

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The above sequence performs the basic unit operation of addition, as follows: in Step 1, the $X' \rightarrow A_R$ signal forms the partial sum of X and A_R in A_R, by triggering each stage of A_R whose corresponding stage in X holds a "0"; also in Step 1, if (X) is positive, the A_L INPUT signal forms the partial sum of 36 zeros plus A_L in A_L, by triggering all stages of A_L; in Step 2, the A_R PROBE signal probes all the "borrow" gates in A_R to produce BORROW and RAPID BORROW signals which complete the sum in A_R; also in Step 2, if (X) was positive, the A_L PROBE signal probes the "borrow" gates of A_L to complete the sum in A_L; and finally, in Step 3, the ASC RESUME signal informs the Master Clock System that the arithmetic sequence has been completed.

Two examples of the numerical processes involved in the Add X to A sequence are given below. For simplicity, the examples use a hypothetical four-bit X register and eight-bit Accumulator.

Example 1: Add X to A

Augend = 10010100 = -107
Addend = 0011 = + 3
Sum = 10010111 = -104

		(A_L) (A_R)	(X)
1.	Initially	1 0 0 1 0 1 0 0	0 0 1 1
2.	$X' \rightarrow A_R$ A_L INPUT (since X_3=0)	0 1 1 0 1 0 0 0	0 0 1 1
3.	A_R PROBE A_L PROBE (since X_3=0)	0 1 1 0 1 0 0 0	0 0 1 1
	Result:	1 0 0 1 0 1 1 1	0 0 1 1
4.	ASC RESUME		

Example 2: Add X to A

Augend = 01100001 = +97
Addend = 1001 = - 6
Sum = 01011011 = +91

		(A_L)	(A_R)	(X)
1.	Initially	0 1 1 0 0 0 0 1		1 0 0 1
2.	$X' \rightarrow A_R$	0 1 1 0 0 1 1 1		1 0 0 1
3.	A_R PROBE	0 1 1 0 0 1 1 1		1 0 0 1
	Result:	0 1 0 1 1 0 1 1		1 0 0 1
4.	ASC RESUME			

(2) ASC SUBTRACT X FROM A SEQUENCE. - The diagram for this sequence is shown on the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. A timing chart for this sequence is on Page B-88 of Appendix B, in this volume.

In this sequence, the double-length extension of a 36-bit subtrahend held in X is subtracted from a 72-bit minuend initially held in A. The resulting 72-bit difference is left in A, and the complement of original contents of X is left in X.

In ASC, the SUBTRACT X FROM A signal sets the Delayed Add flip-flop to "1" and produces COMPLEMENT X, which forms the negative of the subtrahend in X. Next, the following sequence of probes is produced in ASC:

Step 1. "1" FROM DELAYED ADD, which produces $X' \rightarrow A_R$ (and A_L INPUT if X is positive).

Step 2. A_R PROBE (and A_L PROBE if X is positive).

Step 3. B PROBE, which produces ASC RESUME because the Extend Sequence flip-flop is in the "0" state.

These probes perform a basic addition operation, but because X is first complemented, the overall effect is a subtraction of the original (X) from A.

An example of the numerical processes involved in the Subtract X from A sequence is given below. The example uses a hypothetical four-bit X register and eight-bit A.

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Example 3: Subtract X from A

Minuend = 00100001 (+33)
Subtrahend = 1110 (- 1)
Difference = 00100010 (+34)

		(A_L) (A_R)	(X)
1.	Initially	0 0 1 0 0 0 0 1	1 1 1 0
2.	COMPLEMENT X	0 0 1 0 0 0 0 1	0 0 0 1
3.	$X' \rightarrow A_R$ A_L INPUT	1 1 0 1 1 1 1 1	0 0 0 1
4.	A_R PROBE A_L PROBE	1 1 0 1 1 1 1 1	
	Result:	0 0 1 0 0 0 1 0	0 0 0 1
5.	ASC RESUME		

(3) ASC SPLIT ADD X TO A SEQUENCE. - The diagram for this sequence is shown in the upper center portion of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. A timing chart for this sequence is on Page B-90 of Appendix B, in this volume.

The Split Add X to A sequence adds a single-length (36-bit) addend S(u) stored in X to a 72-bit augend stored in A. The addend S(u) is always considered to be a 36-bit positive number. The resulting 72-bit sum is left in A, and the original contents of X are left undisturbed.

When the signal SPLIT ADD X TO A is received, the following sequence of probes is generated in ASC:

Step 1. $X' \rightarrow A_R$ and A_L INPUT.

Step 2. A_R PROBE and A_L PROBE.

Step 3. B PROBE, which produces ASC RESUME because the Extend sequence flip-flop is set to "0".

The only difference between the Add X to A sequence and the Split Add X to A sequence is that the A_L INPUT and A_L PROBE are always produced during the Split Add X to A sequence. The overall effect is that the contents of X, considered to be a 36-bit positive number, is added to A.

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An example of the numerical processes involved in the Split Add X to A sequence is given below, for a hypothetical four-bit X and eight-bit A.

Example 4: Split Add X to A

Augend = 10110110 = -73
Addend = 1101 = +13 (not -2)
Sum = 11000011 = -60

		(A_L)	(A_R)	(X)
1.	Initially	1 0 1 1 0	1 1 0	1 1 0 1
2.	$X' \rightarrow A_R$, A_L INPUT	0 1 0 0 0	1 0 0	1 1 0 1
3.	A_R PROBE, A_L PROBE	0 1 0 0 0	1 0 0	1 1 0 1
	Result:	1 1 0 0 0	0 1 1	1 1 0 1
4.	ASC RESUME			

(4) ASC SPLIT SUBTRACT X FROM A SEQUENCE. - The diagram for this sequence is shown in the upper right-hand corner of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. A timing chart for this sequence is on Page B-89 of Appendix B.

The Split Subtract X from A sequence subtracts a single-length (36-bit) subtrahend S(u) stored in X from a 72-bit minuend held in A. The subtrahend S(u) is always considered to be a 36-bit positive number. The resulting 72-bit difference is left in A, and the complement of the original contents of X is left in X.

In ASC, the SPLIT SUBTRACT X FROM A signal sets the Split Subtract flip-flop to "1" and produces COMPLEMENT X, which forms the complement of the subtrahend in X. Next, the following sequence of probes is produced in ASC:

Step 1. "1" FROM SPLIT SUBTRACT, which produces $X' \rightarrow A_R$

Step 2. A_R PROBE

Step 3. B PROBE, which produces ASC RESUME because the Extend Sequence flip-flop is in the "0" state.

As in the Subtract X from A sequence, these probes perform a basic addition operation with a complemented X so that the overall effect is a subtraction of the original (X) from A. The only difference between the Subtract X from A sequence and the Split Subtract X from A sequence is that the A_L INPUT and A_L PROBE are never produced during the Split Subtract X from A Sequence. As a result, the original content of X is subtracted as a 36-bit positive number from A.

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An example of the numerical processes involved in the Split Subtract X from A sequence is given below, for a four-bit X and an eight-bit A.

Example 5: Split Subtract X from A

Minuend = 10110110 = -73
Subtrahend = 1101 = +13 (not -2)
Difference = 10101001 = -86

		(A_L)	(A_R)	(X)
1.	Initially	1 0 1 1	0 1 1 0	1 1 0 1
2.	COMPLEMENT X	1 0 1 1	0 1 1 0	0 0 1 0
3.	$X' \rightarrow A_R$	1 0 1 1	1 0 1 1	0 0 1 0
4.	A_R PROBE	1 0 1 1	1 0 1 1	0 0 1 0
	Result:	1 0 1 0	1 0 0 1	0 0 1 0
5.	ASC RESUME			

(5) ASC SUBTRACT 1 FROM A SEQUENCE. - The diagram for this sequence is shown on the center of the left side of the Block Diagram, Part of ASC, in Envelope #3 of Volume 7. The timing chart is on Page B-89 of Appendix B.

Certain instructions are executed for the purpose of making some sort of decision as to how the program of instructions is to be continued. This decision in most cases is based on the condition of A. One method of detecting the condition of A employs the ASC Subtract 1 from A sequence. The value one is subtracted from the 72-bit number in A by an artificially produced subtractive signal. The result, the original 72 bit number held in A minus one, is retained in A and the condition of A is reported to the control section. The contents of X is not used or affected in any way.

In ASC, the signal SUBTRACT 1 FROM A sets the Initiate A-1, Extend Sequence, and B Probe flip-flops to "1". Next, the following sequence of probes is produced in ASC:

Step 1. B PROBE, which produces ARTIFICIAL A END BORROW.

Step 2. C PROBE.

Step 3. D PROBE, which clears the Initiate A-1 and Extend Sequence flip-flops to "0", and produces ASC RESUME.

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The ARTIFICIAL A END BORROW signal produced by the B PROBE is sent to stage A_0, where it effects the subtraction of one from A. If A stores all "0's", the subtraction of one from A will produce an A_{71} BORROW signal. In ASC, this A_{71} BORROW signal passes through a gate (V03-10074) and is issued as a SET A ZERO signal. The SET A ZERO signal sets the A ZERO flip-flop V80-30242 (see Block Diagram, Main Control Translator, Envelope #4, Volume 7) to "1". The resulting A ZERO "1" enable is supplied to the auxiliary translator in MCT, and the condition of A after the subtraction of one is thereby reported. An example of the

numerical processes involved is given below.

Example 6: Subtract 1 From A

(A_i) = 00011000 (+24)

(A_f) = 00010111 (+23)

	(A_L)	(A_R)
1. Initially	0 0 0 1 1	0 0 0
2. ARTIFICIAL END BORROW	0 0 0 1 1	0 0 0
Result:	0 0 0 1 0	1 1 1
3. Delay		
4. ASC RESUME		

(6) ASC LOGICAL SEQUENCE. - The diagram for this sequence is shown in the center of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. A timing chart for this sequence is on Page B-91 of Appendix B.

The ASC Logical Sequence adds the value L(Q)(X) to the 72-bit number in A, where L(Q)(X) is a 36-bit positive number whose bits are each equal to the product of the corresponding bits in X and Q. The 72-bit result of the operation, A_i + L(Q)(X), is left in A, (X) is left equal to zero, and the complement of the original contents of Q is left in Q. Operations using this sequence are often called "Q-controlled" operations, because the sequence can be used to add selected bits of the quantity in X to A, by insertion of a "control mask" in Q.

To start the sequence, CTC produced two command signals simultaneously: INITIATE LOGICAL and EXTEND ARITHMETIC SEQUENCE. In ASC, the INITIATE LOGICAL signal sets the Delayed Add and Initiate Logical flip-flops to "1" and produces Q^0 X^0, and the EXTEND ARITHMETIC SEQUENCE signal sets the Extend Sequence flip-flop to "1". Next, the following sequence of probes is produced in ASC:

Step 1. "1" FROM DELAYED ADD, which produces X'→A_R and A_L INPUT.

Step 2. A_R PROBE and A_L PROBE; the A_R PROBE produces CLEAR X and sets the Restore X flip-flop to "1".

Step 3. B PROBE, which produces COMPLEMENT X and clears Restore X to "0".

Step 4. C PROBE, which clears the Extend Sequence flip-flop to "0", and produces Q'→X^0 and CLEAR Q.

Step 5. D PROBE, which produces COMPLEMENT X and sets the E Probe flip-flop to "1".

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Step 6. E PROBE, which clears the Initiate Logical flip-flop to "0" and produces X→Q, CLEAR X, and ASC RESUME.

The first Q'→X' signal, produced on receipt of the INITIATE LOGICAL signal, performs the basic unit operation of logical (bit-by-bit) multiplication in X, as described in the text on the Arithmetic Registers.

Steps 1 and 2 add the logical product in X to A. In this addition, A_L INPUT and A_L PROBE are always produced, so that the content of X is always added as a positive 36-bit value, as in the Split Add X to A sequence. Also, during the addition, the A_R PROBE produces CLEAR X to prepare X for receipt of information.

Because X is cleared in Step 2 and complemented to all ones in Step 3, the Q'→X' signal produced in Step 4 effectively transmits the "control mask" in Q to X. In Step 5, the COMPLEMENT X signal complements the mask in X. Next, Step 6 produces X→Q to transmit the complemented mask back to Q, so that the resulting new mask may be used in another operation.

This sequence is used in three instructions. For the Q-Controlled Transmit (51uv) instruction, A is initially cleared, and the sequence adds L(Q)(u) to A. For the Q-controlled Add (52uv) instruction, A is initially set to the desired augend. For the Q-Controlled Substitute (53uv) instruction, A is initially cleared, one ASC Logical Sequence adds L(Q)(u) to A, then a second ASC Logical Sequence adds L(Q)'(v) to A, where (Q)' is the complemented mask left from the first ASC sequence.

An example of the Logical Sequence is given below, for a four-bit X, a four-bit Q, and an eight-bit A.

Example 7: Logical (Q)(X)

$(A)_i$	00000000
$(Q)_i$	1010
$(X)_i$	1100
$(A)_f$	00001000
$(Q)_f$	0101
$(X)_f$	0000

		(A_L) (A_R)	(X)	(Q)
1.	Initially	0 0 0 0 0 0 0 0	1 1 0 0	1 0 1 0
2.	Q'→X'	0 0 0 0 0 0 0 0	1 0 0 0	1 0 1 0
3.	X'→A_R, A_L INPUT	1 1 1 1 0 1 1 1	1 0 0 0	1 0 1 0
	A_R PROBE, A_L PROBE	1 1 1 1 0 1 1 1	1 0 0 0	1 0 1 0
	CLEAR X		0 0 0 0	
	Result:	0 0 0 0 1 0 0 0	0 0 0 0	1 0 1 0
4.	COMPLEMENT X	0 0 0 0 1 0 0 0	1 1 1 1	1 0 1 0
5.	Q'→X', CLEAR Q	0 0 0 0 1 0 0 0	1 0 1 0	0 0 0 0
6.	COMPLEMENT X	0 0 0 0 1 0 0 0	0 1 0 1	0 0 0 0
7.	X→Q, CLEAR X, and ASC RESUME	0 0 0 0 1 0 0 0	0 0 0 0	0 1 0 1

(7) ASC/SKC SHIFT A SEQUENCE. - The diagram for this sequence is shown on the center of the right side of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. The timing charts are on Page B-92 of Appendix B.

The ASC/SKC Shift A sequence shifts the 72-bit number in A circularly to the left the number of places specified by the shift count "k" initially stored in SK. The value "k" is inserted into SK by the transmission VAK→SAR prior to the time the INITIATE SHIFT A signal, produced in CTC, is sent to SKC. If k = 0, as indicated by the SKT enable SK = 0, no signals are produced in SKC, and no WAIT INTERNAL REFERENCE is produced in CTC. MPD continues, therefore, to advance and no shift is carried out. If SK ≠ 0, the INITIATE SHIFT A signal (1) passes through gate V02-30193 in SKC and is issued to CTC as a WAIT SHIFT signal; (2) passes through gate V03-30193 in SKC and is sent to ASC as SET INITIATE A LEFT, which sets the Initiate A Left flip-flop to "1". The WAIT SHIFT signal sent to CTC produces a WAIT INTERNAL REFERENCE signal for PDC.

In ASC, the setting of the Initiate A Left flip-flop to "1" allows CONTROLLED CLOCK PULSES to pass through gate V06-044. Each pulse produces AL1 (Shift A Left 1) and SHIFT A OR Q. Each AL1 signal shifts (A) left by one place. Each SHIFT A OR Q signal backs SK, and probes a gate enabled by SK = 1. If SK = 1, as a result of a previous shift, the resulting "kth" SHIFT A OR Q signal finds the SK = 1 gate enabled, produces an END SHIFT signal which clears the Initiate A Left flip-flop to "0", and passes through gates V12 and V04-30193 to produce ASC RESUME.

An example of the Shift A sequence is given below for a hypothetical eight-bit A.

Example 8: Shift A

$(A)_i$ 1 0 0 1 0 1 1 0

$(SK)_i$ 4

$(A)_f$ 0 1 1 0 1 0 0 1

		(A_L) (A_R)	(SK)
1.	Initially:	1 0 0 1 0 1 1 0	4
2.	AL1, BACK SK	0 0 1 0 1 1 0 1	3
3.	AL1, BACK SK	0 1 0 1 1 0 1 0	2
4.	AL1, BACK SK	1 0 1 1 0 1 0 0	1
5.	AL1, BACK SK, and ASC RESUME	0 1 1 0 1 0 0 1	0

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(8) SKC/ASC SHIFT Q SEQUENCE. - The diagram for this sequence is shown on the lower-left hand corner of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. The timing charts are on Page B-93 in Appendix B.

The ASC/SKC Shift Q sequence shifts the 36 bit number stored in Q circularly to the left the number of places specified by the shift count "k" initially stored in SK.

This sequence is carried out in the same manner as the ASC/SKC Shift A sequence. The following differences concerning CTC, ASC, and SKC, however, should be noted: (1) the ASC/SKC SHIFT Q sequence is initiated by the INITIATE SHIFT Q command rather than the INITIATE SHIFT A command; (2) if initially SK $\neq$ 0, the INITIATE SHIFT Q signal passes through gate V01-30193 in SKC (not gate V03-30193) and sets the Initiate Q Left flip-flop V82-10043, rather than the Initiate Shift A flip-flop; and (3) Gate V05-10043 (enabled by the "1" output of the Initiate Shift Q flip-flop), not gate V06-10044,conducts the CONTROLLED CLOCK PULSES which time the shifting of Q and backing of SK, and which test for end of the shifting operation. An example of the Shift Q sequence is given below for hypothetical four-bit Q.

Example 9: Shift Q

$(Q)_i = 0\ 0\ 1\ 0$

$(SK)_i = 1$

$(Q)_f = 0\ 1\ 0\ 0$

	(Q)	(SK)
1. Initially	0 0 1 0	1
2. QL 1, BACK SK, ASC RESUME	0 1 0 0	0

(9) ASC/SKC SCALE FACTOR SEQUENCE. - The diagram for this sequence is shown on the lower center section of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. The timing chart is shown on Page B-94 in Appendix B.

Prior to the initiation of the ASC/SKC Scale Factor sequence, a 72-bit number stored in A is left-circularly shifted 36 places by the above described ASC/SKC Shift A sequence, with k = 36. The ASC/SKC Scale Factor sequence then functions to continue shifting the 72-bit number in A until the most significant bit of the original number in A appears in stage A_{34}, or if all 0's or all "1"s were originally stored in A until all the bits of the original word have been tested. In all cases, except when all 0's or all 1's are stored in A, when the sequence is completed, the sign bit of the original word is in A_{35}, and the most significant bit is in A_{34}; the rest of the bits are arranged according to their original pattern as modified by the left circular shifting operations; and SK contains the number of shifts necessary to return (A) to its original position.

When the INITIATE SCALE FACTOR signal is produced in CTC, it produces a SET SK TO 36 signal which inserts a shift count of 36 in SK, and it sets the Initiate Scale Factor flip-flop in ASC to "1". Each CONTROLLED CLOCK PULSE to occur thereafter passes through gate V03-10042 and samples a gate in two comparision circuits. One comparison circuit contains two gates V06-10071 and V05-10071 which are both enabled when the bits stored in A_{34} and A_{35} are the same, either both "0's" or both "1's". The other comparison circuit contains

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two gates, V06-10072 and V05-10072, which are both enabled when the bits stored in A_{34} and A_{35} are different. When each CONTROLLED CLOCK PULSE occurs, only one comparison circuit generates an output. The output from the first circuit ($A_{34} = A_{35}$) produces an AL 1 (shift A left one place) signal, and produces one or more of the following three other signals, depending on the value in SK: BACK SK (if SK $\neq$ 0), SET SK TO 71 (if SK = 0), ASC RESUME (if SK = 38). The output from the second circuit ($A_{34} \neq A_{35}$) simply clears the Initiate Scale Factor flip-flop and produces an ASC RESUME.

When $A_{34} \neq A_{35}$, the sign bit and most significant bit are in A_{35} and A_{34}, respectively, and the operation is completed. Accordingly, the Initiate Scale Factor flip-flop is cleared, and an ASC RESUME is sent to PDC. SK then holds the value "k", which is the number of shifts required to restore the number in A to its original position in A.

If the above condition $A_{34} = A_{35}$ is detected for 36 consecutive CONTROLLED CLOCK PULSES, the following signals are generated when the 37th CONTROLLED CLOCK PULSE is produced: AL 1, which performs the 37th shift; and SET SK TO 71, which inserts the number 71 in SK so that shifting can continue. (Setting SK to 71 is equivalent to setting SK to 72 and producing the BACK SK signal.)

The testing, shifting, and backing of SK then continue. If the condition $A_{34} \neq A_{35}$ is not detected by the time the new count stored in SK is reduced to 38, the following signals are produced: AL 1, which performs the 71st shift; BACK SK which leaves 37 stored in SK; and ASC RESUME and CLEAR INITIATE SCALE FACTOR FLIP-FLOP, which terminate the sequence.

The value stored in SK at the end of an ASC/SKC Scale sequence, designated as "k", is used as an index of the size of the number initially contained in A, as follows:

(a) If k = 36, the original number in A had its sign bit in A_{71} and its most significant bit in A_{70}.

(b) If $0 < k < 36$, the original number in A had its most significant bit somewhere between A_{36} and A_{69}; and the higher-order stages of A, beyond the one holding the most significant bit, all stored the propagated sign bit.

(c) If k = 0, the original number in A had its most significant bit in A_{34} and stages A_{35} through A_{71} all stored the propagated sign bit.

(d) If k = 37, all "0's" or all "1's" were originally stored in A.

(e) If $37 < k \leq 71$, the original number in A had its most significant bit somewhere between A_0 and A_{33}, and the higher order stages of A, beyond the one holding the most significant bit, all stored the propagated sign bit.

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An example for the Scale Factor operation is given below, for a hypothetical eight-bit A.

Example 10: Scale Factor

$(A)_i$	1111	1101
$(A)_f$	1111	1011
$(SK)_i$	4	
$(SK)_f$	7	

Prior to ASC/SKC Scale Factor Sequence	(A_L)	(A_R)	(SK)
1. Initial Conditions:	1 1 1 1	1 1 0 1	4
2. ASC/SKC SHIFT A sequence (k=4)	1 1 0 1	1 1 1 1	0
ASC/SKC Scale Factor Sequence			
1. Set SK to 4	1 1 0 1	1 1 1 1	4
2. ($A_3 = A_2$, and SK $\neq$ 0)			
AL 1, BACK SK	1 0 1 1	1 1 1 1	3
3. ($A_3 = A_2$, and SK $\neq$ 0)			
AL 1, BACK SK	0 1 1 1	1 1 1 1	2
4. ($A_3 = A_2$, and SK $\neq$ 0)			
AL 1, BACK SK	1 1 1 1	1 1 1 0	1
5. ($A_3 = A_2$, and SK $\neq$ 0)			
AL 1, BACK SK	1 1 1 1	1 1 0 1	0
6. ($A_3 = A_2$, but SK = 0)			
AL 1, SET SK TO 7	1 1 1 1	1 0 1 1	7
7. ($A_3 \neq A_2$)			
ASC RESUME	1 1 1 1	1 0 1 1	7

By comparing $(A)_f$ with the $(A)_i$ it can be seen that $(A)_f$ must be shifted seven places to the left to restore $(A)_i$.

(10) ASC/SKC MULTIPLY SEQUENCE. - The diagram for this sequence is shown in the lower right-hand corner of the Block Diagram, Part of Arithmetic Sequence Control, in Envelope #3 of Volume 7. The timing chart is on Page B-95 of Appendix B.

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The ASC/SKC Multiply sequence adds to the 72-bit number, initially stored in A, the product of a 36-bit multiplier stored in Q, and a 36 bit multiplicand stored in X. If A is cleared prior to the initiation of this sequence, D(Q)(X) is formed in A; if A is not initially cleared, A_i + D(Q)(X) is formed in A. The (X) and (Q) are left in their initial state at the end of the sequence.

The ASC/SKC Multiply sequence consists of the following three phases: (a) test for "overflow" and initial correction; (b) the multiplication; and (c) the test for final correction.

(a) TEST FOR OVERFLOW AND INITIAL CORRECTION. - The INITIATE MULTIPLY signal from CTC produces two other signals simultaneously: EXTEND ARITHMETIC SEQUENCE and SET SK TO 36. The EXTEND ARITHMETIC SEQUENCE signal sets the Extend Sequence flip-flop in ASC to "1". The SET SK TO 36 signal inserts a shift value of 36 in SK. In addition to producing the above two signals, the INITIATE MULTIPLY signal probes a set of gates in ASC and a set of gates in the Fault Detector. In ASC gates V10-10052 and V11-10052 are probed to test whether or not an initial correction is necessary and to prepare ASC for the multiply sequence. In the Fault Detector gates V12-10082 and V11-10082 are probed to test for possible "overflow" or loss of information.

If gate V12-10082 conducts (A_{35} = 1) and its output also passes through gate V11-10092 (A_{34} = 0), or if gate V11-10082 conducts (A_{35} = 0) and its output passes through gate V12-10092 (A_{34} = 1), the computer will stop and an OVERFLOW fault will be registered. This signifies, not that an "overflow" has been detected, but that if multiplication were to continue there is danger of an overflow.

If $A_{34} = A_{35}$, the test for "overflow" will not produce any effect.

In ASC, the INITIATE MULTIPLY signal sets the Initiate Multiply flip-flop to "1". If Q is negative (Q_{35} = 1), an initial correction is necessary. For this reason, (Q_{35} = 1), the INITIATE MULTIPLY signal also produces COMPLEMENT X, and sets the Restore X and Delayed Add flip-flops to "1", so that the Delayed Add flip-flop produces a sequence of probes which carries out the addition of the Complement of X to A, which in turn effectively subtracts X from A. When a C PROBE is produced, gate V04-062, enabled by SK $\neq$ 0, sets the Multiply Step flip-flop to "1" so that the multiplication phase is started.

If Q is initially positive, no initial correction is necessary, and the INITIATE MULTIPLY signal from CTC sets both the Initiate Multiply and Multiply Step flip-flops to "1".

(b) THE MULTIPLICATION. - The Multiplication Phase consists of 36 sequences of steps. The particular sequence carried out each time is based on the current value of Q_{35} and the number stored in SK.

If SK $\neq$ 1, each multiplication sequence is as follows:

Step 1. ALl shifts (A) one place to the left.

Step 2. BACK SK subtracts one from k.

Step 3. If Q_{35} = 1, the operation ADD X TO A adds the multiplicand to (A).

Step 4. QL1 shifts (Q) one place to the left.

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If SK = 1, similar sequences are performed, depending on Q_{35}, but, in addition, ASC is prepared for termination by clearing the Extend Sequence flip-flop to "0".

If Q_{35} = 1, the output of gate V04-10061 produces the AL1, QL1, and BACK SK signals and passes through gate V02-10071. The output of gate V02-10071 then clears the Multiply Step flip-flop and sets the Delayed add flip-flop. Subsequence CONTROLLED CLOCK PULSES carry out an ASC addition sequence which terminates by setting the Multiply Step flip-flop back to "1". The next step may then be carried out.

If Q_{35} = 0, the output of gate V04-10061 merely produces the AL1, QL1, and BACK SK signals. The next step may then be carried out immediately. The same CONTROLLED CLOCK PULSE , which samples gate V04-10061 at the beginning of each of the 36 steps in the multiplication phase, also probes gate V10-30193. This gate does not conduct until the initiation of the 36th step. At that time SK is backed to 1. Q_{35} is tested and, depending on its value, the above described operations are carried out as in the other steps. However, on the 36th step, gate V10-30193 in SKC conducts and issues a signal to gate V02-10062 in ASC, gate V02-10062 then conducts, clears the Multiply Step flip-flop, and probes gate V01-10072. If Q_{35} = 0, gate V01-10072 conducts and sets the B Probe flip-flop to "1". The multiplication phase is then completed and the test for final correction initiated.

(c) TEST FOR FINAL CORRECTION. - If Q_{35} = 1 at the start of the 36th multiplication step, an addition of X to A is performed, which leads to the production of a C PROBE. The C PROBE signal passes through a gate enabled by SK = 0, clears the Initiate Multiply and Extend Sequence flip-flops to "0", and tests for the final correction.

If Q_{35} = 0, at the start of the 36th multiplication step, no addition is performed, but the last SHIFT A OR Q signal produces END MULTIPLY STEP, which passes through gate V01-10072, enabled by Q_{35} = 0, and sets the B Probe flip-flop to "1". The resulting B PROBE produces C PROBE, which performs the test for end correction.

If Q_{35} = 1, a final correction is necessary. If this is the case, gate V02-10071, enabled by Q_{35} = 1, sets the Delayed Add flip-flop to "1", thereby initiating the final addition of X to A. If Q_{35} = 0, no correction is necessary, and ASC RESUME is produced.

Example 10: Multiply

Multiplicand: 0011 (3)
Multiplier: 1101 (-2)
Product: 11111001 (-6)

		(A_L)	(A_R)	(X)	(Q)	(SK)
1.	Initially	0 0 0 0 0 0 0 0		0 0 1 1	1 1 0 1	4
2.	COMPLEMENT X			1 1 0 0		
3.	$X' \rightarrow A_R$	0 0 0 0 0 0 1 1				
4.	A_R PROBE	1 1 1 1 1 1 0 0				
5.	COMPLEMENT X			0 0 1 1		
6.	AL1, QL1, BACK SK	1 1 1 1 1 0 0 1			1 0 1 1	3
7.	$X' \rightarrow A_R, A_L$ INPUT	0 0 0 0 0 1 0 1				
8.	A_R PROBE, A_L PROBE	1 1 1 1 1 1 0 0				
9.	AL1, QL1, BACK SK	1 1 1 1 1 0 0 1			0 1 1 1	2
10.	$X' \rightarrow A_R$, A_L INPUT	0 0 0 0 0 1 0 1				
11.	A_R PROBE, A_L PROBE	1 1 1 1 1 1 0 0				
12.	AL1, QL1, BACK SK	1 1 1 1 1 0 0 1			1 1 1 0	1
13.	AL1, QL1, BACK SK	1 1 1 1 0 0 1 1			1 1 0 1	0
14.	$X' \rightarrow A_R$, A_L INPUT	0 0 0 0 1 1 1 1				
15.	A_R PROBE, A_L PROBE	1 1 1 1 0 1 1 0				
16.	$X' \rightarrow A_R$, A_L INPUT	0 0 0 0 1 0 1 0				
17.	A_R PROBE, A_L PROBE	1 1 1 1 1 0 0 1				
18.	ASC RESUME					

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Example 11: Multiply

Multiplicand:	1011	(-4)	
Multiplier:	0110	(+6)	
Product:	11100111	(-24)	

		(A_L) (A_R)	(X)	(Q)	(SK)
1.	Initially	0 0 0 0 0 0 0 0	1 0 1 1	0 1 1 0	4
2.	AL1, QL1, BACK SK	0 0 0 0 0 0 0 0		1 1 0 0	3
3.	AL1, QL1, BACK SK	0 0 0 0 0 0 0 0		1 0 0 1	2
4.	$X' \rightarrow A_R$	0 0 0 0 0 1 0 0			
5.	A_R PROBE	1 1 1 1 1 0 1 1			
6.	AL1, QL1, BACK SK	1 1 1 1 0 1 1 1		0 0 1 1	1
7.	$X' \rightarrow A_R$	1 1 1 1 0 0 1 1			
8.	A_R PROBE	1 1 1 1 0 0 1 1			
9.	AL1, QL1, BACK SK	1 1 1 0 0 1 1 1		0 1 1 0	0
10.	ASC RESUME				

(11) ASC/SKC DIVIDE SEQUENCE. - The diagram for this sequence is called Block Diagram, Divide Portion of ASC, and is found in Envelope #3 of Volume 7. A timing chart for this sequence is given on Pages B-95 and B-96 in Appendix B.

The ASC/SK Divide sequence divides a 36-bit divisor stored in X into a 72-bit dividend initially stored in A, creating a 36-bit quotient in Q and a positive remainder (always smaller than the absolute value of the divisor) in A. The sequence is initiated by the INITIATE DIVIDE, EXTEND ARITHMETIC SEQUENCE and SET SK to 36 signals and consists of four phases: (a) the initial correction; (b) the initial shift; (c) the division; and (d) the final or end correction. During the performance of the division phase, two division checks are performed. These checks determine whether or not the quotient resulting from the operation will exceed the capacity of Q. If it will, the signal DIVIDE CHECK STOP is transmitted to the Control Section, where it initiates an A Fault computer stop.

To understand the function of the initial and end corrections, it is necessary to understand the form in which the quotient is presented. The division is

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performed in such a manner that the remainder is always positive, and that the results always satisfy the following equation:

$$(Q)(X) = (A_i) - (A_f)$$

Where (Q) = quotient
(X) = divisor
(A_i) = dividend
(A_f) = positive remainder

Four examples are given below, in decimal notation:

Example A: $\frac{-30}{+7}$ = -5 and +5 remainder

Example B: $\frac{-30}{-7}$ = +5 and +5 remainder

Example C: $\frac{+30}{-7}$ = -4 and +2 remainder

Example D: $\frac{+30}{+7}$ = +4 and +2 remainder

These results are all correct in that they each satisfy the basic division equation given above.

To produce results like these, it is necessary to perform certain initial and end corrections on (A). For example, if the dividend is negative and the divisor is positive, as is the case for example A above, the following steps are used to obtain the positive remainder:

Initially: (A) = -30, and (X) = +7.

Step 1: Subtract (X) from (A), leaving (A) = -37 and (X) = +7.

Step 2: Divide (A) by (X), leaving -5 in Q and a remainder of -2 in A.

Step 3: Add (X) to (A), leaving a remainder of +5 in A.

The specific rules for initial and end corrections of this type are given in subparagraphs (a) and (d) below.

To understand the nature of the division operation, it is necessary to understand the function of Q during division. For example, decimal division may be performed in two ways:

Method 1. The divisor is alternately shifted one place to the right and subtracted repeatedly from the dividend until subtraction is no longer possible. The number of subtractions performed after each shift is recorded as a positive number.

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```
          ++
          21  = Quotient, Q
012/ 0256
   -012
   -012
    016
   -012
      4 remainder
```

The quotient for this example is interpreted as follows:

$$Q = +2 \times 10^1 + 1 \times 10^0 = 21$$

Method 2. The divisor is alternately shifted one place to the right then repeatedly subtracted (or added if the remainder is negative) until the remainder changes in sign. Each subtraction is counted and the number recorded as positive; each addition is counted and the number recorded as negative.

```
                    +-
                    39  = Quotient, Q
                012/0256
                  -012
                  -012
                  -012
                  9895
(Negative, in     +012
 nine's comple-   +012
 ment system)     +012
                  +012
                  +012
                  +012
                  +012
                  +012
                  +012
                  +012
                    4 remainder
```

The quotient is interpreted as follows:

$$Q = +3 \times 10^1 - 9 \times 10^0 = 21$$

It is interesting that Method 2 applied to binary numbers in the one's complement system is extremely simple, in that after each shifting operation, only one addition or subtraction is required. Each addition is recorded in Q by a digit "0" and each subtraction is recorded by a digit "1". The interpretation of the results in Q is even simpler, in that it requires only that the contents of Q be shifted left by one place and the contents of stage Q_{35} be transmitted to stage Q_0. In applying Method 2 to X and A, the dividend in A is initially shifted into position for the first subtraction or addition, and is shifted to the left by one place after each step. This is done instead of shifting the divisor, as was done in the example for Method 2.

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(a) THE INITIAL CORRECTION. - To start the sequence, CTC first produces a SET SK TO 36 signal which sets the Shift Counter to 36, then produces two command signals simultaneously: INITIATE DIVIDE and EXTEND ARITHMETIC SEQUENCE . In ASC, the EXTEND ARITHMETIC SEQUENCE signal sets the Extend Sequence flip-flop to "1". The function INITIATE DIVIDE signal depends upon the initial condition of (A).

1. A NEGATIVE, X POSITIVE. - If $A_{71} = 1$ and $X_{35} = 0$, the INITIATE DIVIDE signal sets the Initiate Divide, Divide Case, and Delayed Add flip-flops to "1", and produces COMPLEMENT X. The following sequence of probes are produced in ASC:

Step 1. "1" FROM DELAYED ADD, which produces $X' \rightarrow A_R$ and A_L INPUT.

Step 2. A_R PROBE and A_L PROBE.

Step 3. B PROBE.

Step 4. C PROBE which sets the Initiate A Left flip-flop to "1".

These steps perform a basic subtraction unit operation, subtracting X from A.

2. A NEGATIVE, X NEGATIVE. - If $A_{71} = 1$ and $X_{35} = 1$, the INITIATE DIVIDE signal sets the Initiate Divide, Divide Case, and Delayed Add flip-flops to "1". The resulting sequence of probes are produced in ASC:

Step 1. "1" FROM DELAYED ADD, which produces $X' \rightarrow A_R$.

Step 2. A_R PROBE.

Step 3. B PROBE.

Step 4. C PROBE, which sets the Initiate A Left flip-flop to "1".

These steps perform a basic addition unit operation, adding X to A.

3. A POSITIVE. - If $A_{71} = 0$, the INITIATE DIVIDE signal sets the Divide Case flip-flop to "0", and the Initiate Divide and Initiate A Left flip-flops to "1". Thus, initial corrections are made on (A).

(b) THE INITIAL SHIFT. - To position the divisor for the first addition or subtraction, either the first C PROBE (if $A_{71} = 1$) or the INITIATE DIVIDE (if $A_{71} = 0$) sets the Initiate A Left flip-flop to "1".

When this is done, CONTROLLED CLOCK PULSES pass through a gate V06-10044. Each pulse produces AL1 (Shift A Left 1) and SHIFT A OR Q. Each AL1 signal shifts (A) left by one place. Each SHIFT A OR Q signal backs SK, and probes an SKC gate enabled by SK = 1. Because SK is set to 36 before the ASC Divide Sequence is started, the 36th SHIFT A OR Q signal finds the SK = 1 gate enabled, and produces an END SHIFT signal. The END SHIFT signal clears the Initiate A Left flip-flop to "0", sets the Divide Sequence and Divide Step flip-flops to "1", and produces SET SK TO 36. These operations prepare ASC for the division operation.

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It is of interest to note that after the initial shift, the most significant bit of A is in the A_{35} position.

(c) THE DIVISION. - When the Divide Sequence and Divide Step flip-flops are both set to "1", a basic "division step" is performed 36 times. Each "division step" shifts A left one place, compares A_{35} and X_{35}, either adds or subtracts X from A, inserts a "1" into Q_0 if a subtraction has taken place, and shifts Q left by one place.

Each subtraction or addition from A is performed in a manner such that stage A_{35} can always be used to determine the sign of the dividend in A.

1. $A_{35} = X_{35}$. - If A and X are of the same sign, a division step consists of the following sequence of signals:

Step 1. "1" FROM DIVIDE STEP, which produces COMPLEMENT X, SET Q_0 to 1, and BACK SK, sets the Restore X and Delayed Add flip-flops to "1", and clears the Divide Step flip-flop to "0".

Step 2. "1" FROM DELAYED ADD, which produces X'—A_R (and A_L INPUT if X is positive).

Step 3. A_R PROBE (and A_L PROBE if X is positive).

Step 4. B PROBE, which sets the C Probe flip-flop to "1" unless SK is equal to 0.

Step 5. C PROBE, which resets the Divide Step flip-flop to "1" if SK is not equal to 0, and produces SHIFT $Q_0 - Q_{34}$ LEFT 1, and Q_{35}—Q_0.

Steps 1 through 5 effectively perform a basic subtraction operation to subtract X from A, and register a "1" in Q to denote that a subtraction has occurred.

2. $A_{35} \neq X_{35}$. - If A and X are different in sign, a division step consists of a sequence similar to the steps listed for $A_{35} = X_{35}$, except that in step 1, the Restore X flip-flop is not set to "1", and COMPLEMENT X and SET Q_0 TO 1 are not produced. As a result, steps 1 through 5 effectively perform a basic addition operation, adding X to A and effectively registering "0" in Q.

3. DIVISION CHECKS. - Two division checks are made during the division phase. These division checks are intended to terminate any attempted division involving a quotient larger than the capacity of Q.

a. After one sequence of steps based on a comparison of A_{35} and X_{35} is carried out, A_{35} and A_{36} are compared: if the condition $A_{35} \neq A_{36}$ is detected, a DIVIDE CHECK STOP is produced; if the condition $A_{35} = A_{36}$ is detected, the second sequence of steps based on a comparison of A_{35} and X_{35} is carried out, and division continues.

b. If the condition $Q_0 = Q_1$ is detected after the second sequence of steps is completed, a DIVIDE CHECK STOP is produced; if the condition $Q_0 \neq Q_1$ is detected, the division continues.

(d) THE END CORRECTION. - After the 36 sequences of "division steps" are completed so that SK = 0, the E Probe flip-flop is set to "1", and Extend Sequence is set to "0". The resulting E PROBE initiates a sequence which performs the end correction, if necessary, and terminates the ASC/SKC Divide Sequence. The possible end corrections and the conditions under which each is carried out are listed below:

a. If $A_{36} = 1$, either of the following steps is performed:

1. If the divisor is positive ($X_{35} = 0$), the E PROBE initiates a basic adding sequence which adds the divisor to (A).

2. If the divisor is negative ($X_{35} = 1$), the E PROBE initiates a basic subtractive sequence which subtracts the divisor from (A).

b. If $A_{36} = 1$ and the dividend was positive (Divide Case ="0"), or if $A_{36} = 0$ and the dividend was negative (Divide Case = "1"), the signal $Q35 \rightarrow Q_0$ alters the contents of Q_0 to agree with the contents of Q_{35}.

(e) EXAMPLES. - Three examples of division are given below for hypothetical four-bit Q and X registers, and an eight-bit A.

Example 13: Divide

Dividend:	0000	1101 (+13)
Divisor:		0100 (+ 4)
Quotient:		0011 (+ 3)
Remainder:	0000	0001 (+ 1)

	(A_L)	(A_R)	(X)	(Q)	(SK)
Initial Conditions:	0000	1101	0100	0000	4
1. ($A_7 = 0$, SK ≠ 1)					
ALl	0001	1010			
BACK SK					3
2. (SK ≠ 1)					
ALl	0011	0100			
BACK SK					2
3. (SK ≠ 1)					
ALl	0110	1000			
BACK SK					1
4. (SK = 1)					
ALl	1101	0000			
BACK SK					0
SET SK TO 4					4

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Example 13: (cont'd)	(A_L)	(A_R)	(X)	(Q)	(SK)
5. ($A_3 = X_3$)					
1st Divide Check II					
(no effect)					
AL1	1010	0001			
BACK SK					3
SET Q_0 TO 1				0001	
COMPLEMENT X			1011		
(X NEG)					
$X' \rightarrow A_R$	1010	0101			
A_R PROBE	1010	0101			
	1001	1101			
(EXT SEQ = 1,					
REST X = 1)					
COMPLEMENT X			0100		
(DIV SEQ = 1,					
SK $\neq$ 0)					
1st DIVIDE Check I					
(preparatory)					
QL1				0010	
6. ($A_3 \neq X_3$)	1001	1101	0100	0010	3
2nd Divide Check II	Since $A_3 = A4$, division can continue				
AL1	0011	1011			
BACK SK					2
(X POS)					
$X' \rightarrow A_R$	1100	0000			
A_L INPUT					
A_R PROBE	1100	0000			
A_L PROBE					
	0011	1111			
(EXT SEQ = 1,					
RES X = 0,					
DIV SEQ = 1					
SK $\neq$ 0)					
2nd Divide Check I	Since $Q_0 \neq Q_1$, division can continue				
QL1				0100	
7. ($A_3 \neq X_3$)	0011	1111	0100	0100	2
AL1	0111	1110			
BACK SK					1
(X POS)					
$X' \rightarrow A_R$	1000	0101			
A_L INPUT					
A_R PROBE	1000	0101			
A_L PROBE					
	1000	0010			
(EXT SEQ = 1,					
REST X = 0,					
DIV SEQ = 1,					
SK $\neq$ 0)					
QL1				1000	

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Example 13 (cont'd):	(A_L)	(A_R)	(X)	(Q)	(SK)
8. $(A_3 = X_3)$	1000	0010	0100	1000	1
AL1	0000	0101			
BACK SK					0
SET Q_0 TO 1				1001	
COMPLEMENT X			1011		
(X NEG)					
$X' \rightarrow A_R$	0000	0001			
A_R PROBE	0000	0001			
(EXT SEQ = 1,					
REST X = 1)					
COMPLEMENT X			0100		
(DIV SEQ = 1,					
SK = 0					
QL1				0011	
$(A_4 = 0$					
DIV CASE = 0)					
ASC RESUME					

Example 14: Divide

Dividend: 11100001 = -30
Divisor: 1000 = - 7
Quotient: 0101 = + 5
Remainder: 00000101 = + 5

	(A_L)	(A_R)	(X)	(Q)	(SK)
Initial Conditions:	1110	0001	1000	0000	4
1. $(A_7 = 1,$					
$X_3 = 1)$					
Initial Correction					
ADD X TO A	1101	1010			
2. Initial Shift					
$(AL_1$ four places)	1010	1101			0
BACK SK to 0,					
then reset SK TO 4					4
3. Division	1010	1101	1000	0000	4
$(A_2 = X_3)$					
ALI	0101	1011			
BACK SK					3
SET Q_0 TO 1				0001	
SUBT X FROM A	0110	0010			
QL1				0010	
$(A_3 \neq X_3)$					
Divide Check	Since $A_3 = A_4$, division can continue				
AL1	1100	0100			
BACK SK					2
ADD X TO A	1011	1101			

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Example 14: (cont'd)	(A_L)	(A_R)	(X)	(Q)	(SK)
DIVIDE CHECK	Since $Q_0 \neq Q_1$ division can continue				
QL1				0100	
$(A_3 = X_3)$					
AL1	0111	1011			
BACK SK					1
SET Q_0 TO 1				0101	
SUBT X FROM A	1000	0010			
QL1				1010	
$(A_3 \neq X_3)$					
AL1	0000	0101			
BACK SK					0
ADD X TO A	1111	0101			
(SK = 0)					
QL1				0101	

Example 15: Divide (Improper)

Dividend:	11100010	(-29)
Divisor:	1011	(- 4)
Quotient:	01000	(+8, exceeds capacity of Q)
Remainder:	00000011	(+ 3)

	(A_L)	(A_R)	(X)	(Q)	(SK)
Initial Conditions	1110	0010	1011	0000	4
1. $(A_7 = 1, X_3 = 1)$ Initial Correction					
ADD X TO A	1101	1110			
2. Initial Shift					
(AL, four places)	1110	1101			
BACK SK TO 0					0
then reset SK					
TO 4					4
3. Division					
$(A_3 = X_3)$					
AL1	1101	1011	1011	0000	4
BACK SK					3
SET Q_0 TO 1				0001	
SUBT X FROM A	1101	1111			
QL1				0010	
$(A_3 = X_3)$					
Divide Check	Since $A_3 = A_4$, division can continue				
AL1	1011	1111			
BACK SK					2
SET Q_0 TO 1				0011	
SUBT X FROM A	1100	0011			
Divide Check	Since $Q_0 = Q_1$, DIVIDE CHECK STOP				
QL1	1100	0011	1011	0110	2

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8. INPUT AND OUTPUT SECTION

a. GENERAL. - The Input and Output Section contains the following systems: (1) the Typewriter System which provides a printed output, and an optional paper tape output punched in typewriter code; (2) the High-Speed Punch system which provides a seven-level punched paper tape output; (3) the IOB-IOA System which provides means of connecting a variety of optional input and output devices to the 1103 Computer System; and (4) the Photoelectric Tape Reader, which provides means of loading data punched on seven-level paper tape. The Photoelectric Tape Reader is similar to an optional input device in that it communicates via IOA and IOB; however, the control circuitry for the Photoelectric Tape Reader is an integral part of the 1103 Computer System.

b. TYPEWRITER SYSTEM. - The Typewriter (TWP), the Typewriter Register (TWR), and the Typewriter Control (TWC) form a system that produces typewritten output information at the rate of eight characters per second. The system is shown on the Block Diagram, Input and Output Systems, in Envelope #1 of Volume 7. To reproduce binary values as letters or figures on a printed page, the computer program converts the binary information into a typewriter input code and then produces Print (61-v) instructions, causing the typewriter to perform the appropriate functions. A wide selection of letters or figures may be used to represent the stored information.

(1) TYPEWRITER. - A Commercial Controls Corporation model FL Flexowriter (Recorder-Reproducer), with a modified keyboard, is used as the output typewriter. Under computer operation the typewriter is capable of printing eight characters per second. During computer operation, the typewriter can be operated either manually from the keyboard, or remotely by the computer. The typewriter power switch, located to the right of the keyboard, must be ON for both manual and computer operation of the typewriter. While the computer is operating, care must be used not to jam the keys when the typewriter is operated manually.

The typewriter internal wiring has been modified to permit the energizing of the Code Translator solenoids from the Typewriter Register relays, and to permit the operating of a part of the typewriter tape reader circuit from the computer. As a result of the wiring change the tape reader is de-activated. However, the typewriter six-level tape punch is not affected, and if the PUNCH switch is depressed the punch will operate to punch tape in Flexowriter code for all operations performed by the typewriter, whether done manually or under computer control. No provision is made for locking-out the manual keyboard.

All the characters and functions are produced by six-bit function codes received from the computer via TWR. The position of the carriage for upper or lower case characters is determined by Shift Up or Shift Down functions. To set the carriage to the upper case position from the lower case position, a Shift Up function must be executed. The carriage then remains in this position until a Shift Down function is executed. The same is true if the carriage is to be set to the lower case position from the upper case position. If it is desired to produce a single upper case character, the computer program must initiate a Shift Up function, if the carriage is not already up, then a character

function, and then a Shift Down function. The Tab function, when executed, causes the carriage to advance until a tabulated character position is reached. Before the equipment is operated the operator must set the desired tab positions on the tab rack located on the back of the typewriter carriage. Execution of the Carriage Return function causes the typewriter to return to the left margin of the page and the roll of paper to advance. Before equipment operation, the operator must select the desired line spacing with the line space lever located on the left hand side of the typewriter carriage.

During each Print instruction, the typewriter code for the operation to be performed is sent to the Typewriter Register and thence to the typewriter by means of contacts of the TWR relays connected in series with the Code Translator Solenoids, L_{T1} through L_{T6}. The X → TWR AND INITIATE PRINT command from CTC fires a thyratron relay puller, which in turn energizes the Reader Clutch, L_{RC}, located in the typewriter. When energized, the Reader Clutch unlatches a stop within the typewriter and allows a typewriter cycle to be initiated.

This cycle, once initiated, proceeds under its own control and results in the completion of a typewriter operation as determined by the condition of the Code Translator Solenoids. This cycle is prevented from being repeated continuously by the Typewriter Control Circuit, which de-energizes the Reader Clutch before another cycle can be started, thus releasing a latch to provide a mechanical stop. Therefore, only one cycle occurs for each X → TWR AND INITIATE PRINT command from CTC.

A short time after the initiation of the typewriter cycle, the Reader Common Contacts close and complete a common ground circuit. This results in the energizing of the Translator Clutch (L_{TC}), the appropriate Code Translator Solenoids, the Enable Impossible Print relay (K26102), and the Character Acknowledge relay (K26103). The latter two relays are part of the Typewriter Control circuit, and their function is explained in Subparagraph (3) below.

When the Translator Clutch and the Code Translator Solenoids are energized, the typewriter performs the appropriate operation. Later in the cycle the Reader Common Contacts open and de-energize the previously-energized solenoids and relays. Prior to this, the Reader Clutch has been de-energized to prevent the start of another cycle.

During the execution of a Carriage Return function, the Carriage Return contacts open and remain open until the carriage has been completely respositioned. These contacts are used in the Typewriter Control circuit to prevent the execution of another Print instruction until a previously initiated Carriage Return or Tab function has been completed.

If the Typewriter Register holds a code for which the typewriter has no corresponding function, the typewriter cycle proceeds normally but no operation is performed. However, the Typewriter Control circuit detects this condition and produces an A Fault in the computer. The valid typewriter function codes are listed in Appendix B of this volume under the Typewriter Sequence heading.

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(2) TYPEWRITER REGISTER. - The Typewriter Register (TWR) is composed of six thyratron relay pullers (TWR_0 through TWR_5) and their associated relays

(K30064 through K30069), which temporarily store a six-bit function code that determines the particular typewriter function that is to be performed.

During a Print instruction, enables from the "1" side of the six lower-order stages of X (X_0 through X_5) are sent to the corresponding stages in TWR. The X → TWR AND INITIATE PRINT command from CTC fires those thyratrons which received "1" enables from X, and they in turn cause the appropriate TWR relays to be energized. The particular TWR relays which are energized close contacts in the circuits of the appropriate Code Translator Solenoids (L_{T1} through L_{T6}) located in the typewriter, and thus determine the typewriter function to be performed. Contacts of the energized TWR relays also complete circuits to relays in the Impossible Print and Function Translator.

During the typewriter sequence, TWR is cleared by the de-energizing of the normally-energized Acknowledge I and II relays (K26104 and K26105) respectively, which momentarily remove positive voltage to TWR, and thus extinguish the TWR thyratrons and de-energize the TWR relays. The register is thus prepared to receive new information when the next X → TWR AND INITIATE PRINT command is received from CTC.

The register can be manually cleared from the Supervisory Control Panel when the computer is not operating, i.e., when the OPERATING indicator is extinguished, by selecting TEST and depressing the white button located directly beneath the TWR indicators on the right-hand side of the panel. Depressing the button energizes the Clear HPR-TWR relay K30073 and opens a set of contacts in the positive voltage supply to the register.

The Typewriter Register is also cleared by a MASTER CLEAR signal which is produced when a start selection is made in the START SELECTION GROUP on the Supervisory Control Panel.

(3) TYPEWRITER CONTROL. - Typewriter Control (TWC) functions to load and operate the typewriter, to prevent execution of another printing operation until the current operation has been completed, and to produce an A Fault in the computer if the Typewriter Register holds a code for which the typewriter has no corresponding operation, i.e., an Impossible Print code.

During the execution of the Print (61-v) instruction, the X → TWR AND INITIATE PRINT command from CTC transfers the contents of X_0 through X_5 to TWR and energizes the Reader Clutch to initiate the typewriter cycle. Contacts of the TWR relays energize the Impossible Print and Function Translator relays, K26107 through K26113, such that the code held in TWR is duplicated in the translator.

If a Carriage Return or Tab function is to be executed, the Function Relay K26101 is energized through the relay contact "translator tree" circuit. Function relay K26101 holds-in through its own closed contacts and the closed Carriage Return Contacts. Contacts of K26101 also break the TWC RESUME circuit and prevent a Resume signal being sent before K26101 de-energizes.

When the Reader Common Contacts close during the typewriter cycle, the Character Acknowledge relay K26103 and the Enable Impossible Print relay K26102 are energized.

The energizing of K26103 opens the ground circuit of Acknowledge I relay,

which then de-energizes and in turn de-energizes Acknowledge II relay K26105.

Positive voltage to the Typewriter Register and the Reader Clutch is supplied through closed contacts of K26104, which is normally energized. When K26104 is de-energized, these contacts open and remove positive voltage, thus clearing TWR by extinguishing the thyratrons and de-energizing the TWR relays, and preventing the start of another cycle by extinguishing the Reader Clutch. Contacts of K26105 in parallel with the contacts of K26104 will close when K26105 is de-energized and again will complete the voltage circuit. However, the transition period between the switching of the contacts is sufficient to clear TWR and de-energize the Reader Clutch.

Contacts of K26102, when energized, complete the circuit of the Impossible Print relay K26106 to the translator. If an Impossible Print code is held in TWR, the translator furnishes ground potential to energize K26106. When K26106 is energized, it holds in, opens the circuit to de-energize the Reader Clutch, closes contacts to provide an Impossible Print Enable to the Fault Detector to register an A Fault which stops the computer, and furnishes ground potential to energize and hold K26104. Relay K26104 is held in to prevent the clearing of TWR and the production of the TWC RESUME signal.

The A Fault can be cleared by depressing the Clear A Fault button on the Supervisory Control Panel. This energizes K30037, which opens contacts to de-energize K26104, K26105, and K26106. When K26105 is de-energized, it clears TWR, which in turn de-energizes the Translator relays, thus opening the circuit to K26106. When the cycle is well underway, K26104 is energized through closed contacts of K26103 and through the closed Carriage Return Contacts. The closing of a set of K26104 contacts in the TWC RESUME circuit fires the thyratron single-pulse generator which sends a TWC RESUME signal to PDC. In PDC, this signal removes a lockout enable and permits another Print instruction to be executed.

When a valid code is held in TWR, the opening of the Reader Common contacts de-energizes K26102 and K26103. Relay K26104 then energizes through closed contacts of K26103 and the closed Carriage Return Contacts and results in the transmission of the TWC RESUME signal to PDC.

If a Carriage Return or Tab function is being executed, the Carriage Return Contacts open when the carriage is being repositioned, and open the ground circuit to K26104. This may occur after K26103 is de-energized; i.e., K26104 may be re-energized, before the Carriage Contacts close, and close a set of contacts in the Resume circuit. However, K26101, previously energized through the translator, holds-in through the Carriage Return contacts and its contacts open the Resume circuit.

When the carriage has been repositioned, the Carriage Return Contacts again close, energizing K26104, which then results in a TWC RESUME signal to PDC.

The typewriter code and the typewriter sequence are shown in tabular form in Appendix B of this volume, under the Typewriter Sequence heading.

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c. HIGH-SPEED PUNCH SYSTEM. - The high-speed punch (HSP), the high-speed punch register (HPR), and the high-speed punch control (HPC) form a system that produces punched tape output information at the rate of sixty frames per second. (See Block Diagram, Input and Output systems, Envelope #1, Volume 7.)

The high-speed punch uses standard seven level paper tape, and is capable of reproducing six binary bits and an optional seventh level per frame. An entire thirty-six bit word from storage may be punched on six consecutive frames of the tape. To punch tape, the computer program produces Punch (63jv) instructions to reproduce information stored at any storage location onto the punched paper tape. Each Punch instruction causes up to six data holes to be punched in one frame, and causes a seventh-level "control" hole to be punched if the value j in the Punch instruction word is equal to 1, i.e., if UAK_{12} = "1".

(1) HIGH-SPEED PUNCH. - A Teletype Corporation code BRPE2 seven-level high-speed punch (HSP) is used to produce the punched tape output. The power switch located on the front of the punch must be set to the ON position to permit punch operation.

In the punch, a fast operational rate of sixty frames per second is possible because the majority of the moving parts are kept continuously in motion when the power switch is on. A continuously rotating drive shaft oscillates an eccentric drive lever. Each time the lever is driven through an oscillation, a punch pin is driven through the tape to produce a sprocket hole, and a set of "Sync" contacts are closed and then opened. Each of seven Tape Level solenoids, when energized, allows the eccentric drive mechanism to operate one of the seven tape level punch pins. A Tape Feed solenoid, when energized, allows the eccentric drive to advance the tape.

During each Punch (63jv) instruction, a SYNC signal produced by the momentarily-closed Sync contact is used to synchronize the energizing of the solenoids to the motion of the eccentric drive. The SYNC signal triggers thyratrons of the High-Speed Punch Control circuitry so that the desired information is transmitted into the Tape Level solenoids and the Tape Feed solenoid from HPR during the initial portion of the punch oscillation period. The energizing of the appropriate Tape Level solenoids and the Tape Feed solenoid causes the eccentric drive to punch the information in the tape and to advance the tape by one frame.

(2) HIGH-SPEED PUNCH REGISTER. - The High-Speed Punch Register (HPR) is a seven-stage thyratron register (HPR_0 through HPR_6) which temporarily stores digits to be punched on the paper tape.

During a Punch (63jv) instruction, "1" enables from the six lower-order stages of X are sent to the corresponding stages in HPR, and if j equals 1, a "1" enable from UAK_{12} is sent to HPR_6. The contents of HPR_0 through HPR_5 determine the punching of the six information levels on the tape while the contents of HPR_6 determine the punching of the seventh level. The X → HPR AND INITIATE PUNCH command from CTC fires those HPR thyratrons which have received enables from X and UAK. The fired thyratrons then provide enables for thyratron relay pullers. The next SYNC pulse received from High-Speed Punch Control fires the enabled relay pullers and clears the High-Speed Punch Register by applying a negative-going 2.5 millisecond pulse to the HPR thyratrons, thus extinguishing

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them. The register is thus prepared to receive new information when the next X → HPR AND INITIATE PUNCH command is received from CTC.

The register can be manually cleared from the Supervisory Control Panel when the computer is not OPERATING, i.e., when the OPERATING indicator is extinguished, by selecting TEST and then depressing the white button located directly beneath the TWR indicators on the right-hand side of the panel. Depressing the button energizes the Clear HPR-TWR relay K30073 and opens a set of contacts in the voltage supply to the register.

The HPR register is also cleared by a MASTER CLEAR signal, which is produced when a start selection is made in the START SELECTION GROUP on the Supervisory Control Panel.

(3) HIGH-SPEED PUNCH CONTROL. - The High-Speed Punch Control (HPC) loads and operates the High-Speed Punch and sends an HPC RESUME signal to PDC when the punching operation has been started.

During the execution of the Punch (63jv) instruction, the X → HPR AND INITIATE PUNCH command from CTC transmits the contents of UAK_{12} and the six lower-order stages of X to the High-Speed Punch Register, and sets the Init. HS Punch flip-flop to "1", which in turn enables a thyratron gate circuit. During the next oscillation of the punch eccentric drive mechanism, the closing of the Sync contacts generates a SYNC pulse that fires the previously enabled thyratron gate. The output of this gate fires thyratron relay pullers enabled from the High-Speed Punch Register. In addition, the High-Speed Punch Register is cleared to "0", the HPC Resume flip-flop is set to "1", and the Init. HS Punch flip-flop is cleared to "0". The firing of the thyratron relay pullers energizes the Tape Feed solenoid and the appropriate Tape level solenoids. As a result, the content of the High-Speed Punch register is punched on the tape and the tape is advanced. The opening of the Sync contacts produces a pulse from a "NOT" circuit. This pulse passes through the gate enabled by the "1" side of the HPC Resume flip-flop, clears the HPC Resume flip-flop, and sends an HPC RESUME signal to PDC. This resume signal removes an external lockout condition in PDC so that another Punch instruction may be executed.

The detailed sequence of operations initiated by the X → HPR and INITIATE PUNCH commands is shown in tabular form in Appendix B of this volume under the High-Speed Punch Sequence heading.

d. IOB-IOA SYSTEM. - IOB and IOA are shown in the Block Diagram, Input-Output Registers, in Envelope #1 of Volume 7. In both of these registers, each stage consists of two flip-flops with associated Input-Output circuits. Both registers function only as buffer storage registers and therefore do not have shifting or counting properties.

The required INPUT signal to each stage from the external equipment control is a short duration "1" pulse similar to the standard one-half microsecond pulse used in the computer. A pulse of either positive or negative polarity and reasonable bias level may be employed, because transformer inputs are provided.

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The output to the external equipment control from each stage is a WRITE enable applied through a cathode follower. When the stage is set to "1", the WRITE output voltage is from +5 vdc to +15 vdc, and when the stage is set to "0" the WRITE voltage output is from -20 vdc to -30 vdc. Each WRITE output can supply up to 18 milliamperes to the external equipment control when a "1" is stored in the IOA or IOB stage.

(1) IOB REGISTER. - The IOB Register is used not only to receive and supply data from the external equipment, but also to supply SELECT enables used to control the mode of operation of the external equipment. During the execution of the External Function (17-v) instruction, IOB receives a 36-bit "code word" from storage address v via X. When one or more types of external equipment are used, the code word selects the proper one for operation. Several code words, each producing a different mode of external equipment operation, may be used for controlling each unit of external equipment.

During the External Function instruction, the X → IOB command is produced on MP 5. Because the MCT 17 enable is present, the X → IOB signal not only transmits the code word to IOB, but also sets the Select flip-flop to "1". The resulting SELECT SYNC enable is applied to "AND" circuits connected to the 36 IOB stages. Each stage that stores a "1" produces an IOB SELECT enable for the external equipment control. The SELECT SYNC enable is available for use in the external equipment control, if necessary. When the mode selection operation has been completed, a CLEAR IOB signal from the external equipment clears the IOB register to all zeros.

During the execution of the External Write (77jv) instruction, IOB is used to transmit data to the external equipment if the value j is equal to 1. The X → IOB command is received on MP 5. Because the MCT 77 enable is present, this command not only transmits (X) to IOB, but also sets the IOB Write flip-flop to "1". The resulting IOB WRITE SYNC enable is sent to the external equipment control, where it may be used to initiate a writing sequence. The IOB WRITE SYNC enable is applied to "AND" circuits connected to the 36 IOB stages, so that each stage containing a "1" produces an IOB WRITE enable for the external equipment control. After the writing operation has been completed, a CLEAR IOB signal from the external equipment control clears the IOB register.

During the execution of the External Read (76jv) instruction, IOB is used to receive data from the external equipment if the value j is equal to 1. IOB initially contains all zeros, which is due either to a MASTER CLEAR signal or to a CLEAR IOB signal produced by a previous instruction involving IOB. On MP 1, a lockout condition test is initiated so that MPD does not advance to produce MP 5 unless a reading operation to IOB has been performed by the external equipment. If the reading operation has been completed, each "1" signal received via one of the 36 INPUT IOB lines will have set one stage of IOB to "1", and an IOB RESUME signal (not shown on IOB Block Diagram) from the external equipment control will have permitted MPD to be advanced. On MP 5, IOB → X and CLEAR IOB commands transmit the word in IOB to the X register and clear IOB to all zeros.

(2) IOA REGISTER. - No "select" feature is incorporated into IOA. This register supplies eight stages for writing into or reading from optional equipment. In addition, IOA stages 0 through 6 provide means of accepting the seven tape levels of information from the Photoelectric Tape Reader.

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During the execution of an External Write (77jv) instruction, IOA is used if the value j is equal to 0. The X → IOA command is received on MP 5. This command not only transmits (X) to IOA, but also sets the IOA Write flip-flop to "1". The resulting IOA WRITE SYNC enable is applied to "AND" circuits connected to the eight IOA stages, so that each stage containing a "1" produces an IOA WRITE enable for the external equipment control. The IOA WRITE SYNC is also available for use in the external equipment, if necessary. After the writing operation has been completed, a CLEAR IOA signal from the external equipment control clears the IOA register.

During the execution of the External Read (76jv) instruction, IOA is used if the value j is equal to 0. All the IOA flip-flops are initially in the "0" state. On MP 1, a lockout condition test is initiated so that MPD does not advance to produce MP 5 unless a reading operation to IOA has been performed by the external equipment. If the reading operation has been completed, each "1" signal received will have set one stage of IOA to "1", and an IOA RESUME signal (not shown on IOA Block Diagram) from the external control will have permitted MPD to be advanced. On MP 5, IOA → X and CLEAR IOA commands transmit the contents of IOA to X and clear the IOA register.

(3) LOCKOUT CIRCUITS. - The IOA and IOB lockout circuits consist of the Wait Read IOA, Wait Write IOA, Wait Read IOB, and Wait Write IOB flip-flops. These flip-flops are shown on the Block Diagram, Master Clock and Main Pulse Distributor, in Envelope #4 of Volume 7.

(a) LOCKOUT FOR IOB. - The Wait Write IOB flip-flop is set to "1" on MP 5 of an External Write (77jv) instruction with j equal to 1, or on an External Function (17-v) instruction. After the required writing or mode selection operations have been completed in the external equipment, an IOB RESUME signal clears the Wait Write IOB flip-flop to "0".

The Wait Read IOB flip-flop is set to "1" each time an IOB READ ACKNOWLEDGE signal signifies that data has been inserted from the external equipment into IOB. This flip-flop is cleared to "0" on MP 5 of an External Read (77jv) instruction having a j value equal to 1.

If an instruction involving IOB is started before a previous IOB operation has been completed, the advancing of MPD is halted until IOB is ready for the new operation. This is accomplished as follows:

1. WRITE OR SELECT LOCKOUT. - If the current instruction is an External Function, then the MCT 17 and WAIT WRITE IOB "1" enables combine to form a WRITE IOB LOCKOUT enable. If the current instruction is an External Write with j equal to 1, the MCT 77, UAK_{12} "1", and WAIT WRITE IOB "1" enables form the WAIT WRITE IOB LOCKOUT enable. In either case, the TEST LOCKOUT signal produced on MP 1 sets the Wait External flip-flop to "1" so that MPD is stopped. When the previously-initiated IOB operation is completed, the Wait Write IOB flip-flop is cleared by the IOB RESUME signal. The resulting IOB WRITE REFERENCE enable permits the next CONTROLLED CLOCK PULSE to clear the Wait External flip-flop so that MPD is advanced by subsequent CONTROLLED CLOCK PULSES.

2. READ LOCKOUT. - If the external equipment is performing

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reading operations, each transmission into IOB is accompanied by an IOB READ ACKNOWLEDGE signal that sets the Wait Read IOB flip-flop to "1". However, if an External Read instruction with j equal to 1 is started before the IOB READ ACKNOWLEDGE is received, a READ IOB LOCKOUT enable is produced by the combined WAIT READ IOB "0", UAK_{12} "1", and MCT 76 enables. If this situation occurs, MP 1 of the current instruction produces the TEST LOCKOUT signal which sets the Wait External flip-flop to "1" so that MPD is stopped. When information is read into IOB, the IOB READ ACKNOWLEDGE signal sets the Wait Read IOB flip-flop to "1" so that an IOB READ REFERENCE enable is produced. This enable permits the next CONTROLLED CLOCK PULSE to clear the Wait External flip-flop to "0" so that MPD is restarted.

(b) LOCKOUT FOR IOA. - If an instruction involving IOA is started before a previous IOA operation has been completed, the advancing of MPD is halted until IOA is ready for the next operation.

The lockouts for the IOA write and read operations are similar to the lockouts for the corresponding IOB operations, described in the previous subparagraph.

e. PHOTOELECTRIC TAPE READER SYSTEM. - This system is the basic method of loading information into the computer. The functional components of the system are: a Ferranti tape reader and its associated circuits, and the IOA-IOB registers and their control circuits. (See Block Diagram, Input and Output Systems, Envelope #1 of Volume 7.)

A seven-level punched paper tape (see Figure 3-1 of Volume 1, and also see volume titled "ERA TAPE PREPARATION EQUIPMENT") is fed into the reader where it passes through a single reading station. All seven levels of the tape are sensed simultaneously and the information contained in each level is sent, via a control gate, to its corresponding flip-flop in IOA.

The feed holes on the tape generate feed pulses within the reader which are transmitted to the computer and serve to synchronize the actions of the computer and the reader.

(1) PHOTOELECTRIC TAPE READER. - A Ferranti High Speed Tape Reader is used as the prime input device. It is designed to utilize either 5- or 7- level tape, and will operate at speeds of up to 200 frames per second. (See Block Diagram, Input and Output Systems, Envelope #1 of Volume 7; Schematic Diagram, Ferranti Reader, Volume 15; and Instruction Manual, Ferranti High Speed Tape Reader - MK II.)

In conjunction with the reader is a Power Supply and Junction Box (26200) which supplies all power to the reader. When the reader START button is pressed, contacts of K26201 close to hold K26201 energized, and to supply 220 vac to the reader drive motor. The reader drive motor is in operation at all times after the reader START button has been pressed even though the tape may not be feeding through the reader. This motor is connected to the tape feed mechanism by a differential clutch which is operated by the computer. The tape feed mechanism of the reader has a free-running speed of 200 tape frames per second.

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A brake operated by the computer is capable of stopping the tape feed within 0.03 inches after braking commences.

The optical system is based on the principal that the light produced from an "exciter" lamp passes through holes in the tape to photocells. The reading of a single tape frame is accomplished when the tape frame passes over a tape masking plate containing holes for each tape level.

The Ferranti reader requires a program for its operation. This program, called the Ferranti Loading Routine, is normally stored at the first block of MT Unit 0 although it may be stored on the drum or on one of the other tape units. The latter two storage locations, however, have disadvantages. In the case of drum storage the routine may inadvertently be erased and, should the routine be stored on any tape unit other than MT Unit 0, a greater number of selections must be made at the Supervisory Control Panel before starting.

(2) CONTROL CIRCUITS. - Contained within the Ferranti Loading Routine are External Function instructions which place control bits in IOB. Three bits are used and appear numerically in IOB as 2^{17}, 2^{16}, and 2^{15}. They have the following functions:

2^{17} (IOB_{17} SELECT) - - - Select Tape Reader

2^{16} (IOB_{16} SELECT) - - - Start Tape Reader

2^{15} (IOB_{15} SELECT) - - - Stop Tape Reader

The "Select Tape Reader" function must appear in all operations affecting the tape reader. Thus there are the following control combinations:

Start Reader (Free Run) - 2^{17} and 2^{16}

This combination causes the reader to start and continue running, transmitting each frame of information to IOA.

Stop - 2^{17} and 2^{15}

This combination will cause the reader to stop after the next frame of information is read and transmitted to IOA.

Step Tape Reader - 2^{17}, 2^{16}, and 2^{15}

This combination will cause the reader to read and transmit to IOA the next single frame of information.

The operations are controlled by the Tape Feed and PT Stop flip-flop circuits shown in the lower right-hand corner of the Photoelectric Tape Reader Block Diagram. The sequences of operations are described below.

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(a) START READER. - If a previous "stop reader" selection has been made and the resulting "stop reader" operation has been completed, or if a MASTER CLEAR (CLEAR MAIN CONTROL) signal has been received, the Tape Feed and PT Stop flip-flops will both be in the "0" state and the output of multivibrator

V10-093 will be positive. If these conditions are fulfilled, and IOB_{17} SELECT and IOB_{16} SELECT are present, gates V15-083 and V06-083 are enabled so that the next CONTROLLED CLOCK PULSE sets the Tape Feed flip-flop to "1".

When set to "1", the Tape Feed flip-flop operates the tape reader clutch so that the tape drive mechanism drives the tape through the reading station.

The first FEED PULSE read from the tape passes through gate V07-083 to produce CLEAR IOB and IOB RESUME. These signals clear IOB to zero and clear the computer from its "lockout" condition so that additional instructions involving IOB can be executed.

(b) STOP READER. - If a previously initiated "start reader" operation has been completed the Tape Feed flip-flop will be in the "1" state, the PT Stop flip-flop will be in the "0" state, and the output of multivibrator V10-093 will be positive. If these conditions exist, and IOB_{17} SELECT and IOB_{15} SELECT are present, gate V15-083 is disabled and gates V16-083 and V06-083 are enabled. The next CONTROLLED CLOCK PULSE sets the PT Stop flip-flop to "1".

The next FEED PULSE read from the tape passes through gate V09-151 and operates the 3-millisecond delay multivibrator V10-093 to disable V06-083 so that additional CONTROLLED CLOCK PULSES are blocked. The FEED PULSE also clears the PT Stop and Tape Feed flip-flops to "0", and produces CLEAR IOB and IOB RESUME.

During the 3-millisecond delay period, the "0" enable from the Tape Feed flip-flop energizes the tape reader brake so that the tape drive mechanism stops, and the CLEAR IOB and IOB RESUME signals clear the computer so that additional instructions involving IOB can be executed. The clearing of IOB removes the IOB SELECT enables from the control circuit.

(c) STEP READER. - If a previous "stop reader" selection has been made or MASTER CLEAR has been received, the Tape Feed and PT Stop flip-flops will both be in the "0" state and the output of multi-vibrator V10-093 will be positive. If these conditions are fulfilled and IOB_{17} SELECT, IOB_{16} SELECT, and IOB_{15} SELECT are present, gates V15-083, V06-083, and V16-083 are enabled. The next CONTROLLED CLOCK PULSE sets the Tape Feed and PT Stop flip-flops both to "1". The "1" enable from the Tape Feed flip-flop energizes the reader clutch, and the tape drives through the reading station; however, the first FEED PULSE read from the tape performs "stop reader" operations similar to those explained in subparagraph (b) above, so that only one tape frame is read.

(3) PT AMPLIFIERS. - The output from the seven data levels of the tape goes to a set of PT Amplifiers. These seven amplifiers (not shown on the block diagram) are labelled PT_0 through PT_6, consecutively. They correspond to the tape levels as follows:

Tape Level 5 is PT_0 Input

Tape Level 4 is PT_1 Input

Tape Level 3 is PT_2 Input

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Tape Level 2 is PT_3 Input

Tape Level 1 is PT_4 Input

Tape Level 6 if PT_5 Input

Tape Level 7 if PT_6 Input

The purpose of the PT amplifiers is twofold; amplification, and shaping of the signal to a rectangular pulse. The output from each amplifier passes through an inverter stage and a cathode follower after which it is applied as an enabling voltage on the suppressor grid of the appropriate PT input gate. (See Figure 4-19.)

(4) FEED PULSE CIRCUITS. - The feed holes on the punched tape produce negative-going pulses (called FEED PULSES) which are continuous as long as the tape is running through the reader. These pulses are applied from the reader to a blocking oscillator called a single-pulse circuit (V05-083). The input network to the single pulse circuit is a differentiator; therefore, the circuit is triggered only when the input pulse rises in a positive direction. This produces a time delay equal to the input pulse width. Since the output from the single pulse circuit is used to sample the PT Input Gates, this time delay assures that the gates will be enabled when they are sampled (see Figure 4-19). The output from the single-pulse circuit is a positive, rectangular pulse approximately 1/4-microsecond in duration. During a "start reader", "stop reader", or "step reader" operation, the FEED PULSES are used to produce CLEAR IOB and IOB RESUME. During reading, the FEED PULSES are used to probe the PT Input Gates, to operate the Missing Feed Pulse circuit, and to produce IOA READ ACKNOWLEDGE. Each of the latter signals releases the computer from a lockout condition so that an External Read instruction can be executed to assimilate the last-read tape frame.

(5) PT INPUT GATES. - The outputs of the PT Amplifiers pass through inverters and cathode followers to the suppressor grids of the PT Input Gates, V08-083 through V14-083.

The FEED PULSES probe the PT Input Gates, so that each time a frame is read, Pulses corresponding to holes in the tape frame are sent to the lower-order seven stages of IOA. Because IOA is initially cleared, this is the equivalent of the transmission of the binary information on the tape frame to IOA_0 through IOA_6. (See Figure 4-19 for waveforms.)

(6) MISSING FEED PULSE CIRCUIT. - The Missing Feed Pulse circuit consists of three multivibrator circuits (V07-103, V03-083, and V02-083), two "and" circuits, a cathode follower circuit (V03-103), and a relay puller circuit (V01-083). The purpose of these circuits is to stop the computer by energizing the missing feed pulse relay (K30071) and thus registering a computer "B" Fault should a missing feed pulse from the reader occur. This condition produces a MISSING FP indication and a "B" FAULT indication in the Fault Indicators Group.

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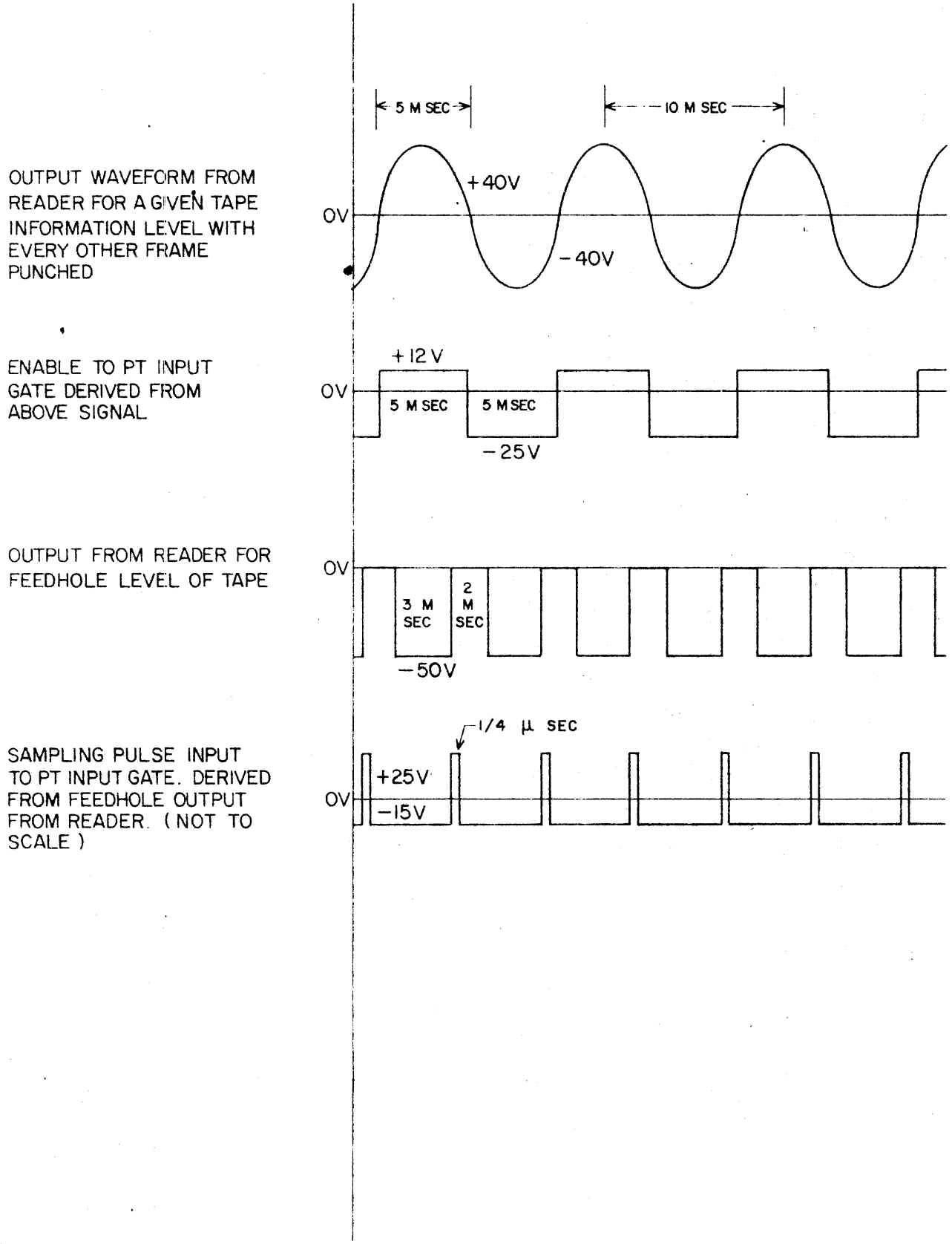

Figure 4-19. Voltage Wave forms from Ferranti Reader And Associated Circuits.

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Figure 4-20 contains a block diagram of the Missing Feed Pulse circuit and associated waveforms. The waveform drawings read from left to right and are designated by letters A through D to correspond with similar designation on the circuit drawing. The output of multivibrator V07-103 is normally positive thus keeping the "AND" circuit which it drives open. The purpose of this multivibrator is to disable the Missing Feed Pulse circuit for seven milliseconds after a reader start selection (IOB_{17} select and IOB_{16} select) has been made, thus allowing the reader tape feed mechanism to reach normal operating speed. This action is accomplished as follows: when an IOB_{17} SELECT is present, gate V06-083 is enabled so that one CONTROLLED CLOCK PULSE passes to another gate (V15-083) enabled by IOB_{16} SELECT. The pulse sets delay multivibrator V07-103. The normally positive output of this multivibrator changes and remains negative for seven milliseconds. This action disables the Missing Feed Pulse circuit for that period of time.

A reader stop selection (IOB_{17} SELECT and IOB_{15} SELECT) will also disable the Missing Feed Pulse circuit as follows: IOB_{17} SELECT enables the clock pulse gate (V06-083) allowing a CONTROLLED CLOCK PULSE through to gate V16-083, enabled by IOB_{16} SELECT. The pulse sets the PT Stop flip-flop (V83-152) to "1", which in turn applies an enable to gate V09-151. This allows the next feed pulse from the reader to set the Tape Feed flip-flop to "0", thereby removing the positive voltage from the "and" circuit that enables the screen grid of the relay puller in the Missing Feed Pulse Circuit. The Missing Feed Pulse circuit is then disabled until seven milliseconds after a reader start is selected.

During normal reader operation the output of delay multivibrator V07-103 is positive and the Tape Feed flip-flop is set to "1" causing the Missing Feed Pulse circuit to be operative.

While the reader is running, the Missing Feed Pulse circuit operates as follows: unless triggered by a feed pulse, delay multivibrator V03-083 has two stable outputs (labelled B and D; on Figure 4-20), B being positive and D negative. The output from delay multivibrator V02-083 is also stable and positive. This means that the relay puller will be energized if one or the other "AND" circuits are not blocked.

With the arrival of the first FEED PULSE from the reader, multivibrator V03-083 is triggered, causing output B to go negative and output D to go positive. Multivibrator V02-083 is not affected because the input circuit is a differentiator and the multivibrator is designed such that a voltage changing in a negative direction is required to trigger it.

Multivibrator V03-083 remains in a triggered condition for 3.5 milliseconds, after which it returns to its quiescent state. With output D changing in a negative direction, multivibrator V02-083 is triggered and its output goes negative. This action must occur simultaneously or before output B from multivibrator V03-083 goes positive so that relay puller V01-083 will not be energized. With the arrival of the next FEED PULSE multivibrator V03-083 is again triggered and the sequence described above repeats itself. It may be observed from Figure 4-20 that at no time are the control and suppressor grids of relay puller V01-083 positive at the same time unless a FEED PULSE is missing. It should be

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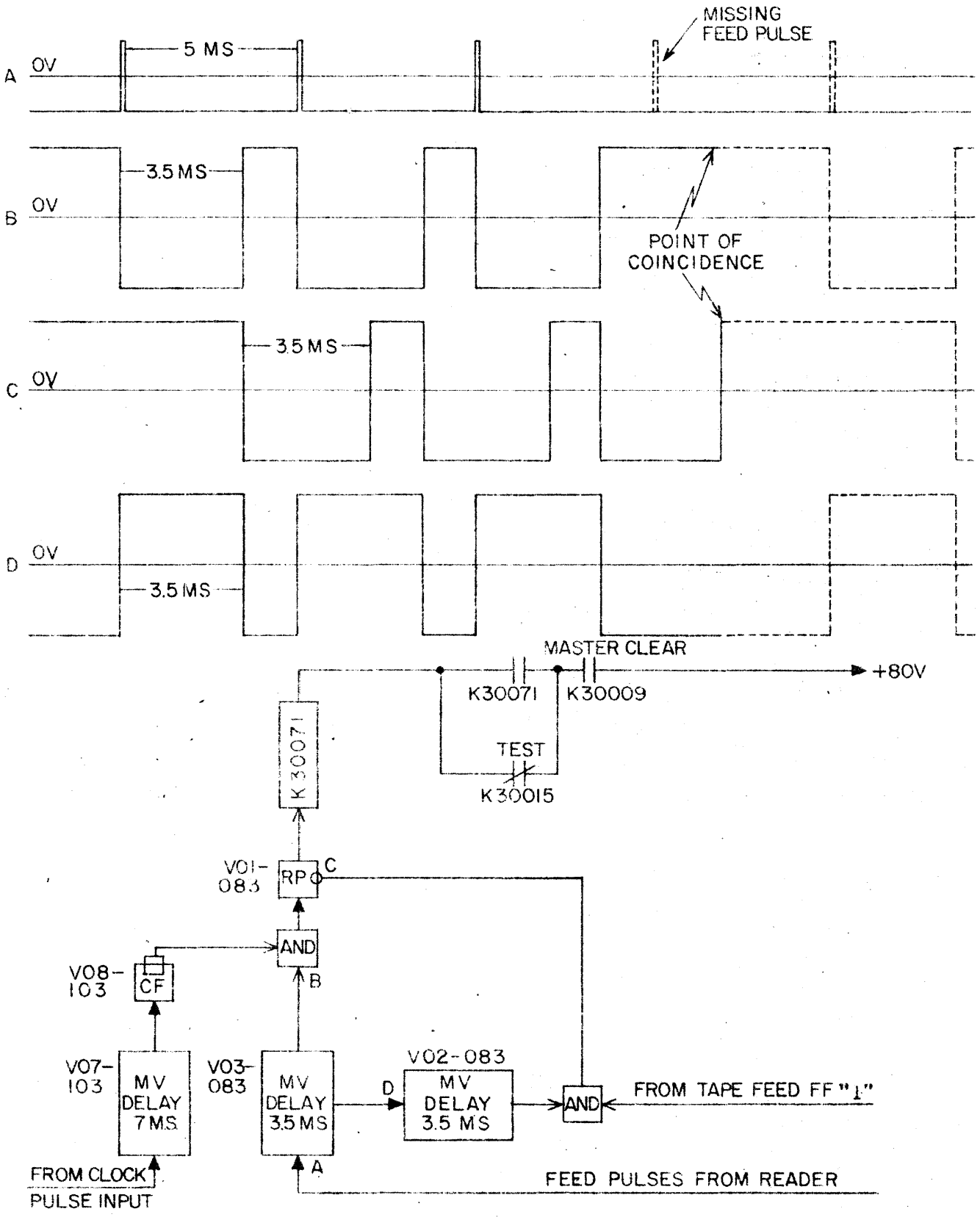

Figure 4-20 Missing Feed Pulse Circuit And Wave Forms

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noted further that once operation is started, Multivibrator V03-083 is always triggered while multivibrator V02-083 is in its triggered condition. Should a missing FEED PULSE occur, output B from multivibrator V03-083 remains positive and hence the grid of the relay puller is up. Approximately two milliseconds after the missing FEED PULSE occurs multivibrator V02-083 returns to its quiescent or positive state. Since the control grid of the relay puller is still positive, coincidence in the relay puller is reached and relay K30071 is energized. This action lights the MISSING FP indicator on the Supervisory Control panel and energizes the computer "B" FAULT relay (K30038). A "B" Fault occurs which stops the computer and the reader and lights the "B" FAULT indicator.

(7) OPERATION. - As stated previously, the Ferranti Reader requires a program for its operation. The procedures for reading a bioctal coded tape containing seventh-level loading insructions into the computer (assuming that the Ferranti Loading Routine from data handling routine of Volume 3 has been previously stored on block one of MT Unit 0) are as follows: (1) Position MT Unit 0 to the beginning of the first block; (2) place bioctal tape in the Ferranti reader and push the reader start button; (3) select MT START; (4) push the START button on the Supervisory Control Panel.

The Ferranti Loading Routine will then be transferred into rapid access storage starting with address 00000. After this has been done, the computer will take address 00000 as its next command and start the loading routine.

Tapes other than bioctal with seventh-level coding may be loaded into the computer by using a suitable Ferranti Loading Routine. Figure 4-21 shows the Ferranti Reader timing with respect to the computer. This figure may be used as an aid to programming loading routines.

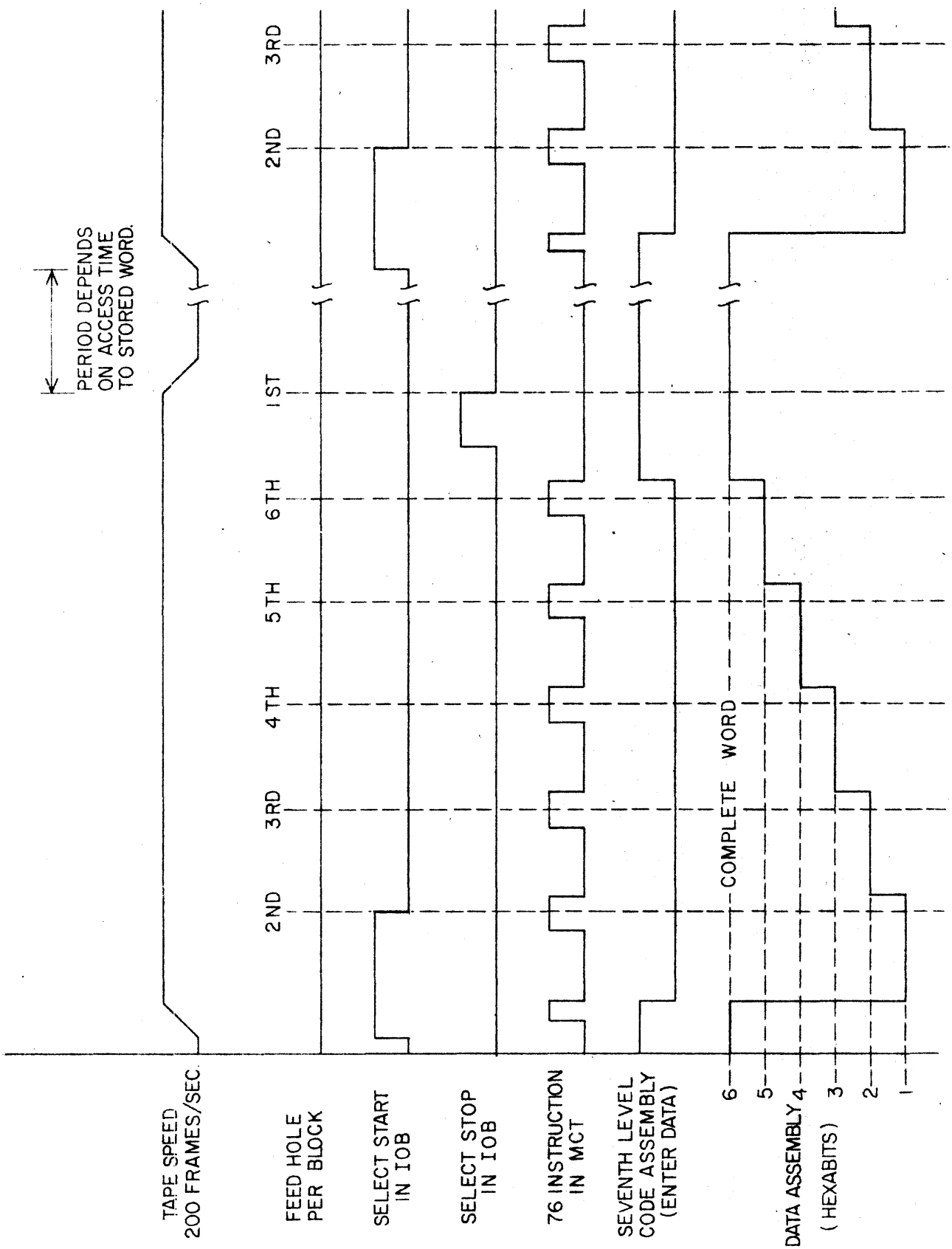

Figure 4-21 Timing Chart For Ferranti Reader Using Bioctal Tape & A Standard Loading Routine

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9. CONTROL SECTION

a. GENERAL. - The Control Section directs the operation of the entire equipment. It provides timing pulses, generates sequences of command pulses for executing the steps of each instruction, and provides the operator with means of manually controlling the mode of operation.

The principal circuits of this section are shown in block form in the lower left quarter of the Block diagram, System, in Envelope #1 of Volume 7. These circuits function to provide the 44 instruction sequences presented in tabular form in Appendix B under the Command Timing heading.

Circuits not shown specifically on the Block Diagram, System, but covered in this paragraph, include the Fault Detector, Stop Control, and Manual Controls.

b. MASTER CLOCK SYSTEM. - The Master Clock System (See Block Diagram of Master Clock, Envelope #4, Volume 7) is a collection of circuits which produce, distribute, and control the basic 500 kc timing pulses of the computer. The principal circuits of the Master Clock System are the following: the 500 kc Oscillator; the Clock Source Selector (CSS); the Clock Rate Control (CRC); and the Pulse Distributor Control (PDC).

(1) CLOCK SOURCES. - Either of the following two clock sources can provide the 500 kc CLOCK PULSES required for the operation of the computer: the Timing Pulse Multiplier (See lower right-hand corner of the Block Diagram of MD System, Envelope #2, Volume 7) or the 500 kc Oscillator (See Master Clock Block Diagram). The Timing Pulse Multiplier produces 500 kc timing pulses, called MD CLOCK PULSES, by quadrupling the 125 kc TIMING PULSES read from the drum. The Oscillator, together with its associated shaping circuit, produces 500 kc CLOCK PULSES directly. Both clock sources produce pulses which are 0.25 microsecond in width. MD CLOCK PULSES are synchronous with the MD system and can be used in all types of computer operation. The Oscillator CLOCK PULSES can be used only in the TEST mode of operation.

(2) CLOCK SOURCE SELECTOR. - The Clock Source Selector (CSS), shown on the Block Diagram of the Master Clock, in Envelope #4 of Volume 7, is composed basically of two flip-flops (CSS I and CSS II), four gates (V05, V06, V07, and V08-30092), and two relays (K30017, and K31101). In the NORMAL mode of operation the Clock Source Selector will automatically select MD CLOCK PULSES from the Timing Pulse Multiplier as the basic clock of the computer. During the TEST mode of operation, however, CSS selects the basic clock in accordance with the manual selections made on the Supervisory Control Panel. If DRUM is selected, CSS selects MD CLOCK PULSES as the basic clock; if OSCILLATOR is selected, CSS selects OSCILLATOR CLOCK PULSES as the basic clock.

In the NORMAL mode of operation, the Select Oscillator relay, K31101, is de-energized. When de-energized, K31101 closes the "1" input circuit and opens the "0" input circuit of CSS I. Regardless of the state of CSS I or CSS II at the moment K31101 is de-energized, both are eventually set to "1" as follows: (1) if CSS I is in the "0" state and CSS II is in the "1" state, the first OSCILLATOR PULSE passes through gate V05-30092 and sets CSS II to "0"; (2) when CSS I and CSS II are both in the "0" state, the next OSCILLATOR PULSE passes through gate V06-30092 and through the normally-closed contacts of K31101, and

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sets the CSS I flip-flop to "1"; (3) when CSS I is set to "1" and CSS II is set to "0", the next MD CLOCK PULSE passes through V08-30092 and sets CSS II to "1"; and (4) when CSS I and CSS II are both set to "1", the MD CLOCK PULSES pass through gate V07-30092 as computer CLOCK PULSES.

If the TEST mode is selected on the Supervisory Control Panel, the 500 kc Oscillator may be selected as a source of CLOCK PULSES. When the SELECT OSCILLATOR button is pushed, relays K30017 and K31101 are energized. This applies -30v to the zero side of CSS I and closes the "0" input circuit to CSS I. As long as this condition exists, CSS I will remain in the "0" state. Gate V05-30092 will be enabled and gate V08-30092 disabled. CSS II is set to "0" by the first OSCILLATOR pulse to occur thereafter and subsequent OSCILLATOR PULSES are gated into the equipment via gates V05-30092 and V06-30092. Releasing the OSCILLATOR selection drops the Oscillator source of CLOCK PULSES. When the RELEASE button is pushed, K31101 de-energizes so that the system reverts to the MD CLOCK PULSE source. It should be noted that switching the clock pulse source during TEST operation does not block CLOCK PULSES to the system although a two microsecond switching delay is introduced.

(3) CLOCK RATE CONTROL. - The Clock Rate Control (CRC) receives the continuous stream of CLOCK PULSES from CSS and as directed, interrupts this stream to produce controlled groups or bursts of CLOCK PULSES.

(a) NORMAL OPERATION. - During NORMAL operation, and if a MD START or MT START is selected, the burst of CONTROLLED CLOCK PULSES is continuous from the START signal to the STOP signal, being interrupted only to introduce a two microsecond delay in two machine operations; INITIATE 75 SEQUENCE and TRANSMIT X TO PCR. The START signal is produced by pressing the START button which momentarily grounds the shaper V01-30102, producing a single pulse which sets CRC I to "0", completing the "AND" circuit inputs and enabling gate V04-30102. The next CLOCK PULSE sets CRC II to "0", enabling gate V03-30102 so that CONTROLLED CLOCK PULSES are emitted. CONTROLLED CLOCK PULSES are continuous until the STOP signal except for two microsecond delays which may be initiated by either INITIATE 75 SEQUENCE or TRANSMIT X TO PCR. Either of these signals set CRC II to "1". With CRC II set to "1", gate V03-30102 is disabled thus interrupting the stream of pulses. However, gate V04-30102 is enabled so that the next CLOCK PULSE returns CRC II to "0" again, enabling gate V03-30102; thus, the stream of CONTROLLED CLOCK PULSES is interrupted for a single two microsecond pulse period. CONTROLLED CLOCK PULSES continue until the STOP signal from Stop Control sets CRC I and CRC II to "1", thus disabling gates V04-30102 and V03-30102. The RESUME signals do not enter into the CRC operation during the NORMAL mode since both K31201 and K31202 remain energized, keeping the RESUME signal circuit open. These RESUME signals are significant to CRC only during the test operation and will be discussed in a subsequent subparagraph.

(b) TEST OPERATION WITH MANUAL OR AUTOMATIC STEP CLOCK. - The STEP CLOCK test procedure permits an instruction to be executed in single CLOCK

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PULSE steps. In this procedure, a single CONTROLLED CLOCK PULSE is gated from CRC each time the STEP pushbutton is pressed or each time the low-speed oscillator generates a pulse. The MANUAL STEP CLOCK selection energizes relay K30027 thus de-energizing both the Step Distributor relay K31201 and the Step Operation relay K31202. This action closes the circuit from the CRC output gate V03-30102 back to the CRC flip-flops' "1" inputs. Pressing the STEP pushbutton ground the shaper, V01-30102. The shaper then produces a single pulse which sets CRC I to "0", initiating a CRC operation. Subsequently a single CONTROLLED CLOCK PULSE from gate V03-30102 is transmitted to the equipment. This pulse also returns through the closed relay circuit and sets CRC to its initial state, CRC I "1" and CRC II "1", thus terminating the MANUAL STEP CLOCK operation. The operation is repeated for each closure of the STEP pushbutton.

The AUTOMATIC STEP CLOCK selection energizes relay K30030 which releases the Step Distributor and the Step Operation relays and energizes relay K30031. The shaper is disabled when K30031 is energized. When the START button is pressed, relay K30048 is energized and together with K30031 produces an enable for the Low-Speed Oscillator, V02-30102. The Low Speed Oscillator generates pulses at a rate which is variable between five and 35 cps and is controlled by the AUTOMATIC STEP RATE knob. Each output pulse from this oscillator initiates a CRC operation by setting CRC I to "0". As in the MANUAL STEP CLOCK operation, the CRC operation is terminated as each emitted CONTROLLED CLOCK PULSE through V03-30102 returns CRC I and CRC II to "1". The CRC operation is repeated for each low-speed oscillator pulse.

(c) TEST OPERATION WITH MANUAL STEP DISTRIBUTOR. - In the STEP DISTRIBUTOR test procedure either a single CONTROLLED CLOCK PULSE is gated from PDC to produce an ADVANCE MPD signal or a burst of CONTROLLED CLOCK PULSES is gated from CRC during the execution of a single internal or external reference. The MANUAL STEP DISTRIBUTOR selection energizes relay K30028 which releases the Step Operation relay K31202. The Step Distributor relay K31201 remains energized. This closes the circuit for the ASC RESUME, RSC RESUME, and the ADVANCE MPD signals to CRC and opens all other relay input circuits to CRC. Depressing the STEP pushbutton initiates a CRC operation, and a CONTROLLED CLOCK PULSE is transmitted by gates V03-30102, V01-30112 and V08-30112 through PDC giving rise to the ADVANCE MPD signal. This pulse is subsequently gated through the Main Pulse Distributor (MPD) and produces an MP which initiates the execution of an instruction step. If the resulting MP from MPD initiates an internal, external, or RSC reference operation, the reference will not be completed, because the ADVANCE MPD signal also returns to CRC through the closed relay circuit and sets CRC I and CRC II to "1", thus terminating the CRC operation. Termination of the CRC operation blocks the CONTROLLED CLOCK PULSES needed for the completion of the reference operation. Also, the initiation of a reference operation disables the ADVANCE MPD circuit, by disabling either V01-30112 or V08-30112 until the completion of the reference (see Subparagraph (4) below). With the ADVANCE MPD circuit disabled as a result of an initiated but incomplete reference, the next closure of the STEP pushbutton produces a burst of CONTROLLED CLOCK PULSES allowing the reference to be completed. This burst of pulses is terminated when a RESUME signal, inidicating the termination of the reference, returns to CRC through the complete relay circuit and sets CRC I and CRC II to "1". This same RESUME signal again enables the ADVANCE MPD circuit by setting the appropriate flip-flop in PDC, so that the next closure of the

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STEP pushbutton produces another ADVANCE MPD signal.

(d) TEST OPERATION FOR MANUAL OR AUTOMATIC STEP OPERATION. - The STEP OPERATION test procedure permits an instruction to be executed as a step. In this test procedure, one instruction is executed during each burst of CONTROLLED CLOCK PULSES from CRC. Either the MANUAL STEP or the AUTOMATIC STEP may be employed in this operation.

The MANUAL STEP OPERATION selection energizes relay K30029 so that the Step Distributor relay K31201 is de-energized and the Step Operation relay K31202 remains energized. This closes the circuit for MP7 from MPD to CRC and opens all other relay input circuits to CRC. Pressing the STEP pushbutton initiates a CRC operation and CONTROLLED CLOCK PULSES are subsequently transmitted to the equipment. At the end of each instruction sequence, MP7 from MPD terminates the burst of pulses by returning CRC I and CRC II to "1".

The AUTOMATIC STEP OPERATION selection energizes relay K30032 which enables the Low-Speed Oscillator, disables the MANUAL STEP circuit and releases the Step Distributor relay K31201. Each output pulse from the Low-Speed Oscillator initiates a CRC operation by setting CRC I to "0". As in the MANUAL STEP OPERATION sequence, MP7 from MPD terminates the burst of CONTROLLED CLOCK PULSES by returning CRC I and CRC II to "1". The overall effect is that the number of instructions executed per second is determined by the setting of the AUTOMATIC STEP RATE potentiometer on the Supervisory Control Panel.

(4) PULSE DISTRIBUTOR CONTROL. - The Pulse Distributor Control (PDC) controls the generation of the ADVANCE MPD signal. Since the ADVANCE MPD signal is used in MPD to produce MP's, PDC controls the timing of each MP step during the execution of an instruction; i.e., each ADVANCE MPD signal gated from PDC causes the next instruction step to be executed. If an internal storage reference, subsequence or other similar subsequence requiring a "wait" is initiated during the instruction step, an appropriate signal to PDC causes PDC to block the ADVANCE MPD signals until the subsequence is completed.

(a) CONTROL FOR START AND STOP. - PDC is enabled when the equipment is started and disabled when the equipment is stopped. When the START button is pressed on the Supervisory Control Panel, a START signal is produced. The START pulse is sent to the zero side of the Stop flip-flop, completing the "AND" circuit required to enable gate V08-30112; CONTROLLED CLOCK PULSES are then gated to MPD as ADVANCE MPD signals by V01-30112 and V08-30112. (The Wait Internal, Wait RSC, and Wait External flip-flops are cleared previously by a signal which CLEARS PDC when a Start Selection Group selection is made.) Although the ADVANCE MPD may be temporarily blocked during the operations which follow, PDC is not permanently disabled until the STOP signal from Stop Control sets Stop flip-flop to "1". This removes the Stop flip-flop "0" enable from the "AND" circuit, thus disabling gate V08-30112 until the next START signal.

(b) CONTROL FOR INTERNAL REFERENCE. - The ADVANCE MPD signal is blocked when the WAIT INTERNAL REFERENCE signal from CTC sets Wait Internal to "1" disabling gate V01-30112. The WAIT INTERNAL REFERENCE signal, simultaneous with the ADVANCE MPD signal, results from the initiation of an internal storage

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reference, as SK operation, or an ASC operation. Thus the further advance of MPD is prohibited following the initiation of an internal reference. When gate V01-30112 is disabled, MTSC CLOCK PULSES as well as CONTROLLED CLOCK PULSES to PDC are blocked. However, CONTROLLED CLOCK PULSES are transmitted to ARAC, ASC, RSC, SCC and SKC, thus permitting the completion of the internal reference. Following a WAIT INTERNAL REFERENCE signal, MPD is not advanced until a RESUME from ARAC, MC, MD, or ASC returns the Wait Internal flip-flop to "0". A RESUME signal indicates the completion of an internal reference. With the Wait Internal flip-flop in the "0" state, the execution of the instruction proceeds to the next step as the ADVANCE MPD signal is gated from PDC.

(c) CONTROL FOR REPEAT SEQUENCE. - The ADVANCE MPD pulse is blocked when the WAIT RSC signal from CTC sets the Wait RSC flip-flop to "1", rendering the "AND" circuit incomplete and disabling gate V08-30112. The WAIT RSC signal occurs on MP 5 during the execution of the Repeat instruction and during each execution of the repeated instruction. This is so that the ADVANCE MPD pulse is blocked long enough for an RSC operation. The ADVANCE MPD pulse is again generated when the RSC RESUME signal returns Wait RSC to "0". This completes the "AND" circuit inputs and again enables gate V08-30112.

(d) CONTROL FOR EXTERNAL REFERENCE. - It is necessary to stop MPD when a reference is made to an external device that either involves an operation dependent on the Arithmetic and Control systems of the computer, or involves an operation in an external device still engaged in some previously initiated operation. Specifically, MPD is stopped when a read or write reference is made to a magnetic tape unit since the completion of such operations is dependent upon the Arithmetic and Control sections of the computer; however, MPD is not stopped when a reference is made to the magnetic tape units for advancing or backing tape, or when reference is made to the typewriter, high-speed punch, or external equipment associated with IOA or IOB, unless a previous reference has been made to the same device and the previously initiated operations have not been completed.

1. LOCKOUT DURING MT REFERENCES. - The operations produced by the four Wait MT Unit j flip-flops in PDC are different, during instructions that require tape backing and advancing, from the operations produced during instructions that require tape reading or writing.

a. BACK OR ADVANCE MT. - The backing or advancing of a particular MT Unit does not require the use of the rest of the machine registers once the advancing and backing operations are started. Therefore, during the execution of these operations, the MT Lockout circuits allow the equipment program to continue, unless another reference is made to the same MT Unit before the previously initiated operation is completed. The four MT Lockout circuits each function in the same manner. As an example, the operation of the lockout circuit for MT Unit 0 is described below.

When an Advance Magnetic Tape or Back Magnetic Tape instruction (66jn- or 67jn-) is executed and j is equal to 0, a TEST LOCKOUT signal is received by PDC on MP1. If MT Unit 0 is not performing a previously initiated back or advance tape operation, the TEST LOCKOUT signal will have no effect on the Wait External flip-flop.

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On MP 5 of the current instruction sequence, an INITIATE LOCKOUT 0 MT signal is received by PDC, and the required advancing or backing operations are initiated in MT Unit 0. The INITIATE LOCKOUT 0 MT Signal sets the Wait MT Unit 0 flip-flop to "1", thereby dropping a 0 MT REFERENCE enable to CTC, so that the next instruction requiring a reference to MT Unit 0 will not be executed to completion until an 0 MT RESUME for the current operation has been received from MT Unit 0 indicating it is again free.

If another instruction involving MT Unit 0 is started before the advancing and backing of the tape has been completed, the Wait MT Unit 0 flip-flop will be in the "1" state due to the INITIATE LOCKOUT 0 MT signal which occurred on MP 5 of the previous ADVANCE or BACK 0 MT instruction. When the Wait MT Unit 0 flip-flop is set to "1" and the negative-going j = 0 and MCT 64-67 enables are present, the positive 0 MT LOCKOUT line enables gate V06-30112. On MP 1 of the current instruction, the TEST LOCKOUT signal passes through gate V06-30112 and sets the Wait External flip-flop to "1" so that MPD is stopped.

If MPD is stopped in this manner, the completion of the MT Unit 0 operations initiated by the previous instruction produces a 0 MT RESUME signal, which clears the Wait MT Unit 0 flip-flop to "0". When the Wait MT Unit 0 flip-flop is in the "0" state and the negative-going j = 0 and MCT 64-67 enables are present, the 0 MT RESUME line enables gate V04-30112 in PDC so that a 0 MT REFERENCE enable is sent to CTC. The next CONTROLLED CLOCK PULSE passes through gates V04-30112 and V03-30112 and clears the Wait External flip-flop to "0" so that MPD resumes operation. Thus the lockout is cleared and CTC prepared for another reference to MT Unit 0.

b. READ OR WRITE MT. - When reading or writing is to be performed in a particular MT unit, the MT lockout circuits stop MPD if a previous back or advance operation is in process in the same MT unit. The four MT lockout circuits each function in the same manner. As an example, the operation of the 0 MT lockout circuit is described below.

When a READ MAGNETIC TAPE or WRITE MAGNETIC TAPE instruction (64jnv or 65 jnv) is executed and j is equal to 0, a TEST LOCKOUT signal is received by PDC at MP1 and both WAIT MT READ OR WRITE and INITIATE LOCKOUT 0 MT are received on MP 5.

The TEST LOCKOUT signal performs the same functions as described in the previous subparagraph; i.e., if a previous advance or back operation has not been completed in MT Unit 0, Wait External is set to "1" and MPD stops. If this occurs, MPD resumes when 0 MT RESUME is received.

On MP 5 of the current instruction, WAIT MT READ OR WRITE sets the Wait External flip-flop to "1" so that ADVANCE MPD is blocked and MPD stops. The INITIATE LOCKOUT MT signal sets the Wait MT Unit 0 flip-flop to "1", dropping the 0 MT REFERENCE ENABLE to CTC. When the reading or writing operation has been completed, 0 MT RESUME is sent from MT Unit 0 to PDC. When the MT Unit 0 flip-flop is set to "0" by this RESUME signal, and the negative-going j = 0 and MCT 64-67 enables are present, an 0 MT RESUME enable is produced for gate V04-30112. The next CONTROLLED CLOCK PULSE passes through gates V04-30112 and V03-30112, setting the Wait External flip-flop to "0". MPD thus resumes operation

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with the O MT RESUME signal.

2. LOCKOUT DURING PRINT REFERENCES. - During the execution of a typewriter operation, the Typewriter Control (TWC) lockout circuit allows the equipment program to continue unless another reference is made to the typewriter before the previously-initiated operation is completed.

When a Print (61jv) instruction is executed, a TEST LOCKOUT signal is received by PDC on MP 1. If no previously initiated printing operation is still in process, the TEST LOCKOUT signal from the current instruction sequence has no effect on the Wait External flip-flop. On MP 2 of the current instruction, the print operation is initiated and an INITIATE LOCKOUT TWC signal sets the Wait TWC flip-flop to "1" so that the next instruction referring to the typewriter will not be executed until TWC RESUME for the current operation has been received.

If the next Print instruction is started before the previously initiated Print operation has been completed, the Wait TWC flip-flop will be in the "1" state due to the INITIATE LOCKOUT TWC signal which occurred on MP 2 of the previous instruction, and the TWC REFERENCE enable to CTC will not be present. When the Wait TWC flip-flop is set to "1" and MCT 61 (negative-going) enable is present, a TWC LOCKOUT enable is applied to gate V06-30112. On MP 1 of the current instruction sequence, the TEST LOCKOUT signal passes through this gate and sets the Wait external flip-flop to "1", stopping MPD.

If MPD is stopped in this manner, the completion of the printing operation produces a TWC RESUME signal from the typewriter, which clears the Wait TWC flip-flop in PDC. When this flip-flop is cleared, a TWC REFERENCE ENABLE is applied to V04-30112 which allows the next CONTROLLED CLOCK PULSE to pass through gates V04-30112 and V03-30112. The Wait External flip-flop is cleared to "0" and MPD resumes operation. The TWC REFERENCE enable is also sent to CTC.

3. LOCKOUT DURING HIGH-SPEED PUNCH REFERENCES. - During the execution of a high-speed punch operation, the HPC Lockout circuit allows the program to continue until another reference is made to the high-speed punch before the completion of the previously initiated operation. The operations produced by this circuit are the same as the operation of the TWC Lockout circuit described in the previous subparagraph, except that the Wait HPC flip-flop in PDC is used, and the lockout operations are performed during the Punch (63jv) instruction.

4. LOCKOUT FOR IOA AND IOB REFERENCES. - During the operation of the external input-output equipment, the Wait Read and Wait Write flip-flops for IOA and IOB operate in a manner similar to the Wait TWC and Wait HPC flip-flops described above. The operation is described in detail in Paragraph 8, Input-Output Section, in this volume.

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c. MAIN PULSE DISTRIBUTOR. - The Block Diagram, Main Pulse Distributor, is in Envelope #4 of Volume 7. All instructions are executed in either 4, 5, 6, 7, or 8 steps with the execution of each step being initiated on a different "main pulse" (MP). The Main Pulse Distributor (MPD) provides the control for selecting and generating only those MPs which are required for the execution of the

instruction. The generation of MPs is not periodical since they are produced by gating the intermittent ADVANCE MPD signals through selected MPD output gates. An MP is produced at the conclusion of each step of an instruction, thus initiating the next step of the instruction. The automatic selectivity of MPD executes each instruction in a minimum of steps. This selectivity is accomplished by combining MPD register outputs with operation code enables from the Main Control Translator. The combinations so derived provide enables for the MPD output gates. MPD is inherently an eight-pulse distributor, but, depending upon the instruction being executed, the pulse cycle may be reduced to as few as four pulses.

The MP cycles produced to execute the steps of the various instructions (indicated by operation code) are as follows:

four-pulse cycle (MP 0, MP 5, MP 6, MP 7) - for instructions 11, 13, 15, 16, 44, 45, 46, and 56;

five-pulse cycle (MP 0, MP 1, MP 5, MP 6, MP 7) - for instructios 12, 17, 31, 32, 33, 34, 47, 76, and 77;

six-pulse cycle (MP 0, MP 1, MP 2, MP 5, MP 6, MP 7) - for instructions 14, 35, 36, 51, and 54;

seven-pulse cycle (MP 0, MP 1, MP 2, MP 3, MP 5, MP 6, MP 7)- for instructions 42, 52, 53, 55, 71, 72, and 73;

eight-pulse cycle (MP 0, MP 1, MP 2, MP 3, MP 4, MP 5, MP 6, MP 7) -for instructions 21, 23, 27, 37, 41, 43, 61, 63, 64, 65, 66, 67, and 74;

special pulse cycles - for instructions 57, 75 and repeated instructions.

As each MP is produced, the MP sets the MPD register to the next MP number. That is, as MP 1 is generated, the MPD register is set to store 2; as MP 2 is generated, the register is set to store 3, etc; so that MPD functions like a counter advanced by ADVANCE MPD signals. If the operation of MPD was entirely dependent upon the number stored in the register, MPD would be a fixed, eight-cycle distributor. Thus the ADVANCE MPD signal probing the enabled MP 0 output gate (V02-30122) would generate MP 0; MP 0 would set the MPD register to store 1 and the MP 1 output gate (V05-30122) would be enabled. Following the conclusion of the instruction step initiated by MP 0, the next ADVANCE MPD signal from PDC would be gated from MPD as MP 1. This process would be cyclic, producing in turn each of the eight MPs. However, the output gates are enabled by "AND" circuits connected to the output of the MPD register and conditional MCT enables; i.e., each output gate is enabled from the output of the MPD register on the condition that the resulting MP is required in the execution of the instruction.

For example, a four-pulse cycle is required for the execution of the Transmit Positive (11uv) instruction. During the execution of this instruction MP 0 is generated when the MPD register stores 0. MP 0 sets the register to store 1.

However, the presence of the MCT 11 enable, applied through a "NOT" circuit, prohibits the MP 1 enable; thus the MP 1 output gate (V05-30122) is not enabled even though the MPD register stores 1. The absence of MP enables 0, 1, 2, 3, 4, 6, and 7 completes the "AND" circuit and produces the MP 5 enabled. This "AND" circuit is complete whenever the number in the MPD register is prohibited from producing a corresponding MP enable due to the presence of a conditioning operation code enable from MCT. When the MP 5 enable present, the next ADVANCE MPD signal is gated (through V05-30142) as MP 5. Thus, by inhibiting MP 1, the MP cycle is made to skip to MP 5, so that a four-pulse cycle (MP 0, MP 5, MP 6, MP 7) is produced.

To produce a five-pulse MP cycle a skip after the MP 1 to MP 5 is made; a six-pulse cycle requires a skip after MP 2 to MP 5; a seven-pulse cycle requires a skip after MP 3 to MP 5; and eight-pulse cycle requires no skip. Notice that only in the eight-pulse cycle is the MPD register actually set to 5, since only in this cycle is an MP 4 produced to set the register; however, the enables resulting from this setting are not used, and the MP 5 enable is derived from the absence of all other MP enables in the same manner as it is derived when a skip is required. During the execution of the Repeat (75jnw) instruction, a special pulse cycle, which excludes MP 6, is generated. Following MP 5 during the execution of the Repeat instruction, the SET MPD to 7 signal from the Repeat Sequence Control (RSC) sets the MPD register to store 7; thus MP 6 is excluded from the cycle. MP 6 is also excluded from the normal cycle during the repeated execution of any instruction. This exclusion is also controlled by the SET MPD TO 7 signal from RSC. Thus, if the normal execution of an instruction required a 5-pulse MP cycle, the repeated execution of this same instruction would be accomplished by the normal pulse cycle with MP 6 excluded. The resulting MP cycle would be MP 0, MP 1, MP 5, MP 7. During the last execution of the repeated instruction both MP 6 and MP 7 are generated, so that the normal instruction termination occurs.

The jump termination for the repeated Threshold Jump (42uv) instruction and the repeated Equality Jump (43uv) instruction requires a special MP cycle which excludes MP 0. This MP pulse cycle is generated when the SET MPD TO 1 signal, occurring after MP 5, from RSC sets the MPD register to store 1. Thus, both MP 6 and MP 7 of the final execution of the repeated Threshold Jump or repeated Equality Jump are not generated, and MP 1 is the next MP generated. This MP 1 initiates a jump termination operation. The jump termination pulse cycle so generated is MP 1, MP 2, MP 3, MP 4, MP 5, MP 6, MP 7.

(1) INITIAL SETTING OF MPD. - The manual selection of MD START results in the PRESET MD signal, which sets MPD to 6. This results in MP 6 and MP 7 being the first pulses generated. The manual selection of MT START results in the PRESET MT signal which sets MPD to "0". This results in the first MPD cycle beginning with MP 6 or MP 0.

(2) STOPPING MPD. - Any stop operation will result in the termination of the MP cycle since the STOP signal from Stop Control to PDC terminates the ADVANCE MPD signal input to MPD. During the Final Stop (57--) instruction, the MP cycle will stop after MP 0. During a Manually Selected Stop (56jv) instruction the MP cycle will stop after MP 5. The MP cycle will also stop as a result of divide faults, MCT faults, and SCC faults.

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d. PROGRAM CONTROL REGISTER. - The Program Control Register (PCR) is the name used to designate the 36 flip-flops which register an instruction word while it is being executed. PCR consists of the Main Control Register (MCR), the U-Address Counter (UAK), and the V-Address Counter (VAK). In preparation for the execution of each instruction PCR receives the instruction from internal storage via the X-Register. MCR receives the six-bit operation code; UAK receives the 15-bit "u" execution address; VAK receives the 15-bit "v" execution address. MCR stores the operation code and produces inputs to MCT. UAK and VAK store the two execution addresses u and v, respectively, and handle the "j", "n" and "k" factors of instructions. During repeat operations the execution addresses of the repeated instruction may be advanced, if so programmed, in UAK and VAK. VAK is also advanced during block transfer operations between MC and MT.

(1) MAIN CONTROL REGISTER. - The Main Control Register is shown on the Block Diagram, Main Control Translator and Main Control Register, in Envelope #4 of Volume 7. At the conclusion of each instruction operation, a new instruction is read into X, and the content of X is transmitted to PCR, which consists of MCR, UAK, and VAK. The X_{30} through X_{35} "operation code" portion of the instruction goes to MCR stages 0 through 5, respectively.

If MD START is selected, MPD is set to 6, and the first instruction is obtained from the address specified by PAK. If MT START is selected, the PRESET MT signal initially sets MCR to 64 (octal), the Read Magnetic Tape code, and sets UAK_0 to "1". This prepares the equipment for the transfer of the first block of information from MT Unit 0 to MC. Further operations after an MT START must be self-sustaining from the program contained in the block of information transferred from MT. Outputs from the "1" and "0" sides of all MCR stages go to MCT to produce the operation code enables.

(2) U-ADDRESS COUNTER. - The U-Address Counter (UAK) is shown on the Block Diagram, Address Registers, in Envelope #3 of Volume 7. At the conclusion of each instruction the "u" execution address of the next instruction is received by UAK from a portion of the X-Register (X_{15} through X_{29}) to prepare for the execution of the next instruction. (This transmission from the X-Register also includes X_0 through X_{14} to VAK and X_{30} through X_{35} to MCR.) The "u" address is stored in UAK until transmitted to SAR in preparation for a storage reference. In lieu of a "u" execution address, UAK may store the "j" and "n" factors during certain operations.

A "j" factor of a coded instruction is stored in UAK_{12} and UAK_{13}. For Manually Selected Jump (45jv) and Manually Selected Stop (56jv) instructions, a "j" factor of octal 0, 1, 2, or 3 is stored in UAK; enables from UAK_{12} and UAK_{13} are used in MCT to produce the proper operation enables. For operations requiring an external storage (MT) reference a "j" factor of 0, 1, 2, or 3 is stored in UAK producing "j" enables for use in PDC to address the proper MT unit. For high-speed punch operations a "j" factor of 1 is stored in UAK_{12} and is used to produce a seventh level hole. For external input-output operations a "j" factor of "1" or "0" is stored to determine the selection of ICE or IOA.

An "n" factor of a coded instruction is stored in UAK_0 through UAK_{11}. An "n" factor, accompanied with a "j" factor, is stored for operations requiring

an external storage (MT) reference. The number "n" stored indicates the number of magnetic tape blocks required by the operation. During the operation, the number "n" is transferred from UAK, via SAR and the X-Register, to the MT Block Counter determined by the accompanying "j" factor.

The counting properties of UAK are utilized during repeat operations. The "jn" factor of the repeat instruction is received by UAK and subsequently transferred to PAK where "jn" is complemented and used in the control of the operation. Following this operation, the "u" execution address of the instruction to be repeated is received from the X-Register. (This transmission from the X-Register also includes the "v" execution address to VAK and the operation code to MCR.) If the "u" address is to be advanced, as determined by a programmed selection of j = 2 or j = 3, this initial address in UAK is advanced by a signal from RSC after each execution of the repeated instruction. Note that the UAK cycle depends upon the initial "u" address of the repeated instruction. If the initial address is an MD address, UAK_{14} is "1" which enables the gate (V01-30214) allowing the ADVANCE UAK signal to sample UAK_0 through UAK_{13}. Thus the count in UAK advances from the initial MD address to MD address 77777, and then continues from MD address 40000 as the repeat operation continues. (It is possible to repeat an instruction a maximum of 4095 times, the capacity of PAK_0 through PAK_{11}.) If the initial address is not an MD address, UAK_{14} is "0" which disables the gate (V01-30214) allowing the ADVANCE UAK signal to sample only UAK_0 through UAK_9. Thus, if the initial UAK address is an MC address, UAK advances from the initial MC address to MC address 01777, then continues from MC address 00000. If the initial address is either the Q-Register address or the Accumulator address, the advance of the ten lower-order stages of UAK is meaningless.

(3) V-ADDRESS COUNTER. - The V-Address Counter (VAK) is shown on the Block Diagram, Address Registers, in Envelope #3 of Volume 7. The operation of VAK is essentially the same as that of UAK. At the conclusion of each instruction the "v" execution address of the next instruction is received by VAK from a portion of the X-Register (X_0 through X_{14}) to prepare for the next programmed operation. (This transmission from the X-Register also includes X_{15} through X_{29} to UAK and X_{30} through X_{35} to MCR.) The "v" address is stored in VAK until transmitted to SAR in preparation for a storage reference. In lieu of a "v" execution address VAK may receive a shifting factor "k" for operations requiring a programmed number of shifts. During such operations, the number of shifts, "k", is transferred from VAK to SAR, thus setting the SK portion of SAR to "k".

As in UAK, the execution address of a repeated instruction in VAK may be advanced by a signal from RSC after each execution of the repeated instruction. The programmed selection of j = 1 or j = 3 controls the advance. The VAK cycle depends upon the initial "v" address of the repeated instruction. This cycle control, provided by the gate (V01-30194), is identical to that of UAK. The counting properties of VAK are also utilized during block transfer operations of information between MC and MT. During these operations the execution address in VAK is transmitted to SAR and VAK is advanced by signals from MT. If the initial "v" execution address during a block transfer is not an MC address, an SCC fault will result.

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e. MAIN CONTROL TRANSLATOR. - The Main Control Translator is shown in the Block Diagram, Main Control Translator and Main Control Register, in Envelope #4 of Volume 7. From the six-bit operation code stored in MCR, MCT produces operation code enables necessary for the execution of the instruction. The outputs from MCR_0 through MCR_2 are translated producing the unit's digit enables of the octal code. The translations so produced are defined as the enables X0 through X7. In like manner, the outputs from MCR_3 through MCR_5 are translated producing the eight's digit enables, defined as 0X through 7X, of the octal code. These enables produce, from the principal translator, the prime operation code enables and produce, in the auxiliary translator, the composite and condition operation code enables.

In the principal translator (the matrix-like circuit in the center of the diagram) the eight's digit enables and the unit's digit enables produce unique prime operation code enables for each computer instruction. Note that enables for 10, 20, 30, 40, 50, 60 and 70 are not produced, and prime operation code enables are produced for 00, 01, 02, 03, 04, 05, 06, 07, 22, 24, 25, 26, and 62 although there are no instructions assigned to them. An MCT fault will occur if MCR stores an operation code which is not included in the repertoire of the equipment.

In the auxiliary translator (the circuits at the top of the diagram), the eight's digit enables, the unit's digit enables, the MCR enables, the prime operation code enables and other relevant enables are combined to produce the following: (1) composite operation code enables, and (2) conditional operation code enables.

Composite operation code enables are produced by combining digit enables and MCR enables; thus enables are produced which represent several operations. They are used if several identical commands occur during the execution of the included operations. Such identical commands must occur at corresponding times during the respective operations. The use of composite operation code enables minimizes the combining of prime operation code enables in the Command Timing circuits.

Conditional operational code enables are used where optional sequences exist. These enables incorporate manual selections, the condition of arithmetic registers, "j" factors, and/or the condition of RSC with a prime operation code enable. To produce conditional operation code enables, the proper digit enables are combined with relevant enables which originate elsewhere in the equipment. The A Zero flip-flop (V80-30242) is included in MCT to produce conditional operation code enables. When A Zero is set to "1" by a signal from ASC, the "1" state registers the fact that the content of A was initially zero.

Outputs from MCT, from both the principal and auxiliary translators, are utilized throughout control, but mainly in CTC and MPD. In CTC, the MCT enables are used in the production of the command signals necessary to execute the instructions. In MPD, the MCT enables are used in the selection of the MP cycle required for the operation. MCT enables are also used in ARAC, PDC, the Fault Detector and Stop Control. Their use in these control circuits is discussed under the associated subjects. Where used, the MCT operation code enables are

identified, except for the STOP and JUMP ON enables, by the term "MCT" included in the enable name.

f. COMMAND TIMING CIRCUITS. - These circuits are shown on the Block Diagram, Command Timing Circuits (sheets 1 and 2) in Envelope #4 of Volume 7. The Command Timing Circuits (CTC) are the gates which produce the command signals necessary to execute the instructions. Each gate is enabled by one or more MCT enables and is probed by one or more MPs from MPD. The output from each gate is a "command" signal.

To facilitate the location of the gates, the block diagram is divided into groups, each labelled with a title which indicates the destination of the commands produced by the gates in the group.

The Command Timing Circuits produce a distinct sequence of commands for each instruction. These instruction sequences are presented in tabular form in Appendix B, under the Command Timing heading. The tables are arranged consecutively by instruction operation code.

On each table, the left-hand column lists the sequence of MPs that produce the sequence by probing the CTC gates.

The "command" column lists the names of the signals produced by each MP. The "Source" column lists the abbreviation for the portion of CTC producing the command. In this latter column, the abbreviations listed in Table 4-5 below are used. The "Destination" column lists the register, storage system, or control circuit that receives the command.

Table 4-5
Portions of CTC

PORTION OF CTC	ABBREVIATION
ARAC COMMANDS	CTC-ARAC
ARITHMETIC REGISTER COMMANDS	CTC-AR
ASC COMMANDS	CTC-ASC
INPUT-OUTPUT (IOA-IOB) COMMANDS	CTC-IO
OUTPUT COMMANDS	CTC-OUT
MT COMMANDS	CTC-MT
PDC COMMANDS	CTC-PDC
PAK COMMANDS	CTC-PAK
PCR COMMANDS	CTC-PCR
RSC COMMANDS	CTC-RSC
SAR (SK) COMMANDS	CTC-SAR
SCC COMMANDS	CTC-SCC
SKC COMMANDS	CTC-SKC
STOP CONTROL COMMANDS	CTC-STOP

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To use the Command Timing tables in Appendix B, it is necessary to understand the basic operation of MPD. There are two general types of MPD cycles: (1) a four, five, six, seven, or eight-pulse cycle produced after an MD START

or MT START; (2) special pulse cycles produced for the Repeat (75jnw) instruction and repeated instructions.

(1) NON-REPEATED INSTRUCTION SEQUENCES. - The sequence for all programmed instructions (except for the Repeat (75jnw) and repeated instructions) consists of a cycle that starts with MP 0, continues to MP 5, then concludes with MP 6 and MP 7. Because the operations performed by MP 6 and MP 7 are the same for all these instructions, these two MPs are not shown at the bottom of each Command Timing table but are listed on Page B-5 instead. As an example, the use of the tables for the Transmit Positive (1luv) instruction is described below.

The Transmit Positive instruction is executed by a four-pulse MPD cycle consisting of MP 0, MP 5, MP 6, and MP 7. This cycle is produced when PCR contains an 1luv instruction word. As shown on Page B-6, MP 0 produces commands which clear X, transmit an address into SAR, initiate a reading operation, and temporarily stop the advancing of MPD (WAIT INTERNAL REFERENCE). When the reading operation to X is completed, the Master Clock resumes the advancing of MPD, and MP 5 is produced next. MP 5 transmits a new address into SAR, initiates a writing operation, and produces another WAIT INTERNAL REFERENCE signal that stops MPD. When the content of X has been written, MPD is advanced to MP 6. As shown on Page B-5, MP 6 produces commands that clear PCR, insert an address from PAK into SAR, initiate a reading operation to obtain a new instruction, and stop MPD. When the reading operation is completed, MPD is advanced to produce MP 7. On MP 7, SAR is cleared and the new instruction is transmitted into PCR.

(2) REPEAT SEQUENCES. - The execution of the Repeat instruction causes the instruction which follows it to be executed n times. During the repeated execution of the instruction which follows, the execution addresses may be advanced after each execution depending upon the selection of j. If j is 0, neither execution address is advanced. If j is 1, the v execution address only is advanced. If j is 2, the u execution address only is advanced. If j is 3, both execution addresses are advanced. If the instruction is executed n times and no jump occurs, the program is jumped to fixed address (F_1). If a jump occurs, the program is jumped to the v execution address of the repeated Jump instruction. All instructions can not be repeated although the execution of the Repeat instruction may set up RSC for the repeat. An attempt to repeat an instruction in which a jump operation is called for will result in the immediate termination of the repeat by the clearing of RSC. Then the jump is made as the normal execution of the instruction continues. (Operation codes, 41, 44, 45, 46, 47 and 56 are the examples of such operations.) However, the Threshold Jump (42uv) and the Equality Jump (43uv) may be repeated and a special Jump Termination sequence is provided solely for these two operations.

The sequences occurring during the Repeat (75jnw) instruction and repeated instructions are shown graphically on Page B-98.

The Repeat instruction is executed by a cycle consisting of MP 0 through MP 5. On MP 5, the next instruction (to be repeated) is inserted into PCR, and a "repeat condition" is registered in RSC by an RSC Initiate Repeat subsequence.

If the value n in the Repeat instruction was not equal to zero, MPD is set to 7 and the resulting MP 7 clears SAR.

Next, the instruction to be repeated in PCR is executed up to n times by a repetitive MPD cycle starting with MP 0 and ending with MP 5. The operations during these instructions (except for the 42uv and 43uv instructions) are the same as those listed on pages B-6 through B-48, but in addition, a test is made on MP 5 to determine whether the cycle should be terminated.

If the cycle is to be terminated because n performances have occurred, MPD is permitted to advance to MP 6 and MP 7 for a CTC Repeat Terminations sequence. In CTC, these MPs insert an instruction obtained from F_1 into PCR.

If the cycle is terminated because a jump occurred, RSC operations cause a CTC Jump Termination sequence to be performed. This sequence, consisting of MP 1 through MP 5, causes the jump address to be inserted into SAR, and the "jump count" (j, n-r) to be stored in Q. Next, MPD is advanced to produce MP 6 and MP 7, which at this time produce the same CTC commands produced by MP 6 and MP 7 after any non-repeated instruction.

g. PROGRAM ADDRESS COUNTER. - The Program Address Counter (PAK) is shown on the Block Diagram, Address Registers, in Envelope #3 of Volume 7. PAK is an additive 15-stage binary counter whose principal function is to store sequentially the consecutive addresses used in the computer program. PAK performs an auxiliary function during repeat operations by serving as a repeat counter and by controlling the advancement of the execution addresses. Information from PAK goes to SAR only. Information input to PAK is either manual or from SAR.

The initial setting of PAK is made manually following the selection of either MD or MT START. This setting need only be made with an MT START if the starting program address is other than 00000, and need only be made with MD START if the starting program address is other than 40000. After the initial setting, the advance of PAK is automatic. At the conclusion of each non-repeated or non-jump instruction the next address in PAK is transmitted to SAR, where it determines the address from which the next instruction is obtained; then PAK is advanced by a signal from CTC. As a result, instructions stored at consecutive storage addresses are performed sequentially, until a jump or repeat condition occurs.

When the program address sequence is broken by a jump instruction, PAK is cleared and the address of the next instruction is transmitted to PAK via SAR from either UAK or VAK.

When a REPEAT (75jnw) instruction is performed, PAK serves as a repeat counter and an auxiliary control. During the Repeat instruction sequence, the complement of the number of repeats to be performed (n') is stored in PAK_0 through PAK_{11}. As each repeat operation is concluded, PAK is advanced by a signal from RSC until the PAK_{11} carry is produced, giving rise to the END REPEAT signal. The complement of the factor "j" is stored in PAK_{12}, PAK_{13} and PAK_{14} to control the advancement of the execution addresses during the repeat. (Note that if "j" is greater than 3, the complemented j value in PAK disables gate V01-30204, because PAK_{14} is set to "0". This gate blocks all carries above PAK_9, making a repeat termination impossible.) Because PAK is used to store n', the jump address w (see description of the Repeat Instruction) cannot be stored in PAK.

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For this reason the address w is stored in the v-portion of a jump instruction stored at "fixed address" 00000, and a jump to this fixed address is made at the conclusion of the operation.

When the execution of consecutively stored program instructions has proceeded to the last address of MDS or MC, the next ADVANCE PAK signal returns PAK to the first MDS or MC address, respectively. This "closed loop" feature prevents transfer of operations from MC to MDS, or vice-versa, unless such a transfer is intentionally programmed by the insertion of an instruction resulting in a jump. The MDS "closed loop" operation is caused by the absence of a carry input on PAK stage 14. The MC "closed loop" operation is caused by a gate that blocks the PAK stage 9 carry if PAK stage 14 is equal to "0", which will be the case if the PAK-stored address refers to MC, Q, or A.

h. REPEAT SEQUENCE CONTROL. - The Repeat Sequence Control (RSC) is shown on a block diagram in Envelope #2 of Volume 7. The Repeat Sequence Control produces special RSC and CTC sequences during the execution of the Repeat (75jnw) instruction and during repeated instructions. These sequences are shown in Appendix B under the RSC heading.

(1) GENERAL. - If a program instruction is to be performed "n" times, the instruction is preceded by the Repeat (75jnw) instruction. In the 75jnw instruction word, the value n determines the maximum number of times the instruction is to be executed, the value w is a "replace" address that is transmitted to the v-address portion of a "fixed address", and the value j causes the u and v address portions of the repeated instruction to be altered after each performance in the following manner:

if j = 0, or 4, u and v are not altered.
if j = 1, or 5, v is increased by 1.
if j = 2, or 6, u is increased by 1.
if j = 3, or 7, both u and v are increased by 1.

During MP 0 through MP 5 of the CTC 75 sequence, the replace address w is transmitted to the v address portion of fixed address F_1. The fixed address is located at either Magnetic Core Storage address 00000 or Magnetic Drum address 40001, depending upon the setting of a switch on the Supervisory Control Panel. However, during the normal mode, this switch must be set to the MC (F_1 = 00000) position. The current program address in PAK is used to locate the next instruction (to be repeated), and then PAK is altered to contain the complements of the values j and n. An INITIATE REPEAT signal initiates an RSC Initiate Repeat sequence.

During an RSC Initiate Repeat sequence, the value n, stored in complemented form in PAK, is altered. If n is equal to "0", the RSC Initiate Repeat sequence is followed by a CTC Repeat Termination sequence. If the value of n is greater than "0", the RSC Initiate Repeat sequence establishes a "hold repeat" condition in RSC and CTC, and a CTC MP 7 Repeat sequence results.

On MP 7, the instruction to be repeated is retained in PCR. If the instruction is not a jump instruction, the normal CTC operations for the particular instruction are performed on MP 0 through MP 5. In addition, the previously established "hold repeat" condition causes special CTC MP 5 Repeat operations to

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be produced on MP 5. These special operations initiate an RSC End Test (No Jump) sequence.

If the next instruction is either a Threshold Jump (42uv) or an Equality Jump (43uv) instruction, the "hold repeat" condition established earlier modifies the CTC operations normally occurring during these instructions. If jump conditions do not occur during the repeat-modified CTC 42 or 43 sequence, an INITIATE END TEST signal initiates an RSC End Test (No Jump) sequence. If jump conditions occur, two signals, INITIATE END TEST and INITIATE JUMP TERMINATION, initiate an RSC End Test (With Jump) sequence.

During an RSC End Test (No Jump) sequence, the value n', stored in PAK, is altered by one count. If the altered value n is not zero, the RSC End Test (No Jump) sequence alters UAK and VAK as specified by the value j, and initiates a CTC MP 7 Repeat sequence, so that the instruction PCR will be retained and will be repeated. If the altered value n is equal to zero, indicating that the proper number of repeat instruction executions have been performed, the RSC End Test (No Jump) sequence is followed by a CTC Repeat Termination sequence.

The CTC Repeat Termination sequence differs from the normal CTC MP 6 and MP 7 sequence in that the previously established "hold repeat" condition causes an additional subcommand, SET SAR TO F_1 to be produced. As a result, the next instruction is obtained from F_1. Usually, F_1 stores a jump instruction, and the v address portion of F_1, inserted during the CTC 75 sequence, causes the program to jump to a new routine starting at the w address specified in the 75jnw instruction.

If the repeated instruction is either a 42uv or a 43uv jump instruction and jump conditions are fulfilled, the resulting RSC End Test (With Jump) sequence initiates a CTC Jump Termination sequence by setting MPD to MP 1.

The CTC Jump Termination sequence is produced in CTC when MPD is set to MP 1 and the "hold repeat" condition exists. The sequence, consisting of MP 1 through MP 5, transmits the values j and n-r, where r equals the number of repeated instruction performances, into the Q register. These values may be used in subsequent program routines to locate the address of the data fulfilling jump requirements. The CTC Jump Terminate sequence is followed by a normal CTC MP 6 and MP 7 sequence, which causes the program to jump to the v address specified in the last performed 42uv or 43uv instruction.

(2) RSC OPERATIONS. - The specific operations that occur in the Repeat Sequence Control are described in detail below.

(a) OPERATIONS DURING THE 75 SEQUENCE. - During the 75 sequence, MP 0 through MP 5, the 75 FF flip-flop is set to "1" and an INITIATE REPEAT signal produces an RSC Initiate Repeat sequence.

The CTC 75 sequence differs from other instruction sequences in that MCR is cleared on MP 3, and the next instruction is transmitted into MCR on MP 5 instead of MP 7. As a result, MCR is empty on MP 4 and MP 5. On MP 3, as MCR is cleared, the SET 75 FF signal registers a "75" condition in RSC by setting the 75 FF flip-flop to "1". In CTC, the 75 instruction sequence operations are made possible by the 75 FF "1" enable from RSC.

The CTC 75 sequence is also unique in that PAK is used to count repeats instead of program addresses. The values j and n are transmitted into PAK on MP 4. Later, PAK is complemented and each ADVANCE PAK signal advances by one count the complemented n value toward "0".

An INITIATE REPEAT signal is produced on MP 5. In CTC, this signal transmits the next instruction from X into PCR, temporarily stops the Master Clock, and complements the value n stored in PAK. In RSC, the Initiate Repeat signal sets the Initiate Repeat and End Repeat flip-flops to "1".

(b) RSC INITIATE REPEAT SEQUENCE. - When the Initiate Repeat flip-flop is set to "1", an Initiate Repeat sequence occurs in RSC. The first operation performed by this sequence alters the repeat count by advancing PAK. If the value n was initially equal to zero, the ADVANCE PAK signal produces a PAK END CARRY or END REPEAT signal that sets the End Repeat flip-flop in RSC to "0". Other operations of the Initiate Repeat sequence clear the 75 flip-flop, register the "hold repeat" condition by setting the "Hold Repeat" flip-flop to "1", and restart the Master Clock with an RSC RESUME signal.

The final operation of the sequence, performed only if the End Repeat flip-flop has remained set to "1", sets MPD to MP 7. If this final operation does not occur, MPD advances in the normal manner to MP 6.

The "hold repeat" condition, registered by the Hold Repeat flip-flop set to the "1" state, alters normal CTC operations so that the MP 6 or MP 7 pulses occurring after the RSC Initiate Repeat sequence perform either a CTC MP 7 Repeat sequence or a CTC Repeat Termination sequence.

(c) CTC MP 7 REPEAT SEQUENCE. - The absence of a Hold Repeat "0" enable in CTC prevents the forming of an X→PCR command, and the instruction stored in PCR during the CTC 75 sequence is retained. The MP 7 operations are followed by the execution of the next (repeated) instruction.

(d) CTC REPEATED INSTRUCTION SEQUENCE. - If the repeated instruction is neither a 42uv nor a 43uv instruction, the MP 0 through MP 5 operations occur in the normal manner, but the presence of the Hold Repeat "1" enable produces additional operations on MP 5. These CTC MP 5 Repeat operations initiate an RSC End Test sequence and alter the value n by advancing PAK.

If the repeated instruction is either a 42uv or a 43uv instruction, the MP 0, MP 1, and MP 2 operations occur in the normal manner, but the presence of the Hold Repeat "1" enable in MCT and CTC alters the MP 3, MP 4, and MP 5 operations. Principally, these operations are altered so that a jump condition, if satisfied, causes the values j and n-r to be transmitted to Q. If a jump condition is satisfied, MP 3 operations produce an INITIATE JUMP TERMINATE signal. On MP 5, an INITIATE END TEST signal initiates an RSC End Test sequence.

(e) RSC END TEST SEQUENCES. - Two forms of RSC End Test sequences are possible. If the repeated instruction was not a jump instruction, or if the repeated instruction was a jump instruction but jump conditions were not fulfilled, an INITIATE END TEST signal produces an RSC End Test (No Jump) sequence. If the repeated instruction was a jump instruction and jump conditions

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were fulfilled, the resulting INITIATE JUMP TERMINATE signal followed by an INITIATE END TEST command produces an RSC End Test (With Jump) sequence.

If the value n-r is not "0", the RSC End Test (No Jump) sequence conditionally advances UAK and VAK as specified by the complemented j value obtained from PAK stages 12 and 13, and sets MPD to MP 7 so that a CTC MP 7 Repeat sequence occurs and the instruction stored in PCR is repeated. If previous MP 7 Repeat sequence operations have altered the complemented n-r value, stored in PAK, to "0", the resulting END REPEAT signal will have set the End Repeat flip-flop to "0". If this has occurred, the RSC End Test (No Jump) sequence allows a CTC Repeat Termination sequence to occur. A CTC Repeat Termination sequence clears the "hold repeat" condition by clearing RSC, and obtains the next instruction from fixed address F_1.

The presence of the Jump Terminate "1" enable causes the End Test sequence to set MPD to MP 1. In CTC, the presence of the Jump Terminate "1" enable produces the MP 1 through MP 5 CTC Jump Terminate sequence of operations. This sequence transmits the values j and n-r into Q and transmits the current contents of VAK into SAR, so that the next instruction will be obtained from the address specified by the last performed 42uv or 43uv instruction. The CTC Jump Terminate sequence is followed by a normal CTC MP 6 and MP 7 sequence, that causes the program to resume at the specified v address.

i. FAULT DETECTOR. - The Fault Detector circuitry is shown on the Block Diagram, Fault Detector and Stop Control, and Block Diagram, Manual Controls, both in Envelope #5 of Volume 7. The Fault Detector detects the presence of faults and stops equipment operation when a fault occurs. Of the 12 types of faults that may be detected, seven produce an A Fault stop equivalent to a Force Stop (CONTROLLED CLOCK PULSES cease) and five produce a B Fault stop equivalent to a Final Stop (CONTROLLED CLOCK PULSES cease and selections on the Supervisory Control Panel drop). The two types of stops are used because the B Faults are more serious than the A Faults, and B Faults usually necessitate the restarting of the computer program. When a fault occurs, the specific type of fault is indicated on the Supervisory Control Panel in Fault Indicators Group.

(1) A FAULTS. - When an A Fault condition exists, an A Fault voltage from the Fault Detector energizes the A Fault relays K30006 and K30036. When this occurs, a sequence of relay operations stops the distribution of CONTROLLED CLOCK PULSES from the Master Clock, and the Operate relays are dropped. However, the contents of the computer storage and flip-flops are not dropped, so that operation may usually be resumed by removing the cause of the fault, pressing the CLEAR A FAULT button, and pressing the START button. Pressing the CLEAR A FAULT button clears all flip-flops used to detect the fault. The specific faults that produce an A Fault condition are listed below.

(a) SCC FAULT. - An SCC Fault is produced if a reference is made to a storage class erroneously. The erroneous references that are detected in the Fault Control are listed in Table 4-6 below.

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TABLE 4-6

SCC FAULT CONDITIONS

SIGNALS PRODUCING THE FAULT		REASON
PULSES	ENABLES	
"1" From Initiate Write (0-14)	A or Q	Partial writing impossible in A or Q.
"1" From Initiate Write (0-14)	Not A, Q, MC, or MD	Unassigned address in SAR
"1" From Initiate Write (15-29)	A or Q	Partial writing impossible in A or Q.
"1" From Initiate Write (15-29)	Not A, Q, MC, or MD	Unassigned address in SAR
"1" From Initiate Write (0-35)	Not A, Q, MC, or MD	Unassigned address in SAR
"1" From Initiate Read	Not A, Q, MC, or MD	Unassigned address in SAR
Initiate Read A	MP 7 Enable	Next instruction should not be read from A.
Internal Storage Resume	MCT 64 and NOT MC	Tape information not writing in MC.
Internal Storage Resume	MCT 65 and NOT MC	Tape information not read from MC.

This table shows that the production of a partial write signal (INITIATE WRITE 0-14 or 15-29) is a fault if a reference is made to A or Q. Also, any INITIATE WRITE or READ signal is invalid if no reference is made to A, Q, MC, or MD. If an instruction sequence is performed that specifies that the next instruction is to be obtained from the A register, the MP 7 enable and the INITIATE READ A signal produce an A Fault. This is detected as a fault because there is a possibility that the ARAC RESUME produced in ARAC may cause the instruction sequence to proceed to MP 7 before PCR has had time to clear and receive the instruction from A, so that an erroneous instruction may be registered in PCR. An SCC Fault is also registered if a Read or Write Magnetic Tape (64jnv or 65 jnv) instruction is being performed and a reference has been completed to an address not in MC. Instructions 64 and 65 specify that operands in the Magnetic Tape System are to be transmitted only to and from MC, so that a reference to an address not in MC is invalid.

When an SCC Fault occurs, the SCC Fault flip-flop is set to "1" and an MCT/SCC FAULT signal is produced. The SCC Fault relay K30059 energizes and closes a contact to produce the A FAULT signal. In the Stop Control, the MCT/SCC FAULT signal produces a STOP signal, which immediately shuts off CONTROLLED CLOCK PULSES.

(b) DIVIDE FAULT. - During the performance of a division, the ASC Divide sequence performs two division checks to determine if the quotient resulting from the division will exceed the capacity of Q. If the quotient is too large, a DIVIDE CHECK STOP signal is produced. In the Fault Detector, this signal sets the Divide Fault flip-flop to "1", so that the Divide Fault relay K30058 energizes. When energized, this relay closes a contact to produce an A FAULT signal. The DIVIDE CHECK STOP signal is also sent to Stop Control to produce a STOP signal.

(c) PRINT FAULT. - During the execution of a Print (61-v) instruction, the lower-order six bits of an operand are translated. If the combination is acceptable, a character is printed or a typewriter function is performed. If the combination is one of the unacceptable combinations, a fault is detected.

When any of these "impossible characters" are present in the Output Translator, a sequence of Output System relay operations produces a PRINT FAULT signal that energizes the Impossible Print Fault relay K30062 in the Fault Detector. When energized, this relay produces an A FAULT signal.

(d) WATER FAULT. - If the pressure of the cooling water in the Blower (90000) Cabinet drops to a preset value, a pressure switch operates to de-energize the Water Fault relay K30072. When de-energized, this relay produces an A FAULT signal.

(e) TEMPERATURE FAULT. - When the temperature above a chassis channel of any bay exceeds 100°F, the low temperature thermostat located at the top of the channel operates to illuminate an indicator above the channel, and to open the Temperature Interlock circuit. This de-energizes the Temperature Fault relay K30074, allowing an A FAULT signal to be produced.

The BYPASS INTERLOCKS key switch on the Supervisory Control Panel provides means of bypassing this circuit so that the computer may be operated even though this fault exists. A buzzer sounds continually if this switch is turned.

(f) ABNORMAL CONDITION. - If the equipment is in the NORMAL operating mode, certain improper switch settings or power supply conditions produce an Abnormal condition fault.

When the POWER SEQUENCE selector switch on the Main Power Panel is not in the OPERATE position, the MT and MD Write voltages are disconnected and an ABNORMAL CONDITION signal is produced. An ABNORMAL CONDITION signal is also produced if the POWER SEQUENCE selector switch on the MC Power Panel is not in the OPERATE position, or if any of the Supervisory Control Panel TEST SWITCH GROUP switches are not in the normal condition. The Abnormal Condition is indicated by the illumination of the ABNORMAL CONDITION indicator in TEST SWITCH GROUP of the Supervisory Control Panel. No fault stop will occur if the equipment is in the TEST mode.

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(g) OVERFLOW FAULT. - When the INITIATE MULTIPLY signal occurs and $A_{34} \neq A_{35}$, the Overflow flip-flop is set to "1". The OVERFLOW STOP signal is produced. This signal, sent to the Stop Control, produces a STOP signal which stops the computer. Also, relay K21602 is energized, which, in turn, energizes the A Fault relay, and illuminates the OVERFLOW indicator. This indicates that there is a possibility that the product about to be formed may be too large for A.

(2) B FAULTS. - When a B Fault condition exists, a B FAULT voltage from the Fault Detector energizes the B Fault relays (K30008 and K30038). When this occurs, a relay sequence stops the distribution of CONTROLLED CLOCK PULSES from the Master Clock, drops the Operate relays, and drops the manual selections previously made at the Supervisory Control Panel. As a result, the equipment can be restarted only by making new manual start selections. The specific faults that produce the B Fault condition are described below.

(a) MCT FAULT. - An MCT Fault is produced if PCR contains an invalid operation code. The fault is registered by the MCT Fault flip-flop, which is set to "1" by MP 0 when invalid MCT enables 00, 01, 02, 03, 04, 05, 06, 07, 10, 20, 30, 40, 50, 60, 70, 22, 24, 25, 26, and 62 are present. When the fault occurs, the MCT Fault flip-flop is set to "1" on MP 0 and an MCT/SCC FAULT signal is produced. MCT Fault relay K30061 energizes and closes a contact that produces a B FAULT signal. In the Stop Control, the MCT/SCC FAULT signal produces a STOP signal that stops CONTROLLED CLOCK PULSES.

(b) MISSING LINE PULSE FAULT. - In the Magnetic Tape Storage System, the magnetic tape stores information in "blocks" consisting of 576 lines. In each block, each line is accompanied by a LINE PULSE written on two parallel timing tracks of the tape. No LINE PULSES are present in the "interblock space", the space between blocks. During the reading of a block, the LINE PULSES are counted. When 576 have been counted, a BLOCK PULSE is produced while an interblock space is passing through the reading station. If more than 576 are counted, the BLOCK PULSE is produced while LINE PULSES are being read. If less than 576 are counted, the BLOCK PULSE is not produced until the next block is read, and additional LINE PULSES are being read. In either case, a LINE PULSE read coincidently with a BLOCK PULSE sets an Error flip-flop to "1", indicating that the block contained either more or less than 576 LINE PULSES. This energizes the MISSING LINE PULSE relay, which, in turn, energizes the B FAULT relay.

This type of fault also occurs if the end of any tape reel is approached. Special LINE PULSES recorded in the interblock spaces at the extremities of each reel of tape produce the fault condition so that the tape is not run too far in one direction.

(c) VOLTAGE (BIAS) FAULTS. - When the detection of a faulty voltage causes the Fault Relay of either the Main or MC Power Supply to de-energize, a BIAS FAULT signal energizes the B FAULT relay, and the VOLTAGE FAULT indicator of Supervisory Control Panel FAULT INDICATORS GROUP illuminates.

(d) IO FAULT. - If the control for the external equipment connected to IOA and IOB calls for a reading operation before the data from a previous reading operation has been assimilated by the computer, or before the data

from a previous write or select operation has been assimilated by the external equipment, four types of IO Faults may occur. Each of these energizes the IO Fault relay K21601, which in turn energizes the B Fault relays. When one of these faults occurs, the IO indicator in Supervisory Control Panel FAULT INDICATORS GROUP glows, and one of the four READ FAULTS indicators on the upper Input-Output panel glows.

1. IOA 1 FAULT. - Each time a reading operation from IOA is performed, an IOA WAIT READ "1" enable is produced in PDC. When the computer is through processing the information, the IOA WAIT READ "1" enable is removed from the Fault Detector. However, if another reading operation occurs before the IOA WAIT READ "1" enable is removed, the IO FAULT relay K21601 is energized.

2. IOA 2 FAULT. - If a writing operation occurs before the IOA WAIT READ "1" enable is removed, the IO FAULT relay is energized.

3. IOB 1 FAULT. - This fault is similar to the IOA 1 FAULT, except that it involves IOB instead of IOA.

4. IOB 2 FAULT. - This fault is similar to the IOA 2 FAULT, except that it involves IOB instead of IOA.

(e) EXTERNAL FAULT. - In the control circuits of the external input-output equipment connected to IOA and IOB, there are usually several fault detection circuits. If any of these produce a fault, an EXTERNAL FAULT signal from the external equipment control energizes the IO Fault relay K21601. Another voltage from the external equipment illuminates the EXTERNAL FAULT indicator on the upper section of the Supervisory Control Panel. When energized, the IO Fault relay illuminates the IO FAULT indicator and energizes the B Fault relay.

j. STOP CONTROL. - The Stop Control is shown on the Block Diagram, Fault Detector and Stop Control, in Envelope #5 of Volume 7. The Stop Control stops the equipment when a Manually Selected Stop (56jv) instruction is executed to produce a stop, when a Final Stop (57--) instruction is executed, or when certain A Faults occur.

(1) MANUALLY SELECTED STOP. - When a Manually Selected Stop (56jv) instruction is executed, a stop is produced if the j value of the instruction word is equal to 0, or if j is equal to 1, 2, or 3 and if the correspondingly labelled SELECT STOP buttons on the Supervisory Control Panel have been pressed.

In the Main Control Translator, the manual selections produce STOP 0, MANUAL STOP 1, MANUAL STOP 2, or MANUAL STOP 3 enables when a 56jv instruction is performed. In the Command Timing Circuits, the 56 instruction sequence produces a STOP CLOCK command on MP 5 if any of these enables are present.

In the Stop Control, the STOP CLOCK command produces a STOP signal that shuts off CONTROLLED CLOCK PULSES in CRC and ADVANCE MPD in PDC (see Block Diagram, Master Clock). In PDC, a STOP ENABLE is produced.

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In the Stop Control, the STOP ENABLE and the STOP 0, MANUAL STOP 1, MANUAL STOP 2, or MANUAL STOP 3 enables produce a 0, 1, 2, or 3 STOP voltage, that energizes a Stop relay. When any of these relays are energized, other relays are de-energized so that certain operating voltages are removed from the equipment. The operands in the Storage and Arithmetic Systems are not destroyed, so the program may be resumed by pressing the START button on the Supervisory Control Panel.

(2) FINAL STOP. - When a Final Stop (57--) instruction is executed, a STOP CLOCK signal is produced in CTC on MP 0. In the Stop Control, this signal produces a STOP signal that shuts off CONTROLLED CLOCK PULSES in CRC and ADVANCE MPD in PDC. In PDC, a STOP ENABLE is produced.

In the Stop Control, the MCT 57 enable and the STOP ENABLE produce a FINAL STOP voltage that energizes the Final Stop relay K30057. When energized, the Final Stop relay drops the Supervisory Control Panel start selections; therefore, new program start selections must be made before the equipment is restarted.

(3) A FAULT STOPS. - In most cases, the A Fault condition causes a relay sequence that shuts off CONTROLLED CLOCK PULSES. However, a few A Fault conditions operate through the Stop Control so that the CONTROLLED CLOCK PULSES are shut off immediately, because these faults are the type that affect operands in the computing system. The particular A Faults which shut off the Master Clock immediately are the Divide Fault, MCT Fault, SCC Fault, and Overflow Fault. These faults produce DIVIDE CHECK STOP, MCT/SCC FAULT, and OVERFLOW STOP signals, respectively.

In the Stop Control, any of these signals produce a STOP signal that immediately stops the distribution of CONTROLLED CLOCK PULSES in the Master Clock. Later, a relay sequence in the Control System relays removes certain operating voltages from the equipment. After the fault has been corrected, if possible, the equipment may be restarted by pressing the START button.

k. MANUAL AND RELAY CONTROLS .- The Manual Controls and associated relay circuitry are shown on the Block Diagram, Manual Controls, in Envelope #5 of Volume 7. The pushbuttons and indicators for these circuits are located on the Supervisory Control Panel. The relays are contained in the Control (30000) Cabinet.

The circuits are divided on the drawing into groups, according to function.

(1) START SELECTION GROUP. - The START SELECTION GROUP pushbuttons and relays provide a means of presetting the equipment before a start is made. Selections for MD START or MT START may be made by pressing the appropriately labelled pushbuttons. Making a selection produces MASTER CLEAR signals and special PRESET signals that preset registers and flip-flops in preparation for the selected type of start.

The pushbuttons and relays are interlocked so that only one of the selections may be made in START SELECTION GROUP. If a new selection is desired, pressing the RELEASE button drops the previous selection, if the equipment is not in operation. After the RELEASE button is pressed, K30009 is energized through

normally-closed contacts of the selection pushbuttons.

Pressing any one of the selection pushbuttons produces a relay sequence that creates the proper set and clear pulses. When one of the buttons is pressed, K30009 is de-energized. A normally-closed contact of K30009 then energizes K30010. Pressing the button also energizes one group of selection relays, K30003 and K30004 or K30001 and K30002. A contact of selection relay K30002 or K30004 re-energizes K30009, which in turn de-energizes K30010. The overall result is that pushing either selection button causes K30009 to de-energize momentarily, causes K30010 to energize momentarily, and causes one group of selection relays to energize and hold. During this sequence, the opening and closing of relay contacts produce the clear and set signals.

The operation of K30009 and K30010 contacts and the operation of selection relay contacts produce MASTER CLEAR I and MASTER CLEAR II signals, and apply screen grid voltage to amplifier V31009-30103. The next CLOCK PULSE produces a MASTER CLEAR III signal. These MASTER CLEAR signals clear PDC, PAK, ASC, SCC, the Fault Detector, MTS, A, Q, and PCR. MASTER CLEAR I and II perform clearing and setting operations through crystal "OR" circuitry connected to the manual pushbuttons on the upper parts of the Supervisory Control. MASTER CLEAR III is applied directly to circuits in the Control (30000) Cabinet.

Other signals produced by making selections are described below.

(a) MT START. - When the MT START button is pressed, the relay sequence causes K30003 and K30004 to energize and hold, and K30010 to energize momentarily. After the MASTER CLEAR signals occur, contacts of these relays produce a PRESET MT signal. This signal sets MCR to 64, UAK to "1", MPD to 0, and PAK to 00000, so that when the equipment is started, the first block of MT Unit 0 is transmitted to the first MC Address, 00000.

(b) MD START. - When the MD START button is pressed, the resulting sequence causes K30001 and K30002 to energize and hold, and K30010 to energize momentarily. After the MASTER CLEAR signals occur, contacts of these relays produce a PRESET MD signal that sets MPD to 6 and sets PAK to 40000. Consequently, when the equipment is started, the first instruction is read from the first address of the drum.

(2) SELECTIVE JUMPS GROUP. - The SELECTIVE JUMPS GROUP pushbuttons and relays provide means of manually selecting programmed Manually Selective Jump (45jv) instructions in the program. If all three RELEASE buttons are pressed, only the 45jv instructions having $j = 0$, produce jumps. If one of the jump selections 1, 2, or 3 is made, not only the 45jv instructions of the program having $j = 0$ produce jumps, but also the instructions having $j = 1$, 2, or 3 produce jumps, depending upon the selection made. If desired, all three selections (1, 2, and 3) may be made, and as a result all 45 jv instructions are performed.

The SELECT JUMP pushbuttons are interlocked by OPERATE relay contacts so that a SELECTIVE JUMPS GROUP selection must be made before the equipment is in operation. The RELEASE JUMP contacts are interlocked by OPERATE relay contacts so that a selection cannot be dropped during operation. When any of these relays are energized, contacts of the relays produce the JUMP ON enable in the

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Main Control Translator when MCR is set to 45 and the j portion of UAK is set to the jump number selected in SELECTIVE JUMPS GROUP. The JUMP ON enable initiates the jump. (See Block Diagram, Main Control Translator.)

(3) SELECTIVE STOPS GROUP. - The SELECTIVE STOPS GROUP pushbuttons and relays control the stopping of computer operations. This group not only provides means of selecting programmed Manually Selective Stop (56jv) instructions for execution, but also provides means of stopping the computer when a Final Stop (57--) instruction is executed, when FORCE STOP is pressed, or when a B Fault occurs.

(a) MANUAL STOP SELECTIONS. - Programmed 56jv stop instructions are selected for execution by pressing SELECT STOP buttons of SELECTIVE STOPS GROUP. If all three RELEASE buttons are pressed, all selections are dropped and only the 56jv instructions having j = 0 are performed. If one of the stop selections 1, 2, or 3 is made, not only the 56jv instructions having j = 0 produce stops, but also the instructions having j = 1, j = 2, or j = 3 produce stops, according to the selection made. Any combination of selections may be made.

Pressing one of the SELECT STOP buttons 1, 2, or 3 energizes one of the Select Stop relays K30024, K30025, or K30026. The selected relay closes contacts that hold the relay energized. In the Main Control Translator, a contact of the selected relay enables an MCT circuit that sends a MANUAL STOP 1, 2, or 3 signal to the Stop Control and to CTC when one of the selected 56jv Stop instructions is performed. (See Block Diagrams, MCT and Stop Control.) If a 56jv instruction having j = 0 is performed, a STOP 0 signal is sent to the Stop Control and to CTC. These signals initiate the stopping of the Master Clock.

In the Stop Control, the receipt of one of these signals produces a 0 STOP, 1 STOP, 2 STOP, or 3 STOP voltage when a STOP enable is received from PDC. The 0, 1, 2, or 3 STOP voltage energizes one of the Stop Control relays K30054 through K30057. The energized relay opens contacts in a STOP circuit, which causes the OPERATING GROUP Start and Operate relays to drop, so that the equipment may be restarted by pressing the OPERATING GROUP START button.

The Manual Stop selections may be made at any time, or may be dropped at any time by pressing the appropriate RELEASE buttons.

(b) FORCE STOP. - If the FORCE STOP button is pressed, K30039 energizes. If this button is pressed before a start is made, the relay holds until OPERATING GROUP START is pressed. When energized, K30039 opens a contact in the STOP circuit so that the OPERATING GROUP Start and Operate relays de-energize, and opens a contact in the circuit of Master Clock relays K31201 and K31202. When K31201 and K31202 are de-energized, the Clock Rate Control Circuit is altered, and thereby distribution of CONTROLLED CLOCK PULSES is discontinued. After a force stop occurs, the equipment may be restarted by pressing the OPERATING GROUP START button.

(c) FINAL STOP. - When a Final Stop (57--) instruction is performed, the Master Clock is set so that MPD is no longer advanced, and a FINAL STOP voltage is produced in the Stop Control.

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In the Stop Control, this voltage energizes K30057, which opens a contact in the STOP AND DROP SELECTION Circuit. This causes the START SELECTION GROUP, OPERATING RATE GROUP, and CLOCK SOURCE GROUP selections to be dropped, so that new selections must be made before the OPERATING GROUP START button is pressed. When the START SELECTION GROUP selection drops, Ready relay K30050 of OPERATING GROUP de-energizes. When de-energized, this relay de-energizes the OPERATING GROUP Operate relays and Master Clock Relays K31201 and K31202. The Master Clock stops the distribution of CONTROLLED CLOCK PULSES. The equipment can be restarted only after new Start selections have been made.

(d) B FAULT. - When a B Fault occurs, B Fault relay K30038, in the Fault Detector, energizes and opens a contact in the STOP AND DROP SELECTION circuit, so that a B Fault produces a stop similar to the Final Stop described above.

(4) A/B FAULT GROUP. - This circuit operates in conjunction with an A Fault or a B Fault, and clears the A Fault portion of the Fault Detector when the CLEAR A FAULT button is pressed. (See Block Diagram, Fault Detector and Stop Control, Envelope #5, Volume 7.)

(a) A FAULT. - When an A Fault condition occurs, Fault Detector A Fault relay K30036 energizes. When this A Fault relay is energized, the OPERATING GROUP Ready relay K30050 de-energizes. When de-energized, K30050 de-energizes the OPERATING GROUP Start and Operate relays, and de-energizes Master Clock relays K31201 and K31202. This stops the distribution of CONTROLLED CLOCK PULSES.

The equipment is restarted by removing the cause of the A Fault (if possible), pressing the A/B FAULT GROUP CLEAR A FAULT button, and then pressing the OPERATING GROUP START button. Pressing the CLEAR A FAULT button momentarily energizes K30037, which applies a CLEAR A FAULT pulse to the A Fault portions of the Fault Detector.

(b) B FAULT. - When a B Fault condition occurs, the Fault detector B Fault relay K30038 energizes. When energized, this relay opens a contact in the STOP AND DROP SELECTION Circuit, so that the START SELECTION GROUP, OPERATING RATE GROUP, and CLOCK SOURCE GROUP selections are dropped. Then the START SELECTION GROUP selections drop, the OPERATING GROUP Ready relay K30050 de-energizes. When de-energized K30050 de-energizes the OPERATING GROUP Start and Operate relays, and de-energizes Master Clock relays K31201 and K31202, which in turn stop the distribution of CONTROLLED CLOCK PULSES. As a result, it is necessary to clear the source of the fault and make a new start selection before operations can be resumed by pressing the START button.

(5) OPERATING GROUP. - The OPERATING GROUP relays and pushbuttons provide means of starting computer operations after all preliminary manual selections have been made. Also, a OPERATING GROUP STEP button on the Supervisory Control Panel provides means of manually advancing the control system when a MANUAL-STEP selection has been made in OPERATING RATE GROUP.

The Ready relay K30050 is energized after START SELECTION GROUP, OPERATING RATE GROUP, CLOCK SOURCE GROUP, and OPERATION MODE GROUP selections have been made.

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When energized, the Ready relay closes a contact in the circuit of K30041 and K30042. Pressing the START button initiates a chain of relay operations. First, K30041 energizes and holds, and K30041 energizes K30042. Next, K30042 energizes K30043, K30044, and K30045, then K30043 energizes K30047 and K30048. Finally, K30047 holds K30042 energized and also de-energizes K30040, which in turn de-energizes K30041. At the end of these operations, Operating relay K30042 and Operate relays K30043 through K30048 remain energized. The Operating relay is held energized through a STOP circuit, which is held closed by Stop relays of GROUP SELECTIVE STOPS GROUPS.

During the relay cycle following the closure of the START button, START pulses are produced by the opening and closing of relay contacts. After the cycle has been completed and the Operate relays are energized, contacts of the Operate relays supply special operating voltages, and remove other voltages to disable manual controls on the Supervisory Control Panel. These outputs are described in detail below.

(a) START. - During the relay sequence, a START pulse is produced by the closing of a K30042 contact and the opening of a K30048 contact. In PDC, this pulse sets the PDC Stop flip-flop to "0" so that CONTROLLED CLOCK PULSES will advance MPD.

(b) START CLOCK or MANUAL STEP. - If HIGH SPEED has been selected in OPERATING RATE GROUP, a START CLOCK signal is produced by the closing of contacts of K30048 and K30041. In the Master Clock, this signal is shaped to form a pulse which sets CRC so that CONTROLLED CLOCK PULSES are released. If a MANUAL STEP selection has been made in OPERATING RATE GROUP, each closure of the STEP button produces a MANUAL STEP pulse that performs the same function.

(c) RUNNING TIME. - While the equipment is in operation, a contact of K30045 applies a-c to the RUNNING TIME meter on the Supervisory Control Panel. This meter measures operating time to the nearest 1/10th second.

(d) PAK SET COMMON. - Before the START button is pressed, a PAK SET COMMON voltage supplies the PAK set and clear buttons, thereby PAK may be set or cleared. During operation, a contact of K30043 interrupts this voltage so that PAK cannot be altered manually.

(e) SET COMMON (OPERATION MODE GROUP). - If TEST has been selected in OPERATION MODE GROUP and the OPERATING GROUP Ready Relay is energized, SET COMMON voltage is applied to all Supervisory Control set and clear pushbuttons except the PAK buttons. This permits the maintenance personnel to set flip-flops manually.

(6) OPERATING RATE GROUP. - The OPERATING RATE GROUP relays and pushbuttons provide means of selecting the rate of operation of the Control System. Although the control circuitry operates only from 500 kc clock pulses, the overall rate of operation may be effectively reduced by altering the Clock Rate Control so that 500 kc CONTROLLED CLOCK PULSES are supplied to the control circuitry singly or in bursts. As a result the equipment performs all operations in steps.

During NORMAL operation, an automatically acquired HIGH SPEED selection

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causes CRC to supply 500 kc CONTROLLED CLOCK PULSES continuously, until a Stop occurs.

For TEST operation, one of six different selections may be made: HIGH SPEED, MANUAL STEP OPERATION, MANUAL STEP CLOCK, MANUAL STEP DISTRIBUTOR, AUTOMATIC STEP CLOCK, or AUTOMATIC STEP OPERATION. A MANUAL STEP CLOCK selection alters CRC so that a single CONTROLLED CLOCK PULSE is distributed each time the GROUP V STEP button is pressed. A MANUAL STEP DISTRIBUTOR selection causes CRC to release bursts of CONTROLLED CLOCK PULSES, each burst lasting from the time the STEP button is pressed until MPD is advanced or a reference to a storage system, Output system, Input-Output system, or Arithmetic system has been completed. A MANUAL STEP OPERATION selection causes CRC to release burst of CONTROLLED CLOCK PULSES each time STEP is pressed, each burst lasting until one complete instruction sequence has been performed. The AUTOMATIC STEP CLOCK and AUTOMATIC STEP OPERATION selections are similar to the MANUAL STEP CLOCK and MANUAL STEP OPERATION selections, except that the CRC operations are not initiated by a pushbutton, but instead are initiated repetitively by a 5 to 35 cps thyratron oscillator. The AUTOMATIC STEP RATE potentiometer on the panel provides means of adjusting the repetitive rate.

The OPERATING RATE GROUP pushbuttons are interlocked so that selections can be made manually only after a CLOCK SOURCE GROUP TEST selection and before a OPERATING GROUP START selection. The selection relays are interlocked so that the automatic selection of MANUAL STEP OPERATION or of HIGH SPEED (occurring after selections OPERATING RATE GROUP NORMAL and START SELECTION GROUP START or MD START) drops any previous OPERATING RATE GROUP selection.

Any OPERATING RATE GROUP selection may be dropped manually by pressing the OPERATING RATE GROUP RELEASE button, providing the equipment is not in operation. After a new selection is made, K30034 and K30035 energize, which causes the Ready relay of OPERATING GROUP to energize. When this occurs, the equipment is ready to be started.

The effects produced by each selection is described in detail below. These subparagraphs refer to the Master Clock Block diagram.

(a) MANUAL STEP CLOCK. - After MANUAL STEP CLOCK is selected and the system is started, each closure of the OPERATING GROUP STEP button causes CRC to pass a single 500 kc CONTROLLED CLOCK PULSE.

Pressing the SELECT MANUAL STEP CLOCK button energizes K30027, and opens contacts in the circuit of CRC relays K31201 and K31202. As a result, the latter two relays de-energize and alter the circuit of CRC so that each MANUAL STEP pulse initiates a CRC flip-flop operation that distributes a single CONTROLLED CLOCK PULSE. The MANUAL STEP pulses are produced by pressing the OPERATING GROUP STEP button.

(b) MANUAL STEP DISTRIBUTOR. - Selecting MANUAL STEP DISTRIBUTOR energizes K30028, which holds energized. When energized, this relay de-energizes CRC relay K31202. This alters the CRC circuitry so that each time the STEP pushbutton is pressed, CRC starts to release CONTROLLED CLOCK PULSES. If the first clock pulse released advanced MPD, CRC is shut off and no additional CONTROLLED CLOCK PULSES are distributed until the next closure of the STEP button.

If however, the previous step produced a storage or output reference command, the resulting WAIT signal prevents the formation of an ADVANCE MPD signal, and CRC continues to distribute CONTROLLED CLOCK PULSES until a RESUME signal is received. As a result, MPD is advanced by one closure of the STEP button if no internal or external reference commands are produced and two closures of the STEP button if a reference is produced.

(c) MANUAL STEP OPERATION. - Selecting MANUAL STEP OPERATION energizes K30029, which holds energized. When energized, this relay drops any other OPERATING RATE GROUP selection that may have been made previously, and de-energizes K31201 in the Clock Rate Control. This alters the circuit of CRC so that each MANUAL STEP pulse causes CRC to distribute CONTROLLED CLOCK PULSES until MP 7 is received from MPD. Thus, each closure of the STEP button steps the system through one complete program instruction.

(d) AUTOMATIC STEP CLOCK. - When this selection is made, K30030 and K30031 energize and hold. In the Clock Rate Control, K30030 de-energizes K31201 and K31202. When this occurs, an oscillator having a frequency adjustable from 5 to 35 cps is enabled and the Manual Step shaper V01-30102 is disabled. Also, the circuit of CRC is altered so that each pulse from the 5-35 cps oscillator causes CRC to pass a single CONTROLLED CLOCK PULSE. This selection effectively slows the operational speed of the control system from 500 kc to 5-35 cps.

(e) AUTOMATIC STEP OPERATION. - When this selection is made, K30032 energizes and holds. In the Clock Rate Control, this relay de-energizes K31201 and enables the 5-35 cps oscillator. When de-energized, K31201 alters the circuit of CRC so that each pulse from the 5-35 cps oscillator causes CRC to distribute CONTROLLED CLOCK PULSES until MP7 is received from MPD. As a result, each pulse from the 5-35 cps oscillator steps the control system through one complete instruction sequence.

(f) HIGH SPEED. - When NORMAL or TEST and HIGH SPEED are selected K30033 energizes and holds. When energized, this relay disables the STEP button circuit and closes a contact in the line connected to the grid of shaper tube V01-30102. After the START button is pressed, the operation of Start relay K30041 and Operate relay K30048 creates a single START CLOCK pulse that triggers the shaper. The resulting shaped pulse causes CRC to distribute CONTROLLED CLOCK PULSES until a stop occurs.

This selection is made either manually in OPERATING RATE GROUP or automatically by selecting NORMAL in CLOCK SOURCE GROUP. After this selection has been made and START is pressed, the Control System operates at a 500 kc rate until a stop occurs.

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(7) CLOCK SOURCE GROUP. - The CLOCK SOURCE GROUP controls provide means of selecting the source of 500 kc CLOCK PULSES. During normal operation, the CLOCK PULSES are obtained from the Magnetic Drum Storage System (MDS). During test operation, the CLOCK PULSES may be obtained from either MDS or from a 500 kc oscillator, by pressing the CLOCK SOURCE GROUP DRUM or OSCILLATOR button.

When OPERATION MODE GROUP NORMAL is selected, a CLOCK SOURCE GROUP DRUM

selection is made automatically. Providing the equipment is not in operation, either selection may be dropped by pressing the RELEASE button. The CLOCK SOURCE GROUP relays are interlocked so that either selection, when made, disables the selection of the other.

When DRUM is selected, K30005 and K30020 energize and hold. In the Master Clock contacts of K31101 cause CLOCK PULSES to set flip-flop CSS I to "1"; therefore the Clock Source Selector, CSS, accepts MDS CLOCK PULSES instead of 500 kc OSCILLATOR PULSES.

When OSCILLATOR is selected, K30017 and K30018 energize. In the Master Clock, K30018 energizes relay K31101. When energized, K31101 transfers the CLOCK PULSES from the "1" input of flip-flop CSS I to the "0" side, which causes CSS to accept 500 kc OSCILLATOR PULSES instead of MDS CLOCK PULSES. This selection is used during test operation if it is desired to operate without the Magnetic Drum System.

(8) OPERATION MODE GROUP. - The OPERATION MODE GROUP pushbuttons and relays provide means of selecting the NORMAL or TEST mode of equipment operation. If the equipment is not in operation, a previous OPERATION MODE GROUP selection is dropped by pressing the RELEASE button. Either TEST or NORMAL may then be selected by pressing the appropriate button. The OPERATION MODE GROUP relays are interlocked so that either selection, when made, prevents the other selection from being made.

Pressing the NORMAL button energizes K30011 and K30012. These relays, when energized, produce automatic selections in OPERATION RATE GROUP and CLOCK SOURCE GROUP, and energize Normal relays K30013, K30016, K30077, K30078, K30046, K30051, and K30052. In CLOCK SOURCE GROUP, a DRUM selection is automatically made. In OPERATING RATE GROUP, a HIGH SPEED selection is automatically made.

The Supervisory Control Panel manual controls that are affected by an OPERATION MODE GROUP TEST selection are described below.

(a) SET COMMON. - The SET COMMON voltage is applied to the set and clear buttons when the Ready relay OPERATING GROUP is energized. This permits the manual setting or clearing of flip-flops.

(b) MT STOP COMMON. - An MT STOP COMMON voltage permits the operation of manual controls located on the left side of the Supervisory Control Panel, labelled ADVANCE, STOP, BACK and STOP DISCONNECT. These controls are used to operate the Magnetic Tape Units manually.

(c) AMPLIFIER MARGINAL CHECK COMMON. - An AMPLIFIER MARGINAL CHECK COMMON voltage is applied to the TEST SWITCH GROUP AMPLIFIER MARGINAL CHECK switches. By setting the TEST SWITCH GROUP switches, selected groups of amplifiers may be checked.

(d) MT WRITE COMMON. - The TEST SWITCH GROUP switches can be set to disconnect write voltage from MT Unit 0, 1, 2, or 3. During NORMAL, the MT WRITE COMMON voltage is interrupted so that these TEST SWITCH GROUP switches are disabled.

(e) MT TEST COMMON. - Voltage is supplied to enable the manual controls located near the OPERATING TIME meter. These controls, labelled LP, LP and WP, AND LP, WP AND STOP are used to introduce artificial pulses into the Magnetic Tape System during TEST.

10. POWER SUPPLY AND DISTRIBUTION

a. GENERAL. - System power is derived from two separate power supply units, as follows: (1) the Main Power Supply, serving the Control (30000) Cabinet, Magnetic Drum (60000) Cabinet, Magnetic Tape (70000) Cabinet, Arithmetic (10000) Cabinet, Cooling System, and external input-output equipment; and (2) the Magnetic Core Storage (MC) Power Supply serving the Magnetic Core Storage (55000) Cabinet.

Each supply furnishes the a-c and d-c voltages required to operate its part of the computer and provides for the regulation, control and distribution of these voltages. Both supplies operate from a 220 vac, three phase, 60 cycle primary source, and in full operation require approximately 45 KW at a power factor of 92% inductive.

The two power supplies are shown on block diagrams in Envelope 5 of Volume 7.

(1) PRIMARY POWER DISTRIBUTION. - From the building power, unregulated 220 vac (indicated by bold lines on the block diagrams) is distributed to the following elements of the two supplies: (a) in the Main Power Supply: the blower motor, the drum motor, the generator motor, the induction regulator, and the power control and sequencing circuit; and (b) in the MC Power Supply: the generator motor, the power control and sequencing circuit, and a portion of the filament transformers.

Application of power to both power supplies is controlled manually by operation of the Main Disconnect Switch S88001.

(2) CONTROL AND SEQUENCING. - The greater portion of each power supply is energized by its own power control and sequencing circuit. On each power control door is a NORMAL ON-OFF button for that supply. Pressing of the NORMAL ON-OFF button energizes a cycle timer which then drives a series of cam operated switches in sequence. As the switches operate, relays within the power sequence control are energized. Their contacts then apply power, by stages, to various components of the power supply and, ultimately, to the computer. To de-energize the equipment, the NORMAL ON-OFF button is pressed. The cycle timer is again actuated and power is removed, by stages, in reverse sequence. Automatic shutdown, due to a power supply fault, is initiated by the computer's protective system.

(3) PROTECTION. - Overload protection is provided by circuit breakers and replaceable fuses in the alternating current distribution systems and by thermal-overload relays and fuses in the direct current distribution system. Other elements of protection include bias sensing circuits and voltage sensing relays to guard against bias and -80V faults, while cabinet interlocks, thermostats, the vane switch, and emergency switches furnish protection to personnel and machine components.

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b. MAIN POWER SUPPLY. - The Main Power Supply consists of step-down transformers, the 88001 motor generator set, the induction regulator, voltage rectifier circuits, d-c voltage regulators, power sequence controls, and a-c and d-c power distribution systems.

This supply controls the application of power to all main equipment circuits and produces and distributes d-c voltages. Table 4-7 lists the voltages used by the main equipment and the source and distribution of each voltage.

(1) TRANSFORMERS. - Transformer T80001 located in the Main Power (80000) Cabinet steps down a single phase of 220 vac to 110 vac as supply for external equipment, bias, -80V fault indicators, and 110 vac service outlets of the computer. A similar transformer (T70001) located in the Magnetic Tape Cabinet supplies 110 vac to the magnetic tape units. Filament transformers located in the main equipment cabinets reduce 220 vac to 6.3 vac as supply for electronic tubes filaments. An external red lamp at the top of each bay indicates the presence of 220 vac in the bay. A center-tapped filament transformer in the Supervisory Control Cabinet supplies 3.2 vac to indicator lights on the Supervisory Control Panel.

During certain test procedures, the outputs of selected filament transformers in the Magnetic Tape, Magnetic Drum, Arithmetic, and Control Cabinets may be reduced to about 5.7 volts by operating the REDUCE HEATHER VOLTAGE switches on the Supervisory Control Panel.

(2) MOTOR-GENERATOR. - This unit develops the bulk of the main equipment's direct current supply. A 20 HP, three phase, squirrel-cage induction motor drives a pair of direct current generators, one developing +250 vdc, the other -125 vdc. The generator output voltages are applied to direct current regulators for regulation to lower values.

(3) INDUCTION REGULATOR. - This unit regulates 220 vac, three-phase, 60 cycle a-c from the primary source and supplies the rectifier circuits and transformers.

(4) VOLTAGE RECTIFIERS. - The rectifier circuits include the -300 vdc reference supply, the +60 vdc and +120 vdc relay supplies and the -30 vdc flip-flop set supply.

(a) NEGATIVE REFERENCE SUPPLY. - The -300 vdc reference supply is produced from 220 vac stepped-up through a center-tapped transformer and rectified by a conventional full wave rectifier circuit employing a pair of 3B28 electron tubes as rectifying elements. The output voltage is filtered by a choke input filter, regulated to -300 vdc and applied, as negative reference, to the d-c regulator control units.

(b) RELAY SUPPLY. - The +60 vdc and +120 vdc relay supplies are produced from 220 vac through step-down transformers and full wave, delta-wye rectifier circuits. The output voltages are not critical and are distributed without regulation to both the main equipment and the Magnetic Core Storage System.

(c) FLIP-FLOP SET SUPPLY. - The -30 vdc set supply employs a step-down transformer and full-wave, selenium bridge rectifier circuit. As in the case of the relay supplies, the output is distributed unfiltered and unregulated.

(5) DC VOLTAGE REGULATORS. - The output voltages of the +250V generator, -125V generator and -300V rectifier supply are regulated to lower voltages by

conventional electronic voltage regulator units. Each unit consists of two or more paralleled 6AS7's (called slave regulators) in conjunction with a control circuit. Each control circuit regulates the current through the slave regulators to maintain a constant output voltage. The voltages produced by these regulators are +200 vdc, +150 vdc, +100 vdc, +80 vdc, +5 vdc, -15 vdc, -25 vdc, and -80 vdc.

(6) POWER CONTROL AND SEQUENCING. - The power control and sequencing circuits include the power control panel, relay sequencing circuits, fault circuits, and miscellaneous relays and circuits effected during energizing or de-energizing of the main equipment power supply.

In the upper left hand corner of the Overall Block Diagram Main Equipment Power Supply in Envelope #5 of Volume 7, running from left to right are shown the cam-operated switches S81901 through S81909. In the upper right hand corner is the Switch Time Distribution chart. To the left of the chart is the fault circuit and, in the d-c distribution system, are the bias sensing circuits, voltage sensing relays, and thermal overload heaters associated with the contacts of this circuit. The main contactor, M-G start coil, and contacts controlled by the sequencing circuit are located in both the a-c and d-c distribution systems.

Table 4-8 lists the steps, sub-steps, action, and result incurred during energizing, partial de-energizing, or fully de-energizing the Main Power Supply.

(a) NORMAL ON SEQUENCE. - In normal operation, to energize the main equipment power, the MAIN DISCONNECT SWITCH is switched to the ON position and then the NORMAL ON-OFF button on the main equipment power control panel is pressed. The sequence of operations is presented in Part A, Table 4-8, Steps 1 and 2.

(b) VOLTAGE FAULT SEQUENCE. - When certain voltages fail, fault relay K81815 is de-energized and a sequence of operations occurs which partially de-energizes the Main Power Supply. These operations are listed in Part A of Table 4-9, Steps 1, 2, 3, and 4.

(c) NEGATIVE DC OVERLOAD SEQUENCE. - The operation of any one of the THERMAL OVERLOAD RELAYS, K81805, K81806, K81807 or K81808 located in the -125 vdc generator output lines, initiates a sequence of operations that removes all direct current voltages except the rectified voltages. Part A of Table 4-9 Steps 5 and 6 lists these operations.

(d) EMERGENCY SEQUENCE. - The emergency circuit opens if one or more of the following events occurs: if the temperature at the top of a bay exceeds 120°F, if air flow in the main air duct decreases, if a cabinet door is improperly opened, or if either of two EMERGENCY OFF buttons is pressed. Operation of the emergency circuit removes all power from the computer with the exception of the drum and blower drive motors. Step 7 of Table 4-9 lists only the operations affecting main equipment power. However, a similar shutdown is initiated simultaneously in MC power.

(e) NORMAL OFF SEQUENCE. - To turn off main equipment power, the NORMAL ON-OFF button on the power control door is pressed, and after the cycle

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timer has completed the off cycle, MAIN DISCONNECT SWITCH S88001 is switched to the OFF position. This sequence is shown in Steps 1 and 2 of Table 4-9.

(f) RE-ENERGIZING MAIN EQUIPMENT POWER. - Operations necessary to re-energize the equipment after a fault or emergency initiated shut-down are listed in Part C, Table 4-9.

(g) MANUAL SELECTION. - Selector switch S82205 may be operated when it is desirable to shut down the equipment partially. When the switch is operated, contacts of section A are opened to partially shut-down the main equipment power supply; contacts of section B short relay contacts within the fault circuit thereby allowing the equipment to be re-energized when the switch is turned back on; contacts of section C energize a power sequence relay in the control cabinet which, in turn, causes an ABNORMAL CONDITION indicator on the Supervisory Control Panel to glow.

Should the selector switch be turned back to the OFF position, the d-c relay supply to the MC Power Supply will be removed, thus de-energizing the Bias Fault relay in that supply, and causing a partial shut-down of MC power.

To re-energize main equipment power from the OFF position, turn the selector switch to the LOW HEATER position, press the CLEAR POWER SUPPLY FAULT button and turn the SEQUENCE CONTROL switch, by steps, to the OPERATE position.

(7) PRIMARY POWER DISTRIBUTION. - From the building power, unregulated 220V, three phase a-c is applied through the main disconnect switch and main fuses to circuit breaker panel E88002 of the motor generator assembly unit. From E88002 distribution in the Main Power Supply is to the power control and sequencing circuit through circuit breaker S88003, the motor-generator set through circuit breaker S88006, the induction regulator through circuit breaker S88004, and the drum and blower drive motor circuits through circuit breaker S88002.

From the induction regulator, regulated 220V, three phase a-c is applied to circuit breaker S81301 (labeled FILAMENT AND POWER SUPPLY) on circuit breaker panel 81300 in the Main Power cabinet. From S81301 power is distributed through secondary circuit breakers S81302-03-04-05-06 and 07 (labeled respectively MTS FILAMENTS, CONTROL FILAMENTS, MDS FILAMENTS, ARITHMETIC FILAMENTS, EXTERNAL EQUIPMENT, and POWER SUPPLY AND POWER SUPPLY FILAMENTS) to the corresponding cabinets.

Within the power supply cabinet, a single phase from the power supply circuit breaker (S81307) goes to the 220V-110V step-down transformer and the voltage rectifier supplies. Within the Magnetic Tape Cabinet, a single phase from MTS FILAMENT circuit breaker S81302 goes to the 220V-110V step-down transformer. In each cabinet a single phase from one breaker goes to the filament transformer primaries.

The 110 vac from the step-down transformer in the power supply is distributed directly to indicators and voltage testing circuits of the Main Power Cabinet and through fuses and manual control switches on the DC DISTRIBUTION PANEL to external equipment and the Supervisory Control Panel. The 110 vac from the MTS step-down transformer is distributed through fuses and control

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switches to the four magnetic tape units.

From the building power, 110 vac is distributed through a switch box and fuses to the motorized valve in the Blower (90000) Cabinet and to convenience outlets in all cabinets.

A 6.3 vac filament supply voltage is distributed directly to electronic circuits within each cabinet.

(8) DIRECT CURRENT DISTRIBUTION. - From the d-c generators, +250 vdc and -125 vdc are distributed through Disconnect Switch S88007 and d-c fuses to relay panel 81000, then through the overload relays of this panel to d-c voltage regulators. The regulator outputs are then distributed through fuses and distribution switches on the 81600 distribution panel to electronic circuits requiring these voltages.

From the rectifier supplies, -300 vdc is distributed through fuses to the main equipment d-c regulator control units. The +60 vdc and +120 vdc relay supplies are distributed directly to electronic circuits of the Main Power Supply and through fuses and distribution switches on the distribution panel to the Control Cabinet and the Supervisory Control Cabinet. From the Supervisory Control Panel they are distributed to fault and sensing relays within the Electrostatic Storage Cabinet.

The -30 vdc supply is distributed through fuses and switches on the d-c distribution panel to circuits of the control cabinet.

(9) OVERLOAD PROTECTION. - Overload protection is provided by fuses, circuit breakers and overload relays in the a-c distribution system and by fuses and overload relays in the d-c distribution system.

(a) AC FUSES AND CIRCUIT BREAKERS. - The a-c fuses include replaceable cartridge fuses at the primary power input, type 3AG replaceable fuses located in twist-lock fuse holders in the rectifier supply units, filament transformer input circuits, and input lines to the tape units in the magnetic tape storage cabinet.

The circuit breakers are magnetic-thermal overload, trip action units located on the motor-generator assembly panel, the Main Power Cabinet and in the motor-starter circuits of the drum and blower drive motors.

The thermal overload coils are a part of the motor-starter units of the motor-generator, blower, and drum drive motors.

(b) DC FUSES AND OVERLOAD RELAYS. - The d-c fuses include replaceable cartridge fuses in the motor generator output lines, and type 3AG replaceable fuses held in twist-lock fuse holders in the output lines of the rectifier supplies and on the d-c distribution panel.

D-C overload relays are in the +250 vdc and -125 vdc generator output lines, and are located on relay panel 81800 in the Main Power Cabinet.

(c) BLOWN FUSE INDICATION. - A blown fuse is indicated by the glowing of a neon lamp associated with the fuse. Most blown fuse indicators are wired directly across the fuse terminals. However, since an absolute voltage of 80 vdc or greater is required to fire a neon lamp, those lamps indicating blown fuses in lines of less than 80 vdc are tied to sources of sufficient value to provide the necessary voltage.

c. MAGNETIC CORE STORAGE POWER SUPPLY. - The Magnetic Core Power Supply consists of power transformers, a motor-generator set, rectifier supplies, voltage regulators, a power sequence control and power distribution system. This supply controls the application of power to the Magnetic Core Storage System and produces and distributes direct current power. The Magnetic Core Power Supply is shown in block form on the Block Diagram, MC Power Supply. Table 4-10 lists the voltages used by the Magnetic Core Storage System and the origin and destination of each voltage.

(1) TRANSFORMERS. - Filament transformers reduce a single phase of 220 vac to 6.3 vac as filament supply for all units within the core storage system. Output voltages of selected transformers may be reduced to about 5.7 vac by operation of the MC REDUCE HEATER VOLTAGE switch located on the Supervisory Control Panel. Other transformers step up 220 vac and apply the increased voltage to the plate circuit of the rectifier supplies.

(2) MOTOR-GENERATOR. - The Motor-Generator unit consists of a three phase, 10 HP motor driving a pair of direct current generators. The generators produce output voltages of +260 vdc and - 165 vdc which are applied to voltage regulator stages for regulation to lower values.

(3) VOLTAGE RECTIFIERS. - The voltage rectifier units produce voltages of -500, -390, -300 and -290 vdc. All units employ conventional full wave rectifier circuit with choke input filters. The -500 vdc is applied without regulation as reference voltage to the regulator stages of the rectifier supplies. The -300 vdc supply is regulated to -300 vdc and serves as the reference voltage for the DC regulator stages of the generator outputs. The -290 and -390 vdc supplies are regulated to -200 and -300 vdc respectively and distributed to circuits of the Magnetic Core Storage System.

(4) VOLTAGE REGULATION. - The voltage regulators regulate the outputs of the +260 and -165 vdc generators and the -390, -300 and -290 vdc rectifiers. Each regulator unit consists of two or more paralleled 6AS7's (the slave regulators) in conjunction with a control circuit. The control circuit regulates the current through the slave regulators to maintain a constant output voltage. The regulator outputs produce DC voltages of +200, +100, +80, +5, -14, -25, -80, -100, -200 and -300. Voltages dividing networks across the -200 and -300 vdc outputs supplies -220 vdc as the bias voltages of the inhibit and drive circuits.

(5) POWER CONTROL AND SEQUENCING. - The power control and sequencing circuits include the MC Power Panel, the relay sequencing circuits, the power fault circuits and miscellaneous relays and circuits effected during energizing or de-energizing of the core storage power supply.

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In the upper left hand corner of the block diagram and running from left to right are the cam-operated switches S57101 through S57108. In the upper right

hand corner is the Switch Time Distribution Chart. To the left of the chart is the fault circuit, and in the DC distribution system are the bias sensing circuits, voltage sensing relays and thermal overload heaters associated with contacts of this circuit. Contacts controlled by the sequencing circuit are located in both the AC and DC distribution systems. Although the core storage power supply has its own power sequencing circuit, certain power sources are supplied through units of the Main Power Supply as follows: regulated 220 vac to the rectifier circuit and filament transformers, +120 vdc (relay supply) to the bias sensing relays and +60 vdc to the voltage fault circuit. Consequently, the main equipment power should be in process of energizing prior to initiating the MC power ON sequence. By the same token, initiation of the MC power OFF sequence should preceed the main power OFF sequences.

Table 4-11 lists the steps, sub-steps, event, and result incurred during energizing, partial de-energizing or fully de-energizing of the MC Power Supply.

MC Power Supply voltages may also be removed manually by operation of the Sequence Control switch (S57805) located on the MC Power Panel. When re-energizing the power supply after a manual shut down, allow the specified amount of time between switch positions to insure proper warm-up. At the BIAS position, press the CLEAR POWER SUPPLY FAULT button to energize the fault relay before preceeding to the next position.

(6) ALTERNATING CURRENT DISTRIBUTION. - From the MAIN DISCONNECT switch (S88001), three-phase 220 vac is distributed through the main circuit breakers S88009 and S88010 to the power sequence control and the motor generator respectively. A single line of 220 vac from S88009 also supplies the power fault indicators. From the Main Equipment AC Regulator, regulated 220 vac is supplied through circuit breaker S81307 of the Main Power Supply and circuit breakers S57701, S57702 and S57703 of the MC Power Supply to the transformer primaries of the power rectifier circuits and filament supply circuits. Filament supply voltage of 6.3 vac from the filament transformer secondaries is distributed to electronic tube filaments of the core storage and core storage power circuits.

(7) DIRECT CURRENT DISTRIBUTION. - The direct current voltages originate at the direct current generators and the voltage rectifier supplies. The output from the positive generator is distributed through a disconnect switch to relay contacts of the power sequence control. One branch of +260 vdc is distributed through a contact of K57309 and through overload relays K57301, K57302 and K57303 to the +200, +150, +100 and +80 vdc regulators. The other branch is distributed through a contact of K57310 to the +5, -14, and -25 vdc bias regulators. The negative generator output is distributed through a disconnect switch to relay contacts of the power sequence control. One branch is distributed through a contact of K57310 and through overload relay K57304 to the bias regulators, +5, -14 and -25 vdc. The other branch is distributed through a contact of K57309 and overload relays K57305 and K57306 to the -80 and -100 vdc regulators. The output of the -290 vdc rectifier supply is distributed through an output fuse and overload relay K57307 to the -200 vdc regulator. The -390 vdc rectifier output is distributed through a fuse and overload relay K57308 to the -300 vdc regulator. The negative reference supply output is regulated at -300 vdc within the supply and applied through an output fuse to the DC regulator control

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units. The -525 vdc supply is supplied unregulated through a fuse to the -300, -200 and -100 vdc regulators. The regulated voltages +200, +150, +100, +80, +5, -14, -25, -80, -100, -200 and -300 vdc, and the -200 vdc inhibit and driver bias voltages are distributed through fuses and switches of the DC distribution panel to electronic circuits of the Magnetic Core Storage System.

(8) OVERLOAD PROTECTION. - Overload protection is provided by fuses, circuit breakers and thermal overload relays in the AC distribution system and by fuses and overload relays in the DC distribution system.

(a) ALTERNATING CURRENT FUSES, CIRCUIT BREAKERS AND OVERLOAD RELAYS. - The alternating current fuses are located in the primary power input lines (Main Disconnect Switch), the input lines of the power rectifier supplies, and the primary circuits of the filament supply transformers. Circuit breakers are of the magnetic thermal overload type and are located in the input lines to the motor-generator unit and the primary lines to the rectifier and filament transformer supplies. The AC thermal overload relays are a part of the motor generator start circuit. The coils operate contacts of the start circuit if the current to the drive motor becomes excessive.

(b) DIRECT CURRENT FUSES AND OVERLOAD RELAYS. - Direct current fuses are located in output lines of the voltage generators, the rectifier circuits and the voltage regulators. The thermal overload relays are located in the branch lines of the DC generator outputs.

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TABLE 4-7

MAIN POWER SUPPLY VOLTAGES

VOLTAGE	SOURCE	DISTRIBUTION
Primary 220 vac	Building supply	Blower drive motor Drum drive motor Power control and sequencing circuit Induction regulator Motor-generator set
Regulated 220 vac	Induction regulator	110 vac and 6.3 vac transf. pri. Rectifier circuits External equipment
110 vac	Step-down transformers	Bias and -80V fault indicators External equipment Supervisory Control Panel Magnetic tape units
110 vac	Building supply	Convenience outlets Motorized valve
6.3 vac	Step-down transformers	Electronic circuits filaments
3.2 vac	Step-down transformer	Supervisory Control Panel indicators
+250 vdc	Motor-generator	Voltage regulator circuits
+200 vdc	+200 vdc regulator	Electronic circuits
+150 vdc	+150 vdc regulator	Electronic circuits Lo-temp. thermostat circuits
+120 vdc	Rectifier supply	Relay circuits
+100 vdc	+100 vdc regulator	Electronic circuits
+80 vdc	+80 vdc regulator	Electronic circuits
+60 vdc	Rectifier supply	Relay circuits
+5 vdc	+5 vdc regulator	Electronic circuits
-15 vdc	-15 vdc regulator	Electronic circuits
-25 vdc	-25 vdc regulator	Electronic circuits
-30 vdc	Rectifier supply	Electronic circuits
-80 vdc	-80 vdc regulator	Electronic circuits
-125 vdc	Motor-generator	Voltage regulators
-300 vdc	Rectifier supply	d-c regulator control units

TABLE 4-8

NORMAL ON-OFF SEQUENCE OF OPERATIONS
FOR MAIN EQUIPMENT POWER SUPPLY

A. NORMAL ON SEQUENCE

STEP	SUB-STEP	EVENT	RESULT
1		Main Disconnect Switch S88001 closed.	Drum Motor Start K60001 energized. Blower Motor Start K90001 energized.
		K60001 energized.	220 vac applied to drum drive motor.
		K90001 energized.	220 vac applied to blower drive motor.
		BLOWER operating.	Vane tilts within cooling air duct of blower cabinet. Mercury switch S90001 connected to vane closes to provide continuity in the Emergency Interlock Circuit and thereby energizes Emergency relays K81903 in the Main Power Supply and K57103 in the MC Power Supply.
		K81903 energized.	Holds K81903. Provides continuity in the power sequencing circuit. Opens EMERGENCY indicator circuit.
2		NORMAL ON-OFF (start-stop) button S82201 pressed.	Energizes K81901
		K81901 energized.	Holds K81901. Energizes K81902. Energizes cycle timer B81901. Lights TIMER ON indicator I82202.
		K81902 energized.	Closes contacts in fault circuit to allow Fault relay K81815 to be energized by bias (see substep 2F).
		Cycle Timer operating.	Operates switches S81901, S81902, S81903, S81904, S81905, S81906, S81907, and S81908 in sequence over a four-minute period. (See "Switch Time Distribution" chart on Overall Block Diagram, Main Equipment Power Supply.)
	A	S81901 actuated four seconds after NORMAL ON-OFF button is pressed.	Holds cycle timer K81902 and TIMER ON indicator. Opens NORMAL ON-OFF circuit, thereby de-energizing K81901.

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TABLE 4-8 (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
2	A (CONT'D)	K81901 de-energized.	Opens contact in timer circuit. Opens contact in NORMAL ON-OFF circuit.
	B	S81902 actuated.	Allows Emergency relay K81903 to be reset only when timer is in the "home" position.
	C	S81903 actuated.	Energizes K81904 and K81905. Lights INIT. SEQ. indicator I82203.
		K81904 and K81905 energized.	Energizes filament dropping relays K10201, K30201, K60201 and K70201.
		K10201, K30201, K60201 and K70201 energized.	Connects resistors into primary circuits of selected filament transformers.
	D	S81904 actuated.	Energizes relay K81906. Lights LOW HEATER indicator I82204. Starts FIL.HRS. meter M82201.
		K81906 energized.	Energizes main contactor K88001.
		K88001 energized.	220 vac applied to induction regulator which in turn applies regulated 220 vac to all transformer primaries. Allows distribution of 6.3 vac and 5.7 vac filament supply, 110 vac supply, -30 vdc "set" supply, +60 vdc and +120 vdc relay supplies, and 220 vac to external equipment.
	E	S81905 actuated.	Energizes K81907. Lights FULL HEATER indicator I82205.
		K81907 energized.	De-energizes K81904 and K81905. Energizes motor-generator start coil K88002. Applies 220 vac to -300 vdc rectifier circuit. (Neg. Ref. supply) Permits distribution of negative reference supply voltage.

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TABLE 4- 8 (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
2	E (CONT'D)	K81904 and K81905 de-energized.	De-energizes filament dropping relays K10201, K30201, K60201 and K70201.
		K10201, K30201, K60201 and K70201 de-energized.	Shorts filament dropping resistors in primary circuit of selected transformers. Applies full heater voltage to circuits supplied by selected transformers.
		K88002 energized.	220 vac applied to motor-generator drive motor. Allows distribution of -125 vdc generator output to -25 vdc regulator.
	F	S81906 actuated.	Energizes K81908. Lights BIAS indicator I82206.
		K81908 energized.	Energizes K81810. Closes contact in circuit of K81909.
		K81810 energized.	Applies outputs of +250 vdc and -125 vdc generators to the +5 vdc, -15 vdc and -25 vdc regulators, which in turn energize bias sensing relays K81201, K81202, and K81203. Allows distribution of bias voltages.
		K81201, K81202 and K81203 energized.	Energizes fault relay K81815. Opens contacts in circuit of BIAS FAULT indicators I82209, I82210 and I82211.
		K81815 energized.	Holds K81815. Closes contact in circuit of relay K81909. Opens contact in +60 vdc line to B Fault relay.
	G	S81907 actuated.	Energizes relay K81909. Lights POS. VOLTAGES indicator I82207.
		K81909 energized.	Energizes K81809.

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TABLE 4-8 (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
2	G (CONT'D)	K81809 energized.	Applies +250 vdc generator output to the +200 vdc, +150 vdc, +100 vdc and +80 vdc regulators. Applies -125 vdc generator output to the -80 vdc regulator which energizes -80 vdc sensing relays K81811, K81812, K81813, and K81814. Allows distribution of +200 vdc, +150 vdc, +100 vdc, +80 vdc and -80 vdc.
		K81811, K81812, K81813 and K81814 energized.	Closes contacts in fault circuit. Opens contacts in circuit of -80V FAULT indicator I82208.
	H	S81908 actuated.	Opens circuit to power sequence relays.
	I	S81901 actuated.	Stops cycle timer. De-energizes K81902. Extinguishes TIMER ON indicator I82202. Closes contact in circuit of K81901.
		K81902 de-energized.	Allows Fault relay K81515 to be reset only through CLEAR POWER SUPPLY FAULT button S82203. Opens contact in shunt circuit of -80V fault contacts.
		B. NORMAL OFF SEQUENCE	
1		NORMAL ON-OFF button S82201 pressed.	Energizes K81901.
		K81901 energized.	Holds K81901. Energizes K81902. Starts cycle timer B81901. Lights TIMER ON indicator I82202.
		K81902 energized.	Provides continuity in fault circuit.
		Cycle Timer operating.	Operates switches S81901, S81908, S81907, S81906, S81905, S81904, S81903, S81902, and S81901 in sequence over a two-minute period. (See Switch Time

TABLE 4- 8 (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
1	(CONT'D)		Distribution chart on Overall Block Diagram, Main Equipment Power Supply, in Envelope #5, Volume 7).
	A	S81901 actuated.	Holds cycle timer circuit. De-energizes K81901.
		K81901 de-energized.	Opens contact in circuit of timer. Opens contact in NORMAL ON-OFF circuit.
	B	S81908 actuated.	Energizes Power Sequence Relay in main control which in turn causes ABNORMAL CONDITION indicator to glow.
	C	S81907 actuated.	De-energizes K81909. Extinguishes POS. VOLTAGE indicator I82207.
		K81909 de-energized.	De-energizes K81809.
		K81809 de-energized.	Removes +250 vdc generator output from +200 vdc, +150 vdc, +100 vdc and +80 vdc regulator. Removes +200 vdc, +150 vdc, +100 vdc, and +80 vdc from main equipment. Removes -125 vdc generator output from -80 vdc regulator. Removes -80 vdc from main equipment.
	D	S81906 actuated.	De-energizes K81908. Extinguishes BIAS indicator I82206.
		K81908 de-energized.	De-energizes K81810. Opens contact in circuit of K81909.
		K81810 de-energized.	Removes +250 vdc from +5 vdc, -15 vdc and -25 vdc bias regulators. Removes -125 vdc from +5 vdc and -15 vdc regulators; removes +5 vdc and -15 vdc from main equipment.

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TABLE 4-8 (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
1	(CONT'D)		
	E	S81905 actuated.	De-energizes K81907. Extinguishes FULL HEATER indicator I82205.
		K81907 de-energized.	De-energizes motor-generator start coil K88002. Energizes K81904 and K81905. Removes 220 vac from -300 vdc rectifier.
		K88002 de-energized.	Stops motor-generator 88002.
		K81904 and K81905 energized.	Energizes filament dropping relays K10201, K30201, K60201, and K70201.
		K10201, K30201, K60201 and K70201 energized.	Switches filament dropping resistors into primary circuit of selected transformers in the Arithmetic, Control, Magnetic Drum and Magnetic Tape cabinets. Applies low filament voltage to circuits supplied by selected transformers.
	F	S81904 actuated.	De-energizes K81906. Stops FIL. HRS. meter M82201. Extinguishes LOW HEATER indicator I82204.
		K81906 de-energized.	De-energizes main contactor K88001.
		K88001 de-energized.	Removes 220 vac supply to induction regulator, rectifier circuits, 220 vac-110 vac step-down transformers, and filament transformers, which stops distribution of +60 vdc, +120 vdc, -30 vdc, 110 vac and filament supply.
	G	S81903 actuated.	De-energizes K81904 and K81905. Extinguishes INIT. SEQ. indicator I82203.
		K81904 and K81905 de-energized.	De-energizes K10201, K30201, K60201 and K70201.

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TABLE 4- 8 (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
1	G (CONT'D)	K10201, K30201, K60201 and K70201 de-energized.	Opens contacts in primary circuit of selected transformers in Arithmetic, Control, Magnetic Drum and Magnetic Tape cabinets.
	H	S81902 actuated.	Closes contact in circuit of K81903.
	I	S81901 actuated.	De-energizes K81902. Stop cycle timer B81901. Extinguishes TIMER ON indicator I82202. Closes contact in circuit of K81901.
		K81902 de-energized.	Closes contacts in fault circuit.
2		Main Disconnect switch to OFF position.	Removes 220 vac from the equipment. Stops blower and drum drive motor.

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TABLE 4-9

SEQUENCE OF OPERATIONS
FOR VARIOUS VOLTAGE FAILURES OR EMERGENCY CIRCUIT INTERRUPTIONS,
AND CORRECTIVE PROCEDURES REQUIRED (MAIN POWER SUPPLY)

A. FAILURES AND INTERRUPTIONS

STEP	SUB-STEP	EVENT	RESULT
1		+5 vdc FAILURE.	De-energizes K81201.
	A	K81201 de-energized.	Lights +5V FAULT indicator I82211. De-energizes K81815.
	B	K81815 de-energized.	Allows Fault relay to be reset only through CLEAR POWER SUPPLY FAULT button S82203. Energizes B Fault relay in Control Cabinet. De-energizes K81909.
	C	K81909 de-energized.	De-energizes K81809.
	D	K81809 de-energized.	Removes positive d-c voltages. Removes -80 vdc. (-80V Fault relays de-energize, -80V FAULT indicator illuminates.)
2		-15VDC FAILURE	De-energizes K81202.
	A	K81202 de-energized.	Lights -15V FAULT indicator I82210. De-energizes K81815.
	B	K81815 de-energized.	See step 1, sub-steps B,C, and D of this table (part A).
3		-25VDC FAILURE	De-energizes K81203.
	A	K81203 de-energized.	Lights -25V FAULT indicator I82209. De-energizes K81815.
	B	K81815 de-energized.	See step 1, sub-steps B,C, and D of this table (part A).
4		-80 VDC FAILURE.	De-energizes -80V Fault relay K81811, K81812, K81813, or K81814.
	A	K81811, K81812, K81813 or K81814 de-energized.	Lights -80V FAULT indicator I82208. De-energizes K81815.

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TABLE 4-9 (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
4	(CONT'D)		
	B	K81815 de-energized.	See step 1, sub-steps B, C, and D of this table (part A).
5		+250 vdc Overload Relay K81801, K81802, K81803 or K81805 tripped.	K81815 de-energized.
	A	K81815 de-energized.	See step 1, sub-steps B, C, and D of this table (part A).
6		-125 vdc Overload Relay K81805, K81806, K81807 or K81808 tripped.	De-energizes K81809 and K81810.
	A	K81809 and K81810 de-energized.	Removes generator output from all regulators except negative generator supply to -25 vdc regulator. Bias and -80 vdc sensers operate to de-energize K81815.
	B	K81815 de-energized	See step 1, sub-steps B, C, and D of this table (part A).
7		Sail (vane) Switch actuated, Hi-Temp Thermostat operates, Cabinet Interlock opened, or an EMERGENCY switch is pressed.	Emergency relay K81903 de-energized.
	A	K81903 de-energized.	Lights EMERGENCY indicator I82201. Removes 220 vac to power sequence relays which in turn removes all power to the equipment with the exception of 220 vac to the drum and blower drive motors. Allows emergency relay to be reset only when timer has returned to Home position.

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TABLE 4-9 (CONT'D)

B. CORRECTIVE PROCEDURE FOR ALL VOLTAGE FAILURES

STEP	SUB-STEP	EVENT	RESULT
1		Set SEQUENCE CONTROL switch S82205 to POS. VOLTAGES position.	Provides continuity in Fault circuit. Energizes Power Sequence relay which causes ABNORMAL CONDITION indicator to glow.
2		Press CLEAR POWER SUPPLY FAULT button S82203.	Energizes K81815.
		K81815 energized.	Holds K81815. Energizes K81909. De-energizes B Fault relay.
		K81909 energized.	Energizes K81809.
		K81809 energized.	Allows distribution of positive d-c and -80 vdc voltages. Energizes K81811, K81812, K81813 and K81814.
		K81811, K81812, K81813 and K81814 energized.	Closes -80vdc fault contacts in fault circuit. Extinguishes -80V Fault indicator I82208.
3		Set Sequence Control switch S82205 to OPERATE position.	Opens circuit to power sequence relay. Extinguishes ABNORMAL CONDITION indicator. Opens contact in shunt circuit of -80 vdc fault contacts.

C. CORRECTIVE PROCEDURE FOR EMERGENCY SHUT-DOWN

1		Press NORMAL ON-OFF button S82201.	K81901 energized.
	A	K81901 energized.	Energizes cycle timer B81901 which then returns to home position.
	B	B81901 in home position.	Equipment power returned to condition commensurate with completion of step 1, Normal On sequence, Table 4-8 (part A).
2		Press NORMAL ON-OFF button S82201.	See step 2, Normal-On sequence, Table 4-8.

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TABLE 4-10
MC POWER SUPPLY VOLTAGES

VOLTAGE	SOURCE	DISTRIBUTION
Primary 220 vac	Building supply	Power sequence control. Motor-generator set.
Regulated 220 vac	Main Equipment AC regulator	Voltage rectifiers. Filament transformer primaries.
6.3 vac	Filament transformers	Electronic circuit filaments.
+260 vdc	Motor-generator	Voltage regulators.
+200 vdc	+200 vdc regulator	Electronic circuits.
+150 vdc	+150 vdc regulator	Electronic circuits.
+120 vdc	Rectifier supply (main equipment power).	Bias Sensing relays
+100 vdc	+100 vdc regulator	Electronic circuits.
+80 vdc	+80 vdc regulator	Electronic circuits.
+60 vdc	Rectifier supply (main equipment power).	Voltage fault circuit
+5 vdc	+5 vdc regulator	Electronic circuits.
-14 vdc	-14 vdc regulator	Electronic circuits.
-80 vdc	-80 vdc regulator	Electronic circuits.
-100 vdc	-100 vdc regulator	Electronic circuits.
-200 vdc	-200 vdc regulator	Electronic circuits.
-220 vdc	R57916 & R57917	Electronic circuits.
-290 vdc	Rectifier Supply	-200 vdc regulator
-300 vdc	Rectifier supply (ref.)	-300 vdc regulator.
-300 vdc	-300 vdc regulator	DC voltage regulator control units.
-300 vdc	-300 vdc regulator	Electronic circuits.
-390 vdc	Rectifier supply	-300 vdc regulator.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR

MAGNETIC CORE POWER SUPPLY

A. NORMAL ON

STEP	SUB STEP	EVENT	RESULT
1		Main Switch (S88001) ON	Energizes circuits of the Main Power Supply Energizes MC Emergency relay K57103.
		K57103 Energized	Holds K57103. Provides continuity to sequence control switch. Opens contact in EMERGENCY OFF indicator circuit.
2		Main Power NORMAL ON-OFF button pressed	Initiates Main Power ON sequence.
3		MC Power NORMAL ON-OFF button pressed	Energizes K57101
		K57101 energized.	Holds K57101. Energizes K57102. Starts cycle timer (B57101). Lights TIMER ON indicator.
		K57102 energized	Provides continuity in MC power fault circuit.
		CYCLE TIMER B57101 running.	Operates switches S57101, S57102, S57103, S57104, S57105, S57106, S57108, and S57101 in sequence over a four-minute period. (See switch time distribution chart on block diagram.)
	A	S57101 actuated.	Holds cycle timer, lights TIMER ON indicator, and energizes K57102. De-energizes K57101.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR

MAGNETIC CORE POWER SUPPLY. (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
		K57101 de-energized	Opens contacts in start circuit and cycle timer circuit.
	B	S57102 actuated	Allows Emergency relay to be reset only when timer is in "home" position.
	C	S57103 actuated	Energizes K57104. Lights INIT. SEQ. indicator.
		K57104 energized	Energizes K55701 through normally-closed contacts of K57106.
		K55701 energized	Opens contacts in 220 vac lines to MC filament transformer primaries thus inserting filament dropping resistors into the primary circuits.
	D	S57104 actuated	Energizes K57105. Lights LOW HEATER indicator. Starts HTR. HRS. meter.
		K57105 energized	Energizes AC Contactor K57701.
		K57701 energized.	Applies regulated 220 vac from the main power supply to the -500 vdc reference supply, filament transformer primaries of the -300 vdc reference supply and regulator circuits, and, through the limiting resistors, a reduced voltage to the MC filament transformer primaries. The output of the latter transformers is reduced to about 5-7 vac. 220 vac is also supplied to the -500 vac reference supply which in turn applies -500 vdc to the control circuits of the rectifier supply regulators.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR MAGNETIC CORE POWER SUPPLY (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
	E	S57105 actuated.	Energizes K57106. Lights FULL HEATER indicator.
		K57106 energized.	Energizes MG Start relay (K88003). De-energizes K55701. Applies 220 vac to -300 vdc rectifier supply which in turn applies regulated -300 vdc to the regulator control circuits.
		K88003 energized.	Applies 220 vac to the motor generator.
		K55701 de-energized	Closes contacts in 220 vac lines to MC filament transformer primaries thus shunting limiting resistors and permitting full heater supply to MC filaments.
	F	S57106	Energizes K57107. Lights BIAS indicator.
		K57107 energized	Closes contact in circuit of K57108 and K57109. Energizes K57310.
		K57310 energized	Closes contacts in generator output lines to bias circuits. The bias voltage +5 vdc, -14 vdc and -25 vdc energize the vias sensing relays K81201, K81202 and K81203, and provide continuity in MC power fault circuit that energizes Bias Fault relay K57312.
		K81201, K81202 and K81203 energized.	Opens contacts in the bias fault indicator lines. Provides continuity in the bias fault circuit thus energizing Bias Fault relay K57312 through the closed contacts of K57102.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR

MAGNETIC CORE POWER SUPPLY (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
		K57312 energized.	Opens contacts in line to equipment Fault Control. Closes holding contact in bias fault circuit. Closes contacts in circuit of relays K57108 and K57109.
	G	S57107 actuated	Energizes K57108 through closed contacts of K57107 and K57312. Lights. POS. VOLTS indicator.
		K57108 energized.	Energizes K57309. Energizes K57315.
		K57309 energized	Closes contacts in output lines of DC generators. Voltage outputs are regulated to +200, +150, +100, +80, -80 and -100 vdc, and distributed to electronic circuits of the MC system; +100 vdc energizes K57313, -80 vdc energizes K57311.
		K57315 energized	Applies 220 vac to +290 vdc and +390 vdc rectifier supplies which in turn are regulated to -200 and -300 vdc respectively. Voltages are distributed through the DC distribution panel to circuits of the MC system.
		K57313 energized.	Closes contact in MASTER CLEAR circuit to produce MASTER CLEAR signal.
		K57311 energized	Closes contacts in circuit of K57312. Opens contacts in circuit of -80 vdc FAULT indicator.
	H	S57108 actuated	Energizes K57109. Lights OPERATE indicator.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR

MAGNETIC CORE POWER SUPPLY (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
		K57109 energized	Opens contacts in +200 vdc and -100 vdc distribution lines. Energizes K57314.
		K57314 energized	Opens contact in MASTER CLEAR circuit.
	I	S57101 actuated	Allows K57101 to be re-energized with start of the OFF Cycle. Stops timer motor. Extinguishes TIMER ON indicator. De-energizes K57102.
		K57102 de-energized	Opens by-pass contacts in bias fault circuit. Fault relay can be energized only through contacts of CLEAR POWER SUPPLY FAULT button.
		B. NORMAL OFF	
1		NORMAL ON-OFF button pressed.	Energizes K57101.
		K57101 energized	Holds K57101. Energizes K57102. Holds K57102. Starts cycle timer (B57101). Lights TIMER ON indicator.
		K57102 energized	Closes contacts in fault circuit which prevents fault relay K57312 from de-energizing with loss of -80 vdc.
		Cycle timer running	Actuates switches S57101, S57108, S57107, S57106, S57105, S57104, S57103, S57102 and S57101 in that sequence over a two-minute period.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR

MAGNETIC CORE POWER SUPPLY (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
	A	S57101 actuated.	De-energizes K57101.μ Holds K52702, and cycle timer, and lights TIMER ON indicator.
		K57101 de-energized.	Permits MC power to be re-energized only through NORMAL ON-OFF button.
	B	S57108 actuated.	De-energizes K57109. Extinguish OPERATE indicator.
		K57109 de-energized.	Removes +200 vdc and -100 vdc operate voltages. De-energizes K57314.
		K57314 de-energized.	Closes contact in MASTER CLEAR line.
	C	S57107 actuated.	De-energizes K57108. Extinguishes POS. VOLTAGE indicator.
		K57108 de-energized.	De-energizes K57309. De-energizes K57315.
		K57309 de-energized.	Removes generator output voltages to +200, +150, +100, +80, -80 and -100 vdc regulators.
		K57315 de-energized.	Removes 220 vac to -290 and -390 vdc rectifier supplies.
	D	S57106 actuated.	De-energizes K57107. Extinguishes BIAS indicator.
		K57107 de-energized.	De-energizes K57310. Opens contact in circuit of K57108 and K57109.
		K57310 de-energized.	Removes generator output voltages from bias regulators. Bias sensing relays de-energize, opening circuit to K57312.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR

MAGNETIC CORE POWER SUPPLY (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
		K57312 de-energized.	Re-sets contacts to normal position.
	E	S57105 actuated.	De-energizes K57106. Extinguishes FULL HEATER indicator.
		K57106 de-energized.	Energizes K55701. De-energizes MG Start relay (K88003). Removes 220 vac from -300 vdc reference supply.
		K55701 energized.	Shunts filament dropping resistors into primary circuit of MC filament transformers.
		K88003 de-energized.	Removes 220 vac supply to MG set.
	F	S57104 actuated.	De-energizes K57105. Extinguishes LOW HEATER indicator. Stops HTR. HRS. meter.
		K57105 de-energized.	De-energizes AC Contactor (K57701).
		K57701 de-energized.	Removes regulated 220 vac from -500 vdc rectifier circuit, MC filament transformers and MC Power Supply filament transformers.
	G	S57103 actuated	De-energizes K57104. Extinguishes INIT. SEQ. indicator.
		K57104 de-energized.	De-energizes K55701.
		K55701 de-energized.	Close contacts in primary circuit of MC filament transformers.
	H	S57102 actuated.	Contacts close, creating energizing path for Emergency relay during next ON cycle.

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TABLE 4-11

NORMAL ON-OFF SEQUENCE OF OPERATIONS FOR

MAGNETIC CORE POWER SUPPLY (CONT'D)

STEP	SUB-STEP	EVENT	RESULT
	I	S57101 actuated.	De-energizes K57102. Stops cycle timer. Extinguishes TIMER ON indicator. Provides energizing path for K57101 when NORMAL ON-OFF is pressed for POWER ON sequences.
		K57102 de-energized.	Opens contacts in bias fault circuit.
	J	Main Disconnect Switch (S88001) Off	Removes AC power from the entire equipment. De-energizes Emergency relay K57103.
		K57103 de-energized.	Opens contact in sequence control switch circuit and relay holding circuit. Closes contact in EMERGENCY OFF indicator circuit.

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TABLE 4-12

SEQUENCE OF OPERATIONS FOR VARIOUS VOLTAGE FAILURES OR EMERGENCY CIRCUIT INTERRUPTIONS IN THE MC POWER SUPPLY

A. BIAS, -80 VDC, OR POSITIVE DC OVERLOAD FAULT

STEP	SUB-STEP	EVENT	RESULT
1	A	K81201, K81202, K81203 K57311, K57301, K57302 or K57303 de-energized.	De-energizes K57312. Lights appropriate voltage FAULT indicator if caused by Bias or -80 V Fault.
	B	K57312 de-energized.	De-energized K57109 and K57108. Closes contact in circuit to equipment Fault Control.
	C	K57109 de-energized.	Remover +200 vdc and -100 vdc voltages. De-energizes K57314.
	D	K57314 de-energized.	Closes contact in master clear line.
	E	K57108 de-energized.	De-energizes K57309 and K57315.
	F	K57309 de-energized.	Removes generator supply to +200, +150, +100, +80, -80 and -100 vdc regulators.
	G	K57315 de-energized.	Removes 220 vac to -290 and -390 vdc rectifier supplies.

B. NEGATIVE DC OVERLOAD FAULT

1	A	Overload relay K57304, K57305, K57306, K57307 or K57308 de-energized.	De-energizes K57309 and K57310.
	B	K57309 and K57310 de-energized.	Removes generator supply to DC regulators. As a consequence, the bias sensing relays de-energize, creating a repeat of part A above.

Note: To re-energize the MC power after bias or overload failure, correct the cause, turn the power sequence switch to POS. VOLTAGE, press the CLEAR POWER SUPPLY FAULT button, then return the SEQUENCE switch to OPERATE.

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TABLE 4-12

SEQUENCE OF OPERATIONS FOR VARIOUS VOLTAGE FAILURES OR EMERGENCY CIRCUIT INTERRUPTIONS IN THE MC POWER SUPPLY

C. EMERGENCY OFF

STEP	SUB-STEP	EVENT	RESULT
1	A	Emergency interlock circuit open, (sail switch open, high temperature thermostat operates, or an EMERGENCY button is pressed).	De-energizes Emergency relay K57103.
	B	K57103 de-energized.	Opens contact in circuit of power sequence switch thus causing all power sequence relays to de-energize thereby removing all power to the MC system with the exception of 220 vac to the power supply START circuit, cycle timer, and EMERGENCY OFF indicator.
			Lights EMERGENCY OFF indicator.

Note: To re-energize the equipment after an emergency stop, return the cycle timer to the "home" position, then re-energize the equipment through the NORMAL ON cycle.

11. COOLING SYSTEM

a. COOLING AIR. - The computer is cooled by water-cooled air streams which enter each of the cabinets through adjustable overlapping grills at the bottom of each bay and leave through a grill at the top of each bay. The air, drawn from the room through dust-removing oil-coated metal filters, is passed over water-cooled coils, then pumped into a plenum chamber by two centrifugal blowers. The air pressure in the plenum chamber is constant but the flow of air through a particular bay is regulated by adjusting the overlap of the grills located at the bottom of that bay. Temperature of the cooling air is maintained at 64°F by the air temperature controller located in the bay behind the regulator.

Under normal conditions the temperature of the cooling air will be raised from 64°F to about 82°F maximum during the heat exchange. Should the exhaust temperature exceed 100°F in any of the tube channels a "Klixon" thermostat mounted at the top of the channel will break contact and create an A FAULT computer stop. This is indicated by operation of the TEMPERATURE indicator on the Supervisory Control Panel and the amber light located above the overheated channel. The thermostat will reset automatically when the temperature is reduced to 90°F (see sub-paragraph 12b (2) of this section).

Each bay, except the bay containing the Supervisory Control Panel, contains a high temperature thermostat mounted above the channel having the highest ambient temperature. This thermostat breaks contact if the exhaust temperature exceeds 120°F. Operation of a high temperature thermostat creates an Emergency computer stop which shuts down the power supply.

A high temperature fault is indicated by operation of the EMERGENCY OFF indicators on the Main and MC Power Supply panels. All high temperature thermostats must be reset manually.

b. COOLING WATER. - The cooling water requirement for the computer depends upon the room temperature and the temperature of the water supplied. Under conditions where the temperature of the water is 50°F, the relative humidity 50%, and the room temperature a maximum of 82°F, a water pressure of 30 psi is needed to provide the 41 gallons per minute necessary for cooling the air.

The water, supplied from the cooling water main, passes through a pressure sensitive "Vacuumstat" valve and a motorized valve in the water intake line. It is then circulated through cooling coils located on each side of the blower bay and finally discharged through a common pipe to the sewer. Condensate from the cooling coils is drained off to the sewer through a 1/2 inch pipe. Water flow through each of the cooling coils is maintained equal by equalizing valves located in the cooling coil discharge pipes. Temperature of the water being discharged from the cooling coils may be checked by observing the thermometers mounted in the discharge pipes near the equalizing valves. The "Vacuumstat" initiates an A FAULT if the water pressure is drastically reduced. The water fault is indicated by the glowing of the WATER indicator on the Supervisory panel. The motorized valve is controlled by an air temperature controller located in the blower cabinet and opens or closes to maintain sufficient cooling.

12. PROTECTIVE INTERLOCKS

a. GENERAL. - The ERA 1103 computer contains two protective interlock systems, as shown on the Block Diagram, Protective Interlocks, in Envelope #6 of Volume 7. They are named as follows: the Fault Interlocks, designed primarily to protect the equipment; the Emergency Interlocks, designed to protect both the equipment and personnel. The operation of either of these interlock systems will stop the computer program and/or remove equipment power.

b. FAULT INTERLOCKS. - The Fault Interlocks consist of a Water Pressure Switch in the Blower (90000) Cabinet and Low Temperature Thermostats distributed throughout the computer. They are connected in two separate circuits and operate as follows:

(1) WATER PRESSURE SWITCH. - This mechanism, connected to the input water line of the cooling system, contains a diaphragm that is positioned by water pressure and a set of contacts that is operated by the diaphragm. During normal operation the contacts close to energize the Water Fault relay located in the Control (30000) Cabinet. When water pressure drops the contacts open to de-energize the Water Fault relay (K30072). This relay, in de-energizing, illuminates the WATER FAULT indicator on the Supervisory Control Panel and energizes the A Fault relay. The subsequent A Fault stops the computer program until water pressure is restored and the START button on the Supervisory Control Panel is pressed.

(2) LOW TEMPERATURE THERMOSTATS. - This circuit consists of 98 bimetal, disc type thermostats distributed through the equipment such that one is located above each vertical row of plug-in chassis. Connected in series, they provide a ground for the Temperature Fault relay (K30074) located in the Control (30000) Cabinet and thus keep it energized during normal operation.

A thermostat is actuated when the exhaust temperature of any tube channel reaches 100°F. Should this happen, the Temperature Fault relay is de-energized which in turn illuminates the TEMPERATURE FAULT indicator on the Supervisory Control Panel, lights an amber indicator above the over-heated channel, and energizes the A Fault relay. The subsequent A Fault stops the computer program until the proper temperature is restored and the START button is pressed. The tripped thermostat will reset automatically when the exhaust temperature drops to 90°F.

c. EMERGENCY INTERLOCKS. - The Emergency Interlocks consist of cabinet door switches, high temperature thermostats, vane switches in the main air duct,

and two EMERGENCY OFF pushbutton switches. They are all connected in series between 220 vac and two parallel Emergency relays: K57103 in the MC Power Supply and K81903 in the Main Power Supply. Should the Emergency Interlock circuit be broken by any one of the switches both Emergency relays de-energize which, in turn, will remove all Main and MC power.

(1) CABINET DOOR INTERLOCK SWITCHES. - Each cabinet door interlock is composed of two switches. One is a plunger type microswitch which is the actual interlock, the other a push button type microswitch in parallel with the first one so that the interlock may be temporarily by-passed, making it possible to open a cabinet door without breaking the Emergency Interlock circuit. There are 36 pairs of these switches throughout the equipment; one pair is mounted on the frame of each cabinet door. The plunger of the one switch protrudes into the channel in which the door runs such that when the door is closed the plunger is depressed. When the plunger is depressed, the switch is closed to provide continuity in the Emergency Interlock circuit. The other switch is mounted such that the button which operates it protrudes outside the cabinet. When it is desired to open a cabinet door without creating an emergency stop the steps listed below must be followed.

Step 1. Press and hold in the by-pass button mounted on the frame adjacent to the door handle.

Step 2. Open the door and pull out the plunger located near the upper corner of the door opening.

Step 3. After pulling out the plunger, release the by-pass button.

Step 4. To close the door, press the by-pass button and hold in until the door is fully closed.

(2) HIGH TEMPERATURE THERMOSTATS. - There are eleven High Temperature Thermostats in the Emergency Interlock circuit which are identical to the Low Temperature Thermostats in the Fault Interlock circuit except they operate at 120°F rather than 100°F and must be reset manually after they have been tripped. There is one located in each bay (with the exception of the Supervisory Control Bay & Blower Cabinet) at the top of the tube channel having the highest ambient temperature. Should the exhaust temperature of a particular bay exceed 120°F, the High Temperature Thermostat associated with that bay will trip which will break the Emergency Interlock circuit and thereby remove all power from the computer. As stated previously, all High Temperature Thermostats must be manually reset by pressing a plunger connected to each thermostat.

There is no indicator lamp connected to the High Temperature Thermostats to show when a particular thermostat has been tripped. It is sufficient that before High Temperature Thermostat operates one or more Low Temperature Thermostats will have been operated and thereby will indicate where the overheated bay is located.

(3) BLOWER VANE SWITCHES. - Mercury switches, operated by air vanes mounted in the main air ducts of the Blower (90000) Cabinet, provide interlock protection for the computer in the event a blower should fail. The air vanes, struck by moving air, maintain a torque on a linkage that close mercury switches as long as the blowers are operating. When the mercury switch contacts are closed, continuity is provided in the Emergency Interlock circuit. Should a blower stop, the weight of the vane allows one of the mercury switches to open and thereby creates an emergency power shutdown in the computer.

(4) EMERGENCY OFF SWITCHES. - On both the Main Power Supply control panel and the MC Power Supply control panel is a red EMERGENCY OFF pushbutton switch. When either one of these switches is manually actuated, the Emergency Interlock circuit is broken.