TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 990/5 Computer

Hardware User's Manual

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NOTE

ALL REFERENCES TO TMS9903 SYNCHRONOUS COMMUNICATIONS CONTROLLER (SCC) OR COMMUNICATIONS PORT 3 ARE RESERVED FOR FUTURE ENHANCEMENTS.

PREFACE

The Texas Instruments Model 990/5 Microcomputer is a complete basic computer packaged on a single, full-size, printed circuit board. The Central Processing Unit (CPU) for the 990/5 is the Model TMS 9900 Microprocessor made by Texas Instruments.

This manual provides information on the 990/5 microcomputer and is directed to both the Original Equipment Manufacturer (OEM) equipment purchaser and the end-user.

Information in this manual is divided into the following sections:

I General Description — Provides an overview description of the Model 990/5 Microcomputer outlining hardware, firmware and software features.

II Installation — Outlines procedures for unpacking the microcomputer from its shipping container, installing it in various chassis configurations, and establishing the switch settings and jumper connections required for various configurations.

III Operation — Describes controls and indicators for 990/5 front panels, general operating procedures for the front panel, and loading procedures.

IV Programming Considerations — Contains information on programming considerations relative to the TMS 9900 microprocessor instruction set, the communications ports address bit assignments, and the asynchronous clock rate selection.

V Interface Requirements — Assists users and OEM equipment purchasers in interfacing peripherals with the 990/5 microcomputer.

Additional information related to the 990/5 microcomputer may be found in the following documents:

Title	Part Number
Model 990 Computer Diagnostic Handbook	945400-9701
Model 990/5 Computer Field Maintenance Manual	946295-9701
Model 990/5 Computer Depot Maintenance Manual	946296-9701
Model 990 Computer Peripheral Equipment Field Maintenance Manual	945419-9701
Model 990 Computer Family Maintenance Drawings:	
Volume I, Processors	945421-9701
Volume II, Peripherals	945421-9702

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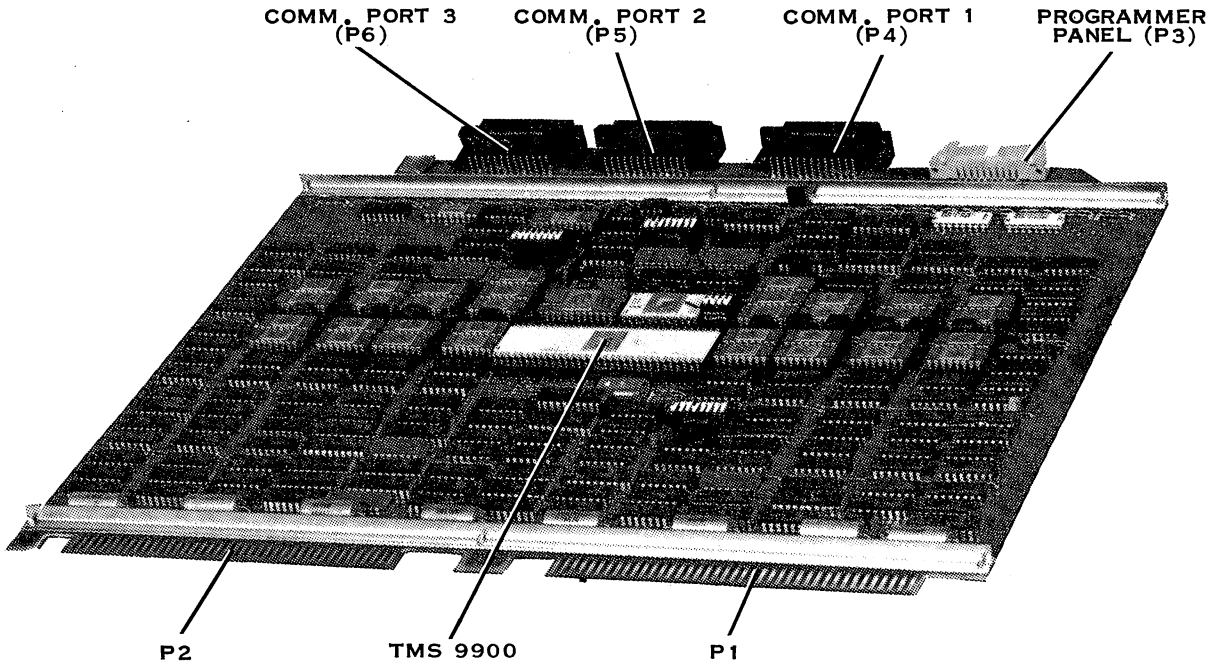

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Figure 1-1. 990/5 Microcomputer Printed Circuit Board

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Texas Instruments Model 990/5 Microcomputer is a complete basic computer packaged on a single, full-size (362 × 274.3 mm or 14.25 × 10.80 in.) printed circuit board (see figures 1-1 and 1-2). The Central Processor Unit (CPU) for the 990/5 is the Model TMS 9900 Microprocessor made by Texas Instruments. In addition to the TMS 9900 microprocessor, the 990/5 microcomputer board provides the following standard features:

- TMS 4116 Dynamic Random-Access Memory (RAM) elements for a choice of 32 or 64K bytes of on-board memory.
- TMS 4700 Read-Only Memory (ROM) elements; the first 1K bytes of ROM are used for self-test and the other 1K bytes for loader programs.
- TMS 9902 Asynchronous Communications Controller (ACC) elements (two) provide interface between the 990/5 and serial, asynchronous communications channels.
- TMS 9903 Synchronous Communications Controller (SCC) element to provide interface between synchronous or asynchronous communications channels.
- Communications Register Unit (CRU) interface logic for serial I/O transfers with front panel and other CRU devices, e.g., 743 KSR, 810 Printer, single-density floppy disk, etc.
- TILINE* interface logic for parallel data transfers to high speed devices such as magnetic tape units, moving head disk and dual-density floppy disk units, etc.
- Host-slave interface logic to transfer interrupts between host processor located in slot 1 and slave processor(s) in other card slots. (Host is always located in slot 1.)
- Clock elements to supply microprocessor and communications controllers with timing signals.
- Vectored interrupt logic to accommodate 16 levels of priority.

1.2 EQUIPMENT DESCRIPTION

A simplified block diagram of the Model 990/5 microcomputer is shown in figure 1-3. Each of the blocks shown in this figure is described in the following paragraphs. The blocks shown in the diagram are described from left to right.

* Trademark of Texas Instruments Incorporated

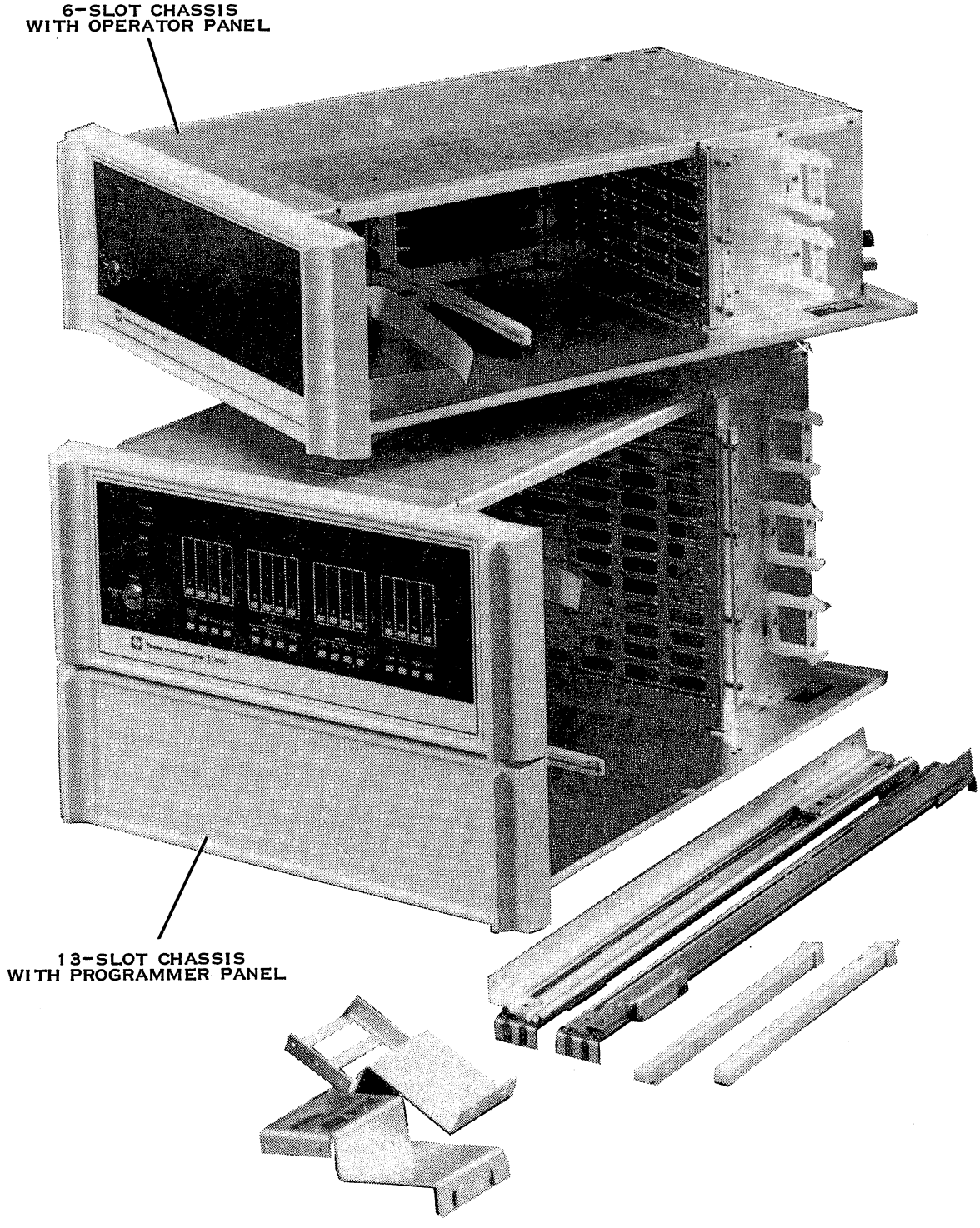


Figure 1-2. 990/5 Chassis Assembly (6- and 13-Slot Chassis)

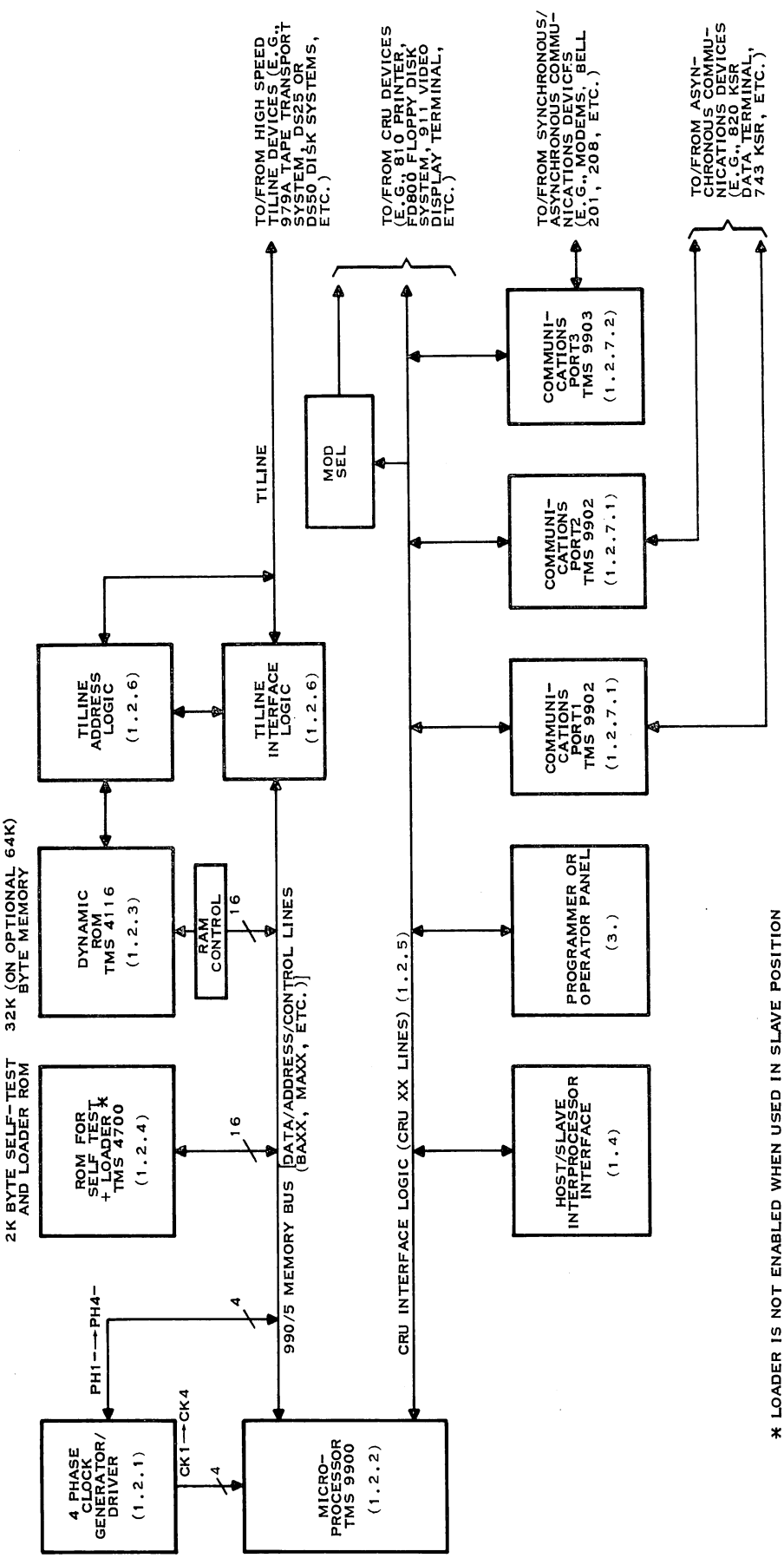


Figure 1-3. Model 990/5 Microcomputer Block Diagram

1.2.1 FOUR-PHASE CLOCK GENERATOR/DRIVER. The clock generator consists of an oscillator, a divide-by-four counter, and a second divide-by-four counter with gating to generate four clock phases. These clock phases provide clock inputs to the TMS 9900. The frequency of the internal oscillator is established by a 64 MHz quartz crystal and an LC circuit. The LC circuit connected to the tank inputs selects the desired crystal overtone. Crystal frequency (fundamental) is 64 MHz; output frequency to the TMS 9900 is 4 MHz. A timing diagram of the four-phase clock generator is shown in figure 1-4.

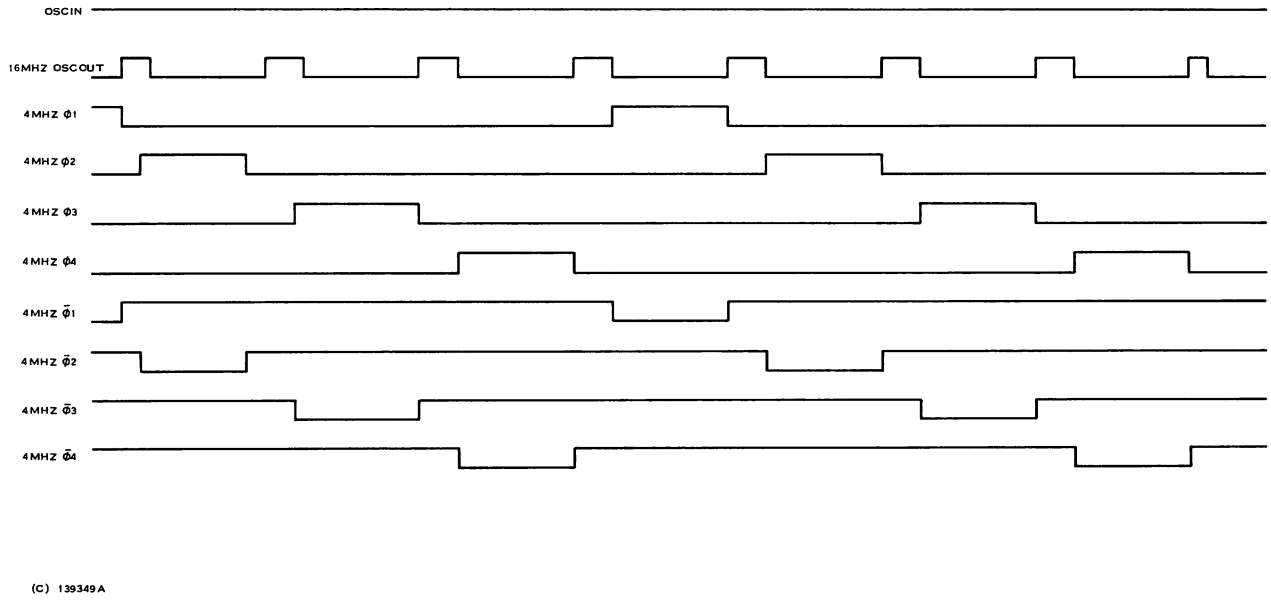


Figure 1-4. Clock Generator Timing Diagram

1.2.2 TMS 9900 MICROPROCESSOR. The TMS 9900 is a 16-bit microprocessor on an integrated circuit chip that functions as a full-scale, general purpose computer when combined with an external memory and a clock source. In addition to its compact size, the microprocessor offers features such as:

- Vectored interrupts and memory located register files for efficient context switching (a switch from one subprogram to another)
- Two I/O channels that include a command-driven (CRU) channel
- A 16-bit direct memory access channel (also buffered to form TILINE address lines external to the TMS 9900)
- Full 64K bytes of memory addressing space
- A flexible set of 69 instructions (five of which are implemented external to the chip and will be explained in paragraph 1.2.2.5).

A summary of TMS 9900 microprocessor characteristics is provided in table 1-1.

Table 1-1. TMS 9900 Microprocessor Characteristics

Item	Characteristic
Word size	16 bits
Maximum memory	64K bytes
Clock rate	4 MHz
Addressing modes	Immediate
	Workspace register
	Workspace register indirect
	Symbolic memory (direct)
	Indexed memory
	Workspace register indirect auto-increment
	Program Counter Relative
	CRU Relative
Interrupts	16 interrupt levels
Working Registers	16 total
Input/Output	Direct (CRU) and Direct Memory Access (DMA)
Address bus	15 bits
Data bus	16 bits
Power	+12 Vdc, ±5 Vdc
Package	64 pins, dual in-line package
Technology	N-channel silicon gate
Instruction set	5 general address modes, set includes multiply and divide

1.2.2.1 Microprocessor Architecture. The memory word of the TMS 9900 is 16 bits in length. Each word is also defined as 2 bytes of 8 bits each. The instruction set of the TMS 9900 allows both word and byte operands. Thus, all memory word locations are on even byte address boundaries. Byte instructions can address either the even or odd byte of a word. The memory space is 65536 bytes (or 32768 words). Word and byte formats are shown in figure 1-5.

1.2.2.2 Registers and Memory. The TMS 9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal hardware registers as program data registers. Dedicated TMS 9900 memory addresses are shown in figure 1-6. The first 32

words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory. Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the interrupt mask level and status information pertaining to the instruction operation. Each bit in the register signifies a particular function or condition that exists in the microprocessor. Figure 1-7 illustrates the bit position assignments. Some instructions use the status register to check for a prerequisite condition, others affect the values of the bits in the register, and others load the entire status register with a new set of parameters. The workspace pointer register (WP) contains the address of the first word in the currently active set of workspace registers. A workspace register file occupies 16 contiguous memory words in the general memory area (see figure 1-6). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. Some workspace registers take on special significance during execution of certain instructions. Table 1-2 lists each of these dedicated workspace registers and the instructions that use them. During instruction execution, the processor addresses any registers in the workspace by adding the register number to the contents of the workspace pointer as shown in figure 1-8.

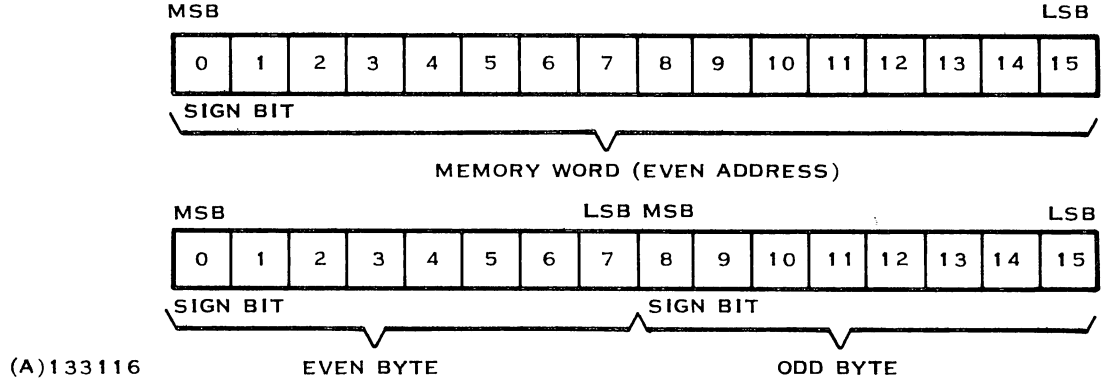


Figure 1-5. Microprocessor Word and Byte Format

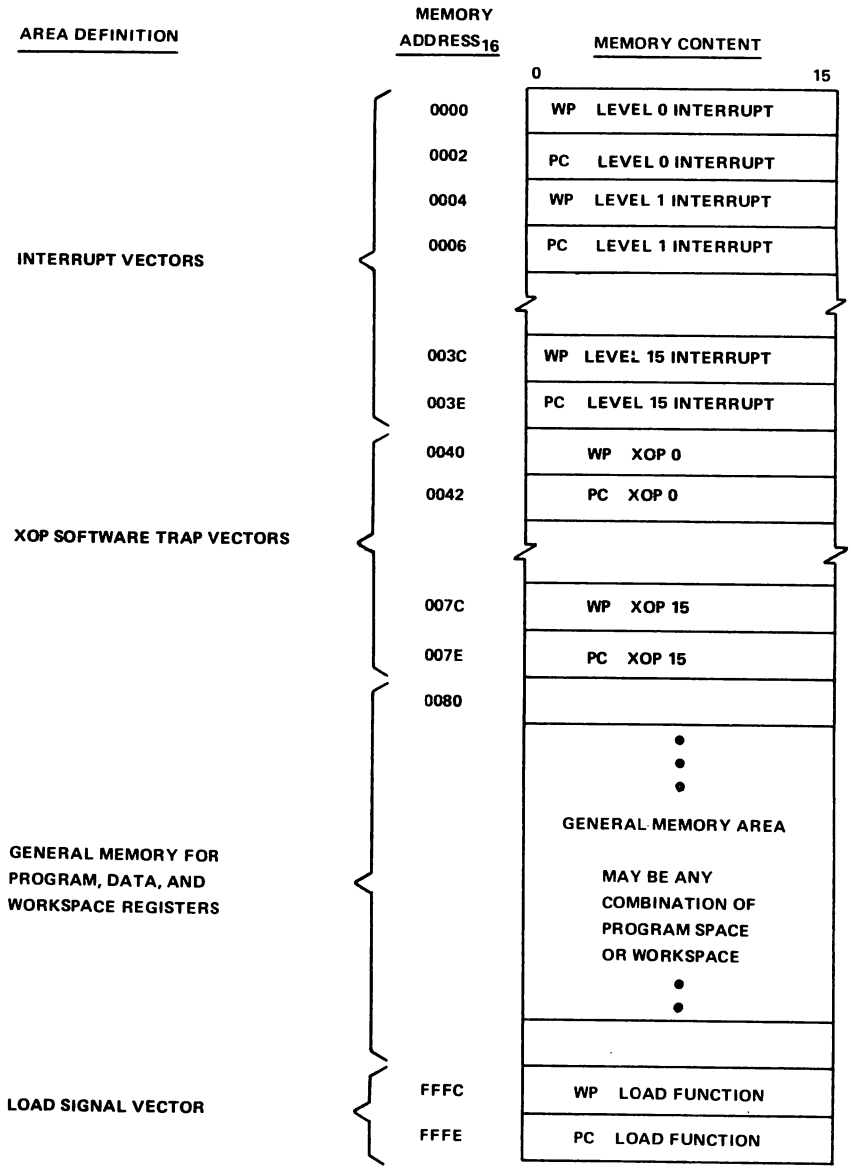


Figure 1-6. Dedicated Memory Addresses

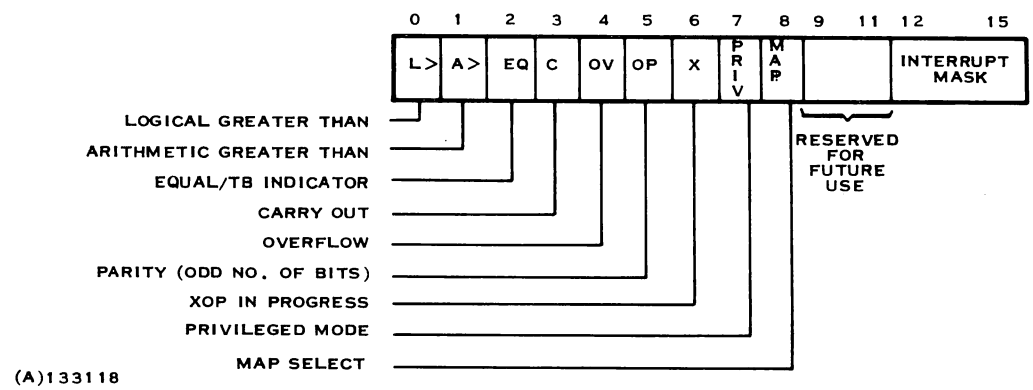


Figure 1-7. Status Register Bit Assignments

Table 1-2. Dedicated Workspace Registers

Register No.	Contents	Used During
0	Shift count (optional)	Shift instructions (SLA, SRA, SRC and SRL)
11	Return address	Branch and Link Instruction (BL)
	Effective address	Software implemented Extended Operation (XOP)
12	CRU base address	CRU instructions (SBO, SBZ, TB, LDCR and STCR)
13	Saved WP register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
14	Saved PC register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
15	Saved ST registers	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD and RESET)

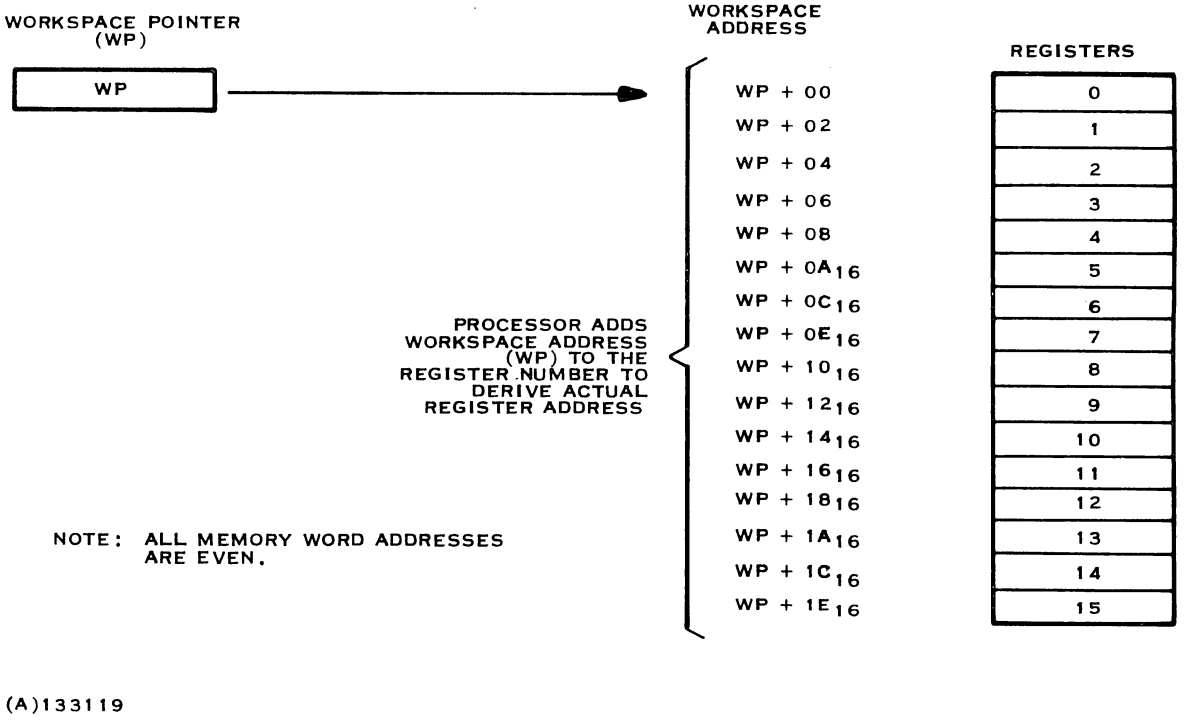


Figure 1-8. Workspace Pointer and Registers

The workspace concept is particularly valuable during operations that require a context switch (a change from one program to another or to a subroutine, as in the case of an interrupt). Such an operation using a conventional multiregister arrangement requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the contents of the program counter, status register, and workspace pointer, the microprocessor accomplishes a complete context switch with only three store cycles and two fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine, and the contents of the WP, PC, and ST registers from the previous routine have been saved in new workspace registers 13, 14, and 15, respectively. A corresponding savings in time occurs when the original context is restored. Instructions in the microprocessor that result in a context switch include:

- Branch and Load Workspace Pointer (BLWP)
- Return from Subroutine (RTWP)
- Extended Operation (XOP)

Device interrupts, power-up RESET—, and LOAD— also cause a context switch by forcing the microprocessor to trap to a service routine.

1.2.2.3 Interrupts. The TMS 9900 microprocessor can accommodate 16 interrupt levels with the highest priority level 0 and the lowest level 15. Level 0 is reserved for the power-up RESET— function, and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements.

The microprocessor continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the microprocessor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15 of the new workspace. The microprocessor then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for the level 0 interrupt that loads zero into the mask. This allows only interrupts of higher priority to interrupt a service routine. The microprocessor also inhibits interrupts until the first instruction of the service routine has been executed so that program linkage is preserved should a higher priority interrupt occur. All interrupt requests should remain active until recognized by the microprocessor in the device service routine. The individual service routines must reset the interrupt requests before the routine is complete. If a higher priority interrupt occurs, a second context switch is made to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters.

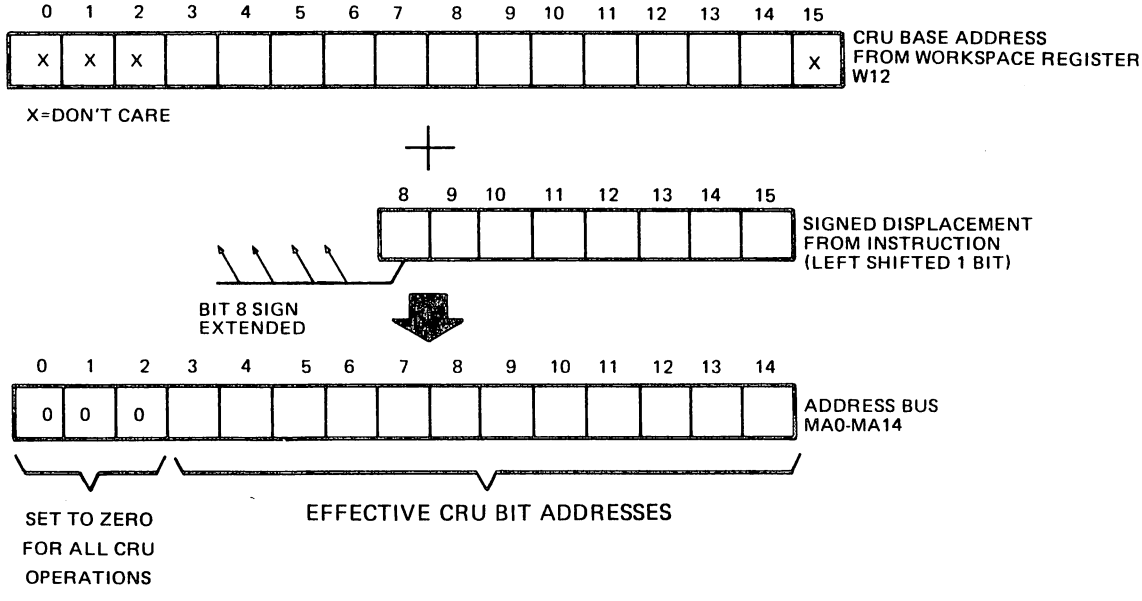
1.2.2.4 Input/Output. The TMS 9900 microprocessor uses a versatile direct command-driven I/O interface designated as the Communications Register Unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The microprocessor employs three dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus at the interface to the CRU system. The microprocessor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move data between memory and CRU data fields.

Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data transaction operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of several data or status bits.

The microprocessor performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the microprocessor develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the microprocessor generates a CRUCLK pulse that indicates to the CRU device that the operation is one of output and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a logic 1 for SBO and a logic 0 for SBZ). The test bit instruction is an input operation that transfers the addressed CRU bit from the CRUIN input line to bit 2 (equal bit, see figure 1-7) of the status register.

The microprocessor develops a CRU-bit address for the single-bit operations from the CRU base address contained in workspace register 12 (W12) and the signed displacement contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from bits 3 through 14 in W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 1-9 illustrates the development of a single-bit CRU address.



NOTE: MEMORY ADDRESS LINES MA3 THROUGH MA14 ARE RENAMED CRUBIT4 THROUGH CRUBIT15 AT THE OUTPUTS OF THE CRU ADDRESS DRIVERS

(A)133120

Figure 1-9. TMS 9900 Single-Bit CRU Address Development

The microprocessor performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from CRU to memory or from memory to CRU as illustrated in figure 1-10. Although the figure shows a full 16-bit transfer operation, any number of bits from 1 to 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts the word to serially transfer it to CRU output bits. If the LDCR involves 8 or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves 9 or more bits, those bits come from the right-justified field within the whole memory word. As the bits are transferred to the CRU interface, the CRU address is incremented for each successive bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a transfer of a byte or less, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves 9 to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero. When the input from the CRU device is complete, the first bit from the CRU is in the least significant bit position in the memory word or byte.

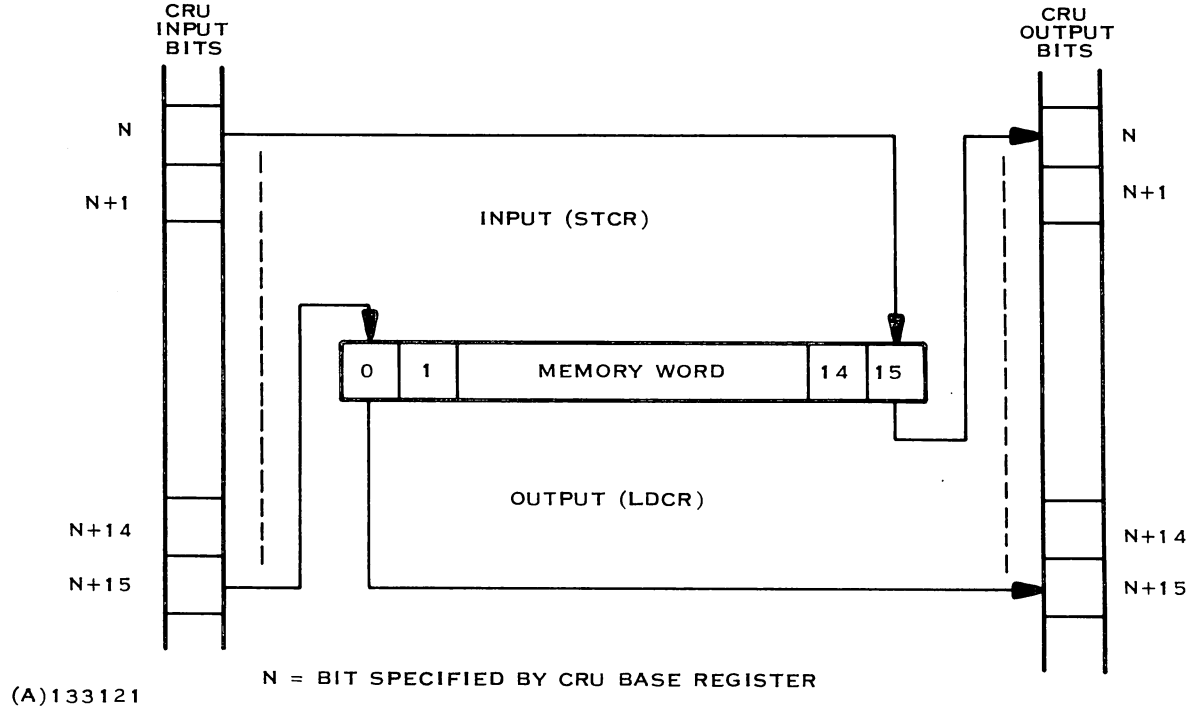


Figure 1-10. TMS 9900 LDCR/STCR Data Transfer

1.2.2.5 External Instructions. The TMS 9900 microprocessor has five external instructions that allow user-defined external functions to be initiated under program control. These instructions are Clock-On (CKON), Clock-Off (CKOF), Reset (RSET), Idle (IDLE), and Load and Restart Execution (LREX). Except for IDLE, these instructions relate to functions that have been implemented on the 990/5 circuit board but these functions do not restrict use of the instructions to initiate various user-defined functions in external devices. IDLE also causes the microprocessor to enter and remain in the idle state until an interrupt, RESET— or LOAD—, occurs. When any of these five instructions are executed by the microprocessor, a unique 3-bit code appears on the three most significant bits of the address bus (A0 through A2) along with the CRUCLK pulse. When the microprocessor is in an idle state, the 3-bit code and CRUCLK pulses occur repeatedly until the idle state is terminated. The external instructions codes are shown in table 1-3.

Table 1-3. TMS 9900 Microprocessor External Instruction Codes

EXTERNAL INSTRUCTION	A0	A1	A2
LREX	H	H	H
CKOF	H	H	L
CKON	H	L	H
RSET	L	H	H
IDLE	L	H	L

1.2.2.6 Load Function. The LOAD— signal permits cold-start ROM loaders and front panels to be implemented for the TMS 9900 microprocessor. When active, LOAD— causes the microprocessor to initiate a trap immediately following the instruction being executed.

Memory location $FFFC_{16}$ is used to obtain the trap vector (WP and PC). The old PC, WP, and ST are loaded into the new workspace, and the interrupt mask is set to 0000. Then, program execution resumes using the new PC and WP.

1.2.3 TMS 4116 DYNAMIC RANDOM-ACCESS MEMORY. The TMS 4116 is a 16,384 one-bit memory element. Each bit of the sixteen-bit word handled by the microprocessor is stored in its own element; a seventeenth element is available for parity. For a basic 990/5, this arrangement of elements allows for storage/retrieval of 32,768 bytes (32K bytes). The microcomputer may be expanded to an additional 32K bytes when 17 more TMS 4116 elements are included; one element for each bit of the 16-bit word and one element for the parity bit.

NOTE

Refresh operations are performed every 15.5 μsecs of one memory cycle duration.

1.2.4 TMS 4700 READ-ONLY MEMORY. The Read-Only Memory contains preprogrammed self-test and loader software. There are two elements; one for the lower order 8 bits, the other for the upper order 8 bits. Together, the two elements provide for storage of 1024 words of 16 bits each. One half of the storage capacity (512 sixteen-bit locations from address $F800_{16}$ to $FBFE_{16}$) is used for computer self-test; the other half of ROM is used for loader programs (addresses $FC00_{16}$ through $FFFE_{16}$).

The ROM can only be addressed by the TMS 9900 microprocessor; ROM cannot be addressed via the TILINE. Note that the lower half of this memory (addresses $F800_{16}$ through $FBFE_{16}$) is addressed at the same address as that reserved for the TILINE peripheral control space (TPCS). Access to either the TPCS or ROM self-test is determined by the state of ENROMAF800 (Enable ROM at address F800). This signal is the result of a set-bit-to-one (SBO) instruction addressed to CRU output bit at location hexadecimal 17F8. When enabled, TMS 9900 microprocessor memory cycles in this address range go to ROM and exercise self-test. The lower half of ROM is disabled by resetting the CRU output bit with an SBZ (set-bit-to-zero) instruction at location $17F8_{16}$. With the lower half of ROM disabled, TMS 9900 microprocessor memory cycles in this address range are directed to the TILINE as accesses to the TPCS. The lower half of ROM is also disabled whenever the 990/5 microcomputer is in the RUN mode. The upper half of ROM, containing loader programs (addressed at $FC00_{16}$ through $FFFE_{16}$), is always ready to accept addresses in this range. Additional information on the TMS 4700 ROM may be found in Section IV, entitled Programming Considerations.

1.2.5 COMMUNICATION REGISTER UNIT INTERFACE LOGIC. The direct command driven input/output interface for the 990/5 microcomputer is called the CRU. The CRU provides for up to 4096 directly addressable input bits and up to 4096 directly addressable output bits. Input and output operations can address each of the bits individually or in fields of from one to sixteen bits. The microprocessor instructions that drive the CRU can set, reset, or test any bit in the CRU array; or the microprocessor instructions can move data between memory and the CRU data fields.

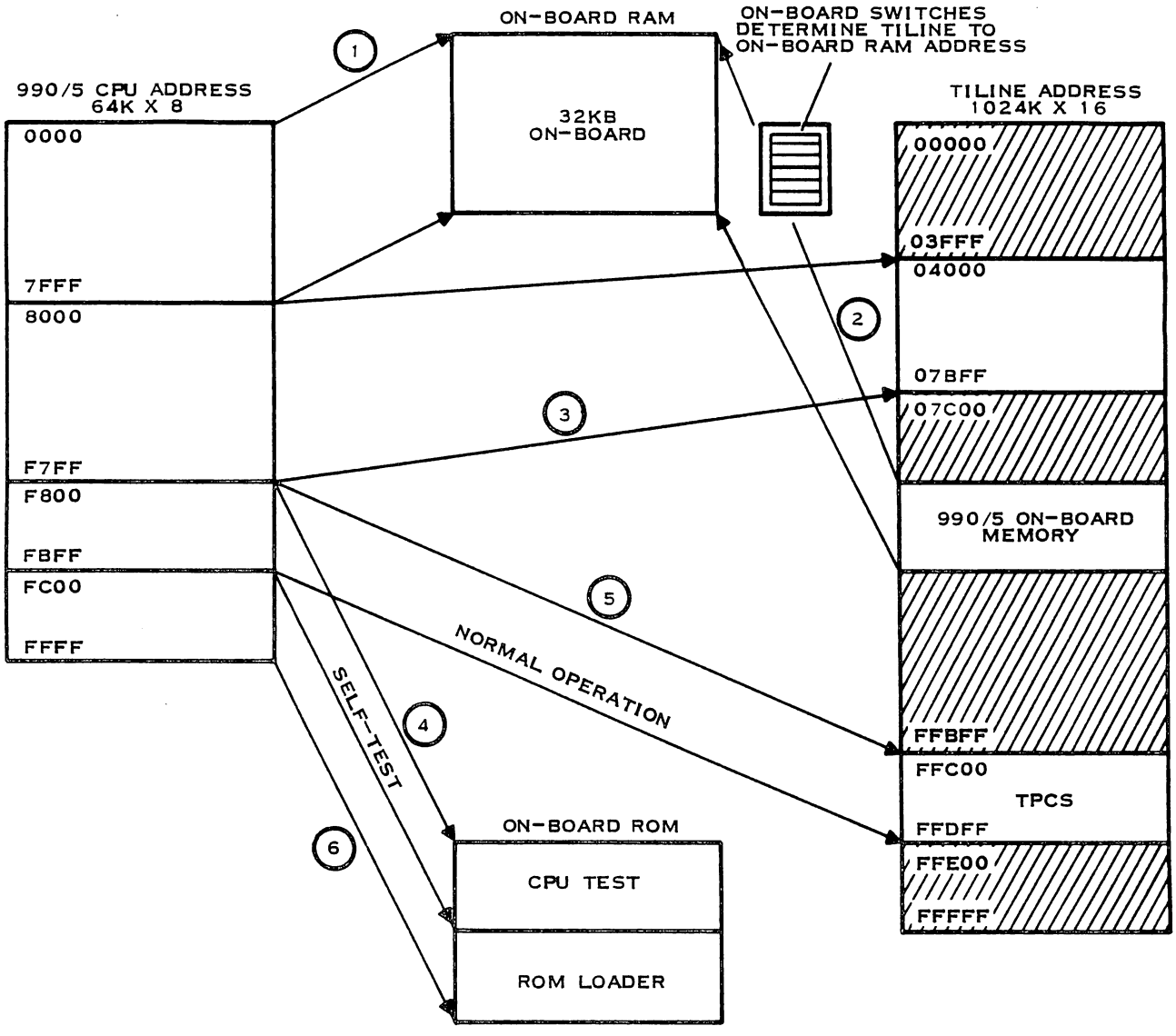
Logic for the CRU is implemented on the 990/5 circuit board and this logic exerts control over the interface data and control lines that consist of a clock, data in, data out, CRU address lines, and decoded module select lines. The 990/5 circuit board logic implements the CRU interface to the 990 chassis backpanel, the programmer panel, the three on-board communications ports, and the host processor interface logic. The CRU interface to the chassis backpanel is disabled when the 990/5 circuit board is installed in a chassis slot other than slot 1. See figures 2-9 and 2-16, respectively, for the basic 6-slot and 13-slot chassis configurations.

1.2.5.1 Module Select Logic. Twenty-four module select signals are decoded by CRU interface logic and are distributed, two per chassis slot, to twelve chassis slots when a 13-slot chassis is in use. Similarly, ten module select signals are distributed to five chassis slots when the 6-slot chassis is used. In either case, no module select signal distribution is made to chassis slot 1. Each full-sized chassis slot has the capability to implement a maximum of 32 input/output bits. The main chassis CRU addresses begin at 000 and extend to a maximum of hexadecimal 09F for a 6-slot chassis and to a maximum of hexadecimal 17F for the 13-slot chassis. If a computer system requires more CRU slots than are available in a main chassis, then from one to seven additional 6- or 13-slot CRU expansion chassis can be added. The chassis and backpanels used in the expansion chassis are identical to those used for the main chassis.

1.2.5.2 Backpanel CRU Interface Signals. Logic on the 990/5 circuit board implements a dedicated CRU interface for the programmer panel and also the standard CRU interface for the main chassis. The interface signals to the main chassis are routed via connectors P1 and P2 on the 990/5 circuit board. The master 990/5 circuit board is installed in slot 1 in the main chassis. The remaining slots are designated slots 2 through 6 for a 6-slot chassis and slots 2 through 13 for a 13-slot chassis. Both connectors in each chassis slot are furnished with the CRU select bits (CRUBIT 12-15) and other CRU interface signals that permit each connector to pass signals to address 16 bits of the CRU. Connector P1 in a chassis slot receives one module select signal corresponding to one 16-bit register whereas connector P2 receives two module select signals and thus may address up to 32 bits of the CRU. Connector P1 also receives the eight most significant bits of the CRU address thus permitting the chassis slot to be used for a CRU expansion driver or for modules that ignore the module select signals and decode their own CRU addresses, i.e., CRUBIT04 through CRUBIT15.

1.2.6 TILINE INTERFACE LOGIC. The 990/5 CRU provides a TILINE bus interface. TILINE is a high-speed, parallel bus interconnecting 990 CPUs, memories, and autonomous high-speed devices such as disk controllers. TILINE permits implementation of tightly coupled multiprocessor systems with advanced features such as shared memory.

The TILINE bus address is 20 bits in length and describes a 1024K × 16 bit address space. The 990/5 CPU generates a 16-bit address identifying locations in a 64K × 8 bit address space. The relationship of these addresses for a 32K byte system and a 64K byte system are shown in figures 1-11 and 1-12, respectively.



1. CPU ADDRESSES 0000-7FFF ALWAYS ADDRESS ON-BOARD RAM
2. TILINE CAN ADDRESS ON-BOARD RAM. TILINE ADDRESS IS SET BY ON-BOARD SWITCHES ANYWHERE IN TILINE ADDRESS SPACE ON 4K WORD BOUNDARIES.
3. CPU ADDRESSES 8000 – F7FF REACH TILINE ADDRESSES 04000 – 07FFF
4. CPU ADDRESSES F800 – FBFF DURING SELF-TEST ADDRESS ON-BOARD ROM
5. CPU ADDRESSES F800 – FBFF AFTER SELF-TEST ADDRESS TILINE PERIPHERAL CONTROL SPACE
6. CPU ADDRESSES FC00 – FFFF ADDRESS ON-BOARD ROM LOADER

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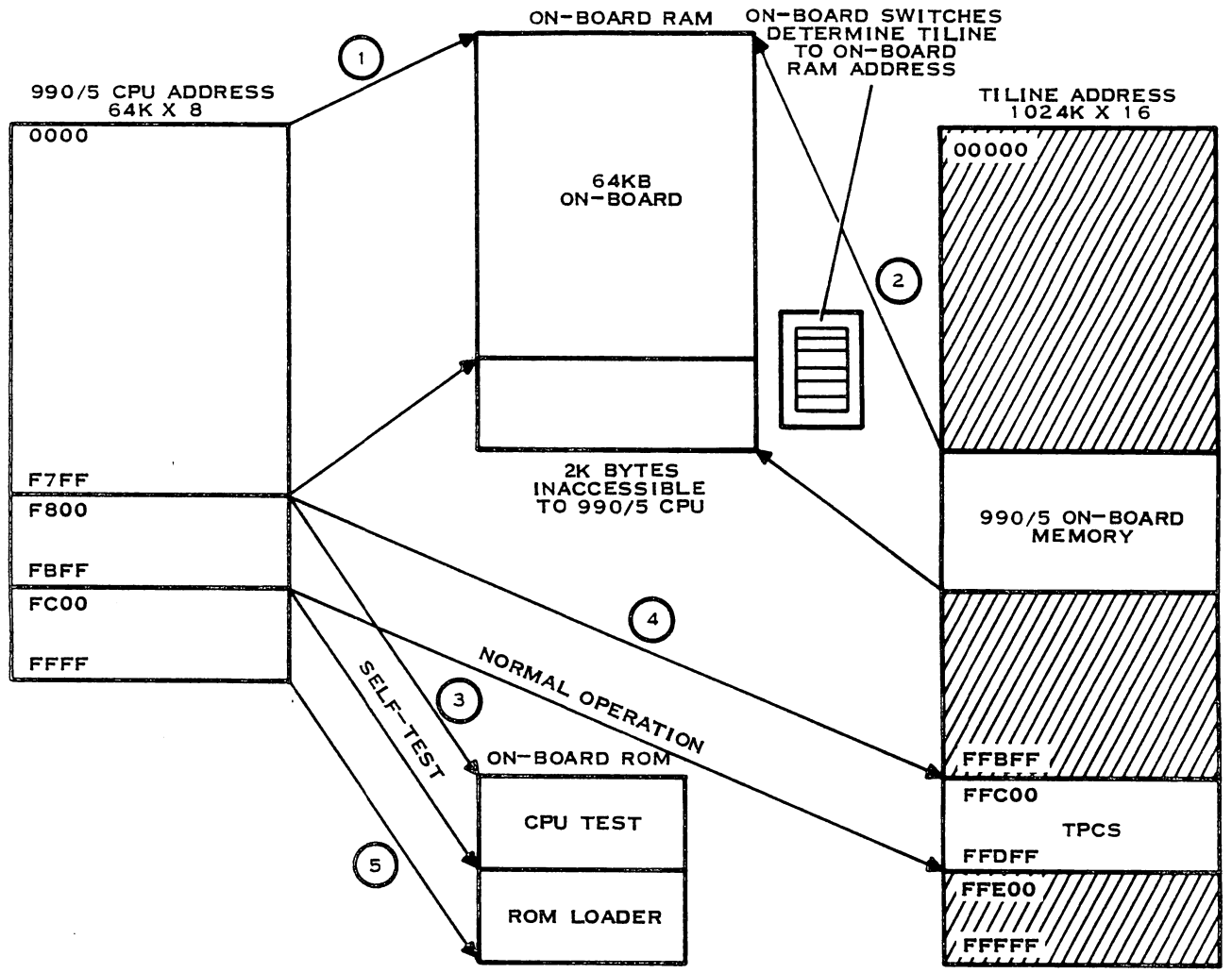
Figure 1-11. 32KB 990/5 and TILINE Addressing



1. CPU ADDRESSES 0000 - F7FF ALWAYS ADDRESS ON-BOARD RAM
2. TILINE CAN ADDRESS ON-BOARD RAM. TILINE ADDRESS IS SET BY ON-BOARD SWITCHES ANYWHERE IN TILINE ADDRESS SPACE ON 4K WORD BOUNDARIES.
3. CPU ADDRESSES F800 - FBFF DURING SELF-TEST ADDRESS ON-BOARD ROM
4. CPU ADDRESSES F800 - FBFF AFTER SELF-TEST ADDRESS TILINE PERIPHERAL CONTROL SPACE
5. CPU ADDRESSES FC00 - FFFF ADDRESS ON-BOARD ROM LOADER

(A) 139350B

Figure 1-12. 64KB 990/5 and TILINE Addressing

1.2.6.1 Master-Slave Concept. There are two classes of devices that connect to the TILINE: TILINE master devices that control data transfers and TILINE slave devices that generate or accept data in response to some master device. (This discussion of TILINE master/slave relationships should not be confused with the CPU host and CPU slave relationship.) Data transfers in either direction always occur between one master and one slave. A processor is an example of a master device; a memory module is an example of a slave device. All slave devices recognize a specific address and are activated only when addressed. For example, a memory module is activated when some master device performs a read operation from an address within the bounds of its address. The configuration of the system must be such that only one slave device recognizes a particular address. For memory modules, pencil switches on the modules are set to provide the desired starting address and size of the module.

Peripheral device controllers are both master and slave devices. Special registers addressed at specific memory addresses near the high end of the memory address space (TILINE peripheral control space) constitute the slave part of the peripheral controller. The registers are loaded by the processor using memory-to-memory move instructions. The registers specify the parameters of a peripheral data transfer. In the case of a disk, they specify disk address, the number of words of data to be transferred, the memory address to which the data is to be transferred, and whether the data is to be read or written. One register in each peripheral controller is a status register for that controller. The bits in the register indicate information such as "operation complete", "read error", "rewind complete", and "illegal command". Other bits in the peripheral controller status register are set by the central processor to command the peripheral to start, stop, clear its interrupt, or reset. All of these registers are addressed by the central processor as consecutive words of memory at some specific address. Pencil switches are used to set the address of the registers for each peripheral controller. When a peripheral controller operation is started by the central processor, it transfers data between memory and the peripheral device by cycle-stealing with the central processor and any other master devices that may be active. When a peripheral controller needs to transfer a word of data over the TILINE, the master device part of the peripheral controller must gain access to the TILINE and then may address a slave (such as a memory module) and read from, or write to it.

1.2.6.2 990/5 TILINE Operation. The 990/5 CPU is both a TILINE slave and TILINE master device. As a TILINE slave device, the 990/5 CPU is seen as a contiguous 32K bytes or 64K bytes (as equipped) block of memory with its starting address selectable at 4K boundaries through the use of eight pencil switches. Switches 1 through 8 are set to the most significant eight bits of the desired starting TILINE address. Switch 1 is the most significant bit; switch 8 is the least significant of the eight bits mentioned above.

As a TILINE master device, the 990/5 microprocessor can access TILINE Peripheral Control Space (TPCS) by decoding accesses in the address range of hexadecimal F800 through FBFE and forcing the five most significant TILINE address bits to logic 1 when the decode is true. In addition, when the 990/5 microprocessor has only 32K bytes of memory, accesses above address hexadecimal 8000 but below address hexadecimal F800 are made to TILINE memory with the address unmapped. This permits more than one processor to share a common 30K bytes of TILINE memory.

1.2.7 COMMUNICATIONS PORTS. Three communications ports are implemented on the 990/5 circuit board. Each port is a CRU device with a dedicated, hardwired CRU address. Ports 1 and 2 are each implemented with a TMS 9902 Asynchronous Communication Controller (ACC) and are addressed at CRU addresses hexadecimal 1700 and 1740, respectively. Port 3 is implemented with a TMS 9903 Synchronous Communication Controller (SCC) with additional external logic and is addressed at CRU address hexadecimal 1780. None of the three ports has a hardware reset. Therefore, a communications enable bit at CRU address hexadecimal 17CE enables all three communications ports. An SBO instruction to the bit should be executed after the software reset of the three ports. The interrupt from each port is enabled or inhibited by directing an SBO or SBZ to the appropriate CRU output bit. The CRU output bits are addressed as follows: port 1 interrupt at

hexadecimal 17C8, port 2 interrupt at hexadecimal 17CA, port 3 interrupt at hexadecimal 17CC. The two ACC ports are used for local asynchronous communications with peripheral devices such as an ASR or printer. The third port may be used in either the asynchronous or the synchronous mode to support either local or modem communications. When used in the synchronous mode, the baud rate for the third port is selectable. All three ports meet standards of EIA RS232-C as established by the Electronic Industries Association.

1.2.7.1 Asynchronous Communications Ports. The TMS 9902 ACC devices used to implement communications ports 1 and 2 provide an interface between the TMS 9900 microprocessor and serial asynchronous communications channels. They perform the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor. Key features of the TMS 9902 ACC are as follows:

- 5- to 8-bit character length
- 1, 1.5, or 2 stop bits
- Even, odd, or no parity
- Fully programmable data rate generation
- Interval timer with resolution from 64 to 16,320 microseconds
- Fully TTL compatible, including single power supply

The TMS 9902 interface to the asynchronous channel is through level shifters which translate the TTL inputs and outputs to standard RS-232. The TMS 9902 interface to the TMS 9900 microprocessor through the CRU provides up to 32 directly addressable output bits and up to 32 directly addressable input bits. The CRU interface consists of 12 address lines and three dedicated input/output lines (CRUIN, CRUOUT, and CRUCLK). When the TMS 9902 is addressed by the TMS 9900 microprocessor, the seven most significant bit address lines (BA03 through BA09) generate a low port select signal that is applied to the chip enable pin (CE—) of the TMS 9902. With CE— active (low), the five least significant bit address lines (BA10 through BA14 that are connected to address pins S0 through S4 of the TMS 9902, respectively) address the CRU input or output bit being accessed. When data is being transferred from the TMS 9900 microprocessor to the TMS 9902, a CRUCLK pulse indicates that the operation is one of output, and valid data on the CRUOUT lines is transferred to the addressed CRU output bit of the TMS 9902. When data is to be transferred from the TMS 9902 to the microprocessor, data from the addressed CRU input bit is placed on the CRUIN line for transfer. More detailed information on the TMS 9902 may be found in Section IV, Programming Considerations.

1.2.7.2 Synchronous Communications Port. The TMS 9903 used to implement communications port 3 provides the system designer with a wide range of capabilities in synchronous and asynchronous communications control. Communications port 3 can be used to support local synchronous or asynchronous communications or can be used with a modem. The TMS 9903 operates in a multi-mode configuration that allows a broad range in the degree of active participation required in the control of high-speed serial communications. Most synchronous data-link control protocols can be supported through software control of sync and fill characters, timing, CRC generation and detection, etc. Universal applicability is further assured through the dynamic character length selection from 5- to 9-bit data words plus parity.

Definition and operation of all communications control is under software control, which makes upgrading to another protocol simply a matter of changing software with no hardware changes required. Key features of the TMS 9903 SCC are as follows:

- DC to 250 KBPS data rate, half- or full-duplex
- Dynamic character length selection
- Line protocols, including BI-SYNC, SDLC, HDLC, and many others
- Programmable polynomial CRC generation and detection
- Interface to unclocked or NRZI data with 32X clocks
- Two programmable sync registers
- On-chip interval timer (64 μs to 16.32 ms)
- Automatic zero insert and delete for SDLC and HDLC
- Single +5 V supply, 20-pin DIP, all inputs and outputs TTL compatible
- N-channel Silicon-Gate technology
- Replaces 100 SSI and MSI devices

The TMS 9903 interface to the synchronous or asynchronous channel is through level shifters which translate the TTL inputs and outputs to the appropriate level. The TMS 9903 interface to the microprocessor through the CRU provides 32 directly addressable output bits and 32 directly addressable input bits. The CRU interface consists of 12 address lines and three dedicated input/output lines (CRUIN, CRUOUT, and CRUCLK).

1.2.8 INTERRUPTS. Logic for 15 vectored interrupt levels (13 external) is contained on the 990/5 microcomputer circuit board. Each interrupt input is terminated with a 470-ohm pull-up resistor and a flip-flop to synchronize interrupts with the microprocessor clock. The highest priority interrupt level is reserved as a power-up trap. The interrupt levels are assigned priority rankings from level 0 (highest priority) to level 15 (lowest priority). All priority interrupt levels with the exception of the power-up interrupt (level 0) are maskable under software control. Interupt inputs are synchronized with the 990/5 clock, encoded, and presented to the TMS 9900 microprocessor along with an interrupt request. The interrupt levels are vectored for rapid reaction to recognized interrupts. That is, corresponding to each interrupt level is a two-word vector located in low-order memory (addresses 00 through 3E, hexadecimal). When the TMS 9900 microprocessor recognizes an interrupt, it loads the vector for that level into the Workspace Pointer (WP, first vector word) and the Program Counter (PC, second vector word) to defined the new workspace and program starting point for the interrupt servicing routine. A number of interrupt conditions are generated on the 990/5 circuit board and are wired directly to interrupt inputs. The interrupt conditions are discussed in the paragraphs that follow.

1.2.8.1 Power Failure Interrupt. When ac power begins to fail in a standard TI chassis, a sensor in the power supply generates a TLPFWP— pulse that is applied to the 990/5 circuit board as a level 1 interrupt. The microcomputer has 7.0 milliseconds of program time after receipt of the power failure warning before a power supply reset halts operation.

1.2.8.2 Error Interrupt. Logic to generate an error interrupt at priority level 2 is contained on the 990/5 circuit board. The error interrupt is a merging of memory parity error detect logic and the TILINE timeout condition. Each of these conditions is latched in an error register. The 990/5 microcomputer may access parity error status and timeout status by executing a CRU read instruction to CRU input bits 12 and 15, respectively, at CRU base address hexadecimal 1FC0. A CRU write instruction similarly addressed clears parity error and timeout conditions. Additionally, a write instruction addressed to CRU output bit 12 at CRU base address hexadecimal 1FE0 (front panel) also clears the parity error condition. Both conditions are cleared by execution of the reset instruction.

1.2.8.3 Real-Time-Clock Interrupt. The standard TI chassis power supply provides a line frequency synchronized clock input to the 990/5 circuit board that is used by logic on the board to implement a real-time-clock interrupt function. This function may be connected to interrupt level 5 (standard) or interrupt level 15, or it may be disconnected. External instructions CKON and CKOF are used to enable or disable the real-time-clock interrupt function.

1.2.8.4 Communications Ports Interrupts. An interrupt from each of the three communications ports may be connected to an external interrupt input by a switch. When activated, connections are as follows: communications port 1 to interrupt level 8, communications port 2 to interrupt level 14, and communications port 3 to interrupt level 6. These interrupts are masked until a CRU output instruction is issued to set output bits 36, 37, and 38, respectively, of CRU base address hexadecimal 1780.

1.2.8.5 Host Processor Interrupt. When a 990/5 microcomputer is installed in a chassis slot other than slot 1, it performs as a slave processor. A host processor (installed in chassis slot 1) may generate an interrupt to the slave processor through the host processor CRU. This interrupt is hardwired to interrupt level 3. The slave processor may mask the interrupt by setting bit 14 of CRU base address hexadecimal 17E0 (see paragraph 1.4).

1.3 990/5 CHARACTERISTICS AND SPECIFICATIONS

The power requirements for the 990/5 circuit board are listed in table 1-4. The specifications for the 6- and 13-slot chassis are listed in table 2-1.

1.4 MULTIPROCESSOR FEATURES

The 990/5 microcomputer features hardware which facilitate multiprocessor applications including multiple CPUs in a single chassis. It should be noted to prospective users that successful multiprocessor applications require careful planning at system and software levels. The most basic multiprocessor feature is the TILINE multi-user bus which permits shared memory modules and access from one CPU to another CPU's memory.

The 990/5 CPU identifies itself as host when plugged into slot 1 of the chassis. As the host, the 990/5 controls external CRU chassis wiring and has, in addition to 1K of ROM self-test, 1K of ROM for bootstrap loading.

A 990/5 CPU in any chassis slot other than slot 1 identifies itself as slave. Slave 990/5 drivers for external CRU chassis wiring are disabled, and the bootstrap loader is disabled. The slave 990/5 has 1K of self-test, controls on-board CRU, and may address TILINE devices in TILINE Peripheral Control Space (TPCS).

An interprocessor communications scheme provides CRU-driven maskable interrupts between processors. Any slave addresses the host at a single CRU address. The host addresses each slave independently. Differentation among multiple slaves is implemented by on-board pencil switches to provide a 4-bit identification code. This identification is independent of the station identification which is used by host 990/5 CPUs only.

Table 1-4. 990/5 Board Current Requirements in Amperes

Voltage*	With 32K Bytes	With 64K Bytes
Operating:		
+5V Main	2.25	2.50
+12V Main	.20	.20
-12V Main	.04	.04
+5V Memory	.30	.30
+12V Memory	.33	.65
-5V Memory	.02	.03
Standby:		
+5V Memory	.30	.30
+12V Memory	.025	.050
-5V Memory	.02	.03

*Maximum tolerance for all voltages except -5V Memory is ±3 percent. Tolerance for -5V Memory is ± 6 percent.

990/5 Microcomputer Board Dimensions:
274.32 mm (10.8 inches) wide by 361.95 mm (14.25 inches) long by 1.5575 mm (.062 inch) thick. Component height on board is 8.89 mm (.350 inch), maximum.

In a single chassis, interprocessor communications are limited to slave-host and host-slave; i.e., no slave-slave direct communications can occur. The slave processor (not to be confused with a TILINE slave device) and the host processor may interrupt each other, mask interrupts from each other, acknowledge interrupts from each other, and enable interrupts from each other on interrupt acknowledge. The host processor uses 64 CRU bits, beginning at CRU address hexadecimal 1F40 (Register R12 = hexadecimal 1E80), to communicate with up to sixteen slave processors. The 990/5 microprocessor circuit board contains four switches that permit selection of one of sixteen groups of four bits each to which the slave processor responds. The 990/5 microprocessor uses four bits at CRU address hexadecimal 1BF0 (Register R12 = hexadecimal 17E0) to communicate with a host processor. Table 1-5 lists the CRU bit assignments and a description of each.

Table 1-5. Interprocessor Communications CRU Bit Assignments

Output Bit	Description
0	Interrupt remote processor
1	Interrupt local processor on receipt of remote processor's interrupt acknowledge
2	Acknowledge interrupt from remote processor
3	Interrupt from remote processor mask (1 = Enable; 0 = Disable)
Input Bit	
0	Interrupt to remote processor active
1	Slave fault (in 990/5) or logic 0 (in other CPUs)
2	Interrupt from remote processor active
3	Slave idle (in 990/5) or logic 0 (in other CPUs)

SECTION II

INSTALLATION

2.1 GENERAL

This section provides information and procedures for unpacking the microcomputer from its shipping container, installing it in either a tabletop or a rackmounted chassis, and checking the operation of the newly installed computer system. This section also includes a procedure for modifying the interrupt structure of the computer and verifying that the proper jumper wire options have been installed. The procedures assume that the user has a fundamental knowledge of basic handtools and cabling techniques, but they do not require a detailed understanding of computer hardware or software. This section does not cover installation of any of the peripheral devices that may accompany the computer shipment. Installation instructions for those devices are included in the Installation and Operation manual that is shipped with each peripheral device. To aid in planning to meet the installation requirements for the computer, table 2-1 summarizes the specifications and requirements of the available chassis for the computer.

Table 2-1. Computer Chassis Specifications

Characteristic	6-Slot Chassis	13-Slot Chassis
Height	178 mm (7 inches)	311 mm (12-¼ inches)
Width	419 mm (16-½ inches)	419 mm (16-½ inches)
Depth	584 mm (23 inches)	584 mm (23 inches)
Ambient Temperature[1]		
Operating[2]	0° to 50°C (32° to 122°F)	0° to 40°C (32° to 104°F)
Storage	-40° to +70°C (-40° to +158°F)	-40° to +70°C (40° to 158°F)
Humidity[3]	0% to 95%	0% to 95%
Altitude	0 to 3.05 km (0 to 10,000 feet)	0 to 3.05 km (0 to 10,000 feet)
Heat Load		
Full Card Slot	30 watts	30 watts
Power Supply	100 watts	170 watts
Exhaust Temperature	65°C (maximum) (149°F (maximum))	65°C (maximum) (149°F (maximum))

Notes:

1. Lower the upper operating limit by 2°C (3.6°F) for every 762 metres (2500 feet) increase in altitude.
2. If the 990/5 board is to be installed in other than a standard TI chassis, the following environmental conditions are required:

Ambient air temperature at board[1]	5°C to 65°C (41°F to 149°F)
Air flow at exhaust	100 ft/min

3. No condensation should be allowed.

Table 2-1. Computer Chassis Specifications (Continued)

Characteristic	6-Slot Chassis	13-Slot Chassis
External Power Requirements		
Standard	115 Vac +15%, -10% 3-wire service (hot, neutral, gnd)	115 Vac +15%, -10% 3-wire service (hot, neutral, gnd)
Optional	100, 200, or 230 Vac +15%, -10% or 220 + 10%, -15% 3-wire service (hot, neutral, gnd)	100, 200, or 230 Vac +15%, -10% or 220 +10%, -15% 3-wire service (hot, neutral, gnd)

There is considerable flexibility in the 990/5 Interrupt, CRU address, and TILINE address assignments. This flexibility is matched in the TI standard software packages by a capability in these software packages to define the I/O assignments. The software and hardware assignments must agree. A 990/5 user, who also intends to use the TI standard software packages, should read the programming considerations in paragraph 4.1 before selecting particular I/O assignments.

2.2 SITE PREPARATION

Site preparation, which includes the power, space, environmental, special supply, and communications requirements for the Model 990/5 Minicomputer System, is covered in detail in the following paragraphs.

2.2.1 HARDWARE ENVIRONMENT CONSIDERATIONS. The customer is responsible for providing an environment that is free of excessive dust and foreign particles. This environment may be a typical office environment free from excessive airborne matter that may cause damage to the equipment. The requirements listed below are necessary for proper operation of the 990/5:

	990 Chassis	Equip. Desk and Single-Bay Pedestal	Rackmount Cabinet
Input Power Frequency:[1]	60 Hz	60 Hz	60 Hz
Input Current:	7.5 amps	20.0 amps	30.0 amps
Watts:	862.5	N/A	N/A
Btu/hr:[2]	2950	N/A	N/A
Power Cord Length:	1.8 m (6 ft.)	3.6 m (12 ft.)	3.6 m (12 ft.)

[1] All units are powered by 115 Vac +15%, -10%.
[2] Calculations are based on 1 watt = 3.413 Btu/hr.

Ac outlets must be located so that the power cords are not stretched or in danger of damage once the hardware is in place. The cord may not lay in traffic lanes and must be capable of carrying a minimum of 20 amps.

The ac input lines for all TI equipment will be dedicated; no non-TI device may share the same ac power lines.

No electrically noisy equipment may be plugged into the power to impair operation of the equipment. Examples of noisy equipment are: air conditioners, compressors, copy machines, electric fans, neon lights, and ac motors.

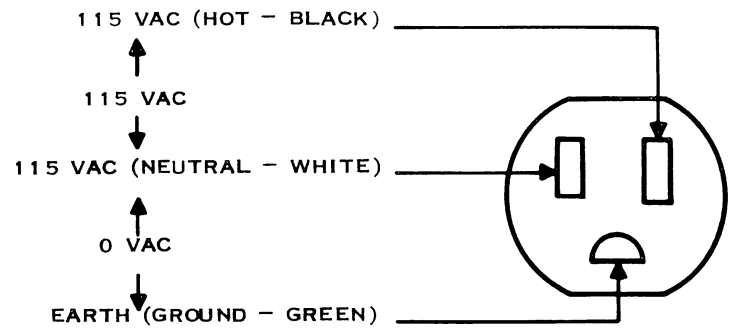
The 115 Vac wiring shall consist of a hot, a neutral, and an earth return. The earth return (ground) will be terminated properly and in such a manner that it makes a good connection to the earth (ground) return at the power source.

The user will ensure that the ac receptacle is wired as shown in figure 2-1.

NOTE

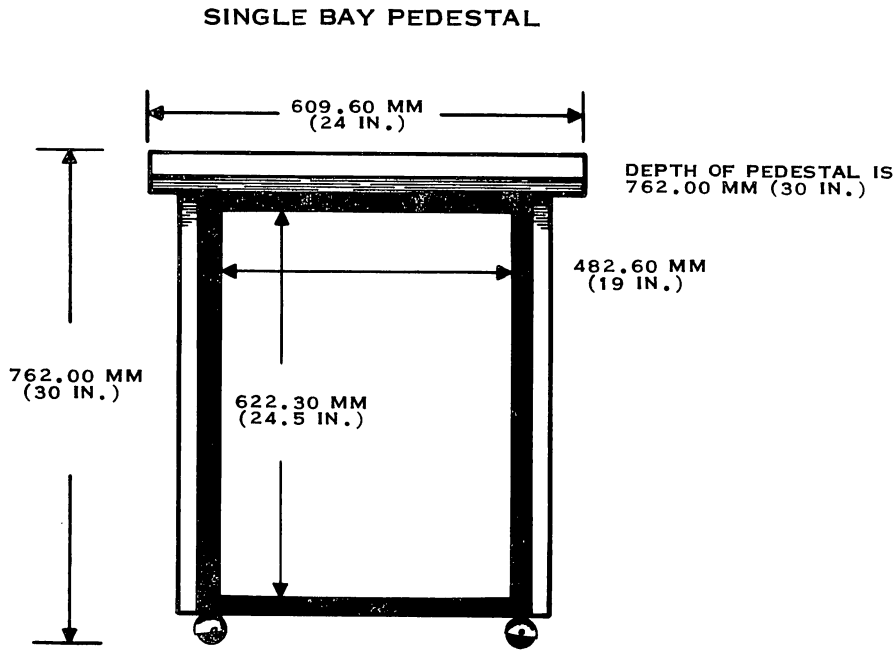
Rackmount cabinets require receptacles for 30 amp service.

2.2.2 SPACE REQUIREMENTS. All equipment will be positioned such that a three-foot clearance exists on all sides of the desk, cabinet, and disk drive. Figures 2-2 and 2-3 give dimensions for space requirements.



(A) 140387

Figure 2-1. Site AC Receptacle Wiring



(A) 140388

Figure 2-2. Single-Bay Pedestal Dimensions

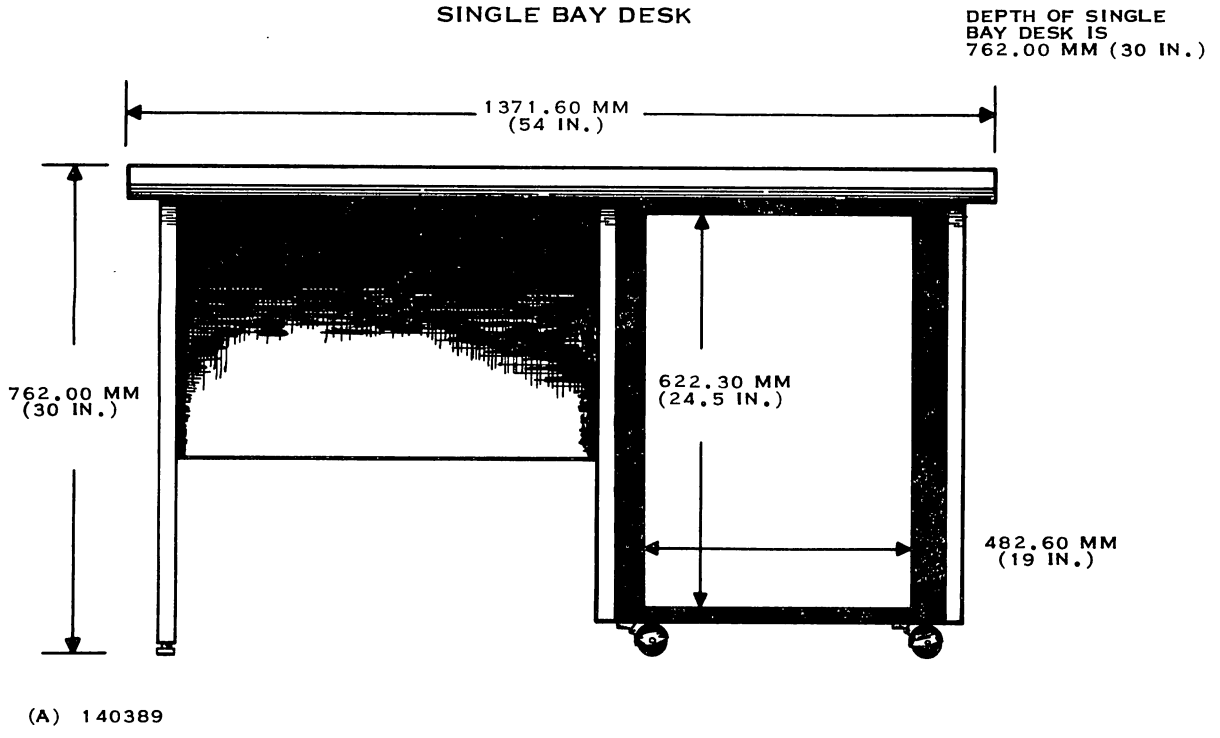


Figure 2-3. Single-Bay Desk Dimensions

2.2.3 INTERCONNECT CABLING REQUIREMENTS. A typical system cabling configuration is given in figure 2-4. The preinstallation site inspection should be completed at least two weeks prior to installation. If the system is to use remote CRTs and line printers, the cables and connector kits should be installed and checked-out at least one week prior to system installation.

Route the peripheral cables in such a manner that there are no breaks or splices in the cables. Both ends of all cables will be clearly marked with a semi-permanent marking, such as good quality masking tape or gum labels. An example of this is shown in figure 2-5. If the user mounts a peripheral in a desk or other device, the desk must not bind any cables, and the control knobs should be easily accessible.

2.2.4 UNPACKING/PACKING (6- AND 13-SLOT CHASSIS). The computer is shipped in a corrugated cardboard container together with the circuit boards and interconnecting cables required to install the system. Upon receipt of the container, inspect to ensure that no signs of physical damage are present. After completion of the preliminary inspection, perform the following steps to remove the computer from its container and ready it for operation. Figure 2-6 illustrates the contents of the shipping container.

NOTE

Save and label shipping carton, shipping brackets, and all packing materials for use should reshipment of the unit become necessary.

1. Position container so that the address label is right-side up.

2. Open top of container and remove cushioning material from corners.

NOTE

If the computer has the tabletop enclosure (6-slot chassis only), no foam block is required to secure circuit boards in chassis.

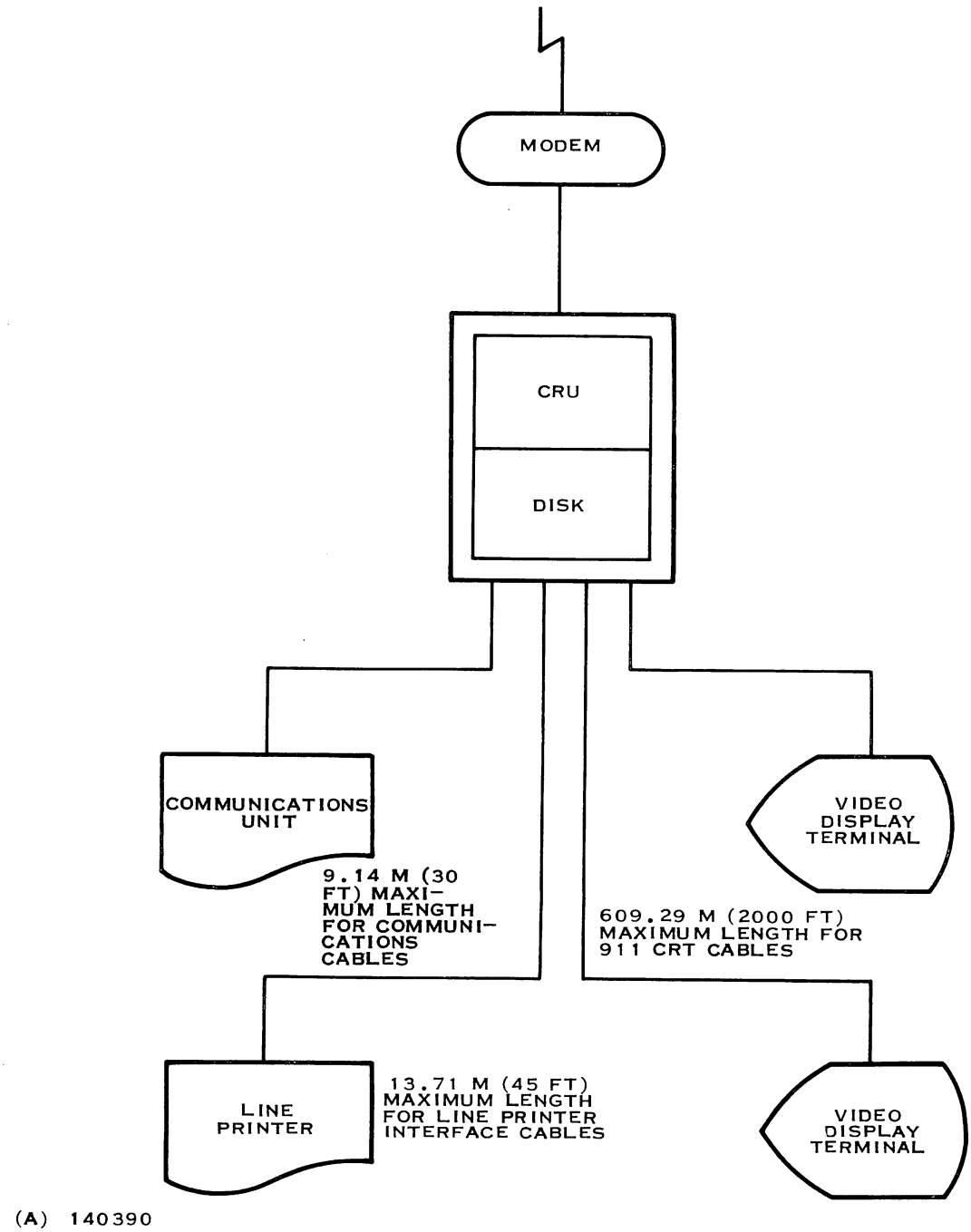


Figure 2-4. Typical System Cabling

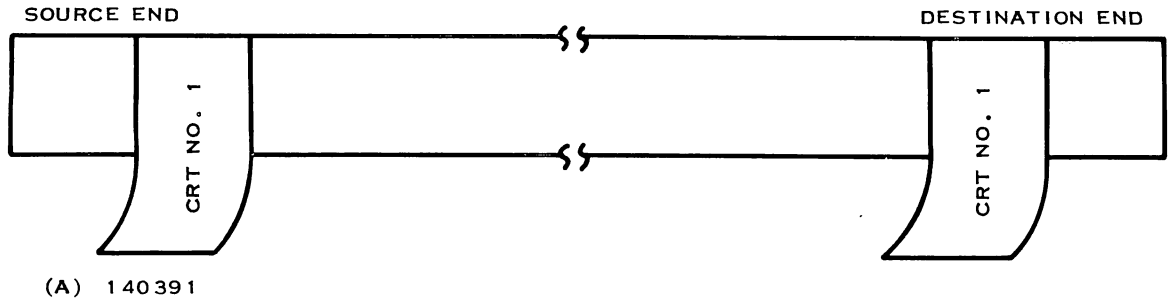


Figure 2-5. Typical Cable Marking for 911 VDU

3. Remove cardboard inner sleeve and foam block (rackmount configurations) from shipping container.

WARNING

Use proper lifting techniques to avoid backstrain when lifting computer chassis.

4. Remove computer and attached shipping pallet from container. When lifting assembly, lift from under the assembly to avoid undue strain on the chassis assembly.

CAUTION

To prevent the mounting screws on the underside of the shipping pallet from scratching table surface, place a shielding material (the packing sleeve removed in step 3 makes an excellent shield) on the table before setting the assembly on the table.

5. Place the removed assembly on a convenient, protected work surface.

NOTE

For rackmount configurations, the slides are packed in the bottom of the shipping container.

6. Remove rackmount slides (if present) and interface cables from bottom of shipping container.

CAUTION

In following steps, do not allow the unit to overhang the work surface so far that it will fall off the surface.

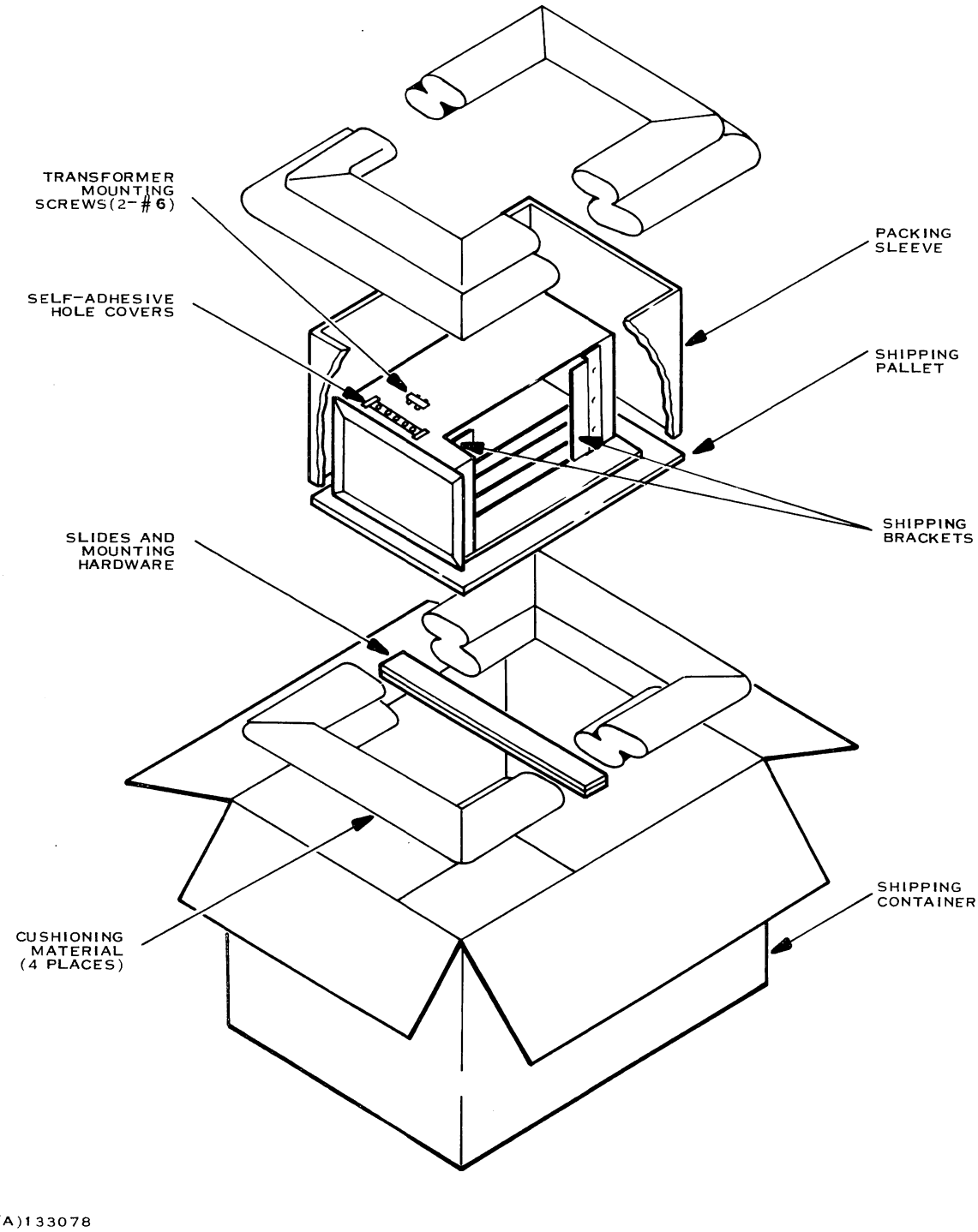


Figure 2-6. Computer Shipping Packaging

7. Position computer and shipping pallet assembly so that front edge of assembly overhangs edge of work surface to reveal two (2) #10 mounting screws that secure computer to shipping pallet. See figure 2-7 for location of all mounting screws.

8. Use a straight blade screwdriver to remove two mounting screws and their associated washers and lock washers. Save screws and washers for reshipment.

9. Reposition computer and shipping pallet assembly so that rear edge of assembly overhangs the edge of work surface to reveal three (3) #10 mounting screws that secure computer to shipping pallet.

10. Remove the three screws, washers, and lock washers and save with shipping carton.

NOTE

If the computer was ordered for overseas operation, two (2) additional mounting screws are visible on the underside of shipping pallet. If these screws are not included on the unit being installed, skip step 11.

11. Remove two (2) #6 transformer mounting screws and their associated washers and lock washers, and save with shipping carton.

12. Lift computer chassis from shipping pallet and place it on work surface such that the rear of unit overhangs work surface to reveal holes for previously removed mounting screws.

NOTE

If unit being installed did not have the two #6 mounting screws (see step 11), skip step 13 and proceed to step 14.

13. Remove two (2) #6 screws taped to top of computer chassis and insert them in holes vacated by two #6 mounting screws removed in step 11. Tighten two new screws to secure transformer to chassis.

14. Remove strip of self-adhesive hole covers that are taped to top of computer chassis. Use three of the hole covers to cover three mounting screw holes along the rear of chassis.

15. Reposition computer chassis such that front edge overhangs work surface to reveal the mounting holes for front mounting screws.

16. Use remaining two (2) self-adhesive hole covers to cover front mounting screw holes.

17. Set computer chassis in a safe position on work surface to continue with remaining portions of installation procedure as described in either the paragraph entitled INSTALLATION (TABLETOP CHASSIS) or the paragraph entitled INSTALLATION (RACKMOUNT CHASSIS).

18. Pack all shipping material into original shipping container and store container for use in reshipment of unit.

19. Inspect computer chassis (and included components) for signs of damage that may have occurred during shipment. If damage has occurred, notify the carrier immediately.

To repack the unit, reverse above procedure using original packing material.

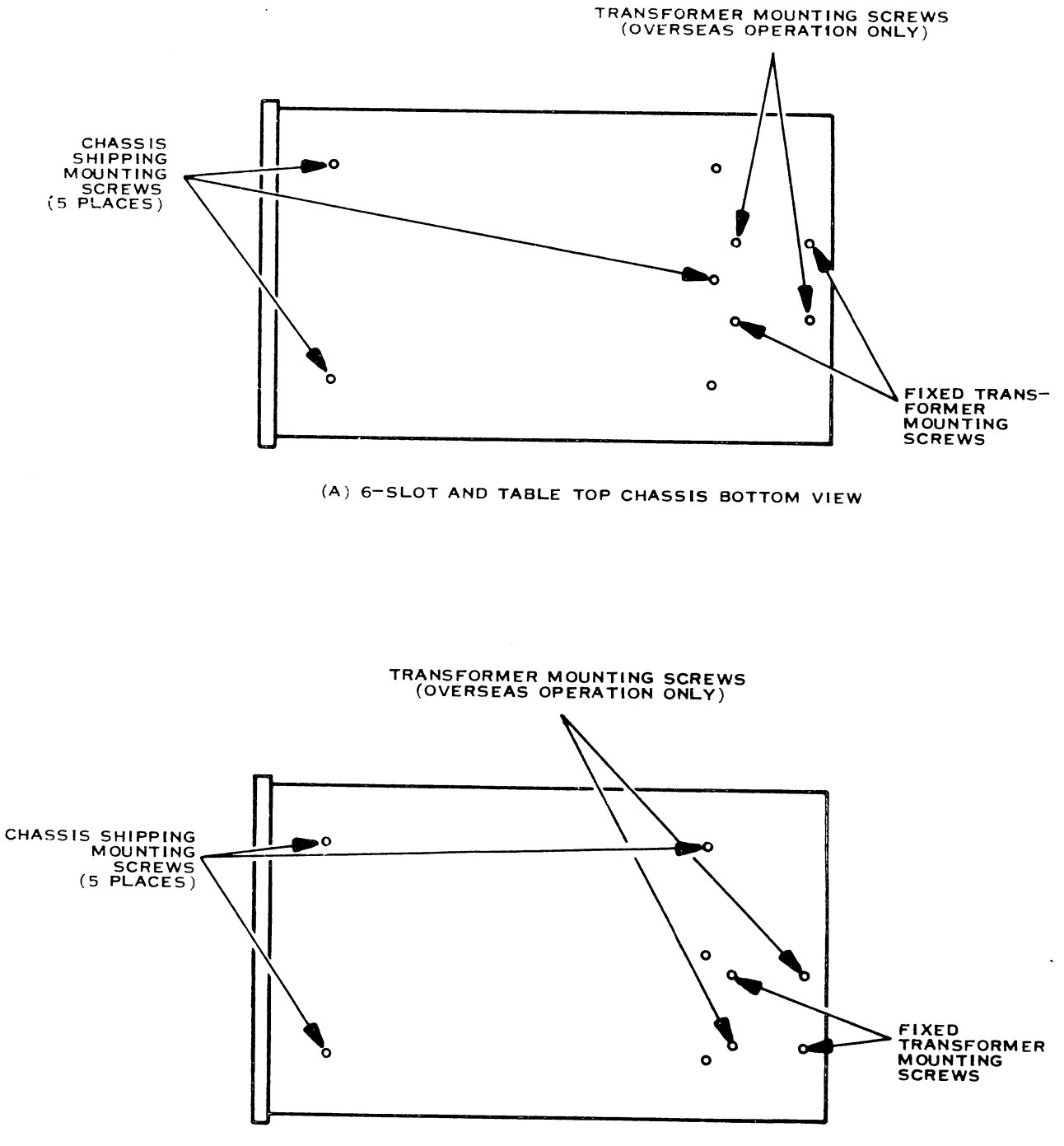


Figure 2-7. Location of Chassis Shipping Pallet Mounting Screws

2.3 INSTALLATION (TABLETOP CHASSIS)

The tabletop chassis is a 6-slot chassis configuration contained in an attractive enclosure. The unit is shipped fully assembled to ensure that all components arrive safely. However, before operating the computer the enclosure must be removed to connect the computer to the system peripheral devices. The following procedure describes the steps required to completely integrate the new computer into its operating environment.

1. Set unpacked chassis assembly in the approximate installation position.

NOTE

The chassis enclosure is secured to the chassis by three (3) oval-head screws on each side of the chassis and one (1) oval-head screw at the rear of the assembly as illustrated in figure 2-8.

2. Remove seven (7) oval-head screws and their associated finishing washers that secure the chassis enclosure to the chassis. Save screws and washers for reinstallation of enclosure.

3. Carefully lift enclosure up from the chassis and set enclosure in a safe place. Remove the shipping brackets that hold the logic boards in place and save for reuse at a later date in the event reshipment is necessary.

NOTE

The chassis is shipped from the factory with interrupts installed in predetermined locations as illustrated in figure 2-9. CRU addresses are fixed and cannot be changed.

4. Determine chassis location and interrupt assignments for each peripheral interface in system. If interrupt assignments do not match the factory-installed interrupts, or if additional interrupt assignments are required, perform interrupt installation procedure described in paragraph 2.6.

5. Remove the interface modules, memory boards and processor boards from the chassis one at a time, and refer to the circuit board jumper modifications paragraph 2.8.2 to verify that all jumper wires are properly installed. Return boards to original slots.

6. Install peripheral device interface cables on proper interface module in computer chassis as described in installation and operation manual included with peripheral device. All interface cables should be routed through cable clamps at rear of chassis and should exit at rear of chassis.

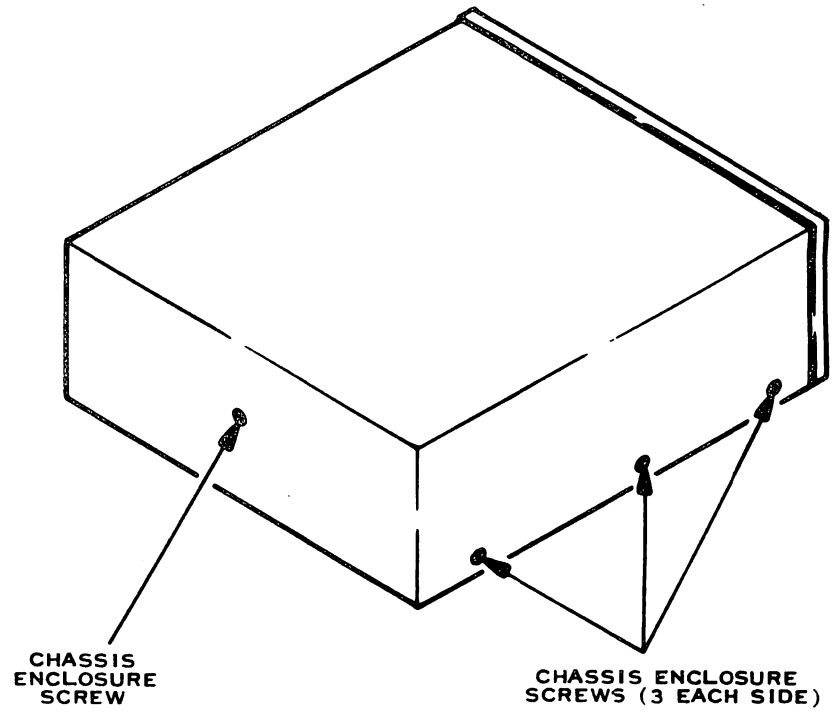
7. Connect ac power cord to a source of ac power with specifications applicable to equipment being installed.

8. Turn key switch on front panel to ON position (or UNLOCK on the programmer panel). Observe that POWER indicator and the RUN indicator on front panel light and that fans operate.

9. Perform system checkout procedure specified in paragraph 2.12.

10. Slip chassis enclosure over chassis and align it so that it mates properly with front panel and mounting-screw holes.

11. Secure chassis enclosure to chassis using seven oval-head screws and finishing washers removed in step 2.



(A)133299

Figure 2-8. Location of Chassis Enclosure Screws

SLOT NO.	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/5	N/A	N/A	990/5	N/A
2	0120		8	0100		4
3	00E0	911A VDT NO. 2	11	00C0	911A VDT NO. 1	11
4	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
5	0060		9	0040		9
6	0020		12	0000		13

(A) 6-SLOT PREWIRED CHASSIS

(A) 133082B

Figure 2-9. 6-Slot Chassis Prewired Configuration

12. Position computer in final installation site.

13. Perform system software installation procedures for operating system to be used with computer. For Texas Instruments supplied software, this information is provided in system operation guide for specific software package.

2.4 INSTALLATION (RACKMOUNT CHASSIS)

Either the 6-slot or the 13-slot chassis can be ordered for mounting in a 19-inch equipment rack. The chassis is shipped with all circuit boards installed in the chassis; the rackmounting hardware is packed in the same carton as the chassis. After performing the unpacking procedure, perform the following steps to install the computer in the rack.

NOTE

The following procedure requires access to the rear of installation rack after computer chassis is mounted in rack.

1. Set unpacked chassis assembly on a convenient work surface near equipment rack in which computer will be installed.

WARNING

Ensure that the power cord is not connected to a source of ac power before continuing with procedure. Failure to observe this precaution could result in severe electrical shock.

2. Remove six (6) screws that secure air filter and rear access plate to rear of chassis. It is not necessary to remove air filter from access plate.

3. Install two clip nuts in predrilled holes in chassis as illustrated in figure 2-10.

4. Reinstall rear access cover/air filter assembly using the six mounting screws removed in step 2.

5. Inspect the front and rear mounting supports in the rack (or desk) to ensure that distance between front and rear supports is 616 mm ± 6 mm (24-1/4 inches ± 1/4 inch) as illustrated in figure 2-11.

6. Determine desired vertical position of bottom edge of computer front panel. When using an EIA standard vertical support, the bottom edge of front panel must be centered between two holes that are 12.7 mm (0.5 inch) apart as illustrated in figure 2-12. Using that figure, locate position of two slide mounting holes on each of four mounting supports. These holes are 16.5 mm (0.65 inch) and 32.4 mm (1.275 inches) above the bottom edge of front panel.

7. Loosely install eight (8) 10-32 × 1/4 mounting screws and their associated flat washers and lock washers in eight selected holes in mounting supports (front and rear). Screws are installed from inside of enclosure as illustrated in figure 2-13.

8. Loosely assemble rear mounting brackets to slides using hardware provided with slides. Finger tighten rear mounting bracket screws.

9. Position left side against front and rear mounting supports such that slide mounting brackets fit between washers of mounting screws and mounting supports. Finger tighten four mounting screws to hold slide in place.

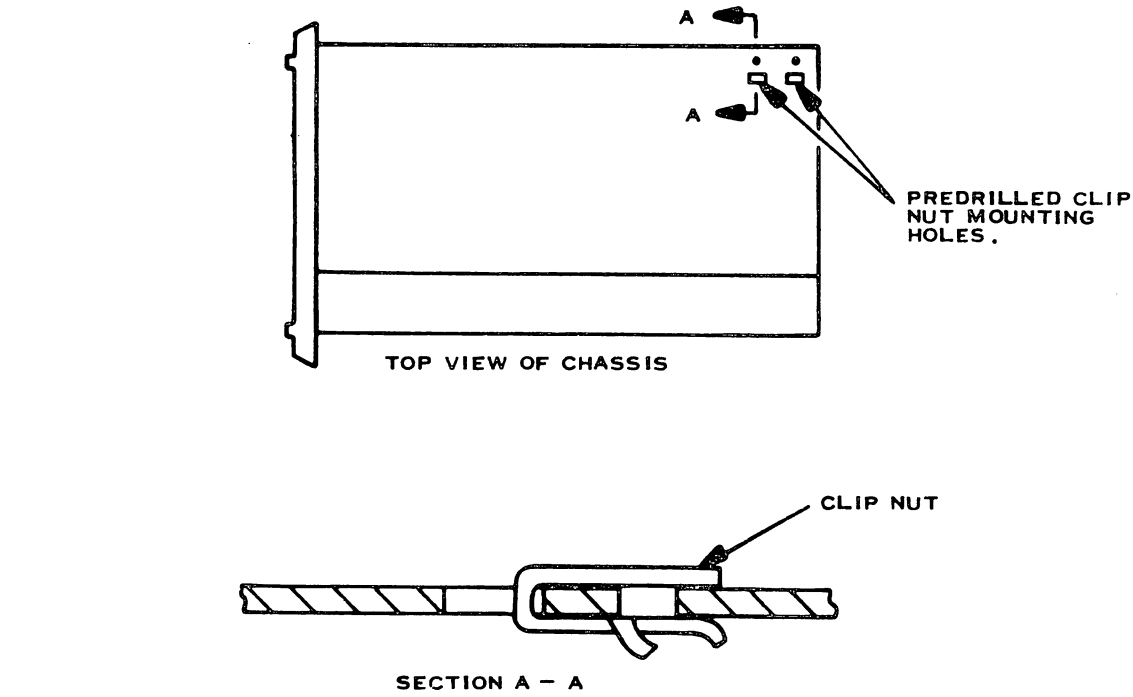


Figure 2-10. Clip Nut Installation

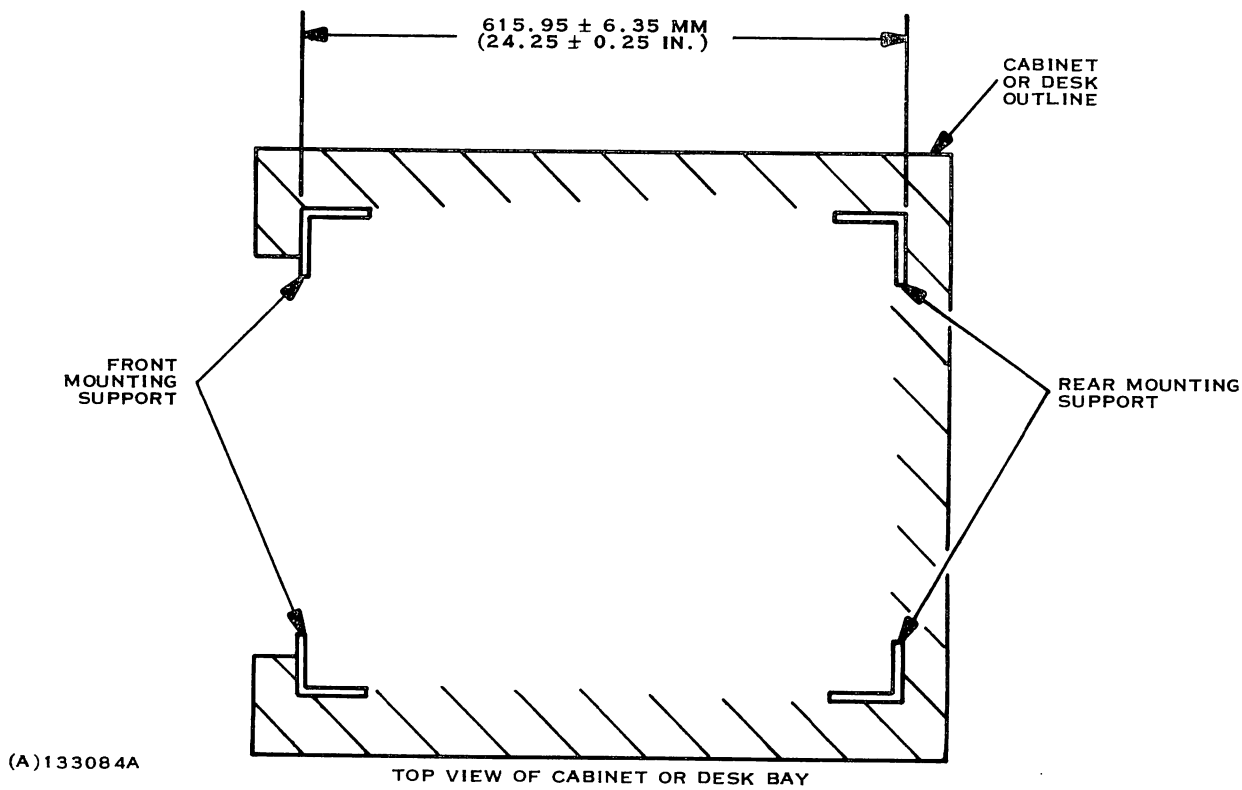


Figure 2-11. Mounting Cabinet Depth Specification

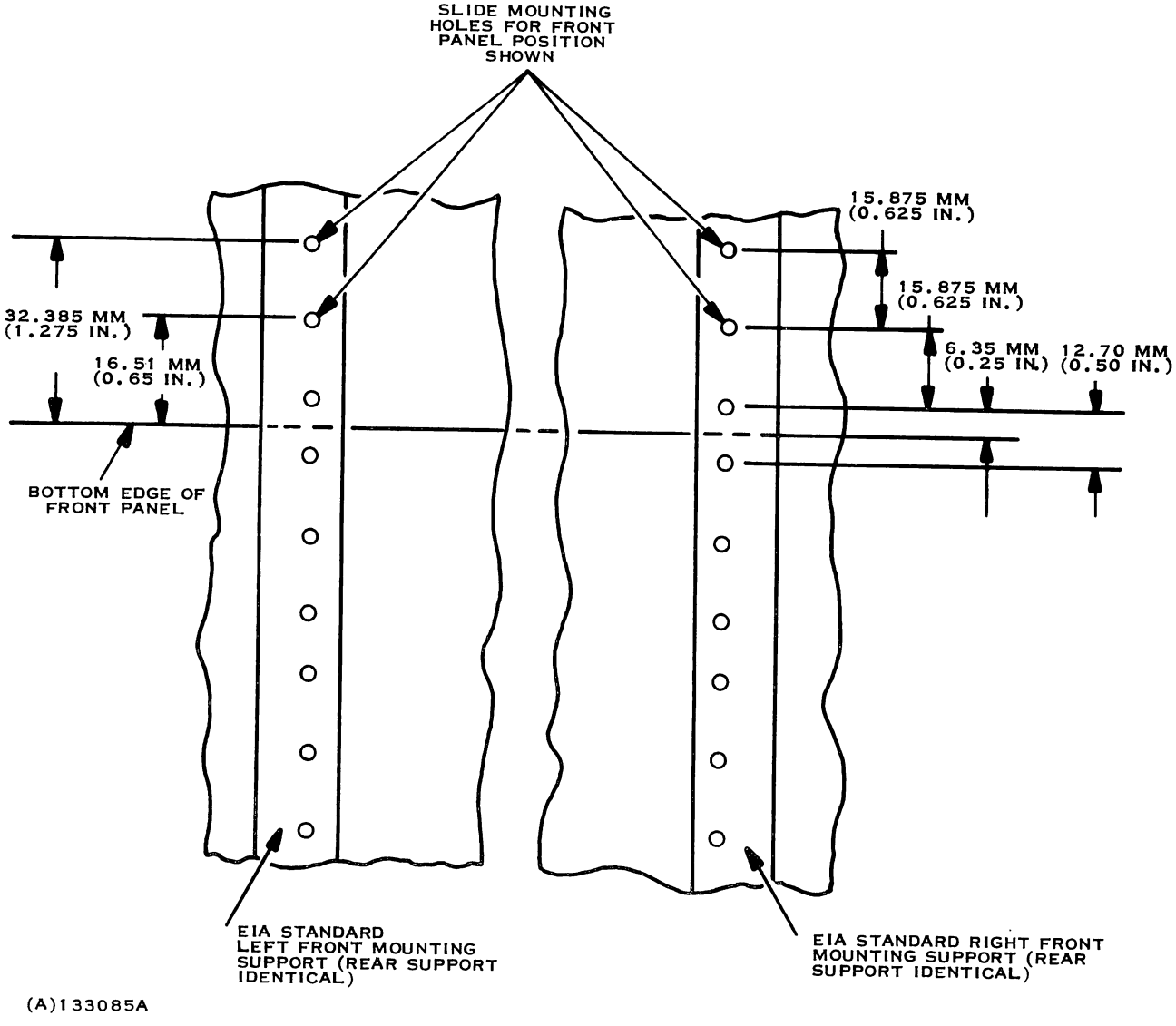


Figure 2-12. Mounting Hole Positioning

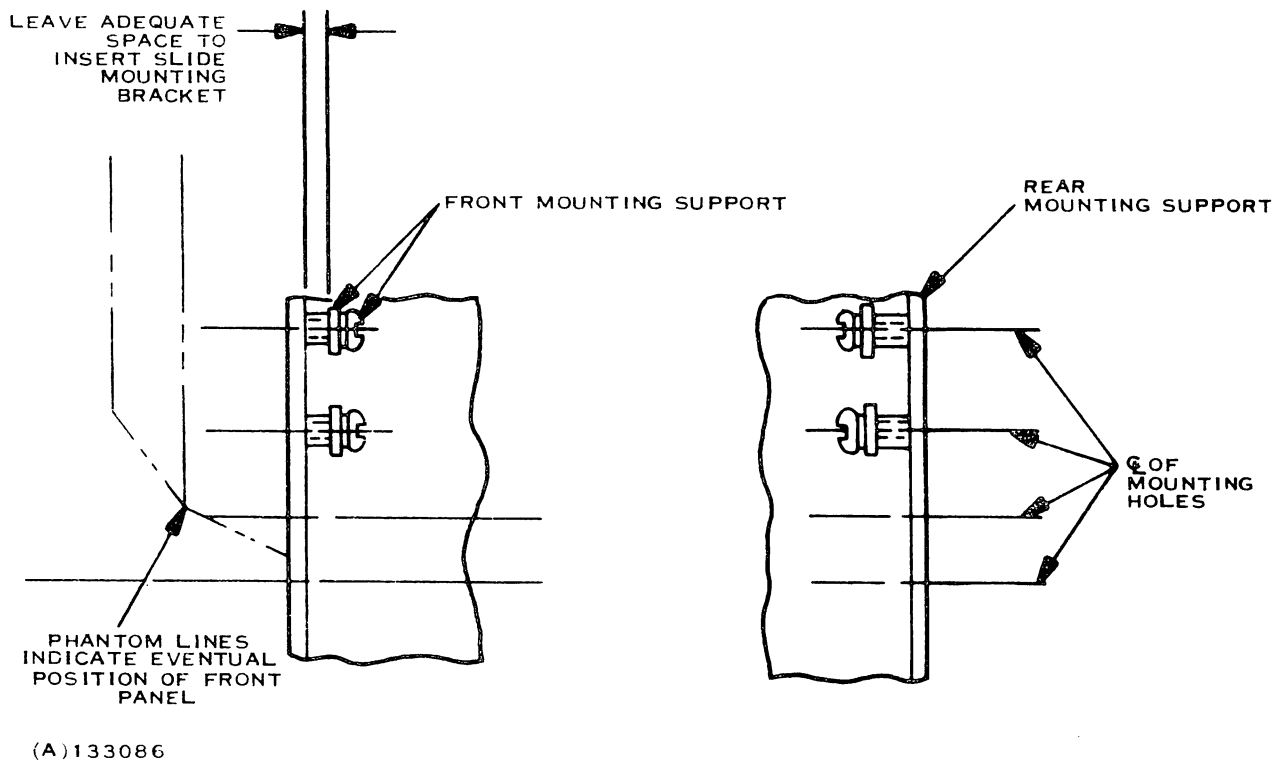


Figure 2-13. Mounting Screw Installation

10. Adjust slide so that distance from center of cabinet mounting screws to innermost point of slide assembly is 39.1 mm (1-1/2 inches) as illustrated in figure 2-14.

11. Ensure that slide assembly is square with cabinet mounting supports and tighten four (4) slide mounting screws and rear bracket mounting screws.

12. Repeat steps 9 through 11 with right side.

13. Extend both slides and release disconnect mechanism to remove inner slide member from slide assemblies.

14. Attach inner slide members to left and right underside of computer chassis using 6-32 × 1/4 self-tapping screws. Do not overtighten screws.

15. Mount ball stud to ball stud carrier bar using a 6-32 nut and lock washer as illustrated in figure 2-15.

16. Loosely attach ball stud carrier bar to top of computer chassis using 6-20 screws and flat washers inserted into clip nuts installed in chassis in step 3.

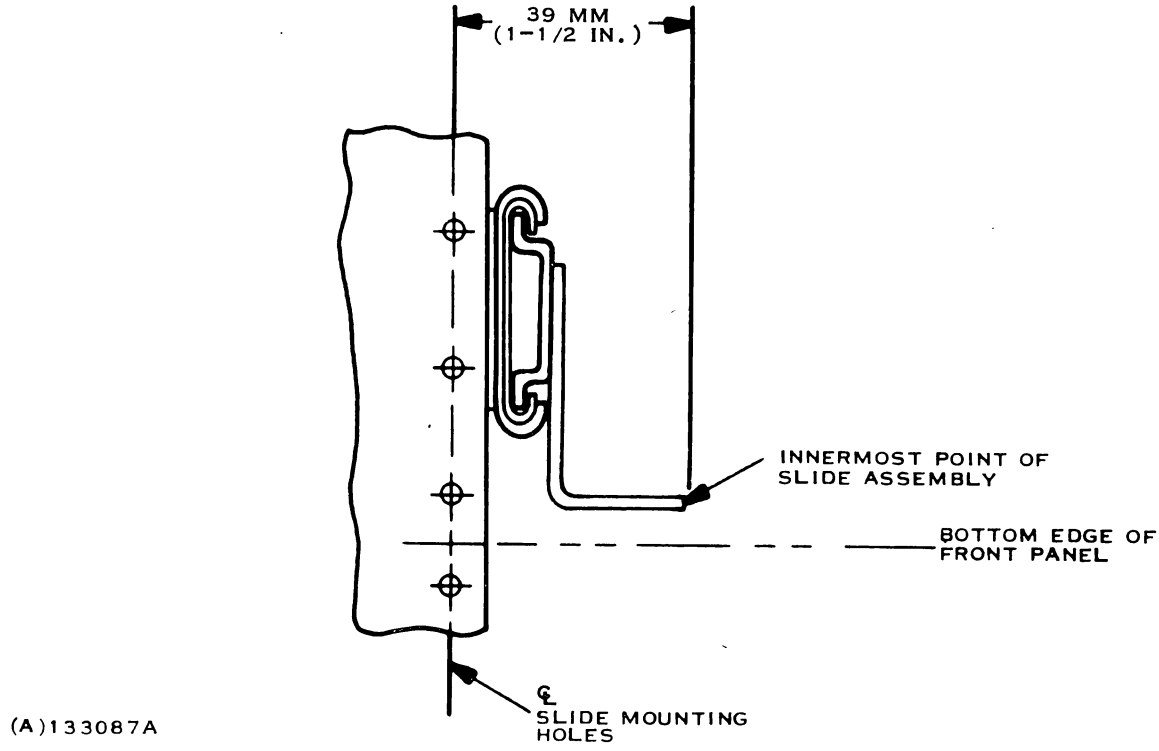


Figure 2-14. Chassis Slide Positioning

17. Insert chassis into mounted slides and reseat the disconnect mechanism. Push chassis into rack. During last inch of travel, lift front of chassis to ensure correct slide mating.

18. Assemble ball stud receptacle to stop plate using mounting hardware provided.

19. Install stop plate assembly to back edge of left rear mounting support of cabinet at a height such that ball stud receptacle mates with ball stud of the computer chassis.

20. Adjust forward-backward position of ball stud carrier bar on computer chassis such that chassis stops and ball stud latches into receptacle when back of front panel is between 0.8 mm to 1.6 mm (1/32 inch to 1/16 inch) from front mounting support of cabinet.

21. Slide computer chassis in and out of cabinet several times to ensure smooth operation and good alignment of all parts. Readjust as required.

22. Connect power cord from back of computer chassis to ac power distribution system of cabinet. Do not apply power at this time.

23. Slide chassis out from the cabinet to expose circuit boards mounted within the computer chassis. Remove shipping brackets that hold logic boards in place and save for reuse in the event reshipment is necessary.

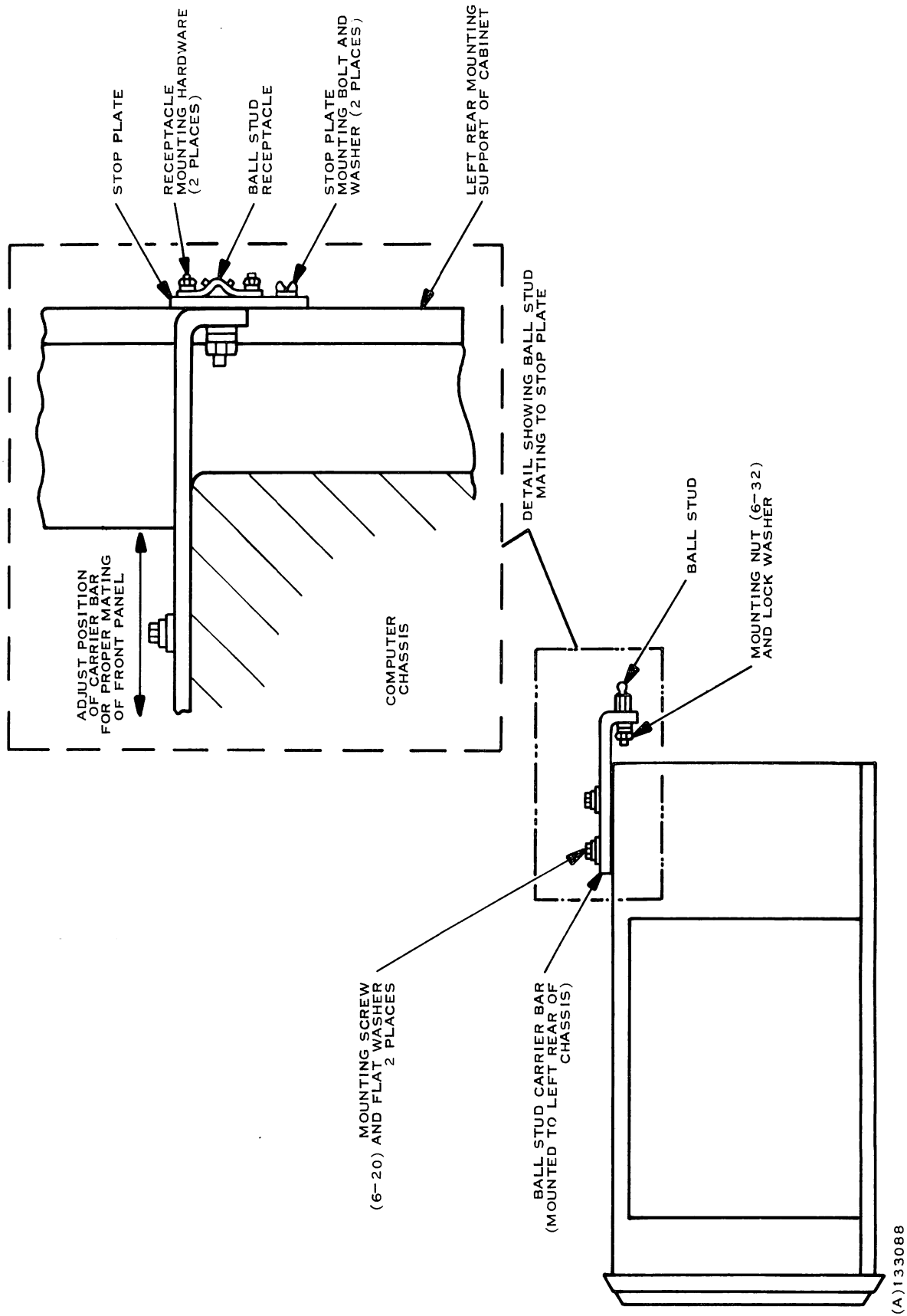


Figure 2-15. Installation of Ball Stud and Stop Plate

NOTE

The chassis is shipped from factory with interrupts installed in predetermined locations. Figure 2-16 illustrates these assignments for the 13-slot chassis; 6-slot chassis assignments are identical to those previously described for tabletop chassis. CRU addresses shown in figure cannot be changed.

24. Determine chassis location and interrupt assignments for each peripheral interface in system. If interrupt assignments do not match the factory-installed interrupts, or if additional interrupt assignments are required, perform interrupt installation procedure (paragraph 2.6) in this section of the manual. If board slot assignments are unknown or an expansion chassis is being used, refer to preparation of slot procedure in this section (paragraph 2.5).

25. Verify that all boards are in their proper slots and are firmly seated in chassis.

26. Install peripheral device interface cables on proper interface module in computer chassis as described in Installation and Operation manual included with peripheral device. All interface cables should be routed through cable clamps at the rear of chassis and should exit at rear of chassis.

27. Turn key switch on front panel to ON (on programmer panel to the UNLOCK) position. Observe that the POWER and RUN indicators on front panel light and that fans operate.

28. Perform the system checkout procedure specified in paragraph 2.12.

29. Slide computer into cabinet to complete final installation of computer.

30. Install blank panels (if supplied) to fill open spaces in cabinet or rack.

31. Perform system software installation procedures for the operating system to be used with computer. For Texas Instruments supplied software, this information is provided in the system operation guide for the specific software package.

2.5 PREPARING A SLOT LOCATION

Current production assemblies have the TILINE access granted jumpers accessible from the connector side of the motherboard when all boards are removed from the chassis. These jumpers are shown in figures 2-17 and 2-18. Simply remove the jumper plug (or cut the jumper, if the jumper is a wire) for the selected 990/5 slot, and reinstall all circuit boards in their proper locations. Therefore:

1. If 990/5 is to be host processor, the 990/5 must be located in slot 1.

2. All slots other than those containing TILINE master devices must have the TILINE access jumper installed.

3. All TILINE master devices must be installed in their proper locations with the jumper open.

SLOT NUMBER	P1 (TOWARD FRONT OF CHASSIS)			P2 (TOWARD REAR OF CHASSIS)		
	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/5	N/A	N/A	990/5	N/A
2	02E0		3	02C0		4
3	02A0		N/A	0280		N/A
4	0260		15	0240		15
5	0220		15	0200		15
6	01E0		10	01C0		10
7	01A0		13	0180		13
8	0160		12	0140		12
9	0120		10	0100		10
10	00E0	911 VDT NO. 2	11	00C0	911 VDT NO. 1	11
11	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
12	0060		9	0040		9
13	0020		15	0000		15

(A)133090B

(B) 13-SLOT PREWIRED CHASSIS

Figure 2-16. 13-Slot Chassis Prewired Configuration

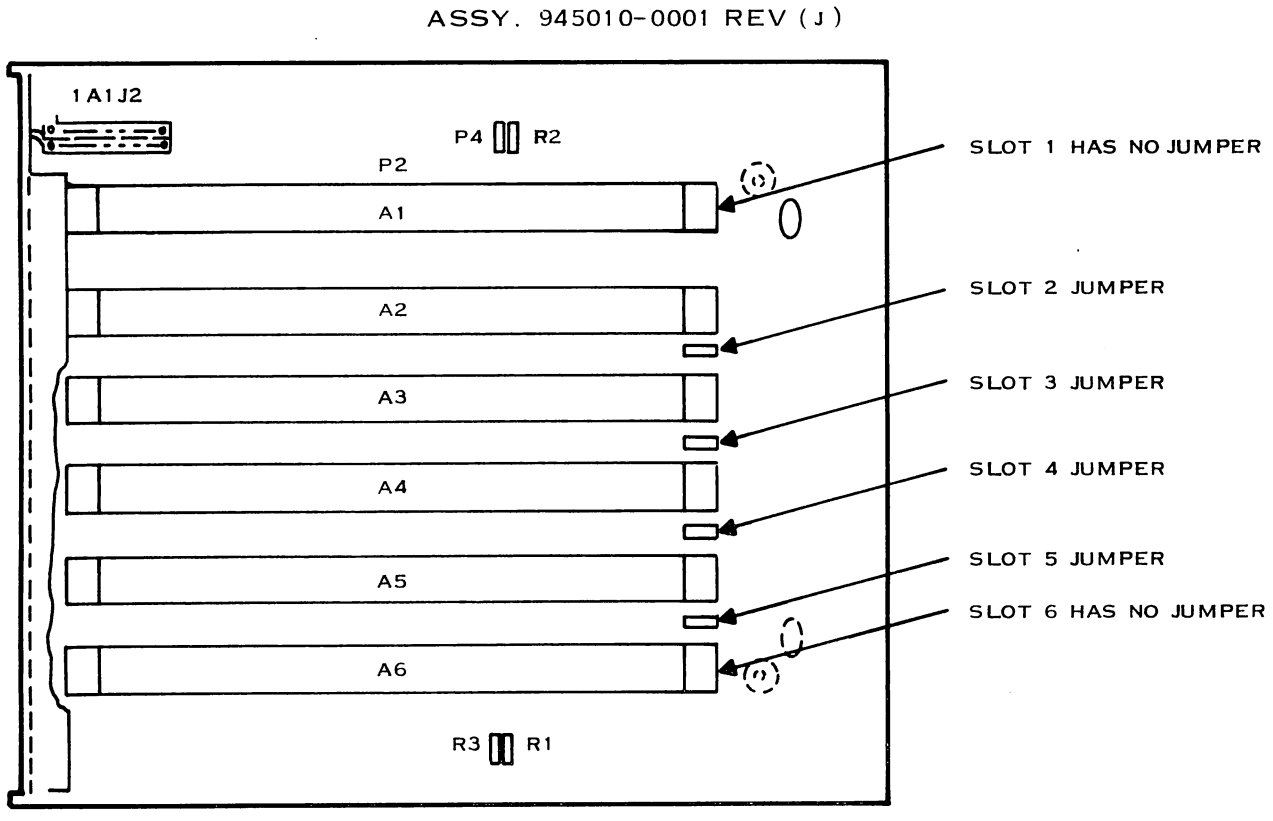


Figure 2-17. TILINE Access Granted Jumper Locations for 6-Slot Chassis (Current Production)

If the chassis is an early production version (i.e., it does not have jumpers as shown in figures 2-17 or 2-18), it is necessary to remove the back cover and power supply to gain access to the TILINE access granted jumpers. For these chassis, the following steps should be followed:

1. Turn off power and unplug the ac line cord.

WARNING

Lethal voltages are exposed when the access cover is removed. Power supply capacitors may retain charges long after ac power is removed.

2. Remove the left access cover (as viewed from the front of the chassis). The cover is fastened by 4 or 6 hex-head machine screws.

3. If the chassis is a 13-slot unit with a 20-amp power supply, slots 1-6 are visible above the power supply. To work on them, jump to step 5.

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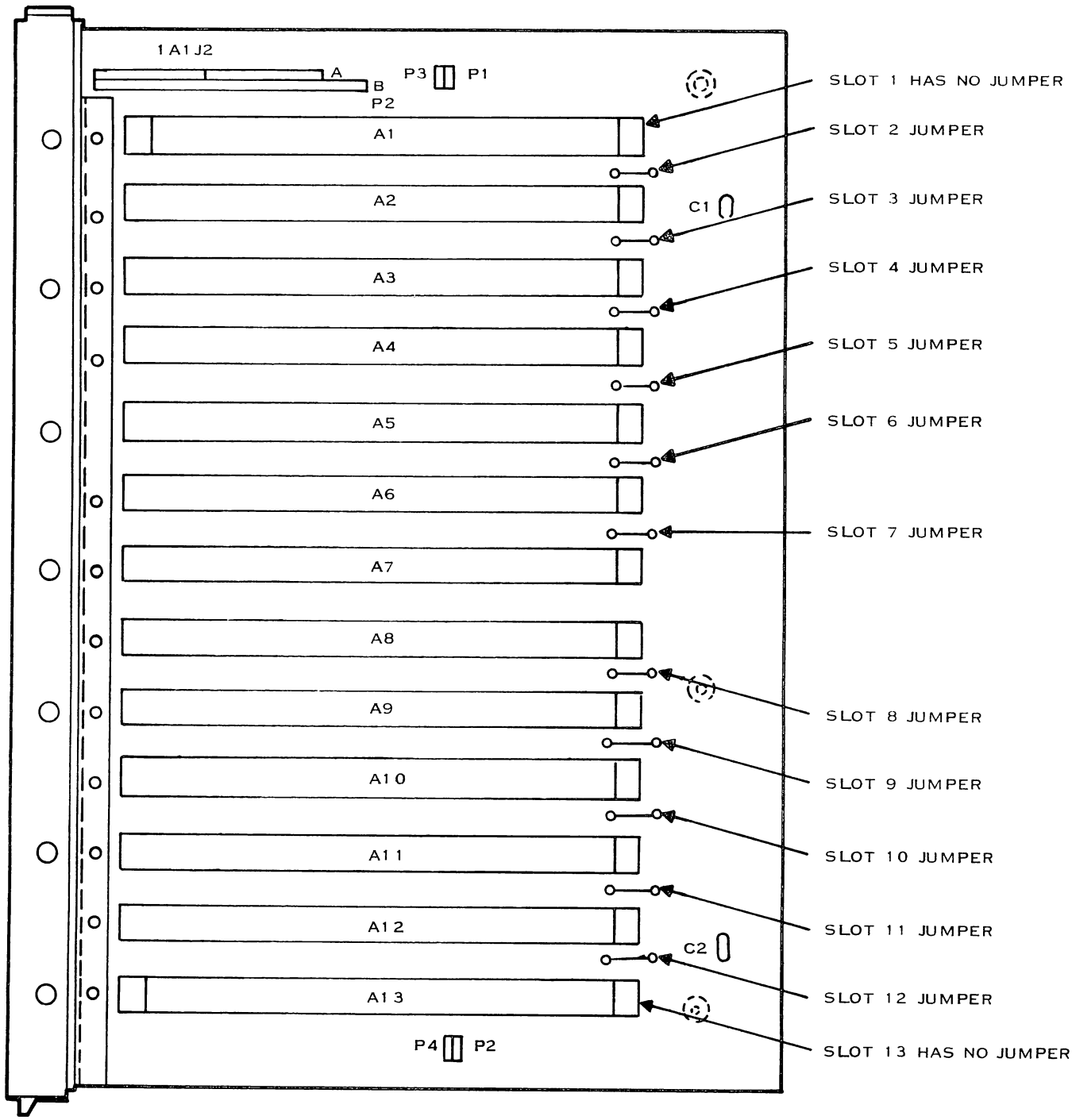


NOTE: JUMPER MAY BE EITHER A REMOVABLE JUMPER PLUG OR A WIRE WHICH MUST BE CUT.

(A) 138672

Figure 2-18. TILINE Granted Jumper Locations for 13-Slot Chassis (Current Production)

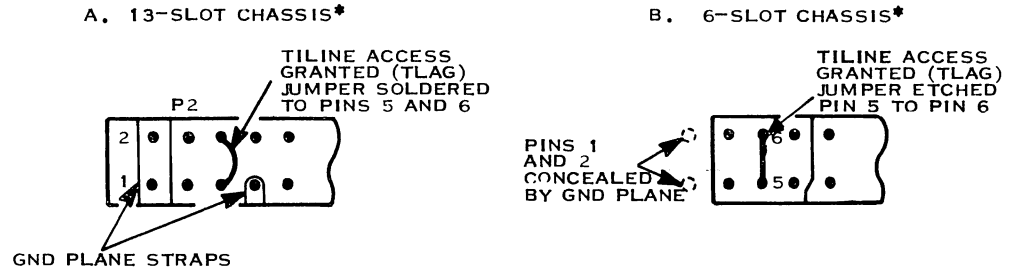
4. Remove the power supply as follows:

   a. Disconnect color-coded connectors from the component side of the power supply board.

   b. Unscrew the machine screws and standoffs which secure the power supply to the frame and to the motherboard.

   c. Carefully pull the power supply board straight forward until the connector at the bottom center of the power supply board is disengaged from the pins protruding from the motherboard. Lift the power supply board out of the chassis.

5. The rear of the motherboard is now exposed. The P2 connectors are at the left side, closest to the fan. Refer to figure 2-19, which gives detailed views of the left end of the P2 connector in a 13-slot and a 6-slot chassis.



*NOTE THESE ARE REAR VIEWS OF THE 990 MOTHERBOARD, I.E., VIEWS FROM THE POWER SUPPLY SIDE.

(A) 133946A

Figure 2-19. TILINE Access Granted Jumpers on the 990/5 Backpanel

In a 13-slot chassis, the TILINE access granted jumpers (P2-5 to P2-6) are wire loops soldered to the connector pins, as shown in view A.

In a 6-slot chassis, the jumpers are part of the printed circuit board etch, as shown in view B. Note that pins 1 and 2 are concealed by the ground plane.

To remove a jumper in the 13-slot chassis, clip the wire loop in two places and remove the excess wire. To remove a jumper in the 6-slot chassis, cut the jumper etch at two points with an X-acto* knife and lift or scrape away the excess conductor.

To install a jumper, solder a short length of #26 AWG wire between P2-5 and P2-6.

*X-acto is a registered trademark of X-acto Corporation.

6. To reinstall the power supply, proceed as follows:

CAUTION

The male pins protruding from the lower center of the motherboard are subject to bending if the mating connector on the power supply is not properly aligned with these pins.

a. Slip the power supply over the cable harness and into the side of the chassis. The metal-shell jumper connector (for the standby power supply) should appear at the bottom center of the power supply board.

b. Align the power supply circuit boards on the two alignment pins and *carefully* slide the board straight back so that the pins protruding from the motherboard slip into the connector on the power supply circuit board. View of these pins is blocked by the power supply board.

c. Reinstall the machine screws and standoffs which hold the power supply in place. Do not omit the lockwashers, as both mechanical and electrical connections are made by the machine screws and standoffs.

d. Reconnect the power supply to the wiring harness by installing the color-coded plastic connectors.

7. Replace the access cover.

2.6 INTERRUPT CONNECTIONS

Interrupt connections required to interface peripheral equipment to the 990/5 processor are usually made before the system is delivered to the customer. These interrupt assignments are coordinated with the software supplied with the system. However, if a controller, such as the TILINE Magnetic Tape Controller (TMTC), is not purchased as part of a system, the user may have to make the interrupt connections as part of the board installation. Standard Texas Instruments software "expects" to find the TILINE Magnetic Tape Controller interrupt assigned to interrupt level 9, which is connected to slot 5 in a 6-slot chassis or slot 12 in a 13-slot chassis. If the controller is installed in another slot, the interrupt jumpers will have to be changed, or a different interrupt level assigned in the software.

The 990/5 processor has 16 interrupt levels, numbered 0-15. Interrupt level 0, which is internal to the processor, has the highest priority. Interrupt levels 3 through 15 are external inputs which are available for assignment to peripheral controllers installed in the chassis. Interrupt level assignments must be coordinated with the software, so that the processor may correctly respond to (and clear) the interrupts.

Chassis backplane wiring brings the interrupt output lines from slots 2-13 and the processor interrupt input lines to wire-wrap pin headers adjacent to slot 1. Jumper wires between the pins connect the circuit board interrupt outputs to the processor interrupt inputs. These jumpers may run directly from pin-to-pin, or may be mounted on jumper plugs which slip over the pins. Figure 2-20 shows the jumper plugs installed in the chassis. The jumper wires are omitted for clarity.

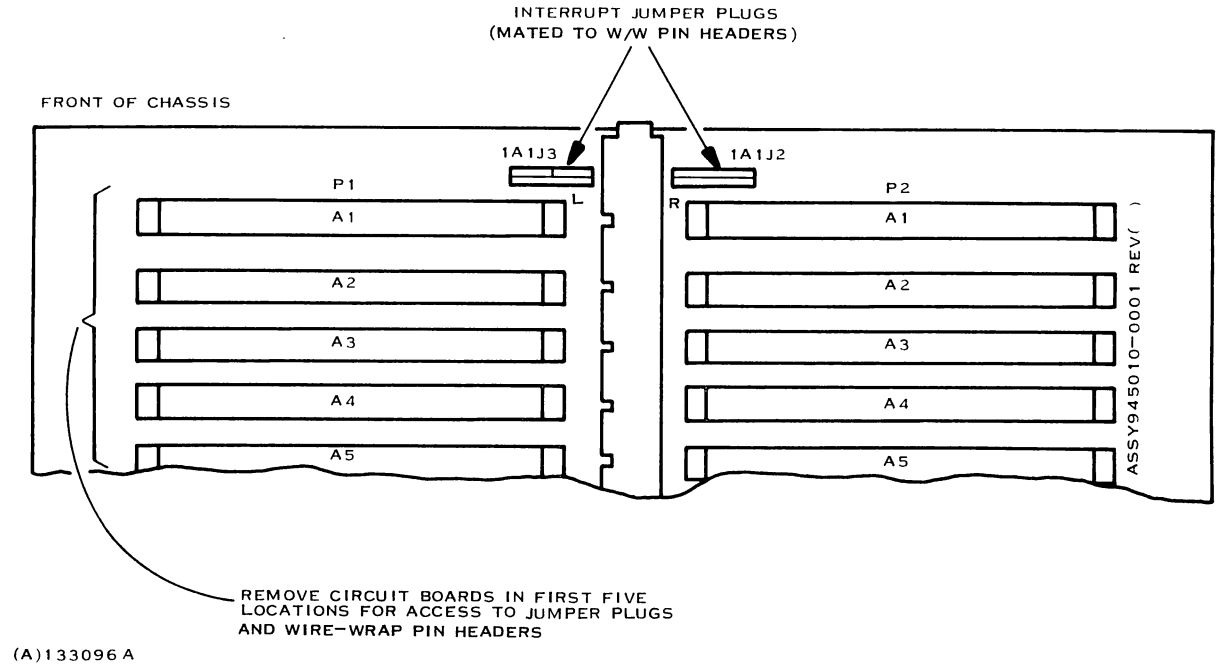


Figure 2-20. Location of Interrupt Jumpers (6- and 13-Slot Chassis)

There are two rows of pins in the header. The top row has 15 pins connected through the backplane to the 15 interrupt levels of the processor. Additional pins on the top row are provided in the 13-slot chassis for special configurations, such as CRU expansion. The bottom row contains 48 pins in a 13-slot chassis or 20 pins in a 6-slot chassis. Two of these pins are wired to each of the possible circuit board interrupt outputs. This allows multiple interrupts to be connected to one interrupt level.

Interrupt pin assignments are shown in figures 2-21 and 2-22, each figure presenting a view of the jumper plugs as seen from the jumper wire side. The "X" marks identify jumper plug positions which have no corresponding pins on the header. The "O" marks identify jumper plug positions which have no corresponding pins on the early production header.

The configuration chart on top of the chassis details the interrupt level and chassis slot assignments. Any modifications should be recorded on the chart.

The information presented here is a brief summary of procedures to be covered in a detailed 990/5 maintenance manual.

CAUTION

Do not remove or install any circuit board or modify any jumper while power is applied to the 990/5.

To gain access to the interrupt jumpers, remove the circuit boards installed in slots 1-5. The interrupt jumpers will be visible on the motherboard just above the slot 1 connectors. The interrupt output of a full-sized board, such as the TMTC, is on P2 of the assigned slot location. Therefore, if slot 8 is chosen for the TMTC, the interrupt output will be found at 8P2 of the wire-wrap pin header. A single jumper should be run from 8P2 pin to the selected interrupt level input to the processor. Level 9 is standard for Texas Instruments tape control software. A jumper is installed between 8P2 and level 9 as part of the standard 990 chassis configuration.

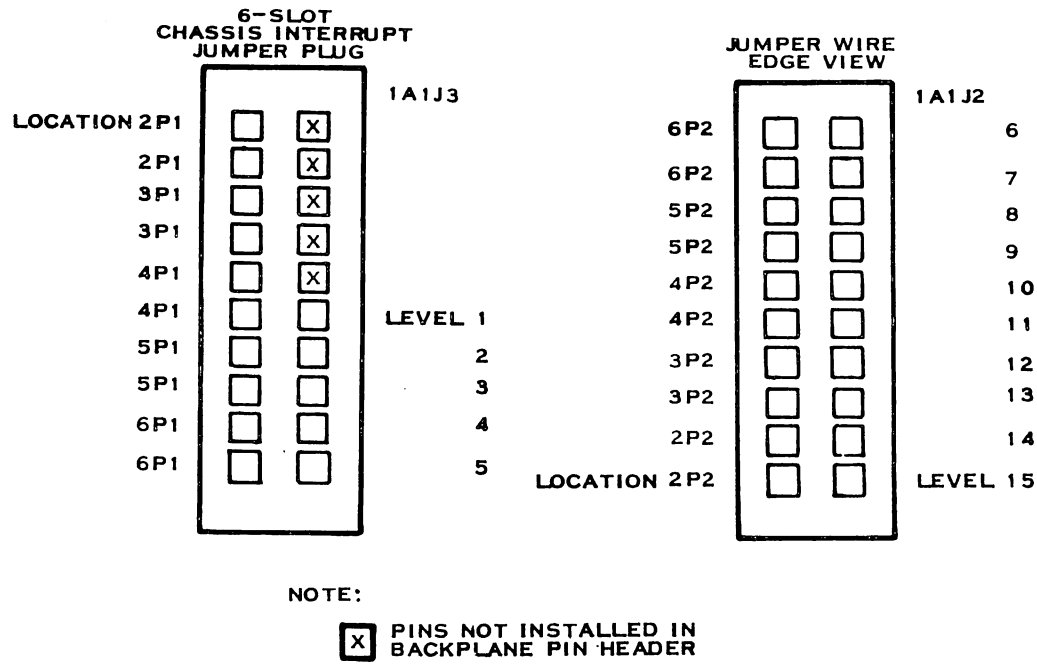


Figure 2-21. 6-Slot Chassis Interrupt Jumper Plugs

After completing any interrupt jumper modifications, carefully reinstall the removed circuit boards (component side up) according to the configuration chart fastened to the top of the computer. Update the configuration chart to correspond to the interrupt jumper modifications.

NOTE

System software is highly dependent on the interrupt structure of the computer. Any deviations from standard interrupt configurations must be brought to the attention of the system programmer before or during software installation.

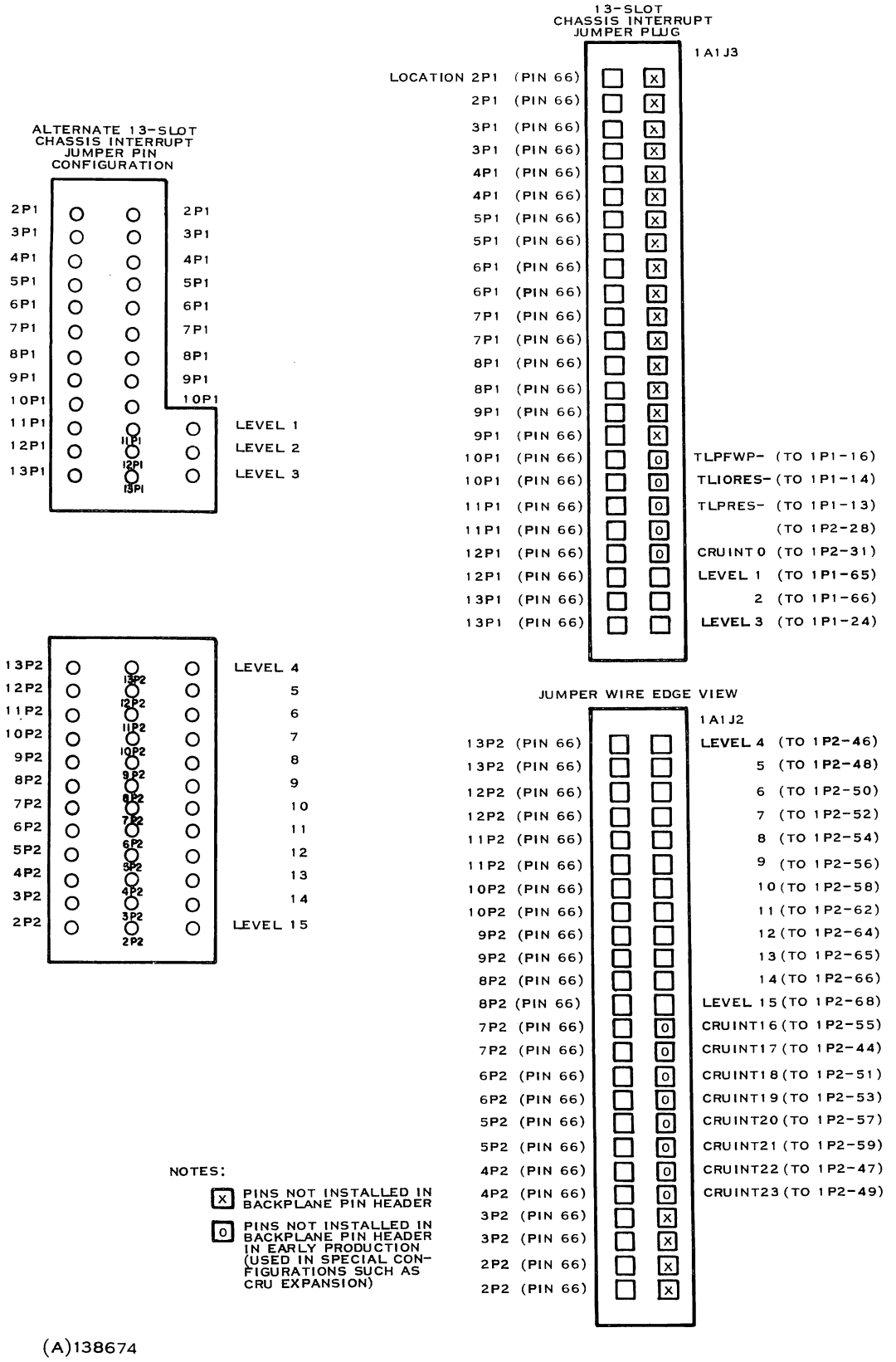


Figure 2-22. 13-Slot Chassis Interrupt Jumper Plugs

2.7 MEMORY CONFIGURATION

The starting address associated with each memory board is normally set up at the factory. For changes to the standard memory system, refer to the memory board address settings provided in Section III of this manual.

2.8 CRU EXPANSION INSTALLATION REQUIREMENTS

Up to seven I/O expansion chassis may be connected to the main chassis when configuring larger 990/5 systems. The electrical interconnection between the main chassis backpanel and the expansion chassis is accomplished via the CRU expansion board which is installed in an unused card slot in the main chassis. The CRU expansion board contains seven top-edge connectors designated P3 through P9 (figure 2-23), each of which contains all necessary data, address, interrupt and interrupt identification lines required to link an external chassis to the main chassis.

Typically, the plugs are assigned to the expansion chassis as follows:

P3 — expansion chassis 1 (buffer board in slot 1 of the expansion chassis must also be programmed for the chassis 1 ID)

P4 — expansion chassis 2

.

.

.

P9 — expansion chassis 9

2.8.1 CRU EXPANSION BOARD JUMPER OPTIONS. The jumper options on the CRU expansion board include:

- Jumper-wire selection of either power-up reset signal (TLPRES—) from the power supply or IORES— from the 990/5 board in the main chassis. Typically, the IORES— signal is used which includes an OR of the main chassis power supply power-on reset and the software CLR instruction (jumper connected between terminals E3 and E4; terminals E1 and E2 are both open).

- Interrupt section enable option. If four or less expansion chassis are being used, interrupt Section A is enabled (jumper wire between E5 and E6) and interrupt Section B is disabled (jumper wire removed between terminals E7 and E8). If five or more chassis are being installed, both sections must be enabled.

These jumper options are shown in figure 2-23 and summarized in table 2-2.

2.8.2 CRU BUFFER BOARD JUMPER OPTIONS. The CRU buffer board in each expansion chassis must be programmed with the proper chassis ID. In the standard configuration, the chassis which is cabled to P3 on the CRU expansion board in the main chassis is designated chassis 1, and the expansion chassis connected to J9 is designated chassis 7 (in numerical order). The chassis ID must then be programmed on the CRU buffer board which is installed in slot 1 of each expansion chassis. The chassis ID is set up by installing plug P4 in the selected position 1 through 7 (see figure 2-24).

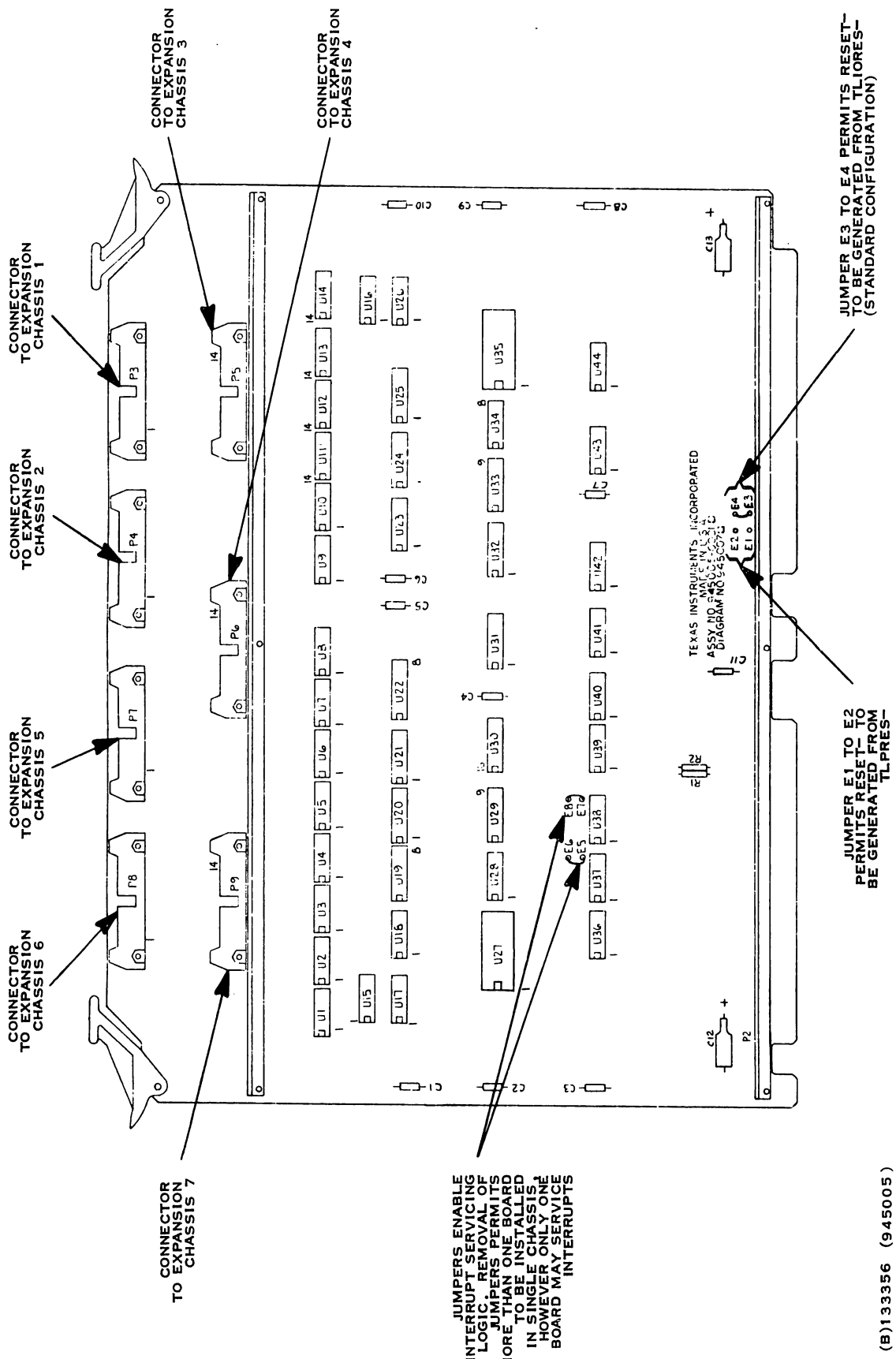


Figure 2-23. CRU Expansion Board Options

Table 2-2. CRU Expansion Board Jumper Options

Reset Source	Jumper Required
TLPRES–	Jumper E1 to E2; E3 and E4 OPEN
IORES–	Jumper E3 to E4; E1 and E2 OPEN

Interrupt Section Enable Option	Jumper Required
Interrupt Section A enabled	Jumper E5 to E6
Interrupt Section B enabled	Jumper E7 to E8

The CRU buffer board also contains provisions for bypassing the interrupt scanner for interrupt level 1 when a peripheral requiring fast interrupt response time is implemented in an expansion chassis. In this case, J1 is installed in D11 and D12. For normal interrupt scanner processing of interrupt level 1, J1 is installed in D13 and D14.

For normal operation, the internal clock enable jumper must be installed between terminals E1 and E2. For maintenance purposes, the internal clock may be disabled by removing this jumper. An external clock source may be connected to the board via terminal E3, and the scan counter may be cleared by temporarily applying a ground to terminal E4. The CRU buffer board jumper options are summarized in table 2-3.

2.8.3 EXPANSION CHASSIS INTERRUPT WIRING. The interrupt wiring for each expansion chassis is performed in a similar fashion to that used in the main chassis.

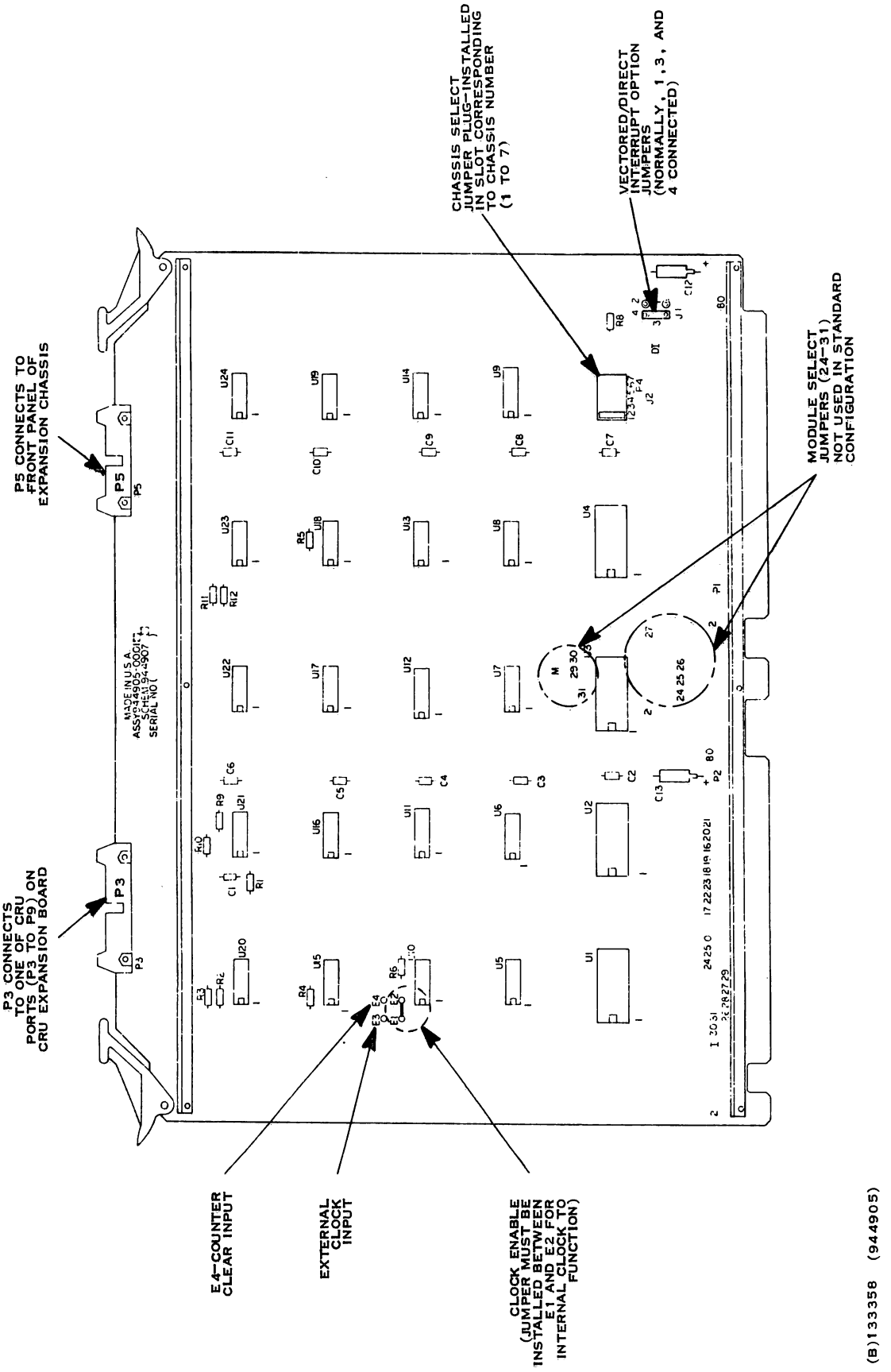


Figure 2-24. CRU Buffer Board Options

Table 2-3. CRU Buffer Board Jumper Options

Chassis ID Select	Jumper Required
1	P4 in position 1 of J2
2	P4 in position 2 of J2
.	.
.	.
.	.
7	P4 in position 7 of J2

Internal Clock Option	Jumper Required
Normal operating system	E1 to E2
Clock disabled	E1 and E2 open

Vectored/Direct Interrupt Option	Jumper Required
Level 1 vectored	J1 in D13, D14
Level 1 direct	J1 in D11, D12

2.9 TILINE EXPANSION

Multiple TILINE chassis to accommodate expansion memory and/or TILINE controllers may be installed on a 990/5 system. The TILINE electrical interconnections between the main chassis backpanel and the backpanel of a 990 expansion chassis are accomplished by installing a TILINE coupler module in the main chassis and a similar TILINE coupler in a 990 expansion chassis. The two couplers are interconnected via two 3.66 metre (12-foot), 60-ohm, shielded, ribbon cables (one 40 conductor cable and one 20 conductor cable). The cabling configuration is shown in figure 2-25.

There are two major types of TILINE devices, masters and slaves. TILINE masters, such as a 990/5 processor, may initiate data transfer operations on the TILINE. Slave devices, such as an expansion memory, are commanded by a master to accept or to transmit data. Some TILINE peripherals, such as a disk controller, can operate either as masters or slaves.

In order to avoid conflicts between competing masters within a chassis, a positional priority scheme is used. This scheme is used in all chassis connected by the TILINE link. The signal line which establishes positional priority among masters is wired along the P2 side of each chassis. The conductor for this signal (TLAG) shorts pins 5 and 6 of the P2 connectors at all slot positions except slot 1 and slot 7.

The first TILINE master device plugged into the chassis (other than in slot 1) should go into slot 7. TILINE master devices may be plugged into other slots, as long as the etch between pins 5 and 6 is cut.

The functions of the TILINE couplers include:

- Address and data buffering between TILINEs
- Address translation for remote memory mapping
- Resolution of timing conflicts in multiprocessor systems
- Providing intersystem interrupt capability and power status via the CRU.

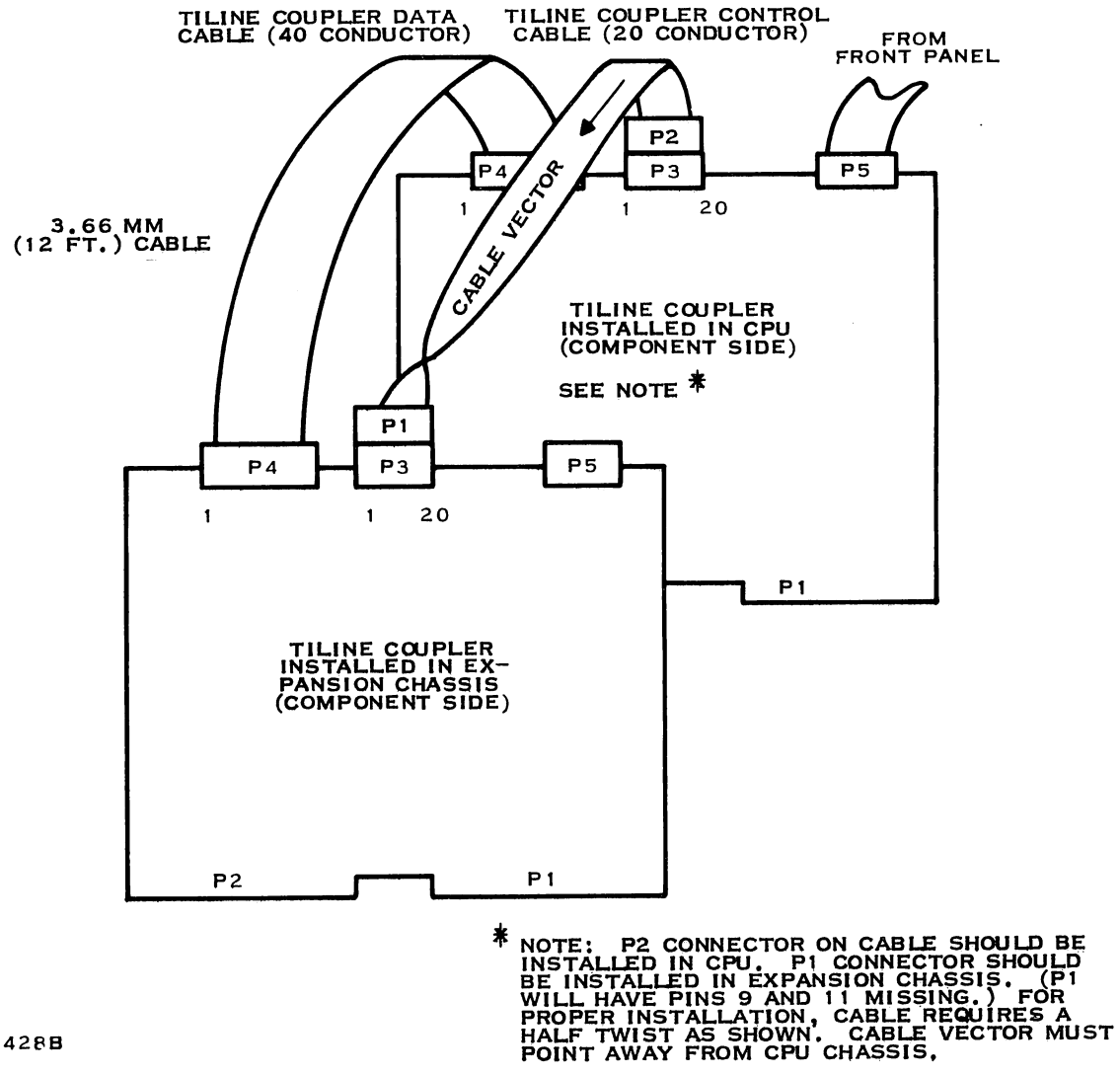


Figure 2-25. TILINE Expansion Cabling

2.9.1 TILINE COUPLER ADDRESS OPTIONS. The TILINE coupler contains three sets of switches that permit the user to assign a memory map for remote addresses. The address space recognized by the local coupler may be changed in 4K increments from 0 to 1 million words using two of the three sets of eight slide switches (figure 2-26). A bias value between 0 and 1020K (in 4K increments) may also be added to the local TILINE address before it is sent to the remote coupler. The bias value is programmed on the coupler using the third set of eight switches.

2.9.1.1 Address Recognized By Coupler. The lower bound switches are used to select the lowest address that will be recognized by the coupler. The decimal equivalent of the binary number set up by these switches is the number of the lowest 4K bank that will be recognized.

Similarly, the upper bound switches are used to enter a binary value whose decimal equivalent reflects the highest 4K bank that will be recognized. Table 2-4 contains several examples of address space and associated switch settings.

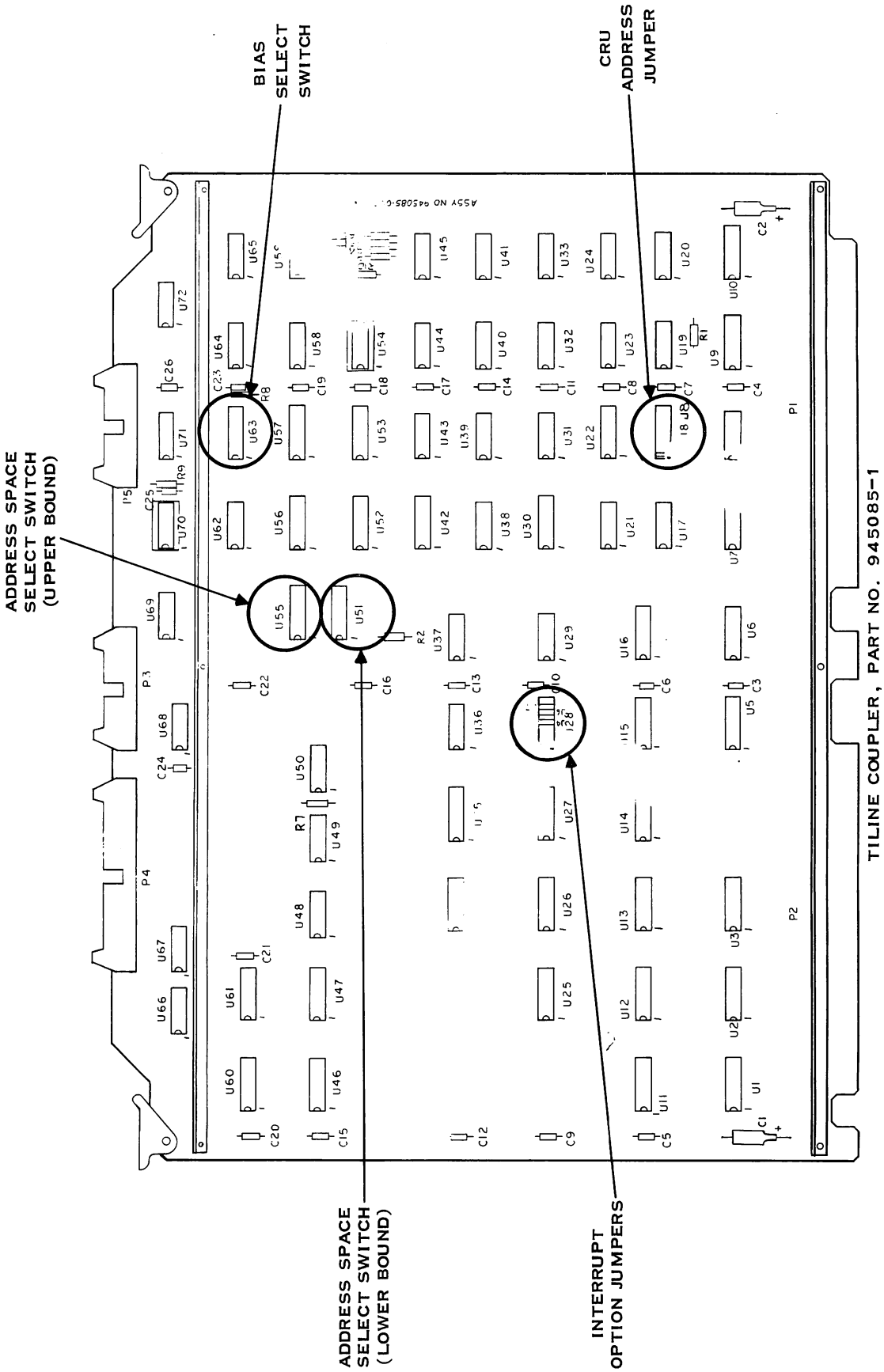


Figure 2-26. TILINE Coupler Options

Table 2-4. Examples of TILINE Coupler Address Space Switch Settings

	ADDRESS SPACE	LOWER BOUND SWITCH								UPPER BOUND SWITCH							
DECIMAL	RECOGNIZED ADDRESS (HEX)	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
0-4K	00000-00FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4K-8K	01000-01FFF	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
8K-12K	02000-02FFF	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
12K-16K	03000-03FFF	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
0-8K	00000-01FFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0-16K	00000-03FFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0-20K	00000-04FFF	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
8K-16K	02000-03FFF	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
32K-64K	08000-0FFFF	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1
64K-320K	10000-4CFFF	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0
0	NONE	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

SWITCH POSITION
1 = OFF, 0 = ON

2.9.1.2 Address Bias Options. The third set of 8 slide switches permits the user to select an 8-bit bias value that may be added to the eight most significant bits of the 20-bit TILINE address before the address is passed on to the remote coupler. This bias feature allows a single block of memory or single TILINE peripheral to be shared among several CPUs. Each CPU may use a different address which is biased to the actual TILINE address by the coupler. Table 2-5 shows several examples of biasing using the bias switches on the coupler.

NOTE

If the TILINE address is within the TILINE peripheral control space ($\geq FFC00_{16}$), whether or not the bias value is added to the address is a jumper option as described in paragraph 2.9.5.

2.9.2 TILINE COUPLER INTERRUPT OPTIONS. Each coupler includes a CRU interface for a maskable interrupt feature in which two input and two output bits are implemented, and a nonmaskable interrupt that may be jumpered as an incoming or outgoing interrupt.

2.9.2.1 CRU Dedicated Start Address Option. The couplers CRU section may be assigned a dedicated address beginning at one of eight different addresses controlled by the position of jumper J8 as indicated in table 2-6.

2.9.2.2 Optional Interrupt Configurations. In addition to the CRU starting address jumper, four other jumpers (J1-J4) may be used to set up a wide variety of interrupt configurations.

The jumpers, when inserted, perform the following functions:

- J1 — sends direct nonmaskable interrupt out
- J2 — brings direct nonmaskable interrupt in

- J3 — sends direct maskable interrupt out
- J4 — sends CRU maskable interrupt out.

The coupler's interrupt circuitry is shown in figure 2-27. In this example, the following conditions exist:

- Disk A can directly interrupt CPU B
- CPU A can interrupt CPU B via the CRU
- CPU B can mask the interrupt from CPU A
- Disk B can interrupt CPU B.

Table 2-5. Examples of TILINE Coupler Bias Switch Settings

Local TILINE Address	Bias	Bias Switch 1 2 3 4 5 6 7 8	Remote TILINE Address
00000	16K	0 0 0 0 0 1 0 0	04000
032CF	4K	0 0 0 0 0 0 0 1	042CF
02F10	1016K (-8K)	1 1 1 1 1 1 1 0	00F10
04000	992K	1 1 1 1 1 0 0 0	FC000
FFC40	1016K (-8K)	1 1 1 1 1 1 1 0	FFC40 (J4 removed) FDC40 (J7 installed)

SWITCH POSITION
1 = OFF, 0 = ON

Table 2-6. TILINE CRU Address Jumpers

Jumper Position (J8)	CRU Address	Base Address
1	FA0	1F40
2	FA2	
3	FA4	
4	FA6	
5	FA8	
6	FAA	
7	FAC	
8	FAE	

2.9.3 IORESET JUMPER OPTION. IORESET may be propagated in the direction of the cable vector to the remote TILINE. This option is disabled by removing jumper J5 (figure 2-27).

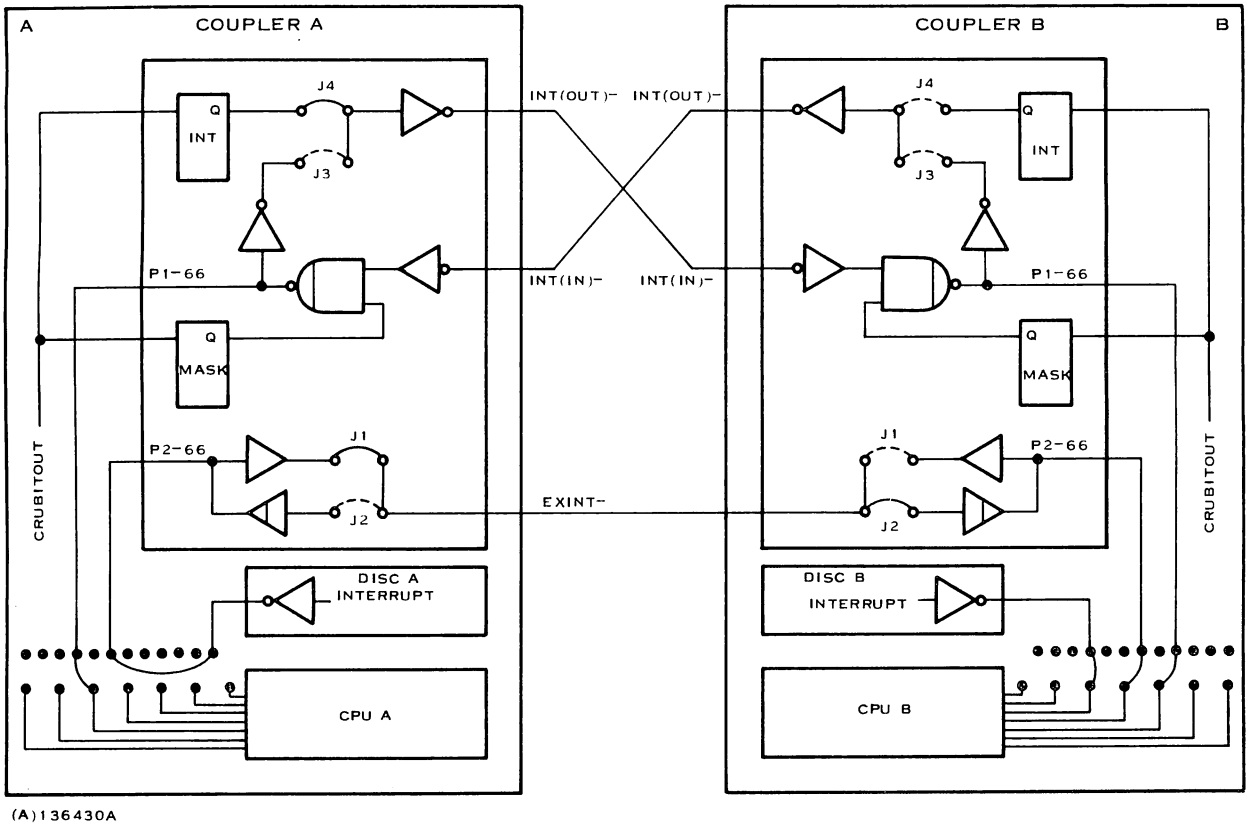


Figure 2-27. TILINE Coupler Interrupt Circuitry, Functional Block Diagram

2.9.4 WRITING TO REMOTE SLAVE OPTION. The data path between two couplers may be assigned as read-only in one or both directions. Removal of jumper J6 disables a coupler from writing to a remote slave.

2.9.5 PERIPHERAL CONTROL SPACE ADDRESS OPTION. By inserting jumper J7, the circuitry used to detect an address in the TILINE peripheral control space address is disabled. If the jumper is used, all addresses sent to the remote coupler have the bias value added in. If the jumper is removed, all addresses except those in the TILINE peripheral control space address have the bias value added.

2.10 LOGIC BOARD INSTALLATION PROCEDURES

Before installing a logic board in the main chassis or one of the expansion chassis, the chassis map located on top of the chassis should be consulted. If adding a new board to the system, the preparation and planning paragraph starting at paragraph 2.5 in this section should be consulted to ensure that the interrupt and CRU addressing requirements of the system are being met. In general, logic boards are either half-sized or full-sized boards. The half-sized boards require the addition of a center card guide into the selected card slot prior to the installation of the logic board.

Procedures for installing both types of logic boards are provided in the following paragraphs.

2.10.1 FULL-SIZED LOGIC BOARD INSTALLATION. The following procedure should be used to install a full-sized logic board into a 990 chassis:

1. Set the key switch on the chassis front panel to the OFF position.

CAUTION

Failure to shut off power to the chassis when installing or removing a logic board may result in damage to the board due to temporary misalignment of board and connector pins.

2. Insert the board into the selected slot of the chassis with the component side of the board facing upward.

3. Ensure that the slots in the circuit board mate properly with the alignment comb on the backpanel connector.

4. Press the board firmly into place, and ensure that the board is properly seated.

5. For a CRU interface board, refer to the associated Installation and Operation manual for cabling information.

6. The board may be removed from the chassis by removing the interface cable and lifting the plastic, pivoted tabs (card ejectors) to free the board from the chassis backpanel.

2.10.2 HALF-SIZED LOGIC BOARDS. Half-sized logic boards may be installed in a 990 chassis using the following procedure:

1. If a center card guide is installed in the desired slot, proceed to step 7. If the center card guide is *not* installed, proceed to step 2.

2. Disconnect the chassis ac power cord from its ac power source.

WARNING

The center card guide installation procedure requires exposure to dangerous ac voltages unless the chassis is disconnected from the ac power source.

3. If the card guide is being installed on a 6-slot or 13-slot chassis, the left-side access panel and the power supply board(s) must be removed. The standby power supply (when used) is mounted piggyback over the main power supply board. To remove the standby supply board, disconnect cable connector plugs 1A6P1 and 1A6P2 and remove five holding screws. To remove the main power supply board, disconnect cable connectors 1A3P1 and 1A3P2 and remove four holding screws and three standoffs from the center of the board.

4. Examine the card comb located between the two rows of connectors on the front side of the motherboard. If a screw is located between the two connectors in the position where the card guide is to be installed, remove the screw and associated hardware from the motherboard and install in an adjacent hole either above or below the original location.

5. Install the center card guide, part number 945226-0001, using a flat washer and screw as shown in figure 2-28. Inspect the card guide to ensure that it is not rotated with respect to the card comb. Correct if misaligned.

NOTE

If two half-sized logic cards are being installed in the same full-sized chassis slot, center the card guide. If only one card is being installed, mount the card guide toward the side of the chassis where the logic card is being installed.

6. Replace the main power supply board and the standby power supply board (if used). Ensure that all screws and standoffs are snug and that all connectors are properly installed. Replace the side access panel.

7. Insert the logic board into the selected half-slot chassis location with the component side of the board facing upward.

8. Ensure that the slots in the circuit board mate properly with the alignment comb on the backpanel connector. Press the board firmly into position.

9. Refer to the associated installation and operation manual for the CRU logic card type for additional cabling information.

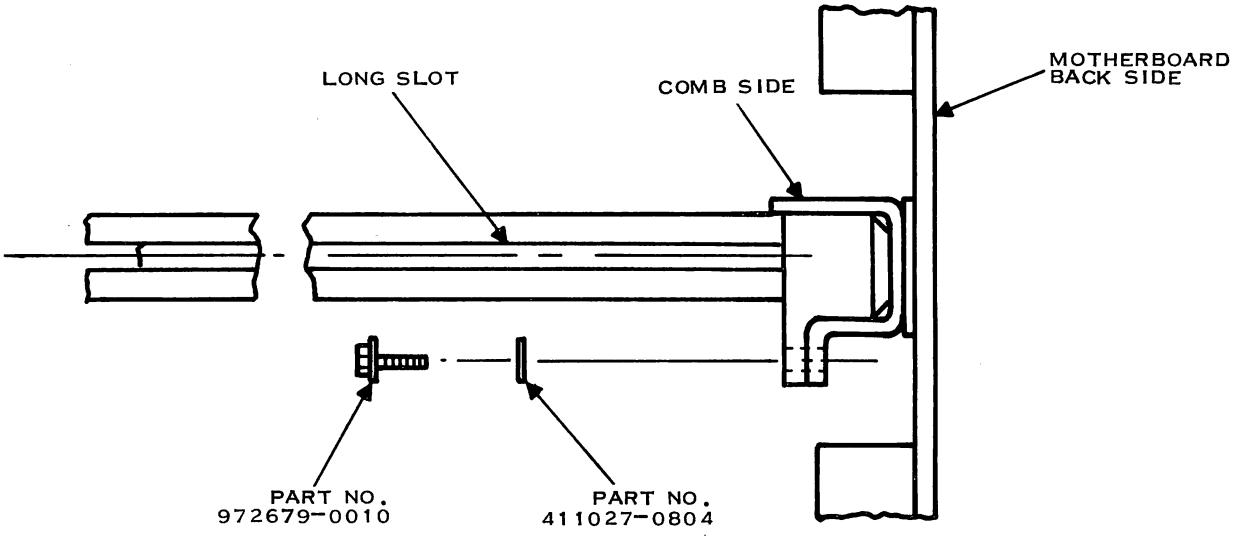


Figure 2-28. Center Card Guide Installation Diagram

2.11 COMMUNICATIONS PORT CONNECTIONS

Connectors for asynchronous communications ports 1 and 2 and asynchronous/synchronous communications port 3 are identical 25-pin RS-232 type subminiature connectors (see figure 2-29). Signals and pin numbers are identified in paragraph 5.4.

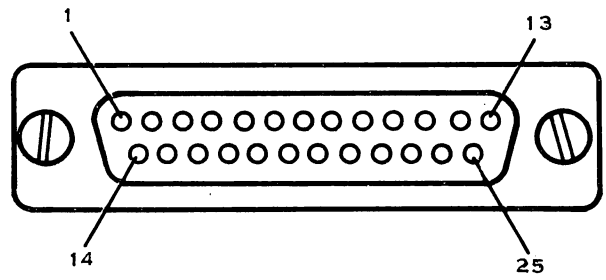


Figure 2-29. Contact Orientation for Ports 1, 2, and 3 (P4, P5, and P6)

2.12 SYSTEM CHECKOUT PROCEDURES

Prior to executing checkout procedures, check that the switches on the 990/5 board are set to the positions required for the particular site where the 990/5 system is being installed. The switch locations are shown in figure 2-30; table 2-7 briefly describes the switch functions.

System checkout procedures are normally performed in the following sequence:

1. 990/5 self-test to check general operation of board.
2. 990/5 diagnostic tests to check AU and RAM circuits.
3. Peripheral diagnostic tests to test other 990/5 System equipment.

Tests referenced in items 2 and 3 are outlined in the *Model 990 Computer Diagnostic Handbook*, part number 945400-9701.

2.12.1 MODEL 990/5 SELF-TEST. This test executes with either an operator front panel or programmer front panel (or MDU Test Set, part number 946710). However, if the 990/5 fails the self-test, the programmer panel (or MDU) will give more definitive results on the type of failure than the operator panel, which will only indicate FAULT.

When the operator panel is being used, setting the key-switch to LOAD initiates the self-test program. At the completion of a successful self-test, the POWER indicator is lighted and the FAULT indicator is OFF.

When a programmer panel (or MDU) is used, the 990/5 exercises a self-test when the key-switch is in the UNLOCK position and HALT then LOAD are pressed. Self-test is executed prior to any program loading from peripheral devices.

When a CPU error is detected during self-test, the processor halts with the FAULT indicator lighted and the RUN indicator extinguished. If a RAM error is detected during self-test, the FAULT, RUN, and IDLE indicators light. The address of the RAM at fault is also displayed on the programmer front panel.

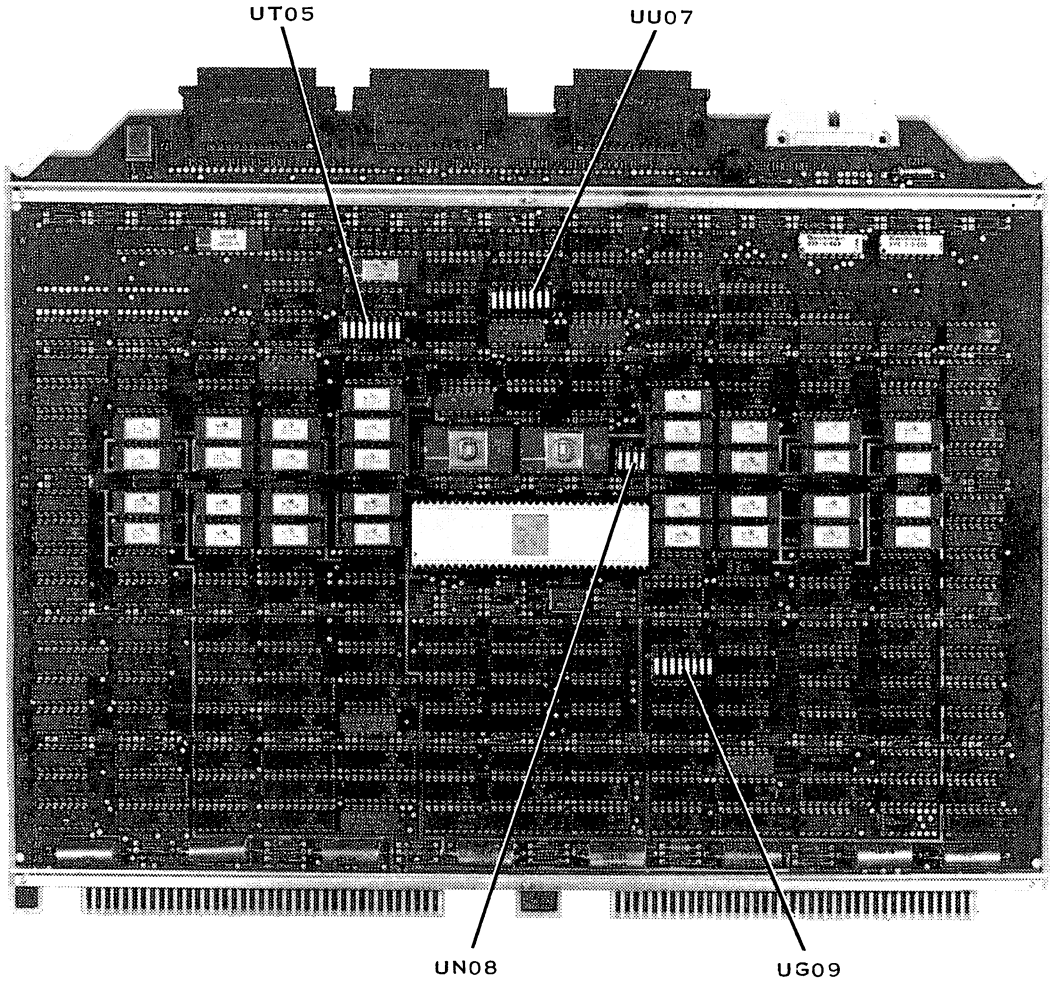


Figure 2-30. Option Switch Locations

Table 2-7. Location of Option Switches on the 990/5

Socket Position	Function with Switch in the "ON" Position	Normal Position
UG09-1	RESET causes power-up through load trap	ON
UG09-2	RESET causes power-up through reset trap	OFF
UG09-3	Real-time clock interrupt connects to interrupt level 15	OFF
UG09-4	Real-time clock interrupt connects to interrupt level 5	ON
UG09-5	Backpanel interrupt 5 connects to level 5	OFF
UG09-6	This unit functions as slave processor	OFF
UG09-7	32K Byte configuration	(32KB) -1 ON (64KB) -2 OFF
UG09-8	Disable ROM (for factory use only)	OFF
UN08-1	SPID0 MSB	ON for 0 OFF for 1
UN08-2	SPID1	
UN08-3	SPID2	
UN08-4	SPID3 LSB	
UT05-1	SASW0 MSB	ON for 0 OFF for 1
UT05-2	SASW1	
UT05-3	SASW2	
UT05-4	SASW3	
UT05-5	SASW4	
UT05-6	SASW5	
UT05-7	SASW6	
UT05-8	SASW7 (MSB)	

Slave Processor I.D.

TILINE Starting Address Switches

NOTE

ON represents a logic 0 TILINE address, i.e., the standard position; all switches ON represents 00000_{16}.

Table 2-7. Location of Option Switches on the 990/5 (Continued)

Socket Position	Function with Switch in the "ON" Position	Normal Position
UU07-1	Port 1 interrupt connected to interrupt level 8 (INT08)	ON
UU07-2	Port 2 interrupt connected to interrupt level 14 (INT14)	ON
UU07-3	Port 3 interrupt connected to interrupt level 6 (INT06)	ON
UU07-4	ID0 MSB	ON for 0 OFF for 1
UU07-5	ID1	
UU07-6	ID2	
UU07-7	ID3	
UU07-8	ID4 LSB	

Communication Station I.D. for TMS 9903 port

A failure at one of the communications ports causes the CRU base address of the failing port to flash five times on the programmer front panel indicators. This is followed by the FAULT, RUN, and IDLE indicators lighting. Troubleshooting Procedures and Corrective Maintenance/Fault Isolation Procedures are found in the *Model 990/5 Microcomputer Field Maintenance Manual*, part number 946295-9701.

2.12.2 MODEL 990/5 DIAGNOSTIC TESTS. After the successful completion of self-test, perform the AU05 and RAM05 tests outlined in the diagnostic handbook. To check out the 990/5, an input device for loading diagnostic software and an output device for messages are required. The input device may be a floppy disk, a disk cartridge, or a 733 ASR data terminal. The output device may be a 733 ASR, 743 KSR, or 820 KSR data terminal, an 810 printer, or a 911 VDT.

2.12.3 PERIPHERAL DIAGNOSTIC TESTS. After successfully completing the AU05 and RAM05 diagnostics, perform the appropriate peripheral diagnostics outlined in the diagnostic handbook.

NOTE

Peripheral field maintenance handbooks are listed in the preface to this user's manual.

SECTION III

OPERATION

3.1 GENERAL

This section describes controls and indicators for 990/5 front panels, general operating procedures for the front panel, and loading procedures.

3.2 990/5 MICROCOMPUTER FRONT PANELS

Two type of front panels are available for the 990/5 computer: programmer front panel or operator front panel. The programmer panel allows manual entry and modification of programs, as well as manual entry of data into selected registers. The operator panel has a LOAD switch position, to activate a loader program, and indicators for POWER and FAULT states.

3.2.1 PROGRAMMER FRONT PANEL

The programmer panel controls and indicators are shown in figure 3-1 and listed and described in table 3-1. Basically, the panel functions in one of two modes, run or halt.

When power is initially applied to the computer, the system comes up in the run mode, which locks out the programmer controls. In this mode of operation, the RUN LED and all DATA DISPLAY LEDs on the panel light and remain lit.

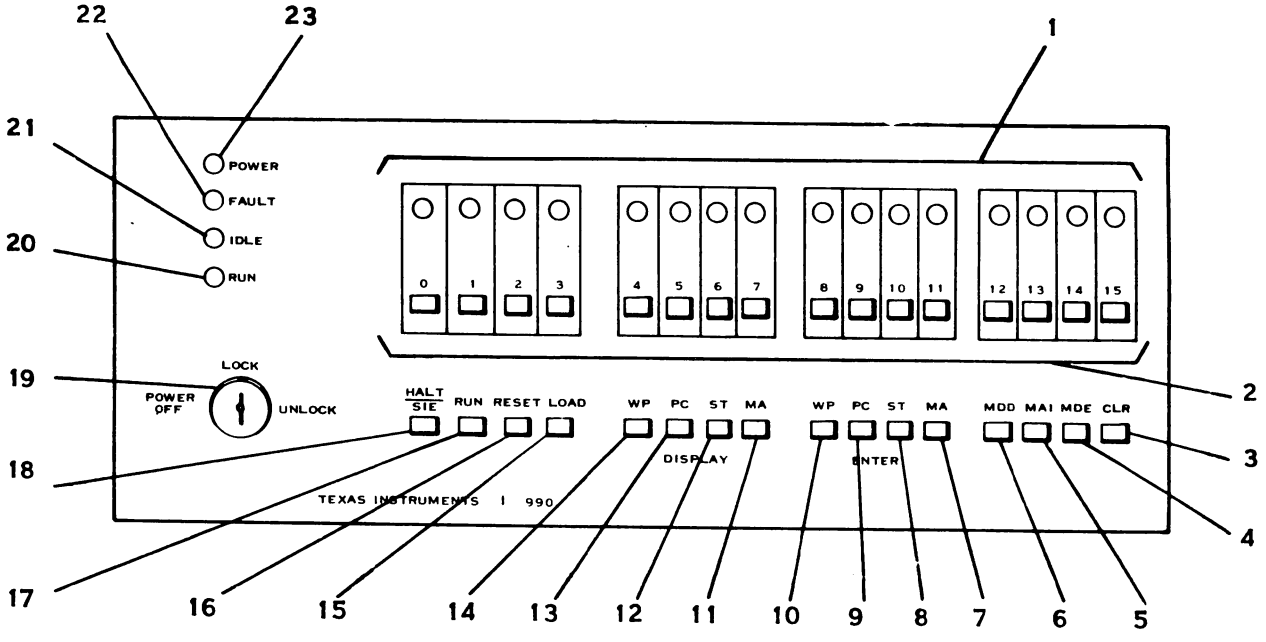


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Figure 3-1. 990 Programmer Panel, Controls, and Indicators

Table 3-1. Programmer Panel,Controls and Indicators

Reference Number	Control or Indicator	Function
1	DATA LEDs	In the run mode of operation, all DATA LEDs light except when the computer halts. At this point, the contents of the CPUs program counter is displayed. A lighted LED denotes logic 1, an extinguished indicator denotes logic 0. The LSB is displayed on the far right of the LEDs. In the halt mode, the LEDs display a computer register contents, memory contents, or a value entered into computer memory via the data entry switches, depending on which switches are pressed (see references 5, 7, 9, 11, 13, 15).
2	DATA entry switches	Used in conjunction with the ENTRY switches on the panel, these switches enter data and addresses into selected computer registers and memory locations (active only when the panel is in the halt mode of operation). In the halt mode, the data LED located immediately above each data entry switch lights as each switch is pressed. The value indicated by the DATA LEDs is then stored in the register or memory address selected by the entry switches.
3	CLR switch	When pressed, this switch clears the DATA LED displays
4	MDE switch	This switch is pressed to transfer a value displayed on the DATA LEDs to the memory location defined by the contents of the memory address (MA) register in the computer.
5	MAI switch	The memory address increment (MAI) switch is pressed to increment the value stored in the CPU's memory address register by a value of 2.
6	MDD switch	When pressed, this switch causes the contents of the memory location defined by the contents of the memory address register to be displayed on the DATA DISPLAY LEDs.
7	ENTER MA switch	When pressed, this switch causes the value displayed by the DATA LEDs to be entered into the computer's memory address register.
8	ENTER ST switch	When pressed, the value displayed on the DATA LEDs is entered into the computer's status register.
9	ENTER PC switch	When pressed, the value displayed on the DATA LEDs is loaded into the computer's program counter.
10	ENTER WP switch	When pressed, the value displayed on the DATA LEDs is loaded into the computer's workspace pointer register.
11	DISPLAY MA switch	When pressed, the value stored in the computer's memory address register is displayed on the DATA LEDs.
12	DISPLAY ST switch	When pressed, the contents of the computer's status register is displayed on the DATA LEDs.

Table 3-1. Programmer Panel Controls and Indicators (Continued)

Reference Number	Control or Indicator	Function
13	DISPLAY PC switch	When pressed, the contents of the computer's program counter is displayed on the DATA LEDs.
14	DISPLAY WP switch	When pressed, the contents of the computer's workspace pointer register is displayed on the DATA LEDs.
15	LOAD switch	When the panel is in the halt mode, pressing this switch causes the computer to trap to the ROM loader starting address.
16	RESET switch	Pressing the RST switch results in an IORESET – pulse being generated, which resets all units in the system.
17	RUN switch	When the computer is halted (programmer panel is active), pressing the RUN switch returns the computer to the run mode of operation and deactivates the panel.
18	HALT/SIE switch	When the computer is in the run mode (RUN LED is lighted), pressing the HALT/SIE switch causes the computer to halt and begin processing the programmer-panel software if the key switch is set to the UNLOCK position. Pressing the switch when the computer is not in the run mode causes the computer to execute a single instruction at the present PC (program counter) address. The contents of the program counter are incremented by two and displayed on the DATA LEDs.
19	Key switch	The key switch (OFF/LOCK/UNLOCK) prevents unauthorized computer turnon or program intervention. In order to apply ac power to the chassis, the key must be inserted into the switch and the switch set to the LOCK position. At this point, power is applied to the computer, but the programmer panel is locked out. In the UNLOCK position, the computer may be halted by pressing the HALT/SIE switch. The key may be removed from the switch in either the OFF or LOCK position.
20	RUN LED	The RUN LED lights when a low-active RUN– signal is generated by the computer indicating the computer is in the run mode. When this LED is lighted, all switches on the panel except the HALT/SIE switch are disabled and the DATA LEDs are driven under program control. When the RUN LED is extinguished, the panel controls are active.
21	IDLE LED	The IDLE LED lights when the computer is executing an idle instruction (indication of computer inactivity for most interrupt-driven software).
22	FAULT LED	The FAULT LED lights when the computer has detected a diagnostic test failure.
23	POWER LED	The POWER LED lights when power is applied to the unit (key switch on the panel set to the LOCK or UNLOCK position).

In order to set the programmer panel to the halt mode, the key must be inserted in the key switch and the switch rotated to the UNLOCK position. At this time, pressing the HALT/SIE switch halts the computer and activates the controls on the programmer panel. The panel may be returned to the run mode by pressing the RUN switch.

3.2.2 OPERATOR FRONT PANEL

The operator panel controls and indicators are shown in figure 3-2 and described in table 3-2.

TABLE 3-2 REFERENCE NJMBER

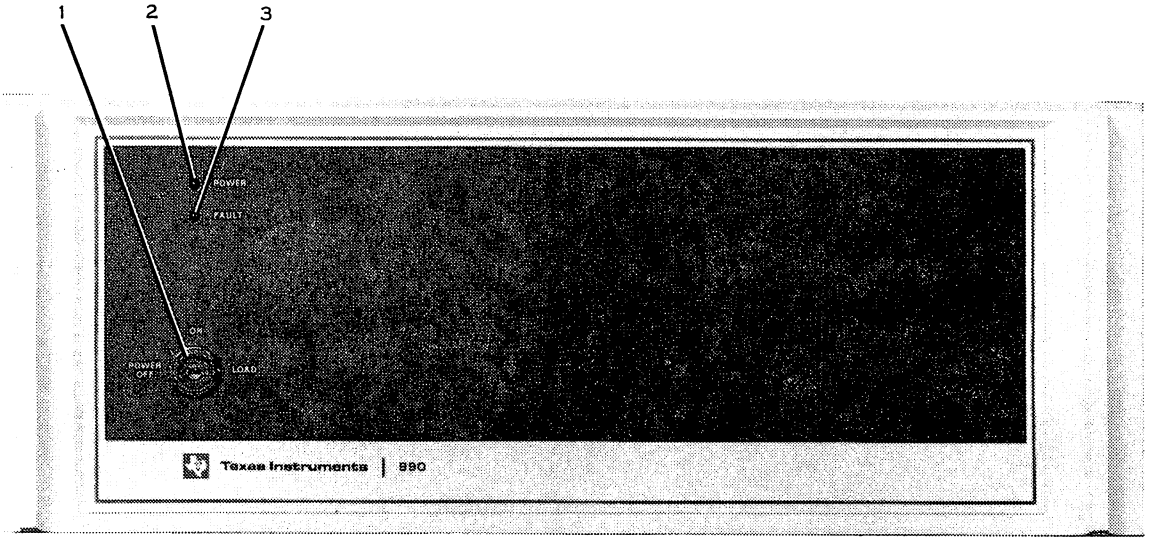

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Figure 3-2. 990 Operator Panel, Control, and Indicators

Table 3-2. Operator Panel, Control and Indicators

Reference Number	Control or Indicator	Function
1	Key Switch	The key switch (OFF/ON/LOAD) prevents unauthorized computer turnon or program intervention. To apply power, the key is inserted and turned to the ON position. The key may then be removed to prevent intervention. To activate loader programs momentarily turn the key to the LOAD position. The spring-loaded switch then returns the key to ON.
2	POWER L.E.D	POWER lights when power is applied to the unit and key switch is not in the OFF position.
3	FAULT L.E.D	FAULT lights when the computer has detected a diagnostic test failure (990/5 self-test).

3.3 GENERAL OPERATING PROCEDURES

The following information is provided as an aid to operators for using the programmer panel in checking various functions of the computer and its software.

To abbreviate these procedures and to allow information to be in tabular format, the following conventions are established:

Current. Current refers to the state of registers at the time the HALT switch is pressed.

Change Data. To change the contents of a register; address the particular register by depressing MA (or MAI) at the appropriate step in the procedure. When current register data is displayed, clear register by pressing CLR and then select new register data with data switches. Finally, press MDE to enter new data into the selected register.

Display/Enter Switches. There are two sets of similar switches: WP, PC, ST, and MA. These switches are differentiated in the following procedures by the notations (ENTER) or (DISPLAY). These notations correspond to the switch functions and the front-panel marking.

Select Data. Data to be entered is set up on data switches 0 through 15 after clearing register with CLR pushbutton switch. (Data is represented in hexadecimal notation.)

Encircled Numbers. These numbers identify controls/indicators on the programmer panel and are keyed to figure 3-1. (Numbers are not repeated in the same procedure.)

3.3.1 WORKSPACE REGISTER DISPLAY. The contents of a workspace register may be displayed by performing the following procedures.

Press		Display
HALT	(18)	Current PC (Program Counter)
WP (DISPLAY)	(14)	Current WP (Workspace Pointer)
MA (ENTER)	(7)	–No change from above –

Press		Display
MDD	(6)	Contents of WP Register 0
MAI	(5)	Address of next register is selected (not displayed)
MDD		Contents of WP Register 1
MAI		Address of next register is selected (not displayed)
MDD		Contents of WP Register 2
.		.
.		.
.		.
MDD		Contents of WP Register 14
MAI		Address of next register is selected (not displayed)
MDD		Contents of WP Register 15

To return to program at the location where HALT was pressed, press RUN (17).

CAUTION

Altering the contents of the WP, PC, or ST registers (by pressing the (ENTER) WP, PC, or ST pushbuttons) alters the return context when RUN is pressed. Care must be taken to ensure that modified WP and PC values create a valid context, i.e., that the instruction pointed to by the PC register does in fact use the workspace identified by the contents of the WP register.

To change contents of a workspace register:

1. Select desired register by entering MA or MAI information.
2. Display contents of selected register (determined in step 1) by pressing MDD.
3. Press CLR pushbutton. This clears the contents of the register to be modified.
4. Enter new data on data switches 0 through 15.
5. Press MDE to enter new value in workspace register.
6. Press RUN to execute program with modified workspace register.

3.3.2 CURRENT INSTRUCTION DISPLAY. To display the current instruction being executed in memory, perform the following:

Press		Display
HALT	(18)	Current PC
MA (ENTER)	(7)	–No change from above.–
MDD	(6)	Instruction being executed.

To display the next word in memory, perform the following:

Press		Display
MAI	(5)	Changes address of current instruction to address of next word in memory (not necessarily the next instruction).
MDD		Displays contents of above address.

If the contents of a location other than the next location in sequence is to be displayed, perform the following assuming the computer is in the HALT mode.

Press		Display
CLR	(3)	All zeros
Data switches corresponding to desired address in hexadecimal	(1)	
MA (ENTER)		Address as selected above.
MDD		Word at location addressed.

To modify contents, enter desired data in hexadecimal via data switches 0 through 15, and press MDE (4).

3.3.3 MASKING INTERRUPTS. To mask interrupts for execution of single instructions (SIE), perform the following:

Press		Display
HALT	(18)	Current PC.
ST (DISPLAY)	(12)	If right four data lights do not display F_{16}, note the status of lamps. Data lights 12 through 15 display states of interrupt masks.
Set right four data lamps to off (zeros).	(1)	
ST (ENTER)	(8)	Interrupts are now masked.

With interrupts masked, it is now possible to execute single instructions (SIE). To return to normal program routine, enable interrupts (logic 1, or data lamps 12 through 15 lighted) as noted above if status was other than F_{16}.

3.4 PROGRAM LOADING PROCEDURES WITH ROM LOADER

The method of loading programs depends on the type of front panel in use with the 990/5 microcomputer. With an operators panel, loading is automatic and requires only that the keyswitch be turned to ON (or LOAD on some chassis). When using the programmer panel, additional data/address/control information may be entered before program loading.

If an error is encountered during a load operation, the fault light on the front panel will flash. In addition to the fault light flashing, the programmer panel will also display status on the data indicators. Error status will be explained in paragraphs 3.4.3 and 3.4.4.

3.4.1 LOAD PROCEDURES USING OPERATOR PANEL. Loading with an operator panel is automatic. No manual interaction to alter load program is possible. The load sequence is started when power to the 990/5 is turned ON (on some chassis the keyswitch must be momentarily set to LOAD).

The ROM loader program first checks to see if a TILINE disk controller is at address $F800_{16}$. If a controller is at $F800_{16}$, the program then checks for units that are online (ready) and not write protected, starting with unit 0 connected to the controller. When a unit is found to be online and not write protected, the loader program then loads the program from the TILINE disk. If the load is unsuccessful, the FAULT light on the operators panel will flash.

If no TILINE controller is at $F800_{16}$ or no TILINE disk units are online, the loader attempts to load from a floppy disk unit at CRU address 0080_{16}. When a floppy disk controller is at CRU address 0080_{16}, each floppy disk unit connected to the controller is tested for online status starting with unit 0. As soon as a unit is found to be online, a load is attempted. If the load is unsuccessful, the FAULT light on the operator panel flashes.

If no CRU floppy disks are online, the load program loops back to the TILINE (address $F800_{16}$) to check for TILINE disks. This cycle repeats indefinitely as long as no units are online and power is on.

3.4.2 LOAD PROCEDURES USING PROGRAMMER PANEL. There are two methods of loading programs using the programmer panel: by default or by entering explicit data on the front panel.

3.4.2.1 Default Loading. The simplest method for program loading using the programmer panel is a default load. This procedure is similar to loading with an operator panel. However, it is recommended that only one load device be online and connected to a controller either at TILINE address $F800_{16}$ (TILINE disk) or at CRU address 0080_{16}. When this requirement has been met, it is only necessary to press HALT then LOAD on the programmer panel to initiate loading procedures. If the load fails, the fault light flashes and status is displayed on data lights. See paragraphs 3.4.3 and 3.4.4 for fault indications.

3.4.2.2 Explicit Loading. In performing explicit load operations, four different device types may be specified:

1. CRU floppy disk, only. (Load will not be performed from a TILINE device.)
2. Cassette recorder (CRU device)
3. TILINE disk unit
4. Magnetic tape unit (TILINE device).

The following are brief descriptions of load procedures for each of the devices listed above.

- To load from a CRU disk the user may use the default load sequence described in 3.4.2.1 provided all other disk units at $F800_{16}$ (TILINE) and all other CRU disk units at CRU address 0080_{16} are offline. If the user does not wish to force TILINE units at $F800_{16}$ to be offline at load time, the user may enter a positive number into location 0080_{16}. This will force the loader to attempt to load only from the CRU disks at CRU address 0080_{16}. If the user wishes to load from a CRU disk at a different CRU address, the new address must be entered into memory location 0082_{16} via the front panel.

- To load from cassette the user must clear location 0080_{16}. This instructs the loader to load from cassette at location 1700_{16} (Comm interface port 1, 9902). If the user wishes to load from a different CRU address (different port), he must enter the address in memory location 0082_{16}.

- To load from disk when the disk controller is at TILINE address F800, the user may load from disk using the default procedure described in 3.4.2.1, providing that the loading device is the only unit online including CRU floppy disk at address 0080_{16}. The user may load from a controller at another TILINE address by entering the new TILINE address into memory location 0082_{16} via the front panel. The ROM loader in the 990/5 will try to load at the first unit (unit 0) connected to the disk controller, and will try each unit until one is found to be online (ready) and not write protected. The user may instruct the ROM loader to begin at a different unit by entering the unit numbers shown below into memory location 0084_{16}.

  Unit 0: 0800_{16}
  Unit 1: 0400_{16}
  Unit 2: 0200_{16}
  Unit 3: 0100_{16}

- To load from magnetic tape, the user must enter the TILINE address of the magnetic tape controller into memory location 0082_{16} and the unit number (listed below) into memory location 0084_{16}.

  Unit 0: 8000_{16}
  Unit 1: 4000_{16}
  Unit 2: 2000_{16}
  Unit 3: 1000_{16}

The following step-by-step procedures show how to handle each of four different loading situations.

Detailed Procedures to Load from CRU Floppy Disk.

CRU Floppy at 0080_{16}			CRU Floppy at Different Address		
Press	HALT	(18)			
Press	CLR	(3)			
Select	0080_{16}	(1)			
Press	MA (ENTER)	(7)			
Press	MDE	(4)			
* Press	LOAD	(15)			
			Press	MAI	(5)
			Press	CLR	
			Select	(Desired CRU address, hex)	
			Press	MDE	
			Press	LOAD	

Detailed Procedures to Load from CRU cassette recorder.

CRU Cassette at 1700_{16} Comm Port 1			CRU Cassette at 1740_{16} Comm Port 2			CRU Cassette at 1780_{16} Comm Port 3	
Press	HALT	(18)					
Press	CLR	(3)					
Select	0080_{16}	(1)					
Press	MA (ENTER)	(7)					
Press	CLR						
Press	MDE	(4)					
* Press	LOAD	(15)					
			Press	MAI	(5)	Press	MAI
			Press	CLR		Press	CLR
			Select	1740_{16}		Select	1780_{16}
			Press	MDE		Press	MDE
			Press	LOAD		Press	LOAD

Detailed Procedures to Load from TILINE Disk at Address Other than $F800_{16}$.

TILINE Disk at Different Address

Press	HALT	(18)
Press	CLR	(3)
Select	0082_{16}	(1)
Press	MA (ENTER)	(7)
Select	(Desired TILINE address, hex)	(1)
Press	MDE	(4)
Press	LOAD	(15)

Detailed Procedures to Load from TILINE Magnetic Tape.

TILINE Magnetic Tape, Unit 0

Press	HALT	(18)
Press	CLR	(3)
Select	0082_{16}	(1)
Press	MA (ENTER)	(7)
Press	CLR	
Select	$F880_{16}$	(In some cases address may be $F890_{16}$)
Press	MDE	(4)
Press	MAI	(5)
Press	CLR	
Select	8000_{16}	(Unit 0; Unit 1 = 4000_{16}; Unit 2 = 2000_{16}; Unit 3 = 1000_{16})
Press	MDE	
Press	LOAD	(15)

3.4.3 FAULT INDICATIONS IN LOADING. Errors encountered during the loading phase will be indicated by a flashing FAULT indicator on the operator or programmer panels. Additionally, the RUN indicator on the programmer panel will be on and status will be displayed on data indicators 0 through 15 for the following conditions:

- If any bits for TILINE loads are set in bit positions 0 through 6, then the unit status is being displayed. If no bits are set in bit positions 0 through 6, the displayed status is for the controller.
- If a status of $F001_{16}$ is displayed, when the load is being forced from floppy disk and no floppy disk is online at the CRU address (0080_{16}) specified.
- For cassette and mag tape loads, an error of $C001_{16}$ means that an illegal character was read in the object code. An error of $C002_{16}$ means that a checksum error was found.

3.4.4 FAULT INDICATIONS IN SELF-TEST MODE. The following indications will be displayed if a failure occurs during self-test:

Type Failure	Indications
AU Failure	The FAULT indicator lights.
Memory Failure	Board address is displayed and the IDLE indicator lamp lights.
Comm. Port Fail.	The CRU base address is flashed on data/address indicators (1700, 1740 or 1780) five times. The FAULT indicator lights and the processor stops.

SECTION IV

PROGRAMMING CONSIDERATIONS

4.1 GENERAL

Information concerning programming considerations for the 990/5 covers the TMS 9900 microprocessor instruction set, communications ports address bit assignments, and asynchronous clock rate selection (comm. port 3). More detailed programming information may be found in the manuals listed in the preface, particularly in the device data manuals/sheets.

The use of standard TI software packages imposes the following considerations: standard TI operating systems furnish an executable OS, linkable modules, and utility programs for linking the modules and assigning interrupt, CRU, and TILINE addresses. The use of the executable OS requires that the storage media and operator's console be at preassigned interrupt, CRU, and TILINE addresses. See figures 2-9 and 2-16 for these preassignments.

The utility programs can assemble an executable OS from the linkable modules with any desired interrupt, CRU, and TILINE address assignments. The use of these utilities requires a working system, either the executable OS or a previously assembled custom OS.

In considering whether to use the standard I/O assignments referenced above or to define special assignments, the user should bear in mind that the software subscription service included with most TI standard software packages may deliver a new package, the use of which imposes the same requirements as the initial software package.

4.2 TMS 9900 MICROPROCESSOR

The TMS 9900 microprocessor is a single-chip, 16-bit central processing unit (CPU). The instruction set of the TMS 9900 includes the capabilities offered by larger minicomputer systems.

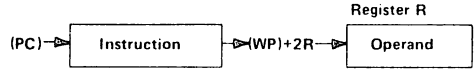
4.3 TMS 9900 INSTRUCTION SET

4.3.1 DEFINITION. Each TMS 9900 instruction performs one of the following operations:

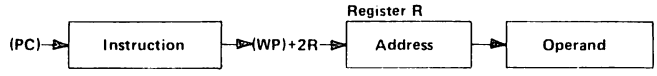
- Arithmetic, logical, comparison, or manipulation operations on data
- Loading or storage of internal registers (program counter, workspace pointer, or status)
- Data transfer between memory and external devices via the CRU
- Control functions.

4.3.2 ADDRESSING MODES. TMS 9900 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags) or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described in paragraph 4.3.5 along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes (R, *R, *R+, @LABEL, or @TABLE(R)) are the general forms used by TMS 9900 assemblers to select the addressing mode for register R.

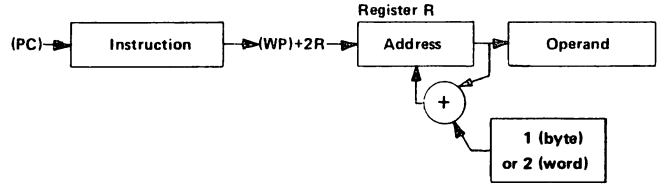
4.3.2.1 Workspace Register Addressing R. Workspace Register R contains the operand.



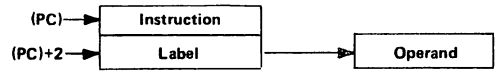
4.3.2.2 Workspace Register Indirect Addressing *R. Workspace Register R contains the address of the operand.



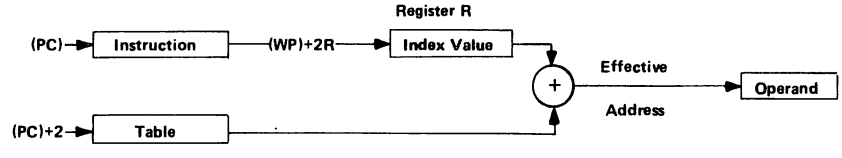
4.3.2.3 Workspace Register Indirect Auto Increment Addressing *R+. Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace register R are incremented.



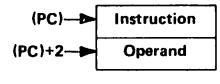
4.3.2.4 Symbolic (Direct) Addressing @Label. The word following the instruction contains the address of the operand.



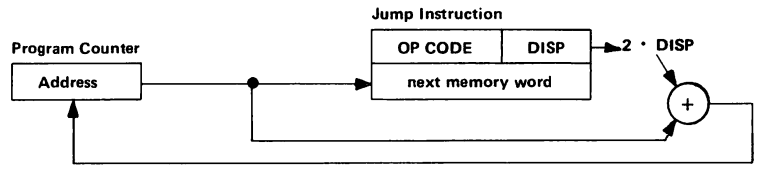
4.3.2.5 Indexed Addressing @TABLE (R). The word following the instruction contains the base address. Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



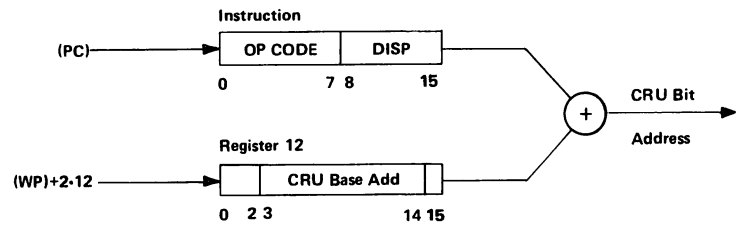
4.3.2.6 Immediate Addressing. The word following the instruction contains the operand.



4.3.2.7 Program Counter Relative Addressing. The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



4.3.2.8 CRU Relative Addressing. The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace register 12). The result is the CRU address of the selected CRU bit.

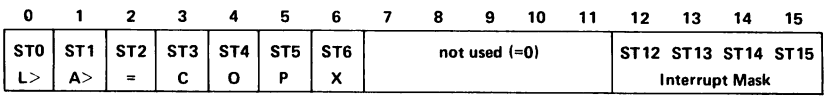


4.3.3 TERMS AND DEFINITIONS. The following terms are used in describing the instructions of the TMS 9900:

Term	Definition
B	Byte indicator (1=byte, 0=word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
W	Workspace register
WRn	Workspace register n
(n)	Contents of n
a → b	a is transferred to b

Term	Definition
|n|	Absolute value of n
+	Arithmetic addition
-	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
$\oplus$	Logical exclusive OR
$\overline{n}$	Logical complement of n

4.3.4 STATUS REGISTER. The status register contains the interrupt mask level and information pertaining to the instruction operation.



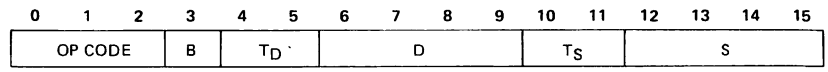
Bit	Name	Instruction	Condition to set bit to 1
ST0	LOGICAL GREATER THAN	C, CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 1 and MSB of IOP = 0, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If (SA) $\neq$ 0
		All others	If result $\neq$ 0
ST1	ARITHMETIC GREATER THAN	C, CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 0 and MSB of IOP = 1, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If MSB(SA) = 0 and (SA) $\neq$ 0
		All others	If MSB of result = 0 and result $\neq$ 0
ST2	EQUAL	C, CB	If (SA) = (DA)
		CI	If (W) = IOP
		COC	If (SA) and $(\overline{DA})$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG, S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result $\neq$ MSB(DA)
		AI	If MSB(W) = MSB of IOP and MSB of result $\neq$ MSB(W)
		S, SB	If MSB(SA) $\neq$ MSB(DA) and MSB of result $\neq$ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 0
		ABS, NEG	If (SA) = 8000_{16}

Bit	Name	Instruction	Condition to set bit to 1
ST5	PARITY	CB, MOVB	If (SA) has odd number of 1's
		LDCR, STCR	If $1 \leq C \leq 8$ and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12–ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

4.3.5 INSTRUCTIONS.

4.3.5.1 Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand.

General format:



If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

The addressing mode for each operand is determined by the T field of that operand.

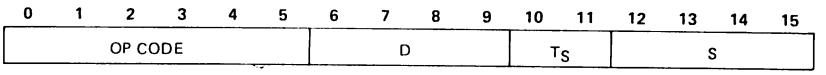
T_S OR T_D	S OR D	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

NOTES: 1. When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).
4. When $T_S = T_D = 10$, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.

Mnemonic	Op Code 0	1	2	B 3	Meaning	Result Compared To 0	Status Bits Affected	Description
A	1	0	1	0	Add	Yes	0-4	(SA)+(DA) → (DA)
AB	1	0	1	1	Add bytes	Yes	0-5	(SA)+(DA) → (DA)
C	1	0	0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1	0	0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0	1	1	0	Subtract	Yes	0-4	(DA) – (SA) → (DA)
SB	0	1	1	1	Subtract bytes	Yes	0-5	(DA) – (SA) → (DA)
SOC	1	1	1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA) → (DA)
SOCB	1	1	1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA) → (DA)
SZC	0	1	0	0	Set zeroes corresponding	Yes	0-2	(DA) AND ($\overline{SA}$) → (DA)
SZCB	0	1	0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND ($\overline{SA}$) → (DA)
MOV	1	1	0	0	Move	Yes	0-2	(SA) → (DA)
MOVB	1	1	0	1	Move bytes	Yes	0-2,5	(SA) → (DA)

4.3.5.2 Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination.

General format:



The addressing mode for the source operand is determined by the T_S field.

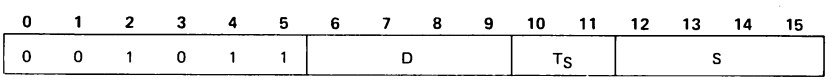
T_S	S	Addressing Mode	Notes
00	0, 1,. . . .15	Workspace register	
01	0, 1,. . . .15	Workspace register indirect	
10	0	Symbolic	
10	1, 2,. . . .15	Indexed	1
11	0, 1,. . . .15	Workspace register indirect auto increment	2

NOTES: 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

Mnemonic	Op Code 0 1 2 3 4 5	Meaning	Result Compared To 0	Status Bits Affected	Description
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D)⊕(SA) → (D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D + 1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient → (D), remainder → (D+1). If D = 15, the next word in memory after WR15 will be used for the remainder.

4.3.5.3 Extended Operation (XOP) Instruction.

General format:



The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow (WP)$

$(42_{16} + 4D) \rightarrow (PC)$

SA→(new WR11)

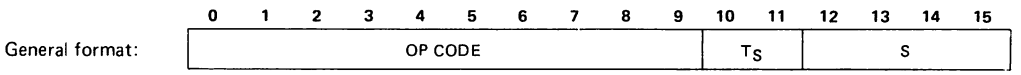
(old WP)→(new WR13)

(old PC)→(new WR14)

(old ST)→(new WR15)

The TMS 9900 does not test interrupt requests ($\overline{INTREQ}$) upon completion of the XOP instruction.

4.3.5.4 Single Operand Instructions.



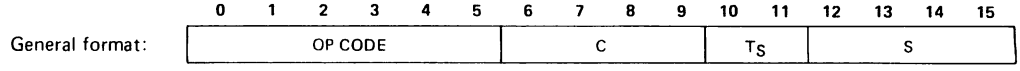
The T_S and S fields provide multiple mode addressing capability for the source operand.

Mnemonic	Op Code 0 1 2 3 4 5 6 7 8 9	Meaning	Result Compared To 0	Status Bits Affected	Description
B	0 0 0 0 0 1 0 0 0 1	Branch	No	–	SA → (PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	–	(PC) → (WR11); SA → (PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	–	(SA) → (WP);(SA+2) → (PC); (old WP) → (new WR13); (old PC) → (new WR14); (old ST) → (new WR15); the interrupt input ($\overline{INTREQ}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	–	0 → (SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	–	$FFFF_{16}$ → (SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	($\overline{SA}$) → (SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	–(SA) → (SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	|(SA)| → (SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	–	(SA), bits 0 through 7 → (SA), bits 8 through 15; (SA), bits 8 through 15 → (SA), bits 0 through 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA) + 1 → (SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA) + 2 → (SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA) - 1 → (SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA) - 2 → (SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	–	Execute the instruction at SA.

*Operand is compared to zero for status bit.

†If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the TMS 9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

4.3.5.5 CRU Multiple-Bit Instructions.

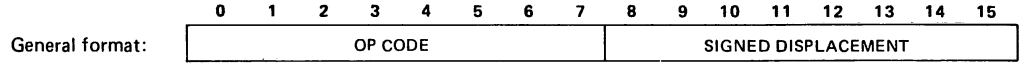


The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 3 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in the workspace register indirect auto-increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

Mnemonic	Op Code 0 1 2 3 4 5	Meaning	Result Compared To 0	Status Bits Affected	Description
LDCR	0 0 1 1 0 0	Load communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if $1 \leqslant C \leqslant 8$.

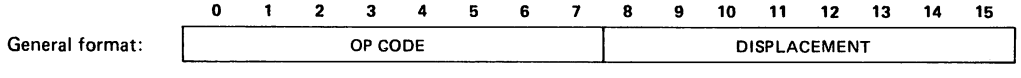
4.3.5.6 CRU Single-Bit Instructions.



CRU relative addressing is used to address the selected CRU bit.

Mnemonic	Op Code 0 1 2 3 4 5 6 7	Meaning	Status Bits Affected	Description
SBO	0 0 0 1 1 1 0 1	Set bit to one	–	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	–	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit = 1, set ST2.

4.3.5.7 Jump Instructions.

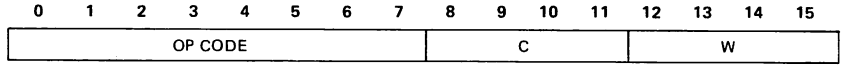


Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of —128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instruction.

Mnemonic	Op Code 0	1	2	3	4	5	6	7	Meaning	ST Condition to Load PC
JEQ	0	0	0	1	0	0	1	1	Jump equal	ST2 = 1
JGT	0	0	0	1	0	1	0	1	Jump greater than	ST1 = 1
JH	0	0	0	1	1	0	1	1	Jump high	ST0 = 1 and ST2 = 0
JHE	0	0	0	1	0	1	0	0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0	0	0	1	1	0	1	0	Jump low	ST0 = 0 and ST2 = 0
JLE	0	0	0	1	0	0	1	0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0	0	0	1	0	0	0	1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0	0	0	1	0	0	0	0	Jump unconditional	unconditional
JNC	0	0	0	1	0	1	1	1	Jump no carry	ST3 = 0
JNE	0	0	0	1	0	1	1	0	Jump not equal	ST2 = 0
JNO	0	0	0	1	1	0	0	1	Jump no overflow	ST4 = 0
JOC	0	0	0	1	1	0	0	0	Jump on carry	ST3 = 1
JOP	0	0	0	1	1	1	0	0	Jump odd parity	ST5 = 1

4.3.5.8 Shift Instructions.

General format:

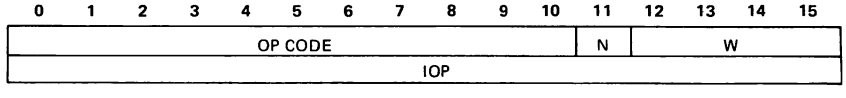


If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

Mnemonic	Op Code 0	1	2	3	4	5	6	7	Meaning	Result Compared To 0	Status Bits Affected	Description
SLA	0	0	0	0	1	0	1	0	Shift left arithmetic	Yes	0-4	Shift (W) left. Fill vacated bit positions with 0.
SRA	0	0	0	0	1	0	0	0	Shift right arithmetic	Yes	0-3	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	0	0	0	0	1	0	1	1	Shift right circular	Yes	0-3	Shift (W) right. Shift previous LSB into MSB.
SRL	0	0	0	0	1	0	0	1	Shift right logical	Yes	0-3	Shift (W) right. Fill vacated bit positions with 0's.

4.3.5.9 Immediate Register Instructions.

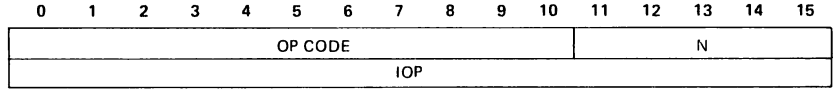
General format:



Mnemonic	Op Code 0 1 2 3 4 5 6 7 8 9 10	Meaning	Result Compared To 0	Status Bits Affected	Description
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(W) + IOP → (W)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(W) AND IOP → (W)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP → (W)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(W) OR IOP → (W)

4.3.5.10 Internal Register Load Immediate Instructions.

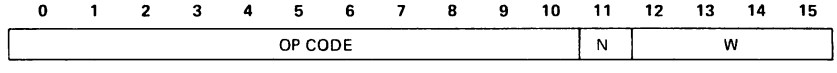
General format:



Mnemonic	Op Code 0 1 2 3 4 5 6 7 8 9 10	Meaning	Description
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP → (WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 through 15 → ST12 through ST15

4.3.5.11 Internal Register Store Instructions.

General format:

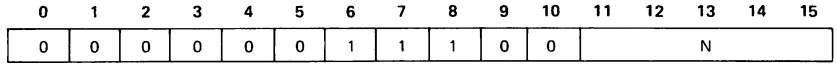


No ST bits are affected.

Mnemonic	Op Code 0 1 2 3 4 5 6 7 8 9 10	Meaning	Description
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST) → (W)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP) → (W)

4.3.5.12 Return Workspace Pointer (RTWP) Instruction.

General format:



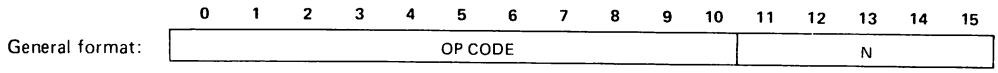
The RTWP instruction causes the following transfers to occur:

(WR15)→(ST)

(WR14)→(PC)

(WR13)→(WP)

4.3.5.13 External Instructions.



External instructions cause the three most-significant address lines (A0 through A2) to be set to the below-described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

Mnemonic	Op Code 0	1	2	3	4	5	6	7	8	9	10	Meaning	Status Bits Affected	Description	Address Bus A0	A1	A2
IDLE	0	0	0	0	0	0	1	1	0	1	0	Idle	–	Suspend TMS 9900 instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L	H	L
RSET	0	0	0	0	0	0	1	1	0	1	1	Reset	12-15	0 → ST12 through ST15	L	H	H
CKOF	0	0	0	0	0	0	1	1	1	1	0	User defined		– – –	H	H	L
CKON	0	0	0	0	0	0	1	1	1	0	1	User defined		– – –	H	L	H
LREX	0	0	0	0	0	0	1	1	1	1	1	User defined		– – –	H	H	H

4.3.6 TMS 9900 INSTRUCTION EXECUTION TIMES. Instruction execution times for the TMS 9900 are a function of:

1) Clock cycle time ($t_c(\phi)$)

2) Addressing mode used where operands have multiple addressing mode capability

3) Number of wait states required per memory access.

Table 4-1 lists the number of clock cycles and memory accesses required to execute each TMS 9900 instruction. Table 4-1 is divided into three parts. The A and B in the Address Modification column refer to Part A and Part B of the table. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$$T = t_c(\phi) \quad (C + W \times M)$$

where:

T = total instruction execution time;

$t_c(\phi)$ = clock cycle time;

C = number of clock cycles for instruction execution plus address modification;

W = number of required wait states per memory access for instruction execution plus address modification;

M = number of memory accesses.

Table 4-1. Instruction Execution Times

Instruction	Clock Cycles C	Memory Access M	Address Modification† Source	Address Modification† Dest.	Execution Time in μsecs.
A	14	4	A	A	3.5
AB	14	4	B	B	3.5
ABS (MSB = 0)	12	2	A	–	3.0
(MSB = 1)	14	3	A	–	3.5
AI	14	4	–	–	3.5
ANDI	14	4	–	–	3.5
B	8	2	A	–	2.0
BL	12	3	A	–	3.0
BLWP	26	6	A	–	6.5
C	14	3	A	A	3.5
CB	14	3	B	B	3.5
CI	14	3	–	–	3.5
CKOF	12	1	–	–	3.0
CKON	12	1	–	–	3.0
CLR	10	3	A	–	2.5
COC	14	3	A	–	3.5
CZC	14	3	A	–	3.5
DEC	10	3	A	–	2.5
DECT	10	3	A	–	2.5
DIV (ST4 is reset)	16	3	A	–	4.0
DIV (ST4 is reset)*	92-124	6	A	–	23-31
IDLE	12	1	–	–	3.0
INC	10	3	A	–	2.5
INCT	10	3	A	–	2.5
INV	10	3	A	–	2.5
Jump (PC is changed)	10	1	–	–	2.5
(PC is not changed)	8	1	–	–	2.0
LDCR (C = 0)	52	3	A	–	13.0
(1 ⩽ C ⩽ 8)	20+2C	3	B	–	5.5 - 9.0
(9 ⩽ C ⩽ 15)	20+2C	3	A	–	9.5 - 12.5
LI	12	3	–	–	3.0
LIMI	16	2	–	–	4.0
LREX	12	1	–	–	3.0
LWPI	10	2	–	–	2.5
MOV	14	4	A	A	3.5
MOVB	14	4	B	B	3.5
MPY	52	5	A	–	13.0
NEG	12	3	A	–	3.0

Table 4-1. Instruction Execution Times (Continued)

Instruction	Clock Cycles C	Memory Access M	Address Modification† Source	Address Modification† Dest.	Execution Time in μsecs.
ORI	14	4	–	–	3.5
RSET	12	1	–	–	3.0
RTWP	14	4	–	–	3.5
S	14	4	A	A	3.5
SB	14	4	B	B	3.5
SBO	12	2	–	–	3.0
SBZ	12	2	–	–	3.0
SETO	10	3	A	–	2.5
Shift (C ≠ 0)	12+2C	3	–	–	3.5 - 10.5
(C=0, bits 12-15 of WR0 = 0)	52	4	–	–	13.0
(C=0, bits 12-15 of WR0=N≠0)	20+2N	4	–	–	5.5 - 12.5
SOC	14	4	A	A	3.5
SOCB	14	4	B	B	3.5
STCR (C=0)	60	4	A	–	15.0
(1⩽C⩽7)	42	4	B	–	10.5
(C=8)	44	4	B	–	11.0
(9⩽C⩽15)	58	4	A	–	14.5
STST	8	2	–	–	2.0
STWP	8	2	–	–	2.0
SWPB	10	3	A	–	2.5
SZC	14	4	A	A	3.5
SZCB	14	4	B	B	3.5
TB	12	2	–	–	3.0
X**	8	2	A	–	2.0
XOP	36	8	A	–	9.0
XOR	14	4	A	–	3.5
$\overline{\text{RESET}}$ function	26	5	–	–	6.5
$\overline{\text{LOAD}}$ function	22	5††	–	–	6.0
Interrupt context switch	22	5	–	–	5.5
Undefined op codes 0000-01FF, 0320-033F, 0C00-0FFF, 0780-07FF	6	1	--	–	1.5

*Execution time is dependent upon the partial quotient after each clock cycle during execution.

**Execution time is added to the execution time of the instruction located at the source address minus 4 clock cycles and 1 memory access time.

†The letters A and B refer to the respective address modification lists, Part A and Part B, that follow.

††Two memory cycles are from ROM, which requires one wait state per cycle. Hence, 0.5 μsec is added to the execution time.

Table 4-1. Instruction Execution Times (Continued)

Address Modification – Part A

Addressing Mode	Clock Cycles C	Memory Accesses M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

Address Modification – Part B

Addressing Mode	Clock Cycles C	Memory Accesses M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

As an example, when the instruction MOVB is used in a system with $t_c(\phi) = 4$ MHz (0.250 μsec) and no wait states are required to access memory variables in the execution time formula, $T = [t_c(\phi)]$ [WM + C]

where:

$t_c(\phi)$ = 0.250
C = 14 (clock cycles from table)
W = 0 (no wait states)
M = 4 (memory cycles from table)

$T = t_c(\phi)$ (WM + C)

$T = [t_c(\phi)]$ [WM + C] = (0.250) (0 × 4 + 14)μs = 3.5 μs.

If two wait states per memory access were required, the execution time is:

T = (0.250) (2 × 4 + 14)μs = 5.5 μs.

If the source operand was addressed in the symbolic mode and two wait states were required, then:

$$T = [t_c(\phi)]\ [WM + C]$$

$$C = 14 + 8 = 22$$

$$M = 4 + 1 = 5$$

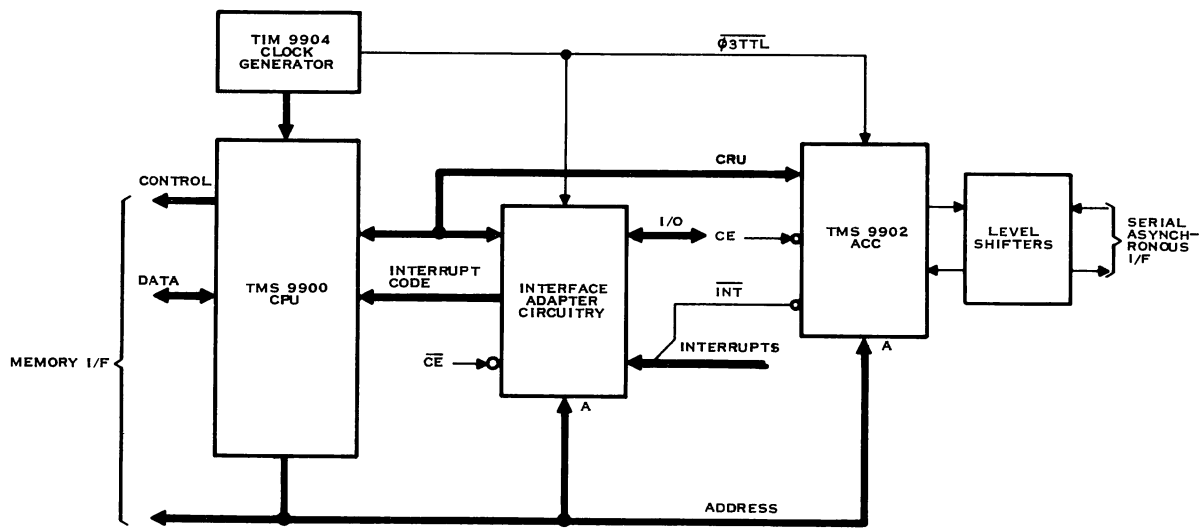
$$T = (0.250)\ (2 \times 5 + 22)\mu s = 55\ \mu s.$$

The following are general definitions of the various wait states and the required number of wait cycles to complete the operation.

Wait cycle = 1 clock cycle (0.250 μsecs)
Refresh cycle (occurs every 15.5 μsecs) = 1 or 2 wait cycles
ROM access always = 1 wait cycle
TILINE access always at least 1 wait cycle but may involve wait cycles up to 10.5 μsecs (42 wait cycles; TILINE timeout).
Interrupts from incoming TILINE cycle may cause 1 or 2 wait cycles.
Normal access time to on-board RAM has no wait cycles.

4.4 TMS 9902 ASYNCHRONOUS COMMUNICATION CONTROLLERS (COMM. PORTS 1 AND 2)

The relationship of the Asynchronous Communications Controllers (ACC) to other components in the 990/5 is shown in figure 4-1. The ACC is connected to the asynchronous channel through level shifters which translate the TTL inputs and outputs to RS-232C levels. The microprocessor transfers data to and from the ACC via the Communications Register Unit (CRU).



(A) 139354

Figure 4-1. TMS 9902 (Ports 1 and 2)

4.4.1 CPU INTERFACE. The ACC interfaces to the CPU through the CRU (figure 4-2). The CRU interface consists of five address-select lines (BA10 through BA14 connected to S0 through S4, respectively), PORT1SEL— or PORT2SEL— connected to chip enable ($\overline{CE}$), and three CRU control lines (CRUIN, CRUOUT, and CRUCLK). When $\overline{CE}$ becomes active (low), the five select lines address the CRU bit being accessed. When data is being transferred to the ACC from the CPU, CRUOUT contains the valid data bit and is strobed by CRUCLK. When ACC data is being read, CRUIN is the data bit output by the ACC.

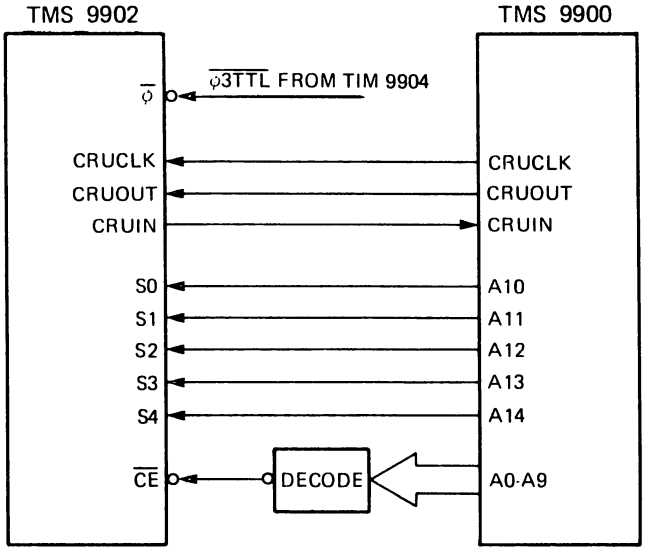


Figure 4-2. ACC-CPU Interconnection

4.4.2 COMMUNICATIONS CHANNEL INTERFACE. The interface to the asynchronous communications channel consists of an output control line ($\overline{RTS}$ connected to P1RTS— or P2RTS—), two input status lines ($\overline{DSR}$ connected to DSR1— or DSR2— and $\overline{CTS}$ connected to CTS1— or CTS2—), and serial transmit (XOUT) and receive (RIN) data lines. The request-to-send ($\overline{RTS}$) line is active (low) whenever the transmitter is activated. However, before data transmission begins, the clear-to-send ($\overline{CTS}$) input must be active. The data set ready ($\overline{DSR}$) input does not affect the receiver or transmitter. When $\overline{DSR}$ or $\overline{CTS}$ changes level, an interrupt is generated.

4.4.3 INTERRUPT OUTPUT. The interrupt output ($\overline{INT}$) is active (low) when any of the following conditions occur and the corresponding interrupt has been enabled by the CPU:

- $\overline{DSR}$ or $\overline{CTS}$ changes levels (DSCH = 1)
- A character has been received and stored in the Receive Buffer Register (RBRL = 1)
- The Transmit Buffer Register is empty (XBRE = 1)
- The selected time interval has elapsed (TIMELP = 1).

4.4.4 CLOCK INPUT. The clock input to the ACC is PH3— (connected to ϕ) and is provided by the four-phase clock generator/driver (74LS362). PH3— is used to generate the internal device clock, which provides the time base for the transmitter, receiver, and interval timer of the ACC.

4.4.5 CONTROL AND DATA OUTPUT. Data and control information is transferred to the ACC using $\overline{CE}$, S0 - S4, CRUOUT, and CRUCLK. Figure 4-2 shows the connection of the ACC to the TMS 9900 CPU. The high-order CPU address lines are used to decode the CE signal when the device is being selected. The low-order address lines are connected to the five address-select lines (S0 - S4). Table 4-2 describes the output bit address assignments for the ACC.

Table 4-2. CRU Output Bits to Ports 1 or 2 (TMS 9902)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET	NOT USED									DSCENB	TIMENB	XBIENB	RIENB	SRKON	RTSON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTMD	LDCTRL	LDIR	LRDR	LXDR	CONTROL, INTERVAL, RECEIVE DATA RATE, TRANSMIT DATA RATE, AND TRANSMIT BUFFER REGISTERS										

CONTROL REGISTER

1	X	X	X	SBS1	SBS2	PENB	PODD	CLK4M	–	RCL1	RCL0

Stop Bits		Party		tint =	Character Length	
00	1-1/2	0X	none		00	5
01	2	10	even	$f_{\overline{\phi}}/(3+CLK4M)$	01	6
1X	1	11	odd		10	7
					11	8

INTERVAL REGISTER

0	1	X	X	TMR7	TMR 6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0

TMR

T_{ITVL} = tint X 64 X TMR

RECEIVE DATA RATE REGISTER

0	0	1	X	RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0

RDR

frcv = tint ÷ 8^{RDV8} ÷ RDR ÷ 2

TRANSMIT DATA RATE REGISTER

0	0	X	1	XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0

XDR

fxmt = tint ÷ 8^{XDV8} ÷ XDR ÷ 2

TRANSMIT BUFFER REGISTER

0	0	0	0	XBR7	XBR6	XBR5	XBR4	XBR3	XBR2	XBR1	XBR0

NOTE 1: LOADING OF THE BIT INDICATED BY ☐ CAUSES THE LOAD CONTROL FLAG FOR THAT REGISTER TO BE AUTOMATICALLY RESET.

Table 4-2. CRU Output Bits to Ports 1 or 2 (TMS 9902) (Continued)

Bit 31 (RESET)– Writing a one or zero to Bit 31 causes the device to be reset, disabling all interrupts, initializing the transmitter and receiver, setting $\overline{RTS}$ inactive (high), setting all register load control flags (LDCTRL, LDIR, LRDR, and LXDR) to a logic one level, and resetting the BREAK flag. No other input or output operations should be performed for 11ϕ clock cycles after issuing the RESET command.

Bit 30–Bit 22– Not used.

Bit 21 (DSCENB)– Data Set Change Interrupt Enable. Writing a one to Bit 21 causes the $\overline{INT}$ output to be active (low) whenever DSCH (Data Set Status Change) is a logic one. Writing a zero to Bit 21 causes DSCH interrupts to be disabled. Writing either a one or zero to Bit 21 causes DSCH to be reset.

Bit 20 (TIMENB)– Timer Interrupt Enable. Writing a one to Bit 20 causes the $\overline{INT}$ output to be active whenever TIMELP (Timer Elapsed) is a logic one. Writing a zero to Bit 20 causes TIMELP interrupts to be disabled. Writing either a one or zero to Bit 20 causes TIMELP and TIMERR (Timer Error) to be reset.

Bit 19 (XBIENB)– Transmit Buffer Interrupt Enable. Writing a one to Bit 19 causes the $\overline{INT}$ output to be active whenever XBRE (Transmit Buffer Register Empty) is a logic one. Writing a zero to Bit 19 causes XBRE interrupts to be disabled. The state of XBRE is not affected by writing to Bit 19.

Bit 18 (RIENB)– Receiver Interrupt Enable. Writing a one to Bit 18 causes the $\overline{INT}$ output to be active whenever RBRL (Receive Buffer Register Loaded) is a logic one. Writing a zero to Bit 18 disables RBRL interrupts. Writing either a one or zero to Bit 18 causes RBRL to be reset.

Bit 17 (BRKON)– Break On. Writing a one to Bit 17 causes the XOUT (Transmitter Serial Data Output) to go to a logic zero whenever the transmitter is active and the Transmit Buffer Register (XBR) and the Transmit Shift Register (XSR) are empty. While BRKON is set, loading of characters into the XBR is inhibited. Writing a zero to Bit 17 causes BRKON to be reset and the transmitter to resume normal operation.

Bit 16 (RTSON)– Request-to-Send On. Writing a one to Bit 16 causes the $\overline{RTS}$ output to be active (low). Writing a zero to Bit 16 causes $\overline{RTS}$ to go to a logic one after the XSR and XBR are empty, and BRKON is reset. Thus, the $\overline{RTS}$ output does not become inactive (high) until after character transmission has been completed.

Bit 15 (TSTMD)– Test Mode. Writing a one to Bit 15 causes $\overline{RTS}$ to be internally connected to $\overline{CTS}$, XOUT to be internally connected to RIN, $\overline{DSR}$ to be internally held low, and the Interval Timer to operate at 32 times its normal rate. Writing a zero to Bit 15 reenables normal device operation.

Table 4-2. CRU Output Bits to Ports 1 or 2 (TMS 9902) (Continued)

Bit 14 (LDCTRL)– Load Control Register. Writing a one to Bit 14 causes LDCTRL to be set to a logic one. When LDCTRL = 1, any data written to bits 0-7 are directed to the Control Register. Note that LDCTRL is also set to a logic one when a one or zero is written to Bit 31 (RESET). Writing a zero to Bit 14 causes LDCTRL to be reset to a logic zero, disabling loading of the Control Register. LDCTRL is also automatically reset to a logic zero when a datum is written to Bit 7 of the Control Register which normally occurs as the last bit written when loading the Control Register with a LDCR instruction.

Bit 13 (LDIR)– Load Interval Register. Writing a one to Bit 13 causes LDIR to be set to a logic one. When LDIR = 1 and LDCTRL = 0, any data written to Bits 0-7 are directed to the Interval Register. Note that LDIR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Interval Register loading is not enabled until LDCTRL is set to a logic zero. Writing a zero to Bit 13 causes LDIR to be reset to logic zero, disabling loading of the Internal Register. LDIR is also automatically reset to logic zero when a datum is written to Bit 7 of the Interval Register, which normally occurs as the last bit written when loading the Interval Register with a LDCR instruction.

Bit 12 (LRDR)– Load Receive Data Rate Register. Writing a one to Bit 12 causes LRDR to be set to a logic one. When LRDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Receive Data Rate Register. Note that LRDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Receive Data Rate Register loading is not enabled until LDCTRL and LDIR have been set to a logic zero. Writing a zero to Bit 12 causes LRDR to be reset to a logic zero, disabling loading of the Receive Data Rate Register. LRDR is also automatically reset to logic zero when a datum is written to Bit 10 of the Receive Data Rate Register, which normally occurs as the last bit written when loading the Receive Data Rate Register with a LDCR instruction.

Bit 11 (LXDR)– Load Transmit Data Rate Register. Writing a one to Bit 11 causes LXDR to be set to a logic one. When LXDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Transmit Data Rate Register. Note that loading of both the Receive and Transmit Data Rate Registers is enabled when LDCTRL = 0, LDIR = 0, LRDR = 1, and LXDR = 1; thus these two registers may be loaded simultaneously when data are received and transmitted at the same rate. LXDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Transmit Data Rate Register loading is not enabled until LDCTRL and LDIR have been reset to logic zero. Writing a zero to Bit 11 causes LXDR to be reset to logic zero, disabling loading of the Transmit Data Rate Register. Since Bit 11 is the next bit addressed after loading the Transmit Data Rate Register, the register may be loaded and the LXDR flag reset with a single LDCR instruction where 12 bits (Bits 0-11) are written, with a zero written to Bit 11.

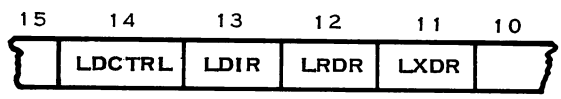
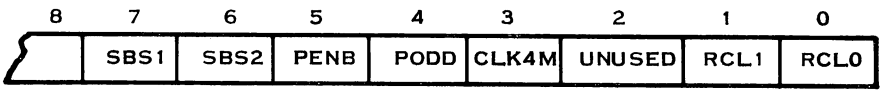


Table 4-2. CRU Output Bits to Ports 1 or 2 (TMS 9902) (Continued)

LDCTRL	LDIR	LRDR	LXDR	Register Enabled
1	X	X	X	Control Register
0	1	X	X	Interval Register
0	0	1	X	Receive Data Rate Register
0	0	X	1	Transmit Data Rate Register
0	0	0	0	Transmit Buffer Register

Control Register Bits

When the register load control flag identifies control register, data in bit positions 0 through 7 select character length, device clock operation, parity, and the number of stop for the transmitter circuit.



Name	Description
SBS1, SBS2	Stop Bit Select
PENB	Parity Enable
PODD	Odd Parity Select
CLK4M	$\overline{\phi}$ Input Divide Select
–	Not Used
RCL1, RCL0	Character Length Select

Bits 7 and 6 (SBS1 and SBS2)–

Stop Bit Selection. The number of stop bits to be appended to each transmitter character is selected by Bits 7 and 6 of the Control Register as shown below. The receiver only tests for a single stop bit, regardless of the status of Bits 7 and 6.

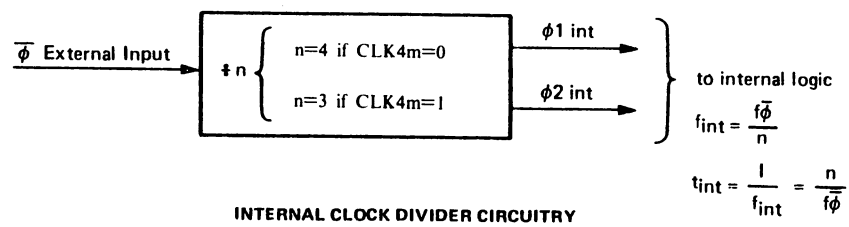
SBS1 Bit 7	SBS2 Bit 6	Number of Transmitted Stop Bits
0	0	1½
0	1	2
1	0	1
1	1	1

Table 4-2. CRU Output Bits to Ports 1 or 2 (TMS 9902) (Continued)

Bits 5 and 4 (PENB and PODD)– Parity Selection. The type of parity to be generated for transmission and detected for reception is selected by Bits 5 and 4 of the Control Register as shown below. When parity is enabled (PENB = 1), the parity bit is transmitted and received in addition to the number of bits selected for the character length. Odd parity is such that the total number of ones in the character and parity bit, exclusive of stop bits(s), will be odd. For even parity, the total number of ones will be even.

PENB Bit 5	PODD Bit 4	Parity
0	0	None
0	1	None
1	0	Even
1	1	Odd

Bit 3 (CLK4M) $\overline{\phi}$ Input Divide Select. The $\overline{\phi}$ input to the TMS 9902 ACC is used to generate internal dynamic logic clocking and to establish the time base for the Interval Timer, Transmitter, and Receiver. The $\overline{\phi}$ input is internally divided by either 3 or 4 to generate the two-phase internal clocks required for MOS logic, and to establish the basic internal operating frequency (f_{int}) and internal clock period (t_{int}). When bit 3 of the Control Register is set to a logic one (CLK4M = 1), $\overline{\phi}$ is internally divided by 4, and when CLK4M = 0, $\overline{\phi}$ is divided by 3. For example, when $f\overline{\phi}$ = 4 MHz, as in a standard 4 MHz TMS 9900 system, and CLK4M = 1, $\overline{\phi}$ is internally divided by 4 to generate an internal clock period t_{int} of 1 μs. The figure below shows the operation of the internal clock divider circuitry. When $f\overline{\phi} > 3.0$ MHz, CLK4M should be set to a logic zero.



INTERNAL CLOCK DIVIDER CIRCUITRY

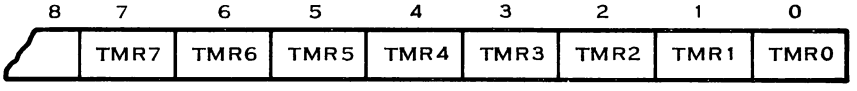
Bits 1 and 0 (RCL1 and RCL0)– Character Length Select. The number of data bits in each transmitted and received character is determined by Bits 1 and 0 of the Control Register as shown below.

RCL1 Bit 1	RCL0 Bit 0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	0	8 bits

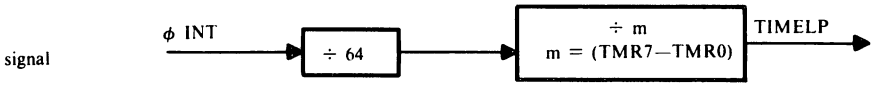
Table 4-2. CRU Output Bits to Ports 1 or 2 (TMS 9902) (Continued)

Interval Register Bits

When the interval register flag is set, data in bit positions 0 through 7 indicate the rate at which interrupts are generated by the interval timer of the TMS9902



As an example, if the Interval Register is loaded with a value of 80_{16} (128_{10}), the interval at which Timer Interrupts are generated is $^{t}ITVL = {}^{t}int \bullet 64 \bullet M = (1\ \mu s)\ (\bullet\ 64)\ (\bullet\ 128) = 8.192$ ms. when $^{t}int = 1\ \mu s$.

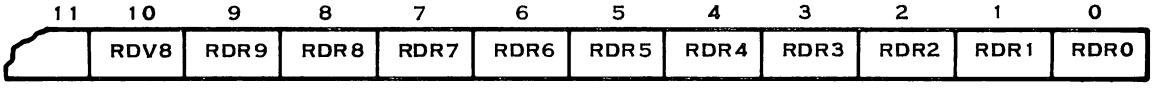


frequency	^{f}int	$^{f}int/64$	$^{f}int/(64)(m)$
time	^{t}int	64 ^{t}int	64 m ^{t}int

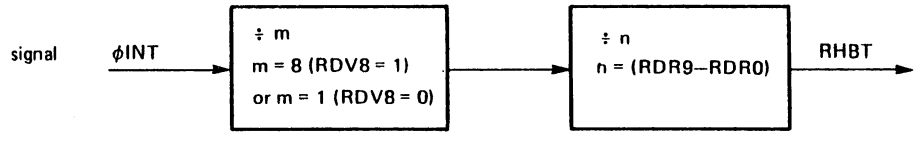
TIME INTERVAL SELECTION

Receive Data-Rate Register Bits

When the receive data-rate register flag is set, data in bit positions 0 through 10 select the bit rate at which data is received from a source external to the 990/5 (9902).



The following diagram describes the manner in which the receive data rate is established. Basically, two programmable counters are used to determine the interval for one-half the bit period of receive data. The first counter either divides the internal system clock frequency (f_{int}) by either 8 (RDV8 = 1) or 1 (RDV8 = 0). The second counter has ten stages and may be programmed to divide its input signal by any value from 1 (RDR9–RDR0 = 0000000001) to 1023 (RDR8–RDR0 = 1111111111). The frequency of the output of the second counter (f_{RHBT}) is double the receive-data rate. Register is loaded with a value of 11000111000, RDV8 = 1, and RDR9–RDR0 = 1000111000 = 238_{16} = 568 10. Thus, for f_{int} = 1 MHz, the receive-data rate = $1 \times 10^{6} \div 8 \div 568 \div 2 = 110.04$ bits per second.



frequency ^{f}int $\quad \frac{^{f}int}{m} \quad \frac{^{f}int}{mn} = {}^{f}RHBT$

RECEIVE DATA RATE SELECTION

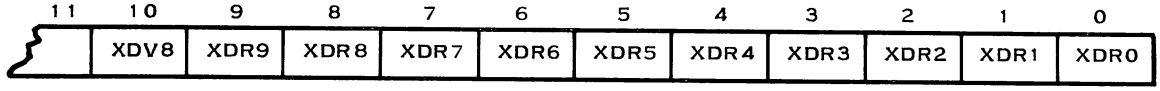
Quantitatively, the receive-data rate ^{f}RCV may be described by the following algebraic expression:

$$^{f}RCV = \frac{^{f}RHBT}{2} = \frac{^{f}int}{2mn} = \frac{^{f}int}{(2)\ (8^{RDV8})\ (RDR9—RDR0)}$$

Table 4-2. CRU Output Bits to Ports 1 or 2 (TMS 9902) (Continued)

Transmit Data-Rate Register Bits

When the transmit data-rate register flag is set, data in bit positions 0 through 10 select the bit rate at which data is to be transmitted to a destination external to the 990/5 (9902).



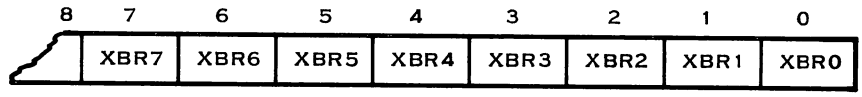
Selection of transmit data rate is accomplished with the Transmit Data Rate Register in the same way that the receive data rate is selected with the Receive Data Rate Register. The algebraic expression for the Transmit Data Rate f_{XMT} is:

$$f_{XMT} = \frac{f_{XHBT}}{} = \frac{f_{int}}{(2)\,(8^{XDV8})\,(XDR9\text{-}XDB0)}$$

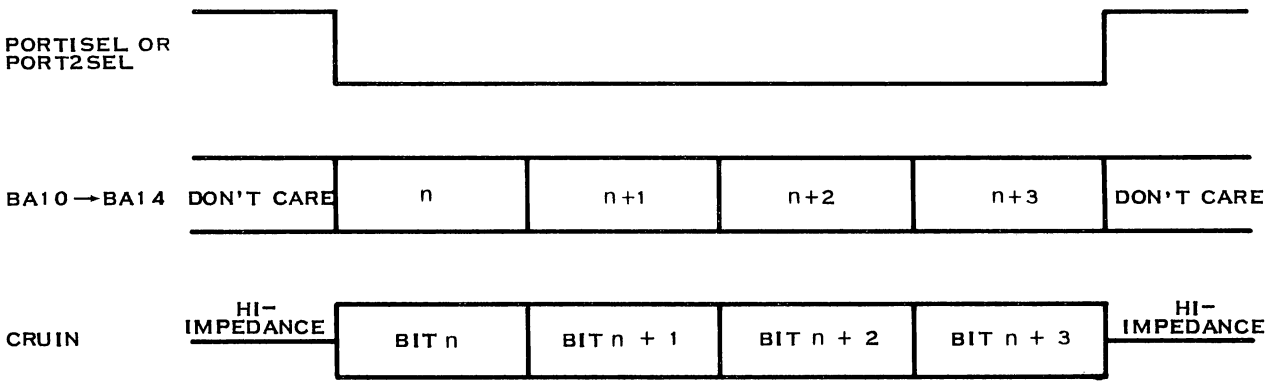
For example, if the Transmit Data Rate Register is loaded with a value of 00110100001, XDV8 = 0, and XDR9–XDR0 = $1A1_{16}$ = 417, the transmit data rate = $1 \times 10^6 \div 2 \div 1 \div 417$ = 1199.04 bits per second.

Transmit Buffer Register Bits

When the transmit buffer register flag is set, data in bit positions 0 through 7 contains the next character to be transmitted to a destination, external to the 990/5 (9902). The Transmit Buffer Register is used for storage of the next character to be transmitted. When the transmitter is active the contents of the Transmit Buffer Register are transferred to the Transmit Shift Register each time the previous character has been completely transmitted. The bit address assignments for the Transmit Buffer Register are shown below. All eight bits should be transferred into the register, regardless of the selected character length. The extraneous high-order bits will be ignored for transmission purposes; however, loading of bit 7 is internally detected to cause the Transmit Buffer Register Empty (XBRE) status flag to get reset.



4.4.6 STATUS AND DATA INPUT. Status and data information is read from the ACC using PORT1SEL— or PORT2SEL ($\overline{CE}$), BA10 through BA14 (connected to S0 through S4, respectively), and CRUIN. The following timing diagram illustrates the relationship of the signals used to access data from the ACC. Table 4-3 describes the input bit address assignments for the ACC.



Bits 36 & 37 of CRU base 1780 are interrupt enables for Port 1 and Port 2, respectively. Bit 39 of CRU base 1780 enables the EIA outputs of Ports 1, 2, and 3.

Table 4-3. CRU Input Bits from Ports 1 or 2 (TMS 9902)

Bit 31 (INT)–	INT = DSCINT + TIMINT + XBINT + RBINT. The interrupt output ($\overline{INT}$) is active when this status signal is a logic 1.
Bit 30 (FLAG)–	FLAG = LDCTRL + LDIR + LRDR + LXDR + BRKON. When any of the register load control flags or BRKON is set, FLAG = 1.
Bit 29 (DSCH)–	Data Set Status Change Enable. DSCH is set when the $\overline{DSR}$ or $\overline{CTS}$ input changes state. To ensure recognition of the state change, $\overline{DSR}$ or $\overline{CTS}$ must remain stable in its new state for a minimum of two internal clock cycles. DSCH is reset by an output to bit 21 (DSCENB).
Bit 28 (CTS)–	Clear to Send. The CTS signal indicates the inverted status of the $\overline{CTS}$ device input.
Bit 27 (DSR)–	Data Set Ready. The DSR signal indicates the inverted status of the $\overline{DSR}$ device input.
Bit 26 (RTS)–	Request to Send. The RTS signal indicates the inverted status of the $\overline{RTS}$ device output.
Bit 25 (TIMELP)–	Timer Elapsed. TIMELP is set each time the Interval Timer decrements to 0. TIMELP is reset by an output to bit 20 (TIMENB).
Bit 24 (TIMERR)–	Timer Error. TIMERR is set whenever the Interval timer decrements to 0 and TIMELP is already set, indicating that the occurrence of TIMELP was not recognized and cleared by the CPU before subsequent intervals elapsed. TIMERR is reset by an output to bit 20 (TIMENB).
Bit 23 (XSRE)–	Transmit Shift Register Empty. When XSRE = 1, no data is currently being transmitted and the XOUT output is at logic 1 unless BRKON is set. When XSRE = 0, transmission of data is in progress.

Table 4-3. CRU Input Bits from Ports 1 or 2 (TMS 9902) (Continued)

Bit 22 (XBRE)–	Transmit Buffer Register Empty. When XBRE = 1, the transmit buffer register does not contain the next character to be transmitted. XBRE is set each time the contents of the transmit buffer register are transferred to the transmit shift register, XBRE is reset by an output to bit 7 of the transmit buffer register (XBR7), indicating that a character has been loaded.
Bit 21 (RBRL)–	Receive Buffer Register Loaded. RBRL is set when a complete character has been assembled in the receive shift register and the character is transferred to the receive buffer register. RBRL is reset by an output to bit 18 (RIENB).
Bit 20 (DSCINT)–	Data Set Status Change Interrupt. DSCINT = DSCH (input bit 29) • DSCENB (output bit 21). DSCINT indicates the presence of an enabled interrupt caused by the changing of state of $\overline{\text{DSR}}$ or $\overline{\text{CTS}}$.
Bit 19 (TIMINT)–	Timer Interrupt. TIMINT = TIMELP (input bit 25) • TIMENB (output bit 20). TIMINT indicates the presence of an enabled interrupt caused by the interval timer.
Bit 17 (XBINT)–	Transmitter Interrupt. XBINT = XBRE (input bit 22) • XBIENB (output bit 19). XBINT indicates the presence of an enabled interrupt caused by the transmitter.
Bit 16 (RBINT)–	Receiver Interrupt. RBINT = RBRL (input bit 21) • RIENB (output bit 18). RBINT indicates the presence of an enabled interrupt caused by the receiver.
Bit 15 (RIN)–	Receive Input. RIN indicates the status of the RIN input to the device.
Bit 14 (RSBD)–	Receive Start Bit Detect. RSBD is set one-half bit time after the 1-to-0 transition of RIN indicating the start bit of a character. If RIN is not still 0 at this point in time, RSBD is reset. Otherwise, RSBD remains true until the complete character has been received. This bit is normally used for testing purposes.
Bit 13 (RFBD)–	Receive Full Bit Detect. RFBD is set one bit time after RSBD is set to indicate the sample point for the first data bit of the received character. RSBD is reset when the character has been completely received. This bit is normally used for testing purposes.
Bit 12 (RFER)–	Receive Framing Error. RFER is set when a character is received in which the stop bit, which should be a logic 1, is a logic 0. RFER should only be read when RBRL (input bit 21) is a 1. RFER is reset when a character with the correct stop bit is received.
Bit 11 (ROVER)–	Receive Overrun Error. ROVER is set when a new character is received before the RBRL flag (input bit 21) is reset, indicating that the CPU failed to read the previous character and reset RBRL before the present character is completely received. ROVER is reset when a character is received and RBRL is 0 when the character is transferred to the receive buffer register.
Bit 10 (RPER)–	Receive Parity Error. RPER is set when a character is received in which the parity is incorrect. RPER is reset when a character with correct parity is received.
Bit 9 (RCVERR)–	Receive Error. RCVERR = RFER + ROVER + RPER. RCVERR indicates the presence of an error in the most recently received character.
Bit 7–Bit 0 (RBR7–RBR0)–	Receive Buffer Register. The receive buffer register contains the most recently received character. For character lengths of fewer than 8 bits the character is right justified, with unused most significant bit(s) all zero(es). The presence of valid data in the receive buffer register is indicated when RBRL is a logic 1.

4.5 TMS 9903 SYNCHRONOUS COMMUNICATIONS CONTROLLER (COMM. PORT 3)

The TMS 9903 Synchronous Communications Controller (SCC) has a wide range of capabilities in synchronous and asynchronous communications control. The SCC interfaces directly with the CPU by means of the communications register unit (CRU) in the 990/5 microcomputer. All device command, status, and data transfers occur under CPU control via the CRU interface. The relationship of the SCC and other components of the 990/5 is shown in figure 4-3.

Device reset and initialization is accomplished by software to provide maximum flexibility with minimum pin count. Data transfers occur bit serially between the SCC and the CPU and are controlled via the five transfer lines BA10 through BA14 (connected to the S0 through S4, respectively), chip enable line PORT3SELA— ($\overline{CE}$), and the three CRU lines (CRUIN, CRUOUT, CURCLK). The five address lines define the 32 bits read from, or written to, the SCC by the CPU. Bits 12 through 31 are control bits and define the contents of the flag register fields thereby determining the mode of operation and configuration of the SCC.

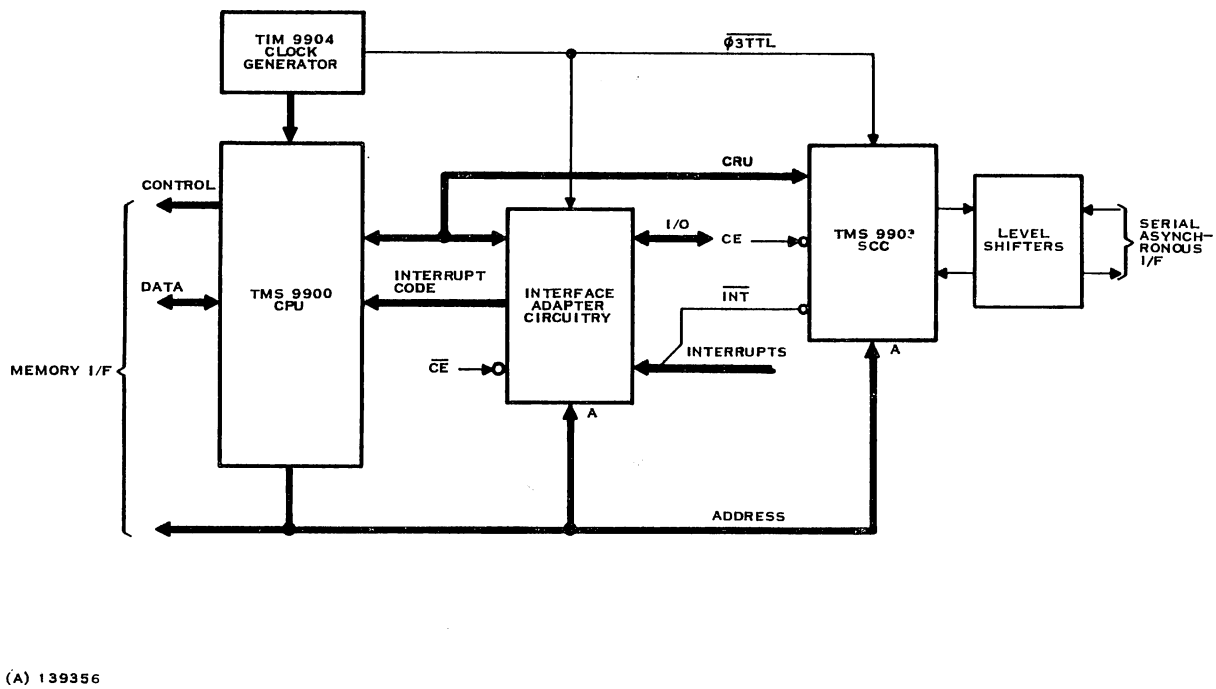


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Figure 4-3. TMS 9903 (Port 3) in the 990/5

4.5.1 CRU OUTPUT DATA TO COMMUNICATIONS CHANNEL (PORT 3). Tables 4-4 through 4-9 describe CRU bit assignments for CRUOUT data. As can be noted from the tables, certain bit fields change their definition depending on the specific mode of operation selected.

Table 4-4. CRU Output Bits to Port 3 (TMS 9903)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET	CLRXMT CLRRCV	CLXCRC CLRCRC	XZINH RSYNDL	LDSYN2	RHRRD LDSYN1	LXBC	LXCRC	XPRNT BRKON	XAIENB	DSCENB	TIMENB	XBIENB	RIENB	RTS	XMTON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTMODE	LDCTRL	LDIR	LRCRC	DRCK32	CRC1	CRC0	MDSL2	MDSL1	MDSL0	CLS1	CLS0	CLK4M	RSCL2	RSCL1	RSCL0

	CRU Address BA10→BA14	Mode* 0	1	2	3	5	6	Name	CRUOUT Value	Description
Single Bit Control Function	31	X	X	X	X	X	X	RESET	0/1	Clear and disable all interrupts. Initialize all controllers, reset all flags, Set LDCTRL
	30	X	X	X	X	X	X	CLRXMT	1	Clear transmitter and reset XMT interrupts
								CLRRCV	0	Clear receiver and reset RCV interrupts
	29	X	X	X	X	X	X	CLXCRC	1	Clear XMT CRC register to all zeros
								CLRCRC	0	Clear RCV CRC register to all zeros
	28	X		X		X	X		NA	
			X					XZINH	1	Inhibit zero insertion
									0	Enable zero insertion
									1	Delete sync characters (disabled when XPRNT is set)
					X			RSYNDL		
									0	Reset RSYNDL
	27	X	X	X	X			LDSYN2	1	Load sync character register 2
									0	Reset LDSYN2
						X	X		NA	
	26	X				X	X		NA	
			X					RHRRD	1	Read RCV holding register
									0	Reset RHRL and RHROV
				X	X			LDSYN1	1	Load sync character register 1
									0	Reset LDSYN1
	25	X	X	X	X	X	X	LXBC	1	Load XMT buffer and CRC register
									0	Reset XBRE (XMT buffer empty) and LXBC
	24	X	X	X	X	X	X	LXCRC	1	Load XMT CRC buffer, enable read of XMTCRC register
									0	Reset LXCRC
	23	X						XPRNT	1	Transmit contents of SYNC2 register when no data available
									0	Abort transmit and suspend XMT operations when no data available
			X						1	Transmit SYNC2 w/o zero insertion when no data available
									0	Abort XMT and suspend XMT operations when no data available

*Mode selected by control bits 8, 7, and 6 (see table 4-6).

Table 4-4. CRU Output Bits to Port 3 (TMS 9903) (Continued)

CRU Address BA10→BA14	Mode* 0	1	2	3	5	6	Name	CRUOUT Value	Description
				X				1	Transmit SYNC2–SYNC1 when no data available
								0	Transmit SYNC1–SYNC1 when no data available
			X					NA	
					X	X	BRKON	1	Forces continuous Logic 0 on output line
								0	Resets BRKON
Single Bit Control Function: 22	X	X	X				XAIENB	1	Enable XMT abort interrupts & reset interrupt
								0	Disable XMT abort interrupts & reset interrupt
			X	X	X	X		NA	
21	X	X	X	X	X	X	DSCENB	1	Enable data set change interrupt & reset interrupt
								0	Disable data set change interrupt & reset interrupt
20	X	X	X	X	X	X	TIMENB	1	Enable timer interrupts & reset interrupt
								0	Disable timer interrupts & reset interrupt
19	X	X	X	X	X	X	XBIENB	1	Enable XMT buffer register interrupts
								0	Disable XMT buffer register interrupt
18	X		X	X	X	X	RIENB	1	Enable RCV interrupts & reset RBRL & ROVER
								0	Disable RBRL interrupts & reset RBRL & ROVER
		X						1	Reset RBRL, ROVER, RABRT, enable RBRL, RABRT, RHRL interrupts Reset RBRL, ROVER, RABRT, disable RBRL, RABRT, RHRL interrupts
17	X	X	X	X	X	X	RTS	1	Reset $\overline{\text{RTS}}$ and disable RTS AUT control
								0	Set $\overline{\text{RTS}}$ and disable RTS AUT
16	X	X	X	X	X	X	XMTON	1	Enable data transmission
								0	Disable transmission after completion of present character
15	X	X	X	X	X	X	TSTMODE	1	Place device in Test Mode. Decrement timers at 32 x normal rate. Tie XOUT to RIN, $\overline{\text{RTS}}$ to $\overline{\text{CTS}}$, SCR to $\overline{\text{SCT}}$. $\overline{\text{SCT}}$ generated internally at timer rate
								0	Normal operation
14	X	X	X	X	X	X	LDCTRL	1	Load control register
								0	Reset LDCTRL
13	X	X	X	X	X	X	LDIR	1	Load interval register
								0	Reset LDIR
12	X	X	X	X	X	X	LRCRC	1	Load RCVCRC register, read RCVCRC register
								0	Reset LRCRC

*Mode selected by control bits 8, 7, and 6 (see table 4-6).

Table 4-4. CRU Output Bits to Port 3 (TMS 9903) (Continued)

	CRU Address BA10→BA14	Mode 0	1	2	3	5	6	Name	CRUOUT Value	Description
Control Register Assignments	11	X	X	X	X			DRCK32	1	32X Data Rate Clock. The SCT frequency is 32 times the transmit data rate, and the SCR frequency is 32 times the receive data rate, resynced on every transition of RIN. (NRZI data encoding.)
									0	Receive data is sampled on the zero-to-one transition of SCR, and transmit data is shifted out on the one-to-zero transition of $\overline{SCT}$.
						X	X		1	32X Data Rate Clock. The SCT frequency is 32 times the transmit data rate, and the SCR frequency is 32 times the receive data rate, resynced on every start bit received.
									0	Receive data is sampled on the zero-to-one transition of SCR, and transmit data is shifted out on the one-to-zero transition of $\overline{SCT}$.
	10	X	X	X	X	X	X	CRC1		CRC Polynomial Select (See Table 4-5)
	9	X	X	X	X	X	X	CRC0		
	8	X	X	X	X	X	X	MDSL2		Mode Select (See Table 4-6)
	7	X	X	X	X	X	X	MDSL1		
	6	X	X	X	X	X	X	MDSL0		
	5	X	X	X	X	X	X	CLS1		Configuration Select (See Table 4-7)
	4	X	X	X	X	X	X	CLS0		
	3	X	X	X	X	X	X	CLK4M	1	4X System Clock. The external clock input is internally divided by 4 to generate the system clock for the device.
									0	The external clock input is internally divided by 3 to generate the system clock for the device.
	2	X	X	X	X	X	X	RSCL2		Receive Character Length Select (See Table 4-8)
	1	X	X	X	X	X	X	RSCL1		
	0	X	X	X	X	X	X	RSCL0		

Table 4-5. CRC Polynomial Selection

CRC	CRC1	CRC0	Name	Polynomial
0	0	0	CRCC-16	$X^{16} + X^{15} + X^2 + 1$
1	0	1	CRCC-12	$X^{12} + X^{11} + X^3 + X^2 + X + 1$
2	1	0	REV. CRCC-16	$X^{16} + X^{14} + X + 1$
3	1	1	CRC-CCITT	$X^{16} + X^{12} + X^5 + 1$

Table 4-6. Mode Selection

Mode	MDSL2	MDSL1	MDSL0	Example Protocol	Sync Character	Fill Character
0	0	0	0	General	None	(SYNC2) or none
1	0	0	1	SDLC	$7E_{16}$	(SYNC2) or none
2	0	1	0	General	(SYNC1)	(SYNC2)
3	0	1	1	Bi-Sync	(SYNC1-SYNC1)	(SYNC1-SYNC1) or (SYNC2-SYNC1)
4	1	0	0			Not Used
5	1	0	1	Asynchronous operation with two stop bits		
6	1	1	0	Asynchronous operation with one stop bit		
7	1	1	1			Not Used

Table 4-7. Configuration Selection

Configuration	CSL1	CSL0	Mode 0	1	2	3	5	6	
0	0	0	x		x	x	x	x	No Parity Generation or Detection
				x					SDLC Normal (Non-Loop)
1	0	1	x		x	x	x	x	No Parity Generation or Detection
				x					SDLC Loop Master
2	1	0	x		x	x	x	x	Even Parity Generation on Transmission and Detection on Reception
				x					SDLC Loop Slave – Pending Synchronization
3	1	1	x		x	x	x	x	Odd Parity Generation on Transmission and Detection for Reception
				x					SDLC Loop Slave – Active

Table 4-8. Receive Character Length Select

RSCL2	RSCL1	RSCL0	Bits/Character
0	0	0	5
0	0	1	6
0	1	0	7
0	1	1	8
1	0	0	9

Table 4-9. CRUOUT Addresses 0-11 – Data Output

CRU Addresses BA10→BA14	LDSYN1	LDSYN2	LDIR	LRCRC	LXCRC	LXBC		All Flags=0
11	–	–	–	–	–	–	–	
10	–	–	–	–	–	–	–	
9	S10D(9)	S20D(9)	–	–	–	–	–	
8			–	RCRC(8)	XCRC(8)	XCRC(8)	XBR(8)	XBR(8)
7			IR0D(7)					
6								
5								
4								
3								
2								
1								
0	S10D(0)	S20D(0)	IR0D(0)	RCRC(0)	XCRC(0)	XCRC(0)	XBR(0)	XBR(0)
	Load Sync Register 1	Load Sync Register 2	Load Timer Register	Load Receive CRC Register	Load Transmit CRC Register	Load Transmit CRC Register and Data Buffer		Load Transmit Data Buffer

4.5.2 CRU INPUT DATA FROM COMMUNICATIONS CHANNEL (PORT 3). Table 4-10 contains descriptions of input data bits 16 through 31 describing receiver status and interrupts. CRU input bits 0 through 15 contain receiver status and data when all flags = 0; i.e., CRUOUT bits 12, 24, 26 and 29 are all zero. If any one of these output bits to the SCC is set (logic 1), CRU input bits 0 through 15 contain the contents of the read-register in the SCC. This information is contained in tables 4-11 and 4-12.

4.5.3 MODEM COMMUNICATIONS, PORT 3 ONLY. When communications port 3 is used to support either a synchronous or an asynchronous modem, the CRU interface provides 48 directly addressable output and input bits. Address assignments for output and input bits 0 through 31 are the same as when the port is used for local communications. Address assignments for CRU output and input bits 32 through 47 are as shown in table 4-13. Table 4-14 contains information on port 3 synchronous clock rate.

To set, transmit, and receive clock rates, load CRU output bits 40 through 43 with values to achieve desired baud rate as shown in table 4-14. The transmit clock rate is set when CRU output bit 44 is set; the receive clock rate is set when CRU output bit 44 is reset. Selectable clock rates are as shown in table 4-14.

Table 4-10. CRUIN Addresses 16-31 – Receiver Status and Interrupts, Port 3

Address S0-S4	Mode 0	1	2	3	5	6	Name	Description
31	x	x	x	x	x	x	INT	INT = DSCINT + RINT + TIMINT + XAINT + XBINT
30	x	x	x	x	x	x	FLAG	FLAG = LDCTRL + LDSYN1 + LDSYN2 + LDIR + LRCRC + LXBC + LXCRC
29	x	x	x	x	x	x	DSCH	DATA SET CHANGE. Set when DSR, RTSAUT, and/or CTS change state. Reset by outout to bit address 21 (DSCENB).
28	x	x	x	x	x	x	CTS	Inverted level of $\overline{\text{CTS}}$ input.
27	x	x	x	x	x	x	DSR	Inverted level of $\overline{\text{DSR}}$ input.
26	x	x	x	x	x	x	RTSAUT	Output of RTSAUT, automatic RTS controller
25	x	x	x	x	x	x	TIMELP	TIMER ELAPSED. Set when selected time interval elapses. Reset by output to bit address 20 (TIMENB).
24	x	x	x	x	x	x	TIMERR	TIMER ERROR. Set when the selected time interval elapses and TIMELP is already set. Reset by output to bit address 20 (TIMENB).
23	x	x					XABRT	TRANSMITTER ABORT. Set by transmitter when no data is available for transmission and no provisions have been made to identify a fill sequence. Reset by output to bit address 22 (XAIENB).
			x	x	x	x		Not used (always = 0 except in test mode).

Table 4-10 CRUIN Addresses 16-31 – Receiver Status and Interrupts, Port 3 (Continued)

Address S0-S4	Mode 0	1	2	3	5	6	Name	Description
22	x	x	x	x	x	x	XBRE	TRANSMIT BUFFER REGISTER EMPTY. Set when the Transmit Buffer Register (XBR) is transferred to the Transmit Shift Register (XSR) and when the transmitter is initialized. Reset by writing a zero to output bit address 25 (LXBC).
21	x	x	x	x	x	x	RBRL	RECEIVE BUFFER REGISTER LOADED. Set when a complete character has been transferred from the Receive Shift Register (RSR). Reset by output to bit address 18 (RIENB).
20	x	x	x	x	x	x	DSCINT	DSCINT = DSCH • DSCENB.
19	x	x	x	x	x	x	TIMINT	TIMINT = TIMELP • TIMENB.
18	x	x					XAINT	XAINT = XABRT • XAIENB.
			x	x	x	x		Not used (always = 0).
17	x	x	x	x	x	x	XBINT	XBINT = XBRE • XMTON • XBIENB.
16	x	x	x	x	x	x	RINT	RINT = (RBRL + RHRL + RABRT) • RIENB.

Table 4-11. CRUIN Address 0-15 – Receiver Status and Data (All Flags = 0), Port 3

Address S0-S4	Mode 0	1	2	3	5	6	Name	Description
15	x	x	x	x	x	x	RIN	Level of RIN Input.
14	x		x	x				Not used (always = 0).
		x					RABRT	RECEIVER ABORT. Set when a flag sequence (01111110) has been previously detected and 7 consecutive ones are received. Reset by output to bit address 18.
					x	x	RSBD	RECEIVE START BIT DETECT. RSBD is set one-half bit time after the 1–0 transition of RIN indicating the start bit of a character. If RIN is not still 0 at this point in time, RSBD is reset. Otherwise, RSBD remains true until the complete.
13	x		x	x				Not used (always = 0).
		x					RHRL	RECEIVE HOLDING REGISTER LOADED. Set when the receiver has received a complete frame. Reset by output of a zero to bit address 26 (RHRRD).
					x	x	RFBD	RECEIVE FULL BIT DETECT. RFBD is set one full bit time after RSBD is set to indicate the sample point for the first data bit of the received character. RFBD is reset when the character has been completely received. This bit is normally used for testing purposes.

Table 4-11. CRUIN Address 0-15 – Receiver Status and Data (All Flags = 0), Port 3 (Continued)

Address S0-S4	Mode 0	1	2	3	5	6	Name	Description
12	x		x	x				Not used (always = 0).
		x					RHROV	RECEIVE HOLDING REGISTER OVERRUN. Set when the contents of the RHR are altered before RHRL is reset. Reset by output of a zero to bet address 26 (RHRRD).
					x	x	RFER	RECEIVE FRAMING ERROR. RFER is set when a character is received in which the stop bit, which should be a logic 1, is a logic 0. RFER should only be read when RBRL (input bit 21) is a logic 1. RFER is reset when a character with the correct stop bit is received.
11	x	x	x	x	x	x	ROVER	RECEIVE OVERRUN. Set when the RBR is loaded with new data before RBRL is reset. Reset by output to bit address 18 (RIENB).
10	x		x	x	x	x	RPER	RECEIVE PARITY ERROR. Set when the character transferred into the RBR contained incorrect parity. Reset when a character with correct parity is transferred to the RBR.
		x					RZER	RECEIVE ZERO ERROR. Set when the last 5 received bits prior to detection of the flag character ($7E_{16}$) are all ones, without being followed by a zero.
9	x		x	x	x	x	RCVERR	RCVERR = ROVER + RPER + RFER.
		x					RFLDT	RECEIVE FLAG DETECT. Set when flag is detected. Reset by output to bit 18.
8	x	x	x	x	x	x	RBR8	(MSB)
7	x	x	x	x	x	x		
6	x	x	x	x	x	x		
5	x	x	x	x	x	x		Contents of the RBR. When other than 9-bit character length is selected, the character is justified to the LSB and unused bit(s) will contain zero(s).
4	x	x	x	x	x	x		
3	x	x	x	x	x	x		
2	x	x	x	x	x	x		
1	x	x	x	x	x	x		
0	x	x	x	x	x	x	RBR0	(LSB)

Table 4-12. TMS 9903 CRU Input Bits 0 through 15 Address Assignments, Read Register Contents (Control Flag Set to 1), Port 3

Control Flag Address	CRUOUT 12 LRCRC	CRUOUT 24 LXCRC	CRUOUT 25 LXBC	CRUOUT 26 RHRRD
15	RCRC(15)	XCRC(15)	XCRC(15)	RHR(15)
14				
13				
12				
11				
10				
9				
8				
7				
6				
5				
4				
3				
2				
1				
0	RCRC(0)	XCRC(0)	XCRC(0)	RHR(0)
	Note 1	Note 2		Note 3

Notes: 1. Contents of the Receive CRC Generation Register, containing current value calculated by loading the CRC generator with each character received, according to the CRC polynomial selected by bits 9-10 of the Control Register.
2. Contents of the Transmit CRC Generation Register, containing current value calculated by loading the Transmit Buffer with bit 25, LXBC set or by loading the CRC generator with bit 24 LXCRC set, according to the CRC polynomial selected by bits of the Control Register.
3. Contents of the Receive Holding Register. This register is used only in mode 1 operation and contains the last 16 bits received prior to the flag.

Table 4-13. CRU Output and Input Bits 32 through 47 Address Assignments (Modem Communications)

Bit	CRU Output	CRU Input
32	Data terminal ready	Data carrier detect
33	Analog Loopback	Ring Indicator
34	Secondary request to send	Secondary data carrier detect
35	Not used	Identification switch position 0
36	Communications port 1 interrupt enable	Identification switch position 1
37	Communications port 2 interrupt enable	Identification switch position 2
38	Communications port 3 interrupt enable	Identification switch position 3
39	Communications enable (All 3 ports)	Identification switch position 4

Table 4-13. CRU Output and Input Bits 32 through 47 Address Assignments (Modem Communications) (Continued)

Bit	CRU Output	CRU Input
40	Clock rate A (See table 4-14)	Not used
41	Clock rate B (See table 4-14)	Not used
42	Clock rate C (See table 4-14)	Not used
43	Clock rate D (See table 4-14)	Not used
44	Strobe Clock rate (1 = transmit, 0 = receive)	Not used
45	Transmit clock select (1 = local, 0 = modem)	Not used
46	Receive clock select (1 = local, 0 = modem)	Not used
47	Not used	Not used

Table 4-14. Communications Port 3 Selectable Transmit and Receive Clock Rates (Synchronous Communications)

CRU Output Bits				Baud Rate
D	C	B	A	
43	42	41	40	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	200
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600

4.6 INTERPROCESSOR COMMUNICATIONS

When the 990/5 microcomputer is installed in a chassis slot other than slot 1, it performs as a slave processor. In a multiprocessor system, the 990/5 or higher level 990 CPU microcomputer installed in chassis slot 1 is referred to as the host processor. The slave processor and the host processor may interrupt each other, mask interrupts from each other, acknowledge interrupts from each other, and enable interrupts from each other on interrupt acknowledge. The host processor uses 64 CRU bits, beginning at CRU address hexadecimal F40 (Register R12 = hexadecimal 1E80), to communicate with up to sixteen slave processors. The 990/5 microprocessor circuit board contains three switches that permit selection of one of 16 groups of four bits each to which the slave processor responds. The 990/5 microprocessor uses four bits at CRU address hexadecimal 8F0 (register R12 = hexadecimal 17E0) to communicate with a host processor. Table 4-15 lists the CRU bit assignments and a description of each.

Table 4-15. Interprocessor Communications CRU Bit Assignments

Output Bit	Description
0	Interrupt remote processor
1	Interrupt local processor after receipt of remote processor interrupt acknowledge
2	Acknowledge interrupt from remote processor
3	Interrupt from remote processor mask
Input Bit	
0	Interrupt to remote processor active
1	Slave fault (in slave processor) or logic 0 (in host processor)
2	Interrupt from remote processor active
3	Slave idle (in slave processor) or logic 0 (in host processor)

4.7 990/5 OPERATION WITH HIGHER LEVEL 990 PROCESSORS

In operating the 990/5 microcomputer in a multiprocessor environment containing a higher level 990 series computer, the following limitations of the 990/5 microcomputer should be observed:

- Memory mapping is not implemented on the 990/5.
- No provision is made to execute XOP instructions off-board the 990/5.
- In the instruction set, instructions LDS, LDD, and LMF are not implemented on the 990/5. No illegal operation codes are detected. Unimplemented or illegal opcodes are treated as NO-OP codes.
- No privileged instructions are implemented on the 990/5.

SECTION V

INTERFACE REQUIREMENTS

5.1 GENERAL

This section will assist users and OEM equipment purchasers in interfacing peripherals with the 990/5 microcomputer. Of primary concern are inputs and outputs of the 990/5 microcomputer; descriptions of internal workings are covered in Sections I and IV. There are four different interfaces on the 990/5 microprocessor board:

- CRU/TILINE interface that connects into the backpanel (P1 and P2)
- Front edge board-mounted connector for the operator or programmer front panel (P3)
- Two RS232/EIA connectors for two asynchronous controllers (P4 and P5)
- One RS232/EIA connector for the synchronous/asynchronous controller (P6)

5.2 CRU/TILINE BACKPANEL CONNECTORS, P1 and P2

This interface is made through the back edge of the 990/5 board. The signals are interfaced in two groups of 80 contacts each for mating with two backplane (motherboard) receptacles. The backpanel serves as an interface for the CRU, interrupts, TILINE, miscellaneous other signals, and power. Table 5-1 lists all backpanel signals by connector pin number. The paragraphs and tables that follow outline signal descriptions.

5.2.1 CRU INTERFACE. The 990/5 microprocessor CRU interface signals are listed in table 5-2. If the microprocessor is not located in slot 1 of the chassis, the CRU inputs/outputs are disabled, i.e., signal SLOT1— goes high disabling output line drivers.

5.2.2. INTERRUPTS. Provision is made for 13 external interrupt inputs on the backpanel. In addition to the external intrrupts, two internal interrupts (power fail and error) are hardwired and not available external to the 990/5. Table 5-3 lists interrupt inputs, connector pin numbers, and switch options. Refer to paragraph 2.6 for wiring interrupts to levels.

5.2.3 CRU TIMING. The following paragraphs describe timing required for CRU operation.

5.2.3.1 CRU Power Supply Timing. Power-up and power-down timing sequences are shown in figure 5-1. This timing applies to TI supplied CRU power supplies only.

5.2.3.2 Processor CRU Output Timing. The processor conforms to minimum CRU timing restrictions as defined by figure 5-2. The figure shows the timing sequence for a LDCR R1, 2 instruction followed by a SBZ 15 instruction. Minimum timing restrictions are for both instructions. CRU addresses and module selects are defined only during the execution of CRU output or CRU input instructions. (If CRUBITOUT and STORECLK— are held high when the processor is not executing a CRU output instruction.) The CRU device clocks the CRUBITOUT line on the positive edge of the STORECLK— pulse.

Table 5-1. 990/5 System Interface Pin Out

Pin	Function	Pin	Function
P1-			
1, 2	GND	P1 - 38	CRUBIT14
3, 4	+5 MAIN	39, 40	+12 MAIN
5, 6	+12 MEMORY	41, 42	-12 MAIN
7, 8	+5 MEMORY	43	MODSEL3–
9, 10	-5 MEMORY	44	MODSEL4–
11	TLREAD	45	MODSEL5–
12	GND	46	MODSEL6–
13	TLPRES–	47	MODSEL7–
14	TLIORES–	48	MODSEL8–
15	GND	49	MODSEL9–
16	TLPFWP–	50	CRUBIT7
17	GND	51	MODSEL10–
18	CRUBITOUT	52	CRUBIT6
19	GND	53	MODSEL11–
20	TLTM–	54	CRUBIT5
21	GND	55	TLMER–
22	STORECLK–	56	CRUBIT4
23	MODSEL0–	57	GND
24	GND	58	TLAV
25	TLGO–	59	GND
26	GND	60	CRUBITIN
27	TLDAT12–	61	MODSEL12–
28	TLDAT13–	62	CRUBIT8
29	120HZ	63	TLWAIT–
30	TLDAT14–	64	CRUBIT9
31	TLDAT15–	65	OPEN
32	CRUBIT13	66	INTA–
33	IAQ–	67	MODSEL13–
34	CRUBIT15	68	CRUBIT10
35	MODSEL1–	69	MODSEL14–
36	CRUBIT12	70	CRUBIT11
37	MODSEL2–	71	TLAK–

Table 5-1. 990/5 System Interface Pin Out (Continued)

Pin	Function	Pin	Function
P1-		P2-26	TLHOLD–
72	GND	27	TLADR17–
73	OPEN	28	RESTART–
74	GND	29	TLADR16–
75	OPEN	30	GND
76	MODSEL15–	31	TLADR19–
77, 78	+5 MAIN	32	MODSEL19–
79, 80	GND	33	TLDAT09–
		34	MODSEL18–
P2-		35	TLDAT02–
1, 2	GND	36	MODSEL17–
3, 4	+5 MAIN	37	TLDAT03–
5	TLAG (OUT)	38	MODSEL16–
6	TLAG(IN)	39, 40	+12 MAIN
7	GND	41, 42	-12 MAIN
8	TLADR14–	43	TLDAT06–
9	TLADR15–	44	TLADR01–
10	TLADR10–	45	TLDAT07–
11	TLADR12–	46	INT4–
12	TLADR11–	47	TLADR06–
13	MODSEL23–	48	INT5–
14	OPEN	49	TLADR07–
15	TLADR13–	50	INT6–
16	MODSEL22–	51	TLADR02–
17	TLADR08–	52	INT7–
18	MODSEL21–	53	TLADR03–
19	TLADR09–	54	INT8–
20	TLDAT11–	55	TLADR00–
21	TLDAT08–	56	INT9–
22	MODSEL20–	57	TLADR04–
23	TLDAT10–	58	INT10–
24	INT3–	59	TLADR05–
25	TLADR18–	60	OPEN

Table 5-1. 990/5 System Interface Pin Out (Continued)

Pin	Function
P2-	
61	TLDAT04–
62	INT11–
63	TLDAT05–
64	INT12–
65	INT13–
66	INT14–
67	TLDAT00–
68	INT15–
69	TLDAT01–
70	SPARE
71, 72	-5 MEMORY
73, 74	+5 MEMORY
75, 76	+12 MEMORY
77, 78	+5 MAIN
79, 80	GND

Table 5-2. CRU Signals

Signature	CPU Pin	Description	
CRUBITOUT	P1-18	CRU data out from 990/5 board	
CRUBITIN	P1-60	CRU data into 990/5 board	
STORECLK–	P1-22	CRU data clock	
CRUBIT15	P1-34	CRU bit address 15	
CRUBIT14	P1-38	CRU bit address 14	
CRUBIT13	P1-32	CRU bit address 13	
CRUBIT12	P1-36	CRU bit address 12	
CRUBIT11	P1-70	CRU bit address 11	Used only by CRU Expander
CRUBIT10	P1-68	CRU bit address 10	
CRUBIT9	P1-64	CRU bit address 9	
CRUBIT8	P1-62	CRU bit address 8	
CRUBIT7	P1-50	CRU bit address 7	
CRUBIT6	P1-52	CRU bit address 6	
CRUBIT5	P1-54	CRU bit address 5	
CRUBIT4	P1-56	CRU bit address 4	

Table 5-2. CRU Signals (Continued)

Signature	CPU Pin	Description
MODSEL0–	P1-23	Module select for 1st 16 I/O
MODSEL1–	P1-35	Module select for 2nd 16 I/O
MODSEL2–	P1-37	Module select for 3rd 16 I/O
MODSEL3–	P1-43	Module select for 4th 16 I/O
MODSEL4–	P1-44	Module select for 5th 16 I/O
MODSEL5–	P1-45	Module select for 6th 16 I/O
MODSEL6–	P1-46	Module select for 7th 16 I/O
MODSEL7–	P1-47	Module select for 8th 16 I/O
MODSEL8–	P1-48	Module select for 9th 16 I/O
MODSEL9–	P1-49	Module select for 10th 16 I/O
MODSEL10–	P1-51	Module select for 11th 16 I/O
MODSEL11–	P1-53	Module select for 12th 16 I/O
MODSEL12–	P1-61	Module select for 13th 16 I/O
MODSEL13–	P1-67	Module select for 14th 16 I/O
MODSEL14–	P1-69	Module select for 15th 16 I/O
MODSEL15–	P1-76	Module select for 16th 16 I/O
MODSEL16–	P2-38	Module select for 17th 16 I/O
MODSEL17–	P2-36	Module select for 18th 16 I/O
MODSEL18–	P2-34	Module select for 19th 16 I/O
MODSEL19–	P2-32	Module select for 20th 16 I/O
MODSEL20–	P2-22	Module select for 21th 16 I/O
MODSEL21–	P2-18	Module select for 22nd 16 I/O
MODSEL22–	P2-16	Module select for 23rd 16 I/O
MODSEL23–	P2-13	Module select for 24th 16 I/O

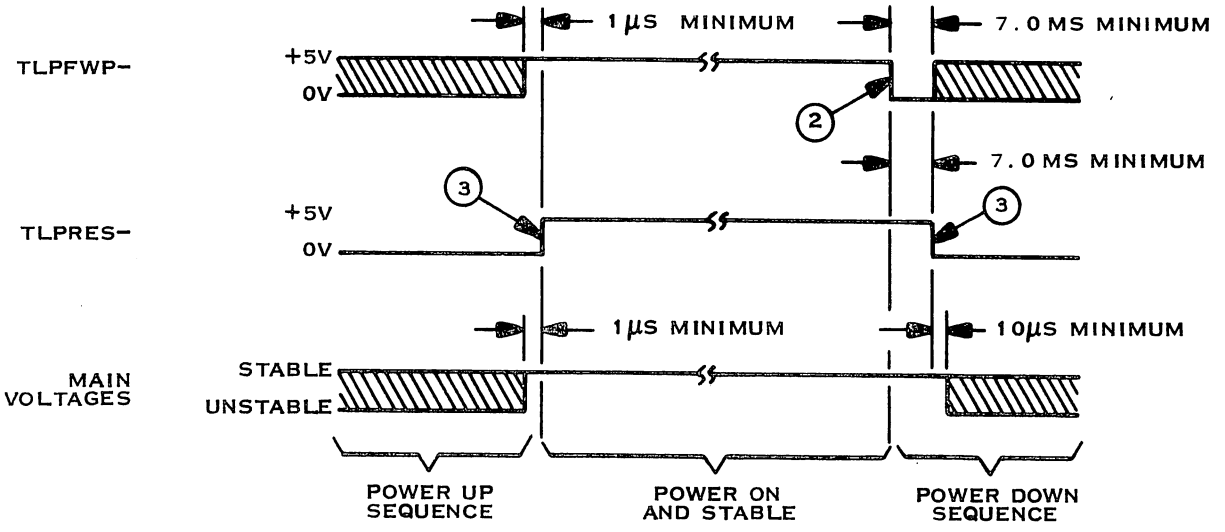
Table 5-3. 990/5 Interrupt Inputs

Signal	Pin No.	Function
INT00–	Not Available*	Power Up
INT01–	Not Available*	Power Fail Interrupt (Highest Priority)
INT02–	Not Available*	Error Interrupt
INT03–	P2 - 24	Host Processor or external interrupt (wired-OR)
INT04–	P2 - 46	External interrupt
INT05–	P2 - 48	Real Time Clock switch selectable to level 5, level 15 or OFF. Also available for external interrupt.
INT06–	P2 - 50	Port 3 interrupt-switched, or external interrupt.
INT07–	P2 - 52	External interrupt
INT08–	P2 - 54	Port 1 interrupt-switched, or external interrupt
INT09–	P2 - 56	External interrupt
INT10–	P2 - 58	External interrupt
INT11–	P2 - 62	External interrupt

Table 5-3. 990/5 Interrupt Inputs (Continued)

Signal	Pin No.	Function
INT12–	P2 - 64	External interrupt
INT13–	P2 - 65	External interrupt
INT14–	P2 - 66	Port 2 interrupt-switched, or external interrupt.
INT15–	P2 - 68	See INT05–. Also available for external interrupt.

*These interrupts are hardwired; not available for use by external circuits.



NOTES:
1. SHADED AREAS INDICATE UNDEFINED VOLTAGES.
2. THE FALL TIME OF TLPFWP– SHALL NOT EXCEED 50NS.
3. THE RISE AND FALL TIME OF TLPRES– SHALL NOT EXCEED 100NS. THERE SHALL BE NO OSCILLATIONS ON EITHER EDGE OF TLPRES–.

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Figure 5-1. Chassis Power Supply Timing

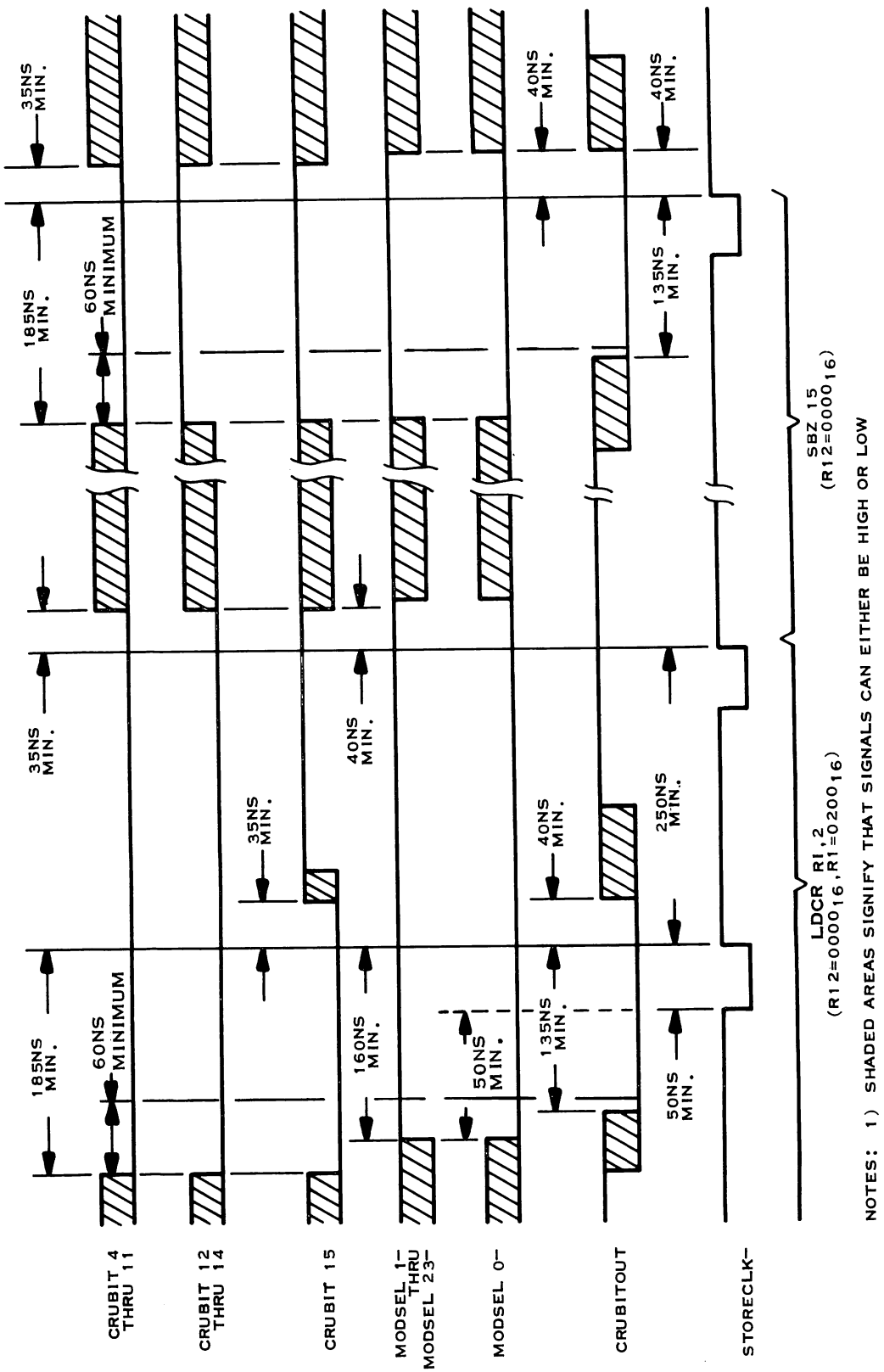


Figure 5-2. CRU Output Timing, Minimum Restrictions

5.2.3.3 Processor CRU Input Timing. The processor conforms to minimum CRU input timing restrictions as defined by figure 5-3 for CRU addresses 000_{16} to $17F_{16}$ and to the same minimum CRU input timing restrictions for CRU addresses from 200_{16} to FFF_{16} even though the delay between when the processor presents the CRU address and when the processor samples CRU data is increased by 250 nanoseconds for CRU expansion addresses 200_{16} to FFF_{16} to allow for propagation delay through the interconnecting cables. The figures show the timing sequences for STCR R1, 2 instruction followed by a TB 15 instruction. Minimum timing restrictions are the same for both instructions. CRU addresses and module selects are defined only during the execution of CRU input or CRU output instructions. CRUBITIN is defined only during the execution of CRU input instruction. The CRU device decodes the CRU address and places the appropriate data on the CRUBITIN line. The CRU module drives the CRUBITIN line with an open collector or three-state gate that is enabled only when that module is selected. Timing restrictions shown in figure 5-3 are based on a clock period of 250 nanoseconds.

5.2.4 TILINE INTERFACE. Table 5-4 lists the TILINE interface signals, description, logic conventions, and terminations.

5.2.4.1 Data Transfer Operations. There are 40 TILINE interface signals that are used exclusively for data transfer operations on the TILINE. As shown in table 5-4, 36 of these signals consist of the 20 address bits and 16 data bits with the remaining 4 signals used primarily for control of the actual data transfer operation. These four signals are: TLGO—, TLREAD, TLTM—, and TLMER—. All signals are transmitted and received between a TILINE master device and a TILINE slave device during a transfer of data. Both a read and write data transfer are described herein.

Timing for the TILINE master to slave write cycle is shown in figure 5-4 and is referenced in the following discussion. When a TILINE master device has access to the TILINE, it may accomplish a memory (slave) write cycle as follows. The master asserts TILINE GO (TLGO—) and at the same time asserts the write command, TILINE READ (TLREAD), by setting both signals low. The master at this time also generates valid write data on the data bus (TLDAT—) and a valid 20-bit address (TLADR—) on the address lines. All slave devices on the TILINE receive the TILINE GO transmitted by the master. The slave devices must decode the address to determine which slave is being addressed. The slave generates a delayed GO signal (using a timer circuit) and uses that signal to strobe for a valid address decode. In the case of a memory module, a delayed GO and a valid address decode generate a memory start signal. It is the responsibility of the slave device to delay GO for a time sufficient to accommodate the worst case address decode time and the worst case TILINE skew, with TILINE skew defined as 20 nanoseconds maximum. When the slave device has delayed GO and decoded the address as valid, it performs the write cycle and then asserts the TILINE TERMINATE (TLTM—). At the time the slave device asserts TLTM—, it must be finished with the TLDAT— TLADR—, and TLREAD signals from the TILINE. The action just described occurs during "time 1" as shown in figure 5-4. This time is defined as the slave access time and must be less than 1.5 microseconds for all TILINE slaves except the TILINE coupler. When the TILINE master receives the asserted TLTM—, it must release TLGO—, TLREAD, TLADR—, and TLDAT— within 120 nanoseconds. This occurs during "time 2" shown in figure 5-4. At this time the master device may relinquish the TILINE to another master device. When the slave receives the release of TLGO—, it must release TLTM— within 120 nanoseconds as shown in "time 3" of figure 5-4. When the master device receives the release of TLTM—, it may begin a new cycle if it has not relinquished the TILINE to another master device. This is shown as "time 4" in figure 5-4.

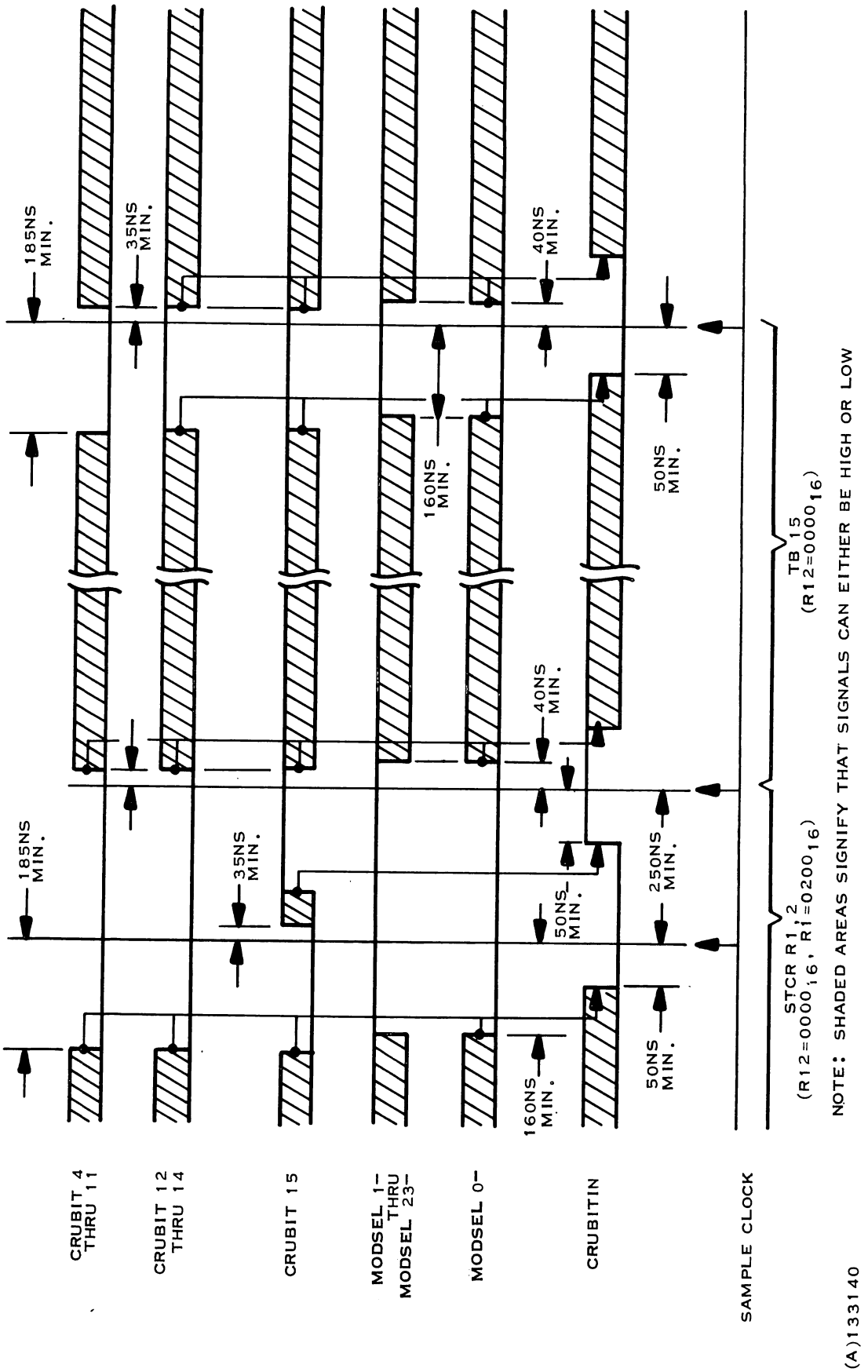


Figure 5-3. CRU Input Timing, Minimum Restrictions

Table 5-4. TILINE Signals

Signal	Description	Logic Convention*	Termination		Pin
TLAV	TILINE Available: From MASTER to MASTER	≥3.0 V: Available ≤0.9 V: Not Available	125Ω ← 3.75 V	In backplane	P1, 58
TLPRES–	Power Master Reset: From Power Supply to all other modules	≥2.0 V: Not Reset ≤0.8 V: Reset Asserted	270Ω ← 5.0 V	In power supply	P1, 13
TLPFWP–	Power Failure Warning Pulse: From Power Supply to all MASTERS	≥2.0 V: No Failure ≤0.8 V: Power Failure Warning	270Ω** ← 5.0 V	In power supply	P1, 16
TLIORES–	Input/Output Reset: From CPU to all other MASTERS	≥2.0 V: Not Reset ≤0.8 V: Reset Asserted	470Ω ← 5.0 V	At source in processor	P1, 14
TLWAIT–	TILINE Wait Signal: From TILINE	≥3.0 V: No Wait ≤1.0 V: Wait Asserted	125Ω ← 3.75 V	In backplane	P1, 63
TLHOLD–	TILINE HOLD Signal: From certain MASTERS	≥3.0 V: No Wait ≤1.0 V: Hold Asserted	125Ω ← 3.75 V	In backplane	P2, 26
GROUND	Signal and Power Ground				
TLGO–	Go: From MASTER to SLAVE, initiates a data transfer.	≥3.0 V: Not Asserted ≤1.0 V: Go Asserted	125Ω ← 3.75 V	In backplane	P1, 25
TLTM–	Terminate: From SLAVE to MASTER, completes a data transfer.	≥3.0 V: Not Asserted ≤1.0 V: Terminate Asserted	125Ω ← 3.75 V	In backplane	P1, 20

Table 5-4. TILINE Signals (Continued)

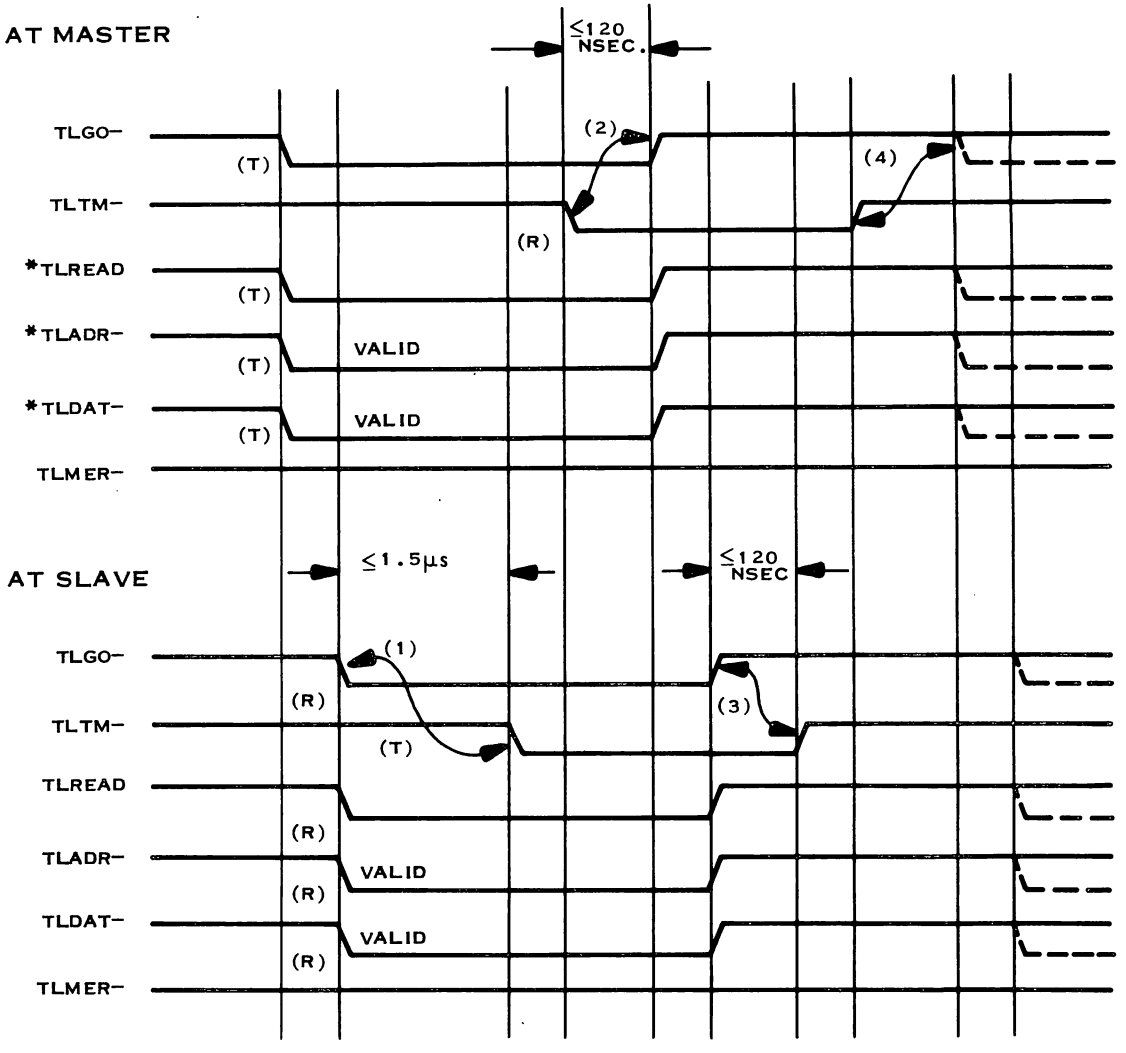
Signal		Description	Logic Convention*	Termination	Pin
TLADR00–	MSB	Address Lines: From MASTER to SLAVE	⩾2.0 V: Logic Zero	None	P2, 55
TLADR01–					P2, 44
TLADR02–					P2, 51
TLADR03–					P2, 53
TLADR04–					P2, 57
TLADR05–					P2, 59
TLADR06–					P2, 47
TLADR07–					P2, 49
TLADR08–					P2, 17
TLADR09–					P2, 19
TLADR10–					P2, 10
TLADR11–					P2, 12
TLADR12–					P2, 11
TLADR13–					P2, 15
TLADR14–					P2, 8
TLADR15–					P2, 9
TLADR16–					P2, 29
TLADR17–					P2, 27
TLADR18–					P2, 25
TLADR19–	LSB				P2, 31
TLDAT00–	MSB	Data Lines: From MASTER or SLAVE	⩾2.0 V: Logic Zero ⩽0.8 V: Logic One	None	P2, 67
TLDAT01–					P2, 69
TLDAT02–					P2, 35
TLDAT03–					P2, 37
TLDAT04–					P2, 61
TLDAT05–					P2, 63
TLDAT06–					P2, 43
TLDAT07–					P2, 45
TLDAT08–					P2, 21
TLDAT09–					P2, 33
TLDAT10–					P2, 23
TLDAT11–					P2, 20
TLDAT12–					P1, 27
TLDAT13–					P1, 28
TLDAT14–					P1, 30
TLDAT15–	LSB				P1, 31

Table 5-4. TILINE Signals (Continued)

Signal	Description	Logic Convention*	Termination		Pin
TLMER–	Memory Error: From SLAVE to MASTER	≥2.0 V: No Error ≤0.8 V: Error	470Ω ← 5.0 V	In backplane	P1, 55
TLREAD	Read Control: From MASTER to SLAVE	≥3.0 V: READ data from SLAVE ≤1.0 V: WRITE data to SLAVE	125Ω ← 3.75 V	In backplane	P1, 11
TLAG	TILINE Access Granted: From MASTER to MASTER establishes MASTER priority	≥2.0 V: Access Granted ≤0.8 V: Access Denied	1KΩ ← 5.0 V	At input in MASTER	P2, 6 (IN) P2, 5 (OUT)
TLAK–	Access Granted Acknowledge: From MASTER to MASTER	≥3.0 V: Not Asserted ≤1.0 V: Acknowledge Asserted	125Ω ← 3.75 V	In backplane	P1, 71

*The 2.0 V specification implies that the signal is to be interfaced using TTL gates. The 3.0 V specification means that driver/receiver circuits are required.

**270Ω for open-collector source, 1KΩ for totem-pole source.



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT.
(TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED
(R) = RECEIVED
*TLREAD, TLADR–, AND TLDAT– MUST BE STABLE AT THE TIME (OR BEFORE) TLGO– IS ASSERTED.

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Figure 5-4. TILINE Master to Slave Write Cycle Timing Diagram

Timing for the TILINE master-to-slave read cycle is as shown in figure 5-5 and is referenced in the following discussion. When a TILINE master device has access to the TILINE, it may accomplish a memory (slave) read cycle as follows. The master asserts TLGO— and at the same time generates a valid address signal (TLADR—) and TLREAD signal. All slave devices on the TILINE receive the TILINE GO transmitted by the master. The slave devices delay the GO signal and decode the address as is done for a write cycle. As in the write cycle, it is the responsibility of the slave device to delay GO for a time sufficient to accommodate the worst case TILINE skew (defined as 20 nanoseconds maximum) and worst case address decode time. When this has been done and the address is decoded as valid, the slave device begins to generate read data. In the case of a memory module this means starting a read cycle. When read data is valid, the slave device asserts TLTM— and at this time must have finished using TILINE signals TLADR— and TLREAD. If a read error is detected during a read cycle, the READ ERROR (TLMER—) signal is asserted by the slave. This signal must have the same timing that the read data would have had and this action occurs during "time 1" as shown in figure 5-5. "Time 1" is defined as the slave access time and must be less than 1.5 microseconds for all TILINE slaves except the TILINE coupler. When the master device receives the asserted TLTM—, it must delay at least for worst case TILINE skew (20 nanoseconds, maximum) and then release TLGO— and TLADR— signal lines. At the time the master device releases TLGO—, it must have finished using the TLDAT— and the TLMER— signals. This action occurs during "time 2" of figure 5-5 and must not require more than 120 nanoseconds. At this time the TILINE master device may relinquish the TILINE to another master device. When the slave device receives the release TLGO—, it must release TLTM— and TLDAT— signals. This action occurs during "time 3" as shown in figure 5-5 and must not be a greater time period than 120 nanoseconds. When the master device receives the released TLTM— it may begin a new cycle if it has not relinquished the TILINE to another master device. This is shown as "time 4" of figure 5-5.

5.2.4.2 Master Device TILINE Acquisition. The three TILINE signals, TILINE Access Granted (TLAG), TILINE Acknowledge (TLAK—), and TILINE Available (TLAV), are used by master devices to schedule the next TILINE master during the last data transfer operation of the present TILINE master. All TILINE master devices are connected to the TILINE is a positional priority system with that TILINE device installed into the highest numbered chassis slot receiving the highest priority. Priority ranking decreases with each chassis slot location toward that chassis slot occupied by the central processor, which has the lowest priority. Figure 5-6 illustrates the connections between TILINE master devices that establish the priority system. In the 990 chassis family backplane, TLAGIN is jumpered to TLAGOUT for all TILINE card slots except slot 7 which is, by convention, the slot used for the first TILINE master device controller. Additional TILINE master device controllers may be inserted in other TILINE card slots at higher or lower priority if the jumper between pins P2-5 and P2-6 is cut in the slot where the controller is installed.

The access controllers for each of the TILINE master devices are identical. A flowchart of the operation of the access controllers is provided in figure 5-7 and is referenced in the following discussion.

When a TILINE master device is inactive or reset, its access controller is in the IDLE state. In this state, TILINE Access Granted (TLAG) is passed on to lower priority master devices and the access controller monitors for a Set Device Access Request signal from the device.

As soon as the device generates a Set Device Access Request signal indicating that it wants to obtain TILINE access, the access controller changes from the IDLE state to the DEVICE ACCESS REQUEST (DAR) state.

In the DAR state the access controller monitors TILINE Access Granted (TLAGIN) and TILINE Acknowledge (TLAK). The access controller also disables TLAGOUT to the lower priority devices. After TLAGIN has been high for at least 100 nanoseconds and after the access controller has been in the DAR state for at least 100 nanoseconds, a high TLAK— causes the access controller to change to the DEVICE ACKNOWLEDGE (DAK) state.

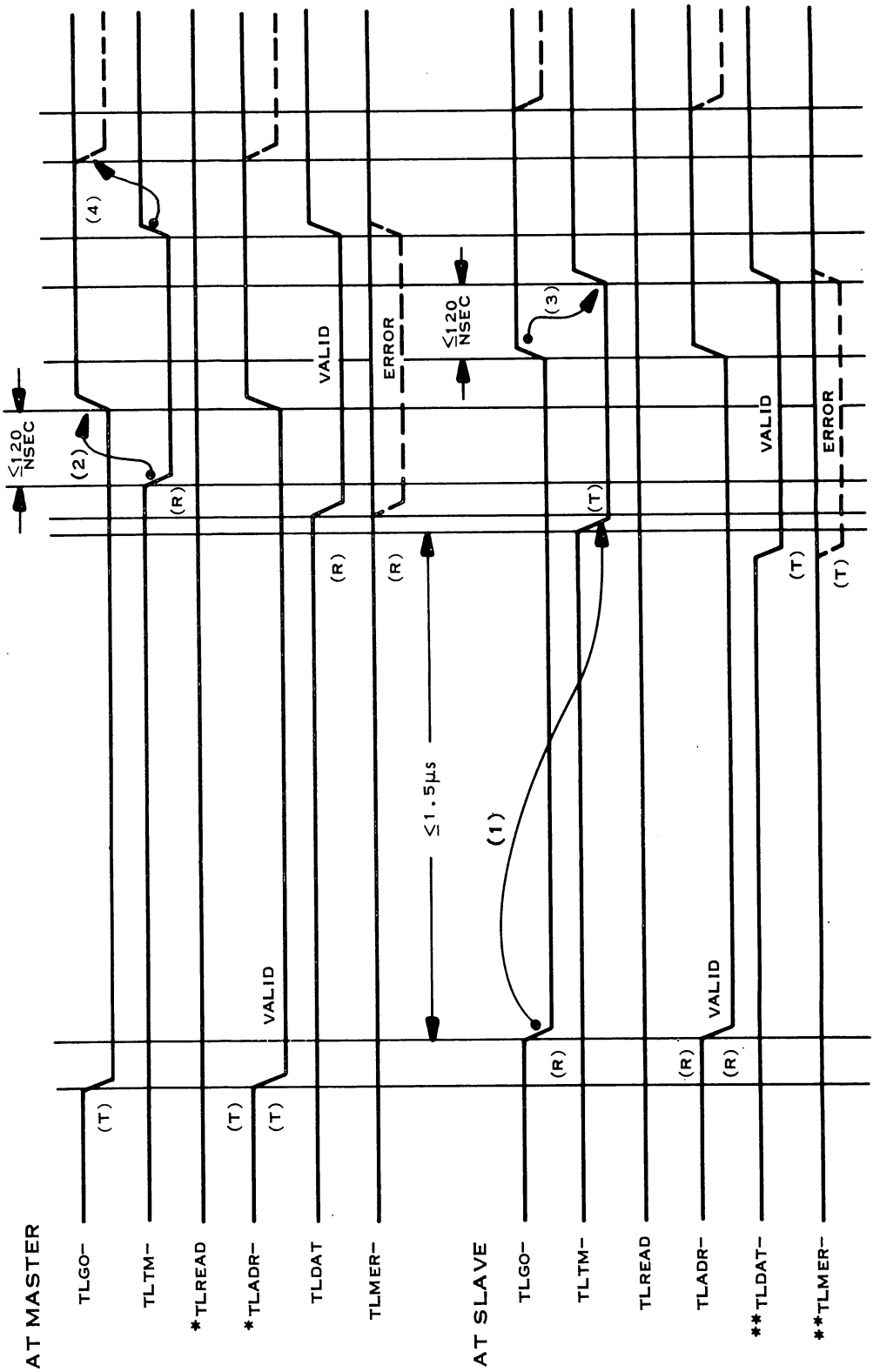

Figure 5-5. TILINE Master to Slave Read Cycle Timing Diagram

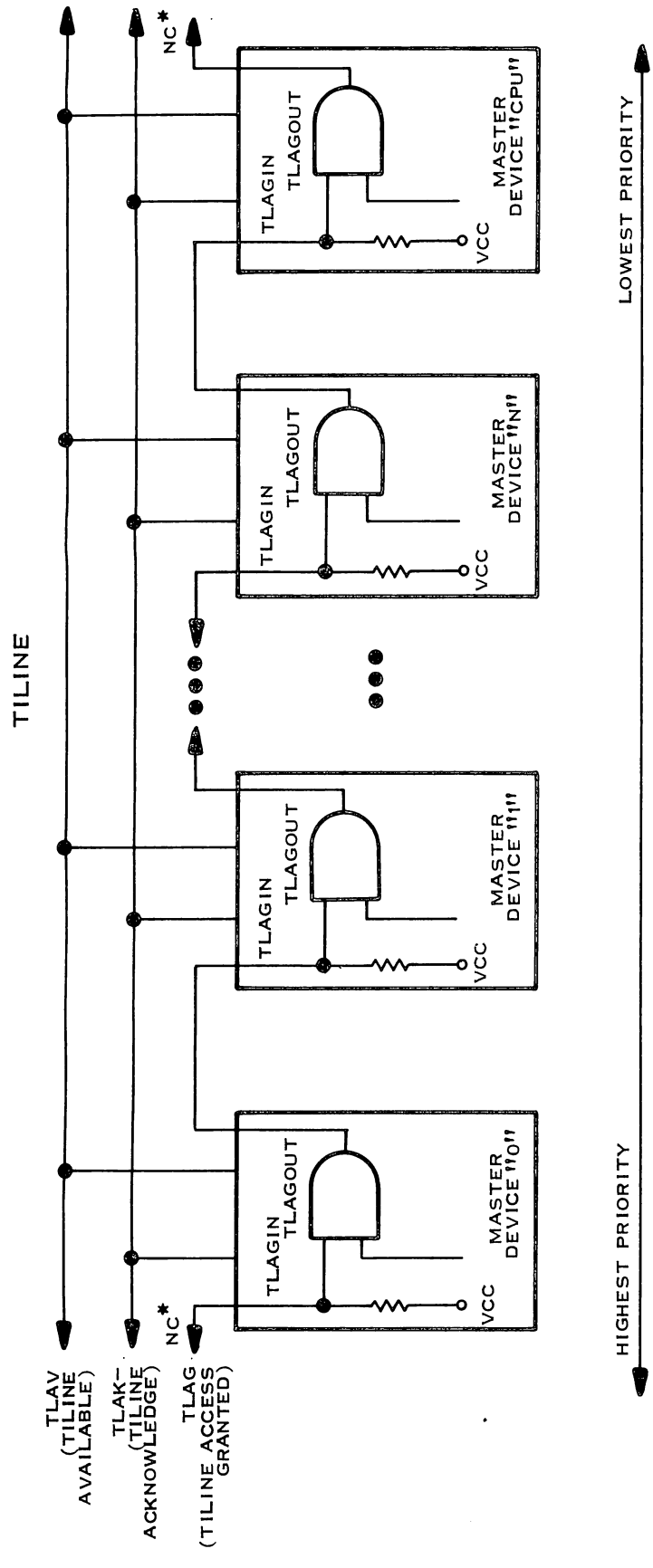

Figure 5-6. TILINE Master Devices Priority Interconnections

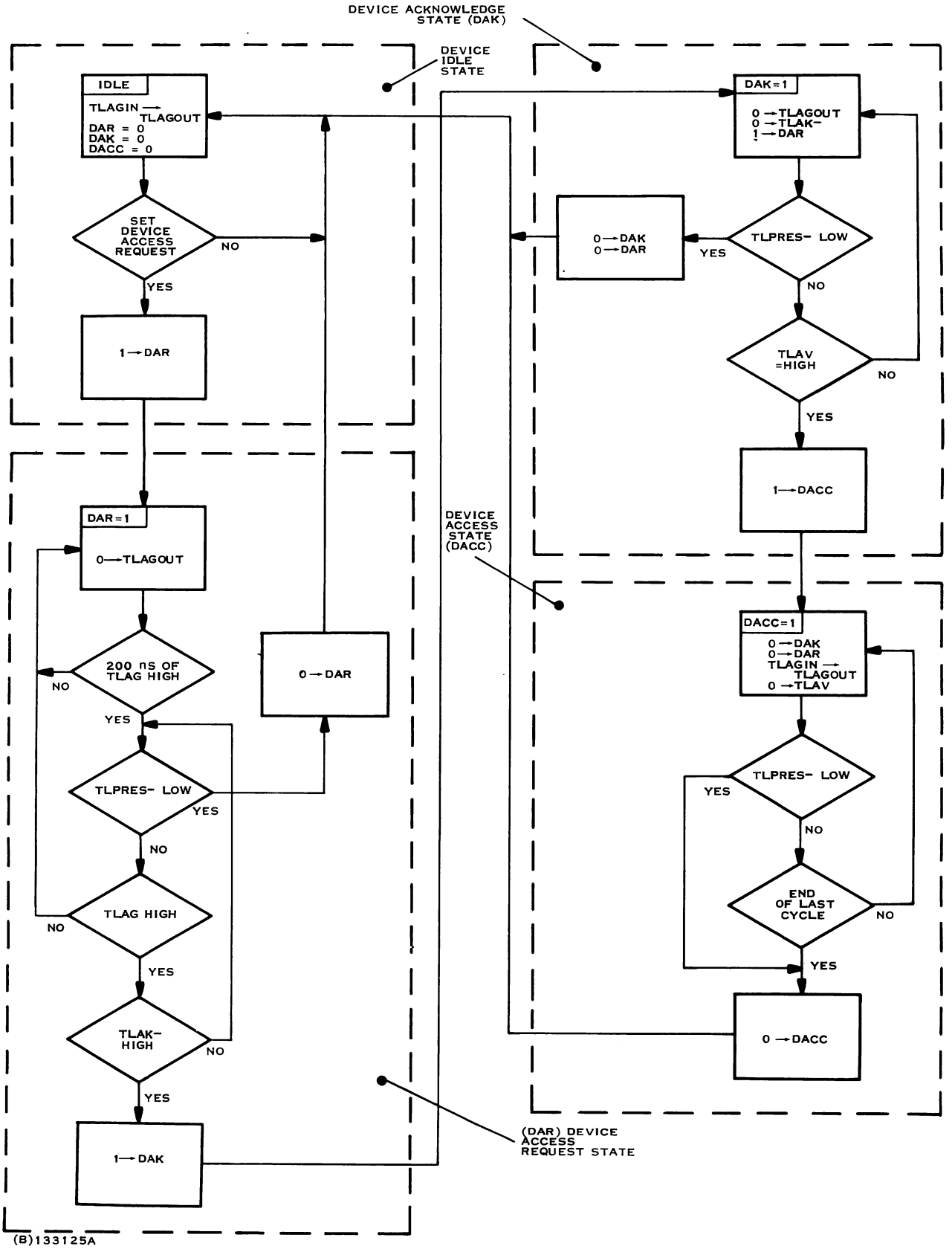

Figure 5-7. TILINE Master Device

In the DAK state the access controller continues to disable TLAG to lower priority master devices and pulls TILINE Acknowledge (TLAK—) low. In this state the access controller monitors TILINE Available (TLAV); and when TLAV is high, the access controller changes to the DEVICE ACCESS (DACC) state.

In the DACC state the TLAG signal is passed on to lower priority master devices and the access controller pulls TLAV low. While in the DACC state the master device has access to the TILINE and may perform data transfers as described previously under data transfers. During the last data transfer the master device performs, it must generate a Last Cycle signal that clears DACC and causes the access controller to return to the IDLE state at the end of the data transfer. Most TILINE device controllers are designed to steal only one TILINE cycle at a time, and the Last Cycle control is wired permanently high.

5.2.4.3 TILINE Special Purpose Functions. In addition to the TILINE signals associated with data transfers and those that establish priority for TILINE access, there are five special function signals. These signals are TILINE I/O Reset (TLIORES—), TILINE Power Failure Warning Pulse (TLPFWP—), TILINE Power Reset (TLPRES—), TILINE Wait (TLWAIT—), and TILINE Hold (TLHOLD—).

The TILINE I/O Reset (TLIORES—) signal is generated by the central processor during execution of its I/O Reset Instruction or in response to the programmer panel RESET switch. TLIORES— is a 100- to 500-nanosecond negative pulse on a normally high line. TLIORES— is also asserted whenever TLPRES— is asserted. TLPRES— is available to all devices connected to the TILINE.

TLIORES— functions to halt and reset all TILINE I/O devics. The devices should reset in an orderly fashion in response to TLIORES—, and any memory cycle in progress should be completed normally. For example, if a tape write is in progress, an end-of-record sequence should occur. When a device is reset while active it must report abnormal completion status.

The TILINE Power Failure Warning Pulse (TLPFWP—) signal is generated by the power supply to indicate that a power shutdown is imminent. This signal is a low pulse that occurs at least 7.0 milliseconds before TILINE Power Reset (TLPRES—) occurs. The negative-going edge of this pulse causes the central processor to trap to the power failure trap location, and the effect of the negative-going edge of TLPFWP— on connected TILINE I/O devices is the same as that of TLIORES—. TLPFWP— remains low until TILINE Power Reset is asserted.

The TILINE Power Reset (TLPRES—) is a normally high signal that goes low at least 10 microseconds before any dc voltage level from the power supply begins to fail due to normal shutdown or because of ac power failure. TLPRES— is generated by the power supply. TLPRES— remains low during and after a power failure. During ac power turn-on, TLPRES— remains at a low level until all dc voltages from the power supply are up and are stable. The purpose of TLPRES— is to reset all device controllers and the central processor during power failure and to directly inhibit all critical lines to external equipment that are powered by a separate power supply. For example, it is TLPRES— that prevents a tape deck from getting a rewind pulse when the central processor is powered up and down. During the power-up sequence, the TLPRES— resets all I/O controllers to their IDLE state and clears any device status information. As TLPRES— goes high, indicating that power is up and stable, the central processor performs the power-up interrupt trap.

The TILINE Wait (TLWAIT—) is a normally high signal, generated by TILINE couplers, that is used to resolve certain conflicts that can arise in computer-to-computer communication over the TILINE. The purpose of TLWAIT— is to directly disable (inhibit) the following signals from all TILINE master devices (including central processors): TLGO—, TLREAD, TLADR—, and TLDAT—. Note that these signals are not inhibited in slave devices. The foregoing signals are

disabled within 40 nanoseconds of the time that TLWAIT— is asserted and remain disabled as long as TLWAIT— stays low. This action should cause no state change in MASTER devices; and except for its TILINE interface drivers, the master device should be unaware that TLWAIT— has been asserted. TLWAIT— inhibits the master device from "seeing" any TILINE Terminate (TLTM—) or TILINE Memory Error (TLMER—) signals that occur and also holds the master devices TILINE timeout timer reset. TLWAIT— allows TILINE couplers to exercise a "higher than any" priority on the TILINE.

The TILINE Hold (TLHOLD—) is a normally high signal that is brought low by a central processor prior to the operand fetch of an ABS instruction. TLHOLD— remains low until the operand store cycle is complete or until the processor determines that the operand store is not needed. ABS is intended to be used as a software interlock. ABS reads a memory word, tests it, and then, if it was negative, subtracts it from zero, and restores it to memory in its original location. In the use of ABS as a software interlock in multiprocessor systems it is possible for one processor to modify a memory word while another processor is performing an ABS instruction on that word. This interference ruins the usefulness of ABS as a software interlock. The asserted TLHOLD— prevents this interference by holding TILINE access for the processor performing ABS. TLHOLD— is used and propagated by TILINE couplers in multiprocessor systems.

5.2.5 MISCELLANEOUS BACKPANEL SIGNALS. Signals listed in table 5-5 are also present at the 990/5 backpanel interface.

Power pins on backpanel connectors are as shown in table 5-6.

5.3 OPERATOR OR PROGRAMMER FRONT PANEL CONNECTOR, P3

The interface to the front panel is a 20-pin male connector. The operator front panel requires only four of the power/signal voltages, and the programmer front panel uses all of the power/signal voltages at connector P3. Table 5-7 lists the power/signal voltages at the front panel interface connector.

5.4 COMMUNICATIONS PORTS INTERFACES P4, P5, P6

There are three communications ports: two for asynchronous communications (P4 and P5) and one for synchronous/asynchronous communications (P6). The interface connectors, mounted on the front edge of the 990/5 board, are identical type D, RS232, 25-pin connectors. Signals and pin numbers for these connectors are listed in table 5-8. Signals and pin numbers for P4 and P5 are similar; P6 has additional pin numbers and signals. Pin numbers not identified are OPEN.

Table 5-5. Miscellaneous Backpanel Signals

Mnemonic	Pin	Function
120HZ	P1-29	Input from power supply. Line frequency oscillator for Real Time Clock signal.
IAQ–	P1-33	Output from TMS9900 microprocessor, indicates current memory read is an instruction fetch.
RESTART–	P2-28	Input (if connected) initiates a LOAD interrupt to TMS9900.

Table 5-6. Backpanel Power Pins

GND	P1-1, 2, 12, 15, 17, 19, 21, 24, 26, 57, 59, 72, 74, 79, 80, P2-1, 2, 7, 14, 30, 60, 79, 80
+5 MAIN	P1-3, 4, 77, 78; P2-3, 4, 77, 78
+5 MEMORY	P1-7, 8; P2-73, 74
+12 MAIN	P1-39, 40; P2-39, 40
+12 MEMORY	P1-5, 6; P2-75, 76
-5 MEMORY	P1-9, 10; P2-71, 72
-12 MAIN	P1-41, 42; P2-41, 42

Table 5-7. Front Panel Power/Signal Voltages

Mnemonic	Pin	Function
CRUBITIN	P3-7	Input to CRUBITIN bus from front panel.
CRUBITOUT	P3-15	Output to front panel from CRUBITOUT bus.
STORECLK–	P3-2	Write operation strobe (output) to front panel.
CRUBIT12	P3-19	Address bits to select a particular bit register in a read or write operation. Output to front panel.
CRUBIT13	P3-20	
CRUBIT14	P3-18	
CRUBIT15	P3-16	
MODSEL–	P3-14	Console select line to the front panel (module select), decoded address bits MA3– through MA10–.
IDLELED–	P3-11	Output to front panel; lights IDLE L.E.D. to indicate processor inactivity.
RUN–	P3-12	Output to front panel; lights the RUN L.E.D. to indicate processor is in the run mode.
RESTART–	P3-5	Input from front panel; generated when HALT/SIE pushbutton is pressed to indicate panel is in the active input mode.
FAULTLED–	P3-6	Output to front panel; lights FAULT L.E.D. when processor fails a test.
POWERLED–	P3-13	Output to front panel; lights POWER L.E.D. when keyswitch is turned to LOCK or UNLOCK position, indicating power is applied.

Table 5-7. Front Panel Power/Signal Voltages (Continued)

Mnemonic	Pin	Function
+5VMAIN	P3-9, 10	Supply voltage to front panel controls and indicators.
GROUND	P3-1, 3, 4, 17	Power return from front panel.

Table 5-8. Communications Interface Signals (P4, P5, and P6)

RS232		990/5					
Pin Number	RS 232 Mnemonic	P4	Port 1	P5	Port 2	P6	Port 3
2	XMTD (output)	2	XMTD1	2	XMTD2	2	XMTD3
3	RCVD (input)	3	RCVD1	3	RCVD2	3	RCVD3
4	RTS (output)	4	RTS1	4	RTS2	4	RTS3
5	CTS (input)	5	CTS1	5	CTS2	5	CTS3
6	DSR (input)	6	DSR1	6	DSR2	6	DSR3
7	GND (Signal Gnd)	7	GND	7	GND	7	GND
8	DCD (input)	–	– – –	–	– – –	8	DCD3
11	SECRTS (output)	–	– – –	–	– – –	11	SECRTS3
12	SECDCD (input)	–	– – –	–	– – –	12	SECDCD3
13	ALBK (output)	–	– – –	–	– – –	13	ALBK3
15	XCLKI (input)	–	– – –	–	– – –	15	XCLK3
17	RCLK (input)	–	– – –	–	– – –	17	RCLK3
19	SECRTS (output)	–	– – –	–	– – –	19	SECRTS3
20	DTR (output)	20	P1A2DTR	20	P1A2DTR	20	DTR3
22	RIND (input)	–	– – –	–	– – –	22	RIND3
24	XCLK0 (output)	–	– – –	–	– – –	24	XCLK3

Table 5-8. Communications Interface Signals (P4, P5, and P6) (Continued)

A brief description of communications mnemonics follows:

XMTD	Transmitted Data from 990/5
RCVD	Received Data to 990/5
RTS	Request to Send from 990/5
CTS	Clear to Send to 990/5
DSR	Data Set Ready to 990/5
GND	Signal Ground
DCD	Data Carrier Detect to 990/5
SECRTS	Secondary Request to Send from 990/5
SECDCD	Secondary Data Carrier Detect to 990/5
ALBK	Analog Loopback from 990/5
XCLKI	Transmit Clock In to 990/5
RCLK	Receive Clock to 990/5
DTR	Data Terminal Ready from 990/5
RIND	Ring Indicator to 990/5
XCLKO	Transmit Clock Out from 990/5

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

HOW TO USE THE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables. The table of contents does not contain four-level paragraph entries. Therefore, for four-level paragraph numbers such as 2.3.1.2, use the three-level number and the corresponding page number. In this case, the three-level number is 2.3.1.

INDEX ENTRIES

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

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The index is divided into sections for the letters of the alphabet. Acronyms and mnemonics (words made up entirely of capital letters) are listed first within each section. Words that begin with a capital letter follow the acronyms and mnemonics.

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