3.3 Hardware Description - Color Video Monitor

3.3.1 Introduction

The Technico color video interface board consists of several different circuits. First is the color video interface. This interface allows the user display on a video monitor or a television set (using an external RF modulator) either 64 characters by 16 lines or 32 characters by up to 28 lines. Each character may be an alpha-numeric or limited graphics character. The interface also provides eight different colors with eight different levels of intensity. Thus, there are 64 variations of color. The characters to be displayed are stored in 1K bytes of RAM on the board. The color and intensity for each character are stored in an additional 1K bytes of RAM. The video output from the color video circuit can be connected to an RF modulator and connected to the antenna input or any standard American TV. The character display and number of lines is selectable by jumpers on the board.

A second feature of the color interface board is 2K bytes of user RAM. This user RAM occupies the same memory space from 800 through FFF (hexidecimal) as the color video interface memory. To write or read from the user RAM, bit 20 of the CRU interface is set to 0. To write or read from the video interface memory, bit 20 is set to a 1.

Another circuit on the board provides an audio cassette interface to write or read data from a standard audio cassette at about 1000 bits/second. The commands for load and save are part of the video monitor.

A software controlled, hardware implemented, single step circuit is provided to allow the user to single step or trace a program during execution.

3.3.2 Theory of Operation

U1 (74LS04) and the crystal form the basic clock occilator for the color video interface board. The output of U1 (pin 4) is the 3.58 MHz reference frequency. The reference is connected to the clock input of U16 (74LS169 counter). The two counters, U16 and U73, will divide the reference frequency by 233. This is accomplished by preloading U16 and U73 with a 78 (hexidecimal) then allowing the counter to count up to FF (hexidecimal). Each time the RC outputs of U16 and U73 go low, U28 (pin 8) will also go low, thereby forcing the two counters to be parallel loaded with a 78 (hexidecimal). The output of the second counter (U78, pin 15) is inverted (by U77) to provide 15.36 KHz horizontal scan reference. This 15.36 KHz reference is used by the horizontal sync circuitry, and also drives the clock input of U34 (74LS393 counter). U34 is a dual 4 bit binary counter and divides the 15.36 KHz signal by 256. The output of this divide circuit (U34, pin 8) is a 60 Hz reference and is used by the vertical sync circuitry.

3.3.2.1 Vertical positioning and vertical synchronization circuit. Vertical positioning is accomplished by U33 (a dual one shot). On the rising edge of the 60 Hz reference signal, the vertical positioning one shot is forcing the Q output (U33, pin 13) to go high. This high is latched by U32 (74LS74 D-type flip-flop). As long as the D input of U32 is high, any horizontal sync pulse will clock a high to the Q output. The other section of U33, the vertical sync one shot, is triggered at the same time as the vertical positioning one shot, the vertical sync one shot provide a pulse to U47 (74LS05 open collector inverter). The output of this inverter is the vertical sync pulse and is connected to the base of Q2 through jumper V1. The /Q output of the vertical sync one shot (U33, pin 12) is connected to the set input on U32. Each time a vertical sync pulse occurs, the Q output of U32 (pin 5) is forced high. If the Q output of U32 is high, then U47, pin 10, will be low. This low will cause the CRT screen to be blanked during top retrace. The timing relationship between vertical sync pulses, a very narrow pulse, and vertical positioning pulses, is such that the

set input of U32 (pin 4) will be released long before the time out of the vertical positioning pulse on U32 (pin 2) 15.36 KHz horizontal sync to sense (via the D input of U32) where in the vertical direction of the screen the user wants to position the display. After the vertical position one shot (U33, pin 13) times out the D input of U32 (pin 2) will go low. Since the D input is low the next 15.36 KHz horizontal sync pulse low to high transition will cause the Q output of U32 (pin 5) will go low, thus releasing the blanking for the top retrace of the screen.

3.3.2.2 Horizontal sync.

The 15.36 KHz horizontal scan reference (U77, pin 6) triggers the horizontal sync one-shot (U48, pin 10 74LS123 one-shot). On each low to high transition of the of the horizontal scan reference, U48 will be triggered causing a positive going pulse on the Q output (pin 5). This pulse is inverted by U47 (74LS05) and is connected via jumper H1 to the base of Q2. On each transition of the horizontal sync pulse, the CRT trace will be forced to the left side of the screen.

3.3.2.3 Left margin adjust and dot clock oscillator.

The horizontal sync pulse (U48, pin 5) is connected to the left margin one-shot (U48, pin 2). This one-shot provides a left margin adjust and varies where the picture will start on the left side of the CRT screen. Each time the one-shot is triggered, the /Q output (U48, pin 4), will go low. When this occurs, U75, which is connected as a gated RC oscillator will be turned off. In addition, when the Q output (U48, pin 13) goes high, U4 (74LS393) will be reset. U75, (a 7400) is the dot clock oscillator. The adjustment R31 allows the user to select how many dots will appear within a given horizontal scan. The output of U75, pin 3, provides the clock for U4 (4-bit binary counter). This counter will allow 8 dot times to occur each time the /LOAD pulse is low (U2, pin 8). This will force the data shift register to be parallel loaded with 8 bits of information each time the dot clock has counted to 8.

3.3.2.4 Serial data circuit.

Each time the load pulse goes low, the data presented at the A-H inputs of U74 (74165 shift register) will be parallel loaded into the shift register. After the load pulse returns high, the dot clock will force the data loaded into the shift register to be shifted out one bit at a time (U74, pin 7). This data output is connected to the serial data input of U76, pin 1, (74LS86, on sheet 3 of 3). Depending upon the state of U76, pin 2 the data may or may not be inverted at this time. The inverting input U76, pin 2) is controlled by U46 (74LS74). U46 selects reverse video or standard video. This is accomplished by the state of signal RAMD7. If RAMD7 is high, a light background with dark characters is selected. If RAMD7 is low a dark background with light characters is selected. U46 is reloaded for each character by the load pulse. In the graphics mode, then U46 is held reset, therefore no inversion of the data will occur. The serial data is inverted by U47, and is then resistively coupled into the base of transistor Q2.

3.3.2.5 Blanking circuits.

U76, pin 6 provides blanking of the C RT screen during left (U76, pin 5) or right margins. If either LEFT or RIGHT is high, the picture on the screen will be blanked. Additionally, top blanking is provided by U47, pin 10 and bottom blanking is provided by U47, pin 6. U27 (74LS27) provides a signal called BUSY, anytime the CRT is not being blanked. Whenever BUSY is high, access to the CRT refresh memory can be inhibited to the processor. Anytime blanking is active (left margin, right margin, top or bottom) the output of U27 (pin 6) will go low indicating that the CRT refresh memory is not busy. The CRT refresh memory has dedicated data bus buffers (U41, U42, U43, U59, U60, U61). The read/write for these buffers is provided by U15 (74LS10). To read from the CRT refresh memory, the signals MEMEN, DBIN, and MUX = CPU have to be high. To write into the CRT refresh memory signal, MEMEN/DBIN and MUX = CPU must be high. Signals MEMEN and DBIN or/DBIN are provided by the 9900 CPU. Signal MUX = CPU is generated by the video board.

3.3.2.6 Color generator.

As indicated earlier, U1 (pin 4) is a 3.58 MHz reference oscillator. That oscillator is connected to a color video module (U66). This module provides gate delays, which will cause the reference frequency to be shifted in time with respect to the reference by each stage in the module. The outputs of the module are connected to the color multiplexer (U65, 74S251). Depending on the states of the A, B and C select inputs of U65, one of the 6 inputs from the module will be transferred to the Y output U65, pin 5). The output, called the colorburst, is connected to the base of Q4, a 3904 transistor. The output of the transistor is then subjected to a low pass filter R43, C14 and is coupled into the base of the output transistor Q2. The selection of which input of the color multiplexer is to be used is dependent upon the data that is stored in the CRT refresh memory. The color selection data in the CRT refresh memory, is latched into U63 (74LS174 latch) and then subsequently latched into U64 (74LS174 latch). This two stage latch is used to keep the color information timing synchronized with the characters that are displayed on the screen. The outputs of the second latch (U64, pins 10, 12, and 15) control which of the 8 inputs of the color multiplexer (U65) will be displayed for that particular character. U67 (74LS08) is used to provide a zero address to the color multiplexer (U65) at the beginning of each horizontal sweep. This provides the 3.58 MHz reference to the colorburst generator on the CRT so that it can synchronize itself and be ready to display color on that line. Transistors Q5, Q6, and Q7 provide intensity control for the selected color. Intensity is controlled on a character basis. By presenting a zero to the bases of any of the three transistors you can turn any one or all of them on. When any of the transistors turn on, Q8 turn on will be affected, and the emmitter voltage will decrease, thus varying the intensity of the color that is displayed on the screen.

3.3.2.7 CRT refresh memory.

The CRT refresh memory consists of four 2114 1K by 4 RAM chips (U21, U22,

U23, U24). The write enable for this memory is controlled by signal /MUX WE. Anytime this signal is low, data will then be written into the currently addressed memory location. The chip enable is controlled by signal /GMODE. Anytime this signal is low, the RAMs U21 and U22 will also be inhibited. This is intended for a future graphics option. The output of the CRT refresh memory is latched by U40 and U39, (74LS174's). Two of the outputs of U39 (pins 7 and 10) are connected to U38 (74LS139). Depending on the states of these two outputs, U38 will select any one of four modes of operation. If both bits are 0, then Y0 will be low and ROM 0 is selected. ROM 0 is the standard character generator. If the input is a 1 then Y1 will be low and USER ROM 1 is selected. If the input is a 2, USER ROM 2 is selected and if the input is 3, the graphics mode will be selected. Another output of U39 (pin 5) is signal RAMD 7. The state of this signal selects the standard video mode or the reverse video mode. The remaining output of U39 (pin 2) and all the output pins of U40 contain the information for the characters to be displayed during the current character time. If the standard character ROM is selected, this would be an ASCII character code.

3.3.2.8 Character generation.

On sheet 2 of 3, the three character generators are shown (U56, U57, U58). U56 can be a TMS4710 character generator or a 2708 EPROM that is programmed for the appropriate characters. Pin 20 is the chip select for each of these character generators. If /ROM0 is low then U56 will be enabled and the standard character generator selected. If /ROM1 or /ROM2 is low, then one of the two user character generators are selected. The character that is to be displayed is presented on the RAMD0 to RAMD6 inputs to the character generators. After the access time has occurred, the output of the character generator will be latched into the shift register via the parallel load. This data will then be clocked out serially.

3.3.2.9 Row and line counter.

Two counters (U20, 74LS393) form the row and line counter. A horizontal sync pulse clocks the first counter (U20, pin 13). On each transistion

from high to low, U20 will count up by one. The clear input of both counters (U20, pins 2 and 12) are controlled by the signal called by the signal called TOP. Whenever a retrace from bottom to top has occurred, the counters will be reset. To operate the system in a mode with 16 lines of data with 64 characters per line, jumpers G and H must be connected. To display 32 characters, jumpers J and H must be connected. Additionally, to provide blanking at the bottom of the screen, jumpers N and T must be inserted. Additional jumpers on the board are for the user to connect at his discretion. When jumpers H and G are connected, U20 (pins 11, 10, 9. and 8) form a 2, 4, 8, and 16 count output. When jumpers J and H are connected, U20 (pins 11, 10, 9, and 8) are the 4, 8, 16, and 32 count outputs. The user can tie these outputs into the AND gate U2 to determine the number of lines that will be displayed on the screen.

3.3.2.10 Character counter.

The character counter consists of U44, U4, U62, and U45. The character counter is clocked each time a /LOAD pulse occurs (U44, pin 3). U44 will divide the /LOAD by 2 (U44, pins 5 and 6). U4 (74LS393, dual 4 bit binary counter) provides CRT refresh address selection. To determine the number of characters that will be displayed on the screen, jumpers A, B and C must be inserted correctly. If 64 characters in width are desired, the jumper A must be connected to jumper B and jumper D to E. If 32 characters are desired, jumper C must be connected to jumper B and jumper E to jumper F.

3.3.2.11 The refresh memory address multiplexer.

U5, U6 and U7 (74LS157 dual 4 bit multiplexers) provide the address for CRT refresh memories. Depending on the state of the select line (pin 1) the address will either be selected from the processor address bus or from the character and line counter address. The select line is controlled by the gating of U27 (74LS27). If the CRT MEM signal is high, (U29, pins 9 and 10), then pin 13 or U27 will be low. If a

RAM select occurs, /RAM CE low, then pin 2 of U27 will be low. At this time, the output of U27 (pin 12) will be high forcing the output of U11 (pin 2) low. This will allow the microprocessor to write or read from the CRT refresh memory.

3.3.2.12 User RAM control.

The user has the option of writing or reading from the CRT refresh memory or the 2K bytes of user RAM on the video interface board. Both RAM memories are allotted address space from 800 to FFF (hexidecimal). U14 (74LS259) determines whether the user memory is to be accessed or the CRT refresh memory is to be accessed. To access the user memory set CRU bit 20 to a 0.

3.3.2.13 User RAM.

Four 2114 1K by 4 RAM chips are provided on the video interface board. This provides an additional 2K bytes of user RAM. One rule must be observed when writing programs that interface with the video interface board. Any program that will access the video interface must not be stored in addresses 800 to FFF. Programs in that area cannot turn off the user memory and turn on the CRT memory because the current character may be written, however when the CPU returns to access the user memory again, it will read the wrong data because the CRT memory is turned on. The video monitor is stored in (2) 2708 EPROM's (U71 and U72) on the CRT memory board.

3.3.2.14 Memory selection.

Memory or I/O selection is determined by the gating network consisting of the address bus buffers, (74LS367 U8, U9, and U10) and gates U25, U26, U29 and U12. Output pin 8 of U25 indicates an address selection from E800 to EFFF (hexidecimal). This is the address space allocated for the video monitor. Output U29, pin 3, provides enable for both the user RAM and the CRT refresh RAM. This is the enable from 800 through FFF (hexidecimal). U12 pin 12 provides enabling for CRU addresses between address 40 and 7E (bit 20 to 3F). U13 (74LS155 dual 1 of 4 bit decoder) selects the proper I/O group. Depending on the state

of CRU clock, we will be able to transfer data in and out of the video interface board CRU. The outputs COUT 0 and CIN 1 and CIN 0 enable different functions on the video interface board. COUT 0 allows the user to set the state the outputs of U14 (74259). CIN 0 allows the user to read data from a standard ASCII keyboard connected to J12. CIN 1 allows the user to read data either from the audio input circuitry or from the three switches S1, S2, or S3. The state of S1, S2, or S3 determines how the monitor will configure the display. If S1 and S2 are left open, then the configuration is 64 characters by 16 lines. If S2 is closed and S1 is open, then the configuration of the display is 32 by 32 lines. If S1 is open, S2 closed then the configuration of the display is 32 characters by 24 lines.

3.3.2.15 Audio cassette interface.

The audio cassette interface will operate at 1000 bits/second. U68 (OPAMP) will allow the toggling information from bit 21 of the CRU output to be smoothed into a sine-like wave and capactively coupled out through C3 to the audio input of a standard audio cassette. The audio cassette input circuit consists of U70 and U69 (OPAMPS). To read the information, the user simply monitors the state of bit 21 on the CRU interface. A sequence of sine waves on the input are rectified and translated to a single pulse.

3.3.2.16 Software controlled single step circuitry.

A software controlled single step circuit is provided for tracing program execution under software control. The reason for the hardware implementation of this single step circuit is to provide the user trace capability for programs that are located in RAM or ROM. The The operation of this circuit is simple. Bit 22 of the CRU output is toggled from a low to a high. This high is inverted by U30. U30, pin 1 will go low causing U31 and U32 (74LS74's) to be reset. When the user is ready to single step the system program will set bit 22 low causing U14, pin 6 to go low thereby releasing the reset on U32 and U31. The program will then toggle from low to high CRU bit 23. This will cause U31 to be clocked, therefore the Q output (pin5) will

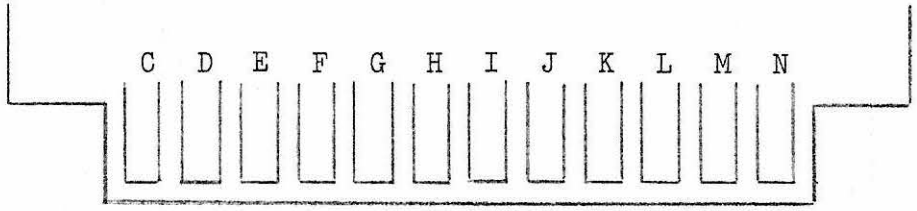
go high. This high is the D input of U31 (pin 12). When the program then executes an RTWP to return to the user program and IAQ , Instruction Aquistion, will occur. This instruction aquisition pulse will clock U31 (pin 11). At this time, the D input of U31 is high, therefore the Q output (pin 9) will go high. The D input of U32 (pin 12) will now be sitting high. The CPU will go out and fetch the user instruction. At the time of the instruction fetch, another IAQ will occur. This IAQ pulse will clock U32 (pin 11). Since the D input (pin 12) was high, the Q output (pin 9) will go high. This high will allow Q1 to be turned on, pulling the collector low. The collector of Q1 is tied to interrupt level 1. Prior to the next aquisition of an instruction the processor will be interrupted, which will take return control to the video monitor in the tracing program.

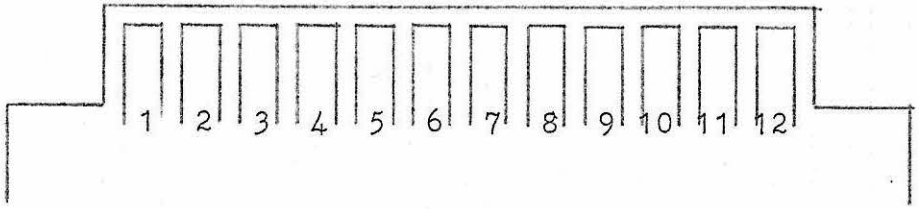
KEYTRONICS/COLOR VIDEO MODULE (T99CVM)
INTERFACE

J1

KEYTRONICS KEYBOARD

"KEY SIDE"

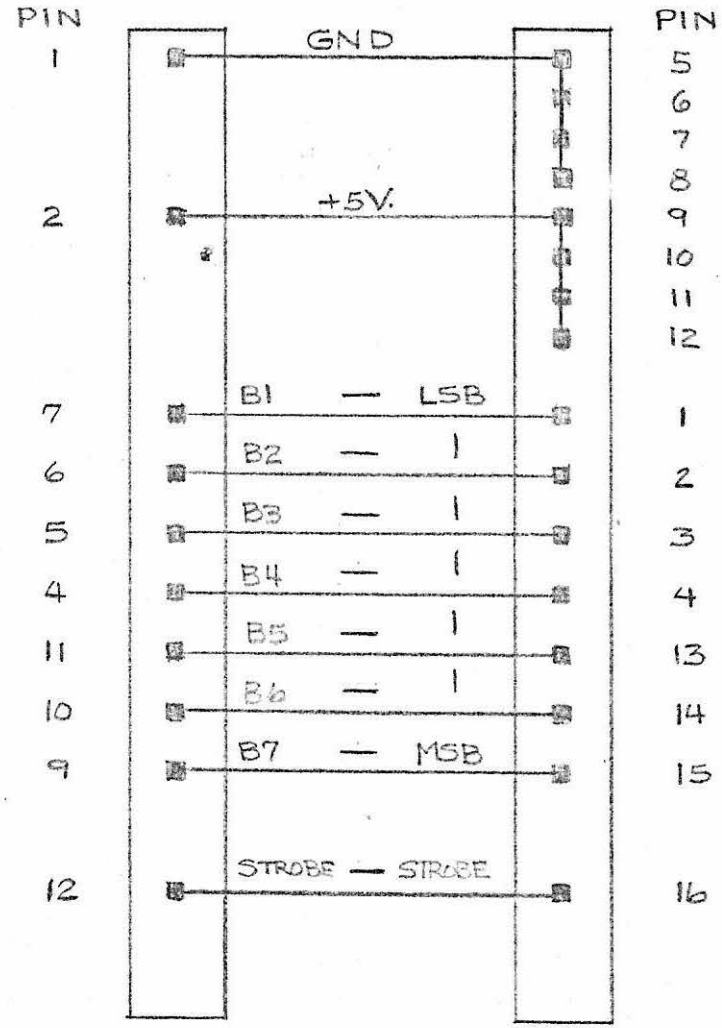




J1

KEYTRONICS KEYBOARD

"BOTTOM SIDE"



TECHNICO INCORPORATED

KEYTRONICS J1 CONNECTOR

T99CVM J12 CONNECTOR

TECHNICO T99CVM VIDEO AND
AUDIO INTERFACE