IBM

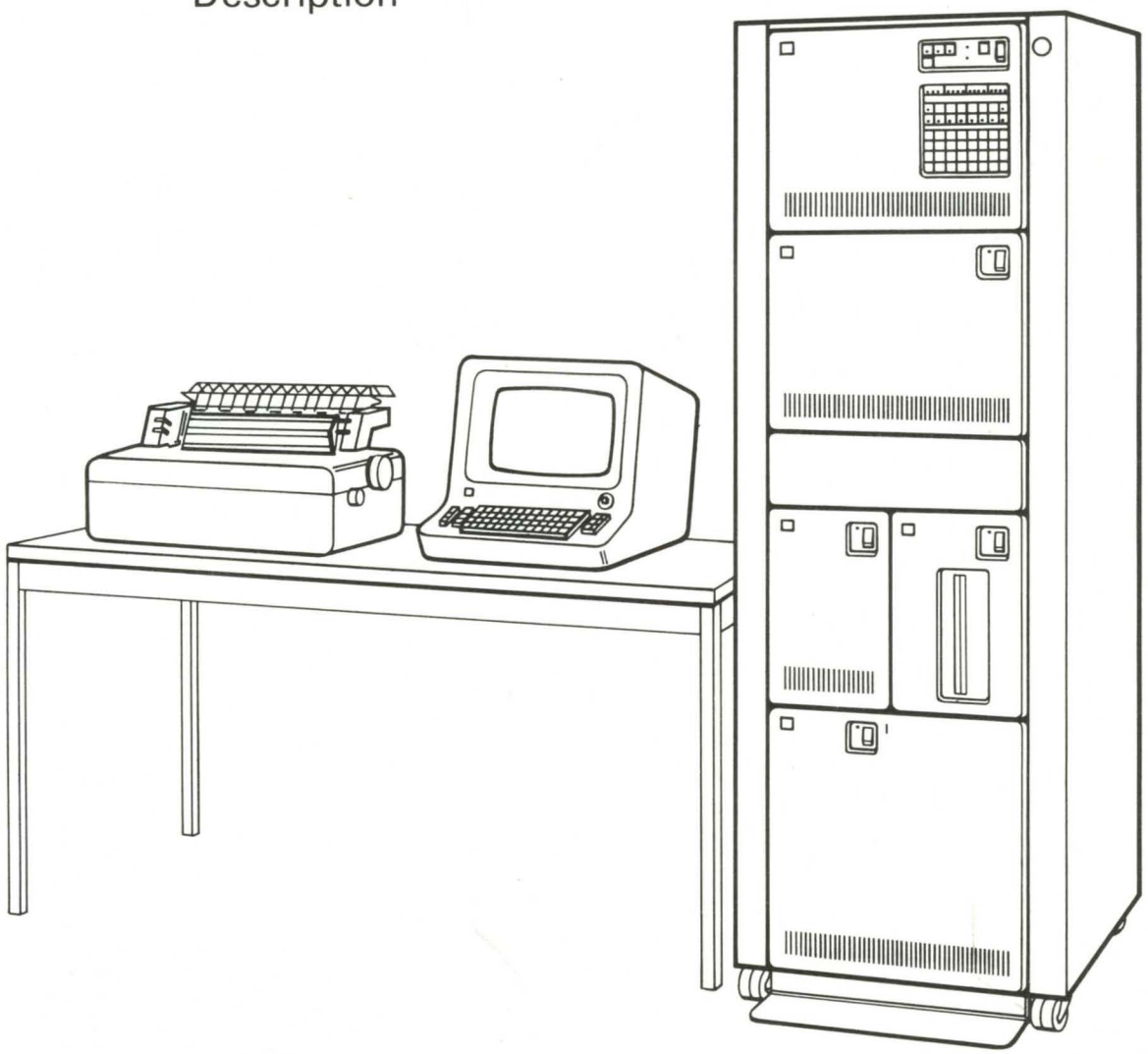
Series/1

GA34-0028-1

File No. S1-09

COMMUNICATIONS DESCRIPTION

IBM Series/1
Communications Features
Description



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Second Edition (March 1977)

This is a major revision of, and obsoletes GA34-0028-0. Significant changes in this new edition include:

1. Chapters 2, 3, and 4 have had descriptions of the jumperable options added.
2. A new appendix (Appendix C) has been added.
3. Technical corrections have been made. These changes are marked by a vertical bar to the left of the affected areas.

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Contents

Preface

This manual describes the functional characteristics of the IBM Series/1 communications features. It is assumed that the reader understands data processing terminology and is familiar with binary and hexadecimal numbering systems. This publication is intended primarily as a reference manual for experienced programmers who require machine code information to plan, correct, and modify programs written in assembler language.

PREREQUISITE PUBLICATIONS

- *IBM Series/1 Model 5, 4955 Processor and Processor Features Description,* GA34-0021; or *IBM Series/1 Model 3, 4953 Processor and Processor Features Description,* GA34-0022.
- *IBM Systems Reference Library: General Information–Binary Synchronous Communications,* GA27-3004.
- *IBM Synchronous Data Link Control General Information,* GA27-3093.

RELATED PUBLICATIONS

- *IBM Series/1 Installation Manual–Physical Planning,* GA34-0029.
- *IBM Series/1 Configurator,* GA34-0042.

SUMMARY OF PUBLICATION

Chapter one contains a general description of the three general types of communications features available for the Series/1. Chapter two–Asynchronous communications features. Chapter three–Binary Synchronous communications features. Chapter four–Synchronous data link control communications features.

Chapters two, three, and four are each divided into two sections. Section 1 contains descriptions of commands, immediate device control blocks (IDCBs), device control blocks (DCBs), operations, and status information. Section 2 contains information on error recovery and the use of the *Communications Indicator Panel* feature.

Appendix A contains a character code chart for ASCII, EBCDIC, Eight Bit Data Interchange, and PTTC codes. In addition to the code chart, Appendix A contains charts showing line control characters for the IBM 2740 and 2741, ASCII line control characters, sample BSC IPL sequence, and condition code charts.

Appendix B contains flowcharts of the various operations that can be performed by the asynchronous communications features.

Appendix C contains diagrams of various cables used to connect the communications features to modems or terminals.

Chapter 1. Introduction

The Series/1 communications features are designed to provide a variety of communications options. The features are the Synchronous Data Link Control Single-Line Control feature (abbreviated SDLC), the Binary Synchronous Communications feature (BSC), and the Asynchronous Communications Control feature (ACC).

All three features provide the capability to communicate with telecommunication terminals and host systems. Only the single-line BSC features are capable of receiving an Initial Program Load (IPL) from a host system.

SUMMARY DESCRIPTION

The features provide a variety of single-line and multiple-line telecommunications capability. In addition, there is a variety of line speeds, line configurations, clocking sources and data codes to choose from. All communications features described in this manual are cycle-stealing devices.

Communications Features

Asynchronous Communications Single-Line Control Feature

This feature provides circuitry for one half-duplex line. It can operate at speeds up to 9,600 BPS (bits per second). It can be used as either a *primary* station or a *secondary* station. The ACC makes no provisions for station-address recognition. Therefore, when ACC is used as a *secondary* station on a multipoint network, the software must provide the ability to recognize station-addresses. No IPL capability is provided.

Asynchronous Communications 8-Line Control and Asynchronous Communications 4-Line Adapter Features

A maximum of eight lines operating half-duplex may be controlled by these features. The bit-rate for each of these lines is a maximum of 2,400 bits per second.

Binary Synchronous Communications Single-Line Control Feature

This feature provides circuitry for one half-duplex, medium speed (up to 9,600 bits per second) line. It also provides the ability to IPL (initial program load) the processor from a host system. This feature can be used as either a *primary* (control) or *secondary* (tributary) station.

Binary Synchronous Communications Single-Line Control/ High Speed Feature

This feature provides circuitry for one half-duplex, high speed (up to 56,000 BPS) line. It also provides the ability to IPL the processor from a host system. This feature can be used as either a *primary* or *secondary* station. This feature is for use in leased-line applications only.

Binary Synchronous Communications 8-Line Control and Binary Synchronous Communications 4-Line Adapter Features

These features can control up to eight half-duplex communications lines at medium speeds. The maximum aggregate bit-rate possible through the 8-line control feature is 33,600 BPS. The ability to IPL from a host system is not provided on multiple-line BSC features.

Synchronous Data Link Control Single-Line Control Feature

This feature provides circuitry for one half-duplex line. This line can handle bit-rates up to 9,600 bits per second (BPS). The SDLC feature operates as a *primary* station or a *secondary* station but provides no IPL capability.

Interfaces

In all features except the high speed BSC, an EIA* RS232-C and CCITT (Consultive Committee on International Telephone and Telegraph) V.24 interface is provided for each line. The interface directly drives or terminates an external modem. The high speed BSC provides interfaces compatible with the Western Electric 303 Data Set (or equivalent), and CCITT recommendation V.35.

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* Electronic Industries Association
2001 Eye Street, N.W.
Washington, D.C. 20006

Types of Data Links

Each communications line can operate in one of three different types of data link. The data links are:

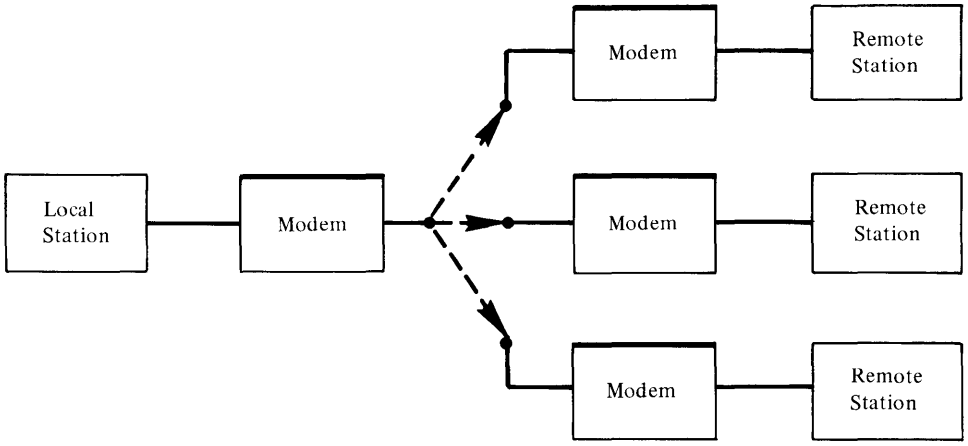
- Point-to-point—non-switched
- Point-to-point—switched
- Multipoint

A line is *point-to-point* when a local station is connected to a single remote station. Such a line is *non-switched* when there is a permanent connection between the local station and the remote station through their respective modems, or when the stations are directly connected.

* Modems not present when using direct connect cable with the ACC feature.

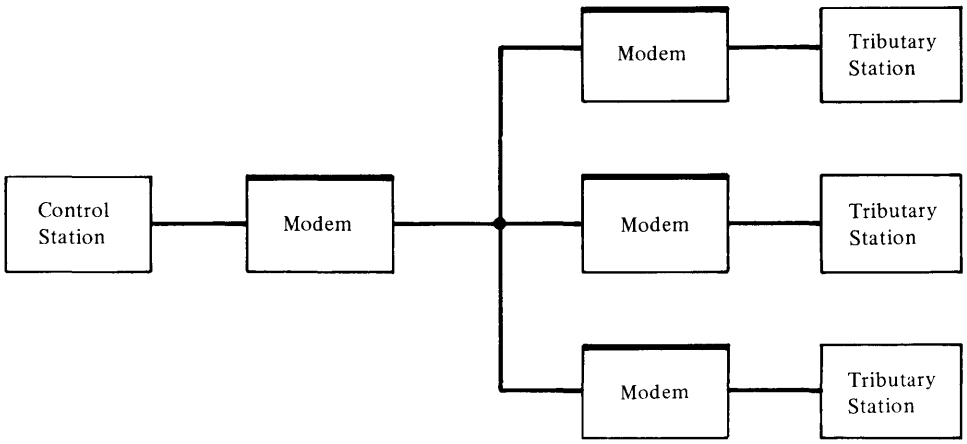
Point-to-point network-nonswitched

A point-to-point line can be *switched* so that one local station can communicate with *one* of several remote stations after a link has been established between the local station and the remote station. The connection is maintained only for the duration of the communication.



Point-to-point network-switched

The primary station in a *multipoint* data link is physically connected to several secondary stations through their respective modems. The primary station polls the secondary stations using unique station addresses. Only the addressed station can respond to the poll.



Multipoint network

Transmission Codes

The communications features can use a variety of transmission codes.

ACC Codes

The ACC features can use the following codes:

- PTTC/EBCD
- PTTC/Correspondence
- Eight Bit Data Interchange

BSC Codes

The BSC features can use the following codes:

- ASCII
- EBCDIC (transparency is standard)

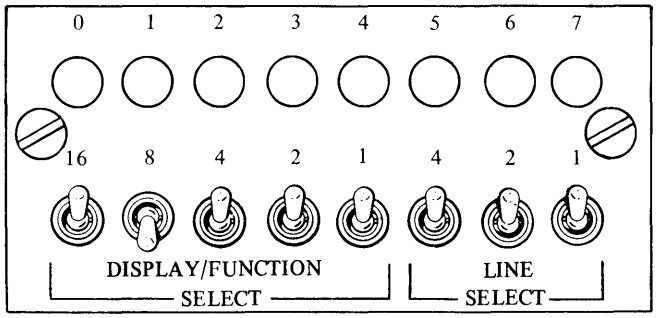
SDLC Codes

Full transparency is inherent in SDLC procedures. The SDLC feature can use *any* eight-bit code including the following codes:

- ASCII
- EBCDIC

COMMUNICATIONS INDICATOR PANEL

The Communications Indicator Panel is available as an option to the communications features. This panel provides a means of displaying various states, conditions, and lines. It also provides a means of manually resetting the 'data terminal ready' line to the modem.



The indicator panel may be used with any of the communications features one at a time. The panel's cable plugs into a connector on a feature control card, and the panel can be moved between processor units and I/O expansion units. Therefore, it is not necessary to have more than one indicator panel. The panel does not attach to the 4953 models A and C.

The indicator panel provides different information for each feature. Detailed information about the indicator panel is given in the chapter for each feature.

COMMUNICATIONS FACILITIES

The communications features can communicate with remote stations over private lines, leased common-carrier facilities, or switched voice-grade common-carrier lines.

The ACC, the SDLC, and the medium speed BSC interfaces conform to the Electronic Industries Association (EIA) standard RS232-C, and to the Consultive Committee on International Telephone and Telegraph (CCITT) recommendation V.24.

The high speed BSC provides the ability to select either an interface that is compatible with a Western Electric 303 (or equivalent) data set, or an interface that is compatible with CCITT recommendation V.35.

Some modems automatically disconnect when the communication feature's 'data terminal ready' (DTR) signal is deactivated. This signal can be deactivated by issuing a Start command with a "disable" operation specified in the DCB, or by using the communications indicator panel.

Chapter 2. Asynchronous Communications Control Features

Section One. Product Description

The Asynchronous Communications Control (ACC) features are optional features which control transfer of serial data to and from remote terminals or host systems via modems and communications line facilities. The ACC features allow the processor to communicate with telecommunications equipment using the start/stop method of data transfer. There are several important items to consider about the ACC features. They are:

- Data transmission is serial-by-bit, using the start/stop method of character and bit synchronization.
- The features can communicate with several different terminals using one of two transmission codes.
- The selection of a code is under program control.
- Line control characters are defined by the program.
- Bit rates from 37.5 to 9,600 bits per second (BPS) are controlled by programming. The multiple-line ACC feature can handle up to 2,400 BPS on all eight lines.
- The ACC features make no provision for station-address recognition. Therefore, when an ACC feature is used as a secondary station on a multipoint network, the software must provide the ability to recognize station-addresses.
- The processor cannot receive an initial program load (IPL) through the ACC features.
- The features provide answertone generation.

ACC FEATURE CONFIGURATIONS

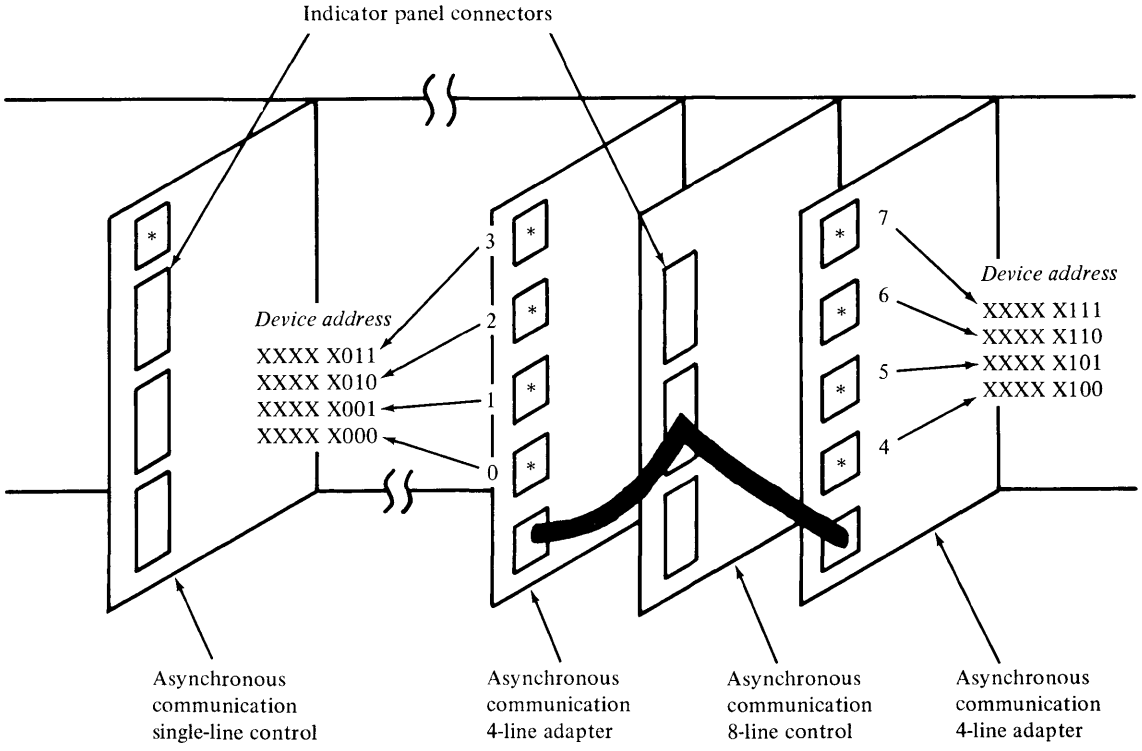
The Asynchronous Communication Control features are available in single-line and multiple-line configurations. The multiple-line configuration provides up to eight lines. The single-line ACC feature contains one card. The multiple-line configuration contains either two or three feature cards—two cards for one to four lines, three cards for five to eight lines.

Note. Throughout the remainder of this chapter, the term *attachment* is used as a general term to refer to either of the following:

1. The Asynchronous Communications Single-Line Control feature.
2. The Asynchronous Communications 8-Line Control feature and one or two Asynchronous Communications 4-Line Adapter features.

When referring specifically to item 1 above, the term *single-line attachment* is used. When referring specifically to item 2, the term *multiple-line attachment* is used.

Each line operates in a half-duplex mode. If desired, each line can be connected to a full-duplex modem to avoid modem turnaround times. If a line is connected to a full-duplex modem, the attachment still operates in half-duplex mode.



* Modem interface connectors

LINE CONTROL

A precise exchange of control characters between stations is necessary to establish and maintain teleprocessing communications. This exchange of control characters is called line control. One of its functions is to prevent two or more stations or terminals from attempting to use the line simultaneously (line contention).

Because each remote terminal may require different line control characters, the ACC attachments provide programmable line control characters. These characters are transferred to the attachment via the DCB (device control block). The DCB that transfers the control characters to the attachment is different from other DCBs. It is identified by bits 12–15 of the control word being set to 1101.

Control Characters

On a transmit operation (using PTTC code), the attachment compares characters coming from the processor with the programmed line control characters. On a receive operation, the attachment compares the characters being received with the programmed line control characters. All recognized control characters, that cause a change of direction (COD), cause the attachment to terminate the operation in progress with either a normal device end interrupt, a DCB command chaining operation, or an exception interrupt with ISB bit 0 on. All received control characters, except upshift and downshift, are placed in storage.

The attachment recognizes the control characters and acts on them as follows:

Eight Bit Data Interchange Code–Receive Mode

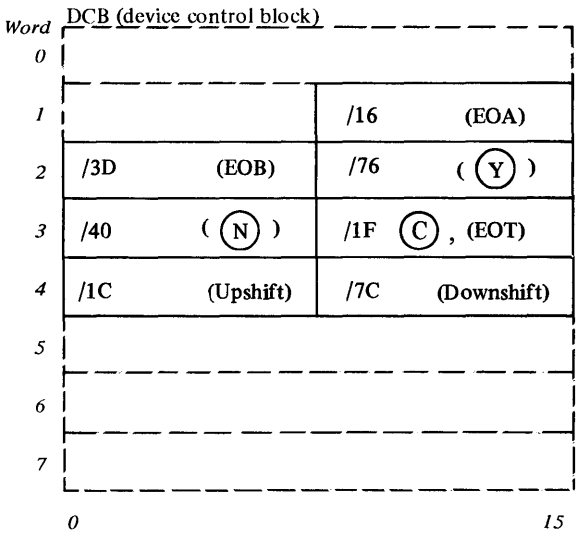
The attachment recognizes any of the seven characters defined in the DCB and treats them as COD characters. When any of the defined characters is received, the attachment presents a device end interrupt or begins a DCB command chaining operation (except when an *Incorrect Length Record** is detected).

Eight Bit Data Interchange Code–Transmit Mode

There is no control character recognition in transmit mode. All ending conditions must be controlled by byte count. A device end interrupt occurs when the byte count is decremented to zero.

PTTC Code–Receive Mode

When it is desired that the attachment operate in PTTC mode, the program should initiate a Set Control operation, specifying the control characters in the DCB as follows:



EOA — This is the low order byte of word 1 of the Set Control DCB.

When the first EOA character (end of address) is received, the attachment begins LRC (longitudinal redundancy check) character accumulation starting with the next character to be received. The EOA character is placed into storage.

EOB — This is the high order byte of word 2 of the Set Control DCB.

When this character (end of block) is received, the attachment compares the next character, which is the LRC character, with the LRC character generated by the attachment. If the LRC characters compare, the attachment terminates the operation with a normal device end interrupt or begins a DCB command chaining operation (except when an *Incorrect Length Record** is detected). If the LRC characters do not compare, or if there is a stop-bit error or VRC error, the attachment terminates the operation with an exception interrupt and sets ISB bit 0 "on," indicating that information as to the cause of the error is available to the program.

Note. The attachment makes no distinction between terminals that use record checking and terminals that do not use record checking. Therefore, the EOB must not be received when record checking is not used.

* See INTERRUPT STATUS BYTE.

COD 1
COD 2

These are: the low order byte of word 2 and the high order byte of word 3 in the Set Control DCB.

For PTTC code, one of these bytes should be loaded (by the program) with the positive acknowledgement character (Ⓨ) and the other byte should be loaded with the negative acknowledgement character (Ⓝ).

If the attachment is in Receive mode, it does not recognize any COD 1 or COD 2 character that occurs between an EOA and an EOT–the characters are simply treated as data. Receive mode is used for receiving data. Receive Response mode is used after a transmit operation to allow recognition of the positive or negative response from the station that received the data. Receive Response is only used where record checking is being performed. If the attachment is in Receive Response mode, it recognizes the COD 1 and COD 2 characters at any time. When the attachment recognizes a COD 1 or COD 2, it places the character in main storage and presents a device end interrupt (except when an *Incorrect Length Record** is detected). The program then must examine the character in storage and determine the appropriate action.

COD 3

This is the low order byte of word 3 in the Set Control DCB.

For PTTC code, this byte should be loaded (by the program) with the Ⓒ (EOT) character. When the defined character is recognized, the attachment terminates the operation with a device end interrupt or begins a DCB command chaining operation (except when an *Incorrect Length Record** is detected).

Upshift

This is the high order byte of word 4 in the Set Control DCB.

For PTTC code the program should load the value 1C (hexadecimal) into this byte. When this character is recognized, the character itself is not placed in storage. The attachment places subsequent characters into storage with the high order bit of each byte on, until a downshift or COD character is received, or until the attachment is reset.

Downshift

This is the low order byte of word 4 in the Set Control DCB.

For PTTC code the program should load the value 7C (hexadecimal) into this byte. When this character is recognized, the character itself is not placed in storage. The attachment places subsequent characters into storage with the high order bit of each byte off, until an upshift character is received. All receive operations begin in lower case.

PTTC Code–Transmit Mode

In this mode all normal ending conditions must be controlled by the byte count.

EOA

This is the low order byte of word 1 in the Set Control DCB.

When this character (end of address) is recognized, the attachment begins LRC accumulation starting with the next character transmitted. Any characters with the same bit configuration as the EOA, occurring between the first EOA and the COD 3 character, are treated as data.

EOB

This is the high order byte of word 2 in the Set Control DCB.

When this character (end of block) is recognized, the attachment transmits the EOB and follows it with the LRC. If the byte count is zero when the EOB is transmitted, the attachment presents a device end interrupt or begins a DCB command chaining operation. If the byte count is not zero, the attachment terminates the operation with an exception interrupt and sets bit 0 on in the ISB and bit 4 on in *cycle steal status word one.*

Note. The attachment makes no distinction between terminals with record checking and terminals without record checking. Therefore, the EOB must not be transmited when record checking is not used.

COD 1
COD 2

These are: the low order byte of word 2 and the high order byte of word 3 in the Set Control DCB.

Any COD 1 or COD 2 character coming from storage is simply transmitted as data.

COD 3

This is the low order byte of word 3 in the Set Control DCB.

In transmit mode, when the attachment recognizes this character, it is again able to recognize the EOA character as an EOA.

Upshift
Downshift

These are: the high order byte and the low order byte of word 4 in the Set Control DCB.

On outgoing data, the shift bit (bit 0 of each byte) is noted and removed from each character. A change in the shift bit causes the appropriate shift character to be inserted into the data stream before the data character is sent.

Note. The attachment does not recognize the shift characters as they come from storage so it does not update the shift mode unless the shift bit accompanying the shift character indicates a change. If the bit changes the current case, two shift characters are transmitted.

* See INTERRUPT STATUS BYTE.

TRANSMISSION CODES

The ACC attachments can serve as control stations to a variety of terminals by using one of the following codes:

- PTTC/EBCD
- PTTC/Correspondence Code
- Eight Bit Data Interchange Code

Line control depends on the requirements of the terminal. For detailed descriptions of terminal line control, consult the technical manual for the terminal.

PTTC Codes for 2740 and 2741

Character Set

The IBM 2740 Models 1 and 2 and the IBM 2741 use two versions of PTTC code. They are PTTC/EBCD code and PTTC/Correspondence code. These codes are similar, but they have some differences in character structure and line control usage. The codes are shown in Appendix A.

Line Control Characters

The line control characters used by the 2740/2741 are shown in Appendix A.

Eight Bit Data Interchange Code

Eight Bit Data Interchange Code is essentially a mirror image of eight bit ASCII. Therefore, the ACC features may communicate with terminals that use 8 bit ASCII code (such as Teletype ASR 33 and ASR 35). These terminals, however, must transmit two stop bits to preclude stop-bit errors in the attachment.

Character Set

The character set for Eight Bit Data Interchange Code is shown in Appendix A.

Line Control Characters

The line control characters for Eight Bit Data Interchange Code are shown in Appendix A.

DATA FLOW

With the exception of the upshift/downshift bit, valid data is placed in storage as it is received. Data received containing bad parity or a stop-bit error is replaced in storage with hexadecimal 00. Data is transmitted exactly as it comes from storage. Therefore, data must be organized in the exact bit configuration required by the code being used and in the sequence in which it is to be transmitted. Figure 2-1 illustrates the relationship between (1) bits in storage, (2) the various transmission codes, and (3) the attachment's storage data register.

Note. ACC attachments transmit by sending out the high order bit of the high order byte first. The received characters are stored in the same manner—the first bit received is the high order bit of the high order byte. If the data address (DCB word 7) is odd, only one character will be moved in or out of storage on the first data transfer.

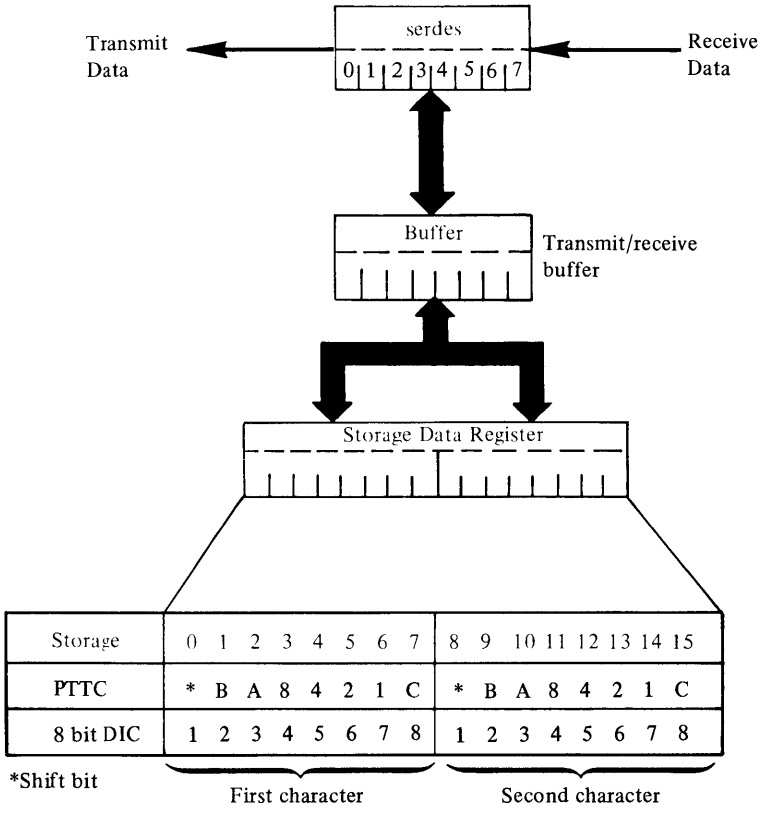


Figure 2-1. ACC feature data flow

LINE ERROR CHECKING

The attachment performs error checks on received data. The type of terminal being communicated with and the code being used determine the type of checking used. LRC (longitudinal redundancy check) and VRC (vertical redundancy check) are provided by the attachment for PTTC code only. LRC is performed when the attachment recognizes an EOB character. The LRC is generated without regard to parity.

If parity checking is required for eight bit data interchange code, the checking must be done by the program.

The attachment also checks each received character for proper stop-bit(s).

TIMEOUTS

The attachment has two programmable timers (timer 1 and timer 2). Each timer is controlled by a 16 bit word in the DCB. Both timers are decremented independently at a rate of 3.33 milliseconds per count. The maximum time that either timer can count is 218.4 seconds. The timers operate by decrementing a count (hexadecimal FFFF to 0001) supplied by the program. When the number is decremented to 0000, the attachment begins or terminates an operation. The timers are used with various operations, defined in the control word of the DCB, as shown below.

Timer 1

- Receive timeout (see 'Receive with Timeout' under 'Operations'–later in this chapter)
- Answertone/Break
- Transmit delay
  - Slows down turnaround time (pre-transmit delay)
  - Allows last character to exit modem before dropping RTS (post-transmit delay)
- Carrier detect timeout

Timer 2

- Program delay
- Clear to send timeout
- Data set ready timeout
- Ring indicator timeout
- DTR Disable delay

For detailed information on the use of the timers with particular operations, see 'Device Control Block' (DCB) later in this chapter.

OPERATING MODES

The attachment can operate in transmit, receive or receive response modes. The modes are selected by several different operations, as explained later under the DCB control word.

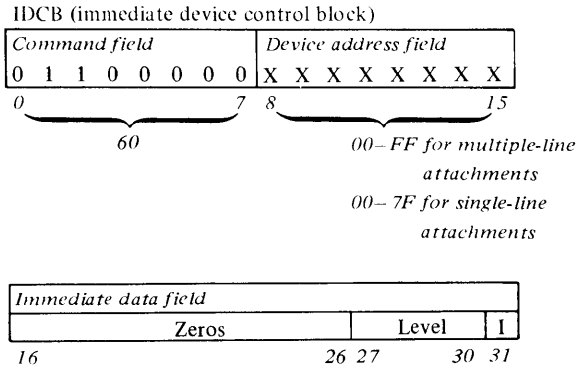
COMMANDS

The Operate I/O instruction points to the IDCB which contains one of the following commands.

- Prepare
- Device Reset
- Start
- Start Cycle Steal Status
- Read ID
- Start Diagnostic 1 or 2
- Start Control

Prepare

The *Prepare* command is used to control the interrupt parameters of the addressed device. The data word contains the level and I-bit. The single-line attachment is always able to accept and execute a *Prepare* command, even if it is busy or has an interrupt pending from a previous command. On a multiple-line attachment, the device returns a condition code 1 (CC1) to this command if it has an interrupt pending, and the I-bit in the IDCB is off. The IDCB for the *Prepare* command has the following format:



Level. This four bit field specifies the priority interrupt level assigned to the device. The binary value of bits 27 through 30 indicates priority levels of 0–3.

Example:

0000 = level 0, 0001 = level 1,
0010 = level 2, 0011 = level 3.

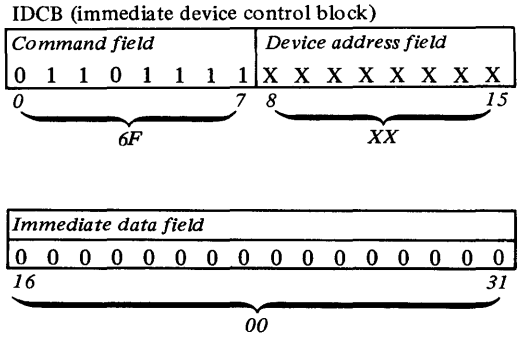
A prepare command issued to any device on a multiple-line attachment prepares *all* of the devices in the attachment to the same level. The I-bit information, however, applies only to the specific device addressed.

I. This bit determines whether the device is allowed to request an interrupt. An I-bit value of 1 permits the device to request an interrupt, and a value of 0 prevents the device from interrupting.

The prepared attachment stores the level data and presents it to the processor each time an enabled device presents an interrupt request. This data is reset on a system reset, a power-on reset, or changed by the successful execution of another *Prepare* command to the attachment.

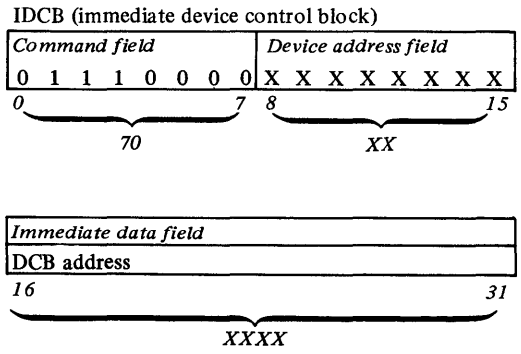
Device Reset

This command resets the addressed device and clears any pending interrupts (except *controller end*). The prepare information (including the I-bit) does not change. Also, the information stored in the device by a Set Control operation does not change. The IDCB for the Device Reset command has the following format:



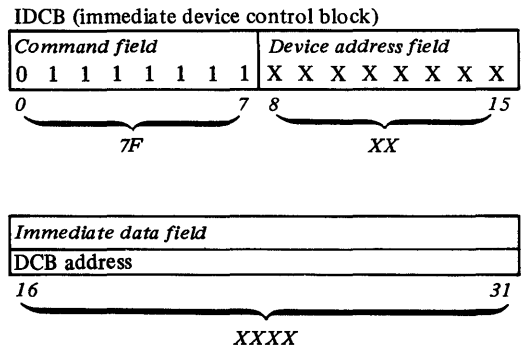
Start

This command initiates a cycle-stealing operating in the addressed device. The format of the IDCB for the *Start* command is:



Start Cycle Steal Status

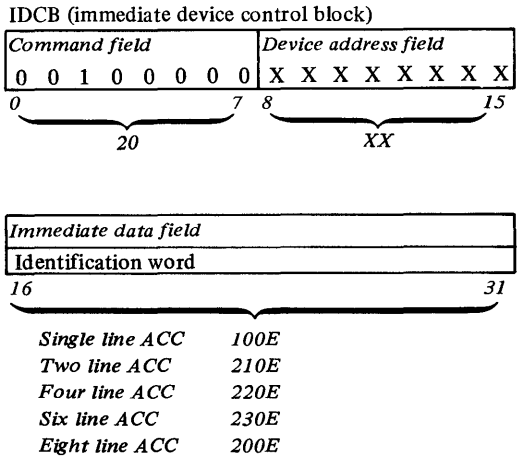
This command initiates a cycle-stealing operation in the addressed device for the purpose of collecting status information relative to the previous cycle-stealing operation. The format for this command is:



See 'Cycle Steal Status Words' for a description of the information transferred to storage by this command.

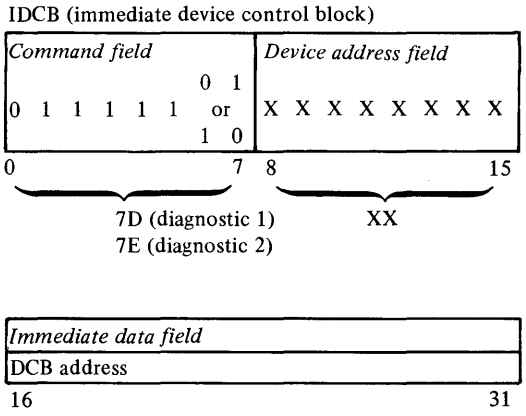
Read ID

This command puts the attachment's identification word (ID) into the data word position of the IDCB. The ID word contains physical information about the attachment that is used to tabulate the system's configuration. The Read ID command is generally used in diagnostic programming.



Diagnostic Commands

There are two diagnostic commands. They are used by diagnostic programs to determine if the attachment is operating properly. These commands are called *Start Diagnostic 1* and *Start Diagnostic 2.* For a full explanation of these commands, refer to chapter 5 of *IBM Series/1 4955 Processor–Theory Diagrams*, SY34-0041; or *IBM Series/1 4953 Processor–Theory Diagrams*, SY34-0042.



Start Control

This command is reserved for use by IBM engineering.

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	1	1	1	0	0	X	X	X	X	X	X	X	X
0							7	8							15
7C								XX							

Immediate data field
DCB address
16 31

Accidental issuance of this command may result in the attachment becoming inoperable. If this happens, the attachment can only be restored to operation by turning power off, then on again.

DEVICE CONTROL BLOCK (DCB)

The DCB is an eight word area in main storage which describes the specific parameters of the cycle-stealing operation. Its location in storage is assigned by the program. The DCB address transferred to the attachment via the IDCB points to word 0. The address of the DCB must be even. If the DCB address is odd, the attachment sets ISB bit 1 on and terminates the cycle-steal operation with an exception interrupt. The data in the DCB is loaded and changed by the program. The DCB is fetched by the attachment, using a cycle-steal address key of zero, after successful execution of a *Start* command, or a *Start Cycle Steal Status* command. The format of the DCB for a *Start Cycle Steal Status* command is different from the DCB for a *Start* command.

DCB (device control block)

Word		
0	Control word	
1	Bit rate constant*	Line control character*
2	Line control character*	Line control character*
	Timer 1	
3	Line control character*	Line control character*
	Timer 2	
4	Line control character*	Line control character*
5	Chain address	
6	Byte count	
7	Data address	
	0	15

*Used with Set Control operation.

Figure 2-2. Format of the DCB for a start command

Words 2 and 3 of the DCB for a *Start* command provide one of two functions, depending on the contents of the control word. If bits 12–15 of the control word equal 1101, words 2 and 3 contain line control characters. In all other cases, words 2 and 3 either contain values for Timers 1 and 2 or are not used.

DCB (device control block)

Word	*Control word*				*Addr key*											
0	0	0	1	0	0	X	X	X	0	0	0	0	0	0	0	0
1	Not used															
2	Not used															
3	Not used															
4	Not used															
5	Not used															
6	Byte count - must be 0006 for ACC															
7	Data address															
	0															15

Figure 2-3. Format of the DCB for a start cycle steal status command

Control Word

The control word is located in word 0 of the DCB. This word delineates the cycle-stealing operation. The format of the control word for a *Start Cycle Steal Status* command is shown in Figure 2-3. The format of the control word for the *Start* command is:

Bit	*Meaning*
0	Chaining flag
1	Not used–must be zero
2	Input flag
3	Not used–must be zero
4	Not used–must be zero
5–7	Cycle steal address key
8–9	Not used–must be zero
10–15	Operation

10	*11*	*12*	*13*	*14*	*15*	
X	X	0	0	0	0	Transmit
X	X	0	0	0	1	Transmit end
X	X	0	0	1	0	Transmit allow break
X	X	0	0	1	1	Transmit end allow break
0	X	0	1	0	0	Receive
0	X	0	1	0	1	Receive with timeout
1	X	0	1	0	0	Receive response
1	X	0	1	0	1	Receive response with timeout
X	X	0	1	1	0	Ring enable
X	X	0	1	1	1	Ring enable with timeout
X	X	1	0	0	0	DTR enable
X	X	1	0	0	1	DTR enable with timeout
X	X	1	0	1	0	DTR enable with tone
X	X	1	0	1	1	DTR enable with tone and timeout
X	X	1	1	0	0	DTR disable
X	0	1	1	0	1	Set control PTTC
X	1	1	1	0	1	Set control 8-bit interchange
X	X	1	1	1	0	Program delay
X	X	1	1	1	1	Reset

Bit	*Description*
0	Chaining flag–If this bit is on, the attachment fetches the next DCB in the chain, after completing the current DCB operation.
1	Not used–must be zero.
2	Input flag–This bit indicates the direction of data transfer. If bit 2 is on, data is transferred from the attachment to the processor. If bit 2 is off, data is transferred from the processor to the attachment. This bit must be on for either a receive operation or a *Start Cycle Steal Status* command.
3–4	Not used–must be zero.
5–7	Cycle-steal address key–This is a three bit key to be presented by the attachment during data transfers. It is used by the processor to determine if the attachment is to be allowed access to certain areas of storage.
8–9	Not used–must be zero.
10–15	The attachment decodes these bits to determine the operation to be performed.

Operations

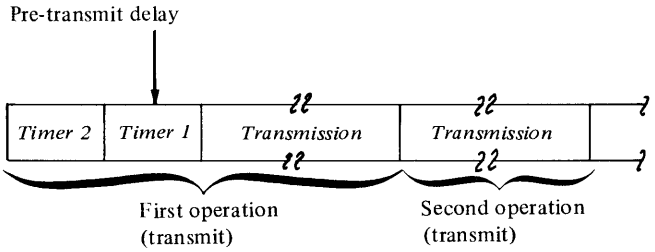
The following paragraphs describe the operations specified by bits 10–15 of DCB word 0 (the control word). Flowcharts for the operations are shown in Appendix B.

Transmit. This operation is used when another transmit type of operation is to follow immediately. Figure 2-4 shows an example of the use of this operation.

The attachment begins this operation by sending a 'request to send' to the modem and starting timer 2. The attachment then waits for a 'clear to send' from the modem. When the attachment gets 'clear to send', it resets timer 2, starts timer 1, and waits for timer 1 to timeout. When timer 1 times-out, the attachment begins fetching data from storage and transmitting the data to the remote station. The delay provided by timer 1, in this case, is called "pre-transmit delay"; its purpose is to allow the receiving station enough time to set up to receive data, and to allow time for the modem and communication lines to stabilize. If the attachment doesn't receive the 'clear to send' from the modem before timer 2 times-out, an exception interrupt occurs.

The attachment presents a device end interrupt or begins a DCB command chaining operation when the byte count goes to zero. The attachment stays in transmit mode and leaves its 'request to send' active at the end of this operation. This allows continuity from one transmit type of operation to another, without sending another 'request to send' and waiting for 'clear to send'.

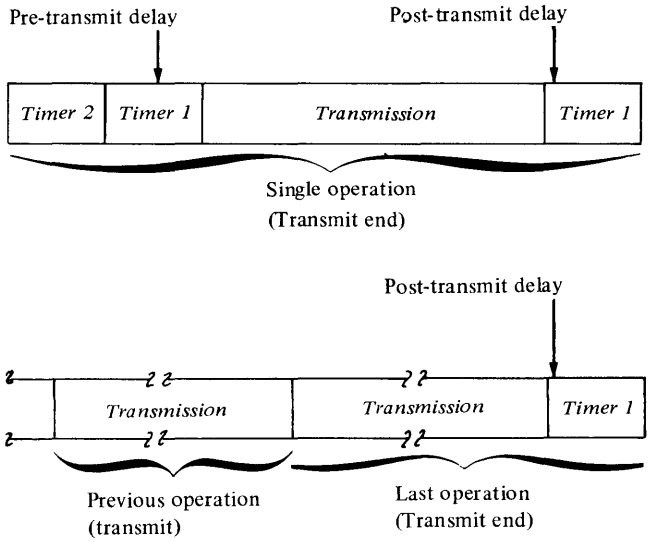
When chaining a series of transmit type of operations, timer 2 is used only in the first operation; timer 1 provides the pre-transmit delay in the first operation only.



Note. Timer 1 should be set for a pre-transmit delay of approximately six milliseconds when the receiving station is a program controlled device and is directly connected or connected through a full-duplex modem.

Transmit End. This operation is used to transmit the last block of data in a chain of transmit type of operations or when only one block is being transmitted. Figure 2-4 shows an example of the use of this operation.

This operation is the same as the *Transmit* operation—except that the attachment exits transmit mode and starts Timer 1 after the last character is sent to the modem. When timer 1 times-out, the attachment resets its 'request to send' (if RTS is *not* permanently jumpered "on"). This delay allows the last character to leave the modem before the attachment resets its 'request to send'. The timer 1 delay at the end of this operation is called "post-transmit delay." Note that timer 1 is used twice in this operation (pre-transmit and post-transmit delays), if this operation is not part of two or more transmit type of operations.



Transmit Allow Break. This operation is the same as the *Transmit* operation, except that it allows the receiving station to stop the transmission. To do this, the receiving station "breaks" the line for at least 150 milliseconds. If the attachment detects this condition, it resets transmit mode and 'request to send', and presents an exception interrupt with bit 0 on in the Interrupt Status Byte. The attachment does not reset RTS if it is permanently jumpered "on."

Transmit End Allow Break. This operation is the same as the *Transmit End* operation, except that this operation allows the receiving station to stop the transmission in the same way as the *Transmit Allow Break* operation.

Receive. This operation allows the attachment to begin placing data into storage when the attachment begins receiving valid data. If the carrier detect jumper is installed, 'carrier detect' must be active before the attachment can begin transferring data to storage.

If while receiving, the attachment detects a bad character, it places hex 00 into storage instead of the bad character. If the indicator panel is connected to the attachment and the switches on the panel are set to 11110, the attachment places the bad character into storage "as is."

The attachment checks every character it receives to see if the character is a COD character. The attachment presents a device end interrupt or begins a DCB command chaining operation when it recognizes a COD character.

The attachment terminates the operation and presents an exception interrupt if any of the following conditions occur:

1. The attachment is in transmit mode when this operation is started.
2. The 'data set ready' line is off when this operation is started.
3. The attachment detects an LRC error.
4. The attachment receives an EOB and a bad character was received during this operation.
5. The attachment detects a "long" or "short" record. This error is called "incorrect length record." Refer to INTERRUPT STATUS BYTE, bit 2.

Receive with Timeout. This operation is the same as the *Receive* operation, except that the attachment uses timer 1 to limit the time it will wait for the first character. It also limits the time between characters. Failure to receive a character within this time results in an exception interrupt with bit 0 set on in the ISB. If the carrier detect jumper is installed, the attachment allows the time specified by timer 1 for 'carrier detect' to become active. If 'carrier detect' does not become active within the specified time, the attachment presents an exception interrupt and posts "modem interface error" in *cycle steal status word one.*

Receive Response. This operation is used with record checking to receive the positive or negative response to a transmit operation.

This operation is the same as the *Receive* operation except that when the attachment is in a *Receive Response* operation, it always recognizes the COD 1 and COD 2 characters. Figure 2-4 shows an example of the use of this operation.

Receive Response with Timeout. This operation is the same as the *Receive Response* operation, except that the attachment uses timer 1 to limit the time that the attachment waits to receive the response.

Ring Enable. This operation is used in switched-line applications. It allows the attachment to recognize the fact that it is being called by another station. This command is only good for one call. The attachment cannot accept other operations until either a call is received or the device is reset. When the attachment detects a "ring," it presents a device end interrupt or begins a DCB command chaining operation.

Ring Enable with Timeout. This operation is the same as the *Ring Enable* operation except that the attachment uses timer 2 to limit the time it will wait for a "ring." If timer 2 times-out, the attachment presents an exception interrupt with ISB bit 0 set on.

DTR Enable. This operation causes the attachment to activate the 'data terminal ready' line. 'Data terminal ready' (DTR) must be active for any communication to take place. When the attachment receives 'data set ready' (DSR) from the modem, it presents a device end interrupt or begins a DCB command chaining operation. The attachment also presents an interrupt or begins a DCB command chaining operation if 'DSR' is already active.

Note. 'DTR' is normally jumpered on for leased lines.

DTR Enable with Timeout. This operation is the same as the *DTR Enable* operation except that the attachment uses timer 2 to limit the time that it will wait for 'DSR' to be returned from the modem. If timer 2 times-out before 'DSR' becomes active, the attachment presents an exception interrupt and sets ISB bit 0 on.

DTR Enable with Answertone. This operation is the same as the *DTR Enable* operation, except that the attachment places an answertone on the transmit line when 'data set ready' becomes active. The duration of the answertone is determined by timer 1. The attachment presents a device end interrupt or begins a DCB command chaining operation when the timer 1 timeout occurs. This operation can be used to generate a break condition. Timer 1 should be set for approximately three seconds for this operation. The exact setting depends on the modem being used. Therefore, you should consult the manual for the modem to determine the proper length of the answertone.

DTR Enable with Answertone and Timeout. This operation combines the functions of the *DTR Enable with Answertone* and *DTR Enable with Timeout* operations.

DTR Disable. This operation causes the attachment to deactivate the 'data terminal ready' line to the modem. The modem then disconnects itself from a switched network. The attachment starts timer 2 at the same time that it deactivates 'DTR'. When the timeout occurs, the attachment presents a device end interrupt or begins a DCB command chaining operation. It is recommended that timer 2 be set for at least one second. This operation should not be used in a leased line application.

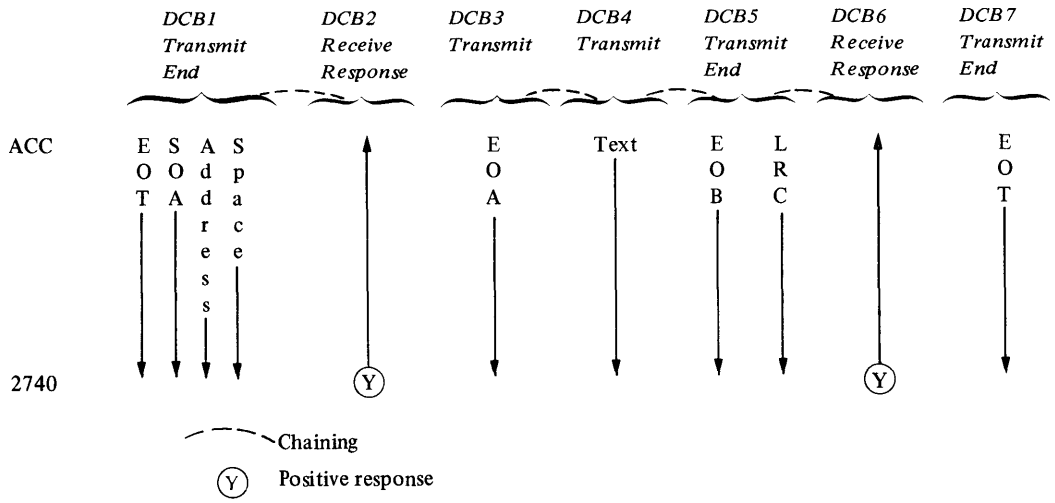


Figure 2-4. An example of using ACC operations

Set Control PTTC. This operation performs three functions:

1. It places the attachment in PTTC mode.
2. It loads the bit rate constant from word 1 of the DCB into the attachment's clock register.
3. It loads the line control characters from the DCB into registers in the attachment for use in transmit and receive operations. This enables the program to specify the bit pattern of all the line control characters. See the topic "Line Control" in this chapter for the location of the line control characters in the DCB.

The attachment presents a device end interrupt or begins a DCB command chaining operation at the end of this operation. The control information in the attachment remains unchanged until another *Set Control* operation is performed, or until a power-on reset occurs.

Set Control 8 Bit Data Interchange. This operation is the same as the *Set Control PTTC* operation, except that this operation places the attachment in 8 bit Data Interchange mode.

Program Delay. This operation provides a means for the program to use timer 2. The attachment loads the value specified in DCB word 3 into timer 2 and starts the timer. When the timeout occurs the attachment presents a device end interrupt or begins a DCB command chaining operation.

DCB Command Reset. This operation resets an individually addressed device. The prepare information, the information supplied by the *Set Control* operation, and 'data terminal ready' are not reset by this operation. A device end interrupt occurs or a DCB command chaining operation begins when the reset is complete.

Bit-Rate Constant

An eight bit hexadecimal number is used to control the bit-rate within a range.

The single-line attachment can run at speeds from 37.5 to 1,200 BPS (low range) with the low-speed jumper installed on the feature card. It can run at speeds from 300 to 9,600 BPS (high range) with the high-speed jumper installed.

Each line in a multiple-line attachment can run at speeds from 37.5 to 1,200 BPS with the low-speed jumper installed. By installing the high-speed jumper, speeds between 300 and 2,400 BPS can be obtained. In a multiple-line attachment, the low-speed and high-speed jumpers are located on the *Asynchronous Communications 4-Line Adapter* feature cards. There is only one set of jumpers on each 4-line adapter card. Therefore, if the high-speed jumper is installed on a 4-line adapter card, all lines associated with that card must run at speeds between 300 and 2,400 BPS.

The bit-rate constant is supplied to the attachment by the program. The constant is taken from the high order byte of DCB word 1 and stored in the attachment during a *Set Control* operation.

The bit-rate constant for low-range operation is determined by the following formula:

$$\text{Constant} = \frac{9600}{\text{BPS}} - 1$$

Round off to nearest whole number and convert to hexadecimal.

Example: Determine the bit-rate constant for 150 BPS.

$$\frac{9600}{150} - 1 = 63 \text{ (decimal)} = 3\text{F (hexadecimal)}$$

Therefore, the hex constant supplied by the program in conjunction with the *Set Control* operation would be 3F.

The bit-rate constant for high-range operation is determined by the following formula:

$$\text{Constant} = \frac{76800}{\text{BPS}} - 1$$

Round off to the nearest whole number and convert to hexadecimal.

Example: Determine the bit-rate constant for 1,200 BPS (with high-speed jumper installed).

$$\frac{76800}{1200} - 1 = 63 \text{ (decimal)} = 3\text{F (hexadecimal)}$$

Therefore, the hex constant supplied by the program in conjunction with the *Set Control* operation would be 3F.

Note. It is recommended that the high-speed jumper be installed when operating at speeds over 300 BPS.

There are some bit rates in the ranges shown above that are incompatible with the attachment. The difference between the bit rate of the attachment and the bit rate of the attached terminal must not exceed 1.5 percent. To determine the difference (in percent) use one of the following methods. An example follows method 2.

Method 1 For attachments that have the low-speed jumper installed.

- Step 1. Divide the terminal's bit rate into 9,600 and round the answer to the nearest whole number.
- Step 2. Multiply the above answer by .000104166. This gives the attachment's bit-time.
- Step 3. Determine the terminal's bit-time by taking the reciprocal of the terminal's bit-rate.

Step 4. Divide the smaller of the bit-times by the larger of the bit-times. Subtract the answer from 1. Multiply this answer by 100. This gives the percentage of difference between the bit-rate of the terminal and the actual bit-rate of the attachment for a given constant.

Method 2 For attachments that have the high-speed jumper installed. Compute the difference in the same manner as method 1, making the following substitutions:

Step 1. Substitute the number 76,800 for 9,600.

Step 2. Substitute the number .0000130208 for .000104166.

Example: Determine the difference between the bit-rate of the attachment and the bit-rate of a terminal that operates at 134.5 BPS.

Step 1 $\frac{9600}{134.5} = 71.37 = 71$

Step 2 .000104166
X 71
.007395786 = attachment's bit-time

Step 3 $\frac{1}{134.5} = .007434944$ = terminal's bit-time

Step 4 $(1 - \frac{.007395786}{.007434944}) 100 = 0.53\%$

Therefore, a terminal with a bit rate of 134.5 bps is compatible with the attachment.

Line Control Characters

When performing a *Set Control* operation, DCB words 2, 3 and 4, and the low order byte of word 1 contain characters (assigned by the program) to be used as line control characters.

The usage of these characters depends on whether Eight Bit Data Interchange Code or PTTC code is being used. Refer to the topic "Line Control" for further explanation.

Note. DCB words 2 and 3 are used for timer information in all DCBs except the DCB for a *Set Control* operation.

Timer 1

DCB word 2 contains the value to which timer 1 is to be set. Refer to 'Timeouts' earlier in this chapter.

Timer 2

DCB word 3 contains the value to which timer 2 is to be set.

Chain Address

This word (DCB word 5) contains the storage address of the next DCB when chaining is indicated. The address of the chain-to DCB must be even. If it is odd, the attachment sets ISB bit 3 on and terminates the operation.

Byte Count

The byte count is a 16 bit word (DCB word 6) which contains an unsigned integer representing the count for this data transfer. The count is always specified in bytes.

Data Address

This word (DCB word 7) contains the storage address of the first data transfer for the operation being performed.

INTERRUPT STATUS BYTE (ISB)

When the attachment presents an interrupt to the processor, the ISB is used to record status that cannot be indicated to the program via condition codes. The attachment presents the ISB to the processor as bits 0–7 of the interrupt ID word. The ISB is presented only when interrupt condition code 2 is reported. Its format is:

Bit	*Name*
0	Device dependent status available
1	Delayed command reject
2	Incorrect length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

The bits and their meanings are:

Bit	*Meaning*
0	Device dependent status available–If this bit is on, additional status is available via the *Start Cycle Steal Status* command (a discussion of this status follows in this chapter). This bit may be set on in conjunction with bit 2 (incorrect length record).
1	Delayed command reject–This bit is set on under any of the following conditions: a. The IDCB contains an odd numbered DCB address. b. The IDCB contains an invalid function/modifier.
2	Incorrect length record–This bit is reported only during receive operations. If ISB bit 0 is off and bit 2 is on, it indicates that the byte count has gone to zero and the attachment has not received a change of direction (COD) character. If ISB bits 0 and 2 are both on, the attachment received a COD character and the byte count was not zero.

3 DCB specification check–This bit is set on under any of the following conditions:
   a. The DCB contains an odd numbered chaining address (DCB word 5).
   b. The byte count (DCB word 6) contains a value other than 6 for a *Start Cycle Steal Status* command.
   c. The data address (DCB word 7) contains an odd address for a *Start Cycle Steal Status* command.
   d. The byte count for a transmit or receive operation is zero.
   e. Bit 2 of the DCB control word (word 0) is not set appropriately for the operation.

4 Storage data check–This bit is set on during cycle-steal output operations only. It indicates that the storage location accessed during the current output cycle contained bad parity. The parity in main storage is not corrected. The attachment terminates the operation.

5 Invalid storage address–This bit is set if the storage address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment terminates the operation.

6 Protect check–The attachment attempted to access a storage location without the correct cycle-steal address key.

7 Interface data check–A parity error was detected on an interface cycle-steal data transfer. The condition may be detected by the processor I/O channel or the attachment. In either case, the operation is terminated and an exception interrupt is presented to the processor.

CYCLE STEAL STATUS WORDS

Three words of status information are available via the *Start Cycle Steal Status* command. This information is available regardless of the setting of ISB bit 0.

The format of the DCB for this command is shown in Figure 2-3. Three words (6 bytes) of status information are transferred into main storage starting at the data address contained in DCB word 7.

Word Zero

Word zero contains the main storage address of the last attempted cycle steal transfer. This residual address may be either a data or DCB address. The value of the residual address must be examined to determine if it is a data address or a DCB address. When reporting a DCB address, the attachment reports the address of the low order byte of the last DCB word that the attachment attempted to fetch.

Word One

Word one has the following format:

Bit	*Name*
0	Overrun
1	Timeout
2	Block check error
3	DCB reject
4	EOB, count not zero
5	VRC error
6	Break detected
7	Stop-bit error
8	Not used
9	Modem interface error
10–15	Not used

The bits and their meanings are:

Bit *Meaning*

0 Overrun–During a receive operation, overrun occurs if the attachment is not able to transfer data to storage before the storage data register is needed for new data.

During a transmit operation, overrun occurs if the attachment is unable to fetch new data from storage in time to keep a steady stream of data going out on the line.

1 Timeout–This bit is set on if:
   a. DSR is not received from the modem within the predetermined time after an *Enable with Timer* operation begins.
   b. During a *Receive with Timeout* or a *Receive Response with Timeout* operation, no data is received within the limits established by timer 1.
   c. During a *Ring Enable with Timeout* operation, 'Ring indicator' is not received from the modem within the limits of timer 2.

2 Block check error–The LRC character received does not compare with the LRC character accumulated by the attachment. *PTTC mode only.*

3 DCB reject–This bit is set under any of the following conditions:
   a. A transmit type of operation is attempted when the attachment is in receive mode.
   b. A receive type of operation is attempted when the attachment is in transmit mode.

4 EOB, count not zero–*Transmit type of operation, PTTC mode only.*–An EOB was transmitted and the byte count was not zero.

5 VRC error–The parity of a received PTTC character was in error. The error interrupt is presented at the end of the message.

6 Break detected–During a *Transmit Allow Break* or *Transmit End Allow Break* operation, a "break" condition was detected. The attachment resets transmit mode and 'request to send' (if RTS is not permanently jumpered "on").

7 Stop-bit error–A character was received with a stop-bit missing. The interrupt does not occur until the count is decremented to zero or a COD character is received.

8 Not used–will be zero.

9 Modem interface error–Conditions which cause this error are:

a. DTR or DSR off at the beginning of a transmit or a receive operation
b. CTS on for more than one second while RTS is off at the beginning of a transmit operation
c. Loss of DTR or DSR during a transmit or receive operation
d. Loss of RTS or CTS during a transmit operation
e. 'Carrier detect' became inactive during a receive operation, or 'carrier detect' did not become active within the time specified by timer 1 at the beginning of a receive with timeout operation. These conditions are applicable only when the carrier detect jumper is installed.

10–15 Not used–will be zero.

Word Two

The high order byte of word two contains status regarding certain key lines of the device and indicates that the following lines or conditions are active:

Bit	*Line Name*
0	Data Terminal Ready
1	Data Set Ready
2	Request To Send
3	Clear to Send
4	Ring Indicator
5	Receive Mode
6–15	Not used (will be zero)

STATUS AFTER RESETS

There are several methods of resetting some or all of the circuits in the attachment. The resets and their effects are shown in the chart below.

	DTR with jmpr	*DTR w/o jmpr*	*RTS with jmpr*	*RTS w/o jmpr*	*Interrupt level*	*I-bit*	*Set control*	*Pending interrupts*	*Residual address*	*DCB*
Power on reset	on	off	on	off	off	off	off	off	off	off
System reset	on	--	on	off	--	--	--	off	--	--
Halt I/O	on	--	on	off	--	--	--	off	--	--
Device reset	on	--	on	off	--	--	--	off	--	--
DCB command reset	on	--	on	off	--	--	--	--	--	--
Indicator panel reset	--	off	--	--	--	--	--	--	--	--

-- not reset

JUMPERABLE OPTIONS

The following options can be selected by installing jumper wires on the feature cards.

Asynchronous Communications Single-Line Control Feature

Request To Send

If this jumper is installed, the attachment maintains 'request to send' in an active condition. This eliminates modem "turn-around" when using a full-duplex modem. This option should always be selected when using a modem which always keeps 'clear to send' active.

Data Terminal Ready

If this jumper is installed, the attachment maintains 'data terminal ready' in an active condition. This option must not be selected for switched-line operation.

Speed Range Jumpers

These jumpers are mutually exclusive; that is, one or the other must be selected, but not both.

Low Range. With this jumper installed, speeds between 37.5 BPS and 1,200 BPS can be selected by programming. However, it is recommended that the high range jumper be used for speeds above 300 BPS.

High Range. This jumper allows the program to select bit rates between 300 BPS and 9,600 BPS.

Carrier Detect

Some modems offer the ability to check the quality of the received signal. When the signal is of acceptable quality, the modem generates the signal 'carrier detect'. If the received signal starts to deteriorate, the modem notifies the attachment by deactivating 'carrier detect'. If the 'carrier detect' jumper is installed on the attachment card, the attachment waits for 'carrier detect' at the beginning of a receive type of operation. If 'carrier detect' does not become active within the specified time (timer 1) or if it becomes inactive during the receive operation, the attachment presents an exception interrupt and signals "modem interface error" to the processor.

Asynchronous Communications 4-Line Adapter Feature

All option jumpers for multiple-line attachments are located on the 4-line adapter cards.

Request To Send

There are four RTS jumpers on the card – one for each line. The jumpers perform the same functions as described for single-line attachments.

Data Terminal Ready

There are four DTR jumpers on the card – one for each line. The jumpers perform the same functions as described for single-line attachments.

Speed Range Jumpers

There is only one set (1 low range and 1 high range) of jumpers for the entire card. Therefore, all four lines on the card must run within the same range. The function of these jumpers is the same as previously described for the single-line attachment, except that the maximum bit rate in high range is 2,400 BPS.

Carrier Detect

There are four carrier detect jumpers on the card – one for each line. The jumpers perform the same functions as described for single-line attachments.

Section Two. Asynchronous Communications Features Operating Procedures

COMMUNICATIONS INDICATOR PANEL

The communications indicator panel is an option that can be a valuable aid to program debugging and machine troubleshooting.

The indicator panel provides a means of displaying various conditions and registers in the attachment. In addition, the 'data terminal ready' line(s) to the modem(s) can be reset from the indicator panel, and one setting of the function/display switches causes any bad data that is received to be placed in storage "as is."

Line Select Switches

The three line select switches are used only with multiple-line attachments. They are used to select a particular line. A line is selected by setting the last three bits of its device address, in binary form, into the line select switches.

These switches are ignored when the indicator panel is used with a single-line attachment.

Function/Display Switches

These switches determine what information is displayed in the indicator lamps. Figure 2-5 is a list of switch settings and the information that is displayed in the indicator lights.

Function/ Display switch setting	*Lamps*	*Information*
00000	0–7	High order byte of the DCB control word
00001	0–7	This information can be used in conjunction with the flowcharts in Appendix B to determine where the attachment is in an operation. Lamps 0–3 identify the subroutine. Lamps 4–7 show bits 12–15 of the DCB control word and identify the operation being performed.

4–7	*Operation*	*Chart*
0000	Transmit	B-1
0001	Transmit End	B-1
0010	Transmit Allow Break	B-1
0011	Transmit End Allow Break	B-1
0100	Receive or Receive Response	B-2
0101	Receive or Receive Response–with timeout	B-2
0110	Ring Enable	B-3
0111	Ring Enable with timeout	B-3
1000	DTR Enable	B-4
1001	DTR Enable with timeout	B-4
1010	DTR Enable with answer-tone	B-4
1011	DTR Enable with answer-tone and timeout	B-4
1100	DTR Disable	B-5
1101	Set Control	B-6
1110	Program delay	B-7
1111	Reset	B-8

00010	0–7	Bit-rate constant
00011	0–7	Line control character 1
00100	0–7	Line control character 2
00101	0–7	Line control character 3
00110	0–7	Line control character 4
00111	0–7	Line control character 5
01000	0–7	Line control character 6
01001	0–7	Line control character 7
01010	0–7	Bits 0–7 of the chain address
01011	0–7	Bits 8–15 of the chain address
01100	0–7	Bits 0–7 of the byte count
01101	0–7	Bits 8–15 of the byte count

Figure 2-5 (Part 1 of 2). Indicator panel information–ACC feature

Function/ Display switch setting	*Lamps*	*Information*
01110	0–7	Bits 0–7 of the data address
01111	0–7	Bits 8–15 of the data address
10000	0–7	Bits 0–7 of Timer 2
10001	0–7	Bits 8–15 of Timer 2
10010	0–7	Bits 0–7 of Timer 1
10011	0–7	Bits 8–15 of Timer 1
10110	0	Overrun
	1	Timeout
	2	Block check error
	3	DCB reject
	4	EOB, count not zero
	5	VRC error
	6	Break detected
	7	Stop-bit error
10111	0–3	Bits 8–11 of the DCB control word
	4	Modem interface error
	5	DTR jumper installed
	6	RTS jumper installed
	7	Carrier detect jumper installed
11001	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Transmit line is in a "space" condition
	6	Receive line is in a "space" condition
	7	Carrier detect
11010	0	Transmit/Receive data request
	1	Receive mode
	2	Receive line (space)
	3	Valid start bit detected
	4	8 bit data interchange code
	5	Transmit mode
	6	Overrun error
	7	Not used
11011	0–7	Contains the last character sent or received (Transmit/receive buffer)
11100	0–7	Lamp test–all lamps should blink
11101	0–7	The Interrupt Status Byte
11110		The lamps have no meaning. On a receive operation, this switch setting causes any bad data that is received to be placed into storage. Normally, the attachment puts hex 00 in storage in place of any received bad data. This switch setting applies to all lines on a multiple-line attachment, regardless of the setting of the line select switches.
11111	0–7	The information displayed is the same as in switch setting 11001. However, this switch setting resets DTR if it is not jumpered "on".

Figure 2-5 (Part 2 of 2). Indicator panel information–ACC feature

ERROR RECOVERY

Block Check Error

Transmit a negative acknowledgment character and notify the user.

DCB Reject

Reset and reinitialize the attachment. Retry the operation. Notify the user if the error persists.

DCB Specification Check

Verify the correctness of the following:

1. The chain address (must be even)
2. The byte count
3. The data address (must be even for a *Start Cycle Steal Status* command)
4. The setting of bit 2 of the DCB control word

If the above are correct, retry the command three times. If the error persists, notify the user.

EOB Count Not Zero

Notify the user.

Incorrect Length Record

Change the byte count or notify the user. This error results if either of the following occurs:

a. Byte count goes to zero before a COD character is received. Under this condition ISB bit 0 will be off.
b. A COD character is received and the byte count is not zero. Under this condition ISB bit 0 will be on.

Interface Data Check

Reset the attachment and retry three times. Notify the user if the error persists.

Invalid Storage Address

Verify the correctness of the DCB address and the data address. If these addresses are correct, retry the command three times. If the error persists, notify the user.

Modem Error

Retry three times. Notify the user if the error persists.

Overrun

Retry the operation. Notify the user if the error persists.

Protect Check

Verify the correctness of the cycle-steal address key and the data address. If these are correct, retry three times. Notify the user if the error persists.

Stop-bit Error

Retry up to three times. Notify the user if the error persists.

Storage Data Check

Reset the attachment and retry three times. Notify the user if the error persists.

Timeout

Increase the value of timer 2 and retry, or notify the user.

VRC Error

Notify the user. Also transmit a negative acknowledgment character if record checking is being used.

Chapter 3. Binary Synchronous Communications Features

Section One. Product Description

The Binary Synchronous Communications (BSC) features control transfer of serial data to and from remote terminals or host systems via modems and communications line facilities.

There are several important items to consider about the BSC features. They are:

- Data transmission uses binary synchronous communications procedures
- EBCDIC and ASCII codes are used
- Bit rates can be as high as 56,000 bits per second (BPS)
- The BSC features serve as control (primary) or controlled (secondary) stations
- The single-line BSC features can receive IPL
- Transparency is standard
- Intermediate Block Checking is standard
- Internal clocking can be selected by installing a jumper wire on the feature cards (medium speed only)
- Answertone generation can be selected by installing a jumper wire on the feature cards (medium speed only).

Data transmission is serial-by-bit, using the binary synchronous communications (BSC) method of character and bit transmission. A general discussion of BSC procedures may be found in *General Information–Binary Synchronous Communications,* GA27-3004.

The BSC features can communicate with terminals or host systems using EBCDIC (Extended Binary-Coded Decimal Interchange Code) or ASCII (American Standard Code for Information Interchange) codes. The selection of a code is under program control.

The medium-speed, single-line feature can handle bit rates up to 9,600 BPS. The high-speed, single-line feature can handle up to 56,000 BPS. The multiple-line feature can handle up to 9,600 BPS on lines 0 and 1; and up to 2,400 BPS on lines 2–7. There is, however, one exception; that being: *when only four lines are installed, each line can run at speeds up to 4,800 BPS.* The bit rate for an individual device (line) is established by the modem's transmit and receive clocks. On medium speed attachments, if the modem does not provide clocking, internal clocking must be used. Internal clocking provides bit rates of 1,200 BPS or 600 BPS (under program control). The high speed attachment makes no provision for internal clocking.

The BSC can serve as a control station or can be controlled by another station in the data link. The single-line BSC features are the only communications attachments through which the system can receive a host initiated IPL (initial program load).

The BSC features provide the ability to send and receive unrestricted binary data. This is known as "transparency." Transparency is available only when using EBCDIC code. A BSC feature enters and exits transparent text mode through codes in the data stream.

Intermediate Block Checking allows the user to increase system efficiency by avoiding line turn-around for each block of data for which separate error detection (BCC checking) is desired.

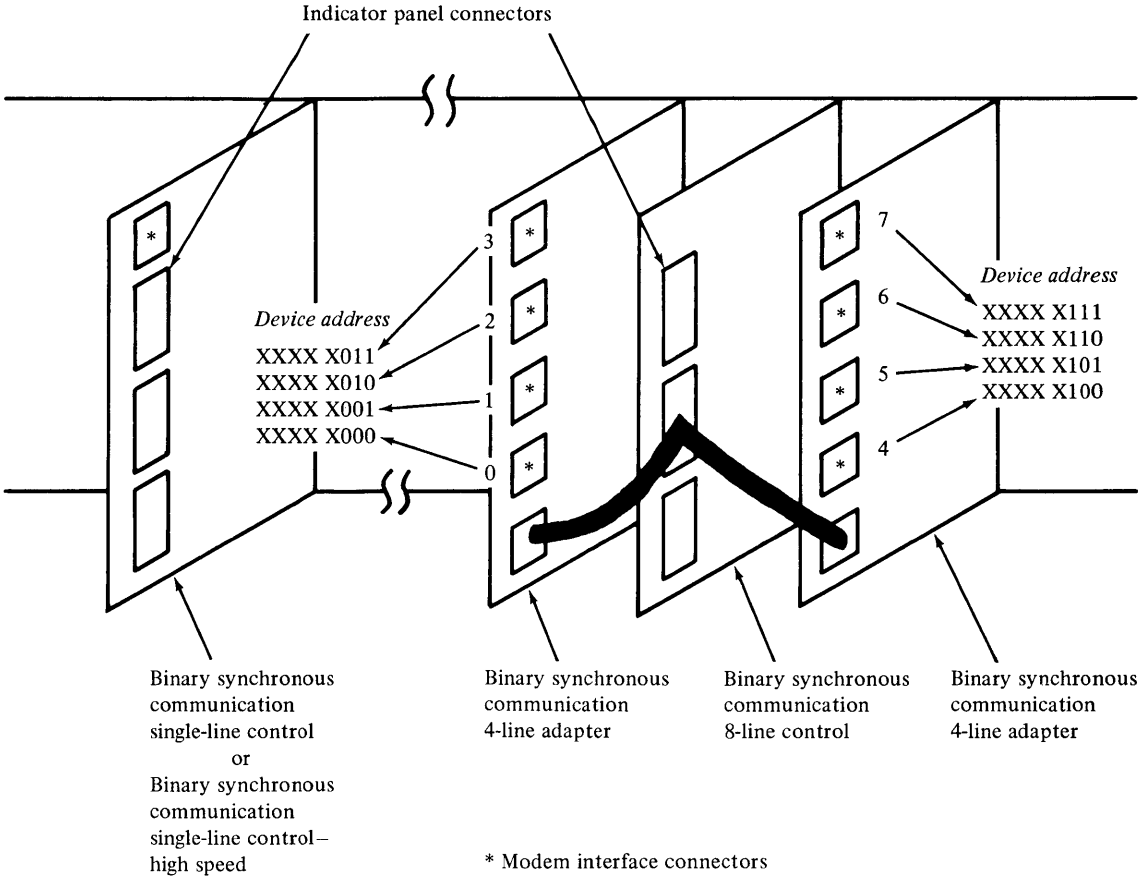
BSC FEATURE CONFIGURATIONS

The BSC features are available in single-line and multiple-line configurations. The multiple-line configuration provides up to eight lines. The single-line configurations are contained on one card. The multiple-line configuration contains either two or three feature cards—two cards for one to four lines, three cards for five to eight lines.

Note. Throughout the remainder of this chapter, the term *attachment* is used as a general term to refer to any of the following:

1. The Binary Synchronous Communications Single-Line Control feature.
2. The Binary Synchronous Communications Single-Line Control/High Speed feature.
3. The Binary Synchronous Communications 8-Line Control feature and one or two Binary Synchronous Communications 4-Line Adapter features.

When referring specifically to items 1 or 2 above, the term *single-line attachment* is used. When referring specifically to item 3, the term *multiple-line attachment* is used.



Each line operates in half-duplex mode.

DATA TRANSMISSION CODES

The BSC attachments allow data communications using EBCDIC or ASCII as line codes. ASCII code can be specified by the program after the IPL. The attachment establishes EBCDIC code if:

- No code is specified
- A Power On Reset occurs
- A System Reset occurs

The EBCDIC and ASCII character assignments are shown in Appendix A.

DATA FLOW

Each character occupies one byte in storage. Transfers to and from storage are two bytes at a time, except that the first and/or last transfers may move only one byte if specified by the data address or byte count.

Transmit

Transmission data is fetched from storage two characters at a time (except as noted above). The high order byte holds the first character to be sent and the low order byte holds the next character. After a character has been transferred into the Serdes (serializer/deserializer), it is transmitted over the line, low order bit first.

ASCII characters in storage are eight bits in length—seven data bits plus one parity bit. This parity bit should not be confused with the parity bit in storage. The ASCII parity bit is bit 0 in a byte of storage.

The attachment does not check the ASCII parity during transmit operations, therefore, the program must maintain odd parity in storage bits 0—7 when using ASCII code. Figure 3-1 illustrates BSC attachment data flow.

Receive

The first bit received is transferred into the low order bit position of a byte, the second received bit is transferred into the next higher bit position, and so on until a character is assembled. Two characters are assembled in the attachment before data is transferred to storage (except as noted above) When two characters are to be transferred to storage, the first character received is loaded into the high order byte of the storage data register and the next character is loaded in the low order byte before the data is transferred to storage. Data is written into main storage without any code translation.

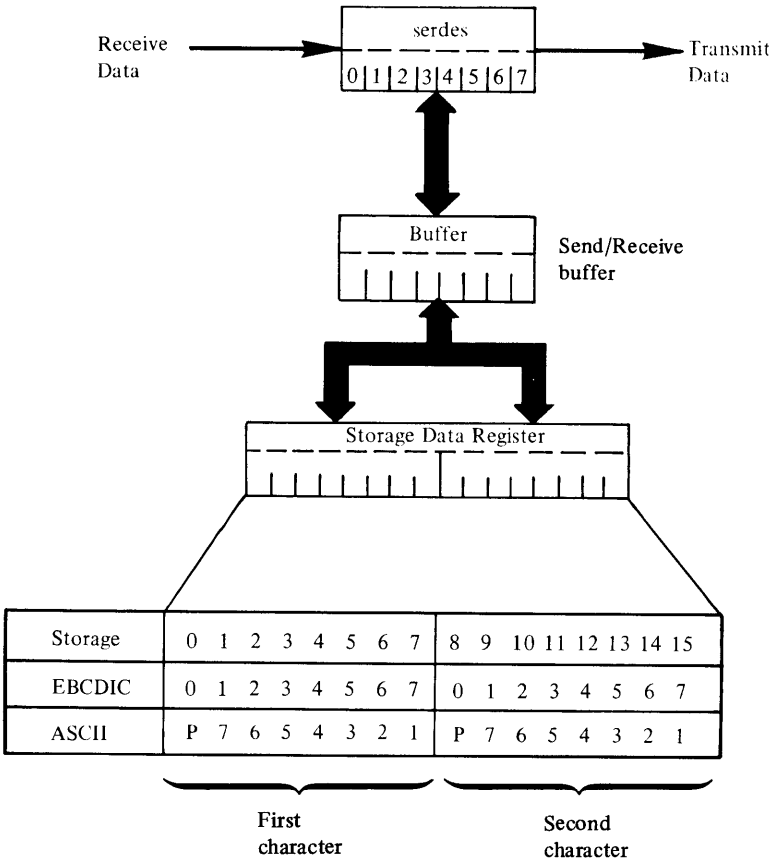


Figure 3-1. BSC feature data flow

CONTROL CHARACTERS AND SEQUENCES

For detailed information on binary synchronous communications conventions, refer to *General Information Binary Synchronous Communications,* GA27-3004.

Figure 3-2 shows the control characters and sequences for BSC.

Name	*Mnemonic*	*EBCDIC*	*ASCII*
Start of heading	SOH	SOH	SOH
Start of text	STX	STX	STX
End of transmission block (note 1)	ETB	ETB	ETB
End of text (note 1)	ETX	ETX	ETX
End of transmission (note 1)	EOT	EOT	EOT
Enquiry (note 1)	ENQ	ENQ	ENQ
Negative acknowledge (note 1)	NAK	NAK	NAK
Synchronous idle	SYN	SYN	SYN
Data link escape	DLE	DLE	DLE
Intermediate block character	ITB	IUS	US
Initial program load (note 2)	IPL	DC1 DC1 ENQ	
Even acknowledge (note 1)	ACK 0	DLE (70)	DLE 0
Odd acknowledge (note 1)	ACK 1	DLE/	DLE 1
Wait before transmit-pos. ack (note 1)	WACK	DLE,	DLE;
Mandatory disconnect (note 1)	DISC	DLE EOT	DLE EOT
Reverse interrupt (note 1)	RVI	DLE@	DLE<
Temporary text delay	TTD	STX ENQ	STX ENQ
Transparent start of text (note 3)	XSTX	DLE STX	
Transparent intermediate block (note 3)	XITB	DLE IUS	
Transparent end of text (note 3)	XETX	DLE ETX	
Transparent end of transmission block (note 3)	XETB	DLE ETB	
Transparent synchronous idle (note 3)	XSYN	DLE SYN	
Transparent block cancel (note 3)	XENQ	DLE ENQ	
Transparent TTD (note 3)	XTTD	DLE STX DLE ENQ	
Data DLE in transparent mode (note 3)	XDLE	DLE DLE	

Notes

1. These control characters and sequences cause a COD (change of direction) interrupt request after the required action has been completed.
2. Not applicable in ASCII format.
3. Transparent mode is not available in ASCII.

Figure 3-2. BSC feature control characters

The functions of the control characters follow.

Mnemonic	*Function*
SOH or STX	Reset control mode and set the adapter to text mode. BCC accumulation starts with the first character after the first SOH or STX.
ETB or ETX	Reset text mode with block check character (BCC) comparison.
EOT	End of transmission.
ENQ	Reset text mode without BCC transmission and comparison.
NAK	Negative response to a request for a reply, or to a block of heading or a block of text in error.
SYN	Transmitted automatically by the adapter to establish and maintain synchronization.
DLE	Alert the adapter to test the next character for a defined control sequence in transparent text mode. In nontransparent text mode, DLE is treated as data.
ITB	Included in the BCC; it causes the BCC to be sent.
IPL	Control characters to initiate an IPL sequence.
ACK 0	Indicate affirmative acknowledgment to even blocks.
ACK 1	Indicate affirmative acknowledgment to odd blocks.
WACK	Indicate a temporary not ready to continue/receive condition.
DISC	Used on switched communication facilities only, to initiate a disconnect.
RVI	Reverse direction of data transfer.
TTD	Alert the receiving station to a temporary text delay.
XSTX	Turn off control mode and set the adapter to transparent text mode.
XITB	Same as ITB, but also turn off transparent text mode.

XETX or XETB	Same as ETB or ETX but also turn off transparent mode.
XSYN	Transmitted automatically by the adapter to establish and maintain synchronization in transparent text mode.
XENQ	Turn off transparent text mode and cancel the current block of data.
XTTD	Alert the receiving station to a temporary text delay in transparent text mode.
XDLE	In transparent text mode, the transmitter adds a second DLE after each data DLE. At the receiver, the first DLE is stripped off and does not enter storage or the BCC.

LINE ERROR CHECKING

Two different types of checking are employed depending on the code selected. CRC (cyclic redundancy check) is used with EBCDIC and LRC/VRC (longitudinal redundancy and vertical redundancy checking) is used with ASCII.

Error correction is accomplished through programmed retransmission of the block that is in error.

SYNCHRONIZATION AND TIMING INFORMATION

The attachment receives strobing pulses from the modem which establish and maintain bit synchronization. If the modem does not supply a strobe, the internal clocking feature must be jumpered on (during installation) to supply synchronization. Whichever form of bit synchronization is used, a specific series of characters precedes each transmission in order to establish character synchronization.

Transmit Synchronization

The attachment automatically begins transmission with a leading pad character (hexadecimal 55) followed by the initial synchronizing pattern of two SYN characters. If internal clocking is being used, the attachment transmits two leading pad characters.

To maintain synchronization the attachment inserts a sync pattern of SYN SYN at every transmit timeout. In transparent text mode this sync pattern is DLE SYN.

Trailing Pad Characters

The attachment automatically transmits a trailing pad character (hexadecimal FF) after every COD character (or after the BCC if the change of direction calls for BCC). This insures that the last character sent (COD or BCC) goes on line in its entirety. A pad of FF also provides the second character of the NAK and EOT control character sequences. The attachment does not begin an interrupt or chaining operation until the entire pad character is transmitted.

SYN and pad characters (leading and trailing) are provided by the attachment and are not stored in main storage.

Receive Synchronization

Character phase (synchronization) is established when two consecutive SYN characters (followed by any non-SYN character) are received and decoded. Synchronization is maintained because the transmit station periodically inserts two SYN characters into the data stream.

SYN and pad characters are deleted by the attachment and are not stored in main storage.

TIMEOUTS

There are three general types of timeouts possible with BSC operations data set ready, receive, and program.

Data Set Ready Timeout

When performing an enable terminal operation, bit 12 of DCB word 0 can be used to cause the attachment to wait only three seconds for 'data set ready' to be returned by the modem. If DSR is not returned within three seconds of DTR being activated, the attachment terminates the operation and presents an exception interrupt.

Receive Timeout

The receive timeout is nominally three seconds and causes the attachment to present an exception interrupt (condition code 2) under the following conditions:

- Character phase is not established within three seconds after the attachment accepts a receive data operation. This is under program control and is effective only if bit 12 is set on in Word 0 of the current DCB.
- A continuous sync pattern, or transparent sync idle (in transparent mode) is received for three seconds.
- While receiving data, no sync pattern, or transparent sync idle, is received for three seconds.

Program Timeout

A two second timeout is available for use by the program. It is initiated by a *Start* command with bit 12 alone on in Word 0 of the associated DCB. After two seconds, the attachment presents a device end interrupt (condition code 3).

OPERATING MODES

The attachment has several operating modes which are selected by control characters.

Text Mode

Text mode is selected when the first SOH or STX control character is decoded by the attachment during a transmit or receive operation. Subsequent SOH and STX characters are treated as data characters. During text mode, the attachment processes header or text characters and accumulates a block check character (BCC). SYN characters and the first SOH or STX characters decoded are not included in the BCC accumulation. Text mode is terminated after an ETX or ETB character is decoded by the attachment.

Transparent Text Mode

Transparent text mode is selected when a DLE-STX control character is decoded during a transmit or receive operation. While in this mode, any kind of binary data can be transmitted or received. The following changes from text mode occur:

- The attachment recognizes individual control characters or control sequences (ETB, STX, ENQ, etc) only as data with no other associated function.
- All inserted SYN characters are automatically preceded by a DLE character (DLE-SYN).
- A second DLE is automatically attached to every data DLE to mark it as such. This second DLE and the inserted DLE-SYNs are automatically deleted upon reception and do not enter main storage.

To leave transparent text mode, the following ending sequences are available:

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

These sequences must be transmitted by using the *Exit Transparent* operation (see 'Device Control Block', Control Word, bit 14). If these sequences are transmitted by the regular transmit operation (in transparent text mode), the transmitting attachment will automatically insert a second DLE between the first DLE and the ETX (or ETB or ENQ or ITB). The receiving station will then discard the first DLE and consider the inserted DLE and the ETX (or ETB or ENQ or ITB) as two data characters and place them in storage. The *Exit Transparent* operation prevents the attachment from inserting a second DLE. Thus, the receiving station will recognize the ending sequences as ending sequences, not data. Because the DLEs in these ending sequences are true DLEs and are not placed in storage at the receiver, they should not be included in the byte count for the receiving station.

Only DLE-ITB leaves the attachment in text mode; all of the others cause a change of direction (COD).

During transparent text mode, a BCC is accumulated as in normal text mode. The only DLE characters included in the BCC are the data DLEs.

Control Mode

In a multipoint configuration, when the attachment receives a valid EOT sequence, it enters control mode. While in control mode, the attachment monitors for its station address. If it does not enter selected mode and receives an SOH or an STX, the attachment exits control mode. The attachment must receive another EOT before it can re-enter control mode.

Selected Mode

The attachment enters selected mode when it decodes its station address twice (contiguously) after establishing byte synchronism. If a receive operation has been initiated, the message sequence starting with the second station address character is transferred to storage.

Note. The attachment's station-address (used in multipoint configuration only) is determined by discrete jumper wires which are installed during installation. Control characters may not be used as an address. The EBCDIC 2-bit or the ASCII 6-bit of the station address are not used by the hardware. The program, however, may use these bits to differentiate between a polling and a selecting sequence.

Multipoint address bit 0 must not be jumpered "on" when using ASCII code.

IPL Mode

Initial program load by a host system may be accomplished through a *single-line* attachment only. A jumper-wire must be installed on the card to allow the attachment to IPL the processor.

When the IPL sequence (DC1-DC1-ENQ) is received, the attachment responds with an EBCDIC acknowledgment (ACK 0). If the attachment is a multipoint tributary station, it must be in selected mode.

The host must then transmit DLE-STX (to put the attachment into transparent text mode) followed by the IPL program. The attachment places this program into main storage beginning at location 0000. The attachment strips the DLE-STX from the loaded IPL program.

Upon receiving a DLE-ETX followed by a valid BCC, the attachment presents a device end interrupt on level zero. Therefore, the IPL'ed program should provide for handling this interrupt. The program should then send a positive acknowledgment back to the host system.

If the IPL operation is unsuccessful, the attachment holds the processor in IPL mode (load light on) and monitors the line for a retry of the IPL operation. A sample IPL sequence is shown in Appendix A.

Notes.

1. In order for an unattended processor to be IPL'ed on a switched network, the modem must be capable of automatically answering calls.
2. On a leased line, the attachment cannot receive an IPL unless 'data terminal ready' is jumpered "on."
3. There are some modems which do not supply clocking and cannot run at speeds higher than 600 BPS. These modems require the use of the internal clocking feature of the BSC attachments. Internal clocking automatically supplies clocking at 1,200 BPS. The 600 BPS rate of internal clocking can only be selected by a program already in storage. Therefore, it is not possible to IPL the system via the BSC attachments when such a modem is used.

COMMANDS

The Operate I/O instruction points to the IDCB which contains one of the following commands.

- Prepare
- Device Reset
- Start
- Start Cycle Steal Status
- Read ID
- Start Diagnostic 1 or 2
- Start Control

Prepare

The *Prepare* command is used to control the interrupt parameters of the addressed device. The immediate data field of the IDCB contains the level and I-bit information. The single-line attachment is always able to accept and execute a *Prepare* command, even if it is busy or has an interrupt pending from a previous command. On a multiple-line attachment, the device returns a condition code 1 (CC1) to this command if it has an interrupt pending. The IDCB for the *Prepare* command has the following format:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
60	*00–FF for multiple-line attachments* *00–7F for single-line attachments*

Immediate data field			
	Zeros	Level	I
16	... *26*	*27* ... *30*	*31*

Level. This four-bit encoded field specifies the priority interrupt level assigned to the device.

Example:
0000 = level 0, 0001 = level 1,
0010 = level 2, 0011 = level 3.

A prepare command issued to any device on a multiple-line attachment prepares *all* of the devices in the attachment to interrupt on the same level. The I-bit information, however, applies only to the specific device addressed.

I. This bit determines whether the device is allowed to request an interrupt. An I-bit value of 1 permits the device to request an interrupt, and a value of 0 prevents the device from interrupting.

The prepared attachment stores the level data and presents it to the processor each time an enabled device presents an interrupt request. This data is reset by a system reset, or a power-on reset. The prepare information can be changed by the successful execution of another *Prepare* command.

Device Reset

This command resets the addressed device and clears any pending interrupts (except *controller end*). The prepare information (including the I-bit) and the residual address do not change. This command does not reset 'data terminal ready'.

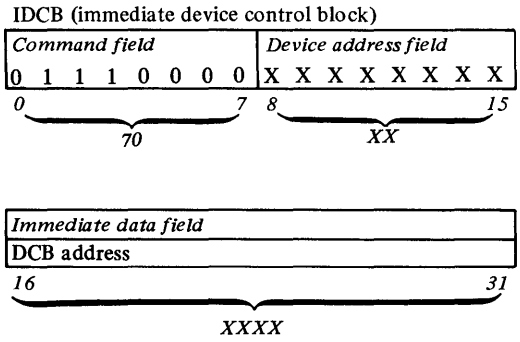
IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 1 1 1 1	X X X X X X X X
0 ... *7*	*8* ... *15*
6F	*XX*

Immediate data field																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16																*31*
00																

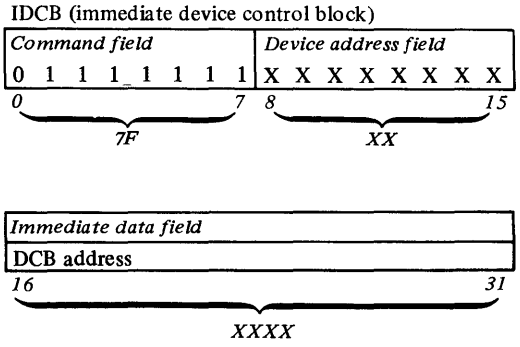
Start

This command initiates a cycle-stealing operation for the addressed device. The format of the IDCB for the *Start* command is:



Start Cycle Steal Status

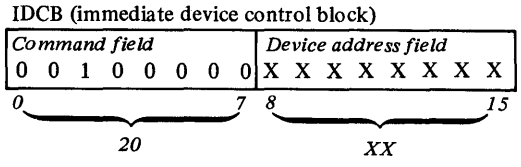
This command causes the device to initiate a cycle-stealing operation for the purpose of sending (to the processor) status information relative to the previous cycle-stealing operation. The format of the IDCB for this command is:

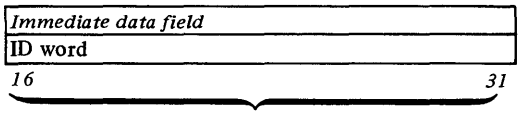


See 'Cycle Steal Status Words' for a description of the information transferred to storage by this command.

Read ID

This command puts the attachment's identification word (ID) into the Immediate Data Field of the IDCB. The ID word contains physical information about the attachment that is used to tabulate the system's configuration. The *Read ID* command is generally used in diagnostic programming.

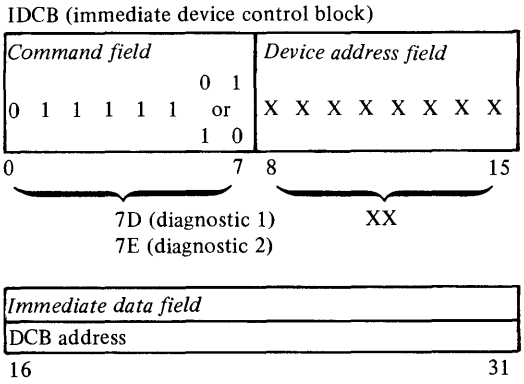




Single line BSC	*1006*
Two line BSC	*2106*
Four line BSC	*2206*
Six line BSC	*2306*
Eight line BSC	*2006*

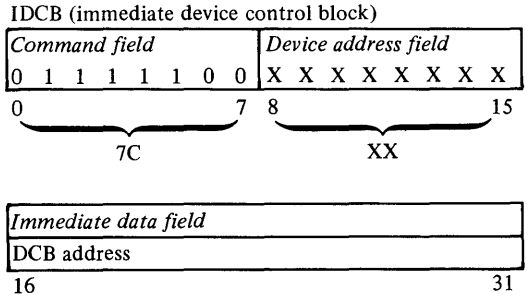
Diagnostic Commands

There are two diagnostic commands. They are used by diagnostic programs to determine if the attachment is operating properly. These commands are called *Start Diagnostic 1* and *Start Diagnostic 2.* For a full explanation of these commands, refer to chapter 5 of *IBM Series/1 4955 Processor–Theory Diagrams*, SY34-0041; or *IBM Series/1 4953 Processor–Theory Diagrams*, SY34-0042.



Start Control

This command is reserved for use by IBM engineering.

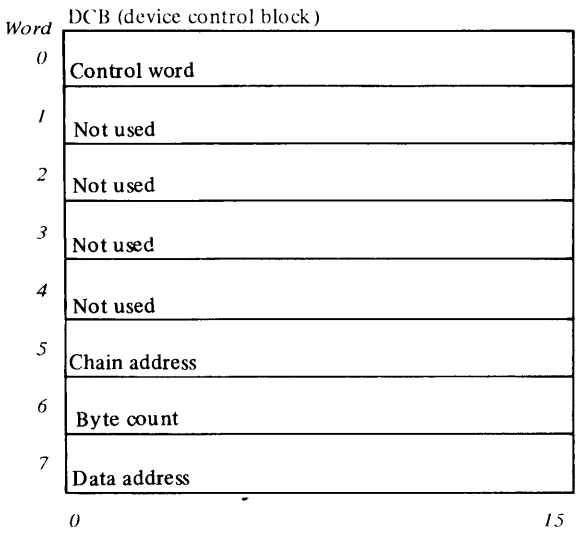


Accidental issuance of this command may result in the attachment becoming inoperable. If this happens, the attachment can only be restored to operation by turning power off, then on again.

DEVICE CONTROL BLOCK (DCB)

The DCB is an eight word area in main storage which describes the specific parameters of the cycle-stealing operation. Its location in storage is assigned by the program. The data in its words is loaded and changed by the program. It is fetched by the attachment, using a cycle-steal address key of zero, after successful execution of a *Start*, or *Start Cycle Steal Status* command. The DCB address transferred to the atachment via the IDCB points to word 0 of the DCB.

The address of the DCB must be even numbered. If the DCB address is odd numbered, the attachment sets ISB bit 1 on (delayed command reject) and terminates the operation.



Control Word

This word prescribes the operation to be performed. The format of the control word is:

Bit	*Name*
0	Chaining flag
1	Not used–must be zero
2	Input flag
3	Not used–must be zero
4	Not used–must be zero
5–7	Cycle steal address key
8	Half rate
9	ASCII mode
10	Enable terminal
11	Disable terminal
12	Start timer
13	Transmit operation
14	Exit transparent
15	Not used

Bit	*Meaning*
0	Chaining flag–If this bit is on, the attachment fetches the next DCB in the chain at the end of the current DCB operation. *Programming note.* Chaining should not be used to receive continuous blocks of data in the high speed attachment (greater than 9,600 BPS), or the multiple-line attachment. Overrun errors may occur if receive operations are chained in these attachments.
1	Not used–Unpredictable results will occur if this bit is set on.
2	Input flag–The setting of this bit tells the device the direction of data transfer, relative to main storage. Bit 2 off = Output (storage to device) Bit 2 on = Input (device to storage) On a *Start* command, this bit being on specifies a receive operation. Receive Operation (Input) The receive operation allows the attachment to start transferring data to main storage after character synchronization is established. The attachment presents a normal device end interrupt or begins a DCB command chaining operation when a change of direction (COD) character is received and the byte count is decremented to zero. The attachment presents an exception interrupt and sets bit 1 of the ISB if 'data set ready' is off when the operation begins. Bit 12 of DCB word 0 may be used with this operation to limit, to three seconds, the time that the attachment will allow for establishing character synchronization. Failure to establish character synchronization within this time results in an exception interrupt with bit 0 set on in the ISB.
3	Not used–must be zero.
4	Not used–must be zero.
5, 6, 7	Cycle steal address key–This is a three bit key presented to the processor by the attachment during cycle-stealing data transfers so that the processor can ascertain whether the attachment is authorized to access certain blocks of main storage.
8	Half rate–The attachment uses this bit only during the *enable terminal* operation. If bit 8 is on, the modem (if it is equipped to recognize half rate) runs at one-half of its normal bit rate. If internal clocking is being used, this bit selects the 600 BPS rate. If the state of the rate select line is to change, the attachment automatically waits 13 seconds before checking for 'data set ready'. This allows the modem enough time to equalize. *Note.* If half rate is on and the attachment generates an answertone, it resets half rate. Therefore, another *enable terminal* operation is required to set half rate again.
9	ASCII mode–If this bit is on, the attachment uses ASCII code. If the bit is off, the attachment uses EBCDIC code.
10	Enable terminal–This bit is used to activate 'data terminal ready' (DTR) to the modem. A device end interrupt occurs 50 milliseconds after 'data set ready' (DSR) is returned by the modem. If 'data set ready' is already active, the interrupt occurs immediately. Bit 12 may be used in conjunction with this operation to limit the time that the attachment will wait for 'data set ready' to become active. If bit 12 is on, failure to get 'data set ready' within three seconds results in DTR being reset and an exception interrupt with ISB bit 0 set on.

On a medium speed, single-line attachment jumpered for IPL operation, a ring indication (switched network only) from the modem also sets DTR on. For manual call or manual answer sequences, bit 10 must be used to set DTR prior to entering data mode.

On a leased line, DTR is normally jumpered "on" permanently.

11 Disable terminal–This bit causes the attachment to deactivate DTR in order to disconnect the modem from a switched network. The attachment presents a device end interrupt or begins a chaining operation two seconds after DSR goes off. If DSR does not drop within three seconds, the attachment presents an exception interrupt with ISB bit 0 set on.

12 Start timer–This bit can be used with an enable terminal operation or with a receive operation to provide a three second timeout. When used alone, bit 12 causes the attachment to start timing a two second period, after which the attachment presents a device end interrupt.

13 Transmit operation–This operation starts a three second timer and turns on 'request to send' (RTS). When the modem returns 'clear to send' (CTS), the attachment establishes synchronization (described under 'Synchronization and Timing Information'). The attachment then starts fetching data from main storage and transmitting the data.

The attachment presents a normal device end interrupt or begins a DCB command chaining operation when a line turn-around character (COD) is transmitted and the byte count goes to zero.

The attachment presents an exception interrupt and sets bit 0 on in the ISB if 'data set ready' is off when the operation begins.

Failure to receive 'clear to send' from the modem within the three second timeout period or CTS being active for three seconds without RTS being active results in an exception interrupt with bit 0 set on in the ISB.

The attachment resets 'transmit mode' and 'request to send' after transmitting the pad character following a COD character. If block checking is used, the attachment resets 'transmit mode' and 'request to send' after transmitting the pad character following the block check character (BCC).

Note. 'Request to send' can be permanently jumpered "on" when desired. 'Clear to send' must not be permanently returned by the modem unless 'request to send' is jumpered "on."

14 Exit Transparent–Since the BSC attachment does not recognize control characters when transmitting in transparent text mode, there must be a method of transmitting control sequences so that they can be recognized as such. This is accomplished by the *exit transparent* operation.

The *exit transparent* operation requires its own DCB and a byte count of 2. Unexpected results may occur if the byte count is greater than two.

This operation should only be used to transmit the control sequences shown below, following a block of transparent text.

a. DLE-ETX
b. DLE-ETB
c. DLE-ITB
)LE-ENQ

used–This bit should be set to zero.

Chain Address

This word contains the storage address of the next DCB and is used when chaining is indicated. The chain address must be even. If it is odd, the attachment sets ISB bit 3 on and terminates the operation.

Byte Count

This 16 bit word contains the number of bytes to be transferred to or from storage.

Data Address

This is the address in main storage where data transfer is to start.

INTERRUPT STATUS BYTE (ISB)

When the attachment presents an interrupt to the processor, the ISB is used to record status that cannot be indicated to the program via condition codes. The ISB is meaningful only when interrupt condition codes 2 or 6 are reported. The processor sees the ISB in bits 0–7 of the *interrupt ID word*. The format of the ISB is:

Bit	*Name*
0	Device dependent status available
1	Delayed command reject
2	Incorrect length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

The bits of the ISB and their meanings follow.

Bit *Meaning*

0 Device dependent status available–If this bit is on, additional status is available via the *Start Cycle Steal Status* command (a discussion of this status follows in this chapter). This bit may be set on in conjunction with bit 2 (incorrect length record).

1 Delayed command reject–This bit is set on under the following conditions:
a. The command field of the IDCB contains an invalid function/modifier bit combination.
b. The IDCB contains an odd numbered DCB address.
c. The command field of the IDCB specified a *Write* command (010X XXXX).

2 Incorrect length record–This error can occur during both transmit and receive operations. It is caused by either of the following conditions:
a. The byte count has been decremented to zero, the attachment has not detected a COD character, and the chaining flag is off.
b. The attachment has detected a COD character and the byte count has not been decremented to zero. In this case, ISB bit 0 is also set on. A *Start Cycle Steal Status* command can be used to determine the location of the COD in storage (residual address).

3 DCB specification check–Any of the following conditions causes this error:
   a. Word 5 of the DCB (chain address) contains an odd numbered address.
   b. Word 6 of the DCB (byte count) contains a count other than six for a *Start Cycle Steal Status* command.
   c. Word 7 of the DCB (data address) contains an odd numbered address for a *Start Cycle Steal Status* command.
   d. A byte count of zero is specified in the DCB for either a transmit or receive operation.
   e. Bit 2 of the DCB control word is not on for a *Start Cycle Steal Status* command.
   f. Bit 3 of the DCB control word is on.

4 Storage data check–This bit is set on during cycle-steal output operations only. It indicates that the main storage location accessed during the current output cycle contains bad parity. The attachment terminates the operation with an exception interrupt.

5 Invalid storage address–This bit is set on if the address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment terminates the operation with an exception interrupt.

6 Protect check–This bit is set on if the attachment attempts to access a storage location without the correct *cycle-steal address key*.

7 Interface data check–This bit is set on if a parity error is detected during an interface cycle steal data transfer. The condition may be detected by the channel or the attachment. In either case, the attachment terminates the operation with an exception interrupt.

CYCLE STEAL STATUS WORDS

When a cycle-steal data transfer is terminated by an exception condition, bit 0 of the ISB may be set on. If bit 0 is on, further information regarding the cause of the exception condition can be found by executing a *Start Cycle Steal Status* command. The *Start Cycle Steal Status* command may be issued at any time.

The format of the DCB for this command is the same as for a normal cycle-steal data transfer. The chaining bit is not checked by the attachment, but it should be off. The byte count must be six. Six bytes of information are transferred to main storage, starting at the data address contained in DCB word 7.

Word Zero

Word zero contains the main storage address of the last attempted cycle-steal transfer. This residual address may be either a data or a DCB address. When reporting a DCB address, the attachment reports the address of the low order byte of the last DCB word that the attachment attempted to fetch.

Word One

Word one has the following format:

Bit	*Name*
0	Overrun
1	Timeout
2	Modem interface error
3	Block check error
4	Multipoint transmit error
5	Answertone jumper installed
6	Multipoint tributary jumper installed
7	Internal clock jumper installed
8–15	Multipoint address

The bits and their meanings follow.

Bits *Meaning*

0 Overrun–During a receive operation, this condition occurs if the attachment is unable to transfer the contents of the storage data register to main storage before it is time to reload the register. During a transmit operation, an overrun occurs if the attachment is unable to reload the storage data register in time to keep a steady stream of data going out on the line.

1 Timeout–The attachment sets this bit on if:
   a. DSR is not received from the modem within three seconds after an enable terminal operation begins (if bit 12 of DCB word 0 is on)
   b. Character phase is not established within three seconds of acceptance of a receive operation (if bit 12 of DCB word 0 is on)
   c. A continuous sync pattern is received for three seconds
   d. While receiving data, no sync pattern is received for a period of three seconds.

   Timeouts are discussed earlier in this chapter.

2 Modem interface error–Conditions which cause this error are:
   a. DTR or DSR off at the beginning of a transmit or a receive operation
   b. CTS on for more than one second while RTS is off at the beginning of a transmit operation
   c. Loss of DTR or DSR during a transmit or a receive operation
   d. Loss of RTS or CTS during a transmit operation
   e. CTS not returned by the modem within three seconds after the attachment activates RTS.

3 Block check error–The BCC received over the data link does not compare with the BCC accumulated in the attachment. In ASCII mode, an LRC or VRC error is indicated by this bit.

4 Multipoint transmit error–This bit indicates that the attachment is a tributary on a multipoint network and a transmit operation was attempted before the controlling station selected this station.

5 Answertone jumper installed–This bit indicates that the attachment is jumpered to provide an answertone when it senses that the 'ring indicator' line from the modem is active.

6 Multipoint tributary jumper installed–The attachment is a tributary station in a multipoint network.

7 Internal clock jumper installed–The internal clock jumper is installed in the attachment. The attachment provides clocking for 1,200 BPS (600 BPS if "half rate" has been specified in the control word of the DCB).

8–15 Multipoint address–This is the multipoint address for which the attachment is wired.

Bit 8 = MP address bit 0, bit 15 = MP address bit 7.

Note. On single-line attachments, bit 8 (MP address bit 0) being on allows the attachment to IPL the processor, regardless of whether or not the attachment is a multipoint tributary. Bit 0 must not be jumpered on when using ASCII code.

Word Two

Word two contains status information regarding certain key lines of the device and indicates that the following modem lines or conditions are active.

Bit	*Condition sensed*
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4	Ring indicator
5	Half rate selected
6	Transmit mode latch
7	Not used (will be off)
8–15	Indicator panel switch setting

STATUS AFTER RESETS

There are several methods of resetting some or all of the circuits in the attachment. They are:

Reset	*Action*
Power on reset	All attachment components are reset to the off condition.
System reset	All attachment components (except DTR latches and the cycle-steal residual address) are reset to the off condition.
Device reset and Halt I/O	All attachment components (except the DTR latches, prepared level and I-bit latches, and the cycle steal residual address) are reset to the off condition.

Note. On a system reset, device reset, or Halt I/O–the information displayed by indicator panel switch settings /0 through /C is not reset.

JUMPERABLE OPTIONS

The following options can be selected by installing jumper wires on the feature cards.

Binary Synchronous Communications Single-Line Control (Medium Speed)

Internal Clocking

With this jumper installed, the attachment provides clocking at 1,200 BPS or 600 BPS (selectable by programming).

Answertone

With this jumper installed, the attachment provides a three second answertone after the modem activates 'data set ready' in response to the attachment activating 'data terminal ready'. This jumper should not be installed if the modem provides an answertone.

Request To Send

If this jumper is installed, the attachment maintains 'request to send' in an active condition. This eliminates modem "turn-around" when using a full-duplex modem. This option should always be selected when using a modem which always keeps 'clear to send' active.

Data Terminal Ready

If this jumper is installed, the attachment maintains 'data terminal ready' in an active condition. This option must not be selected for switched-line operation.

No Ring Indication

This jumper must be installed if the modem does not provide a ring indication.

Multipoint Tributary

This jumper is installed if the attachment is to be used as a multipoint tributary. It causes the attachment to look for its multipoint address on the receive data line after receiving an initial character synchronization sequence.

Multipoint Address Jumpers

These jumpers establish the multipoint address to which the attachment is to respond.

If bit 0 is jumpered "on", the attachment is allowed to respond to a host initiated IPL sequence–regardless of whether or not the multipoint tributary jumper is installed. Bit 0 must *not* be jumpered "on" when using ASCII code.

For switched-line operation, bit 7 must be jumpered "on", and the multipoint tributary jumper must not be installed.

Binary Synchronous Communications Single-Line Control/High Speed

The high speed attachment provides the following jumperable options which perform functions identical to those described for the medium-speed, single-line attachment:

Request to send
Data terminal ready
Multipoint tributary
Multipoint address

In addition to the above options, the attachment has jumpers to select either an interface compatible with a Western Electric 303 data set (or equivalent) or an interface compatible with C.C.I.T.T. recommendation V.35.

Binary Synchronous Communications 4-Line Adapter

The jumpers on this feature are the same as the jumpers on the medium-speed, single-line attachment except that multipoint address bit 0 has nothing to do with IPL because multiple-line attachments cannot IPL. There are four complete sets of jumpers on each card—one set for each line. There are no option jumpers on the 8-line controller card.

COMMUNICATIONS INDICATOR PANEL

Line Select Switches

The three line select switches are used only with multiple-line attachments. They are used to select a particular line. A line is selected by setting the last three bits of its device address, in binary form, into the line select switches.

These switches are ignored when the indicator panel is used with a single-line attachment.

Function/Select Switches

These switches determine what information is displayed in the indicator lamps. Figures 3-3 and 3-4 are lists of switch settings and the information that is displayed in the indicator lights.

Function/ Display switch setting	*Lamps*	*Information*
00000	0–7	High order byte of DCB word 0 (control word)
00001	0–7	Low order byte of DCB word 0 (control word)
00010	0–7	High order byte of DCB word 5 (chain address)
00011	0–7	Low order byte of DCB word 5 (chain address)
00100	0–7	High order byte of DCB word 6 (byte count)
00101	0–7	Low order byte of DCB word 6 (byte count)
00110	0–7	High order byte of DCB word 7 (data address)
00111	0–7	Low order byte of DCB word 7 (data address)
01000	0–7	High order byte of the storage data register
01001	0–7	Low order byte of the storage data register
01010	5	Interrupt condition code bit 4
	6	Interrupt condition code bit 2
	7	Interrupt condition code bit 1
01011	0–7	ISB
01100	0–7	High order byte of cycle steal status word one
01101	0–7	High order byte of the CRC
01110	0–7	Low order byte of the CRC (or LRC)
01111	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Half rate select
	6	Transmit mode
10000	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Transmit data (on = space)
	5	Receive data (on = space)
	6	Transmit mode
	7	Receive mode

Figure 3-3 (Part 1 of 2). Indicator panel information–Single-line BSC features

Function/ Display switch setting	*Lamps*	*Information*
10001	5	Answer-tone jumper installed
	6	Multi-point tributary jumper installed
	7	Internal clocking jumper installed
10100	0–7	Multi-point address
10110	0	COD
	1	BCC
	2	Text mode
	3	Transparent mode
	4	DLE 1
	5	Character phase
	6	SYN 2
	7	SYN 1
10111	0	Selected mode
	1	Control mode
	2	VRC error
	3	BCC error
	4	ASCII mode
11000	0	Second DC1 } IPL sequence
	1	First DC1 }
	2	Addr 2 (MP address received)
	3	Addr 1 (MP address received)
11010	5	ITB sent or received
	6	EOT/NAK sent or received
11011	3	EOT sent or received
11100	0–7	Lamp test, all lamps should be on
11111	0–7	Same as switch setting 10000. Resets DTR.

Note. Switch settings and lamp indications other than those shown above require knowledge of microcode to understand. Therefore, they are not shown here.

Figure 3-3 (Part 2 of 2). Indicator panel information–Single-line BSC features

Function/ Display switch setting	*Lamps*	*Information*
00000	0–7	High order byte of DCB word 0 (control word)
00001	0–7	Low order byte of DCB word 0 (control word)
00010	0–7	High order byte of DCB word 5 (chain address)
00011	0–7	Low order byte of DCB word 5 (chain address)
00100	0–7	High order byte of DCB word 6 (byte count)
00101	0–7	Low order byte of DCB word 6 (byte count)
00110	0–7	High order byte of DCB word 7 (data address)
00111	0–7	Low order byte of DCB word 7 (data address)
01000	0–7	High order byte of the storage data register
01001	0–7	Low order byte of the storage data register
01010	5	Interrupt condition code bit 4
	6	Interrupt condition code bit 2
	7	Interrupt condition code bit 1
01011	0–7	ISB
01100	0–7	High order byte of cycle steal status word one
01101	0–7	High order byte of the CRC
01110	0–7	Low order byte of the CRC (or LRC)
01111	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Half rate select
	6	Transmit mode
10000	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Transmit data
	5	Receive data
	6	Transmit mode
	7	Receive mode

Figure 3-4 (Part 1 of 2). Indicator panel information–Multiple-line BSC features

Function/ Display switch setting	*Lamps*	*Information*
10001	4	Interrupt pending
	5	Answertone jumper installed
	6	Multipoint tributary jumper installed
	7	Internal clock jumper installed
10100	0–7	Multipoint address
10101	0	Enable timer bit
	1–7	Timer value in 50 millisecond increments
10110	0	COD sent or received
	1	BCC sent or received
	2	Text mode
	3	Transparent mode
	4	DLE sent or received
	5	Character phase
10111	0	Selected mode
	1	Control mode
	2	VRC error
	3	BCC error
11000	2	Address 2 (MP address received)
	3	Address 1 (MP address received)
11001	1	ITB sent or received
	2	EOT/NAK sent or received
	7	EOT sent or received
11100	0–7	Lamp test, all lamps should be on
11101	0–7	First character after character phase in receive
11110	0–7	Contains last COD character sent or received
11111		Resets DTR if it is not jumpered "on"

Note. Switch settings and lamp indications other than those shown require detailed knowledge of the microcode to understand. Therefore, they are not shown here.

Figure 3-4 (Part 2 of 2). Indicator panel information–Multiple-line BSC features

ERROR RECOVERY

Operate I/O Condition Codes

Condition Code 3 (Command Reject)

If condition code 3 is received in response to an *Operate I/O* instruction, check the validity of the command field of the IDCB and retry the instruction. Notify the user if the error persists. Only the following bit combinations are valid:

Prepare command	0110 0000
Device reset command	0110 1111
Start command	0111 XXXX
Read ID command	0010 0000
Halt I/O command	1111 0000
Write command*	010X XXXX

X The attachment does not look at these bits during the *Operate I/O* instruction.

* A BSC attachment cannot execute a write command. The attachment does, however, accept the command. When the *Operate I/O* instruction is completed, the attachment reports "delayed command reject" via an exception interrupt with ISB bit 1 set on.

Condition Code 5 (Interface Data Check)

This error occurs if either the processor channel or the attachment detects a parity error on the interface. Retry the instruction three times. Notify the user if the error persists. This error indicates a malfunction in the hardware.

Interrupt Condition Codes

Interrupt condition code 4 (attention) indicates that the 'ring indicator' line from the modem is active. Condition codes 5–7 indicate that the 'ring indicator' line is active in conjunction with another interrupt causing condition.

Condition Codes 2 or 6 (Exception)

Examine the ISB to determine the cause of the interrupt. If bit zero of the ISB is on, issue a *Start Cycle Steal Status* command to determine the cause of the interrupt. See "Interrupt Status Byte" and "Cycle Steal Status Words" for explanation of the exception conditions.

Storage Data Check. Reset the attachment and retry. Notify the user if the error persists.

Interface Data Check. Reset the attachment and retry. Notify the user if the error persists.

DCB Specification Check. Verify the correctness of the DCB address, the data address, the chain address, and the cycle-steal address key; then reissue the command. If the error persists, notify the user.

Invalid Storage Address. Use the same procedure as for a *DCB specification check.*

Protect Check. Use the same procedure as for a *DCB specification check.*

Chapter 4. Synchronous Data Link Control Single-Line Control Feature

Section One. Product Description

The Synchronous Data Link Control (SDLC) Single-Line Control feature is an option which controls transfer of serial data to and from a remote terminal or host system via a modem and communications line facility. In this chapter, this feature is referred to as the *attachment*. The SDLC attachment can be used for connecting a Series/1 processor to telecommunication equipment or other processors having compatible adapters.

There are several important items to consider about the SDLC attachment. They are:

- Data transmission uses synchronous data link control procedures
- Any eight-bit data codes may be used
- It is available as a single-line, medium-speed, half-duplex attachment *only*
- Bit rates can be up to 9,600 BPS
- It may be used as either a primary or secondary station
- Internal clocking is available
- NRZI coding is used with internal clocking
- NRZ coding or NRZI coding may be used with external clocking (supplied by the modem)
- Answertone generation can be provided by installing a jumper on the attachment card
- The attachment does not support station-address-field extensions or control-field extensions.

Data transmission is serial-by-bit, using the synchronous data link control (SDLC) method of character and bit transmission. A general discussion of SDLC procedures may be found in *IBM Synchronous Data Link Control–General Information,* GA27-3093.

The attachment can communicate with host systems or terminals using EBCDIC (Extended Binary-Coded Decimal Interchange Code) or ASCII (American Standard Code for Information Interchange) or any other eight-bit data codes. SDLC uses a specific set of line control characters, but because transparency is inherent in SDLC, the data characters can be any eight-bit code that the sending and receiving stations agree upon.

The SDLC attachment is a single-line half-duplex device that can operate on a switched or non-switched line at rates up to 9,600 BPS (using external clocking).

Internal (business machine) clocking can be connected during installation if the modem does not supply clocking. The characters are transmitted and received using NRZI (non-return-to-zero inverted) coding if internal clocking is used. When clocking is provided by the modem, either NRZ or NRZI coding may be selected by the software. Internal clocking provides the strobe pulses used to strobe bits between the modem and the adapter. In receive mode, it also establishes and maintains bit synchronization through an advance or retard of the data strobe. Transmission rates of 600 or 1,200 bits per second are available through the internal clocking feature.

SDLC FEATURE CONFIGURATIONS

The SDLC attachment is contained on a single card which can be installed in any I/O card slot in the processor enclosure or in an Input/Output Expansion Unit.

The attachment is available only in a single-line, half-duplex configuration.

Connections to the modem and the indicator panel are made by top card connectors.

DATA TRANSMISSION CODES

The SDLC attachment allows data communications using any eight bit data code including EBCDIC or ASCII. The EBCDIC and ASCII character assignments are shown in Appendix A.

DATA FLOW

Each character occupies a byte position in storage. Transfers to and from storage are two bytes at a time, except that the first and/or last transfers may move only one byte if specified by the data address or byte count.

Transmit

Transmission data is fetched from storage two characters at a time. The high order byte holds the first character to be sent and the low order byte holds the next character. After a character has been transferred into *Serdes*, it is transmitted over the line serially, low order bit first. Figure 4-1 illustrates the data flow.

Note. If the data address (DCB word 7) is odd, only one character is fetched from storage on the first data transfer.

Receive

The first bit received is transferred into the low order bit position of a byte, the second bit received is transferred into the next higher bit position, and so on, until a character is assembled. The first character received is loaded into the high order byte of the storage data register and the next character is loaded in the low order byte. The attachment provides buffering for four bytes of data. This allows the attachment to recognize an ending flag without putting the FCS (Frame Check Sequence) into storage. Data is written into main storage without any code translation.

Note. If the data address (DCB word 7) is odd, only one character is sent to storage on the first data transfer.

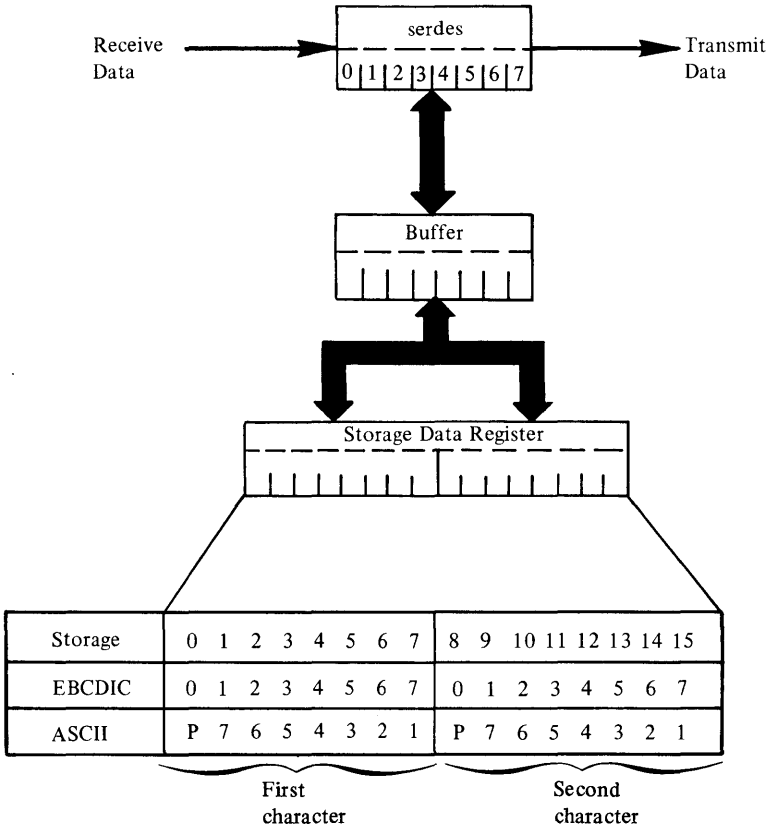
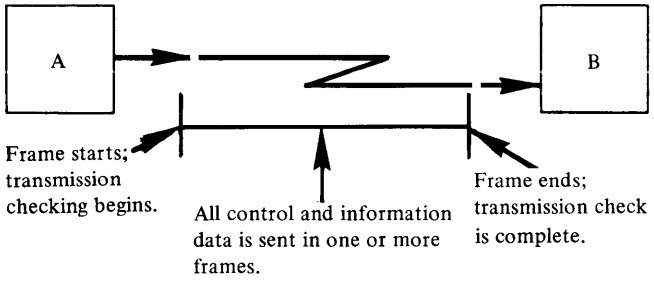


Figure 4-1. SDLC Attachment Data Flow

CONTROL CHARACTERS AND SEQUENCES

Two levels of information grouping are incorporated in SDLC procedures. The basic level, called a *frame*, is checked by the attachment for transmission errors. The frame is the vehicle for every command, every response, and all information that is transmitted using SDLC procedures.

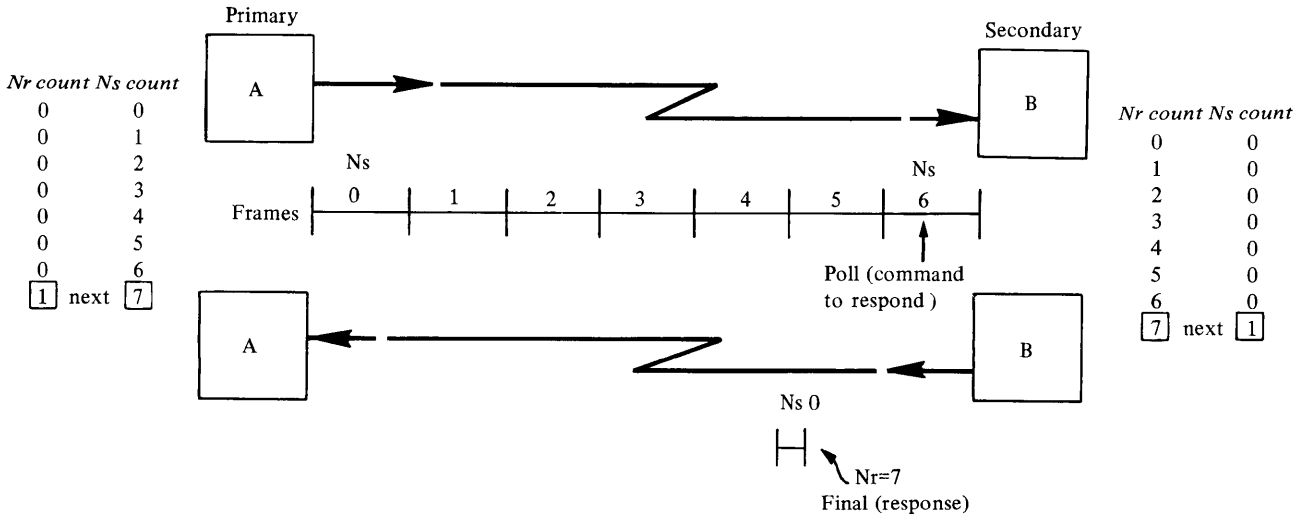


The higher level of grouping, a frame sequence, is checked by the software for missing or duplicated frames. The software at a station transmitting sequenced frames counts and numbers each sequenced frame. This count is known as Ns. The software at a station receiving sequenced frames counts each error-free sequenced frame that it receives; the receiver count is called Nr.

The software advances the Nr count when a frame is checked and found to be error-free. Nr then becomes the count of the "next-expected" frame and should agree with the next incoming Ns count. If the incoming Ns does not agree with Nr, the frame is out of sequence and Nr does not advance. Out-of-sequence frames may be rejected or saved, at the option of the software. The receiving software does, however, accept the incoming Nr count (confirmation) if the out-of-sequence frame is otherwise error free.

The counting capacity for Nr or Ns is 8, using the digits 0 through 7. These counts can "wrap around," that is, 7 is sequentially followed by 0. Up to seven frames may be sent before the receiver reports its Nr count to the transmitter because it may be necessary to repeat some or all of them. The reported Nr count is the sequence number of the next frame that the receiving software expects to receive, so if, at a checkpoint, it is not the same as the transmitter's next sequence number, some of the frames already sent must be repeated.

The Nr and Ns counts of both stations are initialized to 0 at the discretion of the primary station. At other times, the counts advance as sequenced frames are sent and received.



If B responds with Nr =:	*A may send, on request, Ns frames :*
7 (as above, all frames check OK)	7, 0, 1, 2, 3, 4, 5 (continue)
6 (frame 6 discarded because of error)	6, 7, 0, 1, 2, 3, 4 (retransmit and continue)
5 (error on frame 5, 5 and 6 discarded)	5, 6, 7, 0, 1, 2, 3 (retransmit and continue)
4 (error on frame 4, 4–6 discarded)	4, 5, 6, 7, 0, 1, 2 (retransmit and continue)
3 (error on frame 3, 3–6 discarded)	3, 4, 5, 6, 7, 0, 1 (retransmit and continue)
2 (error on frame 2, 2–6 discarded)	2, 3, 4, 5, 6, 7, 0 (retransmit and continue)
1 (error on frame 1, 1–6 discarded)	1, 2, 3, 4, 5, 6, 7 (retransmit and continue)
0 (error on frame 0, no frames accepted)	0, 1, 2, 3, 4, 5, 6 (retransmit)

FRAME FORMAT (F, A, C, I, FCS, F)

All active communications regulated by SDLC procedures have a format called a frame. Each frame is enclosed in *flags*.

Starting from the beginning flag as a reference point, eight consecutive binary bits are dedicated to the address (A) of the secondary station. The next eight consecutive bits comprise the control (command or response) information (C). At least 16 more bits are transmitted after the C-field before the ending flag is sent. These 16 bits (FCS) contain the transmission checking information. Thus, the internal structure of any valid frame must consist of at least 32 consecutive binary bits.

Any information field (I) is sent following the C (control) field and preceding the FCS field. The I-field is not restricted in format or content. In a frame with an I-field, the maximum length is not restricted by procedures. The practical limitation is the maximum transmission length that can be expected to arrive at the receiver error-free most of the time, using the particular communications channel.

The transmission check at the receiver is complete when the ending flag is recognized. The receiving attachment separates I from FCS information when the ending flag is received, and does not put the FCS into storage.

Flag

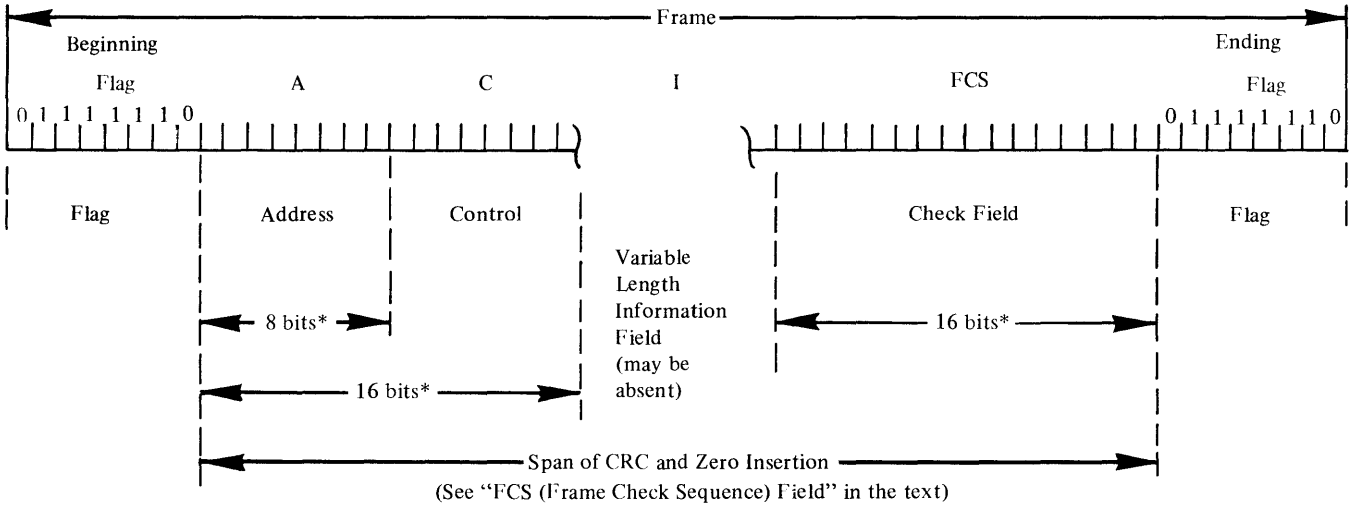
Two flags, the beginning flag and the ending flag, enclose the SDLC frame. The beginning flag serves as a reference for the position of the A (address) and C (control) fields and initiates transmission error checking; the ending flag terminates the check for transmission errors. Both beginning and ending flags have the binary configuration 01111110. The bit-orientation of SDLC allows the flag to be recognized at any time.

A flag may be followed by a frame, by another flag, or by an idle condition.

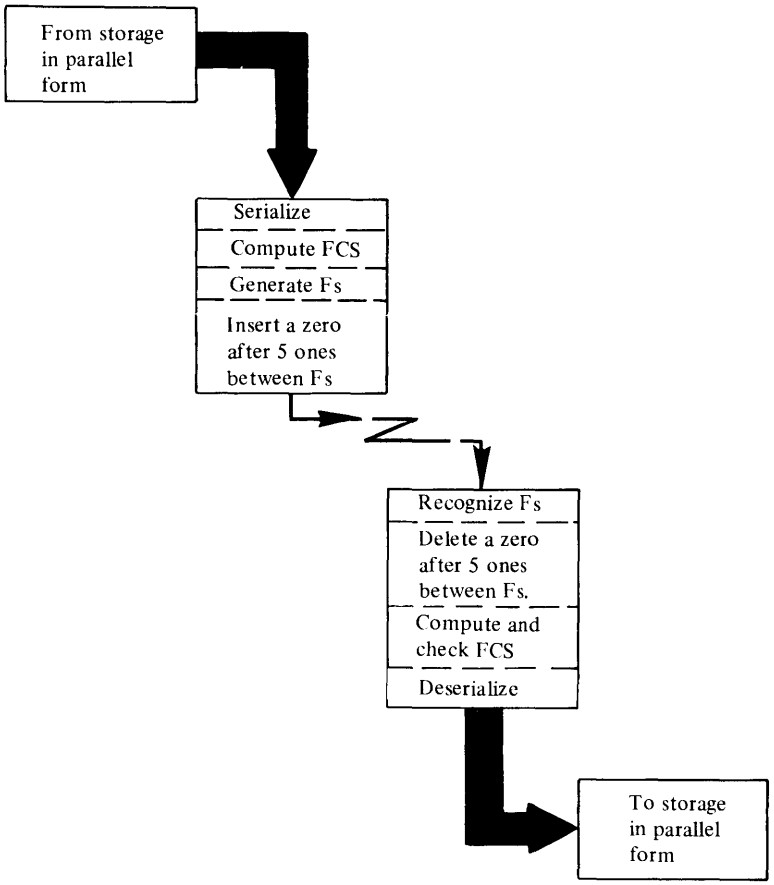
Zero Insertion

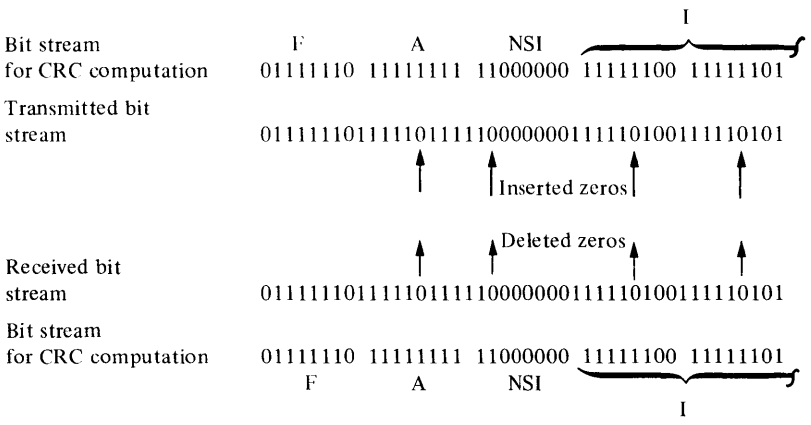
A frame is identifiable because it begins with a flag and contains only non-flag bit patterns. (The frame ends at the next flag.) This characteristic does not restrict the contents of a frame because SDLC procedures require that a binary 0 must be inserted by the transmitter after any succession of five contiguous 1s within the frame. Thus, no pattern of 01111110 (flag) is ever transmitted by chance. After testing for flag recognition, the receiver removes a 0 that follows a received succession of five contiguous 1s. The attachment automatically provides zero insertion and deletion. Inserted and removed zeros are not included in the transmission error check. (A 1 that follows five 1s is not removed.)

Note. When NRZI transmission coding is used, zero insertion eliminates the remaining possibility of prolonged transitionless periods in the active state.



*excluding inserted zeros





Idle Stations

A series of contiguous flags may be transmitted by a station to maintain bit synchronism and to maintain the data link in an active state. A series of flags may also be used to hold the authority to transmit and to avoid timeouts at the linked station(s).

Note. The use of NRZI transmission coding and zero insertion is restricted to the active state of the data link; neither one operates in the idle state.

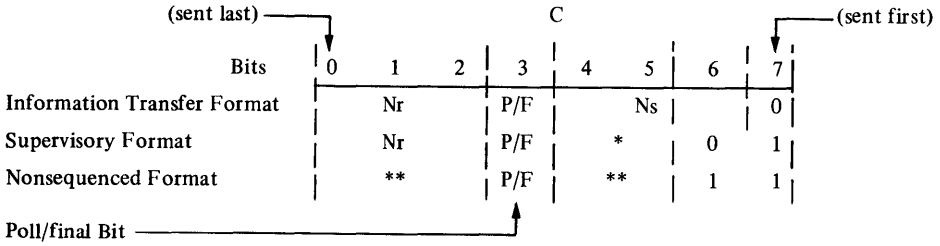
Address Field

The primary station manages a data link by issuing commands to which secondary stations respond. The primary station is never identified, but the secondary station is always identified; this is the function of the address field (A).

A primary station can address all secondaries by sending an *all ones* address (hex FF). Thus, a secondary station may receive a common address or its individual address. However, when a secondary station sends any response, only its individual address is used.

Control Field and the P/F Bit

The control field (C) contains, within its eight binary digits, the capability for encoding the commands and responses required to control a data link. The C-field has three formats, as shown below.



* Codes for supervisory commands/responses

** Codes for nonsequenced commands/responses

Each C-field format contains the format identifier and p/f bits. The codes for the C-field commands and responses are shown below.

Format (Note 1)	*Sent Last* — *Binary Configuration* — *Sent First*	*Acronym*	*Command*	*Response*	*I-Field Prohibited*	*Resets Nr and Ns*	*Confirms frames through Nr-1*	*Defining Characteristics*
NS	000 P/F 0011	NSI	X	X				Command or response that requires nonsequenced information
	000 F 0111	RQI		X	X			Initialization needed; expect SIM.
	000 P 0111	SIM	X		X	X		Set initialization mode; the using system prescribes the procedures.
	100 P 0011	SNRM	X		X	X		Set normal response mode; transmit on command.
	000 F 1111	ROL		X	X			This station is offline.
	010 P 0011	DISC	X		X			Do not transmit or receive information.
	011 F 0011	NSA		X	X			Acknowledge NS commands.
	100 F 0111	CMDR		X				Nonvalid command received; must receive SNRM, DISC, or SIM.
	101 P/F 1111	XID	X	X				System identification in I field.
	001 0/1 0011	NSP	X		X			Response optional if no P-bit.
	111 P/F 0011	TEST	X	X				Check pattern in I field.
S	Nr P/F 0001	RR	X	X	X		X	Ready to receive.
	Nr P/F 0101	RNR	X	X	X		X	Not ready to receive.
	Nr P/F 1001	REJ	X	X	X		X	Transmit or retransmit, starting with frame Nr.
I	Nr P/F Ns 0	I	X	X			X	Sequenced I-frame.

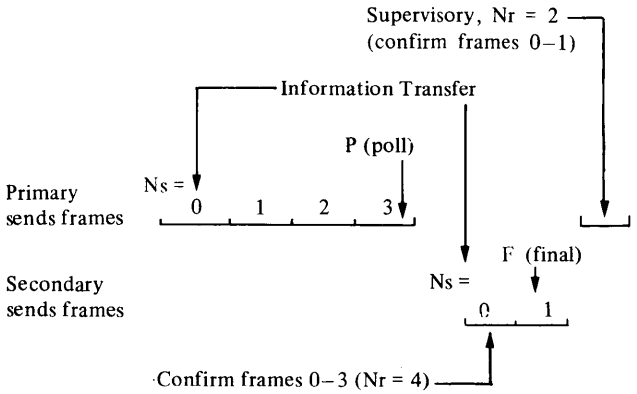
Note 1. NS = nonsequenced, S = supervisory, I = information.

The p/f bit is the send/receive control. A p (poll) bit is sent to a secondary station to authorize transmission; an f (final) bit is sent by a secondary station in response to the p-bit. (Do not confuse the f-bit with the F (flag) frame delimiter pattern.) Normally, only one p-bit is outstanding (unanswered by a final bit) on a data link.

Information Transfer Format

A C-field in this format is a part of each sequenced frame that is transmitted over a data link. It contains the p/f bit and the Nr and Ns counts.

Stations transmitting information-transfer frames request confirmation by sending the Ns count; they confirm by sending the Nr count.



Supervisory Format

This format is an adjunct to the information transfer format. Frames containing a C-field of the supervisory format convey ready or busy conditions and may be used to report sequence errors (thus requesting retransmission). Such frames may be interspersed with frames having a C-field of the information transfer format. Whether or not a primary station has information data to transmit, it may use a frame having a C-field of the supervisory format to poll a secondary station; a secondary station may use the supervisory format to respond to a request for confirmation. Frames with a supervisory format C-field are not counted in the Nr or Ns counts.

Nonsequenced Format

Command and response frames having a C-field of this format are used for data link management. Data link management includes activating and initializing secondary stations, controlling the response mode of secondary stations, and the reporting of procedural errors (not recoverable by retransmission). Information data may also be transmitted, using a frame with a C-field of the nonsequenced format. Frames with a nonsequenced format C-field are not counted in the Nr or Ns counts.

Information Field

SDLC procedures are designed as a vehicle for data contained in the information field (I). The I-field contains data that is moved, via the data link, from place to place in the system. The I-field is unrestricted in format or content; its contents are transparent (invisible) to the components of data link control.

An information field is normally included with every frame having a C-field of the information transfer format. These information transfer frames are the only ones that are sequenced.

There are provisions for an I-field in frames with a nonsequenced format C-field, but these are unprotected by sequence checking.

FCS (Frame Check Sequence) Field

The FCS-field (also called BCC, for *Block Check Character*) contains 16 binary digits. It follows the I-field (if there is one; the C-field, if not) and immediately precedes the ending flag. These 16 digits result from a mathematical computation on the digital value of all binary bits (excluding inserted zeros) within the frame; the purpose is to validate transmission accuracy.

The transmitting SDLC attachment performs the computation and sends the resulting FCS value. The receiving SDLC attachment performs a similar computation and checks its results. The receiving software discards a frame that is found to be in error and does not advance its Nr count.

SYNCHRONIZATION

The basic SDLC attachment receives timing pulses from the modem. This establishes and maintains bit synchronization. Upon starting to transmit, the attachment automatically transmits a flag character. This establishes frame and byte synchronization.

Some modems, in order to operate properly, may require NRZI encoded data and/or pad characters. Bits 9 and 12 of the DCB control word can be used to satisfy particular modem requirements.

If internal clocking is used, the attachment automatically sends two pad characters (hex 00) prior to sending the beginning flag. This causes 16 bit transitions to take place before the flag character is sent.

When NRZI coding is used, zero insertion eliminates the possibility of prolonged transitionless periods.

TIMERS

The attachment has two progammable timers. Each timer can count up to 27 seconds, in 106 millisecond increments. Bits 0–7 of DCB word 1 control one timer; bits 8–15 control the second timer.

Timer 1

Timer 1 can be used in a variety of ways. Following is a list of the uses of this timer.

- Idle Detect Timer–If a receive operation is specified and bits 0–7 of DCB word 1 contain a value other than zero, the attachment runs timer 1 for the duration specified by bits 0–7 of DCB word 1. When this time expires, the attachment begins checking the line for an idle condition. If an idle condition is detected, the attachment presents an exception interrupt.

  If a flag character is detected while timer 1 is running, the attachment immediately begins checking for an idle condition.

  If software assigns a value of zero to timer 1, the attachment does not check for an idle condition.
- Data Set Ready Timeout–During an "enable terminal" operation, this timeout occurs if 'data set ready' is not returned by the modem within the specified time. If the condition of the 'rate select' line will be changed during the enable terminal operation, this timer must be set to a value that will allow the modem enough time to equalize. Consult the manual for the modem being used to determine equalization time.
- Disable Data Terminal Ready Timeout–During a "disable terminal" operation, a timeout occurs if 'data set ready' is not deactivated within the specified time.
- Clear to Send Timeout–During a transmit operation, a *modem interface error* occurs if 'clear to send' is not returned by the modem within the specified time.
- Program Delay–When the operation is not an "enable terminal," a "disable terminal," a "receive" or a "transmit" operation, timer 1 can be used by the software for timing purposes.

Timer 2

Timer 2 is used in two ways:

- Nonproductive Receive Timeout–This timeout is used only during receive operations. Its purpose is to limit the time the attachment will wait for a frame to begin. If a frame does not start before timer 2 expires, the attachment presents an exception interrupt. The timer does not run if the receive line is being held active (continuous flags).
- Hold-line-active Timer–When timer 2 is used in conjunction with a transmit operation with bit 15 on in the DCB control word, the attachment transmits flag characters for the duration of the time specified by bits 8–15 of DCB word 1, or until another transmit operation begins.

Note. When the timers are set to zero, no timeout occurs.

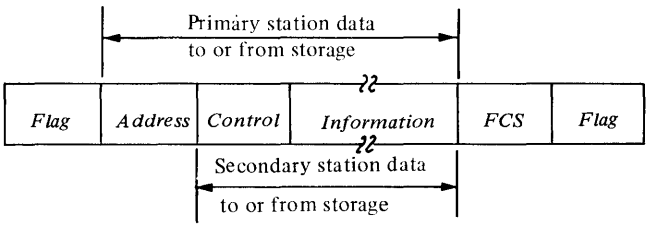
OPERATING MODES

Monitor Mode

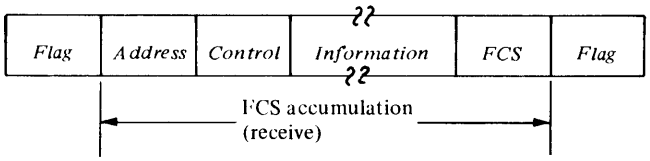
The attachment is placed in monitor mode by a receive command. While in this mode, the attachment is constantly monitoring the line, looking for a flag character. If the attachment is operating as a primary station, it immediately goes into receive mode upon recognizing a flag character. If the attachment is operating as a secondary station, it checks the address following the flag. If the address is its own (or the broadcast address), the attachment goes into receive mode. If the address is not the address of the attachment, the attachment remains in monitor mode.

Receive Mode

When the attachment is operating as a secondary station in receive mode, data is transferred to main storage beginning with the control field. If the attachment is operating as a primary station, data is transferred to main storage beginning with the address field. If the attachment is operating as a secondary station, the attachment automatically checks the received address to determine if the frame is intended for this station. If the frame is intended for this station, the attachment transfers the data (beginning with the control-field) to storage.

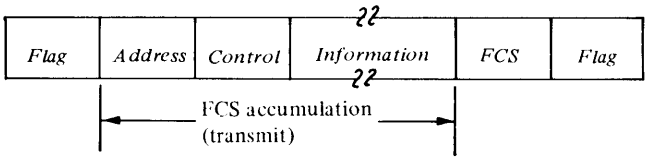


The FCS accumulation starts with the address and includes the FCS received.



Transmit Mode

This mode is established when a transmit command has been issued by the program. FCS accumulation begins with the first character to be transmitted after the beginning flag character and continues until the byte count (DCB word 6) is decremented to zero.



The FCS is then automatically transmitted, followed by a flag character.

If the attachment is operating as a primary, the address of the receiver comes from storage. If the attachment is operating as a secondary, the hardware provides the address field of the frame.

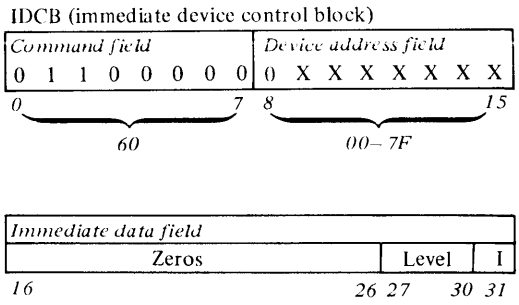
COMMANDS

The Operate I/O instruction points to the IDCB which contains one of the following commands.

- Prepare
- Device Reset
- Start
- Start Cycle Steal Status
- Read ID
- Start Diagnostic 1 or 2

Prepare

The *Prepare* command is used to control the interrupt parameters of the addressed device. The data word contains the level and I-bit. The device is always able to accept and execute a *Prepare* command, even if it is busy or has an interrupt pending from a previous command. The IDCB for the *Prepare* command has the following format:



Level. This four bit field specifies the priority interrupt level assigned to the device. The binary value of bits 27–30 indicates priority levels of 0–3.

Example:

0000 = level 0, 0001 = level 1,
0010 = level 2, 0011 = level 3.

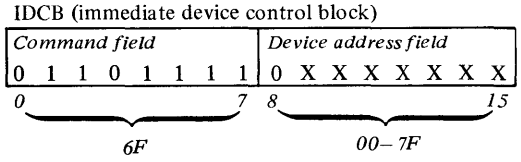
I. This bit determines whether the device is allowed to request an interrupt. An I-bit value of 1 permits the device to request an interrupt, and a value of 0 prevents it.

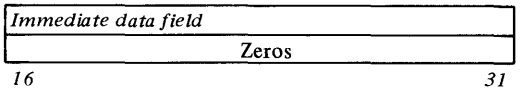
The attachment stores the level data and presents it to the processor each time the attachment presents an interrupt request. The prepare information (level and I-bit) is reset by a system reset, or a power-on reset.

Device Reset

This command resets the addressed device. Any pending interrupts are cleared. The prepared level, I-bit, residual address, and 'data terminal ready' are not reset by this command. The *Device Reset* command has the following format:

IDCB (immediate device control block)

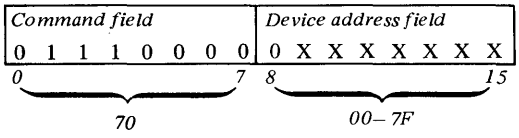


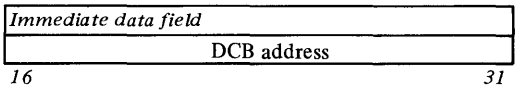


Start

This command transfers the address of a DCB to the attachment. When the *Start* command is accepted, the attachment fetches the DCB from the main storage address specified in the immediate data field of the IDCB, and begins executing the operation.

IDCB (immediate device control block)

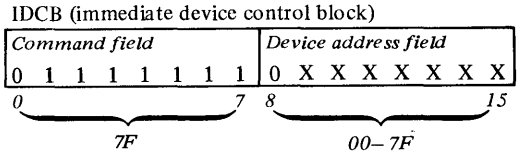


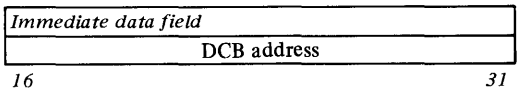


Start Cycle Steal Status

This command causes the attachment to transfer status information (relative to the previous cycle-stealing operation) to main storage. The attachment provides four words of cycle-steal status information. The byte count specified in word 7 of the DCB must be eight.

IDCB (immediate device control block)



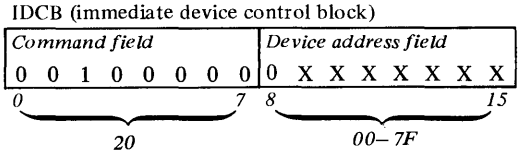


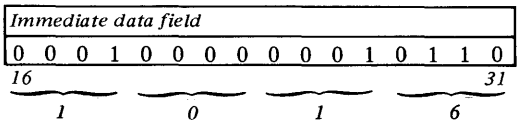
See 'Cycle Steal Status Words' (later in this chapter) for a description of the status information.

Read ID

This command transfers the attachment's identification word from the attachment to the immediate data field of the IDCB. The ID word of the SDLC attachment is shown below as it appears in the immediate data field of the IDCB.

IDCB (immediate device control block)

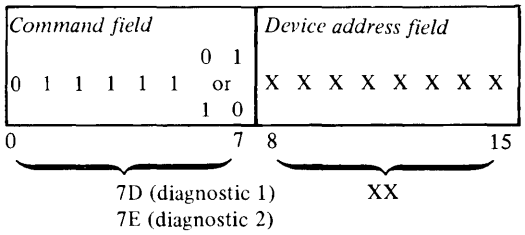


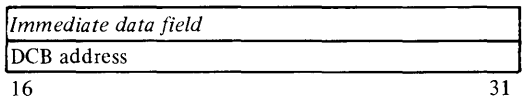


Diagnostic Commands

There are two diagnostic commands. They are used by diagnostic programs to determine if the attachment is operating properly. These commands are called *Start Diagnostic 1* and *Start Diagnostic 2.* For a full explanation of these commands, refer to chapter 5 of *IBM Series/1 4955 Processor–Theory Diagrams*, SY34-0041; or *IBM Series/1 4953 Processor–Theory Diagrams*, SY34-0042.

IDCB (immediate device control block)



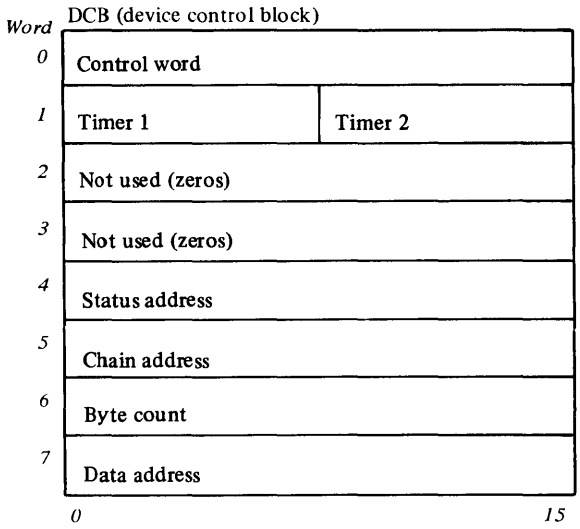


DEVICE CONTROL BLOCK (DCB)

The DCB is an eight word area in main storage which describes the specific parameters of the cycle-stealing operation. Its location in storage is assigned by the program. The data in its words is loaded and changed by the program. It is fetched by the attachment, using a *cycle-steal address key* of zero, after successful execution of a *Start* command, or a *Start Cycle Steal Status* command.

The DCB address transferred to the attachment via the IDCB points to word 0 of the DCB. The DCB address must be even. If the DCB address is odd, the attachment sets Interrupt Status Byte (ISB) bit 1 (delayed command reject) on and terminates the operation with an exception interrupt (condition code 2). The format of the DCB is shown below. Words 1–5 are ignored during a *Start Cycle Steal Status* command.

DCB (device control block)



Control Word

This word delineates the cycle-stealing operation. The format of the control word is:

Bit	*Name*
0	Chaining flag
1	Not used–must be zero
2	Input flag 0 = output 1 = input or receive
3	Not used–must be zero
4	Suppress exception (SE)
5–7	Cycle steal address key
8	Half rate
9	NRZI coding
10	Enable terminal
11	Disable terminal
12	Pad (leading)
13	Secondary/primary 0 = secondary 1 = primary
14	Transmit operation
15	Hold line active (HLA)

Bit	*Meaning*
0	Chaining flag–If this bit is on, the next DCB in the chain is fetched after the successful completion of the current DCB operation. If this bit is off and the operation is successfully completed, the attachment presents a normal ending interrupt.
1	Not used–must be zero.
2	Input flag–This bit indicates the direction of data transfer relative to main storage. Bit 2 off = output (storage to attachment), Bit 2 on = input (attachment to storage). On a *Start* command, a receive operation is specified by this bit being on. This bit must be on for a *Start Cycle Steal Status* command. Receive operation–This operation allows the attachment to begin transferring received data to the processor after synchronization is established. The ending conditions for a receive operation are dependent on several factors: a. The setting of the chaining flag (bit 0) b. The setting of the *suppress exception* bit (bit 4) c. The condition of the p/f (poll/final) bit in the current frame d. Whether any errors occurred in the frame. There are two general types of errors: *suppressible* and *non-suppressible*. Non-suppressible errors always cause an exception interrupt (condition code 2). All errors except the following four are non-suppressible. 1. Overrun 2. Aborted frame 3. Incorrect length record 4. Block check error The action taken when a suppressible error occurs depends on the setting of the suppress exception (SE) bit. If the SE bit is off, the attachment presents an exception interrupt (CC2) and posts the cause of the error in the ISB or *Cycle Steal Status Words*. If the SE bit is on, the attachment posts the error in the Residual Status Block and either presents a device end interrupt (CC3) with IIB bit 0 on or chains to the next DCB. Bits 0–7 of DCB word 1 can be used in conjunction with the receive operation to specify a time after which the attachment will begin checking the line for an idle condition. If an idle condition is detected, the attachment sets bit 5 on in cycle-steal status word 2 and bit 0 on in the ISB, and presents an exception interrupt. Bits 8–15 of DCB word 1 can be used in conjunction with the receive operation to specify the nonproductive receive timeout period.
3	Not used–must be zero.
4	Suppress exception (SE)–This bit is used with receive operations only. When this bit is on, the attachment does not present an exception interrupt upon detecting incorrect length records, aborted frames, overruns, or block check errors. Instead, at the end of the operation, the attachment stores two words of information into the *Residual Status Block*, beginning at the address specified in the *Status Address* (DCB word 4). The first word contains the residual byte count. The second word contains the residual status flags. See the description of the *Status Address* (DCB word 4) for a description of the residual status block.
5, 6, 7	Cycle-steal address key–This is a three bit key presented to the processor by the attachment during data transfers so that the processor can ascertain whether the attachment is authorized to access certain blocks of main storage.

	Conditions			*Results*				
	Chn bit	*SE bit*	*p/f bit*	*Int CC*	*IIB bit 0*	*Chain occur*	*Post resid. status*	*EOC bit* **
No errors	0	0	0	3	0	no	no	n/a
	0	0	1	3	0	no	no	n/a
	0	1	0	3	0	no	yes	1
	0	1	1	3	0	no	yes	1
	1	0	0	n/a	n/a	yes	no	n/a
	1	0	1	2	*	no	no	n/a
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	0	no	yes	1
Suppressible errors	0	0	0	2	*	no	no	n/a
	0	0	1	2	*	no	no	n/a
	0	1	0	3	1	no	yes	1
	0	1	1	3	1	no	yes	1
	1	0	0	2	*	no	no	n/a
	1	0	1	2	*	no	no	n/a
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	1	no	yes	1

* When condition code 2 is reported the IIB is called the ISB and bit 0 has a different meaning. See Interrupt Status Byte for a description of ISB bits.

** See *Status Address* (DCB word 4) for a description of this bit.

8 Half rate–The attachment only recognizes this bit during the Enable Terminal operation; and then only if 'data set ready' is already on. This bit causes the modem to operate at one-half of its normal bit rate (if the modem is equipped to do so). If internal clocking is being used, this bit selects the 600 BPS bit rate. If changing bit rates, when using modem clocking, timer 1 (bits 0–7 of DCB word 1) should be set to allow enough time for the modem to equalize. The attachment will not change rates if timer 1 is set to zero, regardless of whether internal clocking or modem clocking is being used.

9 NRZI coding–This bit causes the attachment to use and recognize NRZI coding. When the internal clocking feature is used, NRZI is automatic and this bit is ignored.

10 Enable terminal operation–This bit causes the attachment to activate the 'data terminal ready' line. A device end interrupt occurs or a chaining operation begins 50 milliseconds after the modem activates 'data set ready'.

Timer 1 may be used in conjunction with this operation to limit the time that the attachment waits for 'data set ready' to become active. If 'data set ready' fails to become active within the specified time, the attachment resets DTR and presents an exception interrupt with bit 0 set on in the ISB.

For manual answer or manual call sequences, this bit must be used to turn 'data terminal ready' on prior to entering data mode. On leased lines, 'data terminal ready' can be jumpered "on."

Programming note. When the modem presents a ring indication, the attachment presents an attention interrupt (condition code 4) and waits 50 milliseconds for the program to perform an enable terminal operation. If after this time the program has not enabled DTR, the attachment will present another attention interrupt (provided that the ring indication is still active).

11 Disable terminal operation–This bit causes the attachment to deactivate the 'data terminal ready' line in order to disconnect from a switched network. Timer 1 can be used in conjunction with this operation to limit the time that the attachment allows for 'data set ready' to drop. If 'data set ready' does not deactivate within the specified time, an exception interrupt occurs with ISB bit 0 set on. A device end interrupt occurs or a chaining operation begins 50 milliseconds after the attachment detects that the 'data set ready' line has been deactivated.

12 Pad–This bit is used only with a transmit operation. If this bit is on, the attachment automatically transmits two pad characters prior to transmitting the first flag character of the first frame. For NRZ code the pad character is a hexadecimal 55. For NRZI code the pad character is a hexadecimal 00.

13 Secondary/primary–This bit determines whether the attachment will operate as a primary or secondary station. On a receive operation, the attachment examines the address portion of a received frame only if the attachment is being used as a secondary station. On a transmit operation the attachment generates its own address only when it is operating as a secondary station. Bit 13 on = primary, bit 13 off = secondary.

14 Transmit operation–The attachment begins this operation by activating 'request to send', then waiting for 'clear to send' to become active. Upon receiving 'clear to send', the attachment transmits the beginning flag character and starts transmitting the data. When the byte count is decremented to zero, the attachment automatically transmits the FCS and the ending flag character. Thus, one DCB causes one frame to be transmitted.

If bit 0 (the chaining flag) is on, the attachment fetches the next DCB and starts the next frame. If bit 15 (hold line active) is off and the attachment is unable to fetch the chained-to DCB in time to cause the next frame to immediately follow the preceding frame, the attachment deactivates 'transmit mode' and the transmission line goes into an idle condition. The next DCB is then treated as a normal transmit operation. Bit 15 (hold line active) can be used to eliminate the possibility of the line idling between frames.

If bit 0 and bit 15 are off and the modem delay jumper is installed, the attachment automatically transmits trailing pad characters (hex FF) for two milliseconds after the ending flag character. The attachment then exits transmit mode and resets 'request to send'.

15 Hold line active–This bit is used in conjunction with bit 14 (transmit operation). If bit 15 is on when the byte count goes to zero, the attachment stays in transmit mode and transmits flag characters until another operation begins or until the time specified in timer 2 passes. If the program sets timer 2 to zero, the line is not held active.

Timers

This word is used to specify the timeout periods of the timers. See 'Timers', previously described in this chapter.

Status Address

This word is used in conjunction with bit 4 (SE) of the control word. Bit 4 of the control word and the status address are used only on receive operations. The address this word contains is the main storage address of the *residual status block*. If bit 4 of the control word is on and the attachment detects any of the conditions that set residual status flags, an exception interrupt does not occur. Instead, the attachment automatically stores two words of information into the *residual status block* and monitors the line, looking for an ending flag character. When the ending flag is detected, the attachment presents a normal device end interrupt or begins a chaining operation. The first word stored in the residual status block is the residual byte count; the second word contains the residual status flags.

Residual Status Flags

The second word of the *residual status block* contains the residual status flags. The bits have the following meanings:

Bit	*Meaning*
0	End of chain (EOC)–This bit indicates that no further chaining will take place. This is usually a result of the attachment receiving a frame in which the p/f bit is on. This bit is also set if the SE bit is on and the chaining flag is off.
1–7	These bits are not used and will be zero.
8	Overrun–This condition occurs if, during a receive operation, the attachment is unable to transfer the contents of the storage data register to the processor before it is time to load another word of data into the storage data register.
9	Abort–This condition occurs if, during a receive operation, the attachment detects an abort condition. An abort condition is eight contiguous 1 bits received after the beginning of a frame.
10	Long frame–This bit indicates that the byte count has been decremented to zero and the current frame has not ended. The attachment continues to monitor the receive line until the end of the frame. However, any data received after the byte count reaches zero is lost.
11	Block check error–The frame check sequence received is incorrect.
12–14	These bits are not used and will be zero.
15	No exception (NE)–This bit indicates either of two conditions. The first condition is that the frame was of the correct length and error free. The second condition is that the attachment received an error free but short frame. To determine which condition caused this bit to be set, examine the residual byte count. If the residual byte count is not zero, a short frame was received.

Chain Address

This word contains the storage address of the next DCB and is used when chaining is indicated (bit 0 of control word on). The chain address must be even. If the address is odd, the attachment sets ISB bit 3 on and terminates the operation.

Byte Count

This 16 bit word contains the number of bytes to be transferred during the operation specified in the current DCB control word.

Data Address

This is the address in main storage where data transfer starts.

INTERRUPT INFORMATION BYTE (IIB)

When the attachment presents an interrupt to the processor, the IIB is used to record information that cannot be indicated to the program via condition codes. IIB bit 0 being on when condition code 3 is reported indicates that the suppress exception bit was on for the previous receive operation and that a suppressible error has been suppressed.

When interrupt condition codes 2 or 6 are reported, the IIB has a fixed format called the *Interrupt Status Byte* (ISB).

Interrupt Status Byte (ISB)

The ISB is meaningful only when interrupt conditions codes 2 or 6 are reported. The processor sees the ISB in bits 0–7 of the *interrupt ID word.* The format of the ISB is:

Bit	*Name*
0	Device dependent status available
1	Delayed command reject
2	Incorrect length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Bit	*Meaning*
0	Device dependent status available–If this bit is on, additional status is available via the *Start Cycle Steal Status* command. A discussion of this status follows in this chapter.
1	Delayed command reject–This bit is set on under the following conditions: a. The command field of the IDCB contains an invalid function/modifier bit combination. b. The immediate data field of the IDCB contains an odd numbered DCB address.
2	Incorrect length record–This error is reported only during receive operations and only when bit 4 of the DCB control word is off. Incorrect length record indicates that the attachment detected a mismatch between the byte count and the frame length or that the p/f bit was on in the frame just received (when chaining). A *Start Cycle Steal Status* command may be issued to obtain the residual byte count and the address of the last attempted data transfer.
3	DCB specification check–This bit is set on if one of the following conditions occurs: a. The DCB contains an odd numbered address in the chaining address (word 5). b. The byte count field (DCB word 6) contains a value other than eight–applies only to *Start Cycle Steal Status* commands. c. The data address (DCB word 7) contains an odd numbered address–applies only to *Start Cycle Steal Status* commands. d. The status address (DCB word 4) contains an odd numbered address–applies only to receive operations, when the SE bit is on. e. The byte count (DCB word 6) equals zero for either a transmit operation or a receive operation. f. Bit 2 of the DCB control word is not on for a *Start Cycle Steal Status* command. g. More than one operation is specified in the control word (word 0) of the DCB. h. Bit 3 of DCB word 0 is on. i. Bit 1 of DCB word 0 is on.
4	Storage data check–This bit is set on during cycle-steal output (storage to attachment) operations only. It indicates that the storage location accessed during the current output cycle contains bad parity. The parity in main storage is not corrected. The attachment terminates the operation.

5 Invalid storage address–This bit is set on if an address presented by the attachment during a cycle-steal to or from storage exceeds the storage size of the system. The attachment terminates the operation.

6 Protect check–This bit is set on if the attachment attempts to store data into a storage location without the correct *cycle-steal address key.*

7 Interface data check–This bit is set on if a parity error is detected on the interface during a cycle-steal data transfer. The condition may be detected by the channel or the attachment. In either case, the operation is terminated and an exception interrupt is presented to the processor.

CYCLE STEAL STATUS WORDS

When a cycle-steal data transfer is terminated by an exception condition, bit-0 of the ISB may be set on. If ISB bit-0 is on, further information regarding the cause of the exception condition may be obtained by executing a *Start Cycle Steal Status* command.

The format of the DCB for this command is the same as for a normal cycle-steal data transfer. The attachment ignores bits 0,4, and 8–15 of the control word; and DCB words 1–5. The byte count must be eight, and the data address must be an even numbered address. Four words are transferred into main storage, starting at the data address contained in DCB word 7.

Word Zero

Word zero contains the main storage address of the last attempted cycle-steal transfer. This residual address may be either a data address, a DCB address, or a status address. Figure 4-2 shows which type of address the residual address can be for various error conditions. Where more than one possibility is shown, the program must decide which type of address cycle-steal status word 0 contains.

	Residual Address		
Error Condition	*DCB Address*	*Status Address*	*Data Address*
Delayed command reject	N/A	N/A	N/A
Incorrect length record		†	X
DCB specification check	*		
Storage data check	X		X
Invalid storage address	X	X	X
Protect check	X	X	X
Interface data check	X	X	X
Overrun		X	X
Timeout	X		X
Modem interface error	X		X
Block check error		X	X
Abort		X	X
Idle or inactivity detected	X		X
Nonproductive receive	X		X

*The address is that of the DCB word in error
†Long frame

Figure 4-2. Residual Address Table

Word One

Word one contains the residual byte count. This is the byte count remaining when an operation ends.

Word Two

Word two has the following format:

Bit	*Name*
0	Overrun
1	Abort
2	Long frame
3	Block check error
4	Timeout
5	Idle detected
6	Nonproductive receive timeout
7	Modem interface error
8–12	Not used
13	Business machine clock selected
14	Answertone jumper installed
15	Modem delay jumper installed

The bits and their meanings follow.

Bit *Meaning*

0 Overrun–During a receive operation, this condition occurs if the attachment is unable to transfer the contents of the storage data register to main storage before it is time to reload the register. During a transmit operation, an overrun occurs if the attachment is unable to reload the storage data register in time to keep a steady stream of data going out on the line.

1 Abort–During a receive operation, this bit is set on if the attachment receives eight consecutive one-bits (no zero-bit insertion) within a normal frame. This indicates that the transmitting station decided to terminate the frame prematurely.

2 Long frame–This bit indicates that the byte count has been decremented to zero and the current frame has not ended. The attachment continues to monitor the receive line until the end of the frame. However, any data received after the byte count reaches zero is lost.

3 Block check error–(Receive operation only) The attachment sets this bit on if the frame check sequence received by the attachment is incorrect.

4 Timeout–The attachment sets this bit on if either of the following timeouts occurs:
a. 'Data set ready' timeout
b. Disable 'data terminal ready' timeout

5 Idle detected–This error occurs if the attachment detects an idle condition after timer 1 times-out during a receive operation.

6 Nonproductive receive timeout–This bit indicates that a nonproductive receive timeout occurred. Refer to 'Timers', earlier in this chapter, for a description of this timeout.

7 Modem interface error–The attachment sets this bit on under the following conditions:
   a. 'Data set ready' is not active when either a transmit or receive operation is initiated.
   b. Loss of DTR, DSR, RTS, or CTS during a transmit operation.
   c. Loss of DTR or DSR during a receive operation.

   Refer to cycle-steal status word 3 for an indication of present modem line status.

8–12 These bits are not used and will be off.

13 Business machine clock–This bit indicates that the internal clocking jumper is installed.

14 Generate answertone jumper installed–This bit indicates that the answertone jumper is installed in the attachment. The attachment provides a three second answertone when a "ring" is detected.

15 Modem delay jumper installed–Some modems require that 'request to send' remains active for a time after the attachment transmits the ending flag. When this jumper is installed, the attachment maintains 'request to send' in the active condition and transmits trailing pad characters for two milliseconds after sending the ending flag.

Word Three

Word three contains status information regarding certain attachment and modem lines. After a modem error, word three indicates the status of the lines at the time of the error. If a modem error did not occur, word three indicates the status at the time the *Start Cycle Steal Status* command was executed.

Bit	*Line Name*
0	Data Terminal Ready
1	Data Set Ready
2	Request To Send
3	Clear To Send
4	Ring Indicator
5	Half Rate Selected
6	Transmit Mode Latch
7	Not used–will be zero

The low order byte (bits 8–15) contains the secondary station address.

STATUS AFTER RESETS

There are several methods of resetting some or all of the circuits in the attachment. They are:

Reset	*Action*
Power on reset	All attachment components are reset off.
System reset	All attachment components (except DTR, "half rate", and the residual address) are reset off.
Halt I/O command	All attachment components (except DTR, prepared level, I-bit, "half rate", residual address, residual byte count, and residual DCB information) are reset off by this command.
Device reset command	This command resets the same components as the Halt I/O command.

JUMPERABLE OPTIONS

The following options can be selected by installing jumper wires on the feature card.

Internal Clocking

With this jumper installed, the attachment provides clocking at 1,200 BPS or 600 BPS (selectable by programming).

Generate Answertone

With this jumper installed, the attachment provides a three second answertone after the modem activates 'data set ready' in response to the attachment activating 'data terminal ready'. This jumper should not be installed if the modem provides an answertone.

Request To Send

If this jumper is installed, the attachment maintains 'request to send' in an active condition. This eliminates modem "turnaround" when using a full-duplex modem. This option should always be selected when using a modem which always keeps 'clear to send' active.

Data Terminal Ready

If this jumper is installed, the attachment maintains 'data terminal ready' in an active condition. This option must not be selected for switched-line operation.

Modem Delay

There are some modems which may lose the last character at the end of a transmit operation. If this jumper is installed, the attachment will keep the transmit data line in a marking condition for two milliseconds after sending the last character to the modem and before resetting 'request to send', thus preventing the last character from being lost.

Secondary Station Address

If the attachment is to be used as a secondary station, the station address is assigned by installing jumpers corresponding to bits of the address.

Section Two. SDLC Feature Operating Procedures

COMMUNICATIONS INDICATOR PANEL

The communications indicator panel is an optional feature that can be a valuable aid to program debugging and machine troubleshooting.

The indicator panel provides a means of displaying various conditions and registers in the attachment. In addition, the 'data terminal ready' line to the modem can be reset from the indicator panel.

Line Select Switches

These switches are used only with multiple-line communications devices. The SDLC attachment does not use these switches.

Function/Display Switches

These switches determine what information is displayed in the indicator lamps. Figure 4-3 is a list of switch settings and the information that is displayed in the indicator lights.

Function/ Display switch setting	*Lamps*	*Information*
00000	0–7	High order byte of DCB word 0 (control word)
00001	0–7	Low order byte of DCB word 0 (control word)
00010	0–7	High order byte of DCB word 5 (chain address)
00011	0–7	Low order byte of DCB word 5 (chain address)
00100	0–7	High order byte of DCB word 6 (byte count)
00101	0–7	Low order byte of DCB word 6 (byte count)
00110	0–7	High order byte of DCB word 7 (data address)
00111	0–7	Low order byte of DCB word 7 (data address)
01000	0–7	Low order byte of word 1 of the Residual Status Block
01001	0–7	Interrupt status byte (ISB)
01010	0–7	High order byte cycle steal status word 2
01011	0–7	High order byte of DCB word 4 (status address)
01100	0–7	Low order byte of DCB word 4 (status address)
01101	0–7	SDLC control 0 Flag detected 1 Buffer service request 2 Idle detect 3 Abort detect 4 Overrun 5 Business machine clock selected 6 Attachment generated answer-tone 7 Modem delay selected

Figure 4-3 (Part 1 of 2). Indicator panel information–SDLC feature

Function/ Display switch setting	*Lamps*	*Information*
01110	0–7	Secondary station address
10100	0–7	Low order byte of DCB word 1 (timer 2)
10101	0–7	High order byte of DCB word 1 (timer 1)
11100	0–7	Lamp test
11101	0–7	Modem status 0 Data terminal ready 1 Data set ready 2 Request to send 3 Clear to send 4 Ring indicator 5 Half rate select 6 Transmit mode 7 Receive mode
11110*		Enable for DTR reset
11111*		Reset DTR

*To reset DTR, the switches must first be set to 11110, then to 11111. This prevents resetting DTR unintentionally.

Figure 4-3 (Part 2 of 2). Indicator panel information–SDLC feature

ERROR RECOVERY

Operate I/O Condition Codes

Condition Code 3 (Command Reject)

If condition code 3 is received in response to an *Operate I/O* instruction, check the validity of the command field of the IDCB and retry the instruction. Notify the user if the error persists. Only the following bit combinations are valid:

Prepare command	0110 0000
Device reset command	0110 1111
Start command	0111 XXXX
Read ID command	0010 0000
Halt I/O command	1111 0000
Write command*	010X XXXX

X The attachment does not look at these bits during the *Operate I/O* instruction.

* The SDLC attachment cannot execute a write command. It does, however, accept the command. When the *Operate I/O* instruction is completed, the attachment reports "delayed command reject" via an exception interrupt with ISB bit 1 set on.

Condition Code 5 (Interface Data Check)

This error occurs if either the processor channel or the attachment detects a parity error on the interface. Retry the instruction (up to three times). Notify the user if the error persists. This error indicates a malfunction in the hardware.

Interrupt Condition Codes

Interrupt condition code 4 (attention) indicates that the 'ring indicator' line from the modem is active. Condition codes 6 and 7 indicate that the 'ring indicator' line is active in conjunction with another interrupt causing condition.

Condition Codes 2 or 6 (Exception)

Examine the ISB to determine the cause of the interrupt. If bit zero of the ISB is on, issue a *Start Cycle Steal Status* command to determine the cause of the interrupt. See 'Interrupt Status Byte' (ISB) and 'Cycle Steal Status Words' for explanation of the exception conditions.

Storage Data Check. Reset the attachment and retry. Notify the user if the error persists.

Interface Data Check. Reset the attachment and retry. Notify the user if the error persists.

DCB Specification Check. Verify the correctness of the DCB address, data address, chain address, status address, byte count and cycle-steal address key. If these are correct, reissue the *Start* command. Notify the user if the error persists.

Appendix A. Reference Information

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII**	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
0	00	0000 0000	NUL	NUL	NUL		
1	01	0001	SOH	SOH	NUL	space	space
2	02	0010	STX	STX		1	1,]
3	03	0011	ETX	ETX	@		
4	04	0100	PF	EOT		2	2
5	05	0101	HT	ENQ	space		
6	06	0110	LC	ACK			
7	07	0111	DEL	BEL		3	3
8	08	1000		BS		4	5
9	09	1001	RLF	HT			
10	0A	1010	SMM	LF	P (even parity)		
11	0B	1011	VT	VT	P (odd parity)	5	7
12	0C	1100	FF	FF	0 (even parity)		
13	0D	1101	CR	CR	0 (odd parity)	6	6
14	0E	1110	SO	SO		7	8
15	0F	1111	SI	SI			
16	10	0001 0000	DLE	DLE		8	4
17	11	0001	DC1	DC1			
18	12	0010	DC2	DC2	H (even parity)		
19	13	0011	TM	DC3	H (odd parity)	9	0
20	14	0100	RES	DC4	((even parity)		
21	15	0101	NL	NAK	((odd parity)	0	z
22	16	0110	BS	SYN		Ⓓ (EOA)	Ⓓ (EOA),9
23	17	0111	IL	ETB			
24	18	1000	CAN	CAN			
25	19	1001	EM	EM			
26	1A	1010	CC	SUB			
27	1B	1011	CU1	ESC	X		
28	1C	1100	IFS	FS		upper case	upper case
29	1D	1101	IGS	GS	8		⩝
30	1E	1110	IRS	RS			
31	1F	1111	IUS	US		Ⓒ (EOT)	Ⓒ (EOT)
32	20	0010 0000	DS	space		@	t
33	21	0001	SOS	!	EOT		
34	22	0010	FS	"	D (even parity)		
35	23	0011		#	D (odd parity)	/	x
36	24	0100	BYP	$	S (even parity)		
37	25	0101	LF	%	S (odd parity)	s	n
38	26	0110	ETB	&		t	u
39	27	0111	ESC	'			
40	28	1000		(			
41	29	1001		)		u	e
42	2A	1010	SM	*		v	d
43	2B	1011	CU2	+	T		
44	2C	1100		,		w	k
45	2D	1101	ENQ	-	4		
46	2E	1110	ACK	.			
47	2F	1111	BEL	/		x	c
48	30	0011 0000		0	form feed		
49	31	0001		1	form feed	y	l
50	32	0010	SYN	2		z	h
51	33	0011		3	L		
52	34	0100	PN	4			
53	35	0101	RS	5	,		
54	36	0110	UC	6			

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII**	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
55	37	0011 0111	EOT	7		Ⓢ (SOA), comma	b
56	38	1000		8			
57	39	1001		9			
58	3A	1010		:	\ (even parity)		
59	3B	1011	CU3	;	\ (odd parity)	index	index
60	3C	1100	DC4	<	< (even parity)		
61	3D	1101	NAK	=	< (odd parity)	Ⓑ (EOB)	
62	3E	1110		>			
63	3F	1111	SUB	?			
64	40	0100 0000	space	@		Ⓝ ,-	!
65	41	0001		A	EOA		
66	42	0010		B	B (even parity)		
67	43	0011		C	B (odd parity)	i	m
68	44	0100		D	" (even parity)		
69	45	0101		E	" (odd parity)	k	
70	46	0110		F		l	v
71	47	0111		G			
72	48	1000		H			
73	49	1001		I		m	,
74	4A	1010	¢	J		n	r
75	4B	1011	.	K	R		
76	4C	1100	<	L		o	i
77	4D	1101	(	M	2		
78	4E	1110	+	N			
79	4F	1111	]	O		p	a
80	50	0101 0000	&	P	line feed		
81	51	0001		Q	line feed	q	o
82	52	0010		R		r	s
83	53	0011		S	J		
84	54	0100		T			
85	55	0101		U	*		
86	56	0110		V			
87	57	0111		W		$	w
88	58	1000		X			
89	59	1001		Y			
90	5A	1010	!	Z	Z (even parity)		
91	5B	1011	$	[	Z (odd parity)	CRLF	CRLF
92	5C	1100	*	\	: (even parity)		
93	5D	1101	)	]	: (odd parity)	backspace	backspace
94	5E	1110	;	Λ		idle	idle
95	5F	1111	¬	–			
96	60	0110 0000	-		ACK		
97	61	0001	/	a		&	j
98	62	0010		b		a	g
99	63	0011		c	F		
100	64	0100		d		b	
101	65	0101		e	&		
102	66	0110		f			
103	67	0111		g		c	f
104	68	1000		h		d	p
105	69	1001		i			
106	6A	1010	¦	j	V (even parity)		
107	6B	1011	,	k	V (odd parity)	e	
108	6C	1100	%	l	6 (even parity)		
109	6D	1101	–	m	6 (odd parity)	f	q
110	6E	1110	>	n		g	comma
111	6F	1111	?	o			
112	70	0111 0000		p		h	/
113	71	0001		q	shift out		
114	72	0010		r	N (even parity)		
115	73	0011		s	N (odd parity)	i	y
116	74	0100		t	. (even parity)		

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII**	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
117	75	0111 0101		u	. (odd parity)		
118	76	0110		v		Ⓨ ,period	-
119	77	0111		w			
120	78	1000		x			
121	79	1001		y			
122	7A	1010	:	z		horiz tab	tab
123	7B	1011	#	{	↑		
124	7C	1100	@	|		lower case	lower case
125	7D	1101	'	}	>		
126	7E	1110	=	~			
127	7F	1111	"	DEL		delete	
128	80	1000 0000					
129	81	0001	a		SOM	space	space
130	82	0010	b		A (even parity)	=	±, [
131	83	0011	c		A (odd parity)		
132	84	0100	d		! (even parity)	<	@
133	85	0101	e		! (odd parity)		
134	86	0110	f				
135	87	0111	g			;	#
136	88	1000	h		X-ON	:	%
137	89	1001	i				
138	8A	1010					
139	8B	1011			Q	%	&
140	8C	1100					
141	8D	1101			1	'	¢
142	8E	1110				>	*
143	8F	1111					
144	90	1001 0000			horiz tab	*	$
145	91	0001	j		horiz tab		
146	92	0010	k				
147	93	0011	l		I	(	)
148	94	0100	m				
149	95	0101	n		)	)	Z
150	96	0110	o			Ⓓ (EOA),"	(
151	97	0111	p				
152	98	1000	q				
153	99	1001	r				
154	9A	1010			Y (even parity)		
155	9B	1011			Y (odd parity)		
156	9C	1100			9 (even parity)	upper case	upper case
157	9D	1101			9 (odd parity)		
158	9E	1110					
159	9F	1111				Ⓒ (EOT)	Ⓒ (EOT)
160	A0	1010 0000			WRU (even)	¢	T
161	A1	0001	~		WRU (odd)		
162	A2	0010	s				
163	A3	0011	t		E	?	X
164	A4	0100	u				
165	A5	0101	v		%	S	N
166	A6	0110	w			T	U
167	A7	0111	x				
168	A8	1000	y				
169	A9	1001	z			U	E
170	AA	1010			U (even parity)	V	D
171	AB	1011			U (odd parity)		
172	AC	1100			5 (even parity)	W	K
173	AD	1101			5 (odd parity)		
174	AE	1110					
175	AF	1111				X	C
176	B0	1011 0000					
177	B1	0001			return	Y	L
178	B2	0010			M (even parity)	Z	H

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII**	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
179	B3	1011 0011			M (odd parity)		
180	B4	0100			- (even parity)		
181	B5	0101			- (odd parity)		
182	B6	0110					
183	B7	0111				Ⓢ (SOA), |	B
184	B8	1000					
185	B9	1001					
186	BA	1010					
187	BB	1011			]	index	index
188	BC	1100					
189	BD	1101			=	Ⓑ (EOB)	
190	BE	1110					
191	BF	1111					
192	C0	1100 0000	{		EOM (even)	Ⓝ ,–	
193	C1	0001	A		EOM (odd)		
194	C2	0010	B				
195	C3	0011	C		C	J	M
196	C4	0100	D				
197	C5	0101	E		#	K	
198	C6	0110	F			L	V
199	C7	0111	G				
200	C8	1000	H				
201	C9	1001	I		X-OFF	M	”
202	CA	1010			S (even parity)	N	R
203	CB	1011			S (odd parity)		
204	CC	1100	⌡		3 (even parity)	O	I
205	CD	1101			3 (odd parity)		
206	CE	1110	⌜				
207	CF	1111				P	A
208	D0	1101 0000	}				
209	D1	0001	J		vertical tab	Q	O
210	D2	0010	K		K (even parity)	R	S
211	D3	0011	L		K (odd parity)		
212	D4	0100	M		+ (even parity)		
213	D5	0101	N		+ (odd parity)		
214	D6	0110	O				
215	D7	0111	P			!	W
216	D8	1000	Q				
217	D9	1001	R				
218	DA	1010					
219	DB	1011			[	CRLF	CRLF
220	DC	1100					
221	DD	1101			;	backspace	backspace
222	DE	1110				idle	idle
223	DF	1111			PAD		
224	E0	1110 0000	\				
225	E1	0001			bell	+	J
226	E2	0010	S		G (even parity)	A	G
227	E3	0011	T		G (odd parity)		
228	E4	0100	U		, (even parity)	B	+
229	E5	0101	V		, (odd parity)		
230	E6	0110	W				
231	E7	0111	X			C	F
232	E8	1000	Y			D	P
233	E9	1001	Z				
234	EA	1010					
235	EB	1011			W	E	
236	EC	1100	⌐				
237	ED	1101			7	F	Q
238	EE	1110				G	comma
239	EF	1111					

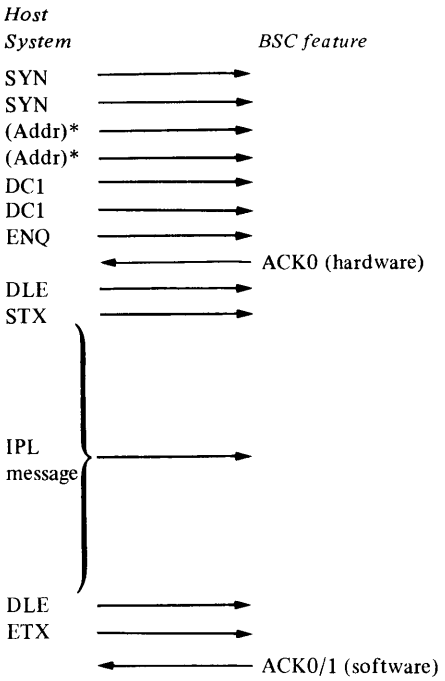
Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII**	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
240	F0	1111 0000	0		shift in (even)	H	?
241	F1	0001	1		shift in (odd)		
242	F2	0010	2				
243	F3	0011	3		O	I	Y
244	F4	0100	4				
245	F5	0101	5		/		
246	F6	0110	6			Ⓨ , ¬	—
247	F7	0111	7				
248	F8	1000	8				
249	F9	1001	9				
250	FA	1010	LVM		⇐ (even parity)	horiz tab	tab
251	FB	1011			⇐ (odd parity)		
252	FC	1100			? (even parity)	lower case	lower case
253	FD	1101			? (odd parity)		
254	FE	1110					
255	FF	1111			delete / rub out	delete	

*When used with the BSCA, the software must maintain parity in bits 0–7 of each byte.

2740 Line Control Characters (EBCD)			
Char	*Hex*	*Alternate Designation*	*Meaning*
Ⓑ	BD/3D	EOB	End of Block
Ⓒ	9F/1F	EOT	End of Transmission
Ⓓ	96/16	EOA	End of Address
Ⓝ	C0/40	No	Negative Response
Ⓢ	B7/37	SOA	Start of Address; used only in addressing
Ⓨ	F6/76	Yes	Positive Response
US	1C/9C		Upshift
DS	7C/FC		Downshift

2741 Line Control Characters (Correspondence)			
Char	*Hex*	*Alternate Designation*	*Meaning*
Ⓒ	9F/1F	EOT	End of Transmission
Ⓓ	16/96	EOA	End of Address
US	1C/9C		Upshift
DS	7C/FC		Downshift

Line Control Characters (ASCII)		
Char	*Hex*	*Meaning*
WRU	A1	Who are you? WRU or Dial requests identification (ID)
XON	89	Transmitter On
XOFF	C9	Transmitter Off
EOT	21	End of Transmission



*Used only if the attachment is a multipoint tributary.

Sample BSC IPL sequence

Operate I/O Condition Codes				
CC Value	*Even*	*Carry*	*Overflow*	*Meaning*
0	0	0	0	Not attached
1	0	0	1	Busy
2	0	1	0	Busy after reset (see *Note* 2)
3	0	1	1	Command reject
4	1	0	0	Intervention required (see *Note* 1)
5	1	0	1	Interface data check
6	1	1	0	Controller busy (see *Note* 3)
7	1	1	1	Satisfactory

Notes.

1. Not reported by any communications attachment.
2. Not reported by multiple-line BSC attachments.
3. Not reported by any single-line communications attachment. Reported on multiple-line attachments when the controller is busy servicing a previous Operate I/O instruction; a subsequent *Controller End* interrupt will occur (interrupt condition code zero).

Interrupt Condition Codes				
CC Value	*Even*	*Carry*	*Overflow*	*Meaning*
0	0	0	0	Controller end (see *Note* 1)
1	0	0	1	PCI (see *Note* 3)
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention (see *Note* 2)
5	1	0	1	Attention and PCI (see *Note* 3)
6	1	1	0	Attention and exception (see *Note* 2)
7	1	1	1	Attention and device end (see *Note* 2)

Notes.

1. Reported only by multiple-line attachments. The controller presents the device address of line 0.
2. The ACC attachments do not report these condition codes. On BSC and SDLC attachments "attention" indicates that the 'ring indicator' line from the modem is active.
3. Not reported by any of the communications attachments.

Appendix B. ACC Features Operational Flowcharts

The following flowcharts can be used in conjunction with the communications indicator panel with its function/display switches set to 00001.

Lamps 4–7 on the indicator panel identify the operation being performed:

4–7	*Operation*	*Chart*
0000	Transmit	B-1
0001	Transmit End	B-1
0010	Transmit Allow Break	B-1
0011	Transmit End Allow Break	B-1
0100	Receive or Receive Response	B-2
0101	Receive or Receive Response–with timeout	B-2
0110	Ring Enable	B-3
0111	Ring Enable with timeout	B-3
1000	DTR Enable	B-4
1001	DTR Enable with timeout	B-4
1010	DTR Enable with answer-tone	B-4
1011	DTR Enable with answer-tone and timeout	B-4
1100	DTR Disable	B-5
1101	Set Control	B-6
1110	Program delay	B-7
1111	Reset	B-8

Lamps 0–3 identify the subroutines within a particular operation. The subroutine numbers are shown in hexadecimal notation in the flowcharts.

Note. These flowcharts are intended to give a general description of various operations and do not reflect the total microprogram.

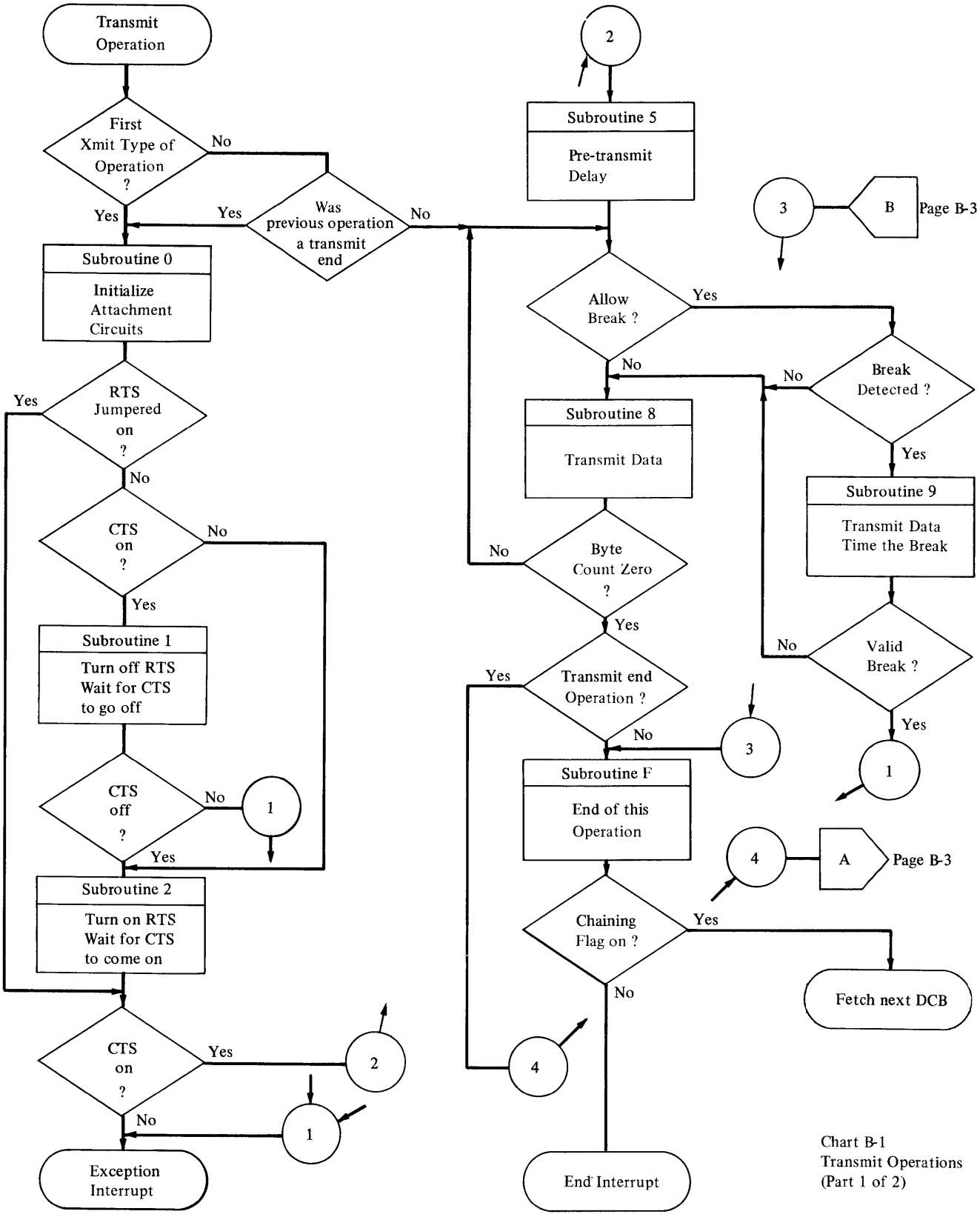


Chart B-1
Transmit Operations
(Part 1 of 2)

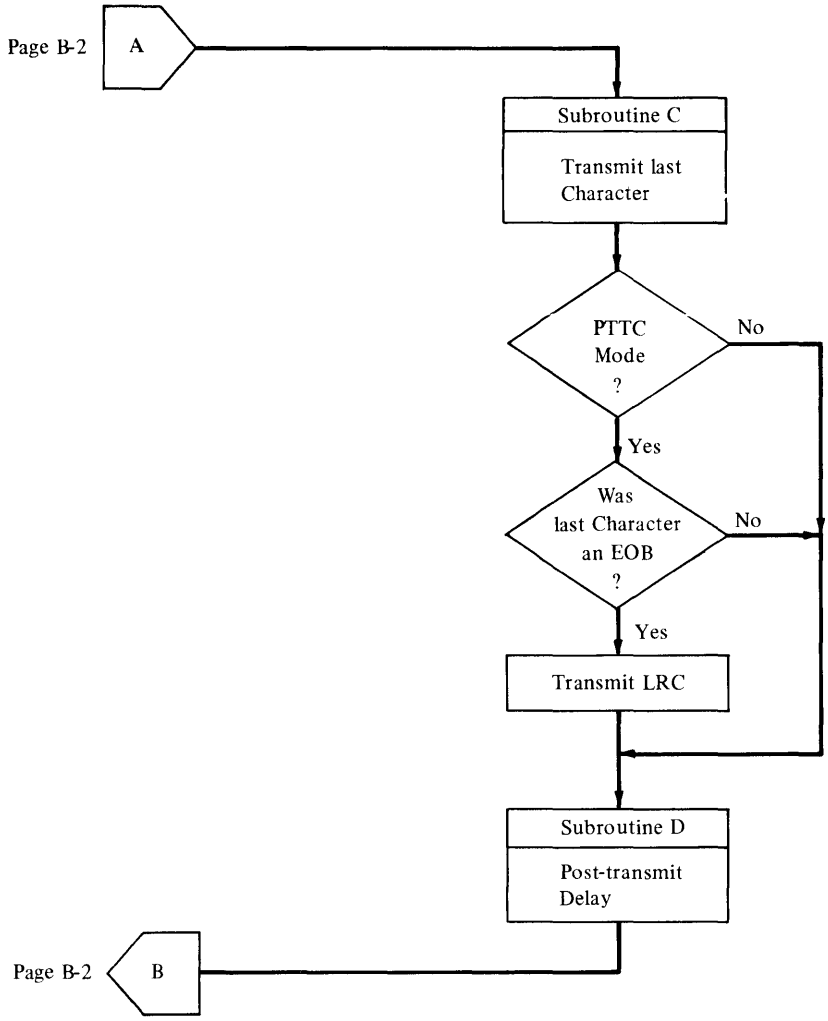


Chart B-1
Transmit Operations
(Part 2 of 2)

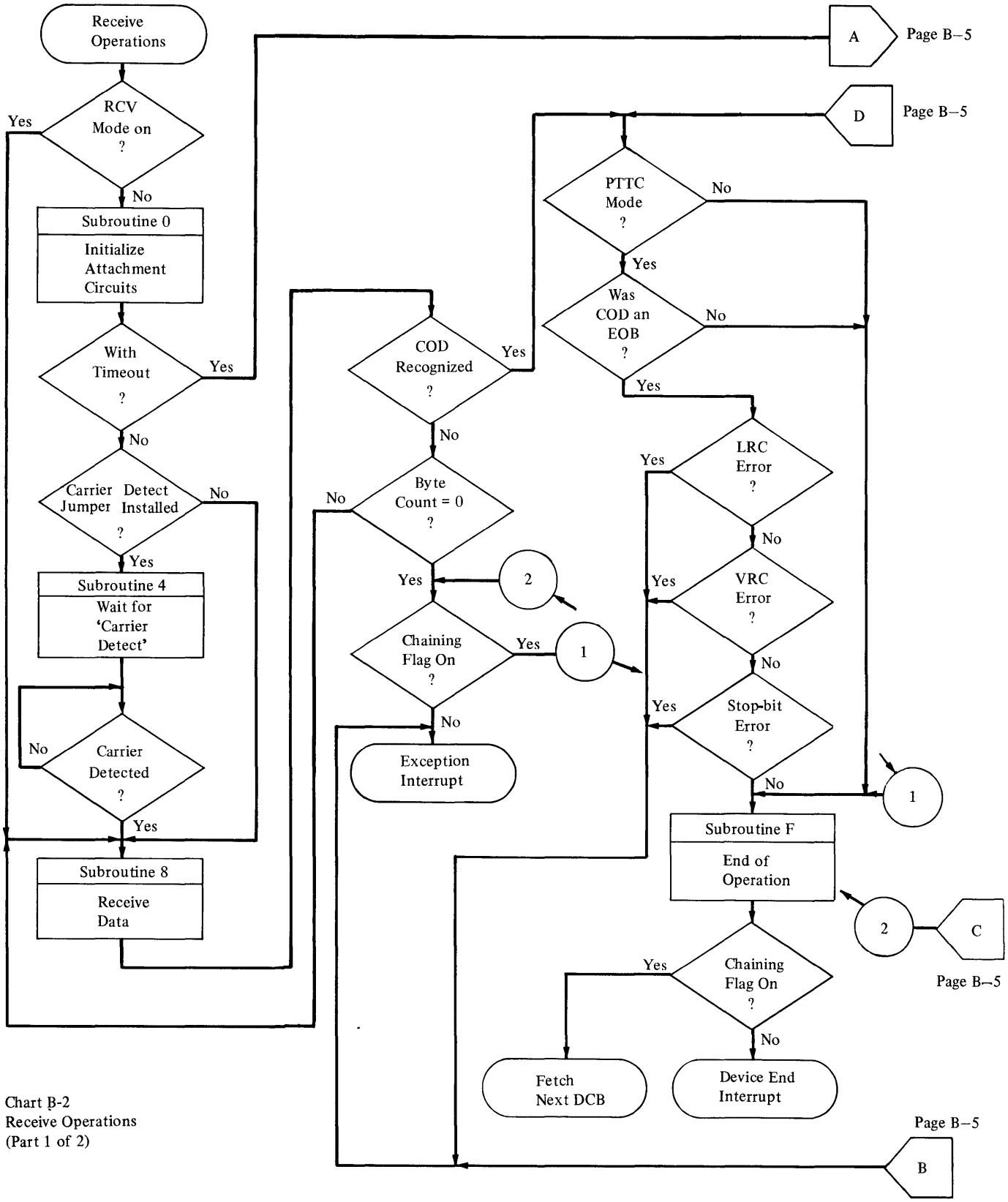


Chart B-2
Receive Operations
(Part 1 of 2)

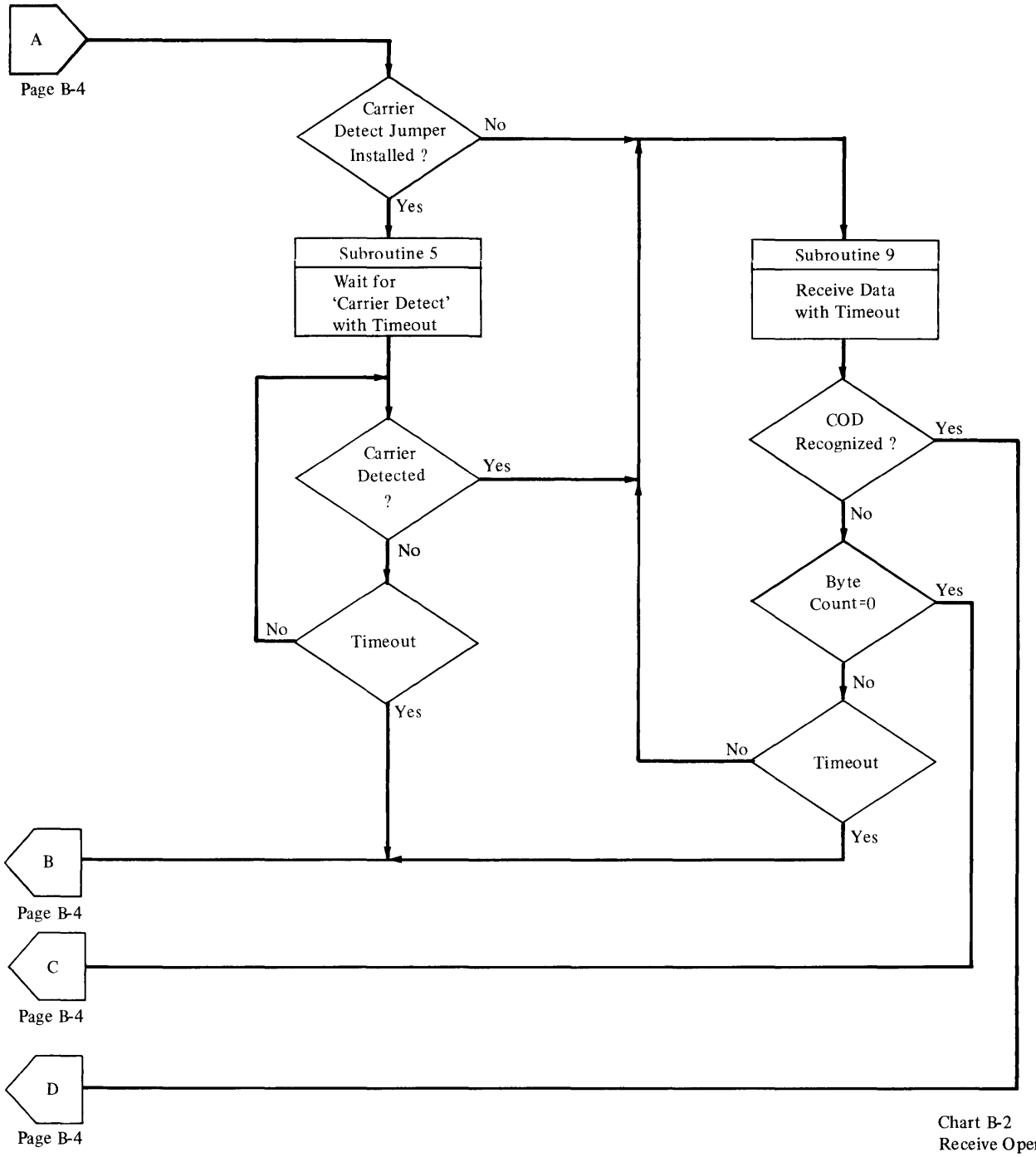


Chart B-2
Receive Operations
(Part 2 of 2)

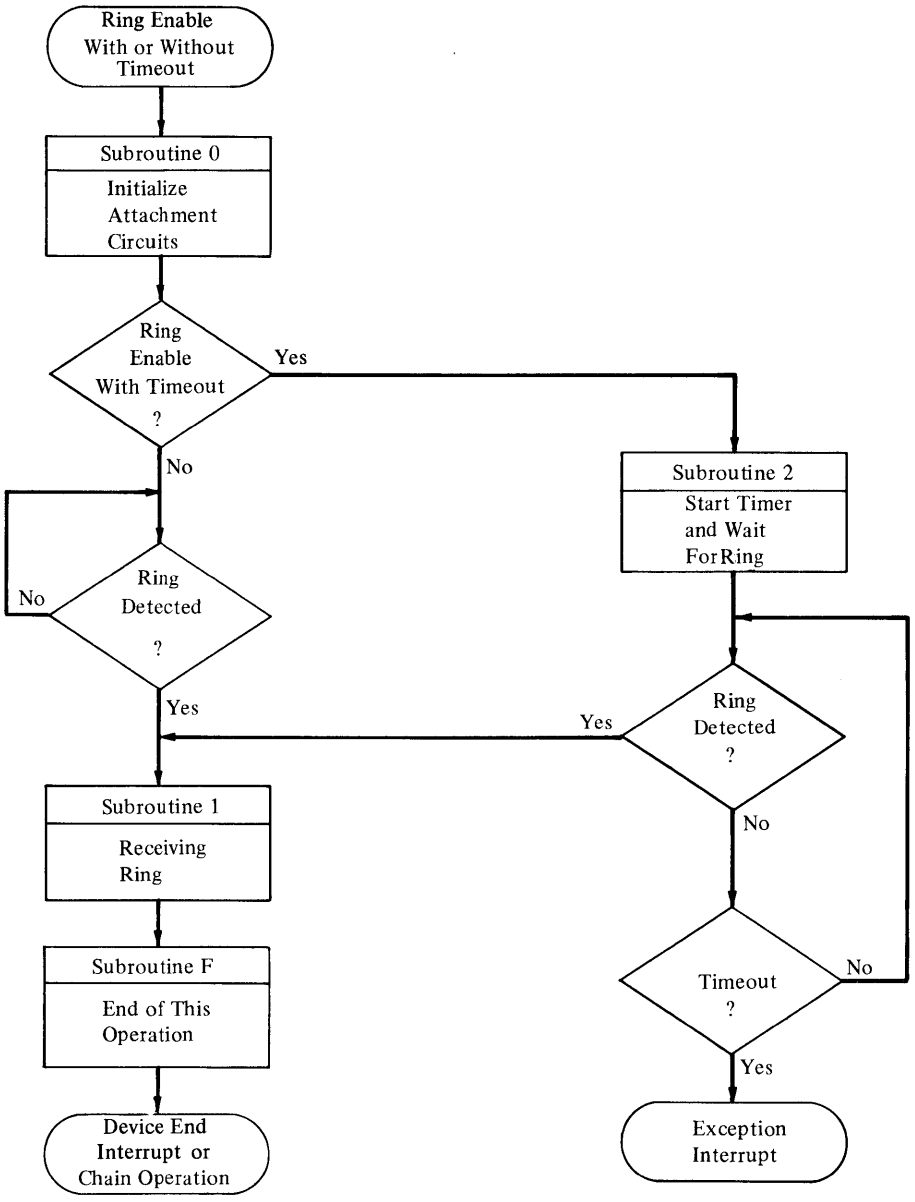


Chart B-3
Ring Enable and
Ring Enable with Timeout

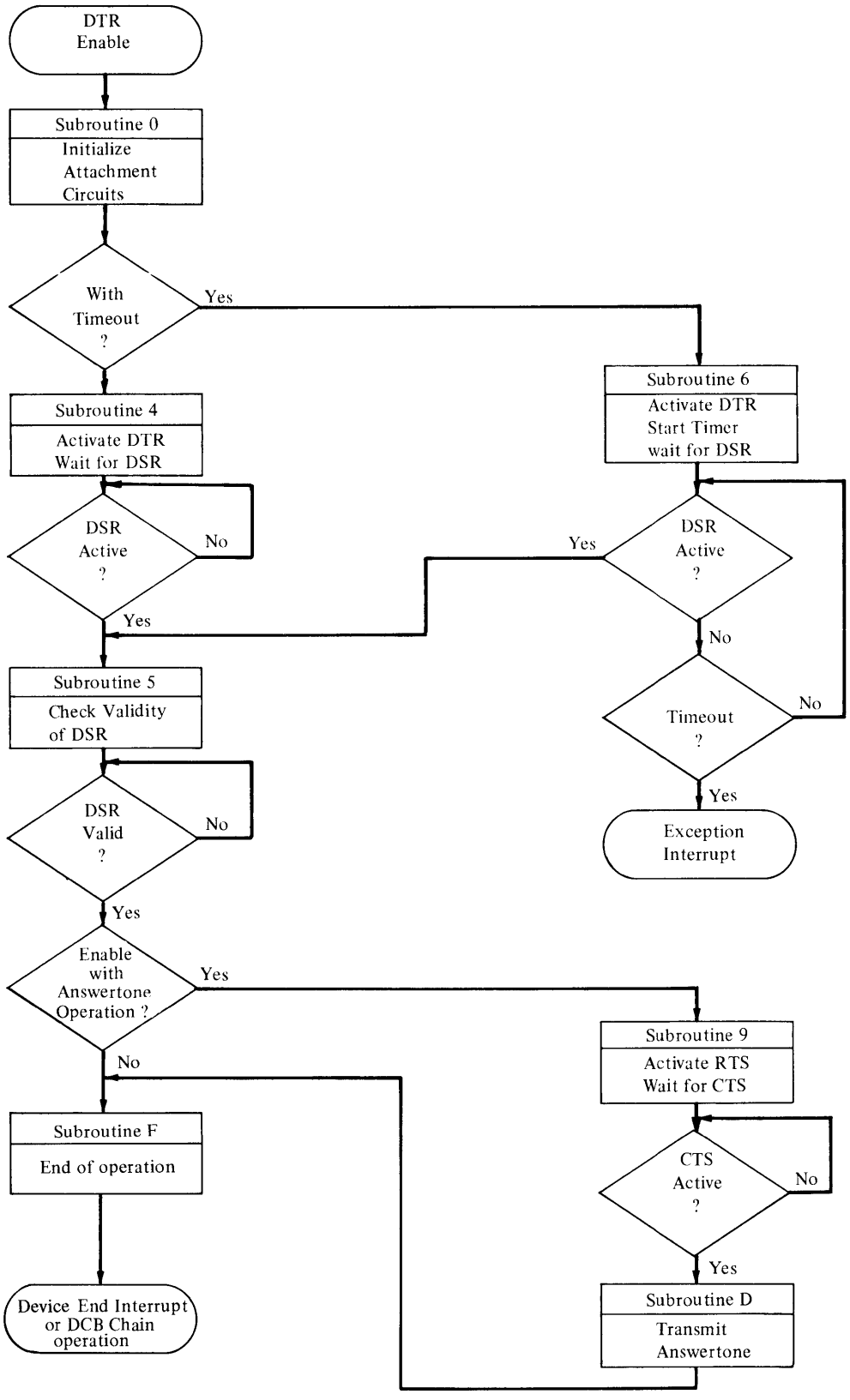


Chart B-4
DTR Enable Operation

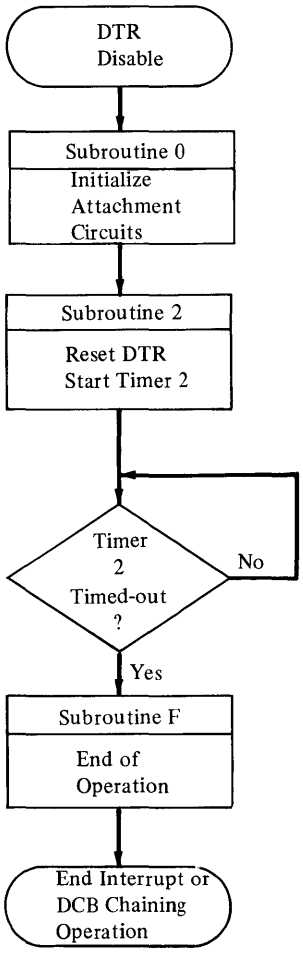


Chart B-5
DTR Disable Operation

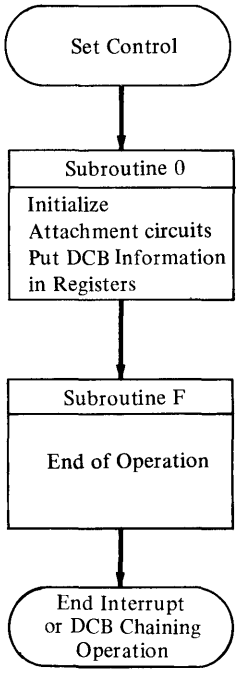


Chart B-6
Set Control Operation

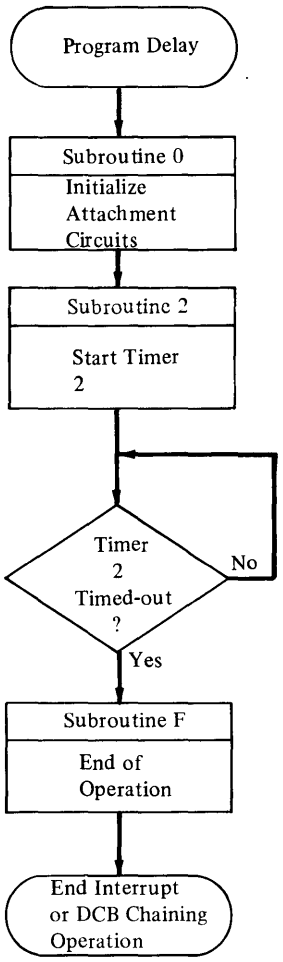


Chart B-7
Program Delay Operation

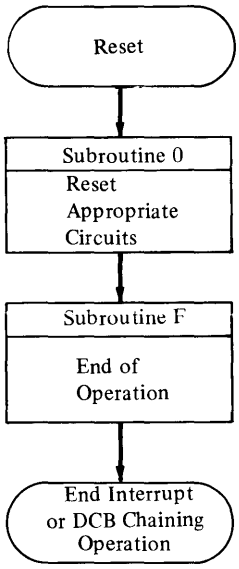
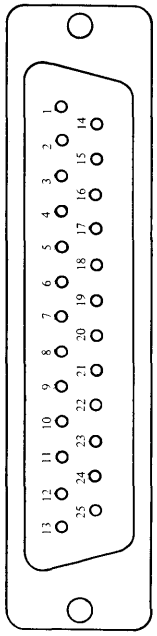
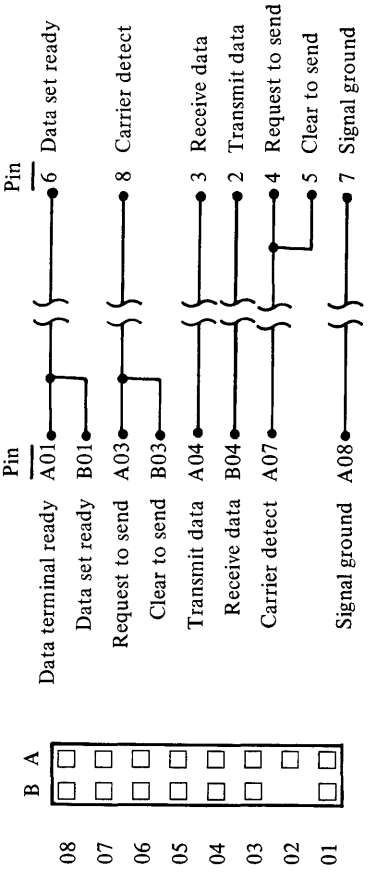


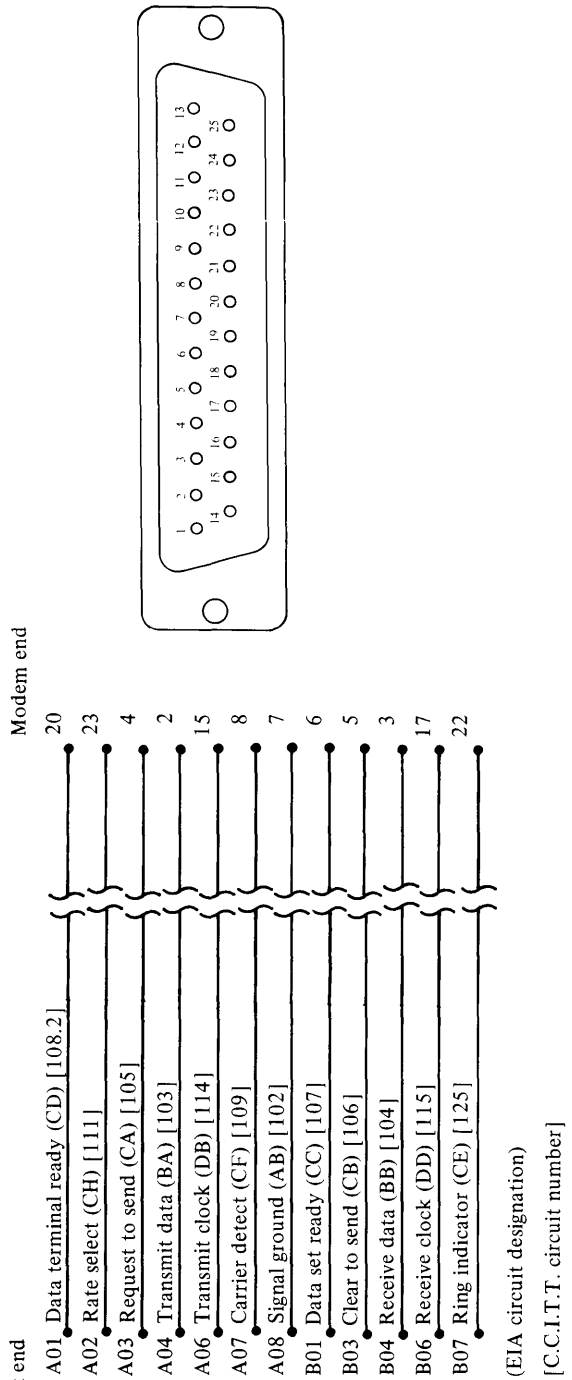
Chart B-8
Reset Operation

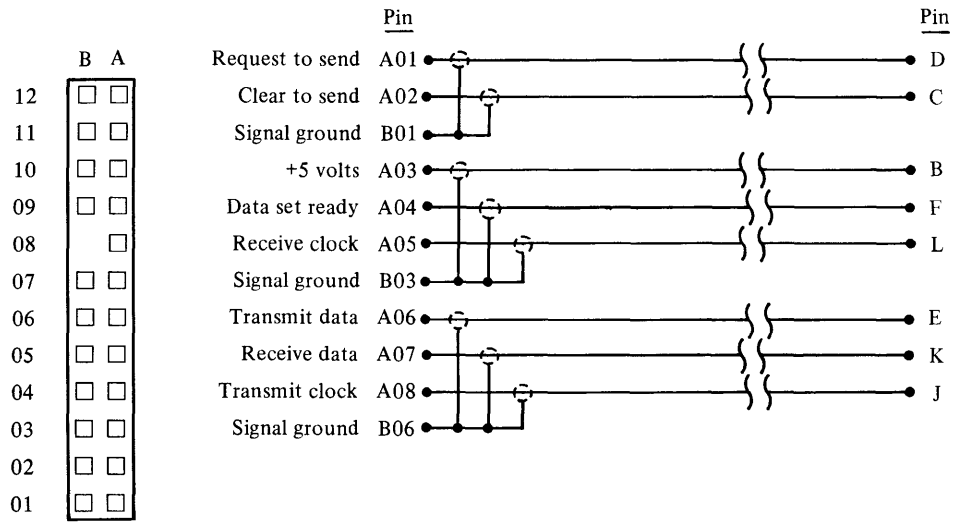
Appendix C. Cable Information



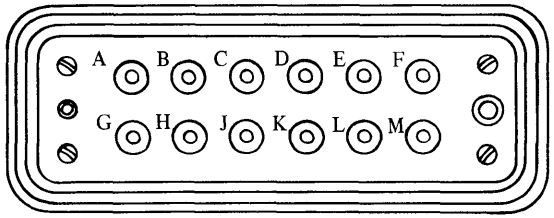

Pin
Pin
Data terminal ready A01
Data set ready B01
Request to send A03
Clear to send B03
Transmit data A04
Receive data B04
Carrier detect A07
Signal ground A08
6 Data set ready
8 Carrier detect
3 Receive data
2 Transmit data
4 Request to send
5 Clear to send
7 Signal ground
B A
08 07 06 05 04 03 02 01

EIA Data Set Cable



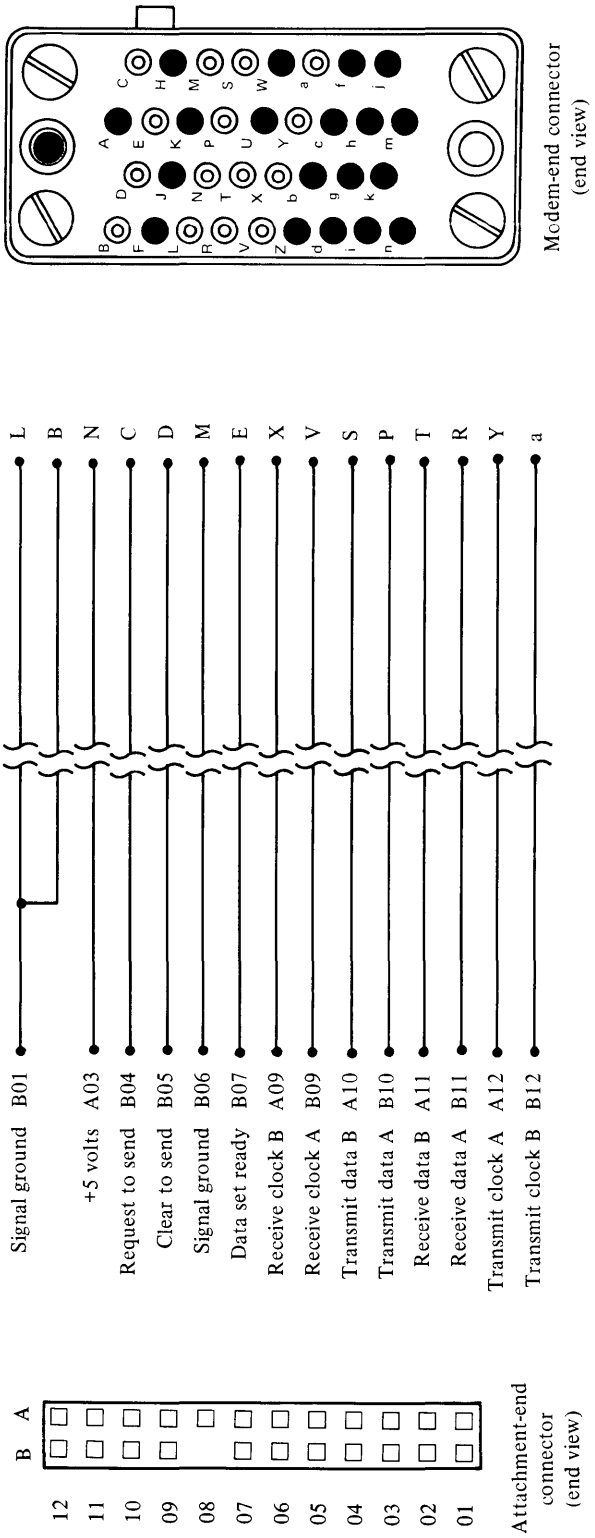


Attachment-end connector (end view)



Modem-end connector (end view)

Binary Synchronous Communications V.35/High Speed DDN Cable



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