

Technical Newsletter No. 6

APPLIED SCIENCE DEPARTMENT

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THE IBM 602-A CALCULATING PUNCH AS A GENERAL PURPOSE CALCULATOR

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INTRODUCTION

Some time ago a study was initiated with the object of adapting catalytic cracking yield and quality predictions to IBM calculators. It was soon recognized that the Card-Programmed Electronic Calculator (CPC) was best suited to this type of work. However, since one of these machines was not immediately available to the author, a system was developed for doing these calculations on the simpler 602-A calculator.

Catalytic cracking yield and quality predictions are typical of many technical calculations. They consist of two basic elements: first, charts or tables which express empirical functions of certain base variables must be consulted; second, values of these functions must be combined according to certain specified arithmetic rules to yield final answers. This paper describes a method by which both of these operations are done on the 602-A calculator in an integrated fashion.

Two general purpose control panels for the 602-A are involved in this work. The first panel permits card-programming of simple arithmetic calculations involving only addition, subtraction, multiplication, and division. Sequential calculations of any length can be performed provided no more than seven numbers must be stored at any step. The second control panel is for performing interpolations in third difference tables of functions of single variables. These tables serve as a highly condensed form of "correlation library" on punched cards.

The two calculation systems for the 602-A, that is card programming and table look-up, have been designed to work together. Interpolated values calculated from the "library" of difference tables serve as the intermediate data on which the final card-programmed calculations are based. No manual handling or key punching of these intermediate data is required.

Although the time saved by the machine calculations, as compared to previous manual methods, is in itself of considerable importance, the release of technical personnel for other work and the accuracy and consistency of the calculated results are probably of even greater importance. While this system of calculation for the 602-A has been

primarily a temporary expedient, until use could be made of the faster and more flexible CPC, it will probably be interesting to small scale users of computing equipment, where the volume of work to be done is insufficient to justify the more expensive machine.

CARD PROGRAMMING SET-UP

The control panel to be discussed is an adaptation of one described by E. V. Hankam¹ of the Watson Scientific Computing Laboratory. Certain features of the Hankam board, for shifting of numbers, have been eliminated, resulting in some simplification of wiring with little loss in flexibility for many types of problems.

The control panel described here is based on the premise that the calculator will read all data in the form of eight-digit numbers, having the decimal point located between the fourth and fifth digits. Such numbers might be indicated as xxxx.xxxx in notational form. All answers which are punched by the 602-A are exactly similar eight-digit numbers.

Possible Operations

The operation of the calculator is under the control of code punches in the cards which it reads. A group of cards for performing a sequential calculation is called a program deck, and punches in these cards may cause any of the following operations to be performed:

- (1) A number read from a card may be placed in any one of seven storage units in the machine.
- (2) A number on a card may be added to, multiplied by, or divided into a number already in a storage unit. Furthermore, a number in storage may be subtracted from a number read from a card. The result of any of these operations may be placed in any of the machine's seven storage units.
- (3) Any two numbers stored in the calculator may be added, subtracted, multiplied or divided and the answer can be read into any desired storage unit.
- (4) At any point in a calculation sequence an answer can be punched into a card.
- (5) All operations are done with full decimal and sign control provided conventions for feeding data to the machine are

^{1.} Hankam, Eric V., A Card Programmed 602-A Board - 9 pp. mimeographed New York: IBM, November 25, 1951

followed. No provision is made for rounding, however, and care must be taken in the sequencing of calculations so that numbers do not exceed the eight-digit capacity of the machine by becoming so large or so small that significant figures are lost.

Card Layout and Coding

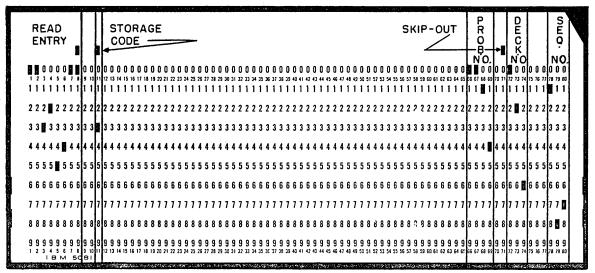


Fig. 1 Data Card

Fig. 1 shows a typical data card for performing the type of operation described in (1) above. The first eight columns of the card contain the number to be stored in the calculator. An X punch in the eighth column is used to denote negative numbers. The eleventh column carries an X punch which indicates that on this type of card the number in Cols. 1-8 is simply to be stored. A digit punch from 2 to 8 in Col. 11 designates which of the seven available storage units is to be used. Col. 71 carries an X punch which causes the card to be "skipped out" of the machine without punching since it is not an answer card. Cols. 66-69 identify the Problem Number of the calculation with which this card is associated. Cols. 72-74 designate the card program deck from which the card comes, and Cols. 78-80 designate the Sequence Number of the card in that program deck.

Fig. 2 shows an instruction card involved in the type of operation discussed in (2) above. Cols. 1-8 again carry the number to be read in from the card. Col. 14 specifies according to a digit code whether this number is to be added to (1) multiplied by (3) or divided into (4) a second number held in a storage unit designated by a digit (called the B-code) in Col. 15.

^{2.} Storage unit 1 is reserved for calculating functions and cannot be used for storage.

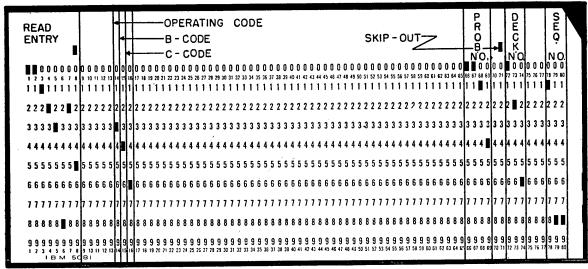


Fig. 2 Instruction Card with Read Entry

Col. 16 specifies (by a digit called the C-code) the storage unit into which the result of the operation is to be placed. If a number in a storage unit is to be subtracted from the number on the card, then Col. 14 should carry a 2 punch.

The card shown in Fig. 2 specifically calls for the number in Cols. 1-8 (-12.3825) to be multiplied (3 in Col. 14) by the number in the fourth storage unit (4 in Col. 15) and the result read into the sixth storage unit (6 in Col. 16). All of the punches in the last columns of the card have the same significance as in Fig. 1.

Fig. 3 shows the third type of card. This card contains no number in Cols. 1-8, since it will deal only with numbers already stored in the machine. The operation to be

	A-GODE OP. CODE	ANSWER	NX IN COL 71	P D A S R E N E O C S Q
	B-CODE	FIELD	FOR PUNCHING	B + K NO NO NO
000000000000000	100 habe le 1 1 10 10 20 21 22 22 24 25 26 27		7 48 49 50 51 52 53 54 55 56 57 58 53 60 61 62 63 64 63	100 01 00 00 10 11 10 11 10 10 10 11 10 10
1111111111111	իիիիի 11111111111	1 1 1 1 1 1 1 1 1 1		
	1 1 1 1 1	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		1 1 1 1 1
	FILLI	3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3		
	1 1 1 1 1	5 5 5 5 5 5 5 6 5 5 5 5 5 5 5 5 5 5 5 5		1 1 1 1 1
	1 1 1 1 1	666666666666666666666666666666666666666		
	1 1 1 1 1	11111111111111111111111		
	1 1 1 1 1	8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8		1 1 1 1
	9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	99999999999999999		
1 2 3 4 5 6 7 8 9 10 11 12 1 BM 5081	12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 2	27 28 29 30 31 32 33 34 35 56 31 38 39 40 41 42 43 44 45 46	11 48 49 50 31 32 33 39 33 36 37 36 37 36 03 61 62 63 64 6	

Fig. 3 Instruction Card without Read Entry

performed is of the type A \odot B = C. ³ Col. 13 carries the A-code (storage unit in which A is held), Col. 14 contains the operating code (1 for addition, 2 for subtraction, 3 for multiplication, and 4 for division), and Cols. 15 and 16 carry the B- and C-codes

^{3.} The symbol Θ denotes any of the four possible basic arithmetic operations $(+, -, \times, +)$.

respectively. In subtraction the first factor, A, must always be the minuend; in division A must always be the divisor.

On the card shown in Fig. 3 the answer is to be punched into the card. For this purpose the eighth storage unit must be used and the X punch must be omitted in Col. 71. The manner in which the control board is wired requires that any time a number is read into the eighth storage unit an answer must be punched. The number then remains in the storage unit for further calculations if needed.

Answers are punched into Cols. 28-35. If the answer is a negative number it will carry an X in Col. 35. An Answer Number is designated in Cols. 75-77. All other code designations in the latter part of the card are the same as in Fig. 1.

Detailed wiring directions for the 602-A card-programmed control panel are given at the end of the article and the programming of a simple illustrative example is shown.

Scope and Speed of Operations

The problems for which this control panel has been used thus far involve program decks of about two hundred cards. A program deck of this size averages about ten minutes running time on the 602-A, and any number of successive related or unrelated program decks can be fed continuously to the calculator.

INTERPOLATION

A frequently recurring problem in technical calculations by IBM machines is that of representing correlations in a form adaptable to machine treatment. If the equation of a correlation is known or can readily be obtained it is generally easiest to evaluate the equation directly through card-programming. If the equation is not known, however, or it is known but extremely cumbersome, then some thought must be given to alternative solutions.

There are at least two straight-forward choices open:

- 1. An approximate analytic expression for the correlation may be devised.
- 2. The correlation may be represented in tabular form.

Which of these choices is adopted must be decided largely upon the basis of circumstances governing a particular instance. Let it suffice to say at this point, however, that it has frequently been found that tabular representation seemed most convenient and satisfactory.

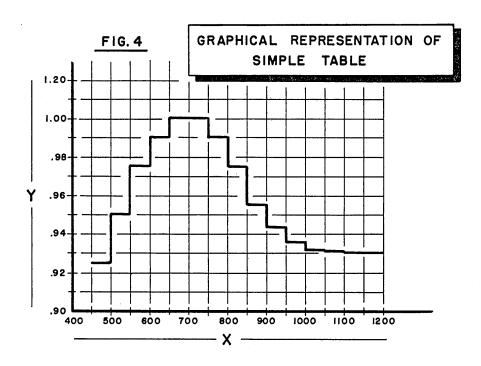
This report considers tables of functions of a single variable. Later work (probably with the Card-Programmed Electronic Calculator) may possibly extend these techniques to tables of functions of two or three variables. For the present, however, this latter type of machine problem has been handled through analytic expressions or not at all.

After having decided to express a function in tabular form there remains a problem as to exactly what kind of a table should be produced. For the sake of consistency (which has a very important significance in this work) a single type of table is much to be de-

sired. It was decided that third difference tables represented the best compromise between several factors considered, namely: ease of preparation, speed of machine calculations, and acceptability of results. The following section discusses briefly what difference tables are and how they can be constructed.

Difference Tables

The simplest type of table which can be devised is one which contains a single value of the function under consideration for each value of the argument which is tabulated. A table of this type is shown in the first two columns of Table I. When a table such as this is used in the form of IBM cards, any intermediate value of the argument will select the value of the function corresponding to the next lowest (or, if desired, the next highest) value of the argument. If all the intermediate values which could be "calculated" from such a table were plotted in graphical form, the result might be represented by the stepwise curve shown in Figure 4. Even though the resulting curve may represent the actual function within tolerable limits of absolute accuracy, nevertheless the erratic manner in which the calculated values vary is quite objectional in studies involving the effects of small changes in the argument.



A better table to use would be a "first difference" table. As shown in the first three columns of Table I, this type of table lists the differences between successive

	4				3d Diff, $\triangle^3 y$ 0100 . 0050 . 0050 . 0050 . 00121 0002 0012 0005 0005
ERENCE TABLES	0	4			2d Diff, $\triangle^2 y$. 0000 . 0100 . 0100 . 0100 . 0040 . 0042 . 0042 . 0000 . 0005 . 0005
VARIOUS TYPES OF DIFFERENCE TABLES	Third Difference Table	Second Difference Table	nce Table		1st Diff, $\Delta^{1}y$. 0250 . 0250 . 0150 . 0100 . 0100 0100 0195 0195 0019 0015 0005 . 0000
TABLE I. V		Secon	First Difference Table	Simple Table	Function, y . 9250 . 9500 . 9750 . 9900 . 99750 . 9555 . 9436 . 9357 . 9300 . 9300
				•	Argument, x 450.0000 500.0000 550.0000 650.0000 700.0000 750.0000 850.0000 850.0000 950.0000 1150.0000 1150.0000

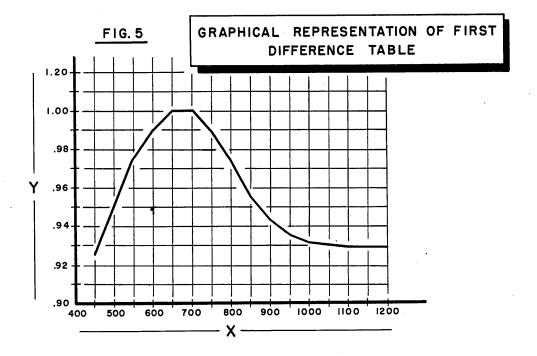
values of y as well as the values themselves. In using such a table, one first calculates

$$p = \frac{x - x_n}{\Delta x} \tag{1}$$

where x_n is the first value of the argument which precedes x in the table and Δx is the constant interval between the tabulated values of the argument. The value of y corresponding to x is then

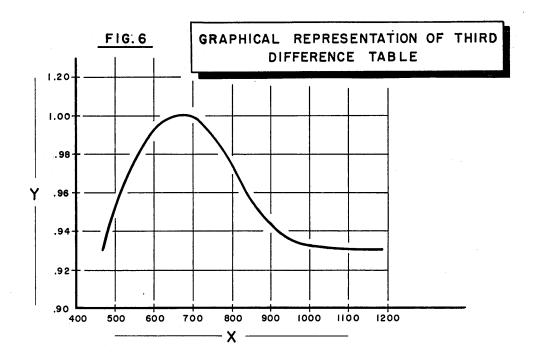
$$y = y_n + p \Delta^1 y_n \tag{2}$$

This is equivalent to ordinary linear interpolation. A graphical representation of the first difference table in Table I is shown in Figure 5.



One may resort to higher order differences to obtain smoother representations of the required function. Second and third difference tables are also shown in Table I. The second difference is the difference between first differences, the third difference is the difference between second differences, and so on. Figure 6 shows a graphical representation of the third difference table given in Table I. In order to make use of higher order differences one must use increasingly involved interpolating procedures. This question will be examined in a moment, but first another aspect of the problem will be considered.

Obviously any type of table can be made a more accurate approximation of the function it represents by increasing the number of values tabulated (i.e. decreasing tabular interval). However, there is a real disadvantage associated with this, particularly when tables are to be expressed on IBM cards. The number of cards necessary goes up in proportion to the number of values tabulated and in many cases to obtain an adequate "smoothness" in a simple table or even a first difference table, an inordinate number of cards is required. This is a considerable handicap for two reasons: first, a large amount of time is required to initially key punch the table, and second, a large amount of time is required to consult the table after it is in card form.



⁴ In many problems "smoothness" rather than "accuracy" determines the number of table cards required. The correlations used in technical calculations are often empirical ones which are not too well defined. This fact does not eliminate the necessity in many studies that the approximating function and its first few derivatives vary continuously.

⁵ The second disadvantage is not too important if a large number of values are to be looked up simultaneously in a table. The problems under discussion, however, require finding only one value in each of several tables for a given problem.

Third difference tables were felt to be the best compromise between ease of construction, speed of use, and both accuracy and "smoothness" of results. Having decided upon third difference tables there remains a choice as to the method of interpolation used in them. The most straight-forward interpolation is done by Newton's formula for forward interpolation. More complicated formulas, such as the central difference formulas of Stirling and Bessel, permit more accurate interpolation in a given difference table. However, the fact that "smoothness" rather than accuracy is generally of controlling importance tends to minimize any advantage to be gained by using these latter equations.

The interpolation formula for third difference tables which has actually been used in this work may be written:

$$y = y_{n-2} + p \Delta^{1} y_{n-2} + p (p-1) \frac{\Delta^{2} y_{n-2}}{2} + p (p-1) (p-2) \frac{\Delta^{3} y_{n-2}}{6}$$
(3)

where p is defined as:

$$p = \frac{x - x_{n-2}}{\Delta x}$$

$$(x_{n-1} \le x \le x_n)$$
(4)

The base value of y and the differences are taken at x_{n-2} since this procedure will give the most accurate value of y for the interval $x_{n-1} \le x \le x_n$. This is because the differences used in equation (3) were calculated from an equal number of points both before and after x.

Illustrative Example

It is desired to calculate the value of y at x = 837 from the third difference table given in Table 1. First, p is calculated from Eq. (4):

$$p = \frac{837 - 750}{50} = 1.740$$

Then, from Eq. (3):

$$y = .9900 + (1.740) (-.0150) + (1.740) (.740) (-.0045) / 2 + (1.740) (.740) (-.260) (.0121) / 6$$

= .9603

^{6.} The tabular interval, Δx , must be constant for a given table of this type.

Card Layout for Third Difference Tables

Figure 7 shows a typical IBM table card. Each card carries the following information:

Cols.			Data
17-19	Code Number	=	identification of a particular table (constant for a given table). All table cards have an X in Col. 17.
20-27	$\mathbf{X}_{\mathbf{n}}$	=	argument value
28-33	y _{n-2}	=	function value
34-39	$\Delta^1 y_{n-2}$	=	first difference
40-45	$\frac{1}{2} \ \Delta^2 y_{n-2}$	=	second difference divided by two
46-51	$\frac{1}{6} \Delta^3 y_{n-2}$	=	third difference divided by six
52-5 9	$\frac{1}{\Delta x}$	=	reciprocal tabular interval for argument (constant for a given table).

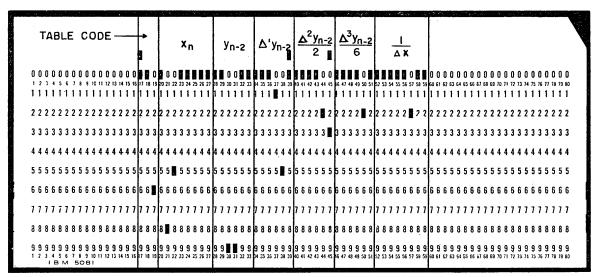


Fig. 7 Table Card

The argument, x, and the reciprocal argument interval, $\frac{1}{\Delta x}$, are eight-digit positive

numbers in the form xxxx.xxxx. The function and its differences are six-digit numbers in the form xx.xxxx. They may be positive or negative; if the latter, they carry an X punch in the last position. The choice of the size of the numbers to be used is, of course, to some extent arbitrary. Modifications should not be made, however, without considering whether changes in control panel wiring also become necessary.

Tables will in general be constructed to cover some limited range of an argument. In order to secure protection against inadvertently over-running a table, each table is

followed and preceded by a card bearing an X punch in Col. 22. This X is a control punch to stop the 602-A calculator should it receive one of these cards during an interpolation calculation.

The last "X in Col. 22" card for each table has an argument value of 9999.9999. The first "X in Col. 22" card has an argument value which is 0.0001 lower than the lowest value the table covers. If a table starts with an argument value of 0000.0000 it has no low limit "X in Col. 22" card. The fact that these error cards will be selected if the table is over-run should become clear in the next section.

Selection of Table Cards

Each of the problems for which this system was designed involves one table look-up in each of 30-60 tables. To do this all the tables are placed in consecutive order of their Code Numbers (Cols. 17-19) and the cards of each table are in consecutive order with respect to their argument values. This "composite" table deck is then placed in the primary feed of an IBM collator. A set of data cards which carry a table Code Number in Cols. 17-19 and the argument value to be looked-up in Cols. 20-27 is placed in the secondary feed. Each set of data cards must contain only one argument value to be looked up in each individual table.

The collator is wired with the control panel shown in Fig. 12. The result of this control is that each data card selects the appropriate table and the card in that table with the next highest (or equal) argument value. The two cards eject together to the second pocket of the collator, with the table card on the bottom. Unselected table cards are rejected to the Primary Select pocket of the collator.

If a data card exceeds the range of the table, it selects the 9999.9999 card with the X in Col. 22. If the data card is below the prescribed range of the table it selects the low error card. (For example, if the lower limit of a table is 500.0000, then a data card requesting a value at 487.0000 would select an error card 499.9999 carrying an X in Col. 22.)

Interpolation Calculation on the 602-A

The merged stack of table and data cards is taken directly from the collator to the card feed of the 602-A. The 602-A is controlled by the interpolation panel which is described under INTERPOLATION CONTROL PANEL.

In this operation all the necessary interpolating information is read from the selected table card by the 602-A and stored. Then the data card is read, the interpolation calculation is performed, and the answer is punched in Cols. 1-8. If the answer is negative the card is X punched in the units position (Col. 8). The calculator then proceeds to the next pair of cards.

The data cards (punched with answers) are now separated from the table cards (X in Col. 17). The latter are remerged with the tables from which they came.

Simultaneous Running of Several Problems

Ten duplicate sets of "composite" table decks are kept on file, each with a digit punch from 9 to 0 in Col. 69. Each of several sets of data cards to be looked-up in tables is assigned a Problem Number which is punched in Cols. 66-69. The last digit of this Problem Number is then compared with the number in Col. 69 of the table cards during the selection operation on the collator. Thus problems with ten consecutive digits in the last column of the Problem Number can be run together in one machine operation. The 602-A calculator performs the interpolation calculation on paired cards without regard to their Problem Number, and thus can deal with any number of problems in one machine run.

Scope and Speed of Operations

Typical problems to which this method has been applied each involve consulting 30-60 tables, depending upon the nature of the problem. The average third difference table used consists of from 5 to 10 cards. Thirty such tables can be run through the collator in a machine time of about one minute. The interpolation calculation on the 602-A takes about four minutes for thirty interpolations.

COMBINATION PROBLEMS

In catalytic cracking yield and quality predictions it is necessary to perform the final calculations, which are sequential in nature, through card-programming. However, many of the numbers which are used in these calculations are secured from difference tables.

Those cards of the program deck which require tabulated data are key punched in Cols. 20-27 with the argument value at which that data is required. These cards in the program deck are always looked-up in the same tables in each problem, so they already carry in Cols. 17-19 the necessary Table Code Number. Once these cards have been key punched with the argument they simply become data cards which can be run through the interpolation procedure in the normal manner. The interpolated answers from this procedure are punched in Cols. 1-8 by the 602-A so that the cards can then be inserted in the proper order in the program deck.

There are actually three classes of cards in a typical program deck:

Class A cards which require data to be key punched in Cols.

1-8 for direct use in the card-programmed calculation. These cards are identified by an X in Col. 2 and a typical card is shown in Fig. 8.

Class B cards which require data to be punched in Cols. 20-27 for table look-ups before use in the card-programmed calculation. These cards are identified by an X in Col. 14 and a typical card is shown in Fig. 9.

Class C cards which require no special key punching.

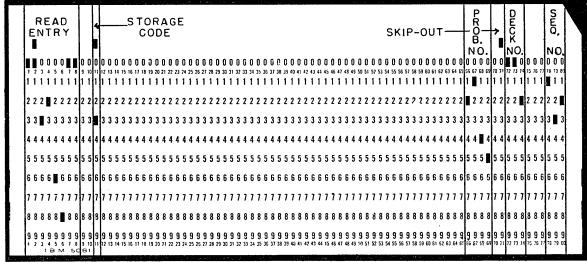


Fig. 8 Class A Card

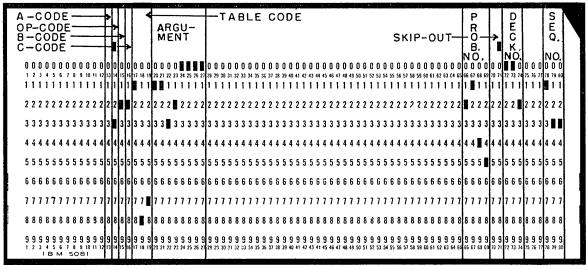


Fig 9 Class B Card

All punches which are invariant from problem to problem, such as identification numbers, control instructions and numerical constants are, of course, pre-punched on the program deck.

It has been found preferable to have the data to be used in Class A and Class B cards key punched into blank cards rather than directly into the program deck. This minimizes

handling of the program deck itself. The blank cards must be key punched with Sequence Numbers (in the case of Class A cards) or Table Code Numbers (in the case of Class B cards) for identification. The Class B cards then go through the table look-up procedure and answers are punched in Cols. 1-8. The data in Cols. 1-8 on both Class A and B cards are then transferred to the actual program deck by the IBM Reproducing Punch. The original data and table look-up values are later listed as a matter of record.

Fig. 10 shows a flow chart of the operations which are gone through in the complete solution of a combination problem. Although this may appear somewhat intricate at first, it is actually quite straightforward for an experienced IBM operator and soon becomes a smooth routine. When a group of problems is done simultaneously the intermediate manual operations are done only once for the group, so that the overall time consumed per problem decreases markedly. ⁷

CARD-PROGRAMMING CONTROL PANEL

This section presents detailed instructions for wiring the control panel which permits the IBM 602-A calculator to function as an elementary card-programmed calculator. It is a modification of a board described by E. V. Hankam of the Watson Scientific Computing Laboratory.

The 602-A calculator to be used with this panel must be an essentially full capacity machine. Eight storage units, eight counters, fourteen pilot selectors and ten co-selectors are used.

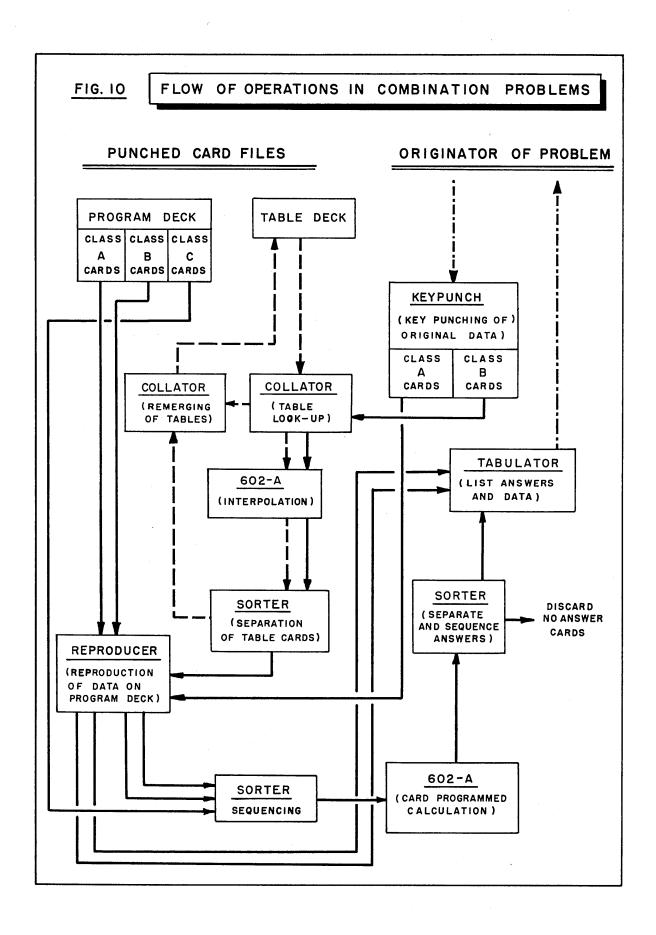
Operations

Addition, subtraction, multiplication and division can be performed on eight-digit numbers with algebraic signs on a fixed decimal basis. The calculator has been wired so that numerical data read in the form ±xxxx.xxxx will automatically be developed to eight-digit answers with the same decimal location. No provision has been made for rounding or dropping of insignificant figures. Eight (or less) digit numbers which cannot be expressed in the form xxxx.xxxx can be handled by the machine. This may, however, require special programming and a consequent reduction in machine speed.

Storage

As many as seven eight-digit numbers can be stored in the machine. Negative numbers are stored in complement form, thus freeing pilot selectors for other operations. All numbers are stored in any one of seven storage units (2), (3),...(8).

^{7.} The desirability of eliminating these intermediate operations is, of course, only minimized by this fact; this is a major reason why it is so advantageous to have the Card-Programmed Electronic Calculator.



<u>Data Cards</u> Numbers may be entered directly from data cards. Negative numbers are identified by a suitable X-punch.

Instruction Cards Data cards are followed by instruction cards. Each instruction card contains a numerical code to perform an operation of the type $A \odot B = C$, i.e., two of the stored factors are selected, an operation is performed on them, and the result of that operation is stored, punched or both. Instruction cards may also carry the number A, instead of obtaining it from storage in the machine.

Notation and Assignment of Units

Brackets enclose counter groups; parentheses enclose storage units.

MC (multiplicand), DD (dividend) [I][1, 2, 3][5, 6, 7, 8]Result of operations = [4][4]Store C-code (i) = $(2), (3), \dots (8)$ Store data and intermediate results MP (multiplier), DR (divisor) (1R) =(1R) (1L)Store B-code (1L) =

Flow of Operations

MULT : $(i) \xrightarrow{P_1} [II] \xrightarrow{P_2} [I] \xrightarrow{P_3} (1R)$; $(i) \xrightarrow{P_4} [II] \xrightarrow{P_5} [I]$; $P_6 \xrightarrow{MPL}$; $[II] \xrightarrow{P_7} (i)$ DIV : $(i) \xrightarrow{} [II] \xrightarrow{} (1R)$; $(i) \xrightarrow{} [II] \xrightarrow{} [I]$; DIV ; $[II] \xrightarrow{} (i)$ ADD : $(i) \xrightarrow{} [II]$; $(i) \xrightarrow{} [II]$; $[II] \xrightarrow{} (i)$ SUB : $(i) \xrightarrow{} [II]$; $(i) \xrightarrow{} [II]$; $[II] \xrightarrow{} (i)$

Remarks: Numbers have to be balance tested, and converted if complements, before being used as factors in multiplication and division. The operation $A \Theta B = C$ is performed such that the first factor A is the multiplier, divisor or minuend.

Programming of Data Cards

Card Form: Col. 1-8 : $\pm A_i$ (X-punch for minus sign in Col. 8)

Col. 11 : storage code (2, 3, ..., 8);

also X-punch to differentiate from instruction cards

Col. 71 : X-punch for SKIP OUT on all cards except those to

be punched

Step	Operation	Instructions	
R	$\pm A_i \longrightarrow [II]$	[II] RI ± (sign is wired from control brush to P-Sel 1)	
		Storage code (Col. 11) is wired (via Digit Sel 2) to p.u. P-Sel 2,3,8 from Read brush	
		X in Col. 11 is wired to P_7 - SKIP from read brush.	
P ₇	[Ⅱ] (i)	[II] RR ; (i) RI ; READ	
		[I] RE ; (resets MC and Remainder on instruction cards)	

Remarks: Only one program step is required for data cards. Since this program step is identical with P_7 of instruction cards, P_1 to P_6 are skipped on data cards. Punching on both data and instruction cards takes place whenever a number is read into (8). On other cards an X-punch in Col. 71 is wired to SKIP OUT.

<u>Programming of Instruction Cards</u> (A \odot B = C, i.e. A_i \odot A_j = A_k)

Card Form: Col. 1-8: numerical data or blank 8
Col. 13: A-code or blank (2,3,...8) 8
Col. 14: Operation - code (1,2,3,4)
Col. 15: B-code (2,3,...8)

Col. 16

Col. 71 : X for SKIP OUT

C-code

Step	Operation	Instructions
R		A-code — via Digit Sel 2 to p.u. P-Sel 2,3,8 from read brush
		Op-code —→ via Digit Sel 1 to p.u. P-Sel 11,14 from read brush
	B-code—→(1L)	(1L) RI, i.e. (1) RI from read brush
	B-code \longrightarrow (1L) C-code \longrightarrow [4]	[4] RI+ from read brush
		R.D.O. P-Sel 2,8 through Co-Sel 9 and 10 p.u. at Read Cycle
	$\pm A \longrightarrow [II]$	[II] RI± (sign is wired from control brush to P-Sel 1)

 $(2, 3, \dots 8)$

⁸ If Col. 13 contains an A-code punch, then Cols. 1-8 must be blank. If Cols. 1-8 contain data, then Col. 13 must be blank.

Step	Operation	Instructions
P ₁	(i) — [II]	(i) RO ; [II] RI+
		N.B. test [II] : P-Sel 9 through Co-Sel 2 p.u. at P ₁
		d.o. P-Sel 28 with "9" pulse through Co-Sel 2
	· · · · · · · · · · · · · · · · · · ·	(1L) RO to p.u. P-Sel 28 through Digit-Sel 2
		P ₄ -SKIP through P-Sel 11 and 12 (if either is p.u.) through T-side of Co-Sel 2
P_2	[II] → [I]	[II] RR ; [I] RI± (± through P-Sel 9)
P_3	[I] — (1R)	[I] RO ; [I] RE ; (1R) RI
P_4	(i) → [II]	(i) RO; [II] RI+ (- for subtraction through P-Sel 12)
		N.B. test [II]: P-Sel 10 through Co-Sel 3 p.u. at P4
1		d.o. P-Sel 28 with "9" pulse through Co-Sel 3
		[4] RR to p.u. P-Sel 28 through Digit-Sel 2
		P ₇ -SKIP through P-Sel 11 and 12 (if either is p.u.) through N-side of Co-Sel 2
P_5	[II] —— [I]	[II] RR; [I] RI± (± through P-Sel 10)
P_6	A [×] B	[II] RI±(through P-Sel 9 and 10 and Co-Sel 4)
	MPL ; [I] RO (T-side of P-Sel 13 or N-side of P-Sel 14)	
		DIV ; (1R) RO ; [I] RI- (T-side of P-Sel 14 or N-side of P-Sel 13)
P ₇	[Ⅱ] 	[II] RR ; (i) RI ; READ
		[I] RE (resets MC or Remainder)

Remarks: Whenever i = 8, (8) PUNCH is wired together with (8) RI on P_7 . An All Cycles impulse is wired to "Punch Interlock" so that punched results can also be read out of (8) on the following instruction card.

Selectors:			d.o.
Pilot-Sel:	1	SIGN of A _i on data cards (control brush)	R. D. O.
	2	a) with A-code from read brush on all cards	end of P ₁
		b) with B-code from beginning of P ₂	end of P ₄
	8	c) with C-code from beginning of P ₅ (through Digit Sel 2 in all cases)	R. D. O. (through Co-Sel 1)

9 N. B. test of [II] to test A at P₁ R. D. O.
10 N. B. test of [II] to test B at P₄ R. D. O.
11 +
12 13 \times from read brushes (Col. 14) through Digit Sel 1 R. D. O.

14 +)

15 free

16 free

17 free

Note: P-Sel 1, 9 and 10 are impulsed at the X p.u.

The other P-Sels are impulsed at the digit p.u.

Co-Sel: 1 : free

 P_1 couple exit P_2 couple exit

4 : Coupled to P-Sel 10

5 & 6 : P₇ couple exit through T-side of P-Sel 13

7 : P₆ (to fill up [II] with "9"s through N-side of Co-Sel 9)

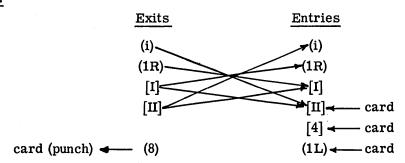
Note: Highest 4 positions of [II] are bussed

8 : free

9 & 10 : read couple

11 & 12 : coupled to P-Sel 11 and 12

Channels:



Shifting:

A number is read out of [II] in two possible ways:

- a) No shift (whenever operation is not MULT)
- b) Shift by four (read out of 5th and drop 4) (whenever operation is MULT)
 - a) is wired through N-side of Co-Sel 5 & 6
 - b) is wired through T-side of Co-Sel 5 & 6

Note: With the exception of the channel of (1R) into [I] the units position of all numbers are read into or out of the 12th position of [I]. This must be done to line up the DD and, for the sake of uniformity, can be done for all other operations.

General Remarks

- 1. There is no provision for reading out the remainder, or rounding.
- 2. (1R) will read in extraneous numbers from data cards; [(1) is impulsed to RI on all cards]; however these numbers will clear out later.
- 3. By means of multiple punches in the storage code a factor can be read from a data card into several storage units. If it is required to read the result C into two storage units, the C-code cannot have a double punch because it is read into a counter from the card.
- 4. The A- or B-code can be left blank so that none of the P-Sel 2, 3,...8 will p.u. This has to be done in case of transfer operations A + O = A (or $O \pm B = \pm B$).
- 5. Instruction cards are blank where data cards are punched, and vice-versa (except for numerical information which may be punched in Cols. 1-8, and X for SKIP OUT in Col. 71).
- 6. When a number is entered in Columns 1-8 of an instruction card, this number will be read into [II] which receives a RI impulse on every card. (P-Sel 1 controls whether it is RI+ or RI-.) The number entered may of course be 10³,..., 10⁻³, and thus can be used to shift any number held in a storage unit by three columns to the left or right.

CARD PROGRAMMING EXAMPLE

As an extremely simple example of card program planning, consider the following equation:

$$w = 1.4300 + 0.2389 \times -0.5432 \left[\frac{x}{y} - z\right]$$

Given the three pieces of data, x, y and z, the problem is to evaluate w.

A sample program planning chart is shown in Fig. 11. The first three cards "load" the calculator with data. The following six cards control the calculation and finally punch the answer into the last card. Several of the instruction cards illustrate the use of cards as direct entries for the factor A in an operation $A \Theta B = C$.

As mentioned above, this is an extremely simple example. Sequential calculations involving more than two hundred cards have been done and even lengthier calculations are planned. In these longer problems it is frequently necessary to introduce new data cards throughout the program deck, rather than merely "loading" the calculator with the first several cards of the deck.

CARD PROGRAMMED 602-A CALCULATOR PLANNING CHART

														;	\vdash	000
1-8	11	13	14	15	16	7.			Stoi	Storage Units				Ċ	+	08-81
Card Entry	St.	A	Op.	В	၁	Skip Out	(2)	(3)	(4)	(5)	(9)	(7)	(8)	An	Ans. No.	Card No.
×	× ~					X	×									100
λ	×e					X	×	y								005
z	X 4					×	×	y	и							003
0.2389			က	7	ည	×	‡ 4	y	13	.2389x						004
1.4300				2	5	×	x	y	Z	1.4300 +.2389x						900
		က	4	7	2	×	ΧIX	y	z	1.4300 +.2389x						900
		2	2	4	2	×	$\frac{x}{y} - z$	y	Z	1.4300 +.2389x						200
. 5432			3	2	2	X	. 5432 $\left[\frac{x}{y} - z\right]$	y	Z	1.4300 +.2389x						800
		2	2	2	8		. 5432 $\left[\frac{x}{y} - z\right]$	y	Z	1.4300 +.2389x			W	00	100	600
	 										:					
f		,	0		ſ		:	•		í			ſ			
Program Deck No.:	Deck I	l	800		Pur	Purpose:	Illustrative Example	ambie		Date:			By:	Ä		

Figure 11

COLLATOR WIRING FOR TABLE LOOK-UP

Figure 12 shows the wiring of the collator for the table look-up operation. After this processing the selected table cards, together with their data cards can now be fed directly into the 602-A.

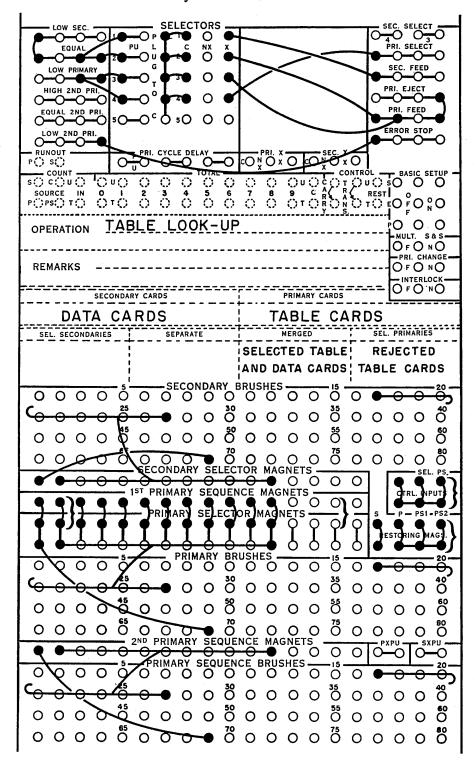


FIGURE 12
WIRING OF COLLATOR FOR TABLE LOOK-UPS

INTERPOLATION CONTROL PANEL

The instructions given below, together with Figure 13, are complete wiring directions for the interpolation calculation discussed earlier. The wiring diagram is only for showing the wiring of channels between storage units, counters, and reading brushes or emitters. It is shown since the use of co-selectors, to prevent back circuits, is somewhat intricate. Control wiring is described in sufficient detail below, and punch wiring (including balance test and conversion) is routine.

The wiring described here gives complete sign control for positive and negative values of the tabulated function and its differences. However, this sign control only holds when the value of x lies in the range $x_{n-1} \le x \le x_n$ where x_n is the first tabulated value of the argument larger than x. (This x_n table card is selected by an x data card when the collator is wired as shown in Figure 12.)

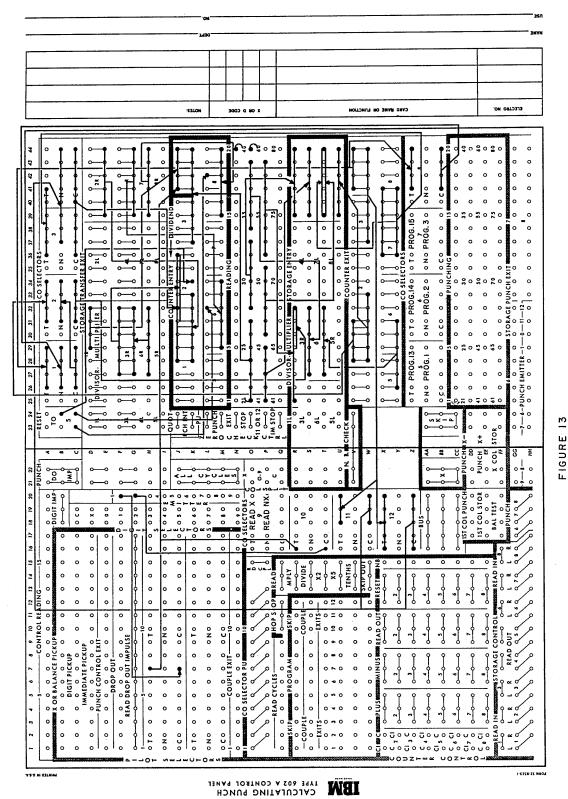
To use this control panel the 602-A requires eight counters, seven storage units, seven pilot selectors and twelve co-selectors.

CONTROL INSTRUCTIONS - INTERPOLATION PROBLEM

Step	Oper	ation	Instructions
Read X	$x_2 \longrightarrow [34]$	(Cols 20-27)	p.u. P-Sel 1 by X in Col 17 (control brush)
*	y ₀ → (2)	(Cols 28-33)	p.u. P-Sel 3 by X in Col 39 (read brush)
	$\Delta^1 y_o \longrightarrow (3)$	(Cols 34-39)	p.u. P-Sel 4 by X in Col 45 (read brush)
	$(\frac{1}{2})\Delta^2 y_o \longrightarrow (4)$	(Cols 40-45)	p.u. P-Sel 5 by X in Col 51 (read brush)
	$\begin{vmatrix} \Delta^{1}y_{\circ} \longrightarrow (3) \\ (\frac{1}{2})\Delta^{2}y_{\circ} \longrightarrow (4) \\ (\frac{1}{6})\Delta^{3}y_{\circ} \longrightarrow (7) \\ \frac{1}{\Delta x} \longrightarrow (1) \end{vmatrix}$	(Cols 46-51)	p.u. P-Sel 6 by X in Col 33 (read brush)
	$\frac{1}{\Delta x} \longrightarrow (1)$	(Cols 52-59)	RDO P-Sel 1
			(1) (2) (3) (4) (7) RI thru T side Co-Sel 9
			[34] RI+ thru T side of P-Sel 1
			Co-Sel 9 is p.u. by couple exit of P-Sel 1
			[12], [78]RE READ & SKIP OUT
Read NX	-x→ [34]		[34]RI- thru N side of P-Sel 1
			[12], [78]RE
P-1	$\frac{1}{\Lambda x}(x_2 - x) \longrightarrow [1$.2]	p. u. Co-Sel 11 & 12
			[12]RI+ [34]RO MPL

Step	Operation	Instructions
P-2	2-p → (1)	p.u. Co-Sel 2 (1)RI [12]RO
P-3	$(2-p) \frac{\Delta^3 y_o}{6} \longrightarrow [78]$	(7)RO [78] RI+ MPL
P-4	$(2-p) \xrightarrow{\Delta^3 y_o} \longrightarrow (7)$	p.u. Co-Sel 10 [78] RO (7) RI [34] RI+ [12] RE
P-5	-(2-p) → [34]	[34] RI - (1) RO [78] RE
P-6	$p \longrightarrow (1)$ $y_{\circ} \longrightarrow [12]$	[34] RO (1) RI [12] RI± through P-Sel 6 N T (2) RO p.u. Co-Sel 8
P-7 & 8	$p \Delta y_{\circ} \longrightarrow [12]$ $p \frac{\Delta^{2} y_{\circ}}{2} \longrightarrow [56]$ $p(2-p) \frac{\Delta^{3} y_{\circ}}{6} \longrightarrow [78]$	12 RI± through P-Sel 3 N (3)RO (4)RO [56]RI+ (7) RO [78] RI+ MPL
P-9	$ \begin{array}{ccc} -1 \longrightarrow [34] \\ p \frac{\Delta^2 y_o}{2} \longrightarrow (6) \\ p(2-p) & \frac{\Delta^3 y}{6} \longrightarrow (7) \end{array} $	Imm. p.u. P-Sel 7 [34] RI- [56] RO (6) RI [78] RO (7) RI
P-10	p-1→ (1)	p.u. Co-Sel 1 [34]RO (1)RI [56]RE [78]RE

Step	Operation	Instructions
P-11 & 12	$p(p-1) \frac{\Delta^2 y_o}{2} \longrightarrow [12]$ $p(p-1) (2-p) \frac{\Delta^3 y_o}{6} \longrightarrow [78]$	12 RI \pm through P-Sel 4 $\frac{N}{T}$ (6) RO (7) RO [78] RI \pm MPL
	·	p.u. P-Sel 2 (and Co-Sel 5, 6, 7 from cpl exit) (used for program extension)
P-13	$p(p-1) (p-2) \frac{\Delta^3 y_o}{6} \longrightarrow [12]$	p.u. Co-Sel 3 & 4 [12] RI± through P-Sel 5 T N [78] RO [34] RE
P-14 & 15	Punch answer	[12] RO (8) RI, punch DO P-Sel 3, 4, 5, 6 READ (Balance test & convert answer)



INTERNATIONAL BUSINESS MACHINES CORPORATION

WIRING OF STORAGE UNIT AND COUNTER ENTRIES AND EXITS FOR INTERPOLATION

31

13 DIGIT FLOATING DECIMAL — MODEL II CPC

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Editor's Note: This article describes a general purpose 13 significant digit floating decimal setup. Complete planning charts for the 605 follow the article. Preceding these charts are notations on planning for the 418 control panel.

If a number is represented as $n\cdot 10^p$, n given to thirteen digits or less and |p|<50, the number is read into the CPC Model II as n and 50+p with the sign of n punched as an X over the last digit of (50+p). For example, $\frac{1}{e}=3.678794411714\times 10^{-1}$, the number read into the CPC would be 367879441171449 and -e as 271828182845950.

Card Layout:

Card Column

1-4	Serial number	
5	Spread read-in control	
6-8	A address	
9	Operation control	
10-12	Baddress	
13-14	C address	
6-20	Ctr grp #1 on SRI	
21-35	Ctr grp #2 on SRI or channel A card read-in	
36-50	Ctr grp #3 on SRI or channel B card read-in	
51-65	Ctr grp #4 on SRI	
66-80	Ctr grp #5 on SRI or compare number with channel C	

Spread Read-In Controls:

The card preceding one in which there are to be numbers read into the five counter groups must contain:

- (1) 9 punched in column 5 signals SRI.
- (2) Ctr addresses, 1,2,3,4,5 punched in column 5. If selective SRI is desired the absence of any of the numbers 1-5 will prevent the number in the card from disturbing the contents of that counter group.

Counter Controls:

There are five counter groups in the 418:

Ctr. grp.	Address	418 Counters
#1	91	2A,2B,6A,6B
#2	92	2C, 2D, 6C, 6D
#3	93	4A, 4B, 4C, 4D
#4	94	8A,8B
#5	95	8C,8D

The counter groups are controlled the same as storage registers in that a number remains in the counter group and is not reset on any read-out, but reading into the counter group resets the counters to zero before read-in. Numbers read into the counter groups are available with a one card delay. Storage registers have the normal two card delay. There is no provision for adding numbers in the counter. The counter groups may be addressed on channels A, B, or C independently of one another.

Storage Control:

It is necessary to use two storage registers to store a thirteen digit number and the two digit exponent. To read a number into a storage bank give a C address to a particular storage register in the bank. This will store the eight high order digits, the two digit exponent, and the sign. The following card should have a 6 punched in column 9 and a C address to another storage register in the same bank. This will store the five low order digits, and again the exponent and sign. It will be noted that A and B addresses consist of three digits. Ordinarily the two high order digits are used for card read-in, counter group, or C \longrightarrow A (or B) addresses. The third digit is used for storage control. To call a number from a storage bank on channel A or B a three digit address is used. For example, a 256 in channel A will read-out of storage registers 25 and 26 in the following manner. The eight high order digits of 25 will become the eight high order digits of the thirteen digit number, the two low order digits will become the exponent, and the sign will come from 25, the eight high order digits of 26 (including the first three which are zeros) will become the five low order digits of the thirteen digit number.

If the contents of 25 are 52718281850 and the contents of 26 are 50002845950, then this will read-out on an A address of 256 as: 271828182845950 with the 5 in the high order position of 25 becoming the sign.

address it will come out as 90000000.....50, the blank spaces will read into the 605 as zeros.

Spread Read-Out Control:

It is possible to read-out of the five counters, print, and punch the numbers contained therein by punching a 9 in column 14. Follow this card by a blank card. It is possible to read-out and print, without punching by the above address and putting Switch #2 in A position. Either operation does not disturb the numbers in the counters.

Compare Channel C:

This operation is mainly for test decks. An X punch in column 25 allows the channel C result of the previous card to be compared with the numbers in 66-80 of this card. If they do not compare the machine will stop. Switch #3 in A position does not allow comparing even if there is an X in column 25.

Octal Conversion:

The operations punch 8 in column 9 will convert the thirteen place floating point decimal number in A to a thirteen place floating point octal number. The exponent readout will be in true figures. Therefore, the number read-in on A must be positive as the sign of C in this operation is reserved for the exponent. For example, the number $\frac{2}{8} + \frac{1}{8^2} + \frac{9}{8^3} + \frac{5}{8^4} + \frac{3}{8^5}$ reads-in on A as 284515380859449 as a decimal number. Its octal equivalent will read-out as 221530000000001- or $e^{5.5}$ reads-in as 244691932264252 and its octal equivalent is 364542211710303. The exponent as well as the number is converted to octal numbers.

Switches:

Set-up Switch #1 on	List every card during calculation			
Set-up Switch #2 on	Double space before printing			
Switch #1 A position	Used in conjunction with Set-up Switch #1, lists every card, but does not calculate.			
Switch #2 A position	Does not allow punching			
Switch #3 A position	Does not allow comparing			

X and Y Puncl	h Contr	ols:
Col. 1	Y	List this card
Col. 1	X	List the next card
Col. 6	x	A
Col. 7	X	-A
Col. 8	x	Double space before printing
Col. 9		See operations controls
Col. 10	X	B
Col. 11	X	-B
Col. 12	X	Eject paper to next sheet
Col. 14	X	Stop machine if C of this card is negative
Col. 25	X	Compare 66-80 of this card with C of preceding card
Col. 20	X	Number in 6-20 is negative
Col. 35	X	Number in 21-35 is negative
Col. 50	X	Number in 36-50 is negative

Number in 51-65 is negative

Number in 66-80 is negative

605 Operations

Col. 65

Col. 80

X

X

Code in Col. 9	Result
- Blank	Transfer A to C without performing other operations
1	A + B
3	$A \cdot B$
4	A ÷ B
5	\sqrt{A} , Read-in B as 99999990002500
6	Split number for storage (See Storage Controls)
8	Octal conversion (See Write-up)
Special Controls	
2	Do not round on multiply or add
7	Do not shift left if zeros are present in high order position of C result
9	Convert exponent of A to floating decimal number
Y	Replace exponent of A by B exponent
Х	Add two high order digits of B to A exponent. High order digits of B in the form 50 + p, where p is the change desired in A exponent.

The special controls are used mainly in reduction of arguments for ease of series calculations. Operation code 7 is used for conversion of floating to fixed decimal numbers.

Notations for Planning 418 Panels

The 605 panel, as designed, will fit any standard 605 without additional equipment or modifications. The 605 must be made to operate, however, as if the tubes and units at I-5-U and I-7-T were removed.* The 418 panel as designed at this installation requires an additional Field Selector, therefore the 418 wiring diagrams are not included. It would seem possible to design a 418 panel for a standard machine which will perform all the manipulations described in the write-up except possibly Spread Read-In and Spread Read-Out.

Channel A: Read the digits into FS 1&2, FS 3&4 (five low order positions)

Read the exponent into the two low order positions of the MQ

Channel B: Read the digits into GS 1 & 2, GS 4

Read the exponent into the two high order positions of the MQ

Channel C: Read the digits (R&R) out of the counter exit; Read the exponent

out of the two low order positions of GS 3, except on square root. On square root pick-up a selector to read the exponent out of the

two high order positions of GS3.

Operation Code X: Pick up a selector to read the two high order digits of B into the

B exponent position of the MQ.

Operation Code Y: Pick up a selector to read the B exponent into the A exponent

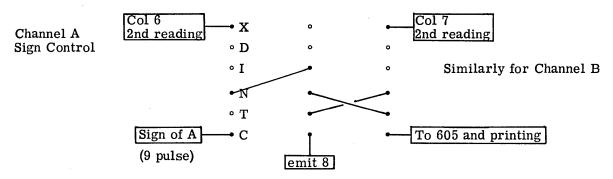
position of the MQ.

Operation Code 7: Pick up a selector to "emit 5" into Channel Shift

Operation Code 8: Wire sign hub of GS 3 to counter sign hub to give proper sign to

exponent on octal conversion.

There is no provision in the 605 for subtraction. This is done in the 418 by changing the sign before reading into the 605. The following method will enable one to get the negative, absolute, or negative absolute value of A or B. Assume all sign controls are converted to "9 pulses". Then three pilot selectors are wired as follows:



^{*} This can be handled by special arrangement with the IBM Corporation

					F	ANEL A.
П	READ OUT	READ IN	SHIFT	PRO	GRAM	COMMENT
	EXIT 1	EXIT 2	EXIT 3	SUPP	PU	COMMENT
1	FS1 &2	½ add		0	1	
2	GS1 &2	ZT	BTSS, Reset	1	all	
3	MQ*	ctr+	**			*GS4ROS ** in 6S; Prog Rpt, Rpt Del PU+; in 3 E
4	RO*	GS3	out 4 **	2		*R&R 🕜 **not on 🕔
5	emit 5	ctr+ *	in 2 **	<u> </u>	all	*ctr-(x), (E _x); ctr-, BTSS(8); MQRI(\(\sigma\) ** in 5(\(\sigma\); in 4 (E _x)
6	GS3 *	ctr- **	in 4 ***	2		*R&R (E,) ** × (/); MQRI (E,) ***not on (/), (E,)
7	GS3 *	ctr- **	***	0		*GS4RO(); RO(8); emit 5 (£, **ctr + (x), (/), (£,); GS3RI(8)*** in 6 (T); BTSS(+); in 2 (£,
8	emit 1 *	ctr+ **		4	all	*MQRO(+), (T)**GS3RI(+), (T); ctr-(+)
9	R&R	GS3 *	**	<u> </u>	<u>@</u>	*MQRI(+), (T); GS4RI(8) ** out 5(1); RS#5PU(+)
10	GS3 * FS1 &2 *	MQ ** ctr+ **	in 5	3)© (S)	*MQRO (E)** FS1 &2 RI (E) *FS3 &4RO (T)** GS4RI (T)*** in 6 (E)
11 12	MQ*	ctr-, BTSS	Reset	8	E,	*GS1&2 RO(8)
13	FS1 &2	ctr+	in 6	P	(A)	*G51 &2 RO(6)
14	FS1 &2	ctr+	in 5	M	⊙ Ø	
15	GS1 &2	+	m 0		٠	
16	R&R	FS1 &2			⊕Ø	
17	FS1 &2	ctr+	in 6	$\vdash \vdash$	-	
18	FS3 & 4	ctr+	in 6	P	8	
19	FS3&4	ctr+	in 5	M	$\odot \oslash$	
20	MQ	FS1 &2	in 4			
21	GS1 &2	+			(8)	AND THE RESIDENCE OF THE PARTY
22	R&R	FS3&4			⊕⊘	
23	FS3&4	ctr+	in 6			
24	MQ	FS3 &4			8	
25	GS1 &2	÷	Reset		\odot	
26	MQ	ctr+			⊕ Ø	
27	emit 5	½ add	in 2			
28	R&R	MQ	out 3		⊕ Ø	
29	MQ	ctr+			8	
30	FS3&4	ctr+	in 4			
31	FS1 &2	ctr+	in 6		⊕(V) (8)	
32	GS4	MQ			8	
33	RO	GS4*		<u> </u>		*MQRI(8)
34	R&R	FS1 &2	out 6		⊕ Ø	
35	FS1 &2	×		1	(8)	
36	R&R*	FS3 & 4	out 6	10	00	*MQRO(8)
37	FS3 &4	ctr+	in 3	0	$\odot \emptyset$	
38	GS1 &2	+ FG2 6.4	Prog Rpt	1		
39	R&R	FS3&4	in 6	8	(A)(A)	
40	FS3 &4 MQ	ctr+ FS3&4	in 6 Rpt Del PU*	10	⊕Ø	*Rpt Del DO(RS7T)
41	GS1 &2	+	Reset	 		Apr 20. 20 (a)
43	MQ	ctr+		 	⊕∅	
44	FS3 &4	ctr+	in 6	 		
45	emit 5	½ add	in 2	\vdash		
46	R&R	FS3&4	out 3	_	⊕Ø	
47	FS1 &2	ctr+	in 6	1		
48	GS4	ctr+	RS#6 PU	1		
49	FS3 &4	ctr-		(1)	⊕Ø	
50	emit 5	MQ	in 5	18		
51	GS4	×	1	10	1	
_	R&R	GS4	out 6	10		
-	GS1 &2	×	Prog Rpt *		Ø	*not(RS8T)
	FS3&4*	×	RS # 7 PU			*FS1 &2 RO (RS8T)
55	R&R	FS3&4	out 6	7	_	
56		ctr+		7	∅	
57	GS1 &2	ctr-, BTSS	Reset	7		
	FS3&4	GS1 &2		P		
_	GS4	FS3&4 *	RS#8 &9 PU	109	∅	*ctr+ (RS8T)
60	RO	GS4	Rpt Del PU	19	<u> </u>	

READ OUT	PANEL B.						
Mark				 	RAM	COMMENT	
2 054				SUPP	PU		
3 RO			Rpt Del DO			W. 194	
4 RAR					(8)	**************************************	
5 MO							
S emit 8			out 6	ļ			
First Fir							
S RO						······································	
				 	اها		
10 F8344							
12 RR R *			in 2 *		ØΘ.	*RTSPII #1 (T)	
12 RR R *			· · · · · · · · · · · · · · · · · · ·	10	189	DIDIO II W	
13 FS1842						*RO(T)**MORI(X) ***not on (T)	
14 (S1842 FS1842 * Out 6	13 FS1 &2	ctr+	in 6		(XA)		
15 RRR	14 GS1 &2	FS1 &2 *			(A)	* × (X)	
16 RRR	15 R&R *	 	out 6	0			
17 CS44	16 R&R	FS3&4	*		\otimes	*out 6⊗	
18 GS1 62* ctr. ** in 3 *** (8)	17 GS4*	MQ**] @ [*MQRO $+$ ** $\frac{1}{2}$ add $+$	
21 RéR	18 GS1 &2*	ctr+ **	in 3 ***	13		*emit 8(+) **ctr-, BTSS(+) *** not on(+)	
21 RéR	19 RO	GS4	out 6	3	⊗⊕		
23 GS1 &2 MQ			in 6	3	[① [
23 GS1 &2 MQ			out 3	3			
24 R&R GS1&2 out 6 3				3	⊗⊙		
25 FS1 & 2				3	(T)		
26 GS1&2 ctr+ 27 FS3&4 ctr+ 28 FS3&4 ctr+ 30 SS3&4 ctr+ 31 R&R FS3&4 out 6 32 FS3&4 ctr+ 33 GS1&2 ctr+ 34 RO GS4 Ctr+ 35 RO GS1&2 out 5 36 RO MQ Prog Rpt P 38 GS3 ctr+ 39 GS3 ctr+ 30 GS1&2 ctr+ 30 GS1&2 out 5 30 FS3&4 ctr+ 31 R&R FS3&4 out 4 32 FS3&4 ctr+ 33 GS1&2 ctr+ 34 RO GS4 GS4DO M 35 RO GS1&2 out 5 36 RO MQ Prog Rpt P 38 GS3 ctr+ 39 GS3 ctr+ 30 GS1&2 ctr+ 31 FS3&4 ctr-, BTSS in 3, Reset P 44 MQ FS3&4 in 5 45 R&R GSA GS4 ctr-, BTSS in 5 GSA 46 Prog Rpt, Rpt Del PU RS #1 PU C22 47 Prog Rpt, Rpt Del PU RS #1 PU C22 48 emit 8 MQ in 5 48 emit 8 MQ in 5 49 emit 1 * ctr+ 40 GS1&2 in 4 *** GS4 51 MQ GS1&2 * in 4 *** GS4 52 GS3 CTr+ 54 R&R GS3 Rpt Del DO GS4 55 GS4 ½ add GS4 56 emit 1 * ctr-, BTSS *** 57 R&R GS4 ½ add GS4 58 FS3&4 GS4 GS4 59 RS\$3,4, &10 PU FS3&4 GS1&2 RI (2) 59 RS\$3,4, &10 PU FS3&4 GS1&2 RI (2) 59 RS\$3,4, &10 PU FS3&4 GS1&2 RI (2) 50 RS\$3,4, &10 PU FS3&4 GS1&2 RI (2)			out 6	<u> </u>			
27 FSS & 4				3			
28 FS3&4 ctr+ in 6 29 R&R FS3&4 out 6 30 FS3&4 ctr+ 31 R&R FS3&4 out 4 32 FS3&4 ctr+ 33 CS1&2 ctr+ 34 RO GS4 GS4 DO M 35 RO GS1&2 out 5 P 36 RO MQ Prog Rpt P 37 emit 1 ZT Reset P 38 CS3 ctr+ GS4 PU P 39 emit 1 ctr- 40 R&R GS3 P 41 emit 1 FS3&4 in 6 P 42 CS1&2 ctr+ 43 FS3&4 ctr-, BTSS in 3, Reset P 44 MQ FS3&4 in 5 45 RAR FS3&4 in 5 46 Prog Rpt, Rpt Del PU RS #1 PU 47 Prog Rpt, Rpt Del PU RS #2 PU 48 emit 8 MQ in 5 49 emit 1 * ctr- 50 emit 8 + Reset * (24) 49 emit 1 * ctr- 50 emit 8 + Reset * (24) 51 MQ GS1&2 * in 4 *** GS4 52 CS3 CT*+ 53 CS4				(3)	(T)		
29 R&R FS3 &4 out 6 30 FS3 &4 ctr+ 31 R&R FS3 &4 out 4 32 FS3 &4 ctr+ 33 GS1 &2 ctr+ 34 RO GS4 GS #4 DO M 35 RO GS1 &2 out 5 P 36 RO MQ Prog Rpt P 37 emit 1 ZT Reset P 38 emit 1 ctr- 40 R&R GS3 40 emit 1 FS3 &4 in 6 41 emit 1 FS3 &4 in 6 42 GS1 &2 ctr+ 43 FS3 &4 ctr- 44 RQ FS3 &4 in 5 45 R&R GS1 &2 out 6 46 Prog Rpt, Rpt Del PU RS #1 PU 47 Prog Rpt, Rpt Del PU RS #2 PU 48 emit 1 * ctr- 49 emit 1 * ctr+ 40 R&R GS3 50 emit 1 * ctr- 40 R&R GS3 50 emit 1 (ctr- 40 R&R GS3 40 P 41 emit 1 FS3 &4 in 6 41 emit 1 42 GS1 &2 ctr+ 43 FS3 &4 ctr- 44 RQ FS3 &4 in 5 50 emit 8 + Reset * (23) 51 emit 8 + Reset * (24) 52 GS3 ctr+ 54 R&R GS3 55 R&R GS3 66 RO MQ 65 R&R GS3 67 P 68 emit 1 * ctr- 68 FS1 &2 cmt 6 68 4 68 FS3 &4 jadd 68 FSS &4 SSS			10	3			
SSS & Carr			 	<u> </u>	la l		
31 R&R FS3&4 out 4 8 32 FS3&4 ctr+ in 6 33 GS1&2 ctr+ in 6 34 RO GS4 GS#4DO M 35 RO GS1&2 out 5 P 36 RO MQ Prog Rpt P 38 GS3 ctr+ GS#4PU P 39 emit 1 ctr- P,NZ 40 R&R GS3 P 41 emit 1 FS3&4 in 6 P 42 GS1&2 ctr- P 43 FS3&4 in 6 P 44 MQ FS3&4 in 5 45 R&R FS1&2 out 6 GS4 46 Prog Rpt, Rpt Del PU RS #1 PU (22) 47 Prog Rpt, Rpt Del PU RS #2 PU (23) 48 emit 8 MQ in 5 (23) 49 emit 1 * ctr+ in 6 ** (24) 49 emit 1 * ctr+			out 6		ا ۱۳		
32 FS3 &4			out 4		 		
33 S1 & 2			Out 4		1 1		
34 RO GS4 GS#4DO M 35 RO GS1&2 out 5 P 36 RO MQ Prog Rpt P 37 emit 1 ZT Reset P 38 GS3 ctr+ GS#4PU P 39 emit 1 ctr- P,NZ 40 R&R GS3 P 41 emit 1 FS3&4 in 6 P 42 GS1&2 ctr+ P 43 FS3&4 ctr-, BTSS in 3, Reset P 44 MQ FS3&4 in 5 8 45 R&R FS1&2 out 6 GS4 46 Prog Rpt, Rpt Del PU R8 #1 PU (22) 47 Prog Rpt, Rpt Del PU R8 #1 PU (22) 48 emit 8 MQ in 5 (23) 49 emit 1 * ctr+ in 6 ** (24) 50 emit 8 + Reset * (24) 51 MQ GS1&2 * in 4 ** GS4 52 GS3 ctr+ Prog Rpt (12) 53 emit 1 ½ add (34) 54 R&R GS3 Rpt Del			in 6	 	ا ۳ ا		
35 RO				м			
36 RO MQ Prog Rpt P 37 emit 1 ZT Reset P 38 GS3 ctr+ GS #4 PU P 40 R&R GS3 P B 41 emit 1 FS3 &4 in 6 P 42 GS1 &2 ctr+ P B 43 FS3 &4 ctr-, BTSS in 3, Reset P 44 MQ FS3 &4 in 5 B 45 R&R FS1 &2 out 6 GS 4 46 Prog Rpt, Rpt Del PU R8 #1 PU (22) 47 Prog Rpt, Rpt Del PU R8 #2 PU (23) 48 emit 3 + Reset * (24) 49 emit 1 * ctr+ in 6 ** (24) 50 emit 8 + Reset * (24) 51 MQ GS1 &2 * in 4 ** GS4 52 GS3 ctr+ Prog Rpt (12)				 	ികി		
37 emit 1			 		1 0 1		
38 GS3	37 emit 1						
39 emit 1	38 GS3	ctr+			18		
41 emit 1 FS3 & 4 in 6 P 8 42 GS1 & 2 ctr+ P P 43 FS3 & 4 ctr-, BTSS in 3, Reset P 44 MQ FS3 & 4 in 5 8 45 R & R FS1 & 2 out 6 GS 4 46 Prog Rpt, Rpt Del PU RS #1 PU (22) 47 Prog Rpt, Rpt Del PU RS #2 PU (23) 48 emit 8 MQ in 5 (22) 49 emit 1 * ctr+ in 6 ** (24) 50 emit 8 + Reset * (24) 51 MQ GS1 & 2 * in 4 ** GS4 52 GS3 ctr+ Prog Rpt (12) 53 emit 1 ½ add (16) (16) 54 R & R GS3 Rpt Del DO GS4 55 GS4 ½ add GS4 56 emit 1 * ctr-, BTSS ** *** 57 R & R GS4 BTSS, Reset (12) 58 FS3 & 4 GS4 Prog Rpt, Rpt Del PU (23) 59 RS #3, 4, & 10 PU FS3 & 4 GS1 & 2 RI (23)	39 emit 1	ctr-	,	P, NZ			
42 GS1 &2 ctr+ P 43 FS3 &4 ctr-, BTSS in 3, Reset P 44 MQ FS3 &4 in 5 8 45 R &R FS1 &2 out 6 GS4 46 Prog Rpt, Rpt Del PU RS #1 PU (22) 47 Prog Rpt, Rpt Del PU RS #2 PU (23) 48 emit 8 MQ in 5 (22) 49 emit 1 * ctr+ in 6 ** (24) *GS3RO (RS3D)** not on (RS3D) 50 emit 8 + Reset * (24) *mot on (RS3D) *not on (RS3D) 51 MQ GS1 &2 * in 4 ** GS4 *ctr+(RS3D)** in 2(RS3D) 52 GS3 ctr+ Prog Rpt (12) 8 53 emit 1 ½ add (58 4 (58 4 (58 4 55 GS4 ½ add GS4 (58 4 (58 4 *FS1 &2 RO(RS3D)*** ctr+(RS3D)**** in 6(RS3D)*** 57 R &R GS4 BTSS, Reset (12) (23) (24) *FS1 &2 RO(RS3D)**** ctr+(RS3D)**** in 6(RS3D)*** <t< td=""><td>40 R&R</td><td>GS3</td><td></td><td></td><td></td><td></td></t<>	40 R&R	GS3					
42 GS1 & 2 ctr+ P 43 F53 & 4 ctr-, BTSS in 3, Reset P 44 MQ F53 & 4 in 5 8 45 R & R F51 & 2 out 6 GS 4 46 Prog Rpt, Rpt Del PU RS #1 PU (22) 47 Prog Rpt, Rpt Del PU RS #2 PU (23) 48 emit 8 MQ in 5 (22) 49 emit 1 * ctr+ in 6 ** (24) 50 emit 8 + Reset * (24) 51 MQ GS1 & 2 * in 4 ** GS4 52 GS3 ctr+ Prog Rpt (12) 53 emit 1 ½ add (16) (16) 54 R & R GS3 Rpt Del DO GS4 55 GS4 ½ add GS4 56 emit 1 * ctr-, BTSS ** *** (17) (17) (17) (17) (18) **FS1 & 2 RO (RS3T) *** ctr+ (RS3T) **** in 6 (RS3T) ***** in 6 (RS3T) ******** in 6 (RS3T) ********** in 6 (RS3T) ************	41 emit 1	FS3 &4	in 6	P] ⑧ [
44 MQ FS3&4 in 5 8 45 R&R FS1&2 out 6 GS 4 46 Prog Rpt, Rpt Del PU RS #1 PU (22) 47 Prog Rpt, Rpt Del PU RS #2 PU (23) 48 emit 8 MQ in 5 (22) 49 emit 1 * ctr+ in 6 ** (24) *GS3RO (RS3T) ** not on (RS3T) 50 emit 8 + Reset * (24) *not on (RS3T) *not on (RS3T) 51 MQ GS1&2 * in 4 ** GS4 *ctr+(RS3T) ** in 2(RS3T) 52 GS3 ctr+ Prog Rpt (12) 53 emit 1 ½ add (16) (8) 54 R&R GS3 Rpt Del DO GS4 *FS1&2 RO(RS3T) ** ctr+(RS3T) *** in 6(RS3T) 55 GS4 ½ add GS4 BTSS, Reset (12) 56 emit 1 * ctr-, BTSS ** *** (17) 8 *FS1&2 RO(RS3T) ** ctr+(RS3T) *** in 6(RS3T) 57 R&R GS4 BTSS, Reset (12) (23) 8				P			
45 R&R	43 FS3 &4	ctr-, BTSS	in 3, Reset	P	_ T		
46 Prog Rpt, Rpt Del PU RS #1 PU (2) 47 Prog Rpt, Rpt Del PU RS #2 PU (23) 48 emit 8 MQ in 5 (22) 49 emit 1 * ctr+ in 6 ** (24) *GS3RO (ES3T) ** not on (ES3T) 50 emit 8 + Reset * (24) *not on (ES3T) 51 MQ GS1 &2 * in 4 ** GS4 *ctr+(RS3T) *** in 2(ES3T) 52 GS3 ctr+ Prog Rpt (12) (12) (12) (12) (12) (13) (14) (15) (1		 		ļ	⑧		
47 Prog Rpt, Rpt Del PU RS #2 PU (23) (8) 48 emit 8 MQ in 5 (22) *GS3RO (RS3T)** not on (RS3T) 49 emit 1 * ctr+ in 6 ** (24) *GS3RO (RS3T)** not on (RS3T) 50 emit 8 + Reset * (24) *not on (RS3T) 51 MQ GS1 &2 * in 4 ** GS4 *ctr+(RS3T)** in 2(RS3T) 52 GS3 ctr+ Prog Rpt (12) (12) (12) 53 emit 1 ½ add (12) (13) (14) (15) <			out 6				
49 emit 1 * ctr+ in 6 ** (24) 8 *GS3RO (ES3T) ** not on (ES3T)		 	1	(22)	_		
49 emit 1 * ctr+ in 6 ** (24) 8 *GS3RO (ES3T) ** not on (ES3T)				(23)	18		
50 emit 8 + Reset * (24) (24) (24) (24) (25) (25) (25) (25) (25) (25) (24) (25) (24) (25)				(22)		+00000 6000 ++ + 6000	
51 MQ GS1 & 2 * in 4 ** GS 4 *ctr+(RS3T) ** in 2(RS3T) 52 GS3 ctr+ Prog Rpt (12) 53 emit 1 ½ add (16) 54 R&R GS3 Rpt Del DO GS 4 55 GS4 ½ add GS4 56 emit 1 * ctr-, BTSS ** *** (17) (17) (17) 57 R&R GS4 BTSS, Reset (12) 58 FS3 & 4 GS4 Prog Rpt, Rpt Del PU (23) 59 RS #3, 4, & 10 PU FS3 & 4 GS1 & 2 RI (23) (8)					ا ۾ ا		
52 GS3 ctr+ Prog Rpt (12) 53 emit 1 ½ add (16) 54 R&R GS3 Rpt Del DO GS 4 55 GS4 ½ add GS4 56 emit 1 * ctr-, BTSS ** *** (17) (8) *FS1&2 RO(RS3D *** ctr+(RS3D **** in 6(RS3T) *** in 6(RS3T) *** 57 R&R GS 4 BTSS, Reset (12) 58 FS3&4 GS 4 Prog Rpt, Rpt Del PU (23) 59 RS *3, 4, &10 PU FS3&4 GS1&2 RI (23) (8)					١७١		
53 emit 1 \frac{1}{2} add (16) (8) 54 R&R GS3 Rpt Del DO GS4 55 GS4 \frac{1}{2} add GS4 56 emit 1 * ctr-, BTSS ** *** (17) (8) *FS1&2 RORS3T) ** ctr+RS3T) *** in 6RS3T 57 R&R GS4 BTSS, Reset (12) 58 FS3&4 GS4 Prog Rpt, Rpt Del PU (23) 59 RS #3, 4, &10 PU FS3&4 GS1&2 RI (23) (3)		 			 	*cir+ (83T) ** in 2 (883T)	
54 R&R GS3 Rpt Del DO GS 4 55 GS4 \$\frac{1}{2}\$ add GS 4 \$\frac{17}{2}\$			Prog Rpt		اھا		
55 GS4 \$\frac{1}{2}\$ add GS4 \$\frac{1}{2}\$ add \$\frac{1}{2}\$ add \$\frac{1}{2}\$ add \$\frac{1}{2}\$ \$		·	Rnt Del DO		╽╝╟		
56 emit 1 * ctr-, BTSS ** *** (1) 8 *FS1&2 RO(RS3T) ** ctr+(RS3T) *** in 6(RS3T) 57 R&R GS4 BTSS, Reset (12) 58 FS3&4 GS4 ProgRpt, RptDelPU (23) 59 RS #3,4, &10 PU FS3&4 GS1&2 RI (23)				G5 4	 		
57 R&R GS 4 BTSS, Reset (12) 58 FS3 &4 GS 4 Prog Rpt, Rpt Del PU (23) 59 RS #3,4, &10 PU FS3 &4 GS1 &2 RI (23) (23) (3)				(17)	la l	*FS1 &2 RO(RS3T) ** ctr+(RS3T) *** in 6(RS3T)	
58 FS3 & 4 GS 4 Prog Rpt, Rpt Del PU (23) 59 RS #3, 4, & 10 PU FS3 & 4 GS1 & 2 RI (23) (3)				(12)	╽╙╎	TOTAL NO COLOT	
59 RS #3, 4, &10 PU FS3 &4 GS1 &2 RI (23) (8)			 	(23)			
80 cmit 1 ctn PTCC Boot				(23)	le l	· · · · · · · · · · · · · · · · · · ·	
Too lemmin Cur-, B155 Reset (23)	60 emit 1	ctr-, BTSS	Reset	23	1 ~ 1		

	PANEL C.									
	READ OUT	READ IN	SHIFT	PROG	RAM					
	EXIT I	EXIT '2	EXIT 3	SUPP	PU	COMMENT				
1	emit 8	ctr+	GS#3 PU	P						
2	emit 4	ctr-, BTSS			⊕					
3	emit 4	ctr+	GS #1 PU	P						
4		ctr-, BTSS								
5		ctr+	GS #2 PU	P] ⊕					
7		ctr-, BTSS	Reset			· · · · · · · · · · · · · · · · · · ·				
8	FS1 &2 R&R	ctr+ FS3&4	out 3	GS3 GS3	⊕					
9	Run	FS1 &2	04. 0	GS3						
10	FS1 &2	ctr+	in 2	GS1						
11	RO	FS1 &2	out 6	GS1] ⊕					
12	R&R	MQ		GS1	1					
13	FS3&4	ctr+		GS1						
14	MQ	ctr+	in 6	GS1] ⊕					
15	R&R	FS3 &4	out 5	GS1						
16	FS1 &2	ctr+	in 4	GS2	⊕					
17	RO R & P	FS1 &2	out 6	GS2	1					
18	R&R FS3&4	MQ ctr+		GS2 GS2						
20	MQ	ctr+	in 4	GS2	⊕					
21	R&R	FS3&4	out 3	GS2	1 🖤					
22	FS1 &2	ctr+	in 5	M	-					
23	RO	FS1 &2	out 6	M						
24	R&R	MQ	-	M	⊕					
25	FS3&4	ctr+		М						
26	MQ	ctr+	in 3	M] ⊕					
27	FS3 &4	ctr+	in 2	P						
28	GS4	MQ *	**		∫⊗⊕	*ctr+(+) in 3(+)				
29	RO	GS1 &2	out 6	3						
30	GS1 &2 emit 5	ctr- ½ add	in 6 in 2	6	⊗⊕					
32	RO	FS3 &4	out 3	<u> </u>						
33	emit 5	½ add	in 2	6	1					
34	emit 4	½ add	in 3	6	⊗⊕					
35	R&R	GS4	out 4							
36	FS1 &2	× *	**			*ctr+(+) ** in 5(+)				
37	GS1 &2	ctr+	in 3 *		⊗⊕	*in 5(+)				
38	GS4	ctr+			1					
39	GS4	MQ		ļ						
40	RO	FS1 &2	out 6	ļ .	4					
41	R&R emit 1	GS4 GS1 &2	in 6	l	1					
43	FS1 &2	GSI & Z	III 0	 	ļ					
44	GS1 &2	ctr-, BTSS	in 3, Reset	<u> </u>	1					
45		ctr+			1					
-	emit 1	ctr+		(13)	 					
47		ctr-		P	1					
48	R&R	GS3								
49		ctr-	in 2	(14)						
	FS3&4	ctr+	*	<u>(1</u>)	1	*Reset 🖭				
51		ctr+	in 2	P	ļ	***************************************				
	FS1 &2	FS3 &4	in 2	P	4					
	FS3 & 4	ctr+	in 6	P	1					
55	RO RO	FS1 &2 GS4	out 6	P	 					
56		ZT	Reset	P	1					
57	Prog Rpt	Rpt Del PU*	RS #6 PU	(15)	1	*Rpt Del DO (RS6T)				
58		GS3		P, NZ						
	FS1 &2	ctr+	in 6	i	1					
60	GS4	ctr+	BTSPU#1		1					

CALCULATE SELECTORS

		·				
		• ctr-	• ctr+	• GS3RI	•	•
1	(A)	• ctr+	• ctr -	• MQRI	• (3), SF#1	•
	\cup	• CS4-4N	• CS3-3N	• CS13-3T	• 21	•
		• Reset	• Sup	• MQRO	• in 6	• FS1&2RI
2	$(\mathbf{E}_{\mathbf{x}})$	•	•	• GS3RO	•	• MQRI
		• 50C ₃	• 20	• 10A ₁	• 11A ₃	• 11A ₂
		RS6-4C, CS13-5T CS16-5T, CS18-5T	• in 2	• ctr+	emit 5	•
3	$(\mathbf{E}_{\mathbf{x}})$	•	• CS10-2C	• CS1-2C	• GS3RO	• in 4
		• PSF#9	• CS8-4N	• CS6-3N	• CS6-2N	• CS8-1N
		• MQRI	• R&R	• in 4	• ctr -	• in 3
4	(E_x)	• ctr -	• GS3RO	• in 2	• CS1-1C	• CS10-1C
		• CS7-5N	• 6A ₁	• CS7-4N	• CS6-1N	• CS15-2N
		• MQRI	• MQRO	• Sup	•	• GS1&2RO
5	NR	• GS4RI	• R&R	•	•	• MQRO
	(8)	• 33A ₂	• 36A ₁	• 6	•	• 12A ₁
		• ctr-, BTSS	• RO	• GS3RI	• GS4RI	• Prog Source
6	(8)	• CS4-4C	• CS3-4C	• CS3-3C	• CS13-3C	•
		• CS7-3N	• CS8-2N	• CS8-3N	• 9A ₂	• RS1-3N 55-60B
		• R&R	•	• MQRI	• in 5	• ×
7	$\overline{(V)}$	• RO	out 4	• CS6-1C	• CS4-3C	• CS4-1C
	\cup	• 4A ₁	• 4A ₃	• CS17-1N	• 5A ₃	• 6A ₂
	* *	•	• GS4RO	• ctr+	• in 6	• out 5
8	$\overline{(}$	• CS3-5C	• CS6-2C	• CS6-3C	• CS3-2C	• CS10-3C
	\circ	• 6A ₃	• 7A ₁	• CS17-2N	• 7A ₃	• 9A ₃
		•	• Prog Source	• FS3&4RO	• GS4RI	•
9	$\overline{(r)}$	•	•	• FS1&2RO	• ctr+	•
	\odot	•	• 52-60A PSF#3, PSF#4	• 11A ₁	• 11A ₂	•
ш		1				

CALCULATE SELECTORS

		Prog Rpt RptDelPU	• BTSS	• RS#5PU	• MQRO	● 1/2 add
10	10 (+)	•	•	•	• GS4RO	• MQRI
		• CS4-5N	• CS3-2N	• CS8-5N	• 17B ₁	• 17B ₂
		• ctr+	• in 3	• ctr +	• in 5	• in 5
11	(+)	• MQRI	•	• ×	•	• in 3
		• 28C ₂	• 28C ₃	• 36C ₂	• 36C ₃	• 37C ₃
		• M	• emit 8	• ctr-, BTSS	•	•
12	(+)	•	• GS1&2RO	• ctr+	• in 3	
		• CS16-3N	• 18B ₁	• 18B ₂	• 18B ₃	
		• MQRO	• GS3RI	• CS1-3C	● Sup	RS6-4C, CS3-1T CS16-5T, CS18-5T
13	(+)	• emit 1	• ctr+	• GS3RI	•	
	T	• 8A ₁	• CS16-1N	• CS6-4N	• SF#1	• RS5-2N
	···	• BTSPU#1	• RO	•	•	• Sup
14	T	● in 2	• R&R	• out 2	•	•
		• 10B ₃	• 12B ₁ , 15B ₁	• 12B ₃	•	• (18), SF#5
		• GS4RO	• in 6	• Sup	•	•
15	\bigcirc s	• MQRO	• CS4-5C	•	•	•
		• 3A ₁	• 3A ₃	• ②, SF#1 SF#2	•	•
*.		• ctr -	•	• p	• Sup	RS6-4C, CS3-1T CS13-5T, CS18-5T
16	$\overline{\div}$	• CS13-2C	• Sup	• CS12-1C	•	•
)	• 8A ₂	• 1	• SF#2	• 8	• PSF#1 PSF#2
		• ctr -	• ctr+	• MQRI	•×	• out 6
17	\times	• CS7-3C	• CS8-3C	• GS4RI	• FS1&2RI	•
	_	• 5A ₂	• 7A ₂	• 12B ₂	• 14B ₂	• 16B ₃
		• Sup	•	•	• Prog Source	• RS6-4C, CS3-1T CS13-5T, CS16-5T
18	(x)	• M	•	•	• RS6-3C	•
18		• 10	•	•	• PSF#10	RSF#8 RS5-3N

REPEAT SELECTORS

		• M	• p	•	• Prog Source	•
1	8	•	•	• 55-60B CS6-5C	•	• Prog Source
	\cup	• RS2-1N	• RS2-2N	• RS2-3N	• RS2-4N	• RS2-5N
		• P	• M	•	• Prog Source	•
2	(8)	• RS1-1C	• RS1-2C	• RS1-3C	• RS1-4C	• RS1-5C
-		• SF#8	• SF#10	• RS10-5N	RS3-4N RS10-4N	• RS3-5N
		• GS3RO	•	•	• Prog Source	•
3	(8)	• emit 1	• in 6	• Reset	• RS2-4C RS10-4N	• RS2-5C
		• 49B ₁	• 49B ₃	• 50B ₃	● [52-54B]	• RS5-5N
		• Prog Source	• ctr+	• in 6	• ctr+	• in 2
4	(8)	•	• ctr-, BTSS	•	• GS1&2RI	• in 4
		●1-9, 28-45B	• 56B ₂	• 56B ₃	• 51B ₂	• 51B ₃
		• ,	•	• Prog Source	• Prog Source	•
5	(+)	• Sup	• CS13-5C	• CS18-5C PSF#8	•	• RS3-5C
		• 13	• PSF#7	●28-39C	• RS6-3N 1-27C	• RS6-5N
		• RptDelDO	• Sup	• Prog Source	•	•
6	+) (×)	• RptDelPU	• P	• RS5-4C	• Prog Source	• RS5-5C
	<u>+</u>) (E _x)	• 57C ₂	• 14	• CS18-4N	• CS3-1T, CS13-5T CS16-5T, CS18-5T	• RS7-5N
		• RptDelDO	• Sup	•	•	•
7	$\overline{(r)}$	• RptDelPU	•	•	•	• RS6-5C
		• 41A ₃	• 5	•	•	• RS8-5N
		• FS1&2RO	• ctr+	• Sup	•	•
8	$\overline{(}$	• FS3&4RO	• FS3&4RI	•	• Sup	• RS7-5C
		• 54A ₁	• 59A ₂	• 7	• 9	● 1-9A
		• Prog Source	•	•	•	•
9	$\overline{(}$	• ,	• Prog Rpt	• M	•	•
		• 16-36A RSF#1, PSF#6	• 53A ₃	• 19	•	•
		• Sup	• (GS4)	• FS1&2RO	•	• Prog Source
10	(8)	•	• P	• emit 1	RS2-4C RS3-4N	• RS2-3C
		• (12), PSF#6 PSF#7, PSF#8	• 24	● 56B ₁	PSF#5 PSF#6	●[46-51B]
L		I DI II I, FUETO	_	±	- D1 # V	

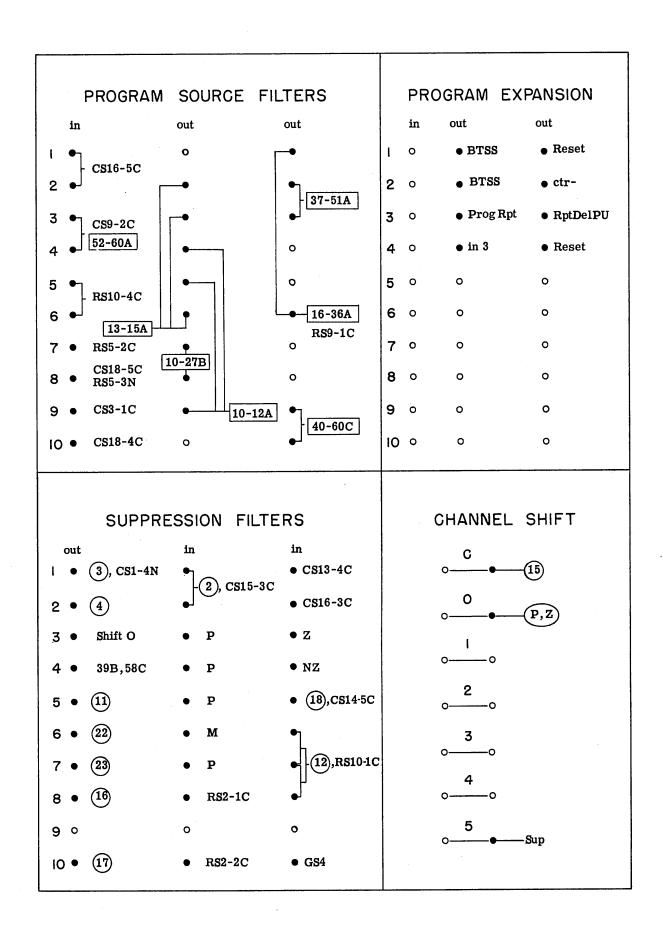


TABLE OF OPERATION WITH ASSOCIATED PROGRAM ACTIVATION, CALCULATE SELECTORS AND REPEAT SELECTORS

	L					
Oper.	Abbr.	Calculate Selectors Transferred	1st Sweep	2nd Sweep	3 or more Sweeps	Last Sweeps
blank	T	13,14	1-9A, 10-27B	none		
				RS5T	RS6T	RS6T
1	(+)	10,11,12,13	1-9A, 10-27B	1-27C, 28-39C, 40-60C	40-60C	40-60C
2	NR	5	none			
				RS6T	RS6T	RS6T
3	\otimes	17,18	1-9A, 10-27B, 28-39C, 40-60C	40-60C	40-60C	40-60C
				RS6T	RS6T	RS6T
4	①	16	1-9A, 13-15A, 16-36A, 37-51A	40-60C	40-60C	40-60C
				RS7T	RS7T	RS8 & 9T
5	\bigcirc	7,8,9	1-9A, 10-12A, 13-15A, 37-51A, 52-60A	10-12A, 13-15A, 37-51A, 52-60A	10-12A, 13-15A, 37-51A, 52-60A	10-12A, 13-15A, 16-36A, 37-51A, 52-60A
6	S	15	1-9A	none		
8	8	5,6	1-9A, 46-51B, 55-60B	RS1T, RS2 or 3 T 10-12A, 13-15A, 16-36A, 52-54B, 55-60B	RS1T, RS2 or 3 T 10-12A, 13-15A, 16-36A, 52-54B, 55-60B	RS4T 1-9B, 28-45B, 46-51B, 52-54B, 65-68B 13 or more Repeats
9	E,	2,3,4	1-9A, 10-12A, 40-60C	RS6T 40-60C	none	
х	A	1	1-9A, 10-27B	none		

SUPPRESSION TYPES

p	Suppress on plus balance	(1)	Suppress except (+)
M		$\stackrel{\bullet}{\otimes}$	
	Suppress on minus balance	(2)	Suppress(S)
\mathbf{Z}	Suppress on zero	3	Suppress(S),(+),(T)
NZ	Suppress on non-zero	4)	$P(\div); M(+); Suppress(S)$
GS1	Group Suppress #1	(5)	Suppress RS7T
GS2	Group Suppress #2	6	Suppress (8), (NR)
GS3	Group Suppress #3	7	Suppress RS8T
GS4	Group Suppress #4	8	Suppress (+)
	_	9	Suppress except RS8T
Sup	Suppress without test	$\widecheck{0}$	M; Suppress 🛇
		11	P; Suppress T
		12	Suppress RS10D
		13	Suppress except RS5T
		14)	P; Suppress RS6T
		15	P, Z, Suppress on operation code 7 [Channel Shift]
		1 6	P RSIT ; M RS2T ; Suppress RS 10T
		17	M RS1T); P RS2T); GS4
		18	Suppress T
		19	M RS8N
		20	Suppress (Ex)
		21	Suppress (S), (+), (T); Do not Suppress (A)
		<u>©©999999999999</u>	M, Suppress RS10T
		23	P, Suppress RS10T
		24)	P; GS4 RS10T

AN ITERATIVE METHOD FOR SOLUTION OF REGRESSION WEIGHTS AND SIMILAR PROBLEMS

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I Introduction

The Personnel Research Laboratory concerns itself principally with psychological studies in the scientific placement of airmen in career fields commensurate with their abilities as determined by an aptitude test battery. A frequent project requested of our division, the Machine Processing Branch of Research Services, is for a regression (or beta) weight solution of a matrix of test intercorrelations and a vector of validity (or criterion) coefficients. Stated in more general terms, the problem is to solve a set of n linear, non-homogeneous equations in n unknowns, where the nth order matrix of coefficients is symmetric, has I's down its diagonal, and has all its non-diagonal elements between 1 and -1. We had been attacking the problem by the straight reduction method but were dissatisfied in that this was highly time consuming. It furthermore involved the associating of matrix rows and columns which meant interspersed master card gang punching on the sorter and reproducer. This resulted in still more time delay and placed a maximum of responsibility on the operator's shoulders, providing for a most insecure atmosphere. The results were, moreover, of questionable accuracy. Given only three digits in the original matrix, the numerous multiplications and divisions necessary in the direct solution often produced an accumulated round-off error sufficient to virtually destroy the significance of the result. We could, of course, have circumvented this latter difficulty by assuming five or six digit elements in the correlation matrix; but the necessary additions would have admittedly been too cumbersome for the same control panel and would have demanded a new and still slower control panel.

^{*}The opinions or conclusions contained in this report are those of the authors. They are not to be construed as reflecting the views or indorsement of the Department of the Air Force.

It was apparent that some self-correcting constantly converging iterative technique would be highly desirable. At first we tried the Gauss-Seidel method* which indeed offered the expected improvements, to some degree, but was still disappointing with regard to speed of convergence. The main difficulty of the Gauss-Seidel method seems to be the arbitrariness with which it corrects. It proceeds routinely from equation 1 to equation n, back to equation 1, and so on, without regard to which weight is in greatest error. It was just this consideration that led us to the "educated correction" iterative method with which this paper is concerned.

This method has already had several months of extremely successful operation at our installation. It was used for the first time on the 20th order regression weight problem presented in Section VII. We had previously obtained a three place solution by the Gauss-Seidel method in about 350 iterations at about a minute an iteration. The new "educated correction" procedure gave similar accuracy within 98 iterations, at the same machine time per iteration, representing a time saving of well over 70%. Both methods took zeros as the original approximations to the beta weights. We could, incidentally, have settled for two places available at about the fiftieth iteration. As we later substantiated on other matrices, this meant that a well-behaved system of twenty linear simultaneous equations could now be solved on the 602-A in less than an hour of machine time, by this technique.

Although its speed of convergence relative to other procedures such as the Gauss-Seidel make it most attractive, it should not be supposed that the "educated correction" method has no other advantages for use on the 602-A. It has indeed many further selling features which will occur to the reader during the following development. It also has far wider applicability than has been suggested. Symmetry and the other properties of a correlation matrix are convenient, but certainly not essential for the success of this method. We have been able to extend its use to some matrix inversion, and to many common problems arising in statistical and factor analysis. It is our hope that its possibilities may be recognized in many other fields of study. That is our primary purpose in writing this paper.

^{*}An article on the use of the CPC for the Gauss-Seidel method can be found in the September 1950 issue of IBM's <u>Industrial Computation Seminar Proceedings</u>. The Kelley-Salisbury method, expounded in the <u>Journal of the American Statistical Association</u>, 21:282-292 (1926), more closely resembles the method of this paper in that it, too, suggests correcting on the variable in greatest error. It, however, calculates the optimal correction at each stage, a procedure too involved to be fruitfully incorporated on the 602-A.

II Table of Notation

```
\mathbf{r}_{ij} = \mathbf{r}_{ji} \dots \mathbf{j}^{th} correlation coefficient of \mathbf{i}^{th} equation = \mathbf{i}^{th} cor. coef. of \mathbf{j}^{th} equation
B_1 \dots i^{th} beta weight
                                               prc.....proper r column number for a given run
V<sub>i</sub>.....i<sup>th</sup> validity coef.
                                               prd.....proper r deck number for a given run
e<sub>i</sub>.....i<sup>th</sup> error term
                                               Fk.....first k card of a given run
x_i \cdot \cdot \cdot \cdot \cdot i^{th} approximated B
                                               Lk.....last k card of a given run
k.....correction term
                                               E_i card .... the (1+23i)^{th} e card, i = 1, 2, 3, ...
(iii)k .....iii<sup>th</sup> correction term
                                               PEi.....program exit i
(iii)....order in which k came
                                               Po....read cycle
(XDI) pu .... (X dig or imm) pick up
                                               Pi.....program step i
do.....drop out
                                               X_i \dots X in card col i
Si .... selector i
                                               D<sub>i</sub>......digit in col i
Csi.....coselector i
                                               X_{k}.....sign of Fk
CB.....control brushes
                                               X_r \cdot \cdot \cdot \cdot \cdot sign of r
RB.....reading brushes
                                               X_e \dots sign of e
col(s).....card column(s)
                                               (X if - or no X if +, over low order position)
MC..... multiplicand
                                               /i/....counter i
MP.....multiplier
                                              i, j, \dots counters i and j
MPL .... multiply
                                               (i) ..... storage unit i
____ ....into
Si ..... thru the transferred side of Si into
        .... thru the normal side of Si into
```

III Statement of the Method

Consider the solution of the n simultaneous equations

$$r_{i1}B_1 + r_{i2}B_2 + ... + r_{in}B_n = V_i$$
 (i = 1, ...n)
for $B_1...B_n$,

where $r_{ij} = r_{ji}$, $r_{ii} = 1$ and $|r_{ij}| < 1$ for $i \neq j$. Suppose a set of values, $x_1, \dots x_n$ is substituted in these n equations for the unknowns. Unless $x_1, \dots x_n$ is identical with $B_1, \dots B_n$,

$$\mathbf{r}_{i1}\mathbf{x}_1 + \mathbf{r}_{i2}\mathbf{x}_2 + \dots + \mathbf{r}_{in}\mathbf{x}_n = \mathbf{a}_i \text{ will not } = \mathbf{V}_i$$
for all $i = 1$ to n .

Let $V_i - a_i = e_i$ and let e_m be the e_i of greatest absolute value. The iterative method of this paper derives a new variable x'_m for the m^{th} equation:

$$x_m' = x_m + e_m$$

The method always corrects on the variable corresponding to the largest numerical error $|e_m|$. This process is found to bring the $x_1, \ldots x_n$ as close to the $B_1, \ldots B_n$ as is desired, merely by correcting a sufficient number of times. By substituting x_m' for x_m in the equations, a new set of errors (e_i') are obtained by the formula:

$$e_i' = e_i - r_{im}e_m$$

since $e'_i = V_i - a'_i = V_i - (a_i + r_{im}e_m) = (V_i - a_i) - r_{im}e_m = e_i - r_{im}e_m$. If subscripts are dropped for the general case, and if e_m is relabeled k, the formula then becomes:

$$e' = e - kr$$

This is the fundamental equation of the method and is the only important operation taking place. The remainder of the programming merely performs operations such as selecting and punching the largest e value ($e_m = k$) after every run, and identifying the equation from which it comes (i.e. the m) by indicating the card column (prc) in which the highest order digit of each r_{im} is punched.

It is convenient to take $x_i = 0$ (i = 1, ..., n) as the first guess to $B_1, ..., B_n$. Then the first $e_i = V_i$, and $e_m = k$ is just the largest numerical V_i , i.e. V_m . Notice that $e_m' = e_m - k = e_m - e_m$ always = 0, which is therefore a check on whether the board is performing correctly. The approximation to any B_i can be determined at any stage of the procedure merely by adding all the k's of the i^{th} equation which have been computed to that point. The operator can stop any time these approximations to the B_i 's are within his desired accuracy.

^{*}See the Supplement to Section VI for the mechanics of this zero check

IV Setup of the Decks

Card	Cols	Prepunched On	Machine Punched On	Information
k	1	all k cards		X ₁
	1	first Fk card	all following k cards	prd
	2-3	first Fk card	all following k cards	prc
	4	first Fk card	all following k cards	X_4
	5-8	first Fk card	all following k cards	k
	50-52	all k cards		k order number
	78-80	all k cards		study number
е	3	all e cards		X_3
	3-4	all e cards		equation (row) number
	9-12	all e cards of first e deck		$first e_i = V_i$
	13-76		e cards	e', 4 cols at a time
	77	all e cards		e deck number
	78	E _i cards		X ₇₈
	78-80	all e cards		study number
	 1	all r cards		r deck number
	2	all r cards		$\mathbf{X_2}$
	3-4	all r cards		equation (row) number
	9-77	all r cards		r's of a given row 3 digits each
	78-80	all r cards		study number

Note: 4 digit e's and k's, and 3 digit r's are assumed. The number of digits can, of course, be increased by appropriate changes on the panel and cards.

The study and row numbers, and the identifying X's, are to be punched on the cards as indicated in the table above. The other information shall now be further elaborated upon.

k card

The stack of cards which goes through the machine on any run contains two k cards: one k at the front of the deck (Fk), and the following k at the back of the deck (Lk). On the first run Fk has $e_m = V_m$ punched in cols 5-8, prd in col 1, prc in cols 2-3, and X_4 . The prd for the first k card is the number of the r deck which contains r_{im} . The prc is the first card column in which the r_{im} values are punched. This is the only k card on

which the operator must key punch cols 1-8. The machine punches them on all succeeding k cards. The consecutive numbering of cols 50-52 (the order numbers from 000 up) on all k cards is most conveniently done with a consecutive number deck on the reproducer. At the end of the run the machine will punch on the Lk card: k in cols 5-8, prd in col 1 and prc in cols 2-3. The operator will then know which r cols and which r deck to read from on the next iteration, and will be able to adjust his wires accordingly. The same holds true, of course, for successive runs.

e card

The first round of e's are just the V's, so that the first deck of e cards must be key punched with appropriate V's in cols 9-12. Only 16 additional sets of e's (calculated during the determination of (001)k to (016)k by the machine) can be punched on the first e deck, and similarly for successive e decks. The last set of e's punched in cols 73-76 of a given deck, must be reproduced into cols 9-12 of the new e deck. The deck number is punched in col. 77. Rather than make use of the reproducer, the programmer may wish to arrange his 602-A panel so that cols 9-12 of the new e deck can be punched on blank e cards merged with the old e cards of the operating stack at the proper time. X_{78} must be punched on the E_1 cards to indicate to the machine the arrival of a new r deck, as described in Section VI. It is important to be sure that X_{78} is reproduced on the E_1 cards of a newly punched deck.

r card

If $n \le 23$, the r card holds a row of the matrix punched in cols 9-77, three cols per r. If, however, n > 23 more than one card must be used for each row of the matrix. This entails punching more than one r deck. Twenty-three r's should be punched on the first deck, twenty-three on the second, and so on, until all the r's have been punched. In a 25th order problem, therefore, each row would be punched on two r cards: the first holding twenty-three r's, and the second holding the last two r's. The deck number goes in col 1. Each r deck should be punched twice, once by matrix rows and once by columns. This permits comparison of the two sets on the reproducer as a check. An error indicates either a mistake in punching or lack of symmetry in the matrix; the latter would necessitate checking the source.

Original correlation cards, with a three digit r punched on each card, are often available. In this case the r decks can be much more conveniently punched by running these source cards through a 602-A whose control board is wired to combine up to 23 r's together on a single r card. Whether the r cards are key punched or machine punched, it is generally advisable to have .999 rather than 1.000 for the diagonal r's. This standardizes the use of three digits for all r's. It only slightly alters the values of the first few correction terms and in no way appreciably affects the final result.

V Running the Problem

The final stack of cards, ready to be run through the machine, is in the following order face up:

- 1. The first Fk card (000)k is on top.
- 2. The r cards from the first equation (row) are next. If there are say three r decks, the r card from the first row and first r deck is the second card in the stack, followed by the r card from the first row and second deck, followed by the r card from the first row and third deck.
- 3. The e card of the first row is next.
- 4. Two and three above repeated for all other rows (from 2 to n).
- 5. The Lk card (001)k is last and on bottom.

The machine is first cleared with a blank Fk card. This clear card must have an X_1 but neither an X_2 , X_3 or X_4 . The rightmost skip stop and the following three sets of wires must be moved after every run of the cards through the machine:

- 1. The four e reading wires which read out of the cols containing the last calculated e.
- 2. The three r reading wires which read out of the proper r cols (prc) and the one prd wire which reads r col 1 through the digit selector.
- 3. The four e punching wires which punch the first four cols of the e card immediately following those containing the last calculated e which is being read.

For the first run e shall be read out of cols 9-12, r out of prd and prc, and e shall be punched in cols 13-16. Upon completion of the first run:

- 1. The Fk card (000)k is filed.
- 2. The Lk card becomes the Fk card (001)k. (Alternately, k can be stored in the proper unit (1) after each run. With the appropriate changes in wiring this would effectively eliminate the necessity of Fk cards.)
- 3. (002)k becomes Lk.
- 4. The e reading wires, the e punching wires and the rightmost skip stop move 4 cols to the right.
- 5. The r reading wires move to the new prc.
- 6. The prd wire moves to that digit of the digit selector which equals the new prd.

If the operator has only one control panel to work with, these operations must all be done while the machine is not running. However, if he has two panels at his disposal he can either:

1. Work two (or more) separate problems in which case the only time delay, outside of machine time, is for moving the skip stop. All

- other preparations for the second problem can be accomplished while the first problem is running; or,
- 2. Use both panels on the same problem which allows him to move the e punching and reading wires on the second panel while the first is still running. In any event, however, the k's (in cols 5-8), and the order number (cols 50-52) can always be recorded while the machine is running. This is achieved by writing down this information for a particular k card on the run during which the immediately following k card is Fk.

The k's are conveniently recorded in the following type table. The sum of the k's in the i^{th} column will be the approximation to B_i .

row number	1	2	3	4		23	24	
prd and pre	109	112	115	118		175	209	
	# k	# k	# k	# k		# k	# k	
	# k	# k	# k	# k		# k	# k	
•	•		•	•	•	•	•	•
•	•	•	•	•	•	•		•
•	•	•	•	•	•	•	•	•

#is the k order number, corresponding to the k in the same cell.

For a "well-behaved" matrix this table will have a property which proves extremely useful in the detection of errors. In any given column the k's will uniformly descend toward zero and, after the first entry, will maintain the same sign. That is, every k will be numerically less than all k's above it and will be of the same sign as all k's above it with the possible exception of the topmost k. By a "well-behaved" matrix is meant one whose off diagonal elements are generally small and positive. Matrices other than these, namely those with elements negative and close to 1, will produce many inconsistencies in the above scheme. This checking criterion should not, therefore, be religiously adhered to unless there is no doubt concerning the "well-behaved" nature of the matrix. The array always provides a pattern nevertheless, and one can justifiably become suspicious if too large an increase or sign reversal is noticed.

In addition to the k sheet the operator will have two piles of k cards for each problem:

1. The Lk pile: the blank ones, which are still to become Lk cards,

face up, in ascending order from top to bottom.

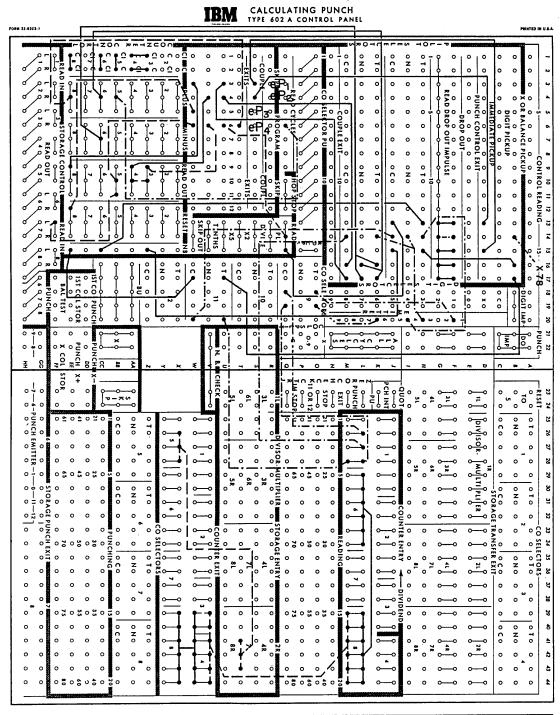
2. The Fk pile: the punched ones, which were former Fk cards, face down, in descending order from top to bottom.

After every run, then, a card moves from the top of the Lk pile to the bottom of the operation stack, the former Lk becomes Fk, and the former Fk goes to the top of the Fk pile, face down.

If, after a particular run, the operator wishes to check back several iterations, he merely plugs the e and r reading wires and the prd wires to the same hubs to which they were plugged at the start of the iteration he is interested in. The e punching wires move over four columns as usual. It should be noticed that the e reading and e punching wires will then be no longer adjacent. If on the next run he wishes to continue his checking operation, he moves the wires to their normal, adjacent positions with the prc and prd wires moving as directed by the new Fk card and the e punching wires again moving four columns to the right. On the other hand, if he at any time prefers to revert back to the run on which he left off, he must again move his e punching and reading wires to non-adjacent positions, in the appropriate manner.

The operator should, of course, always use that order and procedure which best allows him to run his problem most economically and efficiently.

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ELECTRO NO.	CARD NAME OR FUNCTION	X OR D CODE	MOTES: ——wires relating to				
	Process whereby prd, prc, and		conditional programming				
	em are obtained		wires relating to				
			prd-prc accumulation				

VI Description of Programming

Selector, Coselector Table

S	Cs	Picked up at	How	Dropped out at the end of	Information
1	9	Fk CB	x	Fk RB	X₄ identifying Fk card
2		r CB	x	r RB	X ₂ identifying r card
3	11	e CB	x	e RB	X ₃ identifying e card
4		Fk and Lk CB	x	Fk and Lk RB	X_1 identifying Fk and Lk cards
5		prd RB	I	prd RB	prd
6		Fk RB	x	Lk RB	X_k
7		r RB	x	e RB	$X_{\mathbf{r}}$
8		e RB	X	r(or Lk) RB	X_{e}
10	5,6	start of Lk punching	D	Lk punching	punch control exit of S12
12		Fk and Lk RB	X	following RB	$\mathbf{X_1}$ identifying Lk (and Fk) card
13		e P2	I	e P2	e P2
14		E _i CB	x	E _i RB	X_{78} identifying E_i card
15		e P1	I	e P1	e P1
16		end of e P1	x	r(or Lk) RB	sign of e' in $/3$, $4/$ at e P1
17		end of e RB	x	r(or Lk) RB	sign of e_m in /8/ at e RB

Note: The following are used interchangeably:

CB.....control brushes.....control time

RB....reading brushesreading time

Piprogram i.......program i time

Fk Card

CB: X_1 pu S4.

X₄ pu S1.

Po: X_4 to skip out since the Fk card is not to be punched.

|Fk| Cs9 (1) storing |Fk| in the multiplier.

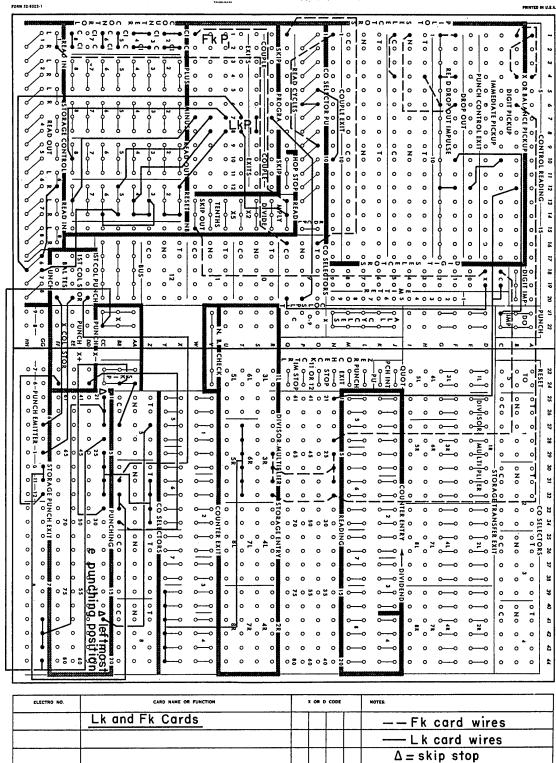
 \boldsymbol{X}_k pu S6 to be $\;$ do $\;$ on Lk card, thus storing the sign of Fk for the entire run.

106 emitted $Cs9_5/5/$. The 1 represents r deck one, whereas the 06 provides for an 09, the initial r col, the first time 3 is emitted into /5/.

(PE1) P1: To read.

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r Card

CB: X₂ pu S2.

Po: X₂ to skip out, skipping out all r decks.

Reset /1, 2/, /3, 4/ and /6/.

$$|r| (MC)_{(2)}$$
.

 X_r pu S7, storing the sign of r.

D₁ goes thru the digit selector_S2_I pu of S5.

 X_2 S5, skip to PE2. Improper r decks therefore go to PE1 which causes the next card to be fed and read, whereas the prd skips to PE2 and goes thru the following program step:

(PE2) P1 (2R) MPL \longrightarrow /1,2/giving |kr|. To read.

e Card

CB: X₃ pu S3.

On the Ei card X78 pu S14.

Po: X_3 to skip to PE 3 where the e programs begin.

 X_e pu S8, storing the sign of e.

$$/1,2/\underline{S3}\underline{S6}\underline{S7}\underline{\mp}$$
 /3,4/ giving - kr.

 $|e|_{--}(3)$.

NB of /8/Cs11pu S17.

3 emitted <u>Cs11</u>/5/. By adding 3 on each e card we maintain the r col, corresponding to that particular e, in /5/. On the E_i card, 34 is emitted <u>S14</u>,/5/, rather than 3. This effectively changes the 175 to 209 (or 275 to 309 etc), and therefore the first e card of the second deck corresponds to a 209 in /5/, (etc). The two lowest order positions of /5/ will thus indicate the prc and the third lowest order the prd, as the selection process of P3 and P4 makes clearer.

(PE3) P1: (3R) $\frac{S8}{S8}$ + $\frac{}{}$ /3,4/ giving e - kr which equals e'.

$$/8/\frac{S17 + }{S17 - }/6/ \text{ giving - } |e_m|.$$

I pu S15.

NB of $/3, 4/\underline{S15}$ pu S16.

(PE4) P2: I pu S13.

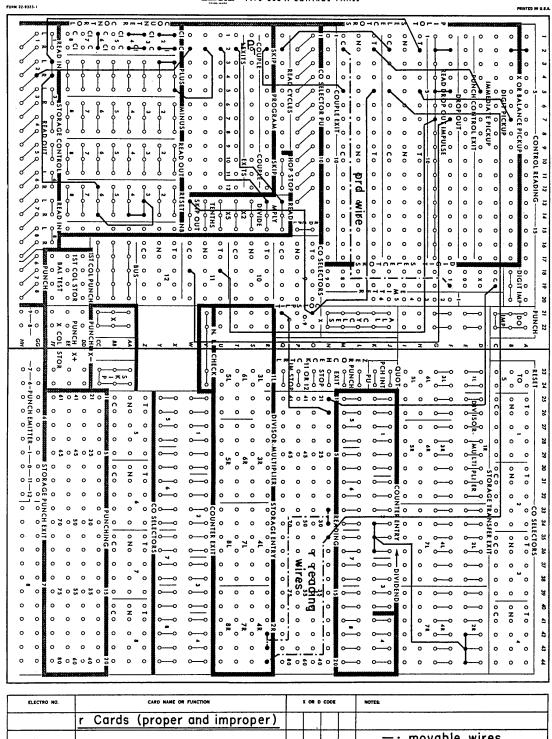
/3,4/___(6) and punch e' in the four columns immediately following those from which e was just read.

/3,4/ $\frac{S16}{S16}$ /6/ giving |e'| - |e_m| which, if positive, means there

is a new em and the next two programs are necessary.

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ELECTRO NO.	CARD NAME OR FUNCTION	X OR D COOE	NOTES:
	r Cards (proper and improper)		
			— · movable wires
			— stationary wires

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ELECTRO NO.	CARD NAME OR FUNCTION	X OR D CODE	NOTES:			
	e Cards		—— movable wires			
			— stationary wires			
			Δ skip stop			

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NB of $\frac{6}{\text{S13}}$ to 'read' which effectively skips the next two programs if and only if $\frac{6}{\text{was}}$ negative on P1.

(PE5) P3: (conditional)

Reset /8/. Thus if there is a new e_m, the old e_m has been cleared out to make way for it.

(PE6) P4: (conditional) $/3, 4/ / 8/ \text{ and the new } e_m \text{ is now in } /8/.$ $/5/ / (7) \text{ clearing (7) and putting in the prc and the prd corresponding to this new } e_m. \text{ The lowest three positions of } /5/ \text{ are read into the second, third and fourth positions of (7).}$ An X_4 may then be punched over the (7) units position, which is independent of the other positions of (7) during punching. It is now evident that when (7) is finally impulsed to punch, the prc and prd will represent the r corresponding to the largest of the e_m 's; i.e. the e_m of the whole run. To read.

An interesting question, which could be asked at this point, is whether it is worth the effort to make these last two program steps conditional. The advantage to taking them on each e card regardless of whether or not a sign inversion had occurred, is that the conditional operations could be selected and several non-conditional operations, such as clearing, could be added. However, the fact that the number of sign reversals to be expected with n equations approximates the natural log of n, implied that a substantial amount of time could be saved by ruling out the latter alternative. This observation is derived from simple probability considerations. In order to have a sign reversal on say the i^{th} of n equations $|e_i'|$ must be greater than all $|e_j'|$ where $j=1,2,\ldots i-1$. The probability (and expectation in this case) that this be so for randomly distributed e's is just 1/i. There is always a sign inversion for e'_1 The probability for this is thus 1 or 1/i where i = 1. When i = 2 the probability is 1/2, and so on. Now making use of the fact that the expectation of the sum equals the sum of the expectations, the expected number of sign inversions is: 1 + 1/2 + 1/3 + ... + 1/n which from a study of the area under the curve y = 1/x is seen to be between $(\ln n)$ and $(1 + \ln n)$. About three sign inversions might therefore be expected when n = 20. This means that about 34 program steps will, on the average, be saved during each run by making the last two e program steps conditional. This empirically amounted to more than a 15% saving of 602-A time with the 20th order matrix solution listed in Section VII.

Lk Card

CB: X_1 pu S4. Po: X_1 pu S12. $X_1 \subset S9^+$ skip to PE7 where the Lk programs begin. (PE7,8) P1: Punch (7). This punches the prd in col 1, the prc in cols 2,3, and both a dummy zero, from the units position of (7), in col 4 and an X₄.
/8/_____(6) and punch in cols 5-8.
Reset /1,2/, /3,4/, /5/, /6/, and /8/.
The punch control exit of S12 pu S10 when Fk punching starts.
To read.

Supplement (e'm zero check)

For the incorporation of the zero check the following additions and modifications in setup are necessary:

- (1) Rather than punch the e row number in cols 3-4 of the e card as directed in Section IV, the corresponding prd-prc number should be punched in cols 1-3. Thus 109 should be punched instead of 01, 209 instead of 24, 212 instead of 25, etc.
- (2) Couple Cs 10 to Cs 9 and Cs 12 to S 13.

The zero check effectively checks on both operator and machine, from run to run, by making use of the fact that the new error term of the equation just corrected is always equal to zero (see Section III). The board is wired to verify on a given run that the e'_m of the previous run is indeed zero. If it is not, as the corresponding e card goes into the stacker the machine will stop and the compare signal will light up. Since generally none of the original e's, namely the V's, are equal to zero, an error signal on the first run is merely by coincidence and should be ignored. Similar considerations hold for out of sequence runs because of the manner in which the zero check was programmed. This could have been avoided by the more straightforward check of the e'_m of the current run, accomplished by reading the prd-prc number of the run from the Fk card directly into (4R) and by reading the e' of the run out of /3, 4/. Although this method has the advantage of notifying the operator of a mistake while the pertinent run is still going through the machine, it does not check the transfers of e' from /3, 4/ to /6/ and to (6), nor does it check the punching of e'. It is therefore not as complete a check as the following:

Fk RB: Fk cols 1-3 Cs 10 (1L) storing the prd-prc of the current run.

r RB: Reset /7/.

e RB: e cols 1-3 $\overline{\text{Cs }10}$ /7/ storing the e identification number.

e P1: (4R)_--/7/ subtracting the prd-prc number of the previous run from the identification number of the e card passing through.

e P2: Rightmost three positions of /7/___ pu of Cs 7-8 and Ipu of S9.

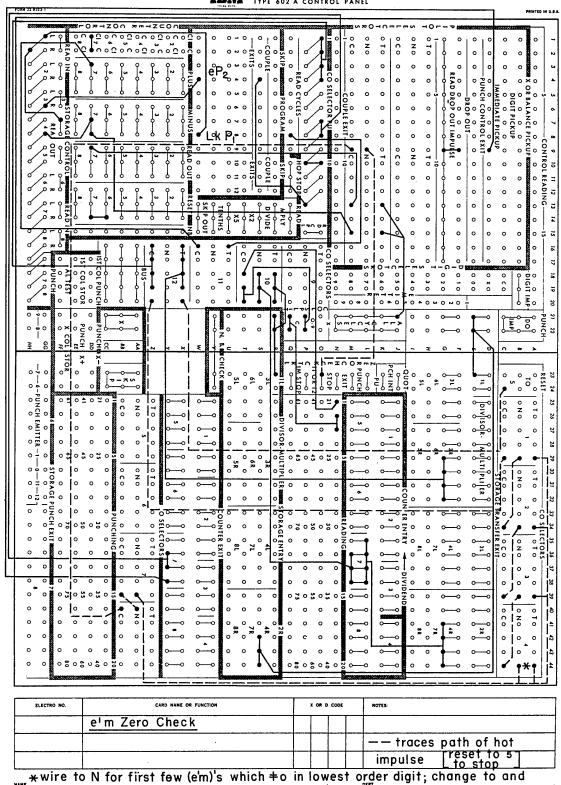
Rightmost four positions of (3R) Cs 12, pu of Cs 1-4.

At x-time of this cycle, x (reset to 5) pulses are taken into a

C hub of each of the Cs 1-4; the corresponding T hubs are spliced

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keep at T after first compare light —— from then on the (em)'s should = o.

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together, with the single pulse Cs7 Cs8 S9 Stop. When the prd-prc number of the previous run and the e identification number are one and the same, the difference developed in eP1 will be zero and neither Cs7, Cs8, or S9 will be picked up. If, at the same time, e is different from zero, at least one of Cs 1-4 will be picked up and a pulse will get through to stop the machine. If either e is zero or the difference is non-zero, the pulse will not get through. Since .999's instead of 1.000's are being used for the diagonal matrix entries, the first few (e'_m) 's will not be zero in their lowest order position. To allow for this, the wire leading out of Cs 4 should come from the N hub. After the first compare light, that is when the (e'_m) 's become identically zero, this wire should be changed to the Thub and be kept there until the solution has been obtained.

Lk RB: Reset /7/.

(1L)___(4R) storing the prd-prc of this run for use on the following run.

VII Solution of a 20th Order Regression Weight Problem

Correlation matrix and validity coefficients:

Validities	-020	220	048	107	161	227	115	198	249	143	039	135	128	128	210	129	126	940	118	060	
20	-190	023	-024	403	555	427	363	286	455	274	284	342	243	375	323	475	189	323	568		
19	-052	023	-057	223	536	413	165	332	538	256	192	396	375	480	354	350	355	233		268	
18	-407	062	075	694	316	591	305	045	161	197	102	348	175	-002	222	281	018		233	323	
17	115	-012	093	019	064	213	-016	526	520	122	800	268	315	250	176	108		018	355	189	
16	-050	002	028	339	358	274	258	352	330	094	338	381	264	291	527		108	281	350	475	
15	017	047	114	262	404	296	538	235	413	110	357	328	470	234		527	176	222	354	323	
14	240	-115	095	083	144	215	087	202	616	-010	158	352	147		234	291	550	-002	480	375	
13	010	026	-085	105	287	287	244	256	283	071	188	197		147	470	264	315	175	375	243	
$\frac{12}{1}$	004	037	254	440	323	316	314	217	315	190	183		197	352	328	381	268	348	396	342	
11	-004	037	-025	116	202	132	321	181	236	109		183	188	158	357	338	800	102	192	284	
10	-143	197	-095	081	208	408	193	083	208		109	190	071	-010	110	094	122	197	256	274	
6	046	063	102	155	304	362	159	204		208	236	315	283	616	413	330	520	161	538	455	
∞ı	104	018	141	045	082	244	072		202	083	181	217	256	565	235	352	526	045	332	286	
7	-073	-004	-032	313	325	802		072	159	193	321	314	244	180	538	258	-016	305	165	363	
91	-240	127	-024	433	338		208	244	362	408	132	316	287	215	296	274	213	591	413	427	
ខា	-222	106	046	341		338	325	082	304	208	202	323	287	144	404	358	990	316	536	555	
41	-466	106	144		341	433	313	045	155	081	116	440	105	083	262	339	019	694	223	403	
ကျ	-049	-033	-	144	046	-024	-032	141	102	-095	-025	254	-085	095	114	028	E60	940	1 90-	-024	
21	-123		-033	106	106	121	-004	018	063	197	280	037	026	-155	047	900	-012	790	620	023	
-1		-123	-049	-466	-222	-240	-073	104	046	-143	-004	004	016	240	017	-050	115	-407	-052	-190	
	-i	2.	က်	4.	5.	6.	7.	œ.	6	10.	11.	12.	13.	14.	15.	16.	17.	18.	19.	20.	

Note on matrix: Decimal points are directly in front of the highest order digit; .999's are the diagonal entries.

Correction Table: (2 place numbers have been used for simplicity)

	20	166	03	15 -0290	27 -0162	40	66 -0028	71	88				-1336	-0019	-136
	19	163	09 (23 1	43 2	56 4	86 (- 0987	- 4000-	660-
	118	160	11 (13 2	19 -0239	29 6	38 -0081	45 -0062	53 -0037	61 -0031	73 -0026	82 -0012	-1268	-0019	-129
	17	157	21	36 -0074	47 -0055	64 2 -0033	84 -0010	N				w 1	-0480	- 2000-	-049
	16	154	33	49 -	58 4	75 -0016	91 8						-0195	-0004	-020
	15	151	0891	51 -0043	68	80 .	5 96 96						6080	-0002	080
	14	148	48 0050	76 0019	85 0014								0083	9000	600
	13	145	41 0082	63 0026	79 0013								0121	9000	013
	12	142	22 0229	44 0055									ation 0284	0000	028
Row Number	11	d prc 139	07 -0520	25 -0193	98						·		Sums after 98th iteration 789 0377 -0708 0284	Guessed corrections 0004 000	1 B's -070
Row N	110	prd ar 133 136	18 0257	37 0078	60 0027	78 0015							after 9 0377	pesser c	Final B's 038 -070
	61		00 2490	05 -0554	31 -0131	77 -0016							Sums 1789	بى -0000	178
	∞1		90	20 0211	24 0179	32 0098	42 0056	57 0030	70 0020	8000			1300	0013	131
	-1	127	10 0468	50 0061	69 0022	81 0013	·						0564	0002	057
	91	124	02	12 0408	30 0139	46 0057	65 0023	87 0009					1746	6000	176
	ای	121	08 0535	14 0281	26 0167	34 0098	52 0036	67 0027	83 0011	93 0007			1162	0012	117
	41	118	16 0298	28 0132	39 0093	54 0048		72 0020	74 0018	8000	95 0006		0657	0018	890
	က၂	115	12 -0008	·									-0008	0000	-001
	21	112	01 2043	17 -0229	35 -0086	62 -0027	9000-						1695	-0007	169
	HI.	109	55 0041	94 0008				. ,					0049	9000	900

VIII Conclusion

There is, of course, no limit to the size of the matrix, since as many r decks as desired, within reason and practicality, can be punched. As a matter of fact, the larger the matrix the more satisfactory the method, for convergence becomes relatively more rapid with the increase in number of equations. We are currently planning to treat matrices up to the 237th order (item analysis) on the same control panel.

The questions of when to stop the iterations and of how to increase accuracy might be of paramount importance in an organization involved in computational work of a precise nature. We shall, therefore, take them up here even though they are not too significant in our work where two or three places are generally adequate. It should be emphasized that once the error terms dwindle in size to a single digit in their lowest order position, further correction becomes meaningless. Unless additional places (i.e. zeros) are added to the e's and the k's, the correction terms will begin to oscillate around zero without the gaining of any further information. Four digit e's and k's will thus give three place betas at best. Five digit e's and k's would require far fewer iterations for three place beta weights; the additional multiplication cycles necessary, however, might very well cancel out the time saved.

Once the k's begin to dip below 9 in their lowest order, a surprisingly good approximation to the remainder for any beta weight can often be guessed, by observing how the k's for the corresponding B have been behaving. If a variable has been corrected comparatively little, the approximation to the B is probably quite good and the remainder is most likely negligible; e.g., variables 3 and 12 in Section VII. On the other hand, if the variables has been frequently corrected, the remainder is most likely relatively large; e.g., variables 4 and 18. After the iteration process has been terminated, this "guessed" correction can be added at the bottom of each k column to give a final approximation to the B's.

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