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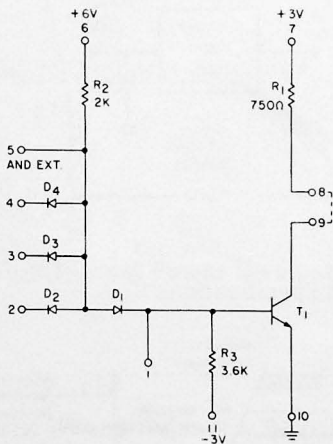
### Functional Description

The AND Inverter, AI-2A module consists of three diode positive AND circuits followed by a saturating transistor inverter.

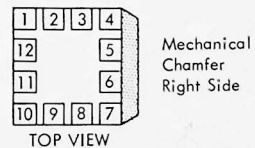
Pins 2, 3 and 4 are the AND inputs, connecting Pin 5 to common anode diodes (FDD module) to extend the AND Fan In.

The OR function can be accomplished by dotting collectors (parallel connected collectors) with other modules - only one collector resistor is required.

### Schematic

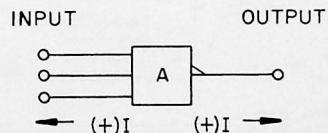


### Terminal Configuration



Pins 1 and 12 Leave Open

### Block Diagram



## Maximum Ratings

Input Voltage = 13V

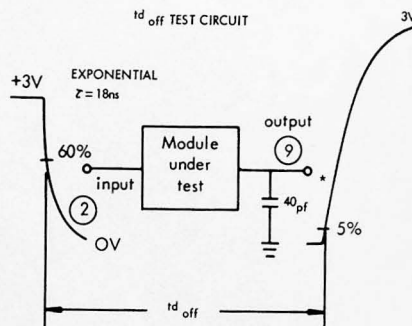
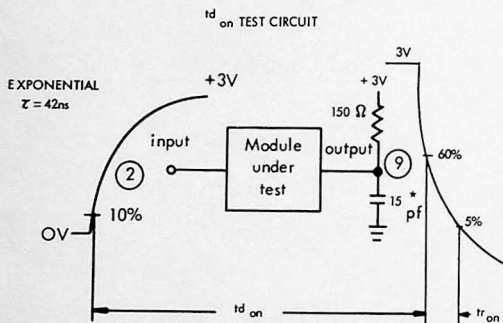
Output Voltage = 8V

$I_E = 24$  Milliamps

## AI-2A Module Functional Tests

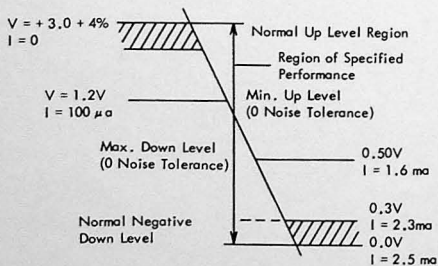
TESTS	TERMINAL CONDITIONS												C	ADDITIONAL LOAD REQUIREMENTS	VARIABLE	LIMITS		UNITS
	1	2	3	4	5	6	7	8	9	10	11	12				MIN	MAX	
DC ON		+1.2V	+1.2V	+1.2V		-5.76V	+3.12V	$V_0$	$V_0$	GND	-3.12V		25 / 75	18.5 ma CURRENT INTO TERM 8	$V_0$		0.30	V
DC ON		+1.2V	+1.2V	+1.2V		-5.76V	+3.12V	$V_0$	$V_0$	GND	-3.12V		25		$V_0$		0.17	V
DC OFF		-0.4V	+6.0V	+6.0V		-6.24V	+2.88V	$V_0$	$V_0$	GND	-2.88V		25		$V_0$	2.84		V
DC OFF		-6.0V	-0.4V	+6.0V		-6.24V	+2.88V	$V_0$	$V_0$	GND	-2.88V		25		$V_0$	2.84		V
DC OFF		+6.0V	+6.0V	-0.4V		-6.24V	+2.88V	$V_0$	$V_0$	GND	-2.88V		25		$V_0$	2.84		V
DC NOISE					+1.07V		+2.88V	$V_0$	$V_0$	GND	-2.88V		75		$V_0$	1.8		V
$t_{d\ on}$	INPUT	+3V	+3V			+6V	+3V	15 pf CAP TO GND	OUTPUT	GND	-3V		25	150 $\Omega$ RESISTOR TIED BETWEEN TERM 7&8	$t_{d\ on}$	8	25	ns
$t_{r\ on}$	INPUT	+3V	+3V			+6V	+3V	15 pf CAP TO GND	OUTPUT	GND	-3V		25	150 $\Omega$ RESISTOR TIED BETWEEN TERM 7&8	$t_{r\ on}$	5	28	ns
$t_{d\ off}$	INPUT	+3V	+3V			+6V	+3V	40 pf CAP TO GND	OUTPUT	GND	-3V		25 / 75		$t_{d\ off}$	11	35 / 42	ns

## Test Waveforms

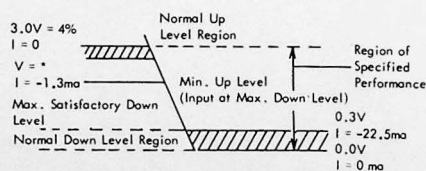


\* Including Probe Capacitance

## Input Requirements



## Output Specifications



\* Voltage as defined by collector load impedance

## Fan In

Can be extended to a total of 15 inputs

## Fan Out

Total collector current for the AOI-2A = 22.5ma

$$22.5\text{ma} \geq I_{R1} + N_1 K_1 + N_2 K_2 + \dots$$

$I_{RC}$  = Total collector load current

$N_1$  = Number of AI-2A loads

$N_2$  = Number of AOI-2A loads

$K_1$  = 2.3ma, AI - 2A loading constant

$K_2$  = 3.0ma, AOI - 2A loading constant

To double the Fan Out, the output collectors and inputs must be paralleled.

## Maximum Power Supply Current Requirements

	<u>ON</u>	<u>OFF</u>
+6V	2.5ma	2.8ma
+3V	4.0ma	0
-3V	1.1ma	1.0ma

## Maximum Power Dissipation

<u>ON</u>	<u>OFF</u>
35mw	20mw

$$\text{Average Normal Power Dissipation} = \frac{\text{NOMINAL ON} + \text{NOMINAL OFF}}{2} = 25\text{mw}$$

## General Wiring Rules (For Printed Circuit Wire - 10Mil Width Lines)

The input single line length should be less than 18 inches to prevent excessive reflections and noise coupling. Maximum length at either input or output should be less than 60 inches unless longer delays specified can be tolerated.