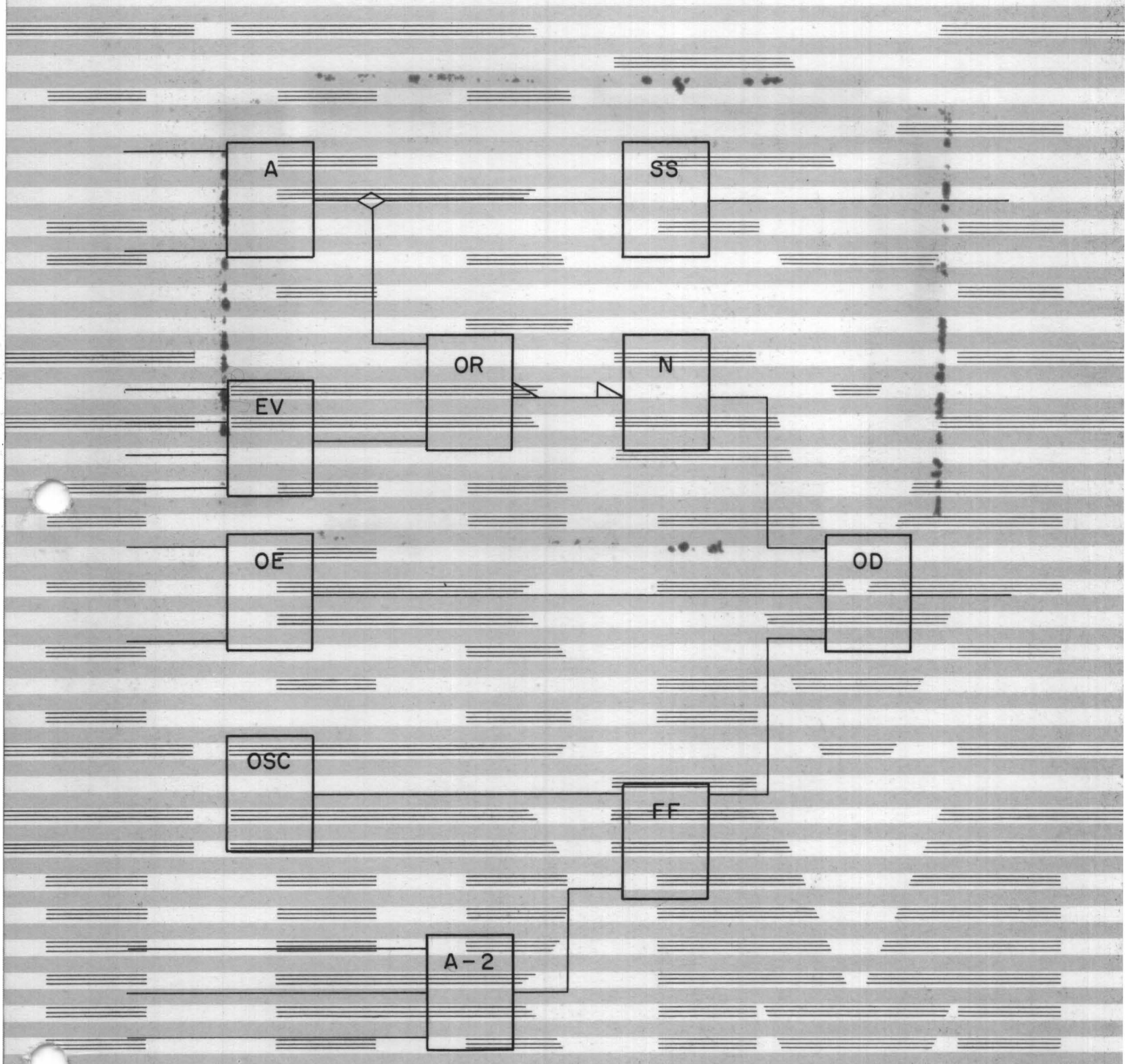
Standards Publication
Logic Documentation Manual

DEB 0-1046-BKT
August 1970



IBM Division Engineering Bulletin

First Edition

Changes or additions to information in this booklet will be incorporated during subsequent revision. Supplements to the booklet will be issued as required prior to revision.

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1.1 INTRODUCTION.

This booklet is for persons associated with the logic circuitry used in IBM products. It is a guide to document logic functions or to interpret logic symbols. The objective is to maintain uniformity in logic notation by adhering to logic symbology standards.

The standards documents in this booklet are grouped into Parts that deal with a given aspect of logic documentation. Each document occupies a Section within the appropriate Part. Two tables are located on the Contents page for subject-to-document or DCS-to-page reference.

The authority, compliance, applicability and deviation requirements of each document must be determined prior to its application. For example, requirements of a "Standard" are more binding than those of a "Practice". Paragraph 1.0, Introduction, of each Section indicates the mandatory or non-mandatory status of the documents comprising the Section. Table 1-1 provides information to assist proper use of document requirements.

New standards documents related to logic documentation may be issued as supplements, then inserted as Sections at the ends of the appropriate Parts during revision of the booklet.

1.2 LOGIC BLOCK SYMBOLS.

Logic block symbols are used to conveniently depict logic functions performed by electronic circuits. The rectangular characteristic of the symbols was chosen for its adaptability to Design Automation (DA) Programs used to generate circuit design information, and Automated Logic Diagrams (ALD). The rectangular blocks contain notation that identifies the logic functions represented by the symbols (i.e., AND, OR, OSC, etc.).

Active inputs to the circuits are shown by horizontal lines that approach block symbols from the left. Active outputs exit from the right of the blocks. Except where they have a direct bearing on the logic function, service voltages and returns are not shown at the logic symbols.

Besides the function identity, block symbols may contain block identifications, circuit type numbers, circuit locations in machines, etc. However, these are related to the physical attributes of the circuits and are beyond the bounds of the logic functions represented by the logic symbols.

1.3 NEW LOGIC BLOCK SYMBOLS.

Adding new symbols to those in existence may be the requirement of a new technology. Because of the impact on the interface between operating units, new symbols must be thoroughly investigated by these units prior to acceptance.

Three alternatives to introduce a new symbol are available:

1) Approval and authorization of a deviation to use a symbol that is not in existing Standards or Practices.

2) A symbol for use on documents released beyond Design Engineering. The Corporate Logic Symbology Committee and/or the IBM Director of Standards function to adopt, modify or reject the proposed symbol. When accepted, the new symbol is placed in a Standard.

3) A symbol for use on documents not released beyond Design Engineering and intended for processing by the EIS DA system only. IES 0-1046-022 describes the requirements for acceptance of such a symbol. When accepted, the new symbol is placed in a Practice.

1.4 DEVIATION FROM ACCEPTED SYMBOLOGY.

When a suitable symbol to represent a circuit function is not in existence and the demand for that symbol is immediate, approval of a deviation from the Standard or Practice that would contain that type of symbol is required. Since existing symbols are the product of an agreement between affected operating units, the proposed deviation requires concurrence by those units and approval by an appropriate authority.

The Deviation Notes column of Table 1-1 indicates the requirements to obtain approval to deviate from the various standards documents.

Also bearing on the decision of a deviation or not are the following:

1) Development projects using SLT/SLD DA and MST DA require formal deviation approval for non-standard symbols.

2) Development projects using EIS DA do not require a formal deviation, provided the requirements of IES 0-1046-022 are complied with.

3) Released logic diagrams must contain only standardized symbols. However, to expedite the standardization process; when a new symbol is required, the Logic Symbology SDP can coordinate the requirements and may issue a Bulletin until full concurrence for adoption of the new symbol has been obtained.

NOTE 1. DEVIATION FROM A STANDARD.

Any deviation from the requirements of a standard requires approval in accordance with established procedures at the location requesting the deviation, and must provide for concurrence of all affected divisions. Contact your local Engineering Standards Department.

NOTE 2. DEVIATION FROM A PRACTICE.

Compliance with a practice is expected, but a practice does not require the formal control and deviation procedure of a standard. Deviation from practices shall be processed in accordance with the procedures at the operating unit.

EXEMPTION NOTES

The variety of products and contractual stipulations nullify deviation procedures in some circumstances. Referring to Table 1-1, the

Exemption Notes column indicates what exemptions are applicable to a specific document.

NOTE A

Products that are designed under special government contracts are exempted from the requirements of this document.

NOTE B

Where requirements conflict with customer contractual specifications, the latter take precedence and shall be exempt from deviation procedure.

NOTE C

Non-system products marketed by the Office Products Division are excluded from the requirements of this document.

NOTE D

Second-order products that do not require logic pages, such as structures, are exempt from the requirements of this document.

NOTE E

This document applies only to unreleased Engineering diagrams produced by EIS DA for product design.

Regardless of the automated documenting system used, the format for and packaging of ALD pages must conform to the applicable requirements given in Parts 5, 6 and 7 of this booklet.

1.5 LOGIC DIAGRAMS.

The majority of logic diagrams are produced by automated documenting systems operating with SLT/SLD, MST, MST/MALD and EIS programs. Logic diagrams released for field distribution are the product of SLT/SLD, MST and MST/MALD processing and are limited to the use of standardized symbology or symbols that have full deviation concurrence and approval.

The EIS documenting program reproduces both standard and non-standard representations and the diagrams are restricted for use by Design Engineering (unreleased documentation). EIS non-standard symbology is controlled by Practices conforming to the requirements of IES 0-1046-022.

Note: Symbology techniques developed and used for product technologies prior to the effective date of a standard listed in Table 1-1 are exempt from its requirements.

TABLE 1-1. IMPLEMENTATION OF ENGINEERING STANDARDS DOCUMENTS

DCS	Authority	Compliance	Approved	Effective	Applicability	Deviation Notes (See Paragraph 1.4)	Exemption Notes (See Paragraph 1.4)
0-1038-001	Division	Bulletin	-	15Aug68	SDD	-	-
0-1046-003	Corporate	Standard	2Feb70	1Feb65	All divisions & subsidiaries	1	A
0-1046-004	Corporate	Standard	-	1Jan65	All divisions & subsidiaries	1	A, B
0-1046-005	Corporate	Standard	22Jan66	15Feb66	All divisions & subsidiaries	1	A, B
0-1046-007	Corporate	Standard	6Sep68	15Sep68	All divisions & subsidiaries	1	A,C,D
0-1046-009	Corporate	Standard	2Sep65	1Sep65	All divisions & subsidiaries	1	A, C
0-1046-010	Corporate	Standard	-	15Sep65	All divisions & subsidiaries	1	A
0-1046-011	Corporate	Standard	27Aug65	1Sep65	All divisions & subsidiaries	1	A,C
0-1046-012	Corporate	Standard	1Nov65	1Sep65	All divisions & subsidiaries	1	A,C
0-1046-017	Corporate	Practice	6Apr67	-Jul67	All divisions & subsidiaries	2	-
0-1046-018	Division	Practice	28Feb69	15Mar69	GSD, SDD	2*	A,C
0-1046-019	Division	Standard	15Sep70	18Sep70	CD, FSD, GSD, SDD, SMD, WTC	1	A,B,C
0-1046-021	Division	Bulletin	1May70	-May70	GSD, SDD	-	-
0-1046-022	Division	Standard	-	-	GSD, SDD SMD, WTC	1	E
0-2820-024	Division	Standard	1Jun65	15Jul65	FED, SDD	1	-
5-7804-000	Division	Standard	-Aug67	-Sep67	FED,SDD,WTC	1**	-

* Concurrence of local FE Technical Operations also required.
** Concurrence of DP/FE Publishing Operations also required.

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1.6 EIS DA SYMBOLS FOR LIMITED USAGE.

Logic symbols used on diagrams which will not be distributed afield may be non-standard provided that they comply with the requirements of IES 0-1046-022 and its supplementing practices.

To insure the interface that satisfies the needs of all users, a task force shall be organized to generate a new practice for a given technology. The task force will be chaired by the prime user and shall provide for representation from:

Engineering Information Systems DA
Field Engineering Division
Logic Symbology Standards Development Project
Component Division Information Systems
Other users

After formulation by the task force, the Logic Symbology SDP will approve the practice. The task force chairman will then contact the local standards organization to arrange for documentation in required format, publication and distribution of the practice.

If the new symbol may be subjected to wide usage, then the Logic Symbology SDP must be contacted to establish possible further action (i.e., coordinate addition of the new symbol to a practice).

1.7 DA PROGRAM RELATED DOCUMENTS.

Logic designers may wish to associate documents in this booklet with available DA programs. The following list provides that information.

Program	Document
SLT/SLD	CES 0-1046-003 and -005
MST	CES 0-1046-003 and -005
MST/MALD	DEP 0-1046-017 (restricted to products with logic diagramming processed through the MALD Program).
EIS	CES 0-1046-003, -009, -017, and DES 0-1046-022 (see MALD).
MALD*	DES 0-1046-022, DEP 0-1046-023 and future DEP not otherwise specified. DES 0-1046-022 permits use of non-standard symbols for unreleased EIS ALD's.

* Formerly FEALD

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1.0 INTRODUCTION

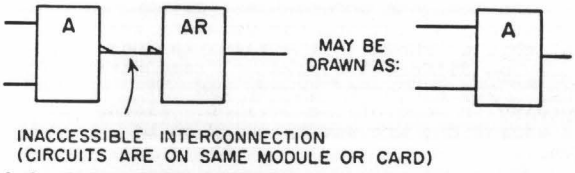
This section defines and establishes basic block symbols and associated notation used to represent digital circuitry on logic diagrams.

Included are rules to select and generate symbols, establish input and output polarities, and to group elementary functions. Use of the rules and other logic notation given in this section will provide diagrams that are easily read and understood without an intimate knowledge of the circuitry performing the functions indicated by the symbols.

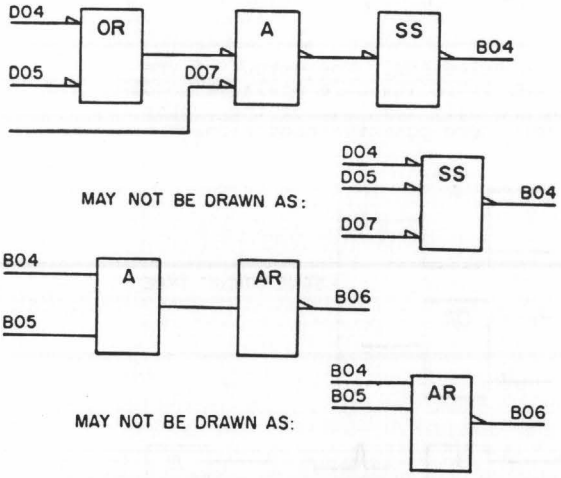
Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 BASIC RULES PERTAINING TO BLOCK SYMBOLS

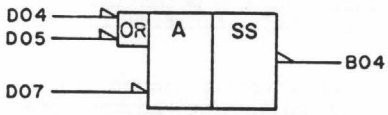
2.1 COMBINATION OF SYMBOLS. The combination into one symbol of any of the basic functions contained in this standard is prohibited, unless the combination results in a logic function defined in this standard, in which case the logic symbol of the latter shall apply. The A (AND) and AR (AMPLIFILR) symbols may, as packaging allows, be combined into the one A (AND) symbol.



2.2 BLOCK LINE POSITION OR GROUPING shall not be used to denote any of the basic logic functions shown in this standard. (See Paragraph 4.1.) Neither shall block line position be used to denote any parameter of the signal such as polarity, pulse length, shift, amplitude, timing, etc. It will be noted that the use of line position to identify a particular lead, such as on a FLIP FLOP, is not a violation of this paragraph.



2.2.1 Butting of Logic Symbols. Butting is recommended for use where present SLDA program restrictions do not apply. (Also see CEP 0-1046-017, SLDA Macro Logic Block Symbols (Part 2, Section B). As packaging allows, logic functions may be butted where no external wiring point exists between logic blocks. There is a single logic connection without logic inversion when the line common to two symbols is perpendicular to the direction of information flow. For example, OR to AND to SS shown above may be drawn as:



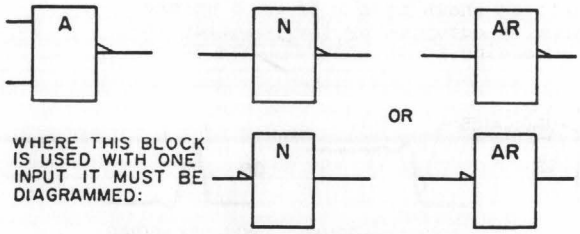
A maximum of three logic block levels can be butted.

Note: The DA capability will be available to EIS users in the future. Check with DA liaison in your area before application.

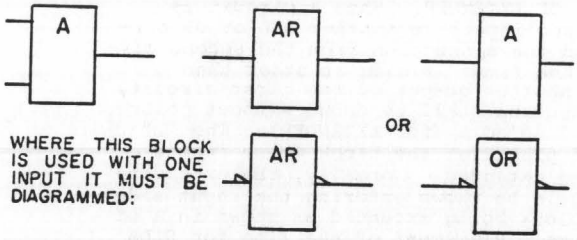
2.3 INPUTS.

2.3.1 Entry To Symbol. No input shall enter a symbol in the vicinity of an output or on the output side of a symbol, except as provided in Paragraph 3.3.

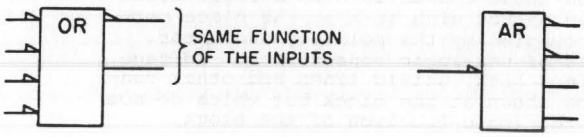
2.3.2 AND or OR Block. An AND or OR block must have at least two inputs unless it is being used as one of the blocks in an EXTENDER arrangement. (See Paragraph 3.3.)



2.3.2.1 Exception. An exception shall be allowed in the ALD's for those cases where only one input of a multiple input device is used to gain entrance to the adjacent circuit within a standard unit, i.e., one diode of the AND device is used to gain entrance to the OR device with an AND, OR, INVERT configuration.



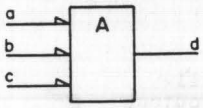
2.4 MULTIPLE OUTPUTS are allowed from logic blocks, provided that each of these meets the definition requirements.



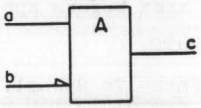
3.0 LINE SYMBOLS

3.1 LINE POTENTIAL. A small open right triangle placed on the input line where it joins the block symbol indicates that a less positive potential is required to satisfy the definition of the logic function identified by the block symbol. A triangle on the output line where it leaves a logic block symbol indicates that a less positive potential condition exists when the logic function is satisfied.

Omission of the triangle from an input line to a block symbol indicates that the more positive potential is required to satisfy the definition of the logic function. Absence of the triangle from an output line indicates that a more positive potential results when the logic function is satisfied.

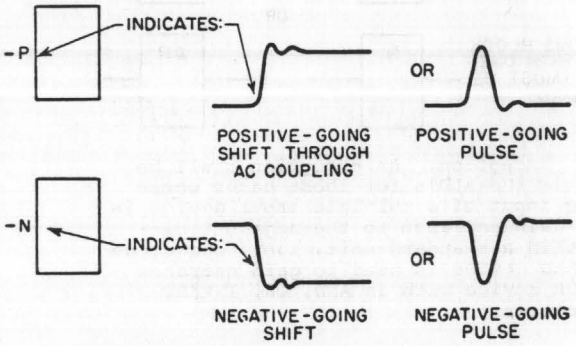


(a) AND (b) AND (c) MUST ALL BE IN THEIR LESS POSITIVE CONDITION FOR (d) TO BE IN ITS MORE POSITIVE CONDITION.



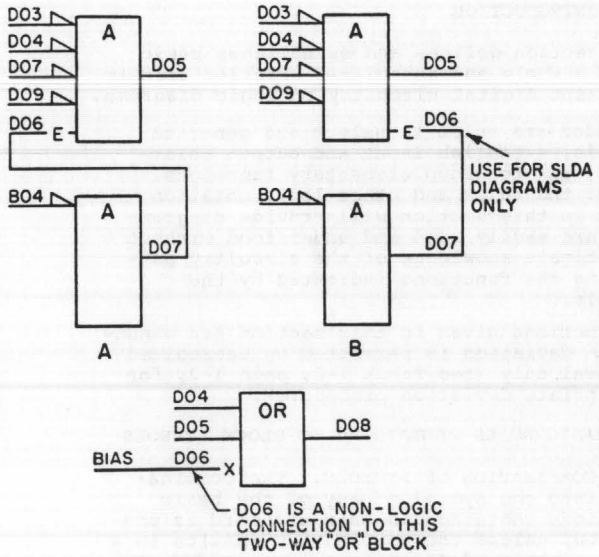
(a) MUST BE IN ITS MORE POSITIVE CONDITION AND (b) IN ITS LESS POSITIVE CONDITION FOR (c) TO BE IN ITS MORE POSITIVE CONDITION.

3.2 AC COUPLING at an input of a logic block shall be shown by a P or an N at the place normally occupied by the polarity indicator according to the conventions shown below.



3.3 USE OF EXTENDER. When a circuit is used to add inputs to another AND or OR circuit, and the connection from the second circuit to the first is made at other than a normal input or output of the first circuit, the connection shall be shown without polarity and labeled E (for EXTENDER). The "E" shall be placed at the block whose inputs are being extended. Normally, the extending line should be shown entering the input side of the block being extended as shown in A of the figure. Placement of the line for SLDA diagrams only is shown in B of the figure.

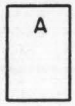
3.4 NON-LOGIC CONNECTIONS to a logic block shall be marked with an X at the place normally occupied by the polarity indicator. Examples of non-logic connections: voltage, bias, feed back, shield lines and other connections shown at the block but which do not affect the logic function of the block.



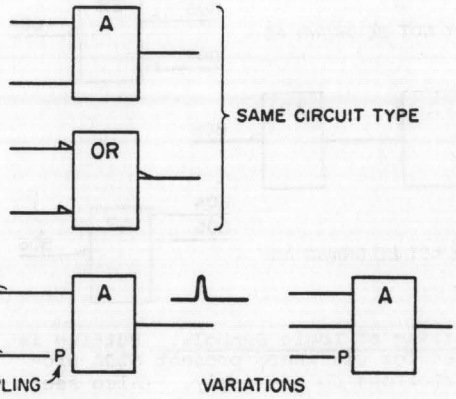
4.0 DEFINITIONS

4.1 A COMPLETE LISTING OF BASIC BLOCKS AND FUNCTION SYMBOL DEFINITIONS. Where a device may have more than one acceptable function symbol (possibly affecting line polarity indication) this is shown in the illustrations by identifying different blocks as "same circuit type." The number of inputs and outputs may vary in some of the devices. Blocks shown as variations are not intended to be inclusive.

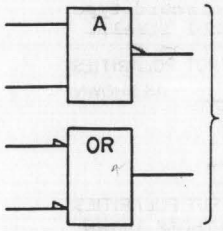
4.1.1 AND. This is a device whose output will stand at its indicated polarity when and only when all of the inputs stand at their indicated polarities. Paragraphs 4.1.1.1 and 4.1.1.2 are the more common types.

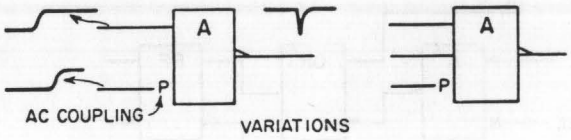


4.1.1.1 Positive AND. The output of the Positive AND is in its more positive condition when and only when all of the inputs are in their more positive condition.

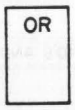


4.1.1.2 Positive AND INVERT. The output of the Positive AND INVERT is in its more negative condition when and only when all of the inputs are in their more positive condition.

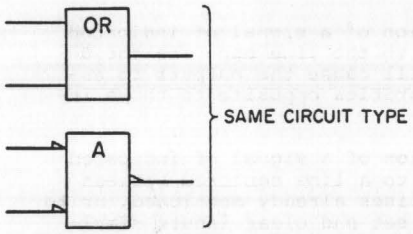




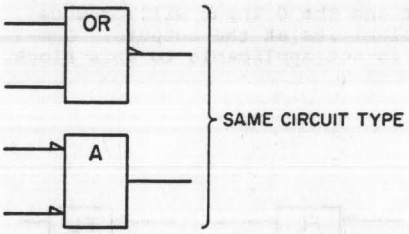
4.1.2 OR. This is a device whose output will stand at its indicated polarity when and only when one or more of its inputs stands at its indicated polarity. Paragraphs 4.1.2.1 and 4.1.2.2 are common types.



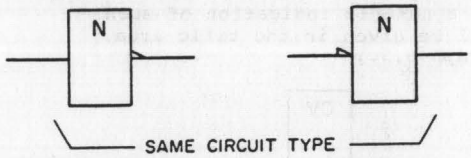
4.1.2.1 Positive OR. The output of the Positive OR is in its more positive condition when and only when one or more of the inputs are in their more positive condition.



4.1.2.2 Positive OR INVERT. The output of the positive OR INVERT is in its more negative condition when and only when one or more of the inputs are in their more positive condition.

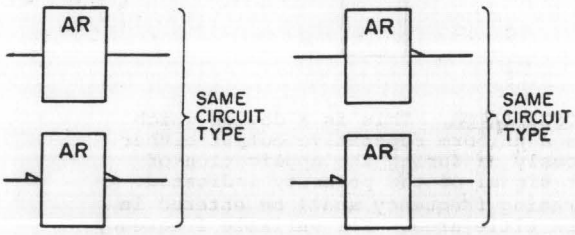


4.1.3 INVERTER. This is a device whose output is in the more positive condition as a result of its input being in the more negative condition and vice-versa. It shall be drawn in one of two ways only: with negative polarity indicated at the input and positive at the output, or vice-versa. An inverter can have no more than one logic input (a return lead or shield connection is not considered a "logic" input.)

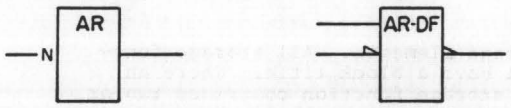


4.1.4 AMPLIFIER. This is a device whose fundamental purpose is to provide adequate driving energy and appropriate impedance matching to other devices. Its output will be at its indicated polarity when and only when its input is at its indicated polarity.

An AMPLIFIER can have no more than one logic input. (More than one physical input may be necessary, for example a return lead or the other lead of a differential input.)

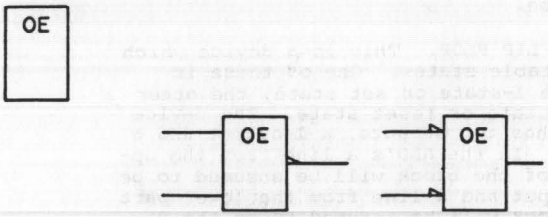


4.1.4.1 Non-Standard Logic Signal Voltage. An AMPLIFIER having input or output of other than standard logic signal voltage shall be made recognizable through labeling at the block.

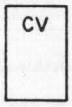


(SEE PARAGRAPH 4.3 REGARDING SUFFIXES)

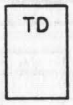
4.1.5 EXCLUSIVE OR. The output of an EXCLUSIVE OR will be at its indicated polarity when one and only one of its inputs is at its indicated polarity.



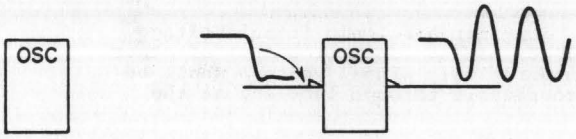
4.1.6 SIGNAL MODE CONVERTER. This is a device that provides the necessary conversion or translation between signal lines having different signal reference values - current mode to voltage mode, voltage mode to voltage mode, etc. Where these reference values are, in fact, current or voltage levels then a numeric indication of such values shall be given in the title area. (See Paragraph 6.3.)



4.1.7 TIME DELAY. This is a device whose primary function is the time delay of a signal without intentional distortion of the signal. The TIME DELAY symbol must always be accompanied by its time delay, which is shown in the 14 character block title. (See paragraphs 6 and 8.3.)



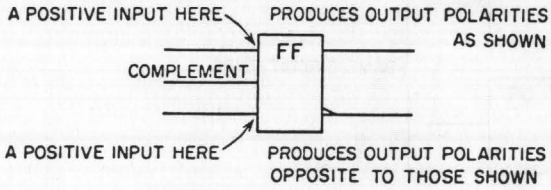
4.1.8 OSCILLATOR. This is a device which produces a uniform repetitive output either continuously or during the application of an input signal of the polarity indicated. The operating frequency shall be entered in the block title area. For variable frequency oscillators, see paragraph 8.3.

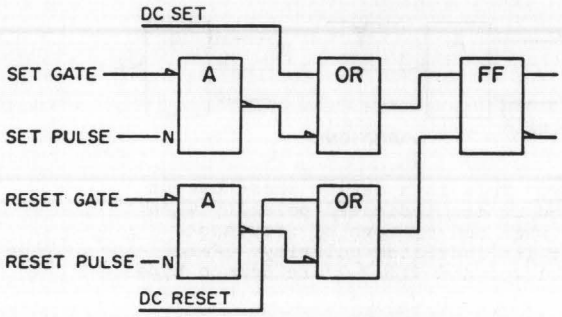


4.1.9 Storage Elements. All storage functions shall have a block title. Where an individual storage function comprises two or more blocks in a cross-coupled arrangement, the block title shall be placed above one of the blocks. The title polarity shall be that shown at the output of the titled block. (See paragraph 7.)

Note: Product design groups using EIS DA or subsequent DA systems should consider paragraphs 4.1.9.1, 4.1.9.2 and 4.1.9.3 superseded by paragraph 2.2 of IES 0-1046-019 upon its publication.

4.1.9.1 FLIP FLOP. This is a device which has two stable states. One of these is called the 1-state or set state, the other is the 0-state or reset state. The device normally has two outputs, a 1 output and a 0 output. In the ALD's a line from the upper part of the block will be assumed to be the 1 output and a line from the lower part of the block will be assumed to be the 0 output. The FLIP FLOP is in the 1 state when its 1 output (the upper output on the ALD) is at its indicated polarity. Regardless of the condition of its inputs, the 1 output and 0 output of a FLIP FLOP in its stable state are always opposite in polarity. The polarities shown at the inputs and outputs of a FLIP FLOP of a particular circuit type are unchanging parts of the symbol itself.





FLIP FLOP WITH INPUT AND'S AND OR'S

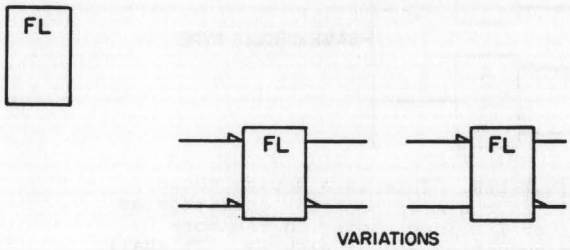
Operation.

(a) Application of a signal of indicated polarity to the line opposite the 1 output will cause the outputs of the block to assume their indicated polarities.

(b) Application of a signal of indicated polarity to the line opposite the 0 output will cause the outputs to assume polarities opposite to those indicated.

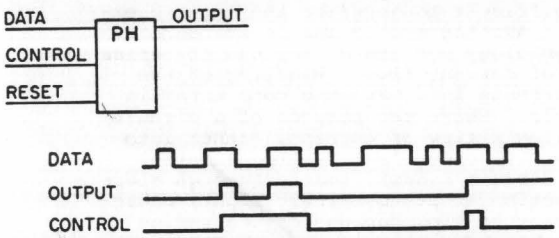
(c) Application of a signal of indicated polarity to a line centered between the two lines already mentioned, or to both the set and clear inputs simultaneously, will change the state of the FLIP FLOP (complement the FLIP FLOP).

4.1.9.2 FLIP FLOP LATCH or FLIP LATCH. The definition of this device is the same as that given for FLIP FLOP except that simultaneous application of signals of indicated polarity at the 1 input and the 0 input will produce unspecified polarities at the outputs. Complement input is not applicable to this block.

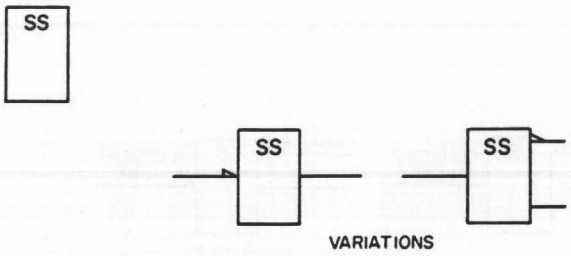


VARIATIONS

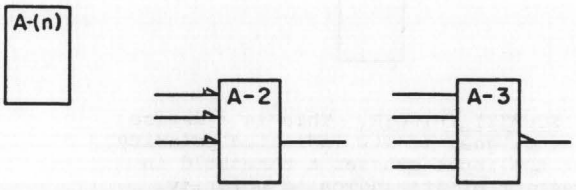
4.1.9.3 POLARITY HOLD. This is a device whose output will be at its indicated polarity whenever the data line and the control line are at their indicated polarity. The output polarity changes whenever data line polarity changes provided the control line is at its indicated polarity. When the control input is caused to go to opposite polarity to that indicated, the output will hold to whatever polarity it possesses at that moment. The PH symbol need not have a RESET input. If it is supplied with one, then the polarity indications on the symbol will be so arranged that the output polarity shown will be opposite that which will exist upon application of the indicated polarity at the RESET input. The data line shall be placed towards the top of the block. The control line shall be centered on the input side of the block. The reset line shall be placed towards the bottom of the block.



4.1.10 SINGLE SHOT. This is a device whose output will change temporarily to the indicated polarity upon the application of an input signal of the indicated polarity. The output will remain in this quasi-stable state for a time which is characteristic of the particular device. The SINGLE SHOT symbol must always indicate in its title area the time duration of the quasi-stable state. (See Section 6.) If a SINGLE SHOT has more than one output and these are not all of the same duration, there must be appropriate labeling at the block or in a referenced note on the page which will relate pin numbers with time durations (see paragraph 8.3).



4.1.11 THRESHOLD. This is a device whose output will be at its indicated polarity when and only when the number of its inputs which stand at their indicated polarity reaches or exceeds the number specified in the function symbol. This symbol shall also be used where an input may have greater weight than 1 in the determination of the threshold. In such case this input shall be suitably titled with a number which denotes the particular weighting factor. The number specified in the A-(n) symbol may not be 1 nor may it be equal to the total weighted value of the inputs.



4.1.12 ODD COUNT. This is a device whose output will be at its indicated polarity when and only when an odd number (1-3-5-7, etc.) of its inputs are at their indicated polarity. An ODD may be shown as an EVEN through proper change in polarity indication.

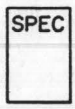
4.1.13 EVEN COUNT. This is a device whose output will be at its indicated polarity when and only when an even number (0-2-4-6, etc.) of its inputs are at their indicated polarity. An EVEN may be shown as an ODD through proper change in polarity indication.

4.1.14 SPECIAL. Under certain circumstances a block should be given the SPECIAL designation. These circumstances, both of which must exist, are:

(a) The function is not covered by any single block symbol given in this standard (as further affected by appropriate use of the standard line symbols).

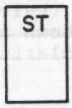
(b) The function cannot be expressed in terms of an interconnected set of individual block symbols as given in this standard (as further affected by appropriate use of the standard line symbols).

A SPECIAL block shall have its function adequately described by wording on the diagram page, either at the block or in a comment area referenced by a note in the titling area of the block.

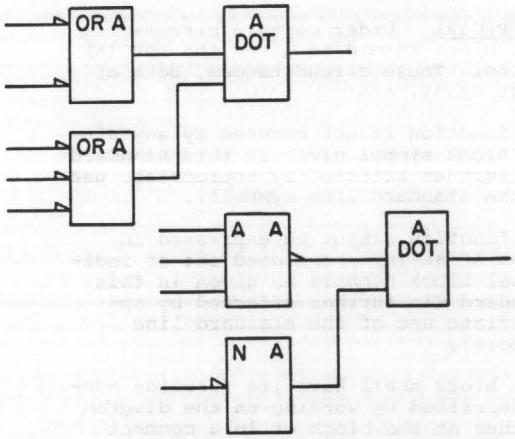


4.1.15 LIMITER. This is a device that limits one or both extremes of a waveform to a predetermined level without intentional distortion of the remaining waveform. It is desirable to state the voltage limitation in the block title (see paragraph 6).

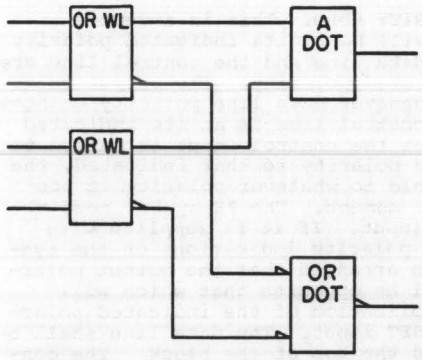
4.1.16 SCHMITT TRIGGER. This is a device whose output goes to its indicated polarity whenever the input crosses a threshold in the direction of its indicated polarity. The output remains at its indicated polarity until such time that the input signal crosses a threshold in the direction opposite to its indicated polarity. The nominal threshold level should be indicated in the block title.



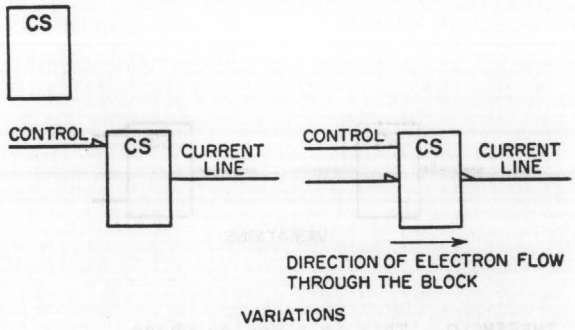
4.1.17 DOT OR and DOT AND. Basic function whose outputs are connected externally so that the connection performs an AND or OR operation (dot AND, dot OR) shall be identified by having an additional A or OR placed in the block to the right of the primary block function symbol. Suffix must match the logic function shown at the DOT block. In the ALD's a block labeled OR DOT or AND DOT will be used to form the junction of lines being joined in this manner. All input and output polarity indications at the DOT block must be identical and the function of the DOT A or DOT OR must agree with the AND and OR definitions as described in Paragraph 4.1.1 and Paragraph 4.1.2 respectively.



4.1.17.1 Wired Logic. When the output of a block enters into both a DOT OR and a DOT AND operation the letters WL (for WIRED LOGIC) shall be placed to the right of the primary block function symbol.



4.1.18 SERIES CURRENT SWITCH. Under some packaging or other physical circumstances it may be difficult to describe the logic operations of AND'ing and OR'ing in standard block symbology because of the use of series control of current flow. Handling of the drive currents in a magnetic core array is an example. Where the purpose of a circuit is to allow a flow of current, either into or out of it, under logic voltage control and the circuit cannot, solely through electrical action at its own logic input, cause the current to flow because of the series flow of this same current through other controlling circuits, the circuit may be assigned the function label CS (SERIES CURRENT SWITCH). The control input of the CS shall be placed toward the top of the block. Application of a signal of indicated polarity to this input will enable (not necessarily cause) the flow of current through the block in the direction indicated by the polarity symbol at the output side of the block on the current line. A negative polarity symbol, for example, will indicate electron flow away from the output side of the block. A line shown opposite the output line will be assumed to be the same current line, separated by the circuitry of the CS. The polarity indication for this line shall be made the same as that of the corresponding output line.



4.1.18.1 Example of Use. The illustration (Figure 2-1) shows the use of the SERIES CURRENT SWITCH (CS) to control a series flow of current through more than one circuit.

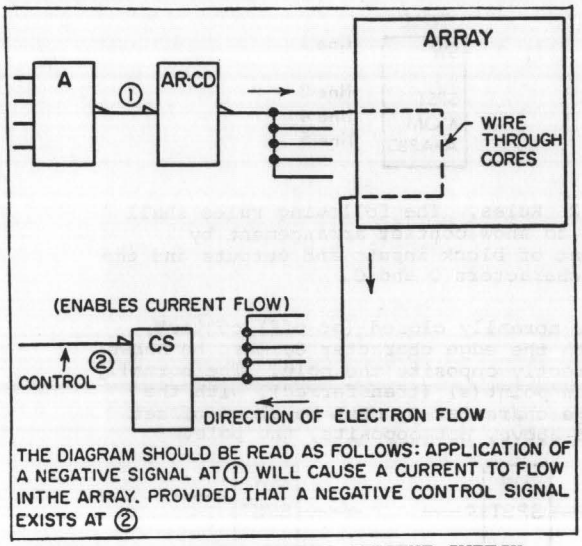
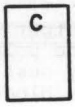


FIGURE 2-1. USE OF SERIES CURRENT SWITCH

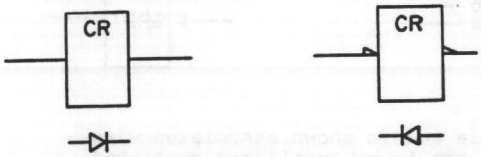
4.2 COMPONENT AND AUXILIARY BLOCKS. This set of block symbols is not a complete nor closed list. When the requirement arises for the representation of an additional circuit component and the amount of usage makes the SPEC symbol impractical, request an addition to the standard.

4.2.1 Array.

4.2.2 Capacitor or Network of Capacitors.



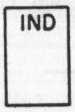
4.2.3 Diode.



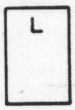
4.2.4 Fuse.

4.2.5 Impedance Network (contains at least two of the three types of components; resistance, inductance, capacitance).

4.2.6 Indicator.

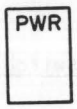


4.2.7 Inductor, or Network of Inductors.



4.2.8 Jumper.

4.2.9 Power Supply.



4.2.10 Relay.

4.2.10.1 Relay Coil and Contacts. These representations pertain to relays. One set of contact points per block is preferred.

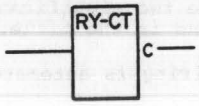
4.2.10.1.1 Hold Coil.

4.2.10.1.2 Pick Coil.

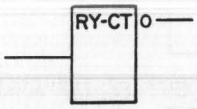
4.2.10.1.3 Pick 1 Coil.

4.2.10.1.4 Single Coil.

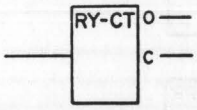
4.2.10.1.5 Normally Closed Point. The output line must be horizontally opposite of the input line, with the edge character C added.



4.2.10.1.6 Normally Open Point. The output line must be horizontally above the input line, with the edge character O added.



4.2.10.1.7 Transfer Point.



4.2.11 Resistor or Network of Resistors.

4.2.12 Thermal Element or Switch.

4.2.13 Transformer.

4.2.14 Switch. The following descriptions apply to manually or electrically operated switches.

4.2.14.1 Logic Block Identification Data.

Line 1 - Symbol identification (SW).

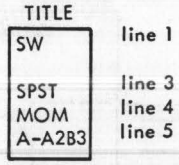
*Line 3 - Switching Characteristics. Typical are SPST for single-pole single-throw, DPDT for double-pole double-throw, and 3PDT for three-pole double-throw.

*Line 4 - Other Characteristics. Typical are MOM for momentary, SHORT for shorting, TOG for toggle, PB for push-button, and ROT for rotary.

Line 5 - Location Code. If the complete code does not fit on this line, the code for the gate, panel, etc., shall be noted in the comment section.

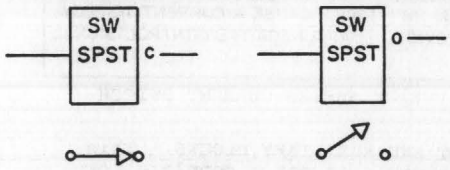
Title Area - Title each switch to describe its function. The name should normally be the same as the panel designation. Switches without on-off significance shall include the two significant conditions in the title.

*Not applicable when wiring is automated.

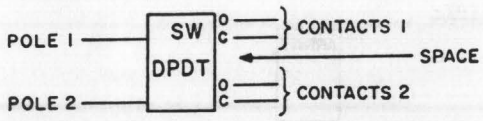


4.2.14.2 Rules. The following rules shall be used to show contact arrangement by placement of block inputs and outputs and the use of characters O and C.

(a) The noramlly closed (or off) contact, with the edge character C, must be shown directly opposite the pole. The normally open point(s) (transferred), with the edge character O, must be shown offset and above, not opposite, the pole.

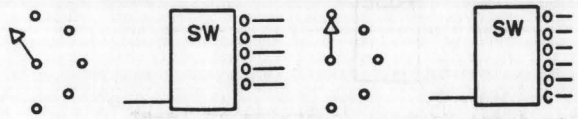


(b) Space shall be provided between the pole and its set of associated contacts and the other set(s) shown on the same block.

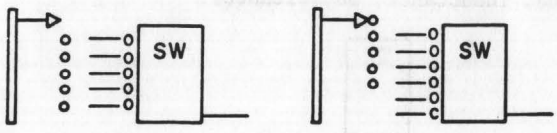


(c) The pole (operating point) may be shown as an input or output of a logic block. If more than one pole is shown on a single block, they must be shown on the same side of the block.

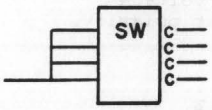
(d) Multiple Points shown associated with a pole are to be considered contacted by the pole one at a time.



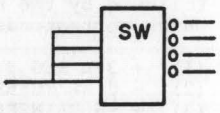
or



(e) When a pole is to make electrical connection with more than one other point at a time, the pole is to be shown as contacting each of the other points.



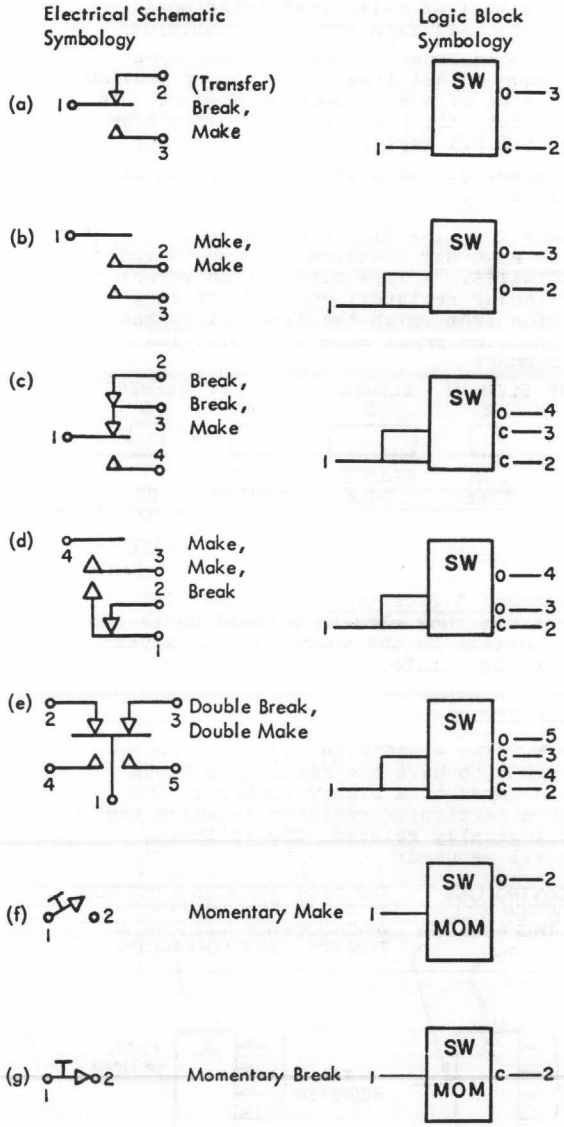
SP to four contacts normally closed

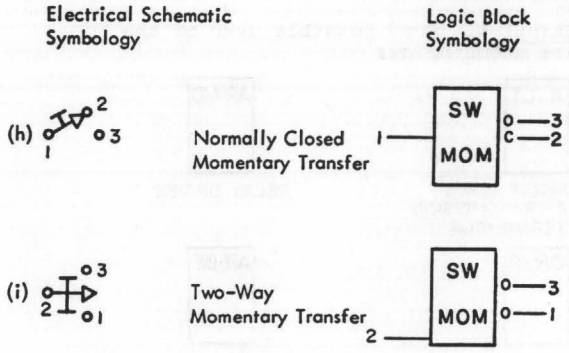


SP to four contacts normally open

(f) The position shown on the block is the non-operated position.

4.2.14.2.1 Examples. The examples shown are the more common types of switches.



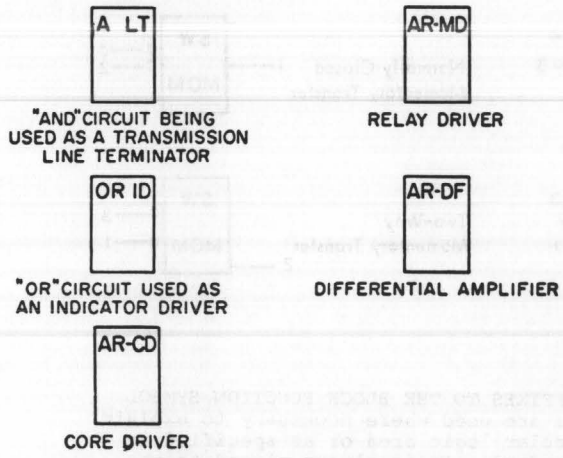


4.3 SUFFIXES TO THE BLOCK FUNCTION SYMBOL. Suffixes are used where necessary to explain a particular logic area or as specified in this standard. It is always placed to the right of the block function symbol; separated by either a space or a dash and can never stand alone. A blank character space is used when only normal input and output logic voltage on signal lines is involved. A dash is used when other than normal logic voltage input or output on signal lines appears on pins which may be accessible. Usage shall be confined to those suffixes listed in Paragraph 4.3.1.

4.3.1 Suffixes.

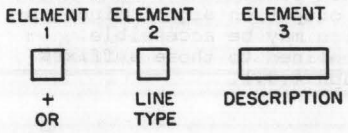
(a)	LT	transmission line terminator	
(b)	LD	transmission line driver	
(c)	ID	indicator driver	
(d)	CD	core driver	
(e)	HD	magnetic head driver	
(f)	MD	magnet driver - relay, clutch, solenoid, etc.	
(g)	V	voltage amplifier	
(h)	DF	differential amplifier	
(i)	FF	flip flop	used for emphasis of storage elements whose elements must exist in multiple block form.
(j)	FL	flip flop latch	
(k)	PH	polarity hold	
(l)	OR	or	used in the identification of blocks whose outputs are connected in the DOT AND or DOT OR arrangement. These suffixes take precedence over all others. Where a suffix which denotes DOT AND or DOT OR supplants a suffix which would normally be separated from the primary function symbol by a dash (see above) the displaced suffix shall be placed above the block in the title area.
(m)	A	and	
(n)	WL	wired logic	
(o)	P	pick	used with the relay block (RY) to denote coil and contact.
(p)	H	hold	
(q)	CT	contact	
(r)	LR	line receiver	

4.3.2 Examples. Some possible uses of the suffix are shown below:



5.0 LINE TITLES

5.1 GENERAL FORMAT FOR ALL LINES ENTERING OR LEAVING A DIAGRAM PAGE. All lines which enter or leave a diagram page shall conform to the following general format:



5.1.1 Element 1. The + or - symbol in element 1 refers solely to the relative level of the signal line with respect to its title. For example, the + symbol indicates that for the title condition, the line will stand at the more positive of its two possible states. The + or - symbol should generally match the output polarity indication shown on the source block.

5.1.1.1 Element 1 Exceptions. An exception will be allowed for those machines in which active (1-state) polarity is predominantly of one type which will be obvious from the line polarity symbols. In these cases element 1 shall be required on all lines which do not conform to the predominate polarity.

5.1.2 Element 2 refers to the physical characteristics of the signal line which control its logic state. Where this is in terms of voltage numeric values shall be indicated.

5.1.2.1 Element 2 Exceptions. Where the line type within a machine is predominately the same or a line has no accessible test point, element 2 may be omitted. Its uses will then denote the exceptional condition. When the unit of measurement of element 2 denotes voltage, the abbreviation for voltage may be omitted. However, the unit of measurement for any other parameter must be shown. See paragraph 5.1.2.3.

5.1.2.2 Indication of Line Type in Line Titles. Where a design group chooses to follow paragraph 5.1.2 without exception, (paragraph 5.1.2.1) the following line title format is recommended:

(a) For lines whose voltage swing is that of the predominate type within the machine:
Show element 1 (+ or - symbol) followed by the nominal voltage which corresponds to that polarity.

Examples: (1) + 3 L REG BIT 6
(2) - 0 WRITE ERROR
(3) + -6 TRANSFER A TO B
(4) - -12 CLEAR B REG

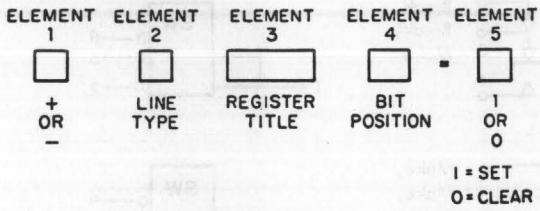
(b) For lines whose voltage swing does not conform to the predominate type:
Show element 1 (+ or - symbol) followed first by the nominal voltage which corresponds to that polarity, then by the voltage which corresponds to the other polarity. The latter voltage must be bracketed by "X's."

Examples: (1) + -4 X-14X TEST INTERLOCKS
(2) -14 X-4X SET HOLD CONDITION

5.1.2.3 Second Order Products. Line type must be shown on all lines entering or leaving the logic area of a second-order product. In other respects, the provisions of paragraphs 5.1.2 and 5.1.2.1 apply.

5.1.3 Element 3. This is a description of the signal line.

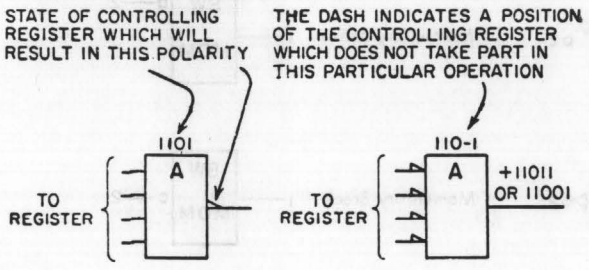
5.2 FORMAT FOR LINE TITLES FOR A REGISTER, COUNTER OR RING BIT POSITION FROM WHICH THE LINE ORIGINATES. A line title which refers to a particular register, counter, or ring bit position from which the line originates or is controlled shall have the following general format:



5.2.1 Element 5 Exceptions. A line title which does not show element 5 shall be assumed to pertain to the source as it exists in the 1 or set state.

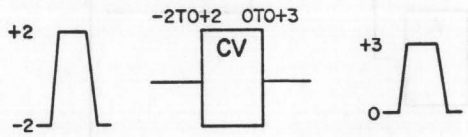
6.0 BLOCK TITLES

6.1 BLOCK TITLE = REGISTER STATUS. Where it is desired to have the title of a block pertain in terms of a binary number to the status of a particular register to which the block is logically related, the following format shall be used:



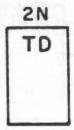
6.2 SPACE. If the block operation cannot be adequately described in the 14 character block title, use "NOTE" in the block title area and comment in the note section.

6.3 SIGNAL MODE CONVERTER. Input and output signal mode parameters shall be defined as in Paragraph 4.1.6.

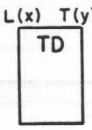


-2TO+2 indicates an input variation from -2 to +2 units or vice versa. Similarly, 0TO+3 describes the variation of the output.

6.4 TIME DELAYS. The time duration is indicated in the 14 character title, followed by N, U, M, or S to denote nano, micro, milli seconds or seconds respectively. Leading blanks are permitted.

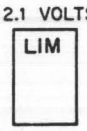


6.4.1 Unequal Leading and Trailing Delay. TIME DELAYS having a different delay time for the leading edge of the output than for the trailing edge shall be identified by the placement of a "L" for leading and a "T" for trailing immediately prior to the separate delay times in the block title area. The input polarity shown at the block must be that which is associated with the "leading" edge of the output.



6.5 SINGLE SHOT. The time duration of the quasi-stable state is followed by N, U, M, or S to denote nano, micro, milli seconds, or seconds respectively. Leading blanks are permitted.

6.6 LIMITER.



7.0 BLOCK ARRANGEMENT OF SIMPLE LOGIC FORMS

7.1 FUNCTIONS PRESENTED AS MULTIPLE BLOCKS. Where the blocks comprising the cross-coupled parts of a LATCH or FLIP FLOP cannot be shown as a single block (FL or FF) then the two or more blocks which take part in the cross-coupling arrangement shall be placed adjacent on the same page. This rule shall also pertain to the POLARITY HOLD, with the additional requirement that the input AND's which form part of the POLARITY HOLD arrangement shall also be held adjacent.

7.1.1 Function Symbols. For block emphasis purposes the various blocks in the cross-coupling arrangement of FLIP FLOP, LATCH, or POLARITY HOLD shall each have the letters FF, FL, or PH (as the case may be) placed to the right of the primary block function symbol, unless this would conflict with a re-requirement for indicating DOT OR or DOT AND usage.

7.1.2 Counters and Registers. The repetitive elements of such logically related system subdivisions as counters and registers shall be arranged in linear fashion on the diagram page and numbered consecutively.

7.1.3 Examples. Figure 2-2 illustrates applications of the arrangement and titling rules given in this section.

8.0 SUPPLEMENTARY INFORMATION

8.1 POLARITY ASSIGNMENT. The question of whether to call a particular block an AND or an OR on the ALD's cannot be answered unequivocally for all cases. The same is true for those other circuits whose internal label is dependent upon a particular choice of input and output polarity indication. An ODD circuit, for instance, obviously becomes an EVEN if the output polarity indicator is changed. In order to establish a consistency in logic representation and to give, as far as possible, a clear rule for establishing block labels where the choice is arbitrary, the following practice is recommended:

> Beginning at a point in the logic where there is a storage block or other circuit type whose block symbol defines its input line polarity permanently, go backward from each input of this block. Assign polarity such that each end of a connecting line between two blocks has the same polarity. The labels of the blocks must, of course, be assigned according to the polarities chosen. The assignment of polarity along the various chains should be continued in this manner until one of the originating-type blocks or groupings is reached or a point of unavoidable conflict in polarity assignment is encountered.

8.2 LINE TITLE POLARITY. To provide consistency in the method of indicating the relative polarity of a line which pertains to the title of the line the following practice is strongly recommended:

> Precede all line titles with a + or - symbol to indicate the condition of the line for which the title state is valid. State the title wherever possible in words having a positive connotation. For instance, title a line "+read" rather than "-not read."

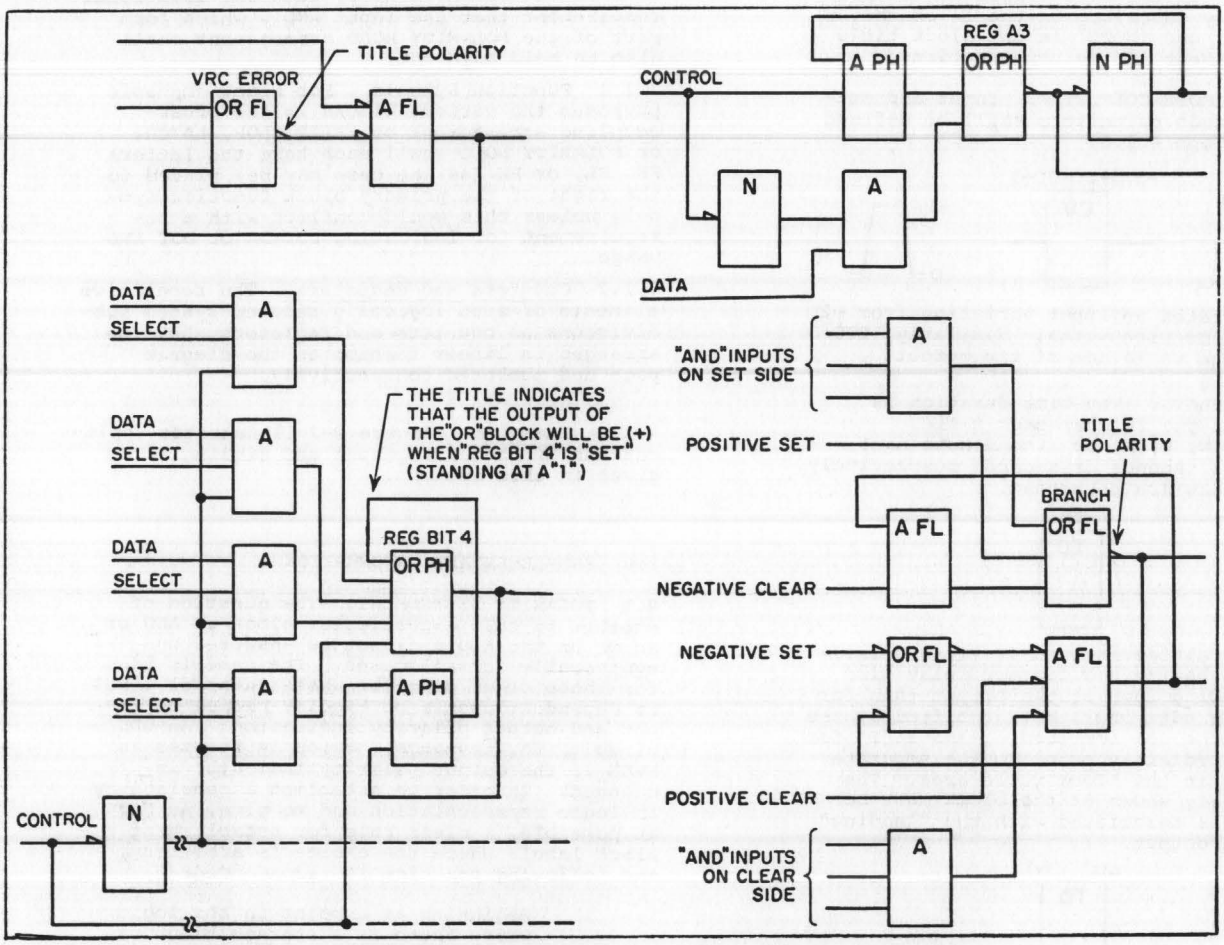


FIGURE 2-2. EXAMPLES OF MULTIPLE BLOCK STORAGE ELEMENTS

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Where a line leaves a page, title it in such a manner that the title polarity will agree with the polarity symbol shown at the source block.

8.3 VARIABLE TIMING OR FREQUENCY. It may, on occasion, be impossible to precisely specify the duration of a SINGLE SHOT or TIME DELAY block because provision exists for an adjustment. Similarly, it may be impossible to specify the output of an oscillator because its output is variable. Where this is the case, it is recommended that the letters VAR be included in the title area of the block or the range should be shown in the title area of the block.

8.3.1 Multiple Variable Circuits. If more than one variable circuit appears on the same card, then "L", "C", or "R" should be used in addition to the "VAR." Where L = left, C = center, R = right will locate the variable component on the card for the particular circuit when viewing the card from the component side with the pins to the bottom. More complex arrangements should be handled by the word NOTE, and spelled out in the comment section.

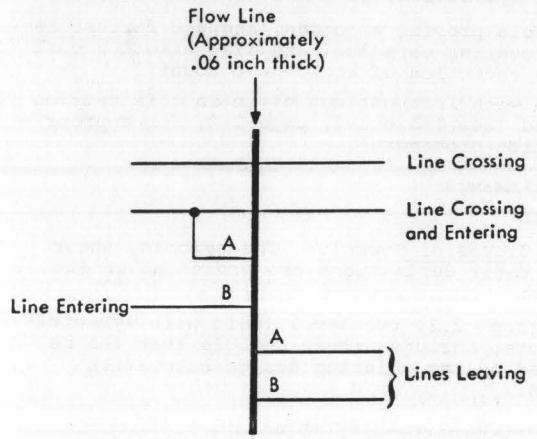
8.4 LOGIC FLOW LINES. Logic flow lines may be utilized on logic diagrams, in which case the following rules are recommended:

a. Parallel transfer between registers, counters, rings, or other well defined storage arrays.
b. Encoding and decoding that involves a specific register or counter where there is an orderly pattern in the configuration.
c. Other orderly patterned use to bring well defined groups of lines from one logically associated group of circuits to another logically associated group of circuits.

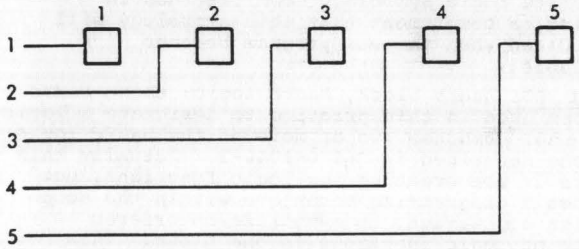
Note: DA Programs do not have the flow line capability.

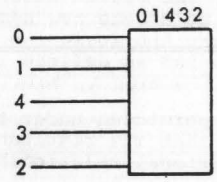
8.4.1 Rules Governing the Use of Logic Flow Lines

a. Information shall travel along a flow line in one direction only.
b. The point where a line crosses a flow line shall be separate from the point where the same line may enter the flow line.
c. Logic Flow Lines shall consist of well defined groups of four or more output or input signal lines.
d. Adequate routing information shall be supplied so that any line entering or leaving a flow line may be readily traced to its destination(s) or origination as the case may be.



8.5 BLOCK AND LINE ARRANGEMENT; wherever possible when an ordered series of numbers or blocks in a horizontal arrangement refers to a vertical arrangement, the correspondence shall be left to right in the horizontal referring to top to bottom in the vertical or vice versa.





1.0 INTRODUCTION

This section defines logic symbols used to represent monolithic circuitry for MST and SLD/SLT. The symbols represent:

a. Two levels of functions, with the first level symmetrical (identical functions).

b. Two levels of functions with the first level non-symmetrical or three levels of logic.

These symbols provide a common language for use between Engineering personnel and also effect a cost savings by reduction of logic page count.

Compliance with instructions given in this section is expected (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 REQUIREMENTS

2.1 GENERAL

2.1.1 Two Groups of Symbols: The symbols, their rules and their definitions are presented in two paragraphs:

a. Paragraph 2.2, two level logic with symmetrical inputs, includes those symbols that can be processed by the existing design automation programs.

b. Paragraph 2.3, three level logic and non-symmetrical two level logic, includes those symbols that require an advanced Design Automation program. This program will be available in November of 1967. However, as you review this section, you will see that if space is reserved for the required symbology, that the Macros in this section may be used in advance of the new program. This advance usage will be permitted, provided that the Corporate Logic Symbology Committee has in writing, a commitment that this symbology will be updated when the new program becomes available.

2.1.2 MACROS Macro block, Macro logic; these terms have been used in this practice to designate a logic symbol that combines two or more of the basic logic functions described in CES 0-1046-3. Actually this practice is not creating new logic functions, but describes a diagramming technique within the scope of design automation, to symbolize an ordered sequence of logic functions in one block. This combined symbol represents the butted block technique; there is no intent to create new symbols. It is important to note that ALL logic functions described in this practice ARE as defined in Basic Logic Block Symbols, Section A, this Part.

Combining of functions is permitted under the rules of this practice provided that the resultant symbol maintains the correct functional relationship between inputs and outputs.

2.1.3 Diagramming Technique. Figure 2-3 is an example of a macro symbol and the actual butted block symbology it represents. The butted block symbol will be produced for the field via the Field Engineering Design Automation (FEDA) print program.

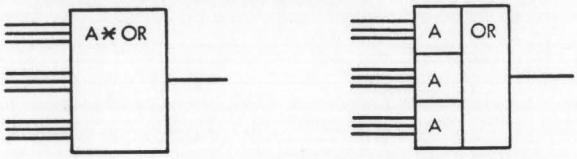


FIGURE 2-3. MACRO AND BUTTED BLOCK SYMBOLS

2.2 TWO LEVEL LOGIC SYMMETRICAL INPUTS

2.2.1 Rules

a. The hardware represented by the symbol must be contained within one integrated circuit module, (other circuitry in the same module is permissible). For SLT/SLD only, this restriction is at the card level.

b. The Inputs represent the first level of logic. Where indicated in the list of symbols they may be multiple functions, however, these functions must be identical, i.e. all AND's. The input function must be shown as the left function in the first tagging line of the symbol.

c. When multiple functions are used at the input level a space must be reserved between the inputs to each logic function. In addition, care must be exercised, when the full complement of inputs to a given input function are not used to remove the outside lines of the group, so as not to create a space that would appear to be additional logic grouping.

d. The outputs are all a function of the second level logic function operating on the first level input functions.

e. Only the following basic functions A, OR, AR, OE or ODD, may be used as first level inputs. Provided that the combined function does not require more than five (5) characters.

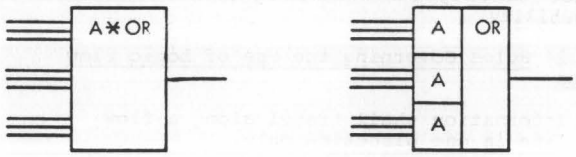
f. For SLT/SLD the inputs to any one input function must all be of the same polarity and contain the same voltage characteristics. (Pin interchangeability on that function.)

2.2.2 List of Symbols- For additional Combinations see paragraph 3.1.1.

2.2.2.1 AND to OR

a. Definition: The A*OR output(s) will stand at its indicated polarity when and only when one or more of the input AND groupings has all its inputs standing at their indicated polarity.

b. Symbol

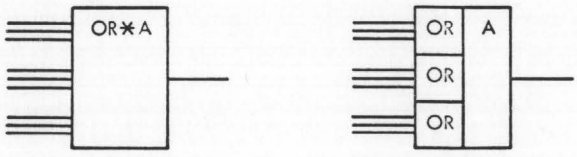


MACRO FEDA

2.2.2.2 OR to AND

a. Definition: The OR*A output(s) will stand at its indicated polarity when and only when all of the input OR groupings have one or more of their inputs standing at its indicated polarity.

b. Symbol

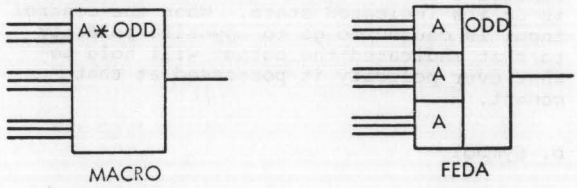


MACRO FEDA

2.2.2.3 AND to ODD

a. Definition: The A*ODD output(s) will stand at its indicated polarity when and only when an odd number of its input AND groupings has all its inputs standing at their indicated polarity.

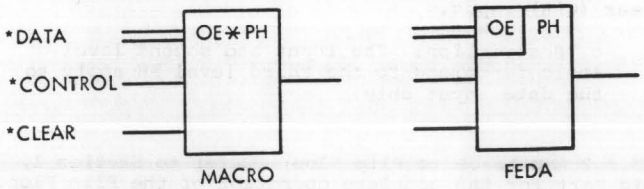
b. Symbol



2.2.2.4 Exclusive OR to Polarity Hold

a. Definition: The output of the OE*PH will be at its indicated polarity when one input to the OE grouping is at its indicated polarity and the control input is at its indicated state. When the control input is caused to go to opposite polarity to that indicated the output will hold whatever polarity it possessed at that moment. Note: The clear input is as specified in Section A, this Part.

b. Symbol



* Not part of the symbol

c. Restriction: The input logic function to the second level PH applies only to the data input, and only one such function is permitted. For multiple functions refer to paragraph 2.3.3.1.

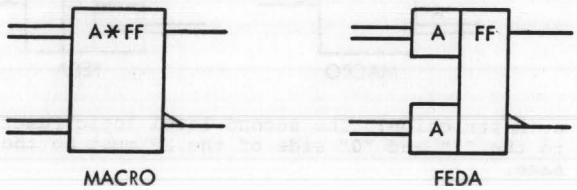
2.2.2.5 AND to Flip Flop; Refer to Section 1, this Part for the complete operation of the FF.

a. Definition:

1. The outputs of the A*FF are caused to go to their indicated polarity when all inputs opposite the "1" output (top) stand at their indicated polarity.

2. The outputs of the A*FF are caused to go the polarity opposite to those indicated when all inputs opposite the "0" output (bottom) stand at their indicated polarity.

b. Symbol

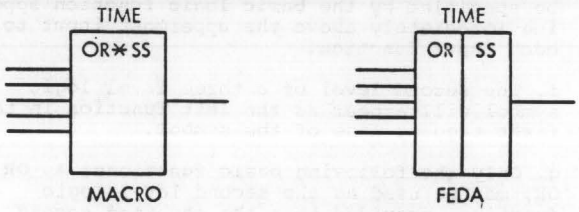


c. Restriction: The input logic function to the second level FF must be the same at the "1" and "0" inputs.

2.2.2.6 OR to Single Shot; Refer to Section A, this Part for complete requirements of the SS.

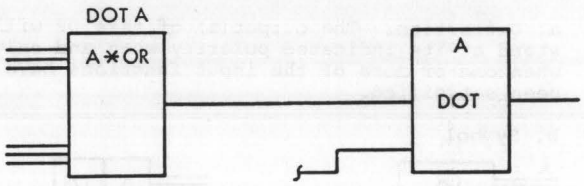
a. Definition: The output(s) of the OR*SS will change temporarily to the indicated polarity when and only when one or more of the inputs stand at its indicated polarity. The output will remain in this quasi-stable state for a time which is characteristic of the particular device.

b. Symbol



c. Restriction: Only one input function is permitted for the two level symbology.

2.2.3 Suffixes: DOT, FL, PH or others as specified in CES 0-1046-3 shall be used where ever possible. When the number of characters in the Macro function prohibits this, due to space requirements, the suffix will be ommitted from the logic block. However, where ever possible the omitted suffix shall be carried in the block title as follows.



CAUTION: When the DOT suffix is not in line one of the logic block, the DA program will not check the suffix and will produce suffix errata, however, DOT wiring rules are checked.

Note: For new design, after November 1967, the suffix conventions specified in paragraph 2.3.5 should be used.

2.3 TWO LEVEL LOGIC NON-SYMMETRICAL INPUT AND THREE LEVEL LOGIC MACROS.

2.3.1 Rules

a. The hardware represented by the symbol must be contained in one integrated circuit module, (other circuitry in the same module is permissible). For SLT/SLD only, this restriction is at the card level.

b. For SLT/SLD the inputs to any one input function must all be of the same polarity and contain the same voltage characteristics. (Pin interchangeability on that function)

SLT/SLD Technologies can NOT utilize the three level MACRO symbology.

c. The outputs are all a function of;
1. the second level logic function operating on the first level input functions, for two level logic.

2. the third level logic function operating on the preceding two levels, for three level logic.

d. Non-symmetrical input functions must be specified by the basic logic function appearing immediately above the uppermost input to each input function.

e. Three level logic, the input function must be specified by the basic logic function appearing immediately above the uppermost input to each input function.

f. The second level of a three level logic symbol will appear as the left function in the first tagging line of the symbol.

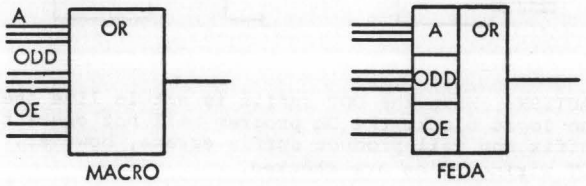
g. Only the following basic functions; A, OR, OE, may be used as the second level logic function, provided that the combined second and third level function does not require more than five (5) characters. The ODD function is permitted in the two level MACROS but not in three level macros.

2.3.2 List of Symbols, Non-Symmetrical Two Level Logic: for additional combinations see paragraph 3.1.2.

2.3.2.1 Non-symmetrical Input Functions to the OR these may be any combination of basic logic functions, excluding storage. (2.3.1 g)

a. Definition: The output(s) of this OR will stand at its indicated polarity when and only when one or more of the input functions have been satisified.

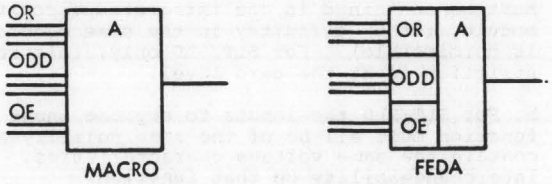
b. Symbol



2.3.2.2 Non-symmetrical input functions to the AND; these may be any combination of basic functions (excluding storage). (2.3.1 g)

a. Definition: The output(s) of the AND will stand at its indicated polarity when and only when all of the input functions have been satisfied.

b. Symbol

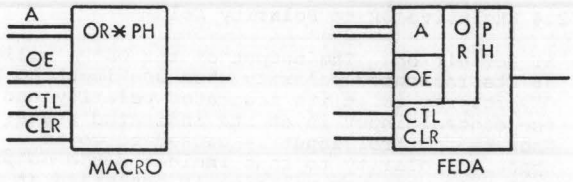


2.3.3 List of Symbols, Three Level Logic: For additional combination see paragraph 3.1.3.

2.3.3.1 AND to OR to PH

a. Definition: The output(s) of the three level logic OR*PH will be at its indicated polarity when one or more of its input functions are satisfied and the control input is at its indicated state. When the control input is caused to go to opposite polarity to that indicated the output will hold to what ever polarity it possessed at that moment.

b. Symbol



NOTE: In this representation it is necessary to establish the control (CTL) input, and if used the clear (CLR) input.

c. Restriction: The input and second level logic functions to the third level PH apply to the data input only.

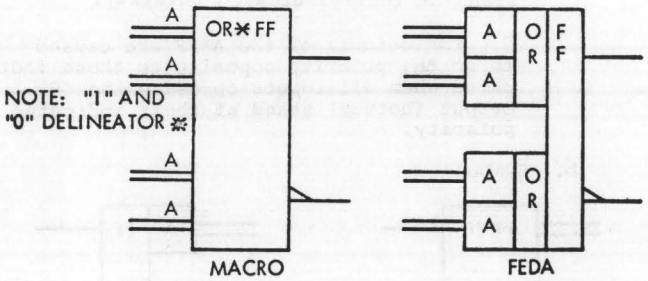
2.3.3.2 AND to OR to Flip Flop; Refer to Section 1, this Part for the complete operation of the Flip Flop.

a. Definition:

1. The outputs of the three level OR*FF are caused to go to their indicated polarity when one or more of the input functions opposite the "1" output (top) has been satisfied.

2. The outputs of the three level OR*FF are caused to go to the polarity opposite to those indicated when one or more of the input functions opposite the "0" output (bottom) has been satisfied.

b. Symbol

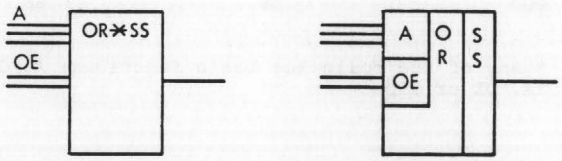


c. Restriction: The second level logic function to the "1" and "0" side of the FF must be the same.

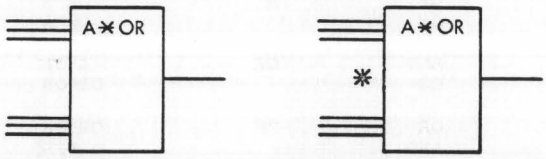
2.3.3.3 AND to OR to Single Shot; Refer to Section A, this Part for complete requirements of the SS.

a. Definition: The output(s) of the three level OR*SS will change temporarily to the indicated polarity when and only when one or more of the input functions are satisfied.

b. Symbol



2.3.4 Delineator; Shall be used with two level symmetrical macros. When the Advanced D.A. program is operational an "*" asterisk will be inserted in the space reserved between functional groupings automatically. The asterisk shall also be used to separate the "1" and "0" areas of a two and three level FF, also the Data, control, and clear inputs to the two level PH.



PRESENT NEW D.A. PROGRAM

2.3.5 Suffixes:

2.3.5.1 FL, PH, or Others: As specified in CES 0-1046-3 shall be used where ever possible. Where the Macro function prohibits this due to space requirements, the FL, PH or Other function shall be placed as the top line output pin position. Note: Output line position one shall be reserved for this purpose. (See Figure 2-4, a.)

2.3.5.2 DOT Functions; shall be indicated by placing the function immediately below the output being DOT'ed and adjacent to the block. Note: Reserve this line position when releasing a circuit who's logical output may be DOT'ed. (See Figure 2-4, b.)

CAUTION: When the DOT suffix is not in line one of the logic block, the DA program will not check the suffix and will produce suffix errata, however, DOT wiring rules are checked.

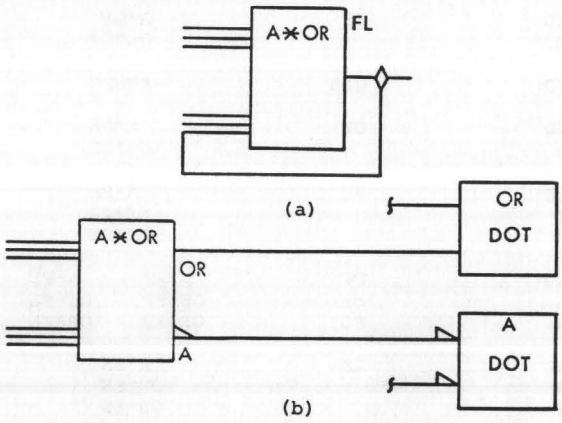


FIGURE 2-4. MACRO BLOCK SUFFIXES

3.0 SUPPLEMENTARY INFORMATION

3.1 LIST OF PERMISSIBLE COMBINATIONS: The definition & symbols given do not cover all possible combinations. The following list is given to fill in the gaps within the rules given for the various types. The definitions change to satisfy the new combinations per Section A, this Part.

3.1.1 Symmetrical Two Level

INPUT LEVEL	OUTPUT LEVEL	SYMBOL
OE	A	OE*A
ODD		ODD*A
OR		OR*A
AND	OR	A*OR
OE		OE*OR
AND	ODD	A*ODD
AND	OE	A*OE
OR		OR*OE
AND	PH	A*PH
OE		OE*PH
OR		OR*PH
AND	FF	A*FF A*FL
OE	or	OE*FF OE*FL
OR	FL	OR*FF OR*FL
AND	SS	A*SS
OE		OE*SS
OR		OR*SS

3.1.2 Non-symmetrical Two Level or Symmetrical where the combination of characters are more than five.

INPUT LEVEL	OUTPUT LEVEL	SYMBOL
*	AND	A
*	OR	OR
*	ODD	ODD
*	OE	OE
ODD	PH	PH
ODD	SS	SS

* Any of the following basic functions; A, OR, AR, OE or ODD.

NOTE: For the symmetrical two level ODD where the functional combination requires more than five characters, use the non-symmetrical symbology described in paragraph 2.3

3.1.3 Three Level Logic

INPUT LEVEL	SECOND LEVEL	OUTPUT LEVEL	SYMBOL
*	OR	A	OR*A
	OE		OE*A
*	AND	OR	A*OR
	OE		OE*OR
*	OR	PH	OR*PH
	AND		A*PH
	OE		OE*PH
*	AND	FF	A*FF A*FL
	OR	or	OR*FF OR*FL
	OE	FL	OE*FF OE*FL
*	AND	SS	A*SS
	OR		OR*SS
	OE		OE*SS

* Any of the following basic functions, A, OR, AR or OE.

1.0 INTRODUCTION

This section defines methods of representing pluggable jumper cards on automated logic diagrams and gives the format for reference page notes about jumper wiring.

Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 TERM DEFINITIONS

2.1 PLUGGABLE JUMPER CARDS resemble ordinary SLT cards, having hubs on them to accept pluggable jumpers. Insertion of these jumpers connects various card tabs. The jumpers are installed or not according to the machine features or wiring configuration. Jumper hubs may also appear on logic cards. The various uses of jumper cards are outlined below.

2.2 TIE DOWN JUMPERS are those which are required to stabilize certain inactive circuits. Tie-downs will be associated with lines which are floating due to the removal of a feature or ACC device if these floating lines may cause improper operation of other circuits which are still active. This definition does not include jumpers which are used to permanently tie a point to a set reference.

2.3 CONFIGURATION WIRING JUMPERS consist of those jumpers which are required to properly select one of two or more existing circuits to fulfill system or feature configuration requirements. Such circuits, while on cards required an ACC, may not themselves be used for that ACC. An example of this application is where different configurations may be wired after cards identified by one ACC are installed. Whether the unused circuits must be tied down or not will be determined by their effect upon the active circuits. Circuits which must be connected by configuration jumpers will be wired into the system as part of the basic wiring.

2.4 FEATURE WIRING is that wiring which is installed to provide a special feature and it is not normally wired as part of the basic machine. RPQ devices fall into this category.

3.0 WHERE USED

3.1 PLUGGABLE JUMPER cards may be used on systems and/or boxes not having lead length or stub restrictions due to circuit speed. Since tie-downs and configuration wiring jumpers are physically located on cards, they do not affect wire nets or rework instructions.

3.1.1 Version Pages must still be prepared for feature and RPQ wiring, however the use of jumper cards greatly reduces the need for version pages.

4.0 IMPLEMENTATION

4.1 REPRESENTATION of pluggable jumper cards is by logic blocks on automated Logic Diagrams generated by the SLDA program. Notes pertaining to jumper wiring configuration are placed on the reference pages of these diagrams. The logic blocks and reference pages are handled in a normal manner through the SLDA program. A pictorial representation of the jumper hubs on the cards is required within the machine documentation to correlate the logic block representation with the physical card.

4.2 RULES. The following rules must be observed in order to make the use of pluggable jumper cards compatible with the SLDA program.

4.2.1 Logic Block Representation Rules.

The following rules must be followed:

(a) The logic block symbol JMPR must be used.

(b) Gate, board and card socket locations must be indicated.

(c) Other logic block symbols such as block serial numbers, print positions and pin positions must be indicated.

(d) Tie-downs must be shown as logical sources, not sinks, tying from the output of the jumper block.

(e) The pluggable jumper card logic block must be placed as close as practical to the area of logic being tied down.

(f) All utilized pluggable jumper card pin locations must be shown on the logic block. Jumper block symbols used must be consistent with circuit flyer representations.

4.2.2 Jumper Card Wiring Details. Jumper card wiring details must be specified in one of the following methods:

(a) In the 14 spaces available in the logic block title above each logic block, or

(b) Use NOTE in the logic block title and refer to details in the comments section of the logic page on which the logic block is located (adequate space in the comments section must exist) or

(c) Use NOTE in the logic block title and refer to one or more reference pages containing jumper card wiring details.

Methods (b) and (c) must not be used at the same time so that the user will not be required to refer to more than one page to locate jumper card wiring details. If several notes are required, it is permissible and may be advantageous to use the comments section of the logic page as an intermediate means of expanding the note above the logic block. If more notes are required than will fit in the comments section of a page, the LADS program may be used to print reference pages of notes.

4.2.3 Reference Page or Comments Section Rules:

The following rules must be followed:

(a) The reference page or comments section must specify the logic page and block representing the repluggable jumper card.

(b) The reference page or comments section must specify jumper card terminals to distinguish them from card socket pins.

(c) The reference page or comments section must specify the jumper card physical location.

(d) Tables should be used to specify jumper card wiring details where possible.

(e) Layouts of pluggable jumper cards used by a specific system must be included on the reference pages.

4.3 ALD AND REFERENCE PAGE NOTATION. The following figures show various logic block representations used with jumper card wiring and their related reference page notes. These figures and notes are examples of implementation of the rules and are not necessarily complete.

4.3.1 Explanation of Jumper Card Function (Not to be included on logic page), (Use with Figure 2-5.) If ACC1, card AA, is removed the circuit between cards AA and AB may be floating. Connecting D04 to D08 on the jumper card will stabilize the AA-AB circuit at ground level. This type jumper circuit may also be used to stabilize floating circuits at any desired level.

4.3.2 Reference Page or Comments Section Notation.

EXAMPLE: NOTE 001, DR124, Logic block AC:
ACC1, Automatic reset on dual inquiry; card (A-A3H2)
If not installed, connect D04-D08 on jumper card (A-A3J2)

4.3.3 Explanation of Jumper Card Function (Not to be included on logic page). (Use with Figure 2-6.) This example is based upon the assumption that the circuitry at logic block BA is used only with a special feature. Adding or removing the B08-D09 jumper on card BB will complete or open the BA to BD circuit.

4.3.4 Reference Page or Comments Section Notation.

EXAMPLE: NOTE 002, DR 124, Logic Block BB
Double print adapter, card (B-C4A1)
If installed, connect B08-D09 on jumper card (B-C4A2)

4.3.5 Explanation of Jumper Card Function (Not to be included on logic pages.) (See Figure 2-7.) Basic wiring which may be connected for different configurations are indicated in this example. A circuit of this type may also be in an opposite configuration such as a single input with any one of several outputs being jumpered.

4.3.6 Reference Page or Comments Section Notation.

NOTE 003, Logic Page DR 124, Logic Block DD

Function	Connect	Do Not Connect	Jumper Card
100 position printer	D12-B13	D13 or B12	C-D4 H3
132 position printer	D13-B13	D12 or B12	"
150 position printer	B12-B13	D12 or D13	"

4.3.7 Jumper Hubs on Logic Cards. In cases where pluggable jumpers are used on logic cards and the hubs are not brought out to external pins the logic blocks are shown as in Figure 2-8.

4.3.8 Reference Page or Comments Section Notes.

NOTE 001, DR 126 Block AB
Internal Timer Feature
If installed, connect B02 to OR
circuit block serial AD

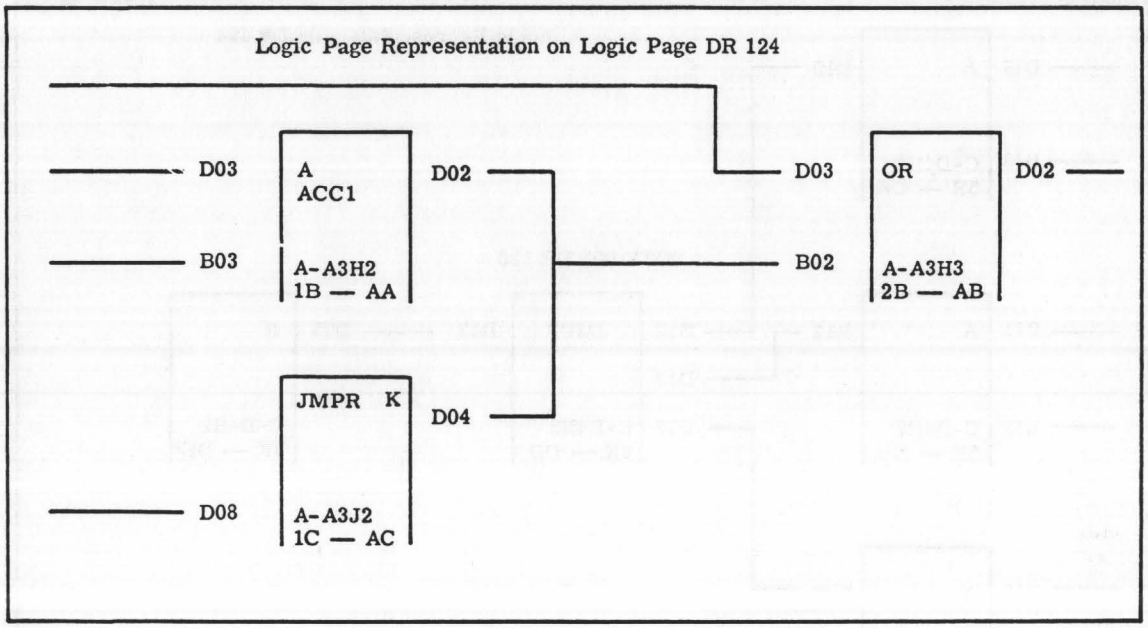


FIGURE 2-5. JUMPER USED TO STABLIZE FUNCTIONS

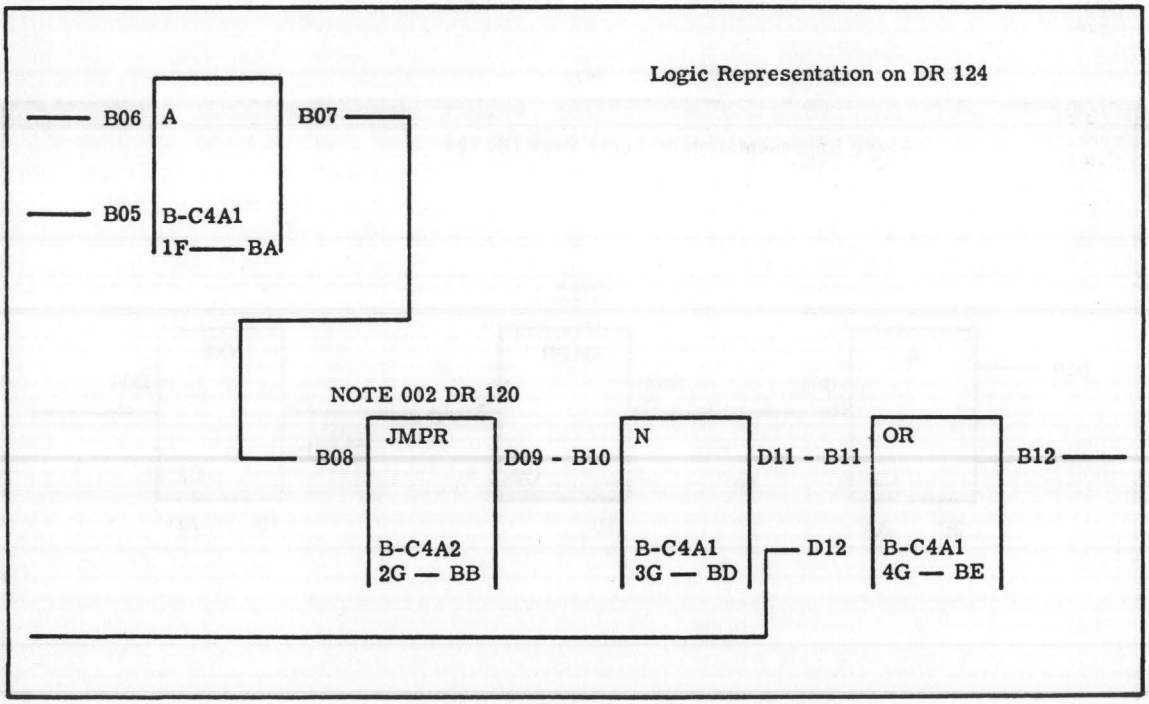


FIGURE 2-6. FEATURE INCORPORATED WITH JUMPER

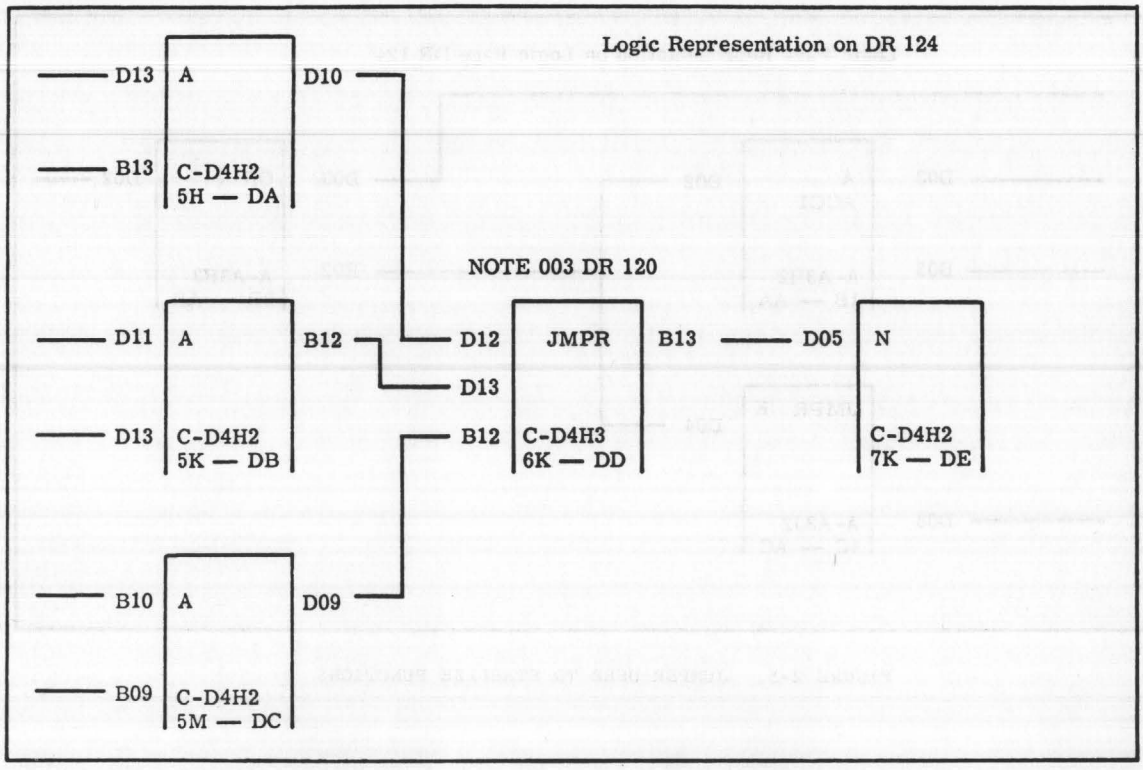


FIGURE 2-7. SELECTING A CIRCUIT WITH JUMPER

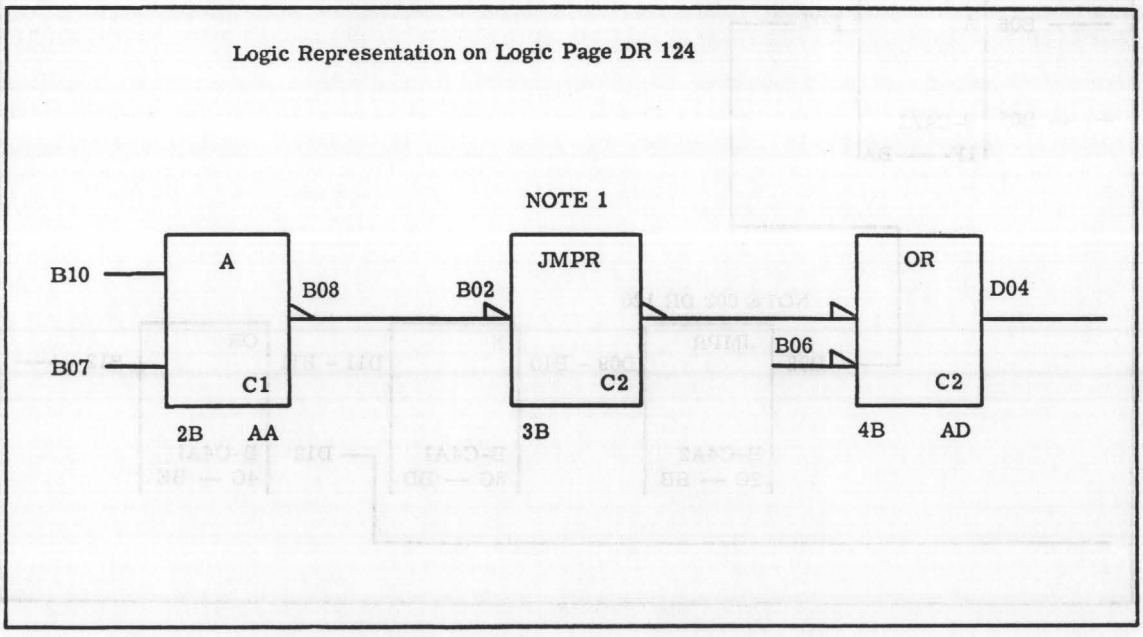


FIGURE 2-8. JUMPER NOT ASSOCIATED WITH EXTERNAL PINS

1.0 INTRODUCTION

This section describes documentation requirements for MAL.

Use of the rules in this section provide a symbol to depict the MAL circuitry and guide documentation of supporting information on logic diagrams. Related standards documents needed to complete the MAL documentation are also given.

Instructions given in this section are not mandatory: no deviation procedures are established.

2.0 REQUIREMENTS

2.1 GENERAL. The Monolithic Array Logic (MAL) module contains a matrix(s) of circuitry wherein each circuit may be constructed to provide a zero down level, or a one up level (logic assignment can be reversed). The module has associated with it logic circuits that perform the decoding function to select a specific address in the array, with additional controls to gate out selected cell(s) in the array.

2.1.1 Logic Representation. The MAL module provides Read Only Storage for a machine function. However, because it contains additional logic functions and must be designed and manufactured utilizing design automation and process automation, the module must be diagrammed on system and card ALD's.

For representation in MST DA Processing, Figure 1 illustrates the logic function in one symbol, utilizing English Pins to indicate a Decoder addressing an array with a Gate Out line. This representation is for use on Engineering Diagrams only that are not intended for the field; the FEALD program will convert this symbol to two blocks inline with proposed CES 0-1046-019.

2.1.2 Bit Pattern Charts. In order that the block symbol serves its purpose (determine the outputs from a given set of inputs), it is necessary to provide reference pages that indicate to those concerned the Bit Pattern pre-stored in the Array Matrix.

2.1.2.1 Bit Pattern documentation for the module will depend on established release procedures. For the MST-A MAL device, the Bit Pattern will reside in "Express". For other ROS devices, the circuit flyer should reference the device documentation that contains the Bit Charts.

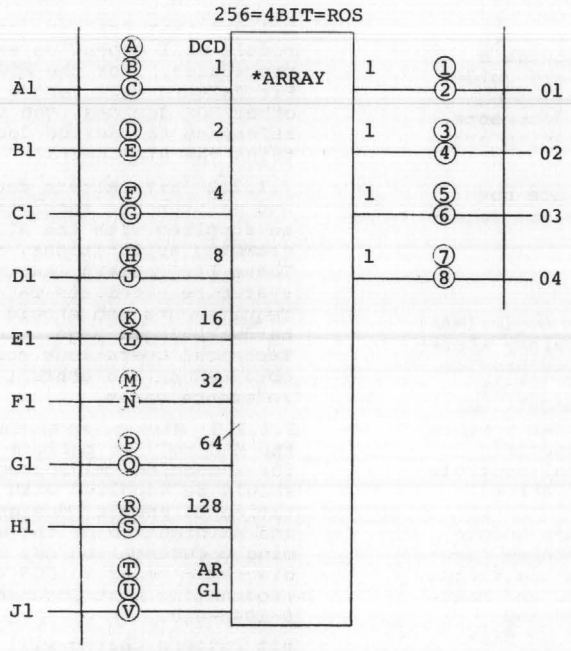
2.1.2.2 Bit Pattern documentation for system and maintenance requires a reference page(s) be supplied with the ALD's. (For microprogramming applications, see Paragraph 2.1.2.3.) These Bit Pattern Charts should reflect the system requirements rather than the device requirements and should cross reference the hardware logic page. Local Field Engineering Technical Operations concurrence should be obtained on the content and format of these reference pages.

2.1.2.3 Microprogramming Documentation. When the MAL modules perform the microprogramming for a machine, microprogramming documentation should be supplied with the release documentation to enable: design control, manufacturing and maintenance of the machine. Microprogramming documentation may be in the form of CAS diagrams; refer to CES 0-1046-004; or, Microprogramming List Documentation, refer to DEP 0-1046-018.

Bit Pattern Charts will follow the address list requirements of the Microprogramming standard that is used. In addition, the address list should cross reference the logic hardware page(s) generating the micro word.

3.0 SUPPLEMENTARY INFORMATION

3.1 The logic representation shown in Figure 2-9 is for the MAL 256 word, 4 bit device. Other ROS devices should be similar, however, since the logic representation is a deviation from the Corporate standard, any new symbol require proper approvals before use. Contact your local Engineering Standards department or the Logic Symbology Standards Development Project (SDP).



Note: Equal signs in block title and circled letters and numerals are for DA purposes only.

FIGURE 2-9. MAL LOGIC REPRESENTATION

Note on Circuit Flyers: Bit tables must appear on a system reference page. The system page containing this block configuration must cross reference the bit tables by a comment.

1.0 INTRODUCTION

This section defines application of logic symbology standards documents to EIS unreleased ALD and applies only to unreleased Engineering diagrams produced by EIS for product design purposes.

Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 REQUIREMENTS

2.1 GENERAL. Implementation of the requirements given in this Section should be in accordance with instructions provided in Paragraph 1.6 of the introduction of this booklet (see page 1-3).

2.1.1 Corporate Engineering Standards. This standard supplements the following Corporate Logic Standards for EIS users ONLY:

CES 0-1046-003, Digital Logic Block Symbology
CES 0-1046-005, Analog Logic Block Symbols
CES 0-1046-010, Automated Logic Diagrams, Pluggable Jumper Card Representation
CES 0-1046-017, Solid Logic Design Automation, Macro Logic Block Symbols
DES 0-1046-019, Functional Logic Block Symbols

2.2 PRACTICES. Whenever existing requirements are deemed inadequate for a technology using EIS or the need would require extensive addition to existing practices, then a new practice(s) shall be prepared and distributed through the Logic Symbology SDP. Refer to the booklet Contents to locate the available EIS practices.

Recommendations in any of the Logic Symbology Practices may be used when applicable, regardless of technology.

Each technology, when need for a new practice has been determined, will insure the necessary interface to satisfy the needs of all users. This will be accomplished by preparing the practice with the concurrence of EIS DA, FE Division, the Logic Symbology SDP and other users of EIS DA.

2.3 LOGIC SYMBOLS. The symbols established in the above Corporate Engineering Standards (Paragraph 2.1.1) shall be used whenever possible. THERE SHALL BE NO ATTEMPT TO CREATE A NEW SYMBOL WHEN ONE ALREADY EXISTS. For example, the AND function is indicated by the **letter "A"; +A, -A, NAND or NOR are** not standard. Another example, all amplifiers are indicated by AR: LD (line driver), MHD (magnetic head driver), or LLD (long line driver) are not standard. A suffix may be added to the AR by a dash. See Paragraph 4.3.1 of CES 0-1046-003.

2.3.1 Responsibility. Compliance to a practice is expected. If the use of a symbol impacts any interface requirements or other persons dependent on the EIS ALD, it is the responsibility of the group issuing the symbol to satisfy all requirements.

2.3.2 New Logic Symbols. A new non-standard symbol for a limited application will not require the task force consideration. (See Paragraph 1.6 of Introduction to the booklet on Page 1-3 to determine procedure.)

A new symbol may fall into either of two categories:

a) The block rules contain a structure of interconnected standard symbols.

b) There is no standard symbol structured in the rules. Approval of the proposed symbol must be obtained from Field Engineering Division and Test Engineering.

In either of the above cases, copies of the new symbol and its description must be sent to:

FE AMD - Raleigh.

CD - Appropriate project office.

SDD - Kingston Logic Symbology SDP.

3.0 SUPPLEMENTARY INFORMATION

3.1 ASSESSMENT.

The Logic Symbology SDP will assess this new approach to logic standards. The SDP will use the Logic Symbology Committee and Committee Correspondents to evaluate the effectiveness of this program.

3.2 ASSISTANCE.

The Logic Symbology SDP requests that problems encountered when using the EIS ALD's be reported. If a problem is recognized, communicate with your local standards organization.

1.0 INTRODUCTION

1.1 SCOPE. This standard defines a functional logic symbology for high density digital circuitry. It defines a dependency notation system that provides for common controls to large portions of circuitry. This standard also provides a new symbology that encompasses in one symbol all types of storage devices; namely, FLIP-FLOPS, FLIP-LATCH, POLARITY-HOLD, and combinations of these.

1.2 OBJECTIVES. To provide a more comprehensive functional diagram by replacing large groupings of interconnected basic logic (AND's, OR's, etc.) by one symbol. To provide more direct information for maintenance by making the important test points stand out. To reduce system page count.

1.3 APPLICABILITY. This standard is applicable to Maintenance Automated Logic Diagrams (MALD's) to development engineering projects working with Design Automation systems capable of producing this symbology (EIS or subsequent DA systems) and all hand generated diagrams.

1.4 OPTIONS. Several Sections of this standard provide two sets of symbols:

Design (DALD), for use on engineering diagrams not intended for field use.

Maintenance (MALD), for use on all diagrams intended for field use.

1.5 SUPERSEDES Paragraph 4.1.9 of CES 0-1046-003 for machines using EIS on subsequent DA systems. However, the remainder of CES 0-1046-003 is supplemented by this standard rather than superseded.

2.0 REQUIREMENTS

2.1 GENERAL. The symbology presented in the following paragraphs may be used on any level of diagrams requiring a logic symbol provided that the circuits are packaged in logical groupings consistent with this standard. It is imperative that the boundary of the symbol used does not encompass any connection points required at that diagram level. For example, the REGISTER described in this standard would not be feasible for card packaged logic which must provide module pins, unless it were contained in one module, but should be used for system logic which only requires that card pins be shown.

2.1.1 Device. The term "device" used in this symbology encompasses different types of packaging that a logic function appears in. Device can be used to describe a group of interconnected circuit elements, or interconnected modules as the case may be. Therefore, a group of interconnected AND and OR circuits performing a defined device function may use that functional symbol providing that engineering information required for that level of design is not lost.

2.1.2 Illustrations. The figures in this standard show the DALD and MALD presentations of defined logic functions with equivalent basic configurations of symbols given in CES 0-1046-003, "Digital Logic Block Symbology".

2.1.2.1 Non-Exhaustive. Figures in this standard exemplify several combinations of defined symbols. There is no intent that these illustrations exhaust all permissible combinations.

2.1.2.2 Pin Information. There is no attempt to show physical pin information with the symbols. When required, it shall be added to the diagrams with its associated signal line in a consistent manner.

2.1.2.3 Design-ALD Symbols. All DALD symbols will have a leading letter (with or without numerals) adjacent to the logic symbols on all input lines and have a leading numeral next to the logic symbol on the output lines. This line information is referred to as "bundle pin" designations and is required for EIS DA purposes. The letters and numerals have no symbolic meaning in this standard, nor have they been assigned to utilize the "bundling" concept. Bundling will be a subject in a future standard. The line function designation or dependency notation is separated from the bundled pin information by a colon. In actual use, a physical pin identity may appear as D04/S:A.

2.1.2.4 Maintenance ALD Symbols. In this standard, the MALD symbol is the one that is used when a figure is required to illustrate a rule.

2.2 FLIP-FLOPS. A group of circuit elements or basic logic functions interconnected to perform the storage function. The FLIP-FLOP (FF) is a device that has two stable states which are referred to as the One state (Set) and the Zero state (Reset). The outputs shall be shown with polarity indicating the One state of the device. The FF has several possible basic inputs that affect the state of the device as indicated in the definitions given below. Any number of inputs may be used and in combinations dependent upon the design of the device. In addition, these inputs or the outputs may be gated dependencies as described in Paragraph 2.3. These input line designations are part of the symbol. See Figure 2-10.

A storage device with S, R, G inputs only may be designated as a FLIP-LATCH, "FL", one with C, CD, R, G may be designated as a Polarity Hold, "PH". All other combinations of inputs shall be designated as a FLIP-FLOP, "FF".

2.2.1 Input, S, (Set) and R, (Reset).

2.2.1.1 Input S. When the S input stands at its indicated polarity (the One state) it imposes the One state on the storage element, and the outputs will stand at their indicated polarity. Its return to the Zero state (polarity opposite that shown) produces no action.

2.2.1.2 Input R. When input R stands at its indicated polarity (its One state) it imposes the Zero state on the storage element. The outputs will stand at the polarity opposite to that shown. The return of the R input to the Zero state produces no action.

2.2.1.3 Application of Inputs R and S. Application of the R and S inputs depends on one or the other being active, but not both. When both R and S inputs are simultaneously brought to their indicated polarity, the polarity the outputs will assume is dependent upon the circuitry, not on the logic function. If this condition is utilized in the logic, then the FF must be noted and the outputs defined in the comment section.

2.2.2 Inputs J and K.

2.2.2.1 Input J. When the J input stands at its indicated polarity (One state), the outputs of the storage device will stand at their indicated polarity (One state). Its return to the Zero state (polarity opposite to that shown) produces no action.

2.2.2.2 Input K. When the K input stands at its indicated polarity (One state), then the outputs of the storage device will stand at the polarity opposite to that indicated (Zero state). Its return to the Zero state produces no action.

2.2.2.3 Application. Inputs J and K are analogous to inputs R and S except that simultaneous application of inputs J and K at their indicated polarity will cause the outputs to change to the polarity opposte to that held just prior to this application. In other words, it complements the storage element.

2.2.3 Input T. Input T is a complementing input. It produces a change in the state of the storage element each time it comes to its indicated polarity; i.e., if the storage device is in its One state (the outputs standing at their indicated polarities), the outputs would be changed to the polarities opposite that shown when the T input comes to its indicated polarity.

2.2.4 Inputs C and CD.

2.2.4.1 Input CD. A single data-type input which at indicated polarity will set the flip-flop and at opposite polarity will reset the flip-flop provided that its associated control input C stands at its indicated polarity.

2.2.4.2 Input C. A control input which at indicated polarity will allow its associated CD entry (which may be further dependent upon a G gating signal) to set or reset the flip-flop according to CD signal polarity. At such time that a C input takes on polarity opposite to that indicated, the FF will retain its existing state.

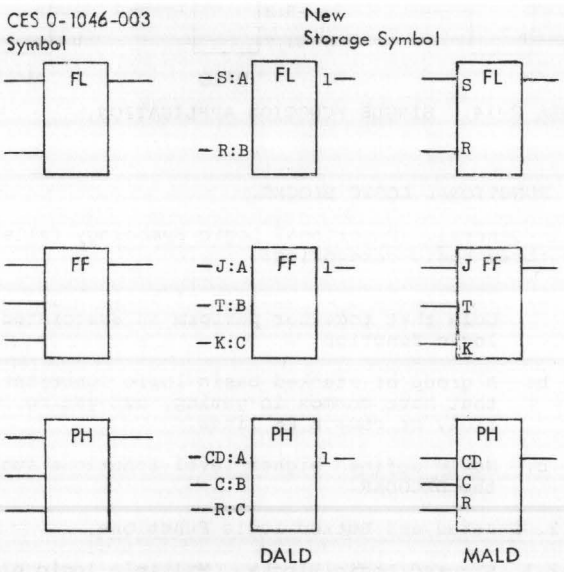


FIGURE 2-10. BASIC STORAGE SYMBOL.

2.2.5 Ambiguous Outputs. Ambiguous autputs exist when there is simultaneous application of two or more input signals of indicated polarity whose combined action is not defined, for instance, S and K inputs.

2.2.5.1 Output Notatipn Scheme. The following convention may be added to the storage element to denote the state of the outputs during application of simultaneous S and R inputs. See Figure 2-11.

RULE: "The application of simultaneous inputs will be considered as always causing the storage element to go to the Set state (outputs stand at their indicated polarity) which will be noted with the letter S. Storage output(s) that go to the opposite polarity will be noted by the letter R. If the state of the output cannot be determined, then the R or S is not shown.

This notation scheme is not based on logic utilization of simultaneous inputs. See paragraph 2.2.1.3.

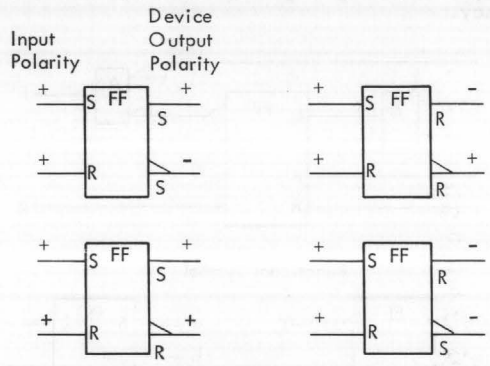


FIGURE 2-11. AMBIGUOUS INPUT NOTATION.

2.2.6 Inherent OR Function. All combinations or multiples of the defined inputs are permissible. These inputs are functionally OR'ed into the storage device in accordance with their definition (excludes simultaneous inputs). See Figure 2-12.

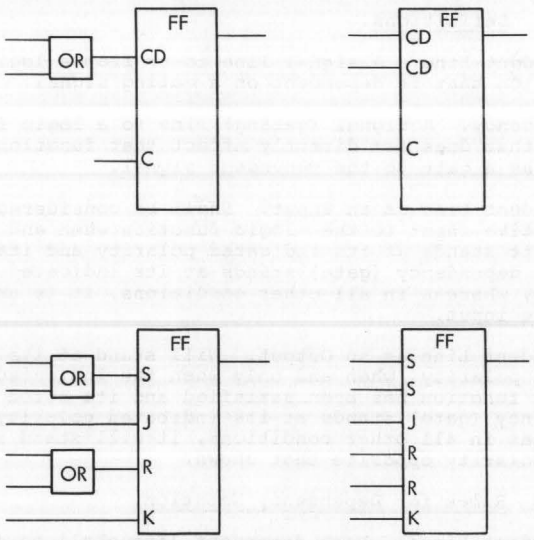


FIGURE 2-12. INHERENT OR IN THE FLIP-FLOP.

2.3 LINE DEPENDENCY NOTATION. This notation can be considered to be a method representing the AND function without the use of the AND logic symbol. Its use simplifies the representation of high density packaged logic. For example, gated storage element or groups of logic AND's and OR's having common connections that perform higher level logic functions.

2.3.1 Explanation, Definition and Rules. Figure 2-13 is provided to illustrate the dependency notation. Input b and Output f are dependent lines. Input d is the dependency for Input b and is called G1. The Input b is noted with a 1 to complete the input dependency notation. Input e is the dependency for Output f. It is indicated as G2. Output f is designated with a 2 to complete its dependency notation. Inputs a, c and Output g are lines that have no dependency.

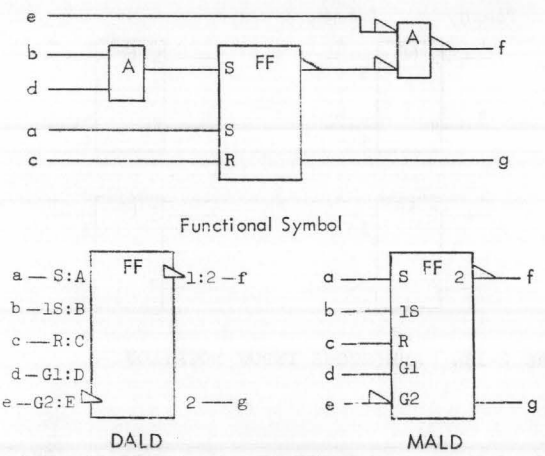


FIGURE 2-13. DEPENDENCY NOTATION.

2.3.2 Definitions.

Dependent Line. A signal line to or from a logic function that is dependent on a gating signal.

Dependency. A signal (gating) line to a logic function that does not directly affect that function, but acts as a gate to the dependent signal.

Dependent Line as an Input. Shall be considered as an active input to the logic function when and only when it stands at its indicated polarity and its noted dependency (gate) stands at its indicated polarity, whereas in all other conditions, it is an inactive input.

Dependent Line as an Output. Will stand at its indicated polarity, when and only when the indicated logic function has been satisfied and its noted dependency (gate) stands at its indicated polarity, whereas in all other conditions, it will stand at the polarity opposite that shown.

2.3.3 Rules for Dependency Notation.

Dependent Lines. Each dependent line shall be identified with the same numeral used to identify its related gating line. The numeral shall be placed opposite the line within the MALD logic block, or in the English Pin Field, on DALD's.

Gating Lines (Dependency). The gating lines shall be numbered 1, 2, etc. Each gate shall have a unique number. In addition to being numbered, each of the dependency lines shall be identified by the letter "G" preceding the numeral. In addition, the following rules apply:

a. Application of numbers to G shall not be duplicated. If more than one control, C Input, is required to the common section of a register (see Paragraph 2.4.3.4), then these also would require non-duplicated numbers.

b. When the dependency notation is used with a Decoder (see Paragraph 2.4.4), the gating line shall be lettered in place of the number; i.e., GA.

c. The dependency notation shall not replace the AND function in the basic form.

2.3.4 Single Function Application. See Figure 2-14. The dependency notation may be applied to a single logic function, other than the AND function. In this application, both the input and output lines shall be drawn to the bottom of the logic symbol.

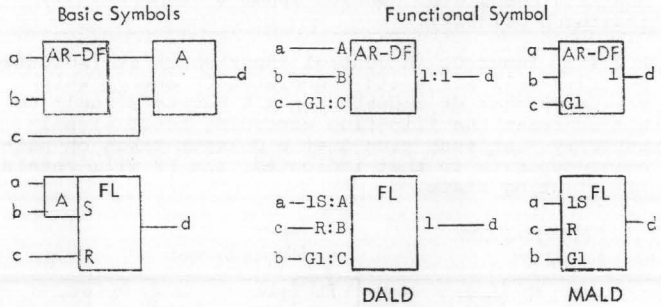


FIGURE 2-14. SINGLE FUNCTION APPLICATION.

2.4 FUNCTIONAL LOGIC BLOCKS.

2.4.1 General. Functional Logic Symbology falls into three basic categories:

a. The stacking or butting of basic logic symbols that together perform an associated logic function.

b. A group of stacked basic logic functions that have common in-gating, out-gating, control, or common FF lines.

c. Newly defined higher level functions such as the DECODER.

2.4.2 Stacked and Butted Logic Functions.

2.4.2.1 Stacked Logic Blocks. Multiple logic blocks of the same type should be stacked when it is advantageous to call attention to their associated logic meaning. For example, a group of signal converters feeding a word register. See Figure 2-15.

2.4.2.2 Butted Logic Blocks. Basic logic blocks should be butted to other basic blocks or to functional blocks whenever it is required to show associated serial logic functions provided that no test point information is suppressed.

RULES:

a. There is no logic connection when the line common to two symbols is the direction of information flow, unless specifically defined in this standard.

b. There is a single logic connection without logic inversion when a line common to two symbols is perpendicular to the direction of information flow.

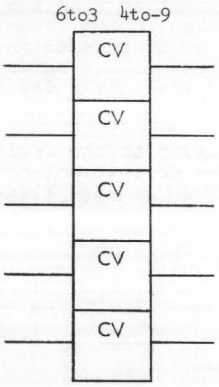


FIGURE 2-15. VERTICALLY STACKED LOGIC.

2.4.3 Functional Logic Blocks with Common Inputs.

2.4.3.1 General. This symbol shall consist of two sections, the data section and the common section. See Figure 2-16.

Data Section. The data section is a group of vertically stacked (butted) functional elements. The height of each logic element may vary with the number of inputs and the amount of data to be placed in each; the width, as required, for maximum data content, shall be the same for all elements.

The horizontal line separating the functional elements may be omitted where specified in the following paragraphs.

Common Section. The common section is located at the tope of the data section and on MALD's separated from the top functional element by a notch which forms a neck. The neck may vary in length consistent with diagramming needs. On DALD's, a double line or equivalent may be used to separate the common section. The height of the common section shall depend on the number of inputs, its width shall be the same as the attached logic elements.

RULES:

a. No lines may pass through the neck area.

b. The common section shall be used only for the dependency (gating) and/or common lines for the register.

c. There shall be no outputs from the common section.

d. The common section shall have the block's functional name on the top line, consistent with the following paragraphs.

e. Basic logic blocks may be butted to the common section or to the data section, as required.

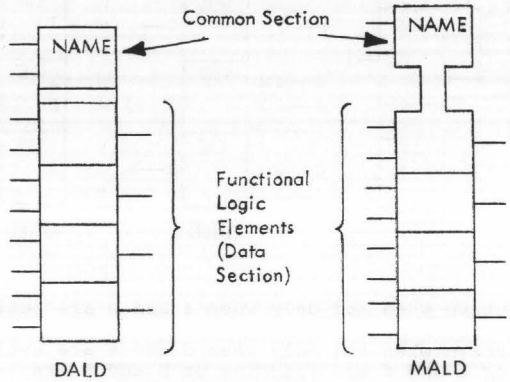


FIGURE 2-16. FUNCTIONAL LOGIC BLOCK.

2.4.3.2 Common Function. The common section may be associated with any group of basic logic elements functionally grouped by their dependent gating. For this application, each functional element shall contain the proper letter(s) that makes it an approved logic symbol. The common section may contain the letters COM at the very top line. See Figure 2-17.

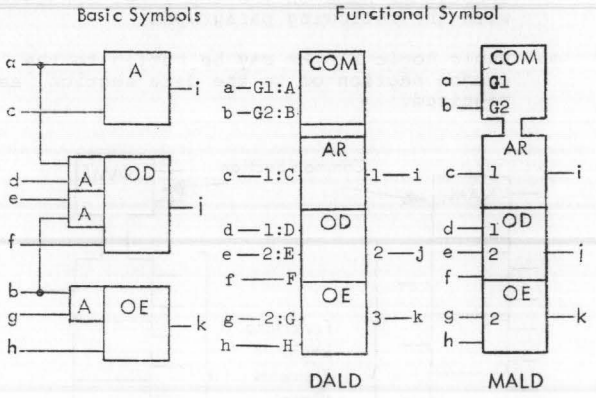
DEFINITION. Definition of a particular Common Functional Logic Block is arrived at by combining the definition of the dependent lines and that basic logic element used to make up the data section.

2.4.3.3 Selector. The selector is a functional logic block that consists of two or more OR's having input and/or output signals dependent upon common gates and utilizing the dependnet notation. See Figure 2-18.

Common Section: Gating lines common to one or more logic elements should be drawn to the common section. The letters SEL may appear on the top line of the common section.

Data Section: The data section consists of two or more stacked logical OR functions. The OR'ed inputs with their outputs are shown with their dependent notation wherever applicable. Non-dependent lines are shown without a dependency notation. On MALD's, the OR function shall be shown by use of the "◇" connection symbol for fan in and fan out. In this representation the horizontal lines separating the OR functions are not required.

Definition: The definition of a SELECTOR function is provided by combining the definition of the dependent lines and that of the basic OR function.



i is active when and only when a and c are active.

j is active when and only when d and a are active, and b or e and f are inactive or b and e are --etc.

k is active when and only when g and b are active and h is inactive or when h is active and g or b is inactive.

FIGURE 2-17. COMMON FUNCTIONAL SYMBOL.

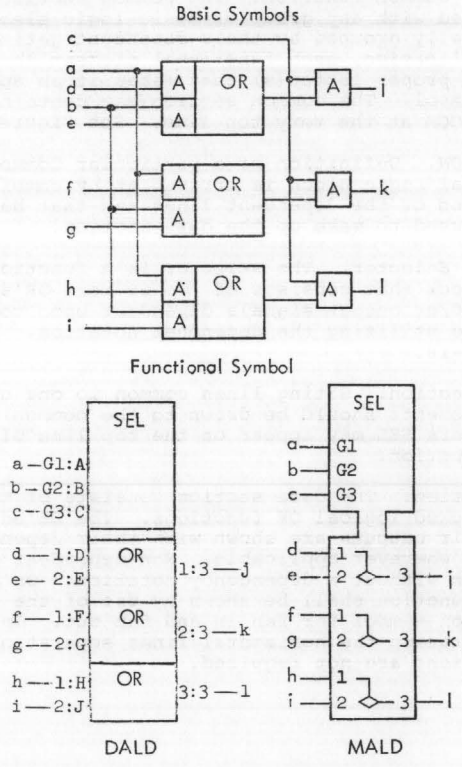


FIGURE 2-18. SELECTOR FUNCTIONAL SYMBOL.

2.4.3.4 Register Functional Logic Block. A register logic block consists of a group of associated FLIP-FLOPS (FF) with common input and/or output gating or other common input lines such as Reset. See Figure 2-19.

Common Section: A line common to all logic elements shall be drawn to the common section of the logic symbol and shall be identified as described in the paragraph under FLIP-FLOPS as applicable. Gating lines common to one or more storage elements should also be drawn to the Common Section. The top line of the common section may contain the letters "REG".

Data Section: The data section shall consist of two or more FF logic elements. The letters "FF" need not appear in each element. However, descriptive nomenclature such as Bit 1, may be placed in each logic element. The horizontal line separating the functional elements may be omitted from the MALD symbol for the simple cases; i.e., CD or S inputs only. All signal inputs must be identified in accordance with Paragraph 2.2. Inputs and/or outputs shall be additionally identified with their dependency notation when applicable.

Definition: Definition of the register function is a combination of the definitions of the particular signals into any given storage element plus the AND definition when the dependency notation is applied.

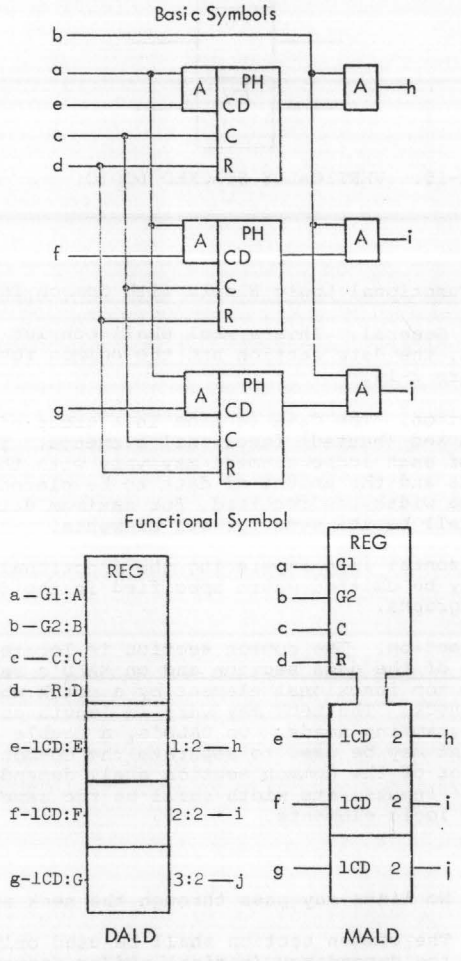


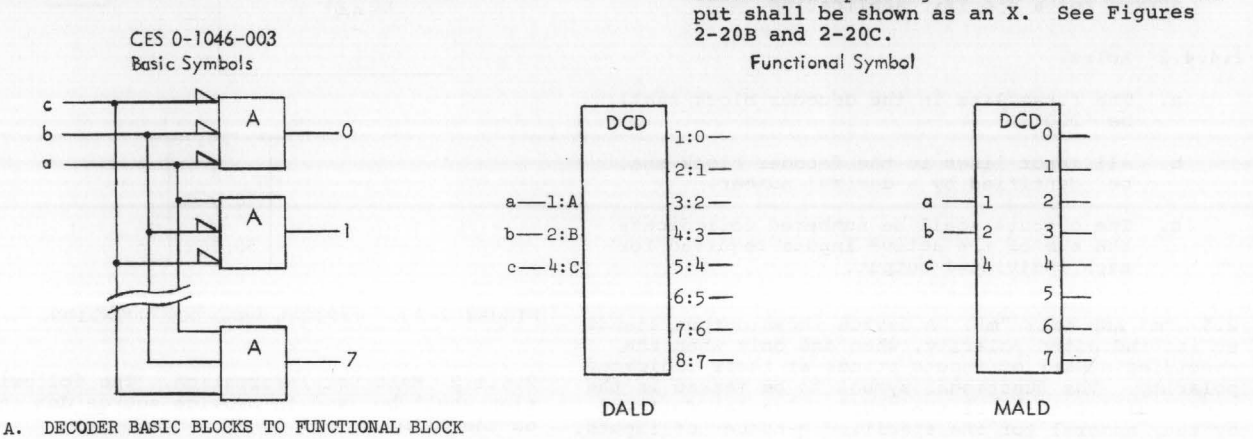
FIGURE 2-19. REGISTER FUNCTIONAL SYMBOL.

2.4.4 Decoder.

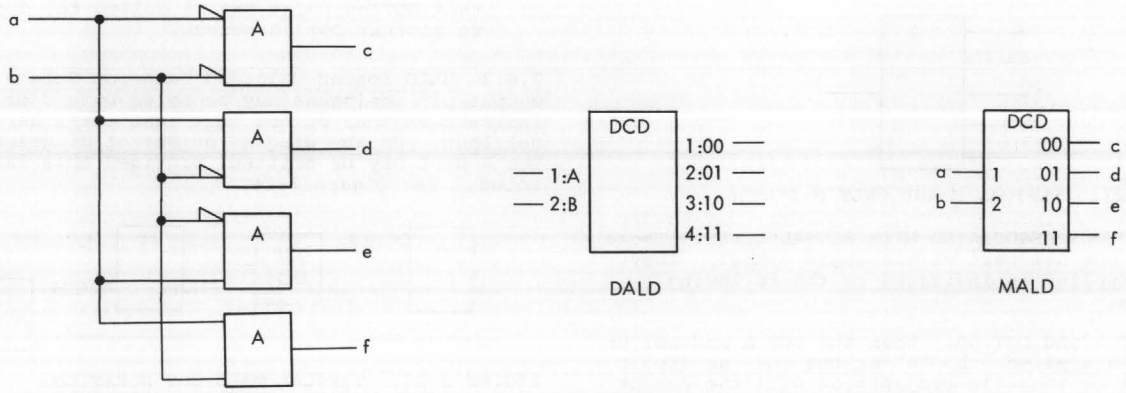
2.4.4.1 Definition: A particular output line from the decoder will stand at its indicated polarity if and only if:

a. The decimal sums of the line labels of all those inputs which assume their indicated polarity equals the value of the line label shown at the output. See Figure 2-20A.

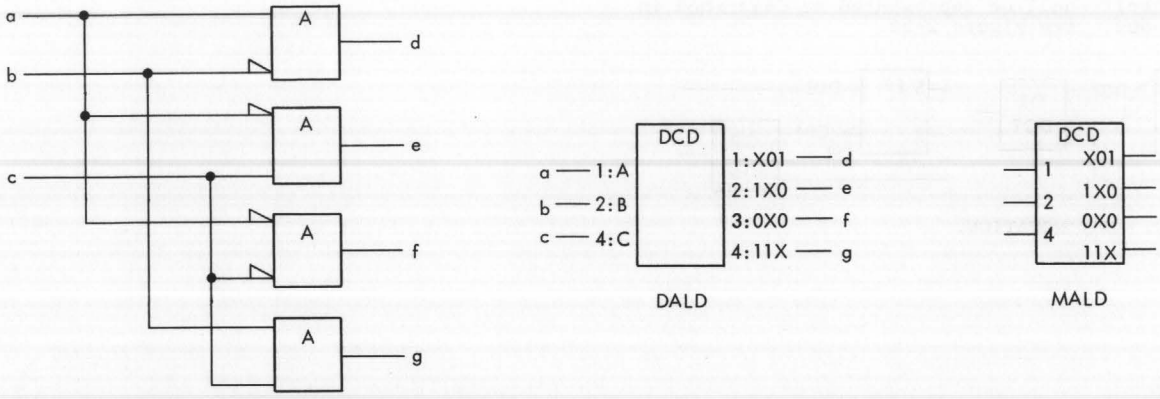
b. The binary value existing at the decoder inputs agrees with the binary number shown at the output line labels. The binary digit position on the output lines shall be established on the basis of a right-to-left (rightmost digit is the low-order bit), top-to-bottom correspondence of the input line positions. Where a decoder output is not affected by a particular entry line, the digit position in the binary number line label corresponding to the non-affected input shall be shown as an X. See Figures 2-20B and 2-20C.



A. DECODER BASIC BLOCKS TO FUNCTIONAL BLOCK



B. DECODER WITH BINARY CODED OUTPUTS



C. DECODER WITH DON'T CARE CONDITION

FIGURE 2-20. DECODER FUNCTIONAL SYMBOL.

c. An intermix of the two output coding methods of a and b is permitted.

NOTES:

1. At any given time there is only one sum. If all input lines are inactive, the sum is 0.

2. The use of all possible outputs is not a requirement. Therefore, all outputs could be inactive for a specific application.

2.4.4.2 Rules.

a. The first line in the decoder block shall be "DCD".

b. All input lines to the decoder block shall be identified by a decimal number.

c. The outputs shall be numbered to indicate the sum of the active inputs required for each individual output.

2.5 "m" AND ONLY "m". A device whose output stands at its indicated polarity, when and only when the specified number of inputs stands at their indicated polarity. The functional symbol to be marked in the block shall consist of the Equals sign (=) followed by the numeral for the specified m-number of inputs. See Figure 2-21.

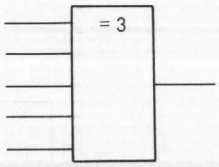


FIGURE 2-21. TYPICAL M AND ONLY M SYMBOL

2.6 NOTATIONS ASSOCIATED WITH SIGNAL LINES. These notations are not part of the logic symbol. They shall be applied as indicated in the following paragraphs.

2.6.1 DOT A and DOT OR. When the DOT A and DOT OR notation is applied, the "A" or the "OR" as applicable shall be shown in conjunction with the output line affected, in a standard location for any set of documents. The functional symbol within the logic block shall not be suffixed. The DOT A or DOT OR function itself shall be represented as described in CES 0-1046-003. See Figure 2-22.

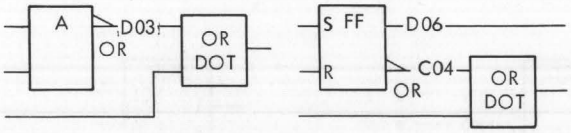


FIGURE 2-22. DOT NOTATION.

2.6.1.1 DALD's produced by EIS DA will not depict the DOT function at the source block. However, it will flag the line and list the DOT function with the Pin List at the bottom of the ALD. See Figure 2-23.

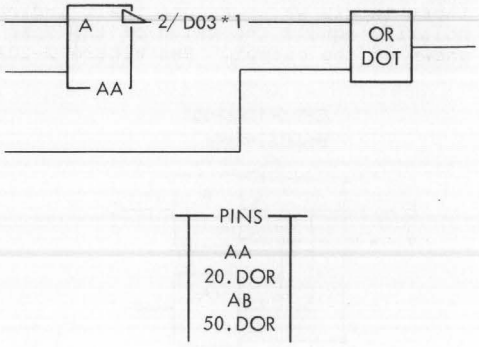


FIGURE 2-23. TYPICAL DALD DOT NOTATION.

2.6.1.2 MALD Dot Information. The following notation shall be used to provide source dot information on the MALD:

A Plus (+) or Minus (▽) indicates what that DOT'ed point can be pulled to, due to another DOT'ed source.

2.6.2 MALD Loaded-Unloaded Notation Scheme. All output pin positions may be noted by a U or L to indicate whether or not that test point has an internal load. On any diagram or set of diagrams, either the U or L may be omitted, provided this fact is noted. See Figure 2-24.

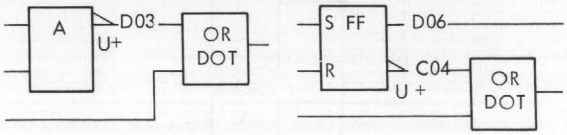
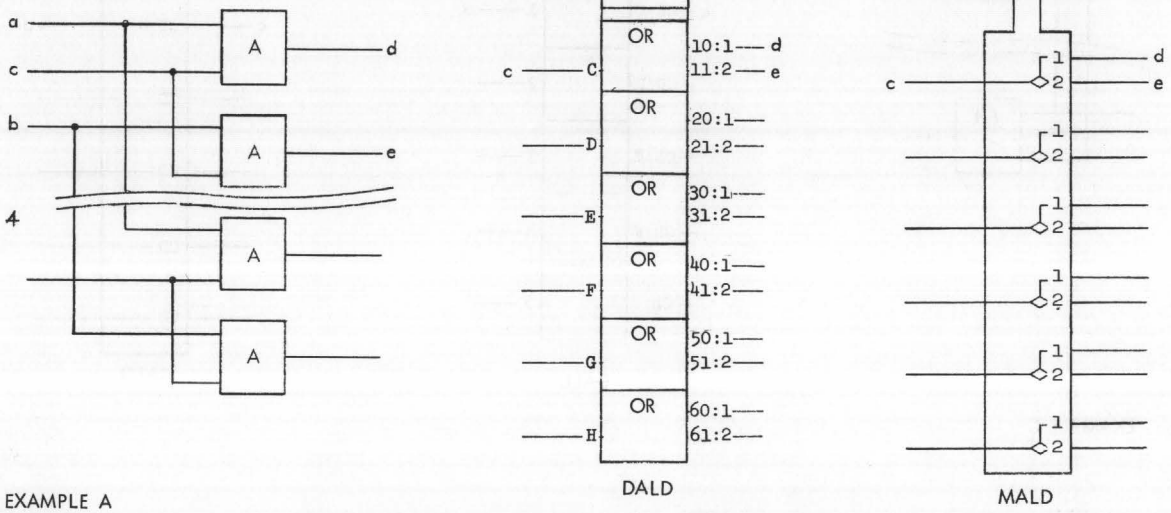


FIGURE 2-24. TYPICAL MALD DOT NOTATION.

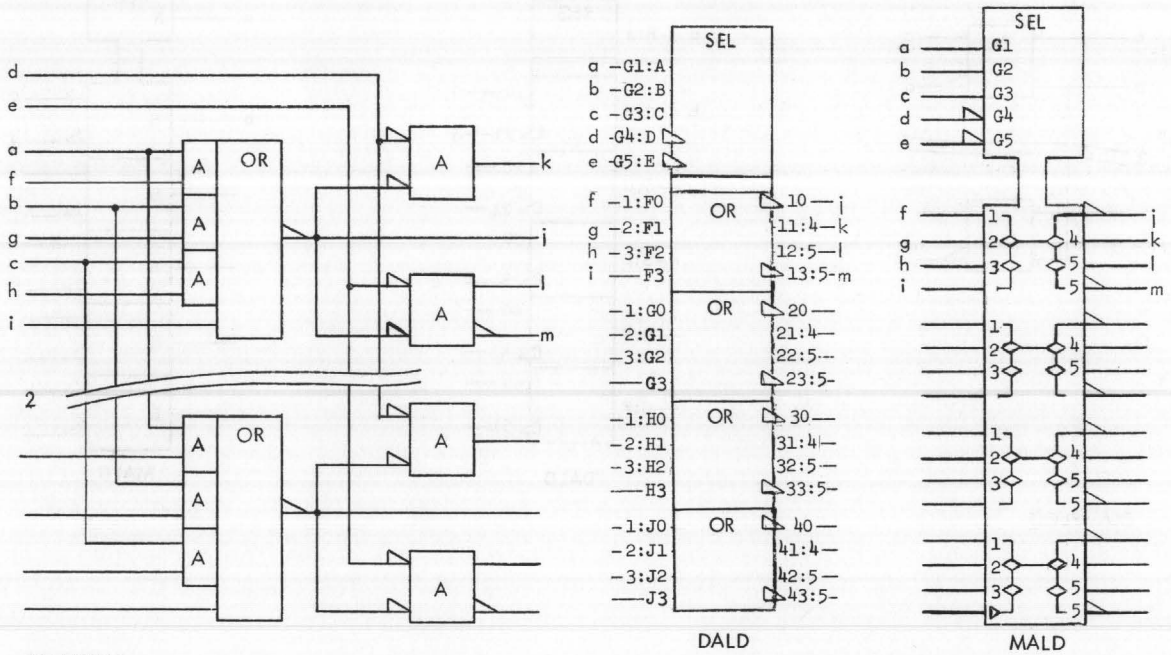
3.1 The following figures are a few examples of functional logic symbols previously defined.



EXAMPLE A

DALD

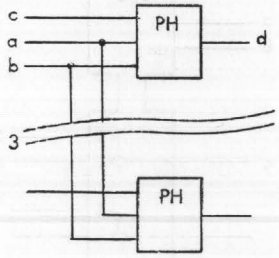
MALD

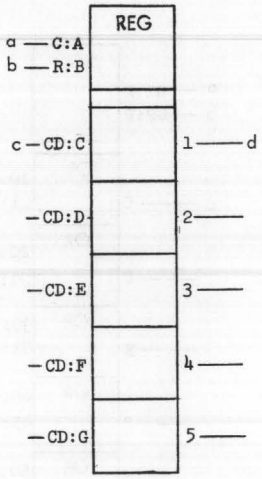


EXAMPLE B

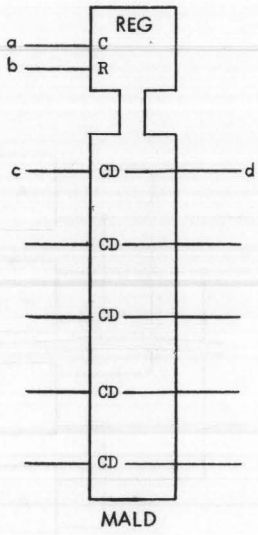
DALD

MALD



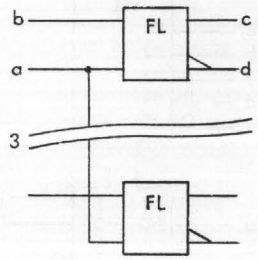


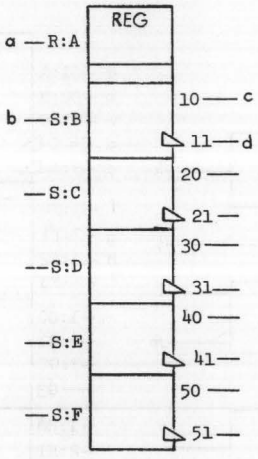
DALD



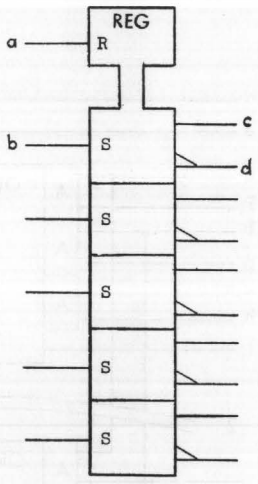
MALD

EXAMPLE C





DALD

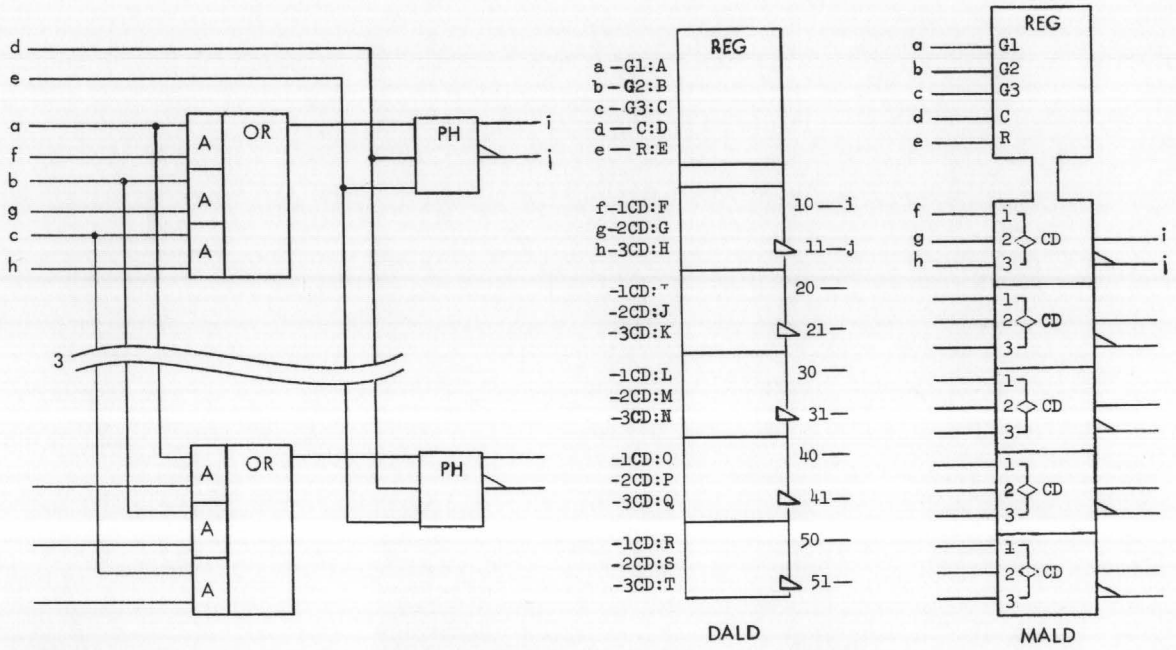


MALD

EXAMPLE D

IBM

Printed in U.S.A.


d
e
a
f
b
g
c
h
A
A
A
OR
PH
i
j
3
A
A
A
OR
PH
REG
a –G1:A
b –G2:B
c –G3:C
d — C:D
e — R:E
f–1CD:F
g–2CD:G
h–3CD:H
10 — i
11 — j
-1CD:
-2CD:J
-3CD:K
20 —
21 —
-1CD:L
-2CD:M
-3CD:N
30 —
31 —
-1CD:O
-2CD:P
-3CD:Q
40 —
41 —
-1CD:R
-2CD:S
-3CD:T
50 —
51 —
DALD
REG
a
b
c
d
e
G1
G2
G3
C
R
f
g
h
1
2
3
CD
i
j
MALD

EXAMPLE E

1.0 INTRODUCTION

This section defines and establishes basic logic block symbols and associated notation used to represent analog circuitry on logic diagrams.

This section defines block symbols and associated notation that represent analog signals and circuitry on logic diagrams. To symbolize all conditions and variations in analog circuitry is not practical, therefore, notes and block titles should be added to diagrams when special or additional information is needed to clarify the functions. The illustrated waveforms are intended to support the definitions given in this section and do not show true electrical characteristics of any circuit. For signal line conditions, positive is indicated by the conventional up direction. Intermixing of digital and analog symbology on the same diagram is permissible.

Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 DEFINITIONS.

2.1 A DIGITAL SIGNAL is a signal that conveys information by any of a limited number of states of that signal where a fixed interpretation is given to each discrete state. A binary signal has two states.

2.2 AN ANALOG SIGNAL is a signal whose amplitude, frequency, phase or other significant parameter can take on any or virtually any value within an operating range and/or period.

3.0 EDGE OF BLOCK CHARACTERS.

3.1 THE INFORMATION CONTENT of an analog signal may be conveyed by many different modes; current, voltage, frequency, compound frequencies, etc. In order that an analog signal may be readily identified, an edge of block character from the following paragraphs shall be used:

3.1.1 U (UP) - An analog signal, voltage or current mode, which is more significant in terms of an ultimate objective when its voltage changes toward the more positive (in the case of voltage mode signal) or as the magnitude of the current increases (in the case of a current mode signal).

3.1.2 D (DOWN) - An analog signal, voltage or current mode, which is more significant in terms of an ultimate objective, when its voltage changes toward the more negative (in the case of a voltage mode signal) or as the magnitude of the current decreases (in the case of a current mode signal).

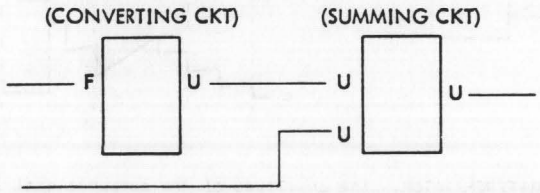
Note 1: Where the information content of an analog signal is conveyed by the duration of a steady state signal, then the U or D shall simply refer to the relative polarity of this signal compared to the no-signal state.

Note 2: Where no specific ultimate significance is applicable, the "U" shall be used.

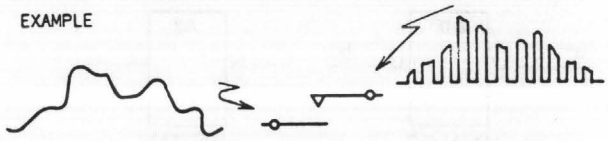
3.1.3 F - Indicates the presence of a signal such as the radio or audio frequency type, in which information is conveyed, not necessarily by the characteristics of one oscillation, but rather by the combined effect of many individual oscillations.

Note: The "F" character is not to be used with analog logic symbols such as SUM, Analog OR, Function Generator and Amplitude Hold. Its use is limited to such symbols as the AND, OR and AR. When a signal is shown in the frequency mode (F) and a parameter of this frequency signal is to be combined with the amplitude(s) of an other signal(s) the frequency mode signal (F) must be converted to a U or D signal.

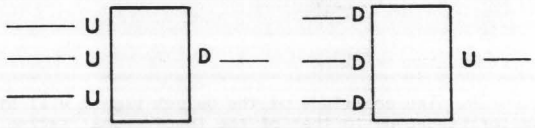
Where more than one frequency mode (F) input signal is to be combined and there is a frequency mode output signal(s), the SPECIAL block symbol shall be used with appropriate block title unless otherwise specified in this standard.



3.1.4 C - Indicates the presence of short duration pulses which have been produced through a sampling technique applied at intervals to an analog signal. Where "C" signals are mixed on a single line, the line shall maintain the "C" coding.



3.1.5 Inversion. The U and D shall be used to denote signal inversion across an analog logic block using these types of signals. This method of showing inversion is not applicable where F and C type signals are indicated.



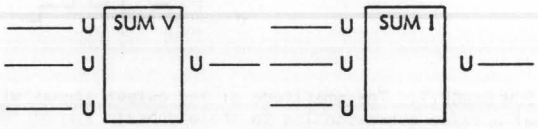
INDICATES INVERSION

3.1.6 Digital edge of block characters when used with analog symbols shall be as specified in CES 0-1046-3.

4.0 SUFFIXES.

4.1 SUFFIXES shall be used in conjunction with an analog logic function to define the characteristics of the output analog signal if they add to the clarity of the block.

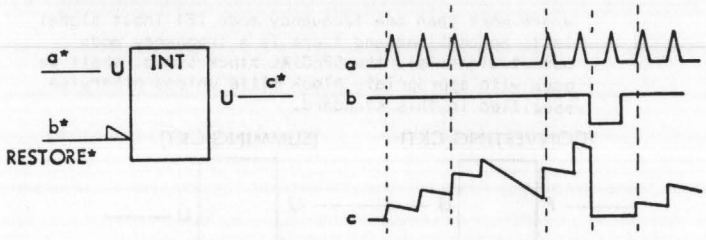
EXAMPLES: I - Current
V - Voltage
Other - Refer to CES 0-1046-3.



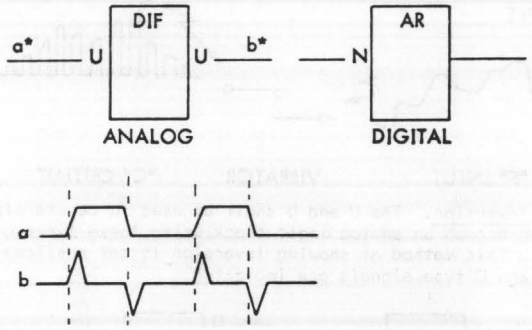
5.0 ANALOG BLOCK AND FUNCTION SYMBOL DEFINITIONS.

5.1 INTEGRATOR. The amplitude of the output signal is a time integral of the amplitude of the input signal. A signal of indicated polarity applied to the restore input, if required, will cause the output amplitude to assume its no-signal level.

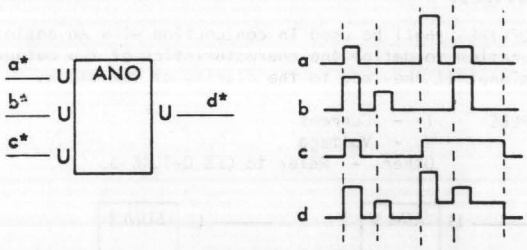
The restore signal is or shall be treated as a binary signal. When, at a later point in time, the restore signal is caused to return to its original polarity, a new period of integration will be initiated. If there is a restore line, it shall be placed towards the bottom of the block.



5.2 DIFFERENTIATOR. The amplitude of the output signal is a function of the time rate of change of a signal applied at the input. In digital logic, the effect of differentiation shall be shown through the use of the letters P or N at the input of the logic block as provided for in CES 0-1046-3.



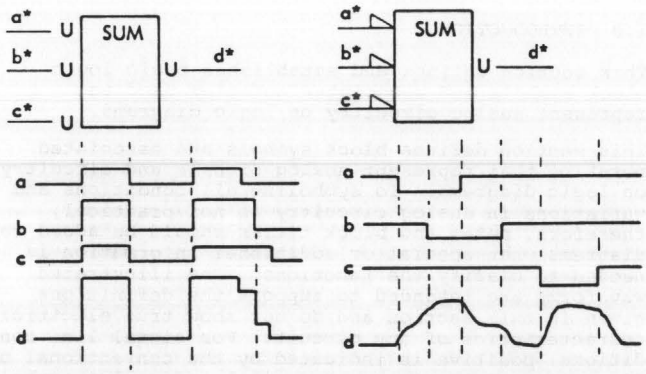
5.3 ANALOG OR. The amplitude of the output signal will stand at a value corresponding to that of the input signal having the greatest amplitude in the direction shown by the line input edge of block character, which must be the same for all inputs. The inputs must be in the same signal mode as the output. The output mode may be indicated by the suffix, I or V (see Paragraph 4.1).



5.4 SUM CIRCUIT. The amplitude of the output signal will stand at a value corresponding to the algebraic sum of the (weighted) values of the input signals. The output shall be an analog signal with the appropriate edge of block character (U or D) shown.

Note: A signal input edge of block character indicates the direction of change that will cause the output to change in its indicated direction.

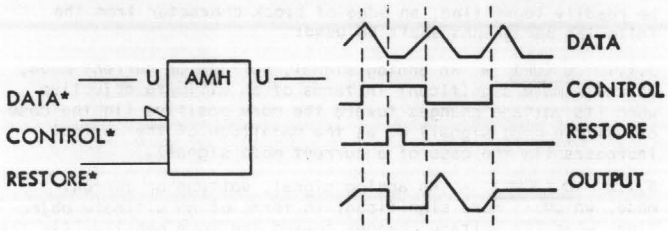
* NOT PART OF SYMBOL



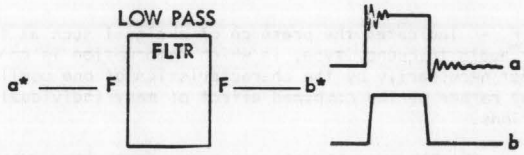
5.5 AMPLITUDE HOLD. Upon application of a signal of indicated polarity at the control input, the output signal will assume an amplitude corresponding to that which is appearing at the data input. When, subsequently, the control signal is caused to assume the polarity opposite to that indicated, the output signal will hold at whatever amplitude it possesses at that moment.

The AMH symbol need not have a restore input. If it is supplied with one, then the polarity indicated on the symbol shall be that which will cause the output to assume its no-signal level.

The control and restore signals are, or shall be, treated as binary signals. The output line shall be placed towards the top of the block. The data line shall be placed opposite the output line. The control line shall be centered upon the input side of the block. The restore line shall be placed towards the bottom of the block.

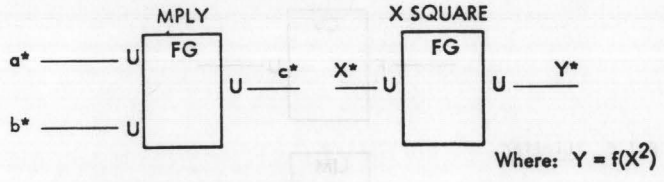


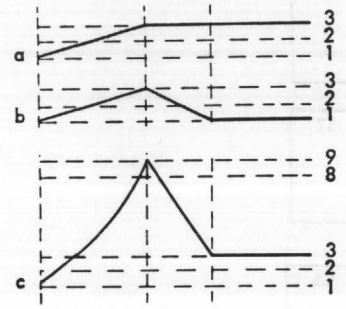
5.6 FILTER. The output signal will correspond to that applied at the input except for amplitude variations resulting from the frequency response characteristics of the FILTER. Where bandpass action (wide or narrow) is accompanied by amplification, this may be shown through use of the AR symbol with appropriate block title. It is recommended that the type of filtering action be shown in the block title information, for example: LOW PASS, HIGH PASS, etc.



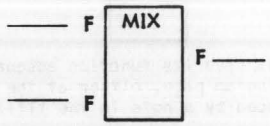
5.7 FUNCTION GENERATOR. This symbol may be used for devices having one or more signal inputs. It shall not be used where another symbol or combination of symbols defined in this standard (analog or binary) can be used to describe the intended function.

The amplitude of the output signal will assume a value which is a particular mathematical function of the value of the input signals. Inputs and outputs shall be treated as analog signals (U or D). It is recommended that the mathematical operation be shown in the block title area; for example, MPLY, DIV, X SQUARED, X CUBED, etc.

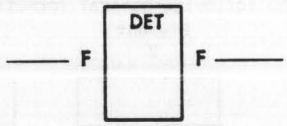




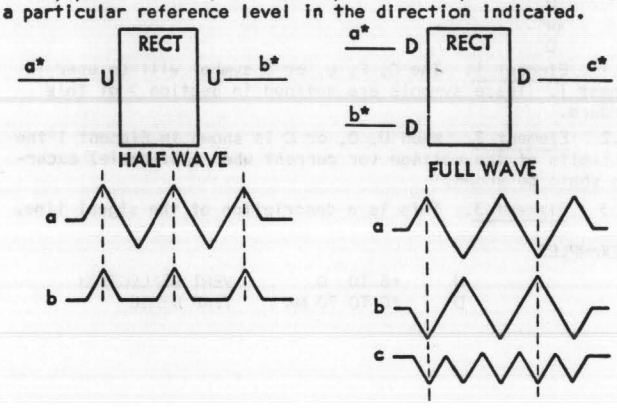
5.8 MIXER. The mixer is restricted to use with two inputs, each of which is an F type signal. The output is an F type signal which contains sum and difference frequencies of the two inputs, intentionally produced through non linear action in the device. If filtering is included in the circuit, then the output frequency should be indicated in the block title.



5.9 DETECTOR. The dectector is a device which acts upon F type signals to recover a carried signal of lower frequency, often an audio signal.

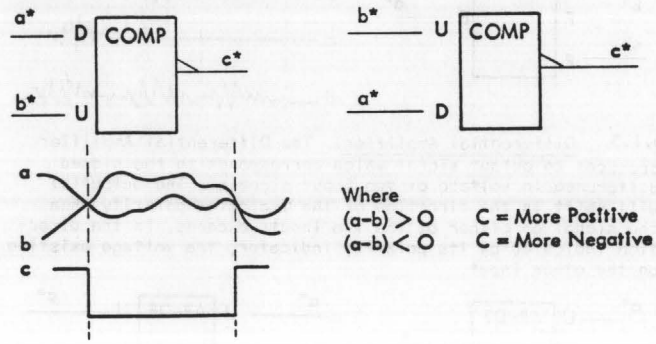


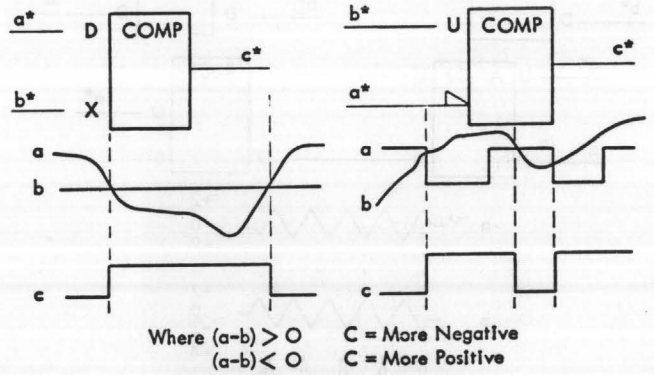
5.10 RECTIFIER. The amplitude of the output corresponds, at any point in time, to that input whose amplitude exceeds a particular reference level in the direction indicated.



* NOT PART OF SYMBOL

5.11 COMPARATOR. The output of the comparator assumes its indicated polarity when and only when the signal on either of the two inputs reaches or exceeds, in the direction indicated by the U or D indicator, the voltage existing on the other input. The output signal of the comparator is essentially two-valued, the period of transition between the two states being purposely made as brief as possible by the characteristics of the device.



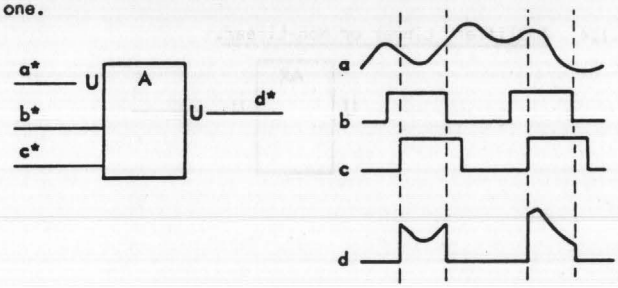


VARIATIONS OF THE COMPARATOR

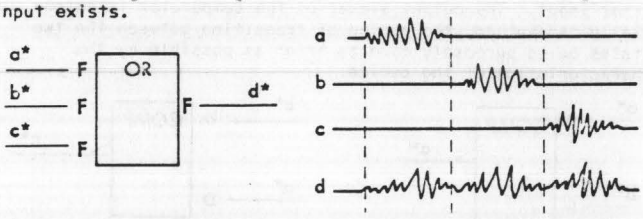
6.0 DIGITAL AND/OR ANALOG BLOCKS AND FUNCTION SYMBOL DEFINITIONS.

6.1 DIGITAL AND ANALOG LOGIC FUNCTIONS. The following symbols are from the basic set of digital logic functions described in CES 0-1046-3 that are also applicable in diagraming analog logic. Their original definitions are maintained. Restrictions for their use with analog signals are specified where applicable.

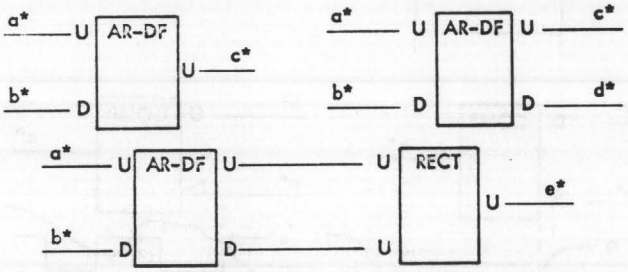
6.1.1 AND, when used with an analog input. The output signal will correspond to the input signal applied to the analog input when and only when all digital inputs stand at their indicated polarities. At other times, the output will assume its no signal value. The number of analog inputs is restricted to one.

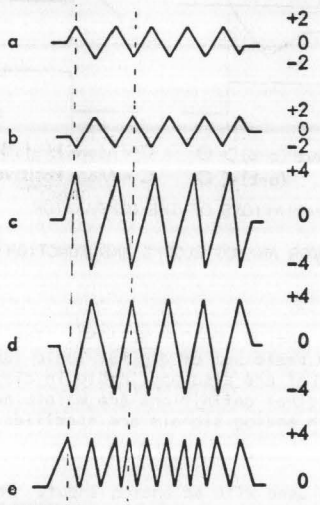


6.1.2 OR, when used with analog inputs. The output signal will correspond to that of the particular analog input signal being applied at the time. It is assumed that the output will not be meaningful during such time that more than one signal input exists.



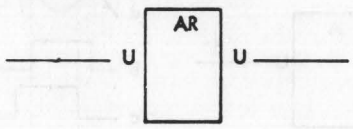
6.1.3 Differential Amplifier. The Differential Amplifier produces an output signal which corresponds to the signed difference in voltage of two input signals. The output(s) will shift in the direction of the indicated polarity when the signal on either of the two inputs exceeds, in the direction indicated by its polarity indicator, the voltage existing on the other input.



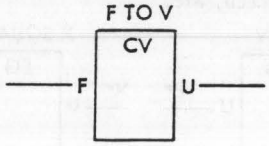


* NOT PART OF SYMBOL

6.1.4 Amplifier, Linear or Non-Linear.



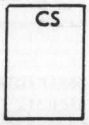
6.1.5 Signal Mode Converter. When used with analog signals, this shall be a single input device where the signal mode is converted or translated. An example would be a circuit which changes frequency variations to amplitude variations. It is recommended that the type of conversion performed be shown in the title area.



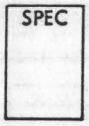
6.1.6 Limiter.

6.1.7 Schmitt Trigger.

6.1.8 Series Current Switch.



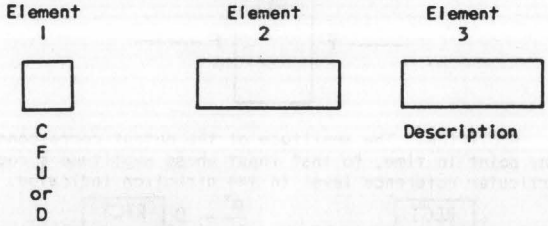
6.1.9 Special.



A Special block shall have its function adequately described by wording on the diagram page, either at the block or in a comment area referenced by a note in the titling area of the block.

7.0 LINE TITLES.

7.1 GENERAL FORMAT FOR ALL LINES ENTERING OR LEAVING A DIAGRAM PAGE. All lines which enter or leave a diagram page shall conform to the following general format:



7.1.1 Element 1. The C, F, U, or D symbol will be used in Element 1. These symbols are defined in Section 3 of this standard.

7.1.2 Element 2. When U, D, or C is shown in Element 1 the two limits of the voltage (or current when applicable) excursion shall be shown.

7.1.3 Element 3. This is a description of the signal line.

EXAMPLES

U	+6 TO 0	VERT DEFLECTION
D	40 TO 70 MA	TEMP SENSE

1.0 INTRODUCTION

This section defines documentation necessary to design, manufacture and maintain the electrical portion of IBM product power systems.

Instructions given in this section are not mandatory: no deviation procedures are established.

2.0 REQUIREMENTS

2.1 GENERAL.

The documents described in the following paragraphs must adhere to all drafting requirements. In addition, in the Drafting Manual, CES 0-1001-000, Section S, Paragraph 2 shall be used for schematic representation and Paragraph 1 shall apply to component letter designations when geographic location coding is not used.

These documents deal primarily with power system representation, nowever where applicable they may be used to show power second order products, for example, power supplies, where these products are supported by their own documentation.

2.1.1 Types of Documents.

2.1.1.1 Logic Schematic.

A drawing that shows the electrical system by use of electrical and electronic symbols. These symbols are arranged on the drawing to show the functioning of the electrical system. This drawing is intended for the Machine Wiring Diagram Manual (ALD).

2.1.1.2 Wiring Diagram.

A drawing that shows the electrical system by use of electrical and electronic symbols. These symbols are arranged on the drawing to show the physical point to point wiring. This diagram is optional if not required for manufacturing or Product Engineering. If generated, it may be retained for Engineering control, it is NOT intended for the Machine Wiring Diagram Manual (ALD).

2.1.1.3 Timing Chart.

A drawing which graphically shows the sequence of operation(s) of the system. When provided this drawing is intended for the Machine Wiring Diagram Manual (ALD).

2.2 LOGIC SCHEMATIC RULES. (See Figure 4-1.)

(a) Single line representation shall be used. This means that point-to-point wiring is not normally shown, however, all physical terminals shall be shown and labeled with their location nomenclature, and wherever practicable descriptive information, i.e. EPO, DC interlock, etc.

(b) Source and control voltage lines should be across the top with vertical lines leading down through controlling contacts to the electrical entity or signal output which cumulates a required functional step. These should be shown at the bottom, from left to right in the order they are energized during power on. This will result in all control coils, lights, power supplies and external signals being represented at the bottom of the drawing.

An acceptable variation of this rule exists if contacts are placed on both lines of a relay coil, lamp, etc. Devices controlled in this manner often require several sets of series or parallel contacts. In these applications, the contacts may be shown horizontally and the device need not be shown at the bottom of the page.

(c) All lettering on the diagrams should be readable from the bottom or right of the drawing. Inputs should be from the left or top and outputs at the right or bottom.

(d) Multi-section components such as relays, section switches, etc., snould have their operating sections depicted separately as required to show their system function. These portions should not normally be duplicated on the drawing(s). However, if it is necessary to show the armature of a switch or relay twice (normally closed and normally open separately) then this condition shall be indicated by a drawing note.

(e) There should be a minimum of crossover lines.

(f) Power supplies or other power assemblies that are supported by their own maintenance documentation may be shown as a block.

(g) The electrical and electronic symbols should be spaced on the drawing in a manner that will provide optimum white space to clearly delineate each function and to provide room for expansion or change.

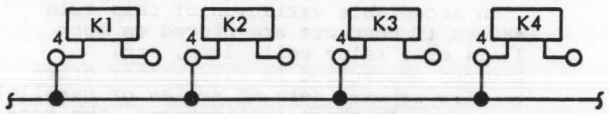
(h) The Logic Schematic is intended as a Machine Wiring Diagram Manual (ALD) document. It shall therefore conform to the proper page size (see Drafting Manual, Section E, Paragraph 3) and be assigned a logic page number per page.

(j) Power Systems Interface pages are a requirement any time there are lines leaving the machine, lines leaving or entering the power system of a given machine type, from or to another type numbered machine shall use the interface page system described in CES 0-1046-012. The interface pages shall be numbered according to CES 0-1046-009.

(k) 50Hz machine diagrams should show by convention or by the addition of notes and/or reference pages the following when applicable:

a. Special Wiring
b. Treatment of neutral wires
c. Alternate connections at terminal boards, transformers, etc.

(l) Critical Wiring. If any wiring sequence is a requirement for operation, i.e. critical wire length, then the particular point to point wiring shall be noted on the logic schematic and a wire sequence specified.



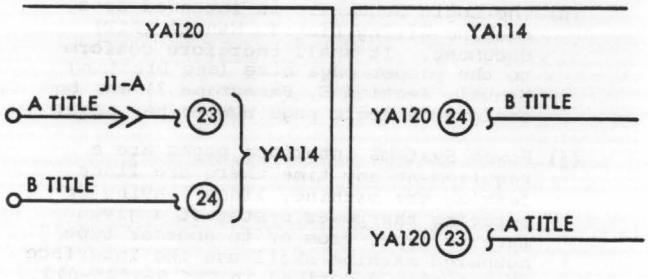
NOTE CRITICAL WIRING

FROM	TO	LENGTH
K2-4	K4-4	4.00 INCH (101, 6)
K4-4	K1-4	5.50 INCH (139, 7)
K1-4	K3-4	2.75 INCH (69, 85)

(m) Off Sheet Lines: All lines entering or leaving the Logic schematic should contain the following:

1. A .25 inch break symbol.
2. A line title, the same title should be used on all interconnecting lines.
3. A circled numeral. A unique number should be used for all interconnecting lines. The circle should be .5 inch (12,7) when three digits are required, and .375 (9,5) when less than three. When the off sheet line, source or sink, is a logic block on an ALD, the logic net number is used in place of the circled numeral.
4. Logic page number of the to or from page. A logic number may bracket several lines.

EXAMPLE:



2.3 TIMING CHART RULES (See Figure 4-2.)

(a) Timing Charts are optional, however, serious consideration should be given to supplying them to the field. The following are some of the sequences that should be considered for timing charts:

a. Power on
b. Power off
c. Thermal Faults
d. Power Supply Faults
e. EPO Faults
f. And combination of the above

(b) Time runs from left to right.

(c) Components energized and signals are represented by horizontal bars. The bars indicate the active state of the component or signal.

(d) Components shall be identified by location and name. Signal lines should show signal level or polarity and line name for the active state.

(e) Component or signal line location should be indicated by logic page number.

(f) An arbitrary sequence number or letter should be assigned to each component or signal line on the chart. Such a number or letter should be shown at the beginning and end of each horizontal bar and the number or letter should indicate what component or signal initiated the action causing the change of state.

(g) Only components and signals which are significant to the sequence should be shown in the chart.

(h) Pick and drop times of relays are not normally shown. When necessary, these or other component reaction times, may be shown as a shaded portion of the horizontal bar.

(j) Important time intervals or sequence check points may be indicated along the bottom of the chart.

(k) Bars with break symbols at both ends represent an item that is continuously energized for that sequence.

2.4 WIRING DIAGRAM RULES: When required: (See Figure 4-3.)

(a) All electrical and electronic symbols making up one component, (i.e. a relay) should remain together on the drawing.

(b) Locate all components for the easiest layout of point to point wiring, keeping crossover lines to a minimum. Allow space for unused sets of relay contacts or spare components.

(c) All lettering on the diagram should be readable from the bottom or right of the drawing. Inputs will enter the left side or top and output lines will leave the right side or bottom except for return and ground lines.

(d) This diagram is not intended for the Machine Wiring Diagram Manual (ALD) and therefore, may be on E size sheet or multiple E size sheets as necessary.

2.5 ADDITIONAL REFERENCE DOCUMENTS.

Serious consideration should be given to supplying to the field a component index and a reference drawing showing physical component layout. These drawings simplify locating components in the equipment and locating various parts of the component on the logic schematic.

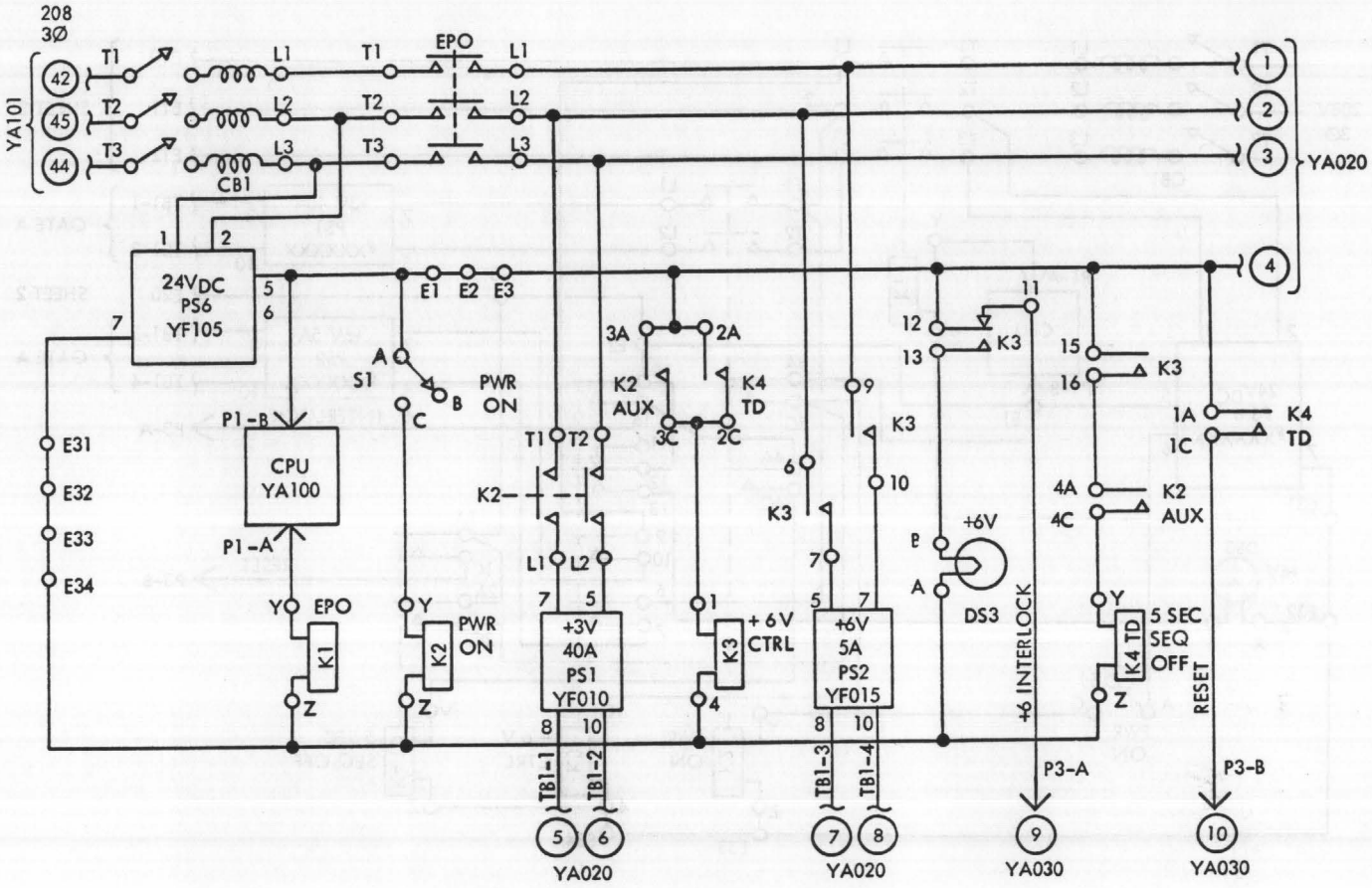


FIGURE 4-1. LOGIC SCHEMATIC, POWER SYSTEM

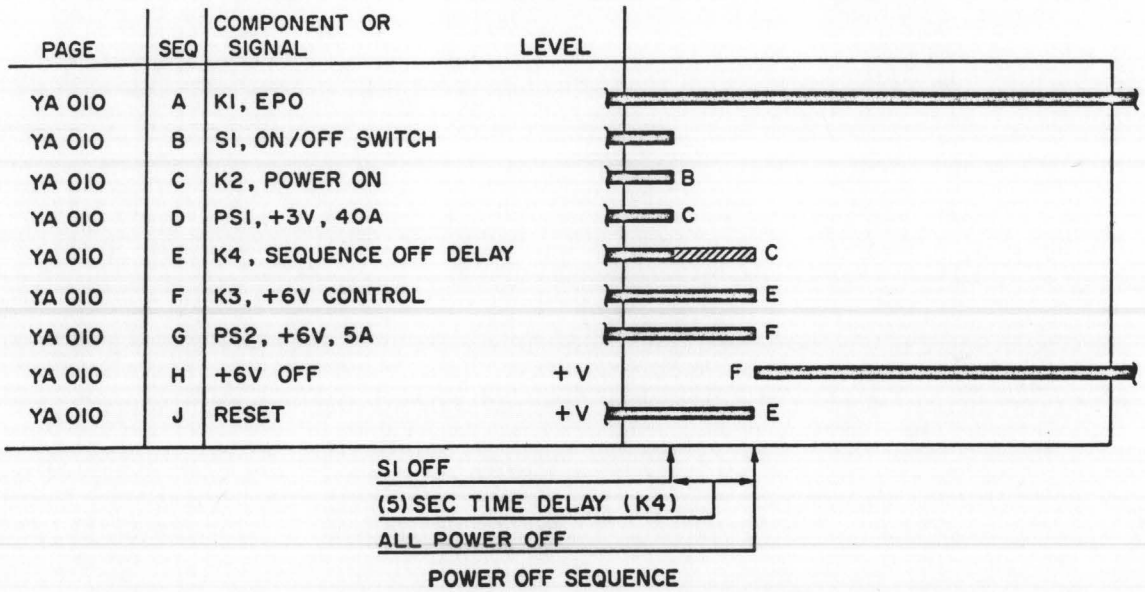


FIGURE 4-2. TIMING CHART, POWER SYSTEM

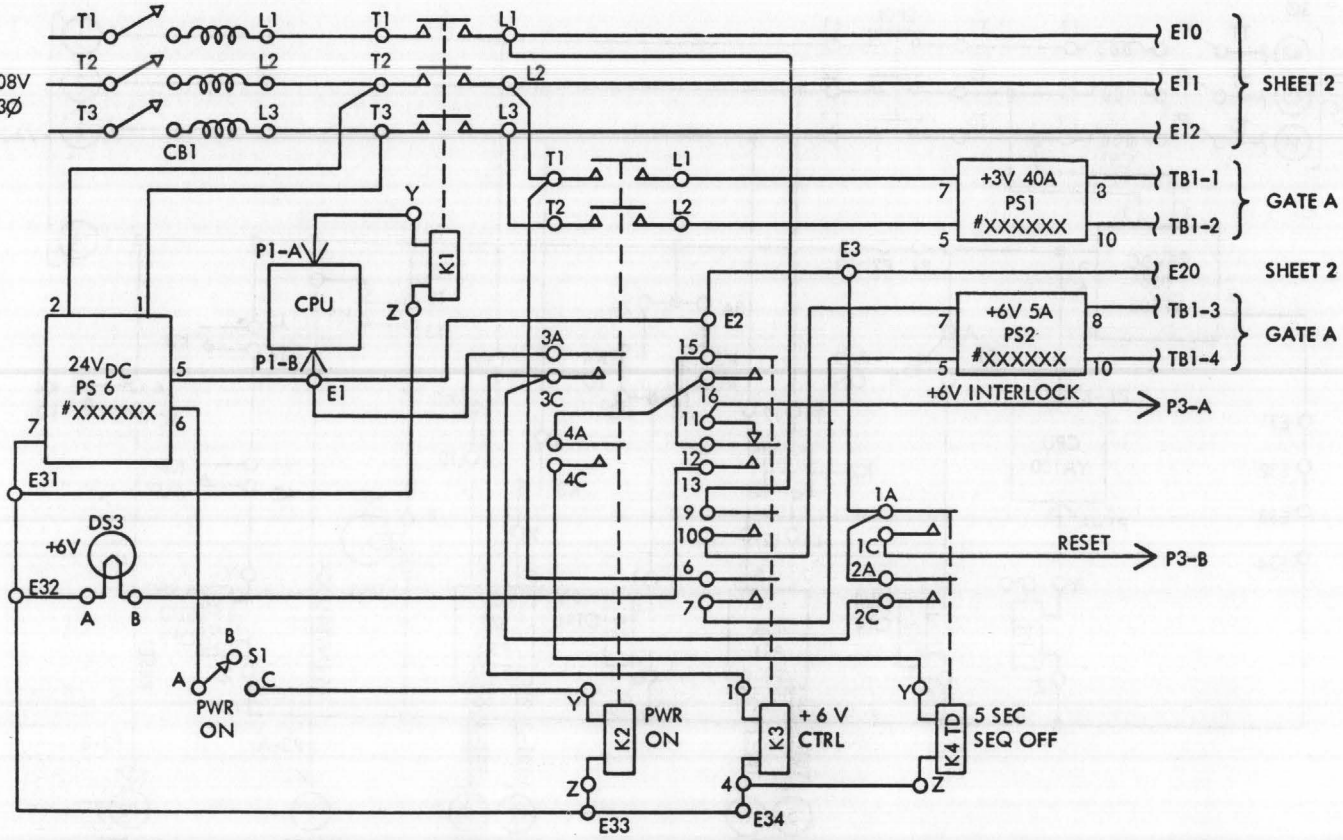


FIGURE 4-3. WIRING DIAGRAM, POWER SYSTEM

1.0 INTRODUCTION

This section defines the micro-language page format to promote uniformity in released CAS logic diagrams. This information is related to that given in DEP 0-1046-018 (SDD).

Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 CAS LOGIC DIAGRAMS (CLD's)

2.1 The CLD's (see Figure 5-1) shall be prepared as explained in paragraphs 2.0 through 5.0.

2.2 LOGIC BLOCKS. Each Read Only Storage (ROS) micro instruction shall be represented by a block on the CLD. Each block must contain the following information:

(a) Actual ROS address - This is the address that would appear in a ROS address register if displayed. (See A, Figure 5-1.) This must be indicated by 3 (4 if desired) hexadecimal characters.

(b) Leg Identifier is from 0 to 6 characters right adjusted. This is a representation of the bits of the READ ONLY STORAGE Address Register which are controlled by branch conditions in the preceding block or blocks. The position of each character in the leg identifier corresponds to a certain bit in the ROS address. The only permissible characters are 0 (zero) or 1 or X. X represents either a 1 or 0 but is not developed as a result of a branch condition. (See B, Figure 5-1.) Leading X's may be replaced with blanks.

(c) The coordinate of the block is row column at lower left corner of box (see C, Figure 5-1).

(d) Leg selector is from 0 to 6 characters, right adjusted. This is a representation of the bits of the ROS address which are controlled by branch conditions in that block. The position of each character in the leg selector corresponds to a specific bit in the next ROS address. (The positioning of characters must correspond to the positioning in the leg identifier.) The only permissible characters are 0 or 1 or X or *. X represents either a 1 or 0 but is not developed as a result of a branch condition. * denotes a bit position whose value (0 or 1) shall be determined by a branch condition (see D, Figure 5-1).

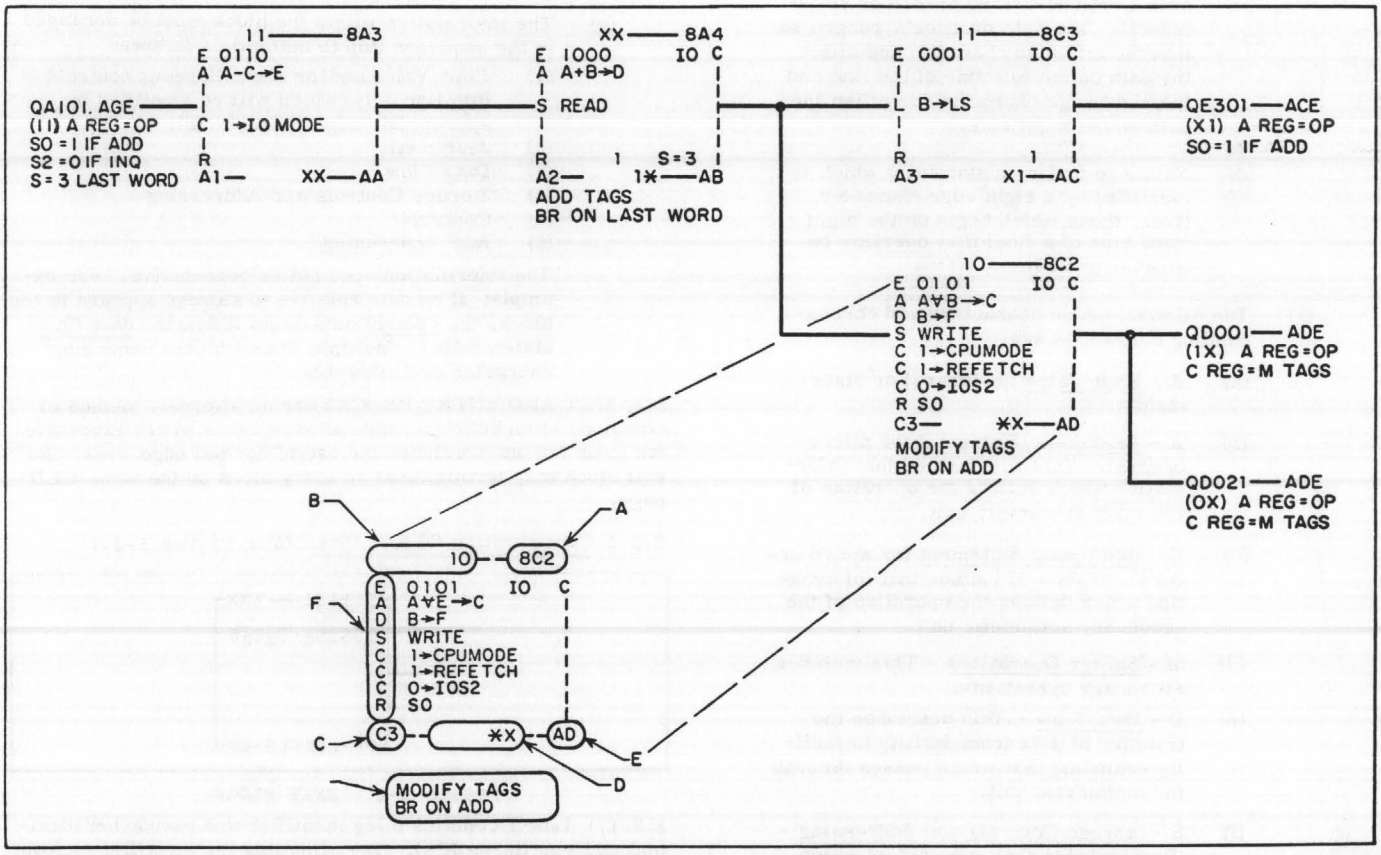


FIGURE 5-1. CAS LOGIC DIAGRAM

(e) The serial number of the block is two alphabetic characters located at the lower right-hand corner (see E, Figure 5-1).

(f) Identification of information within the block. (See F, Figure 5-1.) This is defined by printing in the appropriate edge of the block an alphabetic character which defines the function of the micro orders or statements on that line or a portion of that line.

(1) Edge characters may appear in either the left or the left and right edge (s) of the block. The following rules must be maintained in any case;

(a) A blank space must be provided between the micro orders or statements on that line and the edge character (s).

(b) A line of data that can be identified by a single edge character must always be identified by the left edge character only and no right edge character shall appear.

(c) A line of data that requires the use of different left and right edge characters must partition that data by one or more blank spaces and must contain 2 and only 2 entries (micro orders or statements). The data must be arranged so that the left edge character identifies the data on the left side of the line and the right edge character identifies the data on the right side.

(d) No micro order or statement which is identified by a right edge character (i.e., those which begin on the right hand side of a line) may overflow to another print line.

(2) The allowable edge characters and corresponding definitions are:

(a) E - Emit Value (in Binary) or Statement.

(b) A - Arithmetic Statement (or micro orders). This will include that information which defines the operation of the main arithmetic unit.

(c) B - Arithmetic Statement (or micro orders). This will include that information which defines the operation of the secondary arithmetic unit.

(d) M - Shifter Operations - This includes all shifter operations.

(e) D - Data Flow - This describes the transfer of data from facility to facility excluding that which passes through the arithmetic unit.

(f) S - Storage Controls and Addressing - This includes that information which defines the operation of all storages (excluding ROS) in terms of read, write, etc., and data flow to the storage address register (s). (The data flow to or from the storage data register must be described within the data flow statement or arithmetic area of the block).

(f1) When a line is used specifically to describe local storage, the alphabetic character L must be used.
L - This includes that information which defines the operation of local storage in terms of Read, Write, and Addressing.

(g) C - Control, Miscellaneous - This describes those miscellaneous controls and tests which are not described within the other sections of the block.

(h) R - ROS Addressing - This information describes the data flow to the ROS Address Register and those tests performed which determine the next address to be executed. The branch test micro orders must be presented in a right to left, bottom to top sequence starting with the micro order that determines the lowest order bit on the right side of the lowest print line within the CLD block.

(g) The information within the block must be arranged in the sequence (top to bottom) as follows:

(1) Emit Value and/or miscellaneous controls (top line only) which will be identified by the appropriate edge character(s).
(2) Arithmetic
(3) Data Flow
(4) Storage Controls and Addressing
(5) Controls
(6) ROS Addressing

The information need not be consecutive. For example: if no data relative to storage appears in the block, the control data could follow the data flow statement(s). Multiple lines with the same edge character are allowable.

2.3 EXIT AND ENTRY BLOCKS are an alternate method of communication between pages used in cases where excessive fan in or fan out precludes the use of normal edge lines. No exit block may terminate at an entry block on the same CLD page.

2.3.1 Configuration Of Exit Block (See Figure 5-2.)

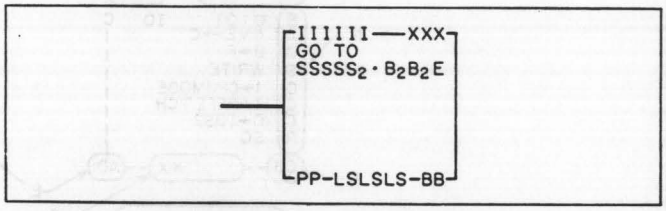


FIGURE 5-2. EXIT BLOCK

2.3.1.1 Line 1 contains a leg identifier and pseudo hexadecimal address (three X's). The allowable leg identifier is from 0 to 6 characters, right adjusted. This is a representation of the bits of the ROS address which are controlled by branch conditions in the previous block. The position of each char-

acter in the leg identifier corresponds to a specific bit in the next ROS address. The only permissible characters are 0 or 1 or X or *. X represents either a 1 or 0 but is not developed as a result of a branch condition. * denotes a bit position whose value (0 or 1) shall be determined by a branch condition.

2.3.1.2 Line 2 contains phrase "GO TO", left adjusted. (1 blank space between GO and TO.)

2.3.1.3 Line 3 contains page number and block serial number and line position of the entry block to which the exit goes.

2.3.1.4 Lines 4 through 7 are blank.

2.3.1.5 Line 8 contains print coordinate (left edge), leg selector (identical to the leg identifier of that block), and block serial number (right edge).

2.3.2 Spacing. A minimum of two block positions must be void of boxes to the right of all exit blocks unless the page boundary intervenes.

2.3.3 Configuration Of Entry Block (See Figure 5-3.)

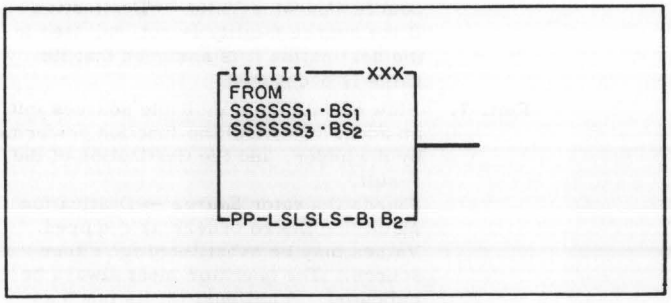


FIGURE 5-3. ENTRY BLOCK

2.3.3.1 Line 1 contains a leg identifier and pseudo hexadecimal address (three X's). The allowable leg identifier is from 0 to 6 characters, right adjusted. This is a representation of the bits of the ROS address which are controlled by branch conditions in the previous block. The position of each character in the leg identifier corresponds to a specific bit in the next ROS address. The only permissible characters are 0 or 1 or X or *. X represents either a 1 or 0 but is not developed as a result of a branch condition. * denotes a bit position whose value (0 or 1) shall be determined by a branch condition.

2.3.3.2 Line 2 contains the word "FROM", left adjusted.

2.3.3.3 Line 3 contains page number, period and block serial number from which the entry came.

2.3.3.4 Lines 4 through 17 may contain additional page and block serial numbers.

2.3.3.5 The last line of the block contains print coordinate (left edge), leg selector (identical to the leg identifier of that block), and block serial number (right edge).

2.3.4 Spacing. All columns to the left of the right most entry block shall be devoid of logic blocks.

3.0 LANGUAGE

3.1 STANDARD LANGUAGE. It is essential that all information on the CLD must utilize a standardized language insofar as structure, abbreviations, the use and definition of symbols, and notation conventions are concerned.

3.2 SPECIAL CHARACTER DEFINITIONS. The allowable special characters and corresponding definitions are:

	Symbol	Definition
(a)	+	True add/Positive Ex: "A+B", B is added (true) to A
(b)	-	Complement add/subtract, negative Ex: "A - B", B is complement added to A
(c)	=	Is equal Ex: "A = B", A is equal to B
(d)	≠	Is unequal Ex: "A ≠ B", A is unequal to B
(e)	→	Is set into Ex: "A→B", A is set into B (destructive read - in is implied)
(f)	•	Is "Anded" with (logical) Ex: "A • B", A is "Anded" with B
(g)	,	And (non - logical) Ex: "A→B, C", A is set into B and C
(h)	?	Indeterminate function (this describes a function which is hardware controlled rather than under the direct control of the micro-program.) Ex: "A ? B→C", A and B are logically combined (under hardware control) and the result is set into C.
(i)	*	Special. Each user (machine group) may assign any one definition they choose. However, it may not be used to indicate any function covered by an already defined symbol, it must be assigned only one definition per page, and it must have an accompanying explanatory note at the bottom of each page on which it is used if it is used to describe more than one function on that machine.
(j)	∀	Is "Exclusive Ored" with Ex: "A ∀ B→C", A is "Exclusive Ored" with B and the result is set into C
(k)	Ω	Is "Ored" with Ex: "A Ω B→C", A is "Ored" with B and the result is set into C
(l)	/	Or Ex: "A / B→C", A or B is set into C
(m)	±	True or complement add/positive or negative Ex: "A ± B→C", B is true or complement added to A and the result is set into C

(n) < Is less than
Ex: "A < B", A is less than B

(o) ¬ Not (boolean - used as the not function on CLD's)

(p) : Is compared to
Ex: "A : B", A is compared to B

(q) (The parentheses are used only for normal English punctuation or to enclose an expression within a statement.

(r))

NOTE. Symbols may be used in combinations provided that their individual definitions are maintained.

3.3 IDENTIFICATION OF FACILITIES. Facilities must be described by one or more alphabetic characters. The number of characters must be held to a minimum to facilitate the usage of statements within the CLD logic block. If excessively long names are used the statements become too long and lose their effectiveness.

3.3.1 Definition of a Facility. A facility is an ordered set of binary bits (or bit) which has:

(a) A name
(b) A length equal to the number of bits in the set
(c) A value which is maintained until changed

A subset of a facility may also be defined as a facility.

3.4 IDENTIFICATION OF PORTIONS OF FACILITIES. Portions shall be identified by one or more numeric characters.

3.4.1 Definition of a Portion. A portion of a facility is that part which is serviced by a complete data path. (Portions will be assigned independently for input and output data paths).

For example: if a data path exists for positions 1 through 4 of an 8 position register to read out, then that data path (positions) must be referred to as a specific portion of that register.

For example:

The statement "D3→E" describes the transfer of portion 3 of the D Register (positions 5 thru 11) to the E Register.

No portion shall be assigned to the total facility, only to parts thereof.

3.4.1.1 Specific Bit Positions are also identified by numerical characters. They should be enclosed within parenthesis when described in order to distinguish them from portions. If a specific bit position is assigned a portion number then it must be referred to by that portion number and the parenthesis not used. It is preferable to assign 2 or more numeric characters when describing bit positions.

3.5 FORMAT OF STATEMENTS AND MICRO ORDERS.

3.5.1 Applicability of Formats. Statements are preferable to individual micro orders and shall be used whenever feasible. When micro orders are described individually they utilize the same symbols, abbreviations, and format as statements. Mnemonics may be used only when space within the CLD block prohibits the use of statements or the existing symbols and abbreviations are inadequate to describe the operation.

3.5.2 Available Formats. The following formats (fmt) must be used for statements and micro orders:

(a) For action-denoting statements

Fmt. 1. Transfer of data from facility to facility
Source →Destination

Fmt. 2. Setting a facility to a specific value or state
Value →Destination

Fmt. 3. Prevent change to the state of or value in a facility
Source ¬ Destination

Fmt. 4. Increment, Decrement, or mask the value in a facility.
Source Operator Value
Destination is assumed to be same as source.

Fmt. 5. Increment, Decrement, or mask the value in a facility then transfer that value to another facility.
(Source Operator Value) →Destination

Fmt. 6. Transfer data through an incrementer or decrementer to another facility.
Source Operator Value →Destination
If the source facility is not indicated in the destination it is assumed that its value is unchanged.

Fmt. 7. Flow of data from multiple sources into an adder (Or ALU) the function performed by the adder, and the destination of the result.
Source Operator Source →Destination
Modifying micro orders as required. Values may be substituted for either source. The operator must always be indicated. Additional inputs (such as forced carries) may be indicated as additional sources with appropriate operator prefixes.

Source and destination are always defined by facility (and portion if appropriate). (See 3.3 and 3.4). Operators are indicated by special symbols (See 3.2). Values are indicated by numeric characters (decimal) except lines identified by edge char E. In all cases the source shall be stated first (left side of statement) and the destination last (right side). Multiple sources and destinations are allowable.

NOTE. The "ON" state of a bit must be indicated as its 1 (one) state. The "OFF" state must be indicated as its 0 (zero) state.

(b) For decision-type statements - All branch tests must be described utilizing one of the following formats.

Fmt. 1. Comparison of values or states of 2 or more facilities.
Facility Operator Facility

Fmt. 2. Test for specific value or state of a facility.
Facility Operator Value

Fmt. 3. Test for the "ON" state of a one bit facility.
Facility

CLD branch tests must be described by indicating the condition which if satisfied will cause or allow the setting of a binary one in the appropriate bit of the next ROS address.

4.0 CLD COMMENTS

4.1 COMMENTS ASSOCIATED WITH A CLD BLOCK (See F, Fig. 5-1). The objective of those comments associated with a particular block are:

(a) To clarify the information within the block. To accomplish this, it is necessary to predetermine which micro orders will require clarification and generate a "standard" comment for each. Then, whenever one is utilized, the corresponding comment must be placed below that block. However, when space is prohibitive or the information is repetitive, this information may be placed within the page comments.

(b) To clarify the reason those functions are performed during that micro instruction. Since the information within the block describes the functions performed in terms of facilities, control, lines, etc., it is necessary to equate these to the instruction(s) being performed. For example: a block may indicate that the B register contents are written in local store.

In terms of the instruction or subroutine being performed, it should be noted that the B register contained the exponent of the floating point divisor and this operation was performed to store the exponent for later use in the micro program. In that case, an appropriate comment might be "store divisor exponent." When space is prohibitive, this information may be presented within the page comments.

4.2 PAGE COMMENTS. These comments must describe the overall objectives of the blocks upon that page in terms of the instruction(s) or subroutines being performed. This information should be similar to that described in Paragraph 4.1 (b) and generally should be presented across the top of the CLD page.

5.0 PAGE ENTRY AND EXIT LINES

5.1 PAGE ENTRY INFORMATION. The following data must be supplied for each entry onto a CLD page:

(a) Line 1 contains the number of the page from which the entry came, followed by a period, followed by the 3 character net source (block serial and line position at edge of block).

(b) Succeeding lines contain:

(1) A descriptive line name.

(2) The leg identifiers of the blocks to which the entry is destined. The identifiers must be separated by commas and each line of identifiers must be enclosed by parentheses.

(c) All columns to the left of the right most left edge-line shall be devoid of logic blocks.

5.2 PAGE EXIT INFORMATION. The following data must be supplied for each exit from a CLD page:

(a) Line 1 contains the page to which the exit is going followed by, at the extreme right, the net source (block serial and line position at edge of block) from which the exit comes.

(b) Succeeding lines contain:

(1) A descriptive line name.

(2) The leg identifier(s) of the block(s) to which the exit is going. The identifiers must be separated by commas and each line of identifiers must be enclosed by parentheses.

(c) A minimum of two block positions must be left void of logic blocks to the right of all right edge lines unless the page boundary intervenes.

5.3 LENGTH OF LINES. No entry or exit line shall utilize less than five horizontal print positions.

6.0 PAGE DATA

6.1 EACH PAGE must indicate at least the following:

(a) The part number
(b) The EC level
(c) The version number
(d) The page number
(e) An appropriate title
(f) Machine type

1.0 INTRODUCTION

This section defines the content and format for microprogram lists used in place of hardware to perform the control logic of a machine. It is also applicable to all systems that utilize microprograms to perform machine functions and may be used instead of CES 0-1046-004, Part 5, Section A.

Besides supplying rules to generate maintenance documentation of a Control Store Program, this section (Section B) provides options necessary to include unique requirements of individual machines such as mnemonic prefixes, assignment of facilities, statement format, support information and document format. However, use of the options requires FE concurrence prior to implementation.

Compliance with instructions given in this section is expected (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 REQUIREMENTS

2.1 FORMAT AND PAGE TYPES: The document is a machine listing consisting of 132 columns and utilizing the IBM "H" print chain, (48 characters). The "H" chain shall be used for in-plant printout, lined paper is recommended.

2.1.1 Title Page: The title page shall consist of the following:

a. Machine Type.
b. Microprogram Name.
c. Part Number. (However, if each machine has a customized document, the machine serial number may replace the part number.)
d. EC Level
e. List of Included Features.

For secionalized release, each section shall contain items "a." through "d." on the first page.

2.1.2 Table of Contents: A separate page tabling the contents of the entire document, preferably by page numbers. Routine names and/or sequence numbers may be used.

2.1.3 Support Information: The following is a list of information that is required:

a. Description and operation of Facilities.

b. A list of the functional symbols with their definitions.

c. A list of all mnemonic operators with their definitions and descriptions.

2.1.4 Routine Requirements

2.1.4.1 Support Information: The following data related to each routine shall precede that particular routine.

a. Routine Flow Diagrams and/or Descriptions. The Flow Diagrams may replace the Flowcharts in the Field Engineering Maintenance Diagram Manual (FEMDM). If these diagrams appear only in the FEMDM, EC controlled supplements shall be shipped with the field B/Ms.

b. Additional information may be added when pertinent to the machine operation. Example: entry points, exit points, status or content of pre-assigned facilities, timing charts, etc.

2.1.4.2 Routine Listing: Shall consist of the list of microinstructions for that routine. Details of the page format are given in paragraph 2.2.

2.1.5 Address List: This list shall be a part of the document described by this practice or it may be a separate document. The address list shall contain the following information in storage address sequence:

a. The true storage location of the microinstruction to match consol display.

b. Routine mnemonic and sequence number.

c. Representation of microinstruction word to match consol display.

d. Whatever data is required to enable the Field Engineer to easily reconstruct the microinstruction word as it is contained in the control store.

e. An EC level may be placed by each microinstruction on the list.

f. If the Microinstruction List is in actual ascending ADDRESS order, no Address List is required. In this case, the information required by Item d shall appear on the Microprogram Listing.

2.2 ROUTINE PAGE FORMAT: (See Figure 5-4.)

2.2.1 Routine Heading: The routine heading shall be placed at the top and/or bottom print line of each page. It consists of the following:

a. Routine mnemonic, a routine name of up to six characters (the first character must be alpha).

b. Routine Name, a definition of the routine mnemonic.

c. Each page shall also contain the part number or machine serial number, EC level and date, machine type, and when applicable, the version identification.

d. A page number is required on each page.

2.2.2 Column Headings: The column headings shall be placed on the second line of each page, listed from left to right, in the following order: See Figure 1.

2.2.2.1 ADDR: True storage location of the microinstruction. It must match any display of any register that addresses the microinstruction.

2.2.2.2 INST: Representation of the microinstruction. It must match the console display.

If the information appears in the address list, this column is optional. However, its use is recommended for short instruction words.

2.2.2.3 SEQ: The sequence number of the microinstruction consisting of up to four decimal digits. The high order zeros should not be printed. This column is not required if the address is used in place of the sequence

number (see Paragraph 2.3.1). When this occurs, Sequence Number is replaced by the address wherever the rules require a Sequence Number.

2.2.2.4 FROM: The routine mnemonic if not within the same routine, and the sequence number of the from instruction. This column may be replaced by listing the FROM information in a sorted cross reference list at the end of the routine. (See 1.9) The sorting key shall be chosen to be the most efficient for the system.

2.2.2.5 TO: The branch leg(s) and its sequence number(s) to be executed next.

2.2.2.6 LABEL: When applicable, the label of the current instruction consisting of up to six alphameric characters. The first character shall be alpha.

2.2.2.7 LEG: When applicable, branch leg identifier of the current instruction. The leg identifier consists of the number of binary bits or hex characters necessary to represent each instruction of a branch.

This column is not required for a two way branch if one leg refers to the sequenced instruction.

Example:

BR IF Z=0

2.2.2.8 NEXT-LABEL: Label of the branch instruction to be executed next. This column is not required if the Next Label is always part of the branch statement.

2.2.2.9 STATEMENT: The expression that describes the operation(s) being performed when executing the microinstruction.

The statement column may be divided into subcolumns whose contents shall be identified by using the characters of Paragraph 2.4.4.3 as headers.

2.2.2.10 COMMENTS: Information that will:

a. Clarify the operation.

b. Define complex mnemonics.

c. Give reference of operations to data or hardware.

d. Relate to status conditions.

Comments or descriptive data not associated with a particular instruction may utilize full print lines. Each line shall be identified by an asterisk (*) in the left most print position used.

2.2.2.11 Overflow: No microinstruction shall be permitted to overflow onto a second page.

2.3 CONNECTIVE SYSTEM

2.3.1 Sequence Number: Every microinstruction, within a routine, shall have a unique sequential identifier. The sequence numbering shall be decimal, assigned in ascending order but not necessarily consecutive. However, consecutive numbering is recommended. If the addresses are in ascending order throughout the entire list, they may be used in place of sequence numbers.

2.3.2 Cross Reference

2.3.2.1 TO Sequence Numbers shall be used in conjunction with any microinstruction when the next instruction is not the next sequence. For branch sets the leg identifier shall precede the sequence number and the TO reference shall be in ascending sequence of the leg identifiers. If all possible legs of the branch set are used and appear as sequential instructions then only the low order leg of the set need be identified.

In the event that the same set of "TO" information is used by many instructions in the list, it will be permissible to give a symbolic name to the entire set and refer to it symbolically. All such named sets of "TO" information must be clearly defined and documented within the descriptive material.

2.3.2.2 FROM Sequence Number, shall be used in conjunction with any microinstruction that has not progressed sequentially from the previous instruction.

2.3.2.3 Branching Between Routines: The sequence number, the next label, and the from sequence number must be preceded by the routine mnemonic.

When addresses are used as sequence numbers, the cross reference by label only is acceptable provided all entry points are listed by label and address in front of the referenced routine.

2.4 LANGUAGE. If, in the application of this standard, a repetitive use of specifics of the basic language appears due to unique machine design characteristics, then named facilities or mnemonic may be used provided that:

a. The definition is described in the basic language within the descriptive material.

b. Such named facilities or mnemonic do not conflict with language defined in Table I.

Although syntax and symbols have been provided to prepare statements down to the smallest detail, the designer is urged to seek out the best combination of meaningfulness and efficiency. This can be accomplished by defining mnemonic operators and facilities commensurate with the particular machine.

2.4.1 Facilities

2.4.1.1 Definition of a Facility. A facility is an ordered set of binary bits (or a bit) which has:

a. A name.

b. A length equal to the number of bits in the set.

c. A value which is maintained until changed.

d. A sub set of a facility may also be defined as a facility.

2.4.1.2 Each Facility shall be identified by up to eight unique characters, the first of which must be alphabetic.

2.4.1.3 Portions of Facilities shall be identified by identifying the byte(s) and/or bit(s) by the following rules:

a. Bytes shall be identified within a facility by consecutive numbers starting with zero for the most significant byte. (Left most)

b. Bits will be identified within a byte by consecutive numbers starting with zero for the most significant bit.

c. A period (.) shall be used to delimit the byte portion from the facility and likewise the bit portion from the byte.

Example: D2.1.3 Bit 3 of byte 1 of facility D2.

d. If it is desirable to represent a facility of more than one byte by bit numbers only, then a double period (..) shall be used.

Example: B..14 Bit 14 of facility B.

NOTE: An option is permitted when, throughout the document, ONLY bits are the referred to portion and this is clearly stated in the support documentation. Then a single period is the delimetor between the facility name and bit position.

e. Concatenation of facilities or portions of facilities shall be shown by using the slash (/) between the applicable bytes and/or bits.

Examples:

Z.0.2/5 bits 5 and 2 of byte 0 of facility Z.

Z.1/3 byte 1 and 3 of facility Z or bit 1 and 3 of facility Z if only bits are the referred to portion.

Z.1.3/3.2 bit 3 byte 1 and bit 2 byte 3 of facility Z.

f. Consecutive Bytes or Bits may be shown by use of the dash, or the word TO.

Example: B..2-14 Bits 2 through 14 of facility B.

g. The above portion conventions may be replaced by clear concise English. For example: Z BIT14 instead of Z.2.6 (of an 8 bit byte). A space shall be left between the facility name and the English.

2.4.2 Indirect Addressing: Occurs when the data to be operated on comes from a portion of a facility specified by the contents of another facility.

2.4.2.1 Documentation of Indirect Addressing shall be governed by the following rules:

a. The facility containing the address modification shall be enclosed by parenthesis and preceded by the accessed facility name.

Example:

A(R1), where A is the accessed facility and R1 is the facility containing the address modification.

b. The length of the data addressed may be indicated by one of the following length operators:

DG	Digit	=half-byte
BY	Byte	=1 byte
HW	Halfword	=2 bytes
FW	Fullword	=4 bytes
DW	Doubleword	=8 bytes

The length operator may be omitted for the majority data length indirectly addressed. This shall be stated within the descriptive material.

Example: A(R1)HW Halfword of data in facility A addressed by the contents of facility R1.

NOTE: The facility name preceding the parenthesis may be omitted for the most often indirectly accessed facility. This shall be stated within the descriptive material.

c. If the address contained in the facility is to be incremented or decremented:

1) After the operation, this shall be indicated within the parenthesis following a comma, following the facility name.

Example:

A(R1,-2) means that the indirect address contained in the facility R1 is decremented by 2 after the operation.

2) Before the operation, this shall be indicated within the parenthesis preceding the facility name and separated by a comma.

Example:

A(-2,R1) means that the indirect address contained in the facility R1 is decremented by 2 before the operation.

Special requirements of the increment/decrement shall be stated in a consistent manner in English after the increment or decrement within the parenthesis.

Example:

A(R1,-2 UNTIL R0=0) means decrement indirect address R1 until counter R0=0.

2.4.3 Functional Symbology

2.4.3.1 Symbols to be used in microinstruction statements are given in Table 1. They are arranged by priority of application, highest priority first. Sub-statements are required for statements that apply these operators in a different priority.

A list of symbol definitions is a requirement to be shown in the support information.

2.4.3.2 Symbol Rules of Application:

a. The comma (,) delimitor shall be used to separate a logic function from the facilities operated on. For the following operators: +, -, +-, =, *=, the commas are not required.

b. Literal value delimitor shall be used with the period preceding the value to indicate that the value is binary. No period shall indicate hexadecimal, the letter D following the literal indicates decimal.

Example: A*='F7' A is set to the hexadecimal value F7

A*='0101' A is set to the binary value 0101

A*='110'D A is set to the decimal value 110

c. Shift Operator Examples:

A*=SL5,A Means Shift Left facility A 5 bit positions and set into A

A*=SR(I),A Means Shift Right facility A the number of bit positions specified by the contents of facility I and set into A

2.4.4 Statement Format: Shall take the form of destination *=source, operator, source. (Branch statement Form is shown in 2.4.4.1 g & h.)

2.4.4.1 Rules for Statement Format:

a. The source shall be a facility and/or a portion of a facility or literal. e.g., A.1.2

b. The source may be indirect (see par. 2.4.2) e.g., B(A)

TABLE 1

A. Delimitors

() Parentheses, enclosing delimitor for facilities holding an indirect address modifier

. Period, delimitor between facility-name.byte number.bit-number and to indicate literal value in binary

'' Apostrophe, enclosing delimitor for literal values

,, Commas, enclosing delimitor for operators expressed in alphabetics

, Single comma to separate multi destinations and to separate facility from increment/decrement in indirect addressing

) Single parenthesis to separate the statement identifier or the mnemonic prefix from the statement

B. Logical Operators

SLn Shift left n bit positions, open ended

SRn Shift right n bit positions, open ended

A Logical AND

OR Logical OR

OE Exclusive OR

/ Slash, separator between concatenated facilities or portions of facilities

C. Arithmetical Operators

+ Plus, True add

- Dash, Complement add

+- Plus dash, True or complement add

D Decimal prefix i.e., ,D+, means decimal add

D. Compare Operators

= Equal to
NE Not equal to
LT Less than
GT Greater than
LE Less than or equal to
GE Greater than or equal to

E. Result Storing Operator

*= Set to

F. Special

* Asterisk, Special, must be defined in microinstruction comment, or if often used and unique for a routing in the introductary comment of this routine, or if unique for a machine in the supporting information (see 2.1.3)

If additional operators are required, contact your local Standards Operation.

c. The source may be concatenated facilities. In this case they shall be separated by the / delimitor with the high order facility or portion preceding the delimitor. e.g.,A.0/B.0

d. The source may be a literal value or a literal value concatenated with a facility. In the latter case rule c shall be followed. i.e., '00'/A.1.

Note: An exception to the positional notation in rule c is given for the carry facility. The carry with a set into will be shown following the set into facility. i.e., AC*=A+B+C

e. When more than one statement is required, a minimum of four spaces shall separate the statements.

f. Instruction statements that are not clearly self-evident under the rules of this practice shall have a mnemonic prefix (see paragraph 2.4.4.2).

g. Branch statements shall take the form Bxx)C1, C2,...Cn where Bxx is the mnemonic for a branch operator and C1, C2, etc. are the branch conditions.

h. Optional form for branch statements of /360 assembler language type are permitted and shall have the form
BR TO d IF c
where d is the definition of the TO address by a label or by a facility or concatenated portions of facilities where indirect addressing may be used and c is the condition in clear, concise English or in the format: source, compare operator, source.

A Branch statement may also be defined by the statement identifier R.

Examples:

BC)ST2,ST4	Conditional Branch on ST2 and ST4
R)ST2,ST4	Conditional Branch on ST2 and ST4

The sequence of the Branch conditions follow the order of the next address portion they modify. An X shall be used to indicate that the corresponding part of the address remains unchanged.

Note: The same Branch statement format shall be used throughout the entire microprogram listing.

2.4.4.2 Mnemonic Prefixes to the statement shall be used when required for clarity. When used, these mnemonic terms must be described in the introduction to the list. The following list contains examples of approved mnemonics:

BR	Unconditional Branch.
BC	Branch on condition.
BAL	Branch and Link.
BMS	Branch and Module Switch

Other mnemonic prefixes may be used. (see paragraph 1.9)

2.4.4.3 Identification of statements (Type of CAS edge character): One of the following characters may precede each statement to define it. A closing parenthesis shall separate these characters from the statement. The allowable characters and corresponding definitions are:

a. E - Emit Value (in Binary, Hex, or Decimal) or Statement. See 2.4.3.2 b

b. A - Arithmetic Statement (or micro orders). This will include that information which defines the operation of the main arithmetic unit.

c. B - Arithmetic Statement (or micro orders). This will include that information which defines the operation of the secondary arithmetic unit.

d. D - Data Flow - This describes the transfer of data from facility to facility excluding that which passes through the arithmetic unit.

e. S - Storage Controls and Addressing - This includes that information which defines the operation of all storages in terms of read, write, etc., and data flow to the storage address register(s). (The data flow to or from the storage data register must be described within the data flow statement of arithmetic statement portion of the microinstruction.

f. When a line is used specifically to describe local storage, the alphabetic character L must be used.
L - This includes that information which defines the operation of local storage in terms of Read, Write, and Addressing.

g. C - Control, Miscellaneous - This describes those miscellaneous controls and tests which are not described within the other sections.

h. M - Shifter - Includes all shift statements not handled by characters A and B.

i. R - Addressing - This information describes the data flow to the Address Register and the tests performed which determine the next address to be executed.

j. It is recommended that the information be arranged in the following sequence:

(1) Emit value and/or miscellaneous controls (top line only) which will be identified by the appropriate edge character(s).
(2) Arithmetic
(3) Shifter
(4) Data Flow
(5) Storage Controls and Addressing
(6) Controls
(7) Addressing

The information need not be consecutive. For example: if no data relative to storage appears, the control data could follow the data flow state-

ment(s). Multiple lines with the same character are allowable.

2.4.4.4 For the greatest clarity, the designer is cautioned in his choice of facility names and labels to avoid wherever possible duplication of operators and mnemonics required by the statement language.

3.0 SUPPLEMENTARY INFORMATION

3.1 RELOCATION: If Engineering requires microprogramming relocation, then the paragraphs requiring true addressing must be altered by a relocation scheme and supporting documentation. (See paragraph 1.9)

```
EXAM        EXAMPLE ROUTINE                 PART# XXXXXX  EC YYYYYY  DATE ZZ/ZZ/ZZ          /360-NN

ADDR INST   SEQ   FROM       TO             LABEL-LEG     NEXT-LABEL    STATEMENT          COMMENT

2000 C4E9   120                  1-130                     ALLSET     R)BR IF Z='0'         BR IF 2ND CHNL IS 'C'
2002 E0DC   121                  1-124                     HINOT3     R)BR IF HZ,NE,'0'     BR IF 2ND CHNL IS NOT 3X
2004 041B   122                                                       A)Z*=G0,A,'01'        MASK FOR 'A'
1688 9864   123                    131                     BRBAD      R)BR                  UNCONDITIONAL BRANCH
168A 042D   124         121                               HINOT3     A)Z*=G0,A,'20'        MASK 2ND CHNL FOR 2X
168C 9426   125         124        00-126                 CONDBR     FOURWA     R)ST1,ST4  CHECK STATUS
                  DCLC 061
1870 3BE9   126         125          132                  FOURWA-00  CHECK1     B)ST5*=1  R)BR  SET ST5.BRANCH UNCOND.
1872 3BD8   127         125          132                  FOURWA-01  CHECK1     B)ST6*=1  R)BR  SET ST5.BRANCH UNCOND.
1874 3BA1   128         125          133                  FOURWA-10  CHECK2     B)ST2*=1  R)BR  SET ST2.BRANCH UNCOND.
1876 3B67   129         125          133                  FOURWA-11  CHECK2     B)ST3*=1  R)BR  SET ST3.BRANCH UNCOND.
1878 5F4D   130         120                               ALLSET               A)DW*=IS,A,'F0'   SET C.U.ADDRESS INTO DW
                                                                               B)IG*='08'        TURN ON POLL ENABLE
1900 D9C1   131       123,130                             BRBAD                A)OPC*=ER         SET ERROR CODE
1902 2404   132       126,127  ERRT 00-001                CHECK1     ERRT ENTRY1 A)BY*=UR,OR,'0F'  USE DEVICE ADDRESS TO CHK
                      131                                                      R)C1,C2
1904 D66E   133       128,129                             CHECK2               A)D*=IH,OE,BY     COMPARE ADDRESSES
1906 1623   134                                                                A)DW*=BY          ADDRESS IS SET TO BUS-IN
1908 EF4D   135                                                                A)FT*='81'        SELECT AND RAISE CONTROL

EXAM        EXAMPLE ROUTINE                 PART# XXXXXX  EC YYYYYY  DATE ZZ/ZZ/ZZ          /360-NN
```

FIGURE 5-4. PAGE FORMAT

1.0 INTRODUCTION

This section defines the content and format for ROS address lists and control field charts and will establish uniformity in the released documentation for ROS controlled machines.

Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 ADDRESS LISTS

2.1 REQUIREMENT. An address list must be provided for each releasable element of a ROS controlled machine, i.e., module array, board assembly, etc.

2.2 CONTENT AND FORMAT. The address list is a sequential listing of ROS addresses. It must be in sequence by address register contents and must provide the following information for each address in the order indicated below.

(a) Both hexadecimal (3 or 4 characters) and binary representation of each address.

(b) The CAS Logic Diagram (CLD) page number and block print coordinate of the addressed micro instruction.

(c) Mode of Operation or Type of Instruction where applicable (0 through 6 characters).

(d) The binary bit configuration of the micro instruction in bit order as displayed on the console or a "set sense amplifier latch" is a logical one. Each control field must be identified on the header line. The bits with each word must be aligned so as to provide spaces between the control fields. In addition, on those machines that utilize more than one control field format a header line must be printed each time the format changes, and the spacing of the bits must change accordingly. Ones and zeros will be used.

(e) The manufacturing EC level of the micro instruction.

(f) The version number if applicable of the micro instruction.

(g) The physical location of the address (micro instruction). (0 to 18 characters)

(1) CCROS physical location.

a. Board. One to four digits, right adjusted.

b. Card Number. One to two digits, right adjusted.

c. Card Row Number. One or two digits, right adjusted.

d. Card Field, if applicable. (Lowest number bit position in that field.) One to three digits, right adjusted.

Example:

Board	Card	Row	Field
0001	02	09	021

(2) TROS physical location.

a. Tape Position Number. Three decimal digits, right adjusted.

b. Tape Stagger Class. One alphabetic character.

c. Word Number. One alphabetic character.

d. Tape Field, if applicable. Low order bit position. One to three digits, right adjusted.

Example:

Tape	Class	Word	Field
127	C	A	021

(h) Optional.

(1) The physical location of the components which select the address, i.e., location of the gate and driver cards.

(2) Below the field heading, the low order bit position of each control field, as a decimal notation.

2.3 PAGE IDENTIFICATION. Each page must indicate the following:

(a) The part number EC level and machine location of the customized physical assembly described on that page.

(b) The part number, EC level and version number of the page.

ADDRESS		CLD			BIT CONFIGURATION										
HEX	BINARY	PAGE	BOX	MODE/TYPE	CA	CB	CC	CD	CN	CV	CS	EC LEVEL	VERSION	PHYSICAL ADDRESS
1C0	0001 1100 0000	QB101	A4		0110	01101	10	0000	1111	01	000	120123		
1C1	0001 1100 0001	QB101	C3		0010	00100	00	0101	1010	01	010	120123		
1C2	0001 1100 0010	QE036	A6		0000	00000	01	0010	1011	01	001	124682A	A01	
1C3	0001 1100 0011	QB104	A3		1000	00000	01	1000	0000	01	001	120123	A01	
1C4	0001 1100 0100	QB104	A4		1000	00000	00	0110	0000	01	100	103684	A01	
1C5	0001 1100 0101	QB104	A5		0100	11001	11	1000	1010	11	000	120124	002	
1C6	0001 1100 0110	QB104	C3		0011	01111	10	1101	1010	11	000	120123	002	
1C7	0001 1100 0111	QB104	C6		1000	11100	10	0011	1101	00	101	120124	002	
	(a)	(b)		(c)				(d)				(e)	(f)	(g)

FIGURE 5-5. ADDRESS LIST

3.0 CONTROL FIELD CHARTS

3.1 REQUIREMENT. A Control Field Chart must be provided for each ROS controlled machine.

3.2 CONTENT AND FORMAT. Each control field chart must provide the following information in the order indicated

3.2.1 Control Fields. Information must be given for each control field.

(a) Field Identification. Identified in the same manner as on the address list.

(b) ROS word bit positions.

(c) Control Field Function. A brief description of the function must be indicated.

3.2.2 Bit Configuration. Information must be given for all bit configurations used in each field.

(a) CLD edge character

(b) Micro order

(c) Bit configuration in binary

(d) Decimal Order

(e) Function

(f) ALD reference. It must include the ALD page and net number to locate the specific line brought up as the result of decoding the bit configuration. Exception: If the ALD page has adequate block titling the net number may be omitted.

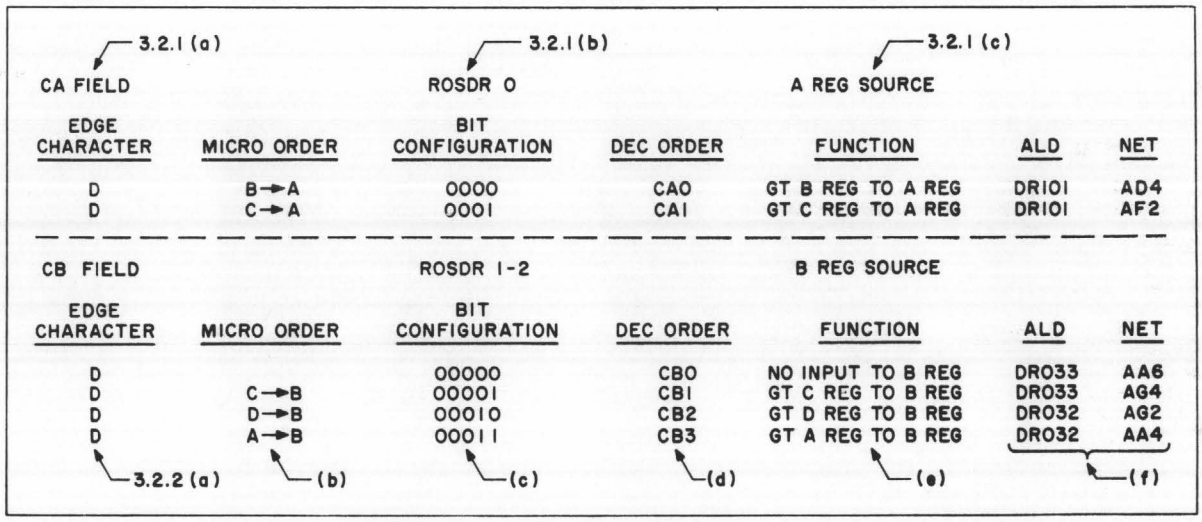


FIGURE 5-6. CONTROL FIELD CHART

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1.0 INTRODUCTION

This section defines the content and format for interface and reference pages of logic diagrams for multiple-usage products. Rules to determine when these pages are needed are included.

Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 DEFINITIONS

2.1 INTERFACE PAGE is the page giving the logical and/or physical connection between logic pages of interconnected products.

2.2 REFERENCE PAGE is the page which gives additional information necessary to explain the contents of logic pages.

2.3 DESIGNER. For purposes of this standard, designer is defined as the group which releases and has engineering control of the multiple usage product (or second order product).

2.4 USER. For purposes of this standard, user is defined as the engineering group which uses, but does not control the design of, the multiple usage product.

2.5 PRODUCT. For purposes of this standard, product is defined as any piece of equipment which is released with logic diagrams.

2.6 MULTIPLE USAGE PRODUCT is a product which is either a machine with a type number, an assembly, or a second order product.

3.0 GENERAL

3.1 INTERFACE AND/OR REFERENCE PAGES are required when the line titles on the logic diagrams do not contain logic page numbers for lines interconnecting the products. The interface pages complete the logic flow between the units. Separate interface pages are required for each use of the multi-usage product. An exception is noted: Wherein the multi-use product(s) are driven by common logic, i.e., a multiplex data bus.

4.0 RULES AND FORMAT FOR INTERFACE PAGES

4.1 GENERAL. Multiple usage products and their logic pages fall into two physical location categories. Paragraphs 4.2 and 4.3 define the format and rules for these categories.

4.2 CATEGORY I. The multiple usage product is physically located within the using machine type and its logic pages are contained within the user's logic manuals.

4.2.1 Page Numbers. The designer shall specify the logic page numbers for the required interface pages.

4.2.1.1 Second Order Products. The second order product designer shall assign interface page numbers from the numbers reserved for his logic. These numbers shall be AANN0 (A = alpha, N = numeric, the last digit, zero). These same page numbers must be used by each user when creating his interface pages. The zero is to permit multiple usage of the second order product by the user who generates pages AANN1, AANN2, etc. as required.

4.2.1.2 Multiple Usage Products. Units with assigned machine type numbers shall have page numbers assigned by the designer. It is recommended that the first numbers of the series be assigned to interface pages. These same page numbers must be used by all users.

4.2.2 Control. The user shall assign part numbers. He will be responsible for releasing the product using pre-assigned page numbers.

4.2.3 Interface Page Content and Format. Each interface page shall contain the following information: (See Fig. 6-1.)

(a) Logic page number specified by the designer.

(b) The name of the product.

(c) The machine type and page part number of the using product.

(d) ENTRY and EXIT blocks for logic lines entering and leaving the multiple usage product or a tabular listing.

(e) Line names and net numbers of all lines running between units.

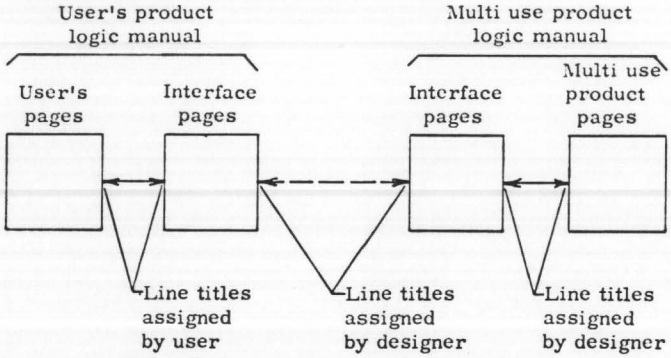
(1) Line names and net numbers in the multiple usage product shall be common for all interface pages.

(2) Line names and net numbers in the using machine type shall be assigned by the user.

4.3 CATEGORY II. The multiple usage product is not physically located within the using machine type and the logic diagrams are not contained within the user's logic manuals.

4.3.1 Page Numbers. The use of corresponding interface pages using the W series of numbers in each physically connected unit's logic manuals provides common location within the volumes. Refer to Section C for details of page assignment.

4.3.2 Control. The user and the designer shall be responsible for releasing the interface pages appearing in their respective logic manuals.



4.3.2.1 Category II Machine Designers. Must check with the user before assigning line titles in order to determine whether or not they share common lines with already existing Category II machines. If common lines do exist, i.e., a multiplex data bus, then identical line titles shall be assigned.

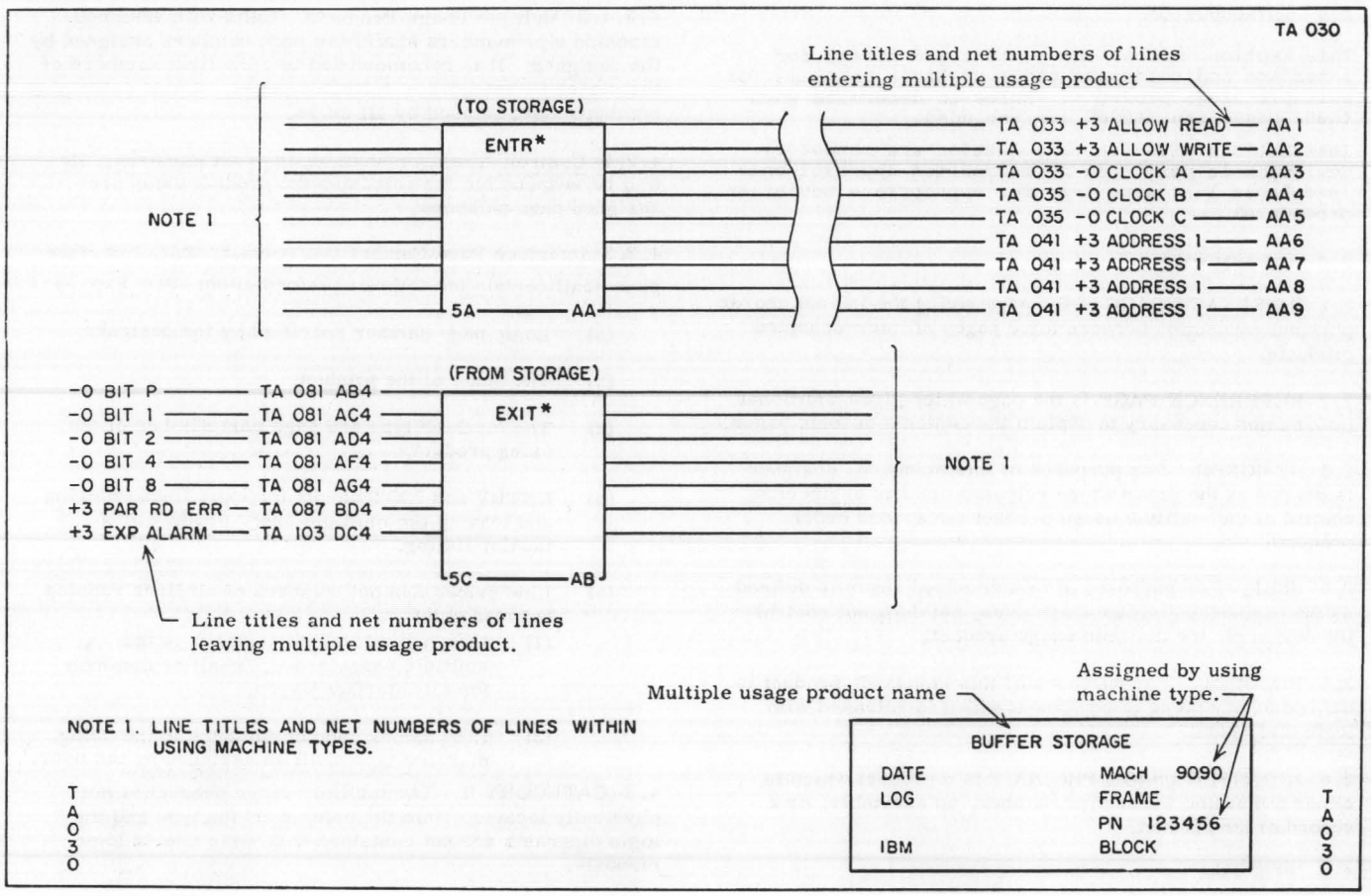


FIGURE 6-1. TYPICAL INTERFACE PAGE (CATEGORY I)

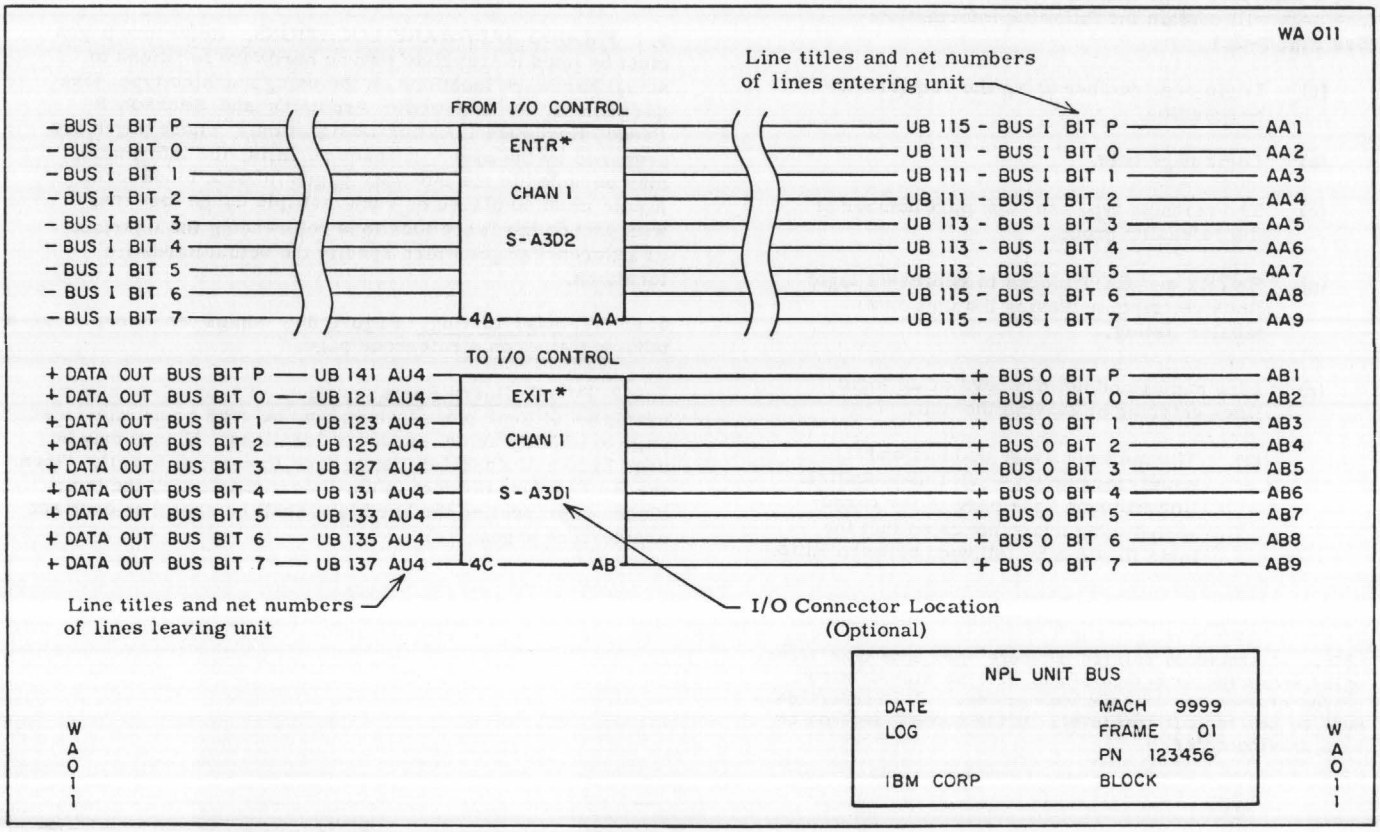


FIGURE 6-2. TYPICAL INTERFACE PAGE (CATEGORY II)

4.3.3 Interface Page Content and Format. Each interface page will contain the following information: (See Fig. 5-2.)

(a) Logic page number using the required W-designation.

(b) Logic page title.

(c) The machine type and page part number of the releasing group.

(d) ENTRY and EXIT blocks to represent logic lines entering or leaving the unit or a tabular listing.

(e) Line names and net numbers of all logic lines entering or leaving the unit.

(1) The multiple usage product and the using machine type must use identical line titles on each page of the corresponding interface pages so that the logic flow can be followed between units.

NOTE. It should be pointed out here that some conditions exist where the interface signal will be plus or minus dependent upon the interfacing machine. This condition must be spelled out completely in the comment section or by a drawing note.

5.0 RULES FOR REFERENCE PAGES

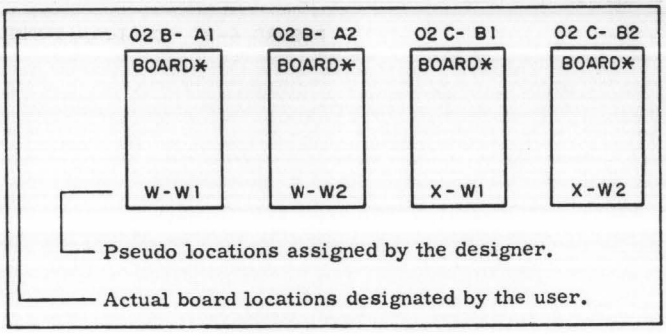
5.1 PSEUDO HARDWARE LOCATIONS. Reference pages must be used to translate pseudo hardware locations to actual hardware locations on the using machine type. (See Section D, Second Order Products and Section B Pseudo Hardware Location Designation.) These pages are prepared by the user. If space permits, the information may be added to the interface pages in logic block form. A note must be placed on each multiple usage logic page with pseudo hardware locations referencing the interface or reference pages which specify the actual hardware locations.

5.1.1 Tabular Listing. Figure 6-3 shows an example of a tabular listing on a reference page.

5.1.2 Pseudo Board Representation. Figure 6-4 shows examples of logic blocks which may be used on an interface page to identify actual hardware locations. Blocks may be used in lieu of a tabular listing (see Paragraph 5.1.1). When the multiple use product is used more than once, the logic blocks representing the hardware shall be shown on each set of interface pages.

Pseudo Locations (within multiple usage product)			Actual Locations (within using machine)		
Frame	Gate	Board	Frame	Gate	Board
50	W-	W1	02	B	A1
50	W-	W2	02	B	A2
50	X-	W1	02	C	B1
50	X-	W2	02	C	B2

6-3. TABULAR LISTING



6-4. EXAMPLE OF LOGIC BLOCKS

1.0 INTRODUCTION

This section defines pseudo-hardware location notation used on logic diagrams for multiple-use assemblies (i.e., second-order products). Rules to determine proper location designations for pseudo-hardware are included.

Instructions in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 GENERAL

2.1 USAGE. Pseudo hardware locations must be shown on automated logic diagrams when a single set of logic pages are prepared for multi-use product and the hardware locations vary between the using machine types. Actual hardware locations are used when locations are fixed within all using machine types.

3.0 RULES

3.1 DESIGNATION. The following rules must be followed to designate pseudo hardware locations.

3.1.1 Frame. The numbers 50 through 63 must be used on the bottom of the logic sketch sheet to designate pseudo frame locations. Only one frame designation shall be shown on a single logic page.

3.1.1.1 Example. If the hardware is always contained within one frame, the pseudo number 50 would be used. If the hardware were located in four frames 50, 51, 52, and 53 would be used as pseudo frame numbers (see Figure 6-5).

3.1.2 Gate. Consectuive alpha characters from the end of the alphabet must be used. For example, if one gate existed it would be Z; if three gates existed they would be X, Y and Z. The letter would appear on line 5 of the logic block and would be followed by a dash. One letter and dash shall be used for each gate required. See Figure 6-6.

3.1.3 Board. The letter W, X, Y, and Z and numeral 1 through 9 designates pseudo board location on line 5 of the logic block. One letter and one number shall be used, sequentially, starting with W1. See Figure 6-6.

3.1.4 Card Socket. Actual card socket positions must be shown on line 5 to designate actual card positions.

3.2 REFERENCE PAGE. Reference pages must be used to translate pseudo hardware location to real locations on the using machine type.

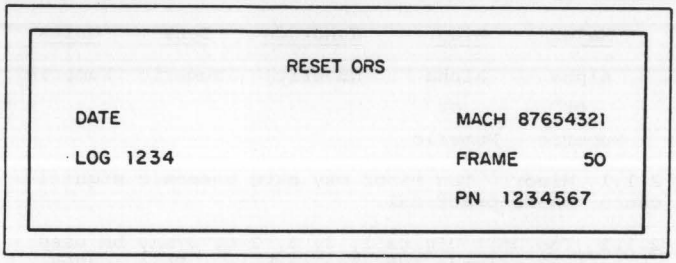


FIGURE 6-5. EXAMPLE OF FRAME NUMBER IN TITLE BLOCK

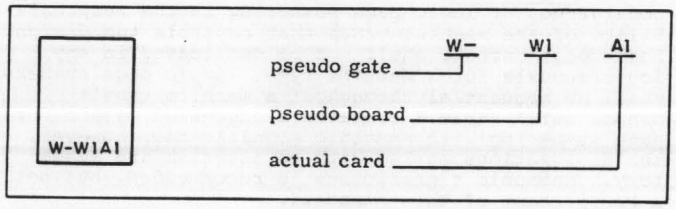


FIGURE 6-6. EXAMPLE OF LINE 5

1.0 INTRODUCTION

This section defines the page-numbering system for SLD/SLT diagrams. Included are rules to insure continuity of logic flow from page to page and to maintain consistency of page numbering for similar units or logic sections regardless of machine type.

Instructions in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 FORM

2.1 PAGE NUMBER. The general form of the page number is:

Major	Minor	Hundreds	Tens	Units
Alpha or Numeric	Alpha or Numeric	Numeric	Numeric	Numeric

2.1.1 Minor. The minor may have mnemonic significance, where practical.

2.1.2 The Unit Digits 1, 3, 5, 7 or 9 may be used on initial release for page numbers. This leaves every other page number open for expansion.

2.1.3 Logic Flow. Continuity of the logic flow and consistency of logic page numbering is the responsibility of the machine group that controls the design. Logic page numbers shall not be duplicated in any logic manuals for a machine type. Logic page numbers shall be sequential throughout a machine type's manual set. Table I contains a suggested method for page numbering with mnemonic significance; however, the designations marked with an asterisk are mandatory. Mnemonic significance is recommended, but not a requirement of this standard.

TABLE I

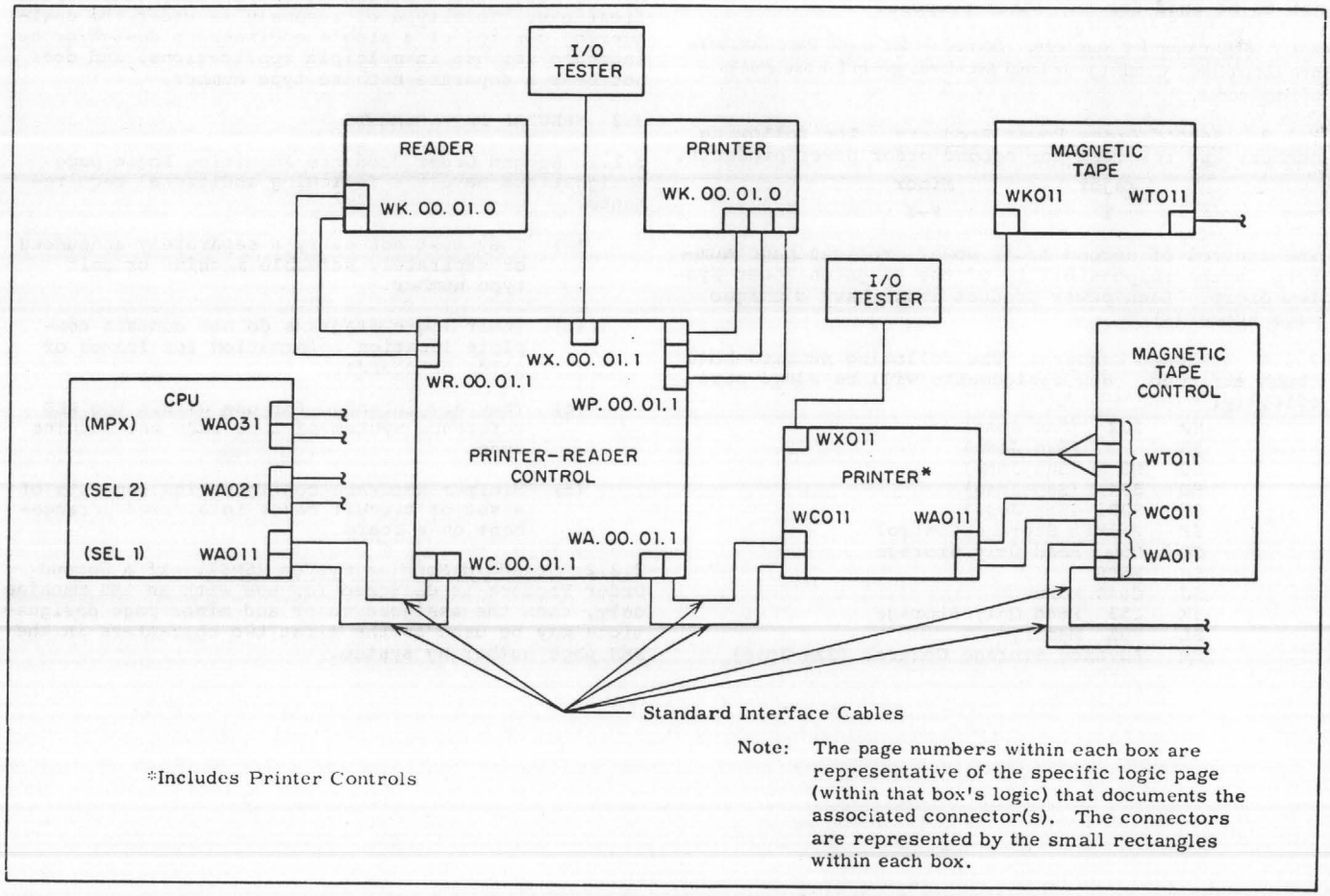
Major	Minor	
0 (numeric)	0-9, A-Z	Master Table of Contents
*A	1-4	Socket Listings
*A	5	Additive Card Code (ACC) Listing
*A	6-8	Tie-down list by feature and/or location. Pictorial representations and description of pluggable cards. Adjustable timings of cards (with limits, narration, etc.). Single shot adjustments and procedures, strobe timings and procedures.
A	A-Z	ADDERS including controls, decode, bussing, etc.
B	A-Z	Bussing which is normally not associated with other sections.
C	A-Z	Counters (including controls, decode, bussing, registers directly associated with the counter).
D	A-Z	Decoders (which are not normally associated with other sections including registers directly associated with this function).
E	A-Z	Not presently assigned.
F	A-Z	I and/or O Channels, Adapters, and Controls
G	A-Z	I and/or O Channels, Adapters, and Controls
H	A-Z	I and/or O Channels, Adapters, and Controls
*I	A-Z	Not to be used.
J	A-Z	I and/or O Channels, Adapters, and Controls
K	A-Z	Controls (which are not normally associated with other sections).
L	S-T	Local Storage and Controls (non-programmable storage).
M	A-Z	Main Storage, Register, and Controls (CPU) (not normally associated with other functions).
N	A-Z	Not presently assigned.
*O	A-Z	Not to be used.
P	A-Z	Console, Console Adapter, Panel
Q	A-Z	Read Only Storage (ROS) Documentation (including CAS Logic Diagrams (CLD's) and address lists).
R	A-Z	Data Registers
*S	A-Z	Reserved for Second Order Products.
*T	A-Z	Reserved for Second Order Products.
*U	A-Z	Reserved for Second Order Products.
*V	A-Z	Reserved for Second Order Products.

Major	Minor	
*W	A-Z	Interface Pages (see Fig. 6-7).

The following minor characters are assigned:

- *A - CPU (Standard Interface) Channels I/O Cable Wiring (Standard Interface) toward next I/O box.
- *C - Cable Wiring (signal and control lines) to channel (toward CPU) for I/O boxes.
- *D - Cable wiring to display unit
- *F - Cable wiring to file
- *K - Cable wiring to Control Unit(s) from I/O units
- *P - Cable wiring to printer (or punch only, or console).
- *R - Cable wiring to Reader
- *S - Cable wiring to Storage
- *T - Cable wiring to Tape Unit
- *X - Cable wiring to I/O Tester

Major	Minor	
*X	A-Z	All types of special features (hand-drawn or automated) which are not associated with other sections.
*Y	A-E	Power Distribution
*Y	F-Z	Power Second Order Products
Z	A-Y	Hardware oriented pages such as cabling, ground routing, etc. For I/O's, these are normally hand-drawn pages showing relay circuitry, brushes, ribbon controls, interlocks, motors, etc.
*Z	Z	Hardware oriented reference pages, relay charts, terminal boards, connector charts, switch charts, voltage nets, ground nets, etc.



*Includes Printer Controls

Note: The page numbers within each box are representative of the specific logic page (within that box's logic) that documents the associated connector(s). The connectors are represented by the small rectangles within each box.

FIGURE 6-7. INTERFACE PAGE NUMBERING

1.0 INTRODUCTION

This section defines the procedure to obtain system page designations for second-order product diagrams and includes a list of page numbers already assigned to these products. Stipulations are given to prevent duplication of page numbers and to permit use of systems logic pages for second-order products in more than one machine or system.

Instructions given in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.1 PAGE NUMBERS

2.1.1 Major and Minor Characters. These numbers consist of two alphabetic characters, e.g., SA, SB, TA, etc. They are the first two characters of the Automated Logic Diagram (ALD) page number. Characters reserved for second order products are:

Major	Minor
S	A-Z
T	A-Z
U	A-Z
V	A-Z

ALD page numbers starting with S, T, U, and V are reserved specifically for second order products and are not to be used for any other purpose.

2.1.2 Application for Numbers. Second Order Logic Page Numbers are controlled. Contact your local Standards group for assignment of page codes.

2.1.3 Second Order Power Products. The following numbers are reserved for second order power products.

Major	Minor
Y	F-Z

The control of second order power products page numbers is the responsibility of the Kingston Power System Group. Each power product shall have a unique page number(s).

2.1.4 Assigned Numbers. The following numbers have been assigned. New assignments will be added periodically.

SA	SJ2	(San Jose)
SB		(San Jose)
SC	M8	(San Jose)
SD	SJ4	(San Jose)
SE	SJB1	(San Jose)
SF	Ramkit Storage Control	
SG	C50 Read Only Storage	
SH	M500	
SJ	C040 Mono	
SK	C55 Read Only Storage	
SL	POK Memory	
SM	Advance Storage Control (San Jose)	
SN	Dolphin Disc File (Hursley)	
SP	Reserved (Endicott)	
SQ	Monolithic Main Storage - P21 (POK)	
SR	BSM Bridge	
SS	Minnow Disc Drive	
ST	RDI Remote Display Interface	
SU	DSI Data Set Interface	
SV	C146 Mono	
SW	ASC Mono	
SX	C86 Mono	
SY	FET--NSØ	
SZ	Monolithic Main Storage - P2IA (POK)	

2.2 USERS

2.2.1 Reference Pages. When a design group elects to use a second order product in a unit (machine type), the user must prepare reference pages to physically relate the pseudo locations contained in the logic for the second order product to the unit.

2.2.2 Interface Pages. For standard I/O pages for use with second order products, see Corporate Engineering Standard CES 0-1046-12.

3.1 DEFINITION

3.1.1 A Second Order Product is an assembly such as read only storage devices, integrated storage devices, power supplies, structures, etc. that has its own logics, wiring diagrams, and/or acceptance specifications. This type of assembly is under the engineering control of a single engineering design group, intended for use in multiple applications, and does not bear a separate machine type number.

3.2 SPECIAL REQUIREMENTS

3.2.1 Second Order Products Requiring Logic page designations have the following additional requirements:

(a) They must not carry a separately announced or separately saleable machine or unit type number.

(b) Their logic diagrams do not contain complete location information for frames or gates or boards.

(c) They are intended for use within the ALD reference system of more than one machine type.

(d) Minimum hardware configuration consists of a set of circuit cards in a fixed arrangement on a board.

3.2.2 Standard Modular System (SMS). If a Second Order Product is designed for use with an SMS machine only, then the assigned major and minor page designations may be used as the first two characters in the SMS page numbering system.

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1.0 INTRODUCTION

This section specifies the types of loose-leaf binders and binder tabs to package logic diagrams and other systems reference material.

Instructions in this section are mandatory: deviation is permitted by accredited approval only (see Table 1-1, page 1-2, for appropriate procedure).

2.1 BINDERS. Binders are available as shown below for Field Engineering Documents. The 11 × 17 inch size is limited to the 1 inch ring in order to fit forms racks which are presently in use in the field. The part numbers shown are to be used on shipping group B/M's for use in the Plant. These binders are also available to Field Engineering under the F.E. form numbers in the table.

2.1.1 Part Numbers of binders are as follows:

Sheet Size	Ring Size and Number	Part Number	F.E. Form Number
8-1/2 × 11"	1.0" - 22 Ring	222836	229-2048
11 × 17"	1.0" - 34 Ring	222837	229-2088
8-1/2 × 11"	1.5" - 22 Ring	853025	229-2049

The full capacity of the 1.0 inch ring binders is 125 sheets. All manual releases must utilize this capacity to its fullest, making allowance for addition of extra pages in the field, e.g., features and E.C.'s.

2.2 SPINE TABS. The above binders have a transparent plastic pocket on the spine which accommodates a paper tab to identify the binder contents.

2.2.1 Drawings. These spine tabs are to be released on form drawings as listed in 2.2.3. To allow for plant-oriented procedure variations and machine requirements, no method of handling will be set forth here. In general, however, it will be necessary to release one tab for each machine type and class of contents, leaving serial number blank. This information must be filled in by the function assembling the manuals in the manner most suitable considering the number of spine tabs to be printed.

2.2.2 Nomenclature Specification.

a. The top line on the tab will show the IBM machine type number. The lettering size specified on the form drawing is for the general case of a four or five digit number. If necessity dictates a line longer than the tab width will accomodate the lettering size may be decreased.

b. The second line is to be filled in with the serial number of the system. Lettering size commensurate with line length may be used.

c. The contents field "_____ to _____" on the ALD tab is to show the two position alpha-prefix shown on SLDA sheets. If some other page numbering scheme is necessary, this lettering size may be decreased to allow more characters per line. When release of field changes or features alters this designation, a new tab must be released for each volume affected.

d. "VOL" must be shown as "VOL XX (It is not necessary to show leading zeroes.)

e. Only (b) above will be filled in by the manual assembly function. All other nomenclature should be pre-printed on the tabs.

2.2.3 Tab Specification. Tabs shall be printed according to the data on the form drawings listed below, depending on the contents.

Contents	Color	Form Number
ALD's (Automated Logic Diagrams)	White	5-7804-1
MDP's (Maint. Diagnostic Programs)	Green	5-7804-2
MDM's (Maint. Diagram Manual)	Red	5-7804-3
CLD's (CAS Logic Diagrams)	Blue	5-7804-4

Note: Contact Engineering Drafting for assistance when planning tabs.

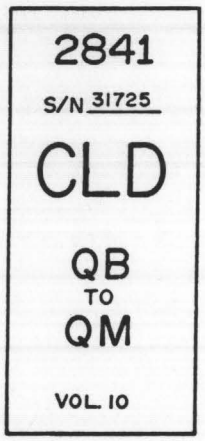

FIGURE 7-1. TYPICAL TAB

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IBM **Division**
Engineering Practice

SUPPLEMENT TO

STANDARDS PUBLICATION

DEB 0-1046-BKT

LOGIC DOCUMENTATION MANUAL

The attached document, DEP 0-1046-023, Logic Symbology for Unreleased EIS Engineering ALD's, NLT-HP, is issued as a supplement to the Logic Documentation Manual, First Edition, August 1970.

DEP 0-1046-023 consists of pages 2-36 through 2-40 and is Section G of Part 2 in the Manual.

Notation of DEP 0-1046-023 should be entered in the Contents (page iii) and Table 1-1 (page 1-2) updated as follows:

TABLE 1-1. IMPLEMENTATION OF STANDARDS DOCUMENTS

DCS	Authority	Compliance	Approved	Effective	Applicability	Deviation Notes	Exemption Notes
0-1046-023	Division	Practice	15Oct70	15Oct70	GSD, SDD	2	E

Automatic distribution of the Manual and its supplements is not maintained.

Direct inquiries to T. B. Atkins, Extension 2449, Department 535, Standards Engineering, Building 003, Kingston.

Printed in U.S.A.

1.0 INTRODUCTION.

This section, under provision of DES 0-1046-022, defines and establishes guidelines for logic symbology used in EIS by NLT-HP engineering groups. This section provides:

a) A basis for user rules definition.

b) Diagramming techniques for generating EIS sketch sheets.

c) Logic symbology and diagramming conventions to satisfy needs of Manufacturing and MALD generation.

d) A means to develop new logic blocks by engineering designers.

Technologies other than NLT-HP may use and/or supplement this section where applicable.

Since this section forms the basis of an interface between GSD/SDD and other divisions, the needs of this interface must be guaranteed by the system manager. This responsibility includes MALD and Test generation.

Compliance with instructions given in this section is expected (see Table 1-1, page 1-2, for appropriate deviation procedure).

2.0 RECOMMENDATIONS.

2.1 FORMAT.

The format of the EIS-ALD is as described in the EIS User Manual, Chapter 30, Section 20.

2.2 BLOCK TYPES.

There are presently eight different types of ALD blocks available. They are: (1) N-normal, (2) L-logic, (3) T-thru, (4) S-service, (5) C-component, (6) R-resistor, (7) D-descriptor, and (8) X-unused pins. The block-type character is placed in the top edge of the block to the left. The use of each block is explained in the EIS User Manual, Chapter 30, Section 30.

Each of the block types contain fields whose location within a block and their length are determined by user defined rules. Figure 2-26 show the block types, their formats and field lengths that pertain to the NLT-HP technology.

2.2.1 Block Format and Contents. The block format rules are:

a) The block function - first item in line 1.

b) The block rule (BRUL), block hardware code (BHC) and block representation (BRC) should be contiguous and in that order. All three of these items concatenated form the basis for the circuit rule.

   The BRUL is four characters long. The format and nomenclature is indicated in the EIS User Manual, Chapter 60, Section 20.

c) The unit type (UTP), portion (P) and subportion (SP) fields or their equivalents should be contiguous and in that order. Their purpose is to uniquely identify an elementary unit circuit.

d) The physical location of the elementary unit should be placed on the last interior line of the fixed fields.

   For NLT-HP circuits, this field will give the chip location on an MCM. The full MCM location of 7 characters will be given in the location field of the title block.

e) The F and DESC field will be located in the top edge of the block to the immediate right of the block-type character.

f) The print position (PPP) field will be in the bottom edge of the block to the left.

g) The block serial (BS) field will be in the bottom edge of the block to the right.

h) Text may appear below the location field. The effect of block text on MALD generation is presently unknown.

2.2.2 Descriptor Type Blocks. The outline of the descriptor (D) block will be shown whenever it is used.

2.3 BLOCK SYMBOLS.

Any symbols previously addressed by existing logic standards and practices or addressed by this practice are to be used. Any symbols not covered by these will be permitted if either its block rules structure is given in terms of standard symbols or FE/TEST ENGINEERING concurs with its block rule.

2.3.1 Block Periphery. Lines entering and/or leaving a block may require:

a) Edge of block (EOB) character.

b) Bundle pin (logic pin).

c) English pin.

d) Physical pin.

e) Strand names.

f) Bundle naming character.

g) Support area flags.

h) Block title.

Figure 2-27 shows the positions of the above peripheral information. The formats of the various fields are as defined in the EIS User Manual. The field lengths are technology dependent.

2.3.1.1 EOB Characters. These characters are described in CES 0-1046-003 and -005.

2.3.1.2 Bundle Pin. All engineering ALD blocks will show letters (with or without numerals) adjacent to the logic symbols on all input lines and numerals next to the logic symbol on the output lines. This line information is referred to as bundle pins. Refer to paragraph 2.5 for bundling techniques.

The logic pins are the individual inputs and outputs of a block to which strands of a bundle are connected. All logic pins within the same logic group character (LGR) must have the same English pin and EOB character.

The field length for both the bundle pin and logic pin field is two characters for NLT-HP.

2.3.1.3 English Pin. The line function or dependency notation is associated with each logic pin by means of the English pin. The field length for NLT-HP is three characters. The following is a list of defined English pins with references as to their usage:

a) S and R: Set and Reset.

b) J and K: Set and Reset (complementary).

c) T: Complement.

d) CD: Controlled data input.

e) C: Control line for data.

f) Gn: Gating dependency.

g) Numerals: Decimal weights (decoder usage) or dependency (dependent lines).

h) Z: Common line. See paragraph 2.3.4.

i) L: Special function indicator. See paragraph 2.3.2.

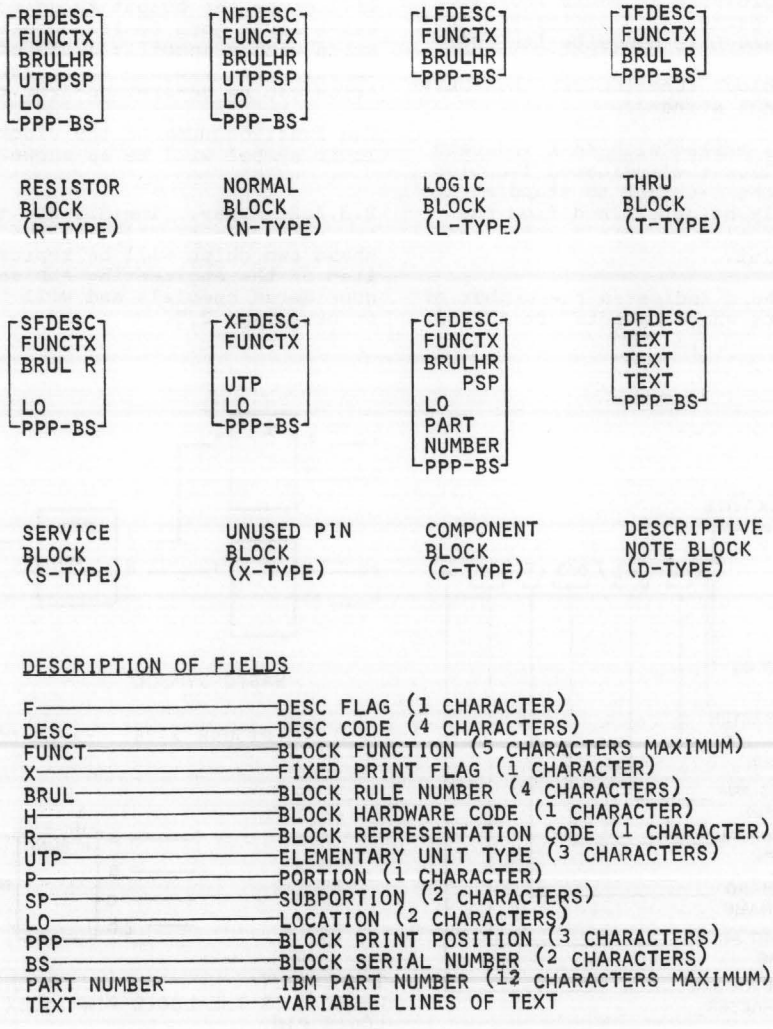
Note: See DES 0-1046-019 for details of items a through g.

2.3.1.4 Physical Pin. This field is hardware dependent and technology defined. The pin may be located either adjacent to the block or in the form of listed information.

2.3.1.5 Strand Names. Care should be taken in assigning strand names to avoid ambiguity on a sheet. The field length for NLT-HP is two characters per strand name. Particular caution should be noted in the use of the blank strand and another named strand used in the same bundle. It is recommended that:

a) A blank strand name be used only on single-strand bundles.

b) Non-blank names be assigned to all strands in a multi-strand bundle.



DESCRIPTION OF FIELDS

F	DESC FLAG (1 CHARACTER)
DESC	DESC CODE (4 CHARACTERS)
FUNCT	BLOCK FUNCTION (5 CHARACTERS MAXIMUM)
X	FIXED PRINT FLAG (1 CHARACTER)
BRUL	BLOCK RULE NUMBER (4 CHARACTERS)
H	BLOCK HARDWARE CODE (1 CHARACTER)
R	BLOCK REPRESENTATION CODE (1 CHARACTER)
UTP	ELEMENTARY UNIT TYPE (3 CHARACTERS)
P	PORTION (1 CHARACTER)
SP	SUBPORTION (2 CHARACTERS)
LO	LOCATION (2 CHARACTERS)
PPP	BLOCK PRINT POSITION (3 CHARACTERS)
BS	BLOCK SERIAL NUMBER (2 CHARACTERS)
PART NUMBER	IBM PART NUMBER (12 CHARACTERS MAXIMUM)
TEXT	VARIABLE LINES OF TEXT

FIGURE 2-26. NLT-HP BLOCK TYPE DEFINITIONS

Such practices provides these advantages:

The single-strand bundle is uniquely indicated.

Locating a particular strand in a multi-strand bundle will be easier.

2.3.1.6 Bundle Naming Character. This character is used to identify which bundle pin names a bundle. The character is printed for input naming pins and for output non-naming pins. See paragraph 2.5.3 for bundle naming techniques.

2.3.1.7 Support Area Flags. These flags are pointers to listed data. See EIS User Manual, Chapter 30, Section 20.

2.3.1.8 Block Titles. These titles are required per CES 0-1046-003 and -005.

2.3.2 L English Pin. The L pin may be used to denote lines to or from a logic function that add special characteristics beyond the indicated function. It should not be used if the special characteristic has already been defined as a logic function.

The input lines (one or more) are at their indicated polarity for the block to perform its indicated function. When any input marked L is opposite its indicated polarity, the block no longer performs its indicated function. The block function can then only be determined from the block structure.

Output lines (one or more) marked with an L indicate that the line does not follow the indicated function. The function that causes the L-output to stand at its indicated polarity can only be determined from the block structure. The exception to this is when the line is used as a test point.

2.3.3 n A*OR, n OR*A. The n indicates the number of AND circuits or OR circuits whose outputs are AND'ed or OR'ed. Separation of the individual AND or OR circuits is indicated by the use of a different logic pin group character for each circuit. See Figure 2-28.

2.3.4 Block Indexing. Block indexing can be done with identical blocks of the same function. A line function designation of Z is to be used to indicate a line common to all circuits. If the common line has a functional English pin, the Z will preceed it. A colon delineates the number of individual circuits from the function of each circuit. See Figures 2-29 and 2-30.

2.3.5 Additional Logic Symbols.

2.3.5.1 Clock Chopper - "CC". A clock pulse generator whose output will stand at its indicated polarity for a short duration whenever the input goes to its indicated polarity.

If the input goes to its opposite polarity before the pulse time is completed, the output will go to its opposite polarity (shortening the pulse).

The clock chopper may have an additional mode. A special input with a function designation of L (Level) will cause the output to go to indicated polarity when the L input goes to its opposite polarity in combination with a specific state of the clock chopper input. The detailed explanation of the circuit operation can be determined from the block rule structure.

The function name of the clock chopper is CC. The logic symbol will be as shown in Figure 2-31.

2.3.5.2 Array. The NLT-HP technology provides for two storage-type chips: 128 x 1 and 8 x 8. Each of these two chips will be represented as a one block item on the engineering ALD sheet. The blocks are considered specials and will be handled as indicated in paragraph 2.3.

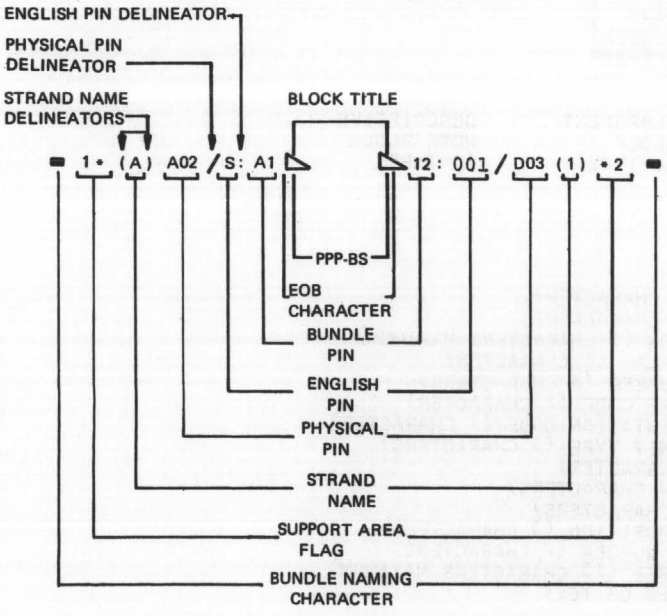


FIGURE 2-27. BLOCK PERIPHERARY NOTATION

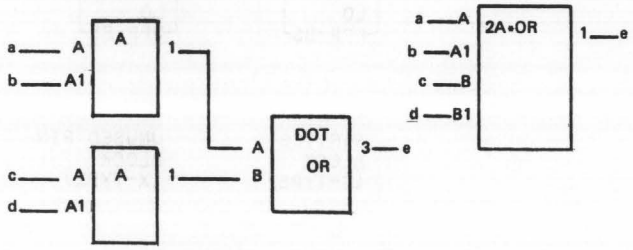
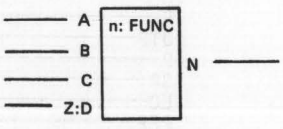


FIGURE 2-28. nA*OR CONSOLIDATION



THE OUTPUT: Nk = Ak (FUNCTION), Bk (FUNCTION), Ck -- WHERE k IS THE LOGIC PIN INDEX AND N IS THE OUTPUT LOGIC PIN.

FIGURE 2-29. BLOCK INDEXING METHOD

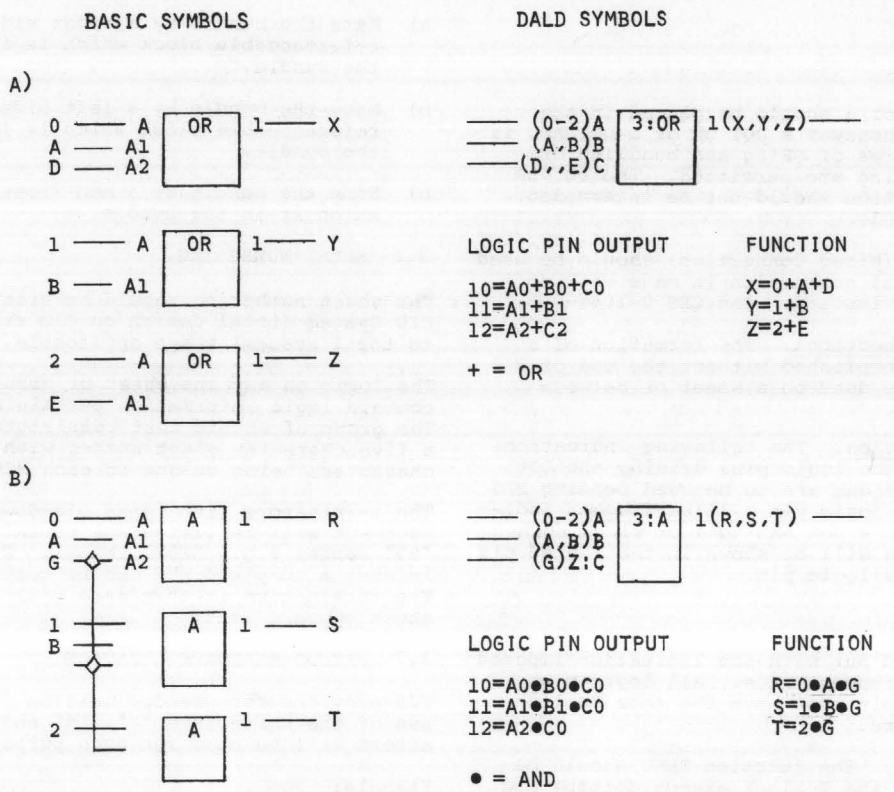


FIGURE 2-30. BLOCK INDEXING EXAMPLES

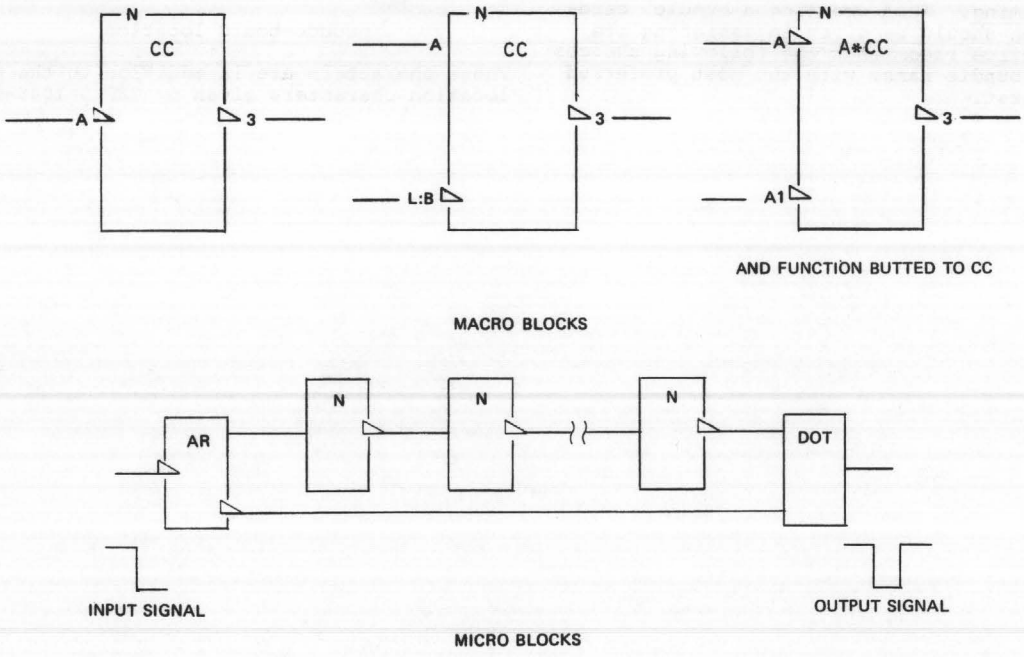


FIGURE 2-31. CLOCK CHOPPER SYMBOLS

2.4 DOTTING.

2.4.1 T-Block Usage.

a) The function OR or A should be placed in the function field whenever a DOT OR or a DOT AND is intended. Mixtures of ORing and bundling or ANDing and bundling are permitted. The DOT OR and DOT AND function should not be intermixed. See CES 0-1046-003.

b) The function WC (Wired Connection) should be used when an electrical connection is made with no logical function implied. See CES 0-1046-003.

2.4.2 Blockless Connections. The formation of a DOT or WC may be accomplished without the use of a T-block. This can be done on a sheet or between sheets.

2.4.3 Dot/WC Indication. The following indications are to be placed on the logic pins driving the Dot or WC. These indications are to be used pending EIS support. The source logic pin will be flagged indicating a dot OR (DO), a dot AND (DA) or wired connection (DW). The flag will be shown in the listed pin field adjacent to the logic pin.

2.5 BUNDLING.

Bundling is permitted but with the limitation imposed by the logic pin assignment; i.e., all logic pins defined by a bundle pin must have the same English pin and EOB characters.

2.5.1 T-Block Usage. The function THRU should be used for all uses of the T-block except dotting and WC. These include bundling, unbundling and re-naming.

2.5.2 Blockless Formation. The formation of a bundle can be done without the use of a T-block. Bundling between sheets is permitted.

2.5.3 Bundle Naming. When creating a bundle, careful consideration should be given in assigning its name. This practice recommends the following choices in establishing bundle names with the most preferred choice listed first.

a) Name the bundle by a right side pin of a cross-referenceable block which is in (or will be in) the bundle.

b) Name the bundle by a left side pin of a cross-referenceable block which is in (or will be in) the bundle.

c) Name the bundle by a non-cross-referenceable pin which is in the bundle.

2.6 SHEET NUMBERING.

The sheet numbering should be oriented towards a one CID System (total design on CID from elementary unit to total system) where applicable.

The logic on any one sheet or group of sheets should contain logic information pertaining to only one MCM. The group of sheets that consistute an MCM will have a five character sheet number with the first three characters being unique to each MCM.

The terminators (including tie-downs) associated with each MCM will be listed and contained on sheets in the "90" range; e.g., NA390, NA391. The exception to this is when a complete MCM can be contained on one sheet. The terminators in this case will be listed in the sheet support area.

2.7 PSEUDO-HARDWARE LOCATION.

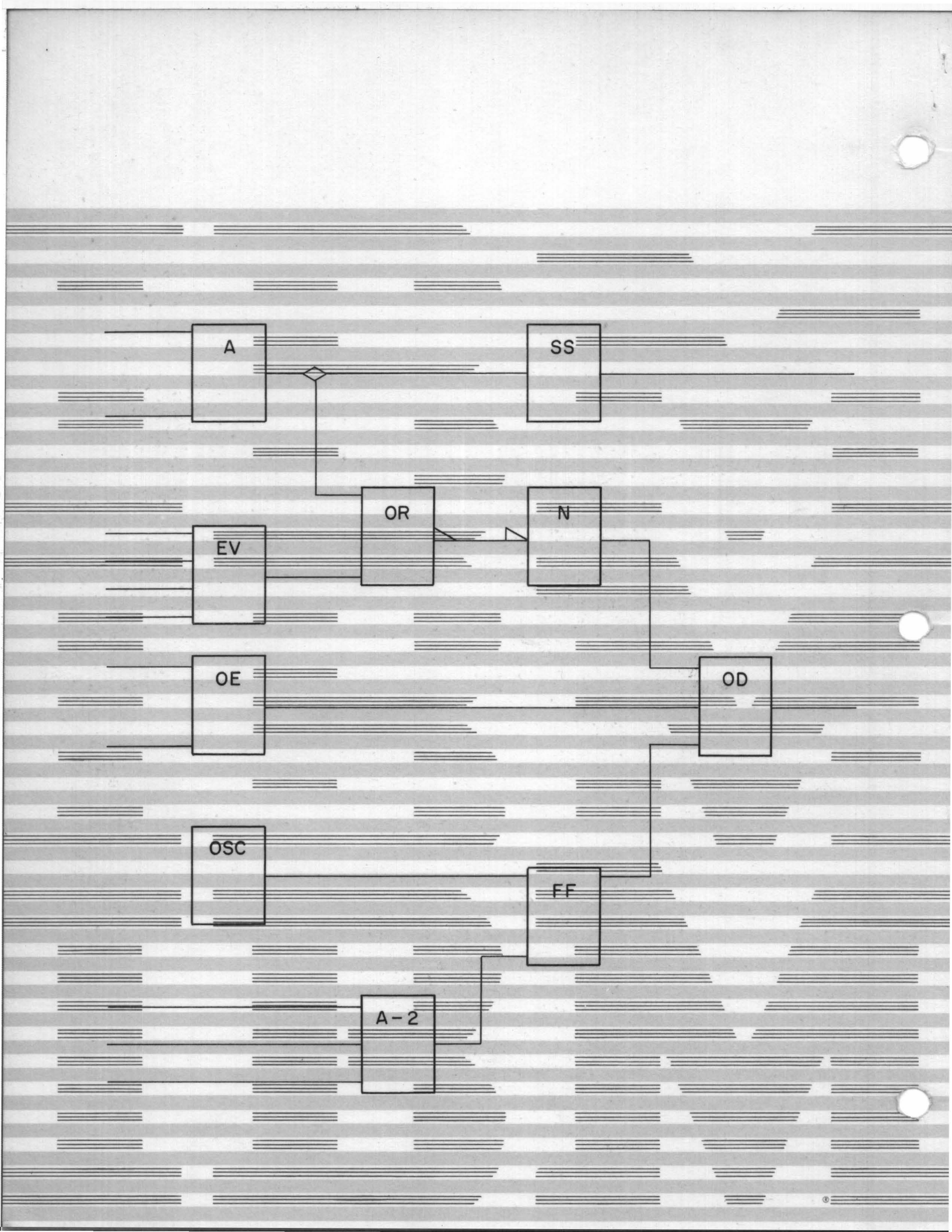
EIS provides for pseudo location indication by the use of the characters "?", "%" and "&". These characters will be used for such purpose.

Example:

1) 1 ? - A1M2
   pseudo-gate location

2) 1A - %1M2
   pseudo-board location

These characters are in addition to the present pseudo location characters given by CES 0-1046-011.


A
SS
OR
N
EV
OE
OD
OSC
FF
A-2