IBM® Customer Engineering

Reference Manual

737 Magnetic Core Storage

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737.11.00 DP PREVENTIVE MAINTENANCE GUIDE AND RECORD

PREVENTIVE MAINTENANCE GUIDE AND RECORD

737

CORE STORAGE UNIT

SERIAL | SUFFIX | DATE INSTALLED

CODE NO. FOR 737 REF. MANUAL

FREQUENCY OF INSPECTION IN MONTHS

YR. →

MO. →

VISUAL CHECK OF PULSE AMPLITUDE TIMING AND DURATION	RESET BUFFER REG & SAR	
	SAR RI AND TURN ON RD BIAS GATE	
	TURN ON READ GATE	
	TURN OFF RD & RD BIAS GATES	
	TURN ON INHIBIT AND WRITE GATE	
	TURN OFF WRITE GATE	
	TURN OFF INHIBIT GATE	
	RO SAMPLE	
	RI SAMPLE	
	READ GATE	
	READ BIAS GATE	
	WRITE GATE	
	INHIBIT GATE (ONES)	
	INHIBIT GATE (ZEROS)	
BIAS TEST OF D. C. VOLTAGES	−160	−144
		−176
	+220	+198
		+242
	−250	−230
		−263
	−100	−90
		−110
	−30	−27
		−33
	−130	−117
		−143
	MSD REF	
	DPD REF	
RIPPLE CONTENT OF D. C. VOLTAGES	MSD REF	
	DPD REF	
	MSD BIAS	
	DPD BIAS	
	SENSE AMPL BIAS	
AIR FILTER		

PREVENTIVE MAINTENANCE GUIDE

737— CORE STORAGE UNIT

Pulse Amplitudes and Timings

Freq. Time
3 mo. 1 hr.

Lower Level	-25v to -30v
Upper Level	+10v minimum
Duration	0.4 μs ±0.1 μs at half amplitude

Driver Pulses:
(Nominal values measured at 50Ω 25w, 1% resistors.)

Name	Rise	Fall	Duration	Amplitude
Read Drive	0.4 μs	0.3 μs	2.0 μs	20.5v
Read Bias Drive	0.5 μs	0.5 μs	3.0 μs	21.0v
Write Drive	1.0 μs	0.6 μs	3.0 μs	20.5v
Inhibit Drive (ones)	0.6 μs	0.3 μs	1.0 μs	20.5v
(zeros)	0.6 μs	0.3 μs	5.5 μs	20.5v

X and Y Drive Pulses (measured across terminating Resistors)

Name	Rise	Fall	Duration	Amplitude
Read	0.5 μs	--	2.0 μs	*
Write	--	0.7 μs	2.0 μs	*

*Voltage drop across terminating resistors should be such as to insure 410 ma (±10ma) of driving current.

Ripple Content of DC Voltage Supplies at Storage Frame

12 mo. .4 hr.

Once in each period of 12 months, check the ripple content of each supply measured at core frame.

Supply	Max. Allowable Ripple
+220v	2.5v Peak to Peak
+150v	5.0v Peak to Peak
+ 15v	5.0v Peak to Peak
- 30v	5.0v Peak to Peak
-100v	5.0v Peak to Peak
-250v	5.0v Peak to Peak
-130v	5.0v Peak to Peak
-100v Delayed	5.0v Peak to Peak
MSD Ref.	1.5v Peak to Peak
DPD Ref.	1.5v Peak to Peak
MSD Bias	2.0v Peak to Peak
DPD Bias	2.0v Peak to Peak
Sense Ampl. Bias	1.5v Peak to Peak

Bias Limits on DC Voltages

1 mo. .3 hr.

Each month bias tests should be performed for one minute of error-free operation at each limit. The following limits apply for each voltage using 4S06:

Nominal Voltage	Recommended Test Limits
+150	+142, +162
+220	+198, +242
-250	-230, -263
-100	- 90, -110
- 30	- 27, - 33
-130	-117, -143
-160	(738 CSU) -144, -176

Air Filters

2 mo. 0.3 hr.

Inspect air filters and replace all those that will impede air flow because of dirt.

737.13.00 LUBRICATION CHART

CODE NO.	ITEM	TYPE OF LUBRICANT				
		6	9	12	17	22
02	Cover and Door Hinges		X			
02	Cover Latch Cams				X	
08	Bias Reset Duo Relay Pivots (Pipe Cleaner)		X			
08	Bias Reset Duo Relay Operating Pad (Light Film)				X	

737.14.00 CLEAN AND INSPECT

737.14.01 General Heat Problems

Refer to section 704.14.01 for heat problems on core storage.

737.14.02 Appearance and Filters

Clean any large accumulations of dust or dirt with an approved vacuum cleaner. Clean all covers with the IBM polish. Check all covers for good latching and unlatching. Check core frame panel air filters and also the core array filter for good air flow. Replace any filter that is dirty. Do not try to clean or recondition any filter.

737.14.03 Motors and Blowers

Tube Panel

With power down be sure all motors and blowers are free to turn. With power up be sure all motors and blowers are running. Check all panels for a good flow of air and be sure there are no hot spots. Check for quiet running operation and for any hot bearing. Methods to check for temperatures of operating conditions are found in section 704.14.01.

Array Blower

With power down be sure fan is free to turn without any binds. Remove side cover with power on and check to see if blower is in operation. Check for hot spots in the right end panel and be sure blower is running quiet. Check air filter and replace when dirty. Methods for checking all temperatures are given in section 704.14.01.

737.14.04 Pluggable Units and Panel Pins

Pluggable Units

Some jumper wires between pluggable units are too tight. Check to see if the insulation is broken and occasionally grounding out on these jumper wires.

Panel Pin

Check for spread and misaligned panel pins. Some crack and break near bottom of the contact area. These should be checked each time a pluggable unit is removed from the machine.

I/O Shoes, Receptacles and Connections

Check for bent, broken or dirty contacts. Check for loose, grounded or shorted connections.

Prongs and contacts are cleaned by wiping with a cloth or finger or using an approved cleaning solvent. Never burnish, sand, file or stone the contacts for the contact surface may be removed.

737.14.05 Thermals

Check thermal contact alignment and clean points for a good "make" surface. Make sure power is knocked down when contact points operate. Check connections to see they are not loose, grounded or shorted. The thermals are set to operate at 131° ± 5° F. Make sure that with all covers off, the thermal will operate and knock down power. Section 704.14.05 contains the description and adjustments of thermals.

737.14.07 Keys, Buttons, Switches and Test Panels

CE Test Panel

Check test lamp, stop lamp and all neons for proper operation. Check all keys and switches to see the correct operation is completed by each. With the test switch on, the storage unit shall automatically cycle through all addresses. If the check stop switch is on, and an error is detected, the unit shall stop with the check stop neon on, the addresses of the error is displayed on the test panel address neons and the error word displayed on the storage buffer register neons. Depressing the check stop reset key resets the check stop neon and allows the test to continue. The test panel circuits shall be capable of detecting an error in any column or in any storage location of the storage unit.

The reset to ones key on the CE test panel is capable of resetting all storage locations to ones regardless of the previous contents of the storage locations. The reset to zeros key on the CE test panel is capable of resetting all storage locations to zeros regardless of the previous contents of the storage locations.

Check back of panel for loose, grounded or shorted connections.

MSD Adjust and DPD Adjust

Check to make sure handle is free of binds when power is off. When power on check that both adjustments can reach both limits of the MSD voltage and DPD voltage. Limits are given in section 737.15.16.

737.14.08 Bias Reset Relay

Check for the following: (1) Core firmly secured to the frame, (2) Loose or burned contact points, (3) Contact point alignment for greatest contact area, (4) Contact pile holding screws tight, (5) Clean contact points. For a complete preventative maintenance routine, refer to section 704.14.07.

737.14.09 Resistors, Capacitors and Inductors

Filament Transformers and Capacitors

Check for loose, grounded or shorted connections. Make sure there is no accumulation of dirt grounding out the transformers or capacitors. Make sure capacitors have not popped their expansion plugs.

Terminating Resistor Panel

Check for any hot or burned resistors. Check for any loose, grounded or shorted connections. An extremely hot resistor can be found by the burning odor it gives off. To check operating temperatures, see section 704.14.01.

Driver Panel Choke and Resistors (CF 3 and 4)

Check for any loose, grounded or shorted connections. Make sure they are operating at normal temperature. Methods of checking temperatures are found in section 704.14.01.

Timing Pulse Terminal Resistors

Check for loose or burned connections. Check resistors for excess heat and blown or burned spots. Temperature checking procedures can be found in section 704.14.01.

Matrix Switches

Check matrix switch panels for loose, grounded, or shorted connections.

737.14.10 Delay Lines and Rectifiers

Check for any loose, grounded or shorted connections. Scope input pulse and output pulse to be sure delay lines meet the limits of each.

737.14.12 Core Line Fuses

Check fuses for any discolorations or unnatural appearance. Check for loose or high resistive soldered connections. If more than one address is in error, be sure to check fuses, for at times they are overlooked.

737.14.13 Block Tube Testing

Block test only after biasing and pulse checking fail to locate general failures. An occasional visual check should be made for open filaments on parallel cathode followers. A block tube check should be made periodically of the master oscillator assembly.

737.14.14 Vibration Testing

Vibration testing should be done where there is no other means of locating a trouble. The trouble area should be the only section vibrated and the machine checked thoroughly after vibration to be sure no other troubles have been added. However, the 737 core storage unit must be capable of performing all normal operations without failure while the pluggable unit panels, driver panels, and pluggable units are vibrated in a manner sufficient to detect any faulty electrical connections or components.

Since the 6136 tubes cannot be biased, a scheduled vibration test should be made of them. While running a pick-up and drop-out storage test, the 6136 tubes and components should be vibrated in a manner to detect any bad or weak components. To effectively vibrate a 6136 tube, the tube should be tapped lightly with your finger or a pencil eraser. Never vibrate any harder then described above.

737.14.15 Pulse Checking

A scheduled procedure must be set up to scope and check on critical and important pulses. These pulses will be found in section 737.15.00. Refer to that section for any scope setups, waveshapes, levels, rise and fall times that are needed.

737.14.22 Core Plane

A chart is shown in section 737.21.22 of the record which is kept of each core plane removal. It is important for machine history to find the planes replaced, failing address, and the reason of failure. This must be kept with the machine and kept up-to-date.

737.14.24 Turret Socket Terminals

Check for any loose, grounded or shorted connections on the turret side of the panel.

*737.15.00 WAVEFORMS AND LEVELS

737.15.16 Marginal Checking

Machine Service Voltages

Once each month bias tests should be made and the machine must operate error free for one minute at each bias limit. Each voltage should be biased to the following limits, and a suitable program (4S06) must run error free for one minute at each bias limit.

NOMINAL VOLTAGE	BIAS TEST LIMITS
+150	+142, +162
+220	+192, +242
-250	-225, -262
-100	-90, -110
-30	-27, -33
-130	-114, -143
-160	-144, -176

Marginal Drive Current Limits

	DPD REFERENCE	MSD REFERENCE
1.	-150v ± 1v	-147v ± 1v
2.	-150v ± 1v	-173v ± 1v
3.	-135v ± 1v	-160v ± 1v
4.	-165v ± 1v	-160v ± 1v

737.15.17 Ripple Content

Check the ripple content of the service voltages every 3 months with the oscilloscope.

SUPPLY	MAXIMUM ALLOWABLE RIPPLE PEAK TO PEAK
+220v	2.5 Volts
+150v	5.0 Volts
+15v	5.0 Volts
-30v	5.0 Volts
-100v	5.0 Volts
-250v	5.0 Volts
-130v	5.0 Volts
-100v Delayed	5.0 Volts
MSD Reference	1.5 Volts
DPD Reference	1.5 Volts
MSD Bias	2.0 Volts
DPD Bias	2.0 Volts
Sense Amplifier Bias	1.5 Volts

737.15.18 Service Voltage Regulation

Special bias voltages at the pluggable unit panel with the 4S05A or 4S06A program operating is as follows:

MSD Bias	-200 ± 2v
DPD Bias	-150 ± 2v
Sense Amplifier Bias	-15 ± 1v

The filament voltage on the pluggable unit wiring panels, measured at any point, is 6.3 ± 0.2v on each side of the transformer center tap. Filament voltage on the driver panels measured at any point is 6.3 ± 0.2v.

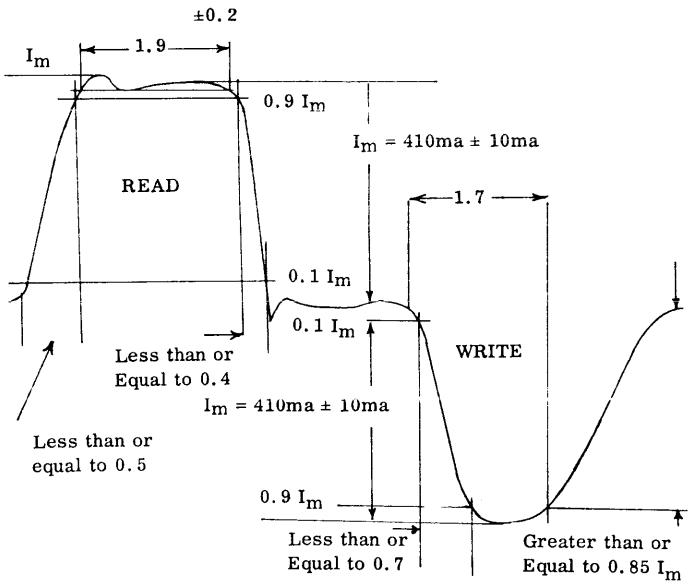
The MSD reference voltage and DPD reference voltage shall be continuously variable from -120 ± 2v to -190 ± 2v.

With the MSD reference voltage set at -160 ± 2v and the DPD reference voltage set at -150 ± 2v, the +150 volt supply is varied from $+142\ ^{-2}_{+0}$v to $+163\ ^{+2}_{-0}$v and the -250 volt supply varied from $-225\ ^{+2}_{-0}$v to $-263\ ^{+0}_{-2}$v with no more than ±1 volt variation in either reference voltage.

737.15.19 Special Pulses X and Y Drive Line Specifications Measured at Terminating Resistors

With all storage locations reset to ones and the MSD reference voltage set at -160v ± 1v, the waveforms of all (128) X and Y drive lines at the terminating resistors must meet all conditions shown in Figure 15-1.

Overshoot and sag shall not exceed 12 ma.



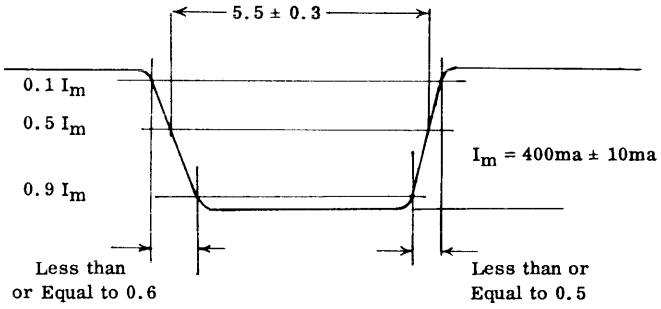
All timings in microseconds.

FIGURE 15-1 X AND Y DRIVE PULSES

Digit Plane Waveform at 50 Ohm Resistors

With all storage locations reset to zeros and the DPD reference voltage set at -150v ± 1v, the 36 digit plane waveforms at the 50 ohm resistors on the driver panels must conform to the waveform shown in Figure 15-2.

With all storage locations reset to ones, the rise time, fall time and peak amplitude of the 36 digit plane waveforms should meet requirements specified in Figure 15-2.



Note: All timings in usec.

FIGURE 15-2 Z DRIVE PULSE

Sense Amplifier Outputs

With storage reading out all zeros, the sense amplifier outputs shall be such that in the 1 microsecond period preceeding the fall of the RO sample pulse, the noise level does not exceed 5 volts.

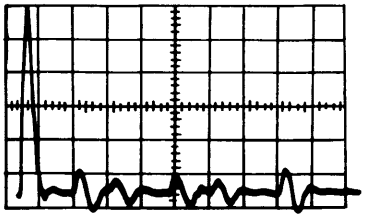
Read-Out Sample

With a complimenting checkerboard program operating, the RO sample pulse must be centered on the composite of ones signal for all sense amplifiers.

737.15.23 Core Array

When a new core storage is installed, not only should it operate at the bias limits but the core storage should be operated to find exactly the bias limits where it starts to foil. These limits should be recorded and kept with the machine. These should be checked occasionally as time permits and any steady change would indicate coming troubles. This should be kept with the machine for ready reference.

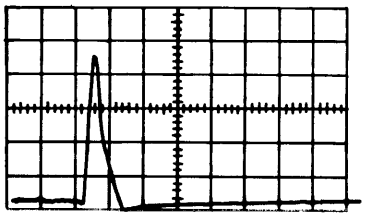
737.15.50 Sync Pulse



CE Test Panel 1.06.01
1 usec/cm 10 Volts/cm
Sync - Test Panel Sync
CLA L(0000) Cont Mem RI

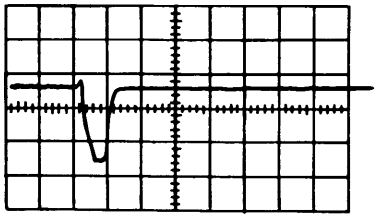
737.15.51 Turn On Read Bias & Stg Address Reg. Read In

A



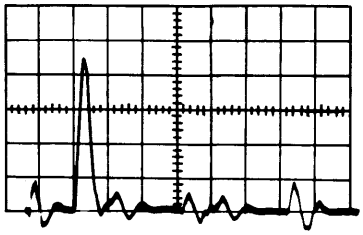
MF3-H33-1 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



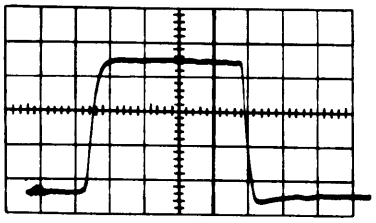
MF3-F33-7 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

C



CF2-F03-5 1.05.04
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

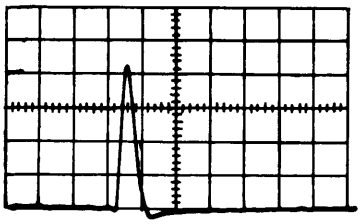
737.15.52 Read Bias Gate



CF2-D03-2 1.05.04
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

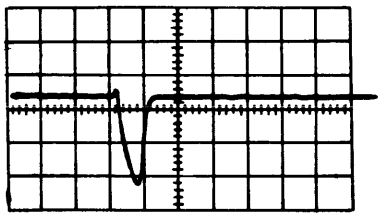
737.15.53 Turn On Read Gate

A



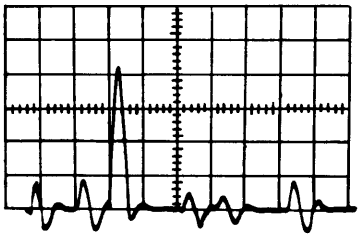
MF3-E32-1 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



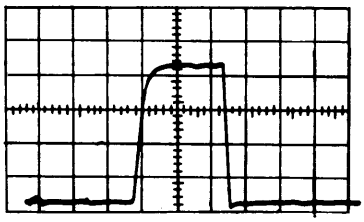
MF3-C32-8 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

C



CF2-A02-8 1.05.04
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

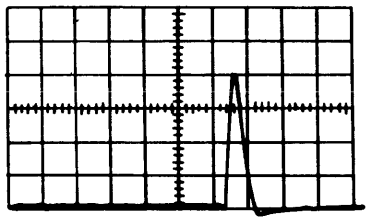
737.15.54 Read Gate



CF2-D02-2 1.05.04
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

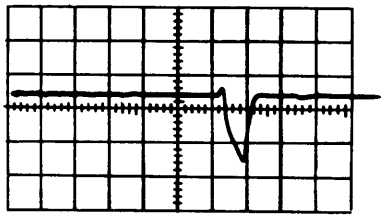
737.15.55 Turn Off Read & Read Bias Gate

A



MF3-H32-5 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



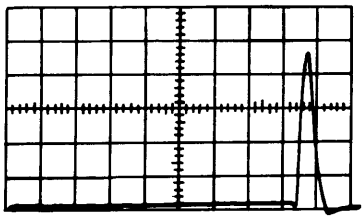
MF3-F32-3 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

C

CF2-A03-8 1.05.04
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

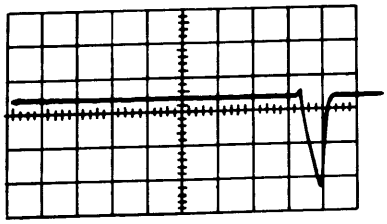
737.15.56 Turn On Inhibit & Write Gate

A



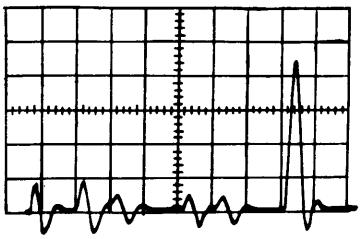
MF3-H31-5 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



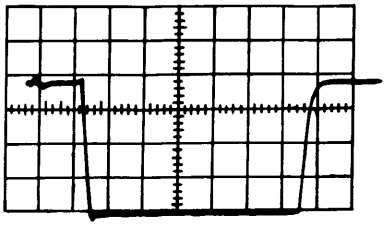
MF3-F31-3 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

C



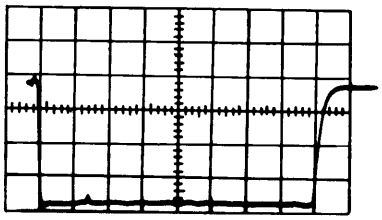
CF2-N04-7 1.05.05
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

737.15.57 Inhibit Gate



CF2-M04-4 1.05.05
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

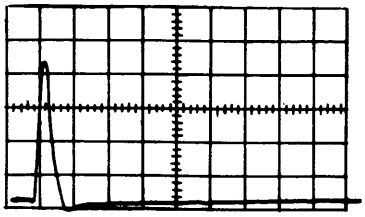
737.15.58 Write Gate



CF2-M03-2 1.05.05
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

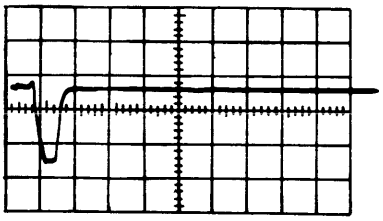
737.15.59 Turn Off Write Gate

A



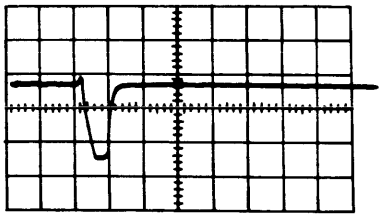
MF3-J33-7 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



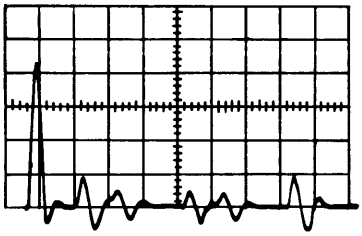
MF3-L33-1 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



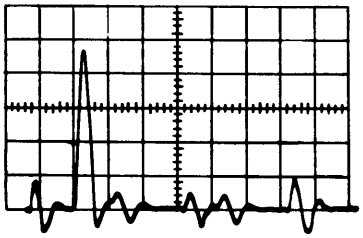
MF3-P33-7 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

C



CF2-K03-2 1.05.05
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

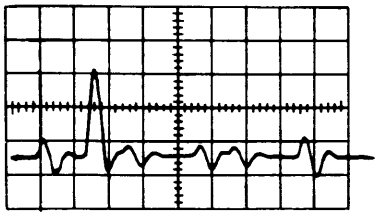
C



CF2-N04-3 1.05.05
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

737.15.60 Turn Off Inhibit Gate

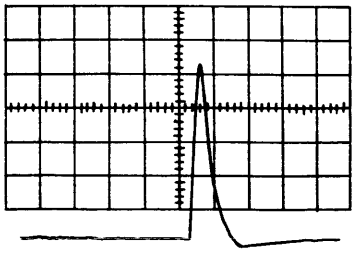
A



MF3-R33-7 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

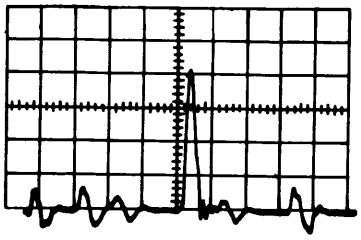
737.15.61 Read Out Sample

A



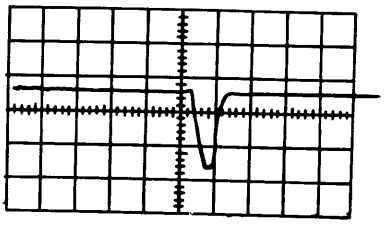
MF3-J32-8 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



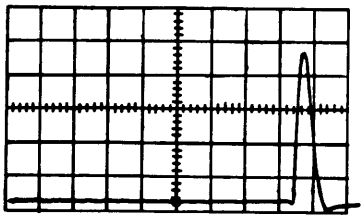
CF1-M10-7 1.03.02 Pos. 2
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

C



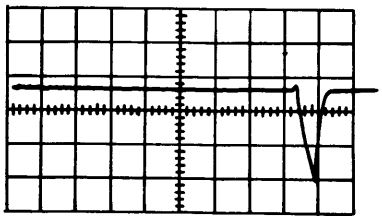
MF3-L32-1 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

737.15.62 Read In Sample
A



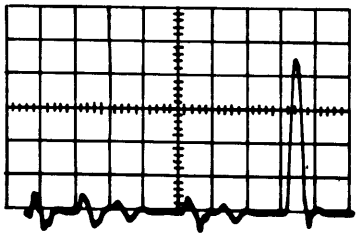
MF3-E31-1 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

B



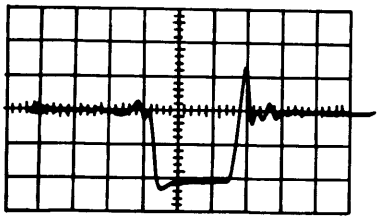
MF3-C31-8 1.05.02
1 usec/cm 20 Volts/cm
Sync - MA0
CLA L(0000) Cont Mem RI

C



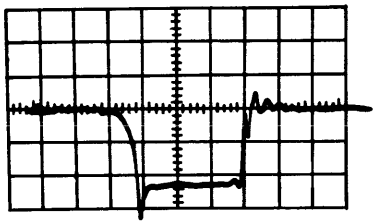
CF1-M10-3 1.03.02 Pos. 2
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

737.15.63 Read Drive - X Matrix



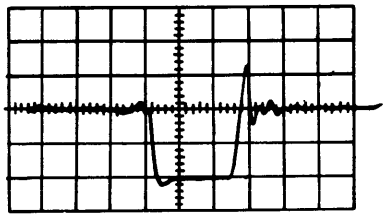
CF3-Km 1.01.08
1 usec/cm 10 Volts/cm
Sync - Sync pulse
MF1 Switch to E time - flip CE
test switch

737.15.64 Write Drive - X Matrix



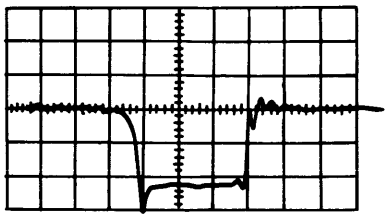
CF3-Dj 1.01.07
1 usec/cm 10 Volts/cm
Sync - Sync pulse
MF1 Switch to E time - flip CE test switch

737.15.65 Read Drive - Y Matrix



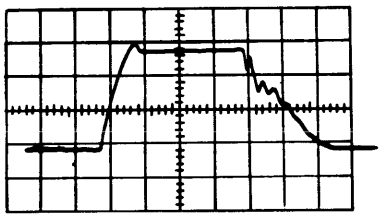
CF3-Gk 1.01.10
1 usec/cm 10 Volts/cm
Sync - Sync pulse
MF1 Switch to E time - flip CE test switch

737.15.66 Write Drive - Y Matrix



CF3-Aj 1.01.09
1 usec/cm 10 Volts/cm
Sync - Sync pulse
MF1 Switch to E time - flip CE test switch

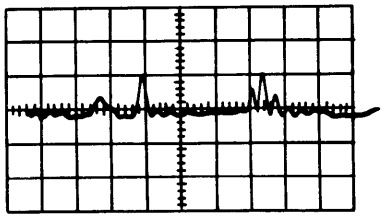
737.15.67 MSAw Output



CF1-Cj 1.01.07
1 usec/cm 20 Volts/cm
Sync - Sync pulse
-200 Volt level
CLA L(All Ones) Cont Mem RI

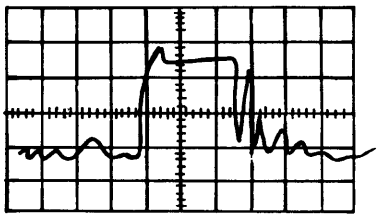
737.05.68 MSAr Output (Zero)

A



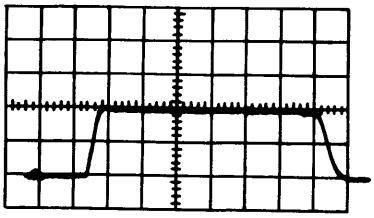
CF1-Gj 0.01.08
1 usec/cm 10 Volts/cm
Sync - Sync pulse
-200 Volt level
CLA L(0000) Cont Mem RI

B (One)



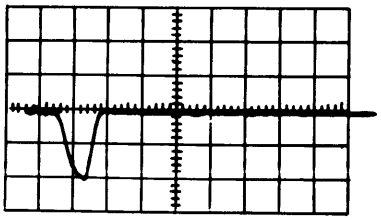
CF1-Gj 1.01.08
1 usec/cm 10 Volts/cm
Sync - Sync pulse
-200 Volt level
CLA L(All Ones) Cont Mem RI

737.15.69 Inhibit Drive for a "One" (DPA)



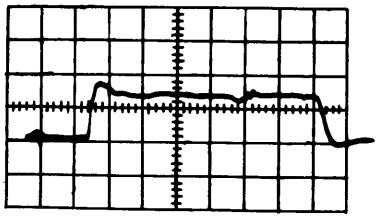
CF1-Lj 1.02.01
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(All Ones) Cont Mem RI

737.15.70 Inhibit Drive for a "Zero" (DPA)



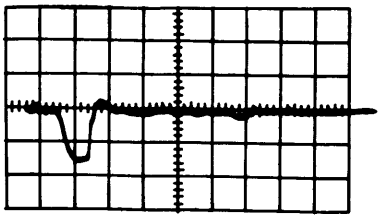
CF1-Lj 1.02.01
1 usec/cm 10 Volts/cm
Sync - Sync pulse
Sign position
CLA (0000) Cont Mem RI

737.15.71 Terminating Resistor for "One"



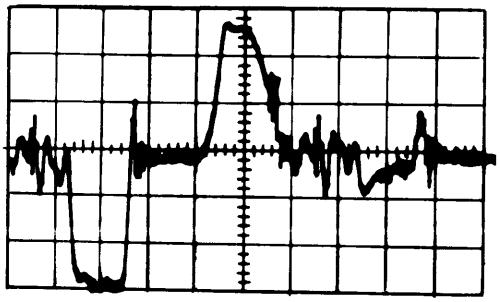
Terminating Resistor 1.02.01
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(All Ones) Cont Mem RI

737.15.72 Terminating Resistor for "Zero"



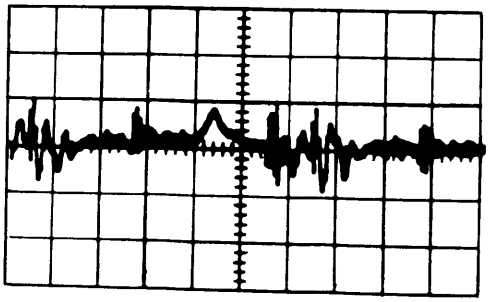
Terminating Resistor 1.02.01
1 usec/cm 10 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

737.15.73 Selected X Drive Line



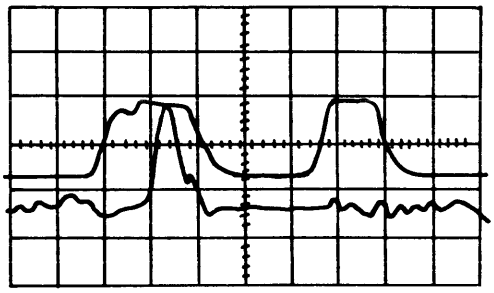
Terminating Resistor 1.01.14
2 usec/cm 2 Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

737.15.74 Non-Selected X Drive Line
(But having a common write driver with the selected line)



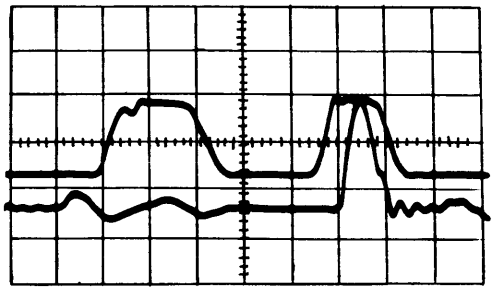
Terminating Resistor 1.01.14
2 usec/cm 2.Volts/cm
Sync - Sync pulse
CLA L(0000) Cont Mem RI

737.15.75 Sense Amplifier Output & RO Sample



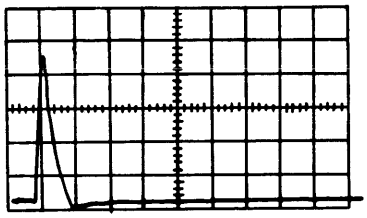
CSF1-N11-2 1.03.01
CSF1-M11-7 1.03.01
.5 usec/cm 20 Volts/cm
Sync - Sync pulse
CLA L(ALL Ones) Cont Mem RI

737.15.76 Sense Amplifier Output & RI Sample



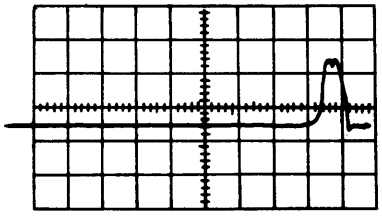
CSF1-N11-2 1.03.01
CSF1-M11-3 1.03.01
.5 usec/cm 20 Volts/cm
Sync - Sync pulse
CLA L(All Ones) Cont Mem RI

737.15.77 Reset Storage Address Reg and Buffer Reg



MF3-C33-8 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0

737.15.78 Reset Storage Address Reg and Buffer Reg



MF3-A33-1 1.05.03
1 usec/cm 20 Volts/cm
Sync - MA0

737.21.00 REMOVALS

737.21.02 Filters and Appearance

Remove the front covers from panels. The filters can be lifted out when the holding screws are loosened. The filter for the core array can be removed when the back cover nearest the array is removed. When replacing this filter, check array blower for proper operation. There is no sure way to check this blower. Before a new filter is installed, look in and make sure the blower is running.

737.21.03 Blower Motors and Blowers

The motors and blowers are held to the base by four bolts. These bolts can be removed from the under side of the base. The core array blower can only be removed after the core array has been removed.

737.21.06 CE Test Panel Components

Screws and nuts are available on the front of the panel to remove most of the switches, knobs and contacts. Unscrew red reflector from the test lamp and then push and twist counterclockwise to remove the test lamp. All neon lamps are pushed and twisted counterclockwise from the front of the panel to remove the neon bulbs.

737.21.22 Core Plane

Make sure power is down. Disconnect the sense winding and the inhibit winding. Check the inhibit color coding when removing and be sure to replace the windings in the same sequence. The inhibit winding current must be in the opposite direction to the X winding. Since the X winding direction is alternated in adjacent planes, the inhibit winding direction must also be alternated. Therefore, at the inhibit wire terminal connections, two color codes are along side of each other and not alternate as might be expected. Unsolder all the X and Y wire connections and bend completely back out of the way. This is done so when the plane is removed the unsoldered ends will not get tangled with cores and wires. Put a paper above and below the plane to be removed. Remove the four (4) screws holding the individual core planes to the frame. The core planes can be removed from any direction, but the most successful direction is out the right end from in front of the array. A light tap on the core plane should free the plane so it can be extracted.

The reverse order should be used to replace the core plane. Make sure the new plane contains the same type core as the one to be replaced. Make sure all insulation is removed from the wire ends of the new core plane to get good solder joints. Put a paper above and below the plane and slowly insert paper and plane into the proper place in the array. When the plane is in the proper position, replace the four holding screws. Care must be exercised to just snug up these screws. Overtightening or uneven tightening puts a strain on the core plane with a result that the core plane frame may crack or break.

When the end leads are soldered, there is less chance for cold solder joints if the power is down and the air conditioning in the room is stopped. With air conditioning on or the blower running, soldering cannot be done effectively. Check each soldered joint for a good contact. Replace all sense and inhibit wires and be sure to follow color code sequence. The resistance of the sense winding should be about 14 ohms, the inhibit winding about 7 ohms.

On replacing the "S" plane, the wires from the switch matrix should be labeled as they are removed. There is no color code to get them back properly, therefore, some identification should be put on each as it is removed.

737.21.23 Core Array

Remove right hand and right end covers exposing the core array. Remove eight (8) screws on the base frame. Remove all X, Y, inhibit and sense wire connections, making sure they can be replaced in the same sequence. The core array is then free to be tipped and can be lifted out.

737.21.24 Turret Assembly

Remove the 5998 drive tube of the turret to be replaced. Remove screws on each side of the base. The base and turret are free to be removed from rear of the machine by unsoldering the connection wires.

737.22.00 ADJUSTMENTS

737.22.08 Bias Reset Relay

This is relay part number 111401. The armature to core air gap is .021" with a contact gap of .012". The pick-up time is 16-20 milliseconds and drops in 3-6 milliseconds. For other adjustments, refer to section 704.22.08.

Array No. _____

Machine Type _____

Machine No. _____

Code for Rejection

A. Early fall one, Trailing edge
B. Early fall, High zero
C. High zero
D. Weak one
E. Weak one, Early fall
F. Mechanical defect
G. Miscellaneous

Test Rejected On

1. Memory Frame Test
   a. Normal
   b. +
   c. –
2. Memory Frame Test with checkerboard
   a. Normal
   b. +
   c. –
3. Main Frame
   a. Normal
   b. +
   c. –

Date Ret.	Plane No.	Addresses			No. Cores	Reason for Rejection							Test Rej. on	Comments
						A	B	C	D	E	F	G		

FIGURE 22-1. CORE PLANE REPLACEMENT CHART

737.31.00 DIAGNOSTIC FORMAT

The diagnostic tests for core storage are written to follow the general routines of 4 DEPR. The sense switches control similar things in each test and the print-outs use similar routines. Each will be discussed under the appropriate program. Load routines needed for each of these are discussed at length in 704.33.00.

737.32.00 CORE STORAGE TESTS

737.32.01 Core Complement Checkerboard Reliability - 4S05, 4S06

Method of Testing

The program writes a complete pattern in core storage and checks each word that is written. It complements the pattern, checks each word that is complemented and then restores the pattern to the original written program. After one complete pattern is read, the program writes and checks the inverse pattern.

Core Storage Pattern

The core storage is tested by putting the following pattern into core storage.

```
00110011
00110011
11001100
11001100
00110011
```

As the actual program locations differ from the physical locations, a memory print-out will show blocks of memory like this.

```
   0 . . . . 20 . . . . 40 . . . . 60 . . . . 77
   .                                           .
   .  0 S       1 S       0 S       1 S        .
   .                                           .
   .                                           .
2000 . . . 2020 . . . 2040 . . . 2060 . . . 2077
   .
   .  1 S       0 S       1 S       0 S
   .
   .
4000 . . .
     0 S       1 S
```

Sense Switch Control

Switch 3 up - print out on error.
Switch 3 down - stop on error.
Switch 6 up - will load next program from the card reader.
Switch 6 down - continuous repeat.

Print-Outs

The first line of the print-out contains the address of the word in error and the error word. The second line contains the indication as to whether it is an initial or complement error and the correct word. The first position of the word is the sign position.

Example 1

```
010111011          11111111111111111111111111101111111
                   11111111111111111111111111111111111
```

In example 1 an initial error occurred at address 273. All ones should have been written. The error word has dropped a one in position 28.

Example 2

```
010111011          00000001000000000000000000000000000
          111111111 00000000000000000000000000000000000
```

The group of ones in front of the correct word in the second line indicates that it is a complement error. The first line print-out gives the error address of 273 and the error is a one bit in position 7 of the word.

Diagnostic Differences

Program 4S05 is loaded into the first 200 locations in storage and tests all of the available storage above 200. Program 4S06 is loaded into the last 200 locations available in storage and tests all of the rest of storage. Both programs (4S05 and 4S06) are run to check all of the storage area. These programs are used with any number of 737 core storages. The programs test for the size of storage and adjusts the program accordingly. The test wipes out the area which is used to test the size of storage. The test words used in this test are located at positions 165 and 166 in 4S05 and positions 77763 and 77764 in 4S06. These two test words alternate through the normal operation of the test.

Remove the 4S05 transfer card punched 4S05 010 and the two blanks punched 4S05 011-012 and insert the tape transfer card and the tape control card punched 4S05 013 and 014 to place 4S05 on tape. Remove the program transfer card punched 4S06 010 and two blanks punched 4S06 011-012 and place cards punched 4S06 13, 14, 15, 16, behind 4S06 loader. Place tape transfer card punched 4S06 017 behind these followed by tape control card punched 4S06 018 to place 4S06 on tape.

The high binary loader 4M27 is used to load 4S05 and the low binary loader 4M16 is used to load 4S06 into core storage.

Diagnostic Characteristics

The program takes about two seconds to make a successful pass in one core storage. The program may fail due to an alteration in the program itself due to a storage failure. If a pattern other then all ones or all zeros is desired in this test, just change the two test words and run the test. The program will run correctly for any test words.

737.32.02 Half-Select Beat Test for 737 Core Storages - 4S11, 4S12

Method of Testing

The program stores zeros in every position of core storage except the program area which contains the test. Each address in turn is written with a test word a number of times and 16 addresses are checked to see if they still retain the zero. The 16 addresses which are checked are those most likely to pick

up a bit during write time. They are the cores that share the same select line as the test address and also share the select lines which contain noise from the core drivers at write time. With sense switch control it is possible to beat each address 20, 100, or 500 times.

Diagnostic Characteristics

The program is designed to give the customer engineer a choice in the method of testing the machine. The test word can be changed and the rotation count can be changed to satisfy any conditions.

To test each core only one time is a complete pass using test word 010101010101, put a 6 in location A9 of test. This will require approximately 1-1/2 minutes to make a complete pass. For maximum speed, although maybe not the worst test, put a 1 in location A9 of test and -377777777777 in location A1 of test.

The constant at A9 which is location 167 for 4S11 or 17764 for 4S12 is chosen as 44 to insure that every core is beat for any test pattern. Any test pattern can be used at A1 which is location 170 or 17765 to test storage. If only one binary bit exists in the test word at A1, a number 1 at A1, all cores are tested except the sign positions of each word. Therefore, it is recommended that the test word at A1 always contain at least two binary bits, a number such as 100001 at A1, to insure that the sign position is always checked.

The speed of the program is 7 minutes per pass when run with sense switches 4 and 5 up. This gives 20 beats per address using the test word of 010101010101. This test word will cause every core to be tested 6 times in a complete pass.

Sense Switch Control

Switch 1 up - continue the diagnostic assuming it is a 4K storage if an error occurs in testing the size of storage.
Switch 1 down - if an error occurs in testing size of storage repeat testing the size of storage.
Switch 4 up - beat each address 20 times.
Switch 4 down and 5 up - beat each address 100 times.
Switches 4 and 5 down - beat each address 500 times.
Switch 6 up - will load next program from card reader.
Switch 6 down - continuous repeat.

Diagnostic Differences

4S11 tests any number of 737 core storages. It loads into the lowest storage positions. It tests for the size of storage and adjusts the addresses accordingly. The test wipes out the part of the program which tests for size of storage. 4S12 is used with any number of 737 core storages, however, it tests only one or two core storages. It loads into the highest storage positions of either one or two core storages.

To place 4S11 on diagnostic tape remove 4S11 program transfer card punched 4S11 010, and two blank cards, 4S11 011-012. Replace these cards by 4S11 tape transfer card 4S11 013, and tape control card 4S11 014. To place 4S12 on diagnostic tape remove 4S12 program transfer card 4S12 008, and two blank cards 4S12 009-010. Behind 4S12 loader place cards 4S12 011-012-013-014, tape transfer card 4S12 015 and tape control card 4S12 016.

737.32.03 Core Storage Diagnostic - 4S17H, 4S17L

Method of Testing

Test of Ability to Select any Storage Location (Storage Deflection). A one (1) is stored and then brought out and added to a starting address which is then stored at this address. The contents of each address contains the location of the address. A transfer is initiated to each address and these locations are tested for the correct word and correct address. The deflection section of the test is written for stopping on errors without any print-outs. If an error halt occurs and the error word which appears in the MQ shows the error in the address portion, the correct address is not shown as stated on the listing. However, the correct address does appear in the accumulator.

Ones and Zeros. Ones are stored in every location in core storage. Each location is tested for ones. Zeros are stored in every location of core storage and each location is then tested for zeros. Errors are printed out on one line as shown below. The error and error address are printed in binary. The position in error is determined by the inconsistent bit. The first position in the error word is the sign.

The example shows that position 14 failed to read or write a one at address 03674.

011110111100 111111111110111111111111111111111

Random Number Test. Random numbers are stored in every location in storage and then each address is tested for the correct random number. Errors print-out in two lines and will print in the same form as before except that two lines will print, giving the error address and error word on the first line and the correct word on the second line.

Sense Switch Control

Switch #1 up	Go to next section of program.
Switch #1 down	Repeat present section.
Switch #3 up	Print on error.
Switch #3 down	Halt on error.
Switch #4 up	Test switch #5.
Switch #4 down	Test zeros only.
Switch #5 up	Alternate ones and zeros.
Switch #5 down	Test ones only.
Switch #6 up	Load next program from card reader.
Switch #6 down	Repeat complete test.

Switches #4 and #5 are used in ones and zeros only while switch #3 is not used in the deflection section.

Sense Lights

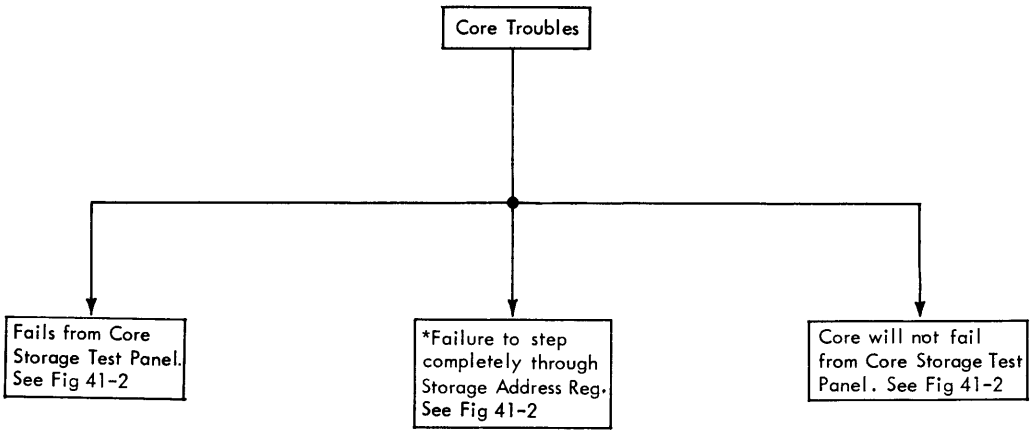
Sense lights indicate which test routine is being performed. Sense light #1 signifies working in the storage deflection section, #2 signifies working in the ones and zeros section and #3 signifies working in random number section.

737.40.00 SERVICE TECHNIQUES ON 737 CORE STORAGE

737.41.00 TROUBLE SHOOTING CHARTS

These charts follow the same format as the 704 CPU trouble shooting charts. These charts cover only the core storage portion of the test. Before these charts are used, a diagnostic or other test must be used on the Central Processing Unit to be sure the trouble is in core storage and not in the CPU.

We have tried to build reliability into these charts to show up intermittent troubles. We have included a selection test, however, any you know or like can be used. Most of the chart is to be used with the included selection test or some other test running in the machine. Below are some of the symbols used in the test.



* When the test switch is on and the test is running the 2000 and 4000 address neons should be the only lights visible and they should not be on constantly.

FIGURE 41-1. CORE STORAGE TROUBLE SHOOTING CHART

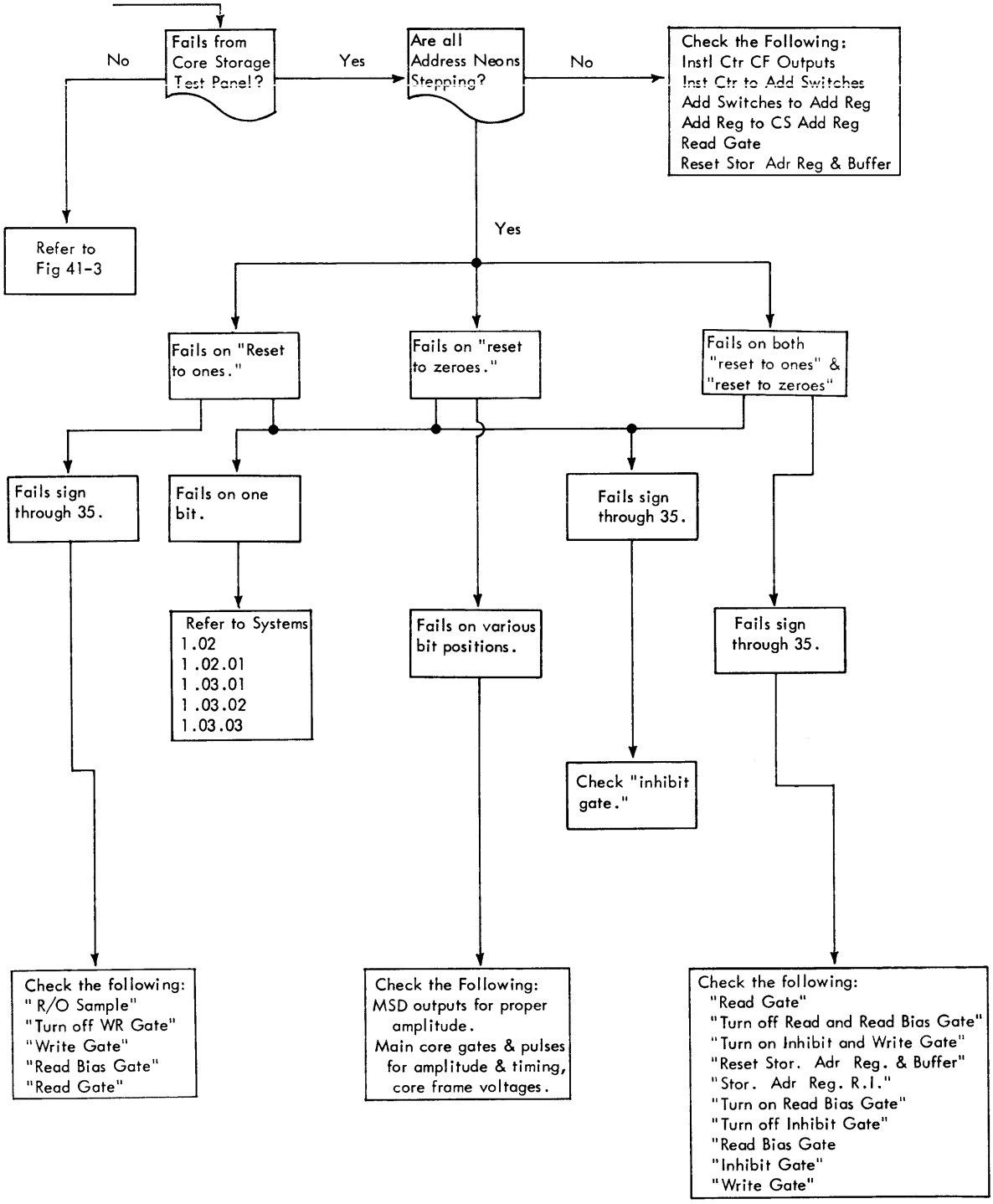


FIGURE 41-2. CORE STORAGE TROUBLES

Location	OPN	DECR	X	ADDR	
0	LXA		A	00	
1	CPY		A	01	
2	TXI	7777	A	01	Loader
3					
4	LXA		AB	23	L (7751)
5	CLA			24	L (26)
6	STO		A	7777	
7	ADD			25	L (1)
10	TIX	1	A	6	
11	CLA			24	L (26)
12	CAS		B	7777	
13	TRA			21	
14	TRA			16	
15	TRA			21	
16	ADD			25	L (1)
17	TIX	1	B	12	
20	TRA			4	Pass Complete
21	LDQ		B	7777	Load MQ with incorrect information from address shown in Acc (Error).
22	HTR			16	
23				7751	Constant
24				26	Constant
25				1	Constant

If Core did not fail from Test Panel the trouble could be an addressing selection failure. This program should find the address or addresses that failed.

Steps 4 through 10 store the address at the address starting at location 26. Step 11 then sets the Accumulator with 26 to be compared with the contents of location 26 which should contain 26. Steps 12 through 17 then compare each sequential storage location after first increasing the amount in the Accumulator by one. In the event of a failure to compare a transfer to step 21 is affected. The MQ is then loaded with the contents of the Storage location which failed to compare and the program halts in step 22. Pressing the start key causes the program to continue testing to determine if any other selections were not stored or selected correctly. All locations not selected correctly will be found and a pattern failure may be established.

FIGURE 41-3. CORE STORAGE SELECTION TEST

737.50.00 SERVICE AIDS

737.51.00 TROUBLE SHOOTING AIDS

In this section is a collection of items which is useful to the Customer Engineer in keeping a 737 Core Storage in good operating condition. Most of the section lists a trouble and a particular fix for that trouble. A test point chart is included to make scoping or testing points available for specific pulses.

737.52.00 TEST POINT CHART

1	Timing Pulse Ctrl Ckts - 1.05.01	
	E Time	MF3 - F29 - 2
	Use Time	MF3 - B29 - 2
	U_3 Till NU_3	MF3 - D29 - 6
2	Gate Generator - 1.05.04-05	
	Read Bias Gate	CSF2 - D03 - 2
	Read Gate	CSF2 - D02 - 2
	Inhibit Gate	CSF2 - K04 - 2
	Write Gate	CSF2 - M03 - 2
3	Timing Pulse Terminations - 1.05.06	
	Reset SAR and Buffer Reg	CSF1 - Jd
	SAR RI and Turn on Read Bias Gate	CSF1 - Rd
	Turn on Read Gate	CSF2 - Ga
	RO Sample	CSF2 - Mb
	Turn off Read and Read Bias Gate	CSF2 - Eb
	RI Sample	CSF2 - Nd
	Turn on Inhibit and Write Gates	CSF2 - Ka
	Turn off Write Gate	CSF2 - Jd
	Turn off Inhibit Gate	CSF2 - Md
4	Core Bias Voltages	
	Sense Amps - 1.10.03	CSF2 - H06 - 1
	MSD Bias - 1.10.02	CSF2 - C21 - 4
	DPD Bias - 1.10.02	CSF2 - L21 - 4
5	Read/Write Ctrl - 1.04.02	
	Read Control (S, 1, 2)	CSF1 - J07 - 8
	(18, 19, 20)	CSF1 - Q07 - 7
	(3-17)	CSF2 - G07 - 6
	(21-35)	CSF2 - Q07 - 6
	Write Control (S, 1, 2)	CSF1 - K07 - 2
	(18, 19, 20)	CSF1 - Q07 - 4
	(3-17)	CSF2 - E07 - 8
	(21-35)	CSF2 - N07 - 8

737.53.00 TROUBLE SHOOTING (TWO CORE STORAGE OPERATION)

737.53.01 Isolation of Two Core Storage Units

This is an aid in cases where core troubles are suspected of giving the trouble and there are two core frames (737's) attached to one main frame (704) and the trouble cannot be traced to any particular core frame. A relatively simple method to isolate one core frame is to pull the PCF tubes on the output of all 36 Buffer Register triggers on either core frame in order to test the other core.

If this does not isolate the trouble then the following method can be used to completely isolate one core frame:

Turn "off" DC power.

Remove tube #6 MF3 - J29-6; 3.42 and 3.21. In two core operation, positions 5-17 of the Address Register, Storage Bus, Address Switches and Instruction Counter are used. For one core operation, positions 6-17 are used. Position #5 on each of these must be crippled. Removal of tube #6 kills Instruction Register position 5 and Address Switch and Address Register position #5.

Add a wire from MF2 - H08 - 5 to MF2 - Axx - 6(-30v). All the A6 points on MF2 are -30v connections. This wire will tie storage bus position #5 to -30v only when Address Switches are gated to the Storage Bus. Position #5 will work normally from Acc, MQ and Storage Register.

Remove the wire from MF2 - 28F to MF4 - 28K. Add a wire from MF4 - E25 - 3 to MF4 - E 25 - 8. In 2 core operation when the address is moved through the adders, position #5 must be used in indexing operations. For one core operation position #5 of the adders must be crippled and position #6 used with index registers. Removing the wire from 28F to 28K kills the carry out of adder 5. Adding the wire from E25-3 to E25-8 gives the adder 6 carry. This carry is needed for indexing operation in one core operation.

Remove tubes 3, 4 and 6, PU9194, MF4-A36, 2.12.01. These tubes kill the microsecond delay unit that tie the 3 index registers to adder 5.

Add wire from MF3 - Nh to MF3-33H (+15). This ties the "Minus on Address line 5" line to (+15v) at all times. This line is the gating used to switch the core operations. With this line up all the time, only one core storage can be gated. Operations controlled are the Gate Generator pulses and the RI Sample pulse.

Remove 2 diodes in PU 9300 MF2 A08 from C30 - D30 and F32 - G32. These diodes remove the input to OR ckt "W" from Storage Register 5 to Adder 5 in MF2-A08 and the input of OR ckt "R" from Complement Index Reg. output to adder 5 in MF2-A08.

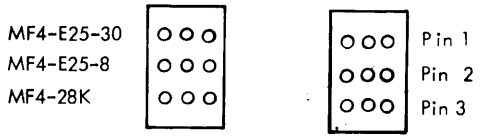
Replace Terminating Resistors. When two 737's are used with one 704 main frame, the terminating resistors of core frame 1 are removed. To test core frame 2 it must be attached to the main frame by the I/O cables and the I/O cables removed from core frame 1. To test core frame 1, tie core frame 1 to the main frame and remove I/O cables to core frame 2. When core frame 2 is removed there are no longer any terminating resistors so the resistors must be soldered into place in core frame 1. When going back to two core operation, just unsolder one end and bend the terminating resistor back out of the way. Then changing from 2 to 1 or vice versa, core operation can be greatly shortened timewise. Also make sure the installation has I/O cables long enough to reach from the main frame to either core frame. This is a necessity to go to single operation.

Turn on DC and test single core operation.

Reverse procedure to return to 2 core operation.

Additional Aid but not necessary. To help simplify this change a three position plug receptacle can be mounted on main frame 4 and the following wiring is done. This eliminates step 4 of the above write up.

Normal 2 core operation has a wire from adder 5 carry output to the adder X carry trigger MF2-28F to MF4-28K and then a wire goes from MF4-28K to MF4-E25-8. Remove the wire going to MF4-E25-8 and bring it to pin 3 of the plug receptacle. From pin 2 run a new wire to MF4-E25-8. Add a new wire from MF4-E25-3 to pin 1. For two core operation plug pin 2 and 3. For one core operation plug pin 1 and 2.



737.54.00 ADDRESS SELECTION TROUBLE SHOOTING

The address selection and core driving circuits present trouble shooting problems that are peculiar to this unit of the computer. Trouble in these circuits causes failures in particu lar addresses only. The customer engineer can learn to spot the trouble location quickly by the address pattern of failures.

737.54.01 Finding Addressing Failures Using CE Test Panel

Assume that, after resetting to ones and turning the test-on switch on, the machine stops at address 7146 when the check stop switch is turned on. Press the check-stop-reset key repeatedly and note carefully the address displayed in the SAR neons each time.

Assume that the stops fall in this pattern:

7146
7147
7240
7241
....
....
....
7247
7340
....
and so on

Note that all failures appear to be at addresses where the tens position is 4. This should indicate some trouble in the Y write (P2) switch core drive circuit for address 40. The eight Y matrix switch cores, address 40 to 47, are failing to be reset. Therefore, storage can neither read nor write in any of the 512 addresses associated with these cores (64 addresses/Y drive line x 8 switch cores = 512 addresses).

Checking the scope wave forms with the machine running in test with the check-stop switch off should quickly locate the trouble.

737.54.02 Address Failures Using Main Frame Operator's Panel

If the failure is in the X matrix (hundreds or thousands position of the address), it may take a lot of button pushing at the CE test panel to determine the pattern. The following method may be quicker. (Assume again that the machine fails in 7146 as the check stop switch is turned on. However, this time there is no simple pattern; a failure seems to occur in every location from 7146 on.)

737.54.03 Locating Troubles in Core Storage by Use of the Operator's Panel Keys

Another method of separating troubles in core storage is as follows:

Clear storage to zeros.

Enter all ones in storage locations 0000, 1111, 2222, 3333, 4444, 5555, 6666, and 7777.

Display each of the above addresses. Assume the trouble occurs in address 4444 and it does not display all ones.

Enter all ones in like addresses. Using the above assumption, this would be addresses 4000, 400, 40 and 4.

Display the above addresses and check for all ones. This should separate address troubles. If no error occurs in this display, then the failure must be in the original address circuits. Assuming the above would be the address circuits of 4444.

1. Turn the test switch off.
2. Clear storage.
3. Store all ones in 7146.
4. Place CLA...7146 in keys.
5. Turn on continuous memory read-in switch.
6. Hit enter-instruction button.

Assume that a failure occurs (accumulator drops a bit).

7. Repeat 2, 3, 4, 5, and 6 using address 0046.

If no failure occurs, the Y matrix (units and tens position) must be all right.

8. Repeat 2, 3, 4, 5, and 6 using address 7100.

A failure here indicates the trouble is in either the 7000 or the 100 drive circuits.

9. Repeat 2, 3, 4, 5, and 6 using address 0100.

No failure here indicates a definite trouble in the 7000 drive circuits. Work back from there to find the particular trouble.

737.55.00 MEMORY RELIABILITY

737.55.01 Staggered Read Modification

For general improvement in 737 Core Storage operation, the read gates are staggered. The "X Read Gate" is from A3.5 - 6.5 and the "Y Read Gate" is from A3.0 - 6.0. The "Write Gate" must be lengthened from A8.5 - A1.0. PU 5151 will now contain both the "X" and "Y" read gate generators (CSF2 - A02) where before the read gate generator was contained in PU 5020 CSF2 - A02 and A03. Now PU 5020 is only used at CSF2 - A03. Remove the delay line CSF2 - J03-8 to R03-5 to lengthen the write gate and also remove tube 01A - CSF2 - J03.

737.55.02 Intermittent Memory Errors at Random Addresses

Memory errors of an intermittent nature and occurring at various addresses in memory have been traced to a loose and corroded filament transformer leads feeding the 5998's in the driver panel.

Troubles of the same nature can be caused by a severe decrease in the speed of the core frame blowers.

When intermittent storage troubles are encountered and a 5998 is suspected to be the source, a good idea is to bias the MSD and DPD reference voltage more negative to improve the cut-off characteristics of the 5998's. If the trouble disappears at this bias voltage, a 5998 is probably at fault. On the other

hand, intermittent failures may be brought on more consistently by biasing the 5998's more positive. Incidentally, the reference voltage should be measured at the edge connectors and not at the potentiometers.

737.55.03 Memory Error - Picking Up or Dropping of Bits

Flaking 6136 Tubes. These are found by vibrating affected circuits. Other possible causes are the sense amplifiers which may be too high or the 100 mfd capacitors in DPA may be heat sensitive. This is noticeable especially after extended operation.

Noisy 6136 Tubes. These have recently been found in the sense amplifier circuits of the 737 Core Storage. These tubes can not be found with a tube tester, therefore, the best way to show them up is to tap the tube lightly (with finger or pencil eraser) while running the "Test for Zeros" test at the CE test panel. Any noisy 6136 tubes can be discovered by watching for a pick up of bits.

737.55.04 Check Stop Rise Time

The check stop line is used to inhibit the resetting of the Storage Address Register and Buffer Register. On some machines, particularly if two or more 737's are with a CPU, the rise time is not fast enough to inhibit this reset. Adding another cathode follower to power this line eliminates that trouble. This can be called for by B/M 562301.

737.56.00 OTHER CORE STORAGE TROUBLES

737.56.01 Switch Core Trouble

If switch cores are suspected and yet test out good, a gentle vibration of the switch core will show up any with internal cold soldered joints.

737.56.02 Pluggable Unit

Jumper wires between PU are too tight on some machines. Terminals are rubbing through the insulation, grounding out to the frames causing unexplained troubles.

737.56.03 Blower Substitution

Overheating occurs in the pluggable unit section. B/M 562509 calls for a new blower with greater capacity to control this heat problem.

737.56.04 Terminal Resistors

If trouble has occurred where the terminal resistors have changed values after extended usage, it is probably because they are the Dalohm 15 ohm 1% resistors. These resistors are bright red in color and have a gauge or gauges along the side.

737.60.00 MACHINE LOGIC

737.61.00 737 CORE STORAGE LOCATIONS

One of the big problems in servicing a machine is knowing locations of components and to be able to readily bring to mind the general picture of the machine logic and data flow.

This section will be devoted entirely to locating of components in the core storage and data flow. The entire logic is shown and then the groups are broken down to show component logic. Also timings and sequences are given to assist the customer engineer.

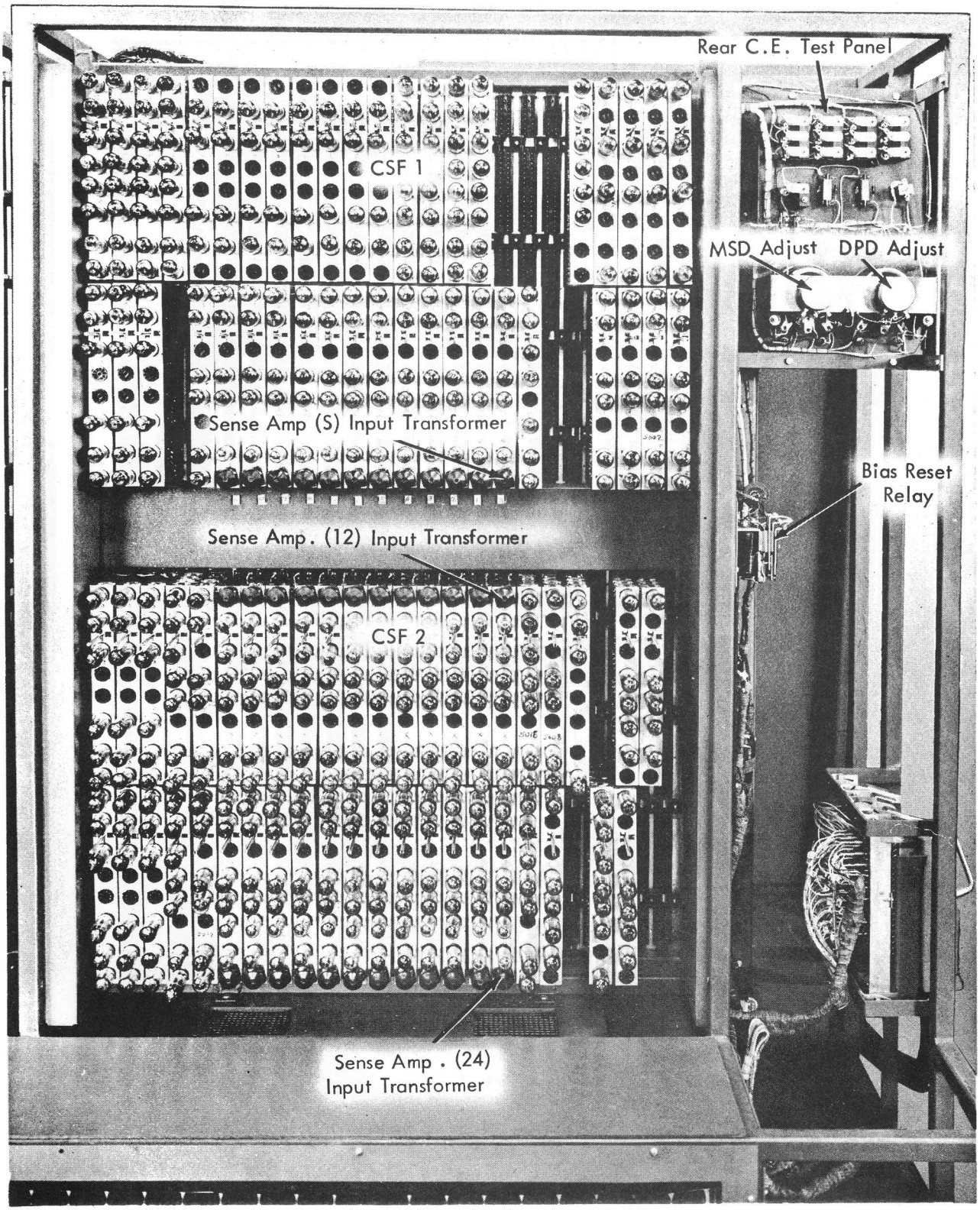


FIGURE 61-1. CSF 1 AND 2, FRONT VIEW

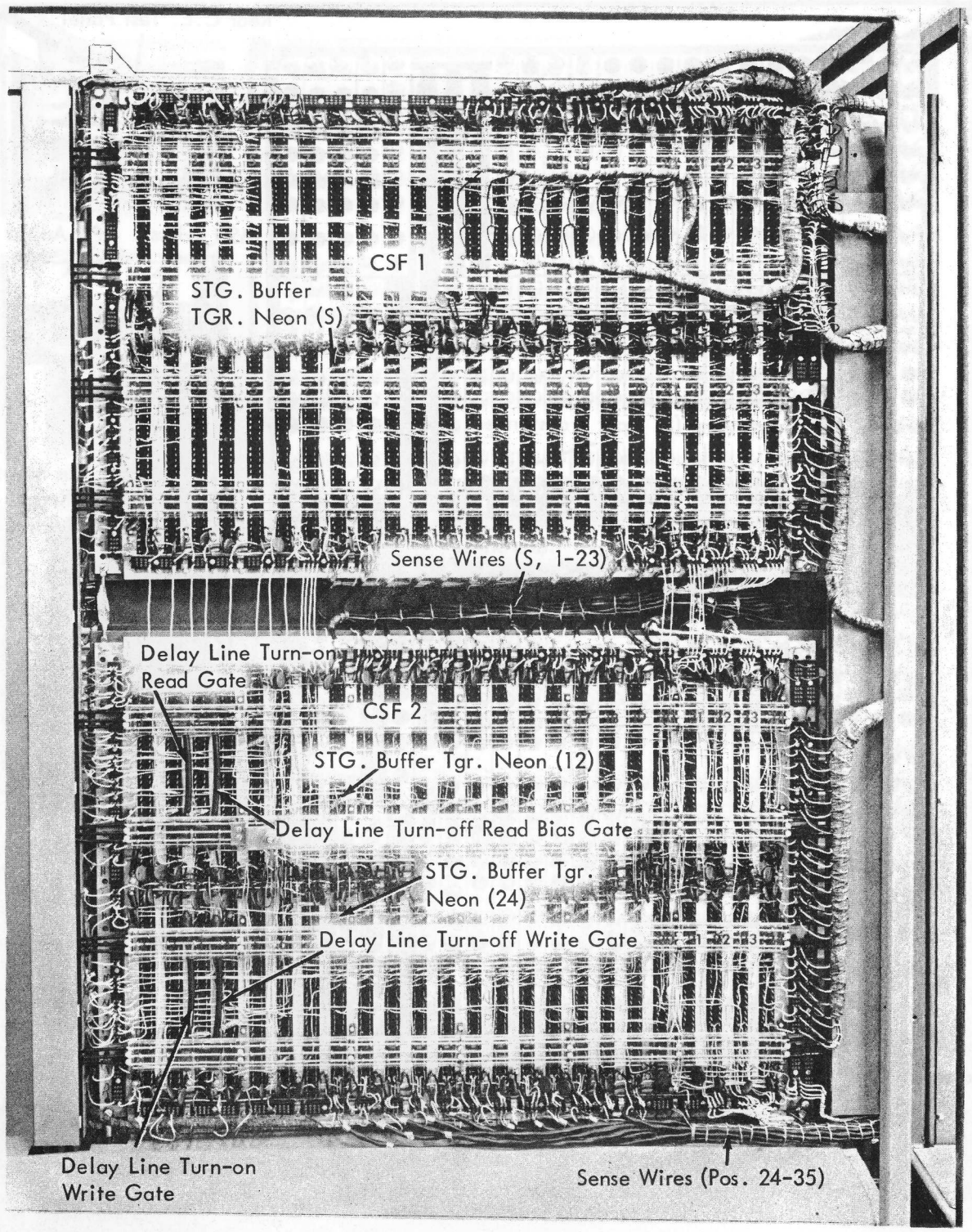


FIGURE 61-2. CSF 1 AND 2, REAR VIEW

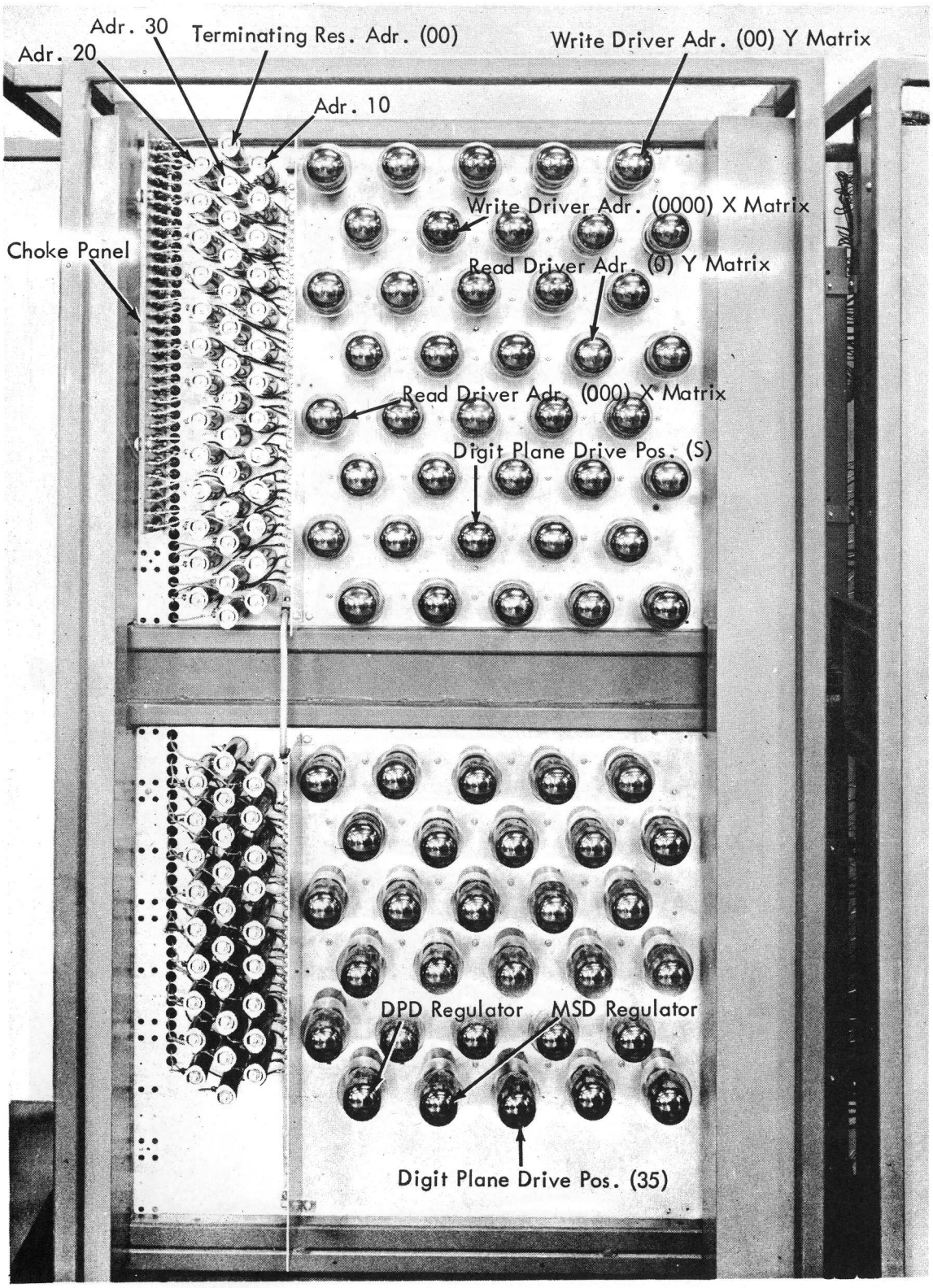


FIGURE 61-3. CSF 3 AND 4, FRONT VIEW

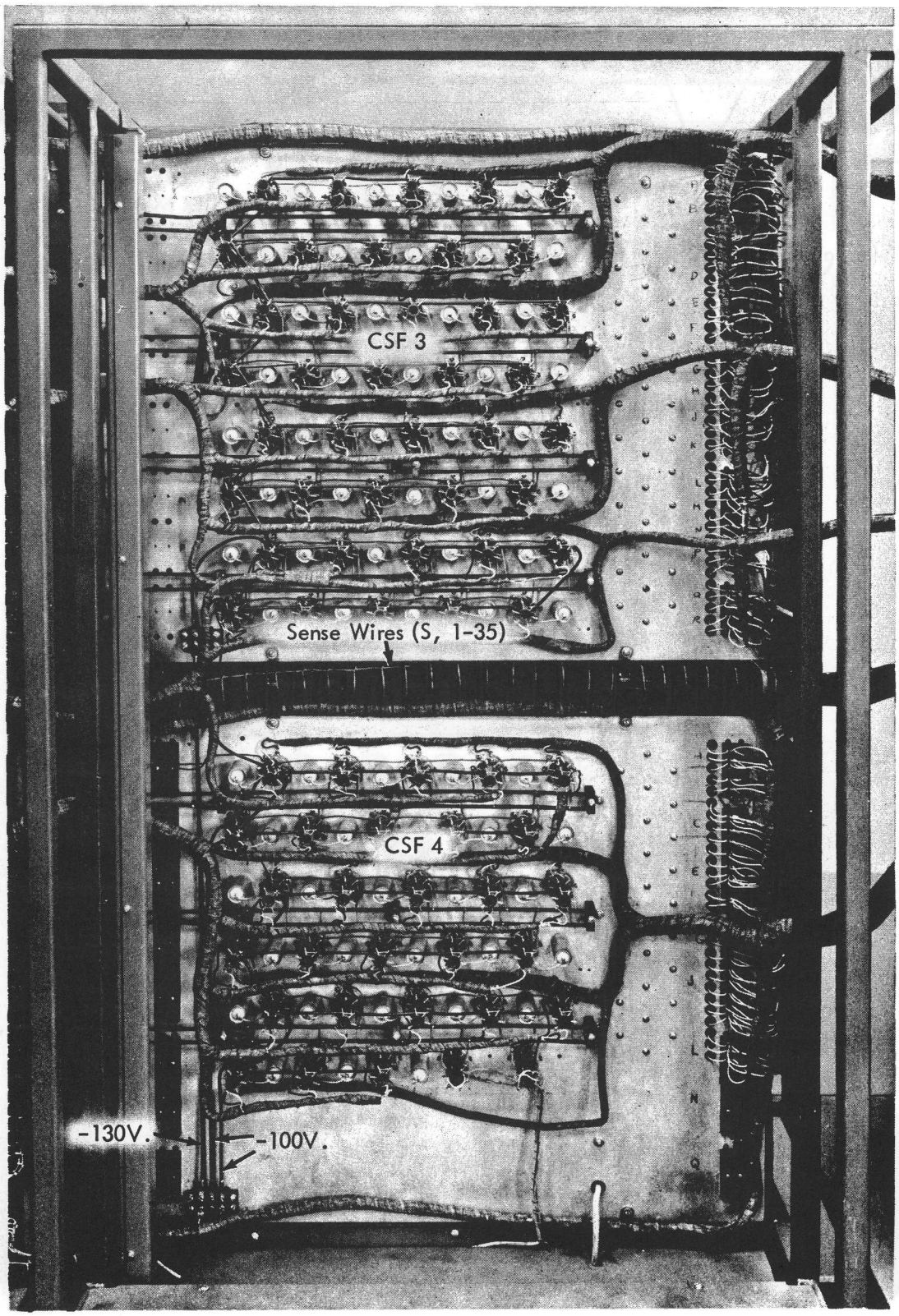


FIGURE 61-6 F IGURE 61-4. CSF 3 AND 4, REAR VIEW

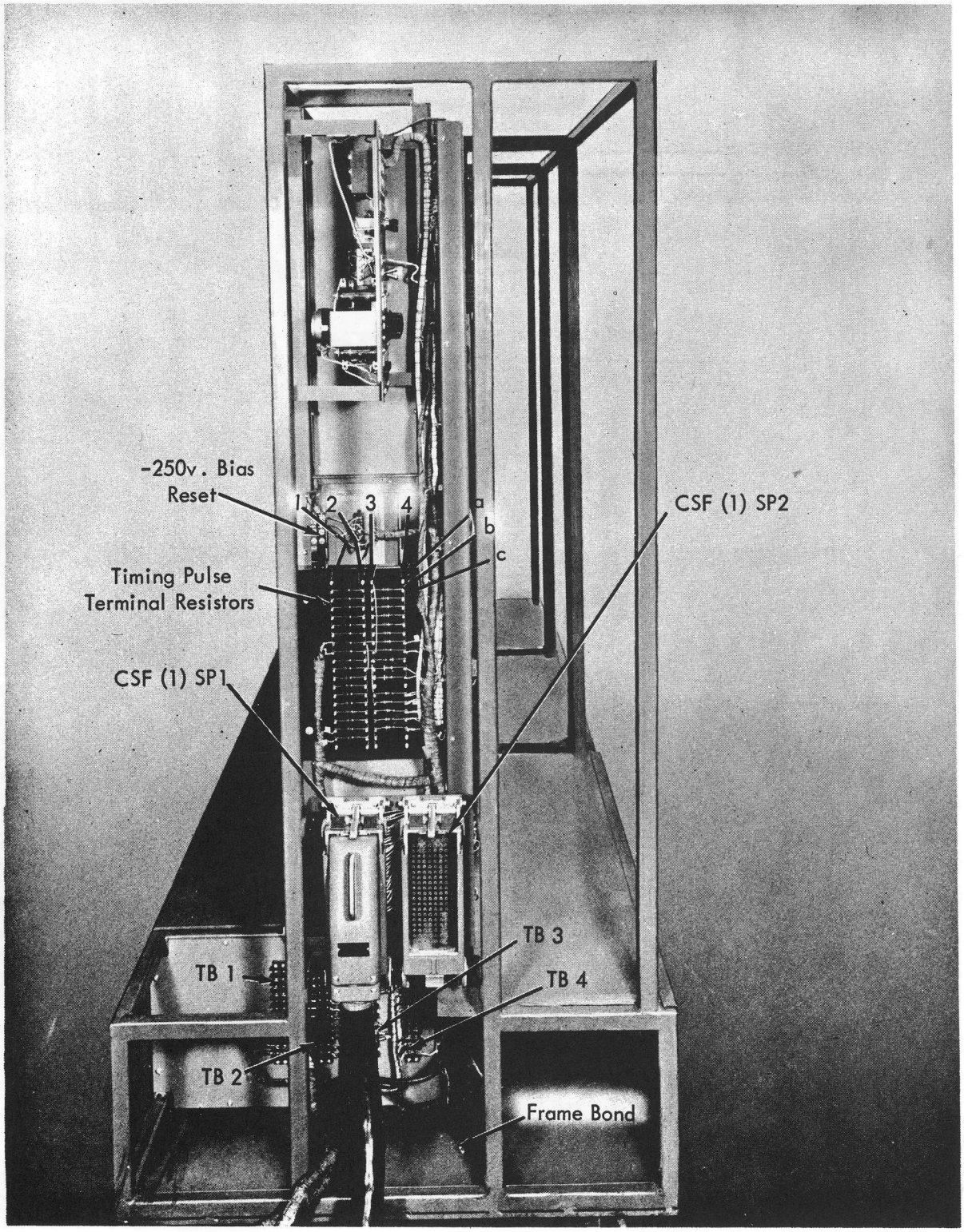


FIGURE 61-5. CORE STORAGE UNIT, RIGHT END VIEW

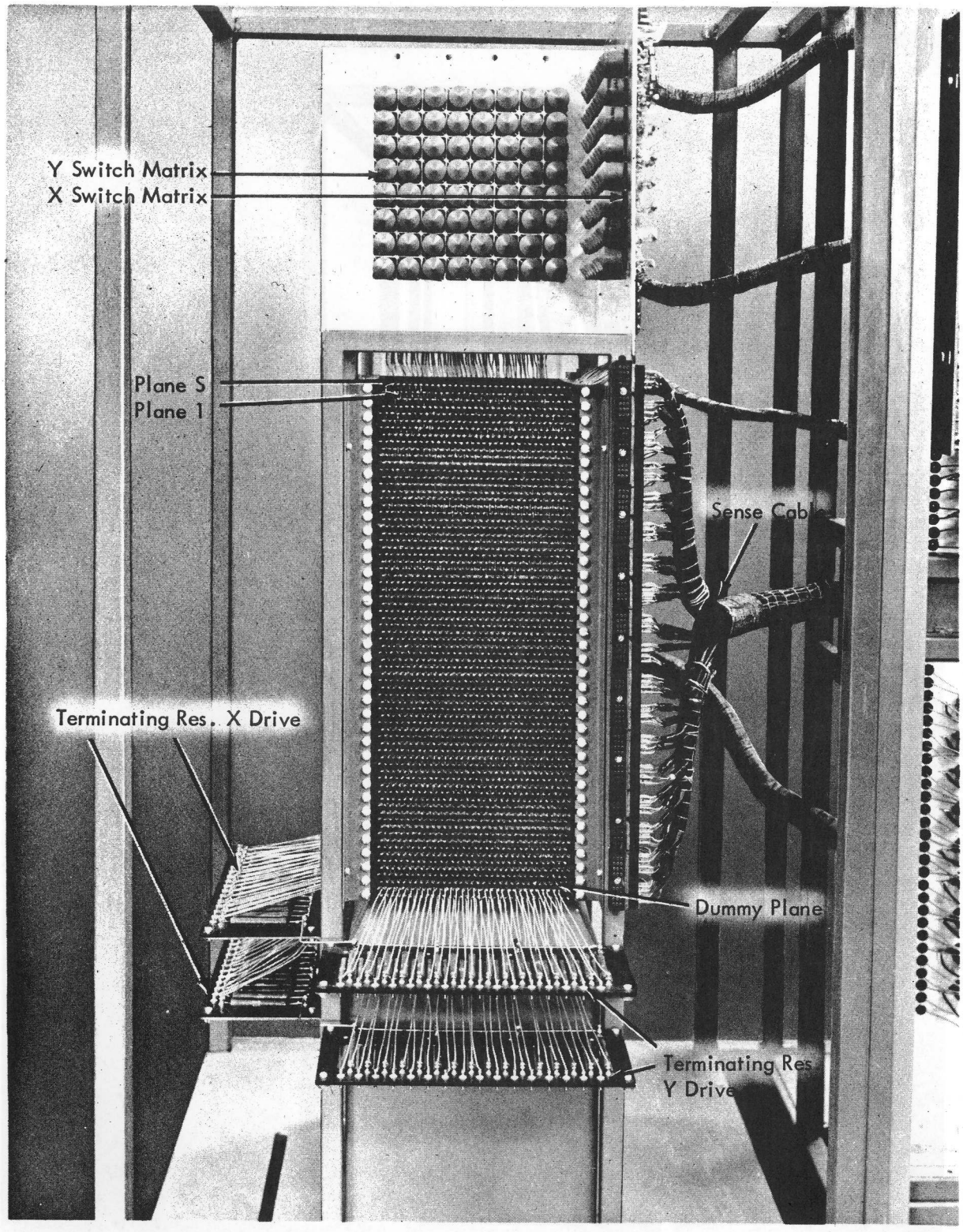


FIGURE 61-6. CORE ARRAY, FRONT VIEW

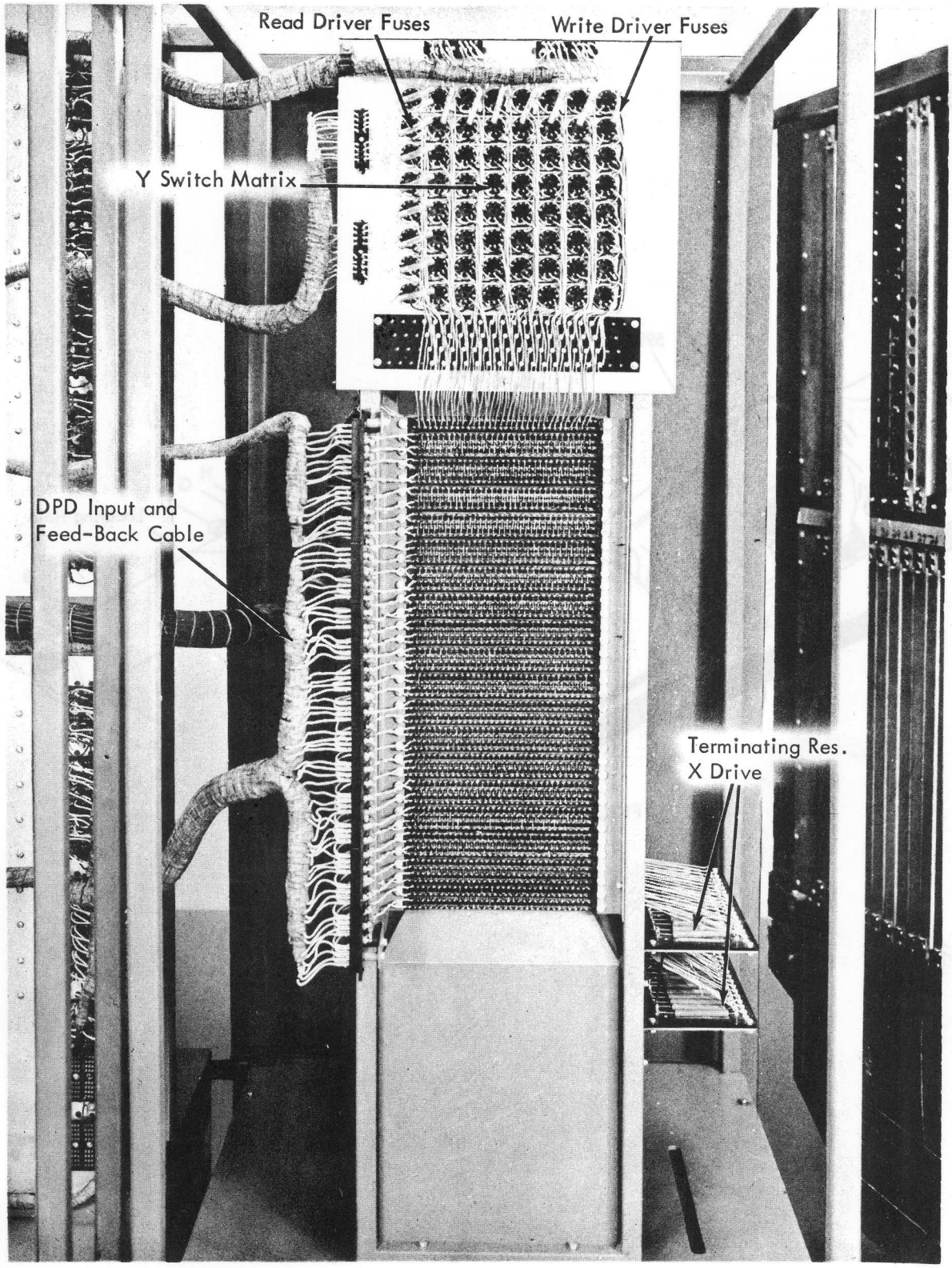


FIGURE 61-7. CORE ARRAY, REAR VIEW

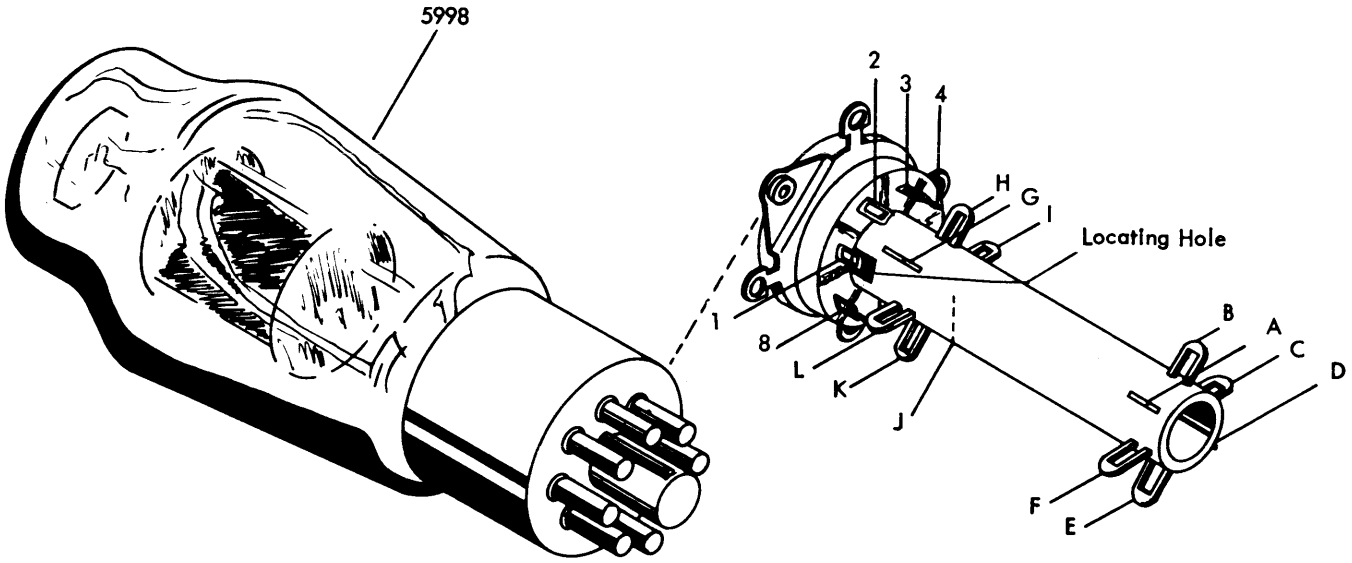


FIGURE 61-8. TURRET SOCKET TERMINALS

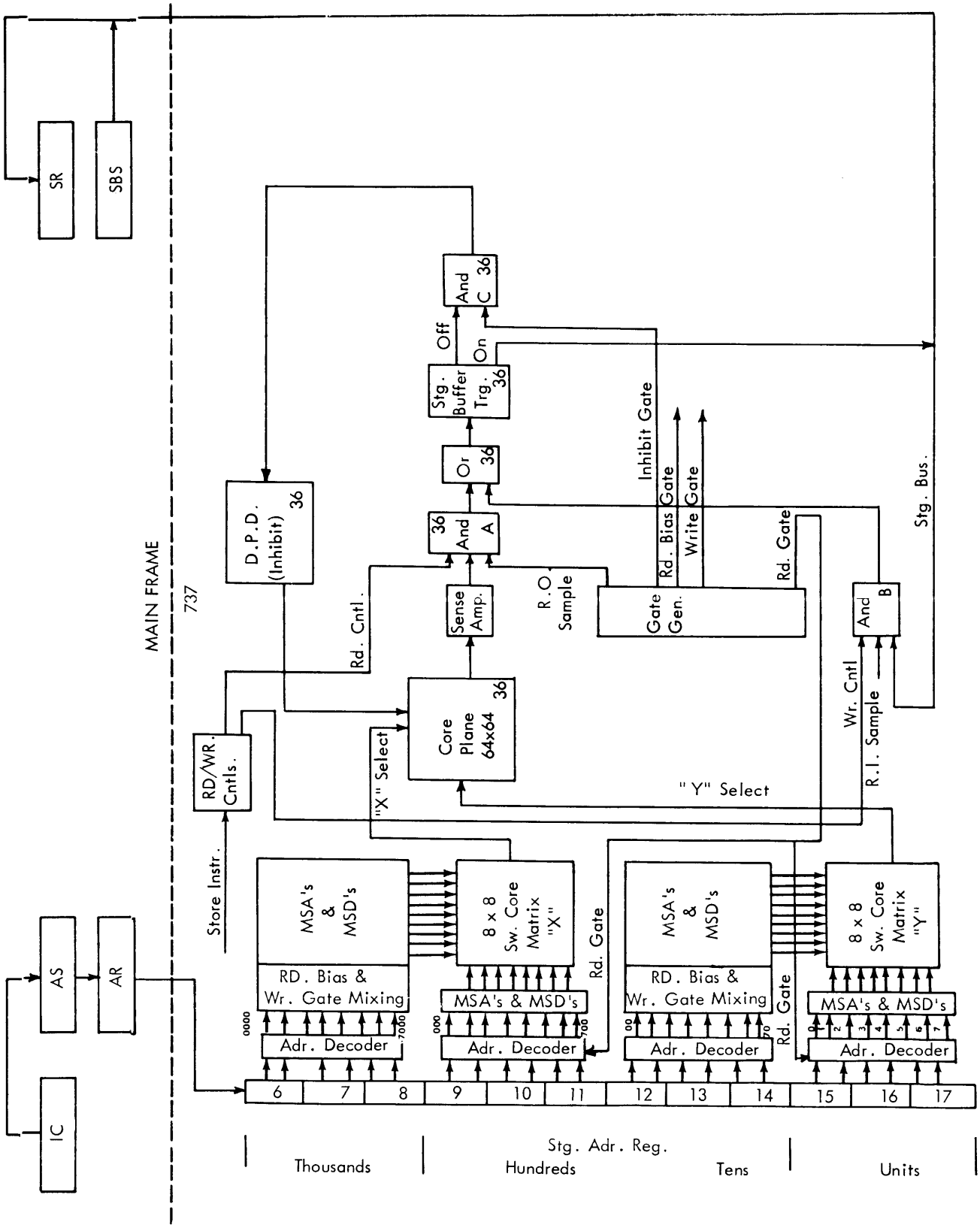


FIGURE 62-1. BLOCK DIAGRAM - CORE STORAGE LOGIC

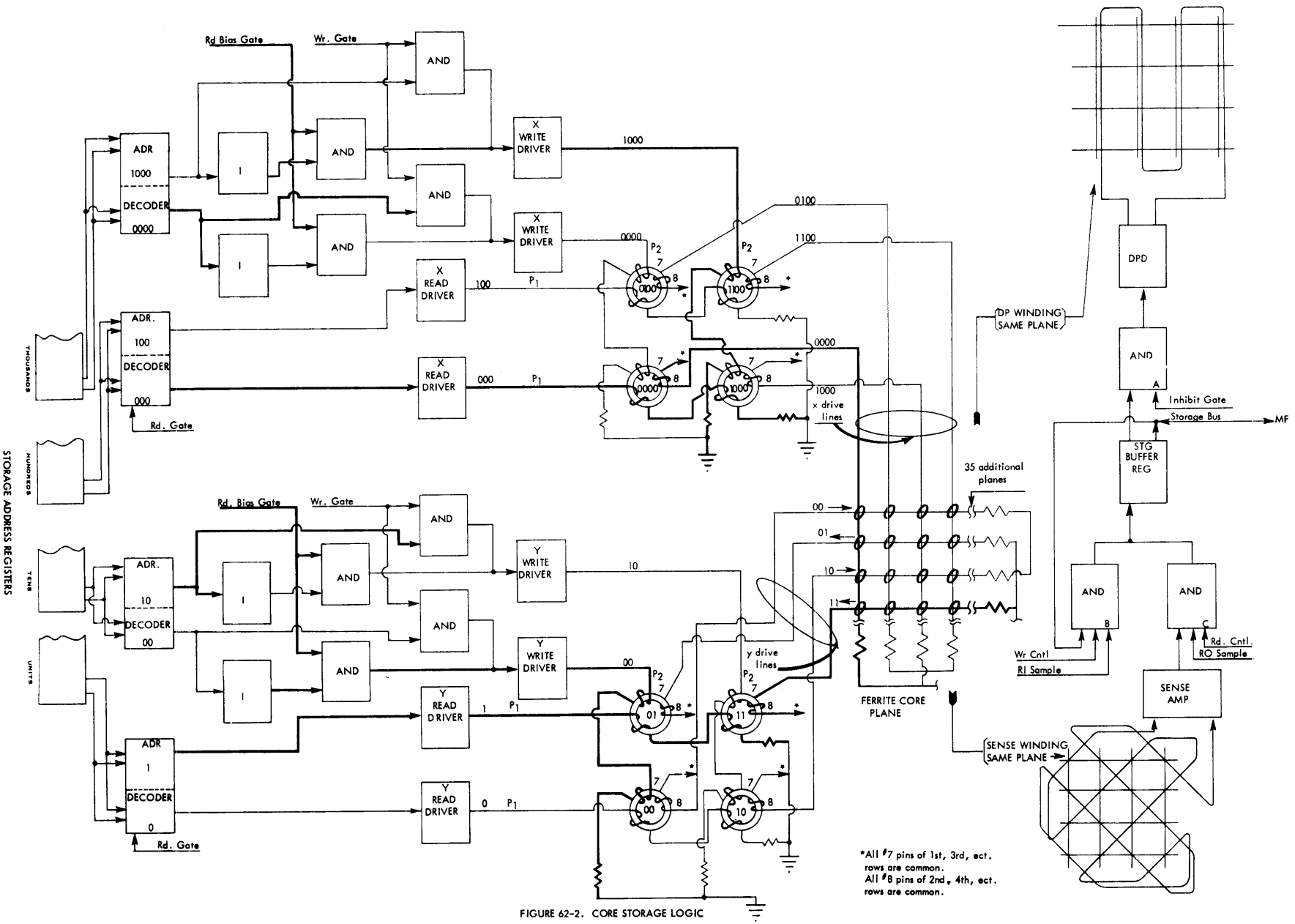
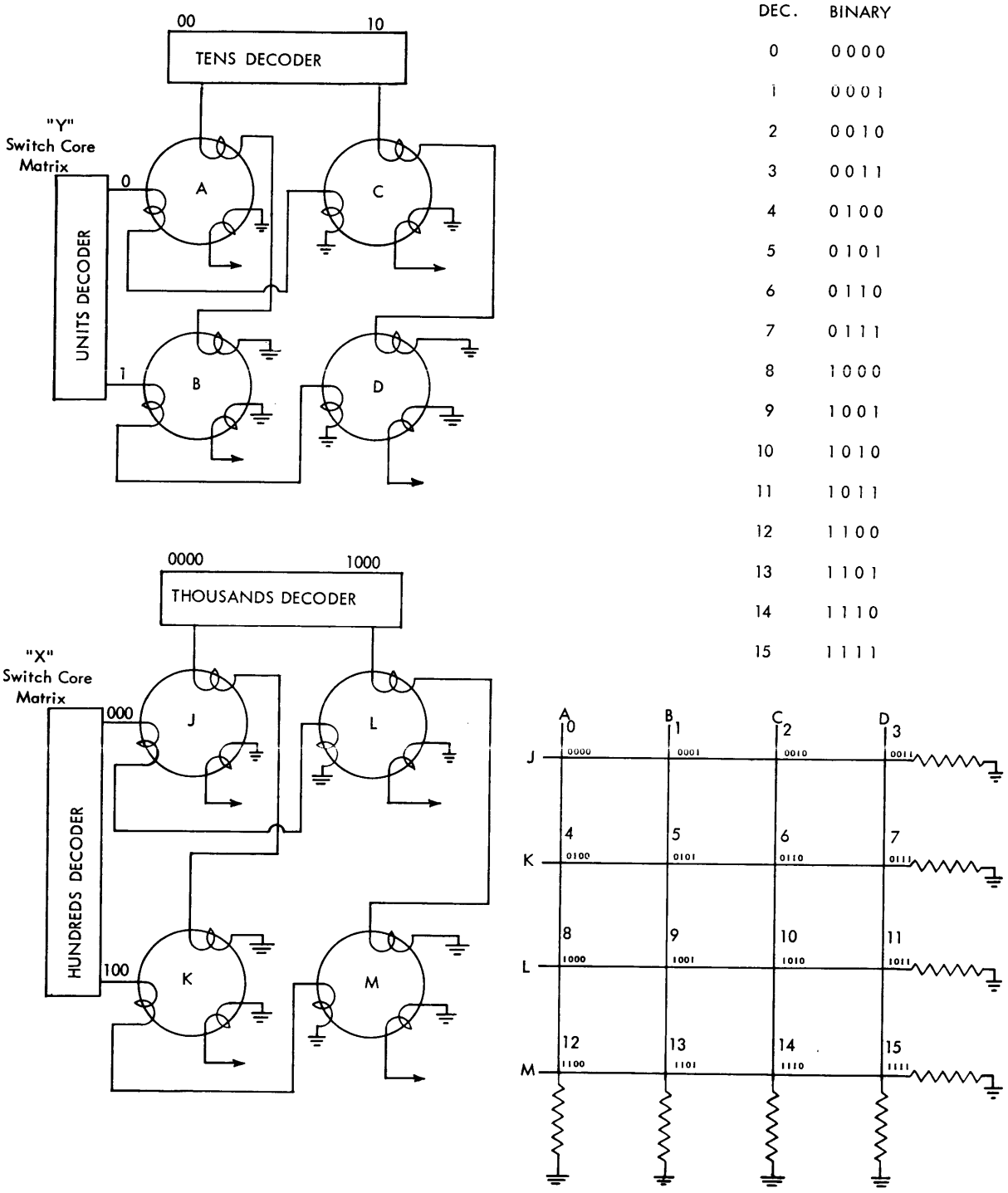


FIGURE 62-2. CORE STORAGE LOGIC

STORAGE ADDRESS REGISTERS



DEC.	BINARY
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	1 1 0 0
13	1 1 0 1
14	1 1 1 0
15	1 1 1 1

FIGURE 62-3. ADDRESS SELECTION

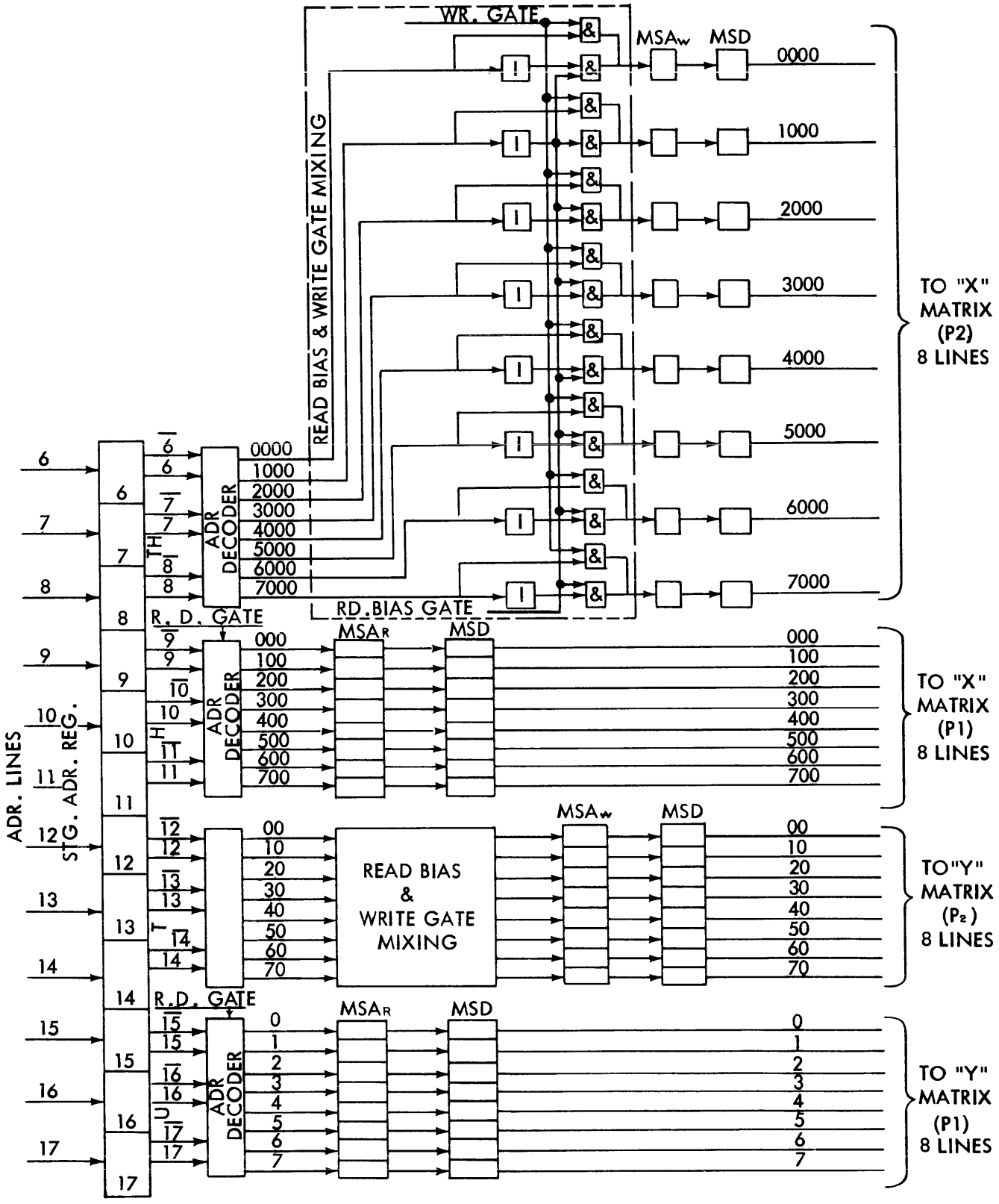


FIGURE 62-4. X AND Y MATRIX SWITCH DRIVE

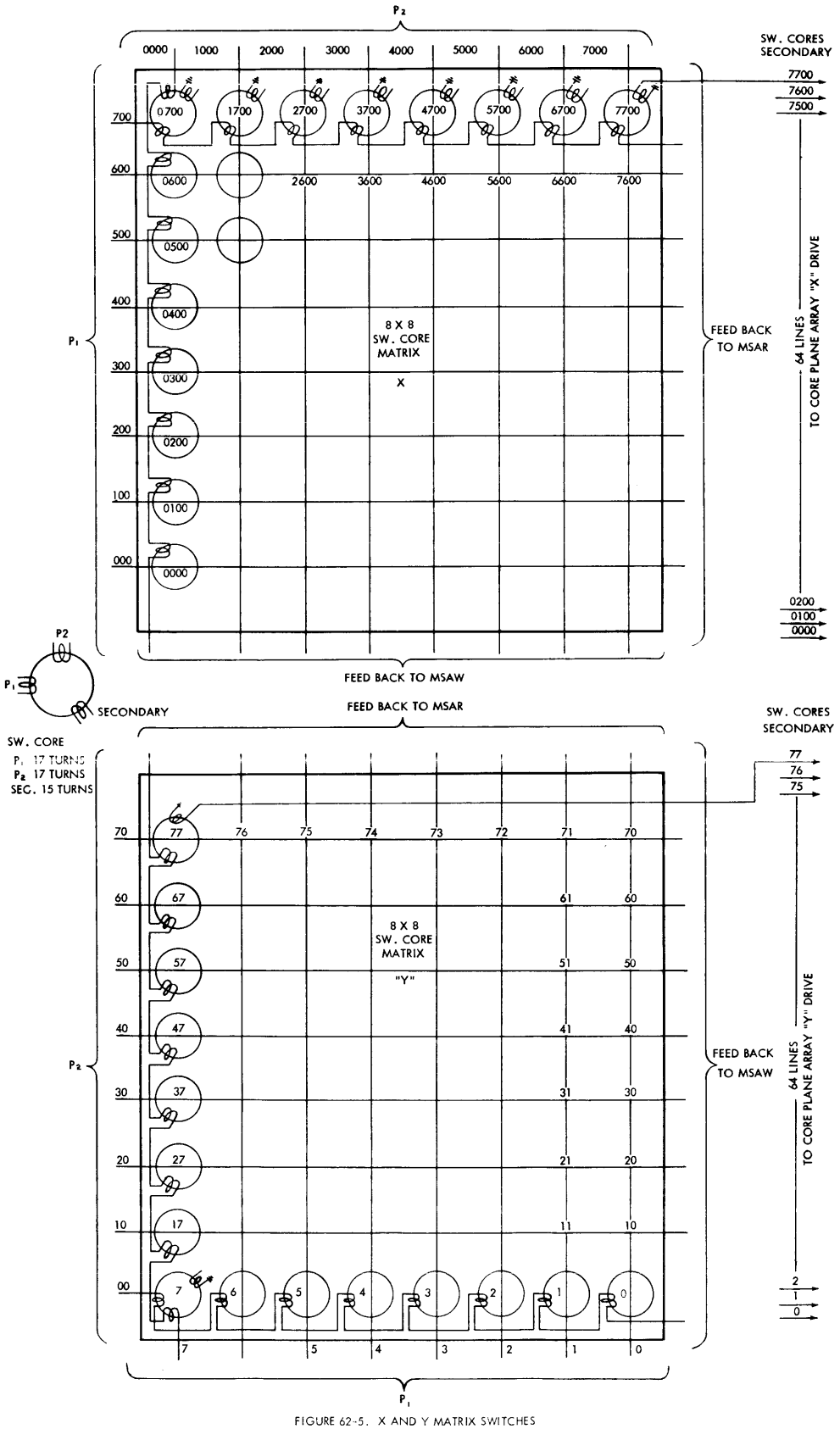


FIGURE 62-5. X AND Y MATRIX SWITCHES

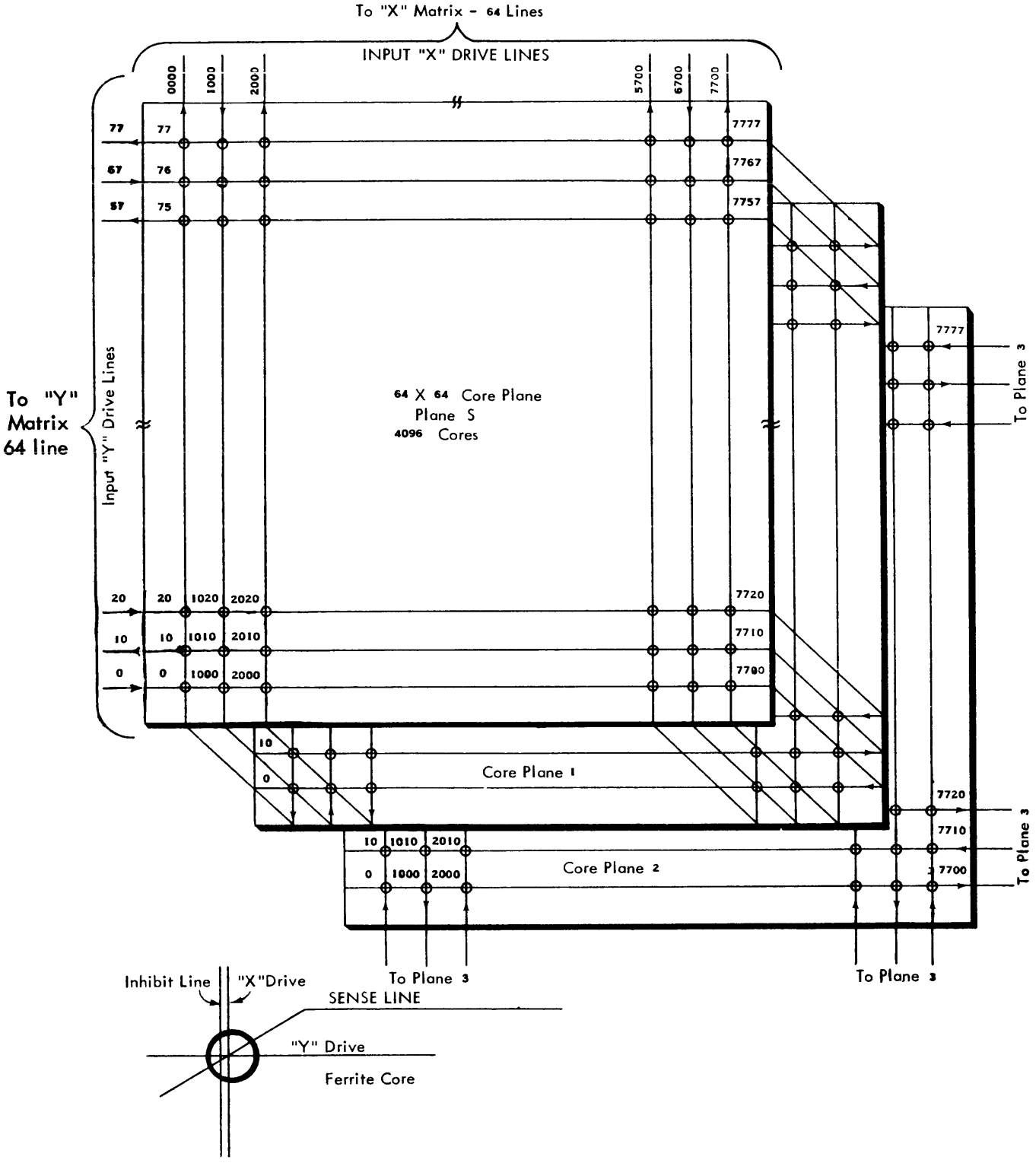


FIGURE 62-6. PARTIAL CORE ARRAY

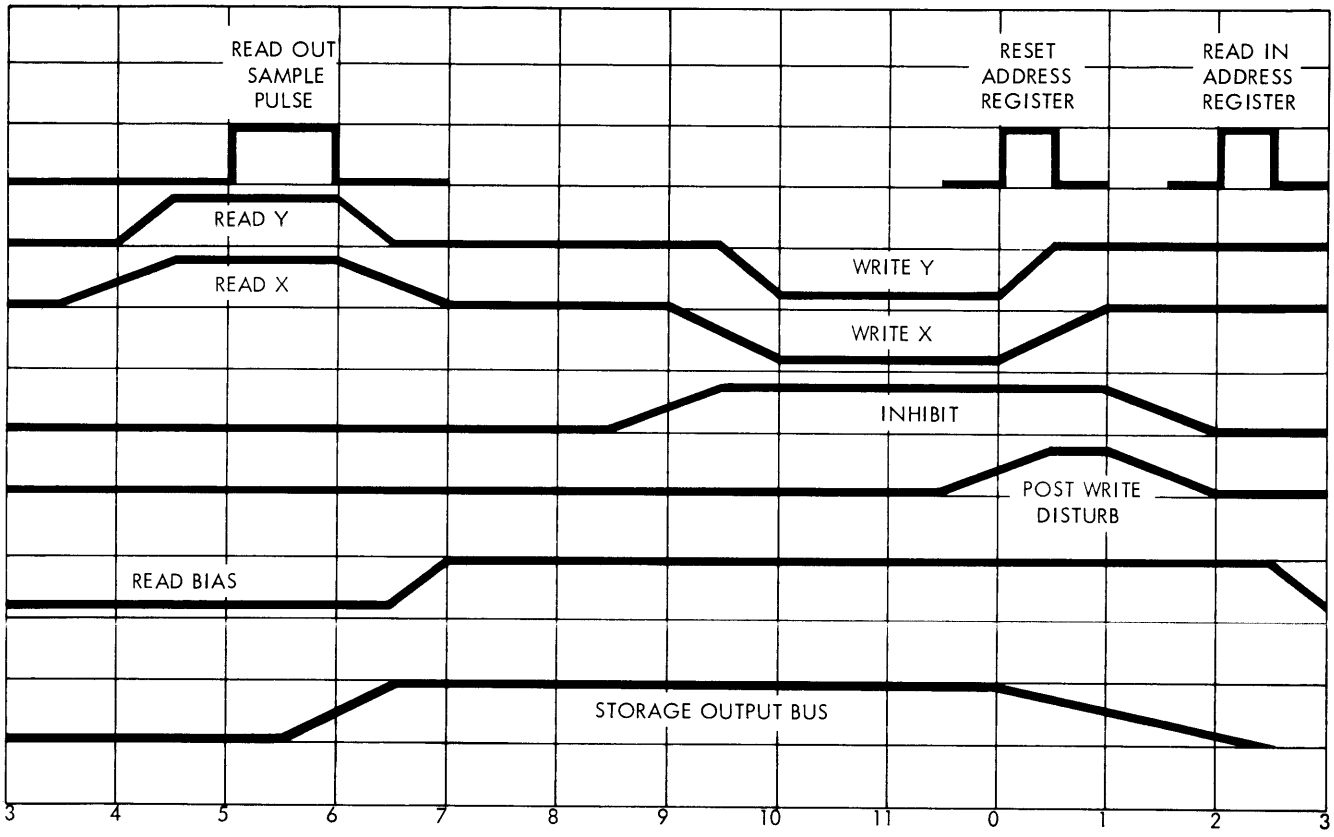


FIGURE 63-1. TIME SEQUENCE

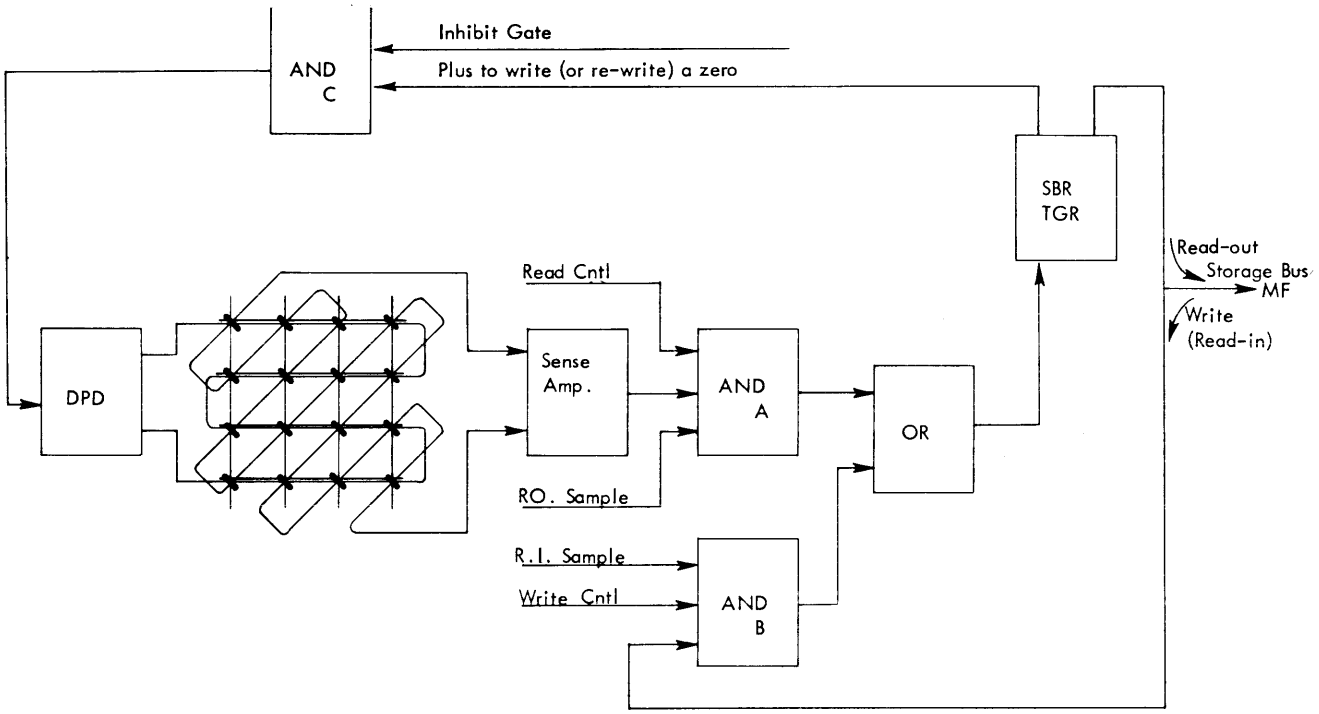


FIGURE 63-2. SIMPLIFIED READ/WRITE CIRCUITS

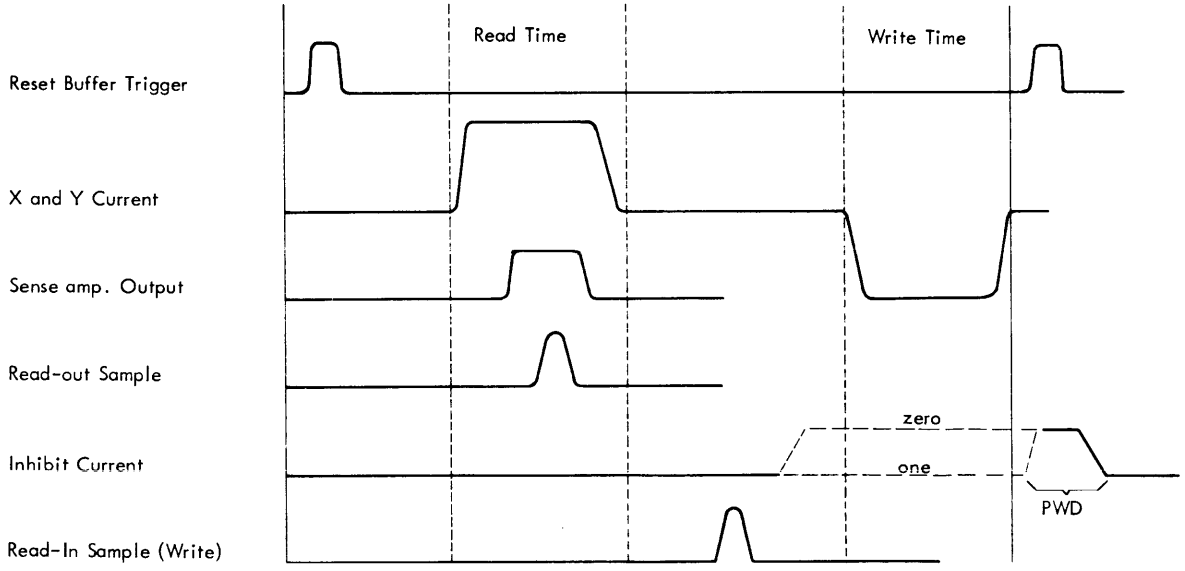


FIGURE 63-3. USE CYCLE SEQUENCE