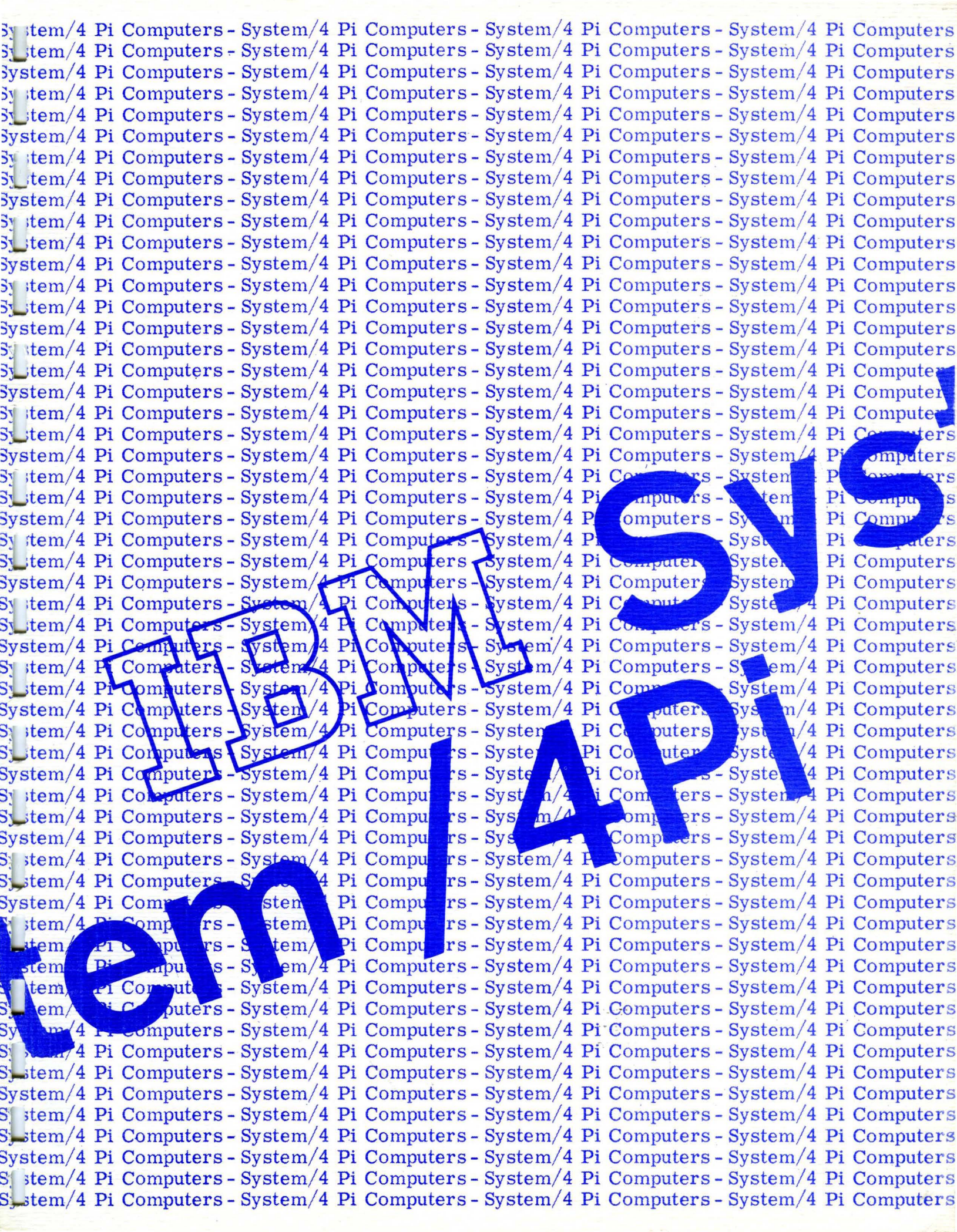
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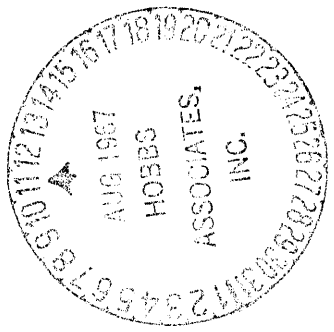
Technical Description of

IBM System/4 Pi Computers



IBM *Federal Systems Division, Electronics Systems Center, Owego, New York*

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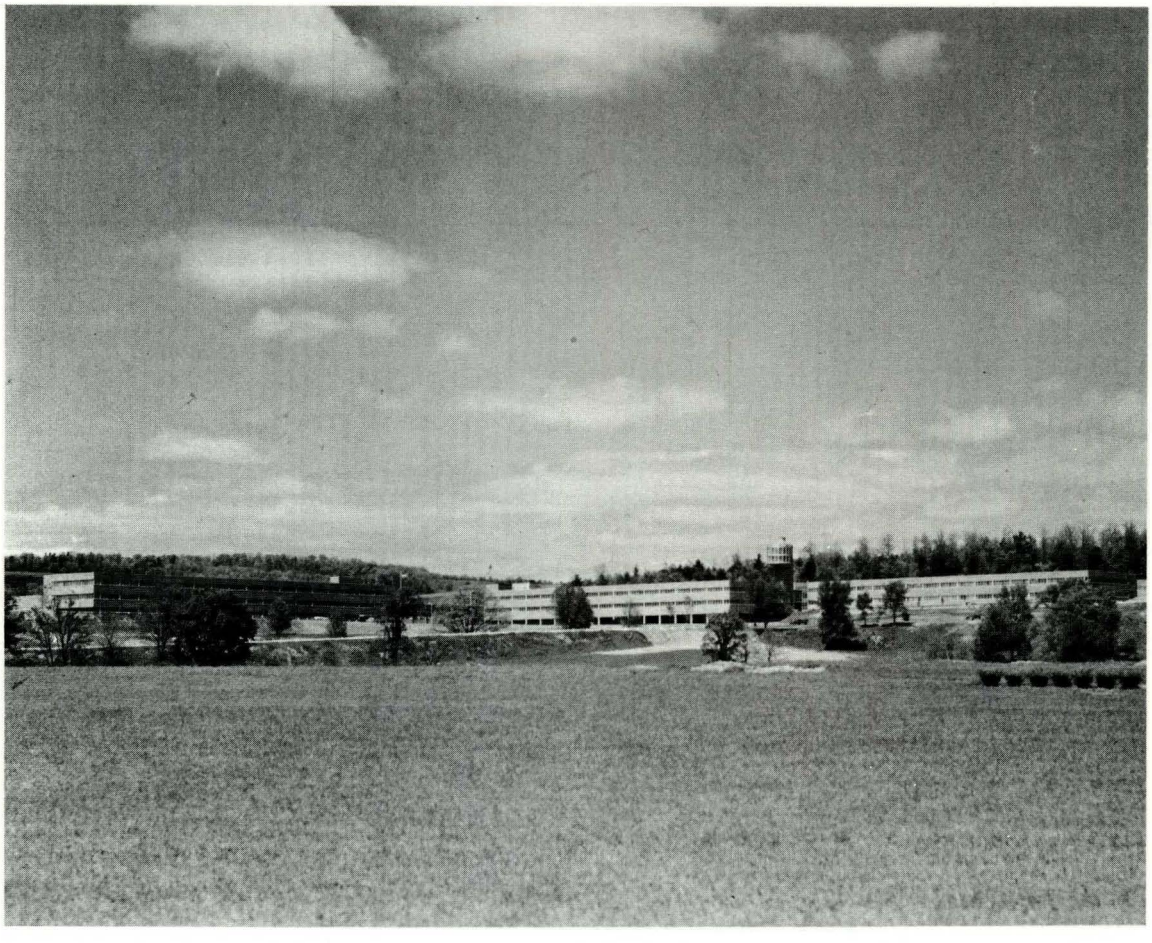
FOREWORD

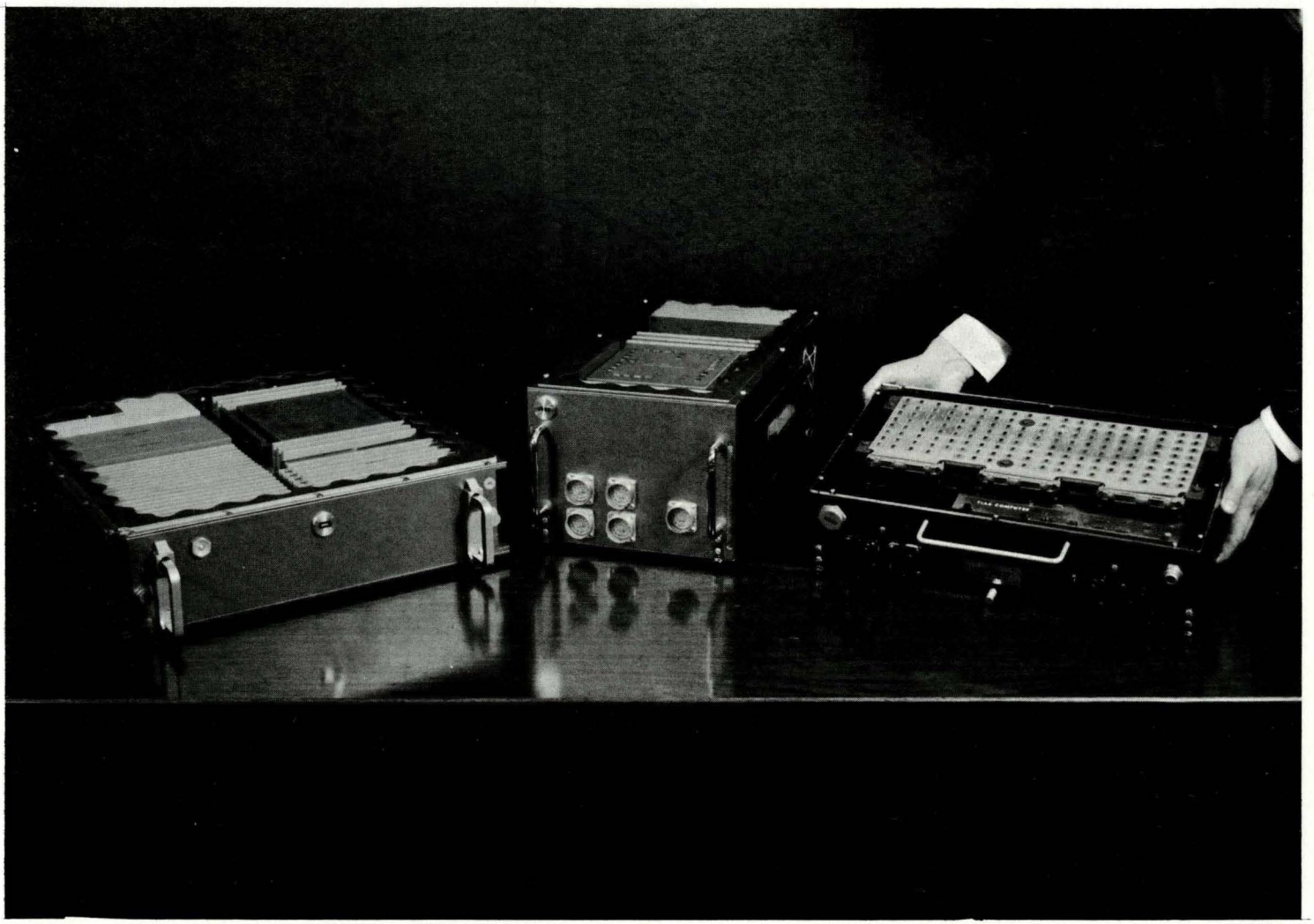
The Federal Systems Division of IBM has developed a family of general-purpose, militarized, digital computers called System/4 Pi. The name 4 Pi refers to the number of steradians in a sphere. It symbolizes System/4 Pi's general-purpose adaptability to the entire spectrum of military and space applications.

System/4 Pi computers are being produced at the IBM Electronics Systems Center in Owego, New York.



Section 1

SYSTEM/4 Pi SUMMARY



Typical System/4 Pi Computer Models
(left to right: EP, CP and TC)

INTRODUCTION

When IBM began its System/4 Pi development program early in 1965, the following guidelines were established:

- Only proven technologies and proven manufacturing techniques would be considered.
- Maximum commonality with IBM's commercial technology would be maintained to insure that the resources of the entire IBM Corporation would be available.
- An off-the-shelf production capability would be developed so that reliable systems could be produced in large quantities with minimum lead time.
- The design of each computer would be general-purpose, so that each computer model could address a wide range of military and space applications.

Adhering to those guidelines, a computer engineering team designed and developed a family of computers that consists of three basic models:

- Model TC (Tactical Computer) — A briefcase-size computer for applications such as missile guidance, helicopters, satellites and submarines.
- Model CP (Customized Processor) — An intermediate-range processor for applications such as aircraft navigation, weapons delivery, radar correlation and mobile battlefield systems.
- Model EP (Extended Performance) — A large-scale data processor for applications requiring real-time processing of large volumes of data, such as manned spacecraft, airborne warning and control systems and command and control systems.

In 1966, System/4 Pi computers were selected for four major military programs with a current contract value to IBM of more than $50 million. Deliveries began in March 1967.

Typical computer configurations are shown in the illustration at the beginning of this section. The characteristics of each configuration are given in Table 1-1.

Table 1-1

TYPICAL SYSTEM/4 Pi COMPUTER CHARACTERISTICS

	Model TC	Model CP	Model EP
Applications	For satellites, tactical missiles, helicopters and other applications with overriding requirements for an exceptionally small, lightweight processor	For guidance and control, mobile battlefield systems, radar data correlation, weapons delivery, missile guidance and ELINT processing.	For military and space applications requiring extremely high-speed calculations involving large volumes of data, such as manned spacecraft and command and control systems.
Organization	general-purpose, parallel		
Main Storage	8,192 8-bit words, expandable to 65,536 words	8,192 32-bit words, expandable in 8,192 word increments	16,384 32-bit words, expandable in 8,192 word increments
Storage Cycle	2.5 μsec.		
Arithmetic	2's complement, fixed-point		2's complement, fixed-point; floating-point option
Data Word Length	16/32 bits		
Instruction Word Length	8/16/24 bits	16/32 bits	
Logic Control	conventional	conventional or microprogrammed	microprogrammed
Instruction Execution Times	Add: 9 μsec. Multiply: 48 μsec.	Add: 3.75 μsec. Multiply: 18.1 μsec.	Add: 2.1 μsec. Multiply: 9.2 μsec.
Weight	18 lbs.	50 lbs.	75 lbs.
Power	56 watts	250 watts	365 watts
Volume	0.38 cu. ft.	0.86 cu. ft.	1.88 cu. ft.

TECHNOLOGY

Circuits

Transistor-transistor logic (TTL) integrated circuits are used in all System/4 Pi computers. The circuits are currently available from several manufacturers.

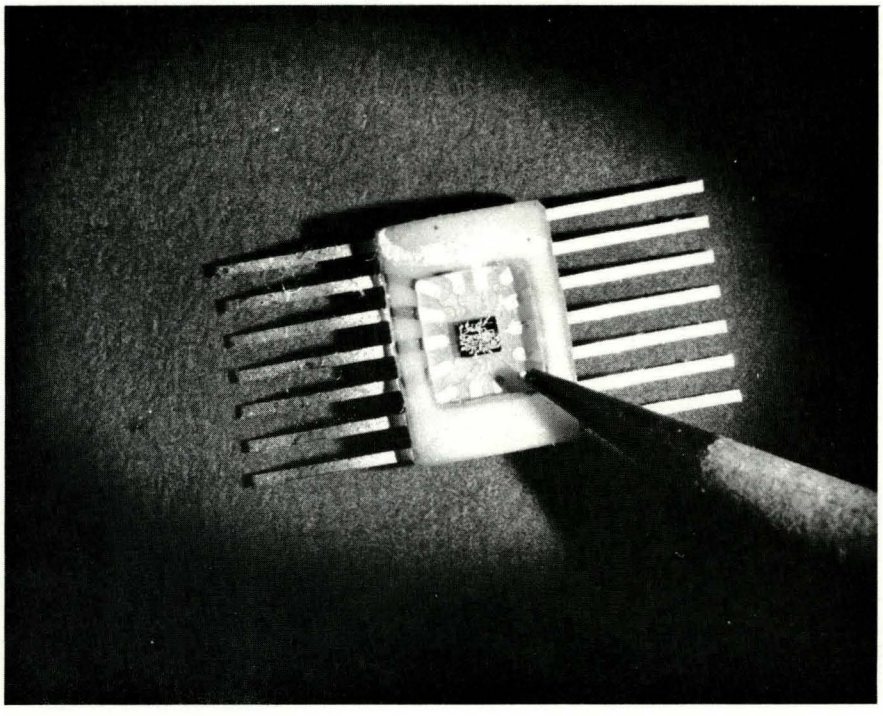


Figure 1-1. TTL Integrated Circuit

In addition to the standard quality control procedures followed by circuit manufacturers, IBM subjects the circuits to its own stringent quality screening. IBM's evaluation includes 100 per cent inspection, burn-in and acceleration/vibration testing. Complete failure analysis data is compiled and used in a reliability improvement program.

Multilayer Interconnection Boards

The basic pluggable electronic module of System/4 Pi is called a page. A page consists of two multilayer interconnection boards (MIBs) bonded to a metal frame. A MIB has up to six layers of printed circuit material bonded together under heat and pressure. Each layer consists of two sheets of etched copper separated by a glass substrate.

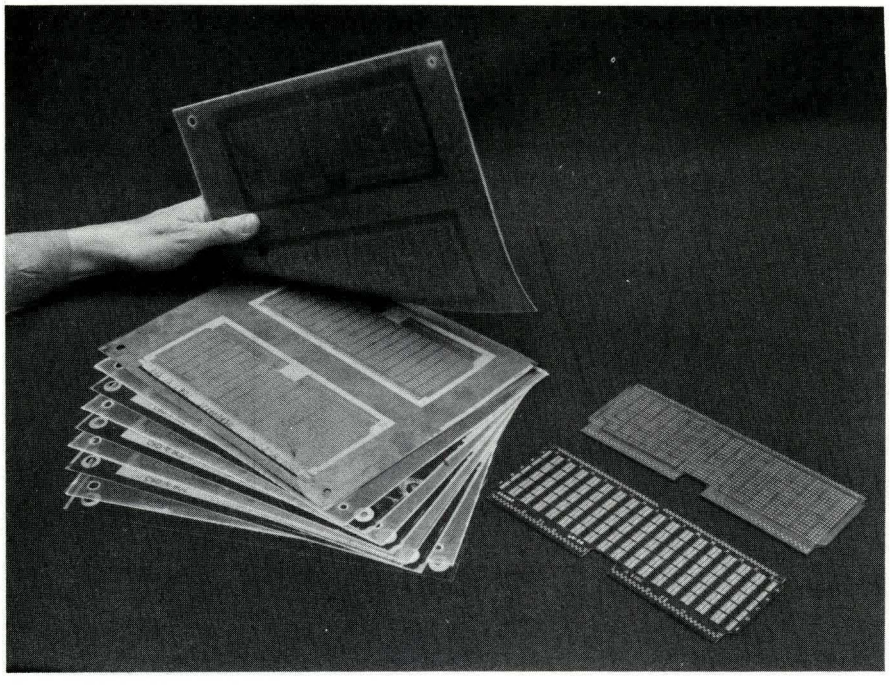


Figure 1-2. Layers of Typical MIB

Integrated circuits and discrete components are soldered to etched patterns on the surface of a MIB. Plated-through holes interconnect MIB layers. Feed-through holes are provided at the top of each MIB for interconnection between MIBs on each side of the metal frame. Figure 1-3 shows a typical page with integrated circuit flatpacks and discrete components.

The pages of a subassembly are interconnected by a MIB backpanel. Page connectors were developed by IBM for the Saturn V Launch Vehicle Digital Computer. The connectors are fully qualified and their reliability has been demonstrated.

IBM has been manufacturing multilayer interconnection boards for militarized applications for more than five years. Reliability rates are the highest in the aerospace and defense industry. A volume production line has been maintained to supply MIBs for advanced computer programs, including Titan II, Titan III, Gemini, Saturn I and Saturn V.

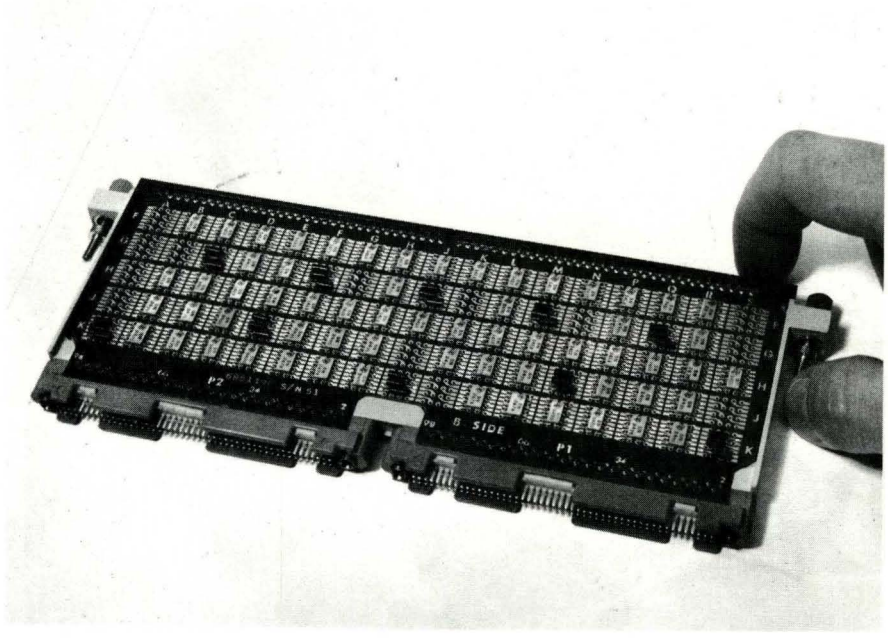


Figure 1-3. System/4 Pi Page

Main Storage

System/4 Pi main storage arrays are assembled from core planes that are militarized versions of those used in IBM System/360 computers. (See Figure 1-4.) The core material used for System/4 Pi is lithium-nickel ferrite, which maintains its magnetic properties over a wide temperature range.

Core dimensions are 0.013-inch inner diameter and 0.021-inch outer diameter. Each core plane contains 16,896 cores, which are automatically wired and tested. The basic storage module has 18 core planes stacked into an array. A conformal coating is applied to the planes for environmental protection of cores, and form padding is placed between planes to further ruggedize the array. Figure 1-5 shows a standard 4 Pi array.

The basic storage module contains 8,192 32-bit words. An additional 256 words are contained in the module, but those are usually reserved for I/O control purposes and are not addressable by the programmer. Additional 8,192-word modules may be added on a plug-in basis.

Read-Only Storage

In certain configurations of System/4 Pi, the computer control is implemented by microprograms contained in a read-only storage (ROS) device. Microprograms direct all activities within the computer, including

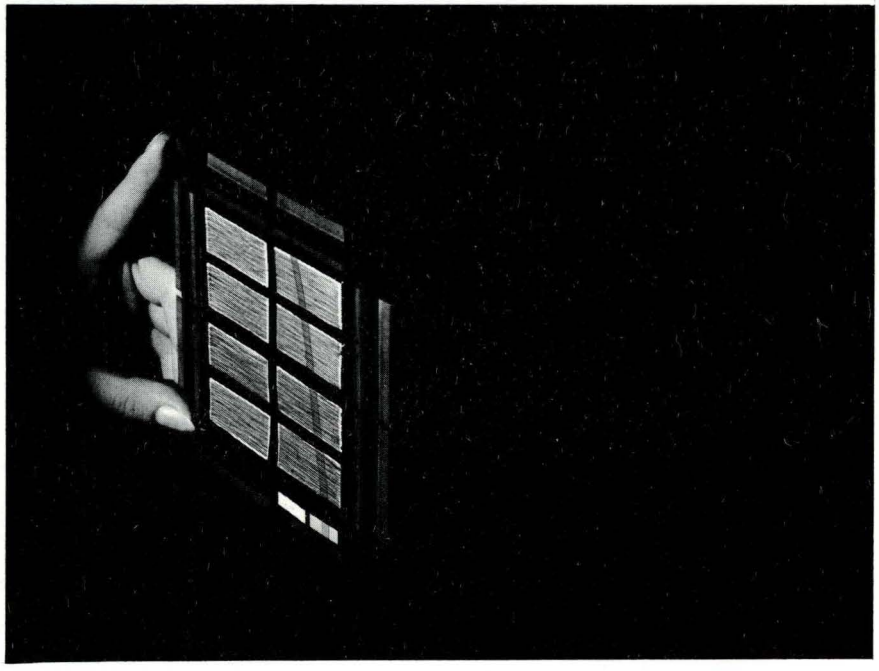


Figure 1-4. Main Storage Core Plane

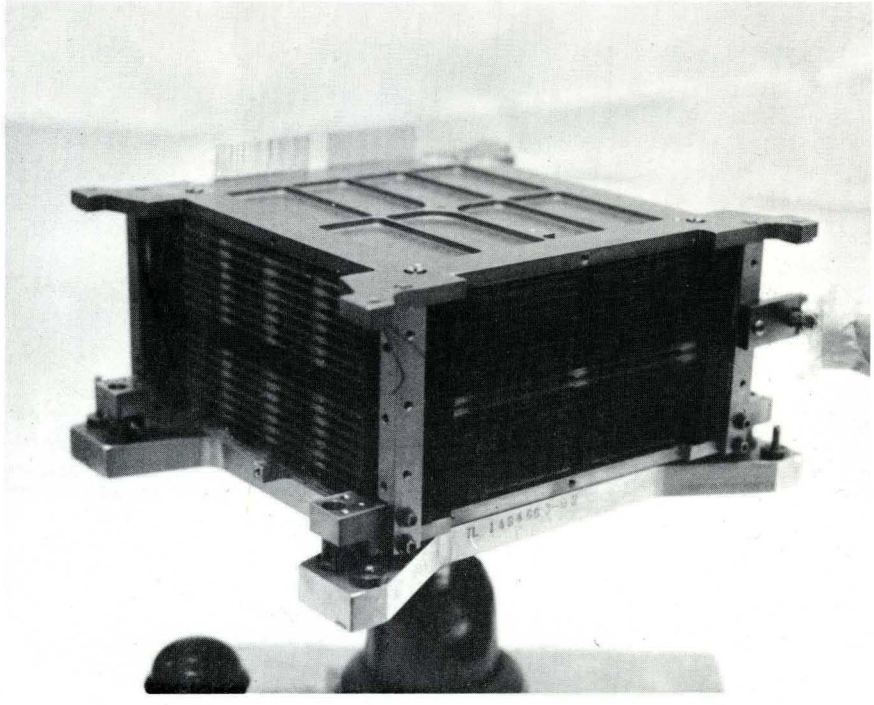


Figure 1-5. Main Storage Array

the selection of paths for data flow, the opening and closing of gates and registers, sequencing of events and all other functions to implement a logical operation or to effect a data transfer.

Unlike conventionally controlled computers, in which computer states have traditionally been stored in elements such as flip-flops, sequence triggers and latches, a microprogrammed processor's computer states are stored discretely in program-like form. When an instruction is read from main storage, the operation code portion specifies a starting address of a microroutine in ROS that will perform the step-by-step execution of the instruction. Every instruction in the computer's repertoire is microprogrammed and executed as a group of microinstructions in ROS.

In System/4 Pi, the ROS microprogrammed control is implemented with magnetic cores 0.007-inch inner diameter and 0.012-inch outer diameter. The cores are automatically wired into a word-organized array. A missing-core technique is used to form bit patterns and to implement the read-only function. A core at the intersection of two wires indicates a logical one, while the absence of a core indicates a logical zero.

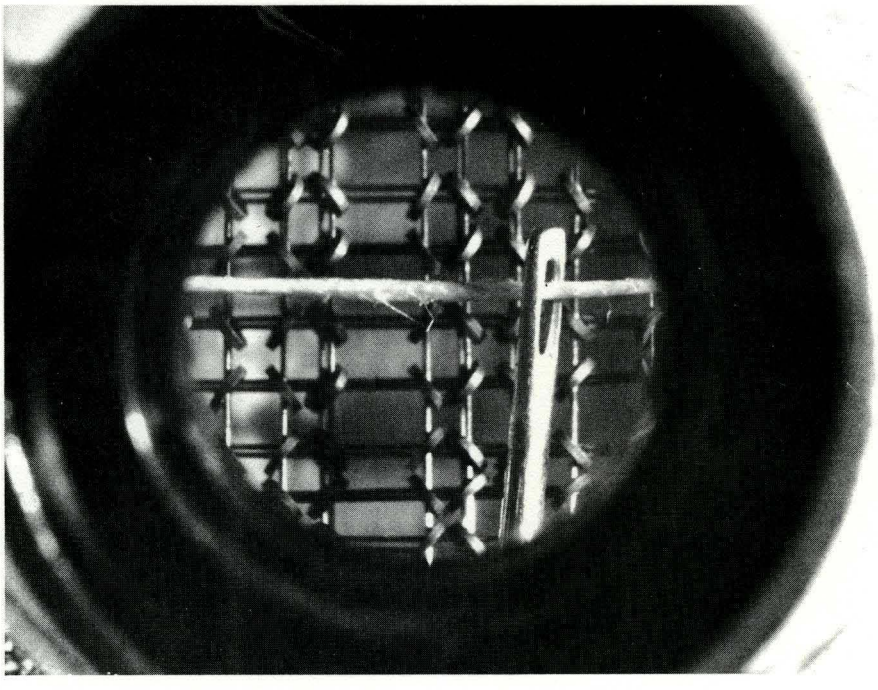


Figure 1-6. Magnified View of Needle and Thread on ROS Plane

ROS core planes are mounted on a MIB containing flatpack drive and sense circuits. Figure 1-7 shows a ROS plane and its associated electronics.

The primary advantage of a ROS-controlled computer is adaptability to special applications. Special microroutines, or application-oriented instructions, may be incorporated into the computer without hardware redesign. Iterative routines can often be executed ten times faster by implementing a ROS microroutine to replace a subroutine that is executed from main storage. This results in considerable savings of main storage locations. Since ROS is a pluggable unit, a user can defer selecting the exact instruction set for his particular application. When the problem to be solved is completely defined, an instruction set can be chosen that will customize the computer to the application.

ROS is expandable from 1,024 to 3,072 words, 70 or 100 bits in length. System/4 Pi Model EP is controlled by ROS, while ROS is offered as an option in Model CP.

MANUFACTURING TEST DATA SYSTEM (MTDS)

MTDS is a single hardware and software factory test equipment complex for System/4 Pi hardware. It consists of an IBM 1800 Data Acquisition and Control System (DACS), input/output adapters and peripheral data processing equipment. The 1800 DACS, when coupled to a suitable adapter unit, executes a program that completely tests a subassembly, assembly or final unit.

MTDS provides a unified solution to the problem of factory testing and eliminates the expense of individual manual tests of equipment, insuring high reliability testing at low cost.

MTDS is one of the most automated factory test complexes in existence. It will satisfy the testing requirements of IBM military and space hardware for at least five years.

Figure 1-8 shows the DACS and peripheral data processing equipment.

SUPPORT PROGRAMMING SYSTEM (SPS)

The SPS is a comprehensive set of programs for System/4 Pi computers. The SPS provides:

(1) Programming aids that enable a program to be expressed in a readily understood language.

(2) Facilities for storing, modifying and accessing precoded and assembled programs.

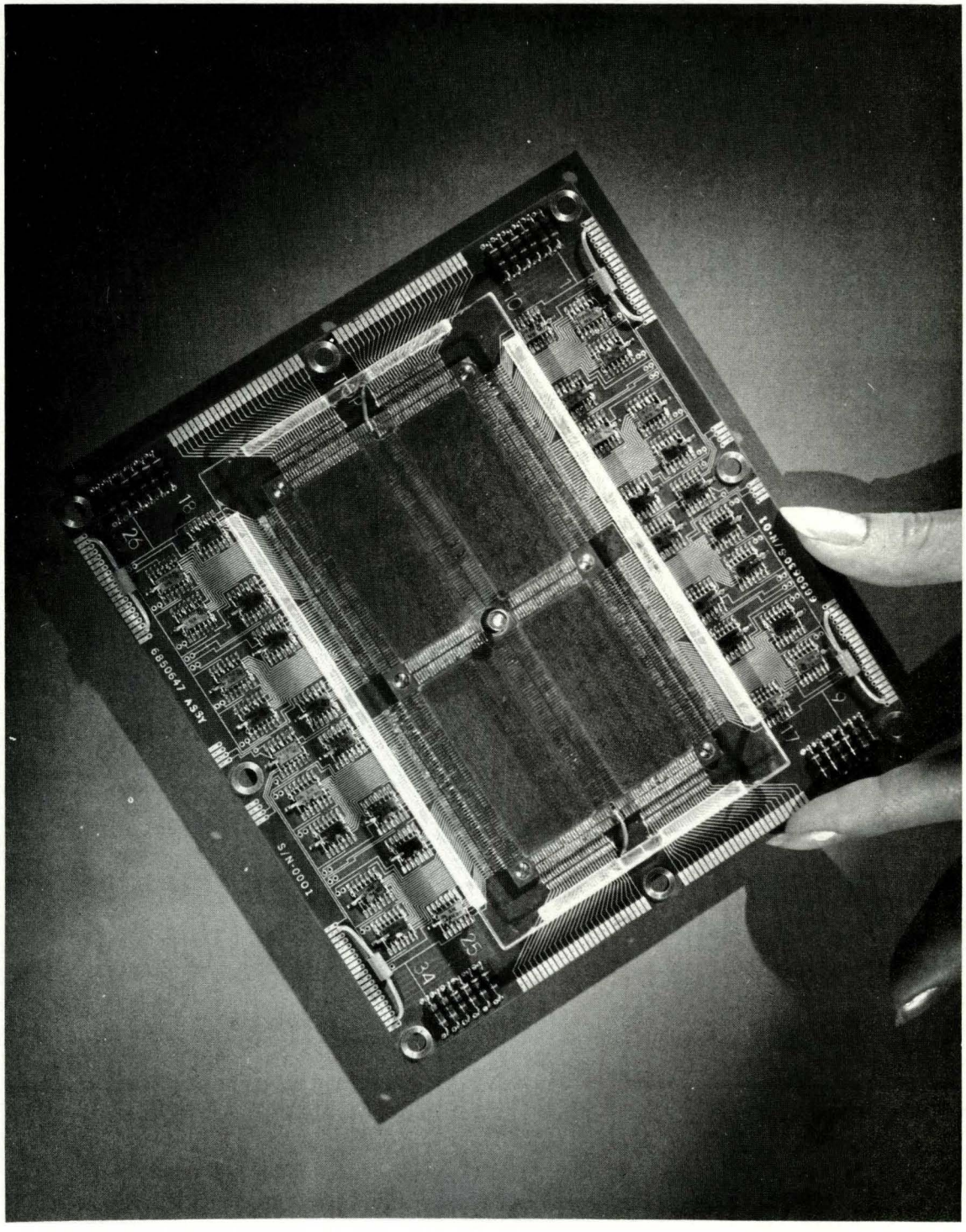


Figure 1-7. ROS Plane With Associated Electronics

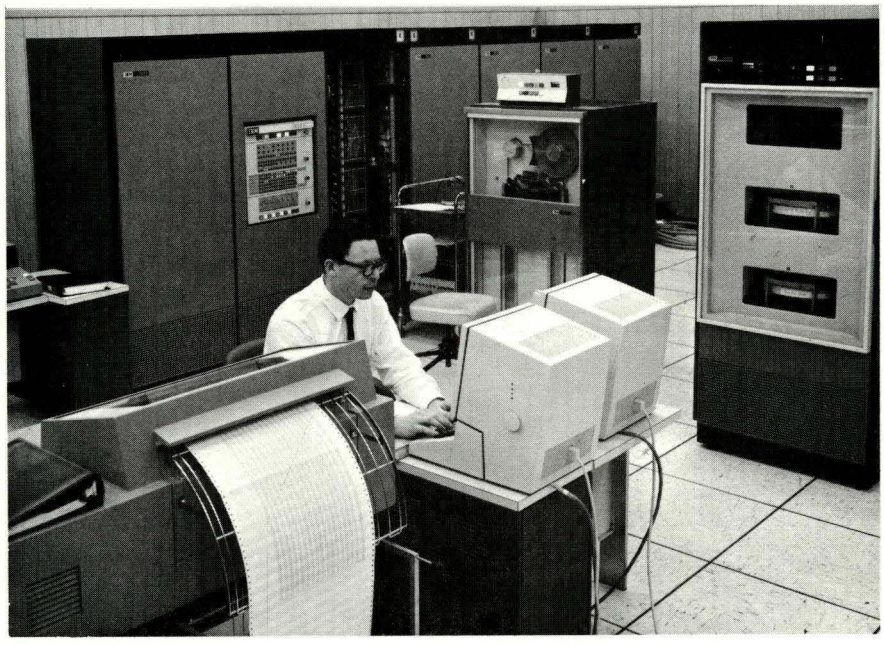


Figure 1-8. MTDS Data Acquisition and Control System with Peripheral Equipment

(3) A program checkout system that insures operational program readiness.

(4) Comprehensive documentation manuals.

The SPS operates on an IBM System/360 computer under the Disk Operating System. SPS programs include the following general facilities:

(1) Assembler

a) Assembly of relocatable programs

b) Various listings under program control

c) Error detection

d) Automatic selection of instruction format

e) Macro-processing and conditional assembly facilities

f) Machine operation definition

(2) Service Programs

a) Linkage Editor

- Combines and relocates programs assembled separately
- Resolves program linkages

b) Job Control

- Provides batch processing for handling the transistion from assembly to linkage editing to simulation

c) Library Maintenance and Service

- Maintains the system disk libraries
- Edits user source programs
- Displays or lists library contents

(3) Simulator

a) Dynamic simulation faciltated through control of a user's written FORTRAN program

b) User access to simulated computer object program data (with symbolic reference)

c) Object program correction

d) Program debugging options (dump, snap, trace)

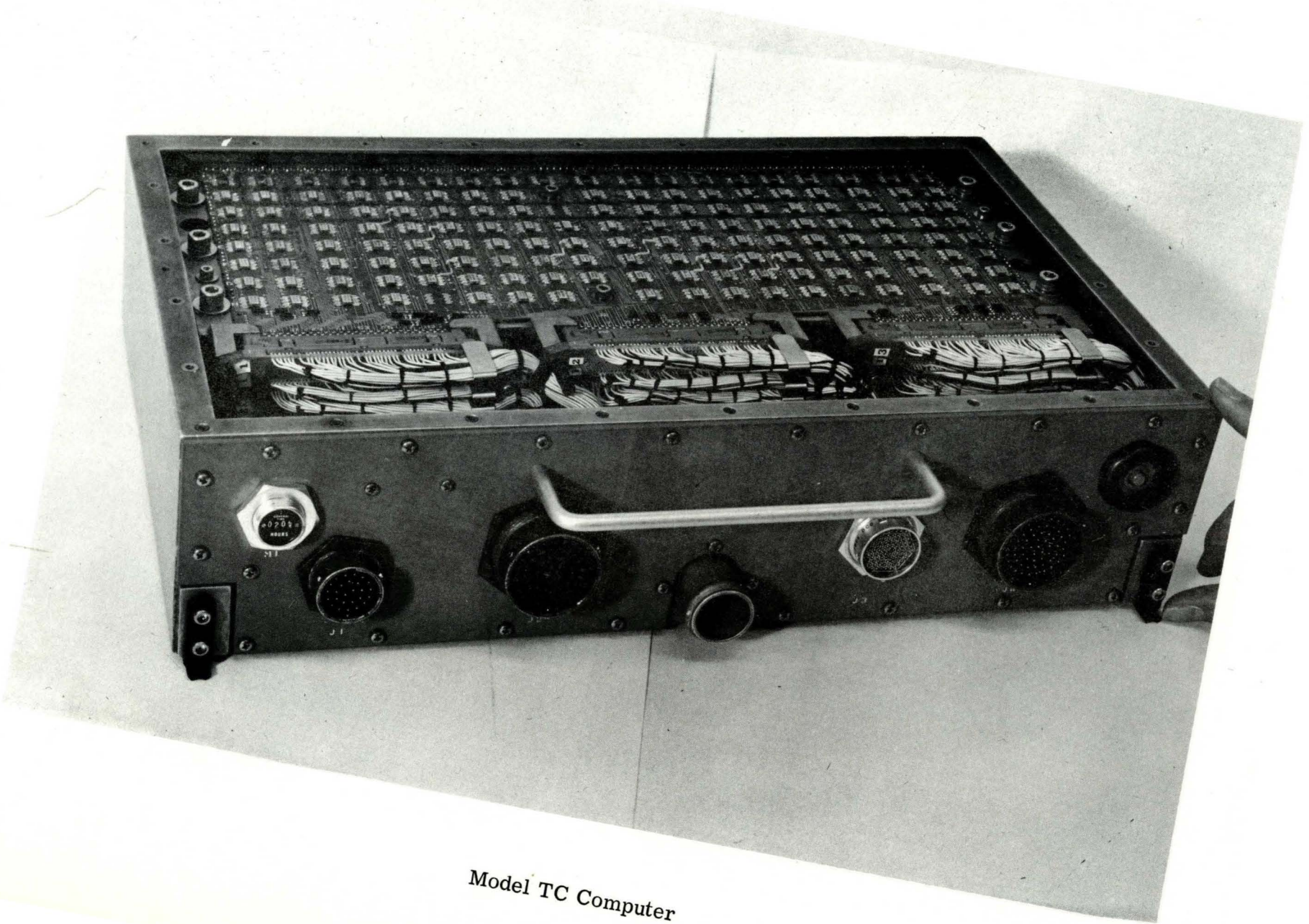
e) Simulation of input/output and interrupt initiation and response.

Support Programming Systems have been delivered and are being used by customers to develop operational programs for System/4 Pi computers. An SPS for each System/4 Pi computer model is available for immediate delivery.

Section 2

MODEL TC

(TACTICAL COMPUTER)



Model TC Computer

SUMMARY

The Model TC (Tactical Computer) is a general-purpose, stored-program, digital computer. It is designed for the low-cost, medium range of computational performance. Hardware requirements are minimized by using a byte (eight-bit) data transfer format and hardware registers to perform multifunctions.

The computer is subdivided into a storage, processor and I/O section. All signals entering or leaving the computer are digital in nature. The 2.5-microsecond, 8,192 bytes of core storage have a parallel eight-bit transfer path to the processor section and operate within a basic three-microsecond machine cycle. Storage is expandable to 16,384 bytes without modification.

The processor is organized as a three-bus system with eight-bit parallel data flow. The processor contains facilities for addressing main storage; fetching or storing information; performing arithmetic and logical data processing; sequencing and timing instructions, and initiating communications between storage and external equipment.

Working registers are located in both hardware and storage. Fifty-four instructions are implemented. Processing rates on the order of 50,000 operations a second are attained by optimizing the machine organization, and by using monolithic logic circuitry and high-speed core storage.

Model TC characteristics are summarized in Table 2-1.

DATA AND INSTRUCTION FORMATS

The Model TC has a standard 16-bit data word. A 32-bit data word may be used when double-precision accuracy is required.

Positive numbers are always in true-binary form; negative numbers are in 2's complement form.

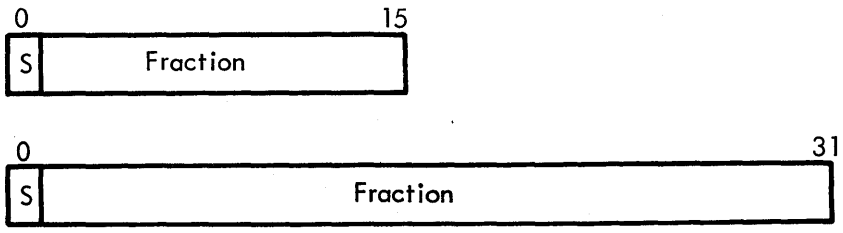


Figure 2-1. TC Data Formats

Table 2-1

MODEL TC CHARACTERISTICS

Type	General-purpose, digital
Organization	Parallel, fixed-point, 2's complement notation
Instructions	54
Instruction Word	8, 16 or 24 bits
Data Word	16 or 32 bits
Computer Cycle	3 μ sec.
Storage Cycle	2.5 μ sec.
Execution Times	
Add	9 μ sec.
Multiply	48 μ sec.
Divide	48 μ sec.
Physical	
Dimensions	10.0 x 16.5 x 4.0 in. (0.38 cu. ft.)
Weight	18 lbs.
Main Storage	8,192 bytes expandable to 65,536 bytes
Technology	TTL integrated circuits
Power	56 watts.
Environment	MIL-E-5400, Class 2

The instruction words in the Model TC are 8, 16 or 24 bits long.

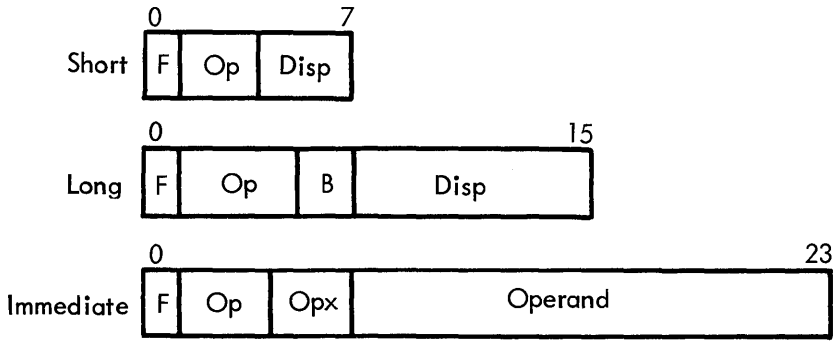


Figure 2-2. TC Instruction Formats

F	Controls instruction format. A zero indicates a short (eight bits) or immediate (24 bits) instruction and a one indicates a long (16 bits) instruction
OP	Defines the operation to be performed
DISP	Displacement value added to the contents of a base register to determine the effective storage address.
B	Designates the base register, if any, to be used in computing the operand address.
OPX	Used as extension bits to further define the operation to be performed

ADDRESSING

Byte locations in storage are consecutively numbered starting with address zero. A group of bytes in storage is addressed by the left-most byte of the group. The addressing capability permits a maximum of 65,546

bytes, using a 16-bit binary address. Some main storage locations are reserved for special purposes.

For addressing purposes, operands can be grouped in two classes: (1) explicitly addressed operands and (2) immediate operands placed as part of the instruction stream.

To permit the ready relocation of program segments and to provide for flexible specifications on input, output and working areas, all instructions referring to main storage employ a full storage address. The address used to refer to main storage is generated as follows:

> Base Address (B) is a 16-bit number contained in one of three storage registers specified in the B-field of the long format instruction. Base register one is implied when computing operand addresses for short format instructions. The base address can be used as a means of static relocation of programs and data. The base address provides addressing for the entire main storage. A special base register, designated linkage register (L), may be used to store the instruction counter for subroutine linking.
>
> Displacement (DISP) is binary number contained in the instruction formats. It is included as part of every address computation. The displacement provides relative addressing for up to 256 syllables (16-bit words) for long-format instructions and 16 syllables for short-format instructions.

In forming the address, the contents of the base register are treated as an unsigned 16-bit positive binary integer. The displacement is similarly treated as a positive binary integer. The two are added as 16-bit binary numbers, ignoring overflow. The resulting sum is the effective address of the left-most byte of the operand.

PROCESSOR ORGANIZATION

The data flow within the processor section is via one of three data buses: X, Y or main. The X-bus gates one of eight registers to the left side of the adder. The Y-bus gates one of three registers to the right side of the adder. Output data from the adder is distributed to any one of seven registers via the main bus. Data inputs and outputs to and from the I/O are transferred via the main bus.

The eight-bit adder uses binary full-adders, packaged one bit for each flatpack, thereby improving performance and packaging effectiveness. The adder executes all arithmetic and address computations. In addition to the add function, the adder also can perform AND, OR and EXCLUSIVE OR functions.

The hardware registers in the processor section are also packaged with two bits contained in each flatpack, without the requirement for external gating hardware.

The interrupt system implemented in the Model TC permits a change in the state of the computer in response to conditions external to the system. Three external interrupt lines are provided.

The occurrence of an interrupt sets a bit in the interrupt level status register (ILSR) and forces an instruction to Branch and Store Instruction Counter. The instruction counter is stored in a location permanently assigned to the interrupt. The interrupt handling routine reads the ILSR to determine the source of the interrupt and proceeds with the required processing.

The priority assigned to the interrupts is under program control. Interrupts are automatically masked during interrupt processing. Interrupts are unmasked under program control by the Load Status Word instruction, which resets the interrupt inhibit latch.

MAIN STORAGE

The Model TC uses an 8,192-word by eight-bit core storage with a 2.5-microsecond cycle time. The access time is 0.9 microseconds. A coincident-current (3D) selection scheme is used. The storage array requires four core planes. Figure 2-3 shows a Model TC main storage array. The operating ambient temperature range is -55°C to +100°C.

The monolithic circuits used in the main storage assembly are designed within state-of-the-art ground rules obtained from integrated circuit manufacturers. The high-voltage, high-current address driver and inhibit driver consist of monolithic pre-driver transformers coupled to discrete chip output stages packaged in flatpacks. The sense amplifier is a monolithic circuit with external networks for threshold setting.

INPUT/OUTPUT

The I/O section of the Model TC performs the following functions:

- Data Transfers. - A serial data channel is implemented which operates in a half-duplex mode. Transmission control is via the read and write command lines, computer supplied shift clock and 11 device address lines. The channel transfers are syllable (16 bits) with each input/output control (IOC) instruction (24-microsecond execution time). The transfer rate is one megahertz.

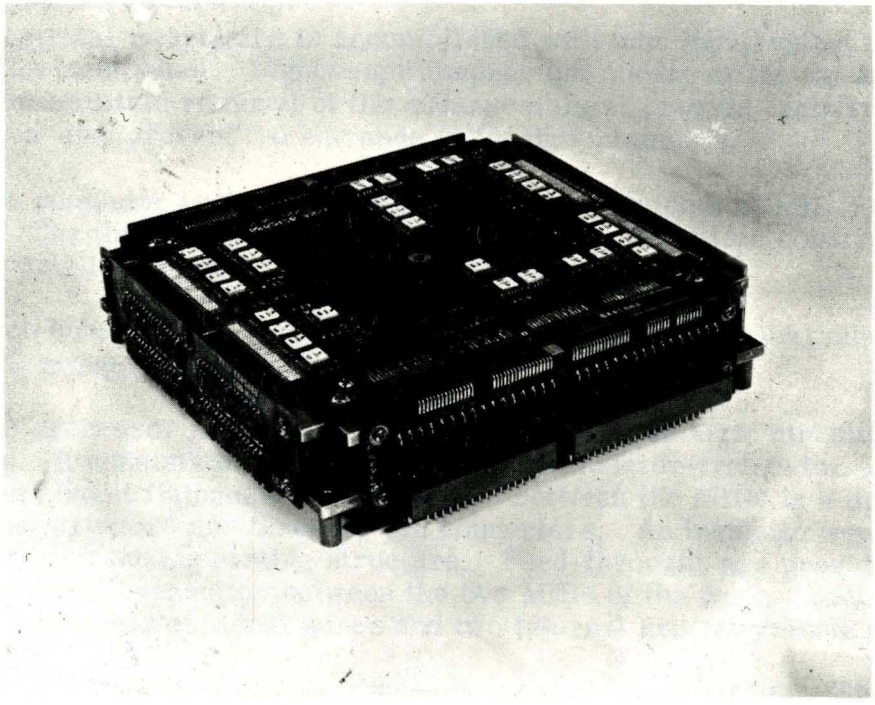


Figure 2-3. TC Main Storage Array

- Device Address Generation - Individual devices sharing the data channel are controlled by 11 address lines decoded from the address field of the IOC instruction word.

- Interrupt Control - All interrupts are buffered by a three-bit register. When an interrupt occurs, the corresponding bit is set and remains pending until the processor services the interrupt. Interrupts provide the only means of external interrogation of the computer.

- Real Time Clock - The I/O section contains a 24-bit real-time counter, driven at a 333-kilohertz bit rate by the computer clock.

The 16 high order bits of the 24-bit counter are read by the computer under program control. The low-order bit of the 16 bits changes state every 768 microseconds. The full range of the counter is in excess of 50 seconds.

PHYSICAL CHARACTERISTICS

The Model TC is packaged in a rugged aluminum structure containing three major subassemblies: processor, input/output, and storage. A wiring harness interconnects subassemblies. The heat generated by the subassemblies is removed by an air-cooled heat exchanger in the bottom of the computer structure.

Electrical interfacing is accomplished with four input/output connectors on the front panel. Lightweight magnesium covers at the top and back of the unit facilitate removal of the subassemblies, provide radio frequency attenuation and prevent the entrance of foreign materials.

The computer is designed to meet the requirements of MIL-E-5400, Class 2. The three subassemblies are all of the same basic construction, differing only in the type of electronic components.

Each subassembly (page) consists of two MIBs, a thermal mounting plate, I/O connectors and circuit components.

The processor page (Figure 2-4) contains all the logic circuitry of the computer. It consists of two MIBs on which transistor-transistor logic (TTL) integrated circuit flatpacks are soldered. Between the MIBs is a metal supporting structure and three 98-pin connectors. An insulator separates each MIB from the supporting structure. Feed-throughs are provided to allow electrical connection between the two MIBs of the page. Each MIB contains two levels of signal wires and two internal ground-voltage planes.

The I/O page is identical in design to the processor page. The timing and operational I/O is packaged on one side of the page and the logic for a portable storage loader is packaged on the other side.

The main storage page (Figure 2-5) contains an 8,192 by eight-bit storage array mounted on the underside. The drive and sense circuits are mounted on top of the page.

The storage array consists of the following subdivisions:

- Four core planes
- Two diode printed circuit boards
- Three resistor termination boards
- One X-line jumper board

INSTRUCTIONS

A complete list of Model TC instructions and execution times is contained in Table 2-2.

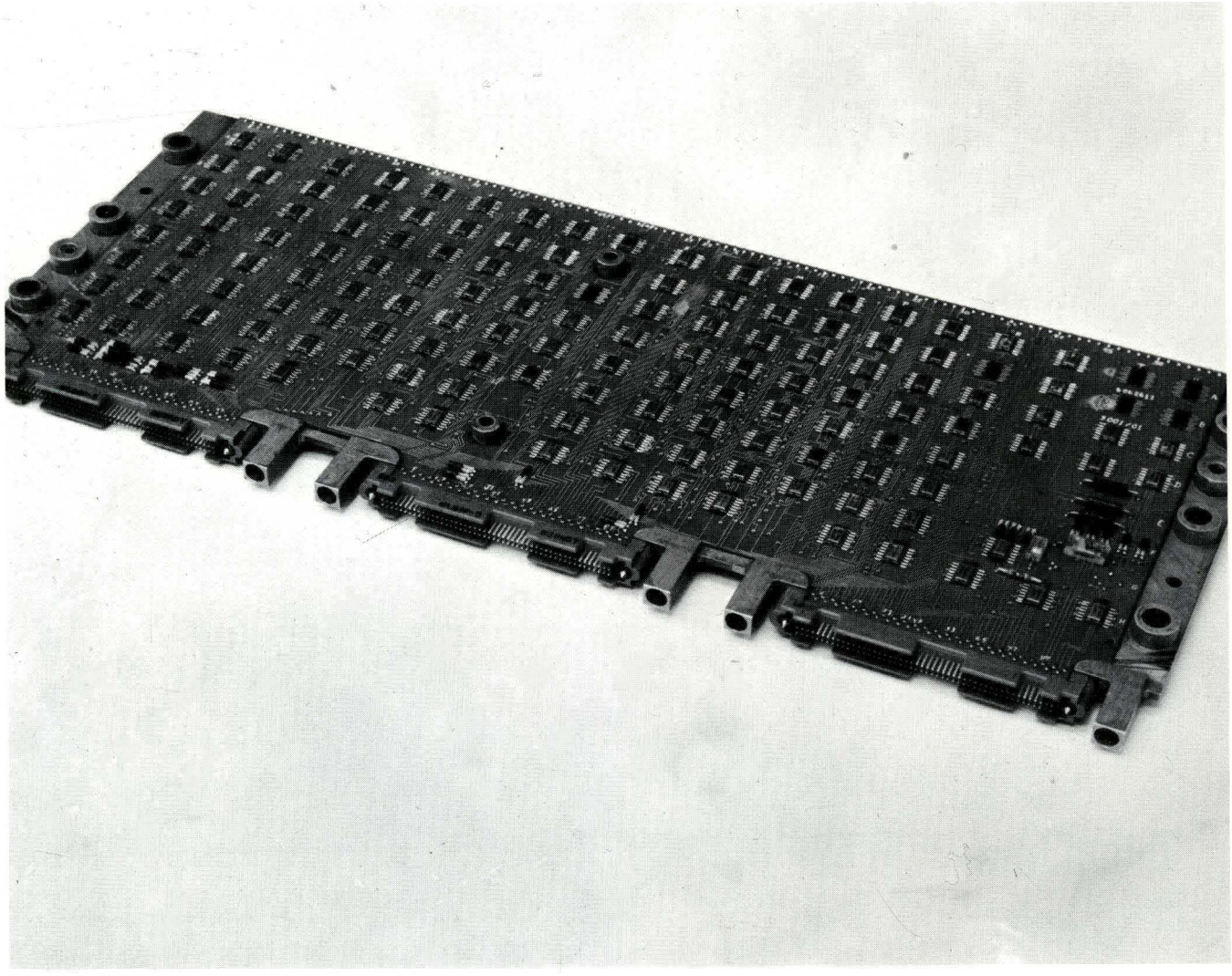


Figure 2-4. Model TC Processor Page

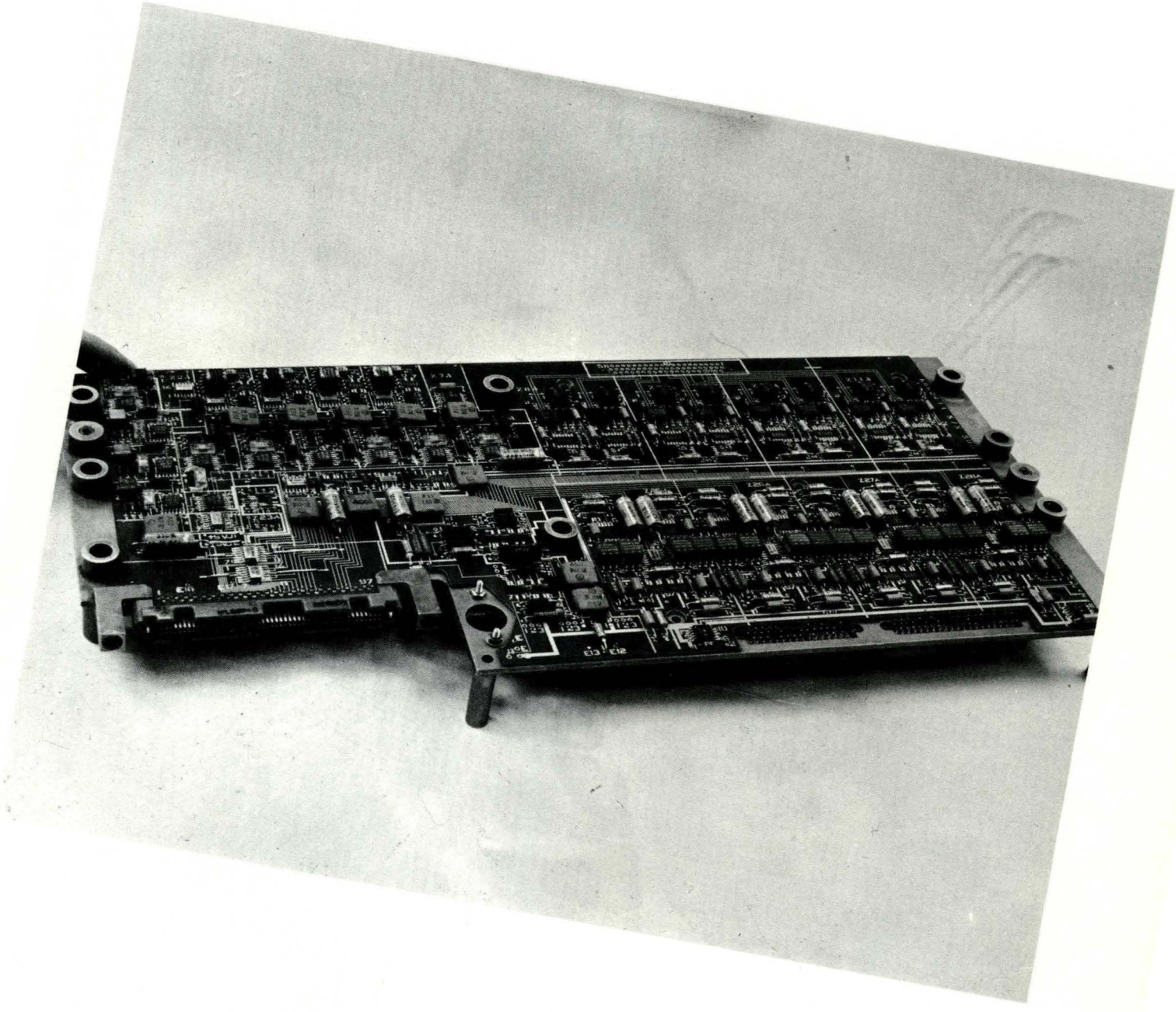


Figure 2-5. Main Storage Page

Table 2-2

MODEL TC INSTRUCTION LIST

Operation	Format	Execution Time (μsec.)
ADD	Short	15
ADD	Long	18*
ADD	Immediate	9
ADD DOUBLE	Long	24*
AND	Immediate	9
AND	Long	18*
ARITHMETIC COMPLEMENT	Short	3
BRANCH	Immediate	9
BRANCH	Long	12
BRANCH BACKWARD ON MINUS	Long	6
BRANCH BACKWARD ON PLUS	Long	6
BRANCH BACKWARD UNCONDITIONAL	Long	6
BRANCH BACKWARD ON ZERO	Long	6
BRANCH FORWARD ON MINUS	Long	6
BRANCH FORWARD ON PLUS	Long	6
BRANCH FORWARD UNCONDITIONAL	Long	6
BRANCH FORWARD ON ZERO	Long	6
BRANCH INDIRECT	Long	12
BRANCH INDIRECT & STORE IC	Long	18
COMPARE	Immediate	9
COMPARE	Long	18*
COMPARE DOUBLE	Long	24*
DIVIDE	Long	54*
EXCHANGE A & Q	Short	3
EXCLUSIVE OR	Long	18*
INPUT/OUTPUT CONTROL	Long	24*
LOAD A	Short	15
LOAD A	Long	18*
LOAD A	Immediate	9
LOAD BASE	Long	18
LOAD BASE 1	Immediate	15
LOAD BASE 2	Immediate	15
LOAD BASE 3	Immediate	15
LOAD DOUBLE	Long	24*

*Execution time is 6 μ sec less if B=00.

Table 2-2. Model TC Instruction List (cont.)

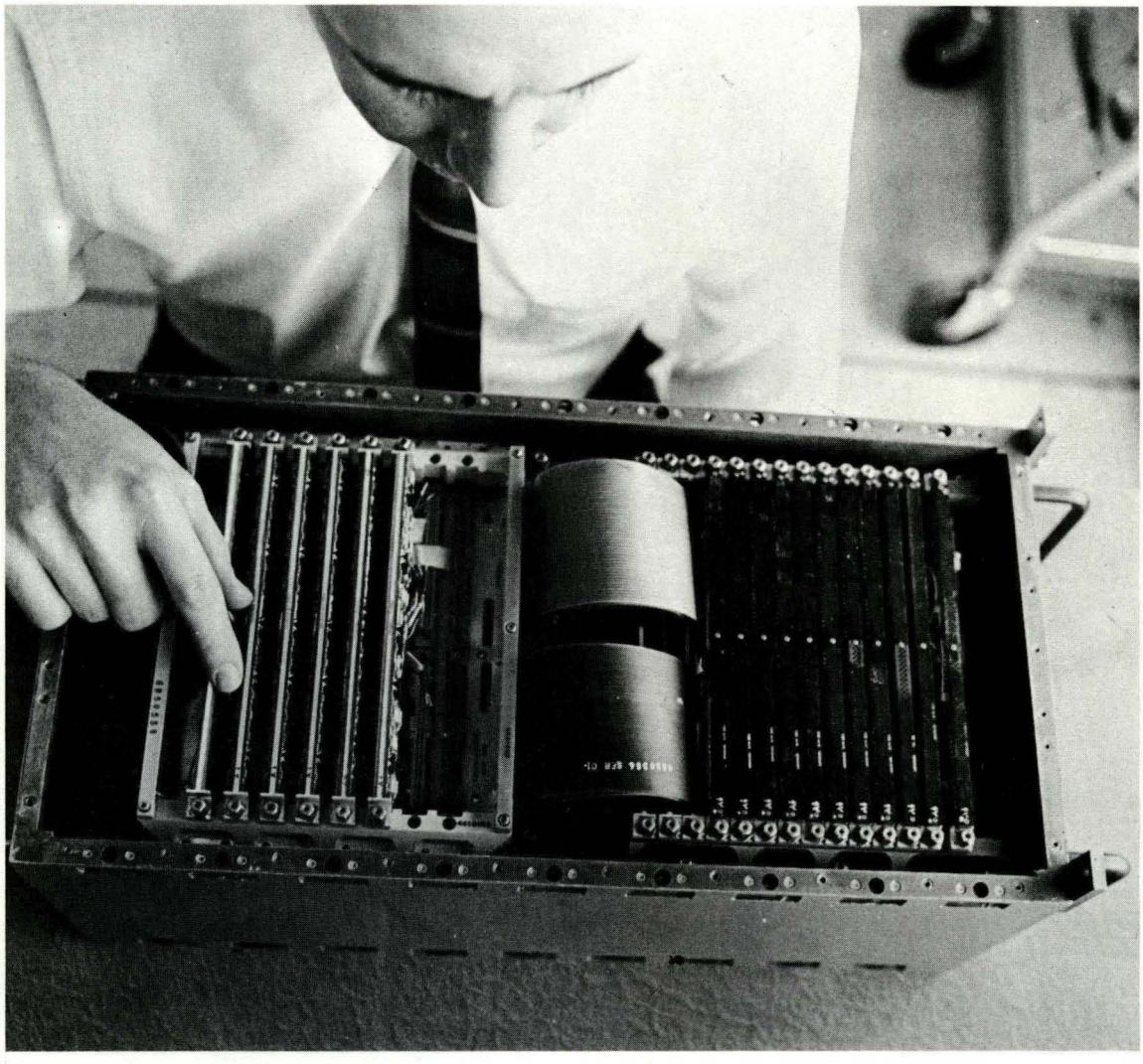
Operation	Format	Execution Time (μsec.)
LOAD STATUS WORD	Long	12
MODIFY BASE	Long	18
MULTIPLY	Short	51
MULTIPLY	Long	54*
NO OPERATION	Short	3
OR	Long	18
SHIFT LEFT DOUBLE	Short	6-18
SHIFT RIGHT ARITHMETIC DOUBLE	Short	6-18
SKIP ON CARRY	Short	3
STORE A	Short	15
STORE A	Long	18*
STORE BASE	Long	18
STORE DOUBLE	Long	24*
STORE IC	Long	18
STORE STATUS WORD	Long	12
SUBTRACT	Short	15
SUBTRACT	Long	18*
SUBTRACT DOUBLE	Long	24*
TALLY	Long	12-24
ZERO Q	Short	3

*Execution time is 6 μ sec. less if B=00.

Section 3

MODEL CP

(CUSTOMIZED PROCESSOR)



Model CP Computer

SUMMARY

The System/4 Pi Model CP (Customized Processor) is a general-purpose, fixed-point, digital computer. The rugged design and flexible control options satisfy varied applications such as real-time control, radar data correlation, navigation, guidance and weapons delivery.

The computer is subdivided into a central processing unit (CPU), main storage, input/output (I/O), an optional read-only storage (ROS) control and a power supply.

The 2.5-microsecond main storage contains 8,192 words, each 36 bits long. Two parity bits and two storage-protect bits are assigned to each storage word, with the remaining 32 bits forming the standard data word. Main storage is expandable in 8,192-word increments.

A microprogrammed logic control element, ideally suited to specialized applications, is available as an option with the Model CP. In the microprogrammed control configuration, each instruction read from main storage is implemented as a short subroutine of microinstructions executed from a ROS device. The movement of data between registers, through the adder, I/O transfers, etc., is completely under the control of microinstructions contained in ROS.

Working registers are located in high-speed hardware. Processing rates on the order of 125,000 operations a second are attained by optimizing the processor organization and by using monolithic logic circuitry and high-speed core storage. Much higher speeds are possible for specialized applications by implementing special microroutines and application-oriented instructions in ROS.

Model CP characteristics are summarized in Table 3-1.

DATA AND INSTRUCTION FORMATS

The Model CP is implemented with a standard 32-bit data word. A 16-bit halfword can also be used when the fullword accuracy is not required. (See Figure 3-1.)

Positive numbers are always in true binary form; negative numbers are in 2's complement form.

Table 3-1

MODEL CP CHARACTERISTICS

Type	General-purpose, digital
Organization	Parallel, fixed point, 2's complement notation
Instructions	61 (basic)
Instruction Word	16 or 32 bits
Data Word	16 or 32 bits
Computer Cycle	417 nsec.
Storage Cycle	2.5μsec.
Execution Times	
Add	3.75μsec.
Multiply	18.13μsec.
Divide	45.42μsec.
Physical	
Dimensions	10 x 7.6 x 19.4-in. (0.86 cu.ft.)
Weight	50 lbs.
Main Storage	8,192 x 32-bit words, expandable in 8,192 word increments
Technology	TTL integrated circuits
Power	250 watts
Environment	MIL-E-5400, Class 2

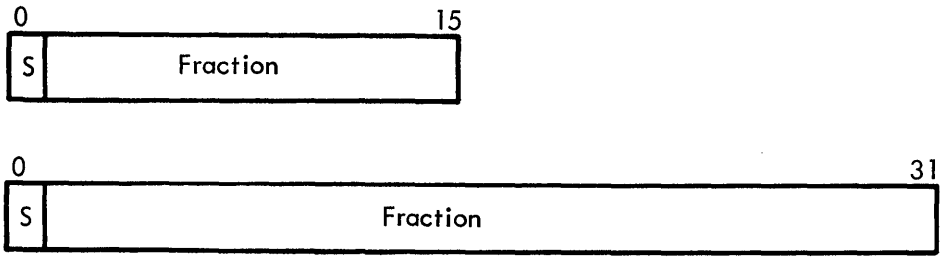


Figure 3-1. CP Data Formats

The instruction words are 16 or 32 bits long.

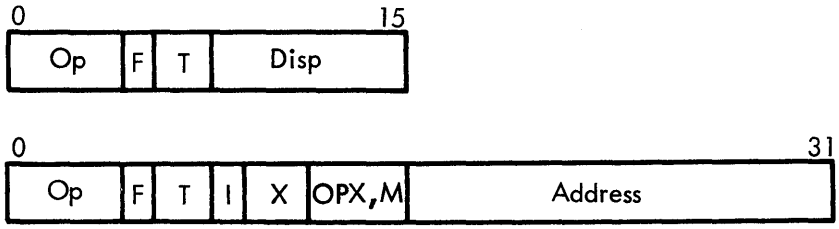


Figure 3-2. CP Instruction Formats

The bits within the instruction words are used as follows:

OP — Defines the operation to be performed.

F — Controls the instruction format. A zero indicates a normal format instruction and a one indicates a long format instruction.

T — Tag field addresses the index register or instruction register used in the address modification.

DISP — Displacement value added to the instruction register or the index register specified by T to compute the effective address (EA). If T is 00 (normal format only), the displacement is added to the Instruction Register. The displacement is in 2's complement form if negative, with the sign in bit 8. The bit in position 8 is automatically extended to the higher order bits (0-7) when the displacement is added to an index register.

I — Indirect addressing bit. If zero, addressing will be direct. If one, addressing will be indirect.

X — Specifies an additional register to be used for preliminary address modification.

OPX, M — Used as operation code extension or modifier, or as specific conditions for branch instructions.

ADDRESS — These 16 bits contain the address in a long format instruction. It can be modified by the contents of an index register or can be an indirect address.

ADDRESSING

All core storage locations are directly addressable under program control. The effective address may be determined by examining the tag, format and indirect address bits shown in Figure 3-2. The effective address is formed as shown in Table 3-2.

Table 3-2

EFFECTIVE ADDRESS GENERATION

Index Register	Relative Address	Direct Address	Indirect Address
0	Instruction Register + DISP*	ADDRESS	C (ADDRESS)**
1	XR1 + DISP	ADDRESS + XR1	C (ADDRESS + XR1)
2	XR2 + DISP	ADDRESS + XR2	C (ADDRESS + XR2)
3	XR3 + DISP	ADDRESS + XR3	C (ADDRESS + XR3)

*DISP may be positive or negative
**C means contents of ADDRESS field in instruction

The recognition of an indirect address control bit in an instruction will cause the address portion to be treated as an indirect address. The address, after indexing (if specified), gives the location of the effective address.

PROCESSOR ORGANIZATION

Data flow within the Model CP is via one of three main data buses: (1) the left adder bus, (2) the right adder bus or (3) the buffer bus. The left adder bus will gate one of several hardware registers to the left side of the adder. The right adder bus controls register gating in the right side of the adder. Output data from the adder is distributed to one of several hardware registers via the buffer register bus (BFR). Data inputs and outputs to the central processor are transferred via the BFR bus.

The interrupt system allows considerable flexibility for the programmer. Several levels of interrupt priority can be assigned. An automatic branch from the normal program sequence is initiated when an interrupt signal is detected. Interrupts are permitted immediately after the completion of an instruction. Each type of interrupt forces a branch to a unique address where the interrupt handling routine is stored. When the interrupt routine is completed, the next lower level interrupt is serviced, or the interrupted program is resumed.

INPUT/OUTPUT

A variety of I/O options are available on the Model CP. High-speed data channels that transfer 16 or 32 bits in parallel can be provided, operating under external or program control. Data rates on the order of 260,000 words a second are possible. In addition, the I/O section can address discrete inputs and outputs.

PHYSICAL CHARACTERISTICS

The Model CP is packaged in a dip-brazed aluminum structure. Heat generated from the subassemblies is conducted to the side walls of the structure. The walls consist of a hollow rectangular extrusion which forms a passage for the cooling air. Thin corrugated sheeting is brazed within the passage to provide the surface area for forced-air convection cooling and to make the structure rigid. The cooling air enters the passage on the rear panel and exits at the front panel.

Lightweight covers at the top and bottom of the unit facilitate removal of subassemblies, provide radio frequency attenuation and prevent entrance of foreign materials.

Table 3-3

MODEL CP BASIC INSTRUCTION SET

Operation	Format	Typical Execution Time (μsec.)
ADD	Normal	3.75
ADD	Long	5.00
ADD HALFWORD	Normal	3.75
ADD HALFWORD	Long	5.00
AND	Normal	3.75
AND	Long	5.00

Table 3-3. Model CP Basic Instruction Set (cont.)

Operation	Format	Typical Execution Time (μsec.)
BRANCH ON CONDITION	Long	4.58
BRANCH OUT ON CONDITION	Long	5.42
BRANCH AND STORE INSTRUCTION COUNTER	Normal	6.46
BRANCH AND STORE INSTRUCTION COUNTER	Long	7.71
COMPARE	Normal	4.79
COMPARE	Long	6.04
COMPARE HALFWORD	Normal	3.96
COMPARE HALFWORD	Long	5.21
DIRECT INPUT OUTPUT CONTROL	Normal	2.50
DIRECT INPUT OUTPUT CONTROL	Long	3.75
DIVIDE	Normal	47.29
DIVIDE	Long	48.54
EXCLUSIVE OR	Normal	3.75
EXCLUSIVE OR	Long	5.00
INSERT STORAGE PROTECT BIT	Long	5.42
LOAD A	Normal	3.75
LOAD A	Long	5.00
LOAD A HALFWORD	Normal	3.75
LOAD A HALFWORD	Long	5.00
LOAD INDEX	Normal	3.75
LOAD INDEX	Long	5.00
LOAD Q	Normal	3.75
LOAD Q	Long	5.00
LOAD STATUS WORD	Long	3.33
MODIFY INDEX	Normal	2.08
MODIFY INDEX	Long	3.33
MODIFY STORAGE HALFWORD	Long	5.83
MULTIPLY	Normal	18.13
MULTIPLY	Long	19.38
MULTIPLY HALFWORD	Normal	11.46
MULTIPLY HALFWORD	Long	12.71
OR	Normal	3.75
OR	Long	5.00
SHIFT LEFT	Normal	Varies
SHIFT LEFT AND COUNT	Normal	Varies
SHIFT LEFT AND COUNT DOUBLE	Normal	Varies
SHIFT LEFT DOUBLE	Normal	Varies
SHIFT RIGHT ARITHMETIC	Normal	Varies
SHIFT RIGHT ARITHMETIC DOUBLE	Normal	Varies

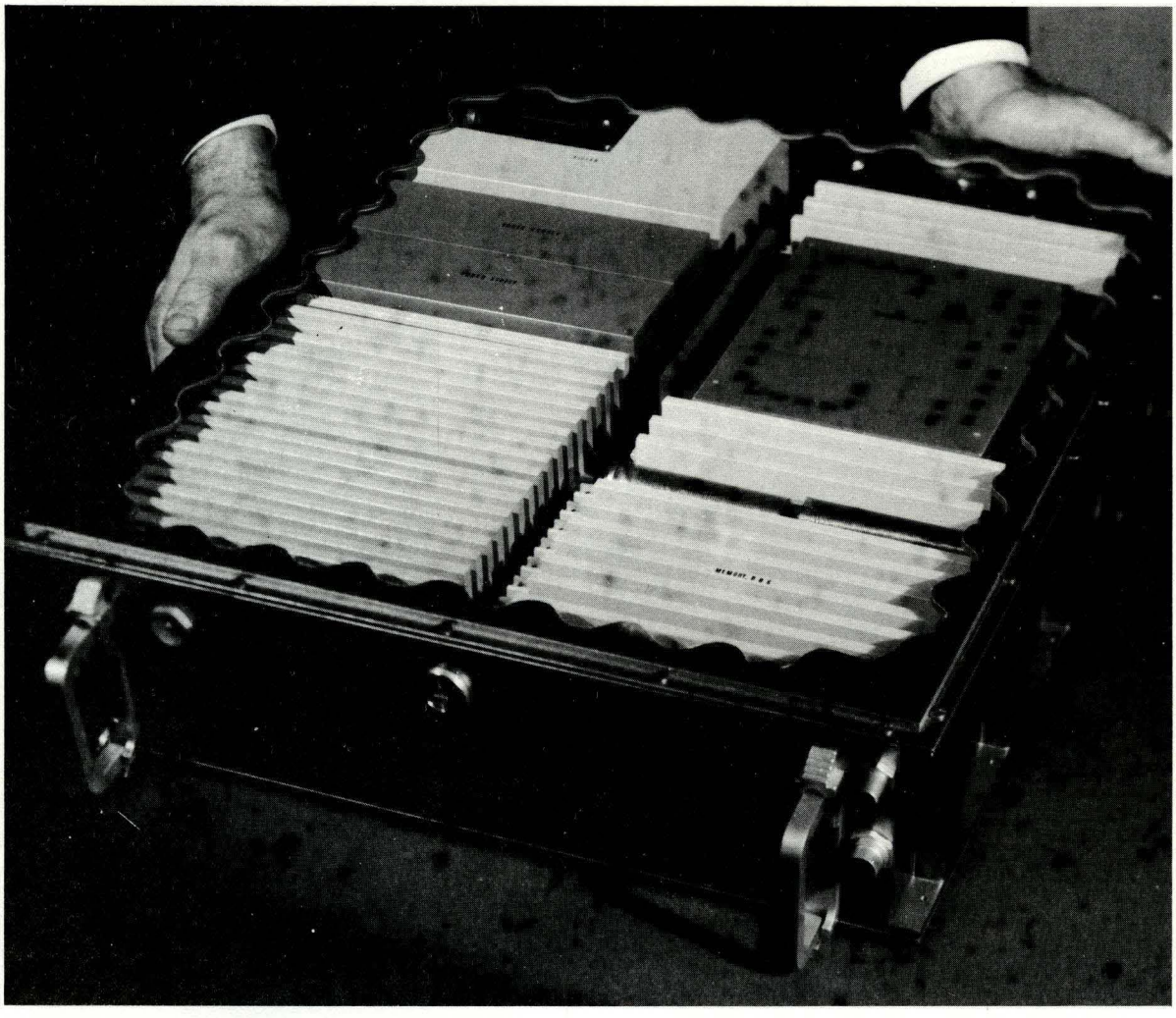
Table 3-3. Model CP Basic Instruction Set (cont.)

Operation	Format	Typical Execution Time (μsec.)
SHIFT RIGHT LOGICAL	Normal	Varies
SHIFT RIGHT ROTATE DOUBLE	Normal	Varies
SKIP ON CONDITION	Normal	2.71
STORE A	Normal	4.58
STORE A	Long	5.83
STORE A HALFWORD	Normal	5.42
STORE A HALFWORD	Long	6.67
STORE INDEX	Normal	5.42
STORE INDEX	Long	6.67
STORE Q	Normal	4.58
STORE Q	Long	5.83
STORE STATUS WORD	Long	5.42
SUBTRACT	Normal	3.75
SUBTRACT	Long	5.00
SUBTRACT HALFWORD	Normal	3.75
SUBTRACT HALFWORD	Long	5.00

Section 4

MODEL EP

(EXTENDED PERFORMANCE)



Model EP Computer

SUMMARY

The Model EP is a high-performance digital computer with a 32-bit parallel data flow. It features microprogram logic control, which provides flexibility in defining special instructions. Microprograms control data flow, permitting changes to a standard instruction set without changing computer hardware.

The 2.5-microsecond main storage contains 16,384 words, each 36 bits long. Four parity bits are included in each storage word, with the remaining 32 bits forming the standard data word. Main storage is expandable in 8,192-word increments.

The input/output section uses an IBM System/360 multiplexer channel augmented by a high-speed interface to handle high data rates. A multiplexer channel provides a flexible and economical means of attaching multiple devices to the computer by time-sharing the channel hardware between the various sub-channels. Up to 128 sub-channels (or devices) can be attached to the multiplexer channel.

The Model EP uses an instruction subset of IBM System/360. Therefore, user programs can be checked on System/360 computers to simplify the overall programming effort.

Model EP characteristics are summarized in Table 4-1.

DATA AND INSTRUCTION FORMATS

The Model EP is implemented with a standard 32-bit data word. (See Figure 4-1.) Sixteen-bit halfword operands may be specified for improved performance and storage efficiency. To preserve precision, some products and all dividends are 64 bits long.

Positive numbers are in true binary form. Negative numbers are in 2's complement form.

Instruction words are 16 or 32 bits long. (See Figure 4-2.)

Table 4-1

MODEL EP CHARACTERISTICS

Type	General-purpose, digital
Organization	Parallel, fixed-point, 2's complement notation (floating point optional)
Instructions	72 (basic)
Instruction Word	16 or 32 bits
Data Word	16 or 32 bits
Computer Cycle	417 nsec.
Storage Cycle	2.5μ sec.
Execution Times	
Add	2.1μ sec.
Multiply	9.2μ sec.
Divide	20.0μ sec.
Physical	
Dimensions	8.25 x 17.5 x 22.5-in. (1.88 cu. ft.)
Weight	75 lbs.
Main Storage	16,384 x 32 bit words, expandable in 8,192 word increments
Technology	TTL integrated circuits
Power	365 watts
Environment	MIL-E-5400, Class 2

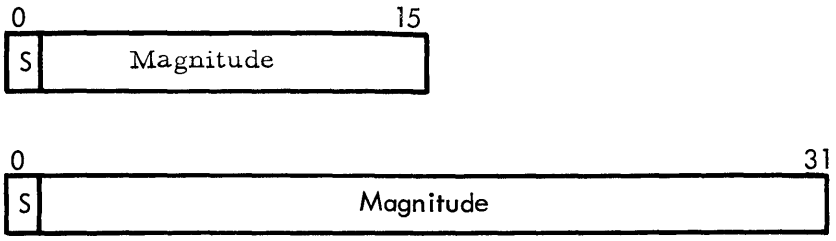


Figure 4-1. EP Data Formats

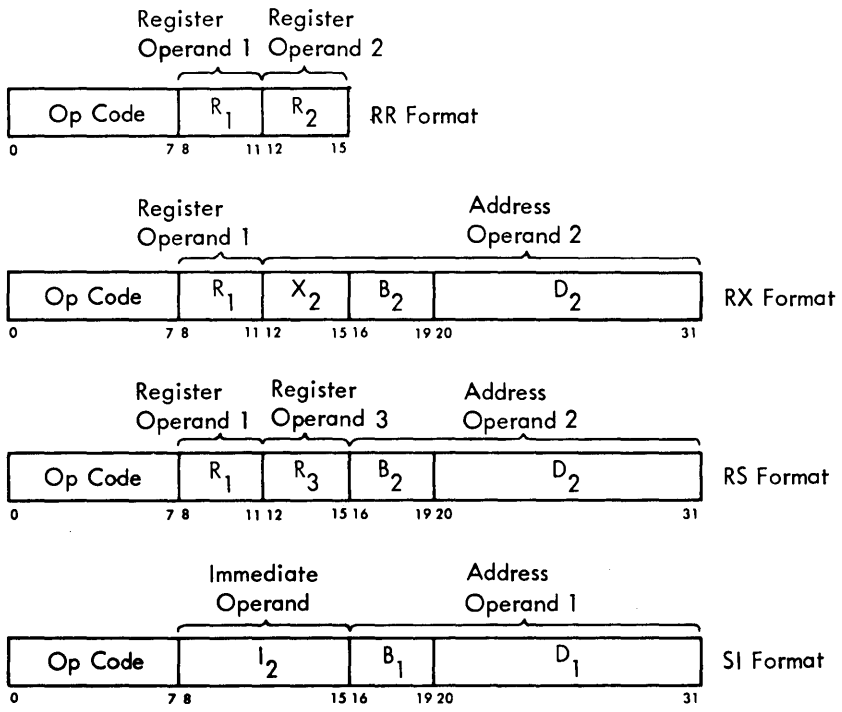


Figure 4-2. EP Instruction Formats

The bits within the instructions are used as follows:

Op Code	Defines the operation to be performed
R1	Specifies one of 16 registers to be used as the first operand
R2	Specifies one of 16 registers to be used as the second operand

X2	Specifies one of 16 registers to be used as an index to form the second operand address
B1	Specifies one of 16 registers to be used as the base to form the first operand address
B2	Specifies one of 16 registers to be used as the base to form the second operand address
D1	A displacement value that is added to the contents of a base and/or index register to form the first operand address
D2	A displacement value that is added to the contents of a base and/or index register to form the second operand address
I2	An eight-bit second operand contained as a part of the instruction.

The basic instruction formats are denoted by the format codes RR, RX, RA and SI. The format codes express, in general terms, the operation to be performed. RR denotes a register-to-register operation; RX, a register and indexed storage operation; RS, a register and storage operation, and SI, a storage and immediate operand operation.

ADDRESSING

Byte locations in storage are consecutively numbered starting with zero. A group of bytes in storage is addressed by the left-most byte of the group. Fixed-length fields, such as halfwords (16 bits), words (32 bits) and double words (64 bits), must be located in main storage on an integral boundary for that unit of information. For example, halfwords must have an address that is a multiple of the number two; words must be located in storage so that their address is a multiple of the number four, and double words must have an address that is a multiple of the number eight.

Operand addressing can be grouped into three classes: (1) explicitly addressed operands in main storage, (2) immediate operands placed as part of the instruction stream and (3) operands located in the general hardware registers.

The address used to refer to main storage is generated from the following three binary numbers:

- Base Address (B) is a 24-bit number contained in the low order 24 bits of register specified by the program in the B-field of the instruction. The B-field is included in every address computation. The base address can be used as a means of static relocation of programs and data.

- Index (X) is a 24-bit number contained in a general register specified by the program in the X-field of the instruction. It is included only in the RX instruction format. The index can be used to provide the address of an element within an array. Thus, the RX-format instructions permit double indexing.

- Displacement (D) is a 12-bit number contained in the instruction format. It is included in every address computation. The displacement provides for relative addressing up to 4,095 bytes beyond the element or base address. In array-type calculations, the displacement can be used to specify one of many items associated with an element. In the processing of records, the displacement can be used to identify items within a record.

In forming the address, the base address and index are treated as unsigned 24-bit positive binary integers. The displacement is similarly treated as a 12-bit positive binary integer. The three are added as 24-bit binary numbers, ignoring overflow. The sum of the three numbers is the effective address of the operand in main storage.

PROCESSOR ORGANIZATION

The processor contains facilities for addressing main storage, fetching stored information, performing arithmetic and logical processing of data, sequencing instructions and controlling the communications between main storage and external devices.

The processor has 16 32-bit general registers implemented in active hardware elements for fixed-point operands. The general registers can be used as base registers in address arithmetic, for indexing or as accumulators in fixed-point arithmetic and logical operations.

When the floating-point feature is added, four 64-bit general registers are provided to handle the floating-point operands.

The Model EP data flow consists primarily of two parallel paths, which may be activated simultaneously. One is a 32-bit-wide adder/shifter path fed by several 32-bit registers. The other is an eight-bit-wide mover path which performs logical operations on bytes of data selected from various processor registers. The computer operates on a 417-nanosecond cycle time, which is the time required for a register-to-register transfer through the adder/shifter path or through the mover path.

Interrupts in the Model EP are serviced by manipulating the program status word (PSW). This double word includes the instruction address, condition code and other fields reflecting the status of the computer. The active or controlling PSW is called the current PSW. By storing the current

PSW during an interrupt, the status of the computer at the time of interruption is preserved. By loading a new PSW or part of a PSW, the state of the computer can be initialized or changed.

The interrupt system permits the processor to change state as a result of conditions in the I/O devices, conditions in the computer or conditions external to the system. Interrupts are demands for immediate computer response. They are processed by a forced departure from the normal program instruction processing routine. Normal requests for I/O service are not classified as interrupts.

Six classes of interrupts are honored by the Model EP:

- Input/Output - conditions generated in the multiplexer channel or I/O devices
- External - conditions generated that are external to the computer.
- Program - unusual conditions encountered in a program
- Supervisor Call - result of executing the SUPERVISOR-CALL instruction
- Machine check - result of a machine malfunction
- Power Transient Detection - results when input power is at an abnormal level. This is a special sub-class machine check.

INPUT/OUTPUT

The Model EP input/output data transfers, as well as certain control signals, are routed between external devices and the main storage via the input/output multiplexer channel and control units. The only other external interface to the computer is through the external interrupt system. Each control unit provides interface adaptation between the multiplexer channel and I/O devices. A single control unit accommodates input and output devices.

The basic data flow is between an I/O device and the multiplexer channel via a control unit, and between multiplexer channel and storage via the processor. Storage locations are arbitrarily assigned as input/output data buffering areas. The assignment of buffer areas is under control of the programmer, and a field of any length can be assigned anywhere in storage.

The multiplexer channel has two basic modes of operation: (1) multiplex mode and (2) burst mode. The capability to sustain several I/O operations on a time-shared basis in the multiplex mode is the most important

feature of the multiplexer channel. In that mode, the channel services the I/O devices asynchronously as the input data becomes available, or when the output devices can accept more data. Each data transfer consists of one byte of data (eight bits) plus a parity bit to verify proper transmission.

The burst mode is an alternate multiplexer channel operation. In that mode, the channel remains connected to a particular device until the transfer of a block of data is completed. All other devices are normally locked out of the channel until the end of the burst transmissions. The burst mode is usually reserved for high-speed, long-record transfers. As in all standard data transfers, the transmission is one byte in parallel. The burst mode can also be used for lower-speed program loading from a tape unit when it is desirable to block off other I/O operations.

PHYSICAL CHARACTERISTICS

The Model EP is packaged in a magnesium-lithium structure. To insure adaptability to all environments, the computer may be cooled by forced air or liquid.

All elements within the structure (pages, ROS assembly, main storage assembly, power supply and RFI filter) are pluggable. Each of the pluggable elements occupies an area less than four inches high and eight inches wide. Lightweight covers at the top and bottom of the structure provide access to all subassemblies during detailed maintenance.

INSTRUCTIONS

A list of the Model EP basic instructions and execution times is included in Table 4-2. The instructions provided with the optional floating-point feature are given in Table 4-3. A short-format floating-point instruction uses 32-bit operands, while a long format instruction uses 64-bit operands.

Table 4-2

MODEL EP BASIC INSTRUCTION LIST

Operation	Format	Execution Time (μsec.)
	FIXED POINT	
LOAD	RR	1.9
LOAD	RX	5.0
LOAD HALFWORD	RX	5.0
LOAD AND TEST	RR	1.9
LOAD COMPLEMENT	RR	2.1
LOAD POSITIVE	RR	2.1
LOAD NEGATIVE	RR	2.1

Table 4-2. Model EP Basic Instruction List (cont.)

Operation	Format	Execution Time (μsec.)
	FIXED POINT	
LOAD MULTIPLE	RS	Variable
ADD	RR	2.1
ADD	RX	5.0
ADD HALFWORD	RX	5.4
ADD LOGICAL	RR	2.1
ADD LOGICAL	RX	5.0
SUBTRACT	RR	2.1
SUBTRACT	RX	5.0
SUBTRACT HALFWORD	RX	5.4
SUBTRACT LOGICAL	RR	2.1
SUBTRACT LOGICAL	RX	5.0
COMPARE	RR	2.1
COMPARE	RX	5.0
COMPARE HALFWORD	RX	6.0
MULTIPLY	RR	9.2
MULTIPLY	RX	10.4
MULTIPLY HALFWORD	RX	11.6
DIVIDE	RR	20.0
DIVIDE	RX	20.8
STORE	RX	5.0
STORE HALFWORD	RX	5.0
STORE MULTIPLE	RX	Variable
SHIFT LEFT SINGLE	RS	Variable
SHIFT RIGHT SINGLE	RS	Variable
SHIFT LEFT DOUBLE	RS	Variable
SHIFT RIGHT DOUBLE	RS	Variable
	LOGICAL	
COMPARE LOGICAL	RR	1.9
COMPARE LOGICAL	RX	5.0
COMPARE LOGICAL	SI	5.4
AND	RR	3.4
AND	RX	5.0
OR	RR	3.4
OR	RX	5.0
EXCLUSIVE OR	RR	3.4
EXCLUSIVE OR	RX	5.0
TEST PARITY	RX	5.0
TEST UNDER MASK	SI	5.0
SUMCHECK	RX	Variable
INSERT CHARACTER	RX	5.0

Table 4-2. Model EP Basic Instruction List (cont.)

Operation		Execution Time (μsec.)
	LOGICAL	
STORE CHARACTER	RX	5.0
LOAD ADDRESS	RX	2.9
SHIFT LEFT SINGLE LOGICAL	RS	Variable
SHIFT RIGHT SINGLE LOGICAL	RS	Variable
SHIFT LEFT DOUBLE LOGICAL	RS	Variable
SHIFT RIGHT DOUBLE LOGICAL	RS	Variable
	BRANCHING	
BRANCH ON CONDITION	RR	4.2
BRANCH ON CONDITION	RX	4.4
BRANCH AND LINK	RR	4.0
BRANCH AND LINK	RX	4.1
BRANCH ON COUNT	RR	4.2
BRANCH ON COUNT	RX	4.4
	STATUS SWITCHING	
LOAD PSW	SI	7.5
LOAD PSW SPECIAL	SI	9.0
SET PROGRAM MASK	RR	2.1
SET SYSTEM MASK	RR	5.0
CHANGE PRIORITY MASK	SI	5.4
SUPERVISOR CALL	RR	15.0
SET STORAGE KEY	RR	4.5
INSERT STORAGE KEY	RR	5.0
	I/O	
START I/O	SI	Variable
TEST I/O	SI	Variable
HALT I/O	SI	Variable
TEST CHANNEL	SI	Variable
READ DIRECT	SI	Variable
WRITE DIRECT	SI	Variable

Table 4-3

MODEL EP OPTIONAL FLOATING POINT INSTRUCTION LIST

Operation	Format	Execution Time (μsec.)
LOAD (LONG)	RR	2.9
LOAD (LONG)	RX	6.2
LOAD (SHORT)	RR	2.5
LOAD (SHORT)	RX	5.1
LOAD AND TEST (LONG)	RR	3.3
LOAD AND TEST (SHORT)	RR	2.5
LOAD COMPLEMENT (LONG)	RR	3.3
LOAD COMPLEMENT (SHORT)	RR	2.5
LOAD POSITIVE (LONG)	RR	3.1
LOAD POSITIVE (SHORT)	RR	2.5
LOAD NEGATIVE (LONG)	RR	3.1
LOAD NEGATIVE (SHORT)	RR	2.5
ADD NORMALIZED (LONG)	RR	5.4
ADD NORMALIZED (LONG)	RX	8.3
ADD NORMALIZED (SHORT)	RR	4.2
ADD NORMALIZED (SHORT)	RX	5.0
ADD UNNORMALIZED (LONG)	RR	5.4
ADD UNNORMALIZED (LONG)	RX	8.3
ADD UNNORMALIZED (SHORT)	RR	5.0
ADD UNNORMALIZED (SHORT)	RX	5.8
SUBTRACT NORMALIZED (LONG)	RR	5.4
SUBTRACT NORMALIZED (LONG)	RX	8.3
SUBTRACT NORMALIZED (SHORT)	RR	4.2
SUBTRACT NORMALIZED (SHORT)	RX	5.0
SUBTRACT UNNORMALIZED (LONG)	RR	5.4
SUBTRACT UNNORMALIZED (LONG)	RX	8.3
SUBTRACT UNNORMALIZED (SHORT)	RR	5.0
SUBTRACT UNNORMALIZED (SHORT)	RX	5.8
COMPARE (LONG)	RR	5.0
COMPARE (LONG)	RX	7.5
COMPARE (SHORT)	RR	3.8
COMPARE (SHORT)	RX	4.7
HALVE (LONG)	RR	2.9

Table 4-3. Model EP Optional Floating Point Instruction List (cont.)

Operation	Format	Execution Time (μsec.)
HALVE (SHORT)	RR	2.5
MULTIPLY (LONG)	RR	35.0
MULTIPLY (LONG)	RX	38.0
MULTIPLY (SHORT)	RR	15.0
MULTIPLY (SHORT)	RX	18.0
DIVIDE (LONG)	RR	42.0
DIVIDE (LONG)	RX	50.0
DIVIDE (SHORT)	RR	19.0
DIVIDE (SHORT)	RX	22.0
STORE (LONG)	RX	9.0
STORE (SHORT)	RX	5.5

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