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3880 Storage Control Model 23 Maintenance Support Manual

3880 MSM	Seq JA0010	PN 6315755 1 of 2	881216 15 Aug 84	A15621 01 Apr 85			

Preface

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Groups of pages can be ordered by including a description (section, volume) and the machine serial number.

Related Publications

A list of related publications can be found in the Maintenance Support Manual, REF section.

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Introduction

Contents of This Section

Description By Section

The 3880 Maintenance Support Manual (MSM) is divided into sections identified by tabs.

The following is a description of the tab labels and the section content.

INTRO Intro-duction

The Introduction section defines the organization of the manual and content of the manual sections.

SENSE Sense Data

The Sense section contains a summary and detailed description of the sense data.

OPER Operations

The Operations section contains data and control flow diagrams and descriptions of the product. Included are description on the:

Subsystem
Functional Areas
Logic cards
Commands
Initial Microcode Load
Storage Director Communications

PDA Problem Determination Aids

The Problem Determination Aids section describes the use, selection, and interpretation of the following topics:

- Trace program
- Dynamic trace tables
- Sync and save tables
- State save tables
- Maintenance connection trace tables
- Abnormal maintenance connection conditions
- Unusual operating conditions
- Unusual maintenance conditions
- Generalized trace facility
- Channel monitor
- Logic analyzer

REF Reference

The Reference section contains tables and descriptions of the external, general, common, and upper and lower port registers.

MD Maintenance Device

The Maintenance Device section describes the interaction of the maintenance device with a storage director that is actively attached to a processor channel.

Sense

Contents of This Section

References to Other Sections

See the REF section for a description of the external and indirect registers.

Formats

The 3880 gives 24 bytes of sense information arranged into error formats. These formats are used to class errors because of where they come from and are reported. The errors can be found in the channel, storage control, subsystem storage, or the device.

The formats are:

Format	Condition
0	Program or system checks
1	Device equipment checks
2	Storage director equipment checks
3	Storage director control checks
4	Uncorrectable data checks
5	Correctable data checks
6	Usage, overrun, and error statistics
7	Controller check 1 (Model 23 only)
8	Controller check 2 and device check 1 (Model 23 only)
F	Subsystem storage errors.

Of these formats, only formats 0, 2, 3, 6 and F are used by the 3880, and only these formats are described in this SENSE section. The remaining formats (1, 4, 5, 7, and 8) describe errors detected and reported by the devices and are described in the device documentation.

Format 0 – Program or System Checks

Format 0 is all program or system check errors. These checks occur in the channel or the channel side of the channel interface, but are detected by a storage director. Examples are a not correctly programmed channel routine, a malfunction in the channel causing a not valid tag sequence, or a parity check.

Format 2 – Storage Director Equipment Checks

Format 2 is all check 2 errors and is generated after the microcode detects a storage director error condition. The storage director sets and sends a unit check signal to the channel at the end of the operation.

Format 3 – Storage Director Control Checks

Format 3 is all check 1 errors. These errors prevent error reporting to the connected channel because of a not operating channel interface or a control error that destroys the integrity of the microcode. Format 3 is divided into two parts: storage director clock stopped check 1 and storage director channel check 1.

Storage Director Clock Stopped Check 1

With a storage director clock stopped check 1, the microcode does not run. When a check is detected that affects the integrity of the microcode, the clock is stopped to stop instruction execution. For more details on a clock stopped check 1 operation, see Sense 110–120.

Storage Director Channel Check 1

The second part of Format 3 checks consists of errors that do not affect the integrity of the microcode, but inhibit communication to the connected channel. The microcode in the failing storage director passes the sense information to the alternate storage director. The alternate storage director reports the information to the first channel that generates a Start I/O command. The resulting selective reset is kept until the sense information is reported. For more details on a channel check 1 operation, see SENSE 125–165.

Format 6 – Usage, Overrun, and Error Statistics

Format 6 is different from format 0, 2, and 3 and does not result directly from a fault or check condition. Format 6 sense information is generated after the channel issues a Read and Reset Buffered Log Command. The channel requests format 6 information to prepare a report on device and channel usage, or to flag an unusually high number of overruns or intermittent failures. A storage director can request the channel to read the log, because a counter is full.

Format F – Subsystem Storage Errors

Format F is divided into small formats (subformats) based on the message in byte 7. Sense byte 7 equals X'Fx'; where x equals the message number as follows:

- 0 = Operation Terminated (Model 23 only)
- 1 = Subsystem Processing Error
- 2 = Subsystem storage equipment check
- 3 = Availability threshold crossed
- 4 = Subsystem storage unusable
- 5 = Subsystem storage initialization required (Model 21 only)
- 6 = Not used
- 7 = Track format not supported for paging (Model 21 only)
- 8 = Storage director communication failure.
- 9 = Caching Reinitiated
- A-F = Not used

Sense Bytes 0-7 Summary

The table on this page gives a summary of bytes 0 through 7 of the sense information. More detailed information on each byte is given in the following pages of this SENSE section.

	SENSE BYTES SUMMARY							
BYTE	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
0	Command Reject	Intervention Required	Channel Bus Out Parity Check	Equipment Check	Data Check	Overrun	Not Used	Not Used
1	Permanent Error (see device lib.)	Invalid Track Format	End of Cylinder	Message to Operator	No Record Found	File Protected	Write Inhibited	Operation Incomplete (not used in Model 23)
2	Not Used	Correctable	Alternate Controller Selected in Model 21 First Error Log in Model 23	Environmental Data Present	Intent Violation (Model 23 only)	Imprecise Ending (Model 23 only)	Write Operation	3880 Model 21 or 23 sense data
3	Restart command in Model 21; Controller Identification/Residual Record Count in Model 23							
4	Device Identification (See SENSE 30 for more information)							
5	Instruction Address Register, High Order Byte; or Diskette Checks; or Cylinder Address, Low Order Byte (See SENSE 30 for more information)							
6	Head Address and Cylinder Address, High Order Byte; or Instruction Address Register, Low Order Byte; or Storage Director Identification; or Subsystem Storage Identifier (See SENSE 32 for more information)							
7	Bits 0 - 3 = Format Identifier (See SENSE 35 for more information)				Bits 4 - 7 = Message Identifier (See SENSE 35 for more information)			

Sense Bytes 0–23

Sense bytes 0 through 6 do not change their contents because of the format and message identified by byte 7. Byte 7 identifies the format and message of the sense information. Bytes 8 through 23 are variable and depend on the format and message identified in byte 7. Bytes 8 through 23 are described under each format description.

Sense Bytes 0—2

Sense bytes 0 through 2 are generated when a unit check occurs. Bytes 0 through 2 describe the error condition in general terms and identify the specific action to recover from the error.

Sense Byte 0

Bit 0 – Command Reject

Bit 0 indicates a command has been rejected. Sense byte 7 identifies the error condition in more specific terms. Any one of the following conditions causes bit 0 to be set:

- A not valid command is received from the channel when the command code is either:
  - not known
  - acceptable only for some devices
  - not acceptable when some features are installed.
- A command that is not valid in paging mode is received on a paging address (Model 21 only).
- A command that is not valid in direct mode is received on a base address (Model 21 only).
- A not valid sequence of commands is detected.
- A not valid or not complete argument has been transferred for a control command.
- A write command has been received that violates the file mask.
- A track accessed by a command has a not correct alternate or defective track pointer. The R0 count area of a defective track points to itself instead of an alternate track.
- A write command is received on a direct address and the Write Inhibit switch is in the read only position. Write inhibited (byte 1, bit 6) is also on (Model 21 only).
- A format write command other than Write Home Address or Write Record Zero is received while accessing a defective track.
- In the domain of a Locate Record command, a command code is decoded that conflicts with the Locate Record parameters (Model 23 only).
- A diagnostic command has been received that violates the file mask (Model 23 only).
- Not valid or not complete home address data has been transferred by a Write Home Address or Diagnostic Home Address command (Model 23 only).

Bit 1 – Intervention Required

Bit 1 indicates that the addressed device is:

- Not physically attached to the system
- Not ready
- For Model 21 only - not available because a subsystem storage to DASD transfer cannot complete because the device is not installed or is not ready. Environmental data present (byte 2, bit 3) is also on.

Bit 2 – Channel Bus Out Parity Check

Bit 2 indicates that a data parity error has been detected in data transferred from the channel. A parity error detected during command transfer is a bus out parity check and not a command reject.

Bit 3 – Equipment Check

Bit 3 indicates that an unusual hardware condition originated in the channel, either storage director, the subsystem storage, the subsystem communication link, or the device.

> **Note:** The subsystem communication link is used in the Model 21 only. The Model 23 storage directors communicate through an area in the dynamic path selection feature in the shared DASD controllers.

The conditions of bit 3 are described in sense bytes 7 through 23.

Bit 4 – Data Check

Bit 4 is set on when the storage director detects a data error in the information received from the device. If correctable (byte 2, bit 1) is also set, the data error is correctable and bytes 15 through 22 in Model 21 or bytes 20 through 23 in Model 23 give the correction information. If the data error is uncorrectable, sense byte 7 defines the specific condition.

Bit 5 – Overrun

A service overrun condition occurs when a response to a request for data was not received by the storage director in the permitted time.

The following conditions cause this bit to be set:

- The storage director receives a data byte from the device or subsystem storage before the previous byte is accepted by the channel.
- During a write operation, a data byte is received too late from the channel.

The storage director posts an overrun error only if it occurs:

- More than 10 times for a single command
- During a format write operation
- During execution of a Read Multiple CKD command.

The detection of an overrun stops data transmission. When writing, the remaining part of the record is padded with '0's. Except in the three conditions given above, the storage director attempts to recover the data overruns by trying the channel command again. If the attempt is not successful, ending status includes unit check (overrun).

Permanent error (byte 1, bit 0) is never presented with overrun (byte 0, bit 5).

Command overrun errors are also detected. They are tried again by the storage director.

Bits 6 and 7

Bits 6 and 7 are not used.

Sense Byte 1

Bit 0 – Permanent Error

The storage director sets this bit on, in combination with one or more additional sense bits, to indicate that internal error recovery has been attempted and failed or that it is not desired.

If environmental data present (byte 2, bit 3) is also on, the sense data is associated with an internal operation (such as a subsystem storage to DASD transfer) rather than with the current command chain. The system should try the operation again that received the unit check.

If environmental data present (byte 2, bit 3) is off, system error recovery procedures should not be attempted.

Bit 1 – Invalid Track Format

Bit 1 is set when:

- During a format write operation, an attempt is made to write data for more than the track will hold
- An index point is detected in the gap that precedes a key or data field.

The Invalid Track Format bit is set when a previous operation attempted to write data for more than the track will hold; this operation results in a record written into index. This record was met while attempting to execute a read, search, or write command. As long as this record remains on the track, invalid track format can be posted while attempting to locate a record successfully written on the track. However, search ID-type commands will execute on any count field successfully written on the track without posting invalid track format.

In the Model 21 only, the storage director sets this bit in paging mode when data is transferred between cache and DASD and the data format is not supported in paging mode. The following formats are not valid:

- Key length other than zero
- Data length other than 4096
- Record is a part of an overflow record
- The track has been formatted without a Home Address
- The Record 0 count field of a defective track points to itself instead of the alternate track.

  If the failed operation is a paging mode read miss, only this bit is set. If the failed operation is a subsystem storage to DASD write, message to operator (byte 1, bit 3) and environmental data present (byte 2, bit 3) are also on.

Bit 2 – End of Cylinder

This bit is set when:

- An attempt is made to continue a multitrack operation across a cylinder boundary.
- Model 21 only - An attempt is made to continue a read or write operation for an overflow record across a cylinder boundary.

Bit 3 – Message to Operator

Bit 3 indicates that a message, defined by byte 7, is to be sent to the operator console.

For Model 21, the operator console messages are as follows:

Byte 7 Console Message

3x ddd REPORTS DISABLED INTERFACE ON (nn) - FAULT CODE = **cccc**

F1 SUBSYSTEM PROCESSING ERROR - FAULT CODE = **cccc - cuu**

F2 SUBSYSTEM STORAGE EQUIPMENT CHECK - FAULT CODE = **cccc -cuu**

F3 SUBSYSTEM STORAGE AVAILABILITY THRESHOLD CROSSED - **cuu**

F4 SUBSYSTEM STORAGE UNUSABLE - FAULT CODE = **cccc - cuu**

F5 SUBSYSTEM STORAGE MUST BE INITIALIZED - FAULT CODE = **cccc - cuu**

F7 TRACK FORMAT NOT SUPPORTED FOR PAGING - DEVICE **ddd - cuu**

F8 STORAGE DIRECTOR COMMUNICATION FAILED - FAULT CODE = **cccc - cuu**

For Model 23, the operator console messages are as follows:

Byte 7 Console Message

3x ddd REPORTS DISABLED INTERFACE (nn) - FAULT CODE = cccc

F1 SUBSYSTEM PROCESSING ERROR - FAULT CODE = cccc - ss-XX-XX

F2 SUBSYSTEM STORAGE EQUIPMENT CHECK - FAULT CODE = cccc - ss-XX-XX

F3 SUBSYSTEM STORAGE AVAILABILITY THRESHOLD CROSSED - ss-XX-XX

F4 SUBSYSTEM STORAGE IS UNUSABLE - FAULT CODE = cccc - ss-XX-XX

F8 STORAGE DIRECTOR COMMUNICATION FAILED - FAULT CODE = cccc - ss-XX-XX

F9 CACHING REINITIALIZED - ss-XX-XX

```
LEGEND:

cccc = Fault symptom code from sense
       bytes 22 and 23
cuu  = Address of the reporting path
ddd  = Device address
nn   = Installation number
cc   = Physical identifier of the
       controller
dd   = Physical identifier of the
       device
ss   = Physical identifier of the
       reporting storage director
```

Sense Byte 1 (Continued)

Bit 4 – No Record Found

In the Model 21, the following conditions cause this bit to be set:

- During execution of a direct mode channel program, two index marks have been detected in the same CCW chain without an intermediate read operation in a home address or data area, or without an intermediate control, write, or sense command. The storage director always verifies that the accessor is placed correctly before reporting this condition.
- While executing a Read Data command in paging mode, the storage director can not locate a record whose logical block identifier was communicated by the preceding Search ID Equal command.
- While attempting to perform an asynchronous operation that required transferring data from the subsystem storage to the 3350, the storage director can not locate a record whose logical block identifier is taken from the subsystem storage directory. Message to operator (byte 1, bit 3) and environmental data present (byte 2, bit 3) are also on.

In the Model 23, this bit is set by the storage director when index has been detected twice (or its cache equal) in the same CCW chain without an intermediate read operation on a data field or home address, or without an intermediate control, write, or sense command. For operations direct to the device, the storage director verifies that the access mechanism is placed correctly before reporting this condition.

Bit 5 – File Protected

Bit 5 indicates one of the following conditions:

- A seek command has violated the file mask.
- A read multitrack or search multitrack operation has violated the file mask.
- In the Model 21, a read or write operation that accesses an overflow record violates the file mask. Operation incomplete (byte 1, bit 7) is also on.
- In the Model 23, a Locate Record operation attempts to go over the boundaries of the Define Extent command.

Bit 6 – Write Inhibited

In the Model 21 only, this bit is on when:

- A write command is received on a base address and the device write inhibit switch is in the read only position. Command reject (byte 0, bit 0) is also on.
- A subsystem storage to DASD write is attempted and the device write inhibit switch is in the read only position. Environmental data present (byte 2, bit 3) is also on.

In the Model 23 only, this bit is turned on when a write command or a Locate Record command specifying a write-type operation is received on a channel that is 'write inhibited' by a Diagnostic Control command. Equipment Check (byte 0, bit 3) is also on.

Bit 7 – Operation Incomplete

This bit is used by the Model 21 only.

This bit is on when:

- Accessing of a segment other than the first requires a switch to a track that is protected by the file mask. File protected (byte 1, bit 5) is also on.
- Accessing of a segment other than the first requires a switch beyond the end of the cylinder. End of cylinder (byte 1, bit 2) is also on.
- A correctable data check is met in a segment other than the last. Data check (byte 0, bit 4) and correctable (byte 2, bit 1) are also on.
- An uncorrectable data check is met in a segment other than the first. Data check (byte 0, bit 4) is also on.
- Accessing of a segment other than the first segment requires a switch to a track that is defective or from an assigned alternate track.
- A seek error is detected while attempting to access a segment other than the first segment.

Sense Byte 2

Bit 0

Bit 0 is not used.

Bit 1 – Correctable

This bit is on when the data error indicated by data check (byte 0, bit 4) is correctable. Bytes 18-22 of format 5 give information to permit correction.

In the Model 21, the following conditions cause this bit to be set:

- A correctable data error is detected in information received from the device during a direct mode read or search operation. Correctable (byte 2, bit 1) is also on, and bytes 15-22 of format 5 give information to permit correction.
- A correctable data check is met in a segment other than the last. Data check (byte 0, bit 4) and operation incomplete (byte 1, bit 7) are also on.

In the Model 23, the following condition causes this bit to be set:

- PCI fetch mode is active when a data error is detected in data transferred to the channel from the device and the data is transmitted correctly on channel command retry. Data check (byte 0 , bit 4) is also on and the ECC displacement and pattern are zero.

Bit 2 – Alternate Controller Selected or First Error Log

This bit in the Model 21 is named Alternate Controller Selected. This bit in the Model 23 is named First Error Log.

In the Model 21, this bit indicates that the controller in the 3350 C2 unit is selected. This bit gives aid in fault isolation between controllers when the dual control option is installed.

In the Model 23, this bit indicates that the 3380 or subsystem storage entered soft error logging mode. Environmental data present (byte 2, bit 3) is also on.

Bit 3 – Environmental Data Present

Bit 3 indicates that sense bytes 8 through 23 give either usage and error statistics or error log information. Byte 7 indicates the formats for bytes 8 through 23.

Bit 3 is set by any of the following:

- A usage counter or error counter overflow.
- An internal error recovery procedure has either failed or completed correctly and the forced error logging mode or soft error logging mode is in effect.
- An error has occurred during a subsystem storage to DASD transfer.
- During a subsystem storage to DASD write, the record or track being updated is found to be a format that is not valid for paging mode (Model 21 only).
- A subsystem storage to DASD write is attempted and the write inhibit switch is in the read-only position.
- The amount of space available for subsystem storage is below one of the reporting thresholds.
- A subsystem processing error is detected that is not associated with the current command chain.
- An attempted communication with the other storage director fails or is not permitted because of the subsystem storage mode switch setting and the attempted communication is not associated with the current command chain.

Bit 4 – Intent Violation

This bit is used by the Model 23 only.

This bit indicates that an update write operation in the domain of a Locate Record command has met a conflict between the Define Extent or Locate Record command parameters and the recorded track format. This condition is reported in the following instances.

- A Write Data command is chained from a Locate Record command with the Write Data subcommand specified and the block size value from the preceding Define Extent command or the Transfer Length Factor value from the Locate Record command, (if specified), is not equal to the actual data length of the record to be updated.
- A Write Update Data command is received in the domain of a Locate Record command with the Write Data subcommand specified and the block size value from the preceding Define Extent command or the Transfer Length Factor value from the Locate Record command, (if specified), is not equal to the actual data length of the record to be updated.
- A Write Key and Data command is chained from a Locate Record command and the block size value from the preceding Define Extent command or the Transfer Length Factor value from the Locate Record command, (if specified), is not equal to the total of the key and data lengths of the record to be updated.
- A Write Update Key and Data command is received in the domain of a Locate Record command and the block size value from the preceding Define Extent command or the Transfer Length Factor value from the Locate Record command, (if specified), is not equal to the total of the key and data lengths of the record to be updated.
- A Write Update Data or Write Update Key and Data command has been received and after orienting to index following a head switch, the expected number of records (Home Address, a record to pass over and a record for update) are not identified on the track.
- A Write Update Data or Write Update Key and Data command has been received and after orienting to index following a head switch, the expected record following home address (record 0) is not identified on the track.
- The R0 data field length is not equal to 8 during a Write Track operation.
- Home Address or Record 0 is not found following a head-switch during a Write Count, Key, and Data Next Track command execution.

Imprecise Ending (Byte 2, Bit 5)

This bit is used by the Model 23 only.

This bit is set to one when an abnormal channel program termination occurs and the exception status is for a preceding completed CCW (i.e., the search function of a Locate Record command). This bit indicates that the CSW command address is not synchronized with the transfer of data by the Model 23 to the device.

Bit 6 – Write Operation

Bit 6 is set to indicate that the error occurred during the execution of a write command.

Bit 7 – 3880 Model 21 or 23 Storage Control Unit

When this bit is on, it indicates that the sense record was made by the 3880 Model 21 or 23.

Sense Bytes 3—5

Sense Byte 3 – Restart Command or Controller Identification/Residual Record Count

In Model 21 this byte is named the restart command. In Model 23 this byte is named the controller identification/residual record count byte.

Model 21:

In Model 21, this byte is set when operation incomplete (byte 1, bit 7) is on. Bits 5-7 identify the type of operation in progress when the unit check occurred. If the bits are set to 0000 0110, a read operation was in progress; if they are set 0000 0101, a write operation was in progress.

Model 23:

In Model 23 for sense formats 1, 2, 6, 7, and 8 this byte identifies the controller for which the sense data is reported. For sense formats 0, 3, 4, 5 and F:

- With Imprecise ending (byte 2, bit 5) set OFF, this byte is zero.
- With Imprecise ending set ON, this byte indicates the number of records that remain to be processed in the domain of the Locate Record command.

Sense Byte 4 – Device Identification

Bits 0 through 7 identify the device associated with the sense information.

Model 21:

When the sense data is presented on a direct address or when sense formats 1, 2, 4, 5, or message 7 of format F are presented on a paging address, the byte description is as follows:

Bit 0 = Device 0
Bit 1 = Device 1
Bit 2 = Device 2
Bit 3 = Device 3
Bit 4 = Not used
Bit 5 = Not used
Bit 6 = Not used
Bit 7 = Not used

When sense formats 0, 3, and messages 0 through 5 and 8 of format F are presented on a paging address, this byte contains all zeros.

Model 23:

When the sense data has been collected as a result of errors detected in the subsystem storage, this byte identifies the device addressed by the command chain.

When this bit is on it is defined as follows:

- Bit 0 - DPS feature installed
- Bit 1 - Reserved, always zero
- Bit 2 - Reserved, always zero except in format 7 where this bit indicates a permanent path error.
- Bit 3 - Reserved, always zero
- Bit 4 - Spindle address 4
- Bit 5 - Spindle address 2
- Bit 6 - Spindle address 1
- Bit 7 - If 0, left actuator; if 1, right actuator

Sense Byte 5 for Model 21

This byte contains different types of information depending on the format being reported in sense byte 7. The following formats are possible:

- When format 3 is identified and not with message 8, the error reported by sense byte 5 reports an Instruction Address Register–High Order Byte error.
- When format 6 is identified, sense byte 5 reports a Diskette Check error.
- When formats 0, 1, 2, 4, 5, or F is identified or has the value X'38', sense byte 5 reports a Cylinder Address–Low Order Byte error.

A description of each of the conditions of sense byte 5 follows.

- Instruction Address Register - High Order Byte

  If sense byte 7 indicates format 3 and not message 8, this byte contains the High-Order Byte of the instruction address register at the time of the error.

- Diskette checks

  If sense byte 7 indicates format 6, this byte contains the number of recoverable diskette checks after an initial microcode load (IML), or whether or not a storage director-to-storage director communication failure occurred during the most recent IML as follows:

  Bit 0 – Communication failure during an IML
  Bit 1 – Not used
  Bits 2-4 – Number of diskette seek errors
  Bits 5-7 – Number of diskette read errors

- Cylinder Address - Low Order Byte

  If sense byte 7 indicates formats 0, 1, 2, 4, 5, F or has the value X'38' this byte contains the most recent seek argument from the channel as follows:

  Bit 0 = Cylinder 128
  Bit 1 = Cylinder 64
  Bit 2 = Cylinder 32
  Bit 3 = Cylinder 16
  Bit 4 = Cylinder 8
  Bit 5 = Cylinder 4
  Bit 6 = Cylinder 2
  Bit 7 = Cylinder 1

Sense Byte 5 for Model 23

This byte contains different types of information depending on the format being reported in sense byte 7. The following formats are possible:

- When format 3 is identified and not with message 8, the error reported by sense byte 5 reports an Instruction Address Register–High Order Byte error.
- When format 6 is identified, sense byte 5 reports a Diskette Check error.
- When formats 0, 1, 2, 4, 5, 7, 8, or F is identified or has the value X'38', sense byte 5 reports a Cylinder Address Low Order Byte error.

A description of each of the conditions of sense byte 5 follows.

- Instruction Address Register - High Order Byte

  If sense byte 7 indicates format 3 and not message 8, this byte contains the High-Order Byte of the instruction address register at the time of the error.

- Diskette checks

  If sense byte 7 indicates format 6, this byte contains the number of recoverable diskette checks after an initial microcode load (IML), or whether or not a storage director-to-storage director communication failure occurred during the most recent IML as follows:

  Bit 0 – Communication failure during an IML
  Bit 1 – Not used
  Bits 2-4 – Number of diskette seek errors
  Bits 5-7 – Number of diskette read errors

- Cylinder Address - Low Order Byte

  If sense byte 7 indicates formats 0, 1, 2, 4, 5, 7, 8, or F, or has the value X'38' this byte contains the most recent seek argument from the channel as follows:

  Bit 0 = Cylinder 128
  Bit 1 = Cylinder 64
  Bit 2 = Cylinder 32
  Bit 3 = Cylinder 16
  Bit 4 = Cylinder 8
  Bit 5 = Cylinder 4
  Bit 6 = Cylinder 2
  Bit 7 = Cylinder 1

Sense Byte 6

Sense Byte 6 for Model 21

This byte contains different types of information depending on the format being reported in sense byte 7. The following formats are possible:

- When formats 0, 1, 2, 4, 5, or F is identified or has the value X'38', sense byte 6 reports a Head Address and Cylinder Address–High Order Byte error.
- When format 3 is identified and not with message 8, sense byte 6 reports an Instruction Address Register–Low Order Byte error.
- When format 6 is identified, sense byte 6 reports the Storage Director Identification.
- When format F is identified with messages 3 or 4, sense byte 6 reports the Subsystem Storage Identifier.

A description of each of the conditions of byte 6 follows.

- Head Address and Cylinder Address - High Order Byte

  If sense byte 7 indicates format 0, 1, 2, 4, 5, F or is equal to X'38', this byte gives the High-Order Cylinder address of the most recent seek argument received from the channel and the head address resulting from the most recent head switch (seek or multitrack operation).

  If an alternate track condition is detected while processing an overflow record and operation incomplete (byte 1, bit 7) is on, the head address is that of the defective track +1. The ERPs use this byte to make the seek argument to continue the operation.

  In direct mode, the head address and High-Order Cylinder address values of rejected seek commands are not given in this byte. In paging mode, they are given.

  Operations that include head switching update the head address bits (bits 3-7) of this byte.

  This byte is formatted as follows:

  Bit 0 = CE cylinder
  Bit 1 = Cylinder 512
  Bit 2 = Cylinder 256
  Bits 3 to 7 = Head address

- Instruction Address Register - Low Order Byte

  If sense byte 7 identifies format 3 and not with message 8, this byte is used to indicate the low order byte of the instruction address register at the time the error occurred.

- Storage Director Identification

  If sense byte 7 identifies the data as format 6, this byte contains the storage director identification.

- Subsystem Storage Identifier

  If sense byte 7 identifies Format F and messages 3 or 4, this byte contains the subsystem storage identifier.

Sense Byte 6 for Model 23

This byte contains different types of information depending on the format being reported in sense byte 7. The following formats are possible:

- When formats 0, 1, 2, 4, 5, 7, 8, or F is identified or has the value X'38', sense byte 6 reports a Head Address and Cylinder Address–High Order Byte error.
- When format 3 is identified and not with message 8, sense byte 6 reports an Instruction Address Register–Low Order Byte error.
- When format 6 is identified, sense byte 6 reports the Storage Director Identification.

A description of each of the conditions of byte 6 follows.

- Head Address and Cylinder Address - High Order Byte

  If sense byte 7 indicates format 0, 1, 2, 4, 5, 7, 8, or F, or is equal to X'38', this byte gives the High-Order Cylinder address of the most recent seek argument received from the channel and the head address resulting from the most recent head switch (seek or multitrack operation).

  If an alternate track condition is detected while processing an overflow record and operation incomplete (byte 1, bit 7) is on, the head address is that of the defective track +1. The ERPs use this byte to make the seek argument to continue the operation.

  Operations that include head switching update the head address bits (bits 4-7) of this byte.

  This byte is formatted as follows:

  Bit 0 = Not used
  Bit 1 = Equal to bit 5 of the High-Order Cylinder Byte
  Bit 2 = Equal to bit 6 of the High-Order Cylinder Byte
  Bit 3 = Equal to bit 7 of the High-Order Cylinder Byte
  Bits 4 to 7 = Head address

- Instruction Address Register - Low Order Byte

  If sense byte 7 identifies format 3 and not with message 8, this byte is used to indicate the low order byte of the instruction address register at the time the error occurred.

- Storage Director Identification

  If sense byte 7 identifies the data as format 6, this byte contains the storage director identification.

Sense Byte 6 SENSE 32

Sense Byte 7

This sense byte consists of two fields, the format identifier in bits 0 through 3 and the message identifier in bits 4 through 7.

Sense Byte 7:							
0	1	2	3	4	5	6	7
Format Identifier				Message Identifier			

Format Identifier

For formats 0 to 6 (except format 3), these bits identify the specific format of sense bytes 5-6 and 8-23. For formats 3 and F, these bits plus the message identifier identify the specific format of sense bytes 5-6 and 8-23. The possible values are defined in the sections that describe the corresponding formats of bytes 8-23.

Formats 0, 2, and 3 pertain to storage control errors. Format 0 is generated when an error or unusual condition is specified by sense bytes 0 through 7. Format 2 is generated after the microcode detects a storage director error condition. Format 3 is generated after an error condition occurs in the channel interface or the control and results in a disconnect-in sequence to the channel.

Formats 1, 4, and 5 pertain to device errors and are described in the device maintenance library.

Format 6 contains usage, overrun and error statistics information that is described in both this Maintenance Support Manual (MSM) and the device MIM.

Message Identifier

These bits give a message that describes the error.

CODE	MEANING
0000	Format 0 - Program or system checks
0001	Format 1 - Device equipment checks
0010	Format 2 - Storage director equipment checks
0011	Format 3 - Storage director control checks
0100	Format 4 - Uncorrectable data checks
0101	Format 5 - Correctable data checks
0110	Format 6 - Usage, overrun, and error statistics
0111	Format 7 - Controller check 1
1000	Format 8 - Controller check 2 and device check 1
1111	Format F - Subsystem storage errors

Note: Format 5 can also be presented on device errors which are not ECC correctable but which need restart displacement information.

Byte 1, Bit 3 – Message to Operator

Byte 1, bit 3 indicates that a message, defined by byte 7, is to be sent to the operator console.

For Model 21, the operator console messages are as follows:

Byte 7 Console Message

3x ddd REPORTS DISABLED INTERFACE ON (nn) - FAULT CODE = **cccc**

F1 SUBSYSTEM PROCESSING ERROR - FAULT CODE = **cccc - cuu**

F2 SUBSYSTEM STORAGE EQUIPMENT CHECK - FAULT CODE = **cccc -cuu**

F3 SUBSYSTEM STORAGE AVAILABILITY THRESHOLD CROSSED - **cuu**

F4 SUBSYSTEM STORAGE UNUSABLE - FAULT CODE = **cccc - cuu**

F5 SUBSYSTEM STORAGE MUST BE INITIALIZED - FAULT CODE = **cccc - cuu**

F7 TRACK FORMAT NOT SUPPORTED FOR PAGING - DEVICE **ddd - cuu**

F8 STORAGE DIRECTOR COMMUNICATION FAILED - FAULT CODE = **cccc - cuu**

For Model 23, the operator console messages are as follows:

Byte 7 Console Message

3x ddd REPORTS DISABLED INTERFACE (nn) - FAULT CODE = cccc

F1 SUBSYSTEM PROCESSING ERROR - FAULT CODE = cccc - ss-XX-XX

F2 SUBSYSTEM STORAGE EQUIPMENT CHECK - FAULT CODE = cccc - ss-XX-XX

F3 SUBSYSTEM STORAGE AVAILABILITY THRESHOLD CROSSED - ss-XX-XX

F4 SUBSYSTEM STORAGE IS UNUSABLE - FAULT CODE = cccc - ss-XX-XX

F8 STORAGE DIRECTOR COMMUNICATION FAILED - FAULT CODE = cccc - ss-XX-XX

F9 CACHING REINITIALIZED - ss-XX-XX

```
LEGEND:

cccc = Fault symptom code from sense
       bytes 22 and 23
cuu  = Address of the reporting path
ddd  = Device address
nn   = Installation number
cc   = Physical identifier of the
       controller
dd   = Physical identifier of the
       device
ss   = Physical identifier of the
       reporting storage director
```

Sense Bytes 8 through 23

The content of sense bytes 8 through 23 changes depending on the value specified in byte 7. See the following descriptions of sense formats for more information.

Format 0—Program or System Checks for Model 21

Format 0 is used when sense bytes 0 through 7 completely describe the error or unusual condition caused by a program or system error.

Bytes 8 to 23 contain the following data:

Bytes 8 through 17 are not used and are set to zero.

Byte 18 through 23 – Skip Displacement

If a Sense command is chained from a correct Read Home Address command and no contingent allegiance exists, bytes 18 through 23 contain the skip displacement bytes on the track.

If a Sense command is not chained from a Read Home Address and a contingent allegiance exists, bytes 8 to 20 contain zeros, byte 21 contains the storage director identification, and bytes 22 and 23 contain the symptom code.

If not, bytes 18 through 23 are set to zero.

Messages for format 0 are described below.

Format 0 Messages

Message 0 – No Message

No additional information required.

Message 1 – Invalid Command

A not valid command was sent to the device that is not in the device command set or the command pertains to a feature that is not installed.

Message 2 – Invalid Command Sequence

A not valid sequence of commands has occurred. Included are the following:

- A read, search, Seek Head, Space Count, or Diagnostic Write Home Address command is received without being preceded by a Seek, Seek Cylinder, Locate Record, Read IPL, or Recalibrate command in the same chain.
- A Read Initial Program Load (IPL), Device Reserve, or Device Release, Set File Mask or Define Extent command was preceded by a Set File Mask or Define Extent command in the same chain.
- A write command has violated the write part of a preceding Set File Mask command.
- A write command has not satisfied the prerequisites.
- A Write, Read IPL, Set File Mask, Define Extent, Device Reserve, or Device Release command was sent in the same chain following a Space Count command.
- An Unconditional Reserve command is preceded by a channel command word (CCW) in the same chain.
- A Space Count command is chained from a formatting write command.
- A write command is received while the SA cylinder is accessed.
- A Locate Record command which specifies a subcommand of Write Data is received and the file mask inhibits all write operations.
- A Locate Record command which specifies a subcommand of Format Write or Write Track is received and the file mask inhibits all write or format write operations.
- A Locate Record command is received without being preceded by a Define Extent command or a Read IPL command in the same command chain.
- Any control, search, or sense command is received in the domain of a Locate Record command.
- Any of the following commands is received in the domain of a Locate Record command: Read Multiple Count, Key, and Data, Read Sector, Diagnostic Read Home Address, and Diagnostic Write Home Address.
- Any of the following commands is received in the domain of a Locate Record command which has a subcommand other than Read Data: Read Home Address, Read Record Zero, Read Count, Read Data, Read Key and Data, or Read Count, Key and Data.
- A Set Path Group Identifier, Sense Path Group Identifier, Set Subsystem Mode, or Sense Subsystem Status command is chained from any command or any command command is chained from one of these commands.

Message 3 – CCW Count Less Than Required

The CCW count of a command is less than required. Included are the following:

- Any seek command with a CCW count of less than six
- A Set Paging Parameters command with a count less than ten
- A Discard Block command with a count of from two to 322
- A Set Subsystem Mode command with a count less than two
- A Search ID Equal command (paging mode only) with a count less than five
- A Write Home Address command with a CCW count of less than seven.

Message 4 – Invalid Argument

The data argument is invalid. Included are the following:

- A Seek, Seek Cylinder, or Seek Head command that seeks a not valid address
- A Set Sector command argument that seeks a not valid sector number
- A Set File Mask command argument that does not have bits 2 and 6 set to zero.

Message 5 – Diagnostic Write Command Not Permitted By File Mask

A Diagnostic Write command is sent that violates bit 5 of the file mask.

Message 6 – Channel Discontinued Retry Operation

The channel does not indicate chaining when retry status is activated. See the MD section of the Maintenance Support Manual (MSM) for the maintenance device (MD), option 5, to perform a check out procedure.

Message 7 – Channel Returned With Incorrect Retry CCW

This message is generated when the command returned after a command retry sequence does not match the command for which the channel command retry status was presented.

Message 8 – IML Device Not Ready

During a Diagnostic Load command, message 8 is activated if the initial microcode load (IML) device is not ready.

Message 9 – IML Device Permanent Seek Check

During a Diagnostic Load command, message 9 is activated if the operation cannot be completed because of an IML device permanent seek check.

Message A – IML Device Permanent Read Check

During a Diagnostic Load command, message A is activated if the operation cannot be completed because of an IML device permanent read check.

Message B – Defective Or Alternate Track Pointer Points to Itself

An alternate track pointer in the record 0 (R0) count field of a defective track equals the track address of the defective track.

Message C – Unconditional Reserve

The microcode was unable to get access to the string switch with the use of of the Unconditional Reserve command.

Message C Through Message F

Message C through message F are not used.

Format 0—Program or System Checks for Model 23

Format 0 is used when sense bytes 0 through 7 completely describe the error or unusual condition caused by a program or system error.

Bytes 8 to 23 contain the following data:

Bytes 8 through 19 are not used and are set to zero.

Byte 20 – Controller Physical Identifier

If Message to operator (byte 1, bit 3) and Environmental data present (byte 2, bit 3) are on, byte 20 contains the controller physical identifier. Otherwise, it is zero.

Byte 21 – Storage Director Identification

Bytes 22 and 23 contain the fault symptom code.

Messages for format 0 are described below.

Format 0 Messages

When Message to Operator (byte 1, bit 3) is off; the messages for Format 0 are as follows:

Note: When Message to Operator (byte 1, bit 3) is off, use Format 0 messages described on this page. If Message to Operator is on, use Format 0 messages described on SENSE 52.

Message 0 – No Message

No additional information required.

Message 1 – Invalid Command

This message indicates the device received a command that is not in the device command set. A not valid command can also pertain to a feature that is not installed.

Message 2 – Invalid Command Sequence

This message indicates an invalid sequence of commands has occurred. Included are the following:

- A Read, Search, Seek Head, Space Count, or Diagnostic Write Home Address command is received without being preceded by a Seek or a Seek Cylinder, Locate Record, Read IPL, or Recalibrate command in the same command chain.
- A Read Initial Program Load (IPL), Device Reserve, Device Release, Set File Mask, or Define Extent command is preceded by a Set File Mask or Define Extent command in the same command chain.
- A Write command has not satisfied the prerequisites of the file mask.
- A Write command is not chained from a stated prerequisite command.
- A write command is received while the surface analysis cylinder is accessed.
- A Write, Read IPL, Set File Mask, Define Extent, Device Reserve, or Device Release command is received in the same chain following a Space Count command.
- A Space Count command is chained from a formatting Write command.
- An Unconditional Reserve command is received as other than the first command in a chain.
- A Locate Record command which specifies a subcommand of Write Data, Format Write, or Write Track is received and the file mask inhibits all write operations.
- A Locate Record command is received without being preceded by a Define Extent or Read IPL command in the same command chain.
- A command received in the domain of a Locate Record command is not correct for the domain.
- A Set Path Group Identifier, Sense Path Identifier, Set Subsystem Mode, or Sense Subsystem Status command is chained from any command or any command is chained from one of these commands.

MESSAGE 3 – CCW COUNT LESS THAN REQUIRED

The CCW count of a command is less than required. The following commands are subject to this condition:

- Any seek command with a CCW count of less than 6.
- A Space Count command with a CCW count of less than 3.
- A Set Path Group Identifier command with a CCW count of less than 12.
- A Define Extent command with a CCW count of less than 16.
- A Locate Record command with a CCW count of less than 16.
- A Diagnostic Control command with a CCW count of less than 4.
- A Write Home Address command with a CCW count of less than 5.
- A Diagnostic Write Home Address command with a CCW count of less than 28.
- A Set Subsystem Mode command with a CCW count of less than 2.

Message 4 – Invalid Data Argument

The data argument is not valid. Included are these general conditions:

- A Seek command argument that is not a valid seek address
- A Set Sector command argument that is not valid
- A Set File Mask command argument that does not have bits 2 and 6 set to zero
- A Write HA or Diagnostic Write HA fails specified parameter checking
- A Set Path Group ID argument is not valid.
- A Diagnostic Control command is received with one of the following:
  - Byte 0 is other than X'02' or X'08'.
  - Byte 0 is X'02' and byte 1 is other than X'80', X'40', or X'20'.
  - Byte 0 is X'08' and byte 1 is other than X'00'.
  - Bytes 2 and 3 are other than zeros

Message 5 – Diagnostic Read or Write Command Not Permitted By File Mask

A Diagnostic Control, Diagnostic Read Home Address, or Diagnostic Write Home Address command is sent that violates bit 5 of the file mask.

Message 6 – Retry Status Presented and Channel Did Not Indicate Chaining

The channel does not indicate chaining when retry status is activated. Select maintenance device (MD) option 5 in the maintenance mode and perform a machine check out.

Message 7 – Channel Returned With Incorrect Retry CCW

The channel retry commands are out of sequence. Perform a machine checkout by selecting maintenance device (MD) option 5 in the maintenance mode.

Format 0—Program or System Checks for Model 23(Continued)

Messages 8 through A

Messages 8 through A are not used.

Message B – Defective or Alternate Track Pointer Points to Itself

The alternate track pointer in record zero (R0) count field of a defective track equals the track address of the defective track or the alternate track equals the track address of the alternate track.

Message C – Dynamic Path Selection Installation Configuration Check

Message C indicates that either: (1), the cables to the controllers attached to a storage director are not correct for the dynamic path selection feature, or (2), the dynamic path selection feature is not installed or operating in one of the controllers.

Messages D through F

Messages D through F are not used.

Format 0 Messages

When Message to Operator (byte 1, bit 3) is on, the messages for Format 0 are as follows:

Note: When Message to Operator (byte 1, bit 3) is on, use Format 0 messages described on this page. If Message to Operator is off, use Format 0 messages described on SENSE 50.

Message 0 - No Message

No additional information required.

Message 1 - Soft Error Logging Complete for Device

This message is generated when soft error logging has been completed for one of the attached devices. The code, SS-CC-DD, is shown on the operator console as follows:

SS	The storage director physical ID is found in sense byte 21
CC	The controller physical ID is found in byte 20
DD	The failing device physical ID as shown in bits 4 through 7 of byte 4

Message 2 - Soft Error Logging Complete for Controller

This message is generated when soft error logging has been completed for one of the attached controllers. The code, SS-CC-DD, is shown on the operator console as follows:

SS	The storage director physical ID is found in sense byte 21
CC	The failing controller physical ID is found in byte 20
DD	The failing device physical ID, connected to the failing controller, as shown in bits 4 through 7 of byte 4

Message F - Soft Error Logging Complete for Subsystem Storage

This message is generated when soft error logging has been completed for the subsystem storage. See the EREP reports for the error which caused the storage director to go into logging mode.

Format 2—Storage Director Equipment Checks

The table below gives a summary of bytes 8 through 23 for format 2. The following pages give more detailed information on format 2.

BYTE NAME	BYTE	BITS 0	1	2	3	4	5	6	7
Transfer Complete Status (XCS)	8	Check 2	Device Buffer High (DBH) = Channel Buffer High (CBH)	Director-to-Device Controller (DDC) End-of-Transfer	Read Data Check	Channel Data Transfer (CDX) End-of-Transfer	Compare Successful	First Sync In Latch	Channel Truncation
Transfer Error Status (XES)	9	Device Overrun	Channel Overrun	Control Interface Parity Check	Clock (CLK) Check 2	Director-to-Device Controller (DDC) Card Check	Control Interface (CTL-I) Sync In Check	Channel Buffer Parity Check	Device Buffer Parity Check
Check (CHK) Register	10	Data Transfer Addressing (DXA) Card Check	Device Counter (DCT) Card Check	Channel Search (CSR) Card Check 2	Channel Data Check	Array Out Parity Check	Sense Register Check	Data Transfer Data (DXD) Card Check	ADT/ASDM Card Check
Channel Transfer Control (CXC)	11	Storage Director Service In	Search High	Search Equal	Read CBI or CBO Select Bit	Set Speed Control Register	Allow Run Channel	Data Transfer (DXR) from Channel	Run Channel
Channel Control 2 (CC2) Register	12	Force Select Out	Read Address Switch	Not Used	Not Used	Channel Switch Locked	Channel Select bit 4	Channel Select bit 2	Channel Select bit 1
Device Bus Out	13	Contents of Device Buss Out (DBO) Register							
Device Bus In	14	Contents of Device Buss In (DBI) Register							
Device Tag Out (DTO) - Model 21	15	Device Tag Out (DTO) Bit 0	Diagnostic Sync In	Maintain DTO Parity	Not Used	DTO bit 4	DTO bit 5	DTO bit 6	DTO bit 7
Device Tag Out (DTO) - Model 23	15	DCC Tag Out Bit 0	DCC Tag Out Bit 1	DCC Tag Out Bit 2	Not Used	Not Used	Not Used	Not Used	Not Used
Device Tag Gate (DTG) - Model 21	16	Select Hold	Tag Gate	Response Gate	Reset Index Latch	Inhibit First Decrement	Control Interface, Control Bit 0	Control Interface, Control Bit 1	Run Device
Device Tag Gate (DTG) - Model 23	16	One-Byte Device	Block Diagnostic Set	Diagnostic Sync In	Inhibit Bus Out Parity	Not Used	Director to Device Control (DDC) Bit 0	Director to Device Control (DDC) Bit 1	Run Device
Device Tag In (DTI) - Model 21	17	Select Active	Tag Valid	Check End	CE Alert	Normal End	Device Alert	Index Latch	Error Alert
Device Tag In (DTI) - Model 23	17	Connection Check Alert	Tag In Sequence Check	End Op Not Cmd Gate	Not Used	Null Disconnect 00	Valid Sync/In 01	Selected Null 11	End Operation 10
Channel Status 2 (CS2) Register	18	Halt I/O	Selective Reset	System Reset	Two or Four Channel Add. Condition Reg. (TACR/FACR) Card Check Card Check	Channel Sequen. Control (CSC) or Four Chan. Add. Sequence Control (FASC) Card Checks	Channel Bus Out (CBO) Parity Check	Two Channel Condition Register (TCR) Card Check	Channel Check 1
Toggle, FRU Register (TFR)	19	CBP Toggle	DBP Toggle	BAP Toggle	FRU Address Bit 1	Not Used	High Speed Channel Active	BC1 Full	BC2 Empty
Microcode Detected Checks	20	Message Number (See SENSE 100)							
Storage Director Physical ID (SDI)	21	Bits in this byte equal the settings of the storage director ID switches on the DCT card.							
Symptom Code	22-23								

Format 2—Sense Byte 8

Sense Byte 8 – Transfer Complete Status

Sense byte 8 displays the data transfer status of the device and channel.

Bit 0 – Check 2

Bit 0 is set with any of the following error conditions:

- Device overrun
- Channel overrun
- Sync-in check
- Control interface check
- Director-to-device controller card check
- Clock check 2
- Error alert (Model 21 only)
- Device counter card check
- Channel data check
- Channel search card check 2
- Channel bus out deskew register parity check
- Channel buffer check
- Device buffer check
- DXA card check
- Array out parity check
- Sense register check
- DXD card check
- Subsystem storage upper/lower check
- Subsystem storage common check
- Port connection/ADT Buffer check.
- Connection check alert—Model 23 only.
- Tag sequence check—Model 23 only.

Bit 0 is reset by the check reset signal.

Bit 1 – Device Buffer High (DBH) = Channel Buffer High (CBH)

Bit 1 indicates that the high-order eight bits (bits 0-7) of channel buffer pointer (CBP) and device buffer pointer (DBP) are the same.

Bit 2 – Director-to-Device Controller (DDC) End-of-Transfer

Bit 2 indicates the transfer of data between the storage director and the device is complete. Bit 2 is set when the device byte counter equals zero and byte 16, bit 7 (run device) is activated.

Bit 2 resets when run device is deactivated.

Bit 3 – Read Data Check

Bit 3 indicates that a correctable data check occurred during the last dynamic control storage read operation. This bit is reset before each dynamic control storage read operation and is used by the diagnostics to determine the number of single bit failures on the dynamic control storage and refresh (DCSR) card.

Bit 4 – Channel Data Transfer (CDX) End-of-Transfer

Bit 4 indicates the end of a channel data transfer. Bit 4 is turned on when the channel byte counter equals zero and after one of the following conditions occurs:

- Read mode – the channel has taken the last byte
- Write mode – the automatic data transfer has taken the last byte
- Search mode – the last byte has been compared.

An overrun retry condition occurs if bit 4 does not activate when it should.

Bit 4 is reset when byte 11, bit 5 (allow run channel) or byte 11, bit 7 (run channel) is deactivated.

Bit 5 – Compare Successful

Bit 5 indicates during a search operation that the data from the device compared correctly with the data from the channel as specified by byte 11, bit 1 (search high) and byte 11, bit 2 (search equal). Bit 5 is set only when CDX end-of-transfer, byte 8, bit 4 (CDX end-of-transfer) is active.

Bit 6 – First Sync In Latch

Bit 6 is set by the first sync-in that occurs after byte 16, bit 7 (run device) is activated.

Bit 6 is reset when byte 16, bit 7 (run device) is deactivated.

Bit 7 – Channel Truncation

Bit 7 is set during data transfer when the channel responds to a service in or data in signal with command out instead of service out or data out.

Bit 7 is reset when byte 11, bit 5 (allow run channel) is deactivated.

Sense Byte 9 – Transfer Error Status (XES)

Sense byte 9 displays check 2 information used for error recovery and field replaceable unit (FRU) identification.

Bit 0 – Device Overrun

Bit 0 is set when the control interface detects an overrun condition during data transfer.

Bit 0 is set under the following two conditions:

- Read mode – the main buffer is full and cannot receive any more data from the control interface
- Write mode – the main buffer is empty and cannot send any more data to the control interface.

The above two conditions are caused by the channel transferring data at less than the normal rate or a circuit failure. If a circuit failure has occurred, XES, bit 4, is set.

During a write operation, bit 0 causes the following data to the device to be written as all zeros with correct parity.

Bit 1 – Channel Overrun

Bit 1 is set when one of the following conditions occurs during the data transfer mode:

- Out tags sequence is not normal
- Data out or service out is less than 80 nanoseconds
- More out tags received than requested
- Out tags overlap more than 100 nanoseconds.

Bit 2 – Control Interface Parity Check

Bit 2 is set when a device bus in parity check occurs.

Bit 3 – Clock (CLK) Check 2

Bit 3 is set when a clock check condition is detected on the data transfer data (DXD), channel data transfer (CDX), channel sequence control (CSC), or control interface (CTL-I) cards. The card detecting the check sets its own card check bit.

A CDX or CSC clock check sets byte 12, bit 7 of format 3 (channel check 1). See SENSE 145 for details of byte 12. The associated level 1 interrupt condition is also set.

Bit 4 – Director-to-Device Controller (DDC) Card Check

Bit 4 indicates that the DDC card detected one of the following conditions:

- Device tag gate (DTG) parity check
- Control interface (CTL-I) control check
- Clock (CLK) check
- Device tag out (DTO) parity check
- Device bus out (DBO) parity check.

Bit 5 – Control Interface Sync In Check

Bit 5 indicates a control interface failure caused by one of the following:

- The device continues to send sync-in after the device count equals 0.
- The sync-in signal is more than 310 nanoseconds.

Bit 6 – Channel Buffer Parity Check

Bit 6 is set either when a parity check is detected on data between the channel and the buffer or when an overrun is detected between the channel and the buffer.

Bit 7 – Device Buffer Parity Check

Bit 7 is set either when a parity check is detected on data between the device and the buffer or when an overrun is detected between the device and the buffer.

Format 2—Sense Byte 9 SENSE 65

Format 2—Sense Byte 10

Sense Byte 10 – Check (CHK) Register

Sense byte 10 displays check 2 information used for error recovery and field replaceable unit (FRU) identification. When bits 0 through 3 are set, transfer complete status (XCS), byte 8, bit 0, is also set.

Bit 0 – Data Transfer Addressing (DXA) Card Check

Bit 0 indicates a DXA card failure that is caused by one of the following conditions:

- Channel buffer pointer (CBP) parity check
- Device buffer pointer (DBP) parity check
- Buffer ALU pointer (BAP) parity check
- Data transfer control (DXC) parity check
- Buffer array out gate one-and-only-one check
- DXA data out register (DOR) select check.

Bit 1 – Device Counter (DCT) Card Check

Bit 1 indicates a failure of the device counter card because of a parity check on the following registers:

- Device count high (DCH)
- Device count low (DCL)
- Maintenance control and/or sense (MCS)
- Pad counter (PCR).

Bit 2 – Channel Search (CSR) Card Check 2

Bit 2 indicates a hardware failure on the channel search card because of one of the following:

- A parity check on the channel high or channel low registers.
- A channel duplicate compare check.

Bit 3 – Channel Data Check

Bit 3 is set when one of the following occurs:

- Halt I/O check
- Channel longitudinal redundancy check (LRC).

Bit 4 – Array Out Parity Check

Bit 4 indicates a parity check on the data leaving the buffer.

Bit 5 – Sense Register Check

Bit 5 indicates a check condition in the transfer complete status (XCS) register hardware.

Bit 6 – Data Transfer Data (DXD) Card Check

Bit 6 indicates a DXD card failure caused by one of the following conditions:

- DXD clock check:
  - Multiple clock check
  - Clock sequential check
  - Load external register clock check
  - External register select check
  - External register address parity check
  - External register multiple decode check

  Any of these six conditions also sets clock check two.
- Buffer state check
- Data in register (DIR) select check
- Data out register (DOR) select check
- Early pad check
- Write enable compare check.

Bit 7 – ADT/ASDM Card Check

Bit 7 is defined as a CMCA card check to indicate errors in the automatic data transfer (ADT) buffer and the auxillary storage director microprocessor (ASDM).

Format 2—Sense Byte 10 SENSE 70

Sense Byte 11 – Channel Transfer Control

Sense byte 11 represents the CXC register, which controls the channel data transfer hardware.

Bit 0 – Storage Director Service In

Bit 0 is activated by the storage director to generate a channel interface service in when data transfer is not being done.

Bits 1 and 2 – Search High and Search Equal

When bits 1 and/or 2 are active, the channel control hardware enters the search mode, as indicated below:

BITS 1	BITS 2	ACTION
0	0	Not search mode
0	1	Search equal
1	0	Search high
1	1	Search high or equal

If at the end of the search operation the action indicated is correct, XCS, bit 5 (compare successful) is set.

A high condition indicates the device data is higher than the main storage data. Bits 1 and 2 must be off to do a read or write operation.

Bit 3 – CBI or CBO Select Bit

Bit 3 is used to read either CBO or CBI when the external register address decode X'06' is active, as shown below:

BIT 3	ACTION
0	Read CBO
1	Read CBI

Bit 4 – Set Speed Control Register

Bit 4, when activated, is used to gate the contents of CXC, bits 1 through 3, 6, and 7 into the channel speed control (SPC) register. This transfer occurs on every cycle that CXC, bit 4, is set.

Bit 5 – Allow Run Channel

Bit 5 is used with bit 7 (run channel).

Bit 6 – Data Transfer (DXR) From Channel

Bit 6 indicates the direction of the data transfer as follows:

- Activated – transfer from the channel to the data transfer hardware
- Deactivated – transfer from the data transfer hardware to the channel.

Bits 1 and 2 (CXC) must be deactivated to do a read or write operation.

Bits 1, 2, and 6 (CXC) must not be changed until bit 7 (run channel) is deactivated. If bits 1, 2, and 6 are changed before bit 7 is deactivated, the channel data transfer (CDX) card switches the direction of the data transfer and cause a data bus parity check.

Bit 7 – Run Channel

Bit 7 indicates that data transfer between the data transfer hardware and the channel is to be completed. The channel mode control circuits are deactivated when bit 7 is deactivated.

Bits 5 and 7 are used together to start, stop, or reset and initialize the CDX automatic data transfer control circuits as follows:

BITS 5	BITS 7	ACTION
0	0	Data transfer stops. Control circuits are reset and initialized.
0	1	Data transfer stops. Control circuits are reset and initialized.
1	0	Data transfer stops and idles. The only signal reset is CDX end-of-transfer XCS, (bit 4). If bit 7 is activated, data transfer continues where it left off.
1	1	Normal data transfer function

Both bits 5 and 7 must be activated for data transfer to occur.

Bit 7 is normally used as a clutch, causing data transfer hardware to idle when bit 7 is deactivated or to continue when bit 7 is activated.

Bit 5 must be deactivated to reset and initialize the channel data transfer circuits. This must be done once and only once for each CCW.

Sense Byte 12 – Channel Control 2 (CC2) Register

Sense byte 12 represents the CC2 register. The microprocessor can set and reset bits 0 and 1 of this register.

Bits 4, 6, and 7 are set by the hardware only. Bit 4 is reset by the microprocessor.

The hardware resets the complete register during power on reset (POR), IML reset, or disable interface reset.

Bit 0 – Force Select Out

Bit 0 is set by the microcode, which permits the hardware to do the select out procedure.

Bit 1 – Read Address Switch

Bit 1 is set to permit the hardware to gate the control unit address switch settings to the microprocessor through the channel bus out (CBO).

Because of the asynchronous condition between gates, the value of the address switches is valid when a maximum of 440 nanoseconds is reached after bit 1 is set.

The microprocessor deactivates bit 1 after the address switch settings are read so the CBO can be used for normal gating.

Bits 2 and 3

Bits 2 and 3 are not used.

Bit 4 – Channel Switch Locked

Bits 4, 5, 6 and 7 inform the microprocessor the interface to be selected. The hardware sets these bits at the first selection. While bit 4 is set, bits 5, 6 and 7 are not changed by the hardware, even if additional channels request service.

Microcode resets bit 4 (unlocked, bit equals 0) when the selected channel operation is completed. The hardware resets bits 5, 6 and 7, or sets them to a new channel if another request is activated.

Bit 5 – Channel Select Bit 4 (Four Channel Switch, Additional)

See bit 4 for details.

Bit 6 – Channel Select Bit 2

See bit 4 for details.

Bit 7 – Channel Select Bit 1

See bit 4 for details.

Sense Byte 13 – Device Bus Out (DBO)

Sense byte 13 represents the DBO register (DBOH for 3380). This register is loaded with data from data transfer bus out during automatic data transfer to the device when device tag gate (DTG), bit 7 (run device), is active.

The register can be loaded or read by the microprocessor for use as a normal external register regardless of the setting of DTG, bit 7.

A microcode load or read generates not predictable results if DTG, bit 7, is active during automatic data transfer to the device.

This register is reset by IML or power on reset only (special reset).

Sense Byte 14 – Device Bus In (DBI)

Sense byte 14 represents the DBI register, (DBIL for 3380), which is loaded with data during any of the following conditions:

- Data from device bus in is loaded during automatic data transfer when DTG, bit 7 (run device) and sync in from the device are active.
- During manual data transfer when DTG, bit 7 (run device) is not active, DBI is loaded with data from device bus in at each T0 clock time when tag valid and tag gate are active.
- Device status information is loaded during the T0 clock time that occurs after the leading edge of either normal end or check end lines.
- The microprocessor can load a device bus in value when run device, as well as tag valid, normal end, check end, or sync in are active. An external register load micro-instruction, address X'08', is executed to complete the special load.

Parity checking is as follows:

- During automatic data transfer, device bus in parity is checked.
- During manual data transfer when DTG bits 5 and 6 are set to 0 and 1 respectively. Parity is checked during tag valid (with tag gate), check end, or normal end. All other conditions of DTG bits 5 and 6 disable DBI parity checking.

The DBI register can be read by the microprocessor regardless of the setting of DTG, bit 7 (run device). However, reading back the contents of DBI during a read mode data transfer risks inspecting the data at a transitional state.

3350 Sense Byte 15 – Device Tag Out (DTO)

Sense byte 15 represents the DTO register, which contains device tag out in bits 0 and 4 through 7. Bits 1 and 2 contain diagnostic sync-in information.

The DTO register is reset by IML or power on reset only (special reset). See the OPER section for details of special reset.

Bit 0 – Device Tag Out

Bits 0 and 4 through 7 contain control or command information to the device.

Bit 1 – Diagnostic Sync In

Bit 1 indicates the microcode forced a sync in. In diagnostic mode, when the automatic data transfer circuits are set up, a single transfer cycle occurs for each transition of DTO, bit 1, from an inactive to an active status.

Bit 2 – Maintain Device Tag Out Parity

Bit 2 must maintain even parity across bits 1 through 3 of this register.

The DTO parity bit maintains odd parity across DTO, bits 0 and 4 through 7.

Bit 3

Bit 3 is not used.

Bits 4 through 7

See bit 0, device tag out.

3380 Sense Byte 15 – Device Tag Out (DTO)

Sense byte 15 bits have special meanings when 3380s are attached to the storage director.

Bit 0 – Device Tag Out Bit 0

Bit 0, together with bits 1 and 2, contain the outbound tags that validate outbound controls or instructions sent to the device. These bits are set by microcode only. Bit 0 can be reset by hardware.

The combinations of these three bits have the following meanings:

BITS 0 1 2	ACTION
0 0 0	Null disconnect
0 0 1	Sync out select
0 1 1	Selected null
0 1 0	Request connection check 1
1 0 0	Poll
1 0 1	Request connection check 2
1 1 1	Command gate
1 1 0	Hardware immediate

Bit 1 – Device Tag Out Bit 1

See bit 0.

Bit 2 – Device Tag Out Bit 2

See bit 0.

Bits 3 Through 7

Bits 3 through 7 are not used.

3350 Sense Byte 16 – Device Tag Gate (DTG)

Sense byte 16 represents the DTG register, which contains the outbound device tag gates in bits 0 through 2, and device data transfer controls in bits 3 through 7. The microprocessor loads the DTG register.

Bit 0 – Select Hold

Bit 0 indicates a device is selected. The bit resets after either normal end or check end is deactivated.

Bit 1 – Tag Gate

Bit 1 indicates a tag is present on the tag bus. This bit resets when the control interface receives tag valid from the device.

Bit 2 – Response Gate

Bit 2 indicates the control interface received either normal end or check end from the device.

Bit 3 – Reset Index Latch

Bit 3 indicates the index latch is to be reset. When bit 3 is active, bit 6 of device tag in is reset.

Bit 4 – Inhibit First Decrement

Bit 4 indicates the device count high (DCH) and the device count low (DCL) registers are to be lowered by one only after the first byte of data is transferred from or to the device. This is done when the first byte of data is a sync byte.

During a read operation, bit 4 also inhibits the transfer of the sync byte to the data transfer hardware.

During a write operation, bit 4 permits the first byte to be loaded before the operation by the microprocessor into the device bus out (DBO) register.

Bits 5 and 6 – Control Interface Control

Bits 5 and 6 control the following:

- The direction of device data transfer
- Parity checking on the device bus in (DBI) register for manual and automatic data transfer.

Four parity checking operations are listed below:

BITS 5 6	ACTION
0 0	Clocking mode, inhibit DBI parity check
0 1	Data transfer from the device, permit DBI parity check.
1 0	Data transfer to the device, inhibit DBI parity check.
1 1	Data transfer from the device, inhibit DBI parity check (manual transfer only).

When bits 5 and 6 equal X'01', the device count high (DCH) and the device count low (DCL) registers are lowered by one, and sync out is generated for each sync in. Communication with the data buffer is inhibited.

Bit 7 – Run Device

Bit 7 indicates that automatic data transfer between the control interface and the device is taking place.

Bit 7 is reset by an IML or a power on reset only (special reset).

3380 Sense Byte 16 – Device Tag Gate (DTG)

Sense byte 16 bits have special meanings when 3380s are attached to the storage director.

Bit 0 – One Byte Device

When bit 0 is active, the control interface is set up for a 1-byte wide data transfer. When bit 0 is not active, the data transfer is 2-bytes wide.

Bit 1 – Block Diagnostic Set

When bit 1 is active, diagnostic sync in is prevented from setting the device bus out (DBO) high and low registers, forcing a parity check. When bit 1 is not active, the setting of DBO high and low is normal.

Bit 2 – Diagnostic Sync In

Bit 2 is used to force sync in under microcode control.

Bit 3 – Inhibit Bus Out Parity

When bit 3 is active, it inhibits the parity bit of device bus out (DBO) high and low registers from being gated on the DBO. This checks the DBO parity checking circuits.

Bit 4

Bit 4 is not used.

Bits 5 and 6 – Director-to-Device Control Bits 0 and 1

Bits 5 and 6 are used by the microcode to control the direction of the automatic data transfer and the state of the parity checking circuits (on or off) of the device bus in (DBI) high and low registers, as follows:

BITS 5 6	ACTION
0 0	Clocking mode, inhibit parity checking
0 1	From device, permit parity checking
1 0	To device, inhibit parity checking
1 1	From device, inhibit parity checking

Note: In clocking mode, the counter is lowered by one with each sync in, sync out is generated, but no data transfer takes place.

Bit 7 – Run Device

When bit 7 is active, automatic data transfer is enabled. When bit 7 is not active, all control interface control circuits are reset, the bus 1 receiver is gated, and the bus 0 driver is gated.

Format 2—Sense Byte 17

3350 Sense Byte 17 — Device Tag In (DTI)

Sense byte 17 represents the DTI register, which contains device tag in signals and the index latch.

Bit 0 — Select Active

Bit 0 indicates a device was selected. Bit 0 remains active as long as bit 0, select hold, of the device tag gate (DTG) register is active. Bits 0 and 1 of the DTI register activate together during a selection sequence.

Bit 1 — Tag Valid

Bit 1 indicates the device received the tag decod3 from the storage director. Bit 1 remains active until bit 1 device tag gate (DTG) is deactivated.

Bit 2 — Check End

Bit 2 indicates a not normal end condition exists. Bit 2 remains active until device tag gate, DTG, bit 1, is deactivated or until byte 16, bit 2 (response gate) is activated.

Bit 3 —

Bit 3 indicates that the device is in CE mode.

Bit 4 — Normal End

Bit 4 indicates that an operation on the device ended as expected.

Bit 5 — Device Alert

Bit 5 indicates an error occurred in the device.

Bit 6 — Index Latch

Bit 6 indicates that index or a correctable error code condition pattern is detected.

Bit 7 — Error Alert

Bit 7 indicates a hardware error in the device. Bit 7 activates a check 2 condition.

3380 Sense Byte 17 — Device Tag In

Sense byte 17 bits have special meanings when 3380s are attached to the storage director.

Bit 0 — Connector Check Alert

Bit 0 is set to the state of the control interface connection check alert signal.

Bit 1 — Tag In Sequence Check

Bit 1 is set by the control interface hardware when an illegal state transition is detected on the Device Tag In lines. Bit 1 is reset with check reset.

Bit 2 — End Operation and Not Command Gate

Bit 2 is active when the end operation inbound tag is active and the command gate outbound tag is not active.

Bit 3

Bit 3 is not used.

Bit 4 — Null Disconnect

Bits 4 through 7 are set according to the decode of the inbound interface tag lines, as follows:

TAG LINES	DTI BIT	ACTION
0 0	4	Null disconnect
0 1	5	Valid sync in
1 1	6	Selected null
1 0	7	End operation

Bit 5 — Valid/Sync In

See bit 4 for details.

Bit 6 — Selected Null

Set bit 4 for details.

Bit 7 — End Operation

See bit 4 for details.

Sense Byte 18 – Channel Status 2 (CS2) Register

Sense byte 18 represents the CS2 register, which is set by the hardware and reset by the microprocessor. The hardware also resets this register under the following conditions:

- Power on
- Initial microcode load
- Recovery from a disable interface condition (two check 1's before the microprocessor recovery).

Bits 4 through 7 are reset by check reset.

Parity is generated when the CS2 register is read.

Bit 0 – Halt I/O

Bit 0 is set when address out and operational in are active and select out is not active. Any external load instruction to the CS2 register resets bit 0.

Bit 1 – Selective Reset

Bit 1 is set when the following conditions occur together:

- Suppress out
- Operational in
- Not operational out
- Remember operational out latch.

Bit 1 is reset by any external load instruction to the CS2 register.

Bit 2 – System Reset

Bit 2 is set from corresponding latches on each channel interface at the time the channel interface is switched. If the IML latch is not active, the CIF system reset latch requests service.

Bit 2 is reset by any external load instruction to the CS2 register.

The system reset latch on each CIF is set from the following three major sources:

1. The channel sets the CIF system reset latch concurrently with not operational out, not suppress out, remember operational out, and not operational out delayed latches.
2. The interface disable latch sets the CIF system reset latch if the remember operational out latch is active. The remember operational out latch makes the reset occur only once for each transition from enabled to disabled.
3. The IML latch sets the CIF system reset latch. However, the request for service is stopped until the IML latch is reset. The IML latch is set by a power on reset, an IML maintenance command, or a reset maintenance command.

Bit 3 – Two or Four Channel Additional Condition Register (TACR/FACR) Card Check

Bit 3 is not used if the machine does not have either the two channel additional feature or the four channel additional (eight channel) feature.

With the two channel additional feature installed, bit 3 is named the two channel additional condition register (TACR) card check. This bit is active when the TACR card detects a check condition on channels C or D.

With the four channel additional (eight channel) feature installed, bit 3 is named the four channel additional condition register (FACR) card check. This bit is active when the FACR card detects a check condition on one of the channels E through H.

The following check conditions activate bit 3:

- Request in logic failure
- Suppress out failure
- Register 17 logic (bit) failure
- Register 17 decode parity failure.

Bit 4 – Channel Sequence Control (CSC) or Four Channel Additional Sequence Control (FASC) Card Checks

Bit 4 is active when one of the following check conditions occur:

- Channel sequence control clock check

  Detected if a clock pulse is continuously up, continuously down, or active out of sequence. This condition also sets XES register bit 3 (clock check 2).

- In tag check

  Detected when address in is active concurrently with service or data in or status in is active concurrently with service or data in.

- Channel select check

  Detected when more than one channel is selected, the selected channel does not follow the priority plan used, or a lock bit failure has occurred.

- Register 16 check

  Detected when bit 0, bit 1, and a special parity latch for bits 0 and 1 do not contain odd parity.

- CC1 parity check

  Detected on wrong parity in CC1 register.

The FASC card replaces the CSC card on machines with the four channel additional (eight channel) feature.

Bit 5 – Channel Bus Out (CBO) Parity Check

Bit 5 is set when the hardware detects a parity error on the bus out from the channel. The check is made during command out following address in and during data transfer. This check causes a check 2 and sets XES, bit 0.

Bit 6 – Two Channel Condition Register (TCR) Card Check

Bit 6 is set when the two channel condition register card detects a check condition on channels A or B, as follows:

- Request in logic failure
- Suppress out logic failure
- Register 17 logic (bit) failure
- Register 17 decode parity failure.

Bit 7 – Channel Check 1

Bit 7 is a summary check bit for channel checks. When bit 7 is active, an interrupt level 1 condition is set in interrupt level register (ILR), bit 1 (new level 1).

Bit 7 is set when any of the following check conditions are active:

- CRO, bit 1 (CIF card check)
- CS2, bit 3 (TACR/FACR card check)
- CS2, bit 4 (CSC/FASC card check)
- CS2, bit 6 (TCR card check).

Format 2—Sense Byte 18 SENSE 95

Sense Byte 19 – Toggle, FRU Register (TFR)

Sense byte 19 indicates the status of the buffer pointer toggle latches, the channel buffer latches, and FRU information differing between buffer card 1 (BFR-1) and buffer card 2 (BFR-2).

Bit 0 – Channel Buffer Pointer (CBP) Toggle

Bit 0 specifies which half of the channel buffer pointer (CBP) is available for microcode access. If bit 0 is off, channel buffer pointer low (CBL) is available; if bit 0 is on, channel buffer pointer high (CBH) is available.

Bit 1 – Device Buffer Pointer (DBP) Toggle

Bit 1 specifies which half of the device buffer pointer (DBP) is available for microcode access. If bit 1 is off, device buffer pointer low (DBL) is available; if bit 1 is on, device buffer pointer high (DBH) is available.

Bit 2 – Buffer ALU Pointer (BAP) Toggle

Bit 2 specifies which half of the buffer ALU pointer is available for microcode access. If bit 2 is off, buffer ALU pointer low (BAL) is available; if bit 2 is on, buffer ALU pointer high (BAH) is available.

Bit 3 – FRU Address Bit 1

Bit 3 stores bit 1 of the buffer array address when an array out parity check occurs. If this bit is 0, the BFR-1 card was being accessed when the check occurred; if this bit is 1, the BFR-2 card was being accessed.

Bit 4

Bit 4 is not used.

Bit 5 – High Speed Channel Active

Bit 5 indicates that the currently selected channel is a high speed channel.

Bit 6 – Buffer/Channel Register One (BC1) Full

Bit 6 indicates that BC1 contains a byte of data.

Bit 7 – Buffer/Channel Register Two (BC2) Empty

Bit 7 indicates that BC2 does not contain a byte of data.

Sense Byte 20 – Microcode Detected Checks

Sense byte 20 contains a 2-digit hexadecimal number that represents the type of microcode checks that generate format 2, message F.

X'01'—Model 21 only The device attempted to end data transfer before the correct time.

X'02'—Model 21 only The selection was lost at the time a device error was detected.

X'03-0F' Not used

X'10'—Model 23 only A tag out sequence check indicates that a not valid tag sequence was detected by the 3380 controller.

X'11-1F' Not used

X'20'—Model 23 only A bus out parity check was detected by the 3380 controller.

X'C2' A not expected level 2 interrupt has occurred.

X'C3' The device interface process has twice requested access repositioning during the same operation.

X'C4' The home address did not contain the correct CCHH or during an internally started find operation the correct segment number is not found in any count field

X'C5' Not used

X'C6' The channel interface process did not get enough lead during a slow channel write operation.

X'C7' A control interface command overrun occurred during a data transfer operation.

X'C8' The value of the device buffer pointer is not equal to the expected value at the end of a data transfer.

X'C9' The value of the channel buffer pointer is not equal to the expected value at the end of a data transfer.

X'CA' The channel cyclic redundancy check stored in the buffer did not equal the device cyclic redundancy check generated during transfer of the field to the device.

X'CB' The device cyclic redundancy check stored in the buffer did not equal the channel cyclic redundancy check generated while transferring the field to the channel.

X'CC' A time-out occurred while waiting for the device interface process to complete an operation.

X'CD' There is no auxiliary storage director microprocessor (ASDM) response for the search.

X'CE' Not used

X'CF' A not valid invalid parameter passed to the error analysis routine.

X'D0-D7' Not used

X'D8' A data check retry operation failed during internal retry.

X'D9' An overrun retry operation failed during internal retry.

X'DA' The offset range has been exceeded.

X'DB' A not supported retriable device error has been reported.

X'DC' Not used

X'DD' A not valid parameter was passed to the retry repositioning routine.

X'DE' An invalid parameter was passed from the lead calculation routine to the retry repositioning routine.

X'DF' A device error occurred during device repositioning.

X'E0-FF' Not used

Sense Byte 21 – Storage Director Physical Identifier (SDI)

The physical identifier is read by sensing the switch settings on the device counter (DCT) card when SDI is addressed.

Sense Bytes 22 and 23 – Symptom Code

The symptom code is a number generated from sense data by the storage control.

Format 2 Messages

Messages 0 through 7

Messages 0 through 7 are not used.

Message 8 – No Message From Storage Director

Message 8 indicates that no additional information is needed from the storage director.

Message 9 – Selective Reset Occurred While Drive Selected

Message 9 indicates that a selective reset occurred while a device was selected.

Message A – Failure To Latch First Sync In

Message A indicates that during data transfer, transfer complete status (XCS) bit 2 (director-to-device controller end-of-transfer) is activated without XCS, bit 6 (first sync in latch) being activated.

Messages B through E

Messages B through E are not used.

Message F – Microcode Detected Checks

Message F indicates that a check is detected by the microcode. See Sense Byte 20 on the environmental recording, editing, and printing (EREP) output for a message number. This message number is explained under format 2, sense byte 20, microcode detected checks. (See SENSE 100).

Format 3—Storage Director Clock Stopped Check 1

When byte 7 equals X'38', the error is a **Clock Stopped Check 1**, and the table below gives a summary of bytes 8 through 23. See SENSE 115-120 for more information on these types of errors.

Note: When byte 7 equals X'39' or X'3A', the error is a Storage Director Channel Check 1 or a Trace Table Saved; see SENSE 125-160 for more information.

BYTE NAME	BYTE	BITS 0	1	2	3	4	5	6	7
FRU Register 2 (FR2)	8	Maintenance (MNT) Register Group Selected	Director-to-Device Controller (DDC) Register Group Selected	Automatic Data Transfer (ADT) Register Group Selected	Channel Sequence Control (CSC) Register Group Selected	External Register Select	Unrecoverable Check 1	Control Storage Store	Read Only Storage (ROS) Selected
Check Register 1 (CK1)	9	ALU Bus Out Parity Check	External Register Address Parity Check	Channel Sequen. Control (CSC) ALU Bus Out Check	Storage Director Microprocessor (SDM) Card Check	Microprocessor Chip Check	Dynamic Control Storage Uncorrectable Data Check	Maintenance Clock Check	Not Used
Check Register 2 (CK2)	10	Maintenance (MNT) Multiple Decode Check	Clock (CLK) Card Check	Dynamic Refresh Control (DRC) or Dynamic Ctrl Storage and Refresh (DCSR) Card Check	Invalid Sequence Check	Dynamic Refresh Control (DRC) Card Check	Invalid Address Check	Control Storage Address Check	Dynamic Control Storage Write Data Check
Check Register 3 (CK3)	11	Control Storage Data Check	Internal or External Register ALU In Check	Internal Microprocessor Check	Microprocessor Program Status Word Swap Latch	Microprocessor Microinstruction Register Bit 0	Microprocessor Equal or All Condition Code	Microprocessor Zero or None Condition Code	Microprocessor Carry Condition Code
Bytes 12 through 14 are not used.									
FRU Register 3 (FR3)	15	Control Storage Address Bit 2	Control Storage Address Bit 3	Control Storage Address Bit 0 or Bit 1	Port Connection Register Group Selected	Not Used	Not Used	Not Used	Not Used
FRU Register 4 (FR4)	16	Not Used	Not Used	Not Used	External Register Address Bit 0	External Register Address Bit 1	External Register Address Bit 2	External Register Address Bit 3	External Register Address Bit 4
Bytes 17 through 20 are not used.									
Storage Director Physical Identifier (SDI)	21	Bits in this byte equal the settings of the storage director ID switches on the DCT card.							
Symptom Code	22-23								

Sense Byte 8 – FRU Register 2

Bit 0 – Maintenance (MNT) Register Group Selected

Bit 0 indicates the maintenance (MNT) card decoded an external register address.

Bit 1 – Director-to-Device Controller (DDC) Register Group Selected

Bit 1 indicates the director-to-device controller (DDC) card decoded an external register address.

Bit 2 – Automatic Data Transfer (ADT) Register Group Selected

Bit 2 indicates the automatic data transfer hardware decoded an external register address.

Bit 3 – Channel Sequence Control (CSC) Register Group Selected

Bit 3 indicates the channel sequence control (CSC) card decoded an external register address.

Bit 4 – External Register Select

Bit 4 is set when an external register operation is being performed.

Bit 5 – Unrecoverable Check 1

Bit 5 indicates that a solid check has occurred and the storage director can not recover from the check.

Bit 6 – Control Storage Store

Bit 6 indicates a data store cycle to control storage was in process when a check condition occurred.

Bit 7 – Read-Only Storage (ROS) Selected

Bit 7 indicates the microcode was executing from read-only storage (ROS) when the condition check occurred.

Sense Byte 9 – Check Register 1

Bit 0 – ALU Bus Out Parity Check

Bit 0 indicates not correct parity is detected from the storage director microprocessor (SDM) card. The check is made on the maintenance card every time-zero (T0) clock time. When inhibit bus in check to the microprocessor is not active, not correct parity on microprocessor input data generates not correct parity on ALU bus out.

Bit 1 – External Register Address Parity Check

Bit 1 indicates not correct parity is detected on the external register address bus from the SDM card. The check is made on the maintenance card every time-zero (T0) clock time. During a microinstruction fetch, not correct parity on control storage data out can cause not correct parity on the external register address bus.

Bit 2 – Channel Sequence Control (CSC) ALU Bus Out Check

Bit 2 indicates not correct parity is detected on ALU bus out from the SDM card. When inhibit bus in check to the microprocessor is not active, not correct parity on microprocessor input data generates not correct parity on ALU bus out.

Bit 3 – Storage Director Microprocessor (SDM) Card Check

Bit 3 indicates that any of the following check conditions have been detected on the SDM card:

- Internal register local store address parity check
- Data even or data odd bus in gating check

Bit 4 – Microprocessor Chip Check

Bit 4 indicates a check condition is detected by the SDM card. Check register 3 describes the check conditions detected by the microprocessor.

Bit 5 – Dynamic Control Storage Or Uncorrectable Data Check

Bit 5 indicates that the data fetched during a dynamic control storage fetch cycle contained a double-bit error that could not be corrected by the error correction hardware.

Bit 6 – Maintenance Clock Check

Bit 6 indicates the maintenance card detected a not valid clock sequence.

Bit 7

Bit 7 is not used.

Format 3—Clock Stopped Check 1–Sense Bytes 8-9 SENSE 115

Sense Byte 10 – Check Register 2

Bit 0 – Maintenance (MNT) Multiple Decode Check

Bit 0 indicates more than one external register address in the maintenance group is being decoded and a failure in the external address decoder hardware on the maintenance card has occurred.

Bit 1 – Clock (CLK) Card Check

Bit 1 indicates that a clock ring gate check is detected on the clock card. The check occurs when more than one of the non-overlapping gates on the clock ring are active at the same time.

Bit 2 – Dynamic Refresh Control (DRC) Hold Check Or Dynamic Control Storage And Refresh (DCSR) Card Check

Bit 2 indicates that one or more of the following check conditions have occurred:

- Refresh timer check
- Refresh address timer check
- Key bit check.

Bit 3 – Invalid Sequence Check

Bit 3 indicates the clock card detected that start and stop are active together from the maintenance card.

Bit 4 – Dynamic Refresh Control (DRC) Card Check

Bit 4 indicates that a parity check has been detected on the DRC card.

Bit 5 – Invalid Address Check

Bit 5 indicates that a not valid address check has been detected.

Bit 6 – Control Storage Address Check

Bit 6 indicates the static control storage (SCS) or the dynamic control storage refresh (DCSR) cards detected not correct parity on the control storage address bus.

Bit 7 – Dynamic Control Storage Write Data Check

Bit 7 indicates that during a store cycle, the DCSR card detected not correct parity on the control storage data bus.

Sense Byte 11 – Check Register 3

Bit 0 – Control Storage Data Check

Bit 0 indicates not correct parity is detected on the data even or data odd bus in during micro-instruction or data fetch cycles. Check register 1, byte 9, bit 4 (microprocessor chip check) is also set.

Bit 1 – Internal or External Register ALU In Check

Bit 1 indicates not correct parity is detected on data even or data odd bus in when the contents of an internal or external register are being gated to the ALU. Check register 1, byte 9, bit 4 (microprocessor chip check) is also set.

Bit 2 – Internal Microprocessor Check

Bit 2 indicates any of the following check conditions are detected in the microprocessor chip:

- Not correct parity in the internal register group (IRG) register or in the instruction address register (IAR).
- Branch decision check.
- Clock decoder check.

Check register 1, byte 9, bit 4 (microprocessor chip check) is also set.

Bits 3 Through 7 – Microprocessor Status

Bits 3 through 7 are status conditions that are latched in the microprocessor at the time the check condition occurs.

Sense Bytes 12 – 14

Sense bytes 12 through 14 are not used.

Sense Byte 15 – FRU Register 3

Bits 0 Through 2 – Control Storage Address

Bits 0 through 2 indicate the high-order control storage address bits at the time the check condition occurs.

Bit 3 - Port Connection Register Group Selected.

Bit 3 indicates that the subsystem storage port connection decoded an external register address.

Bits 4 Through 7

Bits 4 through 7 are not used.

Sense Byte 16 – FRU Register 4

Bits 0 Through 2

Bits 0 through 2 are not used.

Bits 3 Through 7 – External Register Address

Bits 3 through 7 indicate the external register address bus at the time the check condition occurs.

Sense Bytes 17 through 20

Bytes 17 through 20 are not used.

Sense Byte 21 – Storage Director Physical Identifier (SDI)

Sense byte 21 identifies the storage director causing the error.

The physical identifier is read by sensing the switch settings on the device counter (DCT) card when SDI is addressed.

Sense Bytes 22 and 23 – Symptom Code

The symptom code is a number generated from sense data by the storage control.

Format 3 Messages

All format 3 messages are described on SENSE 165.

Format 3—Storage Director Channel Check 1

When byte 7 equals X'39' or X'3A', the error is a **Storage Director Channel Check 1** or a **Trace Table Saved**. The table below gives a summary of bytes 8 through 23. See SENSE 130-160 for more information on these types of errors.

Note: When byte 7 equals X'38', the error is a Clock Stopped Check 1; see SENSE 110-120 for more information.

BYTE NAME	BYTE	BITS 0	1	2	3	4	5	6	7
	8	Not Used							
Transfer Error Status (XES)	9	Device Overrun	Channel Overrun	Control Interface Parity Check	Clock (CLK) Check 2	Director to Device Controller (DDC) Card Check	Control Interface Sync In Check	Channel Buffer Parity Check	Device Buffer Parity Check
Check (CHK) Register	10	Data Transfer Addressing (DXA) Card Check	Device Counter (DCT) Card Check	Channel Search (CSR) Card Check 2	Channel Data Check	Array Out Parity Check	Sense Register Check	Data Transfer Data (DXD) Card Check	Port Connection/ADT Buffer Check
Condition Register 0 (CR0)	11	Channel Bus In (CBI) Parity Check	Channel Interface (CIF) Card Check	Channel Data Transfer (CDX) Card Check	Channel Search (CSR) Card Check 1	Two or Four Channel Addit. Clock Check	Channel Clock Check for Four Channel Addit. Feature	Not Used	Not Used
Channel Status 2 (CS2) Register	12	Halt I/O	Selective Reset	System Reset	Two or Four Channel Addit. Condition Register (TACR/FACR) Card Check	Channel Sequen. Control (CSC) or Four Channel Addit. Sequence Control (FASC) Card Check	Channel Bus Out (CBO) Parity Check	Two Channel Condition Register (TCR) Card Check	Channel Check 1
Channel Control 1 (CC1) Register	13	Operational In	Address In	Status In	Long Select	Control Unit Busy	Condition Register 17 Select, Bit 4	Condition Register 17 Select, Bit 2	Condition Register 17 Select, Bit 1
Channel Control 2 (CC2) Register	14	Force Propagate Select Out	Read Address Switch	Not Used	Not Used	Channel Switch Locked	Channel Select Bit 4	Channel Select Bit 2	Channel Select Bit 1
Channel Status 1 (CS1) Register	15	Service Out	Address Out	Command Out	Not Used	Select Out Trapped	Status In Tag	Data Out	Suppress Out
Channel Status 3 (CS3) Register	16	Command Chain Complete	Command Chain Aborted	Chained Initial Status	Activate Chain Reselect	Not Used	Trace Control 0	Trace Control 1	Trace Control 2
Channel Transfer Control (CXC)	17	Microprocessor Service In	Search High	Search Equal	CBI or CBO Select Bit	Set Speed Control Register	Allow Run Channel	Data Transfer (DXR) from Chn.	Run Channel
Channel Bus Out	18	Contents of CBO Register							
Channel Bus In	19	Contents of CBI Register							
Interrupt Level or Interval Timer Message 3F2X	20	Last Level Bit 2	Last Level Bit 1	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
		Time-Out Message							
Storage Director Physical Identifier (SDI)	21	Bits in this byte equal the settings of the storage director ID switches on the DCT card.							
Symptom Code	22-23								

Sense Byte 8

Byte 8 is not used.

Sense Byte 9 – Transfer Error Status (XES)

Sense byte 9 displays check 2 information used for error recovery and field replaceable unit (FRU) identification. To read the XES register, data transfer control (DXC), bits 0 and 3 must be set to X'01'.

The check 2 bit, XCS register, bit 0, is set by the OR of the XES register.

Bit 0 – Device Overrun

Bit 0 is turned on when the control interface detects an overrun condition during data transfer.

Bit 0 is set under the following two conditions:

- Read mode – the main buffer is full and cannot receive any more data from the control interface.
- Write mode – the main buffer is empty and cannot send any more data to the control interface.

The above two conditions are caused by the channel transferring data at less than the normal rate or a circuit failure. If a circuit failure has occurred, XES, bit 4, is set.

During a write operation, bit 0 causes following data to the device to be written as all zeros with correct parity.

Bit 1 – Channel Overrun

Bit 1 indicates one of the following conditions during the data transfer mode:

- Out tags sequence not normal
- Data out or service out is less than 80 nanoseconds
- More out tags received than requested
- Out tags overlap more than 100 nanoseconds.

Bit 2 – Control Interface Parity Check

Bit 2 is turned on as a result of a device bus in parity check.

Bit 3 – Clock (CLK) Check 2

Bit 3 is set when a clock check condition is detected on the data transfer data (DXD), CDX, CSC, or CTL-I cards. The card detecting the check also sets its own card check bit.

A CDX or a CSC clock check sets byte 12, bit 7 of format 3 (channel check 1). (See SENSE 145 for details of byte 12). The associated level 1 interrupt condition is also set.

Bit 4 – Director-to-Device Controller (DDC) Card Check

Bit 4 indicates that the DDC card detected one of the following conditions:

- Device tag gate (DTG) parity check
- Control interface (CTL-I) control check
- Clock (CLK) check
- Device tag out (DTO) parity check
- Device bus out (DBO) parity check.

Bit 5 – Control Interface Sync In Check

Bit 5 indicates a control interface failure caused by one of the following:

- The device continues to send sync in after the device count equals zero.
- The sync-in signal is more than 310 nanoseconds.

Bit 6 – Channel Buffer Parity Check

Bit 6 indicates a parity check on data between the channel and the buffer or an overrun detected between the channel and the buffer.

Bit 7 – Device Buffer Parity Check

Bit 7 indicates a parity check on data between the device and the buffer or an overrun detected between the device and the buffer.

Format 3—Channel Check 1–Sense Bytes 8-9 SENSE 130

Format 3—Channel Check 1–Sense Bytes 8-9 SENSE 130

Sense Byte 10 – Check (CHK) Register

Sense byte 10 displays check 2 information used for error recovery and field replaceable unit (FRU) identification. When the condition indicated occurs, the corresponding latch is set and remains active until check reset occurs. Bit 0, (check 2) of the transfer complete status (XCS) register is also set.

To read the CHK register, set data transfer control (DXC), bits 0 and 3 to 1 and 0, respectively, and wait one micro-instruction cycle. Transfer error status (XES), XCS, or CHK must not be read immediately after DXC, bits 0 and 3 are set.

Bit 0 – Data Transfer Addressing (DXA) Card Check

Bit 0 is turned on by any of the following check conditions:

- Channel buffer pointer (CBP) parity check
- Device buffer pointer (DBP) parity check
- Buffer ALU pointer (BAP) parity check
- Data transfer control (DXC) parity check
- Buffer chip select one-and-only-one check
- Buffer array out gate one-and-only-one check
- DXA data out register (DOR) Select check.

Bit 1 – Device Counter (DCT) Card Check

Bit 1 indicates a failure of the device counter card because of a parity check on the following registers:

- Device count high (DCH)
- Device count low (DCL)
- Maintenance control and/or sense (MCS)
- Pad counter (PCR).

Bit 2 – Channel Search (CSR) Card Check 2

Bit 2 indicates a hardware failure on the channel search card because of one of the following:

- A parity check on the channel high or channel low registers
- A channel duplicate compare check

Bit 3 – Channel Data Check

Bit 3 is set when one of the following occurs:

- Halt I/O check
- Channel longitudinal redundancy check (LRC).

Bit 3 indicates a failure on one of the following cards:

- Channel interface (CIF)
- Channel sequence control (CSC)
- Channel data transfer (CDX)
- Channel search (CSR).

Bit 4 – Array Out Parity Check

Bit 4 indicates a parity check on the data leaving the buffer.

Bit 5 – Sense Register Check

Bit 5 indicates a check condition in the transfer complete status (XCS) register hardware.

Bit 6 – Data Transfer Data (DXD) Card Check

Bit 6 indicates a DXD card failure caused by one of the following conditions:

- DXD clock check:
  - Multiple clock check
  - Clock sequential check
  - Load external register clock check
  - External register select check
  - External register address parity check
  - External register multiple decode check.

  Any of the above six conditions also set clock check two.
- Buffer state check
- Data in register (DIR) select check
- Data out register (DOR) select check
- Early pad check
- Write enable compare check.

Bit 7 – Port Connection/ADT Buffer Check

This bit indicates that a bit in one of the following registers was turned on:

- Common ADT/ASDM check register (CAAJCK)
- Common port adapter check 1 register (CPACK 1)
- Common port adapter check 2 register (CPACK 2).

Sense Byte 11 – Channel Interface Checks (CR0) Register

Sense byte 11 represents the CR0 register, which indicates hardware detected check conditions in the channel interface circuits. Any of these check conditions set the following:

- Channel check 1, byte 12, bit 7
- New level 1, interrupt level register (ILR), bit 1

The CR0 register can be addressed when channel control 1 (CC1) register, byte 13, bits 5 through 7, are all 0.

The CR0 register is reset by microcode or check reset.

Bit 0 – Channel Bus In (CBI) Parity Check

Bit 0 indicates not correct parity is detected on bus in entering the channel interface (CIF) card.

Bit 1 – Channel Interface (CIF) Card Check

Bit 1 indicates the CIF card detected one of the following check conditions:

- CIF clock check
- CIF propagate select out failure
- System reset logic failure
- Pending system reset logic failure
- Channel bus in (to the channel) parity check
- Channel bus in (from the CDX card) parity check
- Read or Force Switches line from CSC card is active during data transfer
- CIF Selected line is active with CU Selected to other CIF line active.

Bit 2 – Channel Data Transfer (CDX) Card Check

Bit 2 indicates the following check conditions are detected on the CDX card:

- Channel bus out (CBO) load compare check
- CDX clock check
- Channel transfer control (CXC) parity check
- Pending parity check
- Timer and speed control parity check
- Load speed control register check
- Pending counter incremented too high.

Bit 3 – Channel Search (CSR) Card Check 1

Bit 3 is set by the following parity checks:

- CBO register parity check
- CBI register parity check
- CXC register parity check.

Bit 4 – Two or Four Channel Additional Clock Check

Bit 4 is not used if the machine does not have either the two channel additional or the four channel additional (eight channel) feature.

With the two channel additional feature installed, this bit represents a channel clock check detected on one of the two channel additional boards (A3 or A4) for channels A through D.

With the four channel additional (eight channel) feature installed, this bit represents a clock check detected on one of the four channel additional boards (A3 or A4) for channels A through D.

Bit 5 – Channel Clock Check (Four Channel Additional)

Bit 5 is not used if the machine does not have the four channel additional (eight channel) feature installed.

With the four channel additional feature, this bit represents a clock check detected on the four channel additional boards (A1 or A2) for channels E through H.

Bits 6 and 7

Bits 6 and 7 are not used.

Sense Byte 12 – Channel Status 2 (CS2) Register

Sense byte 12 represents the CS2 register, which is set from the hardware and reset by the microprocessor. The hardware also resets this register under the following conditions:

- Power on
- Initial microcode load
- Recovery from a disable interface condition (two check 1's before the microprocessor recovery).

Bits 4 through 7 are reset by check reset.

Parity is generated when this register is read.

Bit 0 – Halt I/O

Bit 0 is set when address out and operational in are active and select out is inactive. Any external load instruction to the CS2 register resets bit 0.

Bit 1 – Selective Reset

Bit 1 is set when the following conditions occur together:

- Suppress out
- Operational in
- Not operational out
- Remember operational out latch.

Bit 1 is reset by any external load instruction to the CS2 register.

Bit 2 – System Reset

Bit 2 is set from corresponding latches on each channel interface at the time the channel interface is switched. If the IML latch is not active, the CIF system reset latch requests service.

Bit 2 is reset by any external load instruction to the CS2 register.

The system reset latch on each CIF is set from the following three major sources:

1. The channel sets the CIF system reset latch concurrently with not operational out, not suppress out, remember operational out, and not operational out delayed latches.
2. The interface disable latch sets the CIF system reset latch if the remember operational out latch is active. The remember operational out latch makes the reset occur only once for each transition from enabled to disabled.
3. The IML latch sets the CIF system reset latch; however, the request for service is stopped until the IML latch is reset. The IML latch is set by a power on reset, an IML maintenance command, or a reset maintenance command.

Bit 3 – Two or Four Channel Additional Condition Register (TACR/FACR) Card Check

Bit 3 is not used if the machine does not have either the two channel additional or the four channel additional (eight channel) feature.

With the two channel additional feature installed, bit 3 is called the two channel additional condition register (TACR) card check. This bit is active when the TACR card detects a check condition on channels C or D.

With the four channel additional (eight channel) feature installed, bit 3 is named the four channel additional condition register (FACR) card check. This bit is active when the FACR card detects a check condition on one of the channels E through H.

The following check conditions activate bit 3:

- Request In logic failure
- Suppress Out failure
- Register 17 logic (bit) failure
- Register 17 decode parity failure.

Bit 4 – Channel Sequence Control (CSC) or Four Channel Additional Sequence Control (FASC) Card Check

Bit 4 is active when one of the following check conditions occur:

- Channel sequence control clock check

  Detected if a clock pulse is continuously up, continuously down, or active out of sequence. This condition also sets XES register bit 3, (clock check 2).

- In tag check

  Detected when address in is active concurrently with service or data in, or status in is active concurrently with service or data in.

- Channel select check

  Detected when more than one channel is selected, or the selected channel does not follow the priority plan used or a lock bit failure has occurred.

- Register 16 check

  Detected when bit 0, bit 1, and a special parity latch for bits 0 and 1 do not contain odd parity.

- CC1 parity check

  Detected on wrong parity in CC1 register.

  The FASC card replaces the CSC card on machines with the four channel additional (eight channels) feature.

Bit 5 – Channel Bus Out (CBO) Parity Check

Bit 5 is set when the hardware detects a parity error on the bus out from the channel. The check is made during command out following address in and during data transfer. This check causes a check 2 and sets XES, bit 0.

Bit 6 – Two Channel Condition Register (TCR) Card Check

Bit 6 is set when the two channel condition register card detects a check condition on channels A or B, as follows:

- Request in logic failure
- Suppress out logic failure
- Register 17 logic (bit) failure
- Register 17 decode parity failure.

Bit 7 – Channel Check 1

Bit 7 is a summary check bit for channel checks. When bit 7 is active, an interrupt level 1 condition is set in interrupt level register (ILR), bit 1 (new level 1).

Bit 7 is set when any of the following check conditions are active:

- CRO, bit 1 (CIF card check)
- CS2, bit 3 (TACR/FACR card check)
- CS2, bit 4 (CSC/FASC card check)
- CS2, bit 3 (TACR card check)
- CS2, bit 4 (CSC card check)
- CS2 bit 6 (TCR card check).

Format 3—Channel Check 1–Sense Byte 12 SENSE 145

Sense Byte 13 – Channel Control 1 (CC1) Register

Sense byte 13 represents the CC1 register, which supplies the selection tag in signals during normal selection sequences.

Bits 0 Through 2 – Operational In, Address In, and Status In

Bits 0 through 2 generate the channel interface signals. Operational in must be active before address in or status in can become active on the channel interface.

Bit 3 – Long Select

When bit 3 is active, it causes the hardware to present control unit busy (short) to any other channel attempting selection. This bit must be reset before CC2, bit 4 (channel switch locked bit) is reset or the control unit busy status-in latch will set not correctly.

Bit 4 – Control Unit Busy

When bit 4 is active it causes the hardware in the channel interface circuits to generate control unit busy as a response to a channel selection on any channel and to set the control unit end latch.

Bit 5 – Condition Register 17 Select Bit 4

Bits 5 through 7 are used to expand the addressing of external address 11 into eight registers as follows:

BITS 5 6 7	REGISTER	INFORMATION SELECTED
0 0 0	CR0	Channel Interface Checks
0 0 1	CR1	Allow Disable
0 1 0	CR2	Not Suppressible Register In
0 1 1	CR3	Control Unit End
0 0 0	CR4	Not Used
0 0 1	CR5	Not Used
1 1 0	CR6	Suppressible Request In
1 1 1	CR7	Not Used

Bit 6 – Condition Register 17 Select Bit 2

See bit 5 for details.

Bit 7 – Condition Register 17 Select Bit 1

See Bit 5 for details.

Sense Byte 14 – Channel Control 2 (CC2) Register

The microprocessor can set and reset bits 0 and 1 of this register.

Bits 4, 6, and 7 are set by hardware only. Bit 4 is reset by the microprocessor.

The hardware resets the complete register during power on reset (POR), IML reset, or disable interface reset.

Bit 0 – Force Propagate Select Out

Bit 0 is set by the microcode, which permits the hardware to start the select out operation.

Bit 1 – Read Address Switch

Bit 1 is set to permit the hardware to gate the control unit address switch settings to the microprocessor through the channel bus out (CBO).

Because of the asynchronous condition between gates, the value of the address switches is valid when a maximum of 440 nanoseconds is reached after bit 1 is set.

The microprocessor deactivates bit 1 after the address switch settings are read so the CBO can be used for normal gating.

Bits 2 and 3

Bits 2 and 3 are not used.

Bit 4 – Channel Switch Locked

Bits 4, 5, 6, and 7 inform the microprocessor the interface to be selected. The hardware sets these bits at initial selection time. While bit 4 is set, bits 5, 6, and 7 are not changed by the hardware, even if additional channels request service.

Microcode resets bit 4 when the selected channel operation is completed. The hardware resets bits 5, 6, and 7, or sets them to a new channel if another request is activated.

Format 3—Channel Check 1–Sense Bytes 13-14 SENSE 150

Sense Byte 15 – Channel Status 1 (CS1) Register

Sense byte 15 represents the CS1 register, which is automatically loaded with information from the channel and control unit to give status information to the microprocessor. The channel hardware also uses this information for control functions.

Correct parity is generated from the output of this register.

Bit 0 – Service Out

Bits 0 through 2, 6, and 7 are set directly from the channel by the signals listed.

Bit 1 – Address Out

See bit 0 for details.

Bit 2 – Command Out

See bit 0 for details.

Bit 3

Bit 3 is not used.

Bit 4 – Select Out Trapped

Bit 4 is set when the following conditions satisfy either a channel or a control unit initiated selection.

- Channel initiated selection set
  - Enabled
  - Not propagating select out
  - Select out
  - Address out
  - Address on bus out must compare and be in good parity
- Channel initiated selection reset
  - Force propagate select out
  - Force disable
  - Special reset
  - Not select out
- Control unit initiated selection set
  - Enabled
  - Not propagating select out
  - Select out
  - Not address out
  - Request in
- Control unit initiated selection reset
  - All channel initiated selection resets
  - Another channel selected

When bit 4 is active, it causes an interrupt level 2 condition to be set into the interrupt level register, bit 2 (new level 2).

Bit 5 – Status In Tag

Bit 5 indicates the condition of status in presented to the channel. This bit is active when byte 13, bit 2 (status in) is active or during automatic hardware sequences when status in is activated.

Bit 6 – Data Out

See bit 0 for details.

Bit 7 – Suppress Out

See bit 0 for details.

Sense Byte 16 – Channel Status 3 (CS3) Register

Sense byte 16 represents the CS3 register. Bits 0 and 1 are set by the hardware and bits 2 through 7 are set by the microprocessor. Bits 0 through 7 are reset by the microprocessor.

Bit 0 – Command Chain Complete

Bit 0 is activated during a command chaining operation when one of the following conditions occurs:

- The hardware moves to command out time after the microprocessor sets byte 16, bit 3 (activate chain reselect) at ending status time. The command is gated into channel bus out.
- The hardware moves to service out time after the microprocessor sets byte 16, bit 2 (chained initial status) at command out time.

Bit 1 – Command Chain Aborted

Bit 1 indicates the hardware detected an abort condition during a command chaining operation.

Bit 1 is activated by the following abort conditions:

- Suppress out stopped before the correct time
- Command out response to ending status
- Halt I/O.

Bit 2 – Chained Initial Status

Bit 2 is set by the microprocessor to permit the hardware to perform an initial selection sequence from command out through status in. The initial status information must be in the channel bus in register before this bit is set.

The microprocessor can also set byte 17, bit 7 (run channel) to cause the hardware to automatically enter the data transfer phase after initial status has been sent.

Bit 3 – Activate Chain Reselect

Bit 3 indicates that command chaining is being performed. This bit becomes active after ending status has been assembled. When bit 3 is set, the hardware can function through the chain reselection sequence up to command out time.

Bit 4

Bit 4 is not used.

Bits 5 through 7 – Trace Control 0, 1, and 2

Bits 5 through 7 are used only by the microcode for trace operations.

Sense Byte 17 – Channel Transfer Control (CXC)

Sense byte 17 represents the CXC register, which controls the channel data transfer hardware and selects the register (CBO or CBI) read when the external register address equals X'06'.

Bit 0 – Microprocessor Service In

Bit 0 is activated by the microprocessor to generate a channel interface service in during times when data transfer does not occur.

Bits 1 and 2 – Search High and Search Equal

When bits 1 and/or 2 are active, the channel control hardware enters the search mode as shown:

BITS 1	2	ACTION
0	0	Not search mode
0	1	Search equal
1	0	Search high
1	1	Search high or equal

If at the end of the search operation the action indicated above is correct, transfer complete status (XCS) register bit 5 (compare successful) is set.

A high condition indicates the device data is higher than the main storage data. Bits 1 and 2 must be off to do a read or write operation.

Bit 3 – CBI or CBO Select Bit

Bit 3 is used to read either CBO or CBI when the external register address decode X'06' is active as shown:

BIT 3	ACTION
0	Read CBO
1	Read CBI

Bit 4 – Set Speed Control Register

Bit 4, when activated, is used to gate the contents of channel transfer control (CXC), bits 1 through 3, 6, and 7, into the channel speed control (SPC) register. This transfer occurs on every cycle that CXC, bit 4, is set.

Bit 5 – Allow Run Channel

Bit 5 is used with bit 7 (run channel).

Bit 6 – Data Transfer (DXR) From Channel

Bit 6 indicates the direction of the data transfer as follows:

- Activated – transfer from the channel to the data transfer hardware
- Deactivated – transfer from the data transfer hardware to the channel.

Bits 1 and 2 (CXC) must be deactivated to do a read or write operation.

Bits 1, 2, and 6 (CXC) must not be changed until bit 7 (run channel) is deactivated. If bits 1, 2, and 6 are changed before bit 7 is deactivated, the channel data transfer (CDX) card switches the direction of the data transfer and causes a data bus parity check.

Bit 7 – Run Channel

Bit 7 indicates that data transfer between the data transfer hardware and the channel is to be completed. The channel mode control circuits are deactivated when bit 7 is deactivated.

Bits 5 and 7 are used together to start, stop, or reset and initialize the CDX automatic data transfer control circuits as follows:

BITS 5	7	ACTION
0	0	Data transfer stops. Control circuits are reset and initialized.
0	1	Data transfer stops. Control circuits are reset and initialized.
1	0	Data transfer stops and idles. The only signal reset is CDX end-of-transfer XCS, (bit 4). If bit 7 is activated, data transfer continues where it left off.
1	1	Normal data transfer function

Both bits 5 and 7 must be activated for data transfer to occur.

Bit 7 is normally used as a clutch, causing data transfer hardware to idle when bit 7 is deactivated or to continue when bit 7 is activated.

Bit 5 must be deactivated to reset and initialize the channel data transfer circuits. This must be done once and only once for each CCW.

Sense Byte 18 – Channel Bus Out (CBO)

Sense byte 18 represents the CBO register, which is loaded during channel communications with one of the following:

- Address out
- Command out
- Service out or data out.

Channel bus out (CBO) is also loaded when the microprocessor generates the following active bits:

- Service in
- Service out.

The CBO register is also loaded with the address switch settings if read address switch, byte 14, bit 1, is active.

This register can be read when the external address is X'06' if channel transfer control (CXC), bit 3, is active.

Sense Byte 19 – Channel Bus In (CBI)

Sense byte 19 represents the CBI register, which is used by microcode for the address during selection, and for status during the end procedure. This register is used by the hardware during automatic data transfer.

The CBI register can be read or written by microcode using external address X'06' if channel transfer control (CXC), bit 3, is active.

Sense Byte 20 – Interrupt Level or Interval Timer Message Code

Bits 0 and 1 – Last Level Bits 2 and 1

Bits 0 and 1 identify the interrupt level at which the microcode was operating when the error occurred.

Bits 2 – 7 (Interrupt Level)

Bits 2 through 7 are not used.

Bits 0 – 7 Interval Timer Message Code

When sense bytes 22 and 23 contain a symptom code of 3F2X, bits 0-7 contain the time-out message. See the ECI section in the ECM for a reference to the 3F2X messages.

Sense Byte 21 – Storage Director Physical Identifier (SDI)

Sense byte 21 identifies the storage director causing the error.

The physical identifier is read by sensing the switch settings on the device counter (DCT) card when SDI is addressed.

Sense Bytes 22 and 23 – Symptom Code

The symptom code is a number generated from sense data by the storage control.

Format 3—Channel Check 1–Sense Bytes 18-23

Format 3—Channel Check 1–Sense Bytes 18-23 SENSE 160

Format 3 Messages

Note: All messages for format 3 are on this page. These messages include both **Clock Stopped Check 1** and **Channel Check 1** conditions.

Messages 0 through 7

Messages 0 through 7 are not used.

Message 8 – Clock Stopped Check 1

Message 8 indicates a hardware check that includes control storage or the microprocessor and stops the microprocessor clock.

See SENSE 110 for a summary of clock stopped check 1 conditions.

Message 9 – Channel Check 1 Or Storage Director Timeout

Message 9 indicates the microcode detected a channel check 1 error or the storage director is waiting for the channel to respond during communication between the storage director and the channel.

See SENSE 125 for a summary of channel check 1 conditions.

Message A – Storage Director Trace Table Saved

Message A indicates a trace table save operation occurred and uses the disconnect-in sequence to return the machine to normal operation.

Messages B through F

Message B through F are not used.

For 3350 Machines

BYTE	BITS 0	1	2	3	4	5	6	7
0 - 7	Sense Byte Summary (See SENSE 10)							
8 - 17	See the Device Maintenance Library							
18	Channel Select for Bytes 20-23	Channel Select for Bytes 20-23	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
19	See the Device Maintenance Library							
20	Command Overrun			Channel A if Byte 18, bits 0, 1 = 00 Channel C if Byte 18, bits 0, 1 = 10				
21	Service Overrun			Channel A if Byte 18, bits 0, 1 = 00 Channel C if Byte 18, bits 0, 1 = 10				
22	Command Overrun			Channel B if Byte 18, bits 0, 1 = 00 Channel D if Byte 18, bits 0, 1 = 10				
23	Service Overrun			Channel B if Byte 18, bits 0, 1 = 00 Channel D if Byte 18, bits 0, 1 = 10				

Format 6—Usage, Overrun, and Error Statistics SENSE 170

Format 6 – Usage Statistics and Overrun Errors (Cont.)

For 3380 Machines

Byte	BITS 0	1	2	3	4	5	6	7
0 - 7	Sense Byte Summary (See SENSE 10)							
8 - 18	See the Device Maintenance Library							
19	Command Overruns			Channel A if Byte 7, bits 4 - 7 = 1000 Channel B if Byte 7, bits 4 - 7 = 1001 Channel C if Byte 7, bits 4 - 7 = 1010 Channel D if Byte 7, bits 4 - 7 = 1011 Channel E if Byte 7, bits 4 - 7 = 1100 Channel F if Byte 7, bits 4 - 7 = 1101 Channel G if Byte 7, bits 4 - 7 = 1110 Channel H if Byte 7, bits 4 - 7 = 1111				
20	Service Overruns			Channel A if Byte 7, bits 4 - 7 = 1000 Channel B if Byte 7, bits 4 - 7 = 1001 Channel C if Byte 7, bits 4 - 7 = 1010 Channel D if Byte 7, bits 4 - 7 = 1011 Channel E if Byte 7, bits 4 - 7 = 1100 Channel F if Byte 7, bits 4 - 7 = 1101 Channel G if Byte 7, bits 4 - 7 = 1110 Channel H if Byte 7, bits 4 - 7 = 1111				
21	Storage Director Identification (SDI)							
22-23	Not Used							

Format 6 – Usage Statistics and Overrun Errors (Cont.) SENSE 175

Sense Byte 5 – Diskette Checks

Bit 0 – Error Information Stored in 3880

Bit 0 indicates that during the storage director-to-storage director path tests, error information was stored in two bytes of control storage at location X'4295'. The meanings of these bits are:

- Byte 0 – Transmit Test
  - 0 – Path test not entered
  - 1 – Command Valid on permanently
  - 2 – Data Received on after test
  - 3 – Error Alert during test
  - 4 – External Bus In (EBI) parity check
  - 5 – Command Valid timeout
  - 6 – Storage director-to-storage director port fails to open
  - 7 – Did not receive Error Alert
- Byte 1 – Receive Test
  - 0 – Path test not entered
  - 1 – Timeout waiting for Confirm to drop
  - 2 – Data Received on after test
  - 3 – Error Alert on
  - 4 – External Bus In (EBI) parity check
  - 5 – Timeout on Confirm
  - 6 – Data Received not as expected
  - 7 – Undefined.

Bit 1

Bit 1 is not used.

Bits 2 through 4 – Diskette Reader Seek Checks

Bits 2 through 4 indicate the number of recoverable seek errors on the diskette reader.

Bits 5 through 7 – Diskette Reader Data Checks

Bits 5 through 7 indicate the number of recoverable data errors on the diskette reader.

Sense Byte 6 – Storage Director Physical Identifier (SDI)

Sense byte 6 identifies the storage director reporting the error.

The physical identifier is read by sensing the switch settings on the device counter (DCT) card when SDI is addressed.

Sense Byte 7

Sense byte 7 is described on SENSE 35.

3350 Sense Bytes 8 Through 23

Bytes 8 through 17

See the device maintenance library.

Byte 18 – Channel Select

Bits 0 and 1 – Channel Select

When bits 0 and 1 = X'00', the information pertains to channels A or B.

When bits 0 and 1 = X'10', the information pertains to channels C or D.

Bits 2 – 7

Bits 2 through 7 are not used.

Byte 19

See the device maintenance library.

Byte 20 – Command Overrun

Sense byte 20 indicates the count of command overruns tried again by the storage director on channels A or C.

Byte 21 – Service Overrun

Sense byte 21 indicates the count of service overruns tried again by the storage director on channels A or C.

Byte 22 – Command Overrun

Sense byte 22 indicates the count of command overruns tried again by the storage director on channels B or D.

Byte 23 – Service Overrun

Sense byte 23 indicates the count of service overruns tired again by the storage director on channels B or D.

3380 Sense Bytes 8 Through 23

Bytes 8 through 18

See the 3380 maintenance library.

Byte 19 – Command Overrun

Sense byte 19 indicates the count of channels A through H command overruns tried again by the storage director.

Byte 20 – Data Overrun

Sense byte 20 indicates the count of channels A through H data overruns tried again by the storage director.

Byte 21 – Storage Director Physical Identifier (SDI)

Sense byte 21 identifies the storage director reporting the error.

The physical identifier is read by sensing the switch settings on the device counter (DCT) card when SDI is addressed.

Bytes 22 and 23

Bytes 22 and 23 are not used.

3350 Format 6 Messages

Messages 0 through 7

Messages 0 through 7 are not used.

Message 8 – Sense Information is for the 3880

When bit 4 is on in the message, the sense information is for the 3880.

Message 9 through F

Messages 9 through F are not used.

3380 Format 6 Messages

Message 0 through 7

Messages 0 through 7 are not used.

Message 8 – Channel A

Message 8 indicates that the information in sense bytes 19 and 20 is for channel A.

Message 9 – Channel B

Message 9 indicates that the information in sense bytes 19 and 20 is for channel B.

Message A – Channel C

Message A indicates that the information in sense bytes 19 and 20 is for channel C.

Message B – Channel D

Message B indicates that the information in sense bytes 19 and 20 is for channel D.

Message C – Channel E

Message C indicates that the information in sense bytes 19 and 20 is for channel E.

Message D – Channel F

Message D indicates that the information in sense bytes 19 and 20 is for channel F.

Message E – Channel G

Message E indicates that the information in sense bytes 19 and 20 is for channel G.

Message F – Channel H

Message F indicates that the information in sense bytes 19 and 20 is for channel H.

Format F Sense Data For Subsystem Storage

Sense data for the subsystem storage is described starting on this page.

Message Descriptions For Format F

Following are the messages used for sense format F (Sense Byte 7, Bits 4-7).

Message 0 - Operation Terminated

This message is used by the Model 23 only.

This message is generated when the subsystem terminates an operation related to an active channel program as the result of termination of caching because of an error or making the subsystem storage not available to the subsystem using the Set Subsystem Mode command.

Sense data is not generated for any internal operation that is terminated. This message is used only to cause the host to send the request again.

Message 1 - Subsystem Processing Error

This message is used when a logic error is detected in the microcode.

Message 2 - Subsystem Storage Equipment Check

This message is generated when:

- A common check, upper port check, or lower port check is received from the subsystem storage
- A port connection/ADT buffer check is detected.
- A microcode timeout occurs on a subsystem storage operation
- A communication check is received from the communication hardware.

When the message is 2, the contents of bytes 8 through 23 are determined by the error type defined in bits 0-3 of byte 8. Byte 8 also contains an operation type in bits 4-7. The error type and the operation type are described on SENSE 200.

Message 3 - Subsystem Storage Availability Threshold Crossed

This message is used when usable storage is below a reporting boundary.

Message 4 - Subsystem Storage is Unusable

For the Model 21, this message is generated when the storage director terminates a paging mode command chain because there is no subsystem storage space available for caching. Preceding sense data was offloaded for each failure as it occurred.

This message can also be because of preceding failures (device failures, controller failures, a no record found condition, or a not valid track format condition) that caused data to be pinned to the subsystem storage.

For the Model 23, this message is generated when the storage director terminates caching or cannot initialize caching because of a failure.

Equipment Check (byte 0, bit 3) is on.

Message 5 - Subsystem Storage Must Be Initialized

This message is used for Model 21 only.

This message is generated when a paging mode command chain is received and the subsystem storage is not initialized. This can occur:

- When the control unit is IMLed without an associated system IPL
- Following a previously offloaded failure that occurred while accessing the subsystem storage control data. The subsystem storage must be initialized to rebuild and relocate the control data.

Message 6

This message is not used.

Message 7 - Track Format Not Supported For Paging or No Record Found.

This message is used for Model 21 only.

This message is generated when a not valid track format or a no record found condition prevents the completion of a subsystem storage to DASD data transfer.

Message 8 - Storage Director Communication Failed

This message is generated when an attempted communication with the other storage director in the subsystem fails or is not permitted.

Message 9 - Caching Reinitiated

This message is used for Model 23 only.

This message is generated when the storage director automatically establishes the caching function following an error. Another Equipment Check (byte 0, bit 3) defining the failure that caused caching reinitialization will be with this sense message. The message will only be sent if caching had been active before to the failure.

Messages A through F

These messages are not used.

Format F Message Summary

MESSAGE CODE	FORMAT F
0	Operation Terminated
1	Subsystem Processing Error
2	Subsystem Storage Equipment Check
3	Subsystem Storage Availability Threshold Crossed
4	Subsystem Storage is Unusable
5	Subsystem Storage Must Be Initialized
6	Not Used
7	Track Format Not Supported For Paging, or No Record Found
8	Storage Director Communication Failed
9	Caching Reinitiated
A-F	Not Used

Format F Messages

When Format F is indicated for a Model 21 or Model 23, the table below gives a summary of bytes 8 through 23. Messages 0 through 8 are described following this page.

	MODEL 21 AND 23 FORMAT F							
BYTES	MESSAGE 0	MESSAGE 1	MESSAGE 2	MESSAGE 3	MESSAGE 4	MESSAGE 5	MESSAGE 7	MESSAGE 8
8	Operation Terminated (Model 23 only)	Microcode Module ID	When the message is 2, bits 0-3 of byte 8 identify the error type and bits 4-7 identify the operation type. See SENSE 200 for a description of the error and operation types.	Amount of Subsystem Storage Available	Reason Code	Reason Code	Reason Code	Reason Code (Bytes 9-18 in Model 23 not used
9					Bytes 9-11 Not Used in Model 21; Bytes 9-19 Not Used in Model 23	Bytes 9-19 Not Used (This message is used for Model 21 only)	Bytes 9-20 Not Used (This message is used for Model 21 only)	Common Status 1 Register
10		Register 0 - 21* Microcode Module ID - 23*						Common Status 2 Register
11		Register 1 - 21* Internal Reg Grp Address - 23*						Not Used
12		Register 2 - 21* Register 0 - 23*		Amount of Subsystem Storage Offline	Amount of Subsystem Storage Offline			Communication Control Register
13		Register 3 - 21* Register 1 - 23*						Common Status 3 Register
14		Module Location High Reg - 21* Register 2 -23*						Test and Set Register
15		Module Location Low Reg - 21* Register 3 - 23*						Microcode Register
16		Register 6 - 21* Register 4 - 23*		Amount of Subsystem Storage that is pinned (Model 21 only)	Amount of Subsystem Storage that is pinned			Storage Size/ Cables In Register
17		Register 7 - 21* Register 5 - 23*						Byte 17 - Message Activation Record Flags; Byte 18 - Not used
18		Internal Register Group Address - 21* Register 6 - 23*						
19		Bytes 19-20 Not Used - 21* Byte 19 is Reg 7 in Model 23, Byte 20 is not used in Model 23						Storage Director Port In Use
20				Subsystem Storage Size	Subsystem Storage Size	Subsystem Storage ID Register		Subsystem Storage ID in Model 21; Controller ID in Model 23
21	Storage Director Physical Identifier	Storage Director Physical Identifier	Storage Director Physical Identifier	Storage Director Physical Identifier	Storage Director Physical Identifier	Storage Director Physical Identifier	Storage Director Physical Identifier	Storage Director Physical Identifier
22	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code
23	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code	Symptom Code

21* = Model 21 only
23* = Model 23 only

Format F, Messages 0 and 1

Format F – Message 0

This message is not used by the Model 21.

This message is used by the Model 23 only.

This message is generated when the subsystem terminates an operation related to an active channel program as the result of termination of caching because of an error or making the subsystem storage not available to the subsystem using the Set Subsystem Mode command.

Sense data is not generated for any internal operation that is terminated. This message is used only to cause the host to send the request again.

Format F – Message 1 – Subsystem Processing Error

This message is generated when a subsystem processing error that is associated with the subsystem storage is detected.

If the error is associated with the current command chain, equipment check (byte 0, bit 3), permanent error (byte 1, bit 0), and message to operator (byte 1, bit 3) are on.

If the error is not associated with the current command chain, equipment check (byte 0, bit 3), permanent error (byte 1, bit 0), message to operator (byte 1, bit 3), and environmental data present (byte 2, bit 3) are on.

Format F – Message 2 – Subsystem Storage Equipment Check

When the message is 2, the contents of bytes 8 through 23 are determined by the error type and operation type as defined in byte 8. Byte 8 contains the error type in bits 0-3 and an operation type in bits 4-7.

The error types are:

- 0 - Not used
- 1 - Port Connection/control check
- 2 - Upper/lower port check
- 3 - Upper/lower general check
- 4 - Communication/common check
- 5 - Cable not plugged
- 6-E Not used
- F - Microcode detected error.

The operation types are:

- 0 - No operation type
- 1 - Error occurred during a directory read operation on the upper port
- 2 - Error occurred during a directory write operation on the upper port
- 3 - Error occurred during a subsystem storage read operation on the upper port
- 4 - Error occurred during a subsystem storage write operation on the upper port
- 5 - Error occurred during a subsystem storage read operation on the lower port
- 6 - Error occurred during a subsystem storage write operation on the lower port
- 7 - Error occurred on an access control switch test/set operation
- 8 - Error occurred while sending a message to the other storage director
- 9 - Error occurred while receiving a message from the other storage director
- A - Error occurred during a dual port transfer (Model 21 only)
- B - Error occurred during a directory read operation on the lower port
- C - Error occurred during a directory write operation on the lower port
- D - Error occurred during a Manual automatic data transfer (ADT) external register operation
- E - Error occurred during an auxiliary storage director microprocessor operation (ASDM)
- F - Error occurred during an Indirect Register Access

In the Model 21– Format F, Message 2:

is generated when:

- A common check, upper port check, or lower port check is received from the subsystem storage
- A port connection/ADT buffer check is detected
- A microcode timeout occurs on a subsystem storage operation
- A communication check is received from the port communication hardware.

If the failure prevents completion of a command chain, and system retry is not desired, permanent error (byte 1, bit 0) and message to operator (byte 1, bit 3) will also be set on and environmental data present (byte 1, bit 0) will be set off.

In the Model 23–Format F, Message 2:

is generated when an error is detected in the subsystem storage.

If the error is not recovered or bypassed by internal error recovery procedures, equipment check (byte 0, bit 3) will be set on.

If system retry is not desired, permanent error (byte 1, bit 0), message to operator (byte 1, bit 3) will be on and equipment check (byte 0. bit 3) will be off.

If the error was detected by an operation other than the current operation, permanent error (byte 1, bit 0) and environmental data present (byte 2, bit 3) are also set.

If soft-error logging or forced logging mode is in effect and the failure was recovered or bypassed by internal error recovery procedures, environmental data present (byte 2, bit 3) is set; not equipment check (byte 0, bit 3).

Note: Subsystem storage errors are bypassed and reported as soft errors if the error occurs either during asynchronous promotion when the promotion is terminated or during initialization when the directory is relocated.

First error log (byte 2, bit 2) is also set if the failure initiated soft-error logging.

Format F, Message 2 SENSE 200

Format F, Message 2, Error Type 1

When the message is 2 and the error type is 1, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Error Type/Operation Type
	0-3	'0001' Port Connection/Control Check
	4-7	Operation Type (see SENSE 200)
9		Common Status 1 Register:
	0	Upper Port Check
	1	Lower Port Check
	2	Test and Set Obtained
	3	Common Check
	4	Upper Port Operation Complete
	5	Lower Port Operation Complete
	6	Upper Port Data Transfer Complete
	7	Lower Port Data Transfer Complete
10		Common Status 2 Register:
	0	Upper Port Double Bit Correction
	1	Upper Port Single Bit Correction
	2	Lower Port Double Bit Correction
	3	Lower Port Single Bit Correction
	4	Not Used
	5	Microcode Register Bit Active
	6	Not Used
	7	Not Used
11		Common Control Register:
	0-1	Not Used
	2	Controlled Machine Reset
	3	Not Used
	4	Common Check Reset
	5	Cause Device Gap Interrupt
	6-7	Not Used
12		Communication Adapter Check Register:
	0	Communication Adapter IR Check
	1-3	Not Used
	4	CA Duplicate IR Addr Decode Check
	5	Port Control IR Parity Check
	6	Port Control IR Read Parity Check
	7	Storage Director Indicator Check
13		Common Storage Address Check Register:
	0	Test and Set Check
	1	Address Decode Check
	2	Upper Port Buffer IR Check
	3	Not Used
	4	Lower Port Buffer IR Check
	5	ECC IR Check
	6	Storage Adapter IR Check
	7	Storage Control IR Check
14		Multiple IR Address Decode Register:
	0	Upper Port Buffer IR Decoded
	1	Lower Port Buffer IR Decoded
	2	ECC IR Decoded
	3	Storage Adapter IR Decoded
	4	Storage Control IR Decoded
	5	Storage Director IR Decoded
	6-7	Not Used

BYTE	BIT	MEANING
15		Common Port Adapter Check 1 Register:
	0	Port Adapter IR Check
	1	SDM ALU Out Parity Check
	2	Ext Reg Addr or Decode Check
	3	Ext Reg Selection Check
	4	IR Data In/Out Parity Check
	5	Read Clock Delay Check
	6	ALU Out Control Check
	7	Ext Reg Read Parity Check
16		Common Port Adapter Check 2 Register:
	0 - 3	Not Used
	4	Clock Check
	5	CD Duplicate IR Addr Decode Check
	6	Not Used
	7	Range Select Check
17		ADT/ASDM Check Register:
	0	ADT/ASDM IR Check
	1	ASDM LS/Ext Reg Addr Parity Check
	2	ASDM Internal Check
	3	ADT Buffer / ASDM CS In Parity Check
	4	AA Duplicate IR Addr Decode Check
	5	Not Used
	6	ASDM CS Addr Parity Check
	7	CAR Check
18		Common Special Operations Read IR Check
	0	Aux Adapter IR Summary Check
	1	Communication Adapter IR Summary Check
	2	Port Adapter IR Summary Check
	3	Port Control IR Summary Check
	4	Control Board IR Summary Check
	5 - 7	Not Used
19		Storage Director Port in Use:
	0	SD 1 Port
	1	SD 2 Port
20		Subsystem Storage ID
21		Storage Director Identification
22-23		Fault Symptom Code

Notes:
1. Byte 8 contains the error type in bits 0-3 and the operation type in bits 4-7. See SENSE 200 for more information.
2. For a description of the register bits shown on this page see SENSE 206-208.

Format F, Message 2, Error Type 1 Description

Byte 8, Error Type/Operation Type

Byte 8 contains the error type and operation type. When bits 0-3 indicate X'0001' the error type is a port connection/control check. Bits 4-7 are defined on SENSE 200.

Byte 9, Common Status 1 (CSTAT1) Register

Bit 0 – Upper Port Check
Bit 1 – Lower Port Check

Upper or Lower Port Check is a logical OR of all upper or lower error bits. This check inhibits OP Complete and is reset when no checks for the upper or lower port are active (reset). The error stops a fetch or store operation for the upper or lower port if Continue on Error Function is not active.

This error condition also activates Storage Director Check Two condition.

Bit 2 – Test and Set Obtained

Test and Set Obtained indicates that the storage director requested the Test and Set register and the register was obtained.

Bit 3 – Common Check

Common check is the logical OR of the checks associated with the Communication Adapter card, the Storage Adapter card, and the Port Control Connection card.

Bit 4 – Upper Port Operation Complete
Bit 5 – Lower Port Operation Complete

Indicates that either a fetch or a store operation is complete for the upper or lower port.

Bit 6 – Upper Port Data Transfer Complete
Bit 7 – Lower Port Data Transfer Complete

Indicates the status of the last data byte in a data transfer operation. On a store operation, it indicates that the last byte of data has been sent from the ADT buffer to the port buffer. On a fetch operation, it indicates that the last byte of data has been received by the ADT buffer or device interface hardware.

Byte 10, Common Status 2 (CSTAT2) Register

Bit 0 – Upper Port Double Bit Correction
Bit 1 – Upper Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 2 – Lower Port Double Bit Correction
Bit 3 – Lower Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 4

Bit 4 is not used.

Bit 5 – Microcode Reg Bit Active

This bit is an OR of all the bits in microcode register GMIC.

Bits 6 and 7

Bits 6 and 7 are not used.

Byte 11, Common Control (CCTL) Register

Bits 0 and 1

Bits 0 and 1 are not used.

Bit 2 – Controlled Machine Reset (CMR)

This bit causes a diagnostic controlled reset; when executed from SD1, resets hardware in SD1 and all storage controls, and when executed from SD2 resets hardware in SD2 and all storage controls.

Bit 3

Bit 3 is not used.

Bit 4 – Common Check Reset (CCR)

This is a microcode reset used to reset common checks and common registers in either storage director.

Bit 5 – Cause Device Gap Interrupt

This bit permits a level 2 interrupt to occur when the device byte count (from DCT card) decreases to a count of less than 64 bytes.

Bits 6 and 7

Bits 6 and 7 are not used.

Byte 12, Communication Adapter Check (CCOMACK) Register

Bit 0 - Communication Adapter IR Check

The Communication Adapter IR Check bit is used to indicate three conditions:

- IR control check
- IR address bus check
- IR data bus check.

Bits 1 through 3

Bits 1 through 3 are not used.

Bit 4 - CA Duplicate IR Address Decode Check

Bit 4 indicates this card detected the duplicate decodes are not equal.

Bit 5 - Port Control IR Parity Check

Bit 5 indicates that a parity error was detected during a register write operation on the data bus. This bit also indicates that a parity error was detected during a register write/read operation on the address bus entering the CMPC card.

Bit 6 - Port Control IR Read Parity Check

Bit 6 indicates that a parity error was detected on the data bus to the CMPC card from either the CMC1/CMSA cards or the CMPB/CME3 cards.

Bit 7 - Storage Director Indicator Check

Bit 7 indicates that both SD1 and SD2 indicators are active or inactive for this execution.

Format F, Message 2, Error Type 1 Description (Continued)

Byte 13, Common Storage Address Check (CSACK) Register

Bit 0 - Test and Set Check

The Test and Set Obtained bit was active at the same time for both storage directors (CSTAT1, Bit 2)

Bit 1 - Address Decode Check

This bit can indicate three error conditions on the address decode bus:

- No address were decoded
- More than one address was decoded
- The shadow decode is in error.

Bit 2 - Upper Port Buffer IR Check

Bit 2 indicates that an error was detected on the upper port buffer IR register interface.

Bit 3

Bit 3 is not used.

Bit 4 - Lower Port Buffer IR Check

Bit 4 indicates that an error was detected on the lower port buffer IR register interface.

Bit 5 - ECC IR Check

This bit indicates that an error was detected on the ECC IR register interface.

Bit 6 - Storage Adapter IR Check

This bit indicates that an error was detected on the storage adapter IR register interface.

Bit 7 - Storage Control IR Check

This bit indicates that an error was detected on the storage control IR register interface.

Byte 14, Multiple IR Address Decode (CMADEC) Register

This register defines which decodes are active when CSACK bit 1 is active.

Byte 15, Common Port Adapter Check 1 (CPACK1) Register

Bit 0 - Port Adapter IR Check

Bit 0 indicates that a control error has occurred and can be caused by the following:

- IR Control Check

  This check can be be caused by:

  - A missing read/write gate
  - Both read and write gates are active at the same time
  - An address decode check occurred.

- IR Address Bus check

  This check indicates that a parity error occurred while writing to register X'1B' with any addressable register.

- IR Data Bus Check

  This check indicates that a parity error occurred while writing to register X'0F'.

Bit 1 - SDM ALU Out Parity Check

Bit 1 indicates that a parity error was detected on the ALU out bus when writing to the X'1B' and X'0F' registers.

Bit 2 - External Register Address or Decode Check

Bit 2 indicates that a parity error was detected on the five-bit address bus when External Read Select was active.

Bit 3 - External Register Selection Check

Bit 3 indicates that an External Register Select is missing when LD Clock D is active.

Bit 4 - Indirect Register Data Out Bus Check

Bit 4 indicates that an indirect register data out bus error occurred on the CMCD card.

Bit 5 - Read Clock Delay Check

Bit 5 indicates that an read clock delay signal is missing from the other cards. A read clock signal is sent out to the other cards using the IR bus and is returned to the CMCD card on a read operation and verified.

Bit 6 - ALU Out Control Check

Bit 6 indicates that the invert ADT run and the invert channel/device run hardware detected an error.

Bit 7 - External Register Read Parity Check

Bit 7 indicates that a parity error was detected while reading registers RDF (the read register for the X'0F') and CWRBS (the X'1B' shadow).

Format F, Message 2, Error Type 1 Description (Continued)

Byte 16, Common Port Adapter Check 2 (CPACK2) Register

Bits 0 through 3

Bits 0 through 3 are not used.

Bit 4 - Clock Check

This card detected a T Clock error which consists of a T Clock sequence problem.

Bit 5 - CD Duplicate IR Address Decode Check

Bit 5 indicates that this card detected that the duplicate decoders are not equal.

Bit 6

Bit 6 is not used.

Bit 7 - Range Select Check

Bit 7 indicates that the two decoders used to address the ADT buffer are not equal.

Byte 17, ADT/ASDM Check (CAAJCK) Register

These errors set Check Register X'00' bit 7 in the storage director indicating that the ADT buffer or the ASDM has an error. The bits in this byte are:

Bit 0 – ADT/ASDM IR Check

This bit when one indicates that a control error is detected. A control error can be generated from a missing Read gate or when both a Read gate and Write gate are active.

Bit 1 – ASDM LS/Ext Register Address Parity Check

This bit when one indicates a parity error is detected when any ASDM external register (excluding IRG) is read or written by ASDM.

Bit 2 – ASDM Internal Check

This bit when one indicates an error detected by ASDM internal circuits.

Bit 3 – ADT Buffer/ASDM CS In Parity Check

This bit when one indicates a parity error detected on the 'Array In' bus as it enters the ADT buffer or ASDM control store. This check is on the CMAA card.

Bit 4 – AA Duplicate IR Address Decode Check

This bit indicates the two decoders on the IR address bus are not equal.

Bit 5 – Not Used

Bit 6 – ASDM CS Address Parity Check

This bit when one indicates an address parity error was detected when reading or writing control store using ASDM.

Bit 7 – Current Address Register (CAR) Check

This bit when one indicates a parity error is detected on the CAR which addresses the ADT buffer or ASDM control store.

Byte 18, Common Special Operations Read IR Check (CSPRDIC) Register

The write address for this register is X'D9'. This special operation inhibits the X'0F' register's IR data bus. This alternate register is addressed when a Check-2 error is being analyzed. The CSPRDIC register is used because the data that is read from the IR (Indirect Registers) bus could contain an error because of a IR bus malfunction. The CSPRDIC register contents will show that the data is valid or invalid. This register does not need any microcode resets, since the register is always counting the inputs. When the original check is reset at its source register, the CSPRDIC register will also set its bits not active. The CSPRDIC register contents are:

Bit 0 – Auxiliary Adapter IR Summary Check

This bit being a one indicates that one of the following is active:

- CAAJCK register bit 0 – ADT/ASDM IR Check
- CAAJCK register bit 4 – AA Duplicate IR Address Decode Check.

Bit 1 – Communication Adapter IR Summary Check

This bit being a one indicates that one of the following is active:

- CCOMACK register bit 0 – Communication Adapter IR Summary Check
- CCOMACK register bit 4 – CA Duplicate IR Address Decode Check.

Bit 2 – Port Adapter IR Summary Check

This bit being a one indicates that one of the following is active:

- CPACK1 register bit 0 – Port Adapter IR Check
- CPACK1 register bit 5 – Read Clock Delay Check
- CPACK1 register bit 7 – External Register Read Parity Check
- CPACK2 register bit 5 – CD Duplicate IR Address Decode Check.

Bit 3 – Port Control IR Summary Check

This bit being a one indicates that one of the following is active:

- CCOMACK register bit 5 – Port Control IR Parity Check
- CCOMACK register bit 6 – Port Control IR Read Parity Check

Bit 4 – Control Board IR Summary Check

This bit being a one indicates that one of the following is active:

- CSACK register bit 1 – Address Decode Check
- CSACK register bit 2 – Upper Port Buffer IR Check
- CSACK register bit 4 – Lower Port Buffer IR Check
- CSACK register bit 5 – ECC IR Check
- CSACK register bit 6 – Storage Adapter IR Check
- CSACK register bit 7 – Storage Control IR Check
- CCOMACK register bit 4 – CA Duplicate IR Address Decode Check

Bit 5 through 7

Bits 5 through 7 are not used.

Byte 19, Storage Director Port in Use

Bit 0 indicates that storage director port 1 is in use. Bit 1 indicates that storage director port 2 is in use. Bits 2-7 are not used.

Byte 20, Subsystem Storage Identification

Byte 20 contains the subsystem storage identification.

Byte 21, Storage Director Identification

Byte 21 contains the storage director identification.

Bytes 22 through 23

Bytes 22 through 23 contain the fault symptom code.

Format F, Message 2, Error Type 2

When the message is 2 and the error type is 2, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Error Type/Operation Type
	0-3	'0010' Upper/Lower Port Check
	4-7	Operation Type (see SENSE 200)
9		Common Status 1 Register:
	0	Upper Port Check
	1	Lower Port Check
	2	Test and Set Obtained
	3	Common Check
	4	Upper Port Operation Complete
	5	Lower Port Operation Complete
	6	Upper Port Data Transfer Complete
	7	Lower Port Data Transfer Complete
10		Common Status 2 Register:
	0	Upper Port Double Bit Correction
	1	Upper Port Single Bit Correction
	2	Lower Port Double Bit Correction
	3	Lower Port Single Bit Correction
	4	Not Used
	5	Microcode Register Bit Active
	6	Not Used
	7	Not Used
11-13		Failing Subsystem Storage Address bits 0-23
14		Upper or Lower Control Register:
	0	Storage Run
	1	Check Reset
	2	Invert Channel/Device Run
	3	Invert Channel/Device ADT Direction
	4-7	Not Used
15		Upper or Lower Port Adapter Check Reg:
	0	DXR/PA Parity Check
	1	SRC Check
	2	DXR/PA Overrun/Underrun Check
	3	Not Used
	4	Not Used
	5	PA/PB Overrun Check
	6	PA/PB Data In/Out Parity Check
	7	Not Used

BYTE	BIT	MEANING
16		Upper or Lower Port Buffer Check Reg:
	0	PB Overrun/Underrun Check
	1	Byte Count Zero Check
	2	Not Used
	3	Byte Counter Parity Check
	4	Byte Counter Shadow Parity Check
	5	PA/PB Data In Parity Check
	6	ECC/PB Data In Parity Check 1
	7	ECC/PB Data In Parity Check 2
17		Not Used
18		Common Status 4 Register:
	0	Not used
	1	SD1 Indicator
	2	SD2 Indicator
	3	Not used
	4	Timer Overflow
	5	Storage Control Board Power Off
	6	Storage Board 1 Power Off
	7	Storage Board 2 Power Off
19		Storage Director Port in Use:
	0	SD 1 Port
	1	SD 2 Port
	2-7	Not Used
20		Subsystem Storage ID
21		Storage Director Identification
22-23		Fault Symptom Code

Notes:
1. Byte 8 contains the error type in bits 0-3 and the operation type in bits 4-7. See SENSE 200 for more information.
2. For a description of the register bits shown on this page see SENSE 212.

Format F, Message 2, Error Type 2 Description

Byte 8, Error Type/Operation Type

Byte 8 contains the error type and operation type. When bits 0-3 indicate X'0010' the error type is a Upper or Lower Port check. Bits 4-7 are defined on SENSE 200.

Byte 9, Common Status 1 (CSTAT1) Register

Bit 0 – Upper Port Check
Bit 1 – Lower Port Check

Upper or Lower Port Check is a logical OR of all upper or lower error bits. This check inhibits OP Complete and is reset when no checks for the upper or lower port are active (reset). The error stops a fetch or store operation for the upper or lower port if Continue on Error Function is not active.

This error condition also activates Storage Director Check Two condition.

Bit 2 – Test and Set Obtained

Test and Set Obtained indicates that the storage director requested the Test and Set register and the register was obtained.

Bit 3 – Common Check

Common check is the logical OR of the checks associated with the Communication Adapter card, the Storage Adapter card, and the Port Control Connection card.

Bit 4 – Upper Port Operation Complete
Bit 5 – Lower Port Operation Complete

Indicates that either a fetch or a store operation is complete for the upper or lower port.

Bit 6 – Upper Port Data Transfer Complete
Bit 7 – Lower Port Data Transfer Complete

Indicates the status of the last data byte in a data transfer operation. On a store operation, it indicates that the last byte of data has been sent from the ADT buffer to the port buffer. On a fetch operation, it indicates that the last byte of data has been received by the ADT buffer or device interface hardware.

Byte 10, Common Status 2 (CSTAT2) Register

Bit 0 – Upper Port Double Bit Correction
Bit 1 – Upper Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 2 – Lower Port Double Bit Correction
Bit 3 – Lower Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 4

Bit 4 is not used.

Bit 5 – Microcode Reg Bit Active

This bit is an OR of all the bits in microcode register GMIC.

Bits 6 and 7

Bits 6 and 7 are not used.

Bytes 11 through 13

Bytes 11 through 13 contain the failing subsystem storage address in bits 0 through 23.

Byte 14, Upper or Lower Control Register (UCTL/LCTL) Register

The upper control register:

- Starts the fetch or store operation for the upper port (channel)
- Resets all latched check bits for the upper port
- Controls the inverting of bit 7 of the CXR register (channel run) and bit 7 of the SPC register. Correct control of these bits will select the desired data path(s).

The lower control register:

- Starts the fetch or store operation for the lower port (device)
- Resets all latched check bits for the lower port
- Controls the setting of DTG register bit 7 (Device Run) and bit 7 of the Device ADT Run register (shadow register). Correct control of these bits will select the desired data path(s).

Format F, Message 2, Error Type 2 Description (Continued)

Byte 15, Upper or Lower Port Adapter Check (UPACK/LPACK) Register

Bit 0 – DXR/PA Parity Check

When on, this bit indicates that a parity error was detected in the buffer registers (BU1/BL1). They are located between the DXR Channel/Device bus and the port buffers.

Bit 1 – SRC Check

When on, this bit indicates that a cyclic redundancy error was detected on the data from storage.

Bit 2 – DXR/PA Overrun/Underrun Check

When on, this bit indicates that an overrun or underrun condition was detected to or from the channel or device.

Bits 3 and 4

Bits 3 and 4 are not used.

Bit 5 – PA/PB Overrun Check

When on, this bit indicates that a port buffer overrun was detected.

Bit 6 – PA/PB Data In/Out Parity Check

When on, this bit indicates that a parity error was detected between the port adapter function and the port buffer.

Bit 7

Bit 7 is not used.

Byte 16, Upper or Lower Port Buffer Check (UPBCK/LPBCK) Register

Bit 0 – PB Overrun/Underrun Check

When on, this bit indicates that:

- A data byte is attempted to be stored into the port buffer on a store operation and the port buffer is full
- A data byte is attempted to be fetched from the port buffer on a fetch operation and the port buffer is empty.

Bit 1 – Byte Count Zero Check

When on, this bit indicates that the byte count equal zero controls are in error.

Bit 2

Bit 2 is not used.

Bit 3 – Byte Counter Parity Check

When on, this bit indicates that a parity error in the byte counter for either a fetch or a store operation.

Bit 4 – Byte Counter Shadow Parity Check

When on, this bit indicates that a parity error in the byte counter shadow register for either a fetch or a store operation.

Bit 5 – PA/PB Data In Parity Check

When on, this bit indicates that a parity error of the bi-directional bus from the CMCD card to the port buffer (CMPB) card on a store operation.

Bit 6 – ECC/PB Data In Parity Check 1

When on, this bit indicates that a parity error in the port buffer containing the first 128 bytes of data on a fetch operation.

Bit 7 – ECC/PB Data In Parity Check 2

When on, this bit indicates that a parity error in the port buffer containing the second 128 bytes of data on a fetch operation.

Byte 17

Byte 17 is not used.

Byte 18, Common Status 4 Register

Bit 0 is not used

Bit 1 – Storage Director 1 Indicator
Bit 2 – Storage Director 2 Indicator

Bits 1 and 2 indicate to the requestor that this storage director is either storage director 1 or 2.

Bit 3 is not used

Bit 4 – Timer Overflow

When on, this bit indicates that the 57 millisecond timer is full.

Bit 5 – Storage Control Board Power Off

When on, this bit indicates that the power for the storage control board is off.

Bit 6 – Storage Board 1 Power Off

When on, this bit indicates that the power for storage board 1 is off or the cable holding this signal is out.

Bit 7 – Storage Board 2 Power Off

If the Storage Board 1 Power Indicator is on (bit 6 above), bit 7 indicates that the power for storage board 2 is off, the board is not there or the cable holding this signal is out.

If bit 6 above is off, then this bit is on, indicating that Storage Board 2 power is off.

Byte 19, Storage Director Port in Use

Bit 0 indicates that storage director port 1 is in use. Bit 1 indicates that storage director port 2 is in use. Bits 2-7 are not used.

Byte 20, Subsystem Storage Identification

Byte 20 contains the subsystem storage identification.

Byte 21, Storage Director Identification

Byte 21 contains the storage director identification.

Bytes 22 through 23

Bytes 22 through 23 contain the fault symptom code.

Format F, Message 2, Error Type 3

When the message is 2 and the error type is 3, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Error Type/Operation Type
	0-3	'0011' Upper/Lower General Check
	4-7	Operation Type (see SENSE 200)
9		Common Status 1 Register:
	0	Upper Port Check
	1	Lower Port Check
	2	Test and Set Obtained
	3	Common Check
	4	Upper Port Operation Complete
	5	Lower Port Operation Complete
	6	Upper Port Data Transfer Complete
	7	Lower Port Data Transfer Complete
10		Upper and Lower ECC Check Register:
	0	ECC Uncorrectable Check
	1	PB/ECC Data In Check 1
	2	PB/ECC Data In Check 2
	3	ECC Data In or ROS Check E1
	4	ECC Data In or ROS Check E2
	5	ROS-M Check
	6	E1/DD Stg Data Out Parity Check
	7	E2/DD Stg Data Out Parity Check
11-13		Failing Subsystem Storage Address bits 0-23
14		Upper or Lower Storage Adapter Check Register:
	0	SSAR Increment Check
	1	Storage Cycle Check
	2	DA Duplicate Card Sel Decode Check
	3	DA Data Address 6-15 Check
	4	SA/DA Data Address 0-23 Check
	5	Operation Complete Check
	6-7	Not Used
15		Storage Control Check Register:
	0	DD/DR Data 0-35 Parity Check
	1	DD/DR Data 36-71 Parity Check
	2	DR Clock Check 1
	3	DR Clock Check 2
	4-7	Not Used

BYTE	BIT	MEANING
16		Upper/Lower Stor. Card Addr. Check Reg:
	0	Stg Card Addr Check - BCDE
	1	Stg Card Addr Check - FGHJ
	2	Stg Card Addr Check - MNPQ
	3	Stg Card Addr Check - RSTU
	4	AR Card Addr Check - K
	5	AR Card Addr Check - L
	6-7	Not Used
17		Not Used
18		Common Status 4 Register:
	0	Not used
	1	SD1 Indicator
	2	SD2 Indicator
	3	Not used
	4	Timer Overflow
	5	Storage Control Board Power Off
	6	Storage Board 1 Power Off
	7	Storage Board 2 Power Off
19		Storage Director Port in Use:
	0	SD 1 Port
	1	SD 2 Port
	2-7	Not Used
20		Subsystem Storage ID
21		Storage Director Identification
22-23		Fault Symptom Code

Note: Sense bytes 10-16 will contain Upper Port Registers if sense byte 9, bit 0 is a one and Lower Port Registers if sense byte 9, bit 1 is a one.

Notes:
1. Byte 8 contains the error type in bits 0-3 and the operation type in bits 4-7. See SENSE 200 for more information.
2. For a description of the register bits shown on this page see SENSE 217.

Format F, Message 2, Error Type 3 Description

Byte 8, Error Type/Operation Type

Byte 8 contains the error type and operation type. When bits 0-3 indicate X'0011' the error type is a Upper or Lower General check. Bits 4-7 are defined on SENSE 200.

Byte 9, Common Status 1 (CSTAT1) Register

Bit 0 – Upper Port Check
Bit 1 – Lower Port Check

Upper or Lower Port Check is a logical OR of all upper or lower error bits. This check inhibits OP Complete and is reset when no checks for the upper or lower port are active (reset). The error stops a fetch or store operation for the upper or lower port if Continue on Error Function is not active.

This error condition also activates Storage Director Check Two condition.

Bit 2 – Test and Set Obtained

Test and Set Obtained indicates that the storage director requested the Test and Set register and the register was obtained.

Bit 3 – Common Check

Common check is the logical OR of the checks associated with the Communication Adapter card, the Storage Adapter card, and the Port Control Connection card.

Bit 4 – Upper Port Operation Complete
Bit 5 – Lower Port Operation Complete

Indicates that either a fetch or a store operation is complete for the upper or lower port.

Bit 6 – Upper Port Data Transfer Complete
Bit 7 – Lower Port Data Transfer Complete

Indicates the status of the last data byte in a data transfer operation. On a store operation, it indicates that the last byte of data has been sent from the ADT buffer to the port buffer. On a fetch operation, it indicates that the last byte of data has been received by the ADT buffer or device interface hardware.

Byte 10, Upper and Lower ECC Check (UECCCK/LECCCK) Register

The ECC check registers indicate internal ECC circuit errors and incoming or outgoing data errors.

Bytes 11 through 13

Bytes 11 through 13 contain the failing subsystem storage address in bits 0 through 23.

Byte 14, Upper or Lower Storage Adapter Check (USADPCK/USADPCK) Register

The storage adapter check indicates the following:

- A parity error occurred while increasing the value of the contents of SSAR. (There are three incrementer predict parity checkers and three parity checkers on the address bus to the incrementer).
- That the card select decoder and the duplicate decoder are different in value.
- That a parity error was detected on the address bus that leaves the CMDA card on a data fetch or store operation.
- That a parity error was detected while sending the address from the CMSA card to the CMDA card.

Byte 15, Upper or Lower Storage Control Check (USCCK/LSCCK) Register

The storage control check register indicates parity errors on the data bus. Also, it indicates clock checks on the CMDR card on the storage board.

Byte 16, Upper or Lower Storage Card Address Check (USCACK/LSCACK) Register

The storage card address check indicates that:

- An address parity error occurred during R/W select
- An address parity error occurred on the 10 bit bus for Array SAR 0-2 bits or word SAR 0-6 bits while performing a data operation.

Byte 17

Byte 17 is not used.

Byte 18, Common Status 4 Register

Bit 0 is not used

Bit 1 – Storage Director 1 Indicator
Bit 2 – Storage Director 2 Indicator

Bits 1 and 2 indicate to the requestor that this storage director is either storage director 1 or 2.

Bit 3 is not used

Bit 4 – Timer Overflow

When on, this bit indicates that the 57 millisecond timer is full.

Bit 5 – Storage Control Board Power Off

When on, this bit indicates that the power for the storage control board is off.

Bit 6 – Storage Board 1 Power Off

When on, this bit indicates that the power for storage control board 1 is on and power to storage board 1 is off or the cable holding this signal is out.

Bit 7 – Storage Board 2 Power Off

When on, this bit indicates that storage board 1 power is on and power for storage board 2 is off, or the cable holding this signal is out.

Byte 19, Storage Director Port in Use

Bit 0 indicates that storage director port 1 is in use. Bit 1 indicates that storage director port 2 is in use. Bits 2-7 are not used.

Byte 20, Subsystem Storage Identification

Byte 20 contains the subsystem storage identification.

Byte 21, Storage Director Identification

Byte 21 contains the storage director identification.

Bytes 22 through 23

Bytes 22 through 23 contain the fault symptom code.

Format F, Message 2, Error Type 4

When the message is 2 and the error type is 4, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Error Type/Operation Type
	0-3	'0100' Communication/Common check
	4-7	Operation Type (see SENSE 200)
9		Common Status 1 Register:
	0	Upper Port Check
	1	Lower Port Check
	2	Test and Set Obtained
	3	Common Check
	4	Upper Port Operation Complete
	5	Lower Port Operation Complete
	6	Upper Port Data Transfer Complete
	7	Lower Port Data Transfer Complete
10		Common Status 2 Register:
	0	Upper Port Double Bit Correction
	1	Upper Port Single Bit Correction
	2	Lower Port Double Bit Correction
	3	Lower Port Single Bit Correction
	4	Not Used
	5	Microcode Register Bit Active
	6	Not Used
	7	Not Used
11		
	0-7	This byte is not used.
12 (see note 3)		Communication Control Register
	* 0	Communication Request
	* 1	Communication Check Reset
	2-7	Not Used
13 (see note 3)		Common Status 3 Register
	* 0	Message Waiting
	* 1	Message Waiting Echo Back to Sender
	* 2	Request Honored
	3	Active Inhibit Storage Director Reset
	* 4	Communication Check
	5	Port Adapter/Control Cables Out
	6	Communication Cable Out
	7	Other Storage Director Power Off
14		Common Storage Control Check Register
	0	SC Clock Check
	1	SC Select Check
	2-7	Not Used
15		Common Storage Card Refresh Address Check Register
	0	Stg Card Ref Addr Ck - BCHJ
	1	Stg Card Ref Addr Ck - DEFG
	2	Stg Card Ref Addr Ck - MNTU
	3	Stg Card Ref Addr Ck - PQRS
	4	AR Card Ref Addr Ck - K
	5	AR Card Ref Addr Ck - L
	6	Stg Board 1 Ref Active
	7	Stg Board 2 Ref Active
16		Common Storage Address Refresh Check Register:
	0-5	Not Used
	6	Ref Address Increment Ck
	7	DA Ref Address Check

BYTE	BIT	MEANING
17		Communication Adapter Check Register:
	0	Communication Adapter IR Check
	1-3	Not Used
	4	CA Duplicate IR Addr Decode Check
	5	Port Control IR Parity Check
	6	Port Control IR Read Parity Check
	7	Storage Director Indicator Check
18		Common Storage Address Check Register:
	0	Test and Set Check
	1	Address Decode Check
	2	Upper Port Buffer IR Check
	3	Not Used
	4	Lower Port Buffer IR Check
	5	ECC IR Check
	6	Storage Adapter IR Check
	7	Storage Control IR Check
19		Storage Director Port in Use
	0	SD 1 Port
	1	SD 2 Port
	2-7	Not Used
20		Subsystem Storage ID
21		Storage Director Identification
22-23		Fault Symptom Code

Notes:
1. Byte 8 contains the error type in bits 0-3 and the operation type in bits 4-7. See SENSE 200 for more information.
2. For a description of the register bits shown on this page see SENSE 222-223.
3. Since the subsystem communication link is not used in the Model 23, bytes 12 and 13, bits 0-2 and 4 are zero.

Format F, Message 2, Error Type 4 Description

Byte 8, Error Type/Operation Type

Byte 8 contains the error type and operation type. When bits 0-3 indicate X'0100' the error type is a Communication or Common check. Bits 4-7 are defined on SENSE 200.

Byte 9, Common Status 1 (CSTAT1) Register

Bit 0 – Upper Port Check
Bit 1 – Lower Port Check

Upper or Lower Port Check is a logical OR of all upper or lower error bits. This check inhibits OP Complete and is reset when no checks for the upper or lower port are active (reset). The error stops a fetch or store operation for the upper or lower port if Continue on Error Function is not active.

This error condition also activates Storage Director Check Two condition.

Bit 2 – Test and Set Obtained

Test and Set Obtained indicates that the storage director requested the Test and Set register and the register was obtained.

Bit 3 – Common Check

Common check is the logical OR of the checks associated with the Communication Adapter card, the Storage Adapter card, and the Port Control Connection card.

Bit 4 – Upper Port Operation Complete
Bit 5 – Lower Port Operation Complete

Indicates that either a fetch or a store operation is complete for the upper or lower port.

Bit 6 – Upper Port Data Transfer Complete
Bit 7 – Lower Port Data Transfer Complete

Indicates the status of the last data byte in a data transfer operation. On a store operation, it indicates that the last byte of data has been sent from the ADT buffer to the port buffer. On a fetch operation, it indicates that the last byte of data has been received by the ADT buffer or device interface hardware.

Byte 10, Common Status 2 (CSTAT2) Register

Bit 0 – Upper Port Double Bit Correction
Bit 1 – Lower Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 2 – Upper Port Double Bit Correction
Bit 3 – Lower Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 4

Bit 4 is not used.

Bit 5 – Microcode Register Bit Active

This bit is an OR of all the bits in microcode register GMIC.

Bits 6 and 7

Bits 6 and 7 are not used.

Byte 11

This byte is not used.

Byte 12, Communication Control (CCOMCTL) Register

Bit 0 – Communication Request

Communication request sets a request for service to change, read or write the communication buffer. If the request has been done, Request Honored will be set (CSTAT3 bit 2). Resetting the request will reset Request Honored.

Bit 1 – Communication Check Reset

This bit being a one causes a communication reset (CR) for any errors that cause a communication check to be set (CSTAT3 bit 4).

Bits 2 through 7

Bits 2 through 7 are not used.

Byte 13, Common Status 3 (CSTAT3) Register

Bit 0 – Message Waiting

Indicates a message transmitted by the other storage director is in the communication buffer waiting to be processed.

Bit 1 – Message Waiting Echo Back to Sender

Indicates that the message waiting bit sent to the other SD, has been set in the other storage director's register (CSTAT3 Bit 0).

Bit 2 – Request Honored

Indicates that the request has been honored for this storage director and that the bidirectional communication bus is available to this storage director.

Bit 3 – Active Inhibit Storage Director Reset

Indicates that Inhibit SD Reset is active because of Special Operations Set Inhibit SD Reset. This status becomes not active when the 57 Millisecond Timer overflows the second time (57-114 millisecond) or when a Special Operations Reset Inhibit occurs.

Bit 4 – Communication Check

Indicates that one of the following errors has been detected:

- A parity error in the communication address register during a read or write operation
- A parity error on the input bus to the communication buffer during a write operation
- A parity error on the output bus of the communication buffer during a read operation to the communication buffer
- A control sequence error during a write/read operation to the communication buffer
- Both SD1 and SD2 Request Honored are active.

Bit 5 – Port Adapter/Control Cables Out

Indicates that a cable(s) between the storage director board and the storage control board is not seated.

Bit 6 – Communication Cable Out

Indicates that a cable(s) between SD1 and SD2 is not seated.

Bit 7 – Other Storage Director Power Off

Indicates that the other storage director's power is off.

Byte 14, Common Storage Control Check (CSCCK) Register

This register indicates that an error has been detected in the oscillator circuitry or that more than one port has been selected (SD1 upper/SD1 lower/ SD2 upper/SD2 lower) on a storage cycle.

Byte 15, Common Storage Card Refresh Address Check (CSCRACK) Register

The Storage Card Refresh Address Check register indicates:

- An address parity error was detected by a storage card during Refresh Select
- Whether storage board 1 or storage board 2 is Refreshed Selected when any of the 0-5 bits of the Storage Card Refresh Address Check registers (CSCRACK) are active.

Format F, Message 2, Error Type 4 Description (Continued)

Byte 16, Common Storage Address Refresh Check (CSARCK) Register

This register indicates the following:

- That an error was detected in the parity predictor across the refresh address incrementer as well as the output of the refresh register
- That a parity error was detected for the parity of word SAR while the refresh cycle was operating.

Byte 17, Communication Adapter Check (CCOMACK) Register

Bit 0 - Communication Adapter IR Check

The Communication Adapter IR Check bit is used to indicate three conditions:

- IR control check
- IR address bus check
- IR data bus check.

Bits 1 through 3

Bits 1 through 3 are not used.

Bit 4 - CA Duplicate IR Address Decode Check

Bit 4 indicates this card detected the duplicate decodes are not equal.

Bit 5 - Port Control IR Parity Check

Bit 5 indicates that a parity error was detected during a register write operation on the data bus. This bit also indicates that a parity error was detected during a register write/read operation on the address bus entering the CMPC card.

Bit 6 - Port Control IR Read Parity Check

Bit 6 indicates that a parity error was detected on the data bus to the CMPC card from either the CMC1/CMSA cards or the CMPB/CME3 cards.

Bit 7 - Storage Director Indicator Check

Bit 7 indicates that both SD1 and SD2 indicators are active or not active for this execution.

Byte 18, Common Storage Address Check (CSACK) Register

Bit 0 - Test and Set Check

The Test and Set Obtained bit was active at the same time for both storage directors (CSTAT1, Bit 2)

Bit 1 - Address Decode Check

This bit can indicate three error conditions on the address decode bus:

- No address were decoded
- More than one address was decoded
- The shadow decode is in error.

Bit 2 - Upper Port Buffer IR Check

Bit 2 indicates that an error was detected on the upper port buffer IR register interface.

Bit 3

Bit 3 is not used.

Bit 4 - Lower Port Buffer IR Check

Bit 4 indicates that an error was detected on the lower port buffer IR register interface.

Bit 5 - ECC IR Check

This bit indicates that an error was detected on the ECC IR register interface.

Bit 6 - Storage Adapter IR Check

This bit indicates that an error was detected on the storage adapter IR register interface.

Bit 7 - Storage Control IR Check

This bit indicates that an error was detected on the storage control IR register interface.

Byte 19, Storage Director Port in Use

Bit 0 indicates that storage director port 1 is in use. Bit 1 indicates that storage director port 2 is in use. Bits 2-7 are not used.

Byte 20, Subsystem Storage Identification

Byte 20 contains the subsystem storage identification.

Byte 21, Storage Director Identification

Byte 21 contains the storage director identification.

Bytes 22 through 23

Bytes 22 through 23 contain the fault symptom code.

Format F, Message 2, Error Type 5

When the message is 2 and the error type is 5, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Error Type/Operation Type
	0-3	'0101' Cable Not Plugged
	4-7	Operation Type (see SENSE 200)
9		Common Status 1 Register:
	0	Upper Port Check
	1	Lower Port Check
	2	Test and Set Obtained
	3	Common Check
	4	Upper Port Operation Complete
	5	Lower Port Operation Complete
	6	Upper Port Data Transfer Complete
	7	Lower Port Data Transfer Complete
10		Common Status 2 Register:
	0	Upper Port Double Bit Correction
	1	Upper Port Single Bit Correction
	2	Lower Port Double Bit Correction
	3	Lower Port Single Bit Correction
	4	Not Used
	5	Microcode Register Bit Active
	6	Not Used
	7	Not Used
11		Common Status 3 Register:
	0	Message Waiting
	1	Message Waiting Echo Back to Sender
	2	Request Honored
	3	Active Inhibit Storage Director Reset
	4	Communication Check
	5	Port Adapter/Control Cables Out
	6	Communication Cable Out
	7	Other Storage Director Power Off
12		Storage Size / Cables Out Register:
	0	Storage Board 1 Cables Out
	1	Storage Board 2 Cables Out
	2	SD1 Diagnostic Mode
	3	SD2 Diagnostic Mode
	4	64M byte Switch
	5	32M byte Switch
	6	16M byte Switch
	7	8M byte Switch
13-18		Not Used
19		Storage Director Port in Use:
	0	SD1 Port
	1	SD2 Port
	2-7	Not Used
20		Subsystem Storage Identification
21		Storage Director Identification
22-23		Fault Symptom Code

Notes:
1. Byte 8 contains the error type in bits 0-3 and the operation type in bits 4-7. See SENSE 200 for more information.
2. For a description of the register bits shown on this page see SENSE 227.

Format F, Message 2, Error Type 5 Description

Byte 8, Error Type/Operation Type

Byte 8 contains the error type and operation type. When bits 0-3 indicate X'0101' the error type is a cable not plugged check. Bits 4-7 are defined on SENSE 200.

Byte 9, Common Status 1 (CSTAT1) Register

Bit 0 – Upper Port Check
Bit 1 – Lower Port Check

Upper or Lower Port Check is a logical OR of all upper or lower error bits. This check inhibits OP Complete and is reset when no checks for the upper or lower port are active (reset). The error stops a fetch or store operation for the upper or lower port if Continue on Error Function is not active.

This error condition also activates Storage Director Check Two condition.

Bit 2 – Test and Set Obtained

Test and Set Obtained indicates that the storage director requested the Test and Set register and the register was obtained.

Bit 3 – Common Check

Common check is the logical OR of the checks associated with the Communication Adapter card, the Storage Adapter card, and the Port Control Connection card.

Bit 4 – Upper Port Operation Complete
Bit 5 – Lower Port Operation Complete

Indicates that either a fetch or a store operation is complete for the upper or lower port.

Bit 6 – Upper Port Data Transfer Complete
Bit 7 – Lower Port Data Transfer Complete

Indicates the status of the last data byte in a data transfer operation. On a store operation, it indicates that the last byte of data has been sent from the ADT buffer to the port buffer. On a fetch operation, it indicates that the last byte of data has been received by the ADT buffer or device interface hardware.

Byte 10, Common Status 2 (CSTAT2) Register

Bit 0 – Upper Port Double Bit Correction
Bit 1 – Upper Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 2 – Lower Port Single Bit Correction
Bit 3 – Lower Port Double Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 4

Bit 4 is not used.

Bit 5 – Microcode Register Bit Active

This bit is an OR of all the bits in microcode register GMIC.

Bits 6 and 7

Bits 6 and 7 are not used.

Byte 11, Common Status 3 (CSTAT3) Register

Bit 0 – Message Waiting

Indicates a message transmitted by the other storage director is in the communication buffer waiting to be processed.

Bit 1 – Message Waiting Echo Back to Sender

Indicates that the message waiting bit sent to the other SD, has been set in the other storage director's register (CSTAT3 Bit 0).

Bit 2 – Request Honored

Indicates that the request has been honored for this storage director and that the bidirectional communication bus is available to this storage director.

Bit 3 – Active Inhibit Storage Director Reset

Indicates that Inhibit SD Reset is active because of Special Operations Set Inhibit SD Reset. This status becomes not active when the 57 Millisecond Timer overflows the second time (57-114 millisecond) or when a Special Operations Reset Inhibit occurs.

Bit 4 – Communication Check

Indicates that one of the following errors has been detected:

- A parity error in the communication address register during a read or write operation
- A parity error on the input bus to the communication buffer during a write operation
- A parity error on the output bus of the communication buffer during a read operation to the communication buffer
- A control sequence error during a write/read operation to the communication buffer
- Both SD1 and SD2 Request Honored are active.

Bit 5 – Port Adapter/Control Cables Out

Indicates that a cable(s) between the storage director board and the storage control board is not seated.

Bit 6 – Communication Cable Out

Indicates that a cable(s) between SD1 and SD2 is not seated.

Bit 7 – Other Storage Director Power Off

Indicates that the other storage director's power is off.

Byte 12, Storage Size/Cables Out (GSSCIN) Register

Bits 0 and 1 – Cables Out

Bits 0 and 1 indicate which cable(s) is not seated.

Note: If storage board 2 is not present, bit 1 will be on.

Bits 2 and 3 – SD1 and SD2 Diagnostic Mode

Bits 2 and 3 indicate which storage director(s) is in diagnostic mode.

Bits 4 through 7 – Storage Size Switches

These bits mirror the setting of the switches that indicate the storage size installed in the machine, either 8M, 16M, 32M, 48M, or 64M bytes.

Bytes 13 through 18

Bytes 13 through 18 are not used.

Byte 19, Storage Director Port in Use

Bit 0 indicates that storage director port 1 is in use. Bit 1 indicates that storage director port 2 is in use. Bits 2-7 are not used.

Byte 20, Subsystem Storage Identification

Byte 20 contains the subsystem storage identification.

Byte 21, Storage Director Identification

Byte 21 contains the storage director identification.

Bytes 22 through 23

Bytes 22 through 23 contain the fault symptom code.

Format F, Message 2, Error Type F

When the message is 2 and the error type is F, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Error Type/Operation Type
	0-3	'1111' Microcode Detected Error
	4-7	Operation Type (see SENSE 200)
9		Common Status 1 Register:
	0	Upper Port Check
	1	Lower Port Check
	2	Test and Set Obtained
	3	Common Check
	4	Upper Port Operation Complete
	5	Lower Port Operation Complete
	6	Upper Port Data Transfer Complete
	7	Lower Port Data Transfer Complete
10		Common Status 2 Register:
	0	Upper Port Double Bit Correction
	1	Upper Port Single Bit Correction
	2	Lower Port Double Bit Correction
	3	Lower Port Single Bit Correction
	4	Not Used
	5	Microcode Register Bit Active
	6	Not Used
	7	Not Used
11		Common Status 3 Register:
	0	Message Waiting
	1	Message Waiting Echo Back to Sender
	2	Request Honored
	3	Active Inhibit Storage Director Reset
	4	Communication Check
	5	Port Adapter/Control Cables Out
	6	Communication Cable Out
	7	Other Storage Director Power Off
12		Storage Size / Cables Out Register:
	0	Storage Board 1 Cables Out
	1	Storage Board 2 Cables Out
	2	SD1 Diagnostic Mode
	3	SD2 Diagnostic Mode
	4	64M byte Switch
	5	32M byte Switch
	6	16M byte Switch
	7	8M byte Switch
13		Not Used
14		Upper and Lower Op/Ctl Register:
	0	0 = Fetch, 1 = Store
	1	Inhibit SSAR Increment
	2	0 = Manual, 1 = Auto
	3	Not Used
	4	Inhibit SRC
	5	Accumulate SRC
	6-7	Not Used

BYTE	BIT	MEANING
15		Upper/Lower Control Register:
	0	Storage Run
	1	Check Reset
	2	Invert Channel/Device Run
	3	Invert Channel/Device ADT Direction
	4-7	Not Used
16		Common Control Register:
	0-1	Not Used
	2	Controlled Machine Reset
	3	Not Used
	4	Common Check Reset
	5	Cause Device Gap Interrupt
	6-7	Not Used
17		Test and Set Register:
	0	Test and Set Being Used
	1	SD1 Ownership
	2	SD2 Ownership
	3-7	Test and Set Bits 3-7
18		Common Status 4 Register
	0	Not used
	1	SD1 Indicator
	2	SD2 Indicator
	3	Not used
	4	Timer Overflow
	5	Storage Control Board Power Off
	6	Storage Board 1 Power Off
	7	Storage Board 2 Power Off
19		Storage Director Port in Use:
	0	SD 1 Port
	1	SD 2 Port
20		Subsystem Storage ID
21		Storage Director Identification
22-23		Fault Symptom Code

Notes:
1. Byte 8 contains the error type in bits 0-3 and the operation type in bits 4-7. See SENSE 200 for more information.
2. For a description of the register bits shown on this page see SENSE 232-233.

Format F, Message 2, Error Type F Description

Byte 8, Error Type/Operation Type

Byte 8 contains the error type and operation type. When bits 0-3 indicate X'1111' the error type is a microcode detected error. Bits 4-7 are defined on SENSE 200.

Byte 9, Common Status 1 (CSTAT1) Register

Bit 0 – Upper Port Check
Bit 1 – Lower Port Check

Upper or Lower Port Check is a logical OR of all upper or lower error bits. This check inhibits OP Complete and is reset when no checks for the upper or lower port are active (reset). The error stops a fetch or store operation for the upper or lower port if Continue on Error Function is not active.

This error condition also activates Storage Director Check Two condition.

Bit 2 – Test and Set Obtained

Test and Set Obtained indicates that the storage director requested the Test and Set register and the register was obtained.

Bit 3 – Common Check

Common check is the logical OR of the checks associated with the Communication Adapter card, the Storage Adapter card, and the Port Control Connection card.

Bit 4 – Upper Port Operation Complete
Bit 5 – Lower Port Operation Complete

Indicates that either a fetch or a store operation is complete for the upper or lower port.

Bit 6 – Upper Port Data Transfer Complete
Bit 7 – Lower Port Data Transfer Complete

Indicates the status of the last data byte in a data transfer operation. On a store operation, it indicates that the last byte of data has been sent from the ADT buffer to the port buffer. On a fetch operation, it indicates that the last byte of data has been received by the ADT buffer or device interface hardware.

Byte 10, Common Status 2 (CSTAT2) Register

Bit 0 – Upper Port Double Bit Correction
Bit 1 – Upper Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 2 – Lower Port Double Bit Correction
Bit 3 – Lower Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 4

Bit 4 is not used.

Bit 5 – Microcode Register Bit Active

This bit is an OR of all the bits in microcode register GMIC.

Bits 6 and 7

Bits 6 and 7 are not used.

Byte 11, Common Status 3 (CSTAT3) Register

Bit 0 – Message Waiting

Indicates a message transmitted by the other storage director is in the communication buffer waiting to be processed.

Bit 1 – Message Waiting Echo Back to Sender

Indicates that the message waiting bit sent to the other SD, has been set in the other storage director's register (CSTAT3 bit 0).

Bit 2 – Request Honored

Indicates that the request has been honored for this storage director and that the bidirectional communication bus is available to this storage director.

Bit 3 – Active Inhibit Storage Director Reset

Indicates that Inhibit SD Reset is active because of Special Operations Set Inhibit SD Reset. This status becomes not active when the 57 Millisecond Timer overflows the second time (57-114 millisecond) or when a Special Operations Reset Inhibit occurs.

Bit 4 – Communication Check

Indicates that one of the following errors has been detected:

- A parity error in the communication address register during a read or write operation
- A parity error on the input bus to the communication buffer during a write operation
- A parity error on the output bus of the communication buffer during a read operation to the communication buffer

- A control sequence error during a write/read operation to the communication buffer
- Both SD1 and SD2 Request Honored are active.

Bit 5 – Port Adapter/Control Cables Out

Indicates that a cable(s) between the storage director board and the storage control board is not seated.

Bit 6 – Communication Cable Out

Indicates that a cable(s) between SD1 and SD2 is not seated.

Bit 7 – Other Storage Director Power Off

Indicates that the other storage director's power is off.

Byte 12, Storage Size/Cables Out (GSSCIN) Register

Bits 0 and 1 – Cables Out

Bits 0 and 1 indicate which cable(s) is not seated.

Note: If storage board 2 is not present, bit 1 will be on.

Bits 2 and 3 – SD1 and SD2 Diagnostic Mode

Bits 2 and 3 indicate which storage director(s) is in diagnostic mode.

Bits 4 through 7 – Storage Size Switches

These bits mirror the setting of the switches that indicate the storage size installed in the machine, either 8M, 16M, 32M, 48M, or 64M bytes.

Byte 13

Byte 13 is not used.

Byte 14, Upper and Lower OP/CTL (UOPCTL/LOPCTL) Register

The OP/CTL register controls:

- The data operation (fetch/store), which transfers data between the subsystem storage and the ADT buffer, device, or channel. The upper port registers are used with channel data operations and the lower port registers are used with device data operations.
- In manual store mode, controls the flow of data between storage and either the ADT buffer or the ASDM control storage. In automatic storage mode, controls the flow of data between the storage and either the channel or the device.
- The disabling of the storage CRC (SRC) function and inhibits the fetching/storing of SRC characters from or to storage.
- The inhibiting of the checking of the SRC bytes from storage.
- Can use the SRC bytes that are kept from several fetch or store operations.

Format F, Message 2, Error Type F Description (Continued)

Byte 15, Upper and Lower Control (UCTL) Register

The upper control register:

- Starts the fetch or store operation for the upper port (channel).
- Resets all latched check bits for the upper port.
- Controls the inverting of bit 7 of the CXR register (channel run) and bit 7 of the SPC register. Correct control of these bits will select the desired data path(s).

The lower control register:

- Starts the fetch or store operation for the lower port (device)
- Resets all latched check bits for the lower port
- Controls the setting of DTG register bit 7 (Device Run) and bit 7 of the Device ADT Run register (shadow register). Correct control of these bits will select the desired data path(s).

Byte 16, Common Control (CCTL) Register

Bits 0 through 1

Bits 0 through 1 are not used.

Bit 2 – Controlled Machine Reset (CMR)

This bit causes a diagnostic controlled reset; when executed from SD1, resets hardware in SD1 and all storage controls, and when executed from SD2 resets hardware in SD2 and all storage controls.

Bit 3

Bit 3 is not used.

Bit 4 – Common Check Reset (CCR)

This is a microcode reset used to reset common checks and common registers in either storage director.

Bit 5 – Cause Device Gap Interrupt

This bit permits a level 2 interrupt to occur when the device byte count (from DCT card) decreases to a count of less than 64 bytes.

Bits 6 and 7

Bits 6 and 7 are not used.

Byte 17, Test and Set (GTS) Register

Both storage directors use the Test and Set register for synchronizing purposes. The GTS register is eight bits in length. Storage director 1 has priority in the use of the Test and Set register.

- Bit 0 – Test and Set being used
- Bit 1 – SD1 ownership
- Bit 2 – SD2 ownership
- Bits 3-7 – Test and set bits

Byte 18, Common Status 4 Register

Bit 0 is not used

Bit 1 – Storage Director 1 Indicator
Bit 2 – Storage Director 2 Indicator

Bits 1 and 2 indicate to the requestor that this storage director is either storage director 1 or 2.

Bit 3 is not used

Bit 4 – Timer Overflow

When on, this bit indicates that the 57 millisecond timer is full.

Bit 5 – Storage Control Board Power Off

When on, this bit indicates that the power for the storage control board is off.

Bit 6 – Storage Board 1 Power Off

When on, this bit indicates that the power for storage control board 1 is on and power to storage board 1 is off or the cable holding this signal is out.

Bit 7 – Storage Board 2 Power Off

When on, this bit indicates that storage board 1 power is on and power for storage board 2 is off, or the cable holding this signal is out.

Byte 19, Storage Director Port in Use

Bit 0 indicates that storage director port 1 is in use. Bit 1 indicates that storage director port 2 is in use. Bits 2-7 are not used.

Byte 20, Subsystem Storage Identification

Byte 20 contains the subsystem storage identification.

Byte 21, Storage Director Identification

Byte 21 contains the storage director identification.

Bytes 22 through 23

Bytes 22 through 23 contain the fault symptom code.

Format F, Message 2, Error Type F (Cont.) SENSE 233

Format F, Message 3 SENSE 235

Bytes 8 through 23 – Message 3 – Subsystem Storage Availability Threshold Crossed

This message is generated when the amount of space available for caching is decreased and crosses one of the reporting boundaries. Message to operator (byte 1, bit 3) and environmental data present (byte 2, bit 3) are also on.

When the message is 3, bytes 8-23 are formatted as follows:

BYTE	MEANING
8-11	Available Subsystem Storage (bytes)
12-15	Off-line Subsystem Storage (bytes)
16-19	In Model 21 - Pinned Subsystem Storage Capacity in bytes; In Model 23 - not used
20	Subsystem Storage Size (times 8M bytes) *
21	Storage Director Identification
22-23	Fault Symptom Code

* Note: If subsystem storage size has not been determined, byte 20 equals 'FF'.

Bytes 8 through 23 – Message 4 – Subsystem Storage Is Unusable – Model 21

This message is generated when the storage director terminates a paging mode command chain because there is no subsystem storage space available for caching. Previous sense data was off-loaded for each failure as it occurred.

This message can also be because of previous failures (device failures, controller failures, a no record found condition, or a not valid track format condition) that caused data to be pinned (bound) to the subsystem storage.

Equipment check (byte 0, bit 3) and message to operator (byte 1, bit 3) are also on.

When the message is 4, bytes 8-23 are formatted as follows:

BYTE	MEANING
8	Reason Code *
9-11	Not Used
12-15	Off-line Subsystem Storage (bytes)
16-19	Pinned (bound) Subsystem Storage (bytes)
20	Subsystem Storage Size (times 8M bytes) **
21	Storage Director Identification
22-23	Fault Symptom Code
Note: Sense bytes 12-19 will contain hex 'F's if sub-system storage is not available to the storage director	

* Reason Code: Byte 8, bits 4 - 7 contain the reason code as follows:

- 0 = No message
- 1 = Data is pinned (bound) because of a device failure
- 2 = Subsystem storage port failure
- 3 = Subsystem storage general failures
- 4 = Set Subsystem Mode command received
- 5 = Subsystem processing error
- 6 = System/Selective Reset while reset protected
- 7 = Subsystem storage is unusable because other storage director has requested initialization
- 8 = Subsystem storage mode switch set to diagnostic mode
- 9 = Data is pinned (bound) because of a device format error
- A = Storage director equipment check
- B = Subsystem storage unusable following IML
- C = Test and Set failure
- D = Diagnostic bit active
- E-F = Not used

Bytes 8 through 23 – Message 4 – Subsystem Storage Is Unusable – Model 23

This message is generated when the storage director terminates caching or cannot initialize caching because of a failure.

Equipment check (byte 0, bit 3) is on.

When the message is 4, bytes 8-23 are formatted as follows:

BYTE	MEANING
8	Reason Code *
9-19	Not Used
20	Subsystem Storage Size (times 8M bytes) **
21	Storage Director Identification
22-23	Fault Symptom Code

* Reason Code: Byte 8, bits 4 - 7 contain the reason code as follows:

- 0 = No message
- 1 = Entering limited caching state
- 2 = Subsystem storage port failure
- 3 = Subsystem storage general failure
- 4 = Caching status miscompare detected
- 5 = Subsystem processing error
- 6 = Other storage director cannot access cache
- 7 = Subsystem storage is unusable because resets received with resets inhibited
- 8 = Subsystem storage mode switch set to diagnostic mode
- 9 = Test and Set register appears locked
- A = Storage Director equipment check
- B = Not used
- C = Not used
- D = Diagnostic bit active
- E-F = Not used

** Notes: For Model 23, byte 8, bit 3: This bit on with any code in bits 4-7 indicates that reinitialization could not be attempted because space in subsystem storage was not available for directory relocation.

If the subsystem storage size has not been determined, byte 20 equals 'FF'.

Note: Messages 5 and 7 are not used by the Model 23.

Bytes 8 through 23 – Message 5 – Subsystem Storage Must Be Initialized – Model 21

This message is generated when the storage director rejects a paging mode request because the storage director has determined that a data loss can have occurred but cannot determine what, if any, of the data stored in the subsystem was lost.

Permanent error (byte 1, bit 0) and message to operator (byte 1, bit 3) are also on.

When the message is 5, bytes 8-23 are formatted as follows:

BYTE	MEANING
8	Reason Code *
9-19	Not Used
20	Subsystem Storage ID Register
21	Storage Director Identification
22-23	Fault Symptom Code

* Reason Code: Byte 8, bits 4-7 contain the reason code as follows:

- 0 = No message
- 1 = Data pinned due to a device failure
- 2 = Subsystem storage port failure
- 3 = Subsystem storage general failures
- 4 = Set Subsystem Mode command received
- 5 = Subsystem processing error
- 6 = System/Selective reset while reset protected
- 7 = Subsystem storage is unusable because other storage director has requested initialization
- 8 = Subsystem storage mode switch set to diagnostic mode
- 9 = Data pinned due to device format error
- A = Storage director equipment check
- B = Subsystem storage unusable following IML
- C = Test and Set failure
- D = Diagnostic bit active
- E-F = Not used

Format F, Messages 5 and 7 For Model 21

Bytes 8 through 23 – Message 7 – Track Format Not Supported for Paging Or No Record Found – Model 21

This message is generated when an invalid track format or a no record found prevents the completion of a subsystem storage to DASD data transfer.

Invalid track format (byte 1, bit 1) or no record found (byte 1, bit 4), message to operator (byte 1, bit 3) and environmental data present (byte 2, bit 3) are also on.

When the message is 7, bytes 8-23 are formatted as follows:

BYTE	MEANING
8	Reason Code *
9-20	Not Used
21	Storage Director Identification
22-23	Fault Symptom Code

* Reason Code: Byte 8, bits 4-7 contain the reason code as follows:

- 0 = No message
- 1 = Invalid Track format error
- 2 = No Record Found error
- 3-F = Not used.

Format F, Messages 5 and 7 For Model 21

Format F, Message 8 For Model 21

Bytes 8 through 23 – Message 8 – Storage Director Communication Failed – Model 21

This message is generated when an attempted communication with the other storage director in the subsystem fails or is not permitted because of the subsystem storage mode switch setting.

If the communication failure occurred while executing a Set Subsystem Mode command; equipment check (byte 0, bit 3), permanent error (byte 1, bit 0), and message to operator (byte 1, bit 3) are also on.

If the communication failure was not associated with the execution of a Set Subsystem Mode command; equipment check (byte 0, bit 3), permanent error (byte 1, bit 0), message to operator (byte 1, bit 3) and environmental data present (byte 2, bit 3) are also on.

When the message is 8, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Reason Code
9		Common Status 1 Register:
	0	Upper Port Check
	1	Lower Port Check
	2	Test and Set Obtained
	3	Common Check
	4	Upper Port Operation Complete
	5	Lower Port Operation Complete
	6	Upper Port Data Transfer Complete
	7	Lower Port Data Transfer Complete
10		Common Status 2 Register:
	0	Upper Port Double Bit Correction
	1	Upper Port Single Bit Correction
	2	Lower Port Double Bit Correction
	3	Lower Port Single Bit Correction
	4	Not Used
	5	Microcode Register Bit Active
	6	Not Used
	7	Not Used
11		Not used
12		Communication Control Register:
	0	Communication Request
	1	Communication Check Reset
	2-7	Not Used
13		Common Status 3 Register:
	0	Message Waiting
	1	Message Waiting Echo Back to Sender
	2	Request Honored
	3	Active Inhibit Storage Director Reset
	4	Communication Check
	5	Port Adapter/Control Cables Out
	6	Communication Cable Out
	7	Other Storage Director Power Off

BYTE	BIT	MEANING
14		Test and Set Register
	0	Test and Set Being Used
	1	SD1 Ownership
	2	SD2 Ownership
	3-7	Test and Set Bits 3-7
15		Microcode Register
	0-7	Microcode Register Bits 0-7
16		Storage Size/ Cables Out Register
	0	Storage Board 1 Cables Out
	1	Storage Board 2 Cables Out
	2	SD1 Diagnostic Mode
	3	SD2 Diagnostic Mode
	4	64 MB Switch
	5	32 MB Switch
	6	16 MB Switch
	7	8 MB Switch
17		Message Activation Record Flags
	0	Primary link unavailable
	1	Response active
	2	Message active
	3	Not used
	4	Message Error
	5	Not used
	6	Not used
	7	Message reset
18		Not used
19		Storage Director Port in Use
	0	SD 1 Port
	1	SD 2 Port
	2-7	Not Used
20		Subsystem Storage ID
21		Storage Director Identification

* Reason Code: Byte 8, bits 4-7 contain the reason code as follows:

- 0 = No message
- 1 = Subsystem storage mode switch set for other storage director
- 2-F = Not used.

Bytes 8 through 23 – Message 8 – Storage Director Communication Failed – Model 23

This message is generated when the other storage director in the subsystem fails to respond to an attempted communication.

If the communication failure occurred while executing a Set Subsystem Mode command to terminate caching for the subsystem, no other error is reported, and equipment check (byte 0, bit 3), permanent error (byte 1, bit 0), and message to operator (byte 1, bit 3) are on.

If the communication failure was detected during any other operation, equipment check (byte 0, bit 3), permanent error (byte 1, bit 0), message to operator (byte 1, bit 3) and environmental data present (byte 2, bit 3) are on.

Note: If a Set Subsystem Mode command request to activate caching fails because of a subsystem storage failure, and that failure was preceded by a communication failure, the Format F, Message 8, sense data will be presented as the cause of the command failing. The sense data will include equipment check (byte 0, bit 3), permanent error (byte 1, bit 0), and message to operator (byte 1, bit 3)

When the message is 8, bytes 8-23 are formatted as follows:

BYTE	BIT	MEANING
8		Reason Code
9-18		Not used
19	0 1 2-7	Storage director port in use SD1 Port SD2 Port Not used
20		Controller Identification
21		Storage Director Identification
22-23		Fault Symptom Code

* Reason Code: Byte 8, bits 4-7 contain the reason code as follows:

- 0 = No message
- 1 = Not used
- 2 = No response from other storage director via dynamic path selection array
- 3 = Dynamic path selection array lock timeout
- 4 = Not used
- 5 = Not used
- 6 = No controller available
- 7-F = Not used.

Note: Byte 20 will be 'FF' if the controller identification is not available.

Format F, Message 8 For Model 23 SENSE 246

Format F, Message 8 Description

Note: For Model 23, bytes 9-18 are not used.

Byte 8, Error Type/Operation Type

Byte 8 contains the reason code.

Byte 9, Common Status 1 (CSTAT1) Register

Bit 0 – Upper Port Check
Bit 1 – Lower Port Check

Upper or Lower Port Check is a logical OR of all upper or lower error bits. This check inhibits OP Complete and is reset when no checks for the upper or lower port are active (reset). The error stops a fetch or store operation for the upper or lower port if Continue on Error Function is not active.

This error condition also activates Storage Director Check Two condition.

Bit 2 – Test and Set Obtained

Test and Set Obtained indicates that the storage director requested the Test and Set register and the register was obtained.

Bit 3 – Common Check

Common check is the logical OR of the checks associated with the Communication Adapter card, the Storage Adapter card, and the Port Control Connection card.

Bit 4 – Upper Port Operation Complete
Bit 5 – Lower Port Operation Complete

Indicates that either a fetch or a store operation is complete for the upper or lower port.

Bit 6 – Upper Port Data Transfer Complete
Bit 7 – Lower Port Data Transfer Complete

Indicates the status of the last data byte in a data transfer operation. On a store operation, it indicates that the last byte of data has been sent from the ADT buffer to the port buffer. On a fetch operation, it indicates that the last byte of data has been received by the ADT buffer or device interface hardware.

Byte 10, Common Status 2 (CSTAT2) Register

Bit 0 – Upper Port Double Bit Correction
Bit 1 – Upper Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 2 – Lower Port Double Bit Correction
Bit 3 – Lower Port Single Bit Correction

During a fetch operation, it indicates that a double or single bit correction occurred and that it can be corrected. This correction does not set a check condition.

Bit 4

Bit 4 is not used.

Bit 5 – Microcode Register Bit Active

This bit is an OR of all the bits in microcode register GMIC.

Bits 6 and 7

Bits 6 and 7 are not used.

Byte 11

This byte is not used.

Byte 12, Communication Control (CCOMCTL) Register

Bit 0 – Communication Request

Communication request sets a request for service to change, read or write the communication buffer. If the request has been done, Request Honored will be set (CSTAT3 bit 2). Resetting the request will reset Request Honored.

Bit 2 – Communication Check Reset

This bit being a one causes a communication reset (CR) for any errors that cause a communication check to be set (CSTAT3 bit 4).

Bits 2 through 7

Bits 2 through 7 are not used.

Byte 13, Common Status 3 (CSTAT3) Register

Bit 0 – Message Waiting

Indicates a message transmitted by the other storage director is in the communication buffer waiting to be processed.

Bit 1 – Message Waiting Echo Back to Sender

Indicates that the message waiting bit sent to the other SD, has been set in the other storage director's register (CSTAT3 Bit 0).

Bit 2 – Request Honored

Indicates that the request has been honored for this storage director and that the bidirectional communication bus is available to this storage director.

Bit 3 – Active Inhibit Storage Director Reset

Indicates that Inhibit SD Reset is active because of Special Operations Set Inhibit SD Reset. This status becomes not active when the 57 Millisecond Timer overflows the second time (57-114 millisecond) or when a Special Operations Reset Inhibit occurs.

Bit 4 – Communication Check

Indicates that one of the following errors has been detected:

- A parity error in the communication address register during a read or write operation
- A parity error on the input bus to the communication buffer during a write operation
- A parity error on the output bus of the communication buffer during a read operation to the communication buffer
- A control sequence error during a write/read operation to the communication buffer
- Both SD1 and SD2 Request Honored are active.

Bit 5 – Port Adapter/Control Cables Out

Indicates that a cable(s) between the storage director board and the storage control board is not seated.

Bit 6 – Communication Cable Out

Indicates that a cable(s) between SD1 and SD2 is not seated.

Bit 7 – Other Storage Director Power Off

Indicates that the other storage director's power is off.

Format F, Message 8 Description (Continued)

Note: For Model 23, bytes 9-18 are not used.

Byte 14, Test and Set (GTS) Register

Both storage directors use the Test and Set register for synchronizing purposes. The GTS register is eight bits in length. Storage director 1 has priority in the use of the Test and Set register.

- Bit 0 – Test and Set being used
- Bit 1 – SD1 ownership
- Bit 2 – SD2 ownership
- Bits 3-7 – Test and set bits.

Byte 15, Microcode (GMIC) Register

This byte is defined and controlled by microcode only. The hardware has no tie-breaking circuits for the register in case either storage director writes to the register at the same time. Therefore, it is possible for a parity error to occur because of a not correct microcode convention or a hardware error. This register is used under the Test and Set ownership. Register bits 0-7 are 'OR'd together and cause status bit 5 of CSTAT2 to go active (Microcode Register Bit Active) when any microcode register bit is active.

Byte 16, Storage Size/Cables Out (GSSCIN) Register

Bits 0 and 1 – Cables Out

Bits 0 and 1 indicate which cable(s) is not seated.

Note: If storage board 2 is not present, bit 1 will be on.

Bits 2 and 3 – SD1 and SD2 Diagnostic Mode

Bits 2 and 3 indicate which storage director(s) is in diagnostic mode.

Bit 4 – Not Used

Bits 5 through 7 – Storage Size Switches

These bits mirror the setting of the switches that indicate the storage size installed in the machine, either 8M, 16M, 32M, 48M, or 64M bytes.

Byte 17, Message Activation Record Flags

Bit 0–Primary Link Unavailable

When this bit is on the primary communication link is not available for storage director communication.

Bit 1–Response Active

When this bit is on a response has been transmitted to the other storage director.

Bit 2–Message Active

When this bit is on a message has been transmitted to the other storage director. The associated response is pending.

Bit 3

Bit 3 is not used.

Bit 4–Message Error Detected

When this bit is on a not valid message has previously been detected.

Bits 5 and 6

Bits 5 and 6 and not used.

Bit 7–Message Reset

When this bit is on a reset occurred while processing a Set Subsystem Mode command.

Byte 18

Byte 18 is not used.

Byte 19, Storage Director Port in Use

Bit 0 indicates that storage director port 1 is in use. Bit 1 indicates that storage director port 2 is in use. Bits 2-7 are not used.

Byte 20, Controller Identification

Byte 20 contains the controller identification.

Byte 21, Storage Director Identification

Byte 21 contains the storage director identification.

Bytes 22 through 23

Bytes 22 through 23 contain the fault symptom code.

Format F, Message 9 SENSE 250

Format F, Message 9 – Caching Reinitiated

This message is generated when the storage director automatically starts the caching function following an error. Another Equipment Check (byte 0, bit 3) defining the failure that caused this message will be with this sense message. The message will only be sent if caching had been active before the failure.

When the message is 9, bytes 8 - 23 are formatted as follows:

BYTE	BIT	MEANING
8		Error Code *
9-20		Not used, must be zero
21		Storage Director Identification
22-23		Fault Symptom Code

* ERROR CODE	DEFINITION
x'00'	No message
x'01'	Entering limited caching state
x'02'	Subsystem storage port failure
x'03'	Subsystem storage general failure
x'04'	Caching status miscompare detected
x'05'	Subsystem Processing Error
x'07'	Reset received with resets inhibited
x'09'	Test and Set Register appears locked
x'0A'	Storage Director Equipment Check

Contents

Section Description

The IBM 3880 Storage Control Model 23 is a general purpose DASD controller with cache designed to run under both the 370 and extended architecture versions of Multiple Virtual Storage/System Product (MVS/SP) operating system. The Model 23 is a control unit for 3380 Direct Access Storage Devices (DASD).

References to Other Sections

See PWR in the Maintenance Information Manual (MIM) for details about the power sequencer and monitor and the operator and power switch panels.

See the CARR section of the MIM for details of channel and control interface wiring.

For an introduction to the Model 23, see the INTRO section in the MIM.

For detailed descriptions of the error codes for each of the functional areas, see the respective section in the Error Codes Manual (ECM).

Functional Areas

The Model 23 contains the following functional areas:

- Channel Interface (CHL–I)
- Control (CTRL)
- Data Buffer (DBFR)
- Port Adapter
- Port
- Subsystem Storage Control
- Subsystem Storage
- Control Interface (CTL–I)
- Maintenance Connection (MNT–C)
- Diskette Drive (DD)
- Power (PWR)

OPER Section Outline

The first portion of the OPER section describes the card to card data flow through a storage director.

The next portion describes each of the functional areas. The discussion includes:

- List of all Cards in Functional Area
- Description of Cards
- Card to Card Diagram
- Description of Data Flow Through Area

Notes:

1. The Maintenance (MNT) area description includes the description of the Diskette Drive area.
2. See the Power (PWR) section of the MIM for the description of the Power functional area.

After describing the functional areas, the Operations section discusses the channel commands used with the 3880 Model 23.

The rest of the Operation sections covers the following topics:

- Disconnected command chaining
- Status information
- Channel interface operations
- Resets
- Initial microcode load
- Storage director communications
- Error alerts
- Diskette drive operations
- Read circuit principles
- Control interface operations
- Device Tag Sequence

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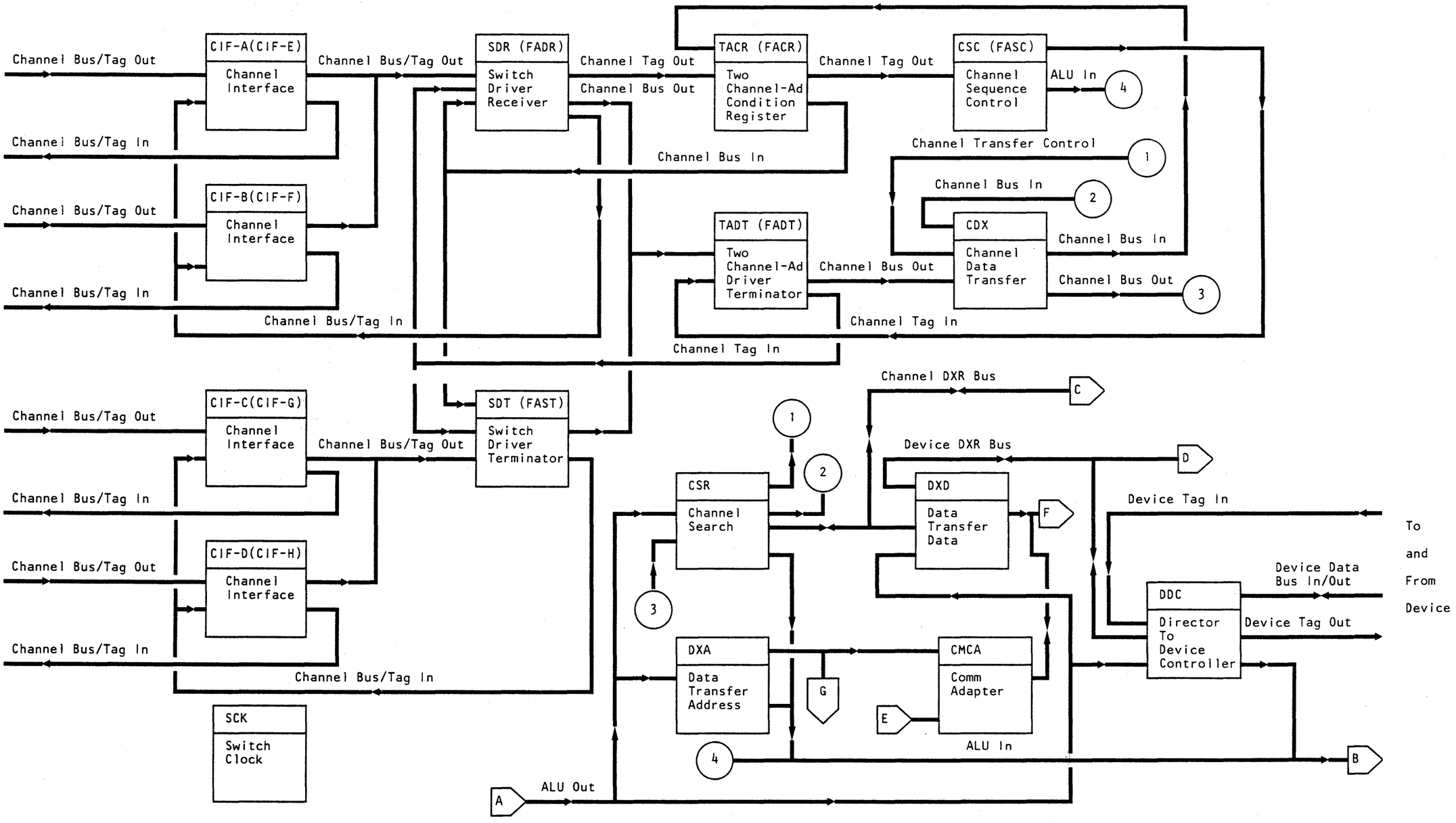
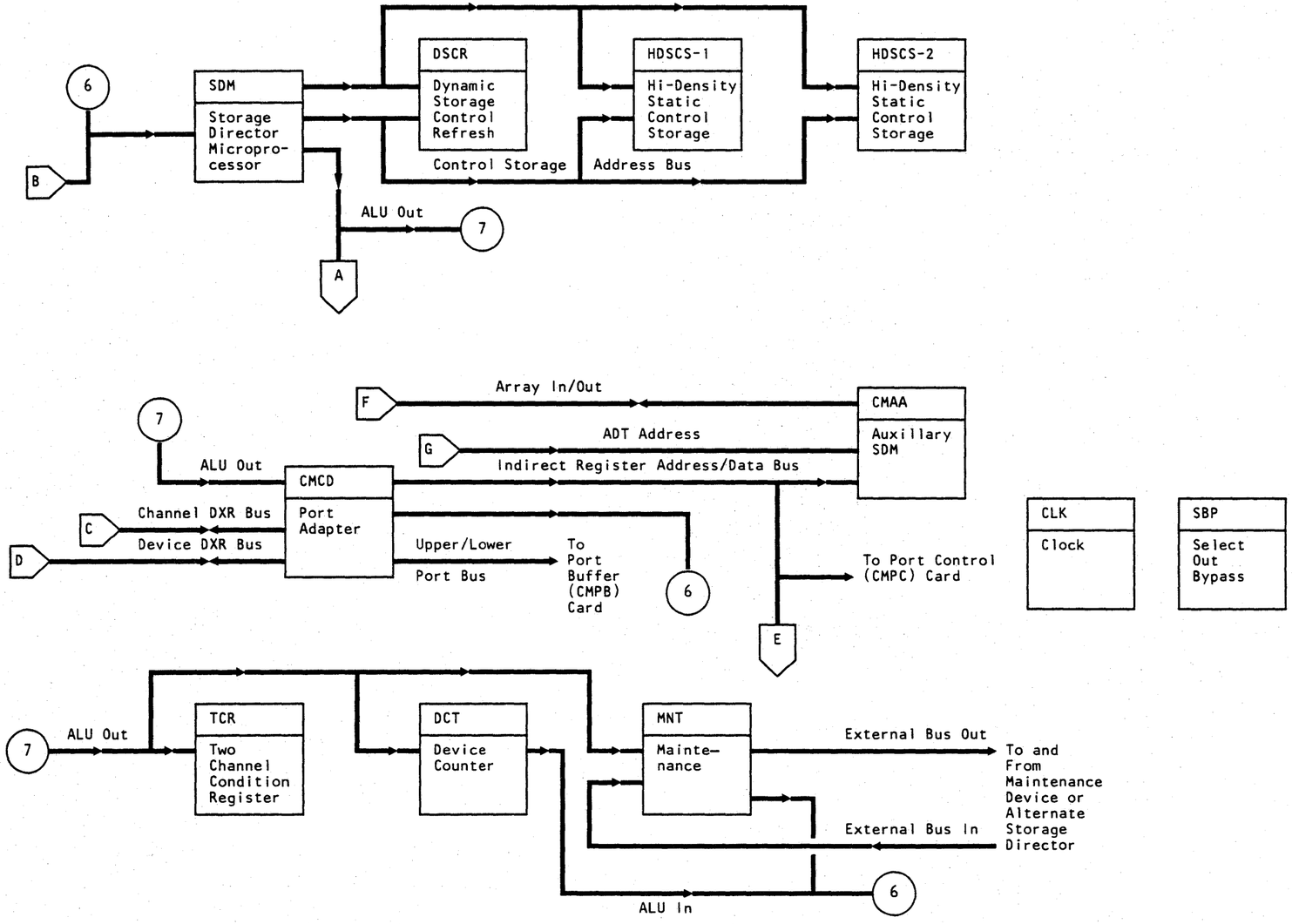


Storage Director Data Flow (Continued)



Data Transfer Between the Channel and the Port Adapter (CMCD Card)

On a Model 23 with the Two Channel Switch—Pair, Additional feature the data flow is as follows:

- The data from a channel enters a channel interface (CIF) card and then goes to the switch driver receiver (SDR) card.
- From the SDR card, the data goes to the two channel additional driver teminator (TADT) card, to the channel data transfer (CDX) card, and then to the channel search (CSR) card.
- The data leaves the CSR card on the channel DXR bus and goes to the port adapter (CMCD) card.

Data Transfers Between the Channel and the Device

Data transfers between the channel and the device always involve the ADT buffer. The data transfers across the channel DXR bus to the DXD card and then to the ADT buffer on the CMCA card. From the ADT buffer, the data transfers back to the DXD card then to the device via the device DXR bus.

Data transfer from the device to the channel is the reverse of the above.

Channel Interface Card Descriptions

Two Channel Switch Pair

The channel interface functional area with the Two Channel Switch Pair feature contains the following cards:

- Channel interface (CIF) cards A and B
- Select out bypass (SBP) cards A and B
- Channel sequence control (CSC) card
- Channel data transfer (CDX) card
- Channel search (CSR) card
- Two–channel condition register (TCR) card

Channel Interface (CIF) Cards

The CIF cards provide the communication paths between a channel and a storage director. Only one channel can communicate with a storage director at any time. There is a CIF card for each channel attachment (A-H). Each CIF card:

- Enables and disables the channel interface
- Transfers data between the channel and the CDX card
- Transfers status and control information between the channel and the channel sequence control (CSC) card
- Informs the storage director microprocessor (SDM) card of a system reset, or a halt I/O by way of the CSC card
- Generates the short busy sequence
- Performs channel and control unit initiated selection sequences

Select Out Bypass (SBP) Cards

Each SBP card bypasses the:

- Select out signal to another storage control
- Select in signal to another storage control or to the channel

A storage director contains one SBP card for each channel interface (CIF) card.

Channel Sequence Control (CSC) Card

The CSC card:

- Contains channel interface hardware information
- Causes Channel Bus Out to be gated from one of the channel interface (CIF) cards to the channel data transfer (CDX) card
- Transfers channel tags out (CTO) from the selected CIF card to the storage director microprocessor (SDM) card

Channel Data Transfer (CDX) Card

The CDX card:

- Transfers data between the channel interface (CIF) card and the channel search (CSR) card
- Matches the data transfer speed of the device to the data transfer speeds of the channel

Channel Search (CSR) Card

The CSR card compares the data on Channel Bus Out (CBO) with the data on Data Transfer (DXR) Bus In during a search operation.

Two Channel Condition Register (TCR) Card

The TCR card contains channel condition registers. The microprocessor uses these registers to control the channel interface (CIF) cards.

A storage director contains one TCR card for the CIF-A and the CIF-B cards.

Two Channel Additional Switch Pair

The two channel additional feature uses the following cards from the two channel switch pair feature:

- Channel interface (CIF) cards A and B
- Select out bypass (SBP) cards A and B
- Channel sequence control (CSC) card
- Channel data transfer (CDX) card
- Channel search (CSR) card
- Two–channel condition register (TCR) card

The two channel additional feature adds the following cards:

- Channel interface (CIF) cards C and D
- Select out bypass (SBP) cards C and D
- Switch clock (SCK) card
- Switch driver receiver (SDR) card
- Switch driver terminator (SDT) card
- Two channel additional condition register (TACR) card
- Two channel additional driver terminator (TADT) card

Switch Clock Card

The switch clock (SCK) card provides timing pulses to the CIF-A through H cards.

Switch Driver Receiver (SDR) Card

The SDR card receives signals from the CIF-A and CIF-B cards, converts them from a 3-volt to a 5-volt level, and sends the signals to the two channel additional condition register (TACR) card and to the two channel additional driver terminator (TADT) card on the storage director board.

The SDR card also receives signals from the TACR and TADT cards on the storage director board, converts them from a 5-volt to a 3-volt level, and sends them to the CIF-A and CIF-B cards.

Switch Driver Terminator (SDT) Card

The SDT card receives signals from the CIF-C and -D cards, converts them from a 3-volt to a 5-volt level, and sends them to the two channel additional condition register (TACR) card and the two channel additional driver terminator (TADT) card on the storage director board.

The SDT card also receives signals from the TACR and TADT cards on the storage director board, converts them from a 3-volt to a 5-volt level, and sends them to the CIF-C and -D cards.

The SDT card contains terminator resistors that terminate the signal lines connecting the SDR and SDT cards on the two channel additional board to the TACR and TADT cards on the storage director board.

Two Channel Additional Condition Register (TACR) Card

The TACR card contains channel condition registers. The microprocessor uses these registers to control the channel interface (CIF) cards.

The TACR card receives signals from the switch driver receiver (SDR) and the switch driver terminator (SDT) cards on the two channel additional board, converts them from a 5-volt to a 3-volt level, and sends them to the channel sequence control (CSC) card.

The TACR card receives signals from the CSC card, converts them from a 3-volt to a 5-volt level, and sends them to the SDR and SDT cards on the storage director board.

A storage director has one TACR card for the CIF-C and the CIF-D cards.

Two Channel Additional Driver Terminator (TADT) Card

The TADT card receives signals from the switch driver receiver (SDR) and the switch driver terminator (SDT) cards on the two channel additional board, converts them from a 3-volt to a 5-volt level, and sends them to the channel sequence control (CSC) card.

The TADT card also receives signals from the CSC card, converts them from a 3-volt to a 5-volt level, and sends them to the SDR and SDT cards on the two channel additional board.

The TADT card contains terminator resistors that terminate the signal lines connecting the TACR and TADT cards on the storage director board to the SDR and SDT cards on the two channel additional board.

Four Channel Additional

The four channel additional feature uses the following cards from the two channel switch pair feature and the two channel additional feature:

- Channel interface (CIF) cards A through D
- Select out bypass (SBP) cards A through D
- Channel data transfer (CDX) card
- Channel search (CSR) card
- Two Channel condition register (TCR) card
- Switch clock (SCK) card
- Switch driver receiver (SDR) card

The Four Channel additional feature adds the following cards:

- Channel interface (CIF) cards E through H
- Select out bypass (SBP) cards E through H
- Four channel additional sequence control (FASC) card
- Four channel additional condition register (FACR) card
- Four channel additional driver terminator (FADT) card
- Four channel additional switch terminator (FAST) card
- Four channel additional driver receiver (FADR) card

Four Channel Additional Sequence Control (FASC) Card

The FASC card:

- Contains channel interface hardware information
- Causes Channel Bus Out to be gated from one of the channel interface (CIF) cards to the channel data transfer (CDX) card
- Transfers channel tags out (CTO) from the selected CIF card to the storage director microprocessor (SDM) card

Four Channel Additional Condition Register (FACR) Card

The FACR card contains channel condition registers. The microprocessor uses these registers to control the channel interface (CIF) cards.

The FACR card receives signals from the four channel additional sequence control (FASC) card, converts them from a 3-volt to a 5-volt level, and sends them to the SDR and four channel additional switch terminator (FAST) cards on the A4 (A3) board.

A storage director has one FACR card for the CIF-C through the CIF-H cards.

Four Channel Additional Driver Terminator (FADT) Card

The FADT card receives signals from the SDR card and the FAST card on the two channel additional board, converts them from a 3-volt level to a 5-volt level, and sends them to the four channel additional sequence control (FASC) card. The FADT card also receives signals from the FASC card, converts them from a 3-volt level to a 5-volt level, and sends them to the SDR and FAST cards on the two channel additional board.

The FADT card contains terminator resistors that terminate the signal lines connecting the FACR and FADT cards on the storage director boards.

Four Channel Additional Switch Terminator (FAST) Card

The FAST card contains terminator resistors that terminate the signal lines connecting the SDR and FAST cards on the four channel additional board to the FACR and FADT cards on the storage director board.

The FAST card receives signals from the FACR and FADT cards, converts them from a 3-volt level to a 5-volt level, and sends them to the CIF cards.

Four Channel Additional Driver Receiver (FADR) Card

The FADR card is installed in addition to the SDR card on machines with the four channel additional feature. The SDR card is on the two channel additional board and the FADR card is on the four channel additional board.

The FADR card receives signals from the CIF-A, B, E, and F cards, converts them from a 3-volt level to a 5-volt level, and sends them to the FACR card and to the FADT card on the storage director board.

The FADR card also receives signals from the FACR and FADT cards on the storage director board, converts them from a 5-volt level to a 3-volt level, and sends them to the CIF-A, B, E, and F cards.

Model 23 Channel Interface OPER 27

Channel Feature Card Layout **OPER 28**

TWO CHANNEL SWITCH PAIR

Storage Director 1 Board 01A-B4 or
Storage Director 2 Board 01A-B3

- Channel Interface A (CIF-A) Card
- Channel Search (CSR) Card
- Channel Interface B (CIF-B) Card
- Two-Channel Condition Register (TCR) Card
- Select Out Bypass A (SBP-A) Card
- Channel Data Transfer (CDX) Card
- Select Out Bypass B (SBP-B) Card
- Channel Sequence Control (CSC) Card

TWO CHANNEL ADDITIONAL SWITCH PAIR

Storage Director 1 Board 01A-B4 or Storage Director 2 Board 01A-B3

- Channel Search (CSR) Card
- Channel Data Transfer (CDX) Card
- Channel Sequence Control (CS C) Card
- Two-Channel Condition Register (TCR) Card
- Two-Channel Additional Driver Terminator (TADT) Card
- Two-Channel Additional Condition Register (TACR) Card

FOUR CHANNEL ADDITIONAL

Storage Director 1 Board 01A-B4 or Storage Director 2 Board 01A-B3

- Channel Search (CSR) Card
- Channel Data Transfer (CDX) Card
- Two-Channel ence Condition Register (TCR) Card
- Four-Channel Additional Sequence Control (FASC) Card
- Four-Channel Additional Driver Terminator (TADT) Card
- Four-Channel Additional Condition Register (TACR) Card

Two-Channel Additional SD 1 Board 01A-A4 or
Two-Channel Additional SD 2 Board 01A-A3

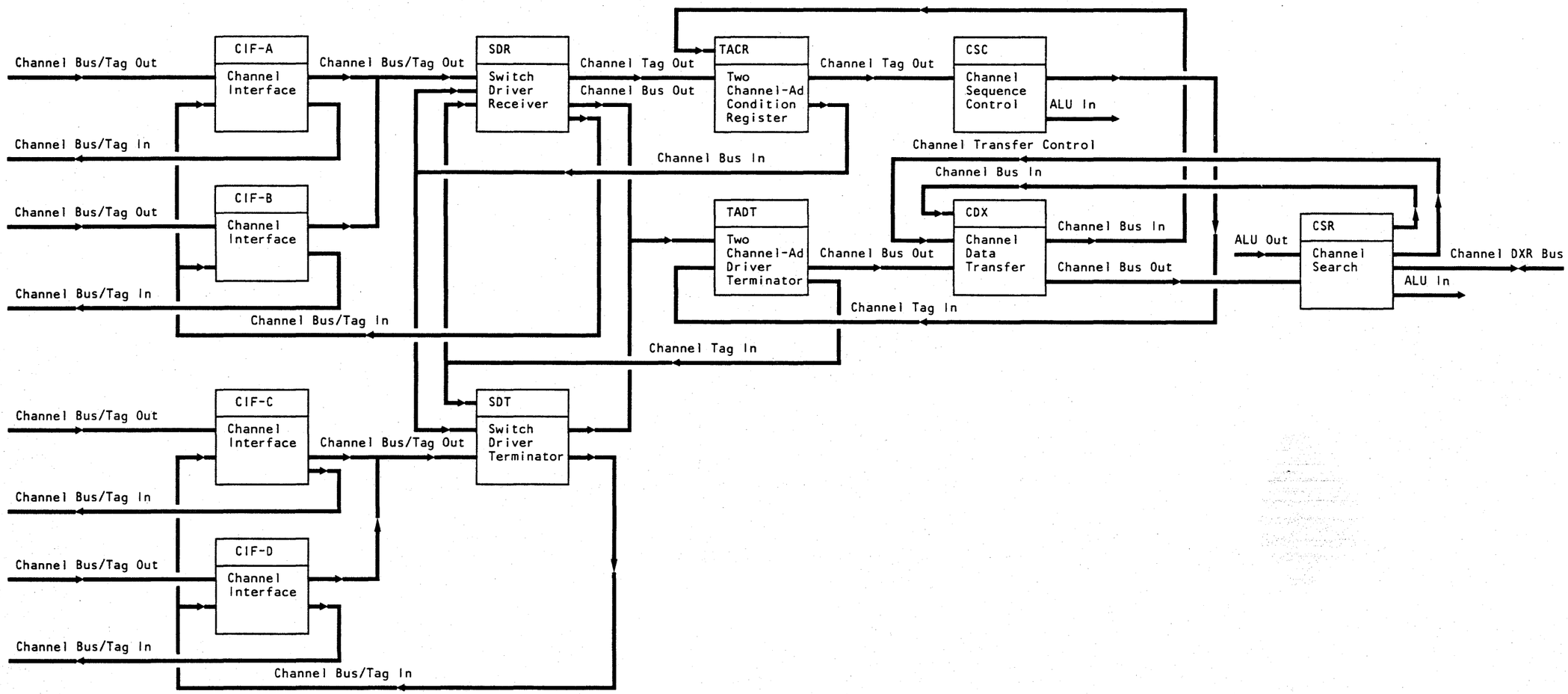
- Channel Interface A (CIF-A) Card
- Select Out Bypass A (SBP-A) Card
- Switch Driver Receiver (SDR) Card
- Channel Interface B (CIF-B) Card
- Select Out Bypass B (SBP-B) Card
- Switch Clock (SCK) Card
- Channel Interface C (CIF-C) Card
- Select Out Bypass C (SBP-C) Card
- Switch Driver Terminator (SDT Card
- Channel Interface D (CIF-D) Card
- Select Out Bypass D (SBP-D) Card

Two-Channel Additional Board SD 1 01A-A4 or
Two-Channel Additional Board SD 2 01A-A3

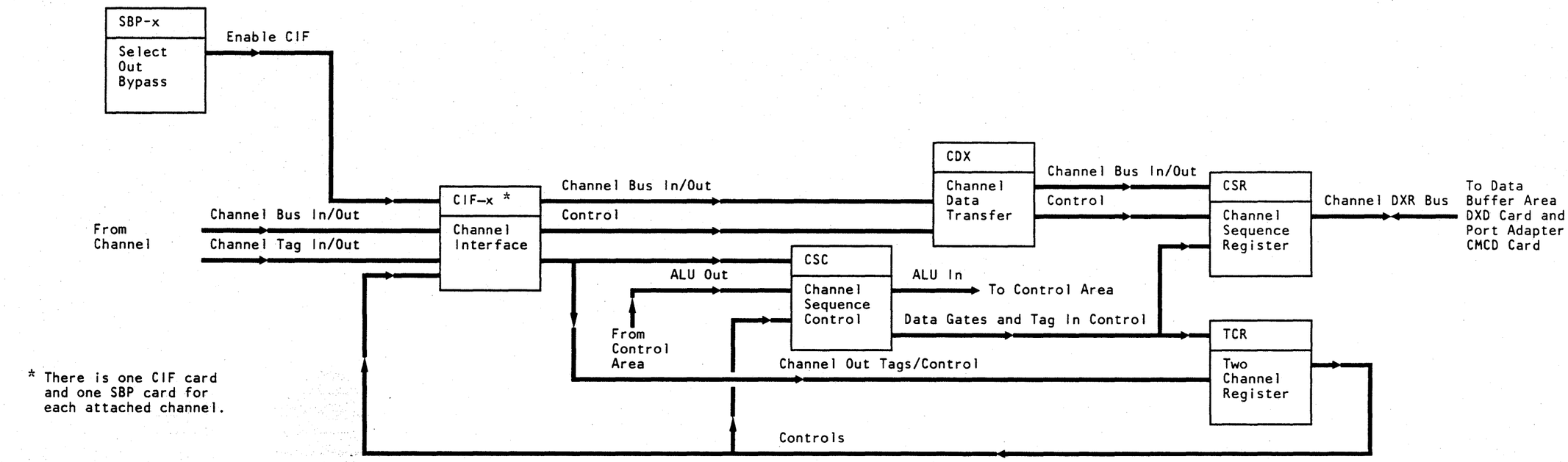
- Channel Interface A (CIF-A) Card
- Select Out Bypass A (SBP-A) Card
- Switch Driver Receiver (SDR) Card
- Channel Interface B (CIF-B) Card
- Select Out Bypass B (SBP-B) Card
- Four—Channel Additional Switch Driver Terminator (FAST) Card
- Channel Interface C (CIF-C) Card
- Select Out Bypass C (SBP-C) Card
- Channel Interface D (CIF-D) Card
- Select Out Bypass D (SBP-D) Card

Four-Channel Additional Board SD 1 01A-A2 or
Four-Channel Additional Board SD 2 01A-A1

- Channel Interface E (CIF-E) Card
- Select Out Bypass E (SBP-E) Card
- Switch Clock (SCK) Card
- Channel Interface F (CIF-F) Card
- Select Out Bypass F (SBP-F) Card
- Switch Driver Receiver (SDR) Card
- Channel Interface G (CIF-G) Card
- Select Out Bypass G (SBP-G) Card
- Four-Channel Additional Driver (FADR) Card
- Channel Interface H (CIF-H) Card
- Select Out Bypass H (SBP-H) Card



Channel Interface with Two Channel Switch—Pair, Additional Feature



Channel Interface with Two Channel Switch Pair Feature

Channel Interface Card to Card Data Flow

The channel interface (CHL-I) functional area:

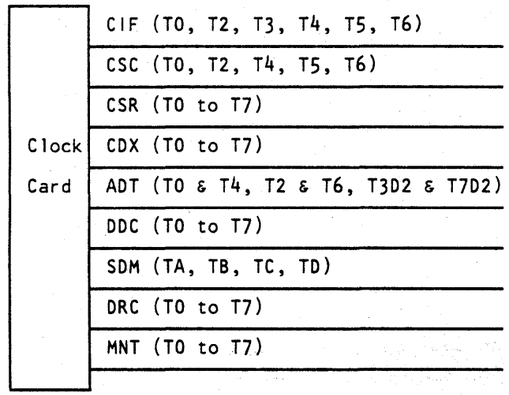
- Moves data between the channel and the data buffer area and between the channel and the port adapter area
- Sends control information from the channel to the control functional area
- Senses and informs the control functional area of the status of the control information lines

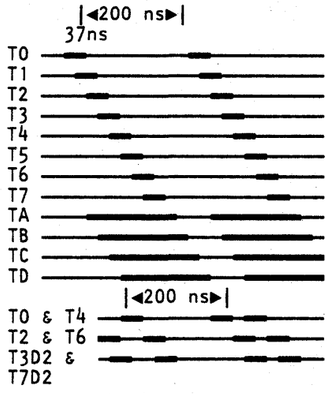
Channel Bus In/Out data flows through the CIF, CDX, and CSR cards to the channel DXR bus. The channel area is controlled by the ALU (in conjunction with the CSC and TCR cards). The ALU senses the Tag Out lines and responds with the necessary data and Tag In lines.

Control Area Card Descriptions

The control functional area of the storage director contains the following cards:

- Storage director microprocessor (SDM)
- Dynamic storage control and refresh (DSCR)
- High density static control storage (two cards: HDSCS–1 and HDSCS–2)
- Clock (CLK)
- Auxiliary Microprocessor Adapter (CMAA) Card





Storage Director Microprocessor (SDM) Card

The SDM card is the processing unit for the storage director.

The SDM card:

- Controls the sequence of microinstructions
- Decodes and executes the microinstructions
- Controls the reading and writing of data into control storage
- Controls the accessing and reading of data from the functional diskette
- Uses the external registers to control all the functional areas
- Selects and controls the controller and/or drives
- Starts data transfer
- Transfers status and command information to and from the channel
- Performs arithmetic and logic unit (ALU) functions
- Contains level 0 read-only storage (ROS) code used to perform maintenance operations that alter or display an external register, an internal register, the instruction address register (IAR) in the microprocessor, or a byte of data in control storage. ROS is located on the SDM card and contains the microcode checkout routine and the functional microcode loader.

Dynamic Storage Control and Refresh (DSCR) Card

The DSCR card stores functional microcode routines and control information not requiring high-speed execution. This storage must be periodically refreshed. The card contains refresh timing and address generation circuits for this purpose.

Dynamic control storage:

- Generates the current address of the block of control storage locations to be refreshed. The control storage is divided into 128 refreshable blocks.
- Provides storage for 96K bytes (48K addressable locations)
- Controls the sequence of dynamic storage refresh cycles
- Provides double bit detection capabilities for data stored in control storage. Single bit errors are corrected.
- Activates a timer and decoder that determine the 23.32 microsecond intervals between refresh cycles. This interval permits a refresh of the entire control storage every three milliseconds.
- Provides priority to refresh cycles over microprocessor cycles in case of concurrent requests. The refresh cycle requires 440 nanoseconds and stops the microprocessor clock pulse for that time. The refresh cycle of 440 nanoseconds equals two microprocessor cycles. The transfer of data or microinstructions to or from static control storage or ROS is not affected by the refresh cycle. However, if an address in dynamic control storage is accessed, the microprocessor clock is stopped 220 nanoseconds for each dynamic control storage location referred to in the instruction. This causes the microinstruction execution time for dynamic control storage to be at least one, and sometimes two, cycles longer than the microinstruction execution time for static control storage or ROS.

When an address parity check is detected, the DCSR card activates the CS Address Check line. When an uncorrectable data check is detected, the DCSR card activates the Uncorrectable Data Check line. The DCSR card also checks for the correct key bit during a Write operation and activates Key Bit Check if the key is not correct.

High Density Static Control Storage (HDSCS) Cards

The HDSCS cards store functional microprocessor routines and control information that requires high speed execution.

The high density static control storage is provided by two cards: high density static control storage one (HDSCS-1) and high density static control storage two (HDSCS-2). HDSCS-1 and HDSCS-2 each provide for the storage of 16K bytes (8K addressable locations).

Clock (CLK) Card

The clock card generates the clock pulses sent to each functional area. The maintenance card (described in the maintenance functional area) controls the clock card permitting selective starting and stopping of the functional area clocks.

The clock card contains a crystal oscillator. The oscillator is the timing source for each storage director and is active at all times after power is turned on.

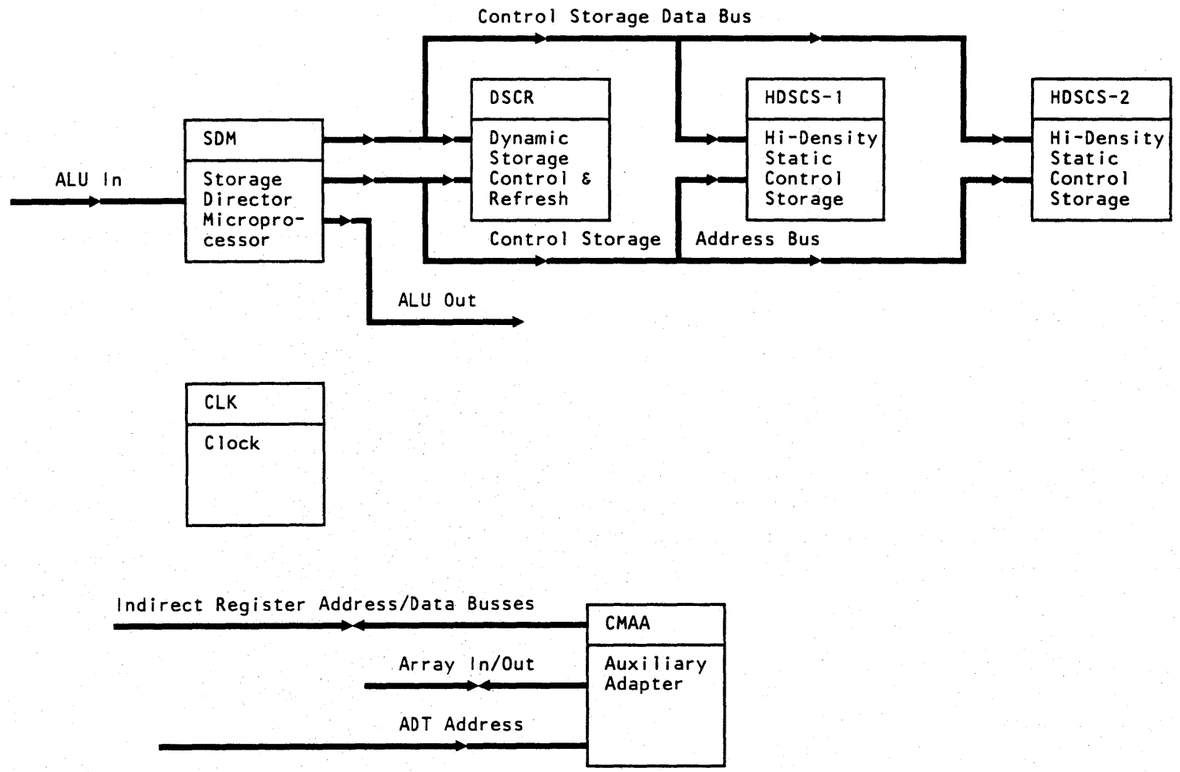
The crystal oscillator pulses are divided into even and odd pulses which become even and odd clock pulses. These even (T0, T2, T4, T6) and odd (T1, T3, T5, T7) pulses are distributed to the functional area in the storage director.

Auxiliary Microprocessor Adapter (CMAA) Card

The CMAA card contains:

- Auxiliary storage director microprocessor (ASDM)
- ASDM control storage (8K bytes)
- ASDM local storage registers
- ASDM indirect registers
- ADT/ASDM two interrupt levels

The auxiliary microprocessor performs DASD gap processing and timing functions. In other 3880 models, the storage director microprocessor (SDM) performs this function.



Control Area Description

Power On Reset

The clock pulses in each storage director begin during power on reset when the following sequence occurs:

1. The Power On Reset line activates and holds the storage director clock ring inactive.
2. The Power On Reset deactivates.
3. The clock ring starts approximately 250 nanoseconds after machine reset (power on reset) deactivates. The dynamic refresh control and the maintenance card timing pulses also activate.
4. A start signal from the maintenance card starts the other functional area timing pulses.

Clock Start and Stop

The clock pulses to each functional area start and/or stop under control of the maintenance (MNT) card, the dynamic control storage and refresh (DSCR) card, or during power on reset (POR).

The graph below shows start and stop conditions and the clocks that they affect.

CLOCK	STOP ON POR	START AFTER POR	START FROM MNT CARD	STOP FROM MNT CARD	MAINT START FROM MNT CARD	MC HOLD FROM DSCR CARD
CIF	X	X				
CDX	X		X	X		
ADT	X	X				
DDC	X		X	X		
SDM	X		X	X	X	X
DSCR	X	X				
MNT	X	X				
CSR	X		X	X		
CSC	X	X	X			
DCT	X		X	X		

A channel check 1 condition or a channel check 2 condition does not stop any clock.

A check 1 condition stops the CDX, DDC, SDM, CSR, and DCT clocks.

Maintenance Card Start and Stop

The maintenance (MNT) card sends three control lines to the clock card:

- Start
- Maintenance Start
- Stop

Start

The Start signal from the MNT card starts all functional area clocks that were not started after POR.

Maintenance Start

The Maintenance Start signal from the MNT card starts only the microprocessor area clock.

Stop

The Stop signal from the MNT card stops all clocks except the automatic data transfer, the channel interface, dynamic refresh control, maintenance, and channel sequence control clocks.

Microprocessor Hold from DSCR

The DSCR card is refreshed every 23.32 microseconds. During the refresh cycle of 440 nanoseconds, the microprocessor clock is stopped by microprocessor hold from the DSCR card to inhibit accessing or fetching. The clock is stopped only if the microprocessor is accessing dynamic control storage when a refresh is required.

Interval Timer

The interval timer is a 650 millisecond time-out that ensures that the microcode does not loop indefinitely when one of the following occurs:

- The storage director is waiting for the channel to respond during communication between the storage director and the channel.
- An error exists in the functional microcode.

The microcode sets the maintenance control/sense (MCS) register, bit 0, to activate the interval timer. Before the 650 millisecond time interval, the microcode resets and, if necessary, again sets the MCS register, bit 0. This reactivates the interval timer. The MCS register, bit 0, must be reset for at least 220 nanoseconds to reactivate the interval timer.

The timer overflow, bit 1, in the interrupt level register (ILR) is set when the MCS register, bit 0, remains active longer than 650 milliseconds +30% to -20%. This condition sets ILR, bit 6, the level 1 interrupt bit.

The microcode resets the MCS register, bit 0, to reset the timer overflow condition.

The interval timer is located on the clock (CLK) card.

Errors

Check 1

An error in the microprocessor, the control storage, or the clock is called a check 1 error. A check 1 error is an error that stops the clock and causes the other storage director to read error information from the failing storage director. This error information is sent to the host system of the other storage director as format 3 sense information. For a check 1 error, sense bytes 8 through 23 contain the contents of the following:

SENSE BYTE	CONTENTS
8	FRU register 2 (bit 4=0)
9	Check register 1
10	Check register 2
11	Check register 3
12	Not used
13	Not used
14	Not used
15	FRU register 3
16	FRU register 4
17	Not used
18	Not used
19	Not used
20	Not used
21	Storage director identification
22-23	Symptom code

Bit 4 of FRU register 2 indicates whether the sense bytes contain check 1 error information (bit 4=0) or channel check 1 error information (bit 4=1).

Check 1 errors are detected by hardware.

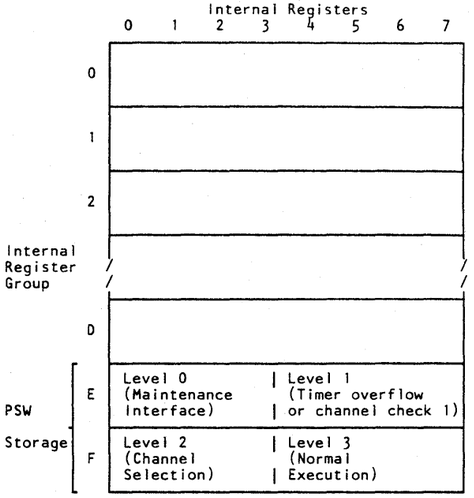
Channel Check

An error in the channel interface is called a channel check 1 error. A channel check 1 error is an error that does not stop the clock but causes the microcode in the failing storage director to send check and status information to the other (alternate) storage director.

Channel check 1 errors are detected by microcode.

Program Status Word Storage

At the end of a microinstruction, the microprocessor monitors a request for an interrupt. When an interrupt occurs, the microprocessor stores the current program status word (PSW). The PSW is stored in one of the following positions:



Each PSW contains:

- Instruction address register (IAR)
- Condition codes (CC)
- Internal register group (IRG)

PSW	IAR (High)	IAR (Low)	CC	IRG

Program Status Word Swap

When the storage of the PSW is complete, the hardware automatically fetches the PSW from the internal register space assigned to the interrupt level about to resume execution. After the IAR, CC, and IRG for the new interrupt level have been retrieved, the PSW swap is complete, and normal microinstruction proceeds at the new level.

The time between execution of the last microinstruction at the previous level and execution of the first microinstruction at the present level is two microinstruction cycles.

Control Area Description (Continued)

Registers

The 3880 Model 23 contains several different kinds of registers:

- Internal
- External
- External Indirect
  - Upper port
  - Lower port
  - Common
  - General
- Shadow

Internal Registers

The control functional area contains 256 internal registers: 32 groups of 8 registers each. (Half of the internal registers are in the storage director microprocessor; half are in the auxiliary storage director microprocessor.) The microcode uses the registers as working registers.

A microinstruction can contain one or two internal register fields to select either one or two internal registers from the same or different internal register groups.

External Registers

External registers are used by the microcode to contain information used in:

- addressing of external indirect registers
- control
- error detection, correction, and recovery
- automatic data transfer control
- status display

The microcode uses two external registers, X'1B' and X'0F' to communicate with the external indirect registers. Data in register X'1B' is used to address an external indirect register. Register X'0F' is used to contain data either read from or to be written to the external indirect register pointed to by external register X'1B'.

External Indirect Registers

Indirect external registers consist of:

- Upper port registers
- Lower port registers
- Common registers
- General registers

These registers are used for transferring data to and from subsystem storage and the ADT buffer, device, or channel.

Each storage director has a set of upper and lower port registers.

Common registers are defined as registers that are common to both upper and lower data ports and data controls. Common registers are associated with a particular storage director; each storage director has its own set of common registers.

There is only one set of general registers; both storage directors can access all of the general registers.

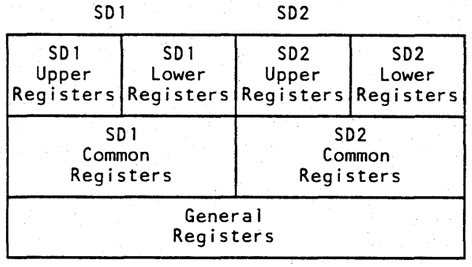


Figure 1. External Indirect Registers

Shadow Registers

Shadow registers are backup registers for some of the external indirect registers.

References

For more detailed information about the 3880 registers, see the REF section.

Card Descriptions

The data buffer area contains the following cards:

- Communication adapter (CMCA) card
- Data transfer addressing (DXA) card
- Data transfer (DXD) card

Data Transfer Data (DXD) Card

The DXD card:

- Transfers data to or from a device or channel
- Matches data transfer speeds between a device and a channel
- Performs cyclic redundancy checking on data transfers between the buffer and the device and between the buffer and the channel.

The DXD card is used during the 3880 Read, Write, and Search operations.

The DXD card transfers data:

- Between the ADT buffer or subsystem storage and the channel
- Between the ADT buffer or subsystem storage and the device
- Between the ADT buffer and the subsystem storage

Data Transfer Address (DXA) Card

The DXA card generates addresses for storing into and fetching from the ADT buffer. (The ADT buffer is on the CMCA card.) In addition, the DXA card contains control registers, sense registers, and address pointer registers.

Communication Adapter (CMCA) Card

The CMCA card performs a buffer function and a port function.

The buffer function (ADT buffer) allows automatic data transfer between subsystem storage and channel and/or device. The data flowing into the buffer comes from the DXD card. The DXA card supplies the buffer addressing.

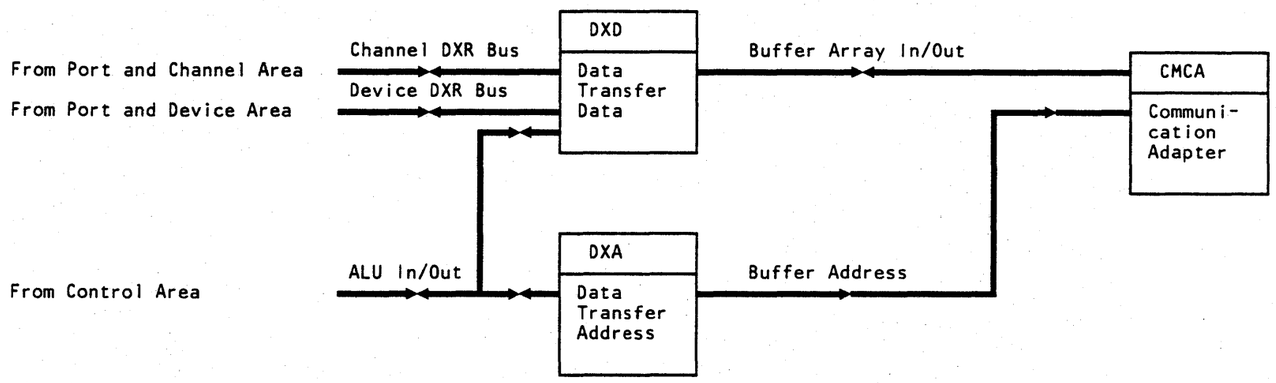
The port function consists of port to port communication. This communication is by way of a 256 byte buffer in port 2.

Data Buffer Card to Card Data Flow

Data transfers to the data buffer area from the channel interface, the device interface, the subsystem storage (upper and lower ports), and the microprocessor ALU area.

Data may be transferred from:

- Device to channel through the buffer
- Device to subsystem storage through the buffer or bypassing the buffer
- Device to subsystem storage and to channel through the buffer
- Channel to device through the buffer
- Channel to subsystem storage through the buffer or bypassing the buffer
- Channel to subsystem storage and to device through the buffer
- Buffer to subsystem storage
- Subsystem storage to buffer
- ALU to subsystem storage
- ALU to buffer



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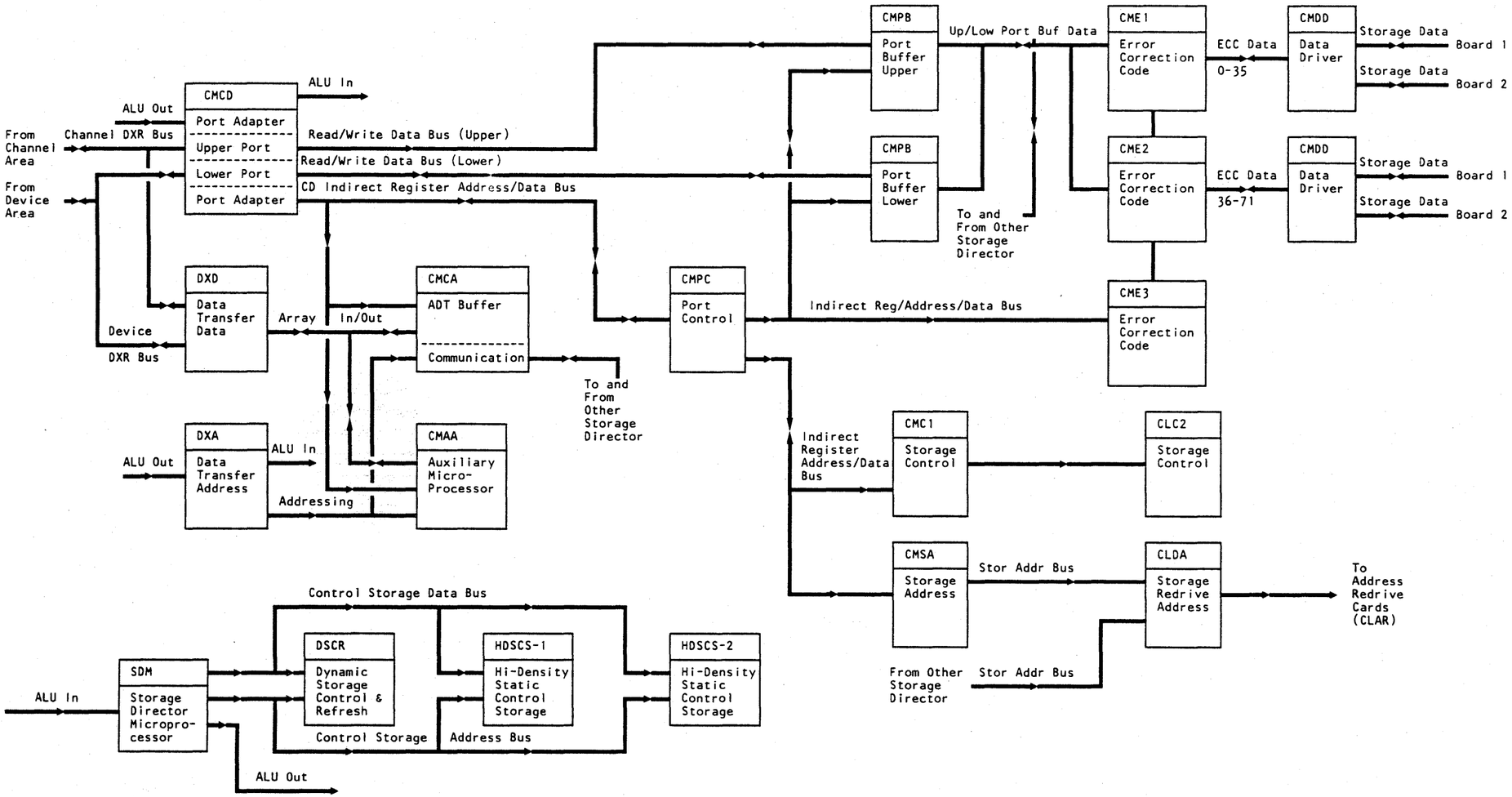


Subsystem Storage Data Flow

The 3880 Storage Control controls data transfers between the subsystem storage and the:

- Channel
- Devices
- ADT Buffer

Note: Data from the channel can go the subsystem storage and the DASD concurrently. Data from the DASD can go the channel and the subsystem storage concurrently.

Data Transfers Between the Channel and Subsystem Storage

Data from the channel area travels on the channel DXR bus to the CMCD card. This data then goes out the CMCD card's upper port and travels directly to the upper port buffer, bypassing the ADT buffer. The data then passes through error correction to the data driver cards on its way to storage.

Data transfer from the subsystem storage to the channel is the reverse of the above.

Data Transfers From the Channel to the DASD with Concurrent Transfer to Subsystem Storage

Data transfer from the channel to the device with concurrent transfer to subsystem storage is called a branching write.

Data from the channel area travels on the channel DXR bus to the DXD card and into the ADT buffer on the CMCA card. The data them goes back to the DXD card and out on the device DXR bus. The data on the DXR bus goes to the control interface area and to the DASD. At the same time the data on the DXR bus goes to the CMCD card. This data then goes out the CMCD card's lower port and travels directly to the lower port buffer. The data then passes through error correction to the data driver cards on its way to storage.

Data Transfers From the Device to the Channel With Concurrent Transfer to Subsystem Storage

Data transfer from the DASD to the channel with concurrent transfer to subsystem storage is called a branching read.

Data from the DASD goes to the control interface area to the device DXR bus. The data on the device DXR bus goes to the DXD card, then to the ADT in the CMCA card and then back to the DXD card. The data leaves the DXD card on the channel DXR bus, goes to the channel functional area and to the channel. At the same time the device DXR bus also goes to the CMCD card lower port. The data passes through the CMCD card lower port to the lower port buffer. The data then passes through error correction to the data driver cards on its way to subsystem storage.

Data Transfers Between Subsystem Storage and the Device

Data in subsystem storage travels through the data driver cards to the ECC cards. From the ECC cards, the data goes through the lower port buffer card and to the lower port of the CMCD card. From the lower port of the CMCD card, the data transfers over the device DXR bus directly to the control interface area, bypassing the ADT buffer.

Data transfer from the device to the subsystem storage is the reverse of the above. Transfer of data from the device to the subsystem storage is called promotion.

Data Transfers Between Subsystem Storage and the ADT Buffer

Data can be transferred between the subsystem storage and the ADT buffer for operations such as directory updates.

Subsystem Storage to ADT Buffer

Data in the subsystem storage goes through the data driver cards and then to the error correction code (ECC) cards. From the ECC cards the data goes to the upper or lower port buffer card and then to the upper or lower port of the CMCD card.

The data travels from the CMCD card to the DXD card via the channel DXR bus or the device DXR bus. The DXD card sends the data to the ADT buffer.

ADT Buffer to Subsystem Storage

From the ADT buffer, the data flows to the DXD card and then across the device DXR bus or channel DXR bus to the device.

If the data is on the channel DXR bus it goes to the upper port on the CMCD card. If the data is on the device DXR bus it goes to the lower port on the CMCD card. From the upper or lower port, the data goes to the upper or lower port buffer (CMPB) cards and then to the error correction cards.

After passing through error correction, the data goes to the data driver cards and is sent to subsystem storage.

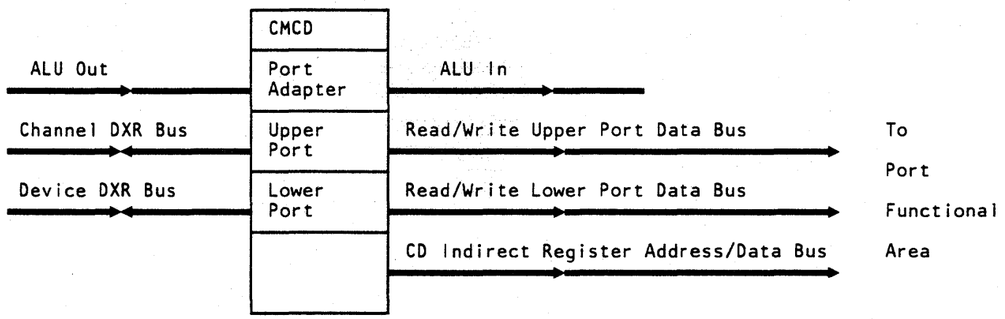
Port Adapter Area

The port adapter area contains only the port adapter card.

Port Adapter (CMCD) Card

The CMCD card is the data transfer and control card. It is the interface between the storage director and the subsystem storage. This card generates the controls for the data buffer and data ports to permit automatic data transfers between the subsystem storage and the channel or between the subsystem storage and the device. The port adapter also generates controls to permit manual data transfers between the storage and the ADT buffer for access by the auxiliary storage director microprocessor (ASDM).

The CMCD card provides data paths from the channel DXR bus to the upper port buffer and from the device DXR bus to the lower port buffer. Storage (cyclic) redundancy checking (SRC) is performed on each of these paths. All subsystem storage and control data pass through the CMCD card.



Card Descriptions

The port functional area contains the following cards:

- Port control (CMPC) card
- Port buffer upper (CMPB) card
- Port buffer lower (CMPB) card

Port Control (CMPC) Card

The port control card supplies the redrive, distribution, and error checking of the external indirect register bus lines between the port connection and the storage address (CMSA) and storage control (CMC1); and between the port buffer (CMPB) and the error correction code (ECC) function.

Port Buffer (CMPB) Cards

The port buffer cards permit asynchronous speedmatch operations between the one byte data bus of the port adapter (CMCD) and the four byte data bus of the ECC function. Each bus is a bi-directional bus. There is one CMPB card for the upper port buffer and one for the lower port buffer of each storage director.

Port Control and Port Buffer Card-to-Card Data Flow

The port connection functional area:

- Is the interface between the storage director microprocessor (SDM) and the subsystem storage control.
- Contains the controls and data buffers to permit automatic data transfers between the channel, device, and subsystem storage.
- Permits control between the two storage directors.

Data Flow

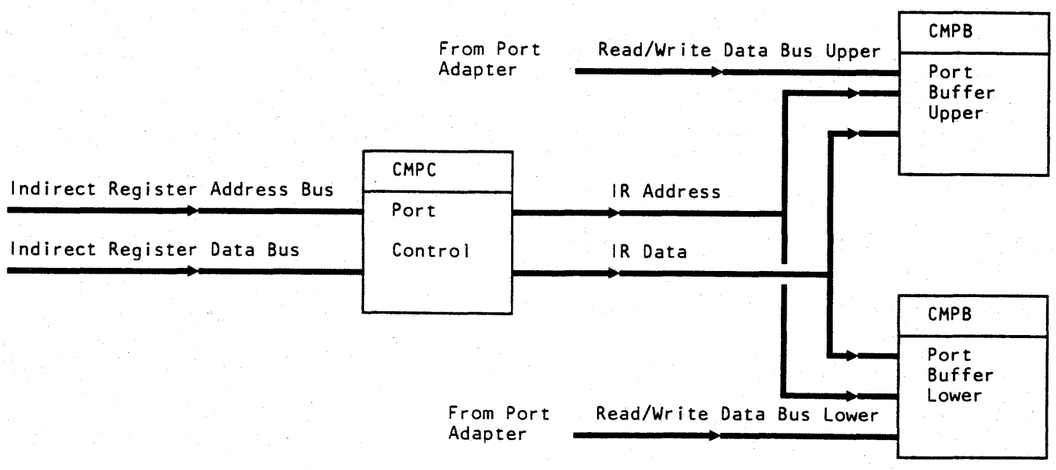
On a store operation, data from the channel DXR bus flows through the CMCD card to the upper port buffer card and then to the subsystem storage area. Data from the device DXR bus flows through the CMCD card to the lower port buffer card and then to the storage area. On a fetch operation, the data flows in the opposite direction.

Addressing and Control Data Flow

Control data residing in the cache is read into the ADT buffer. It can then be accessed by the microcode control program.

All control data and status information are passed to and from the subsystem storage control by way of the X'0F' and X'1B' registers. The X'1B' register is used to address the external indirect registers. The X'0F' register contains data to be passed to and from the external indirect registers.

Subsystem storage sense data is accumulated in indirect registers. This data is transferred by way of the indirect register bus to the CMCD card and then to the SDM card on the ALU In bus.



Card Descriptions

The subsystem storage control area contains the following cards:

- Storage control 1 (CMC1) card
- Storage control 2 (CLC2) card
- Storage drive address (CLDA) card
- Error correction code 1 (CME1) card
- Error correction code 2 (CME2) card
- Error correction code 3 (CME3) card
- Storage driver data (CMDD) card
- Storage address (CMSA) card

Storage Control (CMC1, CLC2) Cards

The storage control cards (CMC1 and CLC2) generate storage timings for the storage control board and the storage boards.

Storage Driver Address (CLDA) Card

The CLDA card interfaces between the storage address (CMSA) card and the storage boards. This card repowers the address bus to the storage board.

Error Correction Code 1 (CME1) Card

The CME1 card performs the following functions:

- Contains one half of the data between the port buffer and the storage data drivers
- Generates some of the 16 check and syndrome bits
- Generates corrected data for one half of the storage data bus

Error Correction Code 2 (CME2) Card

The CME2 card performs the following functions:

- Contains one half of the data between the port buffer and the storage data drivers
- Generates all 16 check and syndrome bits
- Generates corrected data for one half of the storage data bus.

Error Correction Code 3 (CME3) Card

The CME3 card:

- Generates the timing signals for the CME1 and CME2 cards from the phase clocks
- Interfaces the external control lines to the CME1 and CME2 cards
- Performs the syndrome decode and syndrome translation
- Contains a dual control connection to the error correction code (ECC) function which permits each storage director to access registers independently
- Provides access to diagnostic, write check bits, check bits, and syndrome bits

Storage Driver Data (CMDD) Card

The CMDD card is the data driver between the ECC function and the subsystem storage boards.

Storage Address (CMSA) Card

The CMSA card is the interface between the port control connection and the storage board. This card provides the storage address register (SSAR).

Storage Control and Storage Card to Card Data Flow

The storage functional area contains addressing and error correction and data gating controls. The storage control uses the three error correction code cards (CME1, CME2, and CME3) to correct single bit and double bit errors and detect triple bit errors.

Storage Data Flow

On a store operation, 16 bytes of data enter CME1 and CME2 from the port buffer cards. On each four byte transfer from a port buffer, two bytes are gated to CME1, and two bytes are gated to CME2. The error correction code (ECC) cards generate two check bytes that are stored along with the 16 data bytes in the storage cards.

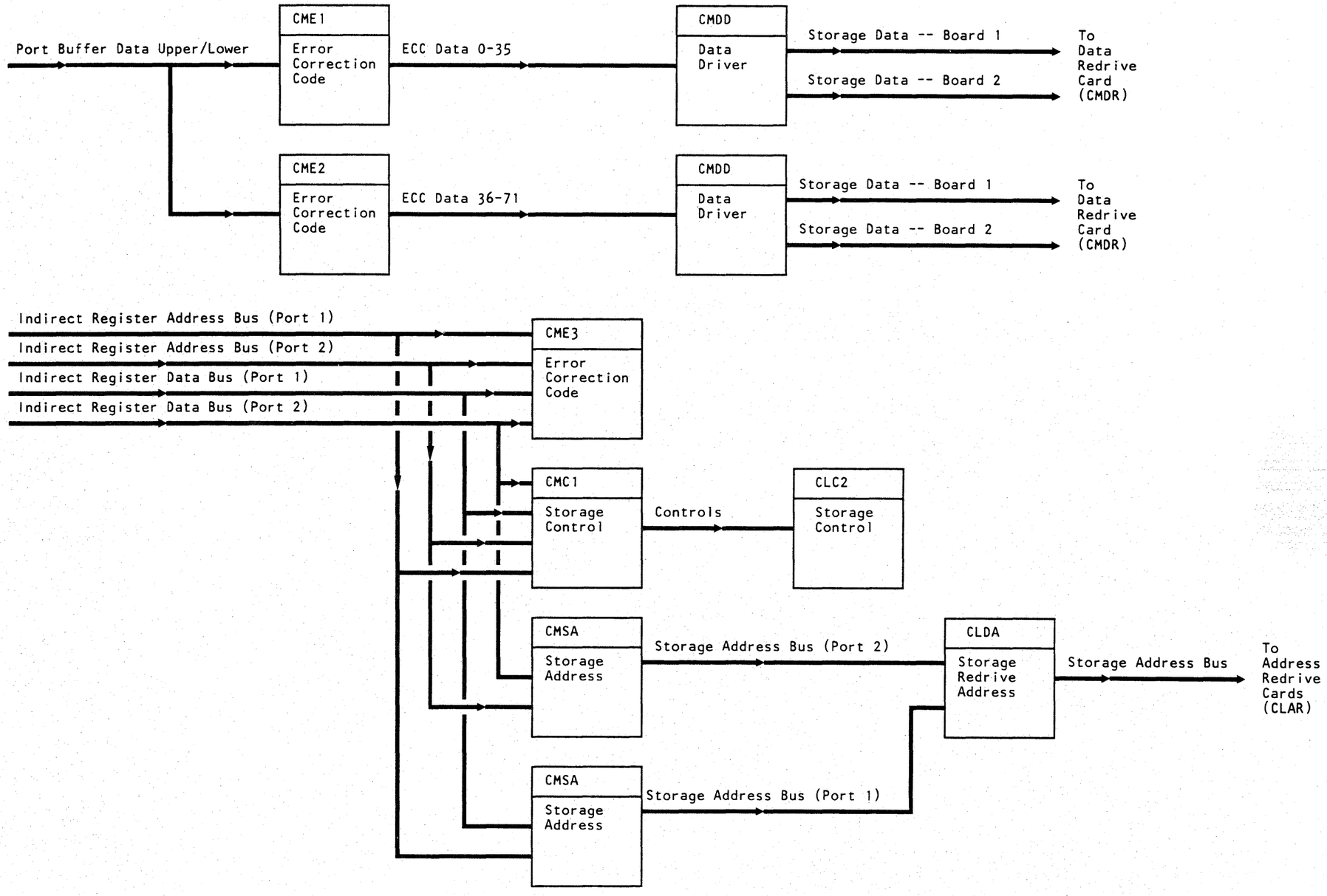
On a fetch operation, 16 bytes of data plus the two check bytes are gated from the storage board to the CMDD cards, and then to the ECC cards. The ECC cards generate syndrome bits, correct single or double bit errors, and inform the storage director of any triple bit errors. The corrected data is then transferred to the selected port buffer.

Storage Addressing

Each upper and lower port (in port 1 and in port 2) has a subsystem storage address register (SSAR) on a CMSA card. When a storage request for a given port is honored, its SSAR is gated to the CLDA card and then to the CLAR cards to address the storage cards.

Storage Control

The CMC1 and CLC2 cards provide the necessary clocking and gating pulses for storing and retrieving data.



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Subsystem Storage Area Card Descriptions

The two storage directors manage the subsystem storage without any assistance from the host system. The storage directors participate equally in the storage management; neither acts as master or slave.

The subsystem storage is a volatile array; a loss of power causes a loss of data in the subsystem storage.

The storage area contains the following cards.

- Data redrive (CMDR) cards
- Address redrive (CLAR) cards
- Storage (CLP4) cards

Data Redrive (CMDR) Cards

Each CMDR card sends and receives data to and from two storage cards for every storage request. Each storage board has two CMDR cards.

Address Redrive (CLAR) Cards

Each CLAR card addresses two storage cards of data for every storage request. Each storage board has two CLAR cards.

Storage (CLP2/CLP4) Cards

Each storage card holds two or four megabytes of data. (The two megabyte cards are only used with 8 megabytes of cache.) The storage cards are addressed in sets of four during a store or fetch.

Storage Operation

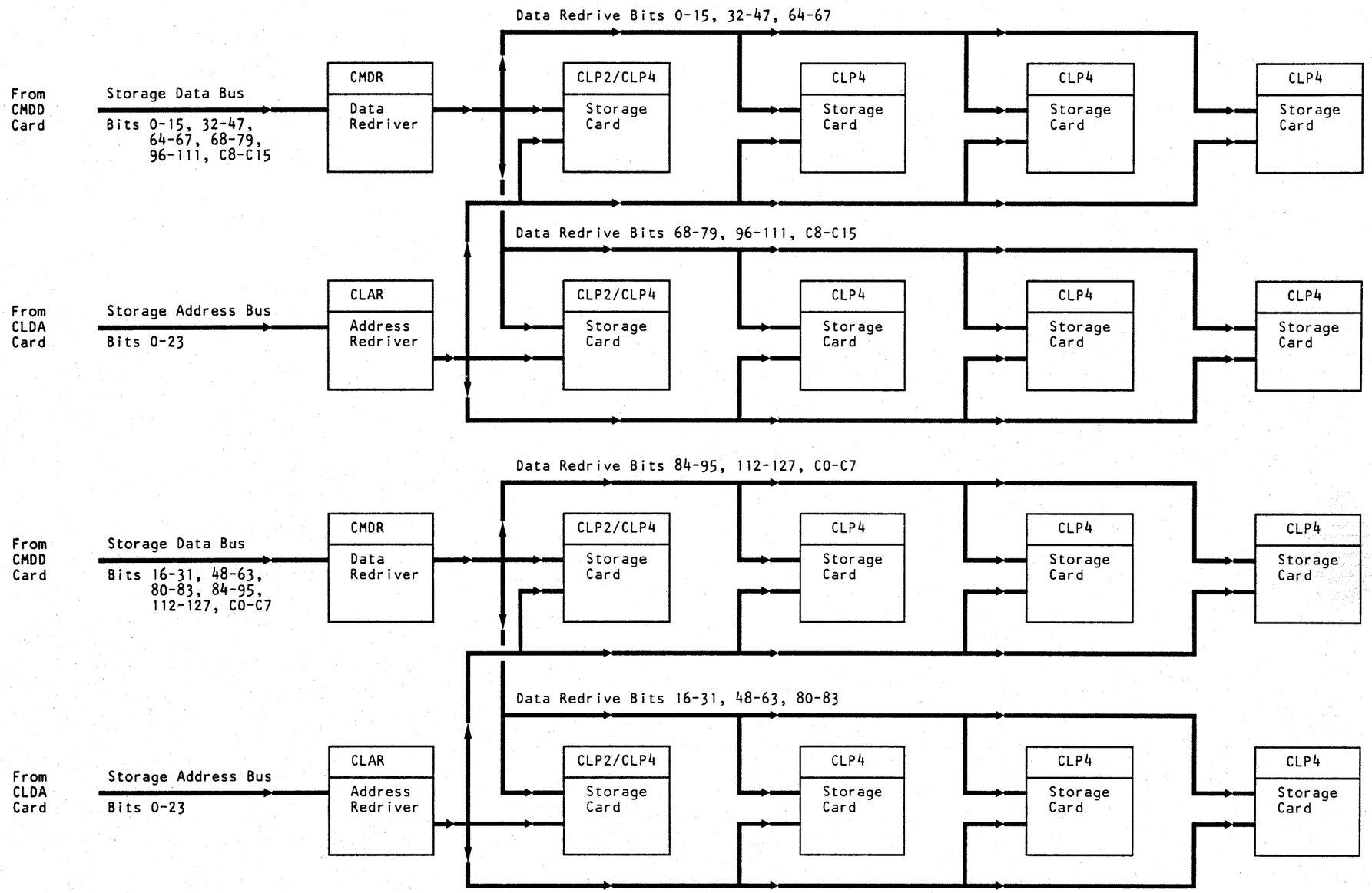
During a fetch or store operation four storage cards are addressed. Each card sends or receives 36 bits for a total of 144 bits (16 data bytes plus two check bytes).

The transfer of data to/from storage to the ECC function takes place in two parts, half the bits are associated with transfer A and the other half are associated with transfer B. Each 8 byte transfer takes 400 nanoseconds.

Concurrent data operations with the different ports (port 1 upper, port 1 lower, port 2 upper, port 2 lower) are multiplexed in 16-byte segments.

Refresh

Refresh occurs every five milliseconds. There are a total of 1024 refresh cycles. Each refresh cycle takes 4.8 microseconds with alternating cycles to high and low storage addresses.



Card Descriptions

The control interface functional area contains the following cards:

- Bidirectional Director–to–device controller (DDCV) card
- Device counter (DCT) card

Bidirectional Director-to-Device Controller (DDCV) Card

The DDCV card connects a storage director to a device controller. The DDCV card is, therefore, the communication path between the storage director and a device controller.

Each storage director can be connected to two device controllers. Only one device controller can communicate with a storage director at any time. The DDCV card:

- Connects the Device Data Bus Out and the Device Tag Bus Out bits to the device controller
- Connects the Device Data Bus In to the data transfer data (DXD) and port adapter (CMCD) cards
- Connects the Device Tag Bus In bits 0 and 1 to the storage director microprocessor (SDM) card
- Synchronizes the sync-in pulses to the control interface clock pulses
- Transfers data between the port adapter (CMCD) card or the data transfer data (DXD) card and the device controller
- Transfers device tag and control information between the storage director microprocessor (SDM) card and the device controller
- Transfers error correction and status information from the device controller to the SDM card

Device Counter (DCT) Card

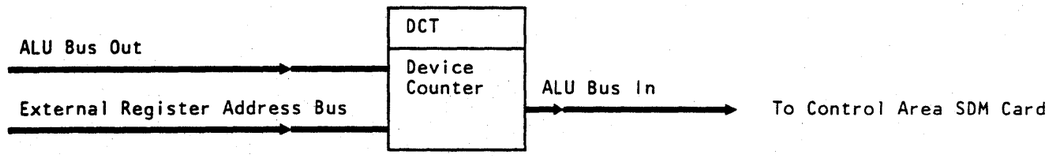
The DCT card:

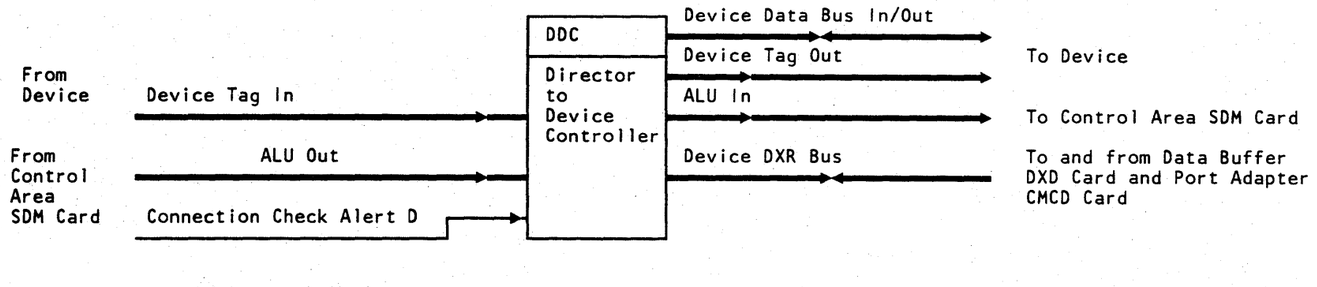
- Counts the number of data bytes transferred between the director-to-device controller card and the device controller
- Informs the microprocessor (SDM) card when the data byte count equals zero
- Controls the wait, process, and status pending indicators on the operator panel
- Selects read-only storage (ROS) on the storage director microcontroller (SDM) card
- Controls the interval timer on the clock (CLK) card
- Selects the external registers on the DDC and the DCT cards
- Contains the storage director identification (SDI) switches
- Sends the storage director identification to the SDM card
- Contains a pad counter

Card to Card Data Flow

Data sent to a device flows through the control interface area. Data between the device and the device DXR bus (to the DXD and CMCD cards) flows through the DDCV card. This data flow and the Device Tag Bus Out is controlled by the SDM card in conjunction with the Device Tag Bus In lines and the DDCV card.

The DCT card counts the number of data bytes transferred, and informs the microprocessor (SDM) card when the data byte count equals zero.





Card Descriptions

The maintenance connection functional area contains the following cards:

- Maintenance device adapter register (MDAR) card
- Maintenance device adapter control (MDAC) card
- Driver receiver (DRR) card
- Maintenance (MNT) card

Maintenance Device Adapter Control (MDAC) Card

The MDAC card:

- Controls and times which storage director is connected first to the diskette drive during initial microcode load (IML). An IML is performed on only one storage director at a time.
- Provides an IML timeout counter and controls.
- Controls the transfer of data to and from the MD and to and from a storage director for the various maintenance operations that can be performed from the MD.

Maintenance Device Adapter Registers (MDAR) Card

The MDAR card:

- Serializes and deserializes data to be transferred to and from the MD over the MD–MDA serial interface.
- Provides registers for storing:
  - Commands from the MD
  - Data from the MD or from a storage director
  - Control storage addresses from the SDM.
  - Control storage addresses from the MD.
  - Information about MD and storage director check and status
- Decodes commands from the MD.
- Provides gating for transferring the content of registers to or from the MD or a storage director.

Driver Receiver (DRR) Card

The DRR card:

- Gates IML data and control signals from the diskette drive to the selected storage director's ALU In.
- Gates the maintenance signals from the MD to the storage director to which the MD is connected.
- Connects the initiating (failing) storage director and the alternate (non–failing) storage director together for transmitting and receiving error data from the FRU and error registers.
- Ensures that the failing storage director will not hang when the alternate (non–failing) storage director is too busy to return Error Alert Response.

Maintenance (MNT) Card

The MNT card:

- Contains the interrupt level register (ILR) that indicates the interrupt level at which the storage director is operating, the last level at which the storage director was operating, and the interrupt levels that are allowed
- Connects the maintenance connection to the storage director microprocessor (SDM) card
- Disconnects maintenance connection from the SDM card
- Connects the failing storage director and the responding storage director together
- Stores and transfers error condition information from the failing to the receiving storage director
- Connects the diskette drive to the SDM card
- Controls the transfer of data from the diskette drive to the static control storage (SCS) and to the dynamic control storage (DCS) cards
- Controls the clock (CLK) card
- Contains storage director reset functions
- Executes maintenance commands received from the MD

Data Flow

IML Read/Write serialized data is transferred between the functional diskette and the MDAR card. IML Read data is deserialized and sent to the connected storage director by way of the DRR and MNT cards. IML Write data is transferred in the opposite direction.

MD data is transferred in the same manner as the IML data.

Error Data

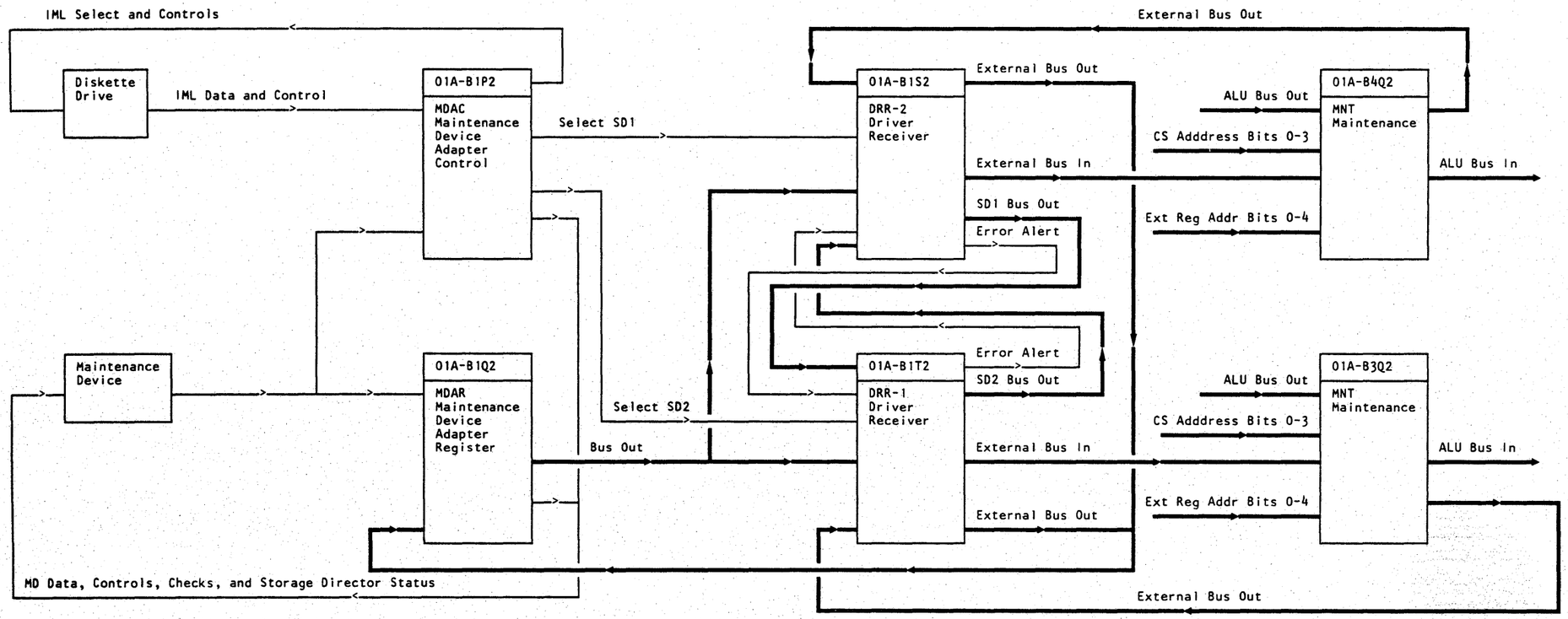
Error information is transferred from a failing storage director. This information is assembled and sent to the host for EREP or console message posting.

The error information is gated through the DRR card to the DRR, and MNT cards in the other storage director. The MNT card then transfers the data to the SDM card.

Address Stop

The MDAR and MDAC cards perform an address compare/address stop function. The address enters serially from the MD to the MDAR card and is compared to the SDM control storage addresses. The MNT card is notified of a successful compare.

Model 23 Maintenance OPER 125



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Read/Write and Control Commands

Note: For more detailed information on channel commands, see the *IBM 3880 Storage Control Model 23 Description*, GA32-0083.

The 3880 Model 23 storage directors recognize the standard Count Key Data architecture commands and the Count Key Data Extensions architecture commands. The 3880 Model 23 also supports commands applying uniquely to the caching function.

The 3880 Model 23 supports the following commands:

Read

- Read device characteristics
- Read home address
- Read R0
- Read count
- Read data
- Read key and data
- Read count, key and data
- Read multiple count, key and data
- Read IPL
- Read sector
- Diagnostic read home address

Write

- Write home address
- Write R0
- Erase
- Write count, key and data
- Write data
- Write key and data
- Diagnostic write home address
- Write count, key and data next track
- Write update data
- Write update key and data

Control

- No operation
- Seek
- Seek cylinder
- Seek head
- Recalibrate
- Space count
- Restore
- Set file mask
- Set sector
- Set path group identifier
- Suspend multipath reconnection
- Define extent
- Locate record
- Set subsystem mode
- Diagnostic control

Sense

- Test I/O
- Sense
- Sense ID
- Read and reset buffered log
- Device reserve
- Device release
- Unconditional reserve
- Sense path group identifier
- Diagnostic sense/read
- Sense subsystem status
- Sense subsystem counts

Search

- Search home address equal
- Search ID equal
- Search ID high
- Search ID equal or high
- Search key equal
- Search key high
- Search key equal or high

Cache Format and Read Operations

Cache Format

The cache is divided into areas called track slots, a track slot is an area of cache allotted for a DASD track.

Valid track images may exist, in cache, in any of three formats:

- As a full track image with all data continuous from home address to index. This is created when the transfer starts immediately following index.
- As a partial track image with all data from the first count field encountered to index. This is created when the transfer starts on a count field and terminates at or before index.
- As a full track in two parts. This is created when part of a track is in cache and the system wants data from the part of the track that is not in cache.

Read Operations

A command chain is considered a read command chain if it contains a search, a read (other than Read Sector or Space Count command) and no write commands.

Read CCW chains in normal cache replacement operate as follows:

- If the track required is in cache (read hit) data flow will be between cache and the channel.
- If the track requested is in cache but the record is not, a front-end promotion will occur and then the operation will continue from cache.
- If the track requested is not in cache (read miss), the data will be read from DASD. The track that caused the read miss will be transferred to cache concurrent with the transfer to the channel.
- The directory entry for a track in cache that has been accessed by the channel will be made most recently used.
- Read chains that access only DASD, Read IPL, and Space Count will not cause promotion.

Front-end Promotion

If a partial track is in the cache but the record requested is not, the following will happen:

- Channel Command Retry will be used while the device is oriented to index and the remainder of the track will be transferred to cache.
- The transfer will start at home address and continue to the start of the partial track. The data will be transferred to the same track slot, immediately following the partial track in the track slot.
- The storage director will reconnect to the channel when the transfer is complete and process the command as a read hit.

Model 23 Cache Format and Read Operations OPER 205

Read Home Address Command

A Read Home Address (X'1A' or X'9A') command causes the five bytes (FCCHH) of the home address area to be transferred from the device to the channel. The validity of the data is verified by the correction code bytes following the home address area.

A Read Home Address does not have to be preceded by any other command in order to be executed.

Read R0 Command

The Read R0 (X'16' or X'96') command causes the storage director to transfer the count key and data areas of record 0 from the device to the channel.

Read Count Command

A Read Count (X'12' or X'92') command causes eight bytes, CCHHRKDD, of the next count area on a record (excluding record 0) to be transferred from the device to the channel. Upon receipt of a Read Count command, the microprocessor issues a read gap 3 tag. After clocking over gap 3, the count area is read and transferred to the channel.

A Read Count command does not have to be preceded by any other command in order to be executed.

Read Data Command

A Read Data (X'06' or X'86') command causes the data area of a record to be transferred from the device to the channel. Upon receipt of a Read Data command, the microprocessor issues a read gap 2 tag. After clocking over gap 2 and the key area, the data area is read and transferred to the channel. The data area to be read is:

- The record following the next count area (excluding record 0)
- The command chained from the count or the key area located on the same record as the data area

A Read Data command does not have to be preceded by any other command in order to be executed.

Read Key-Data Command

A Read Key-Data (X'0E' or X'8E') command causes the key and the data areas of a record to be transferred from the device to the channel. The key and data areas to be read are one of the following:

- The key and the data areas of the record following the next count area (excluding record 0)
- The key and the data areas command chained from the count area located on the same record as the key and the data areas
- A Read Key-Data command is set up, transfers data, and ends data transfer exactly the same as the Read Data command.

Read Count-Key-Data Command

A Read Count-Key-Data (X'1E' or X'9E') command causes the entire next record (excluding record 0) to be transferred from the device to the channel.

A Read Count-Key-Data command is set up, transfers data, and ends data transfer the same as the Read Count and read data commands.

Read Multiple Count-Key-Data Command

A Read Multiple Count-Key-Data (X'5E') command causes the remaining records on a track (excluding record 0) to be read from the device to the channel. Reading starts at the count field of the next record and is completed in one revolution of the disk. When the end of each record is reached, the microprocessor issues the tags necessary to read the next count, key, and data areas.

The result is similar to a chain of Read Count-Key-Data commands, with the following exception. When the last record on a track is read during a Read Count-Key-Data chain, and there are still other Read Count-Key-Data commands in the chain, the next command clocks over the home address and record 0 and reads the next record. In the case of the Read Multiple Count-Key-Data command, when the last record on a track is read, the storage director generates channel end and device end.

A Read Multiple Count-Key-Data command is set up, transfers data, and ends data transfer the same as the Read Count and Read Data commands.

Read Initial Program Load Command

A Read Initial Program Load (X'02') command causes the data area of record 1, cylinder 0, to be transferred from the device to the channel.

A Read IPL command is set up, transfers data, and ends data transfer the same as the Read Data Command.

Read Sector Command

A Read Sector (X'22') command causes one byte of angular position information to be transferred from the device to the channel.

Diagnostic Read Home Address Command

The Diagnostic Read Home Address (X'0A') command causes the storage director to transfer all of the bytes of the home address sub-area from the device to the channel.

Write Operations

To insure that the DASD copy of the data is always valid, all write commands operate directly with the DASD.

A command chain is considered a write chain if any command is a write.

The general rules for write operations are:

- No new tracks are promoted to cache as a result of write command chains.
- All write commands operate with the device. To maximize cache performance, if the requested data is in the cache the 3880 will either concurrently transfer the data to the cache or invalidate the cache copy.
  - Update writes will concurrently transfer the data to the cache.
  - Format writes will invalidate the cache copy.
- All other tracks modified by a write command chain are invalidated.
- Tracks are not made most recently used.

Write Home Address Command

The Write Home Address command (X'19') causes five bytes (FCCHH - flag, cylinder, and head address) to be written on the selected track. When index is located, a type 1 gap is written, then the home address field is written. If the Write Home Address command is not followed by a Write R0 command, the balance of the track is padded with zeros.

This command must be chained from a successful Search Home Address Equal command or have the flag byte, bit 6, set to 1, to flag a defective track. If not, channel end, device end, and unit check are presented in ending status and command reject (sense byte 0, bit 0) is set. The Set File Mask command requirements must be met.

If the channel byte count is less than five, zeros are written to fill out the field. If the channel count is more than five, only the first five are written.

Write Record Zero Command

The Write Record Zero (R0) (X'15') field is normally the track descriptor record but can be used to contain customer data. The format is the same as the Write Count-Key-Data command.

This command must be chained from a Write Home Address or a Search Home Address Equal command in which the CCHH bytes were equal.

Erase Command

The Erase command (X'11') operates the same as the Write Count-Key-Data command except that the data from the channel is not transferred to the device and the device writes pad bytes to index.

The Erase command cannot be chained to another Erase command nor can it be chained to other write commands.

Write Count-Key-Data Command

The Write Count-Key-Data command (X'1D') causes an entire record (count area, key area, and data area) to be transferred from the host and written on the selected device.

This command is chained from a Write R0, another Write Count-Key-Data, or from a Search ID Equal or a Search Key Equal command that has compared equal on all bytes of the searched field recorded on the track. A Read Data or a Read Key-Data command may be inserted between a Search ID Equal command and the Write Count-Key-Data command. A Read Data command may be inserted between a Search Key Equal command and the Write Count-Key-Data command. The last search command establishes these prerequisites for the write command. If the prerequisites are not satisfied, unit check, channel end, and device end are presented in ending status with command reject (sense byte 0, bit 0).

The first eight bytes CCHHRKDD (cylinder, cylinder, head, head, record, key length, and data length, data length) sent from the system storage are for the count area. The balance of the count area bytes are generated by the storage director. The remaining bytes of data are for the key and data areas as specified by key and data length bytes. After the correction code bytes for the data area are written, channel end and device end status are presented. If the amount of data from the channel is less than the field length, zeros are padded to fill the field.

Write Data Command

The Write Data (X'05') command is the normal updating command for the data field. The Write Data command must be chained from a Search ID Equal or a Search Key Equal command in which all bytes of the searched field are equal. If not, command reject (sense byte 0, bit 0) is set.

If the channel data is less than the data length, the field is padded with zeros.

The Write Data command microcode is the same as the data field for a Write Count-Key-Data command.

Write Key-Data Command

The Write Key-Data (X'0D') command is the normal updating command for the key and data fields. A Write Key-Data command must be chained from a Search ID Equal command that has compared equal on all five bytes of the ID. If not, command reject (sense byte 0, bit 0) is set.

The Write Key-Data command microcode is the same as the key and data field for a Write Count-Key-Data command.

Diagnostic Write Home Address Command

The Diagnostic Write Home Address (X'09') command causes 28 bytes of data to be transferred from the channel to the home address area of a track. This command is normally used by a utility program to assign new surface defects for a track.

Write Count-Key-Data Next Track Command

The Write Count-Key-Data Next Track command (X'9D') causes an entire record (count area, key area, and data area) to be transferred from the host and written on the selected device.

This command must be chained from a Write Count-Key-Data, or from a Write Count-Key-Data Next Track command. The command causes the device to, switch to the next track, verify the home address and record zero, and then proceeds to the same track as the Write Count-Key-Data command.

Write Update Data Command

The Write Update Data Command (X'85') causes the specified data to be transferred from the channel to the data area of a record on the device.

Write Update Key and Data Command

The Write Update Key and Data Command (X'8D') causes the specified data to be transferred from the channel to the key and data areas of a record on the device.

No-Operation Command

The No-Operation command (X'03') causes no physical action to be performed. The command causes the storage director to lose head-to-track orientation. Channel end and device end are presented in initial status.

Seek and Seek Cylinder Commands

The Seek (X'07') and Seek Cylinder (X'0B') commands transfer six bytes of address information to the microprocessor.

If less than six bytes are transferred, or if any of the six bytes are not valid, command reject (sense byte 0, bit 0) is set with unit check in ending status. If bus out parity is detected, unit check is set in ending status with bus out parity (sense byte 0, bit 2). Any transfer error prevents the seek from taking place. With no transfer errors, channel end and device end are returned to the channel.

No seek action takes place until a Set Sector, read, search, Write Home Address, or Space Count command is received by the microprocessor.

When the seek is started, the storage director sends control information to the device. The device controller controls the access motion (if required) and signals the microprocessor when the seek is complete and the next required action can be executed.

Seek Head Command

The seek address is transferred to the storage director as in a Seek command. No access motion is started even if the address is not the same as the last seek address.

Recalibrate Command

The Recalibrate command (X'13') causes the microprocessor to transfer information to move to cylinder zero and to select head zero to the selected device controller.

Initial status returned to the channel is zero. Ending status is channel end and device end.

Space Count Command

If a seek has been received but not executed, retry status is presented to the channel and the device starts the seek. At the end of the seek operation, device end is presented to the channel. The channel re-issues the Space Count command (X'0F'). The Space Count command transfers three bytes (KI, DI, DI) from the channel to the microprocessor as the count field is clocked over.

The Space Count command is used to recover from a bad count field.

If the Space Count command is chained from a Read, Search, Write, or Space Count command, the microprocessor causes the selected device to clock to the next count field and then presents device end to the channel.

If not chained as described above, the Space Count command causes the microprocessor to control the selected device to wait for an index, clock to the end of the R0 count field, and present device end to the channel. Command reject (sense byte 0, bit 0) is set if a Space Count command is chained from a Write or Erase command or if a Write, Erase, Set File Mask, Read IPL, Device Reserve, or Device Release command is issued in the chain following the Space Count command.

Invalid track format (sense byte 1, bit 1) is set if index is detected before the Space Count command is completed.

Restore Command

The Restore command (X'17') is not used by devices attached to the storage director and is treated as a No-Operation command. Initial status of zero is followed by channel end and device end in ending status.

Set File Mask Command

The Set File Mask command (X'1F') transfers one byte of control information from the channel to the microprocessor. This byte defines the write, seek, and command retry to program control interrupt (PCI) interaction.

If more than one Set File Mask command is issued in a chain of CCWs, channel end, device end, and unit check are returned in initial status and command reject (sense byte 0, bit 0) is set.

The file mask byte contains the following:

Contents	Description
Bit 0,1	
00	Inhibit only Write Home Address and R0
01	Inhibit all Write commands
10	Inhibit all format Write commands
11	Permit all Write commands
Bit 3,4	
00	Permit all Seek commands
01	Permit Seek Cylinder and Seek Head commands
10	Permit Seek Head command
11	Inhibit all Seek commands
Bit 7	
0	Not PCI fetch mode
1	PCI fetch mode

Note: Bits 2 and 6 must be zero or unit check and command reject (sense byte 0, bit 0) are set.

Set Sector Command

The Set Sector (X'23') command transfers one byte of information from the channel to the microprocessor. If the information is valid, channel end is presented to the channel in initial status. The channel indicates chaining and disconnects from the storage director. If not, channel end, device end, and unit check are presented to the channel and command reject (sense byte 0, bit 0) is set.

If a seek command has been received but not executed, it is started by the microprocessor at this time. The selected device executes the seek. The microprocessor transfers the angular position information provided by the byte from the channel to the device. When the device has reached the sector selected, the storage director activates Request In to the channel. If the channel does not respond in time, Request In is deactivated and activated on the next revolution. If the channel responds, device end status is presented and the next command is ready to be received.

If the byte transferred is zero, Request In is activated at the index. If the byte transferred is 255, the storage director presents channel end and device end in ending status and no operation (including seeks) is executed.

Set Path Group Identifier Command

The Set Path Group Identifier (X'AF') command establishes the path group identifier and sets or changes the path state of the channel interface over which the storage director is receiving.

Suspend Multipath Reconnection Command

The Suspend Multipath Reconnection (X'5B') command caused the storage director to perform the associated CCW chain in single-path mode on the path over which the command was received.

Define Extent Command

The Define Extent (X'63') command causes parameter bytes to be transferred from the channel to the storage director. The parameter bytes define limits on subsequent operations in the channel program, provide a block size value for use by following commands, and indicate global access intent information.

Locate Record Command

The Locate Record (X'47') command causes parameter bytes to be transferred from the channel to the storage director. These bytes specify the location and number of records or tracks to be processed and the operation to be performed by following data transfer commands within the command chain.

The execution of a Locate Record command establishes a span of control or domain for data transfer commands that are chained from the Locate Record command.

Set Subsystem Mode Command

The Set Subsystem Mode command (X'87') causes the storage director to make the subsystem storage available or unavailable to the subsystem or the storage director.

Following presentation of initial status, the storage director receives two bytes from the channel. These bytes indicate the function to be performed and have the following format:

Bits 0,1,2	Operation
0 0 0	No operation
0 0 1	Activate cache
0 1 0	Deactivate cache
0 1 1	Make subsystem storage available to subsystem
1 0 0	Make subsystem storage unavailable to subsystem

Bits 3 through 15 are reserved and must be 0.

Diagnostic Control Command

The Diagnostic Control Command (X'F3') is used to prevent further write operations on a path with a permanent write error. The Diagnostic Control command causes the internal microcode to inhibit write operations on paths with permanent write errors.

Test I/O

The Test I/O with command X'00' causes the microprocessor to transfer the status of the addressed device to the channel. This command is an immediate command and sends the status to the channel in the initial status byte.

Sense information stored by the microprocessor is not changed unless a unit check occurs during execution of this command.

Sense Command

The sense command (X'04') causes the microprocessor to transfer 24 bytes of sense data from control storage to the channel. The sense data bytes identify the error, or condition, of the selected storage director and or device. See the SENSE section for a description of sense data.

The channel may request less than 24 bytes, but not more than 24 bytes.

Channel end and device end are generated and sent to the channel after the transfer, and the sense data is reset.

The Sense command setup, transfer of information, end of transfer, and error recovery are the same as for the Sense I/D command except that 24 bytes are transferred.

Sense I/D Command

The Sense I/D command (X'E4') causes the microprocessor to transfer seven bytes of type and model information on the addressed storage director and device to the channel. The information transferred has the following format:

Byte	Description
0	X'FF'
1,2	Storage director type number (X'3880')
3	Storage director model number (X'CB')
4,5	Device type number (X'3380')
6	Device model number (X'02')

The channel may request less than seven bytes, but not more than seven.

Read And Reset Buffered Log Command

The Read and Reset Buffered Log command (X'A4') causes the microprocessor to transfer 24 bytes of usage and or error data from control storage to the channel. The usage and or error bytes are the same as for sense data when the usage and or error counters overflow.

The channel may request less than 24 bytes, but not more than 24 bytes.

The Read and Reset Buffered Log command setup, transfer of information, end of transfer, and error recovery are the same as for the Sense I/D command except that 24 bytes are transferred.

Device Reserve Command

The Device Reserve command (X'B4') causes the microprocessor to execute a sense command (X'04') and then to reserve the selected device to the channel issuing the command.

The setup, transfer of information, end of transfer, and error recovery for the Sense command part of a Device Reserve command are the same as for the Sense I/D command except that 24 bytes of sense data are transferred.

The reserving of a device to a channel occurs in the storage director. The microprocessor notes the reservation in control storage.

The device is reserved until released by a Device Release command or until a system reset on the same channel occurs.

If the selected device is on a string that has a string switch feature, the reserve command has to inform the string switch attachment in the device controller to reserve the selected device.

Device Release Command

The Device Release command (X'94') causes the microprocessor to execute a Sense command (X'04') and then to release the selected device from the issuing channel.

The setup, transfer of information, end of transfer, and error recovery for the Sense command part of a Device Release command are the same as for the Sense I/D command except that 24 bytes of sense data are transferred.

The releasing of the reservation by a channel takes place in the storage director. The microprocessor resets the reservation in control storage.

If the selected device is on a string that has the string switch feature, the release command has to signal the string switch attachment in the device controller to release the selected device.

Unconditional Reserve Command

The Unconditional Reserve command (X'14') executes the same functions as the Reserve command. In addition, if the addressed device is reserved to another storage director, the reservation is broken and set to the new path. This breaking of the active reservation takes place even if the device path is in use.

This command is normally used to recover from a failure of the reserved storage director to respond to commands.

The Unconditional Reserve command must be the first in a chain or channel end, device end, and unit check status with command reject, sense byte 0, bit 0, are presented.

Sense Path Group Identifier Command

The Sense Path Group Identifier command (X'34') transfers information from the storage director to the channel describing the path group identifier and the current path state.

Diagnostic Sense/Read Command

The Diagnostic Sense/Read command (X'C4') transfers the contents of the Trace/Dump buffer from the storage director to the channel.

Following presentation of initial status, the storage director sends the Trace/Dump information to the channel. The maximum number of bytes that this command can transfer is 8192.

Sense Subsystem Status Command

The Sense Subsystem Status command (X'54') causes information describing the status of the subsystem to be transferred to the channel. The status information is described as follows:

Byte	Description
0,1	Identify the storage director and device that are associated with the I/O request
2	Must be 0
3	Must be 0
4-5	Overall caching status
6-9	Device caching status
10-13	Configured subsystem storage capacity
14-17	Available subsystem storage capacity
18-21	Not used
22-25	Offline subsystem storage capacity
26-39	Are always 0

Sense Subsystem Counts Command

The Sense Subsystem Counts command (X'74') causes the storage director to transfer subsystem counts to the channel without affecting the value of the subsystem counts.

Read Device Characteristics Command

The Read Device Characteristics command (X'64') transfers 64 bytes of device characteristics of the addressed device from the storage director to the channel.

Search Commands

The search commands locate records on the selected device. Information from the channel and information from the device are compared until the data requested is located.

At the end of each field read, the validity of the data is checked. If invalid, device end and unit check status with data check (sense byte 1, bit 0) are presented to the channel. A detection of bus out parity on the channel data causes device end and unit check with bus out parity (sense byte 0, bit 2). If a seek command is received but not started, retry status is indicated to the channel in initial status and the seek is completed.

Search commands do not have to be preceded by any other command to be executed.

Search Home Address Equal Command

The search is started at the index and compares the home address ID (CCHH) bytes. All four bytes must be equal.

If the multitrack bit is off, the search stays on one track and ends when the index is read the second time; if the multitrack bit is on, the head is switched at the index and the search continues as long as the command is repeated.

At the end of each home address field read, without errors, channel end and device end are presented to the channel. The status modifier bit is presented if the search condition is met.

Search Id Equal Command

The Search ID Equal command (X'31' or X'B1') is the same as the Search Home Address Equal command except for the fields read and the comparisons made.

Search Id High Command

The Search ID High command (X'51' or X'D1') is the same as the Search Home Address Equal command except for the fields read and the comparisons made.

Search Id Equal or High Command

The Search ID Equal or High command (X'71' or X'F1') is the same as the search Home Address Equal except for the fields read and the comparisons made.

Search Key Equal Command

The Search Key Equal command (X'29' or X'A9') is the same as the Search Home Address Equal command except for the fields read and comparisons made.

Search Key High Command

The Search Key High command (X'49' or X'C9') is the same as the Search Home Address Equal command except for the fields read and comparisons made.

Search Key Equal or High Command

The Search Key Equal or High command (X'69' or X'E9') is the same as the Search Home Address Equal command except for the fields read and the comparisons made.

Disconnected Command Chaining

Disconnected command chaining

- Allows the storage director to disconnect from the channel on commands that require long delays because of mechanical motion or searches. The channel is free during the delay period.
- Enables multiple requesting, which allows up to 32 separate command chains to be active in the facility.
- Allows the storage director to disconnect from the channel after an operation has started even though chaining is indicated.

The storage director can disconnect between Channel End and Device End. This disconnecting reduces the system interrupts needed to overlap channel data transfers with the mechanical motion of the devices. The storage director retains the information necessary to control a disconnected CCW chain for each drive attached.

Note: This is also referred to as multiple requesting.

Status Information

The status byte (eight bits) notifies the channel of the condition of the storage director and the selected drive. Status is presented twice (initial and ending) for all storage director commands except Set Sector, Test I/O, and No Operation commands.

Except when the sector value equals 255, status is presented at the following three times during the Set Sector command. (When the sector value equals 255 only Device End is presented.)

- Initial.
- Channel End after data transfer from the channel.
- Device End after the device has reached the desired position.

Status is presented once (initial) containing Channel End and Device End on immediate commands (No-Op) except when chained after a write command. In this case, a second status byte (ending) is also transmitted.

A No-Op is processed as an immediate command only if the storage director is not writing or erasing. Channel End and Device End are indicated in the initial status byte (one status byte only). If the unit is writing or erasing, a zero is transmitted in the initial status byte. Channel and Device End are indicated in the ending status byte when the storage director finishes writing or erasing.

Status Bits

The eight status bits are described below.

Bit	Name	Function
0	Attention	Not used.
1	Status modifier	Used with channel end, device end, busy, and unit check bits.
2	Control unit end	The storage director has finished an operation.
3	Busy	The address referred to by the channel is busy. Also used in conjunction with the status modifier to indicate control unit busy.
4	Channel end	The storage director has received all the data needed to do the operation called for and the channel is free.
5	Device end	Indicates that an access mechanism is free to be used.
6	Unit check	Indicates that an unusual or error condition has been detected. With the status modifier, it means command retry is requested.
7	Unit exception	End of file.

Attention

The attention status bit (bit 0) is not used.

Status Modifier

The status modifier bit (bit 1):

- Is set when all search type commands are completed and the condition satisfied.
- Indicates control unit is busy, when it is on in conjunction with the busy bit. When it is on with the channel end, device end, and unit check bits, it indicates retry of the last channel command. The storage director and drive are ready for immediate retry.
- Indicates retry of the last channel command, when it is on in conjunction with the unit check bit.

  When it is on with the channel end bit, it indicates retry of the last channel command. The storage director and drive are not ready for the retry procedure.

Control Unit End

The control unit end bit (bit 2) is set when a control unit busy was generated previously and the busy condition is terminated.

Busy

The busy bit (bit 3):

- Is set when a new command chain is initiated while the selected access mechanism is still in motion because of a previous seek command.
- Sets in response to any command except Test I/O if there is outstanding status for the device.
- Sets when a new command chain is initiated while the storage director is causing a track to be erased following a write command or an erase command.
- Indicates that only the selected device is busy if the status modifier is off.
- Indicates control unit busy if it is on in conjunction with the status modifier (bit 1).

Channel End

The channel end bit (bit 4) is set when the channel portion of the operation is complete.

Device End

The device end bit (bit 5):

- Is set when a device is ready after a seek has been completed.
- Is set when the record is ready to be operated on after a set sector command.
- Is set when an attached device goes from a not ready to a ready condition.
- Is set simultaneously with the channel end bit at the end of all other commands.
- Indicates that an access mechanism is free to be used.
- Indicates control unit is ready to restart a disconnect command retry.

Unit Check

The unit check bit (bit 6):

- Is set whenever an unusual or error condition on the selected drive is detected in the storage director.
- Indicates command retry is requested if it is on in conjunction with the status modifier bit.
- Indicates a system interrupt condition if the status modifier bit is not on and channel end (bit 4) and/or device end (bit 5) is included in the status. The sense bytes provide detailed information about the condition.

Unit Exception

The unit exception bit (bit 7):

- Is set when the data length in the count field is zero.
- Indicates that an end of file was detected. Bit 7 is not set for a Read Count, Write Count-Key-Data, Search Key, or Search ID command. The key field, if any, is transferred.

Status Information

The initial status byte is zero for all commands other than No Operation and Test I/O unless one or more of the following conditions exist. If more than one condition exists, the first condition listed determines the initial status byte:

1. The initial status indicates control unit busy (bit 3) if the selection occurs and if:
   a. Writing is still in progress after chaining is terminated.
   b. An operation is still in progress after a Halt I/O instruction occurs.
   c. The storage director is disconnected during command chaining with writing in progress or with a storage director error recovery procedure in progress.
   d. The storage director is executing a diagnostic test.
   e. A status condition is pending in the storage director for other than the addressed device.
   f. A system reset sequence is in progress.
   g. The storage director is maintaining a contingent allegiance to some device other than the addressed device.
2. A status condition, pending in the storage director is associated specifically with the addressed device or is not associated with any specific device. In this case, the pending status is presented as initial status, and the busy bit is included in the status byte if the command byte is other than Test I/O. The busy bit indicates that the device is busy because of the outstanding status. The pending status is cleared unless it is stacked by the channel. After the status is cleared, the device must be readdressed to determine if the device is available.
3. The device is busy to the interface, in which case the busy bit appears alone in the initial status byte. The device is busy to the interface if channel end occurred without device end for the device, and device end has not yet been generated; or if the device is attached to a controller with the string switch feature and is reserved to the other side of the switch. Discussion in this paragraph does not apply to cases where busy (pending status) occurs with other status bits. When the busy bit occurs with bits other than the status modifier bit, the device is defined to be busy because of the included status, which is outstanding.
4. Status pending in the device. The pending status is presented as initial status, and the busy bit is included if the command is other than Test I/O. The pending status is cleared unless it is stacked by the channel.
5. A unit check condition exists at the device or storage director. Unit check occurs in initial status. Valid commands in the Sense group (xxxx0100) are an exception and receive zero status so that the commands may be executed. This permits transferring of the sense indicators.
6. Initial status indicates command retry.
7. Invalid parity is sensed in the command byte. Unit check occurs.
8. The command is rejected. Unit check occurs. (Not all command rejects occur in initial status however.)

Pending Status Conditions

A pending status condition may exist in either the storage director or device.

Status Pending In The Storage Director

A status condition pending in the storage director, other than control unit end, causes the storage director to appear busy for all devices except the device for which the status condition exists. If the storage director is not busy to the interface, the Request In line is activated, and Select Out and Suppress Out are deactivated. A pending control unit end may cause the storage director to appear busy to all except one device address on the interface for which it is pending. Status pending in the storage director is cleared when it is presented and accepted.

Note that status cannot be cleared from the storage director by a Test I/O if the storage director is busy to the interface.

Status is pending in the storage director if:

1. An interface disconnect was signaled after a command was given but before channel end was accepted by the channel for the command. The ending status for the operation is pending when the operation is complete.
2. Status containing busy, channel end, or unit check was stacked by the channel, or blank status in response to a Test I/O was stacked. The stacked status is pending in the storage director for the device with which the stacking occurred.
3. Control unit busy was presented to the interface. Control unit end is pending for the interface and is included with other status pending in the storage director, if any.
4. A unit check was found to be associated with an operation where device end has already been cleared. Unit check and control unit end are pending in the storage director.

Address Associated With Pending Status

All status conditions in the device are associated with a specific device address, except for control unit end. However, when in the contingent allegiance state, control unit end is associated with a specific address, and that address is the last address presented on the interface by the storage director. When no contingent state exists, the control unit end is associated with the smallest numerical address, which is not command chaining on any interface.

Status Pending In The Device

A status condition pending in the device causes the Request In line to be activated on the interface if the device and storage director are available (not busy), Select Out is deactivated and no contingent allegiance exists in the storage director. Status pending in the device is cleared when status is presented and accepted. Status pending in the device cannot be cleared by a Test I/O if the device or storage director appear busy to the interface. The only status condition which can be pending in the device is device end. When unit check occurs with device end (and not channel end), it is not generated until the device end is presented on the interface and the device end and unit check conditions then become pending in the storage director if stacked. Status is pending if:

1. Channel end occurs alone for an operation. Device end is pending.
2. Busy status (busy bit alone) is presented. Device end is pending on the interface.
3. The device has gone from the not ready state to the ready state. Device end is pending.

Priority Of Pending Status Conditions

The priority of pending status conditions when presented via polling is:

1. Status pending in the storage director, other than control unit end.
2. Unsuppressible status conditions.
3. Suppressible device end status.
4. Control unit end status.

Note: During the contingent allegiance state, control unit end status assumes highest priority.

Command Retry

Command retry recovers from device errors such as data checks, access errors (seek checks), and overruns. It is also used for write padding errors and defective alternate tracks. These errors are not detected by the microcode, but are logged in the 3880 usage and/or error counters.

The retry consists of a status X'4A' (status modifier, channel end, and unit check) or a retry status generated by the 3880. The retry causes the channel to disconnect. The 3880 then reorients and repositions the device and generates device end. The channel replies to device end by re-issuing the command. This causes the operation to be retried. The retry is attempted up to 256 times for the 3380. If the retry is not successful, a permanent seek check is generated and sent to the system where the error recovery procedure (ERP) can be invoked.

Interrupts

Interrupts are controlled either by hardware or by microcode. The microcode controls the interrupt mechanism by setting appropriate bits in the interrupt level register (ILR). The interrupt levels and conditions are given below in order of priority from highest to lowest.

Level 0	Maintenance interface
Level 1	Timer overflow or channel check 1
Level 2	Channel selection or device count less than 64
Level 3	Normal subsystem operation and levels 0, 1, and 2 are inactive

At the end of execution of every microinstruction, the microprocessor monitors the request for an interrupt level status. If an interrupt request exists, fetch and execution of microinstructions stop. The microprocessor automatically initiates a sequence to store the program status word (PSW) of the current level of program execution. Each PSW is stored in a specified area within the internal registers according to its interrupt level. When the current PSW is stored, the hardware automatically fetches the PSW for the level at which the program is to resume.

On machine reset, the ILR is reset to zero, placing program execution at level 3.

Multiple Track Operation

Bit 0 of the command byte identifies a multiple track (M/T) operation. Multiple track is effective only on Read and Search operations.

If the M/T bit is on in a chain of commands, the head is switched to the next track at index time, providing the command is issued between the last record and the index. (If the storage director has issued a read G1 head switching operation to the controller, head switching occurs in the gap after index.) Multiple track eliminates the need for Seek Head commands in a chain of the read or search commands.

Head switching does not occur if bits 3 and 4 of the file mask are both on (file protected), or if the head address would advance past the last head (end of cylinder).

> **Note:** M/T search chains should be started with a single track Read HA or Read R0 to prevent missing the record if the record has passed the head when the M/T search is started.

End of File

End of file defines the end of a logical group of records. It is identified by a count field data length (DLDL) of zero. The data field consists of one byte of zero plus error correction code (ECC) bytes.

The microprocessor signals the system with unit exception status (status byte, bit 7) on Read IPL, Read R0, Read Count-Key-Data, Read Key-Data, Read Data, Write Key-Data, and Write Data commands.

Orientation

The storage director constantly monitors the relative position of the head and the format of the track. The storage director uses this orientation information to determine when to start an operation called for in a command. Orientation is maintained by the microprocessor in the command execution byte. As an operation is performed, the command execution byte is updated as each field of a record is passed.

Channel Interface

The channel interface provides a common connection between the channel and the storage directors. Selection lines are routed serially through each storage director to allow sequential connection to the channel. The information format and signal sequence are common to all storage directors.

The storage director remains attached to the interface until it transfers all information or until the channel signals to disconnect.

The storage control is designed to be used with the block multiplexer channels. In a block multiplex operation, the channel forces burst mode until Channel End time, but does not force burst mode between Channel End and Device End. The channel, by deactivating Select Out, allows the storage director to disconnect following the presentation of Channel End alone even though command chaining is indicated.

Description of Tag Out Lines

The Tag Out lines identify information on the bus out lines. This information remains active until an inbound tag responds.

Operational Out

Operational Out gates all outbound tag lines and is activated with processing unit power on reset. Operational Out is deactivated by the channel for system reset.

Hold Out

Hold Out controls the effect of Select Out, allowing additional channel control of polling. Hold Out is deactivated while Select Out is active which causes the polling sequence to be terminated.

Select Out

Select Out is used to select or poll a control unit. Selecting a control unit means activating Select Out and Address Out. Polling a control unit means activating Select Out without Address Out to enable a pending Request In.

Select Out is connected serially through each control unit. Selection priority is determined by board jumpers in a 3880 control unit. If selected, a control unit activates Operational In. If not selected, Select Out is propagated to the next control unit.

Address Out

Address Out identifies information on bus out as being a device address. Deactivating Select Out while Address Out is active forces a Halt I/O and the storage director disconnects from the interface.

Command Out

Command Out identifies information on bus out as a command. Command Out terminates the current operation when used as a response to Service In/Data In.

Command Out causes a storage director to stack status when used as a response to Status In.

Service Out

Service Out indicates the channel has accepted data on Bus In (read operation).

Service Out indicates the channel has provided, on Bus Out, the data requested by Service In (write operation).

Service Out signals a storage director that status was accepted when used as a response to Status In.

Data Out

Data Out indicates the channel has accepted data on Bus In (read operation).

Data Out indicates the channel has provided, on Bus Out, the data requested by Data In (write operation).

Bus Out

Bus Out transfers data, control, or address information to the processing unit.

Bus Out signals are valid when the identifying outbound tag is active.

Suppress Out

Suppress Out is used alone or with another tag to suppress status, suppress data transfer, chain command control, or cause a selective reset.

		SD1	SD2	
CTL-I		NOT USED	NOT USED	CTL-I
		BUS/TAG	BUS/TAG	
Channel A		BUS IN	BUS IN	Channel A
		TAG IN	TAG IN	
		BUS OUT	BUS OUT	
		TAG OUT	TAG OUT	
Channel B		BUS IN	BUS IN	Channel B
		TAG IN	TAG IN	
		BUS OUT	BUS OUT	
		TAG OUT	TAG OUT	
Channel C		BUS IN	BUS IN	Channel C
		TAG IN	TAG IN	
		BUS OUT	BUS OUT	
		TAG OUT	TAG OUT	
Channel D		BUS IN	BUS IN	Channel D
		TAG IN	TAG IN	
		BUS OUT	BUS OUT	
		TAG OUT	TAG OUT	

Tailgate as viewed from inside the machine.

3880 Control Interface Connectors
Connector Locations – 2 or 4 Channels

Description of the Tag In Lines

Information on the bus in lines is identified. This information remains active until an outbound tag responds.

Request In

Request In invokes a reselection sequence from the channel. This line is controlled by the microcode.

Request In indicates that the storage director is ready to present status.

Concurrent Request Ins from two or more storage directors are resolved by the channel.

Select In

Select In is the return path for Select Out. Select In indicates to the channel that a control unit was not selected.

Operational In

Operational In signals the channel that the storage director is selected and prevents another storage director from connecting to the interface blocks (blocks the propagation of Select Out).

Operational In remains active as long as the director is connected to the channel.

Address In

Address In identifies the information on bus in as being the device address.

Status In

Status In identifies information on Bus In as a status byte. Status In remains active until the channel activates Service (accept) or Command Out (stack).

Service In

Service In signals the channel when the selected device wants to transmit or receive data.

Service In remains active until the channel responds with Service Out, Command Out, or Address Out.

Data In

Data In signals the channel when the selected device wants to transmit or receive data.

Data In remains active until the channel responds with Data Out, Command Out, or Address Out.

Disconnect In

Disconnect In can be raised by a control unit only when is is connected to the channel (has Operational In up). Disconnect In is raised to inform the channel of an error condition in the control unit and the control unit is requesting a reset.

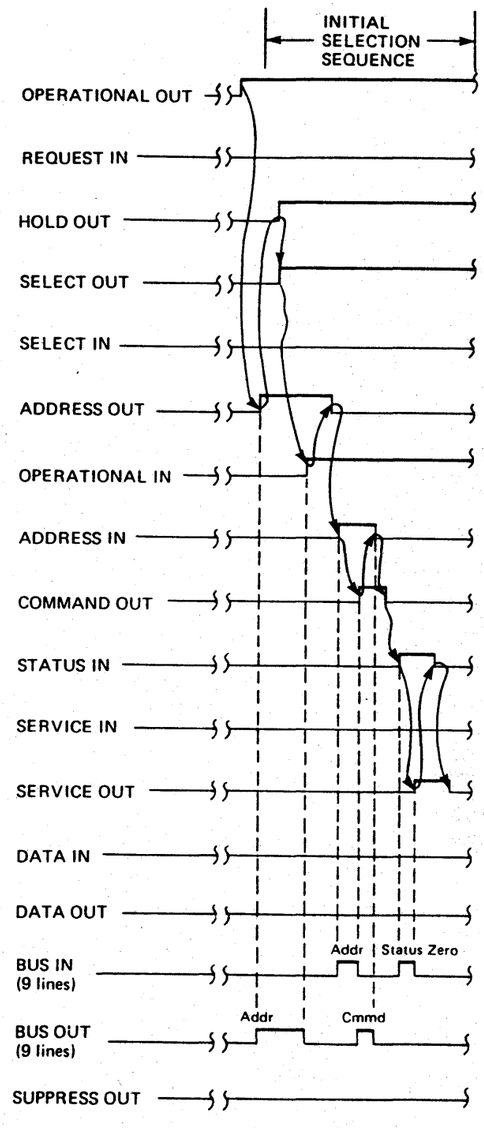
Mark 0 In

The control unit requests a command retry by raising Mark 0 In and Status In, while presenting unit check and status modifier together.

Bus In

Bus In transfers address, status, or data information to the channel. Bus In signals are valid from 100ns after the activation of an identifying inbound tag the activation of the responding outbound tag.

Bus In signals are valid when the identifying inbound tag is active.



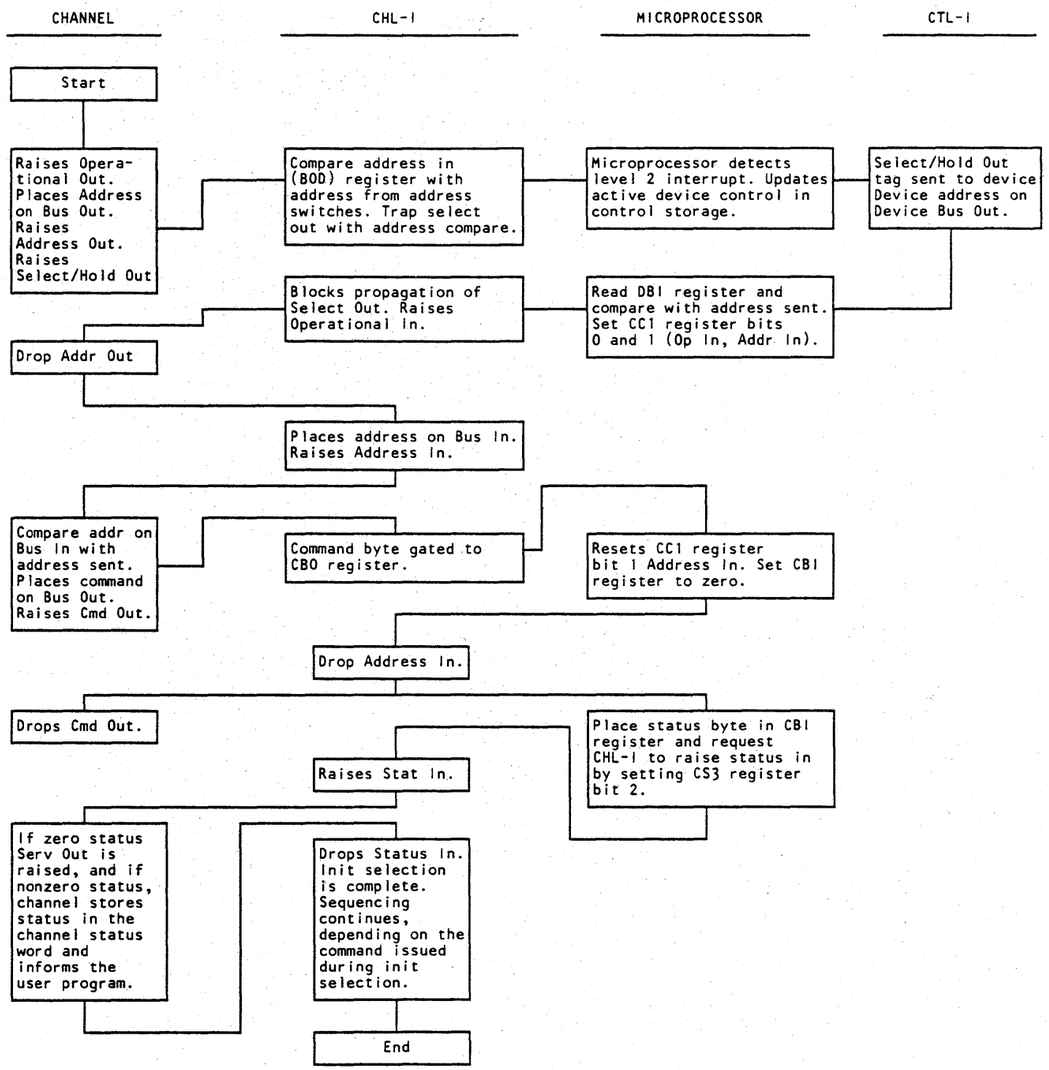
Initial Selection Sequence

Channel Initiated Sequence

When the channel needs access to data on a storage device, it initiates a selection sequence to a storage director that the device is attached to:

1. Operational Out, Hold Out, and Address Out are activated and an address byte containing the address of both, the storage director and the device, is placed on Channel Bus Out. This address byte is sent to all units on the channel.
2. Select Out is activated and sent to the first control unit on the channel.
3. Select Out is propagated to each succeeding control unit, allowing the address byte to be sent to each control unit.
4. Each control unit, in sequence, compares the address with its own address.
5. The control unit with the correct address traps Select Out and answers with Operational In, Address In, and its own address on Channel Bus In.
6. The channel checks the address returned and, if correct, activates Command Out.
7. After checking the device status, the microprocessor in the selected storage director activates Status In with status (normally zero) on Channel Bus In.
8. The channel activates Service Out to indicate acceptance of the status byte.

At this point, the microprocessor and device are ready to start decoding and executing the command.

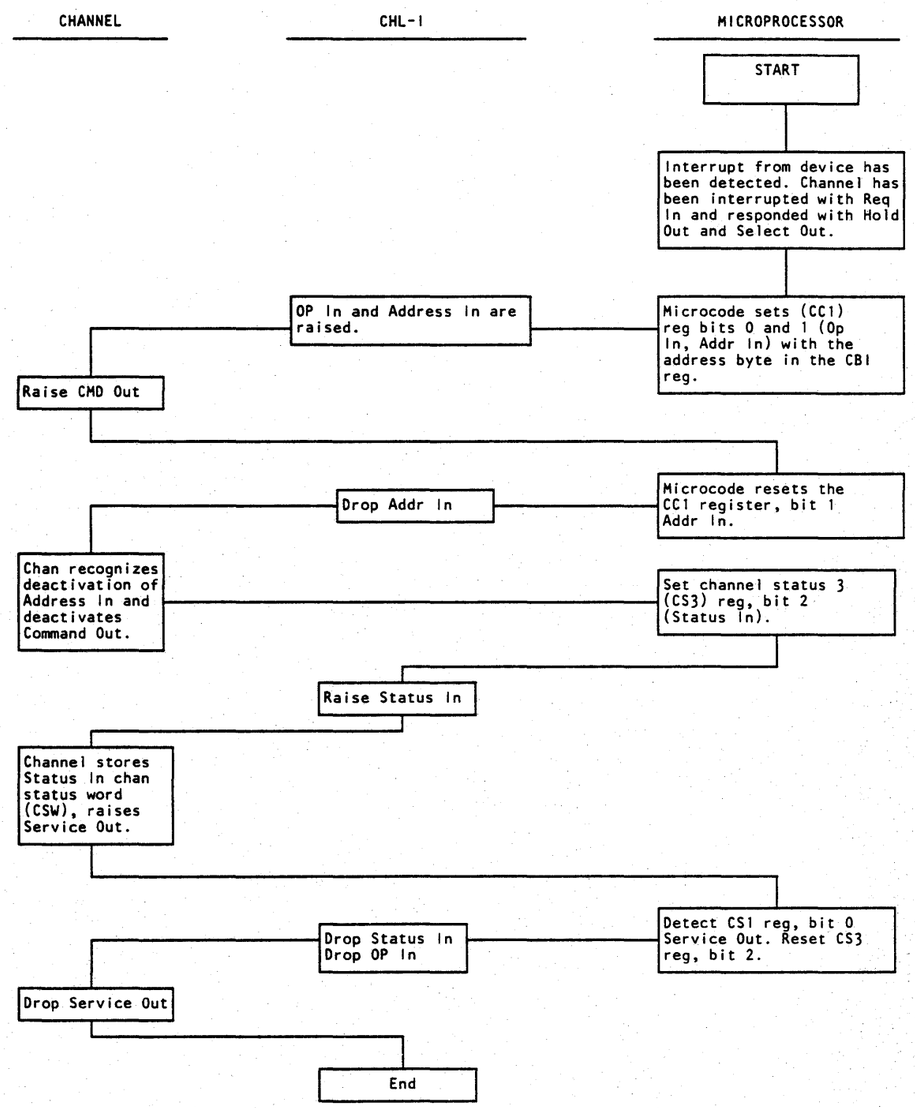


Initial Selection Sequence

Storage Director Initiated Sequence

When the storage director detects a device with status (such as Device End after a seek is completed), it must reconnect with the channel that issued the command and present the status:

1. Operational Out from the channel is active.
2. The storage director deactivates Request In and activates Operational In and Address In.
3. The storage director/device address byte is sent on Channel Bus In.
4. The channel uses the address to determine where the storage director and device are in a command chain.
5. The channel responds with Command Out without a command byte on Channel Bus Out.
6. The storage director deactivates Address In.
7. The channel responds by deactivating Command Out.
8. The storage director activates Status In to the channel with the status byte on Channel Bus In.
9. The channel responds by deactivating Select Out and Hold Out and activating Service Out to indicate acceptance of the status byte.
10. The storage director deactivates Status In and Operational In and waits for the next request from a channel or interrupt from a device.



Resets

A machine reset is issued to all units attached to the subsystem during power on, an IML, a system reset (from the host), or a reset command from the MD. The units may or may not be selected at the time of the reset.

The power-on sequence resets control circuitry and initiates initial microcode load (IML). Normal operation generates sense information on the status of the storage directors and other storage control circuitry, while IML diagnostics are available to generate further information on special error conditions. The sense information is assembled into sense formats that identify errors and unusual conditions. Sense formats also indicate error recovery procedures to be initiated by the system.

The interrupt mechanism determines the priority of concurrent requests for service from the storage director. Maintenance connection requests are given highest priority.

The 3880 Storage Control generates two general reset operations, special reset, and machine reset.

Special Reset

Special reset is initiated when any one of the following lines becomes active:

- Power On Reset
- Initial Microcode Load Reset
- Reset Command

Machine Reset

Machine reset is also initiated with special reset or when the Selective Reset or System Reset lines become active. Therefore, machine reset occurs if any of the following lines becomes active:

- Power On Reset
- Initial Microcode Load Reset
- Reset Command
- Selective Reset
- System Reset

Power On Reset

The Power On Reset line becomes active automatically during the power on sequence and resets the control circuitry including reset of the Select Out Trapped line.

Initial Microcode Load Reset

The Initial Microcode Load Reset line becomes active with a CE entry into the maintenance device and resets the control circuitry including reset of the Select Out Trapped line in the same manner as the power on reset.

Reset Command

The Reset Command line becomes active with a CE entry into the maintenance device and resets the same circuits as those reset by power on reset and initial microcode load reset.

Selective Reset

A selective reset is issued by a system to a single unit that is selected by the system and channel. The selective reset is normally used to reestablish communication with a unit that has an error and is not responding to normal communications.

In the multi-system environment of the storage director (channel interfaces attached to more than one system), a system or selective reset must not affect the operations of the other system.

A selective reset causes the selected drive to be reset, the storage director to reset any interrupt or error condition indications, and the drive to be deselected.

The Selective Reset line becomes active only as a result of a:

- Time-out by the channel
- Malfunction detected at the channel
- Request for disconnect-in from the storage director
- Channel performing selective reset by activating Suppress Out and deactivating Operational Out.

Selective reset resets all reserve and status conditions stored in the storage control for the selected device. An operation in process continues to a normal stopping point with no further data transfer.

System Reset

The System Reset line becomes active under one of the following conditions:

- The System Reset pushbutton at the host is pressed.
- The host system power is turned on.
- The channel is offline to the channel interface.
- Initial microcode loading is performed.
- The channel performs system reset by deactivating Operational Out while Suppress Out is not active.

All storage directors attached to the issuing channel are affected by a system reset.

A system reset:

- Resets all reserve and status conditions stored in the storage control for the resetting channel
- Terminates all block multiplex command chains in progress on the resetting channel
- Resets all device interrupts associated with the resetting channel

Because the storage director and drives may not be selected by the issuing system, a system reset must wait until the interface for this channel can be selected. When the interface for this channel is selected, the interrupt table for the channel is reset, as well as each device connected to the channel. One at a time, all devices available to this channel are selected and checked for pack change status. The availability table is then updated to release these devices to the other channel.

Hardware Sourced Resets

The following resets are sourced from storage director hardware.

Storage Power On Reset

This reset will reset the subsystem storage. It is activated each time the subsystem storage is powered up.

Controlled Machine Reset

This reset is a diagnostic controlled reset. Executing this reset from storage director 1 will reset registers in storage director 1 only; executing this reset from storage director 2 will reset registers in storage director 2 only.

Common Check Reset

This reset is a microcode reset used to reset common check registers and general registers.

Upper/Lower Check Reset

This reset is a microcode reset used to reset upper or lower check registers.

ASDM Reset

This reset is a microcode reset used to reset two write registers associated with the ASDM.

Communication Check Reset

This reset is a microcode reset used to reset all checks associated only with communication.

Initial Microcode Load

An Initial microcode load (IML) transfers the functional code from the IML diskette to control storage. The IML procedure is divided into eight phases.

Phase 1

Phase 1 of the IML performs the following:

- Verifies the microinstructions and the hardware used to load the IML common loader from the diskette drive to control storage (ROS hardcore tests)
- Selects a storage director
- Loads the IML common loader

ROS Hardcore Tests

When an IML command is initiated or power is turned on, the instruction address register (IAR) sets to zero, the ROS select signal activates, and the clock on the clock card starts. This causes instructions to be executed from read-only storage (ROS). These instructions verify the microinstruction and the hardware needed to load track 0 from the diskette to control storage. The hardware includes all the internal registers, all control storage, and the IML and MCR and MSR registers on the maintenance (MNT) card. Track 0 contains the IML common loader which loads the remaining tracks from the diskette to control storage.

If an error occurs during this verification, the storage director hangs. The error condition is placed in the external bus out (EBO) which can be read using the maintenance device (MD). The EBO register is used as an error condition readout register or as a progress register during IML.

Select a Storage Director

After power is turned on, the ROS code in each storage director requests the diskette drive. A tiebreaker circuit allows one of the storage directors to select the diskette drive.

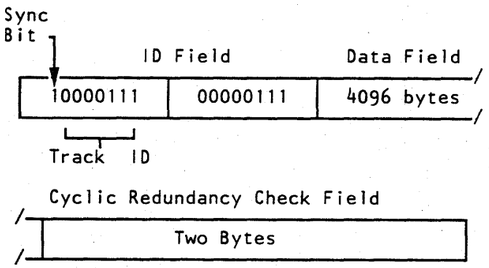
The selected storage director gates the Diskette Drive Data and Diskette Drive Index from the diskette drive to the IML register.

Load the IML Common Loader

Track 0 contains the IML common loader. The ROS code causes the diskette access motor to seek to track 0 by activating and deactivating the EBO register, and by setting a bit in the IML register. The ROS code assumes the head is on track 8, and then steps one track at a time to track 0. The ROS code then assumes that it is at track 0. The diskette is read as follows:

Diskette Drive Index is detected and gated to the microprocessor through IML register. Then, Diskette Drive Data is detected and gated to the microprocessor.

Diskette Drive Data is the serial data read from a track which is formatted as follows:



Note: The serial data read from a track is deserialized by the common overlay loader and controller in the common code.

The sync bit and the track ID are read from the first byte. The sync bit is reset by the ROS code and only the track ID is stored. The second byte, which contains only the track ID, is then read and stored. The rest of the track containing the data and the cyclic redundancy check (CRC) fields is then read.

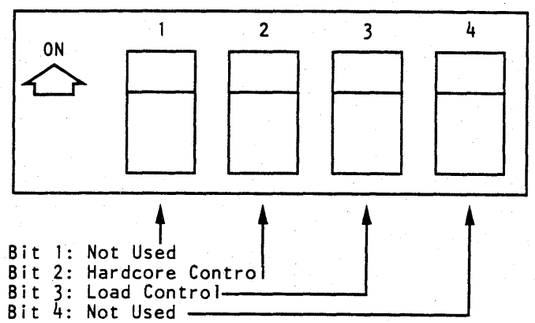
After the track is read and stored, the ROS code compares the first and the second bytes. A successful compare indicates that the diskette access head is on track 0. In case the compare is not successful, the diskette drive steps 8 more times toward track 0. This continues 11 times or until a successful compare occurs. When the compare is successful, the CRC is performed. The CRC detects whether or not the data was read correctly. If the CRC is not successful, the diskette drive steps 8 more times toward track 0. If track 0 cannot be reached or read successfully within 11 tries, the IML hangs, the EBO register is set from ALU Bus Out with the error condition, and the IML request resets.

Besides the IML common loader, the data field of track 0 contains maintenance operations code and pointer sets. The pointer sets are addresses that point to the locations of data on the diskette for each functional microcode load.

Diskette Load Control Switches

Two diskette load control switches on the maintenance (MNT) card indicate to the common loader code which pointer set (functional microcode load) to load from the IML diskette. These switches are set during installation.

The switches on each of the MNT cards appear as follows:



The label on the diskette shipped with the 3880 shows how the switches must be set for each storage director.

Bit 3, load control, determines which of the two functional microcode loads on the diskette are to be loaded.

Bit 2, hardcore control, determines whether the IML hardcores are to be run or not. When this switch is in the position called for on the diskette label, the IML hardcores are run.

Note: At the end of maintenance, the switches must always be set according to the label on the diskette.

Phase 2

The IML hardcore routines are loaded during this phase. The overlay loader contained in the common loader loads the hardcore monitor which controls the loading and running of the IML hardcore routines. The IML hardcore routines test the control and the data buffer functional areas in a storage director.

Phase 3

All functional code tracks except track 1 are loaded during this phase. Track 3 through the last track are loaded one at a time into a staging area. A CRC is performed on the data part of the track. If the CRC is successful, the data is then loaded into its positions in control storage. If the CRC is not successful, the track is loaded again and a CRC is performed again. If the CRC is not successful after the tenth attempt, the error condition is set from ALU Bus Out into the EBO register. Once the data is loaded into control storage, it is checked again. If the data check is not successful, CS Data Check is generated.

The last track to be loaded is track 2. It is loaded into the staging area and remains there.

Phase 4

Phase 4 prepares control storage for loading of track 1.

Phase 5

Track 1 is loaded into control storage during this phase. The data part of the track is checked. If the CRC is not successful after the tenth attempt, the error condition is set from ALU Bus Out into the EBO register. Once the data is loaded into control storage, it is checked again. If the data check is not successful, CS Data Check is generated again.

Phase 6

Phase 6 returns some data that was once moved during phase 4 to its original positions in control storage.

Phase 7

During Phase 7, the overlay loader in the functional code loads any changes located on the overlay track into control storage.

The access, data, and index lines in the other storage director are gated, and the other storage director performs an IML exactly like the first.

Phase 8

A two-storage director path test is performed during this phase.

Storage Director Communication

The storage directors send messages to each other that convey changes in subsystem storage operational states.

The storage directors communicate with each other by two methods. The primary method uses the 3380 Dual Path Switch (DPS); the secondary method uses a register to store encoded messages. The secondary method is a alternate method used when the primary fails.

Communication Registers

When the storage directors cannot use the communication buffer, they communicate through two registers on the Storage Control 1 (CMC1) card.

The sending storage director encodes its messages into eight bits and sends them to a register. The receiving storage director reads the eight bits and decodes them for use.

Change State	Request a change of operational state (such as initialization required) of the other storage director
Make Subsystem Storage Available	Signal the other storage director to make the subsystem storage available
Make Subsystem Storage Unavailable	Signal the other storage director to make the subsystem storage unavailable
Synchronize	Synchronize the storage directors
Acknowledge	Signal receipt and successful execution of a message sent by the other storage director
Activate Primary Communications	Signal other storage director to activate primary communications

Messages

The storage directors can send the following messages:

Error Alert

When a storage director fails (Check 1):

1. The failing storage director notifies the non-failing storage director of the failure.

2. The non-failing storage director collects check information from the failing storage director and assembles it into sense bytes.

3. The non-failing storage director then:

   - Notifies the processor of the failure by presenting unit check to the next start I/O

   - Allows the failing storage director to present an I/O Error Alert sequence to the channel

4. After being notified of the failure:

   a. The system issues a Sense command and receives and logs the sense bytes.

   b. The system issues a selective reset to the failing storage director.

5. If the selective reset executes successfully, the storage director resumes normal operation.

6. If the selective reset fails, the issuing channel is disabled, and the system issues another selective reset across a different channel. The system continues issuing selective resets until the failing storage director is reset or until all the channels are disabled. When all the channels are disabled the storage director clock stops.

Maintenance Operations

The maintenance operations described in this section are those invoke from the maintenance device (MD) by the CE using the procedures in the Maintenance Device section. The hardware and hardware–microcode interactions involved in these operations are described in the following paragraphs.

Overview

The figure on this page is a simplified data flow between the MD and one of the storage directors in the 3880. The maintenance device adapter (MDA) consists of two cards:

- Maintenance device adapter control (MDAC) card
- Maintenance device adapter registers (MDAR) card

The portion of the data flow path between the MD and the MDA is serial by bit; all other portions of the path are parallel. Depending upon the particular maintenance operation, information may be transferred over all or over portions of the data flow path, as shown at he bottom of the figure. This can be understood from the following operations:

- MD to MDA SERDES
- MD to MDA
- MD to MNT
- MD to storage director microcode

MD to MDA SERDES

The MD can hold the MDA in reset state and can shift data into the MDA serializer–deserializer (SERDES). The MD can also shift the data out of the MDA SERDES without any action on the part of the MDA. This makes it possible for the MD to check the operation of the MDA SERDES by transferring a byte of data to the MDA SERDES, retrieving it, and comparing it to the byte sent.

MD to MDA

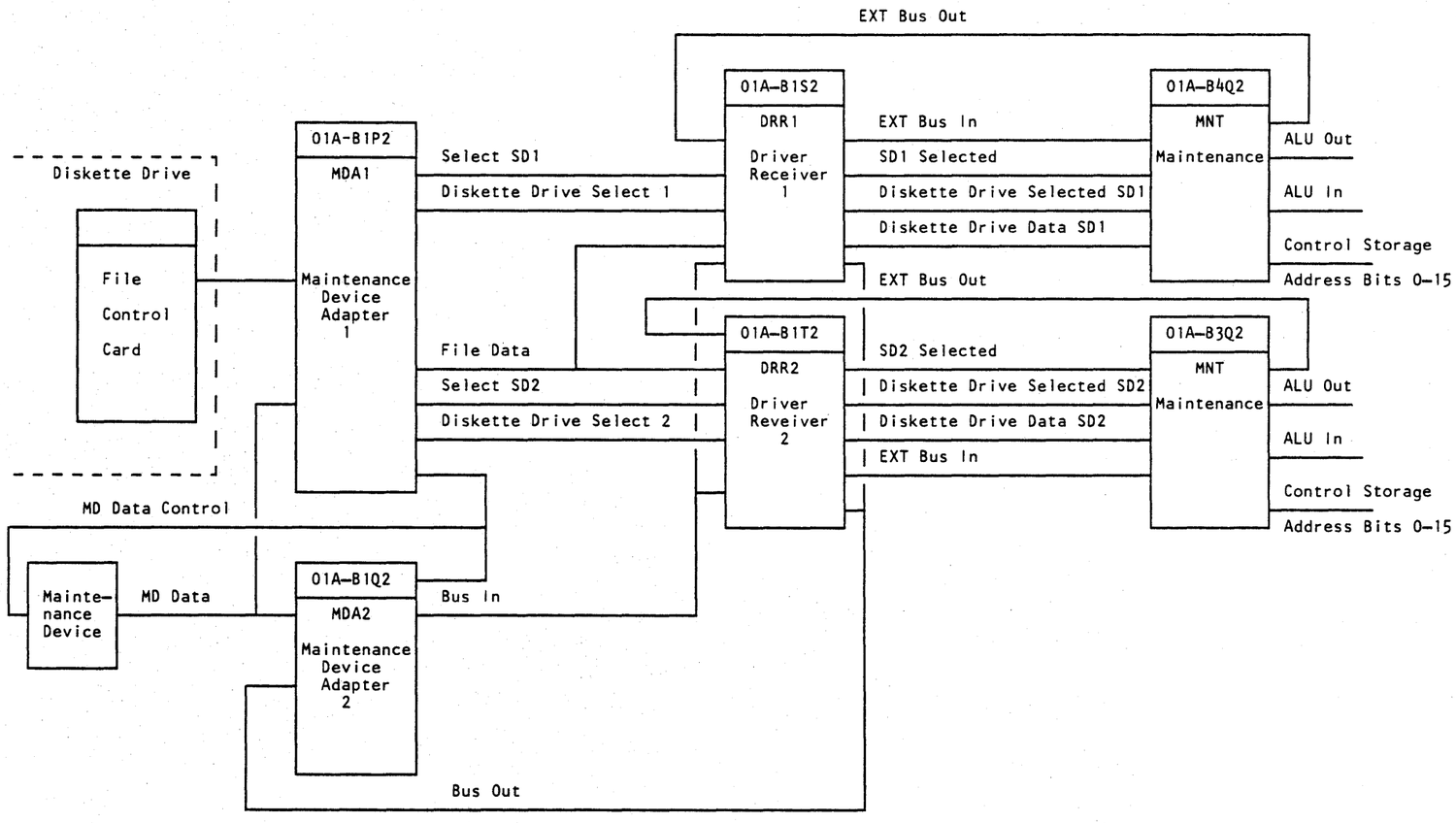
By interacting with the hardware in the MDA, the MD can transfer information to and from registers in the MDA. This transfer is accomplished using two kinds of commands: primary and secondary. Primary commands tell the MDA how it is to handle subsequent data, addresses, or secondary commands. Secondary commands either accomplish specific commands within the MDA or are passed on, over the external bus in (EBI) to the storage director board.

MD to MNT

Secondary commands, addresses, and data may be passed to the MNT card over the EBI to cause hardware in the MNT card to respond. For example, the external registers on the MNT card can be displayed by retrieving them in this way. Other operations, such as start and stop, are executed by hardware on the MNT card.

MD to Storage Director Microprogram

Some secondary commands and any associated addresses and data passed to the MNT card cannot be executed by the hardware alone. They result in level 0 interrupts to the storage director microcode. The microcode responds to them. For example, data in control storage is retrieved for display in this way.



Diskette Drive Components

Diskette Cover

The diskette cover 1 permits insertion and removal of the diskette.

Disk Collet Assembly

When the diskette cover is closed, the spring–loaded collet 2 centers and clamps the disk to the disk drive.

Head Load Actuator Assembly

The head load actuator assembly 3 consists of a magnet and an armature. During a read operation, the head load actuator is energized and allows the head pressure pad arm to push the disk against the read head. At the same time, the head load actuator armature compresses the diskette to load and clean the disk. While not reading or writing, the head load actuator is deenergized, and the pressure pad assembly is held away from the disk to reduce wear on the disk surface and the read head.

Preload Spring

The preload spring 4 loads the leadscrew to ensure head alignment with the disk.

Limit Stops

The upper 5 and lower 7 limit stops restrict head motion on the leadscrew.

Leadscrew Nut and Spring

The leadscrew nut and spring 6 load the head carriage assembly to ensure head alignment with the disk.

Read Head

The read head 8 provides the read and erase functions.

Light Emitting Diode and Phototransistor

When the diskette cover is closed, the continuous light emitted by the light emitting diode (LED) 9 is directed towards the phototransistor 10. Once every revolution, the index hole in the disk allows light from the LED to reach the phototransistor. The phototransistor sends index pulses to the 3880 Storage Control.

File Control Card

The file control card 11 provides the circuits for the stepper motor, head load actuator, and the erase coils in the head. It also provides the amplifiers for the phototransistor and the read head.

The file control card is mounted with components and test points facing outward for servicing.

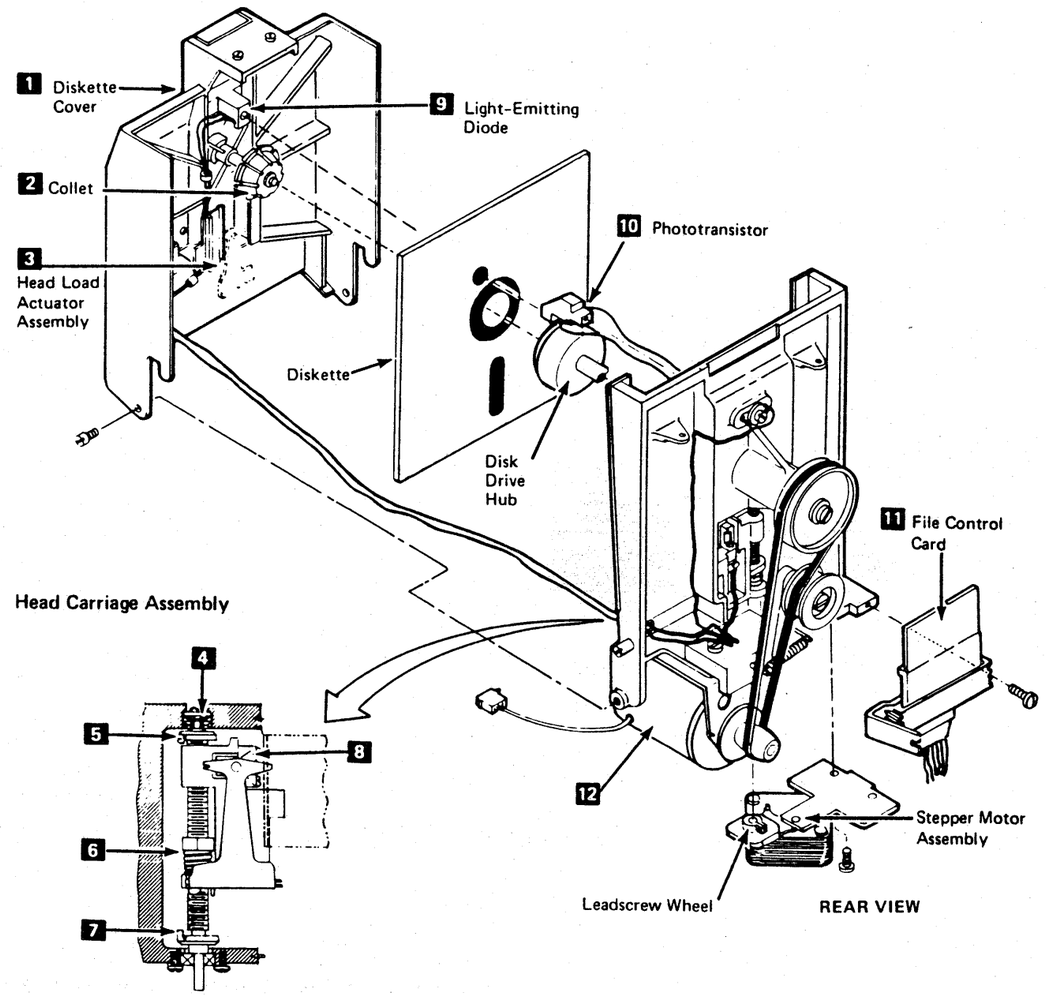
Motor and Drive

The motor 12 rotates the disk at a speed of 360 rpm.

Stepper Motor Assembly

The stepper motor wheel is permanently mounted on the end of the stepper motor shaft. The stepper motor shaft turns in increments of 90 degrees in either direction under the control of the access pulses from the 3880. The stepper motor wheel engages the leadscrew wheel. When the stepper motor rotates 90 degrees, it causes the leadscrew to rotate 90 degrees. The head carriage assembly then moves up or down one track on the disk.

Diskette Drive



3880 MSM		PN 6315723 51 of 54	881216 15 Aug 84	A15621 01 Apr 85			
	Seq JG0001						

Operating Sequence

1. The 3880 activates the AC Power (motor control) line and the drive motor starts turning.

2. Insert the diskette and close the cover. (Diskettes can be inserted or removed with power on.)

   Closing the cover engages the diskette collet assembly **8** in the drive hub **7**, which clamps the diskette in place. With power on, the diskette starts turning.

3. The index pulses **13** are read every 166.6 ms (nominal) after a 10-second delay from power-on time.

4. The 3880 activates the Head Engage line **12**. This causes the head pressure pad **9** to push the read head against the diskette. After an 80 ms settling delay **1**, data is valid for the 3880. The head location is determined by reading the track **2** or by returning the read head to track 0.

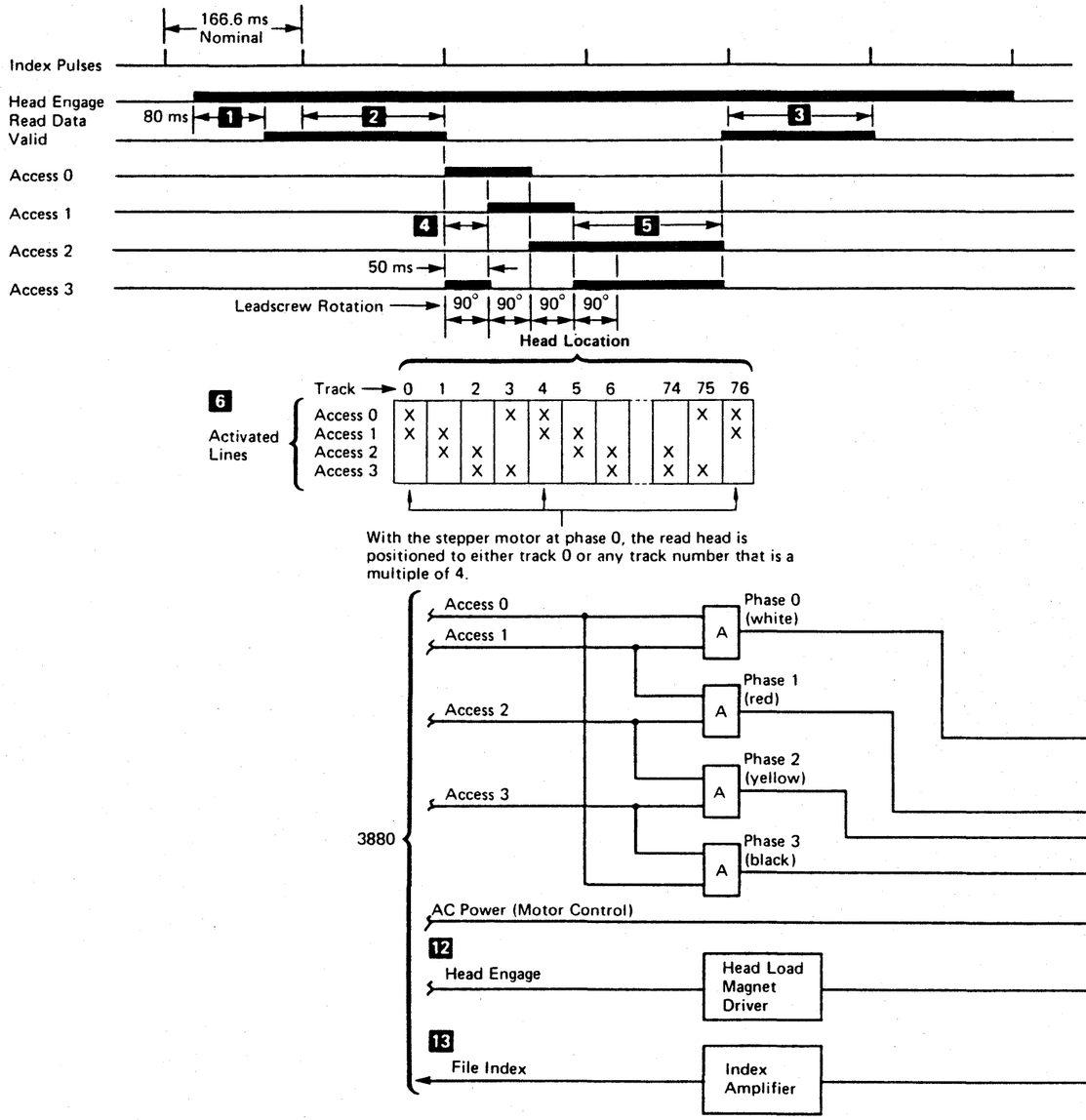
5. For each access command, the stepper motor **11** rotates the leadscrew **10** 90 degrees clockwise or counterclockwise. (A clockwise rotation of the leadscrew, looking down on the unit, moves the carriage up.)

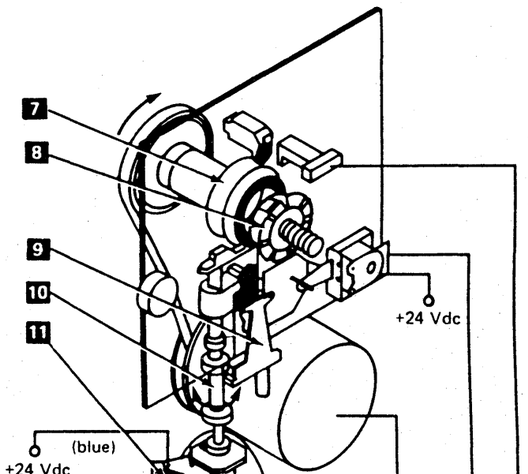
   Two adjacent signal lines must be activated at the same time when accessing **6**. These signals must overlay by no less than 50 ms **4**. Prior to a read operation, the two lines for the selected track must be activated for at least 150ms **5** (50 ms for travel and 100 ms to stabilize).

6. Data is read **3**.

7. The 3880 deactivates the Head Engage line upon completion of the last read or access operation. The pressure pad is then lifted, to reduce diskette and read head wear.

Typical Timing Sequence





Raw Read Data

- Sine wave signal:

  125 kHz (all 0s)
  250 kHz (all 1s)

- Higher voltage at the outer track because of higher diskette speed and lower bit density.

- An all 0s pattern gives higher voltage amplitude than an all 1s pattern.

CAUTION
Do not measure the resistance of the read coils 1 as damage to the head may result.

Read Amplifier

Preamp 2 and differentiator input:

1.0 to 20 mV (all 0s)
0.5 to 15 mV (all 1s)

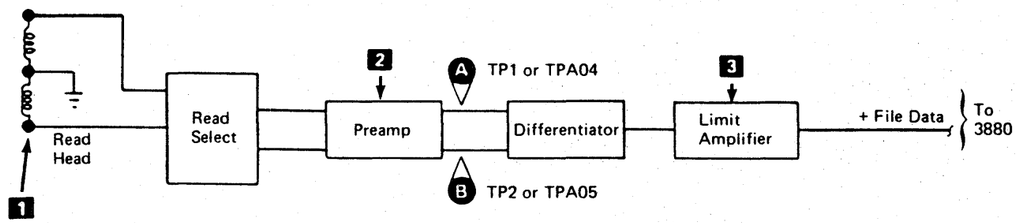
Limit Amplifier

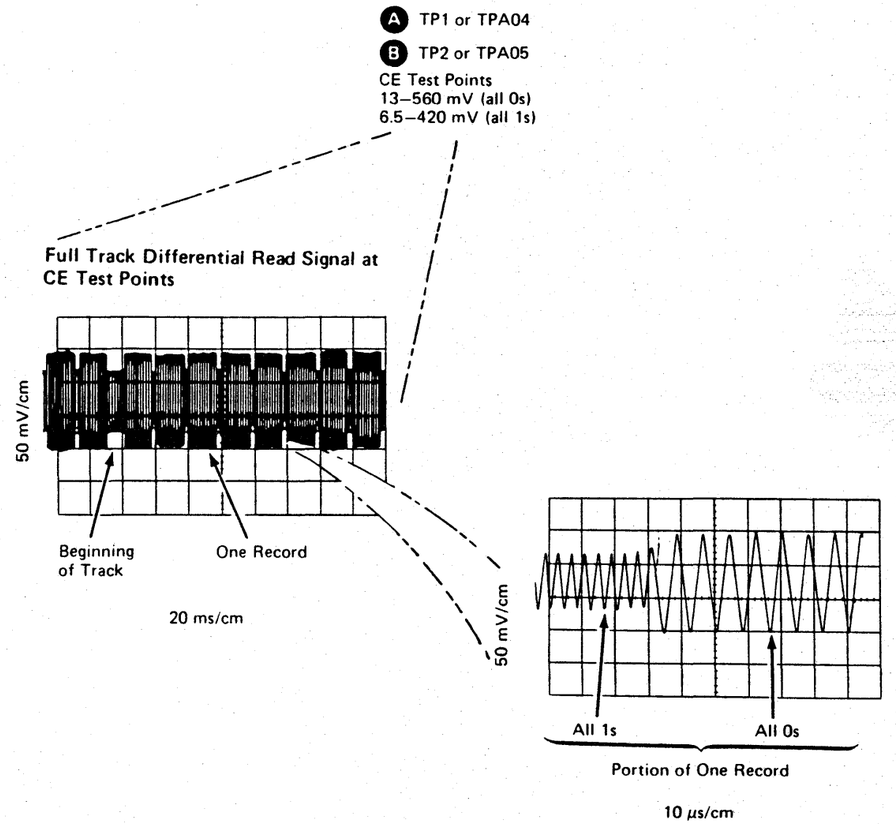
- The amplifier 3 amplifies the signal so that one of the amplifier transistors is cut off. Outputs of the limiter are two out-of-phase square waves.

- A differential rectifier RC network differentiates square waves. The resulting positive- and negative-going pulses (180 degrees out of phase) are the input to an OR circuit. The output is a series of positive pulses. Positive leading edges of the output pulses correspond to peaks in the read signal delayed by a constant amount.

- The file data is a string of 150 ns pulses (+File Data line), that are fed to the initial microcode load (IML) register in the 3880.

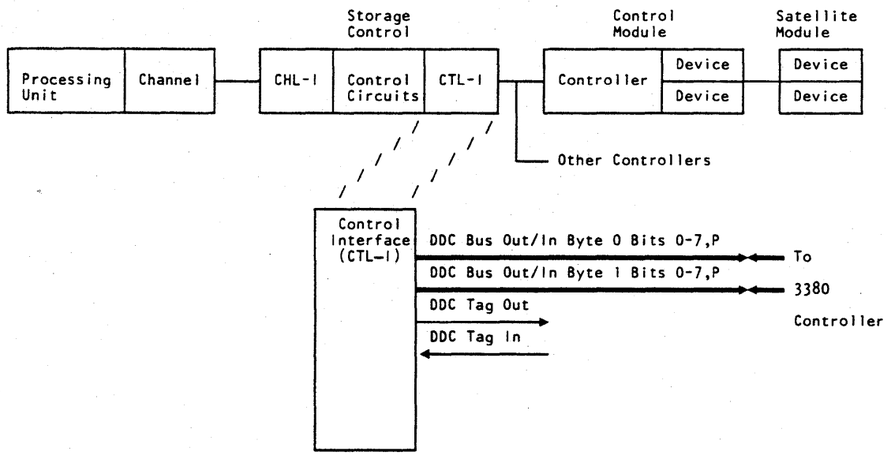
Read/Write Block Diagram





Control Interface

The control interface (CTL–I) is the communication link between the 3880 storage director and the 3380 Controller.



The CTL–I consists of the logic, board wiring, cables, and connectors required to perform the following:

- Transform bits in general purpose registers into signals on the interface cable to the device controller
- Receive signals placed on the interface cable by the device controller and gate them to the general purpose registers or convert them to branch conditions for use by the microcode
- Control operations that require communications between the storage director and the device controller
- Detect malfunctions during CTL–I operations and notify the microcode by setting the check 2 error

DDC Lines

DDC Bus Out/In Byte 0

The DDC Bus Out/In Byte 0 lines carry:

- Read or write data between the storage director and device controller
- Control information from the storage director to the device controller

DDC Bus Out/In Byte 1

The DDC Bus Out/In Byte 1 lines carry:

- Read or write data between the storage director and device controller
- Status information from the device controller to the storage director

DDC Tag Out

The DDC Tag Out Bit 0, 1, and 2 lines carry signals from the storage director to the device controller. The storage director uses these lines to:

- Indicate control data is on the bus out bite 0
- Start operational sequences
- Respond to operational sequences
- Respond to a sync in tag in during a read or write operation

DDC Tag In

The DDC Tag In Bit 0 and 1 lines carry signals from the device controller to the storage director. The device controller uses these lines to:

- Indicate response data is on bus out byte 1
- Respond to operational sequences
- Start operational sequences
- Respond to a sync out tag in during a read or write operation

Note: For a detailed description of the control interface lines see the 3380 MSM OPER section.

Problem Determination Aids

Contents of This Section

Problem Determination Aids

Introduction

The problem determination aids section is designed to assist the customer engineer in finding the causes of difficult hardware and software problems that occur in the subsystem. The following are included in this section.

- Trace function
- Dynamic trace tables
- Sync and save tables
- State save tables
- Maintenance connection trace tables
- Unusual operating conditions
- Generalized trace facility
- Channel monitor

Contents PDA 10

Introduction to The Trace Function

Trace Function

The trace function collects information about channel operations and the execution sequence of the microcode. The program reflects the state of the machine by producing a snapshot of the functional microcode.

The information collected by the trace function is held in control storage until transferred to the maintenance device diskette or printed by an online test (OLT) program. This information helps in the diagnosis of difficult hardware and software errors. It also helps the CE find channel interface failures.

Before a trace can be started, prerequisite data must be supplied to the program through the maintenance device (MD). The prerequisites are: trace options, trace levels, and trace save conditions.

Trace Options

The trace options are:

- Trace all devices
- Trace single device.

The trace all devices option permits the tracing of all the devices attached to the 3880. A device address is not needed for this option.

The trace single device option limits the trace to a single device and requires a 1-byte channel I/O device address.

Trace Levels

The trace level instructs the trace function where to collect the information. There are three trace levels:

- Channel level only
- Block level only
- Both channel and block level.

By selecting channel level only, the program saves command codes, device addresses, and status bytes.

By selecting block level only, the program saves the block ID number from each trace entry of a functional microcode block as it is executed by functional microcode.

By selecting the both channel and block level, all command codes, device addresses, status bytes, and block IDs are saved.

Trace Save Conditions

Trace save conditions allow the trace function to stop and save the status of the machine. There are four conditions:

Sync/save IDs

Addresses

Symptom codes

Save Condition Not Specified

If no save condition is specified, a trace stop must be forced by either of the following option 2 commands:

4 = Stop trace with no save

5 = Stop trace with save

The maximum number of save conditions are:

- Up to three sync/save IDs and no symptom codes
- Up to three addresses
- Up to three symptom codes and up to two sync/save IDs

Sync/Save IDs

The sync/save ID is a defined 3-digit hexadecimal number. When the CE enters this number into the MD, the program runs until it detects the desired block and module number, corresponding with the sync/save ID. The program stops at that point and enters the status information into control storage from the internal registers, the external registers, and the maintenance connection.

Addresses

Actual addresses can be used to stop a trace. Enter the address 'AAA' when the MD requests the sync/save ID hexadecimal digits. The MD then requests entry of the four hexadecimal digits of the address.

Symptom Codes

Symptom codes can be used to stop a trace. Enter "yes" when the MD asks if symptom codes are to be used. The MD then requests entry of the symptom code(s).

The functional microcode generates symptom codes when an error condition is found during a functional microcode operation. To use symptom codes as a trace save condition, the code itself must be masked as described on MD 70.

Trace/Dump Printout

The trace/dump printout is divided into these tables:

- Dynamic trace table
- State save table
- Maintenance connection trace table

Note: These tables are described on PDA 105 through 125.

Running the Trace Function

The trace function is fully automated by using the MD. The program begins when support option 2 is selected on the MD keyboard. See MD 70 for the procedure to select and run the trace function.

Introduction to The Trace Function PDA 100

Dynamic Trace Table

The dynamic trace table is a recorded history of functional microcode entries. The trace table records the latest 512 trace entries in the order of their execution.

Each dynamic trace table varies depending upon the trace levels chosen on the maintenance device (MD) at the start of the trace. The sample on this page is a printout where both channel and block levels where chosen.

Every entry in the dynamic trace table gives either a block trace ID or channel information. A block trace ID **2** has the format of BwwMxxx, where ww stands for the block number and xxx relates to a specific microcode module within that block.

Channel information collected by a trace includes:

- Storage director or channel initiated selection
- Selected channel interface ID
- Selected device address
- Device disconnect or stacked ending status
- Completed command (not shown).

To interpret the printout, determine the correct block description pages to use in this section. Because the newest entry is printed last, begin with the last entry in the table and work from newest entry to oldest. (The last entry in the table is always B04M100, It is caused by the MD and should be ignored.)

The sample printout (figure 1) shows the microcode was in block 7 **6** for both entries 510 and 511, and in block 16 **5** for entry 509.

> **Note:** Figure 2 shows a sample sync and save table containing a brief description of each of the block trace IDs (B07M001 and B07M003 for example). Refer to those tables when analyzing a dynamic trace. The tables begin on page PDA 405. The heading for each table indicates the name of the corresponding block. For example, block 16 (page PDA 4xx) is the ending-status block.

In entry 508 the channel status shows X'20' and the message, 'stacked', that came from block 10, specific connection pending (see PDA 4xx). Entry 506 shows that a storage director initiated selection **4** took place on channel interface A with address X'70' **3**.

Summarizing entries 506 through 511 in Figure 1 and referencing the appropriate PDA 4xx pages indicates:

506 SD initiated a selection to address A70
507 B10M208 (PDA 4xx) Specific Connection Pending block - present CU end status
508 Present stacked status of X'20' (control unit end)
509 B16M101 (PDA 4xx) Ending Status block - exit to Wait block (block 07)
510 B07M001 (PDA 4xx) Wait block - normal wait loop entry
511 B07M003 (PDA 4xx) Wait block - preferred connection required, return to block 10 (Specific Connection Pending)

The V1 and V2 fields **1** are program variables which may be described by the comment information in the trace tables.

Sync and Save Table

An entry ID **7** uses the same alphabetic format as a block trace ID. However, the ID is used solely to identify entry into the block. The ID numbers shown in parentheses are not traced and cannot be used to stop a trace. The ID numbers shown in parentheses are not printed in the dynamic trace table.

The sync and save ID uses a defined 3-digit hexadecimal number. All three digits of the sync and save ID are always shown (for example, '00C'* **9**). Only save points are followed with an asterisk.

The sync and save ID number can be entered into the MD to terminate a trace. When the microcode address associated with the sync and save ID is reached, the trace is stopped and the contents of the microcode registers are saved and can be printed by using OLT T3880D. Trace points which are not sync and save points **11** cannot be used to terminate a trace, but if the microcode goes through the corresponding trace ID, the trace ID will be printed in the dynamic trace table.

The last column of Figure 2 shows the function of the microcode module within the block trace ID. Functions **8** **10** **12** are grouped by their relational position and purpose in a microcode block; such as entry, internal, error exit, or exit.

Sync and save tables begin on page PDA 405.

```
TD03  TRACE/DUMP      3880 S/N 10296          19MAR80

          DYNAMIC TRACE TABLE ENTRIES
                                                  1
ENTRY  CHAN   ADDR     CMND     STATUS     ID        V1   V2   ENTRY
 475                                  2   B07M003                475
 476    A       76                        CHN INIT               476
 477                                      B10M202                477
 478                                      B07M003                478
 479    A       70                        SD INIT                479
 480                                      B10M208                480
 481                                20    STACKED                481
 482                                      B16M101                482
 483                                      B07M001                483
 484                                      B07M003                484
 485    A       76                        CHN INIT               485
 486                                      B10M202                486
 487                                      B07M003                487
/                                                                /
/                                                                /
 506    A   3   70                    4   SD INIT                506
 507                                      B10M208                507
 508                                20    STACKED                508
 509                                  5   B16M101                509
 510                                  6   B07M001                510
 511                                      B07M003                511
 512                                      B04M100                512
```

Figure 1. Dynamic Trace Table Sample

TRACE OR (ID ONLY)	SYNC AND SAVE*	ENTRY 8
7 (B07M001)	------	NORMAL WAIT LOOP ENTRY
(B07M002)	------	ENTRY FROM RESET DEVICE INTERRUPT
(B07M006)	------	ENTRY FROM PREFERRED CONNECTION OR RESET DEVICE INTERRUPT
(B07M104)	------	RETURN FROM INLINES
	9	INTERNAL 10
------	00C*	RESET PROCESS/TAG GATE AND ALLOW DISABLE
	11	EXIT 12
B07M003	------	PREFERRED CONNECTION REQUIRED TO BLOCK B10M101
B07M104	------	HANDLE INTERNAL INTERRUPT TO BLOCK B08M000
B07M202	------	EXIT TO STORAGE DIRECTOR INITIATED SELECTION
B07M203	------	EXIT TO CHANNEL INITIATED SELECTION

Figure 2. Sample Sync and Save Table (Block 07)

State-Save Table

The state-save table entries are bytes of information representing the state of a storage director at the instant a save operation is performed. The state-save tables in the PDA are used to interpret the state-save information from the trace dump printout. When a trace save operation is started, the trace function stops and stores status information from the external, internal, and indirect registers, the maintenance connection, and the working storage portion of control storage.

Use the state-save pages to locate specific information about the internal registers and working storage.

A list of state-save table entries supports a specific type of device. A sample of the state-save table as it appears in a printout is shown in Figure 1.

Activating Conditions

The printout lists the active stop-save events as they were entered to start the trace operation (if not forced by the MD). The event causing the stop save is identified **1**. The stop may be forced by the maintenance device.

External Registers

The external registers contain information on the state of a storage director and its interfaces and connections. Each selectable microcode readable register is saved and appears in the trace-dump printout. Descriptions of the external register bits are given in the REF section of the MSM.

Internal Registers

There are 16 groups (0 - F) of 8 internal registers. The contents of all internal registers are stored in control storage and reproduced on the printout by group and register. However, only the registers in groups A through D contain useful information because these registers generally contain information standardized among all blocks. Registers in groups 0 through 9 and PSW0 through PSW3 only reflect the status of the storage director at the time the save operation was started.

Note: Register GRPE contains PSW0 and PSW1. Register GRPF contains PSW2 and PSW3.

State-Save Trace Table Description

Figure 1 is a sample of a trace printout of the external and internal registers.

Figure 2 is a sample of the internal registers table found in the state-save pages beginning on page PDA 500.

In this example, register 2 of group GRPA of the internal registers in the printout (see figure 1) shows X'04'. This indicates that bit 5 of register 2 is on. A description of bit 5 is shown in Figure 2.

Indirect Registers

Indirect registers are used to control and determine the status of the upper and lower ports and the storage director to storage director communication.

```
STOP SAVE ACTIVATED BY:  FORCED BY MD 1

FOLLOWING SAVE POINTS ACTIVE:

                EXTERNAL REGISTERS

BAH = 00   BAL = 07   BFR = 00   CBH = 42
CBI = 0C   CBL = 00   CBO = 0A   CC1 = 02
CC2 = 00   CHK = 00   CRC = EA   CRO = 10
CR1 = 00   CR2 = 00   CR3 = 00   CR6 = 00
CS1 = 0C   CS2 = 01   CS3 = 04   CXC = 00
DBH = 00   DBI = 00   DBL = 70   DBO = 40
DCH = 84   DCL = 80   DRC = EA   DTG = 46
DTI = 48   DTO = 82   DXC = 00   EBI = AD
ILR = DF   IML = 80   MCS = 24   MSR = 00
PCR = 00   SDI = FD   TFR = 01   XCS = 00
XES = 00   RDB = FF

                INDIRECT REGISTERS

LCTL  =00  UCTL  =00 LSAR0  =01  LSAR1 =80
LSAR2 =00  LOPCTL=00 LCTRH  =06  LCTRL =72
USAR0 =CB  USAR1 =00 USAR2  =00  UOPCTL=00
UCTRH =00  UCTRL =00 CCOMCTL=00  CSTAT1=00
CSTAT2=40  CSTAT3=00 CSTAT4 =00  CACTL =80
CCTL  =00  CARD1 =40 CARD2  =80  CAWR1 =00
CAWR2 =00  CAAJCK=00 GTS    =41  GMIC  =11
GSSCIN=4F  GIDSW =0F

                INTERNAL REGISTERS

     0   1   2   3   4   5   6   7

P    A8  FF  03  1A  00  00  00  B3
S    01  18  1D  A8  01  00  00  00
GRP0 71  DD  73  09  4F  41  84  70
GRP1 E1  10  21  31  41  51  61  71
GRP2 84  00  42  43  4C  FC  00  00
GRP3 80  00  1A  97  14  B3  00  00
GRP4 52  1F  20  20  14  15  5F  23
GRP5 A8  FF  03  1A  00  00  00  B3
GRP6 2F  00  1D  A8  00  00  00  00
GRP7 41  08  1D  A8  00  00  00  00
GRP8 6F  10  1D  A8  00  00  00  00
GRP9 01  18  1D  A8  01  00  00  00
GRPA 00  01  04  00  00  00  00  00
GRPB 00  00  03  85  00  42  20  E4
GRPC 00  04  06  00  80  A6  06  EC
GRPD 80  05  0B  FC  0B  FC  28  90
PSW0 IAR = 4D86   CCR = 2E  IRG = 00
PSW1 IAR = 4600   CCR = 05  IRG = 9D
PSW2 IAR = 17E8   CCR = 10  IRG = 54
PSW3 IAR = 1D9F   CCR = 00  IRG = 59
```

Contents of Register 2, Group A (GRPA)

Figure 1. State Save Table Sample

GROUP A - REGISTER 2		
BIT	NAME	DESCRIPTION
0	Head Switch Error	Set if G1 head switch is not allowed. Reset during processing count or HA.
1	Chained from Read HA	Indicates previous CCW in chain was a Read HA. Reset at end of every CCW except Read HA.
2	PCI data check	Set by retry when recovery from uncorrectable data check must be unit checked as specified by the file mask. Reset at end of CCW.
3	Buffer Operation	Set when data transfer uses the ADT buffer.
4	Channel Turnaround	Indicates channel turnaround occurred in previous gap. Set when chained from an oriented CCW. Reset after processing and gap or by all Control, Sense, Reserve, Release, and Diagnostic commands.
5	Skip Uncorrect-able Data Check	Permits skipping one record with an uncorrectable data check if unoriented. Set at beginning of Control, Sense, Reserve, Release, or Diagnostic commands. Reset after reading or clocking any count or HA. Also reset by data overrun or data check retry.
6	Key Length Not Zero	Set when processing a count field if key length is not zero. Reset at end of command.
7	Data Length Not Zero	Set when processing a count field if data length is not zero. Reset at end of command.

Figure 2. State Save Table Register Description

Microcode Variables

Each field in the next section of the state-save table is headed by an entry name. A description of each of these working storage fields is contained in the state-save table entries section of this section.

Each field of code in the remainder of the state save table is headed by an entry name. The headers for the microcode variables remain the same for all 3880s.

Working Storage

The remainder of state save information is divided into fields and stored in working storage. These individual fields are found on the trace printout under the heading of Microcode Variables (see Figure 1). These fields are grouped in this manual under Working Storage Definition (see Figure 2) and appear in the same order as the fields on the trace printout. See PDA 5xx for the working storage definitions. Each field is divided by a 3-digit hexadecimal number, representing the displacement value within the table. These numbers are the relative addresses of each byte pair. Working Storage Definition provides a short description of each byte pair.

MICROCODE VARIABLES

CVT - COMMUN. VECTOR TBL

Hex	0	1	2	3	4	5	6	7
000	6283	6220	4D86	7000	6280	4582	47FA	4207
008	4208	4209	420A	4300	47C9	4500	420E	4A00
010	3BA2	0800	3BA0	0800	3BA4	0800	3BA8	0800
018	3BAB	0700	3BA2	0700	3BA0	0700	7200	086F
020	3BA5	0700	3BA9	0700	0B5C	2DC0	9801	492A
028	31C4	095F	31C5	095F	022C	0EBF	022E	0908
030	0000	0000	0000	0000	0000	0000	0000	0000
038	0000	0000	0000	0000	0000	0000	0000	0000

INLINE PARAMETER AREA

Hex	0	1	2	3	4	5	6	7
000	0003	0000	0000	0000	0000	0000	0000	0000

INLINE MESSAGE AREA

Hex	0	1	2	3	4	5	6	7
000	8400	0200	0400	0800	1000	2000	4000	8000

INLINE CONTROL STG AREA

Hex	0	1	2	3	4	5	6	7
000	0800	2800	3D50	0000	0000	0000	0000	0000
008	0000	0000	0000	0000	0000	0000	2804	4100
010	040A	40A2	005A	CE3D	0044	8F00	0000	0101
018	F600	00FF	0000	0000	0000	0000	0000	0000
020	0000							

TRACE FUNCTION AREA

Hex	0	1	2	3	4	5	6	7
000	0203	0000	0000	0000	0000	8400	0FFF	0FFF
008	0FFF	4078	055A	422E	0000	FFFF	6304	0000
010	0301	0000	0000	0000	0000	0000	0000	0000

DISKETTE INFO STG AREA

Hex	0	1	2	3	4	5	6	7
000	222D	0101	0221	0101	0000	0004	5185	0000
008	0000	4505	5208	2E36	0000			

Figure 1. Sample of State Save Portion of the Trace Dump

WORKING STORAGE DEFINITION

COMMUNICATIONS VECTOR TABLE (CVT)

The CVT is used to provide a run time link between the diagnostic and functional microcode. They are translated and linked separately.

Hex	Description
000	Address of the check one sense area
001	Address of the normal sense area
002	Undefined
003	Address of the dump table
004	Address of the stored channel switch value
005 to 016	Undefined
017	Address of Contingent Allegiance control block
018 to 03F	Undefined

INLINE (DIAGNOSTIC) PARAMETER AREA

Hex	Description
000 to 007	Inline parameter area

INLINE (DIAGNOSTIC) MESSAGE AREA

Hex	Description
000 to 007	Inline message area

Figure 2. State Save Table Sample

How to Use the Maintenance Connection Tables PDA 120

Maintenance Connection Trace Table

Like the dynamic trace table, the maintenance connection trace table records the last 254 exchanges across the maintenance connection in locations X'002' to X'0FF'. However, unlike the dynamic trace table, the maintenance connection trace table is always active, even after a state save. The exception is when the transfer of actual trace data is dumped to the maintenance device (MD).

Once 254 bytes are entered into the table, old entries are chronologically replaced by new entries. The information in the table wraps around from entry X'0FF' to X'002'. Because of this wrapping effect, the maintenance connection trace table does not directly identify the newest or oldest entries into the table.

Instead, the oldest entry of the table is located by means of a pointer. This pointer is located in position 001 of the maintenance connection trace table. The low order byte in the pointer is the location of the oldest entry. The word preceding the oldest entry is the newest entry. In the example provided, the pointer 728A points to entry 08A as the oldest entry and is the next position in the table to be filled. The newest entry is at 089.

Data can be entered into the maintenance connection trace table through an MD connected directly to a 3880.

Entries made through the MD connected to an 3880 are identified in the printout by the sequence CCC1, CDXX. The code CCC1 indicates that the MD has one byte of data to transmit; the code CDXX identifies the data byte XX.

Entries generated from a drive by using the MD are identified by DCXX. The XX is the byte transmitted from the device. Messages transmitted to the device or the MD are entered in the same format as displayed on the CE panel.

Refer to page PDA 635 for a typical example of a communication sequence, and for a description of maintenance connection commands and responses.

TD01 TRACE/DUMP 3880 S/N 10662 05JUN80

MAINTENANCE CONNECTION

Pointer

Hex	0	1	2	3	4	5	6	7
000	727A	728A	CE9C	DC00	8C9C	4187	1000	DC9C
008	829C	1418	406F	141A	409C	CA9C	DC00	8C9C
010	1020	14E2	409C	4187	1000	1004	E1FF	DC00
018	CE9C	DC00	8C9C	4187	1000	102B	8200	CF9C
020	DC9C	829C	1418	406F	141A	409C	CA9C	DC10
028	D19C	DC00	D29C	DC00	D39C	DC00	CA9C	DC00
030	8C9C	1020	14E2	409C	4187	1000	1004	E1FF
038	DC00	CE9C	DC00	8C9C	4187	1000	DC9C	829C
040	1418	406F	141A	409C	CA9C	DC00	8C9C	1020
048	14E2	409C	4187	1000	1004	E1FF	DC00	CE9C
050	DC00	8C9C	4187	1000	102B	8200	CF9C	CCC1
058	CD30	CF30	CCC1	CD3D	D13D	CCC1	CD04	CA3D
060	CCC1	CD00	1004	E105	CCC1	CD20	CE3D	CCC1
068	0189	D13D	CCC1	CD02	D23D	CCC1	CD03	D33D
070	CCC1	CD00	D43D	CCC1	CD00	CA3D	CCC1	CD00
078	1025	CF3D	FF50	CCC1	CD30	CF30	CCC1	CD3D
080	D13D	CCC1	CD04	CA3D	CCC1	CD00	1025	CF3D
088	CCC1	CD00	409C	4187	1000	1004	E1FF	DC00
090	CE9C	DC00	8C9C	4187	1000	102B	8200	CF9C
098	DC9C	829C	1418	406F	141A	409C	CA9C	DC10
0A0	D19C	DC00	D29C	DC00	D39C	DC00	CA9C	DC9C
0A8	829C	1418	406F	141A	409C	CA9C	DC10	D19C
0B0	DC00	D29C	DC00	D39C	DC00	CA9C	DC00	8C9C
0B8	1020	14E2	409C	4187	1000	1004	E1FF	DC00
0C0	CE9C	DC00	8C9C	4187	1000	1004	E106	DC9C
0C8	829C	1418	406F	141A	409C	CA9C	DC10	D19C
0D0	DC00	D29C	DC00	D39C	DC00	CA9C	DC00	8C9C
0D8	1020	14E2	409C	4187	1000	1004	E1FF	DC00
0E0	CE9C	DC00	8C9C	4187	1000	1004	E102	DC9C
0E8	829C	1418	406F	141A	409C	CA9C	DC10	D19C
0F0	DC00	D29C	DC00	D39C	DC00	CA9C	DC00	8C9C
0F8	1020	14E2	409C	4187	1000	1004	E1FF	DC00

Newest Entry

Oldest Entry

Figure 1. Maintenance Connection Trace Table Sample

Interrupt Bytes Description

The interrupt-byte table contains four interrupt bytes (0 through 3) for each device address. (See page PDA 5xx to determine the device address assignments)

The bytes are:

- Byte 0 - Owed device end (ODE)
- Byte 1 - Pack change interrupt (PCH)
- Byte 2 - Reserve (RESV)
- Byte 3 - Expected device interrupt (EDI)

Within these four bytes, each bit indicates the channel that is associated with the device, as follows:

- Bit 0 - Channel A
- Bit 1 - Channel B
- Bit 2 - Channel C
- Bit 3 - Channel D
- Bit 4 - Channel E
- Bit 5 - Channel F
- Bit 6 - Channel G
- Bit 7 - Channel H

Owed Device End

When the owed device end (ODE) bit is on, it informs the storage control when this device becomes available and also sends a device end.

When set, this bit indicates that a busy signal was sent (in response to a Start I/O operation) to a logical address for one of the following reasons:

- This physical device has an outstanding EDI interrupt waiting for another channel.
- This logical device is reserved to another channel.
- A different logical address on this physical device has an outstanding EDI interrupt waiting.

This bit is reset when the logical device becomes available and the device end is accepted by the channel. It is also reset by a system reset.

Pack Change Interrupt

When the pack change interrupt (PCH) bit on, the storage control owes a pack change interrupt for this logical device.

The bit is set when the first pack change is accepted by a channel to remember all other logical and physical addresses for which a pack change is owed.

The bit is reset when the processor accepts device end or by a system reset.

Reserve

When the reserve (RESV) bit for a channel is on, the logical device is reserved to the channel and the string switch assignment in the controller is set for the physical device for the control unit.

The bit is set by a reserve command and reset by a release command or by a system reset.

Expected Device Interrupt

When the expected device interrupt (EDI) bit is on, it informs the storage control that the device owed the storage control an interrupt, which in turn owes the channel a device end. When EDI is used with the disconnected command chain, the storage control is disconnected from command chaining.

This bit is set when the control unit disconnects from the drive. It is also set when the channel sends access motion commands, set sector commands, or padding commands are occurring and the next channel command word (CCW) in the chain is not a Format Write command.

In all of the above, the disconnected command chain bit is also set to inform the control unit that command chaining was disconnected.

The bit is also set when the string switch is busy and/or the requested drive is assigned to the other side of the switch.

The bit is reset when the interrupt is accepted by the host processor or by a system reset.

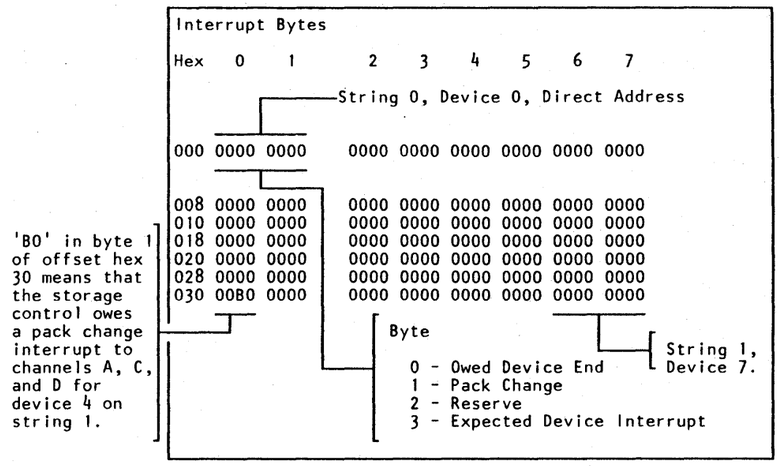
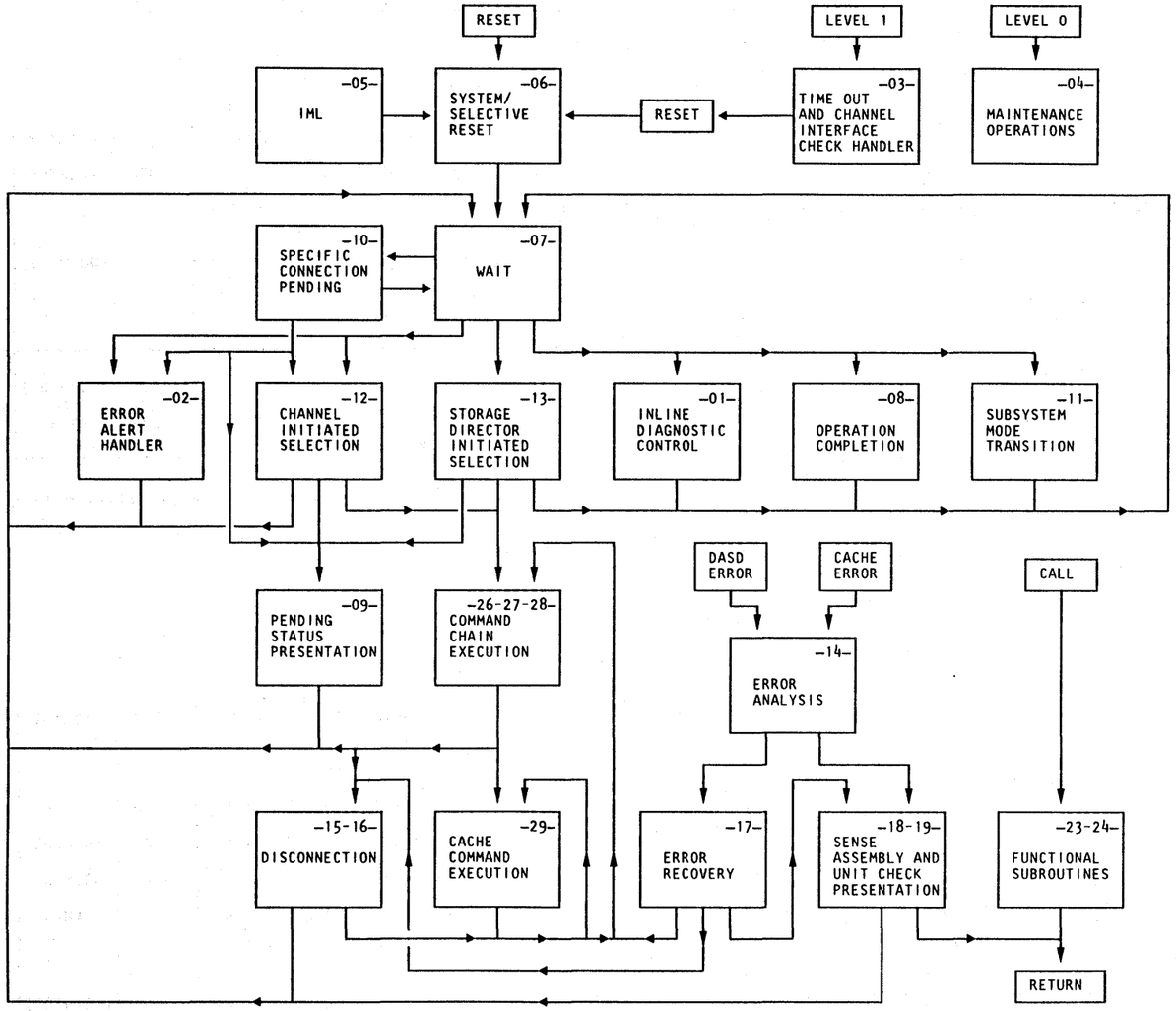


Figure 1. Interrupt Bytes Trace Table Sample

Overview Control Flow for Model 23 PDA 400



Overview Control Flow for Model 23 PDA 400

Inline Diagnostic Control

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B01M101)	---	INLINE CONTROL ENTRY
		INTERNAL
B01M310	002*	INLINE ENTRIES
B01M600	003*	START INLINE OVERLAY AT BEGIN
B01M601	004*	CONTINUE INLINE OVERLAY ENTRY
-------	001*	INVALID SPECIAL COMMAND
		EXIT
B01M715	005*	INLINE CONTROL RETURN TO WAIT BLOCK TO BLOCK B07M000

Timeout and Channel Interface Check Handler

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
B03M102	008*	LEVEL ONE INTERRUPT HANDLER
		EXIT
-------	---	EXIT IS VIA A SELECTIVE RESET TO BLOCK B06M101

System/Selective Reset

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B06M000)	---	POWER ON/SYSTEM/SELECT RESET
(B06M001)	---	RETURN FROM COMMON RESET
(B06M101)	---	COMMON RESET FUNCTIONS
		ERROR EXIT
B06M201	00C*	SELECTIVE RESET FMT 29
		EXIT
B06M002	00A*	TO WAIT FROM SELECTIVE RESET TO BLOCK B07M000
B06M003	00B*	TO WAIT FROM SYSTEM RESET TO BLOCK B07M000

Error Alert Handler

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B02M100)	---	A NEW ERROR ALERT HAS BEEN DETECTED
		INTERNAL
B02M101	006*	TRACE THE NEW ERROR ALERT
B02M102	007*	RETURN TO CALLING BLOCK

Maintenance Operations

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
B04M100	009*	LEVEL ZERO INTERRUPT ENTRY
		INTERNAL
B04M101	---	END OF INTERRUPT LEVEL ZERO RETURN TO PREVIOUS BLOCK

Note: An asterisk (*) identifies sync and save IDs that can be used to initiate a save operation.

Wait

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B07M000)	---	ENTRY TO WAIT
(B07M003)	---	FROM ERROR ALERT HANDLER
		INTERNAL
B07M001	00D*	SELECT WHILE CONTINGENT CONNECTED
		EXIT
-------	---	TO ERROR ALERT HANDLER TO BLOCK B02M100
B07M004	00E*	CHANNEL INITIATED SELECTION TO BLOCK B12M000
B07M005	00F*	SD INITIATED SELECTION TO BLOCK B13M000
B07M006	010*	TO INLINE CONTROL TO BLOCK B01M101
B07M714	011*	ERROR TERMINATION AND EXIT TO BLOCK B18M015
B07M715	012*	SMT DISPATCHER TO BLOCK B11M401

Operation Completion or Continuation

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
B09M000	013*	ENTRY TO PENDING STATUS
		ERROR EXIT
B09M101	016*	ARRAY CANNOT BE INIT OR BAD LTCH FMT 87
B09M201	017*	FORMAT 3 PRESENTATION--ALT SD SENSE VALID FMT 00
B09M202	018*	DEVICE NOT ONLINE FMT 10
B09M203	019*	DPS COMMAND ISSUED TO BASIC MACH FMT 01
B09M204	01A*	UNRESETABLE DEVICE INTERRUPT FMT 14
B09M205	01B*	HOT DEVICE INTERFACE IN-TAGS FMT 73
B09M206	01C*	1/2 SELECTION CODE MISCOMPARE FMT 75
B09M207	01D*	DYNAMIC PATHING INSTALLATION CHK FMT 0C
B09M208	01E*	DEVICE CHECK-2 FMT 16
B09M209	01F*	DEVICE PAD WITHOUT BUSY NOR ATTENTION FMT 18
B09M210	020*	NO MESSAGE FMT 10
B09M211	021*	END OP WITH CONTROLLER/CDP CHK FMT 83
B09M212	022*	USAGE COUNTER OVERFLOW FMT 60
B09M213	023*	CHANNEL BUS OUT PARITY ERROR FMT 00
B09M214	024*	DPS MACHINE SYSTEM RESET INCOMPLETE FMT 86
B09M215	025*	CHNL OVERRUN COUNTER OVERFLOW FMT 6F

Operation Completion or Continuation

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B09M301	026*	POST ERROR LOG MODE CHECK SENSE VALID FMT 00
B09M302	027*	TIME-OUT ON 50 COMMAND FMT 78
B09M304	028*	END-OP ON 18 HEX COMMAND FMT 83
B09M305	029*	TIME-OUT ON CUI SELECTION FMT 7B
B09M306	02A*	UC ON NEXT SIO ON PREV CLEANUP ERROR
B09M307	02B*	NO DEV RESPONSE ON INSTALLED DEV FMT 15
B09M308	02C*	CONTROLLER HAS BEEN FENCED OFF BY SD FMT 7C
B09M309	---	MISSING DEVICE ADDRESS BIT AT SELECTION FMT 1B
B09M310	---	SHORT BUSY TIME OUT FROM SELECTION FMT 88
B09M311	---	A-BOX FAIL TO SET/RESET LONG BUSY LATCH FMT 89
		EXIT
B09M001	014*	RETURN TO WAIT AFTER PENDING STATUS TO BLOCK B07M000
B09M002	015*	EXIT TO WAIT TO BLOCK B07M000

Note: An asterisk (*) identifies sync and save IDs that can be used to initiate a save operation.

Subsystem Mode Transition

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B11M401)	---	SMT DISPATCHER
		ERROR EXIT
B11M101	02D*	BUILD CACHING-TERMINATED SENSE
B11M315	031*	NO CONTROLLER AVAILABLE
B11M410	030*	SMT ERROR HANDLER CACHING TERMINATED
B11M412	032*	SMT ERROR HANDLER LOCK TIMEOUT
B11M413	033*	SMT ERROR HANDLER RESPONSE TIMEOUT
B11M414	034*	SMT ERROR HANDLER LOGIC ERROR
		EXIT
B11M403	02E*	EXIT SMT DISPATCHER TO BLOCK B07M000
B11M415	035*	SMT ERROR HANDLER ERROR TERMINATION AND EXIT TO BLOCK B18M015

Channel Initiated Selection

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B12M000)	---	CHANNEL INITIATED SELECT
		ERROR EXIT
B12M101	---	INTERNAL SELECTIVE RESET-FMT 2C
		EXIT
B12M001	036*	PROPAGATE SELECT OUT FOR NO CONTROLLER TO BLOCK B07M000
B12M002	037*	HIO ON CHNL INITIATED SELECTION TO BLOCK B07M000
B12M003	038*	HIO ON CHNL INITIATED SELECTION TO BLOCK B07M000
B12M004	039*	TO COMMAND EXECUTION FROM SIO TO BLOCK B26M000

Storage Director Initiated Selection

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B13M000)	---	SD INITIATED SELECTION
		EXIT
B13M001	03A*	PROPAGATE SELECT OUT FROM SD INITIATED SELECTION TO BLOCK B07M000
B13M002	03B*	PROPAGATE SELECT OUT DUE TO DPS PATH BUSY TO BLOCK B07M000
B13M003	03C*	HIO ON RECONNECTION TO BLOCK B07M000
B13M004	03D*	TO COMMAND PREPROCESSING TO BLOCK B26M000
B13M005	03E*	HIO FROM SD INITIATED SELECTION TO BLOCK B07M000

Note: An asterisk (*) identifies sync and save IDs that can be used to initiate a save operation.

Error Analysis

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		INTERNAL
B14M002	03F*	ENTER NON-SMB ERROR ANALYSIS
-------	000*	SYMPTOM CODE COMPARE
-------	046*	ENTER SMB ERROR ANALYSIS
		ERROR EXIT
B14M101	044*	CHECK 2 HANDLER FMT FF
B14M102	045*	CHK 2 HANDLER WITH UC EARLY FMT FF
		EXIT
B14M003	040*	EXIT TO SEEK RETRY TO BLOCK B17M003
B14M010	041*	EXIT TO TERMINATOR WHEN CHAIN ABORTS BEFORE SENSE ASSEMBLY TO BLOCK B16M000
B14M011	042*	EXIT TO SENSE ASSEMBLY TO BLOCK B18M000
B14M012	043*	EXIT TO PRESENT UNIT CHECK TO BLOCK B18M001
B14M303	047*	RETURN TO CHIP CHECK TWO RESET BY ERROR ANALYSIS BLOCK TO BLOCK B27M100

Disconnection

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B15M600)	---	PRESENT DEVICE END STATUS
(B15M601)	---	PRESENT CHANNEL END DEVICE END STATUS
(B15M700)	---	INTERNAL DISCONNECTION
(B15M701)	---	DASD MODE DISCONNECTION
(B16M000)	---	ENTRY TO TERMINATOR
(B16M014)	---	END-OF-CHAIN CLEANUP
		INTERNAL
B16M002	049*	HIO OR STACKED END STATUS
B16M004	---	ENTRY TO TERMINATOR
		ERROR EXIT
B16M101	04C*	TIMED OUT WAITING FOR CTL-I FMT 7A
		EXIT
B16M001	048*	TO WAIT FROM CONTINGENT CONNECT TO BLOCK B07M000
B16M003	04A*	TO WAIT FROM NORMAL TERMINATION TO BLOCK B07M000
B16M015	04B*	OPERATION COMPLETE BREAKOUT TO BLOCK B29M304

Error Recovery

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B17M003)	---	ENTRY TO SEEK RETRY
(B17M009)	---	ENTRY TO OFFSET ACTIVE RETRY
(B17M500)	---	ENTRY TO RETRY/SENSE ASSEMBLY
		INTERNAL
B17M207	050*	START DEVICE INTERRUPT PROCESS
B17M208	051*	DATA CHECK DURING PCI MODE
B17M209	052*	ANALYZE CHECK TWO
B17M210	053*	PERMANENT ERROR
B17M211	054*	PERMANENT INTERNAL ERROR
B17M212	055*	CHANNEL ABORTED RETRY PATH
B17M213	056*	PREPARE FOR SENSE ASSEMBLY
B17M215	058*	INTERNAL SEEK CHECK RETRY
B17M305	05A*	DEVICE COMMAND OVERRUN
B17M401	05B*	DEVICE ERROR ON CHANNEL X
B17M402	05C*	CACHE ERROR ON CHANNEL X
B17M403	05D*	STG DIR ERROR ON CHANNEL X
B17M503	064*	CYLINDER CROSSING
B17M504	065*	INTERNAL CYLINDER CROSSING
B17M507	066*	ACTIVE OFFSET RETRY
B17M508	067*	UNCORRECTABLE DATA CHECK
B17M509	068*	NO OFFSET NEEDED
B17M510	069*	CORRECTABLE DATA CHECK

(Continued)

Note: An asterisk (*) identifies sync and save IDs that can be used to initiate a save operation.

Error Recovery (Continued)

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B17M511	06A*	CORRECT COUNT OR KEY
B17M512	06B*	IGNORE DATA CHECK - CORF>DORF
B17M513	06C*	NO SYNC/NO DATA RETRY
B17M514	06D*	PA AND SEEK MISCOMPARE RETRY
B17M515	06E*	DEFECTIVE/ALTERNATE TRACK
B17M600	06F*	COMMAND OVERRUN RETRY
B17M601	070*	DATA OVERRUN RETRY
B17M602	071*	SCAN CAUSED INTENT VIOLATION
B17M603	072*	ALTER RECOVERY
B17M605	073*	CHANNEL AHEAD WHILE READING
B17M606	074*	INTERNAL DATA CHECK RETRY
B17M607	075*	INTERNAL RETRY NO OFFSET
B17M608	076*	INTERNAL CORR DATA CHK
B17M609	077*	RESTORE NON-SMB ENVIRONMENT
B17M610	078*	RESTORE SMB ENVIRONMENT
B17M613	07B*	EXIT TO COMMAND DECODE
B17M700	07E*	HALT I/O CLEAN UP
B17M704	07F*	DEVICE ERROR OFF CHANNEL
B17M705	080*	CACHE ERROR OFF CHANNEL
B17M706	081*	STORAGE DIRECTOR ERROR OFF CHANNEL
B17M707	082*	3380 HEAD SETTLE
B17M709	083*	INTERNAL NO SYNC/DATA RETRY
B17M710	084*	RETRY RECONNECTION FAILED
		ERROR EXIT
B17M205	04E*	BUS OUT PARITY CHECK
B17M206	04F*	INCORRECT CCW RETRIED
B17M214	057*	CHANNEL DID NOT HONOR RETRY

Error Recovery

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B17M301	059*	UNRESETABLE OFFSET EQUIP CHECK FMT 1F
B17M404	05E*	TIMED OUT ON IMMEDIATE OP FMT 78
B17M405	05F*	END OP TO A MODIFIER SEQUENCE FMT 83
B17M406	060*	DRIVE LOGIC CHECK FMT 10
B17M407	061*	INVALID REPONSE CODE FMT 83
B17M408	062*	INVALID RESPONSE CODE FMT 83
		EXIT
B17M204	04D*	EXIT TO COMMAND DECODE TO BLOCK B26M002
B17M415	063*	EXIT TO CHOPS OPERATION COMPLETE BREAKOUT TO BLOCK B29M304
B17M611	079*	EXIT TO SENSE ASSEMBLY TO BLOCK B18M000
B17M612	07A*	EXIT TO TERMINATOR FROM CHANNEL ABORT RETRY TO BLOCK B16M000
B17M614	07C*	EXIT TO COMMAND DECODE TO BLOCK B26M002
B17M615	07D*	EXIT TO COMMAND DECODE TO BLOCK B26M002

Sense Assembly and Unit Check Presentation

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B18M000)	---	SENSE ASSEMBLY
(B18M001)	---	UNIT CHECK PRESENTATION
(B18M015)	---	ERROR TERMINATION AND EXIT
		ERROR EXIT
B18M101	087*	TAG SEQUENCE CHECK FMT 28
B18M103	088*	DEVICE BUS IN CHK FMT 85
B18M104	089*	SYNC IN/TAG OUT FAULT FMT 84
B18M106	08A*	DCC BUS IN PARITY CHECK FMT 80
		EXIT
B18M002	085*	CLEAN UP AFTER SENSE ASSEMBLY TO BLOCK B07M000
B18M014	086*	END OF CHAIN PROCESSING TO BLOCK B16M014

Note: An asterisk (*) identifies sync and save IDs that can be used to initiate a save operation.

Functional Subroutines

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		INTERNAL
B23M710	0B6*	TERMINATE SMB ENVIRONMENT
		ERROR EXIT
B23M101	08D*	HANDLE TIME OUT WAIT FOR END OP
B23M102	08E*	MISSING INDEX ERROR
B23M301	090*	END OP TRANSFER COUNT EQUAL ZERO FMT 85
B23M305	091*	END OP TRANSFER COUNT NOT EQUAL ZERO FMT 84
B23M306	092*	CCA OR TAG-IN CHECK FMT 70
B23M307	093*	STUCK END OP FMT79
B23M309	094*	INVALID TRACK FORMAT FMT 00
B23M310	095*	DRIVE LOGIC CHECK FMT 10
B23M311	096*	DATA CHECK RETRY FMT 80
B23M312	097*	NO SYNC FOUND RETRY FMT 80
B23M313	098*	COMMAND OVERRUN RETRY FMT 20
B23M314	099*	UNEXPECTED RESPONSE CODE FMT 83
B23M315	09A*	DATA OVERRUN RETRY FMT 10
B23M403	09B*	DEVICE STATUS NOT AS EXPECTED FMT 11
B23M404	09C*	SET SECTOR INCOMPLETE FMT 16
B23M405	09D*	NO SEEK/SET SECTOR COMPLETE IN TIME FMT 11

Functional Subroutines

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B23M406	09E*	MISSING END OP FMT 79
B23M407	09F*	TIMEOUT ON IMMEDIATE OP FMT 78
B23M408	0A0*	DRIVE LOGIC CHECK FMT 10
B23M409	0A1*	END OP TO AN IMMEDIATE OP FMT 80
B23M410	0A2*	TIMED OUT ON IMMEDIATE OP FMT 78
B23M411	0A3*	END OP TO A MODIFIER SEQUENCE FMT 83
B23M414	0A4*	CCA OR NO CONTROLLER RESPONSE TO SELECT FMT 70
B23M415	0A5*	INVALID DCC SELECTION RESPONSE FMT 75
B23M507	0A6*	TIMEOUT ON PARM PASS FMT 78
B23M508	0A7*	END-OP ON PARM PASS FMT 83
B23M509	0A8*	CONTROLLER FENCED OFF FMT 7C
B23M510	0A9*	DATA LOCK CAN NOT BE SECURED FMT 80
B23M511	0AA*	EXTRA RCC REQUIRED FMT 74
B23M512	0AB*	END OP RESPONSE FMT 80
B23M513	0AC*	TIME OUT WAITING FOR SELECTED NULL FMT 78
B23M514	0AD*	TIME OUT WAITING FOR SELECTED NULL FMT 78
B23M515	0AE*	NO SENSE FAULT LOG IF DEVICE CHECK 2 FMT 79

Functional Subroutines

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B23M601	0AF*	PA MISCOMPARE FMT 1E
B23M602	0B0*	SEEK INCOMPLETE FMT 1D
B23M611	0B1*	NO EXPECTED STATUS IN TIME FMT 11
B23M612	---	DIAG CCW NOT ALLOWED FOR DIAGNOSTIC CNTL FMT 02
B23M613	---	INVALID ARGUMENT FMT 02
B23M701	0B2*	END OP ON ARRAY DATA TRANSFER FMT 85
B23M702	0B3*	TIMEOUT ON IMMEDIATE OP FMT 78
B23M708	0B4*	INTENT COUNT NOT EXPIRED
B23M709	0B5*	TIMED OUT WAITING FOR DIP TO STOP DURING SMB ENVIRONMENT TERMINATION
B24M101	0B7*	MICROCODE LOGIC ERROR
B24M102	0B8*	OPERATION TERMINATED
B24M103	0B9*	HARDWARE ERROR OCCURRED
B24M400	0BA*	DIRECTORY LOGIC ERROR
		EXIT
B23M000	08B*	TERMINATE FROM QUEUED SEEK DCC TO BLOCK B16M000
B23M001	08C*	HIO OR STACKED STATUS ON STATUS PRESENTATION TO BLOCK B16M000
B23M200	08F*	EXIT CACHE OPERATION COMPLETE TO BLOCK B29M304

Command Chain Execution

TRACE OR (ID ONLY)	SYNC AND SAVE*	
		ENTRY
(B26M000)	---	SET UP FOR COMMAND DECODE
(B26M002)	---	COMMAND DECODE
(B27M100)	---	CHECK TWO RESET BY ERROR ANALYSIS BLOCK
(B29M300)	---	CHOPS NEW TRACK PROCESSING
(B29M303)	---	CYLINDER CROSSING CLEANUP
(B29M304)	---	OPERATION COMPLETE BREAKOUT
		INTERNAL
B26M003	0BB*	TO DCC HOUSEKEEPING FOR PAD
B27M000	0DC*	INITIALIZE SMB ENVIRONMENT AND START DIP
B27M110	0E6*	CHIP DETECTS DIP IN THE ERROR STATE
B29M302	10F*	PROCESS COMMANDS WITH DEVICE
B29M307	112*	PROCESS COMMANDS WITH DEVICE
		ERROR EXIT
B26M100	0BC*	INTERVENTION REQUIRED DUE TO SPINDLE NOT UP FMT 10
B26M101	0BD*	BUS OUT PARITY CHECK FMT 00
B26M102	0BE*	INVALID STATUS 1 FMT 18
B26M104	0BF*	INVALID CCW SEQUENCE FMT 02
B26M105	0C0*	SEEK INCOMPLETE RETRY FMT 40
B26M106	0C1*	INVALID COMMAND CODE FMT 01
B26M107	0C2*	UNEXPECTED DEVICE STATUS EQUIPMENT CHECK FMT 11
B26M108	0C3*	BUS OUT PARITY CHECK--NOT RETRIABLE FMT 00
B26M109	0C4*	DEVICE CHECK-2 IN STATUS FMT 16

Command Chain Execution

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B26M506	0C5*	RECALIBRATE NOT ALLOWED IN FILE MASK FMT 00
B26M509	0C6*	SPID MUST BE FIRST CCW IN CHAIN FMT 02
B26M510	0C7*	INVALID ARGUMENT--SPID FMT 04
B26M512	0C8*	INVALID ARGUMENT--SPID FMT 04
B26M601	0C9*	SET FILE MASK CCW NOT ISSUED FMT 02
B26M602	0CA*	CONTROLLER UNSELECTED BEFORE UNCONDITIONAL RESERVE COMMAND FMT 70
B26M603	0CB*	INVALID DCC IN TAG SEQUENCE FMT 73
B26M604	0CC*	INVALID DCC SELECTION RESPONSE FMT 75
B26M605	0CD*	TIMED OUT ON IMMED OP FMT 78
B26M606	0CE*	DRIVE CHECK FMT 18
B26M607	---	CE DEVICE ENTERVENTION REQUIRED
B26M608	0CF*	CONTROLLER/ADP EQUIPMENT CHECK FMT 80
B26M614	0D0*	SENSE ID NOT FIRST CCW IN CHAIN FMT 02
B26M700	0D1*	COMMAND REJECT - INVALID SEQUENCE
B26M701	0D2*	COMMAND REJECT - INVALID ARGUMENT
B26M702	0D3*	FILE PROTECT
B26M703	0D4*	COMMAND REJECT - DIAG DISALLOWED
B26M704	0D5*	SEEK CHECK RETRY
B26M705	0D6*	STATUS NOT AS EXPECTED
B26M706	0D7*	STATUS NOT ON-LINE
B26M707	0D8*	NO INTERRUPT FROM FILE
B26M708	0D9*	CHANNEL BUS OUT PARITY CHECK

Command Chain Execution

Note: An asterisk (*) identifies sync and save IDs that can be used to initiate a save operation.

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B26M709	0DA*	INSUFFICIENT CCW COUNT FMT 03
B26M710	0DB*	HEAD OFFSET RETRY FMT 80
B26M711	---	VTOC WRITE INHIBIT FMT 00
B27M101	0DD*	COMMAND REJECT - CCW COUNT LESS THAN REQUIRED
B27M102	0DE*	COMMAND REJECT - INVALID/IMPROPER HA DATA
B27M103	0DF*	CHIP HAS INSUFFICIENT LEAD OVER DIP
B27M104	0E0*	NO CHANNEL END OF TRANSFER
B27M105	0E1*	CHANNEL BUFFER POINTER NOT AS PREDICTED
B27M106	0E2*	CHIP DETECTS BUFFER CYCLIC REDUNDANCY CHECK
B27M107	0E3*	NO RECORD FOUND - INDEX TWICE ON S/T SEARCH
B27M108	0E4*	CHIP TIMES OUT WAITING FOR DIP
B27M109	0E5*	CHIP DETECTS INVALID TRACK FORMAT
B27M111	0E7*	STACKED STATUS OR HALT I/O
B27M111	---	CHIP DETECTS CHECK TWO AT CHANNEL END OF TRANSFER. VARIABLES ARE XES AND CHK
B27M112	0E8*	COMMAND REJECT - INVALID SEQUENCE
B27M113	0E9*	COMMAND REJECT - DIAG DISALLOWED FM
B27M114	0EA*	PCI INTERRUPT - FM INDICATES PCI REQUIRED
B27M115	---	COMMAND REJECT - INHIBIT WRITE
B28M000	0EB*	FILE STATUS REQUIRING RESET
B28M001	0EC*	INVALID FILE STATUS
B28M002	0ED*	NO SYNC/NO DATA
B28M003	0EE*	DATA CHECK DBI = X'03'
B28M004	0EF*	DIP DETECTS CHECK TWO
B28M005	0F0*	NO RECORD FOUND
B28M006	0F1*	RECORD ZERO NOT FOUND
B28M007	0F2*	FIRST RECORD NOT IN EXTENT

Command Chain Execution

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B28M008	0F3*	END-OF-CYLINDER ERROR
B28M009	0F4*	CYLINDER CROSSING
B28M010	0F5*	HEAD SWITCH ON ALTERNATE TRACK
B28M011	0F6*	NO RECORD FOUND ON INTERNAL FIND
B28M012	0F7*	MISSING DEVICE END OP INTERRUPT
B28M100	0F8*	OFFSET RESET - REALIGN THE HEAD
B28M101	0F9*	DIP DETECTS COMMAND OVERRUN
B28M103	0FA*	RESIDUAL COUNT RETRY
B28M104	0FB*	DIP DETECTS INVALID TRACK FORMAT
B28M105	0FC*	PHYSICAL ADDRESS MISCOMPARE
B28M106	0FD*	PHYSICAL ADDRESS HEAD MISCOMPARE
B28M107	0FE*	ORIENTED PHYSICAL ADDRESS MISCOMPARE
B28M108	0FF*	DIP DETECTS NO CHANNEL END OF TRANSFER
B28M109	100*	DEFECTIVE TRACK
B28M110	101*	DEVICE BUFFER POINTER NOT AS PREDICTED
B28M111	102*	DIP DETECTS CHANNEL BUFFER POINTER NOT AS PREDICTED
B28M112	103*	MISSING DEVICE END-OF-TRANSFER INTERRUPT
B28M200	104*	DIP DETECTS BUFFER CYCLIC REDUNDANCY CHECK
B28M202	105*	UNEXPECTED DIP INTERRUPT
B28M203	106*	FORMAT WRITE ON DEFECTIVE TRACK
B28M204	107*	DEVICE COUNTER NOT ZERO
B28M205	108*	RECORD LENGTH NOT AS DEFINED
B28M206	109*	DIP DETECTS STATUS PRESENTATION ERROR
B28M207	10A*	DIP ENTERS IDLE STATE
B29M701	114*	END OF CYLINDER
B29M702	115*	NO RECORD FOUND
B29M703	116*	FILE PROTECT
B29M704	117*	INVALID COMMAND

Command Chain Execution

TRACE OR (ID ONLY)	SYNC AND SAVE*	
B29M705	118*	INVALID SEQUENCE
B29M706	119*	INVALID ARGUMENT
B29M707	11A*	CHANNEL DISCONTINUED RETRY
B29M708	11B*	INVALID RETRY CCW
B29M710	11C*	LOGICAL ERROR SENSE
B29M711	11D*	FORMAT FO SENSE
B29M712	11E*	CACHE ERRORS
		EXIT
B29M002	10B*	SENSE SUBSYSTEM STATUS COMMAND ERROR TERMINATION TO BLOCK B18M015
B29M004	10C*	PRESENT CHANNEL END/DEVICE END TO BLOCK B15M601
B29M008	10D*	PRESENT DEVICE END TO BLOCK B15M600
B29M100	10E*	EXIT FROM CACHE TO DASD MODE TO BLOCK B15M701
B29M305	110*	PRESENT DEVICE END STATUS TO BLOCK B15M600
B29M306	111*	EXIT FROM END OF CHAIN TO BLOCK B16M014
B29M600	113*	FROM INTERNAL PROMOTION PROCESSOR TO INTERNAL DISCONNECTION PROCESSING TO BLOCK B15M700
B29M601	02F*	EXIT FROM CACHE SECTOR PROCESSING TO ERROR TERMINATION AND EXIT TO BLOCK B18M015
B29M713	11F*	EXIT FROM CHOPS ERROR HANDLER TO ERROR TERMINATION AND EXIT TO BLOCK B18M015

Sync and Save Tables for Model 23

Note: An asterisk (*) identifies sync and save IDs that can be used to initiate a save operation.

DIRECTORY OF STATE SAVE TABLES FOR MODEL 23 PAGE

DIRECTORY OF STATE SAVE TABLES FOR MODEL 23 PAGE

EXTERNAL REGISTERS

The external registers are summarized in the REF section of the MSM.

INTERNAL REGISTER DEFINITION

GROUP 10-REGISTER 4 TRACK ORIENTATION REGISTER

BIT	NAME
0	Oriented for write
1	Retry active
2	First CCW since DASD data transfer mode was initialized
3	Format write/pad reconnection
4	Read/write mode on
5	DASD data transfer mode
6,7	Intent descriptors '00' = Read '01' = Update write '10' = Format write '11' = Track write

GROUP 10-REGISTER 6 FILE MASK

BIT	NAME	DESCRIPTION
0	Write HA	0 - Inhibit Write HA, R0 1 - Permit Write HA, R0
1	Format write	0 - Permit all format write except Write HA, R0 1 - Inhibit all format write except Write HA, R0
2	Non-format write	0 - Permit all non-format write 1 - Inhibit all non-format write
3,4	Seek	'00' = Permit all seek commands '01' = Permit Seek Cylinder and Seek Head '10' = Permit Seek Headnder and '11' = Inhibit all seek commands
5	Diagnostic mode/seek to CE trks only/ Inhibit retry on HA	0 - Not in diagnostic mode. Allow data check retry on HA fields 1 - Diagnostic mode. Allow diagnostic commands. Allow seek to CE tracks only. Inhibit seek to non-CE tracks. Inhibit data check retry on HA fields.
6	SFM issued	0 - No Set File Mask issued in chain 1 - Set File Mask issued in chain
7	PCI fetch mode	0 - Non-PCI fetch mode 1 - PCI fetch mode

GROUP 10-REGISTER 7

This register contains the CCW being processed.
Set by the initial selection microcode.
Reset by the next CCW overlaying the previous command.

GROUP 12-REGISTER 4, 5, 6, 7

These registers are used to count the number of bytes read from the count, key, or data fields of the device for the duration of a CCW chain (read usage counter). Initialized by a SIO to zeroes.
Updated by count, key, or data field setup.
Reset by disconnection cleanup.

INTERNAL REGISTER DEFINITION (WHEN NOT IN DASD DATA TRANSFER MODE)

GROUP 10-REGISTER 0 READ/WRITE MARKS

BIT	NAME	DESCRIPTION
0	Channel End presented	Set when CE has been sent to the channel without Device End. Reset by sending DE to the channel.
1	No Seek on Read IPL	Set when Seek is suppressed on Read IPL. Reset by Read IPL command execution.
2	Offset active	Set whenever actuator is offset from center of track. Reset by command CCW, initial selection, or reset offset.
3-5		Unused
6	Queued Seek	Set by Queued Seek. Reset by initial selection.
7	Queued Seek at EOC	Set by disconnect command chain for queued seek. Reset by initial selection.

GROUP 10-REGISTER 1 RETRY FLAGS

BIT	NAME	DESCRIPTION
0-3		Unused
4	Initial Selection presented for DCC	Set by presentation of initial status/DCC in progress. Reset by control command/start read/write/No Op/disconnected cleanup.
5		Unused
6	Seek incomplete	Set by initial selection/ reconnection. Reset by command decode after SCB has been set up for Seek retry.
7	Bypass error	Set by sense assembly to indicate that errors should not be checked. Reset by sense assembly.

GROUP 10-REGISTER 2 DCC COMMAND

This register contains the device command. Set before command execution. Reset by the next device command overlaying the previous command. Overlayed when DASD data transfer mode is entered.

GROUP 10-REGISTER 5 FLAG BYTE

This register is set equal to the flag byte in the HA or count field. It is used for count field processing. Valid only after track orientation. When DASD data transfer mode is entered, bits 6 and 7 are moved to register 6 of group 11 (DIP flags).

BIT	NAME	DESCRIPTION
0-5		Unused
6		Defective track
7		Alternate track

GROUP 11-REGISTER 0 DETECTION MARKS FOR INITIAL SELECTION

This register contains detection marks for initial selection. It is set during initial selection. It is reset by overlaying.

BIT	NAME	DESCRIPTION
0		ODE/PCH detected
1		DPS-busy path detected
2		Seek/SS attention detected
3		Device HDA attention detected
4		SPID/SNID command mark
5		TIO command mark
6		CU end mark (CU initiated selection only)
7		Primed Device End (device busy during selection)

GROUP 11-REGISTER 1 DETECTION MARKS FOR INITIAL SELECTION

This register contains detection marks for initial selection. It is set during initial selection. It is reset by overlaying.

BIT	NAME	DESCRIPTION
0		Device not available to this channel
1		Hot interface mark
2		Intervention required
3		1/2 selection code error
4		Sense command (X'04') mark
5		SIO (channel initiated selection) mark
6		Sense type command mark
7		Device end-op detected

GROUP 11-REGISTER 2 BIT SIGNIFICANT DEVICE ADDRESS (BSDS)
This register contains the device address (bit significant). Set by initial selection. Reset by the new device address overlaying the previous address.

GROUP 11-REGISTER 3 BINARY STRING ADDRESS (BNSS)
This register contains the binary string address. Set by initial selection. Reset by the next string address overlaying the previous address.

GROUP 11-REGISTER 4 BIT SIGNIFICANT CHANNEL ADDRESS (BSCS)
This register contains the bit significant channel mask. Set by initial selection. Reset then overlaid by the next channel mask.

GROUP 11-REGISTER 5
BASIC/DPF MACHINE ID (DPFS)

Bits 0-3 are set during array initialization and are permanent.
Bits 4-7 are set during channel selection and are reset when overlaid during the next initial selection.

BIT	NAME	DESCRIPTION
0		Machine type validated
1		Array initialization complete
2		Storage director connected to controller A2
3		DPS machine
4		Basic/DPS non-symmetry error
5		End-op detected during non-level-3 code execution
6		Previously selected (A/B box)
7		Selection end-op but array already initialized

GROUP 11-REGISTER 6 LOGICAL DEVICE ADDRESS (LDAS)
This register contains the logical device address. The format is: 000CDDDD, where 'C' is the controller and 'DDDD' is the device.

GROUP 11-REGISTER 7
IDLE STATUS INFORMATION (IDSS)

BIT	NAME	DESCRIPTION
0	Contingent connection	Set by presentation of unit check Reset by a Sense command or initial selection.
1	Stacked status	Set by check chaining if status is stacked. Reset by execution of any valid initial status.
2	Unit Check to next TIO/SIO	Set by channel overrun counter overflows in retry/alternate Genoa check. Reset by clear status on initial selection if bits 3 and 4 are off, or by a Sense command if bits 3 and 4 are on.
3	Sense data valid	Set by environmental sense data assembly routine or unit check presentation/sense assembly routine. Reset by initial selection with clear initial status or sense commands during command execution.
4	Error log buffer valid	Set by error log mode active and in retry routine. Reset by retry routine if the error is not successfully recovered or if bit 3 is on by the execution of a Sense command.
5	Device selected	Set if valid response to 'sense status 1' after device selection. Reset by device deselection.
6	Do not update available on DPS deselection	Set by command execution if the contingent connection bit is set. Reset by end of chain cleanup.
7	Device type	Set by initial selection. Reset by check chaining.

INTERNAL REGISTER DEFINITION FOR DASD DATA TRANSFER MODE

The following registers are valid in DASD data transfer mode. If bit 5 of the track orientation register (register 4 of group 10) is on, these registers are valid. If bit 5 is off, the non-DASD data transfer mode registers should be used. These registers are valid in blocks 27 and 28 only.

GROUP 6-REGISTER 0 FIND ARGUMENT (RECORD)

This register contains the record portion of the find argument used by the internal find operation.

GROUP 6-REGISTER 1 KEY LENGTH

This register contains the key length of the device interface processor's (DIP) record. (The device interface processor (DIP) is called the auxiliary microprocessor in other sections of the documentation)

GROUP 6-REGISTERS 2, 3 DATA LENGTH

This register contains the data length of DIP's record.

GROUP 6-REGISTERS 4-7 DATA LENGTH

These registers contain the cylinder and head portions of the find argument used by the internal find operation.

GROUP 7-REGISTERS 0, 1 CHANNEL ORIENTATION RECORD AND FIELD (CORF)

BIT	NAME	DESCRIPTION
0-3	Relative index count	Contains the difference between the number of times the channel interface processor (CHIP) has passed index and the number of times the device interface processor (DIP) has passed index. If negative, DIP is ahead. (The CHIP and DIP are called the microprocessor and auxiliary microprocessor, respectively, in other parts of the documentation)
4-7	CORF field	Indicates which field (count, key, data) CHIP is operating on.
8-15	CORF record	Indicates which record CHIP is operating on.

GROUP 7-REGISTER 2 DIP STATE

This register contains the DIP state indicators and global flags describing DIP.

BIT	NAME	DESCRIPTION
0	Status presentation	If set, DIP can perform status presentation; otherwise CHIP must perform it.
1	Stop DIP control	If set, go to the idle state without completing the present operation.
2	High speed channel	Indicates that the channel program is running on a high-speed channel.
3	Intent active	Indicates a non-zero intent count
4	Write intent	If active, indicates write intent; otherwise it indicates read intent.
5-7	DIP state	The status of DIP operations: '000' = Idle - DIP is no longer running. '010' = Error - DIP detected an error. DUSCB in control storage describes the error. '100' = Exec active - DIP is executing something from the op list. '101' = Exec inactive - DIP encountered the next device field when the op list was empty. DIP will read the next field. '110' = First gap - DIP has completed a non-format write operation, and either needs another op or is close to index. '111' = Padding warning - DIP has completed a format write operation, needs another op, and is not close to index. If another format write is not available when the next field begins, padding will begin.

GROUP 7-REGISTER 3 BOTTOM OF BUFFER

This register contains the high-order byte of a 16 bit buffer address that contains the address of the next 256 byte buffer page to be allocated.

GROUP 7-REGISTERS 4, 5 NEXT OPERATION/FIELD

These registers contain the next operation/field (NOF). They identify the next operation for DIP to perform and the fields to process.

BIT	NAME
0	Home address
1	RO count
2	Count
3	Key
4	Data
5	Field modifier
6	Reserved
7	Stop - indicates that DIP should enter idle
8	Read
9	Update write
10	Format write
11	Space
12	Operation modifier
13	Status sync - causes DIP to call channel status presentation upon device completion.
14	Find operation
15	Multitrack operation

GROUP 7-REGISTERS 6, 7 DEVICE ORIENTATION RECORD AND FIELD (DORF)

BIT	NAME	DESCRIPTION
0-3		Unused
4-7	DORF field	Indicates which field (count, key, data) DIP is operating on.
8-15	DORF record	Indicates which record DIP is operating on.

GROUP 7-REGISTER 4, 5 NEXT OPERATION/FIELD

This register contains the next operation/field (NOF). NOF identifies the next operation for DIP to perform, and the field for DIP to process.

BIT	NAME
0	HA
1	RO count
2	Count
3	Key
4	Data
5	Field modifier
6	Reserved
7	Stop - indicates that DIP should enter idle
8	Read
9	Update write
10	Format write
11	Space
12	Operation modified
13	Status sync - Causes DIP to call status presentation upon device op completion.
14	Find operation
15	Multitrack operation

GROUP 7-REGISTERS 6, 7 DEVICE PRESENTATION RECORD AND FIELD (DORF)

BIT	NAME	
0-3	Unused	
4-7	DORF field	Indicates which field (count, key, data) DIP is operating on.
8-15	DORF record	Indicates which record DIP is operating on.

GROUP 8-REGISTER 0 EXPECTED RLL

This register contains the expected ending value of RLL. If the actual value differs from this at end end of transfer, a format two unit check is indicated.

GROUP 8-REGISTER 6, 7 EXPECTED DBH, DBL

This register contains the expected ending value of DBH and DBL. If the actual value differs from this at the end of transfer, a format two unit check is indicated.

GROUP 9-REGISTER 4 CHANNEL BEGINNING OF BUFFER

This register is the high order byte of a 16 bit buffer address. It contains the address of the first 256 byte buffer page to be allocated by chip. This page contains the count field of the record of interest to CHIP.

GROUP 9-REGISTER 5 BUFFER ORIENTATION RECORD
This register indicates which record CBOB (R4G9) is pointing to.

GROUP 9-REGISTER 7 OP LIST TAIL POINTER
This register points to one step beyond the end of the device op queue. Chip uses the op list tail pointer to add operations to the device op list in control store. After every addition, this register is incremented. When the end of the op list is reached, the pointer wraps around to the beginning.

GROUP 10-REGISTER 3 EXPECTED CBL
This register contains the expected ending value of CBL. If the actual value differs from this at end of transfer, a format two condition is flagged.

GROUP 10-REGISTER 5 CURRENT INTENT ACCOUNT
This register indicates the number of records remaining in the current intent count. It is decremented once for every record transferred by chip.

GROUP 11-REGISTER 0 DCC COMMAND
This register indicates the last DCC command to be sent to the device.

GROUP 11-REGISTER 4 DEVICE BEGINNING OF BUFFER
This register is the high order byte of a 16 bit buffer address. It contains the address of the first 256 byte buffer page to be allocated by DIP. This page contains the count field of the record of interest to DIP.

GROUP 11-REGISTER 5 OP LIST HEAD POINTER
This register points to the beginning of the device op queue. DIP uses the op list head pointer to remove operations from the device op list in control store. After every deletion, this register is incremented. When the end of the op list is reached, the pointer wraps around to the beginning.

GROUP 11-REGISTER 6
DIP LIST

BIT	NAME
0	Offset activity
1	Fixed head
2	Index passed flag
3	PCI interrupt
4	Count valid
5	Key valid
6	Defective track
7	Alternate track

GROUP 11-REGISTER 7 TOTAL INTENT COUNT
This register indicates the total intent count. This is the sum of the active intent count, and the remaining intent count.

GROUP 12-REGISTER 1 CHANNEL KEY LENGTH
This register contains the key length of the record of interest to the channel.

GROUP 12-REGISTERS 2,3 CHANNEL DATA LENGTH
This register contains the data length of the record of interest to the channel.

GROUP 13-REGISTERS 0,1 SEGMENT FIELD LENGTH
This register contains DIP's segment field length, in bytes.

GROUP 13-REGISTERS 2,3 SEGMENT CELL NUMBER
This register contains the segment field length, in cell numbers.

GROUP 13-REGISTERS 4,5 CELL NUMBER
This register contains the segment field length, in cell numbers.

GROUP 13-REGISTERS 6,7 DIP FIELD LENGTH
This register contains DIP's field length. This is the value loaded into DCH and DCL, before each transfer.

INTERNAL REGISTER DEFINITION FOR INLINE CONTROL BLOCK

GROUP 10-REGISTER 4		
BIT	NAME	DESCRIPTION
0	Waiting for data received	Set when a display byte has been presented to the MD and a response is expected.
1	3880 routine request.	Set when an inline/offline ID request is received for the 3880 routine overlay band.
2	Trace all/ single option	Set when the trace '3D' option is '02' or '03'.
3	Trace dump primed	Set when trace '30' option is '04' (trace dump). Waiting for the start command. Reset when the dump is started.
4	Trace error display	Set when a trace error is about to be displayed. Reset when a new function is requested.
5	Inhibit link	Run option entered by CE.
6	Loop routine	Run option entered by CE.
7	Bypass error	Run option entered by CE.

GROUP 10-REGISTER 5		
BIT	NAME	DESCRIPTION
0	Inline return primary group = 3.	IRG value when inline returns has primary group 3.
1	CE wait image	Used by inline control to remember that CE wait was on.
2	Trace dump	Set when a trace dump has been initiated. Reset when the trace dump is complete.
3	Maintenance device (MD) mode	Set when a '3B' command is received. Reset when a '30' command is received.
4-7	Inline entry to inline control code	Bits 4-7 are set to a code when and inline/offline routine exits to inline control. The code is used for steering of the microcode.

GROUP 10-REGISTER 6		
BIT	NAME	DESCRIPTION
0	CE wait	Set when inline control determines that an entry is required by the CE before further processing is to be done.
1	Maintenance bus test mode	Set when a 'C0' command is received. Reset when the two bytes which test the maintenance bus are echoed back to the MD.
2-3	Data entry status	These two bits are set to describe the type of data which is being entered. Entered: 00 - No data is being entered 01 - Parameter entry mode 10 - Address entry mode 11 - Known error stop entry mode
4-5	Wait status	These two bits are set to steer inline control when a start command is received: 00 - Initial entry 01 - Inline diagnostic error 10 - End of diagnostic linked series 11 - Diagnostic halt, etc.
6	Trace function	Set when a '3D' command is being processed. Reset when a new function begins.
7	Error display valid	Set when a valid error display is stored in control store. Reset when invalid.

GROUP 10-REGISTER 7		
BIT	NAME	DESCRIPTION
0	Olympus environment	Used by manufacturer.
1	Display flag	Set or reset to control source of dosplay bytes: 0 - From CILMSG 1 - From CILPARM
2	Oltlock	Set when inline control is executing diagnostic type commands (diagnostic load and diagnostic write).
3	Error display in progress	Set when an error display has been initiated by inline control. Reset when display is complete.
4	Command received from device	Set when a command is present from a device controller. Reset when the command has been recognized.
5	Last command from device	Set when a command is received from a device controller. Reset when a command is received from the 3880 MD.
6	Controller selection required	Set when it is determined that a device controller must be selected before an entry is made to an inline.
7	Offline diagnostic	Set when 3880 offlines are run. When set, inline control remains in control and does not return to the functional code.

EXTERNAL INDIRECT REGISTERS

The External Indirect Registers are summarized in the REF section of the MSM.

MAINTENANCE CONNECTION

The Maintenance Connection table traces the communication between 3880 microcode and the customer engineer. A description of this table is found in the PDA 6xx pages of this manual.

WORKING STORAGE DEFINITION

COMMUNICATIONS VECTOR TABLE (CVT)

The CVT is used to provide a run time link between microcode which is translated and linked separately from the functional code and the functional code.

HEX	DESCRIPTION
000	Address of the check one sense area.
001	Address of the normal sense area.
002	Undefined.
003	Address of the dump table.
004	Address of the stored channel switch value.
005 To 016	Undefined
017	Address of contingent connection ctl blk.
018 To 03F	Undefined

INLINE (DIAGNOSTIC) PARAMETER AREA

HEX	DESCRIPTION
000 to 007	Inline parameter area

INLINE (DIAGNOSTIC) MESSAGE AREA

HEX	DESCRIPTION
000 to 007	Inline message area

INLINE (DIAGNOSTIC) CONTROL STORAGE AREA	
HEX	DESCRIPTION
000	Byte 0 - Run options entered by CE Byte 1 - Load device busy count
001	Byte 0 - Control from inline to inline control Bit 0 - Loop in current overlay Bit 1 - No deselect to controller or drive Bit 2 - Single overlay load request Bit 3 - Test locator being loaded Bit 4 - Previous load was single overlay Bit 5 - Redisplay last display on break Bit 6 - Reserved Bit 7 - Previous load was single overlay Byte 1 - Reserved
002	Byte 0 - Current routine ID Byte 1 - Current routine overlay number
003	Byte 0 - Current overlay ID Byte 1 - Current overlay overlay number
004	Byte 0 - Controller and device address Byte 1 - Device type
005	Reserved
006 to 00D	Error bytes from controller
00E	Overlay loader input parameters Byte 0 - Access control byte Bit 0 - Reserved Bit 1 - Use functional or diagnostic bands at track 1 or 2 Bit 2 - Maintain diskette selection Bit 3 - Use inline area of control storage Bit 4 - Use functional overlay band Bit 5 - Use interval timer Bit 6 - Use special 3880 diagnostic band Bit 7 - Multitrack operation Byte 1 - Overlay number
00F	Requested control storage address
010	Overlay loader input parameters Byte 0 - Overlay ID requested Byte 1 - Retry count
011	Link return address
012	Overlay loader stored values Byte 0 - Return code on exit Byte 1 - Saved input IRG value
013	Display bytes
014 to 018	Reserved
019 to 020	Storage for known error stops

TRACE FUNCTION AREA	
HEX	DESCRIPTION
000	Byte 0 - Trace option Byte 1 - Trace level
001	Byte 0 - Trace device Byte 1 - Stop control
002	First pointer address
003	Second pointer address
004	Third pointer address
005	Byte 0 - Trace status X'80' - Trace inactive X'81' - Trace saved by address compare X'82' - Save forced from MD replacing previous trace saved by MD (if any) X'83' - Trace save occured but was destroyed X'84' - Trace active in trace-all mode X'85' - Trace active in single-device mode X'94' - Address compare save occured while trace active in trace-all mode X'95' - Address compare save occured while trace active in single-device mode Byte 1 - Reserved
006 to 011	Reserved
012	First symptom code
013	First symptom code mask
014	Second symptom code
015	Second symptom code mask
016	Third symptom code
017	Third symptom code mask

DISKETTE INFORMATION	
HEX	DESCRIPTION
000	Compaction token
001	Functional code track pointers Byte 0 - First functional track Byte 1 - Last functional track
002	Functional overlay track pointers Byte 0 - First functional overlay track Byte 1 - Last functional overlay track
003	Diagnostic overlay track pointers Byte 0 - First diagnostic overlay track Byte 1 - Last diagnostic overlay track
004	Diskette drive track control Byte 0 - Current track Byte 1 - Destination track
005 to 00B	Functional code part number and engineering change number
00C	3880 diagnostic track pointers Byte 0 - First 3880 diagnostic track Byte 1 - Last 3880 diagnostic track

ALTERNATE STORAGE DIRECTOR PATH TEST COMPLETION CODE	
HEX	DESCRIPTION
000	Byte 0 - Transmit condition codes Byte 1 - Receive condition codes
001 to 038	Reserved

LOAD DEVICE ERROR COUNTS & EBO	
HEX	DESCRIPTION
000	Byte 0 Bit 0 - SD to SD path failure Bit 1 - Reserved Bits 2-4 - Diskette drive seek errors Bits 5-7 - Diskette drive read errors Byte 1 - Other storage director's EBO code

COMMON FLAG STORAGE AREA	
HEX	DESCRIPTION
000	Common flags Bit 0 - Diagnostic load CCW OK Bit 1 - Allow MD display Bit 2 - Controller captured Bit 3 - Check 1 sense area has data Bit 4 - Diagnostic load, write, or sense in progress Bit 5 - Diagnostic write in progress Bit 6 - MD display pending Bit 7 - Forced logging mode on Bit 8 - Overlay load in progress Bit 9 - IML complete Bit 10 - No timeout Bit 11 - Diagnostic mode Bit 12 - Functional code overlayed Bit 13 - Fast control storage stored Bit 14 - Dump table valid Bit 15 - Trace pointer no good - state save
001	Common flags Bit 0 - Error receive sequence due Bit 1 - Error transmit sequence due Bit 2 - Delayed format message X'39' Bit 3 - State save sense byte setup Bits 4-5 - Reserved Bit 6 - Allow MD break Bit 7 - Waiting for data received Bits 8-9 - Reserved Bit 10 - Reset display owed Bit 11 - Schedule inline diagnostic handler Bit 12 - Reserved Bit 13 - Functional overlay TBON loaded Bit 14 - Diagnostic overlay TBON loaded Bit 15 - 3880 diagnostic
002 to 030	Reserved

INTERRUPT BYTES	
Because each storage director can support 32 devices, there are 32 areas in control storage with the following format:	
HEX	DESCRIPTION
000	Byte 0 - Contains the bit significant channel mask (BSCM) marks to indicate that channels are free (available) to use this device. Byte 1 - Contains BSCM marks to indicate what channels have reserved this device.
001	Byte 0 - Contains BSCM marks to indicate channels that have owed device end (ODE) from this device. Byte 1 - Contains BSCM marks to indicate channels that have a pack change (PCH) from this device.

DEVICE ERROR LOG MARK AND COUNT	
This area contains marks relating to usage counter overflows or error log modes. Each logical device has a two-byte error log block.	
HEX	DESCRIPTION
000	Byte 0 - Device error log mark Bit 0 - Seek usage counter overflow Bit 1 - Read usage counter overflow Bit 2 - Seek check error log mode Bit 3 - Data check with offset error log mode Bit 4 - Bypass unit check presentation Bits 5-7 - Reserved Byte 1 - Device error log count Bits 0-3 - Seek check error log count Bits 4-7 - Data check with offset error log count

ACTIVE DEVICE CONTROL BLOCK (DCB)	
HEX	DESCRIPTION
000	Current physical address
001	Byte 0 - Read marks (RWMS) register Byte 1 - File mask (FMKS) register
002	Old physical address
003	Defective fixed heads (DH0, DH1)
004 to 005	Read usage counter
006	Seek usage counter
007	CHIP Cell number for count field
008	Expected physical address
009	Cell number for key field
00A	Cell number for data field
00B	Format 8 counter
00C to 00D	Restart displacements
00E	Key or data length for usage counter
00F	Byte 0 - DPF flags Byte 1 - Reserved

SUPPRESSIBLE INTERRUPT BUFFERS	
Validation marks for the static interrupt fields. It indicates which bit significant channel information is valid.	
HEX	DESCRIPTION
000	Bit significant marks for channels

DISCONNECT CHAIN CONTROL/HOT MASK	
HEX	DESCRIPTION
000	String 0 Byte 0 - Disconnected command chain marks, bit significant by channel Byte 1 - Hot interrupt marks, bit significant by channel
001 to 003	Same as above for strings 1 through 3

PRIMED DEVICE END (PDE)	
HEX	DESCRIPTION
000	String 0 Byte 0 - Primed device end, bit significant by channel Byte 1 - Physical path map, bit significant by channel
001 to 003	Same as above for strings 1 through 3

COUNTER OVERFLOW	
HEX	DESCRIPTION
000	Counter overflow for strings 0 and 1
001	Counter overflow for strings 2 and 3

STATIC REQUEST IN	
HEX	DESCRIPTION
000	Work area
001	Static Request In

BIT SIGNIFICANT DEVICE ADDRESS (BSDA) AND BINARY STRING/SPINDLE PAIR ADDRESS (BNSA)	
HEX	DESCRIPTION
000	Byte 0 - BSDA of the selected device Byte 1 - Binary string/spindle pair address (right justified)

BIT SIGNIFICANT CHANNEL MASK (BSCM) AND UNIT ADDRESS	
HEX	DESCRIPTION
000	Byte 0 - BSCM of the selected channel Byte 1 - Unit address (CU/controller/device) in the channel format

CONTINGENT CONNECTION CONTROL BLOCK	
HEX	DESCRIPTION
000	Byte 0 - Device status (stacked/halted) Byte 1 - Binary unit address
001	Byte 0 Bit 0 - A device is selected Bits 1-7 - Reserved Byte 1 - Reserved

DYNAMIC PATH FEATURE (DPF) ID	
HEX	DESCRIPTION
000	Byte 0 - Validation flag For a basic machine, the combinations can be X'00', 'B0', '0B', or 'BB' For a DPF machine, the combinations can be X'00', 'D0', '0D', or 'DD' Byte 1 - Reserved
001	Byte 0 - Controller 0 identification Bit 0 - Validation Bit 1 - Array initialization complete Bit 2 - SD connected to controller A2 Bit 3 - DPF machine Bits 4-7 - Reserved Byte 1 - Controller 1 identification Bit 0 - Validation Bit 1 - Array initialization complete Bit 2 - SD connected to controller A2 Bit 3 - DPF machine Bits 4-7 - Reserved

State-Save Tables for Model 23

CHANNEL MODE/PATH GROUP ID VALIDATION	
Bit significant channel marks for channel mode of operation and path group ID validation as a result of Set Path Group ID command execution. Reset by system reset.	
HEX	DESCRIPTION
000	Byte 0 - Bit significant channel mode (should be zero for System 370) Byte 1 - Bit significant channel path group ID validation mark

ERROR LOG BUFFER CONTROL	
HEX	DESCRIPTION
000	Byte 0 - Error log type Bit 0 - Seek check Bit 1 - Data check with offset Bit 2 - Data check Bits 3-7 - Reserved Byte 1 - Unit address with which error log buffer is associated

CONTROLLER IDENTIFICATION	
HEX	DESCRIPTION
000	Byte 0 - Controller 0 identification Byte 1 - Controller 1 identification

DRIVE SELECTED MARK	
This mark is set whenever device selection is attempted, whether selection is successful or not. It is reset on device deselection. The purpose of the mark is to present Fmt 29 following a selective reset. This mark is not used to determine the selected state of a device.	
HEX	DESCRIPTION
000	Byte 0 Bit 0 - Drive selection attempted Bits 1-7 - Reserved Byte 1 - Reserved

CONTROLLER ERROR LOG MARK AND COUNT	
This area contains marks relating to error log mode. Each controller has a 2-byte wide error log block.	
HEX	DESCRIPTION
000	Byte 0 - Controller error log mark Bit 0 - Data check error log mode Bits 1-7 - Reserved Byte 1 - Data check error log count

UNSUPPRESSIBLE OR SUPPRESSIBLE INTERRUPT BUFFERS	
This area contains bit significant channel mask marks to indicate channels that a possible suppressible or unsuppressible Request-in may be raised if this device responds with an interrupt while being polled. There is one area per device.	
HEX	DESCRIPTION
000	Byte 0 - Possible suppressible Request-in Byte 1 - Possible unsuppressible Request-in

DEVICE STATUS
During a DPS device selection, will return its status. That status (path busy, owed device end, or pack change is stored in this area.

SENSE BYTES
Contains 24 bytes of sense information for Sense, Reserve, Release, or Unconditional Reserve CCWs.

BUFFERED LOG
Contains 24 bytes of error log information.

FMT 3 - SENSE AREA
Contains 24 bytes of format 3 sense information.

OVERRUN COUNTERS	
Contains counters for command overrun and data overrun for channel x, where x may = A through H.	
HEX	DESCRIPTION
000	Byte 0 - Command overrun counter Byte 1 - Data overrun counter

RETRY MARKS	
HEX	DESCRIPTION
000	Byte 0 - Number of data checks in count or HA field Byte 1 - Number of uncorrectable data check retries in key field
001	Byte 0 - Number of uncorrectable data check retries in data field Byte 1 - Number of command overrun retries
002	Byte 0 - Number of data overrun retries Byte 1 - Number of seek retries
003	Byte 0 - Format/message of prior nested retry Byte 1 - CCW code of the retrying CCW
004	Byte 0 - Sense control block (SCB) 0 = sense pointer Byte 1 - SCB 2 = SCB flags
005	Byte 0 - SCB 3 = Sense code Byte 1 - SCB 4 = Format/message for sense byte 7
006	Byte 0 - SCB 1 = Microcode detected error retry qualifier
007	Byte 0 - Retry flag 1 = internal exception processor flag Bit 0 - Retry status presented Bit 1 - Wait for interrupt Bit 2 - Microcode Set Sector Bit 3 - Interrupt in file Bit 4 - Device End status not presented Bit 5 - Device command overrun Bit 6 - Retry status rejected Bit 7 - Correct key field, or if 0 correct count, HA field Byte 1 - Retry flag 2 = internal exception processor log Bit 0 - HA oriented Bit 1 - Reserved Bit 2 - Offset forward Bit 3 - Reserved Bit 4 - Format write Bit 5 - Correctable data check retry Bit 6 - Command overrun retry Bit 7 - Reserved

BUSY THRESHOLD
This area contains a count of the number of times a SIO has been issued against a busy device. The threshold value is used to determine whether channel blocking will inhibit channel initiated selection.

INLINE COUNTERS	
HEX	DESCRIPTION
000	Byte 0 - This counter tallies the number of workless loops through the idle loop. When the counter overflows, the inline diagnostics are allowed.

RETRY TRACK ORIENTATION	
HEX	DESCRIPTION
000	Byte 0 - Contains track orientation upon entry to retry Byte 1 Bit 0 - Contains after retry field mark. This mark is set by read/write when it is determined that the field being processed is after the retry field. Bit 1 - Contains no sync or data after Read Multiple CKD.

CE ADDRESS	
HEX	DESCRIPTION
000	Byte 0 - Initialized to X'FF' on IML. Controller address is set by Idle on CE poll. Updated to CE controller and device address after CE has entered a diagnostic routine (X'31') Byte 1 - Contains CE marks Bit 7 - CE alert from controller

PATH GROUP IDENTIFICATION	
Contains path group identification for channel x, where x may be A through H.	
HEX	DESCRIPTION
000	Byte 0 - Path group identification control byte Byte 1 - Path group identification
001 to 005	Path group identification

DEVICE CONTROL BLOCK (DCB)
This area contains the permanent DCB for each device. Each block of 16 bytes is moved from this permanent location to the active DCB area on SIO, TIO, or a reconnection after initial presentation. See active DCB description for the details of how this storage area is used.

SEEK CHECK/DATA CHECK WITH OFFSET COUNT	
Each logical device has two bytes	
HEX	DESCRIPTION
000	Byte 0 - Seek check count Byte 1 - Data check with offset count

SEEK USAGE DENOMINATOR
This area contains the number of motion seeks. Each logical device has two bytes.

DATA CHECK NUMER/DENOM	
Each logical device has two bytes	
HEX	DESCRIPTION
000	Byte 0 - Data check count used as a counter 1 Byte 1 - Data check count used as a counter 2

DATA USAGE DENOMINATOR	
Each logical device has four bytes in this table.	
HEX	DESCRIPTION
000 to 001	Bytes-read counter

CHANNEL SWITCHES	
HEX	DESCRIPTION
000	Channel A Byte 0 - SD address Byte 1 - Channel switch setting
000 to 007	Same as above for channels B through H
008 to 018	Format 7 sense bytes 8 through 23

SYSTEM RESET INCOMPLETE
During a system reset, the DPS array is updated in the controller. This mark is set if an end op is received from the controller during this update.

WAIT LOOP ERROR
When the storage director is in the wait loop and a DPS alert is received from the alternate controller, the storage director must read the primary controller's array. This mark is set if an end op is received during this read.

FENCING INFORMATION	
HEX	DESCRIPTION
000	Byte 0 - Controller 0 fence mark Byte 1 - Controller 1 fence mark

DEVICE OPERATION LIST (OP LIST)
This list buffers device operations during asynchronous transfers when Chip is ahead of Dip. This Op list, the Op list head pointer, and the Op list tail pointer form a first-in first-out (FIFO) queue. Chip adds operations to the list with the tail pointer. Dip performs operations and removes them with the head pointer.

PERMANENT DEVICE CONTROL BLOCK EXTENSIONS
This area contains the permanent DCB extensions for each device. Each block of 16 bytes is moved from this permanent location to the active DCB extension area on SIO, TIO, or a reconnection after initial presentation. The bit definitions for this area are the same as for 'Active DCB Extension'.

PERMANENT DEFECTIVE PHYSICAL ADDRESSES
Contains permanent defective addresses for all 32 devices. Valid only on alternate track. They are stored here at DCC time and recovered at reconnection time.

CHIP CONTROL STORE VARIABLES	
HEX	DESCRIPTION
000	Cell address of the current record's count field. It is saved by Chip during read operations on a slow channel, and may be used for retry reorientation during error recovery or retry.
001	During slow channel format write, contains the device operation. During the Read Multiple CKD command, contains the cumulative transfer byte count.
002	First-record indicator
003	Control block for unusual situations encountered by Chip.
004 to 008	Register save area

DIP CONTROL STORE VARIABLES	
HEX	DESCRIPTION
000	Control block for unusual situations encountered by Dip.
001	DORF save area
002	Cell number spaced for reorient

ACTIVE DEVICE CONTROL BLOCK EXTENSION	
HEX	DESCRIPTION
000	Record size
001	Beginning of extent
002	Ending of extent
003	Byte 0 - Active intent count Byte 1 - Remaining intent count
004	Find argument (CC)
005	Find argument (HH), saved KL
006	Byte 0 - Find argument (R) Byte 1 - Flags Bit 0 - Find required Bit 1 - Internal find Bits 2-3 - Intent descriptor: '00' - Read '01' - Update write '10' - Format write '11' - Track write Bit 4 - Locate allowed Bit 5 - Find HA Bit 6 - Index passed Bit 7 - Find previous
007	Byte 0 - Spaced sector count Byte 1 - Sector number
008	Byte 0 - Model 23 flags Bit 0 - Cylinder valid Bit 1 - Bypass cache Bit 2 - Inhibit cache loading Bit 3 - Sequential access Bit 4 - Write DASD only Bits 5-7 - Reserved Byte 1 - Reserved

State-Save Tables for Model 23 PDA 570

REGISTER SAVE AREA WHEN DASD DATA TRANSFER MODE IS TERMINATED	
When control is transferred from DASD data transfer mode to non-DASD-data-transfer mode, certain essential non-DASD-data-transfer registers are stored here.	
HEX	DESCRIPTION
000	Byte 0 - Read/write marks Byte 1 - Retry flags
001	Byte 0 - Initial selection detect marks Byte 1 - Initial selection select marks
002	Byte 0 - Bit significant device address Byte 1 - Binary string address
003	Byte 0 - Bit significant channel mask Byte 1 - Basic/DPS machine ID
004	Byte 0 - Logical device address Byte 1 - Idle status information byte

CHIP PARAMETER AREA
Contains parameters for Define Extent, Locate Record, Seek, Set Sector, and Read Sector commands.

UNUSUAL SITUATION WORK AREA	
HEX	DESCRIPTION
000	Byte 0 - Points to the sense information table Byte 1 - Points to the beginning position in
001	Points to the present position in the current path through the recovery pointer table.
002	Unusual situation indicators and count Byte 0 Bit 0 - Channel is ahead of device Bit 1 - Channel is at the same point as the device Bit 2 - Channel is behind device Bit 3 - Device record is HA Bit 4 - Device record is RO Bit 5 - Reconnection at index Bits 6-7 - Field ID '00' - Device field is count '10' - Device field is key '11' - Device field is data Byte 1 Bit 0 - Read operation Bit 1 - Find indicator Bit 2 - Reserved Bits 3-7 - Error code for format 2F condition
003	Unusual situation relinquish value - indicates the point when Chip must be given control to avoid being passed by Dip.
004	Unusual situation internal error code
005 to 008	Unusual situation internal retry control Byte 0 Bit 0 - Fixed head sparing indicator Bit 1 - Defective alternate indicator Bit 2 - Cylinder crossing indicator Bit 3 - Command overrun indicator Bits 4-7 - Indicates which of the next seven bytes points to an internal error. Bytes 1-7 - Point to internal errors.
009	Head offset parameters
00A	Length of field with error
00B	Reconnection cell number
00C	Adjusted reconnection cell number - used for channel reconnection on a slow channel when lead is required.
00D to 00D	Return address and IRG - used for the return to Chip after a Dip check 2 condition, and within the error recovery block during channel overrun recovery.

UNUSUAL SITUATION REGISTER SAVE AREA	
After an unusual situation has been detected in DASD data transfer mode, error analysis saves these internal registers. The information in parenthesis below indicates the register (R) and group (G).	
HEX	DESCRIPTION
000	(R6G8) - Expected DBH (R7G8) - Expected DBL
001	(R4G9) - Channel beginning of buffer (R5G9) - Buffer orientation record
002	(R6G9) - Work register (R7G9) - Op list pointer
003	(R4G10) - Track orientation register (R5G10) - Current intent count
004	(R6G10) - File mask (R5G10) - Channel command (CCW)
005	(R4G11) - Device beginning of buffer (R5G11) - Op list head pointer
006	(R6G11) - Dip flags (R7G11) - Total intent count
007	(PR0G13) - Segment field length (bytes)
008	(PR2G13) - Segment field length (cell no.)
009	(PR4G13) - Cell number
00A	(PR6G13) - Dip field length
00B	(R0G6) - Find argument (R) (R1G6) - Key length
00C	(PR2G6) - Data length
00D	(PR4G6) - Find argument (CC)
00E	(PR6G6) - Find argument (HH)
00F	(PR0G7) - Channel orientation record and field
010	(R2G7) - Dip state (R3G7) - Bottom of buffer pointer
011	(PR4G7) - Next operation/field
012	(PR6G7) - Device orientation record and field

UNUSUAL SITUATION WORK AREA AND OP LIST
Contains a series of modified DCC commands, follow-by Dip's interrupt address and IRG. The DCC commands are used to reposition Dip on reconnection.

CACHE CONTROL BLOCK	
Contains data required for caching that must be preserved across device disconnections. Valid only for the active device.	
HEX	DESCRIPTION
	Beginning of Active CCB
000	Byte 0 - Mode and current track activity Bit 0 - Cache mode Bit 1 - DASD mode Bit 2 - Internal mode Bit 3 - Save mode for internal promotion Bit 4 - Cache operation required Bit 5 - Track location indicator 0 - Miss 1 - Hit Bit 6 - Allow Write flag Bit 7 - Final Device End presented Byte 1 - Track activity Bit 0 - Search/Read activity Bit 1 - Update Write activity Bit 2 - Format Write activity Bit 3 - Front promotion indicator Bit 4 - Reserved Bit 5 - Find index Bit 6 - Branching promotion indicator Bit 7 - Bypass performance counter update
001	Byte 0 - Flag byte Bit 0 - Set Sector Front Promotion Bits 0-1 - Reserved Bit 2 - MRU finished Bits 3-7 - Reserved Byte 1 - Reserved
002 to 003	Starting SSAR for branching (4 bytes)
004	Write activity for cylinder
005	Process write activity return address
006	Promotion cleanup return address
007	Internal promotion return address
008	Cache-to-channel bytes-transferred counter
009	Bytes 0,1 - Contains a pre-allocated block slot index for CCSABS
	Active Directory Entry Information
00A	Active entry index
00B	Active entry physical address in packed form
	Active Entry Device and Flags
00C	Byte 0 - Device address Byte 1 - Directory flags Bit 0 - Entry busy Bit 1 - Sequential Bit 2 - Valid Bit 3 - Reserved Bit 4 - SDI (bit 7) Bit 5 - Reserved Bits 6, 7 - List offset '00' - MRU list '01' - Reserved '10' - Defective list '11' - Structures slot
00D to 00E	Active entry slot (4 bytes)
	Beginning of the slot header information
00F to 010	Home address track pointer (4 bytes)
011 to 012	Break track pointer (4 bytes)
013 to 014	Index track pointer (4 bytes)
015	First cell number in cache
016	Byte 0 - Slot header flags Bit 0 - Type of promotion 0 - Branching promotion 1 - Internal promotion Bit 1 - Full track image Bit 2 - Partial track image Bit 3 - Split track image Bit 4 - Sequential promotion Bit 5 - Internal front promotion Bits 6-7 - Reserved Byte 1 - Reserved
017	Reserved

EXTENDED CACHE CONTROL BLOCK	
Contains flags for disconnection and reconnection. This data is not transferred to cache during device orientation.	
HEX	DESCRIPTION
000	Byte 0 - Flags Bit 0 - Subsystem mode transition occurred Bit 1 - Unit Check on reconnection Bit 2 - Post final device end reconnection Bit 3 - Standalone CCW Bits 4-7 - Reserved Byte 1 - Reserved

PORT	
This is used to pass information between components that cannot be passed in internal registers. This structure is not preserved across device reconnections. Common to all devices.	
HEX	DESCRIPTION
000	Byte 0 - Port flags Bit 0 - Concurrent operation Bit 1 - Check 2 Bit 2 - Reserved Bit 3 - Error occurred on field transferred to channel Bit 4 - Error occurred on field transferred to cache Bit 5 - CCB active Bit 6 - Perform end of chain cleanup Bit 7 - Reserved Byte 1 - Return code that cannot be passed in register 15
001	Temporary cache usage counter
002	Device of Pack Change Interrupt
003	Sense build return to caching address
004	Reason code for F4 and F9 hardware errors

SUBSYSTEM MODE BLOCK	
Contains indicators for the mode of this SD, the reason for non-caching mode, pending SMT dispatch invocation, and the function to be performed via the SMT Dispatcher block.	
HEX	DESCRIPTION
000	Byte 0 - SD mode Bit 0 - Caching mode Bits 1-7 - Reserved Byte 1 - Termination/reinitialization reason (byte 8 of F4 or F9 sense) X'00' - No message X'01' - Entering limited caching state X'02' - Subsystem storage port failure X'03' - Subsystem storage general failure X'04' - Caching status miscompare detected X'05' - Microcode logic error X'06' - Other SD cannot access cache X'07' - Reset occurred while resets were inhibited X'08' - Subsystem storage mode switch active X'09' - Test and set appears locked to other SD for limited caching X'0A' - Storage director equipment check X'0D' - Diagnostic bit active X'FF' - Non-caching due to command (no error)
001	Byte 0 - SMT agenda Bit 0 - SMT invocation requested Bit 1 - Terminate caching Bit 2 - Reinitialize cache Bit 3 - Recover from resets Bit 4 - Resolve mode miscompare Bits 5-7 - Reserved Byte 1 Bit 0 - IML initiate caching Bit 1 - Complete SSM command Bit 2 - Initialize left DPS Bit 3 - Initialize right DPS Bit 4 - Check for message in left DPS Bit 5 - Check for message in right DPS Bits 6-7 - Reserved
002	Byte 0 - Reserved Byte 1 - Byte 0 of directory address

RESET CONTROL BLOCK	
HEX	DESCRIPTION
000	Byte 0 - Reset flag X'D7' - resets inhibited X'D8' - resets allowed Byte 1 - Undefined
001	Return address save

DASD SUPPORT SERVICES COMPONENT SAVE AREA	
HEX	DESCRIPTION
000	Saved return address
001	DPS alert counter

RW COMPONENT SAVE AREA	
HEX	DESCRIPTION
000	Saved device redundancy code
001	Saved cell number
002	Saved device orientation
003	Saved return address
004	Saved return address (SC040)
005	Saved return address (M17510)
006	Write activity vector
007 to 016	Bit significant cylinder vector mask for heads 0 through 15

DASD EMULATION COMPONENT SAVE AREA	
HEX	DESCRIPTION
000 to 001	Current record pointer
002 to 003	Saved current record pointer
004	Saved value for Read Sector CCW
005	Retry counter and flags
006	Saved return address for orient to record
007	Saved return address track switch/transfer field
008 to 00B	Saved return address and IRG for concurrent operations
00C to 00D	Subsystem storage address for cache dump parameter

CACHE MANAGER COMPONENT SAVE AREA	
HEX	DESCRIPTION
000	Saved internal return address
001	Saved SIT entry offset
002	Saved SIT entry subsystem storage address
003	Subsystem storage access counter
004 to 007	Work area
008	Count of track slots used by structures
009 to 00A	Saved index for lost slots
00B	Saved busy mask
00C	Saved external return address
00D	Subsystem storage address of structures base
00E	MRU anchor pointer
00F	Reserved
010	Defective anchor pointer
011	List counters pointer
012	Diagnostic area 1 pointer
013	CCB base address
014	Directory base address
015	Directory length in subsystem storage words
016	SIT base address
017	SIT length in subsystem storage words
018	Cache slot base address
019	Subsystem storage size

SENSE BUILD FLAGS	
HEX	DESCRIPTION
000 to 01F	Sense offload flags for devices 00 through 31. The two bytes for each device contain: Bit 0 - Unit check any Start I/O Bit 1 - Valid sense Bit 2 - Unrecovered error while disconnected from channel Bits 3-15 - Reserved
020	Start I/O counter
021	Sense offload summary flags Bit 0 - Unit check any SIO present in device buffers Bit 1 - Unit check any SIO present in non-device buffers Bit 2 - Unit check any SIO present in 16K SIO buffer Bits 3-15 - Reserved
022	Retry flags Bit 0 - CHOPS component retry bit Bit 1 - SSA component retry bit Bit 2 - SMT component retry bit Bit 3 - USURP component retry bit Bit 4 - Additional SMT retry bit Bit 5 - Additional SMT retry bit Bits 6-7 Reserved Bits 8-15 - Sense buffer indicator code X'00' - Use appropriate device buffer X'01' - Use non-device buffer X'02' - Use 16K SIO buffer X'03'-'FF' - Reserved

SHARED STRUCTURES ACCESS COMPONENT SAVE AREA	
HEX	DESCRIPTION
000	Saved return address - SSA
001	Saved return address - CS to SS data transfer
002	Saved address of control storage
003 to 007	Save area for registers PR4 through PR12
008	Save area for register PR14

SOFT ERROR LOGGING COMPONENT SAVE AREA	
HEX	DESCRIPTION
000	Saved return address
001	Soft error counter
002	Cache usage counter

SUBSYSTEM STATUS BUFFER	
This buffer is used to build the output of the Sense Subsystem Status command. A subset of this table is used to pass the configured cache size counters between components.	
HEX	DESCRIPTION
000	Byte 0 - SD identification (One's complement of the SDI register) Byte 1 - Device identification
001	Reserved
002	Byte 0 - Overall caching status Bit 0 - Command non-caching Bit 1 - Error non-caching Bit 2 - Limited caching Bit 3 - SS mode switch active Bit 4 - DASD controller 0 available Bit 5 - DASD controller 1 available Bits 6-7 - Reserved Byte 1 - Reserved
003	Byte 0 - Left device caching status Bit 0 - Device 0 caching activated . . Bit 7 - Device 7 caching activated Byte 1 Bit 0 - Device 8 caching activated . . Bit 7 - Device 15 caching activated
004	Byte 0 - Right device caching status Bit 0 - Device 16 caching activated . . Bit 7 - Device 23 caching activated Byte 1 Bit 0 - Device 24 caching activated . . Bit 7 - Device 31 caching activated
005 to 006	Configured cache size in bytes
007 to 008	Cache bytes in track slots on LRU list
009 to 00A	Reserved
00B to 00C	Cache bytes in track slots on defective list
00D to 013	Reserved

RAS INTERFACE TABLE	
HEX	DESCRIPTION
000	Control storage address of base sense regs
001	Control storage address of SD/SS available tags
002	Subsystem storage address of list counters
003	Subsystem storage addr of diagnostic area 1
004	Subsystem storage addr of diagnostic area 2
005	Subsystem storage addr of diagnostic area 3
006	Subsystem storage addr of diagnostic area 4
00C to 00D	Reserved
00E	Control storage address of caching sense buffers

SUBSYSTEM MODE TRANSITION (SMT) CONTROL STORAGE DECLARATIONS	
HEX	DESCRIPTION
000	Byte 0 - RAS subsystem storage available flags Bit 0 - SD2 indicator Bit 1 - Subsystem storage available Bits 2-7 - Reserved Byte 1 Bit 0 - Storage unavailable due to command Bits 1-7 - Reserved
001	Byte 0 - DPS status flags Bit 0 - Left DPS inoperative Bit 1 - No left DPS Bit 2 - Right DPS inoperative Bit 3 - No right DPS Bits 4-7 - Reserved Byte 1 - Reserved
002	Byte 0 - LDAS save area Byte 1 - Reserved
003	Byte 0 - DPS access retry flags Bit 0 - Retry in progress Bit 1 - Suppress DPS retry Bits 2-7 - Reserved Byte 1 - Reserved
004	Byte 0 - SMT environment flags Bit 0 - Retry in progress Bit 1 - Suppress DPS retry Bits 2-7 - Reserved Byte 1 - SMT environment code X'00' - No environment X'01' - Dispatcher (when no function dispatched) X'02' - SSM command (X'87') X'03' - SSS command (X'54') X'04' - IML X'05' - Reset X'06' - Completing SSM command X'07' - Error termination X'08' - Reinitialize cache X'09' - Mode miscompare X'0A' - Initialize DPS X'0B' - Check for message
005	Byte 0 - SMT lock state flags Bit 0 - Left lock busy or state unknown Bit 1 - Left lock DPS check Bit 2 - Right lock busy or state unknown Bit 3 - Right lock DPS check Bits 4-7 - Reserved Byte 1 - Reserved
006	Byte 0 - SSM command arguments Bits 0-2 - Operation 000 - No operation 001 - Activate device caching 010 - Deactivate device caching 011 - Make SS available 100 - Make SS unavailable Bits 3-7 - Reserved Byte 1 - Logical address of device to which command was issued
007 to 040	Temporary return address, message, and general purpose save areas

CORS REGISTER	
HEX	DESCRIPTION
000	Byte 0 - Current cache orientation Bit 0 - Index orientation Bit 1 - Home address orientation Bit 2 - Pre-count orientation Bit 3 - Count orientation Bit 4 - Key orientation Bit 5 - Data orientation Bit 6 - Index passed Bit 7 - Sector processing Byte 1 - Reserved

ADT COUNT AND HA AREA	
HEX	DESCRIPTION
000	Byte 0 - Record count field
001	Reserved
002 to 008	Skip defects
009	Cell number
00A	Two high-order bytes of physical address
00B	Byte 0 - Low-order byte of physical address Byte 1 - Flags
00C	Cylinder
00D	Head
00E	Byte 0 - Record Byte 1 - Key length
00F	Data length

ADT FIXED CACHE MANAGER COMPONENT AREA	
HEX	DESCRIPTION
000 to 007	CMC 16-byte fixed directory area

ADT FIXED SUBSYSTEM STORAGE ACCESS AREA	
HEX	DESCRIPTION
000 to 007	SSA 16-byte fixed area

ADT VARIABLE SUBSYSTEM STORAGE ACCESS AREA	
HEX	DESCRIPTION
000 to 007	First 16 bytes of SSA variable length buffer

Unusual Operating Conditions

Status Pending Hang

There are four conditions that turn on the Status Pending indicator:

1. Contingent Connection
2. Stacked Status
3. Retry Reconnection
4. Internal Reconnect

Each of these states represents unfinished work between a specific channel and a specific device. The storage director does not allow selection unless the specified channel or device connection is requested. Any other selected attempt is defined as a control unit busy by the storage director. If the address requested by the channel on an SIO operation does not match the address in the contingent connection control block (CCCB), the storage director responds with control unit busy. The CCCB is part of the state save tables.

A CONTINGENT CONNECTION HANG ON THE 3880 IS SIMILAR TO A HANG AT IAR 0080 ON THE 3830-2.

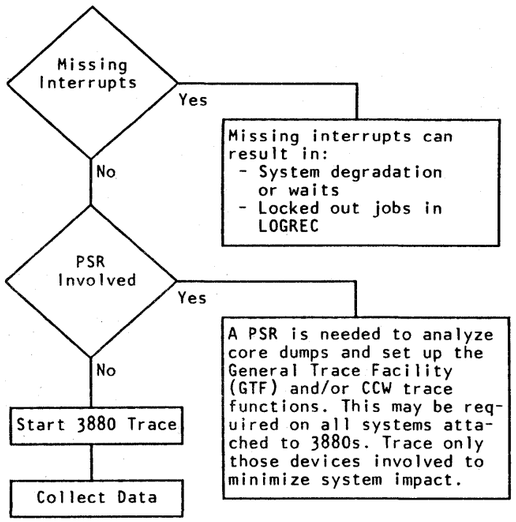
If a retry connection is attempted and an interrupt is pending in the device, the microcode polls for device attention before activating Request In. During internal reconnect, all channel interaction is bypassed.

Unusual Operating Conditions PDA 600

Missing Interrupts

Note: During a contingent connection, control unit end (CUE) is associated with the specific address for which the contingent connection is being maintained.

When presented via polling, the address associated with CUE is always the lowest non-busy device address within the range of addresses recognized by the storage director, whether or not the device exists.



1. Attach the MD to the 3880.
2. Select support mode. (Enter S when the maintenance option menu appears.)
3. Trace only the single device missing the interrupt (if known). If unknown or several devices are missing interrupts, trace all devices.
4. Select trace option 2 (no save events). Trace is now in effect.
5. It is now necessary to try to save trace data when the missing interrupt occurs. If all devices are traced, dynamic trace data may be overlaid by other devices. If tracing one device, trace data is usually valid. To force a save of trace data (dynamic trace table entries and state save table), use MD trace option 5. Option 5 forces a check one error in the 3880. An interface control check occurs and a selective reset is issued to the 3880.
6. Stop the GTF trace. It may also be necessary to get a system core dump.
7. Have your program support and/or the customer analyze the core dumps. Print the GTF trace for the time period of the missing interrupt.
8. Print the 3880 internal trace using OLT T3880D.
9. Dump the trace to the MD in case it is needed for remote analysis.
10. Use all available documentation to determine the source of the problem. The source may be:

    a. Software

    GTF trace and 3880 internal trace usually show the normal ending interrupt. The software receives the interrupt but loses it in the microcode.

    b. Microcode

    GTF shows the missing device end. The 3880 internal trace probably also shows the missing device end.

    c. Hardware

    1) Lost at channel or system level

    GTF shows the device end missing, 3880 trace shows the normal ending sequence. CIM (channel interface monitor) may be useful to trap this type failure (trace channel interface).

    2) Lost at device

    GTF and 3880 internal trace shows the missing device end interrupt. The EDI bit is on for the device in the interrupt byte. CIM may be used to trap this failure (trace control interface).

    3) Lost at control unit

    An open Request In line at the control unit, the interface cable, or the channel results in missing interrupts. This can affect several control units. Scope the Request In line at the failing control unit. Request In line should not be active for extended periods of time.

Unusual Operation Conditions (Cont.) PDA 605

Missing Interrupts (Continued)

The following figures show a DE missing after busy condition to address 50 [1], string 2 device 0 on channel interface B. Seek command (07) [2] receives status of 10 [3] (busy). Entry 503 (no DE) was presented when the device is not busy. This failure may be a hardware failure at the string switch level, microcode in the 3880, or a Reserve on the other side of the string switch left outstanding.

```
                    DYNAMIC  TRACE  TABLE  ENTRIES

ENTRY    CHAN     ADDR      CMND      STATUS      ID          V1     V2     ENTRY

474                         31                    COMMAND                   474
475                         31                    COMMAND                   475
476                         06                    COMMAND                   476
477                                   0C          ENDING                    477
478                                               B31M101                   478
479                                               B07M001                   479
480                                               B07M203                   480
481      B        50                              CHN  INIT                 481
490                                               B13M206                   490
491                         31                    COMMAND                   491
492                         31                    COMMAND                   492
493                         31                    COMMAND                   493
494                         31                    COMMAND                   494
495                         06                    COMMAND                   495
496                                   0C          ENDING                    496
497                                               B31M101                   497
498                                               B07M001                   498
499                                               B07M203                   499
500      B   [1]  50                              CHN  INIT                 500
501                                               B20M005                   501
502              [2]  07                          COMMAND                   502
503                       [3]  10                 ENDING                    503
504                                               B16M101                   504
505                                               B07M001                   505
506                                               B07M203                   506
507      B        50                              CHN  INIT                 507
508                                               B22M107                   508
509                                   00          ENDING                    509
510                                               B31M101                   510
511                                               B07M001                   511
512                                               B04M100                   512
                    END OF DYNAMIC TRACE

                    Address 50 = 0 1 0 1  0 0 0 0
                                                 Device 0
                                                 Controller (string) 2
                                                 Channel B
```

Figure 1. Dynamic Trace Table Sample

Storage Director Busy Hang

Only the process lamp is on. The possible causes are:

- High channel activity or software loop
- Microcode loop with timer disabled
- Repetitive interrupts from a device that cannot be reset.

High Channel Activity or Software Loop

1. Determine if any interface is selected by scoping the +CIF x Selected line. Refer to Status Pending Hang (on PDA 600) for a chart of scope points.
2. A selected interface can aid in determining the system and/or the channel that may be the source of the problem.
3. A 3880 internal trace can be helpful to determine the interface and/or command, and so on.

Microcode Loop With Timer Disabled

1. Scope line 01A-R2S12 (+Timer Enabled) at the suspected failing storage director. If it is disabled, the 3880 may be in a microcode loop.
2. Connect the MD. Select the support mode by entering an S when the maintenance option menu appears.
3. Select Option 5 (manual control).
4. Enter R1 to stop the clock. The IAR address is displayed (A = xxxx). There may be interface control checks at this time on any of the attached systems.
5. Press the Enter key to advance IAR (single cycle). Record the IAR addresses.
6. Enter R to restart the clock. Call the next level of support with a list of addresses recorded.

Repetitive Interrupts From Device

1. Power off the attached strings one at a time to isolate the failure.
2. A 3880 internal trace may help pinpoint the failing device. Figure 1 shows an example of the Disconnect Command Chain/Hot Interrupt table.

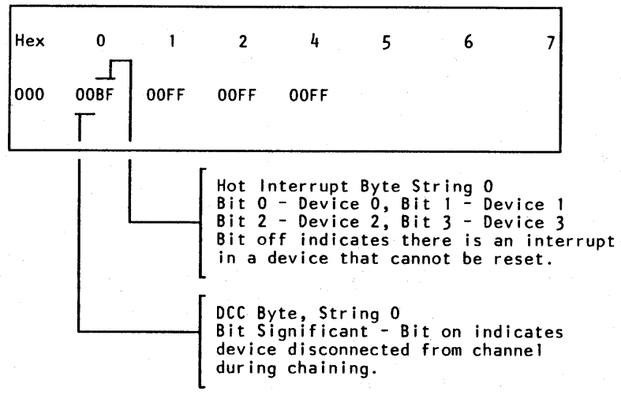


Figure 1. Save Table Hot Interrupt Example

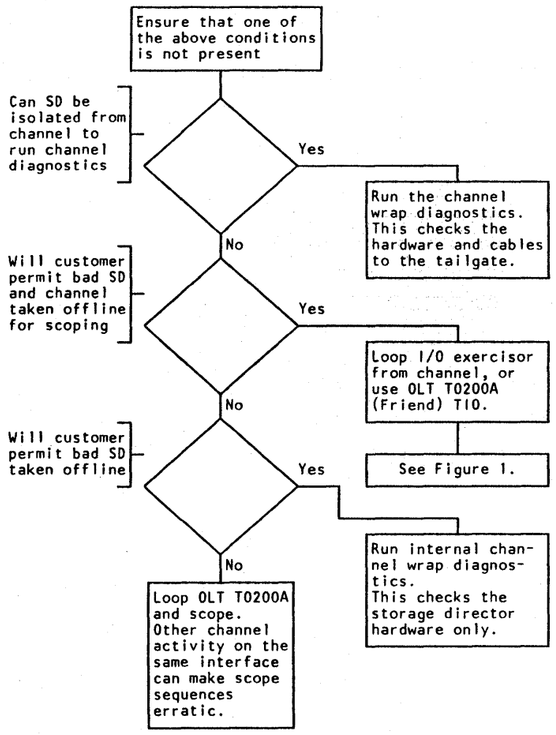
Condition Code 3

1. The control unit is not responding to channel selection. Possible causes are:

   a. The control unit is powered off.
   b. The interface is disabled.
   c. The wrong address is set in the address switches on the CIF card.
   d. The interface cabling is incorrect.
   e. The control unit or channel has a hardware failure.

2. The controller does not respond to control unit selection. Possible causes are:

   a. The controller is powered off.
   b. The interface is disabled.
   c. The address is plugged wrong on the controller address cards.
   d. The interface cabling is incorrect.
   e. The control unit or channel has a hardware failure.



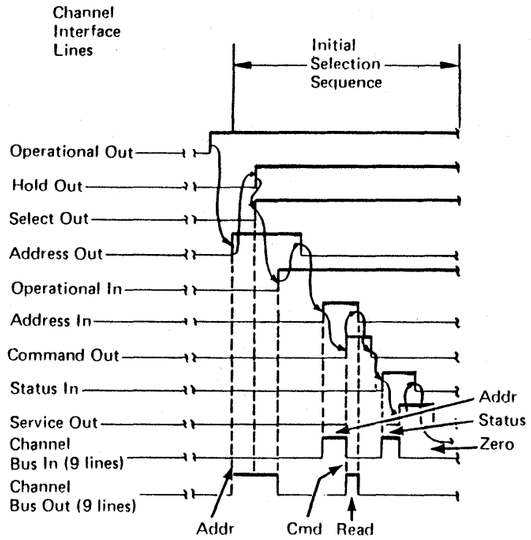


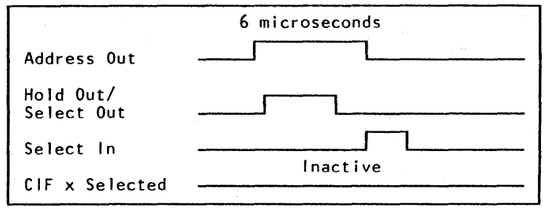
Figure 1. Correct Initial Selection Sequence for a Read

Note: See figures 2 and 3 for sample waveforms.

1. Sync on Address Out line at the failing storage director.
2. Scope the CIF x Selected line. See Status Pending Hang on PDA 600 for scope points.
3. If the CIF x Selected line is active, the channel-to-storage director path is probably correct and the problem is in the storage director-to-controller path. Check this path by running diagnostics between the failing controller and storage director.

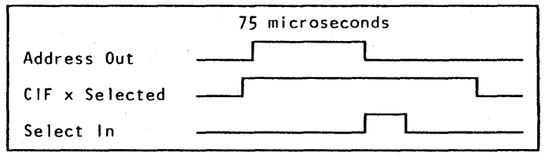
   Note: Process lamp is on if the storage director is being selected.

4. If the CIF x Selected line is not active, the storage director is not being selected by the channel. Ensure that the correct address is on Channel Bus Out at Address Out time and that it has the correct parity. Ensure that the Select Out and Hold Out lines become active just after the Address Out line becomes active. Be aware of the proper interface levels while scoping (approximately 0 to +3.5 Vdc).



This sequence shows a typical initial selection sequence which resulted in Condition Code 3, storage director not selected.

Figure 2. Storage Director Not Selected

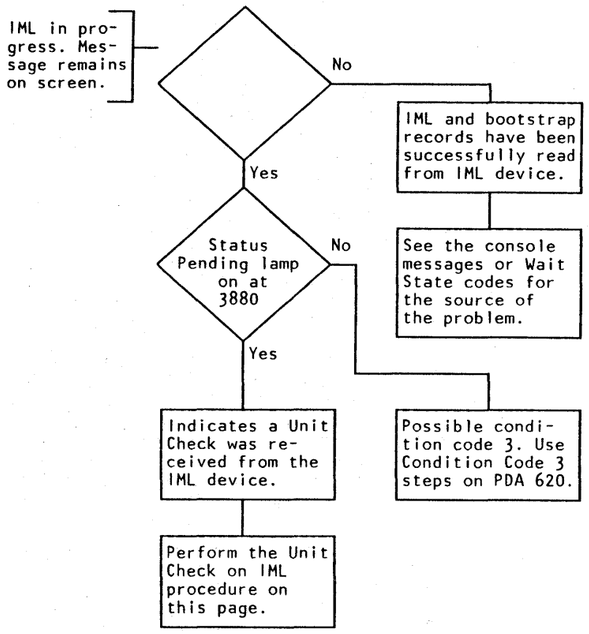


This sequence shows a typical initial selection sequence where the storage director was selected but was not able to select the controller. This causes a Condition Code 3.

Figure 3. Storage Director Selected

IML Failure

Use the following information to help isolate suspected IML failures.



Unit Check On IML

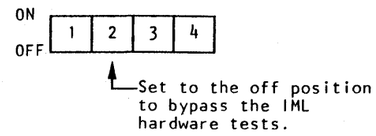
The following steps must be performed while the Status Pending lamp is on. A system reset at this time overlays the sense area in control storage with a selective reset sense group.

1. Connect the MD to the 3880.
2. Select the support mode by entering an S at date message or when the maintenance option menu is displayed.
3. Select the storage director.
4. Select Option 5 (manual control) when the support menu appears.
5. When the manual control frame appears, enter R1 to stop the storage director clock.
6. Enter RSD to reset the storage director. The Status Pending lamp is also turned off.
7. Enter an R to start the storage director clock. The Wait lamp should come on.
8. Press the CS key on the MD keyboard to turn off the AN lamp.
9. Press the reset key (Z) to return to the maintenance option menu.
10. Select Option 8 (diagnostic aids).
11. Select the storage director.
12. When the diagnostic aids menu appears, select Option G (read SD status). The 'Reading Sense Data From SD x' message appears. The Process and Wait indicators flash on and off alternately as the MD receives the data. This operation takes about 2 minutes.
13. When the operation is complete, the IML sense data (from the alternate storage director) and the functional diskette part number are displayed. Press the Enter key.
14. The storage director functional code EC level and contingent connection control block is displayed. The first two bytes of the control block are the address of the failing device and the status presented. Press the Enter key.
15. The storage director format 3 sense area (from the alternate storage director) is displayed. Press the Enter key.
16. The sense byte area is displayed. These sense bytes were generated as a result of the unit check on IML. Use this information to analyze the problem.

Bypass IML Hardware Tests

If an IML cannot be completed due to failures in the IML hardware tests, you can bypass the IML tests and run selected Routine 70 tests, which are equivalent to the IML tests.

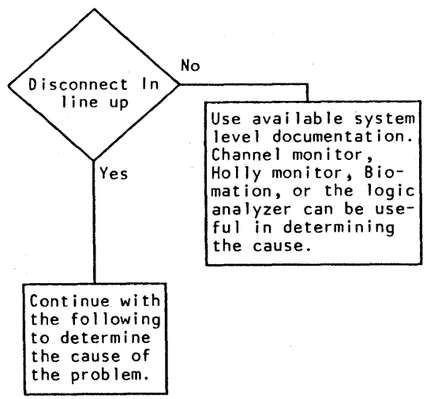
Setting switch two (located on the 3880 diskette load control card at 01A-B4(B3)R2) to the off position, permits the IML hardware tests to be bypassed.



Note: All load control switches are set to the On position at the factory.

Interface Control Check

Analyze the EREP data or the system display frames. Determine the reason for the interface control check for the failing channel.



The Disconnect In line is used by the storage director whenever an error condition occurs that prevents a normal microcode termination of the sequence. Under certain error conditions when the storage director is unable to complete an I/O interface sequence correctly, the storage director hardware interrupts the channel by using the Disconnect In line.

Disconnect In is activated by a storage director only when it is connected to the channel; that is, when Operational In is active. If an error condition occurs that prevents normal microcode termination of the sequence when the storage director is not connected to the channel, the storage director hardware generates a polling sequence and activates the Disconnect In line after the channel sequence has proceeded to the point of activating the Command Out line.

The channel, in response to the Disconnect In line, performs a selective reset. The Disconnect In and Operational In lines are maintained until the initiation of selective reset.

The alternate storage director is notified of the error. It gathers error information from the failing storage director, and then returns an Error Alert Response to the failing storage director. This allows selective reset to be completed. The next SIO to the alternate storage director receives a unit check and causes a format 3 sense group to be presented. If the alternate storage director cannot present sense data to the processor (offline, disabled, not cabled, and so on), the sense data can be read by the MD only.

1. Connect the MD to the 3880.
2. Select Option 8 (diagnostic aids) when the maintenance option menu appears.
3. Select the alternate, non-failing storage director.
4. When the Diagnostic Aids menu appears, select Option G (read SD status). This takes about 2 minutes.

The failing storage director presents a unit check to the next SIO. If a device was selected when the Check 1 occurred, a format 2 sense group (FSC 2929) is presented.

Use sense data for entry to the 3880 Maintenance Manuals (See the ECI section in the ECM, or the START section in the MIM).

Inline Diagnostic or MD Hang

Control storage maintains a table to trace the communication sequences between the MD and 3880, and between the device CE panel and 3880. This maintenance connection trace table helps isolate causes of inline diagnostics or MD hangs. The trace table also contains microcode inline trace points for microcode analysis (1xxx, 2xxx, 4xxx entries).

Figure 1 on this page shows a typical example of a communication sequence between the device CE panel and the storage director.

Figure 1 on the next page shows a typical example of a communication sequence between the MD and the storage director.

Figures 2, 3, and 4 on the next page show other state-save tables containing information related to these sequences.

The following paragraphs describe the format of the entries in the maintenance connection trace table.

Maintenance Connection Commands/Responses:

1. Device CE Panel (or MD at drive) to Storage Director Communication

   DCxx Entry generated from a drive by using a CE panel or the MD. xx is the byte transmitted from the device.

2. Storage Director-To-Device CE Panel or MD.

   The CE panel display uses the same format as the MD:

   82xx Routine is loading
   8Cxx Routine is running
   8Dyy Dynamic error display
   COxx Invalid routine
   COOO Reset occurred while in diagnostic mode
   CAxx Routine ready for execution
   CExx Routine stopped
   CFxx End of routine
   Dxnn Parameter entry required
   Exyy Error or message stop
   Fxyy Error detected by storage CTRL

   where:

   x = Parameter byte number or message byte number

   xx = Routine number

   nn = Routine number

   yy = Error number

3. MD to storage director using the maintenance interface:

   CCC1 Sequence generated by the MD. CCC1 indicates that the MD has a byte of data to transmit. CDxx identifies data byte xx.

4. Storage director to MD using the maintenance interface:

   Dxyy Parameter request. x is the parameter number.

   CAyy All parameters entered are ready to execute.

   CEyy End of message bytes, routine stopped.

   CFyy End of routine.

   E1xx Error or message stop. xx is the message number.

   where:

   yy = Routine number

CE To Storage Director Communication

Hex	0	1	2	3	4	5	6	7
000	726B	119A	1000	11A2	1022	1450	4050	11A2
008	1000	11A6	102B	82BB	1452	40BB	8CBB	4020
010	1020	1454	4054	1188	1000	1184	1022	1456
018	4056	118A	1000	1186	1022	1458	4058	11A0
020	1000	119D	1025	CFBB	DCAB	82AB	1418	406F
028	141A	40AB	CAAB	DC00	8CAB	8CAC	1020	145E
030	40AB	417A	1000	4181	1004	E112	DC20	E200
038	DC20	E300	DC20	E435	DC20	E500	DC20	E633
040	DC20	E702	DC20	E813	DC20	CEAB	CCC1	DC3D
048	D13D	CCC1	CD00	CA3D	CCC1	CD00	4DF7	1004
050	E180	CCC1	CD20	CE3D	CCC1	CD3D	D13D	CCC1
058	CD02	D23D	CCC1	CD03	D33D	CCC1	CD00	D43D
060	CCC1	CD00	CA3D	CCC1	CD00	49FB	1025	CF3D

```
DCAB    Request from drive CE panel to load
        routine AB
82AB    'Routine Loading' sent back to CE panel
CAAB    'Routine Ready to Execute' sent back to panel
DC00    00 from CE panel   'start execution'
8CAB    'Routine Running' sent back to CE panel
E112    Error Byte 1
DC20    Request Error Byte
E200
DC20
E300
DC20
E435
DC20    This sequence is generated by reading the
E500    error bytes from the CE panel at the drive.
DC20
E633
DC20
E702
DC20
E813
DC20
CEAB    End of the message bytes.  Routine is stopped.
```

Figure 1. Maintenance Connection Trace Table Sample

Sample sequence generated by loading routine AB from the drive CE panel, executing the test, and reading out error bytes. 1xxx, 2xxx, 4xxx entries are microcode inline trace points used for microcode analysis.

Inline Diagnostic or MD Hang (Continued)

MD to Storage Director Communication

Hex	0	1	2	3	4	5	6	7
000	726B	119A	1000	11A2	1022	1450	4050	11A2
008	1000	11A6	102B	82BB	1452	40BB	8CBB	4020
010	1020	1454	4054	1188	1000	1184	1022	1456
018	4056	118A	1000	1186	1022	1458	4058	11A0
020	1000	119D	1025	CFBB	DCAB	82AB	1418	406F
028	141A	40AB	CAAB	DC00	8CAB	8CAC	1020	145E
030	40AB	417A	1000	4181	1004	E112	DC20	E200
038	DC20	E300	DC20	E435	DC20	E500	DC20	E633
040	DC20	E702	DC20	E813	DC20	CEAB	CCC1	DC3D
048	D13D	CCC1	CD00	CA3D	CCC1	CD00	4DF7	1004
050	E180	CCC1	CD20	CE3D	CCC1	CD3D	D13D	CCC1
058	CD02	D23D	CCC1	CD03	D33D	CCC1	CD00	D43D
060	CCC1	CD00	CA3D	CCC1	CD00	49FB	1025	CF3D

```
CCC1 DC3D  MD sends 3D to storage director (3D is the trace function).
D13D       Storage director responds with parameter request.
CCC1 CD00  MD sends 00 parameter to storage director (read trace status).
CA3D       Storage director responds "all parameters entered, ready to execute".
CCC1 CD00  MD sends 00 to the storage director (start execution).
E180       Storage director responds with trace status.
CCC1 CD20  MD sends 20 to the storage director (request message bytes).
CE3D       Storage director responds with end of message bytes.
CCC1 CD3D  MD sends 3D to storage director (load trace).
D13D       Storage director responds with parameter request.
CCC1 CD02  MD sends 02 to the storage director (trace all devices).
D23D       Storage director responds with parameter request.
CCC1 CD03  MD sends 03 to the storage director (channel and block trace).
D33D       Storage director responds with parameter request.
CCC1 CD00  MD sends 00 to the storage director (no device address).
D43D       Storage director responds with parameter request.
CCC1 CD00  MD sends 00 to the storage director.
CA3D       Storage director responds with all parameters entered, ready to execute.
CCC1 CD00  MD sends 00 to the storage director (start-execution).
CF3D       End of routine.
```

Figure 1. Maintenance Connection Trace Table Sample

Sequence generated by MD: Read Trace Status, Start Trace.

Inline (Diagnostic) Parameter Area

Hex	0	1	2	3	4	5	6	7
000	0203	0000	OFFF	OFFF	OFFF	OFFF	OFFF	OFFF

Parameters entered for inline diagnostics variable length

Figure 2. Inline Parameter Trace Table Sample

Inline (Diagnostic) Message Area

Hex	0	1	2	3	4	5	6	7
000	8000	0035	0033	0213	0000	2000	4000	8000

Error or Message Bytes Displayed

Figure 3. Inline Message Trace Table Sample

Inline (Diagnostic) Control Storage Area

Hex	0	1	2	3	4	5	6	7
000	009C	0100	AB5E	AB5E	3800	0000	0000	0100
008	0000	0000	0000	0000	0000	0000	1452	4000
010	AB0A	43FB	005A	CF3D	0000	0000	0000	0000
018	0000	0000	0000	0000	0000	0000	0000	0000

Run Options

Current Routine ID

Controller and Device Address

Error Bytes From Controller (8 Bytes)

For other byte assignments, refer to 'Inline (Diagnostic) Control Storage Area' in the state-save portion of the PDA section.

Figure 4. Inline Control Storage Trace Table Sample

Maintenance Interface

MD Adapter Test

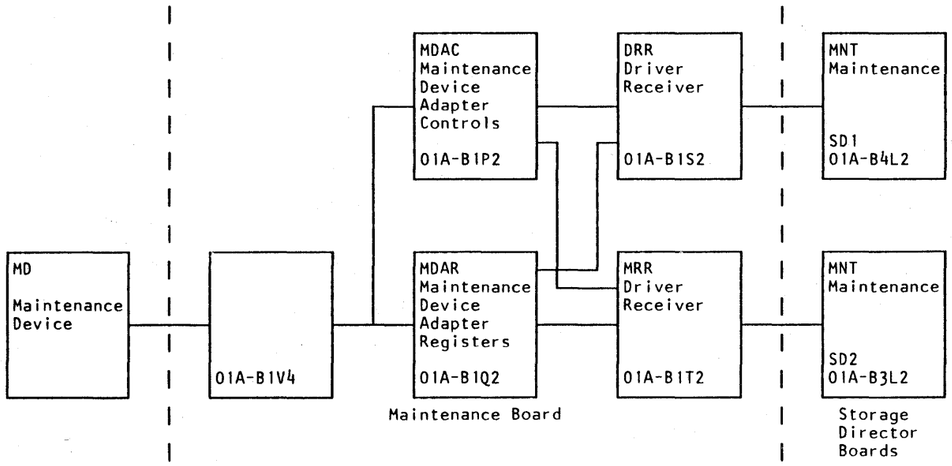
The MD adapter test is used to verify the correct operation of the MPAC (01A-B1P2), MDAR (01A-B1Q2), and DRR (01A-B1T2) cards. This test does not select a storage director. It runs when the storage director is not operational or is powered off. The maintenance device adapter (MDA) is tested with command sequences and the results are verified by the MD. See the Error Correction Index (ECI) section of the Error Code Manual Manual (ECM) regarding any isolation codes received during the test.

Storage Director Select Test

The storage director is selected with this test. Therefore, the storage director must be operational (functional microcode loaded). Commands are sent from the MD to the storage director through the MDA. The results are verified using the MD.

Maintenance Connection Test

This test verifies that the signal lines are connected from the MD through the MDA to the selected storage director. This test uses the functional microcode of the selected storage director.



MD Connector Pin	
5	B09 -MD Enable Interface
7	B06 -MD Shift
9	B02 -MD Status In
13	B07 -MD Data In
15	B05 -MD Write
19	B03 -MD Status Out
21	B04 -MD Read
25	B08 -MD Data Out

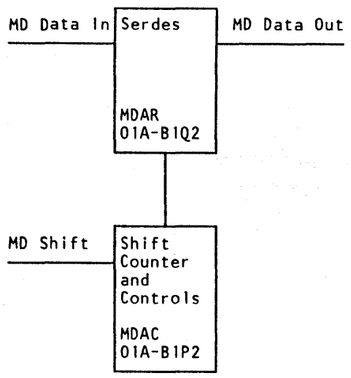
Pins 4, 8, 10, 14, 16, 20, 22, and 24 are ground pins; the other pins are not used.

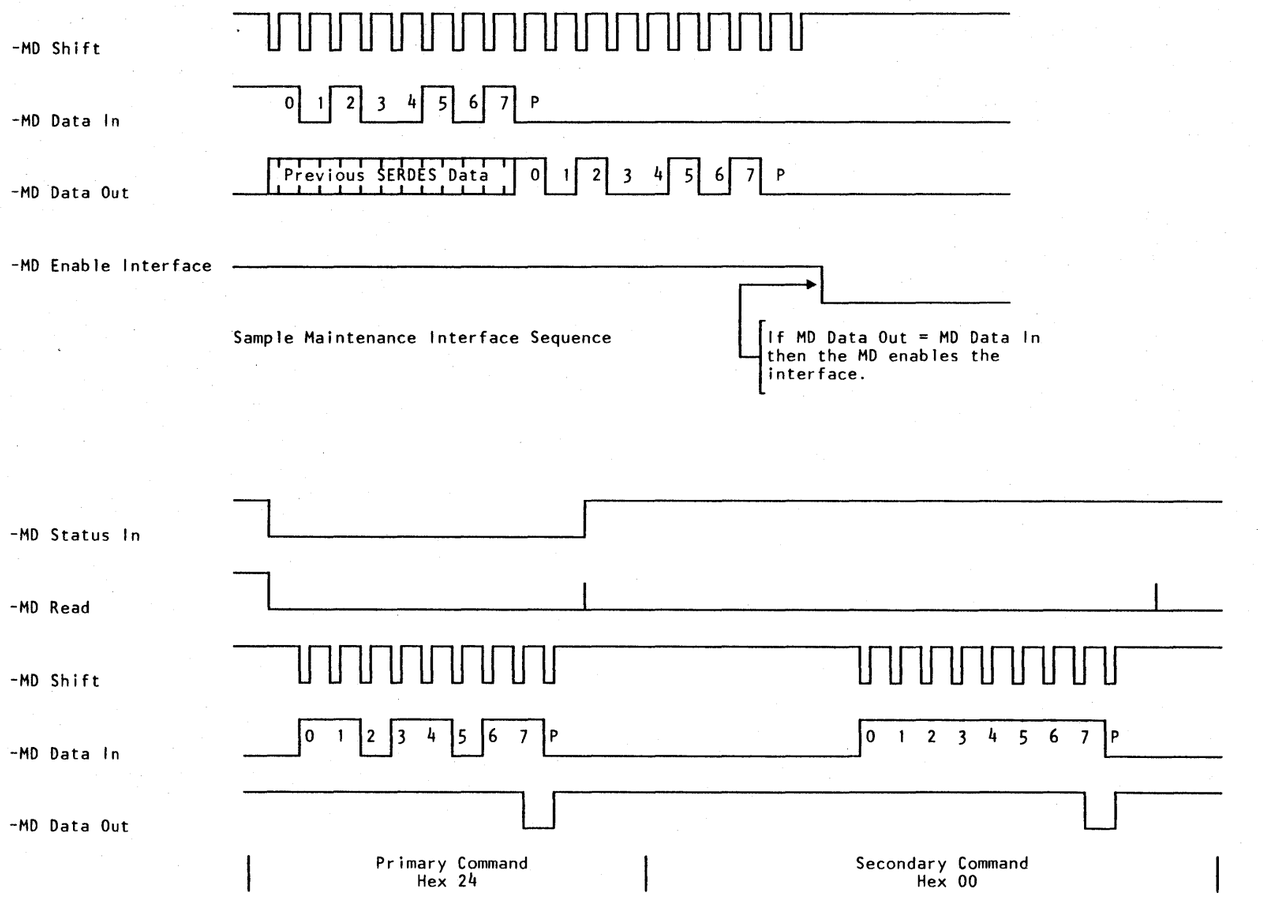
MD To MDA Port Loop

This test is an initial checkout of the MDA Serializer/Deserializer (SERDES) by the MD microcode. It is an exception to the normal MD-to-MDA communication because the MD interface line is not activated.

The MD places the first of nine bits (0-7, P) on the MD Data In bus and activates the MD Shift line. No other control lines are active at this time. The inactive MD Enable Interface line holds the MDA reset. The MD Shift line shifts the first bit on MD Data In into the MDA SERDES. This line is pulsed 18 times. The first nine pulses shift one byte of data into the MDA SERDES, bit 0 first. The second nine pulses shift the byte out of MDA SERDES onto the MD Data Out line. The MD then compares the result to the byte sent.

This test does not select a storage director and loops even if the storage director is not operational.





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Generalized Trace Facility

The Generalized Trace Facility (GTF) is a service aid program used to diagnose system problems. The following can be traced using the Generalized Trace Facility:

- Start I/O Operations
- I/O Interrupts
- PCI Interrupts
- SVC (Supervisor Call) Interrupts
- Program Interrupts
- External Interrupts
- Any Event Defined by GTRACE

The GTF program is particularly useful to help define hardware failures that are subtle in nature and difficult to resolve (for example, missing interrupts, unusual status presentation, and so on). The program can have a high impact on customer throughput. To minimize this impact, trace only those devices involved in the failure.

GTF produces system trace records with two kinds of format: comprehensive and minimal. The GTF trace record output can be maintained in virtual storage (internal mode) or directed to the IEFRDER data set on an external storage device (external mode). If space is limited in either mode, GTF overlays previously stored or written data. To retrieve GTF data, use the edit function of the PRDMP service aid program.

Start GTF

To start the Generalized Trace Facility, enter a Start command from the operator console. Using the Start command, select the IBM-supplied GTF cataloged procedure or your own cataloged procedure. A minimal set of data is recorded on a disk data set.

It is likely that only specific devices and/or options must be traced. Your program support and/or customer system programmer can set up the GTF trace needed for the specific problem.

The following is an example of a cataloged procedure to trace SIO and I/O interrupts for addresses 240 through 247.

```
//  USER Name   PROC    MEMBER = GTF PARM
//  IEF PROC    EXEC    PGM = AHLGTF, REGION = 2880 K
//                      PARM = MODE=EXT, DEBUG=NO, TIME=NO
//  IEFRDER     DD      DSName = SYS1.TRACE, UNIT = TAPE
//                      DISP = ( , KEEP)
//  SYSLIB      DD      DSN = SYS1.PARMLIB (GTFA), DISP=SHR
```

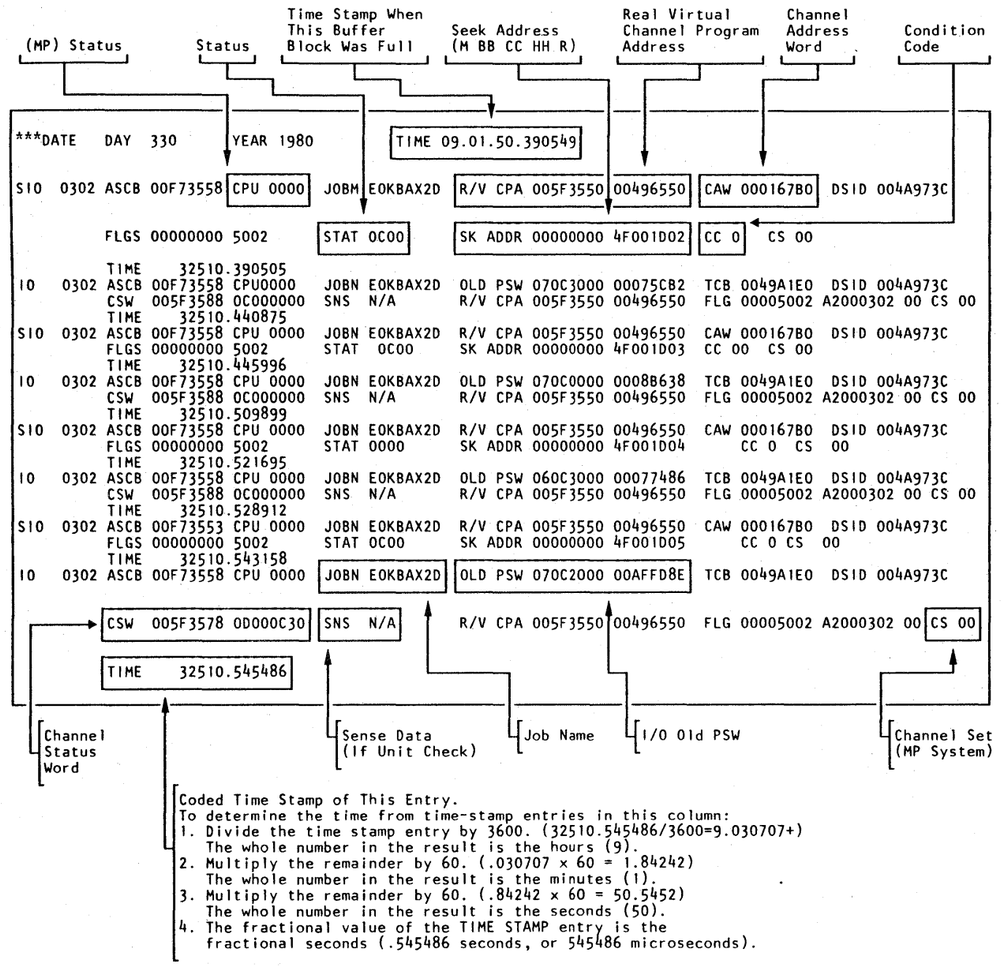
To store the options in SYS1.PARMLIB, use the following JCL:

```
//  GTFPARM     JOB     MSGLEVEL = (1, )
                EXEC    PGM = IEBUPDTE, PARM = NEW
//  SYSPRINT    DD      SYSOUT = A
//  SYSUT2      DD      DSName = SYS1.PARMLIB, DISP=SHR
//  SYSIN       DD      DATA
./  ADD         Name = GTFA, LIST = ALL, SOURCE = 0
TRACE = SIO, IO
I/O = (240, 241, 242, 243, 244, 245, 246, 247)
/*
```

Print GTF

A PSR or system programmer can use the edit function of the PRDMP service aid program to print the GTF data. To avoid printing a large volume of data, select the time frame of the suspected failure.

Sample of Generalized Trace



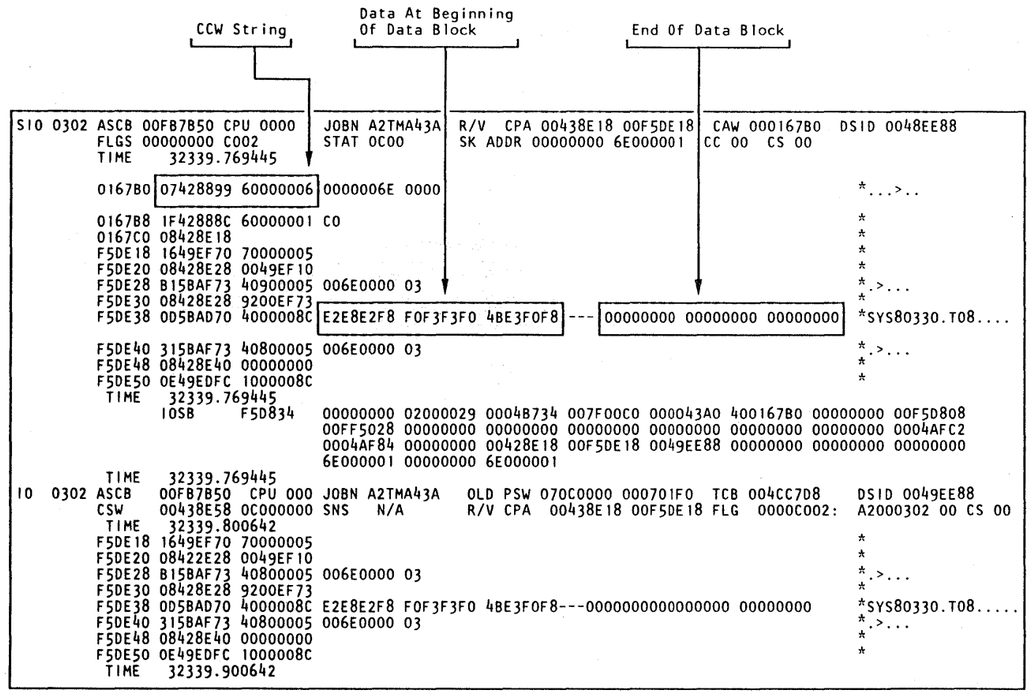
CCW Trace

CCW Trace is an unofficial modification of the operating system. It provides the IBM representative with the ability to trace CCWs and their associated data, in addition to the standard GTF information. It can trace:

- Up to 512 CCWs for each event
- Up to 32767 bytes of data for each CCW
- IOSB on request
- EWA on request

This service aid is installed by the PSR and/or customer and is available in the data link library.

Sample of a CCW Trace




```
SIO 0302 ASCB 00FB7B50 CPU 0000   JOBN A2TMA43A  R/V  CPA 00438E18 00F5DE18  CAW 000167B0  DSID 0048EE88
         FLGS 00000000 C002       STAT 0C00     SK ADDR 00000000 6E000001  CC 00  CS 00
         TIME    32339.769445

         0167B0 07428899 60000006 0000006E 0000                              *...>..

         0167B8 1F42888C 60000001 C0                                         *
         0167C0 08428E18                                                     *
         F5DE18 1649EF70 70000005                                            *
         F5DE20 08428E28 0049EF10                                            *
         F5DE28 B15BAF73 40900005 006E0000 03                                *.>...
         F5DE30 08428E28 9200EF73                                            *
         F5DE38 0D5BAD70 4000008C E2E8E2F8 F0F3F3F0 4BE3F0F8---00000000 00000000 00000000 *SYS80330.T08....

         F5DE40 315BAF73 40800005 006E0000 03                                *.>...
         F5DE48 08428E40 00000000                                            *
         F5DE50 0E49EDFC 1000008C                                            *
          TIME   32339.769445
               IOSB     F5D834   00000000 02000029 0004B734 007F00C0 000043A0 400167B0 00000000 00F5D808
                                 00FF5028 00000000 00000000 00000000 00000000 00000000 00000000 0004AFC2
                                 0004AF84 00000000 00428E18 00F5DE18 0049EE88 00000000 00000000 00000000
                                 6E000001 00000000 6E000001
          TIME   32339.769445
IO  0302 ASCB   00FB7B50  CPU 000 JOBN A2TMA43A   OLD PSW 070C0000 000701F0  TCB 004CC7D8    DSID 0049EE88
         CSW    00438E58 0C000000 SNS   N/A       R/V CPA  00438E18 00F5DE18 FLG  0000C002:  A2000302 00 CS 00
          TIME   32339.800642
         F5DE18 1649EF70 70000005                                            *
         F5DE20 08422E28 0049EF10                                            *
         F5DE28 B15BAF73 40800005 006E0000 03                                *.>...
         F5DE30 08428E28 9200EF73                                            *
         F5DE38 0D5BAD70 4000008C E2E8E2F8 F0F3F3F0 4BE3F0F8---0000000000000000 00000000     *SYS80330.T08.....
         F5DE40 315BAF73 40800005 006E0000 03                                *.>...
         F5DE48 08428E40 00000000                                            *
         F5DE50 0E49EDFC 1000008C                                            *
          TIME   32339.900642
```

Channel Monitor

The purpose of the channel monitor (CM) is to capture and save on tape a large volume of events that occur on an interface. This data can later be displayed and analyzed on-site and/or at a remote location.

The hardware consists of an adapter box and a high-speed buffer array (64 addresses x 64 bits), connected to a PT-2.

For the 360/370 channel interface, the CM is an extension of the Holly monitor. In addition, it can also monitor a DASD controller interface. The PT-2 software programs provide user-flexible control of the events to be captured, stopped on, or displayed. This is helpful on intermittent problems, that cannot be recreated or scoped.

For additional information, see the PT-2 Channel Monitor operation Maintenance Library Manual.

Channel Monitor Connection

T-Connector-To-Channel

1. Stop all activity on the channel to be monitored.
2. For non-308x systems:

   a. Disconnect the bus in and tag in cables (light gray) from the tailgate and connect them to the T-connector. These are the cables from the previous control unit or channel.

      CAUTION
      To prevent possible false Select In errors, place the T-connector between the host system and the first physical unit.

   b. Connect bus/tag jumper cables between the tailgate and the T-connector.

      Note: The channel monitor can be removed from the T-connector any time that the channel is in operation.

3. For 308x systems, use the adapter card kit.

Channel Monitor to PT-2 Connection

1. Set the PT-2 on the feet provided on the bottom of the keyboard.
2. Position the CM latch level so that the end of the handle points toward the CM On/Off switch and is all the way in.
3. Position the socket and pin guides of the CM adapter sockets to the rear of the PT-2 matching sockets. Do not apply downward pressure.
4. Pull and rotate the CM latch level handle counterclockwise until the CM connectors are fully seated on the PT-2 connectors. When fully seated, the handle should be parallel to the back of the PT-2

   CAUTION
   Do not use force. If there are any problems, refer to the procedures in the Channel Monitor Operation manual.

T-Connector-To-Channel Monitor

1. Plug the CM signal cable into the matching socket in the T-connector.
2. Plug the CM power cable into an appropriate power source.

PT-2 Connection

1. Plug the power and video cables into the rear of PT-2.
2. Connect the video cable to the PT-2 and the display unit.
3. Plug the PT-2 power cable into an appropriate power source.

   Do not plug more than two test boxes into a control unit or device convenience outlet. Use the customer receptacle.
4. Power on the CM and then the PT-2.

   Note: If you power on the CM while a program is loaded in the PT-2, you must reload the program.

Channel Monitor Application Programs

The channel monitor application programs are contained on tape cartridge (part 1857013).

CHTOOL

Use the PF keys to select one of the following channel monitoring applications of the CHTOOL program:

- CMDIAG
- CHMCAP
- CHMED
- CTLCAP
- CTLED

This program automatically loads and executes the channel monitor diagnostics (CMDIAG) before loading the selected program.

CMDIAG

The channel monitor diagnostic (CMDIAG) program provides an adapter checkout of the channel monitor hardware.

CHMCAP

The channel monitor initialization/capture (CHMCAP) program (used on 360/370 type channels) selects the options the user wishes to trace and stop on.

1. The channel monitor is initialized with the selected options.
2. The trace continues until either a stop condition is encountered or the user manually stops the trace.
3. The data can be displayed on the screen or recorded on tape.

CHMED

The channel monitor edit (CHMED) program (used only on 360/370 type channels) reads the recorded trace data from tape and displays it in meaningful formats. The trace data can be displayed in either horizontal or vertical mode. A scrolling option allows access to all recorded events. A search facility allows quick and easy access to a specific event within a file.

CTLCAP

The channel monitor initialization/capture (CTLCAP) program selects the trace and stop conditions for the control interface. The selected options can be used to trace a control interface. When a stop condition occurs, the trace data can be displayed on the PT-2 screen or recorded on tape.

CTLED

The controller monitor edit (CTLED) program reads the recorded control interface trace data from tape and displays it in either horizontal or vertical mode. Scrolling and search options permits the CE to find the desired data quickly and easily.

Channel Monitor Initialization Procedure

1. Load the channel monitor application tape program (part 1857013) into the PT-2 by pressing the LCL/IPL key.
2. Enter the requested serial number, branch office, and security code. Press the Enter key. A tape-mounted message appears after SYSCLP is loaded.
3. Enter L CHTOOL. Press the SYS FUNC key and then the Enter key. When the program is loaded, the following menu is displayed.

```
          CHANNEL MONITORING APPLICATIONS

              **360/370 TYPE CHANNELS**
PF 1 - CAPTURE AND SCOPE     PF 2 - EDIT AND SEARCH

          **CONTROL  INTERFACE  CHANNELS**
PF 4 - CAPTURE AND SCOPE     PF 5 - EDIT AND SEARCH

                               PF 7 - DIAGNOSTIC

SERVC-LOC  CHTOOL/0010/0000
31  SEARCHING TAPE FOR (CHTOOL)
41  LOADING
51  LOAD COMPLETE
6R  R01 PRESS THE PF KEY FOR THE FUNCTION TO PERFORM
L  CHTOOL
```

4. Select one of the five channel monitoring applications by pressing the appropriate PF key, followed by the Enter key.

   Note: Loading a capture program causes an adapter checkout of the channel monitor hardware. If an error occurs during this checkout, see the Channel Monitor Operation Maintenance Manual, Maintenance section.

Channel Trace Setup

CHMCAP

1. Use the initialization procedure to select the 360/370 type channel, capture, and scope program (PF1, Enter). If this method is used to select the program, the adapter checkout program (CMDIAG) is automatically loaded. To bypass the adapter checkout, enter L CHMCAP and press the SYS FUNC key.

2. Enter time and date as requested.

3. The following frame appears.

```
                    CHANNEL  MONITOR
                       CAPTURE

PF 1 Build Trace/Stop Table     PF 6  List Tape Trace/Stop Tables
PF 2 Load T/S Table From Tape   PF 7  Trace and Display on Screen
PF 3 Store T/S Table on Tape    PF 10 Cancel Operation
PF 4 Trace and Record on Tape   PF 12 End of job
PF 5 Stop Trace

SERVC-LOC  CMHCAP/0010/0000
2R T03. REENTER IF NOT CORRECT.  PRESS ENTER TO START TIMER
3I T04. TIMER STARTED
3I C36. MOUNT TAPE TO BE USED
5I C80. SELECT FUNCTION
10,24,00,02,28
```

4. Mount the tape cartridge to record the traces.

5. Press the PF1 key to build the trace/stop table. This activates a routine that allows the user to build a trace/stop table or change the existing loaded table. The table can contain up to 10 unique masks and can be stored on tape (PF3).

6. Enter the desired entry or mask number (1 through 10). The existing values for the total number of events and the number of events after stop are now displayed. Change the values or press the Enter key to accept the existing values.

7. The next frame displays the trace conditions.

```
                    TRACE  CONDITIONS

    (ENTER  Y-YES,  N-NO,  ->  CURSOR  RIGHT,  ENTER-END)

   Y ADR IN    RISE     Y STA IN   RISE      Y SRV IN   RISE
   Y DAT IN    RISE     Y ADR OUT  RISE      Y CMD OUT  RISE
   Y SRV OUT   RISE     Y DAT OUT  RISE      Y OPL OUT  RISE
   Y OPL IN    RISE     Y SEL OUT  RISE      Y SEL IN   RISE
   Y HLD OUT   RISE     Y REQ IN   RISE      Y SUP OUT  RISE
   Y DIS IN    RISE     Y OPL OUT  FALL      Y OPL IN   FALL
   Y EXT SYNC  RISE     Y EXT SYNC FALL      N RESET TIMESTAMP
   Y TIMESTAMP OVERFL   Y BYTE COUNT
   N TRACE DEVICES      N TRACE INIT SEL
**WARNING**
-TRACE ON devices:  ADR OUT,  ADR IN, and OP IN FALL must
be traced.  (Traces only the selected dev. from ADIN
or ADOUT to OPIN FALL.)
-TRACE INIT SEL:  TR DEV,  ADR OUT and OP IN FALL must
be  selected.

320
```

A letter to the left of the trace option indicates its state (Y = trace, N = No trace). Change the trace options or press the Enter key to accept the existing values.

8. The next frame displays the existing stop/trace conditions. Any of these events trigger a stop to the trace.

```
                    STOP  CONDITIONS

    (ENTER Y-YES,  N-NO,  -> CURSOR  RIGHT,  ENTER-END)

 Y ADR IN GLITCH     Y STA IN GLITCH     Y SRV IN GLITCH
 Y DAT IN GLITCH     Y MULTI OUT TAGS    Y MULTI IN TAGS
 Y SYSTEM RESET      Y SELECTIVE RESET   Y HALT I/O
 Y SEL IN ERROR      Y OPL IN ERROR      Y COMMAND RETRY
 Y DISC IN RISE      Y EXT SYNC SHIFT    N EVENT MARK
 Y BUS OUT PARITY    Y BUS IN PARITY
 Y PT-2 OVERRUN      N BUFFER FULL


 320
```

Change the stop/trace options or press the Enter key to accept the existing values.

The specific device selection frame appears next. To trace all devices, press the Enter key. To trace only certain devices, you must have previously selected the trace devices on the trace conditions frame.

9. Table entry (X) is now completed. If no more table entries are to be created, enter N and press the Enter key.

10. The channel monitor capture frame appears (Step 3 above) next. Press PF4 to trace and record on tape.

11. Enter the track (1, 2, 3 or 1N, 2N, 3N) to record the trace. Extended mode allows the data to be written after a previously recorded stop number or after the last recorded trace on the track (EOV). Ensure that the Track Protect switch, located inside the top cover of the PT-2, is in the Write/Erase position for the selected track.

12. The problem description frame is displayed.

```
                CHANNEL  PROBLEM  Description

CUSTOMER  Name:
CE Name:                              -> CURSOR  RIGHT
PHONE #:                              <- CURSOR  LEFT
PROBLEM  ID:                          BACK
Description                           SPACE - CURSOR DOWN
:
:
:
SERVC-LOC CTLCAP/0020/0003
2R C21. ANOTHER TABLE ENTRY (Y-YES,N-NO)
3I C80. SELECT FUNCTION
4R C01. TYPE TRACK TO RECORD (1 2 3) OR (1E 2E 3E) TO EXTEND
5I C$1. ENTER Description
3
```

Enter the requested information (for your reference) or press the Enter key to skip it.

13. Answer Y or N to the rearm question. Rearming allows the trace to continue after a stop condition is detected and the trace data is recorded. A different set of trace conditions can be used for each sequential trace. The trace/record/rearm sequence continues until the track is full or the user stops the operation.

14. If the user answers N or no to the rearm question, a message is displayed asking the user to enter the table entry number to be used (previously setup by PF1).

15. To begin tracing, press the Enter key when requested.

16. The Tracing In Progress message is now displayed. If a stop condition occurs, a Recording Data message appears and the trace is recorded on tape. If rearming is active, tracing begins again. If rearming is not active, the channel monitor capture frame appears.

17. To display the trace, load the channel monitor edit program (CHMED).

CHMED

The channel monitor edit program is used with 360/370 type channels.

1. Use the initialization procedure to select 360/370 type channel edit and search program (PF2), or enter L CHMED, press the SYS FUNC key and then the Enter key.

   When the channel monitor edit program is loaded, the following display appears:

```
                    CHANNEL  MONITOR  EDIT

PF 1 - Set Data Display Mode and Options
PF 2 - Display Descriptor Records
PF 3 - Select A New Track, File or Event Number
PF 4 - High Level Search                    PF 5 - Basic Search
PF 6 - Display Next Event Found By The Search Facility
PF 7 - Scroll Up                            PF 8 - Scroll Down
PF 10 - Scroll Backward                     PF 11 - Scroll Forward
PF 9 - Tape Table Of Contents               PF 12 - End Of Job
PROG  INIT - File Selection
SERVC-LOC CHMED /0010/0000
31  Loading
41  Load Complete
51  E00. File Selection
6R  E01. Enter Track Number (1,2,3)
L  CHMED                                                      WAIT
```

   This frame describes the options available with the channel monitor edit program. Only options that are highlighted can be selected at this time. The message asks for a user to select a track for display.

2. Enter the track number. The channel problem description appears. Also displayed is a message asking the user to select a stop number (00 to 99). The default stop number is 00.

3. Enter the stop number. The selected track is read again to find the requested stop number. When the stop number is found, a message asks the user to select an event from the displayed range. Pressing the Enter key alone displays the event that caused the stop condition (entry + 0).

4. Enter the trace event. The tape data is loaded into the PT-2 buffer. The selected event and enough additional trace data to fill the screen are displayed in horizontal mode. (See sample below.)

```
CHM.EDIT   (TRACK  3  STOP00)
           1  23 45
           .     +10    .     +20    .     +30    .     +40    .     +

01 BUS        3  0       3  0       3  0       3  0  0  0  0  0       3  0
     IN       9  0       2  C       2  0       2  0  0  0  0  0       2  0

02 ADR IN  ---11 -----  -11-- ----  -11-- ----1 1---- -----  ---11 -
03 STA IN  ----- 11---  ---11 1---  ---11 -----  -----  -----  ----- -
04 SRV IN  ----- -----  ----- ----  ----- -----  -1111 1111-  ----- 1
05 DAT IN  ----- -----  ----- ----  ----- -----  ----- -----  ----- -
06 OPL IN  --111 11---  11111 1---  11111 ---11  11111 1111-  --111 1
07 SEL IN  ----- -----  ----- ----  ----- -----  ----- -----  ----- -
08 REQ IN  ----- ---11  ----- ----  ----- -11--  ----- -----  11--- -
09 DIS IN  ----- -----  ----- ----  ----- -----  ----- -----  ----- -
10 BUS     3  1  1     0  0  3   0  0        0  4  4   7  7        0
     OUT   9  E  E     0  0  2   9  9        0  0  0   F  F        0

11 ADR OUT 111-- -----  ----- --11 1---- -----  ----- -----  ----- -
12 CMD OUT ----1 -----  --1-- ----  --1-- -----  1---- -----  ----1 -
13 SRV OUT ----- -11--  ----- 11--  ----1 1----  --1-1 -1-11  ----- -
14 DAT OUT ----- -----  ----- ----  ----- -----  ----- -----  ----- -
15 OPL OUT 11111 11111  11111 1111  11111 11111  11111 11111  11111 1
16 SEL OUT 11111 11111  11111 1111  11111 11111  11111 11111  11111 1
17 HLD OUT -111- ----1  11--- ---1  11--- -----  -111- -----  ----- 1
           .     +10    .     +20    .     +30    .     +40    .     +

PRESS MENU KEY FOR HELP OR TYPE S TO LOOK AT THE SEARCH MENU.WAIT
```

5. Use the PF10 (left) and PF11 (right) keys to horizontally scan (scroll) the data. Use the PF8 (down) and PF7 (up) keys to view additional recorded lines. Use the Channel Monitor Operation Manual to obtain additional information about this display.

6. Press the PF1 key to change the display format to vertical mode. The following frame appears:

```
  CMH.EDIT   DATA  DISPLAY

Horizontal Data Display Mode Is Now Active
Enter V To Select The Vertical Mode

     A To Display The Data

     X #### To Modify The BKWD/FWD Scroll Value (NOW: 0020 )
     Y  ## To Modify The Up/Down Scroll Value  (NOW:  09)

     S ##,##..To Suppress The Display Of Lines Number ##,##..
     L ##,##..To Reactivate The Display Of Lines Numb. ##,##...
     L All To Display All Lines

-4095                                                      WAIT
```

   a. Scrolling values and display options can be changed. Enter V to select vertical mode. The trace data is displayed as shown:

```
  CHM.EDIT
EVENT    .PAR .ADDR.ADDR.CMD .STAT.SERV.SERV.DATA.DATA.
 NUMBER  .ERR .OUT .IN  .OUT .IN  .OUT .IN  .OUT .IN  .

1   +5   .    .39  .    .    .    .    .    .    .    .
2   +8   .    .    .39  .    .    .    .    .    .    .
3   +9   .    .    .    .1E  .    .    .    .    .    .
4   +10  .    .    .    .    .00  .    .    .    .    .
5   +11  .    .    .    .    .    .1E  .    .    .    .
    +16  .    .    .32  .    .    .    .    .    .    .
    +17  .    .    .    .00  .    .    .    .    .    .
    +18  .    .    .    .    .0C  .    .    .    .    .
    +20  .    .    .    .    .    .00  .    .    .    .
    +21  .    .    .    .    .    .    .00  .    .    .
    +23  .    .32  .    .    .    .    .    .    .    .
    +26  .    .    .32  .    .    .    .    .    .    .
    +27  .    .    .    .09  .    .    .    .    .    .
    +28  .    .    .    .    .00  .    .    .    .    .
    +29  .    .    .    .    .    .09  .    .    .    .
    +34  .    .    .32  .    .    .    .    .    .    .
    +35  .    .    .    .00  .    .    .    .    .    .
    +36  .    .    .    .    .    .    .00  .    .    .
    +37  .    .    .    .    .    .40  .    .    .    .
    +38  .    .    .    .    .    .    .00  .    .    .
PRESS MENU KEY FOR HELP                              WAIT
```

   b. The data can be scrolled vertically with the PF10 and PF11 keys.

7. Press the Menu key to return the display to the list of available options. See the Channel Monitor Operation Manual for information on additional options.

Channel Monitor Continued)

CTLCAP

The channel monitor initialization/capture (CTLCAP) program is used to check the unidirectional control interface.

1. Use the initialization procedure to select the control interface, capture, and scope (PF4). If this method is used to select the program, the adapter checkout program (CMDIAG) is automatically loaded. To bypass the adapter checkout, enter L CTLCAP, press the SYS FUNC key, and then the Enter key.

2. Enter the time and date as requested. The following frame will be displayed:

```
PF 1 Build Trace/Stop Table     PF 6 List Tape Trace/Stop Tables
PF 2 Load T/S Table From Tape   PF 7 Trace and Display on Screen
PF 3 Store T/S Table on Tape    PF 10 Cancel Operation
PF 4 Trace and Record on Tape   PF 12 End of Job
PF 5 Stop Trace


SERVC-LOC CTLCAP/0010/0000
24 T03. REENTER IF NOT CORRECT. PRESS ENTER TO START TIMER
31 T04. TIMER STARTED
41 C36. MOUNT TAPE TO BE USED
51 C80. SELECT FUNCTION
10,24,00,02,28
```

3. Mount the tape cartridge to record the trace.

4. Press PF1 to build the trace/stop table. This activates a routine that allows the user to build a trace/stop table or change the existing loaded table. The table can contain up to 10 unique masks, and can be stored on tape (PF3).

5. Enter the desired entry or mask number (1 through 10). The existing values for the total number of events and the number of events after stop are displayed next. These can be changed at this time or press the Enter key to accept the existing values.

6. The next frame displays the trace conditions.

```
                    TRACE  CONDITIONS

     (ENTER Y-YES, N-NO, -> CURSOR RIGHT, ENTER-END)

Y TAG VALID           Y SYNC IN           Y CHECK END
Y NORMAL END          Y TAG GATE          Y SYNC OUT
Y SELECT HOLD RISE    Y SELECT ACT RISE   Y INDEX ALERT
Y RECYCLE             Y RESPONSE          Y ERROR ALERT
Y SELECT HOLD FALL    Y SELECT ACT FALL   Y EXT SYNC RISE
Y EXT SYNC FALL       Y RESET TIMESTAMP   N TIMESTAMP OVRFL
Y BYTE COUNT          N TRACE  DEVICES

**WARNING**
-TRACE ON DEVICES: TAG GATE AND SEL ACTIVE FALL MUST BE TRACED
(TRACES ONLY THE SELECTED DEV. FROM TAG GATE TO SEL ACT FALL)

1
```

A letter to the left of the trace option indicates its state (Y = Trace, N = No Trace). These options can be changed at this time or press the Enter key to accept the existing values. Using default options, all devices are traced with all bus and tag lines.

7. The next frame displayed is the existing stop conditions. Any of these events trigger a stop to the trace.

```
                    STOP CONDITIONS
     (ENTER Y-YES, N-NO, -> CURSOR RIGHT, ENTER-END)

Y TAG VALID GLITCH    Y SYNC IN GLITCH    Y CHK END GLITCH
Y NORM END GLITCH     Y ERROR ALERT       Y EXT SYNC
Y BUS OUT PARITY      Y BUS IN PARITY     Y TAG BUS PARITY
Y MULTI IN TAGS       N EVENT STOP
Y PT-2 OVERRUN        N BUFFER FULL
```

These options can be changed at this time or press the Enter key to accept the existing values.

The specific device selection frame appears next. If you want to trace all devices, press the Enter key to bypass. To trace only certain devices, the trace devices must have been previously selected on the trace conditions frame.

8. The table entry (X) is now completed. If no more table entries are to created, enter N and press the Enter key.

9. The control interface monitor capture frame appears (Step 3 above) next. Press PF4 to trace and record on tape.

10. Enter the track to record the trace (1, 2, 3 or 1N, 2N, 3N). Extended mode allows the data to be written after a previously recorded stop number or after the last trace on the track (EOV).

    Ensure that the Track Protect switch, located inside the top cover of the PT-2, is in the Write/Erase position for the selected track.

11. The problem description frame is displayed.

```
     CHANNEL PROBLEM DESCRIPTION

CUSTOMER Name:                  -> CURSOR RIGHT
CE Name?                        <- CURSOR LEFT
PHONE #:                        BACK
PROBLEM 1:                      SPACE - CURSOR DOWN
Description
SERVC-LOC CTLCAP/0020/0003


2R C21. ANOTHER TABLE ENTRY(Y-YES,N-NO)
31 C80. SELECT FUNCTION
4R C01. TYPE TRACK TO RECORD (1 2 3) OR (1E 2E 3E) TO EXTEND
51 C$1. ENTER Description)
```

12. Enter the requested information (for your reference) or press the Enter key to skip it.

13. Answer Y or N to the rearm question. Rearming allows the trace to continue after a stop condition is detected and the trace data is recorded. A different set of trace conditions can be used for each sequential trace. The trace/record/rearm sequence continues until the track is full or the user stops the operation.

14. If the user answers N or no to the rearm question, a message is displayed asking the user to enter the table entry number to be used (previously setup by PF1).

15. To begin tracing, press the Enter key when requested.

16. The Tracing In Progress message is displayed. If a stop condition occurs, a Recording Data message appears, the trace is recorded on tape. If rearming is active, tracing begins again. If rearming is not active, the channel monitor capture frame appears.

17. To display the trace, load the control monitor edit program (CTLED).

How to Eliminate Poll Sequences

The control interface is normally active and initiating poll sequences between the 3880 and the 3350-A2 controller. These consist of 82 tags, and occur even when no channel activity is present. To eliminate the 82 tags from the trace and to prevent this from overlaying other data, the Trace Devices option must be used when the trace conditions are entered.

1. When the trace conditions frame (see PDA 725) appears, select the Trace Devices option 'N'. After the stop options frame appears, the following specific device selection frame appears:

```
                SPECIFIC DEVICE SELECTION

BUS: XXXXXXXX    O TAG/BUS: 00      SYMBOLS  EXPLANATION
00                                  T: TRACE THIS DEVICE
FF                                  O: TRACE NO DATA BYTE
                                    *  IF NOT O, THE 1ST 32 DATA
                                       BYTES ARE TRACED

                                   TV: STOP ON TAG VALID
                                   TG:      "   TAG GATE
                                   SI:      "   SYNC IN
                                   SO:      "   SYNC OUT
                                   CE:      "   CHK END/NORM END

                                   *BLANK OPTIONS ARE INACTIVE

ENTER A COMMAND OR TYPE H FOR HELP
12,22,00,09,24
```

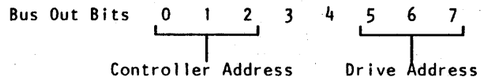
2. Press H and then the Enter key for the help frame.

```
 COMMANDS          EXPLANATION

##                 FIRST  DEVICE  DISPLAYED
H ##,T,O (OR 32), TV (OR TG SI SO CE)
                   MODIFY TRACE AND STOP OPTIONS FOR DEVICE ##.
                   ALL OPTIONS NOT DEFINED ARE DEACTIVATED.
Z ##,##-##,##      DEACTIVATE ALL OPTIONS FOR SPECIFIED DEVICES
C ##,##,##-##      COPY FROM FIRST DEFINED DEVICE TO OTHERS
B  ........#       DEFINE BUS VALUE FOR STOP ON EVENT
       . : BUS BITS 1=ON, O=OFF, X=DO NOT CARE
      # : 1=STOP F ANY BIT DIFFERENT, O=STOP IF ALL BITS EQUAL
T ##               DEFINE TAGBUS HEX VALUE FOR STOP ON EVENT
ENTER              EXIT FROM ROUTINE

D                  DISPLAY ACTUAL DEVICE SELECTION
H
```

3. This frame describes the options needed to select a specific device selection. To return to the device selection frame, enter D. The device selection frame returns and allows you to select the options.

   a. To trace one device, enter M XX.

      - XX is the address on bus out of the control interface.



   b. To trace all devices: Enter M 00, T, then C DO, 01-FF. This traces all devices and eliminates polling sequences.

How to Disable a Bus In Parity Stop

A bus in parity error may occur with some tag sequences. This is a normal condition, however it is suggested that the stop function be disabled when the Stop Conditions frame is displayed.

The channel monitor edit (CTLED) program checks the control interface.

1. Use the initialization procedure (see PDA 710) to select the control interface channel, edit and search program (PF5) or enter L CTLED, press the SYS FUNC key and then the Enter key.

   After the program is loaded, the following display appears:

```
        CONTROL INTERFACE MONITOR EDIT

  PF 1- SET DATA DISPLAY MODE AND OPTIONS
  PF 2- DISPLAY DESCRIPTOR RECORDS
  PF 3- SELECT A NEW TRACK, FILE OR EVENT NUMBER
  PF 4- HIGH LEVEL SEARCH              PF 5- BASIC SEARCH
  PF 6- DISPLAY NEXT EVENT FOUND BY THE SEARCH FACILITY
  PF 7- SCROLL UP                      PF 8- SCROLL DOWN
  PF10- SCROLL BACKWARD                PF11- SCROLL FORWARD
  PF 9- TAPE TABLE OF CONTENTS         PF12- END OF JOB
  PROB INIT- FILE SELECTION
  SERVC-LOC CTLED /0020/0002
  1I LOADING
  2I LOAD COMPLETE
  3I E00. FILE SELECTION
  4R E01. ENTER TRACK NUMBER (1,2,3)
  L CTLEDWAIT
```

   This frame describes the options available with the channel monitor edit program. Only the high-lighted options can be selected at this time. The message asks the user to select a track for display.

2. Enter a track number. The channel problem description appears with a message asking the user to select a stop number (00 through 99). The default stop number is 00.

3. Enter the stop number. The selected track is read again to find the requested stop number. When the stop number is found, a message asks the user to select an event from the displayed range. Press only the Enter key to display the event that caused the stop condition (entry + 0).

4. Enter the trace event. The tape data is loaded into the PT-2 buffer. The selected event and enough additional trace data to fill the screen are displayed in horizontal mode (see sample below).

```
CTL-1.EDIT   (TRACK 2 STOP00)
01 TAG       888   8888  88    8     008   8     88    88    0
       BUS   222   2222  23    4     A7A   F     FF    45    E
02  BUS      246   0246  06    F     8C0   0     80    00    7
       OUT   111   1111  10    F     000   4     33    00    2
03  BUS      00    0     8     6600  02    0000  000   002   00
       IN    00    0     0     4499  C0    0088  D33   880   00
04 TAG GATE  ----- ----- ----- ----- ----- ----- ----- ----- --
05 TAG VALID ----- ----- ----- ----- ----- ----- ----- ----- --
06 SEL HOLD  ----- ----- ----- ----- ----- ----- ----- ----- --
07 SEL ACT   ----- ----- ----- ----- ----- ----- ----- ----- --
08 SYNC IN   ----- ----- ----- ----- ----- ----- ----- ----- --
09 SYNC OUT  ----- ----- ----- ----- ----- ----- ----- ----- --
10 NORM END  ----- ----- ----- ----- ----- ----- ----- ----- --
11 CHECK END ----- ----- ----- ----- ----- ----- ----- ----- --
12 ERR ALERT ----- ----- ----- ----- ----- ----- ----- ----- --
13 EXT SYNC  ----- ----- ----- ----- ----- ----- ----- ----- --
14 IND ALERT ----- ----- ----- ----- ----- ----- ----- ----- --
15 RESPONSE  ----- ----- ----- ----- ----- ----- ----- ----- --
16 RECYCLE   ----- ----- ----- ----- ----- ----- ----- ----- --
             .     -40   .     -30   .     -20   .     -10   .
PRESS MENU KEY FOR HELP
```

5. The data can be scanned (scrolled) horizontally by use of the PF10 (left) or PF11 (right) keys. Additional recorded lines can be viewed by use of the PF8 (down) or PF7 (up) keys. Additional information about this display can be obtained from the Channel Monitor Operation Manual.

6. To change the display format to vertical mode, press the PF1 key. The following frame appears:

```
CTL-1
EDIT     DATA  DISPLAY
Horizontal Data Display Mode Is Now Active
Enter V To Select The Vertical Mode
    A       To Display The Data
    X #### To Modify The BKWD/FWD Scroll Value (NOW: 0020)
    Y ##    To Modify The Up/Down Scroll Value (NOW: 09)
    S ##,##..To Suppress The Display Of Lines Number ##,##...
    L ##,##..To Reactivate The Display Of Lines Numb.##,##..
    L All To Display All Lines
-4095                                                  WAIT
```

   a. Scrolling values and display options can be changed. Enter V to select vertical mode. The trace data is displayed as shown:

```
  CTL-1,EDIT  (TRACK 3 STOP00)

EVENT.T/B.TAG.BUS.BUS.BUS.TAG.TAG.SELECT.SYNC.NOR.CHK.ERR.IND.EX
 NUMB.PAR.BUS.PAR.OUT.IN. GAT.VAL.HLD.ACT.OUT.IN.END.END.ALERT.S

   -425  .   .   .  .08. *   *   *   *   .   .   .   *   .   .   .   .
   -424  .   .   .  .08. *   *   *   *   .   .   .   *   .   .   .   .
   -423  .07 .   .C0 .   .   *   .   *   *   .   .   .   .   .   .   .
   -422  .   .   .  .20. *   .   *   *   *   .   .   .   *   .   .   .
   -421  .0A .   .80 .   .   *   .   .   *   *   .   .   .   .   .   .
   -420  .   .   .  .0C. *   *   *   *   *   .   .   .   *   .   .   .
   -419  .06 .   .C0 .   .   *   .   .   *   *   .   .   .   .   .   .
   -418  .   .   .  .30. *   .   *   .   *   *   .   .   .   *   .   .
   -417  .8A .   .00 .   .   *   .   .   *   *   .   .   .   .   .   .
   -416  .   .   .  .00. *   .   *   .   *   *   .   .   .   *   .   .
   -415  .   .   .  .00 *   .   *   .   *   *   .   .   .   *   .   .
   -414  .8F .   .83 .   .   *   .   .   *   *   .   .   .   .   .   .
   -413  .   .   .  .0D. *   .   *   .   *   *   .   .   .   *   .   .
   -412  .04 .   .10 .   .   *   .   .   *   *   .   .   .   .   .   .
   -411  .   .   .  .80. *   *   *   .   *   *   .   .   .   *   .   .
   -410  .8F .   .01 .   .   *   .   .   *   *   .   .   .   .   .   .
   -409  .   .   .  .00. *   .   *   *   *   *   .   .   .   *   .   .
   -408  .   .   .  .00. *   .   *   *   *   *   .   .   .   *   .   .
   -407  .8F .   .05 .   .   *   .   .   *   *   .   .   .   .   .   .
   -406  .   .   .  .00. *   .   *   .   *   *   .   .   .   *   .   .

PRESS MENU KEY FOR HELP                                        WAIT
```

   b. The data can be scrolled vertically with the PF10 and PF11 keys.

7. Press the menu key to return the display to the list of available options. See the Channel Monitor Operation Manual for information on additional options.

Introduction to the Logic Analyzer

The Biomation Model 1650-D or Model K100-D logic analyzer can be used to monitor and record the sequences of up to 16 different inputs. The channel monitor (discussed on page PDA 710) records only the sequence of events, while the logic analyzer also shows the exact timing relationships of the monitored lines. The channel monitor is limited to NPL level inputs, but each probe of the logic analyzer has individual voltage threshold selection. The time base of the logic analyzer can be varied according to the type of sequence being monitored. When the logic analyzer is used with the PT-2, the recorded data can be analyzed at a remote location.

The procedure for using the logic analyzer is in the *Biomation Model 1650-D Logic Analyzer Operating and Service* manual or the *Biomation Model K100-D Logic Analyzer Operating and Service* manual.

Displaying a PT-2 to Logic Analyzer Tape Record

1. Display the tape record (PF4 key).

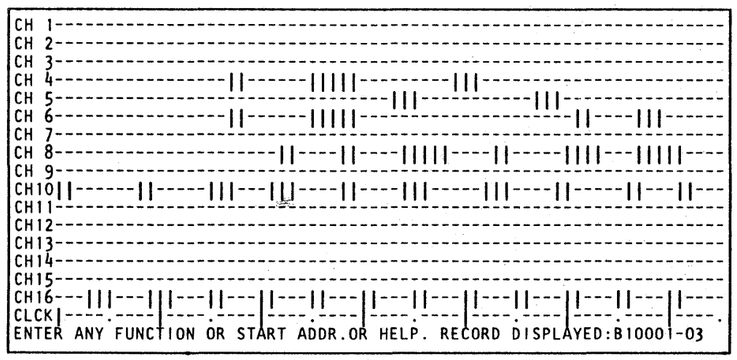
2. Enter the file name, B10XXX, or press the Enter key to get the first record. The descriptor record is displayed as follows:

   B10001&REC.00

3. Enter Y to view the first record.

   To display another record, enter B10XXX and record XX when requested. A maximum of 99 files can be recorded (01 to 99). Each file can have a maximum of 100 records (00 to 99). However, since the PT-2 is not capable of displaying all 512 bits of information in the trace, amplify the display by entering an A. A smaller portion of the trace is displayed, starting at the beginning. Enter a 3-digit number to go directly to offset from beginning.

   A sample trace is displayed below. The verticals line represent positive levels; horizontal lines represent negative levels.



Contents

Contents Of This Section

References To Other Sections

See the SENSE section of this manual for sense bytes and format information.

Bibliography

The following documentation can aid in understanding or repairing the 3880.

- *IBM 3880 Storage Control Description*, GA26-1661
- Divider tabs for *IBM 3880 Storage Control Description*, GX26-1663
- *DASD Functional Unit and Installation Activity Document Code Guide*, Z229-5113
- *IBM Quality Service Technical Activity Reporting Guide*, Z150-0343
- *IBM 3880 Parts Catalog*, S127-0950
- *3350 Reference Manual*, GA26-1638
- *3350 Maintenance Library*, (see note)
- *Introduction to DASD*, GC20-1649

Note: IBM internal: Pages of these manuals can be ordered from the San Jose plant by using the Wiring Diagram/Logic Page Request, Z150-0130 (U/M 015).

Non-IBM: Requests for copies of IBM publications should be made to your IBM representative or to the IBM branch office serving your location.

Storage Directors – External Register Summary

REGISTER NAME (MNEMONIC)		BIT NUMBER OR NAME 0	1	2	3	4	5	6	7	REGISTER ADDRESS	* TYPE	SENSE REFERENCE FORMAT	SENSE REFERENCE BYTE NUMBER	MSM PAGE	CARD	LRM PAGE
Buffer ALU Pointer Register (BAP)	(BAH)	32768	16384	8192	4096	2048	1024	512	256	'02'#	R/W	—	—	REF 65	DXA	HJ200
	(BAL)	128	64	32	16	8	4	2	1	'02'#	R/W	—	—	REF 65	DXA	HJ200
Buffer Increment BAP Register	(BFI)	0	1	2	3	4	5	6	7	'05'	R/W	—	—	REF 65	DXD	HK200
Buffer Register	(BFR)	0	1	2	3	4	5	6	7	'04'##	R/W	—	—	REF 65	DXD	HK200
Channel Bus In Register	(CBI)	0	1	2	3	4	5	6	7	'06'**	R/W	3	19	SENSE 160	CSR	HH220
Channel Bus Out Register	(CBO)	0	1	2	3	4	5	6	7	'06'**	R	3	18	SENSE 160	CDX	HG210
Channel Buffer Pointer Register (CBP)	(CBH)	32768	16384	8192	4096	2048	1024	512	256	'00'###	R/W	—	—	REF 65	DXA	HJ200
	(CBL)	128	64	32	16	8	4	2	1	'00'###	R/W	—	—	REF 65	DXA	HJ200
Channel Counter High Register	(CCH)	32768	16384	8192	4096	2048	1024	512	256	'12'	W	—	—	REF 65	CSR	HH220
Channel Counter Low Register	(CCL)	128	64	32	16	8	4	2	1	'13'	W	—	—	REF 65	CSR	HH220
Channel Control 1 Register	(CC1)	Operational In	Address In	Status In	Long Select	Control Unit Busy	Condition Register 17 Select Bit 4	Condition Register 17 Select Bit 2	Condition Register 17 Select Bit 1	'17'	R/W	3	13	SENSE 150	CSC	HF200
Channel Control 2 Register	(CC2)	Force Propagate Select Out	Read Address Switch	Not Used	Not Used	Channel Switch Locked	Channel Sel Bit 4 (Four-Chan Additional)	Channel Sel Bit 2 (Two-Chan Additional)	Channel Select Bit 1	'10'	R/W	3 2	14 12	SENSE 150	CSC	HF200
Buffer Increment CBP Register	(CFI)	0	1	2	3	4	5	6	7	'04'##	R/W	—	—	REF 65	DXD	HK200
Check Register	(CHK)	Data Xfer Addressing (DXA) Card Check	Device Counter (DCT) Card Check	Channel Search (CSR) Card Check	Channel Data Check	Array Out Parity Check	Sense Register Check	Data Transfer (DXD) Card Check	Port Connection ADT Buffer Check	'13'***	R	2 3	10 10	SENSE 70	DXA	HJ200

*R = Read Only
W = Write Only
R/W = Read or Write

**Addressing these registers also depends on the status of bit 3 of the channel transfer control register.

CXC bit 3 = 1 - CBI
CXC bit 3 = 0 - CBO

***Addressing this register also depends on the status of bits 0 and 3 of the data transfer control (DXC) register.

DXC bits 0,3 = 10 - CHK

#Whether the high (BAH) or low (BAL) bytes of this buffer pointer is addressed depends on the status of the associated BAP toggle (TFR bit 2).

	BAH	BAL
BAP toggle	1	0

##Addressing these registers also depends on the status of bit 5 of the data transfer control (DXC) register.

DXC bit 5 = 0 - BFR
DXC bit 5 = 1 - CFI

###Addressing the high (CBH) or low (CBL) bytes of this register also depends on the status of the CBP toggle (TFR bit 0) and bit 7 of the channel data transfer control (CXC) register.

	CBH	CBL	CRC
CBP toggle	1	0	x
CXC (7)	0	0	1

REGISTER NAME (MNEMONIC)	BIT NUMBER OR NAME								REGISTER ADDRESS	* TYPE	SENSE REFERENCE		MSM PAGE	CARD	LRM PAGE
	0	1	2	3	4	5	6	7			FORMAT	BYTE NUMBER			
Channel (CRC) Redundancy Check Register	0	1	2	3	4	5	6	7	'00'***	R	—	—	REF 65	DXD	HK200
Channel Interface (CR0) Checks Register	Channel Bus In (CBI) Parity Check	Channel Interface (CIF) Card Check	Channel Data Transfer (CDX) Cd Ck	Channel Search (CSR) Card Check 1	Channel Clock Check A - D	Channel Clock Check E - H	Not Used	Not Used	'11'**	R/W	3	11	SENSE 140	CSC	HF200
Condition Register 1 (CR1)	Allow Disable Channel A	Allow Disable Channel B	Allow Disable Channel C	Allow Disable Channel D	Allow Disable Channel E	Allow Disable Channel F	Allow Disable Channel G	Allow Disable Channel H	'11'**	R/W	—	—	REF 65	TCR TACR	HC200 HE200
Condition Register 2 (CR2)	Unsuppress-ible Request In Channel A	Unsuppress-ible Request In Channel B	Unsuppress-ible Request In Channel C	Unsuppress-ible Request In Channel D	Unsuppress-ible Request In Channel E	Unsuppress-ible Request In Channel F	Unsuppress-ible Request In Channel G	Unsuppress-ible Request In Channel H	'11'**	R/W	—	—	REF 65	TCR TACR	HC200 HE200
Condition Register 3 (CR3)	Control Unit End Channel A	Control Unit End Channel B	Control Unit End Channel C	Control Unit End Channel D	Control Unit End Channel E	Control Unit End Channel F	Control Unit End Channel G	Control Unit End Channel H	'11'**	R/W	—	—	REF 65	TCR TACR	HC200 HE200
Condition Register 6 (CR6)	Suppress-ible Request In Channel A	Suppress-ible Request In Channel B	Suppress-ible Request In Channel C	Suppress-ible Request In Channel D	Suppress-ible Request In Channel E	Suppress-ible Request In Channel F	Suppress-ible Request In Channel G	Suppress-ible Request In Channel H	'11'**	R/W	—	—	REF 65	TCR TACR	HC200 HE200

*R = Read Only
W = Write Only
R/W = Read or Write

**Addressing these registers also depends on the status of bit 5 through 7 of the channel control 1 (CC1) register.

CC1 Reg Bit			Select Register
5	6	7	
0	0	0	CR0
0	0	1	CR1
0	1	0	CR2
0	1	1	CR3
1	1	0	CR6

***Addressing this register also depends on the status of bit 7 (Run Channel) of the CXC register.

REGISTER NAME (MNEMONIC)	BIT NUMBER OR NAME								REGISTER ADDRESS	* TYPE	SENSE REFERENCE		MSM PAGE	CARD	LRM PAGE
	0	1	2	3	4	5	6	7			FORMAT	BYTE NUMBER			
Channel Status 1 (CS1)	Service Out	Address Out	Command Out	Not Used	Select Out Trapped	Status In Tag	Data Out	Suppress Out	'14'	R	3	15	SENSE 152	CSC	HF200
Channel Status 2 (CS2)	Halt I/O	Selective Reset	System Reset	Two-Channel Additional Conditional Register (TACR) Card Check	Channel Sequence Control (CSC) Card Check	Channel Bus Out (CBO) Parity Check	Two-Channel Condition Register (TCR) Card Check	Channel Check 1	'15'	R	2 3	18 12	SENSE 95 SENSE 145	CSC	HF200
Channel Status 3 (CS3)	Command Chain Complete	Command Chain Aborted	Chained Initial Status	Activate Chain Reselect	Not Used	Trace Ctl 0 (Single Device)	Trace Ctl 1 (Block Trace)	Trace Ctl 2 (Channel Trace)	'16'	R/W	3	16	SENSE 155	CSC	HF200
Channel Transfer Control (CXC)	SD Service In	Search High	Search Equal	Read Chan Bus In (CBI) Reg	Set Speed Control Register	Allow Run Channel	Data Transf (DXR) From Channel	Run Channel	'07'	R/W	2 3	11 17	SENSE 75 SENSE 155	CSR	HH220
Device Bus In (DBI)	0	1	2	3	4	5	6	7	'08'	R	2	14	SENSE 80	DDCU	HX200
Device Bus Out (DBO)	0	1	2	3	4	5	6	7	'09'	R/W	2	13	SENSE 80	DDCU	HX210
Device Buffer Pointer (DBP) Register (DBH)	32768	16384	8192	4096	2048	1024	512	256	'01'**	R/W	—	—	REF 65	DXA	HJ200
(DBL)	128	64	32	16	8	4	2	1	'01'**	R/W	—	—	REF 65	DXA	HJ200
Device Count High (DCH)	32768	16384	8192	4096	2048	1024	512	256	'0A'	R/W	—	—	REF 65	DCT	HV200
Device Count Low (DCL)	128	64	32	16	8	4	2	1	'0B'	R/W	—	—	REF 65	DCT	HV200
Device Cyclic Redundancy Check (DRC)	0	1	2	3	4	5	6	7	'01'***	R	—	—	REF 65	DXD	HK200
Device Tag Gate FOR 3380s (DTG)	One Byte Device	Block Diagnostic Set	Diagnostic Sync In	Inhibit Bus Out Parity	Not Used	Control Interface Ctl Bit 0	Control Interface Ctl Bit 1	Run Device	'0C'	R/W	2	16	SENSE 85	DDCV	HX210
Device Channel Interface (DCI) FOR 3350s	Select Hold	Tag Gate	Response Gate	Reset Index Latch	Inhibit First Decrement	Control Interface Ctl Bit 0	Control Interface Ctl Bit 1	Run Device	'0C'	R/W	2	16	SENSE 85	DDCV	HX210

*R = Read Only
W = Write Only
R/W = Read or Write

**Whether the high (DBH) or low (DBL) byte of the device buffer pointer (DBP) is addressed depends on the status of the DBP toggle tag gate (DTG) register bit 7.

	DBH	DBL	DRC
DBP toggle	1	0	x
DTG (7)	0	0	1

***Addressing this register also requires that bit 7 (Run Device) of the device tag gate (DTG) register be set to a 1.

REGISTER NAME (MNEMONIC)	BIT NUMBER OR NAME								REGISTER ADDRESS	* TYPE	SENSE REFERENCE		MSM PAGE	CARD	LRM PAGE
	0	1	2	3	4	5	6	7			FORMAT	BYTE NUMBER			
Device Channel Interface Register (DCI) FOR 3380s	Connection Check Alert	Tag In Sequence Check	End Op. Not command Gate	Not Used	Null Disconnect	Valid/ Sync In	Selected Null	End Operation	'0D'	R	2	17	SENSE 90	DDCV	HX200
Device Tag In (DTI) Register FOR 3350s	Select Active	Tag Valid	Check End	CE Alert	Normal End	Device Alert	Index Latch	Error Alert	'0D'	R	2	17	SENSE 90	DDCV	HX200
Device Channel Interface Register (DCI) FOR 3380s	Device Tag Out Bit 0	Device Tag Out Bit 1	Device Tag Out Bit 2	Not Used	Not Used	Not Used	Not Used	Not Used	'0E'	R/W	2	15	SENSE 80	DDCV	HX210
Device Tag Out (DTO) Register FOR 3350s	Device Tag Out Bit 0	Diag Sync In	Maintain DTO Parity	Not Used	DTO Bit 4	DTO Bit 5	DTO Bit 6	DTO Bit 7	'0E'	R/W	2	15	SENSE 80	DDCV	HX210
Data Transfer (DXC) Control	Status Reg Select 0	Not Used	Reset EODIR	Status Reg Select 1	EOP/DEOT Interrupt	CFI Select	Suspend DRC	Initialize Negative Data	'03'	R/W	—	—	REF 70	DXA	HJ200
External Bus In (EBI) Register	0	1	2	3	4	5	6	7	'1E'	R	—	—	REF 70	MNT	HR200
External Bus Out (EBO) Register	0	1	2	3	4	5	6	7	'1E'	W	—	—	REF 70	MNT	HR200
Interrupt Level (ILR) Register	New Level 0	New Level 1	New Level 2	Last Level Bit 0	Last Level Bit 1	Allow Level 0	Allow Level 1	Allow Level 2	'1C'	R/W	—	—	REF 70	MNT	HR200
Initial Microcode (IML) Load Register	Not Diskette Drive Data	Not Diskette Drive Index	Diskette Drive Head Engage	Microcode Detected Check 1	Diskette Drive Request	Control Storage Data Check	Switch Decode 1 (Read Only)	Switch Decode 2 (Read Only)	'1D'	R/W	—	—	REF 70	MNT	HR200
Internal Register (IRG) Group Register	Primary Reg Group Pointer Bit 8	Primary Reg Group Pointer Bit 4	Primary Reg Group Pointer Bit 2	Primary Reg Group Pointer Bit 1	Secondary Reg Group Pointer Bit 8	Secondary Reg Group Pointer Bit 4	Secondary Reg Group Pointer Bit 2	Secondary Reg Group Pointer Bit 1	'1F'	R/W	—	—	REF 70	SDM	HQ200
Maintenance (MCR) Control Register	Error Alert Response	Validate Data Out	Confirm Out	Invalid Command Out	IML Micro-code Detected Ck	Command Valid Out	Inhibit Control Store Ck 1	Check Reset	'18'	W	—	—	REF 70	MNT	HQ200

*R = Read Only
W = Write Only
R/W = Read or Write

REGISTER NAME (MNEMONIC)	BIT NUMBER OR NAME								REGISTER ADDRESS	* TYPE	SENSE REFERENCE		MSM PAGE	CARD	LRM PAGE
	0	1	2	3	4	5	6	7			FORMAT	BYTE NUMBER			
Maintenance Control/Sense Register (MCS)	Enable Timer	Read-Only Storage (ROS) Select	Enable Reset CRC	Not Used	Throttle	Wait	Process	Status Pending	'1A'	R/W	—	—	REF 75	DCT	HV200
Maintenance Sense Register (MSR)	External Bus In (EBI) Parity Ck	Error Alert In	Data Received In	Confirm In	Command Valid In	Diagnostic Mode	Diskette Drive Select	Diskette Drive Busy	'18'	R	—	—	REF 75	MNT	HR200
Pad Counter Register (PCR)	128	64	32	16	8	4	2	1	'01' '0D'#	R W	—	—	REF	DCT	HV200
Storage Director Identification Register (SDI)	128	64	32	16	8	4	2	1	'12'	R	2 3	21 21	SENSE 100 SENSE 120 SENSE 160	DCT	HV200
Channel Speed Control Register (SPC)	Not Used	Channel Speed Control	Channel Speed Control	Channel Speed Control	ALWAYS ON	Not Used	Channel Speed Control	Channel Speed Control	'07'**	W	—	—	REF 75	CDX	HG210
Toggle, FRU Register (TFR)	CBP Toggle	DBP Toggle	BAP Toggle	FRU Address Bit 1	High Speed Chnl Active	Not Used	BC1 Full	BC2 Empty	'13'***	R	2	19	SENSE 100	DXA	HJ200
Transfer Complete Status Register (XCS)	Check 2	DBH=CBH	Director to Device Controller (DDC) End-of-Transfer	Read Data Check	Channel Data Transfer (CDX) End-of-Transfer	Compare Successful	First Sync In Latch	Channel Truncation	'13'***	R	2	8	SENSE 60	DXA	HJ200
Transfer Error Status Register (XES)	Device Overrun	Channel Overrun	CTL-I Interface Check	Clock (CLK) Check 2	Director to Device Controller (DDC) Cd Ck	DDC Sync In Check	Channel Buffer Check	Device Buffer Check	'13'***	R	2 3	9 9	SENSE 65 SENSE 130	DXA	HJ200

*R = Read Only
W = Write Only
R/W = Read or Write

**Addressing these registers also depends on the status of bit 4 in the channel transfer control (CXC) register.
CXC bit 4 = 1 - SPC

***Addressing these registers also depends on the status of bits 0 and 3 of the data transfer control (DXC) register.

DXC Bits		Select Register
0	3	
0	0	XCS
0	1	XES
1	1	TFR
1	0	CHK

#Addressing this register for a read operation also requires that bit 7 of the device tag gate (DTG) register and bit 1 of the transfer FRU (TFR) register be set to a 1.

Subsystem Storage – External Register Summary

Note: The subsystem storage external and indirect registers are in addition to the base 3350 or 3380 external and indirect registers.

External Registers

External registers X'1B' and X'0F' are used to address the registers in the subsystem storage control board. All subsystem storage registers are addressed indirectly by register X'1B'. These subsystem storage registers are named indirect registers. All data is transferred to and from the indirect registers through the X'0F' register. See REF 40 for a summary of the indirect registers.

REGISTER NAME (MNEMONIC)		BIT NUMBER OR NAME								MSM PAGE	CARD	LRM PAGE
		0	1	2	3	4	5	6	7			
Register X'1B'	(WRB) (write)	128	64	32	16	8	4	2	1	REF 95	CMCD	HN200
Register X'1B'	(RDB) (read)	Data that was last set into register X'1B'									CMCD	HN200
Register X'0F'	(WRF) (write)	Data destined for the communication buffer or indirect registers									CMCD	HN200
Register X'0F'	(RDF) (read)	Data from an indirect register or the communication buffer									CMCD	HN200

X'1B' Register

The setting of the X'1B' register is controlled by the microcode. The X'1B' register, when used as a write register, addresses indirectly the subsystem storage indirect registers. When the X'1B' register is used as a read register, it is used to read the contents of the X'1B' register for diagnostic purposes. The X'1B' Shadow (CWRBS) register is the backup register for the X'1B' register.

Write (WRB)

Bit 0 defines whether bits 1-7 address a register to be read or address a register to be written. Bit 0, when one, defines the register to be written except for special operation codes (see REF 95).

The address part of register X'1B' (bits 1-7) is increased for each write to the X'0F' register except when writing or reading the communication buffer. Addressing a register that is not present will cause an error.

Read (RDB)

Bit 0, when zero, defines the register to be read. Data bits 0-7 read from this register was placed last into register X'1B' or its increased value after the X'0F' register has been written. The address part of X'1B' (bits 1-7) is not increased when reading register X'0F' (RDF). Addressing a register that is not present will cause an error. Correct parity is generated for the ALU In Bus when this register is read.

X'0F' Register

The X'0F' register is a data buffer between the subsystem storage indirect registers and the ALU, and the subsystem storage communication buffer and the ALU.

Write (WRF)

The destination of WRF data relies on the setting of register X'1B'. WRF is used for sending data to the communication buffer or to an indirect register. Each writing of register X'0F' will cause the address part of register X'1B' to be increased (except when using the communication buffer).

Read (RDF)

The contents of RDF relies on the setting of register X'1B'. The data that is placed into register X'0F' is loaded from the indirect register defined by register X'1B'. Correct parity is generated for the ALU In Bus when this register is read.

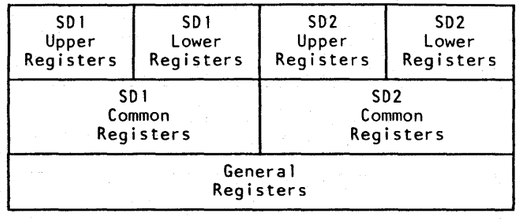
Subsystem Storage – External Register Summary REF 35

Subsystem Storage – Indirect Register Summary

Note: The subsystem storage external and indirect registers are in addition to the base 3350 or 3380 external and indirect registers.

The subsystem storage indirect registers are divided into the following:

- Upper registers
- Lower registers
- Common registers
- General registers



Mnemonic Description

```
Register Mnemonic
-----------------

X YYYYYY
|  |
|  |_____ Register Abbreviation
|
|________ U  Upper Registers
          L  Lowers Registers
          C  Common Registers
          G  General Registers
          A  Auxiliary Storage Director Microprocessor Registers
```

Subsystem Storage – Indirect Register Summary (Cont.)

General Registers

There is one set of registers for both storage directors. These registers are the same whether being addressed from storage director 1 or storage director 2.

REGISTER NAME (MNEMONIC)	BIT NUMBER OR NAME								REGISTER ADDRESS	* TYPE	SENSE REFERENCE			MSM PAGE	CARD	LRM PAGE
											SENSE BYTE		BYTE NUMBER			
	0	1	2	3	4	5	6	7			7**	8***				
General Diagnostic (GDI)	Force Data/Ref Cmd Check	Test Loop W/R ECC	Test Loop W/R Storage	Force DR-A Clock Check	Force DR-B Clock Check	Force SC Clock Check	Force SC Select Check	Force Test/Set Check	'E2' '62'	W R	—	——	——	REF 80	CMC1	JP200
ECC Diagnostic (GECCDI)	Degate Decodes	ECC Force Bit 1	ECC Force Bit 2	ECC Force Bit 3	Invert ROS-M Parity	SD1 Write/Hold Check Byte	SD2 Write/Hold Check Byte	Inhibit DD/Stg Data Out Ck	'E3' '63'	W R	—	——	——	REF 80	CME3	JL200
ECC Check 1 (GECCCK1)	ECC Check Bit 0	ECC Check Bit 1	ECC Check Bit 2	ECC Check Bit 3	ECC Check Bit 4	ECC Check Bit 5	ECC Check Bit 6	ECC Check Bit 7	'6B'	R	F2	1x/2x/3x 4x/5x/Fx	20	REF 80	CME3	JL200
ECC Check 2 (GECCCK2)	ECC Check Bit 0	ECC Check Bit 1	ECC Check Bit 2	ECC Check Bit 3	ECC Check Bit 4	ECC Check Bit 5	ECC Check Bit 6	ECC Check Bit 7	'6C'	R	—	——	——	REF 80	CME3	JL200
ID Switches (GIDSW)	ID Switch 128	ID Switch 64	ID Switch 32	ID Switch 16	ID Switch 8	ID Switch 4	ID Switch 2	ID Switch 1	'69'	R	F2	5x/Fx	12	REF 80	CMC1	JP200
Microcode Register (GMIC)	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	'E1' '61'	W R	F8	——	15	SENSE 247	CMC1	JP200
Storage Size/Cables Out (GSSCIN)	Storage Board 1 Cables Out	Storage Board 2 Cables Out	SD1 Diagnostic Mode	SD2 Diagnostic Mode	64M Byte Switch	32M Byte Switch	16M Byte Switch	8M Byte Switch	'68'	R	F2	5x	12	SENSE 227	CMC1	JP200
ECC Syndrome 1 (GSYN1)	Inverted ECC Syndrome Bit 0	Inverted ECC Syndrome Bit 1	Inverted ECC Syndrome Bit 2	Inverted ECC Syndrome Bit 3	Inverted ECC Syndrome Bit 4	Inverted ECC Syndrome Bit 5	Inverted ECC Syndrome Bit 6	Inverted ECC Syndrome Bit 7	'6D'	R	—	——	——	REF 80	CME3	JL200
ECC Syndrome 2 (GSYN2)	Inverted ECC Syndrome Bit 0	Inverted ECC Syndrome Bit 1	Inverted ECC Syndrome Bit 2	Inverted ECC Syndrome Bit 3	Inverted ECC Syndrome Bit 4	Inverted ECC Syndrome Bit 5	Inverted ECC Syndrome Bit 6	Inverted ECC Syndrome Bit 7	'6E'	R	—	——	——	REF 80	CME3	JL200
Test and Set (GTS)	Test and Set Being Used	SD1 Ownership	SD2 Ownership	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	'E0' '60'	W R	F2	Fx	17	SENSE 233	CMC1	JP200
Write Check 1 (GWRCK1)	Write Check Bit 0	Write Check Bit 1	Write Check Bit 2	Write Check Bit 3	Write Check Bit 4	Write Check Bit 5	Write Check Bit 6	Write Check Bit 7	'E4' '64'	W R	—	——	——	REF 80	CME3	JL200
Write Check 2 (GWRCK2)	Write Check Bit 0	Write Check Bit 1	Write Check Bit 2	Write Check Bit 3	Write Check Bit 4	Write Check Bit 5	Write Check Bit 6	Write Check Bit 7	'E5' '65'	W R	—	——	——	REF 80	CME3	JL200

*R = Read Only
W = Write Only
R/W = Read or Write

**Sense Byte 7 =

Bits	
0-3	4-7
Format ID	Message ID

***Sense Byte 8 =

Bits	
0-3	4-7
Error Type	Operation Type (x)

Subsystem Storage – Indirect Register Summary (Cont.) REF 45

Common Registers

Common registers are registers that are common to both upper and lower data ports of each storage director. They are also used with the data controls of the storage directors. Each storage director has its own set of common registers.

REGISTER NAME (MNEMONIC)	BIT NUMBER OR NAME 0	1	2	3	4	5	6	7	REGISTER ADDRESS	* TYPE	SENSE REFERENCE SENSE BYTE 7**	SENSE BYTE 8***	BYTE NUMBER	MSM PAGE	CARD	LRM PAGE
ADT/ASDM Check (CAAJCK)	ADT/ASDM IR Check	ASDM LS Ext Reg Addr Parity Check	ASDM Internal Check	ADT Buffer ASDM CS In Parity Check	AA Duplicate IR Addr Decode Ck	Not Used	ASDM CS Addr Parity Check	CAR Check	'58'	R	F2	1x	17	SENSE 208	CMAA	HL200
ASDM Control (CACTL) (ACTL)	Execute ASDM	Run ASDM Mode	Not Used	ASDM Reset	Not Used	Not Used	Interrupt Request	Interrupt Level	'C5' '45' '01'	W R R	—	—	—	REF 85	CMAA	HL200
ASDM Read Register 1 (CARD1) (ARD1)	These bits are defined and controlled by the microcode								'C6' '46' '02'	W R R	—	—	—	REF 85	CMAA	HL200
ASDM Read Register 2 (CARD2) (ARD2)	These bits are defined and controlled by the microcode								'C7' '47' '10'	W R R	—	—	—	REF 85	CMAA	HL200
ASDM Write Register 1 (CAWR1) (AWR1)	These bits are defined and controlled by the microcode								'56' '04' '04'	R W R	—	—	—	REF 85	CMAA	HL200
ASDM Write Register 2 (CAWR2) (AWR2)	These bits are defined and controlled by the microcode								'57' '08' '08'	R W R	—	—	—	REF 85	CMAA	HL200
Communication Adapter Check (CCOMACK)	Communication Adapter IR Check	Not Used	Not Used	Not Used	CA Duplicate IR Addr Decode Ck	Port Control IR Parity Check	Port Control IR Read Parity Ck	SD Indicator Check	'5A'	R	F2	1x	12	SENSE 206	CMCA	HM200
Communication Adapter Diagnostic (CCOMADI)	Force This SD Request Honored	Not Used	Not Used	CA Force Bit 3	CA Force Bit 4	CA Force Bit 5	CA Force Bit 6	CA Force Bit 7	'C3' '43'	W R	—	—	—	REF 85	CMCA	HM200
Communication Address (CCOMADR)	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	'C1' '41'	W R	F2	4x	11	REF 90	CMCA	HM200
Communication Control (CCOMCTL)	Communication Request	Communication Check Reset	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	'C2' '42'	W R	F2	4x	12	SENSE 222	CMCA	HM200
Common Control (CCTL)	Not Used	Not Used	Controlled Machine Reset	Not Used	Common Check Reset	Cause Device Gap Interrupt	Not Used	Not Used	'40'	R	F2	1x/Fx	11 16	SENSE 206 & 233	CMCA	HM200
Common Control Shadow (CCTLS)	Not Used	Not Used	Controlled Machine Reset	Not Used	Common Check Reset	Cause Device Interrupt	Not Used	Not Used	'54'	R	—	—	—	REF 90	CMC1	JP200

*R = Read Only
W = Write Only
R/W = Read or Write

**Sense Byte 7 = Bits 0-3 - Format ID
4-7 - Message ID

***Sense Byte 8 = Bits 0-3 - Error Type
4-7 - x = Operation Type

Common Registers (Continued)

REGISTER NAME (MNEMONIC)	BIT NUMBER OR NAME 0	1	2	3	4	5	6	7	REGISTER ADDRESS	* TYPE	SENSE REFERENCE SENSE BYTE 7**	8***	BYTE NUMBER	MSM PAGE	CARD	LRM PAGE
Multiple IR Address Decode (CMADEC)	Upper Port Buffer IR Decoded	Lower Port Buffer IR Decoded	ECC IR Decoded	Storage Adapter IR Decoded	Storage Control IR Decoded	SD IR Decoded	Not Used	Not Used	'55'	R	F2	1x	14	SENSE 207	CMSA	JS200
Common Port Adapter Check 1 (CPACK1)	Port Adapter IR Check	SDM ALU Out Parity Check	Ext Reg Addr or Decode Ck	Ext Reg Selection Check	IR Data In/Out Parity Ck	Read Clock Delay Check	ALU Out Control Check	Ext Reg Read Parity Check	'5C'	R	F2	1x	15	SENSE 207	CMCD	HM200
Common Port Adapter Check 2 (CPACK2)	Not Used	Not Used	Not Used	Not Used	Clock Check	CD Duplicate IR Addr Decode Ck	Not Used	Range Select Check	'5D'	R	F2	1x	16	SENSE 208	CMCD	HM200
Common Storage Address Check (CSACK)	Test and Set Check	Address Decode Check	Upper Port Buffer IR Check	Not Used	Lower Port Buffer IR Check	ECC IR Check	Storage Adapter IR Check	Storage Control IR Check	'5B'	R	F2	1x	13	SENSE 207	CMSA	JS200
Storage Address Diagnostic (CSADI)	DA Force Bit 0	DA Force Bit 1	DA Force Bit 2	DA Force Bit 3	Clamp Addr Incr Predict Pty	Force Storage Addr Decode	Force Storage Ctl Decode	Continue on Error	'C4' '44'	W R	—	——	——	REF 90	CMSA	JS200
Common Storage Address Refresh Check (CSARCK)	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Ref Address Increment	DA Ref Address Ck	'5F'	R	F2	4x	16	SENSE 223	CMSA	JS200
Common Storage Control Check (CSCCK)	SC Clock Check	SC Select Check	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	'13'	R	F2	1x	14	SENSE 222	CMC1	JP200
Common Storage Card Refresh Address Check (CSCRACK)	Stg Card Ref Addr Ck -BCHJ-	Stg Card Ref Addr Ck -DEFG-	Stg Card Ref Addr Ck -MNTU-	Stg Card Ref Addr Ck -PQRS-	AR Card Ref Addr Ck -K-	AR Card Ref Addr Ck -L-	Stg Board 1 Ref Active	Stg Board 2 Ref Active	'5E'	R	F2	1x	15	SENSE 222	CMC1	JP200
Common Status 1 (CSTAT1)	Upper Port Check	Lower Port Check	Test and Set Obtained	Common Check	Upper Port Operation Complete	Lower Port Operation Complete	Upper Port Data Tsfr Complete	Lower Port Data Tsfr Complete	'50'	R	F2	1x/2x/3x 4x/5x/Fx	9	SENSE 206	CMSA	JS200
Common Status 2 (CSTAT2)	Upper Port Double Bit Correction	Upper Port Single Bit Correction	Lower Port Double Bit Correction	Lower Port Single Bit Correction	Not Used	Microcode Reg Bit Active	Not Used	Not Used	'51'	R	F2	1x/2x/4x 5x/Fx	10	SENSE 206	CMC1	JP200
Common Status 3 (CSTAT3)	Message Waiting	Msg Waiting Echo Back To Sender	Request Honored	Active Inhibit SD Reset	Communication Check	Port Adapter/ Control Cables Out	Communication Cable Out	Other SD Power Off	'52'	R	F2	4x 5x/Fx	13 11	SENSE 222	CMCA	HM200
Common Status 4 (CSTAT4)	Not Used	SD1 Indicator	SD2 Indicator	Not Used	Timer Overflow	Stg Ctl Bd Power Off	Stg Board 1 Power Off	Stg Board 2 Power Off	'4F'	R	—	——	——	REF 90	CMCA	HM200
1B Shadow (CWRBS)	1B Shadow Bit 0	1B Shadow Bit 1	1B Shadow Bit 2	1B Shadow Bit 3	1B Shadow Bit 4	1B Shadow Bit 5	Check Bit 6	6-15 Check Bit 7	'53'	R	—	1x	16	REF 90	CMCD	HN200
Common Status 5 (CSTAT5)	Not used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Expanded Storage Installed	'4E'	R	—	——	——	REF 90	CMCD	HN200

*R = Read Only
W = Write Only
R/W = Read or Write

**Sense Byte 7 = Bits 0-3 - Format ID
4-7 - Message ID

***Sense Byte 8 = Bits 0-3 - Error Type
4-7 - x = Operation Type

Upper/Lower Port Registers

REGISTER NAME	MNEMONIC PORT UPPER	MNEMONIC PORT LOWER	BIT NUMBER OR NAME 0	1	2	3	4	5	6	7	REGISTER ADDRESS UPPER	REGISTER ADDRESS LOWER	* TYPE	SENSE REFERENCE SENSE BYTE 7**	SENSE REFERENCE SENSE BYTE 8***	SENSE REFERENCE BYTE NUMBER	MSM PAGE	CARD	LRM PAGE
Control	UCTL	LCTL	Storage Run	Check Reset	Invert Ch/Dev Run	Invert Ch/ Dev ADT Direction	Not Used	Not Used	Not Used	Not Used	'86' '06'	'A6' '26'	W R	F2	Fx	15	REF 100	CMCD	HN200
Control Shadow	UCTLS	LCTLS	Storage Run	Check Reset	Invert Ch/ Dev Run	Inv Ch/Dev ADT Dir	Not Used	Not Used	Not Used	Not Used	'86' '09'	'A6' '29'	W R	—	——	——	REF 100	CMSA	JS200
Byte Count High (See Note)	UCTRH	LCTRH	Byte Count 32768	Byte Count 16384	Byte Count 8192	Byte Count 4096	Byte Count 2048	Byte Count 1024	Byte Count 512	Byte Count 256	'84' '04'	'A4' '24'	W R	—	——	——	REF 100	CMPB	JD200
Byte Count Low (See Note)	UCTRL	LCTRL	Byte Count 128	Byte Count 64	Byte Count 32	Byte Count 16	Byte Count 8	Byte Count 4	Byte Count 2	Byte Count 1	'85' '05'	'A5' '25'	W R	F2	2x	14	REF 100	CMPB	JS200
ECC Check	UECCCK	LECCCK	ECC Uncorrect-able Check	PB/ECC Data In Check 1	PB/ECC Data In Check 2	ECC Data In or ROS Check E1	ECC Data In or ROS Check E2	ROS-M Check	E1/DD/Stg Data Out Parity Ck	E2/DD/Stg Data Out Parity Ck	'12'	'32'	R	F2	3x	10	REF 100	CME3	JL200
OP/CTL	UOPCTL	LOPCTL	Fetch (0) or Store Op (1)	Inhibit SSAR Increment	Manual (0) or Auto (1) Stg Mode	Not Used	Inhibit SRC	Accumulate SRC	Not Used	Not Used	'83' '03'	'A3' '23'	W R	F2	Fx	14	REF 100	CMCD	HN200
OP/CTL Shadow	UOPCTLS	LOPCTLS	Fetch or Store Op	Inhibit SSAR Incr	Manual/Auto Stg Mode	Not Used	Inhibit SRC	Accumulate SRC	Not Used	Not Used	'83' '08'	'A3' '28'	W R	—	——	——	REF 100	CMSA	JS200
Port Adapter Check	UPACK	LPACK	DXR/PA Parity Check	SRC Check	DXR/PA Overrun/ Underrun Ck	Not Used	Not Used	PA/PB Overrun Check	PA/PB Data In/Out Parity Ck	Not Used	'10'	'30'	R	F2	2x	15	REF 100	CMCD	HN200
Port Buffer Check	UPBCK	LPBCK	P/B Overrun/ Underrun Ck	Byte Count Zero Check	Not Used	Byte Ctr Parity Ck	Byte Ctr Shadow Parity Ck	PA/PB Data In Parity Ck	ECC/PB Data In Parity Ck 1	ECC/PB Data In Parity Ck 2	'11'	'31'	R	F2	2x	16	REF 105	CMPB	JD200
Port Buffer Diagnostic	UPBDI	LPBDI	Port Buffer Test Lp W/R	Read Byte Count Shad.	Force Stg Reqst. Act.	Invert Byte Ct Shad Pty	Force Byte Ct Zero Ck	Not Used	Not Used	Not Used	'87' '07'	'A7' '27'	W R	—	——	——	REF 105	CMPB	JD200
Storage Adapter Check	USADPCK	LSADPCK	SSAR Increment Check	Storage Cycle Check	DA Dupl. Card Select Decode Ck	DA Data Addr 6-15 Check	SA/DA Data Addr 0-23 Check	Operation Complete Check	Not Used	Not Used	'17'	'37'	R	F2	3x	14	REF 105	CMSA	JS200
SSAR-0 0-7	USAR0	LSAR0	SSAR Bit 0	SSAR Bit 1	SSAR Bit 2	SSAR Bit 3	SSAR Bit 4	SSAR Bit 5	SSAR Bit 6	SSAR Bit 7	'80' '00'	'A0' '20'	W R	—	——	——	REF 105	CMSA	JS200
SSAR-1 8-15	USAR1	LSAR1	SSAR Bit 8	SSAR Bit 9	SSAR Bit 10	SSAR Bit 11	SSAR Bit 12	SSAR Bit 13	SSAR Bit 14	SSAR Bit 15	'81' '01'	'A1' '21'	W R	—	——	——	REF 105	CMSA	JS200
SSAR-2 16-23	USAR2	LSAR2	SSAR Bit 16	SSAR Bit 17	SSAR Bit 18	SSAR Bit 19	SSAR Bit 20	SSAR Bit 21	SSAR Bit 22	SSAR Bit 23	'82' '02'	'A2' '22'	W R	—	——	——	REF 105	CMSA	JS200
Storage Card Address Check	USCACK	LSCACK	Stg Card Addr Check -BCDE-	Stg Card Addr Check -FGHJ-	Stg Card Addr Check -MNPQ-	Stg Card Addr Check -RSTU-	AR Card Addr Check -K-	AR Card Addr Check -L-	Not Used	Not Used	'15'	'35'	R	F2	3x	16	SENSE 215	CMC1	JP200
Storage Control Check	USCCK	LSCCK	DD/DR Data 0-35 Parity Ck	DD/DR Data 36-71 Parity Ck	DR Clock Check 1	DR Clock Check 2	Not Used	Not Used	Not Used	Not Used	'14'	'34'	R	F2	3x	15	REF 105	CMC1	JP200

Note: These registers each have a backup register whose address is the same. The data in the byte count high and low registers is changed before it is loaded into the backup registers. Reading out the backup register requires that UPBDI/LPBDI bit 1 (Read Count Backup be set).

*R = Read Only
W = Write Only
R/W = Read or Write

**Sense Byte 7 = Bits 0-3 - Format ID
= 4-7 - Message ID

***Sense Byte8 = Bits 0-3 - Error Type
4 -7 - x = Operation Type

Note: External registers not described in this REF section of the MSM are described in the SENSE section. See the External Register Summary tables for the page numbers where the description of the register appears.

External Registers

Buffer ALU Pointer (BAP) Register

The BAP register is a 16-bit register consisting of the high-order byte, buffer ALU high (BAH), and the low-order byte, buffer ALU low (BAL). Together, these bytes contain the address of the buffer location accessed by the microprocessor during most manual buffer accesses. Some of these manual accesses are made using the channel buffer pointer (CBP). The BAP register is a read/write register with the hexadecimal address of '02'.

To set an address into or read an address out of the BAP register, the microprocessor must access the BAH or BAL bytes separately. The microprocessor accesses either the BAH or BAL depending on the state of the BAP toggle, bit 2 of the toggle FRU register (TFR). If the BAP toggle is set to 1, BAH is accessed; if it is set to 0, BAL is accessed.

The BAP changes to its opposite state when the microprocessor reads or writes BAP. For example, if the BAP toggle were set to 1 and the microprocessor read the BAP register, the byte would be read from BAH and the BAP toggle would change to the 0 state. A following read or write of BAP would access BAL.

Buffer Increment BAP (BFI) Register

The BFI register is the actual buffer location specified by the buffer ALU pointer (BAP). When the BFI register is used, the value of the BAP register is increased. The BFI register is a read/write register with a hexadecimal address of '05'.

Buffer (BFR) Register

The BFR register is the same as to the BFI register except that the value in the ALU pointer (BAP) register is not increased when the BFR register is used. The BFR register is a read/write register. Its hexadecimal address is '04', but this address is shared with the CFI register. The register actually to be accessed depends upon the setting of bit 5 of the data transfer control (DXC) register, as follows: when bit 5 = 0 the BFR register is accessed; when bit 5 = 1 the CFI register is accessed.

Channel Buffer Pointer (CBP) Register

The CBP register is a 16-bit register consisting of the high-order byte, channel buffer high (CBH), and the low-order byte, channel buffer low (CBL). Together, these bytes contain the address of the buffer location accessed during channel automatic transfers to and from the buffer. The CBP register is also used during some microprocessor manual buffer accesses.

The CBP register is a read/write register. It has a hexadecimal address of '00', but it shares this address with the channel cyclic redundancy check (CRC) register. Whether the CBP register (either the CBH or CBL byte) or the CRC register is accessed by address '00' depends on the status of the run channel bit, bit 7 of the channel transfer control (CXC) register, as follows: if run channel is off (CXC bit 7 = 0), the CBP register is accessed; if run channel is on (CXC bit 7 = 1), the CRC register is accessed.

To set an address into or read an address out of the CBP register, the microprocessor must access the CBH and CBL bytes separately. The microprocessor accesses either CBH or CBL depending on the state of the CBP toggle, bit 0 of the toggle FRU register (TFR). If the CBP toggle is set to 1, the CBH register is accessed; if it is set to 0, the CBL register is accessed. The CBP toggle changes to its opposite state when the microprocessor reads or writes the CBP register. For example, if the CBP toggle were set to 1 and the microprocessor read the CBP register, the byte would be read from CBH and the CBP toggle would change to the 0 state. Another read or write of the CBP register would access the CBL byte.

Channel Counter High (CCH) and Channel Low (CCL) Registers

The CCH and CCL registers contain the number of data bytes to be transferred to or from the channel. The CCH and CCL registers are write-only registers loaded by microcode.

The CCH and CCL register values are decreased by one by a signal from the data transfer (CDX) card. The channel search (CSR) card generates end of transfer (EOT) when the CCH and CCL registers are decreased by one to zero and the longitudinal redundancy check (LRC) is completed.

The CCH and CCL register addresses are decoded on the channel sequence control (CSC) card.

Buffer Increment CBP (CFI) Register

The CFI register is the actual buffer location specified by the channel buffer pointer (CBP) register. When the CFI register is used, the value in the CBP register is increased. The CFI register operates the same as the BFI register, except that the value in the CBP register, rather than the BAP register, is increased. The CFI register is a read/write register. It has a hexadecimal address of '04', but this address is shared with the buffer (BFR) register. The register actually accessed depends on the setting of bit 5 of the data transfer control (DXC) register, as follows: when bit 5 = 0 the BFR register is accessed; when bit 5 = 1 the CFI register is accessed.

Channel Cyclic Redundancy Check (CRC) Register

The CRC register keeps adding a cyclic redundancy check character as fields are transferred between the channel and the buffer. The hexadecimal address of the CRC register is '00', but this address is shared with the channel buffer pointer (CBP) register. Whether the CRC or CBP is accessed depends on the state of bit 7 of the channel transfer control (CXC) register, as follows: if run channel is off (CXC bit 7 = 0), the CBP register is accessed; if run channel is on (CXC bit 7 = 1), the CRC register is accessed. The CRC register is reset when run channel is turned off.

Condition Register 1 (CR1)

CR1 contains an allow/disable bit for each channel.

Condition Register 2 (CR2)

CR2 contains a not suppressible request-in bit for each channel.

Condition Register 3 (CR3)

CR3 contains a control unit (storage director) end bit for each channel.

Condition Register 6 (CR6)

CR6 contains a suppressible request-in bit for each channel.

Device Buffer Pointer (DBP) Register

The DBP register is a 16-bit register consisting of the high-order byte, device buffer high (DBH), and the low-order byte, device buffer low (DBL). Together, these bytes contain the address of the buffer location accessed during device automatic transfers to and from the buffer. The DBP register is a read/write register. It has a hexadecimal address of '01', but it shares this address with the device cyclic redundancy check (DRC) and pad counter register (PCR) registers. Whether the DBP register (either the DBH or DBL byte) or the DRC and PCR registers are accessed by address 01 depends on the state of bit 7 of the device tag gate (DTG) register, as follows; if DTG bit 7 = 0, the DBP register is accessed. To set an address into or read an address out of the DBP register, the microprocessor must access the DBH and DBL bytes separately. The microprocessor accesses either DBH or DBL depending on the state of the DBP toggle, bit 1 of the toggle FRU register (TFR). If the DBP toggle is set to 1, the DBH byte is accessed; if it set to 0, the DBL byte is accessed.

The DBP toggle changes to its opposite state when the microprocessor reads or writes the DBP register. For example, if the DBP toggle were set to 1 and the microprocessor read the DBP register, the byte would be read from the DBH byte and the DBP toggle would change to the 0 state. Another read or write of the DBP register would access the DBL byte.

Device Count High (DCH) and Device Count Low (DCL) Registers

The DCH and DCL registers contain the total number of bytes (halfwords for a two-byte device) in the field including bytes to be padded or discarded. The DCH and DCL registers are loaded before automatic data transfer by the microcode. The DCH and DCL registers are decreased by one by a signal from the director-director controller (DDC) card. The DDC card generates the end of transfer (EOT) signal when the DCH and DCL registers are decreased by one to zero.

Device Cyclic Redundancy Check (DRC) Register

The DRC register keeps adding a cyclic redundancy check character as fields are transferred between the device and the buffer. The hexadecimal address of the DRC register is '01', but this address is shared with the device buffer pointer (DBP) and pad counter register (PCR) registers. Whether the DRC and PCR registers or the DBP registers are accessed depend on the state of bit 7 of the device tag gate (DTG) register, as follows: if DTG bit 7 = 1 and the DBP toggle = 1, the PCR is accessed; if DTG bit 7 = 1 and the DBP toggle = 0, the DRC register is accessed.

The DRC register is reset whenever run device is turned off (DTG bit 7 = 0). However, the reset of the DRC register or the adding of the device cyclic redundancy check character is stopped when suspend DRC, data transfer control (DXC) register bit 6, is on (DXC bit 6 = 1).

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Note: External registers not described in this REF section of the MSM are described in the SENSE section. See the External Register Summary tables for the page numbers where the description of the register appears.

External Registers (Continued)

Data Transfer Control (DXC) Register

The DXC register controls automatic data transfer operations and gives bits that permit the microcode to control operations including the following registers:

- Transfer complete status (XCS)
- Transfer error status (XES)
- Check (CHK)
- Toggle FRU register (TFR)

Bit 0 – Status Reg Select 0

Bits 0 and 3 are used to select specific registers, all of which share hexadecimal register address '13'. These registers, and the decode of DXC bits 0 and 3 that select them are:

BITS 0,3	REGISTER SELECTED
00	XCS
01	XES
10	CHK
11	TFR

Bit 1

Not used.

Bit 2 – Reset End Op/Device End of Transfer Interrupt (Reset EODIR)

This bit is used by the microcode to reset the end/op device end of transfer interrupt latch. The action of setting this bit resets the latch, whether the bit is on or off.

Bit 3 – Status Reg Select 1

See Bit 0 for details.

Bit 4 – End/Op Device End of Transfer (EOP/DEOT) Interrupt

This bit is used by the microcode to select one of two interrupt modes:

BIT 4	INTERRUPT MODE
0	Normal interrupt mode
1	Speed matching buffer interrupt mode

In the normal interrupt mode, interrupts from level 3 to level 2 are handled just as they are in a machine that does not have the speed matching buffer feature. That is, an interrupt from level 3 to level 2 occurs when Select Out Trapped sets bit 2 (new level 2) of the interrupt level register (ILR) and ILR bit 7 (allow level 2) is set to 1.

In the speed matching buffer interrupt mode, an interrupt from level 3 to level 2 occurs when the EODIR latch is activated, setting ILR bit 2 (new level 2). Again, ILR bit 7 (allow level 2) must be set to 1 for the interrupt to occur. The EODIR latch is reset when DXC bit 2 (reset EODIR) is set. See Bit 2, Reset EODIR, above.

Bit 5 – CFI Select

This bit determines which of the two registers that share hexadecimal address '04' will be accessed by that address: the buffer increment CBP (CFI) register or the buffer (BFR) register. When bit 5 = 1, the CFI register is accessed; when bit 5 = 0, the BFR register is accessed.

Bit 6 – Suspend Device Cyclic Redundancy Check (DRC)

This bit is used by the microcode to either stop the resetting of the DRC register or to stop the adding of a cyclic redundancy check character by the DRC. This stopping makes it possible to add single check character for two fields separated by the fall and rise of Run Device and to add a single check character to two fields that are separated by one or more other fields. Note that automatic padding or discarding is inhibited when suspend DRC is active (DXC bit 6 = 1).

Bit 7 – Initialize Negative Data

This bit is used by the microcode to initialize the buffer to the negative data state. The negative data state is one in which automatic fetch operations are inhibited and the buffer is permitted to fill.

External Bus In (EBI) Register

The EBI register, located on the maintenance (MNT) card, is an 8-bit, read-only register used by the:

- Storage director to get failure data from the failing storage director (bits 0 through 7)
- Maintenance device to control a storage director during failure analysis (bits 0 through 7)

The input to the EBI register is the External Bus In (0-7, P) lines from the maintenance device adapter (MDA). These lines are buffered through the EBI buffer into the EBI register. The output of the EBI register is available to the microprocessor on the ALU In (0-7, P) lines.

External Bus Out (EBO) Register

The EBO register, located on the maintenance (MNT) card, is as 8-bit, write-only register used by the:

- Storage director to control an initial program load (IML) operation (bits 0 through 3)
- Storage director to get failure data from the failing storage director (bits 0 through 7 and P)
- Maintenance device to communicate with a storage director during failure analysis (bit 0 through 7 and P)

The input to the EBO register is the ALU Out Bit (0-7, P) lines from the microprocessor. The output is available to the diskette drive, the alternate storage director, or the maintenance device on the External Bus Out Bit (0-7, P) lines except during execution of a display check register or a display FRU register maintenance command.

Interrupt Level Register (ILR)

The ILR, located on the maintenance (MNT) card, is an 8-bit, read/write register used by the:

- Maintenance device to change or display a storage director register (bit 0)
- Microprocessor to maintain the storage director in the current interrupt level (bits 0 through 2) or to change to another interrupt level
- Microprocessor to define the previous level of interrupts (bits 3 and 4)
- Microprocessor to mask interrupt levels (bits 5 through 7)
- Hardware to start external interrupts (bits 1 and 2)

Initial Microcode Load (IML) Register

The IML register, located on the maintenance (MNT) card, is an 8-bit, read/write register used by the:

- Diskette drive to transmit IML data and index to the microprocessor (bits 0 and 1)
- Microprocessor to control the IML operation (bits 2 through 5)
- Diskette load control switches to select the correct diskette track which loads the storage director (bits 6 and 7)

The output of the IML register is available to the microprocessor on the ALU In 2 Bus Bit (0-7, P) lines.

Internal Register Group (IRG) Register

The IRG register, located on the storage director microprocessor (SDM) card, is addressed as one of the external registers. This register contains the primary and secondary group address for the internal registers.

Maintenance Control Register (MCR)

The MCR register, located on the maintenance (MNT) card, is an 8-bit, write-only register used by the:

- Storage director to verify an initial microcode load (IML) operation
- Storage director to get failure data from the failing storage director
- Maintenance device to start communications
- Control storage for recovery routines

Input to the MCR register is the ALU Out Bit (0-7, P) lines from the microprocessor. The output is available to either the operating storage director or the maintenance device.

Note: External registers not described in this REF section of the MSM are described in the SENSE section. See the External Register Summary tables for the page numbers where the description of the register appears.

External Registers (Continued)

Maintenance Control/Sense (MCS) Register

The MCS register, located on the device counter (DCT) card, contains machine status (wait, process, status pending) information. The MCS register is loaded during a command or an operation.

Although the MCS register is physically located on the DCT card in the control interface area, the MCS register is functionally located in the maintenance connection functional area.

The MCS register contains information that controls the interval timer, read-only storage (ROS), and padding.

The MCS is a read/write register with a hexadecimal address of '1A'.

Bit 0 – Enable Interval Timer

This bit indicates that the interval timer is operating. The microcode sets bit 0 to activate the timer and resets bit 0 to deactivate the timer.

Bit 1 – Read Only Storage (ROS) Select

This bit indicates that the microprocessor is executing the contents of the ROS register. Start DXR Clock, from the maintenance (MNT) card, sets bit 1 to cause the microprocessor to fetch from ROS. Start DXR Clock is activated immediately before the first microinstruction is executed following a Power On Reset (POR) or an Initial Microcode Load (IML) operation. Bit 1 is reset by the microcode after track 0 of the diskette has been completely loaded.

Bit 2 – Enable Reset CRC

This bit is used by the microcode to generate a single channel cyclic redundancy check character over two fields that are separated by the fall and rise of run channel, DXC bit 7. If the MCS register, bit 2, is set to 1, the CRC register is reset when run channel falls; if it is set to 0, the CRC register is not reset at the fall of run channel.

Bit 3

Not used.

Bit 4 – Throttle

This bit is used by the microcode to limit the number of bytes held in the buffer during channel-to-device transfers (write operations). The number of bytes is limited to 8 if the channel is in high speed mode (TFR bit 5 = 1) and to 3 bytes if the channel is not in high speed mode (TFR bit 5 = 0). The throttle is only activated when the channel and device are operating at the same time.

A high speed channel cannot write or search at full speed when connected to a 400-foot cable unless the throttle is activated.

Bits 5 Through 7 – Execution Mode

Bits 5, 6, and 7 indicate the execution mode of the storage director. Each bit activates an indicator on the operator panel. Bit 5 activates the Wait indicator, bit 6 the Process indicator, and bit 7 the Status Pending indicator.

Maintenance Sense Register (MSR)

The MSR, located on the maintenance (MNT) card, is an 8-bit, read/write register used by the:

- Maintenance device to control a storage director during failure analysis (bits 0, and 2 through 5)
- Storage director to get failure data from the failing storage director (bits 0 through 4)
- Storage director to control the initial microcode load (IML) operation (bits 6 and 7)

The MSR bits are turned on by the control and check lines that are either on the MNT card or on other storage director cards. The output is available to the microprocessor on the ALU In 2 Bus Bit (0-7, P) lines.

Pad Counter Register (PCR)

The PCR, located on the DCT card, is an 8-bit read/write register with a hexadecimal address of '01' for read and '0D' for write. The read address is shared with the device buffer pointer (DBP) and the device cyclic redundancy check (DRC) registers. How each of these registers is selected depends upon the state of bit 7 of the device tag gate (DTG) and the state of DBP. When:

- DTG bit 7 = 1 and DBP toggle = 1, the PCR is accessed
- DTG bit 7 = 1 and DBP toggle = 0, the DRC register is accessed
- DTG bit 7 = 0, the DBP register is accessed.

The PCR is used with the device count high (DCH) and device count low (DCL) registers to control padding and discarding of bytes for records transferred between the device and the buffer.

The PCR is initialized with one less than the number in the low-order byte of the record length. The DCH and DCL registers are initialized with the total number of bytes (halfwords for a 2-byte device) in the field including bytes to be padded or discarded. The DCH and DCL registers and the PCR are lowered by one with each byte transferred. At the end of the record transfer, the number of bytes to be padded or discarded is available in the DCL register and is used to automatically control padding and discarding.

Channel Speed Control (SPC) Register

The SPC register, located on the channel data transfer (CDX) cards, uses the CXC register bits 1, 2, 3, 6, 7, and P lines to initialize the channel hardware to perform data transfers in the channel at the data rate of the attached device. The gates for the SPC register are the CDX/CSR Clock T4 line and the CXC Reg (CSR) Bit 4 line.

Storage Directors – External Register Description (Cont.) REF 75

Note: Indirect registers not described in this REF section of the MSM are described in the SENSE section. See the Indirect Register Summary tables for the page numbers where the description of the register appears.

General Registers

General Diagnostic (GDI)

Bit 0 - Force Data/Ref Command Check

This diagnostic function inverts the command parity bit for the command ABC bus.

Bit 1 - Test Loop W/R ECC

This diagnostic function inhibits storage requests so that loop W/R functions can be performed to the ECC without storing data in storage. When this function is active, write and read operations between the ADT buffer, port buffer, and ECC area are performed in the normal way but storage cycles are not executed.

Bit 2 - Test Loop W/R Storage

This diagnostic function inhibits the subsystem storage so that loop W/R functions can be performed, before the array, without storing data in storage.

Bit 3 - Force DR-A Clock Check

This bit forces an error in the clock circuits to cause a clock error.

Bit 4 - Force DR-B Clock Check

This bit forces an error in the clock circuits to cause a clock error.

Bit 5 - Force SC Clock Check

This bit forces a SC clock check (CSCCK register, bit 0).

Bit 6 - Force SC Select Check

This bit forces a SC select check (CSCCK register, bit 1).

Bit 7 - Force Test and Set Check

This bit forces a test and set check (CSACK register, bit 0) by forcing both test and set bits active and GTS bits 0-2 active.

ECC Diagnostic (GECCDI)

Bit 0 - Degate Decodes

This bit degates the decodes of ECC force bits 1, 2, and 3.

Bits 1-3 - ECC Force Bits 1, 2, and 3

These bits are coded to cause different diagnostic ECC functions.

Bit 4 - Invert ROS-M Parity

This diagnostic function inverts the output of ROS parity on fetch operations.

Bit 5 - SD1 Write/Hold Check Bytes

This bit is used to control the write check bytes for storage director 1.

Bit 6 - SD2 Write/Hold Check Bytes

This bit is used to control the write check bytes for storage director 2.

Bit 7 - Inhibit DD/Stg Data Out Check

This bit inhibits UECCCK/LECCCK bits 6 and 7 so that CSCCK bits 0-1 can be checked.

ECC Check Bytes 1 and 2 (GECCCK1/GECCCK2)

The ECC check byte 1 and 2 registers represent the 16 check bits held for either SD1 or SD2 based on the setting of GECCDI bits 5 and 6 (SD1/SD2 Write/Hold Check Byte). GECCCK1 represent check bits 0-7 and GECCCK2 represent check bits 8-15. If GECCDI bits 5 and 6 are not active, the check bytes represent the last fetched check bytes from storage.

ID Switches (GIDSW)

This register mirrors the setting of the ID switches indicating the subsystem storage ID (0-255).

ECC Syndrome Bytes 1 and 2 (GSYN1/GSYN2)

Bits 0-7 of the GSYN1 and GSYN2 registers represent the 16 inverted ECC syndrome bits generated from the last fetched data and check bits. These bits are used by the diagnostics.

Subsystem Storage – Indirect Register Description

Write Check Bytes 1 and 2 (GWRCK1/GWRCK2)

These registers are used to hold the 16 write check bits for ECC when the microcode requires that the check bits be changed. Each register is eight bits in length; GWRCK1 using bits 0-7 and GWRCK2 using bits 8-15. This function is active for both the upper and lower ports in both storage directors.

These bytes will be stored in cache if the appropriate GECCDI bit 5 or 6 (SD1/SD2 Write/hold Check byte control) is active. These bytes are used to go to cache instead of the ECC generated check bytes.

Subsystem Storage – Indirect Register Description

Note: Indirect registers not described in this REF section of the MSM are described in the SENSE section. See the Indirect Register Summary tables for the page numbers where the description of the register appears.

Common Registers

ASDM Control (CACTL/ACTL)

This register controls the ASDM and can be read by either the SDM or the ASDM; it can be written by only the SDM.

ASDM Read Register 1 and 2 (CARD1/CARD2)

The ASDM Read Registers 1 and 2 give a method for the SDM to send a byte of data to the ASDM. The specific bits are defined and controlled by the microcode. These registers can be read by either the SDM or the ASDM; they can be written by only the SDM.

ASDM Write Registers 1 and 2 (CAWR1/CAWR2)

These registers give a method for the ASDM to send a byte of data to the SDM. The specific bits are defined and controlled by the microcode. These registers can be read by either the SDM or the ASDM. They are written into by only the ASDM.

Communication Adapter Diagnostic (CCOMADI)

Bit 0 (Force This SD Request Honored) is used with bits 3-7 (CA Force Bits). Bit 0 causes this storage directors Request Honored to be set active.

Bits 1-2 are not used.

Bits 3-7 are coded to cause different functions. These bits remain active until reset.

X'00' – No Forcing (Normal Mode)

This mode is forced on during power on reset.

X'01' – Invert ASDM CS Parity

This mode forces an ASDM control parity error.

X'02' – Force ASDM LSR Address Parity Check

This mode forces a LSR Address Bus parity error.

X'03' – Force Duplicate Decode Check

This mode forces a duplicate decode error.

X'04' – Force Other SD Communication Request Off

This mode is used to inhibit the other storage director's communication request. Forcing permits one SD to inhibit the other SD from causing a request, which permits a positive check of the priority request circuits. If SD2's power is off, this function will not work.

X'05' – Force ADT Buffer/ASDM CS In Parity Check

This mode inverts bit 7 of the ADT Buffer to ASDM CS bus.

X'06' – Force Other SD Communication Request On

This mode is used to force the other SD communication request active. Forcing permits one SD to activate the other SD's request, which permits a positive check of the priority request circuits. If SD1's power is off, this function is operational.

X'07' – Invert CAR Parity

This mode inverts a CAR parity.

X'08' – Force T-Clock Check

This mode inhibits a T-clock going to the checker.

X'09' – Force Multiple Chip Select Check

This mode forces a multiple chip select error in the communication buffer.

X'0A' – Invert SD1 Indication

This mode forces SD1 Indication active when executed from SD2 and forces SD1 Indication not active when executed from SD1.

X'0B' – Invert ASDM External Address Parity

This mode inverts the ASDM external address parity bit.

X'0C' – Forces External Register Check

This mode forces an external register selection check.

X'0D' – Forces Range Select Check

This mode forces all the range select bits to a one.

X'0E'–X'0F' – Not Used

X'10' – Force ALU Out Control/Ext Address Check

This mode forces an ALU Out Control Check by causing the Invert Chan/Dev Run circuits to be in error. This error will occur immediately. The External Register Address check is also forced.

X'11' – Clamp DXR Parity Active

This mode, on a store operation, forces the parity bit active on the DXR bus to port adapter buffer for both upper and lower ports. On a fetch operation the parity bit is forced active on the DXR bus to the channel or device.

X'12' – Force DXR/PA Overrun

This mode forces an overrun condition for both upper and lower active ports.

X'13' – Force DXR/PA Underrun

This mode forces an underrun condition for both upper and lower active ports.

X'14' – Inhibit Read Clock Delay

This mode inhibits the sample of read clock delay on the Indirect Register bus. This signal is returned from the card containing the indirect register read.

X'15' – Force ALU Control Check

The ALU Control check is forced by causing the invert Chan/Dev ADT Run circuits to have an error. This is an immediate error.

X'16' – Clamp ALU Out Parity Active

This mode causes the ALU out parity to be set active.

X'17' – Invert External Address Active

This mode inverts the External Address parity.

X'18' – Force Addr Dec Ck

This mode forces an CD Duplicate IR Addr Decode Check.

X'19' – Force Write Gate

This mode forces the write gate active on the Indirect Register bus.

X'1A' – Invert X'1B' Register Parity

This mode inverts the X'1B' register parity bit.

X'1B' – Invert X'0F' Register Parity

This mode inverts the X'0F' register parity bit.

X'1C' – Inhibit Read Gate

This mode inhibits the read gate on the Indirect Register bus.

X'1D' – Force PA/PB Port Buffer Overrun

This mode forces a port overrun condition in the CMCD card.

X'1E' – Invert Address Decoder Parity

This mode inverts the parity going to the address decoder.

X'1F' – Invert Address Register In Parity

This mode inverts the parity going to the input of the address register bus.

Note: Indirect registers not described in this REF section of the MSM are described in the SENSE section. See the Indirect Register Summary tables for the page numbers where the description of the register appears.

Common Registers (Continued)

Communication Address (CCOMADR)

The communication address register is used to determine the address to be accessed in the communication buffer (00-FF). The register contents are increased during a read/write operation with the communication buffer each time the RDF/WRF register is accessed.

Common Control Shadow (CCTLS)

This register is a copy of the Common Control (CCTL) register.

Storage Address Diagnostic (CSADI)

Bits 0–3 – DA Force Bits 0–3

This register is used when storage address diagnostics are run. Bits 0-3 are set to cause the following functions.

X'0' – No forcing (Normal Mode)

This mode is forced on during power on reset.

X'1' – Invert Segment/Word SAR Parity

This mode forces checks (USCACK bits 0-5) by inverting the Segment/Word SAR parity during Read/Write operations for storage boards 1 and 2 by using the appropriate addresses.

X'2' – Force Stg Card Ref Address Checks BD1

This mode forces checks (CSRACK bits 0-5) during refresh operations for storage board 1.

X'3' – Force Stg Card Ref Address Checks BD2

This mode forces checks (CSRACK bits 0-5) during refresh operations for storage board 2.

X'4' – Force DA Refresh Address Incr Check

This mode forces check CSARCK bit 6 and inhibits check CSARCK bit 7.

X'5' – Force DA Data Address Parity Check

This mode forces check USADPCK bit 3 (DA Data Address 6-15 Check) by inverting a bit to the checker.

X'6' – Clamp SA/DA P0-P2 Inactive

This mode forces check USADPCK bit 4 (SA/DA Data Address 0-243 Check) by forcing P0/P1/P2 inactive.

X'7' – Force Stg BD1 Ref Address Parity Check

This mode forces check CSARCK bit 7 (DA Ref Address 6-15 Check) to be set.

X'8' – Force Stg BD2 Ref Address Parity Check

This mode forces check CSARCK bit 7 (DA Ref Address 6-15 Check) to be set.

X'9' – Force Stg Card Decode Check

This mode forces check USADPCK bit 2 (DA Duplicate Card Sel Decode Check).

X'A' – Invert Bit/Data Gate-A Parity

This mode inverts Bit/Data Gate Parity for a gate-A transfer.

X'B' – Invert Reg/Bit/Data Gate-B Parity

This mode inverts Reg/Bit/Data Gate Parity for a gate-B transfer.

X'C' – Force Storage Card Select 0-3 Inactive

X'D' – Force Storage Cycle Check

X'E' – Force Operation Complete Check

X'F' – Not used

This mode forces storage Card Select 0-3 inactive for both storage boards 1 and 2. There are four card selects per board; 0, 1, 2, and 3.

Bit 4 – Clamp Addr Incr Predict Parity

This bit, when set to a one, holds the three SSAR Incrementer Predict Parities not active.

Bit 5 – Force Storage Address Decode

This bit, when set to a one, causes the SA Address Decode to be active.

Bit 6 – Force Storage Control Decode

This bit, when set to a one, causes the C1 Address Decode to be active.

Bit 7 – Not Used

Commom Status 4 (CSTAT4)

Bit 0 – Not Used

Bit 1 – SD1 Indicator

Bit 2 – SD2 Indicator

Indicates which SD contains this register.

Bit 3 – Not Used

Bit 4 – Timer Overflow

Indicates that the 57 Millisecond Timer is full.

Bit 5 – Storage Control Board Power Off

This bit indicates that the power for the storage control board is off.

Bit 6 – Storage Board 1 Power Off

This bit indicates that the power for the storage board 1 is off.

Bit 7 – Storage 2 Power Off

This bit indicates that the power for the storage board 2 is off.

X'1B' Shadow (CWRBS)

This register is the shadow register of register X'1B'. When an interrupt occurs, the contents of the X'1B' register can be held by the microcode in the shadow register until the interrupt processing is completed. After the interrupt is completed and under microcode control, the X'1B' register contents are replaced by the shadow register contents.

Common Status 5 (CSTAT5)

Bits 0 through 6–Not Used

Bit 7 – Expanded Storage Installed

This bit indicates that subsystem storage cards contain either 2 or 4 megabytes of storage. Machines without expanded storage contain 1 megabyte storage cards.

Note: Internal registers not described in this REF section of the MSM are described in the SENSE section. See the Indirect Register Summary tables for the page numbers where the description of the register appears.

Common Registers (Continued)

Special Operation Codes

The special operation codes are used to control additional functions on the indirect register bus. The special operations are executed by setting the X'1B' register to a value of X'D0'-X'D9'.

Special Operation Registers

SP OP Hold X'1B' Shadow Register (CSPHLD)

The write address for this register is X'D0'. This special operation causes the X'1B' register to be held or prevented from any more updates. Register CWRBS is the shadow register for the X'1B' register. The shadow register is used when an interrupt in being processed. The interrupt saves the X'1B' contents in this shadow register so that the original X'1B' contents can be restored by execution of SP OP Restore X'1B' register special operation. Since most X'1B' and X'0F' register operations requires the writing of register X'1B' followed with either reading or writing of the X'0F' register, it is possible for an interrupt to occur between the WRB function and the RDF/WRF function. Processing the interrupt gives enough time for restoring the X'1B' register before the immediate reading or writing of register X'0F'.

SP OP Restore X'1B' Shadow Register (CSPRES)

The write address for this register is X'D1'. This special operation permits the X'1B' register to be restored with shadow register CWRBS contents. Register CWRBS contents are loaded into the X'1B' register on the following 220 nanosecond cycle after this special operation. If the register address in the X'1B' register is a register to be written, then the next instruction may be a write to register X'0F'. If the register address in the X'1B' register is a register to be read, then the next instruction must be a dummy cycle followed by a read of register X'0F'.

SP OP Read Communication (CSPRDC)

The write address for this register is X'D2'. This special operation places the storage director in a mode to read the communication buffer. 'Request honored' should be obtained before getting into this mode. This mode is only valid with 'request honored'. A dummy cycle (or slow store) is required after this special operation.

SP OP Write Communication (CSPWRC)

The write address for this register is X'D3'. This register is reset to X'00' by a 'controlled machine reset' or a 'system power on reset'. This special operation puts the storage director in a mode to write the communication buffer. 'Request honored' should be obtained before getting into this mode. This mode is only valid with 'request honored'.

SP OP Set Message Waiting (CSPSMW)

The write address for this register is X'D4'. This special operation sets 'message waiting' to the other storage director. This indicates to the other storage director (receiving storage director) that a message is waiting for action. The receiving storage director's hardware stores the 'message waiting' in bit 0 of register CSTAT3. After this special operation has set status in the receiving unit, the X'1B' register can be changed. This special operation does not need setting if the message does not need the other storage director. The special operation execution can be determined by observing 'msg waiting echo back to sender' in register CSTAT3, bit 1.

SP OP Receiver Reset Message Waiting (CSPRRMW)

The write address for this register is X'D5'. This special operation resets the 'message waiting' bit in its own storage director. If the 'message waiting' bit is off when the operation is received, no change takes place ('message waiting' is still off).

SP OP Sender Reset Message Waiting (CSPSRMW)

The write address for this register is X'D6'. This special operation resets the 'message waiting' bit in the other storage director. If the 'message waiting' bit is off when this operation is received, no change takes place ("message waiting' is still off). To determine if this special operation is executing correctly, observe the 'upper port single error correction' bit in CSTAT2, bit 1.

SP OP Set Inhibit SD Reset (CSPSISR)

The write address for this register is X'D7'. This special operation inhibits the '+selective or system reset' signal on the channel sequence control card from going to the maintenance card (MNT) in the storage director. If a '+selective or system reset' is being inhibited, the reset will be allowed active, when this inhibit has timed out. This inhibit does not stop the channel activity associated with the channel/control unit's handling of interface resets. A timer that overflows in 57-114 milliseconds will reset this bit.

SP OP Reset Inhibit SD Reset (CSPRISR)

The write address for this register is X'D8'. This special operation allows '+selective or system reset' to be active again by resetting the previous inhibit storage director reset condition.

SP OP Reset Timer Overflow (CSPRTO)

The write address for this register is X'D9'. This special operation resets the timer overflow bit (CSTAT4 register, bit 4).

SP OP Read IR Checks (CSPRDIC)

The write address for this register is X'D9'. This special operation inhibits the X'0F' register's IR data bus. This alternate register is addressed when a Check 2 error is being analyzed. The CSPRDIC register is used because the data that is read from the IR (indirect registers) bus could contain an error because of a IR bus malfunction. The CSPRDIC register contents will show that the data is valid or not valid. This register does not need any microcode resets, since the register is always clocking the inputs. When the original check is reset at its source register, the CSPRDIC register will also set its bits not active. The CSPRDIC register contents are:

Bit 0 – Aux Adapter IR Summary Check

This bit being a one indicates that one of the following is active:

- CAAJCK register bit 0 – ADT/ASDM IR Check
- CAAJCK register bit 4 – AA Duplicate IR Address Decode Check

Bit 1 – Communication Adapter IR Summary Check

This bit being a one indicates that one of the following is active:

- CCOMACK register bit 0 – Communication Adapter IR Summary Check
- CCOMACK register bit 4 – CA Duplicate IR Address Decode Check

Bit 2 – Port Adapter IR Summary Check

This bit being a one indicates that one of the following is active:

- CPACK1 register bit 0 – Port Adapter IR Check
- CPACK1 register bit 5 – Read Clock Delay Check
- CPACK1 register bit 7 – External Register Read Parity Check
- CPACK2 register bit 5 – CD Duplicate IR Address Decode Check

Bit 3 – Port Control IR Summary Check

This bit being a one indicates that one of the following is active:

- CCOMACK register bit 5 – Port Control IR Parity Check
- CCOMACK register bit 6 – Port Control IR Read Parity Check

Bit 4 – Control Board IR Summary Check

This bit being a one indicates that one of the following is active:

- CSACK register bit 1 – Address Decode Check
- CSACK register bit 2 – Upper Port Buffer IR Check
- CSACK register bit 4 – Lower Port Buffer IR Check
- CSACK register bit 5 – ECC IR Check
- CSACK register bit 6 – Storage Adapter IR Check
- CSACK register bit 7 – Storage Control IR Check

Bit 5-7 – Not Used

Note: Indirect registers not described in this REF section of the MSM are described in the SENSE section. See the Indirect Register Summary tables for the page numbers where the description of the register appears.

Upper and Lower Port Registers

There are a set of upper and lower port registers for each storage director.

Upper Control Register (UCTL)

Bit 0 - Storage Run

This bit starts the fetch or store operation for the upper port (channel).

Bit 1 - Check Reset

This bit controls the resetting of all resettable check bits for the upper port.

Bit 2 - Invert Channel Run

This bit is set active when data is not transferred to or from the channel (manual data transfer). Correct control of these bits will select the desired data path(s).

Bit 3 - Invert Channel ADT Direction

This bit inhibits the data from leaving the ADT buffer and going to the channel on a automatic storage to channel operation.

Bits 4-7 - Not Used

Lower Control Register (LCTL)

Bit 0 - Storage Run

This bit starts the fetch or store operation for the lower port (device).

Bits 1 - Check Reset

This bit controls the resetting of all resettable check bits for the lower port.

Bit 2 - Invert Device Run

This bit is set active when data is not transferred to or from the device (manual data transfer).

Bit 3 - Invert Device ADT Direction

This bit inhibits the data from leaving the ADT buffer and going to the device on a automatic storage to device operation.

Bits 4-7 - Not Used

Control Shadow – Upper and Lower (UCTLS/LCTLS)

These registers are used for backup of the UCTL/LCTL registers.

Byte Counter High/Low (UCTRH/LCTRH, UCTRL/LCTRL)

The byte counter register is 16 bits in length. Registers UCTRH/LCTRH are the high order bits (0-7) and registers UCTRL/LCTRL are the low order bits (8-15) of the counter. These registers are used with either the fetch or store data operations. The counter is decreased for each byte fetched or stored in the port buffer.

These registers each have a backup (shadow) register whose address is the same as the Byte Counter High/Low registers. Reading out the backup registers requires that UPBDI/LPBDI bit 1 (Read Byte Count Shadow) be set.

ECC Check (UECCCK/LECCCK)

Bit 0 - ECC Uncorrectable Check

This bit indicates that during a fetch operation an error occurred and has not been corrected (three or more bits are in error).

Bit 1 - PB/ECC Data In Check 1

This bit indicates that the port buffer which is registered before the check syndrome matrix contains a parity error. This check is for the CME1 card.

Bit 2 - PB/ECC Data In Check 2

This bit indicates that the port buffer which is registered before the check syndrome matrix contains a parity error. This check is for the CME2 card.

Bit 3 - ECC Data In or ROS Check E1

This bit indicates that the port buffer data at the MUX output of the check two register, from the port buffer, contains a parity error. ECC Data In or ROS Check 1 is for the CME1 card.

Bit 4 - ECC Data In or ROS Check E2

This bit indicates that the port buffer data at the MUX output of the check two register, from the port buffer, contains a parity error. ECC Data In or ROS Check 2 is for the CME2 card.

Bit 5 - ROS-M Check

This bit indicates a byte parity error at the output of the CME3 card.

Bit 6 - E1/DD Storage Data Out Parity Check

This bit indicates that a parity error was detected on the data bus going to the data drivers.

Bit 7 - E2/DD Storage Data Out Parity Check

This bit indicates that a parity error was detected on the data bus going to the data drivers.

OP/CTL Register (UOPCTL/LOPCTL)

Bit 0 - Fetch or Store Operation:

The fetch (bit 0 = 0) or store (bit 0 = 1) operation transfers data between the subsystem storage and the ADT buffer, device, or channel. The upper port registers are used with channel data operations and the lower port registers are used with device data operations. The starting address from which data is stored or fetched is determined by SSAR and is on a 16 byte boundary.

Bit 1 - Inhibit SSAR Increment

This bit, when on, inhibits the incrementing of the SSAR registers.

Bit 2 - Manual or Auto Storage Mode

In manual storage mode (bit 2 = 0), controls the flow of data between storage and either the ADT buffer or the ASDM control storage. In auto storage mode (bit 2 = 1), controls the flow of data between the storage and either the channel or the device.

Bit 3 - Not Used

Bit 4 - Inhibit SRC

This bit controls the disabling of the storage CRC (SRC) function and inhibits the fetching or storing of SRC characters to or from storage.

Bit 5 - Accumulate SRC

This bit inhibits the fetching of the SRC bytes from storage.

Bits 6-7 - Not Used

OP/CTL Shadow – Upper and Lower (UOPCTLS/LOPCTLS)

These registers are used for backup of the OP/CTL (UOPCTL and LOPCTL) registers.

Port Adapter Check – (UPACK/LPACK)

Bit 0 - DXR/PA Parity Check

This bit indicates that a parity error was detected in the buffer registers (BU1/BL1).

Bit 1 - SRC Check

This bit indicates that a cyclic redundancy error was detected on the data from storage.

Bit 2 - DXA/PA Overrun/Underrun Check

This bit indicates that an overrun or underrun condition was detected to or from the channel or device. An overrun condition is detected when the BU1/BL1 registers are full and cannot accept any more data. An underrun condition is detected when the BU2/BL2 registers are empty and the channel or device attempts to take data.

Bits 3-4 - Not Used

Bit 5 - PA/PB Overrun Check

This bit indicates that a port buffer overrun condition was detected. An overrun condition is when a byte of data to be sent to the port buffer from the port adapter did not occur.

Bit 6 - PA/PB Data In/Out Parity Check

This bit indicates that a parity error was detected between the port adapter function and the port buffer.

Bit 7 - Not Used

Note: Indirect registers not described in this REF section of the MSM are described in the SENSE section. See the Indirect Register Summary tables for the page numbers where the description of the register appears.

Upper and Lower Port Registers (Continued)

Upper and Lower Port Buffer Check (UPBCK/LPBCK)

Bit 0 - PB Overrun/Underrun Check

This error, on a store operation, indicates that the port buffer is full and a data byte was attempted to be stored into it. On a fetch operation, this bit indicates that the port buffer is empty and a data byte was attempted to be fetched from it.

Bit 1 - Byte Count Zero Check

This bit indicates that the byte count equal zero controls are in error.

Bit 2 - Not Used

Bit 3 - Byte Counter Parity Check

This bit indicates that a parity error was detected in the byte counter register during a fetch or store operation.

Bit 4 - Byte Counter Shadow Parity Check

This bit indicates a parity error was detected in the byte counter shadow register during a fetch or store operation.

Bit 5 - PA/PB Data In Parity Check

This bit indicates a parity error was detected on the bi-directional bus, from the CMCD card to the port buffer, during a store operation.

Bit 6 - ECC/PB Data In Parity Check 1

This bit indicates a parity error was detected in the port buffer (holding the first 128 bytes of data) during a fetch operation.

Bit 7 - ECC/PB Data In Parity Check 2

This bit indicates a parity error was detected in the port buffer (holding the second 128 bytes of data) during a fetch operation.

Port Buffer Diagnostic – Upper and Lower (UPBDI/LPBDI)

Bit 0 - Port buffer test loop W/R

This diagnostic function inhibits storage requests so that loop W/R functions can be performed to the port buffer without storing data in the storage. Write and read operations between the port buffer and port adapter are performed but the storage cycles are not executed. On store operations the data stays in the port buffer. On fetch operations the data that was previously placed into the port buffer is fetched and sent to the port adapter. Storage access is inhibited until this bit is reset.

Bit 1 - Read Byte Count Shadow

This bit causes the byte count shadow register addresses to be used.

Bit 2 - Force Storage Request Active

This bit forces the storage request active for this port buffer path.

Bit 3 - Invert Byte Count Shadow Parity

This bit causes the byte counter shadow (BCS) parity bit to be inverted.

Bit 4 - Force Byte Count Zero Check

This bit forces a UPBCK/LPBCK bit 1 error.

Bits 5-7 - Not Used

Storage Adapter Check (USADPCK/LSADPCK)

Bit 0 - SSAR Increment Check

This bit indicates that a parity error occurred while incrementing the SSAR registers. There are six parity checkers; three incrementer predict parity checkers and three parity checkers on the address bus to the incrementer.

Bit 1 - Storage Cycle Check

This bit indicates that no storage cycle or more than one storage cycle has occurred.

Bit 2 - DA Duplicate Card Select Decode Check

This bit indicates that the card select decoder and the duplicate decoder value are different.

Bit 3 - DA Data Address 6-15 Check

This bit indicates that a parity error was detected on the address bus leaving the CMDA card during a fetch or store operation.

Bit 4 - SA/DA Data Address 0-23 Check

This bit indicates that a parity error was detected while sending an address from the CMSA card to the CMDA card.

Bit 5 - Operation Complete Check

This bit indicates that the 'inhibit operation complete' signal between the CMSA and the CMC2 did not occur on a store operation.

Bits 6-7 - Not Used

SSAR-0, -1, and -2 (USAR0/LSAR0), (USAR1/LSAR1), (USAR2/LSAR2)

The SSAR registers are used to address the subsystem storage. The registers are 24 bits in length and have a valid address range from X'000000' to X'1FFFFF'.

The SSAR register is increased by one for each sixteen bytes of data fetched or stored unless OP/CTL bit 1 (Inhibit Increment) is active in which case the addressed location is accessed repeatedly.

Storage Control Check (USCCK/LSCCK)

Bit 0 - DD/DR Data 0-35 Parity Check

This bit indicates that a parity error was detected on the data bus going to storage.

Bit 1 - DD/DR Data 36-71 Parity Check

This bit indicates that a parity error was detected on the data bus going to storage.

Bit 2 - DR Clock Check 1

This bit indicates that a clock check was detected.

Bit 3 - DR Clock Check 2

This bit indicates that a clock check was detected.

Bit 4-7 Not Used

Maintenance Device

Contents of This Section

References to Other Sections

See the PDA section in the Maintenance Support Manual (MSM) for an explanation of the stop and save operation.

See the DC section in the Error Code Manual (ECM) for a complete description of the maintenance connection tests.

MD Introduction

The maintenance device (MD) is the primary maintenance tool for the 3880. For more information on the MD, review the instruction label inside the top cover of the MD.

Note: Using the MD at the 3880 can interfere with a device diagnostic in progress.

Three MD diskettes are supplied for the 3880 Models with subsystem storage.

- Diskette 1 - Storage Director Maintenance Maps
- Diskette 2 - Subsystem Storage Maintenance Maps
- Diskette 3 - Power Maintenance Maps

Note: Always start maintenance activities with diskette 1. IPL the MD with diskette 1 and the MD will provide instructions when a diskette change is needed.

All 3880 maintenance analysis procedures (MAPs) are stored on the diskettes. All diagnostic programs are stored on the functional diskettes. When a diskette is loaded in the MD diskette drive, the MAPs start running. The MAPs are used to:

Note: Do not power the MD on or off with a diskette inserted in the MD.

- Test the connection between the MD and the 3880.
- Start the diagnostic programs on the 3880 Storage Control Functional Code Diskette.
- Request actions such as enter symptom information, answer questions, or exchange parts. The MAPs also give MIM page references.

The main parts of the MD are:

- MD diskettes 3. The MD diskettes must remain with the 3880 with which they were shipped.
- Instruction label 4. The label describes how to start and use the MD and what to do when it fails.
- Keyboard/Display (K/D) 5. The K/D is used to enter and display data.
- Operator panel 6.
- MD diskette drive 7.

Note: The 3880 MD connector 1 is located below the A-gate hinge end and above the convenience outlet.

If the MD drive motors fail to operate with power on, connect the MD to another outlet and see PWR 24 for the instructions on how to diagnose the failure of the 3880 convenience outlet.

How To Use The MD On The 3880

The design of the MD is such that the MD works the same on all products that use the MD. However, there are a few items that are different when using the MD on the 3880.

Connect The MD

MD 10 shows the physical connection of the MD to the 3880. Basic operating instructions for the MD are on the label on the inside of the MD cover.

Select An Option

After the MD has completed its checkout procedure, it displays a list of ten optional maintenance procedures. These optional procedures are described on MD 40. Press the numeric button on the MD keyboard that compares to the number in front of the procedure to be used.

Continued Frames

Any frame of information with three dots (. . .) at the end of the last line is not a complete statement. Press the Enter key to display the remainder of the statement. The frame that follows may have three dots at the start of the first line.

Frame 1

```
OBSERVE THE METER
WHILE PRESSING THE
POWER SYSTEM SWITCH
TO POWER ON . . .
```

Frame 2

```
.
. . .(POWER   SWITCH
PANEL)
.
```

Probability Code

Some FRU lists contain probability codes. These codes (from blank to 9) are assigned to each FRU.

```
1. B3(B4)L2 MNT CARD 9
2. B1P2 MDA1 CARD 1
3. B1S2 DRR-1 CARD
4. B1T2 DRR-2 CARD
```

The code displays the probability that the indicated FRU corrects the error condition that caused the FRU list. A 9 is the highest probability and a blank is the lowest.

Enter Key And Fwd Key

The 3880 MD programs use the Enter key, not the forward (FWD) key. Use the Enter key to advance the MD display to the next frame.

PF Key

The PF key normally causes the MD to return to the maintenance option list.

REF Light

When the Ref light is on there is additional information available by pressing the Ref key.

REF Key

When displaying primary FRU's, pressing the Ref key will cause secondary FRU's (if there are secondary FRU's) to be displayed.

Unguided Maintenance

When the maintenance procedures become unguided, the following information is displayed on the MD:

Frame 1

```
STOP END OF
GUIDED MAINTENANCE
PROCEDURES.
```

Frame 2

```
REQUEST DIAGNOSTIC
AID (IF NEEDED)
BEFORE CONTINUING
THIS CALL.
```


How To Use The MD On The 3880 MD 20

MD Error Displays

When the maintenance device (MD) is attached to the 3880, various formats are used to display errors to the CE depending on the operational readiness of the 3880 and the progress of the MD itself. The following paragraphs describe the MD error displays that can be received. Refer to the ECI section of the Error Code Manual (ECM) for an index of the errors.

1. When the IPL - Reset pushbutton is pressed, a read-only storage (ROS) checkout of the MD occurs. The MD then loads the functional microcode followed by a 3880 compatible user code. Errors received in this process display one of the following:

MCPC=XX	(MCPC: microcode program check)
MDH=XX	(MDH: maintenance device hardware check)

   where XX is the error code.

2. If the MD checkout and load procedures result in no errors, and a maintenance option is selected, the MD checks out its ability to communicate with the maintenance device adapter (MDA) in the 3880. If an error occurs, the following display is received:

IC=XXXX	(IC: isolation code)

   where XXXX is the error codes from 0100 to 0900.

3. If no errors are detected in the MDA, the 3880 loads microcode in each storage director, one at a time, until the tie breaker determines the storage director to be selected and the following sequence occurs:

   a. Hardcore diagnostics residing in the ROS are executed.

   b. ROS microcode loads track 0 (TRK0) from the 3880 functional diskette into control storage and branches to it.

   c. The remaining hardcore diagnostics resident on the 3880 functional diskette are executed.

   Errors received in this process display:

IML=XX-Y	(IML: initial microcode load)

   where XX is the error code, and
   Y is a 1 if a single storage director fails and a 2 if both storage directors fail.

IML=F5	(IML: initial microcode load)

   where F5 is normal end.

4. When the ROS and the remaining hardcore diagnostics execute error free, the functional microcode is loaded. Errors received in this process give the following display:

SC=XXXX	(SC: symptom code)

   where XXXX is the error code from 2000 to 3FFF for storage director errors, or F000 to FEFF for subsystem storage errors.

5. The CE can invoke diagnostics to check the 3880 hardware. Errors give the following diagnostic isolation code display:

IC=idYYZZ	(IC: isolation code)

   where id is the routine number 70, 71, 72, 78, 79, or 7E; YY is the first error display byte; and ZZ is the second error display byte.

   Note: Errors in the maintenance device-to-storage director communication path in steps 3, 4, or 5 give the following display:

IC=XXXX	(IC: isolation code)

   where XXXX is the errors from 0100 to 0900.

6. The CE can invoke diagnostics to check the subsystem storage. Errors give the following diagnostic isolation code display:

IC=idYYZZ	(IC: isolation code)

   where id is the routine number 50-6B; and YY is the first error display byte; and ZZ is the second error display byte.

7. If extended MDA tests are needed, they occur at the end of the CE call and give the following display:

IC=XXXX	(IC: isolation code)

   where XXXX is the error code.

MD Maintenance Mode

After the MD is initialized, the maintenance mode option list is displayed. This list of the commands is used to start a maintenance action. The following is a description of each option.

0 – End Call

End Call (option 0) is used at the end of any maintenance action (even if the MD is not connected to the 3880 during the maintenance action).

When option 0 is selected, the MD:

1. Lets entry of information about the repair and entry of a message for the next CE.
2. Informs the CE to reset the machine for customer use (set SDs and subsystem storage on line, and so on).

This option is entered automatically at the end of each option 1 or option 5.

Note: This option must be used if the diagnostic mode switches have been set to the diagnostic position.

1 – Start Repair

Start Repair (option 1) is used to isolate, repair, and verify a hardware failure.

When option 1 is selected, the MD:

- Collects symptom information directly from the 3880
- Selects and executes the needed diagnostic programs
- Requests any additional symptom information
- Determines the most probable cause of the failure
- Displays a list of the most probable FRUs that could cause the failure (in the order of probability)
- Directs the repair of the failure
- Verifies that the repair corrected the failure

2 – Continue Repair

Continue Repair (option 2) lets a repair action continue that was interrupted by an:

- MD power-off
- MD IPL

The original repair action may have been started by a:

- Start repair (option 1)
- Symptom analysis (option 4)
- Machine checkout (option 5)

When option 2 is selected, the MD continues the interrupted repair action at the point where the last error was detected.

3 – Display History

Display History (option 3) lets the display of history information collected on preceding maintenance actions by the MD or by CE entry.

When option 3 is selected, as many as 10 history records are displayed sequentially in the order in which they were recorded on the MD diskette.

The main text contains a summary; reference text contains more detail.

4 – Symptom Analysis

Symptom Analysis (option 4) lets the analysis of hardware failures. This option can be used with or without connecting the MD to the 3880.

When option 4 is selected, symptom information must be entered manually by using the MD keyboard.

This option may be used to obtain the FRU list for any given symptom code.

5 – Machine Checkout

Machine Checkout (option 5) lets the verification of 3880 operation after initial installation or an engineering change.

Note: Machine checkout should not be used for normal troubleshooting. For normal troubleshooting you should use option 1 and enter a symptom code. This is very important when you cannot recreate the error condition, since option 1 will show you the most probable failing FRU's for a given symptom code.

6 – Read/Set Switches

Read/Set Address Switches (option 6) aids in the correct setting of the storage director address switches during initial installation.

It reads the settings of:

- Storage director address switches (on CIF cards)
- Diskette load control switches (on MNT card)
- Storage director physical identifier (on DCT card)
- Subsystem storage physical identifier (on CMC1 card)
- Storage size (on CMC1 card)

7 – Feature Change

Feature Change (option 7) lets updates to the configuration record on the MD diskette after a feature change is made to the 3880.

8 – Diagnostic Aids

Diagnostic Aids (option 8) permits the use of special diagnostic aids that are not part of the guided maintenance procedures. These are:

- Select and run device diagnostic (maintenance) programs.
- Set or reset forced logging mode.
- Read the power sense register. See PWR 39 for a description of the power sense register.
- Trace Options

  Read trace status

  Force trace save

  Dump trace to MD diskette

- Read SD status

  The MD displays the following information:

  The most current format 0, 1, 2, 4, 5, or F sense data

  The most current format 3 sense data for the alternate storage director

  The most current IML code

  The contingent connection control block

  The status of the interval timer

  The status of forced logging

- Operator panel lamp test

9 – SD–SD Error Analysis

SD–SD Error Analysis (option 9) is used to analyze information stored in control storage when an error is detected in the SD–SD connection test on the most recent IML. All SD–SD connection testing repairs and verifications need both storage directors offline.

The MD messages that indicate the SD–SD connection test was completed without error are:

- 0000 All OK
- 0202 SDI switches are set incorrectly
- 8000 IML performed on SD1 only
- 0080 IML performed on SD2 only

All other bit combinations are analyzed by option 9 and the MD presents a FRU group for the analyzed failure.

MD Support Mode

Besides the maintenance mode, the Maintenance Device (MD) can also be used to do more involved operations. The MD support mode is the second part of the support package. Support mode offers expanded capabilities in running diagnostics and controlling storage director operations.

Support mode consists of these options:

0 = Disable interval timer

1 = Enable interval timer

2 = Trace

3 = Microcode patch

4 = IML SD with patch

5 = Manual control

6 = Maintenance communication tests

7 = Run diagnostics

X = Exit support mode

Support Mode Requirements

To perform a support mode command, complete the following actions:

1. Connect the MD to the 3880.
2. Ensure power is turned on in the MD and 3880.
3. Install the correct diskettes in the MD and 3880.
4. Press the IPL Reset pushbutton on the MD.
5. Advance the MD display to the maintenance action list. The following frame is displayed:

```
ENTER NUMBER
FROM THE FOLLOWING
LIST TO SELECT A
MAINTENANCE ACTION
```

6. Enter an S. The following frame is displayed.

```
* * SUPPORT AIDS**
ENTER NUMBER
(1 OR 2) TO SELECT
A STORAGE DIRECTOR.
```

7. Enter 1 or 2 to select the desired storage director. The following frame is displayed.

```
M833M01 ENTER NUMBER
FROM THE FOLLOWING
LIST TO SELECT A
SUPPORT ACTION
```

8. Press the Enter key to display the list of support mode options.
9. Enter the number of the desired option. Each option is described on the following pages.

Concurrent Maintenance Operations

A storage director can be used by a channel while it is being selected by the MD. This procedure is not the normal 3880 maintenance strategy, but may be necessary to analyze some storage director problems.

SUPPORT MODE OPTION		CONCURRENT EXECUTION	PAGE
0	Disable interval timer	Yes	MD-60
1	Enable interval timer	Yes	MD-60
2	Trace	Yes	MD-70
3	Microcode patch	No	MD-60
4	IML SD with patch	No	MD-60
5	Manual control	See Note	MD-90
6	Maintenance communication tests	See Note	MD-60
7	Run diagnostics	See Note	MD-60
X	Exit support mode	Yes	MD-60

Note: Some of the commands in this option can be concurrent. See the description of the specific option for details.

Check 1 Error Reporting

When the MD selects a storage director, the normal error reporting path between storage directors is interrupted. A check 1 error in either storage director cannot be reported to the other and error data can be lost.

Error data is held in the failing storage director for about 500 milliseconds. If the alternate storage director cannot respond to the failing storage director in this time limit, the timer on the failing storage director driver–receiver card starts a reset sequence that resets all error data.

Termination

The following terminate support mode:

- Reset key (K/D)
- PF key (K/D)
- IPL Reset Pushbutton (MD)
- X key (K/D)

The Reset and X keys return the MD to the maintenance mode option list.

The PF key returns the MD to the maintenance mode option list if the MD is in the support mode option list when the PF key is pressed.

The PF key returns the MD to the support mode option list if the MD is in a support mode option or support option command.

When the MD is disconnected from the 3880 or the MD IPL Reset pushbutton is pressed, the following operations take place automatically.

- Check 1 is set to halt
- Check 2 is set to bypass
- Address compare sync is set to 0000
- Address compare halt is reset

Options

0 – Disable Interval Timer

The disable interval timer option lets the selected storage director hardware interval timer to be disabled.

When the interval timer is disabled and the channel fails to respond to an inbound tag, the selected storage director will hang with the process LED on.

1 – Enable Interval Timer

The enable interval timer option lets the selected storage director hardware interval timer to continue timing storage director operations.

2 – Trace

Refer to MD 70

3 – Microcode Patch

The microcode patch option permits the microcode to be modified. The basic commands are:

Erase Patch Area
Duplicate Patch Areas SD1 – SD2
Duplicate Patch Areas SD2 – SD1
Duplicate Patch Areas SD1 (ASDM) – SD2 (ASDM)
Duplicate Patch Areas SD2 (ASDM) – SD1 (ASDM)
Display Patch Area
Modify Patch Area

Up to 64 one word control-storage patches can be stored on the maintenance device diskette using this command. Patches can be applied to control storage in the selected storage director by using support mode option 4.

Entering a patch or pressing the Enter key causes the patch area to be displayed. New patches can be added to update the patch display by entering the address and data and pressing the Enter key. Patches can be deleted by entering the address and pressing the Enter key to update the patch display. During these displays, valid subcommands are displayed in reference text.

4 – IML SD With Patch

The IML SD with patch option lets the selected storage director to be loaded with the patched IML code on the MD diskette.

5 – Manual Control

The manual control option is described on MD 90.

6 – Maintenance Communication Tests

The Maintenance Communication tests option permits the selection of 6 maintenance communication tests and 3 controls for running these tests.

The tests are:

- MD adapter test
- SD select test
- Maintenance connection test
- Support CE function test
- SD – SD loop test (both storage directors must be offline)
- MD – MDA Port loop test

The run controls are:

- Normal run
- Loop test and halt on error
- Loop test and bypass error halt

A complete description of the diagnostic tests is in the DC section of the Error Code Manual (ECM).

7 – Run Diagnostics

The run diagnostics option aids in running the following tests:

70 = Function tests
71 = DDCU wrap tests
72 = Miscellaneous routines
75 = T3880B OLT micro support
77 = DDCV wrap (3380)
78 = Electronic wrap
79 = Block wrap
7E = ASDM Function Tests
SS = Read stored storage director (SD) sense data
DD = Device Diagnostics

Note: When running 3350 diagnostic routine A9 a loop run option must be selected.

The parameter entries for the tests are as follows:

- The first and last test to be run
- Channel select for routines 78 and 79.
- Convergent loop. For a description, see the Introduction section of the ECM.

The run options are:

- No loop, halt on error
- No loop, continue on error
- Loop, halt on error
- Loop, continue on error

L1 = Linked Diagnostics – Subsystem Storage Diagnostic command, 'L1' may be entered to run the subsystem storage linked diagnostics 6B, 50-55, 61-63 (see note).

L2 = Linked Diagnostics – Subsystem Storage Diagnostic command, 'L2' may be entered to run the subsystem storage linked diagnostics 6B, 50-55, 57, 61, 58-60, 62-64 (see note).

SD = Single Diagnostic – Subsystem Storage Diagnostic command, The SD command causes a single subsystem storage diagnostic routine to run (see note). The diagnostic routine may be looped.

The run options are:

- No loop, halt on error
- No loop, continue on error
- Loop, halt on error
- Loop, continue on error

1. Enter SD. The following information is displayed:

```
ENTER DIAGNOSTIC
ROUTINE ID
```

2. Enter a two digit diagnostic routine (50-6B) ID (see note). The following information is displayed:

```
ENTER ONE OF THE RUN
OPTIONS (ENTER 0-3)
0 = NO LOOP, HALT ON
    ERROR
```

```
1 = NO LOOP, CONTINUE
    ON ERROR
2 = LOOP, HALT ON
    ERROR
```

```
3 = LOOP, CONTINUE
    ON ERROR
ENTER OPTION:
```

The diagnostic is loaded into control storage.

3. If parameters are to be entered, the following information is displayed:

```
CMD 10 RECEIVED Dyxx
```

expected
xx = diagnostic routine id.

4. When the last parameter is accepted the following is displayed:


```
CMD xx RECEIVED CAxx
```

xx = diagnostic routine id

At the end of the diagnostic either a message indicating no errors were detected, or an error code and sense bytes are displayed.

If looping is requested, the following message is displayed:

```
PRESS PF   RCVD aaaa
TO STOP    RCVD bbbb
TEST       RCVD cccc
           RCVD dddd
```

As diagnostic information is received by the MD, the data bytes are displayed in the next available slot (aaaa, bbbb, cccc, or dddd). If all slots are full, the new information is placed in slot dddd, and all other information is scrolled causing the information at slot aaaa to be lost. If the new information does not change the data being shown, the display is not updated. Press the Enter key to clear all data slots.

If any other key is pressed the diagnostic is stopped and the following is displayed:

```
ENTER ONE
0 - CONTINUE TEST
1 - REQUEST ERROR BYTES
2 - TERMINATE TEST
```

Only routines L1, L2, SD, SS and the device diagnostics are inline tests. See the ECM for a description of routines 70 through 79.

X – Exit Support Mode

The exit support mode option returns the MD to maintenance mode and displays the maintenance option list.

Note: For routines 6B, 50-55, subsystem storage must be offline to the storage director being tested and the diagnostic mode switch for the SD being tested must be set to the diagnostic position. For routines 57-6A subsystem storage must be offline to both storage directors and both diagnostic mode switches must be set to the diagnostic position.

Trace – Support Option 2

Selecting the Trace Program

Entering a 2 while in support mode causes the following command list:

1 = Start Trace
2 = Read Trace Status
3 = Dump Trace to MD
4 = Stop Trace With No Save
5 = Stop Trace With Save (See Caution on MD 80)
6 = Get Sync–ID Address
X = Go to Maintenance Mode List

1 – Start Trace

To start a trace operation, the following must be specified:

- Trace options
- Trace levels
- Trace save conditions

Trace Options

The trace all devices option permits tracing of all devices. The trace single device option limits the trace to a single device.

Device Address

For the trace all devices option, no address is needed. For the trace single device option, the one–byte channel I/O device address is entered.

Trace Levels

The trace level indicates if information being entered into the trace table is collected from the functional microcode blocks, from the channel, or from both the blocks and the channel. The block trace saves the block ID for each trace entry activated during an operation. The channel trace saves the command codes, device addresses, and status bytes involved in the operation.

Selection is made as follows:

- Channel level only
- Block level only
- Both channel and block levels

Trace Save Conditions

The conditions necessary for the trace program to stop and save the machine status are called save conditions. They are:

- Sync/save IDs
- Addresses
- Symptom codes
- Save condition not specified

The maximum number of save conditions are:

- Up to three addresses
- Up to three sync/save IDs and no symptom codes
- Up to three symptom codes and up to two sync/save IDs

Note: Each time a trace is saved the Check 1 light on the 3880 control panel will flash, and an Interface Control Check will be logged at the host. This is the normal trace save operation.

Sync/Save ID

The sync/save ID is a number assigned to microcode modules for which information representing the state of the traced storage director is stored in the state table when a save operation takes place. Each microcode module resides in a functional microcode block.

Addresses

Actual addresses can also be used to stop a trace. However, the address has four hexadecimal digits instead of the normal three used for a sync/save ID. To use an actual address as a sync/save ID, the CE enters 'AAA' when the MD requests the three sync/save ID hexadecimal digits. The MD then requests the four hexadecimal digits of the actual address.

Symptom Codes

A special sync/save ID, 000, is reserved by the functional microcode for use only when symptom codes are entered as save conditions in the trace operation. The sync/save ID 000 can be used as the only condition, or it can be entered with one or two other sync/save IDs.

The special sync/save ID, 000, causes the trace all devices and trace single device options to search for symptom codes supplied by the specify symptom codes option.

Symptom codes are generated by the functional microcode when an error condition is detected during a functional microcode operation. Most of the symptom codes are in the ranges of 0XXX, 2XXX, 3XXX, and FXXX.

The symptom codes are masked, permitting the trace operation to stop on a specific symptom or to stop on the first of a certain type of symptom encountered.

If fewer than three symptom codes are used, X'FF' must be entered in each unused symptom code space and its matching mask byte space. The first byte entered for these parameters contains the eight high–bits and the second byte contains the eight low–bits. The mask byte contains a zero in each bit position for which the matching code bit is ignored. As an example, assume a bus in parity check has caused symptom code printout with code 3B0X. The four parameters to enter for this symptom code are:

3B – Symptom code high

0X – Symptom code low (where X is a digit from 0–F)

FF – Mask byte high

F0 – Mask byte low

The zero in the mask byte low permits the trace to ignore the variable digit X in the symptom code.

To trace a CSR card check (3B38) for channel A, the four parameters to enter are:

3B – Symptom code high

38 – Symptom code low

FF – Mask byte high

FF – Mask byte low

The FFFF mask causes the trace to check every bit in the symptom code. An exact match is needed.

As a last example, a trace for any clock check (3BXX) needs the parameters:

3B – Symptom code high

XX – Symptom code low (where X is a digit from 0–F)

FF – Mask byte high

00 – Mask byte low

Since a clock check is identified by the first byte of symptom code 3B, the second byte is ignored by the mask bytes.

Save condition not specified

If the no save condition is specified, a trace stop must be forced by either of the following option 2 commands:

- Stop Trace With No Save
- Stop Trace With Save

Messages

Error Messages

The following error messages may occur during a trace operation:

- E101 – An invalid trace option has been selected
- E102 – A trace option has been attempted with trace already active
- E103 – An invalid trace level has been selected
- E104 – An invalid trace address has been selected
- E105 – The trace table is invalid

Trace Status Messages

- E180 - the trace function is inactive.
- E181 - the trace table is valid with trace termination by address compare.
- E182 - the trace table is valid with termination by halt and save (AD).
- E184 - the trace table is being updated by an active trace with a trace all device option.
- E185 - the trace table is being updated by an active trace with a trace single device option.

Other Responses

- Dx3D - parameter request
- CA3D - all parameters entered, ready to execute
- CE3D - end of message bytes, routine stopped
- CF3D - end of routine

2 – Read Trace Status

The Read Trace Status command gives two bytes of trace status information (E1XX) and a description of the status.

The trace status messages are:

E180 – The trace function is inactive.

E181 – The trace table is valid with trace termination by address compare.

E182 – The trace table is valid with termination by halt and save 'AD'.

E183 – The valid trace table was destroyed and the dump table valid flag was reset. Running the trace table dump, OLTS causes a unit exception.

E184 – The trace table is being updated by an active trace with a trace all devices option.

E185 – The trace table is being updated by an active trace with a trace single device option.

3 – Dump Trace to MD

The Dump Trace to MD command copies information from the storage director on to the MD diskette. The information is that stored by the storage director during trace and save operations.

For trace formatting and printing, an online test (OLTS) program, T3880D, is used to printout the dynamic trace and state save tables. For an example of a printout, see PDA 110 and 120.

The display shows the transfer is in progress until the response CF3D (End of Message Bytes, Routine Stopped), is received.

4 – Stop Trace With No Save

The Stop Trace With No Save command stops the trace operation without saving any of the trace information. The trace operation stops without involving the storage director.

5 – Stop Trace With Save

If trace is active, this command forces the halt and save operation. The result is the same as if a save condition were detected by the trace program.

If trace is not active, this command forces a save operation. However, in this case, the save command destroys the previous content of the dynamic trace table by overlaying it with hex 'E' throughout.

Warning: Model 21 Only

The use of the MD trace command Stop Trace With Save may cause a subsystem storage initialization, therefore, a possible system IPL. If an IPL is not acceptable, DO NOT use Stop Trace With Save.

6 – Get Sync–ID Address

The Get Sync–ID Address command permits the MD to display the address of a sync ID for use in the address compare sync operation. This operation is a diagnostic that generates a pulse to sync external equipment when the selected event takes place.

The sync ID is always three characters long, so the high byte is 0X and the low byte is XX.

X – Go to Maintenance Mode List

The Go To Maintenance Mode List command returns the MD to the maintenance mode option list.

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Manual Control – Support Option 5

The manual control support option permits the:

- Control of a storage director, step-by-step, through an operation
- Display of registers and storage locations
- Editing of functional microcode

The chart on MD 100 lists all the manual control commands.

Manual Control Status Display

The manual control status display appears as follows on the MD display when manual control is selected.

```
SD=*  CK1=*  CK2=*  R=*
A=****  CK=**
NOT SELECTED
ENTER COMMAND:_____
```

This display is a main text message that contains storage director status information. (Asterisks appear on the display where variable information may be entered or displayed.) The reference text lists the manual commands that can be used.

The manual control status display is the central point of manual control. All manual commands start and end execution at this point. Any other messages that appear are error messages or part of the manual command sequence.

Status Display Field Definition

SD= – Storage Director Selection Field*

If a storage director is selected, the storage director number (1 or 2) appears instead of the asterisk; if not the asterisk is displayed.

CK1= – Check 1 Halt or Bypass*

If the check is set to halt, an H appears instead of the asterisk. If the check is set to bypass, a B appears instead of the asterisk.

CK2= – Check 2 Halt or Bypass*

If the check is set to halt, an H appears instead of the asterisk. If the check is set to bypass, a B appears instead of the asterisk.

R= – Run Control*

See the Run Control entry in the MD Manual Command Descriptions on MD 160.

*A=**** – Instruction Address Register Contents*

See the IAR Alter entry in the MD Manual Command Descriptions.

Note: If the four asterisks appear after a storage director is selected, the storage director is running.

*CK=** – Storage Director Check Condition*

The information used instead of the two asterisks is a bit-significant byte of check conditions in the selected storage director. Bit assignments are:

0 – Not error alert

1 – IML microcode detected error

2 – Selected error alert

3 – Check 2

4 through 7 – Not used

Comment Field

The comment field describes a condition existing on the selected storage director that may influence the execution of the next manual command.

Command Field

The command field contains the words ENTER COMMAND followed by the manual command entered.

Manual Control Requirements

To do a manual command, complete the follow actions:

1. Connect the MD to the 3880.
2. Install the correct diskettes in the MD and 3880.
3. Ensure power is turned on in the MD and 3880.
4. Press the Reset IPL pushbutton on the MD.
5. Advance the MD display to the maintenance action list. The following frame is displayed:

```
ENTER NUMBER
FROM THE FOLLOWING
LIST TO SELECT A
MAINTENANCE ACTION
```

6. Enter an S. The following frame is displayed.

```
* * SUPPORT AIDS * *
ENTER NUMBER
(1 OR 2) TO SELECT
A STORAGE DIRECTOR.
```

7. Enter 1 or 2 to select the desired storage director. The following frame is displayed:

```
M833M01 ENTER NUMBER
FROM THE FOLLOWING
LIST TO SELECT A
SUPPORT ACTION
```

8. Enter a 5 for manual control. The following frame is displayed:

```
SD=* CK1=* CK2=* R=*
A=**** CK=**
NOT SELECTED
ENTER COMMAND:_______
```

In the above display, the asterisk represents variable digits.

9. Enter a manual control command.

Note: The chart on MD 100 lists all the manual control commands.

Manual Control Command Summary

The tables on this page shows the manual control commands that can be performed while the storage director is actively attached to a processor channel. See MD 120 for the description of the manual control commands.

OPERATION	COMMAND FORMAT	CONCURRENT EXECUTION	COMMENTS
Address register (IAR) set	A****	No	
ASDM control Store -Display -Alter	AMCS AAAA AAAA DDDD	No No No	
Display ASDM external indirect registers	AME	No	
Display ASDM internal registers	AMI	No	
Communication buffer -Display -Alter	ADCB AA AA DD	No No No	This buffer is between the storage directors in a caching subsystem.
Alter/display subsystem address register	SSAR	No	
Subsystem storage external indirect registers -Display -Alter	ADRG AAAA AAAA DDDD	No No No	
ASDM reset	AMR	No	
Alter/display subsystem storage	ADSS	No	
Check registers - display (SDM)	CK	No	
Check 1 H/B - change	CK1	Yes	Active until the storage director is deselected
Check 2 H/B - change	CK2	Yes	Active until the storage director is deselected
Control storage (SDM) -Display -Alter	CS AAAA AAAA DDDD	No No No	
Display access control switch	DACS	No	
Display ASDM check register	AMCK	No	
Display sense buffer	DSB	No	
External register -Display -Alter	E NNN NNN DD	No No No	
Halt of address compare -Set (See Note) -Reset	H**** H	Yes	Active until the storage director is deselected

Note: If an address compare halt is set for an address between X'0000' and X'7FFF', the storage director clock stops at the halt address plus 3. If the address is above X'7FFF', the storage director clock stops at the halt address plus 2.

OPERATION	COMMAND FORMAT	CONCURRENT EXECUTION	COMMENTS
IML ASDM	IMLAM	No	
IML SD with timeout	IML	No	
IML SD* without timeout	IMLT	No	
IML SD* without reset	IMLW	No	
Internal registers (SDM) -Display -Alter	I AA AA DD	No No No	
Loop IML	LOOP	No	
Maintenance operation test	M****	No	
MDA register - display	MDA	Yes	
Null-no command	Enter key only	No	
Patch ASDM control store	PAM	No	Permits control store patches to the selected SD's ASDM from the microcode patch area on the MD diskette.
Patch control storage from MD diskette (SDM)	P	No	Permits control store patches to the selected SD's SDM from the microcode patch area on the MD diskette.
PSW - Display	PSW	No	
Reset - Check 2 - General - MD adapter - Storage director	RCK2 RESET RMDA RSD	No No Yes No	
Run ASDM	RAM	No	Starts execution of the selected SD's ASDM
Run SD clock (see note) - Start - Stop - Step	 R RO R (1-9)	 No No No	
Run single diagnostic	SDIAG	No	Subsystem Storage must be offline to both SDs
Run linked diagnostics	LD1 LD2	No No	Subsystem Storage must be offline to both SDs LD1 runs routines 6B, 50-55, 61-63 LD2 runs routines 6B, 50-55, 57, 61, 58-60, 62-64
Storage director control - Select - Deselect	 SD (1 or 2) SD	 Yes Yes	
Sync on address compare - Set - Reset	 S**** S	 Yes Yes	Active until the storage director is de-selected

Load the Storage Director

Before starting the initial microcode load (IML) operation, complete the following actions. (These actions are only examples of how to use manual control).

1. Connect the MD to the 3880.
2. Ensure power is turned on in the MD and the 3880.
3. Install the correct diskettes in the MD and 3880.
4. Press the Reset IPL pushbutton on the MD.
5. Advance the MD display to the maintenance action list. The following frame is displayed:

```
ENTER NUMBER
FROM THE FOLLOWING
LIST TO SELECT A
MAINTENANCE ACTION.
```

6. Enter an S. The following frame is displayed.

```
** SUPPORT AIDS **
ENTER NUMBER
(1 OR 2) TO SELECT
A STORAGE DIRECTOR.
```

7. Enter 1 or 2 to select the desired storage director. The following frame is displayed:

```
M833M01 ENTER NUMBER
FROM THE FOLLOWING
LIST TO SELECT A
SUPPORT ACTION.
```

8. Enter a 5 for manual control. The following frame is displayed:

```
SD=* CK1=* CK2=* R=*
A=**** CK=**
NOT SELECTED
ENTER COMMAND:_________
```

9. Enter SD1 or SD2 to select desired storage director. Example: SD1

```
SD=1 CK1=* CK2=* R=*
A=**** CK=**
ENTER COMMAND
```

10. Enter IML and wait for the following display:

```
SD1 IML IN PROGRESS
 .
 .
 .
```

11. The following is displayed when the IML operation is completed:

```
IML ENDED WITH
IML CODE = XX
```

Note: The XX represents any hexadecimal digit. Normal end is F5.

12. Press the Enter key to return to the manual control status display.

Note: To IML SD with Patch, see option 4 on MD 60.

Display Control Storage Location

To display control storage location 1F56:

1. Do steps 1 through 9 of 'Load the Storage Director'.
2. Enter CS and wait for the following display:

```
ENTER ADR AND DATA
(AAAA DDDD) TO
CHANGE CS.  ENTER
ADR ONLY TO DISPLAY.
```

3. Enter 1F56 and wait for the following display:

```
1F50=nnnn 1F54=nnnn
1F51=nnnn 1F55=nnnn
1F52=nnnn 1F56=nnnn
1F53=nnnn 1F57=nnnn
```

Note: The n represents data; 1F56 is in the group shown.

Press the Enter key to display the next eight control storage locations.

4. Press the PF key to return to the manual control status display.

Manual Control Examples MD 110

Manual Control Command Descriptions

All MD manual control commands are described below in the same sequence as they are listed in the chart on MD 100. During Alter/Displays, valid sub-commands are listed in the reference text.

A**** – Address Register (IAR) – Set

The A**** command sets the instruction address register in the selected storage director to the value in the **** field of the command entry.

To use this command:

1. Verify that manual control needs have been met.
2. Enter A****, where **** is the desired instruction address register (IAR) value. This new address is displayed in the manual control status display.

AMCS – Alter/Display ASDM Control Store

This command is valid only for a Model 21.

This command alters and displays the selected storage directors ASDM control store. The subcommands and displays are the same as the CS command. The address range of the ASDM is X'0000' to X'0FFF'. The MD will convert the ASDM address to the corresponding SDM control store address.

AME – Display ASDM External Indirect Registers

This command is valid only for a Model 21.

This command displays the external indirect registers of the selected storage directors ASDM. When the command is entered, all registers are displayed.

AMI – Display ASDM Internal Registers

This command is valid only for a Model 21.

This command displays the selected storage directors ASDM internal registers. The displays are the same as the I command without alter.

ADCB – Alter/Display Communication Buffer

The ADCB command permits entry of the following subcommands:

- AA

  Display communication buffer at address AA

- AA DD

  Alter communication buffer at address AA to DD and display

- Enter key only

  Display the next screen of the communication buffer

- PF key only

  Return to manual control status display.

SSAR – Display/Alter Subsystem Address Registers

The SSAR command lets subsystem address registers to be displayed or altered.

To use this command:

1. Verify that manual control needs have been met.
2. Enter SSAR. The following display will appear.

```
1 - DISPLAY UPPER PATH
2 - DISPLAY LOWER PATH
3 - ALTER UPPER PATH
4 - ALTER LOWER PATH
```

3. If a display is requested, the SSAR value is presented as follows:

```
UPPER PATH SSAR
XXXXXX
```

or

```
LOWER PATH SSAR
XXXXXX
```

4. If altering is requested, the MD prompts the user to enter six hex digits of data. The MD then displays SSAR's old and new values.

```
UPPER PATH SSAR OLD
XXXXXX
UPPER PATH SSAR NEW
YYYYYY
```

ADRG – Alter/Display Subsystem Storage Registers

The ADRG command permits the entry of the followings commands:

- NNNNNNN

  Display register NNNNNNN

- NNNNNNN DD

  Alter register NNNNNNN to DD

- Enter key only

  Display the next external register group

- PF key

  Return to manual control status display.

The contents of the subsystem storage registers are displayed in main text. Only registers that can be read are displayed. During these displays, valid subcommands are listed in reference text along with a description of register names.

AMR – ASDM Reset

This command is valid only for a Model 21.

This command sends a reset to the selected storage director's ASDM.

ADSS – Alter/Display Subsystem Storage

The ADSS command lets any subsystem storage address to be displayed or altered using the MD.

To use this command:

1. Verify that manual control needs have been met.
2. Enter ADSS. The MD will then request the subsystem storage address as 6 hex digits. If no address is entered, the MD will display the contents of the next sequential subsystem storage address (address 000000 if this is the first request).
3. If a subsystem storage address is entered, the following display is presented:

```
ENTER DATA TO ALTER
AS 32 HEX DIGITS,
OR ENTER TO DISPLAY
```

4. Sixteen hexadecimal bytes may be entered to alter the requested subsystem storage location. If no data is entered, the subsystem storage is displayed.
5. If a subsystem storage display is requested the following screen is shown:

```
AAAAAA
DDDDDDDDDDDDDDDDDDDD
DDDDDDDDDDDD
```

   Where AAAAAA is the subsystem storage address, and DD is the contents of this address.

6. If data is entered to alter subsystem storage, the following displays are presented:

```
AAAAAA
DDDDDDDDDDDDDDDDDDDD
DDDDDDDDDDDD (OLD)
                    ...
```

```
AAAAAA
DDDDDDDDDDDDDDDDDDDD
DDDDDDDDDDDD (NEW)
```

   Where AAAAAA is the subsystem storage address being altered, DD (OLD) is the former contents of this address, and DD (NEW) is the new contents.

7. This command will repeat until the PF or reset key is pressed to return to the status display.

CK – Check Registers – Display

The CK command displays the check and FRU registers in the selected storage director.

To use this command:

1. Verify that manual control needs have been met.
2. Enter CK to display check and FRU registers in the selected storage director.

```
CHK REGS=XX XX XX
FRU REGS=XX XX XX XX
SC=XXXX
```

Note: The X represents hexadecimal data. The symptom code (SC) is only given if the error alert latch is active.

CK1 – Check 1 Halt/Bypass – Change

The CK1 command reverses the check 1 operation on the selected storage director from halt to bypass or bypass to halt (see the CK1=* field in the manual control status display). This command also sets the check 2 operation to bypass (see the CK2=* field in the manual control status display).

To use this command:

1. Verify that manual control needs have been met.
2. Enter CK1.

CK2 – Check 2 Halt/Bypass – Change

The CK2 command reverses the check 2 operation on the selected storage director from bypass to halt or halt to bypass (see the CK2=* field in the manual control status display). This command also sets the check 1 operation to halt (see the CK1=* field in the manual control status display).

To use this command:

1. Verify that manual control needs have been met.
2. Enter CK2.

CS – Control Storage – Display/Alter

The CS command allows entry of the following subcommands:

- AAAA

  Display control storage location

- AAAA DDDD

  Alter control storage location AAAA to DDDD and display

- Enter key only

  Display the next eight control storage locations

- PF key

  Return to manual control status display

Control storage locations are displayed (in main text) in blocks of eight addresses always starting with an address that is a multiple of eight. During these displays, the valid subcommands are listed in reference text. Entry of an invalid subcommand causes a return to the manual control status display.

Attempting to alter or display an invalid control storage location causes a storage director and/or maintenance device adapter check.

To use this command:

1. Verify that manual control needs have been met.
2. Enter CS. The following information is displayed:

```
ENTER ADR AND DATA
(AAAA DDDD) TO
CHANGE CS. ENTER
ADR ONLY TO DISPLAY
```

3. Enter desired address and, if needed, data according to the given format.
4. Press only the Enter key to page forward eight storage locations.
5. Press the PF key to return to the manual control status display.

DACS – Display Access Control Switch

The DACS command displays the value of the GTS register and the port number.

To use this command:

1. Verify that manual control needs have been met.
2. Enter DACS. One of the following displays will appear.

```
ACCESS CONTROL
SWITCH VALUE IS XX
ACS IS UNOWNED
```

```
ACCESS CONTROL
SWITCH VALUE IS XX
ACS OWNED BY PORT YY
REQUESTING PORT
```

```
ACCESS CONTROL
SWITCH VALUE IS XX
ACS OWNED BY PORT YY
NOT REQUESTING PORT
```

Where XX is the hex value of the GTS, and YY is the port number.

For additional information on the Access Control Switch (ACS) see the SENSE section.

3. Press the PF key to return to the manual control status display.

AMCK – Display ASDM check register

This command is valid only for a Model 21.

This command displays the check register (CAAJCK) from the selected storage director's SDM.

DSB – Display Sense Buffers

The DSB command displays the value of the sense buffers.

To use this command:

1. Verify that manual control needs have been met.
2. Enter DSB.

```
ENTER SENSE BUFFER
TO BE DISPLAYED
(0 - 8).
(0 - 33).      (Not Model 21)
```

3. Enter the decimal number of the sense buffer you want displayed, and the following message will be displayed:

```
SENSE BUFFER XX:
YYYYYYYYYYYYYYYY
YYYYYYYYYYYYYYYY
YYYYYYYYYYYYYYYY
```

Where XX is the sense buffer being displayed, and YY....YY are the 24 sense bytes.

4. Press the Enter key to return to the ENTER SENSE BUFFER display.

5. Press the PF key to return to the manual control status display.

E – External Registers – Display/Alter

The E command lets the entry of the following subcommands:

- NNN

  Display external register NNN
- NNN DD

  Alter external register NNN to DD and display
- Enter key only

  Display the next external register group
- PF key

  Return to manual control status display

The contents of the external registers are displayed (in main text) in groups of 12 registers. Only readable registers are displayed. During these displays, valid subcommands are listed in reference text along with a list of all valid register names.

Entry of any invalid subcommand causes a return to the manual control status display.

To use this command:

1. Verify that manual control needs have been met.
2. Enter E. The following information is displayed:

```
ENTER EXT REG NAME
ADD DATA (NNN DD) TO
CHANGE.  ENTER NAME
ONLY TO DISPLAY
```

3. Enter desired register name and, if needed, data according to the given format.
4. Press the Enter key to display the next group of registers.
5. Press the PF key to return to the manual control status display.

H**** – Halt on Address Compare

The H**** command can be entered in either of the following forms:

- H****

  Set address compare halt
- H

  Reset address compare halt

When an address compare halt is activated, the following message is displayed:

```
WAITING FOR ADDRESS
COMPARE HALT
.
.
```

This display appears when the selected storage director is running after completion of any other manual command. The message display continues until either an address compare occurs or the Enter key is pressed.

To use this command:

1. Verify that manual control needs have been met.
2. Enter H****, where **** is the desired halt address.

   The halt address id displayed as additional text in the manual control status display.

```
SD=X CK1=X CK2=X R=X
A=XXXX CK=X H=****
.
.
```

Note: The X represents variable data.

3. Enter H to remove the address compare halt from the display.

IML – IML SD* With Timeout

The IML command starts the IML sequence on the selected storage director and displays the following message:

```
SD-* IML IN PROGRESS
.
.
.
```

This display remains until either the IML operation is completed or the Enter key is pressed. The IML completion code (IML=**) is then displayed. The Enter or PF key must be pressed to return to the manual control status display.

To use this command:

1. Verify that manual control needs have been met.
2. Enter IML.

   Do not press any key on the maintenance device keyboard while the IML operation is in progress. This causes a premature end of the IML sequence and a storage director and/or maintenance device adapter check. The ENTER key ends the IML sequence if it hangs.

   An IML code of X'F5' shows normal completion.

IMLAM

This command is valid only for a Model 21.

This command loads the selected storage director's ASDM with the initial microcode. After the command is sent the following is displayed:

```
SD* ASDM IML IN
PROGRESS
```

When the load is complete, one of the following messages will be displayed:

```
SD* ASDM IML
COMPLETE
```

or

```
SD* ASDM IML
FAILED, CAAJCK=XX
```

IMLT – IML SD* Without Timeout

The IMLT command does the same function as the IML command except that no IML timeout can occur. Use this command only to diagnose IML problems.

To use this command:

1. Verify that manual control needs have been met.
2. Enter IMLT.

IMLW – IML SD* Without Reset

The IMLW command carries out the same function as the IML command except that IMLW does not allow a reset at the completion of IML.

To use this command:

1. Verify that manual control needs have been met.
2. Enter IMLW.

I – Internal Register – Display/Alter

The I command allows the entry of the following subcommands:

- AA

  Display internal register AA
- AA DD

  Alter internal register AA to DD and display
- Enter key only

  Display the next internal register group
- PF key

  Return to manual control status display

The contents of the internal registers are displayed (in main text) in groups of eight registers. During these displays, valid subcommands are listed in reference text. Entry of an invalid subcommand causes a return to the manual control status display.

Altering any internal register used by the functional microcode that supports manual commands can cause a failure of this or any following manual command.

To use this command:

1. Verify that manual control needs have been met.
2. Enter I. The following information is displayed.

```
ENTER ADR AND DATA
(AA DD) TO CHANGE
INTERNAL REG. ENTER
ADR ONLY TO DISPLAY
```

3. Enter desired address and data, if needed, according to the given format.
4. Press the Enter key to display the next internal register group.
5. Press the PF key to return to the manual control status display.

Loop – Loop IML

The Loop command loops the IML operation on a selected storage director. The IML operation loops until any MD function key is pressed.

To complete this command, press any MD function key. This causes an IML terminated message to be displayed. Press the Enter key to return to the manual control status display.

To use this command:

1. Verify that manual control needs have been met.
2. Enter LOOP.

M**** – Maintenance Operation Test

The M**** command sends two bytes (****) of test data to the diagnostic controller in the selected storage director. The bytes should be returned to the maintenance device from the storage director.

When this command is entered, the following message is displayed.

```
WAITING FOR SD-*
RESPONSE
.
.
```

This message display remains until a response is received from the selected storage director or the Enter key is pressed. The storage director response is displayed when it is received. The Enter key must then be pressed to return to the manual control status display.

To use this command:

1. Verify that manual control needs have been met.
2. Enter M****, where **** is any four hexadecimal digits. This command sends two bytes (****) of test data to the diagnostic controller in the selected storage director. The bytes should be echoed back to the maintenance device.

The storage director response is displayed when it is received. The ENTER key must then be pressed to return to the manual control status display.

MDA – MDA Register – Display

The MDA command displays the maintenance device adapter control and status registers.

To use this command:

1. Verify that manual control needs have been met.
2. Enter MDA. The MDA and Status registers are displayed.

Null – No Command

The Null command is entered by pressing the Enter key with no entry in the command entry field of the manual control status display. The function of this command relies on the contents of the R=* field in the manual control status display. (See the R* command.)

To use this command:

1. Verify that manual control needs have been met.
2. Press the Enter key.

   Each time the Enter key is pressed, the clock steps * times, where * is the digit in the R field.

PAM – Patch ASDM Control Store

This command is valid only for a Model 21.

The PAM command applies control store patches to the selected storage director's ASDM from the microcode patch area on the MD diskette. This patch area may be modified by use of the Microcode Patch Function (S3).

To use this command:

1. Verify that manual control needs have been met.
2. Enter PAM.

P – Patch Control Storage From MD Diskette

The P command applies control storage patches to the selected storage director from the microcode patch area on the MD diskette. This patch area can be changed by option S3 (microcode patch).

To use this command:

1. Verify that manual control needs have been met.
2. Enter P.

PSW – Program Status Word – Display

The PSW command displays the instruction address register (IAR), the channel condition register (CCR), and internal register group (IRG) contents for interrupt levels 1, 2, and 3 on the selected storage director. The L=* field shows the most recently active interrupt level (on the basis of the interrupt level register content).

To use this command:

1. Verify that manual control needs have been met.
2. Enter PSW.

RCK2 – Reset Check 2

The RCK2 command resets any check 2 condition on the selected storage director.

To use this command:

1. Verify that manual control needs have been met.
2. Enter RCK2.

Reset – Reset General

The Reset command resets the selected storage director and then the maintenance device adapter. The command also de-selects the storage director.

To use this command:

1. Verify that manual control needs have been met.
2. Enter RESET.

RMDA – Reset MD Adapter

The RMDA command resets the maintenance device adapter and de-selects the selected storage director.

To use this command:

1. Verify that manual control needs have been met.
2. Enter RMDA.

RSD – Reset Storage Director

The RSD command resets the selected storage director.

To use this command:

1. Verify that manual control needs have been met.
2. Enter RSD.

RAM – Run ASDM

This command is valid only for a Model 21.

This command starts execution of the selected storage director's ASDM.

To use this command:

1. Verify that manual control needs have been met.
2. Enter RAM.

R* – Run SD* Clock

The R* command lets entry of the following subcommands:

- R

  Start the selected storage director

  Note: If the interval timer is not running when this command is used it may cause a check 1 condition. (To enable the interval timer see MD 60).

- RO

  Stop the selected storage director

- R*

  Run the selected storage director

The * field must contain a single decimal digit. This command also sets the R=* field in the manual control status display.

To use this command:

1. Verify that manual control needs have been met.
2. Enter one of the following
   - R – to start the selected storage director
   - RO – to stop the selected storage director
   - RX – to run the selected storage director, where X is a single hexadecimal digit representing the number of cycles to be run

Note: Any time the storage director clock is stopped a Reset command (see MD 150) must be executed prior to starting the storage director clock again.

SD* – Storage Director Control

The SD* command lets entry of the following subcommands:

- SD

  De-select both storage directors

- SD1

  Select storage director 1

- SD2

  Select storage director 2

To use this command:

1. Verify that manual control needs have been met.
2. Enter one of the following
   - SD
   - SD1
   - SD2

S**** – Sync on Address Compare

The S**** command lets entry of the following subcommands:

- S****

  Set address compare sync at address ****

- S

  Reset address compare sync

To use this command:

1. Verify that manual control needs have been met.
2. Enter S****, where **** is the desired sync address.

   The sync address is displayed as additional text in the manual control frame.

   Note: The sync pulse is available at 01A-B1Q2D12.

```
.
SD=X CK1=X CK2=X R=X
A=XXXX CK=XX S=****
.
```

   Note: The X represents variable data.

3. Enter S to remove the address compare sync address from the display.

Bypass IML Error Halt

1. Verify that manual control needs have been met (see MD 90).
2. Enter IML and wait for the IML error halt display.
3. Press the ENTER key. The following frame is then displayed:

```
SD=1 CK1=H CK2=B R=X
A=XXXX CK=XX

ENTER COMMAND:
```

4. Enter RSD (resets storage director).
5. Enter A0008 (sets IAR to 0008).
6. Enter R to start the storage director. Wait until the wait indicator on the operator panel is lighted.
7. Return to main menu (press RST key).
8. Enter S (support mode) and select the storage director under test.
9. Enter 7 (run diagnostics). The following frame is then displayed:

```
RUN DIAGNOSTICS
ENTER TWO CHARACTER
ROUTINE ID FROM THE
FOLLOWING LIST:
```

10. Enter 70 (function tests).
11. Without performing an IML, select the test to be looped from the error condition diagram description of the IML code being analyzed.

    Note: When running routine 70 with IML error halt bypassed, a check 1 condition may result. If it does, put the storage director in check 1 bypass mode and return to step 1.

Loop IML Failure

To loop an IML failure:

1. Verify that the manual control needs have been met (see MD 90).
2. Enter LOOP. The MD initiates the IML procedure to the selected storage director when it sensed the storage director clock has stopped or the IML Select line is deactivated. If the error continues, an effective loop is created from the start of IML to the error address.

Loop On An Address

To loop on an address:

1. Verify that the manual control needs have been met (see MD 90).
2. Enter H****, where **** is the last address of the desired loop.
3. Enter LOOP.The MD now loops from the start of the IML operation to the specified address.

Loop Check 1 Clock Stop Error

To loop check 1 stop errors, perform the same operations as those to loop an IML failure.

Loop Single Diagnostic

1. Verify that the manual control needs have been met (see MD 90).
2. Enter the SDIAG command and follow the procedure for running a single diagnostic (see MD 60 - run diagnostics - SD command).
3. When Run control is requested, MD run option 2 or 3 must be selected to setup the MD for looping.
4. Enter parameters if needed, as described in running a single diagnostic (see MD 60 - run diagnostics - SD command).

    Note: Using diagnostic parameters (as described in the ECM manual), the 3880 may be instructed to loop a specific diagnostic test. When this is done, MD run option 2 or 3 must be selected to inform the MD of the looping operation.

Run Linked Diagnostics

1. Verify that the manual control needs have been met (see MD 90).
2. Enter LD1 or LD2 (see MD 60 - L1 and L2 commands.
    - LD1 runs routines 6B, 50-55, 61-63
    - LD2 runs routines 6B, 50-55, 57, 61, 58-60, 62-64

CTL-I Checkout Requested By Drive

This program is run at the request of a drive maintenance analysis procedure (MAP) that suspects a control interface (CTL-I) failure.

1. Ensure that the storage director to be used is offline. Set all channel switches for the storage director to the disable position on the 3880 operator panel.
2. Connect the MD to the 3880 as shown on MD 5.
3. Power on the MD.
4. Insert the 3880 MD diskette into the MD and press the IPL-reset pushbutton.
5. When the message:

   ```
   MD DISKETTE LOADED
   FOR 3880
   .
   .
   ```

   is received, press the Enter key.
6. Continue pressing the Enter key until:

   ```
   ENTER THE DATE
   .
   .
   .
   ```

   is received. Enter the date.
7. Enter the 3880 machine serial number located on the frame under the logic gate.
8. The following frame should be then displayed:

   ```
   ENTER NUMBER
   FROM THE FOLLOWING
   LIST TO SELECT A
   MAINTENANCE ACTION
   ```

   Enter an 8 to select Diagnostic Aids (option 8).
9. Select Run Diagnostic Program from the Diagnostic Aids list (option D).
10. Enter the routine number and the run parameters when requested by the MD. Refer to the drive MIM for error-stop description and maintenance actions.
11. At the end of the call, ensure that the control interface diagnostic is no longer executing.
12. Disconnect the MD from the 3880 if no further actions are desired.

CHL-I – Routine 75

Routine 75 runs with online test T3880B (OLT-B) to test certain lines in the channel interface (CTL-I).

1. The MD must be connected to the 3880 (see MD 5) and the MD IPL function completed.
2. In order to run a diagnostic routine, option 8 (Diagnostic Aids) must be selected from the maintenance action list. To get this list:
   a. Press the IPL Reset pushbutton on the MD and proceed to the maintenance action list.
   b. If a maintenance action has already been selected, press the PF key. The MD then displays the list.
3. Select Run Diagnostic Program from the Diagnostic Aids list.
4. Enter the routine number (75) when requested. This routine has no run parameters.
5. Perform an initial microcode load IML on the storage director by turning power off, then on to ensure that routine 75 is no longer executing at the end of the call.

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