IBM® Maintenance Library

3830 Storage Control, Model 2

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3830-2

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SAFETY

Be constantly aware of hazardous situations when working on the 3830-2 Storage Control. Take time to review the CE safety practices listed below which have been reprinted from the pocket-size card available from Mechanicsburg (Order No. S229-1264).

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects. Pull tongue forward.
3. Loosen Clothing – Keep Victim Warm
   Take care of these items after victim is breathing by himself or when help is available.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on his back immediately.
2. Clear throat of water, food, or foreign matter.
3. Tilt head back to open air passage.
4. Lift jaw up to keep tongue out of air passage.
5. Pinch nostrils to prevent air leakage when you blow.
6. Blow until you see chest rise.
7. Remove your lips and allow lungs to empty.
8. Listen for snoring and gurglings – signs of throat obstruction.
9. Repeat mouth to mouth breathing 10-20 times a minute. Continue rescue breathing until victim breathes for himself.

Thumb and finger positions

Final mouth-to-mouth position

CE-MLM Feedback forms are provided at the front of Volume R01 for reader comments. If the forms have been removed, send your comments to the address below.

This manual was prepared by the IBM Systems Development Division, Product Publications, Department G24, San Jose, California 95114.

CONTENTS

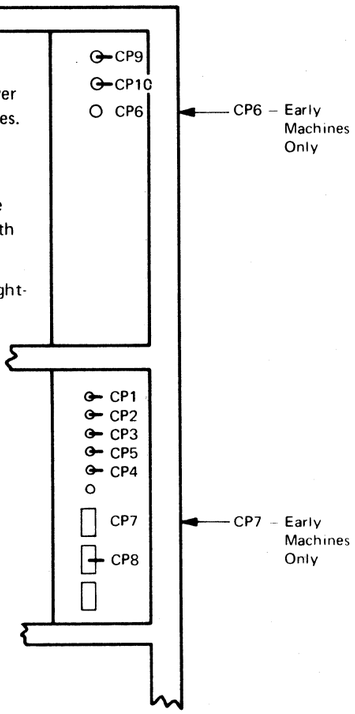
Power

MACHINE IDENTIFICATION

Early 3830-2 Storage Control Units contained some power components that have been discontinued in later machines. The changeover took place with serial numbers 30000 (U.S.A.), 73-81000 (Germany), 97-20000 (Japan).

In this section, information pertaining specifically to one level or the other is labeled "only for early machines (with CP7)" or "only for late machines (without CP7)".

Machines can be identified (early/late) by opening the right-front cover and observing the circuit protectors (CPs) as shown here.



POWER SUPPLY PRINCIPLES

- Solid state sequencing with voltage sensing.
- Relays and contactors control and distribute power.
- Control modules are powered up sequentially.
- MPL file is powered up by control unit and is powered up and down by program control after system is operating.
- Power is shut down if line disturbances are sufficient to affect data integrity.

MAJOR COMPONENTS

Major components are power sequence box, primary power control box, power supplies, and regulators.

Power Sequence Box (YB011)

In this enclosure reside all control circuit components:

1. Time-elapsed meter and associated components.
2. Power system fault-indicating lights and Test/Reset switch.
3. Control circuit logic cards.
4. Control circuit 12V regulator.
5. Control circuit logic board.
6. Control relays.

Primary Power Control Box (YB011)

This compartment contains ac control components:

1. Circuit breakers and circuit protectors.
2. Main distribution circuit breakers.
3. Control unit main ac contactor.
4. MPL file control ac relay.

Power Supplies and Regulators

Major power supplies and regulators are located in the front of the control unit.

1. Two bulk supplies (one in later machines).
2. DC regulators.
3. DC circuit protectors.

BASIC POWER SEQUENCING CONCEPTS

Power Failure Sensor

The power failure sensor determines if the power line disturbance (PLD) ride-through capability has been exceeded and if all voltages are present.

The sensor monitors all bulk supply and bias supply output voltages. The outputs form an OR which indicates when any of the voltages dip below the specified tolerance levels. Any voltage not within tolerance powers down the the subsystem.

A 12-second delay degates the effect of PLD sensing during power on.

Indicator Lights

Three indicators signal fault conditions in the power area:

1. Power Supply Failure – CP tripped.
2. Power Supply Thermals.
3. Gate and Memory Thermals.

Indicators are latched on by fault signals. The first latch set degates the other latches. Latches are reset manually (Test/Reset switch) or by logic during power on.

MPL File Power Control

AC and dc voltages to the MPL file are switched by relays. AC is supplied by energizing K10 and K11. DC (+24, +6, and –3V) is provided by energizing K6. These three relays are energized by a control unit signal (+3V MPL File On, YB148) to the power sequence logic. This signal is activated during the power-on sequence (MPL) or during execution of program instructions requiring MPL file operation. The MPL file is powered down when not in use.

Sequencing of Logic Gate Voltages

Initially the following power supplies turn on:

1. PS5 (–3/+1.25V)
2. PS7 (–3V/+1.25V)
3. PS3 (–36V, early machines only)

Then power to the memory panel B3 (W1 in logics) is applied in the following sequence:

1. PS7 (–3/+1.25V on initially)
2. PS6 (+3.5V)

Finally +6V (PS 3) is turned on to the I/O channel.

Reset Signal

The function of this circuit is to check that the machine completes the power up sequence.

This check is achieved by starting a timer (K1 hold delayed by 12 seconds) with the pick (power-on) signal and checking against selected points in the sequence circuit. If any of the check signals have not changed to their normal on state in the timing period, the 3830-2 is reset to the off condition.

This circuit will also initiate power down sequence, after the machine is fully sequenced up, if a check point reverts to its off state.

The circuit resets to the normal off condition ready for another start cycle once the pick signal is removed.

Power-On Anti-Recycle Circuits

The anti-recycle latch prevents repeated unsuccessful power-on attempts by the 3830-2. Power on is unsuccessful if a voltage is low, a thermal is open or a CP is tripped.

The anti-recycle latch is initially reset off when K1 is down and no power-on signal is available from the stepping switch. When the switch advances to select the 3830-2, K1 is picked to bring up power and set the anti-recycle latch. If a fault now occurs, K1 drops providing the final ANDing condition with the anti-recycle latch to hold K1 driver cut off.

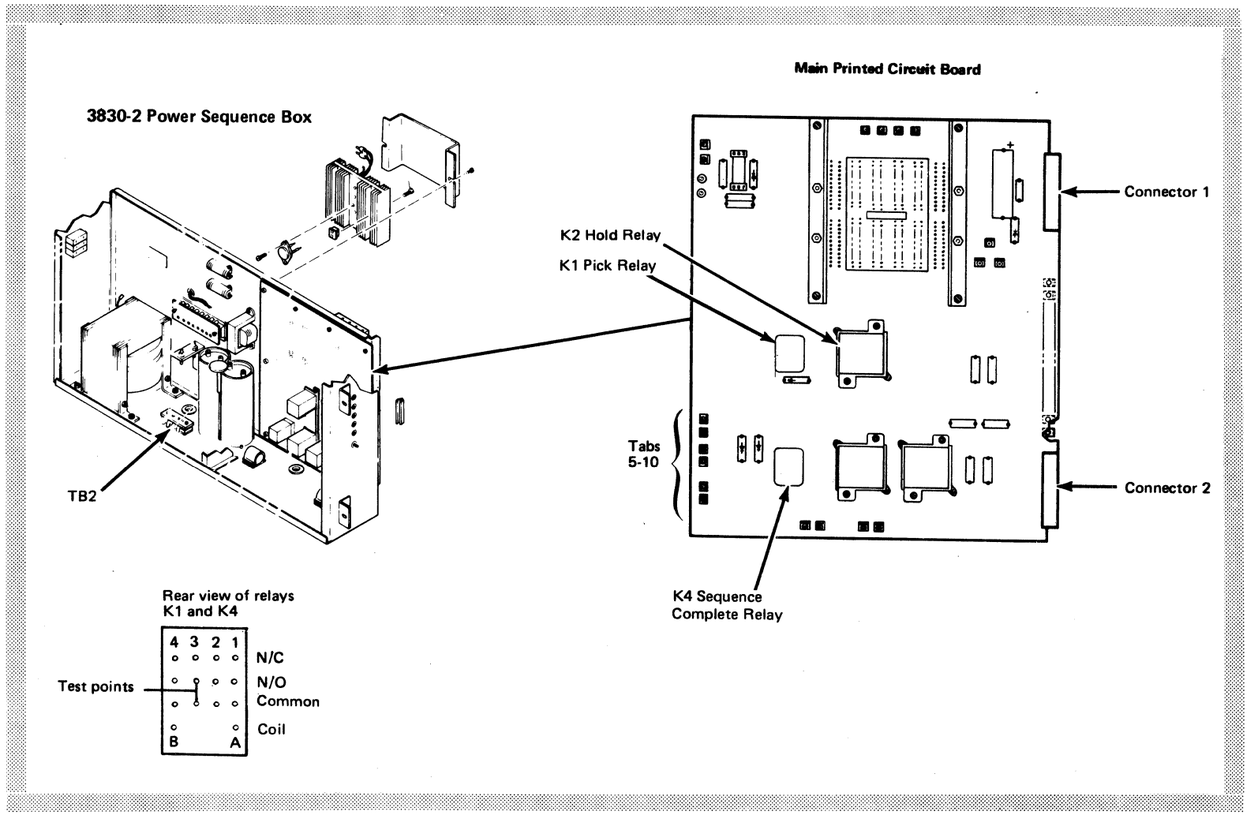
If a tripped CP prevented power-up, reset the CP and try to power up. To reinitiate power up, move Mode switch to a CE position and operate CE panel Power switch. With ac power on, the 3830-2 signals the system to advance the stepping switch to the next subsystem. Now position mode switch to Normal.

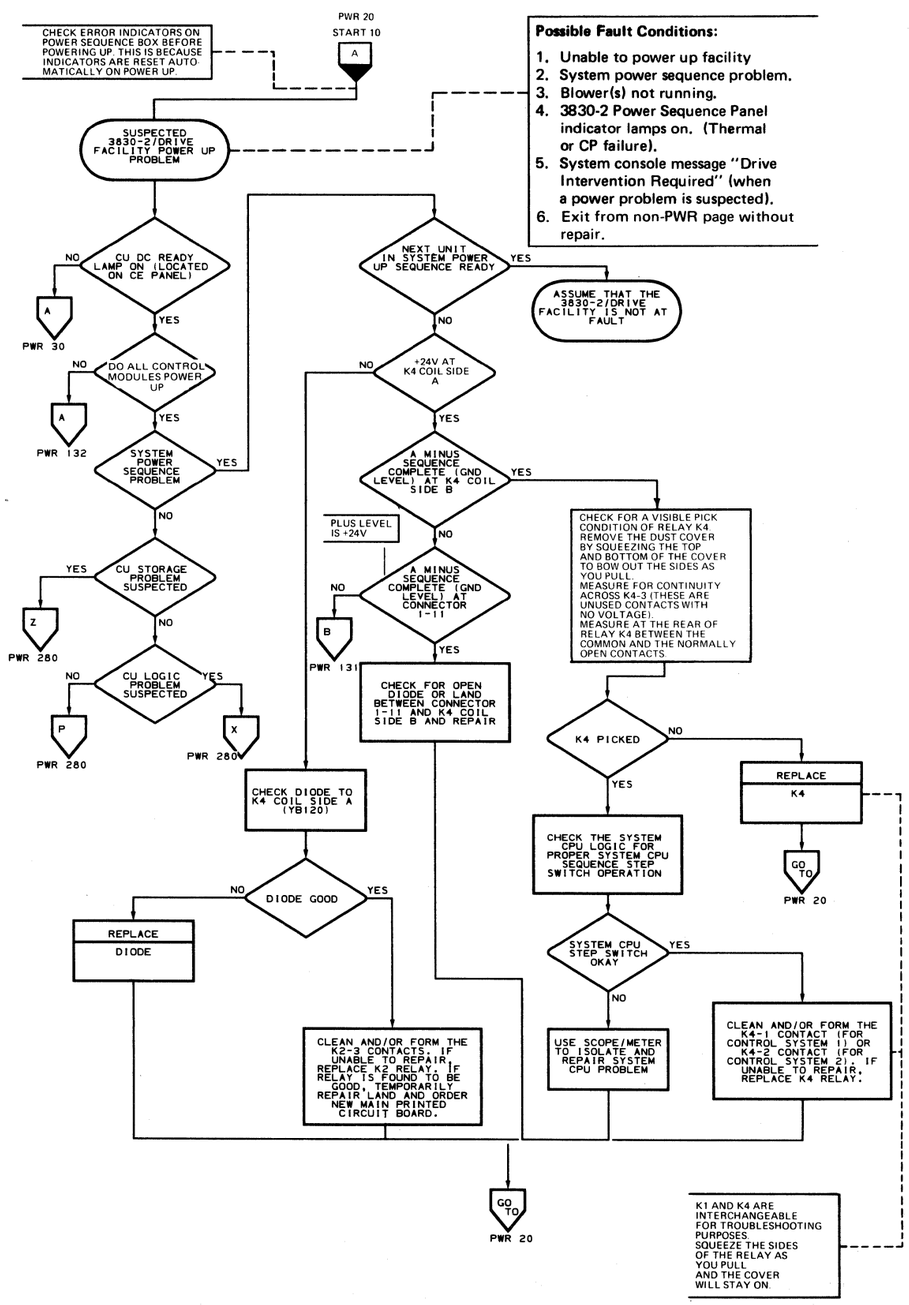
Power On/Off Sequence

Refer to PWR 310 for flowchart of power-on/off sequence.

FACILITY POWER-UP PROBLEM ANALYSIS

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.

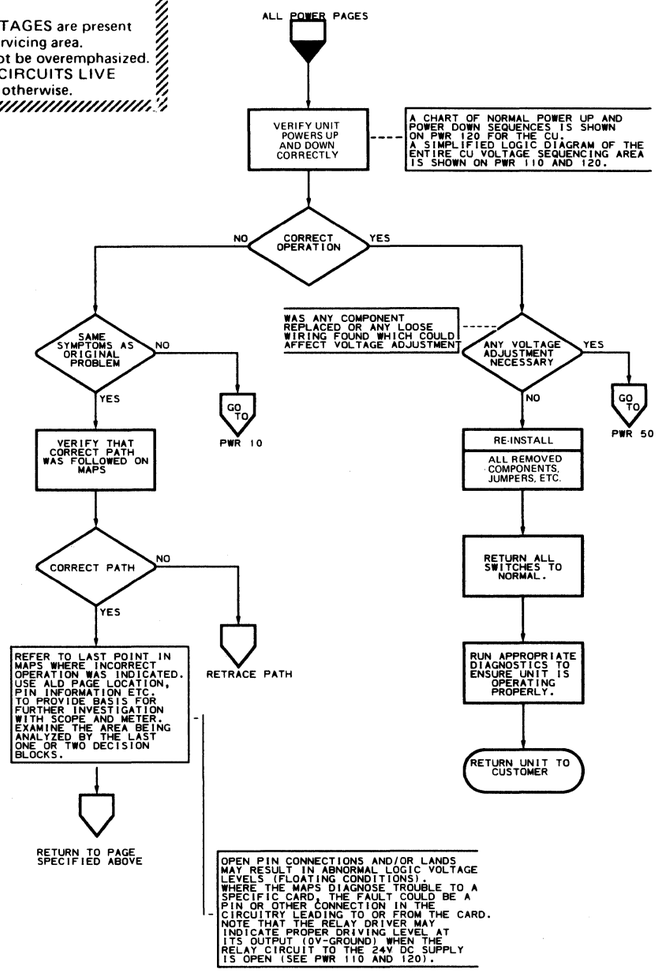




COMMON EXIT – POWER PROBLEM ANALYSIS

FIX VERIFICATION AND CHECKOUT PROCEDURE

DANGER
LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise.



3830-2 POWER PROBLEM ANALYSIS (PART 1 OF 2)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- See PWR 31 for component locations.

START 15, PWR 10 PWR 100 → A

PWR 31 → J

3830-2 CE PANEL DC READY LAMP OFF

CHECK THE POWER SEQUENCE INDICATOR PANEL FOR THE FOLLOWING ERROR INDICATIONS

SCHEMATIC SHOWN ON PWR 31

POWER SUPPLY FAILURE INDICATOR IS ON? YES / NO

CP TRIPPED. INITIALLY RESET TRIPPED CP AND ATTEMPT TO RETURN THE UNIT TO THE CUSTOMER. FOLLOW THE CP TRIPPED EXIT TO ANOTHER PAGE ONLY IF THE CP REPEATEDLY (SOLIDLY) TRIPS OR IF FREQUENT SERVICE CALLS ARE MADE AT THIS INSTALLATION FOR THE SAME CP BEING TRIPPED.	
IF THE CP IS TRIPPED	EXIT TO PAGE
CP 3 TO FANS	PWR 260
CP 4 TO PS 15 BIAS SUPPLY	PWR 80
CP 5 AC TO MPL FILE	PWR 45
CP 6 24V DC POWER SEQ (NOTE 1)	PWR 150, ENTRY A
CP 7 AC TO BULK 2 FOR DRIVERS (NOTE 1)	PWR 70
CP 8 AC TO BULK 1 FOR LOGIC AND STORAGE	PWR 60
CP 10 +24V DC POWER SEQ (NOTE 2)	PWR 150, ENTRY A
CP 11 TO PS 6	PWR 220
CP 12 TO PS 7	PWR 240
CP 13 TO PS 5	PWR 200
CP 14 TO PS 4	PWR 180
CP 15 TO PS 3 (+6V PORTION OF DUAL PS)	PWR 160
CP 16 +6V PS (NOTE 1)	PWR 270
CP 17 -36V PS (NOTE 1)	PWR 270
CP 18 TO PS 3 (-36V PORTION OF DUAL PS) (NOTE 1)	PWR 160

A THERMAL FAILURE INDICATOR IS ON? NO → 2 / YES

ATTEMPT TO POWER UP UNIT

AFTER APPROXIMATELY 15 SECONDS TO 2 MINUTES AFTER POWER DOWN, A FAILING THERMAL WILL NORMALLY CLOSE AGAIN. ALLOWING THE UNIT TO BE POWERED UP.

POWER CAME UP SUCCESSFULLY? YES / NO

PWR 31

CHECK FOR AN OPEN THERMAL BY MEASURING FOR THE PRESENCE OF +12V ACROSS THE RELATED THERMALS

AN OPEN THERMAL WAS FOUND? NO / YES

YB110 YB121

CHECK THE POINT-TO-POINT INPUT WIRING OF THERMALS FROM THE POWER CIRCUIT BOARD CONNECTORS FOR THE LOSS OF +12V. CORRECT THE PROBLEM. IF NO PROBLEM FOUND, REPLACE CARD P A1D1.

CONNECT A JUMPER AROUND THE OPEN THERMAL AND POWER ON THE UNIT IF IT IS NOT ALREADY ON

PRIOR TO JUMPERING PAST A THERMAL, CHECK THE AREA IN QUESTION FOR UNUSUAL AMOUNTS OF HEAT DAMAGE, OPEN COVERS, DUCTS, ETC. THAT ALLOW COOLING AIR TO ESCAPE.
WHEN THE UNIT FEELS SUFFICIENTLY COOL, BYPASS THE THERMAL IN QUESTION TO ALLOW OR MAINTAIN POWER UP FOR FURTHER TROUBLE ISOLATION.
DO NOT LEAVE THE THERMAL BYPASSED WITH POWER ON FOR MORE THAN 5 MINUTES, OR UNTIL AN ABNORMAL HEAT BUILDUP IS FELT AGAIN (WHICH EVER OCCURS FIRST).

GO TO PWR 20

THE RELATED BLOWER IS RUNNING? NO / YES

AC IS AT THE RELATED FAN CONNECTOR? YES / NO

REPLACE THE FAN

CHECK AC INPUT POINT TO THE RELATED FAN

CHECK FOR AIR OBSTRUCTIONS IN THE DUCTS, CLOGGED FILTERS, OPEN PANELS, ETC.

AIR OBSTRUCTION FOUND? YES / NO

CORRECT THE PROBLEM

GO TO PWR 20

CUSTOMER'S ROOM TEMPERATURE BELOW 90 DEG. F (26 DEG. C)? NO / YES

INFORM THE CUSTOMER THAT HIS ROOM TEMPERATURE IS BEYOND THE NORMAL OPERATING RANGE OF UNIT. INFORM YOUR IBM INSTALLATION PLANNING REPRESENTIVE IF THERE IS A COOLING CAPACITY PROBLEM HERE.

INSPECT THE UNIT FOR VISIBLE HEAT DAMAGE TO COMPONENTS. REPLACE ANY DAMAGED COMPONENTS. RUN THE APPROPRIATE DIAGNOSTIC PROGRAMS TO ENSURE PROPER OPERATION

IF NO HEAT DAMAGE IS NOTED, REPLACE THE BAD THERMAL. IF IT IS STILL TRIPPED, OR TRIPS AGAIN WHILE THE CUSTOMER'S ROOM IS BELOW 90 DEG. F. (26 DEG. C)

GO TO PWR 20

2

CB 2 OR CP 1 OR CP 9 TRIPPED? NO / YES

INITIALLY RESET TRIPPED CB OR CP AND ATTEMPT TO POWER UP FROM CPU.

FOLLOW THE CB/CP TRIPPED EXIT TO ANOTHER PAGE ONLY IF THE CB/CP REPEATEDLY (SOLIDLY) TRIPS, OR IF FREQUENT SERVICE CALLS ARE MADE AT THIS INSTALLATION FOR THE SAME CB/CP BEING TRIPPED.

IF THE CB CP IS TRIPPED	EXIT TO PAGE
CB 2 MAIN AC POWER	PWR 40
CP 2 TO CONVENIENCE OUTLET	PWR 135
CP 1 TO 24V DC PS, 7.25V AC SCRID SUPPLY AND 41V AC USE METER SUPPLY	PWR 135
CP 9 +12V TO POWER SEQUENCE BOARD	PWR 150

SEE LOC 2 FOR PC1 LOCATION

+24V POWER ON START SIGNAL PRESENT AT PC 1-5? YES / NO

ATTEMPT TO POWER UP FROM 3830-2 METER PANEL.

POWER UP SUCCESSFUL? NO / YES

YB131 CHECK K1 PICK AND HOLD PATHS THRU CE NORMAL SWITCH.

YB131 REPAIR OPEN CKT FROM PC1-6 THRU SYSTEM STEP SWITCH TO PC1-6.

SWITCH THE OPERATION MODE SWITCH TO CE MODE AND TRY TO POWER UP LOCALLY

CU POWER UP (DC READY LIGHT ON)? NO / YES

POWER DOWN, THEN MOVE OPERATION MODE SWITCH BACK TO NORMAL AND POWER UP FROM CPU

MOVE THE OPERATION MODE SWITCH BACK TO NORMAL

CHECK THE POWER SEQUENCE INDICATORS BY OPERATING THE POWER SEQUENCE PANEL LAMP TEST SWITCH

THIS LATCHES THE LAMPS ON AND LAMP RESET WILL HAVE TO BE PUSHED TO TURN THEM OFF

K PWR 31

CHECK THE CPU LOGIC FOR MISSING POWER UP START SIGNALS. ALSO CHECK THE PREVIOUS SYSTEM UNIT FOR THE PROPER POWER UP SEQUENCE COMPLETE SIGNAL TO THE SYSTEM. USE SCOPE/METER TO ISOLATE AND REPAIR.

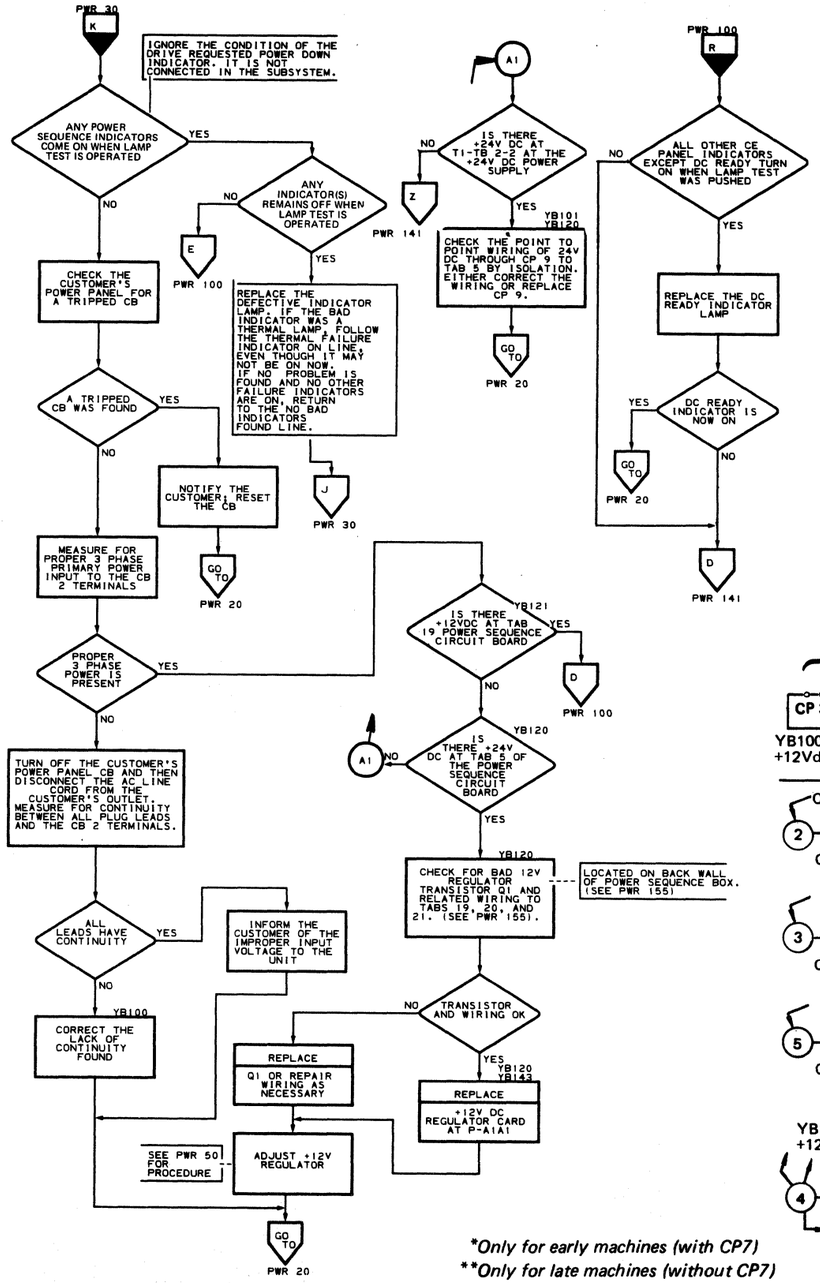
GO TO PWR 20

SYSTEM POWER-ON RELAY UP? NO / YES

YB131 REPAIR OPEN CKT FROM PC1-2 THRU SYSTEM POWER-ON RELAY POINTS, TO PC1-5.

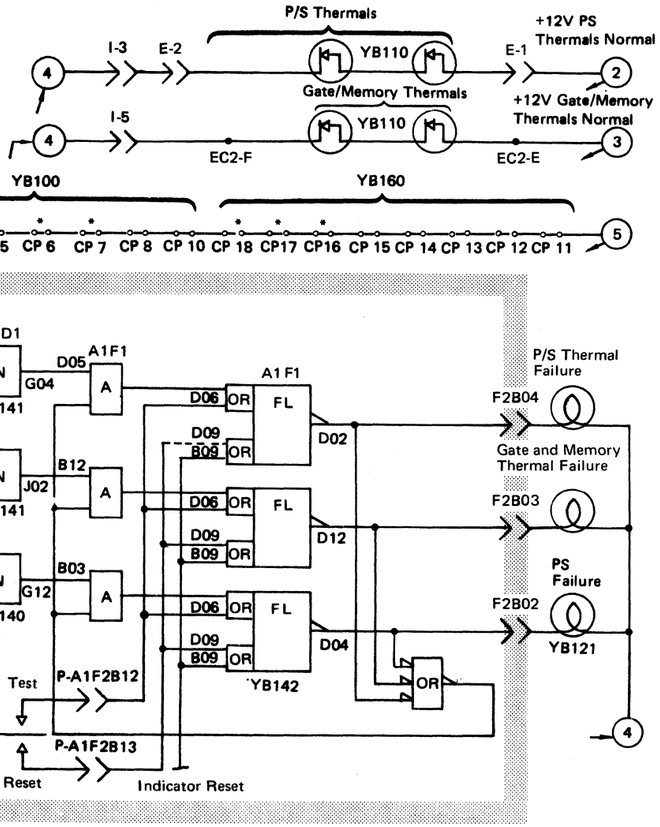
NOTES:
1. Only for early machines (with CP 7).
2. Only for late machines (without CP 7).

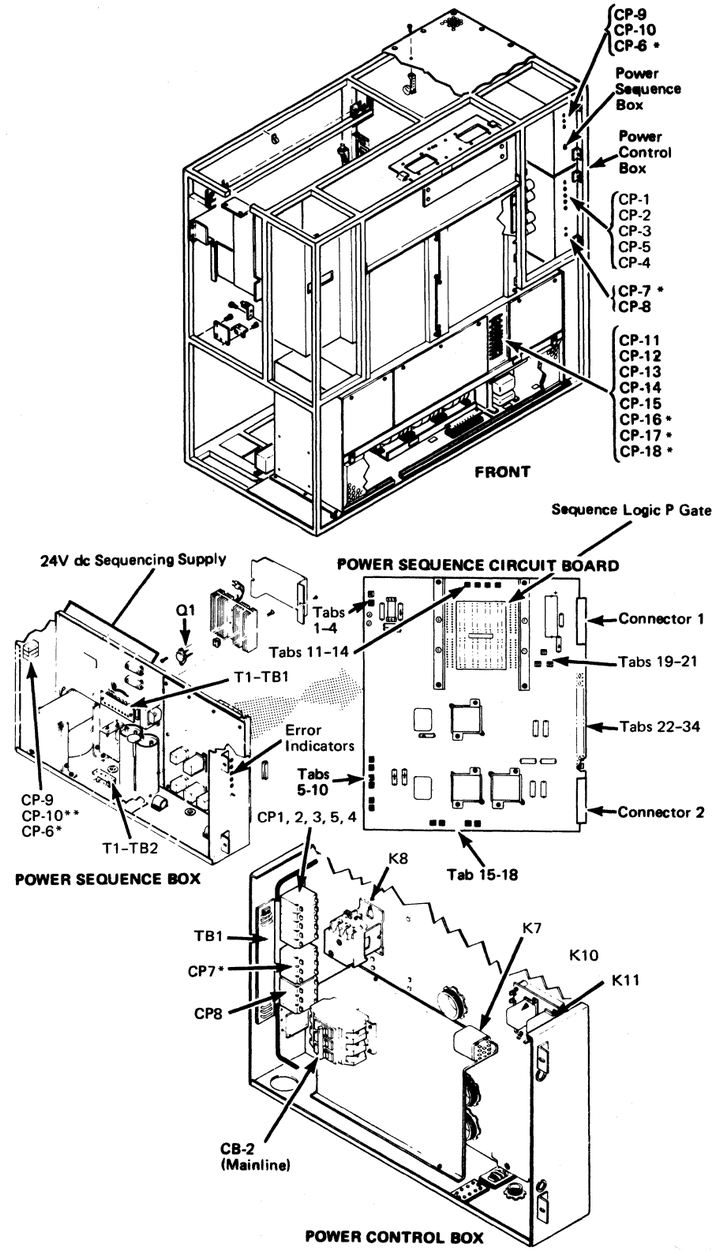
3830-2 POWER PROBLEM ANALYSIS (Part 2 of 2)



*Only for early machines (with CP7)
**Only for late machines (without CP7)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.



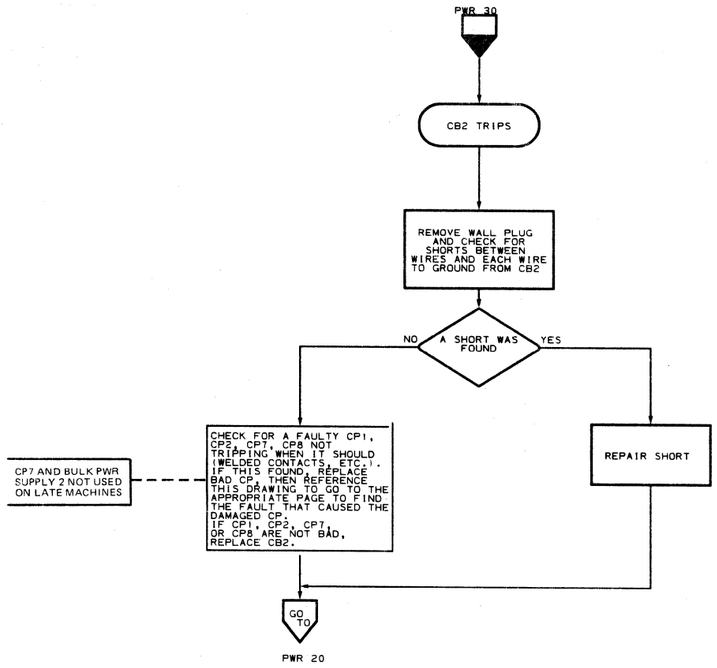


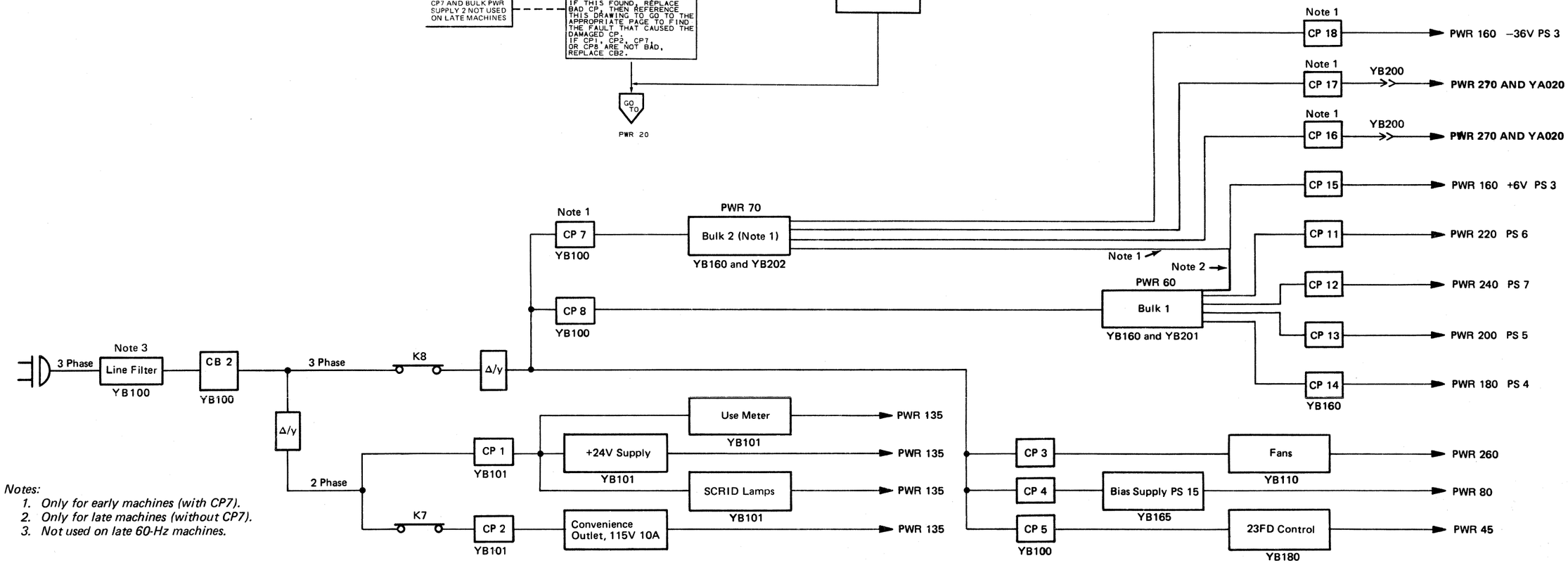
3830-2	BR0500	2347159	437402A	437403	437405	437414			
	Seq 1 of 2	Part Number	15 Mar 72	21 Apr 72	15 Aug 72	4 Jun 73			

DANGER
LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise.

Turn off main circuit breaker at customer's power panel before plugging or unplugging the power plug. See general safety CEM (metal clad plugs)

SEE PWR 300 FOR DISTRIBUTION





Notes:
1. *Only for early machines (with CP7).*
2. *Only for late machines (without CP7).*
3. *Not used on late 60-Hz machines.*

BR0500 Seq 2 of 2	2347159 Part Number

437402A	437403	437405	437414			
15 Mar 72	21 Apr 72	15 Aug 72	4 Jun 73			

CP5 – MPL FILE AC CONTROL

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

LOCATIONS

See MPL 10 for MPL file component locations

See LOC 12 for tab locations

LOGIC LEVELS

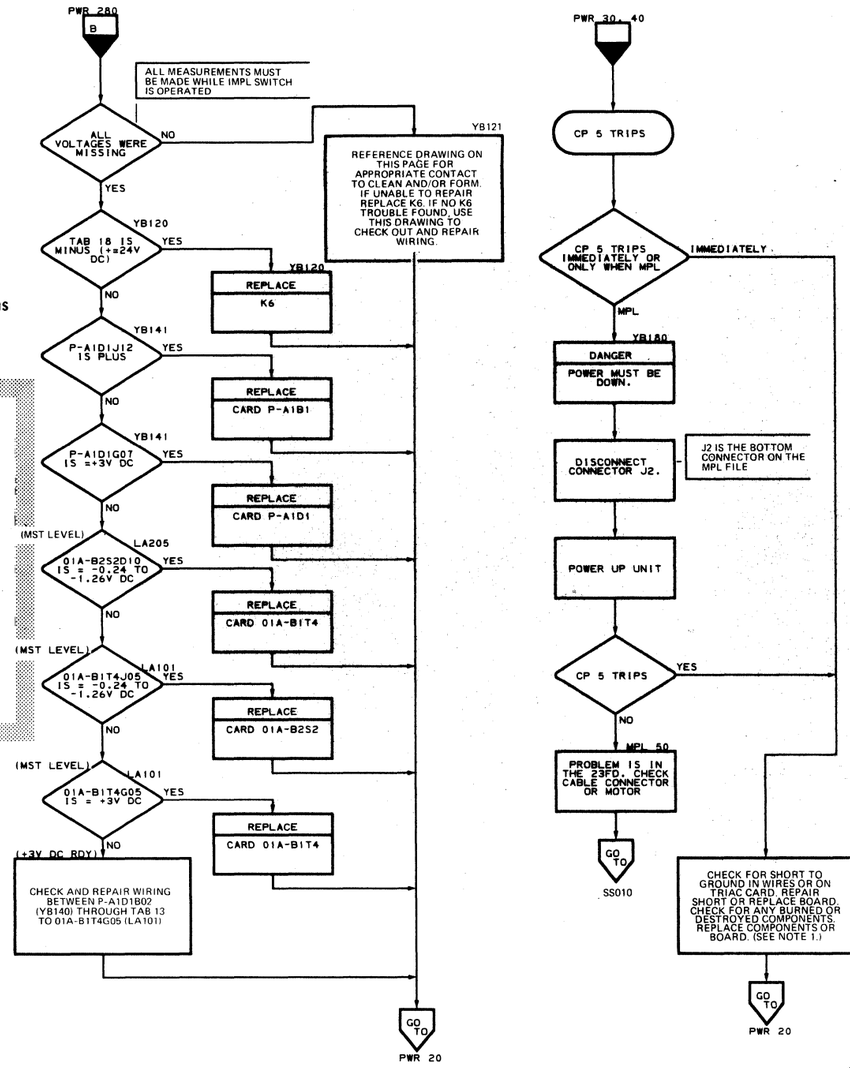
For Power Sequence Logic (P-A1 Board Y8 Pages)

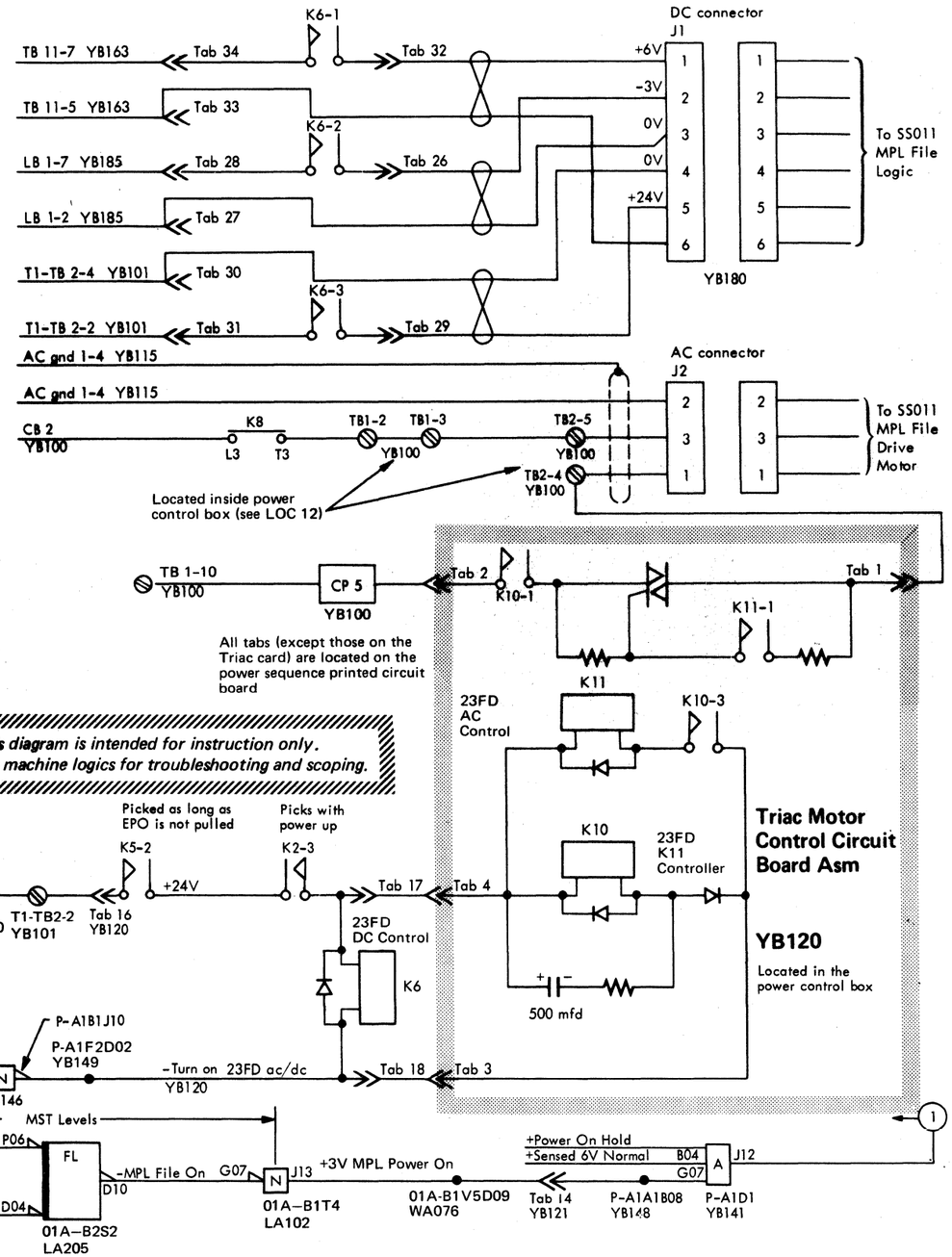
(+) equals +2 to +12V dc
(–) equals ground to +0.29V dc

For CU Logic (LA Pages)

(+) equals +0.23 to +0.68V dc
(–) equals –0.24 to –1.26V dc

Any exceptions to these levels are indicated within the MAP decision block





Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.

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3830-2 POWER SUPPLY ADJUSTMENT PROCEDURE

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
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CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

From all pages where power supply adjustment is indicated

Adjust appropriate power supply as necessary

If unable to power up, centering the PS adjustment potentiometer in question should allow the facility to come up for stable measurements

Measure following DC voltages with Digitec** voltmeter (or equivalent). Adjust if necessary.

Voltage	Page	Monitoring Point	Tolerance Min	Tolerance Max	Power Supply	Adjustment Location: Before EC716230	Adjustment Location: At EC716230 or later
−36.00 Note 3	PWR 170	Panel behind A gate TB11-1 to TB11-4 (gnd)	-35.92	-36.08	PS 3	2	2
1.255	PWR 250	MST gate B3R2G11 Gnd ref B3R2J08	■ 1.253	1.257	PS 7	7	8
6.000	PWR 170	MST gate LB 2-1 Gnd ref LB 2-8	5.98	6.02	PS 3	1	1
-3.00	PWR 210	MST gate, B1D2G06 Gnd ref B1C2J08	-2.995	-3.005	PS 5 *	4	5
1.250	PWR 210	MST gate, B1D2J03 Gnd ref B1C2J08	1.248	1.252	PS 5 *	5	4
					PS 4 * Not Used	3	
-3.000	PWR 250	MST gate, B3R2G06 Gnd ref B3R2J08	■ -2.995	-3.005	PS 7	8	7
3.530	PWR 230	MST gate, B3R2G04 Gnd ref B3R2J08	■ 3.528	3.532	PS 6 * Note 1	6	6
12.00	PWR 150	Sequence panel, Tab 19 Gnd ref Tab 22	11.96	12.04	Pwr Seq Box Card A1	●	

* Voltage adjustment pots are on regulator cards and are unsealed. Do not attempt to alter sealed pots.

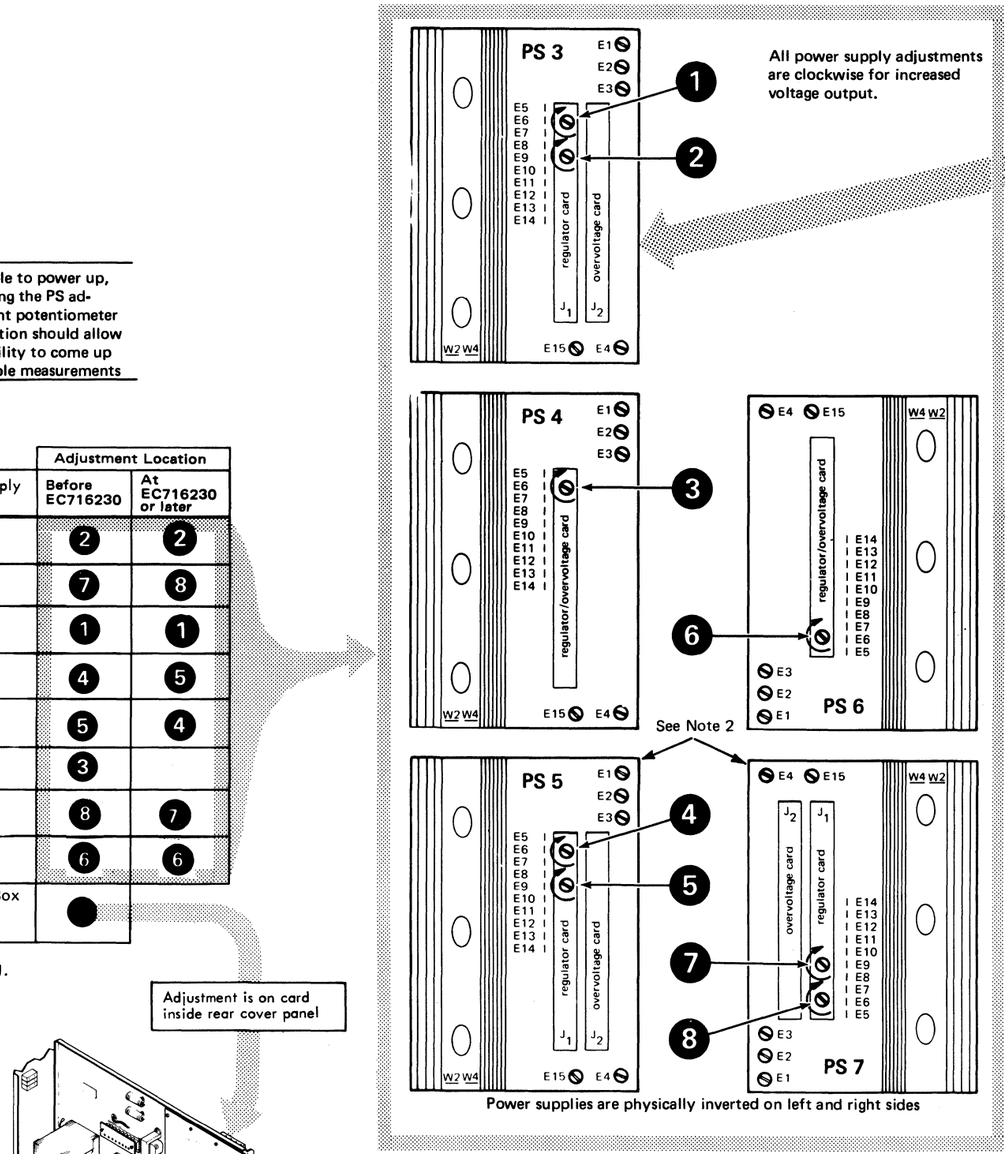
** Trademark of United Systems Corp. IBM P/N 453585

■ Adjust while clock is stopped

If unable to adjust, go to the appropriate page referenced above. Follow the intermittent CP trip entry for troubleshooting, but do not replace CP if told to.

Referenced PWR page

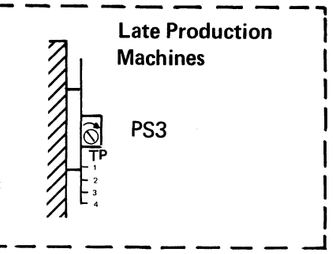
Note 1: *PS7 must be adjusted before PS6.*

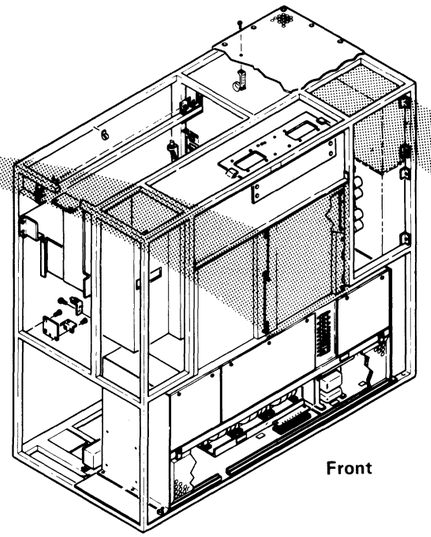


All power supply adjustments are clockwise for increased voltage output.

Power supplies are physically inverted on left and right sides

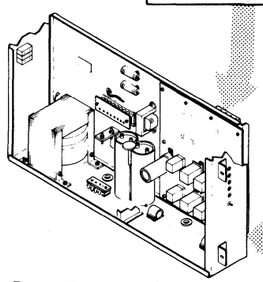
Note 2: Overvoltage card not present if power supplies at EC716230 or later.





Front

Adjustment is on card inside rear cover panel



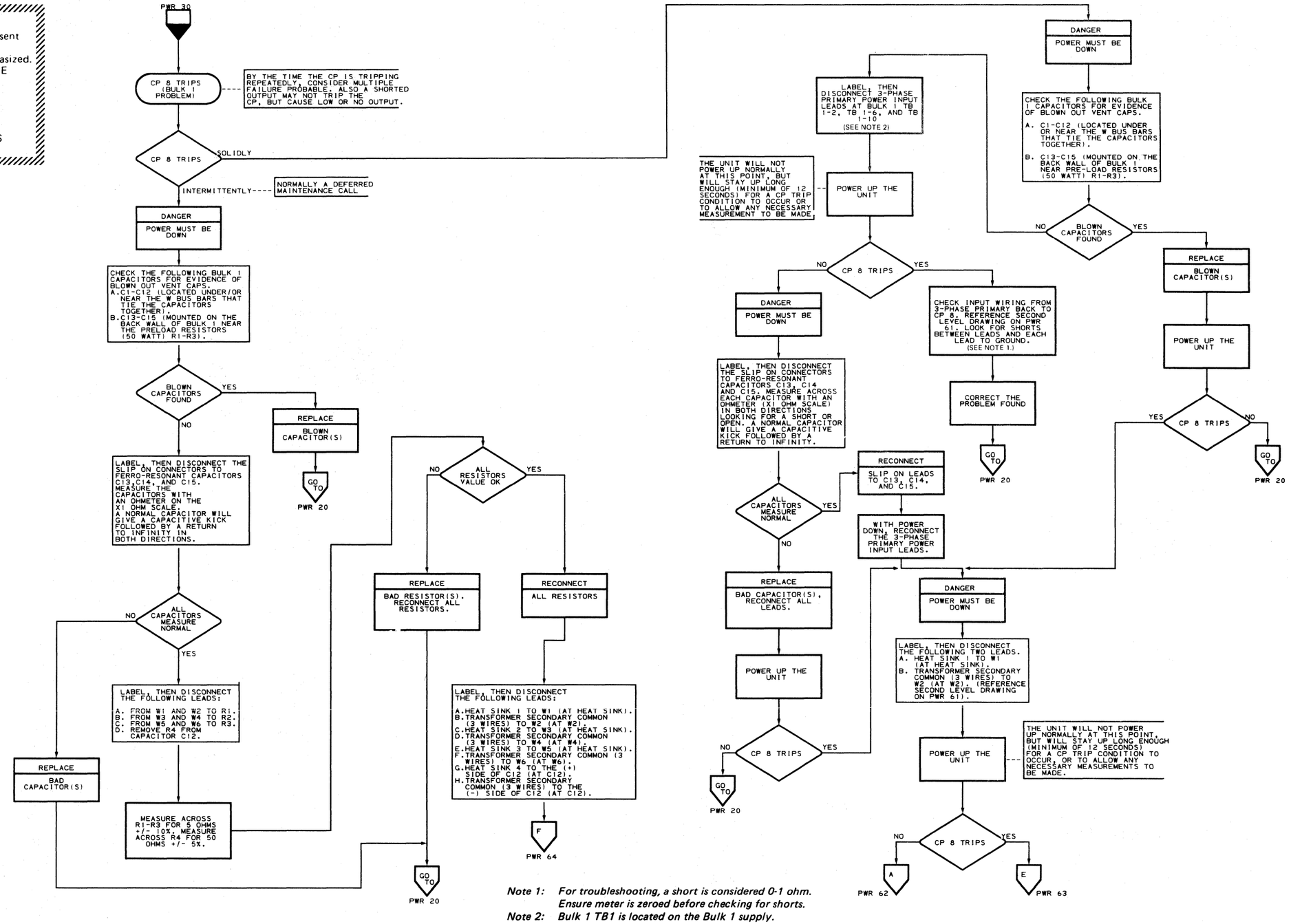
Power Sequence Box

Note 3: Only for early machines (with CP7).

BULK 1 (CP8) POWER PROBLEM (PART 1 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8, AND 10 FOR COMPONENT LOCATIONS.
- SEE PWR 61 FOR VOLTAGE DISTRIBUTION.

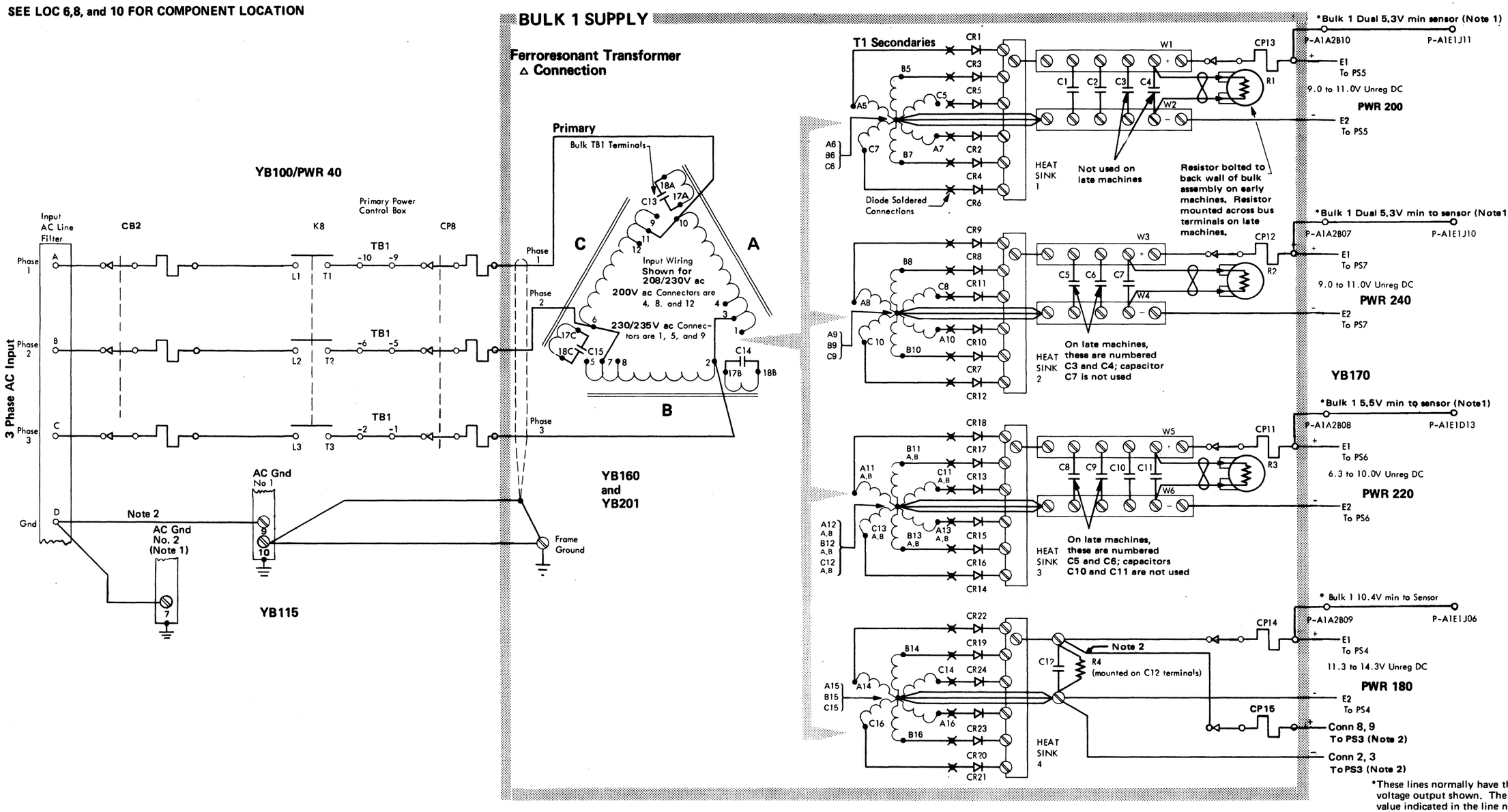


Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.

Note 2: Bulk 1 TB1 is located on the Bulk 1 supply.

BULK 1 (CP 8) POWER PROBLEM (Part 2 of 6)

SEE LOC 6,8, and 10 FOR COMPONENT LOCATION



*These lines normally have the bulk voltage output shown. The minimum value indicated in the line name is what the sensor requires to consider bulk supplies normal.
PLD sensor cards located YB145

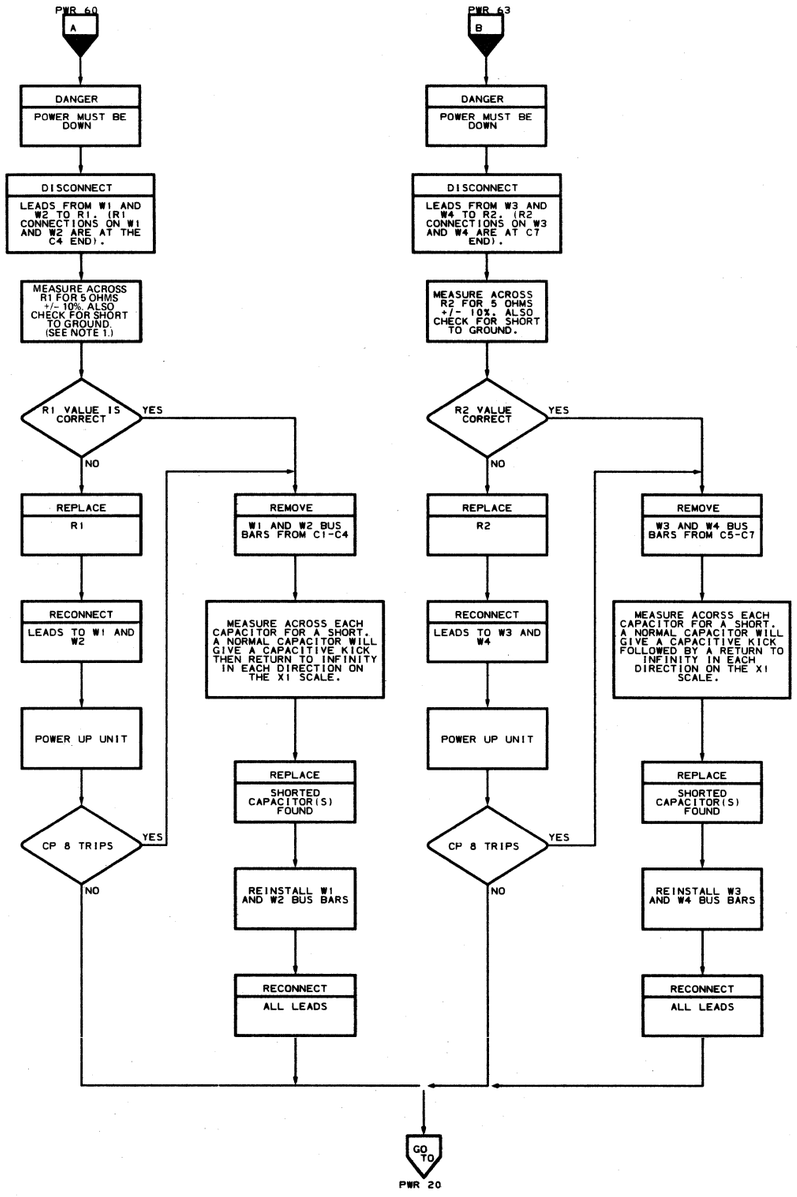
Notes:

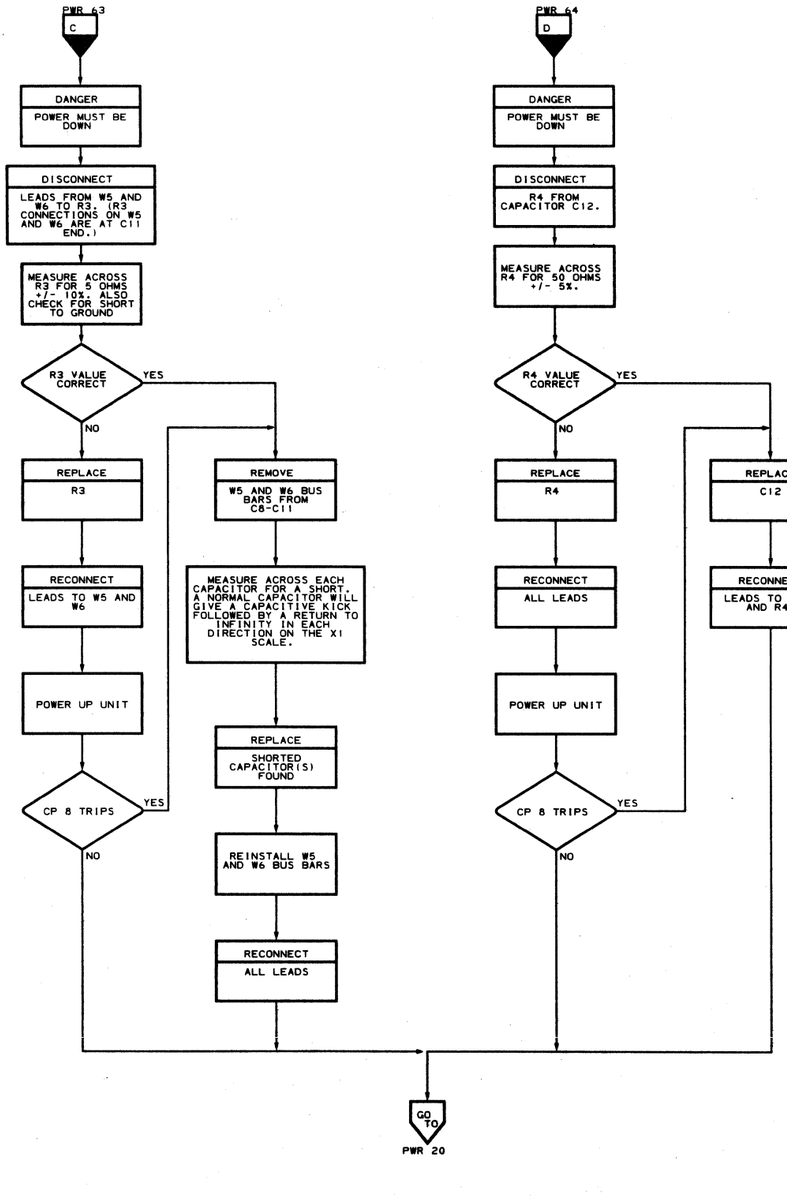
1. *Only for early machines (with CP7).*
2. *Only for late machines (without CP7).*

BULK 1 (CP8) POWER PROBLEM (PART 3 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8, AND 10 FOR COMPONENT LOCATIONS
- SEE PWR 61 FOR VOLTAGE DISTRIBUTION





Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.

3830-2	BR0800 Seq 2 of 2	2347162 Part Number	437402A 15 Mar 72	437403 21 Apr 72	437405 15 Aug 72	437414 4 Jun 73			

BULK 1 (CP8) POWER PROBLEM (PART 4 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8, AND 10 FOR COMPONENT LOCATIONS.
- SEE PWR 61 FOR VOLTAGE DISTRIBUTION

CHECKING POWER DIODES

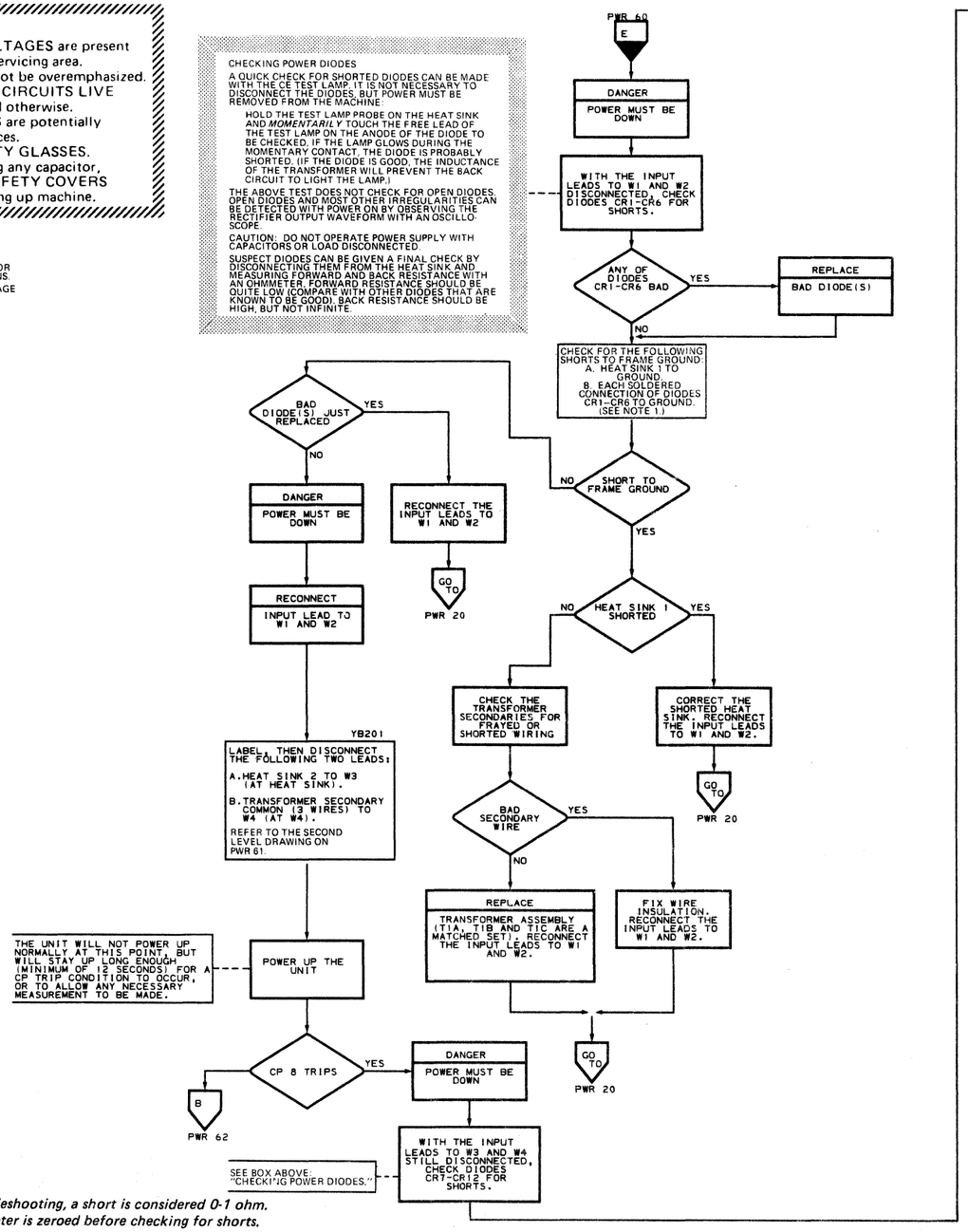
A QUICK CHECK FOR SHORTED DIODES CAN BE MADE WITH THE CE TEST LAMP. IT IS NOT NECESSARY TO DISCONNECT THE DIODES, BUT POWER MUST BE REMOVED FROM THE MACHINE:

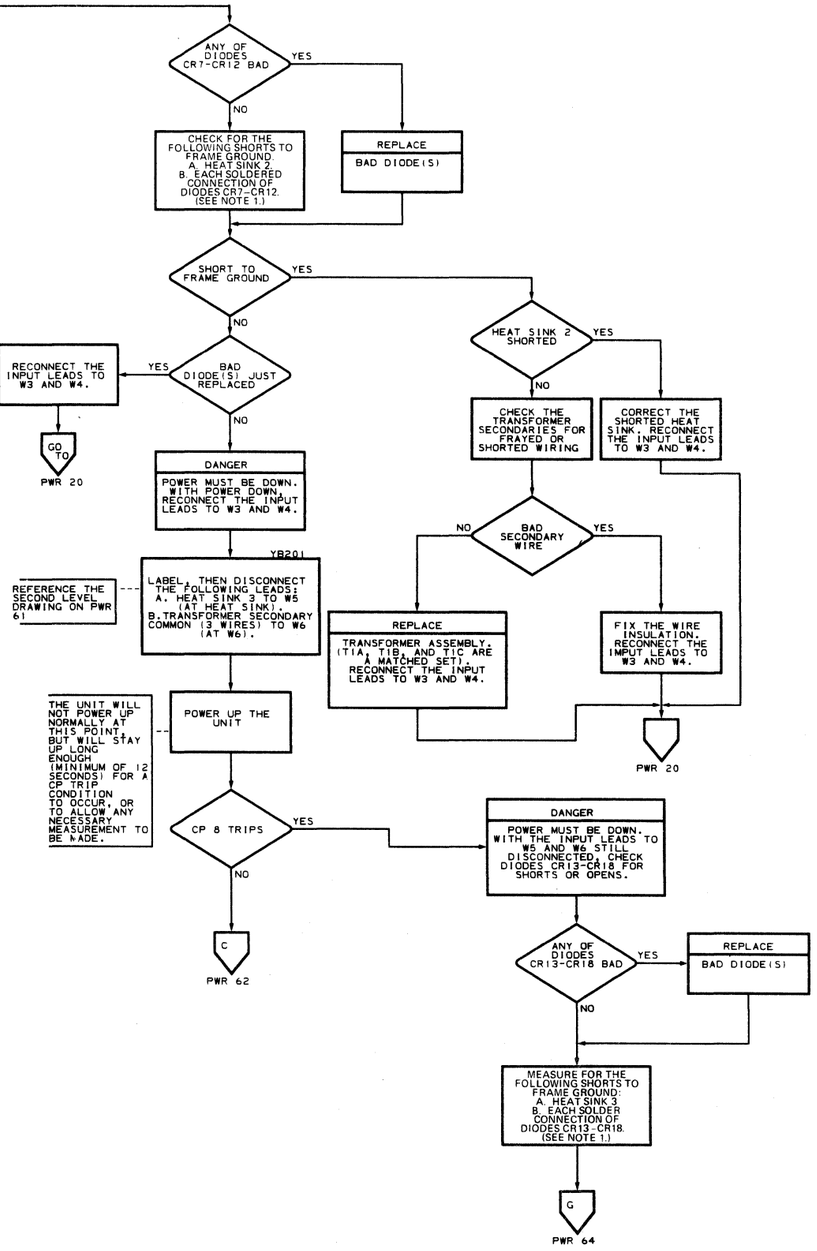
HOLD THE TEST LAMP PROBE ON THE HEAT SINK AND *MOMENTARILY* TOUCH THE FREE LEAD OF THE TEST LAMP ON THE ANODE OF THE DIODE TO BE CHECKED. IF THE LAMP GLOWS DURING THE MOMENTARY CONTACT, THE DIODE IS PROBABLY SHORTED. (IF THE DIODE IS GOOD, THE INDUCTANCE OF THE TRANSFORMER WILL PREVENT THE BACK CIRCUIT TO LIGHT THE LAMP.)

THE ABOVE TEST DOES NOT CHECK FOR OPEN DIODES. OPEN DIODES AND MOST OTHER IRREGULARITIES CAN BE DETECTED WITH POWER ON BY OBSERVING THE RECTIFIER OUTPUT WAVEFORM WITH AN OSCILLOSCOPE.

CAUTION: DO NOT OPERATE POWER SUPPLY WITH CAPACITORS OR LOAD DISCONNECTED.

SUSPECT DIODES CAN BE GIVEN A FINAL CHECK BY DISCONNECTING THEM FROM THE HEAT SINK AND MEASURING FORWARD AND BACK RESISTANCE WITH AN OHMMETER. FORWARD RESISTANCE SHOULD BE QUITE LOW (COMPARE WITH OTHER DIODES THAT ARE KNOWN TO BE GOOD). BACK RESISTANCE SHOULD BE HIGH, BUT NOT INFINITE.





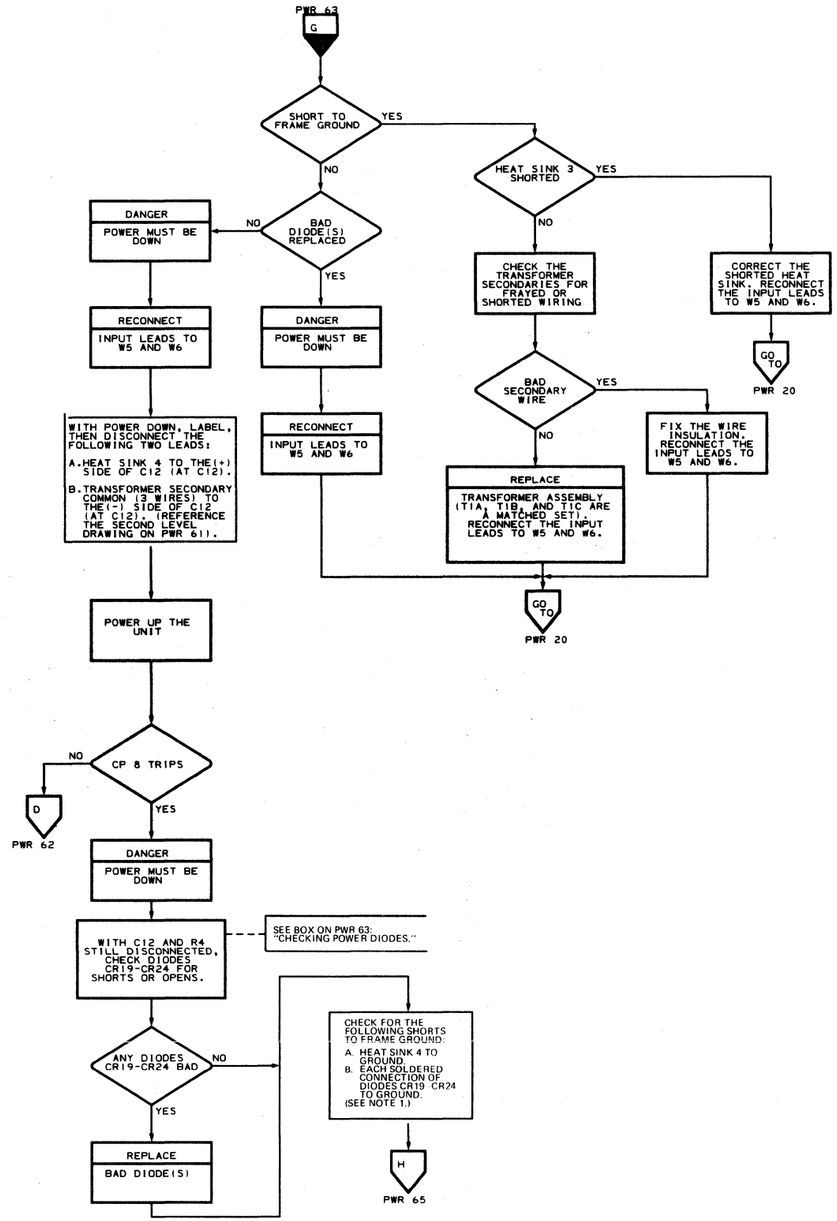
Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.

BR0900	2347163
Seq 1 of 2	Part Number

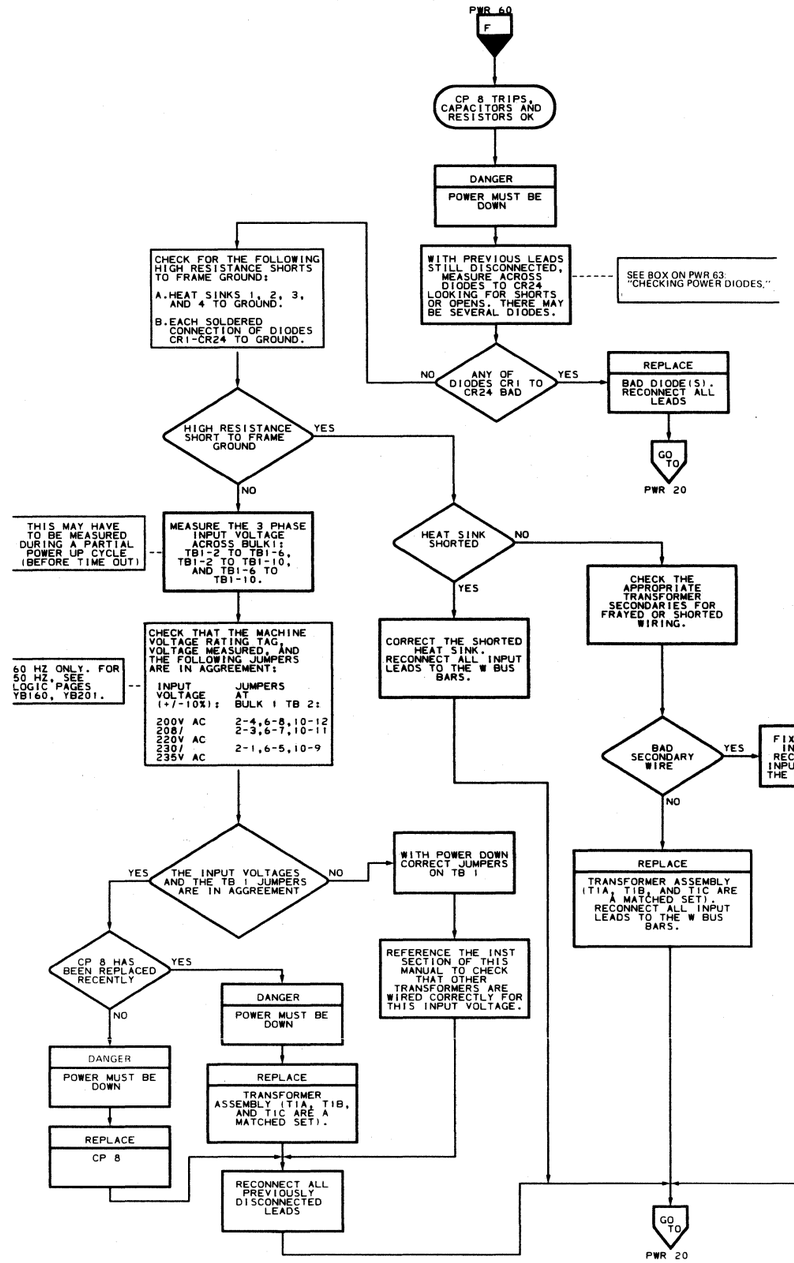
437402A	437403	437405	437414			
15 Mar 72	21 Apr 72	15 Aug 72	4 Jun 73			

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8 AND 10 FOR COMPONENT LOCATIONS
- SEE PWR 61 FOR VOLTAGE DISTRIBUTION



Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.



BULK 1 (CP8) POWER PROBLEM (PART 6 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8, AND 10 FOR COMPONENT LOCATIONS.
- SEE PWR 61 FOR VOLTAGE DISTRIBUTION.

PWR 180-240

V

1

DANGER
POWER MUST BE DOWN

CHECK THE FOLLOWING BULK 1 CAPACITORS FOR EVIDENCE OF BLOWN OUT VENT CAPS:

A. C1-C12 (LOCATED UNDER OR NEAR THE W BUS BARS THAT TIE THE CAPACITORS TOGETHER.)

B. C13-C15 (MOUNTED ON THE BACK WALL OF BULK 1 NEAR PRE-LOAD RESISTORS.) (50 WATT R1-R3).

BLOWN CAPACITOR(S)?
NO
YES

THIS MAY HAVE TO BE MEASURED DURING A PARTIAL POWER UP CYCLE (BEFORE TIME OUT)

MEASURE THE INPUT 3 PHASE VOLTAGE ACROSS BULK1 TB 1-2 TO TB 1-6, TB 1-2 TO TB 1-10, AND TB 1-6 TO TB 1-10.

REPLACE
BLOWN CAPACITOR(S)

60 HZ ONLY. FOR 50 HZ, SEE LOGIC PAGES YB160, YB201.

CHECK THAT THE MACHINE VOLTAGE RATING TAG, INPUT VOLTAGE MEASURED, AND THE FOLLOWING JUMPERS ARE IN AGREEMENT:

INPUT VOLTAGE (+/- 10%)	JUMPERS AT BULK 1 TB 1
200V AC	2-4, 6-8, 10-12
208/220V AC	2-3, 6-7, 10-11
230/235V AC	2-1, 6-5, 10-9

INPUT VOLTAGE AND TB 1 JUMPERS AGREE?
YES
NO

CORRECT JUMPERS ON TB 1

DANGER
POWER MUST BE DOWN

WITH POWER DOWN, LABEL, THEN DISCONNECT SLIP ON CONNECTORS AT C13, C14, AND C15. MEASURE THESE CAPACITORS FOR SHORTS OR OPENS. A NORMAL CAPACITOR WILL GIVE A CAPACITIVE KICK FOLLOWED BY A RETURN TO INFINITY IN BOTH DIRECTIONS ON THE X1 OHMS SCALE.

REFERENCE THE INST SECTION OF THIS MANUAL TO CHECK THAT OTHER TRANSFORMERS ARE WIRED CORRECTLY FOR THIS INPUT VOLTAGE

CAPACITORS MEASURE GOOD?
NO
YES

REPLACE
BAD CAPACITOR(S). RECONNECT ALL LEADS.

RECONNECT THE LEADS TO CAPACITORS C13, C14, AND C15

GO TO PWR 20

2

YB201

FOR THE BULK 1 OUTPUT IN QUESTION, DISCONNECT AND MEASURE ONE OF THE FOLLOWING PRELOAD RESISTORS:

BULK 1 OUTPUT TO: RESISTOR: DISCONNECT AT: OHM VALUE

A.	PS 4,PS3'	R4	ACROSS C12	(50 +/-5%)
B.	PS 5	R1	W1 AND W2	(5 +/-10%)
C.	PS 6	R3	W5 AND W6	(5 +/-10%)
D.	PS 7	R2	W3 AND W4	(5 +/-10%)

PRE-LOAD RESISTOR VALUE CORRECT?
NO
YES

REPLACE
BAD PRELOAD RESISTOR(S)

GO TO PWR 20

FOR THE BULK 1 OUTPUT IN QUESTION, LABEL THEN DISCONNECT ONE SET OF THE FOLLOWING LEADS:

BULK 1 OUTPUT TO: DISCONNECT LEADS:

A. PS 4,PS3'
1. HEAT SINK 4 TO (+) SIDE OF C12.
2. TRANSFORMER SECONDARY COMMON (3 WIRES) TO (-) SIDE OF C12.

B. PS 5
1. HEAT SINK 2 TO W1 (AT HEAT SINK).
2. TRANSFORMER SECONDARY COMMON (3 WIRES) TO W2 (AT W2).

C. PS 6
1. HEAT SINK 3 TO W5 (AT HEAT SINK).
2. TRANSFORMER SECONDARY COMMON (3 WIRES) TO W6 (AT W6).

D. PS 7
1. HEAT SINK 2 TO W3 (AT HEAT SINK).
2. TRANSFORMER SECONDARY COMMON (3 WIRES) TO W4 (AT W4).

FOR THE BULK 1 OUTPUT IN QUESTION, MEASURE THE PROPER GROUP OF DIODES FOR SHORTS OR OPENS:

BULK 1 OUTPUT TO: MEASURE DIODES:

A.	PS 4,PS3'	CR 19-24
B.	PS 5	CR 1-6
C.	PS 6	CR 13-18
D.	PS 7	CR 7-12

SEE BOX ON PWR 63 "CHECKING POWER DIODES"

3

*Only for late machines (with CP 7)

PWR 100, 180-240

U

REFERENCE DRAWING ON PWR 225. DURING A POWER UP CYCLE, MEASURE THE BULK 1 OUTPUT IN QUESTION FOR ONE OF THE FOLLOWING OUTPUTS AT:

BULK 1 OUTPUT TO:	MEASURE AT:	VALUE:
A. PS 4,PS3'	C12(+) TO (-)	POINTS 11.3 TO 14.3V DC
B. PS 5	W1(+) TO W2(-)	9.0 TO 11.0V DC
C. PS 6	W5(+) TO W6(-)	6.3 TO 10.0V DC
D. PS 7	W3(+) TO W4(-)	9.0 TO 11.0V DC

MEASURE CORRECTLY?
NO
YES

1

REFERENCE DRAWING ON PWR 61. CHECK FOR AN OPEN CP THAT HAS NOT TRIPPED AT THE APPROPRIATE POWER SUPPLY, OR AN OUTPUT WIRING PROBLEM TO THE POWER SUPPLY, OR SENSING LOGIC.

REPAIR OR REPLACE AS NECESSARY

GO TO PWR 20

SHORT TO FRAME GROUND?
YES
NO

HEAT SINK 4 SHORTED?
NO
YES

CHECK THE TRANSFORMER SECONDARIES FOR FRAYED OR SHORTED WIRING.

BAD SECONDARY WIRE?
NO
YES

REPLACE
TRANSFORMER ASSEMBLY. (T1A, T1B, AND T1C ARE A MATCHED SET.) RECONNECT THE INPUT LEADS TO C12 AND R4.

FIX THE WIRE INSULATION. RECONNECT THE INPUT LEADS TO C12 AND R4.

CORRECT THE SHORTED HEAT SINK. RECONNECT THE INPUT LEADS TO C12 AND R4.

BAD DIODE(S) JUST REPLACED?
NO
YES

RECONNECT THE INPUT LEADS TO C12 AND R4

CHECK THE FOLLOWING COMPONENTS, LISTED IN ORDER OF PROBILITY OF FAILURE:
1. CP 8 - TRIPPING WITHOUT EXCESSIVE CURRENT.
2. T1A, T1B, T1C - PRIMARY SHORTS TO GROUND OR SECONDARY.
USE SCOPE/METER TO ISOLATE AND REPAIR. THEN RECONNECT ALL LEADS.

GO TO PWR 20

PWR 64

H

3

DIODE(S) MEASURE BAD?
YES
NO

REPLACE
BAD DIODE(S). RECONNECT ALL LEADS.

GO TO PWR 20

FOR THE BULK 1 OUTPUT IN QUESTION, DISCONNECT THEN MEASURE ONE SET OF THE FOLLOWING CAPACITORS FOR SHORTS OR OPENS:

BULK 1 OUTPUT TO:	DISCONNECT AT:	MEASURE ACROSS CAPACITORS
A. PS 4, PS 3'	C12 TERMINALS	C12
B. PS 5	REMOVE W1 BUS FROM CAPACITOR BANK	C1-C4
C. PS 6	REMOVE W5 BUS FROM CAPACITOR BANK	C8-C11
D. PS 7	REMOVE W3 BUS FROM CAPACITOR BANK	C5-C7

A NORMAL CAPACITOR WILL GIVE A CAPACITIVE KICK, FOLLOWED BY A RETURN TO INFINITY IN BOTH DIRECTIONS ON THE X1 OHM SCALE.

CAPACITOR(S) MEASURES BAD?
YES
NO

REPLACE
CAPACITOR(S). RECONNECT ALL LEADS

GO TO PWR 20

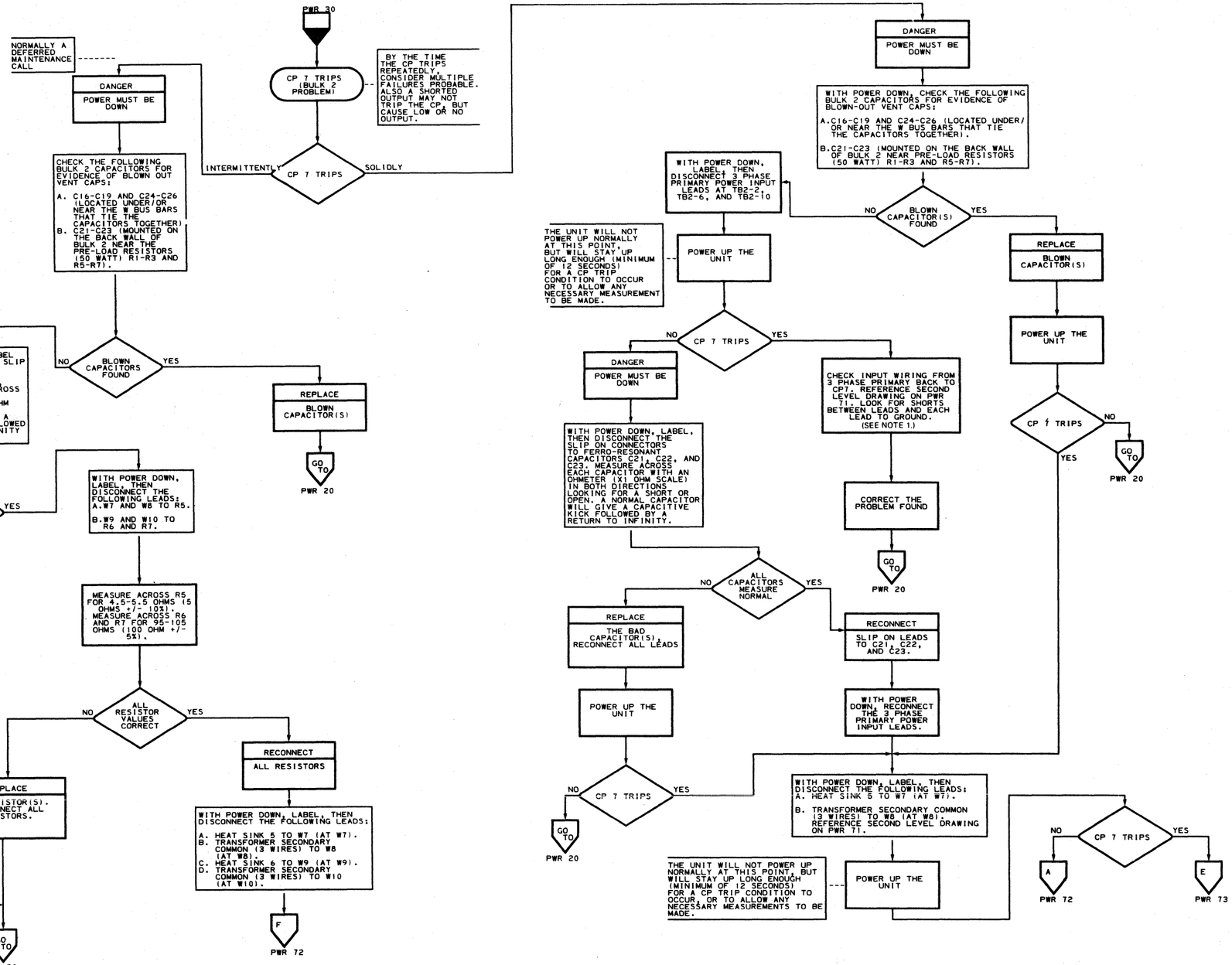
RECONNECT ALL LEADS

REPLACE
TRANSFORMER ASSEMBLY. (T1A, T1B, AND T1C ARE A MATCHED SET.)

BULK 2 (CP7) POWER PROBLEM (Part 1 of 5)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8, AND 10 FOR COMPONENT LOCATIONS.
- SEE PWR 71 FOR VOLTAGE DISTRIBUTION.



Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.

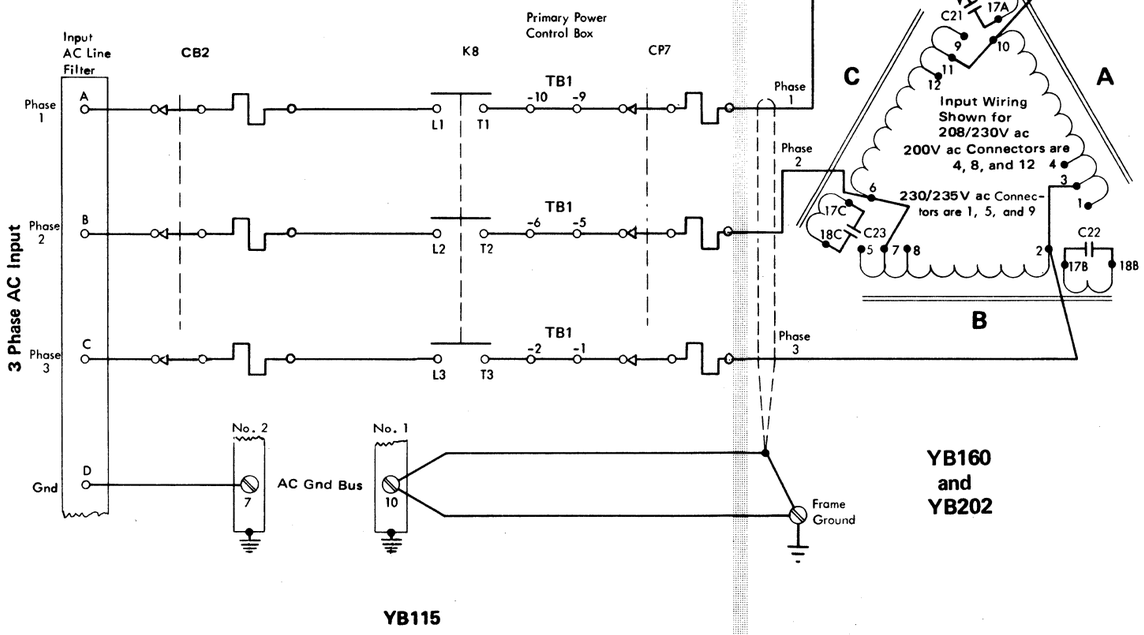
BULK 2 (CP7) POWER PROBLEM (Part 2 of 5)

SEE LOC 6,8, and 10 FOR COMPONENT LOCATION

BULK 2 SUPPLY

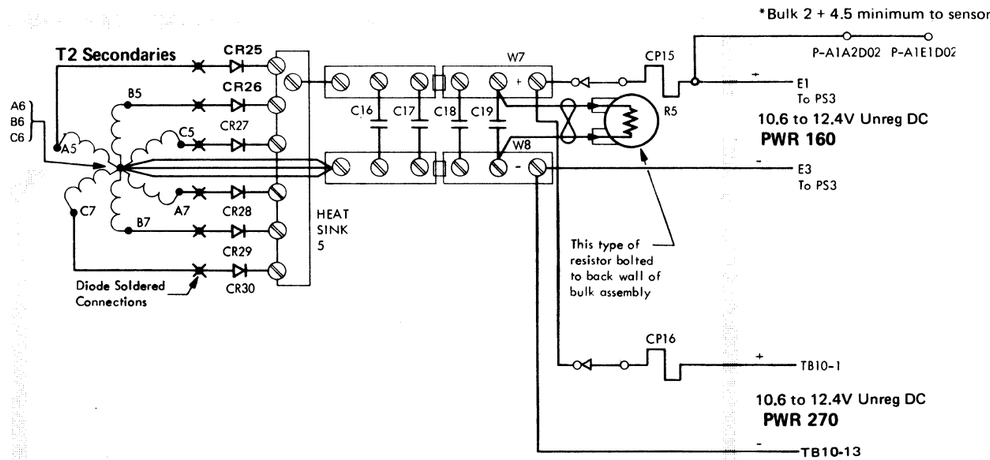
Ferroresonant Transformer T2
Δ Connection

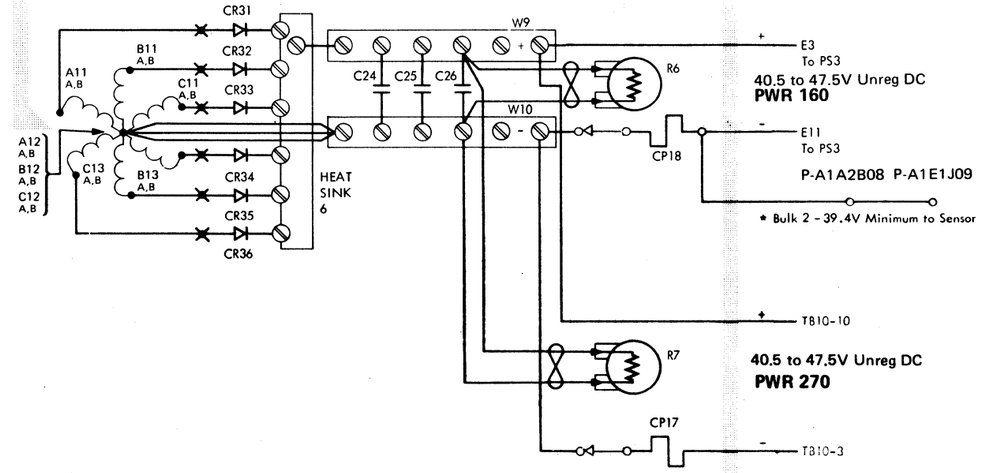
YB100/PWR 40



YB115

YB160 and YB202



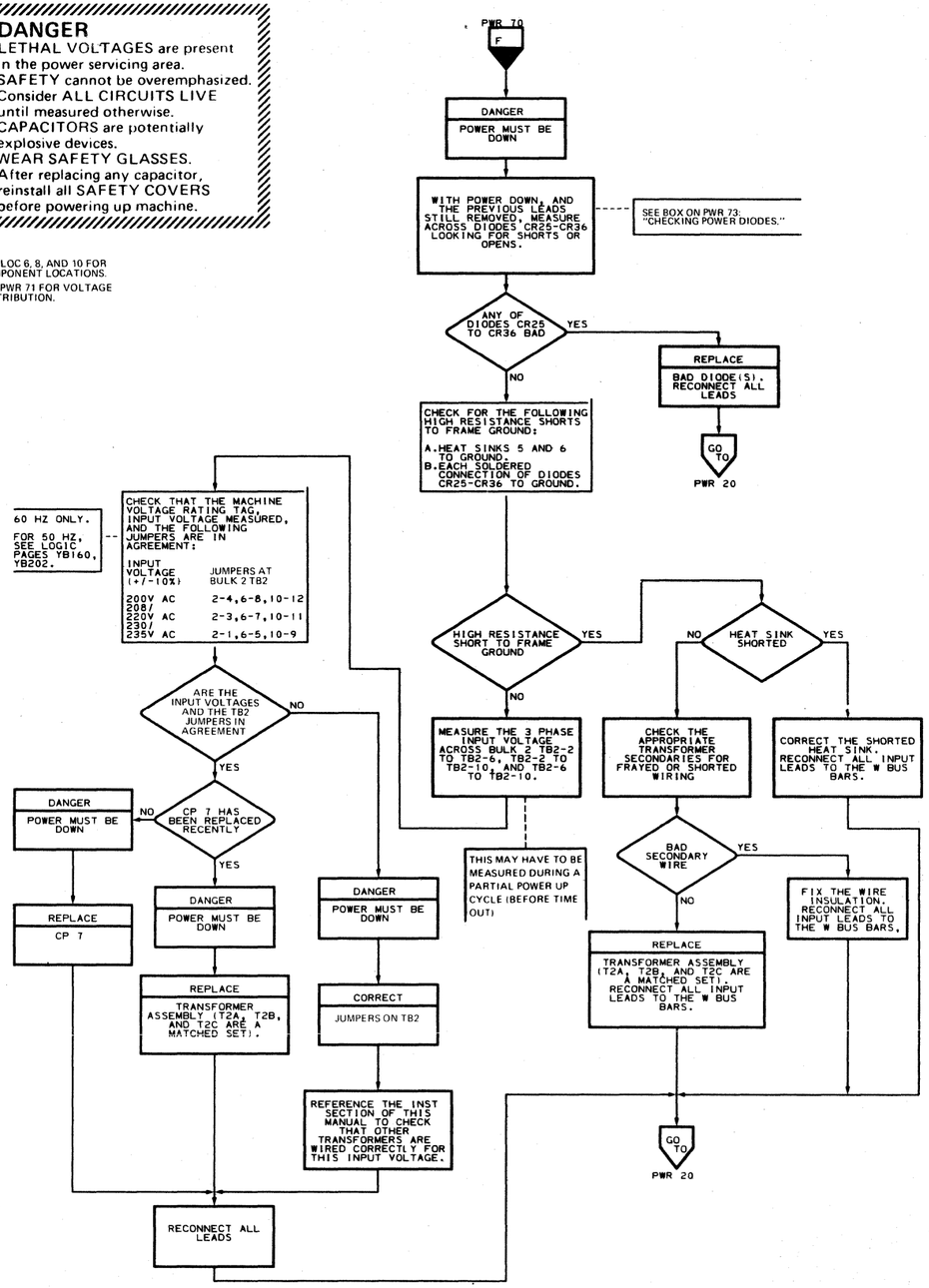


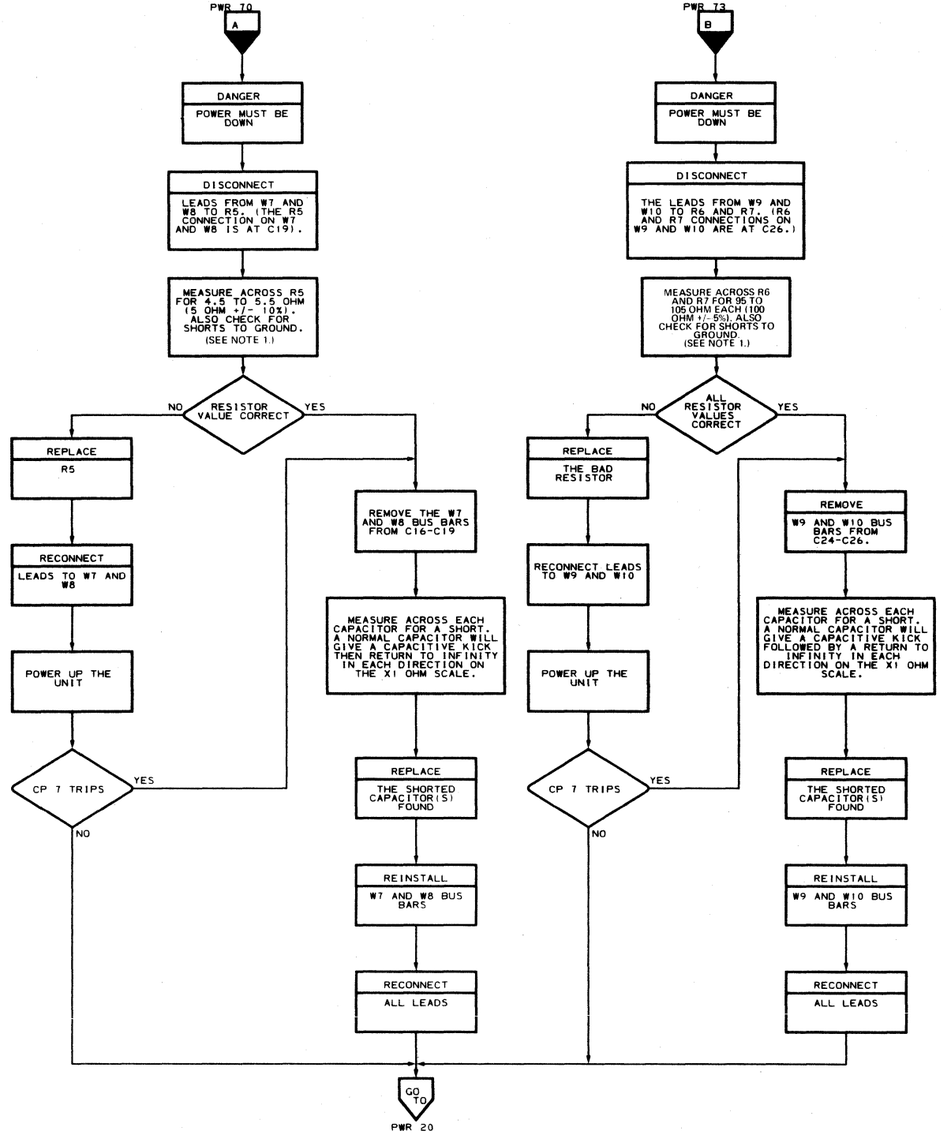
*These lines normally have the bulk voltage outputs shown. The minimum value indicated in the line name is what the sensor requires to consider bulk supplies normal. PLD sensor card on YB145.

BULK 2 (CP7) POWER PROBLEM (Part 3 of 5)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8, AND 10 FOR COMPONENT LOCATIONS.
- SEE PWR 71 FOR VOLTAGE DISTRIBUTION.



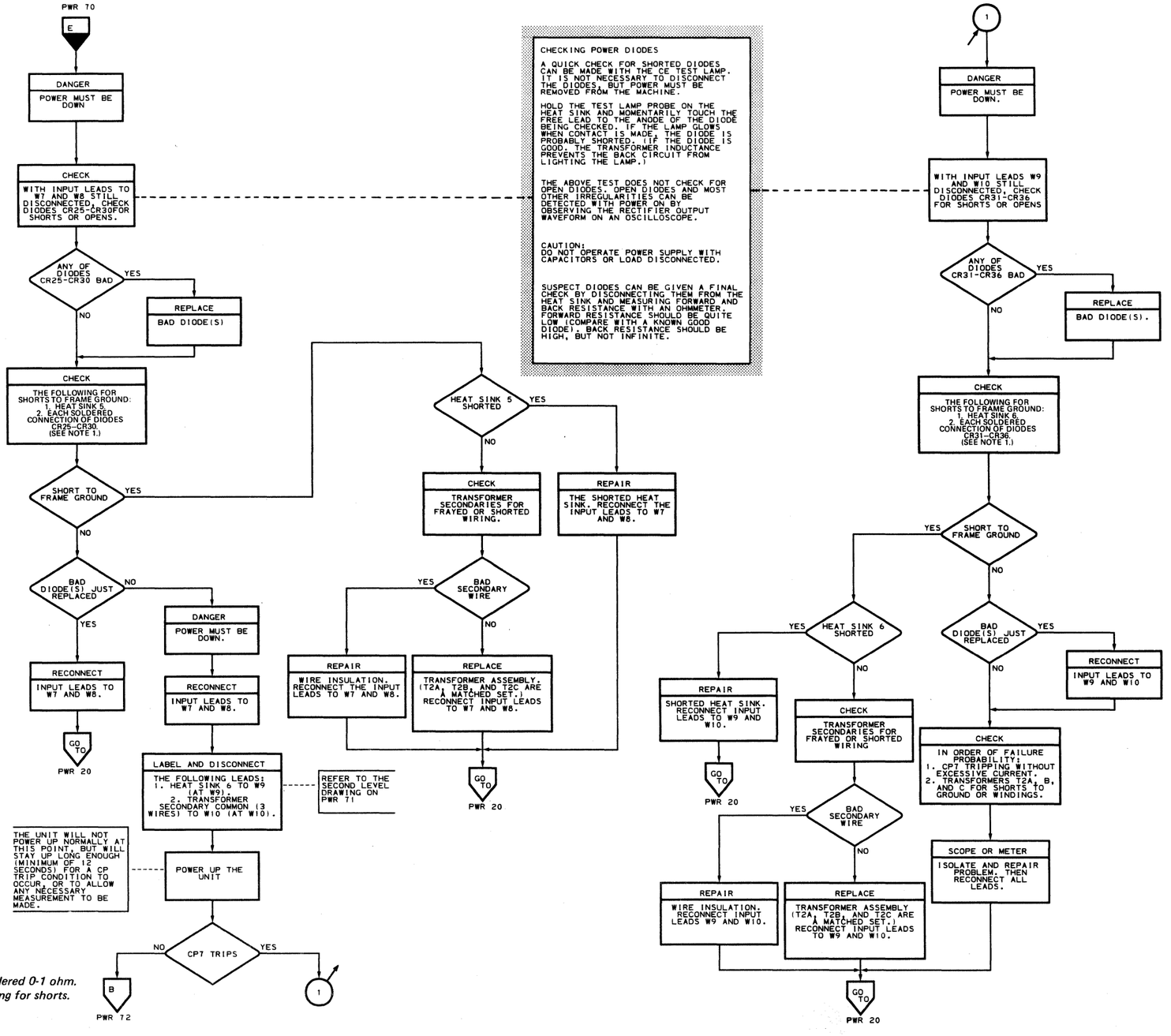


Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.

ONLY FOR EARLY MACHINES (WITH CP7) PWR 72

BULK 2 (CP7) POWER PROBLEM (Part 4 of 5)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.



Note 1: For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.

BULK 2 (CP7) POWER PROBLEM (Part 5 of 5)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 6, 8, AND 10 FOR COMPONENT LOCATIONS.
- SEE PWR 71 FOR VOLTAGE DISTRIBUTION.

(1)

DANGER
POWER MUST BE DOWN.

CHECK
THE FOLLOWING CAPACITORS FOR BLOWN OUT VENT CAPS:
1. C16-C19 AND C24-C26 (LOCATED UNDER/OR NEAR THE "W" BUS BARS THAT TIE THE CAPACITORS TOGETHER).
2. C21-C23 (MOUNTED ON THE BACK WALL OF BULK 2 NEAR PRE-LOAD RESISTORS (50 WATT) R1-R3 AND R5-R7).

BLOWN CAPACITORS? — YES

REPLACE
THE BLOWN CAPACITOR

GO TO PWR 20

NO

MEASURE THE INPUT THREE PHASE VOLTAGE ACROSS BULK 2 TB2-2 TO TB 2-6, TB 2-2 TO TB 2-10, AND TB 2-6 TO TB 2-10

THIS MAY HAVE TO BE MEASURED DURING A PARTIAL POWER UP CYCLE (BEFORE TIMEOUT)

CHECK THAT THE MACHINE VOLTAGE RATING TAG, INPUT VOLTAGE MEASURED, AND THE FOLLOWING JUMPERS ARE IN AGREEMENT:

60 HZ ONLY. FOR 50 HZ, SEE LOGIC PAGES YB160, YB202.

INPUT VOLTAGE (+- 10%)	JUMPERS AT BULK 2 TB 2
200V AC	2-4, 6-8, 10-12
208/220V AC	2-3, 6-7, 10-11
230/235V AC	2-1, 6-5, 10-9

INPUT VOLTAGE AND BULK TB 2 JUMPERS AGREE? — YES

NO

CORRECT JUMPERS ON BULK TB 2

REFERENCE THE INST SECTION OF THIS MANUAL TO CHECK THAT OTHER TRANSFORMERS ARE WIRED CORRECTLY FOR THIS INPUT VOLTAGE

GO TO PWR 20

DANGER
POWER MUST BE DOWN.

LABEL
AND DISCONNECT SLIP-ON CONNECTORS AT C21, C22 AND C23.

MEASURE THESE CAPACITORS FOR SHORTS OR OPENS. A NORMAL CAPACITOR WILL GIVE A "CAPACITIVE KICK" FOLLOWED BY A RETURN TO INFINITY IN BOTH DIRECTIONS ON THE X1 OHM SCALE.

CAPACITORS CORRECT? — NO

REPLACE
BAD CAPACITOR(S).

RECONNECT
ALL LEADS

YES

RECONNECT
LEADS TO CAPACITORS C21, C22 AND C23

FOR THE BULK 2 OUTPUT IN QUESTION, DISCONNECT AND MEASURE THE PROPER PRE-LOAD RESISTORS:

BULK 2 OUTPUT TO:	RESISTOR:	DISCONNECT (REF PWR 71):	OHM VALUE:
A. CP15 CP16	R5	LEADS AT W7 AND W8	4.5-5.5
B. CP17 CP18	R6 R7	LEADS AT W9 AND W10	95-105 EACH

PRE-LOAD RESISTORS VALUE CORRECT? — YES → (2)

NO

REPLACE
BAD PRE-LOAD RESISTOR(S)

GO TO PWR 20

PWR 100 AND 170

(U)

PWR 71

DURING A POWER UP CYCLE, MEASURE THE BULK 2 OUTPUT IN QUESTION FOR THE PROPER OUTPUT:

BULK 2 OUTPUT TO:	MEASURE:	VALUE:
1. PS3(+6V SECTION)	W7(+) TO W8(-)	10.6 TO 12.4V DC
2. PS3(-36V SECTION)	W9(+) TO W10(-)	40.5 TO 47.5V DC

(1) NO — VOLTAGES CORRECT? — YES

PWR 71

CHECK
FOR AN OPEN CP WITHOUT VISIBLE INDICATION. ALSO CHECK FOR AN OUTPUT WIRING PROBLEM IN THE POWER SUPPLY OR SENSING LOGIC.

REPAIR
OR REPLACE AS NECESSARY

GO TO PWR 20

(2)

LABEL AND DISCONNECT
THE PROPER SET OF LEADS FOR THE BULK 2 OUTPUT IN QUESTION:

BULK 2 OUTPUT TO:	DISCONNECT LEADS (REF PWR 71):
A. CP15 AND CP16	1. HEAT SINK 5 TO W7 (AT W7). 2. TRANSFORMER SECONDARY COMMON (THREE WIRES) TO W8 (AT W8).
B. CP17 AND CP18	1. HEAT SINK 6 TO W9 (AT W9). 2. TRANSFORMER SECONDARY COMMON (THREE WIRES) TO W10 (AT W10).

SEE BOX ON PWR 73 "CHECKING POWER DIODES."

FOR THE BULK 2 OUTPUT IN QUESTION, MEASURE THE PROPER GROUP OF DIODES FOR SHORTS OR OPENS:

BULK 2 OUTPUT TO:	MEASURE DIODES:
A. CP15 AND CP16	CR25-CR30
B. CP17 AND CP18	CR31-CR36

DIODE(S) BAD? — YES

REPLACE
BAD DIODE(S) RECONNECT ALL LEADS

GO TO PWR 20

NO

FOR THE BULK 2 OUTPUT IN QUESTION, DISCONNECT THE PROPER SET OF CAPACITORS THEN MEASURE FOR SHORTS OR OPENS:

A NORMAL CAPACITOR WILL GIVE A "CAPACITIVE KICK" FOLLOWED BY A RETURN TO INFINITY IN BOTH DIRECTIONS ON THE X1 OHM SCALE

BULK 2 OUTPUT TO:	DISCONNECT (REF PWR 71):	MEASURE ACROSS EACH CAPACITOR:
A. CP15 CP16	REMOVE W7 BUS FROM CAPACITOR BANK	C16-C19
B. CP17 CP18	REMOVE W9 BUS FROM CAPACITOR BANK	C24-C26

CAPACITOR(S) BAD? — NO

RECONNECT
ALL LEADS

REPLACE
TRANSFORMER ASSEMBLY. (T2A, T2B, AND T2C ARE A MATCHED SET).

YES

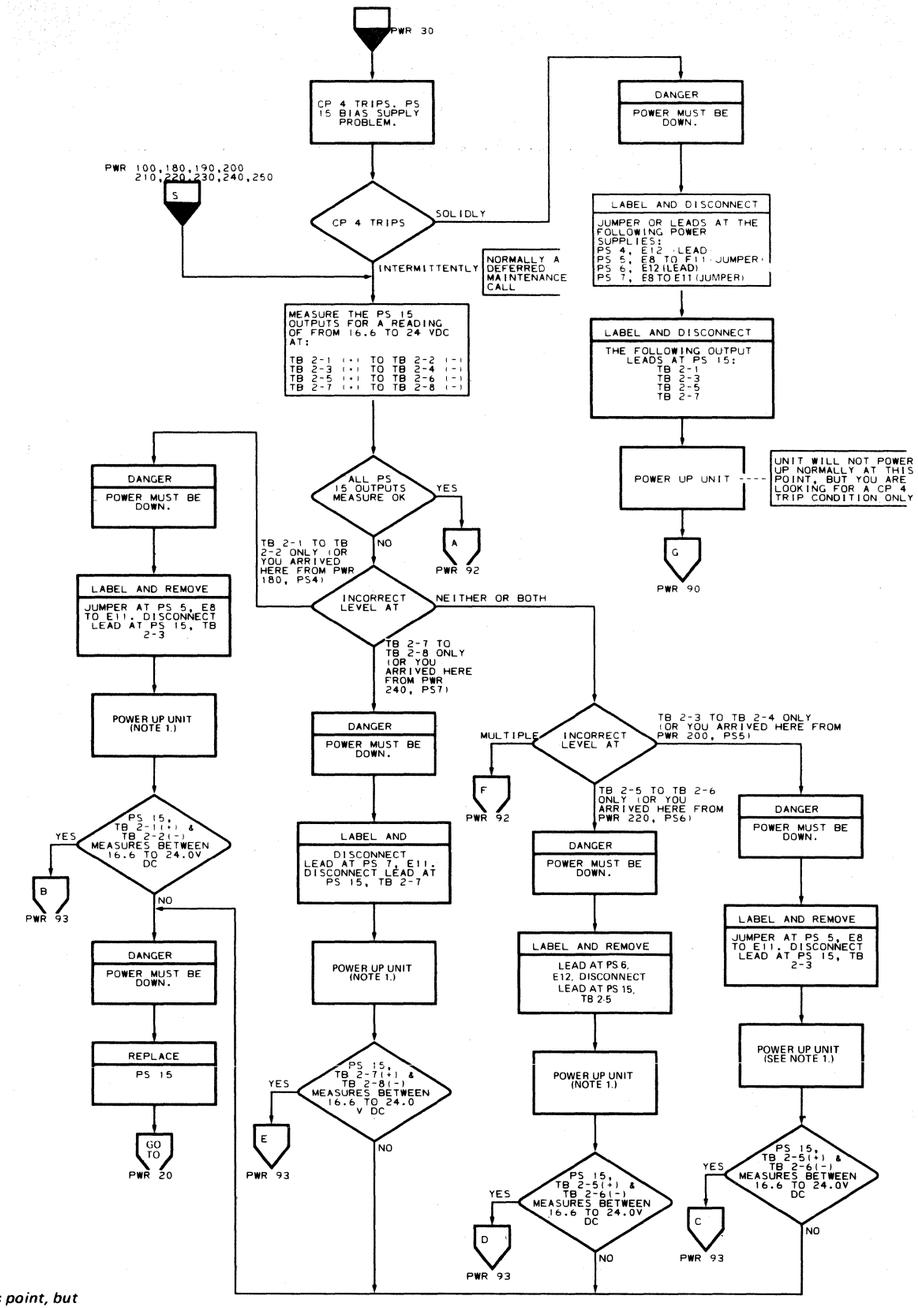
REPLACE
BAD CAPACITOR(S). RECONNECT ALL LEADS.

GO TO PWR 20

CP4 TRIPS (PART 1 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 10 FOR COMPONENT LOCATIONS
- SEE PWR 85 FOR EXTERNAL CIRCUIT AND LOCATIONS

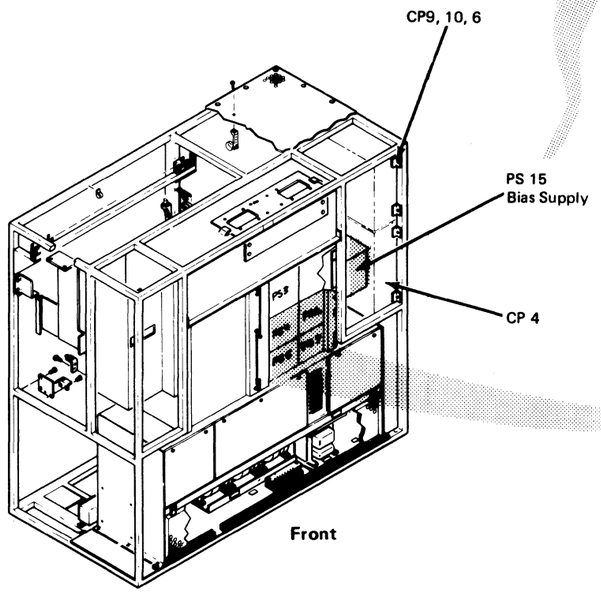


Note 1: Unit will not power up normally at this point, but should remain up long enough to make the required measurement.

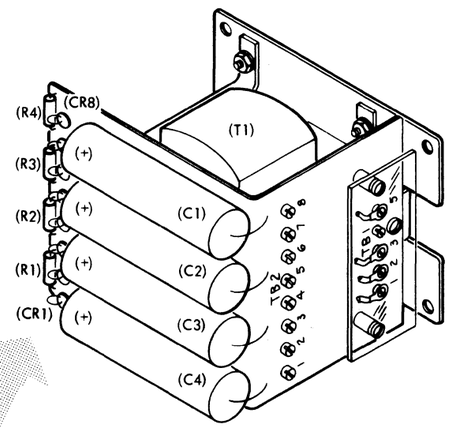
CP4 TRIPS (Part 2 of 6)

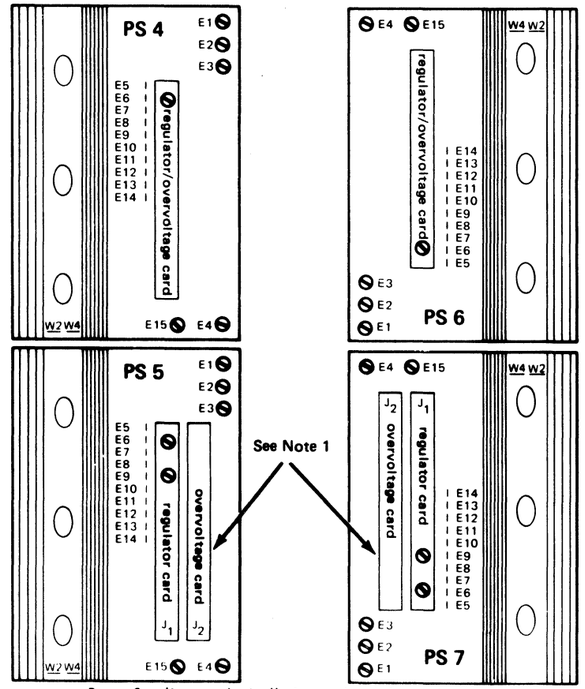
PS15 BIAS SUPPLY DISTRIBUTION

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.



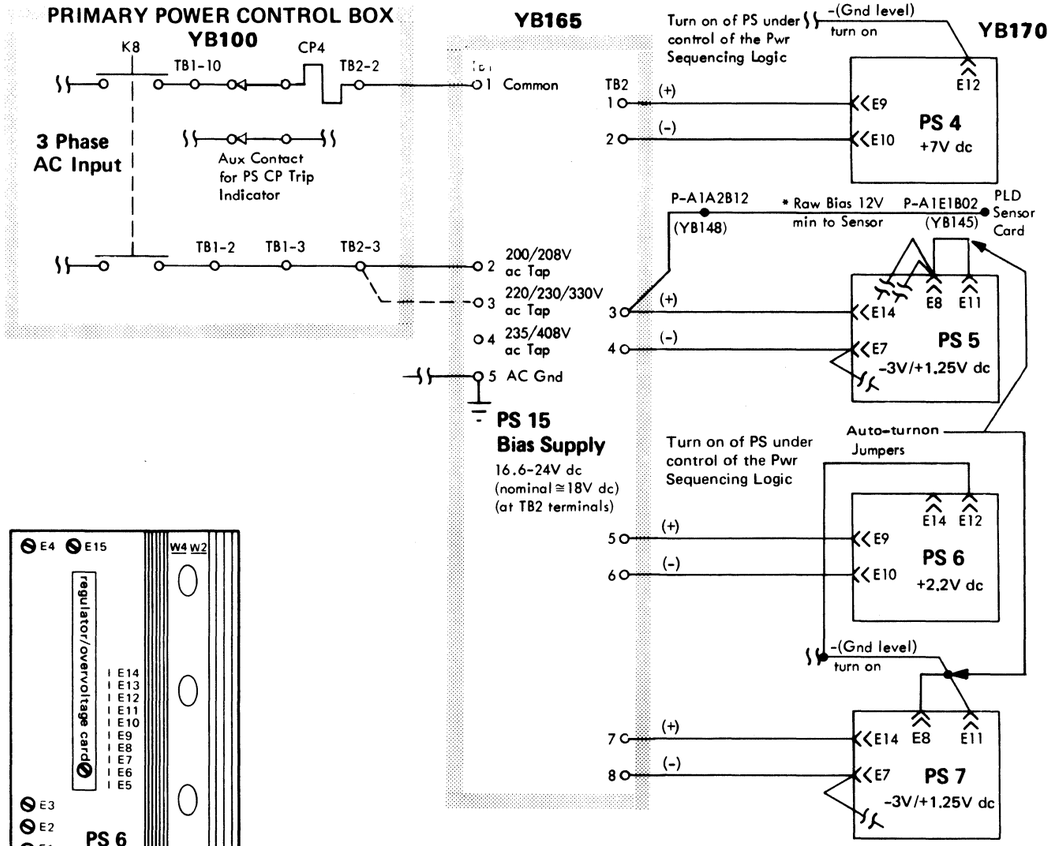
PS 15 Bias Supply





Power Supplies are physically inverted on left and right sides

Note 1: Overvoltage card not present if power supplies at EC 716230 or later.

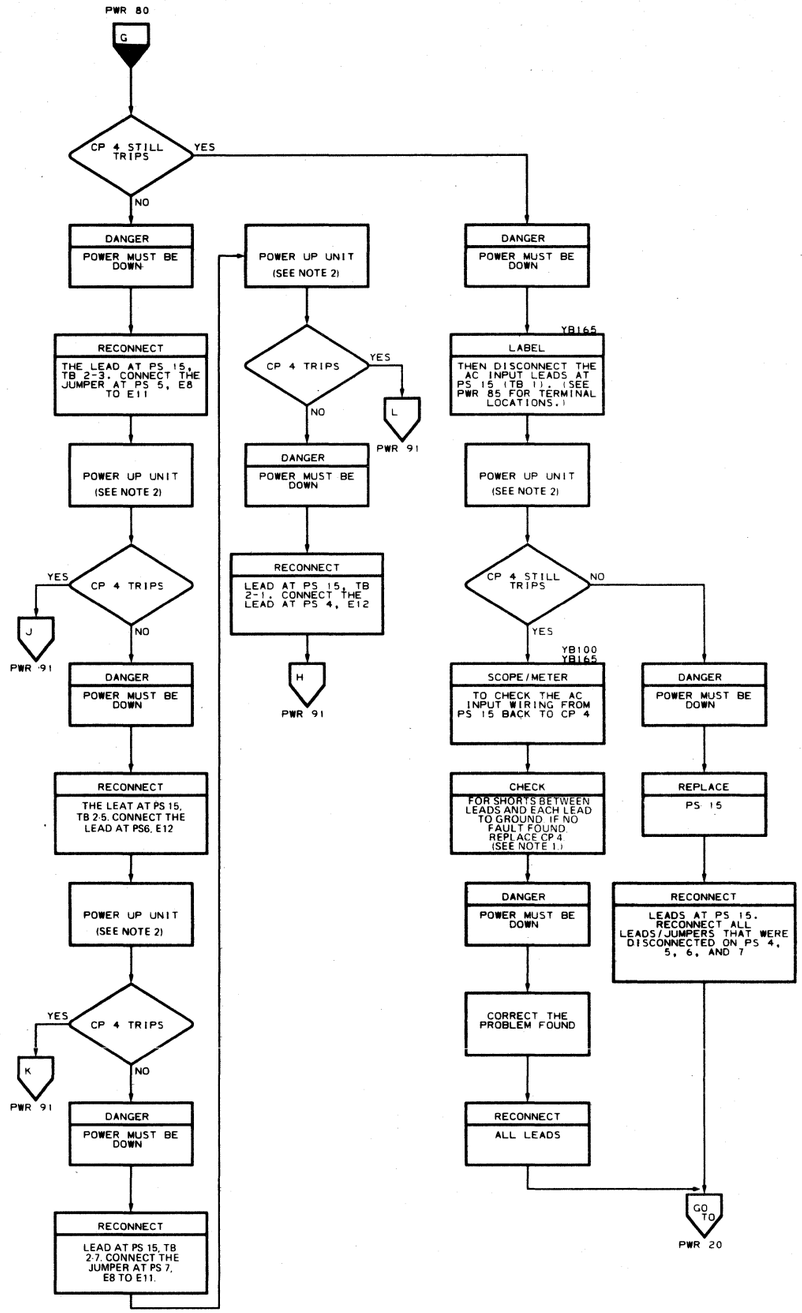


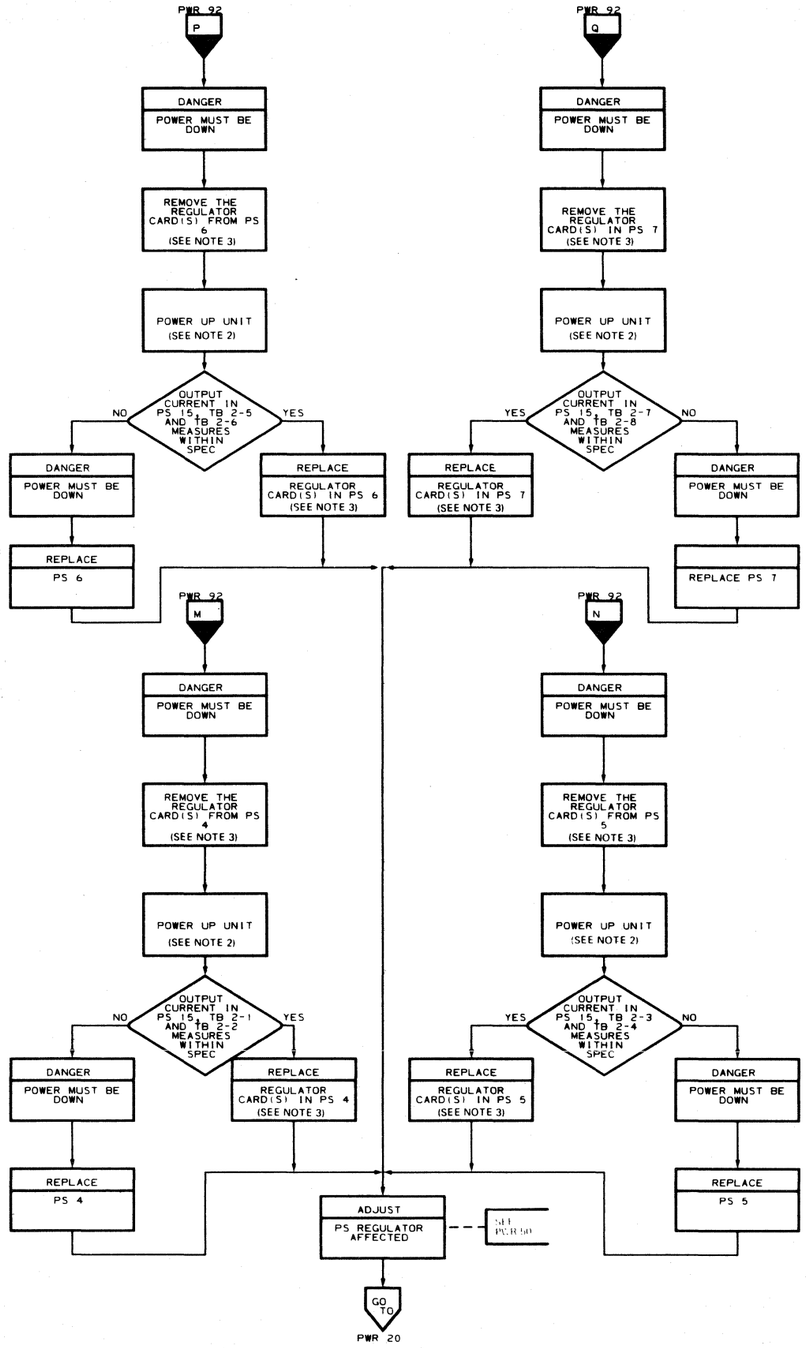
* This line normally has the bias voltage of +16.6 to 24 Vdc. The minimum value in the line name (+12V) is what the sensor requires to consider the bias supply normal.

CP4 TRIPS (PART 3 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 10 FOR COMPONENT LOCATIONS.
- SEE PWR 85 FOR EXTERNAL CIRCUIT AND LOCATIONS.





Note 1: For troubleshooting, a short is considered 0-1 ohm.

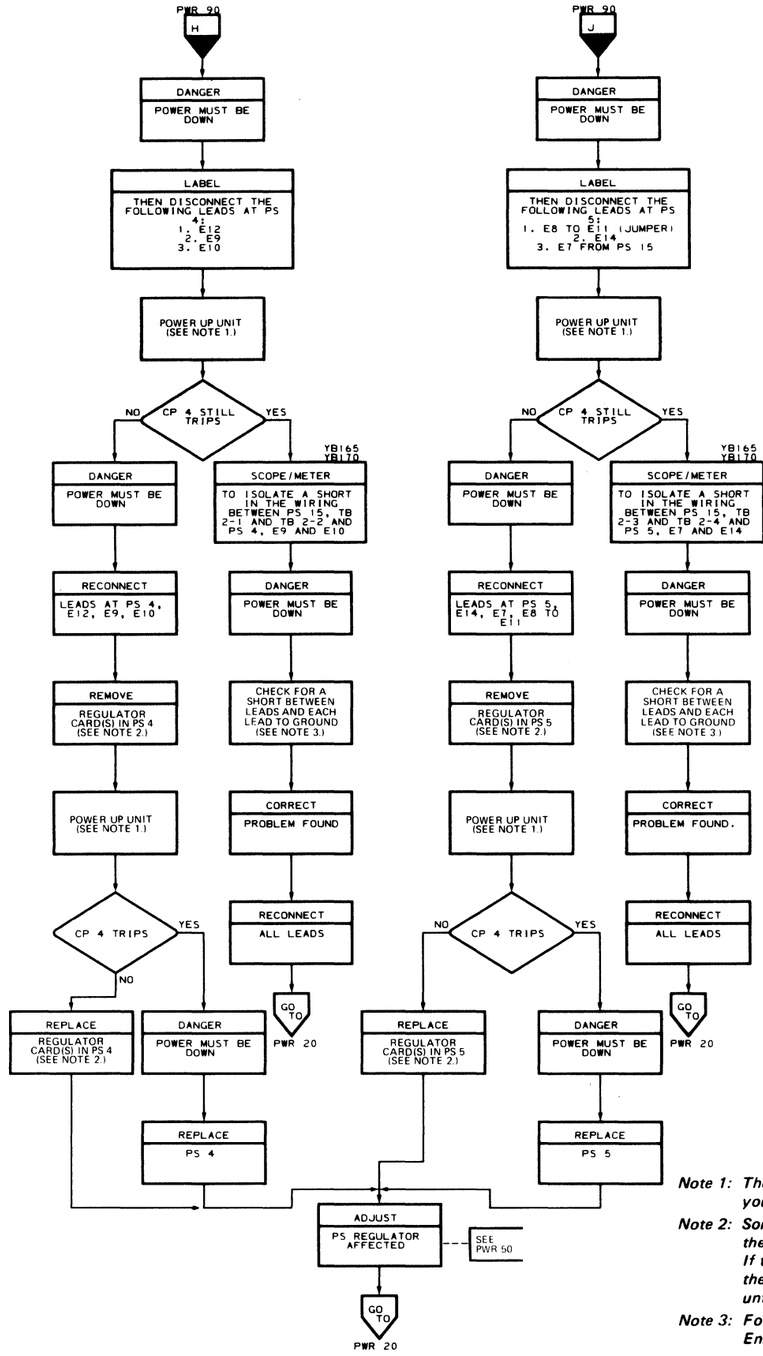
Note 2: Unit will not power up normally at this point, but should remain up long enough to make the required measurement or observe a CP trip.

Note 3: Some power supplies have two cards (one a regulator, the other overvoltage). If there are two cards in the power supply remove them both. If the measurement comes within specifications, insert one card at a time until the shorted card is found.

CP4 TRIPS (PART 4 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 10 FOR COMPONENTS LOCATIONS
- SEE PWR 85 FOR EXTERNAL CIRCUIT AND LOCATIONS



Note 1: The unit will not power up normally at this point, but you are looking for a CP 4 trip condition only.

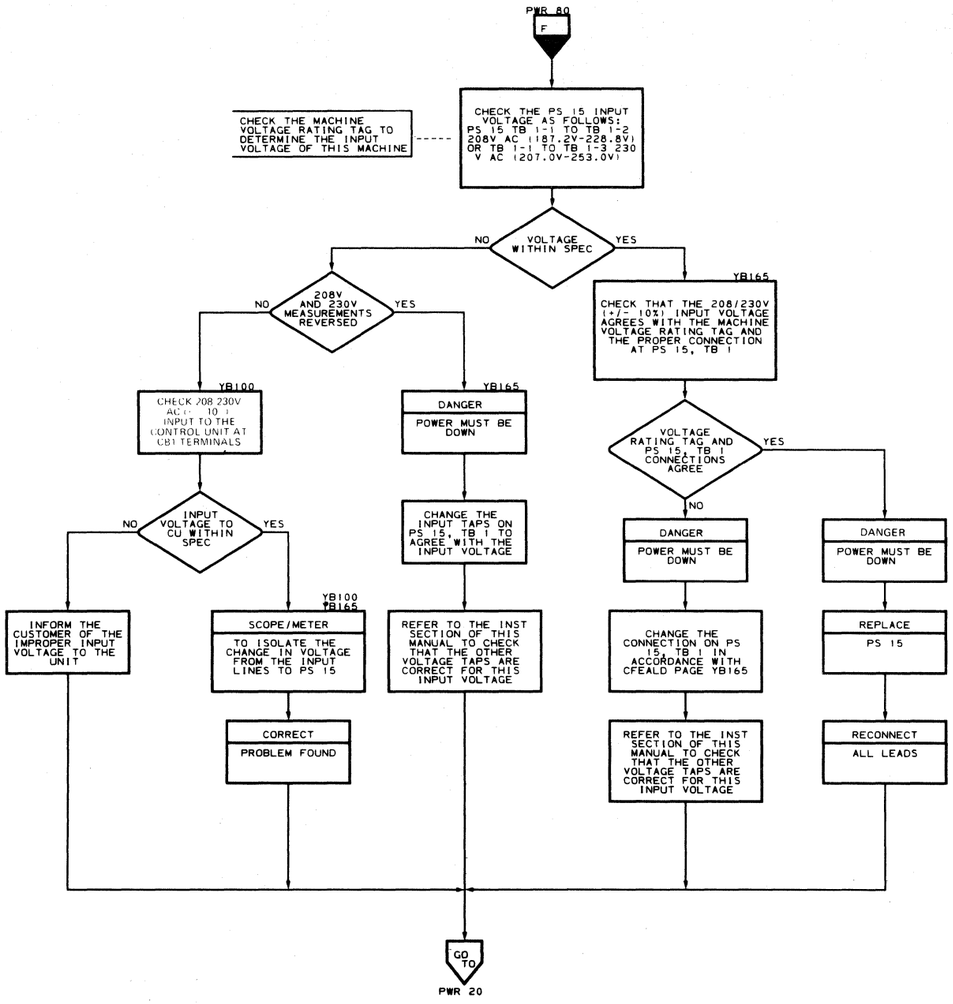
Note 2: Some power supplies have two cards (one a regulator, the other overvoltage).
If there are two cards in the power supply, remove them both. If the CP stops tripping, insert one at a time until the shorted card is found.

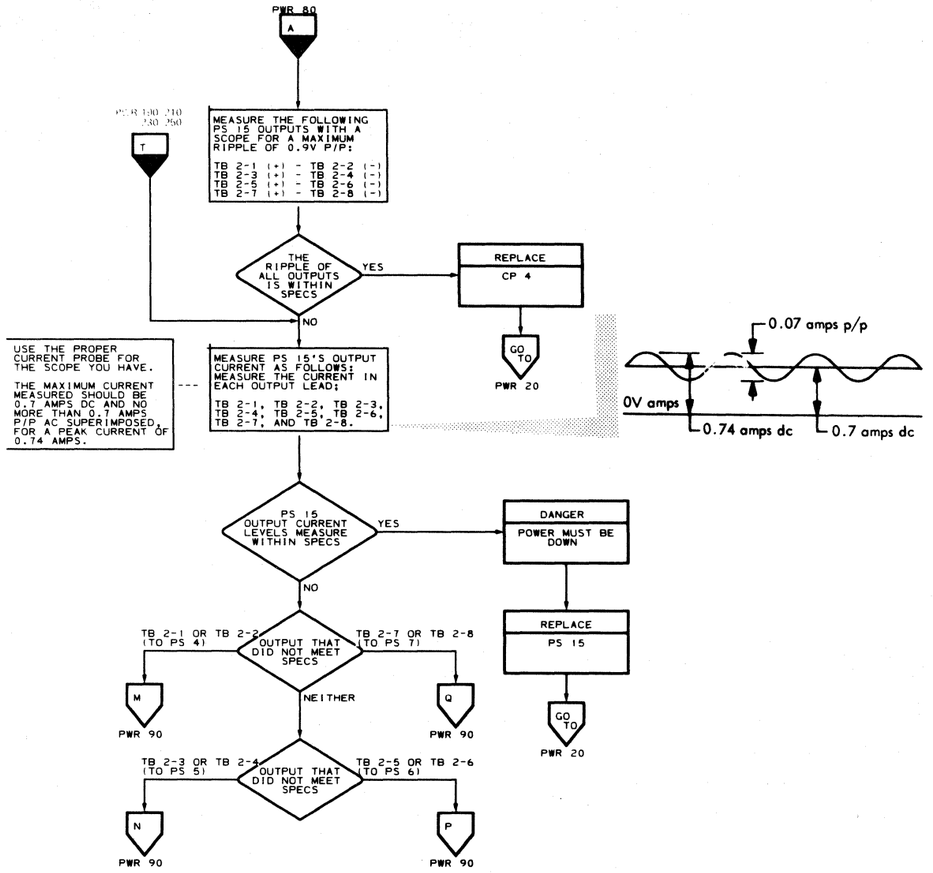
Note 3: For troubleshooting, a short is considered 0-1 ohms. Ensure meter is zeroed before checking for shorts.

CP4 TRIPS (PART 5 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 10 FOR COMPONENT LOCATIONS.
- SEE PWR 85 FOR EXTERNAL CIRCUIT AND LOCATIONS.

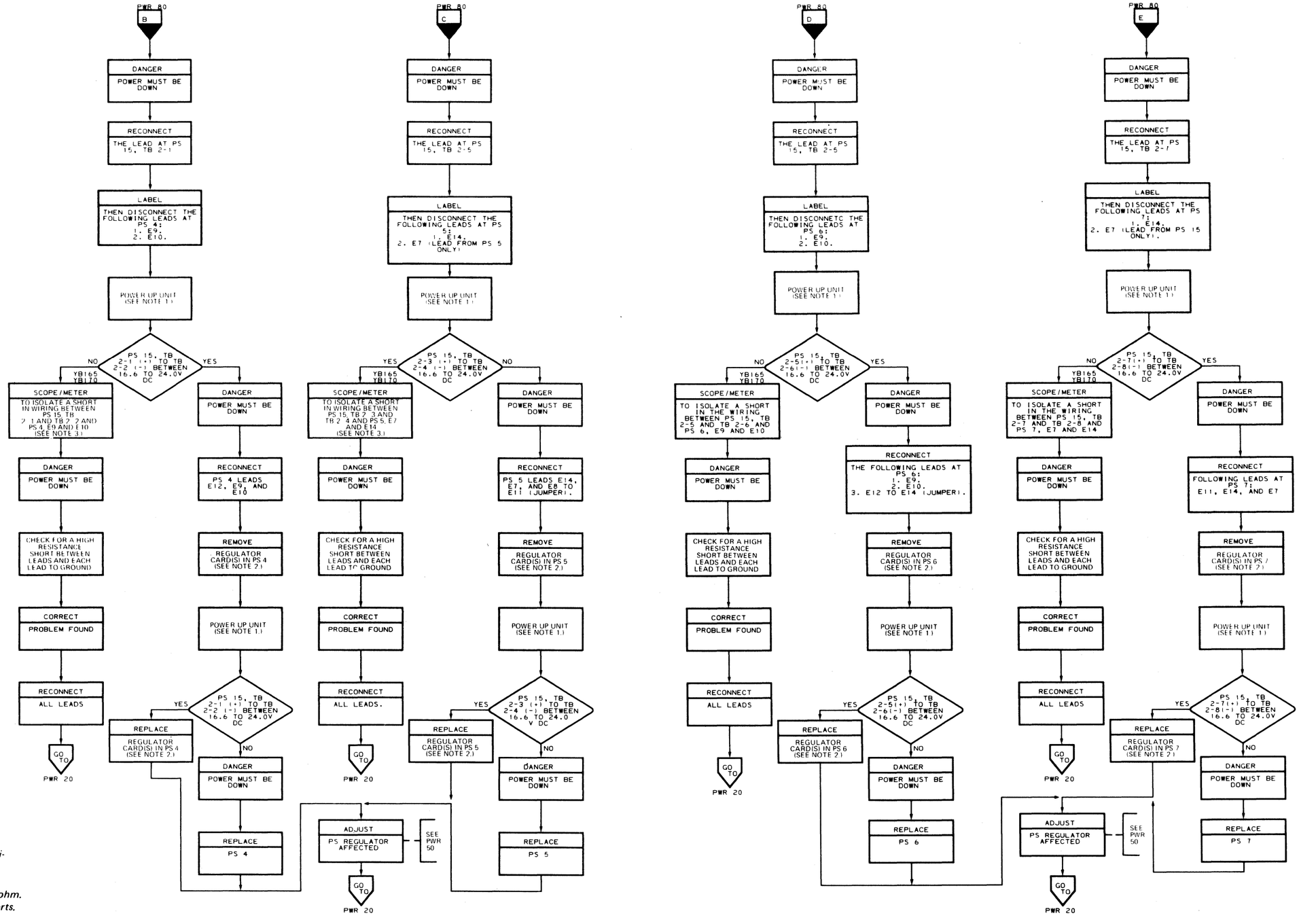




CP4 TRIPS (PART 6 OF 6)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE LOC 10 FOR COMPONENT LOCATIONS
- SEE PWR 85 FOR EXTERNAL CIRCUIT AND LOCATIONS



Note 1: *Unit will not power up normally at this point, but should remain up long enough to make the required measurement.*

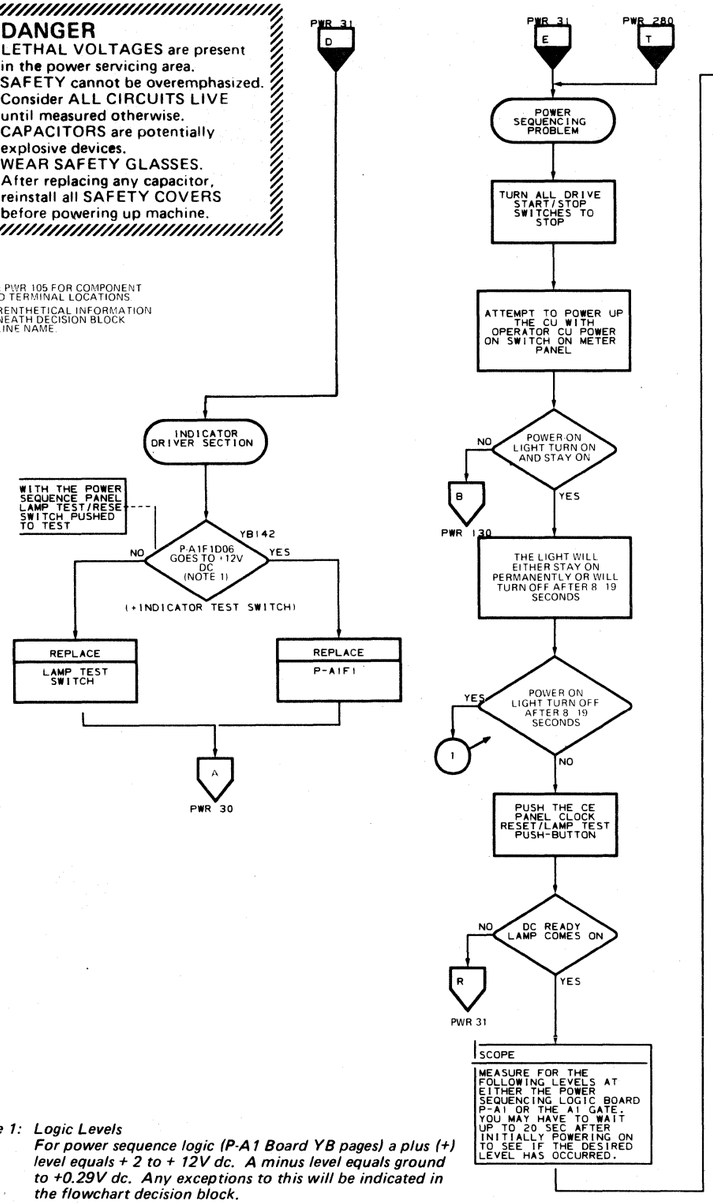
Note 2: *Some power supplies have two cards (one a regulator, the other overvoltage). If there are two cards in the power supply, remove them both. If the measurement comes within specifications, insert one at a time until the shorted card is found.*

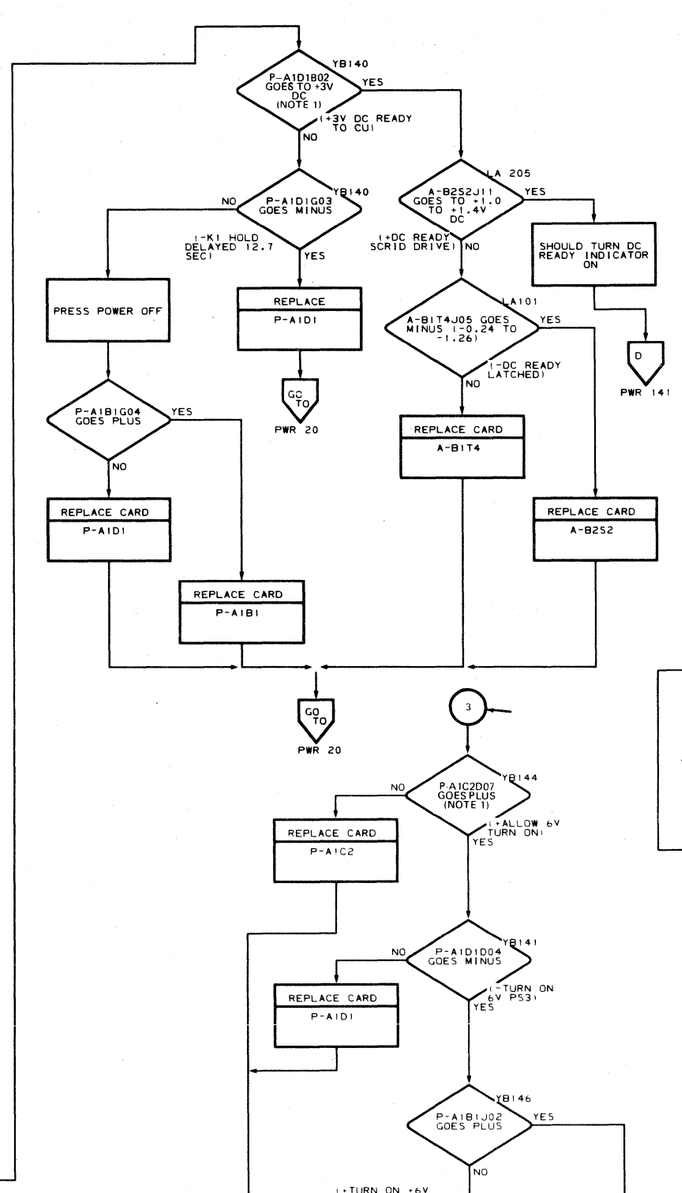
Note 3: *For troubleshooting, a short is considered 0-1 ohm. Ensure meter is zeroed before checking for shorts.*

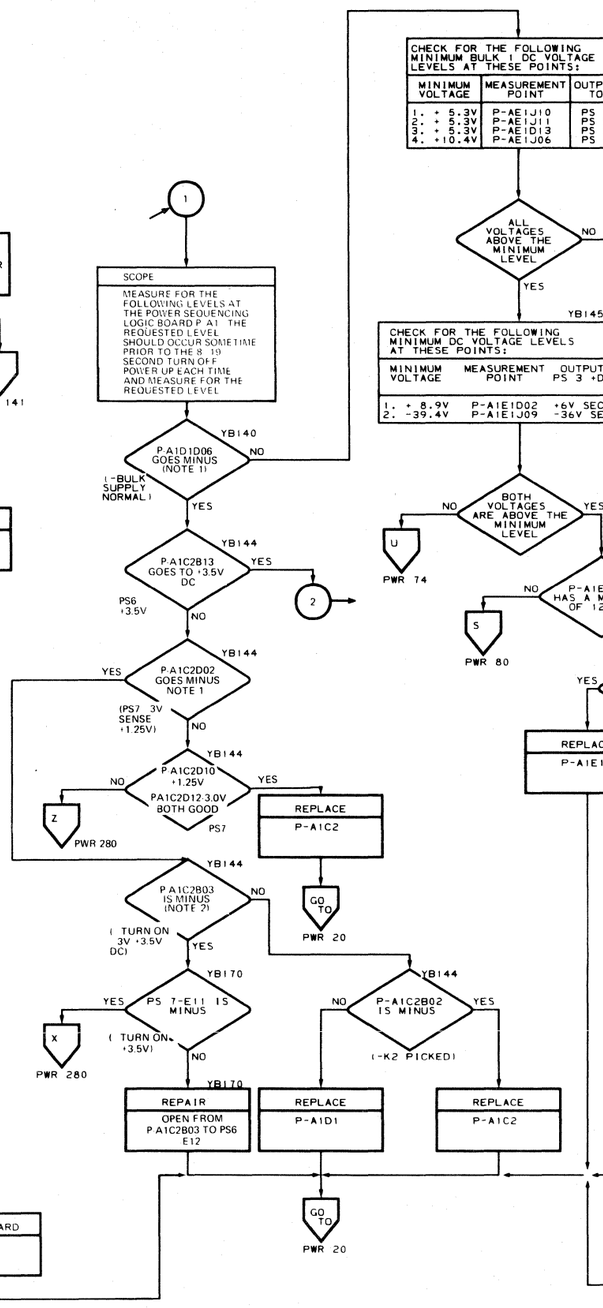
POWER SEQUENCE PROBLEM (PART 1 OF 7)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE PWR 105 FOR COMPONENT AND TERMINAL LOCATIONS
- PARENTHETICAL INFORMATION BENEATH DECISION BLOCK IS LINE NAME







Note 1: Logic Levels
For power sequence logic (P-A1 Board YB pages) a plus (+) level equals + 2 to + 12V dc. A minus level equals ground to +0.29V dc. Any exceptions to this will be indicated in the flowchart decision block.

Note 2: When operating normally; this line will be minus (gnd) with power off. On pushing power on and when K8 is heard picking, the line will go plus for an instant and then go minus to turn on the power supply. When power off is pushed, the line will go plus until K8 is heard dropping, at that time the line will slowly decay to a minus (gnd) level over approximately a five (5) second period.

POWER SEQUENCE PROBLEM (Part 2 of 7)

3830-2 POWER SEQUENCE THEORY AND LOCATIONS

As long as the control unit is connected to the ac supply source and circuit breakers are normal, 24V dc and 12V dc are available at the power sequencing logic panel.

Two Step Process to Produce Final Regulated Voltages

The power supply area produces accurately controlled voltages in a two step process. Bulk supplies 1 and 2 produce six partially regulated dc voltage outputs at levels considerably higher than eventually required. Several highly accurate voltage regulator units (referred to in the diagrams as PS 3, PS 5, PS 6, etc.) produce final regulated voltages from the bulk voltage outputs.

Power supply regulators PS 4, PS 5, PS 6, and PS 7 each have terminals which are used for on-off control of the individual supply. When these terminals are jumpered together, normal output voltage is produced. When the connection between the terminals is removed, output voltage goes to zero. Voltage turn on of PS4 and PS 6 is accomplished remotely by connecting the terminals together with a relay driver-type circuit located in the power sequencing logic area. Power supply regulator PS 3 differs from the other regulators in its method of turn on/turn off. In this supply, a particular terminal must be grounded to remove the output voltage. The supply is remotely turned on by opening the ground connection to the terminal with a relay driver-type circuit located in the sequencing logic area.

Turn on terminals for power supply regulators PS 5 and PS 7 are permanently jumpered at the supply itself. The output of these supplies is dependent on the bulk supplies, which are controlled by a contactor in the ac line (K8).

Power Supply Sequencing for CU Control Storage

Contactor K8 applies ac to the inputs of the bulk supplies. The output voltage of PS 7 begins to rise as its bulk voltage input rises. When the voltage reaches a certain level, a special voltage sensing circuit turns PS 6 on (-3/+1.25V dc).

Controlled Delay in 6V Supply

The 6V dc supply to the channel interface is turned on only when: (1) bulk supply voltage outputs are normal, PS 4 is up, and all thermals are normal; and (2) approximately 12 seconds delay has elapsed following initiation of start sequence.

Timer Operation for Power-Up Sequence Control and Automatic Verification

The principal events in the power up sequencing of the control unit are controlled by a timer consisting of two delay units in series. The timing action is initiated by the closure of the K1-1 points.

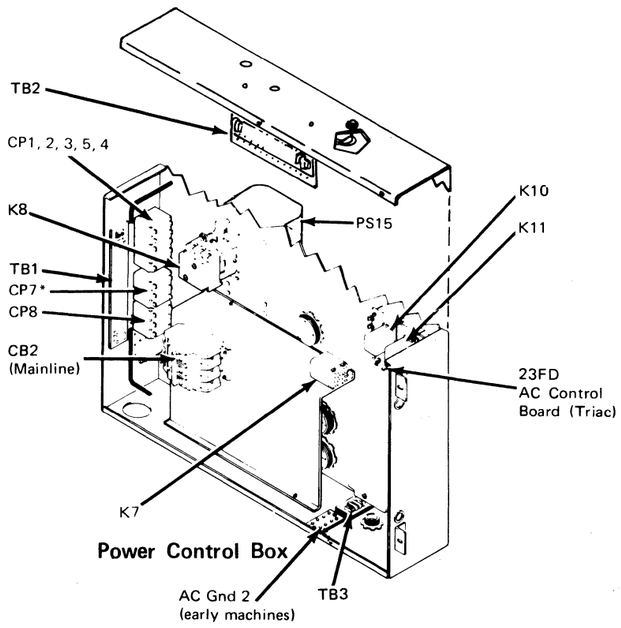
The first output of the timer occurs after a delay of approximately 12 seconds. This output allows turn on of the 6V supply (which supplies the channel interface area). The second output occurs approximately 0.7 seconds later. It tests for presence of all bulk supply voltages and 6V dc. This test is even more comprehensive in that the turn on of the 6V supply is contingent upon proper output of other power supplies and thermal contact conditions. The DC Ready (to control unit) light on the CE panel is also turned on at this time if voltage output and other conditions appear to be normal in the power area.

Anti-Recycle Latch

The anti-recycle flip-flop is set each time the system power on stepper switch initiates a power on sequence. It remains set until the stepper switch contacts open. When K1 drops, it cannot be picked up again until the anti-recycle flip-flop is reset. This reset occurs only when the stepper switch contacts open.

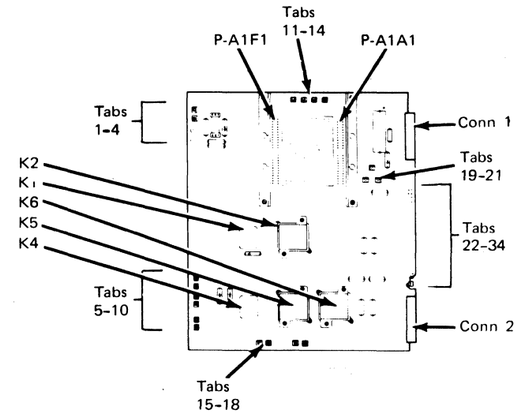
Voltage to be Expected at the Output of a Relay Driver

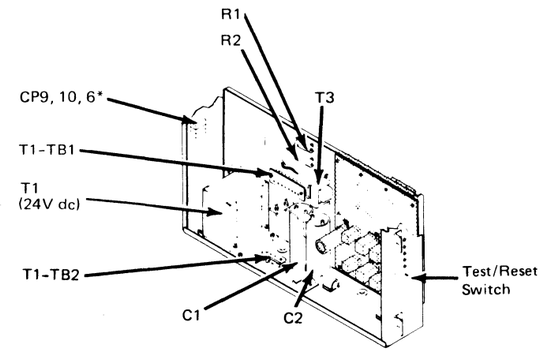
The output of a relay driver circuit will measure: (1) ground if the driver is in the "on" condition or the relay circuit itself is open (therefore no 24V), or (2) 24V if the driver is in the "off" condition and the relay circuit is complete to the 24V source.



Power Control Box

*Not on late machines.





Power Sequence Box

Relay	Functions	Coil Logic Page	Contact Logic Page
K1	Power up sequence pick relay	YB120	YB120
K2	Power up sequence hold relay	YB120	YB120
K3A	Auxiliary power up sequencing complete relay. (with two channel switch addition)	YB121	YB121
K4	Facility power up sequencing complete relay	YB120	YB120
K5	EPO control relay	YB120	YB120
K6	MPL File dc relay	YB120	YB121
K7	AC to cconvenience outlet	YB120	YB101
K8	Distribute ac to control unit	YB120	YB100
K10	MPL file K11 controller relay	YB120	YB100
K11	AC to MPL file	YB120	YB120
K13	Use Meter controller (41V ac to use meter)	YB121	YB121

Logic Card Position	Function/Logic Page
P-A1A1	12V dc regulator (YB143)
P-A1B1	12 and 12.7 second timers, 6V sensor (YB146)
P-A1C2	Memory power sequencing (YB144)
P-A1D1	Power sequencing condition control (YB140 and 141)
P-A1E1	PLD sensor card (YB145)
P-A1F1	Indicator driver card (YB142)

POWER SEQUENCE PROBLEM (Part 3 of 7)

VOLTAGE SEQUENCING LOGIC

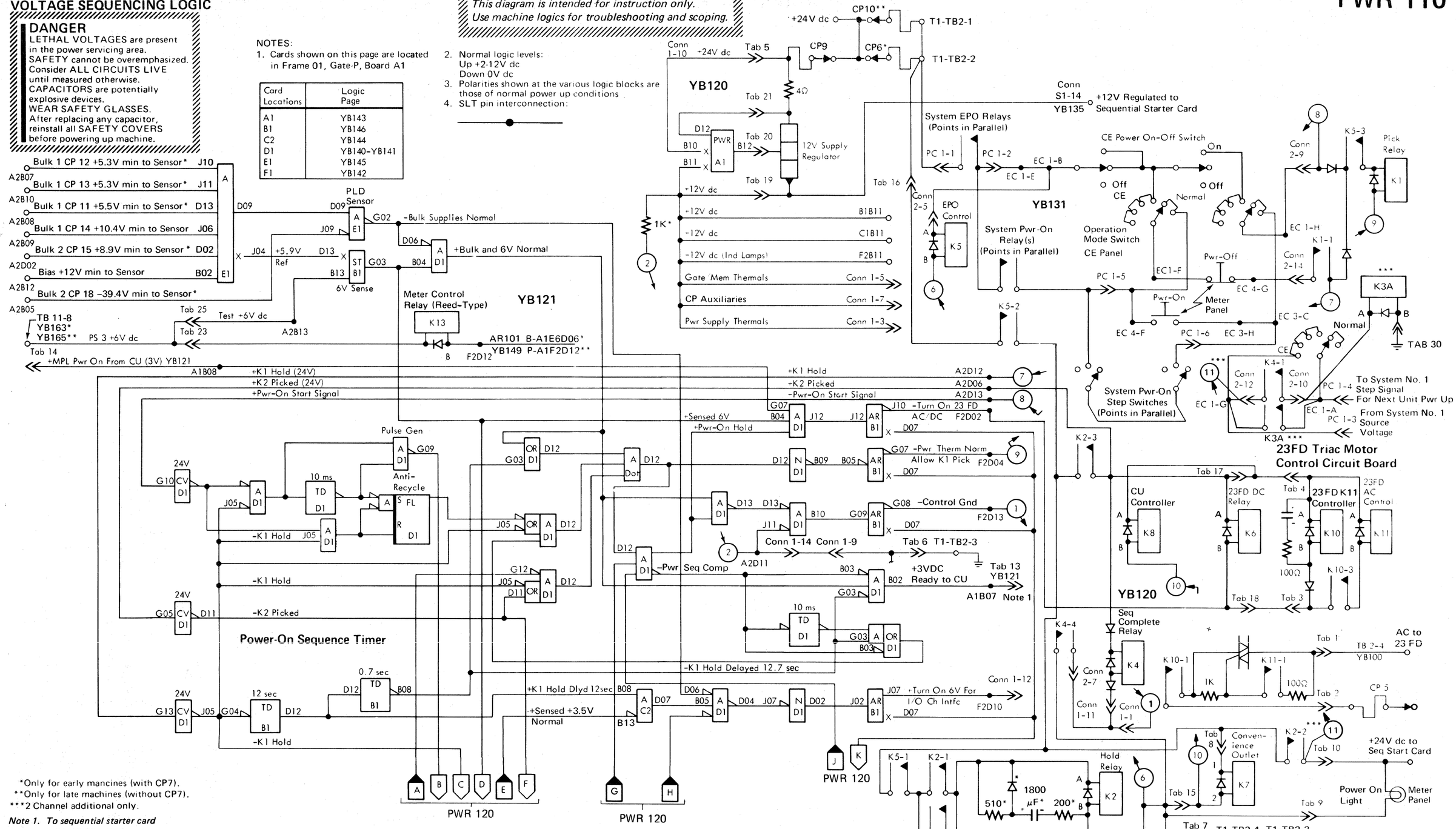
DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

NOTES:
1. Cards shown on this page are located in Frame 01, Gate-P, Board A1

Card Locations	Logic Page
A1	YB143
B1	YB146
C2	YB144
D1	YB140-YB141
E1	YB145
F1	YB142

2. Normal logic levels:
Up +2-12V dc
Down 0V dc
3. Polarities shown at the various logic blocks are those of normal power up conditions
4. SLT pin interconnection:



*Only for early mancines (with CP7).
**Only for late machines (without CP7).
***2 Channel additional only.

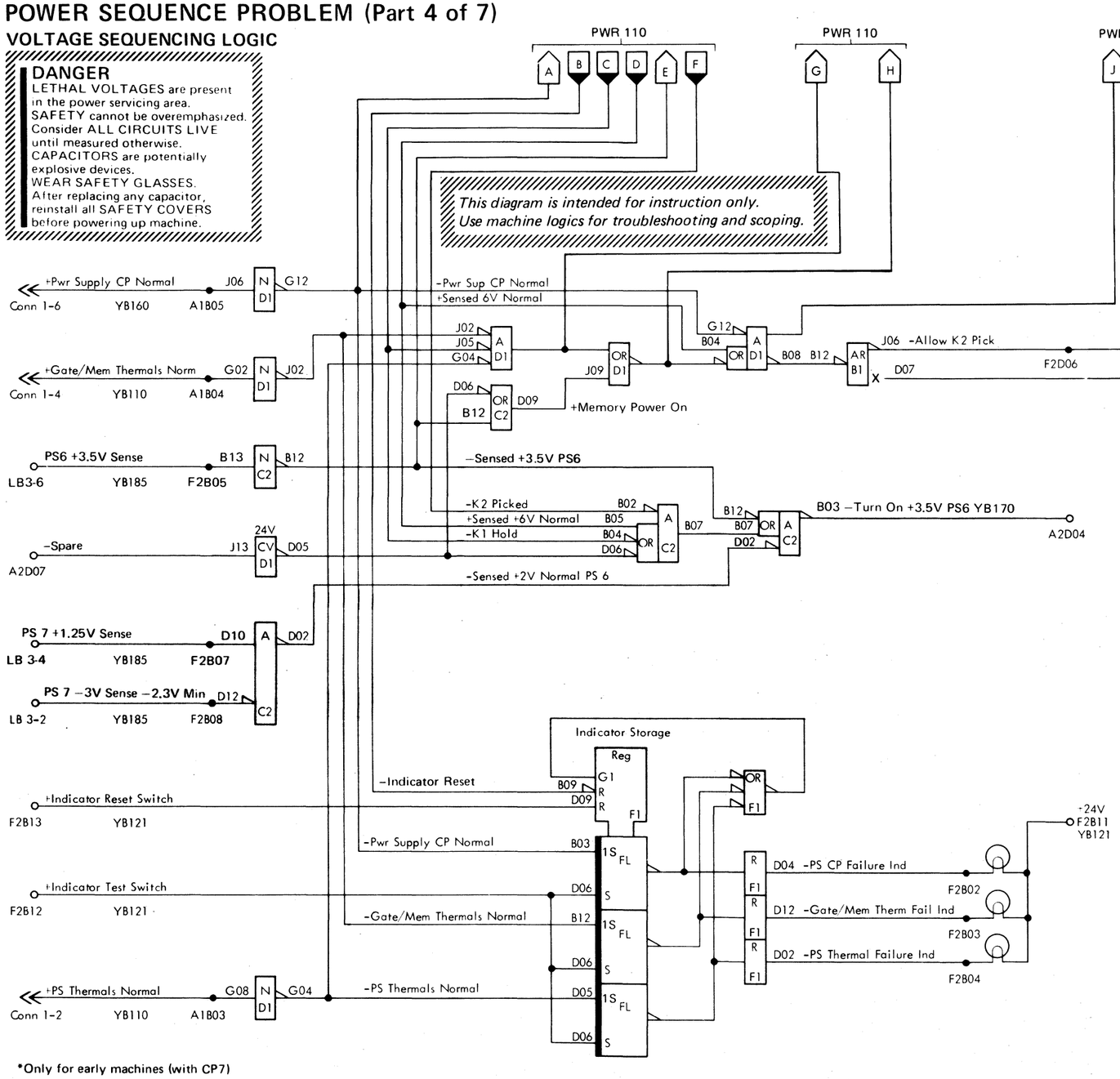
Note 1. To sequential starter card connector S1-17 (TY 135)

POWER SEQUENCE PROBLEM (Part 4 of 7)

VOLTAGE SEQUENCING LOGIC

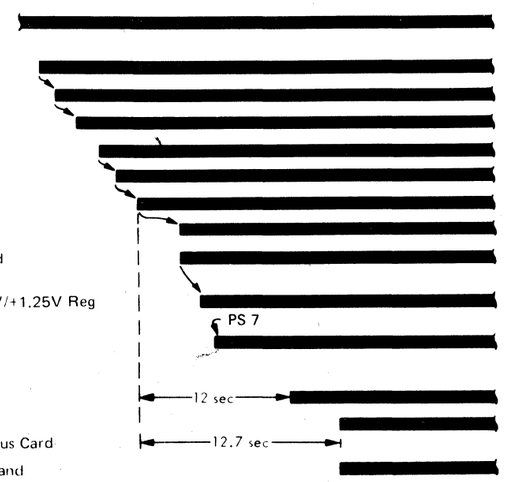
DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

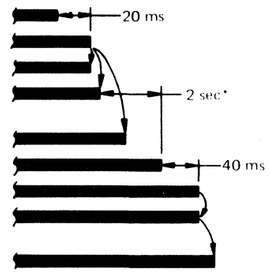


*Only for early machines (with CP7)

Normal Power Up



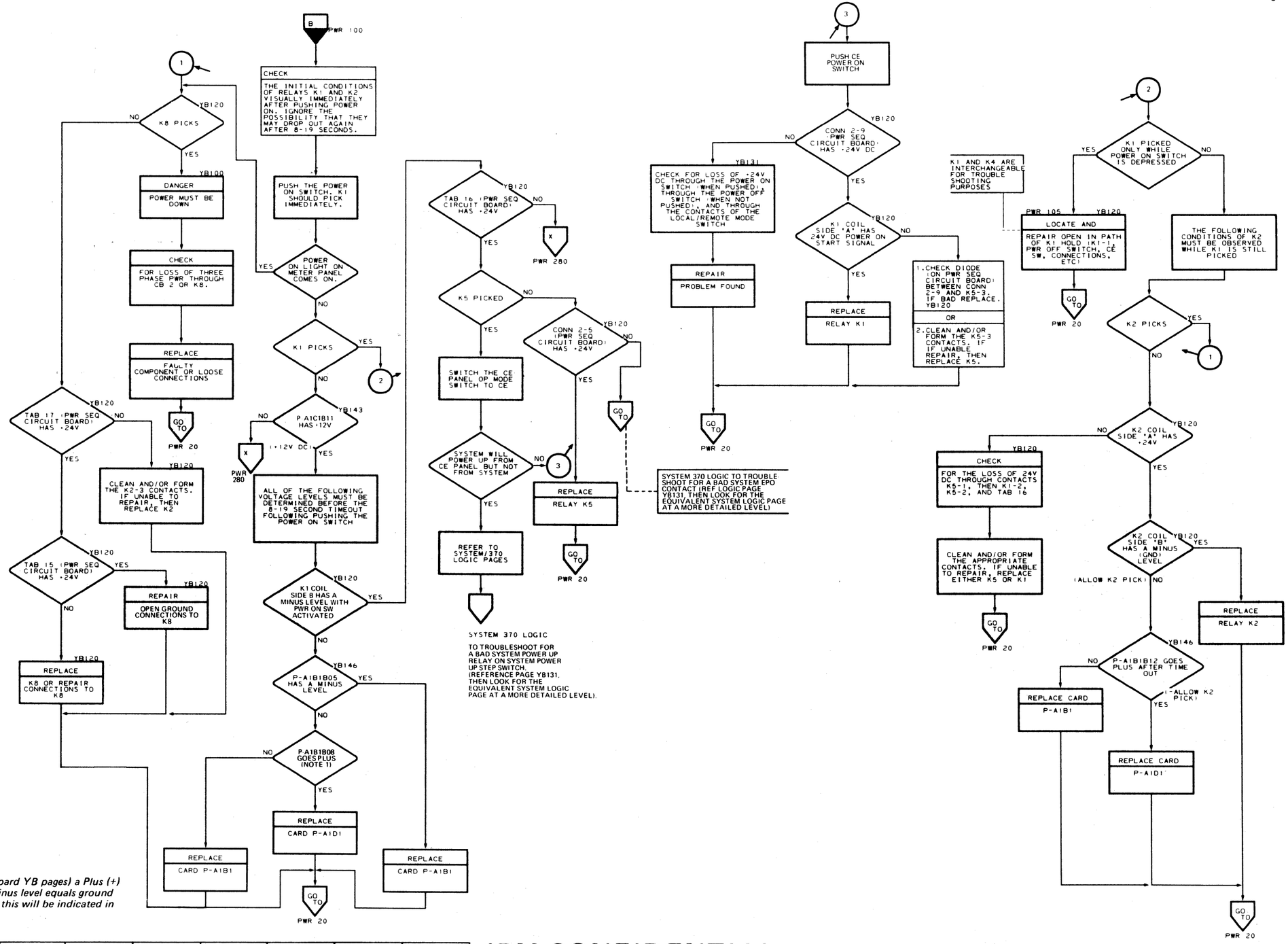
Normal Power Down



POWER SEQUENCE PROBLEM (PART 5 OF 7)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE PWR 105 FOR COMPONENT AND TERMINAL LOCATIONS.
- PARENTHETICAL INFORMATION BENEATH DECISION BLOCK IS LINE NAME.

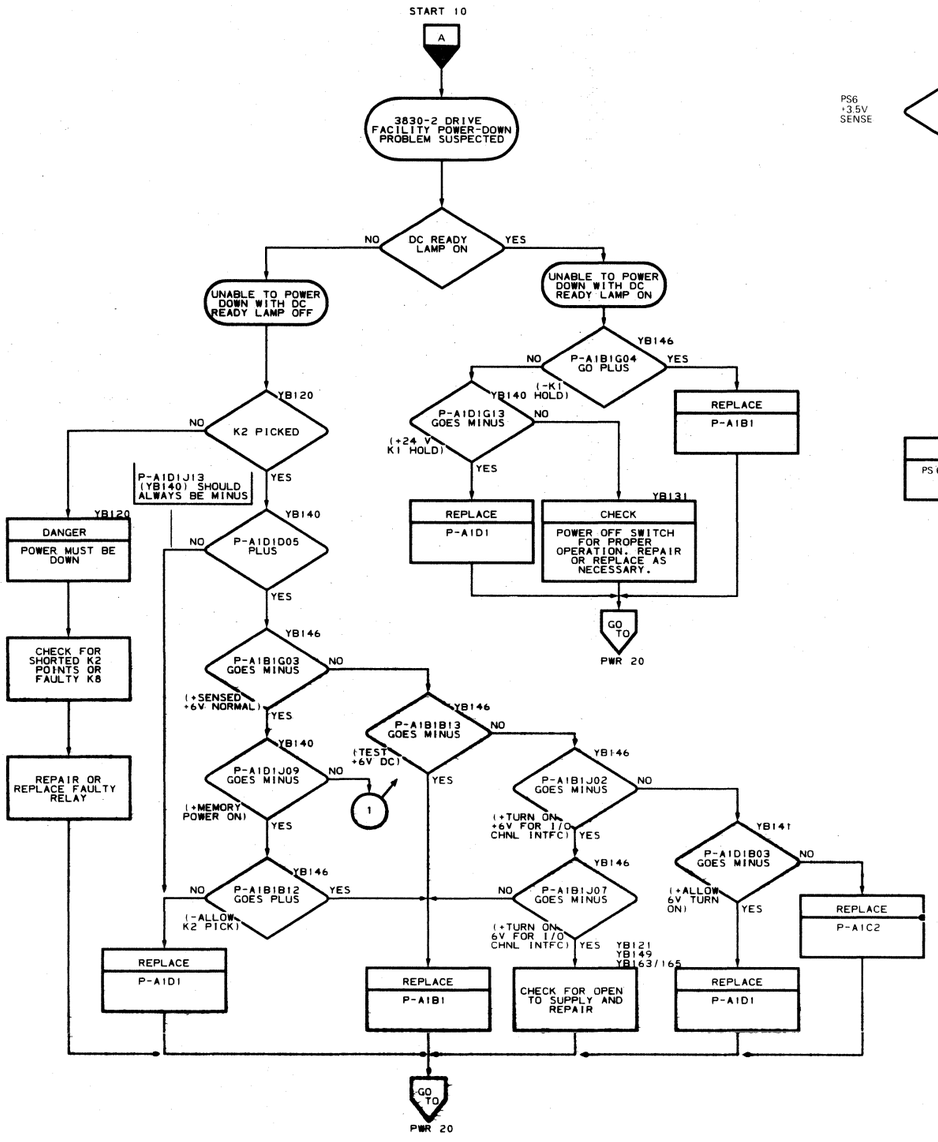


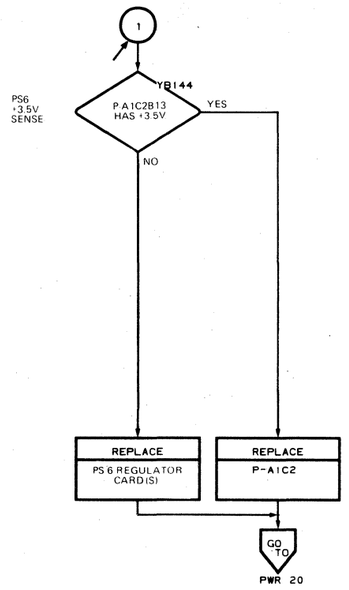
Note 1: Logic Levels:
For power sequence logic (P-A1 board YB pages) a Plus (+) levels equals +2 to +12V DC. A minus level equals ground to +0.29V DC. Any exceptions to this will be indicated in the flowchart decision block.

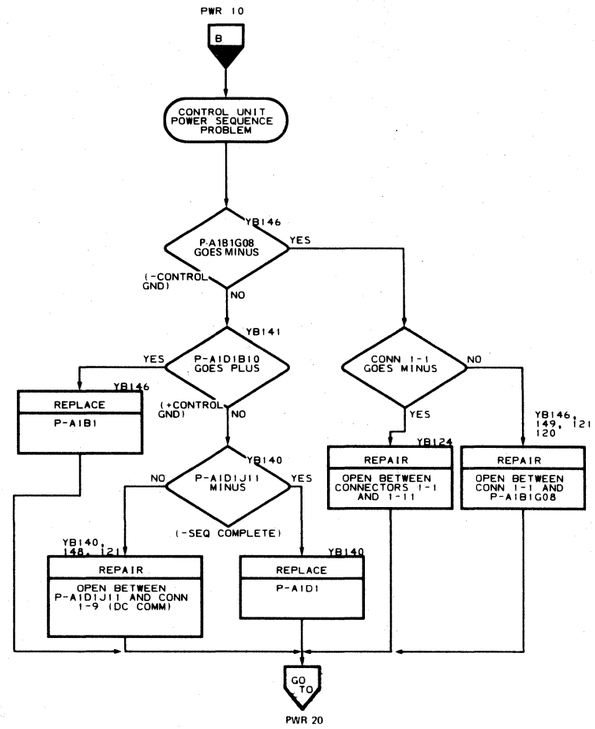
POWER SEQUENCE PROBLEM (PART 6 OF 7)

DANGER
LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE PWR 105 FOR COMPONENT AND TERMINAL LOCATIONS.
- PARENTHETICAL INFORMATION BENEATH DECISION BLOCK IS LINE NAME.







Note 1: *Logic Levels*
For power sequence logic (P-A1 Board YB pages) a plus (+) levels equals +2 to +12V dc. A minus level equals ground to +0.29V dc. Any exceptions to this will be indicated in the flowchart decision block.

POWER SEQUENCE PROBLEM (PART 7 OF 7)

PWR 10
A

3830 DC Ready light on but all controllers not powered up

1. Power off 3830.
2. Check that all EPO cables from 3830 to devices are installed properly (see diagram this page), and device Local/Remote power switch is in Remote position, and no CBs are tripped.
3. Power-on 3830.
   If same symptoms occur (3830 DC Ready on but not all controllers powered up), continue.

Any controller powered up — Yes / No

Check input voltages to sequential start card. Measure from indicated pin to S1-15 (DC Common). If two sequential start cards are installed, make checks on the left-hand card. Make checks in order shown. If voltage is not at indicated level, isolate and repair using logic on YB135.

Terminal	Voltage	Failure
S1-16	+24V	No EPO voltage from TAB 8, or open DC common line to S1-15
S1-13	+24V	No +24V from TAB 10
S1-14	+12V	No logic voltage from TAB 19
S1-17	+3V	No sequential start signal

If above voltages correct, check sequential start card voltages to/from first controller (controller connected to PC5):

S1-1	+24V	No source voltage from controller, or open common ground between 3830 and controller
S1-2	+24V	Sequential start card (K31)
S1-5	+24V	Sequential start card (K32)
S1-3	+24V	Sequential start card (no +24V to controller
S1-6	+24V	Sequential start card (K21 or logic)
S1-4	+24V	Device (Powering Complete not received)

Controller connected to PC5 powered up — Yes / No

If two sequential start cards installed, make this check on left-hand card

Seq start card terminal S1-4 at +24V — No / Yes

Controller problem. Controller is sending Powering Complete before it is powered up.

Go To Device MLM

Replace sequential start card

Go To PWR 20

Controller connected to PC6 powered up — No / Yes

Controller connected to PC7 powered up — No / Yes

Check for +24V from the following pins to S1-15 (DC Common) on the sequential start card.
If two sequential start cards are installed, make checks on left-hand card. Make checks in order shown. If pin not at +24V, isolate and repair using logic on YB135.

Terminal	Failure
S1-4	Controller connected to PC5 not returning Powering Complete
S1-7	Controller connected to PC6 not supplying +24V source voltage to 3830
S1-8	Sequential start card (K31)
S1-11	Sequential start card (K32)
S1-9	Sequential start card (no +24V to controller)
S1-12	Sequential start card (K22 or logic)
S1-10	Controller problem (Powering Complete not received)

Go To PWR 20

Check input voltages to sequential start card no. 2 (right-hand card). Measure from indicated pin to S1-15 (DC Common). Make checks in order shown. If voltage is not at indicated level, isolate and repair using logic on YB135.

Terminal	Voltage	Failure
S1-16	+24V	No EPO voltage from sequential start card no. 1 (conn S2-6), or no DC Common line to S1-15 from sequential start card no. 1 (conn S2-3)
S1-13	+24V	No 24V from sequential start no. 1 (conn S2-1)
S1-14	+12V	No logic voltage from sequential start card no. 1 (conn S2-2)
S1-17	+3V	No sequential start signal to card no. 2 from card no. 1 (conn S2-8)

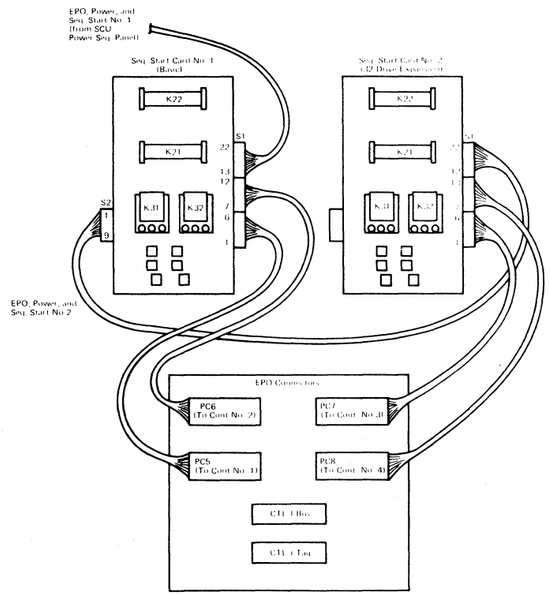
If above voltages correct, check sequential start card voltages to/from third controller (controller connected to PC7):

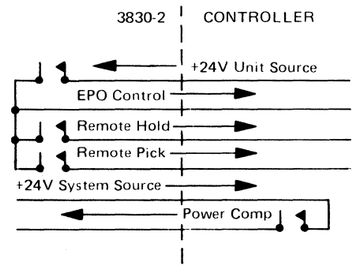
S1-1	+24V	No source voltage from controller or open common ground between 3830 and controller
S1-2	+24V	Sequential start card (K31)
S1-5	+24V	Sequential start card (K32)
S1-3	+24V	Sequential start card (no +24V to controller)
S1-6	+24V	Sequential start card (K21 or logic)
S1-4	+24V	Device (Powering Complete not received)

Go To PWR 20

Check for +24V from the following pins to S1-15 (DC Common) on sequential start card No. 2 (right-hand card). Make checks in order shown. If pin not at +24V, isolate and repair using logic on YB135.

Terminal	Failure
S1-4	Controller connected to PC7 not returning Powering Complete
S1-7	Controller connected to PC8 not supplying +24V source voltage to 3830
S1-8	Sequential start card (K31)
S1-11	Sequential start card (K32)
S1-9	Sequential start card (No +24V to controller)
S1-12	Sequential start card (K22 or logic)
S1-10	Controller problem (Powering Complete not received)

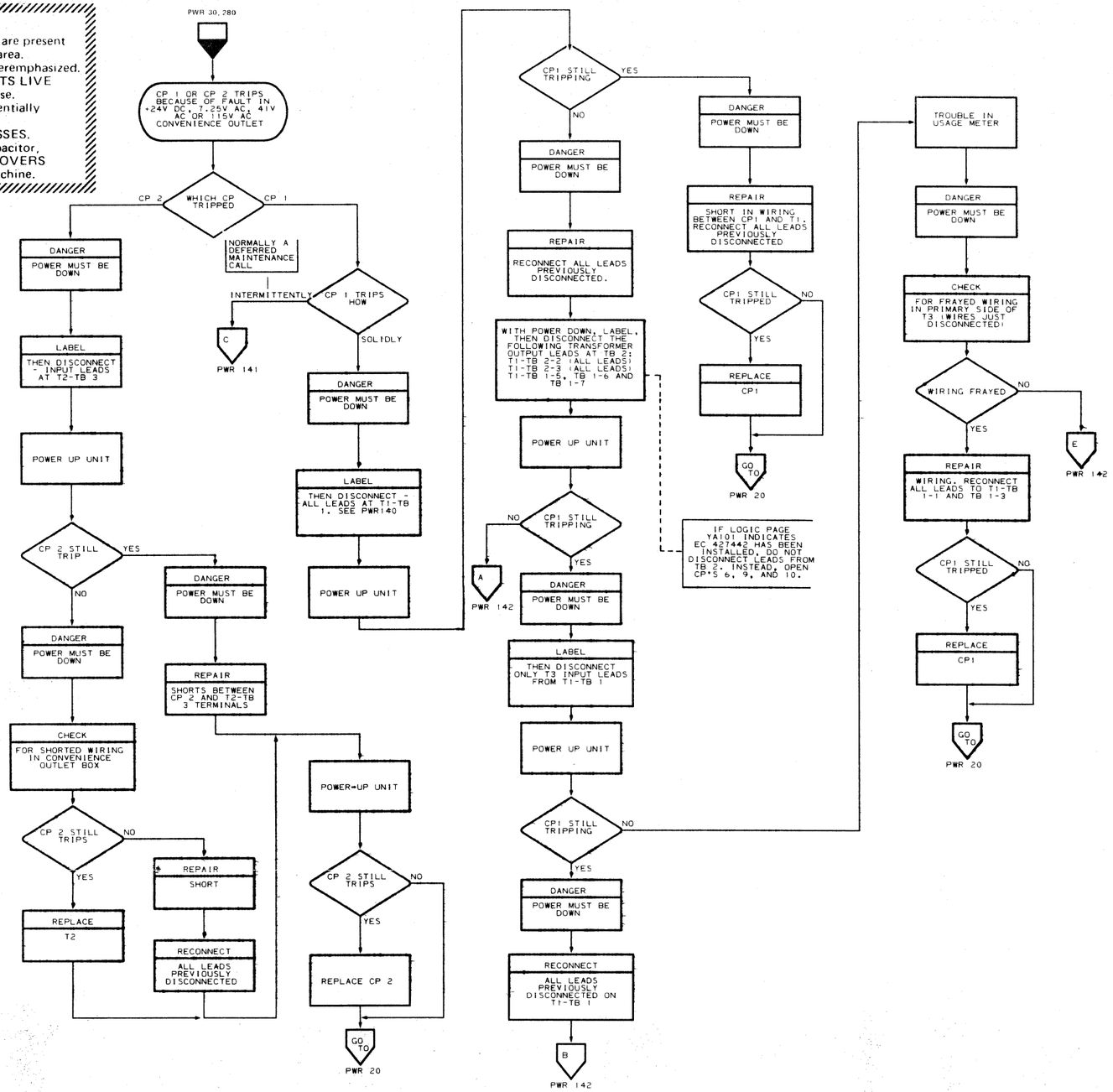




CP1 OR CP2 TRIPS (PART 1 OF 4)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

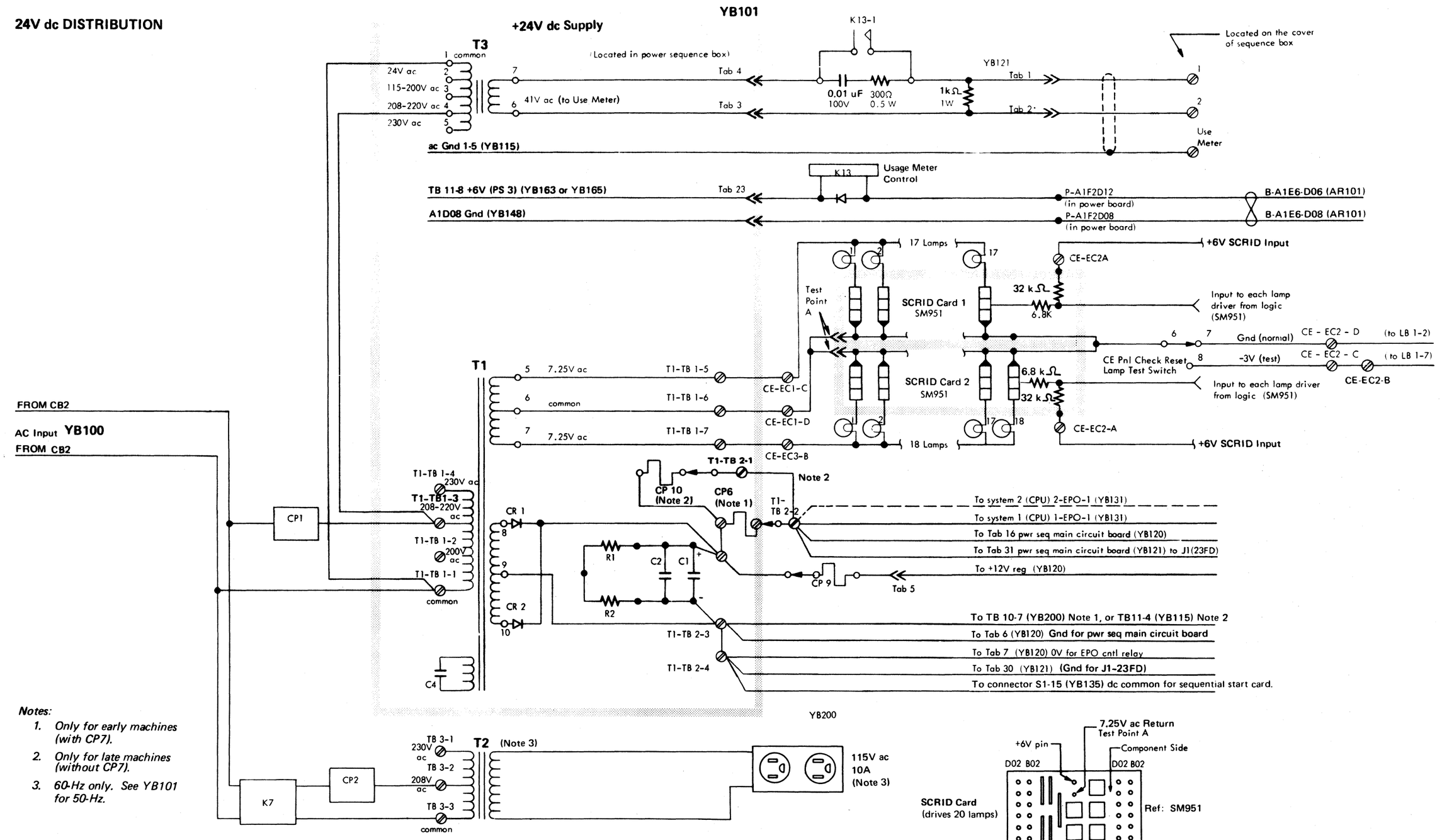
● SEE PWR 140 FOR VOLTAGE DISTRIBUTION



3830-2	BR2000	2347174	437402A	437403	437405	437414	437415		
	Seq 2 of 2	Part Number	15 Mar 72	21 Apr 72	15 Aug 72	4 Jun 73	2 Nov 73		

CP1 OR CP2 TRIPS (Part 2 of 4)

24V dc DISTRIBUTION



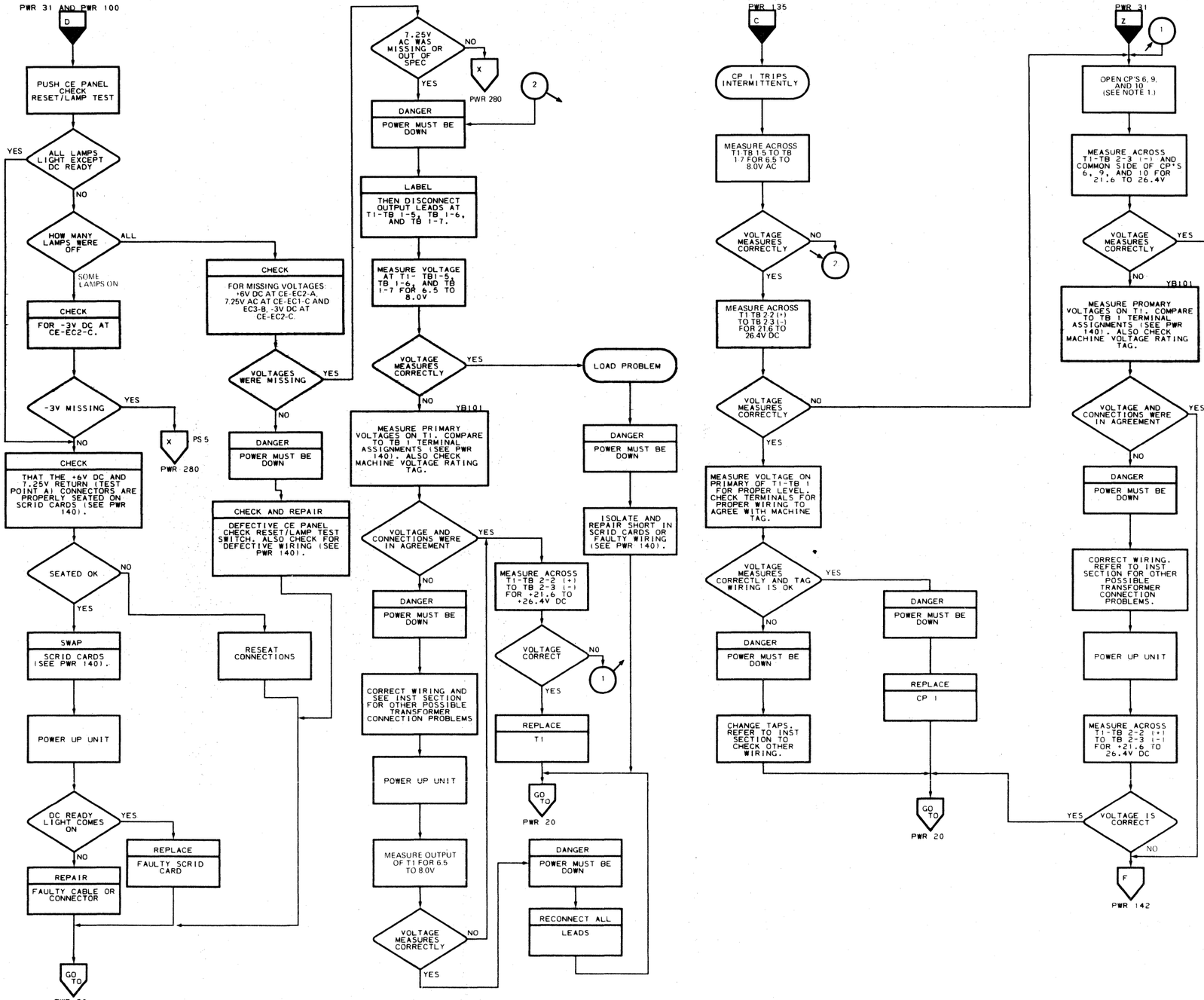
Notes:

1. *Only for early machines (with CP7).*
2. *Only for late machines (without CP7).*
3. *60-Hz only. See YB101 for 50-Hz.*

CP1 OR CP2 TRIPS (PART 3 OF 4)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

• SEE PWR 140 FOR VOLTAGE DISTRIBUTION.



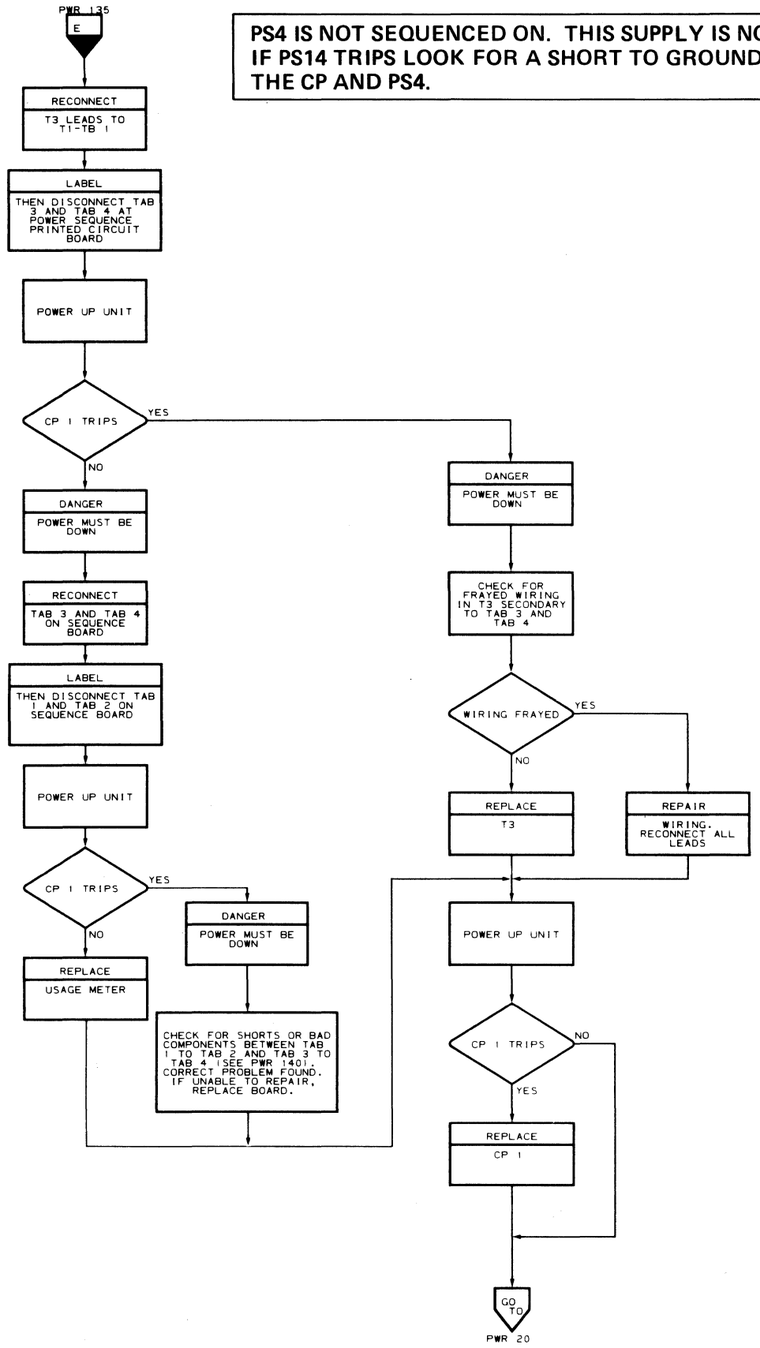
Note 1: CP6 used in early machines.
CP10 used in late machines.

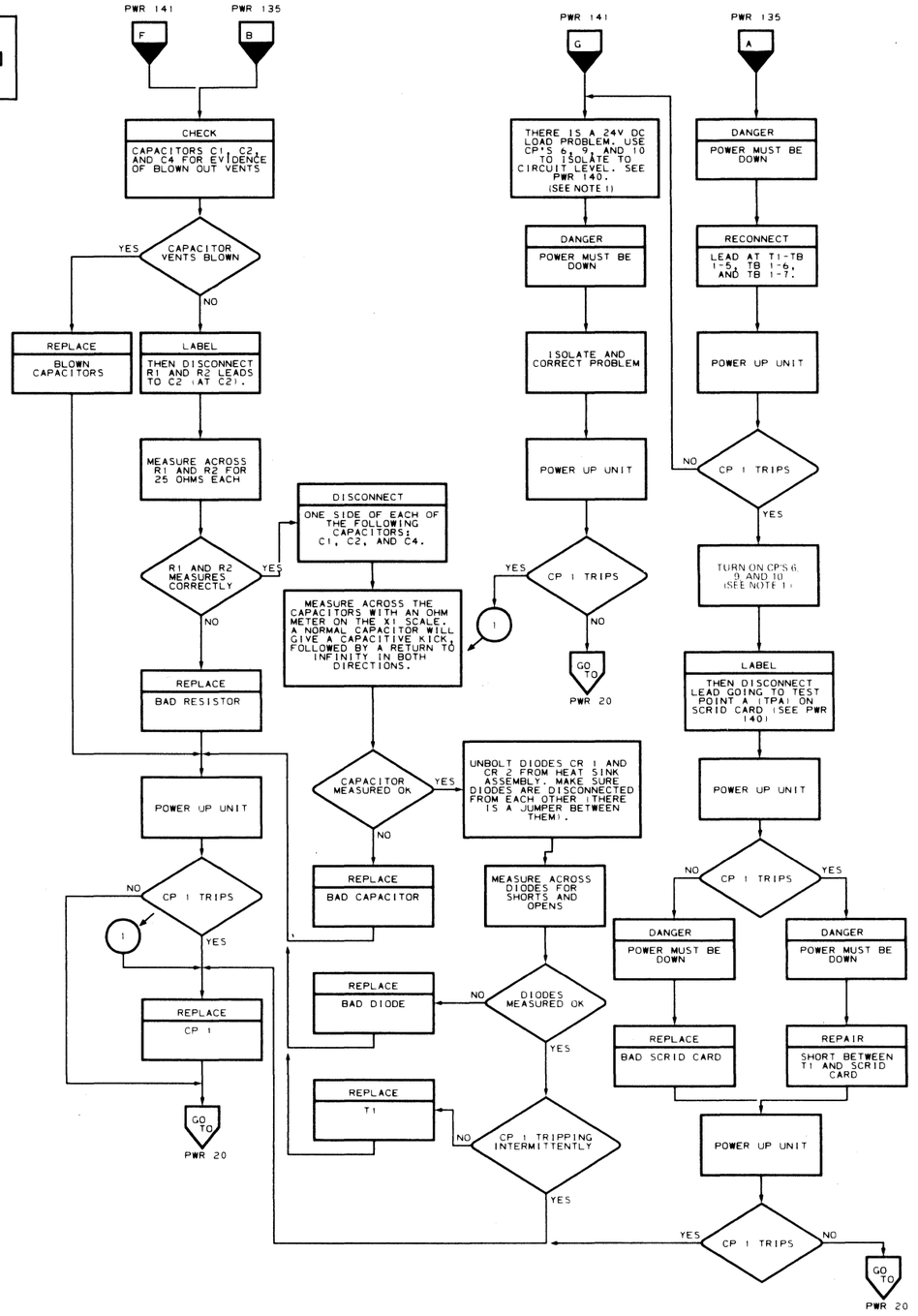
CP1 OR CP2 TRIPS (PART 4 OF 4)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

• SEE PWR 140 FOR VOLTAGE DISTRIBUTION.

PS4 IS NOT SEQUENCED ON. THIS SUPPLY IS NOT USED. IF PS14 TRIPS LOOK FOR A SHORT TO GROUND BETWEEN THE CP AND PS4.

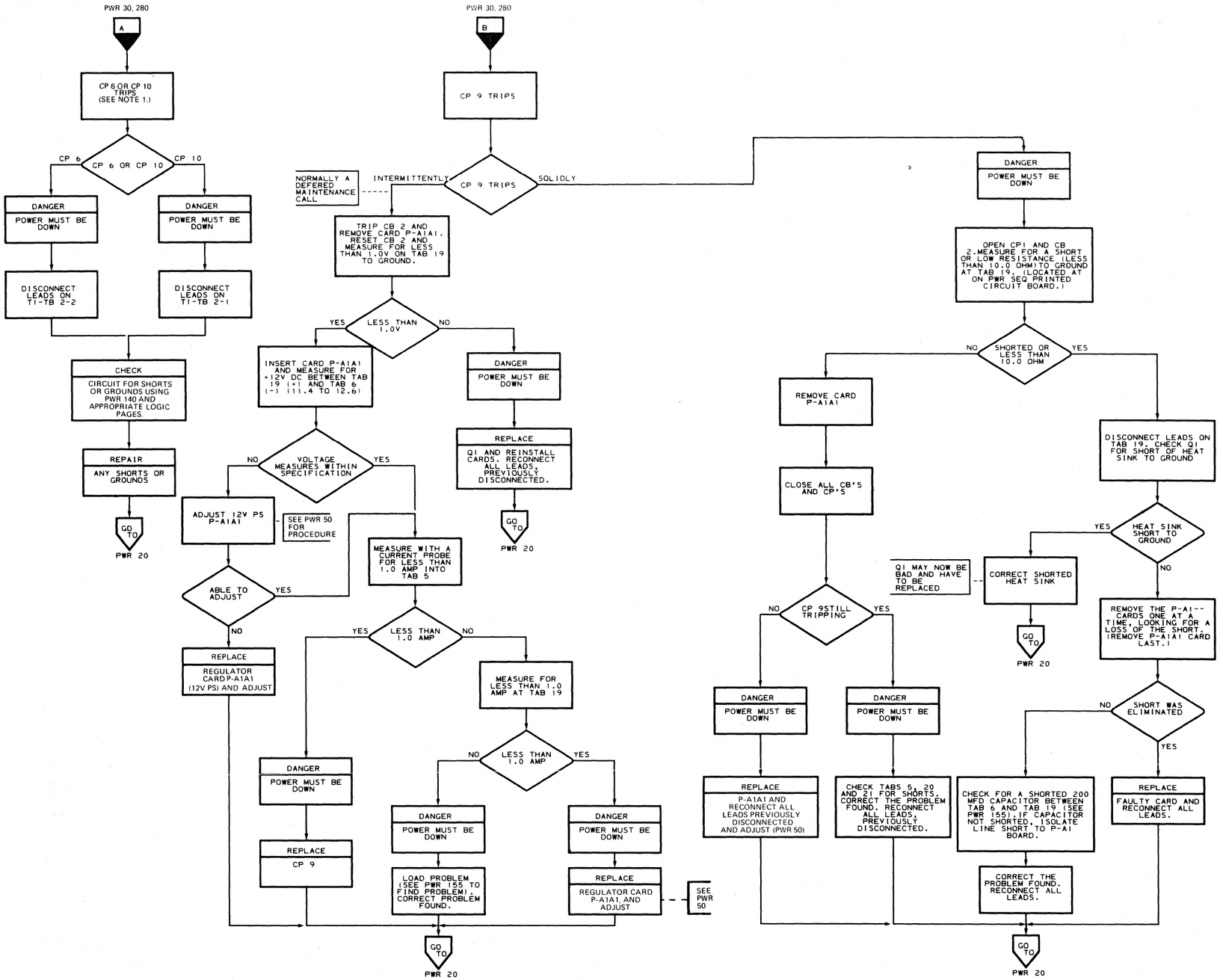




Note 1: CP6 used in early machines.
CP10 used in late machines.

CP6, 9, OR 10 TRIPS (PART 1 OF 2)

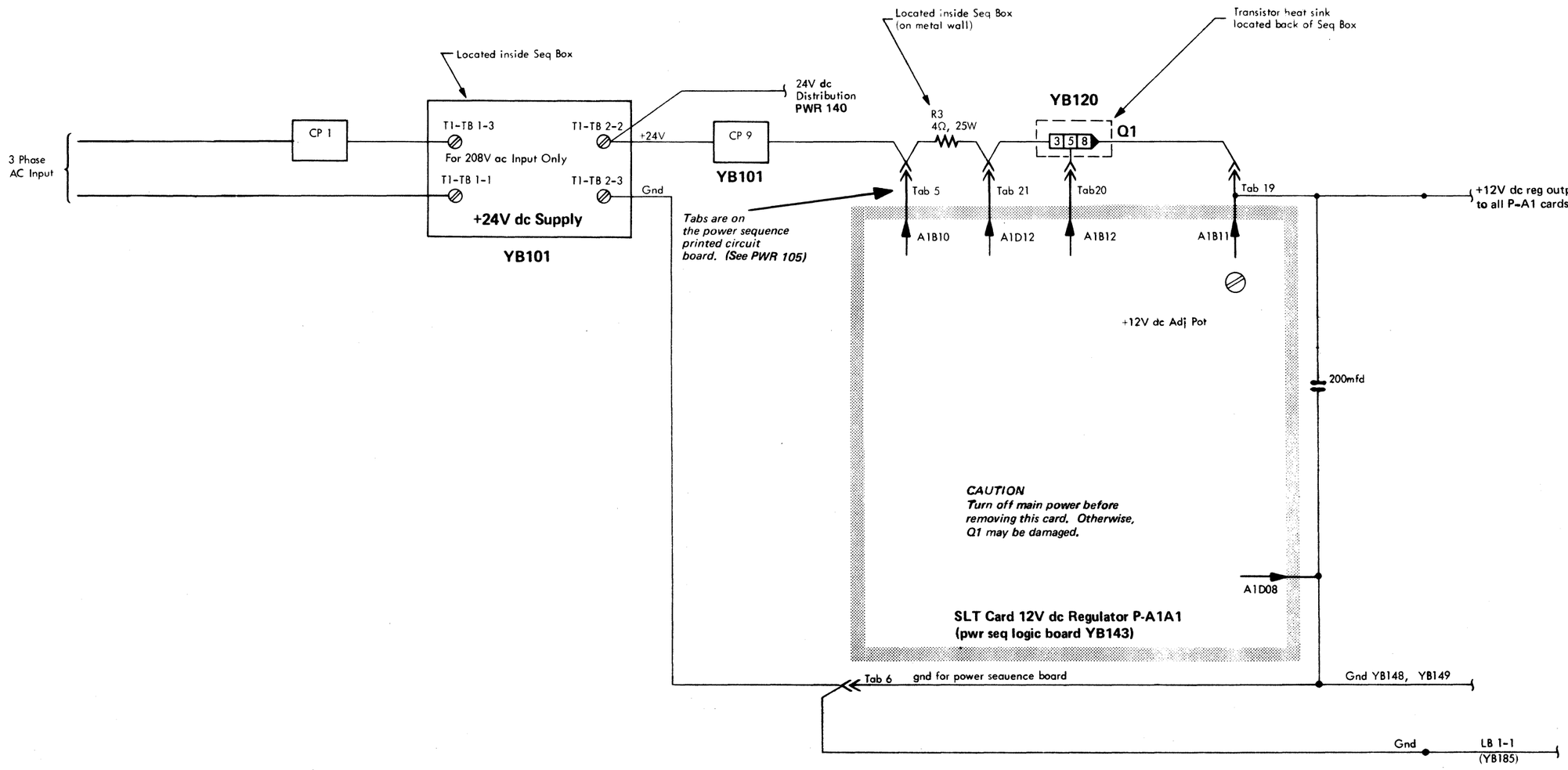
DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.



Note 1: CP6 used in early machines.
CP10 used in late machines.

CP9 TRIPS (Part 2 of 2)

12V dc REGULATOR

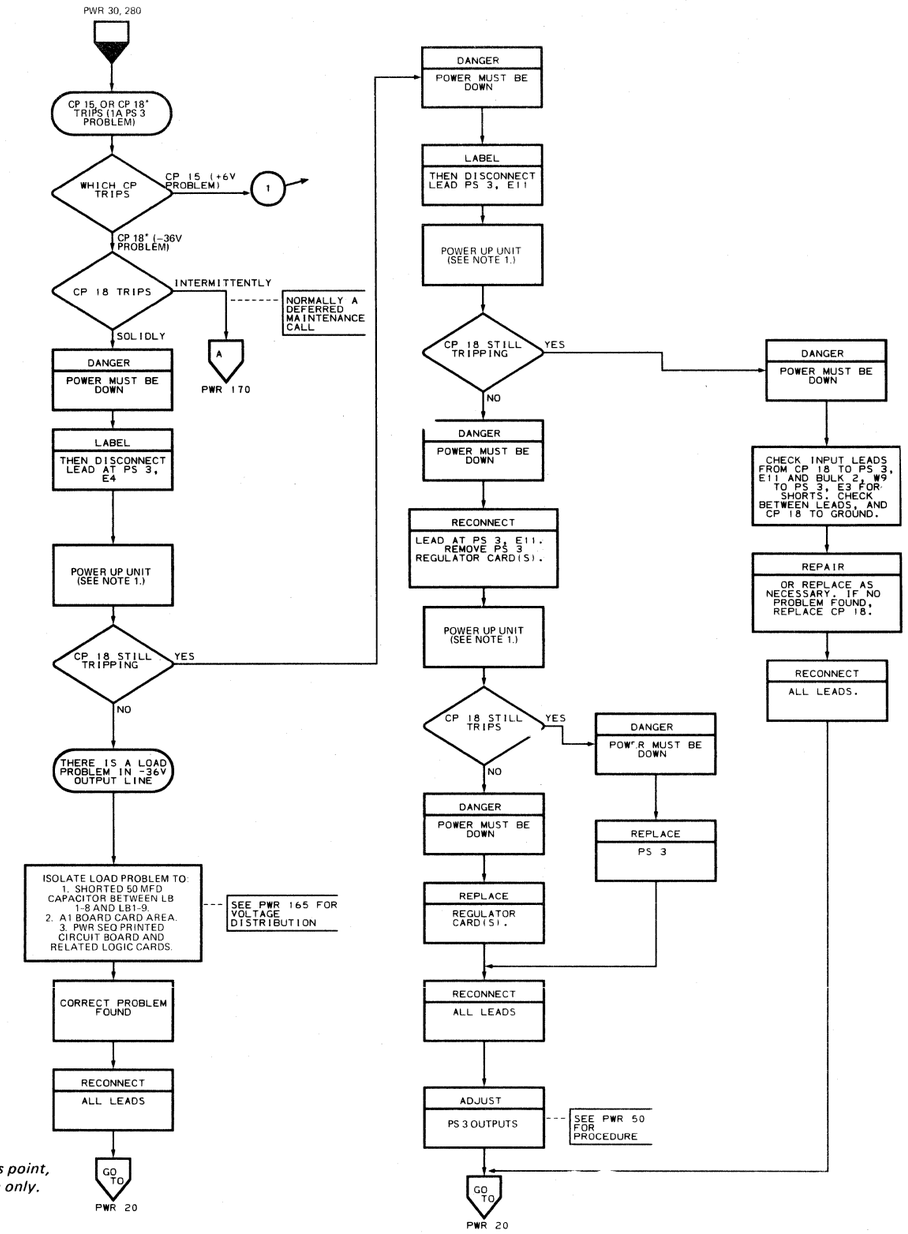


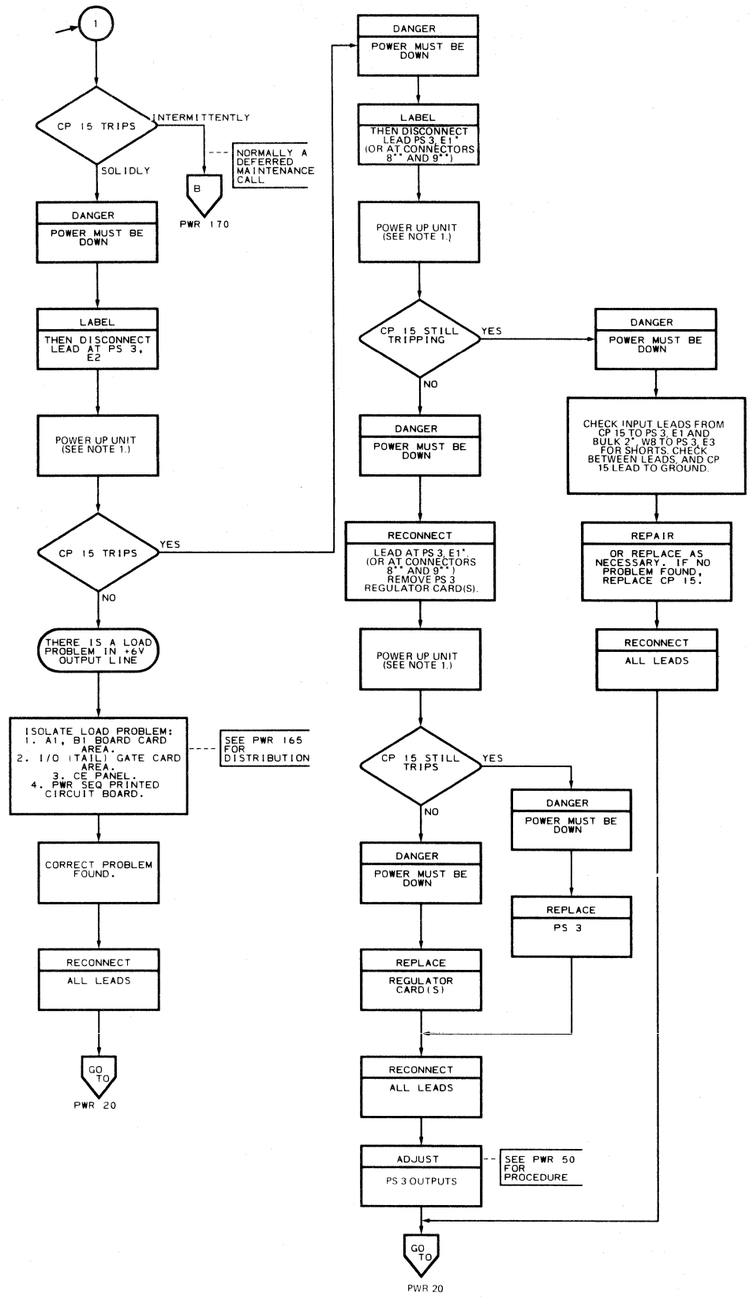
CP15/18 TRIPS (PART 1 OF 3)

SOLID TRIP

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

• SEE PWR 165 FOR VOLTAGE DISTRIBUTION.





Note 1: The unit will not power up normally at this point, but you are looking for a CP trip condition only.

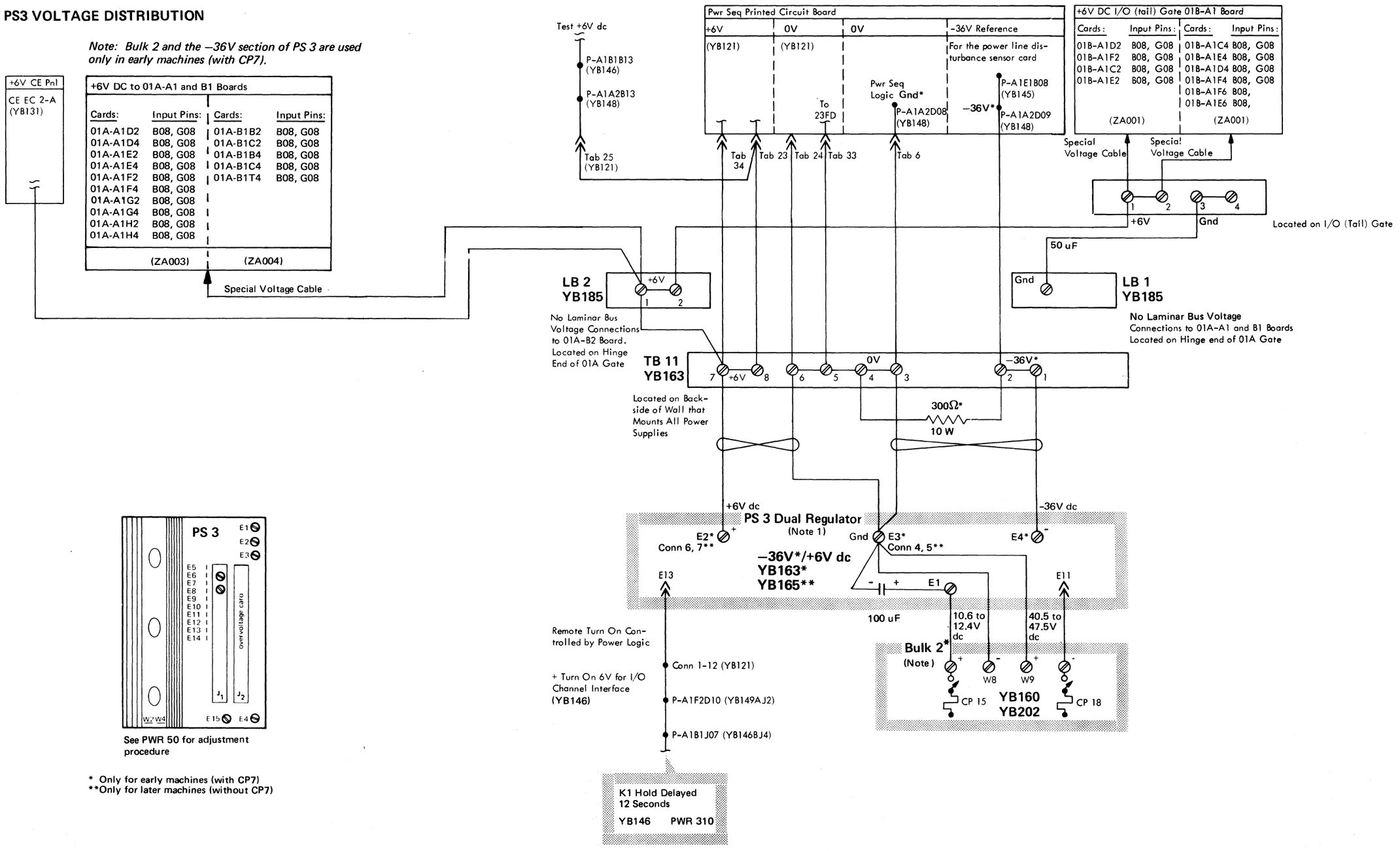
**Only for early machines (with CP7).*

***Only for late machines (without CP7).*

CP15/18 TRIPS (Part 2 of 3)

PS3 VOLTAGE DISTRIBUTION

Note: Bulk 2 and the –36V section of PS 3 are used only in early machines (with CP7).



See PWR 50 for adjustment procedure

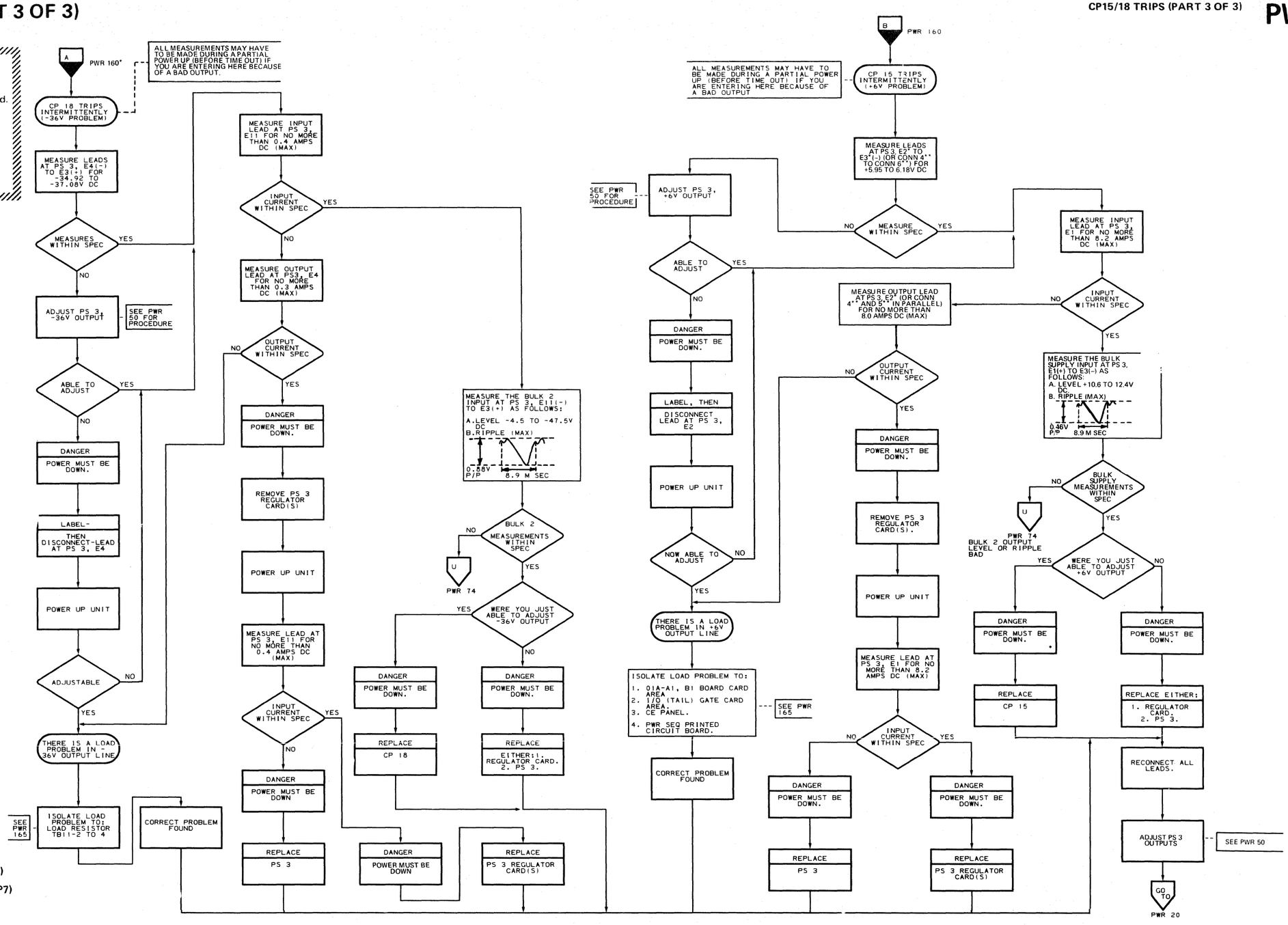
* Only for early machines (with CP7)
**Only for later machines (without CP7)

CP15/18 TRIPS (PART 3 OF 3)

INTERMITTENT TRIP

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

• SEE PWR 165 FOR VOLTAGE DISTRIBUTION.



* Only for early machines (with CP7)

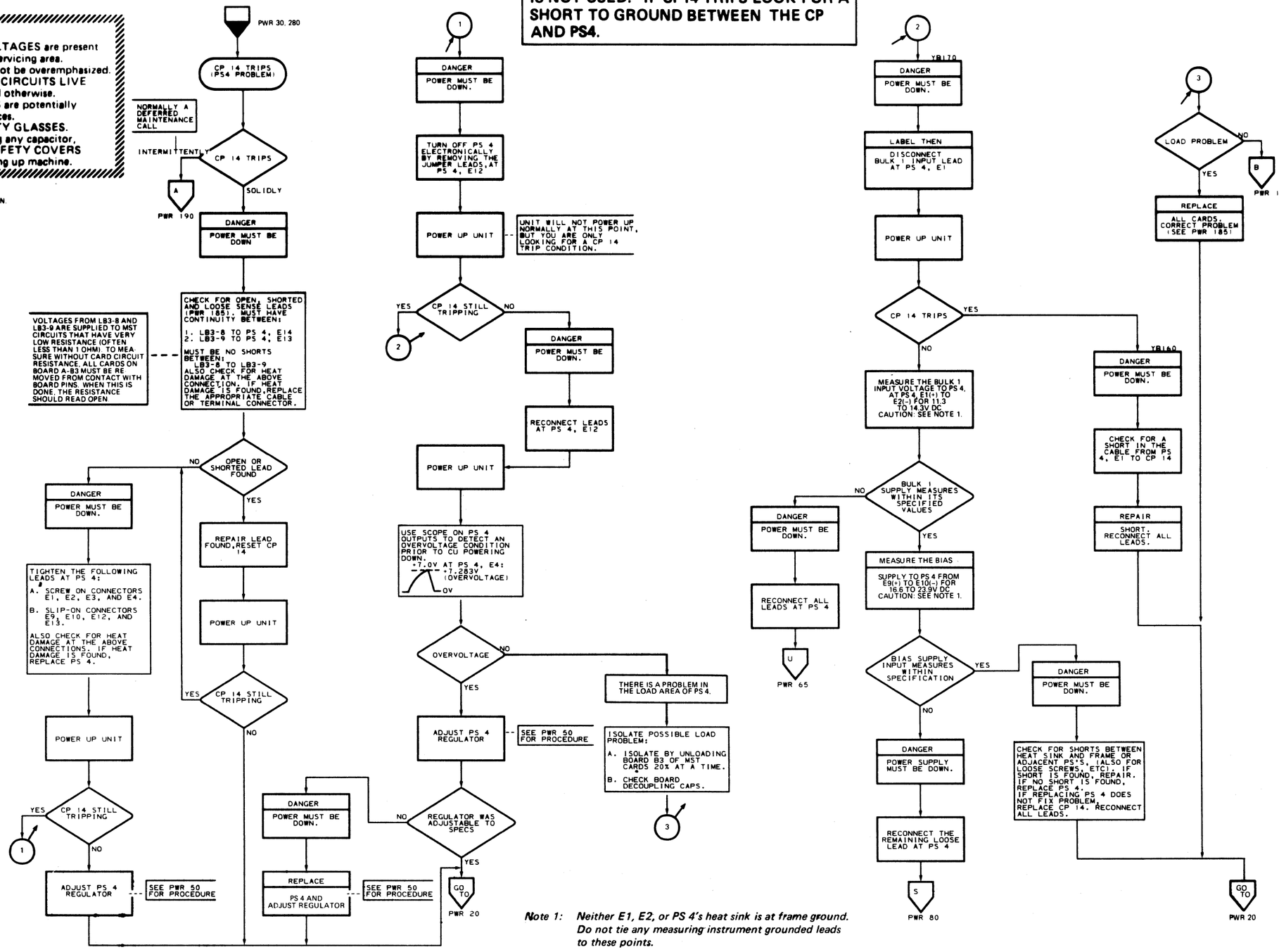
** Only for late machines (without CP7)

CP 14 TRIPS (Part 1 of 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

• SEE PWR 186 FOR VOLTAGE DISTRIBUTION.

PS4 IS NOT SEQUENCED ON. THIS SUPPLY IS NOT USED. IF CP14 TRIPS LOOK FOR A SHORT TO GROUND BETWEEN THE CP AND PS4.

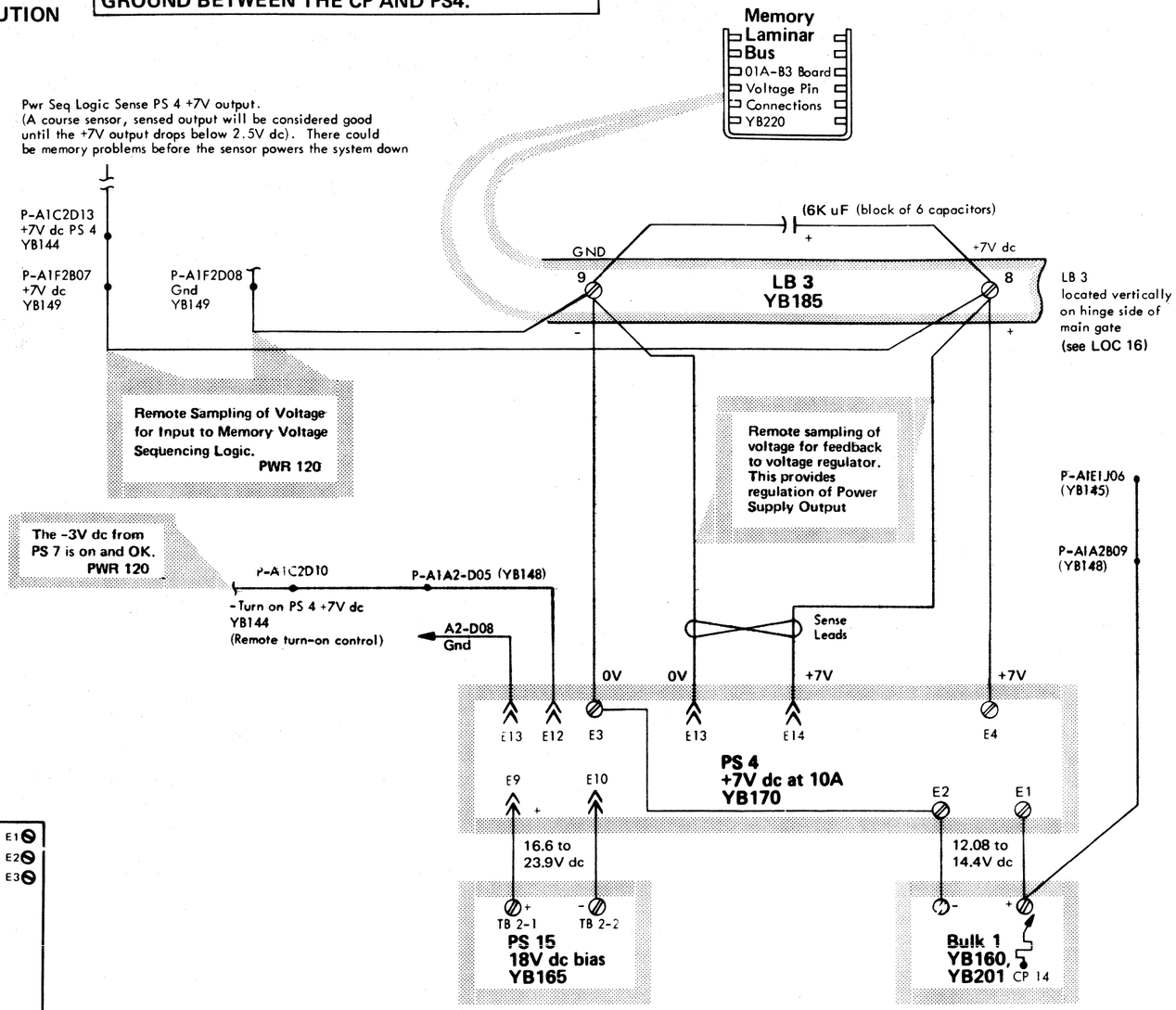


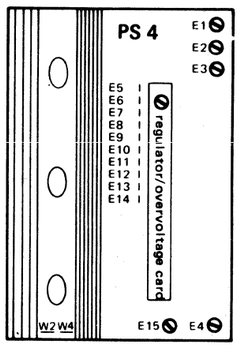
Note 1: Neither E1, E2, or PS 4's heat sink is at frame ground. Do not tie any measuring instrument grounded leads to these points.

CP14 TRIPS (Part 2 of 3)

PS4 IS NOT SEQUENCED ON. THIS SUPPLY IS NOT USED. IF CP14 TRIPS, LOOK FOR A SHORT TO GROUND BETWEEN THE CP AND PS4.

PS4 VOLTAGE DISTRIBUTION





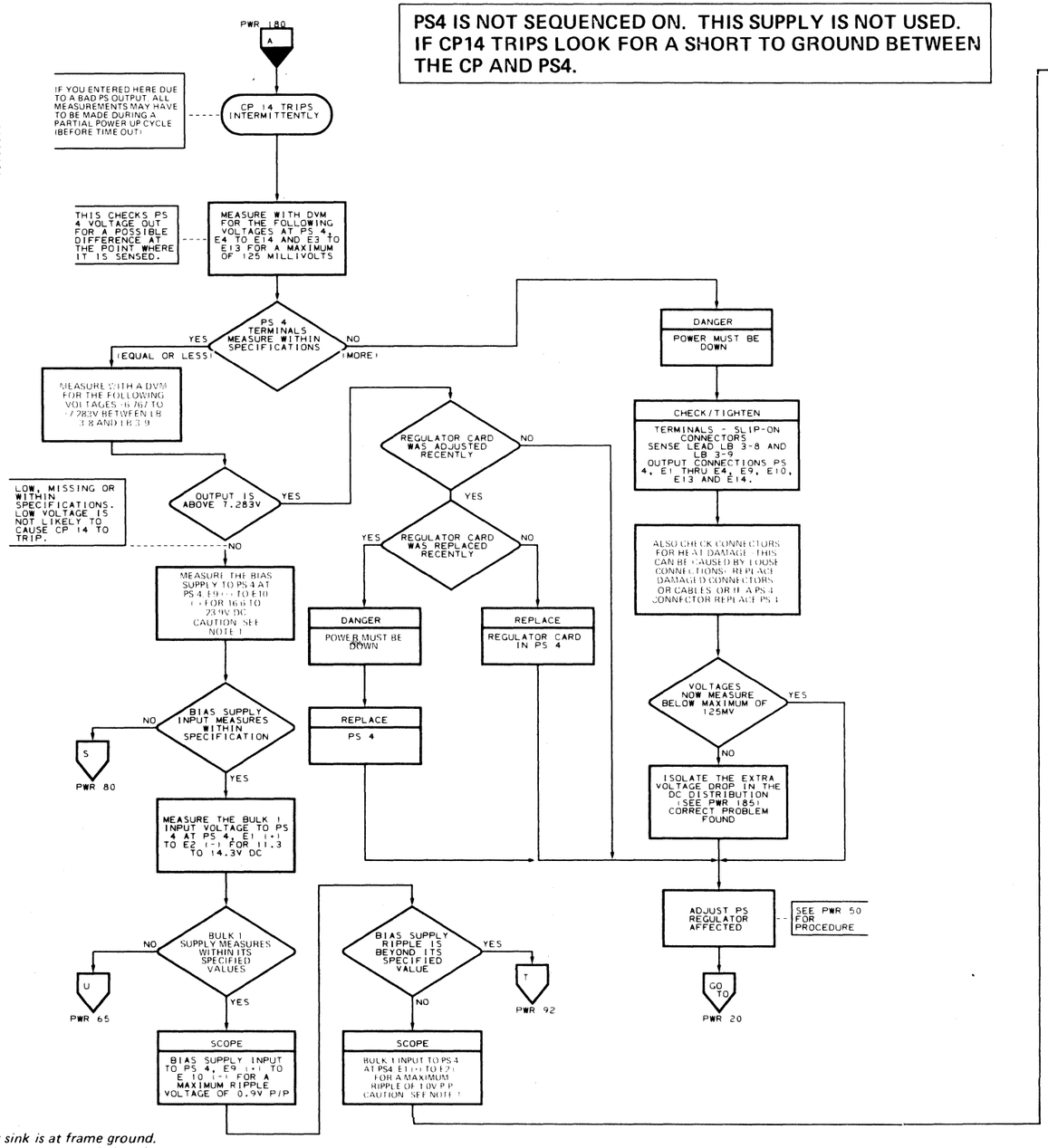
See PWR 50 for adjustment procedure.

CP 14 TRIPS (Part 3 of 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE PWR 185 FOR VOLTAGE DISTRIBUTION

PS4 IS NOT SEQUENCED ON. THIS SUPPLY IS NOT USED. IF CP14 TRIPS LOOK FOR A SHORT TO GROUND BETWEEN THE CP AND PS4.

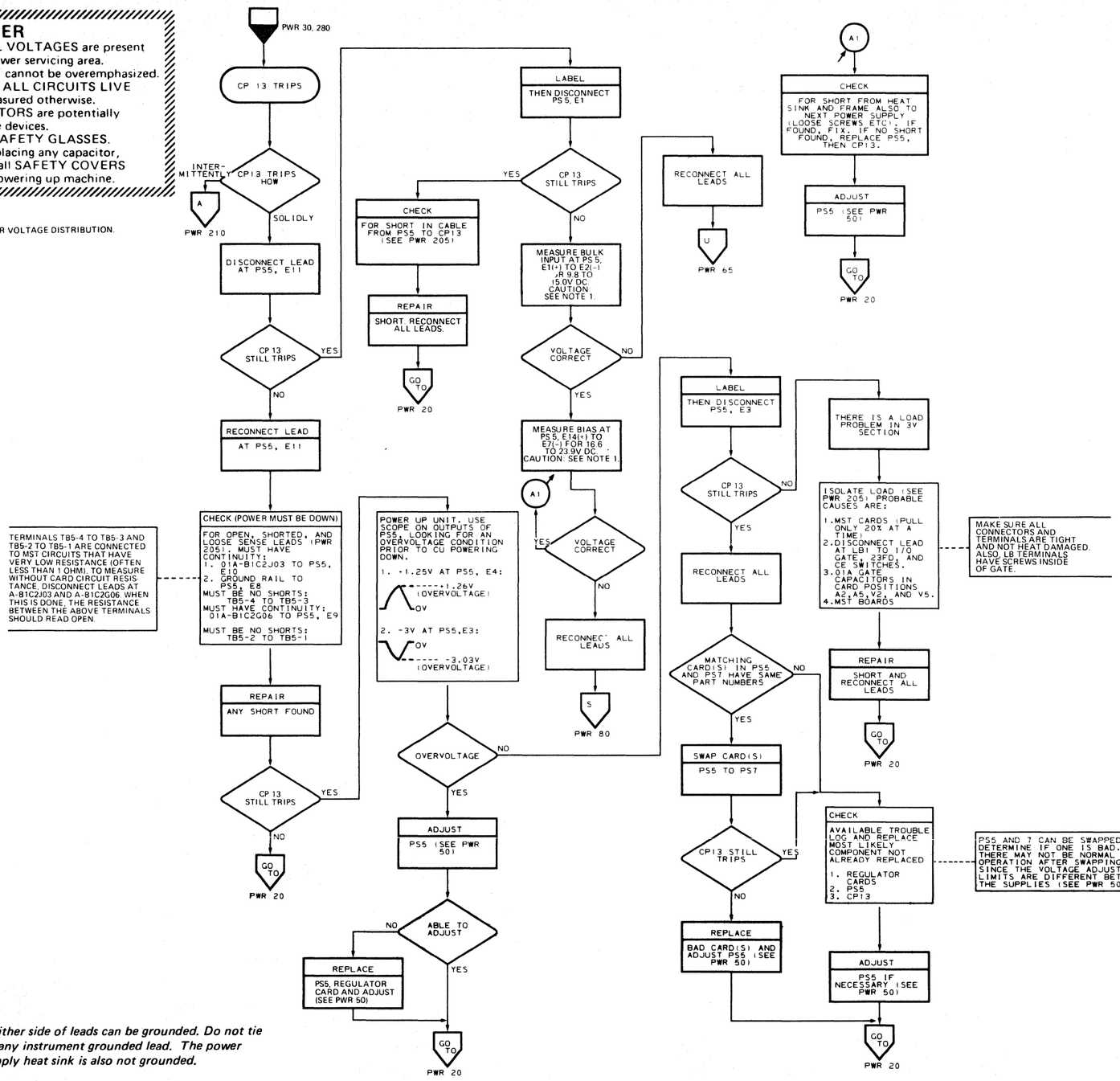


Note 1: Neither E1, E2, nor PS4 heat sink is at frame ground. Do not tie any measuring instrument grounded leads to these points.

CP13 TRIPS (PART 1 OF 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

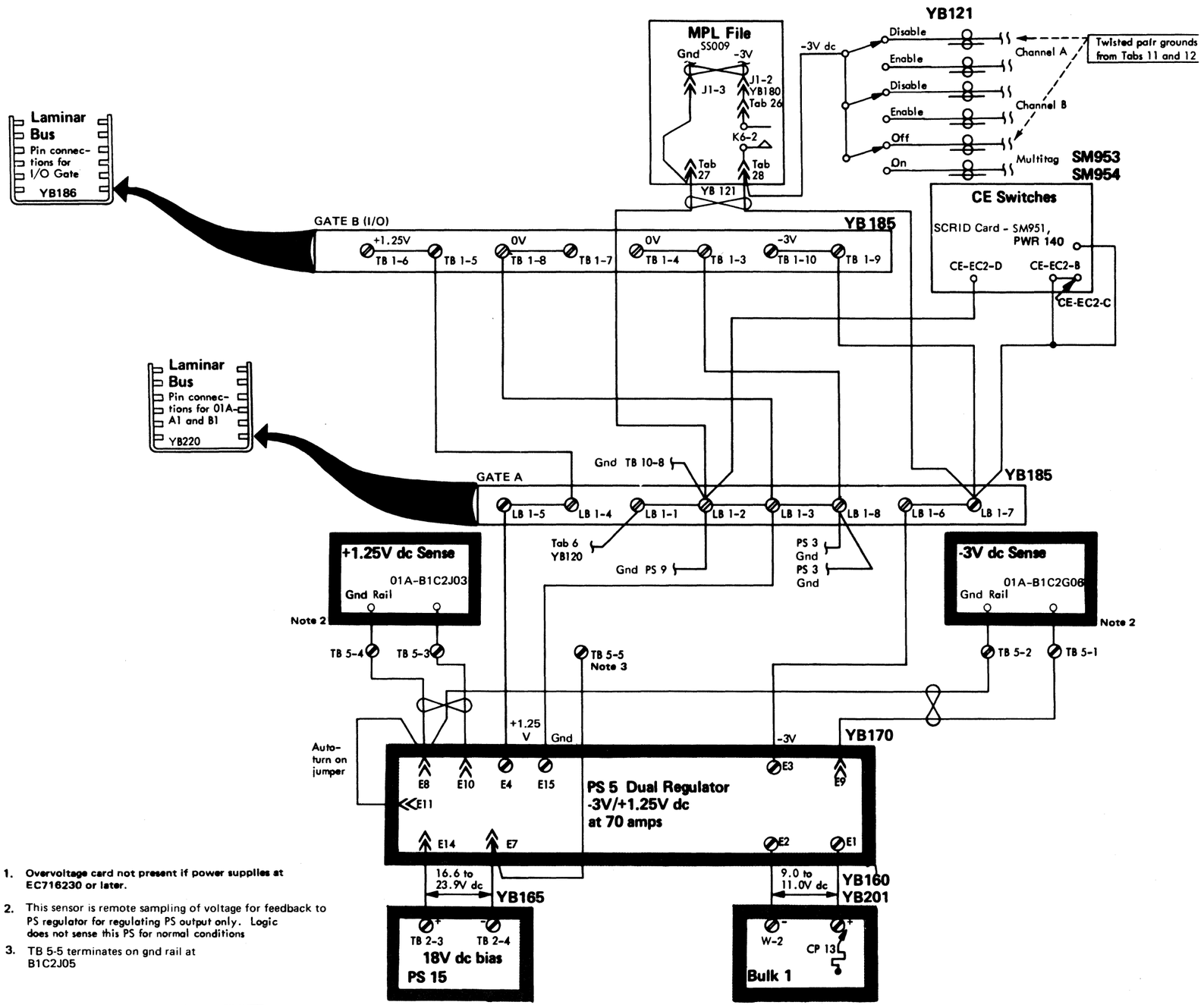
- SEE PWR 205 FOR VOLTAGE DISTRIBUTION.

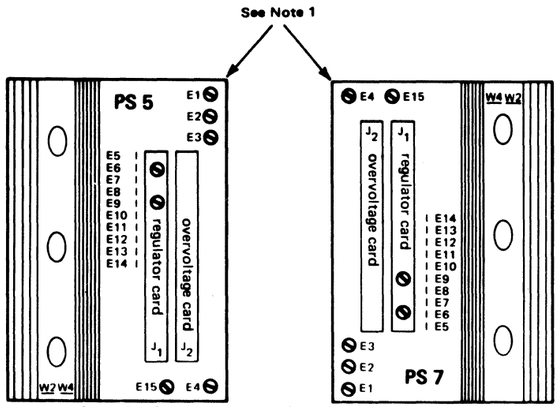


Note 1: Neither side of leads can be grounded. Do not tie to any instrument grounded lead. The power supply heat sink is also not grounded.

CP13 TRIPS (Part 2 of 3)

PS5 VOLTAGE DISTRIBUTION





Power Supplies are physically inverted on left and right sides

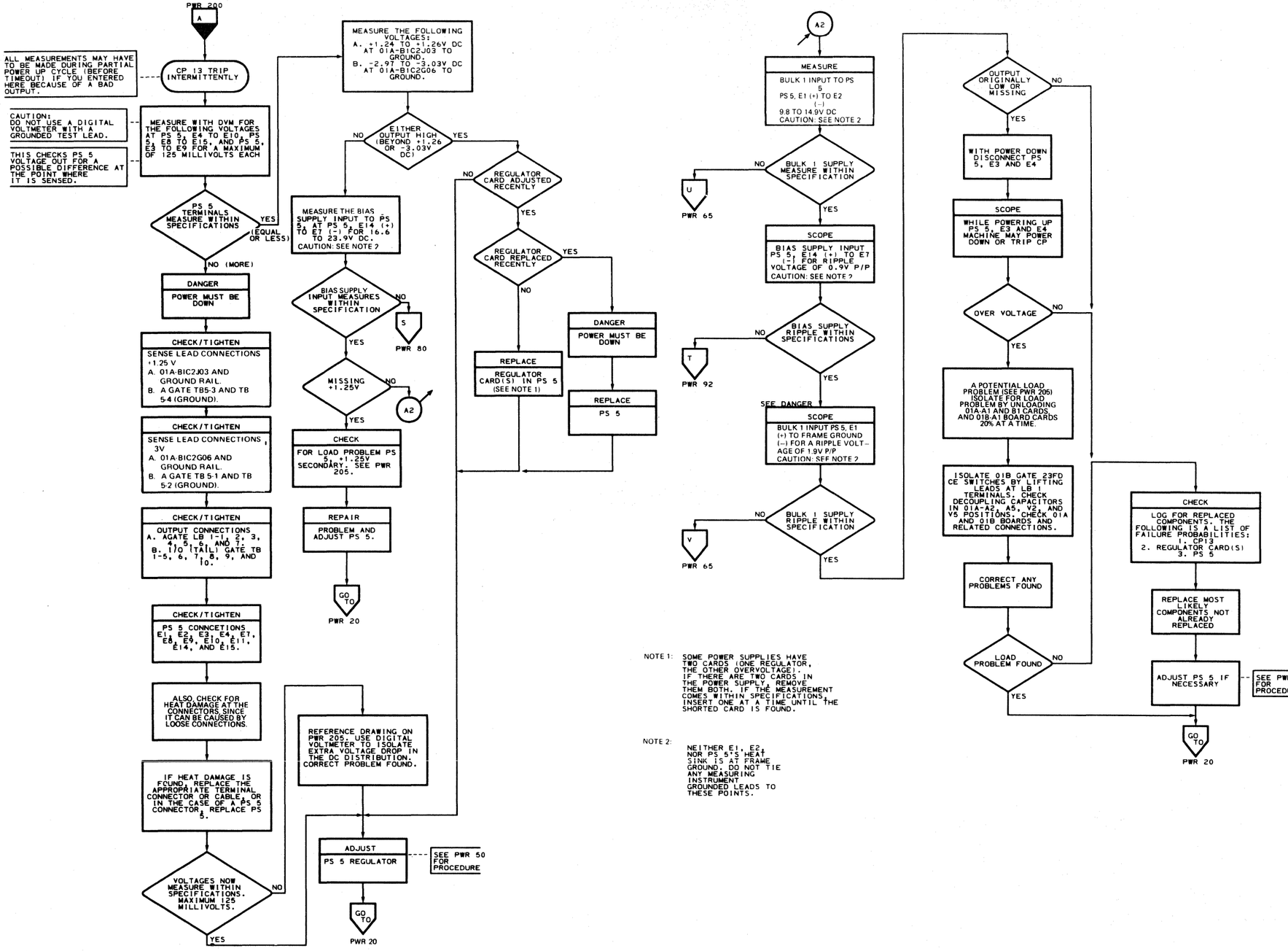
Notes:
1. Overvoltage card not present if power supplies at EC716230 or later.
2. This sensor is remote sampling of voltage for feedback to PS regulator for regulating PS output only. Logic does not sense this PS for normal conditions
3. TB 5-5 terminates on gnd rail at B1C2J05

3830-2	BR2700 Seq 1 of 2	2347181 Part No. (8)	437402A 15 Mar 72	437405 15 Aug 72	437408 16 Oct 72	437414 4 Jun 73	447461 12 Mar 76		

CP13 TRIPS (PART 3 OF 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

• SEE PWR 205 FOR VOLTAGE DISTRIBUTION



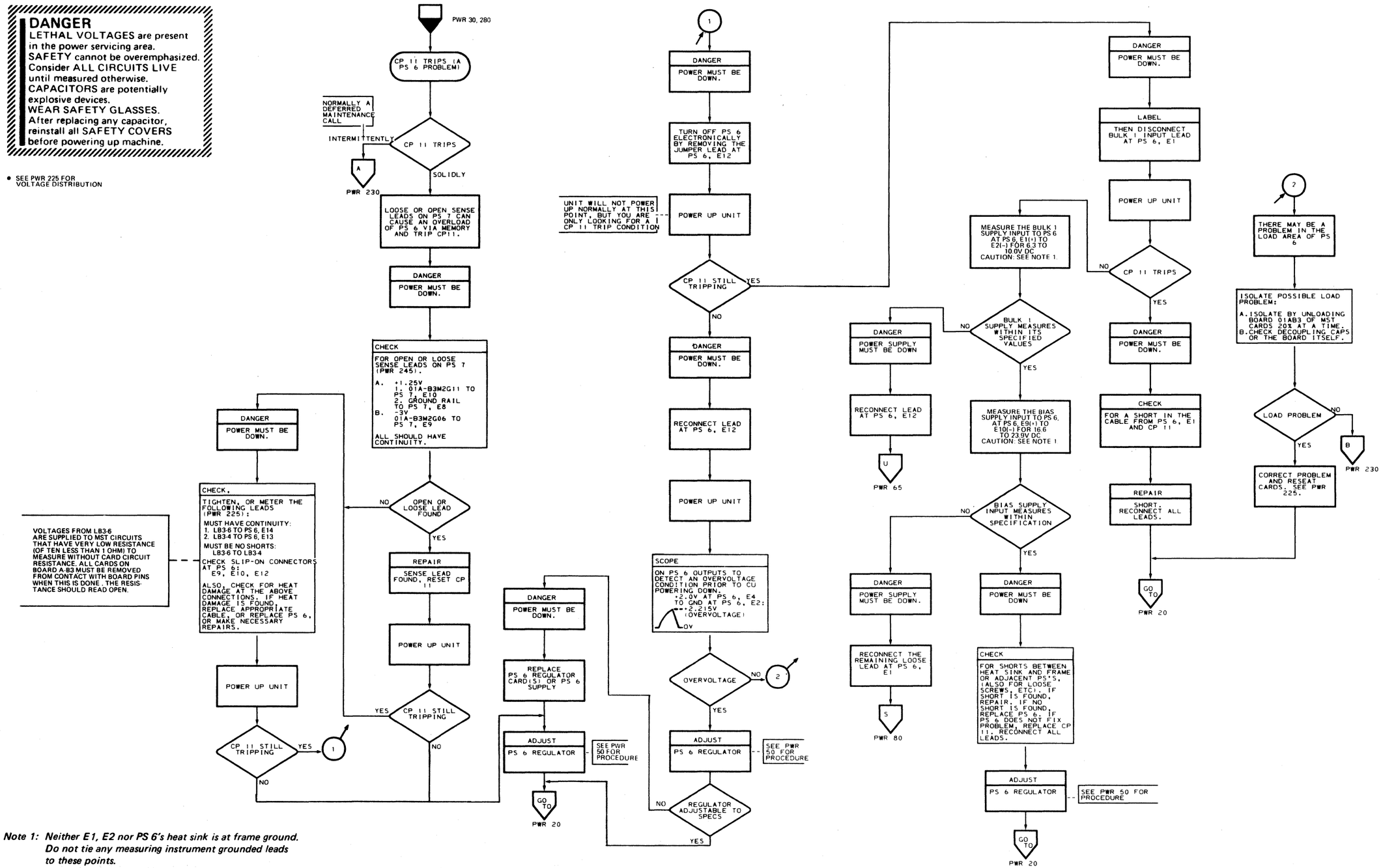
NOTE 1: SOME POWER SUPPLIES HAVE TWO CARDS (ONE REGULATOR, THE OTHER OVERVOLTAGE). IF THERE ARE TWO CARDS IN THE POWER SUPPLY REMOVE THEM BOTH. IF THE MEASUREMENT COMES WITHIN SPECIFICATIONS, INSERT ONE AT A TIME UNTIL THE SHORTED CARD IS FOUND.

NOTE 2: NEITHER E1, E2 NOR PS 5'S HEAT SINK IS AT FRAME GROUND. DO NOT TIE ANY MEASURING INSTRUMENT GROUNDED LEADS TO THESE POINTS.

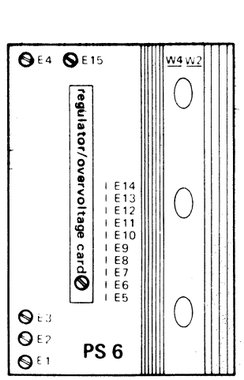
CP11 TRIPS (PART 1 OF 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

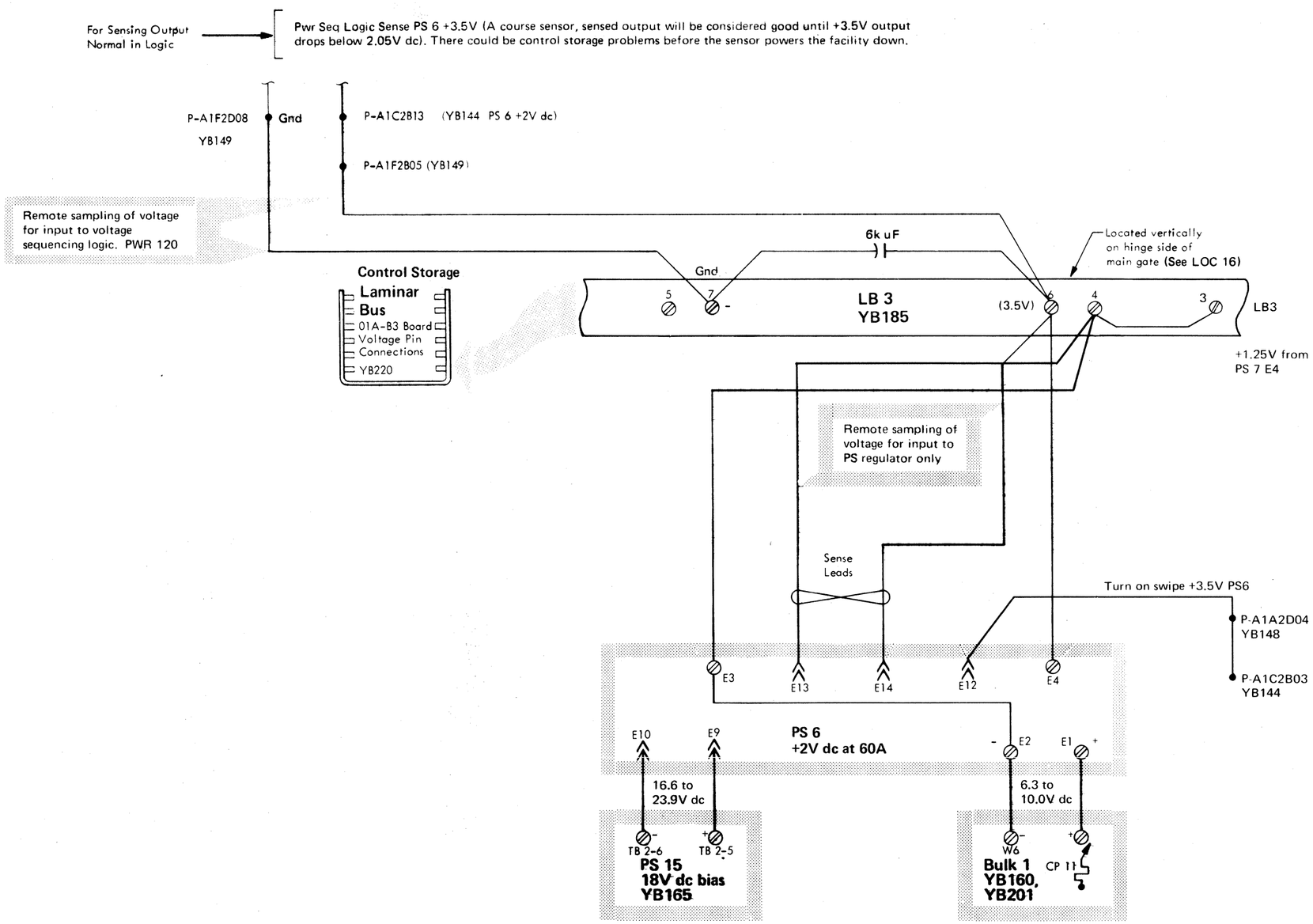
- SEE PWR 225 FOR VOLTAGE DISTRIBUTION



Note 1: Neither E1, E2 nor PS 6's heat sink is at frame ground. Do not tie any measuring instrument grounded leads to these points.



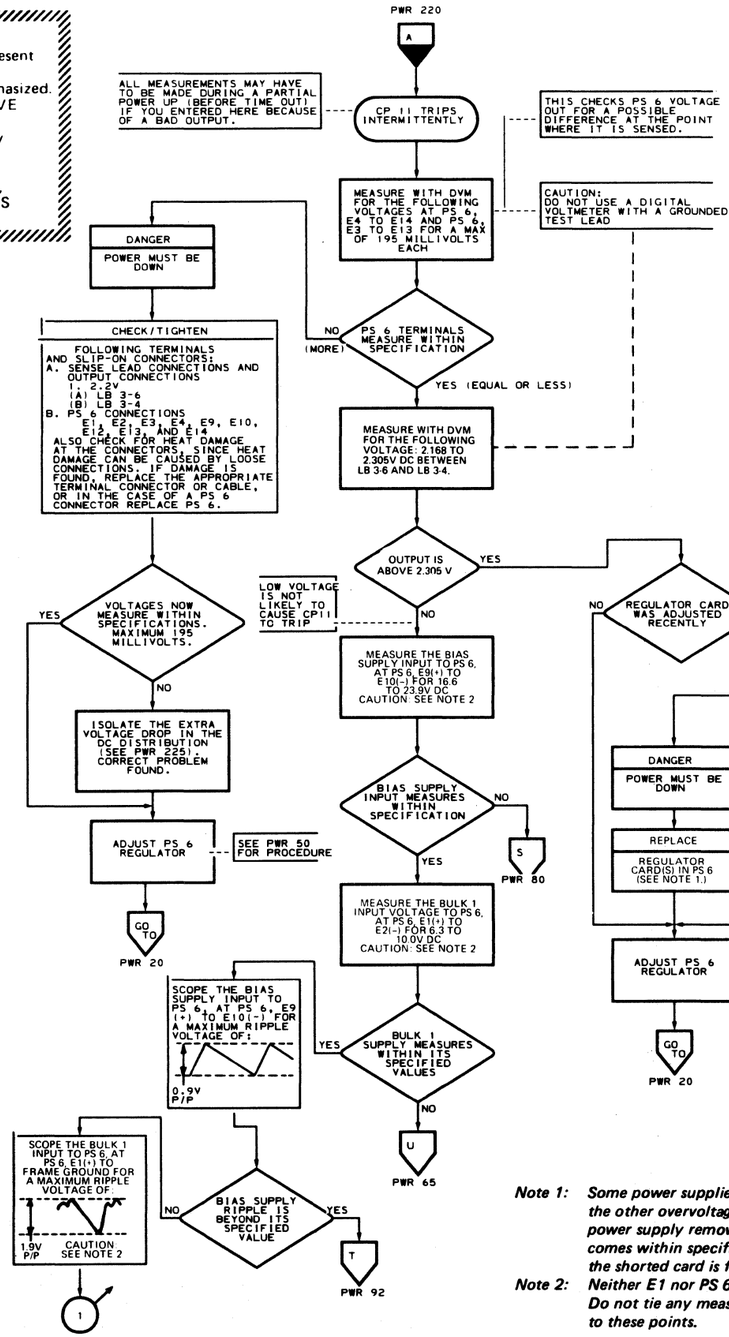
Refer to PWR 50 for adjustment procedure.



CP11 TRIPS (PART 3 OF 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

● SEE PWR 225 FOR VOLTAGE DISTRIBUTION



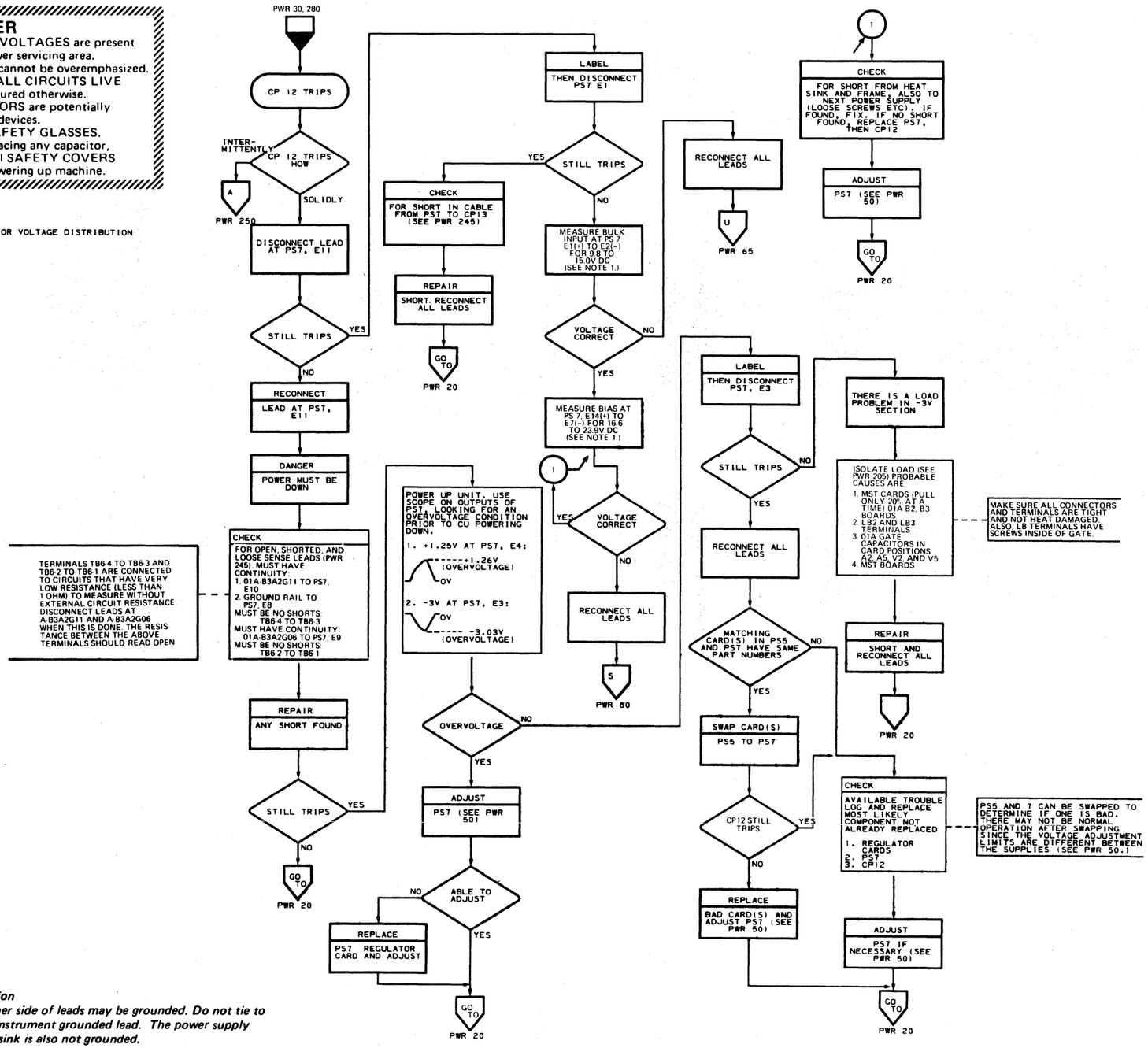
Note 1: Some power supplies have two cards (one a regulator, the other overvoltage). If there are two cards in the power supply remove them both. If the measurement comes within specifications, insert one at a time until the shorted card is found.

Note 2: Neither E1 nor PS 6's heat sink is at frame ground. Do not tie any measuring instrument grounded leads to these points.

CP12 TRIPS (PART 1 OF 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

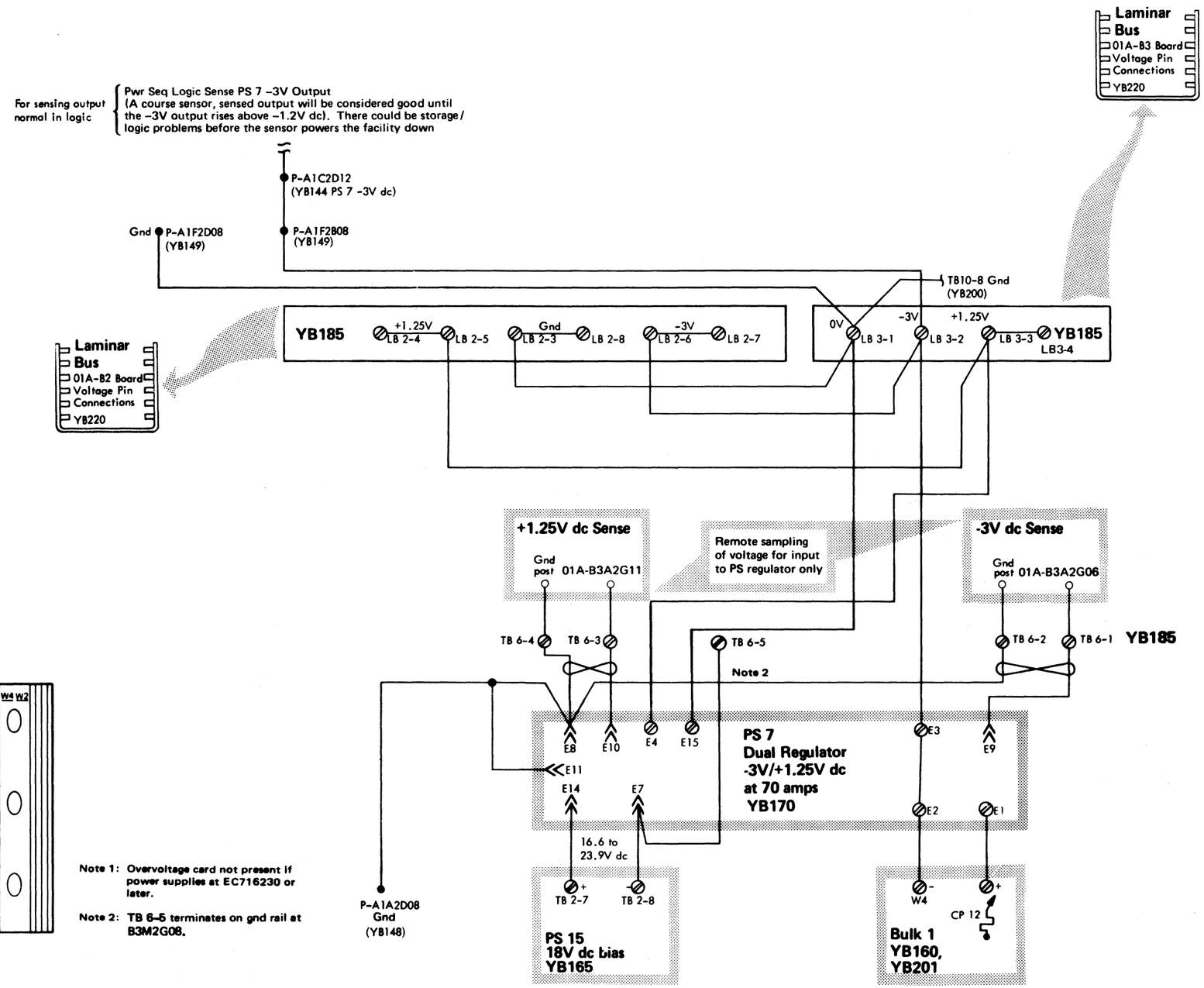
● SEE PWR 245 FOR VOLTAGE DISTRIBUTION

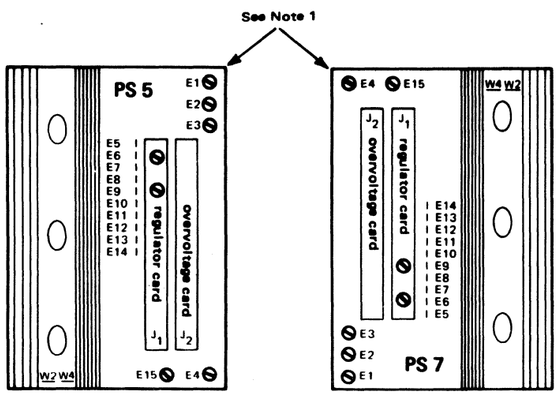


Note 1: Caution
Neither side of leads may be grounded. Do not tie to any instrument grounded lead. The power supply heat sink is also not grounded.

CP12 TRIPS (Part 2 of 3)

PS7 VOLTAGE DISTRIBUTION





Power Supplies are physically inverted on left and right sides. Refer to PWR 50 for adjustment procedure.

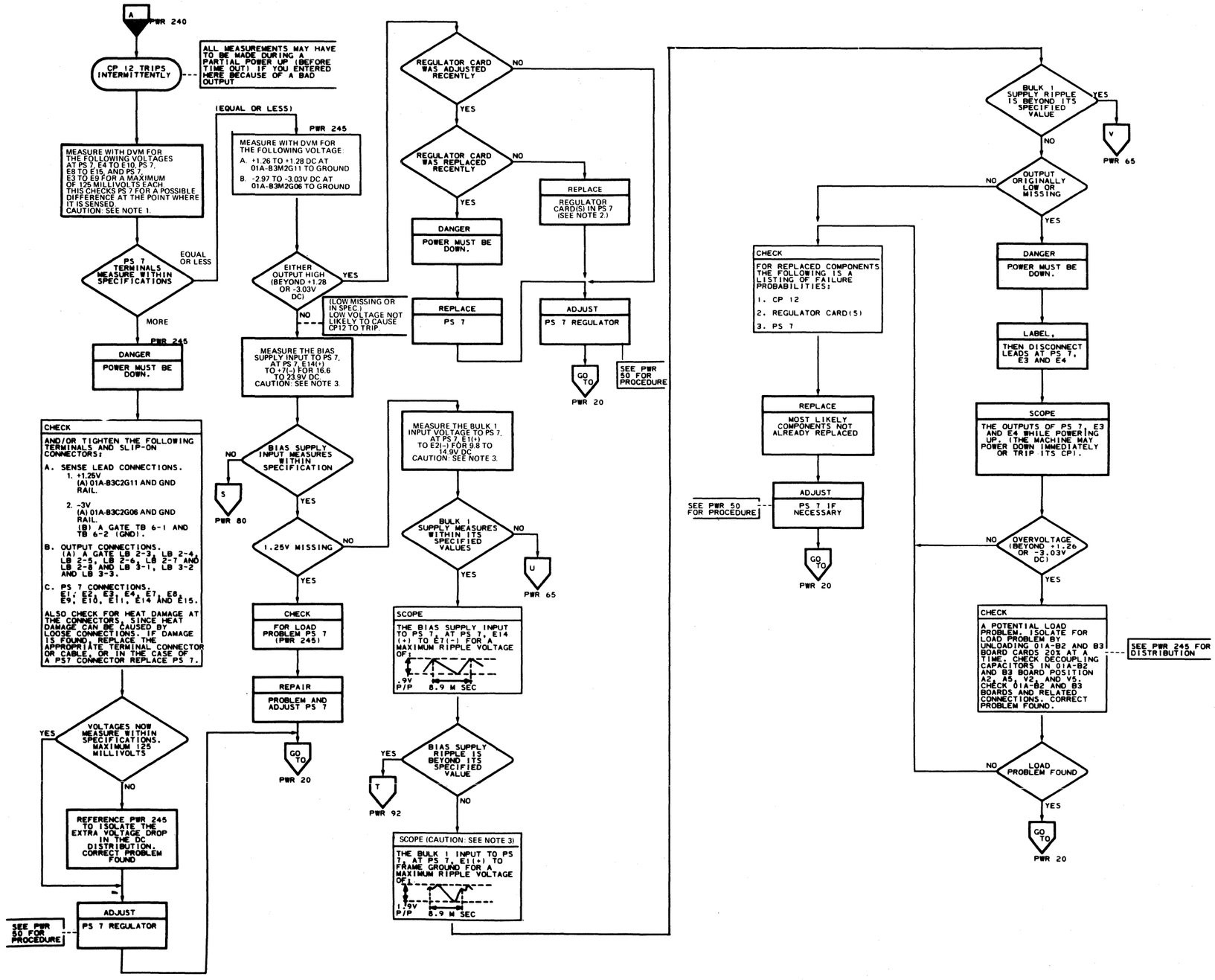
Note 1: Overvoltage card not present if power supplies at EC716230 or later.

Note 2: TB 6-5 terminates on gnd rail at B3M2G08.

CP12 TRIPS (PART 3 OF 3)

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE PWR 245 FOR VOLTAGE DISTRIBUTION.



Note 1: Do not use a digital voltmeter with a grounded test lead.

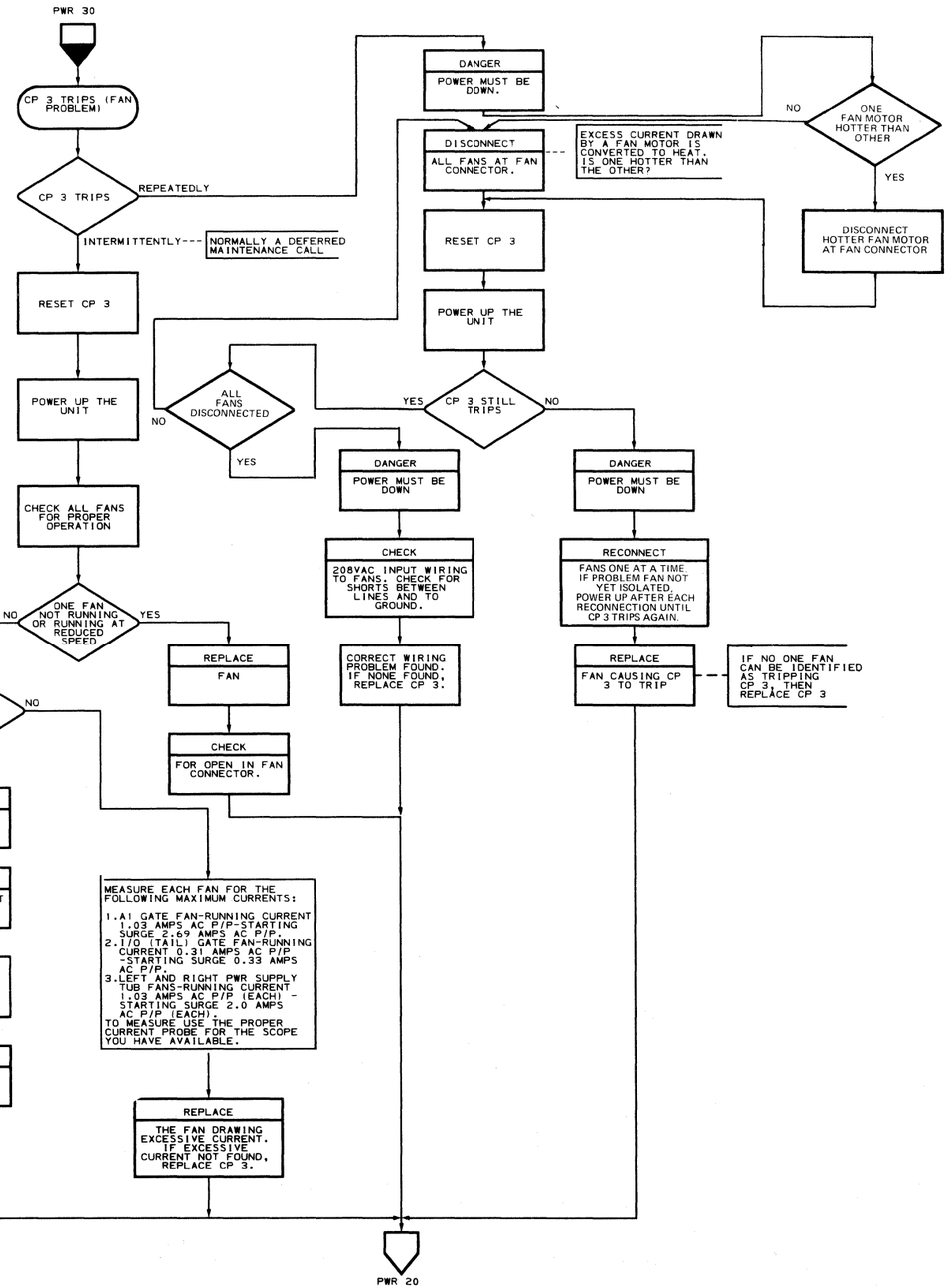
Note 2: Some power supplies have two cards (one a regulator, the other overvoltage). If there are two cards in the power supply remove them both. If the measurement comes within specifications, insert one at a time until the shorted card is found.

Note 3: Neither E1, E2 nor PS 7's heat sink is at frame ground. Do not tie any measuring instrument grounded leads to these points.

CP3 TRIPS (FAN PROBLEM)

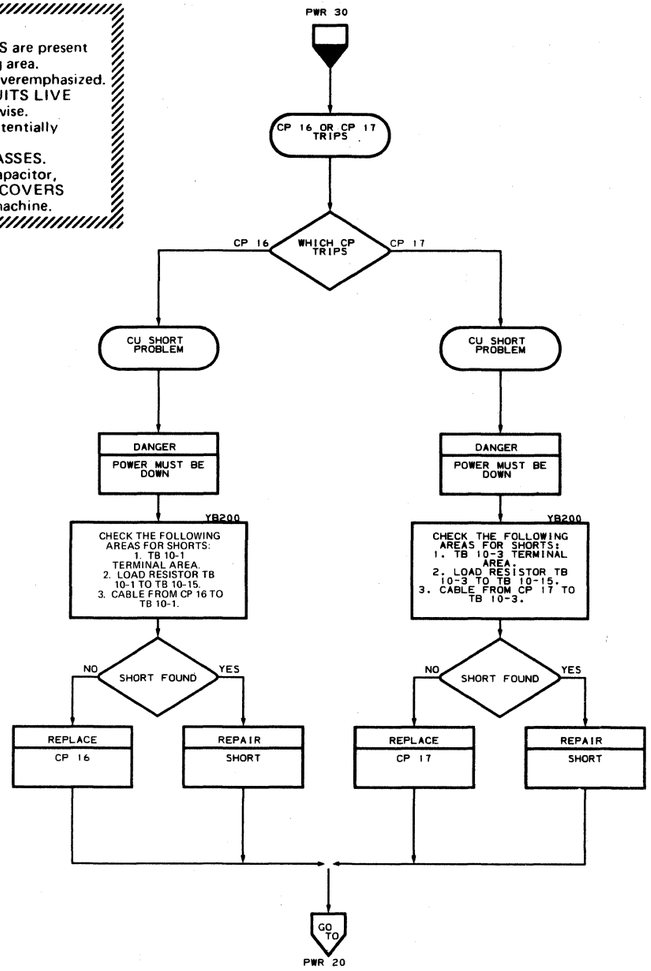
DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

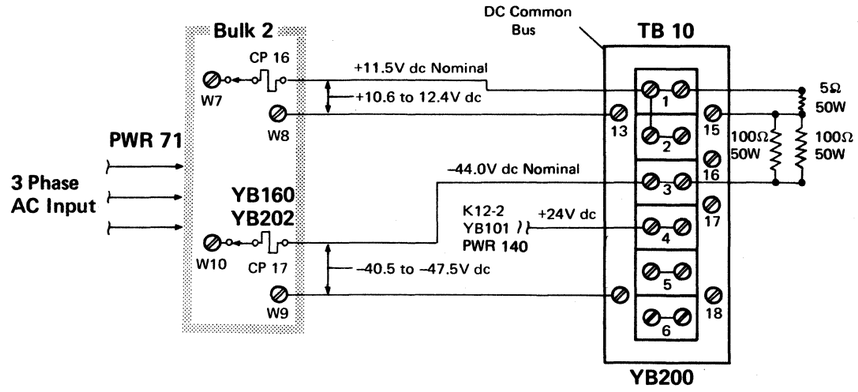
- SEE YB110 FOR CIRCUIT DRAWINGS
  NOTE: POWER SUPPLY FAN NO. 2 NOT USED ON LATE MACHINES.



CP16 OR CP17 TRIPS

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.





Note:
The bulk 2 supply voltages shown on this page are not required by the 3830-2. Terminating resistors are used to maintain balanced loads required for proper operation of the bulk supply.

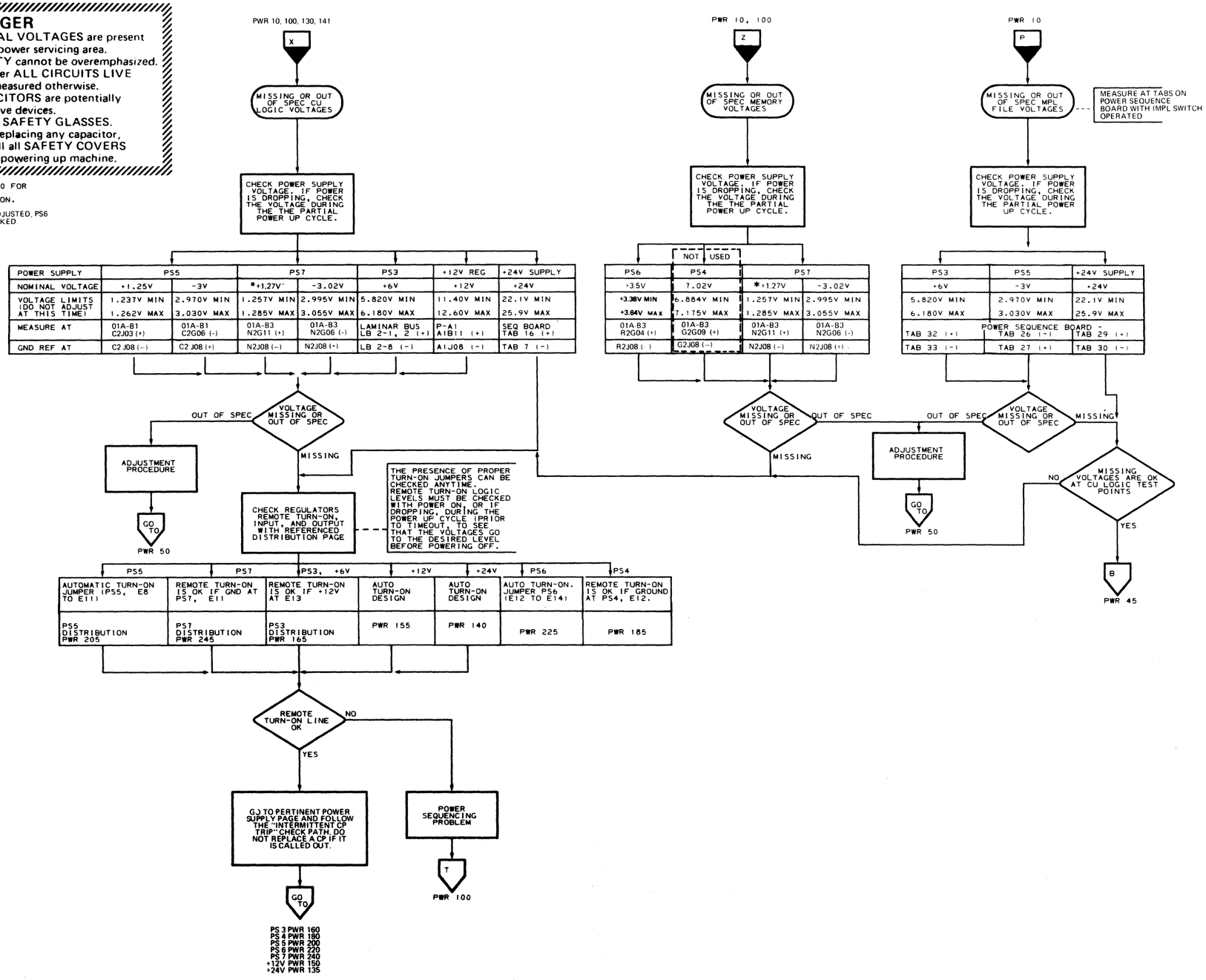
ONLY FOR EARLY MACHINES (with CP 7) PWR 270

3830-2 MISSING OR OUT-OF-SPEC VOLTAGES

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

• SEE PWR 300 FOR VOLTAGE DISTRIBUTION.

* IF +1.27V IS ADJUSTED, PS6 MUST BE CHECKED.



POWER SUPPLY	PS5		PS7		PS3	+12V REG	+24V SUPPLY
NOMINAL VOLTAGE	+1.25V	-3V	*+1.27V	-3.02V	+6V	+12V	+24V
VOLTAGE LIMITS (DO NOT ADJUST AT THIS TIME)	1.237V MIN 1.262V MAX	2.970V MIN 3.030V MAX	1.257V MIN 1.285V MAX	2.995V MIN 3.055V MAX	5.820V MIN 6.180V MAX	11.40V MIN 12.60V MAX	22.1V MIN 25.9V MAX
MEASURE AT	01A-B1 C2J03 (+)	01A-B1 C2G06 (-)	01A-B3 N2G11 (+)	01A-B3 N2G06 (-)	LAMINAR BUS LB 2-1, 2 (+)	P-A1 A1B11 (+)	SEQ BOARD TAB 16 (+)
GND REF AT	C2 J08 (-)	C2 J08 (+)	N2J08 (-)	N2J08 (+)	LB 2-8 (-)	A1J08 (-)	TAB 7 (-)

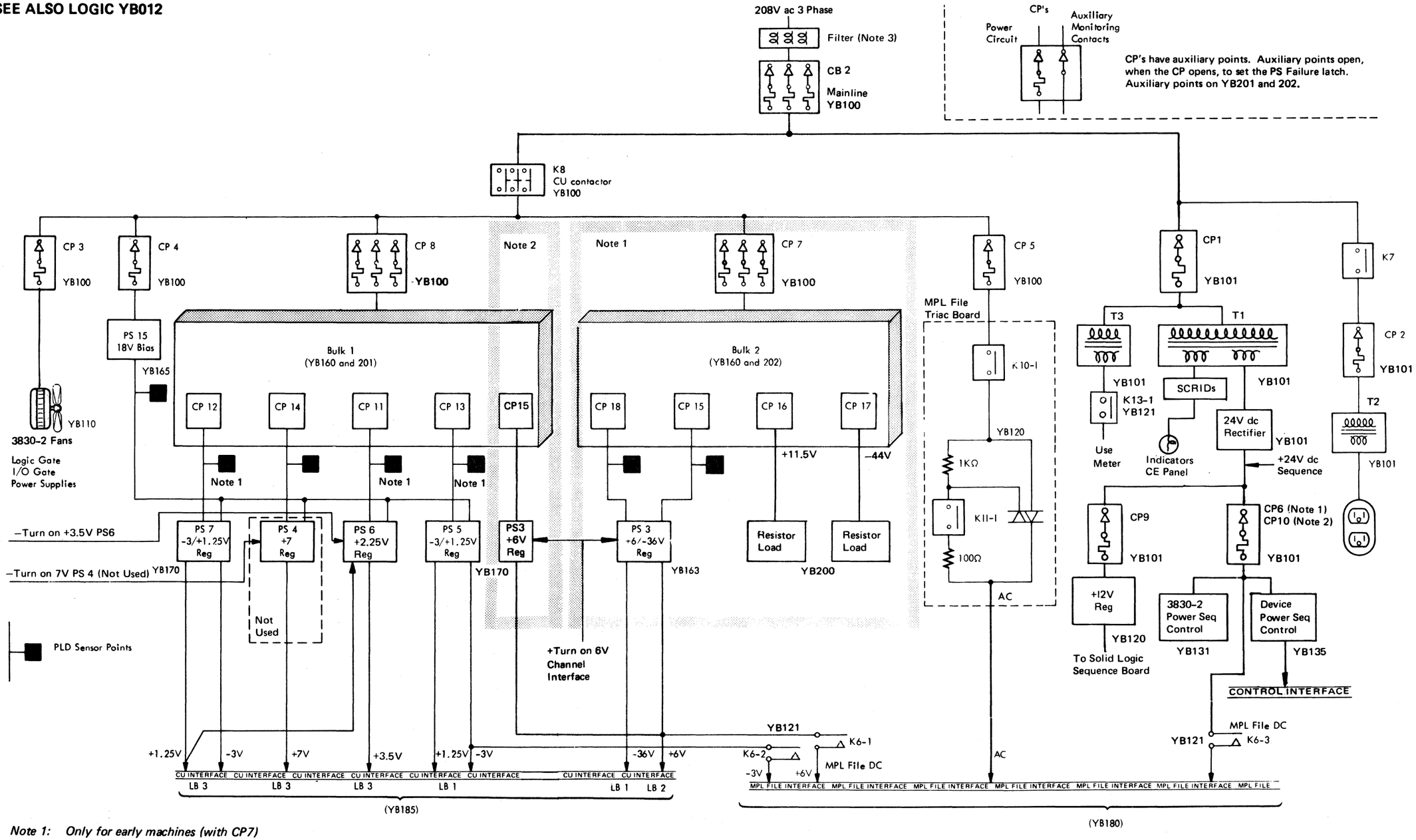
PS6	PS4	PS7	
+3.5V	7.02V	*+1.27V	-3.02V
+3.38V MIN	6.884V MIN	1.257V MIN	2.995V MIN
+3.64V MAX	7.175V MAX	1.285V MAX	3.055V MAX
01A-B3 R2G04 (+)	01A-B3 G2G09 (+)	01A-B3 N2G11 (+)	01A-B3 N2G06 (-)
R2J08 (-)	G2J08 (-)	N2J08 (-)	N2J08 (+)

PS3	PS5	+24V SUPPLY
+6V	-3V	+24V
5.820V MIN	2.970V MIN	22.1V MIN
6.180V MAX	3.030V MAX	25.9V MAX
TAB 32 (+)	POWER SEQUENCE BOARD - TAB 26 (-)	TAB 29 (+)
TAB 33 (-)	TAB 27 (+)	TAB 30 (-)

PS5	PS7	PS3, +6V	+12V	+24V	PS6	PS4
AUTOMATIC TURN-ON JUMPER (PS5, E8 TO E11)	REMOTE TURN-ON IS OK IF GND AT PS7, E11	REMOTE TURN-ON IS OK IF +12V AT E13	AUTO TURN-ON DESIGN	AUTO TURN-ON DESIGN	AUTO TURN-ON. JUMPER PS6 (E12 TO E14)	REMOTE TURN-ON IS OK IF GROUND AT PS4, E12.
PS5 DISTRIBUTION PWR 205	PS7 DISTRIBUTION PWR 245	PS3 DISTRIBUTION PWR 165	PWR 155	PWR 140	PWR 225	PWR 185

DISTRIBUTION, CONTROL UNIT AC AND DC

SEE ALSO LOGIC YB012

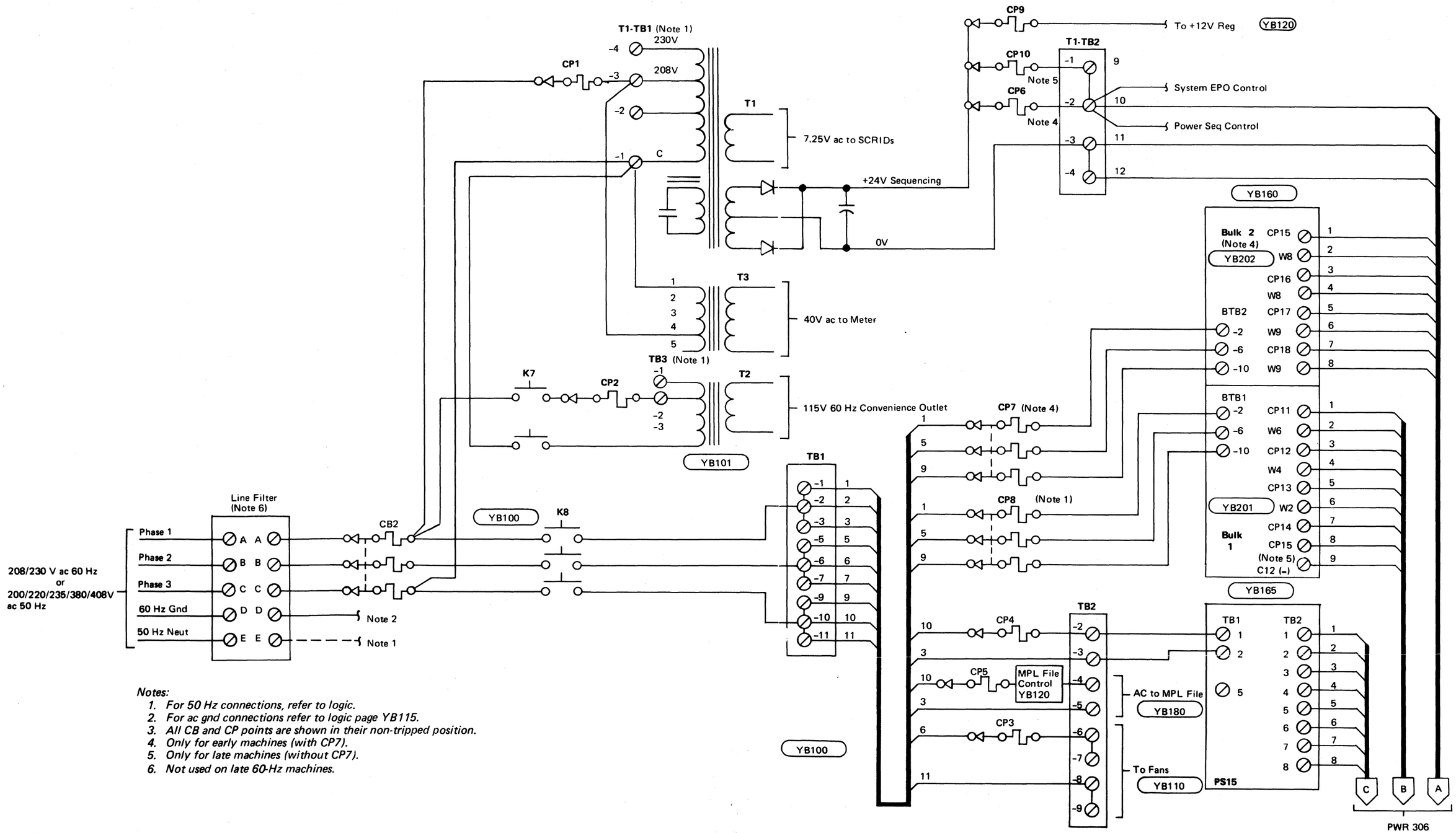


Note 1: Only for early machines (with CP7)

Note 2: Only for late machines (without CP7)

Note 3: Not used on late 60-Hz machines

DISTRIBUTION BY POWER TERMINALS (Part 1 of 2)



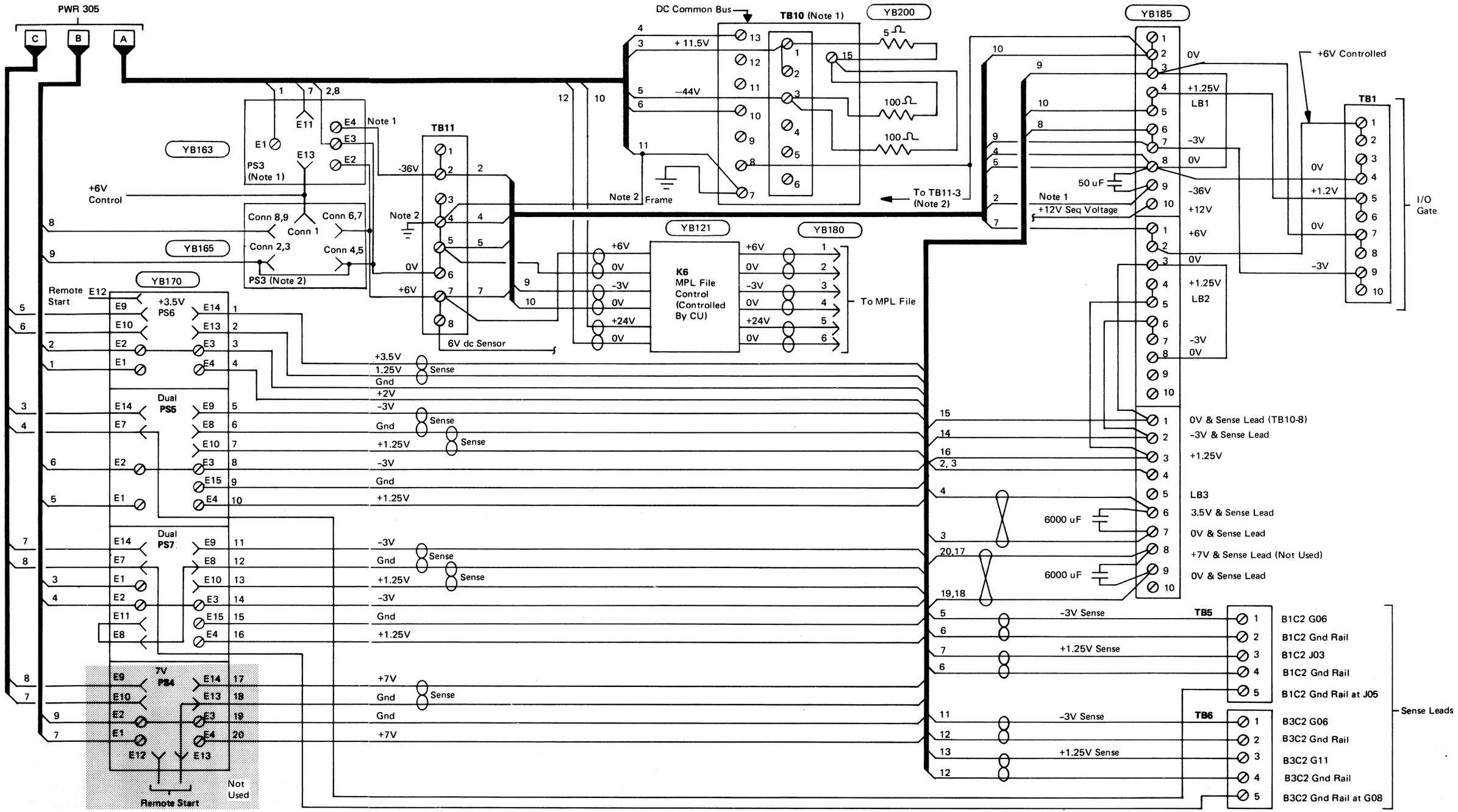
Notes:

1. *For 50 Hz connections, refer to logic.*
2. *For ac gnd connections refer to logic page YB115.*
3. *All CB and CP points are shown in their non-tripped position.*
4. *Only for early machines (with CP7).*
5. *Only for late machines (without CP7).*
6. *Not used on late 60-Hz machines.*

DISTRIBUTION BY POWER TERMINALS (Part 1 of 2)

PWR 305

DISTRIBUTION BY POWER TERMINALS (Part 2 of 2)



Note 1: Only for early machines (with CP7)

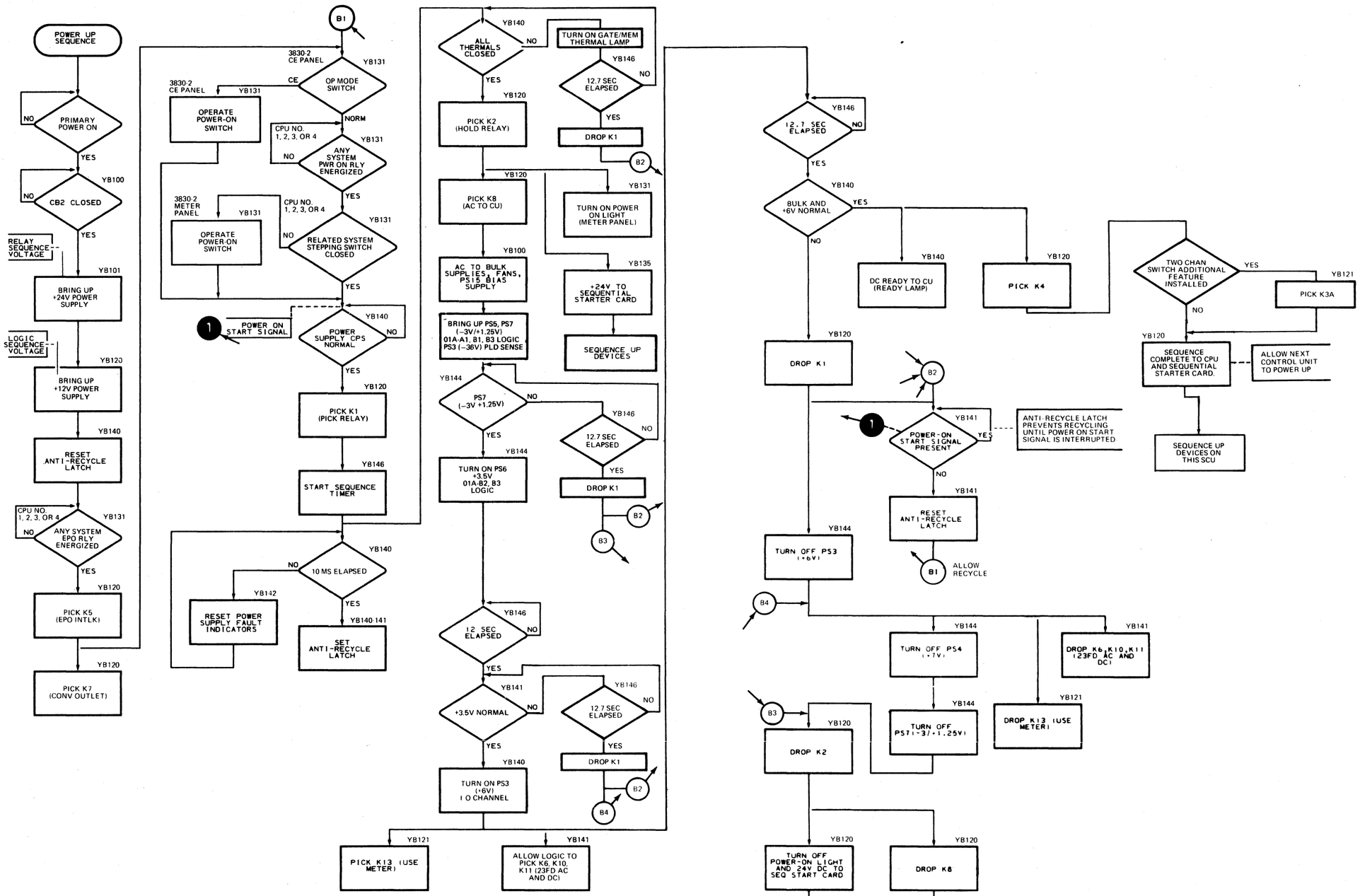
Note 2: Only for late machines (without CP7)

POWER SEQUENCING FLOWCHART (PART 1 OF 2)

POWER UP SEQUENCE

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE PWR 2 FOR WRITTEN DESCRIPTION OF POWER SEQUENCE
- SEE PWR 110 FOR VOLTAGE SEQUENCE LOGIC



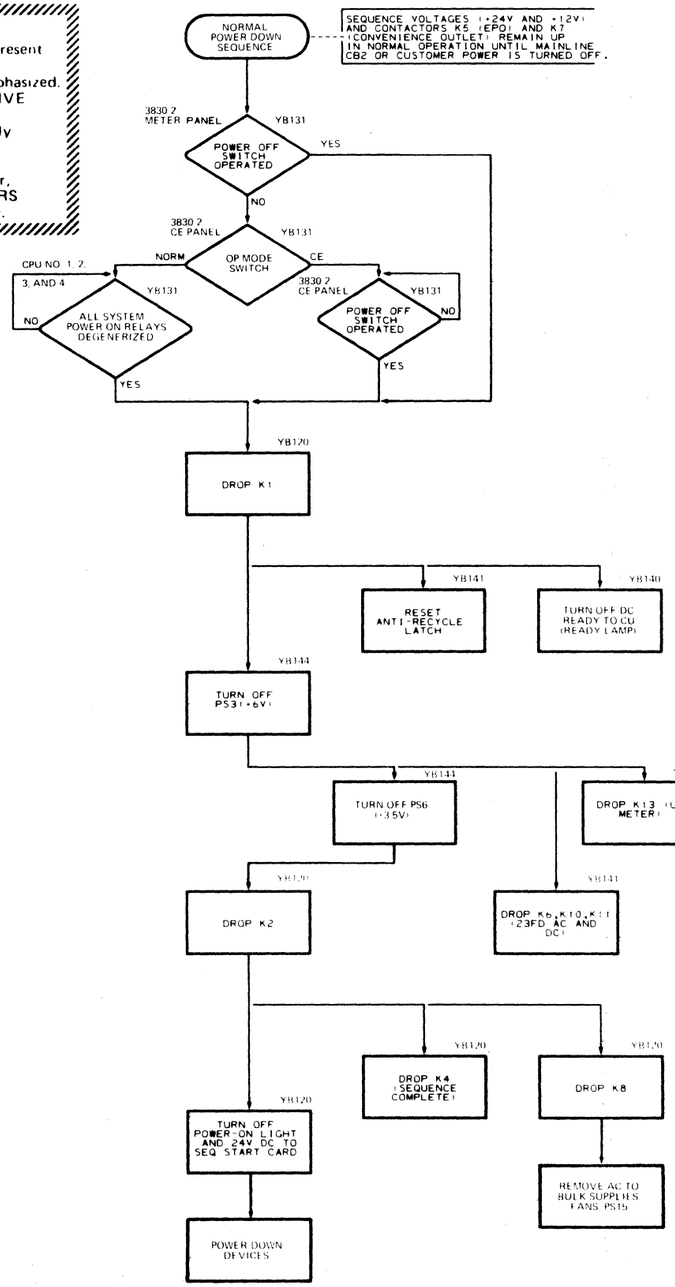
*Only for early machines (with CP 7).

POWER SEQUENCING FLOWCHART (PART 2 OF 2)

NORMAL POWER DOWN SEQUENCE

DANGER
LETHAL VOLTAGES are present in the power servicing area.
SAFETY cannot be overemphasized.
Consider ALL CIRCUITS LIVE until measured otherwise.
CAPACITORS are potentially explosive devices.
WEAR SAFETY GLASSES.
After replacing any capacitor, reinstall all SAFETY COVERS before powering up machine.

- SEE PWR 2 FOR WRITTEN DESCRIPTION OF POWER SEQUENCE
- SEE PWR 110 FOR VOLTAGE SEQUENCE LOGIC



ABNORMAL POWER DOWN SEQUENCES

- Any power supply CP trips.
- Any thermal opens.
- PS3, PS4, PS6, or PS7 low voltage sensed.
- Power line disturbance (PS15 or bulk supply low voltage sensed).

Any of these conditions will cause a complete dc power shutdown, but with minor variations to the normal power down sequence. A power supply CP tripping or a thermal opening will turn on an indicator lamp on the power sequence box.

In every abnormal power shutdown, the anti-recycle latch is reset so that after the problem is corrected power can be restored in the sequence shown on PWR 310, beginning at entry B1.

CONTENTS

INTR

FEATURE DESCRIPTION

INTRODUCTION

This page describes the gate board and card configurations associated with feature codes of the 3830-2. It also describes the features and identifies the maintenance disk for each.

Maintenance Disk for the features are:

4 or 6K machines without "F" register feature:

1 channel	2346600
2 channel	2346601
2 channel addition	2346602

All machines with 8K Snipe, "F" register and offset

1 channel	2346605
2 channel	2346606
2 channel addition	2346607

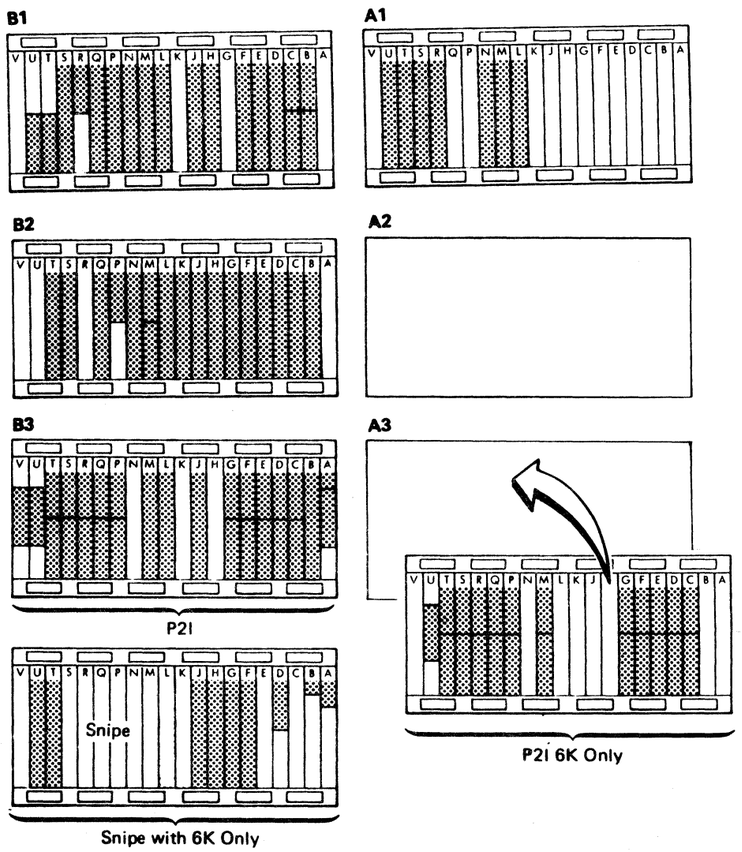
2150 Feature Code Description

Feature Code description expansion of storage to 6K (P21 or Snipe).

Board/Card Configuration

Add board with cards type 7243 in positions C, D, E, F, G, P, Q, R, S, T in gate location A3.

If 2150 feature is used on snipe machine a snipe board, with 6K storage, replaces the P2I board in gate position B3 and no board is required in gate position A3.



2151 Feature Code Description

Expansion of storage to 8K (Snipe) and offset.

Board/Card Configuration

Replace board P/N 818186 with Snipe board P/N 2348886 in gate location B3. Remove board P/N 818186 (if present) in gate position A3. On board P/N 2345450 position U2 and S2, replace cards type 0792 and 0794 with cards type BA82 and BA89 (offset function).

Snipe Board

Storage size can be determined as follows:

F + G = 4K

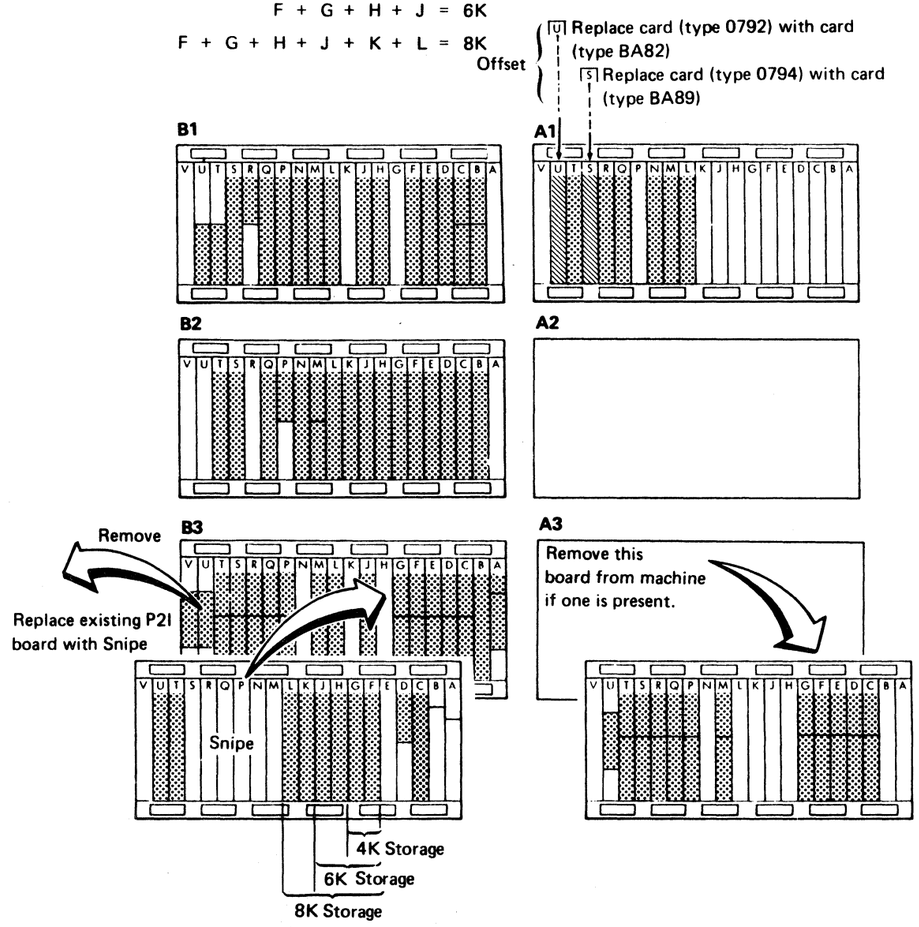
F + G + H + J = 6K

F + G + H + J + K + L = 8K

Offset

U Replace card (type 0792) with card (type BA82)

S Replace card (type 0794) with card (type BA89)

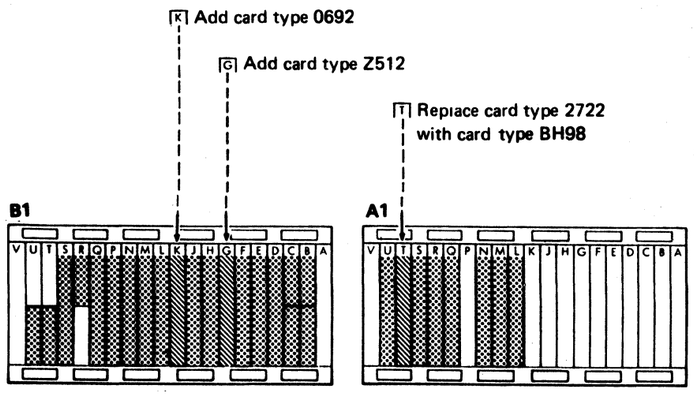


6111 Feature Code Description

Addition of "E" and "F" registers and 64 bit address.

Board/Card Configuration

On board P/N 2345452 gate location B1, add card type 0692 in "K" position and card type Z512 in "G" position. On board 2345450 gate location A1, replace card type 2722 in position "T" with card type BH98.



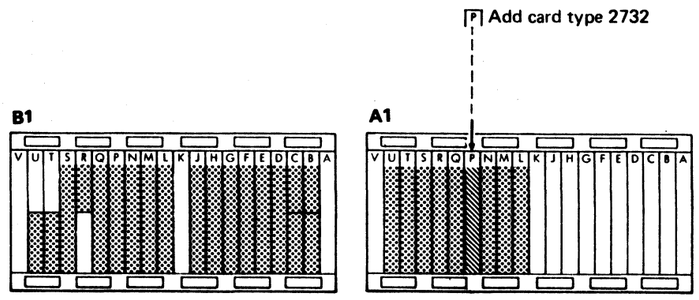
8170 Feature Code Description

Addition of 2 channel switch.

Board/Card Configuration

On board 2345450 gate location A1, add card type 2732 in the "P" position.

Note: *Cards type 7548 and 7552 must also be added in tailgate 01B to complete 2 channel switch addition. See installation instructions for details.*



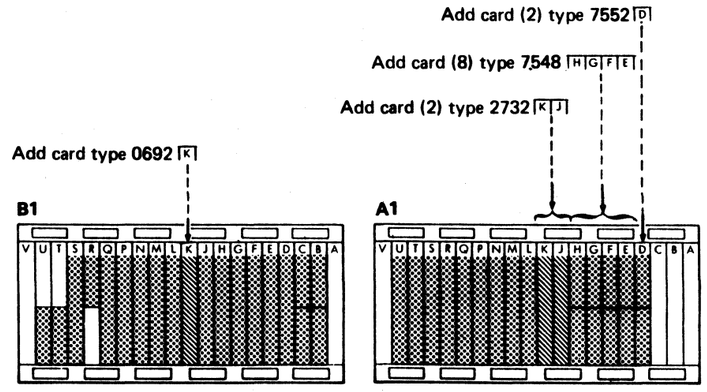
8171 Feature Code Description

Addition of second 2 channel switch.

Board/Card Configuration

"K" position on board P/N 2345452 gate location B1 may have card type 0692 (if 6111 feature is installed) in place. If not, it is required for this feature.

On board 2345450 gate location A1, card type 2732 must be plugged in the "K" and "J" positions. On the same board, plug card type 7548 in positions E2, E4, F2, F4, G2, G4, H2 and H4. 7552 plug in D2, D4.



INTRODUCTION TO THE IBM 3830 STORAGE CONTROL, MODEL 2

The IBM 3830 Storage Control, Model 2, is a standalone control unit designed for attachment to channels conforming to the IBM System/370 architecture.

The 3830-2, with attached disk storage facilities provides high-performance, medium to high capacity, online data handling capabilities for using systems. The disk storage subsystem serves as a primary direct access storage for general applications, such as: airlines reservations, inventory control, message switching, graphic processing, time sharing, and management information systems.

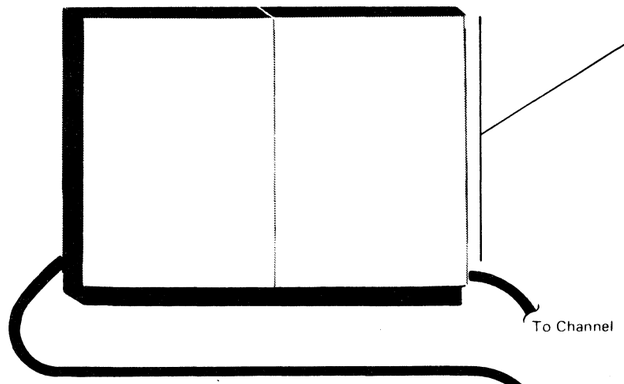
General Description

The 3830-2 with an attached disk storage facility, closely follows the design concepts introduced by the IBM 2314 and the IBM 3330.

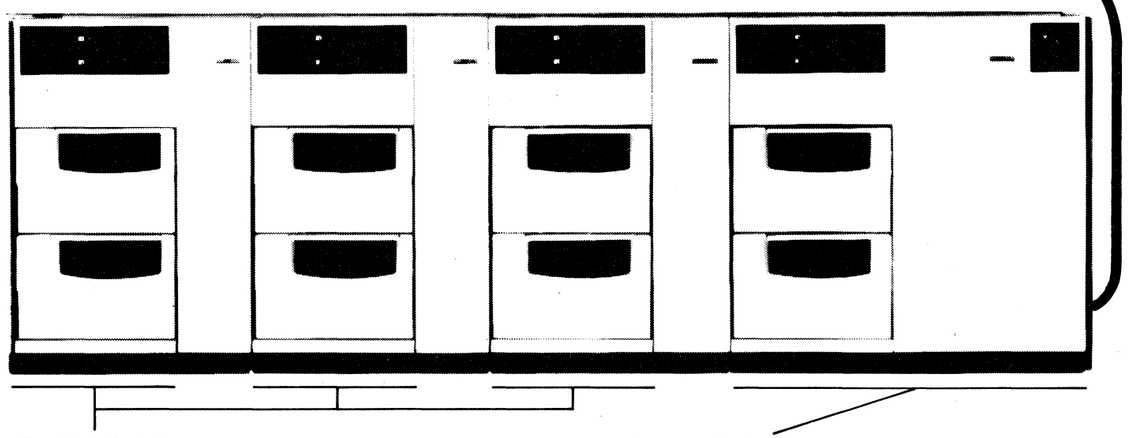
The 3830-2 provides the circuit and microprogram controls to perform commands transmitted from the CPU by the channel.

The 3830-2 can control up to four facilities (control modules). Each facility can contain up to eight devices, with up to four logical addresses on each device (logical address cannot exceed 64 per 3830-2).

IBM 3830 STORAGE CONTROL, MODEL 2



DISK STORAGE FACILITY



The IBM 3830-2 Storage Control performs the following functions:

- Interpret and execute commands issued by the channel.
- Control the channel and facility interfaces.
- Transfer data to and from the channel and disk storage facility.
- Perform data error detection and correction.
- Furnish facility status to the using system.
- Perform diagnostic evaluation of the facility.

The 3830-2 is also referred to as the storage control unit (SCU).

The 3830-2 is functionally controlled by programs resident in its control storage. The control storage is automatically loaded from a read-only device which is included in the 3830-2.

The channel commands that control the subsystem operations are described in the CMD section.

A description of how to read and use the CAS printout of the microprogram is included in the MIC section.

Satellite Modules

Up to eight devices can be attached to each controller. Each device can have up to four logical addresses.

In a disk storage facility, the primary functions performed by each disk drive are:

- Position the access mechanism to a cylinder.
- Select a head.
- Read or write data.
- Respond to commands given by the 3830-2.

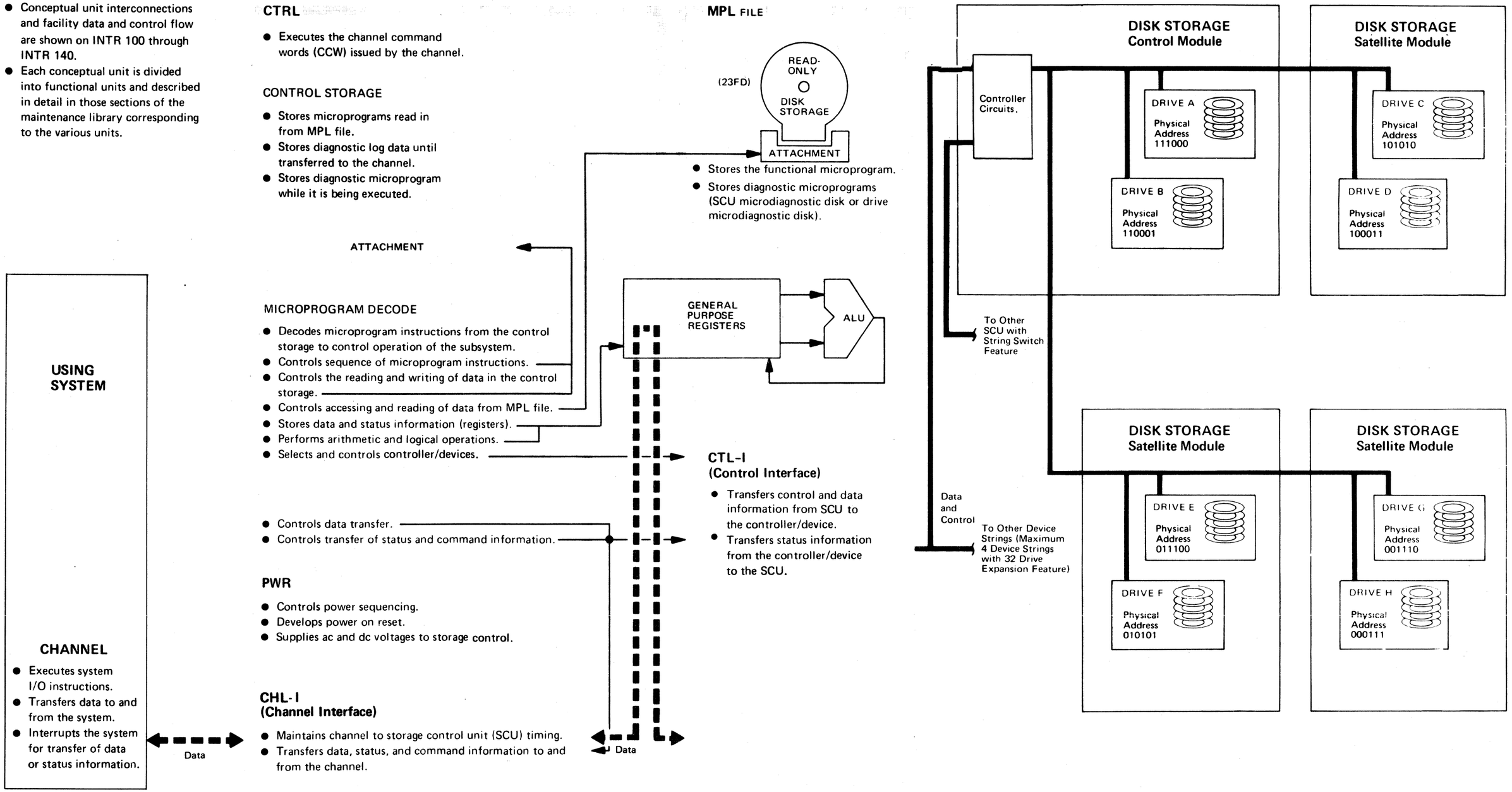
Control Module

One, two, or four control modules can be attached to each 3830 Storage Control, Model 2. The control module contains the controller circuitry for attached devices. This includes the devices in the control module and those in the satellite modules. The primary functions performed by the controller circuitry in a disk storage facility are:

- Respond to commands given by the 3830-2.
- Select one of up to eight disk drives. There can be up to four logical addresses for each drive.
- Control data read and write operations of the device.
- Provide ECC data error correction information.
- Pass on control operations from the 3830-2 to the selected device.
- Provide rotational position information on each drive to the 3830-2.

DISK STORAGE SUBSYSTEM CONCEPTUAL UNITS

- This diagram defines the conceptual units of the subsystem and how these units function.
- Conceptual unit interconnections and facility data and control flow are shown on INTR 100 through INTR 140.
- Each conceptual unit is divided into functional units and described in detail in those sections of the maintenance library corresponding to the various units.



FACILITY ERROR COLLECTION

- This page gives a summary of the various error collection methods and where more information can be found in the MLM.
- Facility error information is collected on three levels; system, storage control unit, and device.

SYSTEM

Performance Data Collection	MSG 10
Console Error Message Analysis	MSG 20
EREP Descriptions	MSG 30–40
OLT Descriptions	OLT 1

STORAGE CONTROL UNIT

Status Information	CMD 180, 181
Sense Information	SENSE 1
Error Symptom Code	FSI 5
Control Storage Contents	CTRL 650, 652
CE Panel	PANEL 10
Check 1 Error Collection	PANEL 40, 41
Check 2 Error Collection	PANEL 50, 51

Error Collection Diagrams (ECD) for each error are located in machine section (CHL–I, CTRL, MPL, CTL–I).

Microdiagnostic Routine Summary	MICRO 10
Microword Formats	MIC 10–18
Command Retry	CMD 210

Check 1 Errors

Check 1 errors are errors that prevent the microprogram from operating correctly; therefore, operation of the SCU is stopped.

Check 2 Errors

Check 2 errors are errors that are detected by circuits in the device or attachment areas of the SCU. These errors do not affect the operation of the microprogram. The microprogram collects, decodes, and transfers this information to the CPU as status and sense data.

Microprogram Detected Errors

The microprogram monitors Check 2 errors while using any of the attachments of the SCU. The microprogram also can detect other errors that are not of a circuit failure type (end of file, command reject, etc.). The microprogram logs errors in control storage, decodes them into sense data, and transfers them to the CPU on a Sense command.

DEVICE

For details of device errors see the device MLM.

Check-2 Error Collection (Controller Error)	PANEL 50
Sense Summary	SENSE 1
Control Storage Contents (Device Error Logging In)	CTRL 650, 652

3830-2 DATA FLOW INTRODUCTION

- INTR 105 – 140 show the basic data flow paths and functional components of the storage control unit.
- References are given to other diagrams for more information.

CONTROL STORAGE

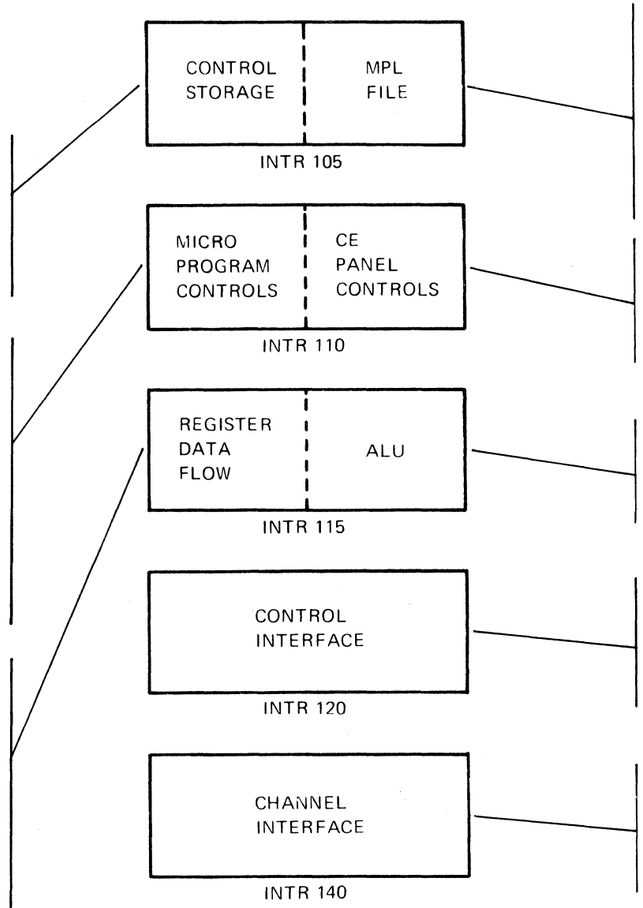
- 4,096-byte writable control store.
- 2,048 or 4,096 byte control store extension feature.
- Four-byte read/write control storage transfer.
- Addressed by the address bus.
- Output of instructions or data is on the read bus.

MICROPROGRAM CONTROLS

- IAR addresses control storage during instruction cycles.
- DAR addresses control storage during data cycles (store/fetch).
- Backup address (BAR) register holds address on errors.
- Error register holds check-1 errors (CU).
- SA-SD registers, error register, or BAR puts data on the write bus to control storage.
- Microprogram decodes control the CU operations.
- ST (status) register and BR (branch) register control microprogram branching.

REGISTER DATA FLOW

- General purpose (GP) registers store data for the use of the microprogram.
- F Registers are used as general purpose registers or as temporary, automatic incrementing storage buffers. Automatic mode is microprogram controlled using Special op (code) 12, and bits set in the TF-register.
- Four Registers, SA, SB, SC, SD are used as entry from and exit to control storage.
- Two Registers, ST and BR are used for microprogram branching.
- Fifteen Registers have exits to the A bus and A register input to ALU.
- All GP registers have exits to the B bus and B register input to ALU.
- Selected registers have entry and/or exits to the channel interface or control interface to the control module.



MPL FILE AND ATTACHMENT

- Functional or diagnostic microprograms on 23FD disk.
- On IMPL (initial microprogram load) operations, the attachment circuitry controls reading of data from the disk through the D bus to the S registers. The data is then transferred via the write bus to control storage.
- Microprogram, through the attachment, controls reading after the first record.

CE PANEL CONTROLS

- CE panel and controls provide data entry, read out, and operation controls for maintenance.
- Clock and cycle controls provide the basic timing of control unit operations.

ARITHMETIC LOGIC UNIT

- Perform logical AND, OR, Add, Subtract, and Exclusive OR operations.
- Only path for register–to–register transfers.

CONTROL INTERFACE (CTL-I)

- Provides a data path to and from the control module(s) attached.
- Provides communication between the microprogram and the control module(s) for control of device operations.

CHANNEL INTERFACE (CHL-I)

- Provides communication between the channel and the CU microprogram.
- Provides a data path to and from the channel.
- May be single channel, two channel, or four channel interface.

READ DATA PATH

Data from the device enters the CTL-I Buffer from CTL-I bus in and is transferred to the MA register. The microprogram transfers the byte from MA to B bus through the ALU and D bus to the MD register. The byte is transferred to the channel interface buffer and onto the channel bus in lines.

WRITE DATA PATH

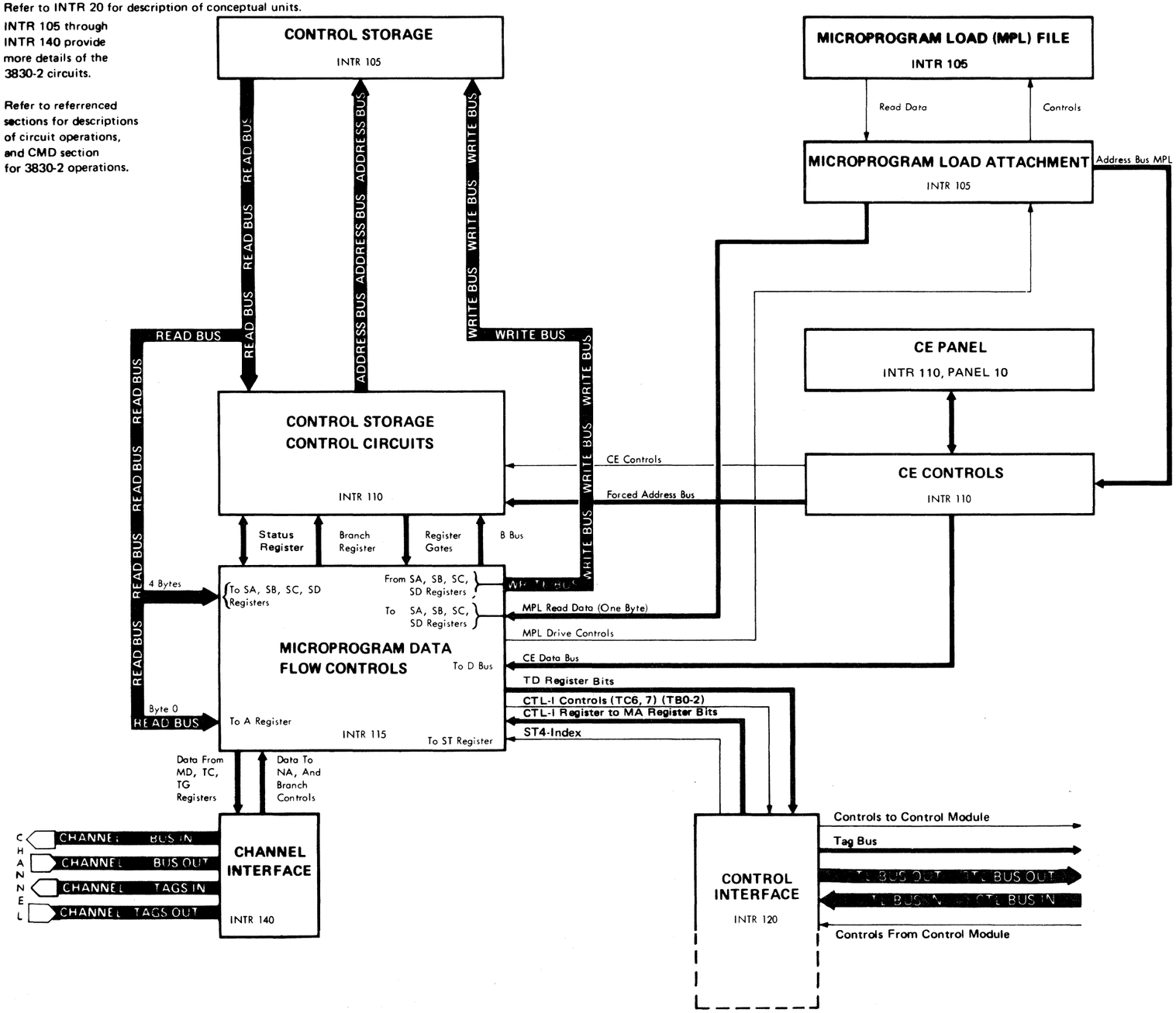
Data from the channel enters the channel interface buffer from channel bus out and is transferred to the NA register. The microprogram transfers the byte from NA to the B bus, through the ALU and D bus to the TA register. The byte is transferred to the CTL-I buffer and onto the CTL-I bus out lines.

3830-2 DATA FLOW

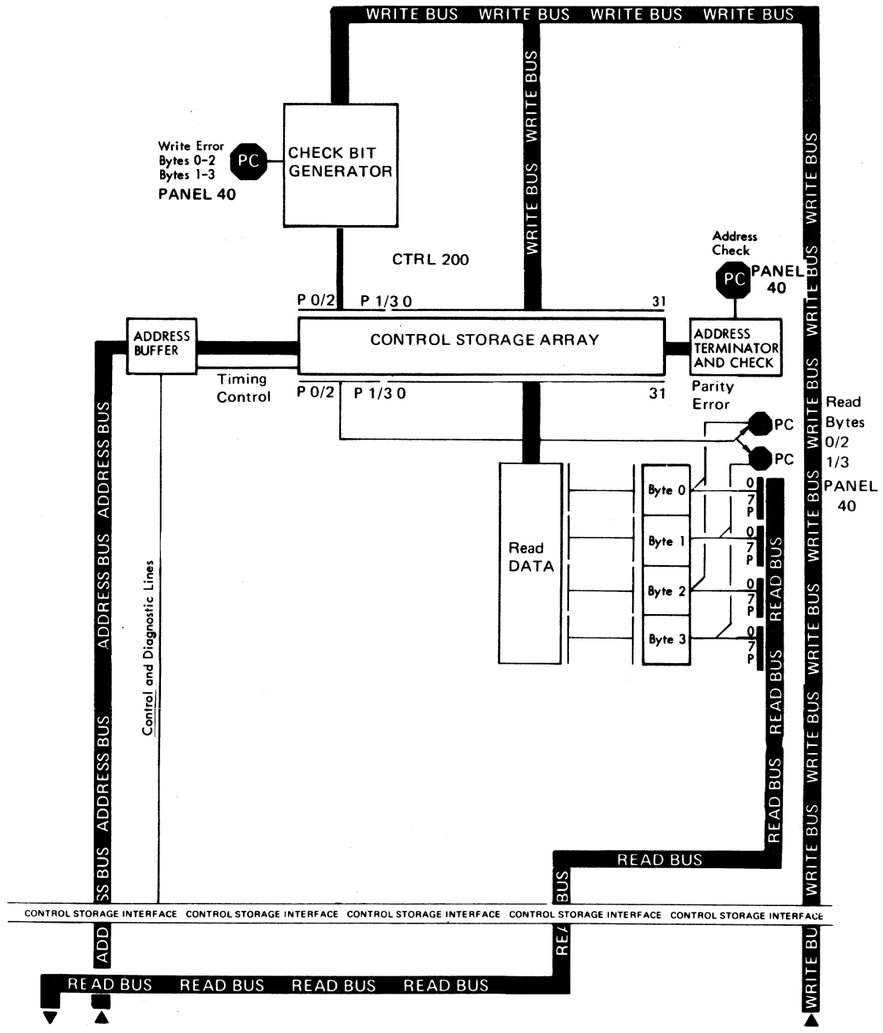
Refer to INTR 20 for description of conceptual units.

INTR 105 through INTR 140 provide more details of the 3830-2 circuits.

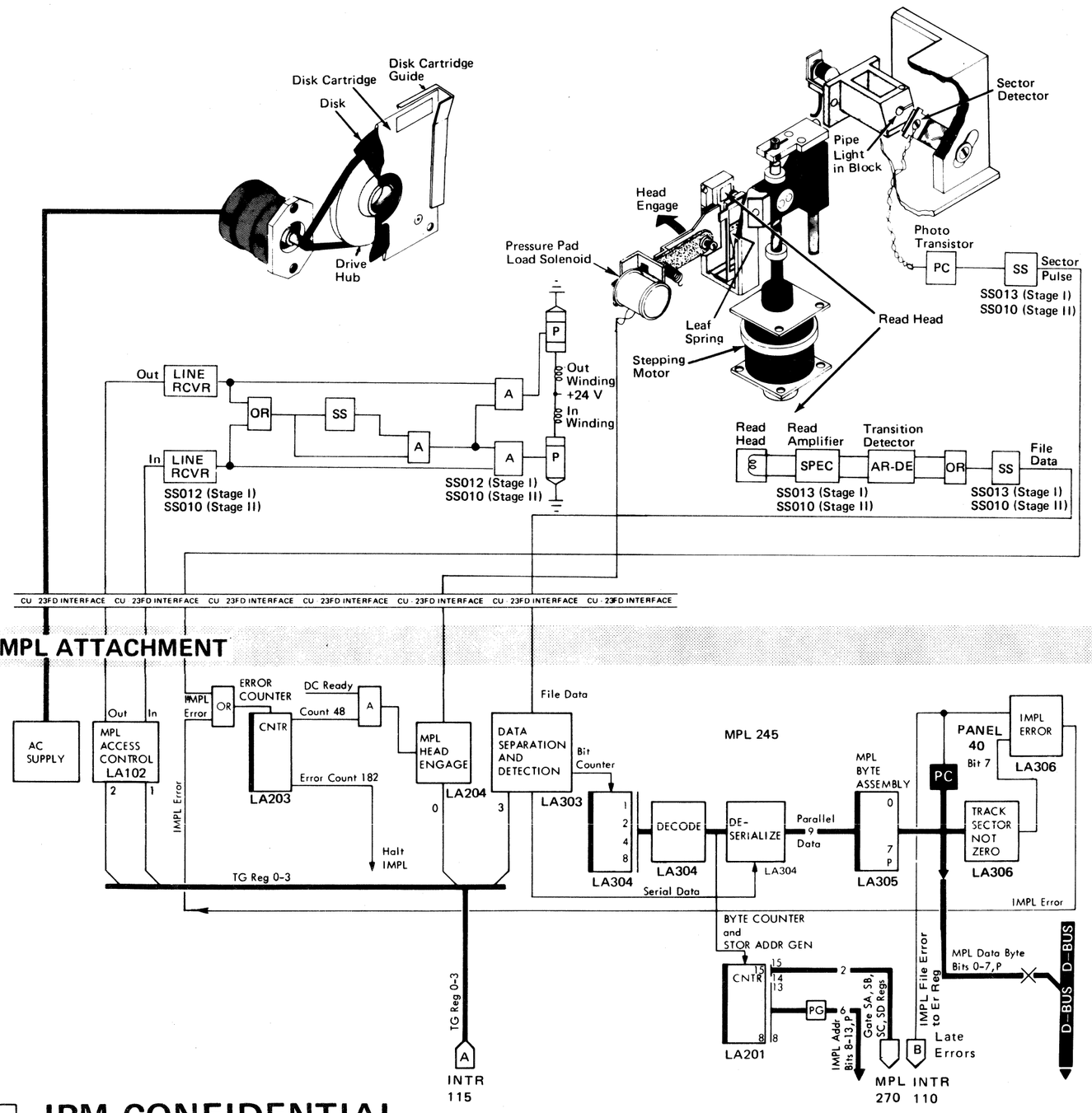
Refer to referrenced sections for descriptions of circuit operations, and CMD section for 3830-2 operations.



CONTROL STORAGE

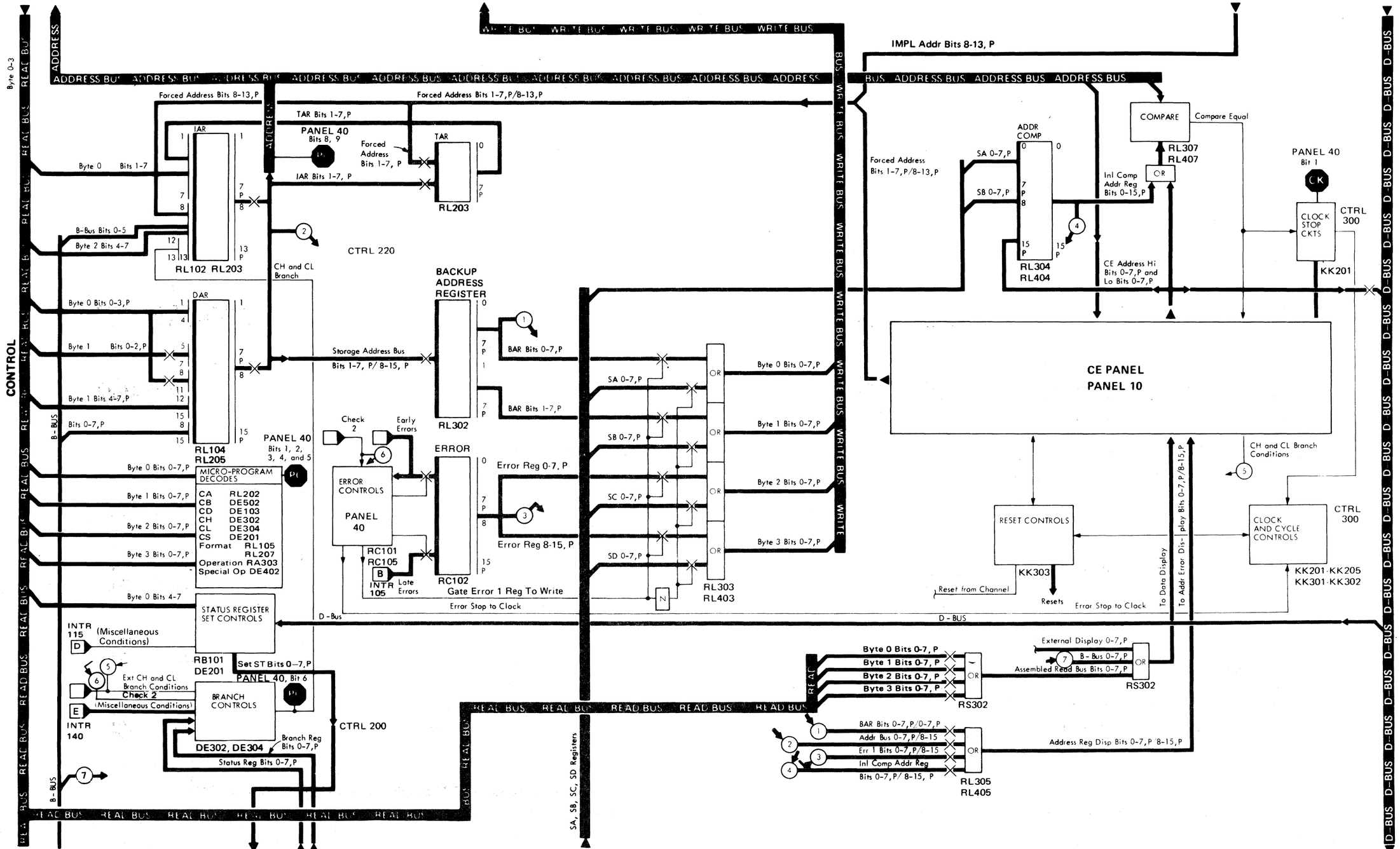


MPL FILE (23FD)



MPL ATTACHMENT

STORAGE CONTROL UNIT CONTROLS



Read Byte 0, Bits 0-7, P

(To Write Bus)

Read Byte 0, Bits 0-7, P

B-BUS

Status Reg Bits 0-7, P

Branch Reg Bits 0-7, P

Assembled Read Bus

READ BUS

Byte 0, Bits 0-7, P

Byte 1, Bits 0-7, P

Byte 2, Bits 0-7, P

Byte 3, Bits 0-7, P

Assembler

D-BUS

PANEL 40 Bit 6

CK

SA RS101

SB RS203

SC RS103

SD RS201

ST RB101

BR RB103

TG RB104

GA RG104

NA RG103

TA RG101

MA RG102

GB RG204

NB RG203

TB RG201

MB RG202

GC RG304

NC RG303

TC RG301

MC RG302

GD RG404

ND RG403

TD RG401

MD RG402

GE * RG504

NE * RG503

TE * RG501

ME * RG502

GF RG604

NF RG603

TF RG601

MF RG602

INTR 105

A

0-3

A-BUS

B-BUS

ZERO TEST RA302

D-Bus Equal Zero

D

INTR 110

INTR 110

Carry In to ALU

RA303

Carry Out Latch

A-REGISTER

REG

RA101 RA201 RA301

PC

PANEL 40 Bit 4

ARITH LOGIC UNIT (ALU)

See RA305 for gating of MPL and CE data onto D-Bus.

PANEL 40 Bit 5

B-REGISTER

N

RA103 RA203 RA301

Sequentially gated to SA, SB, SC, SD

Selected Channel Bus Out and Special Op 14

B To/From Channel Controls INTR 140

C To/From CTL-I INTR 120

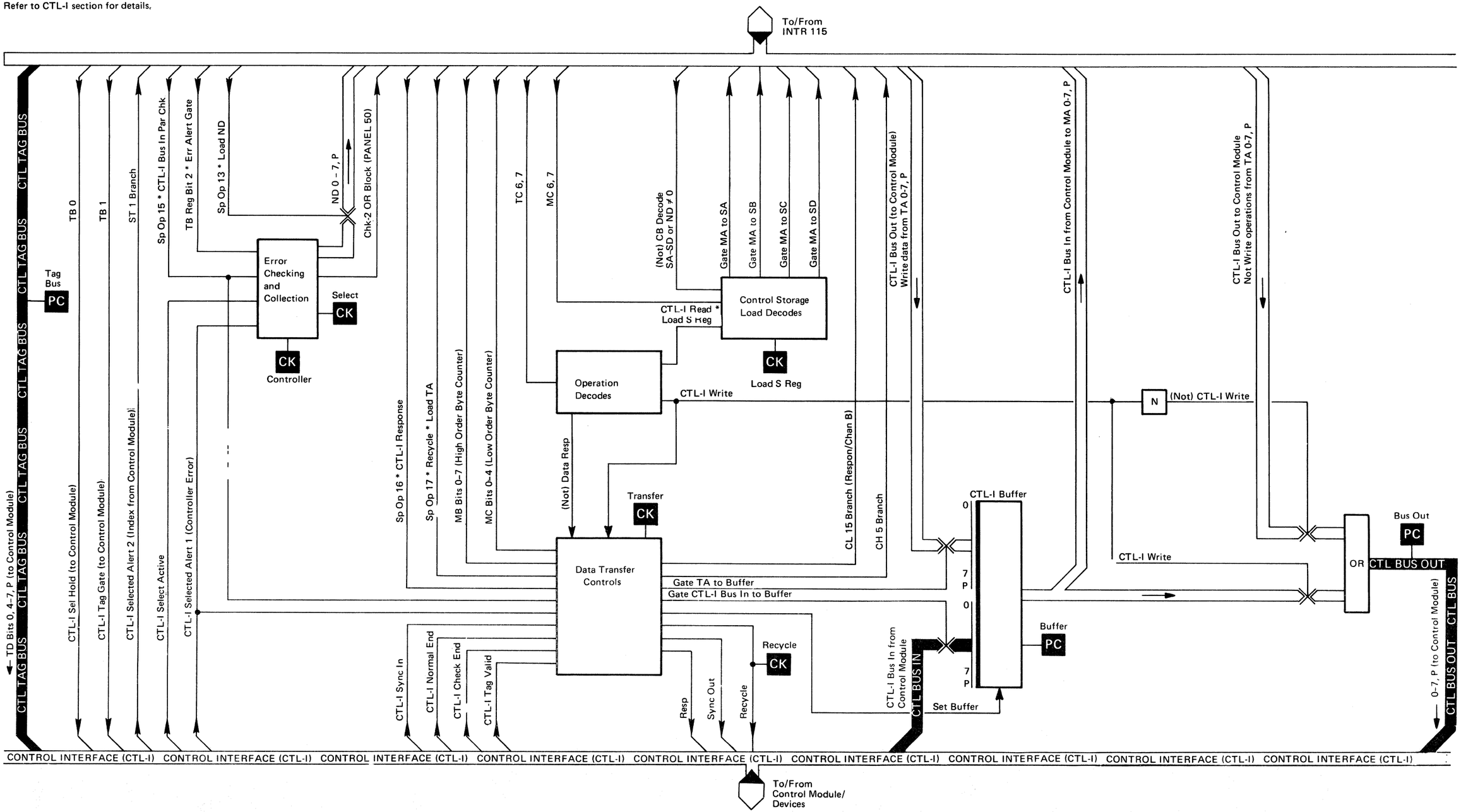
*Two Channel Switch, Additional, only.

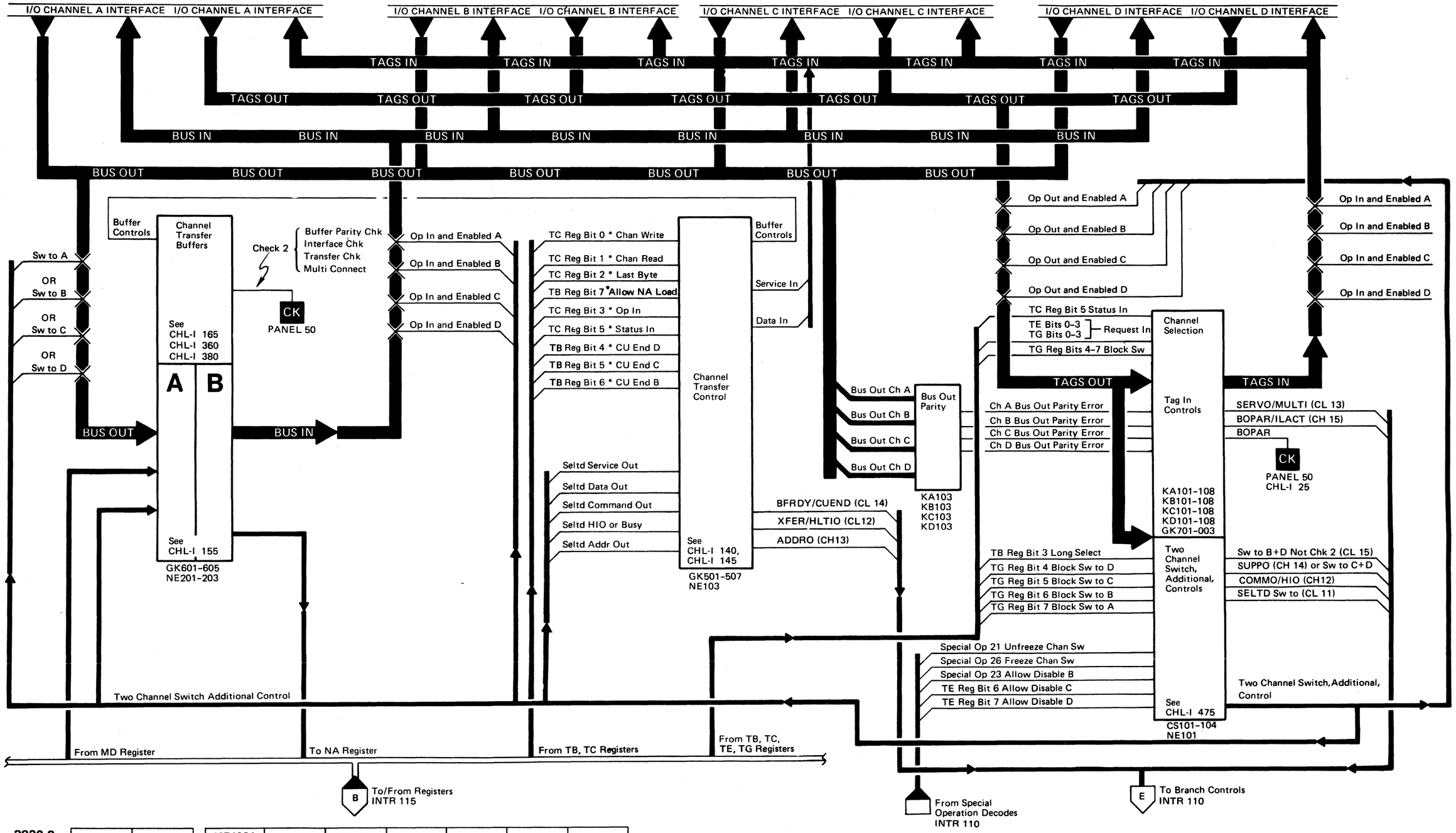
BU0600	2347193
Seq 2 of 2	Part No. (8)

437402A	437404	437405	437408	437414	447460	
15 Mar 72	23 Jun 72	15 Aug 72	16 Oct 72	4 Jun 73	19 Dec 75	

CONTROL INTERFACE (CTL-I)

Refer to CTL-I section for details.





3830-2	BU0700 Seq 2 of 2	2347194 Part Number	437402A 15 Mar 72	437404 23 Jun 72	437405 15 Aug 72	437414 4 Jun 73			

PREFACE TO CMD SECTION

The CMD section describes operations that are controlled by the functional microcode. Although the diagrams combine information pertaining to the 3330 attachment, 3340 attachment, 3340/3340-B2 attachment, 3330/3340 Intermix, and 3330/3340/3350 Intermix, only one of these features and its related microcode will be supplied on the SCU.

The diagrams also combine versions of the microcode pertaining to the various special features available for the SCU and device strings. These features, which may or may not be installed, include the following:

Two Channel Switch
Two Channel Switch, Additional
32 Drive Expansion (provision for four device strings per CU path)
String Switch (provision for two SCUs per device string; always included in 3340 SCU microcode)

Refer to MIC section for microblock and instruction format information.

CONTENTS

CMD

COMMAND SUMMARY

The charts and flowcharts in this section summarize the Storage Control Unit (SCU) commands used by the facility. They describe what the commands do and how they are controlled by the SCU.

CONTROL COMMANDS

Control commands are used to start operations not involving data recorded (or to be recorded) on the pack. These operations include positioning the access mechanism and selecting the head.

For most control functions, the entire operation is specified by the command code. If the command code does not specify the entire control function, the data address field of the CCW designates a main storage location containing the additional information.

SENSE COMMANDS

Two sense commands -- Sense I/O, and Read and Reset Buffered Log -- transfer sense bytes of usage/error log information from the facility to the using system.

Sense I/O Type transfers device type information to the using system.

Test I/O, which is a programmed instruction and not a channel command word (CCW), causes the status byte to be sent to the channel in the initial selection sequence.

READ COMMANDS

Read commands transfer information from the subsystem to main storage of the using system. On all Read commands, the device checks (by means of correction code bytes) the validity of each area of a record as the record is read from a track. A parity bit is added to each byte as it is sent to the channel. All Read commands can operate on overflow records and, except for Read IPL, Read Sector and Read Multiple Count Key Data (CKD), can operate in multitrack mode.

WRITE COMMANDS

Write commands transfer data from main storage to the device for recording on the disk pack. While writing data on the disk pack, the device appends the appropriate correction code bytes to each count, key, and data field as they are written.

Write commands can be grouped into: (1) format Write commands, used to establish records, and (2) nonformat Write commands, used to update previously written records.

SEARCH COMMANDS

Search commands transfer a specific number of bytes from main storage to the SCU. The SCU compares these bytes with data read from a track record. When the condition specified in the search command is satisfied, the status modifier bit is set. The status bytes hold the condition of the status modifier bit until that bit is reset.

Command Summary

Type	Command Name	Hex Code: Single Track	Hex Code: Multi-Track	Page: Command Objective	Page: Command Flowchart	Page: Command Example	Page: Command Description
Control	No Operation	03	–	CMD 16	CMD 25	–	
	Seek	07	–	CMD 15	CMD 20	–	
	Seek Cylinder	0B	–	CMD 15	CMD 20	CMD 35	
	Seek Head	1B	–	CMD 15	CMD 20	–	
	Space Count	0F	–	CMD 16	CMD 30	–	CMD 5
	Recalibrate	13	–	CMD 15	CMD 20	–	
	Restore	17	–	CMD 16	CMD 25	–	
	Set File Mask	1F	–	CMD 15	CMD 20	–	
	Set Sector	23	–	CMD 15	CMD 25	–	
	Diagnostic Load	53	–	CMD 16	CMD 25	–	
	Diagnostic Write	73	–	CMD 16	CMD 30	–	
Sense	Test I/O	00	–	CMD 142	CMD 145	–	CMD 140
	Sense I/O	04	–		CMD 145	–	
	Read and Reset Buffered Log	A4	–		CMD 145	–	
	Read Diagnostic Status 1	44	–		CMD 150	–	
	Device Release	94	–		CMD 150	–	
	Device Reserve	B4	–		CMD 150	–	
	Sense I/O Type*	E4	–		CMD 145	–	
	Unconditional Reserve**	14	–		CMD 150	–	
Read	Read Data	06	86	CMD 107	CMD 120	CMD 130	CMD 100
	Read Key, Data	0E	8E		CMD 120		
	Read Count, Key, Data	1E	9E		CMD 120		
	Read R0	16	96		CMD 110		
	Read Count	12	92		CMD 110		
	Read Home Address	1A	9A		CMD 110		
	Read IPL	02	–		CMD 125		
	Read Sector	22	–		CMD 125		
	Read Multiple Count Key Data*	5E	–		CMD 125		
Write	Write Data	05	–	CMD 77	CMD 85	CMD 90	CMD 70
	Write Key, Data	0D	–		CMD 85		
	Write Count, Key, Data	1D	–		CMD 85		
	Write Spec Count, Key, Data	01	–		CMD 85		
	Write R0	15	–		CMD 80		
	Write Home Address	19	–		CMD 80		
	Erase	11	–		CMD 85		
Search	Search Home Address	39	B9	CMD 55	CMD 55	–	CMD 50
	Search Equal ID	31	B1			–	
	Search High ID	51	D1			–	
	Search High, Equal ID	71	F1			–	
	Search Equal Key	29	A9			–	
	Search High Key	49	C9			–	
	Search High, Equal Key	69	E9			–	

* Supported only in 3330/3340/3350 intermix and 3340/3344 microcode loads.

**Supported only in 3330/3340/3350 intermix microcode loads.

COMMAND	CODE	FUNCTION	DETAIL DESCRIPTION	DATA TRANSFERRED ACROSS CHANNEL	ERROR CONDITIONS				
					ERROR TYPE	COMMAND EXECUTED	SENSE BIT SET	PRESENTED DURING ENDING STATUS	PRESENTED DURING INITIAL STATUS
Seek	07	1. Move the access to the cylinder specified by the seek address. 2. Select the head specified by the seek address.	CMD 20	Six address bytes	Fewer than six address bytes transferred.	No	Command Reject.	Unit Check. Channel End. Device End.	
Seek Cylinder	0B			Six address bytes. For 3330 and 3350 series drives, only the five low-order bits of the sixth byte are used for the seek address. For 3340 series drives, only the four low-order bits of the sixth byte are used.	Address validity.		Command Reject.		
Seek Head	1B	Select the head specified by the seek address			Bus out parity.		Bus Out Parity.		
No Operation	03	No action. Channel End and Device End are presented during initial status.	CMD 25	None					
Recalibrate	13	Move the access to cylinder zero and select head zero	CMD 20						
Restore	17	No action. Zero initial status is followed by final status of Channel End and Device End.	CMD 25						
Set File Mask	1F	Set file mask to indicate permitted Write and Seek commands	CMD 20	One byte of file mask data	More than one Set File Mask command issued in a chain of CCWs	No	Command Reject		Unit Check
Space Count	0F	When chained from a Read, Search, Write, or Space Count command this command locates the start of the next count field (including R0), spaces over the count field, and ends with Channel End and Device End in the gap before the Key field. When not chained, Space Count searches for index, spaces over gap 1, home address, gap 2, and R0 count. End operation in gap following R0 count with Channel End and Device End.	CMD 30	Three bytes used as key length (one byte) and data length (two bytes) for the next command	Index point occurs before an address marker is read.		No Record Found.	Unit Check. Channel End. Device End.	
					Index point sensed while spacing a count area.		Invalid Track Format.		
Set Sector (Feature on 3340 series drives)	23	Used on disconnected command chaining channels to eliminate the need for the channel to maintain connection with the control unit while waiting for the selected record to reach the head.	CMD 25	One byte specifies angular track position (0-127 for 3330 and 3350 series drives, or 0-63 for 3340 series drives)	Angular position specified is greater than 127 (3330 and 3350 series drives) or 63 (3340 series drives) and less than 255	No	Command Reject	Unit Check. Channel End. Device End.	
Diagnostic Load	53	Transfer the specified 512-byte block from the 23FD to the control storage buffer	CMD 25	One byte of control information addresses one sector on the 23FD	Invalid 23FD address	No	Command Reject	Unit Check. Channel End. Device End.	
Diagnostic Write	73	Transfer an inline test from main storage to the CU and executes the test	CMD 30	A maximum of 512 bytes of inline diagnostic microprogram	Fewer than 400 bytes	No	Command Reject	Unit Check. Channel End. Device End.	

DEVICE CONTROL OPERATION

- Moves the heads to a location selected by the using system.

STORAGE CONTROL UNIT | CONTROL MODULE | DEVICE

1 SYSTEM

- Executes Start I/O instruction, which addresses a channel command word (CCW) containing Seek command.

2 CHANNEL

- Executes CCW to transfer the Seek command to the storage control unit (SCU).
- Transfers the seek address data to the control unit.
- Disconnects from control unit until CU signals device end status.

3 CHANNEL CONTROLS

- Control timing of the transfer of data between the channel and CU.
- Check parity of data transferred to the CU.

4 CONTROL CIRCUITS

- Decode the Seek command and control the transfer of seek address information to the CU.
- Calculate difference between present head location and the new address from the system.
- Check status of the module and transfer status to the channel.
- Transfer control and address information to the module.
- Select the addressed module.
- Set up conditions to check for Device End from the module.
- Perform intermediate operations until device status is received.
- Transfer status to the channel when module arrives at the selected track and signal Device End.

6 DEVICE INTERFACE

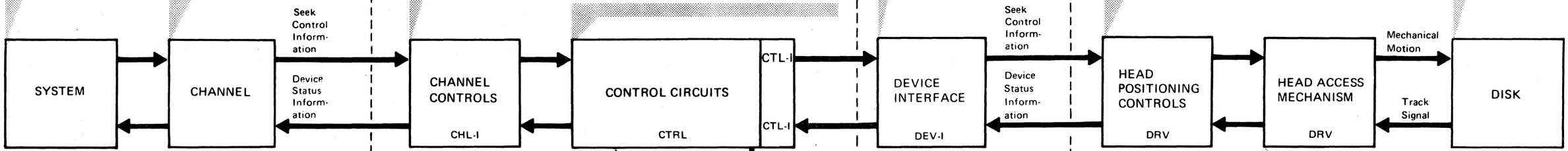
- Transfers control, address, and status information.

7 HEAD POSITIONING CONTROLS AND ADDRESSING

- Control direction and amount of movement of the access mechanism (if required).
- Signal Device End to the CU when new location is reached.
- Maintain head position over the selected track.

9 SERVO DISK

- Provides signal for each track passed from the servo disk.



8 HEAD ACCESS MECHANISM

- Provides mechanical movement of the head assembly.

5 CONTROL INTERFACE

- Tranfers control, address, and status information.
- Selects control module and device.

CONTROL COMMANDS — OBJECTIVES (Part 1 of 2)

SEEK (07)
SEEK CYLINDER (0B)
SEEK HEAD (1B)

Refer to CMD 10 for subsystem components used. Refer to CMD 20 for flowcharts and CAS references.

- Check for valid command.
- No requirement for preceding CCWs.
- Check for Set File Mask limitations. (See CMD 20.)
- If errors occur, present Unit Check, Channel End, and Device End in status. Set command reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer six-byte address from the channel.
  1. If CCW > six, transfer only six bytes.
  2. If CCW < six, do not execute command; present Unit Check, Channel End, and Device End in ending status. Set Command Reject in sense data.
  3. If a Bus Out Parity Error is detected, present Unit Check, Channel End, and Device End in ending status. Set Bus Out Parity in sense data.
- Check address for validity. If invalid, present Unit Check, Channel End, and Device End in ending status. Set Command Reject in sense data.
- Check device status and position.
  1. If not at requested address, control transfer of seek address information to the selected controller/device.
  2. If at requested address, present Channel End and Device End in ending status.
  3. If CTL-I or controller errors (check 2) are detected, present Unit Check, Channel End, and device end in ending status. Set Equipment Check in sense data.
  4. Start access motion and present only Channel End in status to the channel.

Note: *Channel can disconnect while waiting for Seek operation to complete.*

  5. Receive Seek Complete indication from controller/device and present Device End to the channel.
  6. If Seek Incomplete and/or Check 2 occurs:

     3330 and 3350: Do not present Device End to the channel; go into retry mode. (See CMD 210 and Note 1.)

     3340: Present Unit Check, Channel End, and Device End in ending status. Set Equipment Check in sense data.

RECALIBRATE (13)

Refer to CMD 10 for subsystem components used. Refer to CMD 20 for flowcharts and CAS references.

- Check for valid command.
- No requirement for preceding CCWs.
- Check for Set File Mask limitations. (See CMD 20.)
- If errors occur, present Unit Check, Channel End, and Device End in status. Set command reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Send control data across CTL-I to cause the selected controller/device to return the access to cylinder 0 and select head 0.
  1. If CTL-I or controller errors (Check 2) are detected, present Unit Check, Channel End, and Device End in ending status. Set Equipment Check in sense data.
  2. Start access motion and present only Channel End in status to the channel.

Note: *Channel can disconnect while waiting for Seek operation to complete.*

  3. Receive Seek Complete indication from controller/device and present Device End to the channel.
  4. If no Seek Complete occurs or Seek is to an address other than cylinder 0, head 0:

     3330 and 3350: Do not present Device End to the channel; go into retry mode. (See CMD 210 and Note 1.)

     3340: Present Unit Check, Channel End, and Device End in ending status. Set Equipment Check in sense data.

Note 1: *Correct access position is verified on the next Read or Search command to this device. If the access position is incorrect, the control unit suspends the Read or Search command and starts a retry (CMD 210). The control unit performs a Seek to the last seek address for this device. When Seek Complete is received from the device, the control unit continues with the original Read or Search command. This sequence repeats until the correct position is achieved or a retry count of 10 is reached. If retry is unsuccessful, Unit Check, Channel End, and Device End are presented to the channel. Seek Error, with permanent bit on, is set in the sense data.*

SET FILE MASK (1F)

Refer to CMD 10 for subsystem components used. Refer to CMD 20 for flowcharts and CAS references.

- Check for valid command.
- No requirement for preceding CCWs.
- Check for previous SFM in the same chain of commands.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer one byte of data from channel to the control unit. (See CMD 20 and CTRL 650.)
- Check for transfer errors (Check 2).
  1. If a Bus Out Parity Error is detected, present Unit Check, Channel End, and Device End in ending status. Set Bus Out Parity in sense data.
  2. If no error occurs, present Channel End and Device End in ending status.
- Use file mask byte data to control later Write and Seek commands. (See CMD 20.)

SET SECTOR (23)

Refer to CMD 10 for subsystem components used. Refer to CMD 25 for flowcharts and CAS references. Refer to CMD 300 and 305 for descriptions of rotational position sensing.

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer the relative angular track position byte from the channel to the control unit. If a Bus Out Parity Error is detected, present Unit Check, Channel End, and Device End in ending status. Set Bus Out Parity in sense data.
- Check byte for validity: If more than 127 and less than 255 on 3330 and 3350 (or more than 63 and less than 255 on 3340), present Unit check, Channel End, and Device End in ending status. Set command reject in sense data. If the RPS feature is not installed on the 3340, present Channel End and Device End in ending status. A No Operation command is performed, and track orientation is lost.
- If byte is 255, present Channel End and Device End to the channel. Track orientation (see CMD 430) is reset.
- Present Channel End to the channel. The channel should indicate chaining and disconnect.
- If byte is zero, transfer control information to the controller/device to cause reselection of the channel (by request in line) before index point.
- If byte is 1 to 127 for 3330 (63 for 3340), adjust the sector number to compensate for channel reconnection delay. Also, transfer control information to the controller/device to cause reselection before the requested sector.
- If reselection is not accepted by the channel, Request In is dropped and is raised again on the next revolution.
- If Check 2 is indicated in CTL-I or controller/device, present Unit Check and Device End in ending status. Set Equipment Check in sense data.
- If operation is completed correctly, present Device End in ending status.

CONTROL COMMANDS — OBJECTIVES (Part 2 of 2)

RESTORE (17)

Refer to CMD 10 for subsystem components used.
Refer to CMD 25 for flowcharts and CAS references.

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- A No Op is performed.
- Present Channel End and Device End in ending status.

NO OPERATION (03)

Refer to CMD 10 for subsystem components used. Refer to CMD 25 for flowcharts and CAS references.

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If errors occur, present Channel End and Device End in initial status.
- Reset track orientation. (See CMD 430.)
- May cause records or parts of records to be skipped.

DIAGNOSTIC LOAD (53)

Refer to CMD 10 for subsystem components used. Refer to CMD 25 for flowcharts and CAS references. Refer to CMD 165 for description of the use of this command.

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer one byte of control data from the channel to the control unit. This byte identifies the 23FD track address and sector for the selected diagnostic test. If a Bus Out Parity Error is detected, present Unit Check, Channel End, and Device End in ending status. Set Bus Out Parity in sense data.
- Control movement of 23FD head to the selected track.
- Control reading of selected test to buffer area of control storage. (See CTRL 650.)
- If MPL errors occur (see MPL 290 and 295), present Unit Check, Channel End, and Device End in ending status. Set Equipment Check in sense data.
- If transfer is correct, present Channel End and Device End in ending status.

DIAGNOSTIC WRITE (73)

Refer to CMD 10 for subsystem components used. Refer to CMD 25 for flowcharts and CAS references. Refer to CMD 160 for description of the use of this command.

- Check for valid command.
- Check SFM (see CMD 20) to see if command is allowed.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject or File Protected in sense data (see SENSE 1 and CTRL 650).
- If no errors occur, return zero status to the channel.
- Transfer a diagnostic test from the system storage to the control unit control storage buffer area. (See CTRL 650.)
  1. If CCW count > 512, transfer only 512 bytes.
  2. If CCW count < 512, transfer count specified but do not execute command; present Unit Check, Channel End, and Device End in ending status. Set Command Reject in sense data.
  3. If a Bus Out Parity Error is detected, present Unit Check, Channel End, and Device End in ending status. Set Bus Out Parity in sense data.
- Initiate the diagnostic test.
- Store 16-byte error code in control storage. (See CTRL 650.)
- Present Channel End and Device End in ending status.

SPACE COUNT (0F)

Refer to CMD 10 for subsystem components used. Refer to CMD 25 for flowcharts and CAS references.

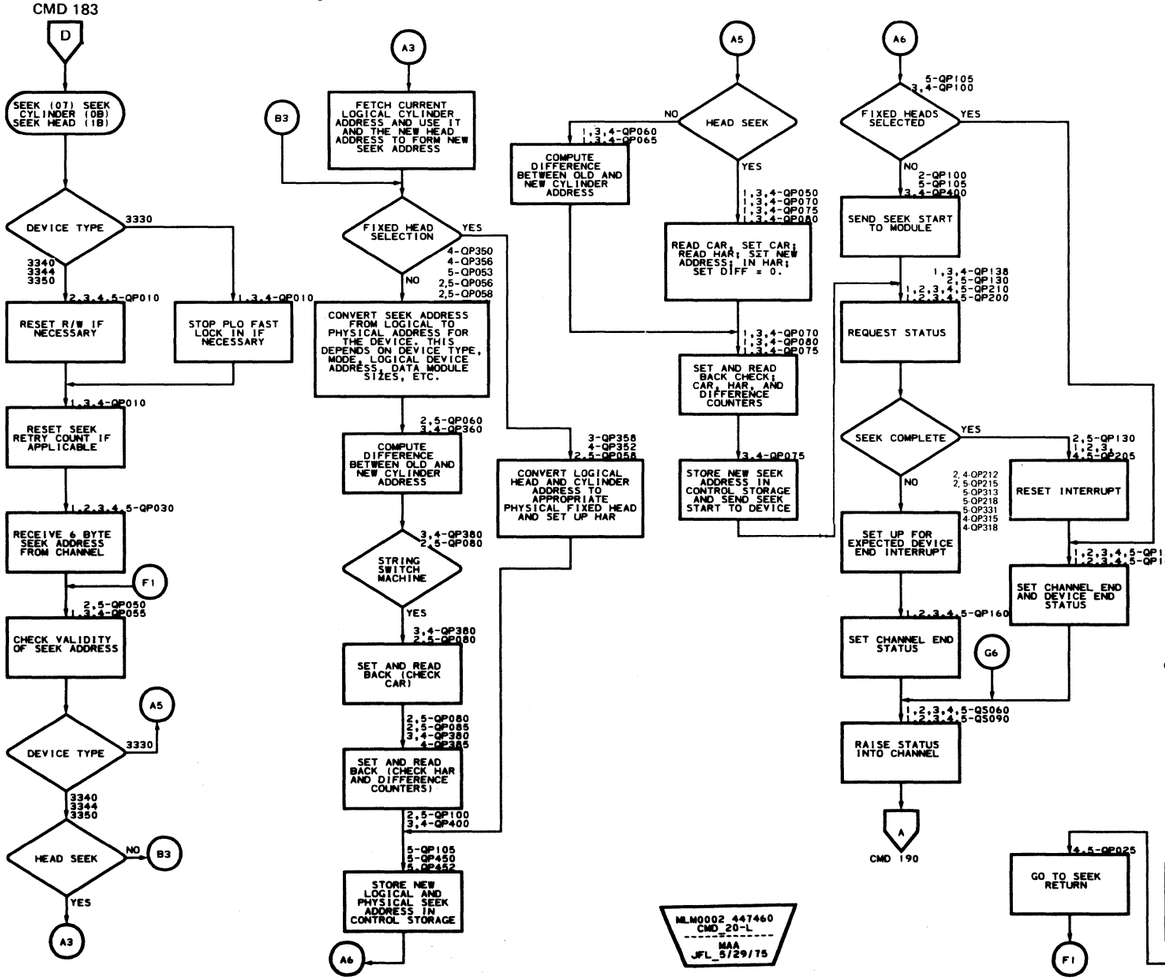
- Check for valid command.
- Present Unit check, Channel End, and Device End in initial status (see SENSE 1 and CTRL 650) under any of the following conditions:
  1. Command is chained from any format Write or Erase command.
  2. Command is chained to any format Write, Erase, or Set File Mask command.
  3. Index is detected before end of the Space Count operation.
- If no errors occur, return zero initial status to the channel.
- Space Count command sequence varies depending on preceding conditions:
  1. If not chained from a Read, Search, Write, or Space Count command;
     a. Wait for index point.
     b. Clock over G1, home address field, and G2.
  2. If chained from a Read, Search, Write, or Space Count command, locate next count field (including R0 count).
  3. Space over count field located and receive three bytes of data (key length, and two bytes of data length) from the channel.

  Note: *If channel sends fewer than three bytes, use zeros for remaining bytes.*

  4. Set end of count field orientation in control storage. (See CMD 430.)
- If check 2 errors occur (from channel interface, CTL-I, or controller/device), present Unit Check, Channel End, and Device End in ending status. Set Equipment Check in sense data.
- If no errors occur, present Channel End and Device End in ending status.

Refer to CMD 15, 16 for command objectives.

Refer to CMD 10 for command operation diagram.



NOTES

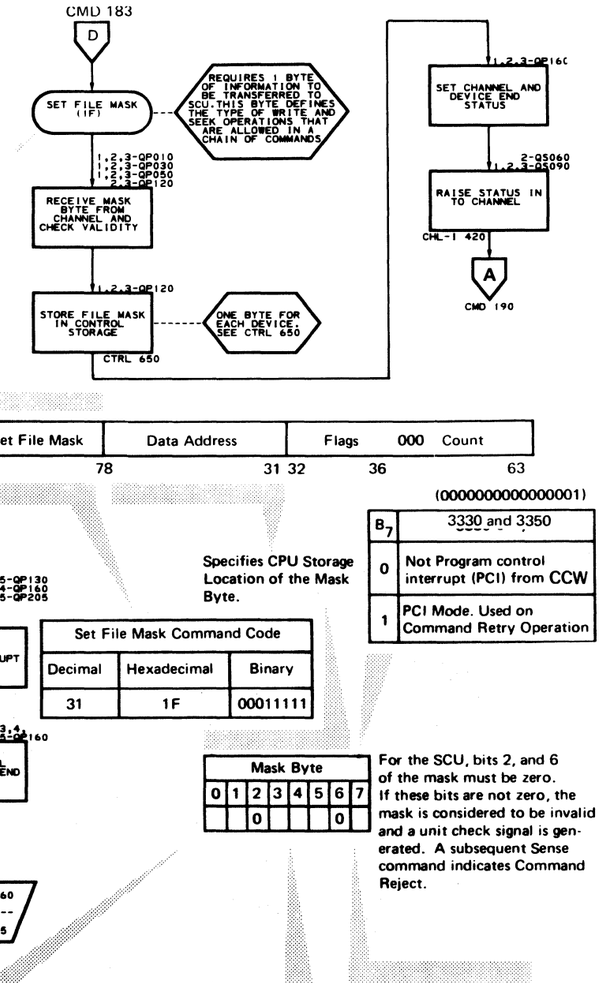
1. THIS FLOWCHART IS USED WITH THE MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:

   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348787, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

ABBREVIATIONS

CAR = CYLINDER ADDRESS REGISTER
DE = DEVICE END
DIFF = DIFFERENCE
HAR = HEAD ADDRESS REGISTER
PLO = PHASE-LOCKED OSCILLATOR

4. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.



CCW	Set File Mask	Data Address	Flags	000	Count
0	78	31 32	36		63

(0000000000000001)

Specifies CPU Storage Location of the Mask Byte.

B_7	3330 and 3350
0	Not Program control interrupt (PCI) from CCW
1	PCI Mode. Used on Command Retry Operation

Set File Mask Command Code		
Decimal	Hexadecimal	Binary
31	1F	00011111

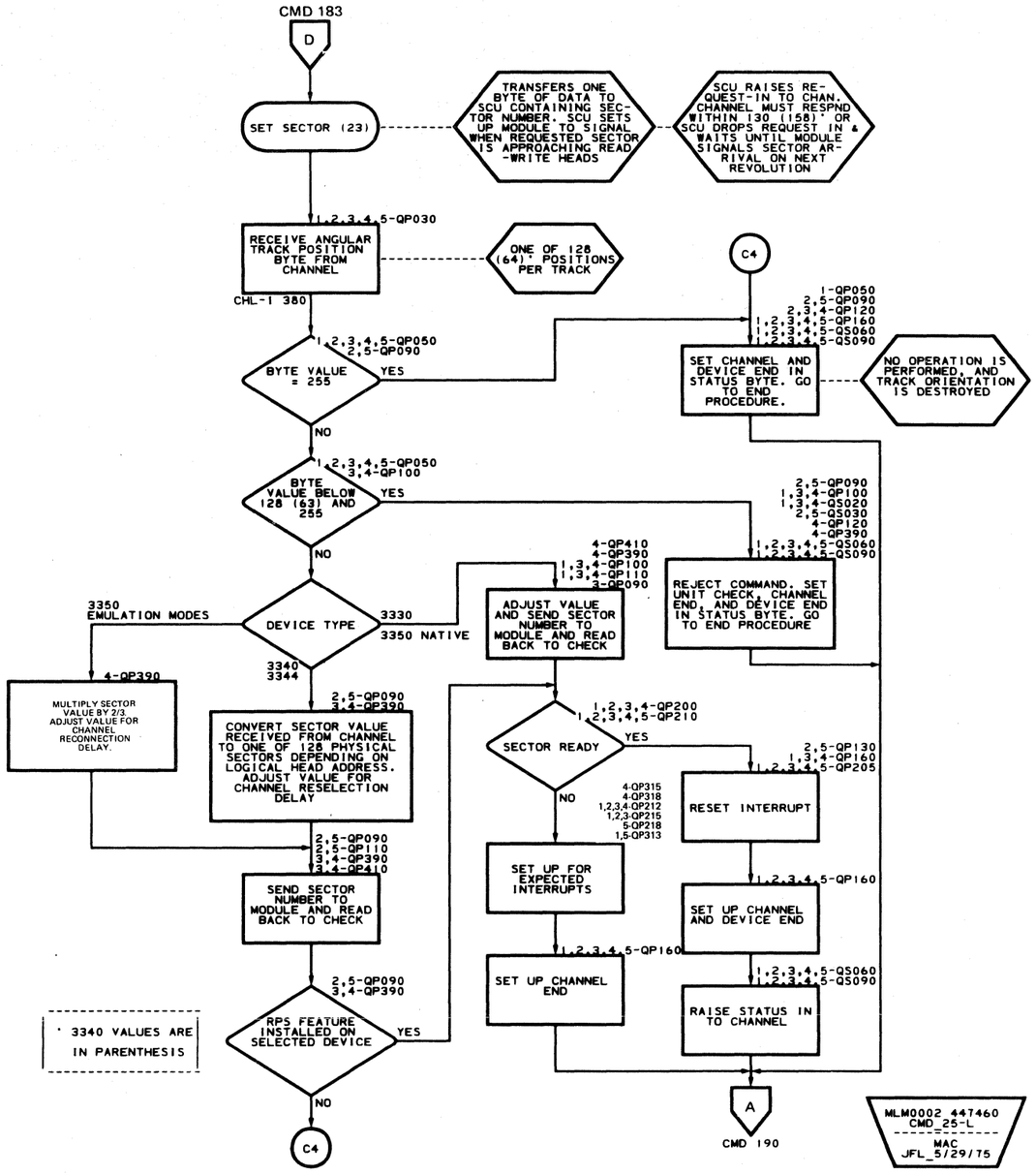
Mask Byte							
0	1	2	3	4	5	6	7
		0				0	

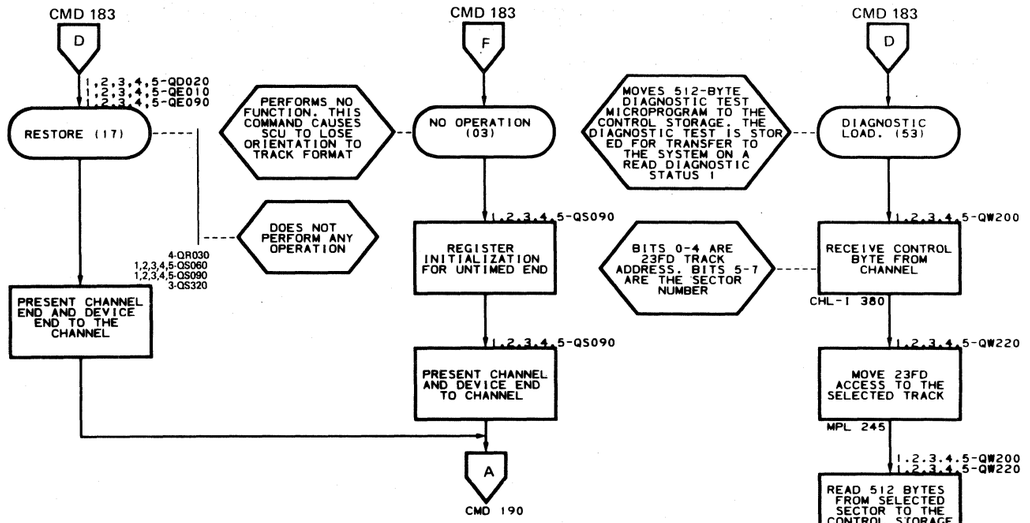
For the SCU, bits 2, and 6 of the mask must be zero. If these bits are not zero, the mask is considered to be invalid and a unit check signal is generated. A subsequent Sense command indicates Command Reject.

B_0	B_1	Permit Write Commands
0	0	All except Write Home Address and Write Record R_0
0	1	None
1	0	Write Data or Write Key & Data
1	1	All

B_3	B_4	Permit Seek Commands
0	0	All
0	1	Seek Cylinder or Seek Head
1	0	Seek Head
1	1	None (also no head switching)

B_5	
0	Inhibit Diagnostic Write command and 3340/3350 seeks to CE track
1	Permit Diagnostic Write command and 3340/3350 seeks to CE tracks only





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   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168881
   5 - 3340/3344 - P/N 4168816

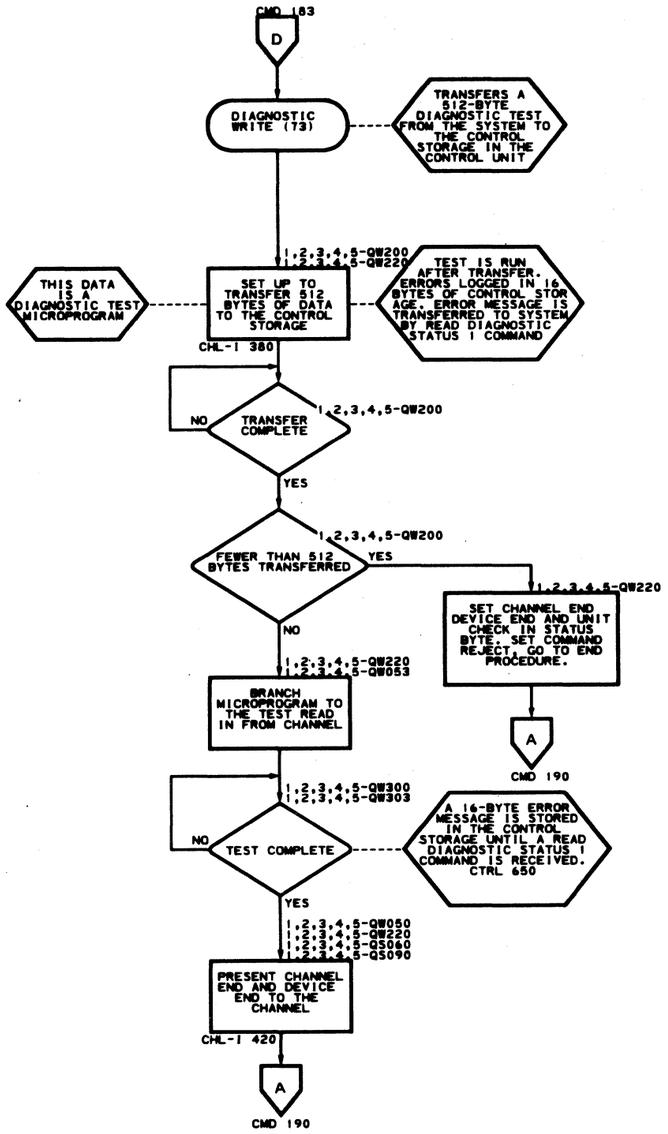
2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

ABBREVIATIONS

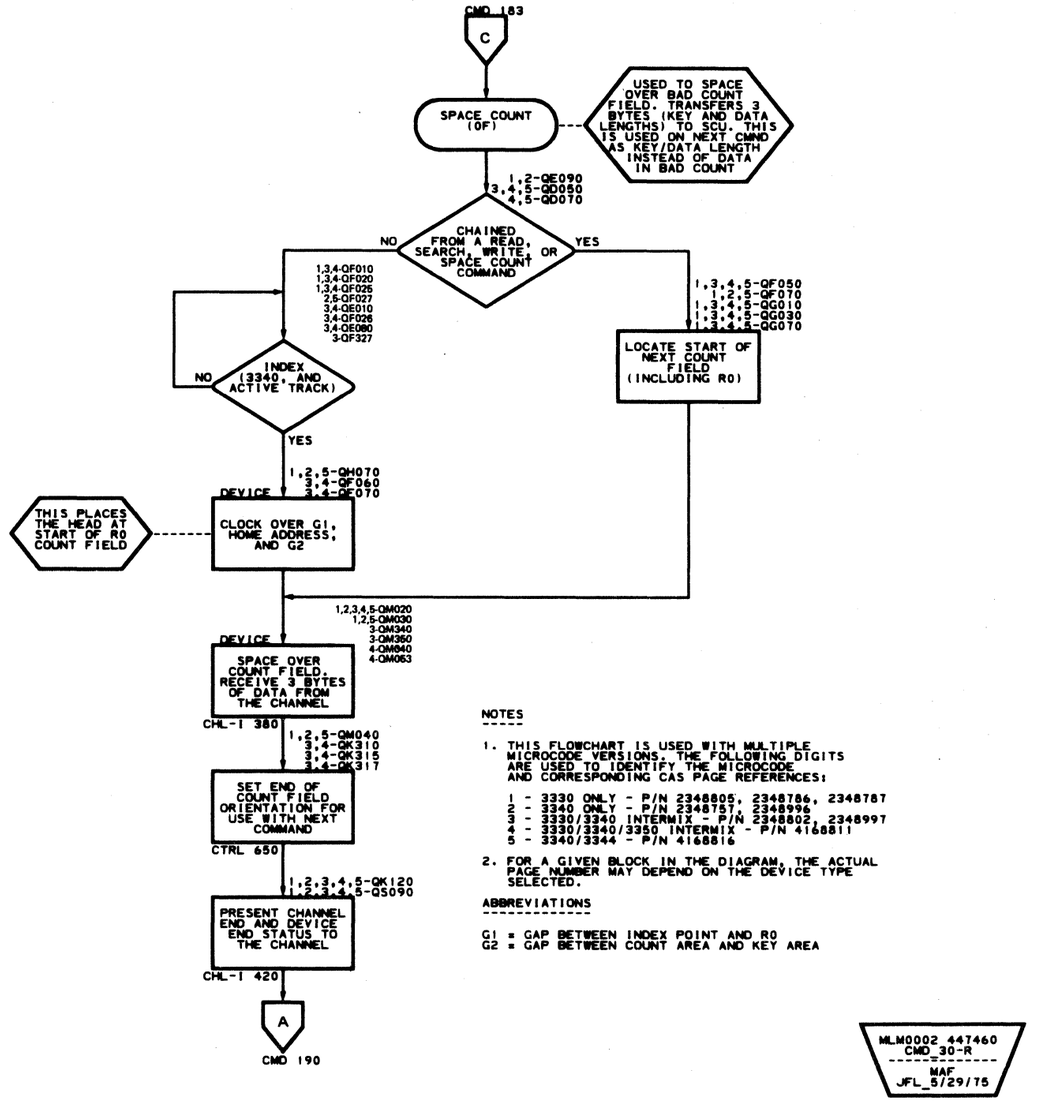
RPS = ROTATIONAL POSITION SENSING

MLM0002 447460
CMD_25-R
MAD
JFL_5/29/75

CONTROL COMMANDS–FLOWCHARTS (Part 3 of 3)



MLM0002 447460
CMD 30-L
MAE
JFL 5/29/75



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   5 - 3340/3344 - P/N 4168816

2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

ABBREVIATIONS

G1 = GAP BETWEEN INDEX POINT AND R0
G2 = GAP BETWEEN COUNT AREA AND KEY AREA

MLM0002 447460
CMD 30-R
MAF
JFL 5/29/75

3830-2/CONTROL INTERFACE OPERATION

- Transfer control information to the drives.
- Transfer address information to the drives.
- Transfer status information to the control unit.
- Transfer diagnostic information to the control unit.

Assume: Initial selection complete

Cylinder Seek Example

0 Transfer low order cylinder address to cylinder address register (CAR).

1 Transfer high-order cylinder address bit, reverse bit, and head address to head address register (HAR).

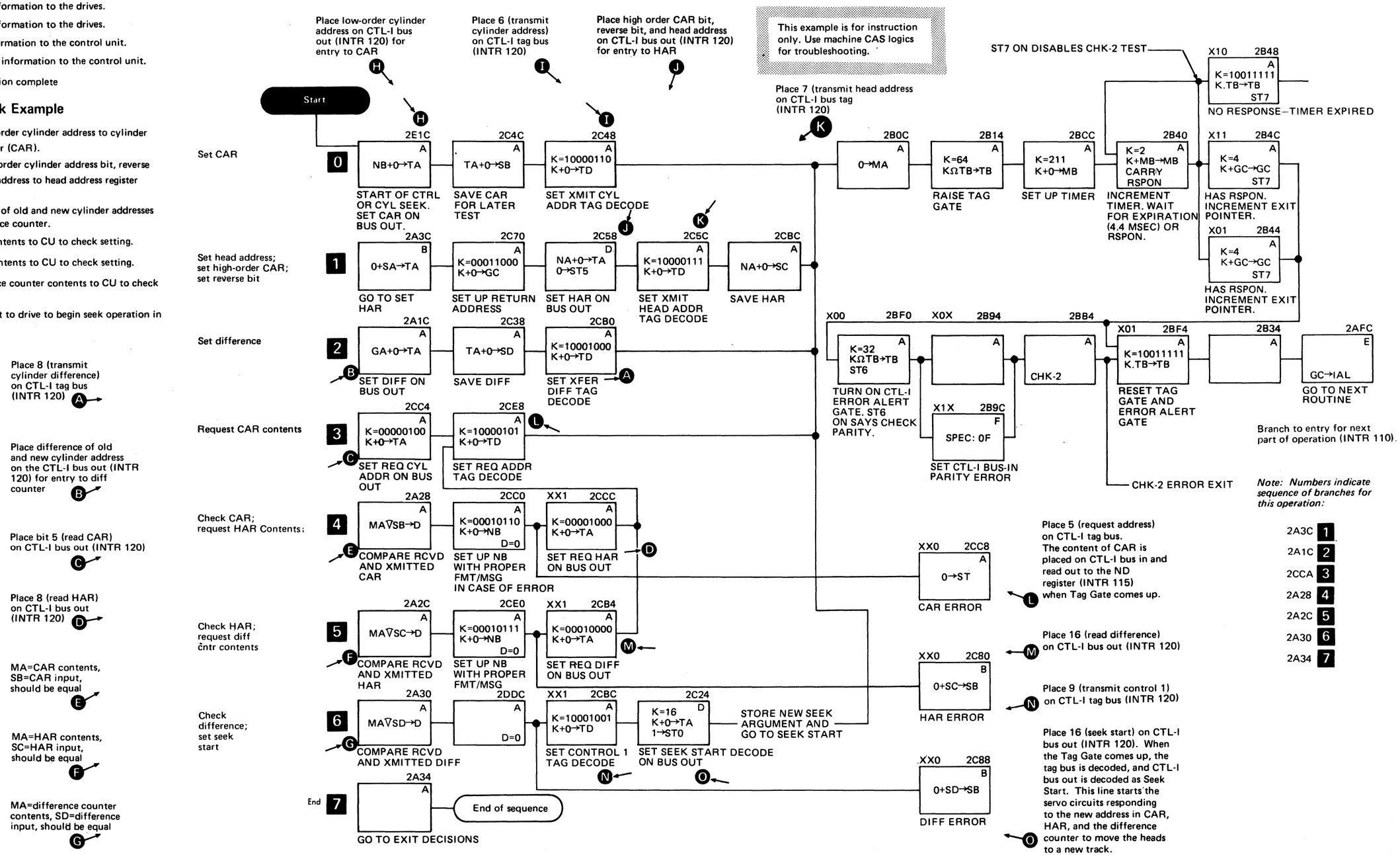
2 Set difference of old and new cylinder addresses in the difference counter.

3 Read CAR contents to CU to check setting.

4 Read HAR contents to CU to check setting.

5 Read difference counter contents to CU to check setting.

6 Send seek start to drive to begin seek operation in the drive.



SEARCH COMMANDS–DESCRIPTIONS

- Status byte bit 1, modifier, is set when a search is successful.
- If a Search command is unsuccessful, the search command must be reissued to continue the search.
- Multi-Track bit not on–search until successful or index is passed twice.
- Multi-Track bit on–head switches to the next track at index.

COMMAND	CODE		FUNCTION	DETAIL DESCRIPTION	DATA COMPARED	ERRORS	COMMENTS
	Single Track	Multi-Track				Set Unit Check, Channel End, Device End	
Search Home Address Equal	39	B9	Locate a home address field selected by the system	CMD 55	Four bytes (CCHH) of home address field from the selected drive and track, with CCHH from the system	Command Reject. Bus Out Parity. Overrun. End of Cylinder. No Record Found. Data Check.	
Search ID Equal	31	B1	Locate a count field selected by the system	CMD 55	Five bytes (CCHHR) of the next count field from the selected drive and track, with CCHHR from the system		
Search ID High	51	D1	Locate a count field selected by the system	CMD 55	Five bytes (CCHHR) of the next count field from the selected drive and track, with CCHHR from the system		Locates any ID from the track that is higher than the ID from the system
Search ID Equal or High	71	F1	Locate a count field selected by the system	CMD 55	Five bytes (CCHHR) of the next count field from the selected drive and track, with CCHHR from the system		Locates the ID from the track that is equal to, or any ID that is higher, than the ID from the system.
Search Key Equal	29	A9	Locate a key field selected by the system	CMD 55	The key field bytes from the selected drive and track, with key from the system		The key field compared is key field of the next record (excluding R0), unless chained from a Read Count or Search ID command. If chained from a count operation the key field searched is in the same record.
Search Key High	49	C9	Locate a key field selected by the system	CMD 55	The key field bytes from the selected drive and track, with key from the system		Same as Search Key Equal, except the key field located is any key field on the track that is higher than the key from the system
Search Key Equal or High	69	E9	Locate a key field selected by the system	CMD 55	The key field bytes from the selected drive and track, with key from the system		Same as Search Key Equal, except the key field located is equal to or higher than the key from the system.

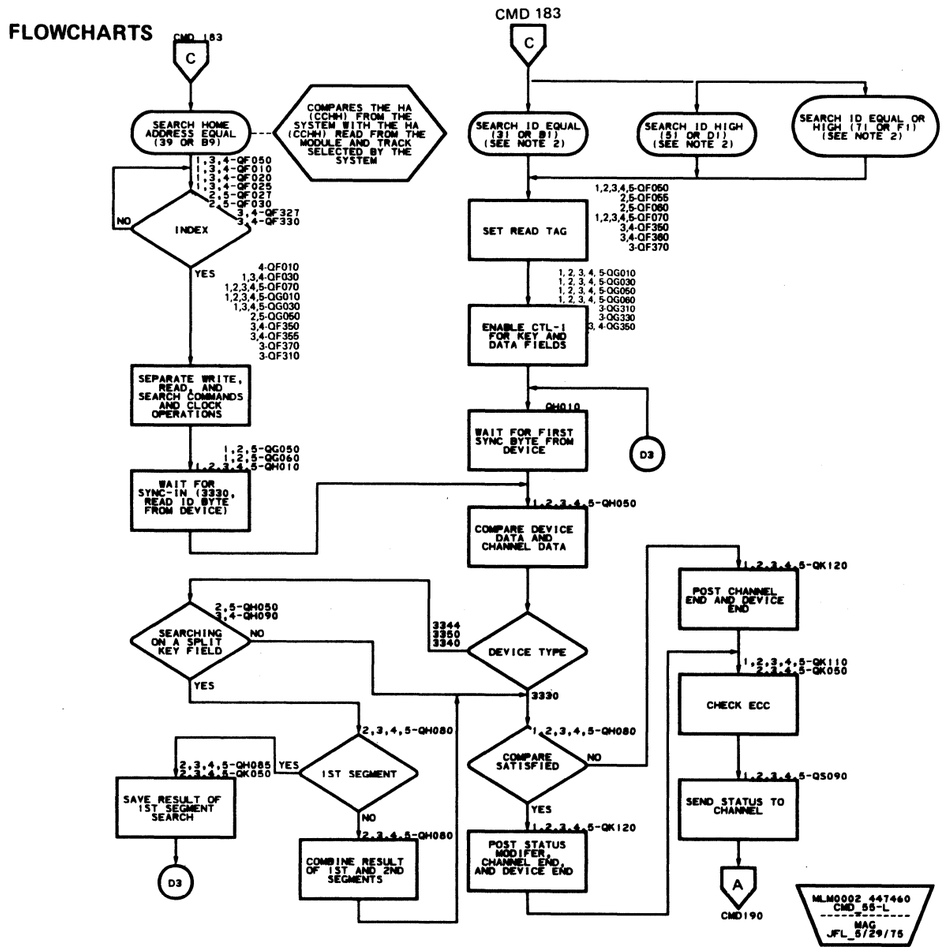
OBJECTIVES

SEARCH HOME ADDRESS EQUAL (39 or B9)
SEARCH ID EQUAL (31 or B1)
SEARCH ID HIGH (51 or D1)
SEARCH ID EQUAL OR HIGH (71 or F1)
SEARCH KEY EQUAL (29 or A9)
SEARCH KEY HIGH (49 or C9)
SEARCH KEY EQUAL OR HIGH (69 or E9)

Refer to CMD 75, CMD 90, CMD 105, and CMD 130 for subsystem components used (channel in write mode, CTL-I read mode).

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer number of bytes called for by the command (HA=4, ID=5, key=0 to 256) from the channel to the control unit. Read the same number of bytes from the selected controller/ device.
- Byte by byte, make comparison called for by the command.
  1. Compare data from device with data from the channel. For example, 5 from the device and 3 from the channel constitute a high condition.
  2. If the CCW count is less than the field length, comparison is on the CCW count bytes only.
  3. The first unequal condition (high or low) encountered sets the condition for the field.
  4. If search condition is satisfied, set status modifier bit in the status byte.
  5. If CCW count is less than field length, read balance of field to check for errors.
- If errors from channel interface, CTL-I, or controller/ device are found, present Unit Check, Channel End, and Device End in ending status. 3330 only: go to retry mode (see CMD 210); set appropriate bits in sense data.
- If no errors are found and:
  1. Search condition is satisfied, present Status Modifier, Channel End, and Device End in ending status. Channel program should skip the next CCW (TIC*-8) and execute the following CCW.
  2. Search condition is not satisfied, present Channel End and device end in ending status. Channel program should execute the next CCW (TIC*-8) and branch back to repeat the Search command.

FLOWCHARTS



- If multitrack bit is off in the command, the search loop continues until satisfied or until two index points have been sensed. If two indexes are sensed first, present Unit Check, Channel End, and Device End in ending status. Set No Record Found indication in sense data.
- If multitrack bit is on in the command, the search loop continues until satisfied or until index is sensed. If index is sensed first, the head address is stepped +1 and the loop continues. If the head address is advanced past the last track in a cylinder, present Unit Check, Channel End, and Device End in ending status. Set End of Cylinder indication in the sense data.

NOTES

1. THIS FLOWCHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:
   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348757, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816
2. COMPARE THE ID (CCHHR) FROM THE SYSTEM WITH THE ID (CCHHR) READ FROM THE MODULE AND TRACK SELECTED BY THE SYSTEM. ON A SEARCH ID HIGH COMMAND, THE SEARCH IS SATISFIED ON ANY RECORD WHERE THE ID FROM THE MODULE IS HIGHER THAN THE DATA FROM THE SYSTEM.
3. COMPARE THE KEY FROM THE SYSTEM WITH THE KEY FROM THE MODULE AND TRACK SELECTED BY THE SYSTEM. ON A SEARCH KEY HIGH COMMAND THE SEARCH IS SATISFIED ON ANY RECORD WHERE THE KEY FROM THE MODULE IS HIGHER THAN THE DATA FROM THE SYSTEM.
4. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

ABBREVIATIONS

CTL-I = CONTROL INTERFACE
DL = DATA LENGTH
ECC = ERROR CORRECTION CODE
ID = IDENTIFIER
KL = KEY LENGTH

WRITE COMMANDS–DESCRIPTIONS

COMMAND	CODE		FUNCTION	DETAIL DESCRIPTION	DATA WRITTEN	ERROR	COMMENTS
	Single Track	Multi-Track				Set Unit Check-Channel and Device End	
Write Count, Key, Data	1D	–	Write one complete record on the selected drive and track	CMD 85	Count, key, and data fields of next record on the track. Data for the fields comes from the system. The count field flag byte, ECC, and gap data come from the SCU.	Command Reject. Bus Out Parity. Overrun. Invalid Track Format.	If file mask is violated, set Command Reject. Must be chained from Write R0; Write Count, Key, Data; Erase; or a successful Search Equal ID or Search Equal Key command. After last Count, Key, Data command on a track, write 0's to index.
Write Special Count, Key, Data	01	–	Same as Write Count, Key, Data command except a 1 is written in bit 4 of the flag byte to indicate a record overflow segment	CMD 85	Same as that of Write Count, Key, Data command		Same as Write Count, Key, Data. Not used for last segment of an overflow record.
Erase	11	–	Erase remainder of track	CMD 85	Zeros		The CU skips writing an address marker, sync byte, or ECC.
Write Home Address (HA)	19	–	3330 and 3350 Compatibility Modes*: Write the five-byte (FCCHH) home address field on the selected drive and track. 3340: Write the seven-byte (SD SD F CC HH) home address field on the selected drive and track. 3350–Native Mode: Write the 9-byte home address field (SD SD SD SD F C C H H) on the selected drive and track.	CMD 80	3330 and 3350 Compatibility Modes*: Five-byte (FCCHH) home address field transferred from the system. 3340: Seven-byte (SD SD F CC HH) home address field transferred from the system. 3350–Native Mode: Nine-byte (SD SD SD SD F C C H H) home address field transferred from the system.	(Format Write commands)	3340 and 3350–Native Mode: Must be chained from a satisfied Search Home Address command (with a CCW count of 4 or more). If not, bit 6 of the flag byte must be set to 1 to indicate a defective track. If it is not, the command is rejected.
Write Record (R0)	15	–	Write count, key, data of R0.	CMD 80	Flag byte from HA field. $CCHHRK_LD_LD_L$ from system written in count field. Key and data from system.		Same as Write Count, Key, Data except must be chained from a write HA or a successful Search HA Equal command
Write Data	05	–	Change the data field of a record	CMD 85	Data from the system. Write the number of bytes specified by the D_LD_L bytes of the count field of the same record.	Command Reject. Bus Out Parity. Overrun.	If file mask is violated, set Command Reject. Must be chained from a successful Search Equal ID or Search Equal Key command.
Write Key-Data	0D	–	Change the key and data fields of a record	CMD 85	Data from the system. Write the number of bytes specified by the K_L and D_LD_L bytes of the count field of the same record.		If file mask is violated, set Command Reject. Must be chained from a successful Search Equal ID command. If K_L = 0, operation is the same as Write Data.

**Note: For 3350 in compatibility modes, the HA is first read internally by the storage control to save the SD bytes. Then the SD bytes, along with the 5 bytes (F C C H H) transferred from the system, are written on the track.*

WRITE OPERATION

Write data from the using system on a pack selected by the system.

1 SYSTEM

- Executes Start I/O instruction, which addresses a channel command word (CCW) containing a Write command.

2 CHANNEL

- Executes the CCW to transfer the write command to the SCU.
- Transfers the address where data is to be stored, to the storage control unit.
- Transfers data from the system to the storage control unit.

STORAGE CONTROL UNIT

3 CHANNEL CONTROLS

- Control timing of transfer of data between the channel and the CU.
- Check parity of data transfered to the CU.

4 CONTROL CIRCUITS

- Decode the Write command.
- Select the addressed module and head.
- Check the status of the module and transfer the status to the channel.
- Set up the write controls in the module.
- Control the byte-by-byte transfer of write data from the channel interface to the controller circuits.
- Checks subsystem for errors.
- Transfers ending status to the channel.
- 3330-Indicate retry status to channel if error is a type that can be retried, and set up to relocate record.
- Control gap types.

5 CONTROL INTERFACE

- Transfers write control information to the control circuits.
- Transfers status of the control circuits and device to the SCU.
- Transfers the byte-by-byte data to the control circuits.

CONTROL MODULE

6 SERDES

- Receives data serial-by-byte from the CU.
- Changes byte of data to serial-by-bit data.
- Sends ECC data to module.
- Sends modified frequency modulation (MFM) data to the module.
- Uses phase-locked oscillator (PLO) pulses to control write timing.
- Controls gap configurations.

7 DEVICE INTERFACE

- Transfers write control information to the control circuits.
- Transfers status of the control circuits and device to the SCU.
- Transfers the byte-by-byte data to the control circuits.

DEVICE

8 WRITE CONTROLS

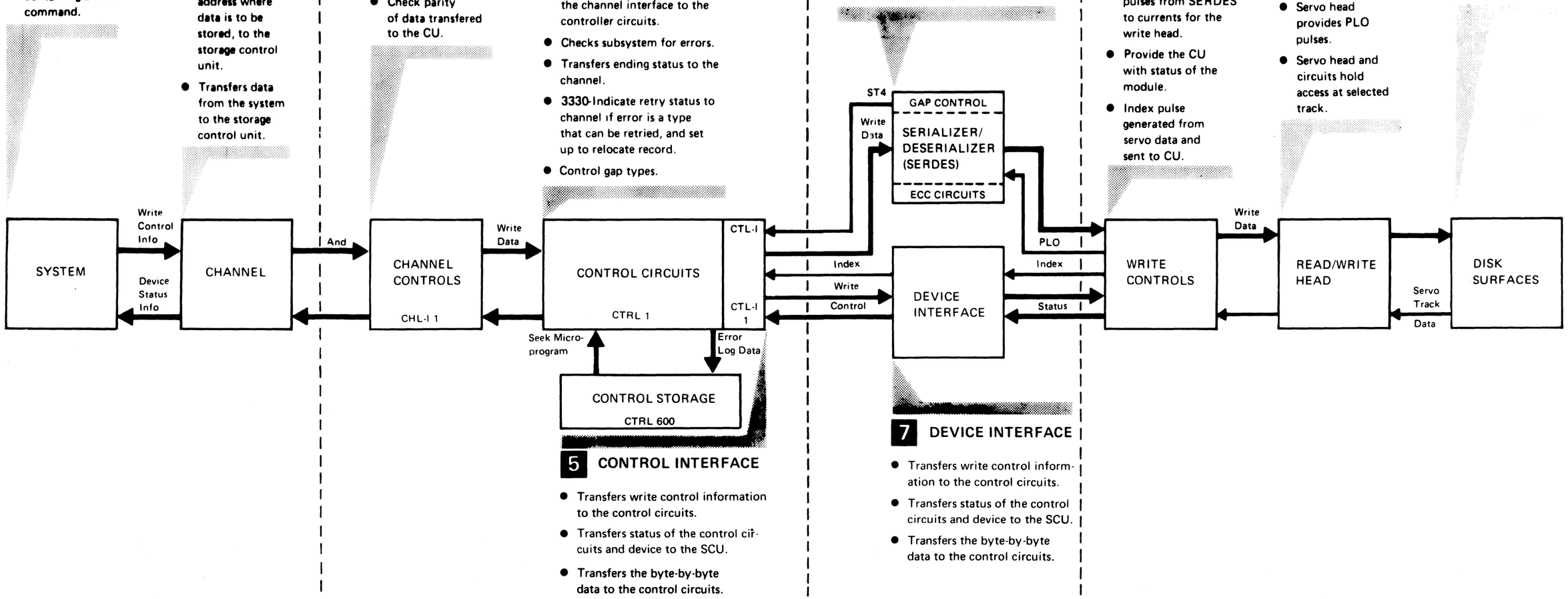
- Set up the module to write on the disk.
- Change data pulses from SERDES to currents for the write head.
- Provide the CU with status of the module.
- Index pulse generated from servo data and sent to CU.

9 READ/WRITE HEAD

- Changes currents in write windings to magnetic flux.
- Selected head accepts data.
- Servo head provides PLO pulses.
- Servo head and circuits hold access at selected track.

10 DISK SURFACES

- Receive and store bits of information on the magnetic coating of the disk.



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437402A 15 Mar 72	437404 23 Jun 72	437405 15 Aug 72	437415 2 Nov 73	437417 15 Apr 74	447460 19 Dec 75	

WRITE COMMANDS — OBJECTIVES

WRITE HOME ADDRESS (19)
WRITE RECORD ZERO (15) } **Format Write**
ERASE (11)
WRITE COUNT KEY DATA (1D) } **Commands**
WRITE SPECIAL COUNT KEY DATA (01)
WRITE KEY DATA (0D)
WRITE DATA (05)

Refer to CMD 75 and CMD 90 for subsystem components used. Refer to CMD 80 and 85 for flowcharts and CAS references.

- Check for valid command.
- Check for chaining prerequisites. These depend on the command:

1. If the command is Write CKD, Write Special CKD, or Erase, it must be chained from one of the following:
   a. Write R0.
   b. Write CKD.
   c. Successful Search Equal ID or Key. (A Read Data or Key Data may be between Search and Write.)
2. If the command is a Write R0, it must be chained from one of the following:
   a. Write HA.
   b. Successful Search HA.
3. If the command is Write Data, it must be chained from a successful Search Equal ID or Key. Furthermore, the search must be on the full field from the disk.
4. If the command is Write Key Data, it must be chained from a successful Search Equal ID (all five bytes).
5. If the command is Write HA (3340 only), it must meet either of the following requirements:
   a. It must be chained from a satisifed Search HA with a CCW count of 4 or more.
   b. Bit 6 of the flag byte, transferred from the channel, must be 1, indicating a defective track.

- Check for Set File Mask limitations. (See CMD 20.)
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Write data, transferred from the channel, on the track selected by the system (plus correction code bytes at end of each field). The commands and their effects are:

1. Write HA: Locate index; write gap and control bytes (called for by the device type), bytes of data from the channel (five for 3330, seven for 3340), and start of following gap. *In 3350 compatibility mode,* SD information is not provided by the system. The storage control internally reads the home address field to obtain the existing SD bytes before the Write HA is executed.
2. Write R0: Start writing in gap before R0 count; write flag byte, count field, gap, key field (if required), gap, data field (if required), and start of next gap.
3. Write CKD and Write Special CKD: Locate gap before next count field; start writing in gap; write count field (flag is same as HA flag byte), gap, key field (if required), and start of next gap.

Note: *In Write Special CKD, set flag byte bit 4 to 1.*

1. Write Key Data: Start writing in gap; write key field (if required) and start of next gap.
2. Write Data: Locate gap before next data field; start writing in gap; write data field (if required) and start of next gap.
3. Erase: Operates as a Write CKD command, except:
   a. The data transferred from the channel is not written on the track; and
   b. Zeros are written in place of the data and to the end of the track.

- Format Write commands change the balance of the track:

1. After last format Write command in a chain, release the channel, write to the next index point, and reconnect after index.
2. Detection of Bus Out Parity Error causes presentation of Unit Check, Channel End, and Device End at end of field.
3. Detection of a data overrun causes presentation of Unit Check, Channel End, and Device End at the normal ending point of the operation, and causes 0s to be written after error is detected.
4. If data overrun is detected, present Unit Check, Channel End, and Device End in ending status. (3330 only: go into retry mode; see CMD 210.)

- If no errors occur, present Channel End and Device End in ending status.
- Nonformat Write commands update existing records.

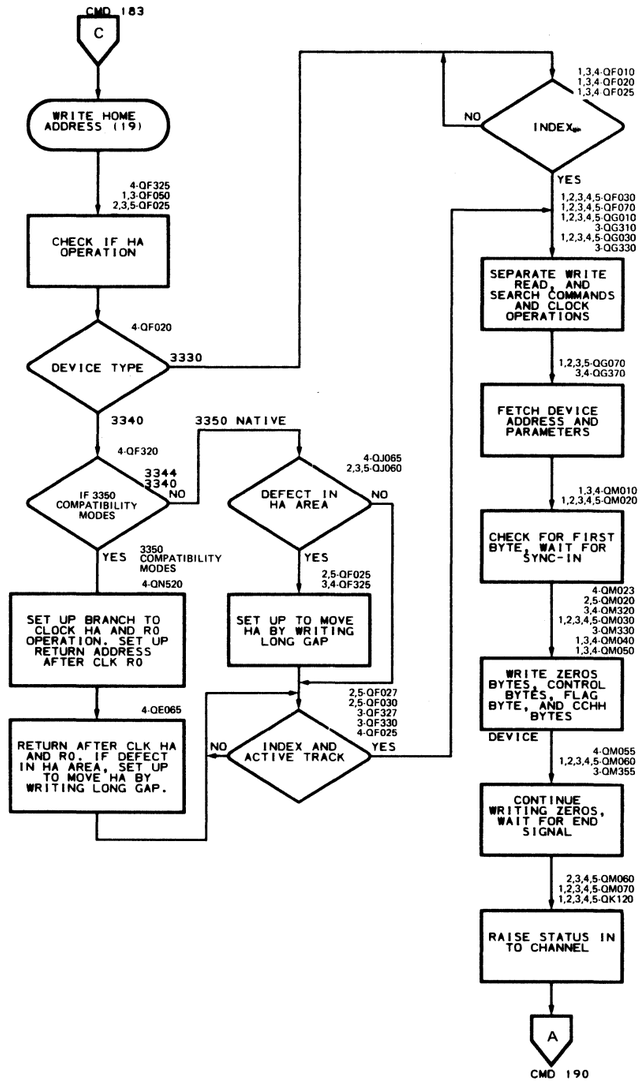
1. These commands change only data or key and data fields.
2. Each new record must be the same size as old record. (If CCW count is small, fill balance of field with 0s.)
3. These commands can be used to update overflow records. (See CMD 400.)

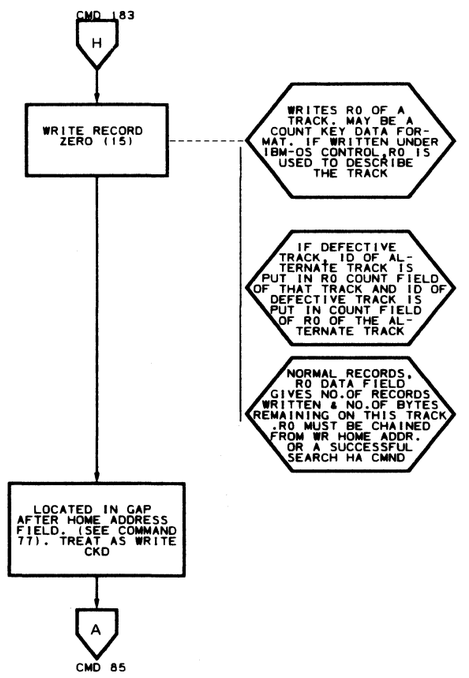
WRITE COMMANDS–FLOWCHARTS (Part 1 of 2)

Refer to CMD 75 for subsystem components used.

Refer to CMD 77 for command objectives.

- Write commands store data from the system on the disk pack of a selected module.
- Format Write commands – Write Home Address, Write R0, Write Count, Key, Data, and Erase – cause the balance of the track to be changed.
- Write Data and Write Key, Data commands change only the key and/or data fields of a record to be changed. (Field length stays the same.)
- Gap configurations may vary with device type; refer to device MLM.





NOTES

1. THIS FLOWCHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:

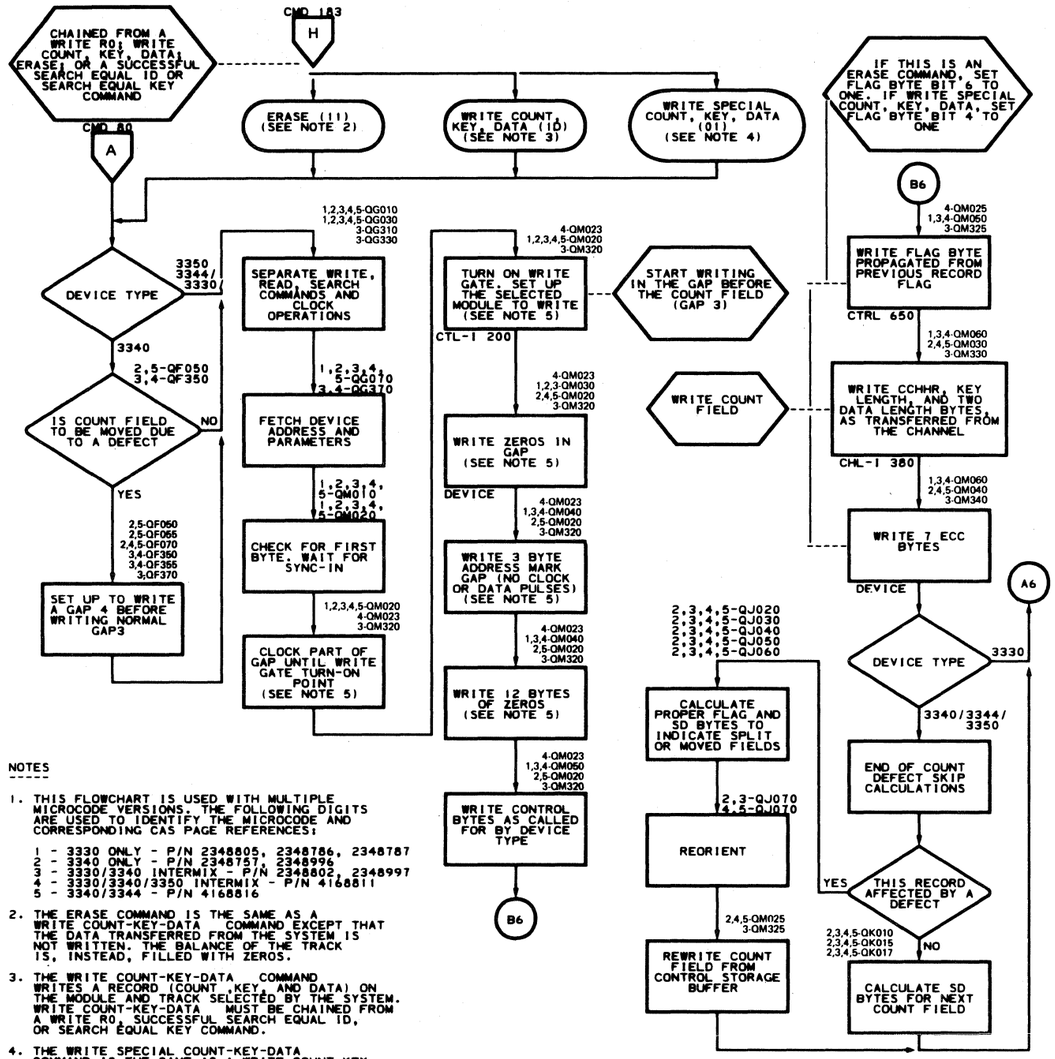
   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348757, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

MLM0002 447460
CMD 80-L
MAI
JFL 5/29/75

MLM0002 447460
CMD 80-R
MAJ
JFL 5/29/75

WRITE COMMANDS–FLOWCHARTS (Part 2 of 2)



NOTES

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   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

2. THE ERASE COMMAND IS THE SAME AS A WRITE COUNT-KEY-DATA COMMAND EXCEPT THAT THE DATA TRANSFERRED FROM THE SYSTEM IS NOT WRITTEN. THE BALANCE OF THE TRACK IS, INSTEAD, FILLED WITH ZEROS.

3. THE WRITE COUNT-KEY-DATA COMMAND WRITES A RECORD (COUNT, KEY AND DATA) ON THE MODULE AND TRACK SELECTED BY THE SYSTEM. WRITE COUNT-KEY-DATA MUST BE CHAINED FROM A WRITE R0, SUCCESSFUL SEARCH EQUAL ID, OR SEARCH EQUAL KEY COMMAND.

4. THE WRITE SPECIAL COUNT-KEY-DATA COMMAND IS THE SAME AS A WRITE COUNT-KEY-DATA COMMAND EXCEPT THAT THE FLAG BYTE BIT 4 IS SET TO 1. THIS INDICATES THAT THIS RECORD IS SEGMENT OF OVERFLOW RECORD. THIS COMMAND IS USED FOR ALL SEGMENTS OF AN OVERFLOW RECORD EXCEPT THE LAST.

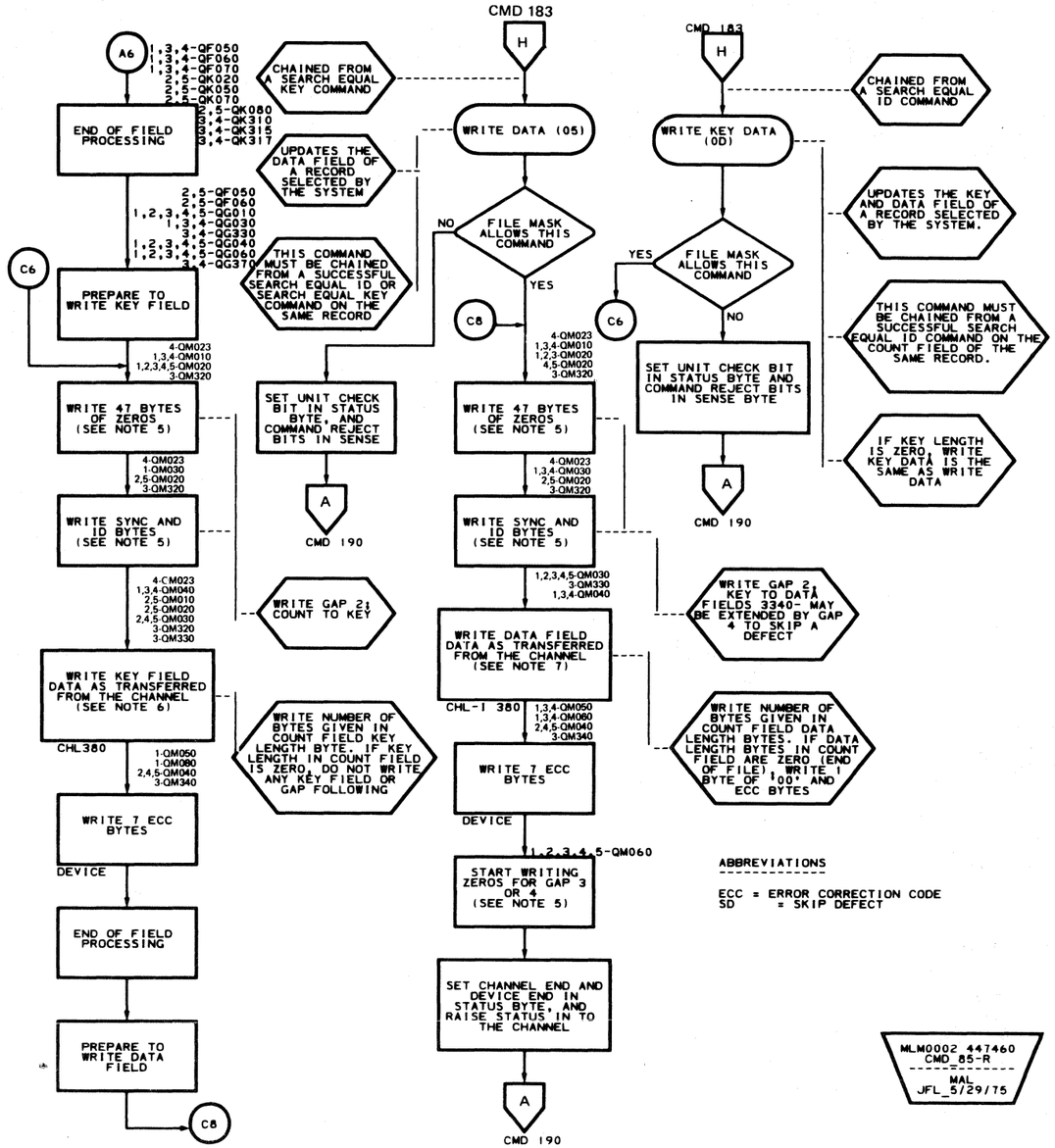
5. 3340: CONTROLLER AUTOMATICALLY SEQUENCES SIGNALS TO THE DRIVE TO TURN ON WRITE GATE, WRITE GAP, ADDRESS MARK, ETC. MICROPROGRAM WAITS FOR REQUEST FOR DATA.

6. 3340: FIELD MAY BE WRITTEN IN TWO SEGMENTS TO SKIP A DEFECT. NO ECC IS WRITTEN AT END OF FIRST SEGMENT.

7. 3340: FIELD MAY BE SPLIT INTO TWO SEGMENTS TO SKIP A DEFECT.

8. FOR A GIVEN BLOCK IN THE DIAGRA, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

MLM0002 447460
CMD_85-L
MAK
JFL_5/29/75



ABBREVIATIONS

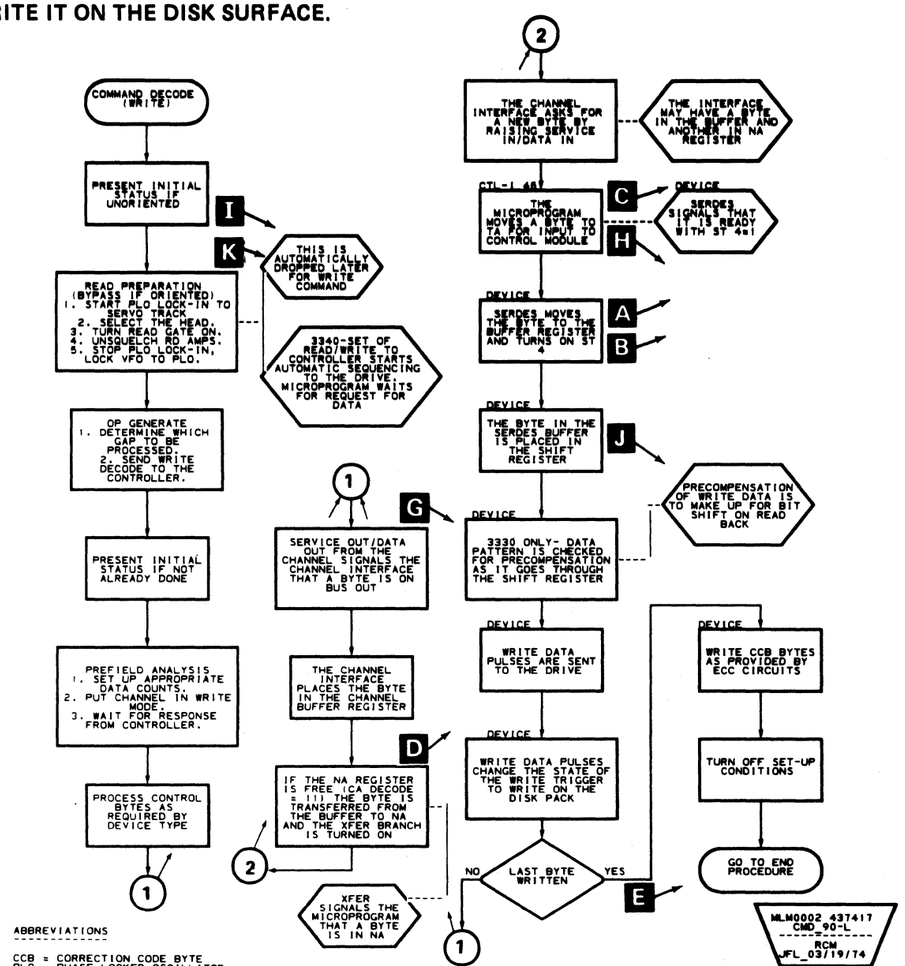
ECC = ERROR CORRECTION CODE
SD = SKIP DEFECT

MLM0002 447460
CMD_85-R
MAL
JFL_5/29/75

3830-2	BX0900 Seq 2 of 2	2347202 Part No. (8)	See EC History	447460 19 Dec 75	447461 12 Mar 76				

WRITE DATA TRANSFER

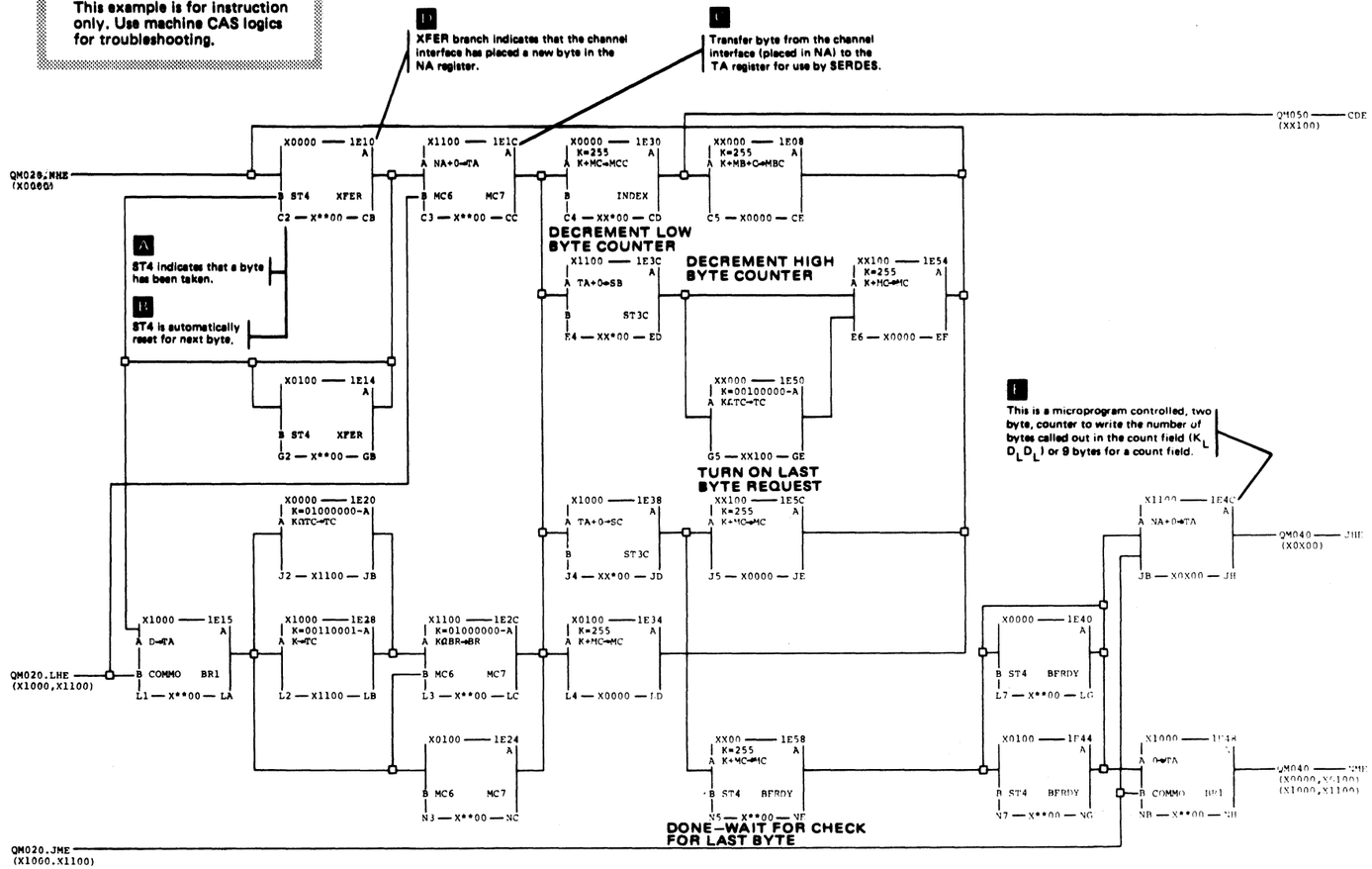
- **TRANSFER DATA FROM THE SYSTEM AND WRITE IT ON THE DISK SURFACE.**

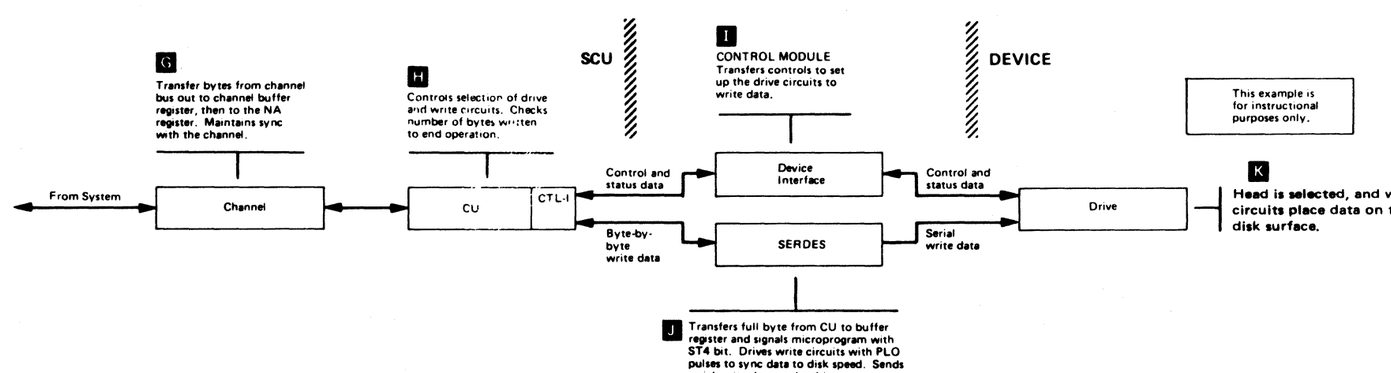


ABBREVIATIONS

CCB = CORRECTION CODE BYTE
PLO = PHASE-LOCKED OSCILLATOR
VFO = VARIABLE FREQUENCY OSCILLATOR

This example is for instruction only. Use machine CAS logics for troubleshooting.





READ COMMANDS–DESCRIPTIONS

COMMAND	CODE		FUNCTION	DETAIL DESCRIPTION	DATA READ	ERRORS (3330 and 3350) Set Unit Check-Channel End Device End			COMMENTS
	Single Track	Multi-Track				Data Overrun	Data Check: Correctable	Data Check: Uncorrectable	
Read Data	06	86	Transfer data area of a record from drive to main storage	CMD 120	First data area after address marker or the data area of the record that was chained from the count or key area of the same record	Yes	Use ECC	Use Command Retry	
Read Key Data	0E	8E	Transfer key and data areas of a record from drive to main storage	CMD 120	First key, data area after address marker or the key, data area that was command-chained from the count area of the same record	Yes	Data field. Use ECC.	Use Command Retry	If the KL equals 0 the command is executed the same as a Read Data command
Read Count Key Data	1E	9E	Transfer count, key, and data areas of a record from drive to main storage	CMD 120	Next record or first record after R0	Yes	Data field. Use ECC.	Use Command Retry	
Read Record Zero (R0)	16	96	Transfer R0 (count, key and data) from the drive to main storage	CMD 110	R0	Yes	Data field. Use ECC.	Use Command Retry	When chained from a Search HA or Read HA command, the Read R0 command is executed immediately and does not initiate a search for index point
Read Count	12	92	Transfer next count field (eight bytes) from the drive to main storage	CMD 110	Next record count field or first count field after R0	Yes		Use Command Retry	
Read Home Address	1A	9A	Transfer five bytes (FCCHH) to channel	CMD 110	Byte 0 = Flag. Byte 1 - Cylinder address. Byte 2 = Cylinder address. Byte 3 = 0. Byte 4 = Head address.	Yes		Use Command Retry	
Read Initial Program Load	02	—	Recalibrate to cylinder 0 and head 0, search for index point, and read R1 data from the drive to main storage	CMD 125	First data area after R0	Yes	Data field. Use ECC.	Use Command Retry	A Read IPL command cannot be preceeded by a Set File Mask command in the same chain
Read Sector	22	—	Provide one byte of angular position information, which is used by a subsequent Set Sector command. When not chained from a Read, Write, or Search CCW, the byte transferred is the angular position required to access the last record processed on the drive. When chained, the byte transferred is the angular position of the record used in the previous CCW.	CMD 125					Causes loss of orientation
Read Multiple CKD	5E	—	Transfer count, key, and data areas of the remaining records of the track from drive to main storage.	CMD 125	Start next record until end of track (excluding R0)	Yes	Use ECC	Yes	23FD Disk P/Ns 4168811 and 4168816 only

ERRORS (3340)
Set Channel End, Device End, and Unit Check in status. Data overrun, correctable data check (data field only), or uncorrectable data check in sense data. For correctable data check, retry status is presented. When the command is reissued, unit check is presented, which breaks the command chain.

READ OPERATION

Reads data, selected by the system, from the disk surface and transfers it to the system.

STORAGE CONTROL UNIT

CONTROL MODULE

DEVICE

1 SYSTEM

- Executes Start I/O instruction, which addresses a channel command word (CCW) containing a Read command.

2 CHANNEL

- Executes the CCW to transfer the Read command to the CU.
- Transfers the address of the selected data to the CU.
- Transfers data from the CU to the system.

3 CHANNEL CONTROLS

- Controls the timing of the transfer of data and control information between the channel and the CU.
- Checks parity of data transferred to the CU.

4 CONTROL CIRCUITS

- Decode the Read command.
- Select the addressed module and head.
- Check the status of the module and transfer the status to the channel.
- Set up the read controls in the module.
- Control the serial-by-byte transfer of read data from the control circuits to the channel interface.
- Check subsystem for errors.
- Transfer ending status to the the channel.
- 3330 – Indicate retry status to the channel if error occurs and is a type that can be retried, and set up to relocate record.

5 ISC/CONTROL INTERFACE

- Transfers read control information to the control circuits.
- Transfers control/drive status to the CU.
- Transfers byte-by-byte data from the control module to the CU.

6 SERDES

- Receives the modified frequence modulation (MFM) data from the module.
- Recognizes gaps and synchronizes to the data.
- Changes serial-by-bit drive data to serial-by-byte data.
- Sends data to the CU and ECC.
- Uses phase-locked oscillator (PLO) pulses to maintain synchronization when not reading.
- Uses ECC bytes to check for errors.

7 DEVICE INTERFACE

- Transfers read control information to the selected module.
- Transfers status of the selected module to the CU.

8 READ CONTROLS

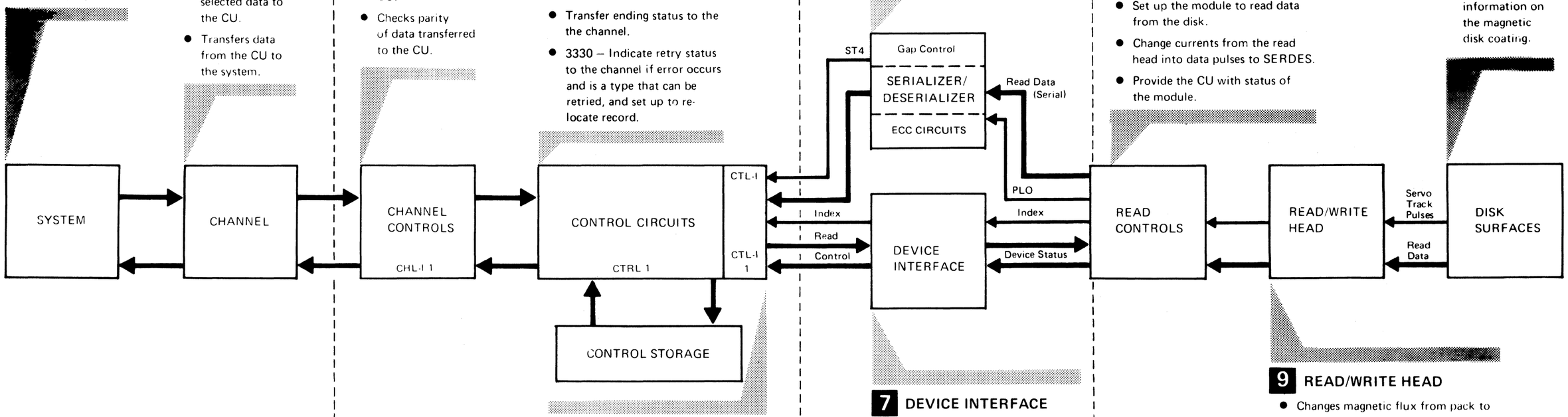
- Set up the module to read data from the disk.
- Change currents from the read head into data pulses to SERDES.
- Provide the CU with status of the module.

9 READ/WRITE HEAD

- Changes magnetic flux from pack to read current signals.
- Selected head provides data pulses.
- Servo head provides PLO pulses.
- Servo head and circuits hold access at selected track.

10 DISK SURFACES

- Contain bits of information on the magnetic disk coating.



READ COMMANDS OBJECTIVES

READ MULTIPLE COUNT KEY DATA (5E)
READ HOME ADDRESS (1A or 9A)
READ RECORD ZERO (16 or 96)
READ COUNT (12 or 92)
READ COUNT KEY DATA (1E or 9E)
READ KEY DATA (0E or 8E)
READ DATA (06 or 86)
READ INITIAL PROGRAM LOAD (02)

Refer to CMD 105 and CMD 130 for subsystem components used. Refer to CMD 110 through CMD 125 for flowcharts and CAS references. Refer to CMD 400 for Read overflow operations. Read to CMD 430 for Read multitrack operations.

- Check for valid command.
- No requirement for preceding CCWs except that no Set File Mask command may precede a Read IPL in the same chain.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer data, from the disk track selected by the system, through the control unit to the channel.

Note: *Correction code bytes for each field are read and checked. HA, count, and key fields are stored in control storage for use in error correction (3330 only: retry and correct in control storage.) The commands and their effects are:*

1. Read Home Address:Wait for index; clock gap and control bytes; read five bytes (FCCHH); end in gap.
2. Read R0:If not in gap after HA, wait for index; clock gap, control bytes, HA field, and gap. Balance of operation is the same as Read CKD operation.
3. Read count: Clock through all fields and gaps until a count field is located (excluding R0 count); read eight bytes of data (CCHHRKDD); end in gap.
4. Read CKD: Clock through all fields and gaps until a count field is located (excluding R0 count); read the count field data; clock gap and read key data (if required); clock gap; read data field (if required); end in gap.
5. Read Key Data: Clock through all fields and gaps (including R0 key) to the next key field; read key field; clock gap; read data field; end in gap. If key CCW count = 0, this command is the same as a Read Data command.
6. Read data: Clock through all fields and gaps (including R0 data) to the next data field; read data field; end in gap.
7. Read IPL: Seek to track 0 and select head 0; wait for index; clock all gaps and fields to the data field of record 1; read data field; end in gap.

- If Check 2 errors are indicated, end operation and present Unit Check, Channel End, and Device End in ending status. Set appropriate sense data in control storage.
- If Data Overrun or Data Check is indicated, do one of the following:

1. If 3330 or 3350: Entry retry mode.
2. If 3340: Present Unit Check, Channel End, and Device End in ending status. Set Data Check or Data Overrun in sense data.

- If no errors occur, present Channel End and Device End in ending status.

8. Read Multiple CKD: Clock through all fields and gaps until a count field is located (excluding R0 count), read the count field data, clock gap and read key data (if required); clock gap; read data field (if required); repeat the Read operation until index.

   If Data Overrun or Data check is indicated, present Unit Check, Channel End, and Device End in ending status. Set Data Check or Data Overrun in sense data.

2. For 3330: if a Seek or Set Sector command has been executed, or if a device power-on or system reset has occurred, the byte is zero.

- If Check 2 errors are indicated, present Unit Check, Channel End, and Device End in ending status. Set appropriate sense data in control storage.
- If no errors occur, present Channel End and Device End in ending status.

READ SECTOR (22)

Refer to CMD 105 for subsystem components used. Refer to CMD 300 and CMD 305 for use of the command.

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer angular position information from controller/ device to the control unit, and send one byte to the channel.

1. Normally this information is the angular position required to reprocess the last record processed on the device selected.

READ COMMANDS—FLOWCHARTS (Part 1 of 4)

Refer to CMD 105 for sub-system components used.

Refer to CMD 107 for command objectives.

Read commands transfer data from a selected disk storage module to the system.

Read commands can operate in multi-track mode. Multi-track operations (high order bit of command on) allow the CU to cause automatic head switching at index time without a Seek Head command.

Read Count Key, Data; Read Key, Data; and Read Data commands can operate on overflow records. Overflow records allow data records of more than one track in length. Overflow operations indicated by a bit in theflag byte.

With 3330 device selected, if a data check is detected during a Read command, the CU uses ECC to correct the error, if correctable, or command retry if not. With 3340 or 3350 device selected, if a data check is detected during a Read command, the CU uses ECC to correct the error, if correctable and in the data field (there is no correction capability on HA, count or key fields). The 3350 uses command retry if the error is not correctable.

NOTES

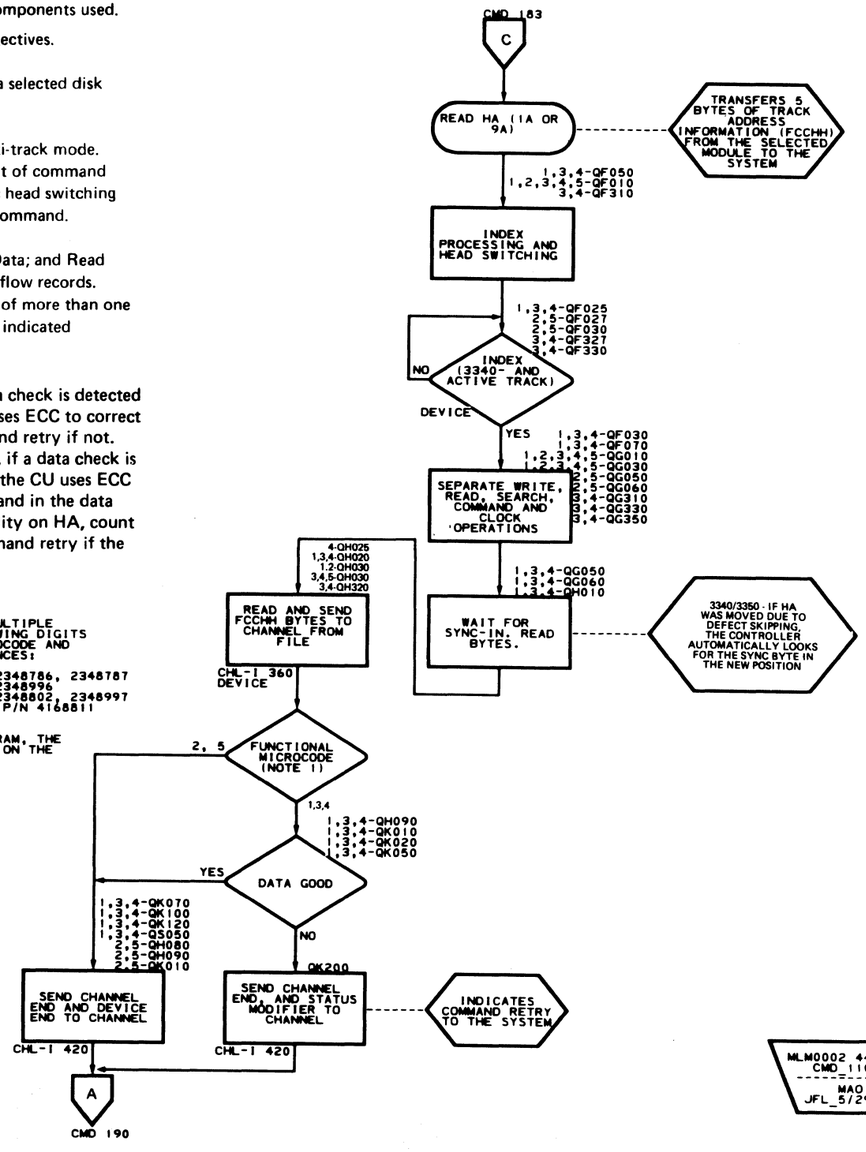
1. THIS FLOWCHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:

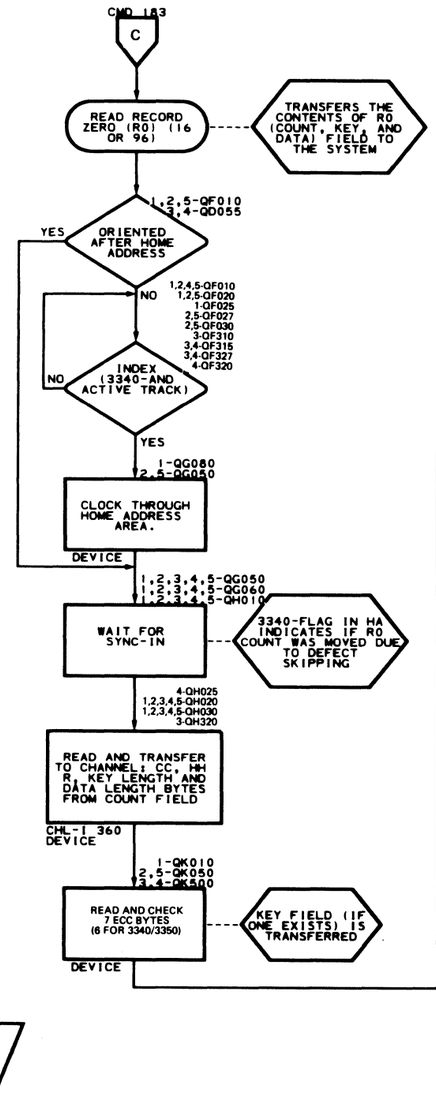
   1 - 3330 ONLY - P/N 2348605, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348757, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

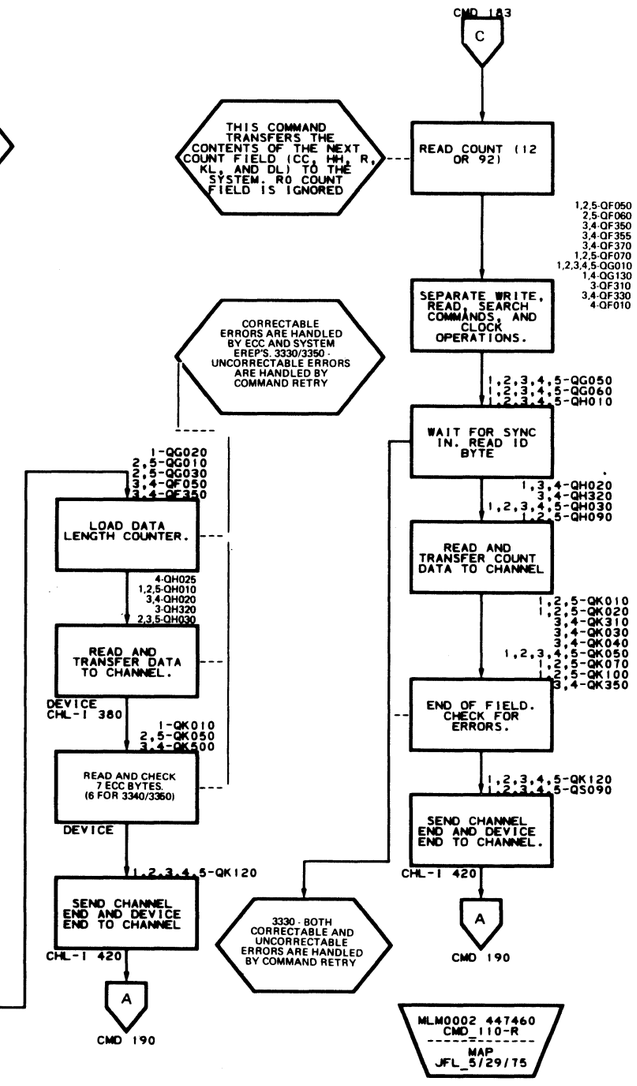
ABBREVIATIONS

DL = DATA LENGTH
ECC = ERROR CORRECTION CODE
KL = KEY LENGTH



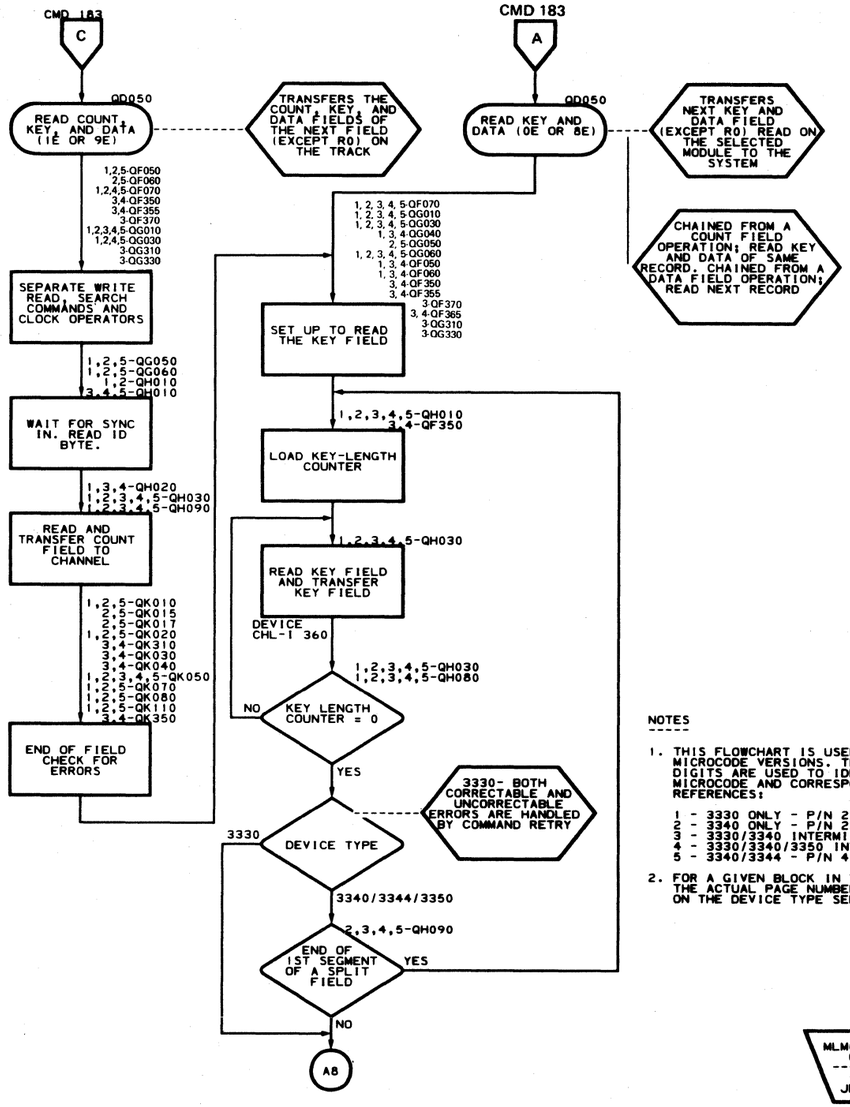


MLM0002 447460
CMD 110-L
MAO
JFL 5/29/75



MLM0002 447460
CMD 110-R
MAP
JFL 5/29/75

BX1100 Seq. 1 of 2	2347204 Part No. (8)	437402A 15 Mar 72	437404 23 Jun 72	437405 15 Aug 72	437415 2 Nov 73	437417 15 Apr 74	447460 19 Dec 75	447461 12 Mar 76



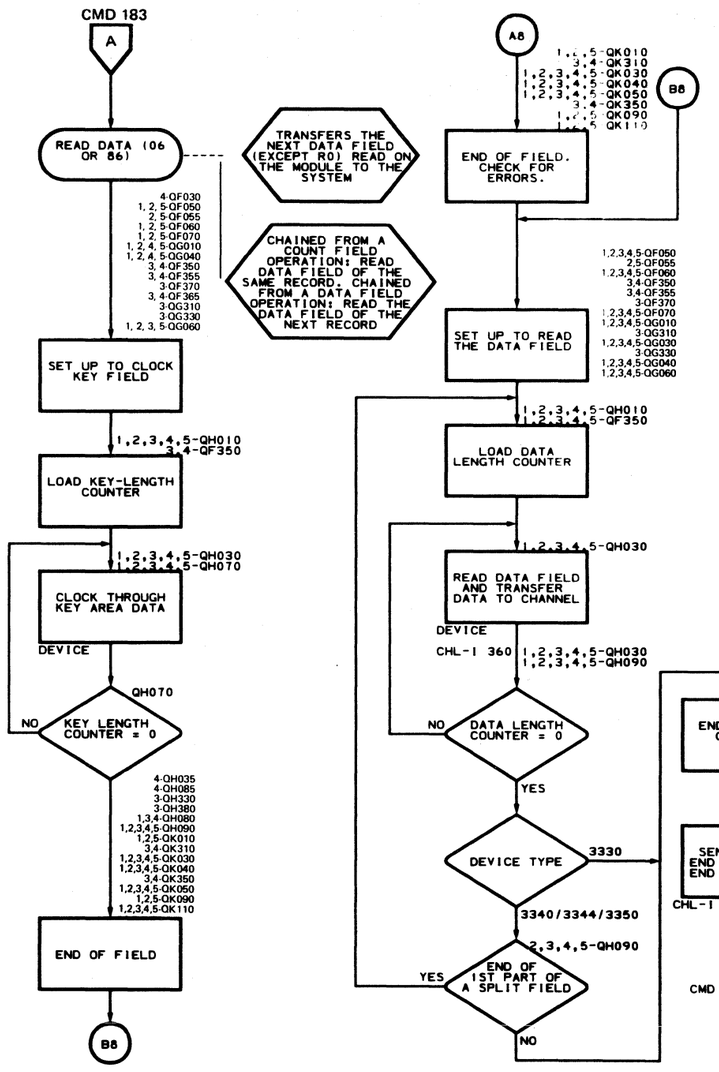
NOTES

1. THIS FLOWCHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:

   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348757, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - 4168811
   5 - 3340/3344 - P/N 4168816

2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

MLM0002 447460
CMD_120-L
MAQ
JFL_5/39/75

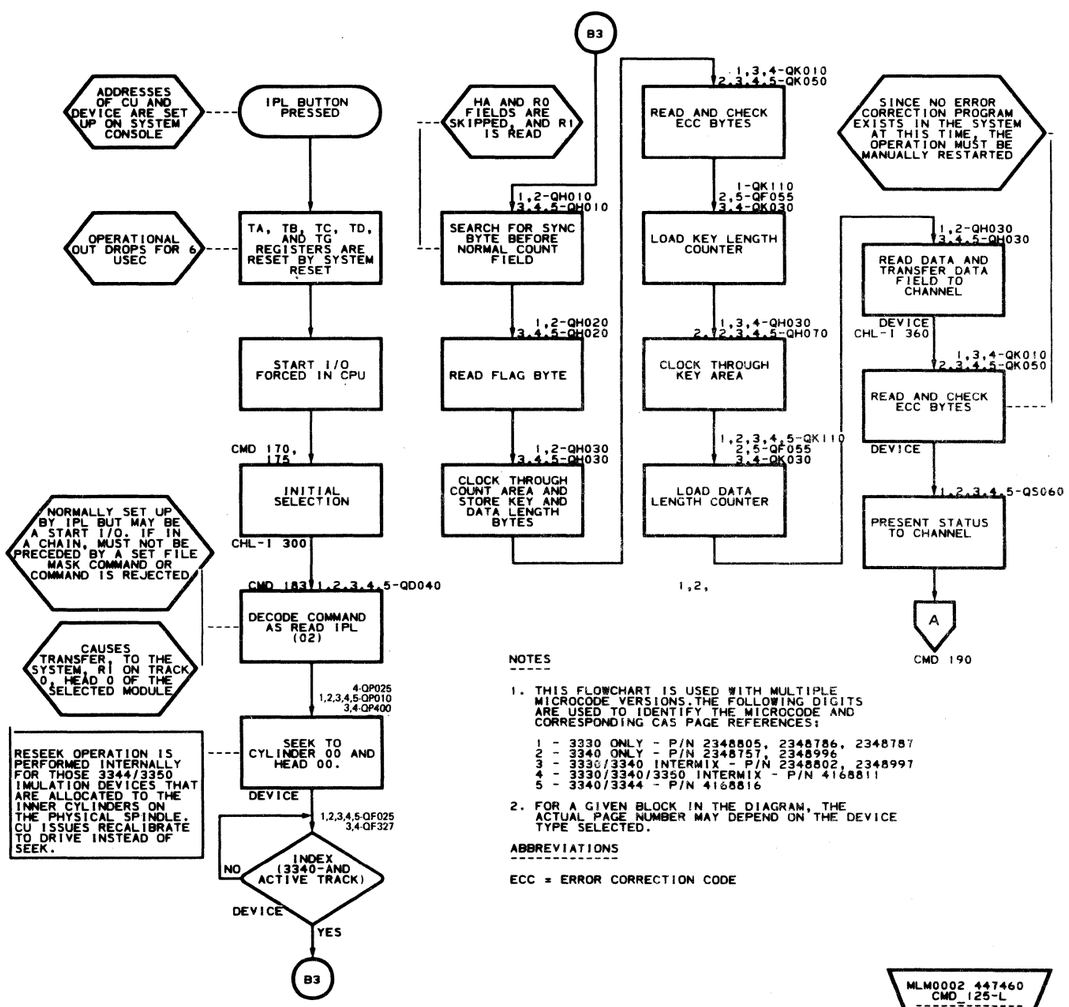


MLM0002 447460
CMD_120-R
MAR
JFL_5/29/75

BX1100 Seq. 2 of 2	2347204 Part No. (8)

437402A 15 Mar 72	437404 23 Jun 72	437405 15 Aug 72	437415 2 Nov 73	437417 15 Apr 74	437417 19 Dec 75	447461 12 Mar 76

READ COMMANDS–FLOWCHARTS (Part 3 of 4) CMD 125

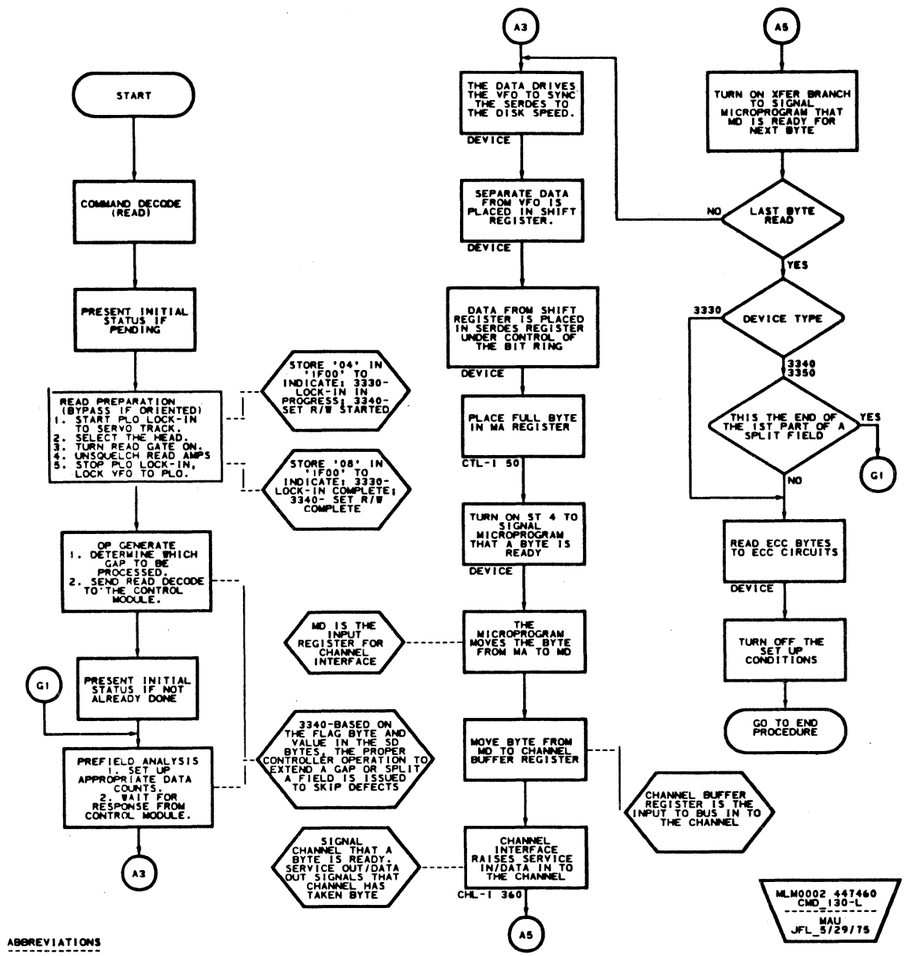


MLM0002 447460
CMD 125-L
MAS
JFL 6/5/75

MLM0002 447460
CMD 125-R
MAT
JFL 5/29/75

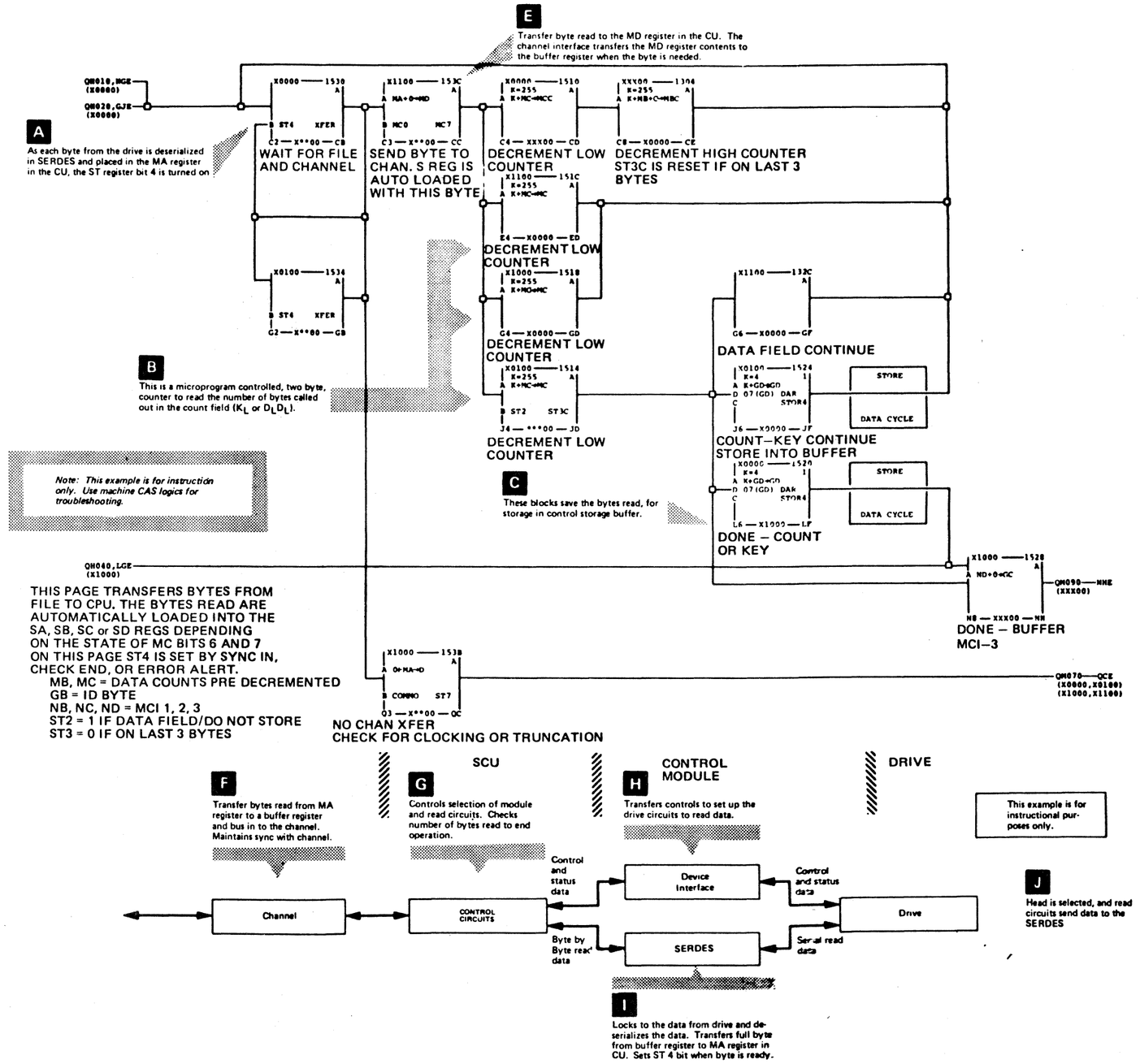
READ DATA TRANSFER

- Read data from the disk and transfer the data to the system.



ABBREVIATIONS

ECC = ERROR CORRECTION CODE
PLO = PHASE-LOCKED OSCILLATOR
R/W = READ/WRITE
VFO = VARIABLE FREQUENCY OSCILLATOR



BX1300 Seq. 1 of 2	2347206 Part No. (8)	See E/C History	447461 12 Mar 76	447463 16 Dec 76				

SENSE COMMANDS–DESCRIPTIONS **CMD 140**

Command	Code		Function	Detail Description	Data Transferred	Errors Set Unit Check-Channel and Device End	Comments
	Single Track	Multi-Track					
Test I/O	00	–	Determine the status of a device on a channel.	CMD 145	One status byte.	Command Reject. Bus Out Parity.	Status byte is normally zero.
Sense I/O	04	–	Determine the type of error or unusual condition that caused the last unit check.	CMD 145	24 bytes of sense information.	Command Reject. Bus Out Parity.	Sense data is reset after transfer.
Read and Reset Buffered Log	A4	–	Supply usage or error statistics on the addressed drive.	CMD 145	24 bytes of statistics on the drive drive.	Command Reject. Bus Out Parity.	Data is reset after transfer.
Read Diagnostic Status 1	44	–	Determine the type of error(s) found on running a diagnostic test (part of a diagnostic write command). Transfer a diagnostic test from the storage control unit to the system (after a diagnostic load command).	CMD 150	16 bytes of error code message. 512 bytes of diagnostic test data.	Command Reject. Bus Out Parity. Overrun.	If the command is not preceded by a Diagnostic Write or Load command, 16 bytes of data from the error code message area are transferred.
Device Reserve	B4	–	Set bits in control storage and in controller (with String Switch feature) to reserve addressed devices. Transfer 24 bytes of sense data to the channel.	CMD 150	24 bytes of sense information.	Command Reject. Bus Out Parity.	If command is not the first one in the chain, Command Reject will be set in sense data.
Device Release	94	–	Store null value in control storage and in controller (with String Switch feature) to cancel reservation for devices addressed. Transfer 24 bytes of sense data to the channel.	CMD 150	24 bytes of sense information.	Command Reject. Bus Out Parity.	If command is not the first one in the chain, Command Reject will be set in sense data.
Sense I/O Type	E4		Determines the I/O device type and model number.	CMD 145	7 bytes of sense information.	Command Reject. Bus Out Parity.	Supported only in 3340/3344 Intermix microcode (P/N 4168816) and 3330/3340/3350. Intermix microcode (P/N 4168811 at EC 442498 or later.)
Unconditional Reserve	14	–	Resets bits in control storage and in controller to cancel reservation for addressed device for another path. It then sets bits to reserve addressed device via this path.	CMD 150	24 bytes of sense information	Command Reject. Bus Out Parity. Equipment Check.	Supported only in 3330/3340/3350 Intermix microcode (P/N 4168811 at EC 437464 or later).

SENSE COMMANDS — OBJECTIVES

TEST I/O (00)

Refer to CMD 145 for flowchart and CAS references.

- Test I/O is not part of a CCW from the channel.
- Test I/O is an immediate command and has only one status byte.
- The initial status byte presented is normally zero.
- If status for the selected device has been stacked or is pending (see CMD 181), present it to the channel.
- Sense data in control storage is not changed unless a Unit Check occurs on the Test I/O command (Bus Out Parity, Command Reject).

SENSE I/O (04)

Refer to CMD 145 for flowchart and CAS references. Refer to SENSE 1 for sense data layout and bit meanings.

- Sense data was set up, in control storage, in the proper format. This was done by the end procedure routine of the command that presented the unit check. (See CMD 190.)
- A Unit Check status on a command sets up a contingent connection state (see CMD 181) on the selected controller/ device. The Unit Check also forces a busy condition to other addresses.
- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer 24 bytes of sense data from control storage to the channel. Fewer than 24 bytes are transferred if the channel truncates the operation.
- Reset the sense data in control storage.
- Present Channel End and Device End in ending status.

READ AND RESET BUFFERED LOG (A4)

Refer to CMD 165 for subsystem components used. Refer to CTRL 650 for layout of log data in control storage. Refer to CMD 145 for flowchart and CAS references. Refer to SENSE 1 for environmental data meanings.

- Log data is information pertaining to the operation of a given device.
- Data transferred is the same as sense format 6.
  1. If limits are exceeded, a Unit Check is presented, and a Sense I/O command will transfer format 6 data.
  2. If the CPU program calls for the data (that is, the end-of-day routine) with a Read and Reset Buffered Log command, the sense data is set up and transferred to the channel. To clear the complete log, the command must be repeated for each device attached.
- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Set up sense data format 6 in control storage. Normally, this data is in coded form in log area of control storage.
- Transfer 24 bytes of data to the channel. (Twenty–four is maximum; transfer fewer bytes if CCW count is less.)
- Reset log area for the selected device. Reset sense data area of control storage.
- Present Channel End and Device End in ending status.

READ DIAGNOSTIC STATUS 1 (44)

Refer to CMD 160 and CMD 165 for use of command and subsystem components used. Refer to CTRL 650 for layout of control storage error code message data. Refer to CMD 150 for flowchart and CAS references.

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and Device End in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors occur, return zero status to the channel.
- Transfer data from control storage to the channel.
  1. If the command is chained from a preceding Diagnostic Write CCW, transfer 16-byte error code message. Sixteen is maximum; if CCW count is less than 16, transfer CCW count only.)
  2. If the command is chained from a preceding Diagnostic Load CCW, transfer 512-byte block of data (diagnostic test).
  a. If CCW count > 512, transfer only 512 bytes.
  b. If CCW count < 512, transfer CCW count and set Command Reject.
  3. If no diagnostic Write or Load command, transfer 16 bytes from error code message area. (Data is invalid.) If CCW count is less than 16, transfer CCW count only.)
- If Bus Out Parity Error or Command Reject is indicated, present Unit Check, Channel End, and Device End in ending status. Set appropriate bits in sense data.
- If no errors occur, present Channel End and Device End in ending status.

UNCONDITIONAL RESERVE (14)

- Used with SCUs with the string switch feature installed. (See Note 1.)
- Check for valid command.
- Must be first command in chain.
- If errors occur, present Unit Check, Channel End, and device end status. Set Command Reject in sense data (see SENSE 1 and CTRL 650).
- If no errors, return zero status to the channel.
- Check addressed controller/device:
  1. If controller or device is 3350 operating in 3330-1 compatibility mode, set Command Reject.
  2. Force reset of Reserve indication to addressed device on other channel and set Reserve indication for addressed device in control unit and controller.
- Balance of operation is the same as a Sense I/O operation.

DEVICE RESERVE (B4)

- Used with SCUs with more than one channel attached or with the string switch feature installed. (See Note 1.)
- Check for valid command.
- No requirement for preceding CCWs, except that the command must not be preceded by a Set File Mask command in the same chain.
- If errors occur, present Unit Check, Channel End, and device end in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors, return zero status to the channel.
- Check addressed controller/device:
  1. If controller is out of service (powered down Interface Disabled, etc.), set up to present condition code 3. (See Note 2.)
  2. If device is reserved to other channel or control unit, set Pending Device End indicator.
  3. If device is available, set Reserve indication in the control unit and/or the controller.
- Balance of the operation is the same as a Sense I/O operation.

DEVICE RELEASE (94)

- Used with SCUs with more than one channel attached or with the string switch feature installed. (See Note 1.)
- Check for valid command.
- No requirement for preceding CCWs, except that the command must not be preceded by a Set File Mask command in the same chain.
- If errors occur, present Unit Check, Channel End, and device end in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.
- If no errors, return zero status to the channel.
- Check addressed controller/device:
  1. If controller is out of service (powered down Interface Disabled, etc.), set up to present condition code 3. (See Note 2.)

Notes:

1. *Refer to device MLM for circuit description of string switch feature.*
2. *On SCU with 3330 feature and without string switch feature, the command is executed.*

SENSE COMMANDS – OBJECTIVES (Continued)

2. If device is reserved to other channel or control unit, set Pending Device End indicator.
3. If device is available, reset Reserve indication in the control unit and/or the controller.

- Balance of the operation is the same as a Sense I/O operation.

SENSE I/O TYPE (E4)*

Refer to CMD 145 for flowchart and CAS references.

- Check for valid command.
- No requirement for preceding CCWs.
- If errors occur, present Unit Check, Channel End, and device end in status. Set Command Reject in sense data. (See SENSE 1 and CTRL 650.)
- If no errors, return zero status to the channel.
- Transfer 7 bytes of sense data to the channel as follows (Hex):

		3330-1	3330-11	3340 (35)	3340 (70)	3344	3350
Byte 0	'FF'						
Byte 1	'38' } Control						
Byte 2	'30' } Unit						
Byte 3	'02' } Type						
Byte 4	Device Type No.	'33'	'33'	'33'	'33'	'33'	'33'
Byte 5	Device Type No.	'30'	'30'	'40'	'40'	'44'	'50'
Byte 6	Device Model No.	'01'	'11'	'01'	'02'	'00'	'00'

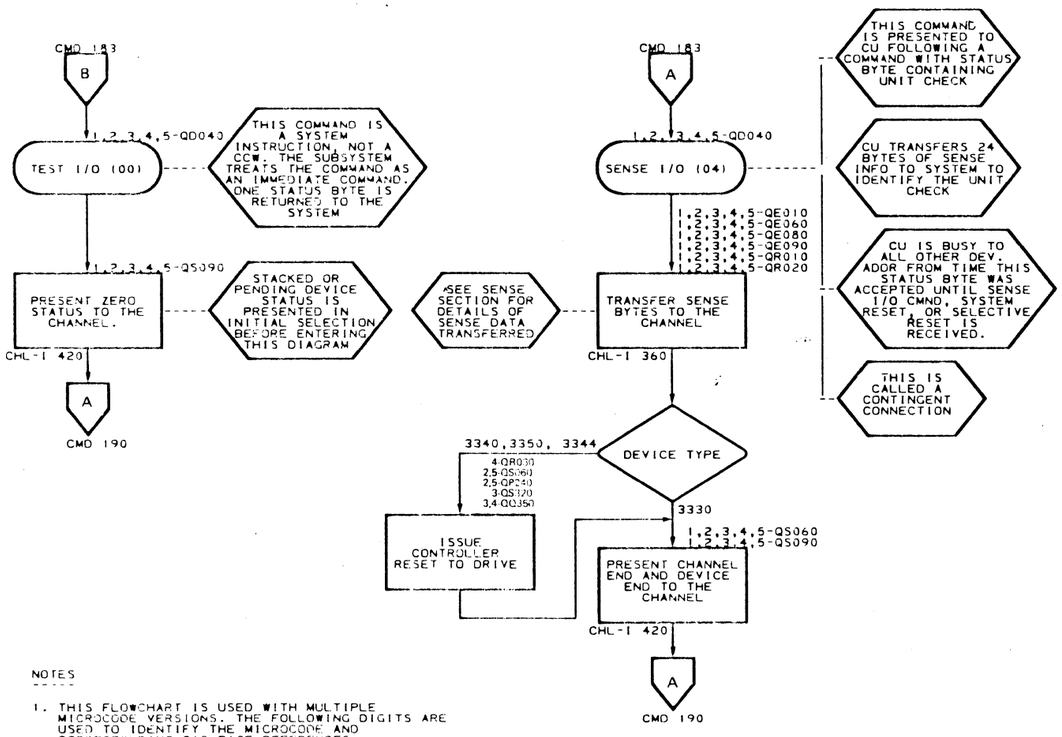
- Present Channel End and Device End in ending status.

For microcode P/Ns 4168811 and 4168816 only.

BX1400 Seq. 2 of 2	2347207 Part No. (8)	See EC History	447461 12 Mar 76	447463 16 Dec 76				

SENSE COMMANDS—FLOWCHARTS (Part 1 of 2)

- Execution of Sense Commands transfers sense and status information to using system.
- Sense information summary referenced on SENSE 1.



NOTES

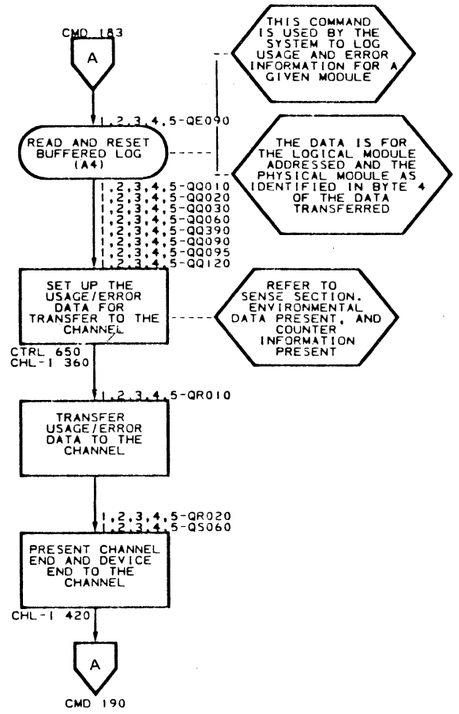
1. THIS FLOWCHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:

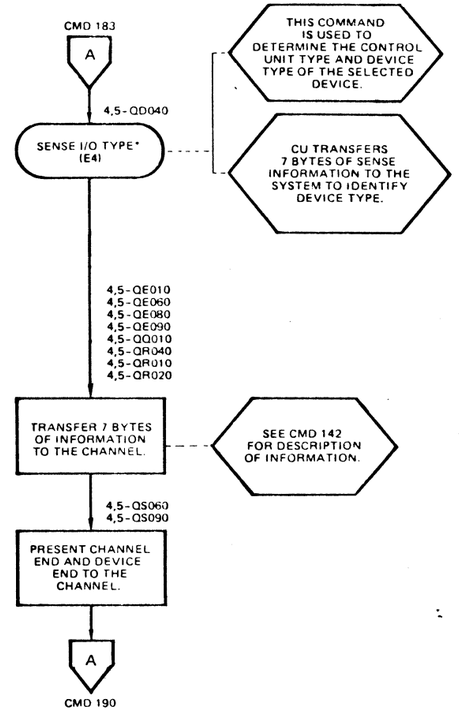
   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348757, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

MLM0002 447460
CMD_145-L
MAV
JFL_5/29/75

BX1450	4290609	447463
Seq 1 of 1	Part No. (8)	16 Dec 76

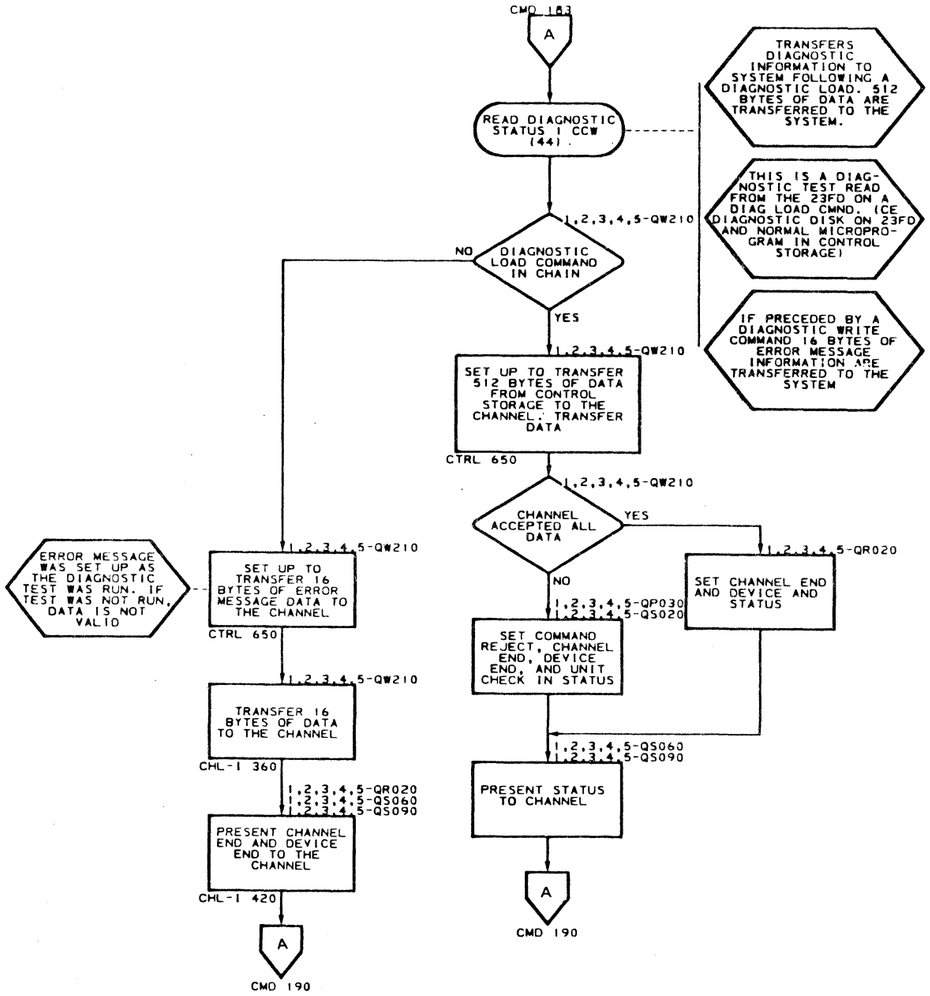


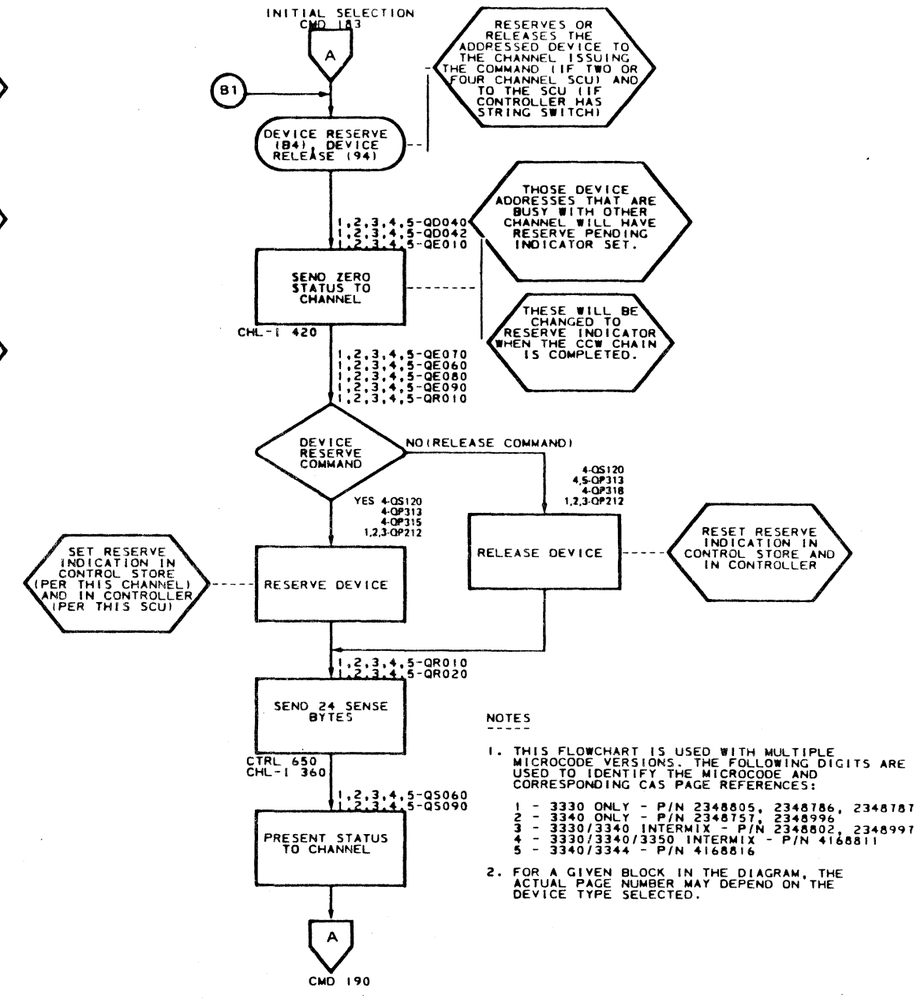


*FOR MICROCODE P/Ns 4168811 AND 4168816 ONLY.

MLM0002 447460
CMD_145-R
MAW
JFL_5/29/75

SENSE COMMANDS–FLOWCHARTS (Part 2 of 2) **CMD 150**





NOTES

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   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348757, 2348996
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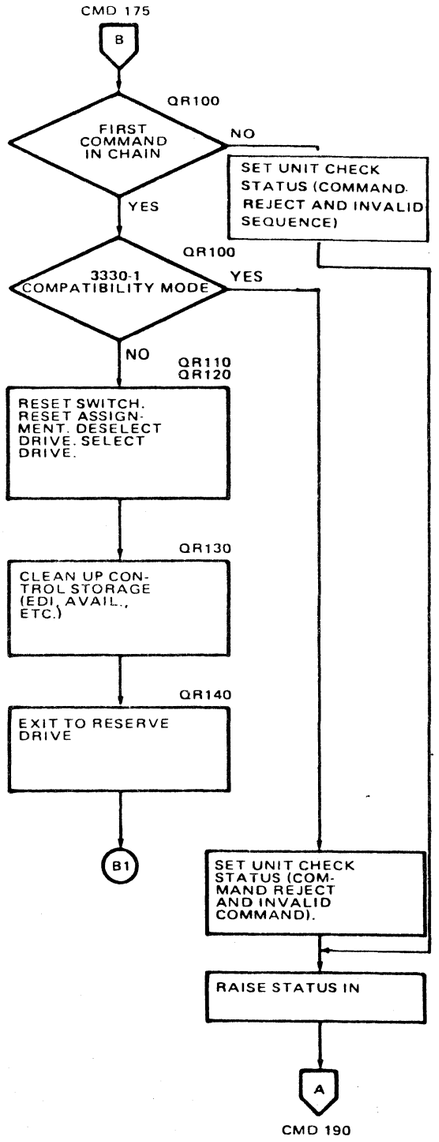
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.



MLM0002 447460
CMD_150-L
MAX
JFL_5/29/75

MLM0002 447460
CMD_150-R
MAY
JFL_6/5/75

BX1500 Seq. 1 of 2	2347208 Part No. (8)	See EC History	447461 12 Mar 76	447463 16 Dec 76				

TRANSFER INLINE DIAGNOSTICS TO CONTROL UNIT

- Diagnostics stored in system diagnostic library can be sent to SCU to test subsystem.
- After diagnostic is run, error code is returned to system.

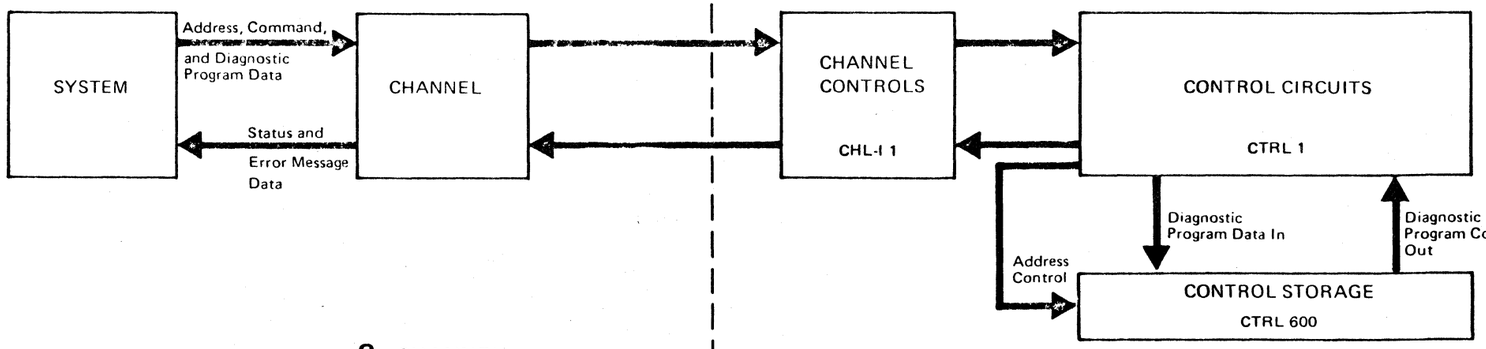
To provide maximum facility availability, the SCU can execute diagnostic tests on a drive concurrent with normal system operations on the remaining drives. This mode of operation allows the customer engineer to diagnose and repair most drive failures while the facility continues to operate other attached drives. The SCU provides a transient block of 512 bytes (128 words) of control storage to allow temporary residence for a specific diagnostic test.
The transient area is loaded under control of the Online Test Executive Program (OLTEP). A special command, Diagnostic Write, loads a selected test into control storage and instructs the CU to execute the test. Loading and execution can also be initiated from the CE panel.
After the test, error message information or test results are transferred from the SCU to main storage by a Read Diagnostic Status 1 command. If the CE panel is used, the test results are displayed in the CE panel indicators.

CENTRAL PROCESSING UNIT

STORAGE CONTROL UNIT

1 SYSTEM

- Executes a Start I/O instruction that addresses a Diagnostic Write command.
- After receiving Device End status, executes a Start I/O instruction that addresses a Read Diagnostic Status 1 command.



2 CHANNEL

- Transfers address and command information to the selected subsystem.
- Transfers status of subsystem to the system.
- Transfers diagnostic data to the subsystem.
- Transfers error code from subsystem to the system.

3 CHANNEL INTERFACE

- Controls timing of data to and from the channel.
- Checks parity of data transferred to the SCU.

4 CONTROL CIRCUITS

- Decode the Diagnostic Write command.
- Set up and control the transfer of data from channel interface to the control storage diagnostic buffer area.
- Run inline diagnostic.
- Store 16-byte error code in the control storage buffer area if errors are found.
- Send Channel End and Device End status to the channel.
- Decode Read Diagnostic Status 1 command.
- Transfer error code from the control storage to the channel on Read Diagnostic Status 1 command.
- Send Channel End and Device End status to the channel.

5 CONTROL STORAGE

- Stores main microprogram to control Diagnostic Write and Read Diagnostic Status 1 commands.
- Stores diagnostic from system in a buffer area.
- Stores error code for any errors found.

READ DIAGNOSTICS TO SYSTEM

- Diagnostic tests resident in diagnostic library stored on the CE diagnostic 23FD disk (MPL file) can be read to CPU of using system.
- Execution of Diagnostic Load CCW followed by Read Diagnostic Status 1 transfers 512 bytes from 23FD to CPU.

Any diagnostic test stored on the CE 23FD disk can be selected by the using system. To transfer the diagnostic test, the using system must execute a Diagnostic Load CCW followed by a Read Diagnostic Status 1 command. The Diagnostic Load command transfers 512 bytes (containing the specific diagnostic) from the 23FD to control storage. The Read Diagnostic Status 1 command then transfers the 512 bytes from control storage to the using system main storage. Refer to CMD 25 and CMD 30 for description of the command operations.

CPU **SCU**

1 SYSTEM

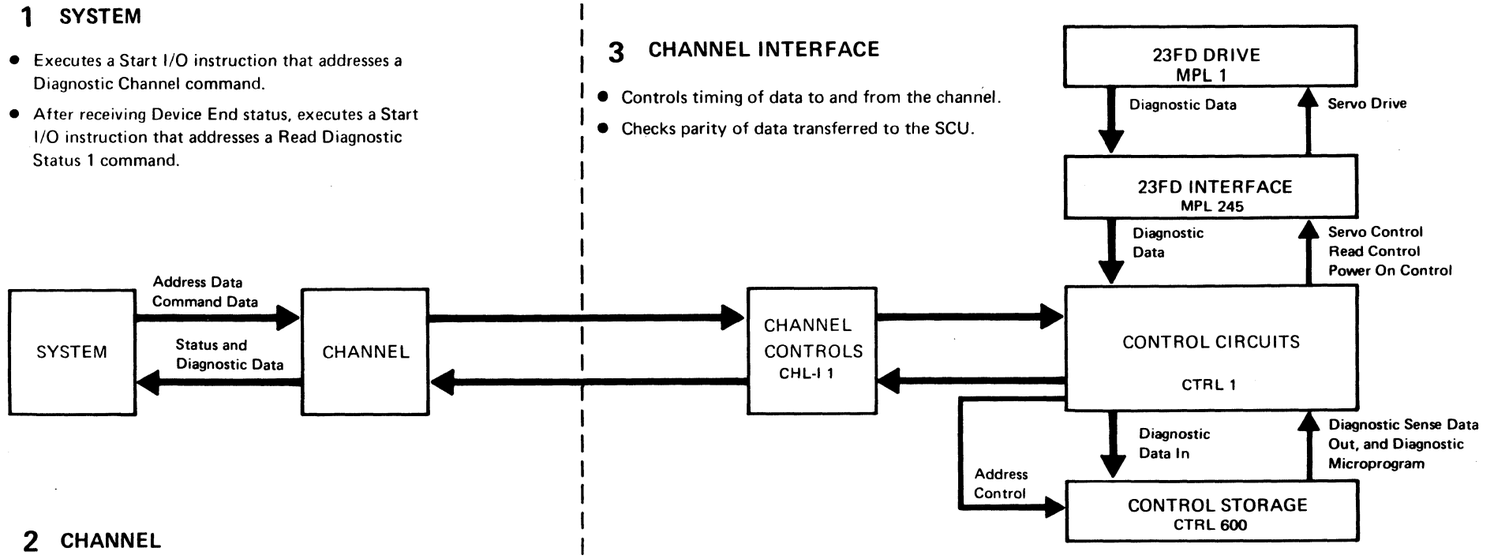
- Executes a Start I/O instruction that addresses a Diagnostic Channel command.
- After receiving Device End status, executes a Start I/O instruction that addresses a Read Diagnostic Status 1 command.

2 CHANNEL

- Transfers address and command information to the selected subsystem.
- Transfers status of subsystem to the system.
- Transfers diagnostic from subsystem to system storage.

3 CHANNEL INTERFACE

- Controls timing of data to and from the channel.
- Checks parity of data transferred to the SCU.



4 23FD DRIVE

- Provides drive for disk.
- Provides for movement of head from track to track.
- Picks up data signals from disk via read head.

5 23FD INTERFACE

- Starts 23FD drive motor.
- Moves ahead to track selected by the Diagnostic Load commands.
- Moves disk into contact with the head.
- Reads 512 bytes of data from the disk.

6 CONTROL STORAGE

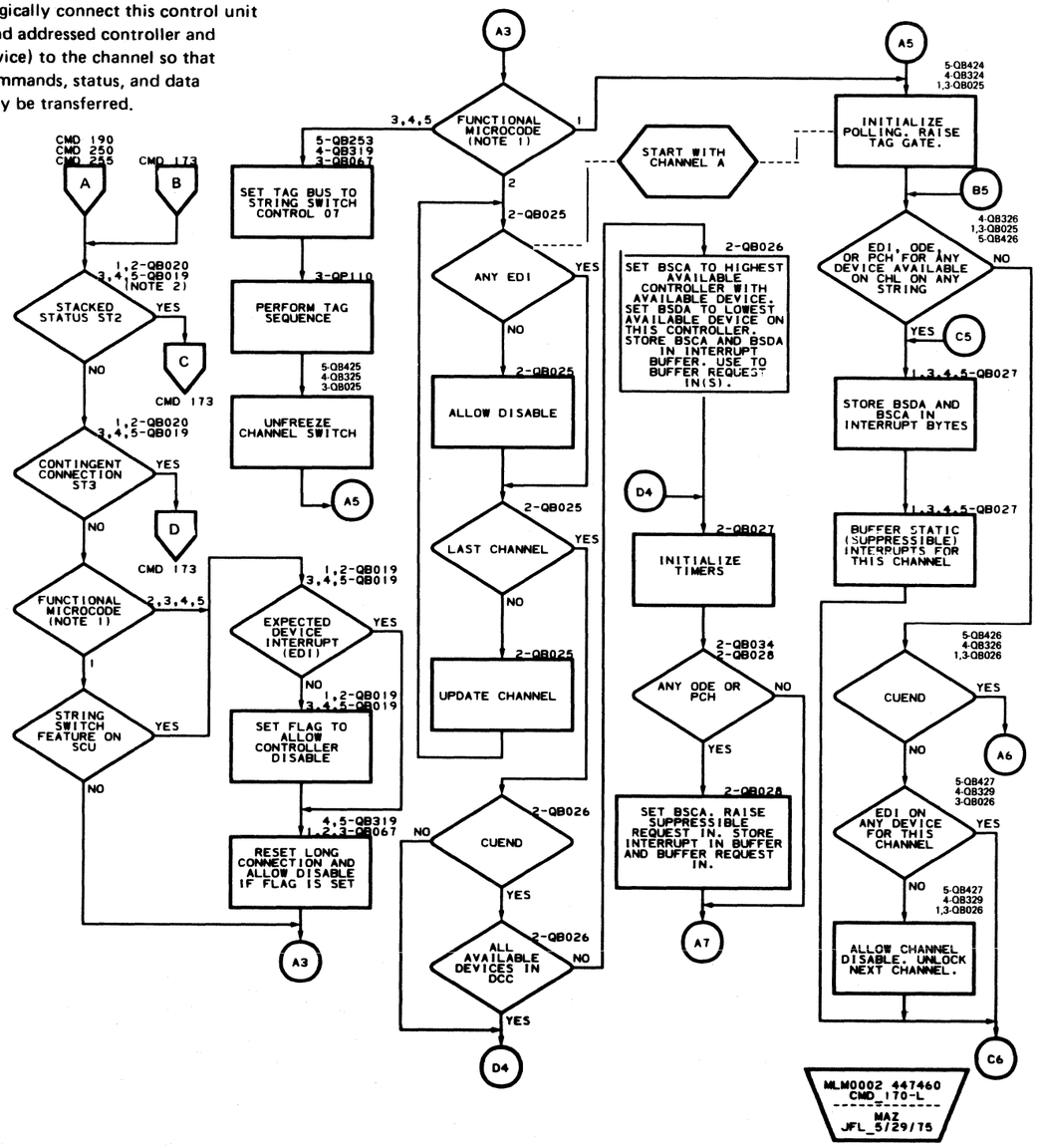
- Stores microprogram to control the operation of subsystem.
- Stores diagnostic data read from 23FD by the Diagnostic Load operation. This data is then transferred by the Read Diagnostic Status 1 command.
- Reads diagnostic data out to CU on diagnostic sense operation.

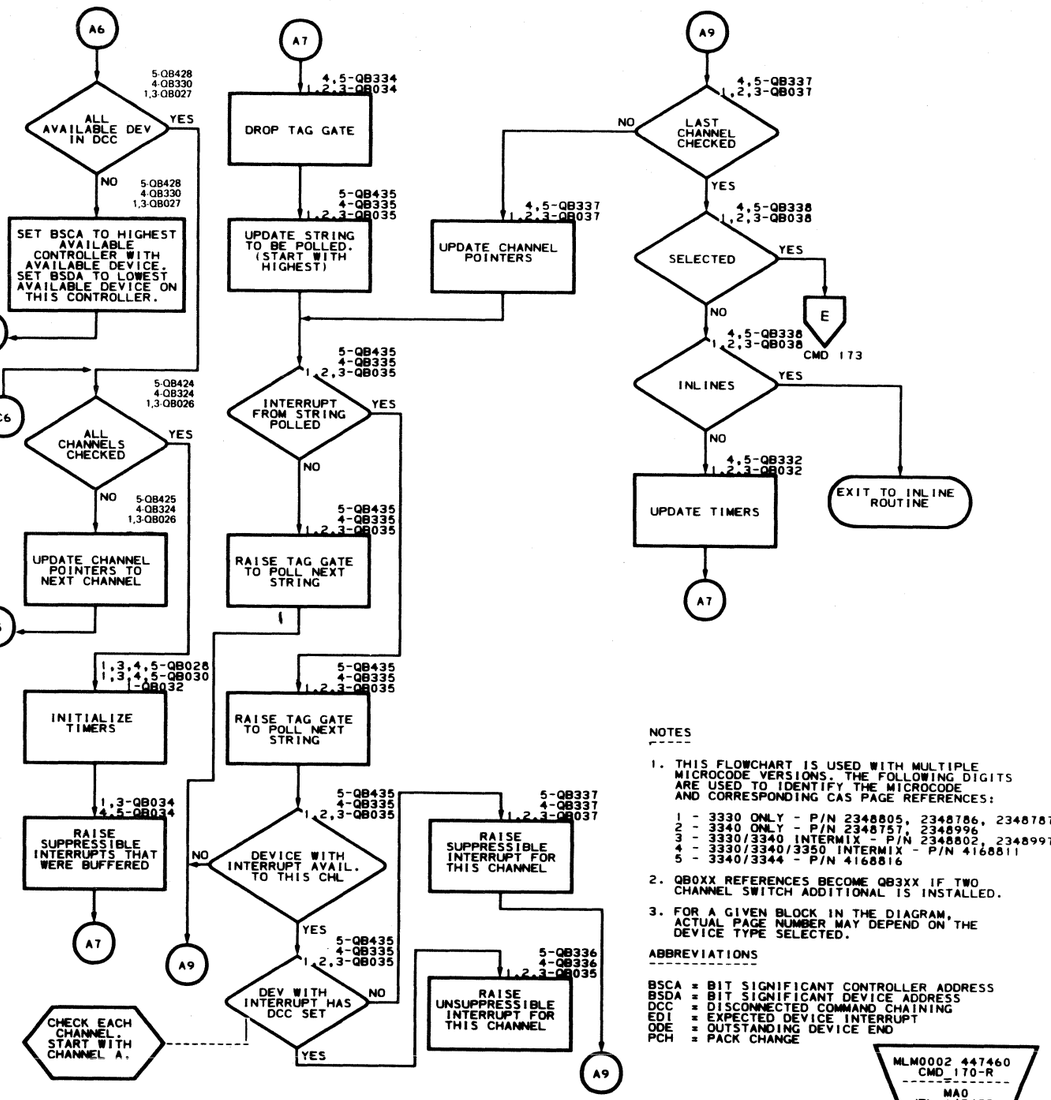
7 CONTROL CIRCUITS

- Decode the Diagnostic Load command.
- Send Start, Seek and Read control lines to the 23FD interface according to the control byte sent with the Diagnostic Load command.
- Transfer diagnostic data from 23FD to the control storage.
- Transfer Channel End and Device End to the channel after data is read into control storage.
- Decode Read Diagnostic Status 1 command.
- Control transfer of data from control storage to the channel.
- Transfer subsystem status to the channel.
- Control transfer of data (512 bytes) from control storage to the channel.
- Send Channel End and Device End status to the channel.

POLLING IDLE LOOP AND INITIAL SELECTION (Part 1 of 4)

- Poll for interrupt conditions.
- Check for channel selection.
- Check for inline operations.
- Handle request in conditions.
- Logically connect this control unit (and addressed controller and device) to the channel so that commands, status, and data may be transferred.





NOTES

1. THIS FLOWCHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:

   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348787, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

2. QB0XX REFERENCES BECOME QB3XX IF TWO CHANNEL SWITCH ADDITIONAL IS INSTALLED.

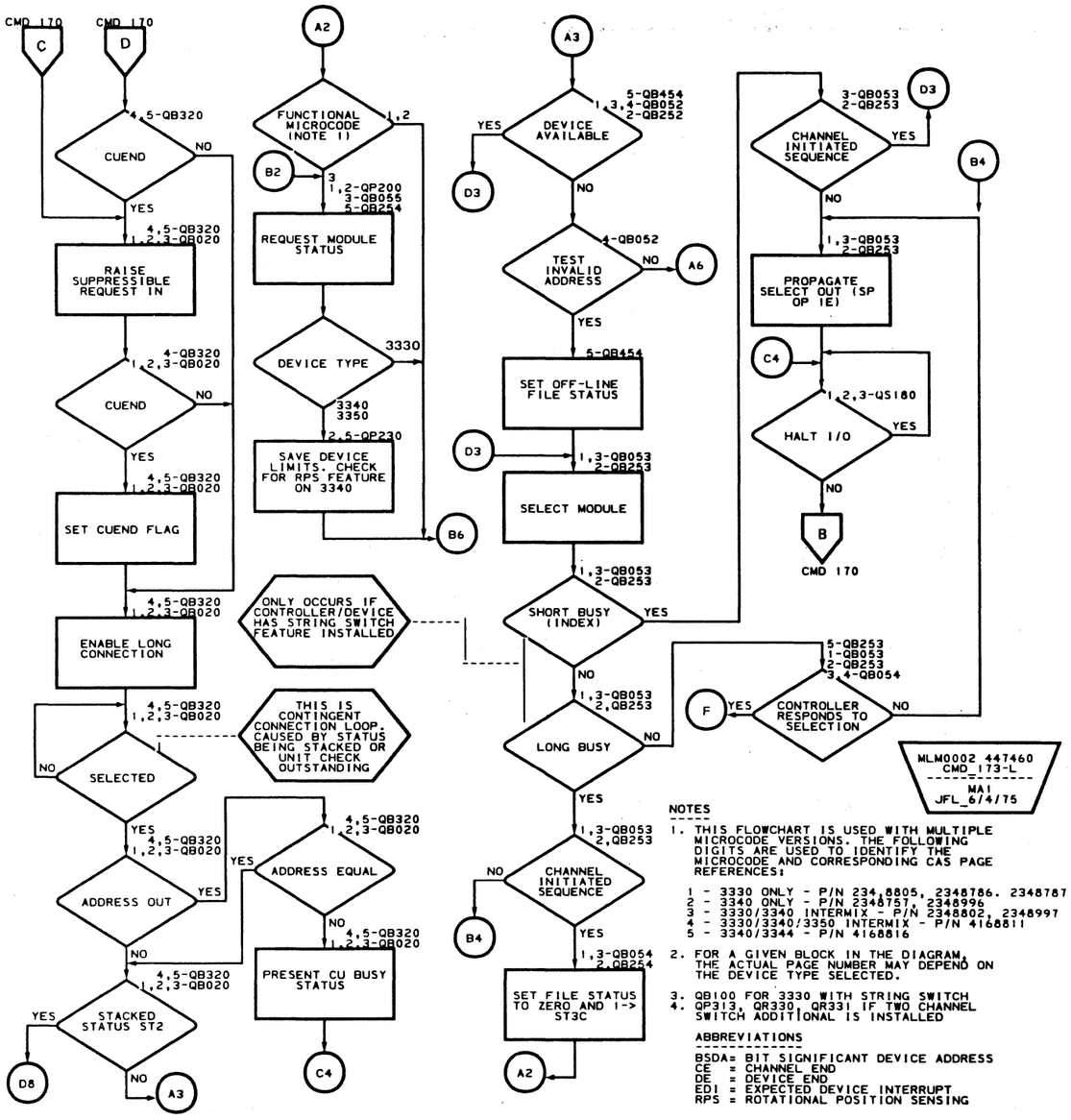
3. FOR A GIVEN BLOCK IN THE DIAGRAM, ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

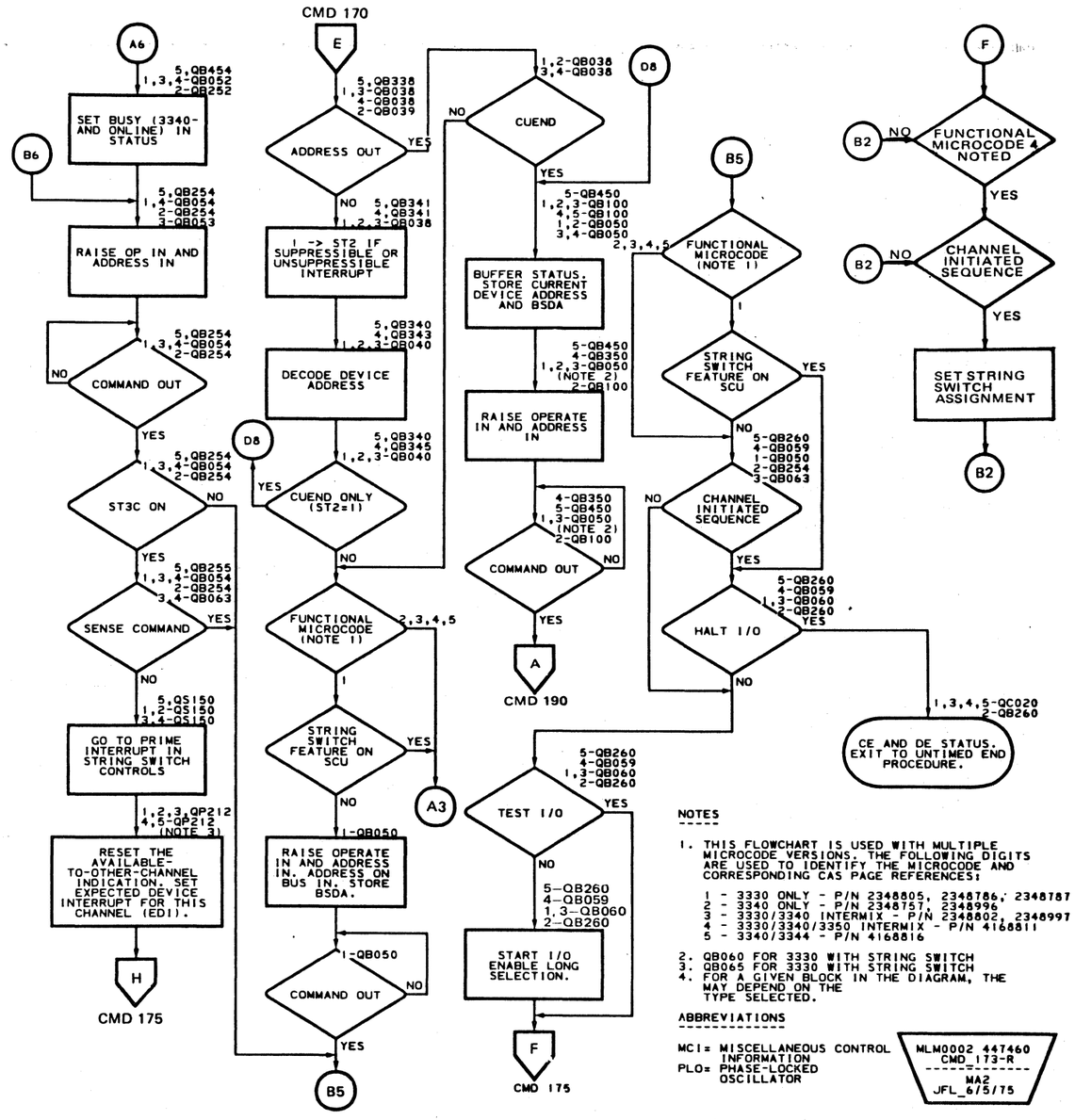
ABBREVIATIONS

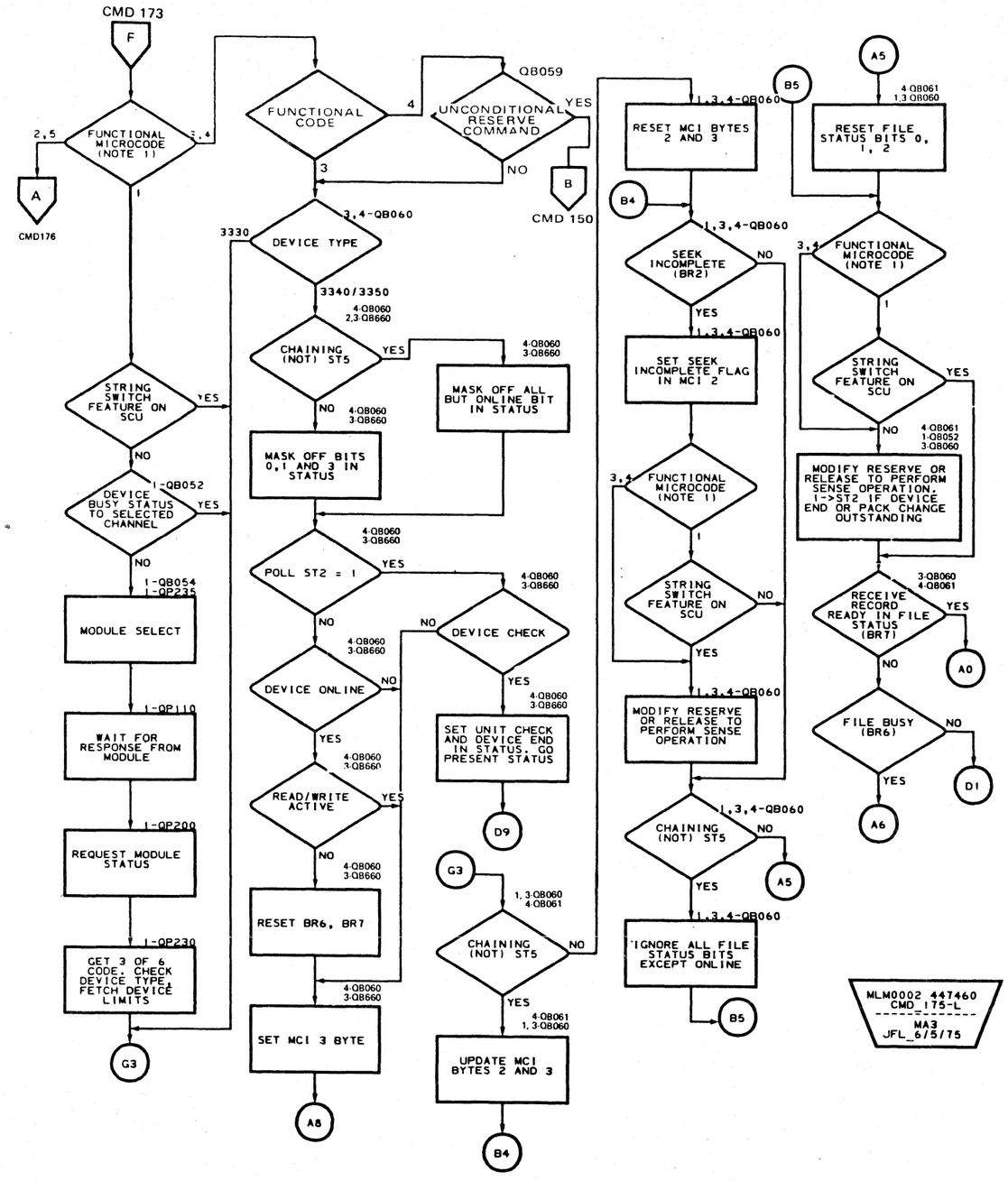
BSCA = BIT SIGNIFICANT CONTROLLER ADDRESS
BSDA = BIT SIGNIFICANT DEVICE ADDRESS
DCC = DISCONNECTED COMMAND CHAINING
EDI = EXPECTED DEVICE INTERRUPT
ODE = OUTSTANDING DEVICE END
PCH = PACK CHANGE

MLM0002 447460
CMD_170-R
MAO
JFL_6/3/75

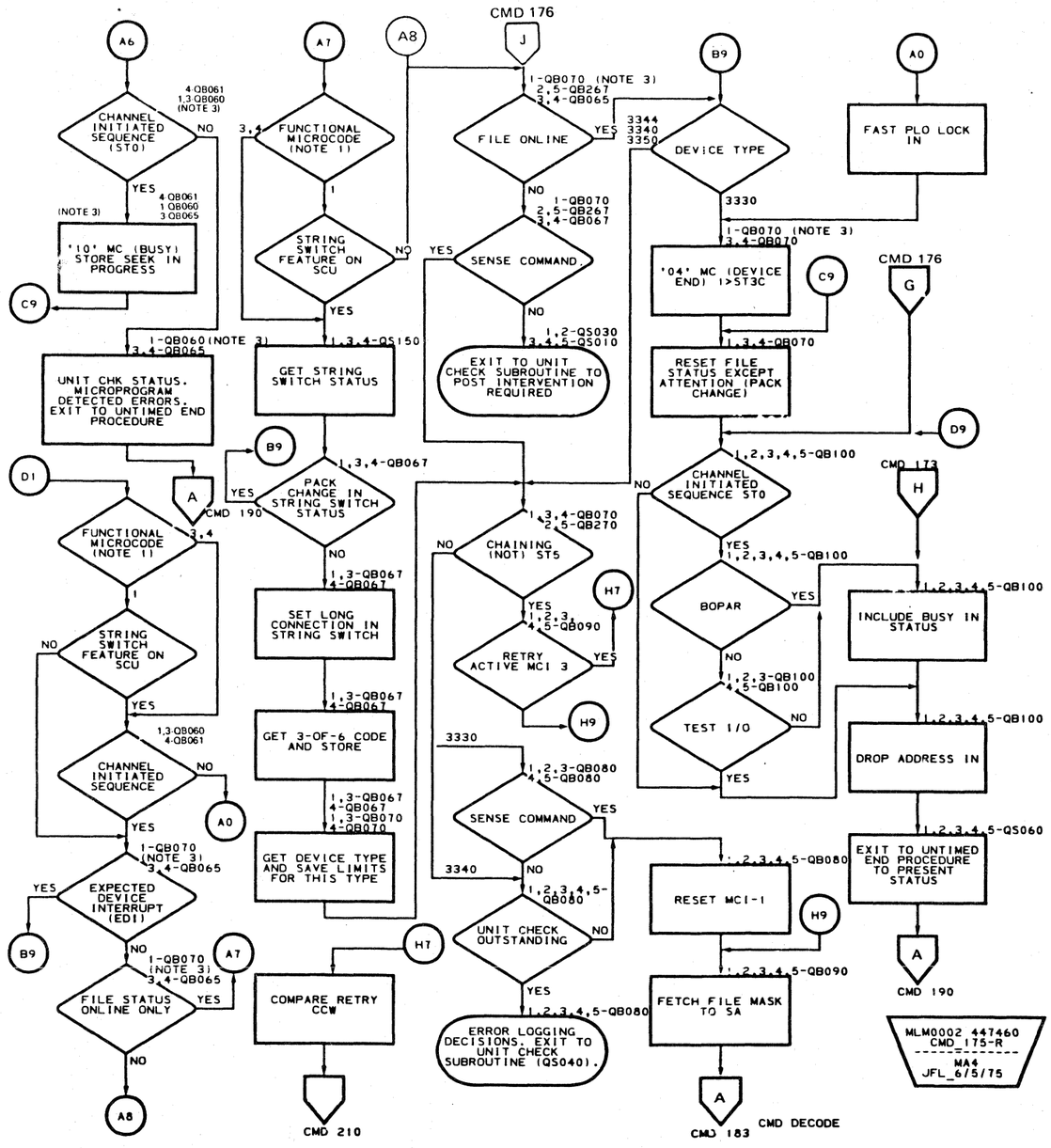
POLLING IDLE LOOP AND INITIAL SELECTION (Part 2 of 4)





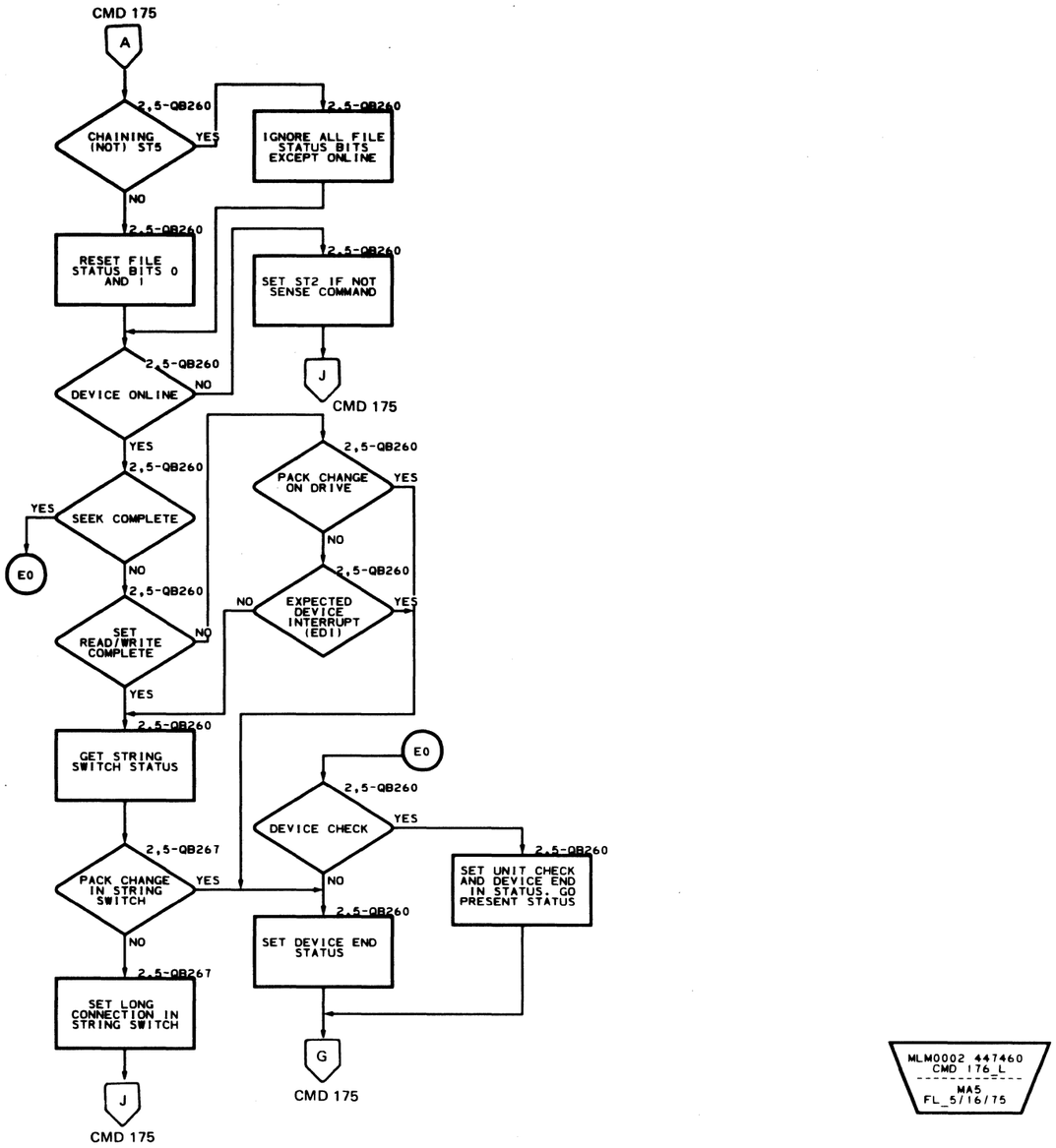


BX1600 Seq 2 of 2	2347209 Part No. (8)	See EC History	447461 12 Mar 76	447463 16 Dec 76				



POLLING IDLE LOOP AND INITIAL SELECTION (Part 4 of 4)

POLLING IDLE LOOP AND INITIAL SELECTION (Part 4 of 4)



MLM0002 447460
CMD 176_L
MA5
FL_5/16/75

BX1650	2354814	437417	447460	447461				
Seq.1 of 2	Part No. (8)	15 Apr 74	19 Dec 75	12 Mar 76				

STATUS INFORMATION (Part 1 of 2)

- The status byte (eight bits) notifies channel of the condition of the CU and the selected drive.
- Status is presented twice (initial and ending) for all SCU commands except Seek, Set Sector (if RPS installed), and the immediate commands.
- Status is presented three times by Seek Cylinder commands (which cause access motion).
  1. Initial.
  2. Channel End after data transfer from the CPU.
  3. Device End after the device has stopped seeking (gated attention).
- Status is presented once (initial) containing Channel End and Device End on immediate commands (No-Op) except when chained after a Write command. In this case a second status byte (ending) is also transmitted.

  No-Op is processed as an immediate command only if the control unit is not writing or erasing. Channel End and Device End are indicated in the initial status byte (one status byte only). If the unit is writing or erasing, 0 is transmitted in the initial status byte. Channel and Device End are indicated in the ending status byte when SCU finishes writing or erasing.

1 STATUS MODIFIER

- Set when a Search High, Search Equal, or Search High or Equal command is completed and the condition satisfied.
- Indicates CU Busy when on in conjunction with the Busy bit. When on with Channel End, Device End and Unit Check, indicates retry of last channel command. The CU and drive are ready for immediate retry.
- Indicates retry of last channel command when on in conjunction with Unit Check bit. When on with Channel End, indicates retry of last channel command. The CU and drive are not ready for the retry procedure.

2 CONTROL UNIT END

- Set when a CU Busy was generated previously and the busy condition is terminated.

3 BUSY

- Set when a new command chain is initiated while the selected access mechanism is still in motion because of a previous Seek command.
- Set in response to any command except Test I/O if there is outstanding status for the device.
- Set when a new command chain is initiated while the CU is causing a track to be erased following a Format Write command or an Erase command.
- Indicates that only the selected device is busy if the status modifier is off.
- Indicates CU busy if on in conjunction with the status modifier (bit 1).

Status Byte

Bit	Name	Function
0	Attention	Not used
1	Status Modifier	Used with Channel End, Device End, Busy, and Unit Check
2	Control Unit End	The CU has finished an operation
3	Busy	Access mechanism in the addressed drive is moving. Also used in conjunction with status modifier to indicate CU busy.
4	Channel End	The CU has received all the data needed to do the operation called for and the channel is free
5	Device End	Indicates that an access mechanism is free to be used
6	Unit Check	Indicates that an unusual or error condition has been detected. With status modifier, it means command retry is requested.
7	Unit Exception	End of file

4 CHANNEL END

- Set when the channel portion of the operation is completed.

5 DEVICE END

- Set when a device is ready after a Seek is completed.
- Set when the record is ready to be operated on after a Set Sector command (if RPS installed).
- Set when an attached device goes from a not ready to a ready condition.
- Set simultaneously with Channel End at the end of all other commands.
- Indicates that an access mechanism is free to be used.

6 UNIT CHECK

- Set whenever an unusual or error condition on the selected drive is detected in the CU.
- Indicates command retry requested if on in conjunction with status modifier.
- Indicates a system interrupt condition if status modifier is not on and Channel End (bit 4) and/or Device End (bit 5) is included in status. The sense bytes provide detailed information about the condition.

7 UNIT EXCEPTION

- Set when the data length in the count field is zero.
- Indicates that an End of File was detected during a Read IPL, Read R0, Read CKD, Read KD, Read D, Write KD, Write D, or Search KD command. It is not set for Read count, Write CKD, Search Key or Search ID commands. The key field, if any, is transferred.

STATUS INFORMATION (Part 2 of 2)

INITIAL STATUS BYTE

The initial status byte is zero for all nonimmediate commands and Test I/O unless one or more of the following conditions exist. If more than one condition exists, the first condition listed determines the initial status byte:

1. The initial status indicates Control Unit Busy (Bit 3) if selection occurs and if:
   a. Writing is still in progress after chaining is terminated.
   b. An operation is still in progress after a Halt I/O occurs.
   c. The CU is disconnected during command chaining with writing in progress or with a CU error recovery procedure in progress.
   d. The CU is executing a microprogram diagnostic test.
   e. A status condition is pending in the CU for other than the addressed device.
   f. A system reset sequence is in progress.
   g. The CU is maintaining a contingent connection to some device other than the addressed device.
2. A status condition, pending in the CU, is associated specifically with the addressed device or is not associated with any specific device. In this case, the pending status is presented as initial status, and the busy bit is included in the status byte if the command byte is other than Test I/O. The busy bit indicates that the device is busy because of the outstanding status. The pending status is cleared unless it is stacked by the channel. After the status is cleared, the device must be readdressed to determine if the device is available.
3. The device is busy to the interface, in which case the busy bit appears alone in the initial status byte. The device is busy to the interface if Channel End occurred without Device End for the device, and Device End has not yet been generated; or if the device is attached to a controller with the string switch feature and is reserved to the other side of the switch. Discussion in this paragraph does not apply to cases where busy (pending status) occurs with other status bits. When busy occurs with bits other than status modifier, the device is defined to be busy because of the included status, which is outstanding.
4. Status pending in the device. The pending status is presented as initial status, and the busy bit is included if the command is other than Test I/O. The pending status is cleared unless it is stacked by the channel.
5. A Unit Check condition exists at the device or CU. Unit Check occurs in initial status. Valid commands in the sense group (xxxx0100) are an exception and receive zero status so that the commands may be executed. This permits transferring of the sense indicators.
6. Initial status indicates command retry.
7. Invalid parity is sensed in the command byte. Unit Check occurs.
8. The command is rejected. Unit Check occurs. (Not all command rejects occur in initial status however.)

PENDING STATUS CONDITIONS

A pending status condition may exist in either the device or the CU.

Status Pending in the Control Unit

A status condition pending in the CU, other than Control Unit End, causes the CU to appear busy for all devices except the device for which the status condition exists. The condition causes the Request In signal to rise if the CU is not busy to the interface, Select Out is down, and Suppress Out is down. A pending Control Unit End may cause the CU to appear busy to all except one device address on the interface for which it is pending. Status pending in the CU is cleared when it is presented and accepted.

Note that status cannot be cleared from the CU by a Test I/O if the CU is busy to the interface.

Status is pending in the CU if:

1. An interface disconnect was signaled after a command was given but before Channel End was accepted by the channel for the command. The ending status for the operation is pending when the operation is complete.
2. Status containing Busy, Channel End, or Unit Check was stacked by the channel, or blank status in response to a Test I/O was stacked. The stacked status is pending in the CU for the device with which the stacking occurred.
3. Control Unit Busy was presented to the interface. Control Unit End is pending for the interface and is included with other status pending in the CU, if any.
4. A Unit Check was detected associated with an operation where Device End has already been cleared. Unit Check and Control Unit End are pending in the CU.

Address Associated with Pending Status

All status conditions in the device are associated with a specific device address, except for Control Unit End. However, when in the contingent connection state, Control Unit End is associated with a specific address, and that address is the last address presented on the interface by the CU. When no contingent state exists, the Control Unit End is associated with the smallest numerical device address on the highest possible controller address which is not command chaining on any interface.

Status Pending in the Device

A status condition pending in the device causes Request In to rise on the interface if the device and CU are available (not busy), Select Out is down, and no contingent connection exists in the CU. Status pending in the device is cleared when status is presented and accepted. Status pending in the device cannot be cleared by a Test I/O if the device or CU appears busy to the interface. The only status condition which can be pending in the device is Device End. When Unit Check occurs with Device End (and not Channel End) it is not generated until the Device End is presented on the interface, and the Device End and Unit Check conditions then become pending in the CU if stacked. Status is pending if:

1. Channel End occurs alone for an operation. Device End is pending.
2. Busy status (busy bit alone) is presented. Device End is pending on the interface.
3. The device has gone from the not ready state to the ready state. Device End is pending.

Priority of Pending Status Conditions

The priority of pending status conditions when presented via polling is:

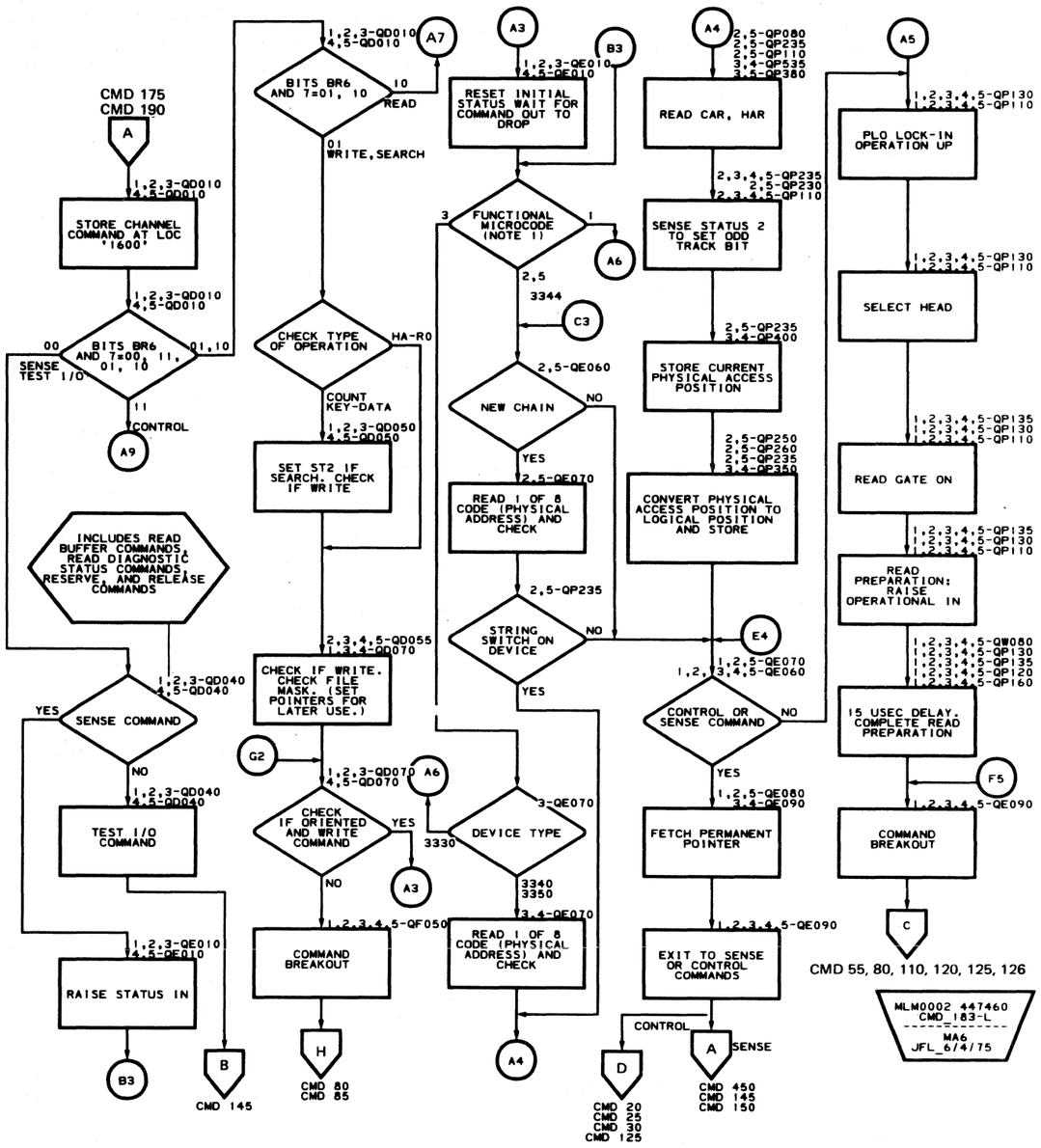
1. Status pending in the CU, other than Control Unit End.
2. Unsuppressible status conditions.
3. Suppressible Device End status.
4. Control Unit End status.

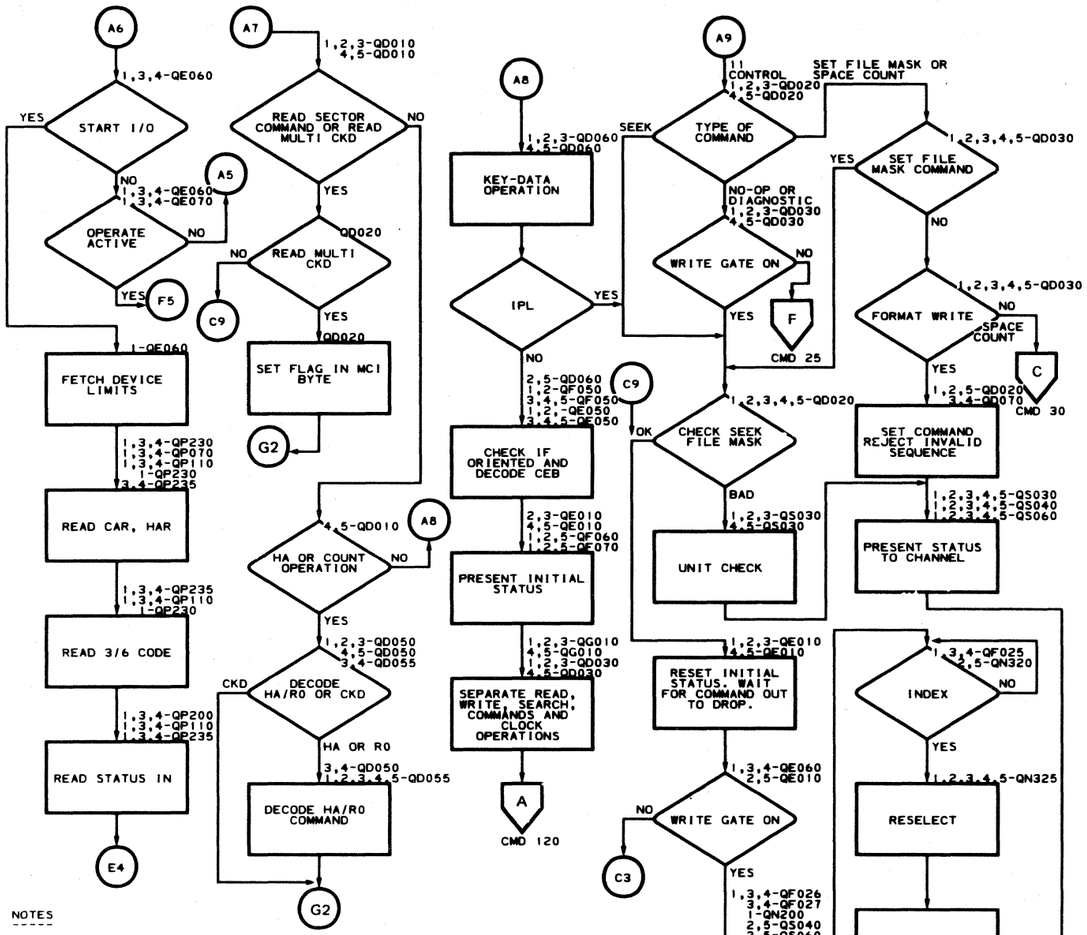
Note: During the contingent connection state, Control Unit End status assumes highest priority in the preceding table.

The microcode supporting 3350 Control Unit End is associated with the smallest numerical device address on the last controller used by a control unit which is not command chaining on any interface. In the non-contingent case status can be cleared by addressing any device attached to the control unit.

COMMAND DECODE

- Decode the command byte from the channel.
- Check if valid command and command sequence.
- Break out to individual command flowcharts.





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   3 - 3330/3340 INTERMIX - P/N 2348802,2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816

2. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

ABBREVIATIONS

CAR = CYLINDER ADDRESS REGISTER
CEB = COMMAND EXECUTION BYTE
CKD = COUNT-KEY-DATA
HA = HOME ADDRESS
HAR = HEAD ADDRESS REGISTER
IPL = INITIAL PROGRAM LOAD
PLO = PHASE-LOCKED OSCILLATOR
R0 = RECORD ZERO

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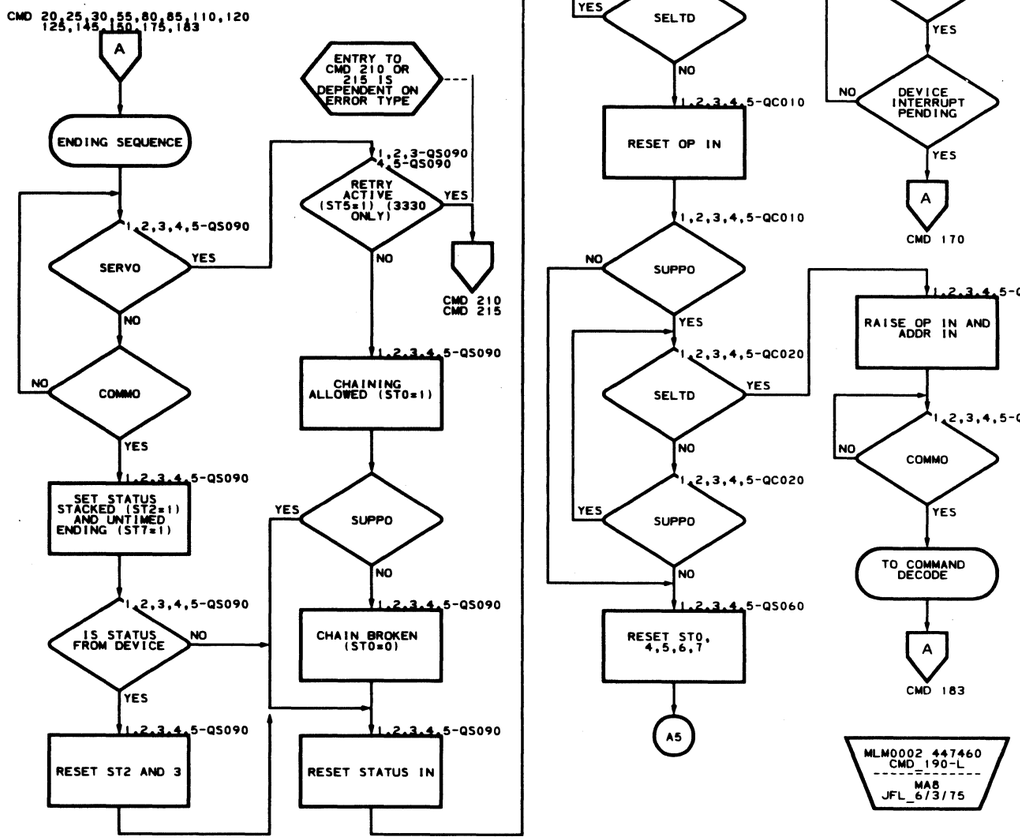
ENDING SEQUENCE

OBJECTIVES

- Present ending status to the channel.
- Check if chaining.
- If oriented and chaining, perform timed initial selection routine.
- Complete read/write housekeeping functions.
- Update interrupt and available bytes.
- Make exit decisions.



DISCONNECTED COMMAND CHAINING

- Allows the CU to disconnect from the channel on commands that require long delays because of mechanical motion or searches. The channel is free during the delay period.
- Disconnected command chaining enables multiple requesting, which allows up to 16 (32 if 32-drive expansion feature is installed) separate command chains to be active in the facility.

Disconnected command chaining allows the CU to disconnect from the channel after an operation, such as Seek or Set Sector, has started even though chaining is indicated.

Since burst mode is not forced during the execution of Seek or Set Sector commands, the CU can disconnect between Channel End and Device End. The disconnect function reduces the CPU interrupts needed to overlap channel data transfers with mechanical motion of the devices. The CU retains the information necessary to control a disconnected CCW chain for each drive in the facility. In effect, the CU is capable of simultaneously executing up to 32 CCW chains (one per drive). ***Note: This is also referred to as multiple requesting.*** During a Seek operation, the CU attempts to reconnect after mechanical motion is completed. During a Set Sector operation, the CU attempts to reconnect when the desired rotational position is detected. In either case, the channel is made available during access motion and rotational delay periods. Disconnect is also allowed on command retry procedures (3330 and 3350) and for format write padding of 0s.

Two examples of disconnected command chaining:

Disconnect command chaining can involve two or more channels, or one channel may have several CCW chains.

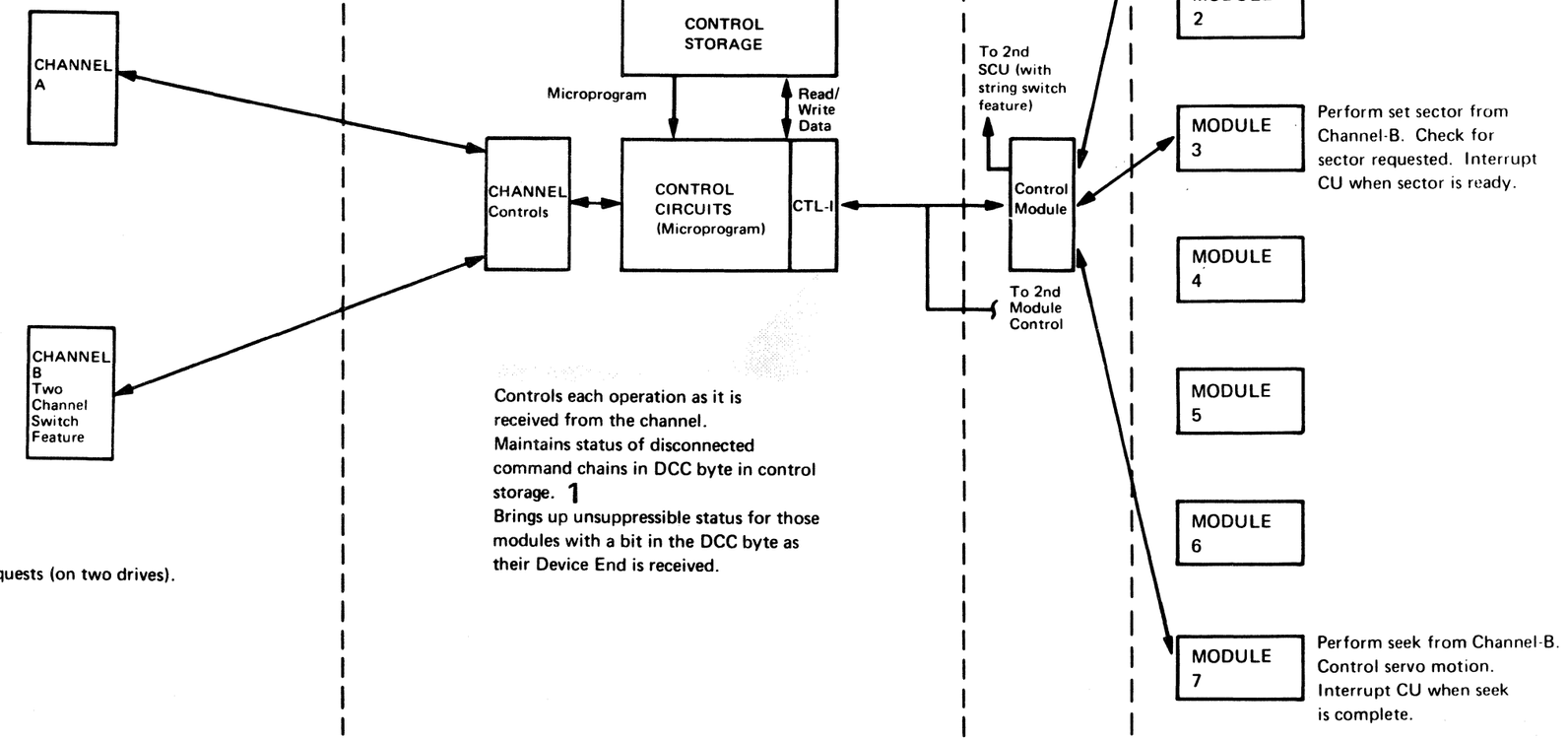
CHANNEL A
1. Issues Seek command to module 0.
2. Disconnects until Device End (seek complete) is received.

CCW Chain Example– Module 0
1. Seek–Locate cylinder
   Disconnected
2. Set Sector–Locate area on track.
   Disconnected
   Search ID–Locate a record.
   TIC – 8
   Write Data–Write data field

CHANNEL B
1. Issues Seek command to module 7.
2. Disconnects until Device End (seek complete) fr module 7 is received.
3. Issues Set Sector command to module 3.
4. Disconnects from this chain until Device End from module 3 (sector is ready) is received.

CCW Chain Example–Module 7
1. Seek–Locate cylinder
   Disconnected
2. Read Home Address–Read Home Address field.
   CCW Chain Example–Module 3
   Seek–Locate cylinder
   Disconnected
3. Set Sector–Locate record.
   Disconnected
   Search ID–Locate record.
   TIC –8
4. Read Key Data–Read key and data fields.

} Multiple requests (on two drives).

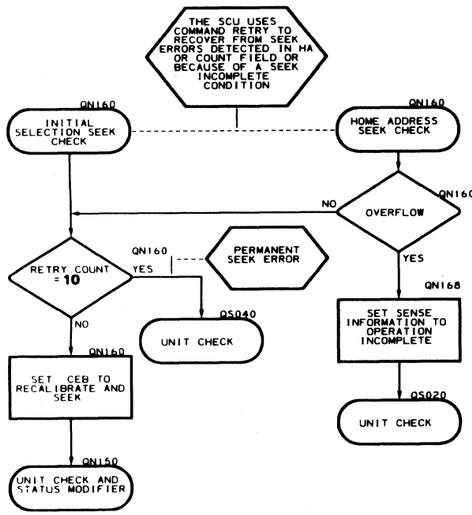


COMMAND RETRY (3330 AND 3350) (Part 1 of 3)

Command retry permits error recovery without requiring intervention from the using system. The CU resorts to command retry for the following conditions:

A SEEK MALFUNCTIONS

The SCU will attempt to recover from seek errors when home address is clocked or because of a Seek Incomplete condition. If, during a Seek operation, a Seek Incomplete condition occurs or a Seek Error is detected while reading home address or processing a count field, the CU sets the command execution byte (CEB) to recalibrate and seek. The CU then retries the Seek. Unit Check and Status Modifier indications are present in the sense information. The retry is attempted up to ten times and a permanent seek error is posted to the system, where error recovery procedure (ERP) can be invoked.



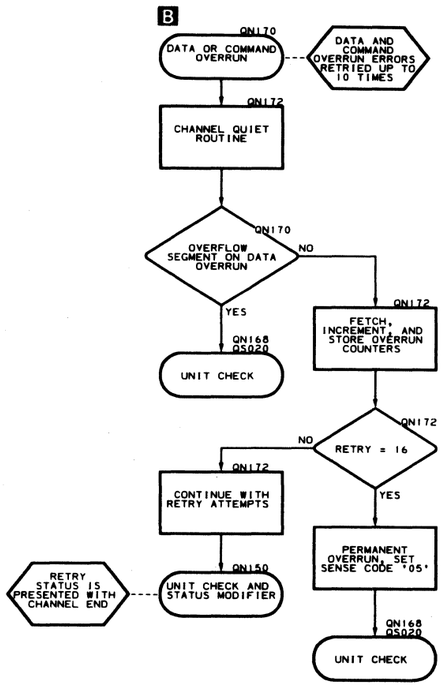
ABBREVIATIONS

CEB = COMMAND EXECUTION BYTE
MCI = MISCELLANEOUS CONTROL INFORMATION

B DATA OR COMMAND OVERRUN

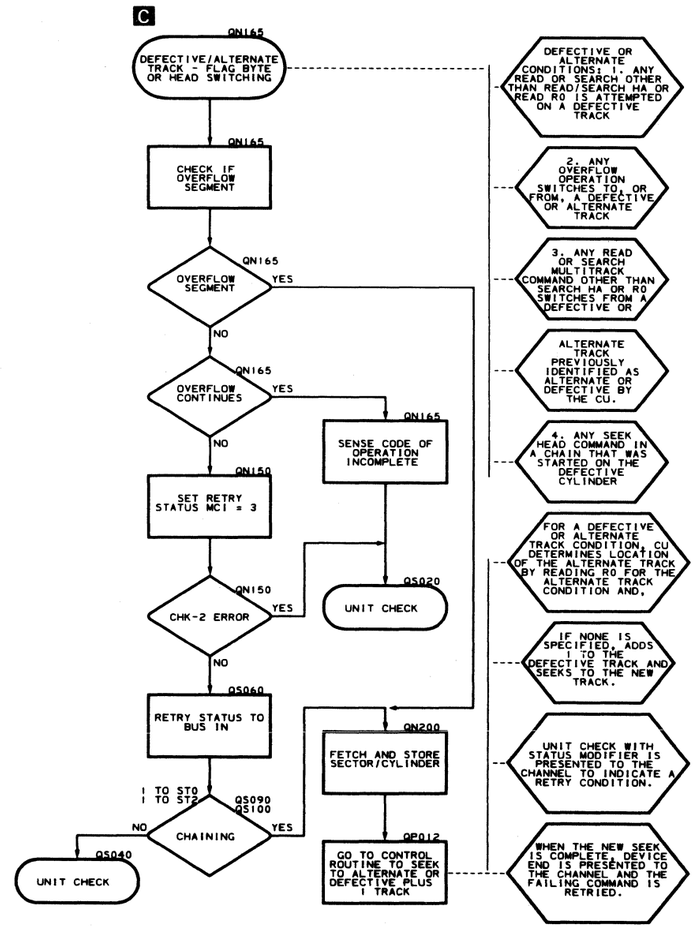
If data or commands are not processed in a normal sequence at the proper time, they can be lost.

Note: If 3350 command retry pages differ from 3330, they are shown in parentheses.



C DEFECTIVE OR ALTERNATE TRACK

When the CU detects a defective or alternate track condition before data transfer starts, command retry will be invoked. The CU determines the location of the defective/alternate track and seeks to the appropriate track. After the Seek is completed, Device End is presented and the command is reissued. The CU processes the command normally, verifies the correct access, and continues with the user's command chain.



D DATA ERROR

Correctable Data Error Not in Data Fields (3330)*

If a data error is detected at the completion of a Read or Search in the count or key fields, and it is correctable, CU signals retry status to the channel. Then the CU reorients on the failing track and signals Device End to the channel to begin retry. The failing field, which was buffered in control storage, is corrected by the CU.

Processing a reissued Read command in the count or key fields causes the corrected data from control storage to be transferred to the channel; the CCW then continues. For a search in the count or key fields, the CU executes a compare against the corrected data in control storage and continues with the CCW. When clocking in a count field, the corrected data is used only by the CU.

*For 3350, data errors in all fields except data fields are treated as uncorrectable.

Uncorrectable Data Errors

If a data error is detected at the completion of a Read, Clock, or Search operation and it is uncorrectable, the CU signals Retry Status to channel with Unit Check and Status modifier. Then the CU reorients on the failing track location, and signals Device End; the channel reissues the command. The retry is attempted up to 28 times and Unit Check is posted to the system where ERP can be invoked.

Command retry is not used for uncorrectable data errors occurring during the clocking of a key field.

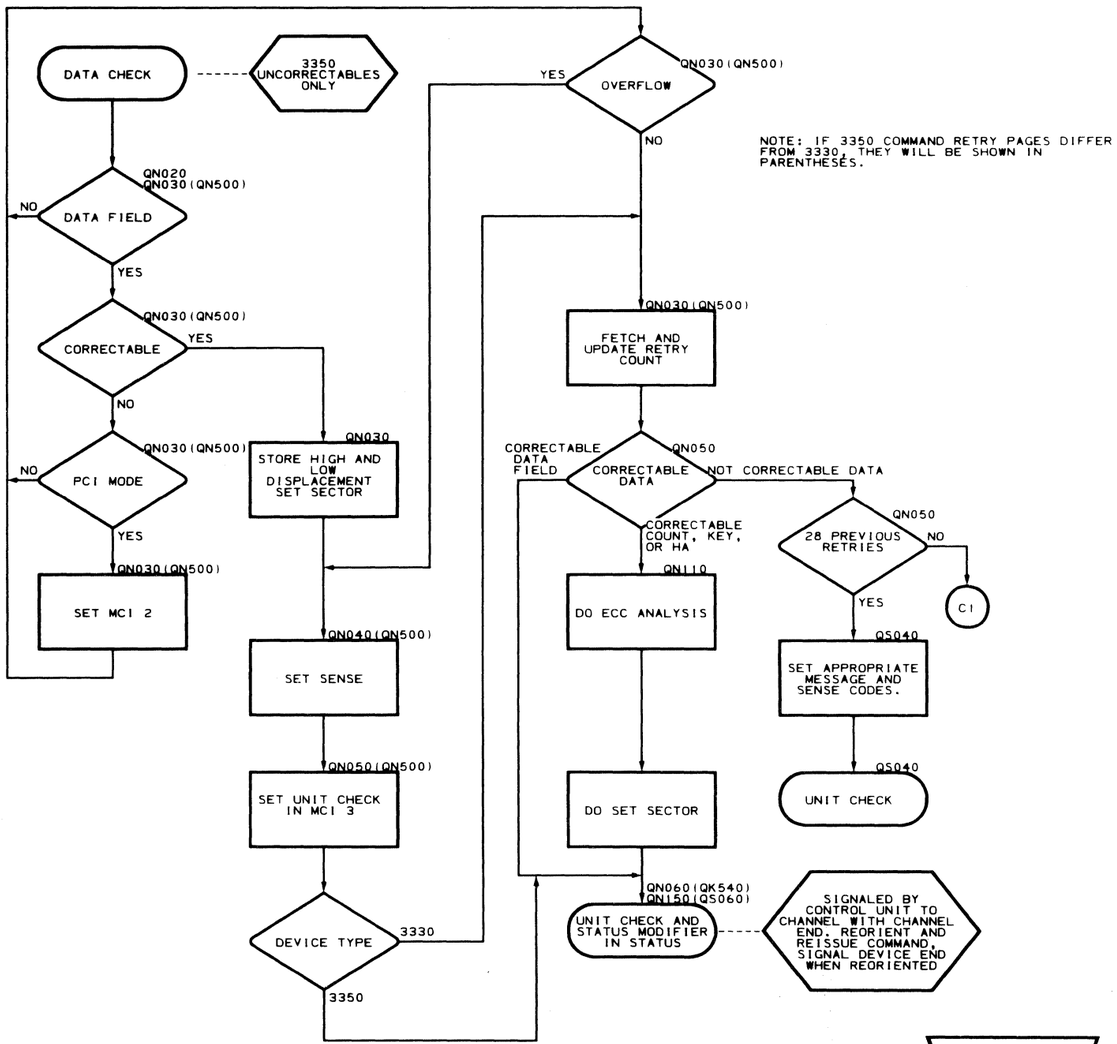
When an error is determined as uncorrectable, the CU attempts to recover by offsetting the read heads from normal track position on 3330 only. There is no offsetting for 3350.

After the head shift is made, the CU orients on the record and tries to read it. If, after any retry, the error becomes correctable, the CU proceeds as if a correctable error were detected.

Correctable Data Errors in Data Fields

Correctable data errors in the data field are corrected by the system ERP using correction information sent to the channel in the sense data. (See SENSE 1.)

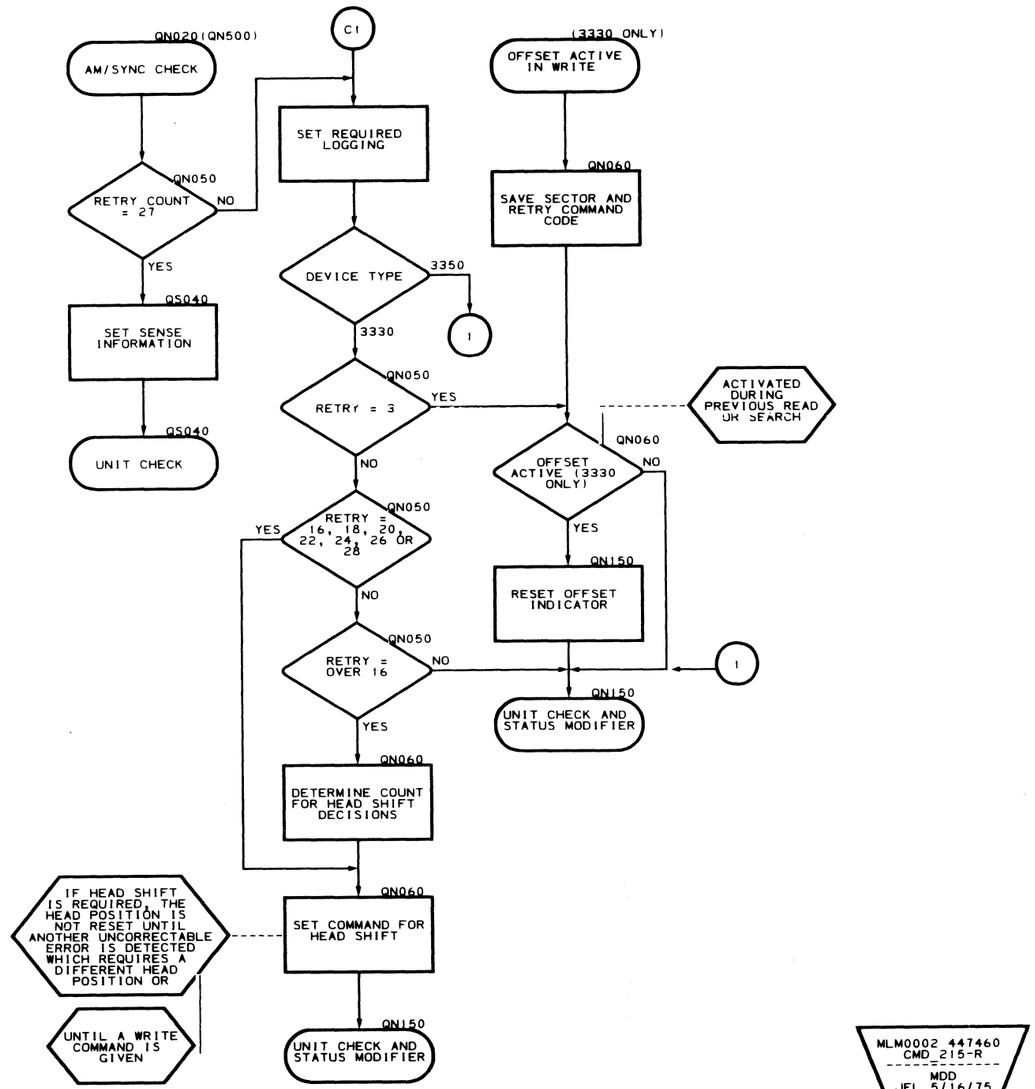
COMMAND RETRY (3330 AND 3350) (Part 2 of 3)



NOTE: IF 3350 COMMAND RETRY PAGES DIFFER FROM 3330, THEY WILL BE SHOWN IN PARENTHESES.

ABBREVIATIONS

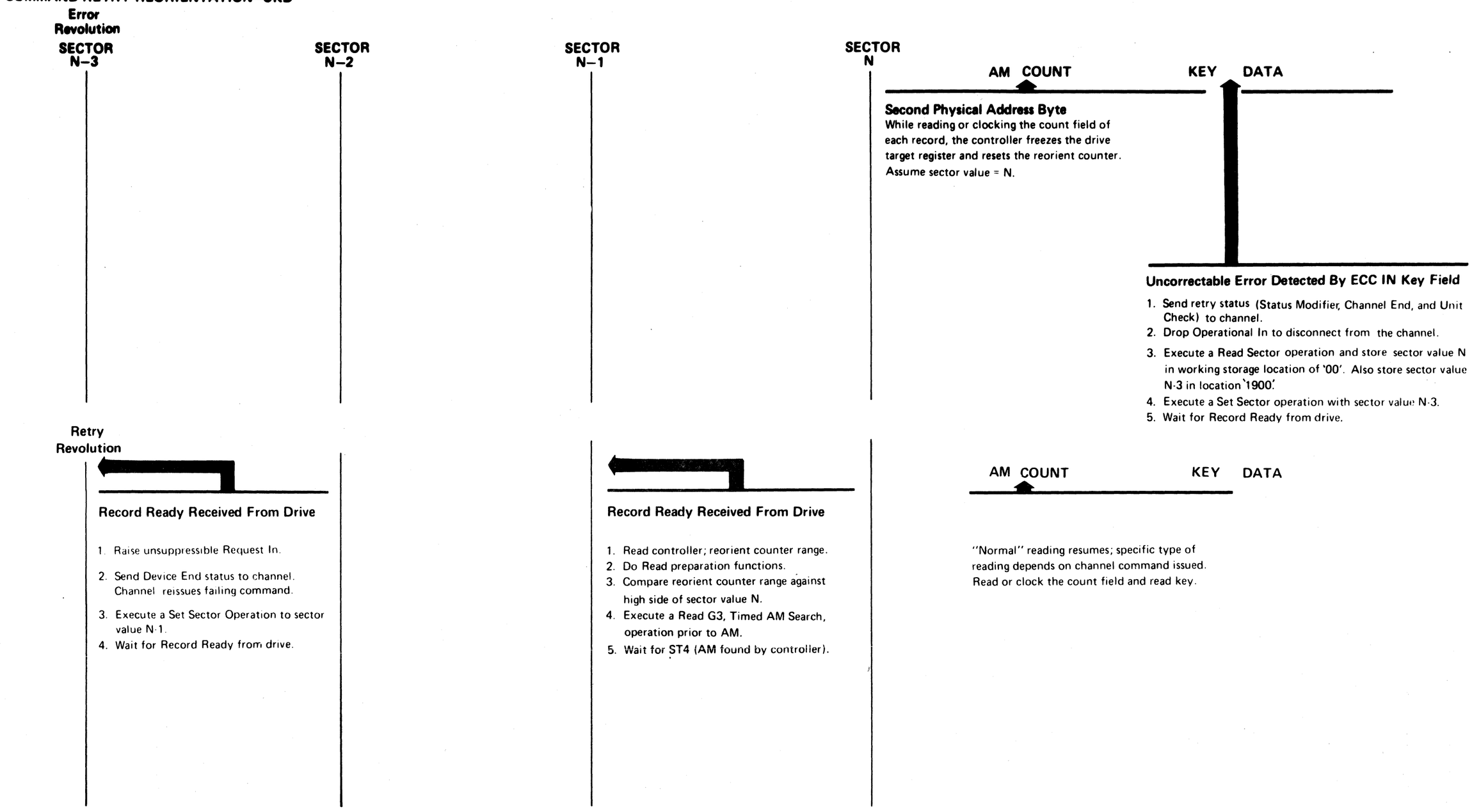
AM = ADDRESS MARKER
ECC = ERROR CORRECTION CODE
MCI = MISCELLANEOUS CONTROL INFORMATION
PCI = PROGRAM CONTROL INTERRUPT



COMMAND RETRY (3330 AND 3350) (Part 3 of 3)

COMMAND RETRY (3330 AND 3350) (Part 3 of 3)

COMMAND RETRY REORIENTATION–CKD



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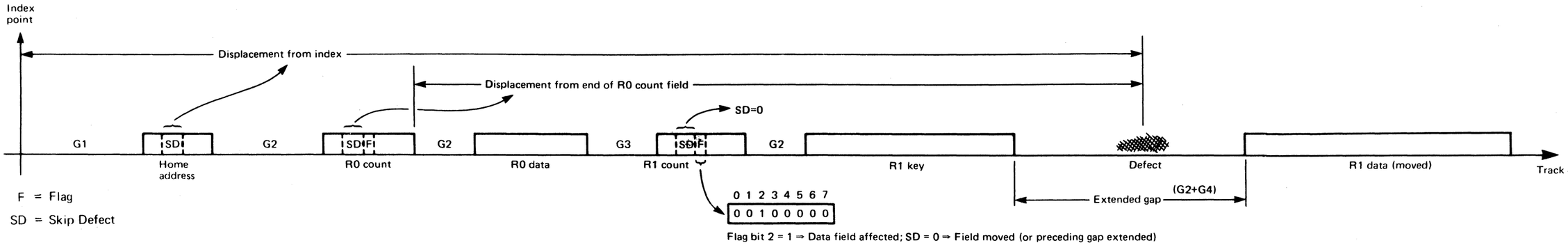
437402A 15 Mar 72	437404 23 Jun 72	437405 15 Aug 72	437415 2 Nov 73	437417 15 Apr 74	447460 19 Dec 75	

DEFECT SKIPPING EXAMPLES (3340 ONLY)

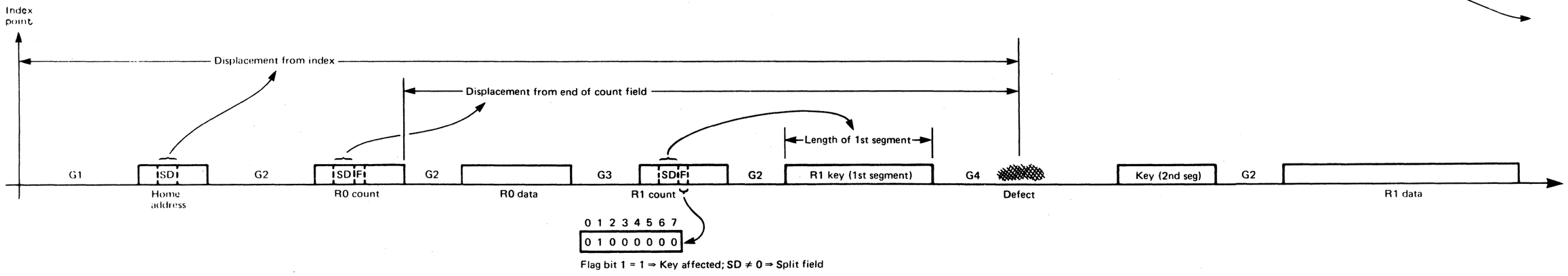
Note: 3350 is similiar, however, there are 3 sets of SD bytes. Three defects per logical track may be skipped. In this case, a field could be moved more than once or moved and split.

EXTENDED GAP



SD = 0 in all count fields that lie beyond the defect

SPLIT FIELD



RESETS (Part 1 of 3)

- Set up machine to start microprogram control.
- Store error information for later use on a sense-type command. Refer to CTRL 650 for control storage layout.

There are four types of resets:

POWER-ON RESET

Power-On Reset is automatically actuated during any power-on sequence of the subsystem. After reset, the instruction address register (IAR) contains address '0000'. Depending on the Mode switch setting, the SCU either remains stopped or starts on Initial Microprogram Load operation.

PUSH BUTTON (MANUAL) RESET

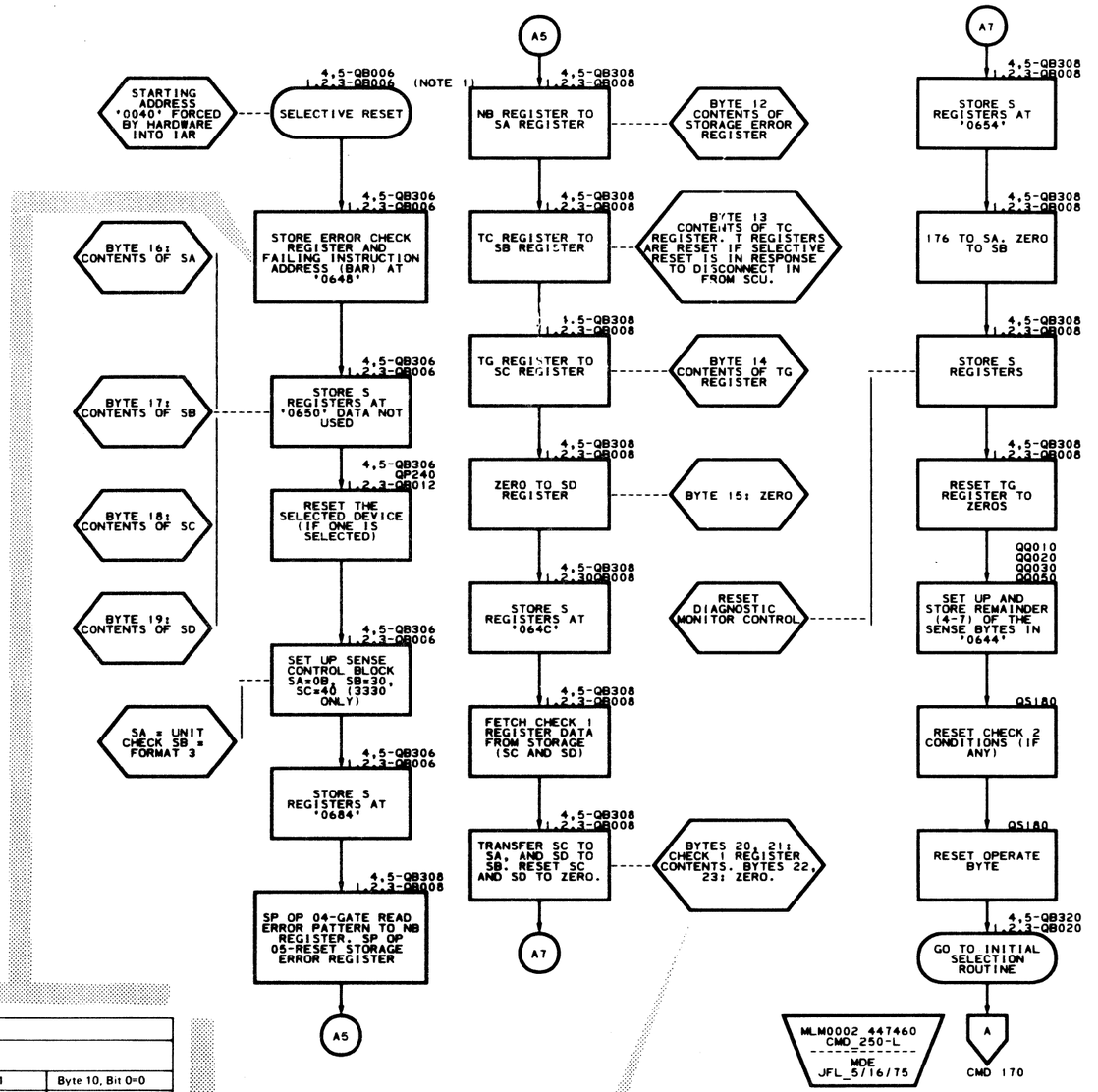
If the Mode switch is in any of three CE modes, pressing the Reset push button resets the subsystem. The subsystem clock remains stopped until restarted.

SELECTIVE RESET

When the using system actuates the Selective Reset line, the IAR is forced to hex address '0040'. This address is the start of a store routine which will save the check 1 error latches and the backup register (which contains the address of the last executed instruction). The selected device, if any, is reset. Unit Check is presented in response to the next Start I/O instruction.

SYSTEM RESET

When the using system actuates the System Reset line, the IAR is forced to hex address '0000'. This address is the start of a reset sequence that returns the subsystem to a zeroed condition.



Stored Data Available to System on Sense I/O Command (See SENSE 20)						
Bytes 8 and 9	Byte 10 (20) Check 1 Register			Byte 11 (21) Check 1 Register		
Backup address register (address of control storage word addressed when error was detected).	0	Bit 0 = 1	Bit 0 = 0		Byte 10, Bit 0 = 1	Byte 10, Bit 0=0
	1	Clock Error	Clock Error	0	Zero	Stor Addr Bus 0–7
	2	CA Decode Even	CS Decode	1	Stor Multiple Read Error	Stor Addr Bus 8–15
	3	CA Decode Odd	Zero	2	ECC Logic Error	Stor Write Bus 0/2
	4	CB Decode Even	A Register	3	Zero	Stor Write Bus 1/3
	5	CB Decode Odd	B Register	4	Cycle Control	BSM Low Error
	6	Branch/Status	ALU	5	CD Decode	BSM High Error
	7	Special Operation	23FD Parity	6	Zero	23FD Not Ready
				7	Zero	Zero

NOTES

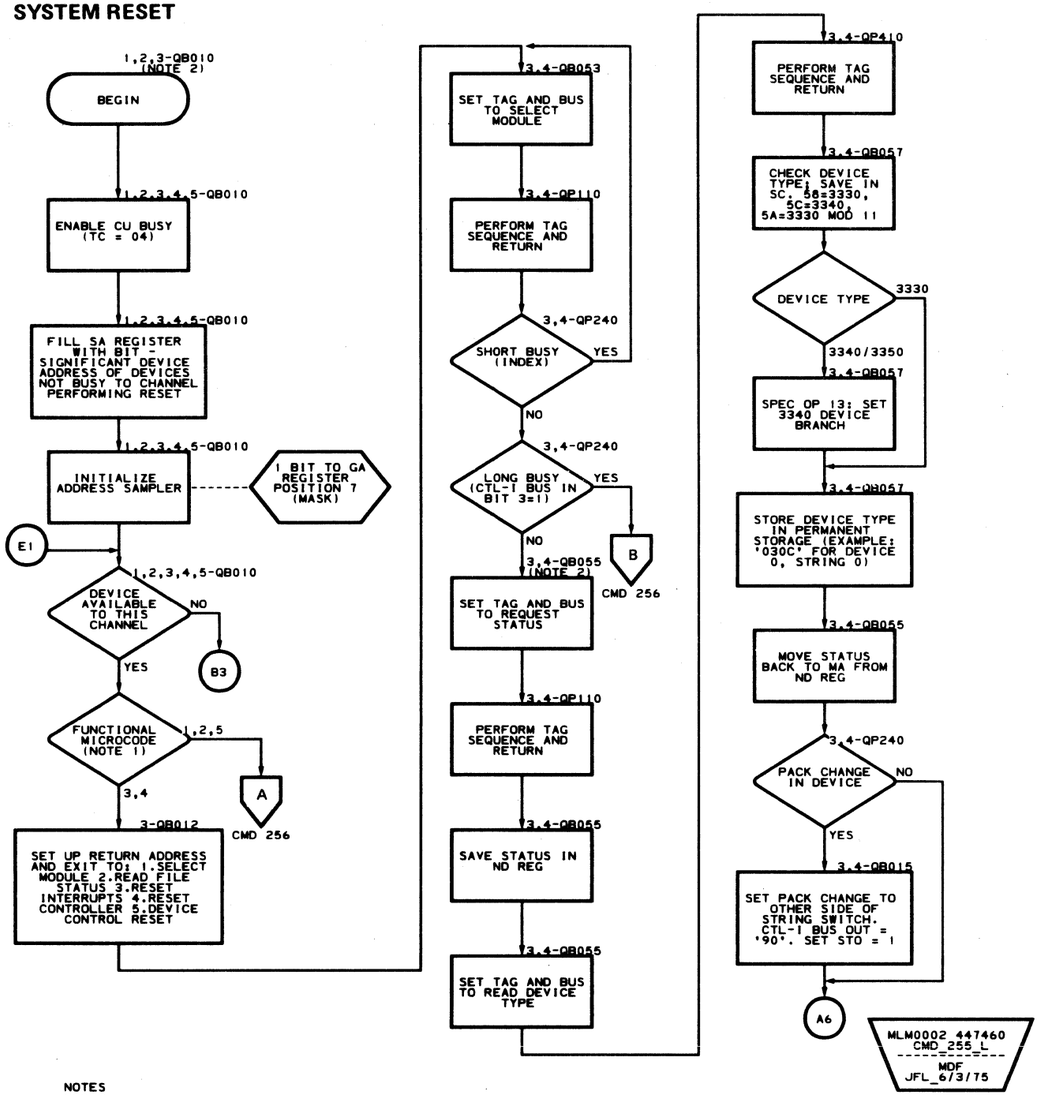
1. QB0XX REFERENCES BECOME QB3XX IF TWO CHANNEL SWITCH ADDITIONAL IS INSTALLED.

ABBREVIATIONS

BAR = BACKUP ADDRESS REGISTER
IAR = INSTRUCTION ADDRESS REGISTER

RESETS (Part 2 of 3)

SYSTEM RESET



NOTES

1. THIS FLOWCHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:
   1 - 3330 ONLY- P/N 2348805, 2348786, 2348787
   2 - 3340 ONLY - P/N 2348751, 2348996
   3 - 3330/3340 INTERMIX - P/N 2348802, 2348997
   4 - 3330/3340/3350 INTERMIX - P/N 4168811
   5 - 3340/3344 - P/N 4168816
2. QB0XX REFERENCES BECOME QB3XX IF TWO CHANNEL SWITCH ADDITIONAL IS INSTALLED.
3. QB0XX REFERENCES BECOME QB4XX IF 3340/3344 IS INSTALLED.
4. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

ABBREVIATIONS

DCC = DISCONNECTED COMMAND CHAINING
PCH = PACK CHANGE

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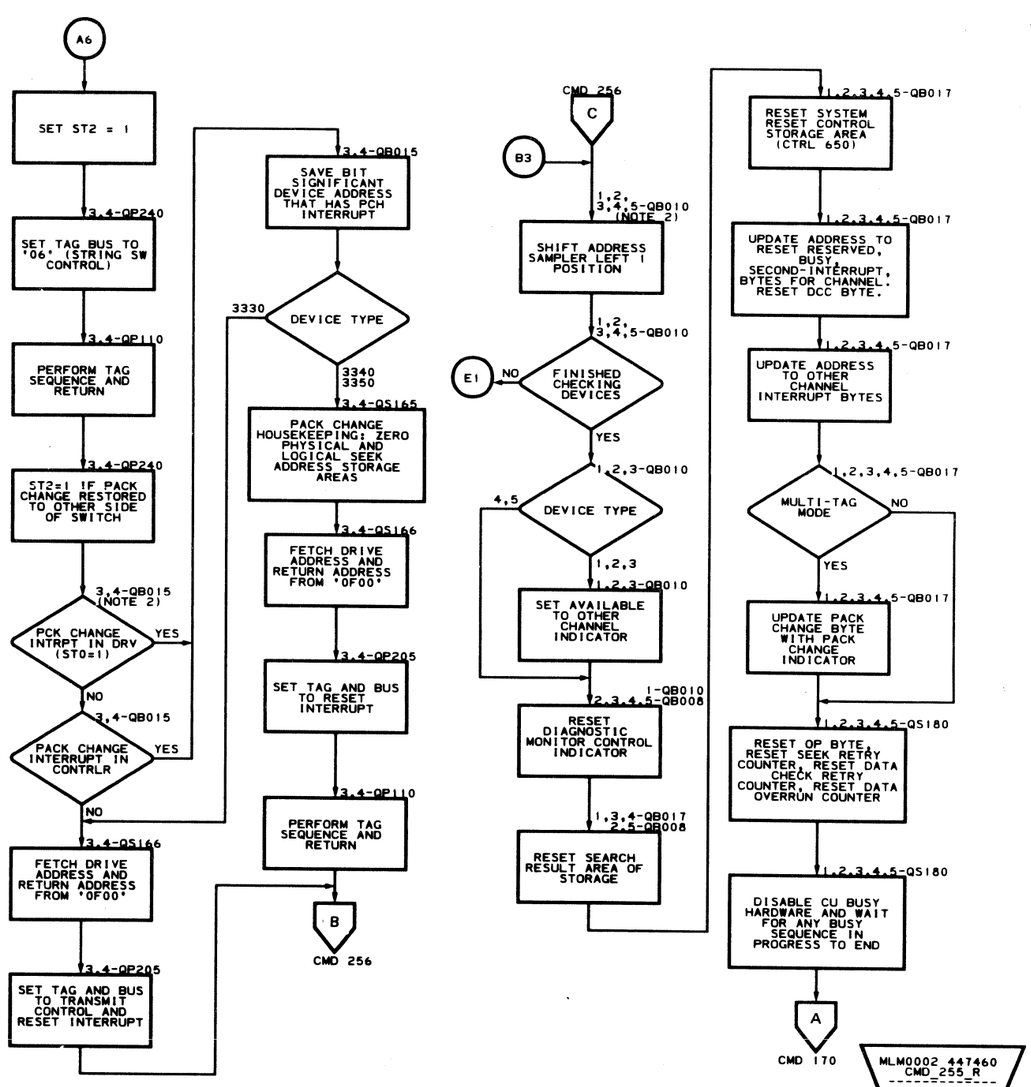
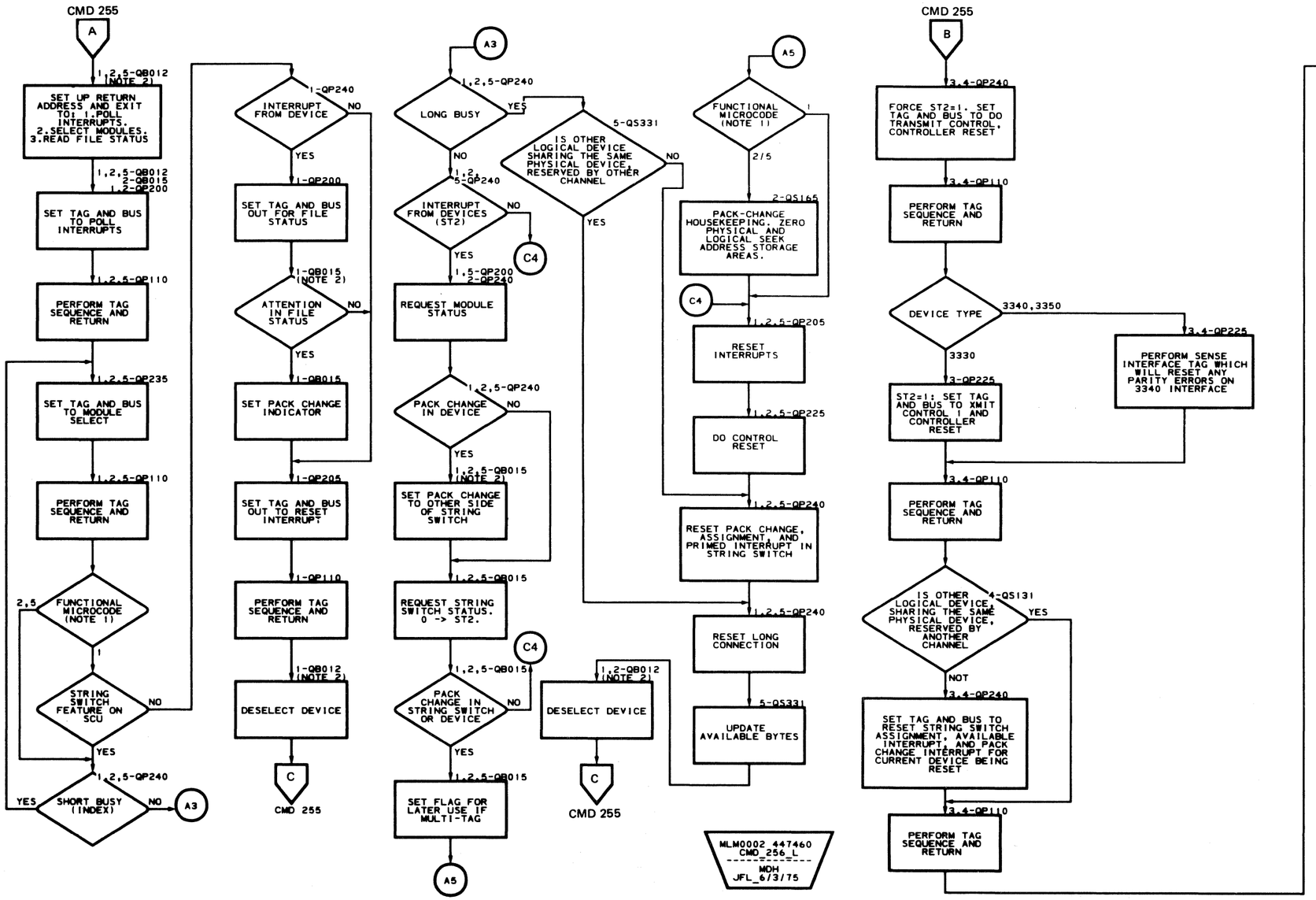


RESETS (Part 3 of 3)

SYSTEM RESET (continued)



NOTES

1. THIS FLOW CHART IS USED WITH MULTIPLE MICROCODE VERSIONS. THE FOLLOWING DIGITS ARE USED TO IDENTIFY THE MICROCODE AND CORRESPONDING CAS PAGE REFERENCES:

   1 - 3330 ONLY - P/N 2348805, 2348786, 2348787
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2. QB0XX REFERENCES BECOME QB3XX IF TWO CHANNEL SWITCH ADDITIONAL IS INSTALLED.

3. FOR A GIVEN BLOCK IN THE DIAGRAM, THE ACTUAL PAGE NUMBER MAY DEPEND ON THE DEVICE TYPE SELECTED.

ROTATIONAL POSITION SENSING (Part 1 of 2)

- Standard on 3330 and 3350, feature on 3340.

The facility provides rotational position sensing (RPS). On devices without RPS, the channel and storage control maintain connection while a record search is in progress. RPS allows the channel and storage control to be released during most of a record's search time, thereby increasing their availability for other operations.

Two commands have been added for the RPS function, Read Sector (CMD107, 125) and Set Sector (CMD16, 25):

READ SECTOR

The Read Sector command transfers one byte of information from the SCU to main storage. This byte provides the sector number (angular displacement from index) of the last record processed. If the last record processed was an overflow record, the sector number returned is that of the first segment processed in the current command chain.

Execution of a Read Sector command causes loss of the previously established record orientation. Therefore, if further processing of records of the same track (or cylinder) is desired, a search for the desired record must be made.

In 3350 compatibility mode the angular position number is not retrieved from the target register in the drive. It is calculated from the track-used counter. It is valid only if the Read Sector command follows the command processing the record of interest. If the Read Sector command follows the Set Sector command, the byte transferred to the channel has no relationship to the Set Sector command argument.

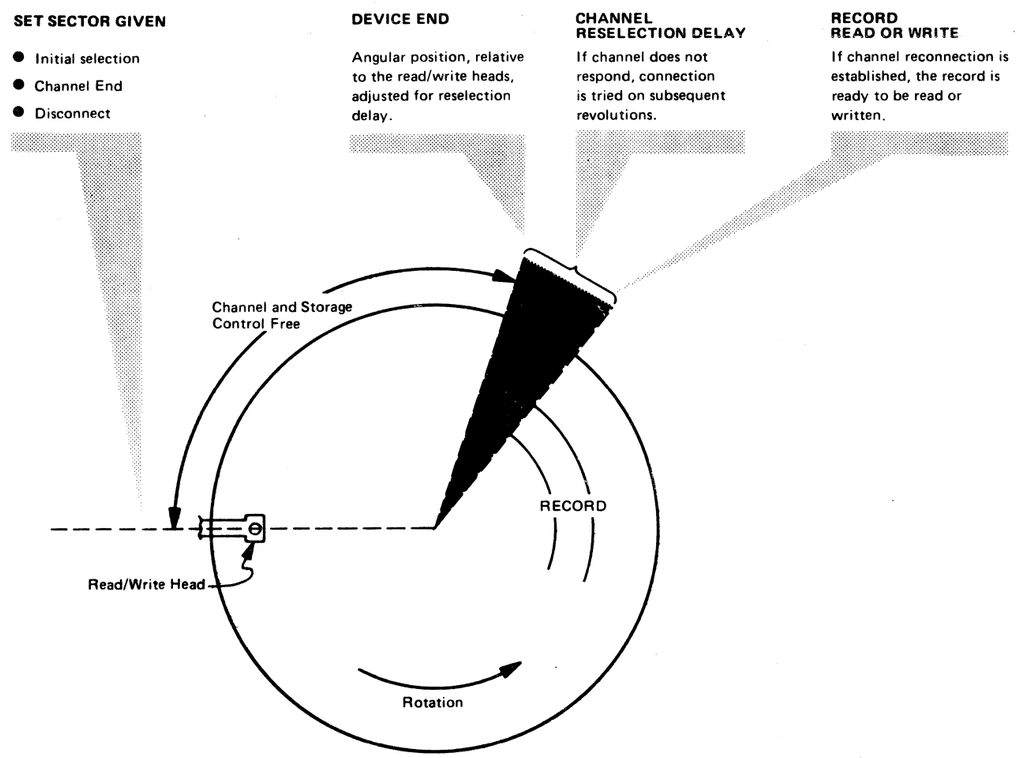
SET SECTOR

The Set Sector command transfers one byte of data from main storage to the SCU. This byte specifies one of 128 (3330 and 3350) or 64 (3340) possible angular positions per logical track. The byte value is checked for validity by the SCU. If the value is proper, the SCU generates Channel End and allows the channel to disconnect.

When the desired angular position (which has an adjusted reselection delay factor) is reached, the SCU signals Device End. The channel can then connect to continue the command chain. If the channel does not respond, connection is tried on subsequent revolutions.

In 3350 compatibility mode, the sector value from the channel is adjusted by 2/3 to ensure that the desired record is not passed.

READ/SET SECTOR OPERATION



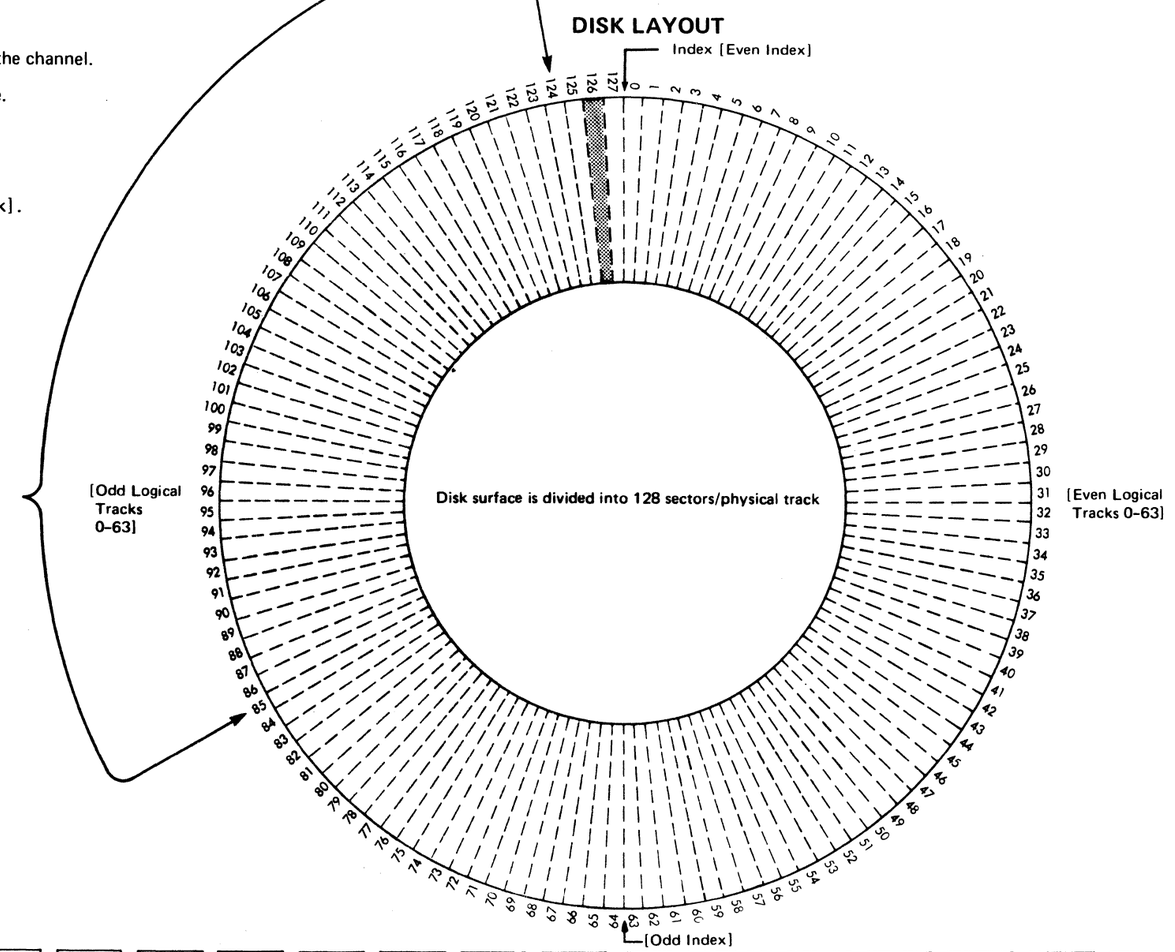
ROTATIONAL POSITION SENSING (Part 2 of 2)

Note: 3330 figures are followed by 3340 figures in [ ].

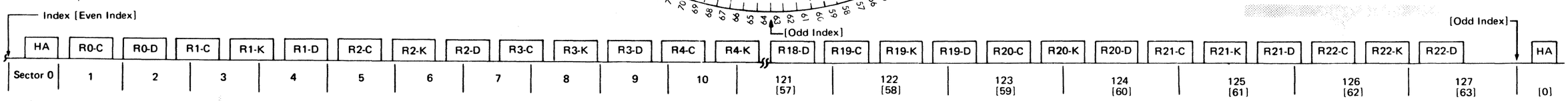
- Rotational positional sensing (RPS) minimizes time lost by the channel.
- RPS circuits are in the control module of the selected device.
- Number of sectors and timing vary with the device type.
- Rotation time 16.7 [20.2] milliseconds.
- 128 sectors [per physical track or 64 sectors per logical track].
- Sector time 130 [158] microseconds.
- Sector argument from the system is from 0-127 [0-63].

For 3350 compatibility modes, the end-of-track virtual index can occur in the range indicated depending on the number of records written on the track.

DISK LAYOUT



TRACK LAYOUT



1

When record is written, the sector number may be stored in the system by a Read Sector command.

Example: Record 22 is written. Sector 126 [62] is stored by use of the Read Sector command.

The sector can be calculated by the system if the record size is fixed.

2

Assume:

Head is at this point when a Set Sector command is received (sector 126) [62].

Sector 124 [59] is set in target register of selected module when a record starting in sector 126 [62] is to be searched. Target always set two [three] less than desired sector.

3

When sector counter and target register compare, CU raises request in to the channel. Channel can then do a Search ID for record 22 with a minimum loss of CPU time.

OVERFLOW RECORD

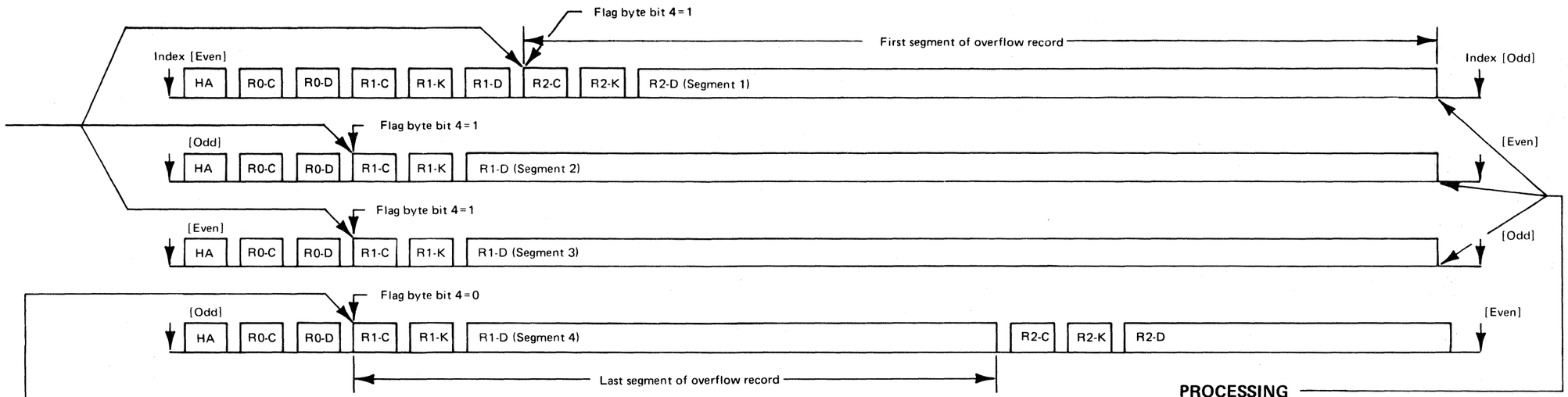
- Allow logical data records longer than one track.
- Formatting controlled by the system.
- Reading and nonformatting Write operations controlled by the CU.

FORMATTING

These segments are written using Write Special Count-Key-Data (CKD) commands.

Command sequence:

Set Sector
Search ID (R1)
TIC*-8
Write Special CKD (1st segment)
Seek Head (next track)
Search ID (R0)
TIC*-8
Write Special CKD (2nd segment)
Seek Head (next track)
Search ID (R0)
TIC*-8
Write Special CKD (3rd segment)
Seek Head (next track)
Search ID (R0)
TIC*-8
Write CKD (4th segment)



PROCESSING

CU switches to the next head on all overflow records (flag byte bit 4 = 1) of Read and nonformatting Write commands.

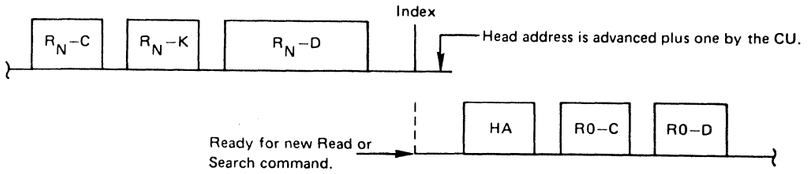
Command Sequence:
Search ID (R1),TIC*-8. Read Key-Data, Read Data, Write Key-Data or Write Data (read or write segments 1, 2, 3, and 4 with auto head switching at index, controlled by the CU).
3330 and 3350.
Errors on the first segment (excluding correctable data field data checks) are retried by the CU.
3340–
Errors on any segment of the overflow record are handled by the system error recovery procedures.
An error on the second or subsequent segments (Data Check, defective track, etc.) causes sense byte 1 bit 7, operation incomplete, to be set. A restart CCW is provided to the system error recovery procedure (ERP) in sense byte 3. After the ERP has corrected the problem, the restart CCW is sent to the CU to resume the operation.

00000110	(06)	A Read command was in progress.
00000101	(5)	A Write command was in progress.

See SENSE 35, byte 3

MULTIPLE TRACK (M/T) OPERATION

- Bit 0 of the command byte identifies a M/T operation.
- Effective only on Read and Search operations.
- If M/T bit is on in a chain of commands the head is switched to the next track at index time, providing the command is issued between the last record and index. (If the CU has issued a Read G1 head switching operation to the controller, head switching occurs 39 bytes past the index.)
- Eliminates the need for Seek Head commands in a chain of Read or Search commands.



Head switching does not occur:

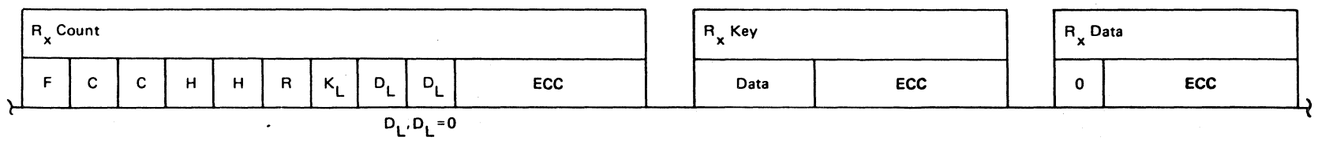
If bits 3 and 4 of file mask are both on (file protected), or
if head address would advance past last cylinder (end of cylinder).

Programming note:

M/T Search chains should be started with a single track Read HA or Read R0 to prevent missing the record if the record has passed the head when the M/T Search is started.

END OF FILE

- Defines the end of a logical group of records.
- Identified by a count field data length ($D_L D_L$) of zero.
- Data field consists of one byte of zero plus ECC bytes.
- Signals the system with Unit Exception status (status byte, bit 7) on Read IPL, Read R0, Read CKD, Read KD, Read D, Write KD, and Write D commands.



ORIENTATION

- Microprogram keeps track of relative position of the head and the format of the track.
- Microprogram uses the orientation information to determine when to start an operation called for in a command.
- Orientation is maintained by the microprogram in the command execution byte (CEB).
- As an operation is performed, the CEB is updated as each field of a record is passed.

Command Execution Byte (CEB)

Bit	0	1	2	3	4	5	6	7
Use	Clocking	Truncation	HA	Count	Key	Data	Operation	Type

Orientation Bits

00 = Search
01 = Write
10 = Read
11 = Space Count

Clock 0	Truncate 1	HA 2	Count 3	Key 4	Data 5	Command 6 7	CURRENT CEB	NEXT CEB
0	0	0	0	0	1	X X	Process Data	End
0	0	0	0	1	1	X X	Process Key	Process Data
0	0	0	1	1	1	X X	Process Count	Process Key (Data)
0	0	0	1	0	0	X X	Process Count	End
0	0	0	0	1	0	X X	Process Key	End
1	0	0	0	0	1	X X	Clock Data	Process Next Record
1	0	0	0	1	1	X X	Clock Key	Clock Data
1	0	0	1	1	1	X X	Clock Count	Clock Key (Data)
1	0	0	0	1	0	X X	Clock Key	Process Data
1	0	0	1	0	0	X X	Clock Count	Process Key (Data)
1	0	0	1	0	1	X X	Clock Count	Process Key (Only)
1	0	0	1	1	0	X X	Clock Count	Clock Key
1	1	0	0	0	1	X X	Clock/Truncate Data	End
1	1	0	0	1	0	X X	Clock/Truncate Key	End
1	1	0	1	0	0	X X	Clock/Truncate Count	End
1	1	1	0	0	0	X X	Clock/Truncate HA	End
1	1	0	0	1	1	X X	Clock/Truncate Key	Clock/Truncate Data
1	1	0	1	1	1	X X	Clock/Truncate Count	Clock Key (Data)
0	0	1	0	0	0	X X	Process HA	End
1	1	1	1	1	1	X X	Clock HA	Clock R0
1	0	1	1	1	1	X X	Clock HA	Read-Write R0
1	0	1	1	0	0	X X	Clock HA	Search ID R0 Count
1	1	1	1	1	0	X X	Clock HA	Clk R0 CT/K, Pro Data
1	1	1	1	0	0	X X	Clock HA	Clk R0 CT, Pro K/D
1	1	1	1	0	1	X X	Clock HA	Clk R0 CT, Pro Key

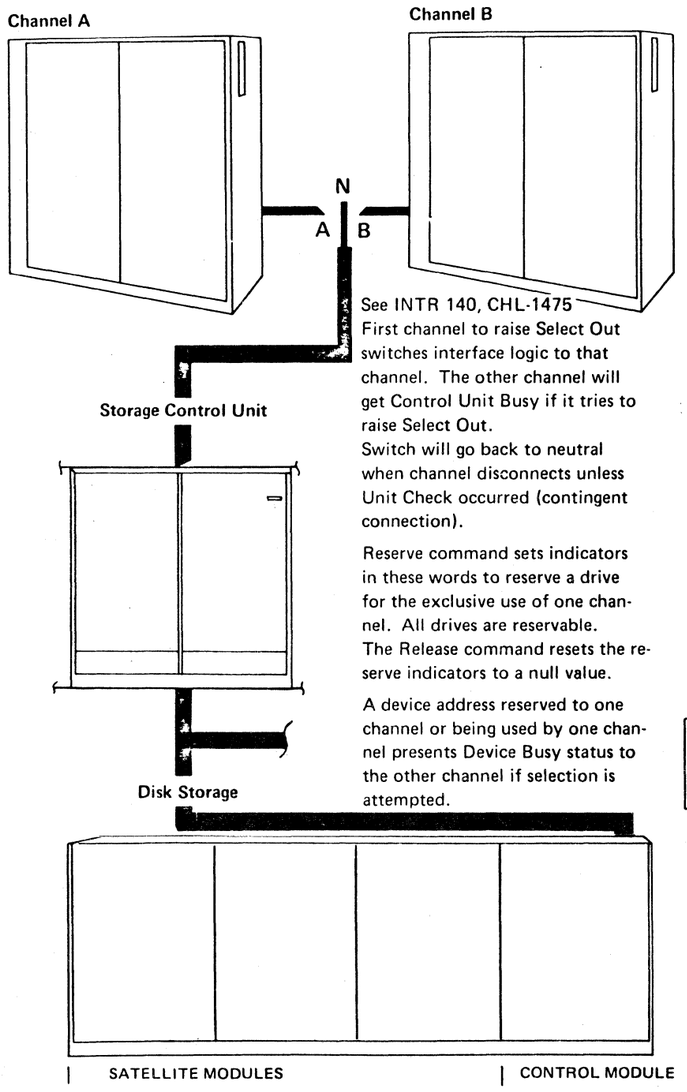
Clock 0	Truncate 1	HA 2	Count 3	Key 4	Data 5	Command 6 7	NEW CEB	COMMENT
-	-	-	-	-	-	- -		Read or Write
0	0	0	0	0	1	X X		Read or Write
0	0	0	0	1	1	X X		Read, Search, Space Count
-	-	-	-	-	-	- -		Search Only
							NEW CEB	
1	0	0	0	0	1	X X		
1	0	0	0	1	1	X X		
0	0	0	0	0	1	X X		Read or Write
0	0	0	0	1	1	X X		Read or Write
0	0	0	0	1	0	0 0		Search Only
1	0	0	0	1	0	X X		
-	-	-	-	-	-	- -		
-	-	-	-	-	-	- -		
-	-	-	-	-	-	- -		
-	-	-	-	-	-	- -		
1	1	0	0	0	1	X X		
1	0	0	1	1	1	X X		
0	1	0	1	1	1	X X		Bit 1 Means R0 Count
0	1	0	1	0	0	X X		Bit 1 Means R0 Count
1	0	0	1	1	0	X X		
1	0	0	1	0	0	X X		
1	0	0	1	0	1	X X		

6 7 Command	
0 0	Search
1 0	Read
0 1	Write
1 1	Space Count

TWO CHANNEL SWITCHING CONCEPT AND COMMANDS

Note: *If 3340 microprogram is installed in the SCU, the two channel switch, additional, feature cannot be installed.*

The two channel switch feature enables two channels to share the SCU and allows individual drives to be reserved for the exclusive use of either channel. The channels may be attached to the same or different CPUs. Channel switching and device reservation are made under control of the system(s) programs.

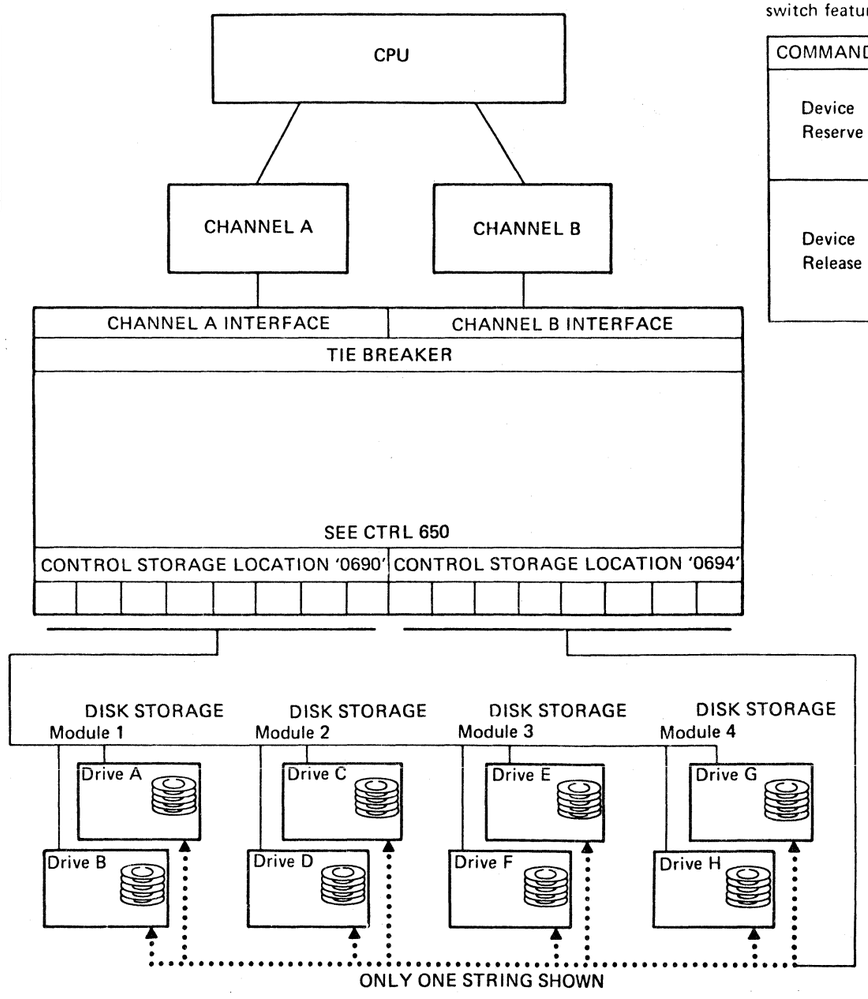


See INTR 140, CHL-1475
First channel to raise Select Out switches interface logic to that channel. The other channel will get Control Unit Busy if it tries to raise Select Out.
Switch will go back to neutral when channel disconnects unless Unit Check occurred (contingent connection).

Reserve command sets indicators in these words to reserve a drive for the exclusive use of one channel. All drives are reservable. The Release command resets the reserve indicators to a null value.

A device address reserved to one channel or being used by one channel presents Device Busy status to the other channel if selection is attempted.

CHANNEL SWITCHING AND DEVICE RESERVATION CONCEPTS



DEVICE RESERVE AND DEVICE RELEASE

Reservation of a device is done by execution of a Device Reserve command. Release of a device, previously reserved, is done by execution of a Device Release command. In addition, 24 bytes of sense data are transferred to the channel when either command is performed.

A flowchart that lists the general microprogram steps and CLD page references for either command, is on CMD 150.

Refer to CMD 142 for command objectives. The string switch feature modifies these commands; see the device MLM.

COMMAND	CODE	FUNCTION	ERROR TYPE
Device Reserve	B4	1. Set bits in control storage ('0690' = channel-A; '0694' = channel-B) to reserve addressed devices. 2. Transfer 24 bytes of sense data to the channel. 3. Send ending status to channel	QD042 If command is not the first one in the chain, command reject is set in sense data and Unit Check is set in initial status.
Device Release	94	1. Store null value in control storage ('0690' channel-A; '0694' = channel-B) to cancel reservation for devices addressed. 2. Transfer 24 bytes of sense data to the channel. 3. Send ending status to channel.	

ALTERNATE PATH RECOVERY (APR)

This function uses an Unconditional Reserve (UR) Command to break device allocation to the interface that has become inoperative, and establishes a path on an operable interface.

UNCONDITIONAL RESERVE

If a storage control attached to a string of drives with string switch feature and Alternate Path Recovery stops operating while an interface is selected or an assignment register position is set, no operation to the string or effected drive is possible from another storage control.

To eliminate this condition the select latch and assignment register position can be reset through the use of the Unconditional Reserve (UR) command. Once the select latch and/or assignment register position for the desired drive have been reset, the string is reserved for the storage control through which the UR command was issued and normal operation may continue on the functional interface.

Refer to CMD 150 for a flow chart that lists the general microprogram steps and CLD page references. Refer to CMD 142 for command objectives. Refer to device MLM for more detailed information.

CONTENTS

MIC

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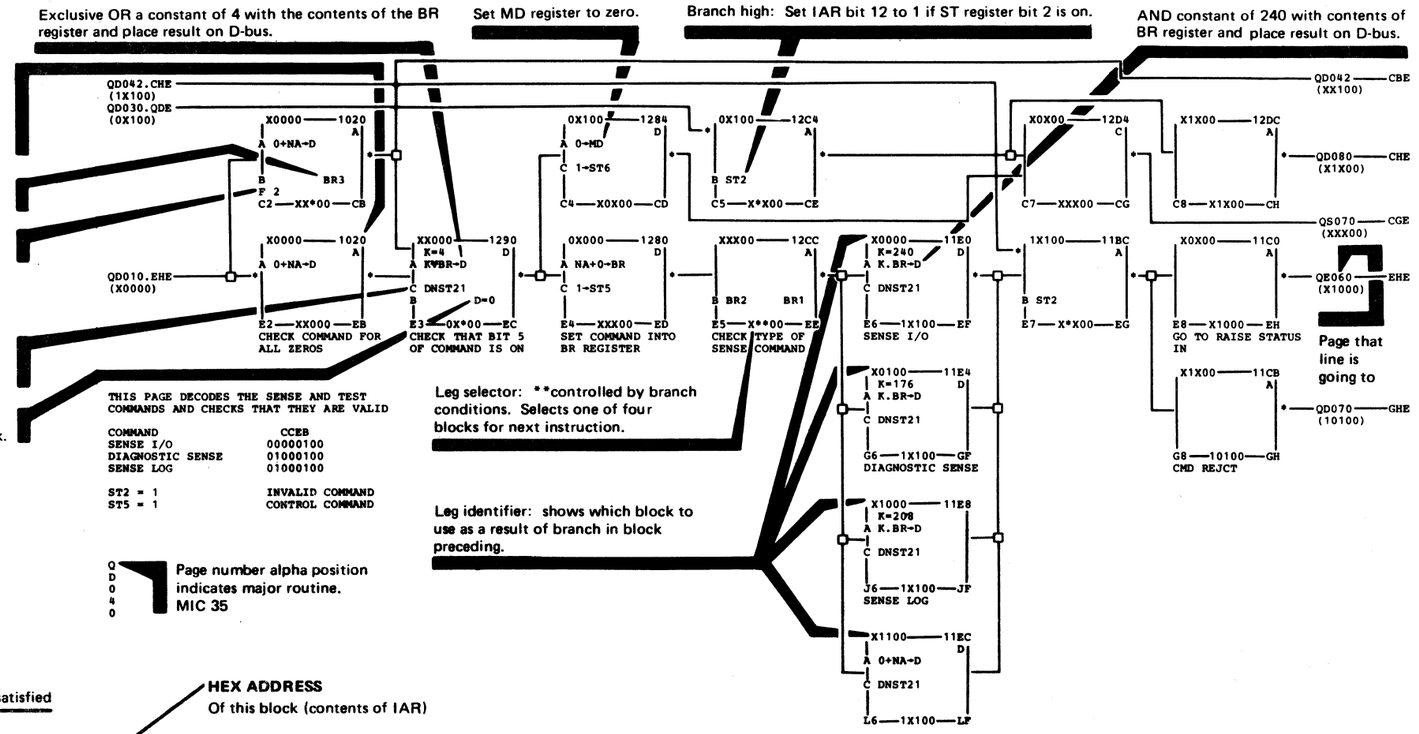
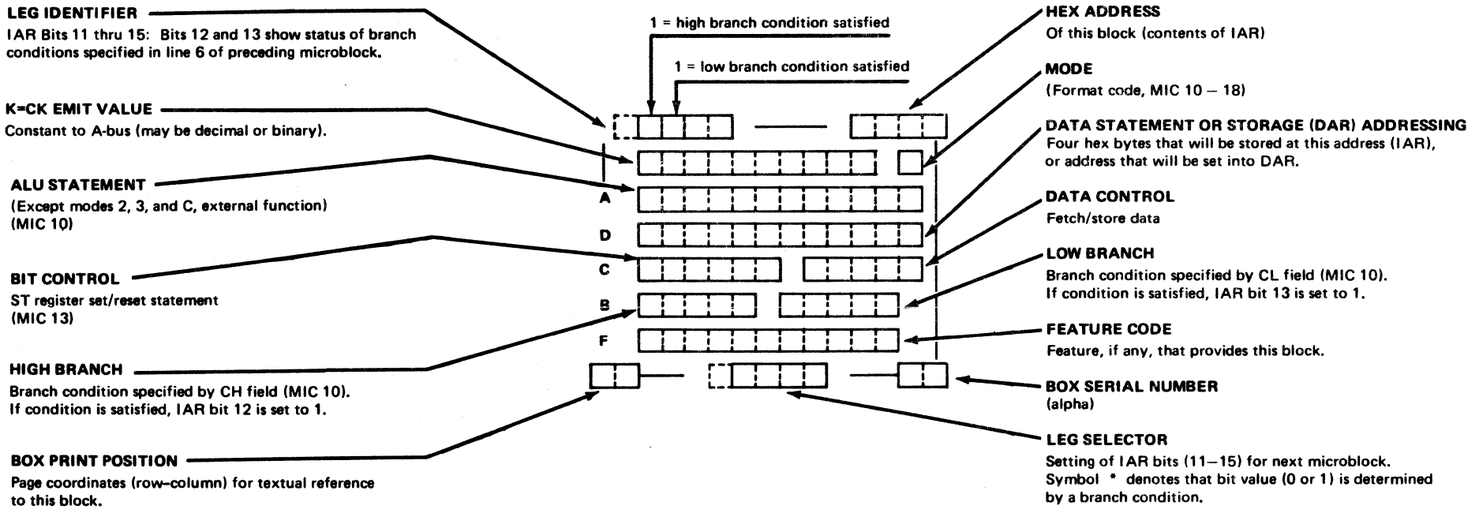
MICROPROGRAM INTRODUCTION

- Control of the control unit (CU) and modules is performed by use of an internally stored program.
- Each microprogram instruction is decoded in the control unit when read out of the control storage.
- Decoded lines cause the control unit circuits to perform an action.
- Microprogram controls actions of the channel interface, MPL file, control interface, and the modules by placing bits in registers that have outputs to the other units.
- Information or data is available to the microprogram by use of registers in the control unit with inputs from other units.
- Because control storage contents are lost when power is off, the microprogram is permanently stored on the MPL file (23FD).
- An initial microprogram load (IMPL) operation transfers the microprogram to the control storage on power up.
- Microprogram is listed on condensed logic diagrams (CLDs).
- Each block represents an instruction.
- A group of instructions that performs a given operation is called a routine.
- To perform an operation called for by a channel command word (CCW), the microprogram uses a series of routines (MIC 35).

SAMPLE MICROPROGRAM ROUTINE
COMMAND DECODE – SENSE



MICROBLOCK FORMAT



MICROCODE VERSIONS (3330 Series)

00 – Basic
02 – String Switch Attachment
04 – String Switch with 32 Drive Expansion

MICROCODE FEATURES (Line F of microblock)

1 – Single or Two Channel Switch
4 – Two Channel Switch Additional

ADDITIONAL REFERENCE

More details of microprogram instruction decoding shown on:

MIC 35	–	Major routine layout.
MIC 10–18	–	Microblock layout.
CTRL 500	–	Format field descriptions.
MIC 30–31	–	Sample microblocks.
CTRL 230	–	Addressing circuits.
CTRL 240	–	Addressing circuits
START 100	–	Manual microword decoding.

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MICRO – ORDERS

The micro-order is a coded statement that appears inside the microblock. It specifies a function to be performed during the microprogram.

This page lists the typical micro-orders encountered in the microprogram routines and gives a brief functional definition. Also listed are page references to the MLM and CFEALDs for quick reference to the hardware involved in the micro-order. Refer to MIC 2 for a description of the fields and edge characters that are associated with each micro-order and MIC 5 for register assignments.

Field	Micro-Order or Reg Used	Field Bits	Function	Page References MLM	Page References CFEALD
C S	DNST21	0010	Set ST register bit 2 if the D bus is nonzero	CTRL 240	RB101
	0 → ST0	1100	Reset ST register bit 0	CTRL 240	RB101
	0 → ST1	1001	Reset ST register bit 1	CTRL 240	RB101
	0 → ST2	1010	Reset ST register bit 2	CTRL 240	RB101
	0 → ST3C	1011	Reset ST register bit 3	CTRL 240	RB101
	0 → ST4	1000	Reset ST register bit 4	CTRL 240	RB101
	0 → ST5	1101	Reset ST register bit 5	CTRL 240	RB101
	0 → ST6	1110	Reset ST register bit 6	CTRL 240	RB101
	0 → ST7	1111	Reset ST register bit 7	CTRL 240	RB101
	1 → ST0	0100	Set ST register bit 0 to 1	CTRL 240	RB101
	1 → ST1	0001	Set ST register bit 1 to 1	CTRL 240	DE201
	1 → ST3C	0011	Set ST register bit 3 to 1. This bit takes value of carry out of ALU if "C" is added to D bus statement	CTRL 240	RB101
	1 → ST5	0101	Set ST register bit 5 to 1	CTRL 240	RB101
	1 → ST6	0110	Set ST register bit 6 to 1	CTRL 240	RB101
	1 → ST7	0111	Set ST register bit 7 to 1	CTRL 240	RB101
C A	GA	1001	GP register with outgates to the A bus	CTRL 235	RG104
	GB	1000	GP register with outgates to the A bus	CTRL 235	RG204
	GC	0001	GP register with outgates to A bus	CTRL 235	RG304
	MA	1111	GP register usually used for device read data	CTRL 235	RG102
	MB	1110	GP register usually used for byte counter high	CTRL 235	RG202
	MC	0111	GP register usually used for byte counter low	CTRL 235	RG302
	MD	0110	GP register with outgates to the A bus usually used for channel bus in	CTRL 235	RG402
	NA	1011	GP register usually used for CU address and channel conditions	CTRL 235	RG103
	NB	1010	GP register with outgates to the A bus	CTRL 235	RG203
	NC	0011	GP register	CTRL 235	RG303
	ND	0010	GP register outgates to the A bus, used for CTL-I error input	CTRL 235	RG403
	TA	1101	GP register usually used for CTL-I bus out bits	CTRL 235	RG101
	TB	1100	GP register usuually used for CTL-I gates.		RG201
	TC	0101	GP register usually used for CTL-I controls	CTRL 235	RG301
	TD	0100	GP register usually used for CTL-I tags	CTRL 235	RG401
C B & C D	BR	01110	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RB103
	GA	00101	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG104
	GB	00100	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG204
	GC	01101	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG304
	GD	10010	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG404
	MA	01011	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG102
	MB	01000	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG202
	MC	01111	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG302
	MD	01100	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG402

Field	Micro-Order or Reg Used	Field Bits	Function	Page References MLM	Page References CFEALD
C B & C D Cont.	NA	00111	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG103
	NB	10110	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG203
	NC	10101	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG302
	ND	10100	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG403
	SA	00000	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RS101
	SB	00001	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RS203
	SC	00010	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RS103
	SD	00011	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RS201
	ST	10001	GP register usually used for status indications	CTRL 235	RB101
	TA	01001	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG101
	TB	00110	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG201
	TC	10111	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG301
	TD	01010	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RG401
	TG	01001	GP register with outgates to the B bus; ingates from the D bus	CTRL 235	RB104 RA301
	0	10000	Forces all –0s to B register		
C H	ADDRO/ MC6	1101	Set IAR bit 12 to 1 if Address Out detected or MC6=1 in data response state	CTRL 230	DE306
	ILACT/ BOPAR	1111	Set IAR bit 12 to 1 if inline active or (after Sp. Op. 18) bus out parity check	CTRL 230	DE306
	BR0	0111	Set IAR bit 12 to 1 if BR register bit 0 is one	CTRL 230	RB103
	BR2	1000	Set IAR bit 12 to 1 if BR register bit 2 is one	CTRL 230	DE301
	BR4	1001	Set IAR bit 12 to 1 if BR register bit 4 is one	CTRL 230	DE301
	BR6	1010	Set IAR bit 12 to 1 if BR register bit 6 is one	CTRL 230	RB103
	CARRY	0010	Set IAR bit 12 to 1 if there was a carry out of ALU in previous microblock	CTRL 230	RA301
	CHK-2	1011	Set IAR bit 12 to 1 if Check 2 error detected	CTRL 230	RC105
	INLIN	1001	During Inline mode BR-4 replaced by INLIN after Spec Op 07		KP105
	COMMO	1100	Set IAR bit 12 to 1 if Command Out and HIO are active. Ext bch condition 12	CTRL 230	DE306
	SECTR	1000	During IMPL, BR-2 replaced by SECTR (Sector pulse or read parity error)	CTRL 230	LA306
	SUPPO/ XCHAN	1110	Set IAR bit 12 to 1 if Selected Suppress Out detected or (after Sp. Op. 18) chan C/D selected	CTRL 230	DE306
	ST0	0011	Set IAR bit 12 to 1 if ST register bit 0 is one	CTRL 230	RB101
	ST2	0100	Set IAR bit 12 to 1 if ST register bit 2 is one	CTRL 230	RB101
	ST4	0101	Set IAR bit 12 to 1 if ST register bit 4 is one	CTRL 230	RB101
	ST6	0110	Set IAR bit 12 to 1 if ST register bit 6 is one	CTRL 230	RB101
	0	0000	Set IAR bit 12 to zero	CTRL 225	DE302
	1	0001	Set IAR bit 12 to 1	CTRL 230	DE302
C L	BR1	0111	Set IAR bit 13 to 1 if BR register bit 1 is 1	CTRL 230	RB103
	BR3	1000	Set IAR bit 13 to 1 if BR register bit 3 is 1	CTRL 230	DE301
	BR5	1001	Set IAR bit 13 to 1 if BR register bit 5 is 1	CTRL 230	DE301
	BR7	1010	Set IAR bit 13 to 1 if BR register bit 7 is 1	CTRL 230	RB103
	BTRDY	1000	During IMPL BR3 replaced by BTRDY (Byte Ready)	CTRL 230	LA306
	CUEND/ BFRDY	1110	Set IAR bit 13 to 1 if Buffer Full is detected or (after Sp. Op. 18) Control Unit End latch is on	CTRL 230	DE306
	RSPON/ CHANB	1111	Set IAR bit 13 to 1 if CTL-I Tag Valid, Normal End, or Check End (after Sp. Op. 18), or chan B/D selected	CTRL 230	DE306

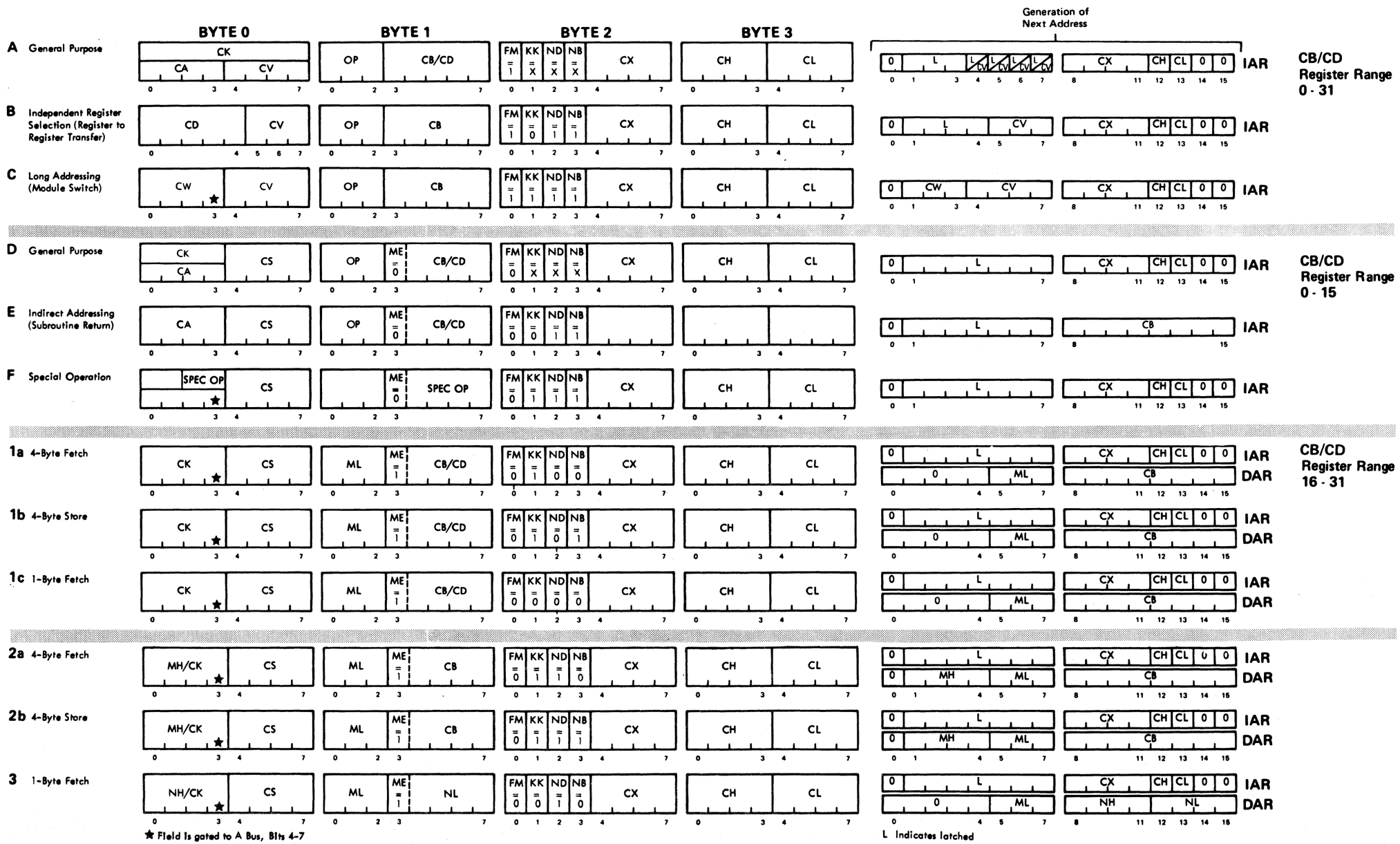
Field	Micro-Order or Reg Used	Field Bits	Function	Page References MLM	Page References CFEALD
C L Cont.	D=0	0010	Set IAR bit 13 to 1 if the D bus is equal to zero	CTRL 230	RA302
	HLTIO/ XFER	1100	Set IAR bit 13 to 1 if Halt I/O latch or (after Sp. Op. 18) Transfer latch is set	CTRL 230	DE306
	ILXEQ	1001	During Inlines, BR5 replaced by ILXEQ (Inline Execute Switch latch)	CTRL 230	KP105
	INDEX (ST1)	0011	Set IAR bit 13 to 1 if ST1=1 and Index is detected	CTRL 230	DE306
	SELTD/ MC7	1011	Set IAR bit 13 to 1 if CU selected or MC7=1 in data response state	CTRL 230	DE306
	SERVO/ MULTI	1101	Set IAR bit 13 to 1 if Service Out or (after Sp. Op. 18) Multi-Tag Switch (two channel switch feature) is active	CTRL 230	DE306
	ST3	0100	Set IAR bit 13 to 1 if ST register bit 3 is one	CTRL 230	DE307
	ST5	0101	Set IAR bit 13 to 1 if ST register bit 5 is one	CTRL 230	RB101
	ST7	0110	Set IAR bit 13 to 1 if ST register bit 7 is one	CTRL 230	DE301
	0	0000	Set IAR bit 13 to zero	CTRL 230	DE301
	1	0001	Set IAR bit 13 to one	CTRL 230	DE301
SPECIAL OPERATIONS See page MIC 5	Sp Op 0	000000	Pgm-Stop Statement		DE402
	Sp Op 1	000001	Chk-Stop Statement		DE402
	Sp Op 3	000011	Error 2 Reset to User		DE402
	Sp Op 4	000100	Gate Read Error Pattern to NB		DE402
	Sp Op 5	000101	Reset Storage Error Register		DE402
	Sp Op 6	000110	Set Address Compare from SA and SB		DE402
	Sp Op 7	000111	INLIN (Inline) Branch in CE Mode ILXEQ (Data Entry) Branch in CE Mode		DE402
	Sp Op 8	001000	Stop MPL Operation		DE402
	Sp Op 9	001001	Start MPL Operation		DE402
	Sp Op 10	001010	Gate MPL Data to SD Reg via D Bus		DE402
	Sp Op 12	001100	F-reg Control (See MIC 5)		
	Sp Op 13	001101	Load ND Register		
	Sp Op 14	001110	Gate Check 2 Conditions to NA Register		
	Sp Op 15	001111	Set CTL-I Bus in Parity Error		
	Sp Op 13	001101	Load ND register		
	Sp Op 14	001110	Gate Check 2 Conditions to NA Register		
	Sp Op 15	001111	Set CTL-I Bus In Parity Error		
	Sp Op 16	010000	CTL-I Response End		
	Sp Op 17	010001	CTL-I Recycle/Load CI Buffer from TA		
	Sp Op 18	010010	Gate Alternate Branch Condition		
	Sp Op 19	010011	Set Inline Active latch/Set Dev Branch		DE402
	Sp Op 20	010100	Reset Inline Active latch/Reset Dev Branch		DE402
	Sp Op 21	010101	Unfreeze Channel Switch		DE402
	Sp Op 22	010110	Allow Disable A		DE402
	Sp Op 23	010111	Allow Disable B		DE404
	Sp Op 24	011000	Gate Comparison Assist latches to MB		DE402
	Sp Op 26	011010	Freeze Channel Switch		DE402
	Sp Op 28	011100	Selective Reset after Check 1		
	Sp Op 30	011110	Propagate Select Out		
	AΩB → D	0000	A register ORed with B register and the results placed on D bus	CTRL 410	RA303
	A·B → D	0001	A register ANDed with B register and the results placed on D bus	CTRL 410	RA303
	A∀B → D	0010	A register Exclusive ORed with the B register and the results placed on the D bus	CTRL 410	RA303
	A+B → D	0011	A register added to the B register and the results placed on the D bus	CTRL 410	RA303
	A+B–C→DC	0100	A register and B register and present condition of Carry In (ST3C) added	CTRL 410	RA303
	A–B+C→DC	0101	ADD, Complement, Carry	CTRL 410	RA303
	A+B → DC	0110	A and B registers are added and results placed on D bus. Set ST register bit 3 to 1 if carry occurred	CTRL 410	RA303
	A–B+1→DC	0111	ADD twos complement (Subtract)	CTRL 410	RA303
	DAR		Data Address Register		RL104
	IAL		Lower byte of Instruction Address Register		RL102
	IAR		Instruction Address Register		RL102

From	Register Position	Meaning	To
CTL-I (Buffer)	MA 0 MA 1 MA 2 MA 3 MA 4 MA 5 MA 6 MA 7 MA P	CTL-I Bus In 0 CTL-I Bus In 1 CTL-I Bus In 2 CTL-I Bus In 3 CTL-I Bus In 4 CTL-I Bus In 5 CTL-I Bus In 6 CTL-I Bus In 7 CTL-I Bus In P	Control Unit
Control Unit	MB 0 MB 1 MB 2 MB 3 MB 4 MB 5 MB 6 MB 7 MB P	Byte Counter High	CTL-I
Control Unit	MC 0 MC 1 MC 2 MC 3 MC 4 MC 5 MC 6* MC 7* MC P	Byte Counter Low *S Register Set Control 00 = SA, 11 = SB, 10 = SC, 01 = SD	CTL-I
Control Unit	MD 0 MD 1 MD 2 MD 3 MD 4 MD 5 MD 6 MD 7 MD P	Bus In 0 Bus In 1 Bus In 2 Bus In 3 Bus In 4 Bus In 5 Bus In 6 Bus In 7 Bus In P	Selected Channel
Selected Channel	NA 0 NA 1 NA 2 NA 3 NA 4 NA 5 NA 6 NA 7 NA P	Bus Out 0 Bus Out 1 Bus Out 2 Bus Out 3 Bus Out 4 Bus Oug 5 Bus Out 6 Bus Out 7 Bus Out P	Control Unit (Not Sp Op 14)
Channel Channel Channel Channel CTL-I CTL-I CTL-I	NA 0 NA 1 NA 2 NA 3 NA 4 NA 5 NA 6 NA 7 NA P	Channel Buffer Parity Check Interface Check — Channel A or C Interface Check — Channel B or D Data Transfer Check CTL-I Check CTL-I Load S Register Check Compare Assist Check Interface Check C/D or Multiconnect Error Generated Parity	Control Unit (Gated by Sp Op 14)
CTL-I/ Controller	ND 0-7	Refer to Detailed Chart and TD Register	Control Unit

From	Register Position	Meaning	To
If Spec Op 13 and TD1=0	ND 0 ND 1 ND 2 ND 3 ND 4 ND 5 ND 6 ND 7	CTL-I Controller Check CTL-I Select Active or Select Check CTL-I Buffer Parity Error CTL-I Unexpected End Check CTL-I Tag Bus Parity Check CTL-I Bus Out Parity Check CTL-I Transfer Error Not Used	
If Spec Op 13 and TD1=1	ND 0 ND 1 ND 2 ND 3 ND 4 ND 5 ND 6 ND 7	CTL-I Selected Alert 1 CTL-I Select Active CTL-I Sync In CTL-I Unexpected End Check CTL-I Normal End CTL-I Check End CTL-I Tag Valid Not Used	
Control Unit	TA 0 TA 1 TA 2 TA 3 TA 4 TA 5 TA 6 TA 7 TA P	CTL-I Bus Out 0 CTL-I Bus Out 1 CTL-I Bus Out 2 CTL-I Bus Out 3 CTL-I Bus Out 4 CTL-I Bus Out 5 CTL-I Bus Out 6 CTL-I Bus Out 7 CTL-I Bus Out P	Tag modifiers to Control Module
Control Unit	TB 0 TB 1 TB 2 TB 3 TB 4 TB 5 TB 6 TB 7 TB P	Select Hold Tag Gate Error Alert Gate Allow Busy to Other Channel(s) Enable CU End Channel D Enable CU End Channel C Enable CU End B/Disable CU End A Allow NA Load	Controller Controller CTL-I Channel
Control Unit	TC 0 and TC 1 TC 2 TC 3 TC 4 TC 5 TC 6 and TC 7	00 Reset 01 Channel Read Control 10 Channel Write Control 11 Freeze Transfer Last Byte Request Operational In Address In Status In 00 — Not Data Response State 01 — CTL-I Write 10 — CTL-I Read — No Load S Register 11 — CTL-I Read — Load S Register	Channel CTL-I
Control Unit	TD 0 TD 1 TD 2 TD 3 TD 4 TD 5 TD 6 TD 7 TD P	CTL-I Tag Bit 0 Gate Control Module Status Not Used Not Used Decode 8 Bit Decode 4 Bit Decode 2 Bit Decode 1 Bit Parity for Tag Bus	Controller Tag Bus

From	Register Position	Meaning	To
Control Unit	TE 0 TE 1 TE 2 TE 3 TE 4 TE 5 TE 6 TE 7 TE P	Unsuppressible Request In Channel D Suppressible Request In Channel D Unsuppressible Request In Channel C Suppressible Request In Channel C Not Used Not Used Allow Disable Channel C Allow Disable Channel D	Channel
Control Unit	TG 0 TG 1 TG 2 TG 3 TG 4 TG 5 TG 6 TG 7 TG P	Unsuppressible Request In Channel B Suppressible Request In Channel B Unsuppressible Request In Channel A Suppressible Request In Channel A Block Switch to Channel D Block Switch to Channel C Block Switch to Channel B Block Switch to Channel A	Channel
Control Unit (Gated by MPL latch)	TG 0 TG 1 TG 2 TG 3 TG 4 TG 5 TG 6 TG 7 TG P	Engage MPL File Head Move MPL One Track In Move MPL One Track Out MPL File Start Read Not Used Not Used Not Used Not Used	MPL File
Control Unit	Sp Op 0 Sp Op 1 Sp Op 2 Sp Op 3 Sp Op 4 Sp Op 5 Sp Op 6 Sp Op 7 Sp Op 8 Sp Op 9 Sp Op 10 Sp Op 11 Sp Op 12 Sp Op 13 Sp Op 14 Sp Op 15 Sp Op 16 Sp Op 17 Sp Op 18 Sp Op 19 Sp Op 20 Sp Op 21 Sp Op 22 Sp Op 23 Sp Op 24 Sp Op 26 Sp Op 28 Sp Op 30	Pgm-Stop Statement Chk-Stop Statement Not Used Error 2 Reset to User Gate Read Error Pattern to NB Reset Storage Error Register Set Address Compare From SA & SB INLIN(Inline) Branch in CE Mode and ILXEQ (Data Entry) Branch in CE Mode Stop MPL Operation Start MPL Operation Gate MPL Data to SD Reg via D Bus Not Used Used with TF-reg Control Bits to: Force Parity Errors Increment Local Store REGs Read Diagnostic Plug Card. Load ND Register (See chart to left) Gate Check 2 Conditions to NA Register Set CTL-I Bus In Parity Error CTL-I Response End CTL-I Recycle/Load CTL-I Buffer from TA Gate Alternate Branch Condition Set Inline Active Latch/Set Dev Branch Reset Inline Active Latch /Reset Dev Branch Unfreeze Channel Switch Allow Disable A Allow Disable B Gate Comparison Assist Latches to MB Freeze Channel Switch Selective Reset after Check 1 Propagate Select Out	Clock Clock CHL-I, CTL-I Control Storage Control Storage CE Controls Branch Controls Branch Controls MPL File MPL File MPL File CTL-I CE CE Channel Channel Channel CHL-I Channel
	GF NF TF MF	Refer to MIC 40	

MICROWORD FORMAT SUMMARY



★ Field Is gated to A Bus, Bits 4-7

L Indicates latched

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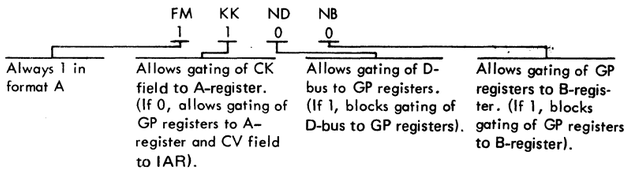
MICROWORD FORMAT A (FM = 1, ND AND NB ≠ 11)

- General purpose use.
- Cannot be used to modify status bit settings.

A FORMAT DECODE

- Four bits of the microword are decoded to determine the format. (Some formats decode a fifth bit.)
- Six configurations of these four bits are collectively known as format A (see CTRL 500):
- In the example, the format is decoded as:



B CK FIELD (BYTE 0, BITS 0 - 7)

- Specified by KK =1.
- CK field is gated to the A-register.

C OP FIELD (BYTE 1, BITS 0 - 2)

- Decoded to specify the ALU function to be performed.
- In the example, 001 is decoded as A·B→D.

D CB/CD FIELD (BYTE 1, BITS 3 - 7)

- Decoded to select a GP register to serve as B-entry and/or destination register.
- NB and ND bits determine the function of the CB/CD field.
- In the example, 01110 indicates that the BR register is to be used for both B-entry and destination registers.

E CX FIELD (BYTE 2, BITS 4 - 7)

- Gated to bits 8-11 of IAR.

F CH FIELD (BYTE 3, BITS 0 - 3)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 0001 sets IAR (12) to 1 unconditionally.

G CL FIELD (BYTE 3, BITS 4 - 7)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 0010 sets IAR(13) to 1 if the D-bus is zero as a result of the ALU function performed in the preceding microprogram step.

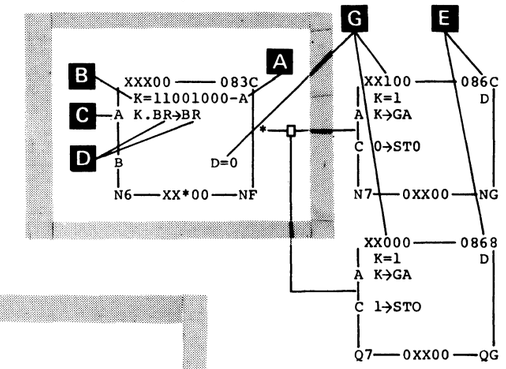
H CA FIELD (BYTE 0, BITS 0 - 3)

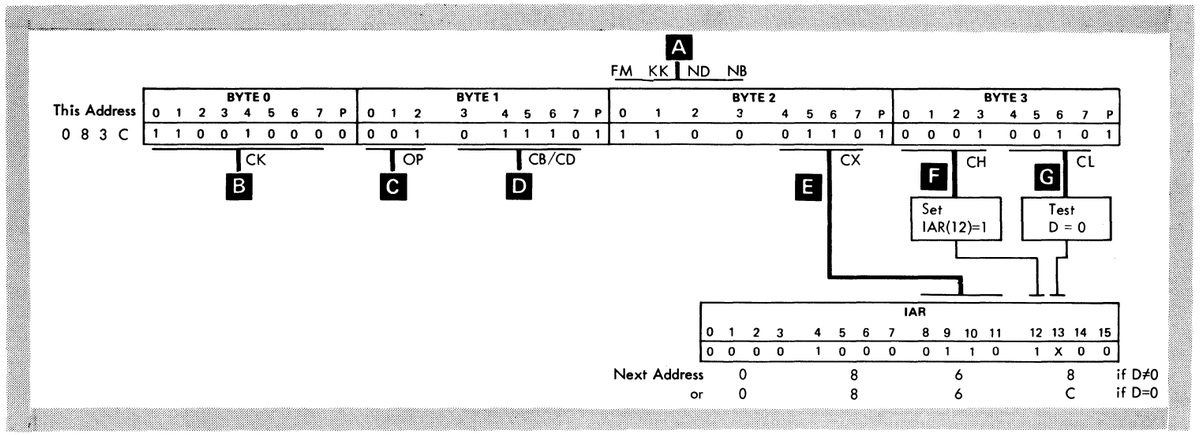
- Specified by KK=0.
- Decoded to select a GP register to serve as A-entry register.
- In the example, CA is not specified.

J CV FIELD (BYTE 0, BITS 4 -7)

- Specified by KK=0.
- Gated to bits 4-7 of IAR.
- In the example, CV is not specified.

Format A Example





Format A Bit Assignment Chart

	BYTE 0		BYTE 1		BYTE 2					BYTE 3	
	0 1 2 3 4 5 6 7		0 1 2	3 4 5 6 7	0	1	2	3	4 5 6 7	0 1 2 3	4 5 6 7
H	CA	CV	OP	CB/CD	1	0	0	0	CX	CH	CL
	CA	CV	OP	CD	1	0	0	1	CX	CH	CL
Format Configurations	CA	CV	OP	CB	1	0	1	0	CX	CH	CL
	CK		OP	CB/CD	1	1	0	0	CX	CH	CL
	CK		OP	CD	1	1	0	1	CX	CH	CL
	CK		OP	CB	1	1	1	0	CX	CH	CL

Hex Value in Field	A-Entry	Bits 4-7 of IAR	ALU Control	B Entry and Destination Bit 3 = 1	Bit 3 = 0	FM	KK	ND	NB	Bits 8-11 of IAR	Branch High (IAR Bit 12)	Branch Low (IAR Bit 13)	
0	0		A Ω B→D	0	SA	Specifies format A,B,C	Defines bits 0-3 of byte 0	Defines bits 3-7 of byte 1			0	0	0
1	GC		A • B→D	ST	SB						1	1	1
2	ND		A ∀ B→D	GD	SC						Carry	D = 0	2
3	NC		A + B→D	TG	SD						ST0	Index • ST1	3
4	TD		A + B + C→DC	ND	GB						ST2	ST3C	4
5	TC		A − B + C→DC	NC	GA						ST4	ST5	5
6	MD		A + B→DC	NB	TB						ST6	ST7	6
7	MC		A − B + 1→DC	TC	NA						BR0	BR1	7
8	GB			GF	MB						BR2*	BR3**	8
9	GA			GE	TA						BR4***	BR5****	9
A	NB			NF	TD						BR6	BR7	A
B	NA			NE	MA						CHK-2	SELTD/MC7	B
C	TB			TF	MD						COMMO ADDRO/MC6 SUPPO/XCHAN ILACT & DEV/ BOPAR	HLTIO/XFER	C
D	TA			TE	GC							SERVO/MULTI	D
E	MB			MF	BR							CUEND/BFRDY	E
F	MA			ME	MC							RSPON/CHANB	F

*During IMPL BR2 replaced by SECTR
**During IMPL BR3 replaced by BTRDY
***Following Spec Op 7, BR4 replaced by INLIN
****Following Spec Op 7, BR5 replaced by ILXEQ

MICROWORD FORMAT B (FM, KK, ND, NB = 1011)

- Register to register transfer.

A FORMAT DECODE

Decoding of format B (FM, KK, ND, NB = 1011) sets up the following controls (see CTRL 500):

- Blocks ingating to A register.
- Allows gating of GP registers to B register.
- Allows gating of D bus to GP registers.
- Allows gating of CV and CX fields to IAR.

B CD FIELD (BYTE 0, BITS 0 - 4)

- Decoded to select a GP register to serve as destination register.
- In the example, 00011 selects the SD register.

C CV FIELD (BYTE 0, BITS 5 - 7)

- Gated to bits 5-7 of IAR.

D OP FIELD (BYTE 1, BITS 0 - 2)

- Decoded to specify the ALU function to be performed.
- In the example, 011 is decoded as A+B→D.
- The A bus entry is always zero for this mode.

E CB FIELD (BYTE 1, BITS 3 -7)

- Decoded to select a GP register to serve as B entry register.
- In the example, 00100 indicates that the GB register is to be used for B entry.

F CX FIELD (BYTE 2, BITS 4 - 7)

- Gated to bits 8-11 of IAR.

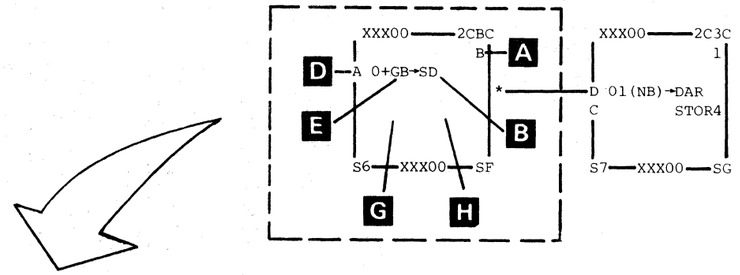
G CH FIELD (BYTE 3, BITS 0 - 3)

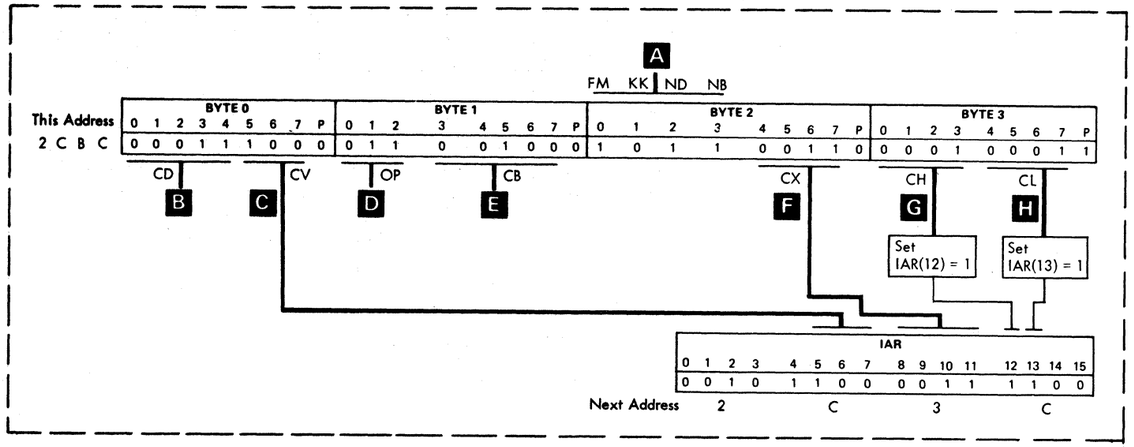
- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 0001 sets IAR(12) to 1 unconditionally.

H CL FIELD (BYTE 3, BITS 4 - 7)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 0001 sets IAR (13) to 1 unconditionally.

Format B Example





Format B Bit Assignment Chart

Hex Value in Field	BYTE 0 CD Destination Bit 0=1	BYTE 0 CD Destination Bit 0=0	BYTE 0 CV Bits 5-7 of IAR	BYTE 1 OP ALU Control	BYTE 1 CB B-Entry Bit 3 = 1	BYTE 1 CB B-Entry Bit 3 = 0	BYTE 2 FM KK ND NB (1 0 1 1)	BYTE 2 CX Bits 8-11 of IAR	BYTE 3 CH Branch High (IAR Bit 12)	BYTE 3 CL Branch Low (IAR Bit 13)	
0	0	SA		A Ω B→D	0	SA			0	0	0
1	ST	SB		A • B→D	ST	SB			1	1	1
2	GD	SC		A∀ B→D	GD	SC			Carry	D = 0	2
3	TG	SD		A + B→D	TG	SD			ST0	Index•ST1	3
4	ND	GB		A + B + C→DC	ND	GB			ST2	ST3C	4
5	NC	GA		A - B + C→DC	NC	GA			ST4	ST5	5
6	NB	TB		A + B→DC	NB	TB			ST6	ST7	6
7	TC	NA		A - B + 1→DC	TC	NA			BR0	BR1	7
8	GF	MB			GF	MB			BR2*	BR3**	8
9	GE	TA			GE	TA			BR4***	BR5****	9
A	NF	TD			NF	TD			BR6	BR7	A
B	NE	MA			NE	MA			CHK-2	SELTD/MC7	B
C	TF	MD			TF	MD			COMMO	HLTIO/XFER	C
D	TE	GC			TE	GC			ADDRO/MC6	SERVO/MULTI	D
E	MF	BR			MF	BR			SUPPO/XCHAN	CUEND/BFRDY	E
F	ME	MC			ME	MC			ILACT & DEV/ BOPAR	RESPON/CHANB	F

*During IMPL BR2 replaced by SECTR
**During IMPL BR3 replaced by BTRDY
***Following Spec Op 7, BR4 replaced in INLIN
****Following Spec Op 7, BR5 replaced by ILXEQ

MICROWORD FORMAT C (FM, KK, ND, NB = 1111)

- Long addressing (module switching).

A FORMAT DECODE

Decoding of format C (FM, KK, ND, NB = 1111) sets up the following controls (see CTRL 500):

- Allows gating of CW field to A-register (4–7).
- Allows gating of GP registers to B-register.
- Allows gating of D-bus to GP registers.
- Allows gating of CW, CV, and CX fields to IAR.

B CW FIELD (BYTE 0, BITS 0 - 3)

- Gated to bits 0–3 of IAR and to bits 4–7 of the A-bus.

C CV FIELD (BYTE 0, BITS 4 - 7)

- Gated to bits 4–7 of IAR.

D OP FIELD (BYTE 1, BITS 0 - 2)

- No ALU statement is allowed for this format; however, the D-bus may be nonzero after this block is executed.

E CB FIELD (BYTE 1, BITS 3 - 7)

- Selects a GP register to be gated to the B-register.
- In the example, 10000 does not gate a GP register.

F CX FIELD (BYTE 2, BITS 4 - 7)

- Gated to bits 8–11 of IAR.

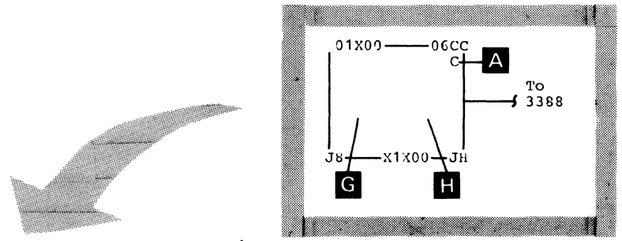
G CH FIELD (BYTE 3, BITS 0 - 3)

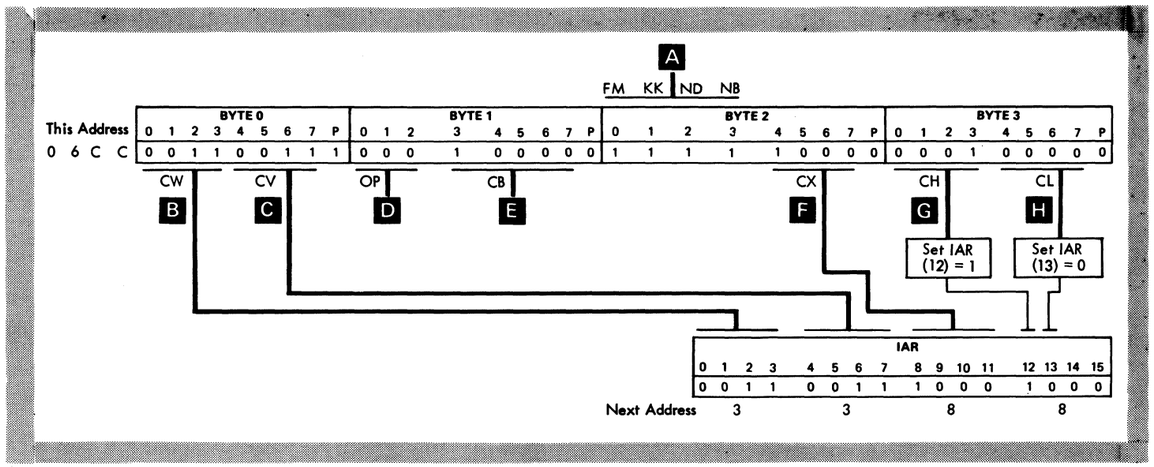
- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 0001 sets IAR (12) to 1 unconditionally.

H CL FIELD (BYTE 3, BITS 4 -7)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 0000 sets IAR (13) to 0 unconditionally.

Format C Example





Format C Bit Assignment Chart

Hex Value in Field	BYTE 0 (0 1 2 3 4 5 6 7)		BYTE 1 (0 1 2)	BYTE 1 (3 4 5 6 7)		BYTE 2 (0 1 2 3)	BYTE 2 (4 5 6 7)	BYTE 3 (0 1 2 3)	BYTE 3 (4 5 6 7)	
	CW	CV	OP	CB		1 1 1 1	CX	CH	CL	
↓	Bits 0–3 of IAR and bits 4–7 of A Bus	Bits 4–7 of IAR	ALU Control	B Entry Bit 3 = 1	Bit 3 = 0	FM KK ND NB	Bits 8–11 of IAR	Branch High (IAR Bit 12)	Branch Low (IAR Bit 13)	
0			A Ω B→D	0	SA			0	0	0
1			A • B→D	ST	SB			1	1	1
2			A ∇ B→D	GD	SC			Carry	D = 0	2
3			A + B→D	TG	SD			ST0	Index • ST1	3
4			A + B + C→DC	ND	GB			ST2	ST3C	4
5			A - B + C→DC	NC	GA			ST4	ST5	5
6			A + B→DC	NB	TB			ST6	ST7	6
7			A - B + 1→DC	TC	NA			BR0	BR1	7
8				GF	MB			BR2*	BR3**	8
9				GE	TA			BR4***	BR5****	9
A			No effective ALU (Suppress D Bus)	NF	TD			BR6	BR7	A
B				NE	MA			CHK-2	SELTD/MC7	B
C				TF	MD			COMMO ADDRO SUPPO/XCHAN ILACT & DEV/ BOPAR	HLTIO/XFER	C
D				TE	GC				SERVO/MULTI	D
E				MF	BR				CUEND/BFRDY	E
F				ME	MC				RSPON/CHANB	F

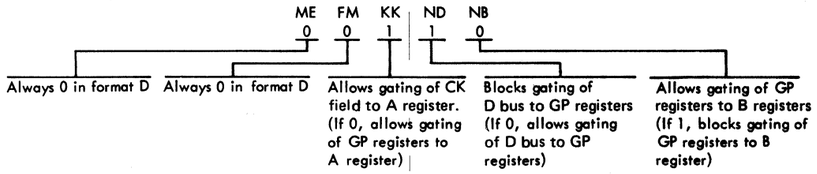
*During IMPL BR2 replaced by SECTR
**During IMPL BR3 replaced by BTRDY
***Following Spec Op 7, BR4 replaced by INLIN
****Following Spec Op 7, BR5 replaced by ILXEQ

MICROWORD FORMAT D (ME, FM = 00 AND ND, NB ≠ 11)

- General purpose use with ability to modify status bits.

A FORMAT DECODE

- Five bits of the microword are decoded to determine the format.
- Six configurations of these five bits are collectively known as format D.
- In the example, the format is decoded as:



B CK FIELD (BYTE 0, BITS 0 - 3)

- Specified by KK=1.
- Gated to bits 0-3 of the A register or to bits 4-7 of the A-register, depending on CX(7).
- In the example, 0100 is gated to bits 4–7 of the A-register.

C CS FIELD (BYTE 0, BITS 4 - 7)

- Decoded to set or reset specific status (ST) bits.
- ST(4) is set by hardware only; it cannot be set by the CS field.
- The example (0010) is decoded as DNST21. This result sets ST(2) to 1 if the D bus is nonzero following execution of the ALU function in line A of the microblock.

D OP FIELD (BYTE 1, BITS 0 - 2)

- Decoded to specify the ALU function to be performed.
- In the example, 010 is decoded as A∀B→D.

E CB/CD FIELD (BYTE 1, BITS 3 - 7)

- Decoded to select a GP register to serve as B-entry and/or destination register.
- The high-order (ME) bit of the CB/CD field is always 0 in format D.
- NB and ND bits determine the function of the CB/CD field.
- In the example, 00001 indicates that the SB register is to be used as B entry and that the D bus is to be suppressed.

F CX FIELD (BYTE 2, BITS 4 - 7)

- Gated to bits 8–11 of IAR.
- The low-order bit CX(7) determines the gating of the CK field to the A-register.
- In the example, CX(7)=0; therefore CK is gated to A-register bits 4–7.

G CH FIELD (BYTE 3, BITS 0 - 3)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 1110 sets IAR(12) to 1 if SUPPO (Suppress Out) is up.

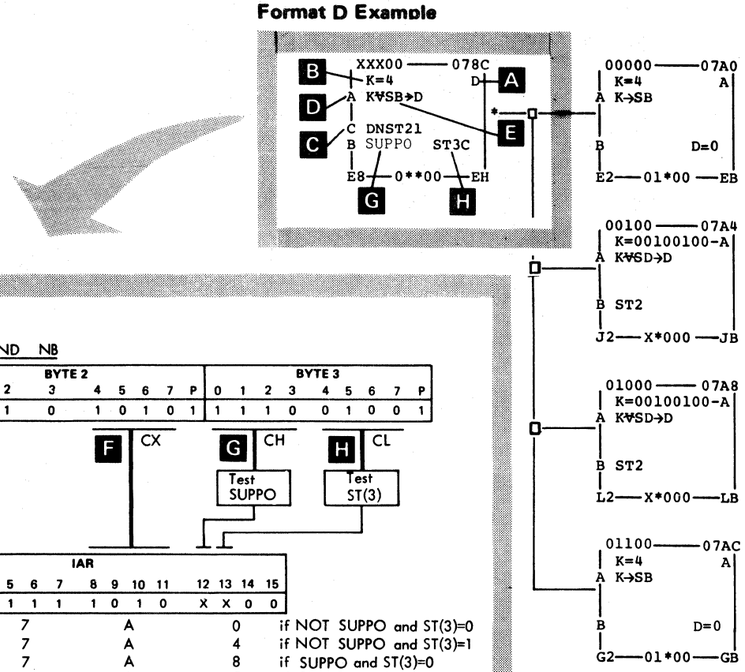
H CL FIELD (BYTE 3, BITS 4 - 7)

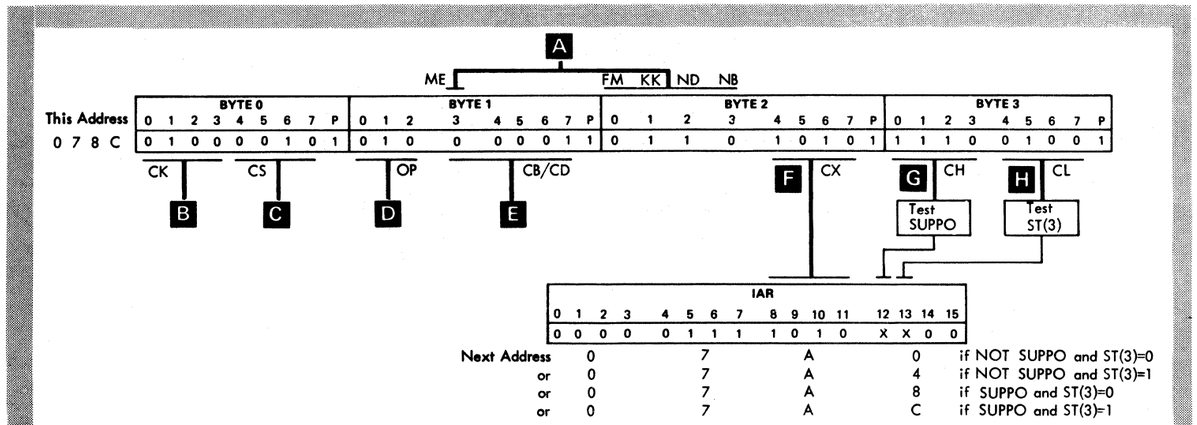
- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 0100 tests for ST(3) being on.

J CA FIELD (BYTE 0, BITS 0 - 3)

- Specified by KK=0.
- Decoded to select a GP register to serve as A-entry register.
- In the example, CA is not specified.

Format D Example





Format D Bit Assignment Chart

Hex Value in Field	BYTE 0 0 1 2 3 4 5 6 7		BYTE 1 0 1 2	3 4 5 6 7	BYTE 2 0	1	2	3	4 5 6 7	BYTE 3 0 1 2 3	4 5 6 7	Hex Value in Field
Format Configurations	CA	CS	OP	0 CB/CD	0	0	0	0	CX	CH	CL	
	CA	CS	OP	0 CD	0	0	0	1	CX	CH	CL	
	CA	CS	OP	0 CB	0	0	1	0	CX	CH	CL	
	CK	CS	OP	0 CB/CD	0	1	0	0	CX	CH	CL	
	CK	CS	OP	0 CD	0	1	0	1	CX	CH	CL	
	CK	CS	OP	0 CB	0	1	1	0	CX	CH	CL	
	Ck gated to A-Register per byte 2, bit 7 A-Entry	Status Set/Reset	ALU Control	ME B entry and Destination	FM Specifies that format is not A, B, or C	KK Defines bits 0-3 of byte 0	ND Defines bits 3-7 of byte 1	NB	Bits 8–11 of IAR If format specifies CK field for A-Bus entry: CX(7)=0 if K<16. This directs CK field to A-Register bits 4-7 CX(7)=1 if K>15. This directs CK field to A-Register bits 0-3	Branch High (IAR Bit 12)	Branch Low (IAR Bit 13)	
0	0		A Ω B→D	SA						0	0	0
1	GC	1→ST1	A ● B→D	SB						1	1	1
2	ND	DNST21	A∀B→D	SC						Carry	D = 0	2
3	NC	1→ST3C	A + B→D	SD						ST0	Index ● ST1	3
4	TD	1→ST0	A + B + C→DC	GB						ST2	ST3C	4
5	TC	1→ST5	A - B + C→DC	GA						ST4	ST5	5
6	MD	1→ST6	A + B→DC	TB						ST6	ST7	6
7	MC	1→ST7	A - B + 1→DC	NA						BR0	BR1	7
8	GB	0→ST4		MB						BR2*	BR3**	8
9	GA	0→ST1		TA						BR4***	BR5****	9
A	NB	0→ST2		TD						BR6	BR7	A
B	NA	0→ST3C		MA						CHK-2	SELTD /MC7	B
C	TB	0→ST0		MD						COMMO ADDRO/MC6 SUPPO/XCHAN ILACT & DEV/ BOPAR	HLTIO/XFER SERVO/MULTI CUEND/BFRDY RSPON/CHANB	C
D	TA	0→ST5		GC								D
E	MB	0→ST6		BR								E
F	MA	0→ST7		MC								F

*During IMPL BR2 replaced by SECTR
**During IMPL BR3 replaced by BTRDY
***Following Spec Op 7, BR4 replaced by INLIN
****Following Spec Op 7, BR5 replaced by ILXEQ

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MICROWORD FORMAT E (ME, FM, KK, ND, NB = 00011)

- Indirect addressing (64-way branch) with address update capability.

A FORMAT DECODE

Decoding of format E (ME, FM, KK, ND, NB = 00011) sets up the following controls (see CTRL 500):

- Allows gating of GP registers to A register.
- Allows gating of GP registers to B register and to IAR (8-13).
- Allows gating of D ous to GP registers.

B CA FIELD (BYTE 0, BITS 0 - 3)

- Decoded to select a GP register to serve as A entry register.
- In the example, 1001 selects the GA register.

C CS FIELD (BYTE 0, BITS 4 - 7)

- Decoded to set or reset specific status (ST) bits.
- DNST21 sets ST(2) if the D bus is nonzero.
- ST(4) is set by hardware only; it cannot be set by the CS field.
- The example (0000) does not set or reset any status bits.

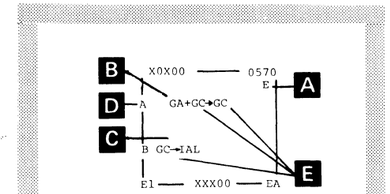
D OP FIELD (BYTE 1, BITS 0 - 2)

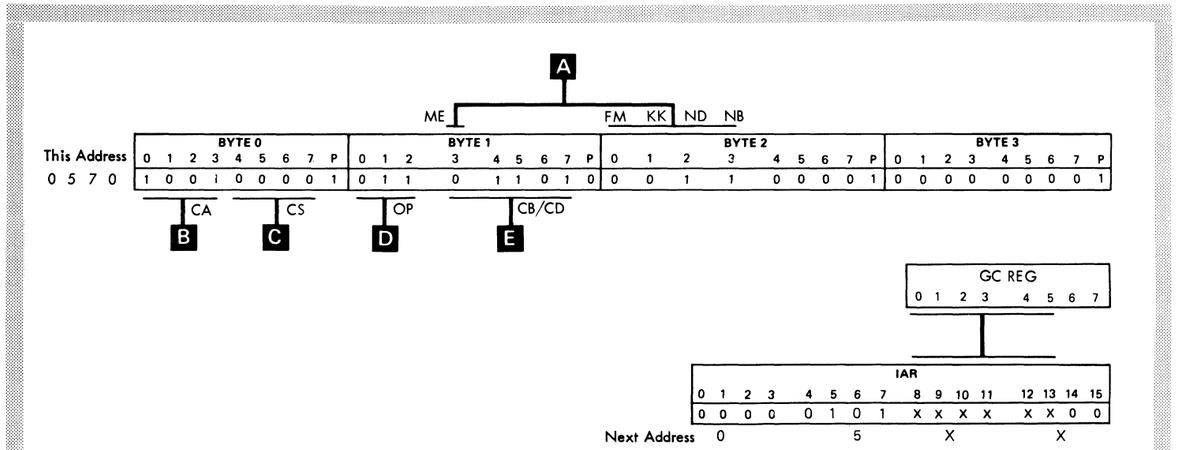
- Decoded to specify the ALU function to be performed.
- In the example, 011 is decoded as A+B→D.

E CB/CD FIELD (BYTE 1, BITS 3 - 7)

- Decoded to select a GP register to serve as a B entry and destination register.
- The initial contents of the selected register (bits 0-5) are also placed in the low-order byte of the IAR.
- In the example, '01101' selects the GC register.

Format E Example





Format E Bit Assignment Chart

Hex Value in Field	BYTE 0 CA (0 1 2 3) A Entry	BYTE 0 CS (4 5 6 7) Status Set/Reset	BYTE 1 OP (0 1 2) ALU Control	BYTE 1 0 CB/CD (3 4 5 6 7) ME B Entry and Destination	BYTE 2 (0 1 2 3) FM KK ND NB	BYTE 2 (4 5 6 7) Ignored	BYTE 3 (0 1 2 3 4 5 6 7) Ignored
0	0		A Ω B→D	SA			
1	GC	1 →ST1	A ● B→D	SB			
2	ND	DNST21	A ∀B→D	SC			
3	NC	1 →ST3C	A + B→D	SD			
4	TD	1 →ST0	A + B + C→DC	GB			
5	TC	1 →ST5	A − B + C→DC	GA			
6	MD	1 →ST6	A + B→DC	TB			
7	MC	1 →ST7	A − B + 1→DC	NA			
8	GB	0→ST4		MB			
9	GA	0→ST1		TA			
A	NB	0→ST2		TD			
B	NA	0→ST3C		MA			
C	TB	0→ST0		MD			
D	TA	0→ST5		GC			
E	MB	0→ST6		BR			
F	MA	0→ST7		MC			

MICROWORD FORMAT F (ME, FM, KK, ND, NB = 00111)

- Accomodates special operations required by CCU or user hardware.

A FORMAT DECODE

Decoding of format F (ME, FM, KK, ND, NB = 00111) sets up the following controls (see CTRL 500):

- Blocks ingating of A register and outgating of D bus.
- Allows special Op fields to be decoded.
- Allows gating of CX field to IAR(8-11)

B SPECIAL OP FIELD (BYTE 0, BITS 2, 3 AND BYTE 1, BITS 4 - 7)

- Decoded to activate 1 of 64 special operation controls.
- The 3830 Model 2 utilizes 24 special operation codes.
- In the example, 001110 selects special operation 14. Gate check 2 conditions to NA Register.

C CS FIELD (BYTE 0, BITS 4 - 7)

- Decoded to set or reset specific status (ST) bits.
- DNST21 sets ST(2) if the D bus is nonzero.
- ST(4) is set by hardware only; it cannot be set by CS field.
- The example (1111) resets ST(7). Note that ST(7) is reset after its status is tested (item F).

D CX FIELD (BYTE 2, BITS 4 - 7)

- Gated to bits 8-11 of IAR.

E CH FIELD (BYTE 3, BITS 0 - 3)

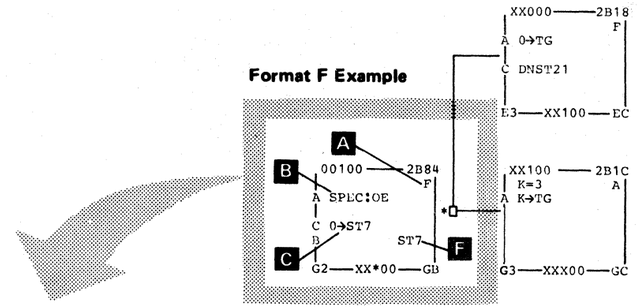
- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 0001 sets IAR(12) to 1 unconditionally.

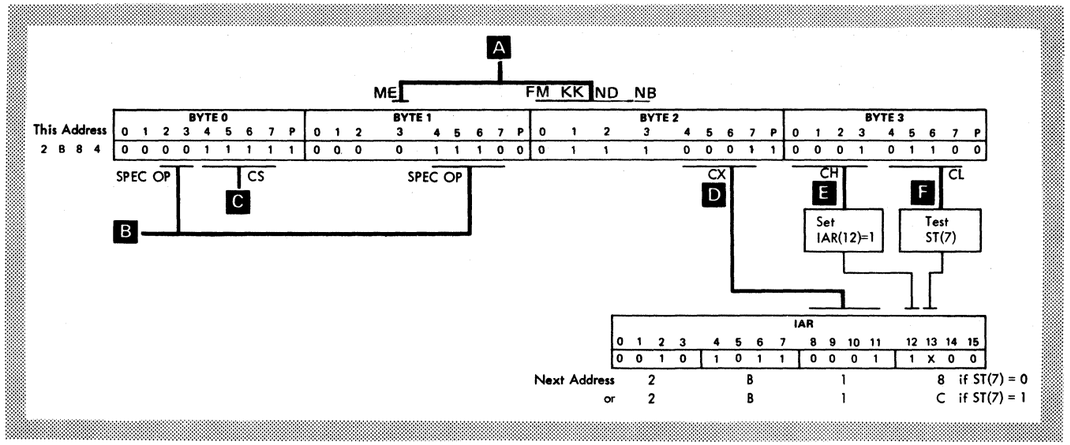
F CL FIELD (BYTE 3, BITS 4 - 7)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 0110 sets IAR(13) to 1 if ST(7) = 1 upon entering this microblock.

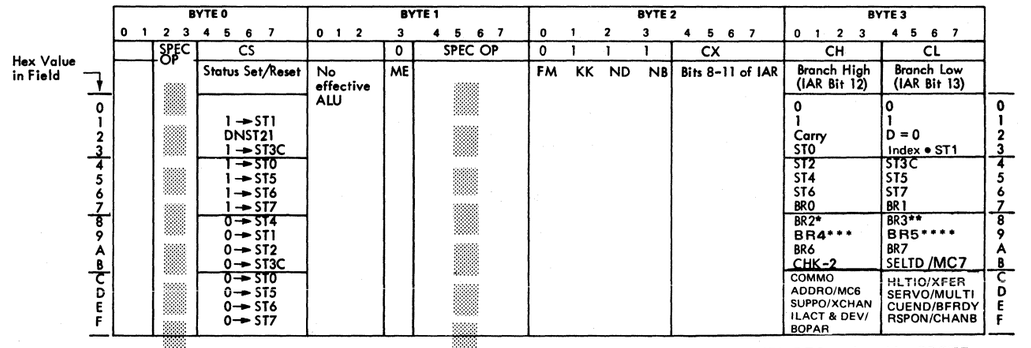
Sp Op 0	Pgm-Stop Statement
Sp Op 1	Chk-Stop Statement
Sp Op 2	Not Used
Sp Op 3	Error 2 Reset to User
Sp Op 4	Gate Read Error Pattern to NB
Sp Op 5	Reset Storage Error Register
Sp Op 6	Set Address Compare From SA & SB
Sp Op 7	INLIN (Inline) Branch in CE Mode and ILXEQ (Data Entry) Branch in CE Mode
Sp Op 8	Stop MPL Operation
Sp Op 9	Start MPL Operation
Sp Op 10	Gate MPL Data to SD Reg via D Bus
Sp Op 11	Not Used
Sp Op 12	Not Used
Sp Op 13	Load ND Register
Sp Op 14	Gate Check 2 Conditions to NA Reg
Sp Op 15	Set CI Bus In Parity Error
Sp Op 16	CI Response End
Sp Op 17	CI Recycle/Load CI Buffer from TA
Sp Op 18	Gate Alternate Branch Condition
Sp Op 19	Set Inline Active Latch/Set Dev Branch
Sp Op 20	Reset Inline Active Latch/Reset Dev Branch
Sp Op 21	Unfreeze Channel Switch
Sp Op 22	Allow Disable A
Sp Op 23	Allow Disable B
Sp Op 24	Gate Comparison Assist Latches to MB
Sp Op 26	Freeze Channel Switch
Sp Op 28	Selective Reset After Check-1
Sp Op 30	Propagate Select Out

Format F Example





Format F Bit Assignment Chart



*During IMPL BR2 replaced by SECTR
**During IMPL BR3 replaced by BTRDY
***Following Spec Op 7, BR4 replaced by INLIN
****Following Spec Op 7, BR5 replaced by ILXEQ

MICROWORD FORMAT 1 (ME, FM, KK, ND, NB = 10100/10101/10000)

- Fetch/store, with data address update capability.

A FORMAT DECODE

Three configurations of bits ME, FM, KK, ND, NB are used to define formats 1a, 1b, and 1c:

- Format 1a (10100)--four-byte fetch. The four bytes of data at the address specified by DAR(0-13) are fetched and placed in storage registers SA, SB, SC, SD.
- Format 1b (10101)--four-byte store. The data in SA, SB, SC, SD is stored at the address specified by DAR(0-13).
- Format 1c (10000)--one-byte fetch. The four bytes of data at the address specified by DAR(0-13) are fetched, but only the one byte indicated by DAR(14, 15) is placed in the SA register. The contents of SB, SC, SD remain unchanged.
- Following the fetch or store operation, the data address is updated by the ALU function K+B→B.

Decoding of format 1a, 1b, or 1c sets up the following controls (see CTRL 500):

- Allows gating of CK field to A register(4—7).
- Allows gating of GP registers to B register and to DAR(8—15).
- Allows gating of D bus to GP registers.
- Allows gating of CX field to IAR(8-11).
- Sets zeros in DAR(1-4).
- Allows gating of ML field to DAR(5-7).

B CK FIELD (BYTE 0, BITS 0 - 3)

- Gated to bits 4—7 of the A bus.

C CS FIELD (BYTE 0, BITS 4 - 7)

- Decoded to set or reset specific status (ST) bits.
- DNST21 sets ST(2) if the D bus is nonzero.
- ST(4) is set by hardware only; it cannot be set by the CS field.
- The example (0000) does not set or reset any status bits.

D ML FIELD (BYTE 1, BITS 0 - 2)

- Gated to bits 5-7 of DAR.

E CB/CD FIELD (BYTE 1, BITS 3 - 7)

- Decoded to select a GP register to serve as a B entry and destination register.
- The initial contents of the selected register are also placed in the low-order byte of DAR.
- In the example, 10110 selects the NB register.
- If no register is selected, zeros are placed in the low-order byte of DAR.

F CX FIELD (BYTE 2, BITS 4 -7)

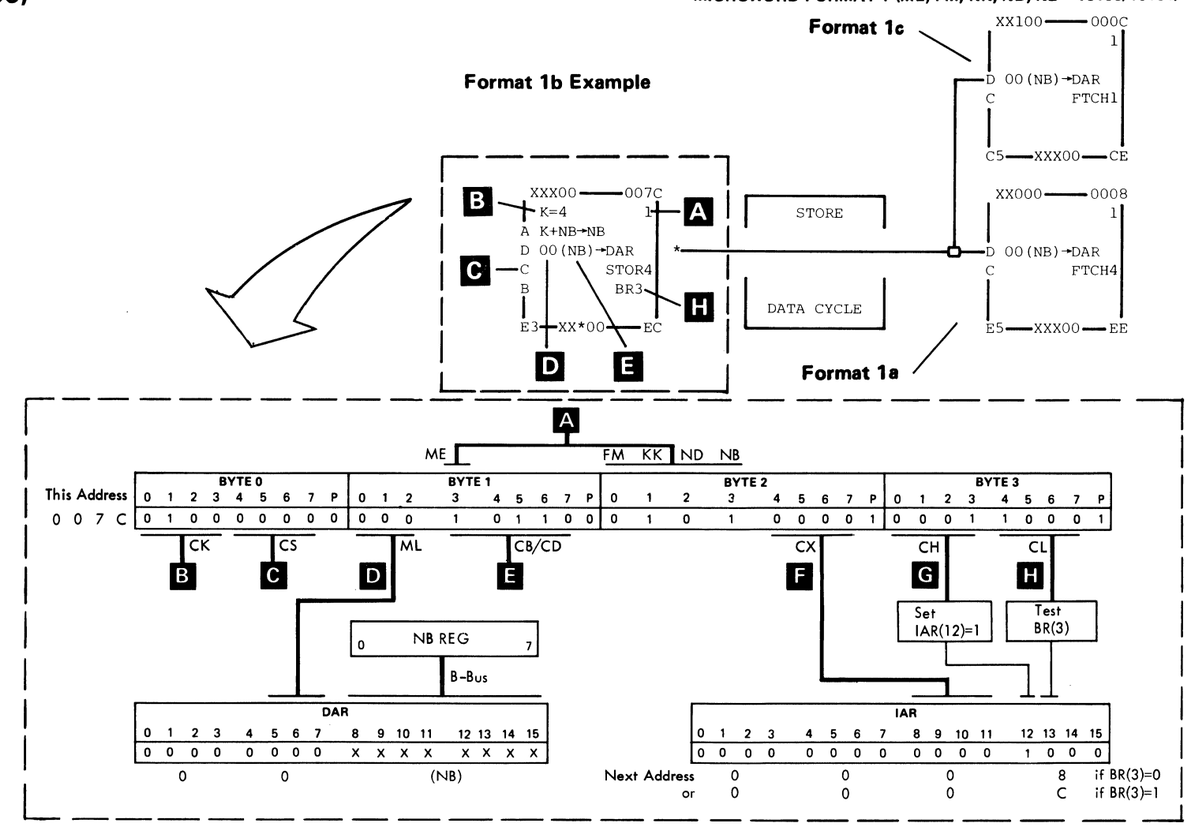
- Gated to bits 8-11 of IAR.

G CH FIELD (BYTE 3, BITS 0 - 3)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 0001 sets IAR(12) to 1 unconditionally.

H CL FIELD (BYTE 3, BITS 4 - 7)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 1000 tests for BR(3) being on.



Format 1 Bit Assignment Chart

Format Configurations / Hex Value in Field	BYTE 0 (0 1 2 3 4 5 6 7)		BYTE 1 (0 1 2 3 4 5 6 7)			BYTE 2 (0 1 2 3 4 5 6 7)					BYTE 3 (0 1 2 3 4 5 6 7)		
1a	CK	CS	ML	1	CB/CD	0	1	0	0	CX	CH	CL	
1b	CK	CS	ML	1	CB/CD	0	1	0	1	CX	CH	CL	
1c	CK	CS	ML	1	CB/CD	0	0	0	0	CX	CH	CL	
	A Bus Bits 4-7	Status Set/Reset	DAR Bits 5-7	ME	B Entry and Destination, and DAR Bits 8-15	FM	KK	ND	NB	Bits 8-11 of IAR	Branch High (IAR Bit 12)	Branch Low (IAR Bit 13)	
0					0						0	0	0
1		1→ST1			ST						1	1	1
2		DNST21			GD						Carry	D = 0	2
3		1→ST3C			TG						ST0	Index•ST1	3
4		1→ST0			ND						ST2	ST3C	4
5		1→ST5			NC						ST4	ST5	5
6		1→ST6			NB						ST6	ST7	6
7		1→ST7			TC						BR0	BR1	7
8		0→ST4			GF						BR2*	BR3**	8
9		0→ST1			GE						BR4***	BR5****	9
A		0→ST2			NF						BR6	BR7	A
B		0→ST3C			NE						CHK-2	SELTD/MC7	B
C		0→ST0			TF						COMMO ADDRO/MC6 SUPPO/XCHAN ILACT & DEV/ BOPAR	HLTIO/XFER SERVO/MULTI CUEND/BFRDY RESPON/CHANB	C
D		0→ST5			TE								D
E		0→ST6			MF								E
F		0→ST7			ME								F

*During IMPL BR2 replaced by SECTR
**During IMPL BR3 replaced by BTRDY
***Following Spec Op 7, BR4 replaced by INLIN
****Following Spec Op 7, BR5 replaced by ILXEQ

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MICROWORD FORMAT 2 (ME, FM, KK, ND, NB = 10110/10111)

- Four-byte fetch/store using any address in control storage.

A FORMAT DECODE

Two configurations of bits ME, FM, KK, ND, NB are used to define formats 2a and 2b:

- Format 2a (10110) -- four-byte fetch. The four bytes of data at the address specified by DAR (0-13) are fetched and placed in storage registers SA, SB, SC, SD.
- Format 2b (10111) -- Four-byte store. The data in SA, SB, SC, SD is stored at the address specified by DAR (0-13).

Decoding of format 2a or 2b sets up the following controls (see CTRL 500):

- Allows gating of MH field to A register (4—7) and to DAR (1—4)
- Allows gating of ML field to DAR (5-7)
- Allows gating of GP registers to B register and to DAR (8—15)
- Blocks gating of D bus to GP registers
- Allows gating of CX field to IAR (8-11)

B MH FIELD (BYTE 0, BITS 0 - 3)

- Gated to bits 1-4 of DAR.
- Contents are added to contents of register specified by CB field; result is placed on the D bus but is not gated to any register.
- In the example, the implicit ALU statement is 7+TE→D.

C CS FIELD (BYTE 0, BITS 4 - 7)

- Decoded to set or reset specific status (ST) bits.
- DNST21 sets ST (2) if the D bus is nonzero.
- ST (4) is set by hardware only; it cannot be set by the CS field.
- The example (1111) resets ST (7).

D ML FIELD (BYTE 1, BITS 0 - 2)

- Gated to bits 5-7 of DAR.

E CB FIELD (BYTE 1, BITS 3 - 7)

- Decoded to select a GP register to serve as B entry.
- The initial contents of the selected register are also placed in the low-order byte of DAR.
- If no register is selected, zeros are placed in the low-order byte of DAR.
- In the example, 11101 selects the TE register.

F CX FIELD (BYTE 2, BITS 4 - 7)

- Gated to bits 8-11 of IAR.

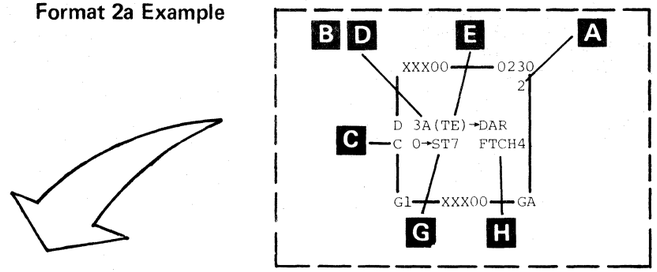
G CH FIELD (BYTE 3, BITS 0 - 3)

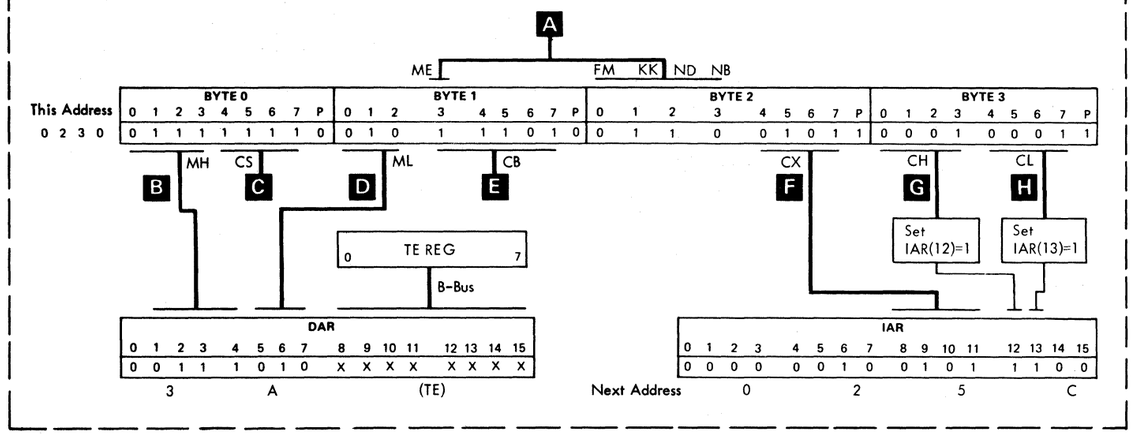
- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 0001 sets IAR(12) to 1 unconditionally.

H CL FIELD (BYTE 3, BITS 4 - 7)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 0001 sets IAR(13) to 1 unconditionally.

Format 2a Example





Format 2 Bit Assignment Chart

	BYTE 0		BYTE 1			BYTE 2				BYTE 3		
	0 1 2 3	4 5 6 7	0 1 2	3	4 5 6 7	0 1 2 3	4 5 6 7			0 1 2 3	4 5 6 7	
Format Configurations 2a	MH	CS	ML	1	CB	0 1 1 0	CX			CH	CL	
2b	MH	CS	ML	1	CB	0 1 1 1	CX			CH	CL	
Hex Value in Field	DAR Bits 1-4 and A bus Bits 4-7	Status Set/Reset	DAR Bits 5-7	ME	B Entry	FM KK ND NB	Bits 8-11 of IAR			Branch High (IAR Bit 12)	Branch Low (IAR Bit 13)	
0					0					0	0	0
1		1→ST1			ST					1	1	1
2		DNST21			GD					Carry	D = 0	2
3		1→ST3C			TG					ST0	Index•ST1	3
4		1→ST0			ND					ST2	ST3C	4
5		1→ST5			NC					ST4	ST5	5
6		1→ST6			NB					ST6	ST7	6
7		1→ST7			TC					BR0	BR1	7
8		0→ST4			GF					BR2*	BR3**	8
9		0→ST1			GE					BR4***	BR5****	9
A		0→ST2			NF					BR6	BR7	A
B		0→ST3C			NE					CHK-2	SELTD/MC7	B
C		0→ST0			TF					COMMO ADDRO/MC6 SUPPO/XCHAN ILACT & DEV/ BOPAR	HLTIO/XFER SERVO/MULTI CUEND/BFRDY RESPON/CHANB	C
D		0→ST5			TE							D
E		0→ST6			MF							E
F		0→ST7			ME							F

*During IMPL BR2 replaced by SECTR
**During IMPL BR3 replaced by BTRDY
***Following Spec Op 7, BR4 replaced by INLIN
****Following Spec Op 7, BR5 replaced by ILXEQ

MICROWORD FORMAT 3 (ME, FM, KK, ND, NB = 10010)

- One-byte fetch.
- Entire address is provided by the microword.

A FORMAT DECODE

Decoding of format 3 (ME, FM, KK, ND, NB = 10010) sets up the followina controls (see CTRL 500):

- Allows gating of NH field to A-register (4-7) and to DAR (8-11).
- Blocks gating of D-bus to GP registers.
- Allows gating of CX field to IAR (8-11).
- Sets zeros in DAR (1-4).
- Allows gating of ML field to DAR (5-7).
- Allows gating of NL field to DAR (12-15).

B NH FIELD (BYTE 0, BITS 0 - 3)

- Gated to bits 8-11 of DAR.

C CS FIELD (BYTE 0, BITS 4 - 7)

- Decoded to set or reset specific status (ST) bits.
- DNST21 sets ST(2) if the D-bus is nonzero.
- ST(4) is set by hardware only; it cannot be set by the CS field.
- The example (0000) does not set or reset any status bits.

D ML FIELD (BYTE 1, BITS 0 - 2)

- Gated to bits 5-7 of DAR.

E NL FIELD (BYTE 1, BITS 4 - 7)

- Gated to bits 12-15 of DAR.

F CX FIELD (BYTE 2, BITS 4 - 7)

- Gated to bits 8-11 of IAR.

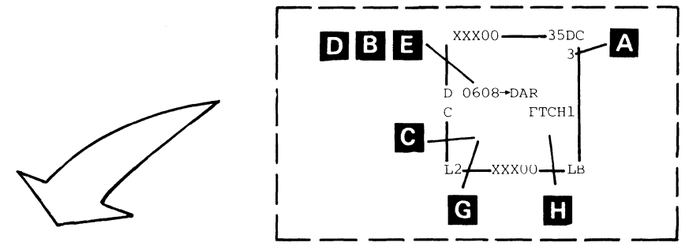
G CH FIELD (BYTE 3, BITS 0 - 3)

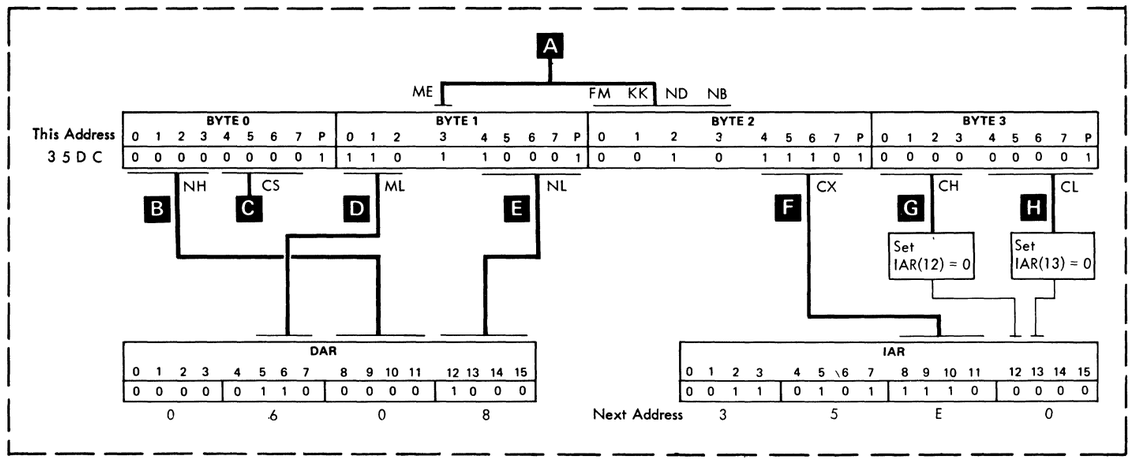
- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 12 to 1.
- In the example, 0000 sets IAR(12) to 0 unconditionally.

H CL FIELD (BYTE 1, BITS 4 - 7)

- Senses a hardware condition to determine a branch.
- If satisfied, sets IAR bit 13 to 1.
- In the example, 0000 sets IAR(13) to 0 unconditionally.

Format 3 Example





Format 3 Bit Assignment Chart

Hex Value in Field	BYTE 0 NH (0 1 2 3)	BYTE 0 CS (4 5 6 7)	BYTE 1 ML (0 1 2)	BYTE 1 (3)	BYTE 1 NL (4 5 6 7)	BYTE 2 (0 0 1 0)	BYTE 2 CX (4 5 6 7)	BYTE 3 CH (0 1 2 3)	BYTE 3 CL (4 5 6 7)	
▼	DAR bits 8-11 and A bus bits 4-7	Status Set/Reset	DAR bits 5-7	ME	DAR bits 12-15	FM KK ND NB	Bits 8-11 of IAR	Branch High (IAR Bit 12)	Branch Low (IAR Bit 13)	
0								0	0	0
1								1	1	1
2		1 → ST1						Carry	D = 0	2
3		DNST21						ST0	Index•ST1	3
4		1 → ST3C						ST2	ST3C	4
5		1 → ST0						ST4	ST5	5
6		1 → ST5						ST6	ST7	6
7		1 → ST6						BR0	BR1	7
8		1 → ST7						BR2*	BR3**	8
9		0 → ST4						BR4***	BR5****	9
A		0 → ST1						BR6	BR7	A
B		0 → ST2						CHK-2	SELTD/MC7	B
C		0 → ST3C						COMMO	HLTIO/XFER	C
D		0 → ST0						ADDRO/MC6	SERVO/MULTI	D
E		0 → ST5						SUPPO/XCHAN	CUEND/BFRDY	E
F		0 → ST6						ILACT & DEV/ BOPAR	RESPON/CHANB	F
		0 → ST7								

*During IMPL BR2 replaced by SECTR.
**During IMPL BR3 replaced by BTRDY.
***Following Spec Op 7, BR4 replaced by INLIN.
****Following Spec Op 7, BR5 replaced by ILXEQ.

MICROPROGRAM INSTRUCTION EXAMPLES (Part 1 of 2)

- Examples of the standard microprogram block operation are given.
- Examples of some more difficult to understand microprogramming techniques are given.

```
X1X00——2F28
|              A|
A 0→SA          |*
|               |
|               |
N6——XXX00——NF
```

Set the SA register to all zeros.

```
XXX00——2F08
| K=7           A|
A K→GB           |*
|                |
B           D=0  |
|                |
N3——XX*00——NC
```

Set the GB register = 7 from the emit field (K).

Set branch low condition if the D bus was zero in the last block.

```
0XX00——148C
| K=-70         A|
A K→SA           |*
|                |
|                |
E8——XXX00——EH
```

Set the SA register with the complement of 70 (185).

```
XXX00——0430
|              A|
A 0+0→TG         |*
|                |
|                |
L4——XXX00——LD
RESET MPL FILE
TAGS
```

Set the TG register to zero. No input from A or B register to the ALU.

Add 4 from emit field to contents of NC. Place results in NC register. Update address for next data cycle.

```
XXX00——2F80
| K=4           1|
A K+NC→NC        |
*D 02(NC)→DAR    |*
C          STOR4 |
B CARRY          |
|                |
C2——X*X00——CB
RESET CONTROL
STORAGE
```

Set the DAR to address control storage on a data cycle. Address is hex 02xx, "xx" is contents of NC register on entry to this block.

Store four bytes from SA, SB, SC, and SD in control storage.

```
XX100——2F34
|              A|
A GA+GA→GA       |*
|                |*
|                |
N4——XXX00——ND
SHIFT SAMPLER
```

Add the contents of GA register to the contents of GA and place results in GA register. (GA has outputs to both A and B bus.)

```
XX100——141C
| K=255         |
A K+MB+C→MBC     |*
|                |
B           D=0  |
|                |
G6——XX*00——GF
```

Add 255 from emit field to the contents of the MB register plus a carry of one if ST3C=1 and place results in MB. If ST3C=0 on entry, MB is decreased by 1. If ST3C=0 on entry and MB=0, ST3C is not turned on. If ST3C=1 on entry, MB is not changed. ST3C is turned off if there is no carry. ST3C is turned on if there is a carry.

```
XX100——13A4
|               D|
A 0-0+C→GCC      |*
|                |
C 0→ST4          |
B           ST7  |
|                |
J4——XX*00——JD
```

A and B registers = 0. B register is complemented to = 255. If ST3C = 1, GC register is set to 0 and ST3C is set to 1. If ST3C = 0, GC register is set 255 and ST3C is reset to zero.

```
XXX00——14AC
| K=-1          A|
A K+MC→MCC       |*
|                |
B CARRY  ST3C    |
|                |
G9——X**00——GJ
```

CARRY is set by a carry out of the ALU. If turned on in a block it stays on for the first part of the next block for branching. ST3C is set by a carry out of a ALU operation if "C" is added to D bus statement. ST3C stays on until reset by 0→ST3C or no carry out of ALU with "C" statement. For both CARRY and ST3C, branch condition is result of conditions set up before entering block.

```
XX100——1054
| K=32          A|
A K+SC→DC        |*
|                |
B          BR3   |
|                |
L5——0X*00——LE
   WRITE
CHECK FILE MASK
FOR ALLOW NO
WRITE
```

Add 32 to contents of SC register and place results on D bus only. "C" causes ST3C to be turned on if there is a carry out of ALU.

```
00X00——0B40
| K=0           D|
A K+0→MCC        |
|                |
C 0→ST5          |
|                |
Q7——01X00——QG
ZERO STATUS
```

Add an emitted zero to zero. Set MC register to zero. Turn off ST3C as there can be no carry out (MC "C").

```
X0X00——0C80
| K=1           A|
A K+GA→GA        |*—D-
*|               |
B CARRY          |
F 2              |
J4——X*X00——JD
INTERRUPTS GONE-
DELAY BEFORE
SAMPLING
```

Add one to contents of GA register and place result in GA. Loop in this block until carry out sets CARRY.

```
XXX00——17E0
|               D|
A NA-SD+1→D      |
|                |
C DNST21         |
B ST0            |
|                |
L4——X*X00——LD
COMPARE
```

Add the complement of the contents of SD to the contents of NA register plus a forced carry in of 1. Place results on the D bus.

If D bus is not zero ST2 is set to 1. If D bus is zero ST2 is unchanged.

```
XXX00——1494
| K=-0          A|
A K+0+C→DC       |*
|                |-
|                |
N8——XXX00——NH
DUMMY WORD TO
FORCE CARRY
```

ST3=1 ←

Add complement of zero (255) to zero plus carry of 1 (ST3C = 1) and set ST3C to 1. This is done to force a carry branch in the next block.

```
X0100——2444
| K=18          A|
A K-SC+1→D       |*—□
|                |
B ST4            |
|                |
N9——X*100——NJ
```

ST4 is turned on by the data transfer circuits when a new byte is ready or wanted. Loop in this block until ST4 = 1.

```
X0X00——2F20
|               D|
A GA.SA→D        |
-|               |*
C 0→ST2          |
|                |
N2——XXX00——NB
TEST IF DEVICE
INTERRUPT TO
RESET
```

AND contents of GA and SA registers. Place results on the D bus. D = 0 branch checks the result in the next block. AND gives a 1 output if both inputs are 1. 0 is placed in ST2.

```
XX000——2F78
|              A|
A GA Ω NB→NB     |*
|                |
|                |
F 2              |
Q4——XX100——QD
OR BIT SIG ADDRESS
OF PACK CHANGE
INTERRUPTS
TOGETHER
```

OR contents of GA and NB registers. Place results in NB register. OR gives a 1 output if either input is 1.

```
X1X00——2F8C
| K=00001001-A  |
A K⊻GD→GD        |*
|                |
|                |
F 2              |
G4——XX100——GD
UPDATE ADDRESS TO
RESET RESERVED
BUSY TO, AND
INTERRUPT BYTES
FOR RESETTING
CHANNEL.
```

Exclusive OR nine from emit field with contents of GD register. Place results in GD register. Exclusive OR gives a 1 output if one and only one input is 1. In this example bits 4 and 7 of the GD register will be inverted.

```
XXX00——2F70
|               1|
|                |
D 02(GD)→DAR     |*
C          FTCH1 |
|                |
F 2              |
E6——XXX00——EF
FETCH BUSY TO
BYTES
```

"2" Indicates that this block is used on two channel switch feature only.

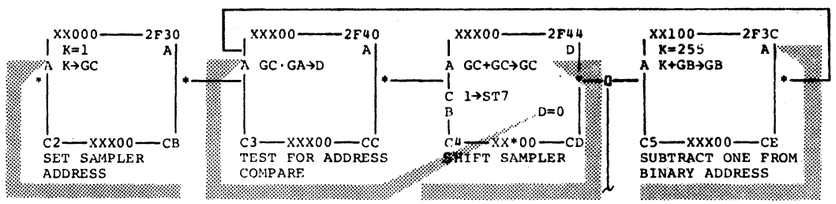
Read four bytes out of control storage. Place the byte selected by the two low order bits of DAR in the SA register.

```
XXX00——0C38
|               3|
|                |
D 02C8→DAR       |*
C 0→ST3C FTCH1   |
|                |
F 2              |
L7——XXX00——LG
FETCH BUSY TO
CHANNEL A BYTE
```

Address control storage at hex 02C8. ST3C is set to 0.

MICROPROGRAM INSTRUCTION EXAMPLES (Part 1 of 2)

MICROPROGRAM INSTRUCTION EXAMPLES (Part 2 of 2)

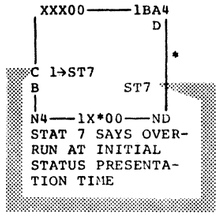


Set up GC register to use it as a counter.

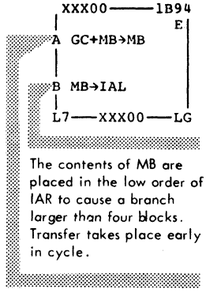
Check counter (GC) with contents of GA (only one bit is on). Stay in loop until equal (D bus ≠ 0).

Add contents of (GC) to GC and place results in GC. This results in shifting the bit one position to the left.

Add 225 to the contents of GB register and place results in GB. This decrements GB by one.



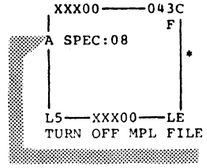
ST7 is the low order branch condition in this block. ST 7 is turned on (1→ST 7) after the branch has been set up.



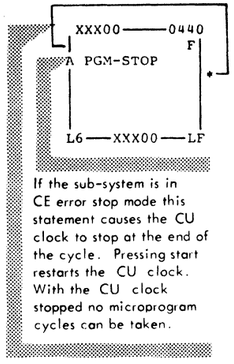
The contents of MB are placed in the low order of IAR to cause a branch larger than four blocks. Transfer takes place early in cycle.

A constant in GC is added to the contents of MB and placed in MB register (late in cycle). This sets up MB for the next branch

HEX	PAGE
10	QE020CB
14	QE020GB
18	QE020LB
24	QE015EB
28	QE015NB
2C	QE040CA
30	QE040NA



Special operations are used to control operations outside of the CU. This special operation (hex 08) is used to turn off the MPL mode latch in the 23FD attachment and stop the drive motor in the 23FD.



If the sub-system is in CE error stop mode this statement causes the CU clock to stop at the end of the cycle. Pressing start restarts the CU clock. With the CU clock stopped no microprogram cycles can be taken.

In this example, if the clock is re-started, this block is re-addressed and the clock stops again. If the output of the block goes to another block, the microprogram will continue.

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MICROPROGRAM ROUTINES

The microprogram is divided into a number of routines. Each routine performs a basic function, but it may be used in different ways for a number of operations.

For example, a Read Data command following a Search ID command would:

Start in chained reselection

Go through Initial Selection to Command Decode

Present Status In Oriented Initial status

Go to load counts to clock key field

Go to read/clock file to clock key field

ECC processing

Re-entry control

Gap spacing

Back to load counts for the data field

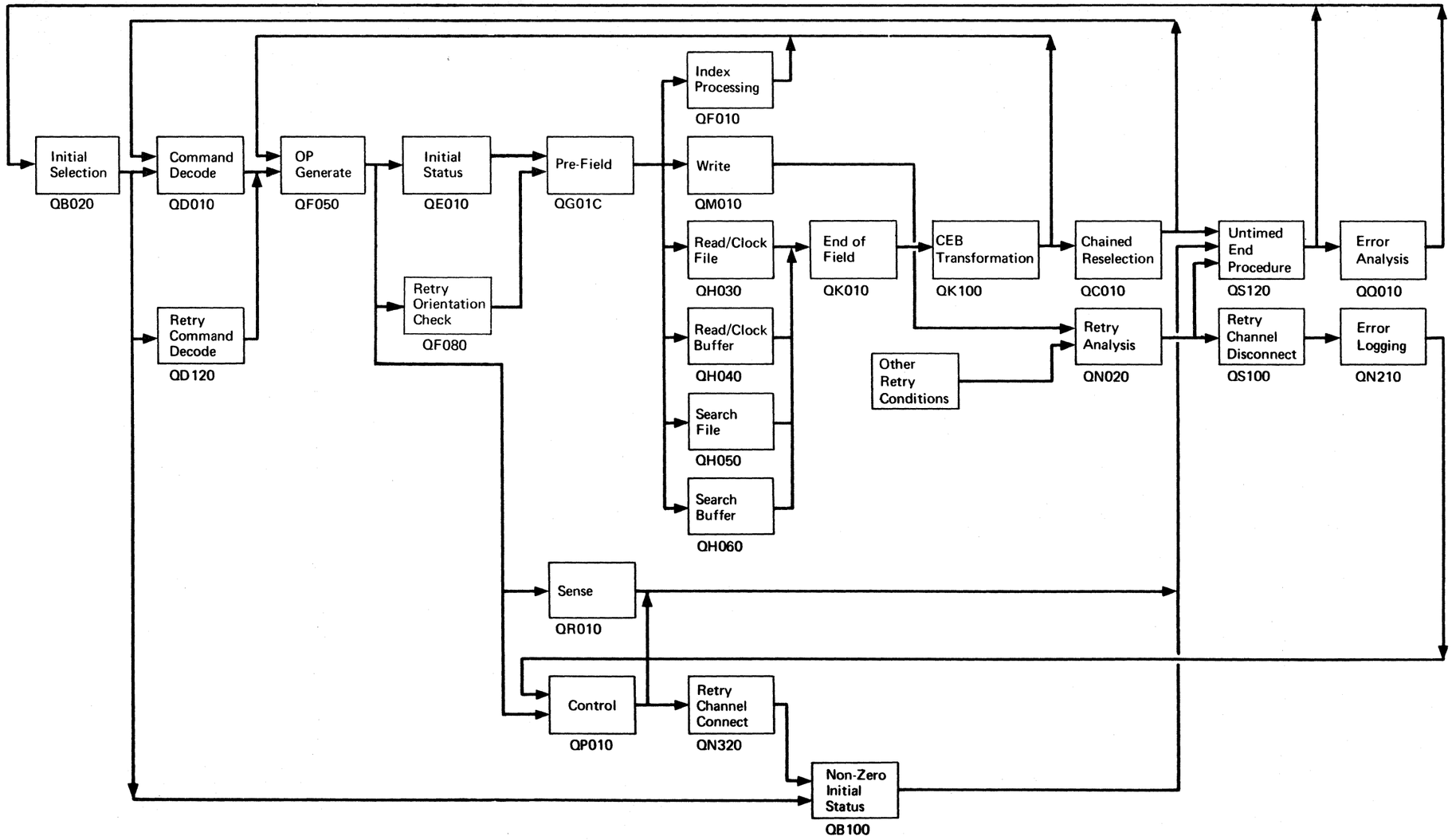
Read/clock file to read data field

ECC processing

Back to chained reselection (if not the last command in the chain)

or

Untimed end procedure (if this is the last command in the chain)



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REGISTER EXPANSION FEATURE

The Register Expansion Feature is located on a Z512 card that is installed in location B1G2.

The Z512 card contains registers GF, MF, NF, and TF. The Z512 operates like a General Purpose Register until certain microprogram instructions are performed, at which time it assumes the following characteristics:

The MF, NF, and GF Registers become local store registers having 32 storage locations each. They are addressable from bits 3 thru 7 of the TF Register. This mode is reached by performing a microprogram Special Operation 12 ('0C') while TF Register bit 0 is on. To reset this mode, the same Special Operation is performed with TF Register bit 0 off.

While in the above mode, if TF Register bit 1 is on, bits 3 thru 7 of the TF Register become an incrementing register that is advanced whenever a CB of MF, CD of MF, or CD of TA occurs. If an MF to MF or MF to TA instruction is used, the register is only incremented once. Bit 1 on also loads the contents of the D-Bus into MF whenever a CD of TA occurs.

To guarantee correct parity in the TF Register, a parity predict circuit is examined everytime the address register is incremented. The parity of the TF Register is checked every machine cycle. When a failure occurs, a Type 1 error CB Decode Even Error is posted.

When the clock is stopped and the display switch is in the Register Display position, the local store position of the MF, NF, and GF Registers is defined by bits 3 thru 7 of the TF Register. This says that if these registers are being used as general purpose registers and you wish to display them, you must set TF to zero. (Refer to PANEL section for register store and display operation.)

CONTENTS

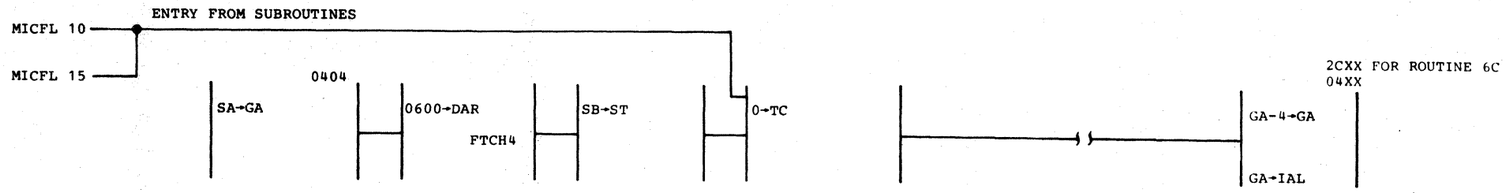
MICFL

CHANNEL WRAP DIAGNOSTIC DESCRIPTION (Part 1 of 3)

HOUSEKEEPING

EACH ROUTINE

1. Is loaded into control storage addresses 0400 – 05FC by the control program. Most routines also use the addresses between 2000 – 2FFC.
2. Begins in address 0404.
3. Begins with housekeeping that is used by the subroutines to reset the channel controls and branch to the next subroutine.
4. Returns to the control program only after all subroutines have been run on both channels A/C and B/D (unless running only one channel or looping on an error).



SETUP SUBROUTINE ADDRESS

EACH ROUTINE STARTS IN ADDRESS 0404. UPON ENTRY FROM THE CONTROL PROGRAM, THE SA REGISTER CONTAINS THE ADDRESS OF THE NEXT SUBROUTINE TO BE RUN (FC FOR INITIAL ENTRY).

FETCH CHANNEL OPTIONS AND CHANNEL ADDRESSES

0600 CONTAINS:

0600
NOT USED

0601
CHANNEL OPTIONS

BIT 2=1
RUNNING ONLY ONE CHANNEL

BITS 6 & 7
00 CHANNEL A
01 CHANNEL B
10 CHANNEL C
11 CHANNEL D

THIS BYTE IS LOADED DURING ROUTINE 60 BY A PARAMETER ENTRY.

THESE BYTES ARE LOADED DURING ROUTINE 64 AND WILL BOTH CONTAIN THE SAME ADDRESS IF RUNNING ONLY ONE CHANNEL.

0602
CONTROL UNIT ADDRESS RECEIVED VIA REQUEST IN SEQUENCE FOR CHANNEL A/C

0603
CONTROL UNIT ADDRESS RECEIVED VIA REQUEST IN SEQUENCE FOR CHANNEL B/D

PLACE CHANNEL OPTIONS IN SI REGISTER FOR MICRO BRANCHING

ST2=1
RUNNING ONLY ONE CHANNEL

ST6 & 7
RUNNING
00 CHANNEL A
01 CHANNEL B
10 CHANNEL C
11 CHANNEL D

RESET CHANNEL CONDITIONS

THIS AREA OF HOUSEKEEPING IS USED TO RESET CONDITIONS THAT WERE SET BY SUBROUTINES. EACH SUBROUTINE IS WRITTEN TO RUN ALONE USING ONLY HOUSEKEEPING. THIS GIVES THE ABILITY TO RUN ONLY ONLY ONE SUBROUTINE WITH THE LOOP-ON-ERROR OPTION.

BRANCH TO SUBROUTINE THEN DECREMENT SUBROUTINE ADDRESS

THIS WORD IS USED FOR A 64-WAY BRANCH INTO THE VARIOUS SUBROUTINES.

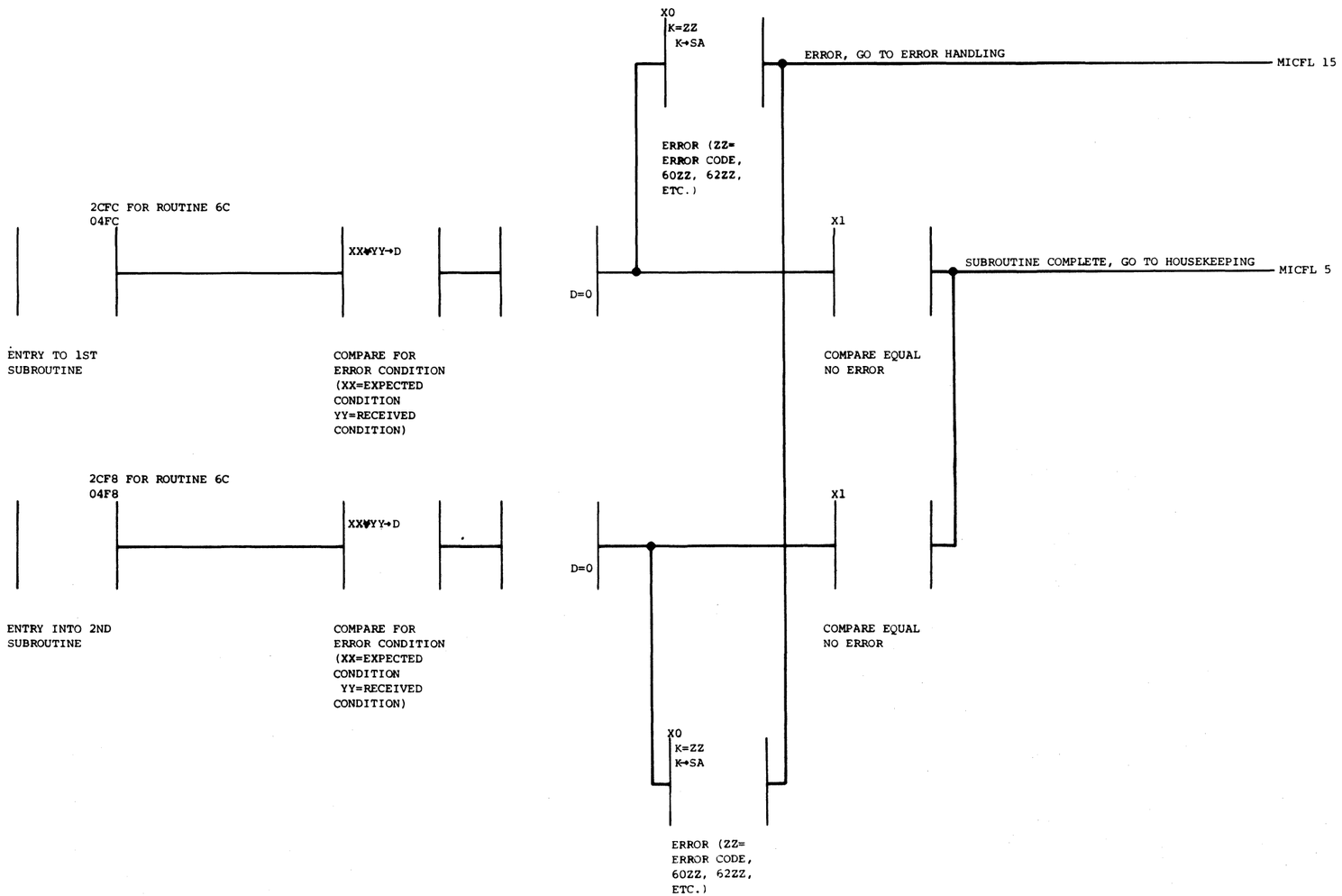
THIS WORD ALSO DECREMENTS THE SUBROUTINE COUNTER (GA REGISTER) TO POINT TO THE NEXT SUBROUTINE.

CHANNEL WRAP DIAGNOSTIC DESCRIPTION (Part 2 of 3)

SUBROUTINES

EACH SUBROUTINE (FC, F8, F4, ETC):

1. Is branched to by using the GA register for a 64-way branch.
2. Starts with FC, F8, F4, etc. (addresses 04FC, 04F8, 04F4, etc., except routine 6C, which uses addresses 2CFC, 2CF8, 2CF4, etc.).
3. Is self-sufficient, and requires only housekeeping to run, allowing the loop-on-error option to loop a single subroutine.

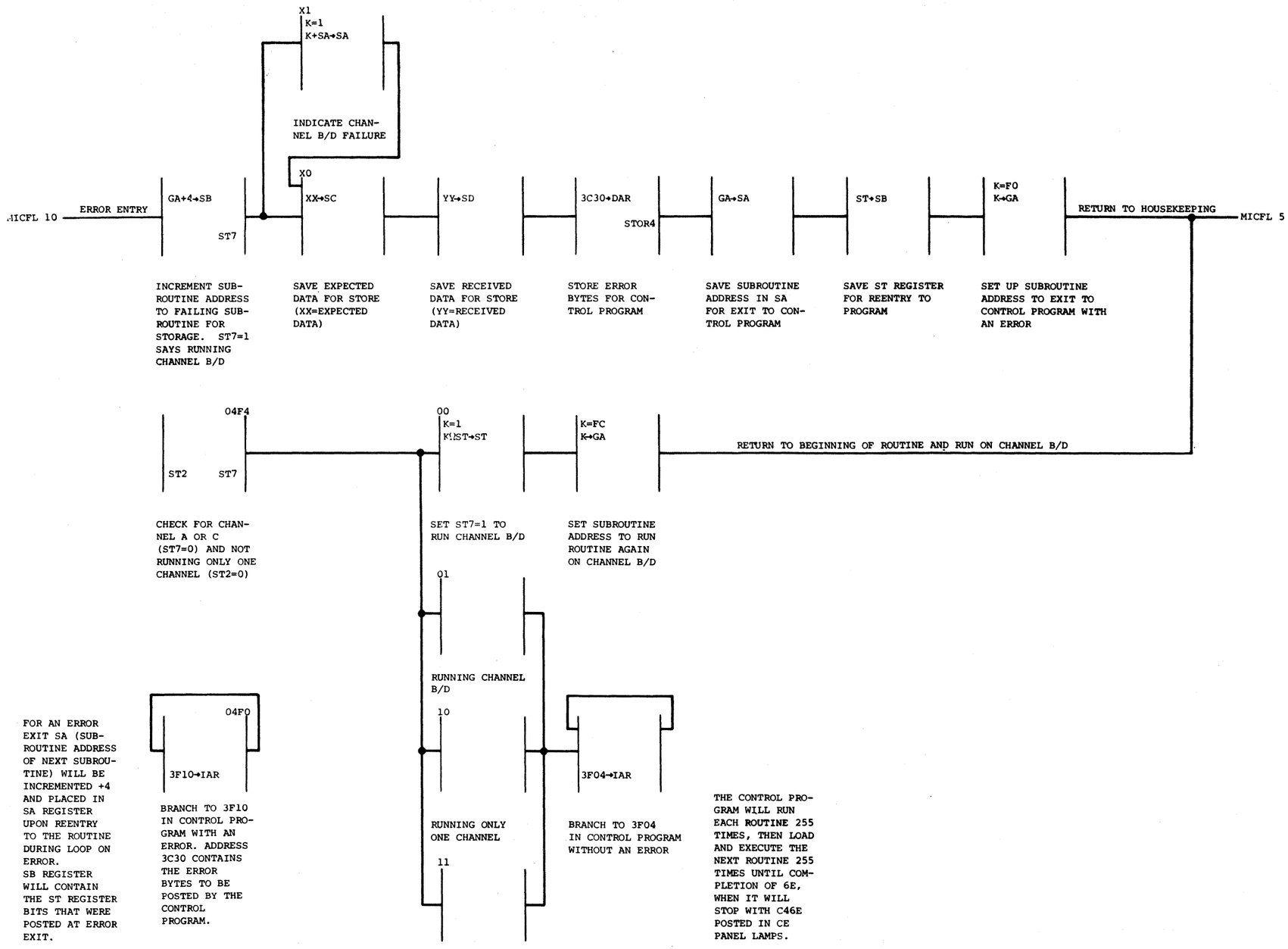


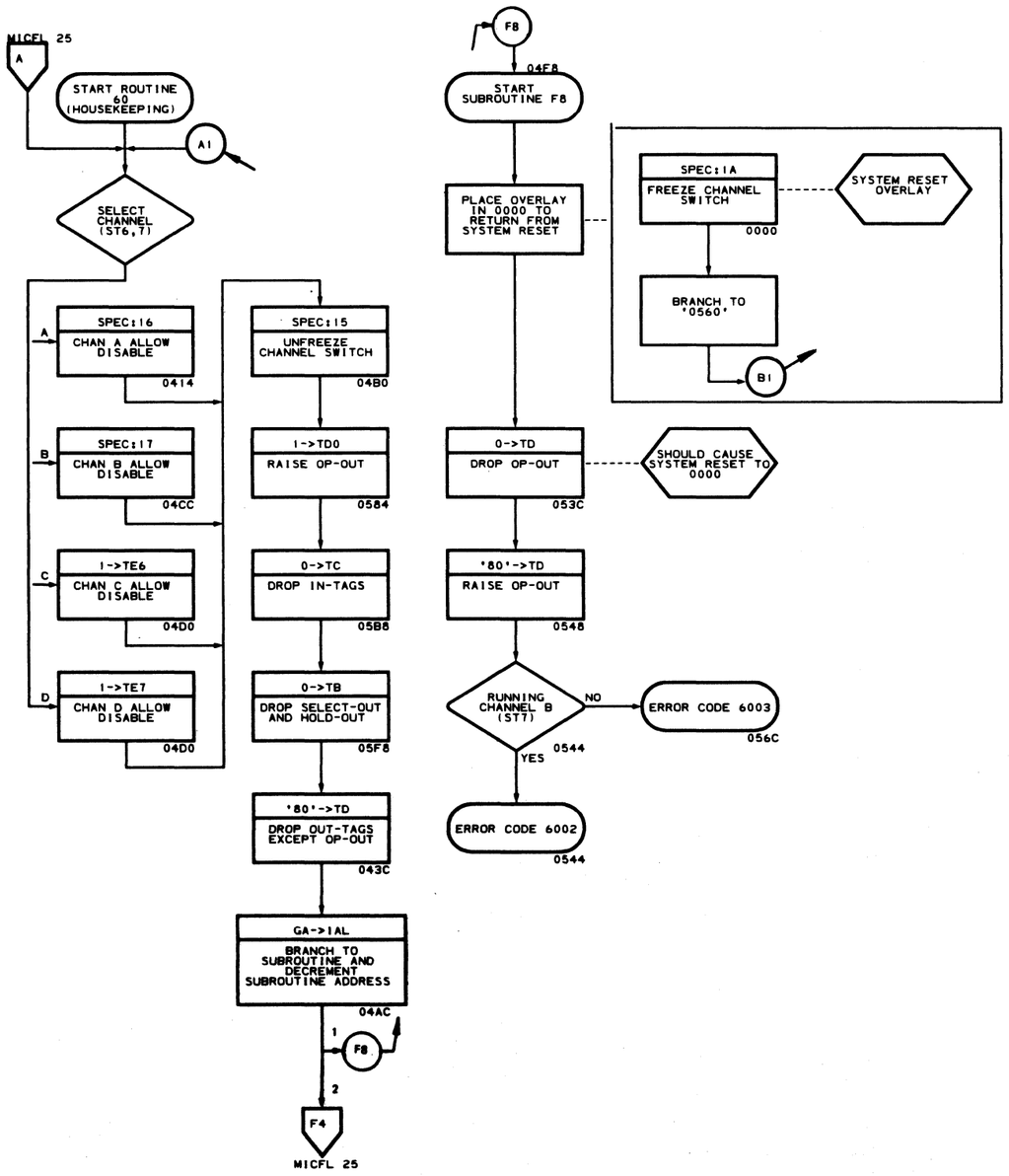
CHANNEL WRAP DIAGNOSTIC DESCRIPTION (Part 3 of 3)

ERROR HANDLING, ERROR AND NORMAL EXITS

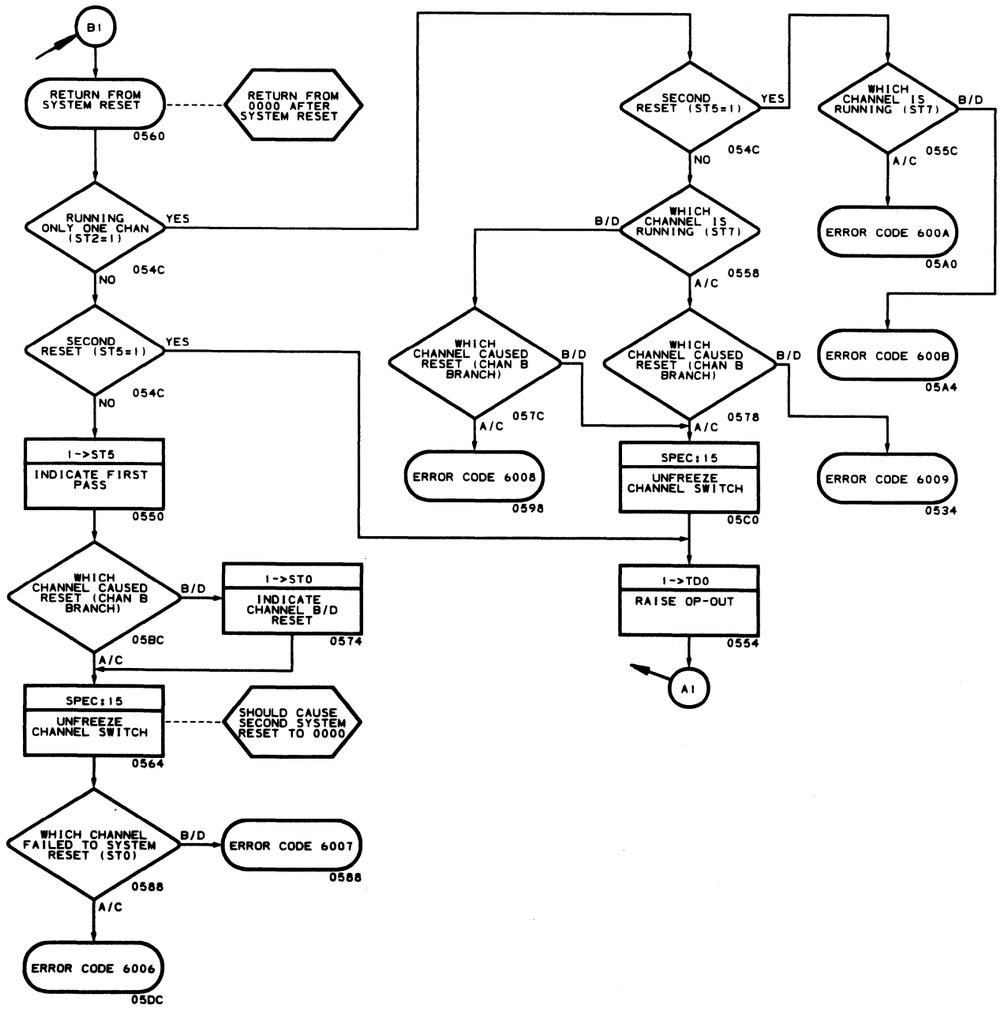
ERROR HANDLING:

1. Is branched directly into from an error.
2. Stores the subroutine address and error bytes in 3C30 for the control program display.
3. Sets the subroutine address for exit to the control program error entry (3F10).





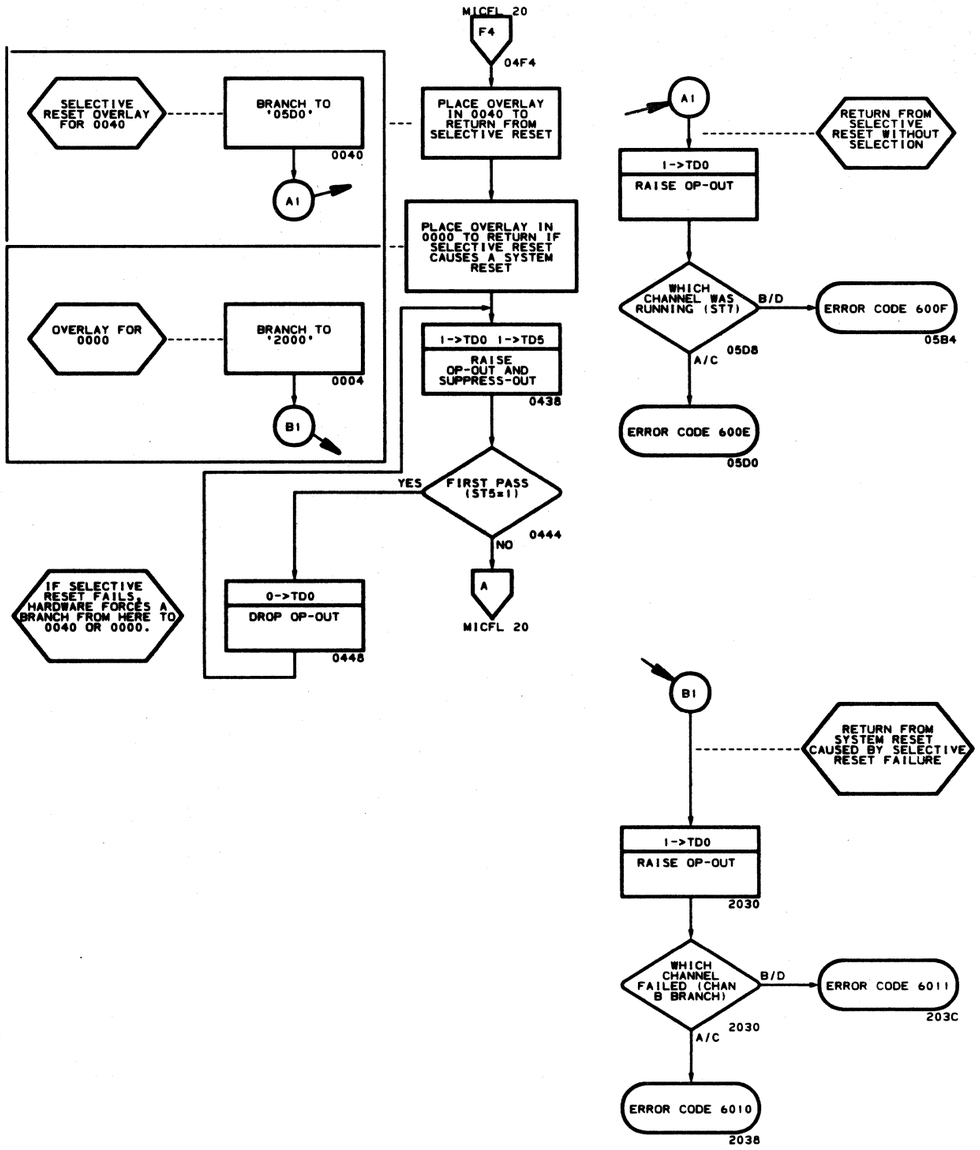
MLM0002_437408
MICFL_20_L
60A
JFL_11/22/72



MLM0002_437408
MICFL_20_R
60C
JFL_11/22/72

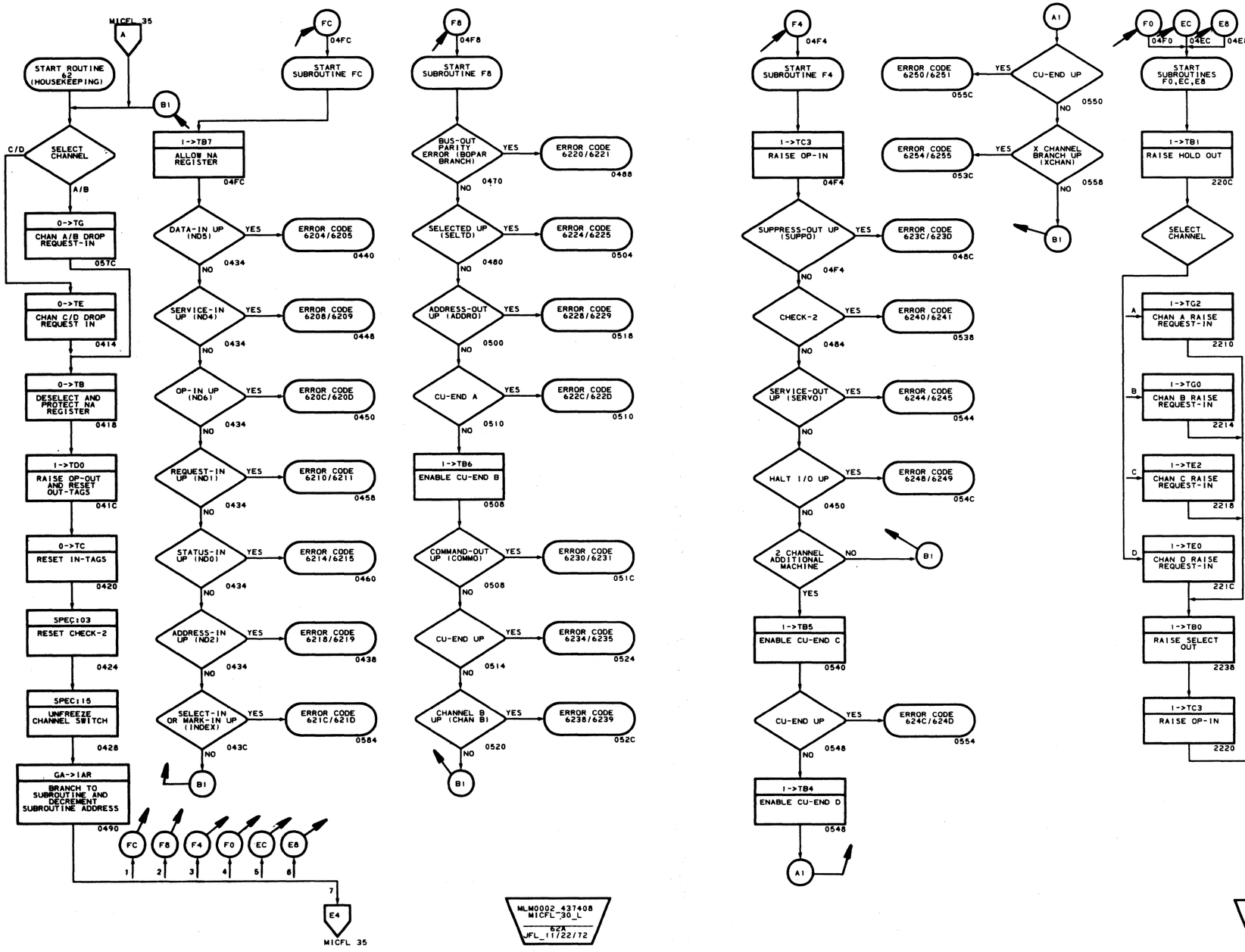
ROUTINE 60 (Part 2 of 2)

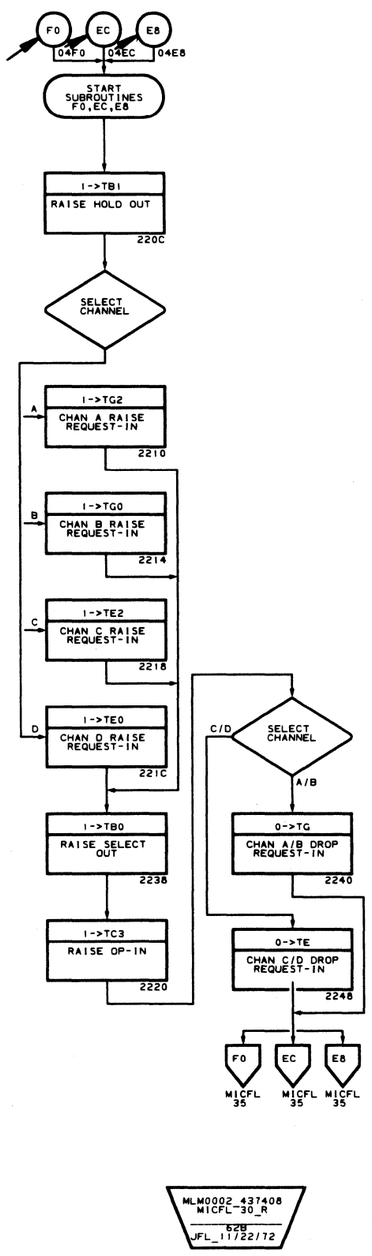
MICFL 25



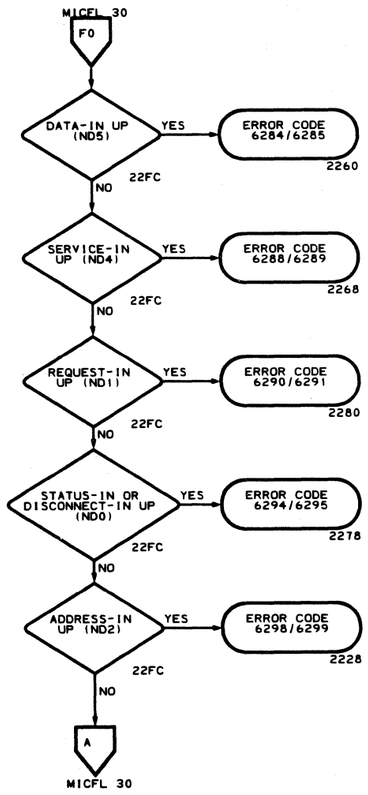
MLM0002_437408
MICFL_25_L
60E
JFL_11/22/72

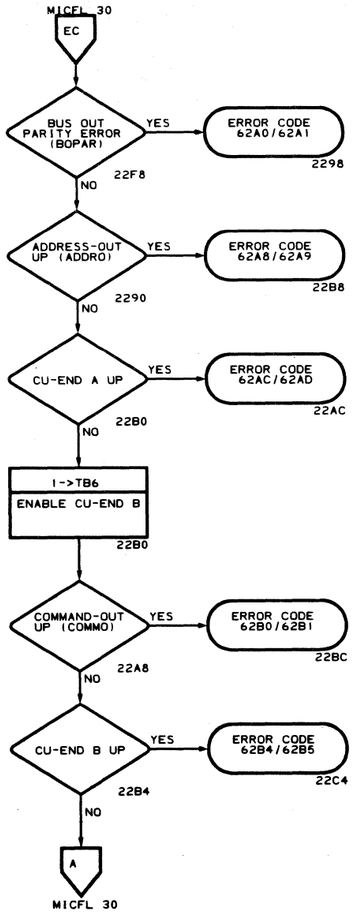
ROUTINE 62 (Part 1 of 2)

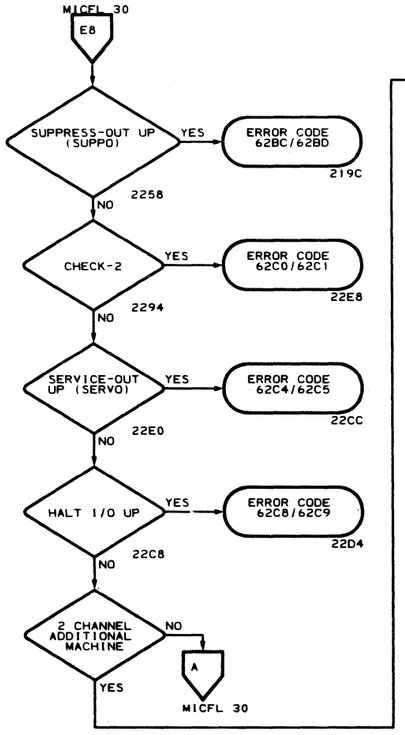


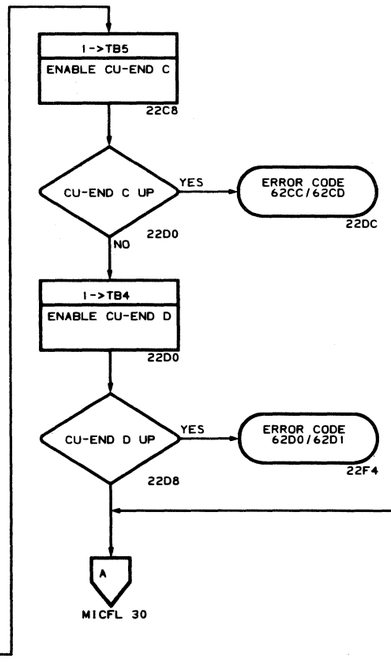


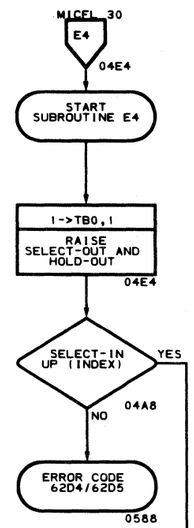
ROUTINE 62 (Part 2 of 2)



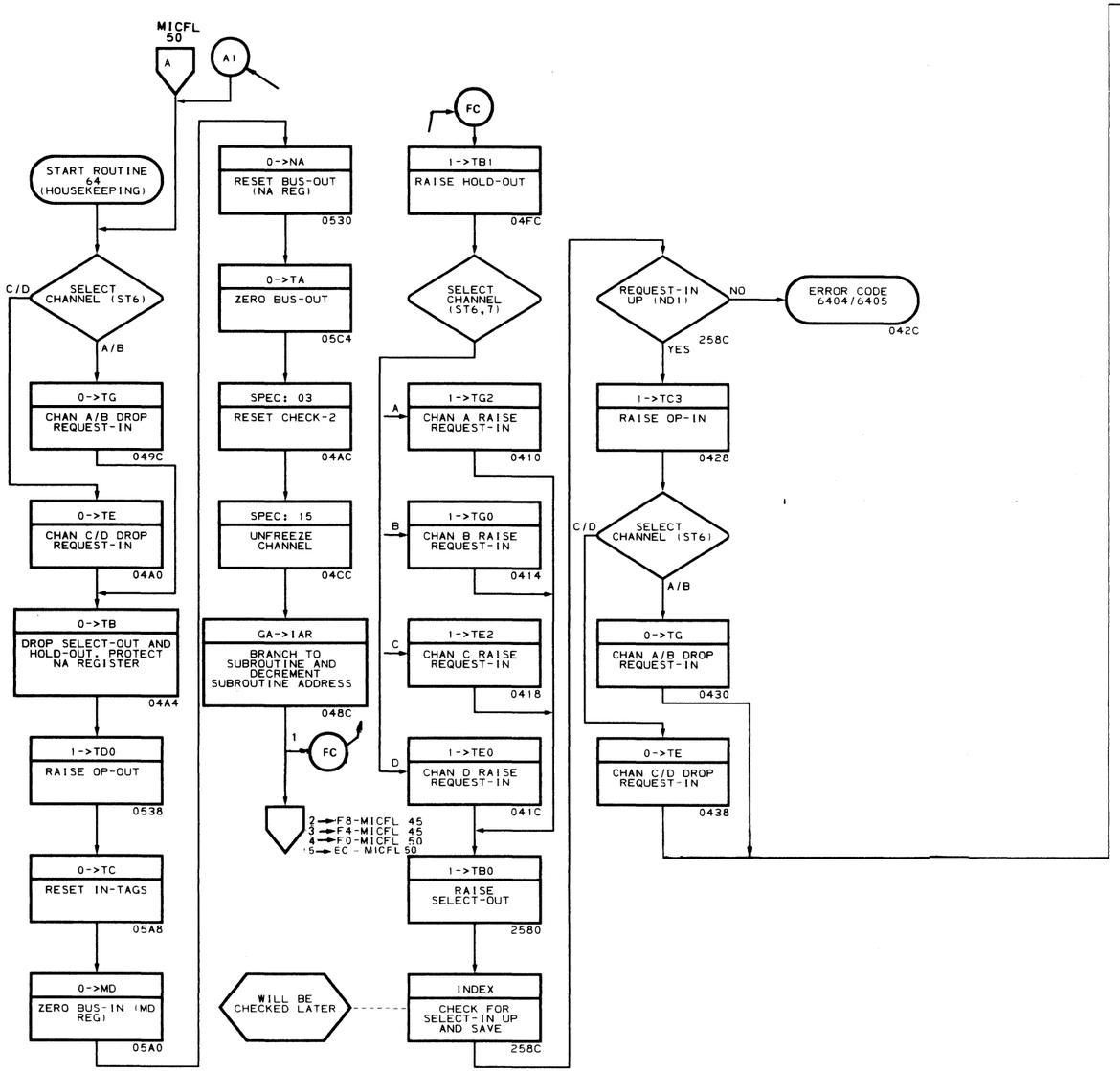


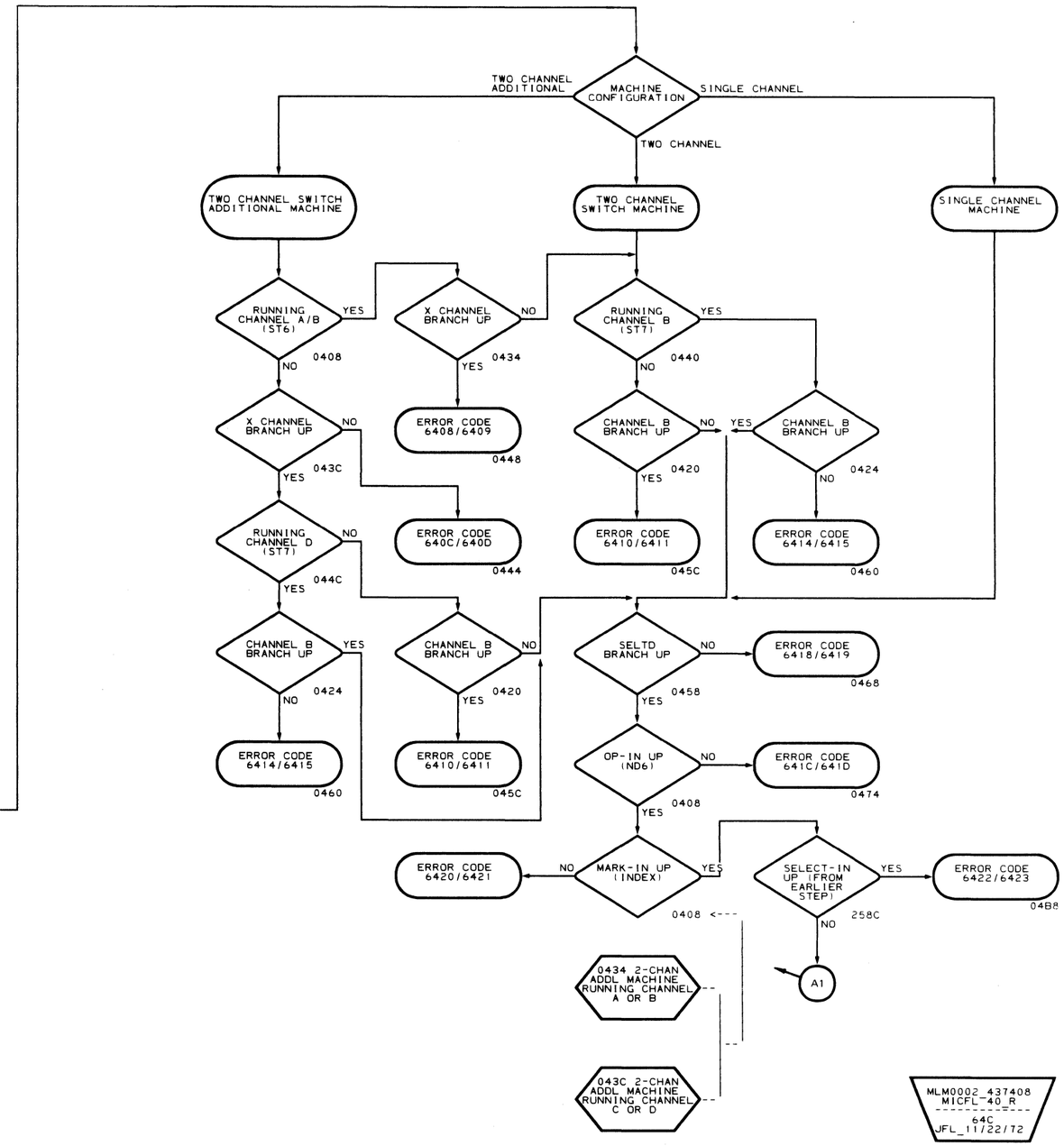






3830-2
CB0500 Seq 2 of 2
2354778 Part Number
437408 16 Oct 72

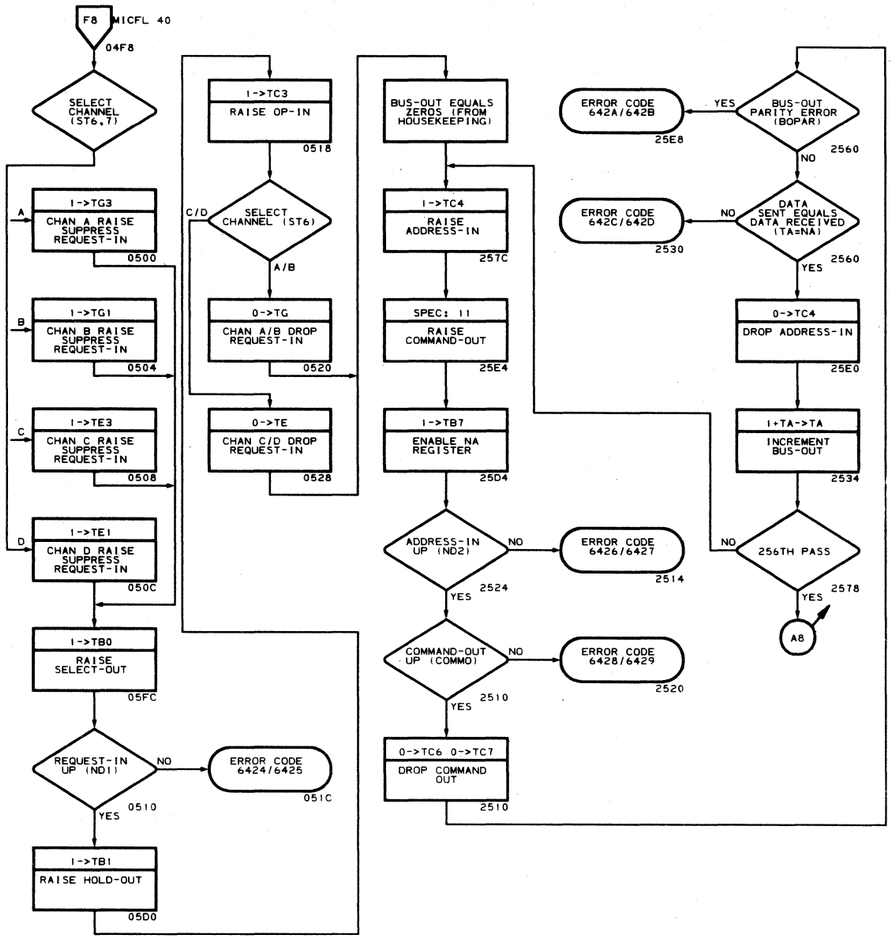


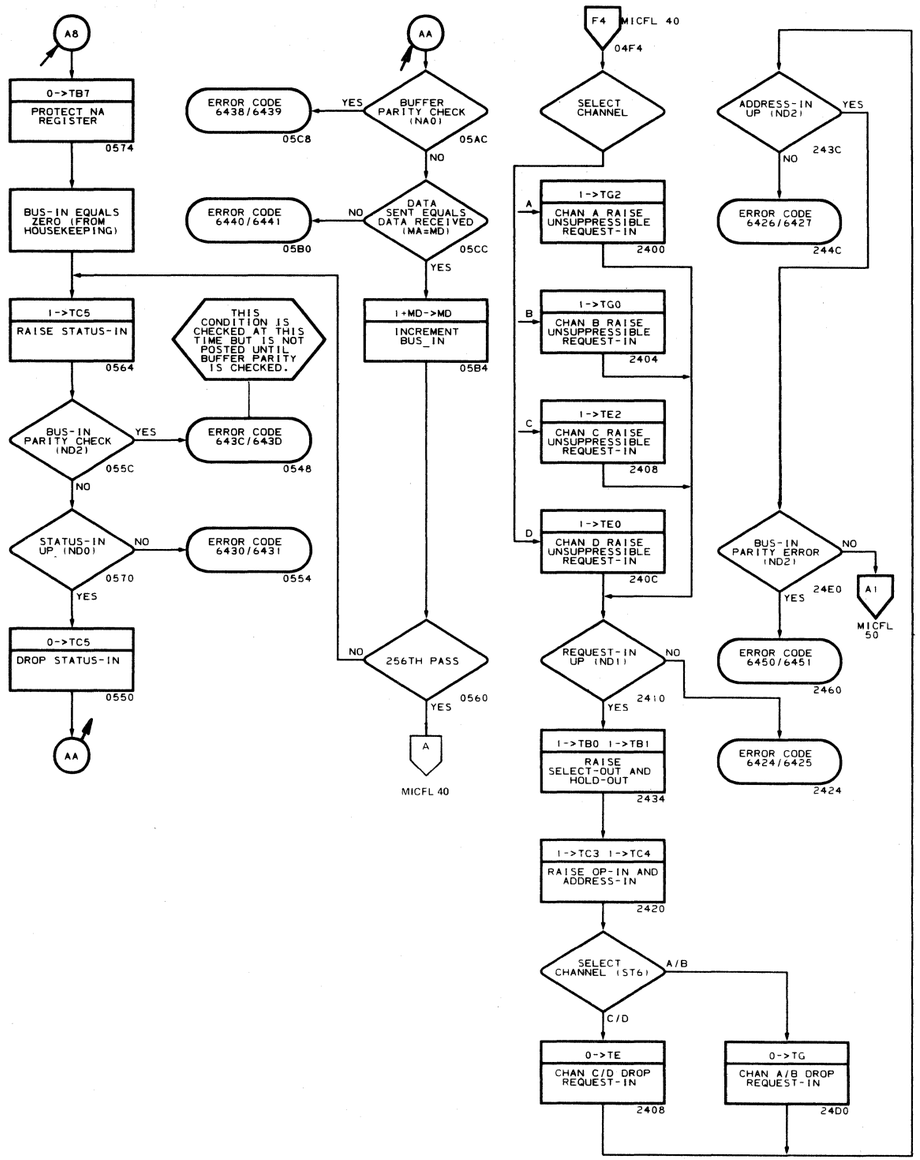


MLM0002_437408
MICFL_40_L
64A
JFL_11/22/72

MLM0002_437408
MICFL_40_R
64C
JFL_11/22/72

ROUTINE 64 (Part 2 of 3)



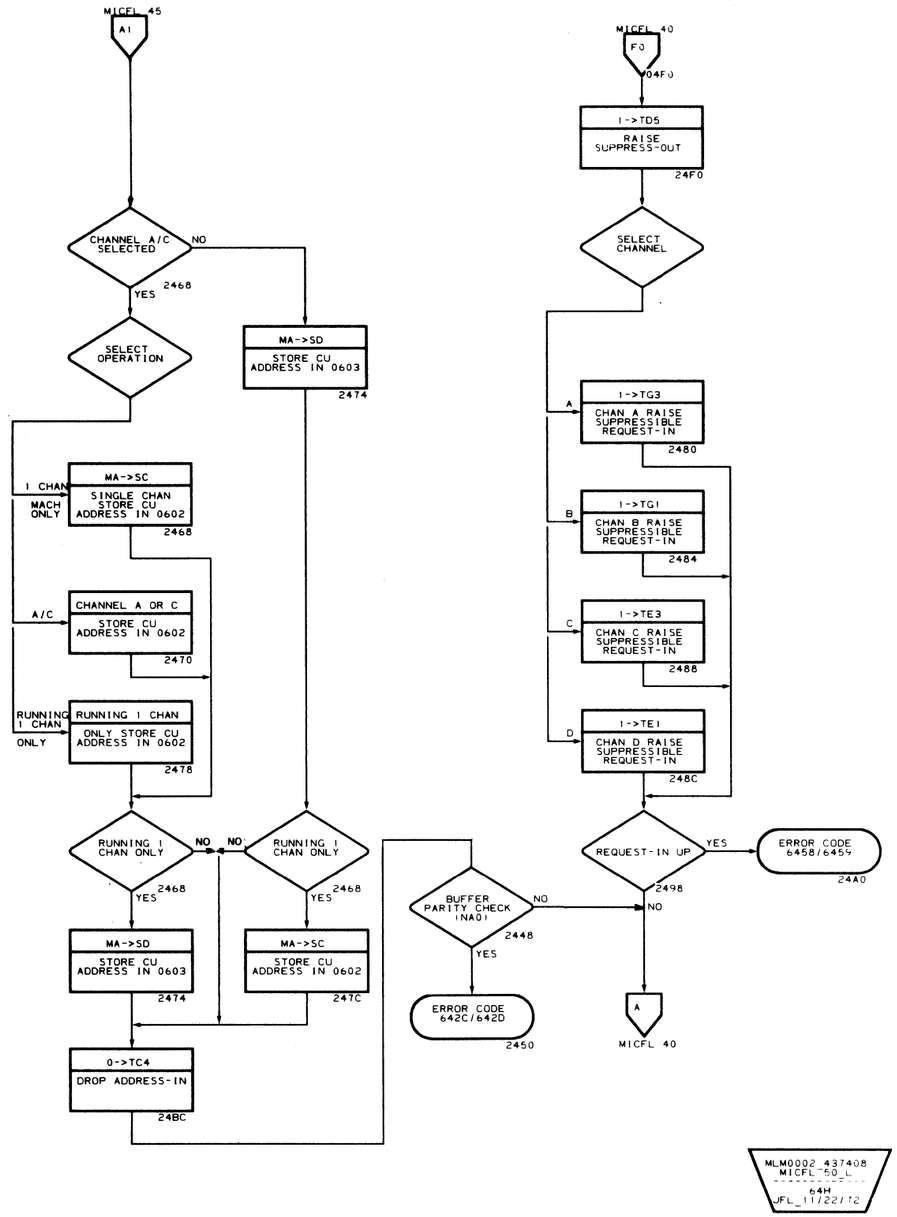


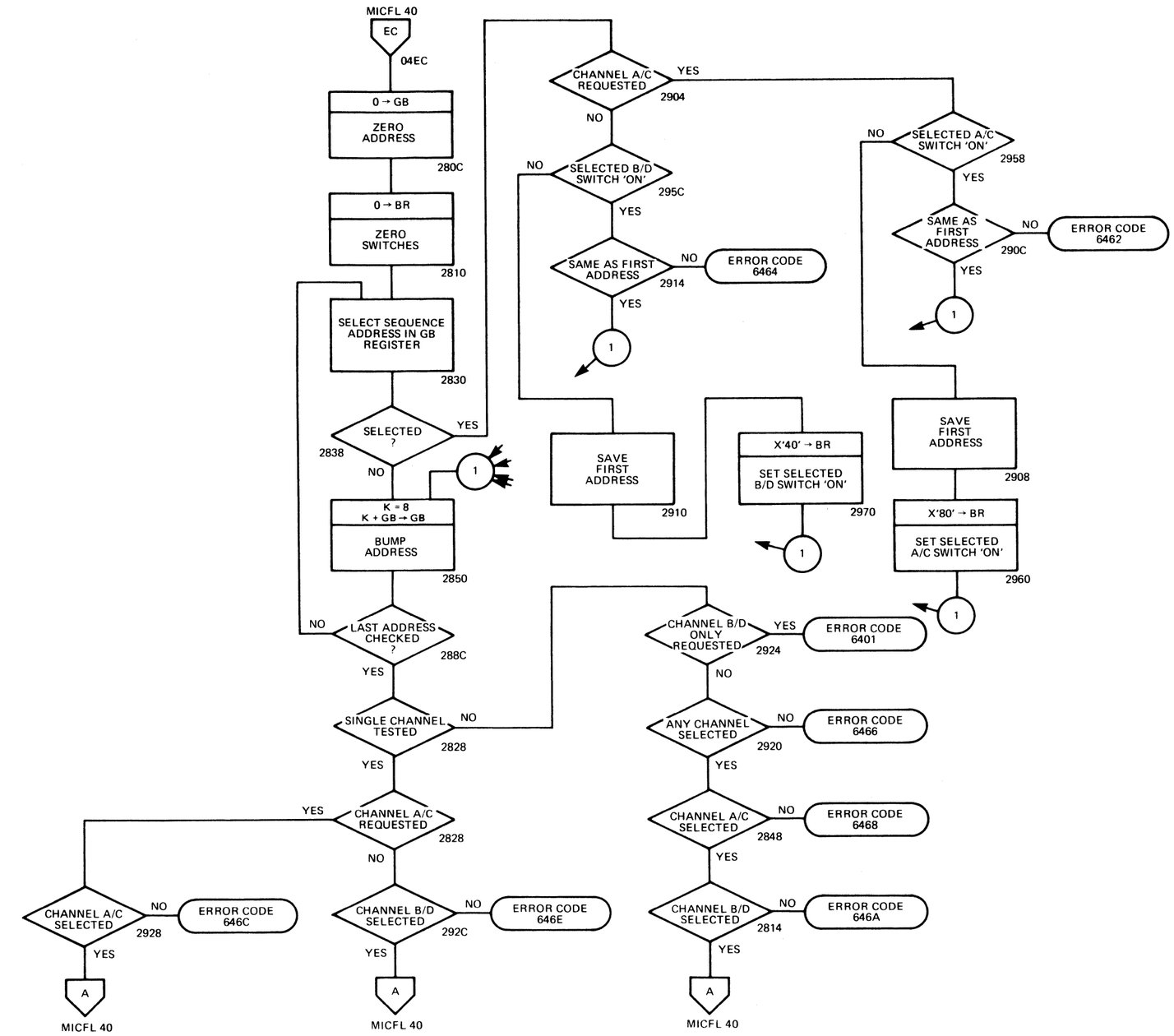
MLM0002_437408
MICFL_45_L
64D
JFL_11/09/72

MLM0002_437408
MICFL_45_R
64F
JFL_11/22/72

ROUTINE 64 (Part 3 of 3)

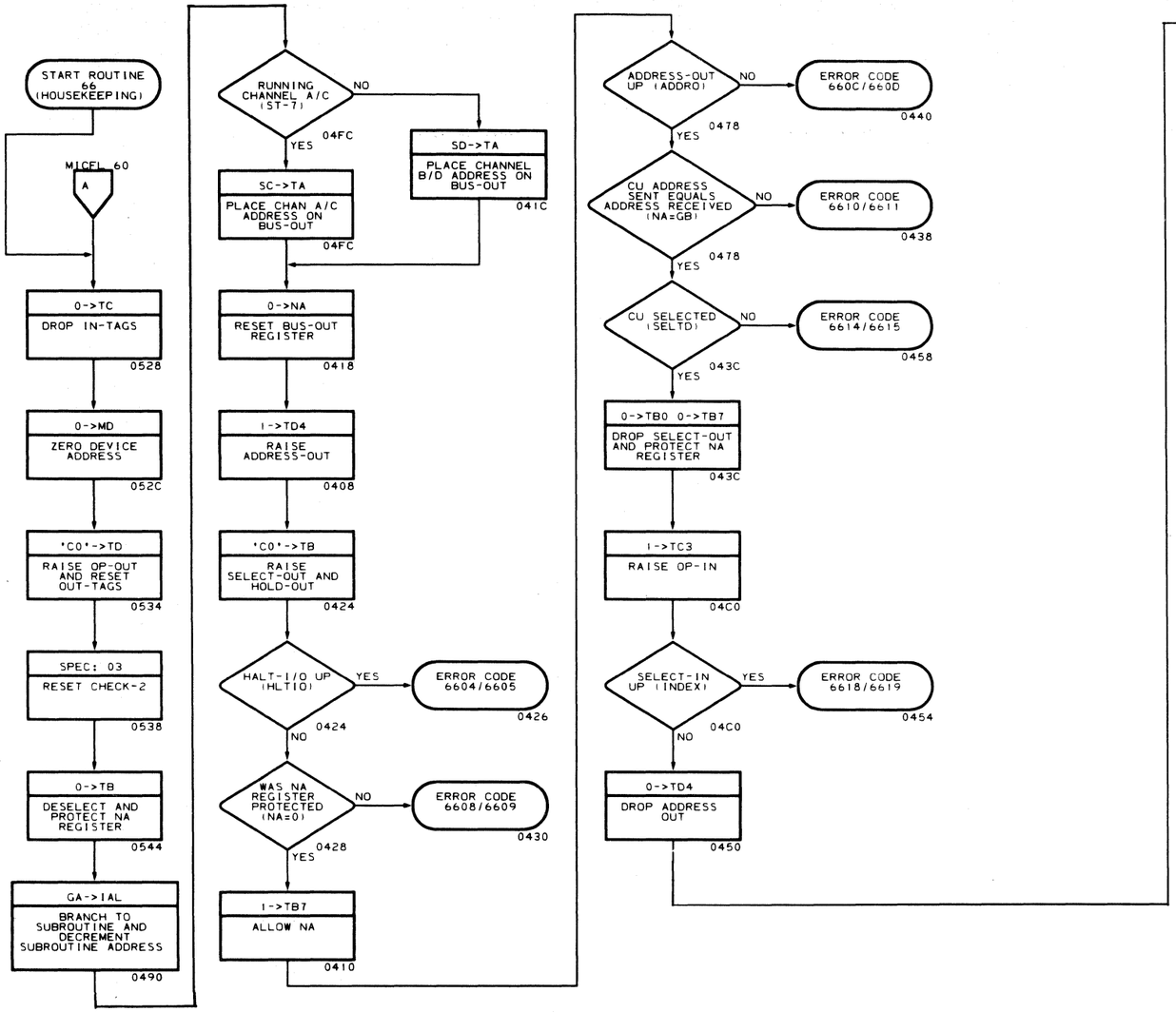
MICFL 50

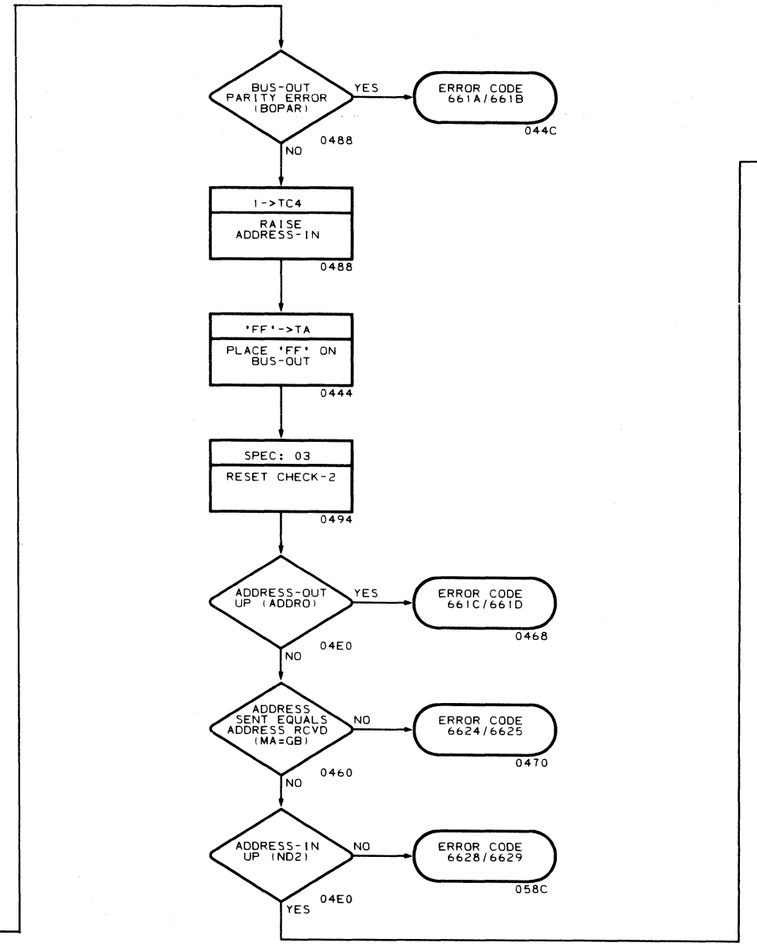


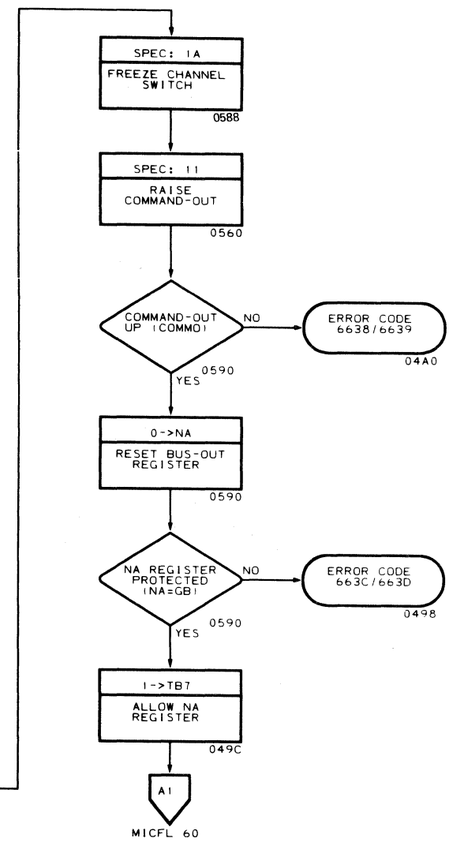


ROUTINE 66 (Part 1 of 2)

MICFL 55



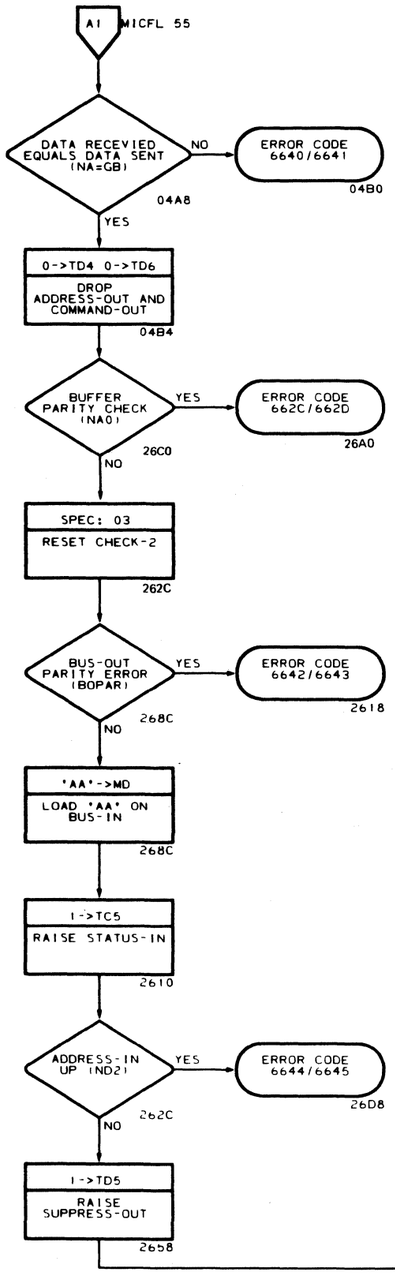


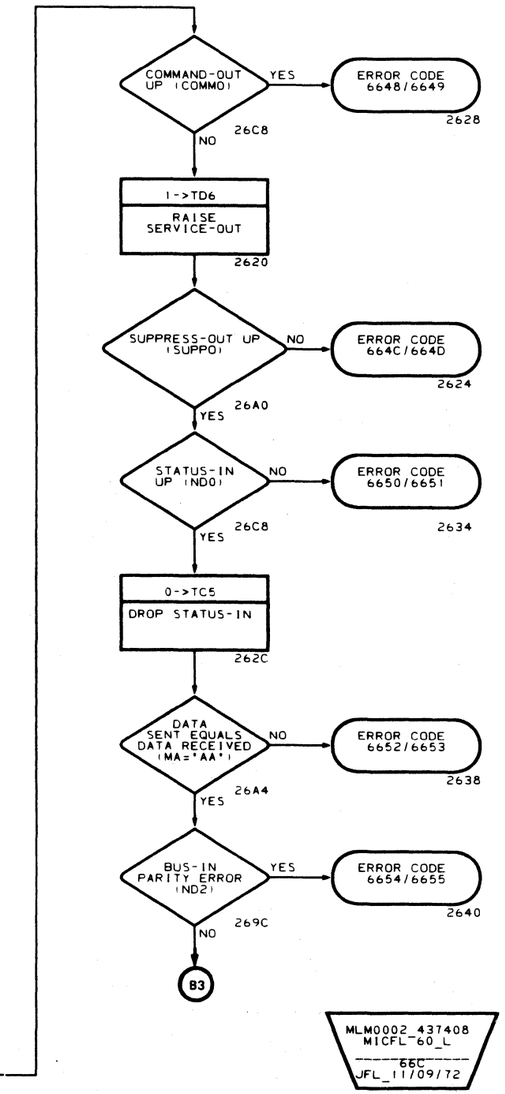


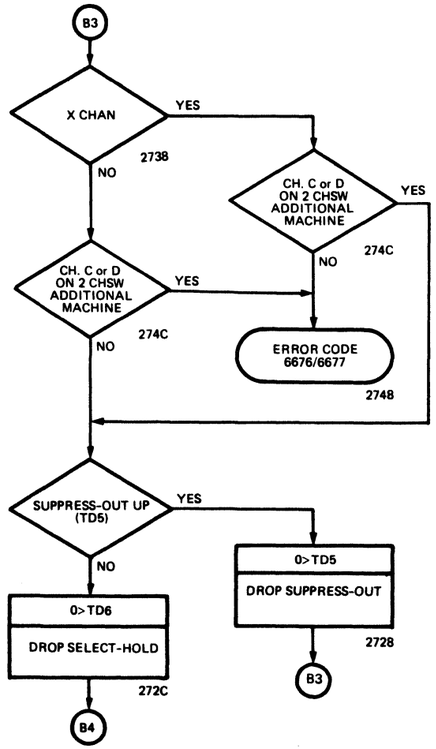
MLM0002_437408
MICFL-55_L
65A
JFL_11/27/72

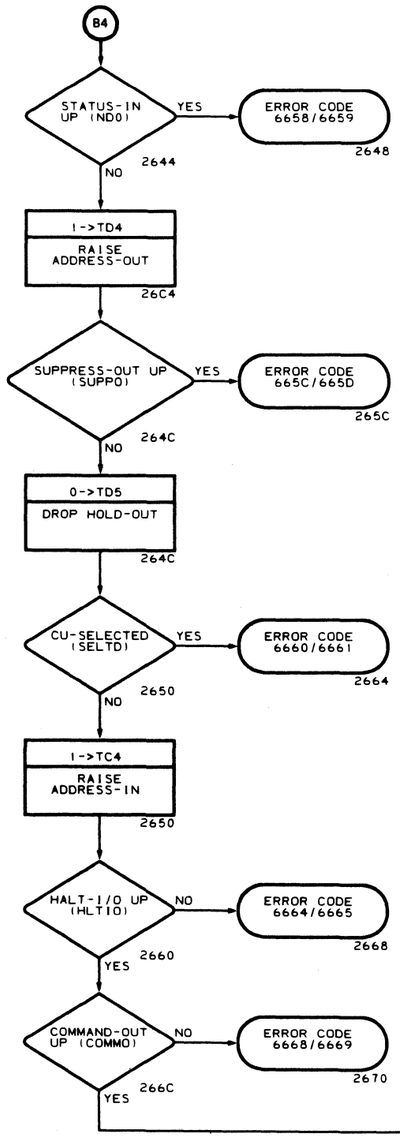
MLM0002_437408
MICFL-55_R
66B
JFL_11/09/72

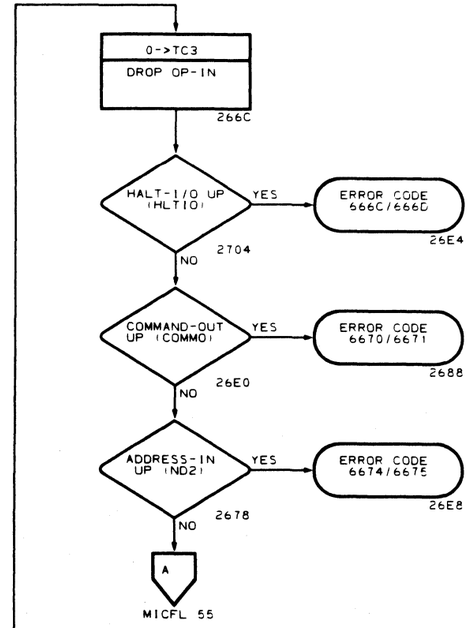
ROUTINE 66 (Part 2 of 2)





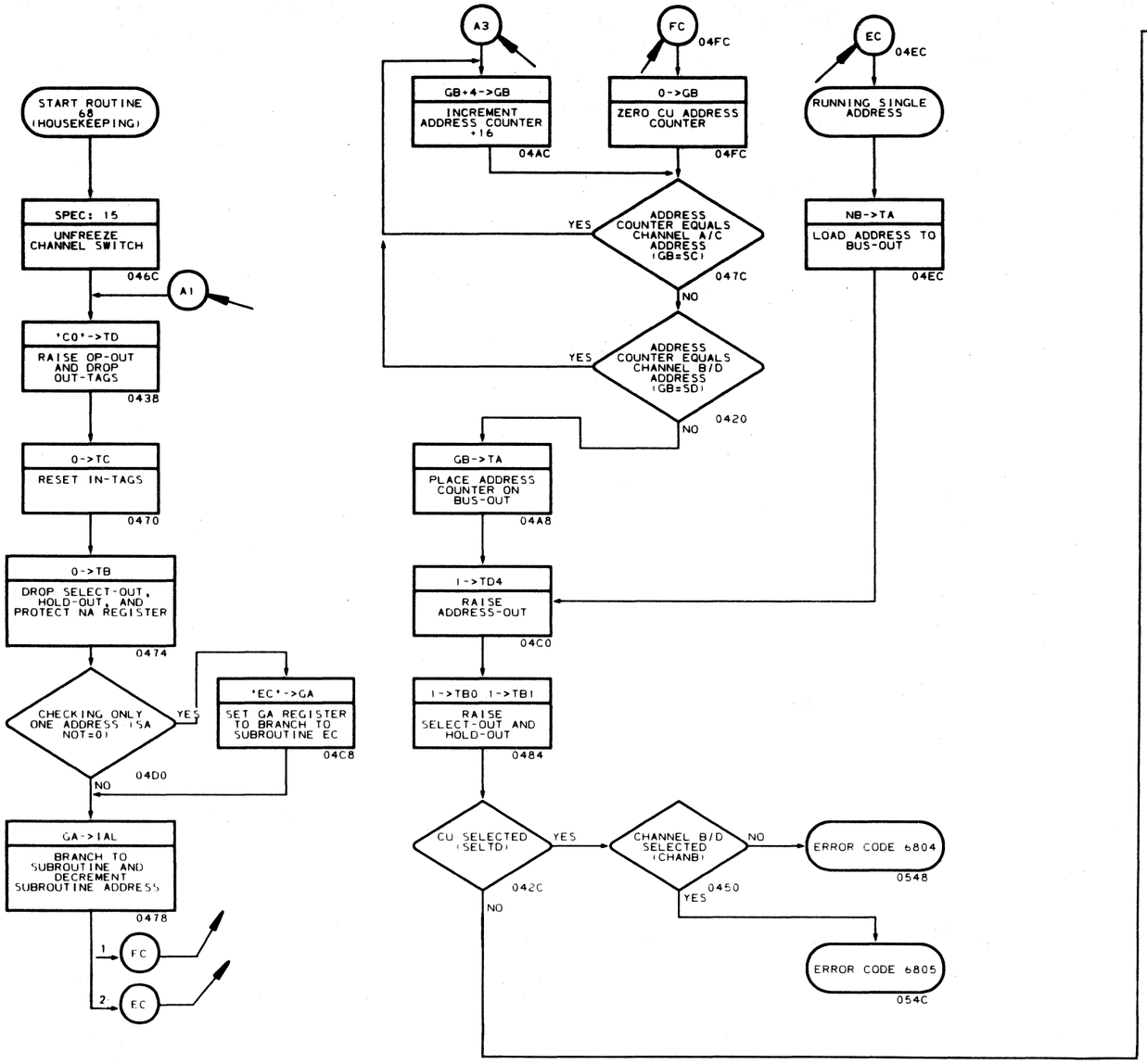


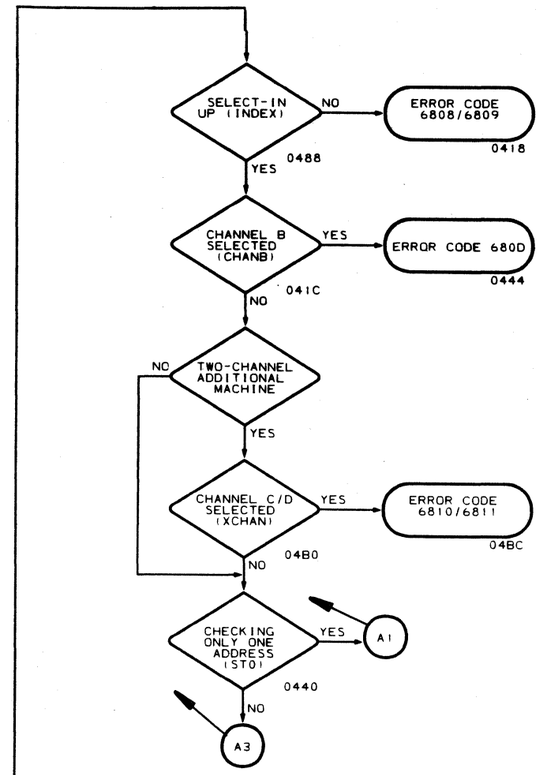




MLM0002_437408
MICFL-60_L
66C
JFL_11/09/72

MLM0002_437408
MICFL-60_R
66D
JFL_11/27/72



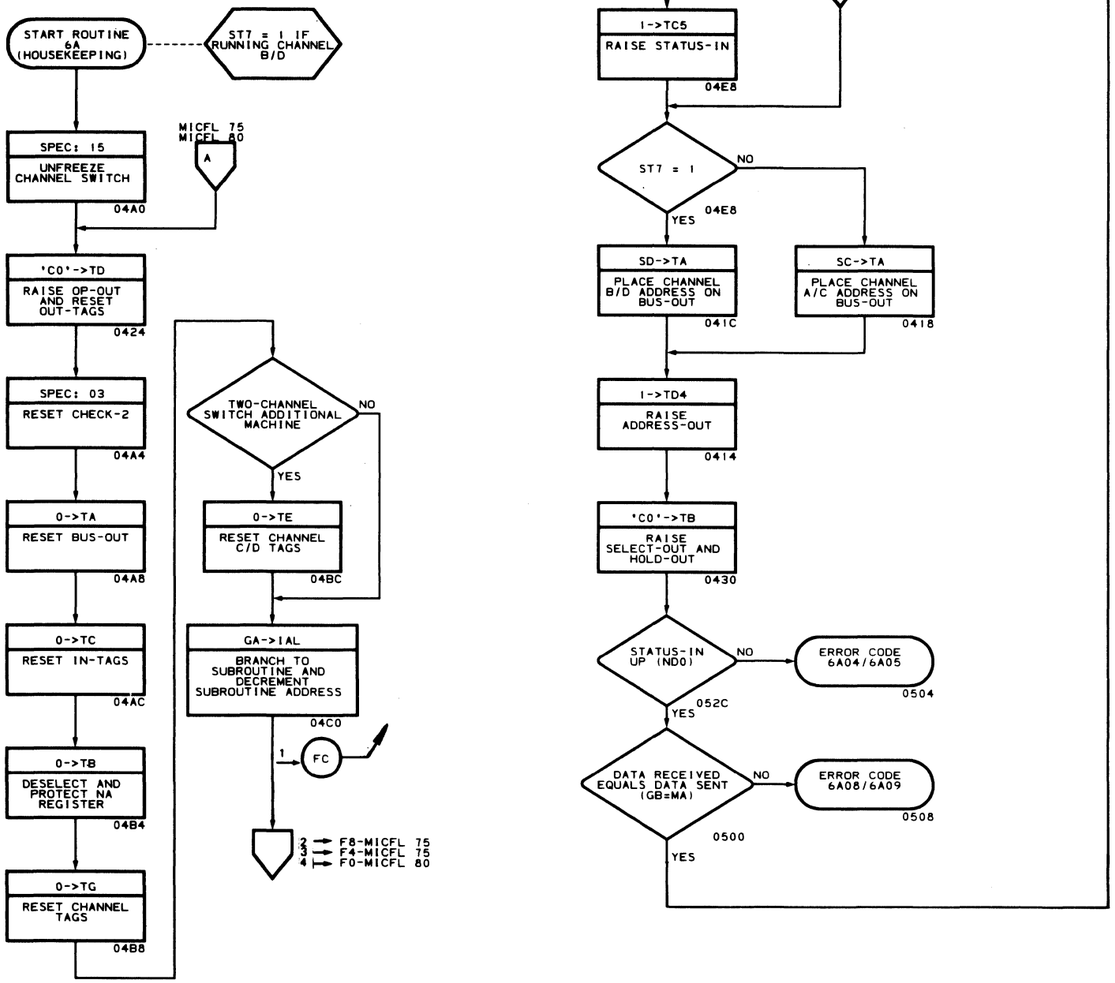


MLM0002_437408
MICFL-65_L
68A
JFL_11/27/72

MLM0002_437408
MICFL-65_R
68B
JFL_11/27/72

ROUTINE 6A (Part 1 of 3)

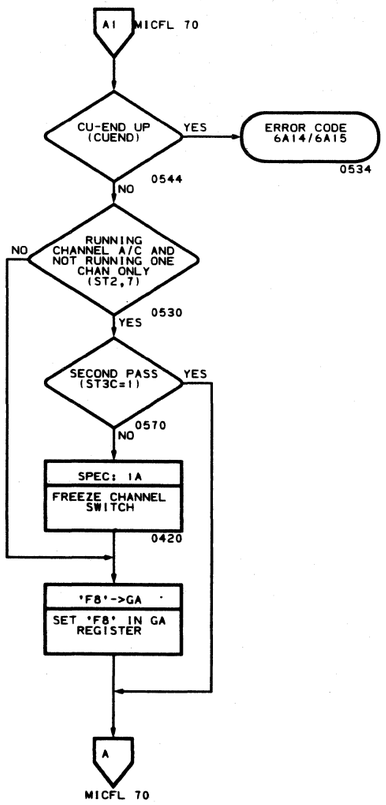
MICFL 70

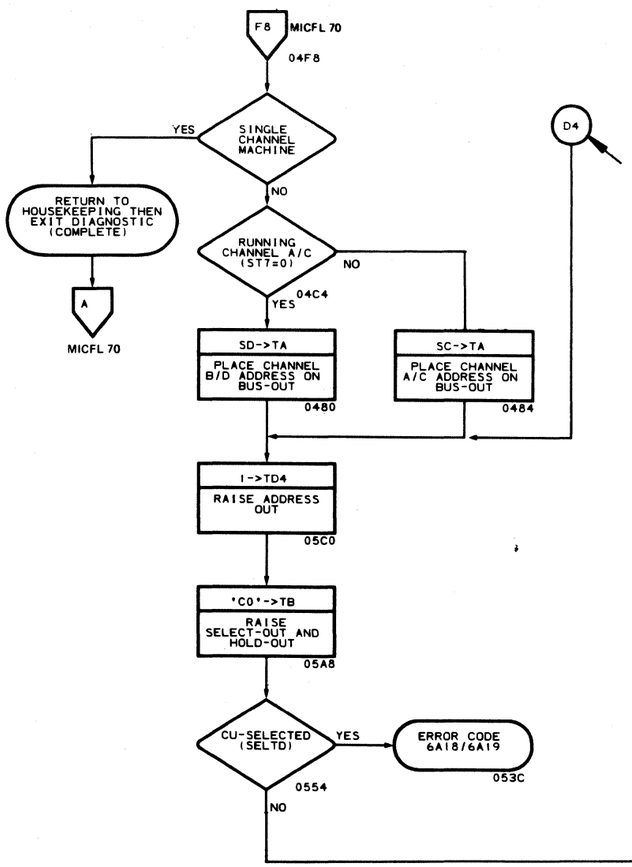


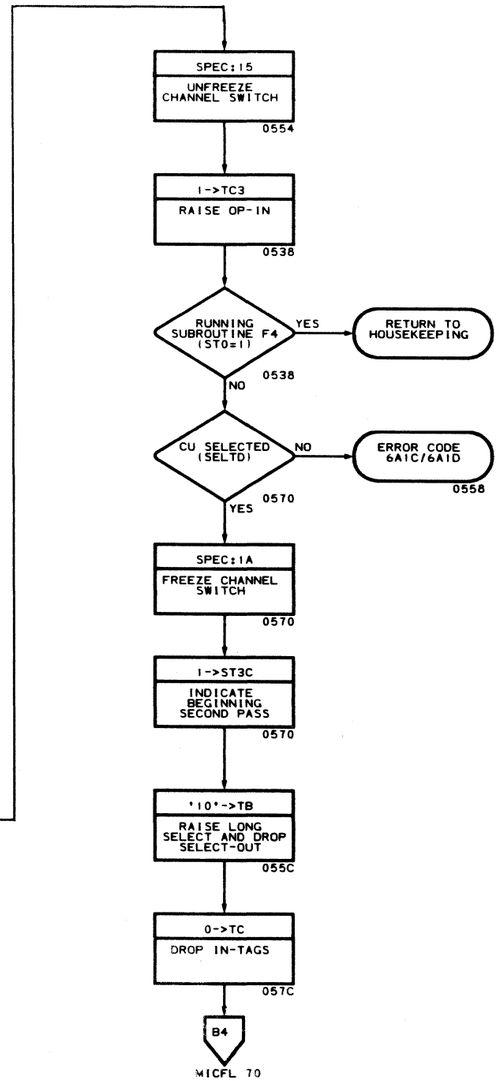
MLM0002 437408
MICFL-70_L
6AA
JFL_11/27/72

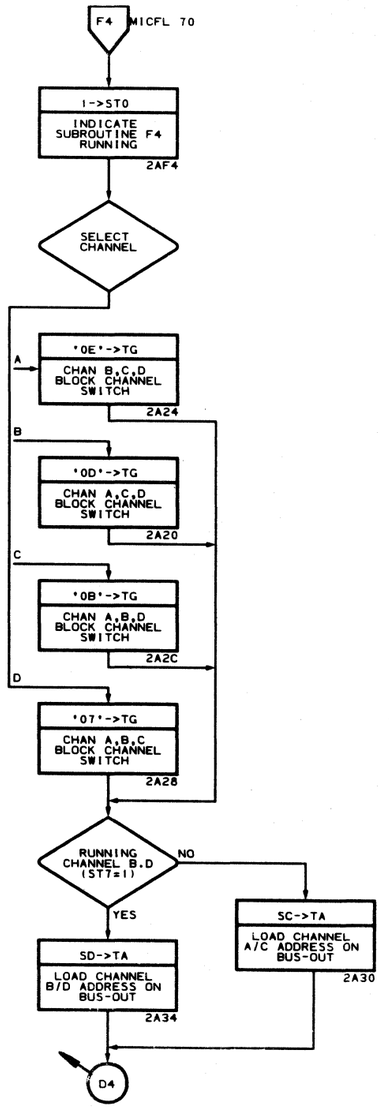
MLM0002 437408
MICFL-70_R
6AB
JFL_11/27/72

ROUTINE 6A (Part 1 of 3) MICFL 70







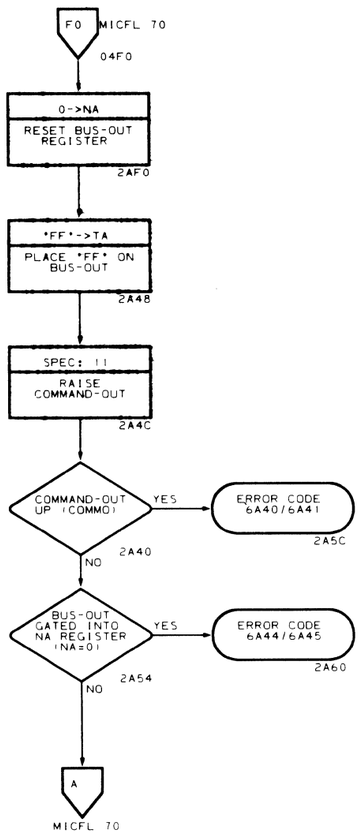


MLM0002_437408
MICFL-75_L
6AC
JFL_11/27/72

MLM0002_437408
MICFL-75_R
6AD
JFL_11/27/72

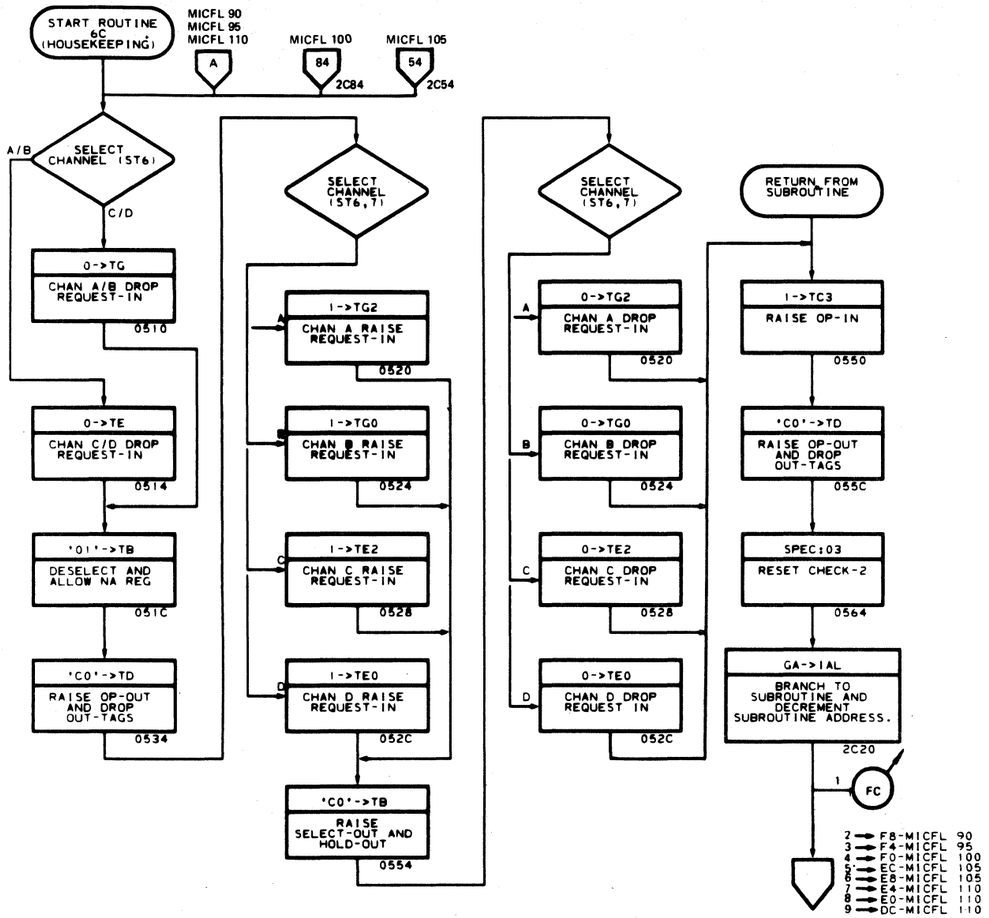
ROUTINE 6A (Part 3 of 3)

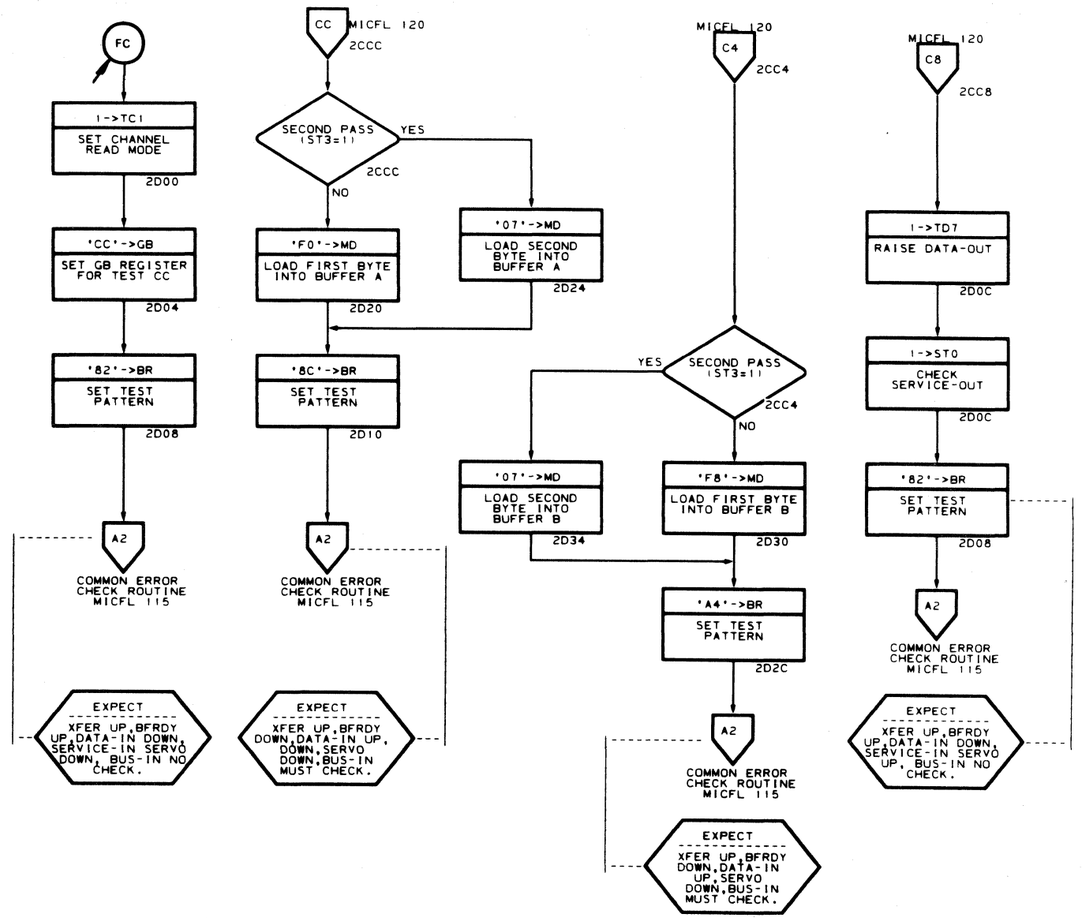
ROUTINE 6A (Part 3 of 3)



MLM0002_437408
MICFL-80_L
6AE
JFL_11/27/72

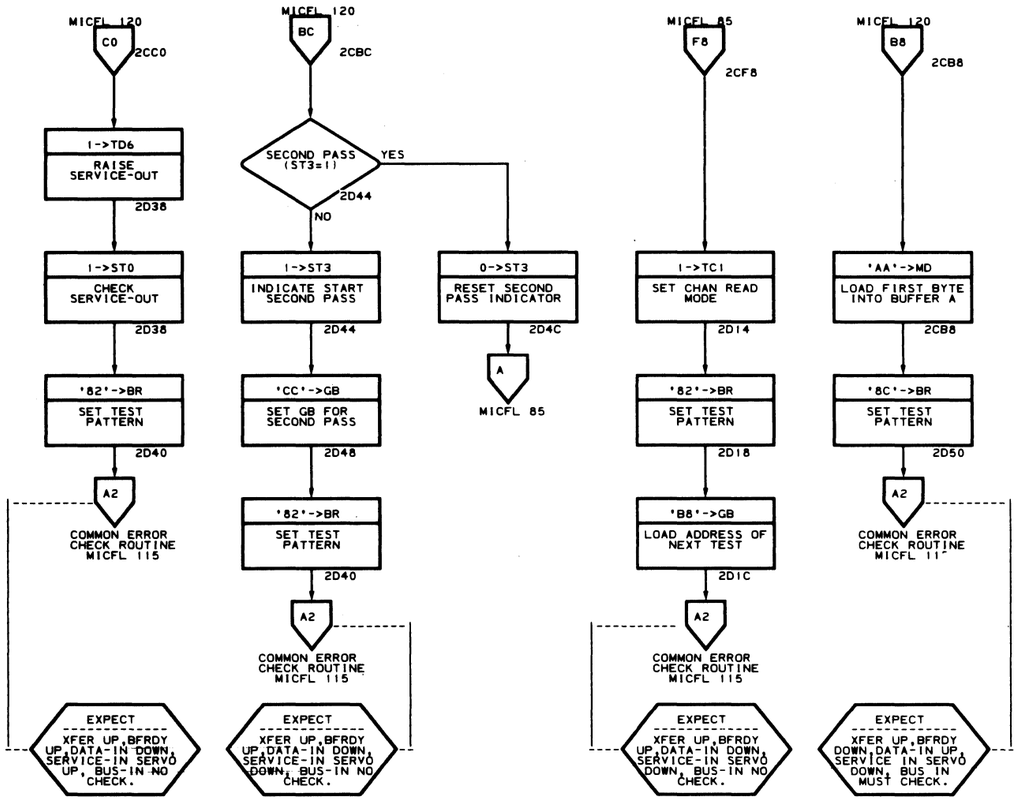
ROUTINE 6C (Part 1 of 8)



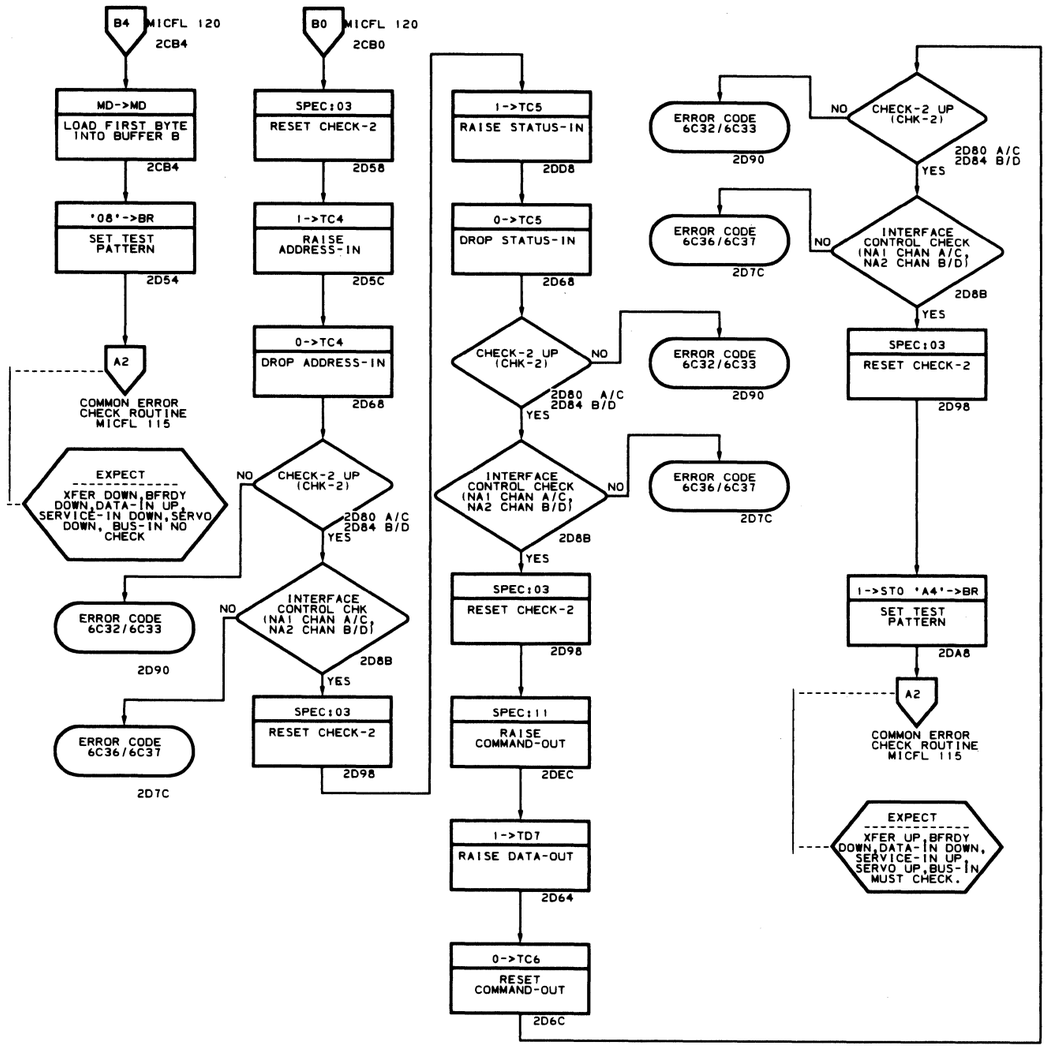


MLM0002_437408
MICFL-85_L
6CA
JFL_11/27/72

MLM0002_437408
MICFL-85_R
6CC
JFL_11/27/72

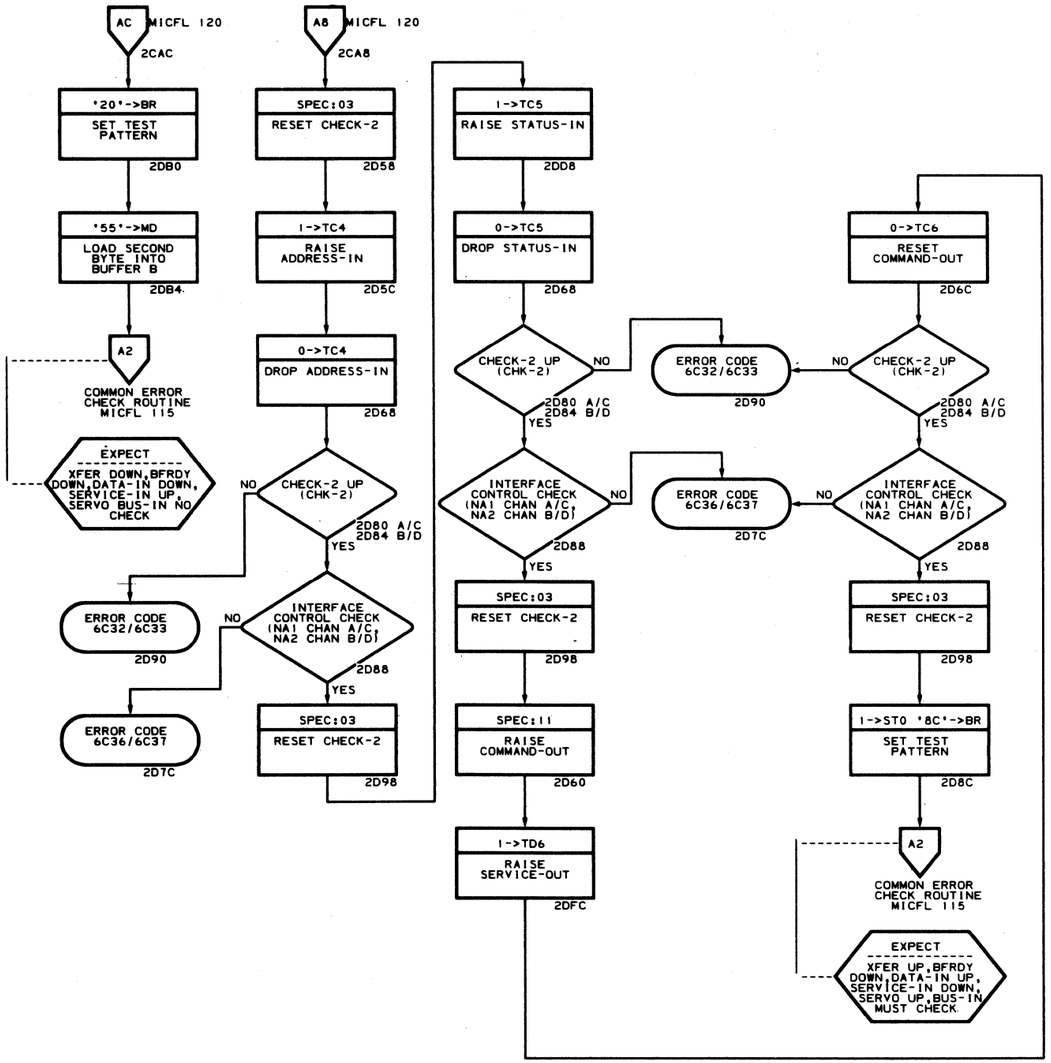


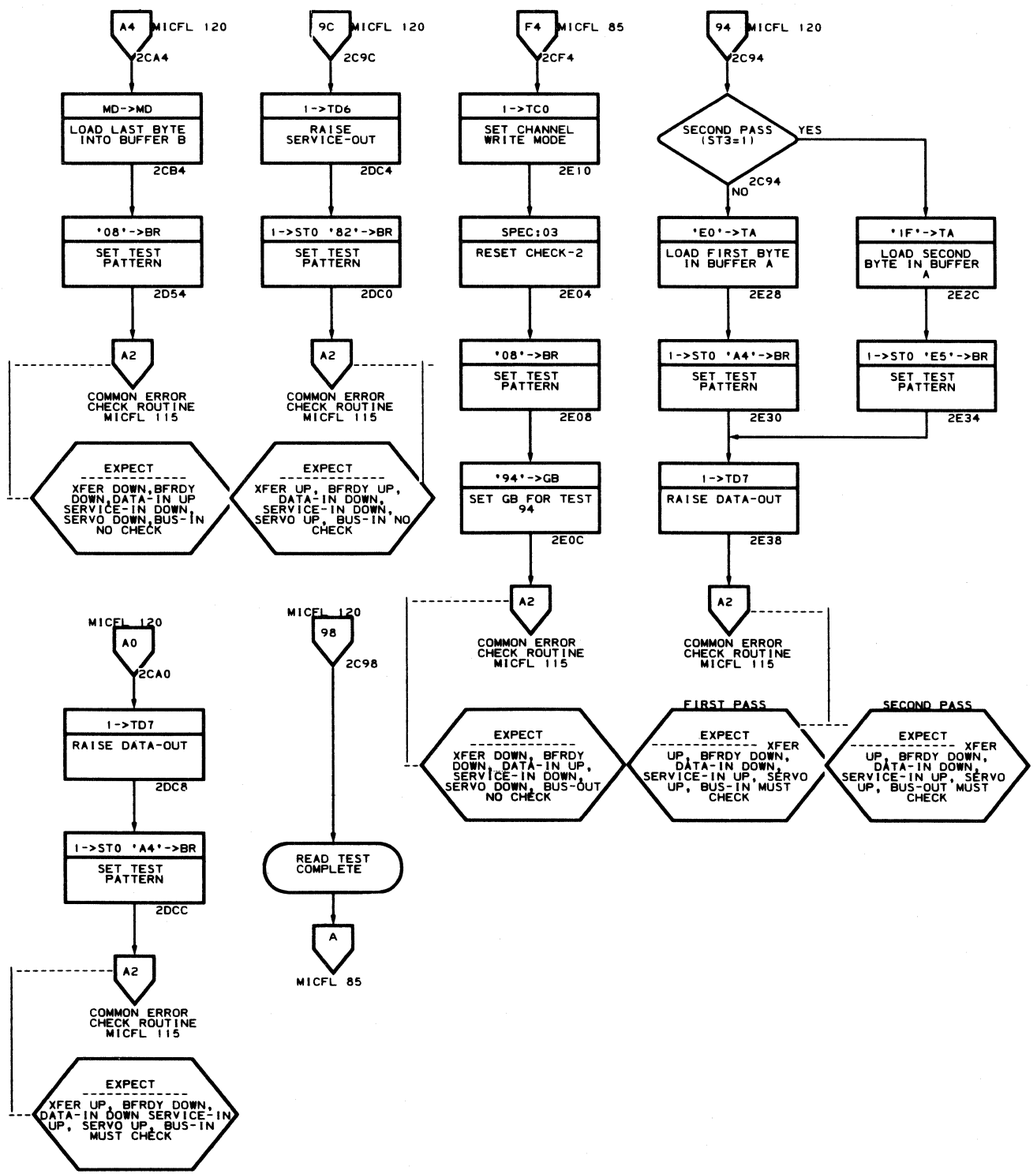
MLM0002_437408
MICFL-90_L
6CE
JFL_11/27/72



MLM0002_437408
MICFL-90_R
6CG
JFL_11/27/72

ROUTINE 6C (Part 3 of 8) MICFL 95





MLM0002_437408
MICFL-95_L
6CK
JFL_11/27/72

MLM0002_437408
MICFL-95_R
6CM
JFL_11/27/72

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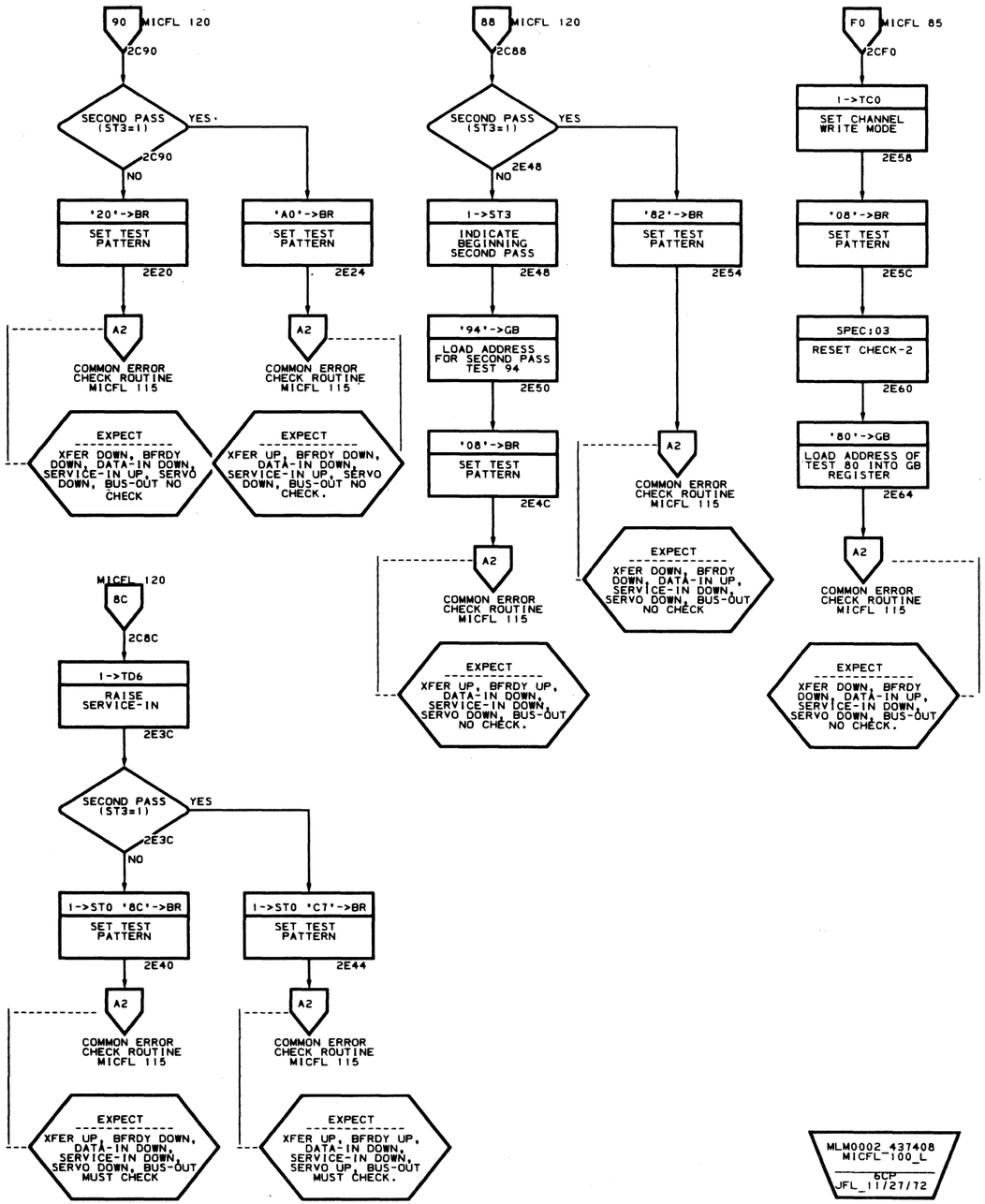
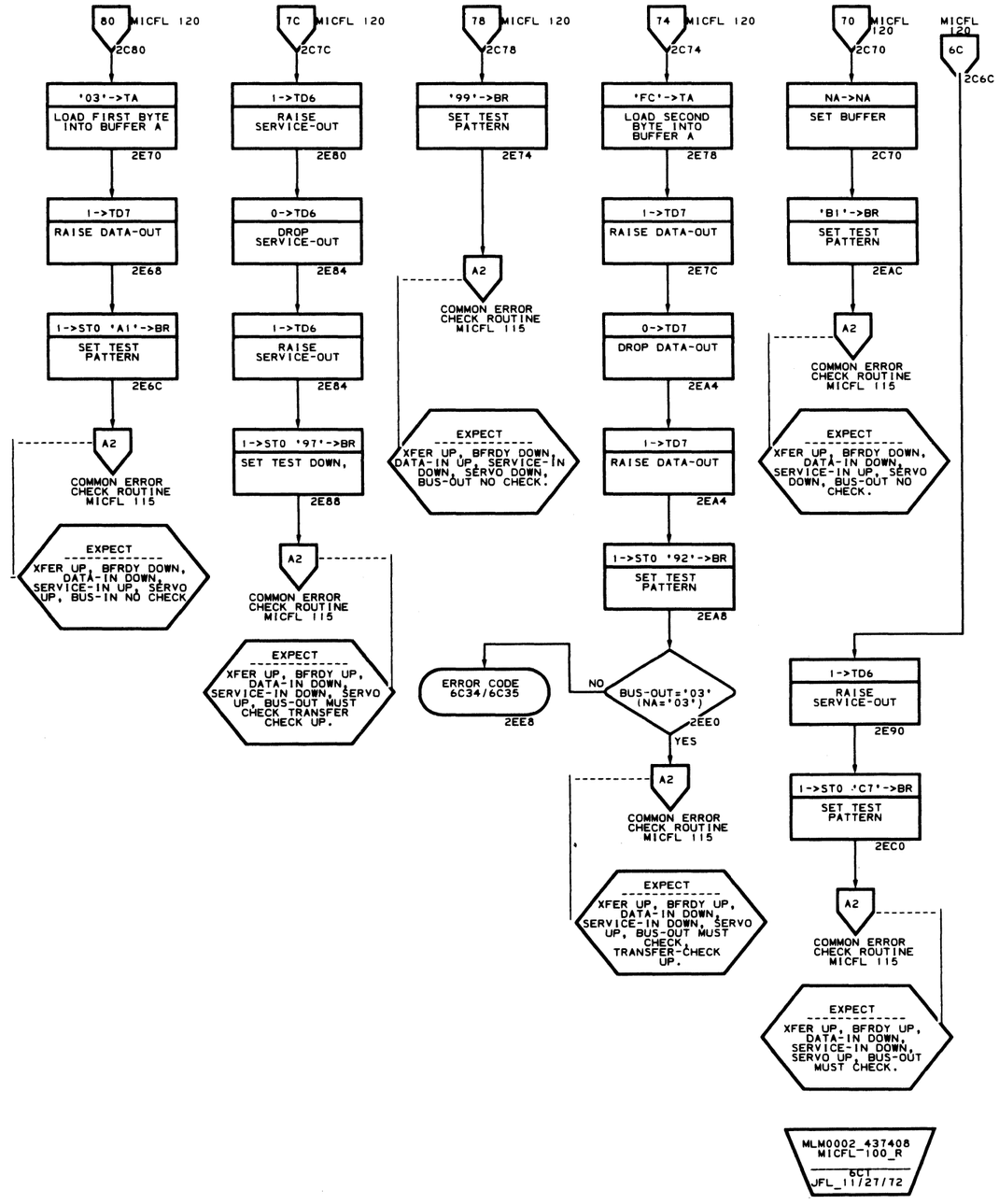
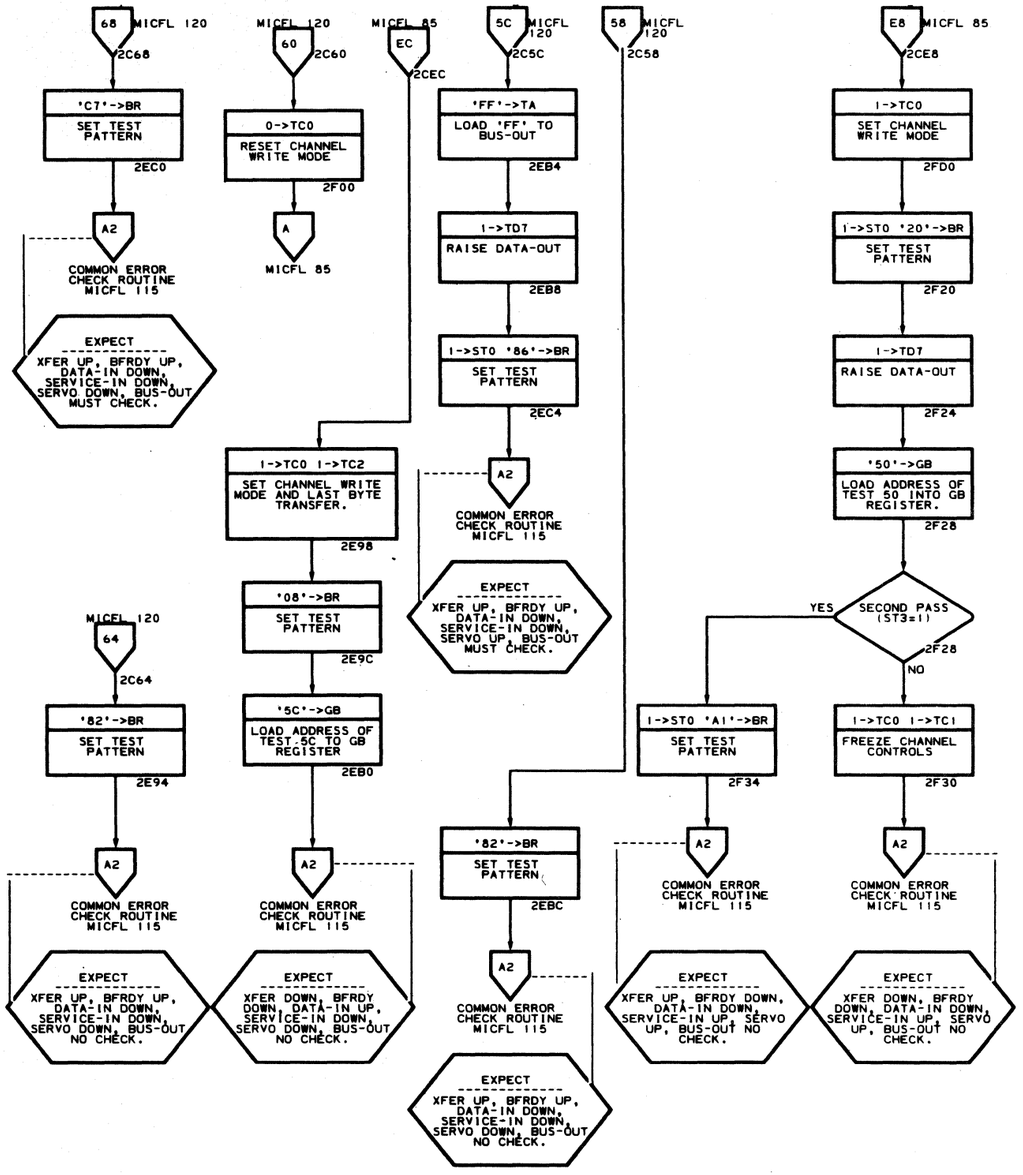
ROUTINE 6C (Part 4 of 8)

MICFL 100





MICFL 100



MLM0002_437408
MICFL-105L
6CW
JFL_11/27/72

3830-2

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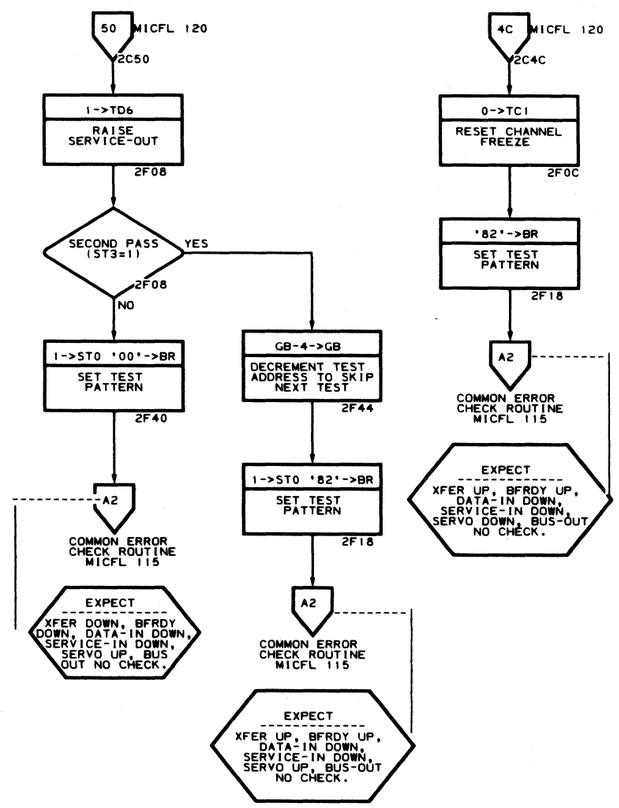
ROUTINE 6C (Part 5 of 8)

MICFL 105



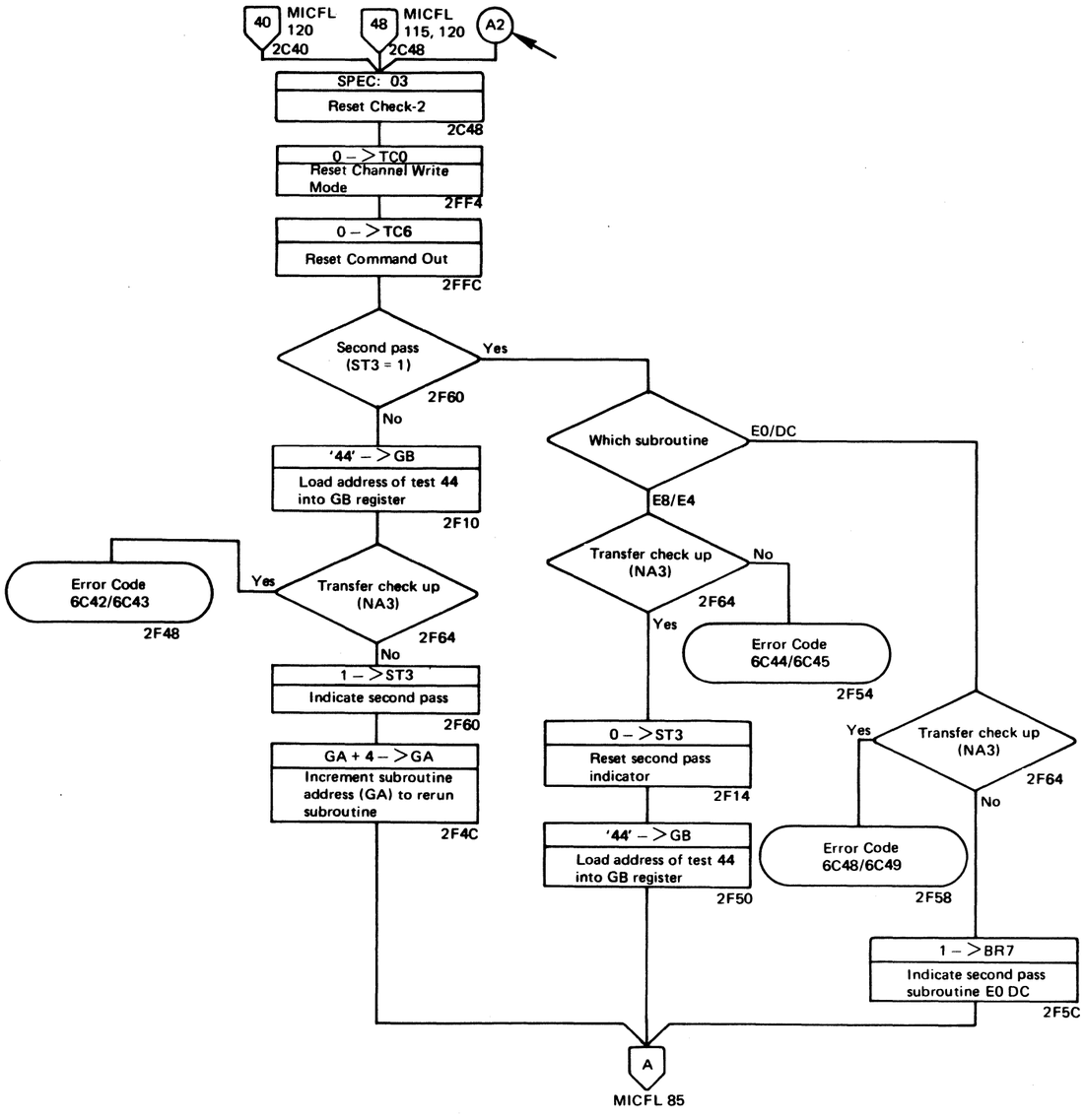
MLM0002_437408
MICFL-105_R
6CX
JFL_11/27/72

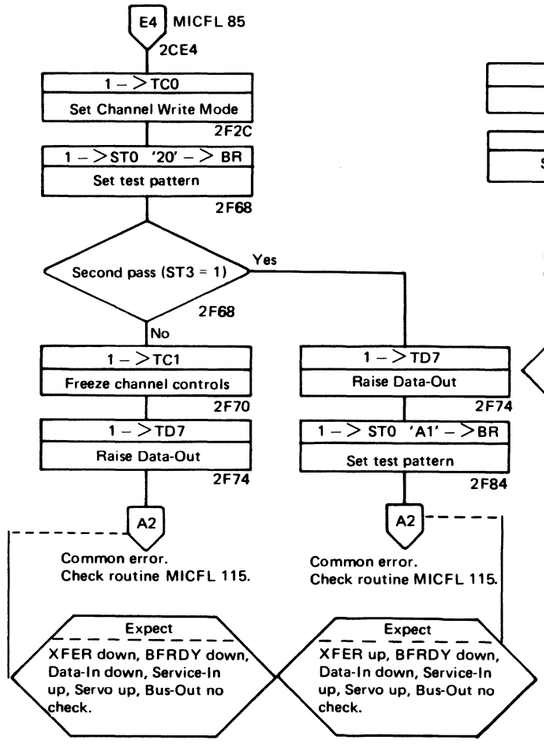
ROUTINE 6C (Part 5 of 8)

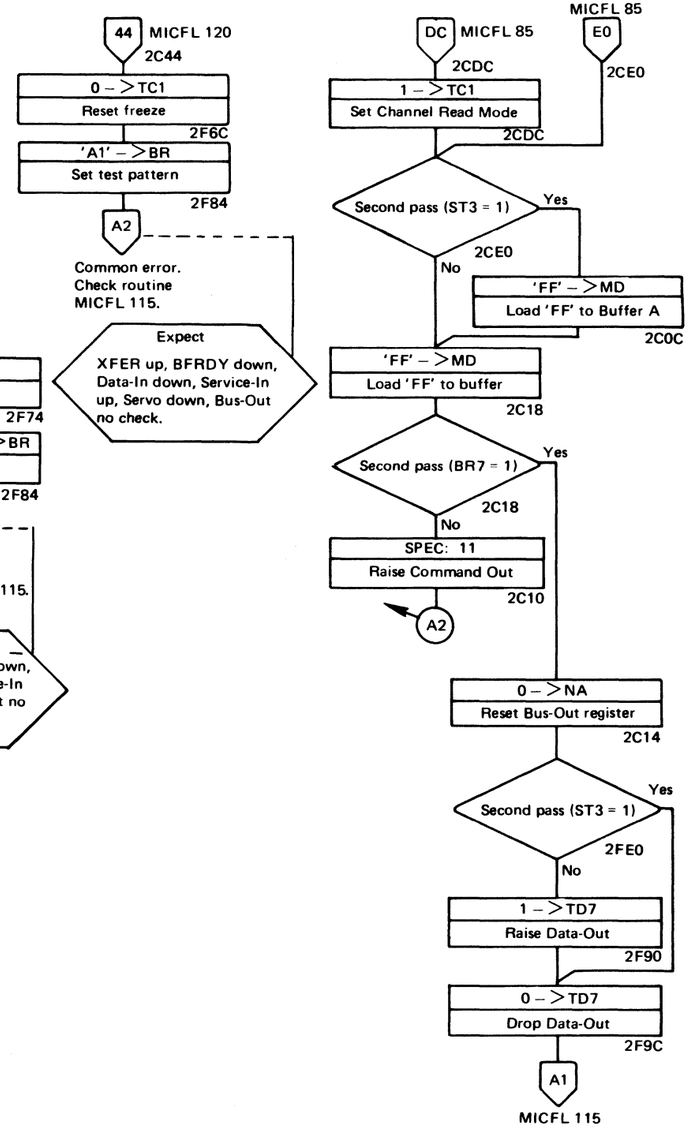
MICFL 105

ROUTINE 6C (Part 6 of 8)

MICFL 110

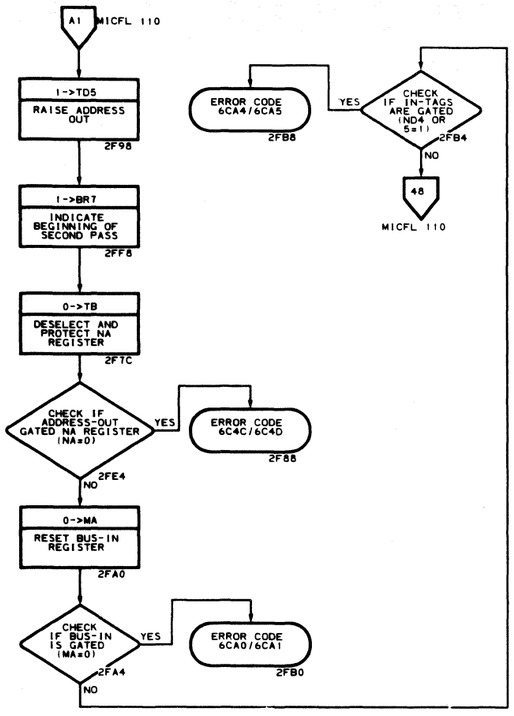


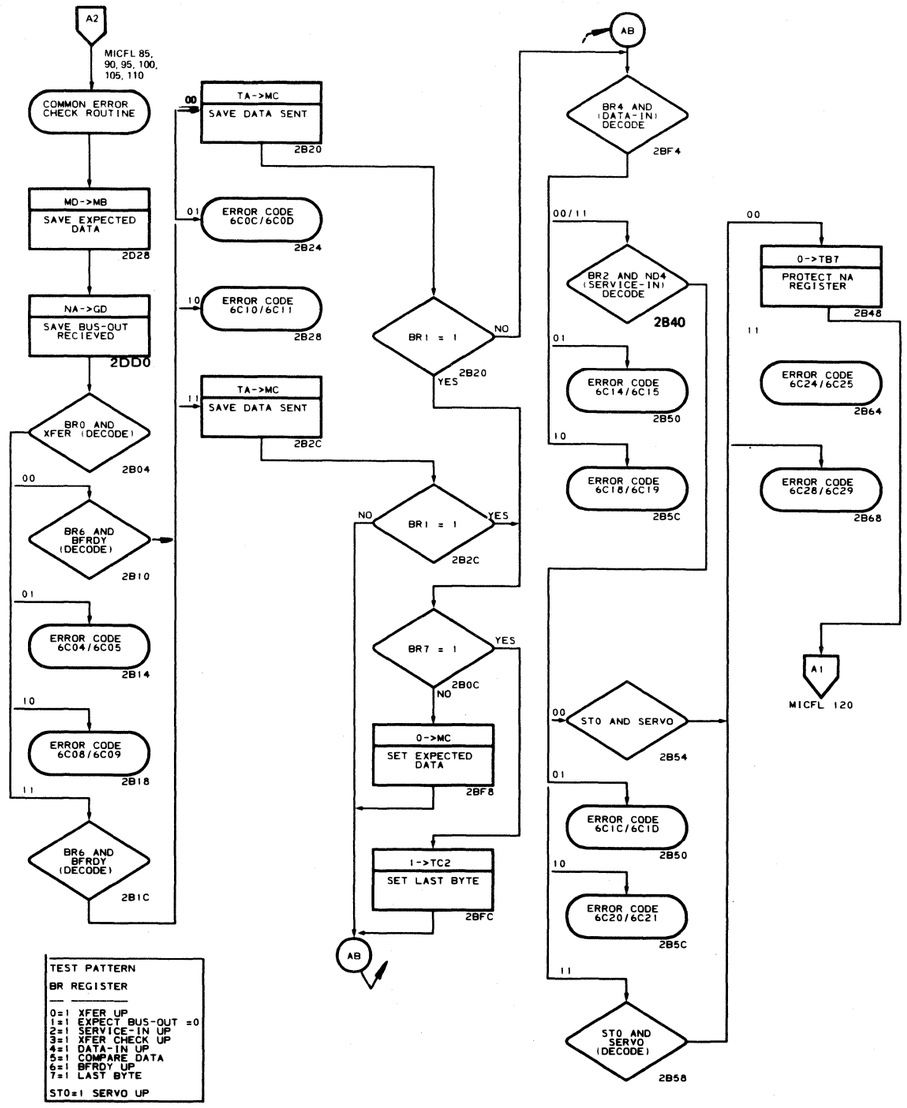




ROUTINE 6C (Part 7 of 8)

MICFL 115





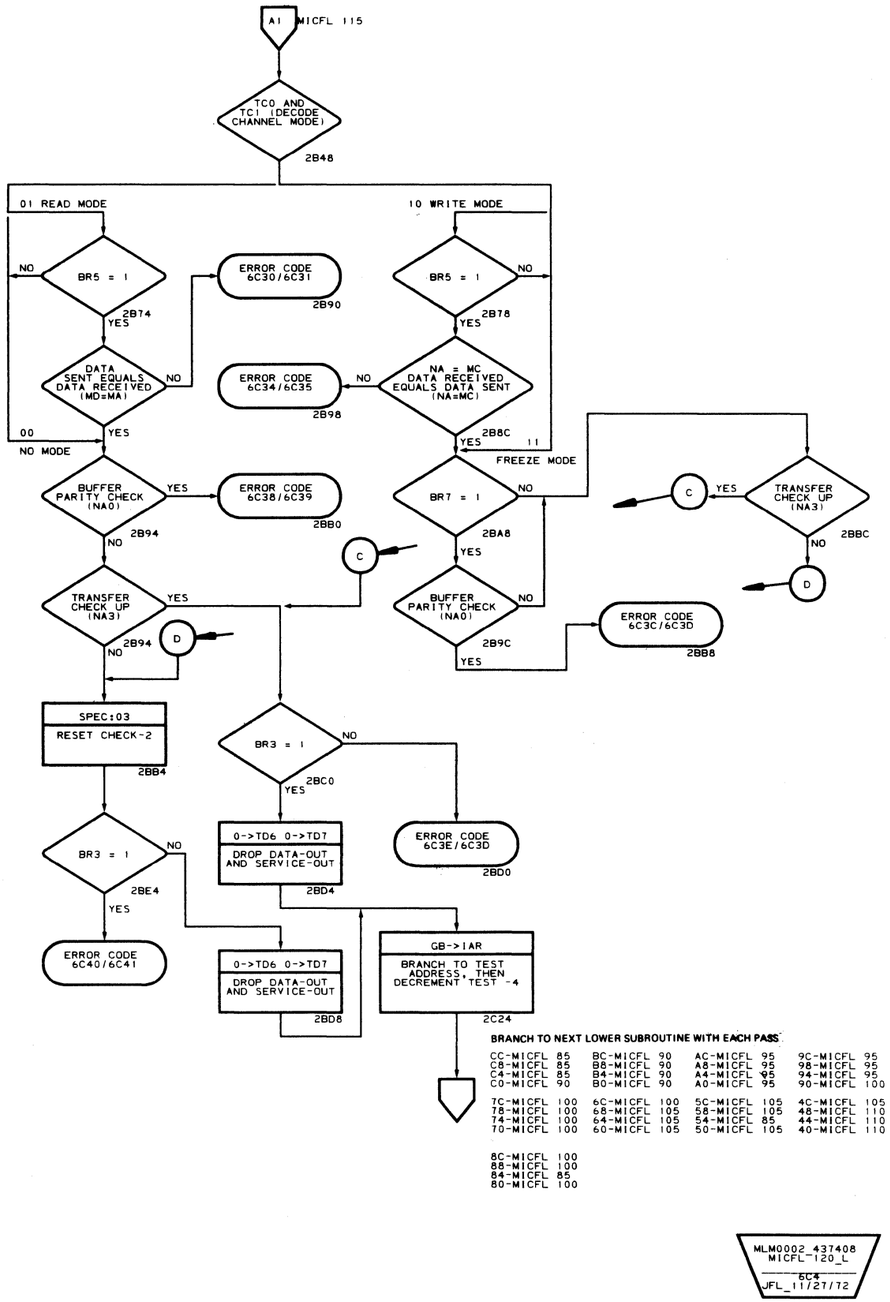
TEST PATTERN BR REGISTER
0=1 XFER UP
1=1 EXPECT BUS-OUT =0
2=1 SERVICE-IN UP
3=1 XFER CHECK UP
4=1 DATA-IN UP
5=1 COMPARE DATA
6=1 BFRDY UP
7=1 LAST BYTE
ST0=1 SERVO UP

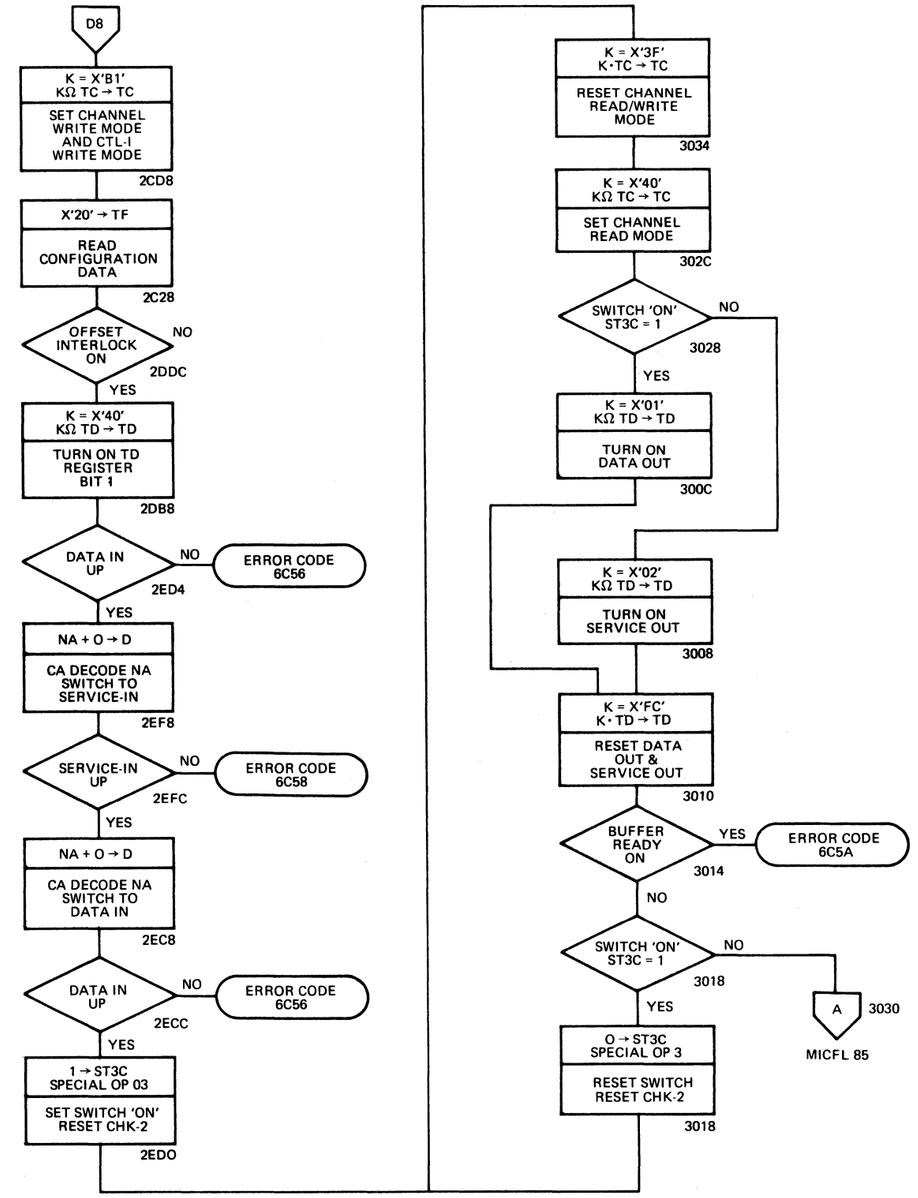
MLM0002_437408
MICFL_115_L
6C2
JFL_11/27/72

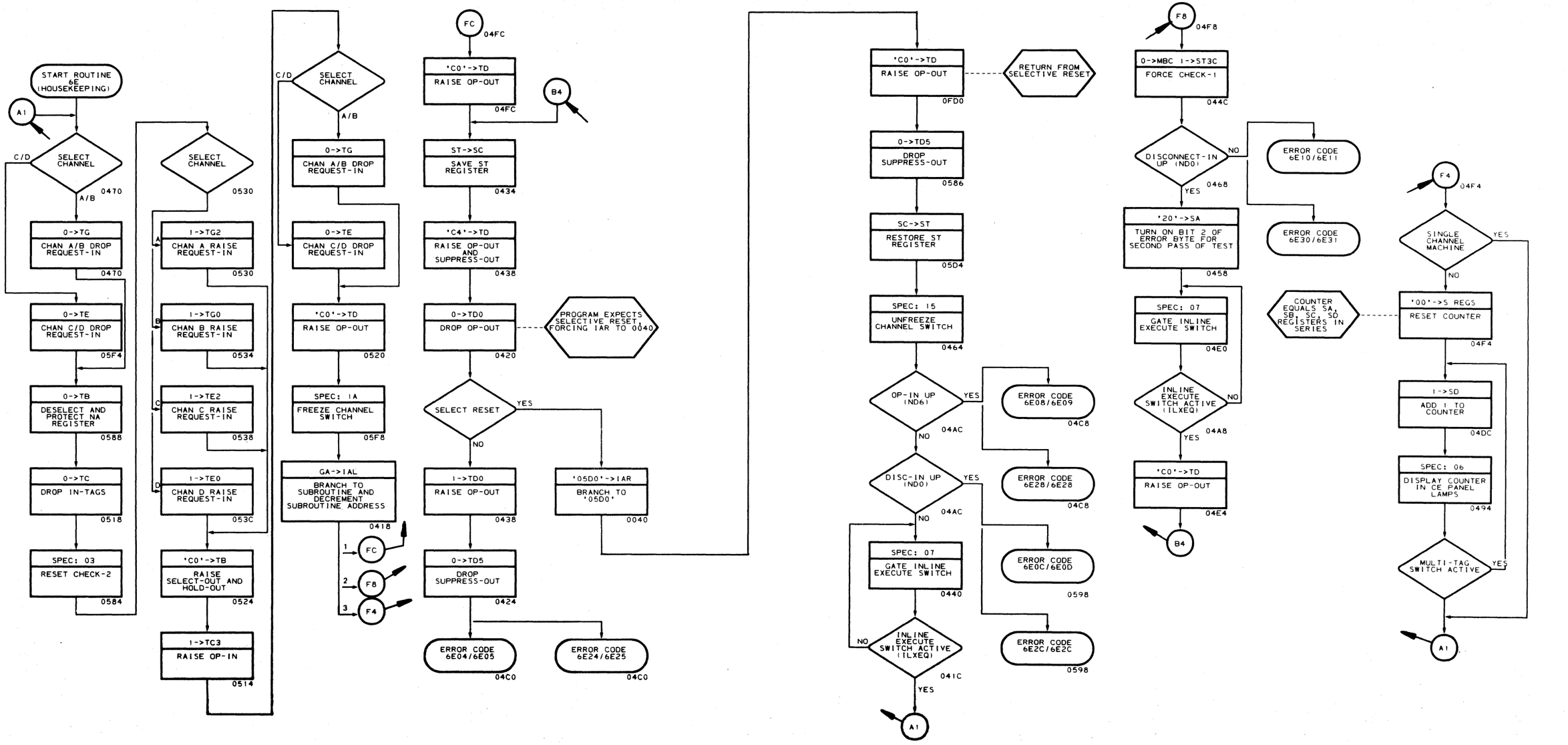
MLM0002_437408
MICFL_115_R
6C3
JFL_11/27/72

ROUTINE 6C (Part 8 of 8)

MICFL 120

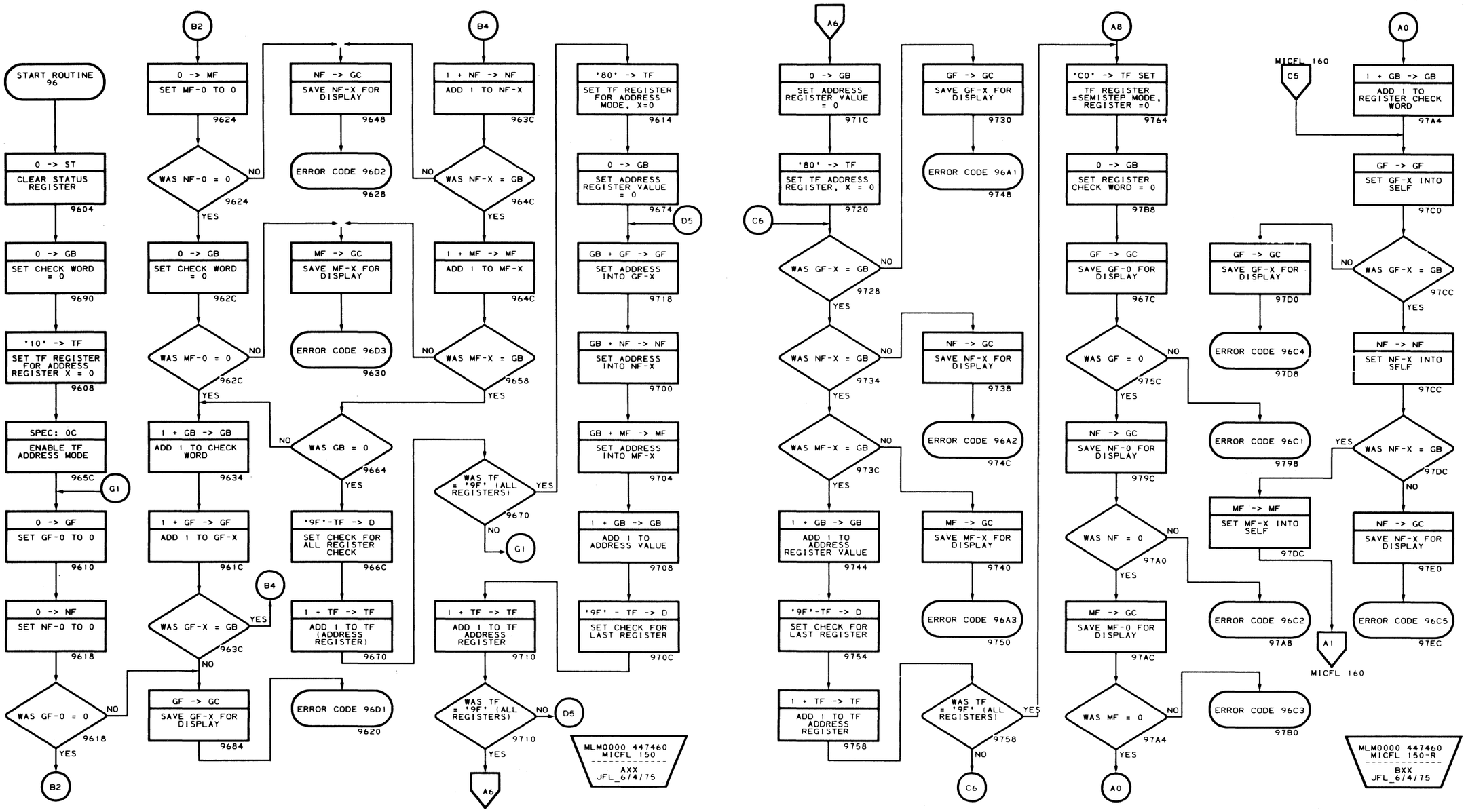


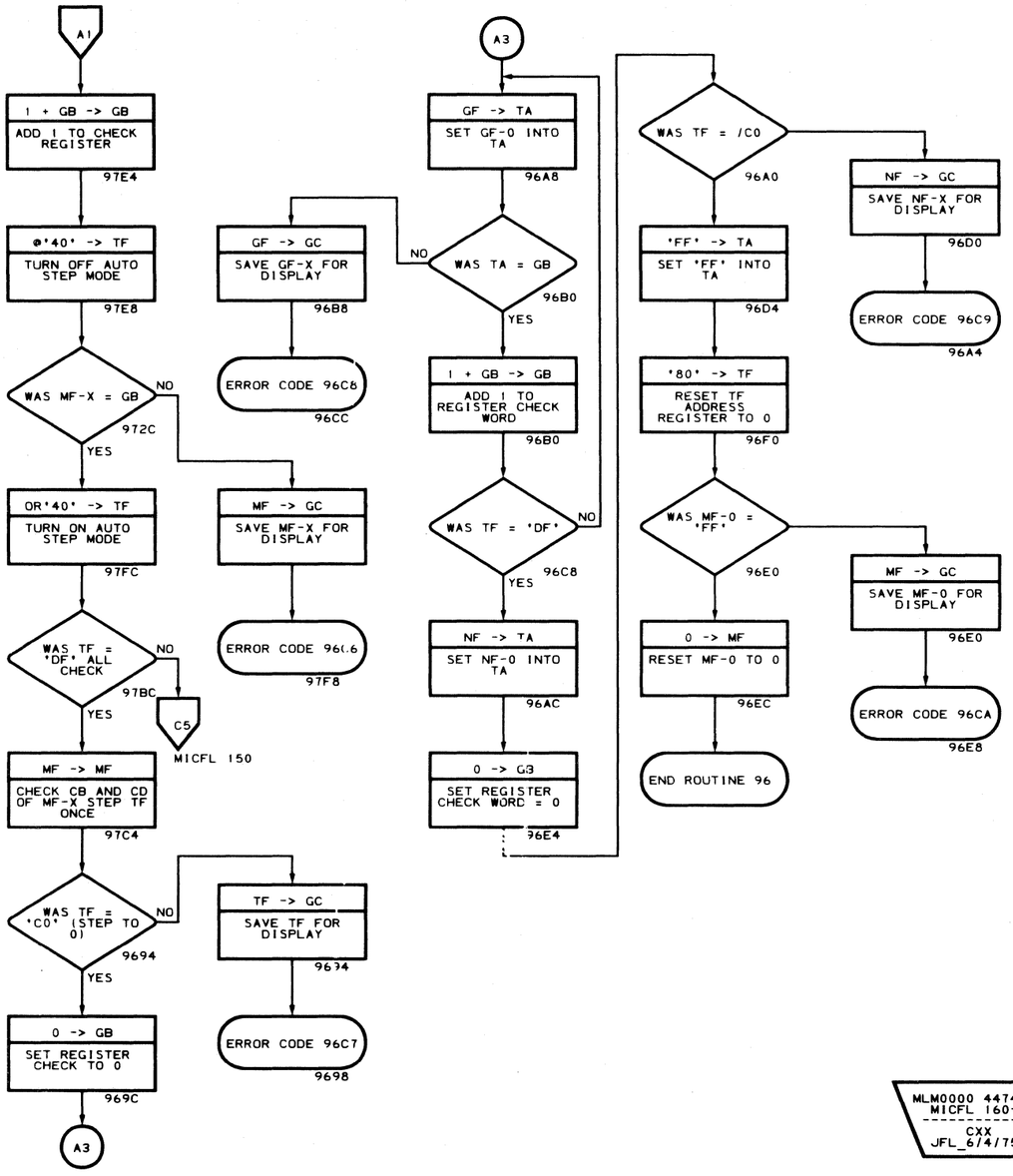




MLM0002_437408
MICFL_125_L
6EA
JFL_11/27/72

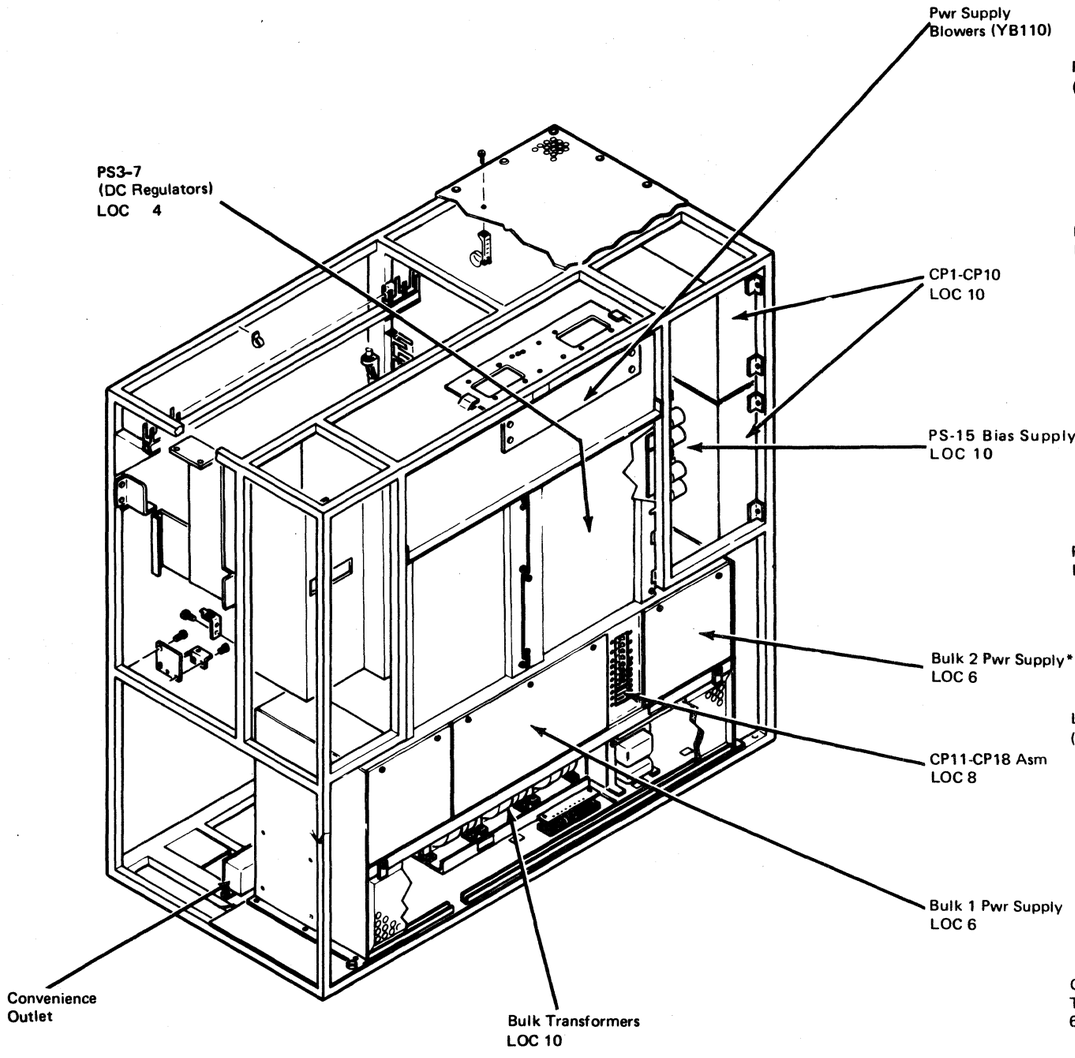
MLM0002_437408
MICFL_125_R
6EB
JFL_11/27/72



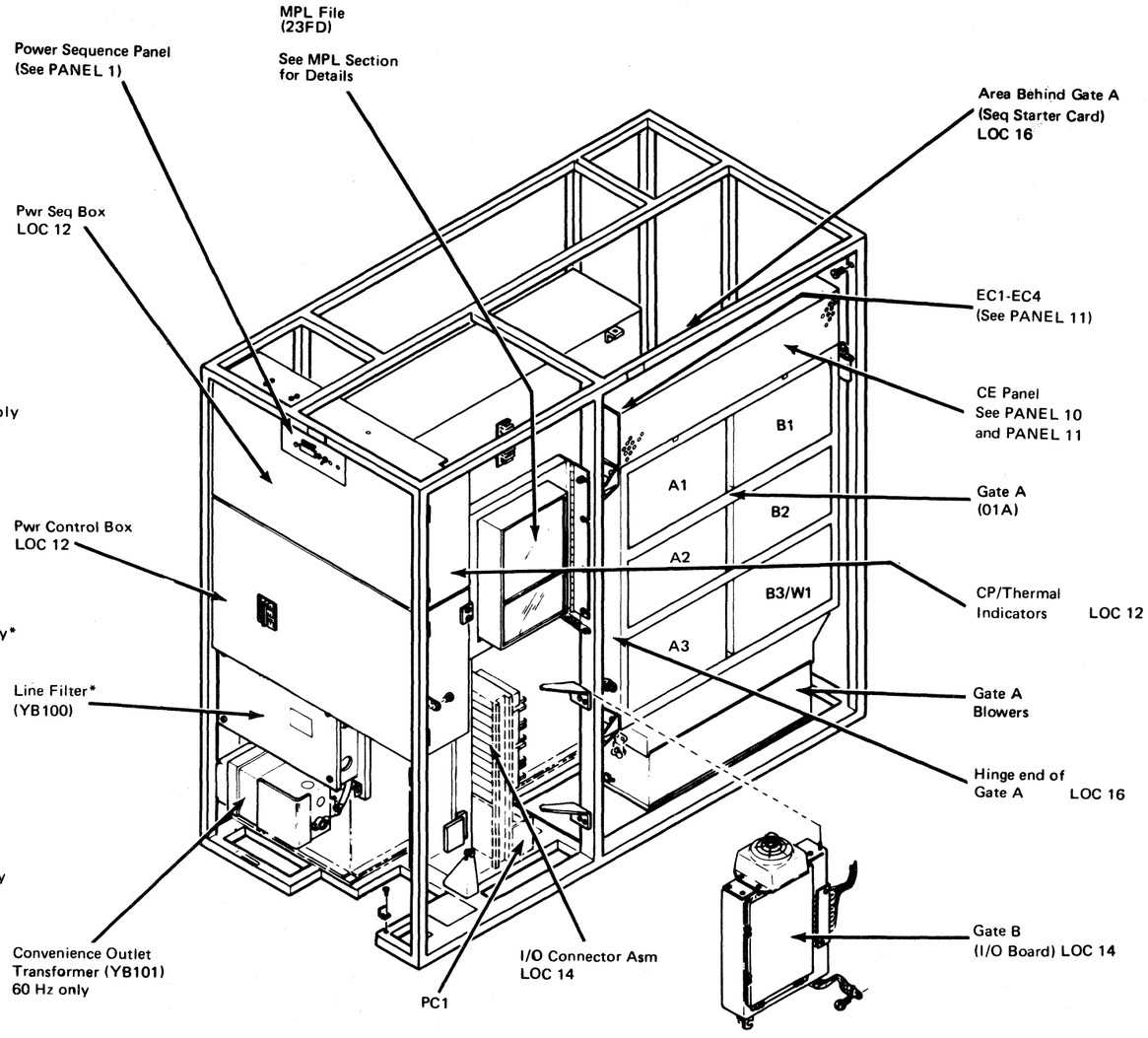


MLM0000 447460
MICFL 160-L
CXX
JFL_6/4/75

COMPONENT INDEX

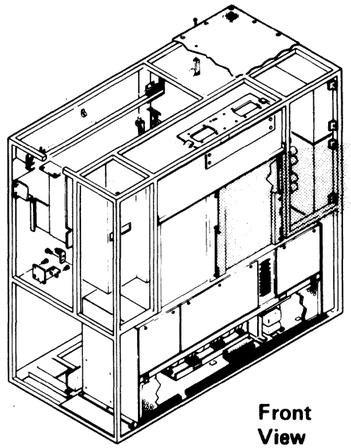


Front View

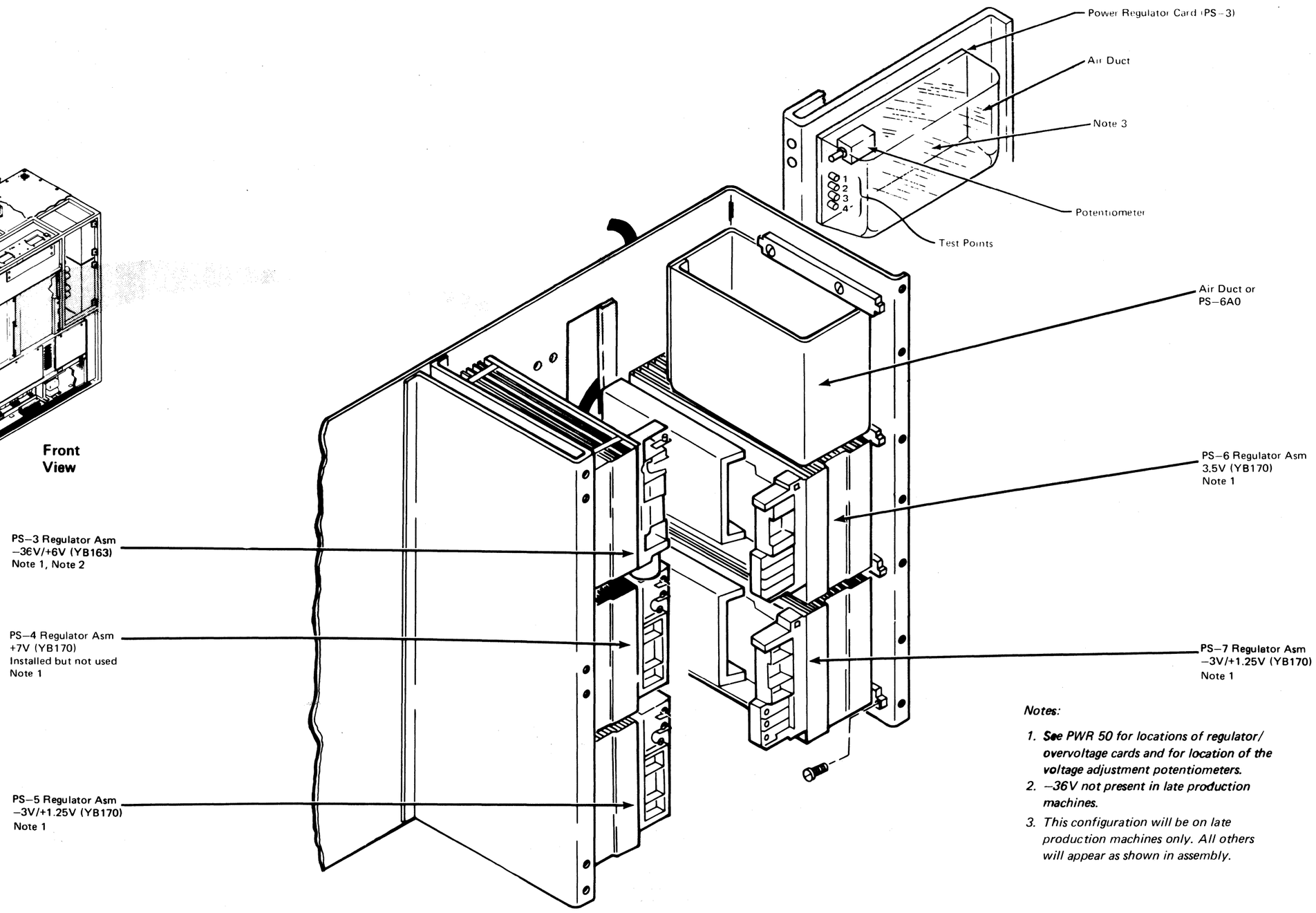


Rear View

* Not used in late production machines

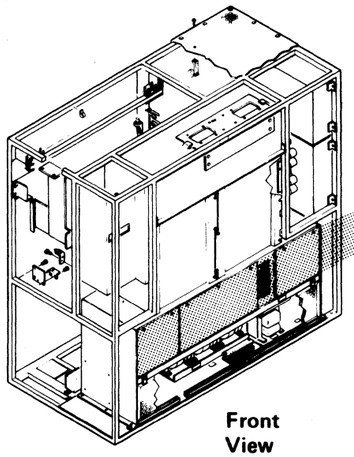


Front View



Notes:

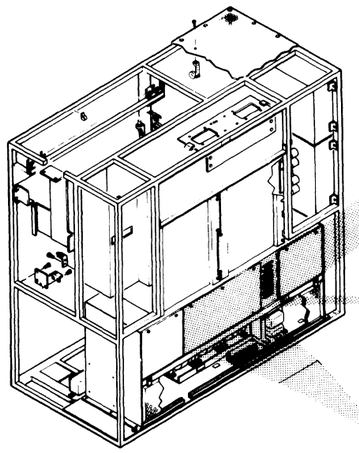
1. *See PWR 50 for locations of regulator/overvoltage cards and for location of the voltage adjustment potentiometers.*
2. *–36V not present in late production machines.*
3. *This configuration will be on late production machines only. All others will appear as shown in assembly.*



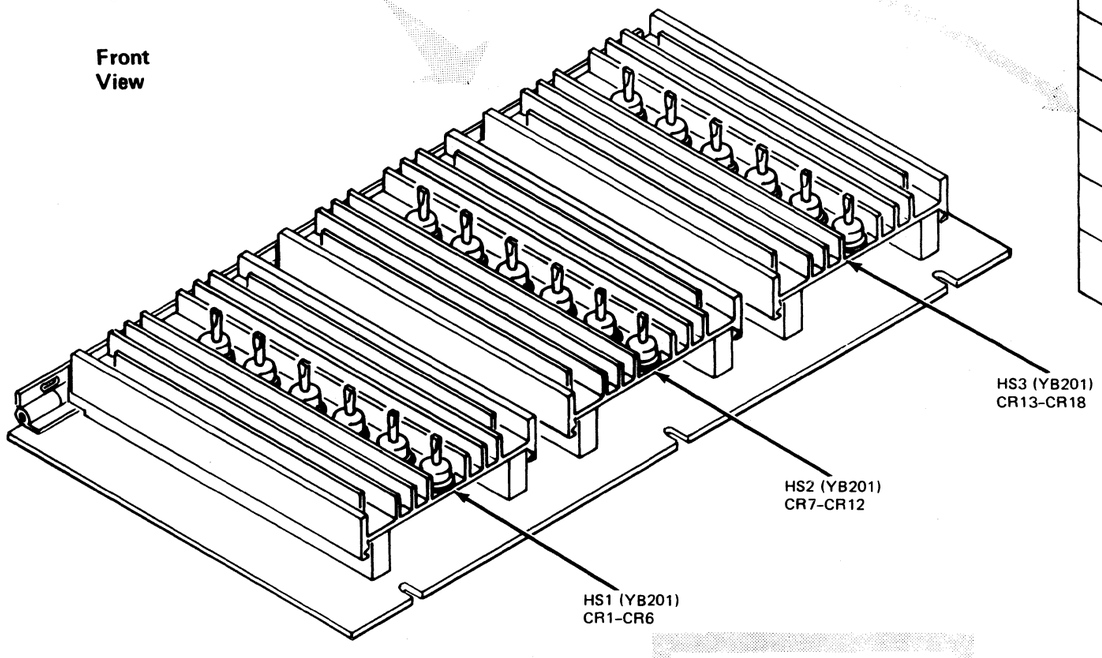
Front View

This configuration will be on late production machines only. All others will appear as shown in assembly.

**Not used in late production machines.*

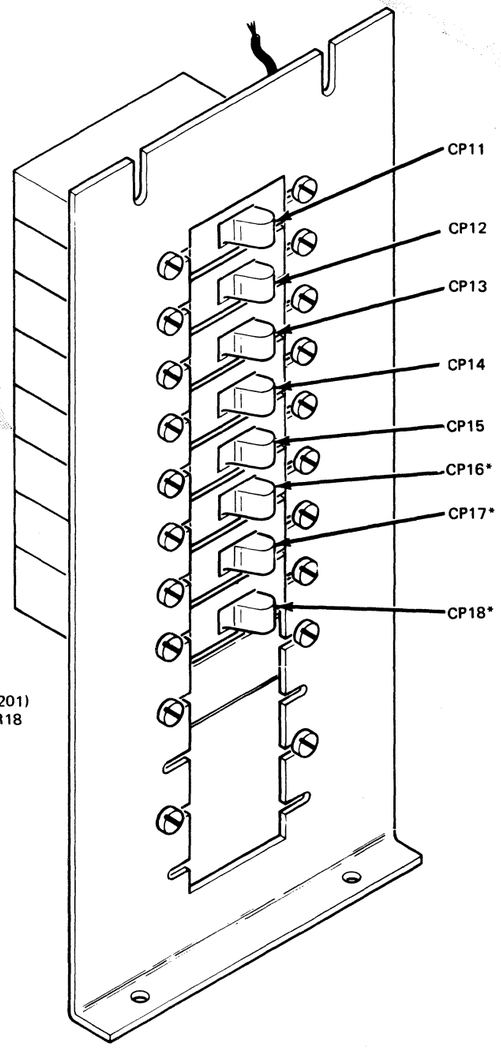


Front View

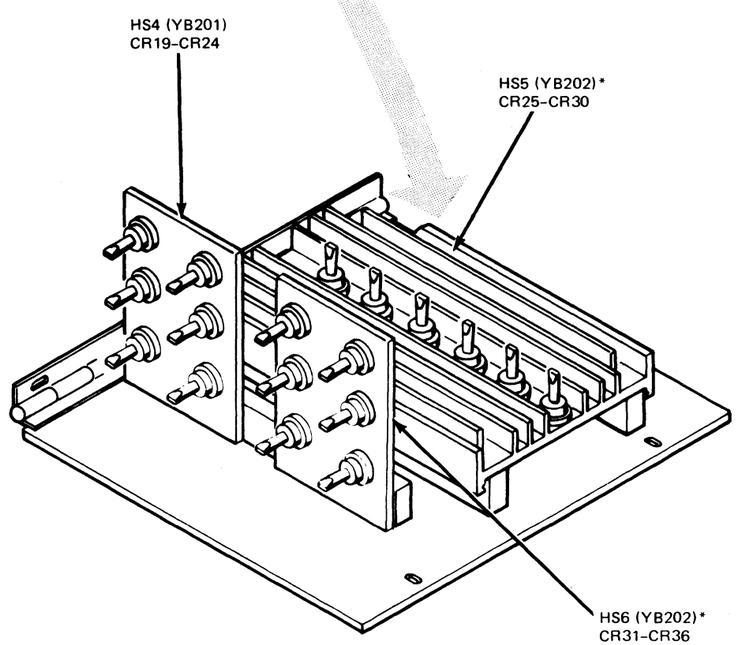


Note 1. The diodes are identified on the machine.

Heat Sinks 1, 2, and 3
Diodes CR1–CR18

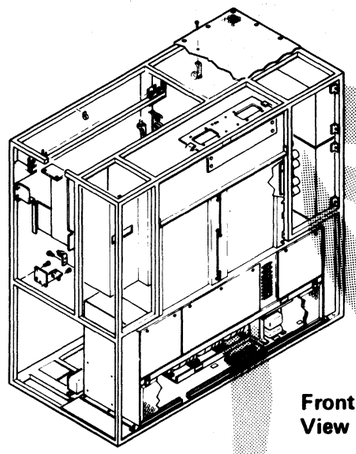


** Not used in late production machines*

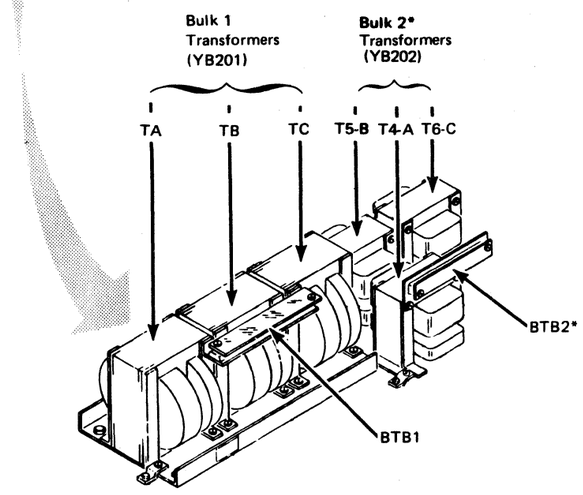


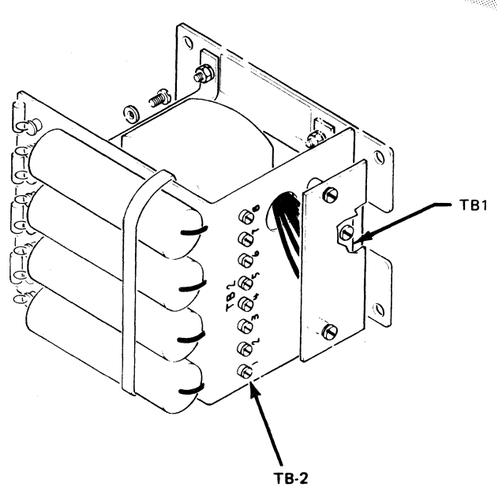
Heat Sinks 4, 5, and 6
Diodes CR19–CR36

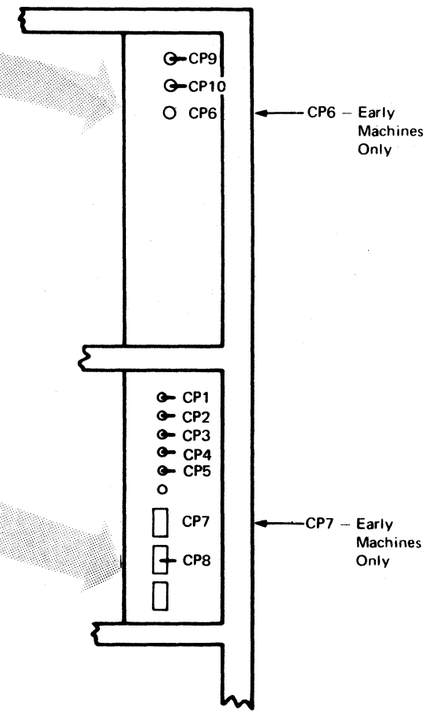
BULK TRANSFORMERS, BIAS SUPPLY, AND CPS 1-10



Front View

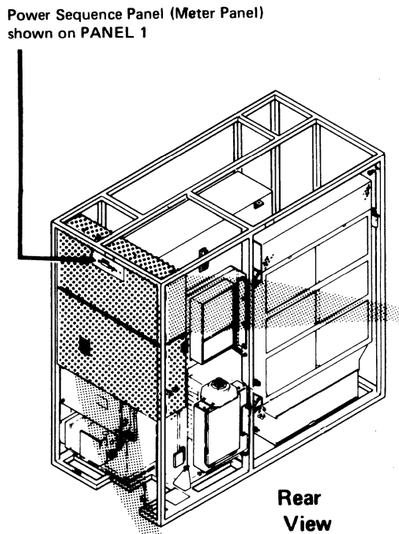


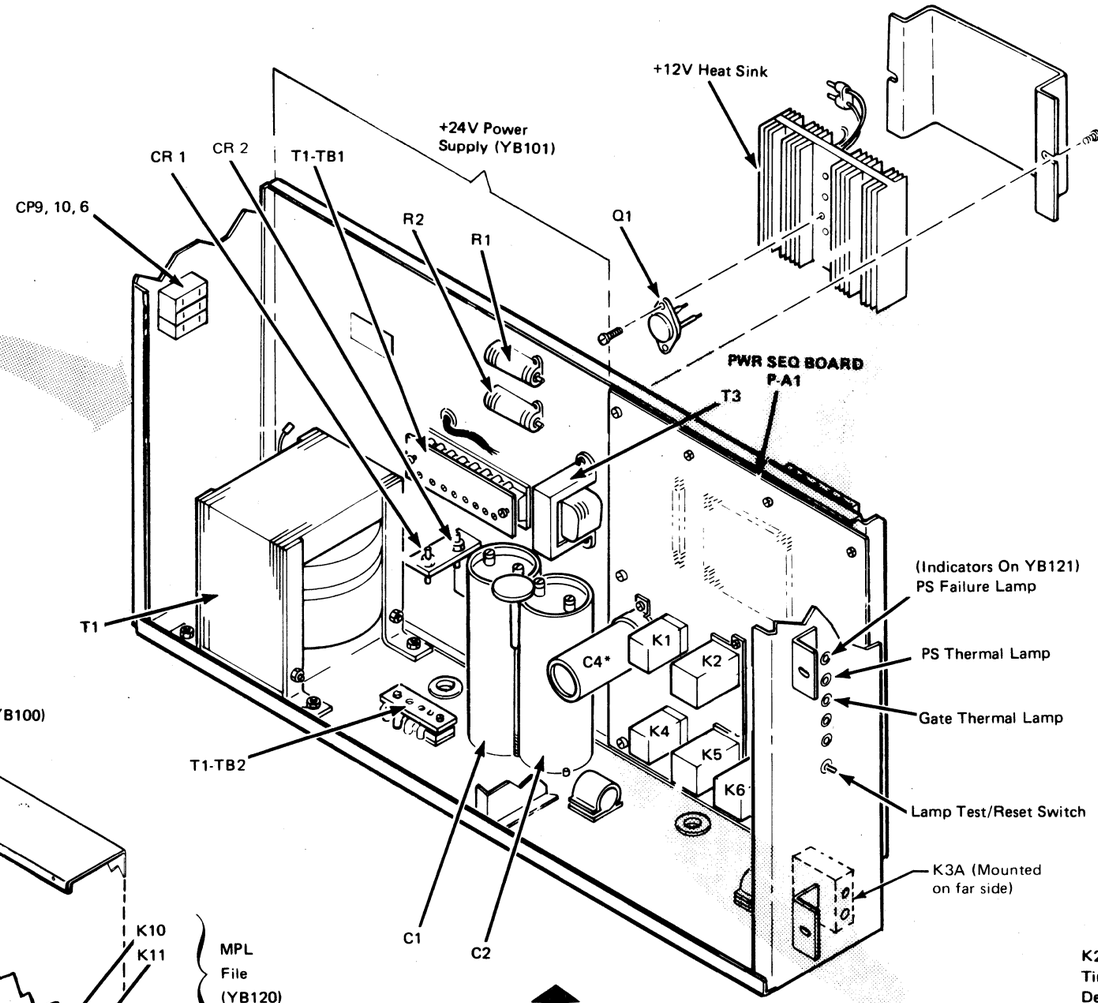


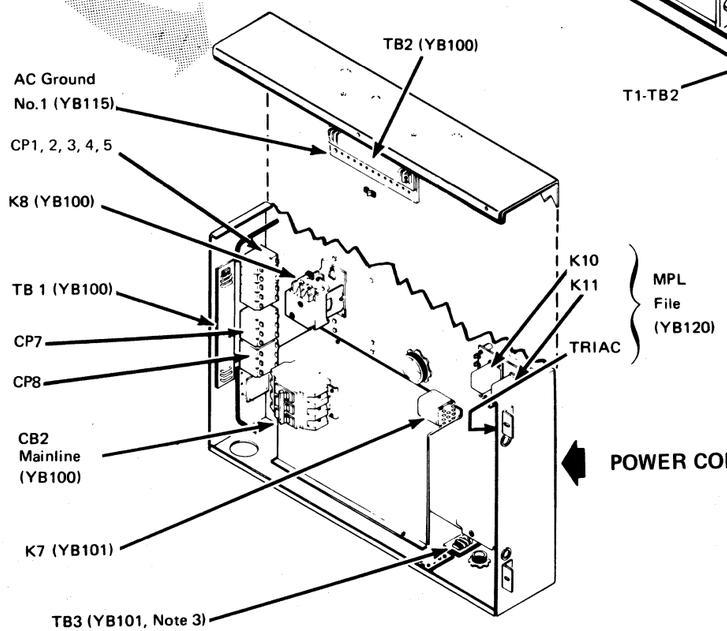


*Not used in late production machines.

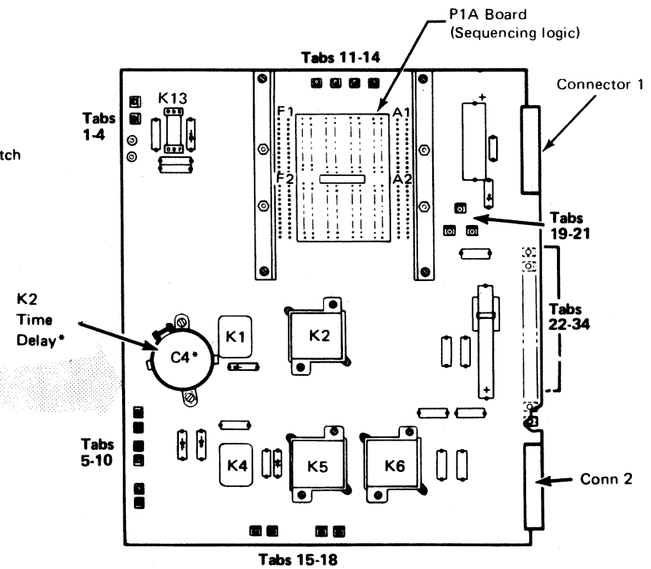
POWER CONTROL BOX AND POWER SEQUENCE BOX



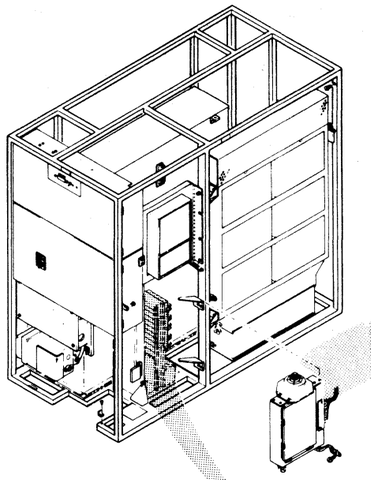




*Not used in late production machines

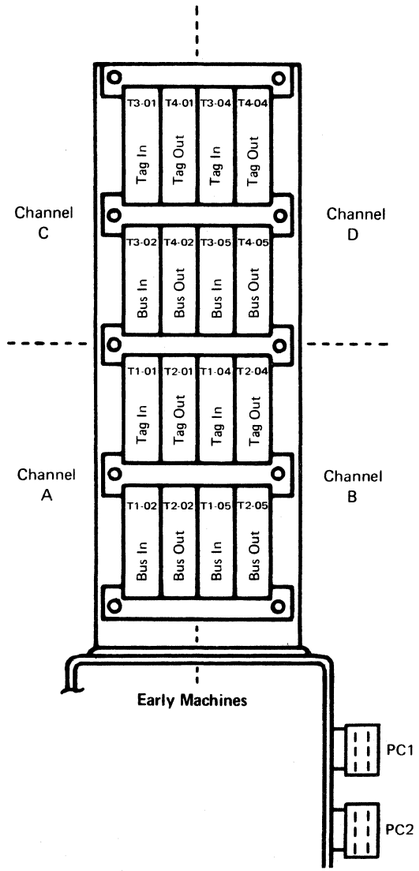


Component Side (Power Seq Board, YB120,121)

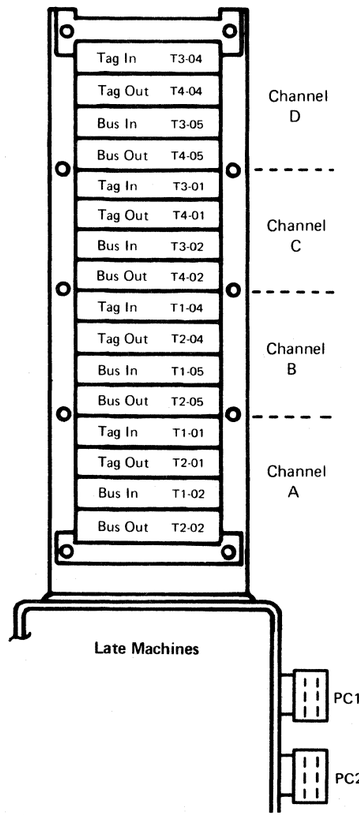


Rear View

I/O CONNECTORS (CHANNEL INTERFACE)

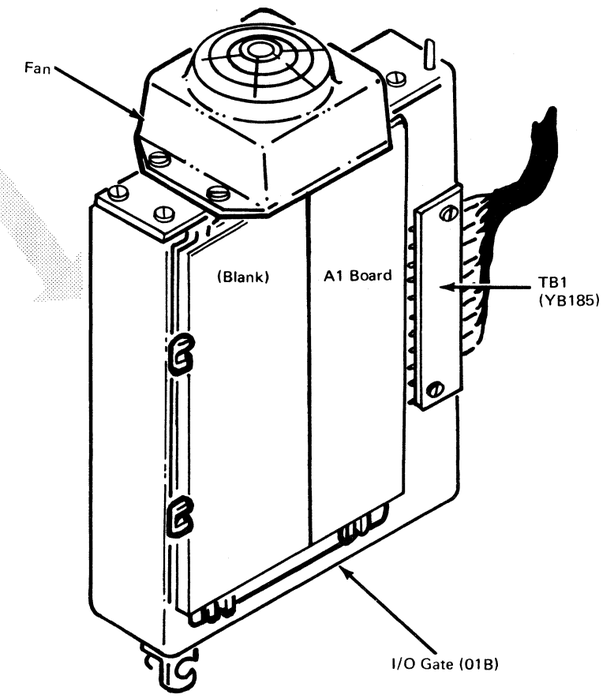


Early Machines

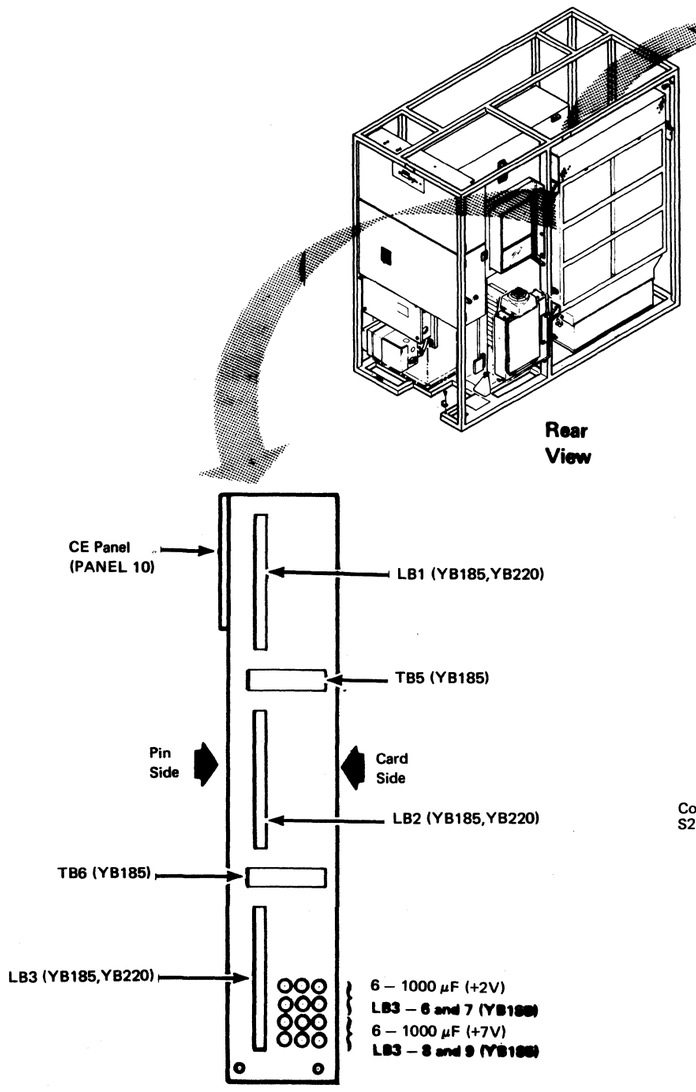


Late Machines

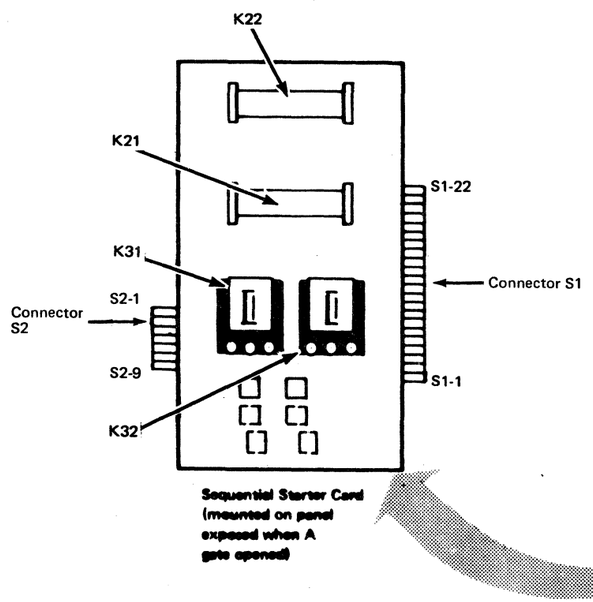
I/O GATE (CHANNEL DRIVERS AND TERMINATORS)



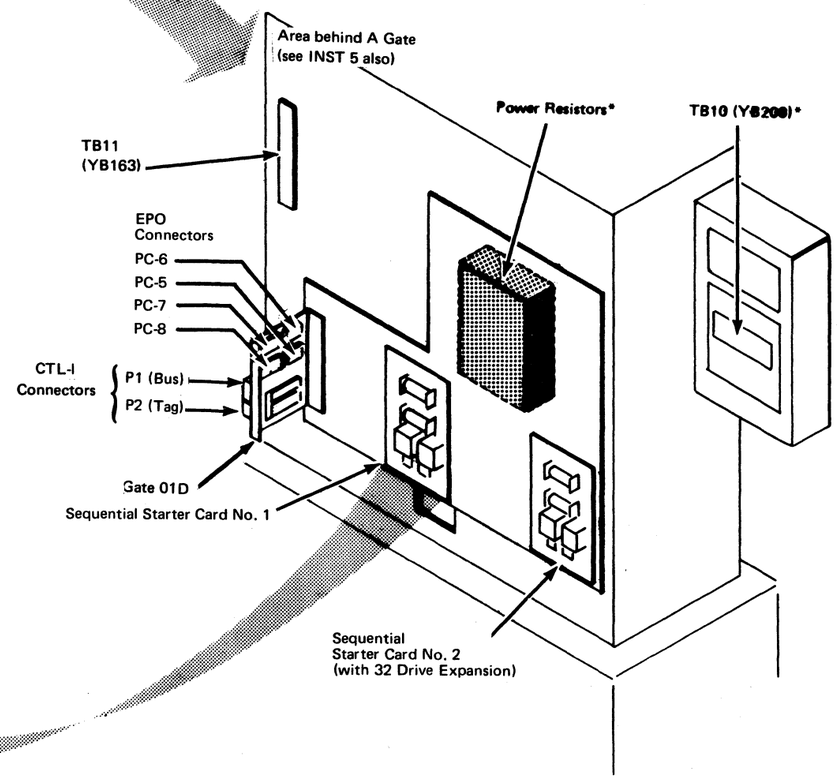
GATE A AND AREA BEHIND GATE



End View of
Gate 01A



Sequential Starter Card
(mounted on panel
exposed when A
gate opened)



*Not used in late production machines

CD0600 Seq 1 of 1	2347361 Part Number	437403 21 Apr 72	437404 23 Jun 72	437405 15 Aug 72	437414 4 Jun 73	437415 2 Nov 73		

CONTENTS

INSTALLATION INSTRUCTIONS

SPECIAL TOOLS AND TEST EQUIPMENT REQUIRED FOR INSTALLATION:

	Part Number
Digitec* Voltmeter	453585
Tektronix** 453 Scope	453047
MPL File CE Disk	
SLT/MST Maintenance Tools	

*Trademark of United Systems Corp.
**Trademark of Tektronix, Inc.

Follow each installation step in sequence to ensure correct operation.

1 UNPACKING AND LOCATING

Check When Complete

___ 1 Remove packing and check for damage. (See Packing/Unpacking instructions taped to cover.)

___ 2 Do an inventory of the parts in the shipping group.

___ 3 Remove the covers as necessary.

___ 4 Adjust leveling jacks.

2 CABLING—CONTROL MODULE TO 3830-2 STORAGE CONTROL

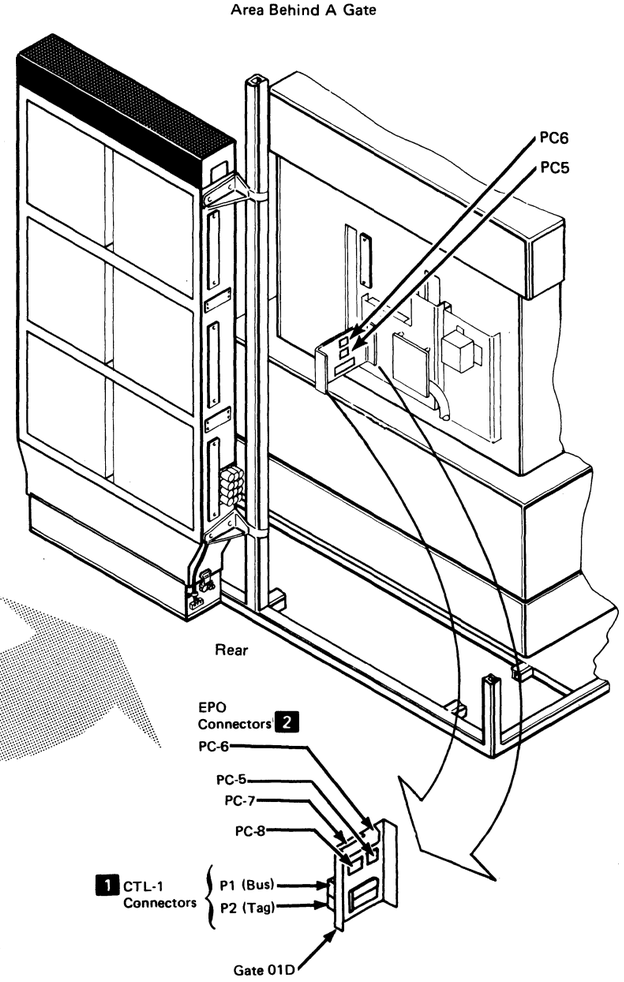
Check When Complete

These instructions are for cable plugging at the 3830-2 only. Refer to device installation instructions for cable plugging of attached devices.

DANGER
Do not connect 3830-2 ac power cable until instructed.

___ 1 Position CTL-I cables from Control Module(s) to 3830-2
Bus on top
Tag on bottom
Do not connect until Wrap Test is complete. Terminate with two (2) Bus Terminators (PN 5440649) in the bus and tag CTL-I connectors of the last cabled controller. **1**

___ 2 Position EPO cable from Control Modules(s) to connector in 3830-2. Do not connect until step 4, Channel Interface Cabling. **2**



INSTALLATION INSTRUCTIONS
(60-Hz Machines Only)

3 CONTROL UNIT POWER CHECK (60 HZ)

For 50 Hz machines, go to step **3** WORLD TRADE on next page.

Check When Complete

____ **1** Open power control and sequence box covers.

____ **2** Turn off 3830-2 mainline CB-2, then connect 3830-2 power cable to ac outlet.

____ **3** Measure ac line voltage at input to CB-2 and determine if it is 208 or 230V ac. If line voltage agrees with the voltage tag on the 3830-2, proceed to step 5.

____ **4** If customer's voltage does not agree, remove ac power connector and rewire the following transformers as shown on YB026. Then reconnect power cable to ac outlet.

	Transformer	Terminal Block
____	T1 SCRID and seq	T1-TB1 E
____	T2 conv outlet	TB3 F
____	Bulk 1 supply	BTB1 B
____	Bulk 2 supply (Note 1)	BTB2 C
____	Bias supply	PS15 TB1 D

____ **5** For power sequencing, verify that EPO jumper plug is in PC-1 G (See Figure 1 for EPO jumper plug wiring).

____ **6** Turn all drive start/stop switches to Stop if drive cables previously connected.

____ **7** Turn off CB2 in 3830-2.

____ **8** Connect 3830-2 power cable to ac outlet and turn on 3830-2 mainline CB2. Check that all CPs in 3830-2 are on.

____ **9** Set operation mode switch on 3830-2 CE panel to CE Mode.

____ **10** Operate Power On switch on 3830-2 CE panel. Power will sequence up in the control unit.

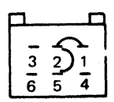
____ **11** Check operation of cooling fans in 3830-2
a. Regulator. A
b. MST logic gate. I
c. I/O tailgate (01B). H

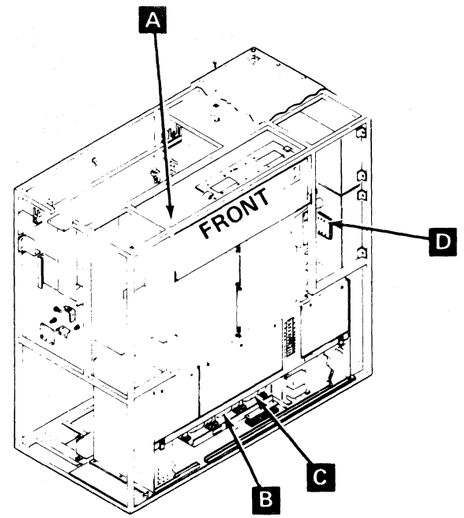
____ **12** Measure the dc voltages with Digitec voltmeter, and adjust as necessary using the procedure on PWR 50.

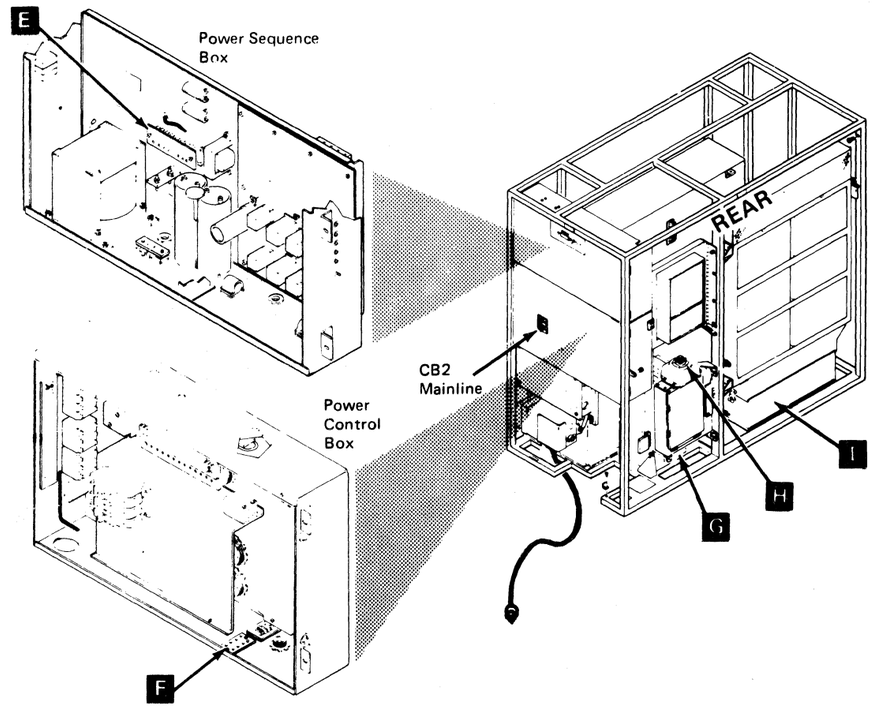
____ **13** When finished go to INST 15A.

Note 1: Only for early machines (with CP7).

Figure 1: EPO Jumper Plug Wiring







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INSTALLATION INSTRUCTIONS
(50Hz Machines Only)

3 CONTROL UNIT POWER CHECK (50HZ) (World Trade)

Check When Complete

____ **1** Determine type and level of voltage at ac outlet: delta (Δ) 200, 220, 235 or wye (Y) 380/408.

____ **2** Refer to the chart on logic page YB026 and verify that the following terminals are wired correctly:

	Power Component	Terminal Block
____	Primary Power Jumpers	T1 F
____	T2 Conv Outlet Transformer	TB3 G
____	T1 SCRID and Seq Transformer	T1-TB1 E
____	Bulk 1 Supply Transformer	BTB1 B
____	Bulk 2 Supply Transformer (Note 1)	BTB2 C
____	Bias Supply Transformer	PS15 TB1 D

____ **3** If wiring of 3830-2 agrees with ac power source, proceed to step 5.

____ **4** If wiring does not agree with power source, refer to YB026 and rewire terminals listed in table above.

____ **5** For power sequencing, verify that EPO jumper plug PC-1 H (See Figure 1 for EPO jumper plug wiring).

____ **6** Turn all drive start/stop switches to Stop if drive cables previously connected.

____ **7** Turn off CB2 in 3830-2.

____ **8** Connect 3830-2 power cable to ac outlet and turn on 3830-2 mainline CB2. Check that all CPs in 3830-2 are on.

____ **9** Set operation mode switch on 3830-2 CE panel to CE Mode.

____ **10** Operate power-on switch on 3830-2 CE panel. Power will sequence up in the control unit.

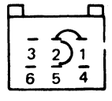
____ **11** Check operation of cooling fans in 3830-2:
- a. Regulator A
- b. MST logic gate J
- c. I/O tailgate (01B) I

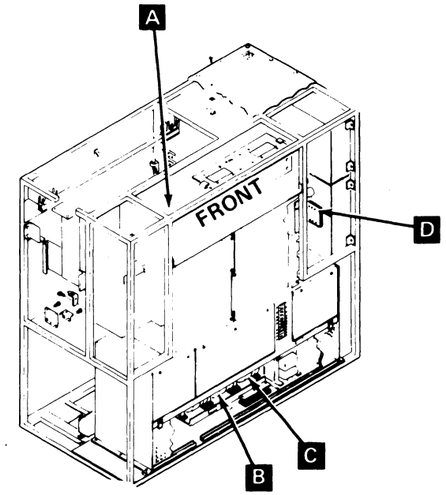
____ **12** Measure the dc voltages with Digitec voltmeter, and adjust as necessary using the procedure on PWR 50.

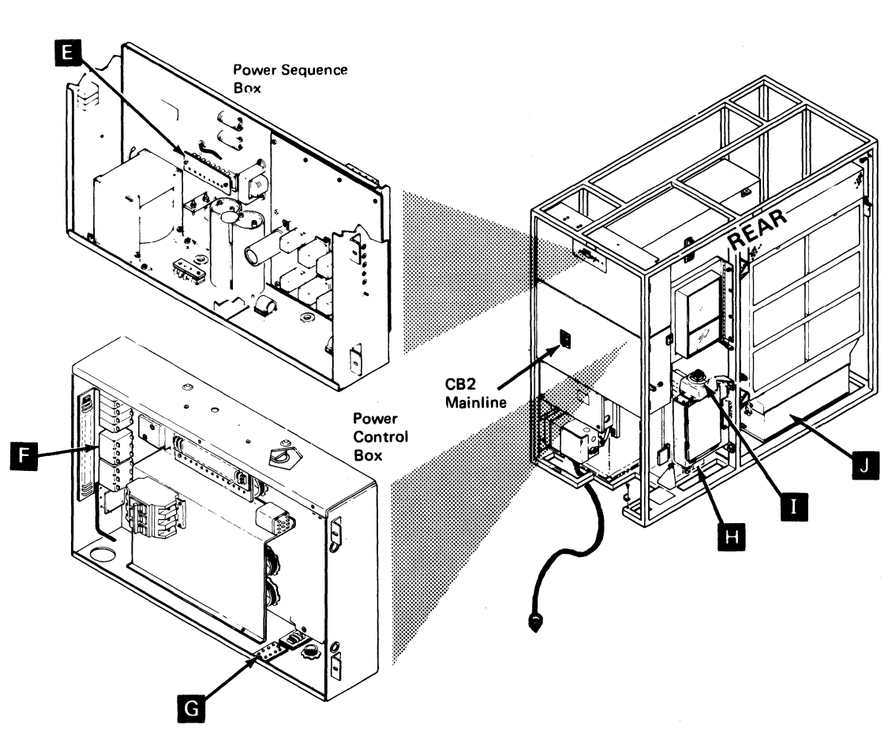
____ **13** When finished go to INST 15A.

Note 1: *Only for early machines (with CP7)*

Figure 1: EPO Jumper Plug Wiring







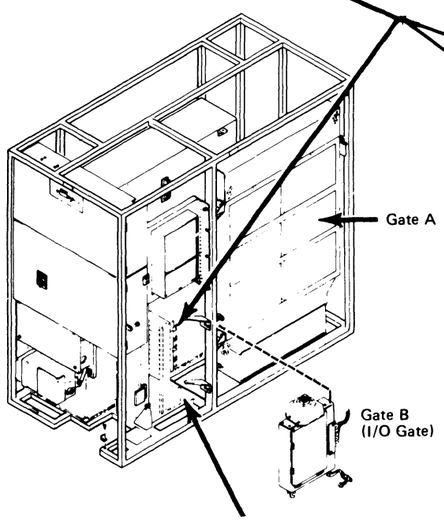
INSTALLATION INSTRUCTIONS

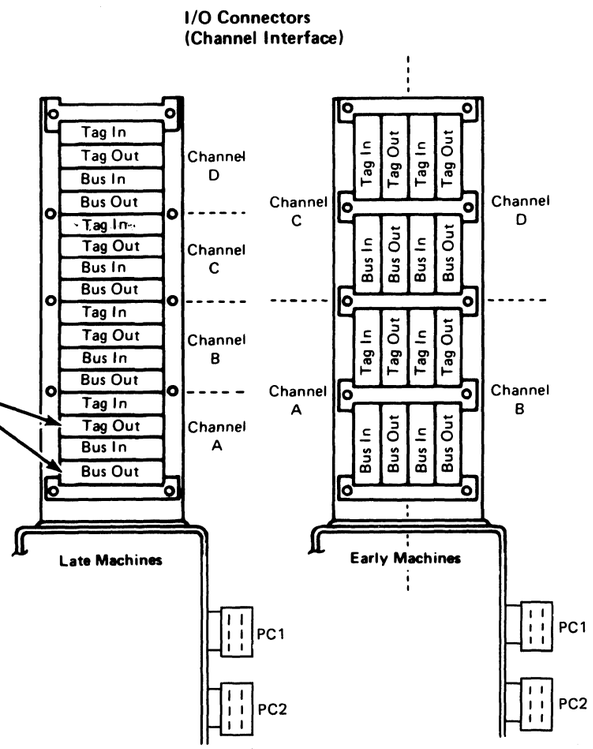
4 CHANNEL INTERFACE CABLING

Check When Complete

___1 Power down 3830-2 from CE panel.

___2 If last device on channel, plug bus terminator (P/N 5440649) and tag terminator (P/N 5440650) into bus out and tag out receptacles for that channel.





___3 Remove EPO jumpers from PC-1. Connect CPO cable(s) from CPU or channel(s) to PC-1, PC-2 (2 Channel) and PC-3 – PC-4* (2 Channel Additional).

Connect Drive EPO sequence cables – PC-5 (first string), PC-6 (second string), PC-7 and PC-8 (third and fourth string – 32 drive expansion feature only)

Remote Switch Feature – Connect remote switch cable(s) to PC-10 and PC-11 if remote switch feature is installed.**

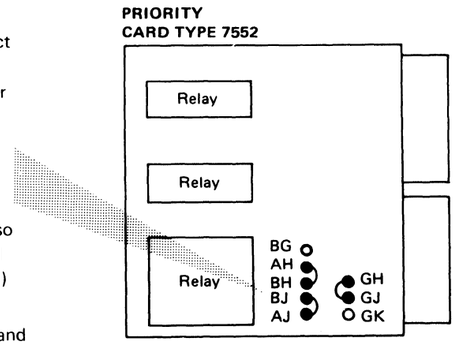
* PC-3 and PC-4 are located on bracket below 01B gate.
** PC-10 (Channel A and B) and PC-11 (Channel C and D) are located below 01B gate and to the left of PC-3 and PC-4 bracket.

___4 Establish channel priority by connecting Select Out jumpers. Card is located in I/O gate at B-A1E6. (See logic page AR101.) Use jumper assembly P/N 816645 or 815925.

High priority is shown. For lowest priority, connect the following jumpers: AH–BG, AJ–BH, and GJ–GK.

If Two Channel Switch feature is installed, also connect jumpers for channel B priority. Card is located at B-A1F6. (See logic page BR101.)

If Two Channel Switch, Additional, feature is installed, also connect jumpers for channel C and D priorities. Cards are located at A-A1D2 and A-A1D4, respectively. (See logic pages CR101 and DR101.)



___5 Go to INST 16 next.

ADDRESSING

START

In a 3830 subsystem, address plugging must be carefully performed to ensure correct subsystem operation.

__ **6.** Obtain the subsystem addresses assigned to this 3830 by the customer.

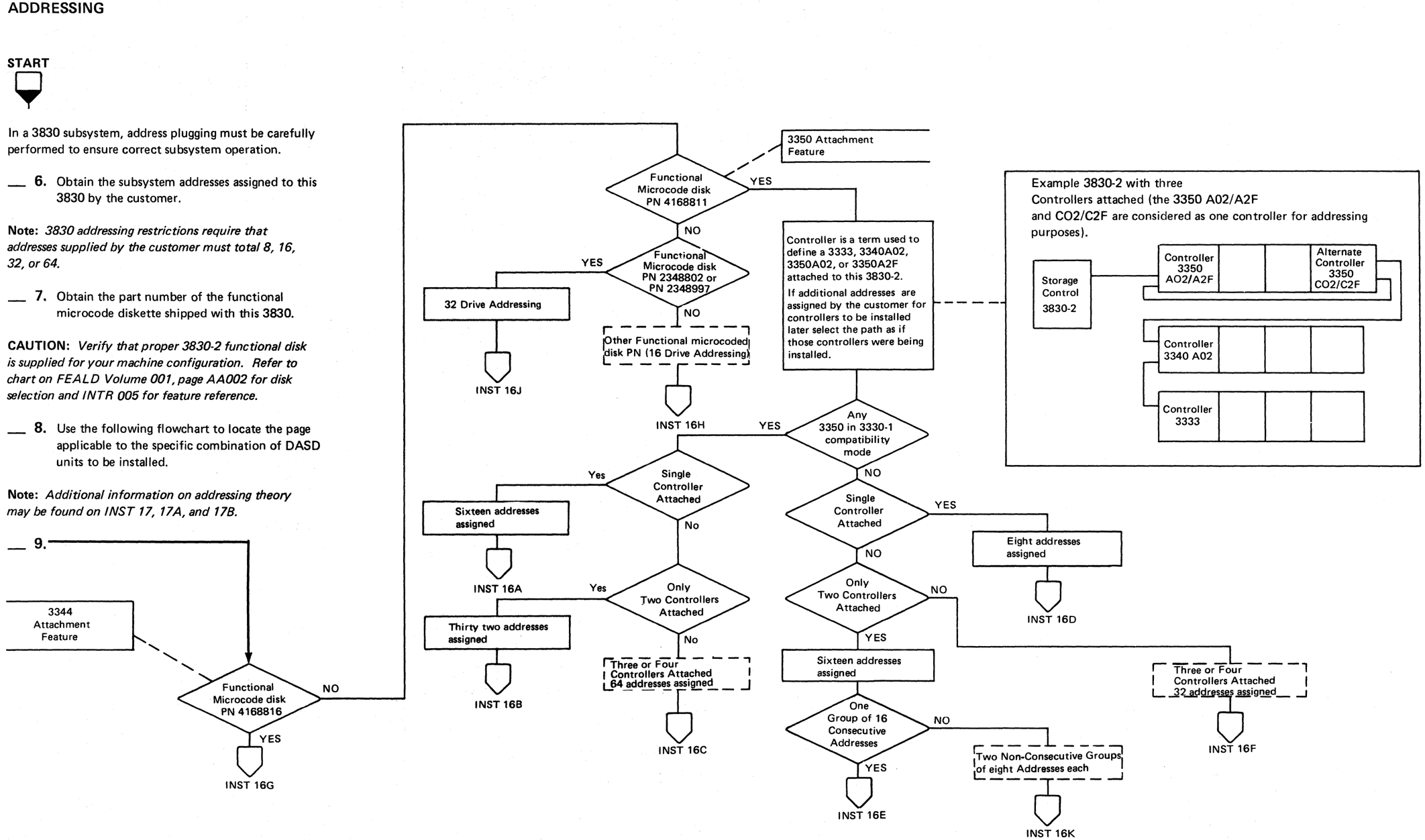
Note: *3830 addressing restrictions require that addresses supplied by the customer must total 8, 16, 32, or 64.*

__ **7.** Obtain the part number of the functional microcode diskette shipped with this 3830.

CAUTION: *Verify that proper 3830-2 functional disk is supplied for your machine configuration. Refer to chart on FEALD Volume 001, page AA002 for disk selection and INTR 005 for feature reference.*

__ **8.** Use the following flowchart to locate the page applicable to the specific combination of DASD units to be installed.

Note: *Additional information on addressing theory may be found on INST 17, 17A, and 17B.*



ADDRESSING

This page is to be used for a 3830 with 16 addresses assigned, and at least one of its attached 3350s will operate in 3330-1 compatibility mode.

When 3350s are to be operated in 3330-1 compatibility mode, the 3350 operates as two 3330s and requires two logical addresses per spindle, a primary and a secondary.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied. These are not consecutive addresses.) Use the valid address column to determine if the primary and secondary address assignments are valid. Any 3350 not in compatibility mode and any 3340 or 3330 use a primary address only.

__ **2.** Plug the Address Select Cards(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.) Each channel must be plugged according to the allocation of addresses for that channel. They may or may not all be plugged the same. If different addresses are required see Note 1.

__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 20) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

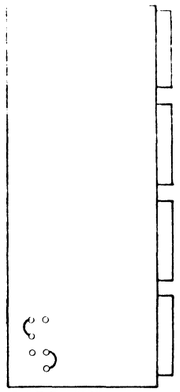
Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

__ **4.** Plug the cards at A1S2, A1T2, A1U2, and B1G2 according to the card diagrams on this page.

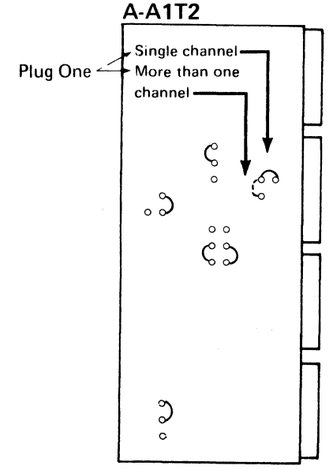
__ **5.** Go to INST 18, entry C.

A-A1S2



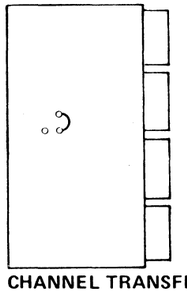
CARD TYPE BA89

A-A1T2



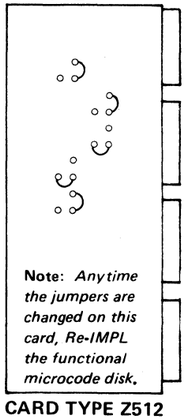
TRANSFER BUFFER CONTROL CARD TYPE BH98

A-A1U2



CHANNEL TRANSFER CONTROL CARD TYPE BA82

A-B1G2

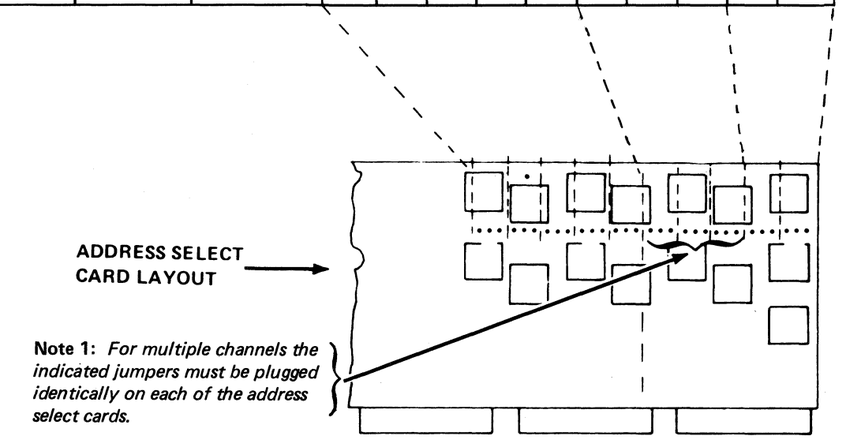


Note: *Anytime the jumpers are changed on this card, Re-IMPL the functional microcode disk.*

CARD TYPE Z512

Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	VALID ADDRESS COMBINATIONS		PLUG ADDRESS SELECT CARD AS SHOWN BELOW
	PRIMARY	SECONDARY	
00-27	00-07	20-27	
08-2F	08-0F	28-2F	
10-37	10-17	30-37	
18-3F	18-1F	38-3F	
40-67	40-47	60-67	
48-6F	48-4F	68-6F	
50-77	50-57	70-77	
58-7F	58-5F	78-7F	
80-A7	80-87	A0-A7	
88-AF	88-8F	A8-AF	
90-B7	90-97	B0-B7	
98-BF	98-9F	B8-BF	
C0-E7	C0-C7	E0-E7	
C8-EF	C8-CF	E8-EF	
D0-F7	D0-D7	F0-F7	
D8-FF	D8-DF	F8-FF	



Note 1: *For multiple channels the indicated jumpers must be plugged identically on each of the address select cards.*

This page is to be used for a 3830 with 32 addresses assigned, and at least one of its attached 3350s will operate in 3330-1 compatibility mode.

When 3350s are to be operated in 3330-1 compatibility mode, the 3350 operates as two 3330s and requires two logical addresses per spindle, a primary and a secondary.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied. These are not consecutive addresses.) Use the valid address column to determine if the primary and secondary address assignments are valid. Any 3350 not in compatibility mode and any 3340 or 3330 use a primary address only.

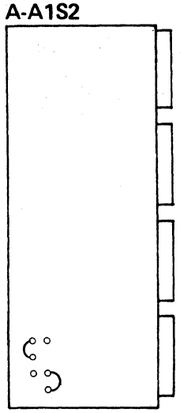
__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.) Each channel must be plugged according to the allocation of addresses for that channel. They may or may not all be plugged the same. If different addresses are required see Note 1.

__ **3.** Mark the plugging and microdiagnostic channel wrap parameter value (shown to the right of the plugging column in Figure 2) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Plug the cards at A1S2, A1T2, A1U2, and B1G2 according to the card diagrams on this page.

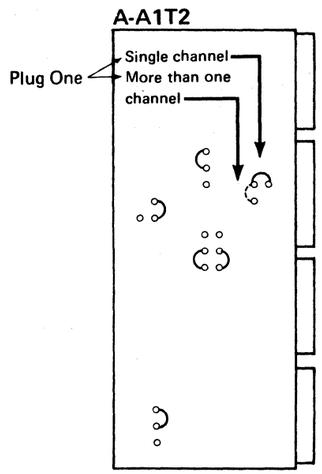
__ **5.** Go to INST 18, entry C.

A-A1S2



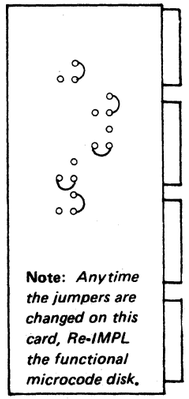
CARD TYPE BA89

A-A1T2



TRANSFER BUFFER CONTROL CARD TYPE BH98

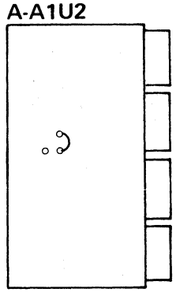
A-B1G2



Note: *Anytime the jumpers are changed on this card, Re-IMPL the functional microcode disk.*

CARD TYPE Z512

A-A1U2



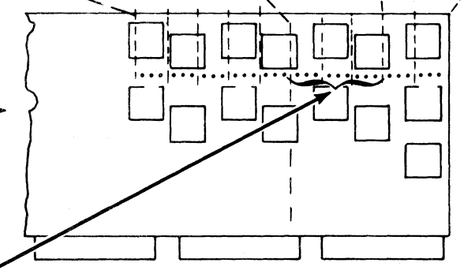
CHANNEL TRANSFER CONTROL CARD TYPE BA82

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A	A-A1Q2
	B	A-A1P2
Two-channel Switch Additional (Four Channels)	A	A-A1Q2
	B	A-A1P2
	C	A-A1K2
	D	A-A1J2

Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	VALID ADDRESS COMBINATIONS		PLUG ADDRESS SELECT CARD AS SHOWN BELOW	MICRODIAGNOSTIC CHANNEL WRAP PARAMETER
	PRIMARY	SECONDARY		
00-37	00-27 10-17	20-27 30-37	ooo oOO oOO oOO oOO oOO ooo ooo oOO oOO	30
00-2F	00-07 08-0F	20-27 28-2F	ooo oOO oOO oOO oOO ooo oOO ooo oOO oOO	28
08-3F	08-0F 18-1F	28-2F 38-3F	ooo oOO oOO oOO oOO OOo ooo ooo oOO oOO	30
10-3F	10-17 18-1F	30-37 38-3F	ooo oOO oOO oOO oOO ooo OOo ooo oOO oOO	28
40-77	40-47 50-57	60-67 70-77	ooo oOO oOO OOo oOO oOO ooo ooo OOo oOO	30
40-6F	40-47 48-4F	60-67 68-6F	ooo oOO oOO OOo oOO ooo oOO ooo OOo oOO	28
48-7F	48-4F 58-5F	68-6F 78-7F	ooo oOO oOO OOo oOO OOo ooo ooo OOo oOO	30
50-7F	50-57 58-5F	70-77 78-7F	ooo oOO oOO OOo oOO ooo OOo ooo OOo oOO	28
80-B7	80-87 90-97	A0-A7 B0-B7	ooo oOO oOO oOO OOo oOO ooo ooo oOO OOo	30
80-AF	80-87 88-8F	A0-A7 A8-AF	ooo oOO oOO oOO OOo ooo oOO ooo oOO OOo	28
88-BF	88-8F 98-9F	A8-AF B8-BF	ooo oOO oOO oOO OOo OOo ooo ooo oOO OOo	30
90-BF	90-97 98-9F	B0-B7 B8-BF	ooo oOO oOO oOO OOo ooo OOo ooo oOO OOo	28
C0-F7	C0-C7 D0-D7	E0-E7 F0-F7	ooo oOO oOO OOo OOo oOO ooo ooo OOo OOo	30
C0-EF	C0-C7 C8-CF	E0-E7 E8-EF	ooo oOO oOO OOo OOo ooo oOO ooo OOo OOo	28
C8-FF	C8-CF D8-DF	E8-EF F8-FF	ooo oOO oOO OOo OOo OOo ooo ooo OOo OOo	30
D0-FF	D0-D7 D8-DF	F0-F7 F8-FF	ooo oOO oOO OOo OOo ooo OOo ooo OOo OOo	28



Note 1: *For multiple channels the indicated jumpers must be plugged identically on each of the address select cards.*

ADDRESSING

This page is to be used for a 3830 with 64 addresses assigned, and at least one of its attached 3350s will operate in 3330-1 compatibility mode.

When 3350s are to be operated in 3330-1 compatibility mode, the 3350 operates as two 3330s and requires two logical addresses per spindle, a primary and a secondary.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

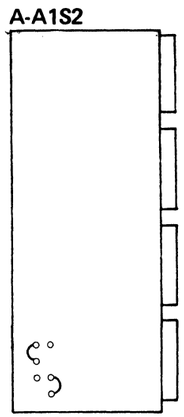
__ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied. These are not consecutive addresses.) Use the valid address column to determine if the primary and secondary address assignments are valid. Any 3350 not in compatibility mode and any 3340 or 3330 use a primary address only.

__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.) Each channel must be plugged according to the allocation of addresses for that channel. They may or may not all be plugged the same.

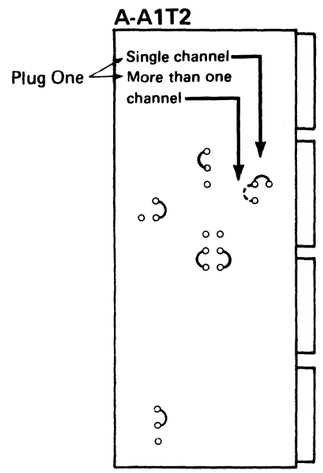
__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 38) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Plug the cards at A1S2, A1T2, A1U2, and B1G2 according to the card diagrams on this page.

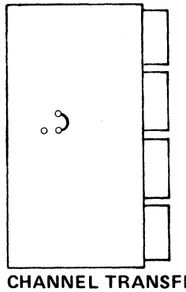
__ **5.** Go to INST 18, entry C.



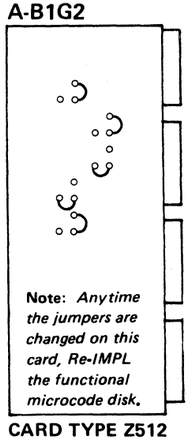
CARD TYPE BA89



TRANSFER BUFFER CONTROL CARD TYPE BH98



CHANNEL TRANSFER CONTROL CARD TYPE BA82



CARD TYPE Z512

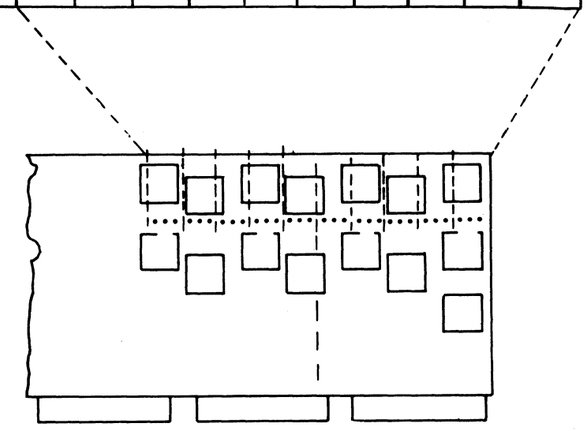
Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	VALID ADDRESS COMBINATIONS		PLUG ADDRESS SELECT CARD(S) AS SHOWN BELOW
	PRIMARY	SECONDARY	
00-3F	00-07 08-0F 10-17 18-1F	20-27 28-2F 30-37 38-3F	
40-7F	40-47 48-4F 50-57 58-5F	60-67 68-6F 70-77 78-7F	
80-BF	80-87 88-8F 90-97 98-9F	A0-A7 A8-AF B0-B7 B8-BF	
C0-FF	C0-C7 C8-CF D0-D7 D8-DF	E0-E7 E8-EF F0-F7 F8-FF	

ADDRESS SELECT CARD LAYOUT →



ADDRESSING

This page is to be used for a 3830 with eight addresses assigned, and all attached 3350s will be operated in native mode or in 3330-11 compatibility mode.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied.)

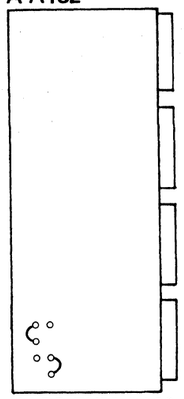
__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.) Each channel must be plugged according to the allocation of addresses for that channel. They may or may not all be plugged the same. If different addresses are required see Note 1.

__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 00) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Plug the cards at A1S2, A1T2, A1U2, and B1G2 according to the card diagrams on this page.

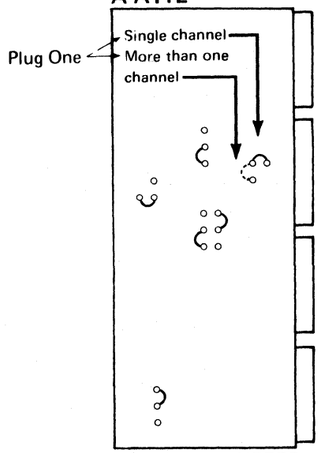
__ **5.** Go to INST 18, entry B.

A-A1S2



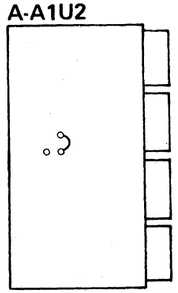
CARD TYPE BA89

A-A1T2



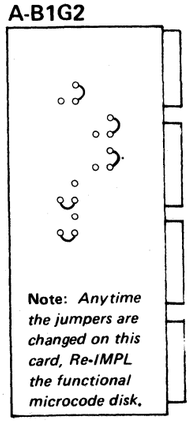
TRANSFER BUFFER CONTROL CARD TYPE BH98

A-A1U2



CHANNEL TRANSFER CONTROL CARD TYPE BA82

A-B1G2



Note: *Anytime the jumpers are changed on this card, Re-IMPL the functional microcode disk.*

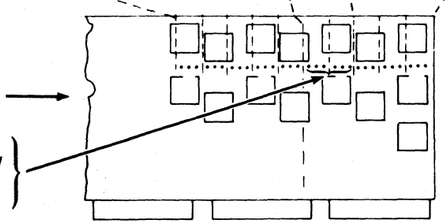
CARD TYPE Z512

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	PLUG ADDRESS SELECT CARD(S) AS SHOWN BELOW
00 - 07	
08 - 0F	
10 - 17	
18 - 1F	
20 - 27	
28 - 2F	
30 - 37	
38 - 3F	
40 - 47	
48 - 4F	
50 - 57	
58 - 5F	
60 - 67	
68 - 6F	
70 - 77	
78 - 7F	
80 - 87	
88 - 8F	
90 - 97	
98 - 9F	
A0 - A7	
A8 - AF	
B0 - B7	
B8 - BF	
C0 - C7	
C8 - CF	
D0 - D7	
D8 - DF	
E0 - E7	
E8 - EF	
F0 - F7	
F8 - FF	



Note 1: *For multiple channels the indicated jumpers must be plugged identically on each of the address select cards.*

ADDRESSING

This page is to be used for a 3830 with 16 consecutive addresses assigned and only two controllers attached. All attached 3350s will be operated in native mode or 3330-11 compatibility mode.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied.)

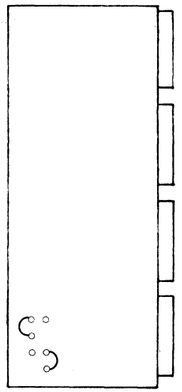
__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.) Each channel must be plugged according to the allocation of addresses for that channel. They may or may not all be plugged the same. If different addresses are required see Note 1.

__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 08) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Plug the cards at A1T2, A1U2, B1G2, and A1S2 according to the card diagrams on this page.

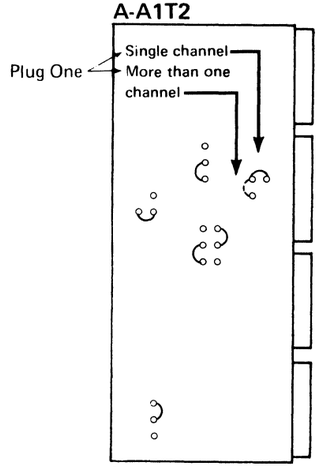
__ **5.** Go to INST 18, entry B.

A-A1S2



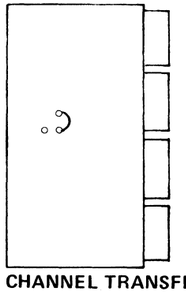
CARD TYPE BA89

A-A1T2



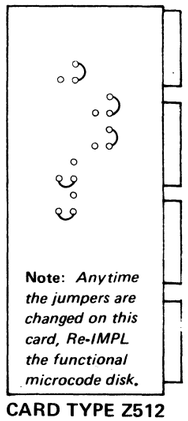
TRANSFER BUFFER CONTROL CARD TYPE BH98

A-A1U2



CHANNEL TRANSFER CONTROL CARD TYPE BA82

A-B1G2



Note: *Anytime the jumpers are changed on this card, Re-IMPL the functional microcode disk.*

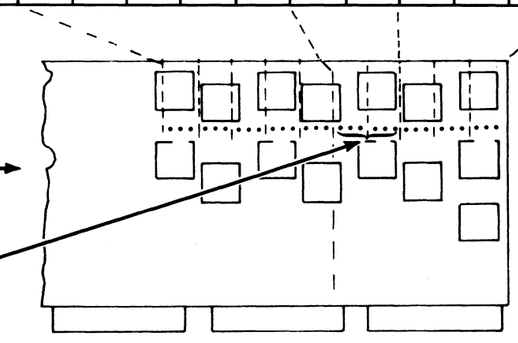
CARD TYPE Z512

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

FIGURE 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	VALID ADDRESS COMBINATIONS	PLUG ADDRESS SELECT CARD AS SHOWN BELOW
00 - 0F	00 - 07 08 - 0F	
10 - 1F	10 - 17 18 - 1F	
20 - 2F	20 - 27 28 - 2F	
30 - 3F	30 - 37 38 - 3F	
40 - 4F	40 - 47 48 - 4F	
50 - 5F	50 - 57 58 - 5F	
60 - 6F	60 - 67 68 - 6F	
70 - 7F	70 - 77 78 - 7F	
80 - 8F	80 - 87 88 - 8F	
90 - 9F	90 - 97 98 - 9F	
A0 - AF	A0 - A7 A8 - AF	
B0 - BF	B0 - B7 B8 - BF	
C0 - CF	C0 - C7 C8 - CF	
D0 - DF	D0 - D7 D8 - DF	
E0 - EF	E0 - E7 E8 - EF	
F0 - FF	F0 - F7 F8 - FF	



Note 1: *For multiple channels the indicated jumpers must be plugged identically on each of the address select cards.*

ADDRESSING

This page is to be used for a 3830 with 32 addresses assigned, and all attached 3350s will be operated in native mode or in 3330-11 compatibility mode.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied.)

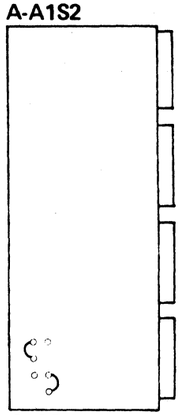
__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.)

__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 18) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Plug the cards at A1S2, A1T2, A1U2, and B1G2 according to the card diagrams on this page.

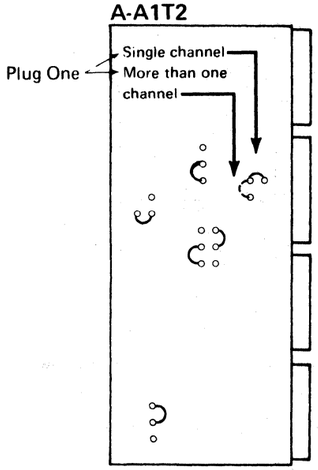
__ **5.** Go to INST 18, entry B.

A-A1S2



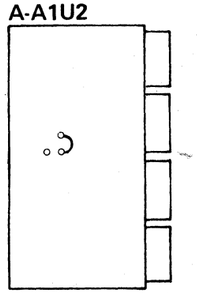
CARD TYPE BA89

A-A1T2



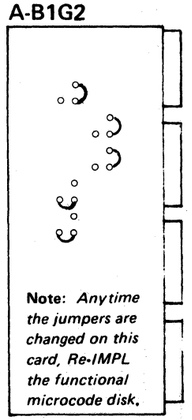
TRANSFER BUFFER CONTROL CARD TYPE BH98

A-A1U2



CHANNEL TRANSFER CONTROL CARD TYPE BA82

A-B1G2



Note: *Anytime the jumpers are changed on this card, Re-IMPL the functional microcode disk.*

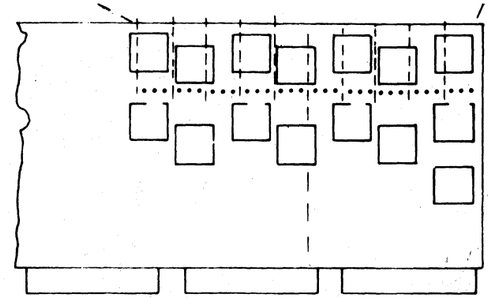
CARD TYPE Z512

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

ADDRESS RANGE	VALID ADDRESS COMBINATIONS	PLUG ADDRESS SELECT CARD(S) AS SHOWN BELOW
00-1F	00-07 08-0F 10-17 18-1F	o o o | o ⌒ | o ⌒ | o ⌒ | o ⌒ | o o o | o o o | o ⌒ | o ⌒ | o ⌒
20-3F	20-27 28-2F 30-37 38-3F	o o o | o ⌒ | ⌒ o | o ⌒ | o ⌒ | o o o | o o o | ⌒ o | o ⌒ | o ⌒
40-5F	40-47 48-4F 50-57 58-5F	o o o | o ⌒ | o ⌒ | ⌒ o | o ⌒ | o o o | o o o | o ⌒ | ⌒ o | o ⌒
60-7F	60-67 68-6F 70-77 78-7F	o o o | o ⌒ | ⌒ o | ⌒ o | o ⌒ | o o o | o o o | ⌒ o | ⌒ o | o ⌒
80-9F	80-87 88-8F 90-97 98-9F	o o o | o ⌒ | o ⌒ | o ⌒ | ⌒ o | o o o | o o o | o ⌒ | o ⌒ | ⌒ o
A0-BF	A0-A7 A8-AF B0-B7 B8-BF	o o o | o ⌒ | ⌒ o | o ⌒ | ⌒ o | o o o | o o o | ⌒ o | o ⌒ | ⌒ o
C0-DF	C0-C7 C8-CF D0-D7 D8-DF	o o o | o ⌒ | o ⌒ | ⌒ o | ⌒ o | o o o | o o o | o ⌒ | ⌒ o | ⌒ o
E0-FF	E0-E7 E8-EF F0-F7 F8-FF	o o o | o ⌒ | ⌒ o | ⌒ o | ⌒ o | o o o | o o o | ⌒ o | ⌒ o | ⌒ o

ADDRESS SELECT CARD LAYOUT →



ADDRESSING

This page is to be used for a 3830 with 64 addresses assigned, and with 3344 Attachment Feature (Functional Microcode diskette PN 4168816).

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 add retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied.)

__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (see Figure 1 for Card(s) location chart.)

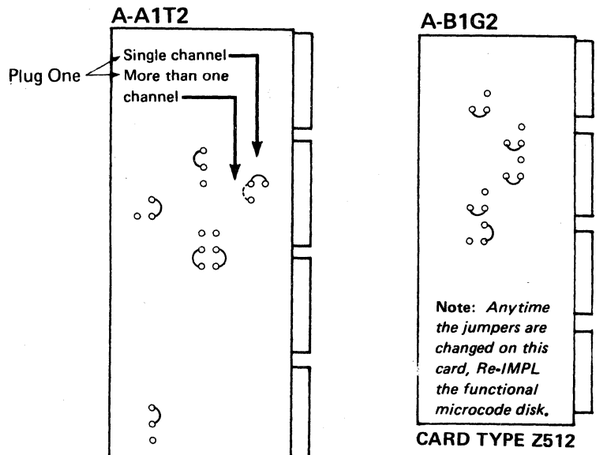
__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 38) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Plug the cards at A1T2, A1U2, and B1G2 according to the card diagrams on this page.

Note: If 8K (2151 feature, see INTRO 5) is installed use Figure 3 to plug A-B1G2, A-A1U2, and A-A1S2 and the card diagrams to plug A-A1T2.

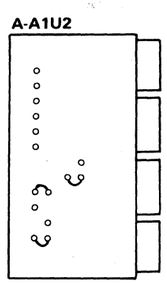
__ **5.** Go to INST 18, entry C.

CARD DIAGRAMS



TRANSFER BUFFER CONTROL CARD TYPE BH98

CARD TYPE Z512



CARD TYPE 0792

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	PLUG ADDRESS SELECT CARD(S) AS SHOWN BELOW
00-3F	○ ○ ○ ○ ∩ ○ ∩ ○ ∩ ○ ∩ ○ ○ ○ ○ ○ ○ ○ ○ ∩ ○ ∩
40-7F	○ ○ ○ ○ ∩ ○ ∩ ○ ∩ ∩ ○ ○ ○ ○ ○ ○ ○ ∩ ○ ∩ ○
80-BF	○ ○ ○ ○ ∩ ○ ∩ ○ ∩ ∩ ○ ○ ○ ○ ○ ○ ○ ∩ ∩ ○ ∩
C0-FF	○ ○ ○ ○ ∩ ○ ∩ ∩ ○ ∩ ○ ○ ○ ○ ○ ○ ○ ∩ ∩ ○ ∩

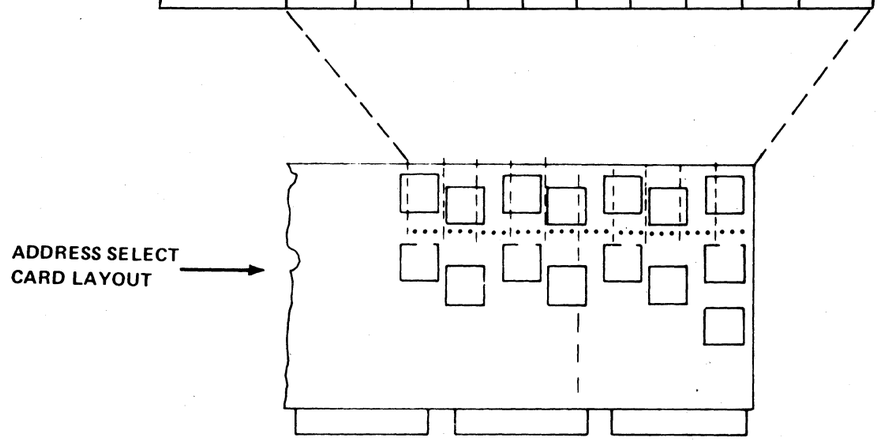
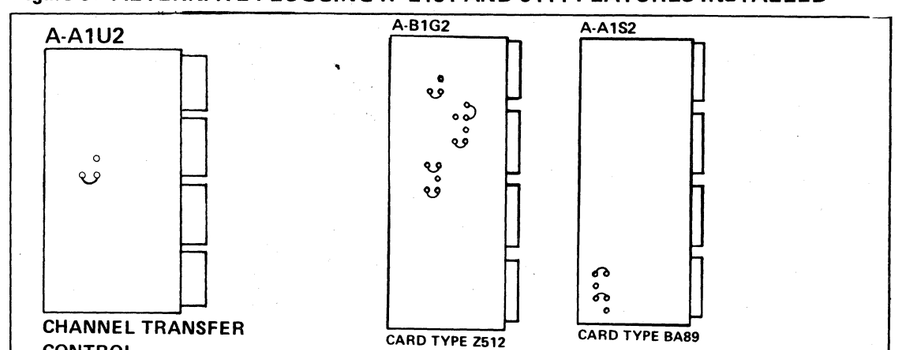


Figure 3: ALTERNATE PLUGGING IF 2151 AND 6111 FEATURES INSTALLED



If 2151 feature (Expanded Control Store, 8K) and 6111 feature (register expansion) is installed and using 3344 microcode diskette P/N 4168816, plug A-A1S2, A-A1U2 and A-B1G2 as shown above.

This page is to be used for a 3830 with 16 addresses assigned, no 3344s or 3350s in the system, and using one of the following microcode diskettes:

P/N 2348786 or
P/N 2348805 or
P/N 2348787 or
P/N 2348757 or
P/N 2348996

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied.)

__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.) Each channel must be plugged according to the allocation of addresses for that channel. They may or may not all be plugged the same. If different addresses are required see Note 1.

__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 00) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Choose one of the following using INTRO 5 to determine features:

a. If 4K (basic) or 6K (2150 feature) machine without Register Expansion (6111 feature) use figure 3 to plug A-A1U2 and A-A1T2.

b. If 6K (2150 feature) and Register Expansion (6111 feature) are installed use figure 4 to plug A-A1U2, A-A1T2 and A-B1G2.

c. If 8K (2151 feature) and Register Expansion (6111 feature) are installed microcode diskette P/N 4168811 must be used. Return to INST 16 to determine correct address plugging.

__ **5.** Go to INST 18, entry A.

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

Figure 3: 4K or 6K without 6111 feature

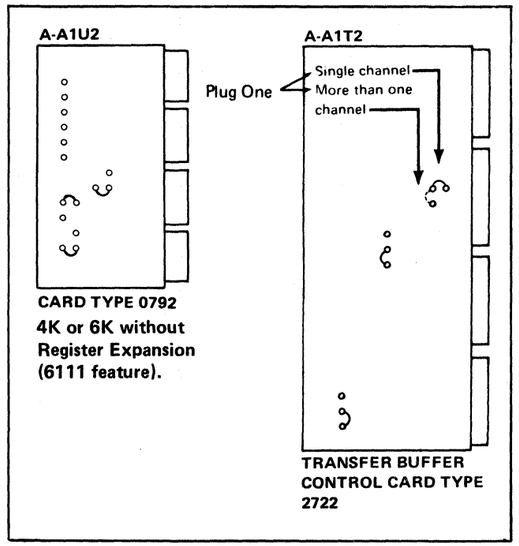


Figure 4: 6K Machine with Register Expansion

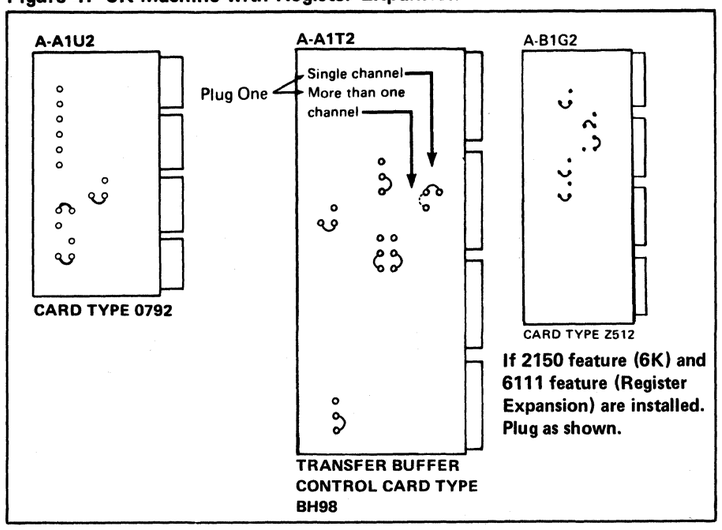
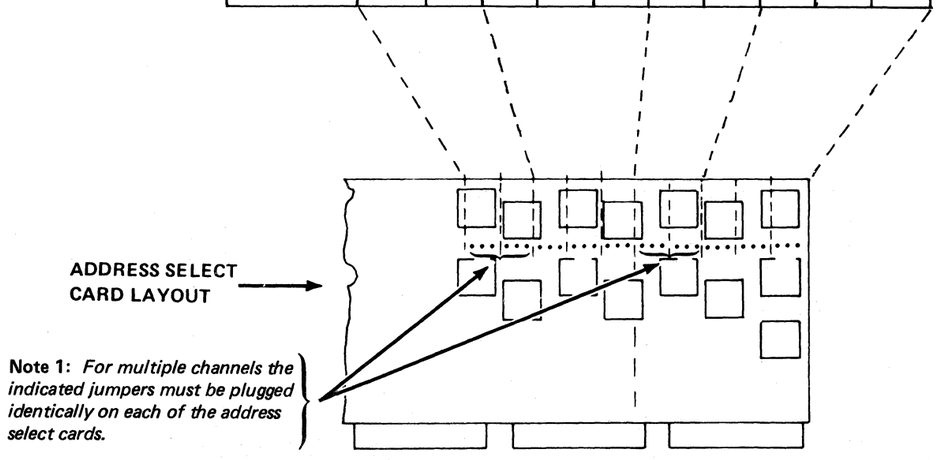


Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	PLUG ADDRESS SELECT CARD(S) AS SHOWN BELOW
00-0F	○○○ ○⌒ ○⌒ ○⌒ ○⌒ ○○○ ○⌒ ○⌒ ○⌒ ○⌒
10-1F	○○○ ⌒○ ○⌒ ○⌒ ○⌒ ○○○ ⌒○ ○⌒ ○⌒ ○⌒
20-2F	○○○ ○⌒ ⌒○ ○⌒ ○⌒ ○○○ ○⌒ ⌒○ ○⌒ ○⌒
30-3F	○○○ ⌒○ ⌒○ ○⌒ ○⌒ ○○○ ⌒○ ⌒○ ○⌒ ○⌒
40-4F	○○○ ○⌒ ○⌒ ⌒○ ○⌒ ○○○ ○⌒ ○⌒ ⌒○ ○⌒
50-5F	○○○ ⌒○ ○⌒ ⌒○ ○⌒ ○○○ ⌒○ ○⌒ ⌒○ ○⌒
60-6F	○○○ ○⌒ ⌒○ ⌒○ ○⌒ ○○○ ○⌒ ⌒○ ⌒○ ○⌒
70-7F	○○○ ⌒○ ⌒○ ⌒○ ○⌒ ○○○ ⌒○ ⌒○ ⌒○ ○⌒
80-8F	○○○ ○⌒ ○⌒ ○⌒ ⌒○ ○○○ ○⌒ ○⌒ ○⌒ ⌒○
90-9F	○○○ ⌒○ ○⌒ ○⌒ ⌒○ ○○○ ⌒○ ○⌒ ○⌒ ⌒○
A0-AF	○○○ ○⌒ ⌒○ ○⌒ ⌒○ ○○○ ○⌒ ⌒○ ○⌒ ⌒○
B0-BF	○○○ ⌒○ ⌒○ ○⌒ ⌒○ ○○○ ⌒○ ⌒○ ○⌒ ⌒○
C0-CF	○○○ ○⌒ ○⌒ ⌒○ ⌒○ ○○○ ○⌒ ○⌒ ⌒○ ⌒○
D0-DF	○○○ ⌒○ ○⌒ ⌒○ ⌒○ ○○○ ⌒○ ○⌒ ⌒○ ⌒○
E0-EF	○○○ ○⌒ ⌒○ ⌒○ ⌒○ ○○○ ○⌒ ⌒○ ⌒○ ⌒○
F0-FF	○○○ ⌒○ ⌒○ ⌒○ ⌒○ ○○○ ⌒○ ⌒○ ⌒○ ⌒○



Note 1: *For multiple channels the indicated jumpers must be plugged identically on each of the address select cards.*

CG0425 Seq. 2 of 2	4290986 Part No. (8)	447460 19 Dec 75	447461 12 Mar 76	447465 15 Dec 78		

ADDRESSING

This page is to be used for a 3830 with 32 addresses assigned and no 3344s or 3350s in the subsystem.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

___ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied.)

___ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.)

___ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 01) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

___ **4.** Choose one of the following using INTRO 5 to determine features:

a. If 6K (2150 feature) machine without Register Expansion (6111 feature) use figure 3 to plug A-A1U2 and A-A1T2.

b. If 6K (2150 feature) and Register Expansion (6111 feature) are installed use figure 4 to plug A-A1U2, A-A1T2 and A-B1G2.

c. If 8K (2151 feature) and Register Expansion (6111 feature) are installed microcode diskette P/N 4168811 must be used. Return to INST 16 to determine correct address plugging.

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

___ **5.** Go to INST 18, entry B.

Figure 3: 6K WITHOUT 6111 FEATURE

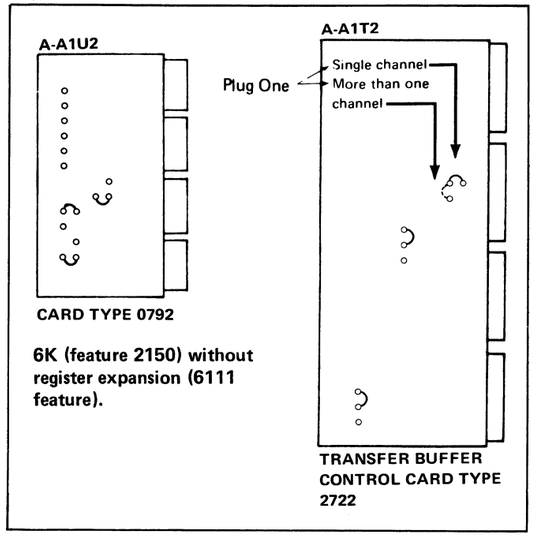


Figure 4: 6K MACHINE WITH REGISTER EXPANSION

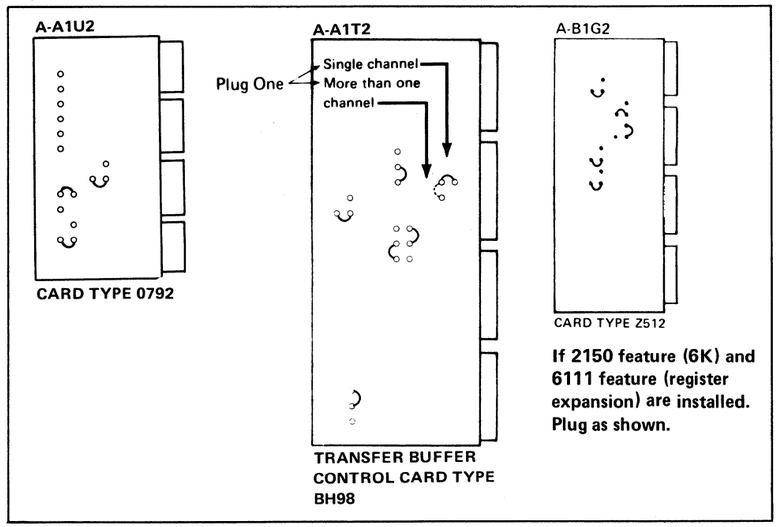
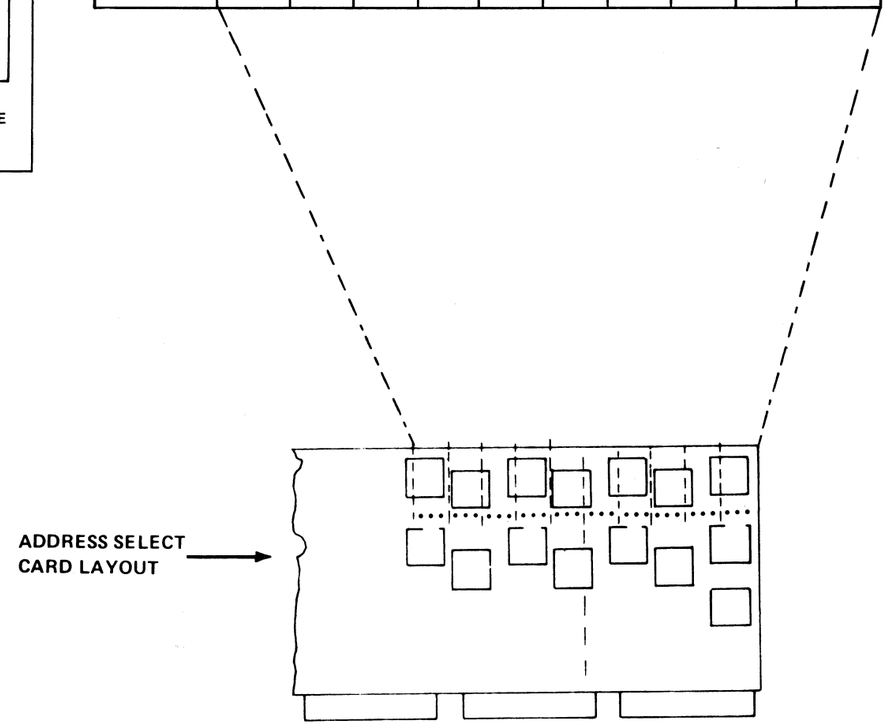


Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	PLUG ADDRESS SELECT CARD(S) AS SHOWN BELOW
00-1F	○ ○ ○ ○ ○ ○ ○ ⌒ ○ ⌒ ○ ⌒ ○ ○ ○ ○ ○ ○ ⌒ ○ ⌒ ○ ⌒
20-3F	○ ○ ○ ○ ○ ○ ⌒ ○ ○ ⌒ ○ ⌒ ○ ⌒ ○ ○ ○ ⌒ ○ ○ ⌒ ○ ⌒
40-5F	○ ○ ○ ○ ○ ○ ⌒ ○ ⌒ ○ ○ ⌒ ○ ⌒ ○ ○ ○ ⌒ ○ ⌒ ○ ⌒
60-7F	○ ○ ○ ○ ○ ○ ⌒ ○ ⌒ ○ ○ ⌒ ○ ⌒ ○ ○ ○ ⌒ ○ ⌒ ○ ⌒
80-9F	○ ○ ○ ○ ○ ○ ⌒ ○ ○ ⌒ ⌒ ○ ○ ○ ○ ○ ⌒ ○ ⌒ ⌒ ○
A0-BF	○ ○ ○ ○ ○ ○ ⌒ ○ ○ ⌒ ⌒ ○ ○ ○ ○ ○ ⌒ ○ ○ ⌒ ○
C0-DF	○ ○ ○ ○ ○ ○ ⌒ ⌒ ○ ⌒ ⌒ ○ ○ ○ ○ ○ ⌒ ⌒ ○ ⌒ ○
E0-FF	○ ○ ○ ○ ○ ○ ⌒ ○ ⌒ ○ ⌒ ○ ○ ○ ○ ○ ⌒ ○ ⌒ ○ ⌒ ○



ADDRESSING

This page is to be used for a 3830 with two non-consecutive groups of eight addresses assigned and only two controllers attached. All attached 3350s will be operated in native mode or 3330-11 compatibility mode.

CAUTION: *Addresses shown in Figure 2 are the ONLY valid combinations that can be used.*

If the addresses you were given do not appear in Figure 2, return to INST 16 and retrace your path in the flow diagrams. If this is the correct page and you still cannot match addresses, verify them with the customer. See INST 17 for additional information.

__ **1.** Match the customer-supplied addresses to the address range in Figure 2. (Address range is the lowest and highest address supplied. These are not consecutive addresses.)

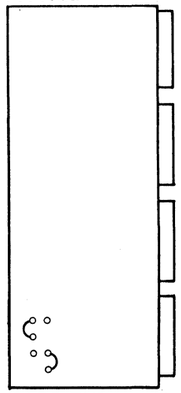
__ **2.** Plug the Address Select Card(s) as indicated in Figure 2. (See Figure 1 for Card(s) location chart.) Each channel must be plugged according to the allocation of addresses for that channel. They may or may not all be plugged the same. If different addresses are required see Note 1.

__ **3.** Mark the plugging and the microdiagnostic channel wrap parameter value (parameter value = 10) on the label attached to the shroud of the address card. This information will be used later during checkout. If no label is available write this information in Note 1. on MICRO 200, Step 11 and MICRO 210, Step 4.

__ **4.** Plug the cards at A1S2, A1T2, B1G2, and A1U2 according to the diagrams on this page.

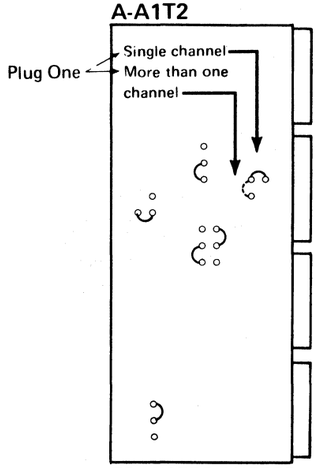
__ **5.** Go to INST 18, entry B.

A-A1S2



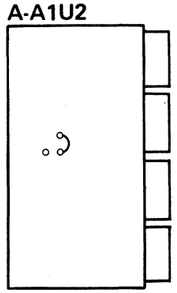
CARD TYPE BA89

A-A1T2



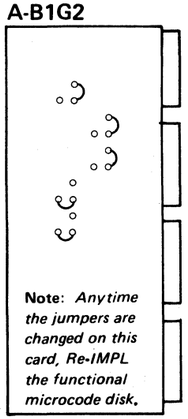
TRANSFER BUFFER CONTROL CARD TYPE BH98

A-A1U2



CHANNEL TRANSFER CONTROL CARD TYPE BA82

A-B1G2



Note: *Anytime the jumpers are changed on this card, Re-IMPL the functional microcode disk.*

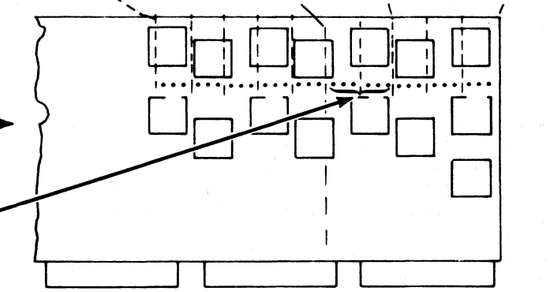
CARD TYPE Z512

Figure 1: CARD LOCATION CHART

CHANNEL FEATURE	CHNL	LOCATION
Single Channel	A	A-A1Q2
Two-channel Switch	A B	A-A1Q2 A-A1P2
Two-channel Switch Additional (Four Channels)	A B C D	A-A1Q2 A-A1P2 A-A1K2 A-A1J2

Figure 2: ADDRESS SELECT CARD(S) PLUG CHART

ADDRESS RANGE	VALID ADDRESS COMBINATIONS	PLUG ADDRESS SELECT CARD AS SHOWN BELOW
00 - 17	00 - 07 10 - 17	○○○ ○◠◠ ○◠◠ ○◠◠ ○◠◠ ○◠◠ ○○○ ○◠◠ ○◠◠ ○◠◠
80 - 1F	08 - 0F 18 - 1F	○○○ ○◠◠ ○◠◠ ○◠◠ ○◠◠ ◠◠○ ○○○ ○◠◠ ○◠◠ ○◠◠
20 - 37	20 - 27 30 - 37	○○○ ○◠◠ ◠◠○ ○◠◠ ○◠◠ ○◠◠ ○○○ ◠◠○ ○◠◠ ○◠◠
28 - 3F	28 - 2F 38 - 3F	○○○ ○◠◠ ◠◠○ ○◠◠ ○◠◠ ◠◠○ ○○○ ◠◠○ ○◠◠ ○◠◠
40 - 57	40 - 47 50 - 57	○○○ ○◠◠ ○◠◠ ◠◠○ ○◠◠ ○◠◠ ○○○ ○◠◠ ◠◠○ ○◠◠
48 - 5F	48 - 4F 58 - 5F	○○○ ○◠◠ ○◠◠ ◠◠○ ○◠◠ ◠◠○ ○○○ ○◠◠ ◠◠○ ○◠◠
60 - 77	60 - 67 70 - 77	○○○ ○◠◠ ◠◠○ ◠◠○ ○◠◠ ○◠◠ ○○○ ◠◠○ ◠◠○ ○◠◠
68 - 7F	68 - 6F 78 - 7F	○○○ ○◠◠ ◠◠○ ◠◠○ ○◠◠ ◠◠○ ○○○ ◠◠○ ◠◠○ ○◠◠
80 - 97	80 - 87 90 - 97	○○○ ○◠◠ ○◠◠ ○◠◠ ◠◠○ ○◠◠ ○○○ ○◠◠ ○◠◠ ◠◠○
88 - 9F	88 - 8F 98 - 9F	○○○ ○◠◠ ○◠◠ ○◠◠ ◠◠○ ◠◠○ ○○○ ○◠◠ ○◠◠ ◠◠○
A0 - B7	A0 - A7 B0 - B7	○○○ ○◠◠ ○◠◠ ○◠◠ ◠◠○ ○◠◠ ○○○ ◠◠○ ○◠◠ ◠◠○
A8 - BF	A8 - AF B8 - BF	○○○ ○◠◠ ◠◠○ ○◠◠ ◠◠○ ◠◠○ ○○○ ◠◠○ ○◠◠ ◠◠○
C0 - D7	C0 - C7 D0 - D7	○○○ ○◠◠ ○◠◠ ◠◠○ ◠◠○ ○◠◠ ○○○ ○◠◠ ◠◠○ ◠◠○
C8 - DF	C8 - CF D8 - DF	○○○ ○◠◠ ○◠◠ ◠◠○ ◠◠○ ◠◠○ ○○○ ○◠◠ ◠◠○ ◠◠○
E0 - F7	E0 - E7 F0 - F7	○○○ ○◠◠ ◠◠○ ◠◠○ ◠◠○ ○◠◠ ○○○ ◠◠○ ◠◠○ ◠◠○
E8 - FF	E8 - EF F8 - FF	○○○ ○◠◠ ◠◠○ ◠◠○ ◠◠○ ◠◠○ ○○○ ◠◠○ ◠◠○ ◠◠○



Note 1: *For multiple channels the indicated jumpers must be plugged identically on each of the address select cards.*

INSTALLATION INSTRUCTIONS (Addressing Supplement)

ADDRESSING FOR 3344 AND 3350 FEATURES

Address Select Card Plugging

With 3344 Attachment feature, the Address Select card must be plugged for "64 Addresses Compare."

With 3350 Attachment feature, refer to the description of 64 Drive Addressing Capability. Use jumper assembly P/N 816645 to connect bits 0-4 on the Address Select Card for the customer's address for the 3830-2. Use INST 16 to determine the proper table for address plugging. Card is located at A-A1Q2. (See logic pages KA103 and 104.)

If 3350 Attachment feature is installed, ensure bits 3 and 4 of the controller's address cards are plugged to answer to bits 3 and 4 of the CU (Control Unit) address.

If Two Channel switch feature is installed, also connect the Channel B address select card jumpers. Read "CAUTION" below. Card is located at A-A1P2. (See logic pages KC103 and 104.)

If Two Channel Switch Additional feature is installed, also connect channel C and D address select card jumpers. Read "CAUTION" below before plugging. Cards are located at A-A1K2 (channel C) and A-A1J2 (channel D). (See logic pages KC103, 104 and KD103, 104.)

CAUTION
If Two Channel Switch, or Two Channel Switch Additional, feature is installed the following rules must be followed or, on some interrupt conditions, incorrect CU addresses will be generated and system errors will result.

1. *If 3 or 4 controllers are attached to the CU, bits 3 and 4 of address compare must float.*
2. *If only 1 or 2 controllers are attached to the CU, bit 3 of address compare must be plugged the same on the Address Select Card of all channels of the CU.*
3. *If only 1 controller is attached to the CU, bits 3 and 4 must be plugged the same on the address compare of the Address Select Card for all channels.*

64 Drive Addressing Capability for 3350 Attachment

With 3350 Attachment feature the 3830-2 CU has 64 Drive Addressing capability. This refers to the number of addresses the CU will answer to, not the physical number of drives attached to the CU (a maximum of 32 drives can be attached to one CU).

The 3350 operates in one of three modes:

Native mode; as a 3350 and requires one logical address per spindle.

3330 Model 11 Compatibility mode; the 3350 operates as one 3330 Model 11 and requires one logical address per spindle.

3330 Model 1 Compatibility mode; the 3350 operates as two 3330 Model 1's and requires two logic addresses per spindle.

These 3 modes can be intermixed on one controller.

When two logical addresses are required by one physical drive, all bits of the two addresses will be the same except bit 2, for example: Address 47 (0100 0111) bit 2 off and address 67 (0110 0111) bit 2 on. Bit 2 on selects one half of the disk storage area, bit 2 off selects the other half. Therefore, to have two addresses for one drive, bit 2 must be left floating on the address compare section of the Address Select card.

Native 3330s, 3340s, 3350s, and 3350s in 3330-11 compatibility mode must be assigned to a primary address.

Address Select Card

The Address Select Card Plugging is shown on Addressing pages INST 16A through INST 16K for all possible combinations of selecting the CU with 3340 or 3350 Attachment Features.

Use INST 16 to select the correct Addressing page and follow the procedure on the selected page to plug the Address Select Card.

64 Address Compare:

The 3344 Attachment Feature requires "64 Addresses Compare". The 3350 Attachment Feature, with 3 or 4 controllers attached to the CU and any 3350 operating in 3330 Model 1 Compatibility mode, also requires "64 Addresses Compare." With other 3350 configurations, use of "64 Addresses Compare" will provide for any future change. However, with some system configurations, 64 addresses may not be available. To provide for this, other addressing options are made available. Use of these options will depend on the number of controllers attached to the CU and the 3350 mode of operation (a 3350 operating in 3330 Model 1 Compatibility mode requires two logical addresses and must have Bit 2 of the CU address floating).

8, 16, or 32 Address Options:

32 Addresses Compare, Bit 2 off; used with up to four controllers, with none of the 3350s operating in 3330 Model 1 Compatability mode.

32 Addresses Compare, Bit 2 on; used with up to four controllers, with none of the 3350s operating in 3330 Model 1 Compatability mode.

32 Addresses Compare, Bit 2 floating; used with up to two controllers, with one or more 3350s operating in 3330 Model 1 Compatability mode.

16 Addresses Compare, Bit 2 off; used with up to two controllers, with none of the 3350s operating in 3330 Model 1 Compatability mode.

16 Addresses Compare, Bit 2 on; used with up to two controllers, with none of the 3350s operating in 3330 Model 1 Compatability mode.

16 Addresses Compare, Bit 2 floating; used with one controller with one or more 3350s operating in 3330 Model 1 Compatability mode.

8 Addresses Compare, Bit 2 off; used with one controller, with none of the 3350s operating in 3330 Model 1 Compatability mode.

8 Addresses Compare, Bit 2 on; used with one controller, with none of the 3350s operating in 3330 Model 1 Compatability mode.

INSTALLATION INSTRUCTIONS (Addressing Supplement)

The 3830-2 detects and interprets only bits 0-4 of the address presented by the channel on bus out. Connect both Address Compare and Address Select.

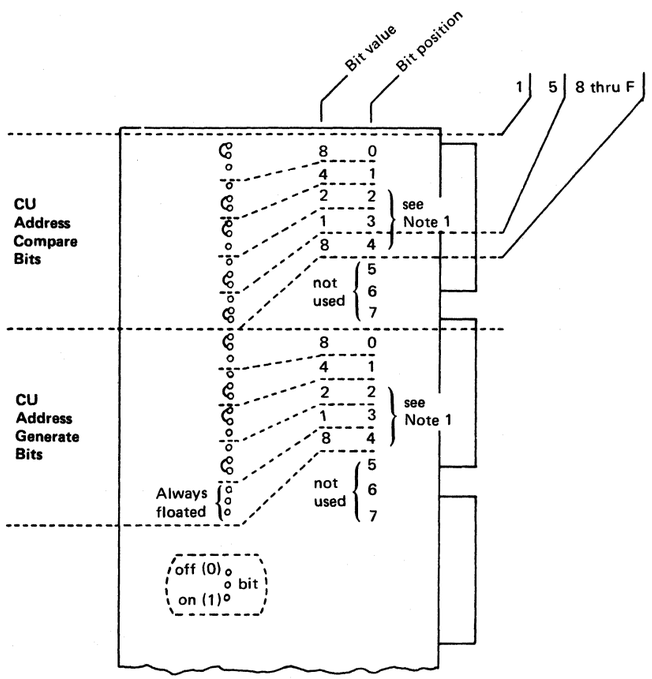
Figure 1 shows the Address Select card plugged for address range 158 through 15F. The Address Select card is located at A-A1Q2. (See logic pages KB103 and 104.)

If Two Channel Switch feature is installed, also connect the channel B address select card jumpers as described above. Card is located at A-A1P2. (See logic pages KB103 and 104.)

If Two Channel Switch, Additional, feature is installed, also connect channels C and D address select card jumpers as described above. Cards are located at A-A1K2 and A-A1J2 respectively. (See logic pages KC103, 104, and KD103, 104.)

Figure 1: Address Select Card

Example: Address select card shown plugged for address range 158 through 15F.



Channel A; A-A1Q2 (KA103, 104)
Channel B: A-A1P2 (KB103, 104)
Channel C: A-A1K2 (KC103, 104)
Channel D: A-A1J2 (KD103, 104)

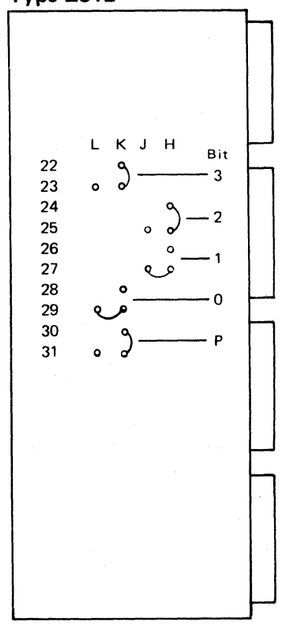
Jumper PN 816645

Notes:

1. *Bits 3 and 4 must be plugged identically for all channel inputs (these bits define attached controllers). If functional microdisk PN 4168811 with any 3350s in 3330-1 compatibility mode is installed, then bits 2, 3, and 4 must be plugged identically for all channel inputs.*
2. *Always plug for the actual storage size regardless of functional disk Part Number (See INTRO 5).*

If 3344 attachment feature is present, check that jumpers on A-B1G2 are plugged correctly. If 3350 attachment feature is present, check that card jumpers on A-B1G2 and A-A1S2 are plugged correctly.

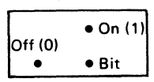
Type Z512



A-B1G2

Bit Definition, Bit 1

Bit 0 On = ECC (3830 P2I) } Refer to
Off = No ECC (Snipe) } INTR 005
Bit 1 On = No 3330-1 Compatability
Off = 3330-1 compatability mode or 3344
Bit 2 On = 8K storage } Note 2
Off = 6K storage
Bit 3 On = Offset Interlock (Jumper on with functional microcode P/N 4168811 only)
Off = No offset Interlock
Bit P = Odd parity for bits 0-3

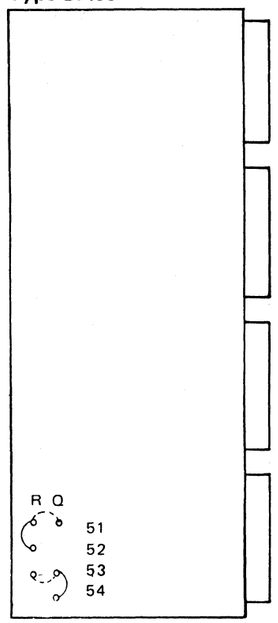


Shown jumpered for:

No E.C.C.
3330-1 Compatability Mode
8K Storage
Offset Interlock

(Jumpers are used by micro-diagnostics and functional code to determine machine configuration.)

Type BA89



A-A1S2

Enable Offset Interlock
(Jumper active with Functional Microcode P/N 4168811 only)

– Q53 to Q54
– R51 to R52

Disable Offset Interlock

– R51 to Q51
– R53 to Q53

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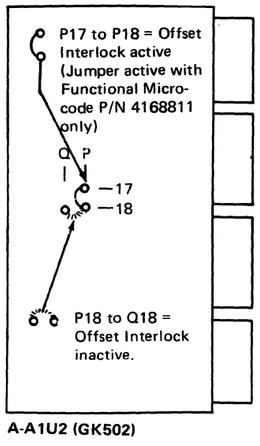
INSTALLATION INSTRUCTIONS (Addressing Supplement)

CHANNEL TRANSFER CONTROL CARD

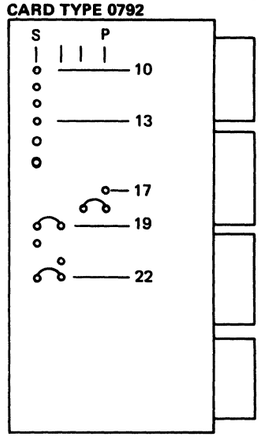
Jumper as shown on card layout for type of card present. Card type BA82 is used with 3350 attachment feature.

CHANNEL TRANSFER CONTROL CARD TYPE BA82



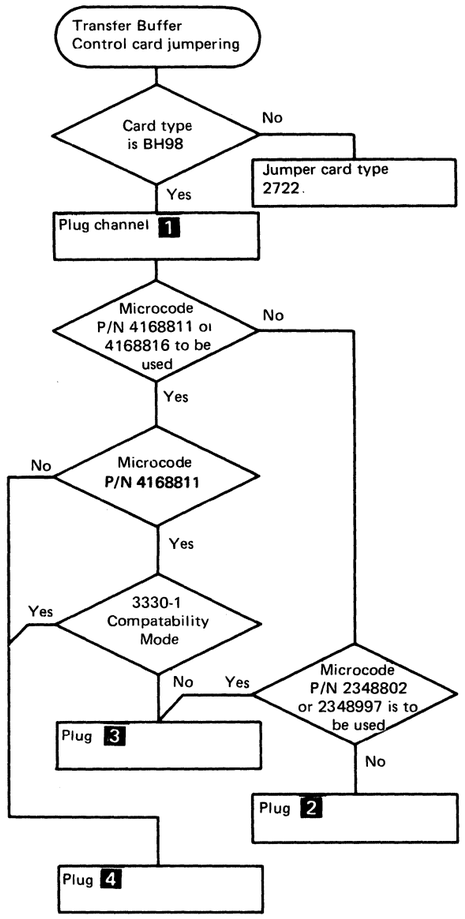
A-A1U2 (GK502)

CHANNEL TRANSFER CONTROL CARD TYPE 0792

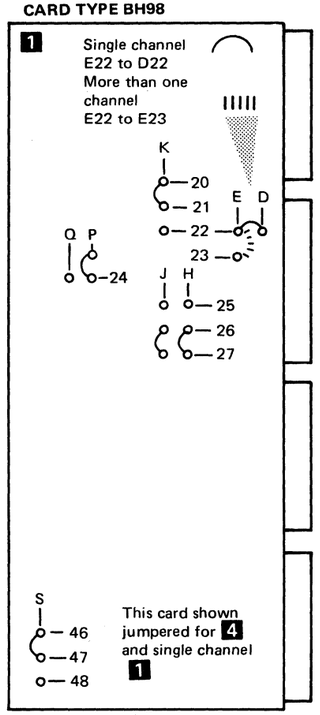


A-A1U2 (GK502)

TRANSFER BUFFER CONTROL CARD

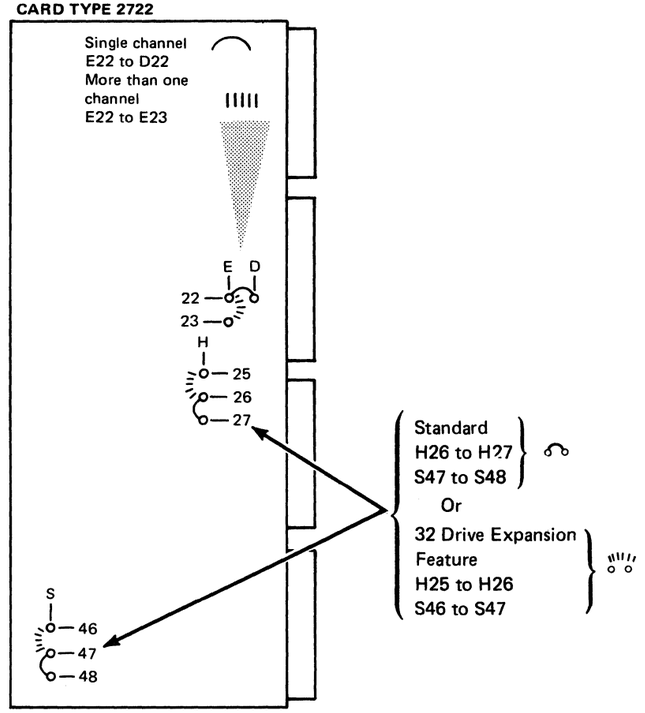


TRANSFER BUFFER CONTROL CARD TYPE BH98



A-A1T2

TRANSFER BUFFER CONTROL CARD TYPE 2722



A-A1T2

Card BH98 Address Plugging	
16 Addresses	
2	H26 to H27 J26 to J27 K21 to K22 S47 to S48 P24 to Q24
32 Addresses	
3	H25 to H26 J26 to J27 K21 to K22 S46 to S47 P24 to Q24
64 Addresses	
4	H26 to H27 J26 to J27 K20 to K21 S46 to S47 P23 to P24

A

Use the primary address range assigned and the Controller address column indicated to determine the controller address assignments. Record this information in Figure 1 to be used in Step 5, INST 26.

B

Use the primary address range assigned and the Controller address column indicated to determine the controller address assignments. Record this information in Figure 1 to be used in Step 5, INST 26.

C

Use the primary address range assigned and the Controller address column indicated to determine the controller address assignments. Record this information in Figure 1 to be used in Step 5, INST 26.

PRIMARY ADDRESS ASSIGNED *See Note 1.*	CONTROLLER ADDRESS ASSIGNMENTS *See Note 1.*	CONTROLLER ADDRESS ASSIGNMENTS *See Note 1.*	CONTROLLER ADDRESS ASSIGNMENTS *See Note 1.*
00-07	0	0	0
08-0F	1	1	1
10-17	0	2	2
18-1F	1	3	3
20-27	0	0	See Note 2.
28-2F	1	1	See Note 2.
30-37	0	2	See Note 2.
38-3F	1	3	See Note 2.
40-47	0	0	0
48-4F	1	1	1
50-57	0	2	2
58-5F	1	3	3
60-67	0	0	See Note 2.
68-6F	1	1	See Note 2.
70-77	0	2	See Note 2.
78-7F	1	3	See Note 2.
80-87	0	0	0
88-8F	1	1	1
90-97	0	2	2
98-9F	1	3	3
A0-A7	0	0	See Note 2.
A8-AF	1	1	See Note 2.
B0-B7	0	2	See Note 2.
B8-BF	1	3	See Note 2.
C0-C7	0	0	0
C8-CF	1	1	1
D0-D7	0	2	2
D8-DF	1	3	3
E0-E7	0	0	See Note 2.
E8-EF	1	1	See Note 2.
F0-F7	0	2	See Note 2.
F8-FF	1	3	See Note 2.

→GO TO INST 25 and Continue.

FIGURE 1

PRIMARY ADDRESSES ASSIGNED	CONTROLLER ADDRESS ASSIGNMENTS

Note 1: *All Channel inputs must be capable of addressing all attached 3333s, 3340 A02s, and 3350 A02/A2Fs, and all associated logical addresses.*

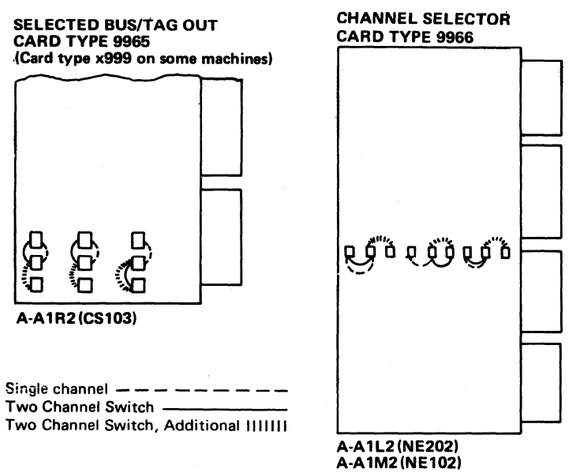
When 3350s are to be operated in 3330-1 compatibility mode, the 3350 operates as two 3330s and requires two logical addresses per spindle, a primary and a secondary. In strings where there are no 3350s operating in 3330-1 mode only primary addresses are used.

Note 2: *No Real Device can be assigned to this address. This is reserved for secondary addresses.*

INSTALLATION INSTRUCTIONS

Check When Complete

___ **7** Check that card jumpers on A-A1L2, A-A1M2, and A-A1R2 match channel options as indicated by the jumper coding shown here.



___ **8** If Two Channel Switch, Additional feature is installed, make sure that violet jumpers are installed from B-A1E6D06 to B-A1E8B04 and from B-A1E6D12 to B-A1B1D09. (See logic page AR101-102).

___ **9** On a two channel switch machine, jumper 01A-A1V2D07 to 01A-A1M2S03 and 01A-A1K2J13 to 01A-M2S04 (NE103) using purple wire. These wires must be removed if two channel switch additional is installed.

___ **10** Verify that the address range (including primary and secondary addresses) does not conflict with other control units on the same channel.

___ **11** If the attached CPU or channel has Block Multiplex feature, be sure that it is activated. Check U.C.W. plugging in the CPU or channel for 3830 addresses. System performance can be seriously degraded if 3830 addresses are plugged for "Share" at CPU or channel. Be aware of all the addresses involved with 64 or 32 drive addresses.

___ **12** If 3344s installed or any 3350 in 3330-1 compatability mode installed review physical planning guide for resulting individual drive addresses.

___ **13** Go to INST 26 next.

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INSTALLATION INSTRUCTIONS

5 CONTROL UNIT MICRODIAGNOSTICS

_____ Insert 3830-2 diagnostic disk in 23FD and perform step A on START 25, and step B on START 27. Verify controller address assignments by checking the controller plugging (Use the controller INST section and the information recorded in Figure 1 on INST 18 of this section).

CAUTION: *Verify that proper 3830-2 diagnostic disk is supplied for your machine configuration. See INTR 005.*

6 SYSTEM TEST

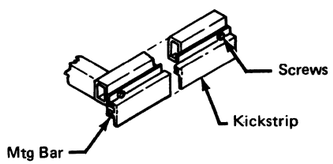
_____**1** Connect channel Bus and Tag cables between channel and 3830-2

_____**2** Run online test 3830AAA from the CPU. Refer to step C on START 27.

7 COVER INSTALLATION

_____**1** Mount kickstrips. Light tapping with a hammer may be required to properly seat them.

Note: If installation is on a non-raised floor do not attempt to mount kickstrip (P/N2277387) on right end of 3830-2.



_____**2** Re-install covers removed in step **1**.

8 RECORDS

_____**1** Assist customer with his checkout of the facility.

_____**2** Complete all installation records.

_____**3** Retain these installation procedures in the Maintenance Library for future reference.

INDEX

CHANNEL INTERFACE (cont'd)–CP15 OR 18 INDEX 2

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