



Maintenance Library

3705

**Communications Controller
Theory—Maintenance
Volume III**

SY27-0107-6



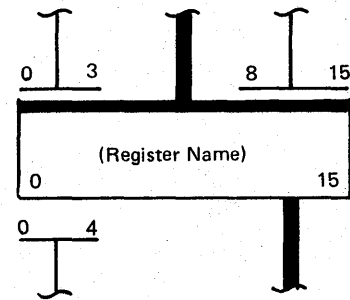
ABBREVIATIONS

A	And circuit or ampere	ck	check	ESC	emulation subchannel	L2	level 2
AA	automatic answering	clk	clock	EXT	external	L3	level 3
ABAR	attachment buffer address register	cm	centimeter	FCS	final control sequence	L4	level 4
ABO	adapter bus out (register)	CMDR	channel adapter command register	FET	field effect transistor modem card	L5	level 5
ac	alternating current	CMND	command	FETOM	Field Engineering Theory of Operation Manual	mA	milliampere
ACO	automatic call originate	com	common	FF	flip flop	Mem TB	memory terminal board
ACF/NCP/VS	Advanced Communications Function for Network Control Program/Virtual Storage	COS	Call Originate Status	FL	flip latch	modem	modulator/demodulator
ACR	abandon call and retry	CP	circuit protector	FRU	field replaceable unit	ms/divn	milliseconds per division
ACU	automatic calling unit	CPU	central processing unit	GB	ground bus	MST	monolithic system technology
adr	address	CR	compare register (instruction)	gnd	ground	mV	millivolt
AEQ	automatic equalizer	CRC	cyclic redundancy check	hex	hexadecimal	NB	Digit Signal
AHR	add halfword register (instruction)	CR1	compare register immediate (instruction)	Hlfwd	halfword	N/C	normally closed
ALD	automated logic diagram	CRQ	Call Request	horz	horizontal	NCP	network control program
ALU	arithmetic logic unit	CS	cycle steal	HS	heat sink	NCR	and character register (instruction)
AMP	amplifier	CSAR	cycle steal address register	Hz	Hertz	NHR	and halfword register (instruction)
APAR	authorized program analysis report	CSB	communication scanner	I	instruction (cycle)	N/O	normally open
AR	add register (instruction)	CSCD	clear to send, carrier detect	IAR	instruction address register	NR	and register (instruction)
ARI	add register immediate (instruction)	CSMC	cycle steal message counter	IC	insert character (instruction)	NR1	and register immediate (instruction)
B	branch (instruction)	ctrl	control	ICS	initial control sequence	NRZI	non-return-to-zero inverted
BAL	branch and link (instruction)	CTS	Clear To Send	ICT	insert character and count (instruction)	ns	nanoseconds
BALR	branch and link register (instruction)	CUCR	Cycle Utilization Counter Register	ICW	interface control word	NSC	native subchannel
BAR	buffer address register	CUE	Control Unit End (status)	IFT	internal functional test	OBR	outboard recorder
BB	branch on bit (instruction)	CW	control word	IN	input (instruction)	O/C	overcurrent
BC	bit clock	CWAR	control word address register	INCWAR	inbound control word address register	OCR	or character register (instruction)
BCB	bit control block	DAA	data access arrangement	Init	initial	OE	exclusive or
BCC	bit clock control	DA	data modem ready	int	internal	OH	off hook (modem)
BCL	branch on C latch (instruction)	dB	decibel	intf	interface	OHR	or halfword register (instruction)
BCT	branch on count (instruction)	DBAR	diagnostic buffer address register	I/O	input/output	OLT	on line test
BO	bus out	dc	direct current	IPL	initial program load	OLTEP	on line test executive program
BP	break point	DCE	data circuit-terminating equipment	IR	interrupt remember	OLTLIB	on line test library
bps	bit per second	DCM	diagnostic control module	ISACR	initial selection address and command register	OLTSEP	on line test standalone executive program
BSC	binary synchronous communication	DCR	data channel ready	L	load (instruction)	op	operation
BSM	bridge storage module	DE	Device End (status)	LA	load address (instruction)	op reg	operation register
BZL	branch on Z latch (instruction)	DET	detector	LAR	lagging address register	OR	or register (instruction)
CA	channel adapter	diag	diagnostic	LCD	line code definer	ORI	or register immediate (instruction)
CACHKR	channel adapter check register	dist	distance	LCOR	load character with offset register (instruction)	OS	Operating System
CACR	channel adapter control register	DLO	data line occupied	LCR	load character register (instruction)	OSC	oscillator
CADB	channel adapter data buffer	DOS	Disk Operating System	LED	light emitting diode	OUT	output (instruction)
CAMR	channel adapter mode register	DPR	digit present	LGF	leading graphics flag	OUTCWAR	outbound control word address register
CASNSR	channel adapter sense register	DR	display register or data ring (modem)	LH	load halfword (instruction)	OVRN	overrun
CASTR	channel adapter status register	DCS	distant station connect (ACO only)	LHOR	load halfword with offset register (instruction)	O/V	overvoltage
CB	circuit breaker	DSR	data set ready	LHR	load halfword register (instruction)	P	parity
CBAR	CSB buffer address register	DT	data tip (modem)	LIB	line interface base	PC	parity check
CCB	character control block	DTE	data terminal equipment	lim	limiter	PCF	primary control field
CCR	compare character register (instruction)	DTR	data terminal ready	LOR	load with offset register (instruction)	PCI	program controlled interrupt
CCT	coupler cut through (modem)	EC	edge connector	LOSC	last oscillator sample condition	PDF	parallel data field
CCU	central control unit	EB	extended buffer	LR	load register (instruction)	PEP	partitioned emulation programming
CD	carrier detect	ECP	emulation control program	LRI	load register immediate (instruction)	PG	parity generation
CDS	configuration data set	EIA	Electronic Industries Association	LS or ls	local store	pgm	program
CE	Channel End (status)	enbl	enable	lt	latch	PH	polarity hold
chan	channel	EON	end of number (ACO only)	L1	level 1	PND	Present Next Digit
char	character	EPO	emergency power off			P/N	part number
CHR	compare halfword register (instruction)					POR	power on reset position

POSC	present oscillator sample condition	stk	stacked
pot	potentiometer	svc	service
P-P	post processor modem card	sw	switch
PPB	prime power box	SYN	synchronous idle
PUT	programmable unijunction transistor	sync	synchronization or synchronous
PWI	power indicator	TAR	temporary address register
R	resistance or resistor	TB	terminal board
rcv	receive	TIC	Transfer In Channel
rd	read	tr	trigger
rdy	ready	TRM	test register under mask (instruction)
RE	register and external register (instructions)	TSL	Technical Service Letter
ref	reference	T2	test 2
reg	register	T3	test 3
regen	regenerative	T4	test 4
req	request	UC	Unit Check (status)
RI	register immediate (instruction) or ring indicator (modem)	UE	Unit Exception (status)
RLSD	receive line signal detector	V	volts
RMS	root mean square	V/divn	volts per division
ROS	read-only storage	wd	word
RPL	remote program loader	wr	write
RR	register to register (instructions)	XCR	exclusive-or character register (instruction)
RS	register to storage (instructions)	xfer	transfer
RSA	register and storage with addition (instructions)	xfmr	transformer
RT	register branch or register and branch (instructions)	XHR	exclusive-or halfword register (instruction)
RTS	Request To Send	xmt	transmit
rly	relay	XR	exclusive-or register (instruction)
SAR	storage address register	XRI	exclusive-or register immediate (instruction)
SCF	secondary control field	2W	two-wire line connection (implies half-duplex)
SCR	silicon controlled rectifier or subtract character register (instruction)	4W	four-wire line connection (implies duplex, but actual duplex depends on the line set type and telephone company equipment.
SCRID	silicon controlled rectifier indicator driver		
SDF	serial data field		
SDLC	synchronous data link control		
SDR	storage data register		
sec	second		
sel	selection		
SEP	separator (ACO only)		
seq	sequence		
SG	signal ground		
SH	switch hook (modem)		
SHR	subtract halfword register (instruction)		
SIG	signal		
SIO	start I/O		
SMS	standard modular system		
SR	subtract register (instruction)		
SRI	subtract register immediate (instruction)		
SRL	Systems Reference Library		
S/S	start/stop		
ST	store (instruction)		
STC	store character (instruction)		
STCT	store character and count (instruction)		
STH	store halfword (instruction)		

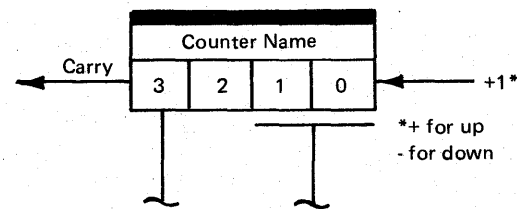
LEGEND

1. Logic Diagrams

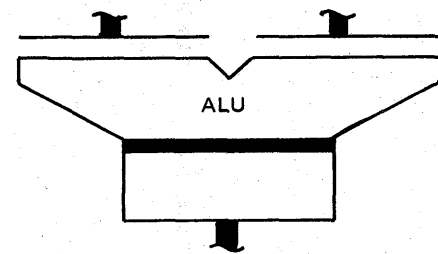


Register

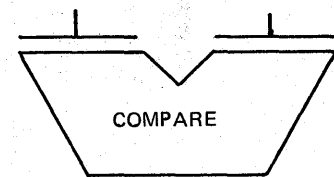
The input side is denoted by a thick line. A partial transfer of contents is shown by numbered input and/or output lines.



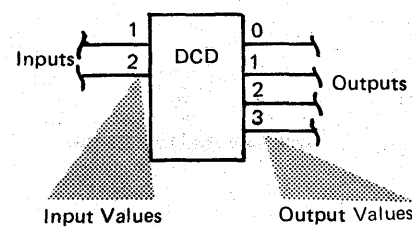
Counter



ALU

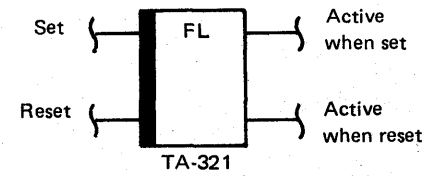


Compare



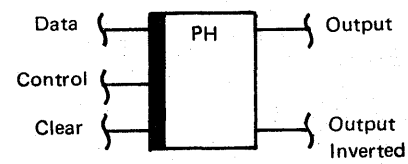
Decode

The active output is the output whose output value equals the sum of the active input values.



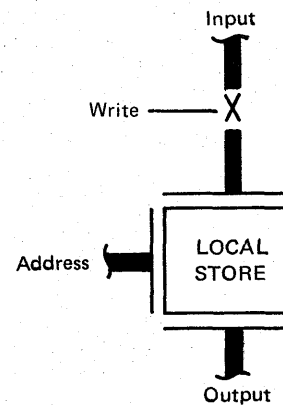
Flip Latch

Input side is denoted by a thick line. ALD reference page may be shown beneath.



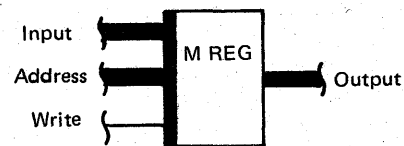
Polarity Hold

The 'output' of the polarity hold block is at the indicated polarity when both the 'data' and the 'control' lines go to their indicated polarity. When the 'control' line goes to the polarity opposite to that indicated, the 'output' line holds at the polarity it is at. When the 'clear' line goes to its indicated polarity, the 'output' line goes to the polarity opposite to that indicated.



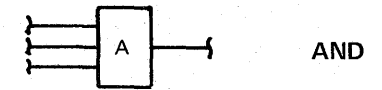
Local Store

Read---Output from the local store addressed. Contents of local store is not destroyed. Write---Input contents stored in the local store addressed when 'write' is active.

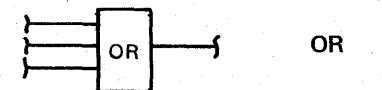


M REG

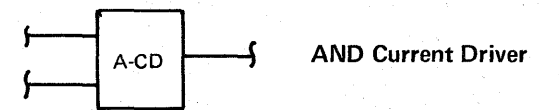
See Local Store



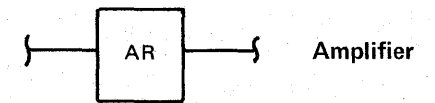
AND



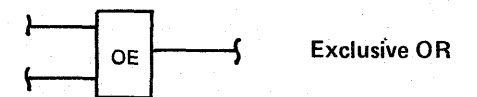
OR



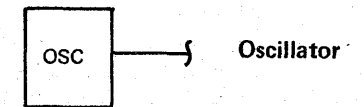
AND Current Driver



Amplifier



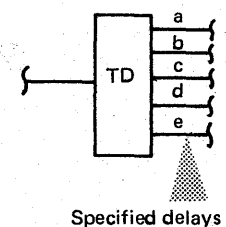
Exclusive OR



Oscillator



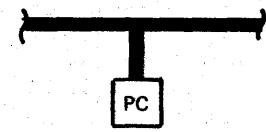
Negator (Inverter)



Time Delay

An input pulse starts the time delay. Each output pulse has the same duration as the input pulse but is delayed by the specified amount.

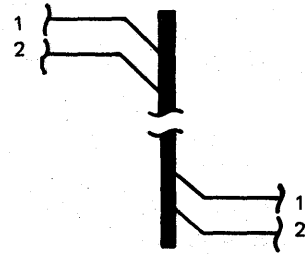
LEGEND (PART 2)



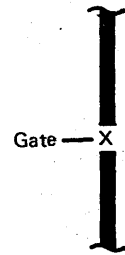
Parity Check
Parity check on the data bus



Parity Generate
Parity generated on the data bus



Multiple Line Transfer



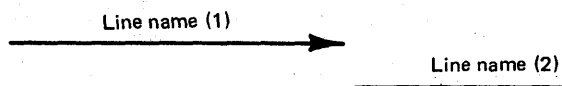
Gated Bus
Gate must be active for data to flow on bus.



Test Point



Signal that may be scoped.



Above symbol indicates change in line name.

2. Flowcharts



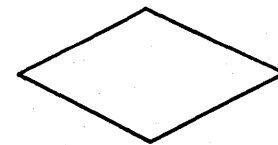
Terminal
Indicates the beginning or end of the event.



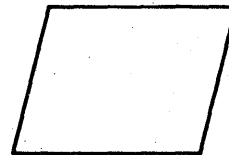
Process
Indicates a major function or event.



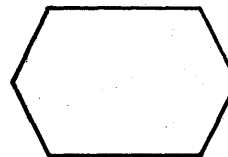
Annotation
Gives descriptive comment or explanatory note.



Decision
Indicates a point in a flowchart where a branch to an alternate path is possible.



Input-Output
CCU executes the control program input/output instructions.

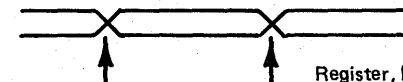


Hardware Process
Type 2 scanner hardware action resulting from input/output instructions or signals from the line/autocall interface.

3. Timing Charts

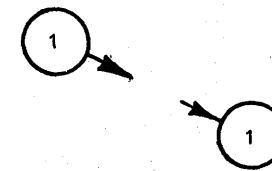


Numerals at the beginning and end of the bar identify the signal(s) (also on the same chart) that activate and deactivate this line. '(Not)' with the number indicates that lack of the signal conditions the line.



Register, bus, or local store content changes value at these points.

4. General



On-page Connector

Indicates a connection between two parts of the same page. The arrow leaving the symbol points (line-of-sight) to a correspondingly-numbered symbol.



Off-page Connector

Indicates a connection between diagrams located on separate pages. The location of the correspondingly-lettered symbol is shown adjacent the symbol.

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2A	CW—CZ	ROS-Type 2 attachment base—CCU
3	DF—DZ	CCU
4	RA—RS	Type 1 scanner and channel adapter
A04	PA—PS	Type 4 channel adapter
5	QA—QR	Type 2 channel adapter
A05	SA—SR	Type 3 channel adapter
6	TA—TB	Type 2 scanner
7	VA	Type 1 LIB—reference material
8	VB	Type 1 LIB—line sets 1A,1B,1C,1D,1E,1F,1G, 1GA, 1H, 1J, 1K, 1N, 1S, 1T, 1TA, 1U, 1W, 1Z
9	VC—VD	Type 2 LIB—line set 2A
10	VE—VF	Type 3 LIB—line sets 3A, 3B
11	VG—VH	Type 4 LIB—line sets 4A, 4B, 4C
12	VJ	Type 5 LIB—line sets 5A, 5B
13	VL	Type 6 LIB—line set 6A
14	VN	Type 7 LIB
15	VO	Type 8 LIB—line sets 8A, 8B
16	VS	Type 9 LIB—line set 9A
17	GA—GC	Remote Program Loader Diskette Controller
18	VU	Type 10 LIB—line set 10A
19	VW	Type 11 LIB—line sets 11A, 11B
20	VX	Type 12 LIB—line sets 12A, 12B
21	MM	FET storage (3705-II)
22	TD—TE	Type 3 or 3HS scanner
23	TF	Type 3 or 3HS scanner
24	TA—TB	Type 2 scanner (3705-II)

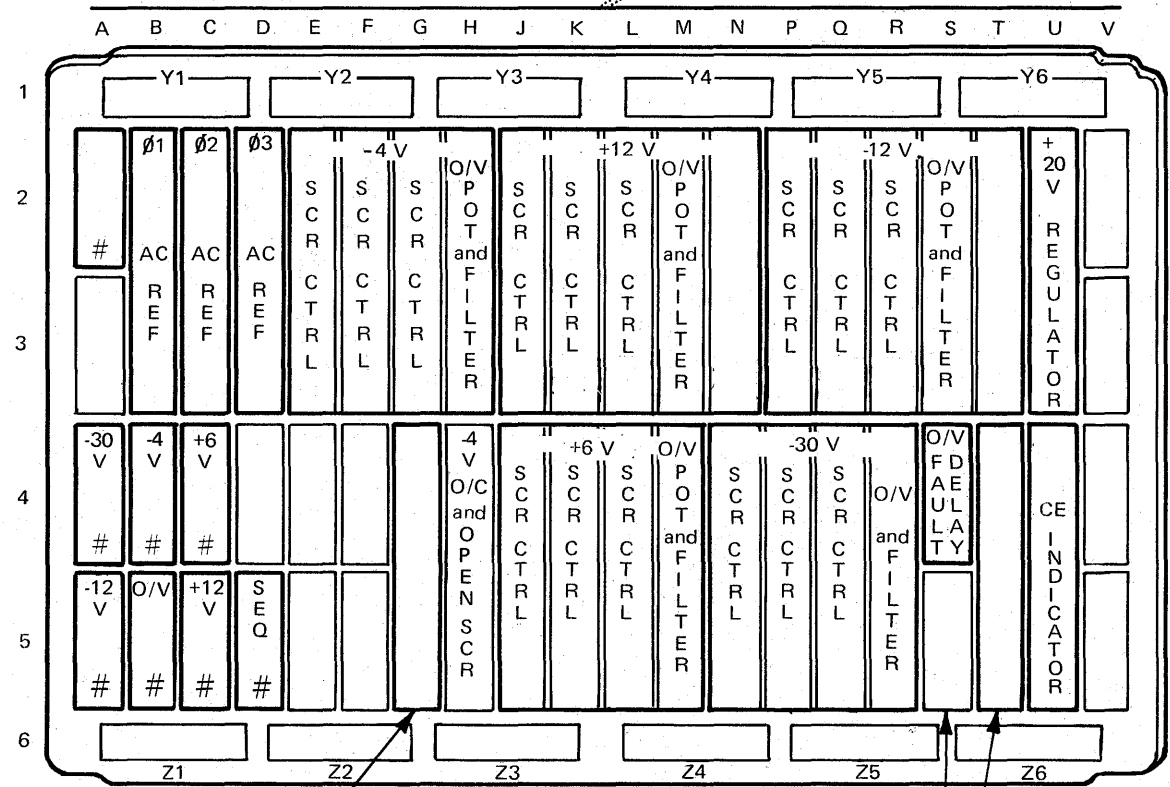
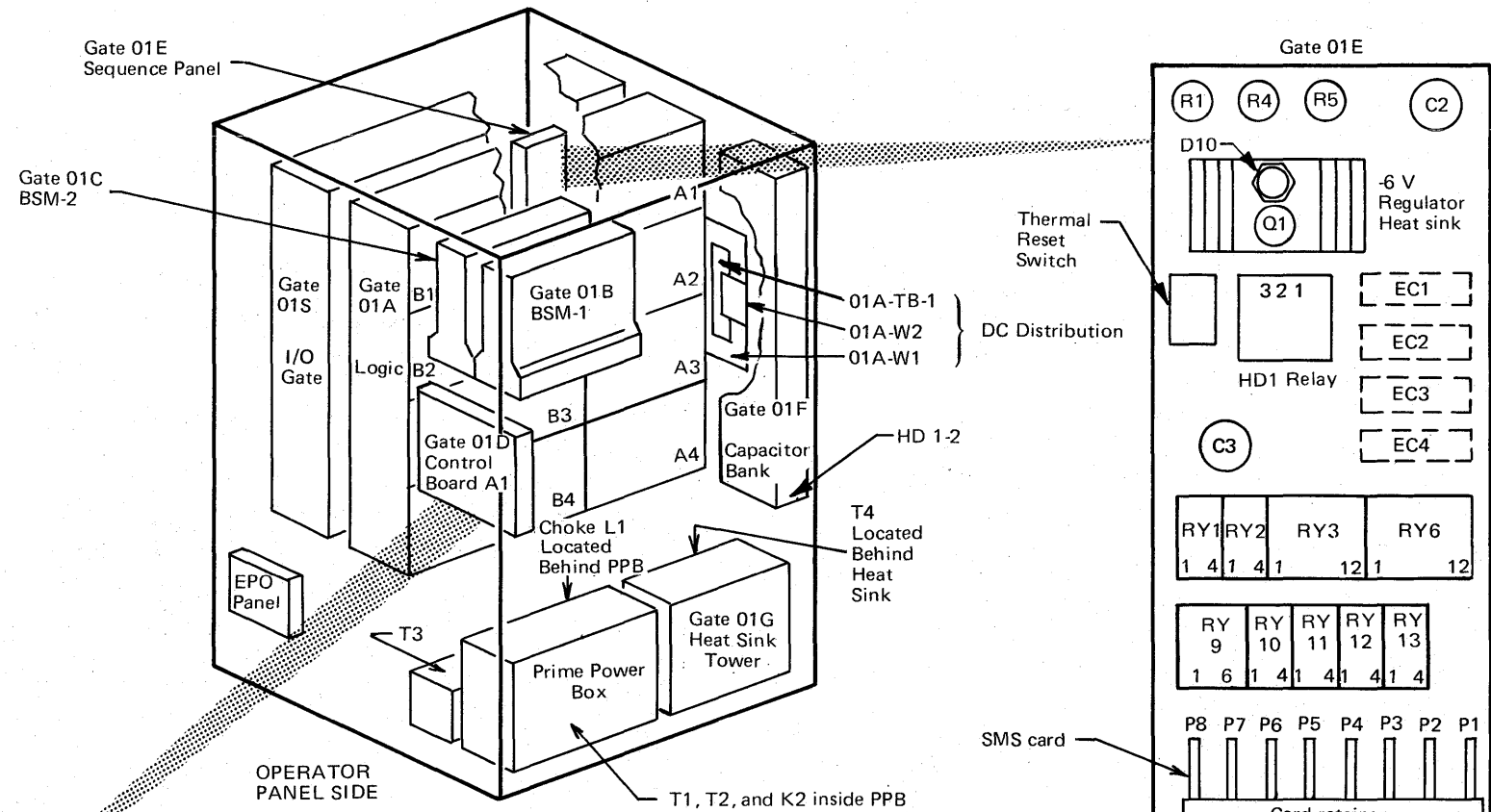
3705-I POWER SUPPLY

COMPONENT LOCATIONS

- See D-300 through D-450 for a 3705-II with more than three cards in the OXD power control gate.
- D-150 through D-240 are used for the 3705-I and a 3705-II with more than three cards in the OXD power control gate. (See D-500 through D-590 for a 3705-II with only two or three cards in the OXD power control gate.)
- The expansion frame physical locations are identical except there is no EPO panel nor sequence panel (gate 01E).
- Refer to the following chart for the component layouts of other units.
- Power MAPs for all 3705-IIs begin on page D-600.

Unit	Layout reference
Prime power box	YZ301 sheet 2-3
Heat sink tower (01G)	YZ301 sheet 4-5
Capacitor bank (01F)	YZ301 sheet 6
EPO panel	YZ301 sheet 11
BSM-1&2 (01B&C)	YZ301 sheet 7
I/O Gate (01S)	YZ301 sheet 9

- Expansion frame control board (OXD-A1) does not have a card at the T4 position.



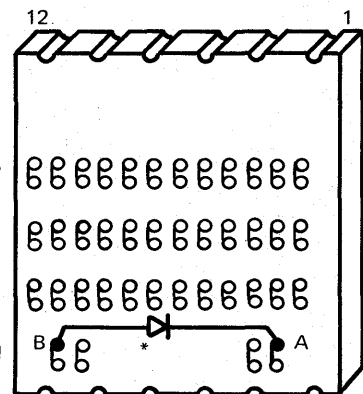
O/V - over voltage
O/C - over current

01D-A1 CONTROL BOARD
indicates cable
Power Sequence and Under Voltage Detect
CARD SIDE
-30 V Pot and Temperature Tracking
Meter and Indicator Driver

SMS card P8 plugs into the sequence panel connector labeled J8

Diode #	01E location
D1	RY6 - 'A' to 'B'*
D2	EC2 - a to e*
D3	RY2 - 'A' to 'B'*
D4	EC2 - b to e*
D5	RY12 - 'A' to 'B'*
D6	RY11 - 'A' to 'B'*
D7	RY10 - 'A' to 'B'*
D8	RY9 - 'A' to 'B'*
D9	EC2 - f to c*

* indicates anode (+) side of diode.



12 position Wire Contact Relay Base (wiring side)

SEQUENCE PANEL (Relay side of panel)
Power Control Cable Plug
P1 - 3705
P2 - 1st expansion frame
P3 - 2nd expansion frame
P4 - 3rd expansion frame

3705-I FAULT INDICATORS

Service Note: If an undervoltage LED is on but the power will not remain on to scope the associated SCRs, the voltage sequence can be made to hang up by removing the filter card for the next voltage to sequence on. For example: to scope the +6 V SCRs, remove the -30 V filter card.

Power on voltage sequence:

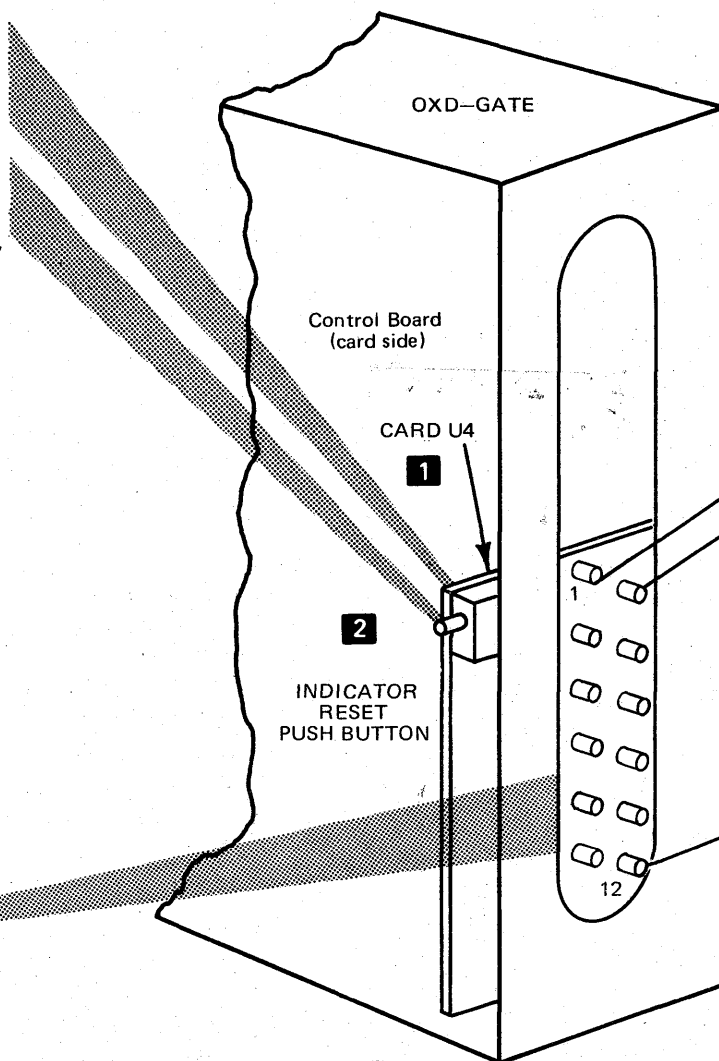
1. ± 12 V, -4 V
2. +6 V
3. -30 V

To scope the -30 V SCRs, prevent OIE-RY12-3 N/O from making by removing the contact wire from the relay.

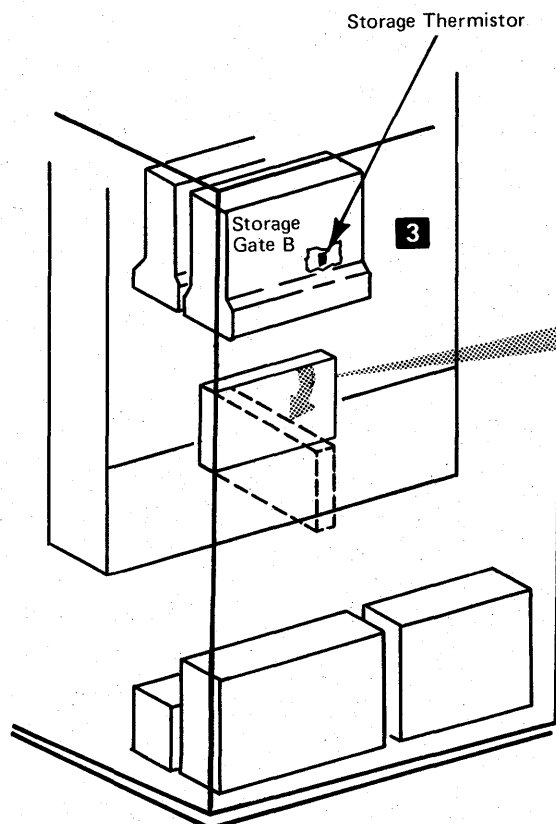
1 There are 12 light-emitting diodes (LEDs) on one card located on the control board at 01D-A1U4. When on, these LEDs indicate the following fault conditions:
 Overvoltage on any logic voltage
 Overcurrent on the -4 V supply
 One or more open SCR in the -4 V supply
 Undervoltage on any logic voltage

2 Once a LED is on, it stays on even if power drops. To turn the LED (s) off, press the Indicator Reset button located on the U4 card.

- The indicators will not turn on during 'power on reset' or while the Power Off push button is pressed. Consequently, the LEDs will not assist you with a power-on sequence problem.
- All fault indications that cause power down turn on the 'power check' light.



LED #	Fault Indication	Causes Power Down	Duration Of Fault Before Power Down	Level at which sense relays pick, LED turns on, under-voltage causes power down	Action To Be Taken If Respective LED Is On
1	+6 V Overvoltage	Yes	200 ms	+6.6 V	Follow procedure for checking SCRs in ± 12 V, +6 V, -30 V supplies on D-150
2	+12 V Overvoltage	Yes	200 ms	+14 V	
3	-12 V Overvoltage	Yes	200 ms	-14 V	
4	-30 V Overvoltage	Yes	200 ms	-37 V	
5	-4 V Overvoltage	Yes	200 ms	-4.7 V	Follow procedure for checking SCRs in -4 V supply on D-170
6	-4 V SCR (s) Open	No	—	LED Turns On	
7	-4 V Overcurrent	Yes	Immediate	180 to 200 Ampere	Follow procedure for checking SCRs in ± 12 V, +6 V, -30 V supplies on D-150
8	-4 V Undervoltage	Yes	Immediate	-3.0 V to -3.5 V	
9	+6 V Undervoltage	Yes	Immediate	+5.4 V to +5.59 V	
10	+12 V Undervoltage	Yes	Immediate	+9.0 V to +10.0 V	
11	-12 V Undervoltage	Yes	Immediate	-8.7 V to -10.3 V	Follow procedure for checking SCRs in ± 12 V, +6 V, -30 V supplies on D-150
12	-30 V Undervoltage	Yes	Immediate	-7.0 V to -10.0 V	

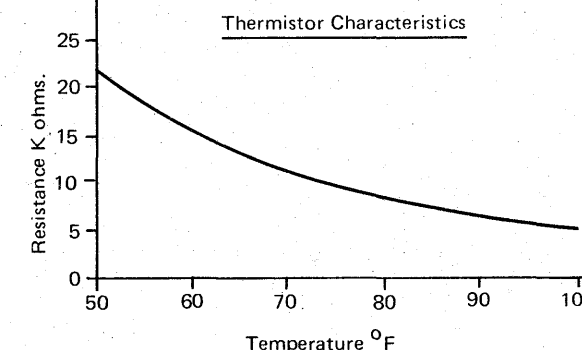


LED #12 (-30 V undervoltage) may be turned on as a result of a defective storage thermistor.

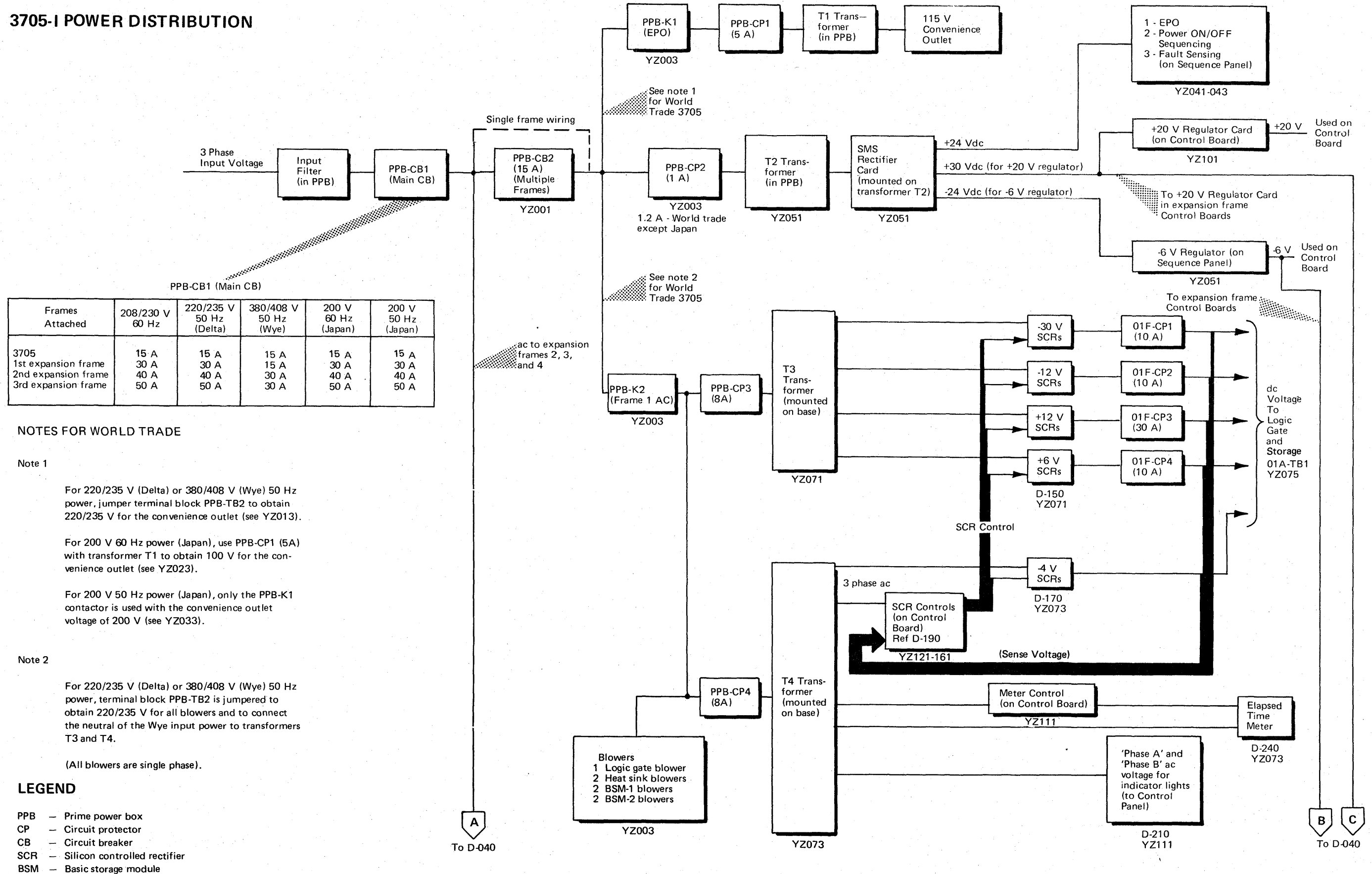
The thermistor is located in gate B below the core array. An unused thermistor is located in gate C.

- 3** To check a thermistor:
1. Pull the -30 V temperature tracking card from the S5 position of the associated control board.
 2. Use an ohmmeter to measure the thermistor resistance between 0XD-A1S5B13 and D13.
 3. The characteristics of the thermistor are shown in the attached graph. The temperature can be assumed to be 10° F higher than the air temperature outside the 3705 covers. Replace thermistors that have resistance readings outside a $\pm 30\%$ range at the operating temperature.
 4. Insert the card removed from the S5 position.

4 LED No. 6 may turn on if the -4 volt supply is adjusted beyond its normal range, or if the machine has undergone a severe power-line disturbance.



3705-I POWER DISTRIBUTION



PPB-CB1 (Main CB)

Frames Attached	208/230 V 60 Hz	220/235 V 50 Hz (Delta)	380/408 V 50 Hz (Wye)	200 V 60 Hz (Japan)	200 V 50 Hz (Japan)
3705	15 A	15 A	15 A	15 A	15 A
1st expansion frame	30 A	30 A	15 A	30 A	30 A
2nd expansion frame	40 A	40 A	30 A	40 A	40 A
3rd expansion frame	50 A	50 A	30 A	50 A	50 A

NOTES FOR WORLD TRADE

Note 1

For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, jumper terminal block PPB-TB2 to obtain 220/235 V for the convenience outlet (see YZ013).

For 200 V 60 Hz power (Japan), use PPB-CP1 (5A) with transformer T1 to obtain 100 V for the convenience outlet (see YZ023).

For 200 V 50 Hz power (Japan), only the PPB-K1 contactor is used with the convenience outlet voltage of 200 V (see YZ033).

Note 2

For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, terminal block PPB-TB2 is jumpered to obtain 220/235 V for all blowers and to connect the neutral of the Wye input power to transformers T3 and T4.

(All blowers are single phase).

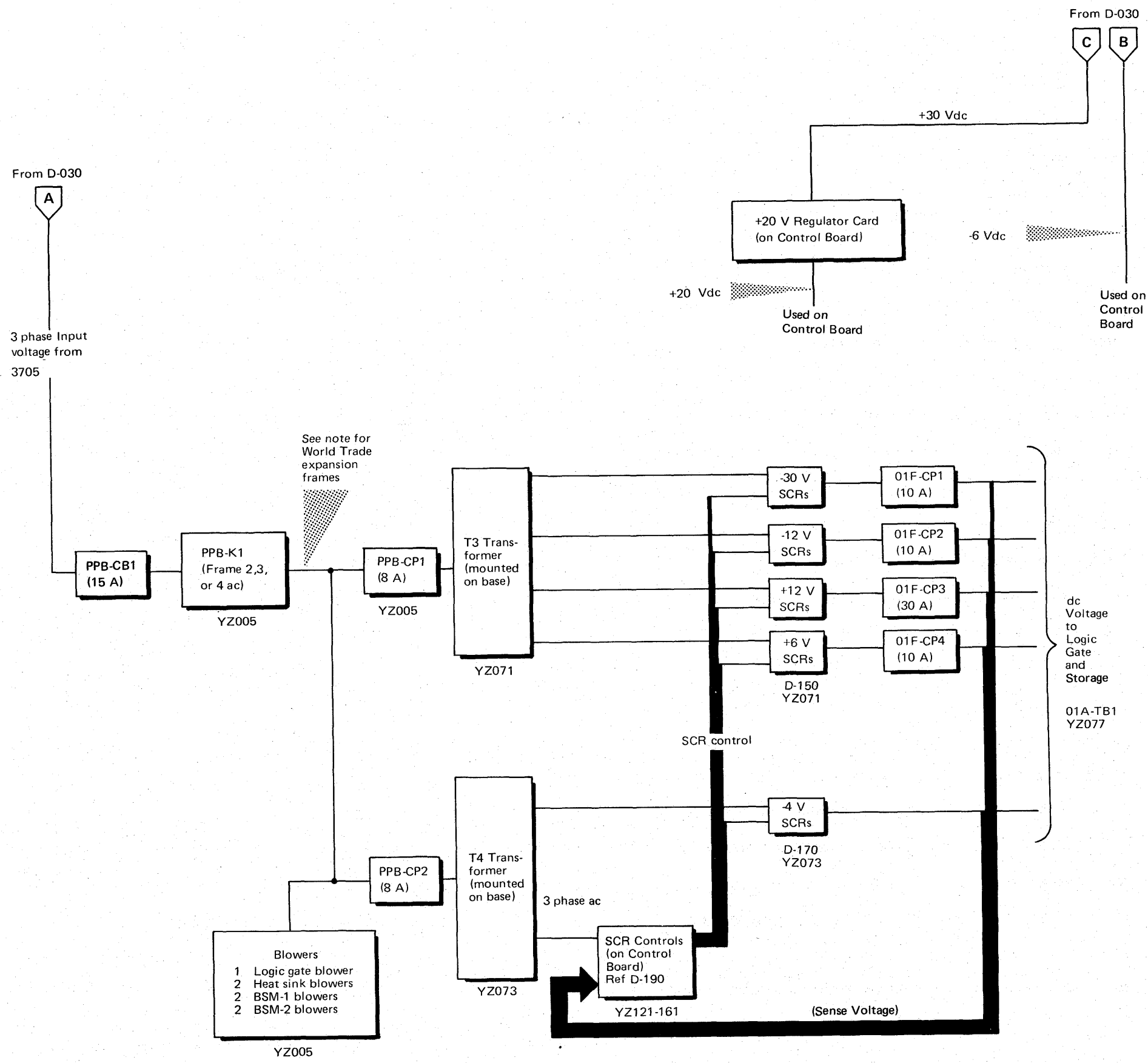
LEGEND

- PPB — Prime power box
- CP — Circuit protector
- CB — Circuit breaker
- SCR — Silicon controlled rectifier
- BSM — Basic storage module

3705-I EXPANSION FRAME POWER DISTRIBUTION

NOTE FOR WORLD TRADE

- 220/235 V (Delta) or 380/408 V (Wye) 3 phase 50 Hz expansion frames are jumpered to obtain 220/235 V for all blowers and to connect the neutral of the Wye input power to transformers T3 and T4. See YZ015.



3705-I POWER-ON SEQUENCE

- Shows the sequence of events that occur during normal power-on operation (1) when the Local/Remote Power switch is set to the LOCAL position, and the Power On switch is depressed, or (2) when the Local/Remote Power switch is set to the REMOTE position, and the host CPU brings power up.

1 The 4 second delays are located on P8 on the Sequence Panel gate 01E.

Contact or action causing pickup	Power Supply Components or Action	Timing Relationships
EPO-J (1, 2, 3, or 4)	YZ051 PPB-K1 (EPO)	(+24 Vdc For Relays) D-120
PPB-K1 #1 point	YZ051 01E-RY9 (Remote)	Remote position of Local/Remote Power Switch
Press Power On Switch	YZ053 Power On switch or CPU Power On	Local position of Local/Remote Power Switch
Local Power On Switch or CPU Power On	YZ053 01E-RY6 (Power On)	
01E-RY6-9	YZ053 Power Check Light	
01E-RY6-12 N/O	YZ054 Power On Reset	
01E-RY6-2	YZ055 01E-RY13 (Power Off Override)	
01E-RY6-11	YZ055 01E-HD1 (ac contactors on)	D-090
01E-HD1-1	YZ052 PPB-K2 (ac to 3705)	
PPB-K2 #4 point (3705)	YZ052 PPB-K1 (ac to Expansion frame #1)	
PPB-K1 #4 point (Expansion frame 1)	YZ052 PPB-K1 (ac to Expansion frame #2)	
PPB-K1 #4 point (Expansion frame 2)	YZ052 PPB-K1 (ac to Expansion frame #3)	
ac applied to each frame	YZ005 +12 V, -12 V, -4 V (every frame)	
+12 V, -12 V, -4 V up in each frame	YZ101 +12 V, -12 V, -4 V sense relays	
Transistor that picks +12 V, -12 V, -4 V sense relay	YZ101 Ground for +6 V sequence	+20 V approx. +1 V (approx.)
+12 V, -12 V, -4 V sense relay points in each frame	YZ056 01E-RY1 (+12 V, -12 V, -4 V up)	1 → 4 sec. delay ← D-080
01E-RY1-4	YZ055 0XF-HD1 (Turn on +6 V)	
0XF-HD1-(1&2)	YZ071 +6 volts (all frames)	
+6V up in each frame	YZ101 +6 V sense relays	
Transistor that picks +6 V sense relay	YZ101 Ground for -30 V sequence	+20 V approx. +1 V (approx.)
+6 V sense relay points in each frame	YZ056 01E-RY2 (+6 V up)	D-070
01E-RY2-3	YZ055 0XF-HD2 (Turn on -30 V)	
0XF-HD2-(1, 2, 3)	YZ071 -30 volts (all frames)	
-30 V up in each frame	YZ101 -30 V sense relays	
RY3-1 N/C	YZ054 Power-On Reset Controlled	+24 Vdc (Blocks Power Fault Indicators) Ground
-30 V sense relay points in each frame	YZ056 01E-RY12 (-30 V up)	
01E-RY12-3	YZ053 01E-RY3 (Sequence complete)	1 → 4 sec. delay ← D-060
01E-RY3-10 N/O	YZ053 Power ON Light	

3705-I MAINTENANCE CHARTS AND PROCEDURES

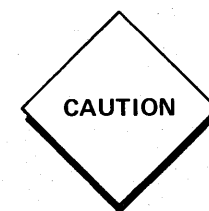
POWER ON SEQUENCE

- This procedure is based on the fact that a failure results in the power-on sequence hanging at the failure point.
- A procedure to isolate the failing frame for power-on problems on multiframe machines is within area outlined.
- Check lists used in this flowchart are not all inclusive, but assist you in locating the problem more readily. Following the check list is a logic page reference for your use when the check list does not pin point the problem.

Notes:

1. +24 Vdc can be +20 V to +35 V depending on loading and input line voltage.
2. -24 Vdc can be -20 V to -35 V depending on loading and input line voltage.
3. +30 Vdc can be +25 V to +40 V depending on loading and input line voltage.
4. Verify that all CPU interfaces are disabled to avoid channel errors when powering down.

SAFETY - Observe normal safety practices when servicing this power supply.

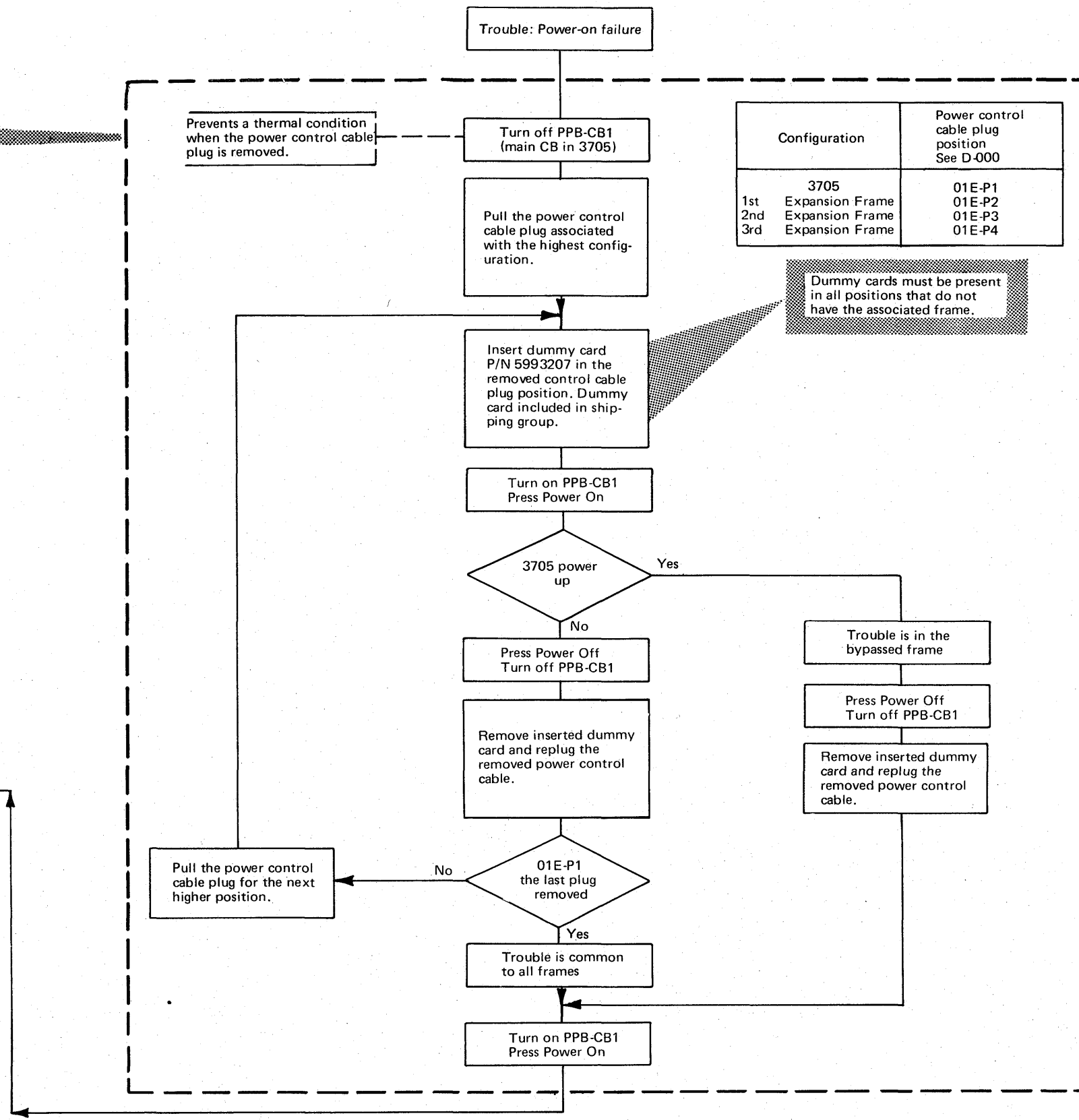
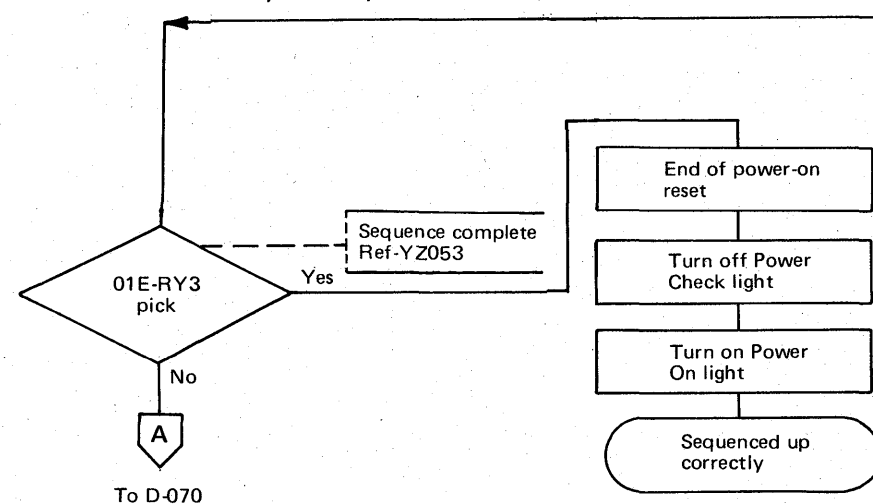


Power must be off in the 3705 whenever a card is to be substituted or replaced.

Connect the I/O interface cables to bypass the 3705 when you are working on a power supply voltage sequence problem. The 3705 relies on power sequencing during power on and off to prevent the drivers and receivers from generating noise on the channel interface signal lines.

INTERPRETATION OF DECISION BLOCK PATHS

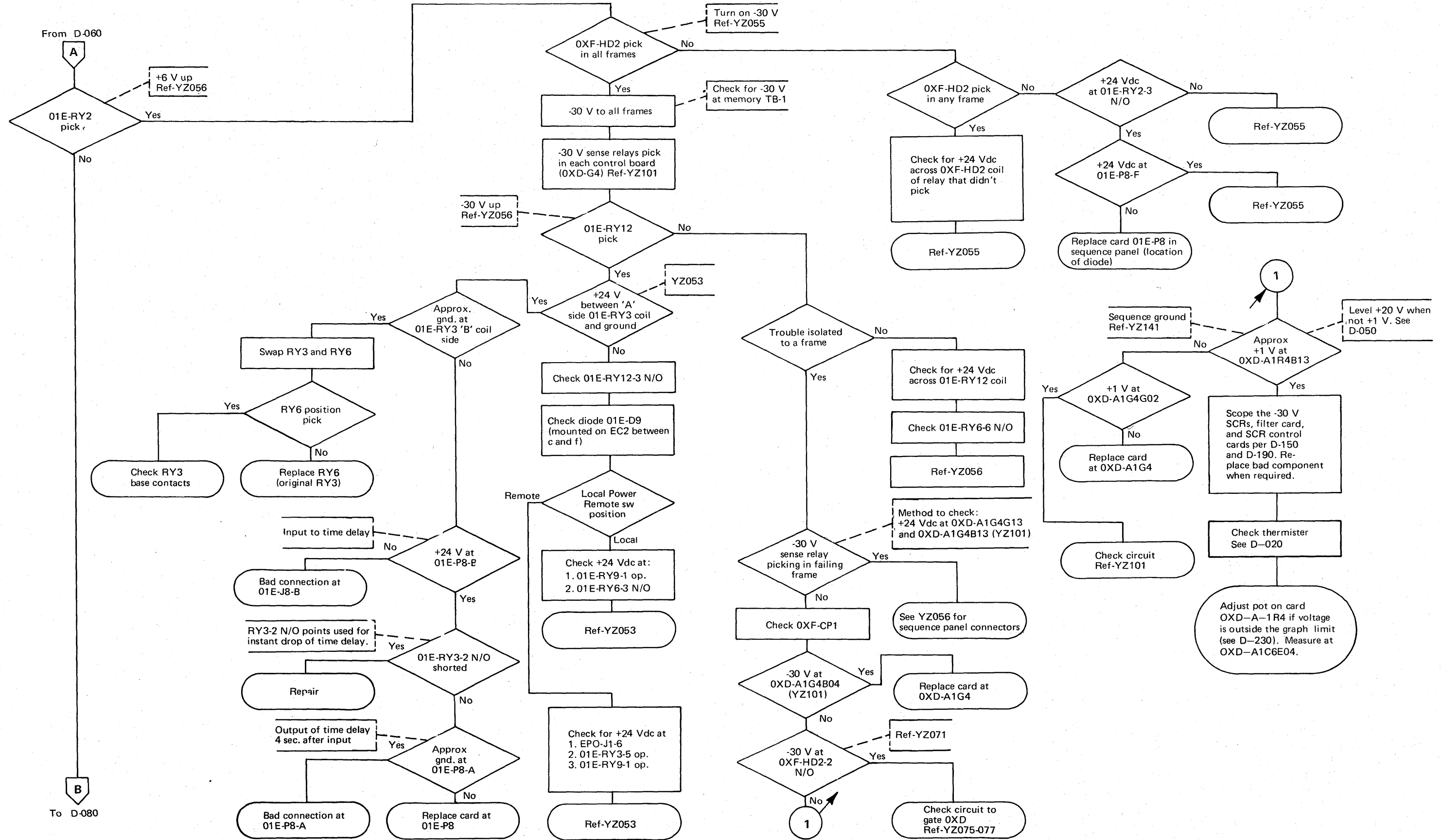
- Yes—Normal operation in which the relay picks and holds according to the power-on sequence chart on D-050 and drops according to the power-down sequence chart on page D-250.
- No—The relay fails to pick.
- Momentarily picks but doesn't hold—Do not take either the Yes or No path. This is a failure and you should determine why the relay did not hold up.

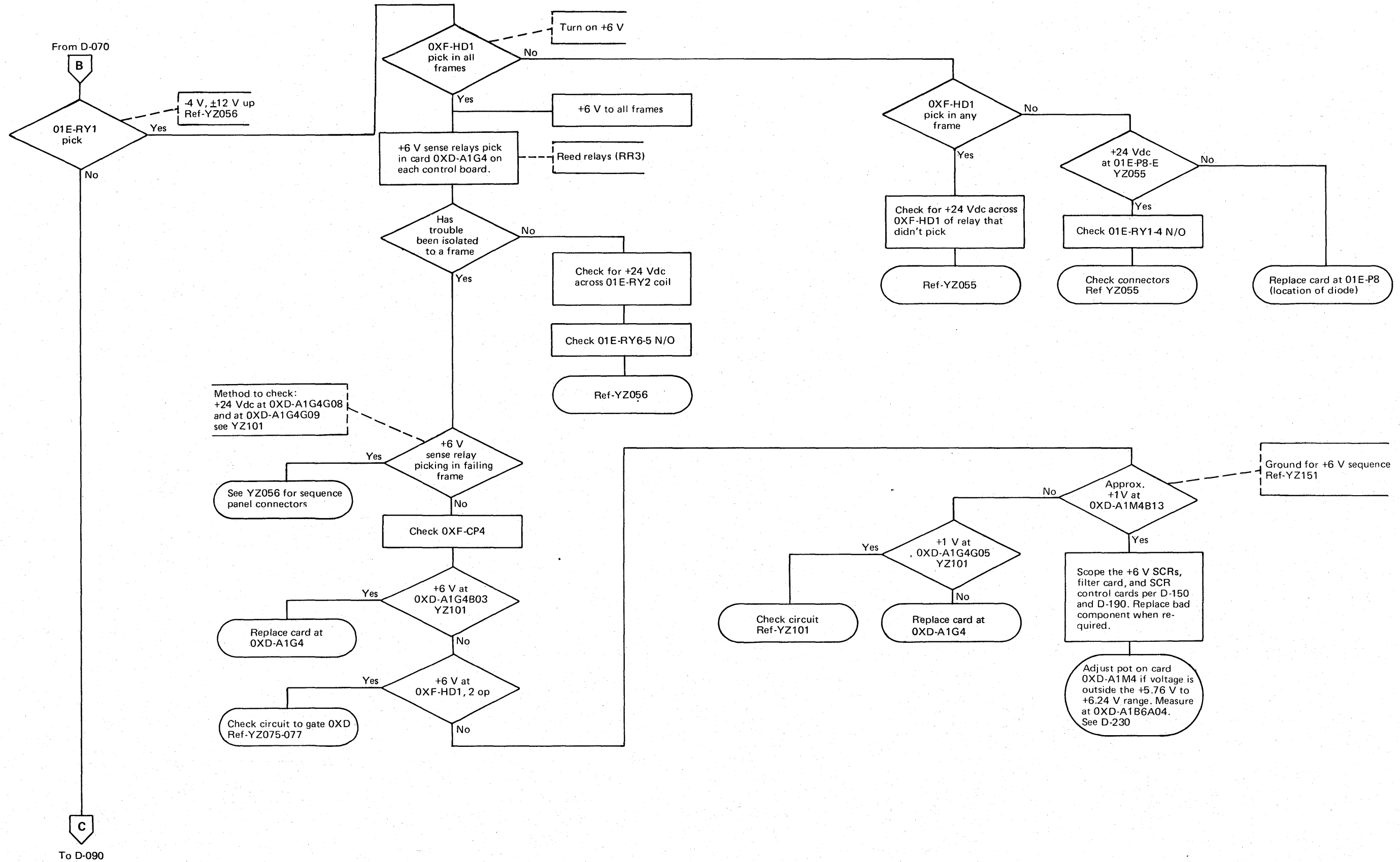


Configuration	Power control cable plug position See D-000
3705	01E-P1
1st Expansion Frame	01E-P2
2nd Expansion Frame	01E-P3
3rd Expansion Frame	01E-P4

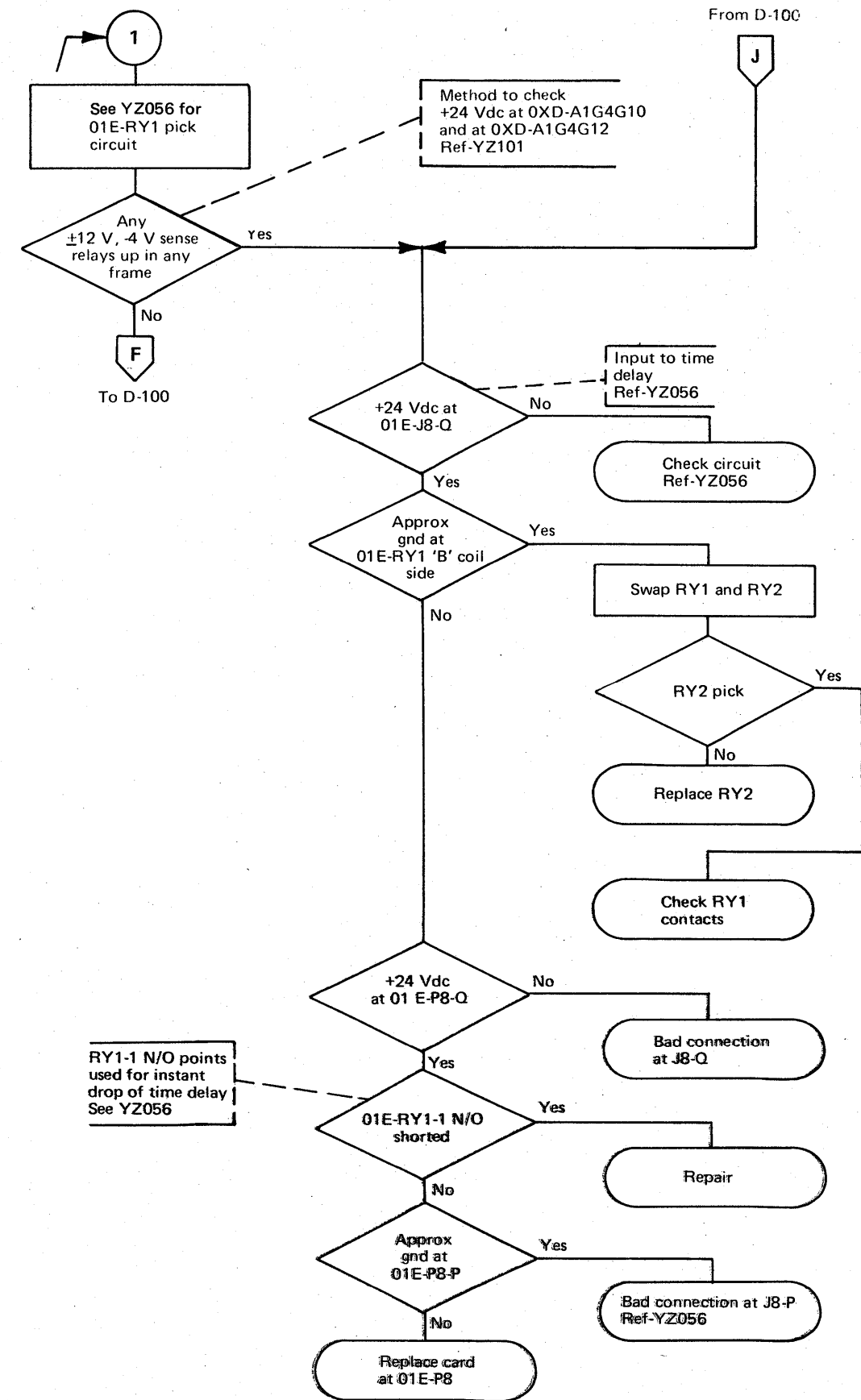
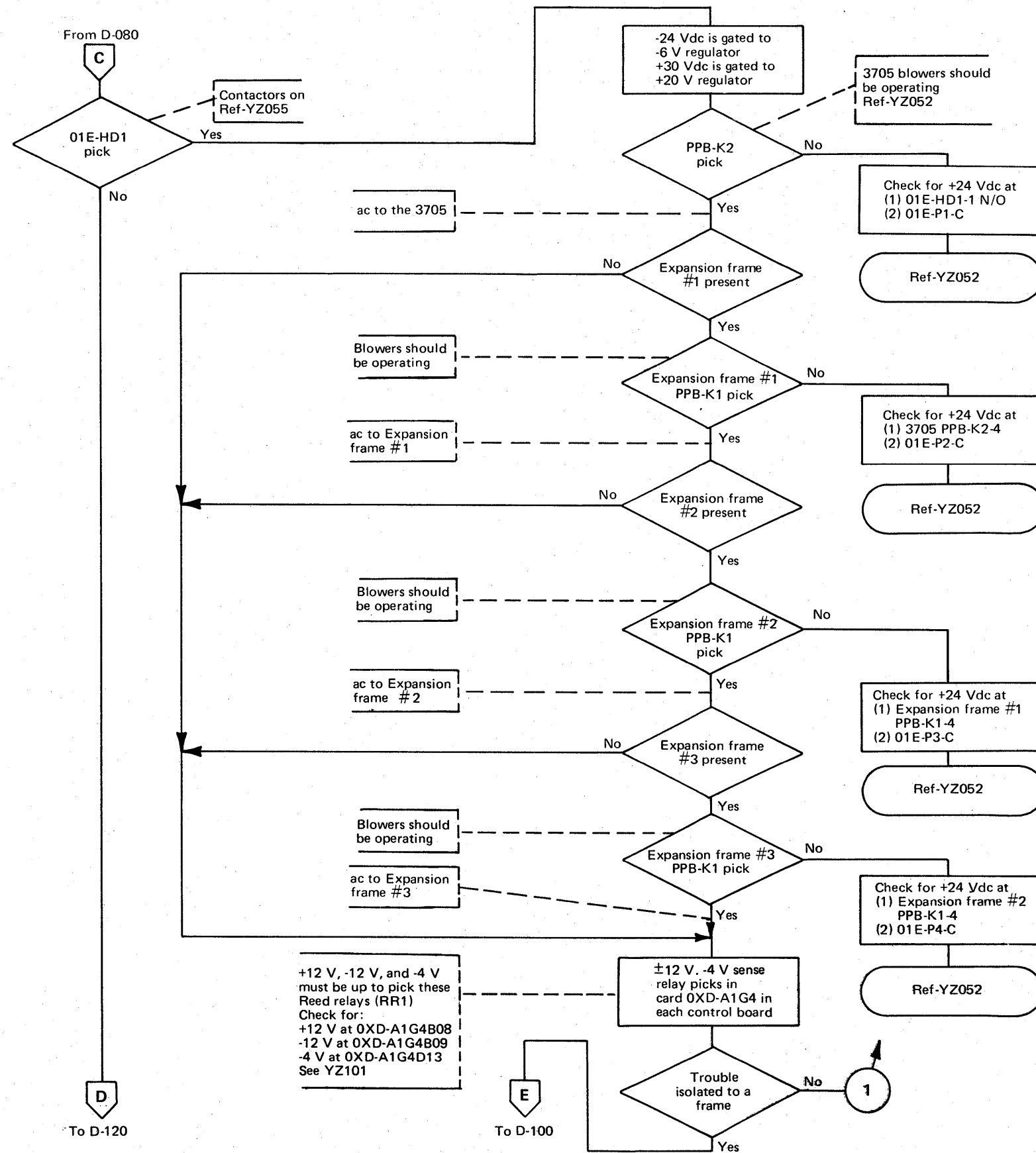
Dummy cards must be present in all positions that do not have the associated frame.

Prevents a thermal condition when the power control cable plug is removed.

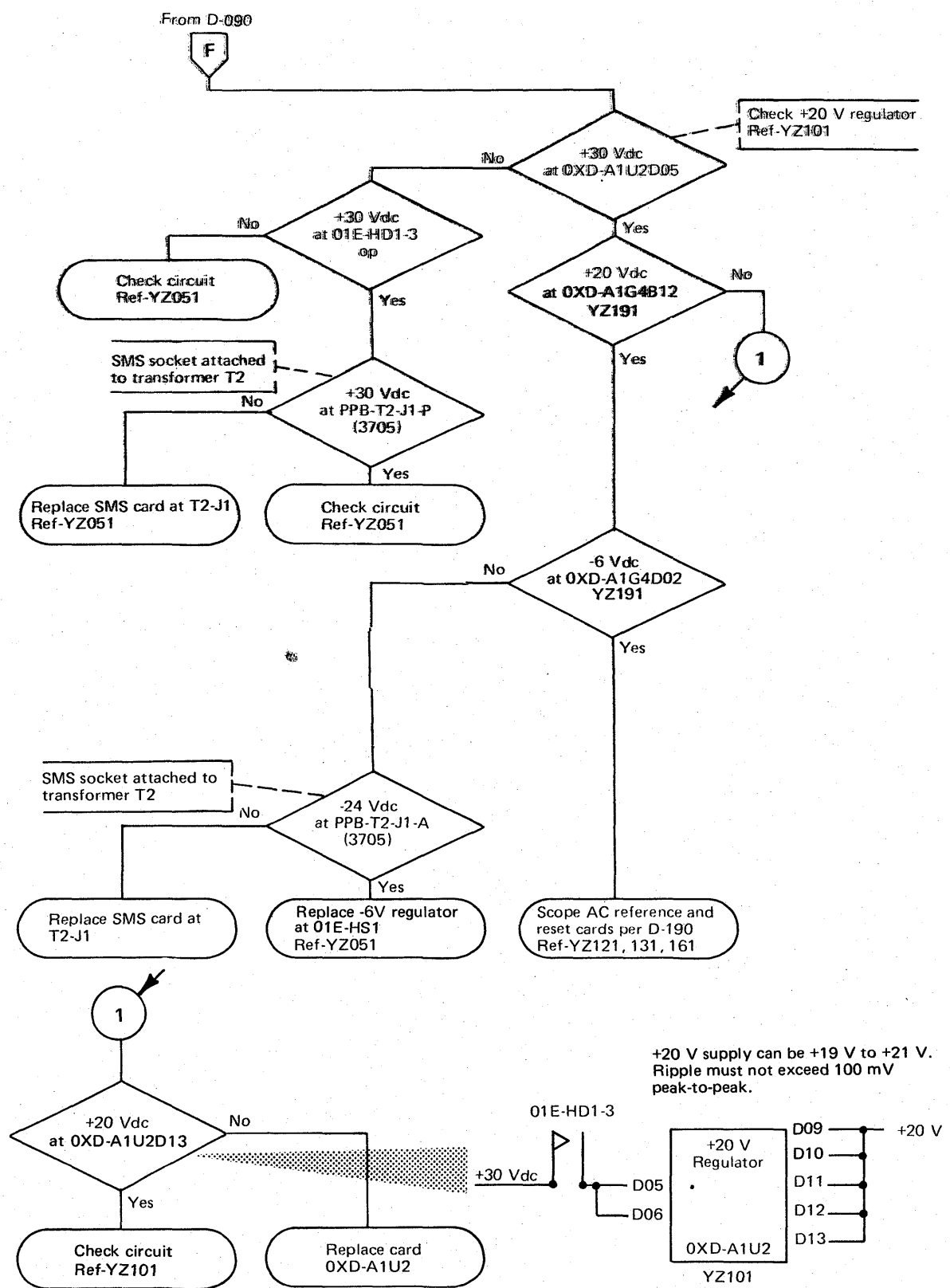
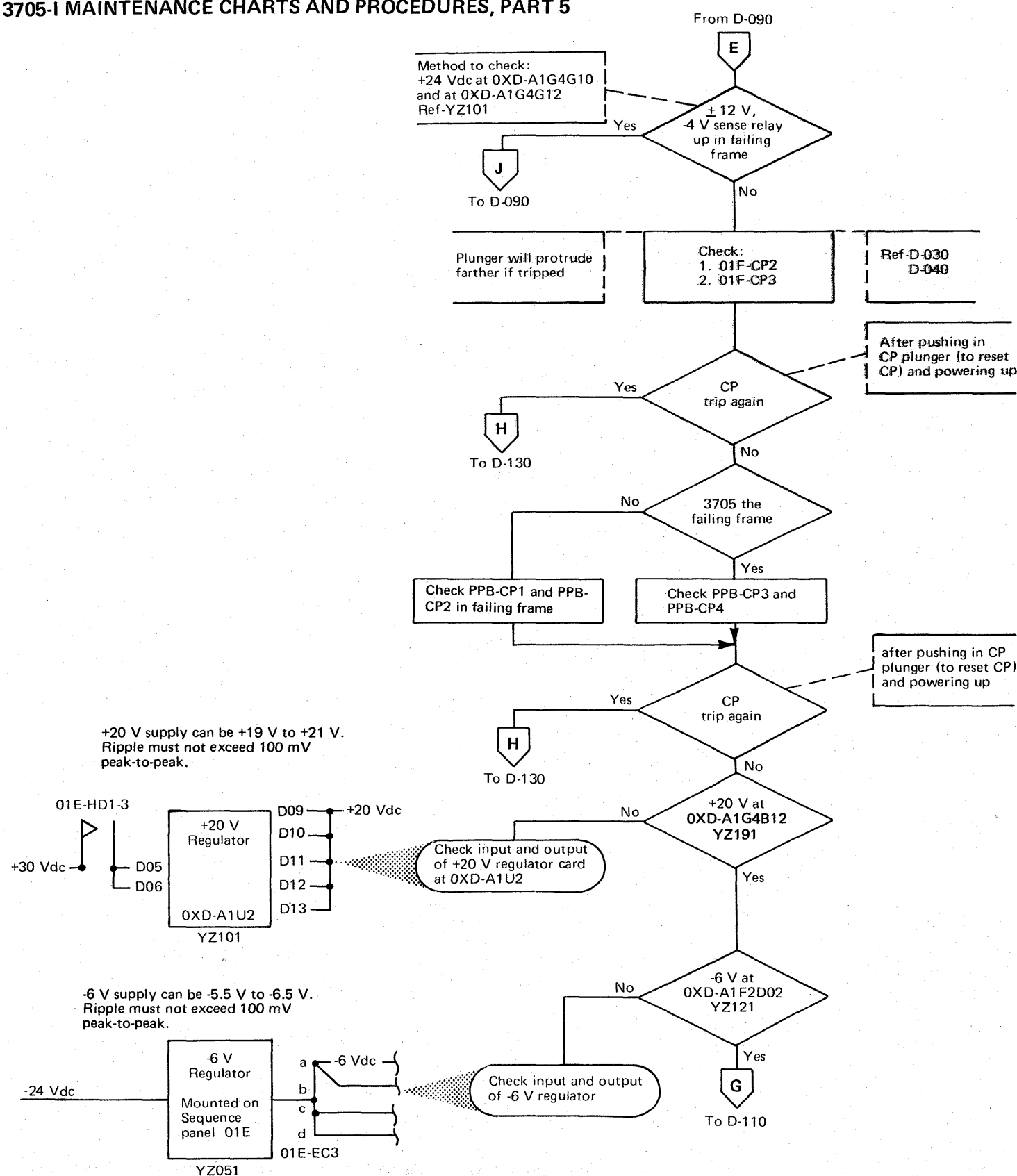




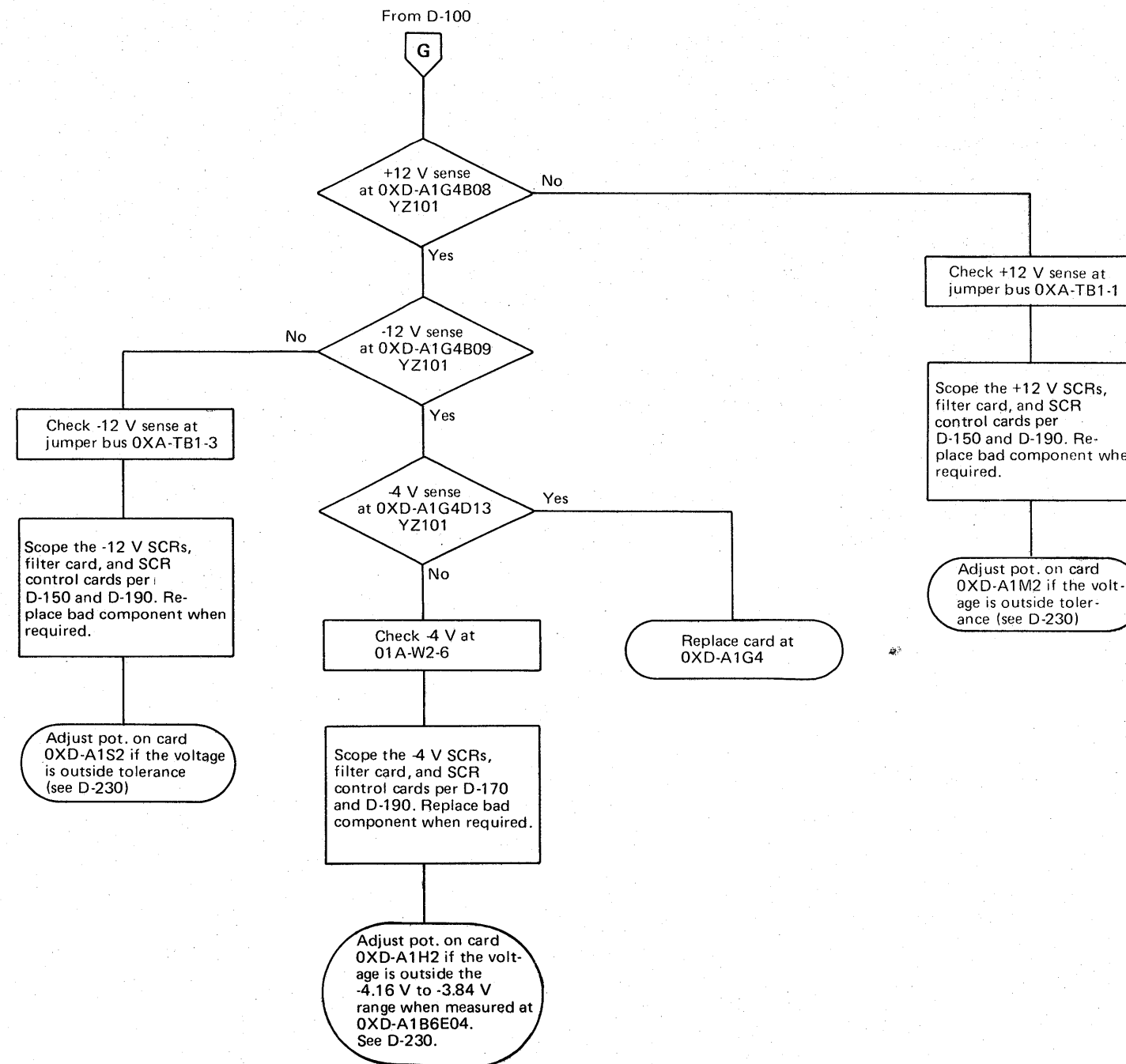
3705-I MAINTENANCE CHARTS AND PROCEDURES, PART 4



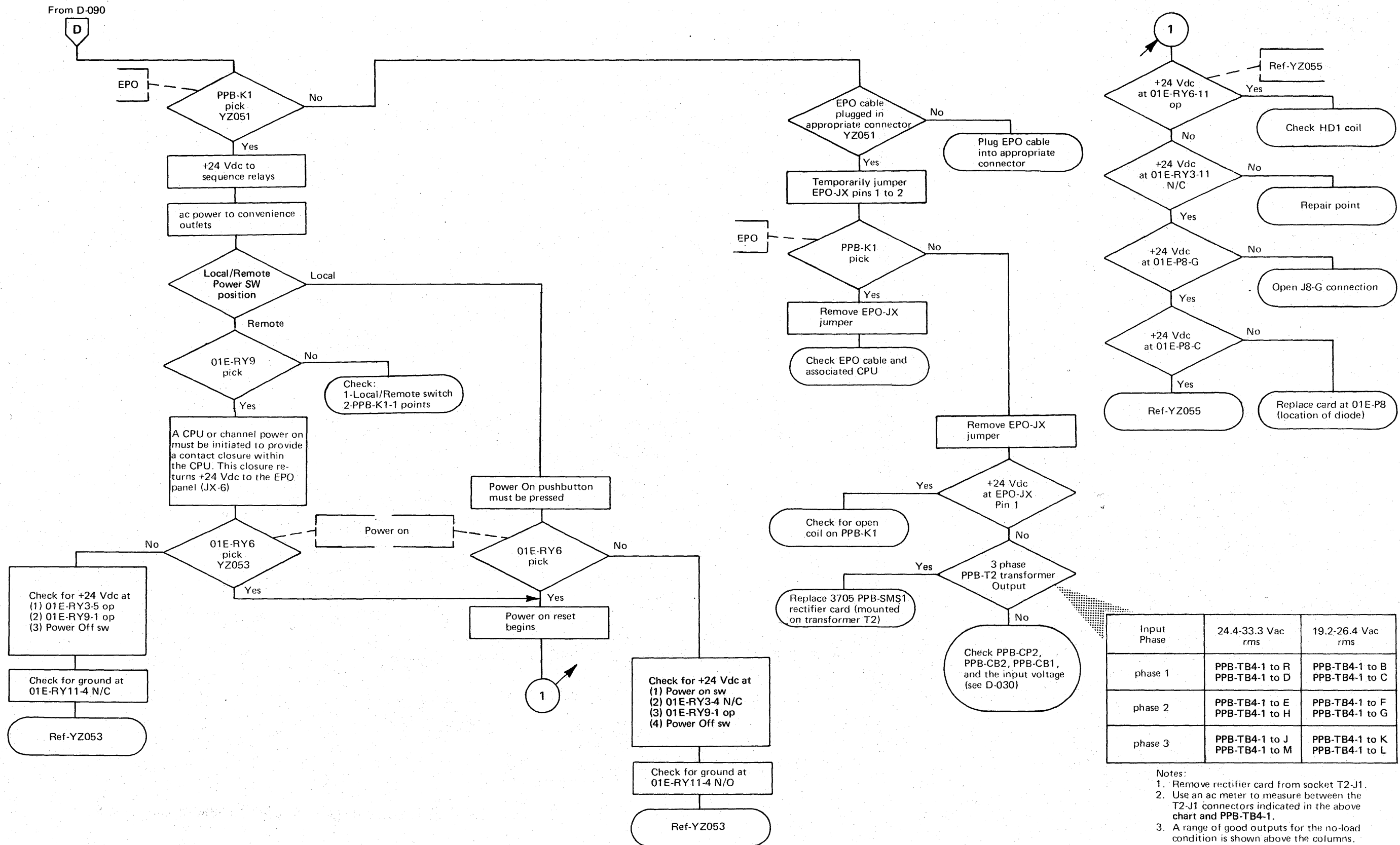
3705-I MAINTENANCE CHARTS AND PROCEDURES, PART 5



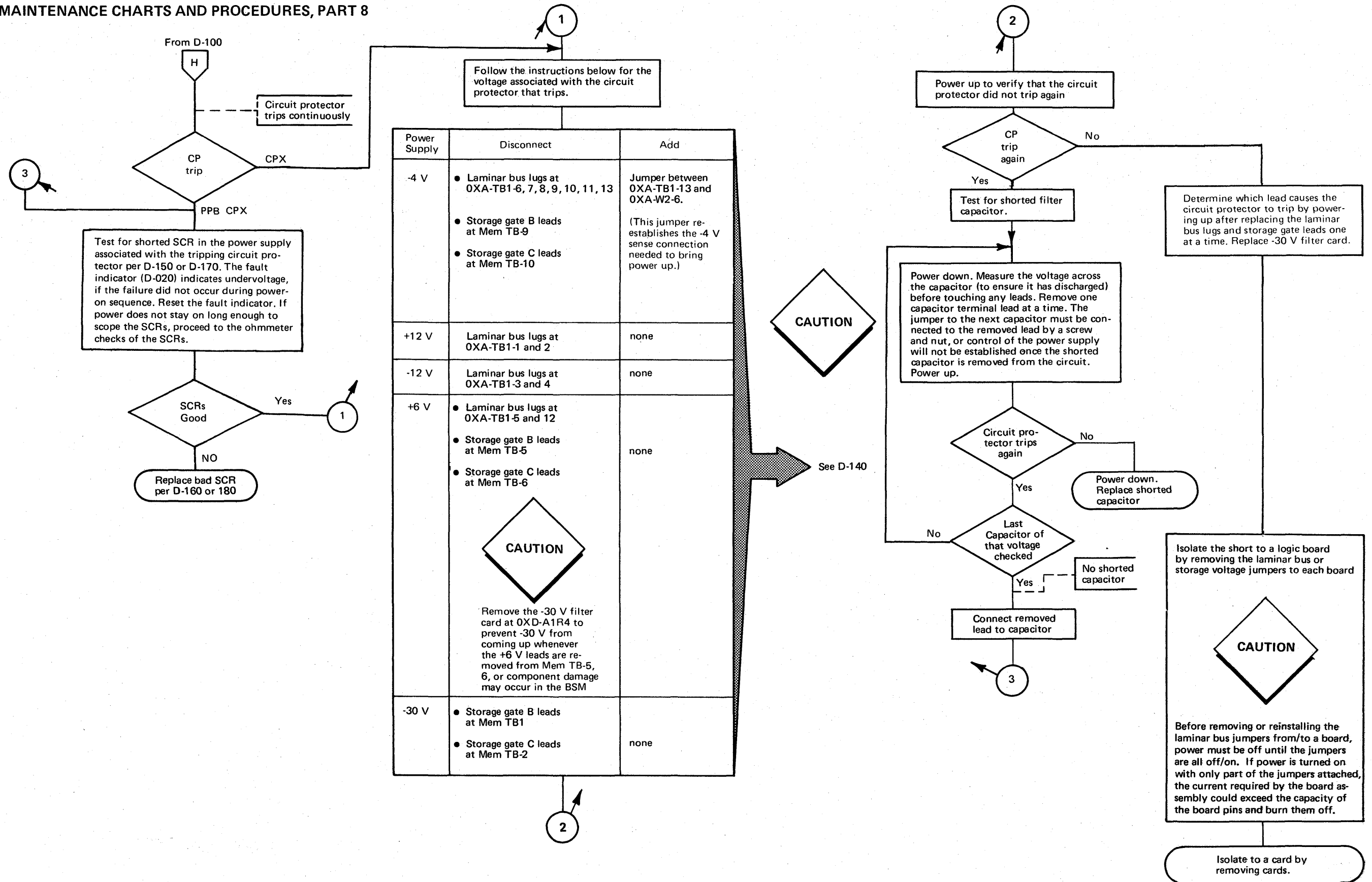
3705-I MAINTENANCE CHARTS AND PROCEDURES, PART 6



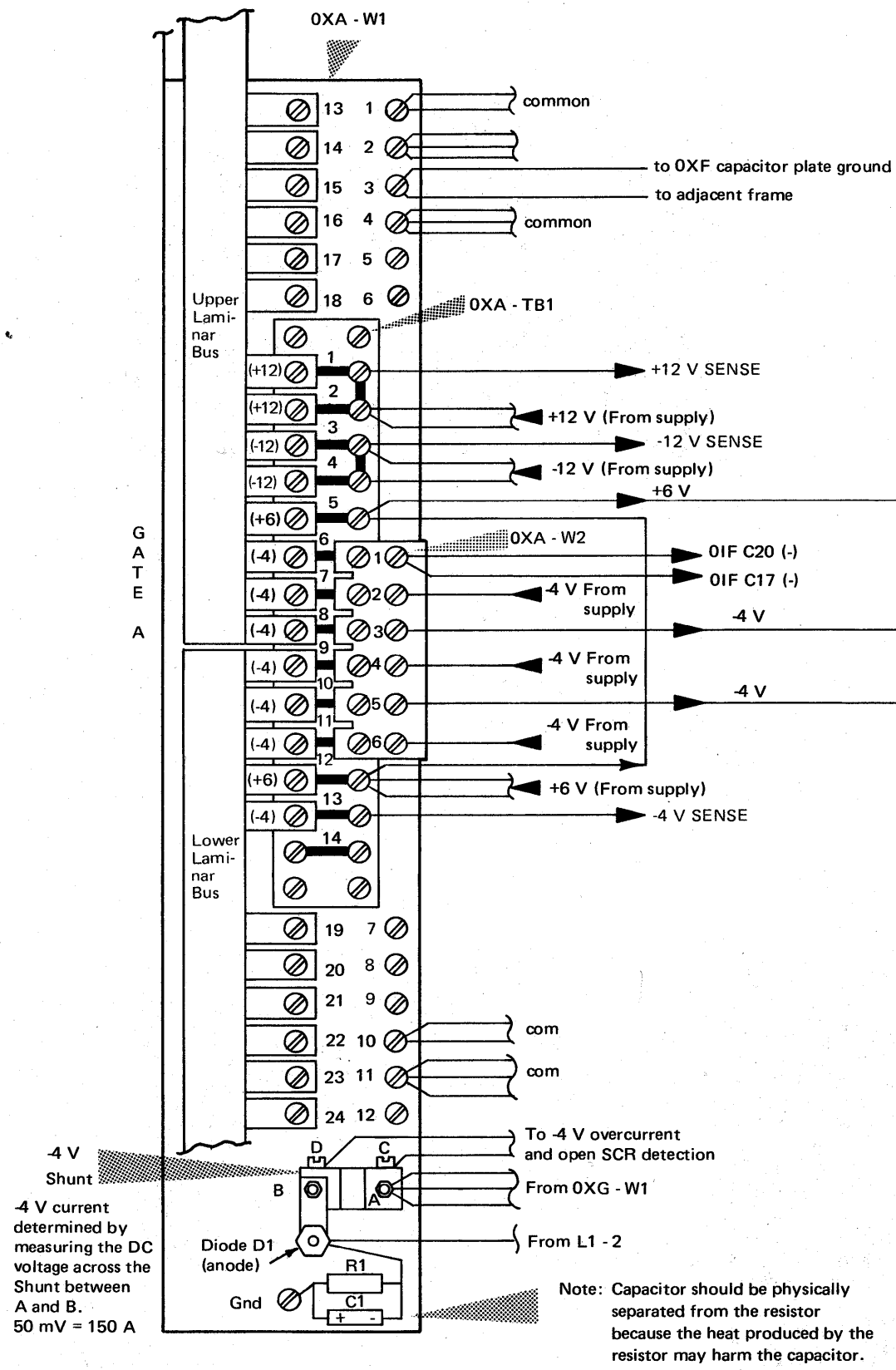
3705-I MAINTENANCE CHARTS AND PROCEDURES, PART 7



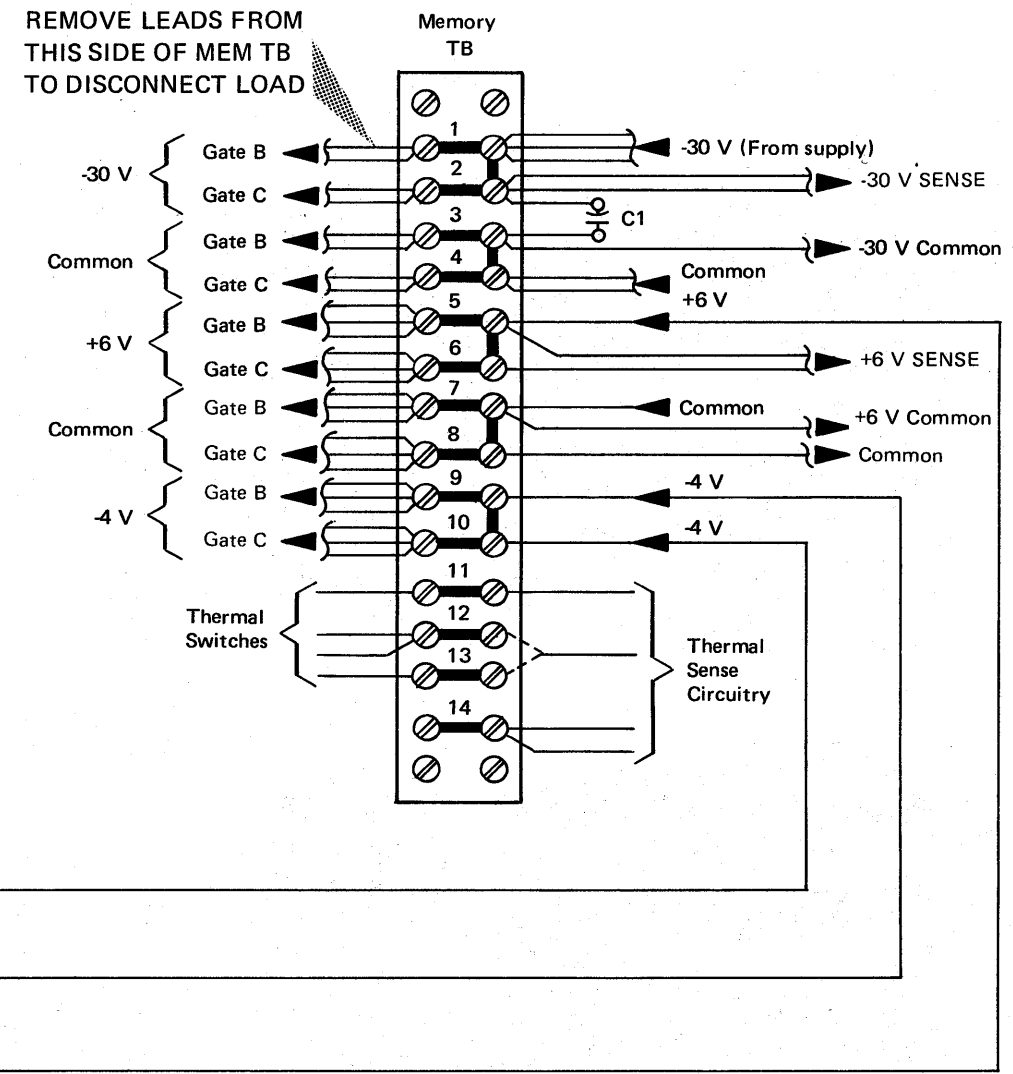
3705-I MAINTENANCE CHARTS AND PROCEDURES, PART 8



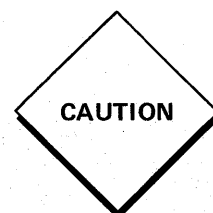
3705-I DC VOLTAGE DISTRIBUTION



4 V Shunt
4 V current determined by measuring the DC voltage across the Shunt between A and B.
50 mV = 150 A



Logic - YZ075 or YZ077



- Do not remove any of the wires labeled SENSE
- Do not remove any of the terminal board (TB) jumpers which connect a voltage with its sense lead.
- Do not bend the laminar bus tab too sharply because it may crack upon straightening.

CHECKING ±12 V, +6 V, -30 V SCR'S

Note: See D-560 for similar information on a 3705-II with only two or three cards in the OXD power control gate.

For -4 V, see D-170

Because the wave shapes for the ±12 V, +6 V, and -30 V are similar, only representative samples are shown.

- Setup the scope as follows:
 Sync the scope on LINE.
 Horizontal sweep at 2 ms/divn
 Vertical sweep-appropriate to voltage
- Put the scope probe on terminal 1 of the choke for the voltage being tested (see chart below).
 See **A** for the location of the choke.

Voltage	Choke
+6 V	L2
-12 V	L3
-30 V	L4
+12 V	L5

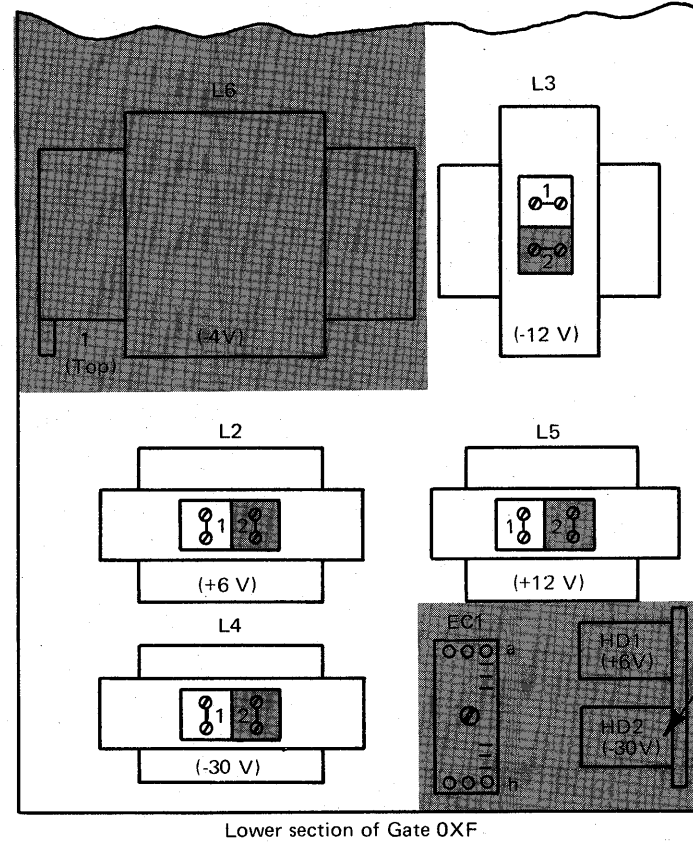
- There should be six pulses within 16.7 ms as shown in **B** (20.0 ms for 50Hz).

a. If one pulse is missing as shown in **C**, the problem is most likely an open SCR'.

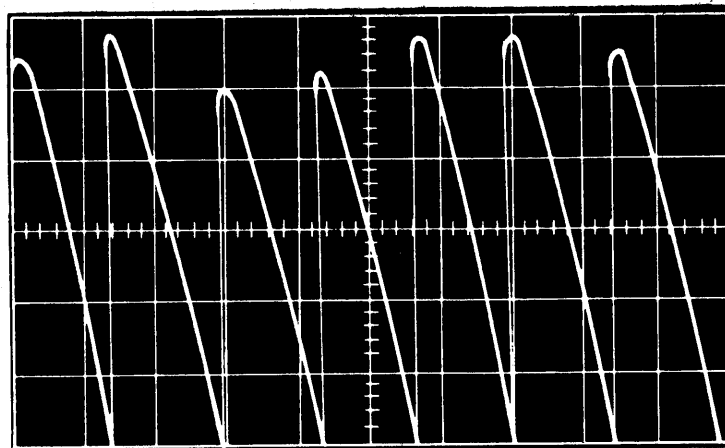
b. To locate an 'open SCR', scope the SCR cathodes at the OXD-A1xxxx points in **D**. The cathode wave

shape for a good SCR is shown in **E**. When an SCR does not conduct, the cathode wave shape has no 'step' in the negative going portion, as shown in **F**.

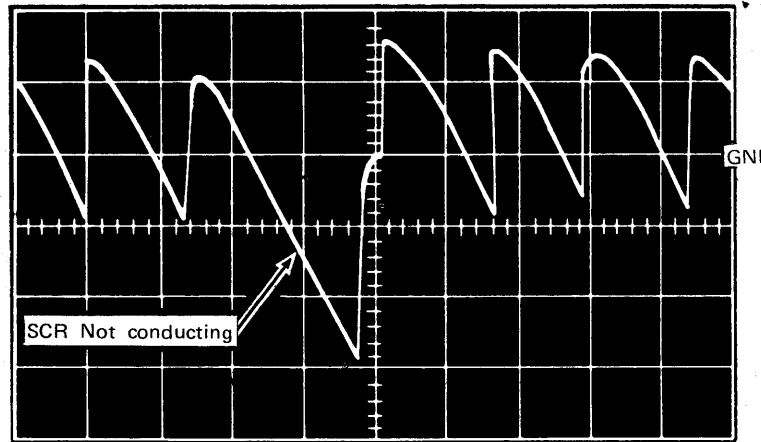
c. If two pulses are missing as shown in **G**, the problem is most likely a bad SCR control card since one SCR control card drives two SCRs. **D** shows the SCR control card that drives the appropriate SCRs for each voltage.



A Capacitor Bank



B NORMAL OPERATION +6 V at L2-1
 Horz - 2 ms/divn
 Vert - 2 V/divn
 Sync - Line



C ONE SCR OPEN +12 V at L5-1
 Horz - 2 ms/divn
 Vert - 10 v/divn
 Sync - Line

3705-II

Note: Not applicable to a 3705-II with only two or three cards in the OXD power control gate.

01F-HD2 applies +12 V to the basic frame logic.

0XF-HD2 applies +12 V to the expansion frame logic and turns on the -30 V power supply if one is present.

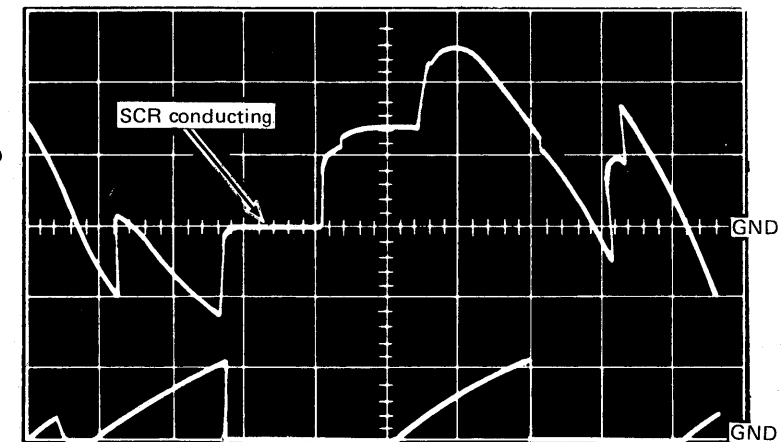
Voltage	Filter Card	SCR NO.	SCR Control Card	SCR Cathode OXD-A1xxxx
-30 V See 3705-II below	R4	1	N4	A4B04
		2	P4	A4B05
		3	Q4	A4B07
		4	Q4	A4B09
		5	P4	A4B10
		6	N4	A4B12
+6 V	M4	9	J4	C4B04
		10	K4	C4B05
		11	L4	C4B07
		12	L4	C4B09
		13	K4	C4B10
		14	J4	C4B12
-12 V	S2	17	P2	A5B04
		18	Q2	A5B05
		19	R2	A5B07
		20	R2	A5B09
		21	Q2	A5B10
		22	P2	A5B12
+12 V	M2	25	J2	C5B04
		26	K2	C5B05
		27	L2	C5B07
		28	L2	C5B09
		29	K2	C5B10
		30	J2	C5B12

D

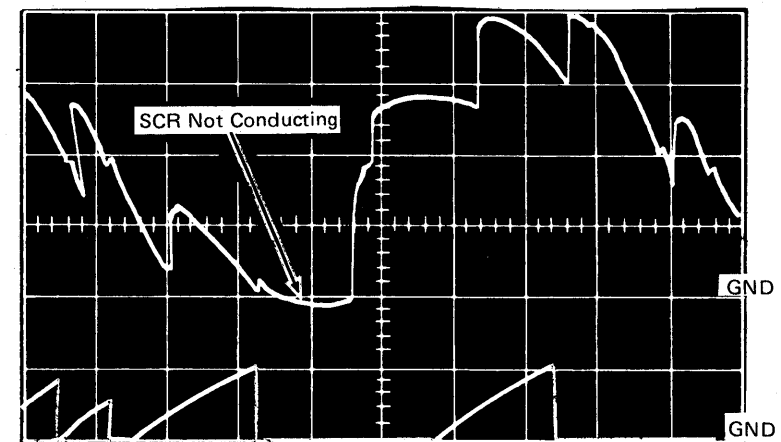
3705-II

Basic frame: -30 V SCR control cards are not installed since the -30 V is never used. The -30 V power supply components may not be installed in some machines.

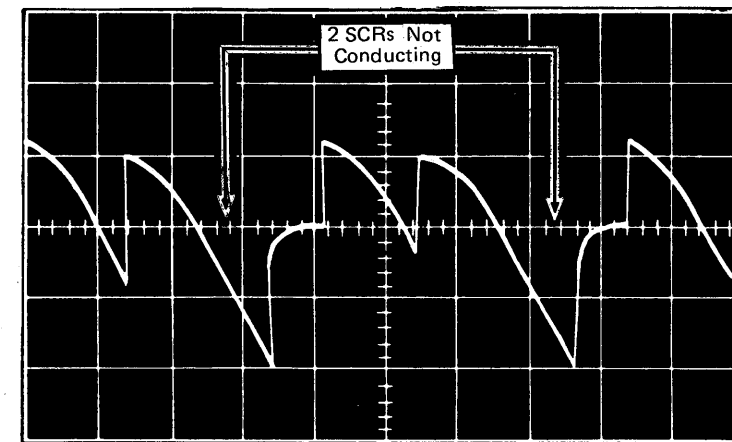
Expansion frames: The -30 V power supply components may or may not be installed. If installed, the -30 V is only used for power-up sensing.



E Upper - CATHODE OF GOOD SCR (+12 V) at OXD-A1C5B12
 Lower - RAMP at OXD-A1J2B09
 Horz - 2 ms/divn
 Sync - Line
 Vert - Upper - 20 v/divn
 Lower - 10 v/divn



F Upper - CATHODE OF OPEN SCR (+12 V) at OXD-A1C5B12
 Lower - RAMP at OXD-A1J2B09
 Horz - 2 ms/divn
 Sync - Line
 Vert - Upper - 20 v/divn
 Lower - 10 v/divn



G BAD SCR CONTROL CARD-1 PHASE NOT FIRING
 2 SCRs -30 V at L4-1
 Horz - 2 ms/divn
 Vert - 20 V/divn
 Sync - Line

SERVICE AID

The SCR control cards that drive the SCR are all interchangeable within a power supply or with another power supply.

CHECKING ± 12 V, +6 V, -30 V SCR'S, PART 2

- 4 Press Power Off push button. Turn off PPB-CB1, the main CB in the 3705. Remove the appropriate SCR control cards, PN 5862617, associated with the shorted SCR (see **D** on D-150). Turn on PPB-CB1. Press Power On push button.

- 5 If one SCR is shorted, the wave shape will be similar to **H**.

- 6 If the wave shapes are good, insert the SCR control cards removed in paragraph 4.

LOCATING THE SHORTED SCR

- Turn off PPB-CB1.
- Remove heat sink cover.
- Remove 2 screws that hold the front edge of the heat sink that contains the bad SCR (see **I** for heat sink locations).
- Pull the heat sink assembly to the front of the tower.
- Test for 'anode' to 'cathode' shorts
 - Remove the *three* center tap leads from the secondary winding of transformer T3 as specified in the following table.

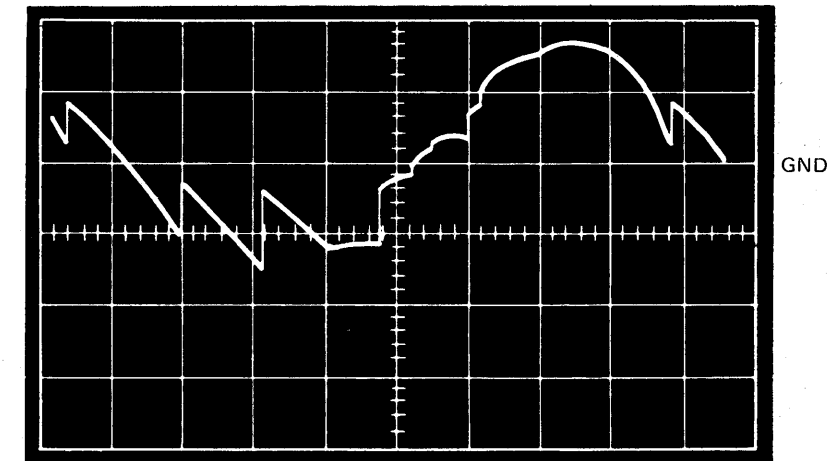
Voltage	Remove 3 Xmfr leads at:
-30 V	T3-TB1-9
-12 V	T3-TB1-10
+12 V	T3-TB1-11
+6 V	T3-TB1-12

Ref: YZ071

- Use an ohmmeter to determine which SCR is shorted. A shorted SCR may appear as a direct short with a low resistance between the cathode and anode, or may appear as a diode, with a high resistance in one direction and a low resistance in the other. A good SCR has a high reading between the cathode and anode in both directions. Check all SCRs on the heat sink.

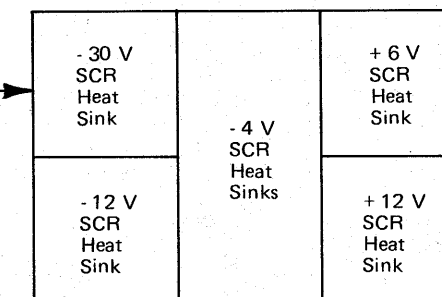
- Test for 'gate' to 'cathode' shorts
 - Remove the three SCR control cards associated with that voltage (see **D** on D-150).
 - Use an ohmmeter to measure the resistance between the gate and cathode of each SCR (see **J**).

- Readings of 50 ohms or greater in both forward and reversed directions indicate no short. A reading of only a few ohms indicates a short.
- Unsolder the leads to the bad SCR.
 - Remove the nut and lockwasher that hold the SCR to the heat sink and remove SCR.
 - Mount the new SCR on heat sink.
 - Resolder leads to proper SCR terminals.
 - Slide the heat sink into the tower so the rear slots engage the insulators.
 - Replace 2 front screws—make sure the front slots engage the insulators. If washers were used with these screws, discard them. Washers are no longer used.
 - Replace heat sink cover.
 - Make sure the SCR control cards associated with this voltage are removed. Bring power up and ensure there is no voltage at the respective measurement point (see D-230). Turn power off. Use an ohmmeter to measure between pins J05 and B13 on the removed SCR control cards. If the reading is 150 ohms, replace the SCR control card. Readings of 10 ohms or less are normal. Repeat measurements between G02 and G04.
 - Reinsert good SCR control cards.
 - Replace the center tap leads removed in (6).
 - Turn on PPB-CB1 and power up to verify the repair

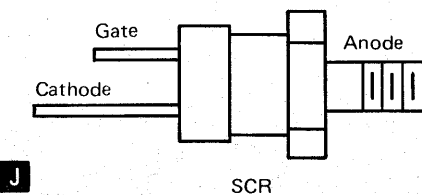


H One SCR Shorted +6 V at L2-1
 Horz — 2 ms/divn
 Vert — 5 V/divn
 Sync — Line

May not be installed in a 3705-II



I Gate 01G Heat Sink Locations.



J

CHECKING -4V SCR'S

Note: See D-560 for similar information on a 3705-II with only two or three cards in the OXD power control gate.

For ± 12 V, +6 V, -30 V, see D-150.

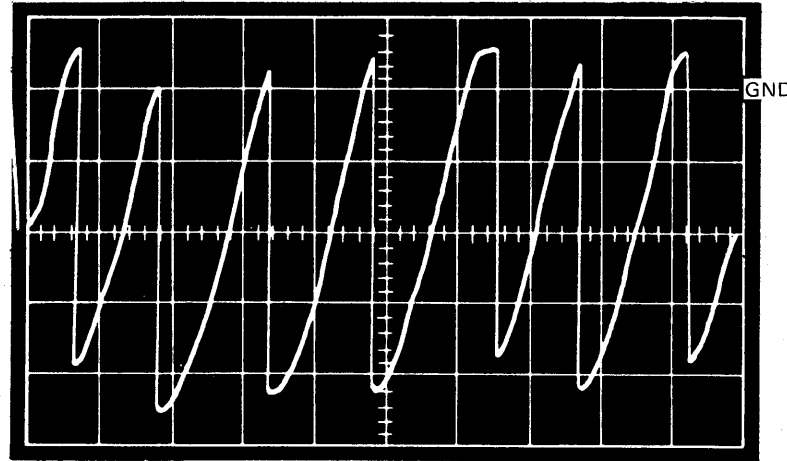
- 1 Set up the scope as follows:
 Sync - Line
 Horizontal sweep - 2 ms/divn
 Vertical sweep - appropriate to voltage
- 2 Scope at anode of diode D1 (end with wires). Diode is located at bottom of OXA-W1 distribution common plate (see YZ075/077 or D-140).
- 3 There should be six pulses within 16.7 ms as shown in 1 (20.0 ms for 50 Hz).
- 4 2 shows a wave shape with one pulse missing. The problem is most likely an 'open SCR'. To locate a specific 'open SCR' change the vertical sweep to 0.5 V/divn and scope the 'regenerative gate' at the heat sink edge connectors according to the following chart.

SCR No.	SCR Regen. Gate
7	0XG-EC1-h
8	0XG-EC1-g
15	0XG-EC2-g
16	0XG-EC2-h
23	0XG-EC3-h
24	0XG-EC3-g

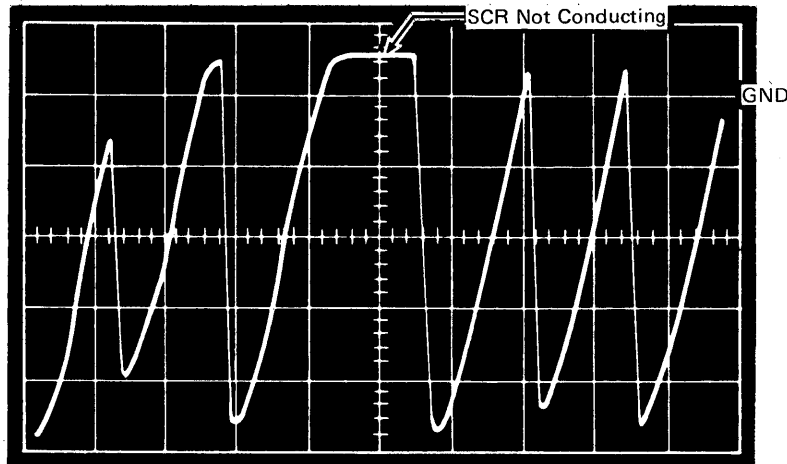
Refer to 7 on D-180 for the location of the edge connectors.

The wave shape of the 'regenerative gate' during normal operation is shown in 3. The amplitude of the 'regenerative gate' varies with power loading (1.5 V, ± 0.75 V for 140 A load). However, if the SCR is 'open', no pulse will appear on the scope.

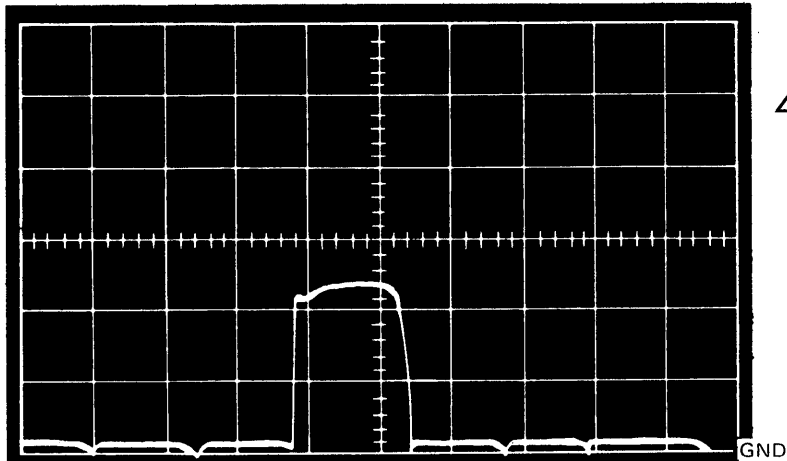
Note: The regenerative gate may not be found on all machines because it is only a test point. An alternate test is to observe each SCR anode wave shape with an oscilloscope. A good SCR anode wave shape is shown in 4, and an 'open' SCR anode wave shape is shown in 5.



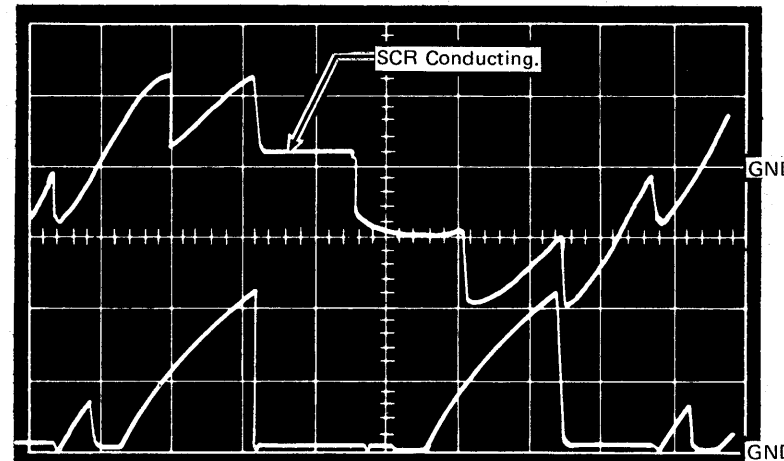
1 NORMAL OPERATION -4 V at Anode of Diode D1
 Horz - 2 ms/divn
 Vert - 2 V/divn
 Sync - Line



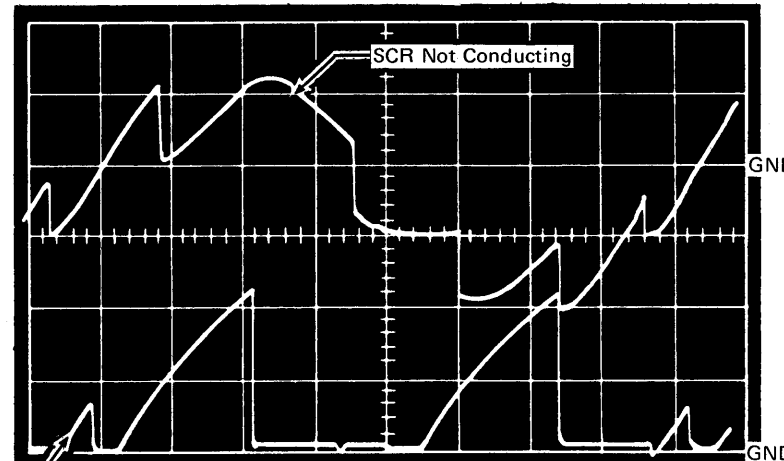
2 OPEN SCR -4 V at Anode of Diode D1
 Horz - 2 ms/divn
 Vert - 2 V/divn
 Sync - Line



3 SCR Regenerative Gate -
 NORMAL OPERATION at 0XG-EC1-h
 Horz - 2 ms/divn
 Vert - 0.5 V/divn
 Sync - Line



4 Upper - GOOD SCR ANODE WAVE SHAPE (-4 V) at 0XG-TB1-1
 Lower - RAMP at 0XD-A1E2B09
 Horz - 2 ms/divn
 Sync - Line
 Vert - Upper - 10 V/divn
 Lower - 5 V/divn



5 Upper - OPEN SCR ANODE WAVE SHAPE (-4 V) at 0XG-TB1-1
 Lower - RAMP at 0XD-A1E2B09
 Horz - 2 ms/divn
 Sync - Line
 Vert - Upper - 10 V/divn
 Lower - 5 V/divn

Note: Multiple extraneous pulses may appear between the good ramp pulses as shown above. The smaller extraneous pulses have no adverse effect.

CHECKING -4 V SCR'S, PART 2

- 5 If two pulses are missing, as shown in **6**, the problem is most likely a bad SCR control card because one SCR control card drives two SCRs (see the following chart). A bad SCR control card can quickly be isolated by interchanging the three SCR control cards in the -4 V supply with any other supply (see D-000 for other positions).

SCR No.	SCR Control Card
7	E2
8	E2
15	F2
16	F2
23	G2
24	G2

- 6 A 'cathode' to 'anode' short of an SCR in the -4 V supply causes circuit protector PPB-CP4 to open. The SCR may open due to the high shorting current. A 'control gate' to cathode' short may not cause PPB-CP4 to open.

(a) Test for 'anode' to 'cathode' short (SCR did not open).

1. Power down and turn off PPB-CB1.
2. Remove each T4 transformer lead to the SCR anode at OXG-TB1-X (see YZ073). Use an ohmmeter to determine which SCR is shorted by measuring between each OXG-TB1-X anode lead and the ground bus HS-GBW1 (see **7**). A shorted SCR may appear as a direct short with a low resistance between the cathode and anode, or may appear as a diode, with a high resistance in one direction and a low resistance in the other. A good SCR has a high reading between the cathode and anode in both directions. Check all SCRs.

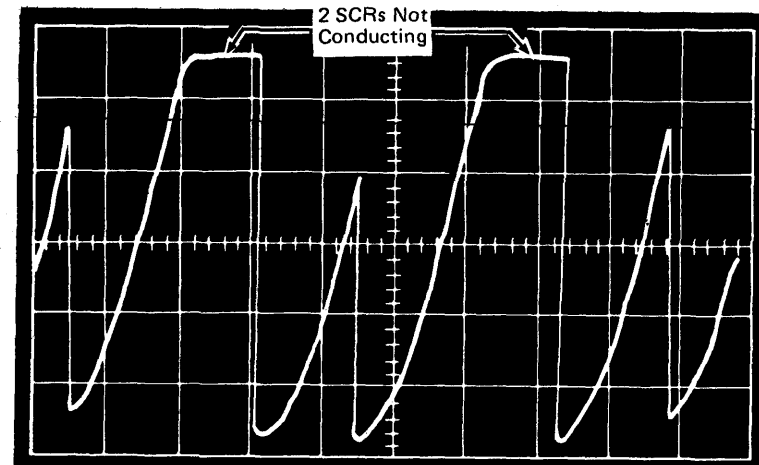
3. Connect the T4 transformer leads at OXG-TB1-X

(b) Test for 'control gate' to 'cathode' short.

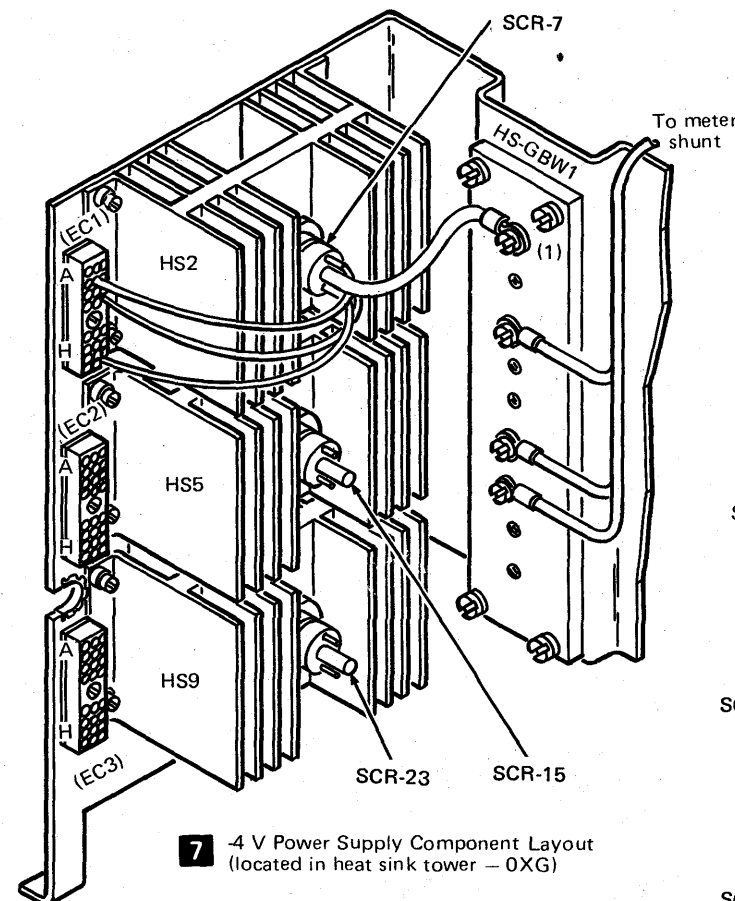
1. Remove SCR control cards at OXD-A1E2, F2, and G2.
2. Use an ohmmeter to measure the resistance between the control gate (white) and the cathode (red) —see **8**. Readings of 50 ohms or greater in both forward and reversed directions, indicate no short. A reading of a few ohms indicates a short.

3. If all SCRs are good, reinsert the SCR control cards and turn on PPB-CB1.

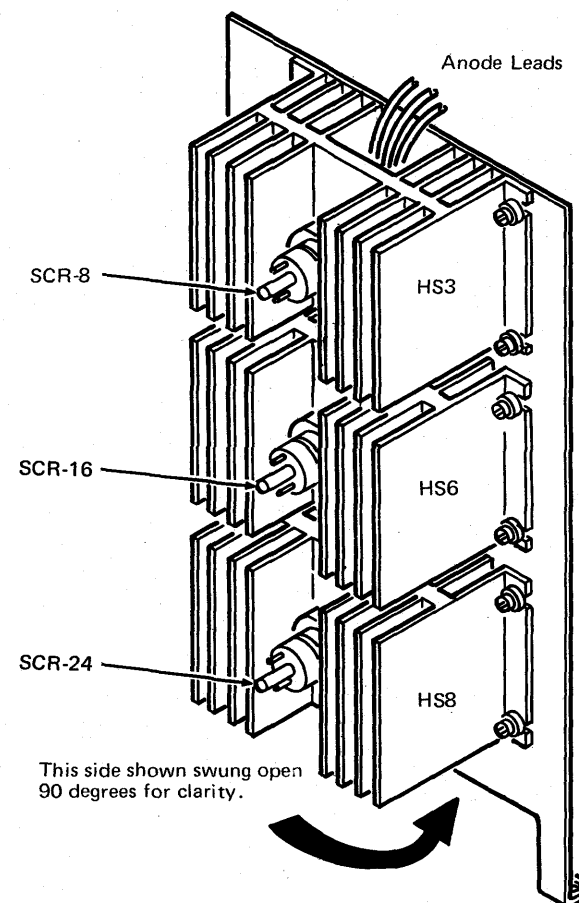
If the trouble has not been determined by the above procedure, continue the analysis by referring to D-190 and D-200.



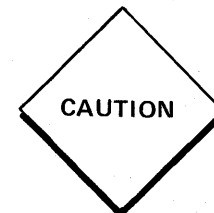
6 Bad voltage regulator card -4 V at Anode of Diode D1
Horz - 2 ms/divn
Vert - 2 V/divn
Sync - Line



7 -4 V Power Supply Component Layout
(located in heat sink tower - OXG)

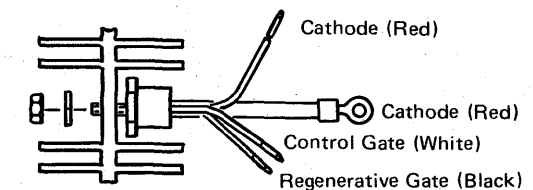


This side shown swung open 90 degrees for clarity.

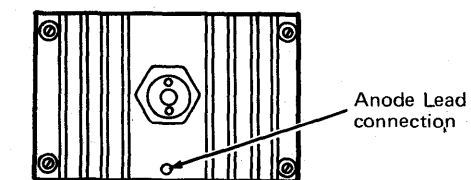


TO REPLACE A -4 V SUPPLY SCR (INCLUDING HEAT SINK)

- (1) Turn off PPB-CB1, main CB in the 3705.
- (2) Remove heat sink cover.
- (3) Remove the three SCR leads to the edge connector.
- (4) Remove the heavy cathode lead from ground bus HS-GBW1.
- (5) If the SCR to be replaced is SCR-7, SCR-15, or SCR-23 (see **7**), loosen and lift the edge connector located directly in front of the SCR assembly to be replaced.
- (6) Remove the two screws that hold the front edge of the heat sink to be removed.
- (7) Carefully slide the heat sink forward until the anode lead attached to the rear of the heat sink can be reached with a screwdriver (see **9**). Remove this lead from the heat sink.
- (8) Install the new SCR assembly by performing steps 1 through 7 in reverse. Do not substitute any other washer for those removed with the screws in step 6, because a larger washer could short the heat sink.
- (9) Remove the SCR control cards in OXD-A1E2, F2, and G2 if they are plugged. Bring power up and check that there is no -4 V at the measurement point, OXD-A1B6E04. Turn power off.
- (10) Use an ohmmeter to measure between pins J05 and B13 on the removed -4 V SCR control cards. If the reading is 150 ohms, replace the SCR control card. Readings of 10 ohms or less are normal. Repeat measurements between G02 and G04.
- (11) Reinsert good SCR control cards, turn on PPB-CB1 and then bring up power to verify the repair.



8 -4 V SCR Leads



9 -4 V Heat Sink

SCR CONTROLS

Note: Not applicable to a 3705-II with only two or three cards in the OXD power control gate.

One Phase of -4 V Supply

- This page shows one phase of the -4 V power supply and card inputs and outputs.
- The controls of the SCR are similar in all power supplies.
- The -4 V supply is the only supply to have SCRs with regenerative gates (not on all machines), a shunt for over-current detection, and a stabilizing circuit for low current (0-10A).

AC REFERENCE AND RESET CARD

There are three 'ac ref. and reset' cards in each frame — one for each phase. If one phase is lost, the power supply adjusts the SCR outputs from the other two phases to attempt to compensate for the lost phase. Consequently, if one 'ac ref. and reset' card goes bad, the customer may not be aware of the failure. The SCR open fault indicator (D-020) provides a visual indication that one or more -4 V SCRs is not operating correctly. With a lost phase, two SCRs do not operate in each power supply in each frame.

DC SIGNAL LEVELS

Voltage varies with potentiometer setting and power supply. The following table gives the range of voltages for NORMAL operation.

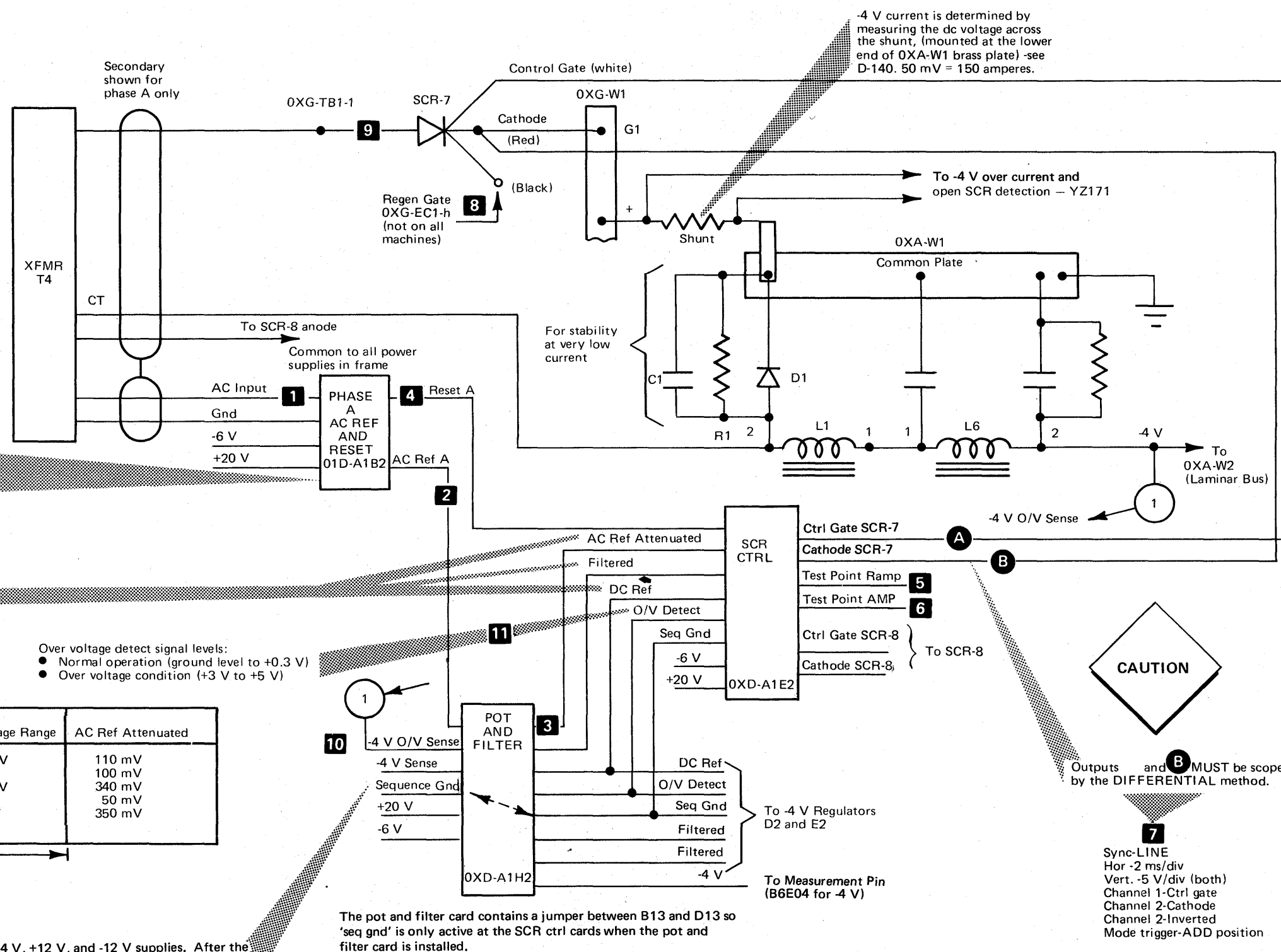
Power Supply	'DC Ref' Voltage Range	'Filtered' Voltage Range	AC Ref Attenuated
-4 V	1.25 V to 1.5 V	0.6 V to 0.75 V	110 mV
+12 V	1.85 V to 2.4 V	3.6 V to 4.4 V	100 mV
-12 V	2.6 V to 3.3 V	1.0 V to 1.25 V	340 mV
+6 V	1.6 V to 1.85 V	3.3 V to 3.7 V	50 mV
-30 V	*2.2 V to 2.8 V	*0.7 V to 1.0 V	350 mV

CE Meter or Weston 901 meter
 (CE meter may vary 10% from Weston)

*Reading will vary outside the range as room temperature varies.

SEQUENCE GROUND

It is tied to ground for the -4 V, +12 V, and -12 V supplies. After the -4 V, ±12 V supplies have sequenced up, this line signals the +6 V SCR controls to turn on by dropping from approximately +20 V to less than +1V. After the +6V supply has sequenced up, a similar level signals the -30V SCR control to turn on.



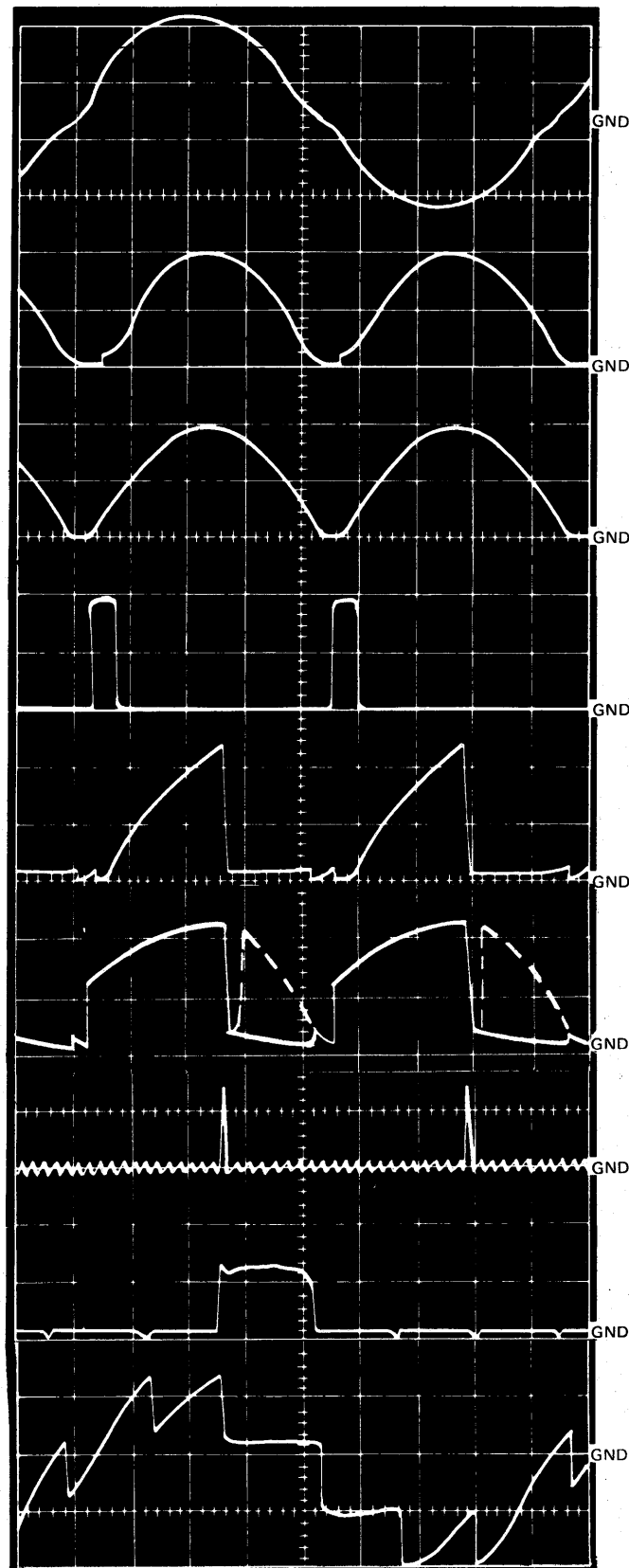
CAUTION
 Outputs **A** and **B** MUST be scoped by the DIFFERENTIAL method.
7
 Sync-LINE
 Hor -2 ms/div
 Vert -5 V/div (both)
 Channel 1-Ctrl gate
 Channel 2-Cathode
 Mode trigger-ADD position
 If an attempt is made to scope the 'control gate' with respect to the 'cathode' by putting scope ground on either 'control gate' or 'cathode', component damage will occur.

The pot and filter card contains a jumper between B13 and D13 so 'seq gnd' is only active at the SCR ctrl cards when the pot and filter card is installed.

SCR CONTROLS, PART 2

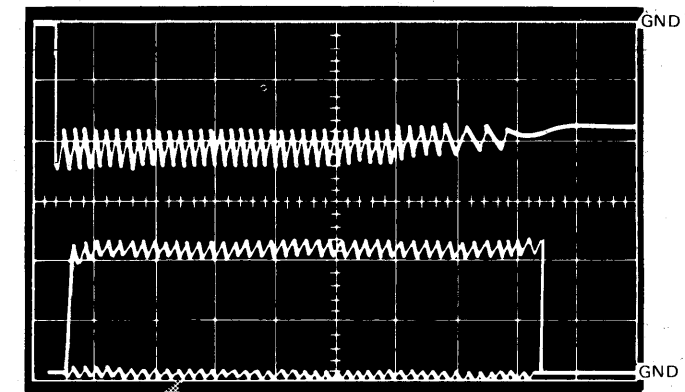
Scope settings for scope pictures 1-9:
 Horz — 2 ms/divn
 Vert — Line

- 1** AC Input at 0XD-A1B2B02
Vert — 20 V/divn
- 2** AC Ref A at 0XD-A1B2D13
Vert — 5 V/divn
- 3** AC Ref A (attenuated) at 0XD-A1H2D05
Vert — 50 millivolts/divn
- 4** Reset A at 0XD-A1B2B13
Vert — 2 V/divn
- 5** Test Point — RAMP at 0XD-A1E2B09
Vert — 5 V/divn
Note: Multiple ramp pulses may exist. See **E** on page D-170.
- 6** Test point — AMP at 0XD-A1E2J02
Vert — 5 V/divn
Note: The waveform indicated by the dashed lines may be present. They have no adverse effect.
- 7** SCR Trigger Pulse
Channel 1-Ctrl gate at 0XD-A1E2J05
Channel 2-Cathode at 0XD-A1E2B13
Vert — 5 V/divn (both channels)
Invert channel 2 and ADD
- 8** SCR-7 Regenerative Gate at 0XG-EC1-h
(Only used as a test point to verify that the SCR conducts)
Vert — 1 V/divn
Note: The regenerative gate may not be on all -4 V SCRs.
- 9** SCR-7 Anode at 0XG-TB1-1
Vert — 10 V/divn



10 -4 V DC Sense at 0XD-A1H2J02
Vert — 2 V/divn
Horz — 0.2 sec/divn
Sync — Power On push button

11 -4 V O/V Detect at 0XD-A1H2J12
Vert — 2 V/divn
Horz — 0.2 sec/divn
Sync — Power On push button



Power on transient — During power-on sequence this signal follows the -4 V excursions as seen in scope picture 10.

DESCRIPTION OF SCR CONTROLS

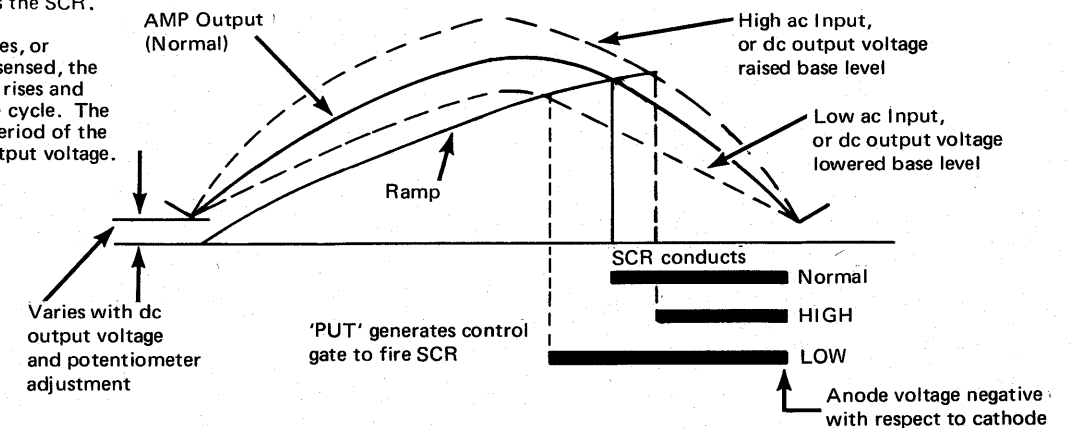
Wave shapes 1 through 9 apply to all power supplies except picture 8 which is unique to the -4 V supply.

- 1** ac input from transformer T4.
- 2** ac reference — a delay of approximately 500 microseconds occurs between the zero crossing of the ac input and the zero voltage point of the ac reference.
- 3** ac reference after passing through a resistor network to attenuate the signal.
- 4** Reset pulse — triggers the start of the 'ramp' in picture 5.
- 5** Ramp — starts after the reset pulse falls. The ramp is one input to an analog compare module (PUT).
- 6** AMP — output of the operational amplifier. This signal is the amplified 'ac ref A attenuated' whose base line is established by the output voltage and the potentiometer setting. The PUT (programmable unijunction transistor) compares the 'ramp' and 'AMP' output as indicated below and conducts when the 'ramp' voltage exceeds the 'AMP' voltage. The PUT output generates the control gate pulse which fires the SCR.

If the ac line input voltage rises, or a higher dc output voltage is sensed, the base output level of the AMP rises and the PUT conducts later in the cycle. The SCRs conduct for a shorter period of the cycle, and this lowers the output voltage.

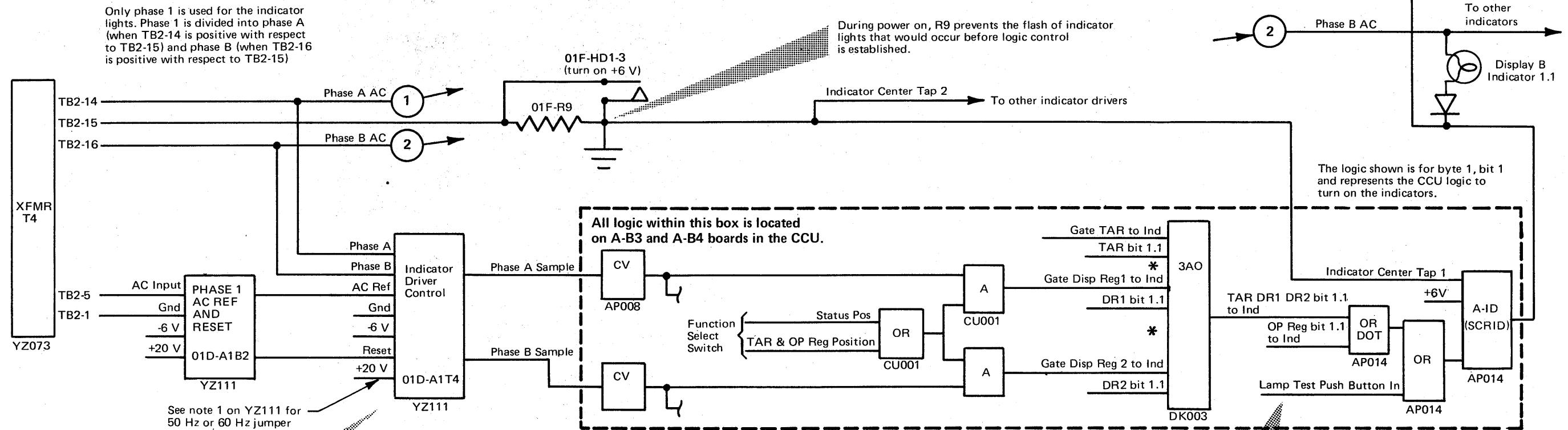
If the ac line input voltage falls, or a reduced dc output voltage is sensed, it lowers the base of the 'AMP' output, and the PUT conducts earlier in the cycle. The SCRs conduct for a longer period of the cycle, and this raises the output voltage (see drawing below).

- 7** SCR trigger pulse — fires the SCR. SCR conduction occurs when the control gate is positive with respect to the cathode. The SCR trigger pulse is initiated by the negative shift of the PUT output.
- 8** SCR-7 regenerative gate indicates the time the SCR is conducting. It is only a test point and is not connected to any circuit. It may not be found on all -4 V SCRs.
- 9** SCR-7 anode voltage — cuts off SCR conduction when the anode voltage goes negative with respect to its cathode.



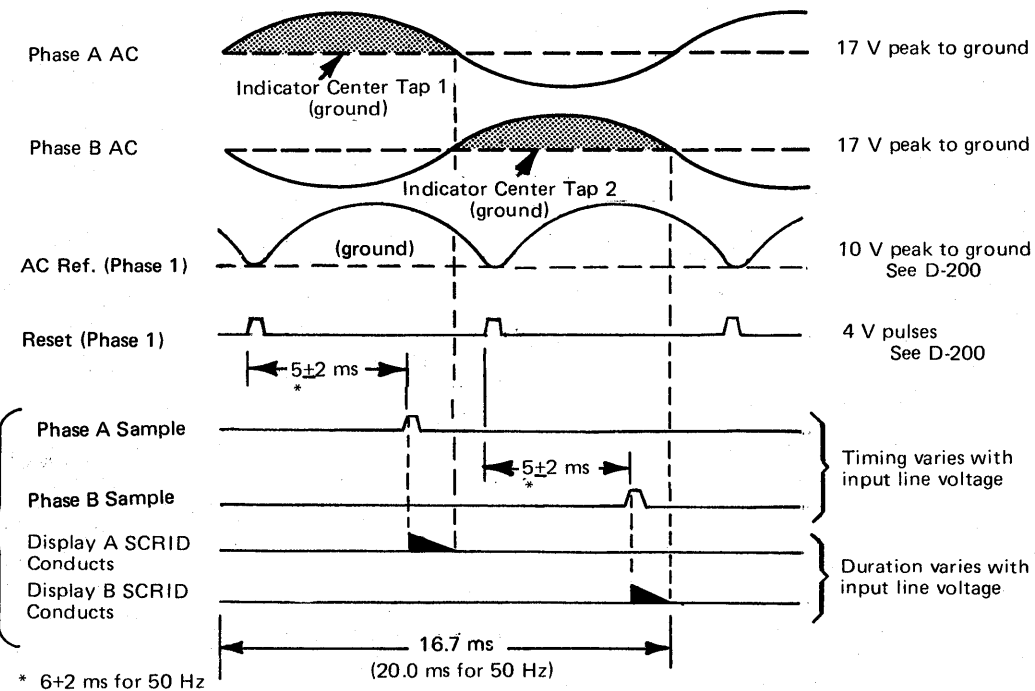
INDICATOR LIGHTS—SUPPLY/CONTROL

Note: See D-570 for similar information on a 3705-II with only two or three cards in the OXD power control gate.



The indicator driver control keeps those indicator lights that are 'on' at a relatively constant intensity during power line variations. The timing of the 'phase A sample' and 'phase B sample' pulses varies with the input voltage. These pulses, in turn, control the duration of conduction of the display A and B SCRIDs (silicon controlled rectifier indicator driver). This duration determines the intensity.

The indicator driver control operates on the same principle as the SCR control as explained on D-200.



Note: When the Lamp Test push button is pressed, the intensity of the indicator lights will increase.

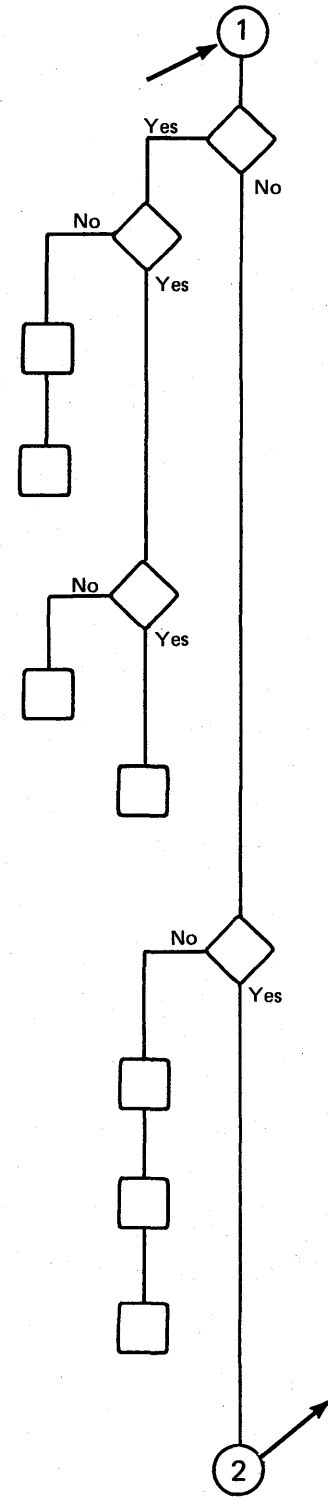
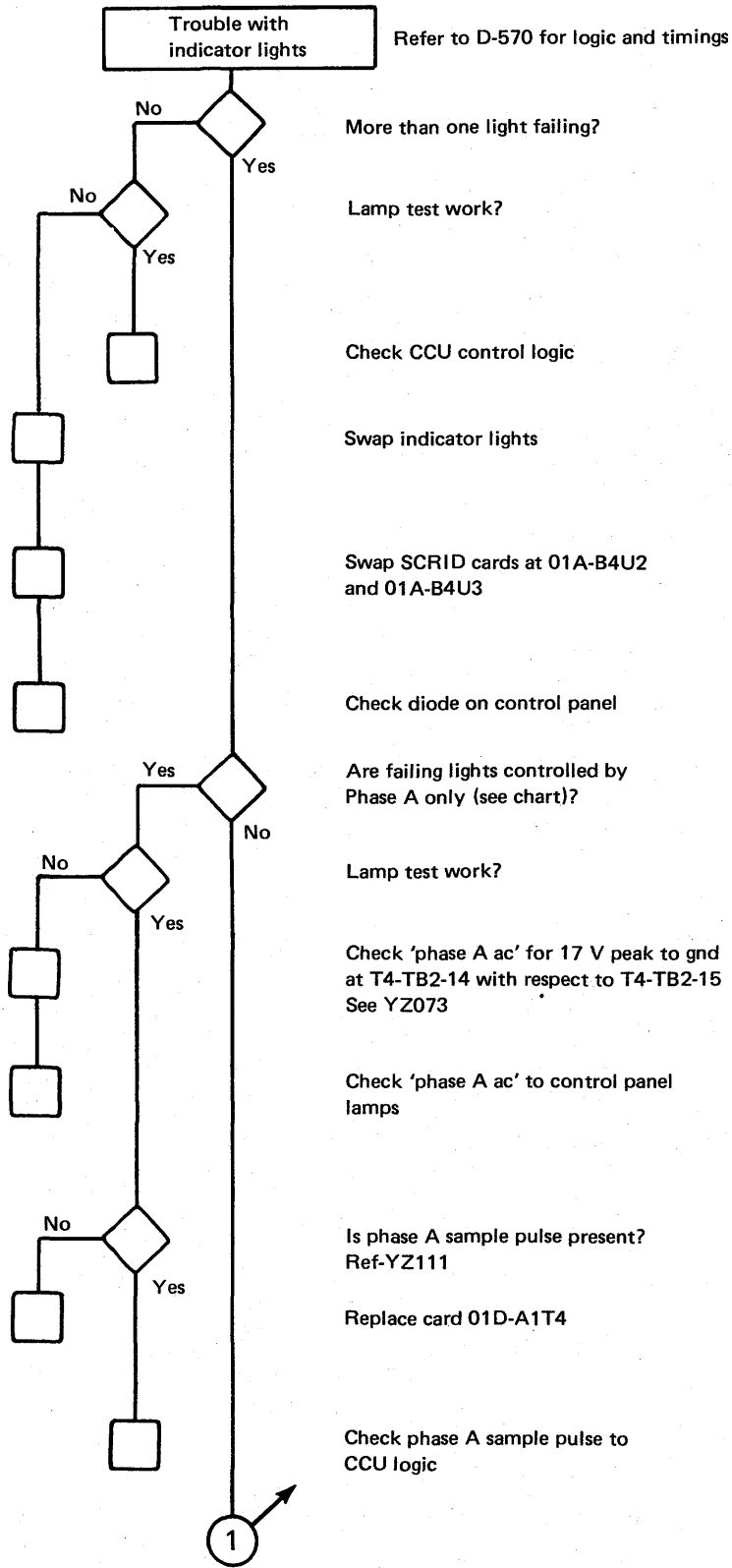
Amplitude varies linearly with line voltage. Values given are for 220 V line.

The timing of the 'phase A sample' with respect to the 'reset' pulse will change with input voltage variations (also 'phase B sample'). The indicator driver control card controls this timing. If the timing is outside this range, the light intensity will be too bright or too dim. The 01D-A1T4 card must be replaced to correct these conditions because there is no adjustment.

A peak voltage higher than the rated RMS voltage of the lights can be used without exceeding the average wattage of the light, because the lights receive pulses of current.

INDICATOR LIGHTS—CHARTS AND PROCEDURES

Note: See D-575 for similar information on a 3705-II with only two or three cards in the OXD power control gate.



Are failing lights controlled by phase only (see chart)?

Lamp test work?

Check 'phase B ac' for 17 V peak to gnd at T4-TB2-16 with respect to T4-TB2-15 See YZ073

Check 'phase B ac' to control panel lamps

Is phase B sample pulse present? Ref-YZ111

Replace card 01D-A1T4

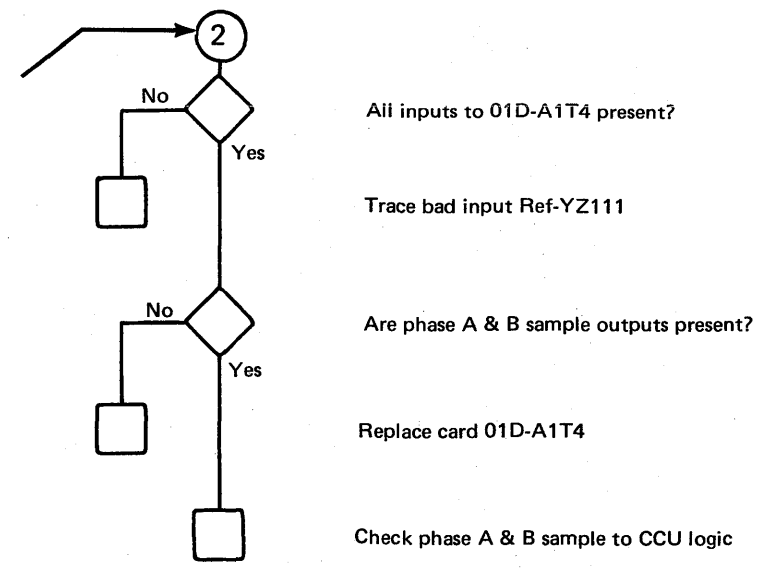
Check phase B sample pulse to CCU logic

Lamp test work?

Check inputs to indicator driver cards

Check 01F-HD1-3N/O

Check Xfmr T4 outputs at T4-TB2-14 & 16 with respect to T4-TB2-15 (17 V peak to ground)



Indicator Driver Card (SCRID)	Phase A ac	Phase B ac	Logic page
	Indicator Display A	Indicator Display B	
01A-B4U2	0.0	0.0	AP012
	0.1	0.1	AP012
	0.2	0.2	
	0.3	0.3	
	0.4	0.4	AP013
	0.5	0.5	AP013
	0.6	0.6	
0.7	0.7		
01A-B4U2	1.0	1.0	AP014
	1.1	1.1	AP014
	1.2	1.2	
	1.3	1.3	
	1.4	1.4	AP015
	1.5	1.5	AP015
	1.6	1.6	
1.7	1.7		
01A-B4U3	Chan 1 Intf A Enbl	Chan 1 Intf B Enbl	AP009
	Chan 2 Intf A Enbl	Chan 2 Intf B Enbl	
	Panel Active		
		CCU Check	AP009
	Spare Hard Stop Wait	Spare Pgm Display Test Pgm Stop	AP010
01A-B4U3	Load X.4	X.4	AP011
	X.5	X.5	
	X.6	X.6	
	X.7	X.7	

DC VOLTAGE MEASUREMENT

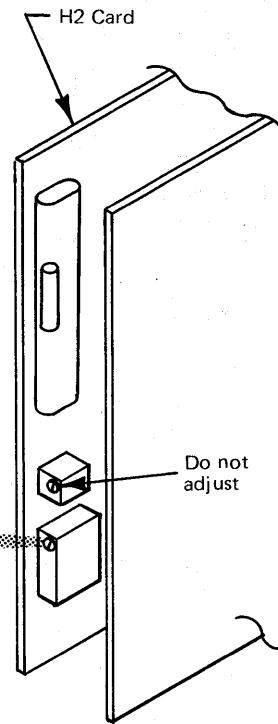
Note: See D-580 for similar information on a 3705-II with only two or three cards in the OXD power control gate.

- Voltages should be set using a Weston 901 meter (PN 460879) or equivalent.

All voltage measurements should be made at the specified points in the control board (except +3.4 V and +8.5 V).

Voltage	Voltage Measurement Points OXD-A1xxxxx	Card Location Of Voltage Adjustment Potentiometer	Maximum Ripple (peak to peak)
-30 V Note 1	C6E04	S5	1200 mV
-12 V	C6C04	S2	480 mV
- 4 V	B6E04	H2	80 mV
+ 6 V	B6A04	M4	240 mV
+12 V	B6C04	M2	480 mV
+3.4 V	01B-TB2-1 02B-TB2-1	None	80 mV
+8.5 V	01B-TB2-3 02B-TB2-3	None	200 mV

1



4 V pot and filter card H2 has two potentiometers. The voltage adjustment potentiometer is the only pot on the cards for the other voltages.

POWER SUPPLY REGULATION AND MAXIMUM CURRENT

Voltage	Power Supply Regulation	Maximum Rated Output Current	
		3705	Each expansion frame
-30 V Note 1	±1.20 V	8A	8A
-12 V	±1.20 V*	10A	10A
- 4 V	±0.16 V	160A	160A
+ 6 V	±0.24 V	10A	10A
+12 V	±1.20 V *	30A	30A
+3.4 V	±0.34 V	30A	3705-II basic frame only
+8.5 V	±0.85 V	10A	

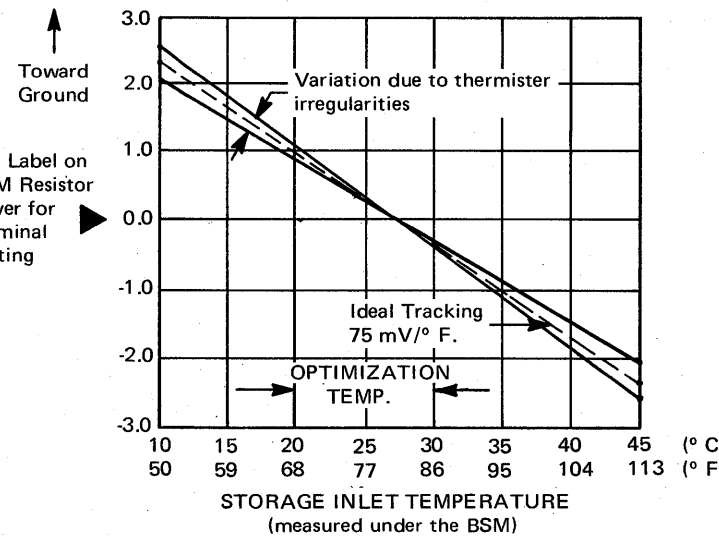
* ±0.84 V in the 3705 or expansion frame when that frame contains a LIB type 3 or LIB type 4.

LIB type 3 - Limited Distance 3a Type 1 (two wire), or Limited Distance 3b Type 1 (four wire)

LIB type 4 - Limited Distance 4a Type 2, or Leased Line 4b (two wire), or Leased Line 4c (four wire)

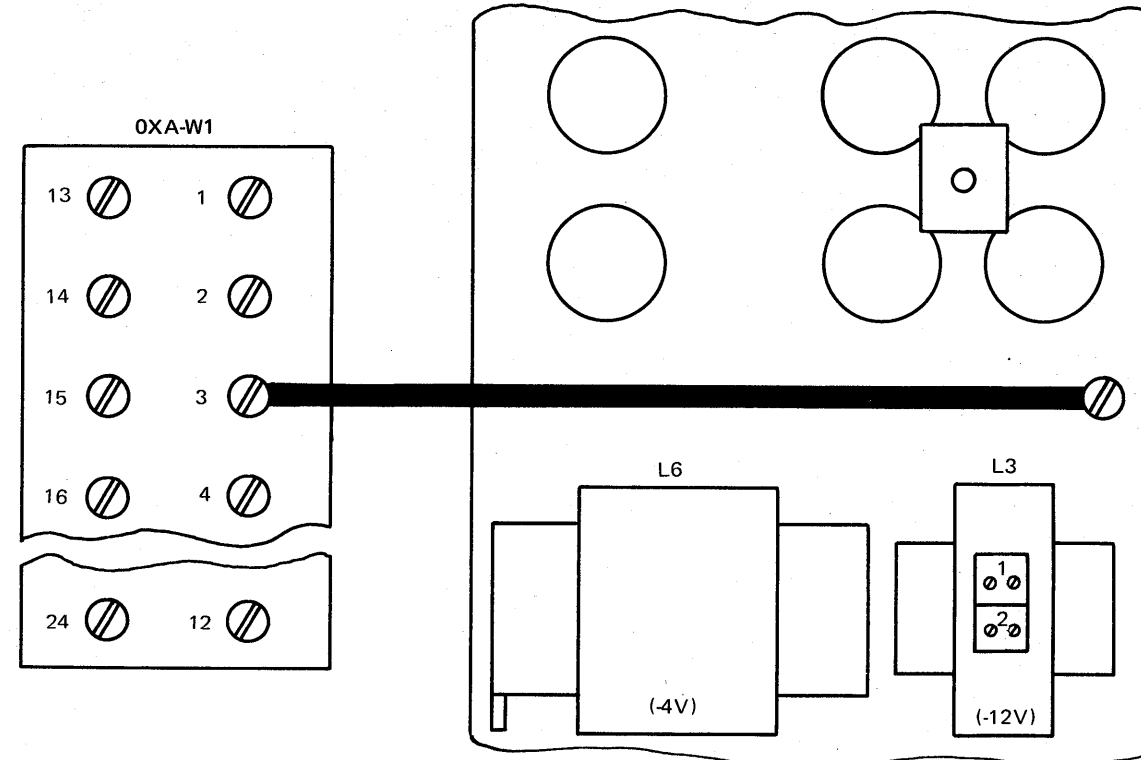
Note:
1. -30 V is not present on the 3705-II basic frame and may or may not be present on 3705-II expansion frames.

1 -30V is temperature compensated as indicated in the following chart.



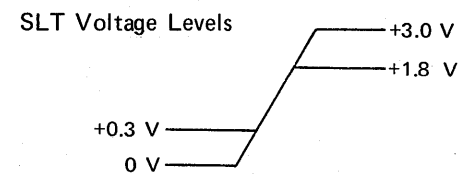
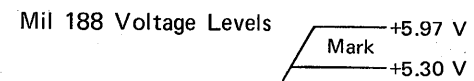
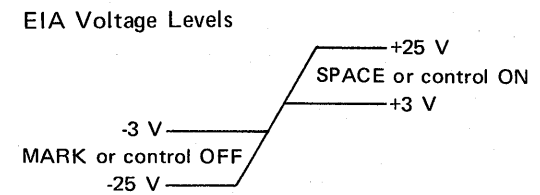
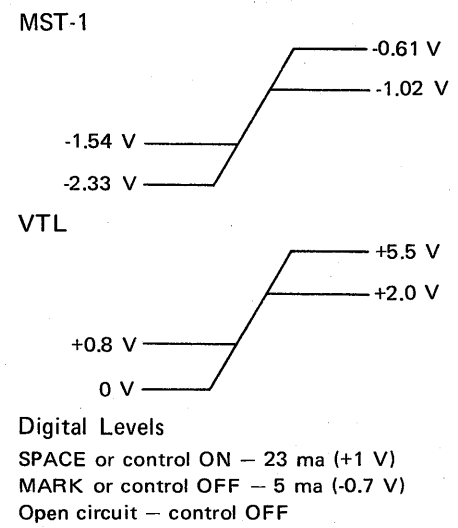
DC COMMON-FRAME GROUND CONNECTION

- dc common and frame ground are tied together in each 3705 and expansion frame by a wire that connects jumper bus 01A-W1-3 to the capacitor plate base. See YZ075 and YZ077.
- Eight jumper assemblies (P/N 1770813) are mounted between frame ground (at board mounting screws) and the dc signal ground pin positions for each logic board located on gate (s) OXA.



Lower section of gate OXF (capacitor bank)

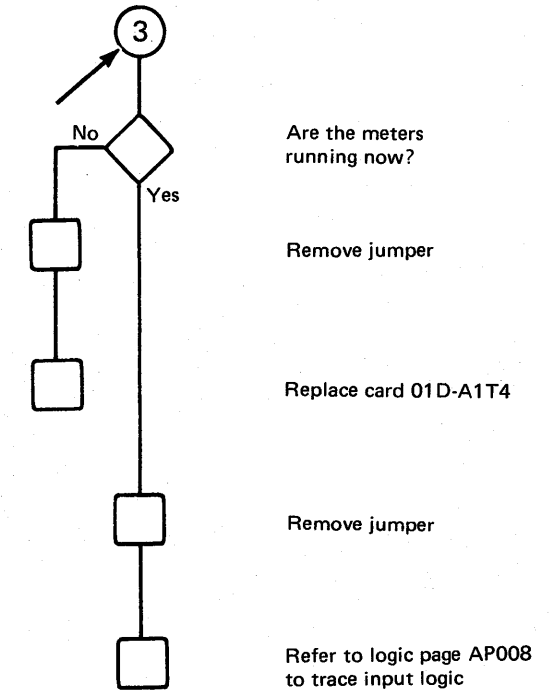
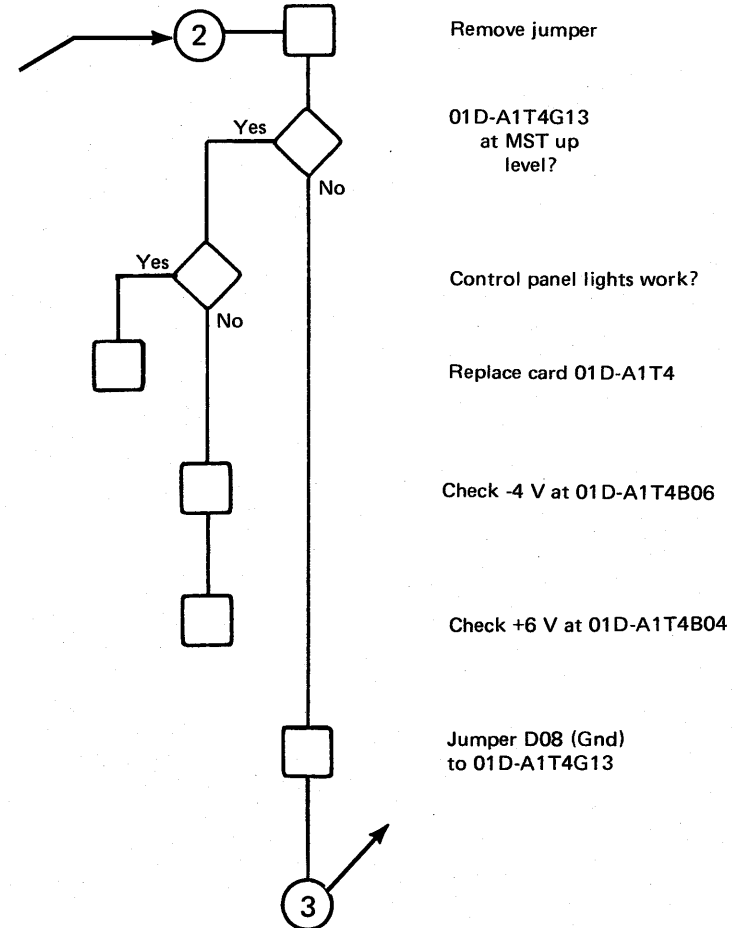
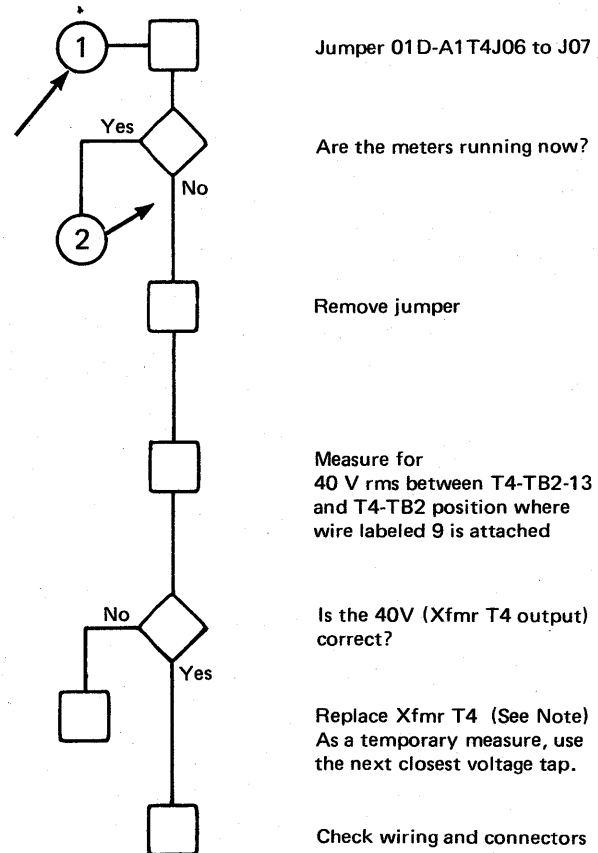
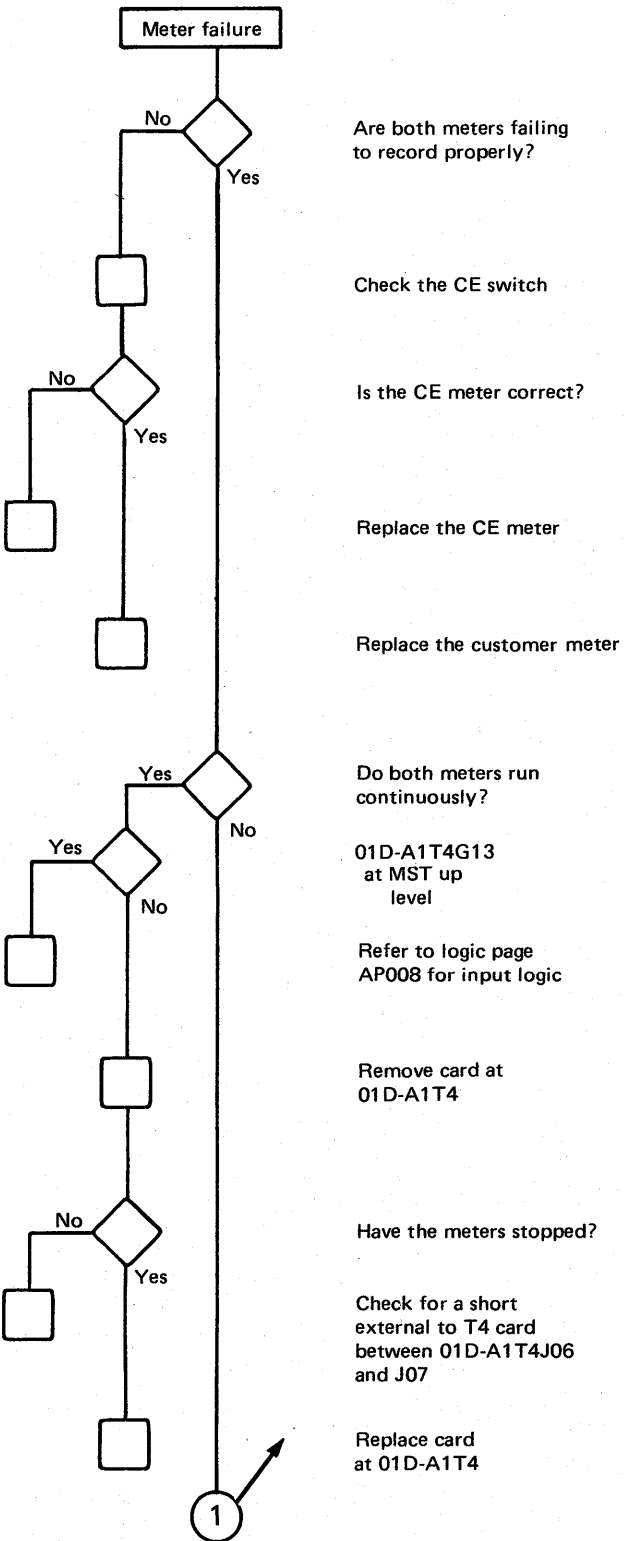
LOGIC VOLTAGE LEVELS



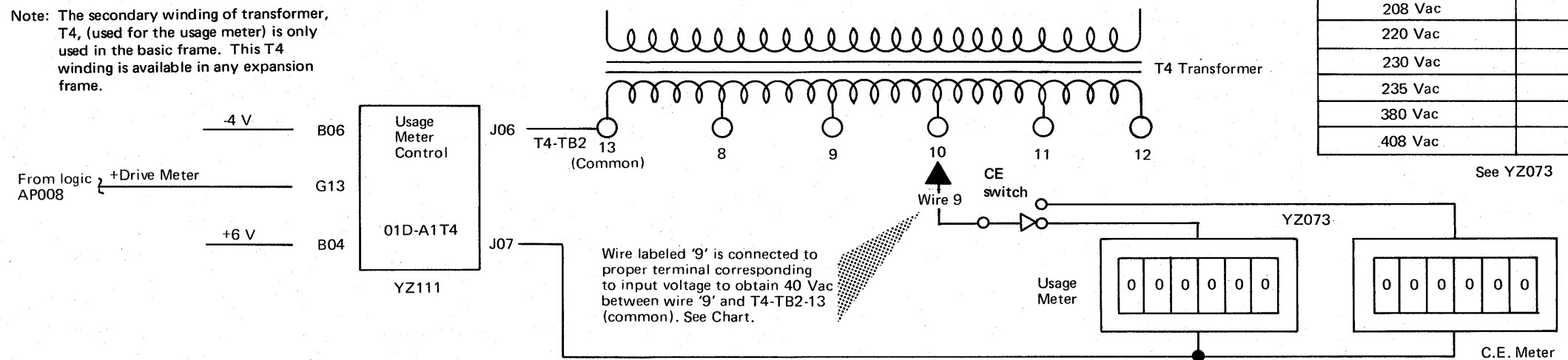
USAGE METER

Note: See D-590 for similar information on a 3705-II with only two or three cards in the OXD power control gate.

See 1-030 for the conditions that cause the usage meter to run.



Note: The secondary winding of transformer, T4, (used for the usage meter) is only used in the basic frame. This T4 winding is available in any expansion frame.



Input Voltage	T4-TB2 terminal
Common	13
200 Vac	12
208 Vac	11
220 Vac	10
230 Vac	9
235 Vac	8
380 Vac	10
408 Vac	8

See YZ073



3705-I POWER-DOWN SEQUENCE

• This page shows the sequence of events that occur during normal power-off operation, (1) when the Local/Remote Power switch is set to the LOCAL position, and the Power Off switch is pressed, or (2) when the Local/Remote Power switch is set to the REMOTE position, and the host CPU brings power down.

1 Remote feature machines do not use the REMOTE/LOCAL POWER switch. Normal power off is the same as the LOCAL position of the REMOTE/LOCAL POWER switch. The Remote power off feature is on Remote Feature 3705's only (see page D-251 for details).

2 01E-RY13 (power-off override) drops 3 to 4 seconds after 01E-RY6 (power on) drops. If the power-down sequence has not been completed by the time the power-off override relay drops, the following events occur:

– 01E-RY13-1 N/O drops 01E-HD1 (contactors on) —see YZ055. The power down sequence continues from **3**

– 01E-RY13-1 N/C picks 01E-RY11 (fault sense) through the 01-RY-2 N/O (± 12 V, -4 V up) which turns on the Power Check light.

This circuit prevents a failure to complete a power-down sequence which might have occurred due to a condition such as a sticking relay.

Contact or action causing dropout	Power Supply Components or Action	Timing Relationships
(Local) Press Power Off Switch YZ053	Power Off Switch or CPU Power Off Switch	
1 (Remote Feature) Decode Output X'79' Byte 0 Bit 1	01E-RY15 (Remote Power Off)	
Power Off Switch	01E-RY6 (Power On)	
(Remote Feature) 01E-RY15-1 NC		
01E-RY6-12 N/C YZ054	Power Off Reset	Floating Ground
01E-RY6-9 YZ053	Power On Light	
(Remote)	0XF-HD2 24 V Seq To Diskette	
01E-RY6-10 (Local) YZ055	0XF-HD2 (Turn On -30V)	Ground put on -30 V at Mem TB1-1
01E-RY6-2 YZ055	01E-RY13 (Power Off Override)	← 3-4 Seconds → 2
0XF-HD2-(1,3) YZ071	-30 V (all frames)	
(Remote 3705) 0XF HD2-2	+24 V for Diskette	
-30 V drops YZ101	-30 V Sense Relays (all frames)	
-30 V Sense Relays in all frames YZ056	01E-RY12	
01E-RY12-4 YZ055	0XF-HD1 (Turn On +6 V)	
0XF-HD1-(1 & 2) YZ071	+6 volts (all frames)	
+6 volts drops YZ101	+6 V Sense Relays (all frames)	
+6 V Sense Relay transistor turnoff YZ101	Ground for -30 V sequence	+1 V (approx) +20 V (approx)
+6 V Sense Relays in all frames YZ056	01E-RY2 (+6 V Up)	
01E-RY2-4 YZ055	01E-HD1 (Contactors On)	
3 01E-HD1-1 YZ052	PPB-K2 (ac to 3705)	
01E-HD1-1 YZ052	PPB-K1 (ac to Expansion Frames 1, 2, and 3)	
PPB-K2 (3705), PPB-K1 Expansion Frames (Domestic) YZ003-005	+12 V, -12 V, -4 V (all frames)	
+12 V, -12 V, -4 V drops YZ101	+12 V, -12V, -4 V Sense Relays (all frames)	
+12 V, -12 V, -4 V Sense Relay transistor turnoff YZ101	Ground for +6 V sequence	+1 V (approx) +20 V (approx)
+12 V, -12 V, -4 V Sense Relays in all frames YZ056	01E-RY1 (+12 V, -12V, -4 V Up)	
01E-RY1-3 YZ053	01E-RY3 (Sequence Complete)	
RY3-1 N/C YZ054	Power-On Reset Controlled	Ground +24 Vdc
	PPB-K1 (EPO)	
	01E-RY9 (Remote)	Remote position of Local/Remote Power Switch
		Local position of Local/Remote Power Switch



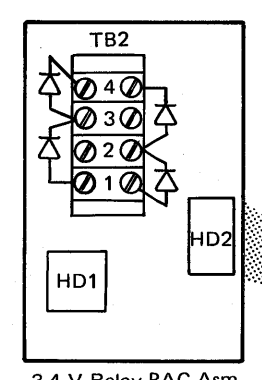
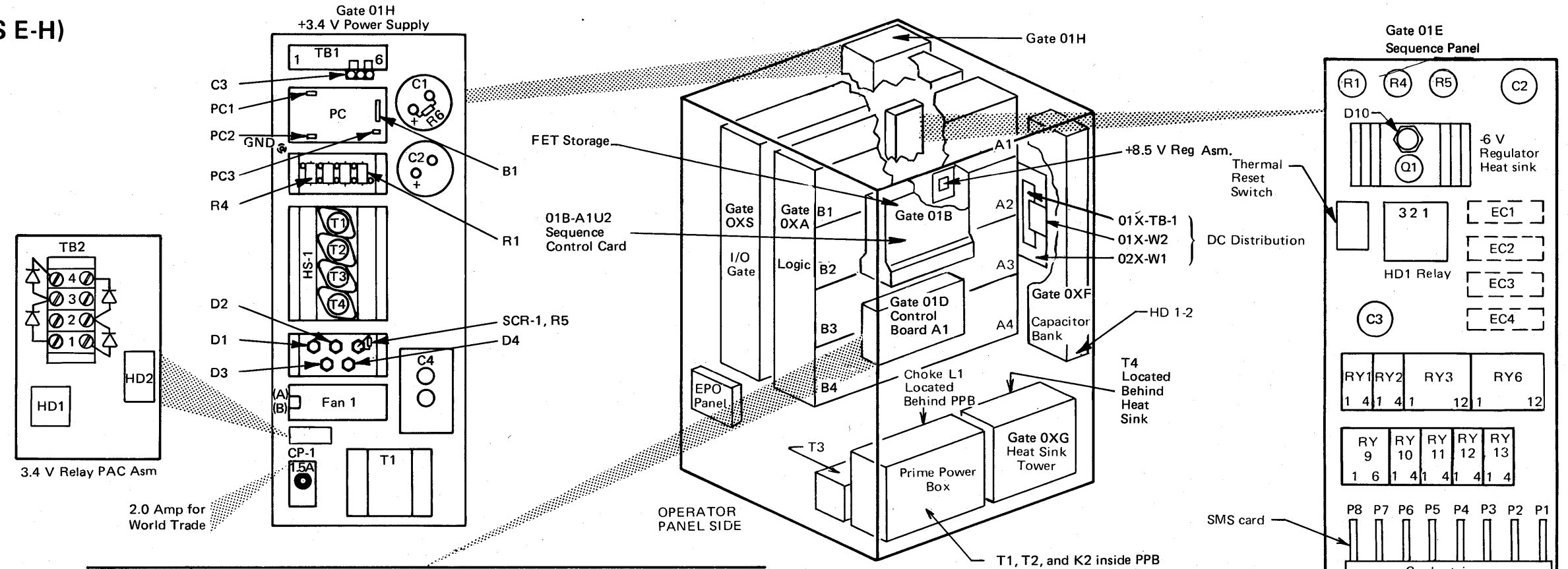
3705-II POWER SUPPLY (BASIC FRAME OF MODELS E-L AND FIRST EXPANSION FRAME OF MODELS E-H)

Note: See D-500 through D-590 for a 3705-II with only two or three cards in the OXD power control gate.

COMPONENT LOCATIONS (See Note)

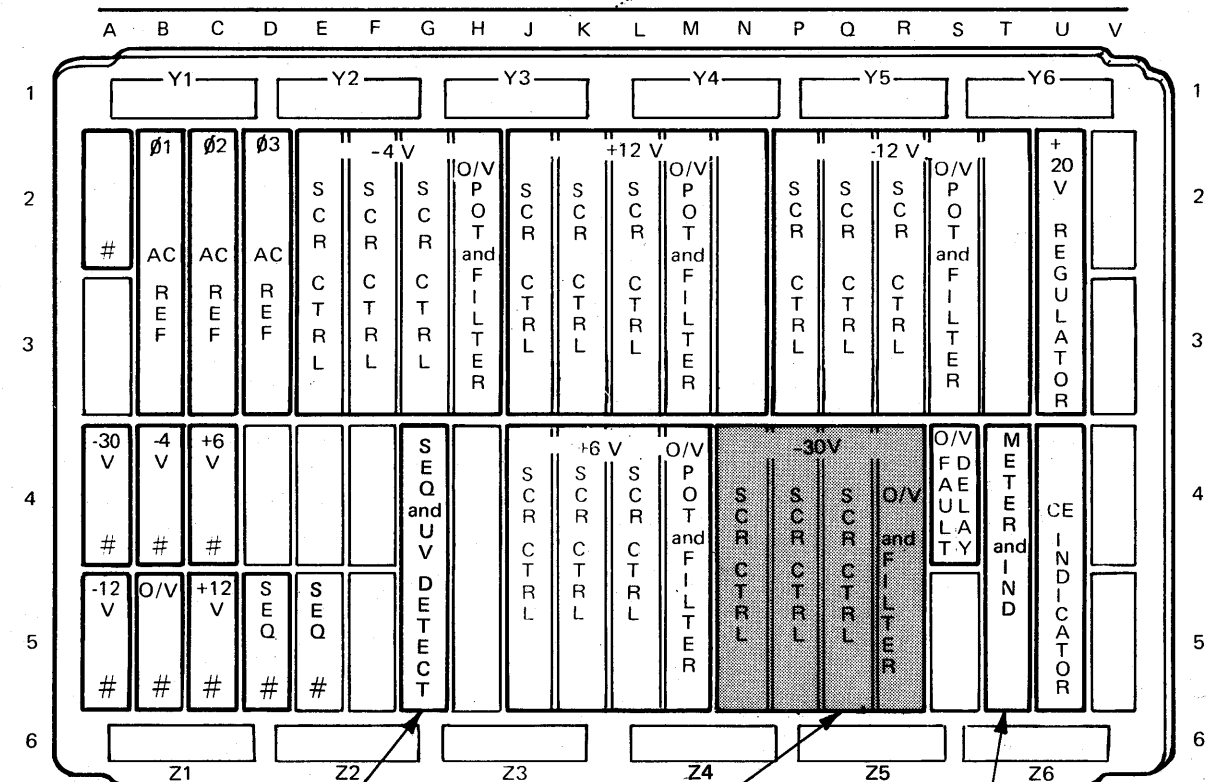
The 3705-II can have several configurations of -30 V power supplies depending on whether the 3705-II was field or factory converted from a 3705-I or was built new at the factory.

- A field or factory converted basic frame retains the -30 V power supply components but the -30 V cards in 01D-A1 are removed. The -4 V shunt on 01A-W1 is not used. The expansion frames retain their -30 V power supply components. The factory convert removes the -30 V cards in OXD-A1 while the field convert leaves them in, but only uses the -30 V for power-up sensing. The -4 V shunt on 0XA-W1 is not used.
- A factory built 3705-II basic frame does not contain a -30 V power supply nor -30 V cards in OXD-A1. The -4 V shunt is not installed.
- The expansion frame physical locations are identical except there is no EPO panel, no sequence panel (gate 01E) nor +3.4 V power supply.
- Refer to the following chart for the component layouts of other units.



Unit	Layout reference
Prime power box	YZ301 sheet 2-3
Heat sink tower (01G)	YZ301 sheet 4-5
Capacitor bank (01F)	YZ301 sheet 6
EPO panel	YZ301 sheet 10
FET storage (01B)	YZ301 sheet 15
I/O Gate (01S)	YZ301 sheet 8
+3.4 V Reg (01H)	YZ301 sheet 16
+8.5 V Reg (01B)	YZ301 sheet 15

- Expansion frame control board (OXD-A1) does not have a card at the T4 position.
- A sequence control card is located on FET storage gate 01B-A1U2.



Note: Component locations for the first expansion frame of Models J-L are shown on D-301.

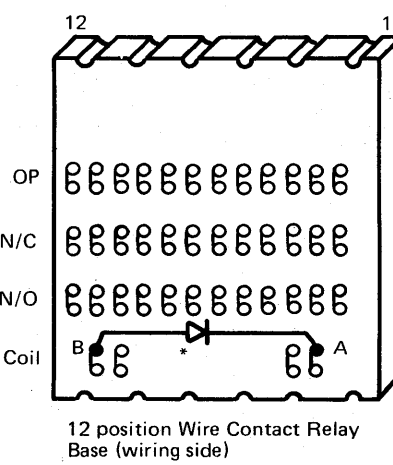
indicates cable
O/V - over voltage
O/C - over current
Expansion frames may have the -30 V control cards. They are always removed in the basic frame and the first expansion frame of 3705-II Models J-L.

SMS card P8 plugs into the sequence panel connector labeled J8

Power Control Cable Plug
P1 - 3705
P2 - 1st expansion frame
P3 - 2nd expansion frame
P4 - 3rd expansion frame

Diode #	01E location
D1	RY6 - 'A' to 'B'*
D2	EC2 - a to e*
D3	RY2 - 'A' to 'B'*
D4	EC2 - b to e*
D5	RY12 - 'A' to 'B'*
D6	RY11 - 'A' to 'B'*
D7	RY10 - 'A' to 'B'*
D8	RY9 - 'A' to 'B'*
D9	EC2 - f to c*

* indicates anode (+) side of diode.





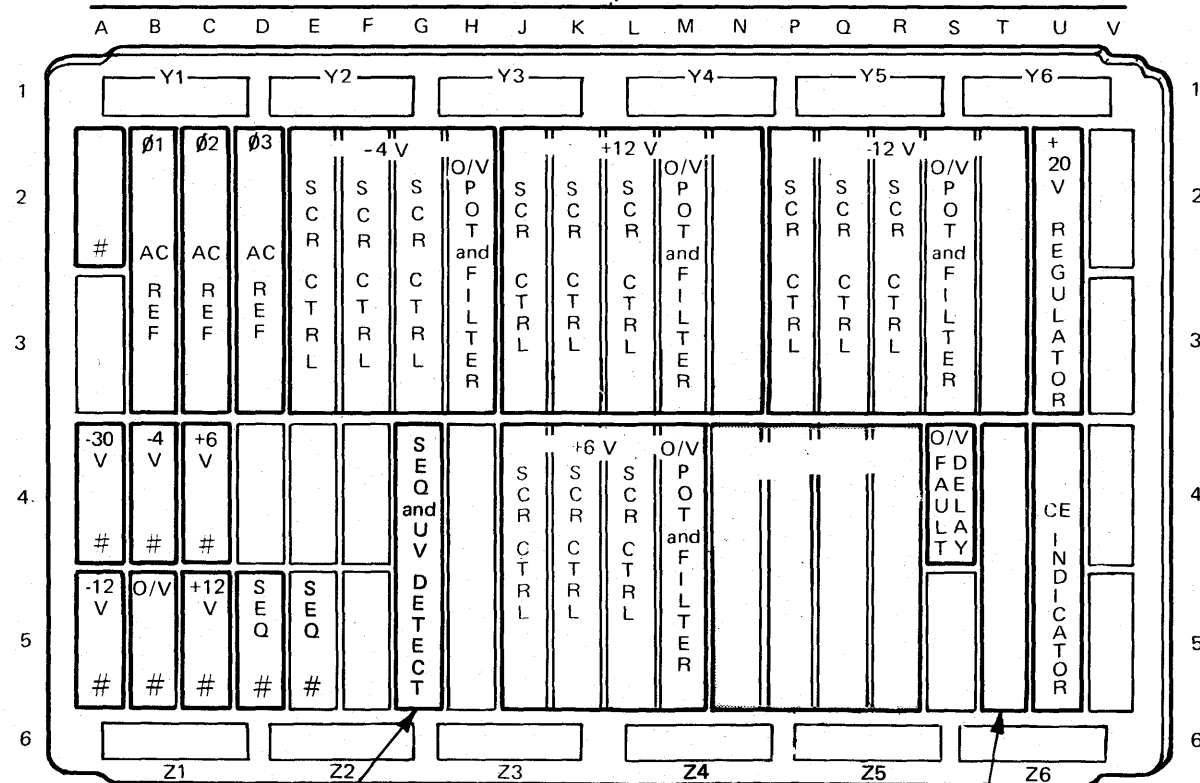
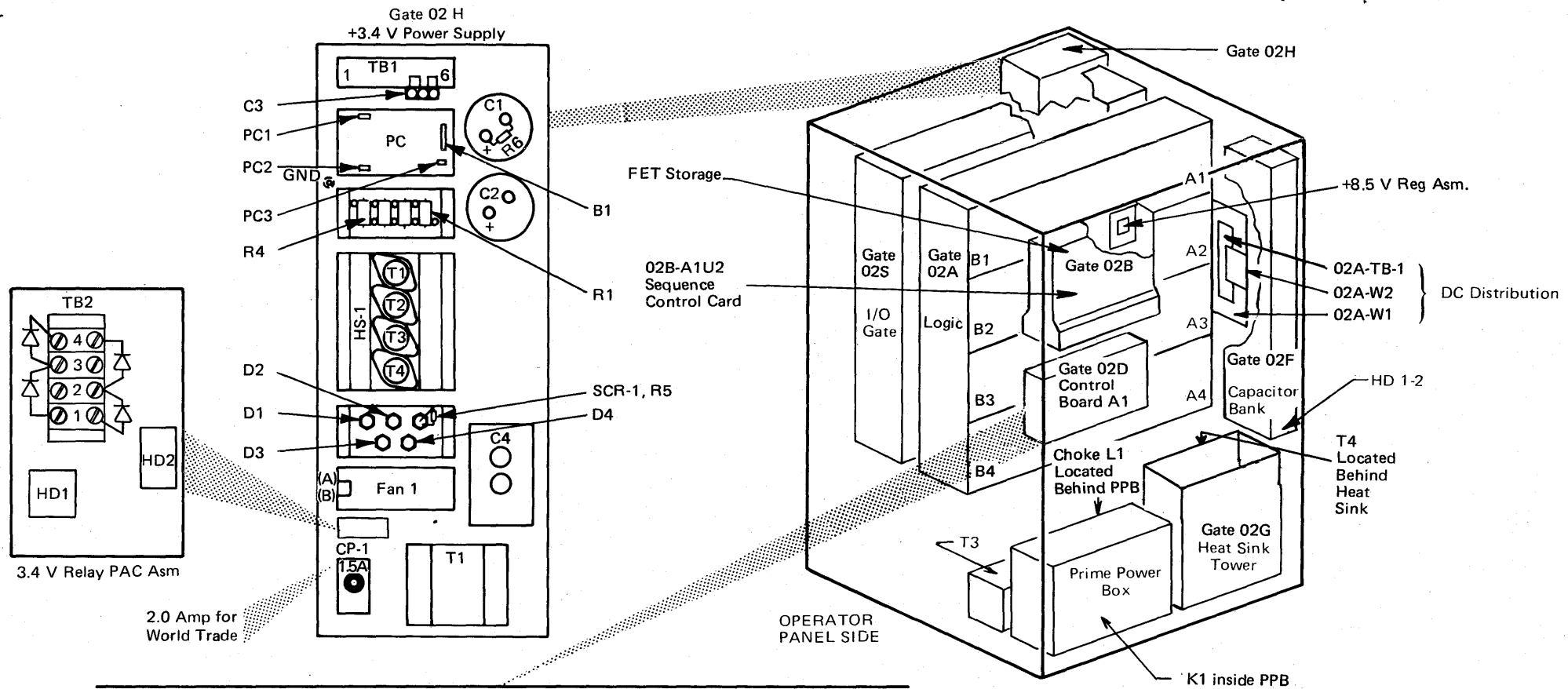
3705-II POWER SUPPLY (FIRST EXPANSION FRAME – MODELS J-L ONLY)

Note: See D-500 through D-590 for a 3705-II with only two or three cards in the OXD power control gate.

COMPONENT LOCATIONS

Unit	Layout reference
Prime power box	YZ301 sheet 3
Heat sink tower (02G)	YZ301 sheet 4-5
Capacitor bank (02F)	YZ301 sheet 6
Control gate 02D	YZ301 sheet 11
FET storage (02B)	YZ301 sheet 15
I/O Gate (01S)	YZ301 sheet 8
+3.4 V Reg (02H)	YZ301 sheet 16
+8.5 V Reg (02B)	YZ301 sheet 15

- A sequence control card is located on FET storage gate 02B-A1U2.

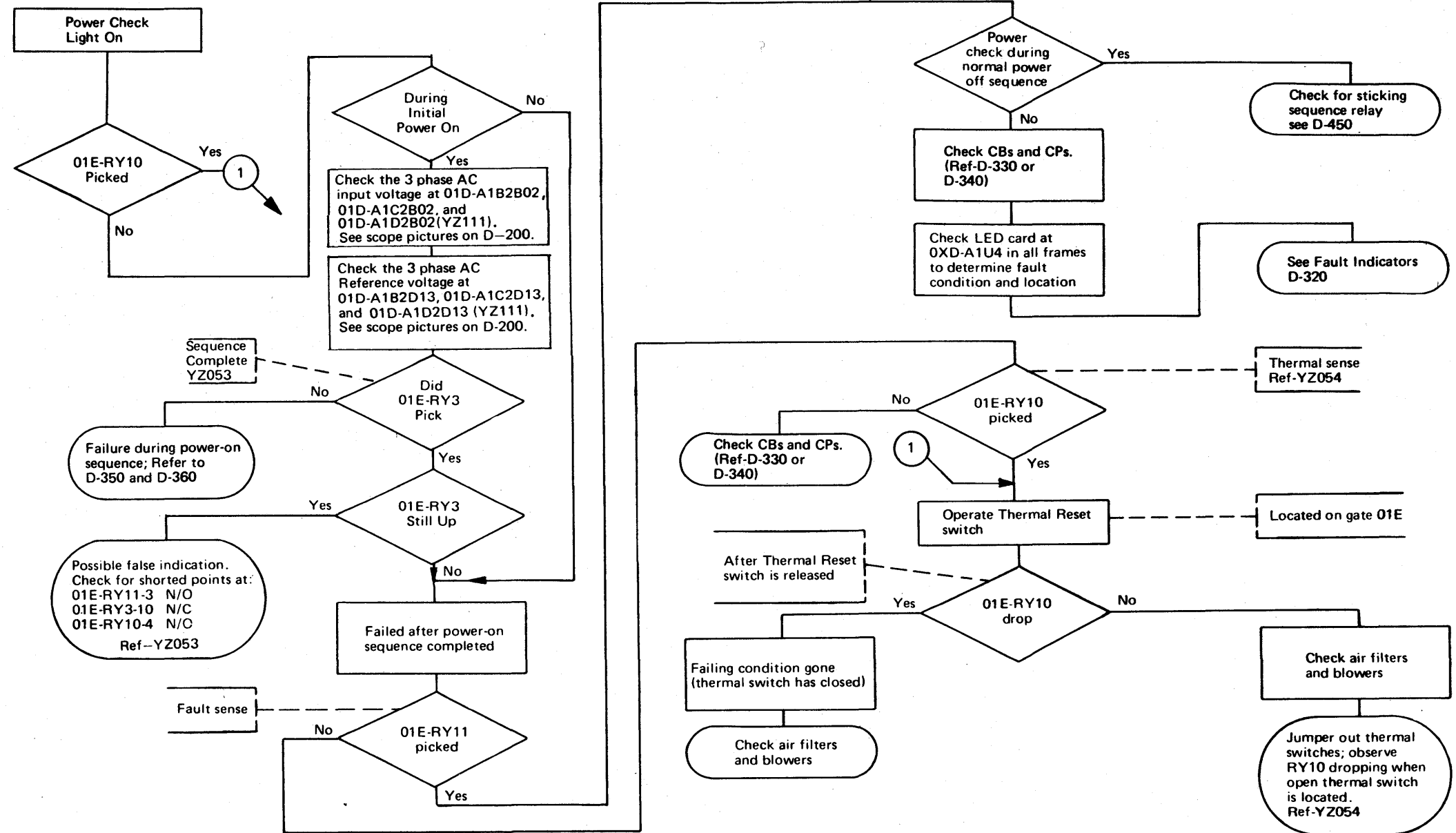


O2D-A1 CONTROL BOARD
indicates cable
O/V - over voltage
O/C - over current
Power Sequence and Under Voltage Detect
CARD SIDE
Meter and Indicator Driver

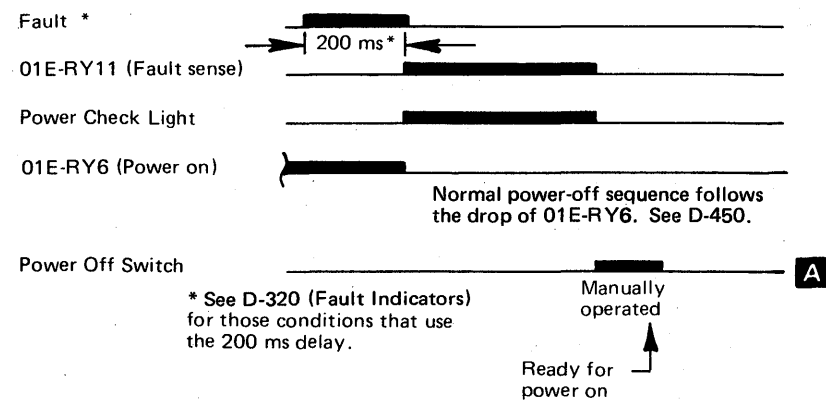
3705-II POWER CHECK

Note: See D-510 for similar information on a 3705-II with only two or three cards in the OXD power control gate. For power MAPs on all 3705-II, refer to D-600.

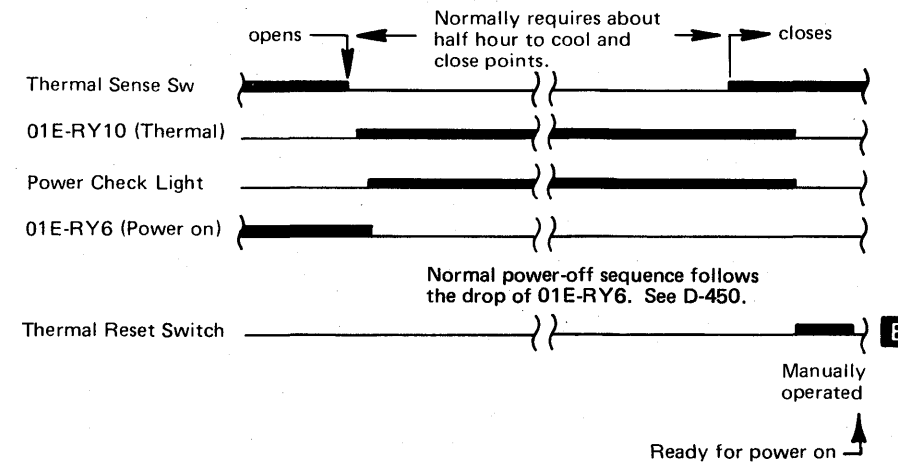
- The Power Check light turns on during a normal power-on sequence and turns off when the sequence has successfully completed.
- A power-off sequence occurs, and the Power Check light turns on for any of the following check conditions:
 - Overvoltage on any logic voltage
 - Undervoltage on any logic voltage
 - Thermal sense on the logic gates, storage gates, and power supplies.
- If the power check resulted from conditions 1-2, reset the Power Check light by pressing the Power Off switch. Power can now be turned on. **A**
- If a normal power-down sequence has not been completed within 3-4 seconds, power is forced off, 01E-RY11 (fault sense) is turned on, and the Power Check light turns on. Reset the Power Check light by pressing the Power Off switch. Power can now be turned on.
- If the power check resulted from a thermal condition, reset the power check light by pressing the Thermal Reset switch (located on the sequence panel-gate 01E) after the thermal contact that detected the thermal condition has cooled off and closed its contact (usually about a half hour). Power can now be turned on. **B**
- Power check logic is on YZ041.



POWER CHECK—FAULT SENSE POWER OFF



POWER CHECK—THERMAL SENSE POWER OFF



3705-II FAULT INDICATORS

Note: See D-520 for fault indicators on a 3705-II with only two or three cards in the OXD power control gate.

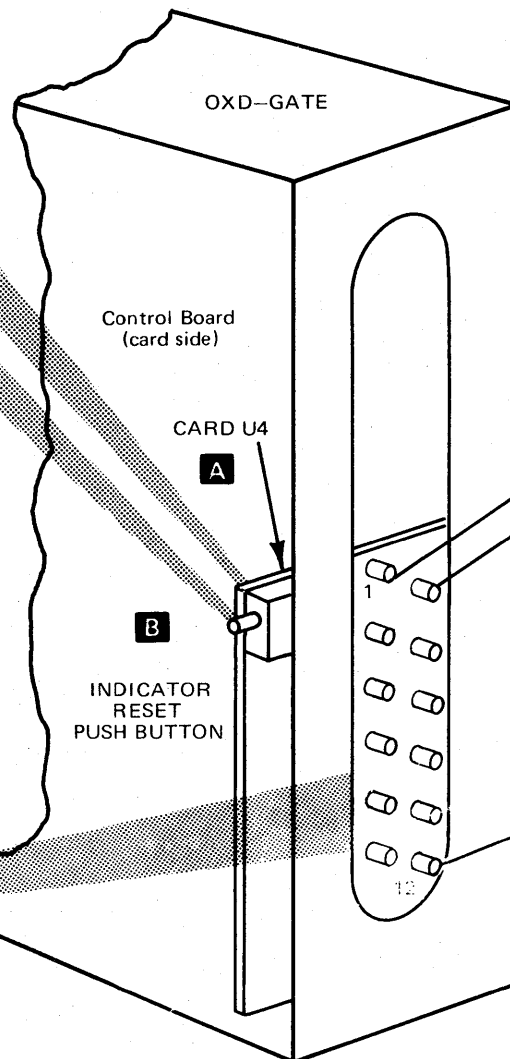
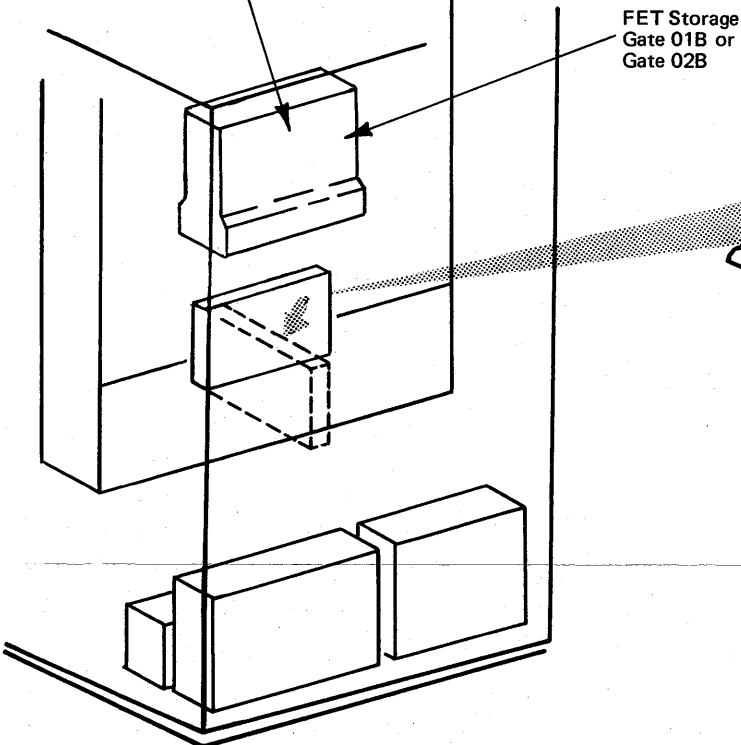
See D-020 for fault indications on expansion frames with an active -30 V power supply.

A There are 12 light-emitting diodes (LEDs) on one card located on the control board at OXD-A1U4. When on, these LEDs indicate the following fault conditions:
Overvoltage on any logic voltage
Undervoltage on any logic voltage

B Once a LED is on, it stays on even if power drops. To turn the LED (s) off, press the Indicator Reset button located on the U4 card.

- The indicators will not turn on during 'power on reset' or while the Power Off push button is pressed. Consequently, the LEDs will not assist you with a power-on sequence problem.
- All fault indications that cause power down turn on the 'power check' light.

Sequence card at 01B-A1U2 or 02B-A1U2 includes fault sensors for +3.4 V, +8.5 V and FET storage -4 V.



LED #	Fault Indication	Causes Power Down	Duration Of Fault Before Power Down	Level at which sense relays pick, LED turns on, under-voltage causes power down	Action To Be Taken If Respective LED Is On
1	+6 V Overvoltage	Yes	200 ms	+6.6 V	See Note 1
2	+12 V Overvoltage	Yes	200 ms	+14 V	
3	-12 V Overvoltage	Yes	200 ms	-14 V	
4	+8.5 V Overvoltage	Yes	Immediate	+9.7 V	See Note 2
5	-4 V Overvoltage	Yes	200 ms	-4.7 V	See Note 3
6	+3.4 V Overvoltage	Yes	Immediate	+4 V	See Note 4
7	+3.4 V Undervoltage	Yes	Immediate	2.8 V	
8	-4 V Undervoltage	Yes	Immediate	-3.0 V to -3.5 V	See Note 3
9	+6 V Undervoltage	Yes	Immediate	+5.4 V to +5.59 V	See Note 1
10	+12 V Undervoltage	Yes	Immediate	+9.0 V to +10.0 V	
11	-12 V Undervoltage	Yes	Immediate	-8.7 V to -10.3 V	See Note 2
12	+8.5 V Undervoltage	Yes	Immediate	2.8 V	

Notes:

- Follow procedure for checking SCRs in $\pm 12V$ or +6 V supplies on D-150.
- Follow procedure for checking +8.5 V on D-372.
- Follow procedure for checking SCRs in -4 V supply on D-170.
- Follow procedure for checking +3.4 V supply on D-371.

Service Note:

If an undervoltage LED is on but the power will not remain on to scope the associated SCRs, the voltage sequence can be made to hang up by removing the jumper between 01B-A1V4D03 and D04 or 02B-A1V4D03 and D04 or the filter card for the next voltage to sequence on. For example: to scope the +6 V SCRs, remove the jumper between 01B-A1V4D03 and D04 or 02B-A1V4D03 and D04; to scope the $\pm 12 V$, -4V, remove the +6 filter card.

Power on voltage sequence:

- $\pm 12 V$, -4 V
- +6 V
- +8.5 V, +3.4 V (sequenced via a signal from 01F-HD2 to 01B-A1V4D03 or 02F-HD2 to 02B-A1V4D03).

3705-II POWER-DISTRIBUTION—BASIC FRAME

Note: See D-530 for power distribution in a 3705-II basic frame with only three cards in the O1D power control gate.

Those 3705-II basic frames that were field/factory converted from 3705-I contain -30 V power supply components but the -30 V has been crippled by the removal of the control cards from O1D-A1.

PPB-CB1 (Main CB)

Frames Attached	208/230 V 60 Hz	220/235 V 50 Hz (Delta)	380/408 V 50 Hz (Wye)	200 V 60 Hz (Japan)	200 V 50 Hz (Japan)
3705	15 A	15 A	15 A	15 A	15 A
1st expansion frame	30 A	30 A	15 A	30 A	30 A
2nd expansion frame	40 A	40 A	30 A	40 A	40 A
3rd expansion frame	50 A	50 A	30 A	50 A	50 A

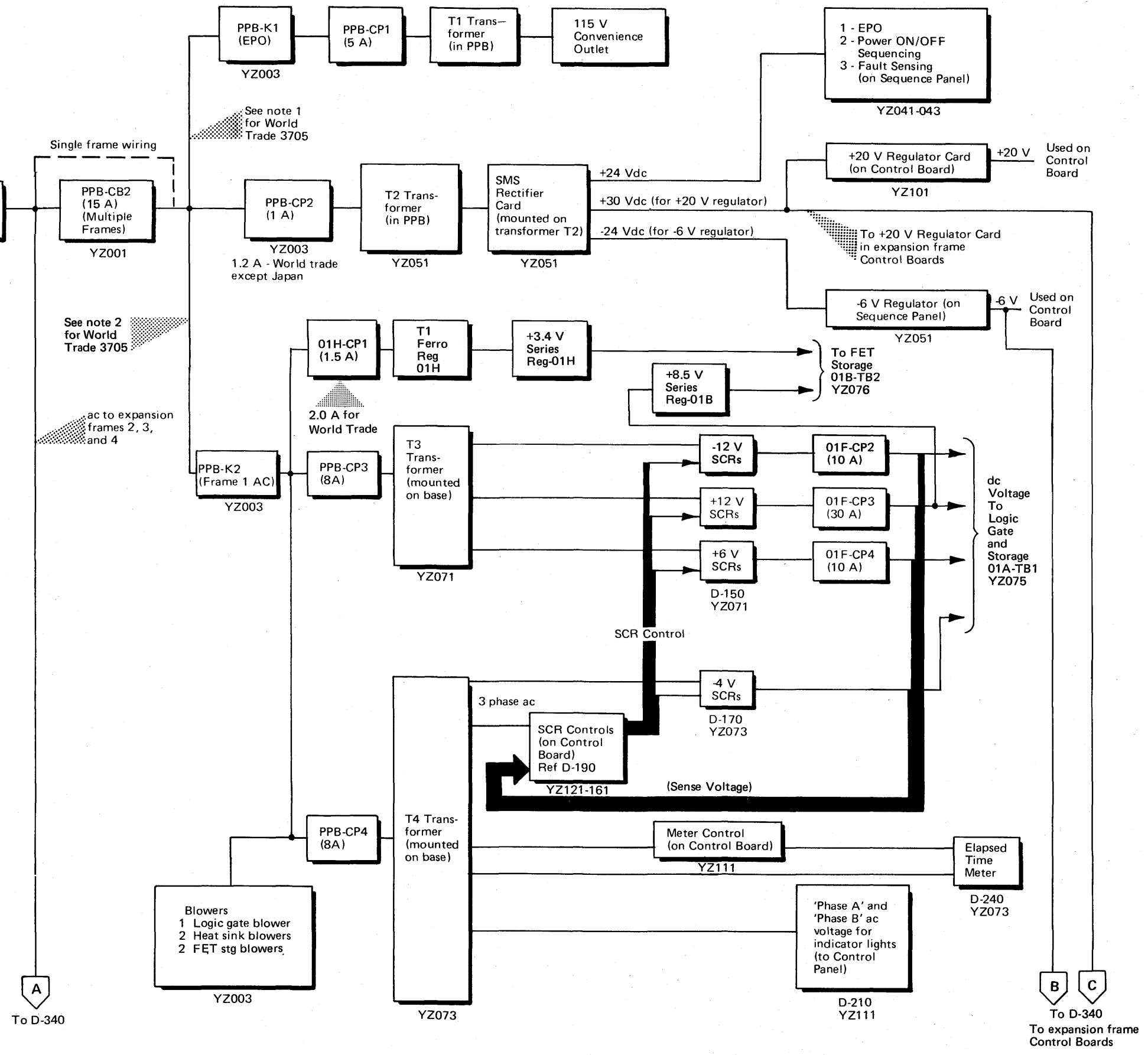
NOTES FOR WORLD TRADE

Note 1
 For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, jumper terminal block PPB-TB2 to obtain 220/235 V for the convenience outlet (see YZ013).
 For 200 V 60 Hz power (Japan), use PPB-CP1 (5A) with transformer T1 to obtain 100 V for the convenience outlet (see YZ023).
 For 200 V 50 Hz power (Japan), only the PPB-K1 contactor is used with the convenience outlet voltage of 200 V (see YZ033).

Note 2
 For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, terminal block PPB-TB2 is jumpered to obtain 220/235 V for all blowers and to connect the neutral of the Wye input power to transformers T3 and T4.
 (All blowers are single phase).

LEGEND

- PPB — Prime power box
- CP — Circuit protector
- CB — Circuit breaker
- SCR — Silicon controlled rectifier



To D-340

Blowers
 1 Logic gate blower
 2 Heat sink blowers
 2 FET stg blowers

YZ003

YZ073

YZ111

D-210 YZ111

'Phase A' and 'Phase B' ac voltage for indicator lights (to Control Panel)

D-240 YZ073

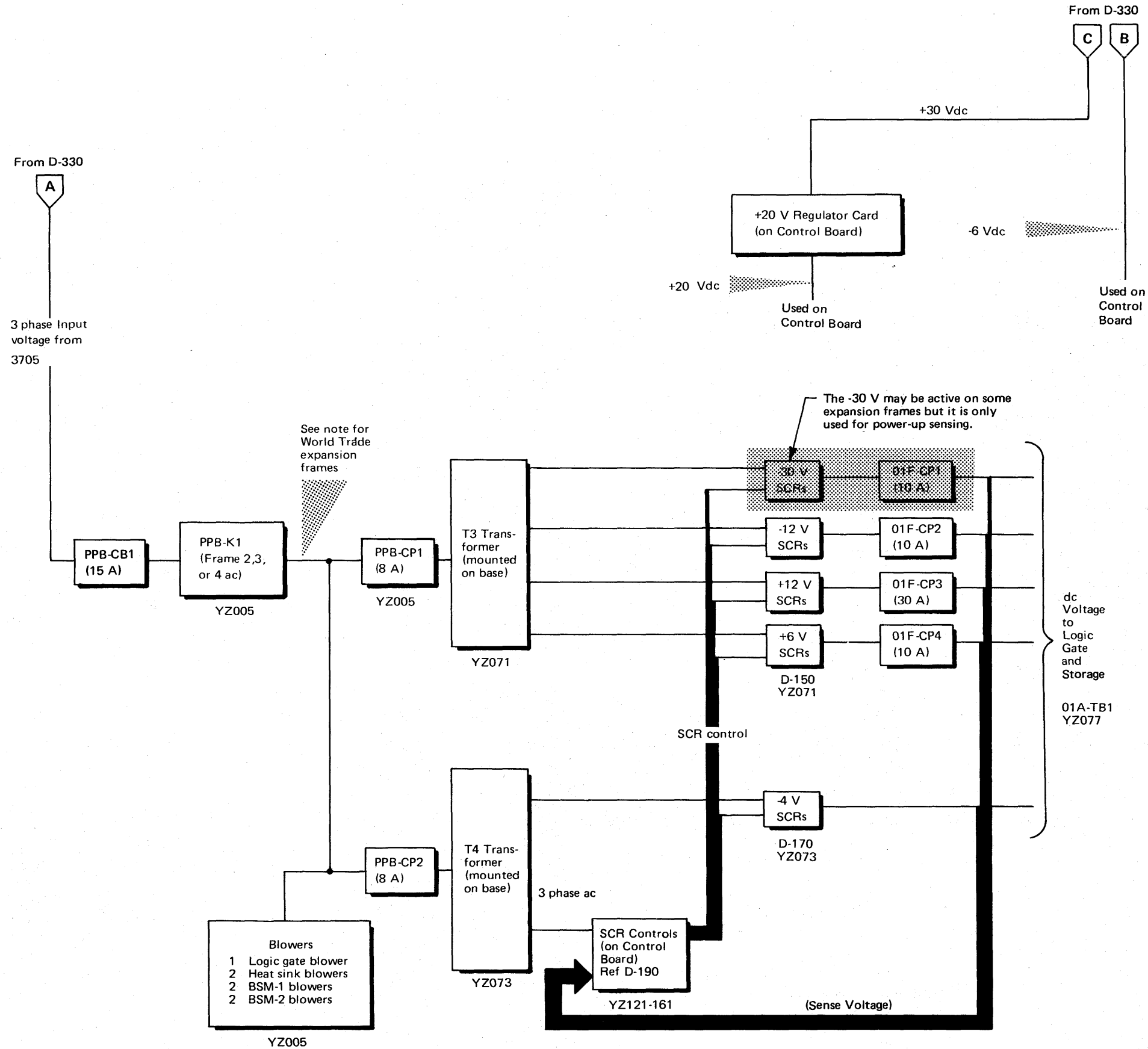
To expansion frame Control Boards

3705-II EXPANSION FRAME POWER DISTRIBUTION

Note: See D-535 for power distribution in a 3705-II expansion frame with only two cards in the OXD power control gate.

NOTE FOR WORLD TRADE

- 220/235 V (Delta) or 380/408 V (Wye) 3 phase 50 Hz expansion frames are jumpered to obtain 220/235 V for all blowers and to connect the neutral of the Wye input power to transformers T3 and T4. See YZ015.



FET STORAGE POWER ELEMENTS

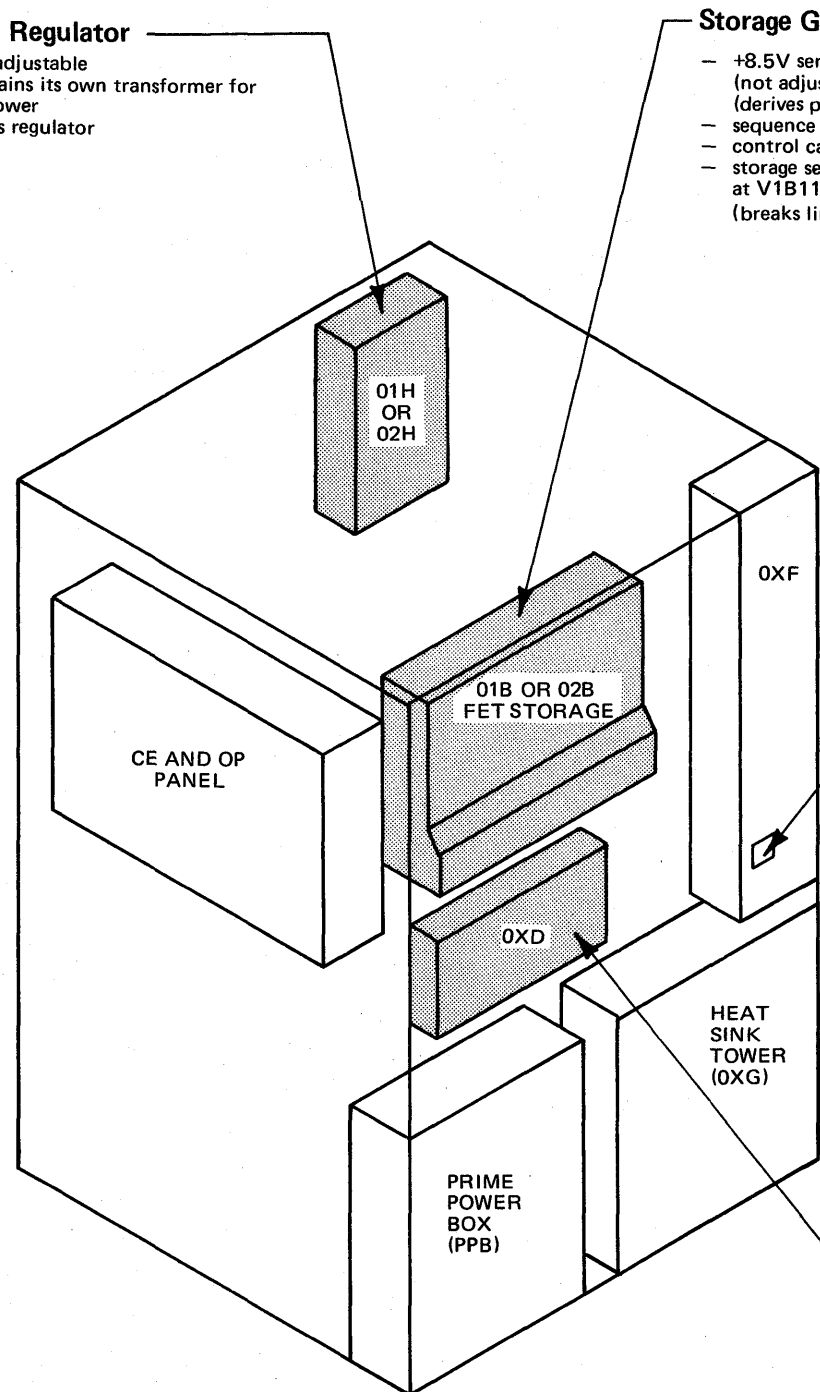
Note: Not applicable to a 3705-II with only two or three cards in the OXD power control gate. Refer to D-505.

+3.4V Regulator

- not adjustable
- contains its own transformer for ac power
- series regulator

Storage Gate

- +8.5V series regulator (not adjustable) (derives power from +12V)
- sequence control card (U2)
- control cables (V2 & V4)
- storage sequence interrupt jumper at V1B11 - V1B13 (breaks line to 01F-HD1 or 02F-HD1)



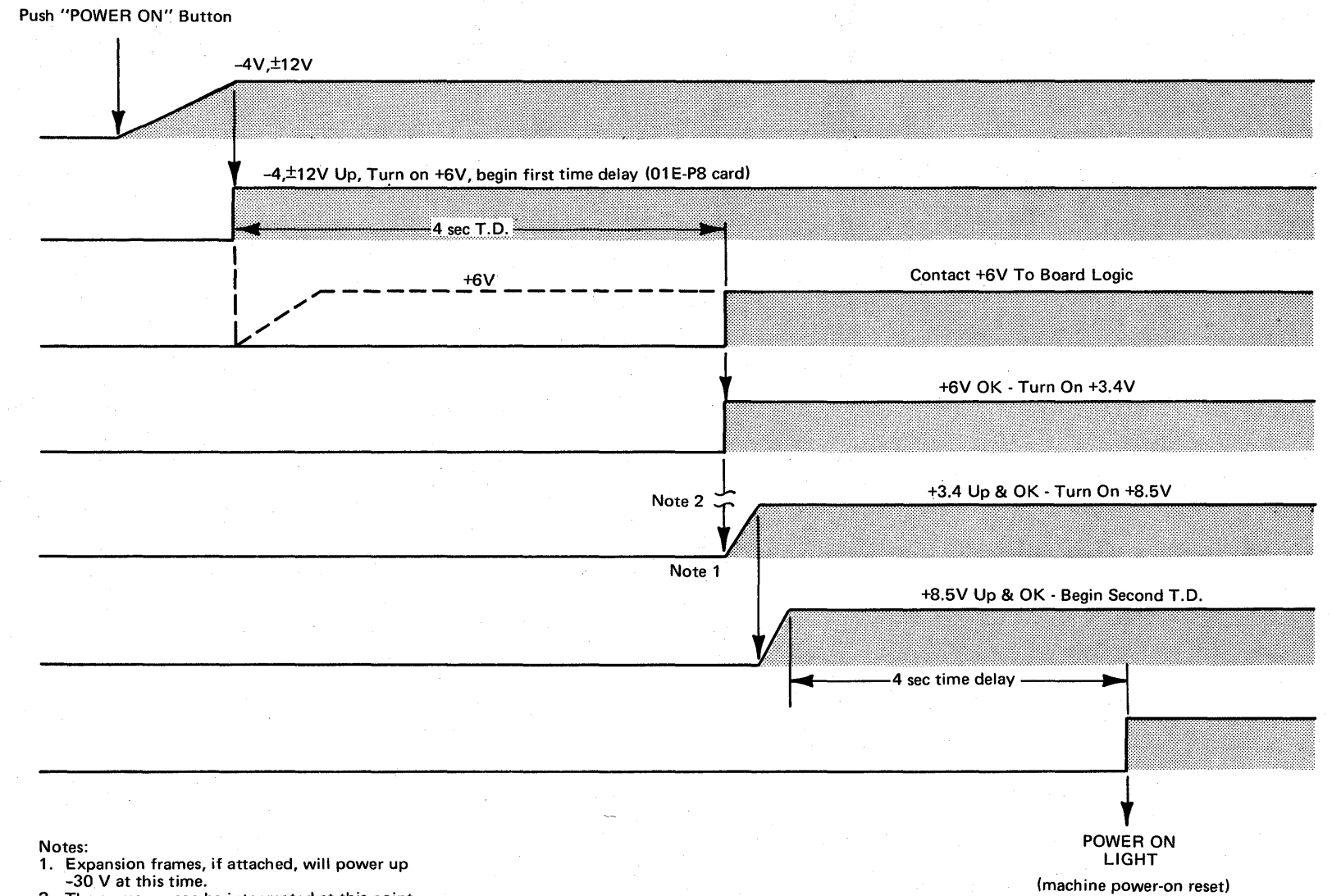
Relay 01F-HD1 or 02F-HD1

- contacts +6V to load
- also starts sequencing of +3.4V & +8.5V

Swing Out Power Gate

- storage power sequence cable plugs into OXD-E5
- includes storage voltage fault indicators

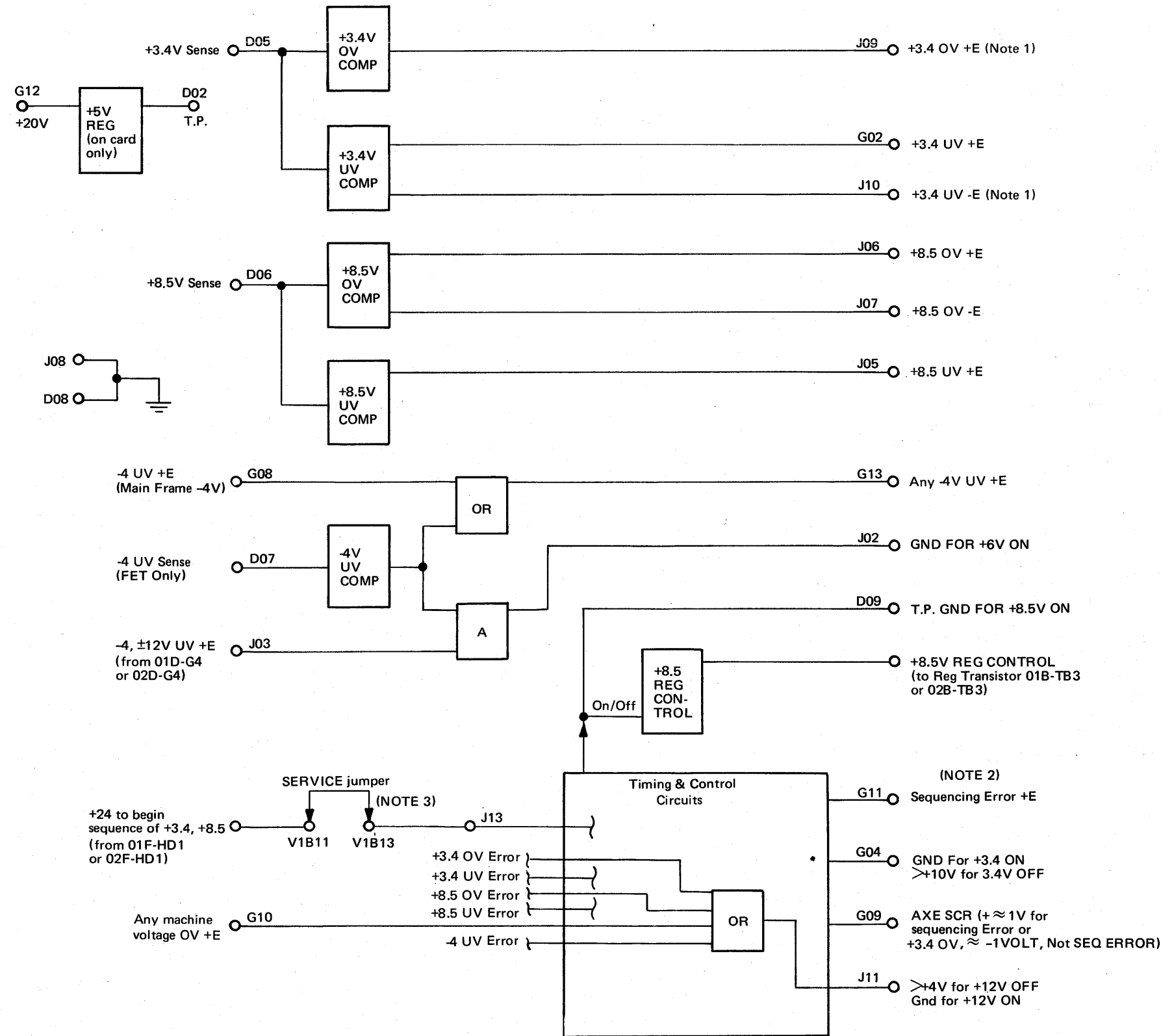
Simplified Power On Sequence



- Notes:
1. Expansion frames, if attached, will power up -30 V at this time.
 2. The sequence can be interrupted at this point as a service aid to decide if a power problem is before or after this point. If array cards are removed the +3.4V and +8.5V can be manually operated.

FET STORAGE POWER ELEMENTS (PART 2)

01B-A1U2 or 02B-A1U2 Power Sequence Card Function Diagram



- Notes:
1. +E is 15V to 22V. -E is +2V to -6V.
 2. +E if +8.5V or +3.4V don't come up within 2 sec after +24V appears at J13 or if +3.4V goes OVER VOLTAGE.
 3. Jumper may be removed to manually exercise +8.5V and +3.4V according to flow chart.

3705-II POWER-ON SEQUENCE

Note: See D-540 for power on sequence of a 3705-II with only two or three cards in the OXD power control gate.

- Shows the sequence of events that occur during normal power-on operation (1) when the Local/Remote Power switch is set to the LOCAL position, and the Power On switch is depressed, or (2) when the Local/Remote Power switch is set to the REMOTE position, and the host CPU brings power up.

1 The 4 second delays are located on P8 on the Sequence Panel gate 01E.

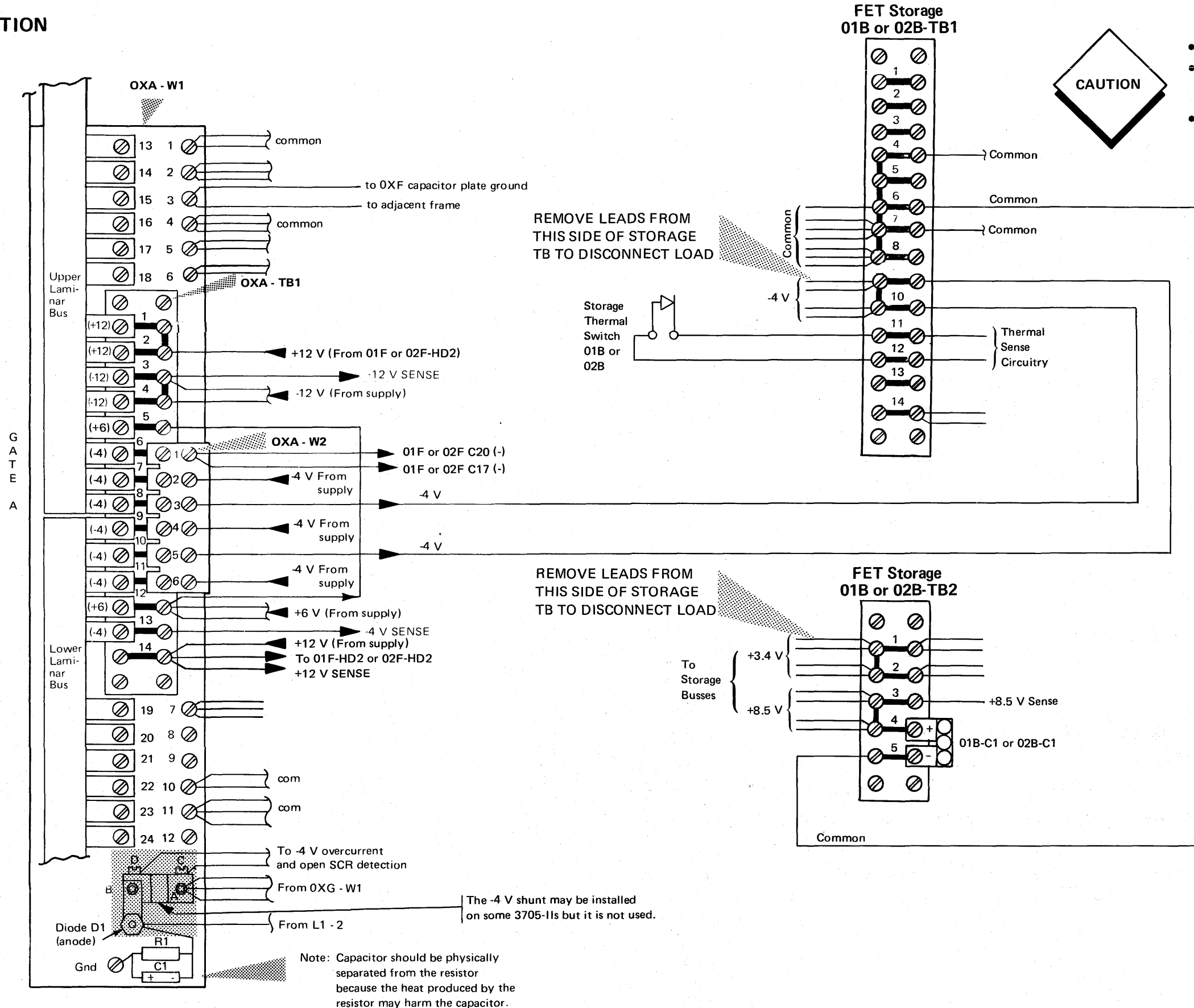
Contact or action causing pickup	Power Supply Components or Action	Timing Relationships	
EPO-J (1, 2, 3, or 4)	YZ051 PPB-K1 (EPO)	(+24 Vdc For Relays)	D-420
PPB-K1 #1 point	YZ051 01E-RY9 (Remote)	Remote position of Local/Remote Power Switch	
Press Power On Switch	YZ053 Power On switch or CPU Power On	Local position of Local/Remote Power Switch	
Local Power On Switch or CPU Power On	YZ053 01E-RY6 (Power On)		
01E-RY6-9	YZ053 Power Check Light		
01E-RY6-12 N/O	YZ054 Power On Reset		
01E-RY6-2	YZ055 01E-RY13 (Power Off Override)		
01E-RY6-11	YZ055 01E-HD1 (ac contactors on)		D-390
01E-HD1-1	YZ052 PPB-K2 (ac to 3705)		
PPB-K2 #4 point (3705)	YZ052 PPB-K1 (ac to Expansion frame #1)		
PPB-K1 #4 point (Expansion frame 1)	YZ052 PPB-K1 (ac to Expansion frame #2)		
PPB-K1 #4 point (Expansion frame 2)	YZ052 PPB-K1 (ac to Expansion frame #3)		
ac applied to each frame	YZ005 +12 V, -12 V, -4 V (every frame)		
+12 V, -12 V, -4 V up in each frame	YZ101 +12 V, -12 V, -4 V sense relays		
Transistor that picks +12 V, -12 V, -4 V sense relay	YZ101 Ground for +6 V sequence	+20 V approx. +1 V (approx.)	
+12 V, -12 V, -4 V sense relay points in each frame	YZ056 01E-RY1 (+12 V, -12 V, -4 V up)	1 → 4 sec. delay ←	D-380
01E-RY1-4	YZ055 0XF-HD1 (Turn on +6 V); begin +3.4 V and +8.5 V sequence		
+3.4 V and +8.5 V	+8.5 V sense relay		
+8.5 V sense relay Note 1	01E-RY12 (+8.5 V up)	Note 1	
0XF-HD1-(1&2)	YZ071 +6 volts (all frames)		
+6V up in each frame	YZ101 +6 V sense relays		
Transistor that picks +6 V sense relay	YZ101 Ground for -30 V sequence Note 2	+20 V approx. +1 V (approx.)	
+6 V sense relay points in each frame	YZ056 01E-RY2 (+6 V up)		D-370
01E-RY2-3	YZ055 01F-HD2 (Apply +12 V to logic) 0XF-HD2 (Turn on -30 V)—Note 2		
0XF-HD2-(1, 2, 3)	YZ071 Apply +12 V to all logic. Apply -30 V—Note 2		
-30 V up in each expansion frame—Note 2	YZ101 -30 V sense relays—Note 2		
RY3-1 N/C	YZ054 Power-On Reset Controlled	+24 Vdc (Blocks Power Fault Indicators) Ground	
+8.5 V sense relay point in basic frame and -30 V sense relay points in each expansion frame	YZ056 01E-RY12 (+8.5 V up)		
01E-RY12-3	YZ053 01E-RY3 (Sequence complete)	1 → 4 sec. delay ←	D-360
01E-RY3-10 N/O	YZ053 Power ON Light		

- Notes:
- The +8.5 V sense relay picks 01E-R12 when the 3705-II has no expansion frames, or the expansion frames contain no -30 V power supplies.
 - Applies to expansion frames that have a -30 V power supply.

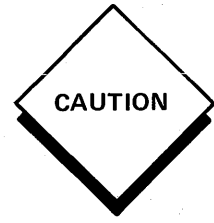


3705-II DC VOLTAGE DISTRIBUTION

Note: See D-550 for DC voltage distribution on a 3705-II with only two or three cards in the OXD power control gate.



- Do not remove any of the wires labeled SENSE
- Do not remove any of the terminal board (TB) jumpers which connect a voltage with its sense lead.
- Do not bend the laminar bus tab too sharply because it may crack upon straightening.



Logic YZ076

REMOVE LEADS FROM THIS SIDE OF STORAGE TB TO DISCONNECT LOAD

REMOVE LEADS FROM THIS SIDE OF STORAGE TB TO DISCONNECT LOAD

The -4 V shunt may be installed on some 3705-II's but it is not used.

Note: Capacitor should be physically separated from the resistor because the heat produced by the resistor may harm the capacitor.

3705-II POWER-DOWN SEQUENCE

Note: This power down sequence does not apply to a 3705-II with only two or three cards in the OXD power control gate.

- This page shows the sequence of events that occur during normal power-off operation, (1) when the Local/Remote Power switch is set to the LOCAL position, and the Power Off switch is pressed, or (2) when the Local/Remote Power switch is set to the REMOTE position, and the host CPU brings power down.

1 01E-RY13 (power-off override) drops 3 to 4 seconds after 01E-RY6 (power on) drops. If the power-down sequence has not been completed by the time the power-off override relay drops, the following events occur:

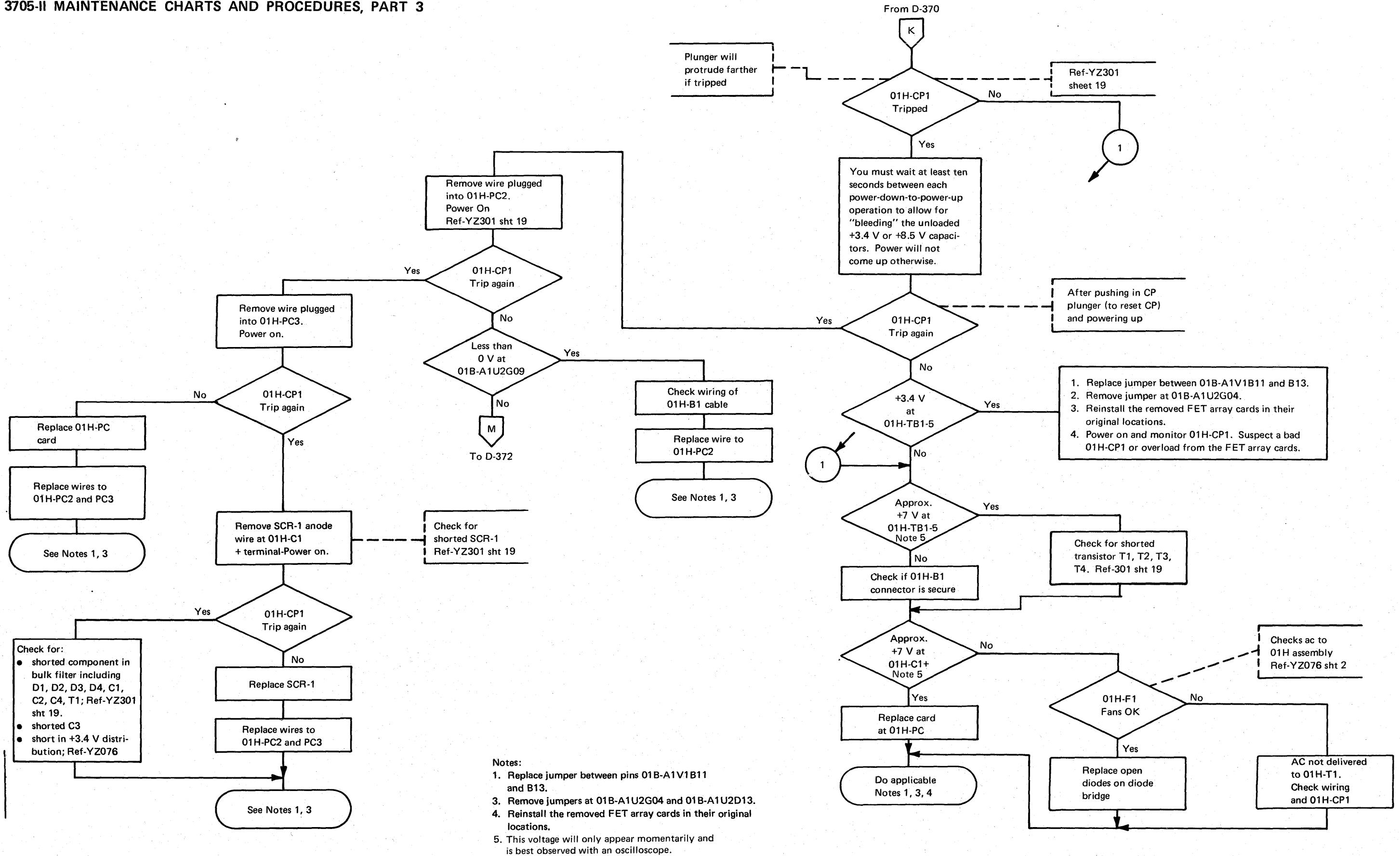
- 01E-RY13-1 N/O drops 01E-HD1 (contactors on) —see YZ055. The power down sequence continues from **2**
- 01E-RY13-1 N/C picks 01E-RY11 (fault sense) through the 01-RY-2 N/O (± 12 V, -4 V up) which turns on the Power Check light.

This circuit prevents a failure to complete a power-down sequence which might have occurred due to a condition such as a sticking relay.

Notes:

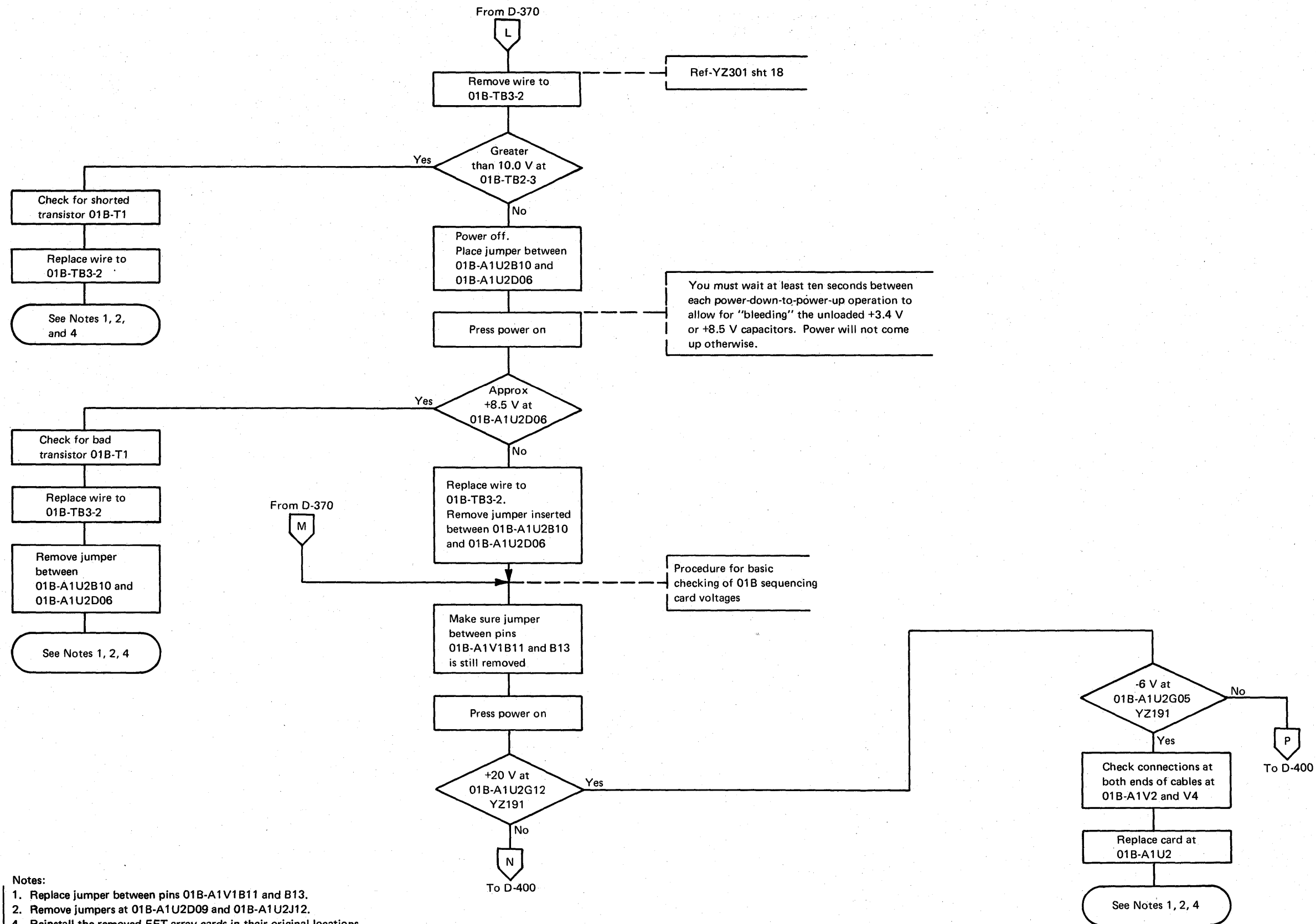
- Applies to expansion frames that have a -30 V power supply.
- When the 3705-II has no expansion frames, 01E-RY6-6 drops 01E-RY12.

Contact or action causing dropout	Power Supply Components or Action	Timing Relationships
(Local) Press Power Off Switch YZ053	Power Off Switch or CPU Power Off Switch	
Power Off Switch	01E-RY6 (Power On)	
01E-RY6-12 N/C YZ054	Power Off Reset	Floating Ground
01E-RY6-9 YZ053	Power On Light	
01E-RY6-10 (Local) YZ055	01F-HD2 (Apply +12 V to logic)—basic frame 0XF-HD2 (Turn On -30 V)—Note 1	Ground put on -30 V at Mem TB1-1 Note 1
01E-RY6-2 YZ055	01E-RY13 (Power Off Override)	3-4 Seconds 1
0XF-HD2-(1,3) Note 1 YZ071	-30 V (all expansion frames with -30 V)	Note 1
-30 V drops Note 1 YZ101	-30 V Sense Relays (all expansion frames with -30 V)	Note 1
-30 V Sense Relays in any expansion frame with -30 V Notes 1, 2 YZ056	01E-RY12 (+8.5 V up)	
01E-RY12-4 YZ055	0XF-HD1 (Turn On +6 V) and drops +3.4 V and +8.5 V	
0XF-HD1-(1 & 2) and 01H-HD1 (+12) YZ071	+6 and +12 volts (all frames)	
+6 and +12 volts drops YZ101	+6 and +12V Sense Relays (all frames)	
+6 V Sense Relay transistor turnoff YZ101	Ground for -30 V sequence Note 1	+1 V (approx) +20 V (approx)
+6 V Sense Relays in all frames YZ056	01E-RY2 (+6 V Up)	
01E-RY2-4 YZ055	01E-HD1 (Contactors On)	
2 01E-HD1-1 YZ052	PPB-K2 (ac to 3705)	
01E-HD1-1 YZ052	PPB-K1 (ac to Expansion Frames 1, 2, and 3)	
PPB-K2 (3705), PPB-K1 Expansion Frames (Domestic) YZ003-005	-12 V, -4 V (all frames)	
-12 V, -4 V drops YZ101	-12 V, -4 V Sense Relays (all frames)	
-12 V, -4 V Sense Relay transistor turnoff YZ101	Ground for +6 V sequence	+1 V (approx) +20 V (approx)
-12 V, -4 V Sense Relays in all frames YZ056	01E-RY1 (+12 V, -12V, -4 V Up)	
01E-RY1-3 YZ053	01E-RY3 (Sequence Complete)	
RY3-1 N/C YZ054	Power-On Reset Controlled	Ground +24 Vdc
	PPB-K1 (EPO)	
	01E-RY9 (Remote)	Remote position of Local/Remote Power Switch
		Local position of Local/Remote Power Switch

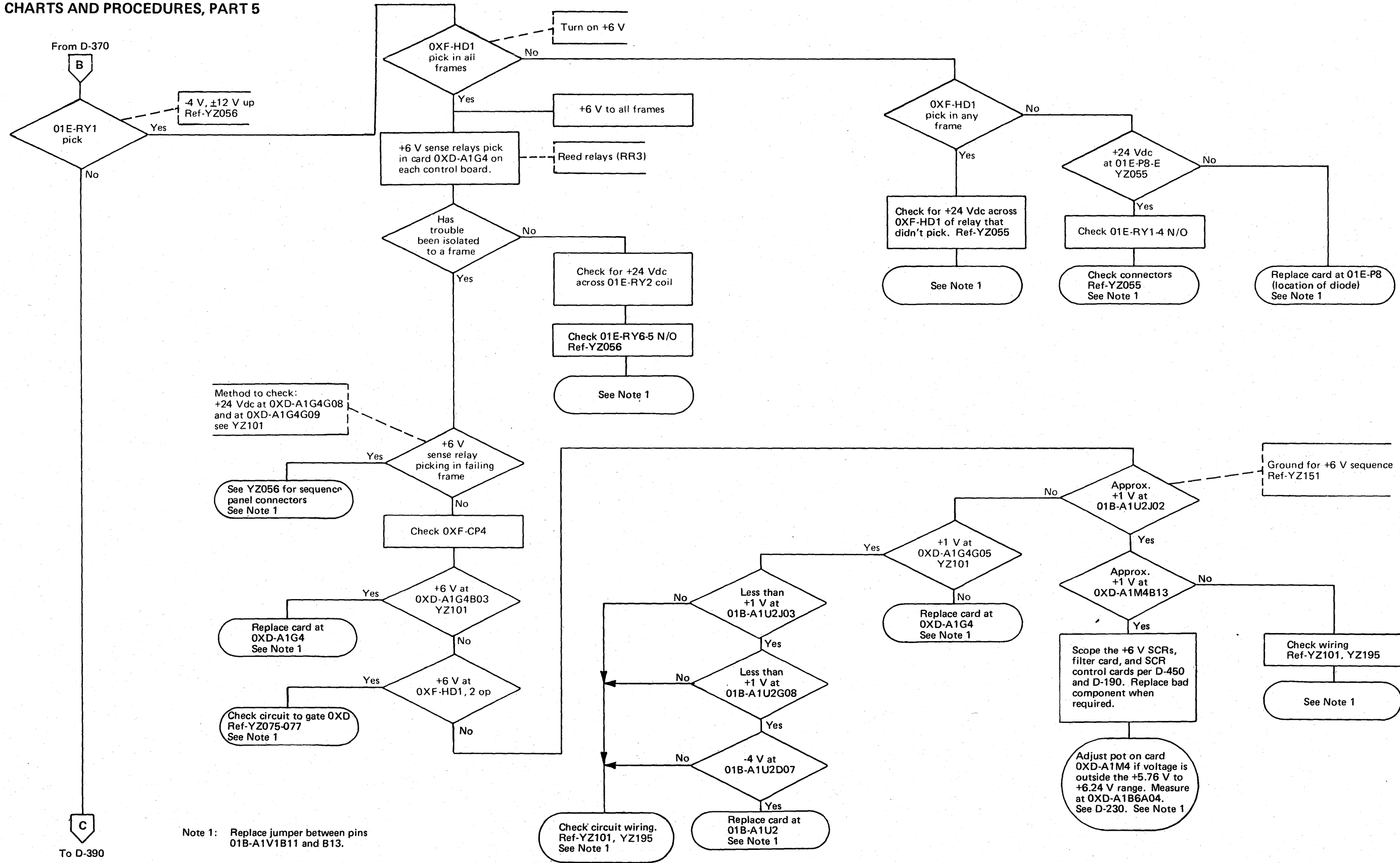


Notes:
 1. Replace jumper between pins 01B-A1V1B11 and B13.
 3. Remove jumpers at 01B-A1U2G04 and 01B-A1U2D13.
 4. Reinstall the removed FET array cards in their original locations.
 5. This voltage will only appear momentarily and is best observed with an oscilloscope.

3705-II MAINTENANCE CHARTS AND PROCEDURES, PART 4



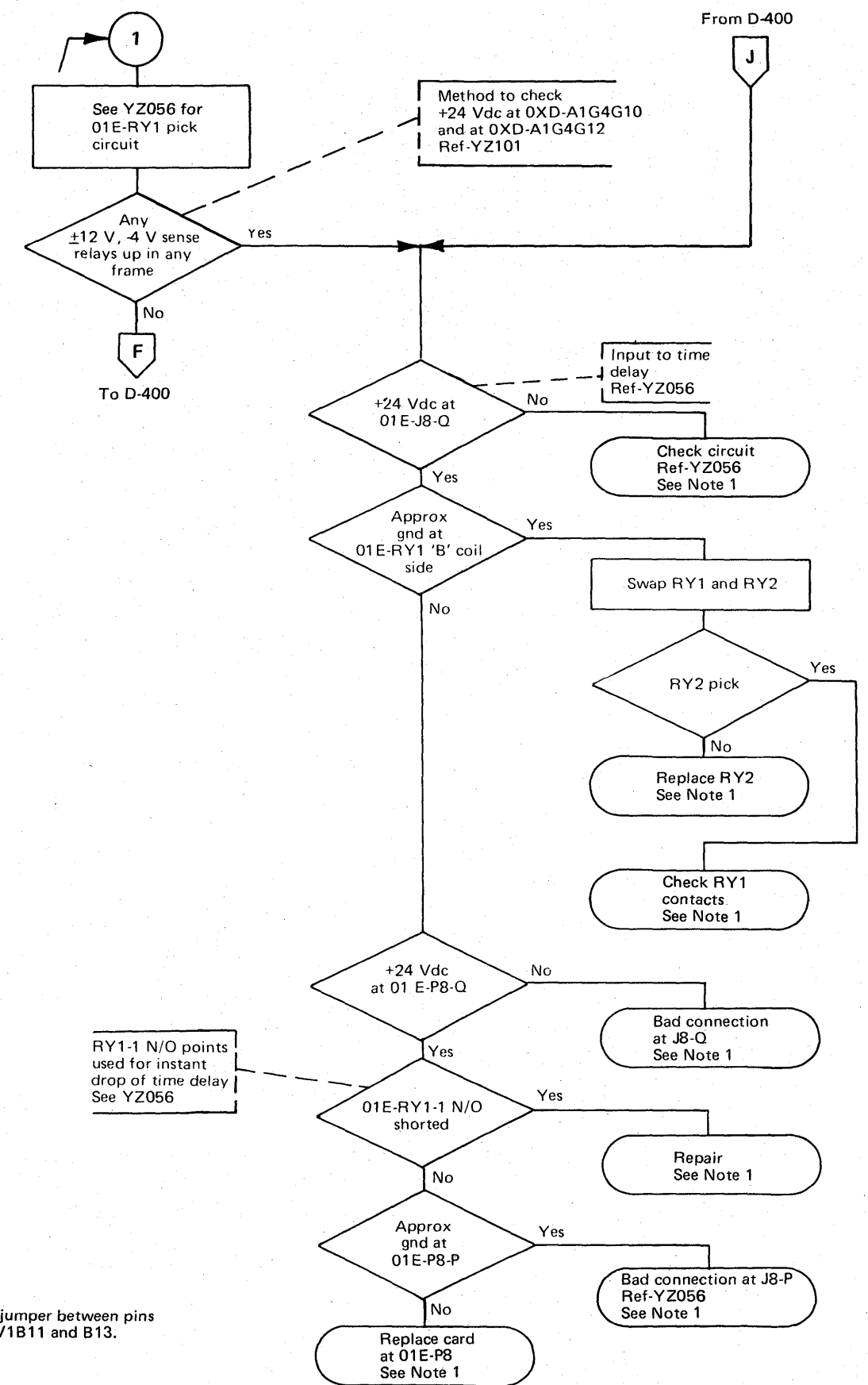
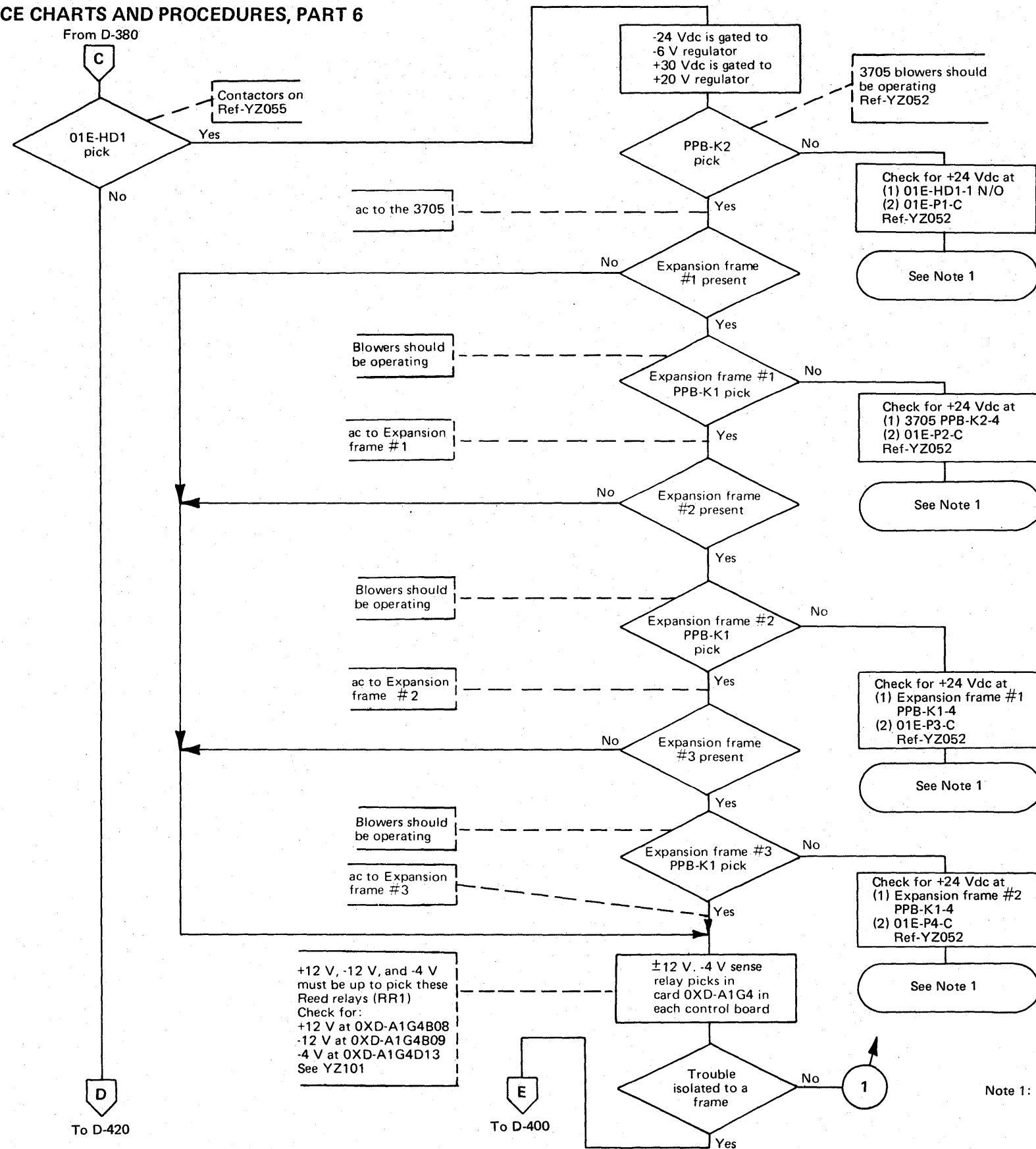
- Notes:
1. Replace jumper between pins 01B-A1V1B11 and B13.
 2. Remove jumpers at 01B-A1U2D09 and 01B-A1U2J12.
 4. Reinstall the removed FET array cards in their original locations.



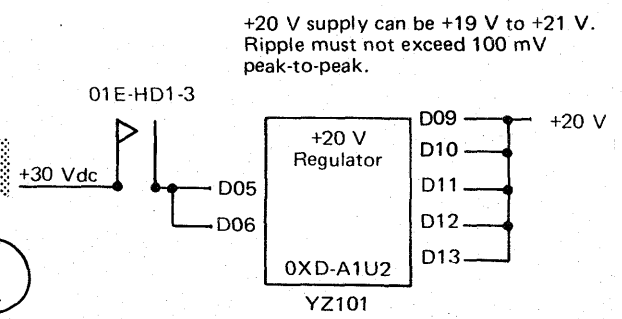
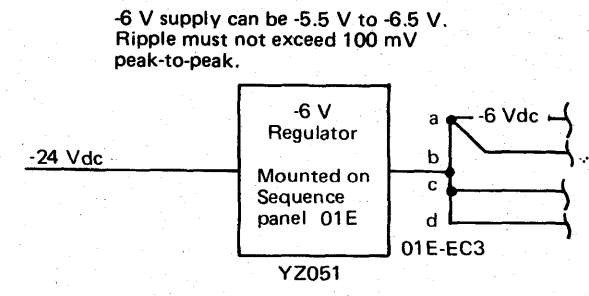
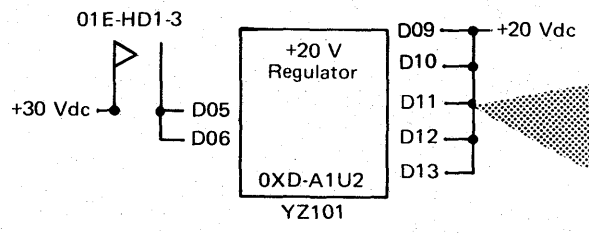
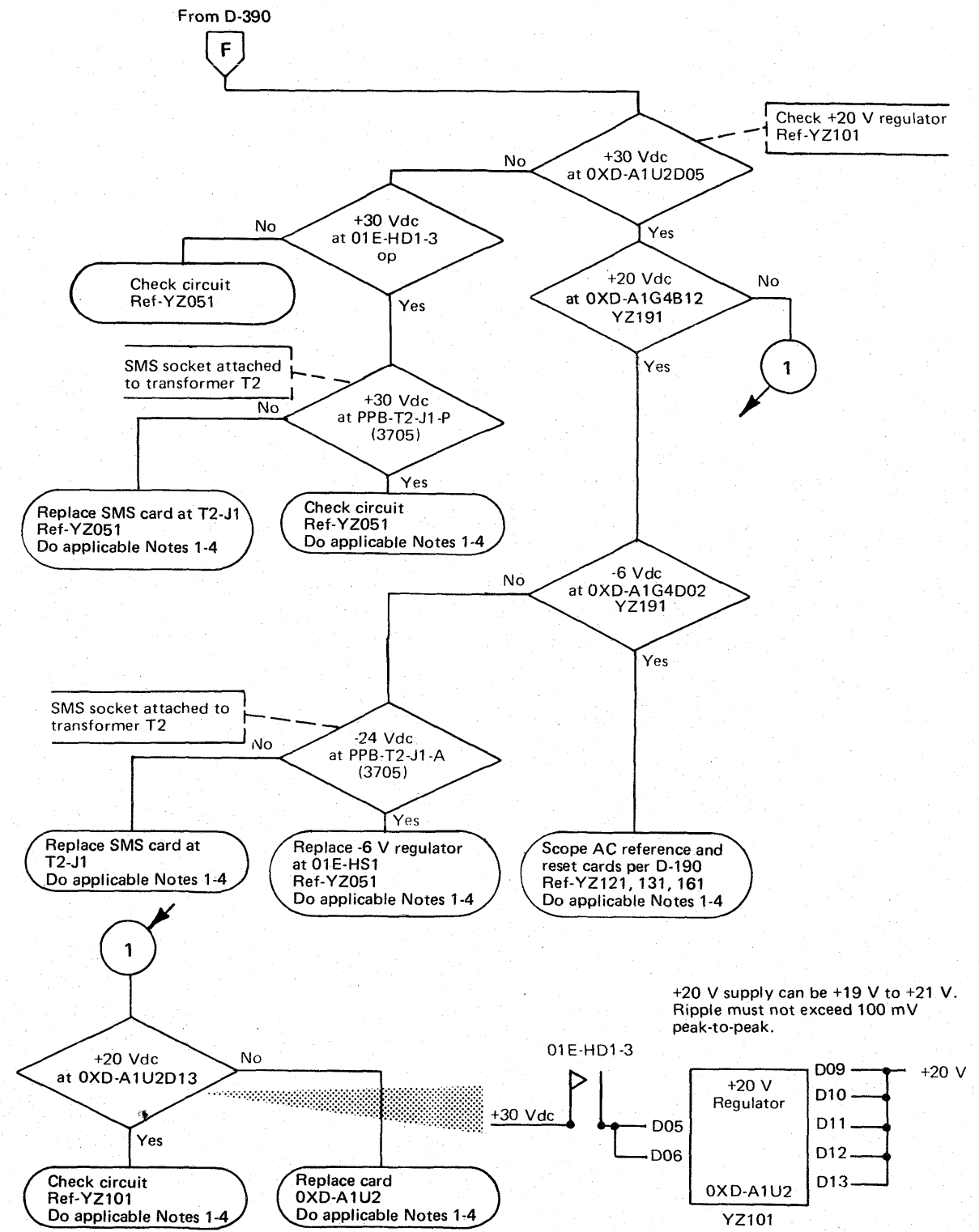
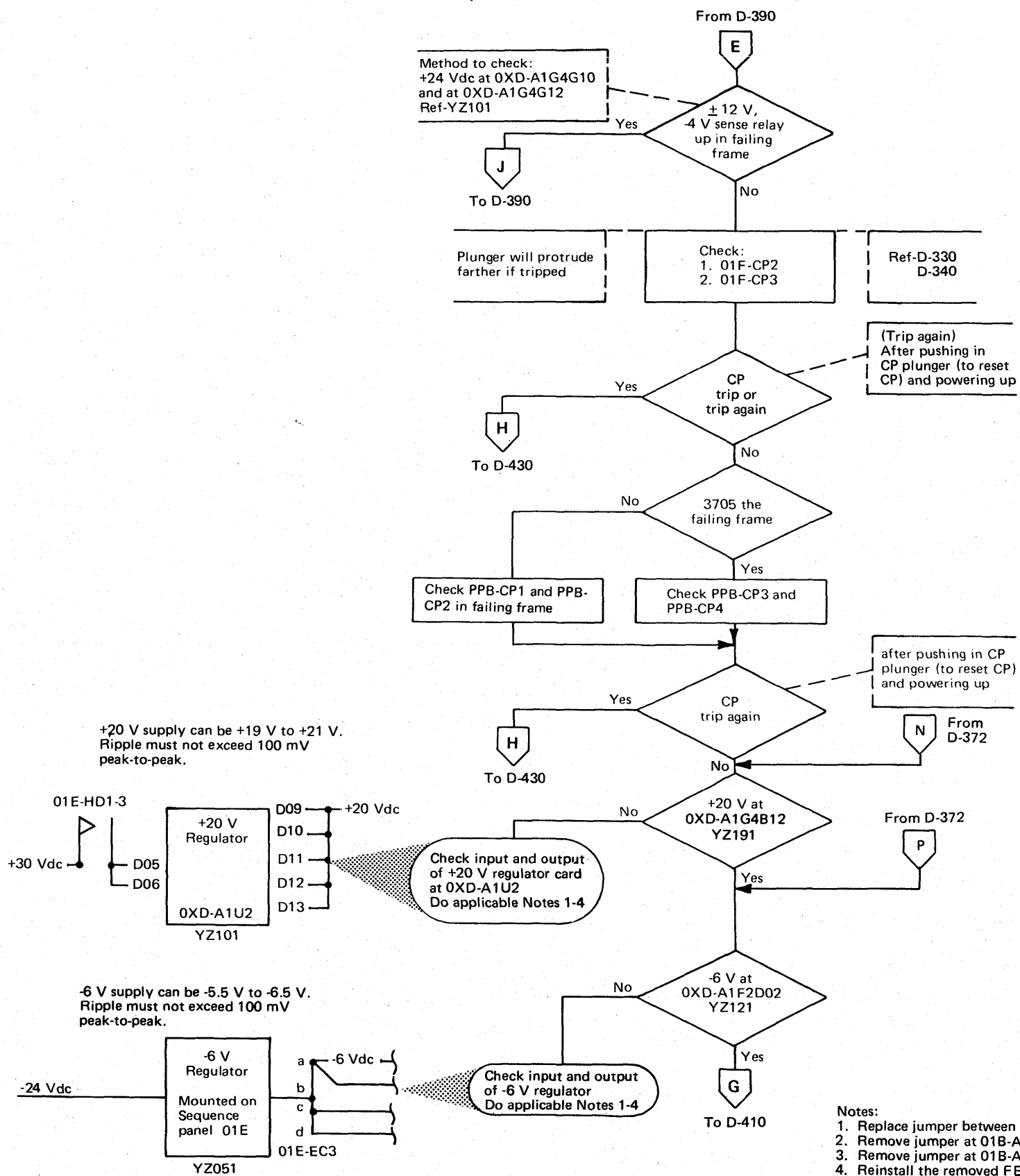
Note 1: Replace jumper between pins 01B-A1V1B11 and B13.

To D-390

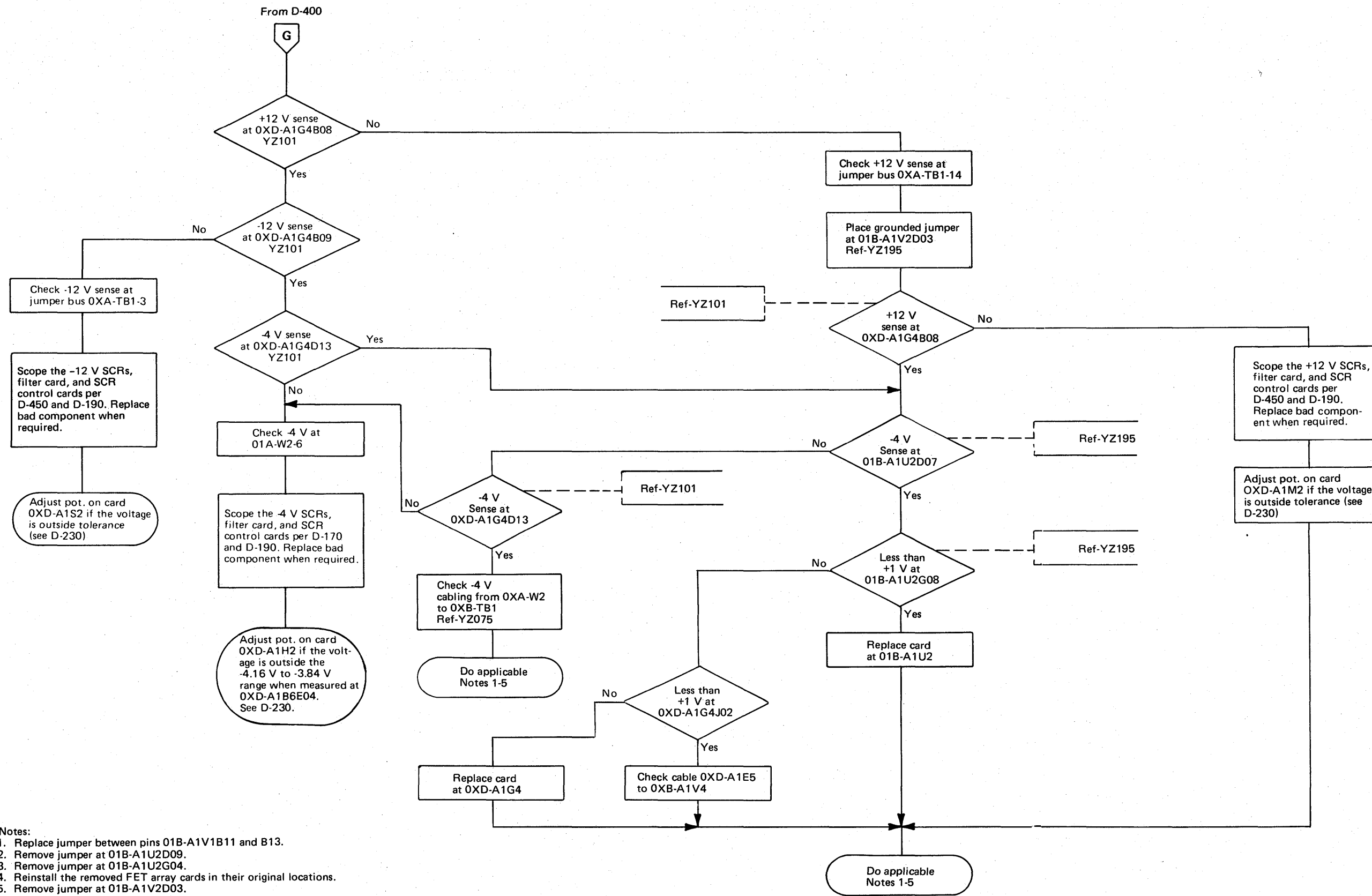
3705-II MAINTENANCE CHARTS AND PROCEDURES, PART 6



Note 1: Replace jumper between pins 01B-A1V1B11 and B13.

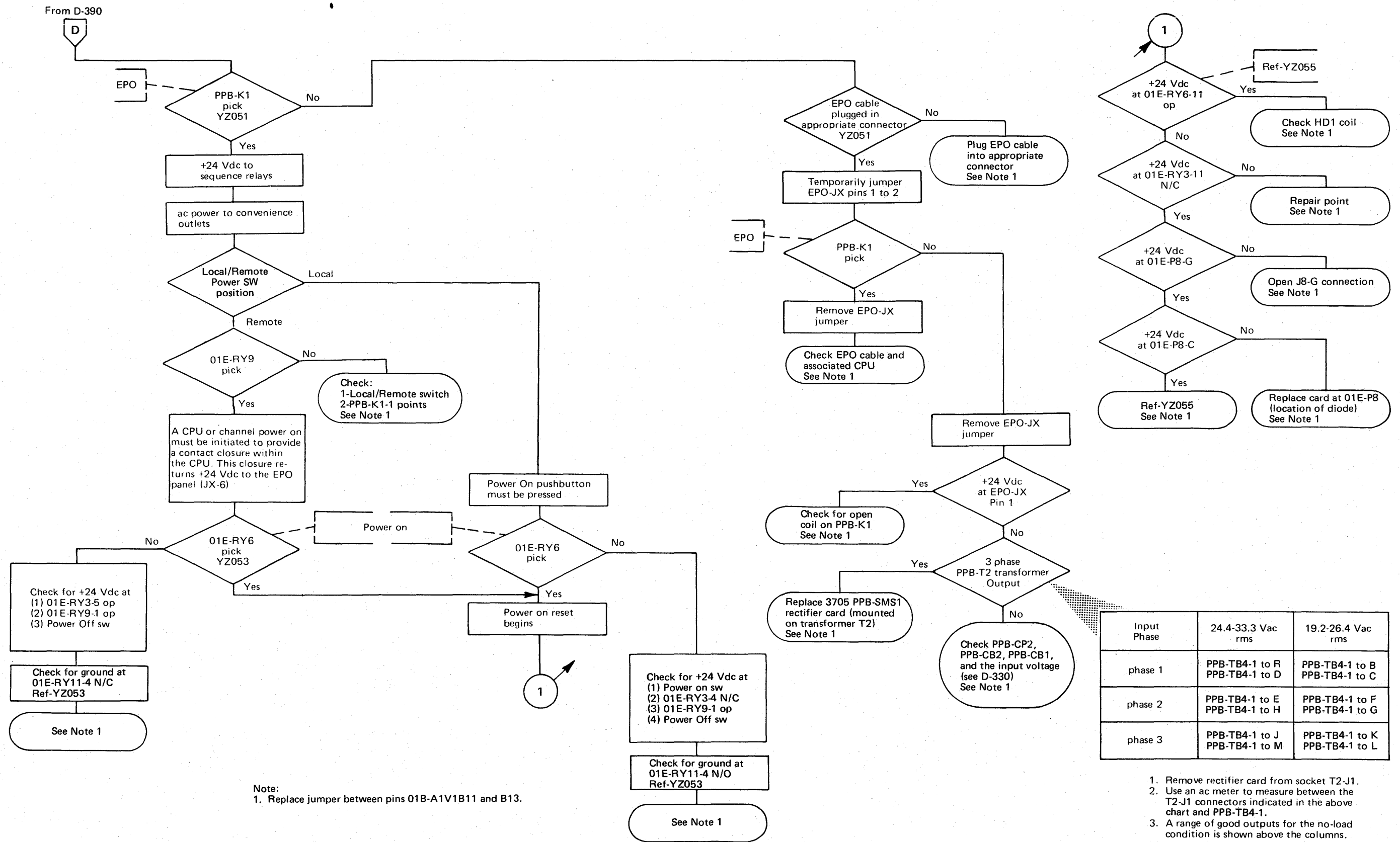


3705-II MAINTENANCE CHARTS AND PROCEDURES, PART 8



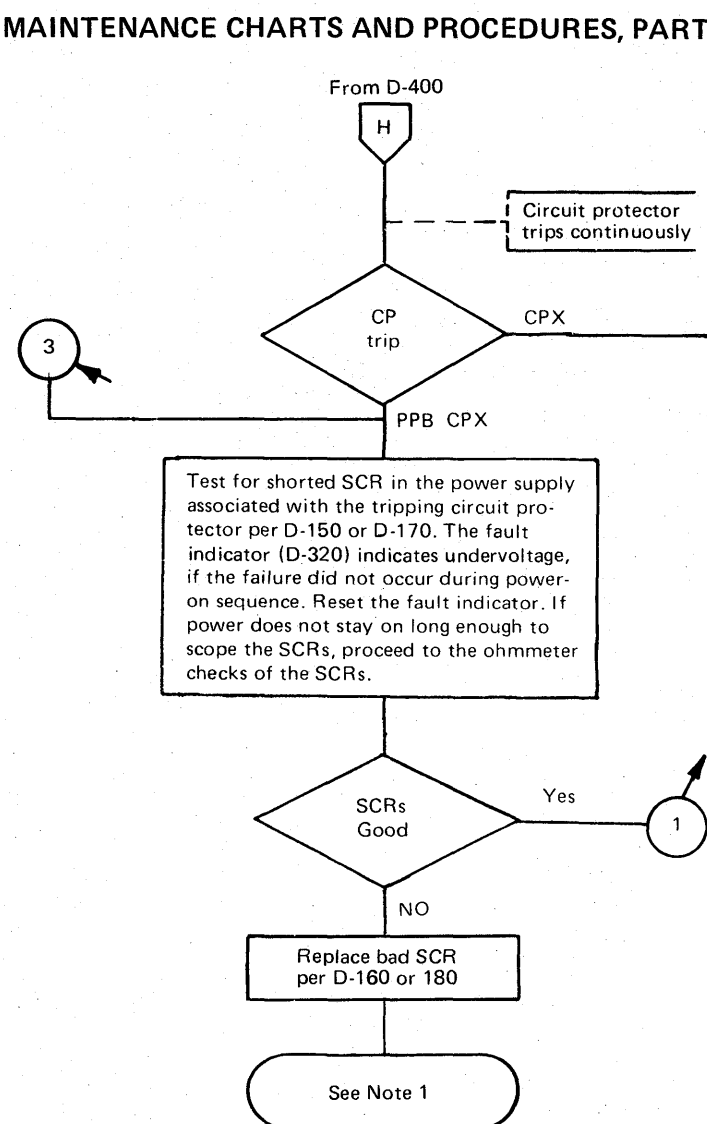
- Notes:
1. Replace jumper between pins 01B-A1V1B11 and B13.
 2. Remove jumper at 01B-A1U2D09.
 3. Remove jumper at 01B-A1U2G04.
 4. Reinstall the removed FET array cards in their original locations.
 5. Remove jumper at 01B-A1V2D03.

3705-II MAINTENANCE CHARTS AND PROCEDURES, PART 9



1. Remove rectifier card from socket T2-J1.
2. Use an ac meter to measure between the T2-J1 connectors indicated in the above chart and PPB-TB4-1.
3. A range of good outputs for the no-load condition is shown above the columns.

3705-II MAINTENANCE CHARTS AND PROCEDURES, PART 10

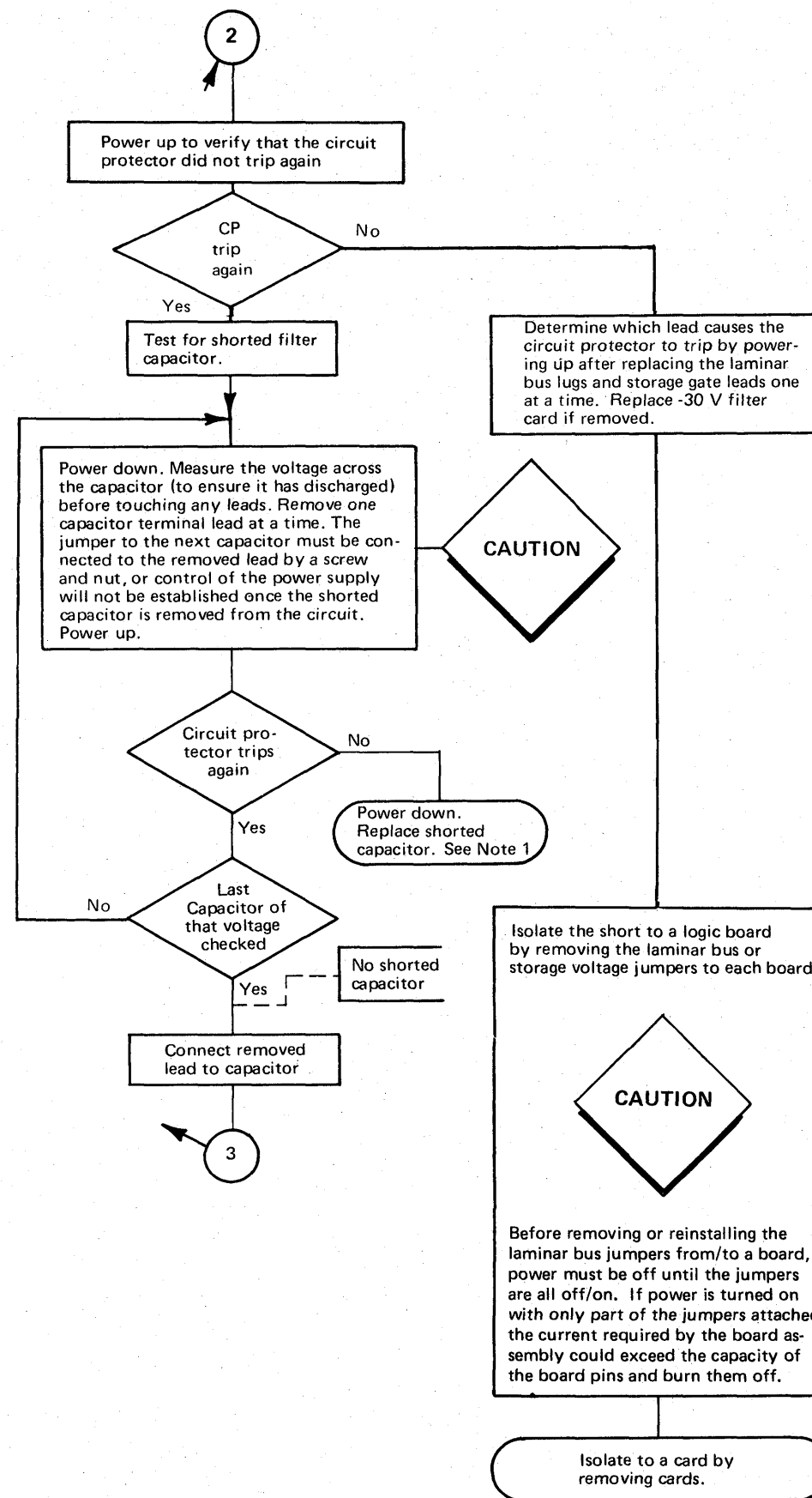


This section applies to 3705-II expansion frames that will contain BSMs.

Follow the instructions below for the voltage associated with the circuit protector that trips.

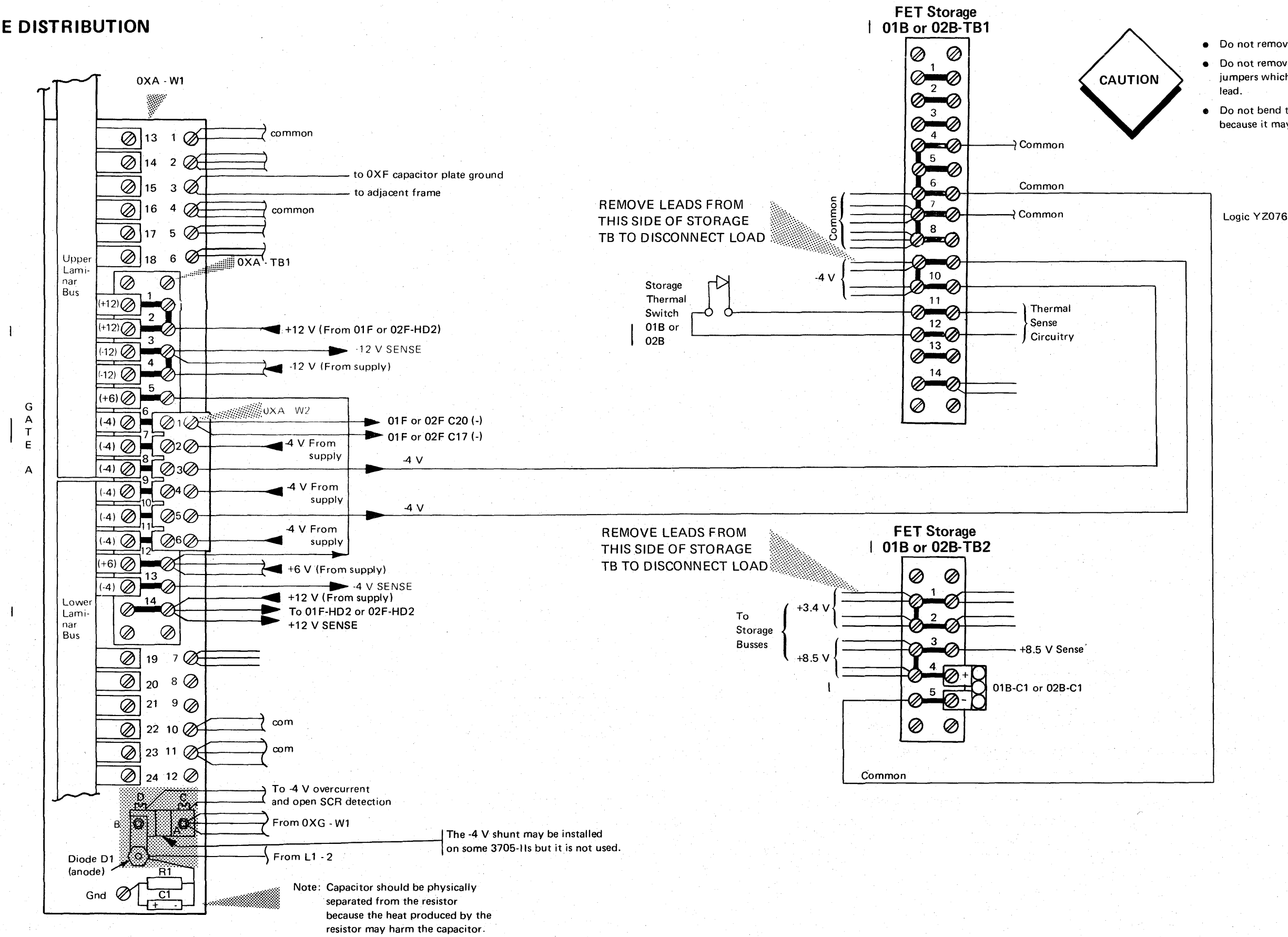
Power Supply	Disconnect	Add
-4 V	<ul style="list-style-type: none"> Laminar bus lugs at OXA-TB1-6, 7, 8, 9, 10, 11, 13 Storage gate B leads at Mem 01B-TB1-9, 10 	Jumper between OXA-TB1-13 and OXA-W2-6. (This jumper re-establishes the -4 V sense connection needed to bring power up.)
+12 V	Laminar bus lugs at OXA-TB1-1 and 2	none
-12 V	Laminar bus lugs at OXA-TB1-3 and 4	none
+6 V	<ul style="list-style-type: none"> Laminar bus lugs at OXA-TB1-5 and 12 Storage gate B leads at Mem TB-5 Storage gate C leads at Mem TB-6 	none
	CAUTION Remove the -30 V filter card at OXD-A1R4 to prevent -30 V from coming up whenever the +6 V leads are removed from Mem TB-5, 6, or component damage may occur in the BSM	
-30 V	<ul style="list-style-type: none"> Storage gate B leads at Mem TB1 Storage gate C leads at Mem TB-2 	none

See D-440

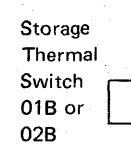


Note:
1. Replace jumper between pins 01B-A1V1B11 and B13.

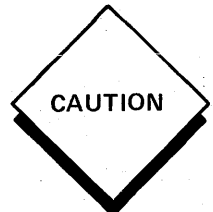
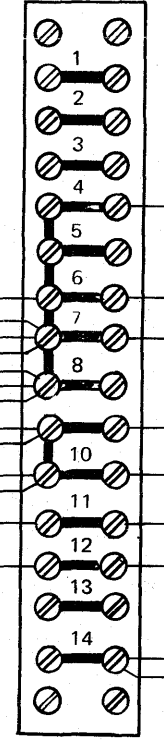
3705-II DC VOLTAGE DISTRIBUTION



REMOVE LEADS FROM THIS SIDE OF STORAGE TB TO DISCONNECT LOAD



FET Storage | 01B or 02B-TB1



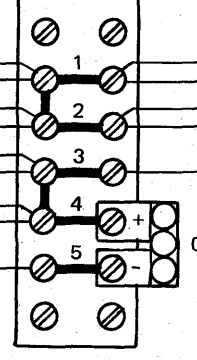
- Do not remove any of the wires labeled SENSE
- Do not remove any of the terminal board (TB) jumpers which connect a voltage with its sense lead.
- Do not bend the laminar bus tab too sharply because it may crack upon straightening.

Logic YZ076

REMOVE LEADS FROM THIS SIDE OF STORAGE TB TO DISCONNECT LOAD

To Storage Busses

FET Storage | 01B or 02B-TB2



3705-II POWER-DOWN SEQUENCE

• This page shows the sequence of events that occur during normal power-off operation, (1) when the Local/Remote Power switch is set to the LOCAL position, and the Power Off switch is pressed, or (2) when the Local/Remote Power switch is set to the REMOTE position, and the host CPU brings power down.

1 01E-RY13 (power-off override) drops 3 to 4 seconds after 01E-RY6 (power on) drops. If the power-down sequence has not been completed by the time the power-off override relay drops, the following events occur:

- 01E-RY13-1 N/O drops 01E-HD1 (contactors on) -see YZ055. The power down sequence continues from **2**

- 01E-RY13-1 N/C picks 01E-RY11 (fault sense) through the 01-RY-2 N/O (± 12 V, -4 V up) which turns on the Power Check light.

This circuit prevents a failure to complete a power-down sequence which might have occurred due to a condition such as a sticking relay.

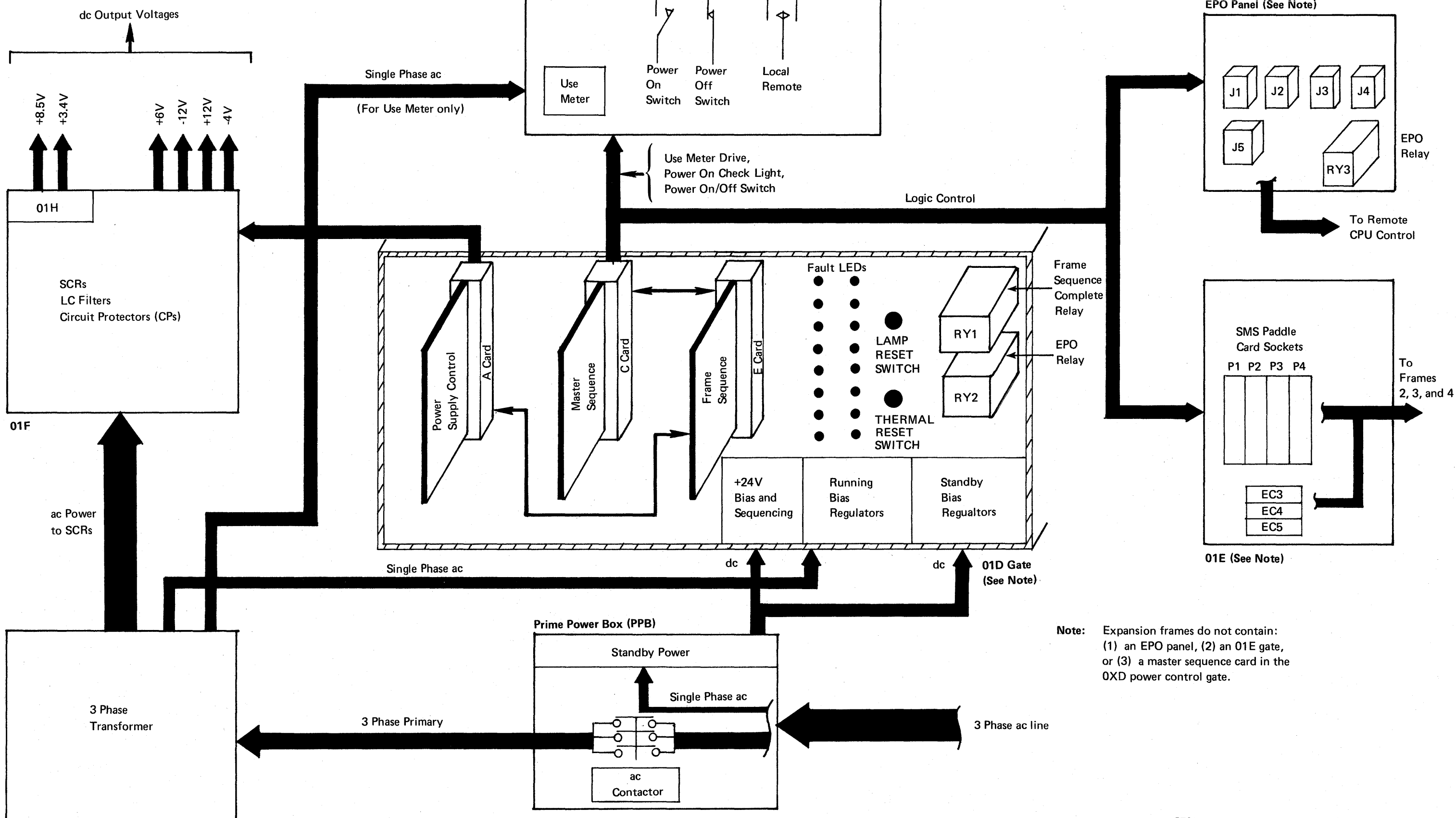
Notes:

1. Applies to expansion frames that have a -30 V power supply.
2. When the 3705-II has no expansion frames, 01E-RY6-6 drops 01E-RY12.

2

Contact or action causing dropout	Power Supply Components or Action	Timing Relationships
(Local) Press Power Off Switch YZ053	Power Off Switch or CPU Power Off Switch	
Power Off Switch	01E-RY6 (Power On)	
01E-RY6-12 N/C YZ054	Power Off Reset	Floating Ground
01E-RY6-9 YZ053	Power On Light	
01E-RY6-10 (Local) YZ055	01F-HD2 (Apply +12 V to logic)-basic frame 0XF-HD2 (Turn On -30 V)-Note 1	Ground put on -30 V at Mem TB1-1 Note 1
01E-RY6-2 YZ055	01E-RY13 (Power Off Override)	3-4 Seconds 1
0XF-HD2-(1,3) Note 1 YZ071	-30 V (all expansion frames with -30 V)	Note 1
-30 V drops Note 1 YZ101	-30 V Sense Relays (all expansion frames with -30 V)	Note 1
-30 V Sense Relays in any expansion frame with -30 V Notes 1, 2 YZ056	01E-RY12 (+8.5 V up)	
01E-RY12-4 YZ055	OXF-HD1 (Turn On +6 V) and drops +3.4 V and +8.5 V	
OXF-HD1-(1 & 2) and 01H-HD1 (+12) YZ071	+6 and +12 volts (all frames)	
+6 and +12 volts drops YZ101	+6 and +12V Sense Relays (all frames)	
+6 V Sense Relay transistor turnoff YZ101	Ground for -30 V sequence Note 1	+1 V (approx) +20 V (approx)
+6 V Sense Relays in all frames YZ056	01E-RY2 (+6 V Up)	
01E-RY2-4 YZ055	01E-HD1 (Contactors On)	
01E-HD1-1 YZ052	PPB-K2 (ac to 3705)	
01E-HD1-1 YZ052	PPB-K1 (ac to Expansion Frames 1, 2, and 3)	
PPB-K2 (3705), PPB-K1 Expansion Frames (Domestic) YZ003-005	-12 V, -4 V (all frames)	
-12 V, -4 V drops YZ101	-12 V, -4 V Sense Relays (all frames)	
-12 V, -4 V Sense Relay transistor turnoff YZ101	Ground for +6 V sequence	+1 V (approx) +20 V (approx)
-12 V, -4 V Sense Relays in all frames YZ056	01E-RY1 (+12 V, -12V, -4 V Up)	
01E-RY1-3 YZ053	01E-RY3 (Sequence Complete)	
RY3-1 N/C YZ054	Power-On Reset Controlled	Ground +24 Vdc
	PPB-K1 (EPO)	
	01E-RY9 (Remote)	Remote position of Local/Remote Power Switch
		Local position of Local/Remote Power Switch

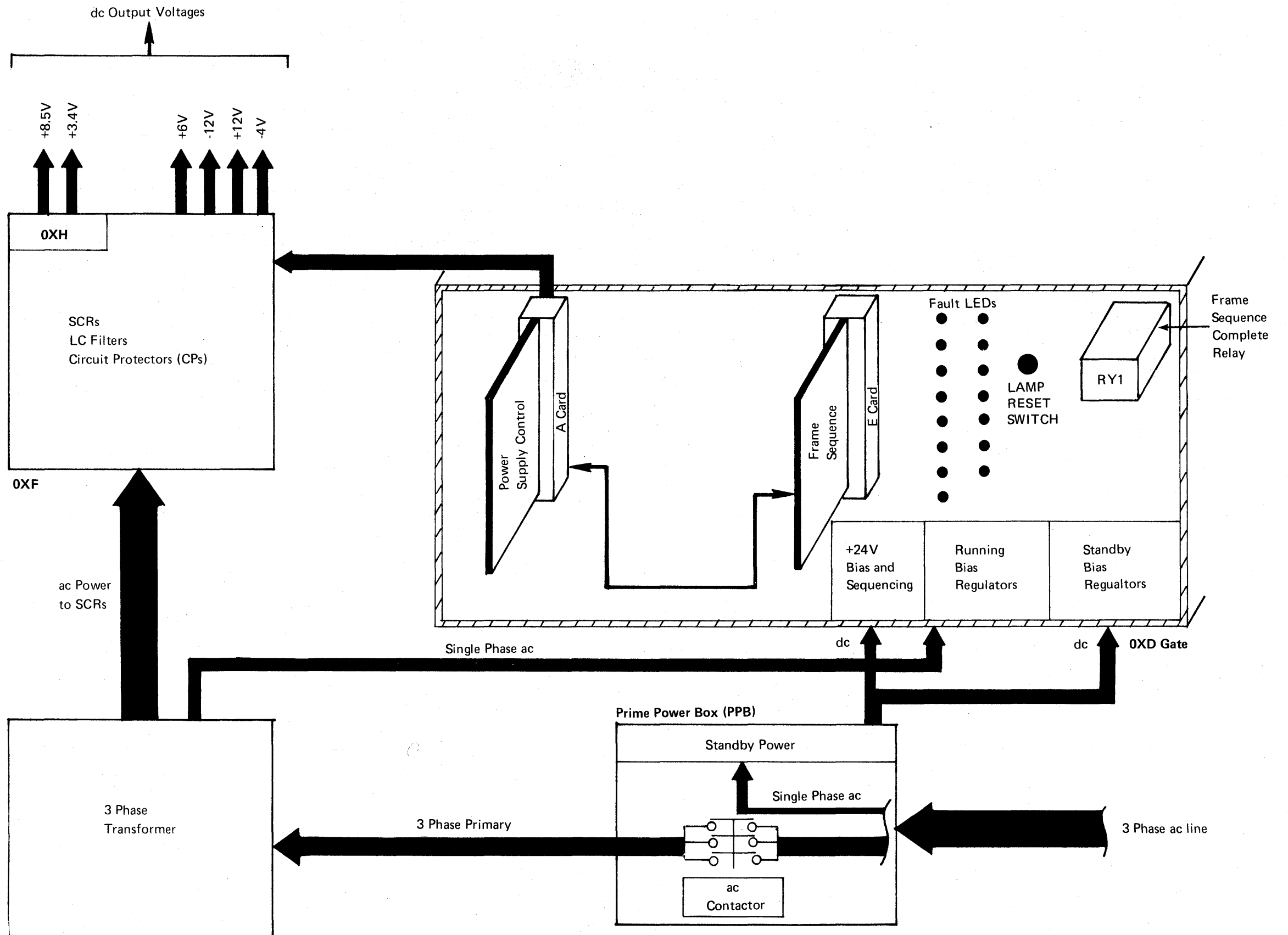
**3705-II MODIFIED POWER—BASIC FRAME
(01D GATE WITH ONLY THREE CARDS)**



Note: Expansion frames do not contain:
(1) an EPO panel, (2) an 01E gate,
or (3) a master sequence card in the
OXD power control gate.

3705-II MODIFIED POWER-EXPANSION FRAME (OXD GATE WITH ONLY TWO CARDS)

Note: Expansion frames do not contain (1) a control panel, (2) a master sequence control card in the OXD gate, (3) an O1E gate, or (4) an EPO panel.



3705-II POWER SUPPLY (OXD GATE WITH ONLY TWO OR THREE CARDS)

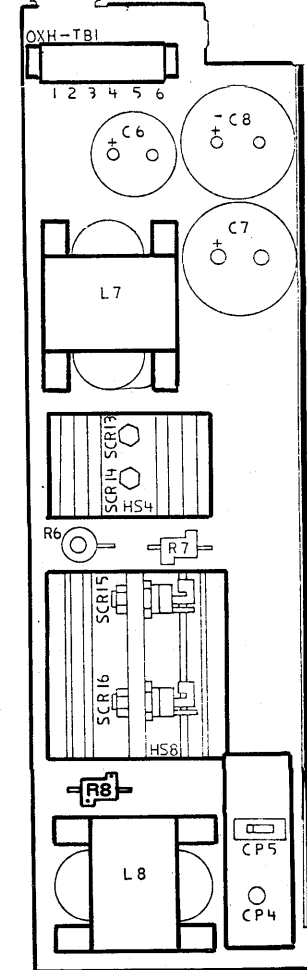
Note: For a 3705-II with more than three cards in the OXD gate, see D-300.

Component Locations

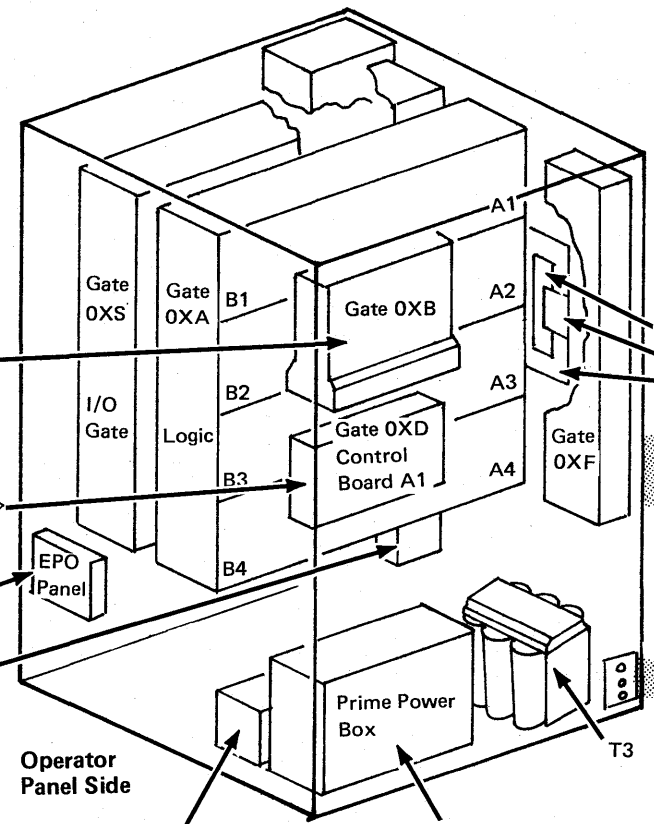
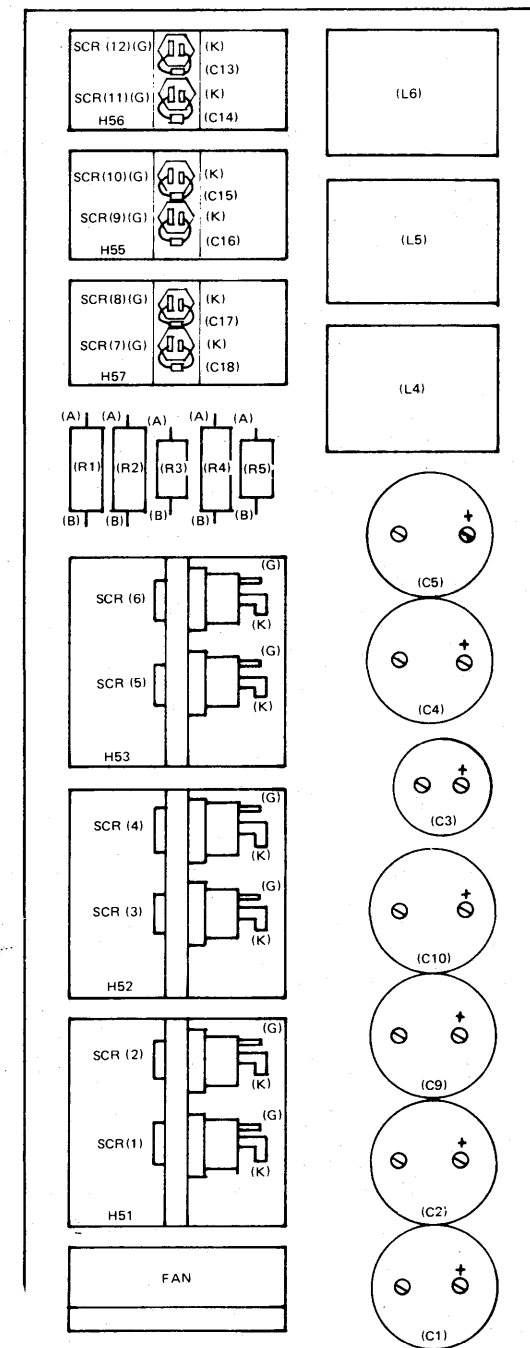
Note: The 3705-II expansion frame with modified power does not contain (1) a control panel, (2) a master sequence card in the OXD gate, (3) an O1E gate, or (4) an EPO panel. An RPO power supply assembly (S30251) must be installed in the EPO panel location if an expansion frame without modified power is to attach to a 3705-II basic frame with modified power. Otherwise the physical locations of components in the basic frame and expansion frames are the same.

Unit	Layout Reference
Prime power box	YZ586 sheets 2, 3, or 13
OXD	YZ586 sheet 11
O1E	YZ586 sheet 9
EPO panel	YZ586 sheet 10
FET storage (OXB)	YZ586 sheet 15
I/O Gate (OXS)	YZ586 sheet 8
OXF	YZ586 sheet 6
OXH	YZ586 sheet 16

Gate OXH (Present on basic frame and first expansion frame only)



Gate OXF
Power Supply Mounting Asm.
-4V, +6V and ±12V



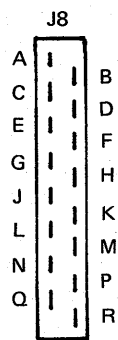
FET Storage
(Base frame and first expansion frame only)

OXD-A1
Power Supply Control Card

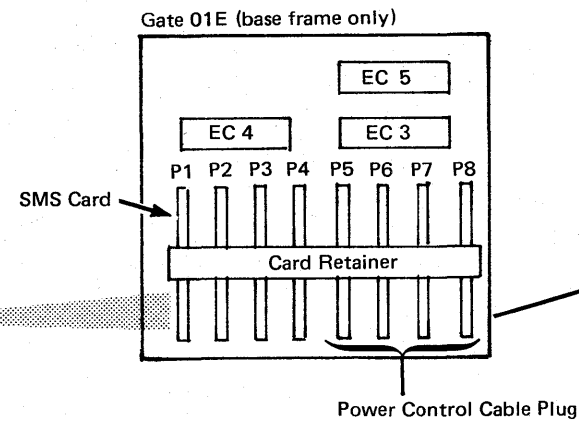
O1D-C1 (Base frame only)
Master Sequence Card

OXD-E1
Frame Sequence Card
*(Base frame only)

8-Position SMS Card
Connector (P1-P8, card side)

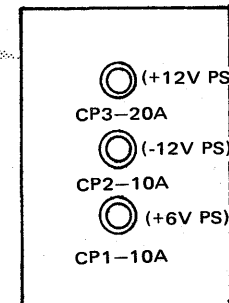


Wiring Side



P1 - 3705
P2 - 1st expansion frame
P3 - 2nd expansion frame
P4 - 3rd expansion frame

*RPO S30251 power supply assembly is mounted in EPO panel location on expansion frames (without modified power) that attach to a 3705-II basic frame with modified power.



**3705-II POWER CHECK
(OXD GATE WITH ONLY TWO OR THREE CARDS)**

Note: See D-600 for 3705-II Maintenance Analysis Procedures.

- The Power Check light turns on during a normal power-on sequence and turns off when the sequence has successfully completed.
- A power-off sequence occurs, and the Power Check light turns on for any of the following check conditions:
 1. Overvoltage on any logic voltage
 2. Undervoltage on any logic voltage
 3. Thermal sense on the logic gates, storage gates, and power supplies.
- If the power check resulted from conditions 1-2, reset the Power Check light by pressing the Power Off switch. Power can now be turned on.
- If the power check resulted from a thermal condition, reset the power check light by pressing the THERMAL RESET switch (located on the power sequence control gate-OXD after the thermal contact that detected the thermal condition has cooled off and closed its contact (usually about a half hour). Power can now be turned on.

**3705-II FAULT INDICATORS
(OXD GATE WITH ONLY TWO OR THREE CARDS)**

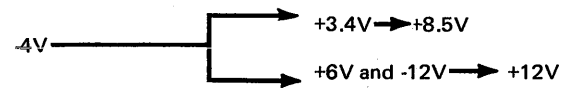
There are 16 light-emitting diodes (LEDs) located on the panel of gate OXD. When on, these LEDs indicate the following fault conditions;

- Overvoltage on any logic voltage
- Undervoltage on any logic voltage
- 3.4 or 8.5V TIME FAULT
- 'THERMAL' Sense

Once a LED is on, it stays on even if power drops. To turn the LED(s) off, press the LAMP RESET button located on the panel of gate OXD.

- All fault indications cause power down and turn on the 'power check' light.

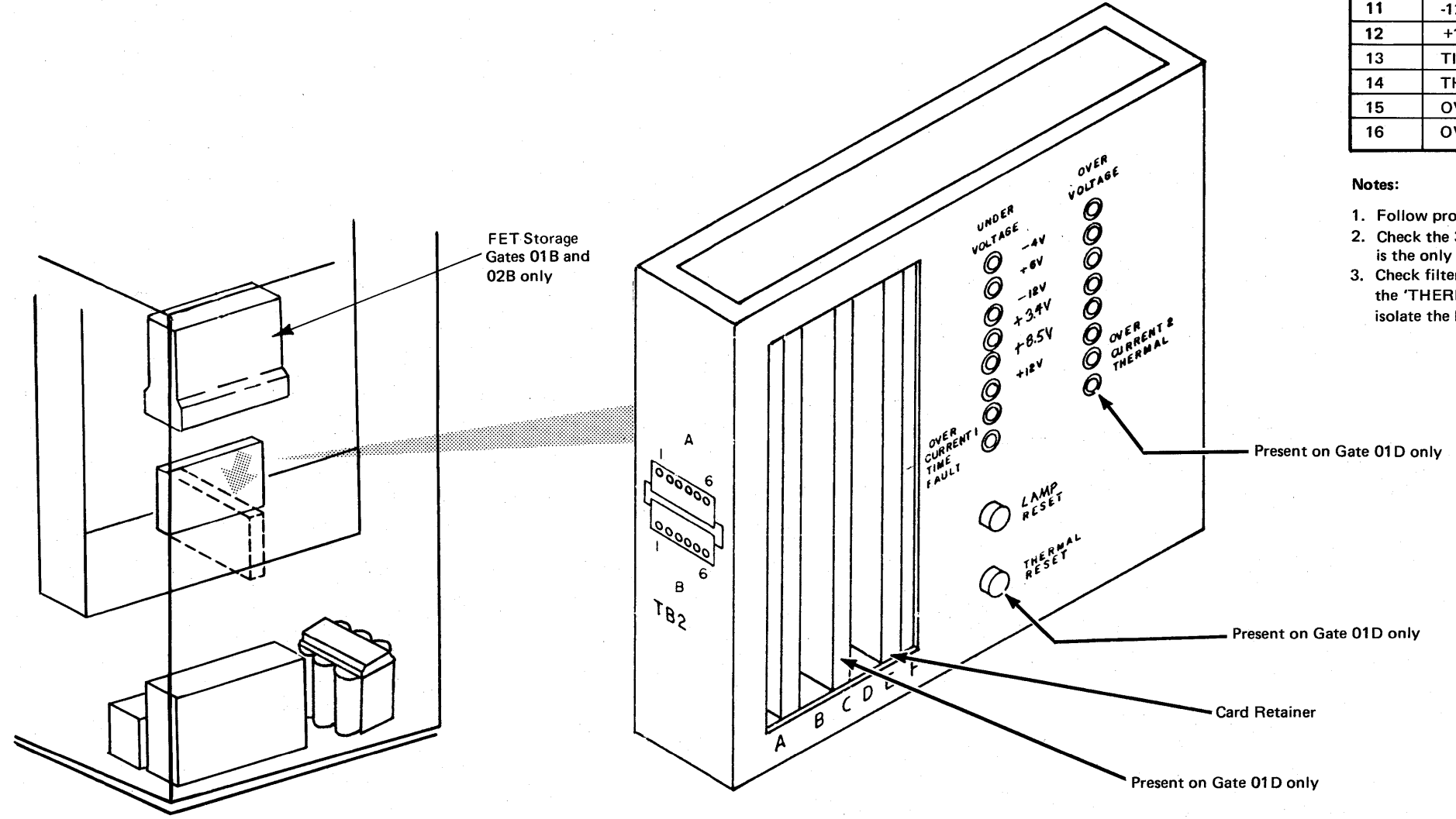
Power On Voltage Sequence:



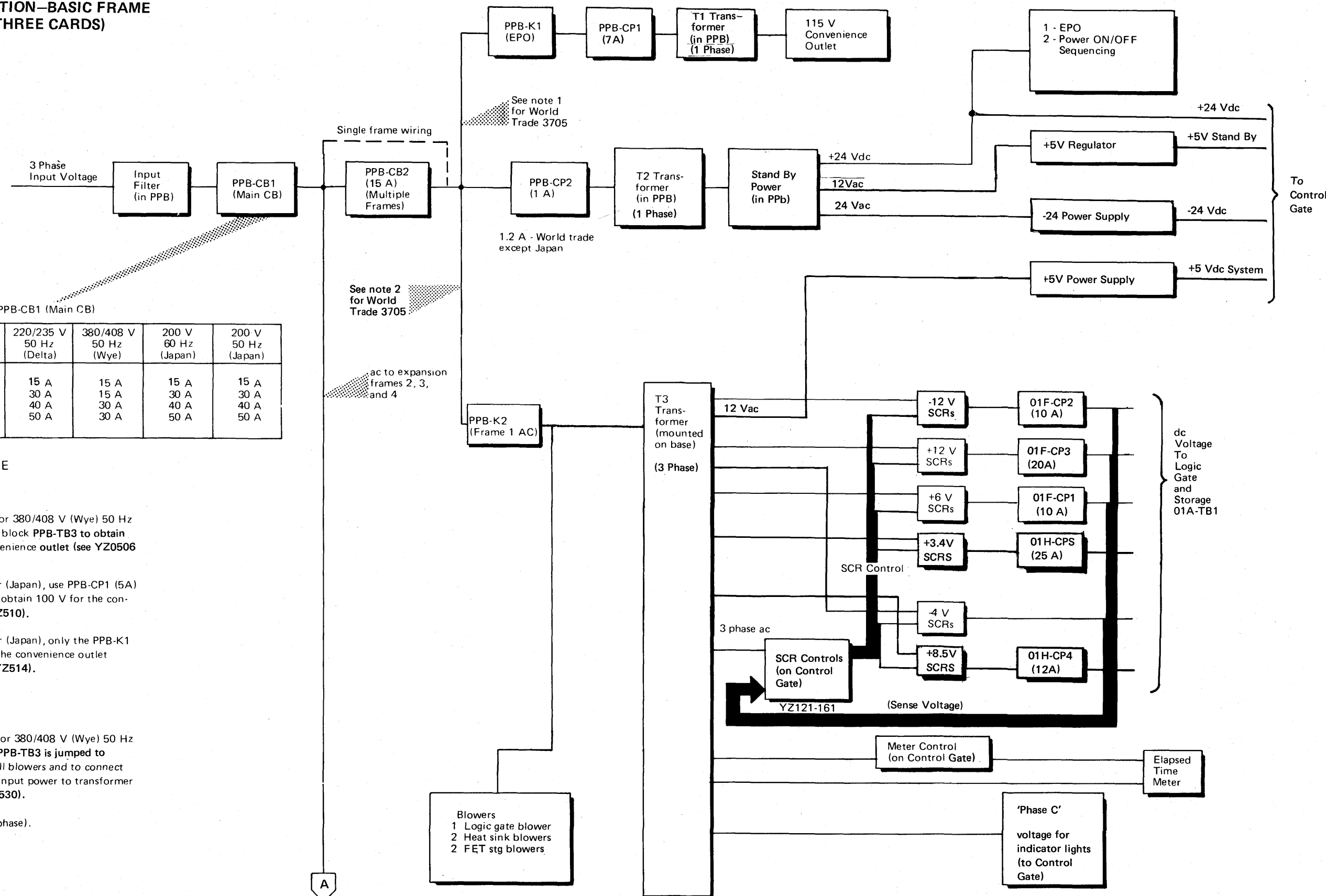
LED#	Fault Indication	Causes Power Down	Duration of Fault Before Power Down	Level at which sense relays pick, LED turns on, under-voltage causes power down	Action To Be Taken If Respective LED is On
1	-4V OVERVOLTAGE	Yes	Immediate	-4.7V	See Note 1 and refer to: D-670 D-670 D-670 D-670 D-670 D-670 D-640 D-645 D-650 D-655 D-660 D-665 See Note 2 See Note 3 N/A N/A
2	+3.4V OVERVOLTAGE	Yes	Immediate	+4V	
3	+8.5V OVERVOLTAGE	Yes	Immediate	+9.7V	
4	+6V OVERVOLTAGE	Yes	Immediate	+6.6V	
5	-12V OVERVOLTAGE	Yes	Immediate	-14V	
6	+12V OVERVOLTAGE	Yes	Immediate	+14V	
7	-4V UNDERVOLTAGE	Yes	Immediate	3.0V to 3.5V	
8	+3.4V UNDERVOLTAGE	Yes	Immediate	2.8V	
9	+8.5V UNDERVOLTAGE	Yes	Immediate	+2.8V	
10	+6V UNDERVOLTAGE	Yes	Immediate	+5.4V to +5.59V	
11	-12V UNDERVOLTAGE	Yes	Immediate	-8.7V to -10.3V	
12	+12V UNDERVOLTAGE	Yes	Immediate	+9.0V to +10.0V	
13	TIME FAULT	Yes	1 Second	+VTL Logic Level	
14	THERMAL	Yes	Immediate	+VTL Logic Level	
15	OVERCURRENT 1	Not Used	N/A	N/A	
16	OVERCURRENT 2	Not Used	N/A	N/A	

Notes:

1. Follow procedure for checking SCRs as shown on D-560.
2. Check the 3.4V and 8.5V power supply if a 'TIME FAULT' is the only fault indication.
3. Check filters and blowers. Power on the 3705 and observe the 'THERMAL CHECK' light. If the light turns on again, isolate the light to frame and check thermistors and wiring.



3705-II POWER DISTRIBUTION—BASIC FRAME
(01D GATE WITH ONLY THREE CARDS)



PPB-CB1 (Main CB)

Frames Attached	208/230 V 60 Hz	220/235 V 50 Hz (Delta)	380/408 V 50 Hz (Wye)	200 V 60 Hz (Japan)	200 V 50 Hz (Japan)
3705	15 A	15 A	15 A	15 A	15 A
1st expansion frame	30 A	30 A	15 A	30 A	30 A
2nd expansion frame	40 A	40 A	30 A	40 A	40 A
3rd expansion frame	50 A	50 A	30 A	50 A	50 A

NOTES FOR WORLD TRADE

Note 1

For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, jumper terminal block PPB-TB3 to obtain 220/235 V for the convenience outlet (see YZ0506 and YZ508).

For 200 V 60 Hz power (Japan), use PPB-CP1 (5A) with transformer T1 to obtain 100 V for the convenience outlet (see YZ510).

For 200 V 50 Hz power (Japan), only the PPB-K1 contactor is used with the convenience outlet voltage of 200 V (see YZ514).

Note 2

For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, terminal block PPB-TB3 is jumped to obtain 220/235 V for all blowers and to connect the neutral of the Wye input power to transformer T3 (see YZ508 and YZ530).

(All blowers are single phase).

LEGEND

- PPB — Prime power box
- CP — Circuit protector
- CB — Circuit breaker
- SCR — Silicon controlled rectifier

To D-535

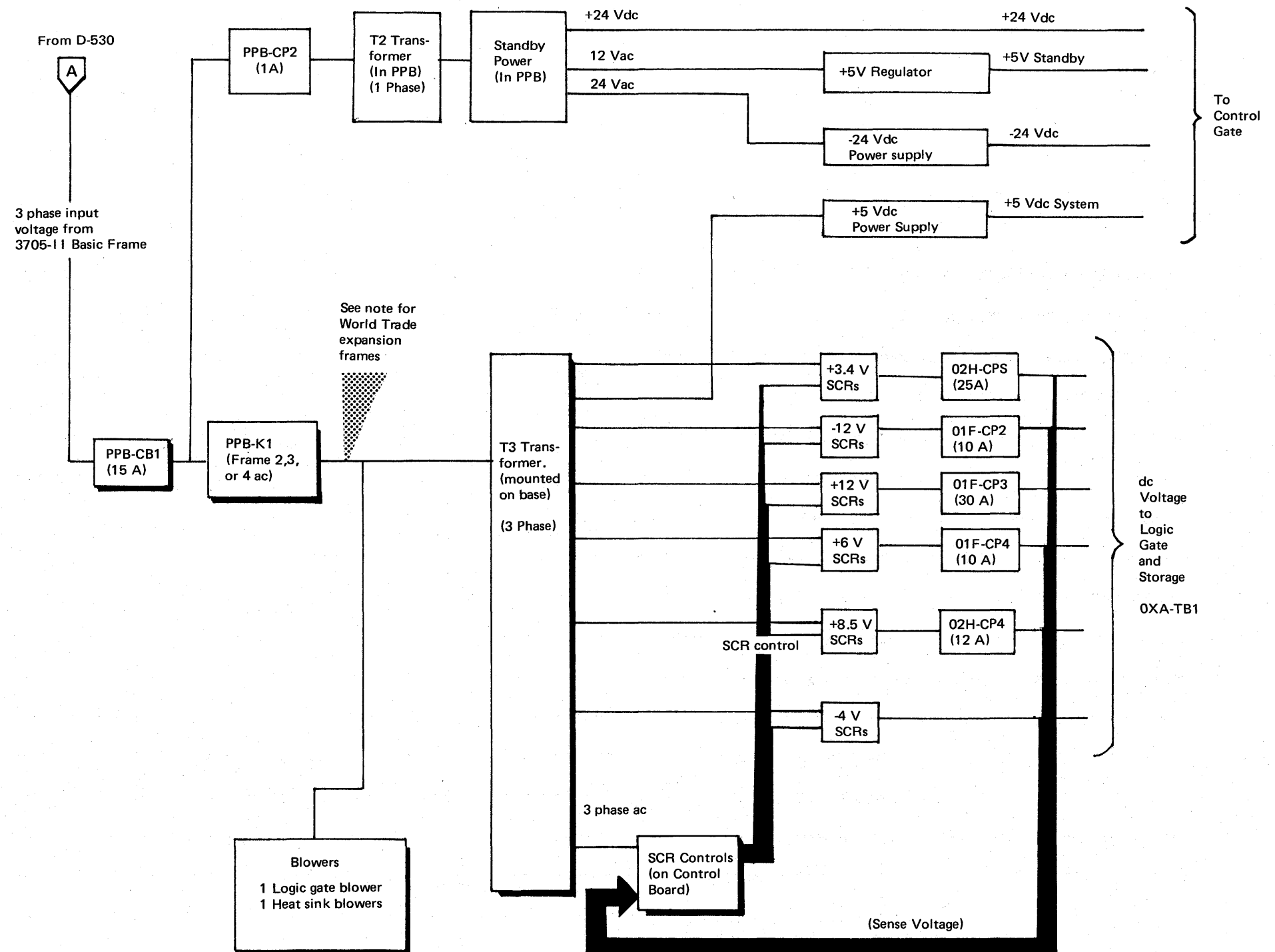
- Blowers
- 1 Logic gate blower
 - 2 Heat sink blowers
 - 2 FET stg blowers

'Phase C'
voltage for
indicator lights
(to Control
Gate)

**3705-II EXPANSION FRAME POWER DISTRIBUTION
(0XD GATE WITH ONLY TWO CARDS)**

NOTE FOR WORLD TRADE

- 220/235 V (Delta) or 380/408 V (Wye) 3 phase 50 Hz expansion frames are jumpered to obtain 220/235 V for all blowers and to connect the neutral of the Wye input power to transformer T3.

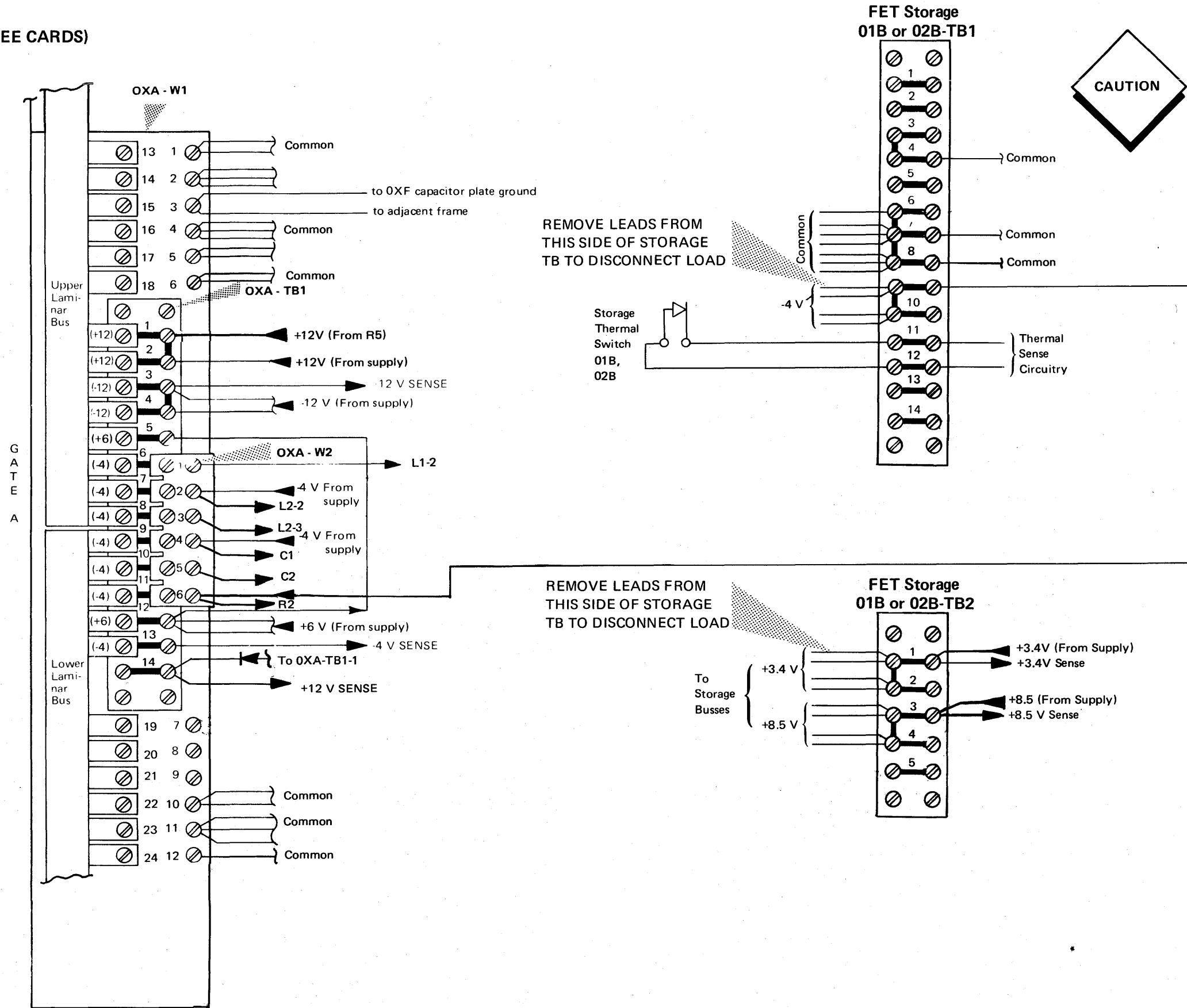


**3705-II POWER-ON SEQUENCE
(OXD GATE WITH ONLY TWO OR THREE CARDS)**

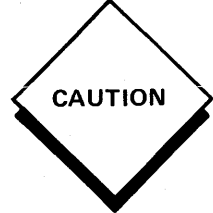
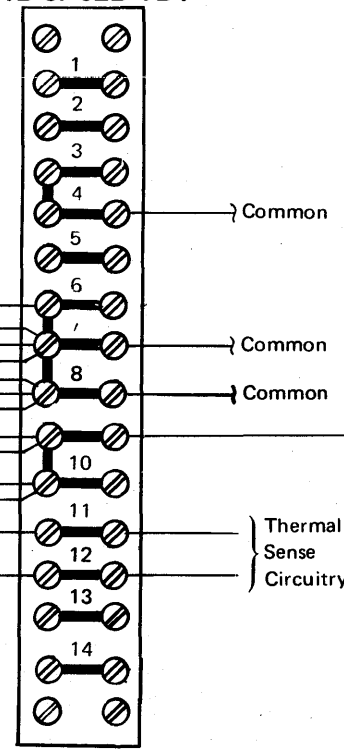
• Shows the sequence of events that occur during normal power-on operation (1) when the Local/Remote Power switch is set to the LOCAL position, and the Power On switch is depressed, or (2) when the Local/Remote Power switch is set to the REMOTE position, and the host CPU brings power up.

Contact or action causing pickup	Power Supply Components or Action	Timing Relationships
EPO-J (1, 2, 3, or 4)	PPB-K1 (EPO)	(+24 Vdc For Relays)
PPB-K1 #1 point		Remote position of Local/Remote Power Switch
Press Power On Switch	Power On switch or CPU Power On	Local position of Local/Remote Power Switch
Local Power On Switch or CPU Power On		
Local Power On Switch or CPU Power On	Power Check Light	
Local Power On Switch or CPU Power On	Power On Reset	
01D-C1 Transistor picks K2	PPB-K2 (ac to 3705)	
PPB-K2 # 4 point (3705)	PPB-K1 (ac to Expansion frame #1)	
PPB-K1 # 4 point (Expansion frame 1)	PPB-K1 (ac to Expansion frame #2)	
PPB-K1 # 4 point (Expansion frame 2)	PPB-K1 (ac to Expansion frame #3)	
ac applied to each frame		
01D-C1 transistor	+5V 'Start Sequencing' signal sent to each expansion frame	
01D-C1 transistor	12-second timer started	
-4 V up in each frame	-12V, +3.4V, and +6V sequence begins when -4V up in each frame	
-12V and +6V up in each frame	+12V sequence begins when +6V and -12V up in each frame	
+3.4V up in each frame	+8.5V sequence begins when +3.4V up in each frame	
+8.5 and +12V up in each frame	Sequence complete (all frames)	
Power-On sequence complete (every frame)	Power ON Light	+24 Vdc

**3705-II DC VOLTAGE DISTRIBUTION
(OXD GATE WITH ONLY TWO OR THREE CARDS)**



**FET Storage
01B or 02B-TB1**

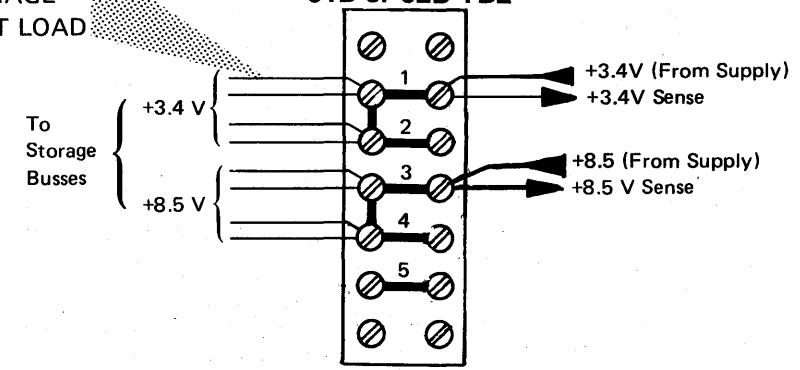


- Do not remove any of the wires labeled SENSE
- Do not remove any of the terminal board (TB) jumpers which connect a voltage with its sense lead.
- Do not bend the laminar bus tab too sharply because it may crack upon straightening.

REMOVE LEADS FROM THIS SIDE OF STORAGE TB TO DISCONNECT LOAD

REMOVE LEADS FROM THIS SIDE OF STORAGE TB TO DISCONNECT LOAD

**FET Storage
01B or 02B-TB2**



G
A
T
E
A

CHECKING +3.4V, +8.5V, +6V, ±12V and -4V SCRs (OXD GATE WITH ONLY TWO OR THREE CARDS)

Because the wave shapes for the +3.4V, +8.5V, -4V, +6V, and ±12V SCRs are similar, only representative samples are shown.

Note: The +3.4V, +8.5V, +6V and ±12V supplies are each associated with an individual pair of SCRs. The -4V supply is associated with three pairs of SCRs.

1. Setup the scope as follows:

- Sync the scope on LINE.
- Set horizontal sweep at 5ms/divn.
- Set the vertical sweep appropriate to voltage.

2. Put the scope probe on the heat sink for the voltage being tested (see chart below). See **1** or **2** for the location of the heat sink.

Voltage	Heat Sink
-4V	1, 2, and 3
+8.5V	4
-12V	5
+12V	6
+6V	7
+3.4V	8

3. There should be two pulses within 16.7 ms as shown in (20.0 ms for 50Hz).

- If one pulse is missing as shown in **4**, the problem is most likely an 'open SCR' or control card.

Note: A single SCR, firing alone for voltages other than -4V, does not sustain the output voltage and allow the 3705 power to remain on. During the power-on sequence, however, you will see the traces shown in **4** for a few seconds.

- To locate an 'open SCR', follow either Procedure A or Procedure B.

Procedure A

- Use two scope probes with the Vert-Volt/divn for the A and B traces at the same setting.
- Attach the A probe to the heat sink associated with the SCRs you are checking **1** or **2**.
- Attach the B probe to the cathode of either SCR.
- The wave shape displayed on the scope should resemble either **5** or **6** (vertical adjustment of

the traces may be necessary to obtain the proper display).

- The display (probe A) for the conducting SCR is shown in **5**, and the display for an 'open' SCR is shown in **6**.

See Note

Procedure B

- Turn off PPB-CB1.
- Remove (unsolder) lead from the gate of either SCR associated with the supply being tested.
- Turn on PPB-CB1 and power-on the 3705 while observing for the waveform shown at **4**.
- If the waveform at **4** appears, you have removed the gate connection from the open SCR. If no SCR fires, you have removed the gate from the good SCR.
- Turn off PPB-CB1 and replace the open SCR.

See Note

Note: Three pairs of SCRs are associated with -4V. Each pair of SCRs operates from one phase of the 3-phase input (refer to YZ530). The 3705 may operate with one or two phases missing, therefore, it is essential that each pair of SCRs be checked for an 'open' condition. Do not conclude that -4V SCRs are operating properly until each phase has been checked individually.

Locating a Shorted SCR

A shorted SCR is the principal cause of a tripped circuit breaker or circuit protector in a 3705-II.

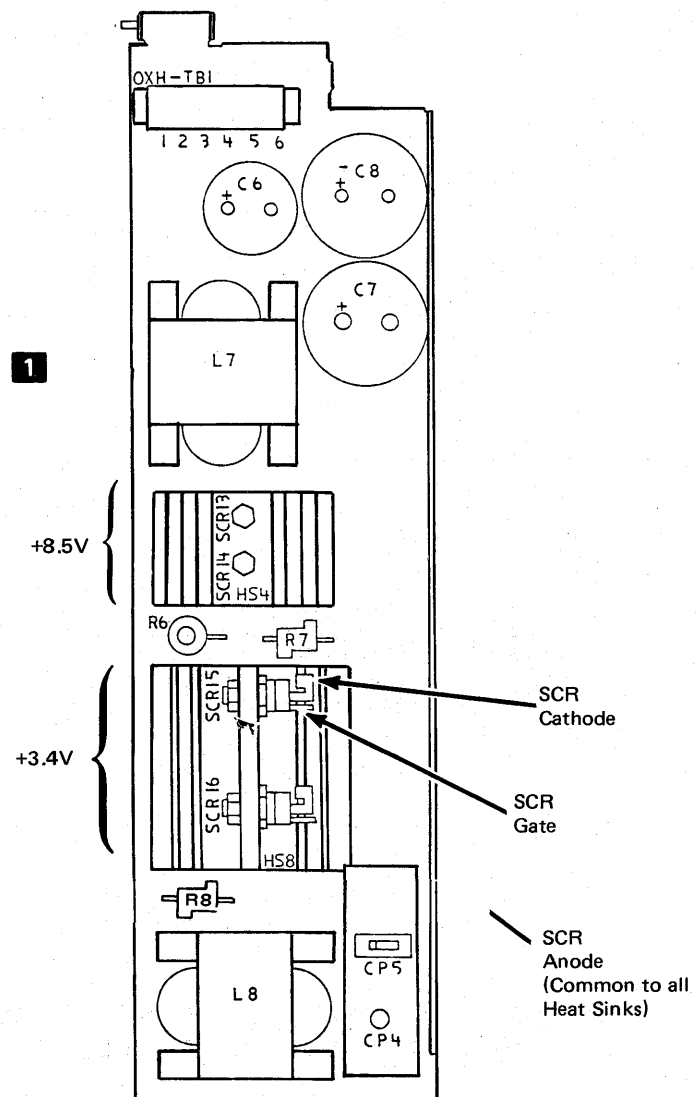
- If PPB-CB1 (main CB) trips during power-on of a 3705-II with only two or three cards in the OXD power control gate, the probable cause is a shorted SCR in the -4V dc power supply.
- If CP5 trips, the probable cause is a shorted SCR in the +3.4V dc power supply.
- A shorted SCR in the +6V, +8.5V, or ±12V dc power supply either acts like a fuse and opens the associated circuit, or causes one of the following conditions:
 - Overheats transformer wires.
 - Trips PPB-CB1 (main CB).
 - Trips CP1, CP2, CP3, or CP4.

Testing the SCR for Shorts

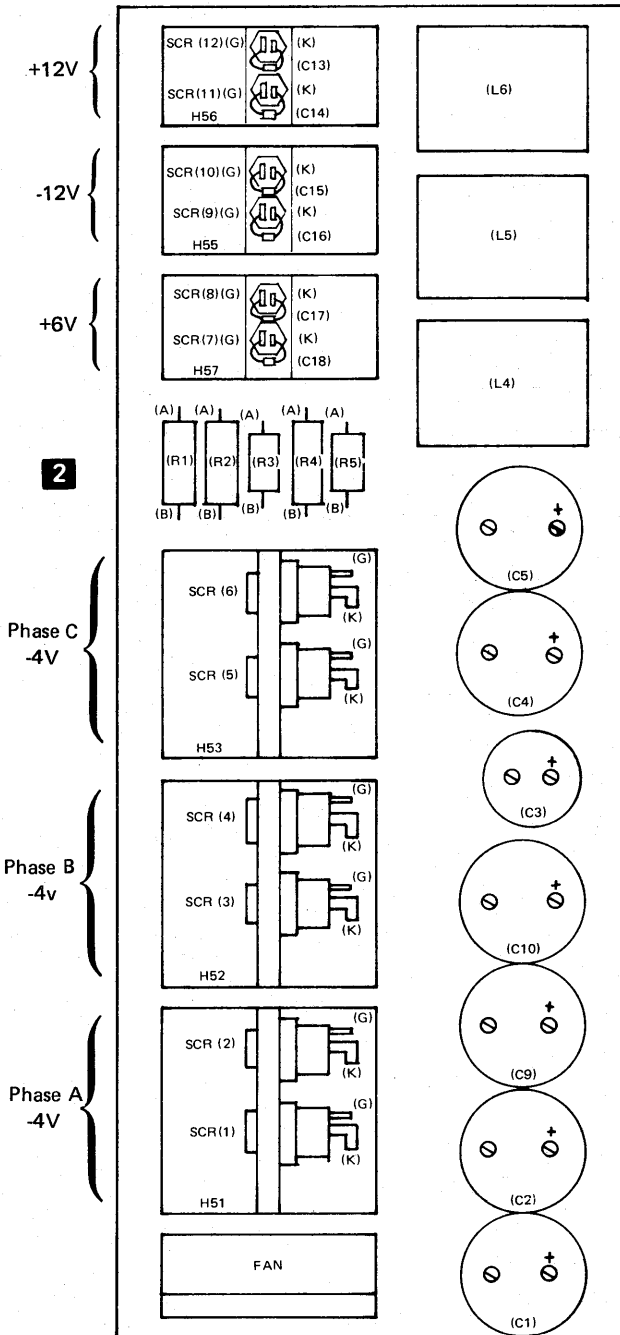
- Turn off PPB-CB1.
- Isolate the SCR to be tested.
 - Remove the power supply control card from OXD-A1A1.
 - Remove the cathode connection from the SCR. Note: For an SCR in the -4V supply, remove the cathode connection at the cathode. For SCRs in power supplies other than -4V, remove the cathode connection at T3-TB2 (refer to YZ530).
- Test for 'anode' to 'cathode' shorts. Use an ohmmeter to determine which SCR is shorted. A shorted SCR may appear as a direct short with a low resistance between the cathode and anode, or may appear as a diode, with a high resistance in one direction and a low resistance in the other. A good SCR has a high reading between the cathode and anode in both directions. Check all SCRs associated with the failing power supply.
- Test for 'gate' to 'cathode' shorts. Use an ohmmeter to measure the resistance between the gate and cathode of each SCR (see **7**). Readings of 50 ohms or greater in both forward and reversed directions indicate no short. A reading of only a few ohms indicates a short.
- Unsolder the leads to the bad SCR.
- Remove the nut and lockwasher that hold the SCR to the heat sink and remove SCR.
- Mount the new SCR on heat sink.
- Resolder leads to proper SCR terminals. Turn on PPB-CB1 and power up to verify the repair.

CHECKING +3.4V, +8.5V, +6V, +12V AND -4V SCRs--Part 2
(0XD GATE WITH ONLY TWO OR THREE CARDS)

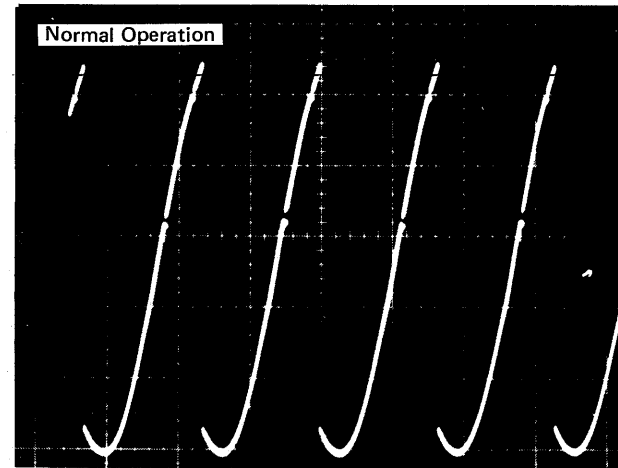
Power Supply Mounting Assembly (0XH)
+3.4V and +8.5V



Power Supply Mounting Assembly (0XF)
-4V, +6V, and ±12V

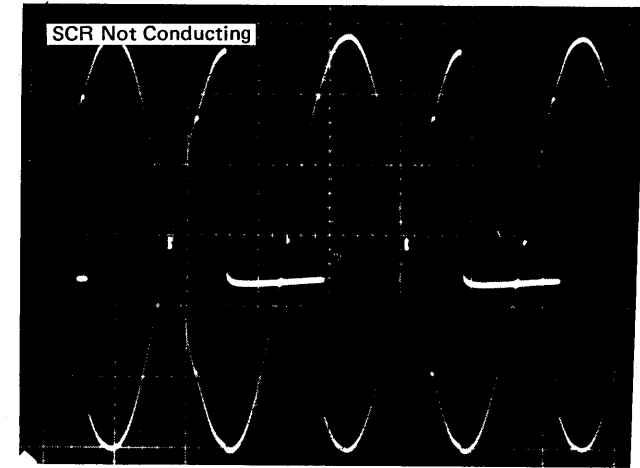


3

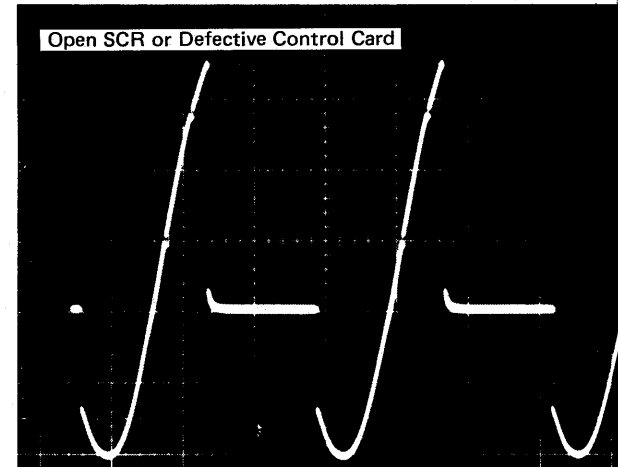


Horz - 2 ms/divn
Vert - Appropriate to Voltage Under Test
Sync - Line

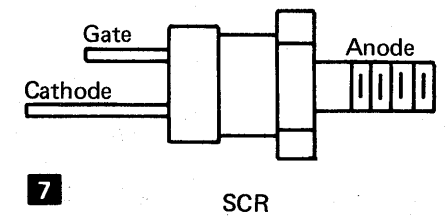
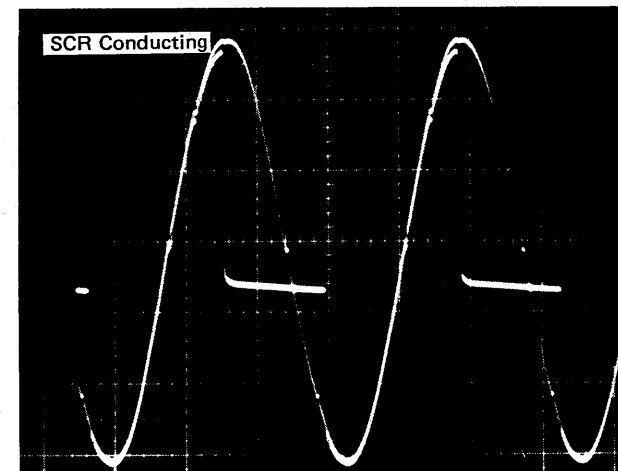
6



4



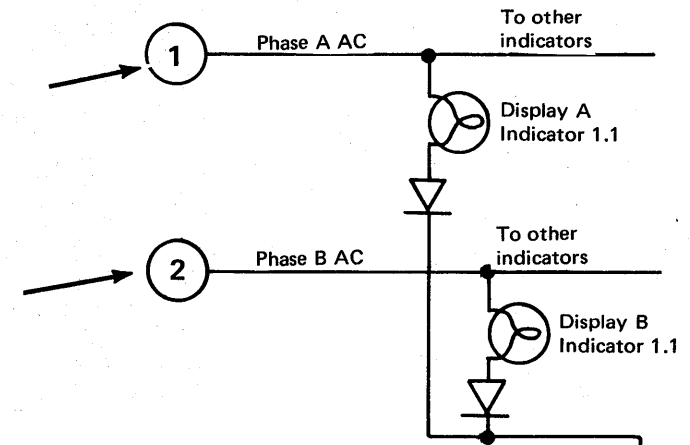
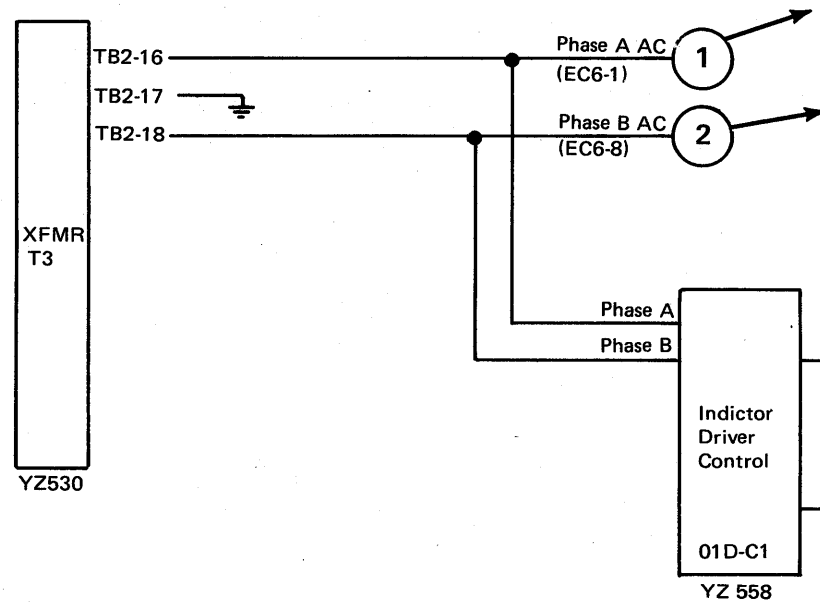
5



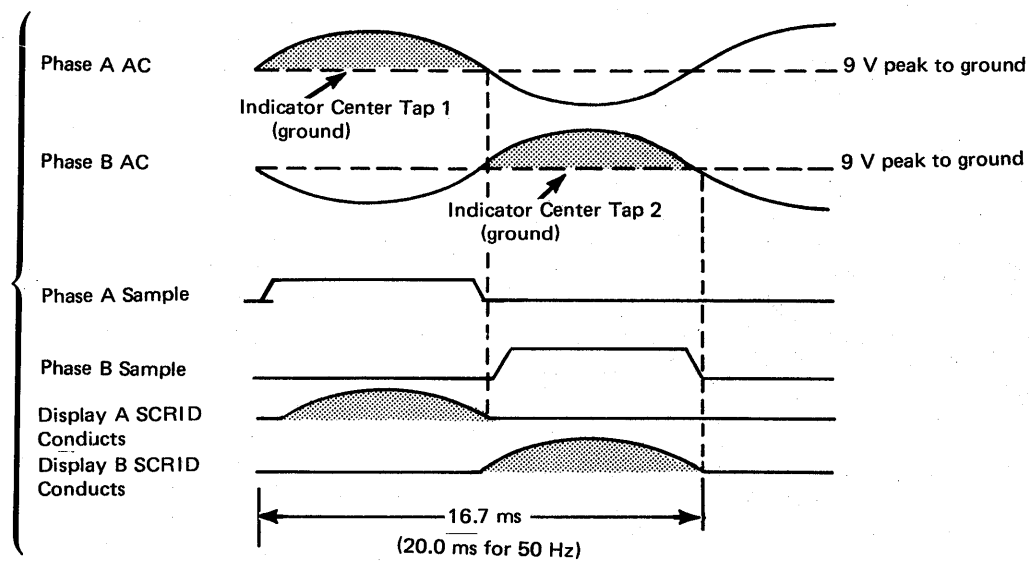
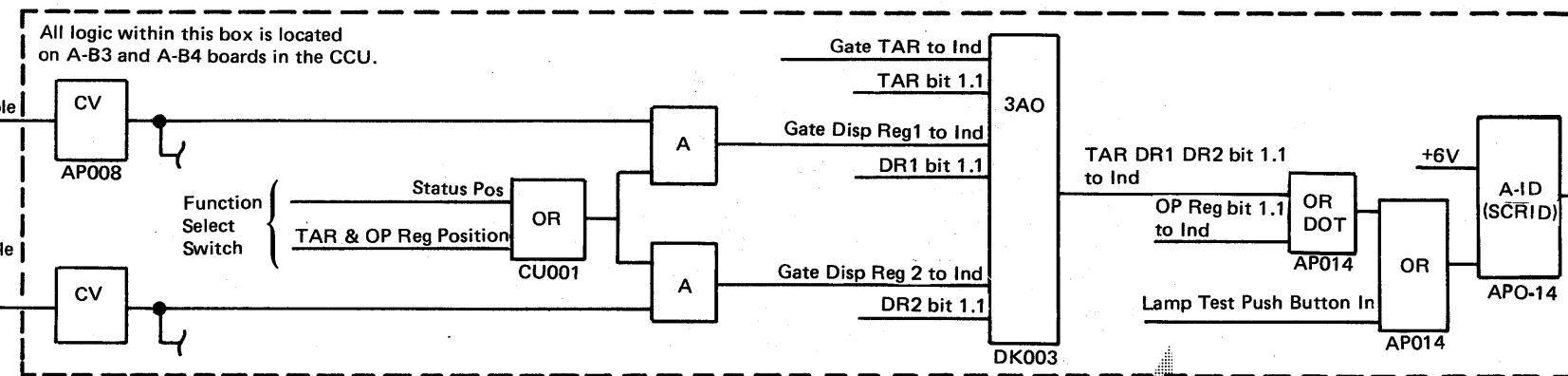
7

INDICATOR LIGHTS—SUPPLY/CONTROL
 (OXD GATE WITH ONLY TWO OR THREE CARDS)

One center-tapped winding of T3 is used for the indicator lights. The center-tapped winding is divided into phase A (when TB2-16 is positive with respect to TB2-17) and phase B (when TB2-18 is positive with respect to TB2-17)



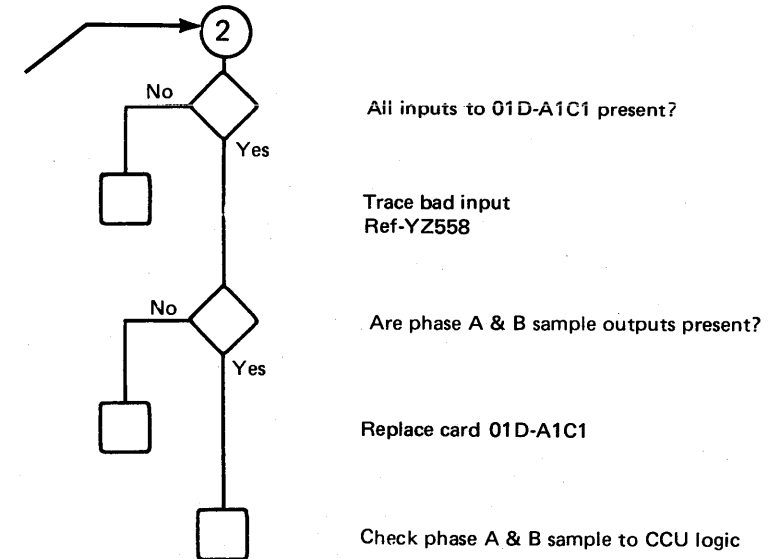
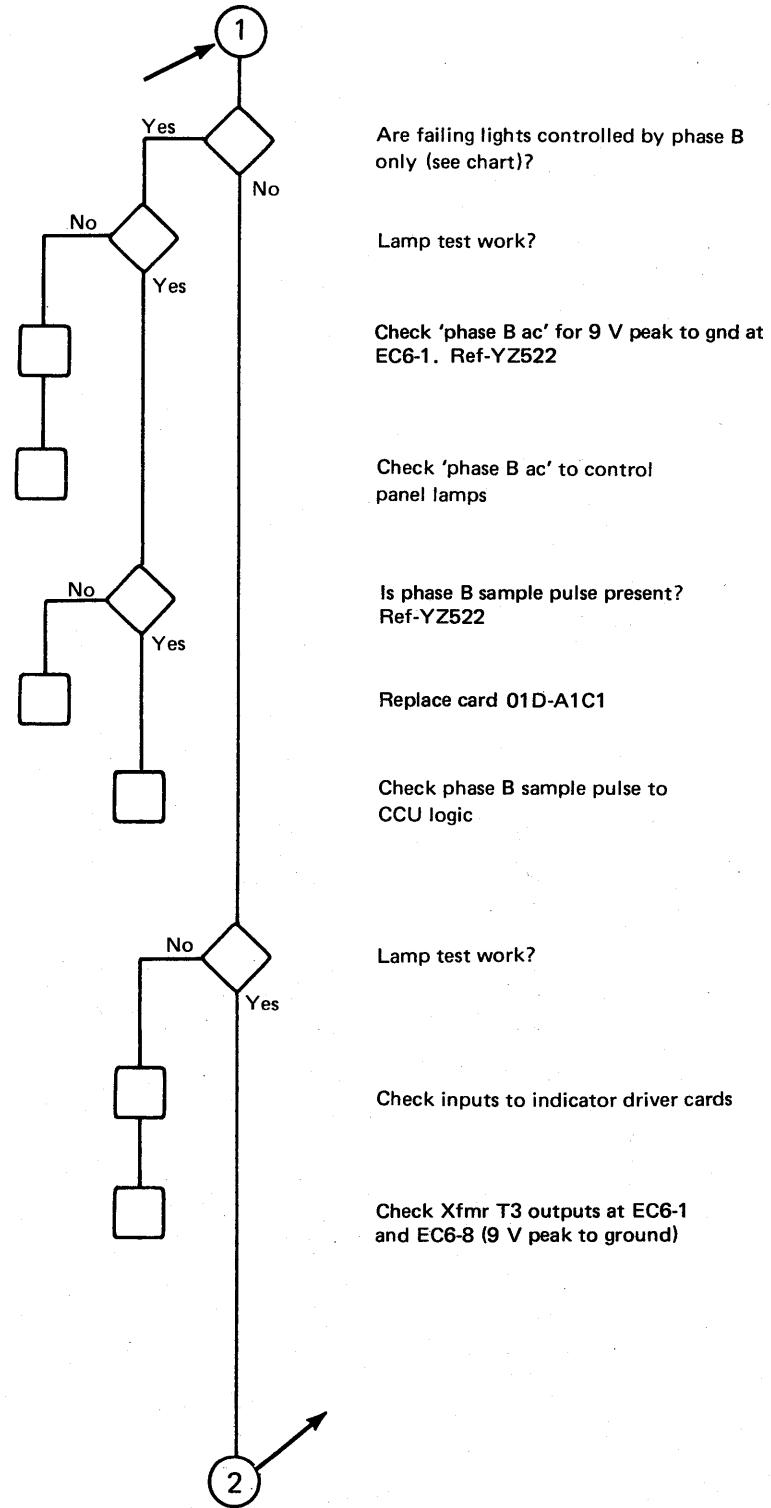
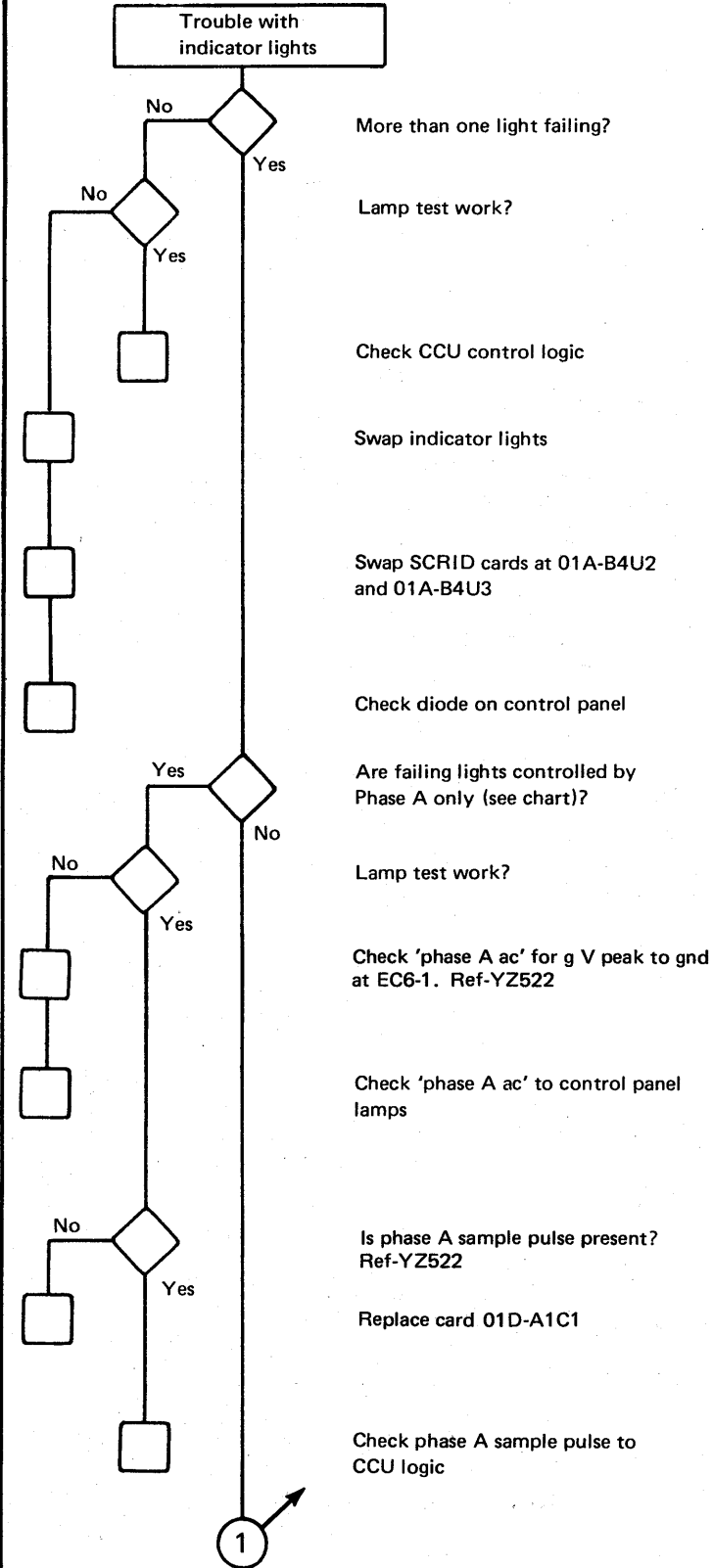
The logic shown is for byte 1, bit 1 and represents the CCU logic to turn on the indicators.



Note: When the Lamp Test push button is pressed, the intensity of the indicator lights will decrease.

**INDICATOR LIGHTS—CHARTS AND PROCEDURES
(0XD GATE WITH ONLY TWO OR THREE CARDS)**

Refer to D-570 for logic and timings



Indicator Driver Card (SCRID)	Phase A ac	Phase B ac	Logic page
	Indicator Display A	Indicator Display B	
01A-B4U2	0.0	0.0	AP012
	0.1	0.1	AP012
	0.2	0.2	
	0.3	0.3	
	0.4	0.4	AP013
	0.5	0.5	AP013
	0.6	0.6	
0.7	0.7		
01A-B4U2	1.0	1.0	AP014
	1.1	1.1	AP014
	1.2	1.2	
	1.3	1.3	
	1.4	1.4	AP015
	1.5	1.5	AP015
	1.6	1.6	
1.7	1.7		
01A-B4U3	Chan 1 Intf A Enbl	Chan 1 Intf B Enbl	AP009
	Chan 2 Intf A Enbl	Chan 2 Intf B Enbl	
	Panel Active		
		CCU Check	AP009
	Spare Spare Hard Stop Wait	Spare Pgm Display Test Pgm Stop	AP010
01A-B4U3	Load X.4	X.4	AP011
	X.5	X.5	
	X.6	X.6	
	X.7	X.7	

**DC VOLTAGE MEASUREMENT
(OXD GATE WITH ONLY TWO OR THREE CARDS)**

- Voltages should be set using a digital voltmeter.

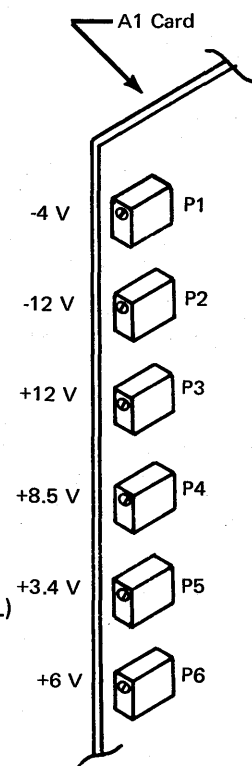
Voltage	Voltage Measurement	Location of Voltage Adjustment Potentiometer on Card OXD-A1C1	Maximum Ripple (peak to peak)
-4V	B06 on any board	P1	80mV
-12V	OXA-TB1-3	P2	480mV
+12V	OXA-TB1-1	P3	480mV
+8.5V	OXB-A1J2D07	P4	200mV
+3.4V	OXB-A1J2D03	P5	80mV
+6V	OXA-TB1-T2	P6	240mV

3705-II basic frame
(Also on first expansion frame of Models J, K, and L)

Power Supply Regulation And Maximum Current

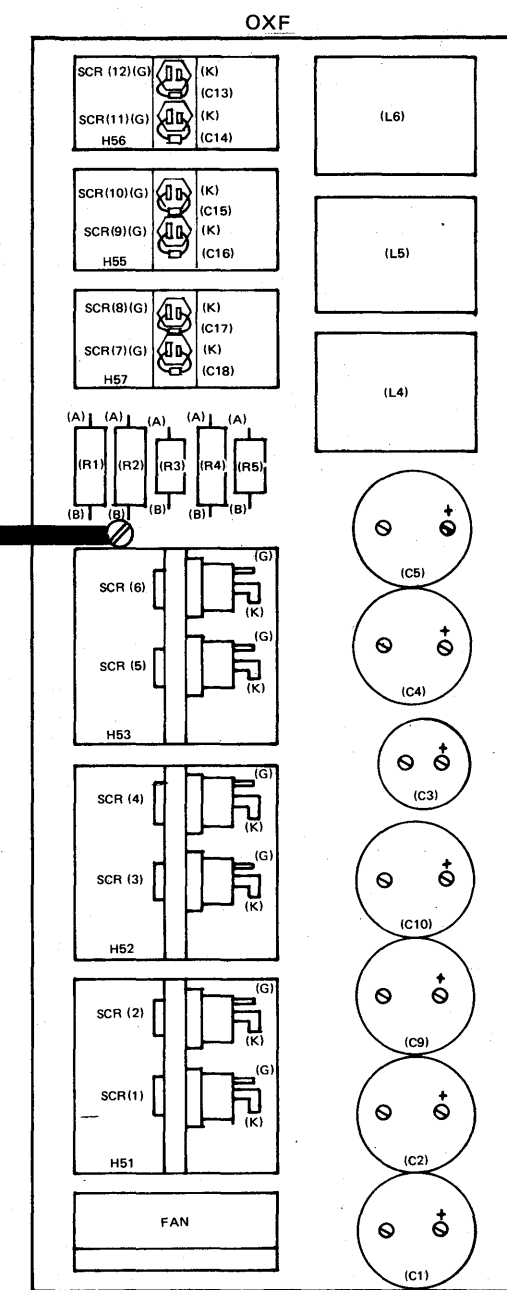
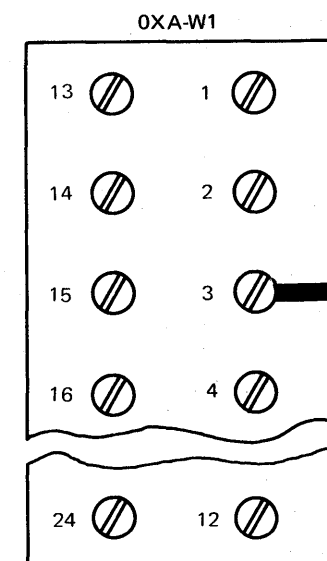
Voltage	Power Supply Regulation	Maximum Rated Output Current	
		3705	Each expansion frame
-12 V	+0.84V	9A	9A
- 4 V	+0.16 V	200A	200A
+ 6 V	+0.24 V	8A	8A
+12 V	+0.84V	14A	14A
+3.4 V	+0.20V	34A	
+8.5 V	+0.43V	10.6A	

3705-II basic frame or first expansion frame on Models J, K, and L only



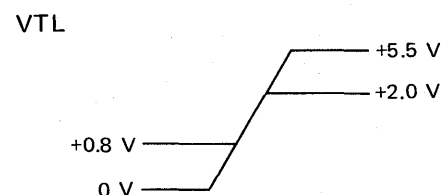
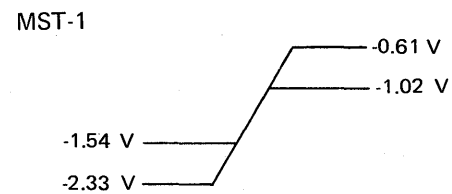
DC Common--Frame Ground Connection

- dc common and frame ground are tied together in each 3705 and expansion frame by a wire that connects jumper bus OXA-W1-3 to the plate base. See YZ536.
- Eight jumper assemblies (P/N 1770813) are mounted between frame ground (at board mounting screws) and the dc signal ground pin positions for each logic board located on gate (s) OXA.

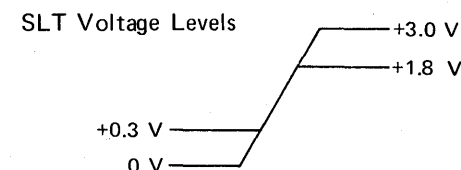
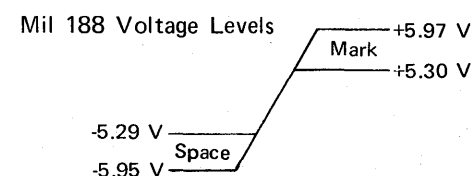
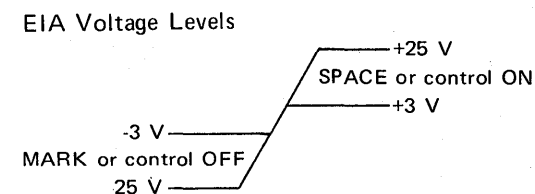


Power Supply Mounting Asm.

LOGIC VOLTAGE LEVELS

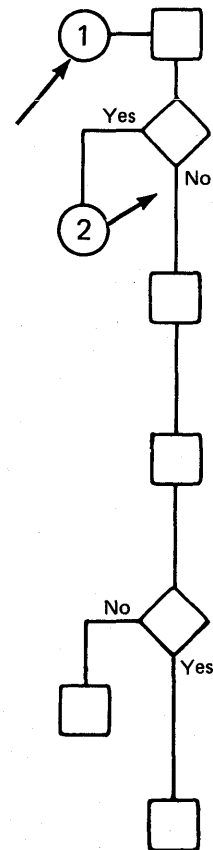
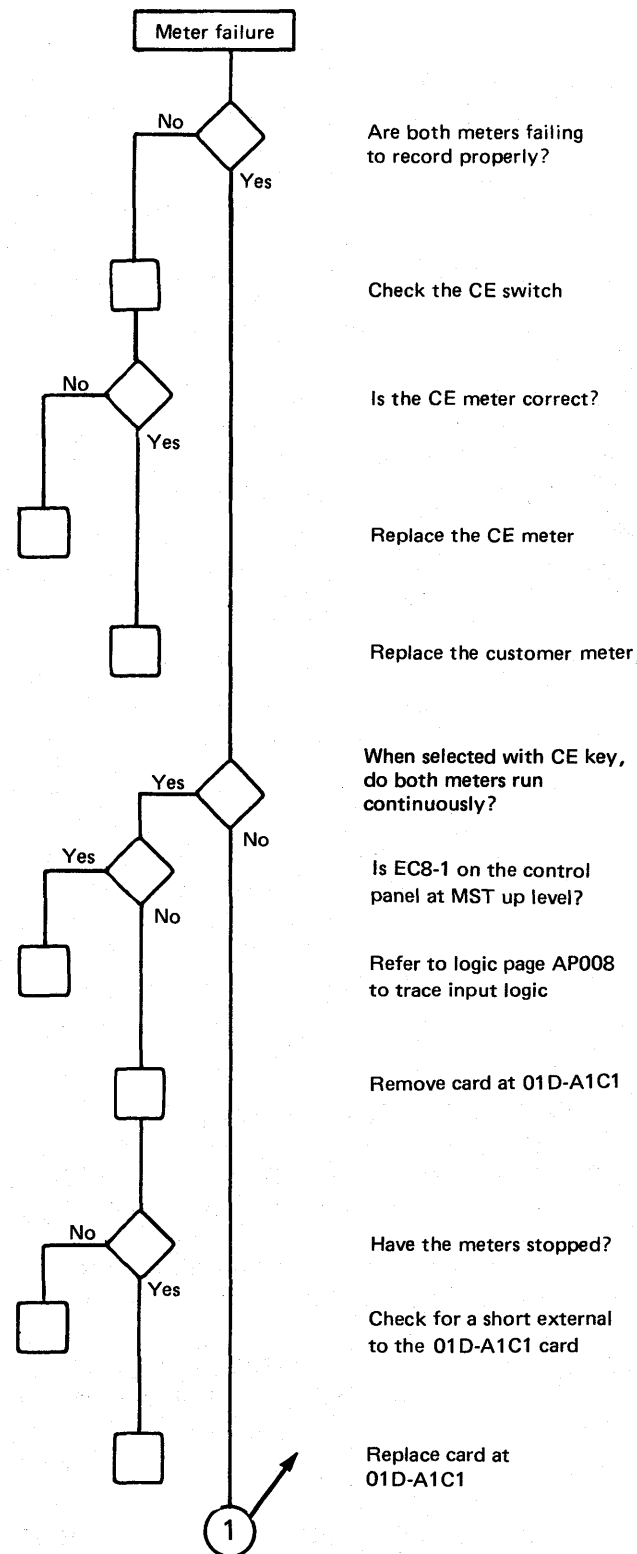


Digital Levels
SPACE or control ON - 23 ma (+1 V)
MARK or control OFF - 5 ma (-0.7 V)
Open circuit - control OFF



USAGE METER (OXD GATE WITH ONLY TWO OR THREE CARDS)

See 1-030 for the conditions that cause the usage meter to run.



Attach a jumper between TB1-12 and M2B (meter) on the 01D gate (YZ522, YZ524)

Are the meters running now?

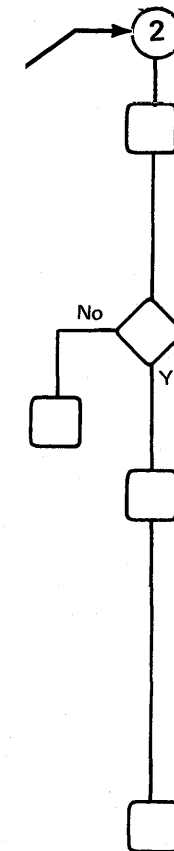
Remove the jumper (TB1-12 to M2B)

Measure for 40Vrms between TB2-19 and TB2-20 on T3 output (YZ524, YZ530)

Is the 40V correct?

Replace transformer T3 (See Note)

Check wiring and connectors



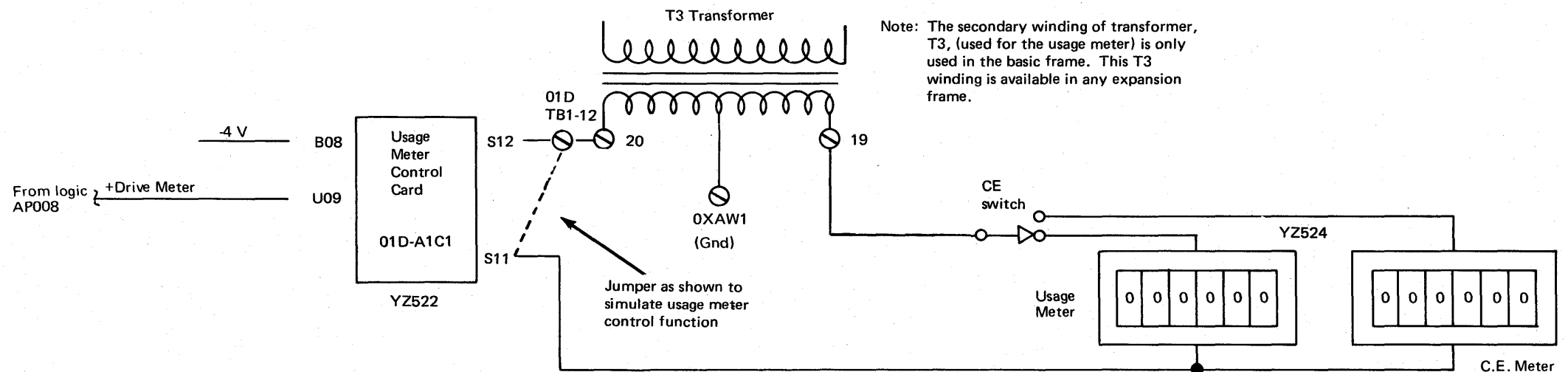
Remove the jumper (TB1-12 to M2B)

Is EC8-1 on the control panel at MST up level (YZ522)?

Refer to logic page AP008 to trace input logic

Check the -4V circuitry

Replace card at 01D-A1C1



3705-II POWER MAINTENANCE ANALYSIS PROCEDURES (MAPs)

POWER ON SEQUENCE

- These MAPs are based on the fact that a failure results in the power-on sequence hanging at the failure point.
- A procedure to isolate the failing frame for power-on problems on multiframe machines is included.
- Check lists used in the MAPs are not all inclusive, but assist you in locating the problem more readily. Following the check list is a logic page reference for your use when the check list does not pin point the problem.

Notes:

1. +24 Vdc can be +20 V to +35 V depending on loading and input line voltage.
2. -24 Vdc can be -20 V to -35 V depending on loading and input line voltage.
3. +30 Vdc can be +25 V to +40 V depending on loading and input line voltage.
4. Verify that all CPU interfaces are disabled to avoid channel errors when powering down.

SAFETY Observe normal safety practices when servicing this power supply.

Power must be off in the 3705 whenever a card is to be substituted or replaced. You must turn off CB1 (on PPB) before replacing cards in the OXD gate. Otherwise, unpredictable LED indications may occur.



Connect the I/O interface cables to bypass the 3705 when you are working on a power supply voltage sequence problem. The 3705 relies on power sequencing during power on and off to prevent the drivers and receivers from generating noise on the channel interface signal lines.

INTERPRETATION OF DECISION BLOCK PATHS (RELAY OPERATION)

Yes—Normal operation in which the relay picks and holds according to the power-on sequence chart on D-250 and drops according to the power-off sequence chart on page D-450.

No—The relay fails to pick.

Momentarily picks but doesn't hold—Do not take either the Yes or No path. This is a failure and you should determine why the relay did not hold up.

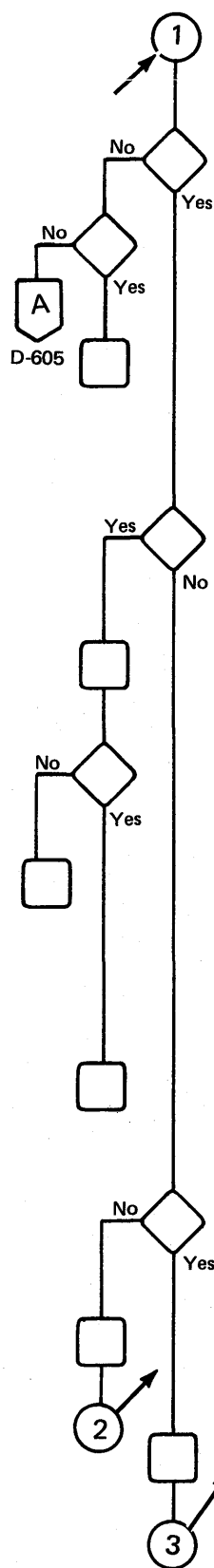
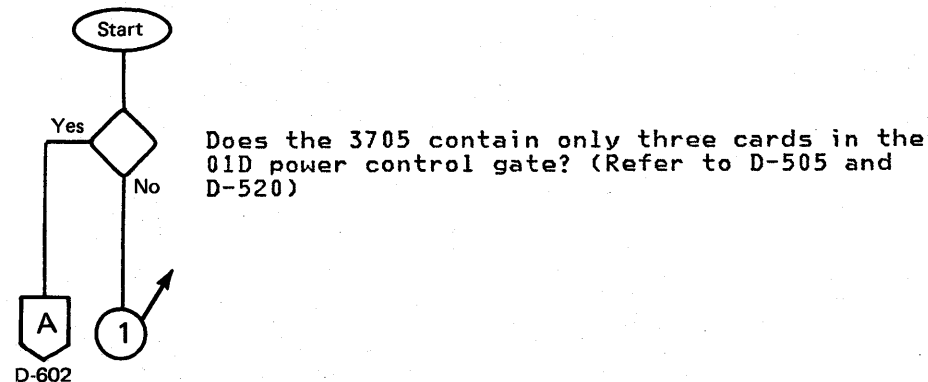
POWER SYSTEM IDENTIFICATION

A 3705-II basic frame or expansion frame can contain either a standard power system or a modified version of the standard power system.

Before using the power MAPs, you must determine the type of power system installed in the 3705-II basic frame and each of the attached expansion frames. The type of power system installed in each frame can be identified by examining the power control gate (D-gate). If the D-gate in an individual frame contains more than three cards, a standard power system is installed in that frame. If the D-gate contains only three cards (basic frame) or two cards (expansion frame), a modified power system is installed in the frame. Frames with either of the power systems installed can be attached to each other. (An expansion frame without modified power must contain RPO S30251 before attachment can be made to a basic frame with modified power.)

The Power MAPs are arranged in the following sequence.
Page MAP

D-600	FRAME ISOLATION—BASIC FRAME WITHOUT MODIFIED POWER SYSTEM
D-602	FRAME ISOLATION—BASIC FRAME WITH MODIFIED POWER SYSTEM
D-605	PROBLEM ISOLATION IN A FAILING BASIC FRAME WITHOUT MODIFIED POWER SYSTEM
D-610	PROBLEM ISOLATION IN A FAILING FRAME WITHOUT MODIFIED POWER SYSTEM
D-620	PROBLEM ISOLATION IN A FAILING BASIC FRAME WITH MODIFIED POWER SYSTEM
D-630	PROBLEM ISOLATION IN A FAILING EXPANSION FRAME WITH MODIFIED POWER SYSTEM
D-640	-4V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM
D-645	+3.4V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM
D-650	+8.5V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM
D-655	+6V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM
D-660	-12V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM
D-655	+12V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM
D-670	OVERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM



Is the POWER CHECK light on ?

Is the 3705 powered up but cannot be powered down?

- Observe relay 01E-RY6 while pressing the POWER OFF switch.
- Verify that the POWER OFF switch opens and that relay 01E-RY6 in the first frame drops (YZ053).

Is 01E-RY10 picked (thermal sense relay, YZ054)?

Press the THERMAL RESET switch on the 01E gate.

Does 01E-RY10 remain dropped even when the switch is released?

- Jumper out the thermal switches (01E-JXQ to 01E-JXR, YZ054) one frame at a time until 01E-RY10 drops when the THERMAL RESET switch is pressed and released.
- Check the air filters and blowers in the last frame jumpered out.

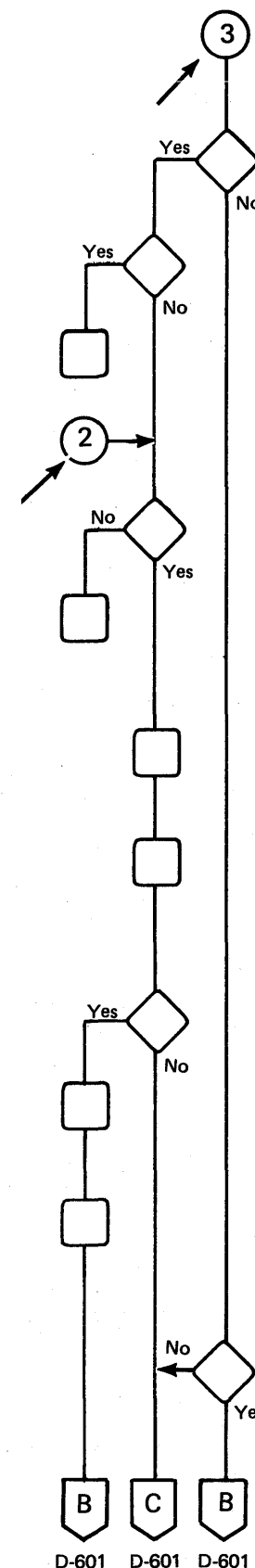
*The thermal condition is gone (thermal switch has dropped).

- Check all air filters and blowers.

Did the power check occur during the initial power-on sequence?

*The power check occurred after the power-on sequence was completed.

- Check the 3 phase AC input voltage at 01D-A1B2B02, 01D-A1C2B02 and 01D-A1D2B02 (YZ111). See scope pictures on D-200.
- Check the 3 phase AC reference voltage at 01D-A1B2D13, 01D-A1C2D13 and 01D-A1D2D13 (YZ111). See scope pictures on D-200.



Did 01E-RY3 pick during the power-on sequence (sequence complete relay, YZ053)?

Is 01E-RY3 still picked?

- *Possible false indication.
- Check for shorted points at:
01E-RY11-3 N/O
01E-RY3-10 N/C
01E-RY10-4 N/O

Is 01E-RY11 picked (fault sense relay)?

- Check CBs and CPs (refer to D-330 for basic frame and D-340 or D-535 for expansion frame).

Check CBs and CPs in the basic frame (refer to D-330).

Check the LEDs on the 01D gate of the basic frame to determine the failing power supply (refer to "3705-II FAULT INDICATORS" on page D-320).

Are any expansion frames present?

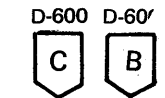
Check the CBs and CPs in the expansion frames (refer to D-340 and D-535).

Check the LEDs on the 01D gate of the expansion frames to determine the failing power supply (refer to "3705-II FAULT INDICATORS" on page D-320 or D-520).

Are any expansion frames present?

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

FRAME ISOLATION—BASIC FRAME WITHOUT MODIFIED POWER SYSTEM (01D GATE WITH MORE THAN THREE CARDS)—PART 2 OF 2



- Turn off PPB-CB1 (main circuit breaker in 3705).
- Disconnect the lead from the POWER OFF switch 'B' side common (prevents FAULT SENSE when no frames are connected at the 01E gate).
- Pull the power control cable located at 01E-P1.

- To prevent a thermal condition, turn off PPB-CB1 (main circuit breaker in 3705).
- Pull the power control cable plug associated with the frame farthest from the 3705.

Frame Position	Cable Plug Position
Expansion frame 3	01E-P4
Expansion frame 2	01E-P3
Expansion frame 1	01E-P2
3705	01E-P1

- Insert the dummy paddle card PN 5993207 in the position of the removed power control cable plug. The dummy paddle card is included in the shipping group.
- Turn off PPB-CB1.
- Press POWER ON.

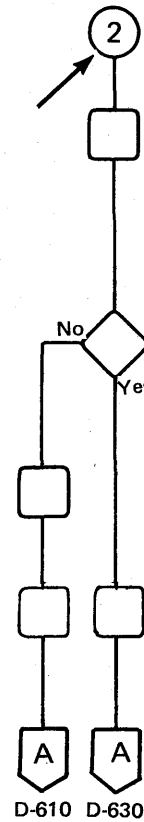
Does the 3705 power on now?

- Press POWER OFF.
- Turn on PPB-CB1.
- Remove the inserted dummy paddle card and replug the removed power control cable.

Was the 01E-P1 plug the last plug removed?

- Pull the power control cable plug for the next frame.

- *The trouble is common to all frames.
- Reconnect the lead to the POWER OFF switch 'B' side common if applicable.
- Turn on PPB-CB1.



- *The trouble is in the bypassed frame.
- Press POWER OFF.
- Turn off PPB-CB1.
- Remove the inserted dummy paddle card and replug the removed power control cable.
- Turn on PPB-CB1.

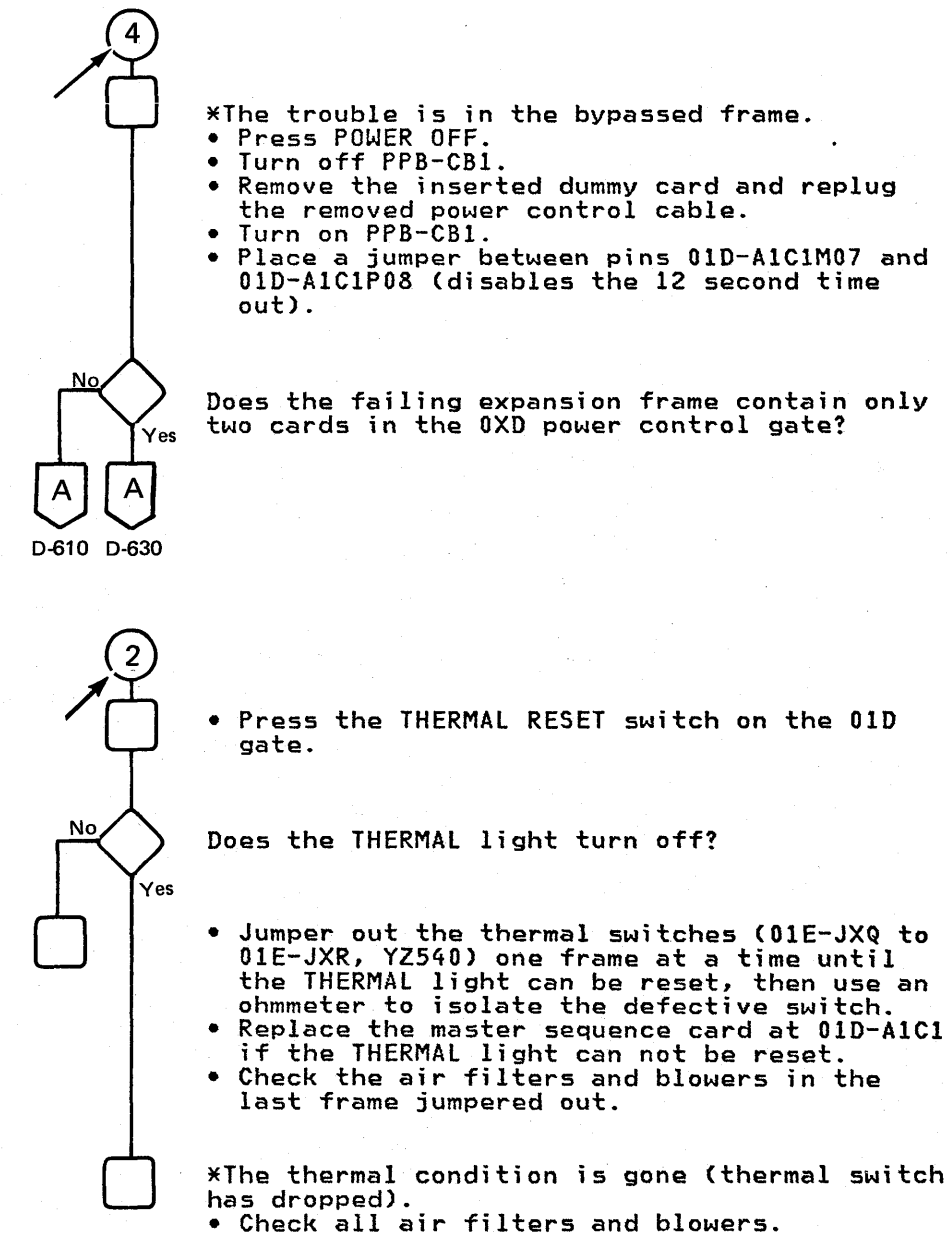
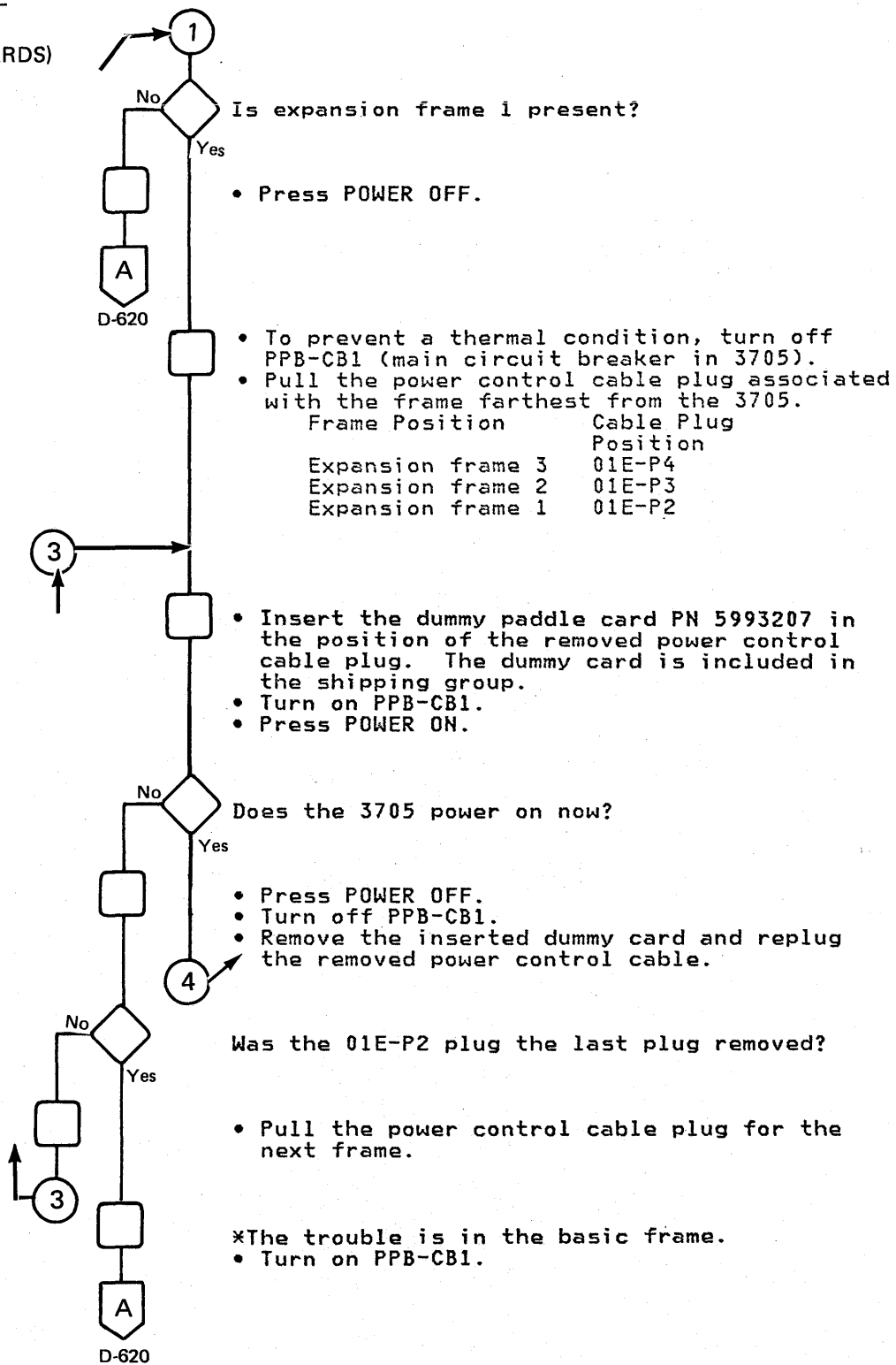
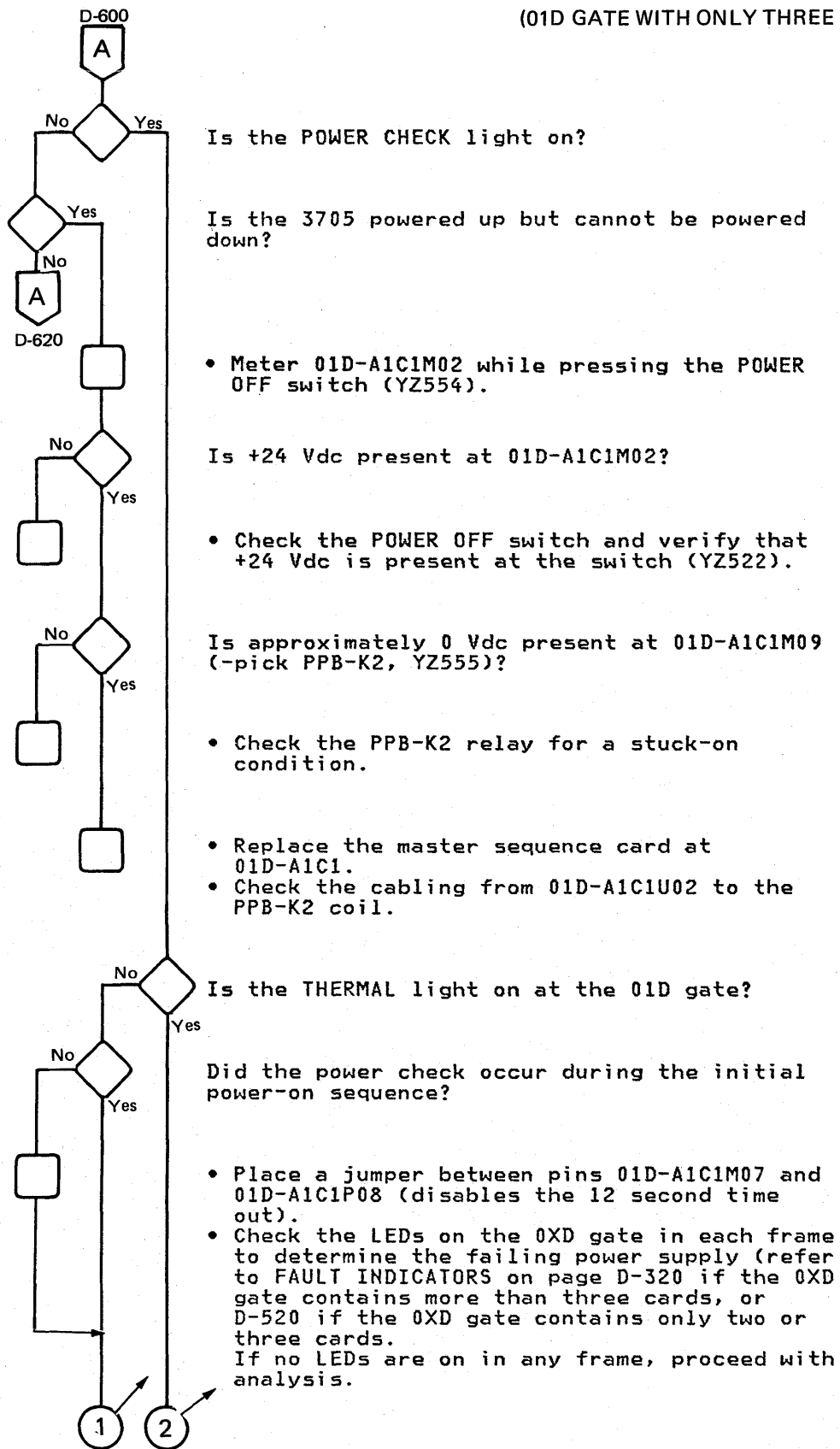
Does the failing frame contain only two cards in the 0XD power control gate? (Refer to D-505 and D-520.)

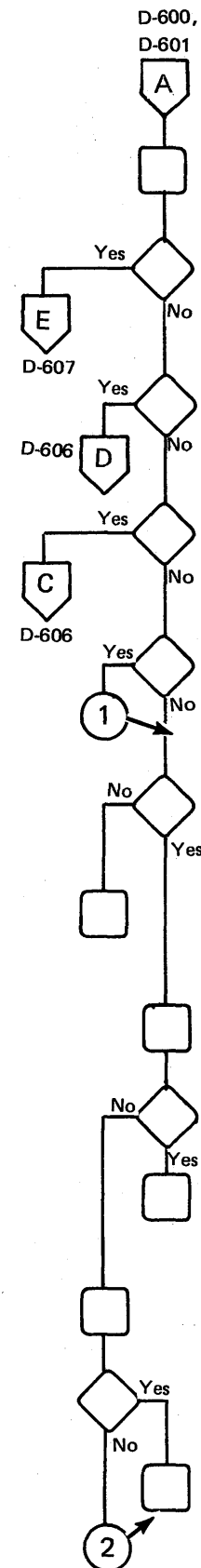
- Reconnect the lead to the POWER OFF switch 'B' side common if applicable.
- Check for loose cables and cards on the 0XD gate.



**3705-II POWER—MAINTENANCE
ANALYSIS PROCEDURES (MAPs)**

**FRAME ISOLATION—BASIC FRAME
WITH MODIFIED POWER SYSTEM
(01D GATE WITH ONLY THREE CARDS)**





- Press POWER OFF.
- Press POWER ON.

Is 01E-RY2 picked (+6V up, YZ056)?

Is 01E-RY1 picked (-4V, +12V, -12V up)?

Is 01E-HD1 picked (contactors on, YZ055)?

Is PPB-K1 picked (EPO, YZ051)?

Is the EPO cable plugged in the appropriate connector?

- Plug the EPO cable into the appropriate connector.

- Temporarily jumper EPO-JX pins 1 to 2.

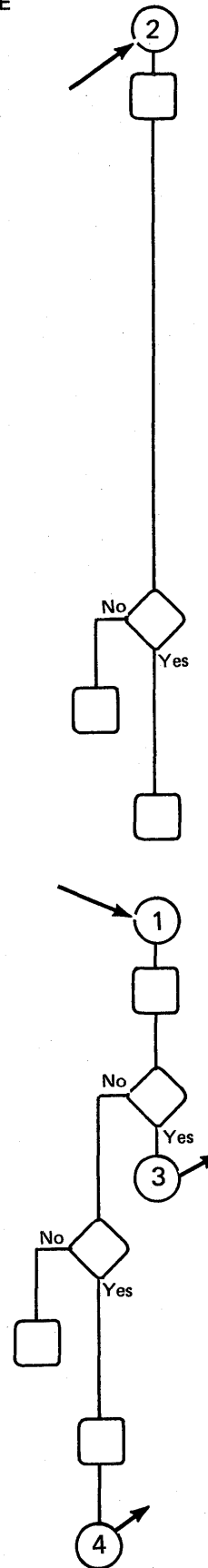
Does PPB-K1 pick?

- Remove the EPO-JX jumper.
- Check the EPO cable and associated CPU.

- Remove the EPO-JX jumper.

Is +24 Vdc present at EPO-JX pin 1?

- Check for an open coil on PPB-K1.



- Remove the rectifier card from socket PPB-T2-J1.
- Use an ac meter to measure between the PPB-T2-J1 connectors and PPB-TB4-1 (see chart below).
Expected voltage from 24.2 to 33.3 Vac rms between pins:
PPB-TB4-1 to R
PPB-TB4-1 to D
PPB-TB4-1 to E
PPB-TB4-1 to H
PPB-TB4-1 to J
PPB-TB4-1 to M
Expected voltage from 19.2 to 26.4 Vac rms between pins:
PPB-TB4-1 to B
PPB-TB4-1 to C
PPB-TB4-1 to F
PPB-TB4-1 to G
PPB-TB4-1 to K
PPB-TB4-1 to L

Are all voltages within the specified range?

- Check PPB-CP2, PPB-CB2, PPB-CB1 and the input voltage (see D-330).

- Replace the 3705 PPB-SMS rectifier card (mounted on transformer PPB-T2).

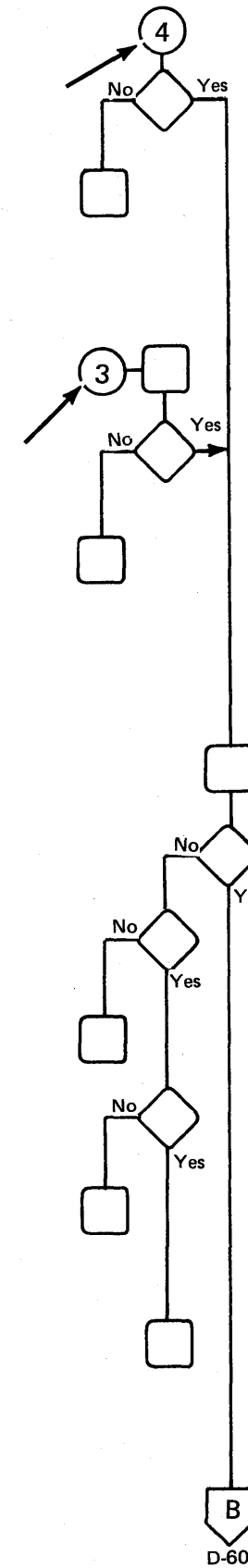
*+24V is now present at sequence relays.
*AC power is present at convenience outlets.

Is the LOCAL/REMOTE switch in the local position?

Is 01E-RY9 picked?

- Check the LOCAL/REMOTE switch.
- Check the PPB-K1-1 points.

*A CPU or channel power-on must be initiated to provide a contact closure within the CPU. This closure returns +24 Vdc to the EPO panel (JX-6).



Does 01E-RY6 pick (YZ053)?

- Check for +24 Vdc at:
(1) 01E-RY3-5 op
(2) 01E-RY9-1 op
(3) POWER OFF switch
- Check for ground at 01E-RY11-4 N/C.

*POWER ON pushbutton must be pressed.

Is 01E-RY6 picked (YZ053)?

- With POWER ON pressed, check for +24 Vdc at:
(1) POWER ON switch
(2) 01E-RY3-4 op
(3) 01E-RY9-1 op
(4) POWER OFF switch
- Check for ground at 01E-RY11-4 N/C.

*Power on reset begins

Is +24 Vdc present at 01E-RY6-11 op (YZ055)?

Is +24 Vdc present at 01E-RY3-11 N/C?

- Repair the 01E-RY3-11 points.

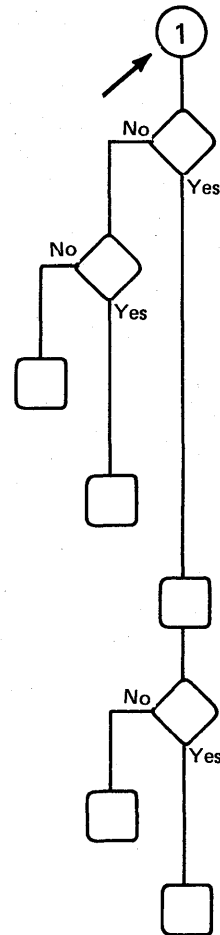
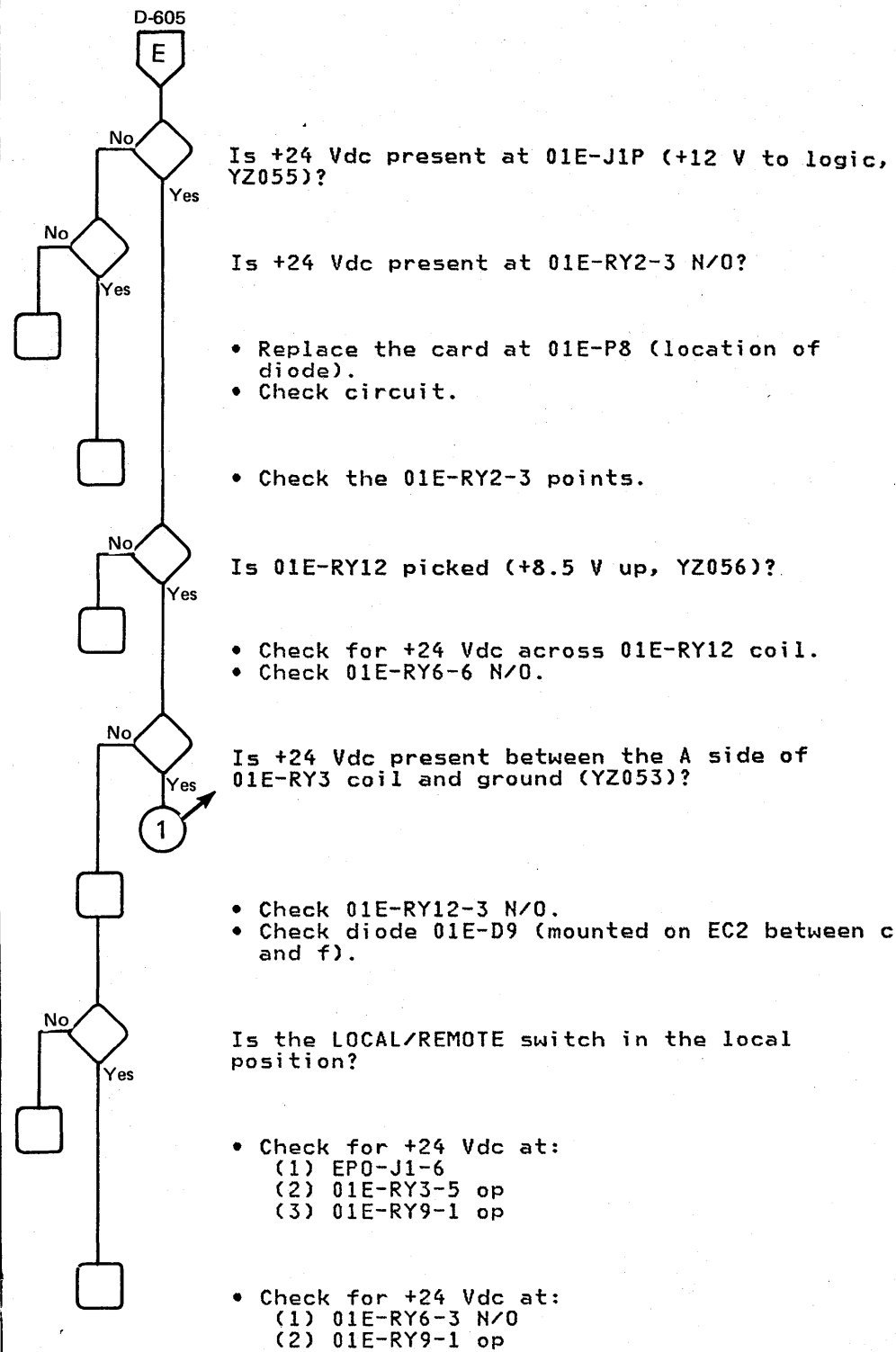
Is +24 Vdc present at 01E-J8C?

- Replace the card at 01E-P8 (location of diode).
- Check circuit.

- Check the 01E-RY6-11 points.

**3705-II POWER—MAINTENANCE
 ANALYSIS PROCEDURES (MAPs)**

**PROBLEM ISOLATION IN A FAILING
 BASIC FRAME WITHOUT MODIFIED
 POWER SYSTEM (01D GATE WITH MORE
 THAN THREE CARDS)—PART 3 OF 3**



Is approximately 0 Vdc present at 01E-RY3 B coil side?

Is 01E-RY3-2 N/O shorted (instant drop of time delay)?

- Replace the card at 01E-P8.
- Check circuit.

- Repair the 01E-RY3-2 points.

- Swap 01E-RY3 and 01E-RY6.
- Press POWER ON.

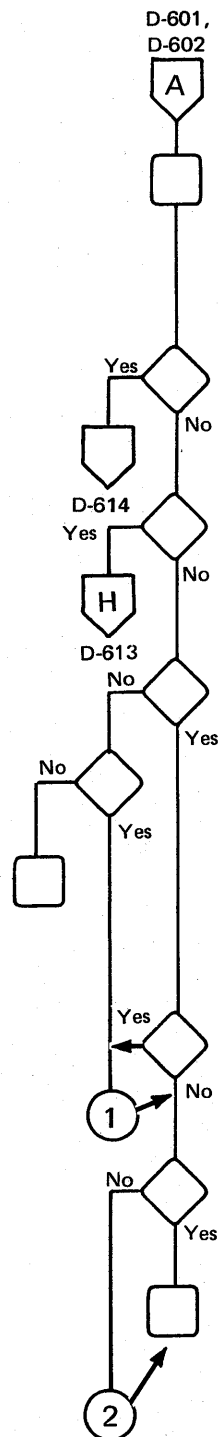
Does the relay in the 01E-RY6 position pick?

- Replace the relay in the 01E-RY6 position.

- Check the 01E-RY3 base contacts.

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

PROBLEM ISOLATION IN A FAILING FRAME WITHOUT MODIFIED POWER SYSTEM (0XD GATE WITH MORE THAN THREE CARDS)—PART 1 OF 7



- Remove the jumper between pins 0XB-A1V1B11 and 0XB-A1V1B13 if the 0XB gate is present (prevents +3.4V and +8.5V from sequencing up).
- Press POWER ON.

Is +24 Vdc present at 01E-JXH (+6V up, YZ056)?

Is +24 Vdc present at 01E-JXK (-4V, +12V, -12V up)?

Is the failing frame an expansion frame?

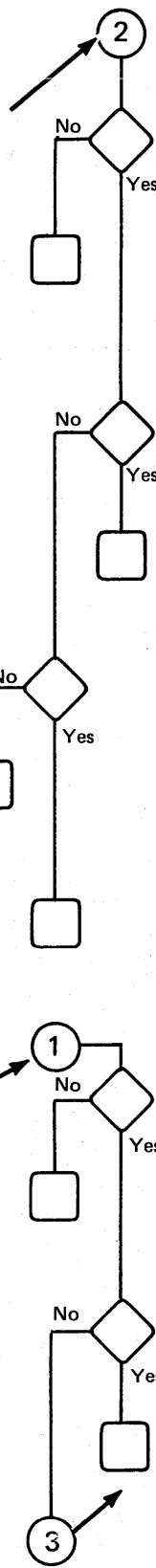
Is PPB-K2 picked?

- Check the PPB-K2 coil.
- Check circuit.
- See note 1 if applicable.
- See note 2.

Is PPB-K1 picked in the failing frame (YZ052)?

Is +24 Vdc present at 01E-JXC?

- Check the PPB-K1 coil.
- Check circuit.
- See note 1 if applicable.
- See note 2.



Is the RPQ S30251 power supply present in the failing frame (D-505)?

- Check PPB-K1-4 in previous frame (PPB-K2-4 if previous frame is basic frame).
- Check circuit.
- See note 1 if applicable.
- See note 2.

Is +24 Vdc present at RPQ-TB3-5 in the failing frame (YZ599)?

- Check the circuit to 01E-EC3.
- See note 1 if applicable.
- See note 2.

Is AC present at RPQ-TB3-2?

- Check RPQ-T1 and RPQ-CP1.
- See note 1 if applicable.
- See note 2.

- Check RPQ-D2 and RPQ-C2.
- See note 1 if applicable.
- See note 2.

Is +24 Vdc present at 01E-JXB?

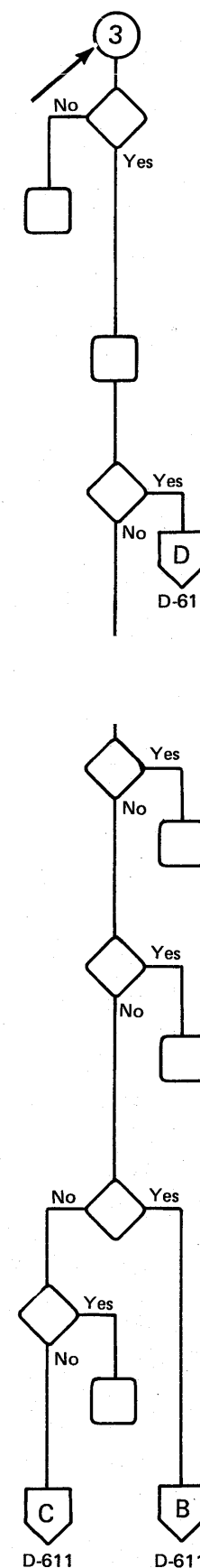
- Check PPB-K1-4 (PPB-K2-4 in basic frame).
- See note 1 if applicable.
- See note 2.

Is +24 Vdc present at 0XD-A1G4G12 (-4 V, -12 V, +12 V sense relay RR1 up, YZ056)?

- Check the cabling from 0XD-A1G4G12 to 01E-PXK.
- See note 1 if applicable.
- See note 2.

Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
2. Reconnect the jumper between pins 0XB-A1V1B11 and 0XB-A1V1B13.



Is +24 Vdc present at 0XD-A1G4G10?

- Check the cabling from 01E-PXJ to 0XD-A1G4G10.
- See note 1 if applicable.
- See note 2.

Is +20 Vdc present at 0XD-A1G4B12 (YZ191)? *+20 V supply can vary from +19 V to +21 V with maximum ripple of 100 mV peak-to-peak.

Is +20 Vdc present at 0XD-A1U2D13? *Check of +20 V regulator (YZ101)

- Check circuit (YZ101, YZ191).
- See note 1 if applicable.
- See note 2.

Is +30 Vdc present at 0XD-A1U2D05?

- Replace the +20 V regulator card at 0XD-A1U2.
- See note 1 if applicable.
- See note 2.

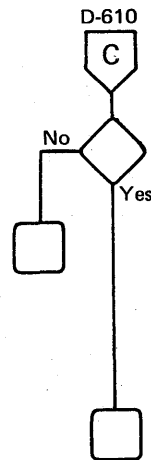
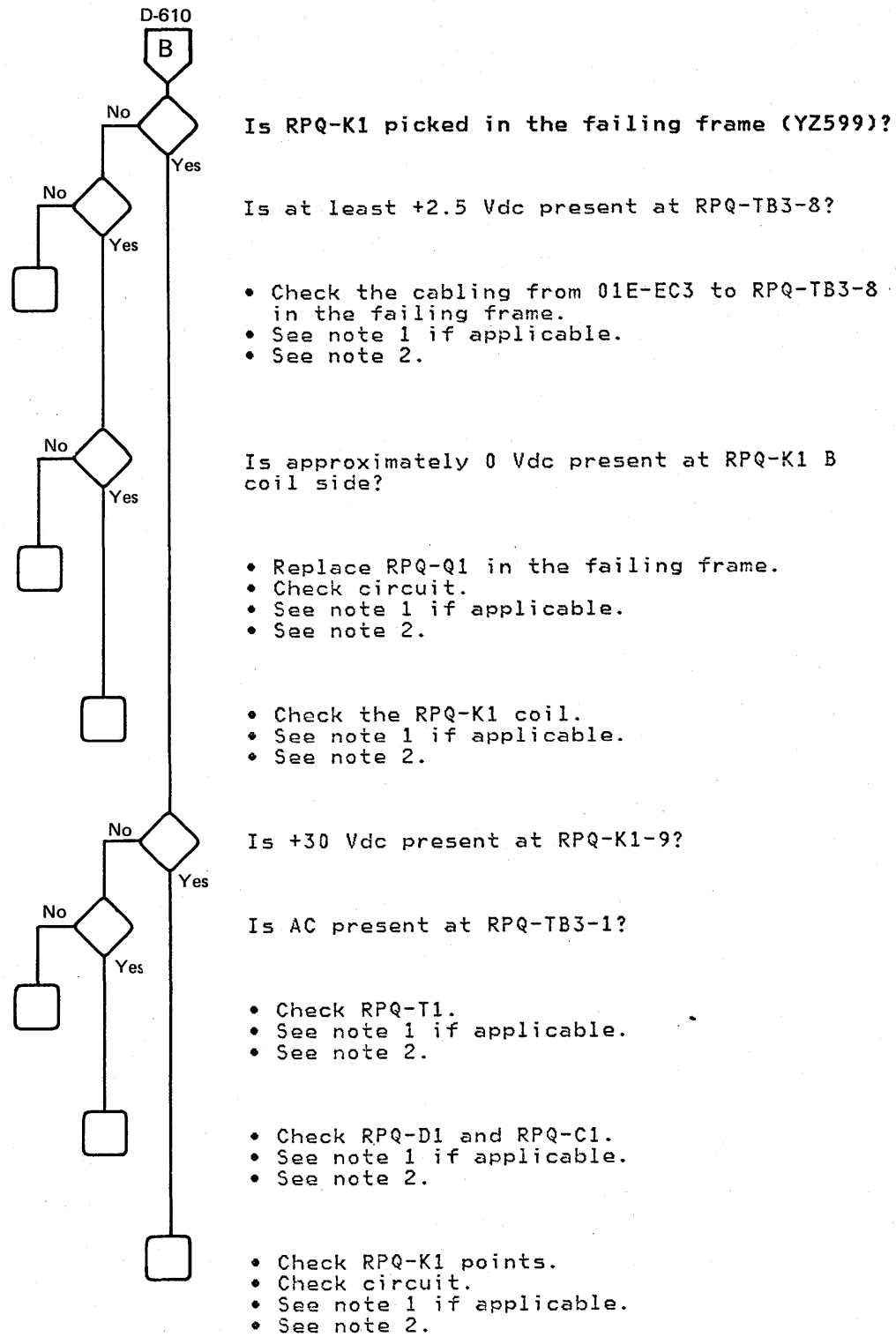
Is the RPQ S30251 power supply present in the failing frame (D-505)?

Is +30 Vdc present at 01E-EC3-e (YZ051)?

- Check the cabling from 01E-EC3 (YZ101, YZ191).
- See note 1 if applicable.
- See note 2.

3705-II POWER-MAINTENANCE ANALYSIS PROCEDURES (MAPs)

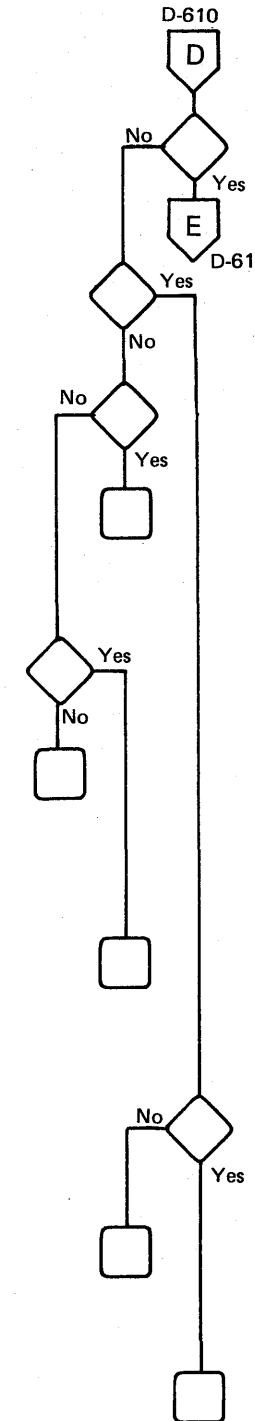
PROBLEM ISOLATION IN A FAILING FRAME WITHOUT MODIFIED POWER SYSTEM (OXD GATE WITH MORE THAN THREE CARDS)-PART 2 OF 7



Is +30 Vdc present at 01E-HD1-3 N/O?

- Replace the SMS card at PPB-T2-J1 in the basic frame.
- Check circuit.
- See note 1 if applicable.
- See note 2.

- Check the 01E-HD1-3 points.
- Check circuit.
- See note 1 if applicable.
- See note 2.



Is -6 Vdc present at 01E-EC3-a (YZ051)?

Is the RPQ S30251 power supply present in the failing frame (D-505)?

Is -24 Vdc present at 01E-C2(-)?

- Check the cabling from 01E-EC3 (YZ051, YZ191).
- See note 1 if applicable.
- See note 2.

Is -24 Vdc present at 01E-C2(-)?

- Replace the SMS card at PPB-T2-J1 in the basic frame.
- Check circuit.
- See note 1 if applicable.
- See note 2.

- Replace the -6 V regulator at 01E-HS1.
- Check circuit.
- See note 1 if applicable.
- See note 2.

Is AC present at RPQ-TB3-3 in the failing frame (YZ599)?

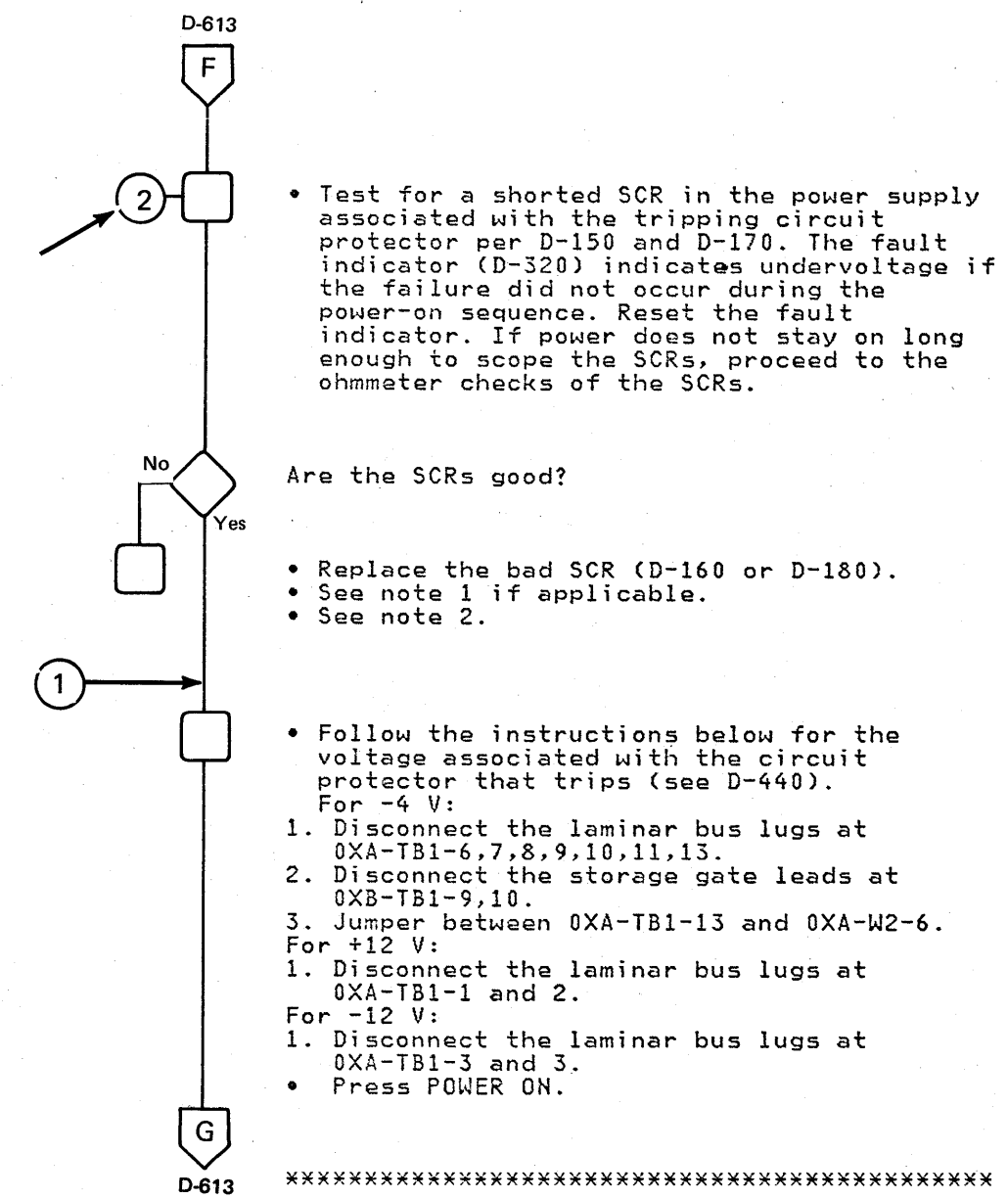
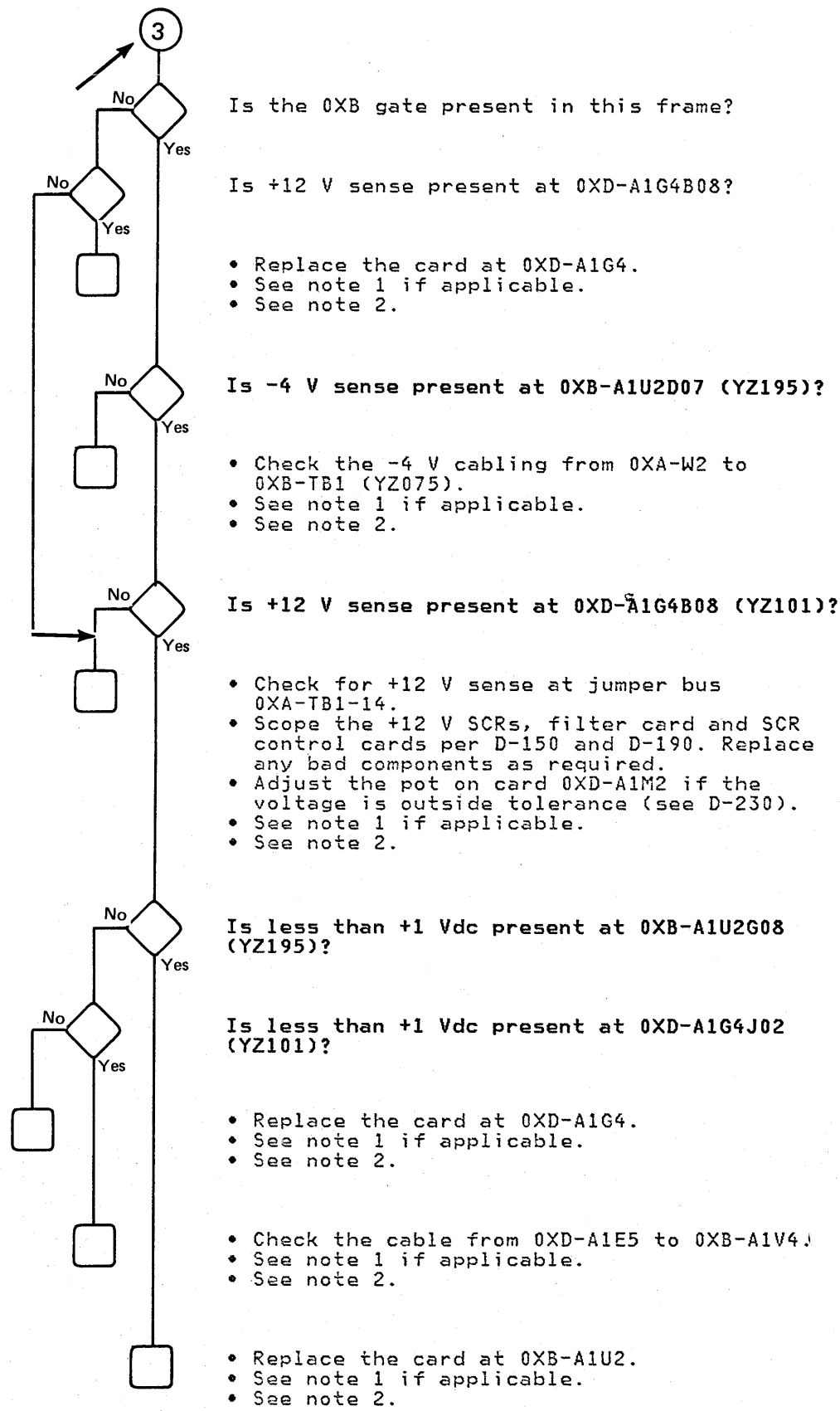
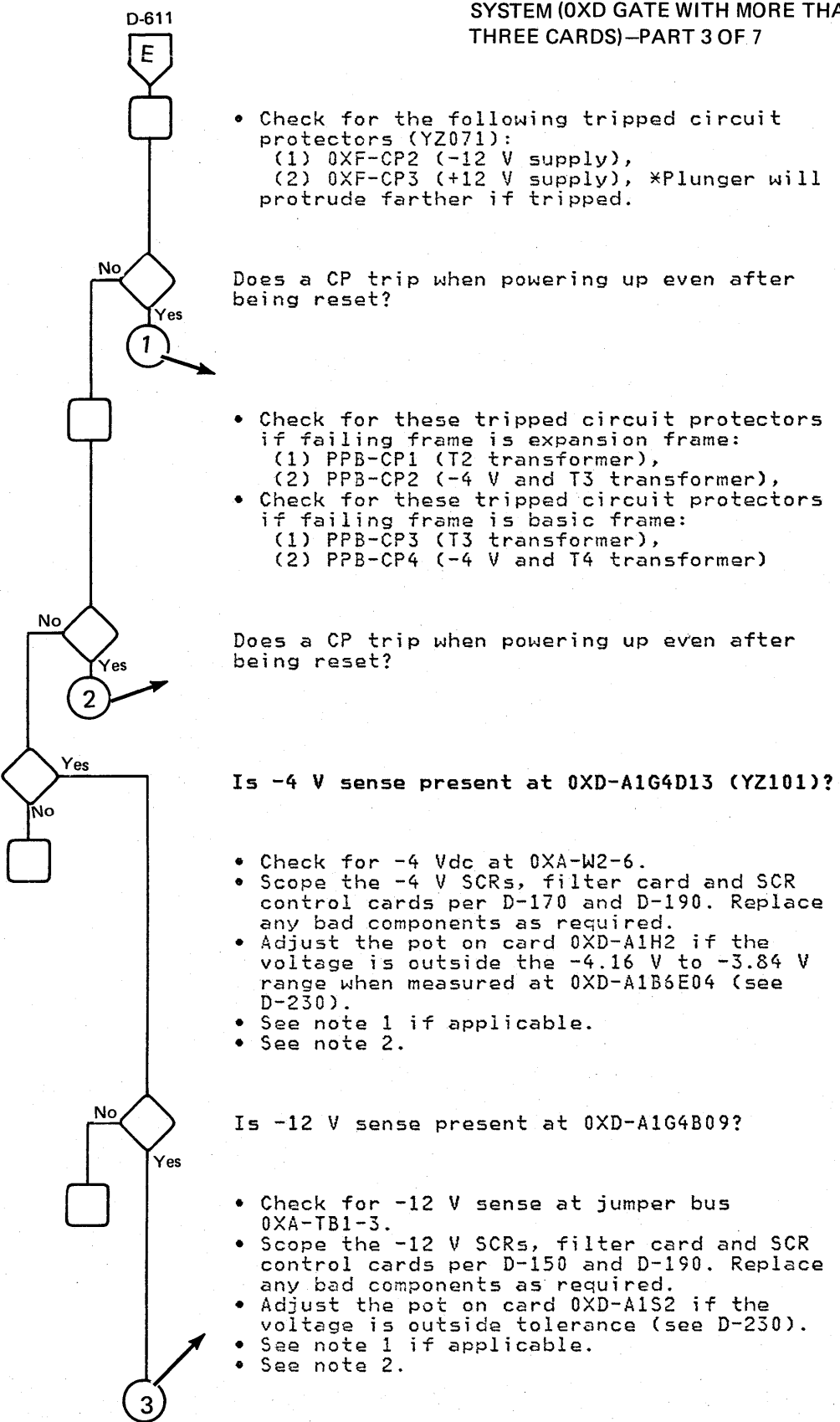
- Check RPQ-T1.
- See note 1 if applicable.
- See note 2.

- Check circuit.
- See note 1 if applicable.
- See note 2.

- Notes:
1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
 2. Reconnect the jumper between pins 0XB-A1V1B11 and 0XB-A1V1B13.

**3705-II POWER—MAINTENANCE
ANALYSIS PROCEDURES (MAPs)**

**PROBLEM ISOLATION IN A FAILING
FRAME WITHOUT MODIFIED POWER
SYSTEM (OXD GATE WITH MORE THAN
THREE CARDS)—PART 3 OF 7**

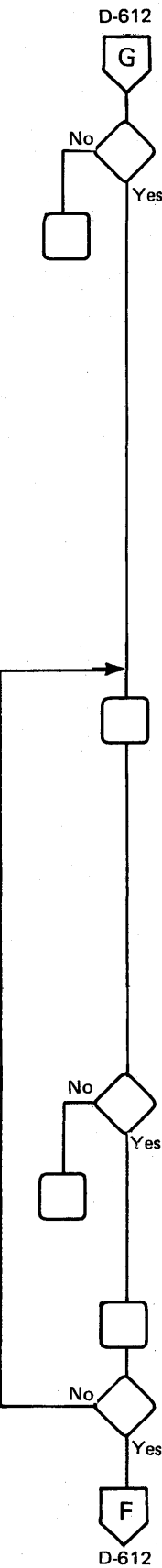


Notes:

- Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
- Reconnect the jumper between pins OXB-A1V1B11 and OXB-A1V1B13.

**3705-II POWER—MAINTENANCE
 ANALYSIS PROCEDURES (MAPs)**

**PROBLEM ISOLATION IN A FAILING
 FRAME WITHOUT MODIFIED POWER
 SYSTEM (OXD GATE WITH MORE THAN
 THREE CARDS)—PART 4 OF 7**



Does the CP trip again?

- Determine which lead causes the circuit protector to trip by powering up after replacing the laminar bus lugs and storage gate leads one at a time.

Caution: Isolate the short to a logic board by removing the laminar bus or storage voltage jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.

- Isolate to a card by removing cards.
- See note 1 if applicable.
- See note 2.

*Test for shorted filter capacitor.
 • Press POWER OFF.

DANGER
 Measure the voltage across the capacitor (to ensure it has discharged) before touching any leads.

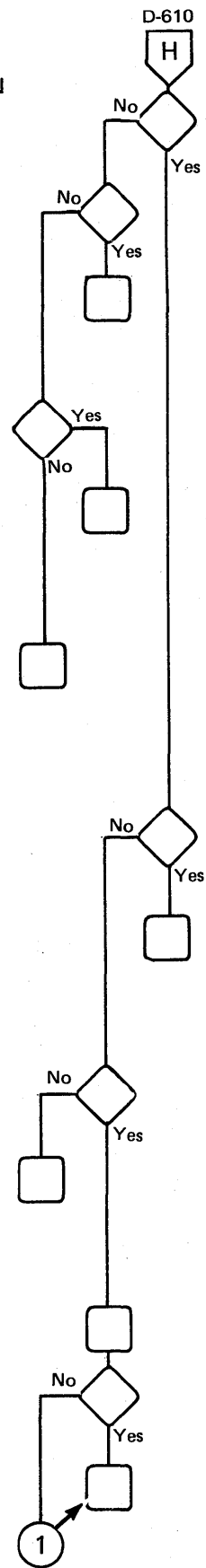
- Remove one capacitor terminal lead at a time. The jumper to the next capacitor must be connected to the removed lead by a screw and nut, or control of the power supply will not be established once the shorted capacitor is removed from the circuit.
- Press POWER ON.

Does the CP trip again?

- Replace the shorted capacitor.
- See note 1 if applicable.
- See note 2.

- Reconnect the lead to the capacitor.

Have all capacitors for this voltage been checked?



Is OXF-HD1 picked in the failing frame (applies +6 V to logic, YZ055)?

Is +24 Vdc present at 01E-JXN?

- Check the OXF-HD1 coil.
- See note 1 if applicable.
- See note 2.

Is +24 Vdc present at 01E-RY1-4 N/O?

- Check 01E-RY1-4 N/O.
- Check circuit.
- See note 1 if applicable.
- See note 2.

- Replace the card at 01E-P8 (location of diode).
- Check circuit.
- See note 1 if applicable.
- See note 2.

Is +24 Vdc present at 0XD-A1G4G09 (+6 V sense relay RR3 up, YZ056)?

- Check the cabling from 0XD-A1G4G09 to 01E-PXH.
- See note 1 if applicable.
- See note 2.

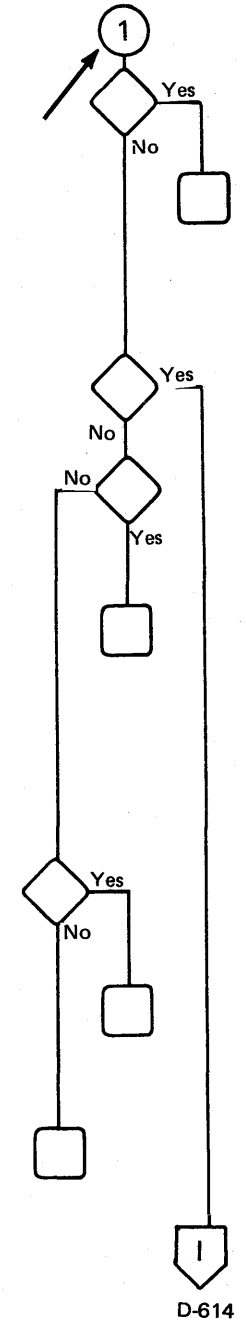
Is +24 Vdc present at 0XD-A1G4G08?

- Check the cabling from 01E-PXG to 0XD-A1G4G08.
- See note 1 if applicable.
- See note 2.

- Check OXF-CP4 (YZ071).

Is +6 V present at 0XD-A1G4B03 (YZ101)?

- Replace the card at 0XD-A1G4.
- See note 1 if applicable.
- See note 2.



Is +6 V present at 0XF-HD1-1,2 op (YZ071)?

- Check the 0XF-HD1-1,2 points (YZ071).
- Check the circuit to gate 0XD (YZ075 or YZ077).
- See note 1 if applicable.
- See note 2.

Is the 0XB gate present in this frame?

Is approximately +1 Vdc present at 0XD-A1M4B13 (ground for +6 V sequence, YZ151)?

- Scope the +6 V SCRs, filter cards, and SCR control cards per D-150 and D-190. Replace bad components as required.
- Adjust the pot on card 0XD-A1M4 if the voltage is outside of the +5.76 V to +6.24 V range. Measure at 0XD-A1B6A04. See D-230.
- See note 1 if applicable.
- See note 2.

Is approximately +1 Vdc present at 0XD-A1G4G05?

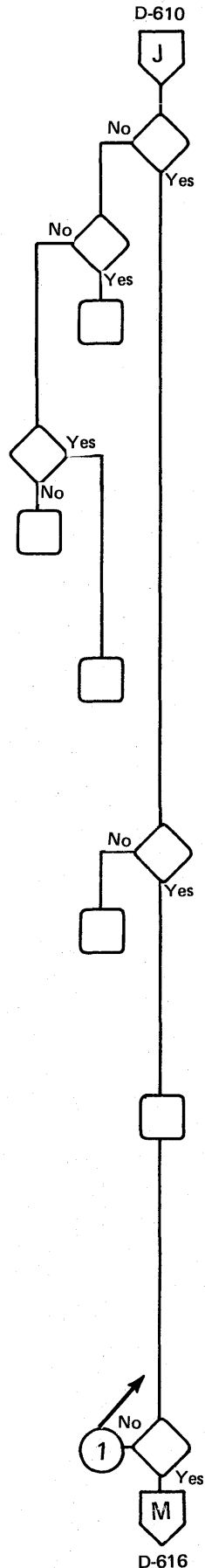
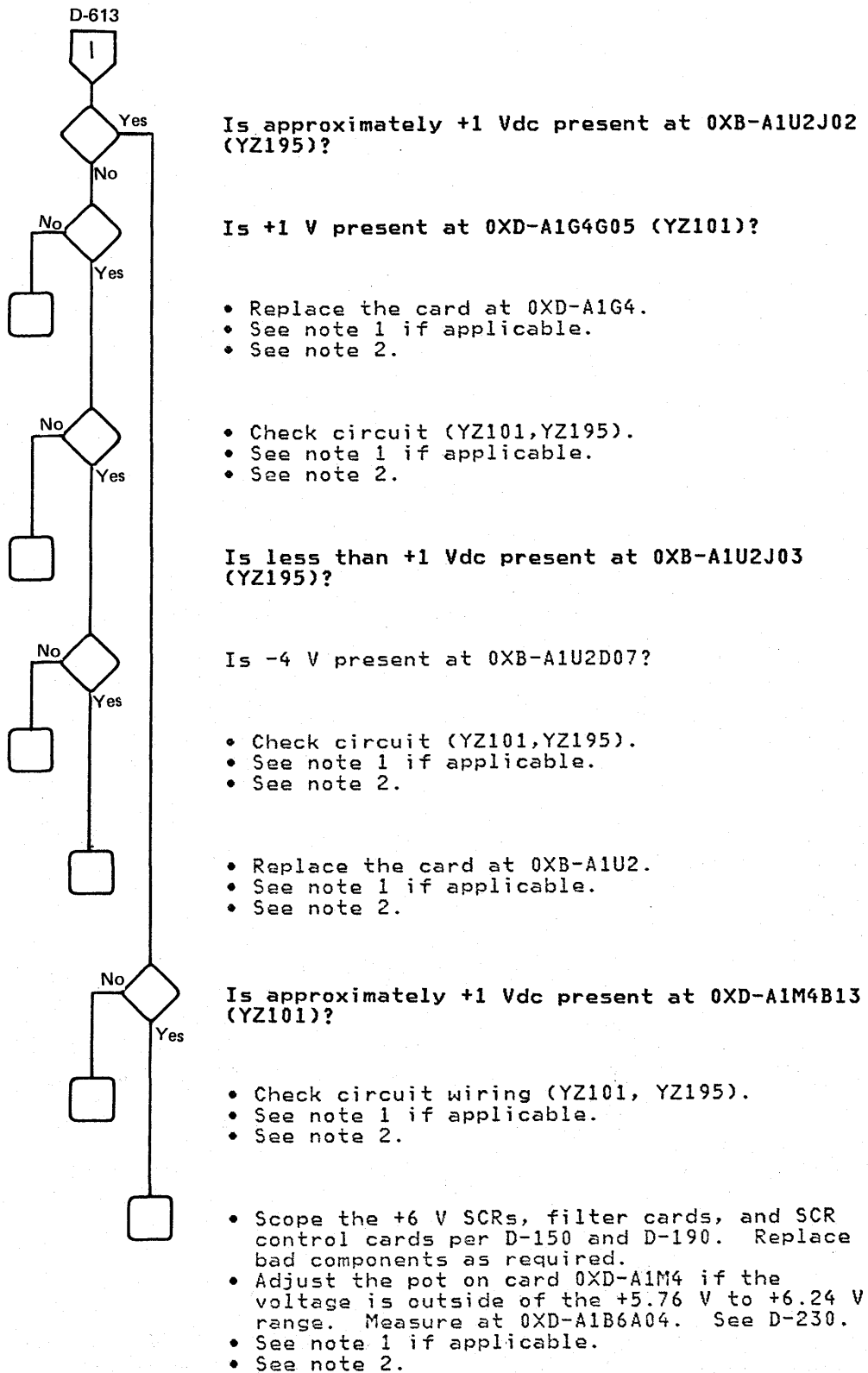
- Replace the card at 0XD-A1G4.
- See note 1 if applicable.
- See note 2.

- Check circuit (YZ101).
- See note 1 if applicable.
- See note 2.

- Notes:
1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
 2. Reconnect the jumper between pins 0XB-A1V1B11 and 0XB-A1V1B13.

**3705-II POWER—MAINTENANCE
ANALYSIS PROCEDURES (MAPs)**

**PROBLEM ISOLATION IN A FAILING
FRAME WITHOUT MODIFIED POWER
SYSTEM (0XD GATE WITH MORE THAN
THREE CARDS)—PART 5 OF 7**



Is 0XF-HD2 picked in the failing frame (applies +12 V to logic, YZ055)?

Is +24 Vdc present at 01E-JXP?

- Check the 0XF-HD2 coil.
- See note 1 if applicable.
- See note 2.

Is +24 Vdc present at 01E-RY2-3 N/O?

- Check 01E-RY2-3 points.
- Check circuit.
- See note 1 if applicable.
- See note 2.

- Replace the card at 01E-P8 (location of diode).
- Check circuit.
- See note 1 if applicable.
- See note 2.

Is the 0XB gate present in this frame?

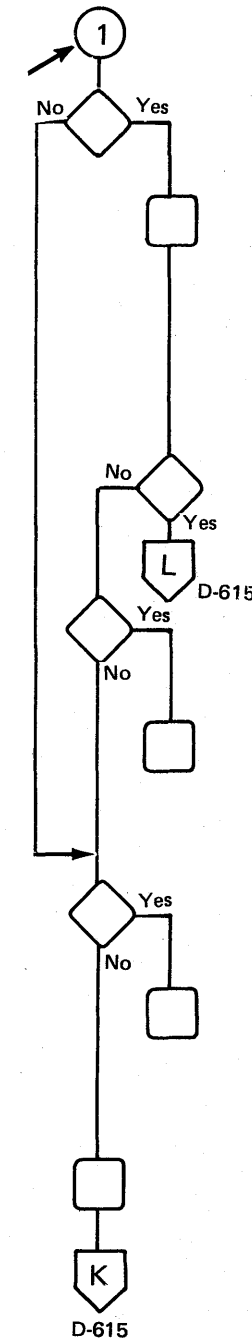
- Check the -30 V supply if present in this expansion frame.
- Check the connections at 01E-JXL and 01E-JXM.
- See note 1 if applicable.
- See note 2.

- Press POWER OFF.

CAUTION
Remove the FET array cards. Possible locations at 0XB-A1 are J2/J4, K2/K4, L2/L4, M2/M4, N2/N4, P2/P4, Q2/Q4, and R2/R4. Keep them in order so that each may be installed in its original location.

- Place grounded jumpers at 0XB-A1U2G04 and at 0XB-A1U2D13 (turns on +3.4 V, YZ195).
- Press POWER ON.

Is +3.4 Vdc present at 0XB-TB2-1 (YZ075, sheet 1)?



Is 0XH-CP1 tripped (YZ075, sheet 2)?

- Press POWER OFF.
*You must wait at least ten seconds between each power-down-to-power-up operation to allow for "bleeding" the unloaded +3.4 V or +8.5 V capacitors. Power will not come up otherwise.
- Reset 0XH-CP1.
- Press POWER ON.

Does 0XH-CP1 trip again?

Is +3.4 Vdc present at 0XH-TB1-5?

- See note 1 if applicable.
- See notes 2, 3 and 4.
- Power on and monitor 0XH-CP1. Suspect a bad 0XH-CP1 or an overload from the FET array cards.

Is approximately +7 Vdc present at 0XH-TB1-5?

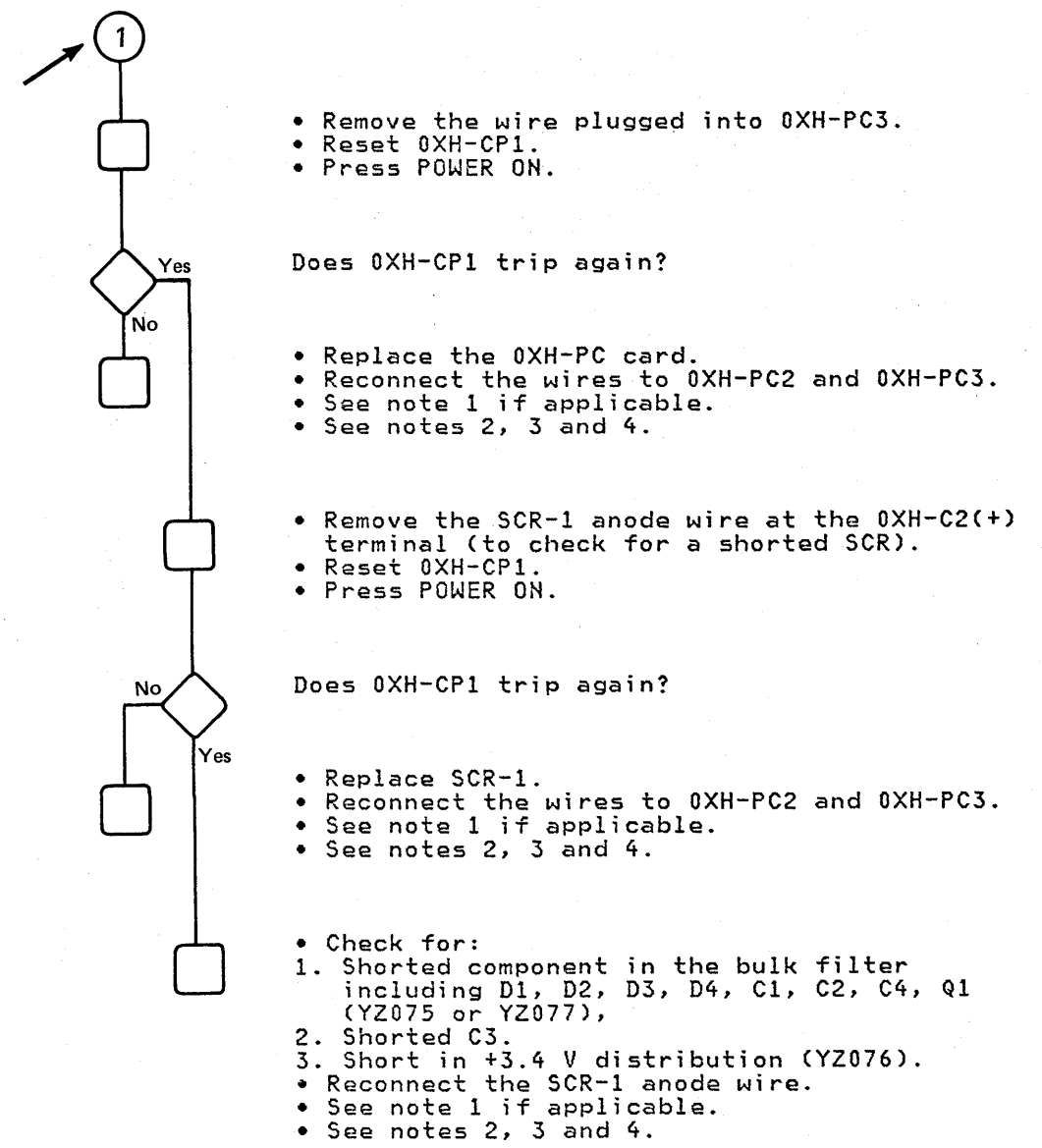
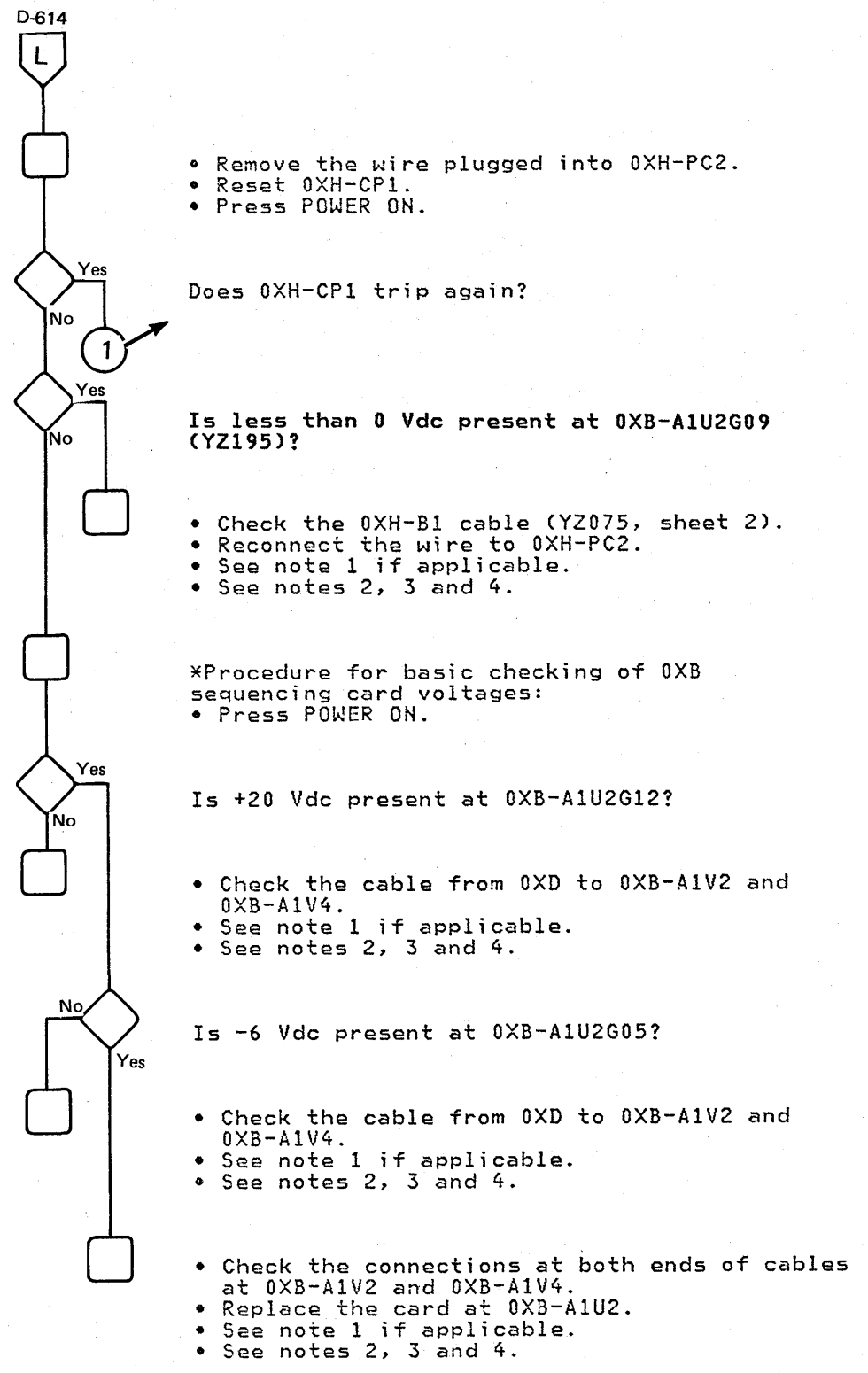
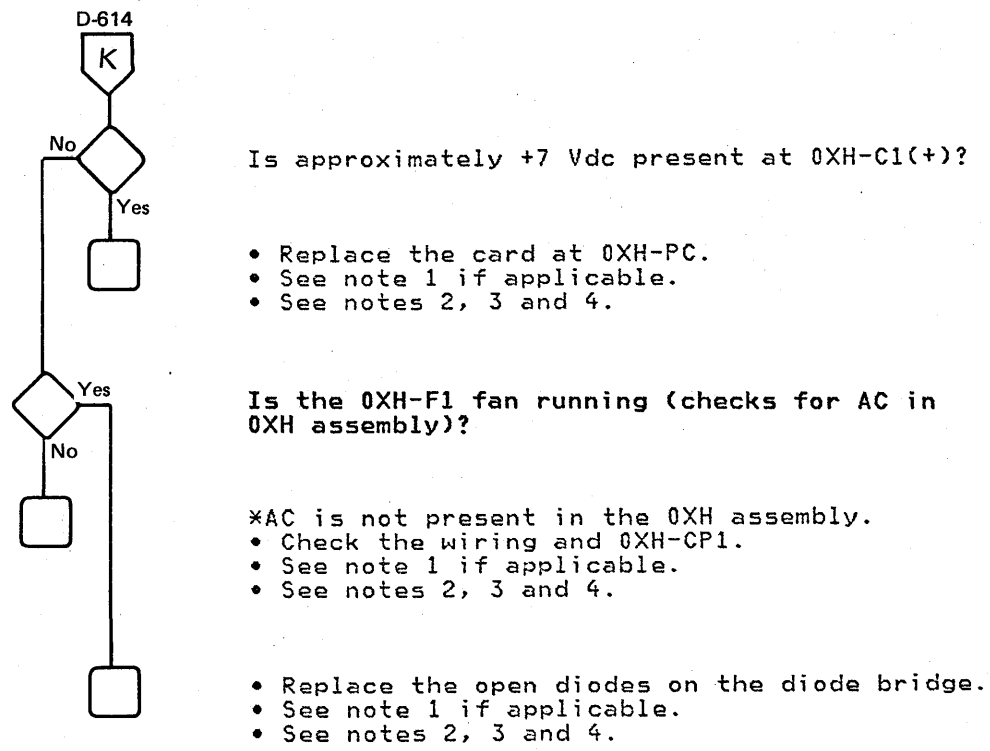
- Check for a shorted transistor at Q1, Q2, Q3 or Q4.
- See note 1 if applicable.
- See notes 2, 3 and 4.

- Check 0XH-B1 connector.

- Notes:**
1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
 2. Reconnect the jumper between pins 0XB-A1V1B11 and 0XB-A1V1B13.

3705-II POWER-MAINTENANCE ANALYSIS PROCEDURES (MAPs)

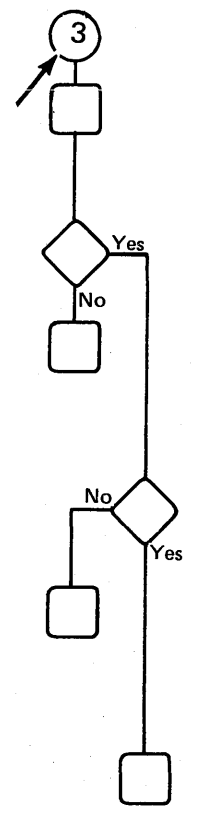
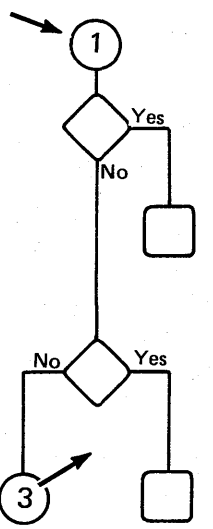
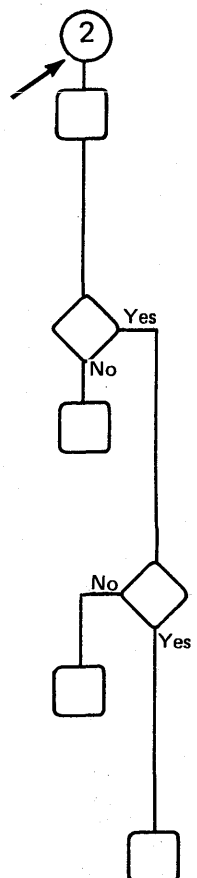
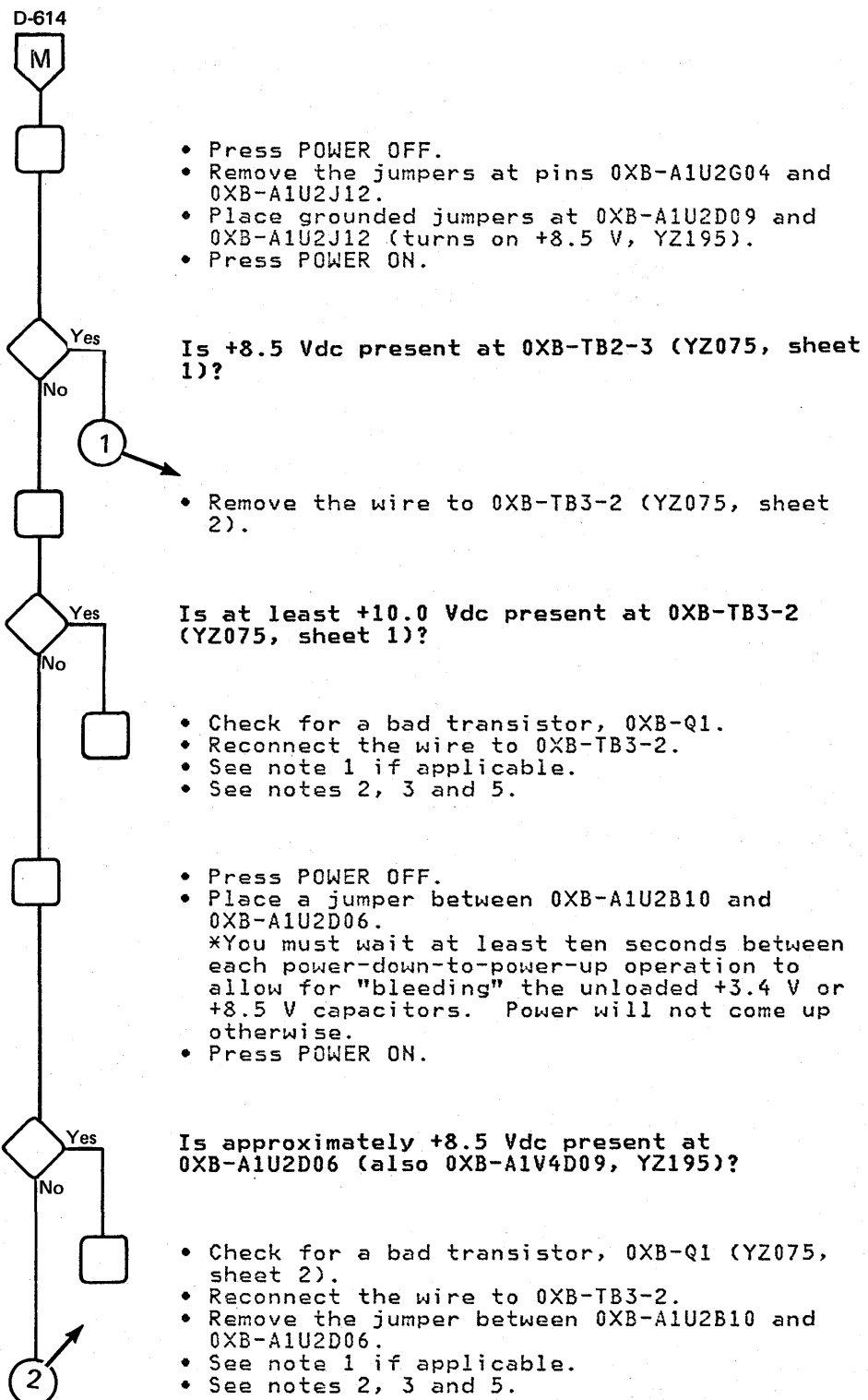
PROBLEM ISOLATION IN A FAILING FRAME WITHOUT MODIFIED POWER SYSTEM (OXD GATE WITH MORE THAN THREE CARDS)-PART 6 OF 7



 Notes:
 1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
 2. Reconnect the jumper between pins 0XB-A1V1B11 and 0XB-A1V1B13.
 3. Reinstall the removed FET array cards in their original locations.
 4. Remove the jumpers at pins 0XB-A1U2G04 and 0XB-A1U2D13.

**3705-II POWER—MAINTENANCE
ANALYSIS PROCEDURES (MAPs)**

**PROBLEM ISOLATION IN A FAILING
FRAME WITHOUT MODIFIED POWER
SYSTEM (0XD GATE WITH MORE THAN
THREE CARDS)—PART 7 OF 7**



- Reconnect the wire to 0XB-TB3-2.
- Remove the jumper between 0XB-A1U2B10 and 0XB-A1U2D06.
- *Procedure for basic checking of 0XB sequencing card voltages.
- Press POWER ON.

Is +20 Vdc present at 0XB-A1U2G12 (YZ191)?

- Check the cable from 0XD to 0XB-A1V2 and 0XB-A1V4.
- See note 1 if applicable.
- See notes 2, 3 and 5.

Is -6 Vdc present at 0XB-A1U2G05?

- Check the cable from 0XD to 0XB-A1V2 and 0XB-A1V4.
- See note 1 if applicable.
- See notes 2, 3 and 5.

- Check the connections at both ends of cables at 0XB-A1V2 and 0XB-A1V4.
- Replace the card at 0XB-A1U2.
- See note 1 if applicable.
- See notes 2, 3 and 5.

Is +24 Vdc present at 01E-JXM (YZ056)?

- Replace the sequence card at 0XB-A1U2.
- See note 1 if applicable.
- See notes 2, 3 and 5.

Is less than +1 Vdc present at 0XB-A1U2J05 (YZ195)?

- Replace the card at 0XD-A1G4.
- Check the cabling to 01E-JXM (YZ056).
- See note 1 if applicable.
- See notes 2, 3 and 5.

*Procedure for basic checking of 0XB sequencing card voltages.
• Press POWER ON.

Is +20 Vdc present at 0XB-A1U2G12 (YZ191)?

- Check the cable from 0XD to 0XB-A1V2 and 0XB-A1V4.
- See note 1 if applicable.
- See notes 2, 3 and 5.

Is -6 Vdc present at 0XB-A1U2G05?

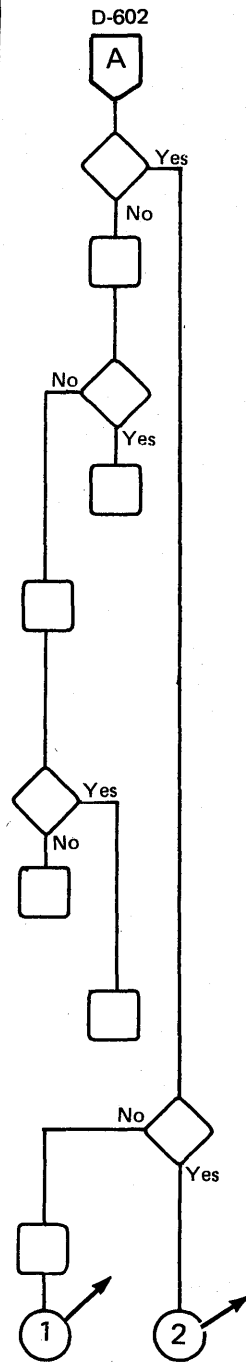
- Check the cable from 0XD to 0XB-A1V2 and 0XB-A1V4.
- See note 1 if applicable.
- See notes 2, 3 and 5.

- Check the connections at both ends of cables at 0XB-A1V2 and 0XB-A1V4.
- Replace the card at 0XB-A1U2.
- See note 1 if applicable.
- See notes 2, 3 and 5.

- Notes:
1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
 2. Reconnect the jumper between pins 0XB-A1V1B11 and 0XB-A1V1B13.
 3. Reinstall the removed FET array cards in their original locations.
 4. Remove the jumpers at pins 0XB-A1U2G04 and 0XB-A1U2D13.
 5. Remove the jumpers at pins 0XB-A1U2D09 and 0XB-A1U2J12.

3705-II POWER-MAINTENANCE ANALYSIS PROCEDURES (MAPs)

PROBLEM ISOLATION IN A FAILING BASIC FRAME WITH MODIFIED POWER SYSTEM (01D GATE WITH ONLY THREE CARDS)-PART 1 OF 5



Is +24 Vdc present at 01D-TB1-6 (YZ524)?

- If more than 2.4 V ripple is present at 01D-TB1-6, replace the capacitor PPB-C1.

Is +24 Vdc present at 01D-TB1-8?

- Replace the diode between 01D-TB1-6 and 01D-TB1-8.

- Use an ac meter to measure the PPB-T2 output voltages. Expected voltage is approximately 20 Vac rms between: PPB-T2-TB5-1 and PPB-T2-TB5-6, PPB-T2-TB5-2 and PPB-T2-TB5-6

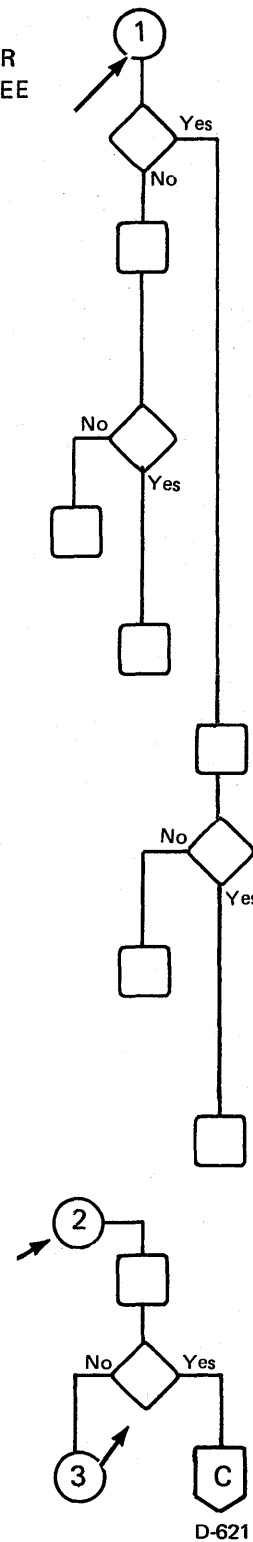
Are these voltages within the specified range?

- Check PPB-CP2, PPB-CB2, PPB-CB1 and the input voltage (YZ502 and YZ518).
- Check primary of PPB-T2.

- Check the diodes at PPB-T2-TB5-1 and at PPB-T2-TB5-2.

Is +5 Vdc Standby present at 01D-A1C1P03 (YZ559)?

- If more than 200 mV ripple is present at 01D-A1C1P03, replace the capacitor 01D-C2 (YZ524).



Is approximately +12 Vdc present at 01D-TB1-2 (YZ524)?

- Use an ac meter to measure the PPB-T2 output voltages. Expected voltage from 11 to 27 Vac rms between: 01D-TB1-1 and 01D-Gnd TB, 01D-TB1-3 and 01D-Gnd TB

Are these voltages within the specified range?

- Check the PPB-T2 transformer and cabling to 01D-TB1.

- Check the diodes at 01D-TB1-2.

- Remove the cards at 01D-A1C1 and 01D-A1E1.

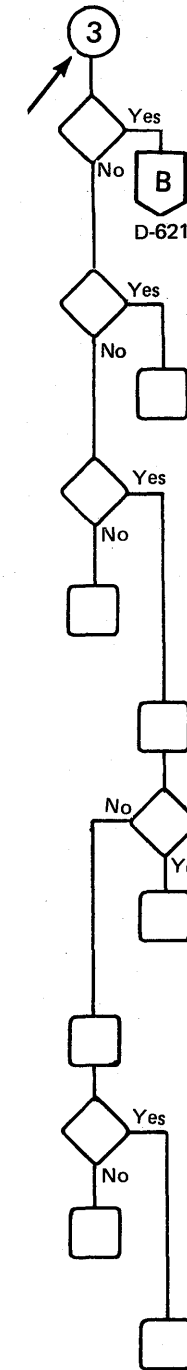
Is +5 Vdc Standby present at 01D-A1C1P03 now (YZ559)?

- Replace the +5 V Standby regulator at 01D-Q3 (YZ524).
- Reinstall the cards at 01D-A1C1 and 01D-A1E1.

- One of these two cards is shorting the +5 V standby supply.
- Replace the defective card.

- Press POWER ON.

Does PPB-K2 pick (even if only momentarily) (YZ522)?



Is PPB-K1 picked?

Is 01D-RY2 picked (EPO relay)?

- Check the 01D-RY2-3 points.

Is the EPO cable plugged in the appropriate connector?

- Plug the EPO cable into the appropriate connector.

- Temporarily jumper EPO-JX pins 1 to 2.

Does 01D-RY2 pick?

- Remove the EPO-JX jumper.
- Check the EPO cable and associated CPU.

- Remove the EPO-JX jumper.

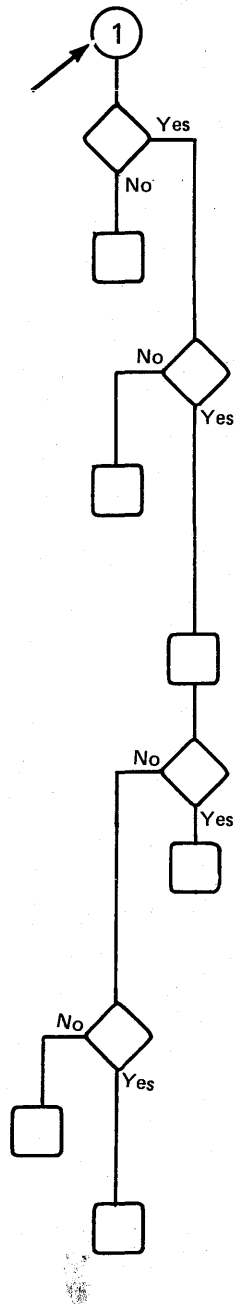
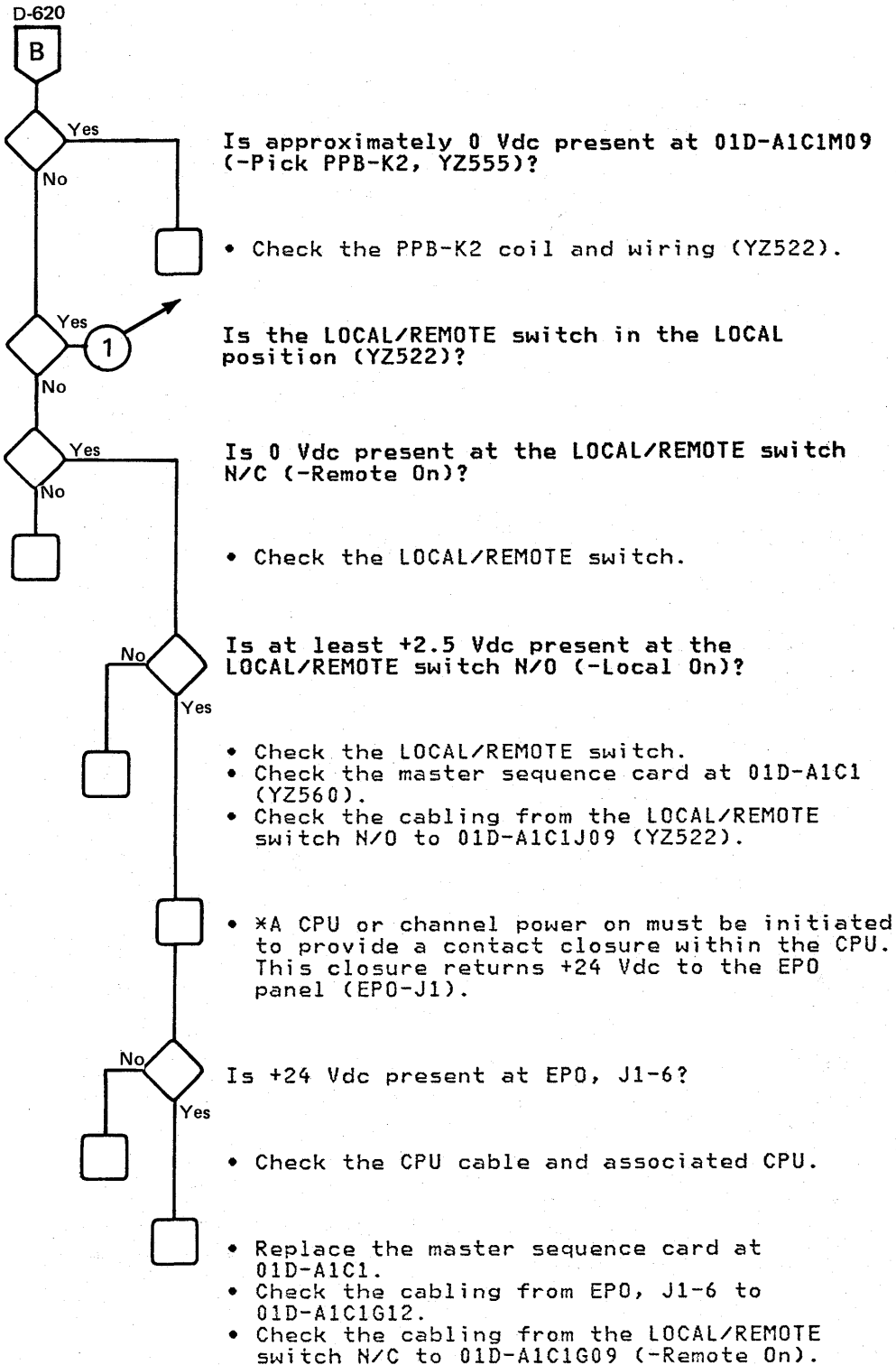
Is +24 Vdc present at EPO-JX pin 1?

- Check the cabling from 01D-TB1-8 to EPO-JX-1.

- Check the 01D-RY2 coil.

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

PROBLEM ISOLATION IN A FAILING BASIC FRAME WITH MODIFIED POWER SYSTEM (01D GATE WITH ONLY THREE CARDS)—PART 2 OF 5



Is 0 Vdc present at the LOCAL/REMOTE switch N/O (-Local On)?

- Check the LOCAL/REMOTE switch.

Is at least +2.5 Vdc present at the LOCAL/REMOTE switch N/C (-Remote On)?

- Check the LOCAL/REMOTE switch.
- Check the master sequence card at 01D-A1C1 (YZ560).
- Check the cabling from the LOCAL/REMOTE switch N/C to 01D-A1C1G09 (YZ522).

Meter 01D-A1C1P02 while pressing the POWER ON switch (YZ554).

Is +24 Vdc present at 01D-A1C1P02?

- Replace the master sequence card at 01D-A1C1.
- Check the cabling from the LOCAL/REMOTE switch N/O to 01D-A1C1J09 (YZ522).

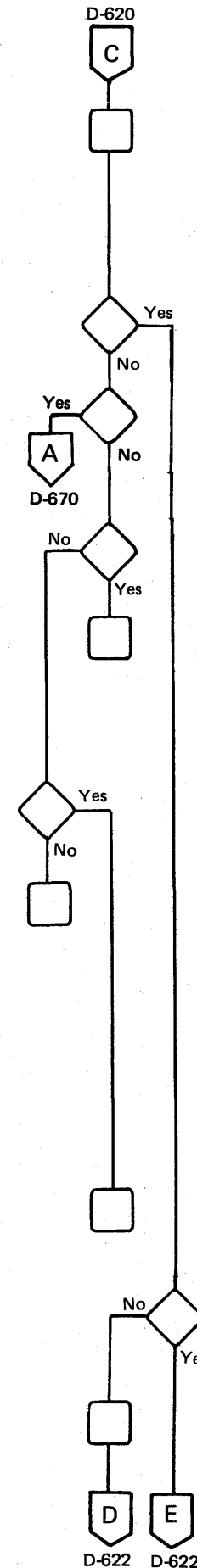
Is +24 Vdc present at 01D-TB1-9 (YZ522, YZ524)?

- Check the 01D-RY2-1 points.

- Check the POWER ON switch and verify that +24 Vdc is present at the switch.
- Check cabling from POWER ON switch to 01D-A1C1J02.

Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
6. Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.



- Press POWER OFF.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12 second time out).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08.
- Press POWER ON.

Does PPB-K2 pick and remain picked?

Is any over voltage LED on at the 01D gate?

Is 0 Vdc present at 01E, J1-F (-Crash, YZ540)?

- Replace the frame sequence card at 01D-A1E1.
- If the problem still exists, replace the master sequence card at 01D-A1C1 instead.
- Check for a short at 01E-JXF.
- See notes 1 and 6.

Is 24 Vdc present at POWER OFF switch, COM (+24 V Pow Off sw, YZ522)?

- Press POWER OFF.
- Check the -24 V standby supply at 01D-C1(-) and replace the capacitor 01D-C1 if more than 2.4 V ripple is present (YZ524).
- Check the +24 V standby supply at PPB-C1(+) and replace the capacitor PPB-C1 if more than 2.4 V ripple is present.
- Replace the master sequence card at 01D-A1C1.
- If the problem still exists, check 01D-C3 instead.
- Check the cabling from the POWER OFF switch, COM to 01D-A1C1G02 (YZ522).
- See notes 1 and 6.

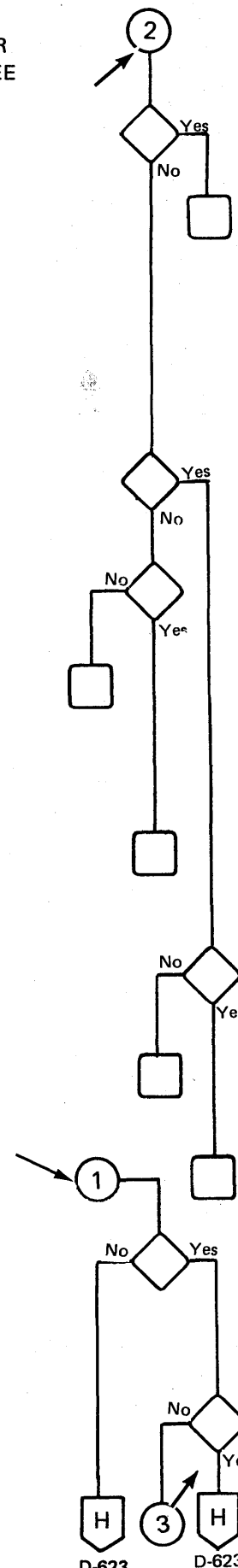
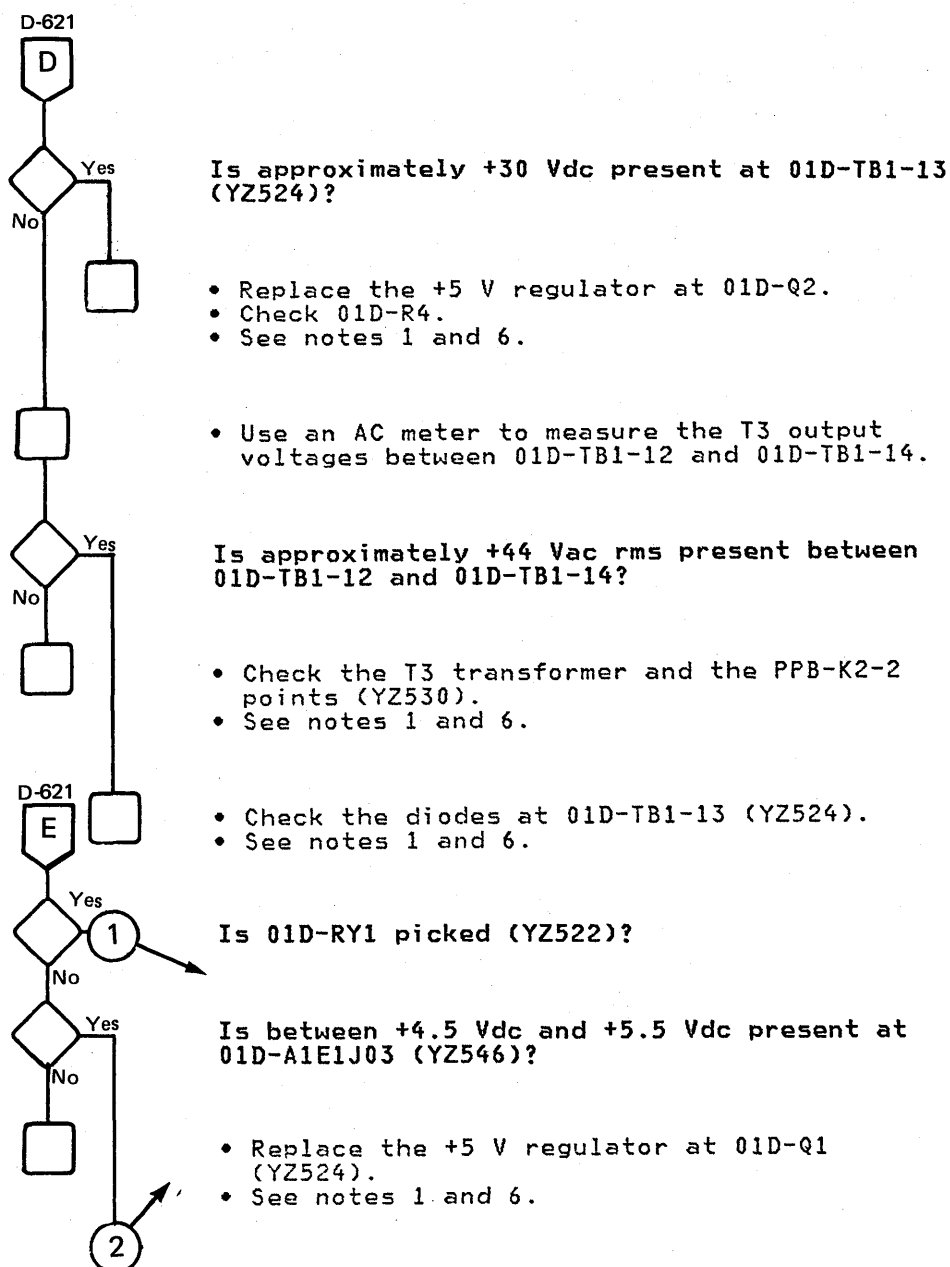
- Check for a shorted POWER OFF switch.
- See notes 1 and 6.

Is between +4.5 Vdc and +5.5 Vdc present at 01D-Q2-3 (YZ524, YZ586, Sheet 5 of 11)?

- If more than 200 mV ripple is present at 01D-Q2-3, replace the capacitor 01D-C3.

**3705-II POWER—MAINTENANCE
 ANALYSIS PROCEDURES (MAPs)**

**PROBLEM ISOLATION IN A FAILING
 BASIC FRAME WITH MODIFIED POWER
 SYSTEM (01D GATE WITH ONLY THREE
 CARDS)—PART 3 OF 5**



Are any of the LEDs on the 01D gate on?

- Check the LEDs on the 01D gate in the order listed below and go to the appropriate page (see D-520):

Any	0/V	--	D-670
-4 V	U/V	--	D-640
+3.4 V	U/V	--	D-645
+8.5 V	U/V	--	D-650
+6 V	U/V	--	D-655
-12 V	U/V	--	D-660
+12 V	U/V	--	D-665

Is at least +2.5 Vdc present at 01E-EC3-e (+Start pwr on seq, YZ540)?

Is at least +2.5 Vdc present at 01D-TB1-7 (YZ524)?

- Replace the master sequence card at 01D-A1C1.
- Check the cabling from 01D-A1C1U05 to 01D-TB1-7.
- See notes 1 and 6.

- Check the cabling from 01D-TB1-7 to 01E-EC3-e.
- See notes 1 and 6.

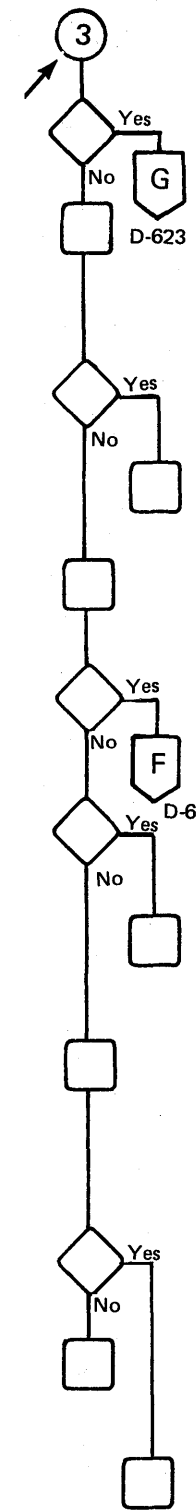
Is 0 Vdc present at 01D-RY1-B (-drive for 0XD-RY1, YZ522)?

- Replace the frame sequence card at 01D-A1E1.
- Check the cabling from 01D-A1E1B02 (YZ551).
- Check the cabling from 01E-EC3-h to 01D-A1E1B13 (YZ540).
- See notes 1 and 6.

- Check the 01D-RY1 coil (YZ522).
- See notes 1 and 6.

Is expansion frame 1 present?

Is +24 Vdc present at 01E-J4C (YZ540)?



Is +24 Vdc present at 01E-J1B?

- Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
- Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

Is +24 Vdc present at 01E-EC3-a?

- Check the PPB-K2-4 points and cabling.
- *The +24 V power supply in expansion frame 1 is faulty.

Is the RPQ S30251 power supply present in expansion frame 1 (D-505)?

Is +24 Vdc present at PPB-T2-TB5-3 in expansion frame 1 (YZ526)?

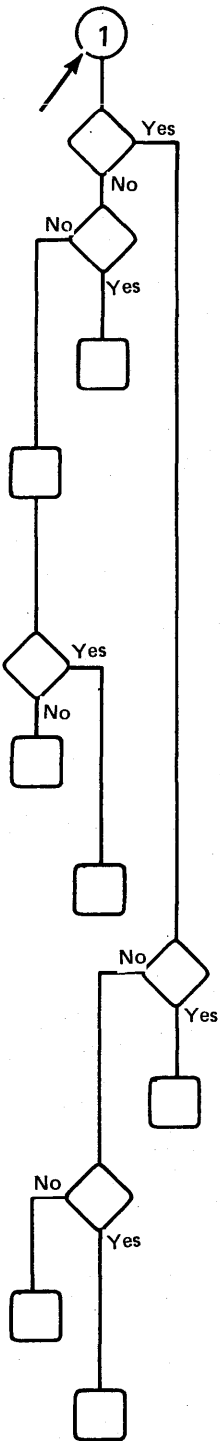
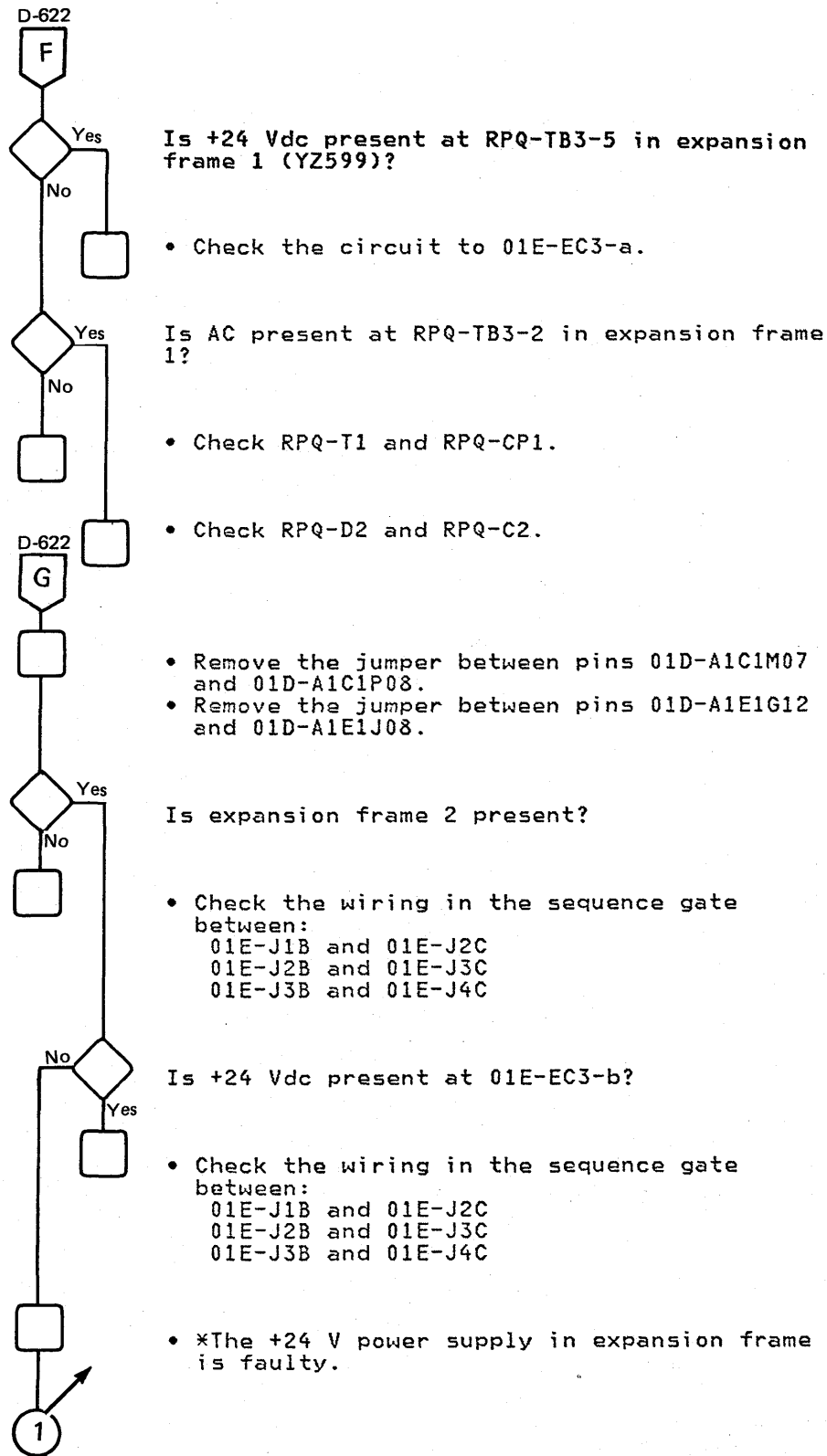
- Check the cabling from PPB-T2-TB5-3 to 02D-TB1-8.
- Use an ac meter to measure the PPB-T2 output voltages in expansion frame 1. Expected voltages from 24.2 to 33.3 Vac rms between: PPB-T2-TB5-1 and PPB-T2-TB5-6, PPB-T2-TB5-2 and PPB-T2-TB5-6

Are the voltages within the specified range?

- Check PPB-CP1, PPB-CB1 and the input voltage in expansion frame 1 (YZ518).
- Check the diode at PPB-T2-TB5-3.

3705-II POWER-MAINTENANCE ANALYSIS PROCEDURES (MAPs)

PROBLEM ISOLATION IN A FAILING BASIC FRAME WITH MODIFIED POWER SYSTEM (01D GATE WITH ONLY THREE CARDS)-PART 4 OF 5



Is the RPQ S30251 power supply present in expansion frame 2 (YZ599, D-505)?

Is +24 Vdc present at PPB-T2-TB5-3 in expansion frame 2 (YZ526)?

- Check the cabling from PPB-T2-TB5-3 to 03D-TB1-8.
- Use an ac meter to measure the PPB-T2 output voltages in expansion frame 2. Expected voltage is 20 Vac rms between: PPB-T2-TB5-1 and PPB-T2-TB5-6, PPB-T2-TB5-2 and PPB-T2-TB5-6

Are the voltages within the specified range?

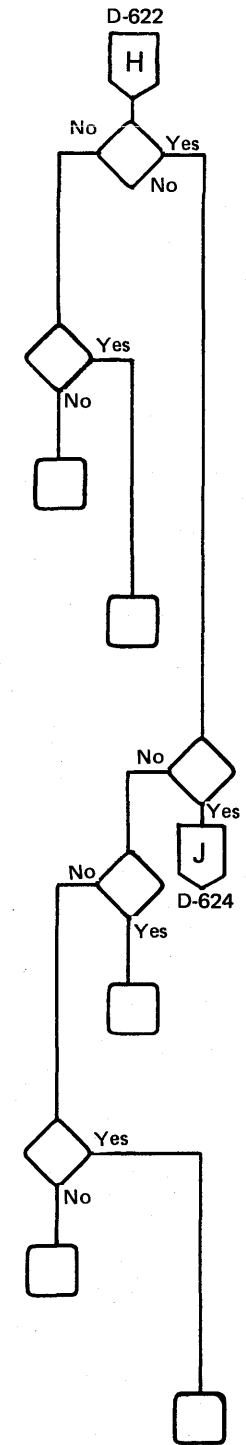
- Check PPB-CP1, PPB-CB1, and the input voltage in expansion frame 2 (YZ518).
- Check the diodes at PPB-T2-TB5-3.

Is +24 Vdc present at RPQ-TB3-5 in expansion frame 2 (YZ599)?

- Check the circuit to 01E-EC3-b.

Is AC present at RPQ-TB3-2 in expansion frame 2?

- Check RPQ-T1 and RPQ-CP1.
- Check RPQ-D2 and RPQ-C2.



Is +24 Vdc present at 01E-J1N (+24 V pick 0XF-HD1, YZ540)?

Is +24 Vdc present at 01E-J1K (+24 V for HD1 driver)?

- Check the cabling from 01E-J4J to 01E-J1K.
- See notes 1 and 6.
- Replace the master sequence card at 01D-A1C1.
- See notes 1 and 6.
- Check the cabling from 01E-J1K to 01E-A1C1J07.
- Check the cabling from 01D-A1C1G07 to 01E-J1N (YZ555).

Is +24 Vdc present at 01E-J1P (+24 V pick 0XF-HD2)?

Is +24 Vdc present at 01D-A1C1M06 (pick 0XF-HD2, YZ555)?

- Check the cabling from 01D-A1C1S02 to 01E-J1P.
- See notes 1 and 6.

Is +24 Vdc present at 01D-A1C1P04 (sequence complete old, YZ556)?

- Check the cabling from 01E-J1H to 01D-A1C1J04.
- See notes 1 and 6.
- Replace the master sequence card at 01D-A1C1.
- See notes 1 and 6.

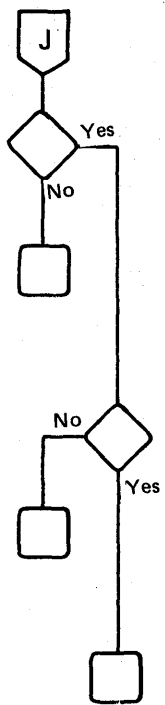
Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
6. Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

PROBLEM ISOLATION IN A FAILING BASIC FRAME WITH MODIFIED POWER SYSTEM (01D GATE WITH ONLY THREE CARDS)—PART 5 OF 5

D-623D



Is +24 Vdc present at 01D-A1C1P05 (sequence complete new, YZ556)?

- Check the 01D-RY1-1 points (YZ522).
- Check the cabling from 01D-RY1-1 to 01D-A1C1G04.
- See notes 1 and 6.

Is approximately 0 Vdc present at POWER ON indicator 1-B (YZ522)?

- Replace the master sequence card at 01D-A1C1.
- Check the cabling from 01D-A1C1S03 to the POWER ON indicator (YZ556).
- See notes 1 and 6.

- Check the POWER ON light.
- See notes 1 and 6.

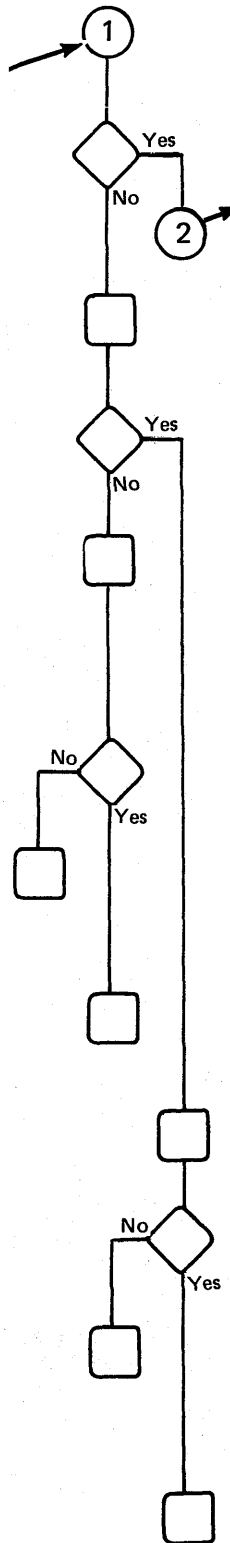
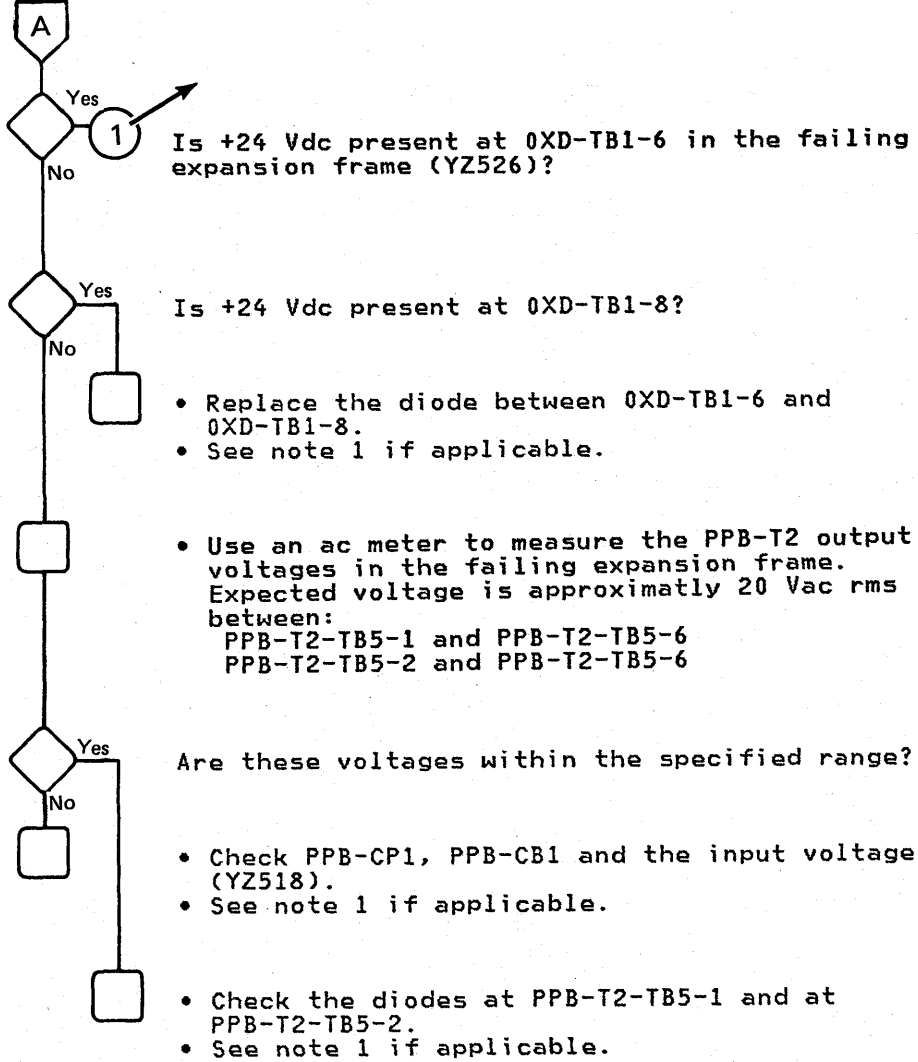
Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
6. Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

3705-II POWER—MAINTENANCE
ANALYSIS PROCEDURES (MAPs)

PROBLEM ISOLATION IN A FAILING
EXPANSION FRAME WITH MODIFIED
POWER SYSTEM (OXD GATE WITH ONLY
TWO CARDS)—PART 1 OF 2

D-601,
D-602



Is +5 Vdc Standby present at OXD-Q3 (YZ526)?

- If more than 200 mV ripple is present at OXD-Q3, replace the capacitor OXD-C2.

Is approximately +12 Vdc present at OXD-TB1-2?

- Use an ac meter to measure the PPB-T2 output voltages in the failing expansion frame. Expected voltage from 10 to 16 Vac rms between:
OXD-TB1-1 and OXD-Gnd TB
OXD-TB1-3 and OXD-Gnd TB

Are these voltages within the specified range?

- Check the PPB-T2 transformer and cabling to OXD-TB1.
- See note 1 if applicable.

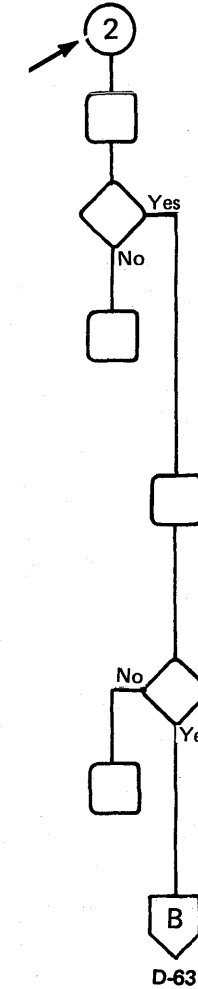
- Check the diodes at OXD-TB1-2.
- See note 1 if applicable.

- Remove the card at OXD-A1E1.

Is +5 Vdc Standby present at OXD-Q3 now (YZ546)?

- Replace the +5 V regulator at OXD-Q3 (YZ526).
- Reinstall the card at OXD-A1E1.
- See note 1 if applicable.

- Replace the defective card at OXD-A1E1.
- See note 1 if applicable.



- Press POWER ON.

Does PPB-K1 pick in the failing expansion frame (even if only momentarily)?

- Check the PPB-K1 coil.
- Check the cabling from 01E-PXC to the PPB-K1 A coil in the failing expansion frame.
- See note 1 if applicable.

- Press POWER OFF.
- Place a jumper between pins OXD-A1E1G12 and OXD-A1E1J08 (disables the 12 second time out).
- Press POWER ON.

Does PPB-K1 pick and remain picked?

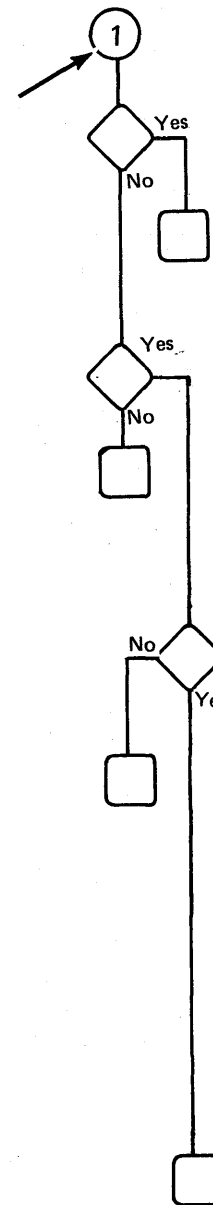
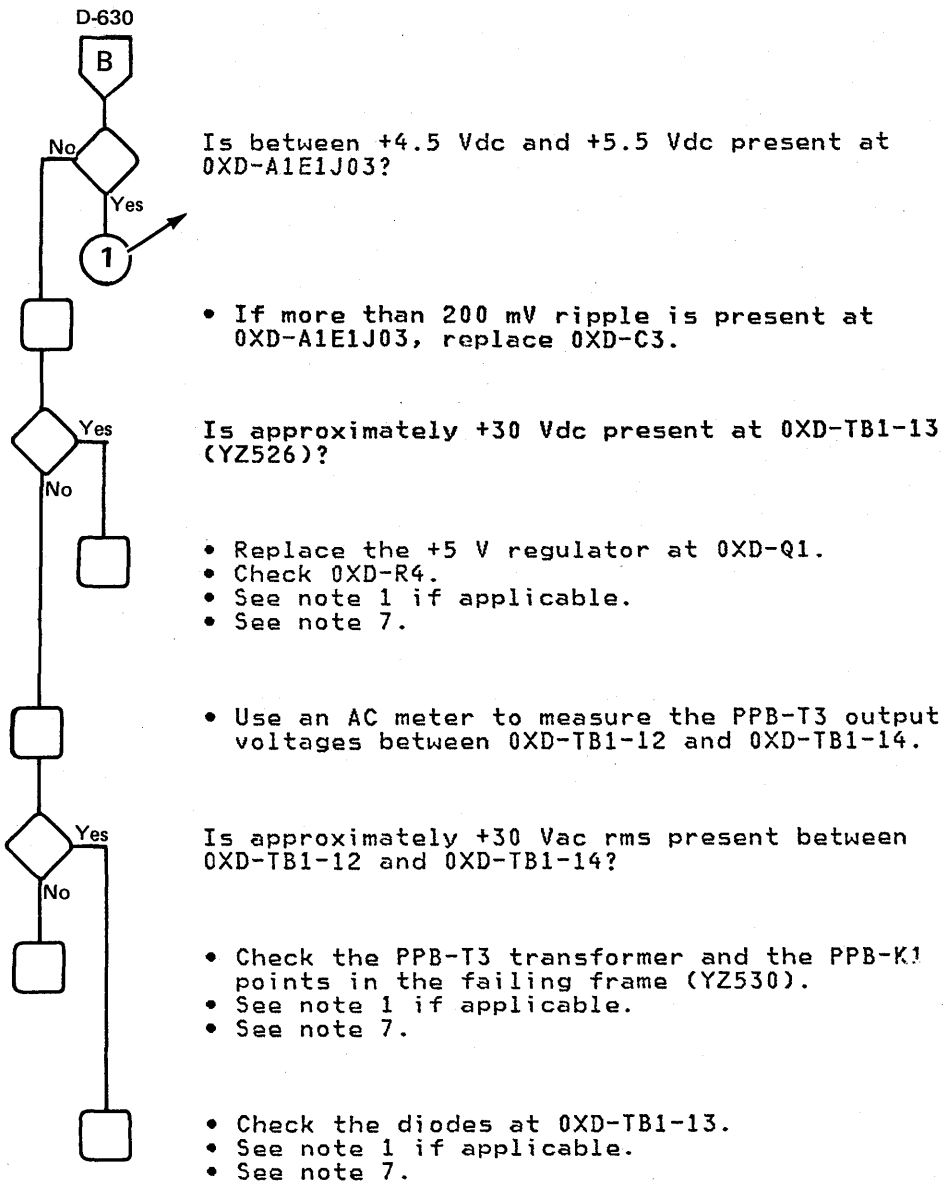
- Check the LEDs on the OXD gate in the failing frame in the order listed and go to the appropriate page (see D-520):
(1) Any 0/V -- D-670
(2) -4 V U/V -- D-640
(3) +3.4 V U/V -- D-645
(4) +8.5 V U/V -- D-650
(5) +6 V U/V -- D-655
(6) -12 V U/V -- D-660
(7) +12 V U/V -- D-665
- If no LEDs are on, check the frame sequence card at OXD-A1E1.

Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
7. Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

PROBLEM ISOLATION IN A FAILING EXPANSION FRAME WITH MODIFIED POWER SYSTEM (OXD GATE WITH ONLY TWO CARDS)—PART 2 OF 2



Is OXD-RY1 picked (YZ568)?

- Check the OXD-RY1-1 N/O points.
- See note 1 if applicable.
- See note 7.

Is at least +2.5 Vdc present at OXD-TB1-7 (+ start pwr on seq, YZ526)?

- Check the cabling from 01E-EC3-f,g,h to OXD-TB1-7.
- See note 1 if applicable.
- See note 7.

Is approximately 0 Vdc present at OXD-RY1-B (YZ568)?

- Check the LEDs on the OXD gate in the failing frame in the order listed below and go to the appropriate page (see D-520):
 - (1) Any 0/V -- D-670
 - (2) -4 V U/V -- D-640
 - (3) +3.4 V U/V -- D-645
 - (4) +8.5 V U/V -- D-650
 - (5) +6 V U/V -- D-655
 - (6) -12 V U/V -- D-660
 - (7) +12 V U/V -- D-665
- If no LEDs are on, check the frame sequence card at OXD-A1E1.

- Check the OXD-RY1 coil.
- See note 1 if applicable.
- See note 7.

Notes:

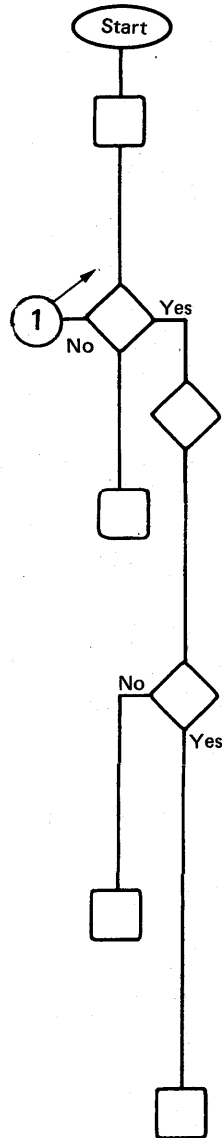
1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
7. Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

-4V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM (OXD GATE WITH ONLY TWO OR THREE CARDS)—PART 1 OF 1

Caution: A shorted SCR can damage a phase control card (OXD-A1A1), also a defective phase control card can damage an SCR (see "Testing the SCR for Shorts" on page D-560).

- Press POWER OFF.
- Place a jumper between pins OXD-A1E1G12 and OXD-A1E1J08 (disables the 12 second time out) if not already present.
- Press POWER ON.



Is 0 Vdc present at OXA-TB1-13 (-4 V sense, YZ536)?

Is -24 Vdc present at OXD-C1(-) (-24 V bulk supply, YZ524 or YZ526)

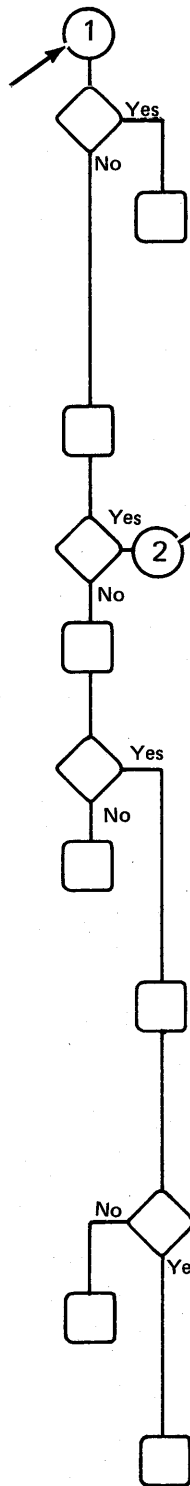
- If more than 2.4 V ripple is present, replace the capacitor OXD-C1.
- Check the diode at PPB-T2-TB5-4.

Is at least +1.0 Vdc present at OXD-A1E1P04 (drive signal for -4 Vdc supply, YZ551, YZ556)?

Caution: Do not short OXD-A1E1P04 to adjacent pins; card damage may occur.

- Replace the frame sequence card at OXD-A1E1.
- If the problem still exists, replace the phase control card at OXD-A1A1 instead (see Caution at top of this column).
- Adjust voltages (D-580).
- See note 1 if applicable. See note 7.

- Replace the phase control card at OXD-A1A1 (see Caution at the top of this column).
- If the problem still exists, check OXF-L1,L2,L3 choke and SCRs instead (YZ586, sheet 6).
- See note 1 if applicable.
- See note 7.



Is -4 Vdc present at OXA-TB1-13?

- Replace the frame sequence card at OXD-A1E1.
- Check the cabling from OXA-TB1-13 to OXD-A1E1M08 (YZ536).
- See note 1 if applicable.
- See note 7.

Scope the -4 V SCRs at OXF-HS1 (YZ530, YZ586, sheet 6).

Are both SCRs firing (see D-560)?

Scope the gate pulses at OXD-A1A1B09 (YZ566).

Are the gate pulses present?

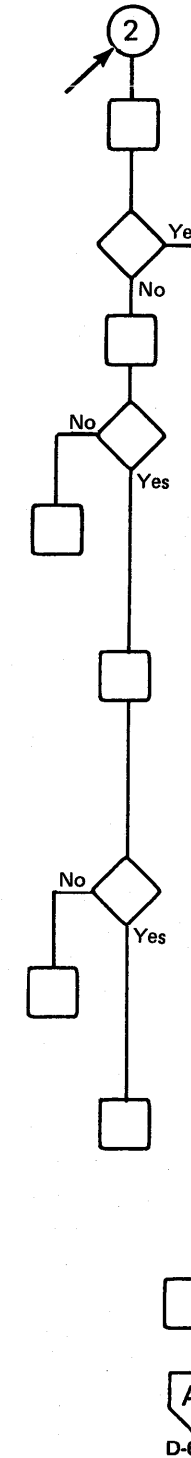
- Replace the phase control card at OXD-A1A1. See Caution at the top of column one.
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

Press POWER OFF. Measure the resistance of the pulse transformer secondary coils between the following pins:
OXD-A1A1G11 and OXD-A1A1J11
OXD-A1A1G13 and OXD-A1A1J13

Is less than 20 ohms present (YZ566)?

- Replace the phase control card at OXD-A1A1 (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Check for ac at the cathode of the failing SCR(s).
- Check the failing SCR(s) and cabling from the phase control card.
- See note 1 if applicable.
- See note 7.



Scope the -4 V SCRs at OXF-HS2 (YZ530, YZ586, sheet 6).

Are both SCRs firing (see D-560)?

Scope the gate pulses at OXD-A1A1B07 (YZ566).

Are the gate pulses present?

- Replace the phase control card at OXD-A1A1.
- See note 1 if applicable.
- See note 7.

Press POWER OFF. Measure the resistance of the pulse transformer secondary coil between the following pins:
OXD-A1A1G06 and OXD-A1A1J06
OXD-A1A1G09 and OXD-A1A1J09

Is less than 20 ohms present (YZ566)?

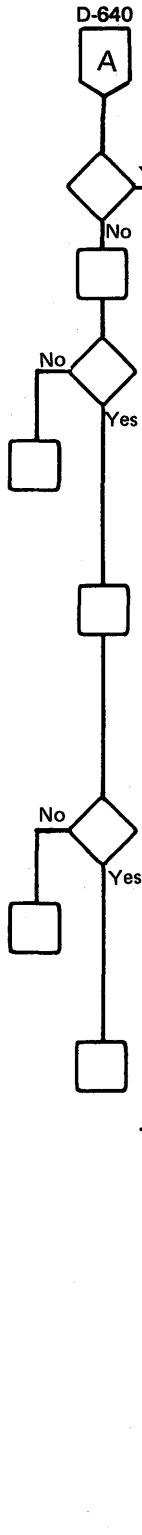
- Replace the phase control card at OXD-A1A1. (see Caution at the top of column one).
- See note 1 if applicable.
- See note 7.
- Check for ac at the cathode of the failing SCR(s).
- Check the failing SCR(s) and cabling from the phase control card.
- See note 1 if applicable.
- See note 7.

Scope the -4 V SCRs at OXF-HS3 (YZ530, YZ586, sheet 6).

- Notes:**
- Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
 - Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

3705-II POWER-MAINTENANCE ANALYSIS PROCEDURES (MAPs)

-4V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM (OXD GATE WITH ONLY TWO OR THREE CARDS)-PART 2 OF 2



Caution: A shorted SCR can damage a phase control card (OXD-A1A1), also a defective phase control card can damage an SCR (see "Testing the SCR for Shorts" on page D-560).

Are both SCRs firing (see D-560)?

- Scope the gate pulses at OXD-A1A1B11 (YZ566).

Are the gate pulses present?

- Replace the phase control card at OXD-A1A1 (see Caution at the top of this column).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

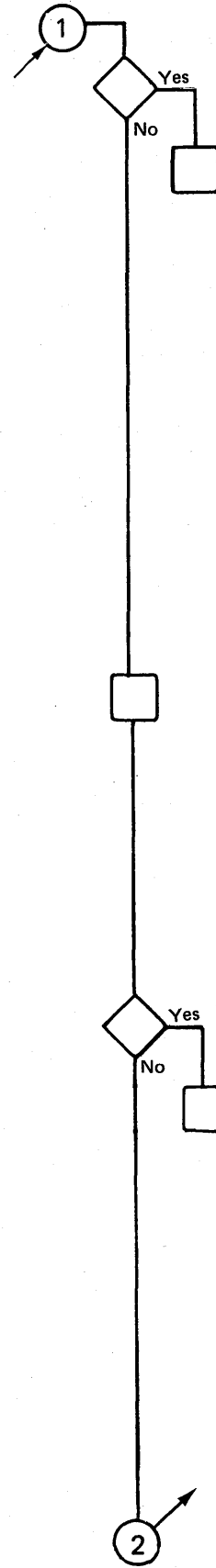
- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coil between the following pins:
 OXD-A1A1G02 and OXD-A1A1J02
 OXD-A1A1G04 and OXD-A1A1J04

Is less than 20 ohms present (YZ566)?

- Replace the phase control card at OXD-A1A1 (see Caution at the top of this column).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Check for ac at the cathode of the failing SCR(s).
- Check the failing SCR(s) and cabling from the phase control card.
- See note 1 if applicable.
- See note 7.

- Press POWER OFF.
- Disconnect the laminar bus lugs at OXA-TB1-6,7, and 8 (YZ536, D-550).
- Press POWER ON.



Is -4 Vdc present at OXA-TB1-13?

- Determine which lead causes the under-voltage on the -4 V supply by powering up after replacing the laminar bus lugs one at a time.

Caution: Isolate the short to a logic board by removing the laminar bus or storage voltage jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.

- Isolate to a card by removing cards.
- See note 1 if applicable.
- See note 7.

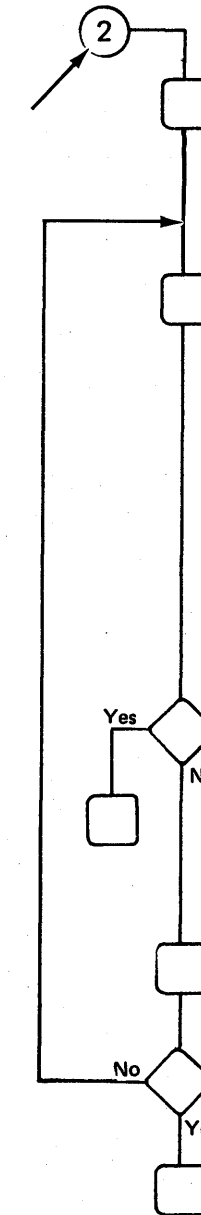
- Press POWER OFF.
- Reconnect the laminar bus lugs at OXA-TB1-6,7, and 8.
- Disconnect the laminar bus lugs at OXA-TB1-9, 10, 11, and 13.
- Place a jumper between OXA-TB1-13 and OXA-W2-6.
- Press POWER ON.

Is -4 Vdc present at OXA-TB1-13?

- Determine which lead causes the under-voltage on the -4 V supply by powering up after replacing the laminar bus lugs one at a time.

Caution: Isolate the short to a logic board by removing the laminar bus or storage voltage jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.

- Isolate to a card by removing cards.
- See note 1 if applicable.
- See note 7.



- Press POWER OFF.
- Reconnect the laminar bus lugs at OXA-TB1-9, 10, 11, and 13.
- Remove the jumper between OXA-TB1-13 and OXA-W2-6.

- Test for a shorted filter capacitor (OXF-C1, OXF-C2, OXF-C9, or OXF-C10). (YZ586 sheet 6)

DANGER
 Measure the voltage across the capacitor (to ensure it has discharged) before touching any leads.

- Remove one capacitor terminal lead at a time. The jumper to the next capacitor must be connected to the removed lead by a screw and nut, or control of the power supply will not be established once the shorted capacitor is removed from the circuit.
- Press POWER ON.

Is -4 Vdc present at OXA-TB1-13?

- Replace the shorted capacitor.
- See note 1 if applicable.
- See note 7.

- Press POWER OFF.
- Reconnect the lead to the capacitor.

Have all capacitors for this voltage been checked?

- Adjust the -4 V pot on the phase control card at OXD-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it. See Caution at the top of column one on this page.
- Adjust voltages (D-580).
- Check for open OXF-L1, OXF-L2 and OXF-L3 chokes (YZ586, sheet 6).
- See note 1 if applicable.
- See note 7.

- Notes:**
1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
 7. Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

+3.4V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM (OXD GATE WITH ONLY TWO OR THREE CARDS)

Caution: A shorted SCR can damage a phase control card (OXD-A1A1), also a defective phase control card can damage an SCR (see "Testing the SCR for Shorts" on page D-560).

- Press POWER OFF.

Note: Frames without storage must have a jumper installed between OXD-E1G08 and OXD-E1J08.

Caution: Remove the FET array cards. Possible locations at OXB-A1 are J2/J4, K2/K4, L2/L4, M2/M4, N2/N4, P2/P4, Q2/Q4, and R2/R4. Keep them in order so that each may be installed in its original location.

Is OXH-CP5 tripped (YZ586, sheet 16)?

- Place a jumper between pins OXD-A1E1G12 and OXD-A1E1J08 (disables the 12 second time out) if not already present.
- Press POWER ON.

Is 0 Vdc present at OXB-TB2-1? (+3.4 V sense, YZ536)

Is at least +1.0 Vdc present at OXD-A1E1M07 (drive signal for +3.4 V supply, YZ551)?

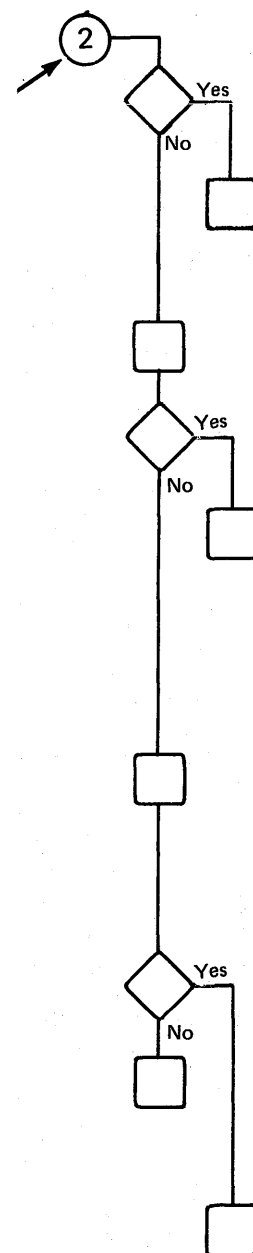
Caution: Do not short OXD-A1E1M07 to adjacent pins. Card damage may occur.

- Replace the frame sequence card at OXD-A1E1.
- If the problem still exists, replace the phase control card at OXD-A1A1 instead (see Caution at the top of this column).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See notes 3 and 7.

Is approximately 40 Vac peak-to-peak (15 Vac rms) present at cathode of SCR 3 (+3.4 V supply input voltage, YZ566)?

- Check PPB-T3 and the PPB-K2-1 points (YZ530).
- See note 1 if applicable.
- See notes 3 and 7.

- Replace the phase control card at OXD-A1A1 (see Caution at the top of this column).
- Adjust Voltages (D-580).
- If the problem still exists, check OXH-CP5, OXH-L8 choke, SCRs, and T3 instead (YZ586, sheet 16).
- Check circuit.
- See note 1 if applicable.
- See notes 3 and 7.



Is +3.4 Vdc present at OXB-TB2-1?

- Replace the frame sequence card at OXD-A1E1.
- Check the cabling from OXB-TB2-1 to OXD-A1E1M05.
- See note 1 if applicable.
- See notes 3 and 7.
- Scope the +3.4 V SCRs at the base of OXH-HS8 (YZ586, sheet 16).

Are both SCRs firing? (see D-560)

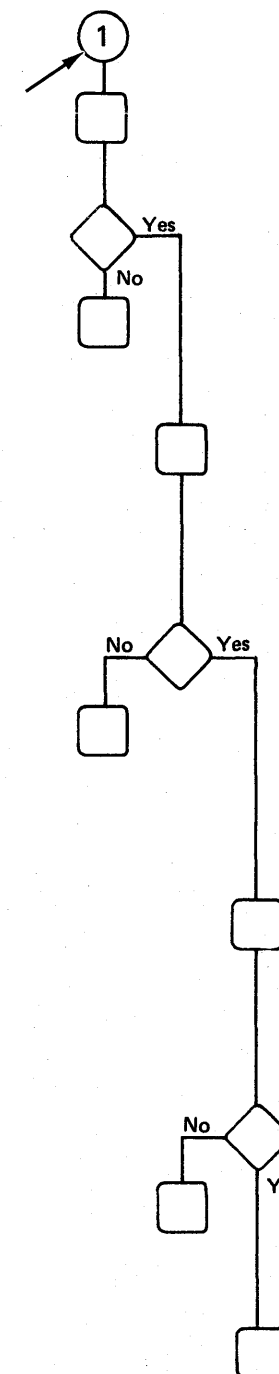
- Adjust the +3.4 V pot on the phase control card at OXD-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See notes 3 and 7.

- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins: OXD-A1A1S05 and OXD-A1A1U05, OXD-A1A1S07 and OXD-A1A1U07

Is less than 20 ohms present? (YZ566)

- Replace the phase control card at OXD-A1A1 (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See notes 3 and 7.

- Check for ac at the cathode of the failing SCR.
- Check the failing SCR and cabling from the phase control card.
- Check OXH-CP5.
- See note 1 if applicable.
- See notes 3 and 7.



- Press POWER OFF.
- Reset OXH-CP5.
- Press POWER ON.

Does OXH-CP5 trip again?

- Suspect a bad FET array card or a defective circuit protector, OXH-CP5.
- See notes 1 and 7 if applicable.
- See note 3.

Does OXH-CP5 trip again?

- Press POWER OFF.
- Disconnect the storage gate leads at OXB-TB2-1 and OXB-TB2-2. Be sure that the +3.4 V sense lead is still connected to the supply voltage (YZ536).
- Reset OXH-CP5.
- Press POWER ON.

Does OXH-CP5 trip again?

- Check for a shorted board or card in the OXB gate.
- Reconnect the storage gate leads at OXB-TB2-1,2.
- See notes 1 and 7 if applicable.
- See note 3.

Does OXH-CP5 trip again?

- Press POWER OFF.
- Reconnect the storage gate leads at OXB-TB2-1,2.
- Disconnect the leads at OXH-C7(+) and OXH-C8(+) (YZ586, sheet 16).
- Reset OXH-CP5.
- Press POWER ON.

Does OXH-CP5 trip again?

- Check for a shorted capacitor, OXH-C7 or OXH-C8.
- See notes 1 and 7 if applicable.
- See note 3.

- Check for a bad circuit protector, OXH-CP5.
- Reconnect the leads at OXH-C7(+) and OXH-C8(+).
- See notes 1 and 7 if applicable.
- See note 3.

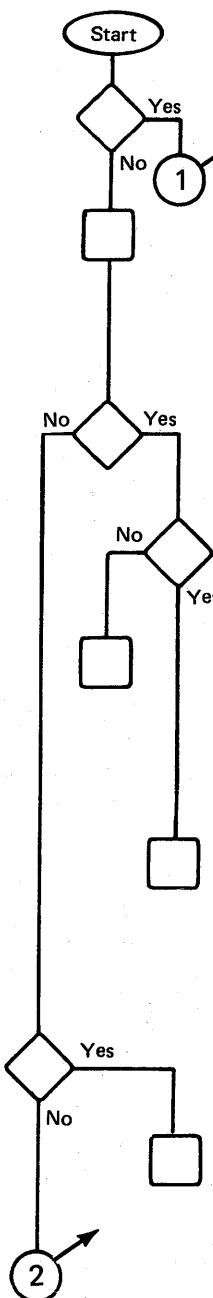
Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
3. Reinstall the removed FET array cards in their original locations.
7. Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

**3705-II POWER—MAINTENANCE
ANALYSIS PROCEDURES (MAPs)**

**+6V UNDERVOLTAGE PROBLEM IN A
FRAME WITH MODIFIED POWER SYSTEM
(OXD GATE WITH ONLY TWO OR THREE
CARDS)**

Caution: A shorted SCR can damage a phase control card (OXD-A1A1), also a defective phase control card can damage an SCR (see "Testing the SCR for Shorts" on page D-560).



Is OXF-CP1 tripped (YZ586, sheet 4)?

- Press POWER OFF.
- Place a jumper between pins OXD-A1E1G12 and OXD-A1E1J08 (disables the 12 second time out) if not already present.
- Press POWER ON.

Is 0 Vdc present at OXA-TB1-12 (+6 V sense, YZ536)?

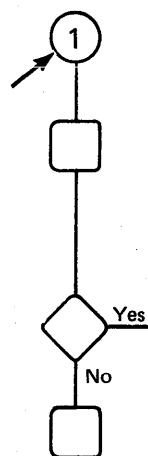
Is at least +1.0 Vdc present at OXD-A1E1M04 (drive signal for +6 V supply)? Caution: Do not short OXD-A1E1M04 to adjacent pins. Card damage may occur.

- Replace the frame sequence card at OXD-A1E1.
- If the problem still exists, replace the phase control card at OXD-A1A1 instead (see Caution at the top of this column).
- Adjust voltages (D-580).
- Check circuit.
- See note 1 if applicable.
- See note 7.

- Replace the phase control card at OXD-A1A1 (see Caution at the top of this column).
- Adjust voltages (D-580).
- If the problem still exists, check OXF-CP1, OXF-L4 choke, SCRs, and T3 instead (YZ586, sheet 6).
- See note 1 if applicable.
- See note 7.

Is +6 Vdc present at OXA-TB1-12?

- Replace the frame sequence card at OXD-A1E1.
- Check the cabling to OXD-A1E1P02 (YZ529).
- See note 1 if applicable.
- See note 7.



- Press POWER OFF.
- Disconnect the laminar bus lugs at OXA-TB1-5 and OXA-TB1-12 (YZ536, D-550).
- Reset OXF-CP1.
- Press POWER ON.

Does OXF-CP1 trip again?

- Determine which lead causes the circuit protector to trip by powering up after replacing the laminar bus lugs one at a time.

CAUTION

Isolate the short to a logic board by removing the laminar bus jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.

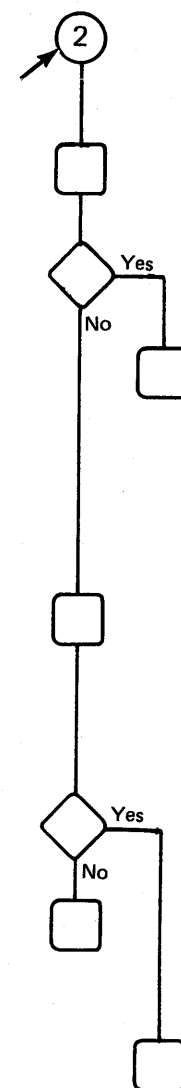
- Isolate to a card by removing cards.
- See notes 1 and 7 if applicable.

- Press POWER OFF.
- Reconnect the laminar bus lugs at OXA-TB1-5 and OXA-TB1-12.
- Disconnect the lead at OXF-C3(+) (YZ586, sheet 6).
- Reset OXF-CP1.
- Press POWER ON.

Does OXF-CP1 trip again?

- Replace the shorted capacitor, OXF-C3.
- See notes 1 and 7 if applicable.

- Check for a bad circuit protector, OXF-CP1.
- Reconnect the lead at OXF-C3(+).
- See notes 1 and 7 if applicable.



- Scope the +6 V SCRs at the base of OXF-HS7 (YZ586, sheet 6)

Are both SCRs firing (see D-560)?

- Adjust the +6 V pot on the phase control card at OXD-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins: OXD-A1A1G07 and OXD-A1A1J07, OXD-A1A1G08 and OXD-A1A1J08

Is less than 20 ohms present (YZ566)?

- Replace the phase control card at OXD-A1A1 (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Check for ac at the cathode of the failing SCR.
- Check the failing SCR and cabling from the phase control card.
- See note 1 if applicable.
- See note 7.

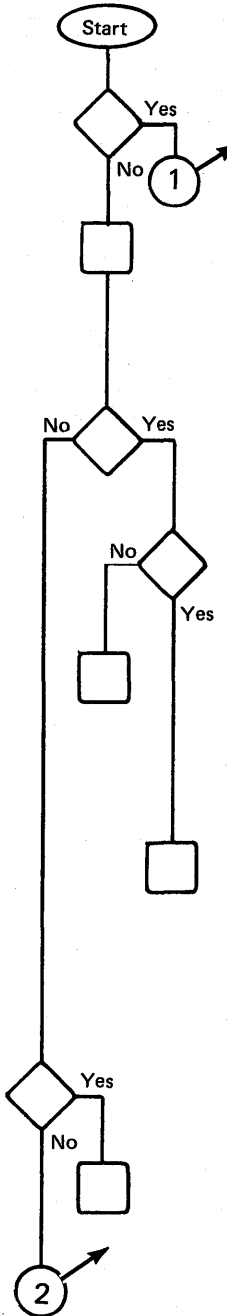
Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
7. Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

3705-II POWER—MAINTENANCE ANALYSIS PROCEDURES (MAPs)

-12V UNDERVOLTAGE PROBLEM IN A FRAME WITH MODIFIED POWER SYSTEM (OXD GATE WITH ONLY TWO OR THREE CARDS)

Caution: A shorted SCR can damage a phase control card (OXD-A1A1), and a defective phase control card can damage an SCR (see "Testing the SCR for Shorts" on page D-560).



Is OXF-CP2 tripped (YZ586, sheet 6)?

- Press POWER OFF.
- Place a jumper between pins OXD-A1E1G12 and OXD-A1E1J08 (disables the 12 second time out) if not already present.
- Press POWER ON.

Is 0 Vdc present at OXA-TB1-3 (-12 V sense, YZ536)?

Is at least 1.0 Vdc present at OXD-A1E1M13 (drive signal for -12 V supply)?

Caution: Do not short OXD-A1E1M13 to adjacent pins; card damage may occur.

- Replace the frame sequence card at OXD-A1E1.
- If the problem still exists, replace the phase control card at OXD-A1A1 instead (see Caution at the top of this column).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Replace the phase control card at OXD-A1A1 (see Caution at the top of this column).
- Adjust voltages (D-580).
- If the problem still exists, check OXF-CP2, OXF-L5 choke, SCRs, and T3 instead (YZ586, sheet 6).
- Check circuit.
- See note 1 if applicable.
- See note 7.

Is -12 Vdc present at OXA-TB1-3?

- Replace the frame sequence card at OXD-A1E1.
- Check the cabling to OXD-A1E1P07 (YZ529).
- See note 1 if applicable.
- See note 7.

- Press POWER OFF.
- Disconnect the laminar bus lugs at OXA-TB1-3 and OXA-TB1-4 (YZ536, D-550).
- Reset OXF-CP2.
- Press POWER ON.

Does OXF-CP2 trip again?

- Determine which lead causes the circuit protector to trip by powering up after replacing the laminar bus lugs one at a time.

CAUTION

Isolate the short to a logic board by removing the laminar bus jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.

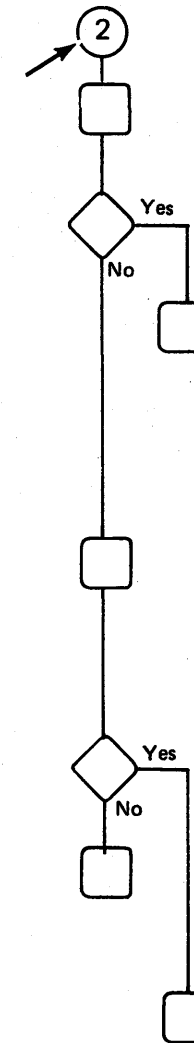
- Isolate to a card by removing cards.
- See notes 1 and 7 if applicable.

- Press POWER OFF.
- Reconnect the laminar bus lugs at OXA-TB1-3 and OXA-TB1-4.
- Disconnect the lead at OXF-C4(+).
- Reset OXF-CP2.
- Press POWER ON.

Does OXF-CP2 trip again (YZ586, sheet 6)?

- Replace the shorted capacitor, OXF-C4.
- See notes 1 and 7 if applicable.

- Check for a bad circuit protector, OXF-CP2.
- Reconnect the lead at OXF-C4(+).
- See notes 1 and 7 if applicable.



- Scope the -12 V SCRs at the base of OXF-HS5 (YZ586, sheet 6).

Are both SCRs firing (see D-560)?

- Adjust the -12 V pot on the phase control card at OXD-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins:
 OXD-A1A1G03 and OXD-A1A1J03
 OXD-A1A1G05 and OXD-A1A1J05

Is less than 20 ohms present (YZ566)?

- Replace the phase control card at OXD-A1A1 (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Check for ac at the cathode of the failing SCR.
- Check the failing SCR and cabling from the phase control card.
- See note 1 if applicable.
- See note 7.

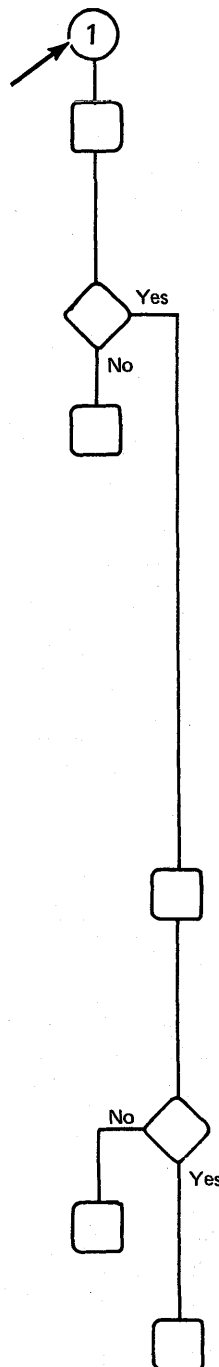
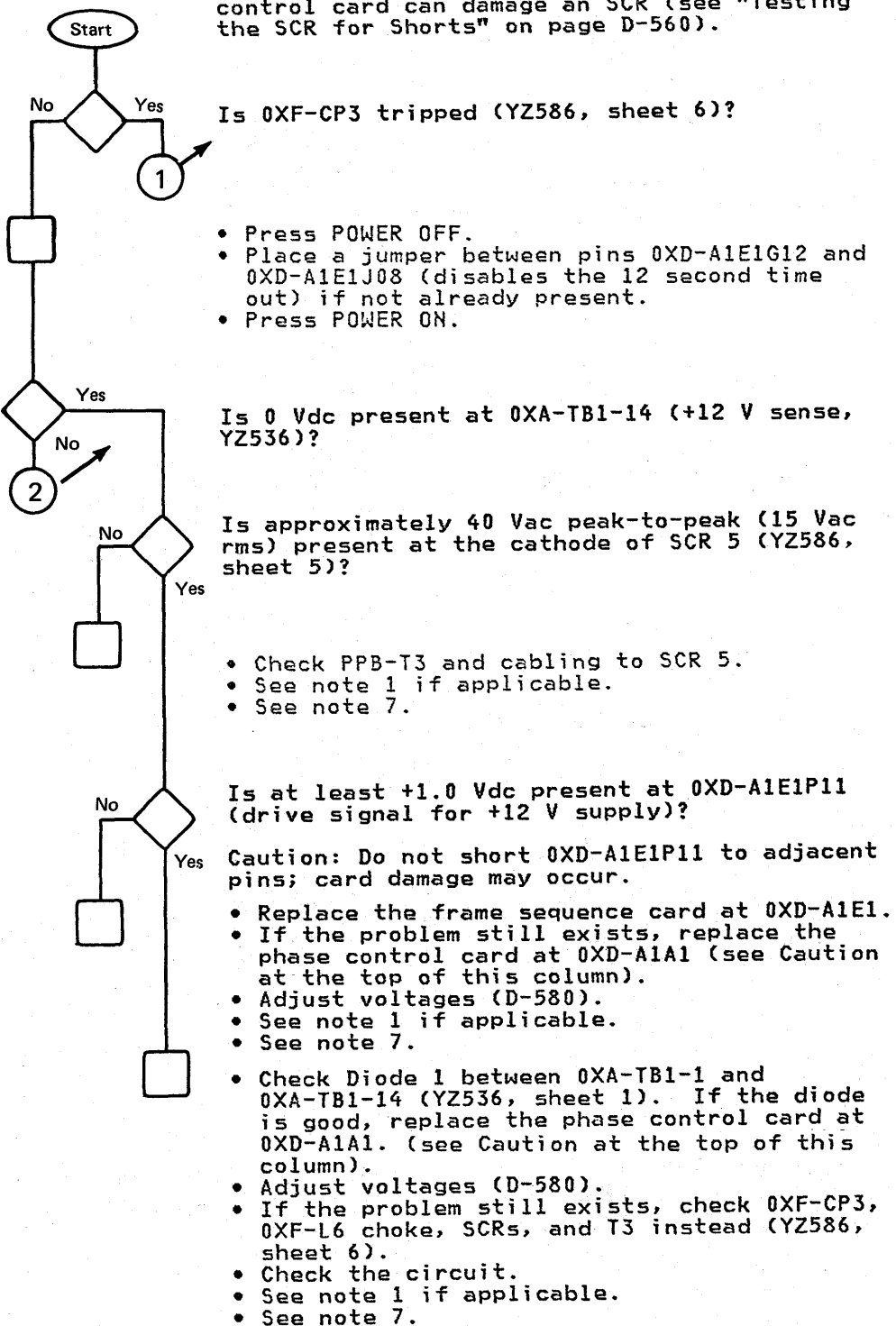
Notes:

1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
7. Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

**3705-II POWER—MAINTENANCE
ANALYSIS PROCEDURES (MAPs)**

**+12V UNDERVOLTAGE PROBLEM IN A
FRAME WITH MODIFIED POWER SYSTEM
(OXD GATE WITH ONLY TWO OR THREE
CARDS)**

Caution: A shorted SCR can damage a phase control card (OXD-A1A1), and a defective phase control card can damage an SCR (see "Testing the SCR for Shorts" on page D-560).



- Press POWER OFF.
- Disconnect the laminar bus lugs at OXA-TB1-1 and OXA-TB1-2 (YZ536, D-550).
- Reset OXF-CP3.
- Press POWER ON.

Does OXF-CP3 trip again?

- Determine which lead causes the circuit protector to trip by powering up after replacing the laminar bus lugs one at a time.

CAUTION

Isolate the short to a logic board by removing the laminar bus jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.

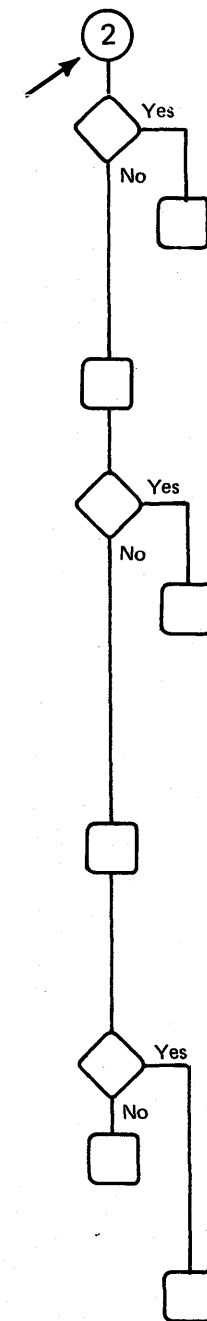
- Isolate to a card by removing cards.
- See notes 1 and 7 if applicable.

- Press POWER OFF.
- Reconnect the laminar bus lugs at OXA-TB1-1 and OXA-TB1-2.
- Disconnect the lead at OXF-C5(+) (YZ586, sheet 6).
- Reset OXF-CP3.
- Press POWER ON.

Does OXF-CP3 trip again?

- Replace the shorted capacitor, OXF-C5.
- See notes 1 and 7 if applicable.

- Check for a bad circuit protector, OXF-CP3.
- Reconnect the lead at OXF-C5(+).
- See notes 1 and 7 if applicable.



Is +12 Vdc present at OXA-TB1-1?

- Replace the frame sequence card at OXD-A1E1.
- Check the cabling to OXD-A1E1M03 (YZ529).
- See note 1 if applicable.
- See note 7.

- Scope the +12 V SCRs at the base of OXF-HS6 (YZ586, sheet 6).

Are both SCRs firing (see D-560)?

- Adjust the +12 V pot on the phase control card at OXD-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it. (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins:
OXD-A1A1G10 and OXD-A1A1J10
OXD-A1A1G12 and OXD-A1A1J12

Is less than 20 ohms present (YZ566)?

- Replace the phase control card at OXD-A1A1 (see Caution at the top of column one).
- Adjust voltages (D-580).
- See note 1 if applicable.
- See note 7.

- Check for ac at the cathode of the failing SCR.
- Check the failing SCR and cabling from the phase control card.
- See note 1 if applicable.
- See note 7.

Notes:

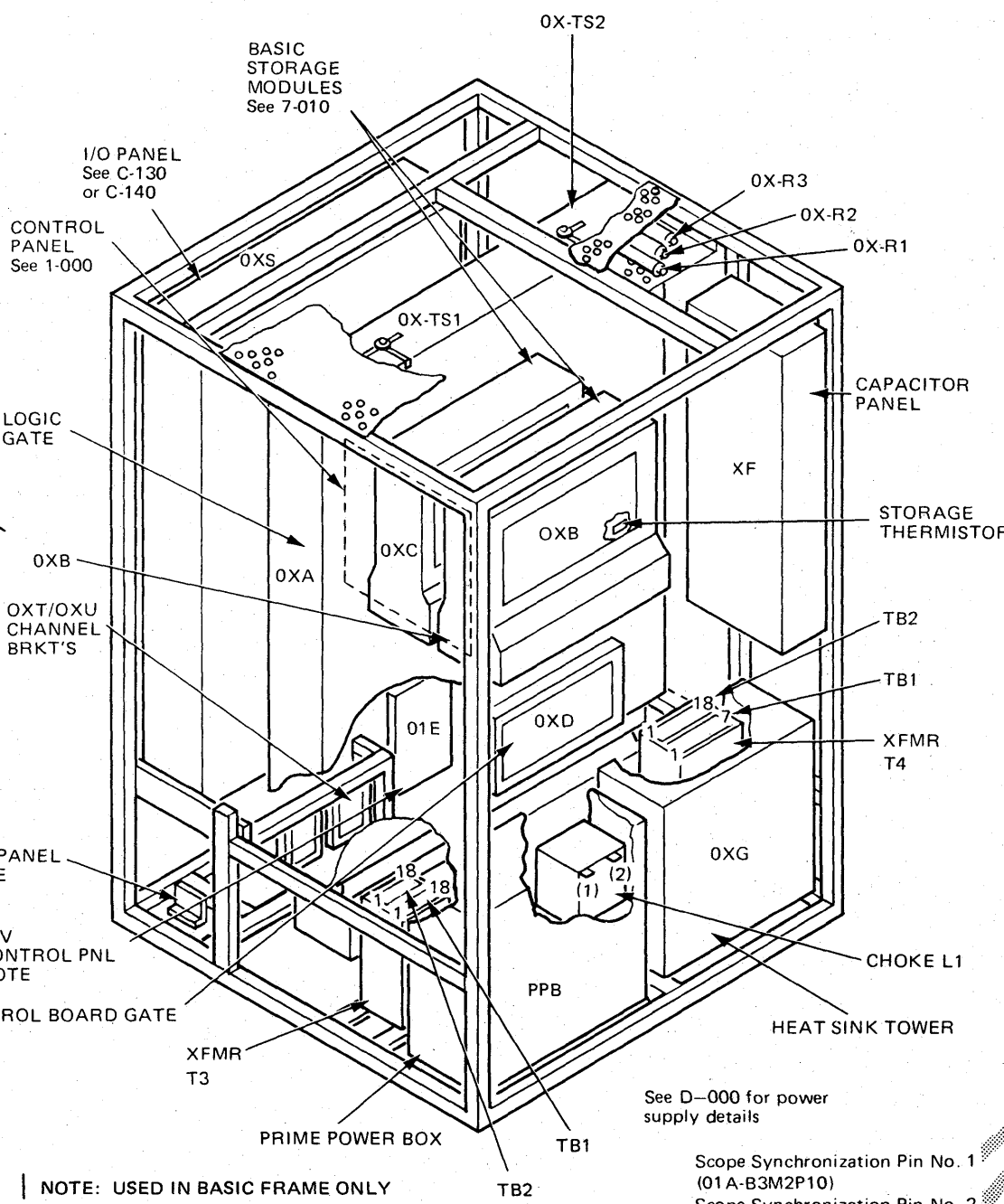
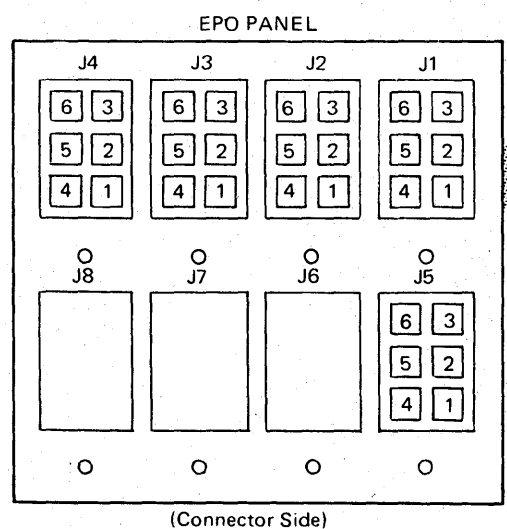
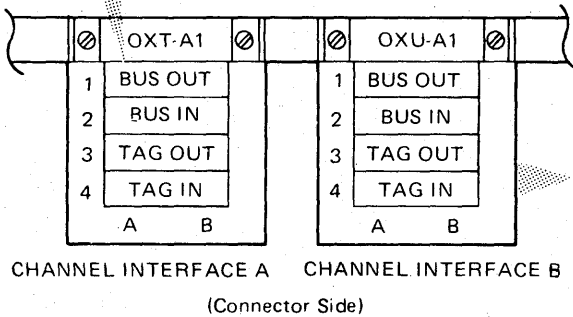
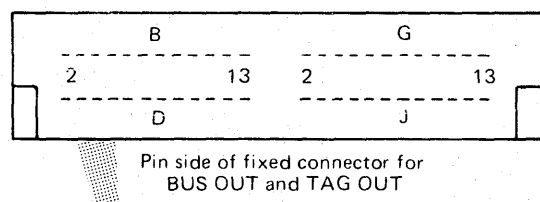
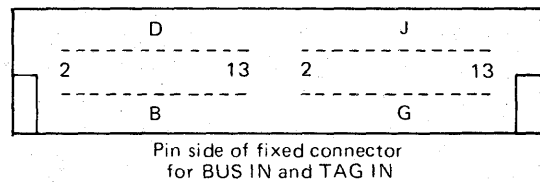
1. Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
7. Remove the jumper between pins OXD-A1E1G12 and OXD-A1E1J08.

3705-I PHYSICAL LOCATIONS

See logic pages YZ301 sheets 1-13 for physical location details not shown on this page.

- 0XA-X1 Board = Type 1 LIB
- 0XA-X2 Board = Type 2 LIB
- 0XA-X3 Board = Type 3 LIB
- 0XA-X4 Board = Type 4 LIB
- 01A-X5 Board = Type 5 LIB
- 0XA-X6 Board = Type 6 LIB
- 0XA-X7 Board = Type 7 LIB
- 0XA-X8 Board = Type 8 LIB
- 0XA-X9 Board = Type 9 LIB
- 0XA-W1 Board = Type 10 LIB
- 01A-W2 Board = Type 11 LIB
- 0XA-W3 Board = Type 12 LIB

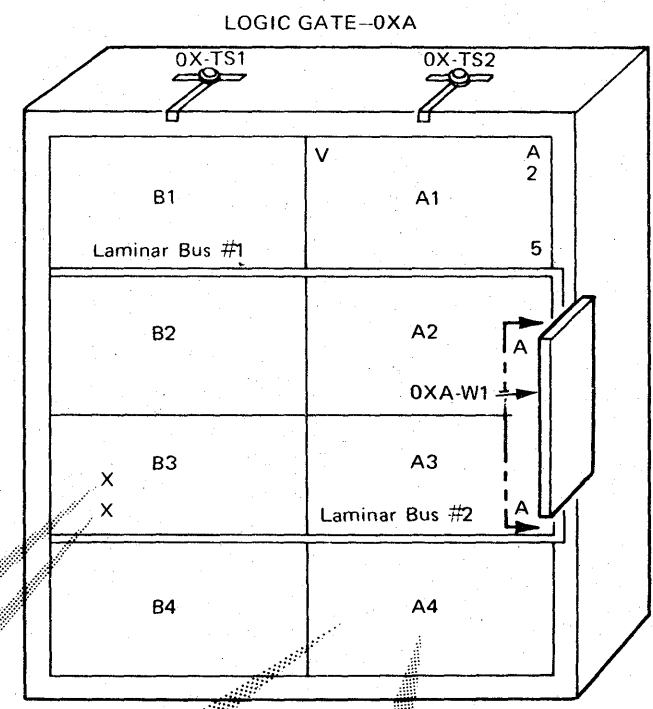
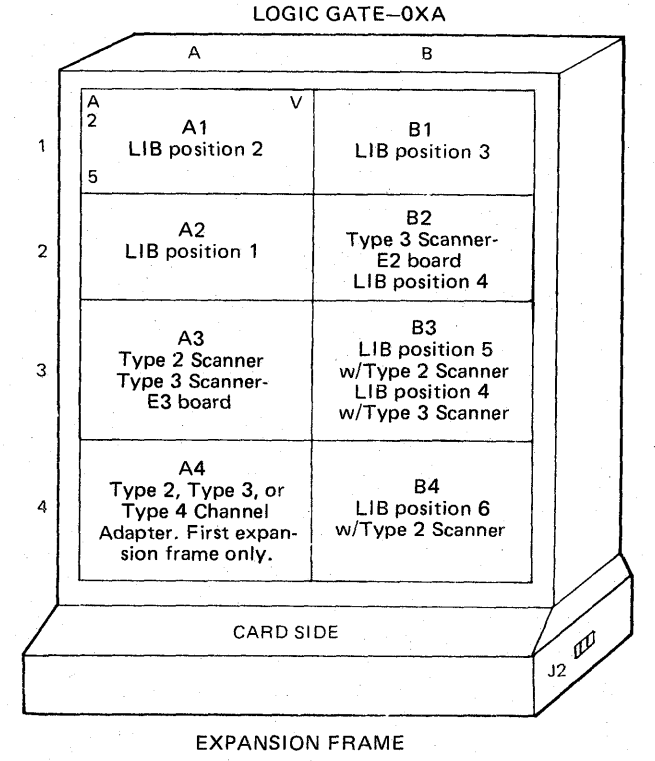
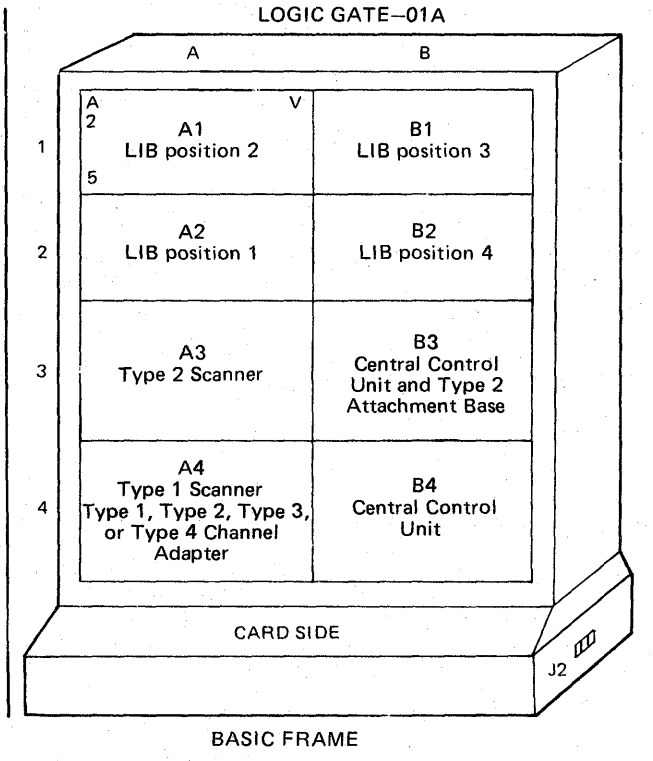
Terminator Assemblies		BUS TAG CABLE	
S/360	P/N 5440649	P/N 5440650	P/N 5353920
S/370	P/N 2282675	P/N 2282676	P/N 5466456



See D-000 for power supply details

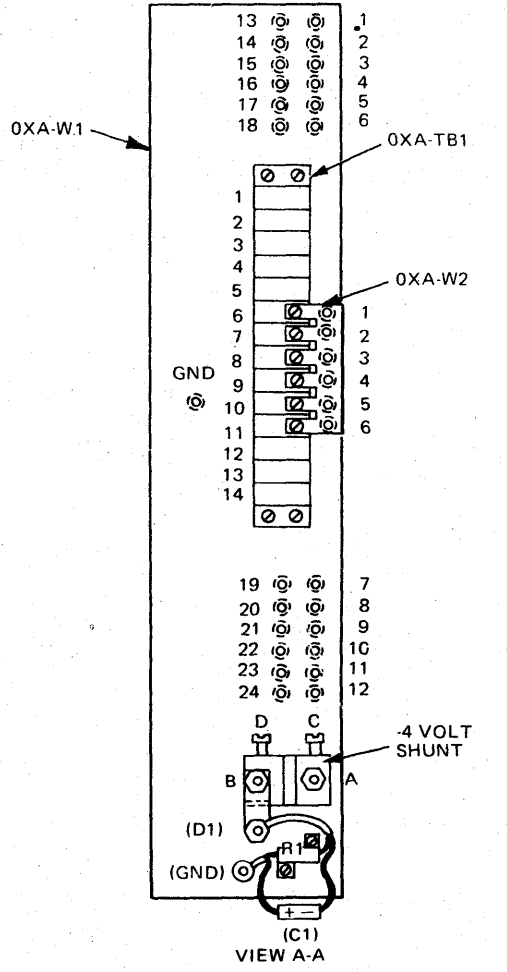
Scope Synchronization Pin No. 1 (01A-B3M2P10)
Scope Synchronization Pin No. 2 (01A-B3M2P13)

NOTE: USED IN BASIC FRAME ONLY



- Y4 = Type 1 Channel Adapter and Type 1 Communication Scanner
- Z4 = Type 2 Channel Adapter
- W4 = Type 3 Channel Adapter
- E4 = Type 4 Channel Adapter

Diskette Controller with or without Type 1 Communication Scanner-Note 1



TOOLS AND TEST EQUIPMENT

PREVENTIVE MAINTENANCE

A. Special tools, test equipment, and maintenance supplies to be shipped with the 3705:

Description	P/N
Thermometer	5392366 (3705-1 only)
"Y" Jumper	1770810
Jumper	1770811
Test Block	1770812

B. Test equipment and non-technology related tools required for the 3705:

1. Test equipment

P/N	Description	Quantity
454550	454 Tektronix* Scope	1
or		
453047	453 Tektronix* Scope	1
453585	Digitec**251 or 266 Meter	1
453545	db Meter	1
5851882	MST 1 CE Indicator Latch Card	1

2. Tools

P/N	Description	Quantity
453631	Microfiche Viewer	1
5801645	Back Panel Indicator Card	1

C. Technology related tools

Refer to Tools and Test Equipment TSL No. 43 and to the *Monolithic System Technology, Packaging, Tools, Wiring Change Procedure, SY22-6739* for tool requirements of the IBM 3705. Some of these tools may not be part of the normal maintenance package and should not be ordered by the Branch Office.

* Trademark of Tektronix, Inc.

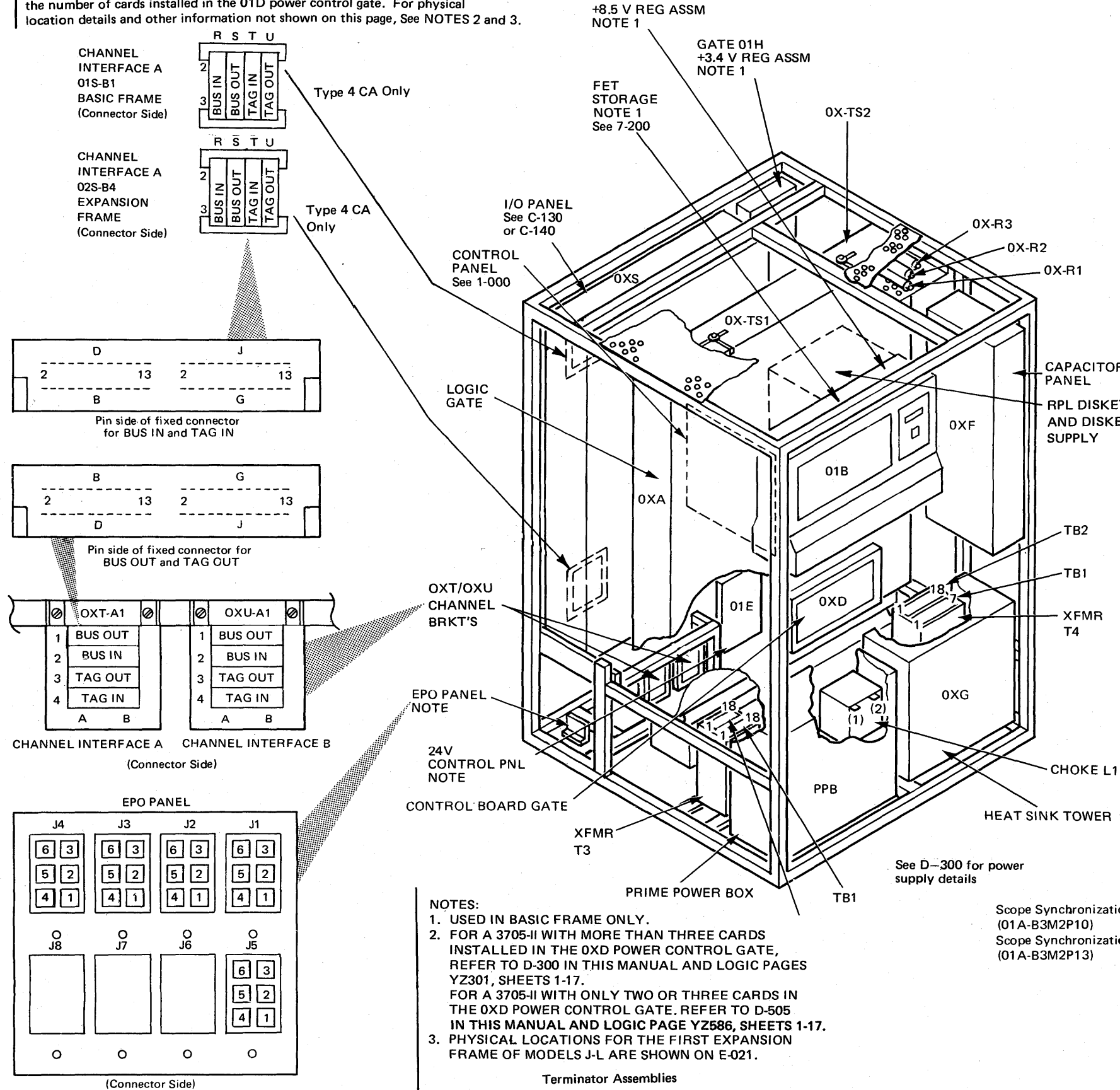
** Trademark of United Systems Corporation

UNIT	FREQ	CHECK	WHEN CHECKED
		1. Check all voltages	At installation
		2. Tighten all screw type connections of power system	At installation and 6 months after installation
		3. Check indicators	On each call
1	6	4. Check cooling fans	Determined by the operating environment
		5. Check air filters	
2	12	6. Check line cord, plug, terminals, and grounding	Every 12 months
		7. Scope all SCRs	Every 12 months

3705-II PHYSICAL LOCATIONS

(BASIC FRAME OF MODELS E-L AND FIRST EXPANSION FRAME OF MODELS E-H)

The location and types of power supply components in a 3705-II depend upon the number of cards installed in the 01D power control gate. For physical location details and other information not shown on this page, See NOTES 2 and 3.

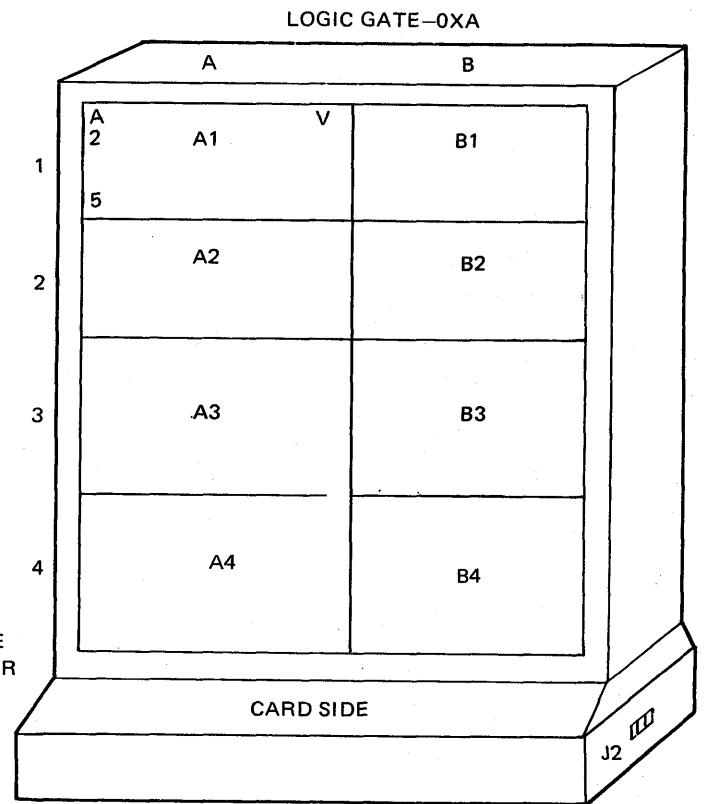


- NOTES:**
1. USED IN BASIC FRAME ONLY.
 2. FOR A 3705-II WITH MORE THAN THREE CARDS INSTALLED IN THE 0XD POWER CONTROL GATE, REFER TO D-300 IN THIS MANUAL AND LOGIC PAGES YZ301, SHEETS 1-17. FOR A 3705-II WITH ONLY TWO OR THREE CARDS IN THE 0XD POWER CONTROL GATE. REFER TO D-505 IN THIS MANUAL AND LOGIC PAGE YZ586, SHEETS 1-17.
 3. PHYSICAL LOCATIONS FOR THE FIRST EXPANSION FRAME OF MODELS J-L ARE SHOWN ON E-021.

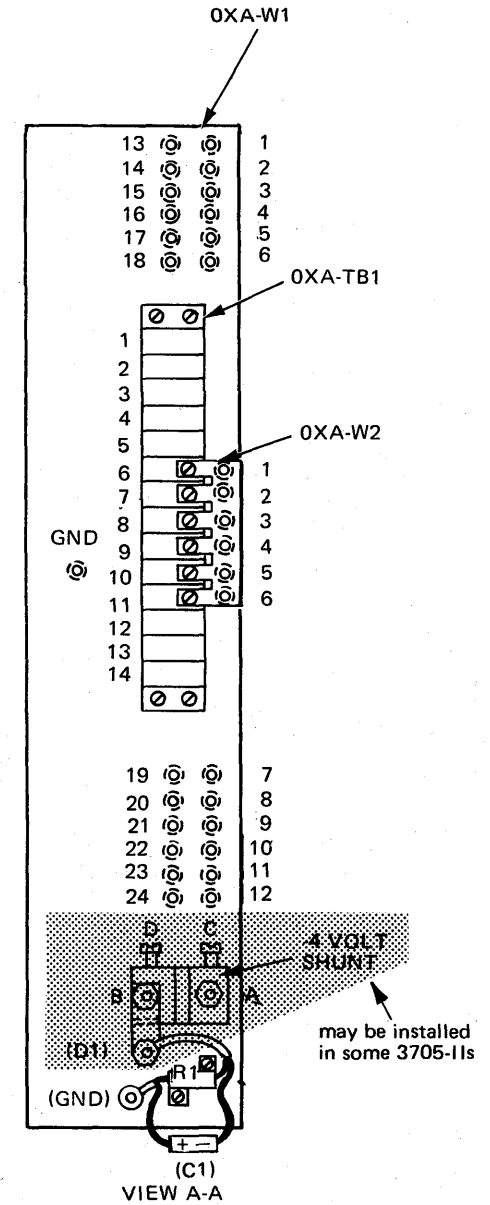
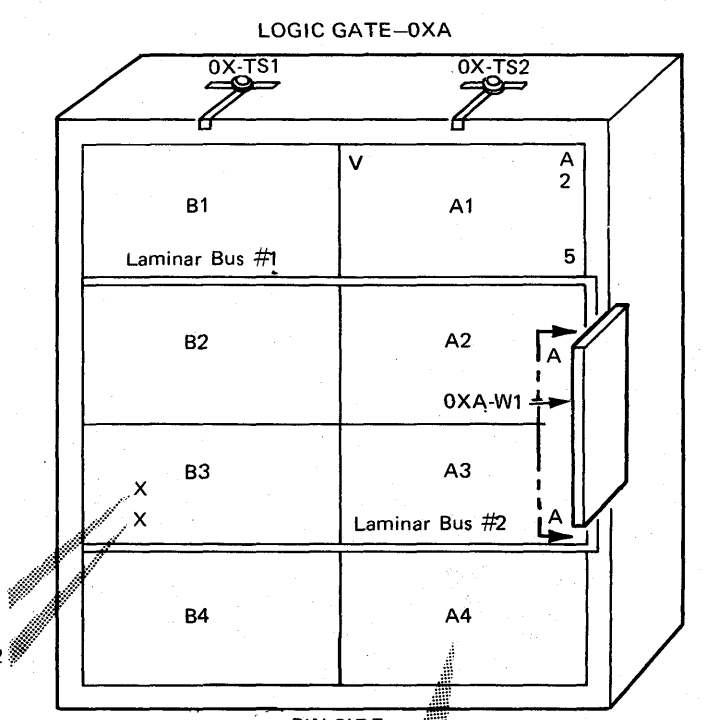
Terminator Assemblies

	BUS	TAG	CABLE
S/360	P/N 5440649	P/N 5440650	P/N 5353920
S/370	P/N 2282675	P/N 2282676	P/N 5466456

See E-030 for the feature board locations for all possible configurations.



- OXA-X1 Board = Type 1 LIB
- OXA-X2 Board = Type 2 LIB
- OXA-X3 Board = Type 3 LIB
- OXA-X4 Board = Type 4 LIB
- O1A-X5 Board = Type 5 LIB
- OXA-X6 Board = Type 6 LIB
- OXA-X7 Board = Type 7 LIB
- OXA-X8 Board = Type 8 LIB
- OXA-X9 Board = Type 9 LIB
- OXA-W1 Board = Type 10 LIB
- O1A-W2 Board = Type 11 LIB
- OXA-W3 Board = Type 12 LIB



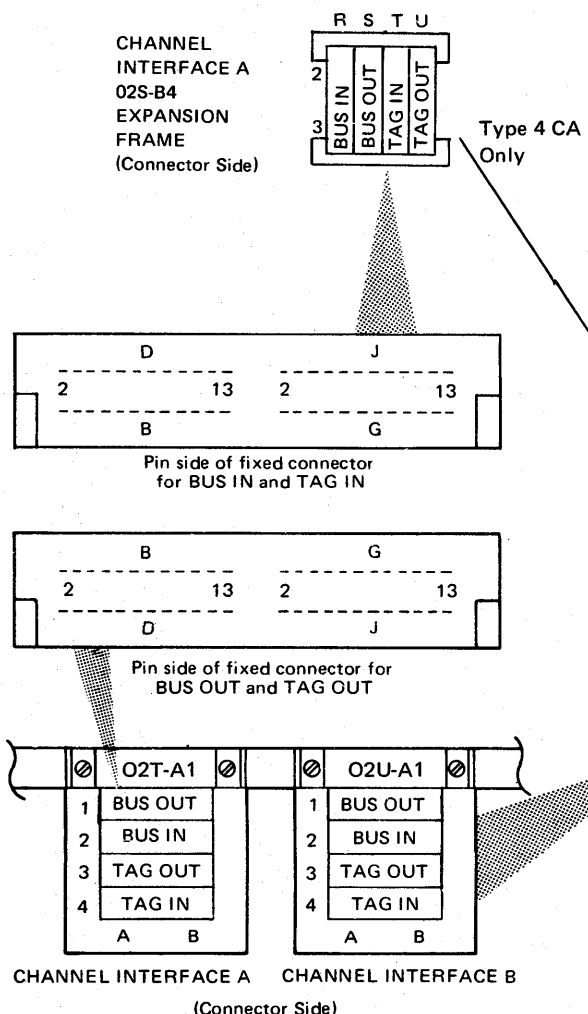
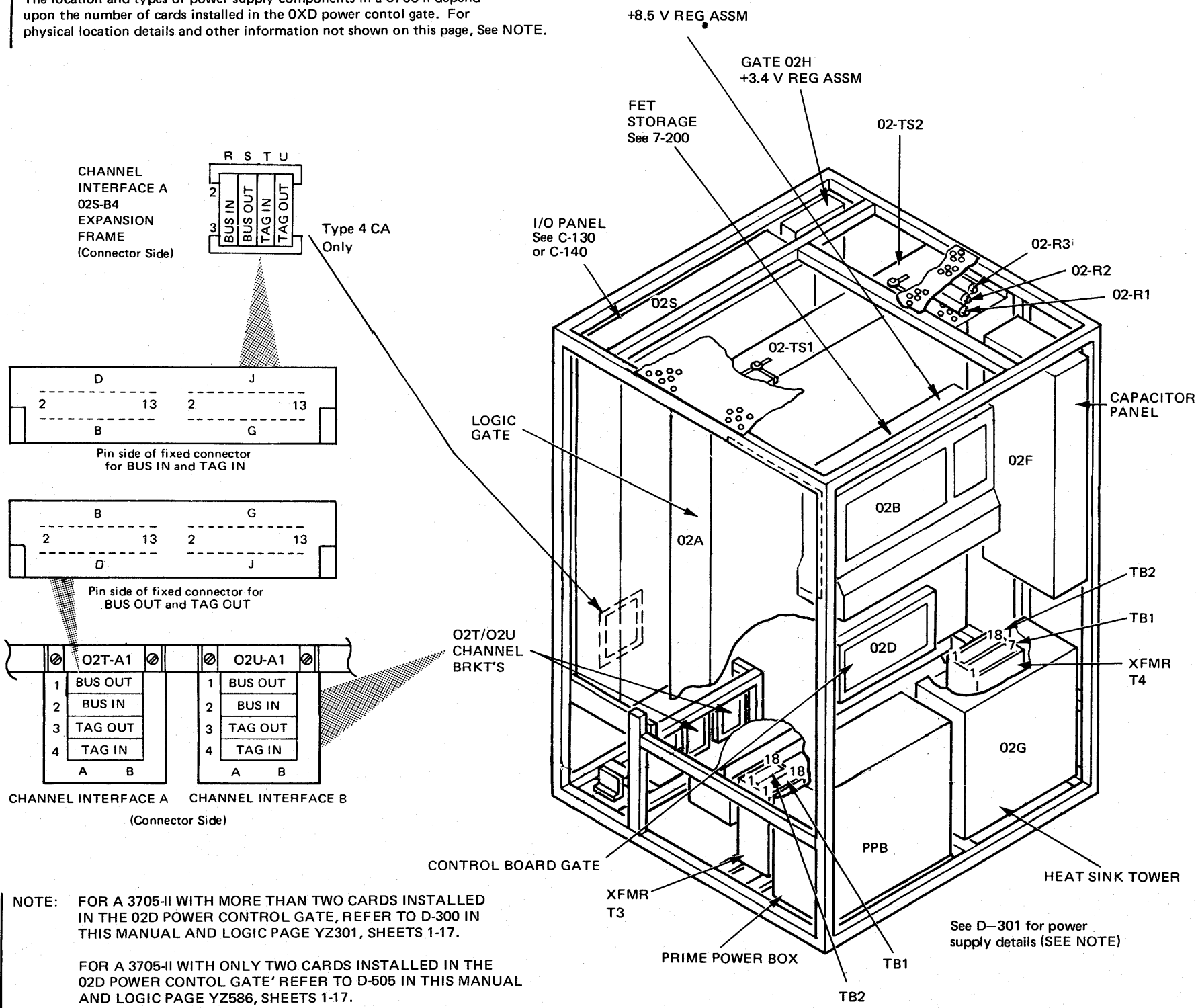
- Y4 = { Type 1 Channel Adapter and Type 1 Communication Scanner
- Z4 = Type 2 Channel Adapter
- W4 = Type 3 Channel Adapter
- E4 = Type 4 Channel Adapter

MISC



3705-II PHYSICAL LOCATIONS (FIRST EXPANSION FRAME OF MODELS J-L ONLY)

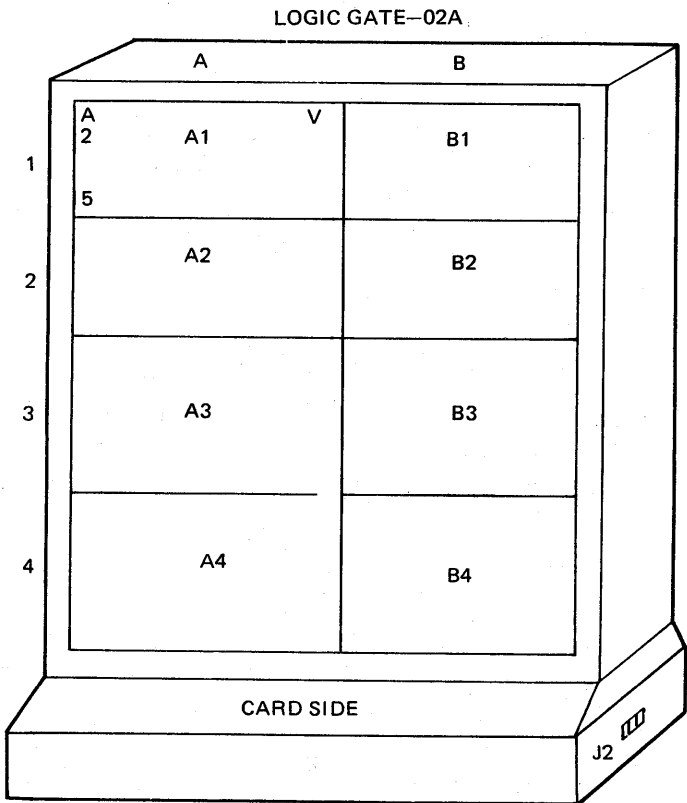
The location and types of power supply components in a 3705-II depend upon the number of cards installed in the OXD power control gate. For physical location details and other information not shown on this page, See NOTE.



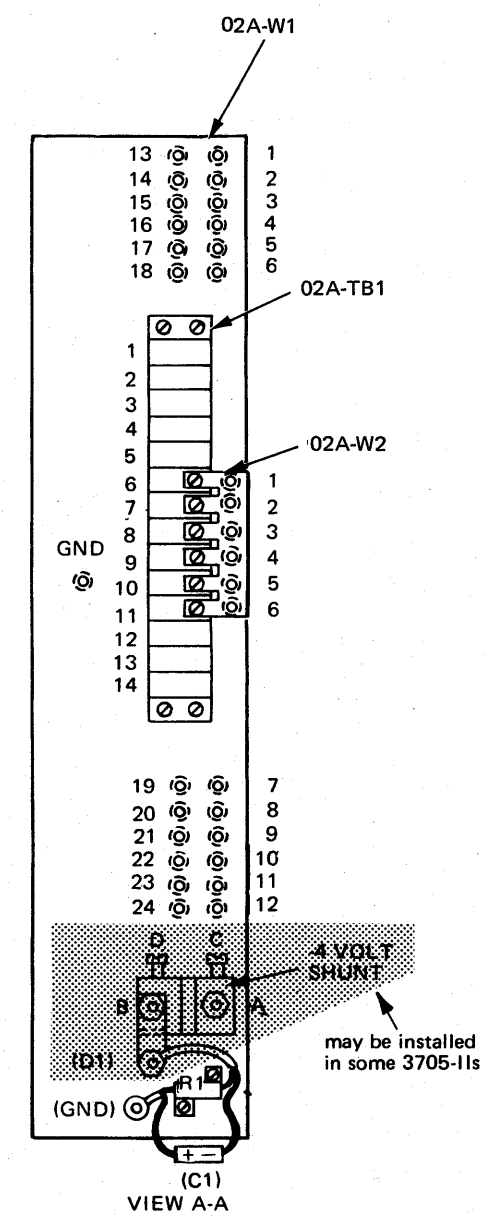
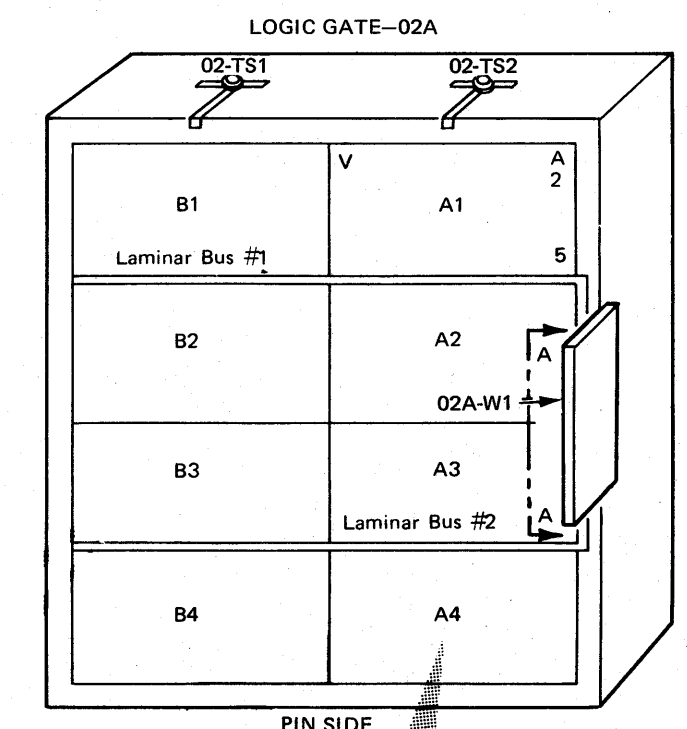
NOTE: FOR A 3705-II WITH MORE THAN TWO CARDS INSTALLED IN THE O2D POWER CONTROL GATE, REFER TO D-300 IN THIS MANUAL AND LOGIC PAGE YZ301, SHEETS 1-17.

FOR A 3705-II WITH ONLY TWO CARDS INSTALLED IN THE O2D POWER CONTROL GATE REFER TO D-505 IN THIS MANUAL AND LOGIC PAGE YZ586, SHEETS 1-17.

See E-030 for the feature board locations for all possible configurations.



- 02A-X1 Board = Type 1 LIB
- 02A-X2 Board = Type 2 LIB
- 02A-X3 Board = Type 3 LIB
- 02A-X4 Board = Type 4 LIB
- 02A-X6 Board = Type 6 LIB
- 02A-X7 Board = Type 7 LIB
- 02A-X8 Board = Type 8 LIB
- 02A-X9 Board = Type 9 LIB
- 02A-W1 Board = Type 10 LIB
- 02A-W3 Board = Type 12 LIB



- Z4 = Type 2 Channel Adapter
- W4 = Type 3 Channel Adapter
- E4 = Type 4 Channel Adapter



3705-II FEATURE BOARD LOCATIONS

3706 (Expansion Frame) 02A-XX		3705 (Basic Frame) 01A-XX	
A1	B1	A1	B1
A2	B2	A2	B2
A3	B3	A3	B3
A4	B4	A4	B4

NOTES: 1. All channel adapters are mounted in the basic frame and first expansion frame; therefore the other expansion frames are not shown here since they only contain scanners and LIBs.
2. See E-040 for the permissible combinations of channel adapters and the remote program loader feature.

3. The numbered entries are listed by priority; a (2) entry is valid only if (1) is not present. The bullet entries are listings of combinations without any priority.
4. The key symbols tie the CA numbers to a given combination; for example **1**, indicates the location on the feature board of CA #1, CA #2, CA #3, and CA #4 for "four CA4s".

Legend: CA #1 = Channel adapter number 1
CA4 = Type 4 channel adapter
RPL = Remote Program Loader

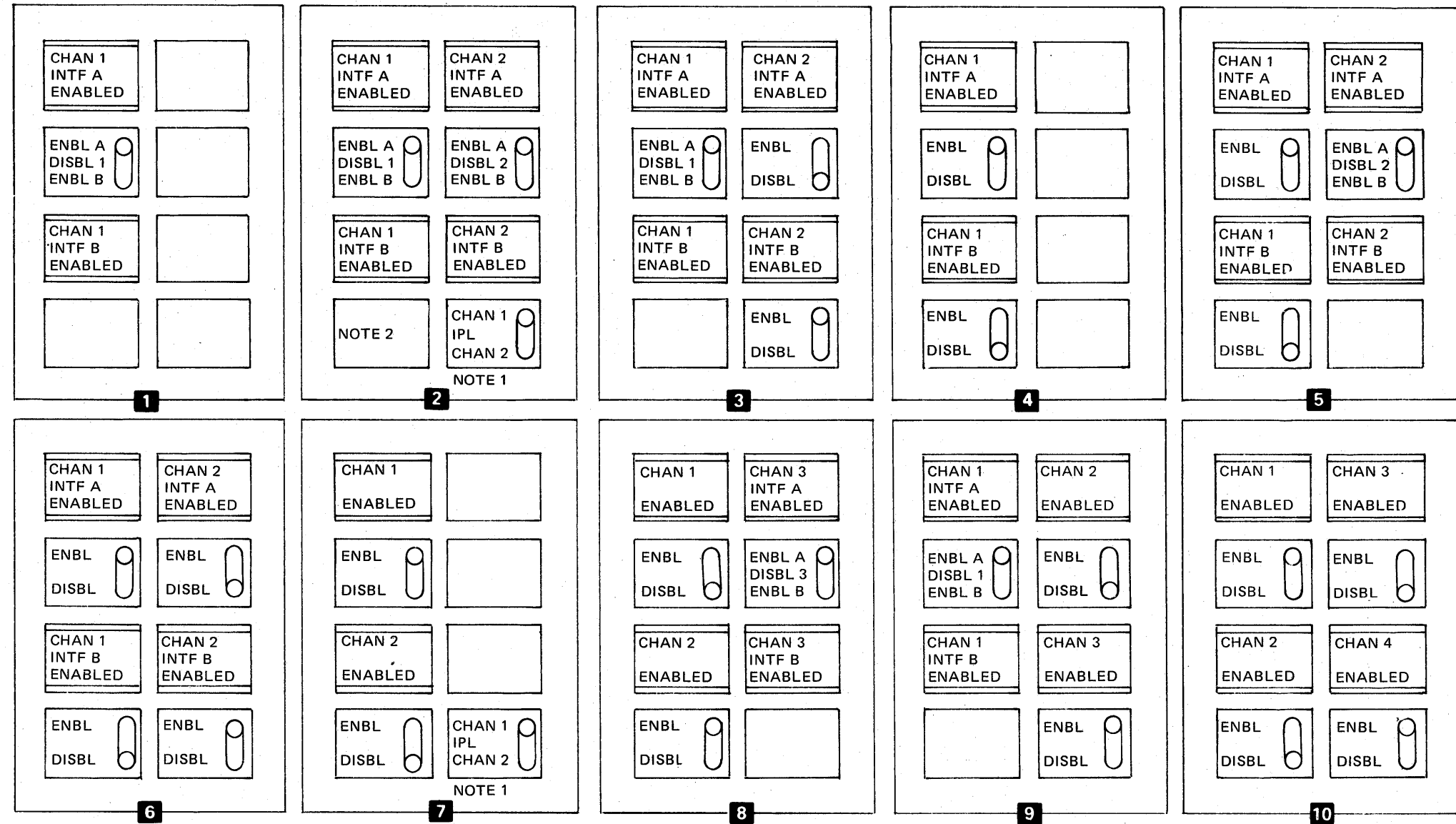
3705-II ALLOWABLE HARDWARE COMBINATIONS AND CONTROL PANEL CONFIGURATIONS

ALLOWABLE HARDWARE CONFIGURATIONS

Remote Program Loader And Channel Adapter Combinations								
RPL	CA #1 TYPE	CA #2 TYPE	CA #3 TYPE	BOARD LOCATIONS				CONTROL PANEL TYPE
				RPL	CA #1	CA #2	CA #3	
1	-	-	-	3705-B1	-	-	-	NO SWITCHES
1	1	-	-	3705-B1	3705-A4	-	-	1
1	1	2	-	3705-B1	3705-A4	3706-A4	-	2
1	1	3	-	3705-B1	3705-A4	3706-A4	-	3
1	2	-	-	3705-B1	3705-A4	-	-	1
1	2	2	-	3705-B1	3705-A4	3706-A4	-	2
1	2	3	-	3705-B1	3705-A4	3706-A4	-	3
1	3	-	-	3705-B1	3705-A4	-	-	4
1	3	2	-	3705-B1	3705-A4	3706-A4	-	5
1	3	3	-	3705-B1	3705-A4	3706-A4	-	6
1	4	-	-	3705-B1	3705-A4	-	-	1
1	4	2	-	3705-B1	3705-A4	3706-A4	-	2
1	4	3	-	3705-B1	3705-A4	3706-A4	-	3
1	4	4	-	3705-B1	3705-A4	3706-A4	-	2
1	4	4	4	3705-B1	3705-A4	3706-B4	3706-A4	9

Channel Adapter Combinations - No Remote Program Loader								
CA #1 TYPE	CA #2 TYPE	CA #3 TYPE	CA #4 TYPE	BOARD LOCATIONS				CONTROL PANEL TYPE
				CA #1	CA #2	CA #3	CA #4	
1	-	-	-	3705-A4	-	-	-	1
1	2	-	-	3705-A4	3706-A4	-	-	2
1	3	-	-	3705-A4	3706-A4	-	-	3
2	-	-	-	3705-A4	-	-	-	1
2	2	-	-	3705-A4	3706-A4	-	-	2
2	3	-	-	3705-A4	3706-A4	-	-	3
3	-	-	-	3705-A4	-	-	-	4
3	2	-	-	3705-A4	3706-A4	-	-	5
3	3	-	-	3705-A4	3706-A4	-	-	6
4	-	-	-	3705-A4	-	-	-	1
4	2	-	-	3705-B1	3705-A4	-	-	7
				OR				
				3705-A4	3706-A4	-	-	2
4	3	-	-	3705-A4	3706-A4	-	-	3
4	4	-	-	3705-B1	3705-A4	-	-	7
				OR				
				3705-A4	3706-A4	-	-	2
4	4	4	-	3705-B1	3705-A4	3706-A4	-	8
				OR				
				3705-A4	3706-B4	3706-A4	-	9
4	4	4	4	3705-B1	3705-A4	3706-B4	3706-A4	10

CONTROL PANEL CONFIGURATIONS



- NOTES:
1. The IPL source switch is installed only for two type 4 CAs with a CA1 ROS.
 2. The IPL source switch may already be installed in this location on some machines.
 3. Switches and indicators in the left column are for CAs in the basic frame.
 4. Switches and indicators in the right column are for CAs in the expansion frame.

TYPE 3 OR 3HS COMMUNICATION SCANNERS

INTRODUCTION

Similarities of Type 2, Type 3, or Type 3HS Scanners (See Notes).

- Structure and Architecture
- First five bytes of the ICW
- Input-Output for X'40'-X'47'
- Autocall operation (see B-090)
- Interface attachment (input/output, CSB common, LIBs).
- Level 2 interrupt operation (see B-300)
- Program addressing (see B-290).

The type 3 communication scanner provides the interface between the line attachment hardware (line or autocall interfaces) and the CCU. The primary function of the scanner is to monitor the communication lines for service requests. Four type 3 or type 3HS scanners may be installed in the 3705-II and three type 3 scanners may be installed in the 3705-I expansion frames (none in the basic frame). Each scanner supports synchronous half-duplex and duplex lines operating at various line speeds. For each line interface, the control program initializes the line type (BSC, SDLC, autocall), character length, type of bit clocking (business machine or modem), bit clocking speed for business machine clocking, and interrupt priority.

Functions of the Type 3 and Type 3HS Scanners (See Notes).

The scanner:

- Scans the line/autocall interface addresses in the LIB positions it supports.
- Performs character assembly/disassembly
- Provides character buffering
- Signals program level 2 interrupts to the attachment base when program service is required.
- Provides bit clock addresses for the LIB positions it supports so the LIB can generate the strobe pulse for receive operations.
- Provides up to four oscillators that generate business machine transmit and receive pulses for use by the line/autocall interfaces.
- Signals program level 1 interrupts for failures in the scanner, LIB, and line/autocall interface. The cause of the level 1 interrupt is buffered in the check register.
- Monitors the state of certain carrier equipment and autocall unit lines for interfaces that are selected by the control program and buffers the state in the display register where the program may display it on the control panel.
- Performs Control Character Decode.
- Cycle-steals data to and from main storage.
- Maintains CS storage address and byte count.
- Translates USASCII to EBCDIC and EBCDIC to USASCII.
- Monitors data for line control characters.
- Performs modem interface control.
- Performs cycle steal count update.
- Performs block check character accumulation.

Notes:

1. Autocall, address substitution, upper scan limit, and high-speed select are not used by the type 3HS scanners.
2. The type 3HS scanner allows only two line interface addresses and attaches to a LIB1 only.

Type 2 Attachment Base (See Notes).

The type 2 attachment base provides common interface controls to the central control unit and line addressing controls for the type 3 or type 3HS scanner and is contained on two cards located at A-B3D2 and A-B3E2 (see F-020).

The attachment base:

- Generates line interface addresses for all type 3 or type 3HS scanners for scan addressing
- Performs address substitution under program control
- Provides a buffer for the interface address for program addressing
- Provides the mechanism for buffering program level 2 interrupts by priority.

Scanner Initialization

The scanner and its associated LIBs are placed in a disabled state (1) during a power-on sequence, (2) during an IPL, (3) by a control panel reset, or (4) during the execution of an Output X'43' when the general register specified by the R field contains appropriate bits. The control program must

enable each scanner by executing Output X'43' with bits 0.1 = 1 and 1.6 = 1 before the control program can initialize each ICW (interface control word) and the associated line or autocall interface. This initialization must occur before the line interface can be placed in operation.

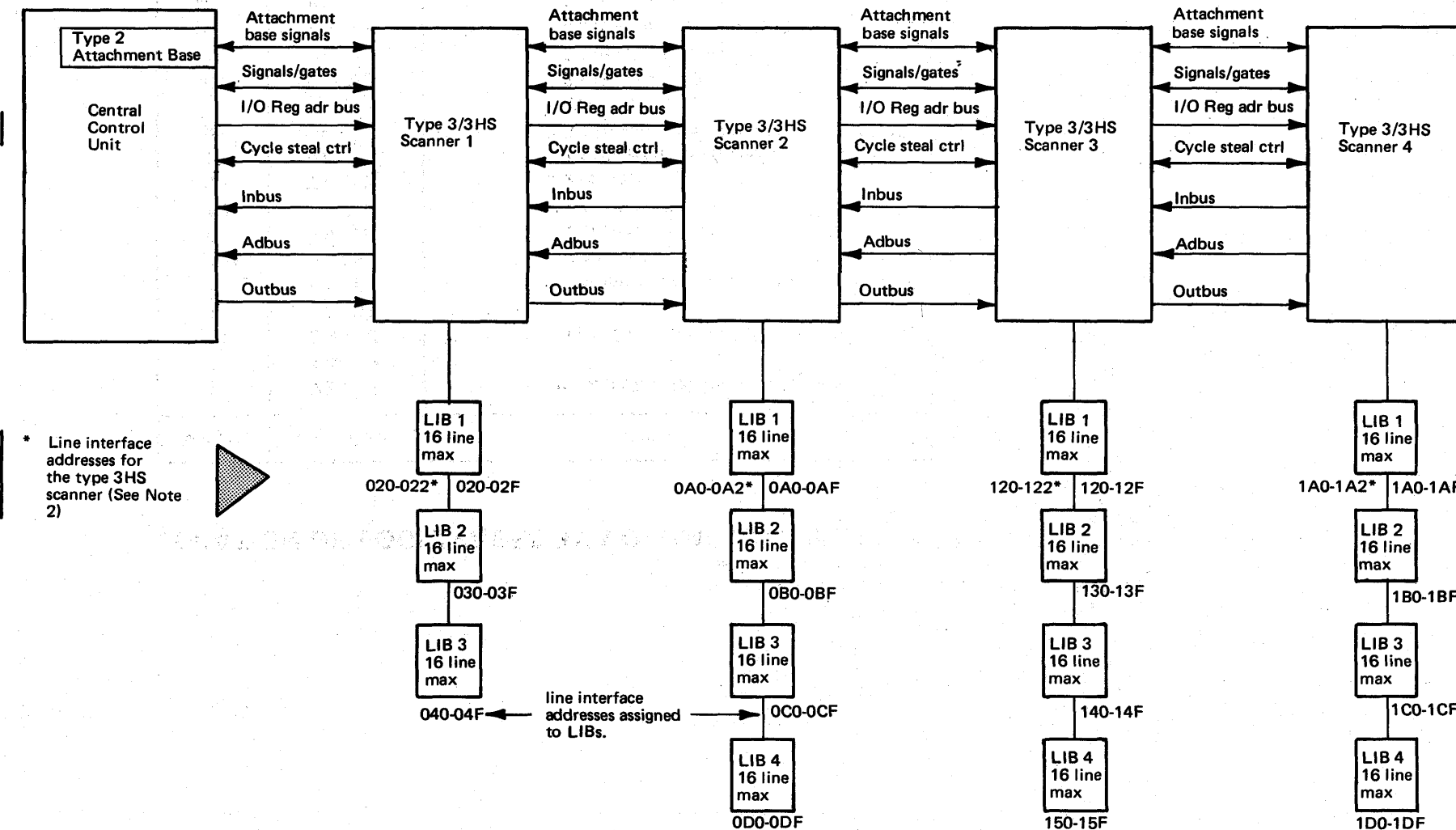
Interface Control Word (See Notes).

The ICW provides the normal communications link between the control program and the scanner, and between the control program and the interface hardware. The scanner contains 64 ICWs, one for each of the line/autocall interfaces that may be attached (see Note 2). Certain fields within the ICW are used to buffer information about the interface between successive scans.

The ICW:

- Serializes the character to be transmitted
- Deserializes the received character
- Buffers the autocall digit
- Buffers the mode of operation
- Buffers the status of the operation
- Is used to initialize the line interface hardware and the scanner operation for that interface.
- Buffers Cycle Steal Addresses
- Buffers bcc
- Buffers PDF Array Pointers
- Buffers Line Control Data

TYPE 3 or 3HS SCANNER CONFIGURATION FOR 3705-II



TYPE 3 OR TYPE 3HS COMMUNICATION SCANNER INTRODUCTION, PART 2

Program Addressing

The control program accesses the ICW or scanner during that part of the scanner cycle called CCU time. During CCU time, the scanner implements the input and output instructions (see Input/Output section) that apply to that scanner. During this time, the interface address in ABAR (attachment buffer address register) accesses the associated ICW and selects the scanner. The control program executes input instructions to obtain the status of this ICW, or executes output instructions to change the contents of this ICW.

The control program also executes input instructions to obtain (1) the interface address in ABAR, (2) the status of the check register, and (3) the status of the display register.

The control program also executes output instructions to (1) set the interface address in ABAR, (2) set the state of the substitution control register, (3) set the state of the upper scan limit latches in the selected scanner, (4) enable or disable a LIB or scanner, (5) set or reset the scanner control functions, or (6) set high speed select.

Note: Items 2, 3, and 6 are not applicable to type 3HS scanner operations.

Since program addressing is similar to that in the type 2 scanner it is not included in this section. See B-290 for program addressing details.

Scan Addressing (See Notes).

Each scanner services the line/autocall interface during that part of the scanner cycle called CSB time. During CSB time, the scan counter in the attachment base provides an interface address to all scanners in parallel to be used by each scanner for scan addressing. Each scanner uses this interface address to access the corresponding line/autocall interface and the associated ICW. The scanner receives the status of the line/autocall interface and determines if a bit service request is active. If a request is active, the scanner, under control of the primary control field in the ICW, performs the bit service operation and updates the ICW content. The scanner signals a character service level 2 interrupt when appropriate. If the scanner does not detect a bit service request, the bit service operation does not occur.

The scan counter furnishes 96 discrete interface addresses to all scanners in parallel even though the type 3 scanner can attach only up to 64 line sets, (the type 3HS scanner attaches to two 1GA line sets or a single 1TA line set only—see Notes). The address substitution mechanism in the attachment base can modify certain addresses before they are sent to the scanners. Each scanner contains an upper scan limit mechanism and a high speed select mechanism for modifying the interface address received from the attachment base. Modification only occurs during scan addressing. Address substitution and upper scan limit modification are both under control of the program.

Notes:

1. Autocall, address substitution, upper scan limit, and high-speed select are not used by the type 3HS scanner.
2. The type 3HS scanner allows only two line interface addresses and attaches to a LIB1 only.

Cycle Steal

The type 3 or type 3HS scanner can steal cycles from the CCU under control of certain fields in the ICW. The cycle steals are used to store data in or fetch data from main storage.

Level 1 Interrupts

Failures in the scanner can affect all communication lines attached to the 3705, or can affect at least a group of lines within a particular LIB. The detection of one or more of the failures is indicated by a scanner level 1 interrupt request. Each scanner contains a check register which buffers the condition that causes the level 1 interrupt.

Transmit Operation

The program initializes the operation by assigning a beginning storage address and byte count in the line interface ICW. The scanner then performs cycle steals to fetch data from main storage and place it in the PDF array. The first character to be transmitted is transferred from the PDF array to the SDF (serial data field).

The control program indicates in the ICW the type of line control to use. The scanner implements the line control (such as initial SYN and PAD, and response characters). After all the data has been transmitted the scanner sends the ending character or sequence and then causes a program level 2 interrupt. The SDF serializes the character and sends it to the line interface a bit at a time under control of the bit service request from the line interface. The line interface then sends the bits to the modem or transmission line under control of the transmit oscillator located in the scanner or external clock in the modem.

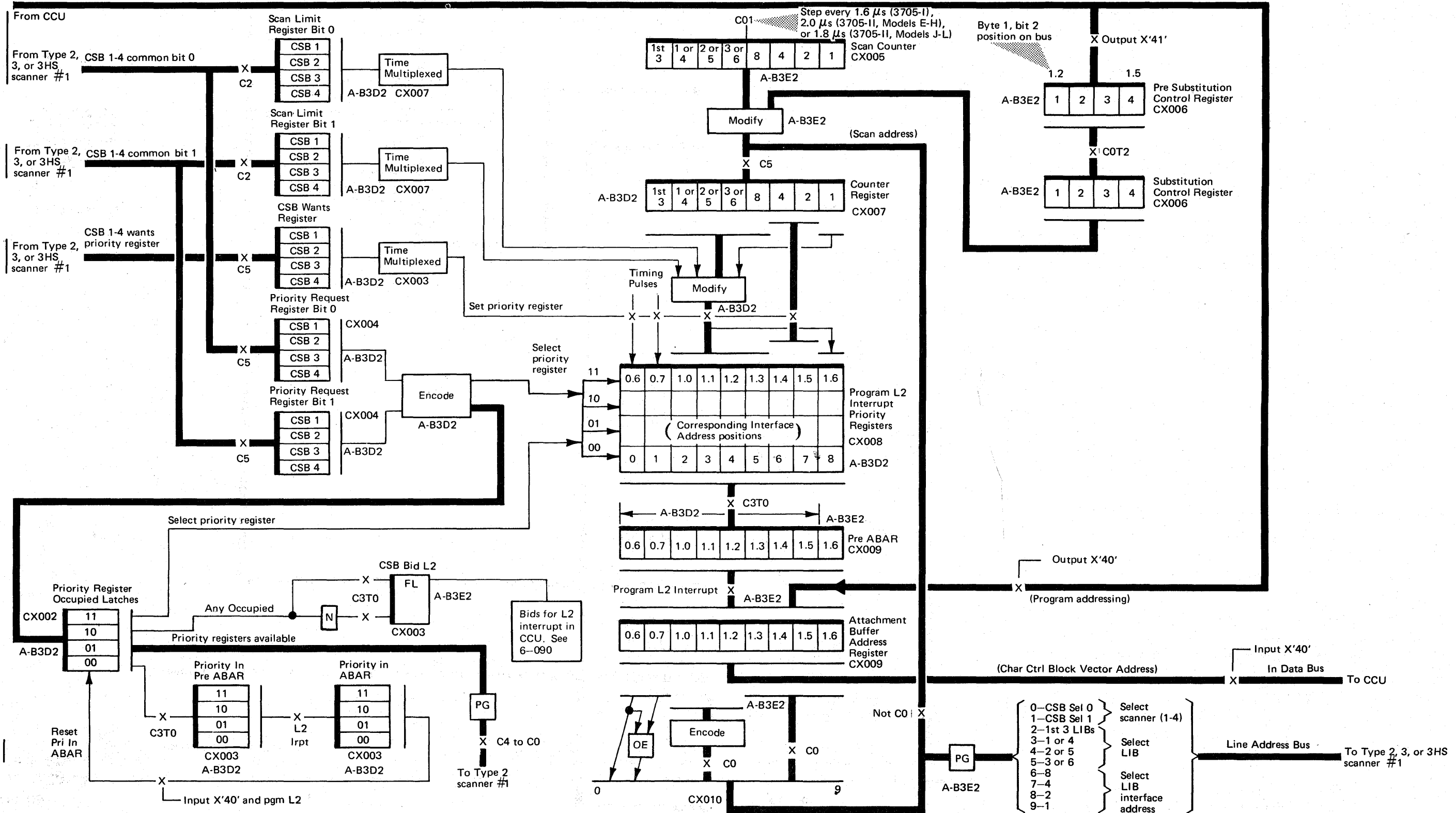
Receive Operation

The line interface receives the bits from the modem or transmission line. The line interface strobes the bits into its receive buffer. The strobe is under control of the bit clock control (located in the LIB) for business machine clocking. The scanner contains the receive oscillator that controls the bit clock circuit in the LIB. The modem receive clock pulses generate the strobe pulses when external clocking is specified by the control program for synchronous operation. In either case, the strobe generates a bit service request in the line interface which signals the scanner that the receive buffer contains the received bit. The scanner places the bits into the SDF until a character has been assembled and then transfers the character to the PDF array. The scanner will use cycle steal to store the received character from the PDF array to main storage two characters at a time if the cycle steal address is on an even boundary. The scanner determines when an ending character or sequence has been received and then causes a program level 2 interrupt.

TYPE 2 ATTACHMENT BASE DATA FLOW

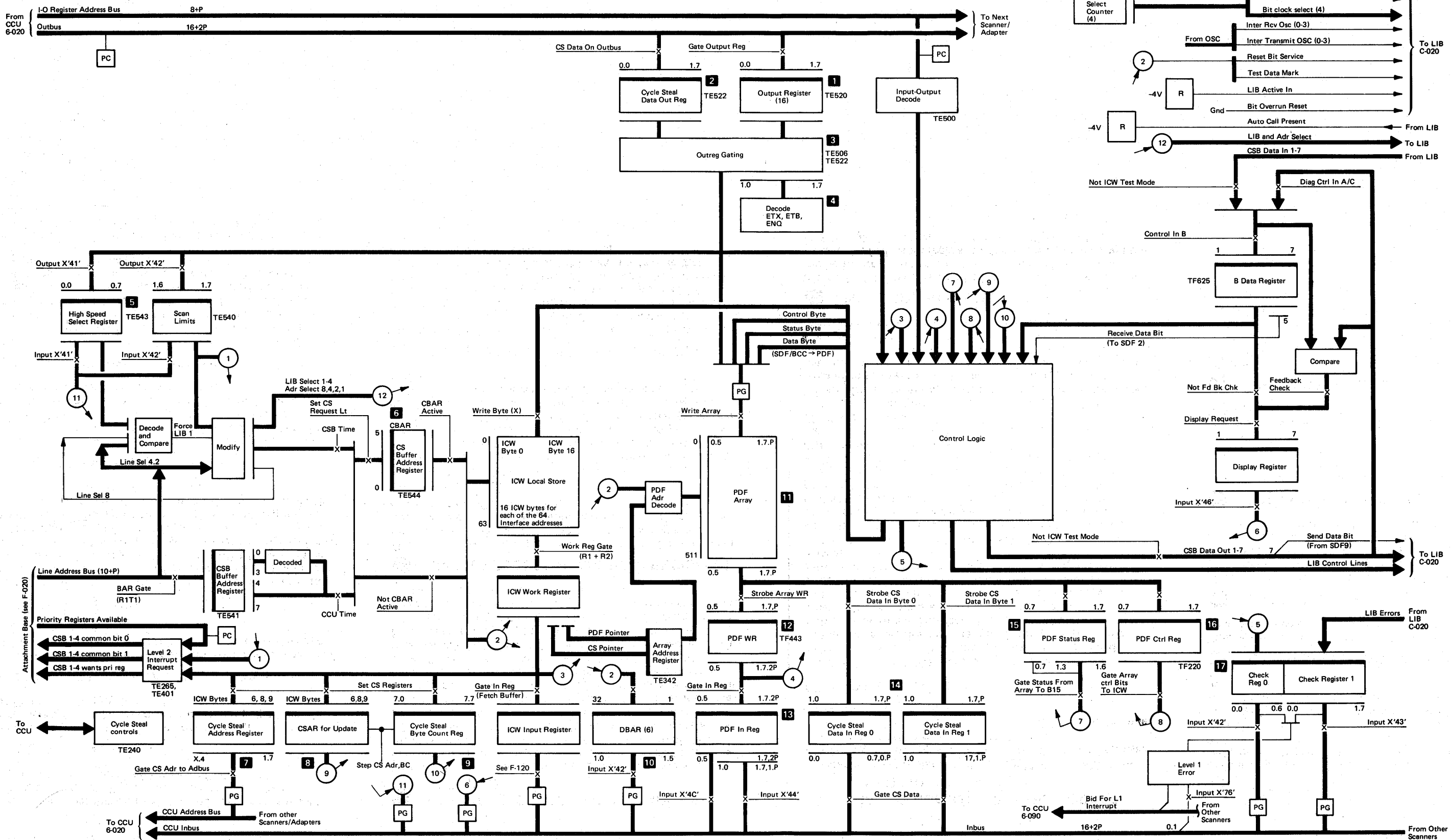
The logic for the attachment base is located on two MST cards A-B3D2 and A-B3E2. The logic is distributed between the cards as indicated on this page.

Z Bus



SCANNER DATA FLOW

(See Note)



Note: The scanner data flow description on Page F-040 notes the differences in type 3 and type 3HS scanner operation.

TYPE 3 OR TYPE 3HS SCANNER DATA FLOW DESCRIPTION

This page describes those data flow components that are used on the type 3 or type 3HS scanner and not on the type 2 scanner. The key symbols refer to Page F-030.

1 OUTPUT REGISTER

The output register buffers the data from a specified general register that the CCU places on the outbus during the execution of an Output X'4X' type instruction.

2 CYCLE STEAL DATA OUT REGISTER

This register buffers the halfword of data from main storage that the CCU places on the outbus during a transmit cycle-steal operation (see F-360).

3 OUTREG GATING

The "outreg gating" logic gates part/or all of the output register contents directly/or offset to its destination by means of (1) outreg bus 0.0-0.7, (2) outreg bus 1.0-1.7, and (3) alternate outreg bus A.0-A.7, depending on the output instruction (see F-280 for a typical gating example). The "outreg gating" logic also gates data byte 0 then data byte 1 from the 'CS data out register' to the PDF array by means of outreg bus 1.0-1.7 during a transmit cycle-steal operation (see F-360).

4 DECODE END CHARACTERS

When the scanner detects an ETX, ETB, or ENQ character on outreg bus 1.0-1.7 during a BSC transmit cycle-steal data fetch, the scanner stops the cycle-steal operation, transmits the end character, the BCC, and Pad characters, turns the line around and requests a level 2 interrupt (see F-400).

5 HIGH SPEED SELECT REGISTER

Each scanner has a HS select register that allows address substitution to be performed on a scanner basis. The scanner substitutes the even-numbered address in that scanner's LIB 1 for all scan counter line addresses that contain the even/odd-numbered selected lines that are associated with a position in the HS select register that contains a 1. See Page F-090 for scan addressing using high speed select.

Note: Autocall, address substitution, upper scan limit, and high-speed select options are not used by the type 3HS scanner.

6 CBAR (CYCLE STEAL BUFFER ADDRESS REGISTER)

This register is used during cycle-steal operations to buffer the selected ICW address for use during a following CCU time since the cycle stealing is done asynchronous with 'gated bit service' CSB time. At the first available CCU time following the cycle-steal machine cycle for a *transmit* cycle steal, the address in CBAR (1) selects the PDF array in which the scanner loads the two data bytes and (2) selects the ICW so the scanner can write the updated CS byte count, the updated CSAR and the regenerated CS valid bit into the correct ICW (see F-360). At the first available CCU time following the cycle-steal machine cycle for a *receive* cycle-steal, the address in CBAR selects the ICW so the scanner can write the updated CS and PDF pointers, the updated CSAR, the updated CS byte count, and the regenerated CS valid bit into the correct ICW (see F-450).

7 CSAR (CYCLE STEAL ADDRESS REGISTER)

The scanner loads this register with the current address of main storage where data is to be stored or fetched during a cycle-steal operation. The current address comes from ICW bytes 6, 8, and 9 (see F-360 and F-450).

8 CSAR FOR UPDATE

The scanner loads the same address in this register as it loaded into CSAR. On a *transmit* cycle-steal operation, the scanner increments the address in this register each time a data byte is loaded into the PDF array (see F-360). On a *receive* cycle-steal operation the scanner increments the address in this register each time a data byte is set in the 'CS data in register' (see F-450).

9 CYCLE STEAL BYTE COUNT REGISTER

The scanner loads this register with the current CS byte count from ICW byte 7 at the same time CSAR is loaded. On a *transmit* cycle-steal operation, the scanner decrements the CS byte count for each data byte that is loaded into the PDF array (see F-360). On a *receive* cycle-steal operation, the scanner decrements the CS byte count for each data byte that is set in the 'CS data in register' (see F-450).

10 DBAR (DIAGNOSTIC BUFFER ADDRESS REGISTER)

The scanner sets the status of the actual ICW addressing lines into this register whenever a bid for a level 1 interrupt is caused by the scanner detecting a 'work register or array error' (TE706). The level 1 program then inputs DBAR to determine the failing line (see F-190).

11 PDF ARRAY

The type 3 scanner PDF array contains 512 addressable buffers 12 bits in length (11 bits + parity). Each of the 64 ICW addresses provided by the type 3 scanner is associated with an array of eight buffers. The type 3HS scanner provides 2 ICW addresses and each address is associated with an array of 16 buffers. Each array therefore provides character buffering for a maximum of eight characters with a type 3 scanner and 16 characters with a type 3HS scanner.

The ICW addressing lines that select the ICW local store also select the associated PDF array (see F-390). Selecting one of the eight or 16 buffers is accomplished by means of the 'array address register' that is set by either the PDF pointer or the CS pointer. The PDF and CS pointers for a type 3 scanner are in ICW byte 12 only, and the pointers for a type 3HS scanner are in ICW bytes 12 and 17. The PDF pointer can not be used when the CS pointer is being used and vice versa. See Page F-390 for a summary of CS/PDF pointer use.

The PDF array buffers data, control, and status bytes (see F-490). On a *transmit* cycle-steal operation, data is transferred from main storage to the PDF array. The data is buffered until the scanner transfers it to the SDF where the data is serialized for transmission (see F-360). Received data is transferred from the SDF to the PDF array and a *receive* cycle-steal operation transfers the data to main storage (see F-450).

12 PDF WORK REGISTER

When a PDF buffer is selected by the PDF pointer for read out (no 'write array'), the contents of the selected PDF buffer is set into the PDF work register so that the control logic and the PDF in register have access to it (see F-410 and F-440).

13 PDF IN REGISTER

During a 'fetch buffer' (level 2 interrupt or an Output X'40' while in level 3 or level 4), the scanner sets the contents of the PDF work register into the 'PDF in register' while also setting the contents of the ICW local store into the 'ICW input register' (see F-250). The 3705 control program now has access to the status of the ICW and PDF array as they were at the time of the 'fetch buffer'.

14 CYCLE STEAL DATA IN REGISTER

This register buffers the data to be transferred to main storage by a receive cycle-steal operation (see F-450).

15 PDF STATUS REGISTER

When a PDF buffer is selected by the CS pointer for read out (no 'write array') and the PDF buffer contains a status byte (PDF bits 0.5 and 0.6 = 11), the scanner sets the status byte into the PDF status register (see F-480 and F-490). The scanner uses the contents of this register to set ICW byte 15.

16 PDF CONTROL REGISTER

When a PDF buffer is selected by the CS pointer for read out (no 'write array') and the PDF buffer contains a control byte (PDF bits 0.5 and 0.6 = 10), the scanner sets the control byte into the PDF control register (see F-480 and F-490). The scanner uses the contents of the PDF control register to set bits in ICW bytes 0 and 14.

17 CHECK REGISTER 0

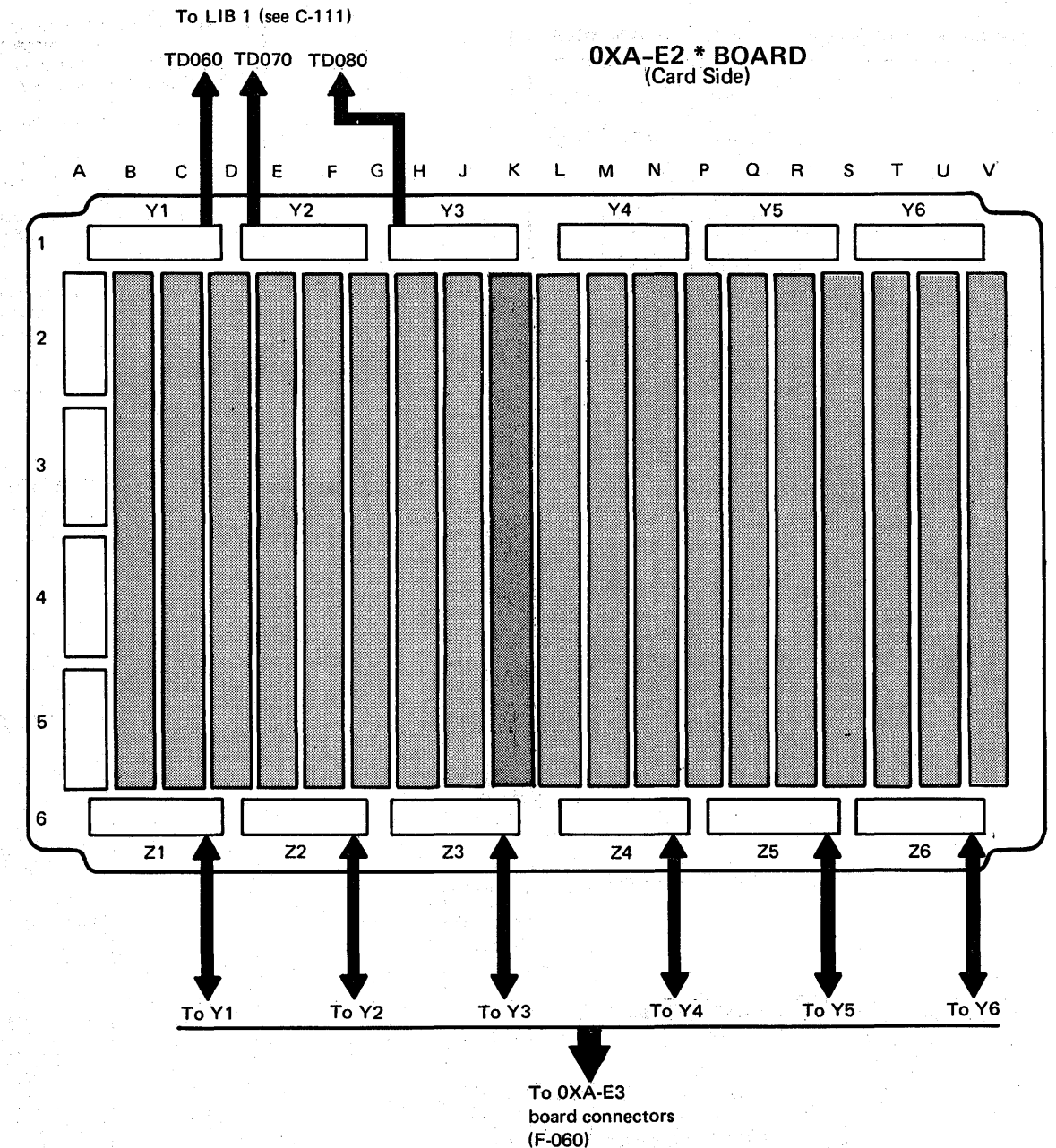
When the scanner detects an ICW work register check for any bytes other than 0, 2, 10, or 14, or a PDF array check, the scanner sets a corresponding bit in check register 0 and then requests a level 1 interrupt. Check register 0 expands the check register function of check register 1.

COMMUNICATION SCANNER BOARD 0XA-E2 LAYOUT

The type 3 scanner occupies two board locations; 0XA-E2 and 0XA-E3

Card Loc	ALD Page	Function
E2T2	TF200	ICW byte 0 and 14-input gates, input registers, work registers, and local store arrays.
	TF205	
E2S2	TF210	ICW byte 15 and 16-input gates, input registers, work registers, and local store arrays.
	TF215	
E2N2	TF220	PDF control register, PDF status register
	TF221	SCF update
	TF222	ICW byte 14 update
E2U2	TF300	ICW byte 2 and 10-input gates, input registers, work registers, and local store arrays.
	TF305	
E2M2	TF310	ICW byte 5 and 11-input gates, input registers, work registers, and local store arrays.
	TF315	
E2R2	TF320	New EPCF state 0
	TF321	Set new EPCF states 1 and 3
	TF322	Set new EPCF state 2
	TF323	Set EPCF state 4
	TF324	Set EPCF state 5, 6
	TF325	New EPCF states 6, 7, 8
	TF326	Rec and Xmit conditions
	TF327	New ICW Bits 16.6 and 16.7
	TF328	New ICW bits 16.4 and 16.5
	TF329	ICW bits 16.4-16.7, EPCF state c
	TF360	Set EPCF 0 BSC receive
	TF361	Set EPCF 0 SDLC receive
	TF364	Set EPCF state 4 receive
	TF365	Set EPCF state 5 receive
	TF368	ICW write pulse generation
E2Q2	TF340	ICW byte 15 control
	TF344	
E2G2	TF400	ICW byte 3 and 13-input gates, input registers, work registers, and local store arrays.
	TF405	
E2V2	TF410	ICW byte 4 and 12-input gates, input registers, work registers, and local store arrays.
	TF415	
E2H2	TF420	SDF to PDF bits 0-2
	TF421	SDF to PDF bits 3-7
	TF422	New SDF bits 0-4 and tag time
	TF423	New SDF bits 5-9
	TF424	CSB LIB data out bus
	TF426	New CSB bits to array

Card Loc	ALD Page	Function
E2K2	TF440	Control character ROS address assembly
	TF441	Character decode encode ROS
	TF442	EBCDIC to USASCII translate ROS
	TF443	PDF work reg array parity check
	TF444	PDF to SDF and BCC gates
	TF445	ROS char decode reg-PDF work reg control
	TF446	PDF In register
E2L2	TF461	Old BCC input selection
	TF462	Data select and LRC generation
	TF463	CRC generation
	TF464	New BCC (ICW byte 10)
	TF465	New BCC (ICW byte 11)
	TF466	BCC character compare
	TF467	BCC controls and gating
E2F2	TF480	PDF array pointer control (ICW byte 12)
	TF485	Generate SDLC flag X'00' and X'07'
	TF486	Generates X'55' or X'FF'-BSC final status to array
	TF487	New ICW 13.2, 13.4, 13.5-reset byte 12
	TF488	New and old EPCF decode inverters
E2J2	TF500	Inverters
	TF501	LCD state decodes regen of LCD (ICW byte 2)
	TF502	Interrupt go-set PCF state 0 or 4
	TF503	Set PDF 5 or 6
	TF504	Set PCF 7
	TF505	New PCF states-PCF decode
	TF506	SDF transfer
E2C2	TF600	Inverters and terminators
	TF601	CSB data out 7-test data latch
	TF602	Receive data bit-last line state
	TF603	SDLC BSC Counter (ICW byte 4)
	TF604	Bit service reset
	TF605	SDLC BSC counter control (ICW byte 4)
	TF606	Regen output 47
	TF607	ICW Byte 5 regen
E2D2	TF620	Feedback check
	TF621	CSB data in gating
	TF622	Display bus gate
	TF623	Display reg and gating to inbus
	TF624	Scanner diagnostic line wrap simulator
	TF625	B data register
	TF626	Control out and control in latches
E2E2	TF800	Inverters
	TF801	New ICW bits 13.6, 13.7-misc ctrls
	TF802	Set/reset ICW bit 13.0 (seq 0)
	TF803	Set/reset ICW bit 13.1 (seq 1)
	TF804	EPCF decodes
	TF805	Set PDF control bits 0,1,2,4,7 and cycle steal message count controls
	TF806	Set PDF ctl 10, set L2 go, set BSC EOM
	TF807	PDF Array inbus gating
E2B2	TF810	Inverters
	TF811	EPCF decodes and update BCC
	TF812	Write SDF to PDF
	TF813	Transfer PDF to SDF-set timeouts
	TF814	Control character combinations
	TF815	Generate transmit SYN and DLE
	TF816	Gate data check and set array bits 6 and 9, set EPCF 8



Card Loc	ALD Page	Function
E2P2	TF820	Set ICW bits 5.4 and set DLE response character state
	TF821	Misc controls
	TF822	Initial and final status
	TF823	ICW byte 15 work register control
	TF824	Set L2 on the fly
	TF825	Inverters and EPCF decodes
	TF826	Set 14.1, 14.7 VRC
	TF827	BCC to SDF transfer
	TF828	New Sync (ICW 16.0)
	TF829	Set array status

Indicates card location

*E2 is the psuedo board location for half of the type 3 scanner. The actual board location is 0XA-B2

Cards G2, M2, S2, T2, U2, and V2 can be swapped on this board

COMMUNICATION SCANNER BOARD 0XA-E3 LAYOUT

0XA-E3* BOARD
(CARD SIDE - See Notes 1 and 2)

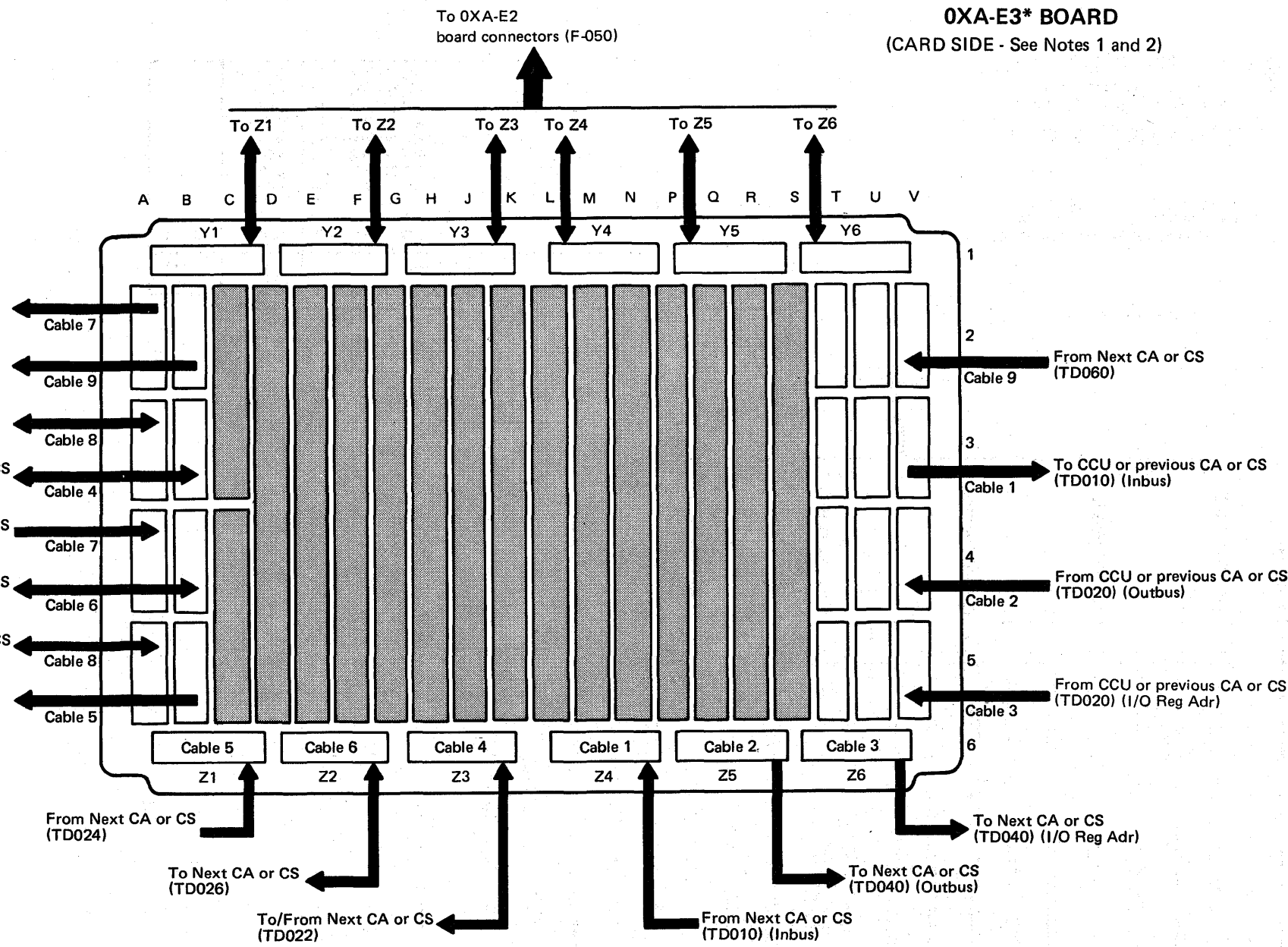
Card Loc	ALD Page	Function
E3F2	TE200	ICW byte 6 and 8-input gates, input registers, work registers, and local store array.
	TE205	
E3G2	TE210	ICW byte 7 and 9-input gates, input registers, work registers, and local store array.
	TE215	
E3J2	TE220	Cycle steal address update Cycle steal address and byte count update Cycle steal address register byte 0 Cycle steal address register byte 1 Cycle steal address register byte X Work register byte count equals 0
	TE221	
	TE222	
	TE223	
	TE224	
E3K2	TE240	Cycle steal controls Cycle steal controls Cycle steal data register byte 0 Cycle steal data register byte 1
	TE241	
	TE242	
	TE243	
E3R2	TE260	Inbus byte 0 Inbus byte 1 Bit clock drive Inbus parity check and parity generation Identify CBS level 1 Priority reg available
	TE261	
	TE262	
	TE263	
	TE264	
	TE265	
E3N2	TE300	PDF array row selection Array address drivers PDF array buffers for LIB 2 lines 0-3 PDF array buffers for LIB 2 lines 4-7 PDF array buffers for LIB 2 lines 8-B PDF array buffers for LIB 3 lines 8-B PDF array buffers for LIB 3 lines C-F PDF array buffers for LIB 2 lines C-F Array bits 0 thru 5 out Array bits 6 thru P out Array pointer bits and pointer comparison Array pointer bits and pointer comparison ICW extension bits
	TE301	
	TE302	
	TE303	
	TE304	
	TE305	
	TE306	
	TE307	
	TE308	
	TE309	
	TE350	
	TE351	
	TE352	
	E3P2 (Note 3)	
TE311		
TE312		
TE313		
TE314		
TE315		
TE316		
TE317		
TE318		
TE319		
E3M2	TE320	PDF array row select Array address drivers PDF array buffers for LIB 1 lines 0-3 PDF array buffers for LIB 1 lines 4-7 PDF array buffers for LIB 1 lines 8-B PDF array buffers for LIB 1 lines C-F Array bits 0 thru 5 in and parity gen Array bits 6 thru 10 in Array bits 0 thru 5 out Array bits 6 thru P out
	TE321	
	TE322	
	TE323	
	TE324	
	TE325	
	TE326	
	TE327	
	TE328	
	TE329	
E3D2	TE340	Array timings Cycle steal request Array pointer bits and pointer comparison Array write gating and regen of bit 6.5 Pointer selection Write array and step pointer Array full-array empty-override
	TE341	
	TE342	
	TE343	
	TE344	
	TE345	
	TE346	

Card F2 can be swapped with G2
Card N2 can be swapped with P2
(see Note 3).

Indicates card location

Card Loc	ALD Page	Function
E3L2	TE400	ICW write timings Level 2 interrupt CSB clock T pulse decode Drivers Drivers
	TE401	
	TE402	
	TE403	
	TE404	
E3S2	TE500	I/O decodes Input decode Output decode Parity sample gates ICW write pulse generation Output 77 sync lth-BSC timer ctrl Outreg bus gating
	TE501	
	TE502	
	TE503	
	TE504	
	TE505	
	TE506	

- Notes:**
- E3 is the psuedo board location for half of the scanner. The actual board location is 0XA-A3.
 - Internal board connections exist between the sockets for similar cable numbers. For example, socket A2 is wired to socket A4 for cable 7.
 - Card location E3P2 is blank in any 3705 frame that contains a type 3HS scanner.

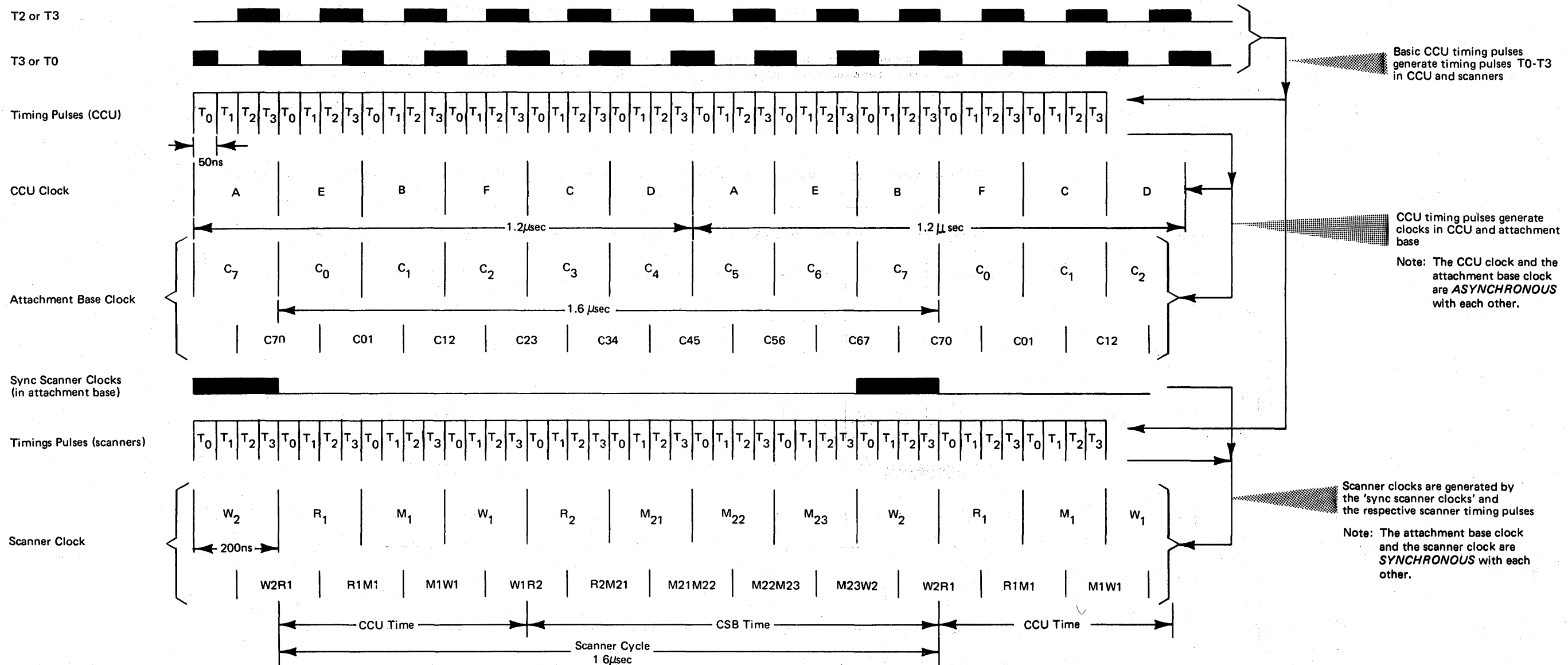


Card Loc	ALD Page	Function		
E3Q2	TE502	Outreg byte 0 and outbus parity check Outreg byte 1 and outbus parity check CS data buf byte 0-outreg bus gating 1.0, 1.1 CS data buf byte 1-outreg bus gating 1.2, 1.3 Outreg bus gating bits 1.4-1.7 Outreg bus gating byte 0-regen ICW bits 16.2 and 16.3 Outreg gating alternate bus A.0-A.7 ETB, ETX, ENQ decodes for ASCII-EBCDIC		
	TE521			
	TE522			
	TE523			
	TE524			
	TE525			
	TE526			
	TE527			
	E3H2		TE540	Scan limit latch and LIB adr bits 0-3 CSB BAR bits 0-3 and LIB select CSB BAR bits 4-7 and intf adr select High speed select reg and adr modify CBAR and ICW address select Line abbus par chk-forced scan limits
			TE541	
TE542				
TE543				
TE544				

Card Loc	ALD Page	Function
E3E2	TE700	Level 1 error set and reset function ICW work register check and PDF array check LIB select and bit clock errors CSB errors DBAR 42 and 43 input select Bid level 1 Reset functions Inverters
	TE701	
	TE702	
	TE703	
	TE704	
	TE705	
	TE706	
	TE707	
E3C2	TE710	150-600-1200 bps line oscillators
E3C4*	TE720	2000 or 2400 line oscillators

* E3C4 location is blank if a type 3HS scanner is installed.

CLOCK AND TIMINGS – BRIDGE STORAGE



Basic CCU timing pulses generate timing pulses T₀-T₃ in CCU and scanners

CCU timing pulses generate clocks in CCU and attachment base

Note: The CCU clock and the attachment base clock are **ASYNCHRONOUS** with each other.

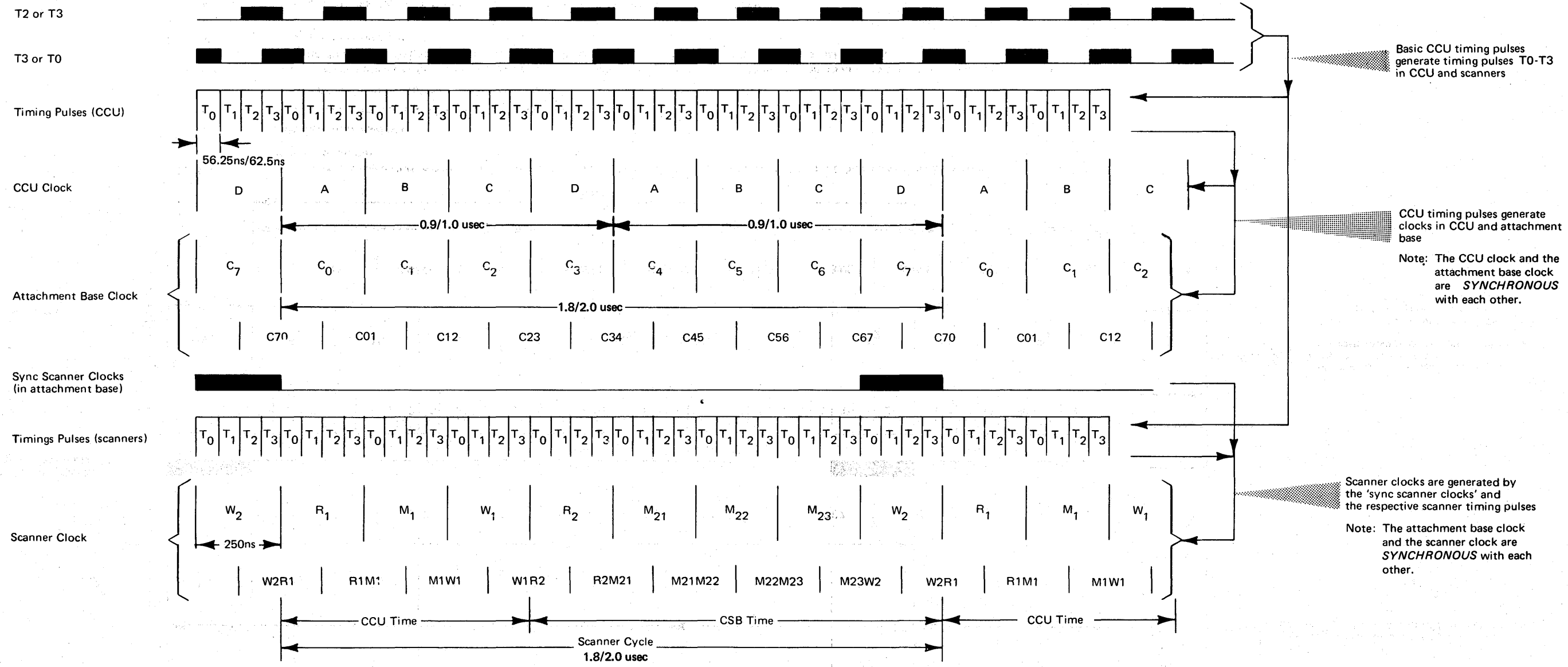
Scanner clocks are generated by the 'sync scanner clocks' and the respective scanner timing pulses

Note: The attachment base clock and the scanner clock are **SYNCHRONOUS** with each other.

- CCU Time - Program addressing occurs as described on F-010 and B-290. ABAR supplies the address of the ICW that the control program wants to input or output.
- R1 - ICW local store read out
- M1 - ICW content modified as required by an Input or Output instruction.
- W1 - Modified ICW contents written into ICW local store
- CSB Time - Scan addressing occurs as described on F-010 and F-100. Each scanner uses the address from the scan counter to determine the state of a line on that scanner and to modify the contents of the associated ICW, if required, if bit service request is active.
- R2 - ICW local store read out
- M21 } - ICW contents modified as required if bit service request is active from the interrogated line.
- M22 }
- M23 }
- W2 - Modified ICW contents written into ICW local store

CLOCK AND TIMINGS – FET STORAGE

Models J-L/E-H



Basic CCU timing pulses generate timing pulses T0-T3 in CCU and scanners

CCU timing pulses generate clocks in CCU and attachment base
 Note: The CCU clock and the attachment base clock are **SYNCHRONOUS** with each other.

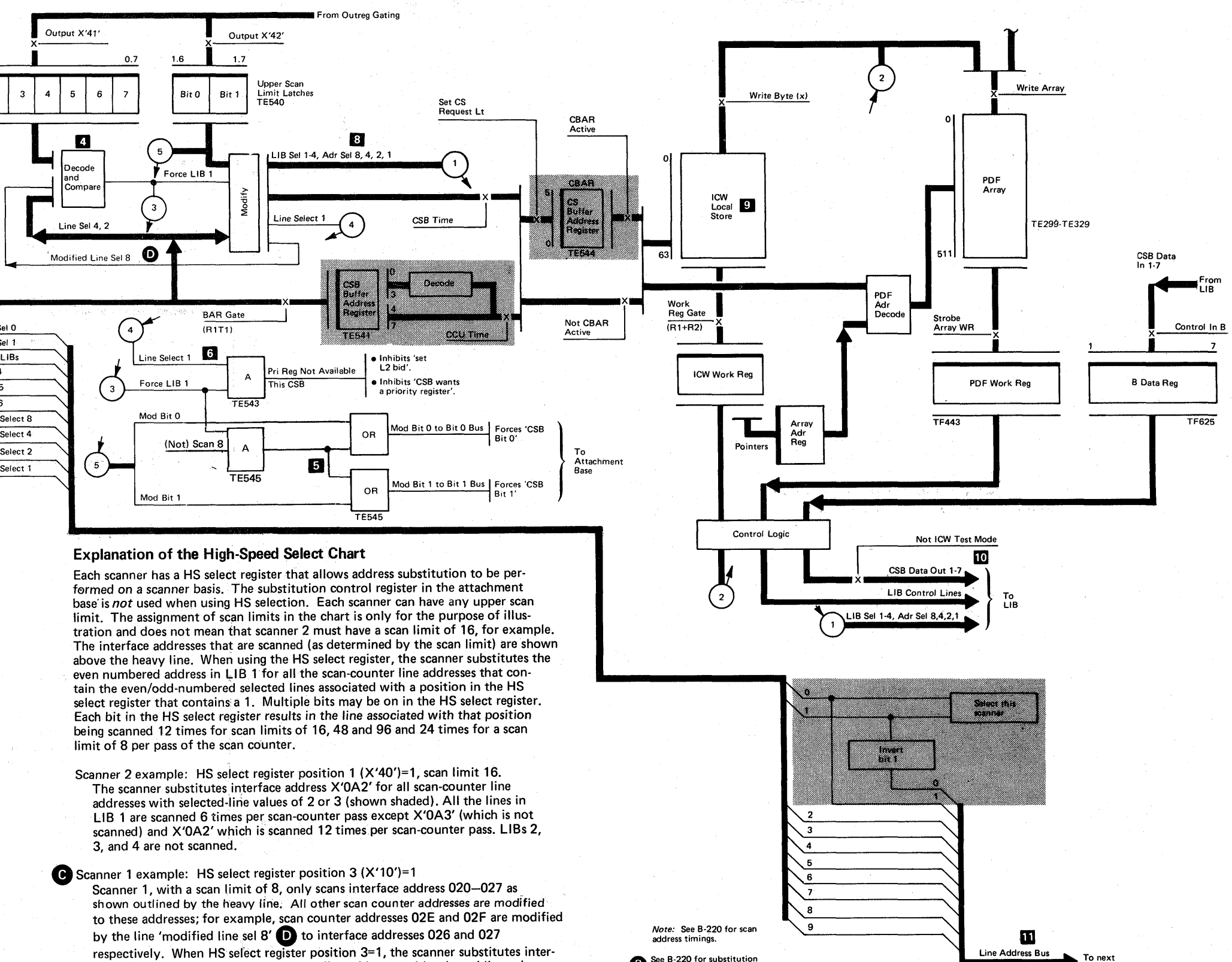
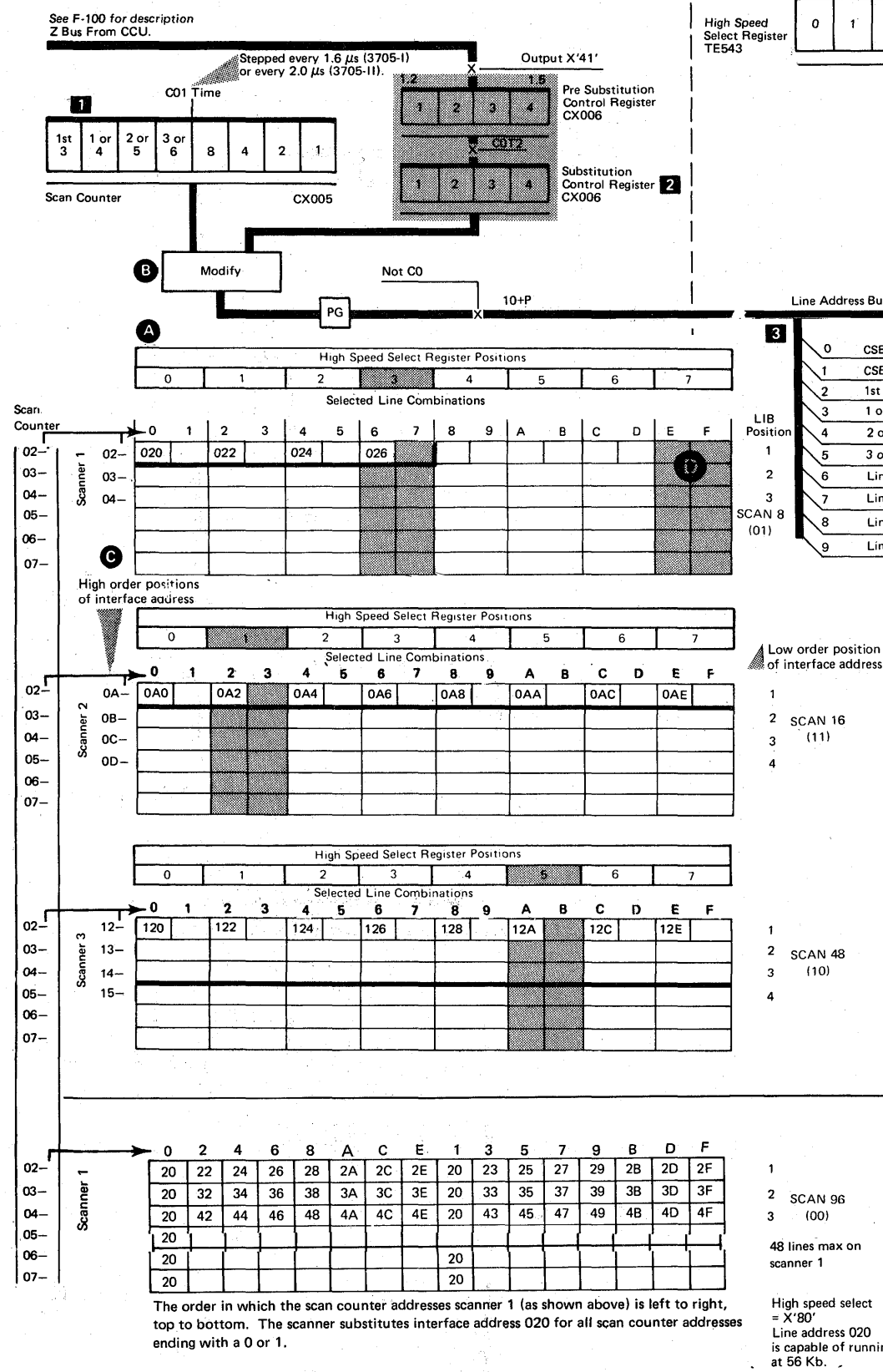
Scanner clocks are generated by the 'sync scanner clocks' and the respective scanner timing pulses
 Note: The attachment base clock and the scanner clock are **SYNCHRONOUS** with each other.

- CCU Time – Program addressing occurs as described on F-010 and B-290. ABAR supplies the address of the ICW that the control program wants to input or output.
- R1 – ICW local store read out
- M1 – ICW content modified as required by an Input or Output instruction.
- W1 – Modified ICW contents written into ICW local store
- CSB Time – Scan addressing occurs as described on F-010 and F-100. Each scanner uses the address from the scan counter to determine the state of a line on that scanner and to modify the contents of the associated ICW, if required, if bit service request is active.
- R2 – ICW local store read out
- M21 } ICW contents modified as required if bit service request is active from the interrogated line.
- M22 }
- M23 }
- W2 – Modified ICW contents written into ICW local store

SCAN ADDRESS DATA FLOW USING HIGH SPEED SELECT

(Not Applicable to Type 3HS Scanners)

ATTACHMENT BASE TYPE 3 SCANNER



Explanation of the High-Speed Select Chart

Each scanner has a HS select register that allows address substitution to be performed on a scanner basis. The substitution control register in the attachment base is *not* used when using HS selection. Each scanner can have any upper scan limit. The assignment of scan limits in the chart is only for the purpose of illustration and does not mean that scanner 2 must have a scan limit of 16, for example. The interface addresses that are scanned (as determined by the scan limit) are shown above the heavy line. When using the HS select register, the scanner substitutes the even numbered address in LIB 1 for all the scan-counter line addresses that contain the even/odd-numbered selected lines associated with a position in the HS select register that contains a 1. Multiple bits may be on in the HS select register. Each bit in the HS select register results in the line associated with that position being scanned 12 times for scan limits of 16, 48 and 96 and 24 times for a scan limit of 8 per pass of the scan counter.

Scanner 2 example: HS select register position 1 (X'40')=1, scan limit 16. The scanner substitutes interface address X'0A2' for all scan-counter line addresses with selected-line values of 2 or 3 (shown shaded). All the lines in LIB 1 are scanned 6 times per scan-counter pass except X'0A3' (which is not scanned) and X'0A2' which is scanned 12 times per scan-counter pass. LIBs 2, 3, and 4 are not scanned.

Scanner 1 example: HS select register position 3 (X'10')=1. Scanner 1, with a scan limit of 8, only scans interface address 020-027 as shown outlined by the heavy line. All other scan counter addresses are modified to these addresses; for example, scan counter addresses 02E and 02F are modified by the line 'modified line sel 8' (D) to interface addresses 026 and 027 respectively. When HS select register position 3=1, the scanner substitutes interface address X'026' for all scan-counter line addresses with selected line values of 6 and 7. These addresses are shown shaded. Line interface addresses X'020', X'021', X'022', X'023', X'024' and X'025' are each scanned 12 times per scan-counter pass. Address X'026' is scanned 24 times per scan-counter pass. Address X'027' and LIBs 2 and 3 are not scanned. HS select register positions 4-7 are not used with scan 8.

SCAN ADDRESSING

Description for F-090. The numbers refer to corresponding numbers on the data flow.

1 Scan Counter

The scan counter runs continuously, stepping through 96 different states. See F-110 for details on the scan counter positions and sequence of interface address outputs. The scan counter steps every 1.6 μ s when used on a 3705-I (see Note 1). Without modification, the scanner can not handle line speeds higher than 4,800 bps without the possibility of undetected bit overrun/underrun conditions.

With a type 3 scanner, three modifications can be made to the scan counter output to allow the scanner to handle line speeds of up to 56,000 bps. These modifications are made in conjunction with the substitution control register, the upper scan limit latches, and the high-speed select register. Address modification, when using the substitution control register, modifies the addresses placed on the line address bus that affects all the scanners. Address modification, when using the high-speed select register in a scanner, modifies the addresses only in that scanner. The substitution control registers should *not* be used when the high-speed select registers are used. The upper scan limits are used with either type of address modification or by themselves since they modify the addresses on a scanner basis. (See Note 2).

2 Address Substitution (Substitution Control Register)

Never used when the high-speed select register is used. See B-230 for the description of scan addressing when using the substitution control register. (See Note 2).

3 Line Address Bus

Ten address bits plus a parity bit are on the line address bus, but for scan addressing, CSB sel 0 and CSB sel 1 are ignored. Parity is generated over the eight bit address on line address bus positions 2-9.

4 Address Substitution (High-Speed Select Register)

The contents of line address bus positions 4, 2 and modified address 8 (scan 8 modifies address 8 as described in the upper scan limit modification chart on this page) is decoded into 1 of 8 selected line even-odd combinations as shown in the chart on F-090 (see Note 2). If a 1 is in the HS select register position corresponding to the decoded selected line combination, the scanner raises 'force LIB 1' to modify the address. This modification forces:

- LIB select 1.
- Address select (x) where x = even address of the decoded selected-line combination
- ICW addressing for LIB 1 and line select (x).

Notes:

1. For the 3705-II, every 2.0 microseconds if the Cycle time is 1.0 microseconds (Models E-H) and every 1.8 microseconds if the cycle time is 900 nanoseconds (Models J-L).
2. Type 3HS scanners attach to a LIB 1 in the 3705-II only. Interface addresses 0 and 2 are the only addresses selected. The address substitution, upper scan limit, and autocal options are not applicable to type 3HS scanner operations.

'Force LIB 1' forces a scan limit of 11 (scan 16) to the attachment base over CSB bits 0 and 1 **5** to enable the attachment base to modify the scan counter output to reflect the fact that an address has been substituted for the one the scan counter is pointing to. This is necessary if the L2 interrupt priority register is to present the same address that caused the L2 interrupt.

If the address on the line address bus was the odd address of the selected line combination, or if line select 8 = 1 for scan 8, the scanner raises 'line select 1' to inhibit setting 'L2 bid' and 'CSB wants a priority register' **6**. This prevents the scan counter that is pointing to the odd address from transferring the wrong address to the L2 interrupt priority register when the even address caused the interrupt.

If the decoded selected line combination finds a 0 in the corresponding position of the HS select register, the state of the upper scan limits determines what modifications are made to the line address.

7 Upper Scan Limit Modification

Each type 3 scanner has two upper scan limit latches. Each scanner modifies the address on the line address bus according to the state of its upper scan limit latches. See the chart to the right for the actual line address bit positions modified by the four states of the upper scan limit latches. The line address bus output may be modified in some form as shown in the chart. A zero in the '1st 3' position of the ICW local store address selects ICWs associated with LIBs 1, 2, 3 and also combines with a one in the '1 or 4', '2 or 5', or '3 or 6' positions for LIB select 1, 2, or 3.

If the scan counter output is not modified by the HS select register or by address substitution, the four states of the upper scan limit latches create the following effective scan periods:

3705-I

Upper Scan Limit State	Actual Scan Counter Period	Number of Interfaces actually scanned by Scanner	Number of times each interface is scanned in Scan Counter Period	(1.2 usec Cycle Time) Effective Scan Period
00	153.6 usec	96	1	*153.6 usec
10	153.6 usec	48	2	76.8 usec
11	153.6 usec	16	6	25.6 usec
01	153.6 usec	8	12	12.8 usec

3705-II

Upper Scan Limit State	Actual Scan Counter Period	Number of Interfaces actually scanned by Scanner	Number of times each interface is scanned in Scan Counter Period	(1.0 usec Cycle Time) Effective Scan Period	(0.9 usec Cycle Time) Effective Scan Period
00	192 usec	96	1	*192 usec	172.8
10	192 usec	48	2	96 usec	86.4
11	192 usec	16	6	32 usec	28.8
01	192 usec	8	12	16 usec	14.4
Scan limit state and scan counter period are not applicable for type 3HS scanners		2	48	4.0 usec	3.6 usec

*The effective scan period is for 96 addresses since the type 2 attachment base steps through 96 addresses.

3. The upper scan limit for a type 3HS scanner is forced to a value of 01 by the 3705 hardware and is not a program option.

8 LIB Select and Address Select

Every 1.6 (3705-I) microseconds, the scanner selects a line interface, or autocal interface, by sending the modified line address bus output to the LIB and interface by means of the LIB select and address select lines. (See Note.)

9 ICW Local Store

Each type 3 scanner contains a local store array that contains 64 addressable interface control words (ICW). Each ICW contains 16 bytes plus 16 parity bits. (Each type 3HS scanner local store array contains two ICWs only. Each ICW contains—in addition to 16 bytes with 16 parity bits—ICW bits 17.0, 17.1.) A distinct ICW is associated with each line interface, or autocal unit interface, attached to the scanner through a LIB. A duplex line interface has two distinct ICWs. See chart on B-250 for the relationships between the modified line address bus output, ICW array selection, and interface address selected for each scanner.

See B-220 for scan address timings to read out and write into the ICW associated with the selected interface address. CSB time gates the address to the local store, and the contents

of the selected ICW are placed in the ICW work register at R2 time. The scanner control logic examines the contents of this ICW and the 'control in B' status.

When a hardware interface bit service or a program service level 2 interrupt is required, the ICW contents are modified and written back into the local store at W2T1T2 time. If the ICW contents are not modified, they normally are not written into the local store array because the original contents are not destroyed during read-out.

10 LIB Control

The scanner control logic sends a 'control in B' signal to the selected interface which gates the status of certain data communications equipment lines and certain latches in the interface hardware back to the scanner. See F-530 for details.

11 Line Address Bus to Next Scanner

Line address bus positions 2-9 pass directly to the next scanner. Position 0 reverses position with the inverted position 1; however, these two positions are not used during scan addressing.

UPPER SCAN LIMIT MODIFICATIONS OF LINE ADDRESS BUS (Type 3 Scanner only)

Upper Scan Limit	Position	Address Bit Positions								Interface Lines Selected (assume scanner #1)	Modification Performed
		1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1		
00 (64 lines)	Line adr bus	1	1 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	1 ↓	LIB sel = 1; Adr sel = 1 (021)	Invert '1st 3' bit
	Local store adr	0	1 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	1 ↓		
10 (48 lines)	Line adr bus	X	0 ↓	1 ↓	0 ↓	0 ↓	1 ↓	1 ↓	1 ↓	LIB sel = 2; Adr sel = 7 (037)	Force '1st 3' bit to 0
	Local store adr	0	0 ↓	1 ↓	0 ↓	0 ↓	1 ↓	1 ↓	1 ↓		
11 (16 lines)	Line adr bus	X	X	X	X	1 ↓	1 ↓	0 ↓	0 ↓	LIB sel = 1; Adr sel = C (02C)	Force '1 or 4' bit to 1 and '1st 3', '2 or 5', '3 or 6' to 0.
	Local store adr	0	1	0	0	1 ↓	1 ↓	0 ↓	0 ↓		
01 (8 lines)	Line adr bus	X	X	X	X	1 ↓	1 ↓	0 ↓	X	LIB sel = 1; Adr sel = 5 (025)	If bit 8 = 1, force it to 0 and force bit 1 to 1.
	Local store adr	0	1	0	0	0	1 ↓	0 ↓	1		
	Line adr bus	X	X	X	X	0	1 ↓	0 ↓	X	LIB sel = 1; Adr sel = 4 (024)	If bit 8 = 0, do not modify it, but force bit 1 to 0. In both cases, force bit '1 or 4' to 1, and bits '1st 3', '2 or 5', or '3 or 6' to 0.
	Local store adr	0	1	0	0	0	1 ↓	0 ↓	0		

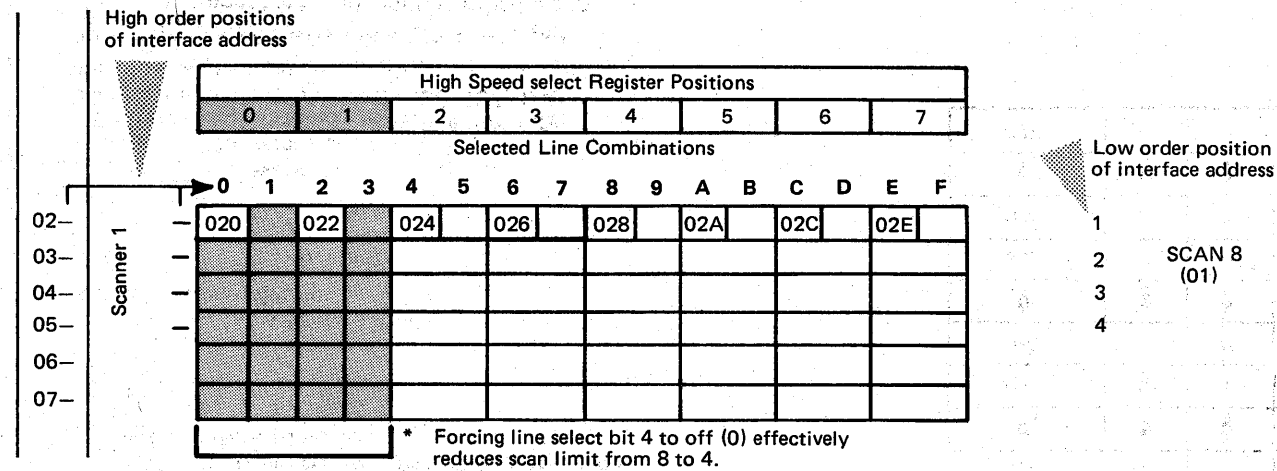
UPPER SCAN LIMIT MODIFICATIONS OF LINE ADDRESS BUS (Type 3HS Scanner Only)

Upper Scan Limit (See Note 3)	Position	Address Bit Positions								Interface Lines Selected (assume scanner #1)	Modification Performed
		1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1		
01 (2 lines)	Line adr bus	X	X	X	X	X	X	0	X	LIB sel = 1; Adr sel = 0 (020)	Force '1 or 4' bit to 1 and '1st 3', '2 or 5', '3 or 6' to 0.
	Local store adr	0	1	0	0	0	0	0	0		
	Line adr bus	X	X	X	X	X	X	1	X	LIB sel = 1; Adr sel = 2 (022)	Force bits 8, 4, and 1 to 0. Force bit 2 to 1.
	Local store adr	0	1	0	0	0	0	1	0		

↓ indicates no modification

X indicates don't care

SCAN ADDRESSING (TYPE 3HS SCANNERS ONLY)



Explanation of Type 3HS Scanner Addressing

With a type 3HS scanner, only line interface addresses 0 and 2 on a LIB 1 are scanned. Hardwired modifications to scan addressing circuits provide 48 scans of each selected line interface per scan counter cycle. The modifications force the following conditions to occur.

1. A scan limit of 8 is established which restricts interface line selection to a range of 020-027.
2. Line select bit 4 is forced off (0) and narrows the interface line selection range to 020-023.
3. High-speed select register positions 0 and 1 are forced on (1) to cause scanning of interface line addresses 0 and 2 only.

SCAN COUNTER (See Notes)

- Stepped every 1.6 (3705-1), 2.0 (3705-11, Models E-H), or 1.8 (3705-11, Models J-L) microseconds at C01 time (see F-090).
- There are 96 different states—one for each interface address in the type 2 communication scanner. The type 3 scanner can handle up to 64 interface addresses. The type 3HS scanner handles two interface addresses only.
- The relationship of the output state of the scan counter with respect to the line address bus bit positions is shown in the charts.

Position '1st 3' — A one indicates LIB 1,2 or 3 is selected. (See Note 2).
A zero indicates LIB 4,5 or 6 is selected.

Position '1 or 4' — A one selects LIB 1 if position '1st 3' is a one, or LIB 4 if position '1st 3' is a zero. (See Note 2).

Position '2 or 5' — A one selects LIB 2 if position '1st 3' is a one, or LIB 5 if position '1st 3' is a zero.

Position '3 or 6' — A one selects LIB 3 if position '1st 3' is a one, or LIB 6 if position '1st 3' is a zero.

See Note 2

Only one position, from among '1 or 4', '2 or 5', and '3 or 6', can be active at a time.

These four positions define the LIB to be selected.

Positions 8,4,2,1 form the hex representation for the line address within the selected LIB. See Note 1.

- The scan counter generates interface addresses in the sequence shown in the charts. The LIBs are selected in sequence (see Note 2)—however, the even interface addresses within each LIB are generated consecutively, followed by the odd interface addresses.

Notes:

- With the type 3HS scanner only line interface addresses 020, 022, 0A0, 0A2, 120, 122, 1A0, and 1A2 can be used.
- Type 3HS scanners attach to a LIB 1 only and do not use upper scan limit, address substitution, or the autocall option.

TYPE 3 COMMUNICATION SCANNER (BASIC FRAME) SEQUENCE OF INTERFACE ADDRESSES GENERATED BY SCAN COUNTER

Interface Address (Hex)	Scan Counter Bit Positions								LIB Selected	Interface Line Selected
	1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1		
	← LIB Address →				← Interface line within selected LIB →					
020	1	1	0	0	0	0	0	0	1	0
022	1	1	0	0	0	0	1	0		2
024	1	1	0	0	0	1	0	0		4
026	1	1	0	0	0	1	1	0		6
028	1	1	0	0	1	0	0	0		8
02A	1	1	0	0	1	0	1	0		A
02C	1	1	0	0	1	1	0	0		C
02E	1	1	0	0	1	1	1	0		E
021	1	1	0	0	0	0	0	1		1
023	1	1	0	0	0	0	1	1		3
025	1	1	0	0	0	1	0	1		5
027	1	1	0	0	0	1	1	1		7
029	1	1	0	0	1	0	0	1		9
02B	1	1	0	0	1	0	1	1		B
02D	1	1	0	0	1	1	0	1		D
02F	1	1	0	0	1	1	1	1	1	F
030	1	0	1	0	0	0	0	0	2	0
↓	↓	↓	↓	↓	Even lines then odd lines				↓	↓
03F	1	0	1	0	1	1	1	1	2	F
040	1	0	0	1	0	0	0	0	3	0
↓	↓	↓	↓	↓	Even lines then odd lines				↓	↓
04F	1	0	0	1	1	1	1	1	3	F
050	0	1	0	0	0	0	0	0	4	0
↓	↓	↓	↓	↓	Even lines then odd lines				↓	↓
05F	0	1	0	0	1	1	1	1	4	F
060	0	0	1	0	0	0	0	0		
↓	↓	↓	↓	↓	Even lines then odd lines					
06F	0	0	1	0	1	1	1	1		
070	0	0	0	1	0	0	0	0		
↓	↓	↓	↓	↓	Even lines then odd lines					
07F	0	0	0	1	1	1	1	1		

Since up to four LIBs can be attached to a type 3 scanner, these scan-counter interface addresses do not select a LIB or interface line but they are used for address substitution (see F-100).

TYPE 3HS COMMUNICATION SCANNER (BASIC FRAME) SEQUENCE OF INTERFACE ADDRESSES GENERATED BY SCAN COUNTER

Interface Address (Hex)	Scan Counter Bit Positions								LIB Selected	Interface Line Selected
	1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1		
	← LIB Address →				← Interface line within selected LIB →					
020	1	1	0	0	0	0	0	0	1	0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	0		0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	0		0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	0		0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	0		0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	1		0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	1		0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	1		0
022	1	1	0	0	0	0	1	0		2
020	1	1	0	0	0	0	0	1		0
022	1	1	0	0	0	0	1	0		2

ICW CONTROL AND DATA FIELDS (BYTES 0-5)

The ICW (interface control word) is the link between the control program and the type 3 scanner and the type 3 scanner and the interface hardware. Certain fields in the ICW buffer information about the interface between successive scans.

In addition the ICW controls the cycle steal operations between the PDF (parallel data field) and the SDF (serial data field) and between the PDF and main storage.

The type 3 scanner ICW consists of 128 information bits and is physically located in the scanner local store (130 information bits for a type 3HS scanner ICW).

BYTE 3, 4.0, 4.1 SET MODE

Set/reset ICW bit 5.4
Set/reset ICW bit 5.5
Set/reset ICW bit 5.6
Diagnostic mode
Set/reset data terminal ready
Synchronous mode
Set/reset ICW bit 5.7
Data rate select
Oscillator select bit 1
Oscillator select bit 2

BYTE 3-AUTO CALL DESCRIPTION

Interrupt Remember (IR)
Power Indicator (PWI)
Call Request (CRO)
Data Line Occupied (DLO)
Present Next Digit (PND)
Digit Present (DPR)
Data Set Status (DSS) Call Orig. Status (COS)
Abandon Call and Retry (ACR)

BYTE 1-AUTO CALL DESCRIPTION

(not used)	(DIGIT) NBR 8	(DIGIT) NBR 4	(DIGIT) NBR 2	(DIGIT) NBR 1
------------	---------------	---------------	---------------	---------------

OUTPUT X'43' F-270 Display Request

OUTPUT NAME	OUTPUT X'44' (F-280)							OUTPUT X'45' (F-290)				OUTPUT X'46' (F-300)							OUTPUT X'47' (F-310)		OUTPUT X'47' (F-310)		OUTPUT X'46' (F-300)																									
BYTE.BIT	SECONDARY CONTROL FIELD (SCF)							PARALLEL DATA FIELD (PDF)				LINE CONTROL DEFINER (LCD)		PRIMARY CONTROL FIELD (PCF)		SERIAL DATA FIELD (SDF)							MISC ICW BITS		MISC ICW BITS		MISC ICW BITS																					
DESCRIPTION	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7	3.0	3.1	3.2	3.3	3.4	3.5	3.6	3.7	4.0	4.1	4.2	4.3	4.4	4.5	4.6	4.7	5.0	5.1	5.2	5.3	5.4	5.5	5.6	5.7
Abort detected	Normal Service Request Interlock	Character Overrun/Underrun	Modem Check	Not Level 2 Bid	End of Message Interrupt	Program Flag	Line Trace Active	The PDF is physically located in the PDF array.									LCD (F-130) 4 bit field. Defines line control and dial interface.	PCF (F-140) 4 bit field. Defines state of communication line.		SDF 10 bit field used: 1. as character serializer/deserializer 2. to initialize line interface by means of set mode (PCF/EPCF state X'1')							Oscillator select bit 1	Oscillator select bit 2	Internal Timer (BSC) Ones Counter (SDLC)		Timeout Control Last Line State	Display Request	Internal Timer (BSC) Ones Counter (SDLC)		Level 2 Interrupt Pending	Priority Select Register bit 1	Priority Select Register Bit 2	Transparent text NRZI Control	Diagnostic bit 0	Diagnostic bit 1	External Modem Clock							
BSC																																																
SDLC																																																
ALD REF	TF200-TF205							TE299-TE329				TF300-TF305				TF400-TF405							TF410-TF415				TF310-TF315																					
INPUT	INPUT X'44' (F-210)							INPUT X'45' (F-210)														INPUT X'47' (F-210)																										

ICW CONTROL AND DATA FIELDS (BYTES 6-17)

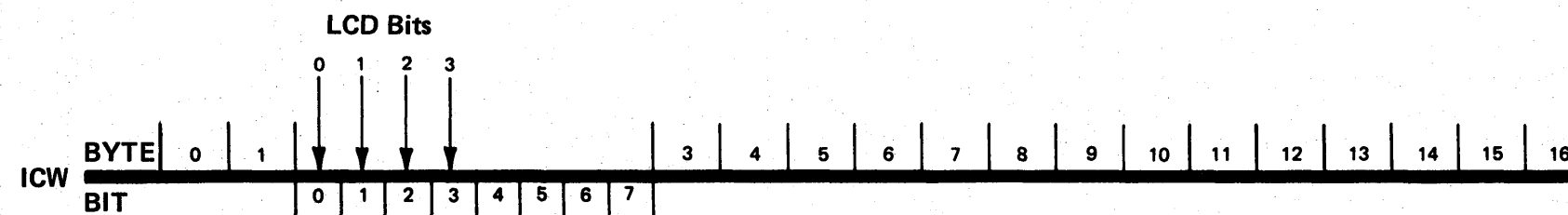
OUTPUT	OUTPUT X'48' (F-320)							OUTPUT X'49' (F-320)										OUTPUT X'4A' (F-320)																														
NAME	CYCLE STEAL ADDRESS		CYCLE STEAL CONTROL					CYCLE STEAL BYTE COUNT							CYCLE STEAL ADDRESS										BLOCK CHECK CHARACTERS																							
BYTE.BIT	6.0	6.1	6.2	6.3	6.4	6.5	6.6	6.7	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7	8.0	8.1	8.2	8.3	8.4	8.5	8.6	8.7	9.0	9.1	9.2	9.3	9.4	9.5	9.6	9.7	10.0	10.1	10.2	10.3	10.4	10.5	10.6	10.7	11.0	11.1	11.2	11.3	11.4	11.5	11.6	11.7
DESCRIPTION	Cycle Steal Address Byte X HIGH ORDER BIT (6.0)		ETB/ETX/ENQ in data	Cycle Steal Valid	Data Chain Flag	Message Chain Flag	Cycle Steal Byte Count 8-bit field containing the byte count of the buffer currently allocated to the ICW							Cycle Steal Address Byte 0					Cycle Steal Address Byte 1					BCC-1				BCC-2			BCC (Block Check Characters) 16-bit field in which the bcc is accumulated.																	
BSC																																																
SDLC																																																
ALD REF	TE200-TE205				TE210-TE215			TE200-TE205					TE210-TE215					TF300-TF305				TF310-TF315																										
INPUT	INPUT X'48' (F-230)							INPUT X'49' (F-230)										INPUT X'4A' (F-230)																														

OUTPUT	OUTPUT X'4E' (F-340)							OUTPUT X'4F' (F-350)										OUTPUT X'45' (F-290)				OUTPUT X'4E' (F-340)																				
NAME	ICW CONTROLS							STATUS EXCEPTION							BSC/SDLC CONTROL STATUS (F-150-160)			EXTENDED PCF (EPCF)				EXTENDED ICW CONTROLS																				
BYTE.BIT	12.0	12.1	12.2	12.3	12.4	12.5	12.6	12.7	13.0	13.1	13.2	13.3	13.4	13.5	13.6	13.7	14.0	14.1	14.2	14.3	14.4	14.5	14.6	14.7	15.0	15.1	15.2	15.3	15.4	15.5	15.6	15.7	16.0	16.1	16.2	16.3	16.4	16.5	16.6	16.7	17.0	17.1
DESCRIPTION	Cycle Steal PDF Array Pointer			PDF Array Pointer				Sequence 0	Sequence 1	Ready-to-Send Turnaround Control	Sequence 2	(reserved)	(reserved)	CS Message Counter	Received Line Signal Detect	Format Exception Idle Detect	Flush	Data Check	Bad Pad	Flag Off Boundary	ACK Expected	2 Control Characters	DLE Sequence Error	Length Check	Initial Status (BSC)		Final Status (BSC)			Leading Graphics	New Sync	Data Terminal Ready	On-line Terminal Test Diagnostic	(reserved)	EPCF (F-140) EPCF (Extended Primary Control Field) 4 bit (hex) character. Defines the state of the communication line when combined with the PCF.				Cycle Steal PDF Array Pointer (type 3HS scanner only)	PDF Array Pointer (type 3HS scanner only)		
BSC															See F-160 for BSC bits																											
SDLC															See F-160 for SDLC bits																											
ALD REF	TF410-TF415				TF400-TF405			TF200-TF205					TF210-TF215			TF210-TF215				TE-352																						
INPUT	INPUT X'4E' (F-240)							INPUT X'4F' (F-240)										INPUT X'4B' (F-240)				INPUT X'41' (F-190)																				

ICW LINE CONTROL DEFINER

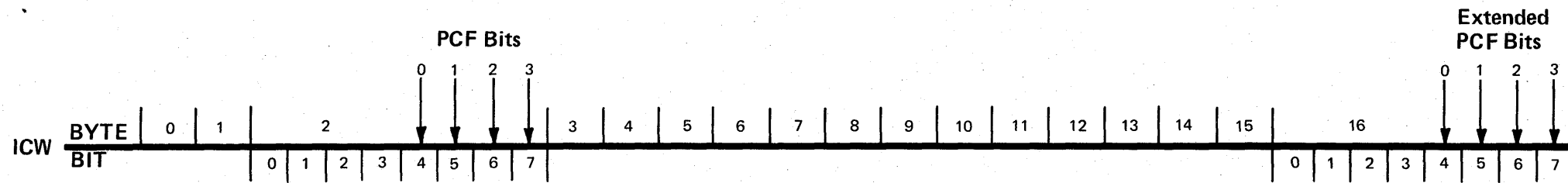
LCD (Line Control Definer)

The LCD is used during transmit and receive operations to define the line control used by the line interface. LCD bit 0 (located in ICW 2.0) defines EP (Emulation Program) or NCP (Network Control Program) mode. The offstate of this bit (LCD hex characters 0-7) defines EP mode. The onstate of this bit (LCD hex characters 8-E) defines NCP mode; LCD X'F' defines a feedback check for both EP and NCP modes (see key symbol 5 on page F-530).



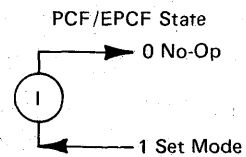
	LCD HEX CHARACTER	TYPE OF LINE CONTROL
EP	0	Reserved
	1	Reserved
	2	Reserved
	3	Dial (Auto-Call unit)
	4	BSC EBCDIC Line Control
	5	BSC USASCII Line Control
	6	BSC Transparent USASCII Line Control
	7	Reserved
NCP	8	Reserved
	9	SDLC 8 bit byte length—search for SDLC control characters (Flag, Abort, Idle).
	A	Reserved
	B	Reserved
EP and NCP	C	BSC EBCDIC Line Control
	D	BSC USASCII Line Control
	E	Reserved
	F	Feedback check

ICW-PRIMARY/EXTENDED PRIMARY CONTROL FIELD



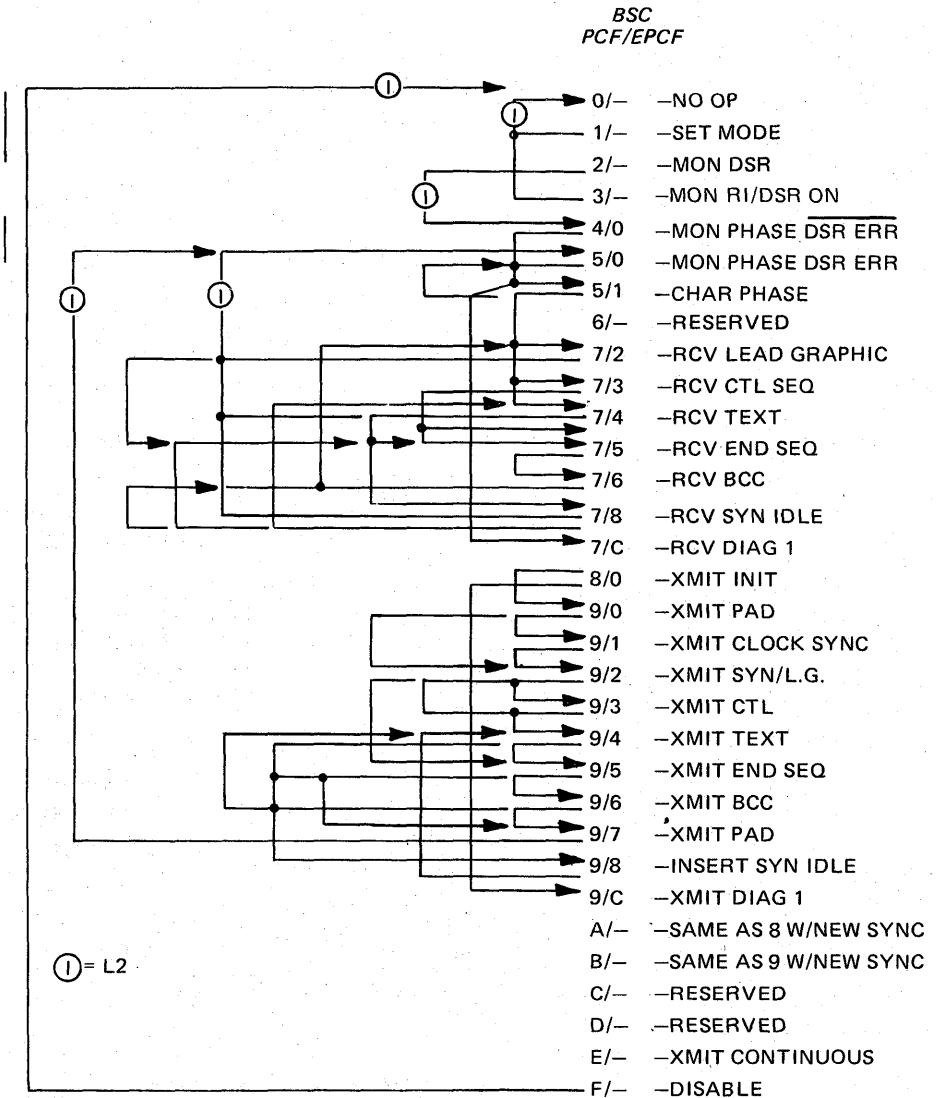
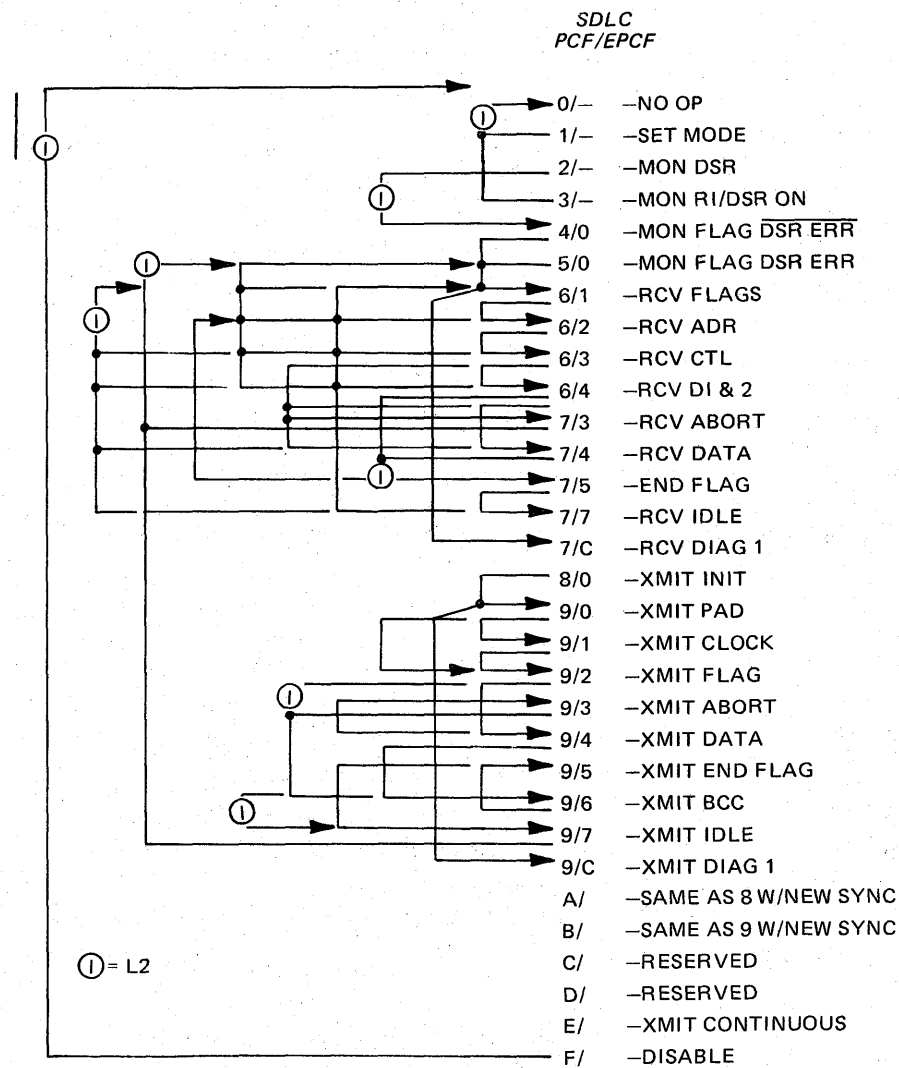
- The PCF (primary control field) and EPCF (extended primary control field) define the state of the line interface at any particular time. They are used to buffer the operation being performed on that line interface between successive scans.
- The control program initially sets the status of the PCF/EPCF.
- The control program executes Output X'45' to set or change the PCF/EPCF states.
- The type 3 scanner automatically changes PCF status under certain conditions (see diagrams).
- The control program executes Input X'45' to determine the PCF status, and Input X'4B' to determine the EPCF status.
- The scanner interpretation of the PCF/EPCF depends upon the state of the LCD field. The interpretations for a binary synchronous interface and a synchronous data link control interface are shown on this page. See B-090 for the interpretation of the PCF/EPCF for an autocal interface.
- Refer to the state transfer diagrams in the ALDs for the conditions that change the PCF/EPCF states.

Explanation of diagrams.

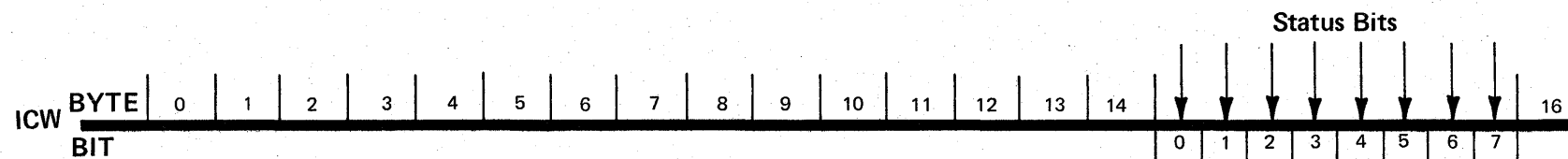


The control program sets PCF/EPCF X'1/-'. This is indicated by no line going toward 1. Once the scanner executes set mode (PCF/EPCF X'1/-'), the scanner automatically sets PCF/EPCF X'0/-' (No-Op). This is indicated by the line leaving 1 and going to 0. A level 2 interrupt request occurs and is indicated by the ① inserted within the line. A dash represents a don't care condition of the EPCF bits.

Note: See B-310 for the logic circuits that cause 'interrupt go'. This causes the level 2 interrupt request.



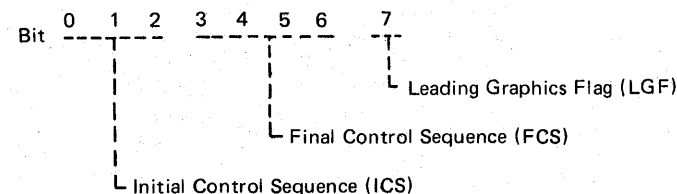
ICW BYTE 15 (BSC STATUS)



EP MODE

For EP LCD states, the initial and final control sequences are in the data stream except for transparent endings.

STATUS BYTE FORMAT FOR BSC TRANSMIT IN NCP MODE



Initial Control Sequence (BSC Transmit)

Used at the beginning of a BSC transmit operation for control characters.

The initial control sequence bits are defined as:

- Bit 012
- 000 - No Initial Control
- 001 - Start of Text STX
- 010 - Transparent Start of Text DLE-STX
- 011 - Start of Header SOH
- 100 - Special XMIT EOT
- 111 - Prog Flag X'FF' (set by hardware)

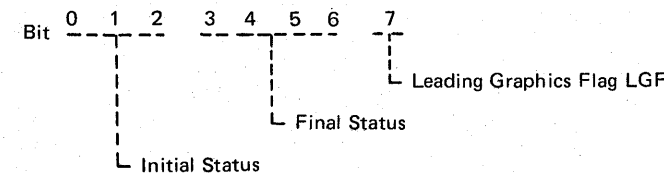
All other combinations are undefined for BSC transmit. Use of any undefined combination may result in undefined operation.

Final Control Sequence (BSC Transmit)

Used at the end of a BSC transmission. Its meaning is defined in conjunction with the initial control sequence field.

ICS	FCS	LGF	
Bit 012	3456	7	
000	0011	0/1	XMIT ENQ, turn line around. ENQ may be in data stream of leading graphics.
000	0110	0/1	XMIT ACK-0, turn line around.
000	0111	0/1	XMIT NAK, turn line around.
000	1101	0	XMIT, RVI, turn line around.
000	1110	0/1	XMIT ACK-1, turn line around.
000	1111	0/1	XMIT WACK, turn line around.
001	0011	0	XMIT STX-ENQ (TTD), turn line around, byte count set to zero.
001	1001	0	XMIT STX-data-ETX, turn line around, no skip byte on ITB in data.
001	1010	0	XMIT STX-data-ETB, turn line around, no skip byte on ITB in data.
001	1101	0	XMIT STX-data-ETX, turn line around, skip byte on ITB in data.
001	1110	0	XMIT STX-data-ETB, turn line around, skip byte on ITB in data.
010	0011	0	XMIT DLE-STX-data-DLE-ENQ, turn line around.
010	0100	0	XMIT DLE-STX-data-DLE-ITB
010	1001	0	XMIT DLE-STX-data-DLE-ETX, turn line around.
010	1010	0	XMIT DLE-STX-data-DLE-ETB, turn line around.
010	1101	0	XMIT data-DLE-ETX, turn line around ITB was previously sent
010	1110	0	XMIT data-DLE-ETB, turn line around. ITB was previously sent.
011	0011	0	XMIT SOH-data-ENQ, turn line around.
011	1001	0	XMIT SOH-data ETX, turn line around, no skip byte on ITB in data.
011	1010	0	XMIT SOH-data ETB, turn line around, no skip byte on ITB in data.
011	1101	0	XMIT SOH-data-ETX turn line around, skip byte on ITB in data.
011	1110	0	XMIT SOH-data-ETB, turn line around, skip byte on ITB in data.
<i>Note: If DLE-STX is in data stream ending is DLE-ETX or DLE-ETB.</i>			
100	1100	0	XMIT EOT, turn line around.
100	1110	0	XMIT DLE-EOT, turn line around.

STATUS BYTE FORMAT FOR BSC RECEIVE



Initial Status (BSC Receive)

The initial status bits are set according to the first text control character received.

- Bit 012
- 000 - Control mode - no text received
- 001 - text mode - STX first character
- 010 - transparent text mode - DLE-STX first characters
- 011 - Heading - SOH first character
- 100 - Special Status - DLE-EOT (DISC) first characters

Final Status (BSC Receive)

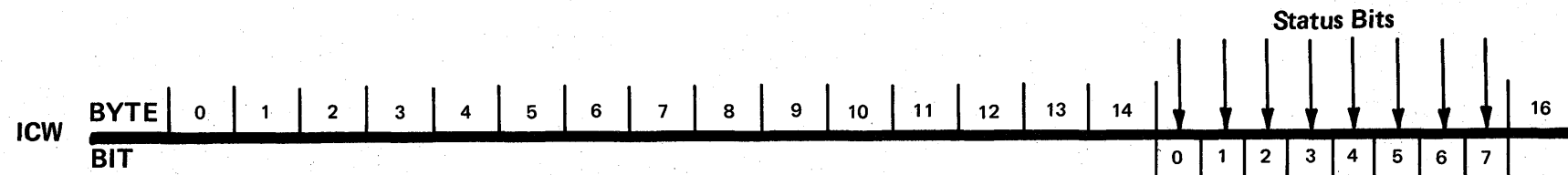
The final status bits are set according to the ending control characters received.

- Bits 3-6
- 0000 - Timeout
- 0001 - ITB
- 0010 - ENQ
- 0011 - EOT
- 0100 - 'STICK'
- 0101 - Wrong ACK
- 0110 - NAK
- 1000 - ETX
- 1001 - ETB
- 1010 - RVI
- 1011 - Positive ACK
- 1100 - WACK
- 1101 - WACK
- 1110 - WACK
- 1111 - WACK

Leading Graphics (BSC Receive)

The leading graphics bit is set if the first character after the phase character is not an initial or final status.

ICW BYTE 15 (SDLC STATUS)



STATUS BYTE FORMAT FOR SDLC TRANSMIT

The status byte is set by the network control program to inform the scanner of the action to perform at the end-of-frame.

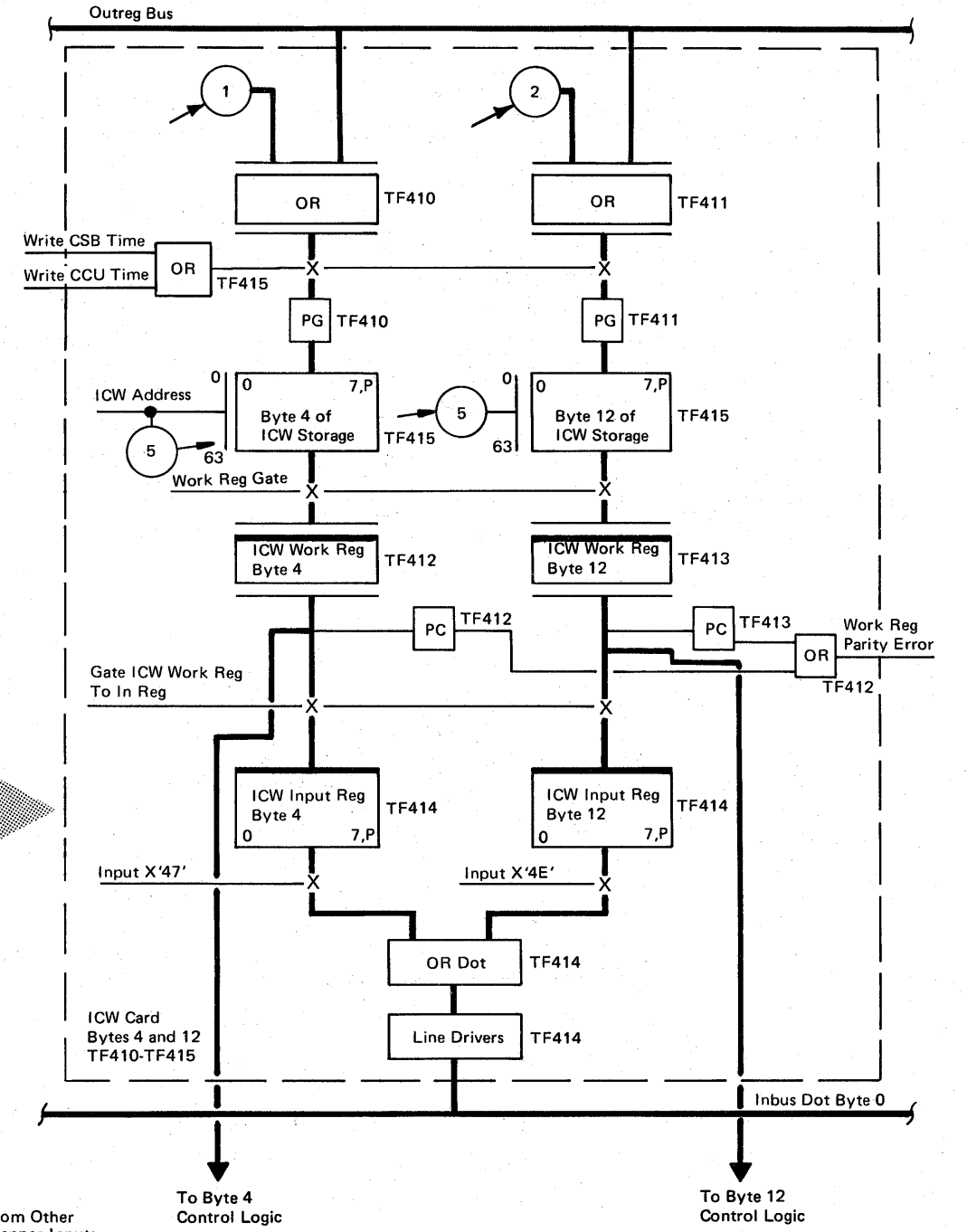
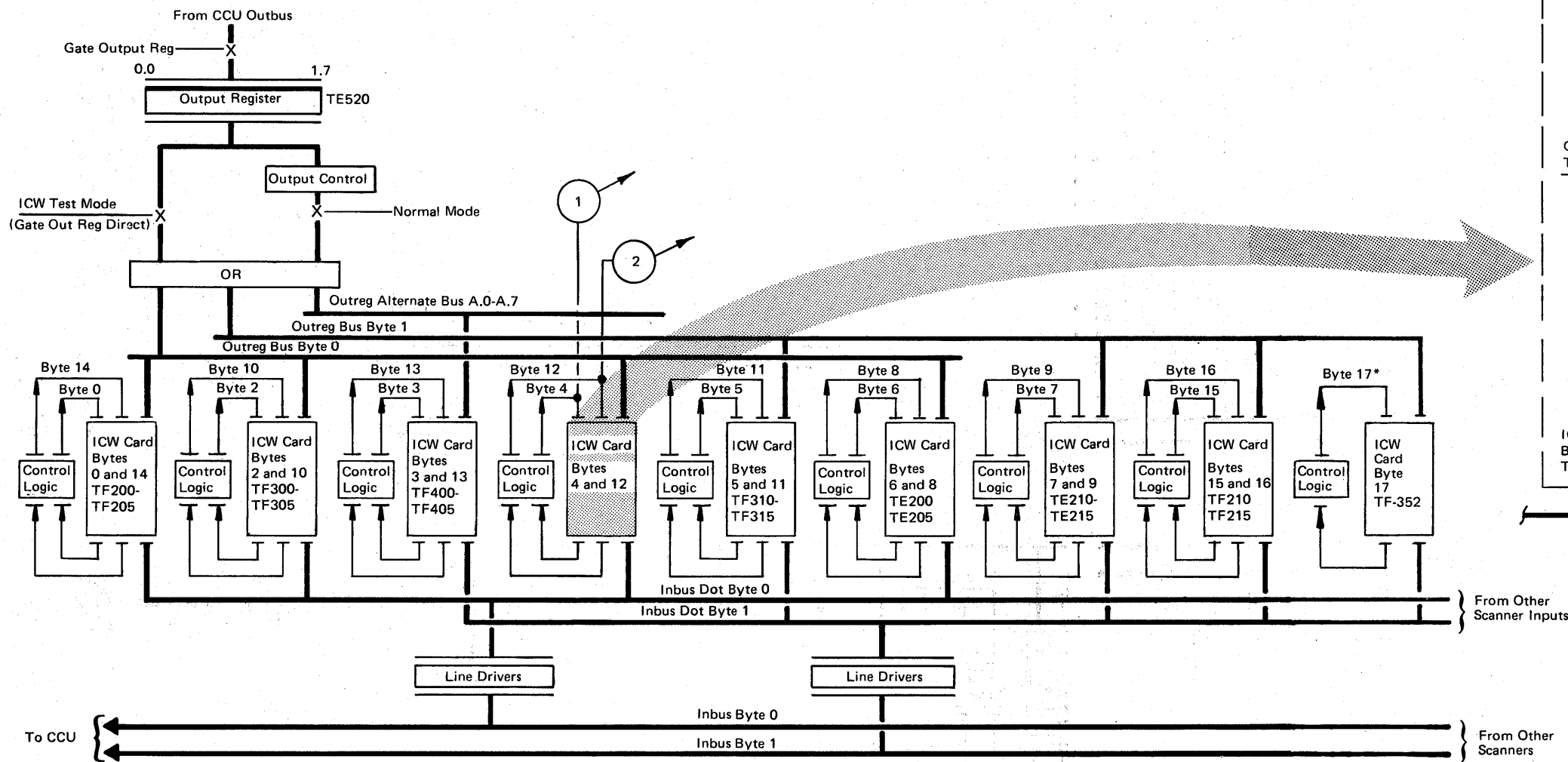
- Bits 0-3 Not used in SDLC transmit
- Bit 4
 - Bit 4 is on — transmit extra flag ahead of SDLC test frame.
 - Bit 4 is off — do not transmit extra flag ahead of SDLC test frame.
- Bit 5
 - If a line turnaround is not required (bit 7=0) and:
 - Bit 5 is on — transmit continuous flags.
 - Bit 5 is off — go to the line idle state.
- Bit 6
 - If a line turnaround is required (bit 7=1) and:
 - Bit 6 is on — transmit 9 consecutive ones before turning the line around.
- Bit 7
 - Bit 7 is on — Turn the line around to receive.

STATUS BYTE FORMAT FOR SDLC RECEIVE

- Bit 0 Control exception. Set by the scanner hardware to indicate a control frame was indicated by the "control" character but a Flag character was not received three characters later.
- Bit 1 Reserved
- Bit 2 Reserved
- Bit 3 Idle. Set by the network control program to request a level 2 interrupt if the receive line goes to an idle state after a Flag is detected.
- Bit 4 Reserved
- Bits 5-7 Not used in receive.

ICW DATA FLOW

All ICW cards except byte 17 may be swapped.
See the description of ICW test mode for Output X'43' (F-270), X'44' (F-280), X'45' (F-290), X'46' (F-300), and X'4F' (F-350) instructions.



* Byte 17 is used with the type 3HS scanner only.

INPUT X'40' (INTERFACE ADDRESS)

Input X'40' is used to obtain the interface address from ABAR (attachment buffer address register) in the attachment base. When Input X'40' is executed, the attachment base gates the interface address in ABAR to the 0.6 through 1.6 bit positions of the general register specified by the R field. The attachment base also gates a 1 to position 0.4 and a 0 to each of the remaining positions in the general register.

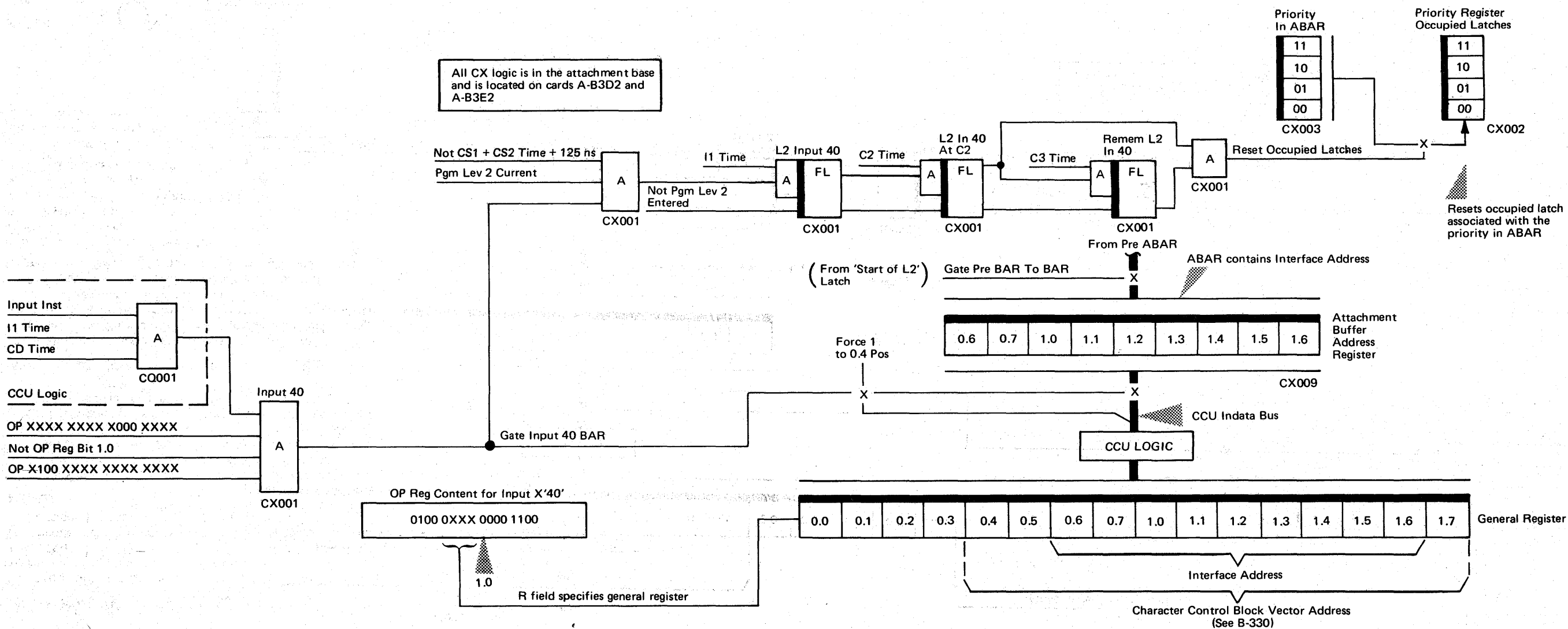
If Input X'40' is executed during program level 2, the attachment base resets the 'priority register occupied' latch associated with the interface address in ABAR. This indicates that (1) the character service request is being serviced by the control program and (2) the 'program level 2 interrupt priority register', from which the ABAR was loaded, is now available for another level 2 interrupt of the same priority. Subsequent Input X'40' instructions within the same character service interrupt do not reset the 'priority register occupied' latches. An exit instruction must be executed in program level 2 to reset the L2 input 40 latches before another 'reset occupied latches' signal can occur.

INPUT X'40' TIMINGS

FET STORAGE*

CCU CLock (*)	A	B	C	D	A	B	C	D	A	B	A	B	C	D
I1 Time of Input X'40'					(Next Instruction)				Exit Instr					
Gate Input 40 BAR														
Write LS (in CCU)														
Pgm Lev 2 Entered													Exit	
Pgm Lev 2 Current														Exit
L2 Input 40 FL														
Attachment Base Clock (*)	C4	C5	C6	C7	C0	C1	C2	C3	C4	C5	C0	C1	C2	C3
L2 In 40 AT C2 FL														
Remem L2 In 40 FL														
Reset Occupied Latches														

*For timing with bridge storage see B-120



INPUT X'41' AND X'42'

INPUT X'41' (HIGH SPEED SELECT)

The 3705 control program uses this instruction to determine the setting of the high-speed select register and to obtain ICW bits 17.0 and 17.1 during type 3HS scanner operations. The scanner gates the contents of the high-speed select register to the general register specified by the R field.

Notes:

1. ICW bits 17.0 and 17.1 contain meaningful information only after a) a level 2 interrupt occurs, or b) an Output X'40' instruction is executed in program level 3 or 4.
2. The high-speed select register option is not applicable to type 3HS scanner operation.

INPUT X'42' (DBAR/CHECK REGISTER 0)

The 3705 control program uses this instruction to determine the state of check register 0, DBAR (diagnostic buffer address register), and scan limit bits. The scanner gates these bits to the general register specified by the R field.

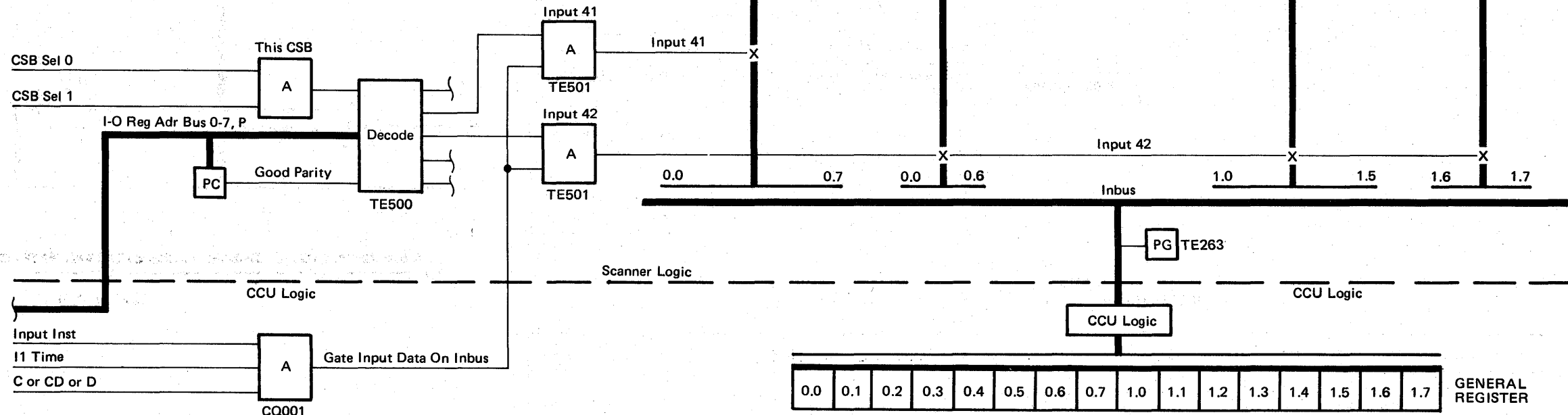
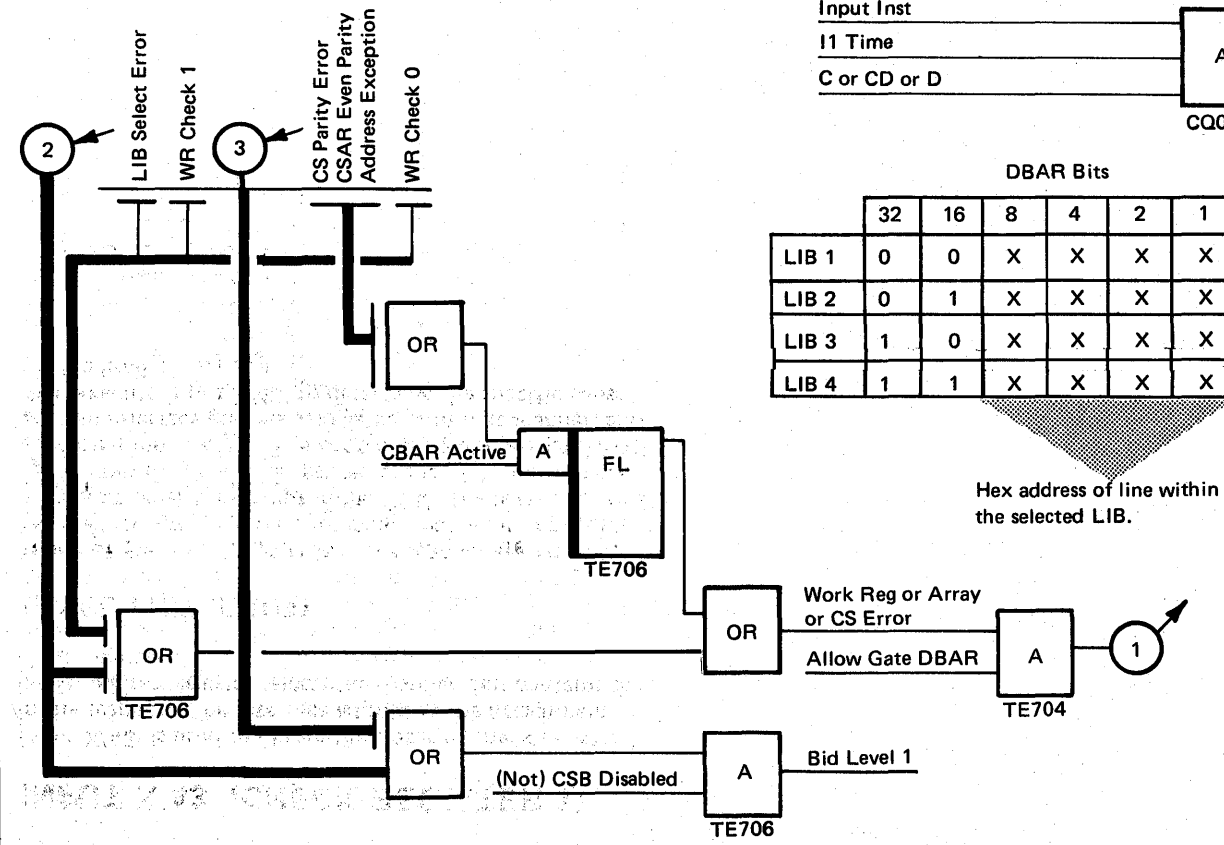
The scanner sets the cycle-steal address, currently in CBAR, into DBAR **1** when the following errors occur:

- ICW work register checks 0 thru 7.
- PDF array check.
- LIB select error.
- CS parity error (CS inbound/outbound data).
- CSAR even parity.
- CSAR address exception.

An Output X'42' instruction also sets DBAR as well as the scan limits. Upper scan limit option is not applicable to type 3HS scanner operations.

LEVEL 1 INTERRUPT

If any of the check register bits in a scanner are set to 1, the scanner sets the level 1 interrupt request that bids for a program level 1 interrupt in the CCU. The level 1 routine determines which scanner caused the level 1 interrupt by executing Input X'76'. The control program can set ABAR with an interface address associated with that scanner, and then execute Input X'42' and Input X'43' to determine the specific cause for the level 1 interrupt.



General Register Bit Pos.	INPUT X'41'		INPUT X'42'	
	Description	Check Register 0 Position	Cause of Check	
0.0	High speed select reg 0	ICW work reg check 2	Set to 1 if scanner detects a parity check (even) from ICW work register for Byte 3 or Byte 13.	TE701
0.1	High speed select reg 1	ICW work reg check 3	Same as above for ICW Byte 4 or Byte 12.	TE701
0.2	High speed select reg 2	ICW work reg check 4	Same as above for ICW Byte 5 or Byte 11.	TE701
0.3	High speed select reg 3	ICW work reg check 5	Same as above for ICW Byte 6 or Byte 8.	TE701
0.4	High speed select reg 4	ICW work reg check 6	Same as above for ICW Byte 7 or Byte 9.	TE701
0.5	High speed select reg 5	ICW work reg check 7	Same as above for ICW Byte 15 or Byte 16.	TE701
0.6	High speed select reg 6	PDF array check	Set to 1 if scanner detects a parity check (even) on the PDF array output.	TE701
0.7	High speed select reg 7	0		
1.0	Cy Stl PDF Array Ptr Bit 16*	DBAR 32		TE704
1.1	PDF Array Ptr Bit 16*	DBAR 16		TE704
1.2	0	DBAR 8		TE704
1.3	0	DBAR 4		TE704
1.4	0	DBAR 2		TE704
1.5	0	DBAR 1		TE704
1.6	0	Scan limit 0**		TE540
1.7	0	Scan limit 1**		TE540

* General register bit positions 1.0 and 1.1 are associated with ICW bits 17.0 and 17.1, respectively (type 3HS scanner only).
 ** Scan limit is not applicable to type 3HS scanner operations.

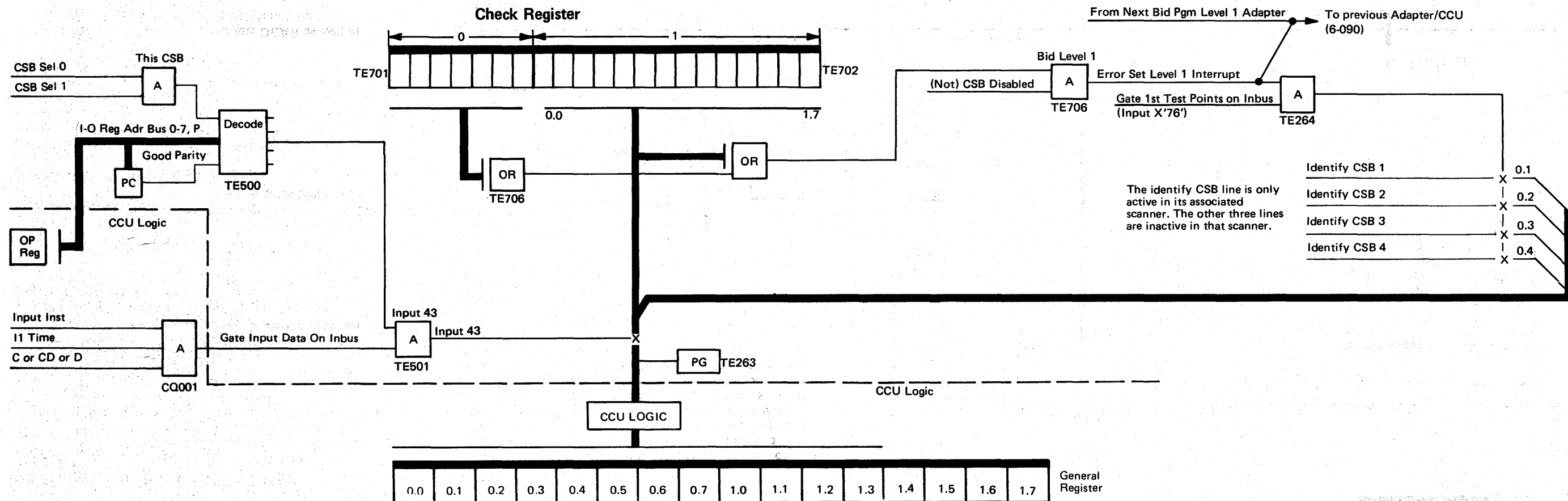
INPUT X'43' (CHECK REGISTER 1)

Input X'43' is used to obtain the status of check register 1 in the scanner. The interface address in the attachment buffer address register selects the scanner that contains the check register.

LEVEL 1 INTERRUPT

If any of the check register bits in a scanner are set to 1, the scanner sets the level 1 interrupt request that bids for a program level 1 interrupt in the CCU. The level 1 routine determines which scanner caused the level 1 interrupt by executing Input X'76'. The control program can set ABAR with an interface address associated with that scanner, and then execute Input X'43' to determine the specific cause for the level 1 interrupt.

General Register (R)	Check Register Position	Cause Of Check	Reference
0.0	LIB 1 BCC Check	Set to 1 if the scanner detects a LIB 1 BCC local store parity error during a bit clock selection.	TE702
0.1	LIB 2 BCC Check	Same as above for LIB position 2.	TE702
0.2	LIB 3 BCC Check	Same as above for LIB position 3.	TE702
0.3	LIB 4 BCC Check	Same as above for LIB position 4.	TE702
0.4	0		
0.5	0		
0.6	LIB Select Check	Set to 1 if more than one LIB was selected, or more than one line was accessed on the selected LIB, or no line was accessed on the selected LIB, or a line was accessed on a LIB that was not selected.	TE702
0.7	Inbus Check	Set to 1 if the scanner detects a parity error (even) on Inbus bytes 0 or 1.	TE263
1.0	ICW Work Reg Check 1	Set to 1 if the scanner detects a parity error (even) from ICW work reg for Byte 2 or Byte 10.	TE701
1.1	Priority Reg Avail Check	Set to 1 if the scanner detects a parity error (even) in the priority register available lines (4 + P).	TE703
1.2	CCU Outbus Check	Set to 1 if the scanner detects a parity error (even) on the Outbus (16 + 2P).	TE703
1.3	Line Adr Bus Check	The line adr bus parity is used to predict the parity of the address as modified by the scanner's upper scan limits. If this predicted parity does not compare with the actual parity of the modified address, the scanner sets this bit to 1.	TE703
1.4	Bad Inbound or Outbound CS Data	Scanner sets to 1 if CCU detects a parity check on the data the scanner is cycle stealing to or from storage.	TE703
1.5	CSAR Check	Scanner sets to 1 if CCU detects a parity check (even) in the Cycle Steal Address Register.	TE703
1.6	Address Exception	Scanner sets to 1 if the CCU detects that the address in CSAR exceeds the CCU storage size or points to a protected area of storage not assigned to the scanner. Scanner sets to 0 if 1.5 is a 1.	TE703
1.7	ICW Work Reg Check 0	Set to 1 if scanner detects a parity check (even) from ICW work reg for Byte 0 or Byte 14.	TE701



INPUT X'44', X'45', AND X'47'

INPUT X'44' (ICW BYTE 0 AND PDF ARRAY)

The 3705 control program uses this instruction to determine the states of the SCF (secondary control field) and the PDF (parallel data field) from the PDF array. The scanner gates the contents of the ICW Input register byte 0 (SDF) and PDF In register to the general register specified by the R field. See the chart below for the bit definitions.

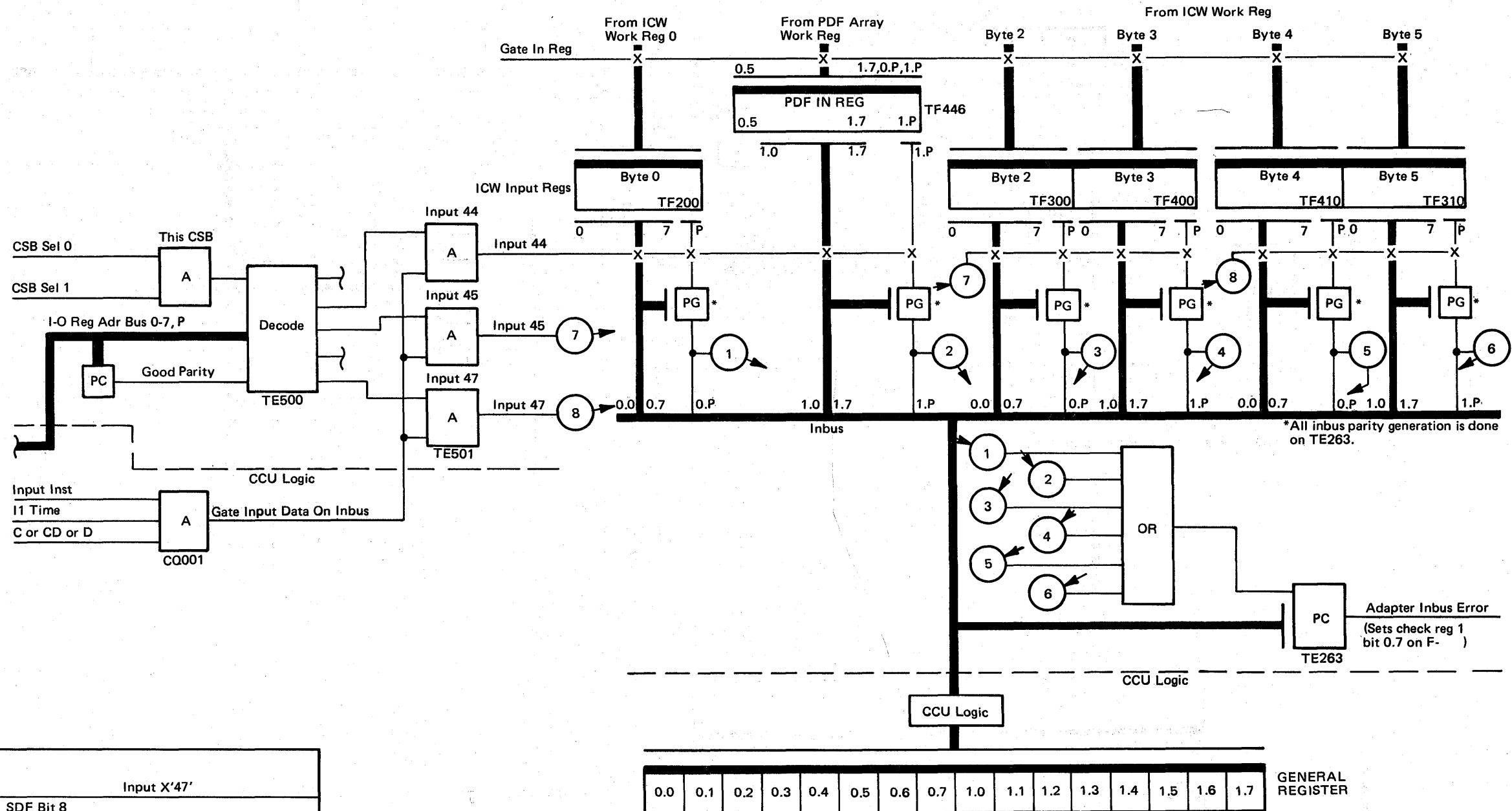
INPUT X'45' (ICW BYTES 2 AND 3)

The 3705 control program uses this instruction to determine the states of the LCD, basic PCF, and SDF. The scanner gates the contents of the ICW Input register byte 2 (LCD and basic PCF) and byte 3 (SDF) to the general register specified by the R field.

INPUT X'47' (ICW BYTES 4 AND 5)

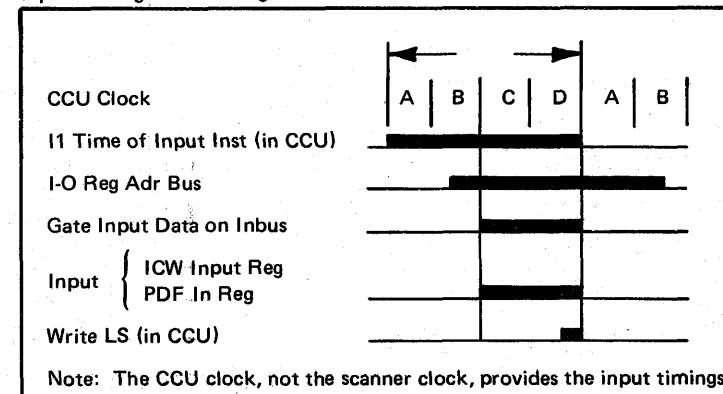
The 3705 control program uses this instruction to determine the states of the bits in ICW bytes 4 and 5 as defined in the chart below. The scanner gates the contents of the ICW Input register bytes 4 and 5 to the general register specified by the R field.

The ICW Input registers and PDF In register are loaded from the ICW and PDF array work registers respectively when a level 2 interrupt or Output X'40' in levels 3 or 4 raises 'fetch buffer'.



General Register Bit Pos.	Input X'44'	Input X'45'	Input X'47'
0.0	SCF 0 (Abort Detect-SDLC)	LCD Bit 0	SDF Bit 8
0.1	SCF 1 (Service Request Interlock)	LCD Bit 1	SDF Bit 9
0.2	SCF 2 (Character Overrun/Underrun)	LCD Bit 2	Ones Count-SDLC or Interval Timer-BSC; Bit 4
0.3	SCF 3 (Modem Check)	LCD Bit 3	Ones Count-SDLC or Interval Timer-BSC; Bit 2
0.4	SCF 4 (Not L2 Bid)	PCF Bit 0	Ones Count-SDLC or Interval Timer-BSC; Bit 1
0.5	SCF 5 (End of Message)	PCF Bit 1	Last Line State-SDLC
0.6	SCF 6 (Program Flag)	PCF Bit 2	Display Request
0.7	SCF 7 (Line Trace Active)	PCF Bit 3	Ones Count-SDLC or Interval Timer-BSC; Bit 16
1.0	PDF Bit 0	SDF Bit 0	Ones Count-SDLC or Interval Timer-BSC; Bit 8
1.1	PDF Bit 1	SDF Bit 1	L2 Interrupt Pending
1.2	PDF Bit 2	SDF Bit 2	Priority Bit 1
1.3	PDF Bit 3	SDF Bit 3	Priority Bit 2
1.4	PDF Bit 4	SDF Bit 4	NRZI Control-SDLC or Transparent Text-BSC
1.5	PDF Bit 5	SDF Bit 5	Diagnostic 0
1.6	PDF Bit 6	SDF Bit 6	Diagnostic 1
1.7	PDF Bit 7	SDF Bit 7	External Modem Clock

Input Timing-FET Storage *



* See B-140 for bridge storage timing.

INPUT X'46' (DISPLAY REGISTER)

The 3705 control program uses this instruction to determine the setting of the display register. The scanner gates the contents of the display register to the general register specified by the R field.

DISPLAY REQUEST OPERATION

After the attachment base address register (ABAR) has been set to the proper interface address, the control program executes an Output X'43' with bit 0.2=1 to set the display request bit (ICW bit 4.6). As long as the display request bit is on, every scan of that interface causes the display register to trap the contents on the B display bus.

For the display register contents to be meaningful, only one display request bit may be on in an ICW associated with a scanner. Because each scanner contains a display register, each scanner may contain one ICW that uses the display request bit. Input X'46' should not be executed until the interface has been scanned at least one time after setting the display bit. This ensures that the data in the display register is valid for the interface just selected and is not the result of a former display trap operation.

B DISPLAY BUS – NORMAL OPERATION

During 'control in B' time, the B data register traps the line interface status that is on 'CSB data in' 1. If B data 6 contains a diagnostic mode status bit and the line is operating in BSC or SDLC mode, the scanner forces bit 1 (CTS) and bit 3 (DTR). If there is not a feedback check, the contents of the B data register and the forced bits are gated to the B display bus and are then loaded into the display register if the display request bit is on.

During 'control in A' time, a feedback test 2 is made between the line interface A register contents on 'CSB data in' and the 'set' A register lines on 'CSB data out'. Any discrepancy causes a feedback check that inhibits gating the B data register contents to the B display bus. Instead, the line, or lines, that caused the feedback check are forced to zero and the remaining CSB data-in lines and CSB data-out lines that match, force their corresponding bits to ones. Thus the lines that caused the feedback check can be distinguished from the lines that are working correctly.

B DISPLAY BUS – DIAGNOSTIC MODE 0

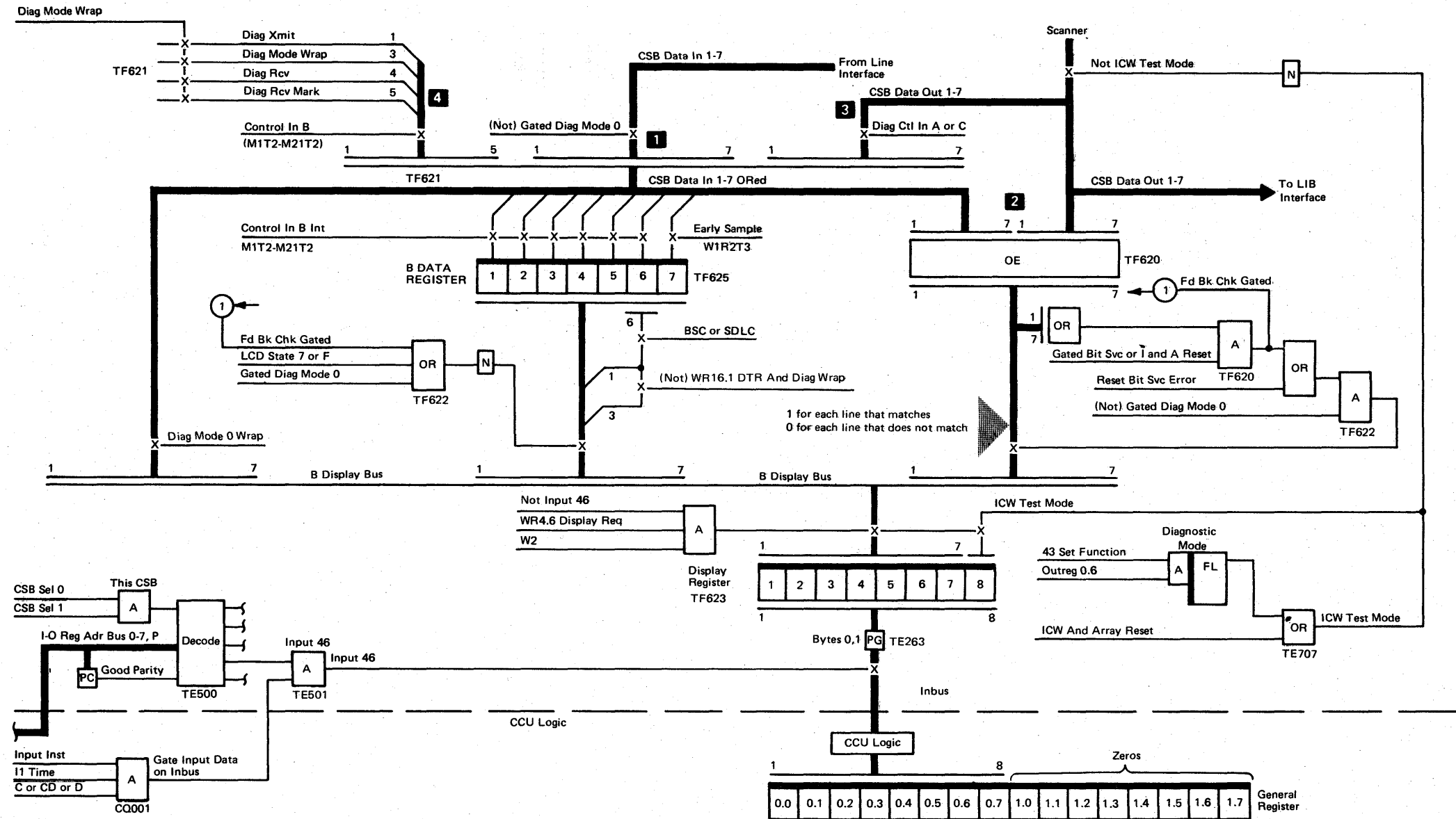
When a line is in diagnostic mode 0, the scanner performs a Diagnostic Scanner Wrap.

The control program sets the receive line, then the transmit line, to diagnostic mode 0 (Output X'46') and then sets the PCF, EPCF, and LCD states. Normal line functions are then simulated within the scanner: an associated LIB is not required. During the Diagnostic Scanner Wrap, the scanner gates the 'CSB data out' lines 3 to the B display bus and then to the display register for the line that has the display request bit on. 'Gated diag mode 0' inhibits the display register trapping the B data register or the feedback lines.

'Control in B' gates the diagnostic signals 4 to the B data register where:

- 'Diag xmit' simulates CTS.
- 'Diag mode 0 wrap' simulates DSR.
- 'Diag rcv' simulates RLSD.
- 'Diag rcv mark' simulates the receive data bit buffer.

The diagnostic signals are not gated to the display register since the display register traps at W2 time and the diagnostic signals are gated during 'control in B' time.



General Register Position	Line Interface From B Data Register	Autocall Interface from B Data Register	Feedback Check	Diagnostic Mode 0
0.0	Clear To Send: 1 if the CTS line from the modem is on, or if diagnostic wrap forces CTS on.	Abandon Call and Retry: 1 if the ACR line from the autocall unit is on.	Line or lines that caused the feedback check, set the corresponding bits to 0. The remaining CSB data-in and CSB data-out lines that match, set their corresponding bits to 1.	The 'CSB data out' lines. The interpretation of these lines depends on the line function being performed. See F-530 for the various combinations by line function.
0.1	Ring Indicator: 1 if the ring indicator line from the modem is on.	Present Next Digit: 1 if the PND line from the autocall unit is on.		
0.2	Data Set Ready: 1 if the DSR line from the modem is on, or if diagnostic wrap forces DSR on.	Data Line Occupied: 1 if the DLO line from the autocall unit is on.		
0.3	Receive Line Signal Detector: 1 if the RLSD line from the modem is on.	Power Indicator: 1 if the PWI line from the autocall unit is on.		
0.4	Receive Data Bit Buffer: 1 if the line interface receive data bit buffer contains a mark (1). This bit is 0 if the bit buffer contains a space (0).	Bit is always 0.		
0.5	Diagnostic Wrap Mode: 1 if the line interface is in diagnostic wrap mode.	Call Originating Status: 1 if the COS line from the autocall unit is on.		
0.6	Bit Service Request: 1 if the line interface bit service request is on.	Bit Service Request: 1 if the autocall interface bit service request is on.		
0.7	ICW Test Mode: 1 if 'diagnostic mode' latch is set by Output X'43' or by 'ICW and array reset'.	Same as Line Interface.	Same as Line Interface	Same as Line Interface

INPUT X'48' (ICW BYTES 6 AND 7)

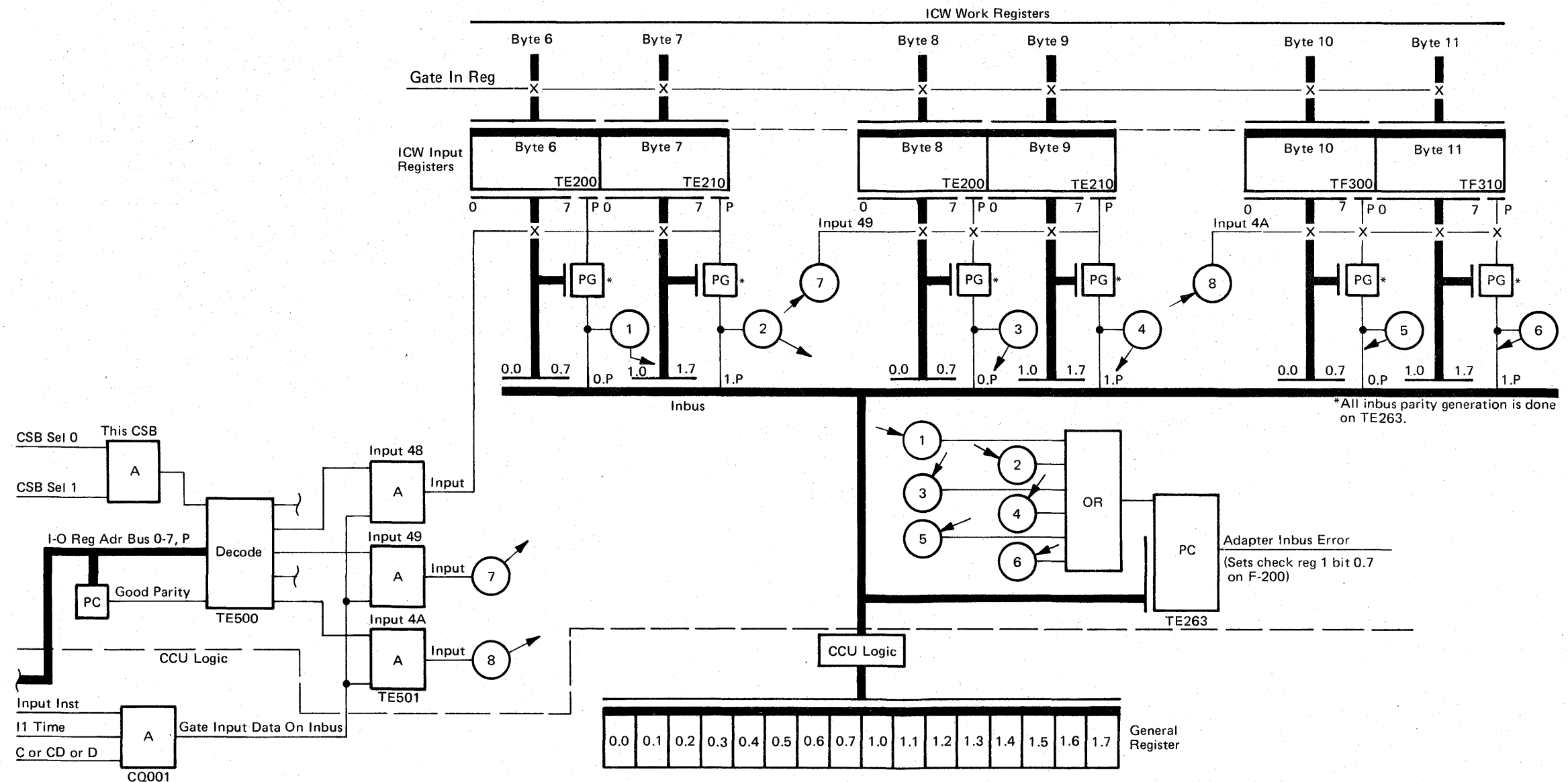
The 3705 control program uses this instruction (1) to determine the contents of the cycle steal byte count and cycle steal extended address bits X.4-X.7, (2) to determine the state of the cycle steal control bits, and (3) to determine whether ETB, ETX, or ENQ characters were in the cycle steal data. The scanner gates the contents of ICW input register bytes 6 and 7 to the general register specified by the R field.

INPUT X'49' (ICW BYTES 8 AND 9)

The 3705 control program uses this instruction to determine the contents of the cycle steal address register. The scanner gates the contents of ICW input register bytes 8 and 9 to the general register specified by the R field.

INPUT X'4A' (ICW BYTES 10 AND 11)

The 3705 control program uses this instruction to determine the contents of the old BCC (block check character). The 16 bit BCC accumulation for SDLC, BSC EBCDIC, or BSC USASCII is buffered in these two bytes between bit services. The scanner gates the BCC accumulation from ICW input register bytes 10 and 11 to the general register specified by the R field.



*All inbus parity generation is done on TE263.

General Register Bit Pos.	Input X'48'	Input X'49'	Input X'4A'
0.0	Cycle Steal Address X.4	Cycle Steal Address Register Bit 0.0	Old BCC Bit 0.0
0.1	Cycle Steal Address X.5	Cycle Steal Address Register Bit 0.1	Old BCC Bit 0.1
0.2	Cycle Steal Address X.6	Cycle Steal Address Register Bit 0.2	Old BCC Bit 0.2
0.3	Cycle Steal Address X.7	Cycle Steal Address Register Bit 0.3	Old BCC Bit 0.3
0.4	ETB, ETX, or ENQ Char in CS Data	Cycle Steal Address Register Bit 0.4	Old BCC Bit 0.4
0.5	Cycle Steal Valid	Cycle Steal Address Register Bit 0.5	Old BCC Bit 0.5
0.6	Data Chain Flag	Cycle Steal Address Register Bit 0.6	Old BCC Bit 0.6
0.7	Message Chain Flag	Cycle Steal Address Register Bit 0.7	Old BCC Bit 0.7
1.0	Cycle Steal Byte Count Bit 128	Cycle Steal Address Register Bit 1.0	Old BCC Bit 1.0
1.1	Cycle Steal Byte Count Bit 64	Cycle Steal Address Register Bit 1.1	Old BCC Bit 1.1
1.2	Cycle Steal Byte Count Bit 32	Cycle Steal Address Register Bit 1.2	Old BCC Bit 1.2
1.3	Cycle Steal Byte Count Bit 16	Cycle Steal Address Register Bit 1.3	Old BCC Bit 1.3
1.4	Cycle Steal Byte Count Bit 8	Cycle Steal Address Register Bit 1.4	Old BCC Bit 1.4
1.5	Cycle Steal Byte Count Bit 4	Cycle Steal Address Register Bit 1.5	Old BCC Bit 1.5
1.6	Cycle Steal Byte Count Bit 2	Cycle Steal Address Register Bit 1.6	Old BCC Bit 1.6
1.7	Cycle Steal Byte Count Bit 1	Cycle Steal Address Register Bit 1.7	Old BCC Bit 1.7

INPUT X'4B', X'4C', X'4E', AND X'4F'

INPUT X'4B' (ICW BYTE 16)

The 3705 control program uses this instruction to determine the state of the Extended PCF, New Sync, DTR and OLTT diagnostic bits. The scanner gates the contents of ICW input register byte 16 to the general register specified by the R field.

INPUT X'4C' (PDF ARRAY BITS 0-10)

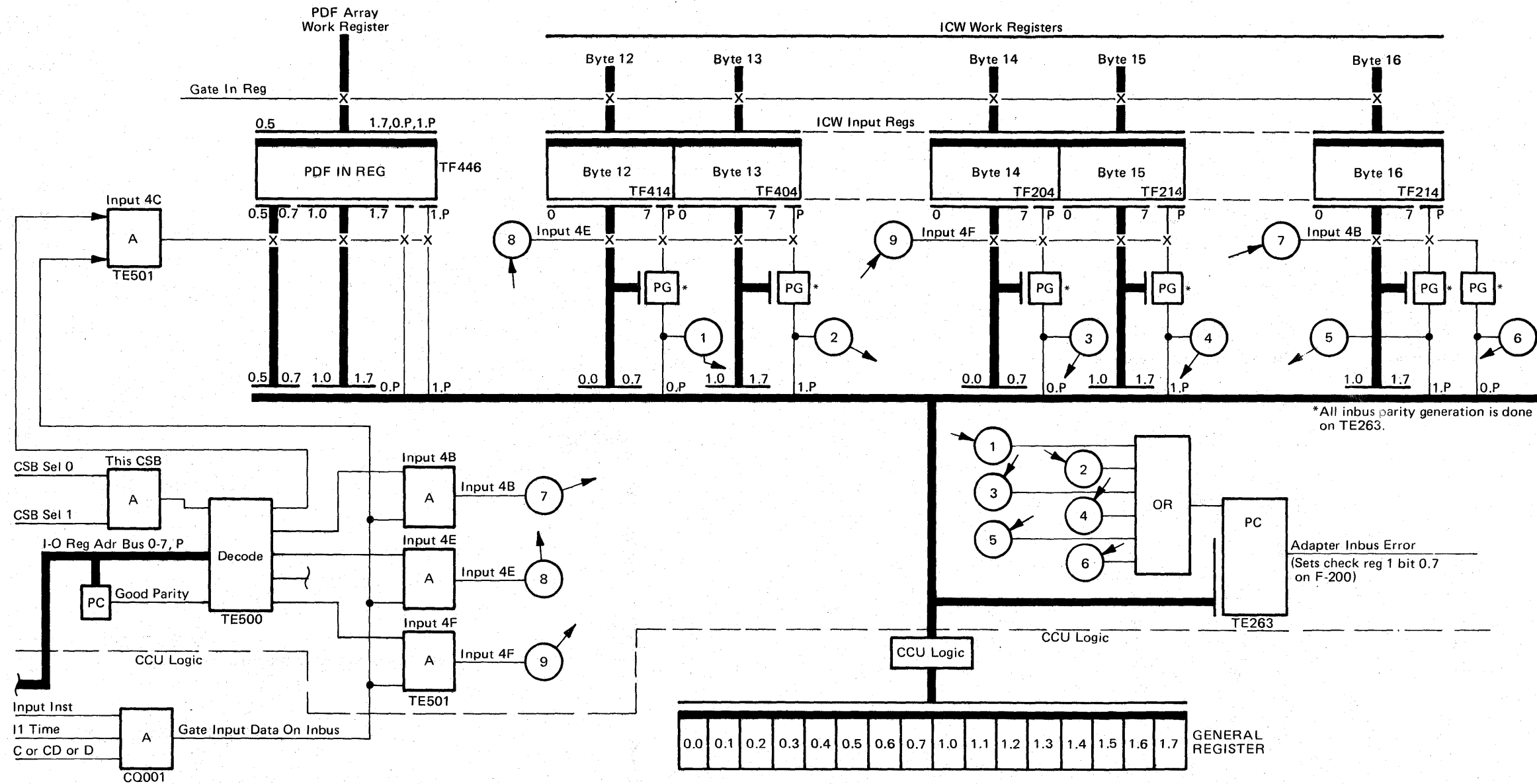
The 3705 control program uses this instruction to determine the contents of PDF array bits 0-10. The scanner loads the PDF work register with the contents of the PDF array buffer that is selected by the PDF pointer (ICW bits 12.4-12.7) **1**. 'Fetch buffer' loads the contents of the PDF work register into the PDF in-register just as 'fetch buffer' loads the contents of the ICW work registers into the ICW input registers. The scanner gates the contents of the PDF in-register to the general register specified by the R field.

INPUT X'4E' (ICW BYTES 12 AND 13)

The 3705 control program uses this instruction to determine the PDF array address that the cycle steal and PDF pointers point to and to determine the states of the sequence field, message counter field and the turnaround control bit. The scanner gates the contents of ICW input register bytes 12 and 13 to the general register specified by the R field.

INPUT X'4F' (ICW BYTES 14 AND 15)

The 3705 control program uses this instruction to determine the state of the status fields as shown on the chart for BSC or SDLC. The scanner gates the contents of ICW input register bytes 14 and 15 to the general register specified by the R field.



General Register Bit Pos.	Input 4B	Input 4C	Input 4E	Input 4F	
				BSC	SDLC
0.0	0	0	Cycle Steal Pointer—PDF Array Address Bit 8	Receive Line Signal Detect	Receive Line Signal Detect
0.1	0	0	Cycle Steal Pointer—PDF Array Address Bit 4	Format Exception	Idle Detected (15 consecutive SDLC zeros)
0.2	0	0	Cycle Steal Pointer—PDF Array Address Bit 2	Flush	Flush
0.3	0	0	Cycle Steal Pointer—PDF Array Address Bit 1	VRC or BCC Check	BCC Check
0.4	0	0	PDF Pointer—PDF Array Address Bit 8	Bad Flag or Pad	Flag Off Boundary
0.5	0	PDF Array Bit 0	1 PDF Pointer—PDF Array Address Bit 4	ACK Expected	Two Control Characters
0.6	0	PDF Array Bit 1	PDF Pointer—PDF Array Address Bit 2	Leading DLE Sequence Error	0
0.7	0	PDF Array Bit 2	PDF Pointer—PDF Array Address Bit 1	Length Check	Length Check
1.0	New Sync	PDF Array Bit 3	Sequence 0	Initial Status Bit 0	Control Exception (Rcv'd data in control frame)
1.1	Data Terminal Ready And Diag Wrap	PDF Array Bit 4	Sequence 1	Initial Status Bit 1	0
1.2	On Line Terminal Test Diagnostics	PDF Array Bit 5	RTS Turnaround Control	Initial Status Bit 2	0
1.3	0	PDF Array Bit 6	Sequence 2	Final Status Bit 3	Program Requested Interrupt on 'line idle detect' or 'Flag'
1.4	Extended PCF Bit 0	PDF Array Bit 7	0	Final Status Bit 4	0
1.5	Extended PCF Bit 1	PDF Array Bit 8	0	Final Status Bit 5	1 = Xmit Flag } After Transmission in Not turnaround 0 = Xmit Idle }
1.6	Extended PCF Bit 2	PDF Array Bit 9	Message Counter Bit 0	Final Status Bit 6	Xmit Pad Before Line Turnaround
1.7	Extended PCF Bit 3	PDF Array Bit 10	Message Counter Bit 1	Leading Graphics	Line Turnaround After Transmission

OUTPUT X'40' AND X'41'

Output X'40' loads an interface address in ABAR (attachment buffer address register) to the attachment base. When Output X'40' is executed in program levels 3 or 4, the attachment base gates the contents of the ICW work register to the ICW input register and the contents of the PDF array (selected by the PDF pointer) to the PDF in register where they are available to the control program by means of Input instructions X'44', '45', '47', '48', '49', '4A', '4B', '4C', '4E', and '4F'.

The control program must execute Output X'40' to initialize ABAR with an interface address associated with an installed type 3 scanner after the 3705 is powered on and before other inputs and outputs are issued to the scanner. Otherwise, an input/output check may occur.

Output X'41' sets the substitution control register bits in the attachment base and the bits in the high-speed select register (located in the scanner).

General Register (R)	Output X'40'			
0.0	*			
0.5	*			
0.6	Interface Address	Bit 0	Scanner	00 = 1 01 = 2 10 = 3 11 = 4
0.7		Bit 1		
1.0		Bit 2	LIB	010 = LIB 1 011 = LIB 2 100 = LIB 3
1.1		Bit 3		101 = LIB 4 110 = LIB 5
1.2		Bit 4		111 = LIB 6
1.3		Bit 5	Line	0 - F (hex)
1.4		Bit 6		
1.5		Bit 7		
1.6		Bit 8		
1.7	*			

General Register (R)	Output X'41'							
0.0	High Speed Select Reg							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0.7								
1.0	*							
1.1	*							
1.2	Substitution Ctrl Reg							
1.3	Bit 1	Bit 2	Bit 3	Bit 4				
1.4								
1.5								
1.6	*							
1.7	*							

*Bit Position Unused

OP Reg Content for Output X'40'

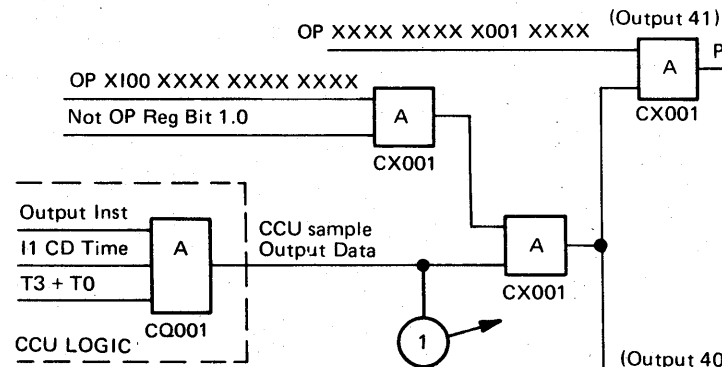
0100 0XXX 0000 0100

R field

OP Reg Content for Output X'41'

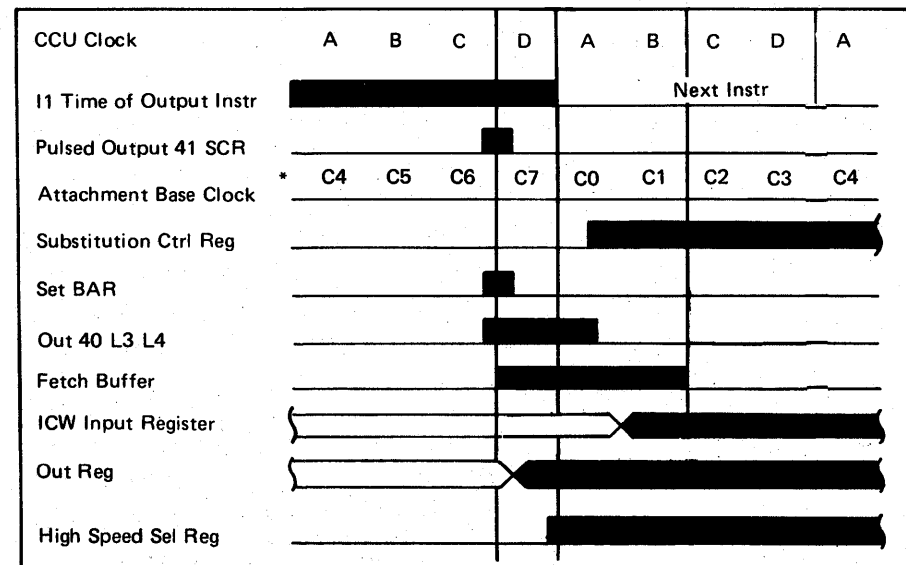
0100 0XXX 0001 0100

1.0

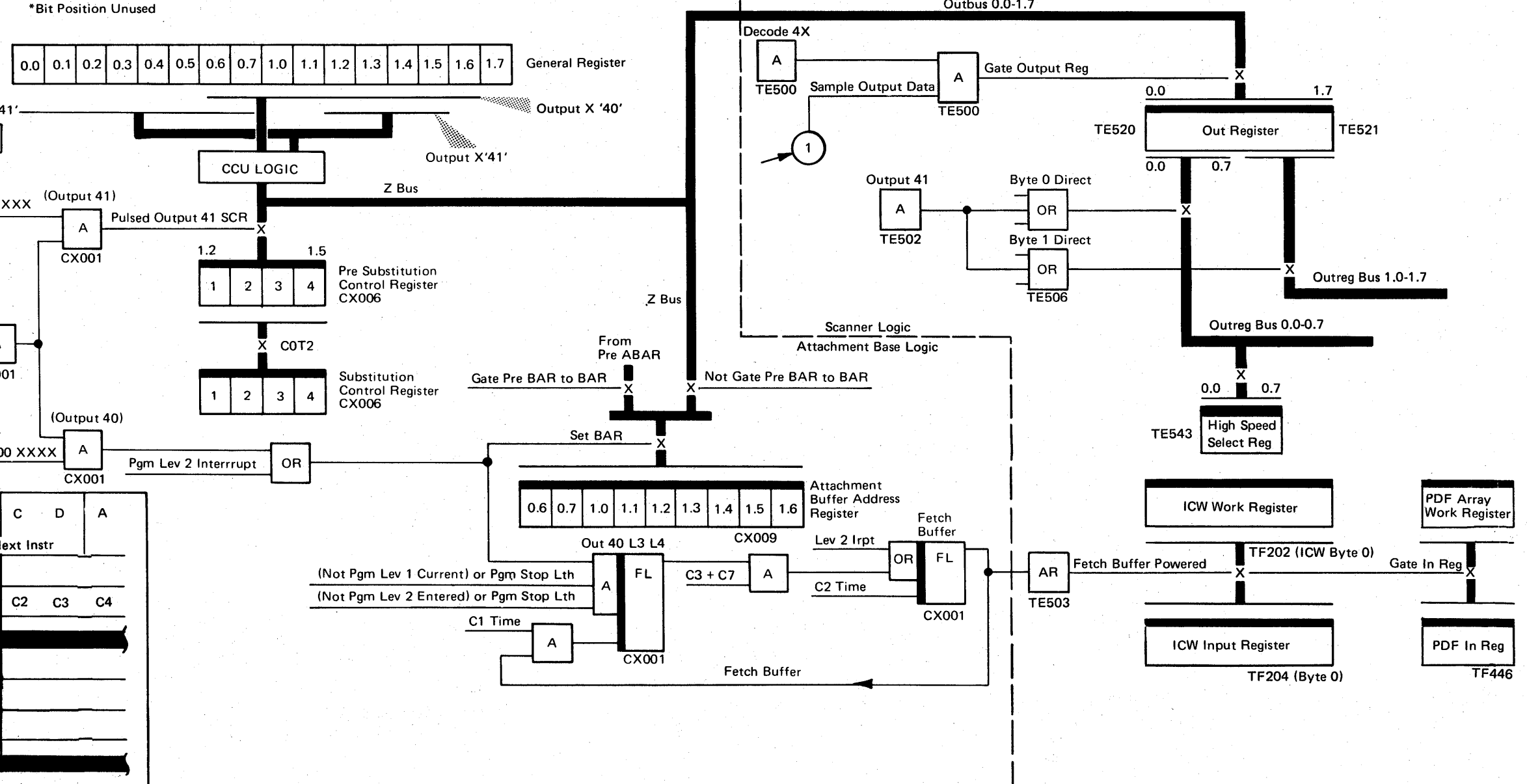


Output Timings

FET Storage **



** For bridge storage timing, see B-160

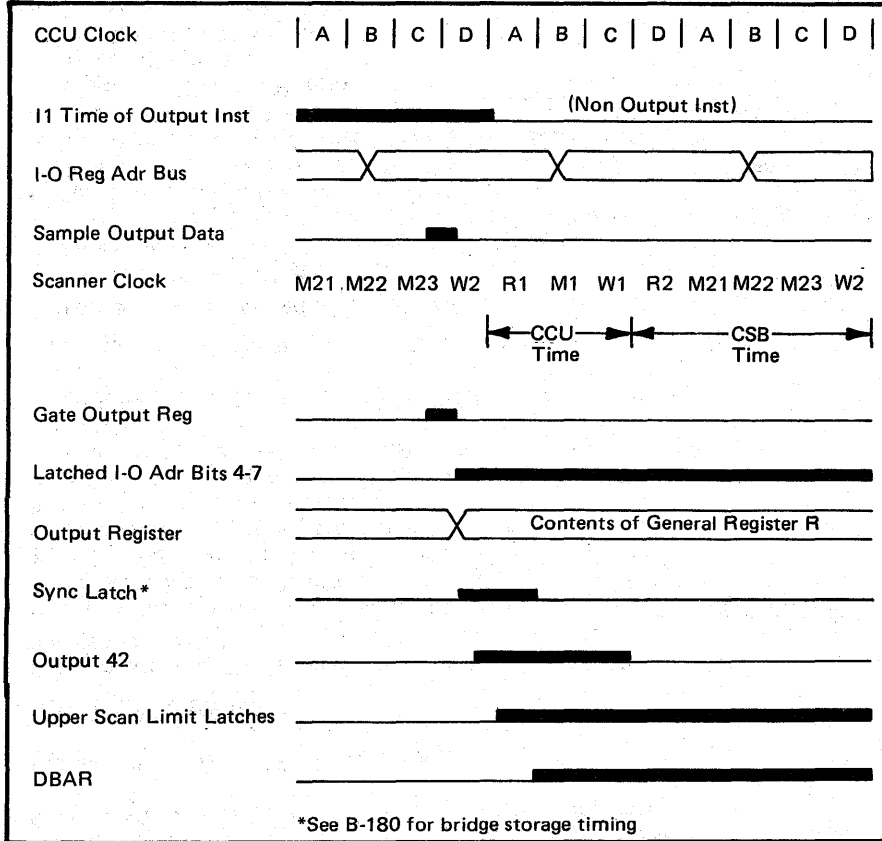


OUTPUT X'42' (DBAR/SCAN LIMITS)

The 3705 control program uses this instruction to set the contents of the upper scan limits and DBAR (diagnostic buffer address register) in the selected scanner. The interface address in the attachment buffer address register selects the scanner. (See Note).

Normally the scanner traps the ICW address in DBAR when an ICW work register, array check LIB select error, CS parity error, CSAR even parity, or CSAR address exception occur. The level 1 routine of the control program executes an Input X'42' to obtain the address of the failing line from DBAR. The diagnostic program uses Output X'42' to set DBAR only to verify the correct operation of DBAR and the Input X'42' instruction.

Output Timings—FET Storage*

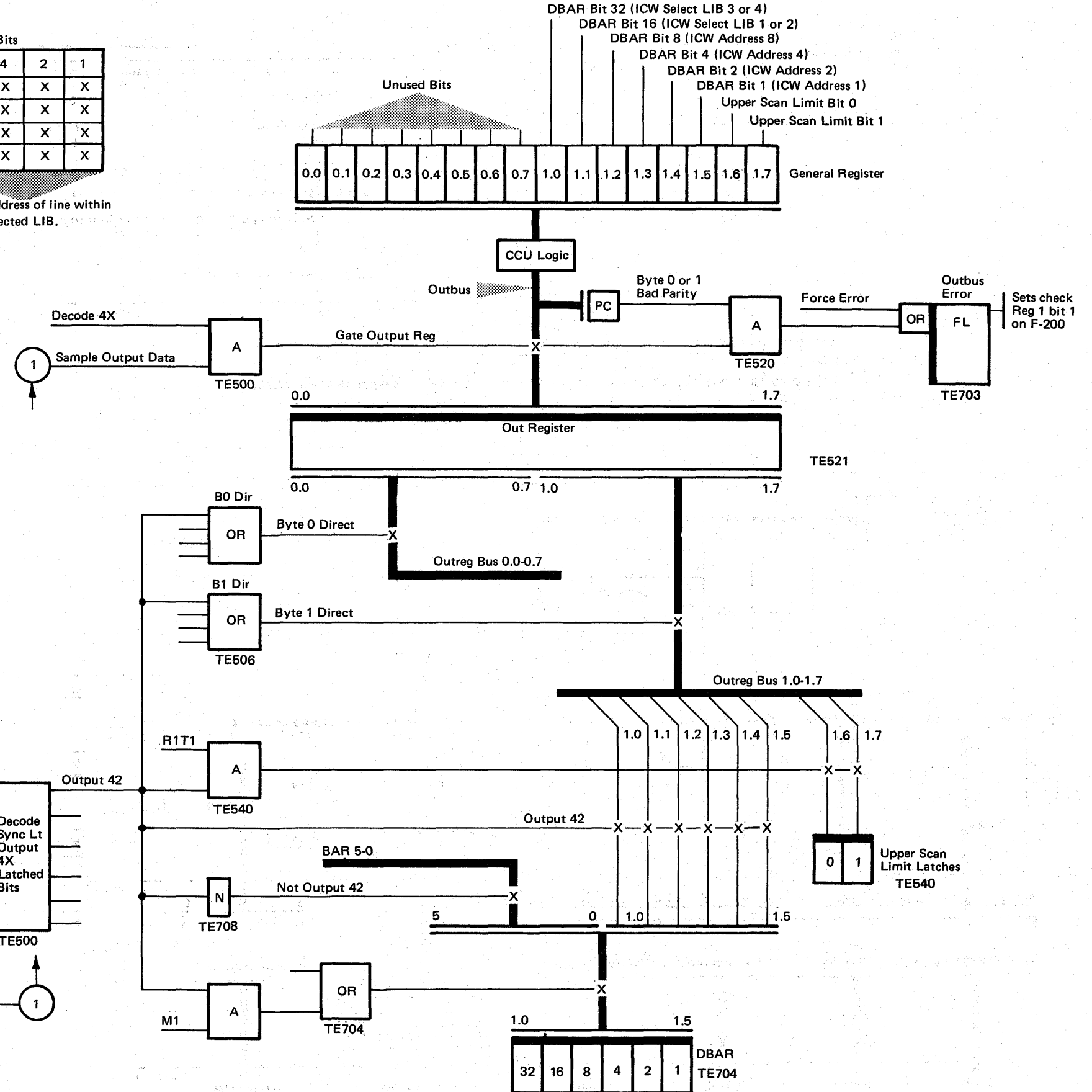


*See B-180 for bridge storage timing

*The scanner sets the sync latch whenever the scanner decodes an Output X'41' thru X'4F' instruction. When set, the sync latch allows the scanner to execute the Output X'4X' instruction the next CCU time.

DBAR Bits		32	16	8	4	2	1
LIB 1		0	0	X	X	X	X
LIB 2		0	1	X	X	X	X
LIB 3		1	0	X	X	X	X
LIB 4		1	1	X	X	X	X

Hex address of line within the selected LIB.



Note: The scan limit select option is not applicable to type 3HS scanner operation. Therefore, upper scan limit bits 0 and 1 (Output X'42' general register bits 1.6 and 1.7, respectively) must be set to zero.

OUTPUT X'43' (CONTROL)

The 3705 control program uses this instruction to set or reset various control functions in a type 3 scanner. The interface address in the attachment buffer address register selects the scanner. When Output X'43' is executed, the bit configuration in the general register specified by the R field determines which control functions are set or reset.

SELECTIVE LIB RESET

A set function (0.0=1), with a 1 in the associated disable LIB position, sets the 'LIB X disabled' latch. This causes a selective LIB reset to each line attached to LIB X when the scan counter selects that line interface. 'LIB X disabled' also inhibits the setting of any of the check register positions. The reset continues until the 3705 control program resets the 'LIB X disabled' latch by the reset function (0.1=1) and a 1 in the associated disable LIB position, leaving LIB X *enabled*. For a summary of the reset actions see **2** and **3**.

SELECTIVE SCANNER RESET

The set function (0.0=1) with bit 1.6=1 *resets* the 'CSB enable' latch. This forces the reset actions in **1**, **2** and **3**. As each line interface is selected by the scan counter, the line interface is reset. Thus, a complete scan period is required to reset the entire scanner. The reset ends when the 'CSB enable' latch is turned on by the *reset* function (0.1=1) with bit 1.6=1 and the scanner is *enabled*.

SUMMARY OF RESET ACTIONS

ICW Test Mode **3**

In test mode, the ICW is treated as storage and only output instructions are allowed to change the ICW bits.

- Forces 'control out A' and 'control in A'—TF626.
- Forces 'control out B' and 'control in C'—TF604.
- Holds 'CSB data out 1-7' to 0—TF424.
- Inhibits 'B7 bit svc req' from generating 'gated bit svc or I and A rst'—TF625.
- Sets display register position 8—TF623.
- Alters the outreg gating for Output X'44', X'45', X'46', X'4F'.
- Inhibits: 'set cs req latch'—TE341, 'set L2 bid'—TE401, 'CSB wants a prior reg'—TE401.
- Inhibits the ROS and transparency ROS functions—TF816.

ICW and Array Reset **2** (I and A Reset)

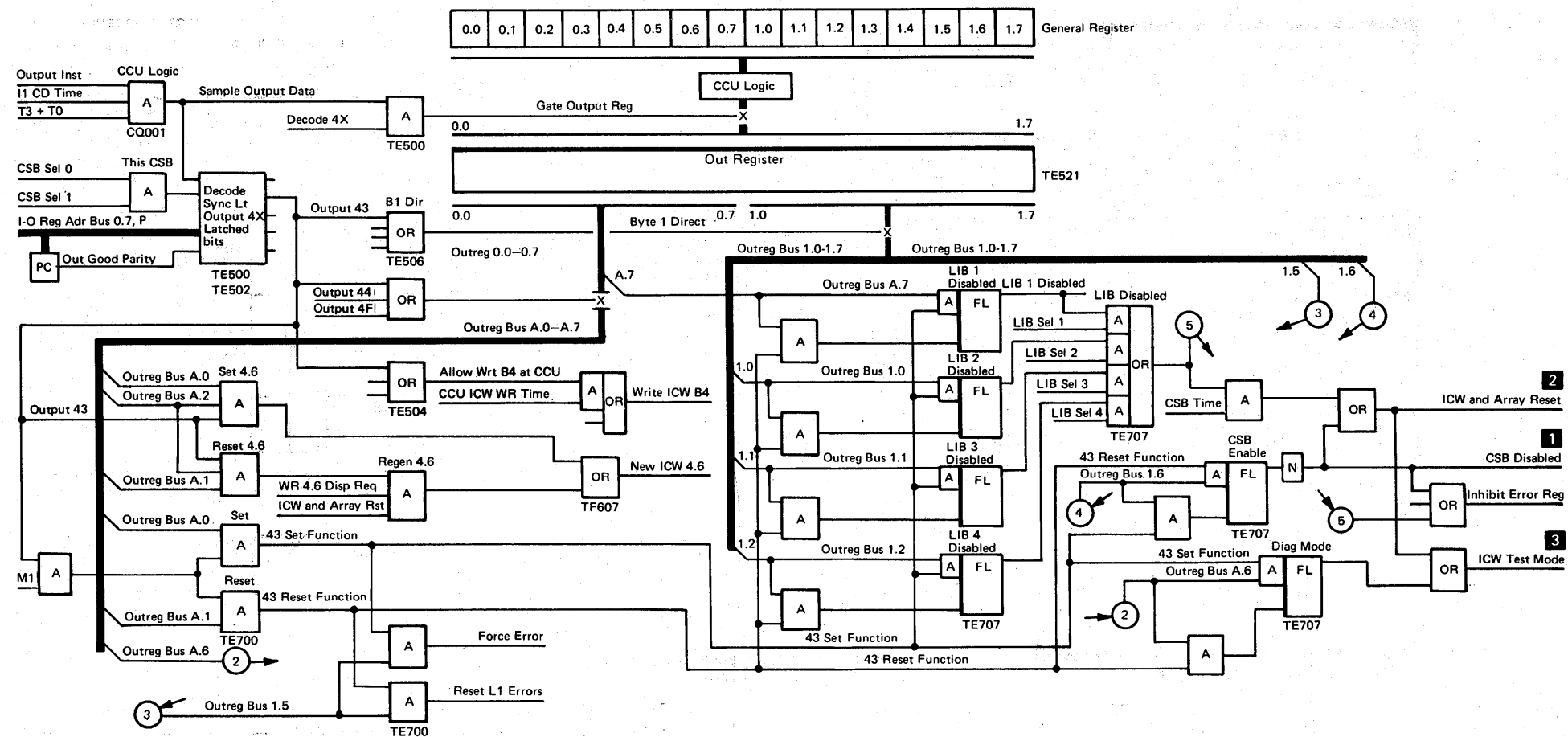
Affective for LIB disabled or CSB disabled.

- Forces ICW TEST Mode.
- Forces 'write at W2 T1 T2 time for all ICW bytes.
- Forces 'gated bit svc or I and A rst'—TF625 (instead of by B7 bit svc req or diag bit svc).
- Sets PCF 0-3 to X'0', (No OP)—TF505.
- Sets ICW bits: 0.4 (not L2 bid)—TF221, 4.5 (last line state)—TF602.
- Initializes BCC in ICW bytes 10 and 11—TF305, TF315.
- Resets ICW bits: 0.1 (svc req)—TF221, 0.7 (trace)—TF221, 4.2-4.4 and 4.7, 5.0 (ones counter)—TF603, 4.6 (display request) TF607, 5.5-5.7 (diag 0-1, ext clk)—TF607, 6.5 (cs valid)—TE343.
- Sets ICW byte 12 to ones (CS and PDF pointers to array) TF480.
- Forces 'write array'—TE345.
- Sets 'select PDF pointer' latch—TE344.
- Inhibits 'strobe array WR' from loading PDF array WR—TE344.

Initialize ECWs for the affected line interfaces
Resets PDF array for affected line interfaces

CSB Disable **1**

- Forces 'ICW and Array Reset' and 'ICW Test Mode'.
- Resets: Upper scan limit latches—TE540, 'CS busy' latch—TE240, 'CS request' latch—TE240.
- Resets 'CBAR bits 0-1' latches—TE544.
- Inhibits set of: 'LIB sel error', 'adr excep error', 'bad data', 'SAR even parity', 'In reg error', 'pri req error', and 'BAR error' latches—TE703.
- Inhibits 'bid level 1'—TE706.



Output Reg Pos	Position Name	Set Function (0.0 = 1)	Reset Function (0.1 = 1)
0.0	Set Function	A 1 causes the set function for output positions 0.2 through 1.6 when the corresponding bit is 1. This bit should not be 1 if 0.1 is 1.	Must be a 0 if the reset function is on (bit 0.1 = 1).
0.1	Reset Function	A 1 causes the reset function for output positions 0.2 through 1.6 when the corresponding bit is 1. This bit should not be 1 if 0.0 is 1.	Must be a 0 if the set function is on (bit 0.0 = 1).
0.2	Display Request	A 1 sets ICW bit 4.6. A 0 does not change ICW bit 4.6.	A 1 resets the ICW bit 4.6. A 0—no change.
0.3	Not used	No effect.	No effect.
0.5			
0.6	Diagnostic Test Mode	A 1 sets the diagnostic mode latch. See summary 3 in text. A 0 has no effect.	A 1 resets the diagnostic mode latch. A 0—no change.
0.7	Disable LIB pos 1	A 1 sets the 'LIB 1 disabled' latch. When LIB 1 is selected, 'ICW and array reset' and 'ICW test mode' lines generate reset, inhibit, and set functions. See summaries 2 3 in text. A 0 has no effect.	A 1 <i>enables</i> LIB 1 by resetting the 'LIB 1 disabled' latch. A 0 has no effect.
1.0	Disable LIB pos 2	Same as 0.7 for LIB 2.	Same as 0.7 for LIB 2.
1.1	Disable LIB pos 3	Same as 0.7 for LIB 3.	Same as 0.7 for LIB 3.
1.2	Disable LIB pos 4	Same as 0.7 for LIB 4.	Same as 0.7 for LIB 4.
1.3	Not used	No effect.	No effect.
1.4			
1.5	Type 2 Scanner N L1 Request	A 1 sets all 21 latches in the check register and causes a level 1 interrupt. A 0 has no effect.	A 1 resets the check register latches and the level 1 interrupt. A 0 has no effect.
1.6	Disable Interrupt Requests	A 1 resets the 'CSB enable' latch to <i>disable</i> the scanner. 'CSB disabled', 'ICW and array reset', and 'ICW test mode' lines generate reset, inhibit, and set functions. See summaries 1 2 3 in text.	A 0 has no effect. Note: The 3705 control program <i>must</i> set the 'CSB enable' latch in each scanner before they may be initialized.
1.7	Not used	No effect.	No effect.

OUTPUT X'44' (SCF/PDF)

The 3705 control program uses this instruction (1) to reset the following SCF (secondary control field) bits in the ICW: SDLC abort detected, service request, overrun/underrun, modem check, end of message, (2) to set SCF bit 4 (not L2 bid), (3) to set or reset SCF bit 0.6 (program flag) and SCF bit 0.7 (trace control), and (4) to output data to the PDF array in the selected scanner. The interface address in the attachment buffer address register selects the scanner and the associated ICW.

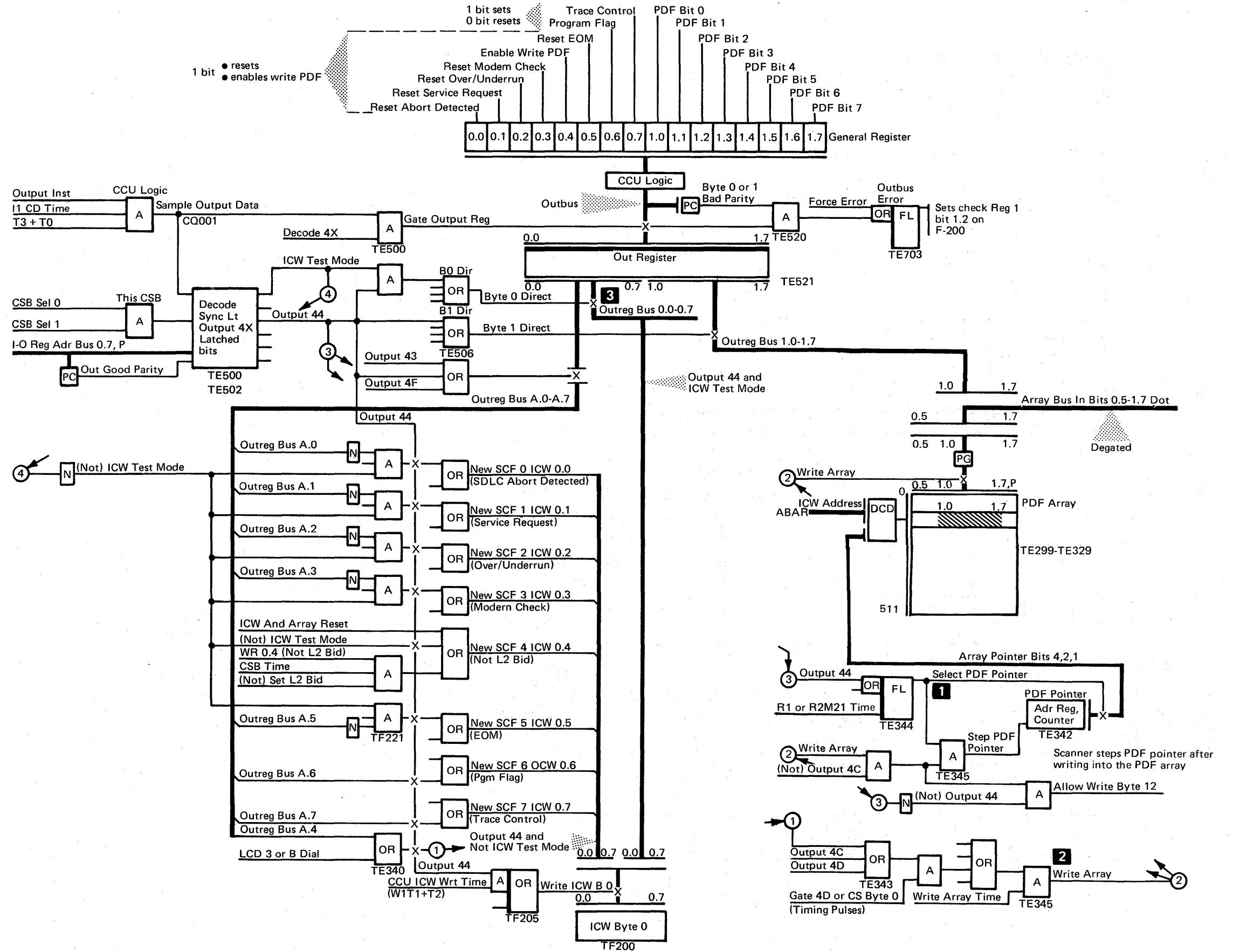
NORMAL OPERATION (NOT ICW TEST MODE)

'Output 44' gates outreg 0.0-0.7 to the alternate bus and outreg 1.0-1.7 directly to the outreg bus 1.0-1.7. Alternate bus bits set/reset associated SCF bits. 'Output 44' always sets SCF 4 (not L2 bid) when not in ICW test mode, while 'set L2 bid' resets SCF 4.

'Output 44' turns on the 'select PDF pointer' latch 1. This latch gates the PDF array pointer bits to the decode circuit where the value of these bits combines with the value of the ICW address bits (from ABAR) to select the buffer associated with the selected ICW interface. Alternate bus bit 0.4 or a dial LCD, gated by 'output 44', turns on 'write array' 2 that (1) writes the PDF data (on outreg bus 1.0-1.7) into the selected PDF array buffer position then (2) steps the PDF pointer by 1. However, 'output 44' inhibits writing the incremented count to ICW byte 12. The scanner loads the PDF data into PDF array positions 1.0-1.7 and places zeros in positions 0.5-0.7 to indicate that the contents is data.

ICW TEST MODE

When in ICW test mode (see F-270), 'output 44' gates outreg 0.0-0.7 directly to outreg bus 0.0-0.7 3. The diagnostic program uses this means to control setting/resetting the SCF bits in ICW byte 0. 'ICW test mode' also inhibits the regeneration of the old SCF bits from the ICW work register. The loading of the PDF data is the same as for normal operation.



OUTPUT X'45' (LCD/PCF/EPCF)

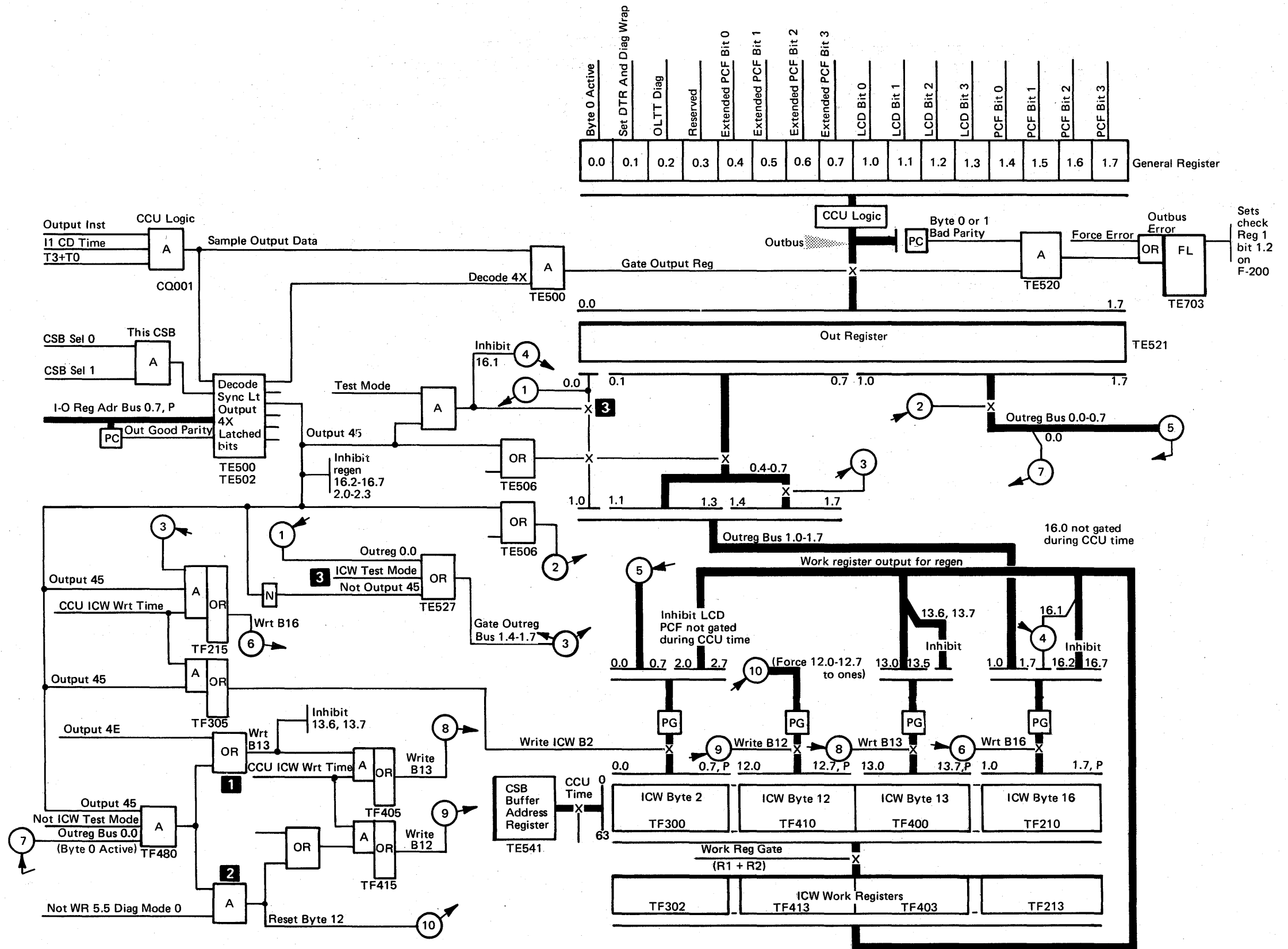
The 3705 control program uses this instruction to set the LCD and PCF in ICW byte 2 and to set the extended PCF in ICW byte 16 if "Byte 0 Active" (0.0) is =1. The interface address in the attachment buffer address register selects the scanner and the associated ICW.

NORMAL OPERATION (NOT ICW TEST MODE)

'Output 45' gates outreg 0.1-0.7 to outreg bus 1.1-1.7 if outreg 0.0=1 and gates the LCD and PCF in outreg 1.0-1.7 to outreg bus 0.0-0.7. Write ICW B2' then sets the LCD and PCF bits in ICW byte 2 while 'Wrt B16' sets bits 1.0-1.7 in ICW byte 16. If outreg bus 0.0=1 (Bit 0 active), the scanner resets bits 13.6 and 13.7 (cs message count) **1** and resets the cs pointer and PDF pointer in ICW byte 12 to all ones **2**.

ICW TEST MODE

When in ICW test mode (see F-270), 'output 45' gates outreg bits 0.0-0.7 to outreg bus 1.0-1.7 to test ICW byte 16. **3**



Note: Output X'45' timing is similar to that on F-260.

OUTPUT X'46' (SDF)

The 3705 control program uses this instruction (1) to set the SDF bits in ICW bytes 3 and 4 and (2) to indirectly set 5.4 (NRZI control), 5.5 (diag mode 0), 5.6 (diag mode 1), and 5.7 (external clock) when a set mode (PCF state 1) is executed. The interface address in the attachment buffer address register selects the scanner and the associated ICW.

NORMAL OPERATION (NOT ICW TEST MODE)

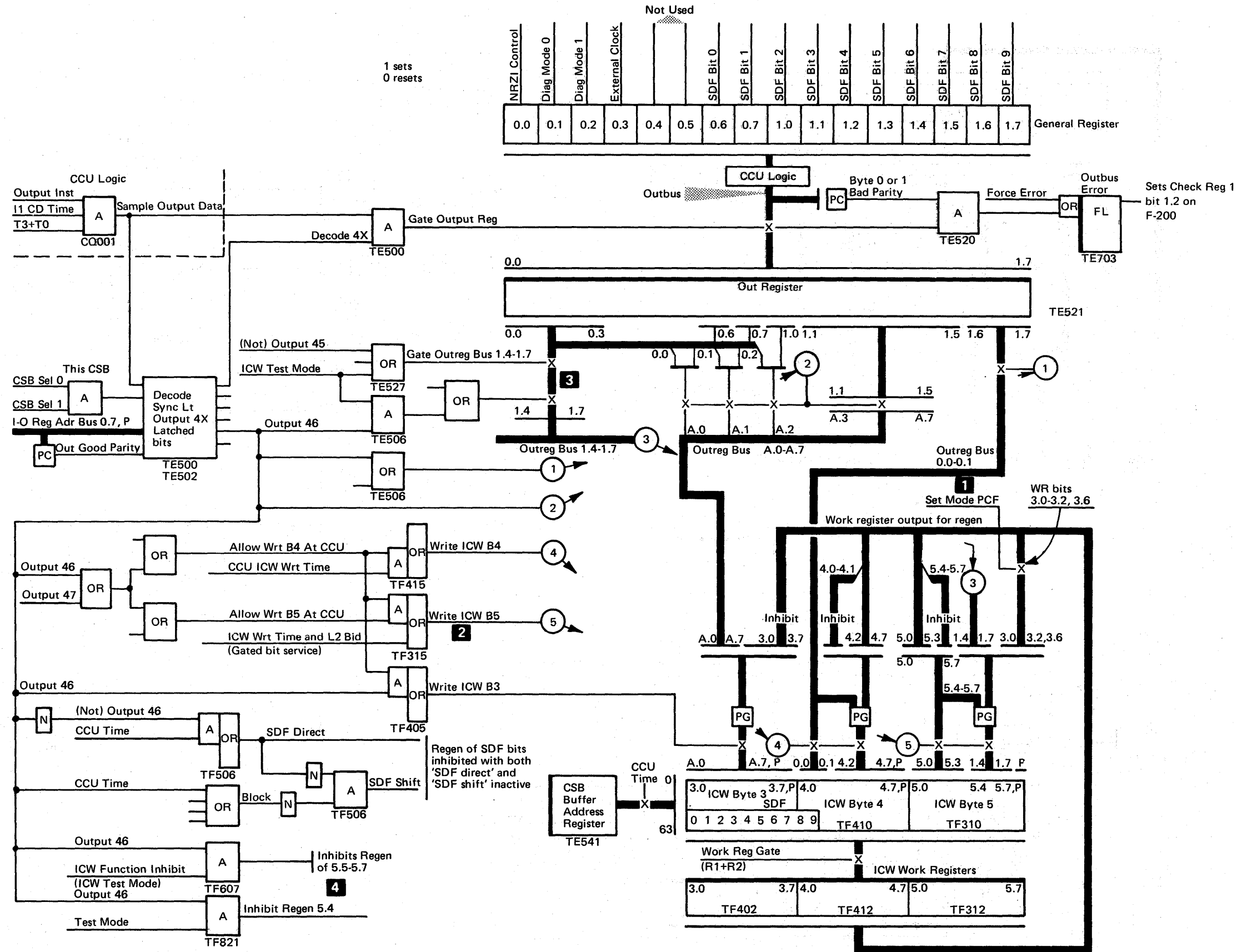
'Output 46' gates SDR bits 0-7 from outreg 0.6, 0.7 and outreg 1.0-1.5 to the alternate bus and SDR bits 8 and 9 from outreg 1.6-1.7 to outreg bus 0.0, 0.1. 'Write ICW B3' and 'write ICW B4' then set the SDF bits into ICW bytes 3 and 4.

Setting ICW Byte 5 During Set Mode

'Output 46' gates the SDR bits from outreg 0.0 (NRZI control), 0.1 (diag mode 0), 0.2 (diag mode 1), 1.1 (diag mode), 1.2 (DTR), 1.3 (sync mode), 1.4 (external clock), 1.5 (DRS) to the alternate bus and gates the SDR bits from outreg 1.6 (osc select bit 1) and 1.7 (osc select bit 2) to outreg bus 0.0-0.1. 'Write ICW B3' and 'Write ICW B4' then set the SDF bits into ICW bytes 3 and 4. When a set mode (PCF X'1') is executed (1), 'write ICW B5' sets work register bits 3.0 (NRZI control), 3.1 (diag mode 0), 3.2 (diag mode 1), and 3.6 (external clock) into 5.4-5.7. 'Gated bit service' forces 'write ICW B5' (2) during CSB time when PCF X'1' is active.

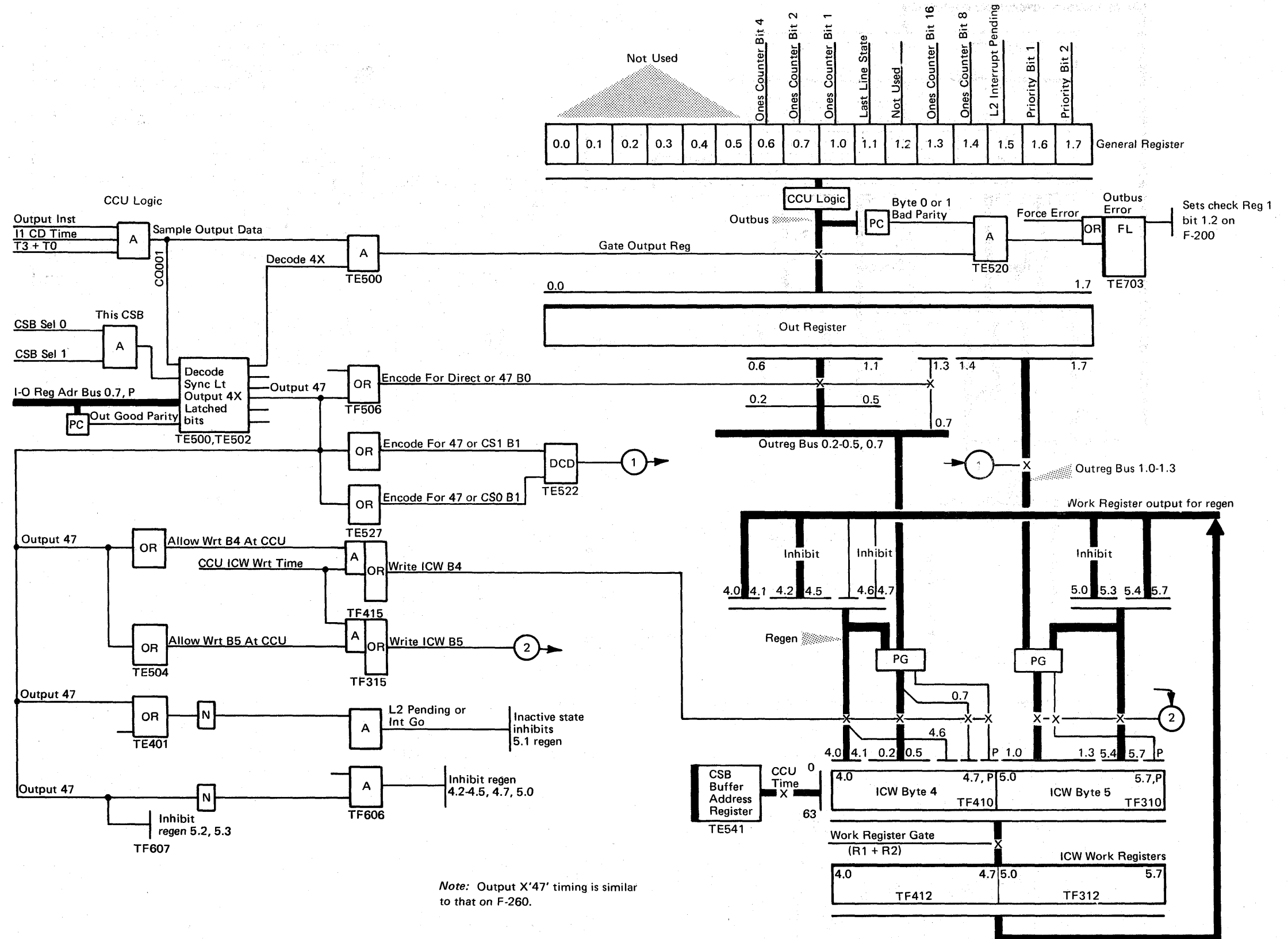
ICW TEST MODE

When in ICW test mode (see F-270), 'output 46' gates outreg bits 0.0 (NRZI control), 0.1 (diag mode 0), 0.2 (diag mode 1), and 0.3 (external clock) to outreg bus 1.4-1.7 (3) and then 'write ICW B5' sets them into 5.4-5.7 (4) while inhibiting the regen of 5.4-5.7 (4). ICW bytes 3 and 4 are tested in the normal manner as described above.



OUTPUT X'47' (MISC ICW BITS)

The 3705 control program uses this instruction to set the 'last line state' bit, the content of the ones counter, and the priority bits in ICW bytes 4 and 5. The interface address in the attachment buffer address register selects the scanner and the associated ICW.



OUTPUT X'48', X'49', X'4A'

The interface address in the attachment buffer address register selects the scanner and the associated ICW for the above output instructions.

Output X'48' (CS CONTROL AND BYTE COUNT)

The 3705 control program uses this instruction (1) to set the extended address bits X.4-X.7, CS valid, data chain flag, and message chain flag bits in ICW byte 6 and (2) to set the contents of the cycle steal byte-count field in ICW byte 7. When initializing a cycle steal operation, the control program executes an Output X'48' instruction after executing an Output X'49' instruction.

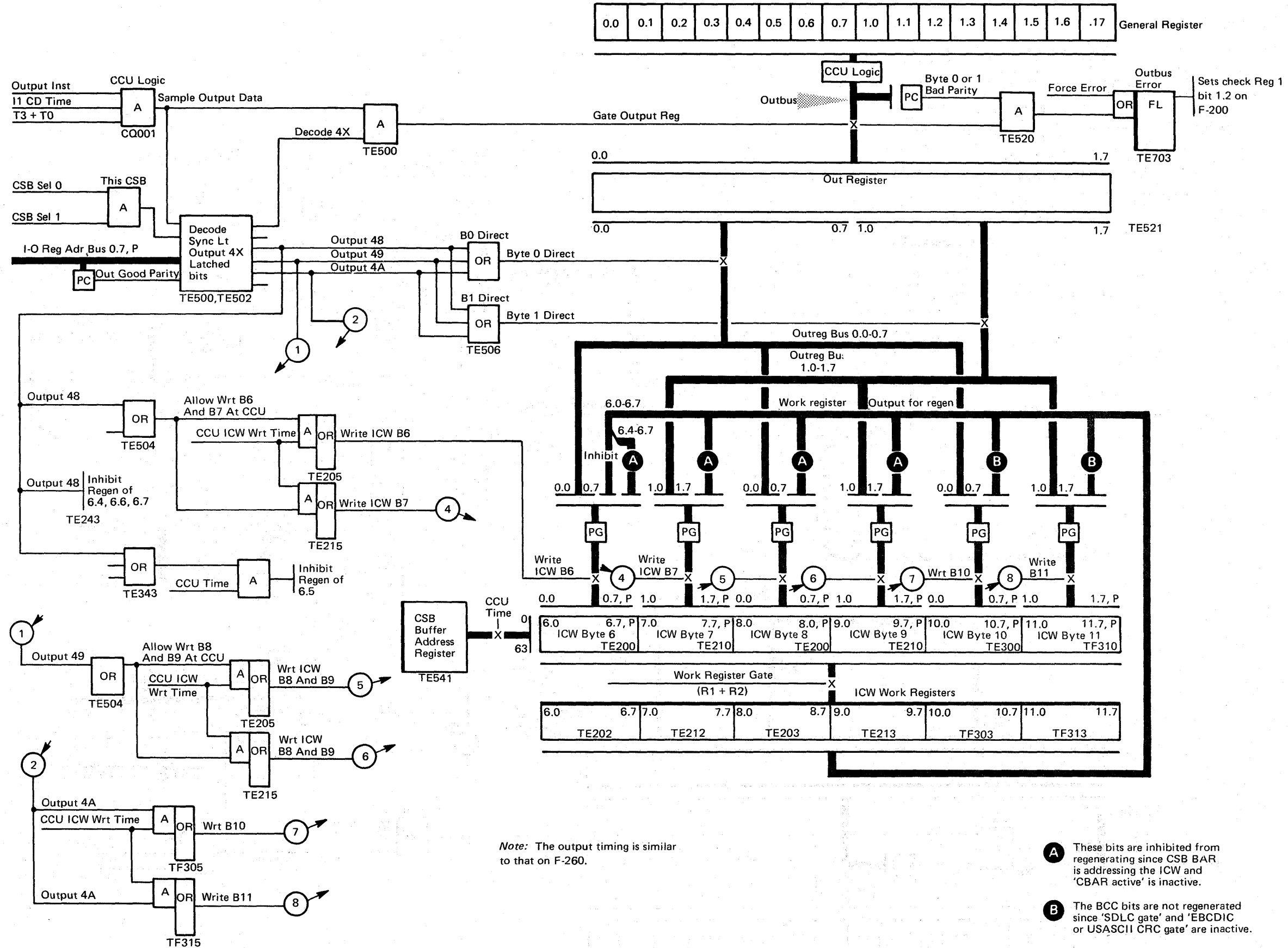
OUTPUT X'49' (CYCLE STEAL ADDRESS REGISTER)

The 3705 control program uses this instruction to set the storage address of the first byte of data that the scanner is to cycle steal (to/from) into CSAR (located in ICW bytes 8 and 9). Storage is addressed from the address formed by combining the extended address bits X.6 and X.7 with the CSAR bits. When initializing a cycle steal operation, the control program executes an Output X'49' instruction before the Output X'48' instruction.

OUTPUT X'4A' (BLOCK CHECK CHARACTER)

The 3705 control program may use this instruction to set the contents of the BCC in ICW bytes 10 and 11. This is normally not done since the BCC is accumulated as data is transmitted or received for SDLC, BSC EBCDIC, and BSC USASCII.

General Register Bit Pos.	Output X'48'	Output X'49'	Output X'4A'
0.0	CS Adr X.4	CSAR Bit 0.0	BCC Bit 0
0.1	CS Adr X.5	CSAR Bit 0.1	BCC Bit 1
0.2	CS Adr X.6	CSAR Bit 0.2	BCC Bit 2
0.3	CS Adr X.7	CSAR Bit 0.3	BCC Bit 3
0.4	0 Reserved	CSAR Bit 0.4	BCC Bit 4
0.5	CS Valid	CSAR Bit 0.5	BCC Bit 5
0.6	Data Chain Flag	CSAR Bit 0.6	BCC Bit 6
0.7	Message Chain Flag	CSAR Bit 0.7	BCC Bit 7
1.0	CS Count Bit 128	CSAR Bit 1.0	BCC Bit 8
1.1	CS Count Bit 64	CSAR Bit 1.1	BCC Bit 9
1.2	CS Count Bit 32	CSAR Bit 1.2	BCC Bit 10
1.3	CS Count Bit 16	CSAR Bit 1.3	BCC Bit 11
1.4	CS Count Bit 8	CSAR Bit 1.4	BCC Bit 12
1.5	CS Count Bit 4	CSAR Bit 1.5	BCC Bit 13
1.6	CS Count Bit 2	CSAR Bit 1.6	BCC Bit 14
1.7	CS Count Bit 1	CSAR Bit 1.7	BCC Bit 15



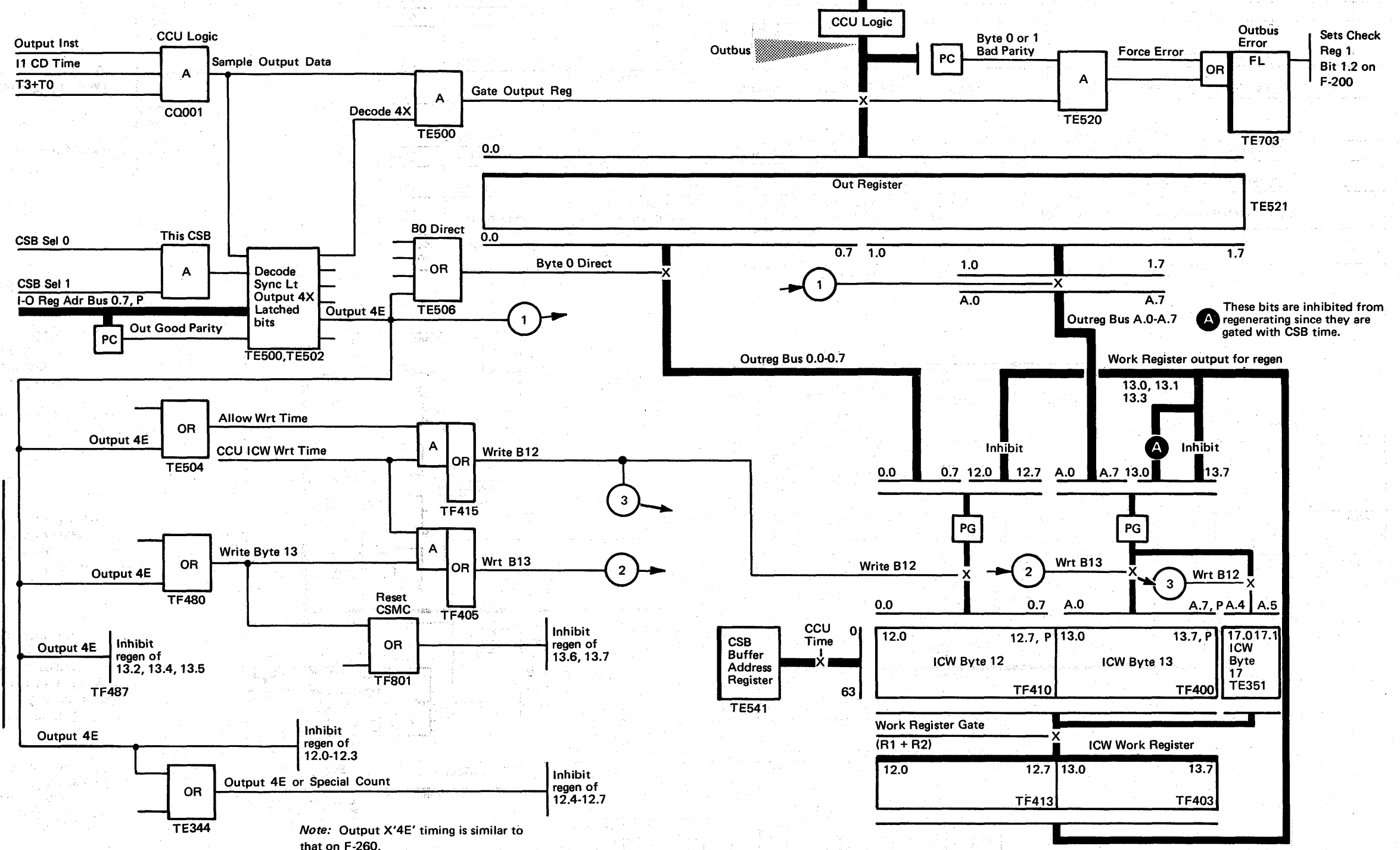
- A** These bits are inhibited from regenerating since CSB BAR is addressing the ICW and 'CBAR active' is inactive.
- B** The BCC bits are not regenerated since 'SDLC gate' and 'EBCDIC or USASCII CRC gate' are inactive.

OUTPUT X'4E' (CS/PDF POINTERS-ICW CONTROL)

The 3705 control program uses this instruction to set the contents of the CS pointer address, the PDF pointer address, the sequence field, the CS message counter, and the RTS turnaround control bit in ICW bytes 12 and 13. For type 3HS scanner operation, the high-order bit of the CS pointer address and the PDF pointer address are set in ICW byte 17 (ICW controls extended). The interface address in the attachment buffer address register selects the scanner and the associated ICW.

CS Pointer Bit 8	CS Pointer Bit 4	CS Pointer Bit 2	CS Pointer Bit 1	PDF Pointer Bit 8	PDF Pointer Bit 4	PDF Pointer Bit 2	PDF Pointer Bit 1	Sequence 0	Sequence 1	RTS Turnaround Control	Sequence 2	CS Pointer Bit 16	PDF Pointer Bit 16	CS Message Counter Bit 0	CS Message Counter Bit 1
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

General Register



Note: Output X'4E' timing is similar to that on F-260.

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OUTPUT X'4F' STATUS

The 3705 control program uses this instruction (1) to set/reset the status in ICW byte 15, (2) to reset ICW byte 14 bits 0.0, 0.1, 0.3, 0.4, 0.6, and 0.7 if the corresponding bit is a one (a zero has no effect), and (3) to set/reset ICW byte 14 bits 0.2 and 0.5. The interface address in the attachment buffer address register selects the scanner and associated ICW.

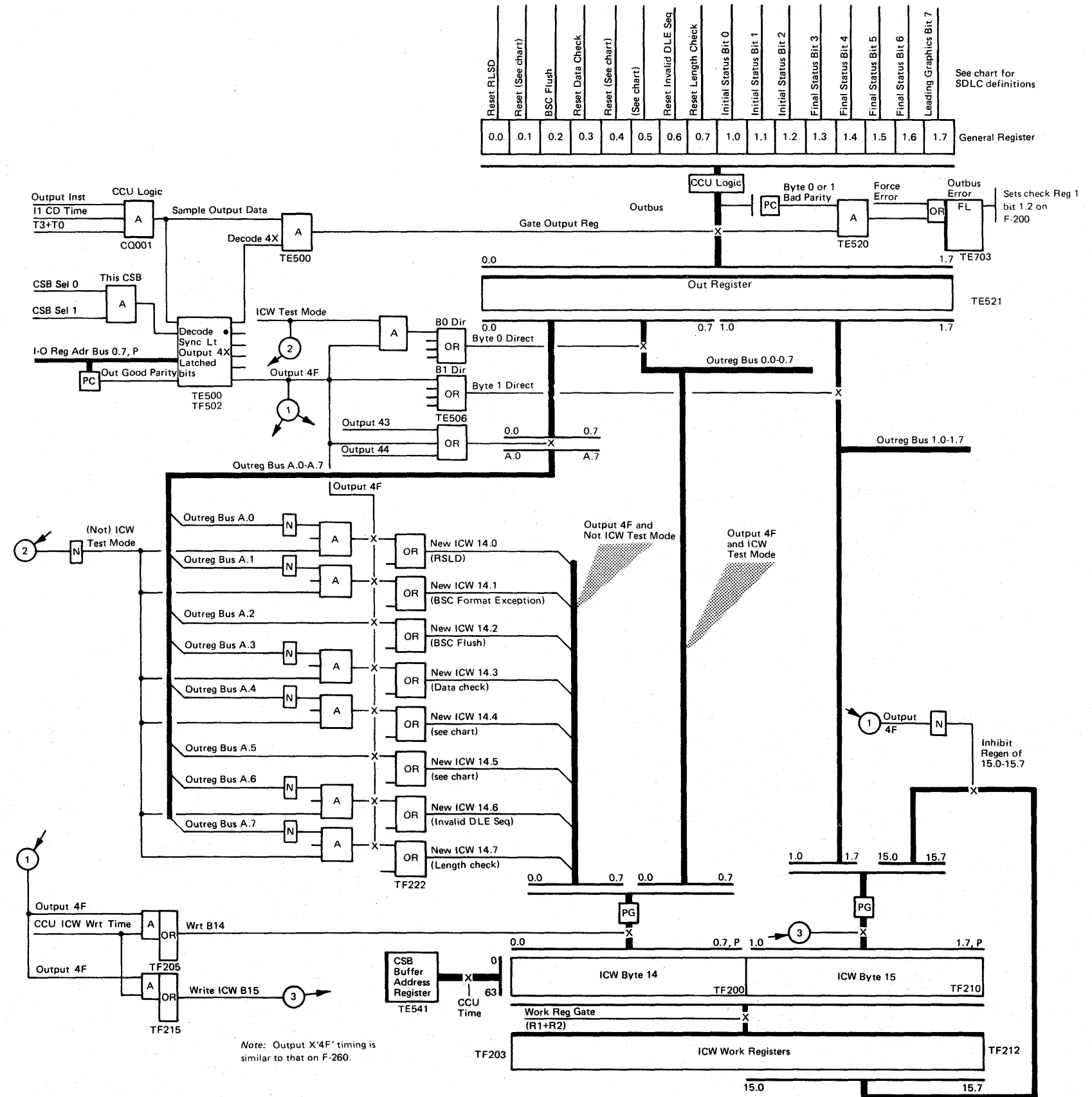
NORMAL OPERATION (NOT ICW TEST MODE)

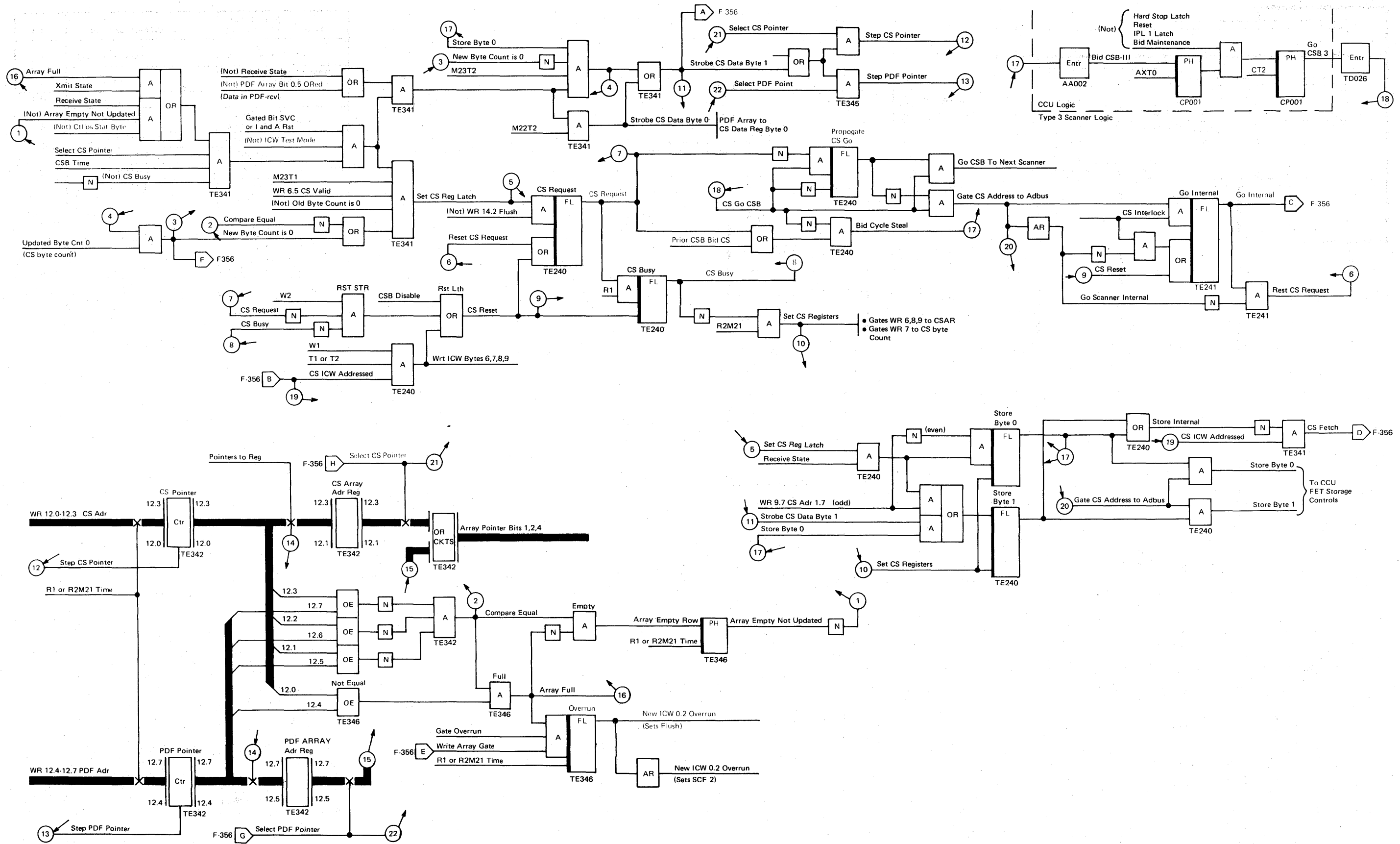
'Output 4F' gates outreg 0.0-0.7 to the alternate bus and outreg 1.0-0.7 directly to outreg bus 1.0-1.7. Alternate bus bits set/reset the corresponding bits in ICW byte 14 (1). The status bits that are 1s (on outreg bus 1.0-1.7) set the corresponding bits in ICW byte 15. Those status bits that are 0s reset the corresponding bits in ICW byte 15 (2).

ICW TEST MODE

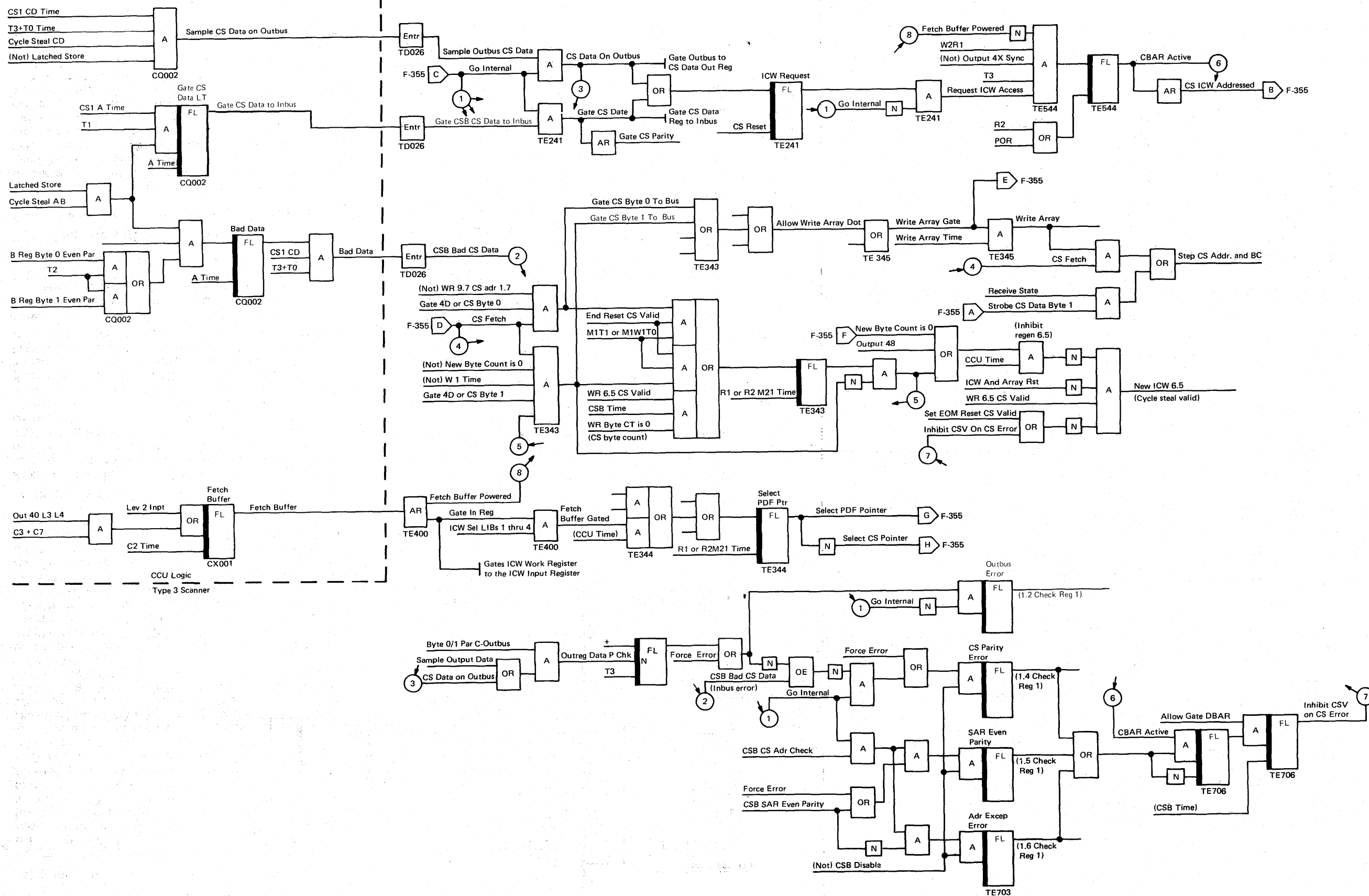
When in ICW test mode (see F-270), 'output 4F' gates outreg 0.0-0.7 directly to outreg bus 0.0-0.7 (3). The diagnostic program uses this means to set/reset the bits in ICW byte 14. 'ICW test mode' also inhibits the regeneration of the old bits from the ICW byte 14 work register (4).

General Register Bit Pos.	BSC	SDLC
0.0	Reset RLSD	Reset RLSD
0.1	Reset BSC Format exception	Reset idle detected
0.2	Set/reset flush	Set/reset flush
0.3	Reset data check	Reset data check
0.4	Reset bad pad/flag	Reset flag off boundary
0.5	Set/reset ACK expected	Set/reset two control characters
0.6	Reset invalid DLE sequence	Reset invalid DLE sequence
0.7	Reset length check	Reset length check
1.0	Initial status bit 0	0 (except for diagnostics)
1.1	Initial status bit 1	0 Reserved
1.2	Initial status bit 2	0 Reserved
1.3	Final status bit 3	Prog Req Irpt on idle defect or flag
1.4	Final status bit 4	Use two flags
1.5	Final status bit 5	1=xmit flag after xmit 0=xmit idle if no turn
1.6	Final status bit 6	Xmit Pad before line turnaround
1.7	Leading graphics bit 7	Line turnaround after transmission





CYCLE STEAL DATA FLOW (PART 2)



Cycle Steal Operation —Transmit

Introduction

During a transmit operation, the scanner transfers data from the storage to the PDF array by means of cycle stealing. Cycle stealing normally transfers two bytes at a time. When CSAR (cycle steal address register) initially addresses an odd storage location (CSAR bit 1.7=1) the scanner transfers data byte 1 to the PDF array and then increments CSAR to an even address. All subsequent data is transferred two bytes at a time.

The CS pointers determine which of the eight buffers (16 buffers for the type 3HS scanner) associated with the selected ICW will receive each transferred data byte. The initial state of the CS and PDF pointers is set by the 3705 control program (Output X'4E') or is reset to X'F' by an Output X'45' when the EPCF state is set. The scanner increments the CS pointer as each data byte is loaded into the PDF array buffer.

data byte from the PDF array buffers to the SDF when the "tag" is detected. The PDF pointers determine which buffer transfers the data byte to the SDF. The scanner increments the PDF pointer as each data byte transfers to the SDF.

The scanner initiates a cycle steal request to fetch two more bytes of data whenever two buffers of the PDF array that is associated with the selected ICW are empty. The scanner tests the states of the CS and PDF pointers to determine when two buffers are empty. See the "CS and PDF Pointer Sequence" chart on F-380.

Scanner Tests for Empty Buffers

At each 'bit service request' (except when the array is full, the PDF pointer is selected, or CS is busy) the scanner steps the CS pointer by 1 and then compares CS pointer bits 12.1-12.3 with PDF pointer bits 12.5-12.7 (see Note 1). An unequal condition indicates that there are at least two empty buffers so a cycle steal is requested to transfer two bytes of data to the empty buffers. An equal condition indicates that the buffers are either full or empty and a second test is made. The scanner compares CS pointer bit 12.0 with PDF pointer bit 12.4 (see Note 2) and, if they are equal, the array is empty. If they are not equal, the array is full.

Notes:

1. For the type 3HS scanner, CS pointer bits 12.0-12.3 are compared with PDF pointer bit 12.4-12.7.
2. For the type 3HS scanner, CS pointer bit 17.0 is compared with PDF pointer bit 17.1.

Cycle Steal Operation—Transmit

The keying numbers refer to the diagram on this page and F-370.

The 3705 control program sets ICW bytes 8 and 9 with the storage address for the first byte of data to be fetched **1**. The 3705 control program then sets ICW byte 7 with the CS byte count and sets ICW byte 6 with the extended portion of the storage address, the data chain flag, the message chain flag and the cycle steal valid bit **2**. CS valid (ICW bit 6.6) notifies the scanner that the address, byte count and any flags are valid and to request a cycle steal operation from the CCU. Refer to the "Cycle Steal Timing Chart—Transmit" on F-370 for details of the following sequence.

When 'bit service request' is active on the selected interface address, the scanner tests the pointers to determine if there are two empty buffers in the PDF array associated with the

selected interface address. (The entire sequence of testing the pointers for our transmit example is shown on F-380.) Since the array is empty **3** and 'cycle steal valid' is on, the scanner sets the 'CS request' latch. This sends 'bid cycle steal' to the CCU. The scanner raises 'set CS registers' which gates (1) the CS address from ICW work register bytes 6, 8, and 9 to CSAR and CSAR update register **4**, (2) the CS byte count from ICW work register byte 7 to the CS byte count register **5**, and (3) the ICW address to CBAR **6**. CBAR saves the selected address to use to address the ICW and PDF array during a following CCU time. At this time the two data bytes must be loaded into the associated PDF buffers and the updated byte count and updated CSAR are written into the ICW that requested the cycle steal. The 'CS busy' latch prevents all other scanned line 'interface ICWs containing a 'CS valid' bit on from requesting a cycle steal.

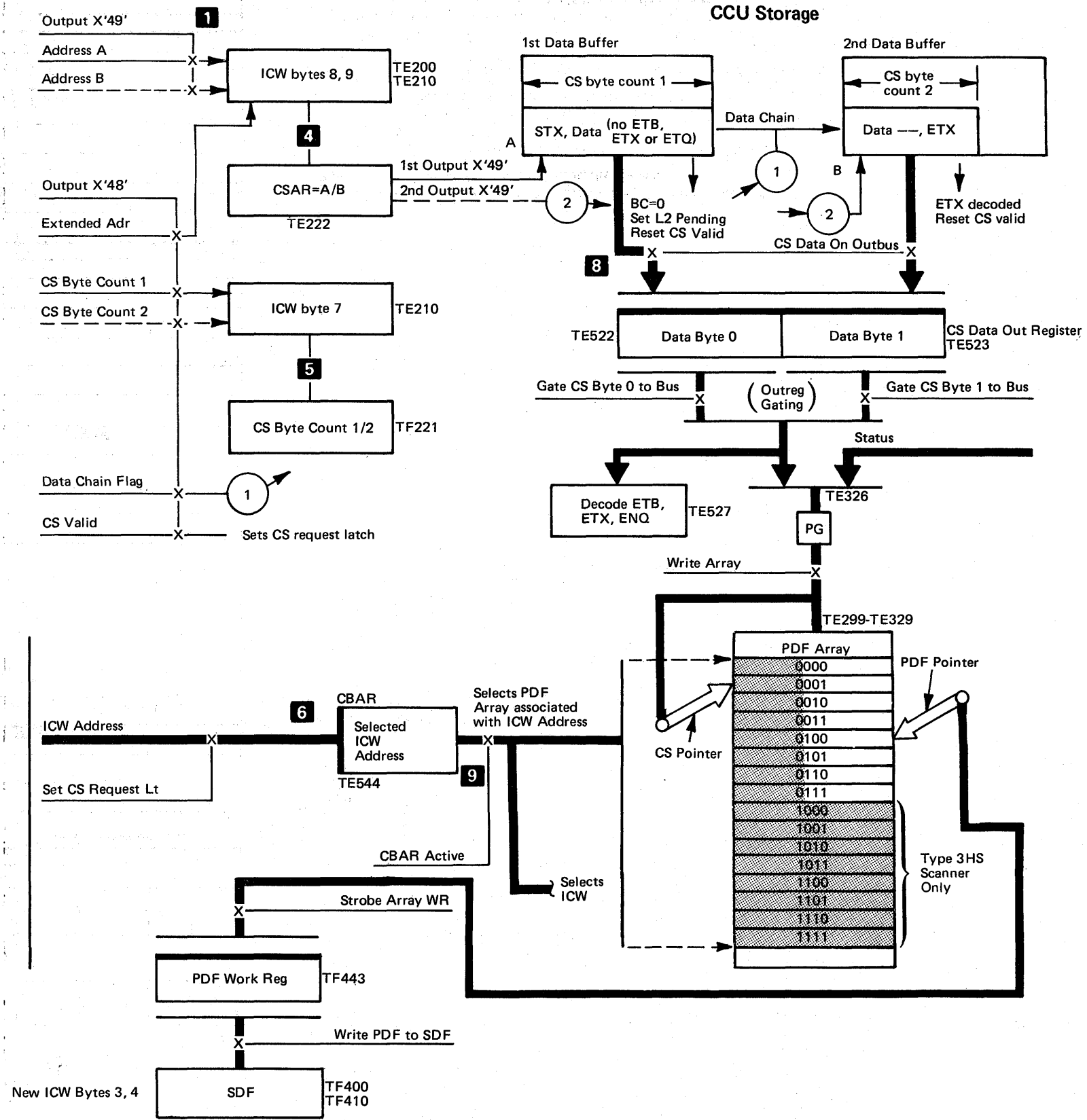
When the CCU can take a CS cycle, the CCU returns 'CS go CSB' **7** to the first scanner. If the first scanner did not request the cycle steal, that scanner propagates the 'CS go CSB' signal to the next scanner. This continues from scanner to scanner until the signal is trapped by the scanner that requested the cycle steal.

The scanner gates the address from CSAR to SAR where the CCU uses it to address the storage location of the data to be fetched. When the CCU raises 'sample CS data on outbus', the scanner gates the data into the CS data out register **8**. The scanner then requests access to the ICW during CCU time and, if there is no Output X'4X' nor a 'fetch buffer' operation underway, sets the 'CBAR active' latch. The address in CBAR then selects the ICW and the associated PDF array **9**. The scanner sets data byte 0 in the buffer selected by the CS pointer and then increments the CS pointer and CSAR update register and decrements the CS byte count. The scanner then sets data byte 1 into the next sequential buffer and again increments the CS pointer and CSAR update register and decrements the CS byte count. The scanner stores the updated CS and PDF pointers, the updated CSAR and CS byte count, and the regenerated cycle steal valid bit in the ICW. 'CS reset' turns off the CS busy latch to end this cycle steal operation.

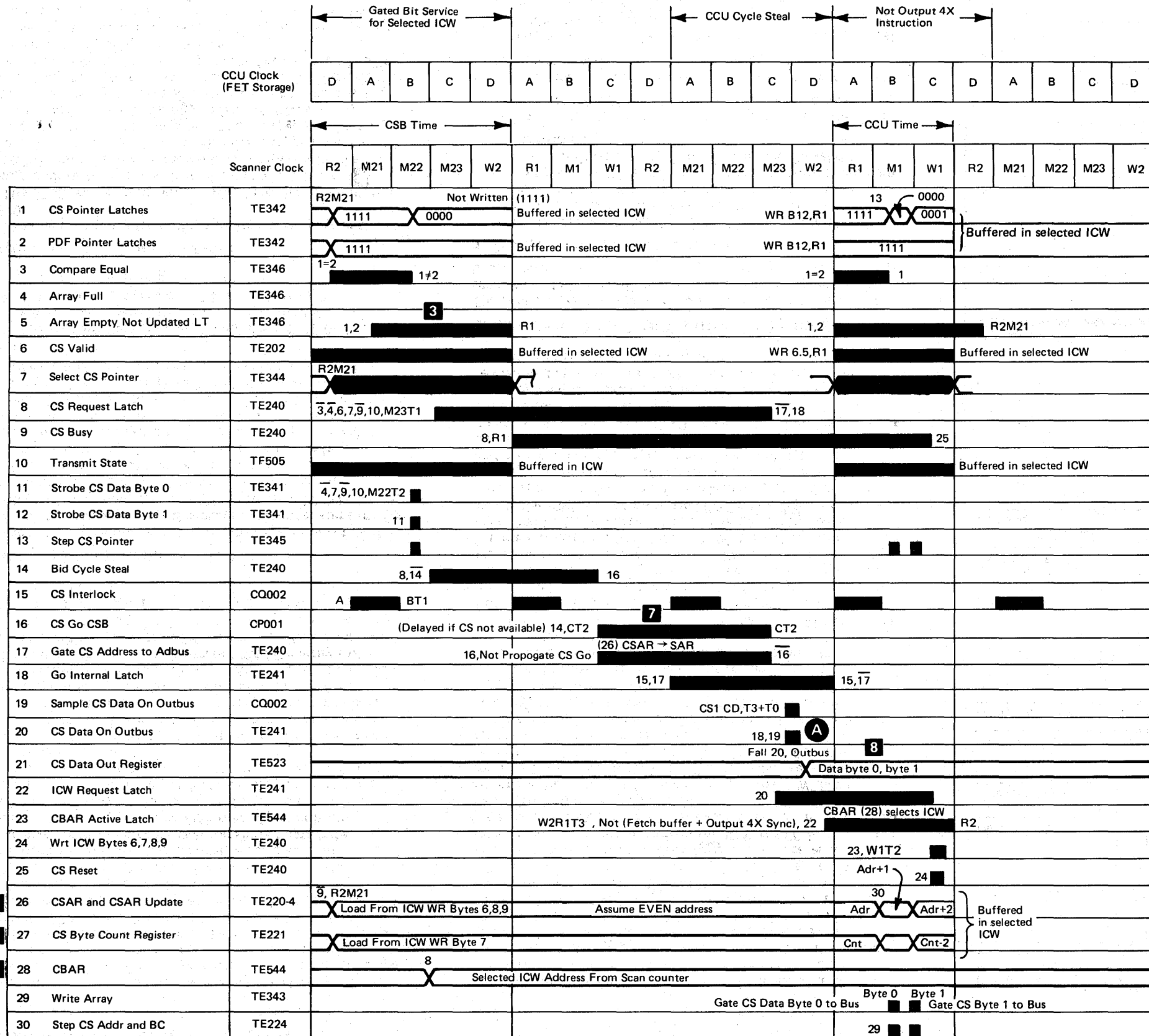
Ending Cycle Steal Data Transfers for Transmit

The above cycle steal operation is repeated for the transfer of each two data bytes until the cycle steal valid bit is reset. This occurs when:

- The cycle steal byte count goes to 0.
 - If the data chain flag (ICW bit 6.6) is on and if no ETX, ETB, or ENQ character has been detected in the received data just fetched, the scanner sets 'L2 interrupt pending' (ICW bit 5.1) to notify the control program to set up CSAR, CS byte count, flags and CS valid for the next data buffer.
 - If the data chain flag bit is off, the scanner uses the final status from ICW byte 15 to initiate the ending sequence.
- An ETB, ETX, or ENQ character is detected in the received data just fetched.
 - The scanner sets ICW bit 6.4 (ETB + ETX + ENQ in data) and inhibits any additional transfers to the PDF array by resetting CS valid. No L2 interrupt is made.



CYCLE STEAL TIMING CHART—TRANSMIT



Test for empty buffers.

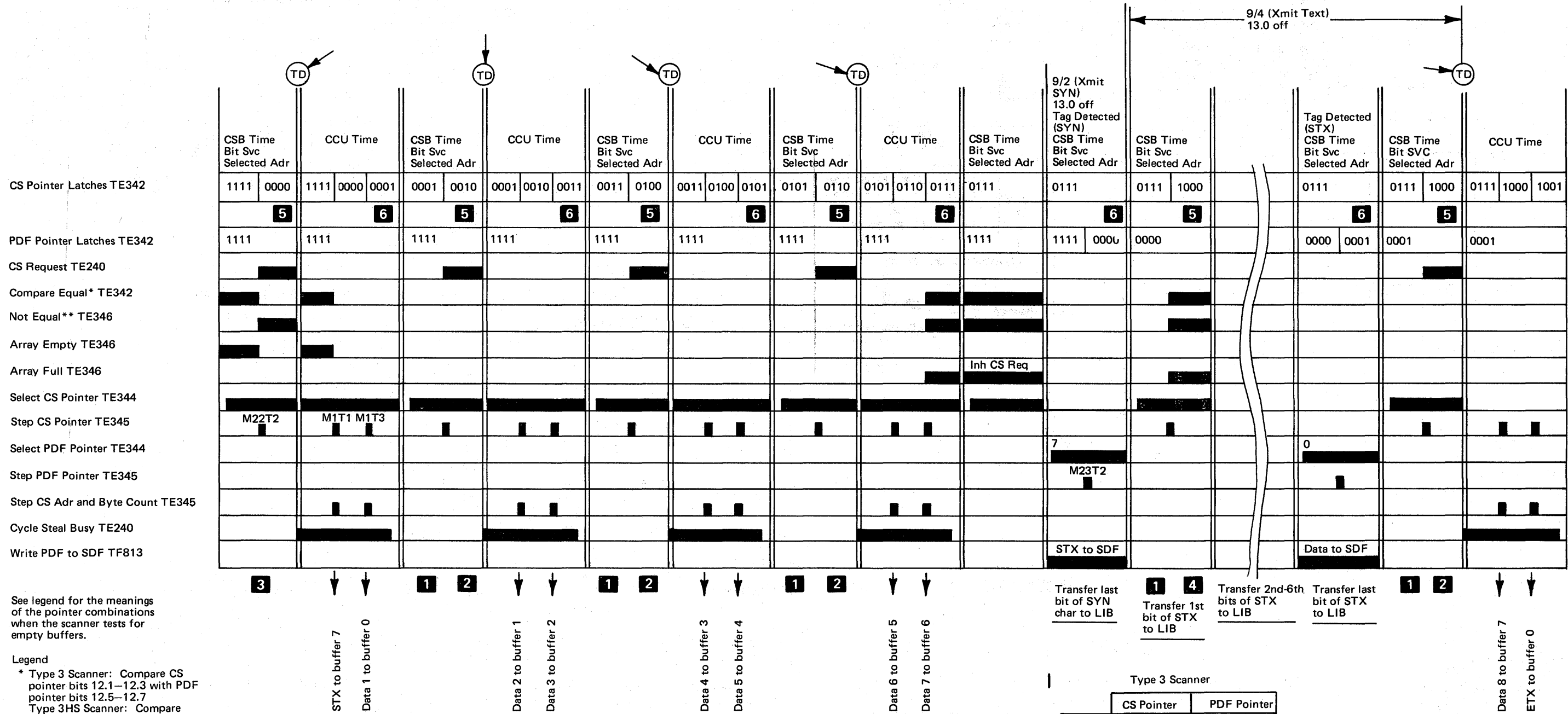
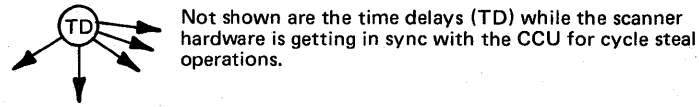
Repeat this sequence at the next gated bit service for this selected ICW as long as there are buffer(s) empty. Test for empty buffers every bit service.

A If the scanner detects an outbus byte 0 or byte 1 parity check while the cycle-steal data is on the outbus, the scanner:

- Sets the 'CS parity error' latch (TE703). This causes the scanner to bid for a level 1 interrupt.
- Activates 'work reg or array or CS error' (TE706). This sets the cycle-steal address, currently in CBAR, into DBAR.
- Inhibits the regeneration of 'cycle steal valid' (ICW bit 6.5) that terminates the cycle-steal operation.

The control program executes an Input X'43' instruction to determine what caused the level 1 interrupt—bit 1.4 will be on. The control program executes an Input X'42' instruction to determine the line program address (trapped in DBAR) that was active when the CS parity error occurred.

See F-360 for a description of the testing of the CS and PDF pointers to determine the availability of the PDF buffers.



See legend for the meanings of the pointer combinations when the scanner tests for empty buffers.

Legend

- * Type 3 Scanner: Compare CS pointer bits 12.1–12.3 with PDF pointer bits 12.5–12.7
- Type 3HS Scanner: Compare CS pointer bits 12.0–12.3 with PDF pointer bits 12.4–12.7
- ** Type 3 Scanner: Compare CS pointer bit 12.0 with PDF pointer bit 12.4
- Type 3HS Scanner: Compare CS pointer bit 17.0 with PDF pointer bit 17.1

- 1 Array not empty, not full—at least 1 empty buffer
- 2 Array not empty, not full—at least 2 empty buffers
- 3 Array empty
- 4 Array full—1 empty buffer
- 5 Do not store updated pointers—no write byte 12
- 6 Store updated pointers—write byte 12

Type 3 Scanner

	CS Pointer	PDF Pointer
Array	1nnn	0nnn
Full	0nnn	1nnn
Array	0nnn	0nnn
Empty	1nnn	1nnn

Type 3HS Scanner

	CS Pointer	PDF Pointer
Array	1nnnn	0nnnn
Full	0nnnn	1nnnn
Array	0nnnn	0nnnn
Empty	1nnnn	1nnnn

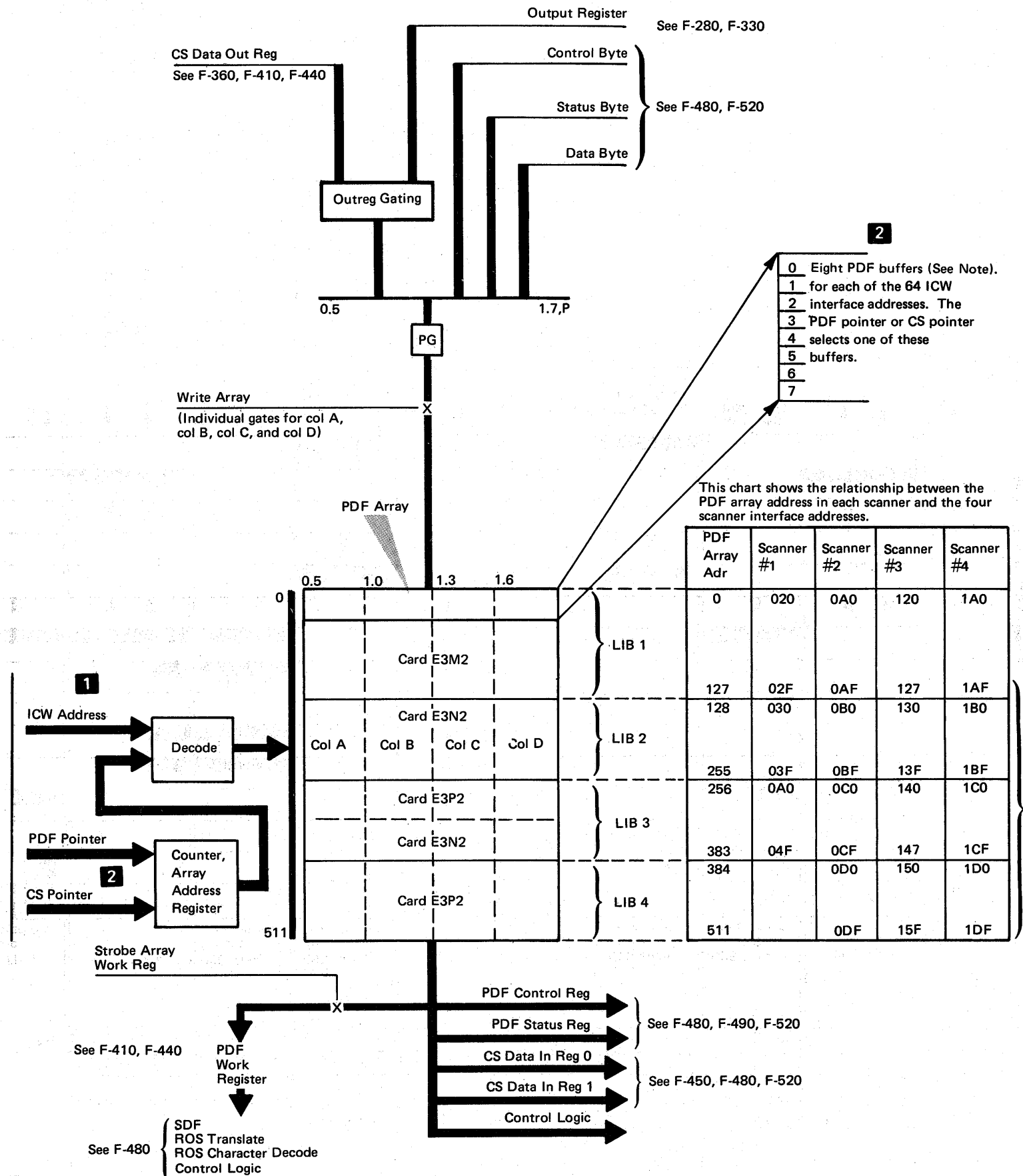
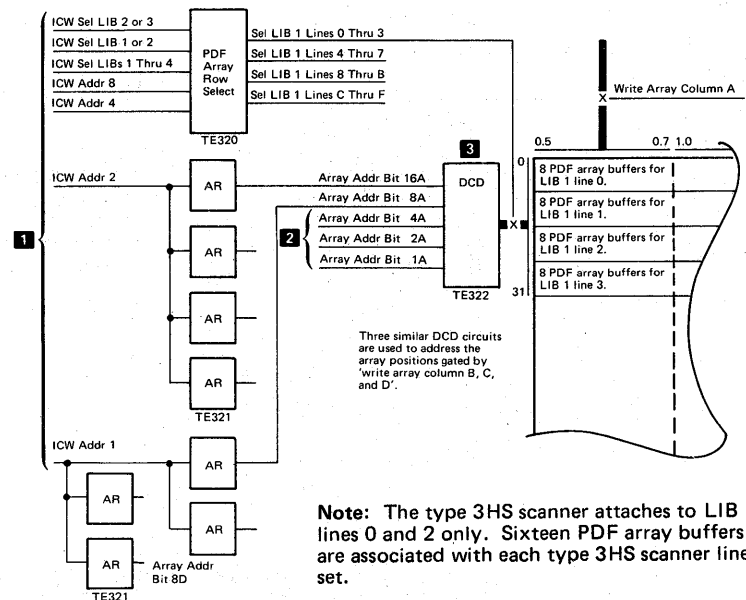
PDF ARRAY—SUMMARY OF CS/PDF POINTER USE

PDF Pointers Selected	CS Pointers Selected
<ol style="list-style-type: none"> Fetch buffer (Gate In Reg) No 'write array' nor 'step PDF pointer'. Output X'44' 'Write array' and 'step PDF pointer' at M1T1 but updated pointer is not written into ICW Byte 12. Output X'4C' 'Write array' at M1T1 but no 'step PDF pointers'. ICW and array reset. 'Write array' and 'step PDF pointers' at M22T1 and M23T2. Dial (LCD 3 or B). No 'Write array' nor 'step PDF pointers'. SDF to PDF (Receive). 'Write array' and 'step PDF pointer' at M22T1. Status Character to PDF. 'Write array' and 'step PDF pointer' at M23T2. Control character to PDF. 'Write array' and 'step PDF pointer' at M23T2. Status character and control character to PDF. 'Write array' and 'step PDF pointer' at M22T1 (status) and M23T1 (control). ITB skip. No 'write array'. PDF to SDF (Transmit). No 'write array' but 'step PDF pointer' at M23T2 except if PCF=E or PDF=first DLE in transparency. 	<ol style="list-style-type: none"> Output X'4D'. 'Write array' for byte 0 and byte 1 and two 'step CS pointer' at M1T1 and M1T3. CS data-out register byte 0 to PDF (Transmit). 'Write array' and 'step CS pointer' at M1T1. CS data-out register byte 1 to PDF (Transmit). 'Write array' and 'step CS pointer' at M1T3. CS test of pointers to determine if the PDF array has room for data from CS data out register (Transmit). No 'write array' but 'step CS pointers' at M22T2, however updated pointer is not written into ICW byte 12. PDF array "data" to CS data in register bytes 0 and 1 (Receive-one byte). No 'write array' but 'step CS pointers' at M22T1. PDF array "data" to CS data in register byte 0 and byte 1. (Receive-two bytes). No 'write array' but 'step CS pointers' at M22T2 (load bytes 0 and 1) at M23T2 (overlay byte 1). PDF array "status" to PDF status register and PDF control register (Receive). No 'write array' but 'step CS pointers' at M22T2. The scanner then gates the "status" from the PDF status register. PDF array "control" to PDF status register and PDF control register (Receive). No 'write array' but 'step CS pointers' at M22T2. The scanner then gates the "control" from the PDF control register. PDF array "status" to PDF status register and PDF control register then PDF array "control" overlays the "status" in the PDF control register (Receive). No 'write array' but 'step CS pointers' at M22T2 and M23T2.

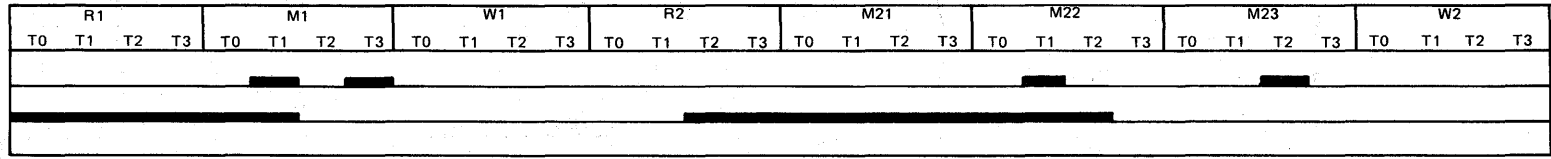
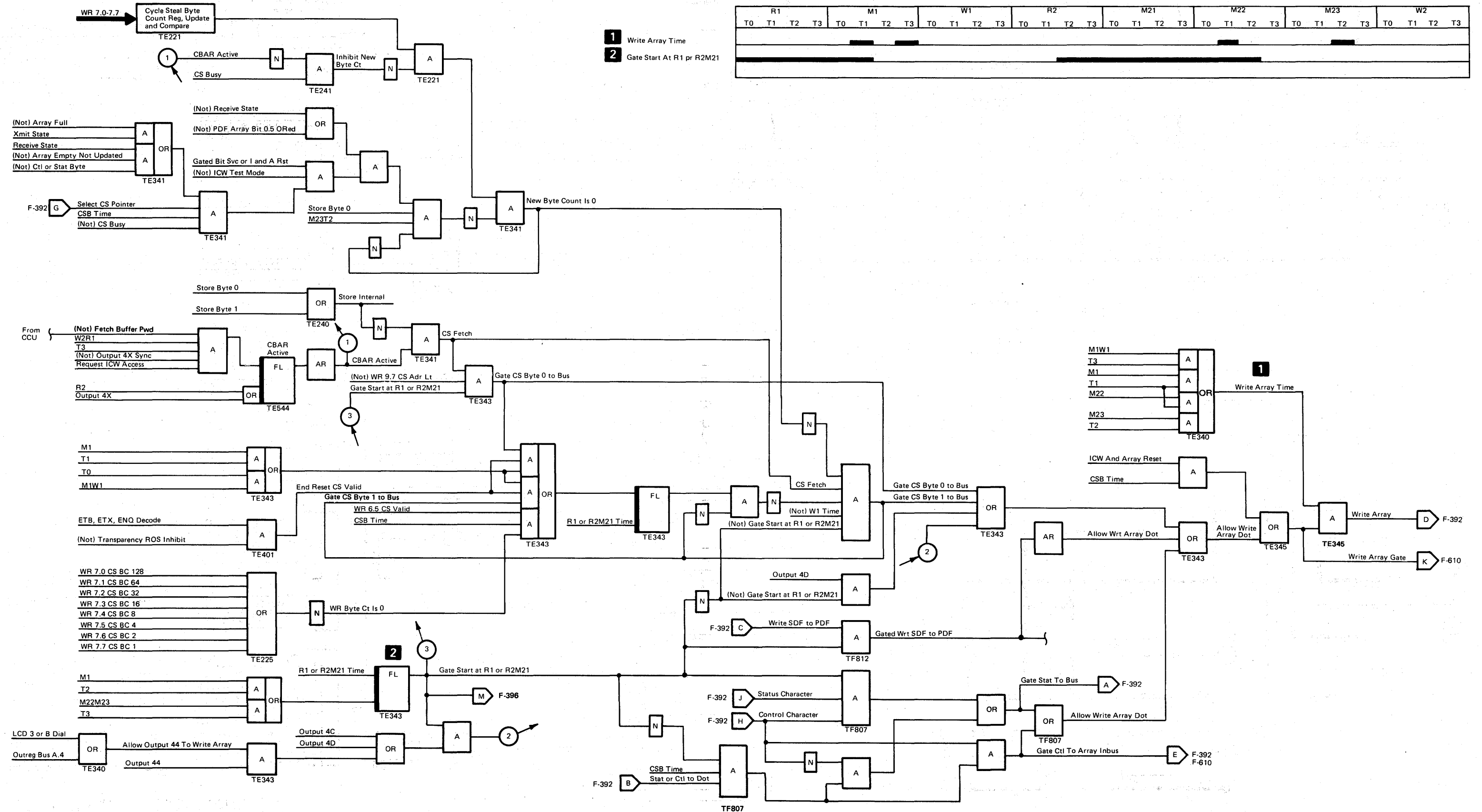
Logic Pages TE 344/345

Note: See page F-392 for PDF or CS pointer selection second level diagrams.

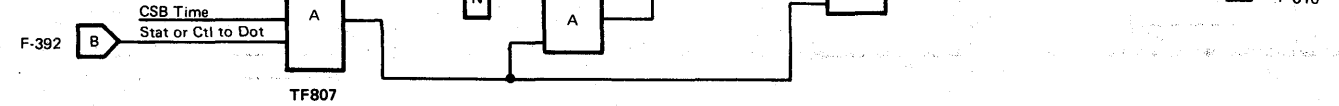
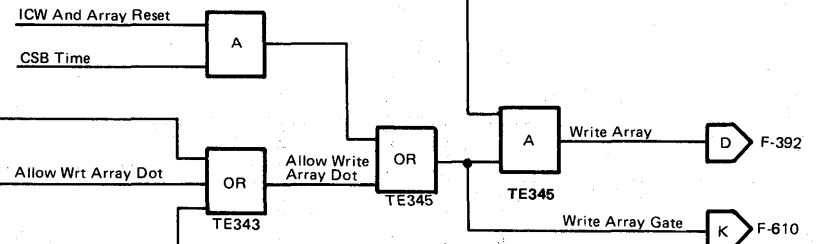
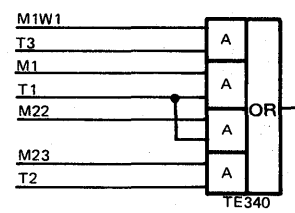
PDF Array Address Selection For LIB 1 Lines 0 Thru 3 (See Note).



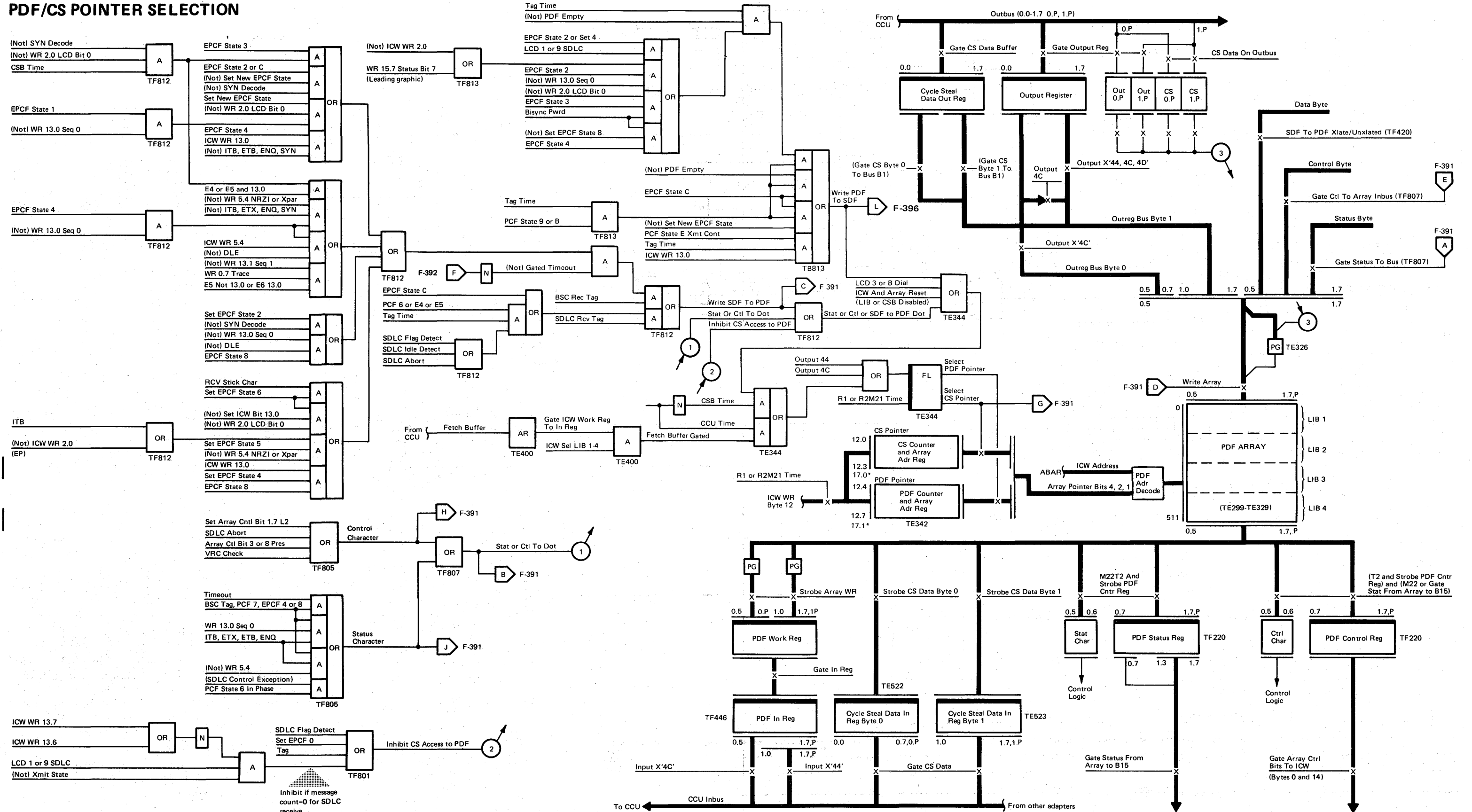
WRITE ARRAY CONDITIONS



1 Write Array Time
2 Gate Start At R1 or R2M21



PDF/CS POINTER SELECTION



* ICW bits 17.0 and 17.1 are used with the type 3HS scanner only. Sixteen PDF array buffers are associated with each type 3HS scanner line set.

FORCING CONTROL CHARACTERS AND CONSTANTS TO THE SDF

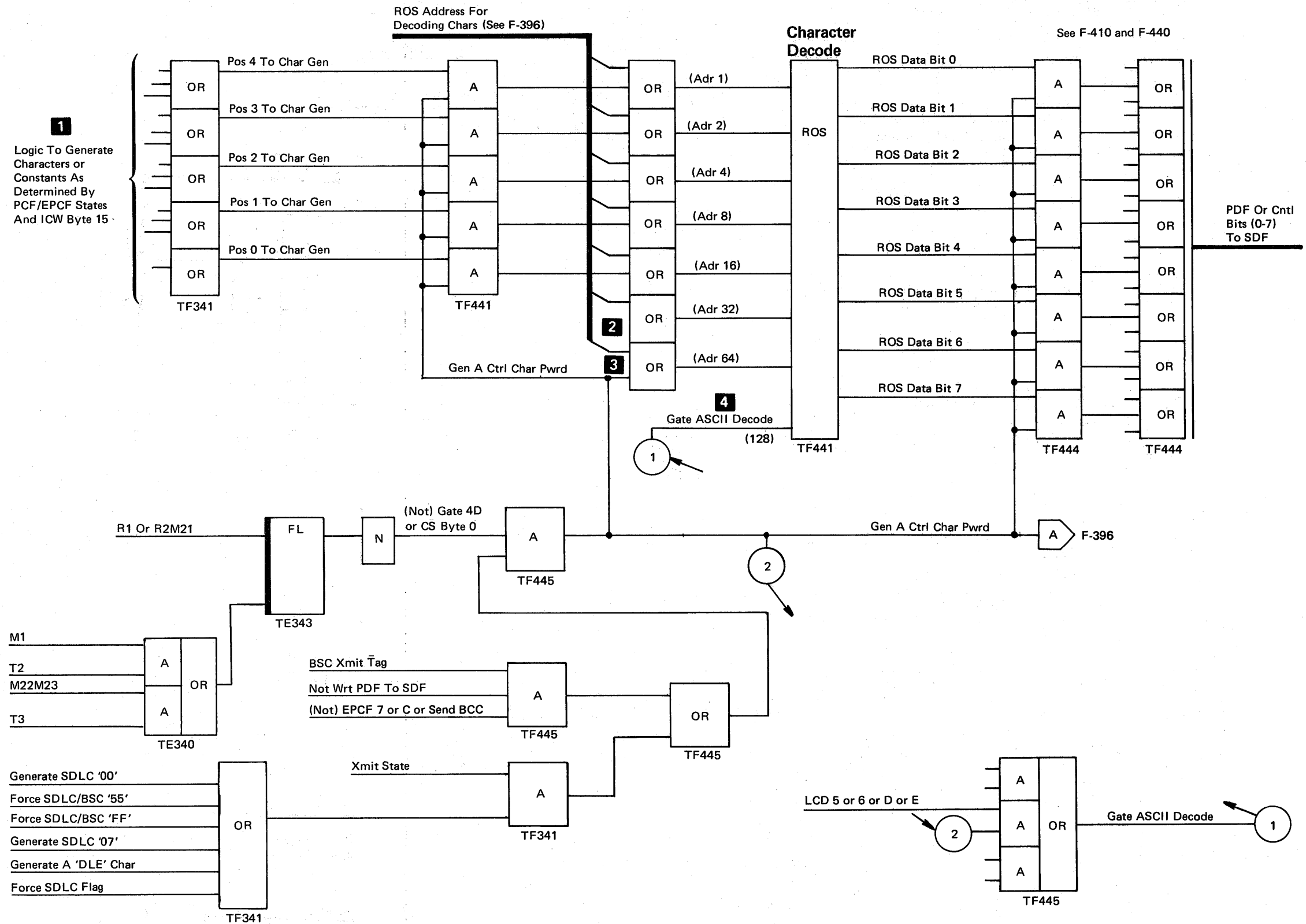
The scanner uses the character-decode ROS for generating control characters and constants and for decoding control characters (see F-396).

When in transmit mode, the scanner generates control characters and constants by generating an eight bit ROS address for the desired address. Five of these address bits are variable and are generated by logic determined by PCF/EPCF states and by ICW byte 15 **1**. Address bit 32 is always inactive **2**, address bit 64 is always forced active **3**, and address bit 128 is forced active for USASCII lines only **4**. The five variable bits that are used to generate a specific character or constant are defined in the following chart.

When generating control characters and constants, the scanner addresses ROS from M22M23T3 time to R1 time to provide valid characters to the SDF at W2 write time since the ROS data-bit output is valid 50 nano-seconds after being addressed.

Character/ Constant	Position to Char Gen 0 1 2 3 4	ROS Address <small>00000001</small> N0000001	ROS Data Bit Output (Hex)	
			EBCIDIC	USASCII
PAD(00)	0 0 0 0 1	X1000001	00	00
PAD(FF)	0 0 0 1 0	X1000010	FF	FF
ENQ	0 0 0 1 1	X1000011	2D	85
ITB	0 0 1 0 0	X1000100	1F	1F
PAD(55)	0 0 1 0 1	X1000101	55	55
ACK 0	0 0 1 1 0	X1000110	70	B0
NAK	0 0 1 1 1	X1000111	3D	15
SYN	0 1 0 0 0	X1001000	32	16
ETX	0 1 0 0 1	X1001001	03	83
ETB	0 1 0 1 0	X1001010	26	97
STX	0 1 0 1 1	X1001011	02	02
EOT	0 1 1 0 0	X1001100	37	04
RVI	0 1 1 0 1	X1001101	7C	BC
ACK 1	0 1 1 1 0	X1001110	61	31
WACK	0 1 1 1 1	X1001111	6B	3B
7E	1 0 0 0 0	X1010000	7E	FF
PAD(07)	1 0 0 0 1	X1010001	07	07
SOH	1 0 0 1 0	X1010010	01	01
PAD(1F)	1 0 0 1 1	X1010011	1F	1F
DLE	1 0 1 0 0	X1010100	10	10

- Notes: 1. ROS address 128;
 If X = 0, then the ROS data bit output is EBCDIC.
 If X = 1, then the ROS data bit output is USASCII.
 2. ROS forces the parity bit for USASCII.



CONTROL CHARACTER DECODE

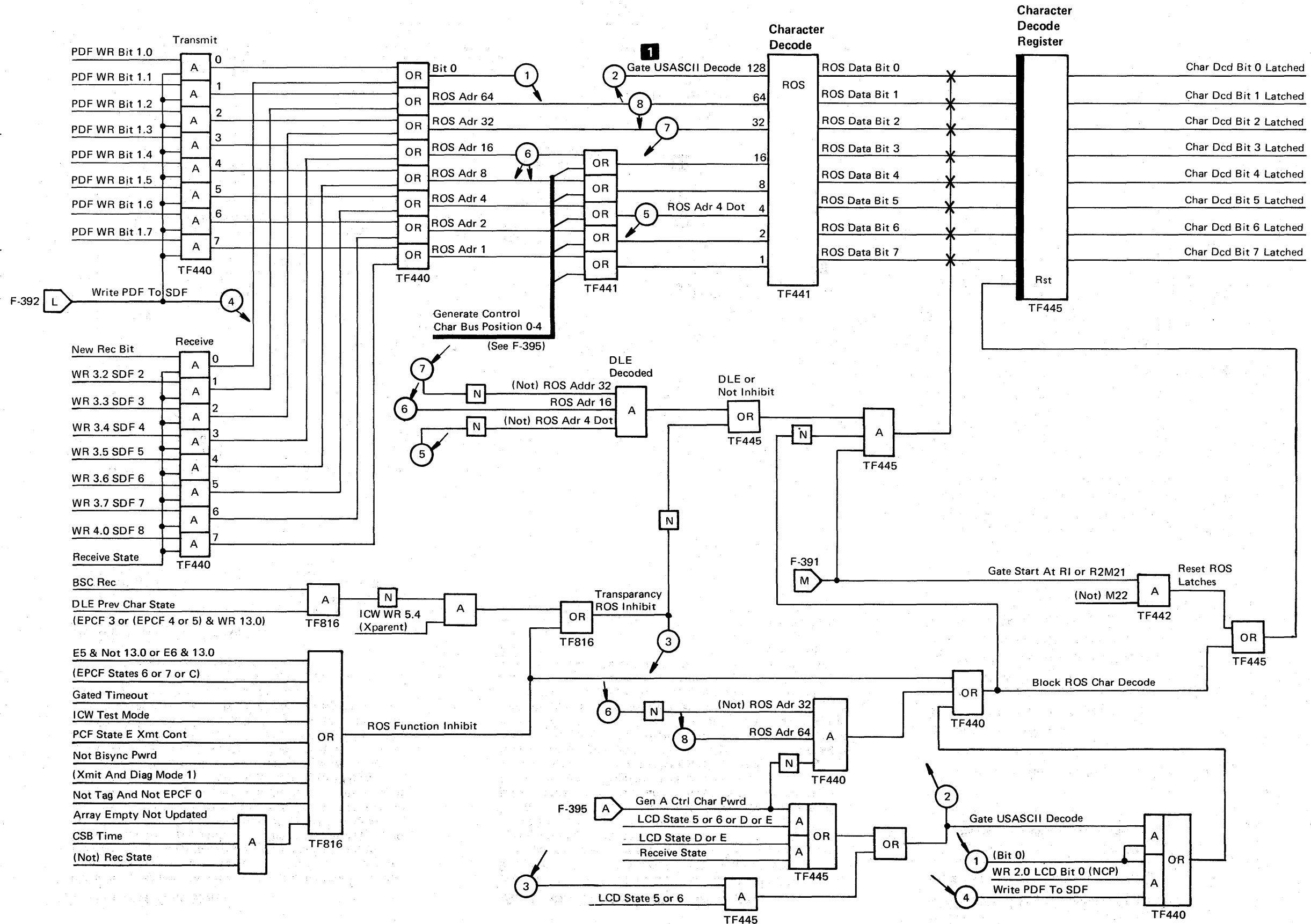
During a transmit operation, the scanner gates the character in the selected PDF array into the PDF work register. The scanner uses the bits of this character to address the character-decode ROS. ROS activates combinations of eight ROS data bits depending on the input character configuration. The scanner latches these eight ROS output states in the character-decode register that provides the input to the decode logic.

During a receive operation, the scanner uses the bits of the assembled receive character in the SDF to address the character-decode ROS.

The following chart shows the 'ROS data-bit' outputs that ROS activates for different characters in the PDF work register (transmit) or in the SDF (receive).

Input Character	EBCDIC	USASCII	ROS Data Bits							
			0	1	2	3	4	5	6	7
SOH	01	01	0	0	0	0	1	1	1	0
STX	02	02	0	0	0	0	0	0	1	0
ETX	03	03	1	0	1	1	1	0	0	1
DLE	10	10	0	0	1	0	1	0	0	0
ITB	1F	1F	1	0	1	0	0	0	0	1
ETB	26	17	1	0	1	1	1	0	1	0
ENQ	2D	05	0	0	1	1	0	0	1	1
SYN	32	16	0	0	1	0	1	1	0	0
EOT	37	04	0	1	0	0	0	1	0	0
NAK	3D	15	0	0	0	0	0	1	1	1
ACK 1	61	31	0	1	0	0	1	0	1	1
WACK	6B	3B	0	1	0	0	1	1	1	1
ACK 0	70	30	0	1	0	0	1	1	1	0
RVI	7C	3C	0	1	0	0	1	1	0	1

- Notes:
- The scanner forces ROS address bit 128 to a 1 bit when in USASCII mode **1**.
 - The scanner does not use the USASCII parity bit when addressing ROS.
 - The PDF addresses ROS in transmit mode and the SDF addresses ROS in receive mode.



BSC TRANSMIT

To begin a BSC transmission, the 3705 control program must execute an:

- Output sequence for "Set Mode" to initialize the line set (see F-530).
- Output X'4F' to set the initial control, final control and leading graphics control in ICW byte 15 when using NCP mode (LCD X'C' or 'D'). See F-150 for the control fields in ICW byte 15. When using EP mode (LCD X'4', '5', or '6'), the initial and final control characters are in the data stream, except for transparent endings which the EP program must set in ICW byte 15.
- Output X'45' to set (1) the LCD (EP mode or NCP mode), (2) the PCF to X'8', and (3) EPCF to X'0' (transmit initial). Output X'45' also resets the CS and PDF pointers in ICW byte 12 to X'F'.
- Output X'49' to set ICW bytes 8 and 9 with the storage address of the first byte of data to be fetched by cycle stealing.
- Output X'48' to set (1) ICW byte 7 with the CS byte count and (2) ICW byte 6 with the extended portion of the storage address, the data chain flag, and the cycle steal valid bit.

The scanner transmits PAD and SYN characters (forced by the PCF/EPCF states) to get the receiving modem in character phase. When in NCP mode, the scanner then transmits the initial control or leading graphics, if specified. When in EP mode, the scanner transmits the initial control character from the PDF array. This character and the data to follow are placed in the PDF by cycle stealing - see F-410. The scanner then transmits the data. The scanner inserts SYN sequences (SYN-SYN or DLE-SYN) every second. The scanner also generates the BCC characters. When all the data has been transferred, the scanner transmits the final control sequence (as specified in ICW 15 for NCP mode, or the end character in the data stream for EP mode), the BCC if required, and a PAD character if the line is to turnaround to the receive state. At the completion of the turnaround the scanner initiates a level 2 interrupt request. If a turnaround is not required (ITB sequence), the level 2 interrupt request is not made until after the end characters (ETB or ETX) have been transmitted and the line has been turned around, or the byte count goes to zero.

Normal Text Mode

When in normal text mode, the scanner monitors the data as it is fetched from CCU storage. If the scanner detects an ITB character in the PDF during a PDF to SDF transfer, the scanner transmits the ITB followed by the BCC and then continues transmitting the next block of data, but skips the next character if so directed by the final control "status" in ICW byte 15 (NCP mode). If the scanner detects an ETX, ETB, or ENQ in the data stream fetched from storage by cycle stealing, the scanner resets 'cycle steal valid' (ICW bit 6.5) then transmits the characters queued in the PDF (including the ETX or ETB character), the BCC and a PAD. In NCP mode the scanner sets 'length check' (ICW bit 14.7). When the line has turned around, the scanner requests a level 2 interrupt.

Transparent Text Mode

When in transparent text mode, the scanner monitors the data stream for a DLE character. If a DLE is detected in the PDF, the scanner inserts an additional DLE without updating the BCC accumulation. The receiving station recognizes this DLE-DLE sequence as a DLE data character.

Since all characters are transparent, the scanner does not recognize any control sequence in the data stream while in transparent text mode. The control status (ICW byte 15) as set by the 3705 control program, determines which ending sequence to use when the data has been transmitted. The options are DLE ITB, DLE ETX, DLE ENQ, or DLE ETB. The DLE ETX, DLE ENQ, or DLE ETB causes a line turnaround to receive state before the scanner requests a level 2 interrupt. The DLE ITB causes the scanner to (1) leave transparent mode, (2) send the BCC, and (3) request a level 2 interrupt for the next block of data.

EBCDIC/USASCII Translation

For BSC transmit operation, the type 3 scanner performs an EBCDIC to USASCII code translation when the LCD = X'D' (NCP USASCII) or LCD X'E' and not in transparent text state. No translation occurs for EP USASCII.

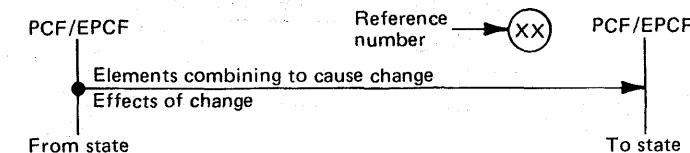
BSC Transmit State-Transfer Diagram

Once the 3705 control program sets the PCF/EPCF states to 8/0 (transmit initial) to start the BSC transmission, the control program turns over the execution of the entire transmit operation to the scanner. The scanner automatically changes the PCF/EPCF states as required based on the LCD state, the state of ICW bits (especially ICW byte 15), the data characters in the data stream, and others as shown in the transmit state-transfer diagram. The scanner uses the level 2 interrupt request to notify the control program when additional control program service is required. State-transfer diagrams are located in the ALDs to enable you to determine exactly what sequence the scanner followed in executing the transmit operation up to the interrupt.

Selected sections of the state-transfer diagram for a BSC transmit operation are shown below. This example has been used to illustrate (1) cycle steal operation-transmit (F-360, F-370, and F-380) and (2) BSC transmit details (F-420). The data flow for this operation is on the facing page for your reference when examining this state-transfer diagram. The keying numbers refer to the data flow on F-410.

How to Read State-Transfer Diagrams

These state-transfer diagrams are read:



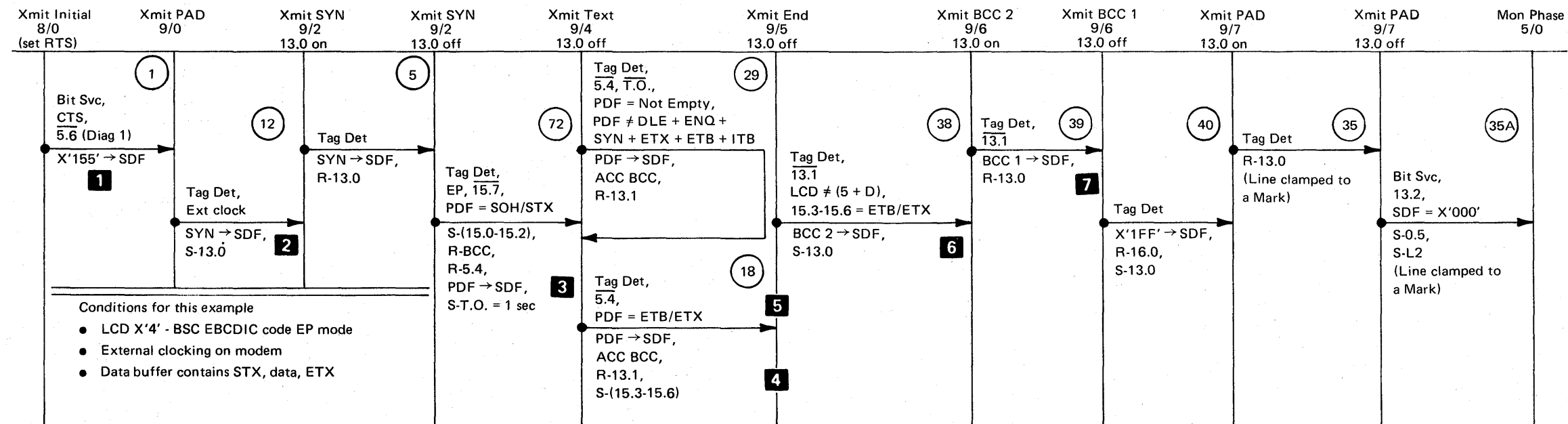
If for example: (refer to reference number 38 below)

- The PCF = X'9' and
- The EPCF = X'5' and
- ICW bit 13.0 is off (not seq 0) and
- Tag has been detected as the last bit of the ETX character is transferred to the LIB and
- ICW bit 13.1 is off (not seq 1) and
- the LCD is not BSC USASCII code and
- ICW bits 15.3 - 15.6 (final control status) contain an ETB or ETX character-set when the ETX was set in the SDF from the PDF.

Then the scanner:

- Sets EPCF = X'6' and
- Transfers the low order byte of the BCC character (BCC 2) from ICW byte 11 to the SDF and
- Sets ICW bit 13.0 (seq 0) to indicate that this character is the first of a multi-byte transmission.

Example of BSC Transmit State-Transfer Diagram



Legend:

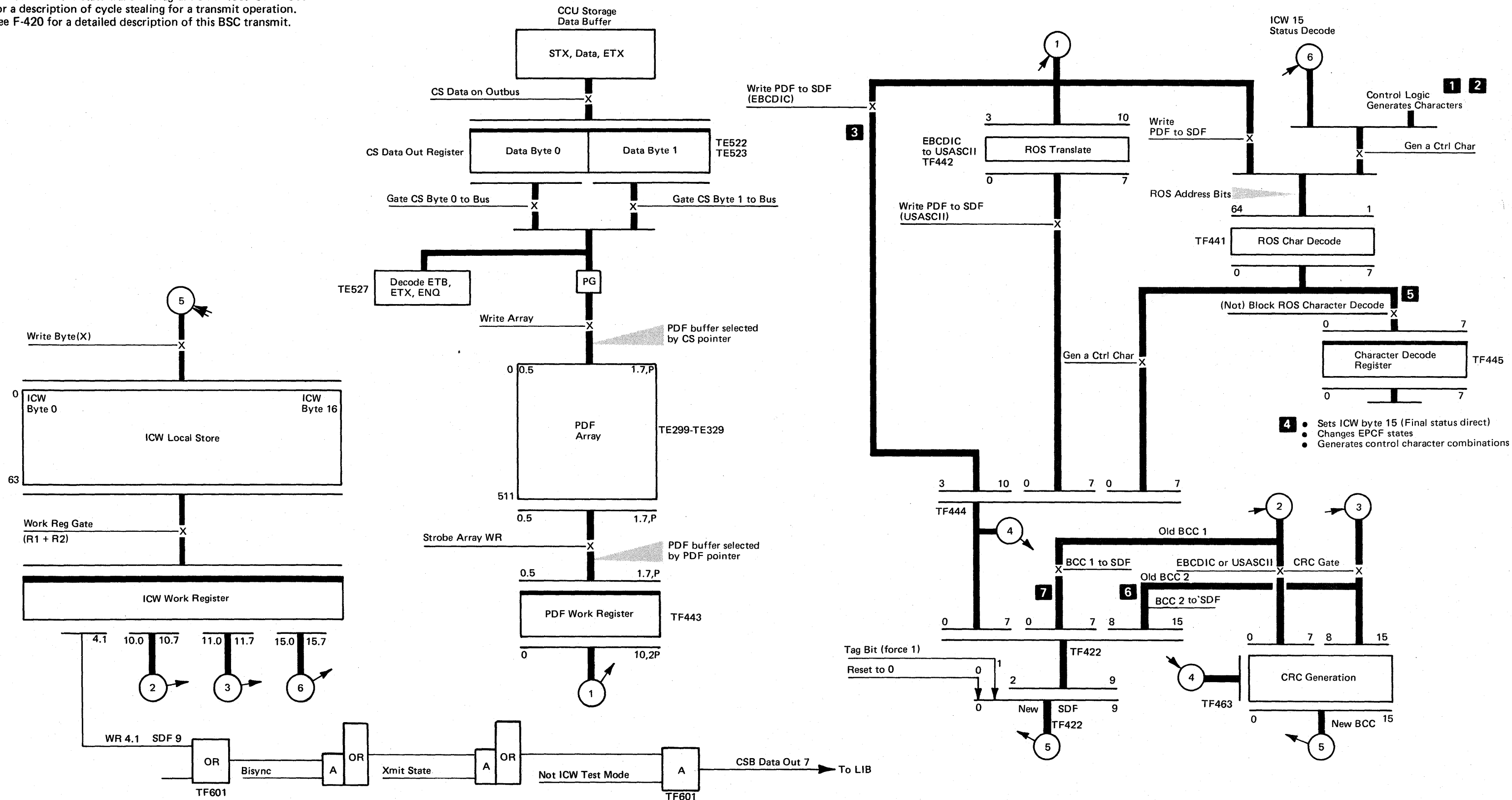
S = Set
R = Reset
EP = Emulation Program mode
8/0 = PCF X'8' and EPCF X'0'
13.0 = ICW bit 13.0 (seq 0) = 1
P = PCF
E = EPCF

T.O. = Timeout
ACC = Accumulate BCC
X'155' → SDF means the scanner generates character X'55' for the SDF. The 1 is the tag bit set into SDF 1.
L2 = Level 2 interrupt request

PDF = SOH/STX means a SOH or STX character is detected in the PDF selected by the PDF pointer for a PDF to SDF transfer.
① = Reference number used by the diagnostic engineer to refer you to this portion of the state-transfer diagram.
+ = OR
• = And

BSC TRANSMIT DATA FLOW

For use with the state-transfer diagram on F-400. See F-360 for a description of cycle stealing for a transmit operation. See F-420 for a detailed description of this BSC transmit.





BSC TRANSMIT DETAILS

This example illustrates the details for the transmission of the PAD two SYNs, and the STX characters as shown on F-400.

Note: This example uses LCD = 4 (EBCDIC code - Emulator Program).

The scanner holds 'CSB data out 7' (send data buffer) at the mark level while CTS (clear to send) is off (TF601). **A** While CTS is off, 'SDF direct' regenerates the data in the SDF and 'shift' is inhibited (TF506).

When CTS turns on, the scanner sets PCF = 9 (TF505). **B** State 9/0 becomes the active PCF/EPCF state at the next 'bit service request' for that interface. The scanner then:

- Removes the mark hold and sends the bit in SDF 9 to the LIB at 'bit service request' time (TF601). **C**

- Shifts SDF 0-9 under control of 'bit service request'. **D**

During this shift, the scanner:

-Inhibits 'SDF direct'.

-Places a zero in SDF 0. **E**

The scanner detects the transmit tag during 'gated bit service' when SDF 1-7 contains all zeros and SDF 8 is 1 (TF422). **F** The scanner:

- Sets EPCF X'2' that modifies PCF X'9' to "transmit SYN" (TF322). **G**

- Sets SDF = X'132' (SYN character and tag bit)-TF815.

- Sets ICW bit 13.0 (Sequence 0)-indicates the first of two SYN characters (TF802)

The scanner sends the bits in SDF 9 to the LIB at each 'bit service request' time. When the scanner detects the tag, the scanner:

- Resets ICW bit 13.0-indicates the second SYN character is to be transmitted (TF802).

- Sets SDF = X'132' (SYN character and tag bit)-TF815.

When the scanner detects the tag, after transmitting the second SYN character, and if no leading graphic is to be generated and the character in the PDF work register = SOH of STX, the scanner:

- Sets EPCF X'4' that modifies PCF X'9' to "transmit text" (TF323).

- Sets ICW bits 15.0-15.2 = 001 to indicate the initial control character STX (was the first character in the buffer for our cycle steal example) was transmitted.

- Resets the BCC.

- Resets ICW bit 5.4.

- Transfers the STX character in the PDF to the SDF **H** (TF813).

- Forces a tag bit into SDF 1 (TF442).

- Resets SDF 0.

- Sets the contents of the ones counter internal timer in ICW byte 4 to 10110 to start a 1 sec timeout (TF603).

SDF = X'155' (Initial PAD character) generated by the scanner when setting PCF state 9. See TF486.

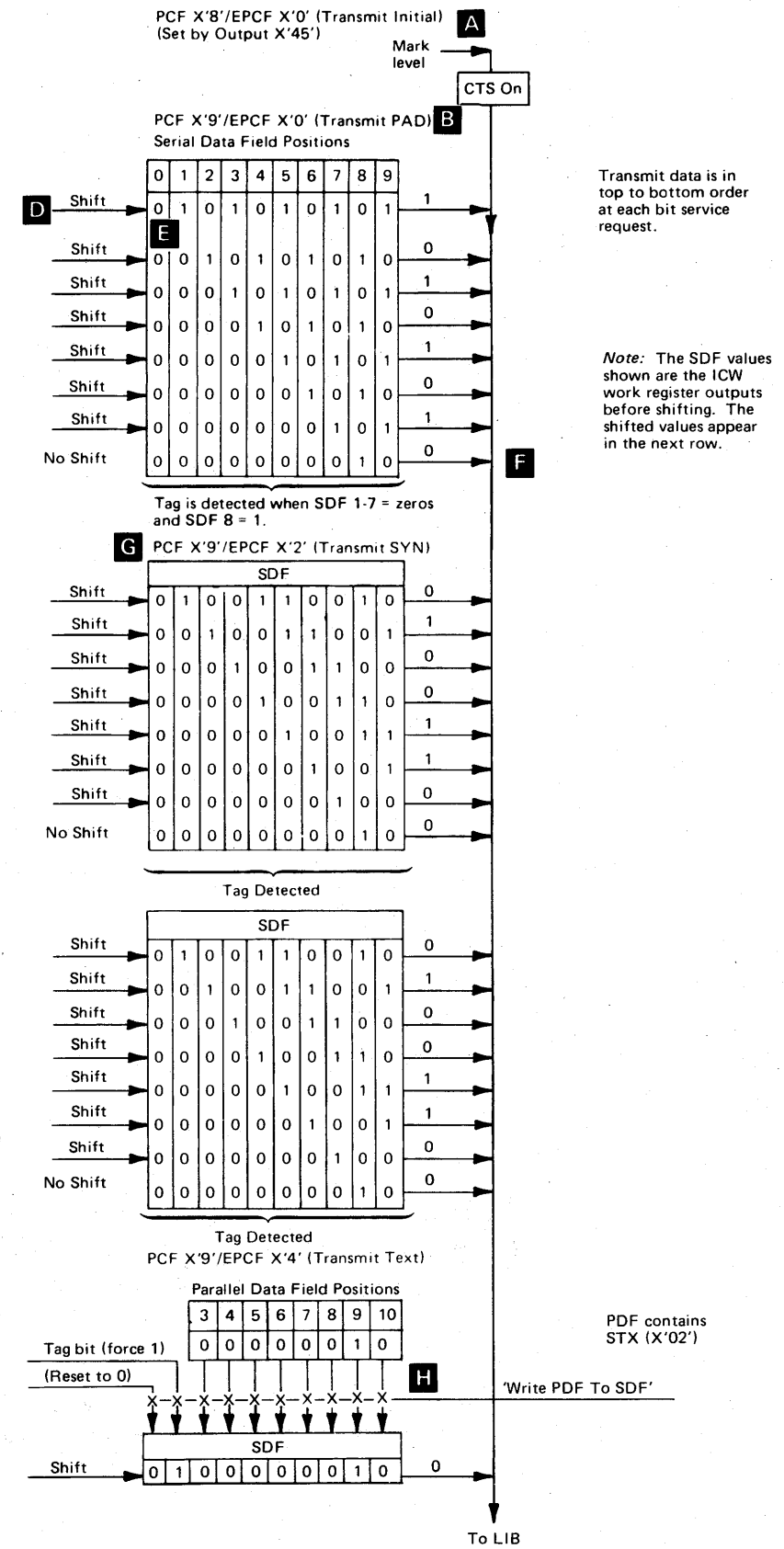
Shift when bit service is received from scanned line interface during 'control in B'

SDF = X'132' (SYN character forced by the scanner when it sets EPCF X'2') TF815. Set into ICW during the same bit service request that detected the tag. The SDF 9 output is used during this bit service scan.

Shift when bit service is received from scanned line interface during 'Control in B'

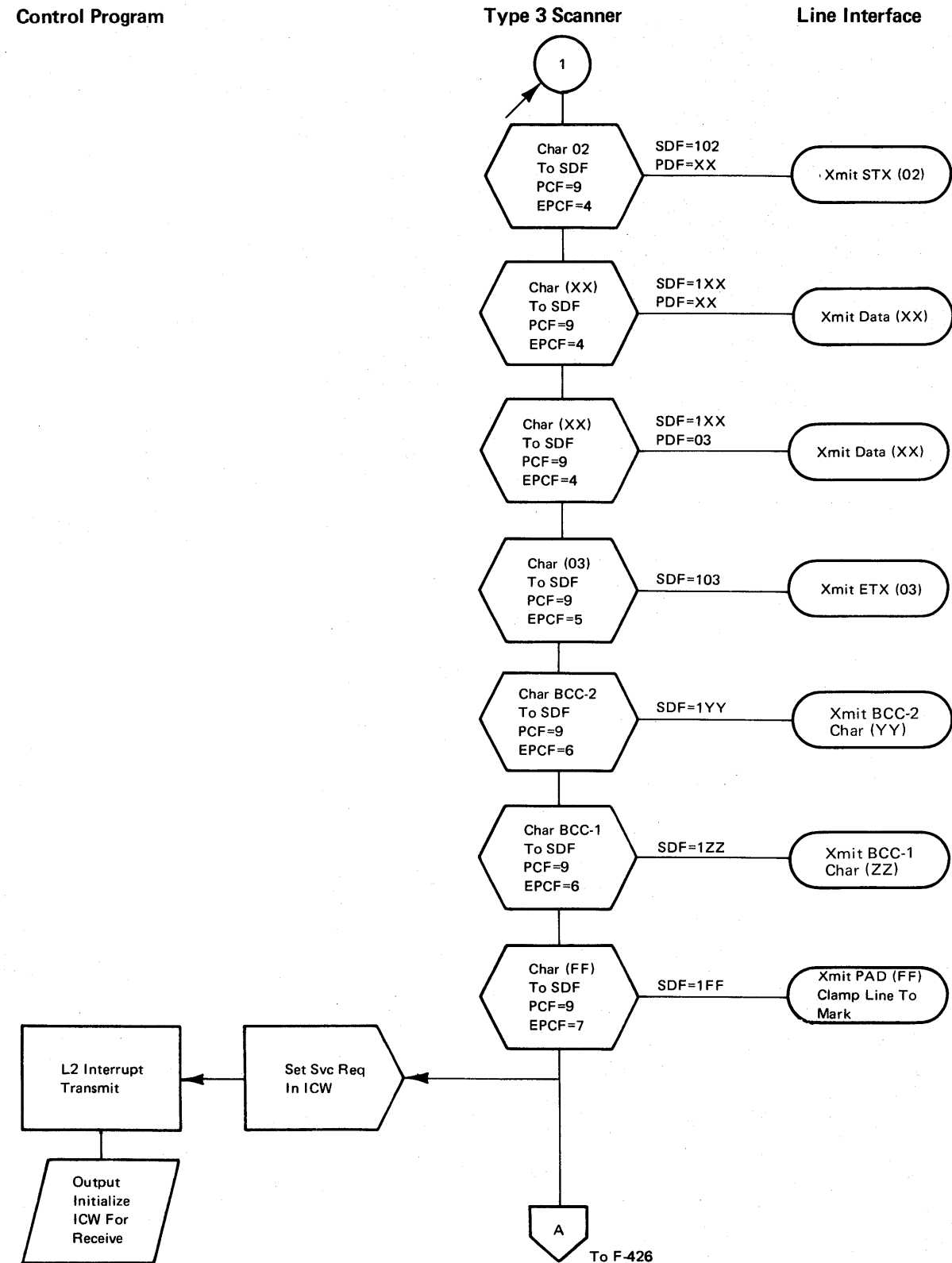
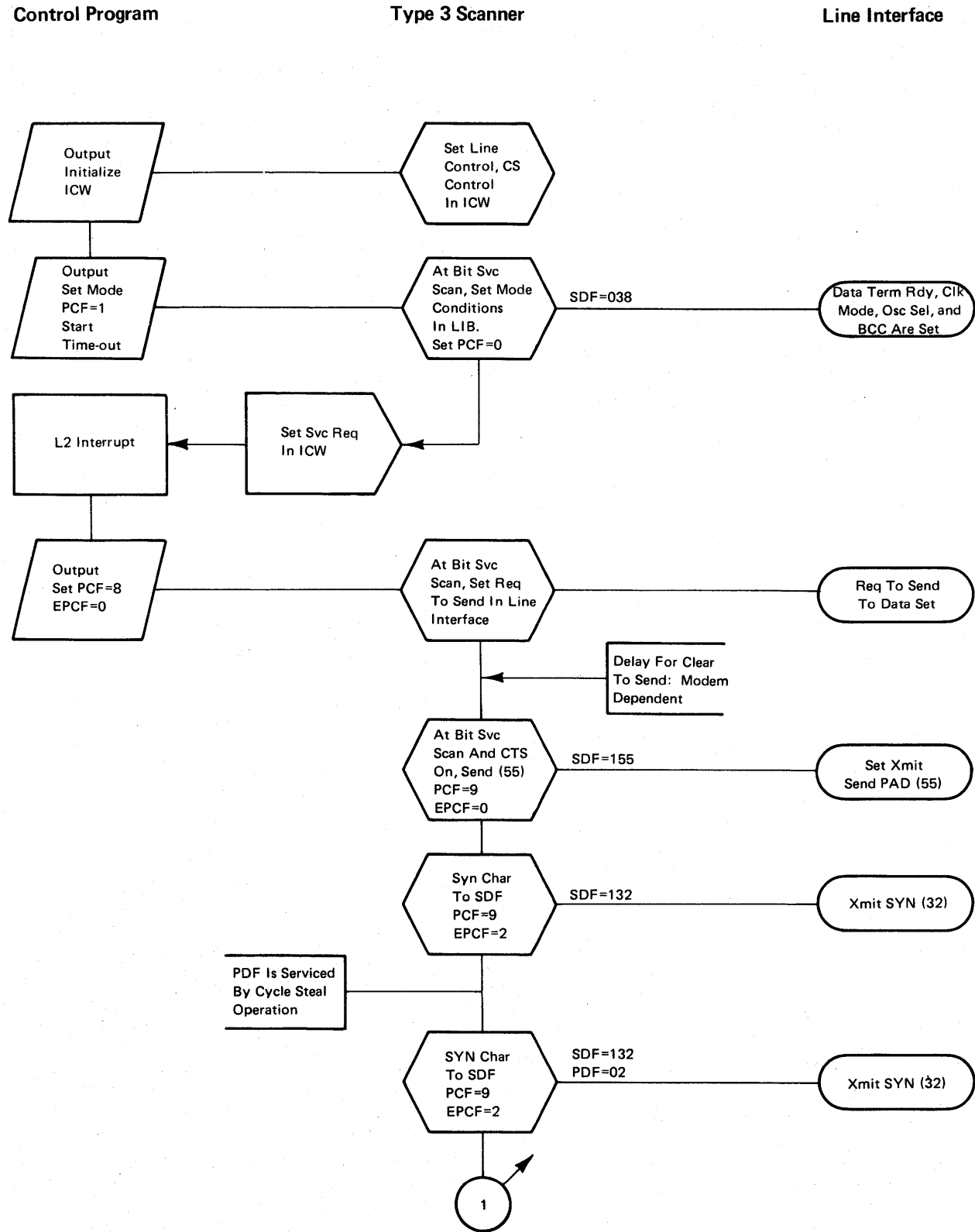
SDF = X'132' (SYN character forced by the scanner when in EPCF X'2' and 13.0 is on (TF815). Set into ICW during the same bit service request that detected the tag. The SDF 9 output is used during this bit service scan.

Shift when bit service is received from scanned line interface during 'Control in B'

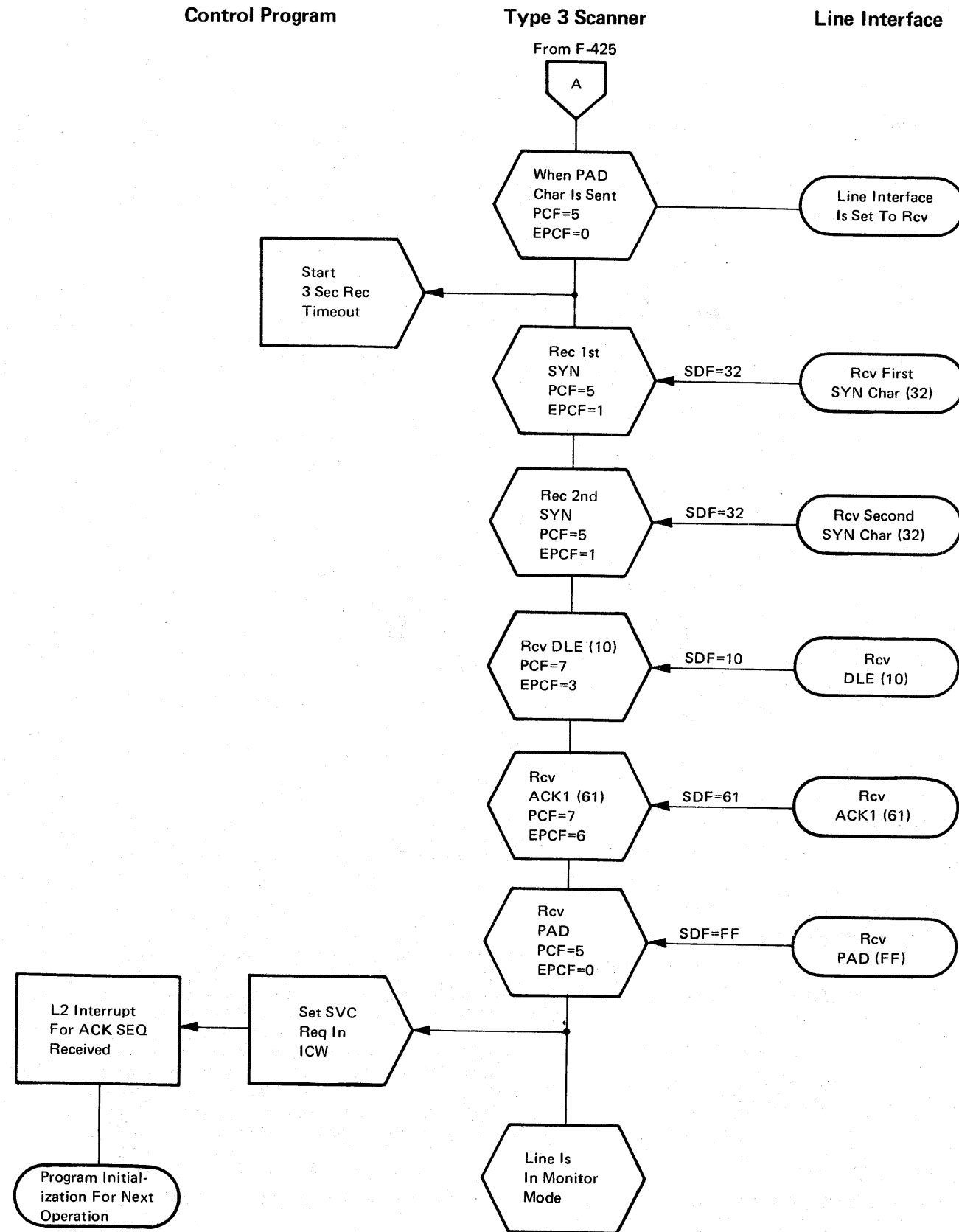


BI-SYNC TERMINAL OPERATION

Note: This operation uses EBCDIC code over a non-switched half-duplex line.



BI-SYNC TERMINAL OPERATION (PART 2)



SDLC TRANSMIT

To begin an SDLC (synchronous data link control) transmission, the 3705 control program must execute an:

- Output sequence for "set mode" to initialize the line set (see F-530).
- Output X'4F' to set the SDLC transmit control/status byte in ICW byte 15 (see F-160). The scanner uses this status to determine the type of ending to perform at the end-of-frame (turnaround or to transmit Idle or Flag characters).
- Output X'45' to set (1) the LCD to X'9'-SDLC, (2) the PCF to X'8', and (3) EPCF to X'0' (transmit initial). Output X'45' also resets the CS and PDF pointers in ICW byte 12 to X'F'.
- Output X'4D' to set the "address" and "control" characters in the first two PDF buffers selected by the CS pointers (X'F' and X'0'). The CS pointers now point to X'1', the PDF buffer for the first byte of data fetched by cycle stealing.
- Output X'49' to set ICW bytes 8 and 9 with the storage address of the first byte of data to be fetched by cycle stealing.
- Output X'48' to set (1) ICW byte 7 with the CS byte count and (2) ICW byte 6 with the extended portion of the storage address, the data chain flag, the message chain flag, and the cycle steal valid bit. If this is a "control" frame, the 3705 control program sets the CS byte count to zero and sets the cycle steal valid bit.

The scanner transmits (1) a PAD character (X'55') to synchronize the receive modem and a Flag character (X'7E'); both characters are forced by the PCF/EPCF states, (2) the "address" character from the first PDF buffer, (3) the "control" character from the second PDF buffer, and (4) the data characters fetched from the CCU storage data buffer by cycle stealing. When the CS byte count goes to zero and the data chain flag (ICW bit 6.6) is on, the scanner sets 'L2 interrupt pending' (ICW bit 5.1). This will cause an L2 service request at CS 8 time if 0.4 is on and notifies the control program to setup CSAR, the CS byte count, the flags, and CS valid for the next CCU storage data buffer. If the data chain flag is off, the scanner transmits all the data characters then the BCC character. The scanner then uses the status byte in ICW byte 15 to determine what ending character sequence to transmit. If the status byte does not specify a line turnaround (ICW bit 15.7 = 0), the scanner requests a level 2 interrupt. If the status byte specifies a line turnaround (ICW bit 15.7 = 1), the scanner changes to a receive monitor Flag state (5/0) with "Request to Send" active or inactive as determined by ICW bit 13.2 (RTS turnaround control). When the line turnaround is complete, the scanner requests a level 2 interrupt.

The scanner always transmits the data as it was received from storage by cycle stealing; no translation is done during an SDLC transmit operation. The scanner monitors the sequence of transmit data bits and when a consecutive sequence of 5 binary ones is noted, the scanner automatically inserts a binary zero bit before transmitting the next data bit. This includes the transmission of block check characters. Thus there will never be a consecutive sequence of transmitted binary one digits exceeding 5 within the frame except the Flag or Abort. The scanner generates the Flag, Abort and Idle characters as needed.

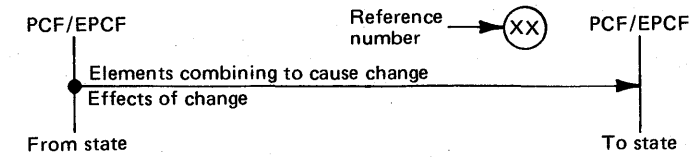
SDLC Transmit State-Transfer Diagram

Once the 3705 control program sets the PCF/EPCF states to 8/0 (transmit initial) to start the SDLC transmission, the control program turns over the execution of the entire transmit operation to the scanner. The scanner automatically changes the PCF/EPCF states as required based on the LCD state, the state of ICW bits (especially ICW byte 15), and others. The scanner uses the level 2 interrupt request to notify the control program when additional control program service is required. State-transfer diagrams are located in the ALDs to enable you to determine exactly what sequence the scanner followed in executing the transmit operation up to the interrupt.

The keying numbers refer to the data flow on F-440.

How to Read State-Transfer Diagrams

These state-transfer diagrams are read:



If for example: (see reference number 11)

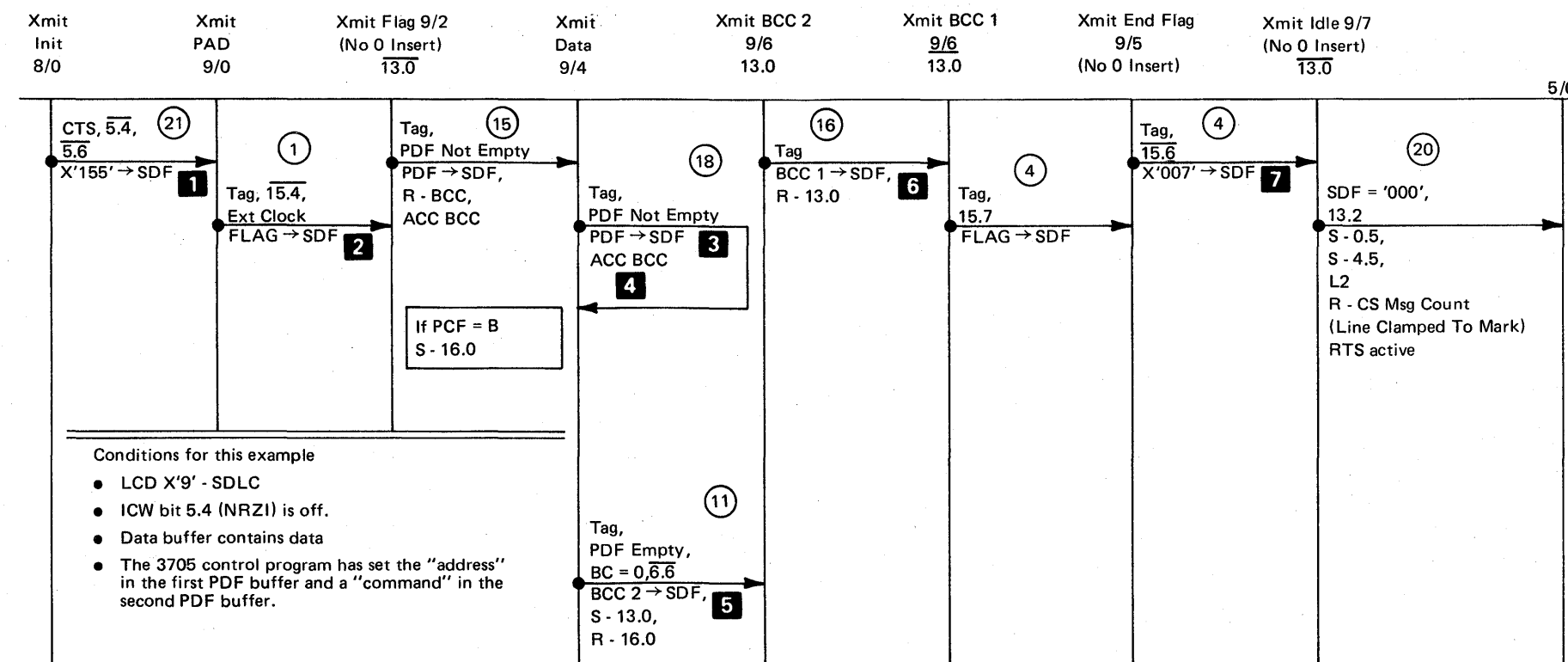
- The PCF = X'9' and
- The EPCF = X'4' and
- Tag has been detected and
- The PDF is empty (the CS pointer and PDF pointer select the same buffer) and

- The CS byte count has gone to zero and
- ICW bit 6.6 (data chain flag) is off

Then the scanner:

- Sets EPCF = X'6' and
- Transfers the low order byte of the BCC character (BCC 2) from ICW byte 11 to the SDF and
- Sets ICW bit 13.0 (seq 0) to indicate that the next character transmitted is the first of a multi-byte transmission and
- Resets ICW bit 16.0 (new sync).

Example of SDLC Transmit State-Transfer Diagram



Legend:

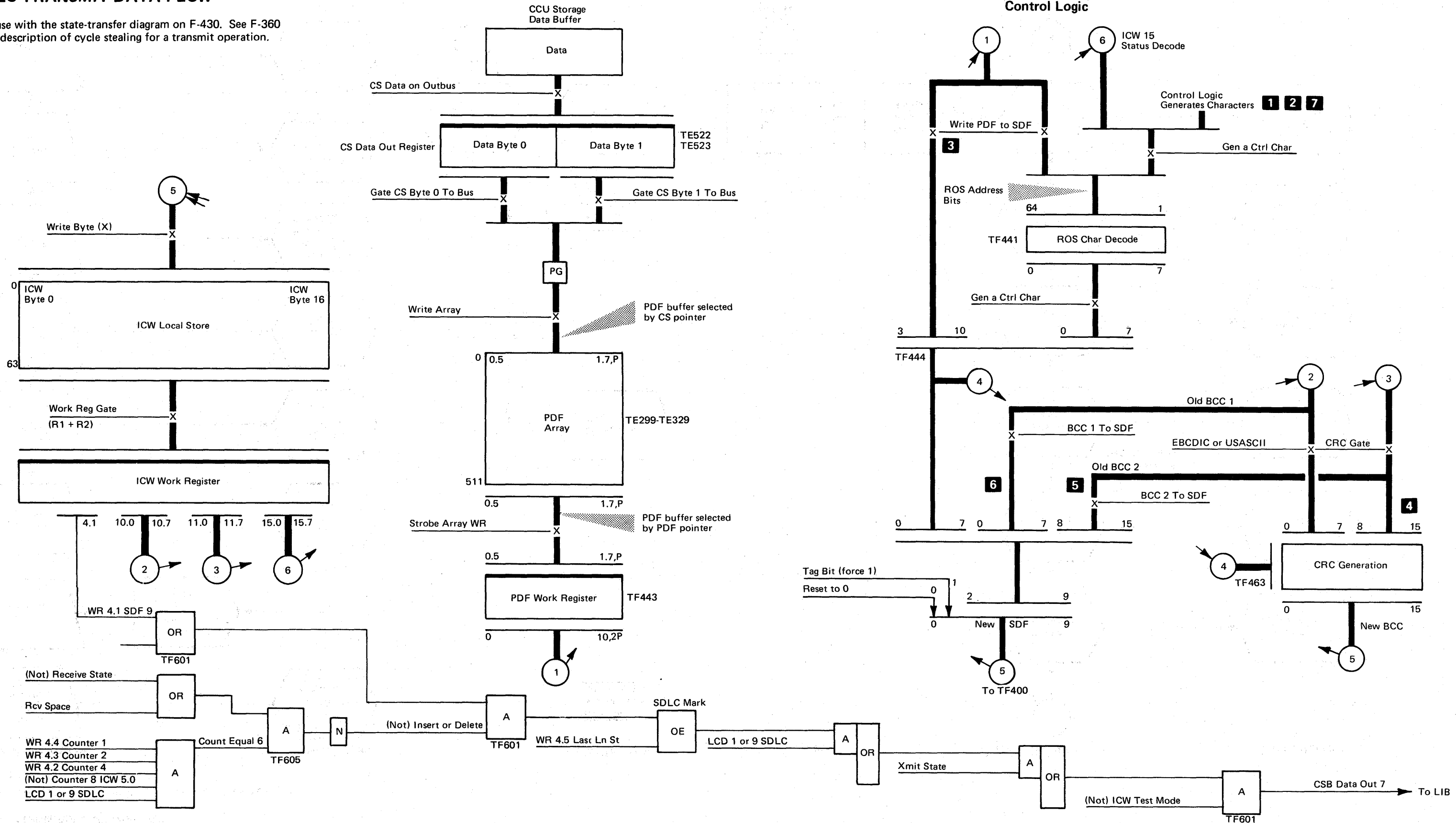
- S = Set
- R = Reset
- 8/0 = PCF X'8' and EPCF X'0'
- 13.0 = ICW bit 13.0 is 0 (Not seq 0)
- Tag = Tag detected as the last bit is transmitted from SDF 9.
- CTS = "Clear to Send" received from transmitting modem
- Ext Clock = Line is to use modem clock for bit service.

- X'155' → SDF means the scanner generates the PAD character X'55' for the SDF. The 1 is the tag bit set into SDF 1.
- L2 = Level 2 interrupt request
- ACC = Accumulate BCC
- (21) = Reference number used by the diagnostic engineer to refer you to this portion of the state sequence chart.

- + = OR
- = And
- P = PCF
- E = EPCF
- X'007' → SDF means the scanner generates the Idle character X'07' for the SDF. The 0 indicates that a tag bit is *not* set into SDF 1.

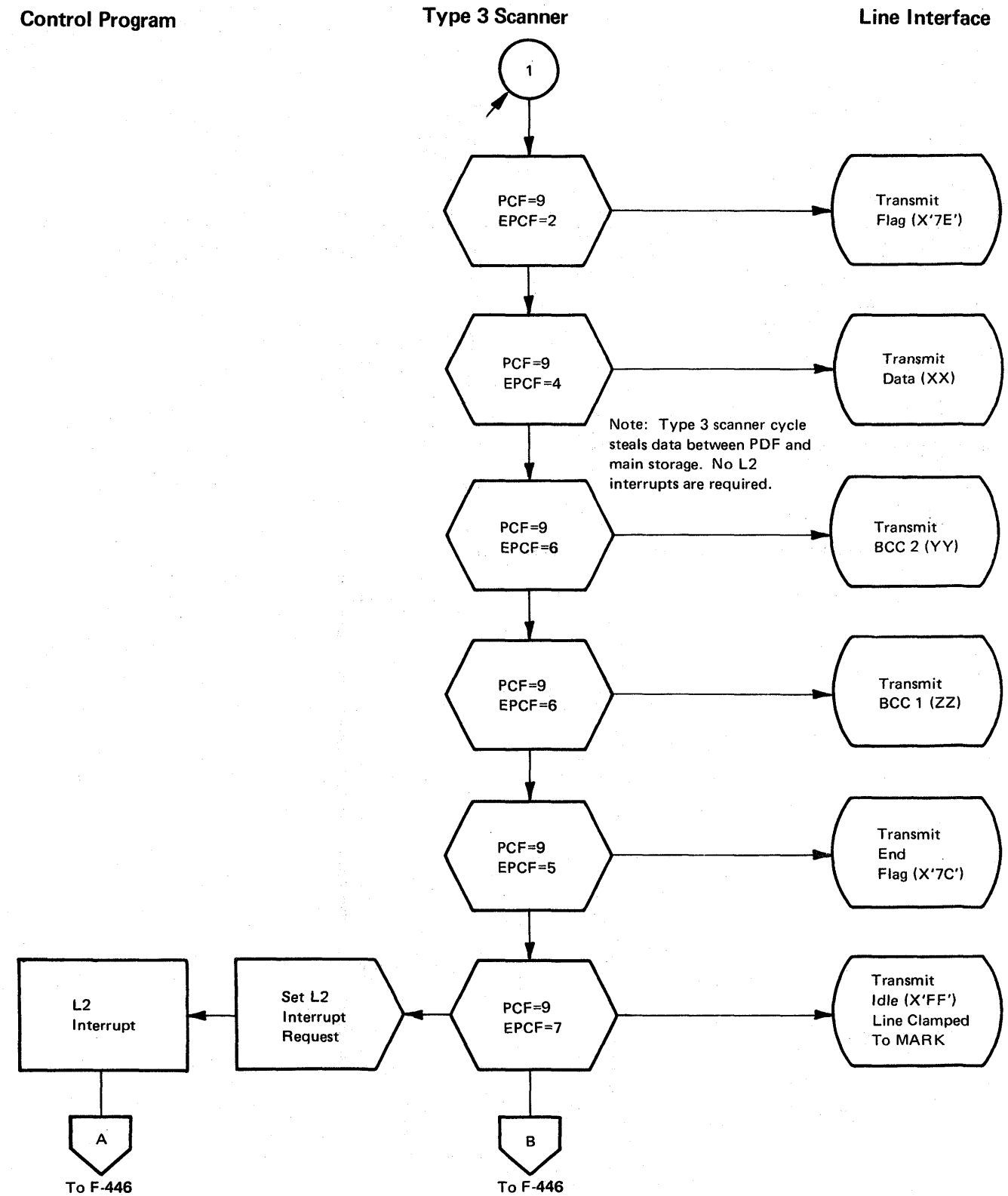
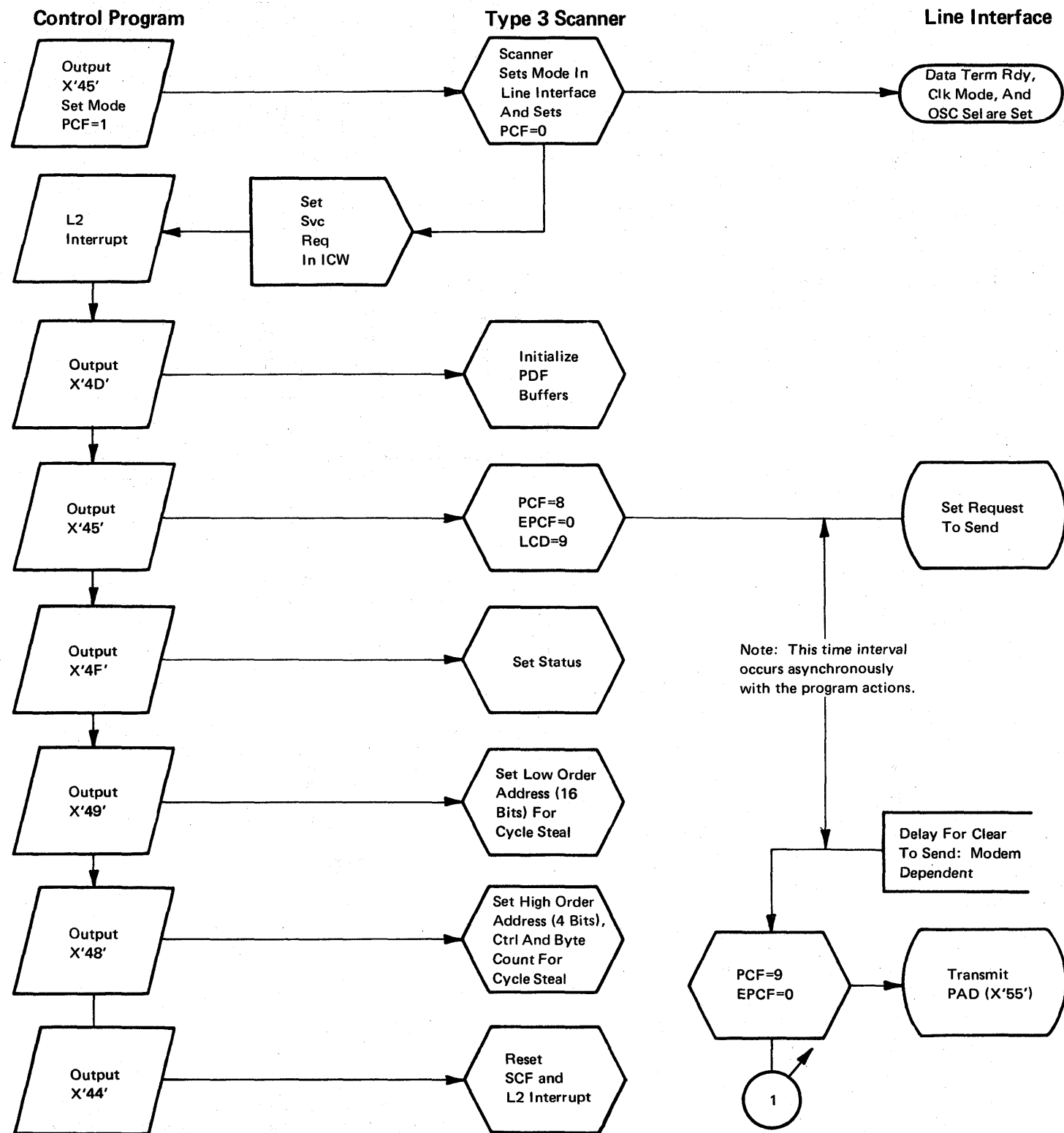
SDLC TRANSMIT DATA FLOW

For use with the state-transfer diagram on F-430. See F-360 for a description of cycle stealing for a transmit operation.

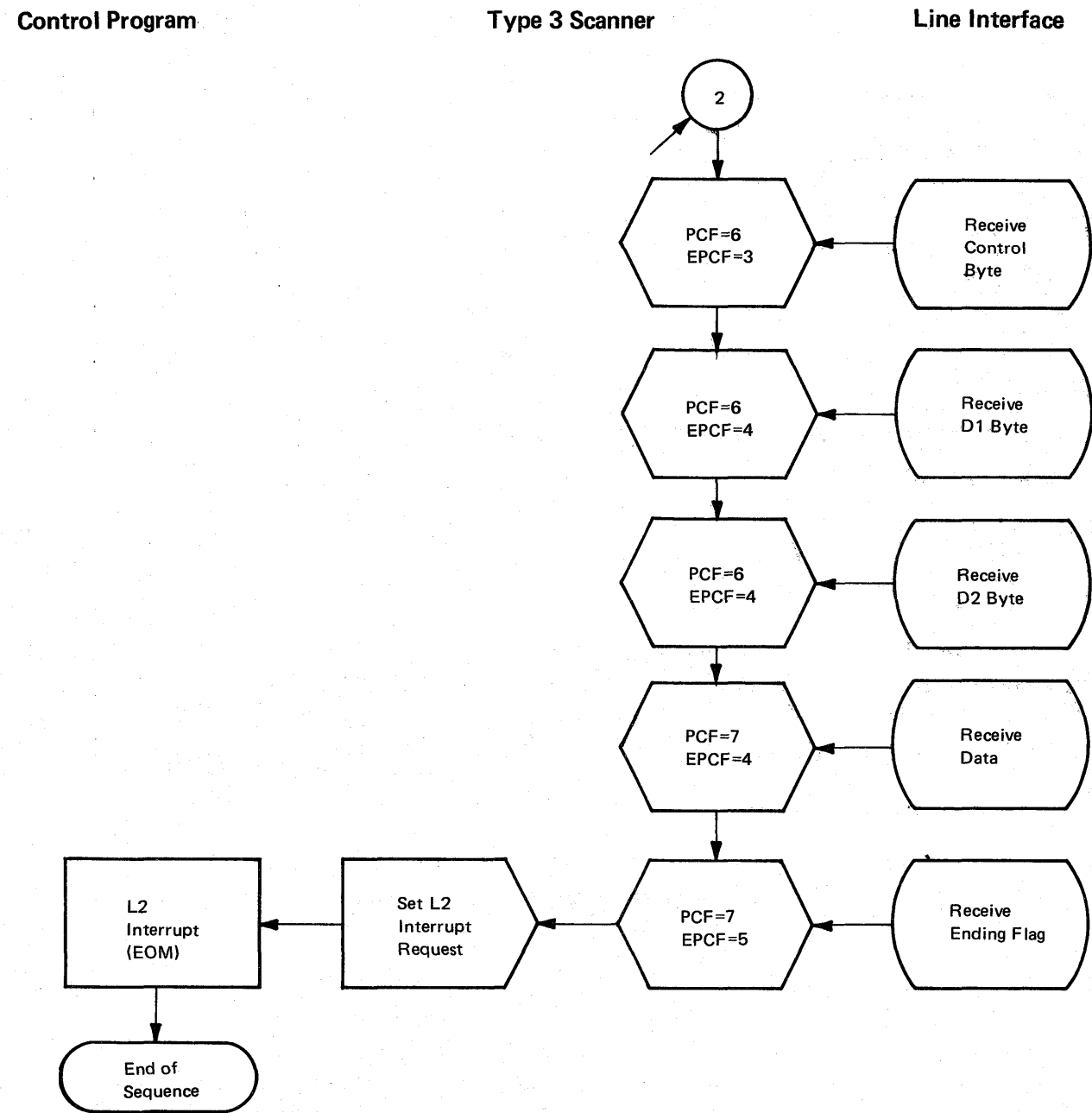
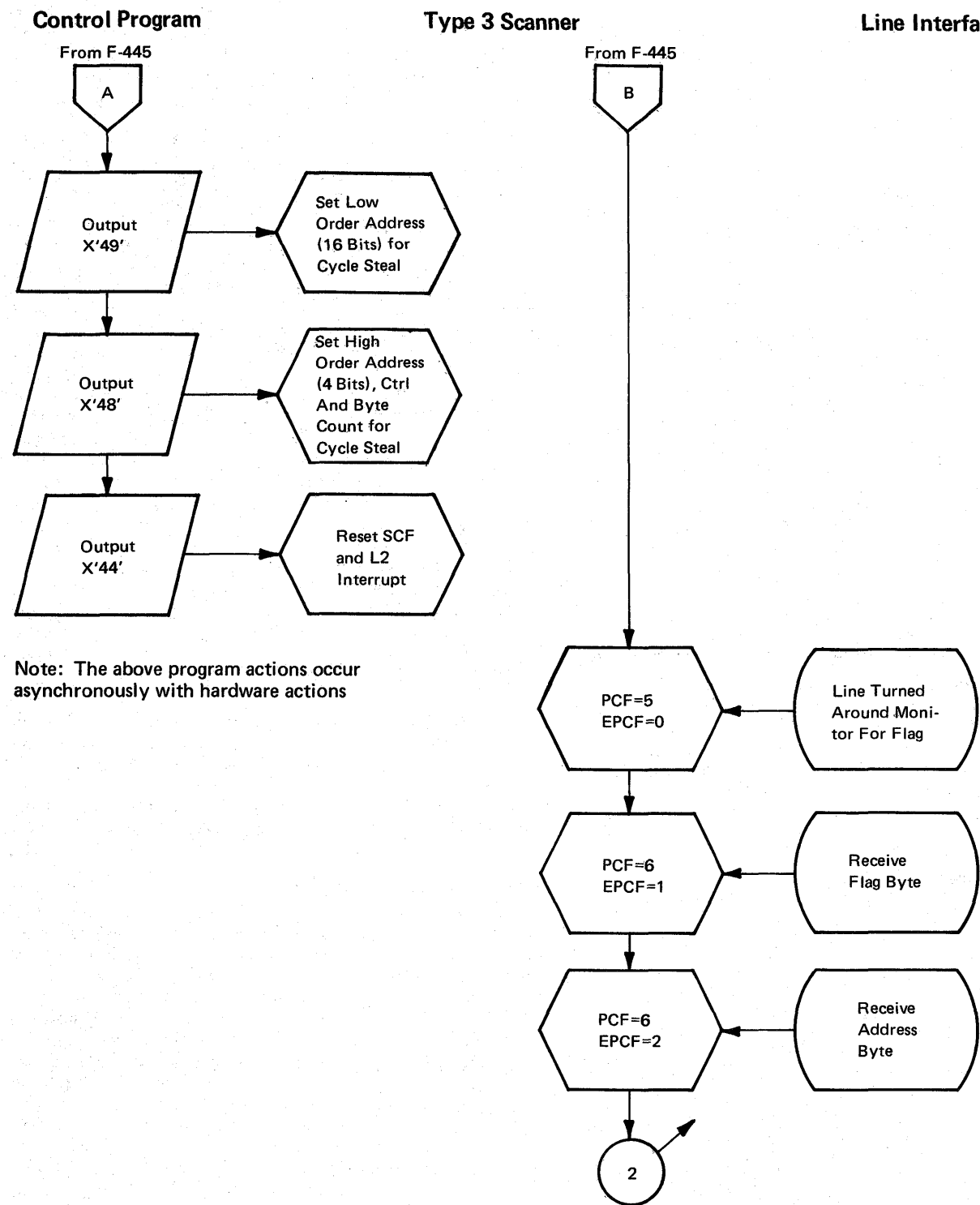


SDLC TERMINAL OPERATION

Note: This operation is in NCP mode over a non-switched half-duplex line



SDLC TERMINAL OPERATION (PART 2)



CYCLE STEAL OPERATION—RECEIVE

Introduction

During a receive operation, the scanner transfers data, control, and status to the PDF array depending on the LCD, PCF, and EPCF states. All data to be stored is first transferred from the SDF to the PDF array that is selected by the PDF pointers. At some later scan of this ICW, the scanner transfers the data, two bytes per cycle steal, from the PDF array (selected by the CS pointer) to main storage. Status bytes are buffered in the PDF array (after the data) and are transferred later to ICW byte 15 by the cycle steal interface hardware. Control bits are also buffered in the PDF array (after the data) and are used to set bits in ICW bytes 0 and 14 after the data preceding them has been stored.

Cycle stealing normally transfers two bytes at a time. When CSAR (cycle steal address register) initially addresses an odd storage location (CSAR bit 1.7 = 1), the scanner transfers data byte 1 to the storage data buffer and then increments CSAR update to an even address **1**. All subsequent data is transferred two bytes at a time.

The CS pointers determine which of the eight PDF buffers (associated with the selected ICW) transfers its data byte to storage. The initial state of the CS and PDF pointers is set by the 3705 control program (Output X'4E') or is reset to X'F' by an Output X'45' when the EPCF state is set. The scanner increments the CS pointer as each data byte is transferred to the 'cycle steal data in register'. The scanner also decrements the cycle steal byte count register and increments the CSAR update register.

The CS pointers determine which of the PDF buffers (associated with the selected ICW) transfers its data byte to storage. (See Note). The initial state of the CS and PDF pointers is set by the 3705 control program (Output X'4E') or is reset to X'F' by an Output X'45' when the EPCF state is set. The scanner increments the CS pointer as each data byte is transferred to the 'cycle steal data in register'. The scanner also decrements the cycle steal byte count register and increments the CSAR update register.

Note: Eight PDF buffers are associated with the type 3 scanner line set and 16 buffers are associated with the type 3HS scanner line set.

During a receive operation, the scanner transfers one data byte from the SDF to a PDF buffer when "tag" is detected. The PDF pointers determine which PDF buffer receives the data byte from the SDF. The scanner increments the PDF pointer as each data byte transfers to the PDF buffer.

When using BSC, the scanner initiates a cycle steal request to transfer two more bytes of data whenever two or more buffers of the PDF array associated with the selected ICW are loaded. When using SDLC, the scanner initiates a cycle-steal request when the content of the CS message count is incremented to a non-zero state as described on F-510 and shown in a logic flow on F-520. When using BSC, the scanner tests the states of the CS and PDF pointers to determine when two buffers (at least) are loaded. See F-460.

Scanner Tests For Loaded Buffers

At each 'bit service request' (except when (1) the array is empty, (2) the PDF pointer is selected, (3) the CS busy latch is on, or (4) a status or control character is in the PDF buffer selected by the CS pointer), the scanner steps the CS pointer by 1 and then compares CS pointer bits 12.1-12.3 with PDF

pointer bits 12.5-12.7 (CS pointer bits 12.0-12.3 with PDF pointer bits 12.4-12.7 for a type 3HS scanner). An unequal condition indicates that there are at least two loaded buffers so the scanner requests a cycle steal to transfer two bytes of data to the storage data buffer. An equal condition indicates that the buffers are either full or empty and a second test is made. The scanner compares CS pointer bit 12.0 with PDF pointer bit 12.4 (CS pointer bit 17.0 with PDF pointer bit 17.1 for a type 3HS scanner) and if they are equal, the array is empty. If they are not equal, the array is full. The array normally does not test as "full" once the CS pointer has been updated by 1.

Cycle Steal Operation—Receive

The keying numbers refer to the diagram on this page and F-460. The BSC receive example on F-470 will be used in this description.

The 3705 control program sets ICW bytes 8 and 9 with the storage address for the first byte of data to be stored. The 3705 control program then sets ICW byte 7 with the CS byte count and sets ICW byte 6 with the extended portion of the storage address and the cycle steal valid bit. CS valid (ICW bit 6.5) notifies the scanner that the address and byte count are valid and to request a cycle steal operation when two buffers are loaded (BSC). Refer to the "Cycle Steal Timing Chart—Receive", F-460, for details of the following sequence.

When 'bit service request' is active on the selected interface address, the scanner tests the pointers to determine if there are two loaded buffers in the PDF array associated with the selected interface address. The STX character has been transferred to PDF buffer 1111 but the next buffer, 0000 is empty. Therefore the first test **2** finds only one buffer loaded and the scanner does not set the 'CS request' latch. After the "data 1" character has been transferred to PDF buffer 0000, the next test **3** finds at least two buffers loaded and the scanner sets the 'CS request' latch **4**. This sends 'bid cycle steal' to the CCU. The scanner raises 'set CS registers' as long as 'CS busy' is off and this gates (1) the CS address from ICW work register bytes 6, 8, and 9 to CSAR and the 'CSAR Update' register **5** and (2) the CS byte count from ICW work register byte 7 to the CS byte count register **6**. 'Set CS request Lt' gates the ICW address to CBAR **7** where the selected address is saved for use in addressing the ICW during a following CCU time. At this time the STX and data 1 characters are loaded into the 'CS data in' register **8** and the CS byte count and 'CSAR update' register are updated. The 'CS busy' latch prevents all other scanned line-interface ICWs containing a 'CS valid' bit from requesting a cycle steal.

When the CCU can take a CS cycle, the CCU returns 'CS go CSB' **9** to the first scanner. If the first scanner did not request the cycle steal, that scanner propagates the 'CS go CSB' signal to the next scanner. This continues from scanner to scanner until the signal is trapped by the scanner that requested the cycle steal.

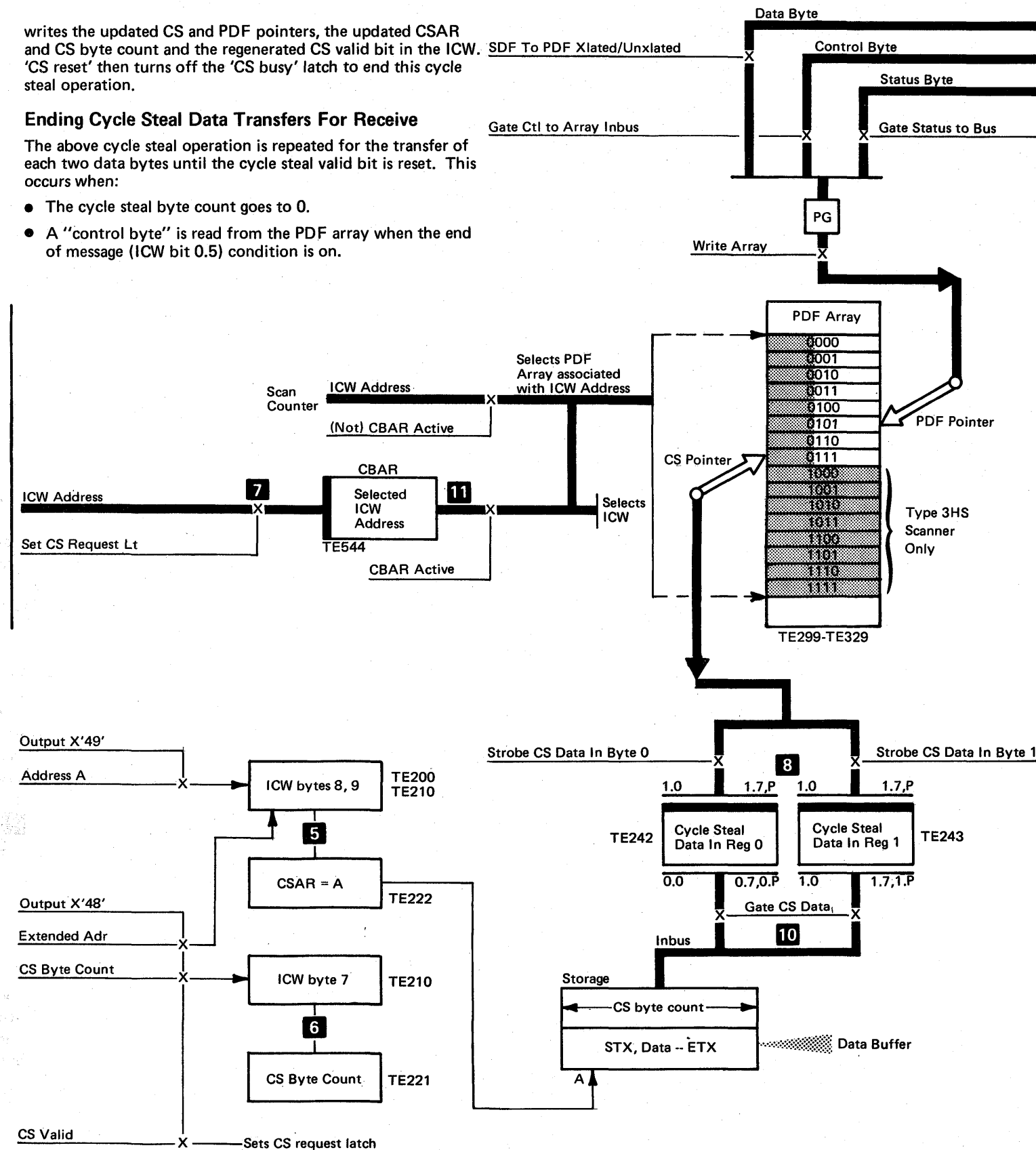
The scanner gates the address from CSAR to SAR where the CCU uses it to address the storage location for the data to be stored. When the CCU raises 'gate CS data on inbus', the scanner gates the data from the 'CS data in' register to the Inbus **10**. The scanner then requests access to the selected ICW during CCU time and, if there is no Output X'4X' nor a 'fetch buffer' operation underway, sets the 'CBAR active' latch. The address in CBAR then selects the ICW **11** and the scanner

writes the updated CS and PDF pointers, the updated CSAR and CS byte count and the regenerated CS valid bit in the ICW. 'CS reset' then turns off the 'CS busy' latch to end this cycle steal operation.

Ending Cycle Steal Data Transfers For Receive

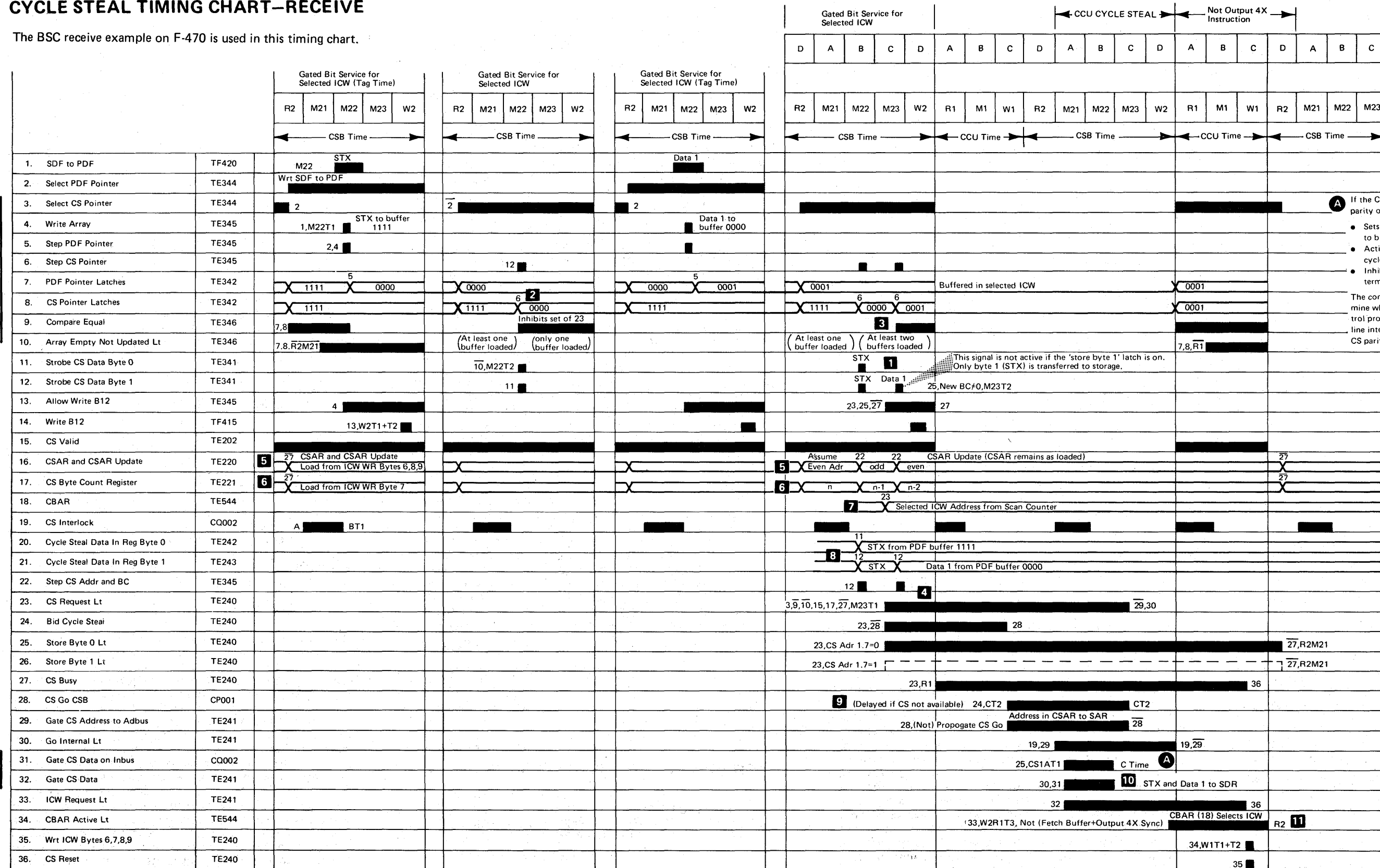
The above cycle steal operation is repeated for the transfer of each two data bytes until the cycle steal valid bit is reset. This occurs when:

- The cycle steal byte count goes to 0.
- A "control byte" is read from the PDF array when the end of message (ICW bit 0.5) condition is on.



CYCLE STEAL TIMING CHART—RECEIVE

The BSC receive example on F-470 is used in this timing chart.



A If the CCU detects a B register byte 0 or byte 1 parity check (even parity on the Inbus-CQ002) while cycle stealing, the scanner:

- Sets the 'CS parity error' latch (TE703). This causes the scanner to bid for a level 1 interrupt.
- Activates 'work reg or array or cs error' (TE706). This sets the cycle-steal address, currently in CBAR, into DBAR.
- Inhibits the regeneration of 'cycle steal valid' (ICW bit 6.5) that terminates the cycle-steal operation.

The control program executes an Input X'43' instruction to determine what caused the level 1 interrupt—bit 1.4 will be on. The control program executes an Input X'42' instruction to determine the line interface address (trapped in DBAR) that was active when the CS parity error occurred.

CYCLE STEAL TIMING CHART—RECEIVE

BSC RECEIVE

To initialize a line interface for a BSC (binary synchronous communication) receive operation, the 3705 control program must have performed a set mode to initialize the line set (oscillator, clocking, diagnostic mode, etc) and must (1) have previously set the line interface to a transmit state that ended with a line turnaround to the receive state, or (2) set the LCD/PCF/EPCF to a receive monitor state.

The scanner monitors the receive data stream for two consecutive SYN characters to acquire character phase. When the scanner decodes the first SYN character, the scanner sets EPCF to X'1', sets ICW bit 13.0 (seq 0), and continues to monitor the receive data stream (see F-500). If the next character received is not a SYN character, the scanner sets EPCF to X'0', resets ICW bit 13.0, and resumes monitoring for two consecutive SYN characters. If the second character detected is a SYN character, the scanner is in character phase and resets ICW bit 13.0. The scanner then decodes the next non-SYN character(s) to determine if a text message, control message, or a response message is being received.

Control Character(s)

If the scanner decodes SOH, STX, or DLE-STX as the first non-SYN character(s) at the beginning of a message, the scanner sets a corresponding initial status in ICW bits 15.0-15.2 **2**. If the LCD = X'C' or X'D' (NCP mode), the scanner discards the control character(s) (by not transferring them to the PDF). After the first data byte is received the scanner requests a level 2 interrupt to notify the network control program to assign a data buffer for the coming text. The network control program must also execute an:

- Output X'49' to set ICW bytes 8 and 9 with the storage address of the data buffer in which the first byte of data is to be stored by cycle stealing.
- Output X'48' to set (1) ICW byte 7 with the CS byte count and (2) ICW byte 6 with the extended portion of the storage address and the cycle steal valid bit.

If the LCD = X'4', X'5', or X'6' (EP mode), the emulation program would have (1) pre-assigned the first data buffer, (2) setup CSAR with the data buffer address (Output X'49') and (3) set-up the CS byte count and the cycle steal valid bit (Output X'48'). Therefore, for EP, the scanner transfers the control character(s) to the PDF so that they may be stored with the text that is received.

Control Characters Stripped from the Text—NCP Mode

Normal Text Mode

- SYN
- ETX
- ETB
- ENQ

Transparent Text Mode

- DLE-SYN sequence
- DLE-ITB sequence
- DLE-EXT sequence
- DLE-ETB sequence

- DLE-ENQ sequence
- First DLE of DLE-DLE sequence

Note: DLE-STX characters are not stripped from the text if it follows an ITB ending; data characters may intervene between the ITB ending characters and the DLE-STX characters.

Control Characters Stripped from the Text—EP Mode

Normal Text Mode

- SYN
- DLE-SYN sequence
- First DLE of DLE-DLE sequence

BCC Accumulation

The scanner accumulates the BCC on all characters received following STX, SOH or the first DLE-STX except SYN characters in normal text mode and the first DLE of a DLE sequence when in transparent text mode. The scanner includes the DLE and STX characters in the BCC accumulation when the DLE-STX sequence is received in normal text mode causing transparent mode to be set. The scanner does not include the DLE or SYN characters in the BCC accumulation when the DLE-SYN sequence is received in transparent text mode.

End Control Characters

When the scanner decodes an end-control character (ACK, NAK, RVI, WACK, TTD, EOT, DISC, ETB, DLE-ITB, DLE-ETX, or DLE-ETB) as an ending, the scanner sets a corresponding final status in ICW bits 15.3-15.6 (see F-150). If the LCD = X'C' or X'D' (NCP mode), the scanner discards the end-control character(s) (by not transferring them to the PDF). If the LCD = X'4', X'5', or X'6' (EP mode), the scanner transfers the end-control character(s) to the PDF so that they may be stored behind the text. The end-control character(s) are accumulated in the BCC if in text mode. If the BCC character follows the end-control character(s) the scanner receives and verifies the check characters for validity. The BCC character is not transferred to the data buffer unless ICW bit 0.7 (trace) is on and the control character is not ITB. In EP mode, with ICW 0.7 (trace), the scanner stores the BCC character (BCC 2 and BCC 1) behind the end-control character. In NCP mode with ICW 0.7 (trace), the scanner stores the BCC character behind the last data character. The BSC LRC/CRC characters are valid if the check remainder is X'0000'. If not, the scanner sets 'array bus in bit 5 dot' **8** in the control byte. This sets SCF control register bit 1.2 **9** when the CS pointer selects that PDF buffer which in turn sets ICW bit 14.3 (data check). In either case, the scanner sets ICW bit 0.5 (EOM), resets ICW bit 6.5 (CS valid bit) and requests a level 2 interrupt **7**. ICW bits 0.1 and 0.5 indicate a normal ending while ICW bits 0.5 and 14.3 (as well as 0.2, 0.3, 14.0, 14.1, 14.4, 14.6, or 14.7) indicate an abnormal ending.

BSC Receive State—Transfer Diagram

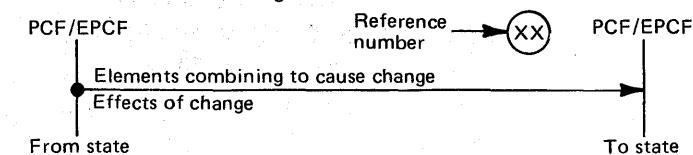
Once the PCF/EPCF state has been set to receive monitor phase, the 3705 control program turns over the execution of the entire receive operation to the scanner. The scanner automatically

changes the PCF/EPCF states as required based on the LCD state, the state of various ICW bits, the data characters in the received data stream, and others. The scanner uses the level 2 interrupt request to notify the control program when additional program service is required. State-transfer diagrams are located in the ALDs to enable you to determine exactly what sequence the scanner followed in executing the receive operation up to the interrupt.

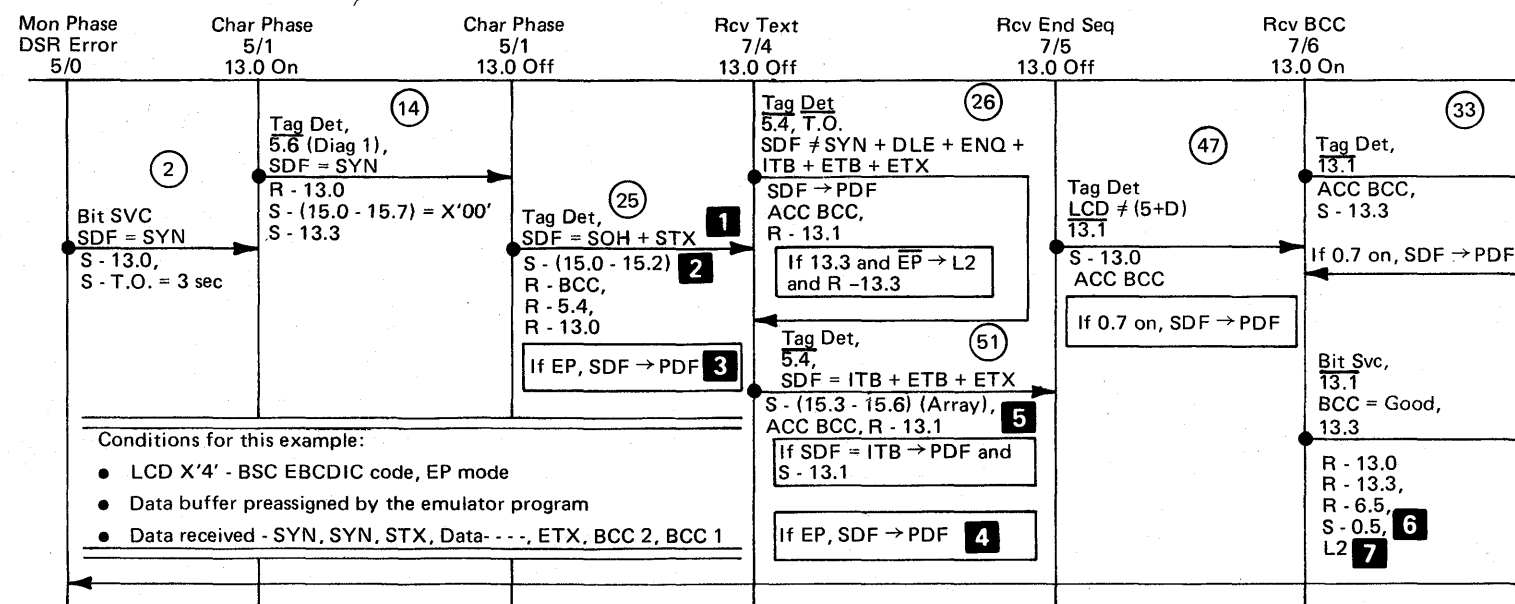
Selected sections of the state-transfer diagram for a BSC receive operation are shown below. This example has been used to illustrate (1) cycle steal operation-receive (F-450) and (2) BSC receive details (F-500). The data flow for this operation is on the facing page for your reference when examining this state-transfer diagram. The keying numbers refer to the data flow on F-480.

How to Read State—Transfer Diagrams

These state-transfer diagrams are read:



Example of BSC Receive State-Transfer Diagram



Legend:

S = Set
R = Reset
EP = Emulator Program Mode
7/4 = PCF X'7' and EPCF X'4'
13.0 = ICW bit 13.0 (seq 0) = 1
P = PCF
E = EPCF

ACC = Accumulate BCC
L2 = Level 2 interrupt request
EP = SOH + STX means the character just received in the SDF is decoded as a SOH or STX by the character decode register

(25) = Reference number used by the diagnostic engineer to refer you to this portion of the state-transfer diagram.
+ = OR
• = And

If, for example: (refer to reference number 51 below)

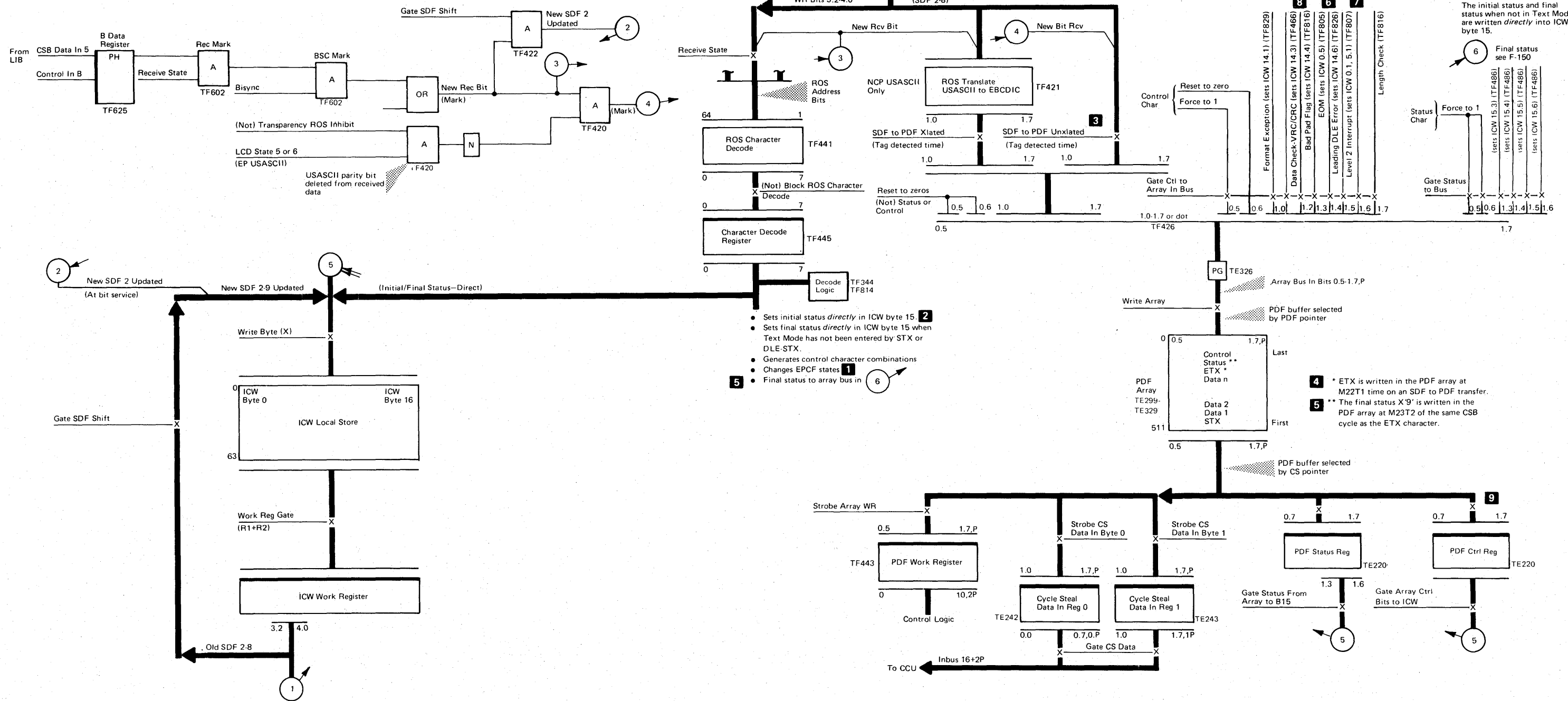
- PCF = X'7' and
- EPCF = X'4' and
- Tag has been detected as the last bit of the ETX character has been received and
- ICW bit 5.4 (transparency) is 0 and
- The character in the SDF is decoded as an ITB or ETB or ETX character (done in the character decode register)

Then the scanner:

- Sets EPCF = X'5' and
- Sets the final status code associated with the end-control character in 'array bus in bits 6-9' to write it into the PDF array. When this buffer is selected by the CS pointers the status is set into the PDF status register and PDF control register. The scanner gates the status from the PDF status register into ICW bits 15.3-15.6 and
- Accumulates the end-control character in the BCC and
- Resets ICW bit 13.1 (seq 1)-has no effect here and
- Transfers the end-control character to the PDF array since this example is in EP mode.

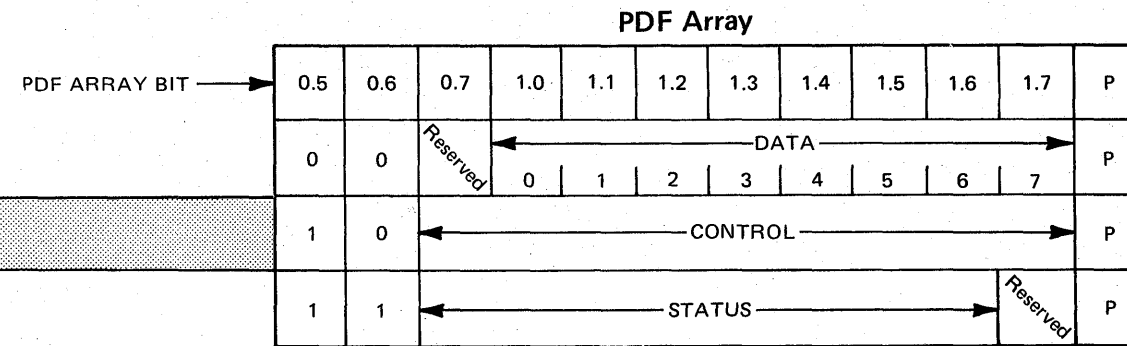
BSC RECEIVE DATA FLOW

For use with the state-transfer diagram on F-470. See F-450 for a description of cycle stealing for a receive operation.



PDF ARRAY/CONTROL REGISTER/STATUS REGISTER ENTRY FORMAT

RECEIVE STATE ONLY



The scanner writes the final status (shown below) for a BSC receive through the PDF array only after entering text mode (STX or DLE-STX). The scanner writes the initial and final status (shown on F-150) for a BSC receive directly to ICW byte 15 if text mode has not been entered.

PDF Control Register

Bit	SDLC	BSC
0.7	Set ICW 0.0 ((Abort Detect))	Reserved
1.0	Set ICW 14.1 (Idle Detect)	Set ICW 14.1 (Format Exception)
1.1	Reserved	Reserved
1.2	Set ICW 14.3 (Data check)-CRC	Set ICW 14.3 (Data check)-VRC/CRC
1.3	Set ICW 14.4 (Flag off boundary)	Set ICW 14.4 (Bad Pad)
1.4	Set ICW 0.5 (End of Message)	Set ICW 0.5 (End of Message)
1.5	Reserved	Set ICW 14.6 (Invalid DLE sequence)
1.6	Set ICW 14.7 (Length Check)	Set ICW 14.7 (Length Check)
1.7	Set L2 Interrupt	Set L2 Interrupt

PDF Status Register

Bit	SDLC	BSC
0.7	Set ICW 15.0 (Control Exception)	0
1.0	0	0
1.1	0	0
1.2	0	0
1.3	0	Ending Character or Timeout
1.4	0	Detected
1.5	0	Reserved
1.6	0	Reserved
1.7	Reserved	Reserved

FINAL STATUS BSC RECEIVE

1.3	1.6	
0 0 0 0	Timeout	
0 0 0 1	ITB	
0 0 1 1	ENQ	
1 0 0 1	ETX	
1 0 1 0	ETB	

BSC RECEIVE DETAILS

This example illustrates the details for receiving the PAD, two SYNs, and the STX characters as shown on F-470.

Note: This example uses LCD = 4 (EBCDIC code-Emulation Program).

The scanner shifts the received data (PAD and SYN) through the SDF (serial data field) at each bit service request looking for the sync configuration. 'PCF state 5' causes 'SDF shift' that gates each 'new rcv bit' into SDF 2 position while shifting the contents of SDF 2-8 positions. Zeros are placed in SDF 0, 1 since nothing shifts into these positions. The 'new rcv bit' and SDF 2-8 are sampled in the ROS character decode circuit each gated bit service until ROS decodes a SYN character (TF344) **1**. During this bit service, the scanner:

- Sets EPCF = X'1' that modifies PCF X'5' to "character phase" (TE321) **2**.
- Sets ICW bit 13.0 (sequence 0)-TF802. This indicates the first of a two-byte sequence (character phase).
- Sets the contents of the ones counter in ICW byte 4 to 00010 to start a 3 sec timeout (TF603).
- Blocks 'SDF shift' and 'SDF direct' to reset the SDF to zeros (TF506).
- Inserts a tag bit in SDF 2 (TF821) **3**.

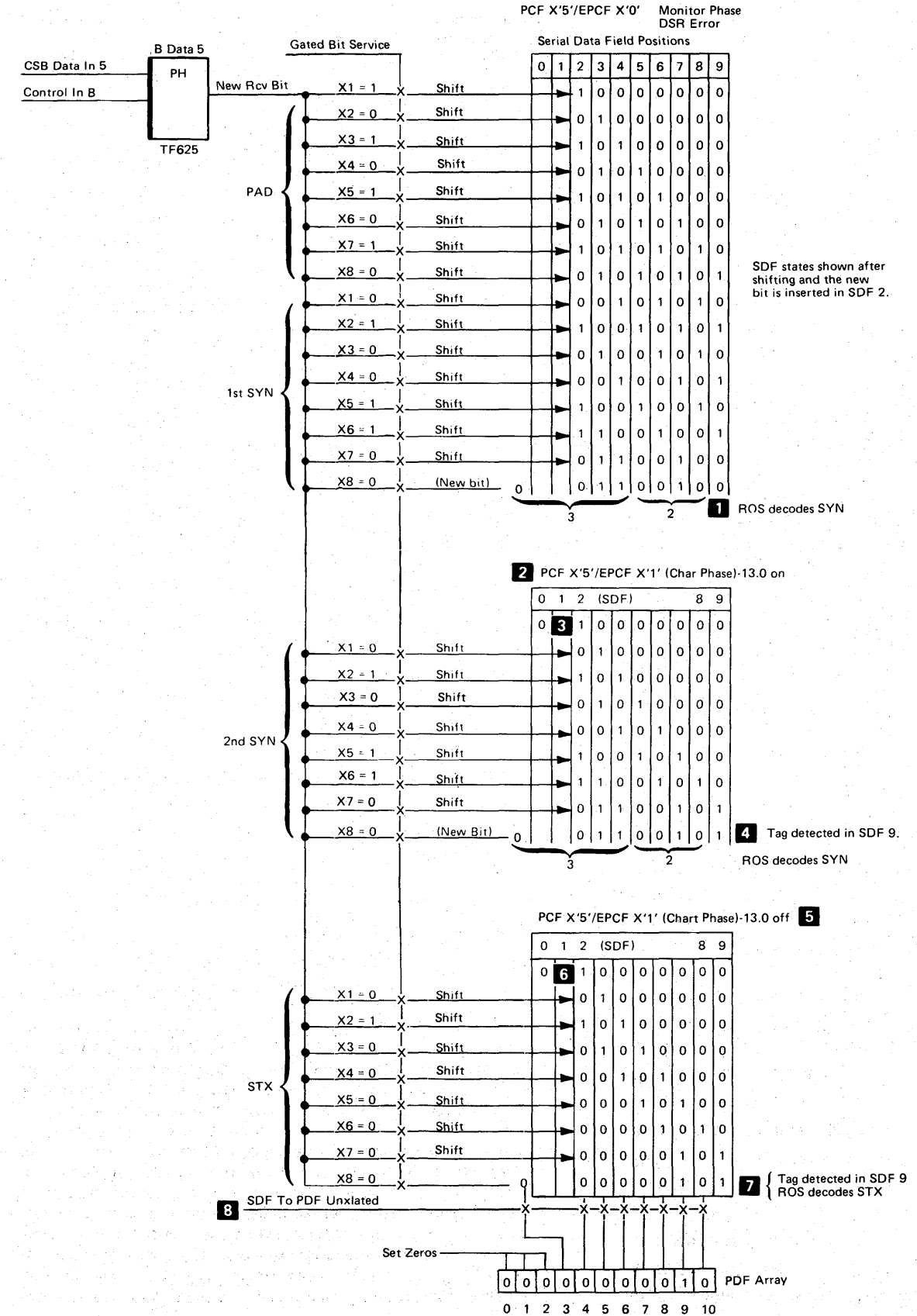
The scanner shifts the received data (SYN) through the SDF at each bit service request until the tag bit is detected in SDF 9 (TF422) **4**. ROS also decodes the SYN character during this bit service request. During this bit service, the scanner:

- Resets ICW bit 13.0 (sequence 0)-TF802 **5**. This indicates the second of a two-byte sequence (character phase).
- Sets ICW bit 13.3 (sequence 2)-TF485. (Not used for EP).
- Blocks 'SDF shift' and 'SDF direct' to reset the SDF to zeros (TF506).
- Inserts a tag bit in SDF 2 (TF821) **6**.
- Set ICW byte 15 = X'00' (TF342/3).

The scanner shifts the received data (STX) through the SDF at each bit service request until the tag is detected (TF422) **7**. ROS also decodes the STX character. During this bit service request, the scanner:

- Resets ICW bit 13.0.
- Brings up 'write SDF to PDF' (LCD specifies EP)-TF812. This:
 - Allows 'SDF to PDF unxlated' **8** to gate the STX character from the 'new rcv bit' and SDF 2-8 to the PDF (TF420).
 - Brings up 'write array' that writes the STX character into the PDF array address selected by the combination of the ICW address bits and the PDF pointer (TF812).
 - Increments the PDF pointer count by 1 (TE345).
- Raises 'initialize BCC' (TF826) that:
 - Inhibits generating a new BCC and writes zeros to ICW bytes 10 and 11.
 - Resets ICW bit 5.4 (BSC transparent text)-TF821.
- Blocks 'SDF shift' and 'SDF direct' to reset the SDF to zeros (TF506).
- Causes 'SDF to PDF unxlated' to set a tag in SDF 2 (TF422).
- Sets PCF X'7' (TF504).
- Sets EPCF X'4' that modifies PCF X'7' to "receive text" (TF323).

The scanner continues to receive the text characters.



SDLC RECEIVE

To initialize a line interface for an SDLC (synchronous data link control) receive operation, the network control program must (1) have performed a "set mode" to initialize the line set (oscillator, clocking, diagnostic mode, etc) (2) have previously set the line interface to a transmit state that ended with a line turnaround to the receive state or (3) set the LCD/PCF/EPCF to a receive monitor state with an Output X'45' instruction. Output X'45' also resets the CS and PDF pointers in ICW byte 12 to X'F'. The network control program must also execute an:

- Output X'49' to set ICW bytes 8 and 9 with the storage address of the assigned data buffer in which the "address" and "control" bytes will be stored by cycle stealing.
- Output X'48' to set (1) ICW byte 7 with a CS byte count of two and (2) ICW byte 6 with the extended portion of the storage address and the cycle steal valid bit.

The scanner monitors the receive data stream for a Flag character X'7E'. The low order bits of the ones counter (ICW bits 4.2-4.4) count the ones as they are received. The scanner detects the Flag when the count equals 7 and the next bit received is a space (0)-See TF602. The Flag character is not transferred to the data buffer in CCU storage. If ICW bit 5.6 (diag 1) is off, the scanner changes to PCF X'6'/EPCF X'1' state. The scanner remains in this state as long as Flag characters are received. The first non-Flag/non-Abort character (address) sets EPCF to X'2'. The scanner transfers the address character to the PDF array and accumulates the BCC. When the next character is assembled in the SDF, the scanner sets EPCF X'3' (provided a Flag or Abort character was not detected), writes the control character in the PDF buffer selected by the PDF pointer, and accumulates the BCC. The scanner tests the control character to determine if an information or supervisory control frame is currently being received. If bit 7 of the control character is a zero, the frame being received is an information frame: if bit 7 is a one, the frame is a supervisory frame **6**.

Information Frame

As long as the CS message count (ICW bits 13.6-13.7) is 00 during a receive state and when using SDLC, the signal 'inhibit CS access to PDF' (TF801) picks the 'select PDF pointer' latch every bit service **7**. This inhibits setting the 'CS request' latch. If 'WR 4.0-SDF 8' (bit 7 of the control character is in SDF 8 when the tag bit is detected in SDF 9) is a zero, or ICW bit 0.7 (trace) is on, **8**, the scanner increments the CS message count and sets ICW bit 13.1 (seq 1). Since the CS message count is no longer 00, the 'inhibit CS access to PDF' signal drops and allows a CS request. This occurs at the bit service that follows the bit service during which the tag was detected and the control character was written into the PDF buffer. The scanner now transfers the "address" and "control" characters to the data buffer by cycle stealing and the CS byte count goes to zero. The scanner then requests a level 2 interrupt to notify the network control program to set up the storage address for the next data buffer, set the new CS byte count and set the CS valid bit. The scanner continues to receive the data from the line and store it in the data buffer until the ending Flag is received. This signals the scanner to load a control byte (set bits for EOM and level 2 interrupt) in the PDF buffer selected by the PDF pointers and to check the validity of the check characters

received. The SDLC CRC checking is valid if the check remainder is X'F0B8'. Note: the SDLC CRC is stored in complement form. If the check is not valid, the scanner also sets 'array bus in bit 1.2 dot' **9** in the control byte that is written in the PDF buffer. This sets PDF control register bit 1.2 **10** (when that PDF buffer is selected by the CS pointer) that in turn sets data check (ICW bit 14.3). In either case, the scanner sets ICW bit 0.5 (EOM), resets ICW bit 6.5 (CS valid bit) and requests a level 2 interrupt **5**. ICW bits 0.1 (normal service request) and 0.5 indicate a normal ending while ICW bits 0.5 and (0.2, 0.3, 14.0, 14.3, 14.4, 14.6, or 14.7) indicate an abnormal ending.

Supervisory Frame

When the ending Flag character is detected, the scanner decrements the PDF pointers by two (to back over the two BCC bytes) and sets ICW bit 13.3 (seq 2)-see reference number 51 on the SDLC Receive state-transfer diagram in the ALDs page TD007. At the next bit service time (see reference number 52 on ALD page TD007) the scanner checks the validity of the check characters received and if the check is valid, the scanner (1) resets ICW bit 13.3, (2) sets EOM and a level 2 interrupt condition in the PDF control byte, (3) increments the CS message count to "not 00". 'Select CS pointer' becomes active and allows the cycle steal operation to transfer the "address" and "control" characters to the data buffer and the PDF control byte to ICW bytes 0 and 14. If the SDLC CRC check is not valid, the scanner sets data check as explained under Information Frame in addition to the five items listed above.

If a Flag or Abort is received instead of the address, control, BCC 2, or BCC 1 characters, the scanner returns to the monitor-for-Flag state without setting any error bits. If the Flag character does not follow the BCC 1 character, the scanner sets ICW bit 15.0 (control exception) **11** through the PDF array and continues receiving data as if this were an information frame.

Conditions That Cause a Level 2 Interrupt

- The CS byte count goes to zero while still receiving data.
- The scanner detects an ending Flag character. The EOM **4** is passed through the PDF array so that the EOM is not presented to the network control program until all the data, including the BCC, has been stored.
- The line goes idle **12** (16 ones) while receiving data. The Abort bit (ICW bit 0.0) is set with the Idle bit (ICW bit 14.1).

SDLC Receive State-Transfer Diagram

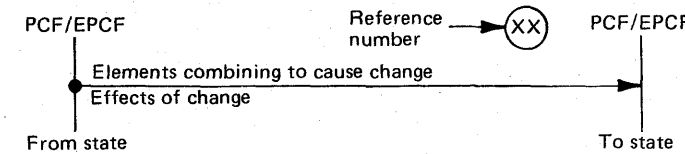
Once the PCF/EPCF state has been set to receive monitor phase, the network control program turns over the execution of the

entire receive operation to the scanner. The scanner automatically changes the PCF/EPCF states as required based on the state of various ICW bits, the Flag and Abort characters in the received data stream, and others. The scanner uses the level 2 interrupt request to notify the network control program when addition program service is required. State-transfer diagrams are located in the ALDs to enable you to determine exactly what sequence the scanner followed in executing the receive operation up to the interrupt.

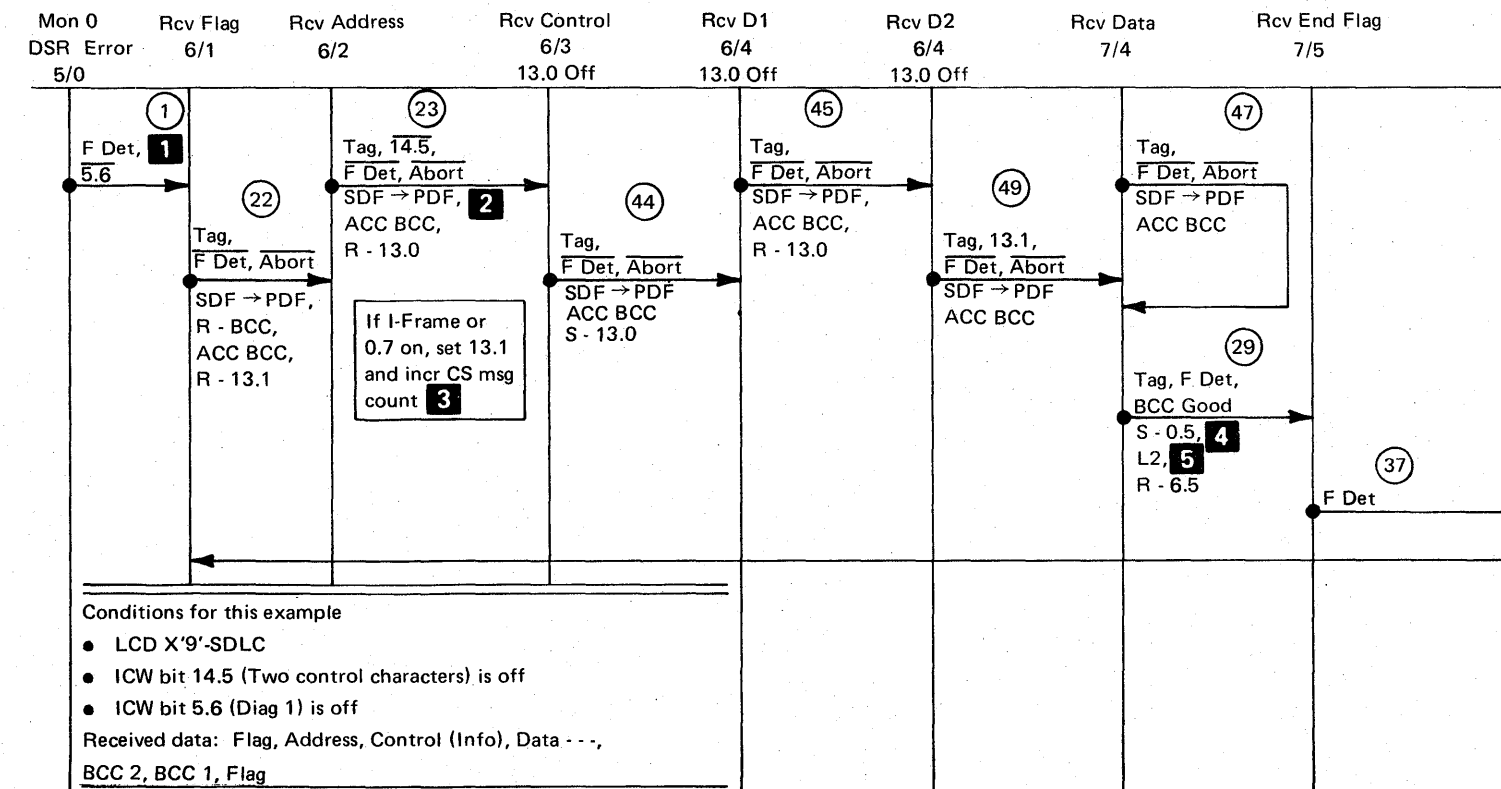
Selected sections of the state-transfer diagram for an SDLC receive operation are shown below. The data flow for this operation is on the facing page for your reference when examining this state-transfer diagram. The Keying numbers refer to the data flow on F-520.

How to Read State-Transfer Diagrams

These state-transfer diagrams are read:



Example of SDLC Receive State-Transfer Diagram



Legend:

- S = Set
- R = Reset
- 6/1 = PCF X'6' and EPCF X'1'
- 13.0 = ICW bit 13.0 (seq 0) = 1
- P = PCF
- E = EPCF
- ACC = Accumulate BCC
- L2 = Level 2 interrupt request
- F Det = Flag character has been detected
- ②③ = Reference number used by the diagnostic engineer to refer you to this portion of the state-transfer diagram
- + = OR
- = And

If for example: (refer to reference number 23 below).

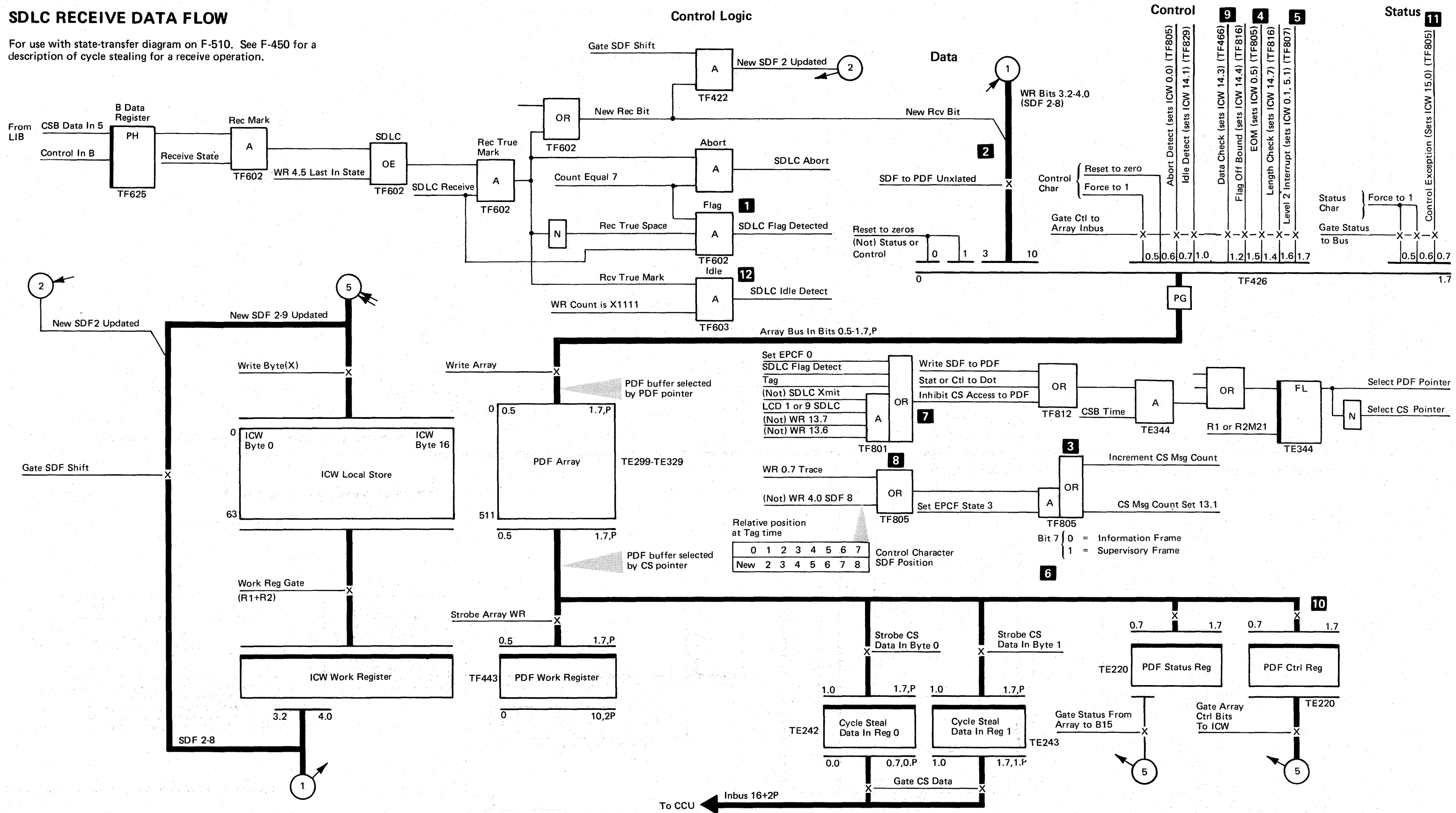
- PCF = X'6' and
- EPCF = X'2' and
- Tag is detected when the last bit of the control or command character is received and
- ICW bit 14.5 (two control characters) is off and
- The character just received in the SDF is not a flag or abort

Then the scanner:

- Sets EPCF = X'3' and
 - Transfers the received control/command character in the SDF to the PDF and
 - Accumulates the BCC for the control/command character and
 - Resets ICW bit 13.0 (has no effect here).
- If this is an information frame or ICW bit 0.7 (trace) is on, the scanner:
- Sets ICW bit 13.1 (seq 1) and
 - Increments the CS message count (ICW bits 13.6-13.7).

SDLC RECEIVE DATA FLOW

For use with state-transfer diagram on F-510. See F-450 for a description of cycle stealing for a receive operation.



DATA IN/OUT-LIB TO SCANNER

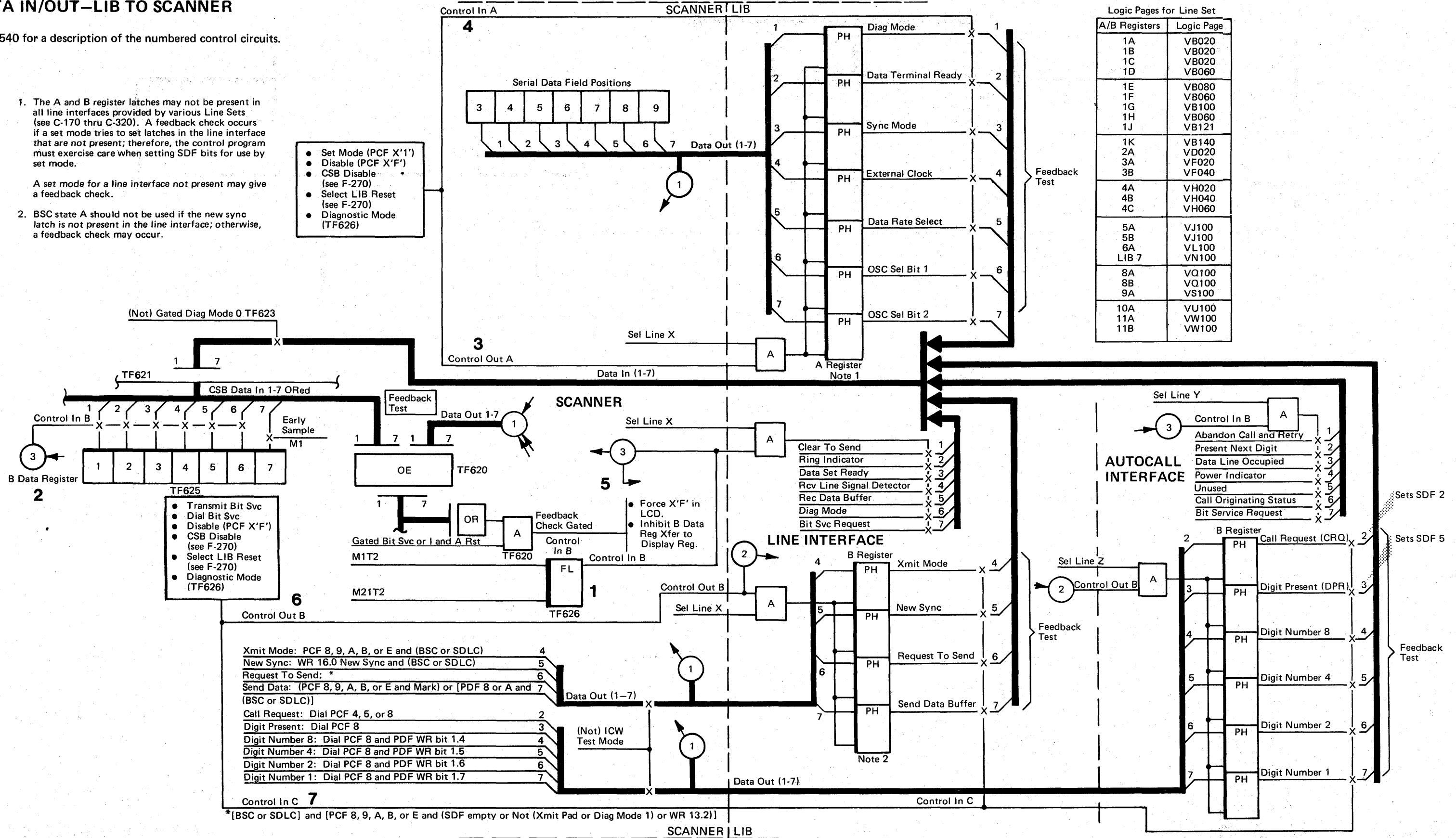
See F-540 for a description of the numbered control circuits.

- Notes:
- The A and B register latches may not be present in all line interfaces provided by various Line Sets (see C-170 thru C-320). A feedback check occurs if a set mode tries to set latches in the line interface that are not present; therefore, the control program must exercise care when setting SDF bits for use by set mode.
 - BSC state A should not be used if the new sync latch is not present in the line interface; otherwise, a feedback check may occur.

- Set Mode (PCF X'1')
- Disable (PCF X'F')
- CSB Disable (see F-270)
- Select LIB Reset (see F-270)
- Diagnostic Mode (TF626)

Logic Pages for Line Set

A/B Registers	Logic Page
1A	VB020
1B	VB020
1C	VB020
1D	VB060
1E	VB080
1F	VB060
1G	VB100
1H	VB060
1J	VB121
1K	VB140
2A	VD020
3A	VF020
3B	VF040
4A	VH020
4B	VH040
4C	VH060
5A	VJ100
5B	VJ100
6A	VL100
LIB 7	VN100
8A	VQ100
8B	VQ100
9A	VS100
10A	VU100
11A	VW100
11B	VW100



DATA IN/OUT LIB INTERFACE, PART 2

Description for F-530. The numbers refer to control circuits shown on F-530.

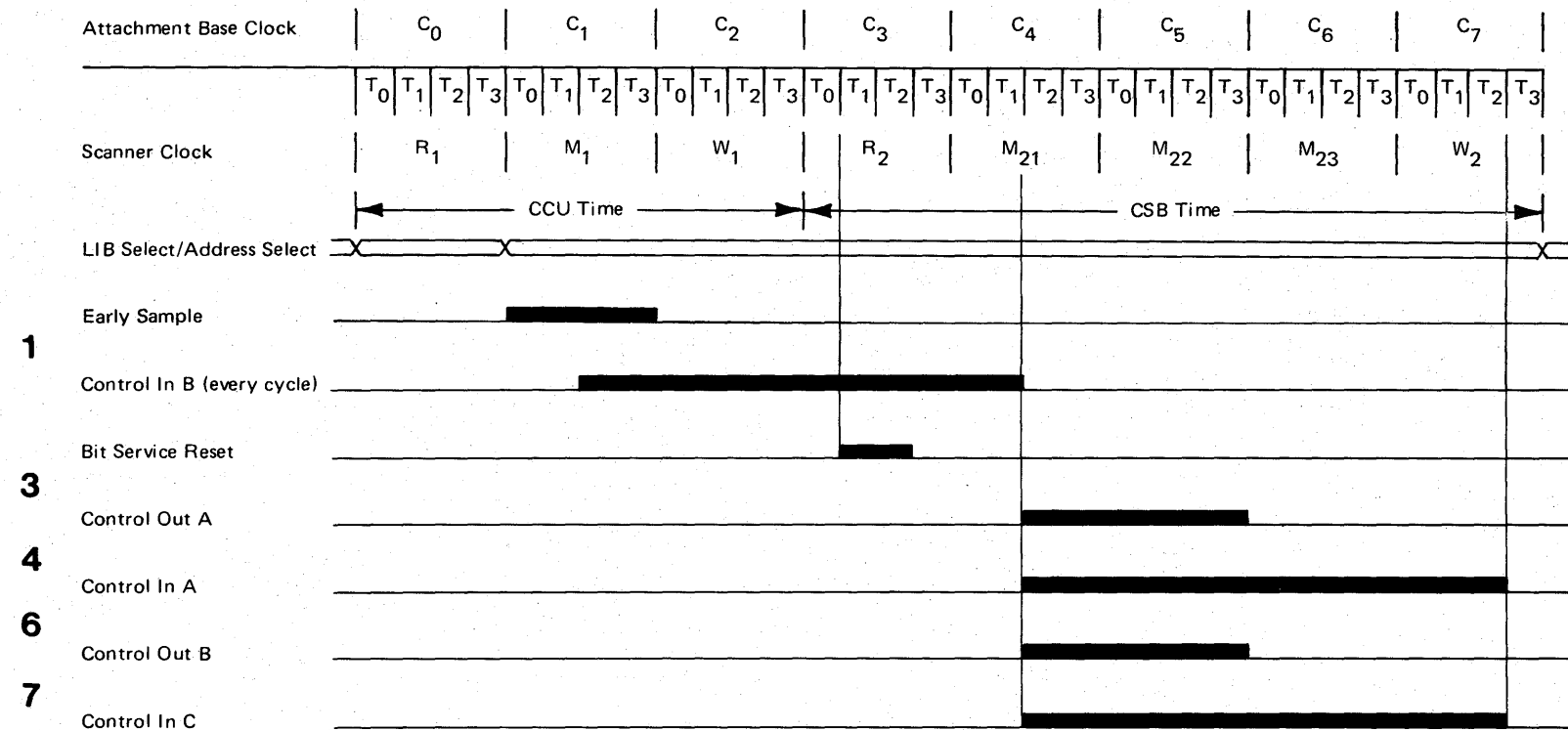
- 1 Every 1.6 (3705-1) microseconds during scan addressing, the type 3 scanner selects a line interface, or auto call interface, by sending that interface address to the LIB and interface over the 'LIB select' and 'address select' lines (see Note). The scanner sends a 'control in B' signal to the interface that gates the status of certain data communication equipment lines and certain latches in the interface hardware back to the scanner.
- 2 This status is stored in the B data register and is available to the control logic and the display register. See F-220 for the status bits buffered in the B data register.
- 3 PCF state X'1' (set mode) gates the set mode SDF bit configuration over the data out lines and gates this data into the 'A register' of the scanned interface by sending the 'control out A' signal. Bit service request is not required to set the 'A register' and the scanner gates this data to the A register every scan time until a bit service does occur. The scanner then sets PCF = 0 and requests a L2 interrupt.
- 4 The scanner ensures the latches are set to the correct value by sending 'control in A' to the interface hardware which gates feedback signals (from those latches just set) over the data-in lines to the scanner.
- 5 At gated bit service, if any latch does not agree with the value to which it was to have been set, a feedback error results which sets the LCD field to hex 'F'. This temporarily suspends scanner-to-interface action for that line. Level-2 interrupts for the faulty interface are also suppressed except for set mode. These errors must be recognized by a periodic scan of the LCD fields for all interfaces. The 3705 interval timer is used to provide this periodic scan of the LCD fields. Line and autocal interface feedback error detection is at the interface level; but if failures are detected in a group of interfaces, the interface hardware, type 3 scanner hardware or program logic may be at fault.
- 6 With 'bit service' on, a transmit or autocal operation sends 'control out B' to the interface and control logic places the appropriate bits on the data out lines.
- 7 The 'control in C' signal, sent to the interface, causes a feedback test.

- 3 & 6 The CSB disable latch turns on by executing Output X'43' (1 in byte 0, bit 0 and 1 in byte 1, bit 6), by an IPL reset, by the control panel Reset pushbutton, or by power on/off reset. When the CSB disable latch is on, the data out lines are held off while 'control out A' and 'control out B' are sent to the interface to reset the hardware latches. A feedback test then occurs (See F-530).
- 3 At each scan time, a disable (PCF state F) sends 'control out A' and 'control out B' to the interface with data out lines held off to reset the control latches in the LIB. The fall of 'data terminal ready' signals the data communications equipment that the interface is disabled and for the data communications equipment to terminate that connection. A feedback test then occurs. The scanner will not finish the disable sequence, set PCF 0, or request a L2 interrupt until bit service time.
- 3 & 6 The diagnostic mode latch turns on by executing Output X'43' with bits 0.0 and 0.6 set to 1. When the diagnostic mode latch is on, the data out lines are held off while 'control out A' and 'control out B' are sent to the interface to reset the hardware latches. A feedback test then occurs.

- 3 & 6 When Output X'43' is executed with the set function on (1 in 0.0) and any 'disable LIB position 1-6' on (1 in corresponding byte and bit), the line 'select LIB reset' is active while scanning the interface/autocal lines on the disabled LIB. At this time the data out lines are held off while 'control out A' and 'control out B' are sent to the interface to reset the hardware latches. A feedback test then occurs. (See F-530).
 - Two signals are sent from the type 3 scanner to the interface without any control signals to gate them. These are the 'reset bit service' and 'test data' lines.
 - The 'reset bit service' line resets the 'bit service' latch in the interface hardware on the cycle in which it is sensed. This notifies the interface hardware that the service request has just been honored. A feedback check then occurs.

- When diagnostic wrap mode is used, the scanner places the transmitted data of the diagnostic transmit line in a 'test data' latch in the type 3 scanner hardware. The receive lines sample the state of this 'test data' latch and use it as received data.
- Bit Overrun Reset
Grounded in the scanner
- LIB Active In
Held at the down level in the scanner
- Auto Call Present
Terminated in the scanner but not used.

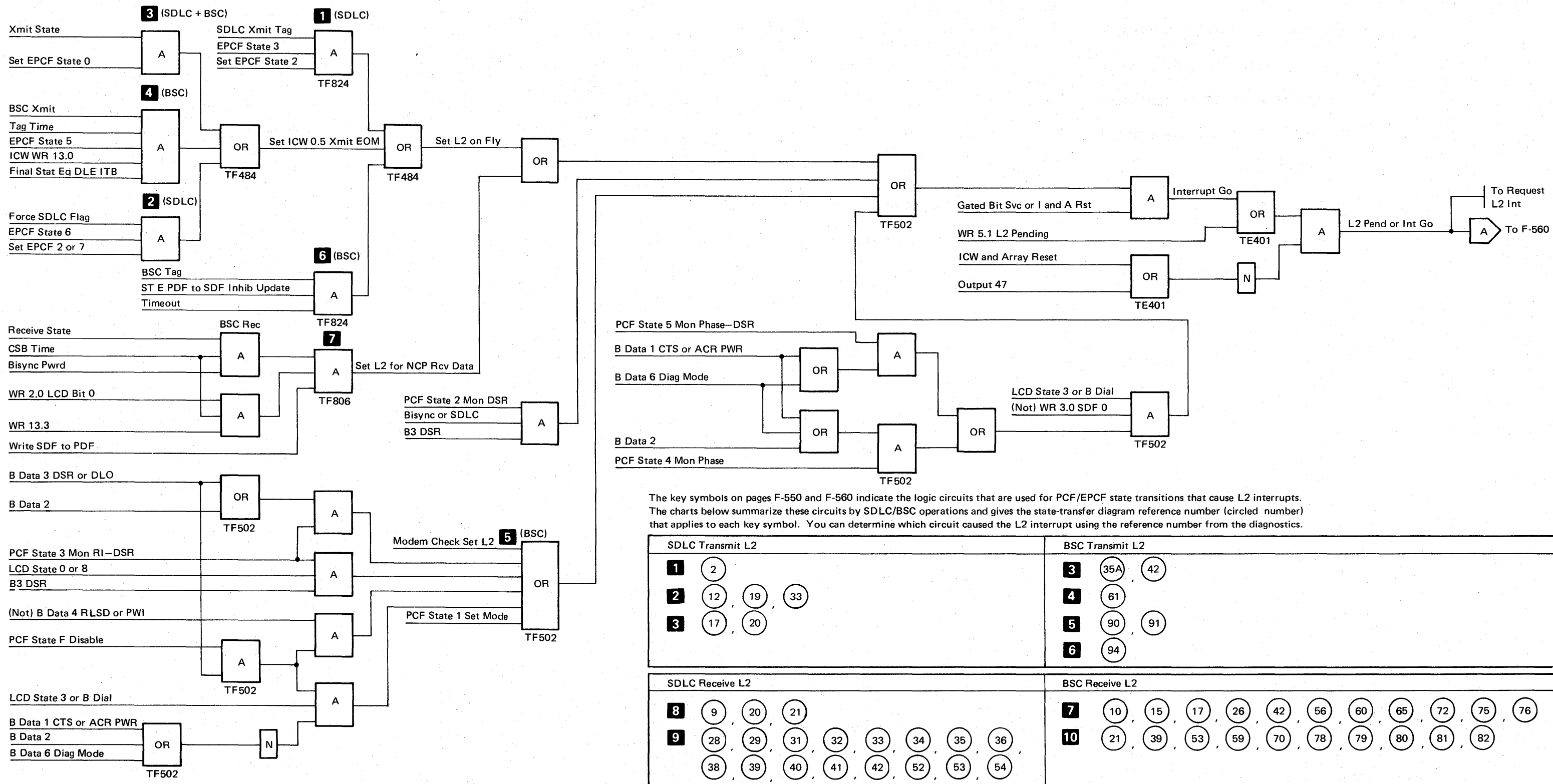
SCANNER INTERFACE TIMING TO LIBS



Note: For the 3705-11, every 2.0 microseconds if the cycle time is 1.0 microseconds and every 1.8 microseconds if the cycle time is 900 nanoseconds.

LEVEL 2 INTERRUPT

For use in determining the circuit that caused a level 2 interrupt when the state-transfer diagram reference number is known.

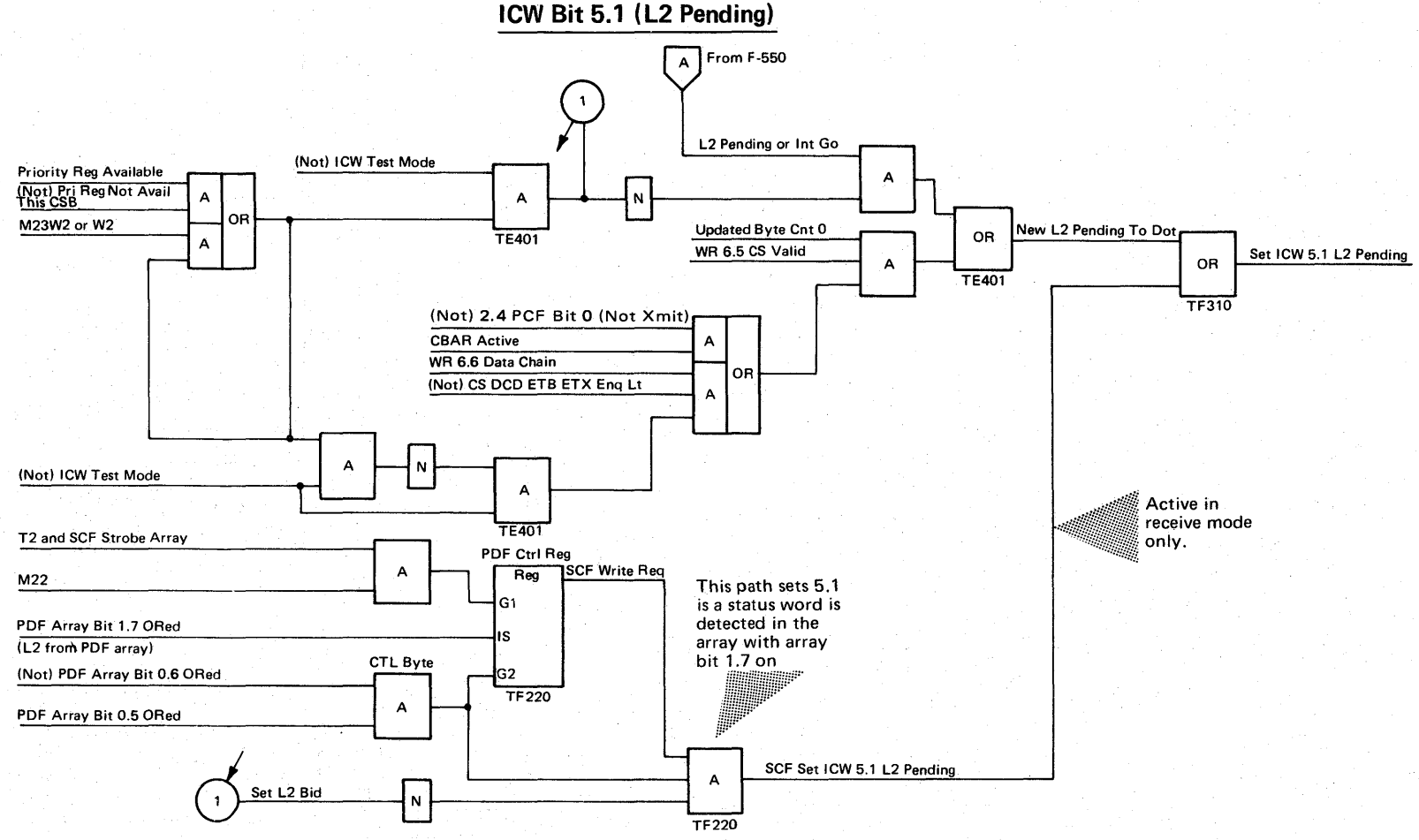


The key symbols on pages F-550 and F-560 indicate the logic circuits that are used for PCF/EPCF state transitions that cause L2 interrupts. The charts below summarize these circuits by SDLC/BSC operations and gives the state-transfer diagram reference number (circled number) that applies to each key symbol. You can determine which circuit caused the L2 interrupt using the reference number from the diagnostics.

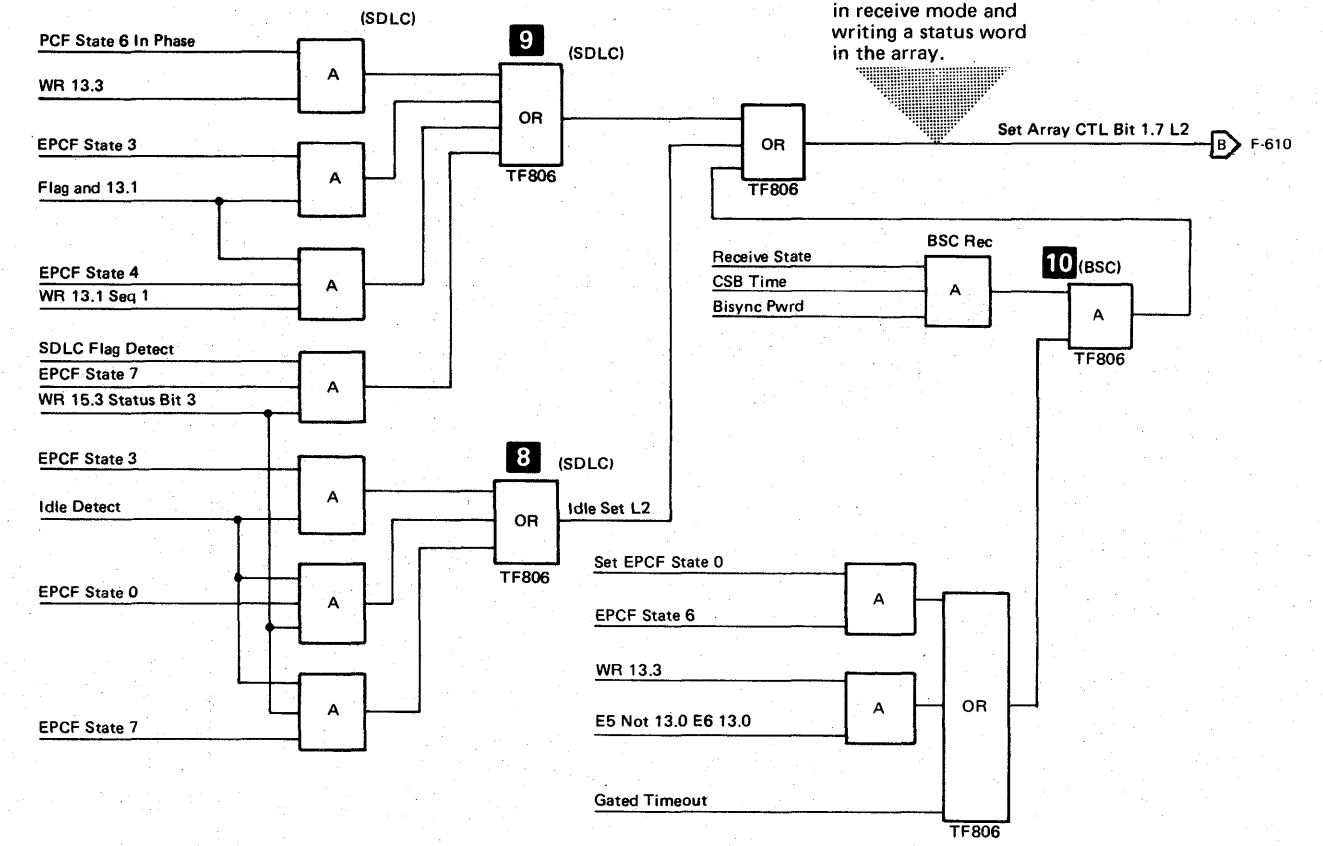
SDLC Transmit L2		BSC Transmit L2	
1	(2)	3	(35A), (42)
2	(12), (19), (33)	4	(61)
3	(17), (20)	5	(90), (91)
		6	(94)

SDLC Receive L2		BSC Receive L2	
8	(9), (20), (21)	7	(10), (15), (17), (26), (42), (56), (60), (65), (72), (75), (76)
9	(28), (29), (31), (32), (33), (34), (35), (36), (38), (39), (40), (41), (42), (52), (53), (54)	10	(21), (39), (53), (59), (70), (78), (79), (80), (81), (82)

LEVEL 2 INTERRUPT (PART 2)

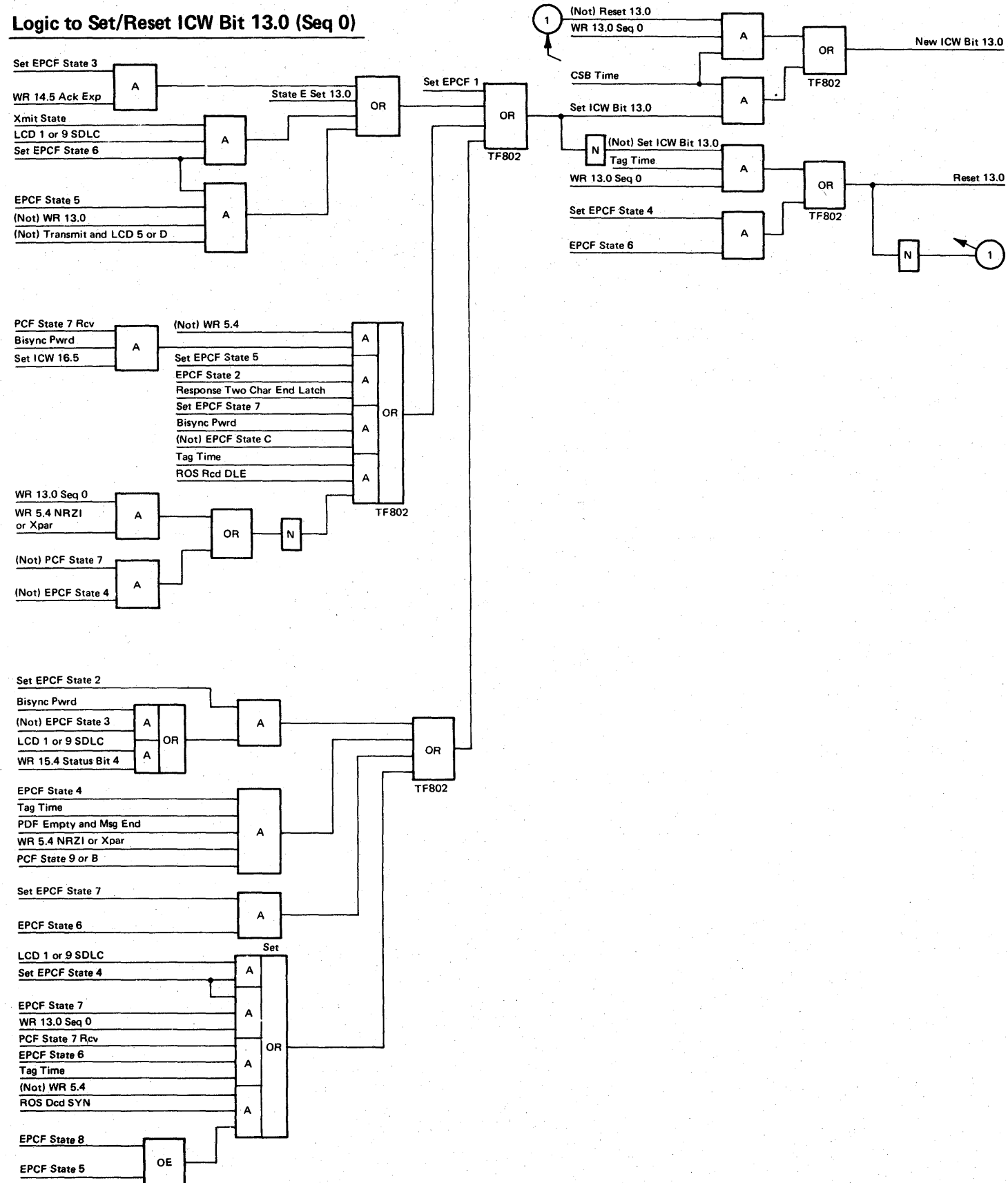


L2 Interrupt Set Into the PDF Array

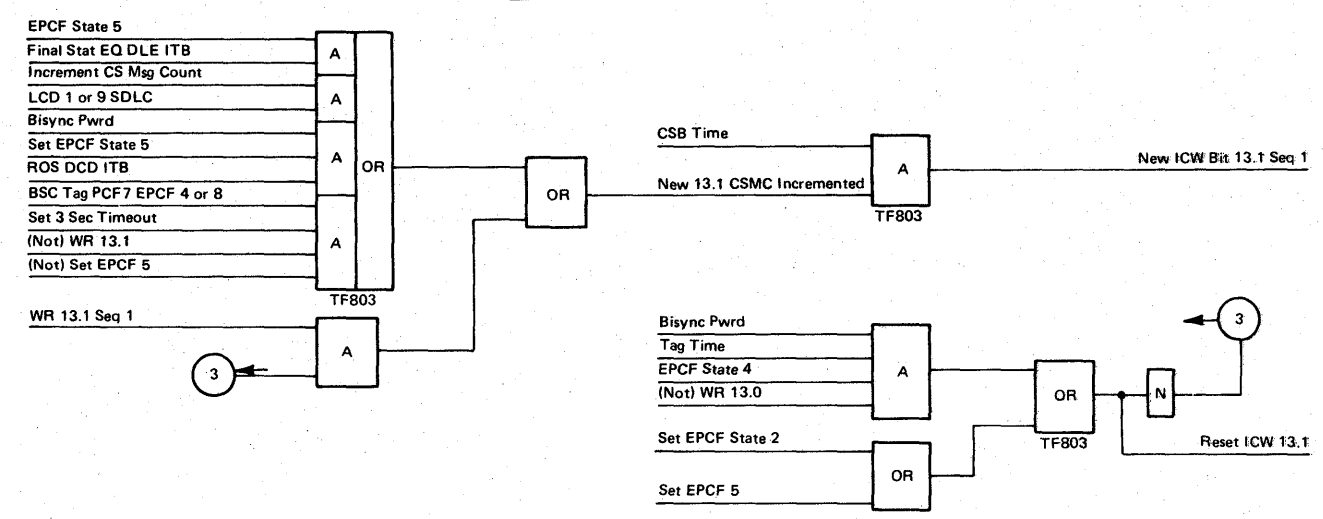


SET/RESET OF ICW BITS 13.0, 13.1, 13.6 AND 13.7

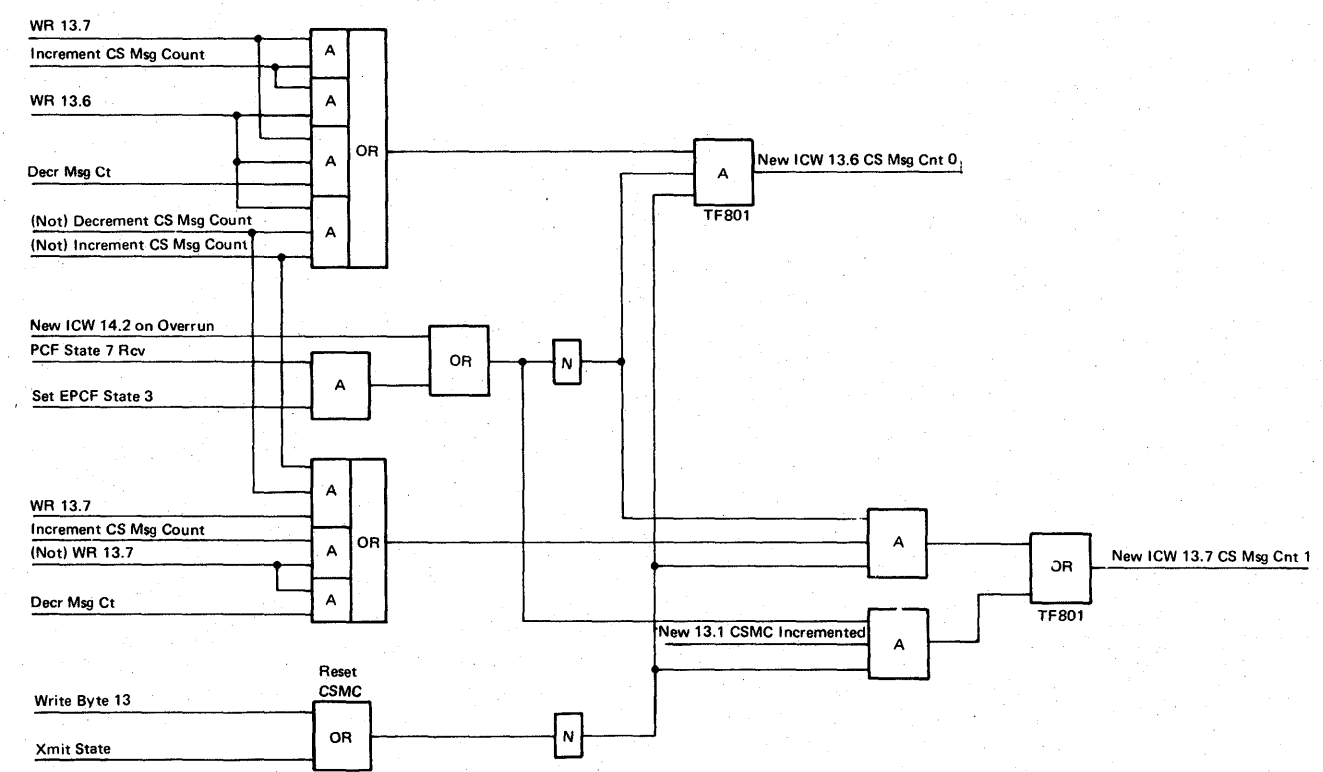
Logic to Set/Reset ICW Bit 13.0 (Seq 0)



Logic to Set/Reset ICW Bit 13.1 (Seq 1)

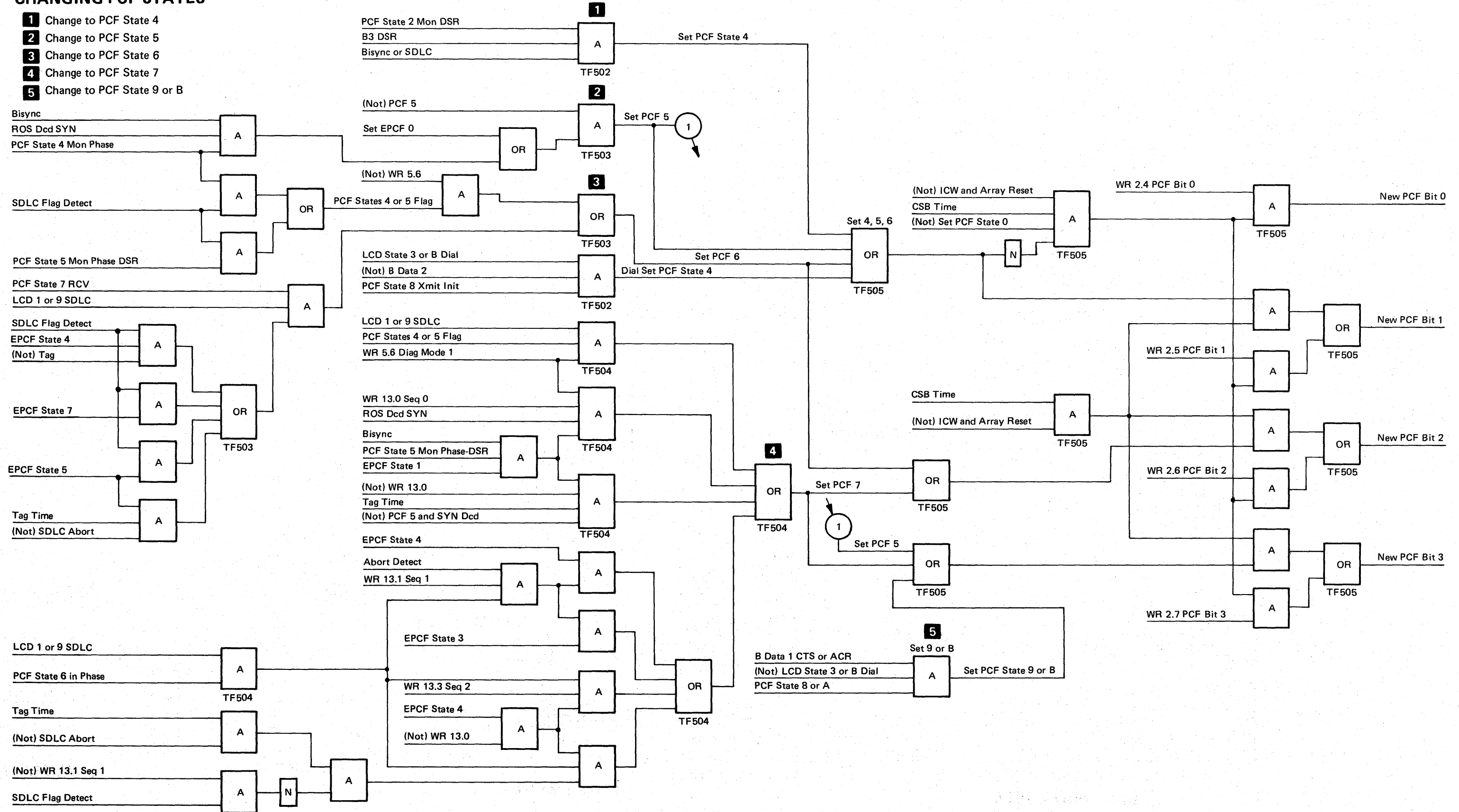


Logic to Set/Reset ICW Bits 13.6 and 13.7 (CS MESSAGE COUNT)



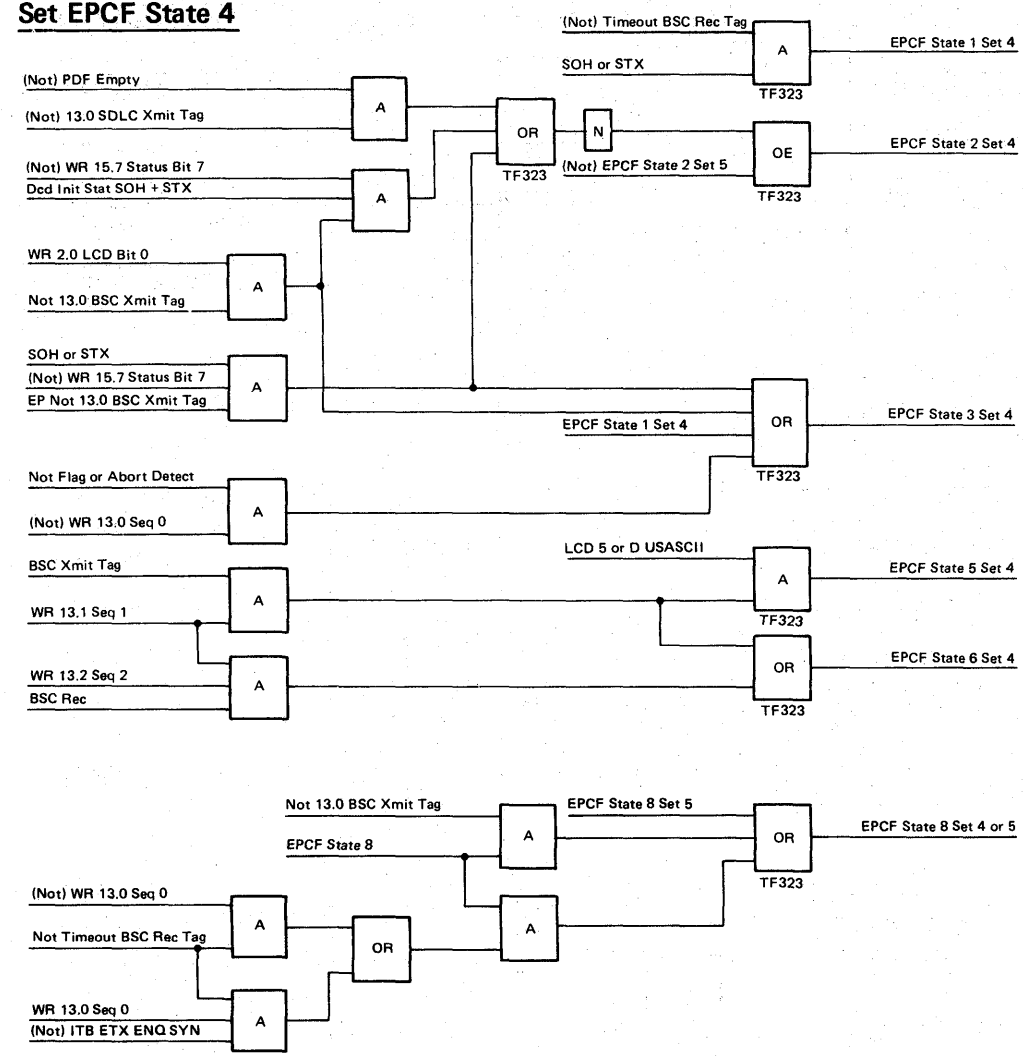
CHANGING PCF STATES

- 1** Change to PCF State 4
- 2** Change to PCF State 5
- 3** Change to PCF State 6
- 4** Change to PCF State 7
- 5** Change to PCF State 9 or B

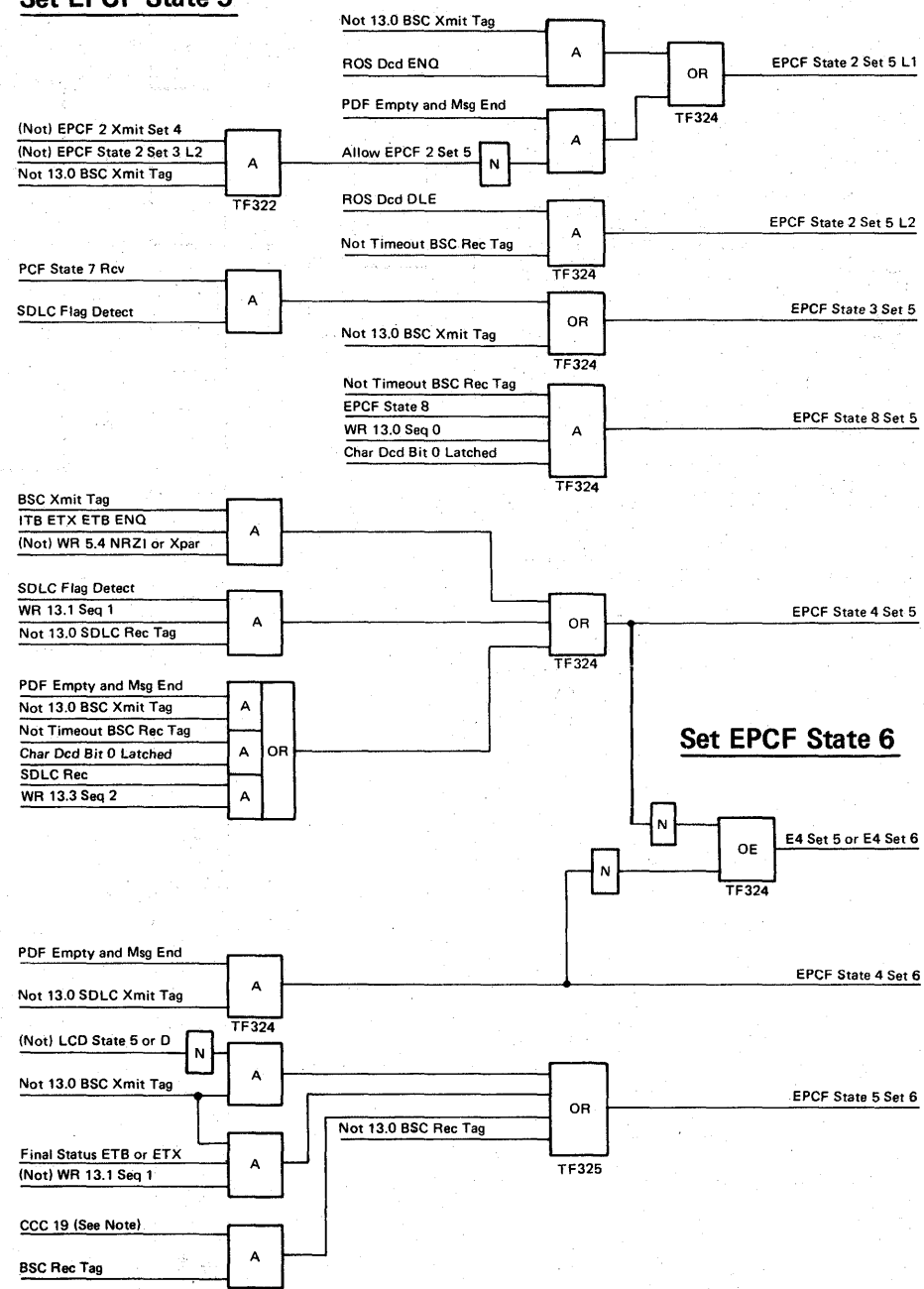


CHANGING EPCF STATES

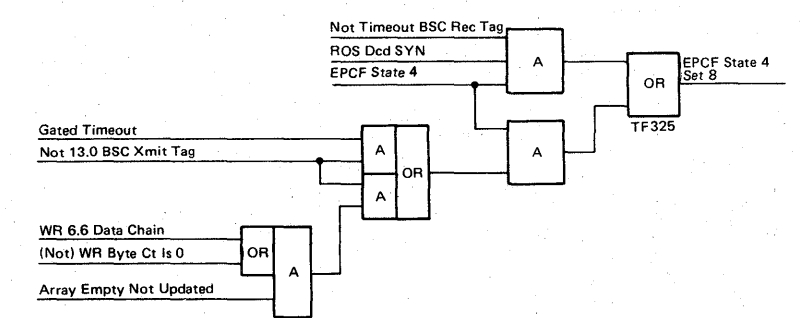
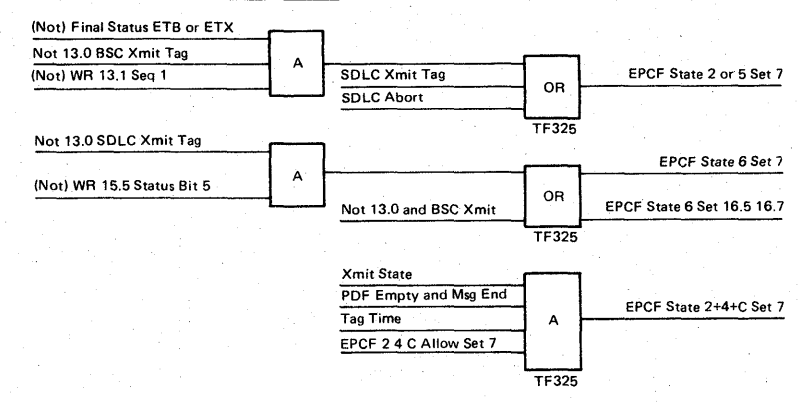
Set EPCF State 4



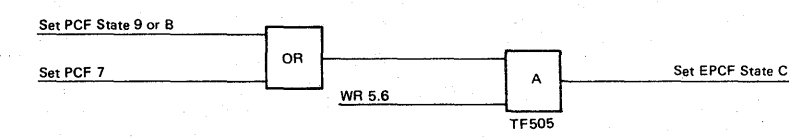
Set EPCF State 5



Set EPCF States 7 and 8



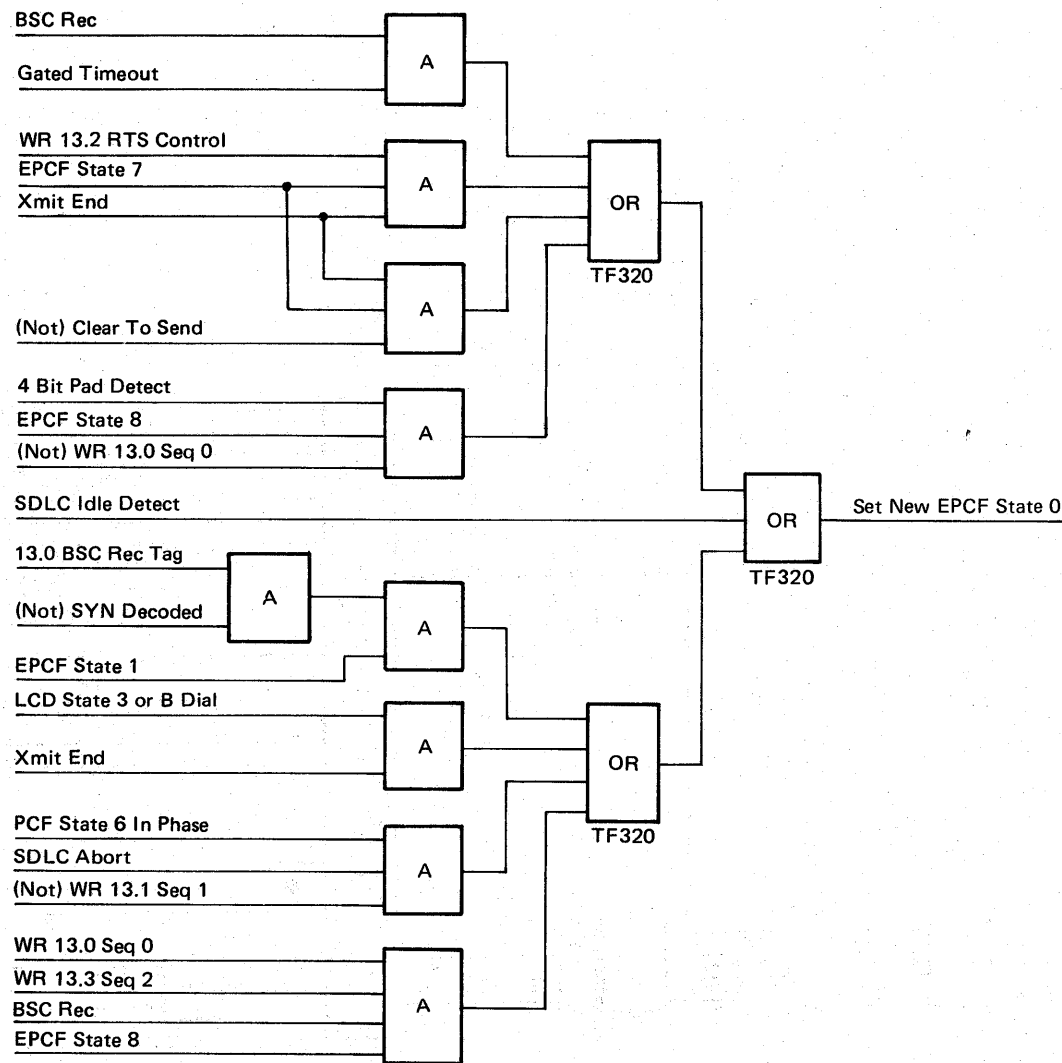
Set EPCF State C



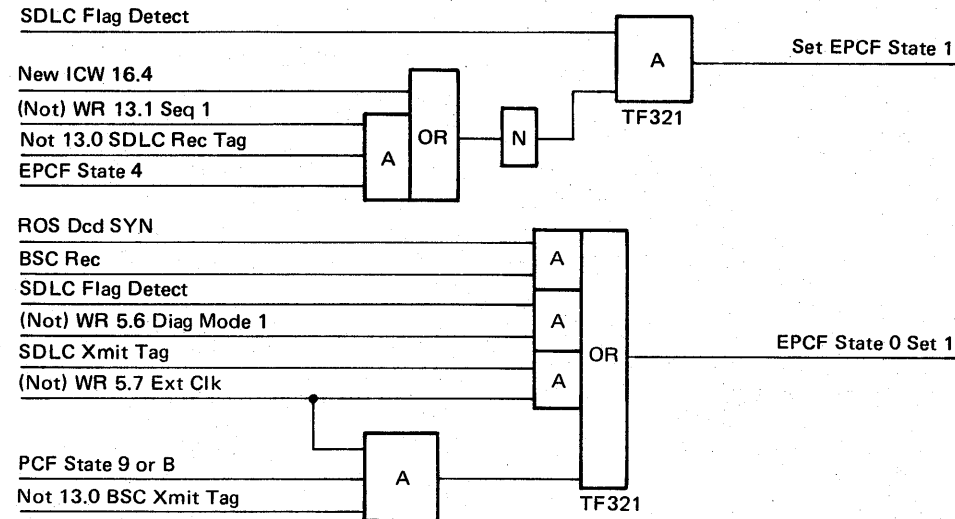
Note: CCC 19 is active for these characters:
ACK, WACK, RVI, NAK, STIK, DISC, ENQ
or EOT.

CHANGING EPCF STATES (PART 2)

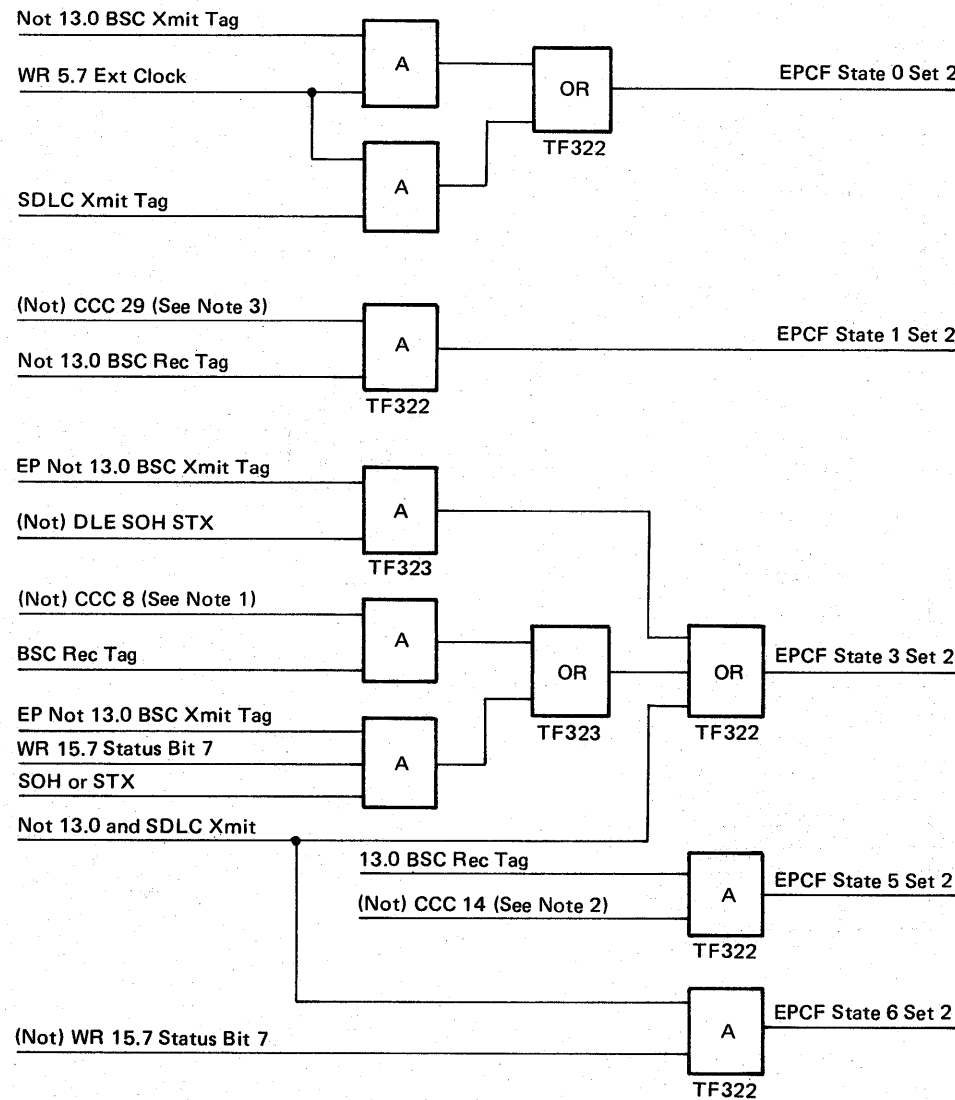
Set EPCF State 0



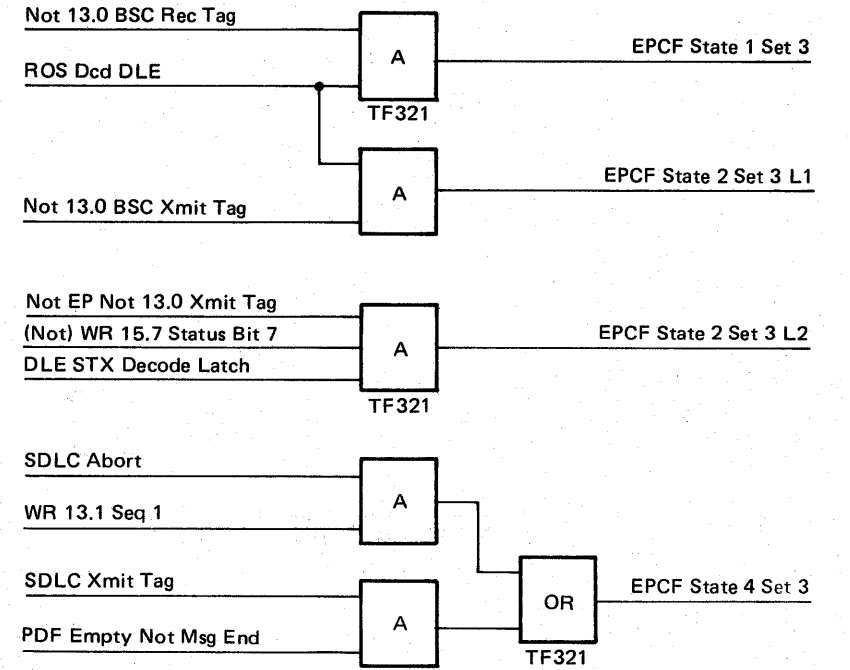
Set EPCF State 1



Set EPCF State 2



Set EPCF State 3

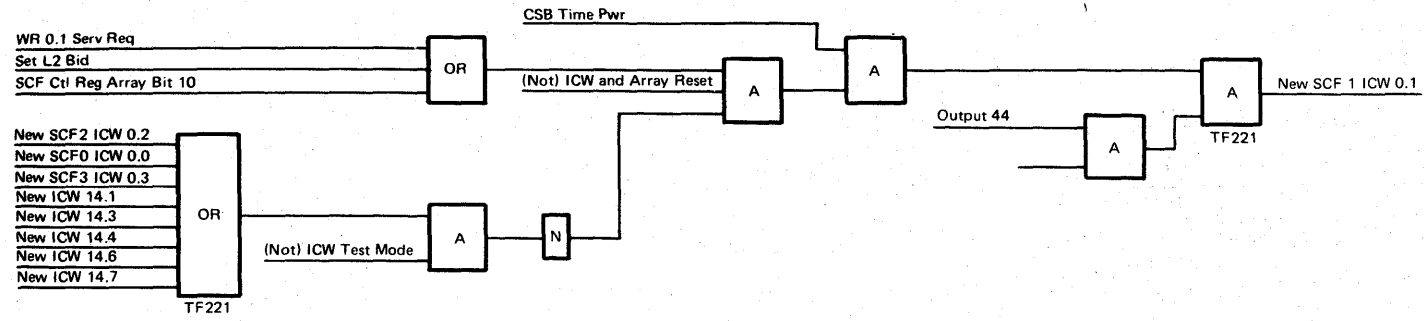


Notes:

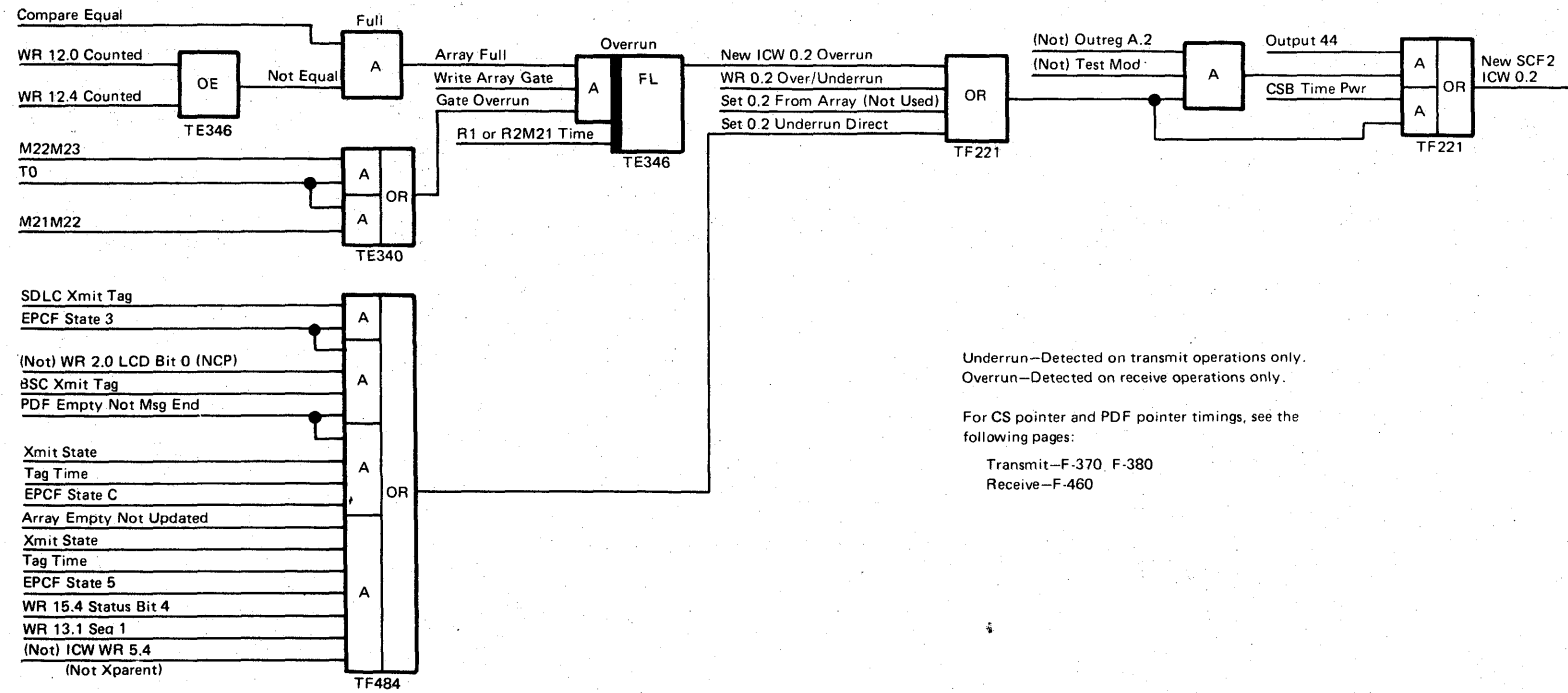
- 1. CCC 8—DLE, ACK, WACK, RVI, SOH, STX, NAK, STIK, DISC, ENQ, or EOT.
- 2. CCC 14—DLE, ACK, WACK, RVI, NAK, STIK, DISC, ENQ, or EOT.
- 3. CCC 29—ENQ, SYN, DLE, EOT, SOH, STX, or NAK.

SET OF ICW BITS 0.1-0.5 (SCF BITS 1-5)

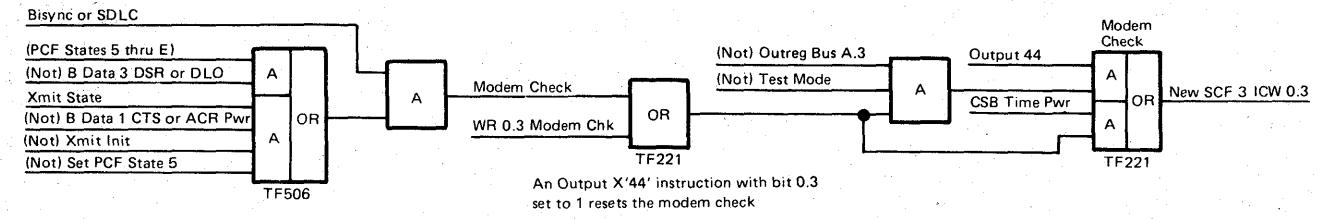
ICW Bit 0.1 (Service Request)



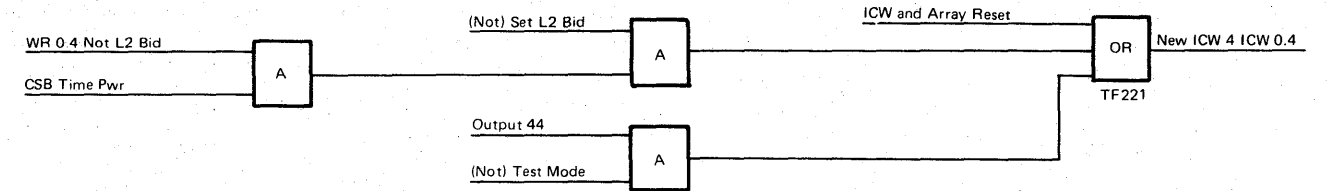
ICW Bit 0.2 (Overrun/Underrun)



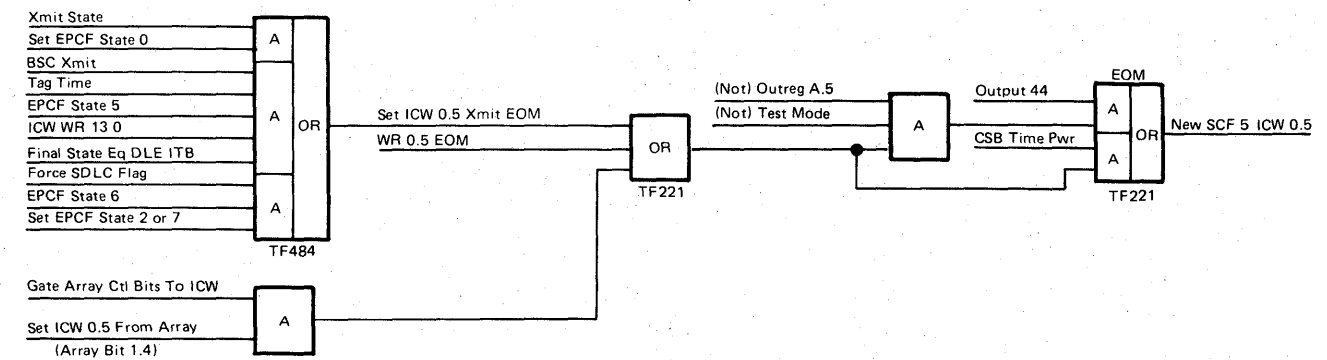
ICW Bit 0.3 (Modem Check)



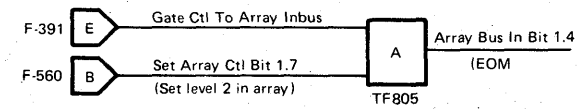
ICW Bit 0.4 (Not L2 Bid)



ICW Bit 0.5 (End of Message)



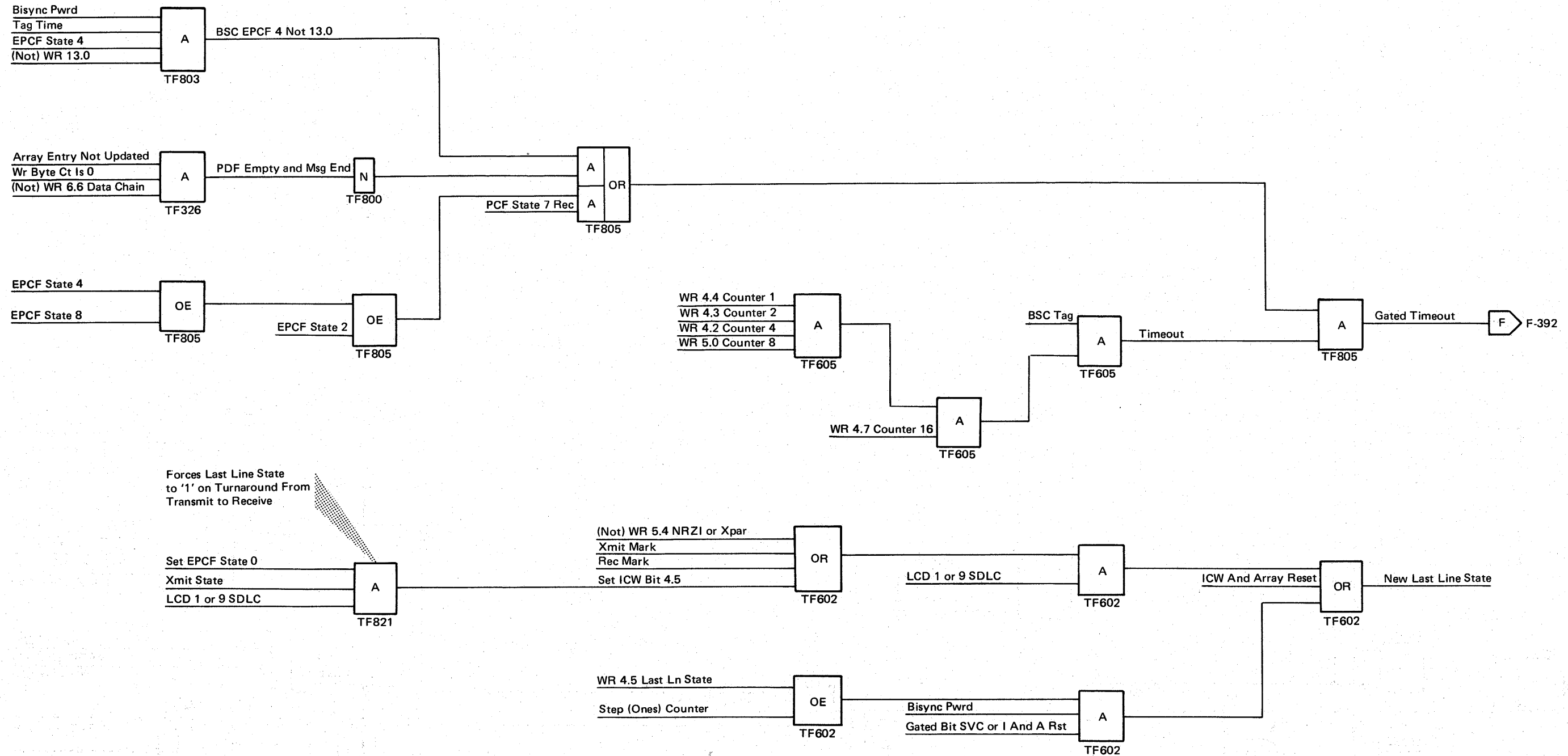
Setting EOM in the Array



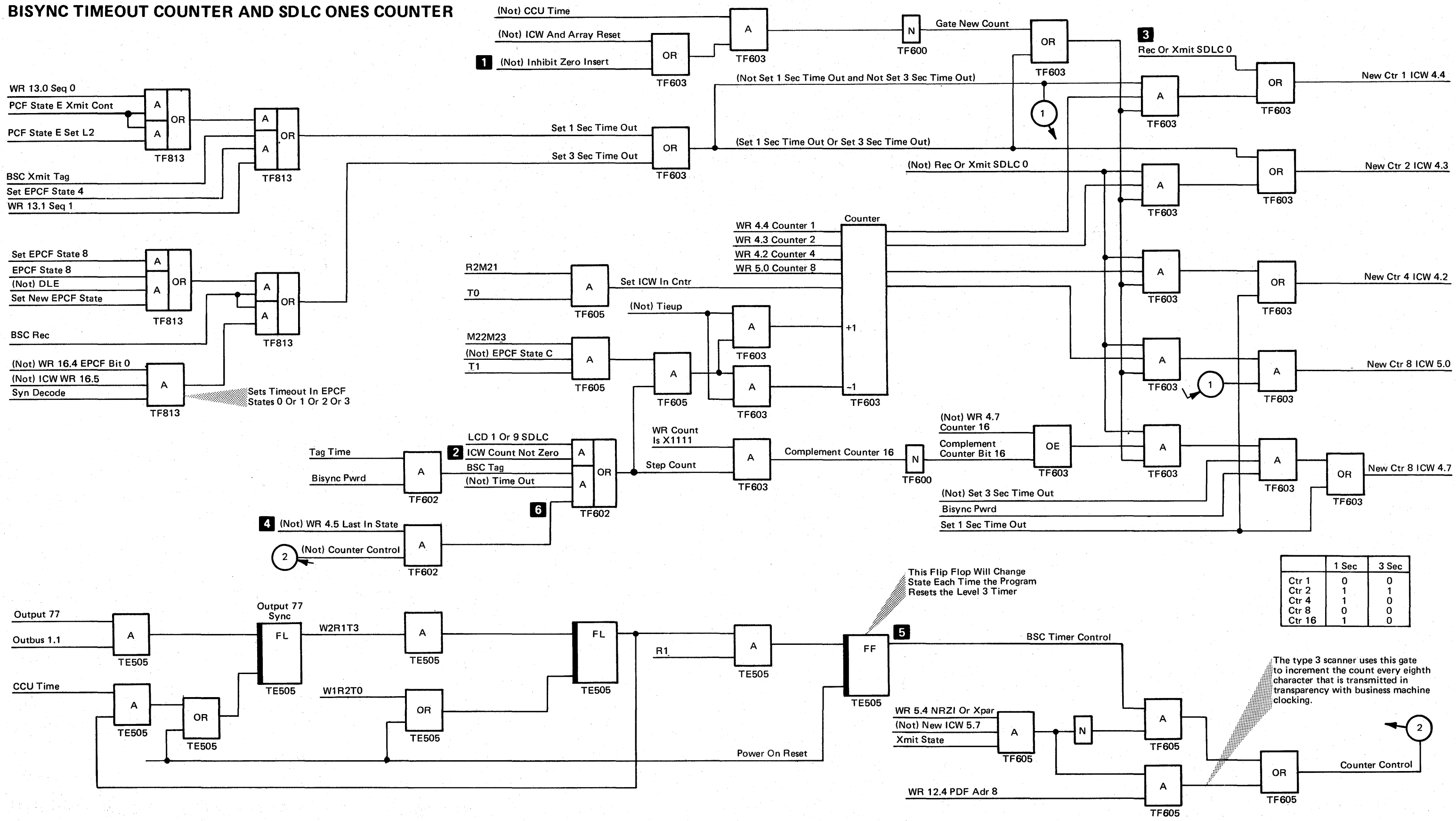
- The type 3 scanner writes the EOM into the array whenever L2 interrupt is written into the array (see F-560).
- The type 3 scanner writes the EOM into the array when in receive mode.

GENERATION OF LAST LINE STATE AND GATED TIMEOUT

(ICW BIT 4.5)



BISYNC TIMEOUT COUNTER AND SDLC ONES COUNTER



(Not) CCU Time
 (Not) ICW And Array Reset
 1 (Not) Inhibit Zero Insert

R2M21
 T0
 M22M23
 (Not) EPCF State C
 T1

LCD 1 Or 9 SDLC
 2 ICW Count Not Zero
 BSC Tag
 (Not) Time Out

4 (Not) WR 4.5 Last In State
 2 (Not) Counter Control

(Not) WR 4.7 Counter 16
 Complement Counter Bit 16
 (Not) Set 3 Sec Time Out
 Bisync Pwrld
 Set 1 Sec Time Out

This Flip Flop Will Change State Each Time the Program Resets the Level 3 Timer

	1 Sec	3 Sec
Ctr 1	0	0
Ctr 2	1	1
Ctr 4	1	0
Ctr 8	0	0
Ctr 16	1	0

The type 3 scanner uses this gate to increment the count every eighth character that is transmitted in transparency with business machine clocking.

BISYNC TIMEOUT COUNTER AND SDLC ONES COUNTER (PART 2)

SDLC Ones Counter

The SDLC ones counter is used to count received or transmitted one bits (marks). During a power-on reset or scanner disable **1**, the ones counter is forced to zero. The counter will remain at zero until a zero bit (space) is transmitted or received (count equals zero inhibits stepping the counter **2**). The first zero bit (space) received or transmitted forces counter bit 1 on **3**. The counter then increments once for each one bit (mark) transmitted or received. When a zero bit (space) is transmitted or received, the counter is reset to a count of one.

In transmit mode, if a character or character string containing five or more consecutive one bits (not a flag, abort or idle) is to be transmitted, a zero bit is inserted after the fifth one bit and the counter is reset to one.

In receive mode, if a character or character string containing five consecutive one bits followed by a zero bit is received, the zero bit is stripped from the accumulated SDF character and the counter is reset to a count of 1.

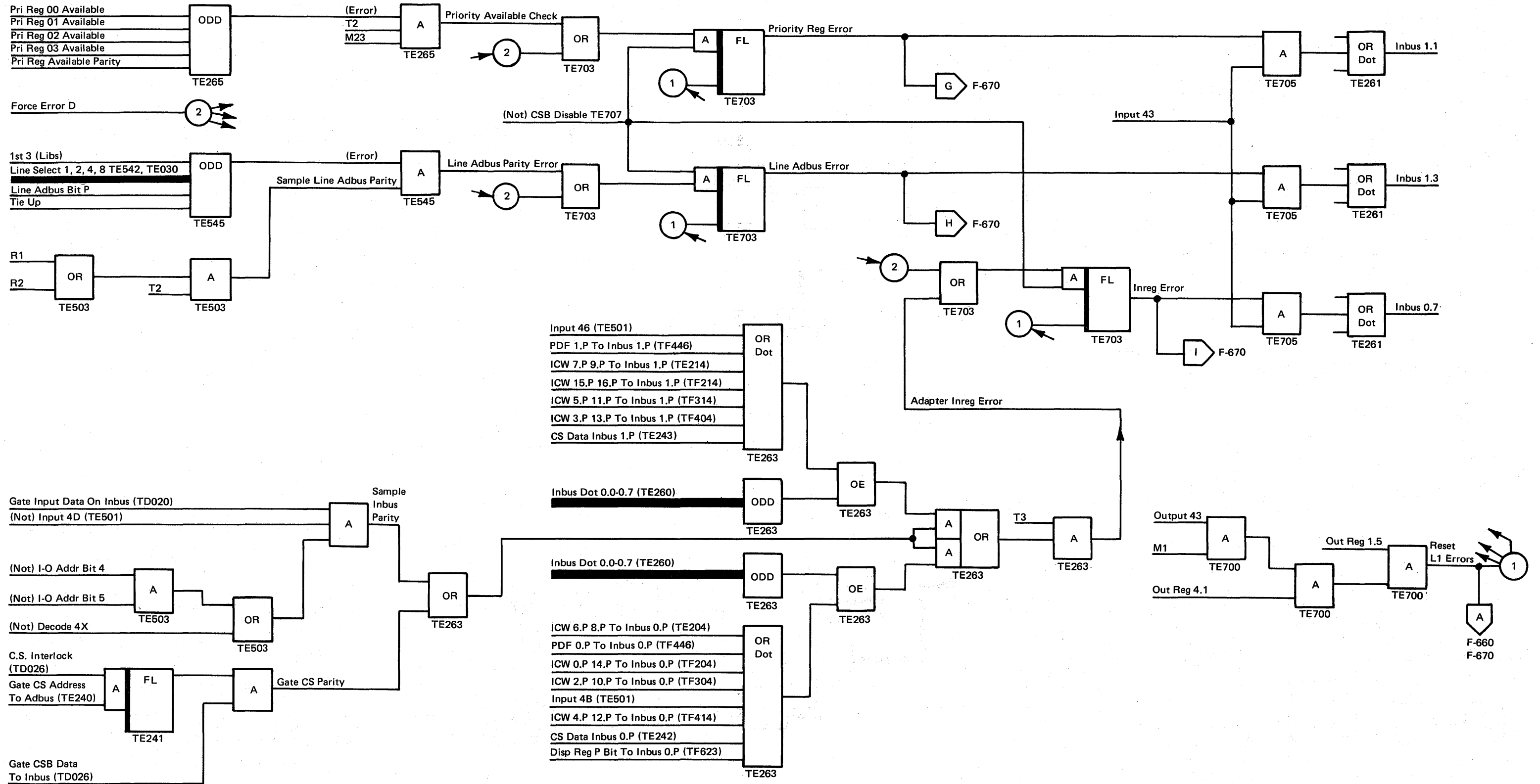
Bisync Timeout Counter

The bisync timeout counter, which is the same hardware as the SDLC ones counter, is used to generate a one-second timeout in transmit mode (for SYN insertion) and a three-second timeout in receive mode (SYN not received after establishing character phase or three seconds of continuous SYNs). The counter is reset to its initial count after receiving or transmitting a SYN, if not in EPCF state 8 (DLE SYN in transparent mode). The count is also initialized when leaving EPCF state 8.

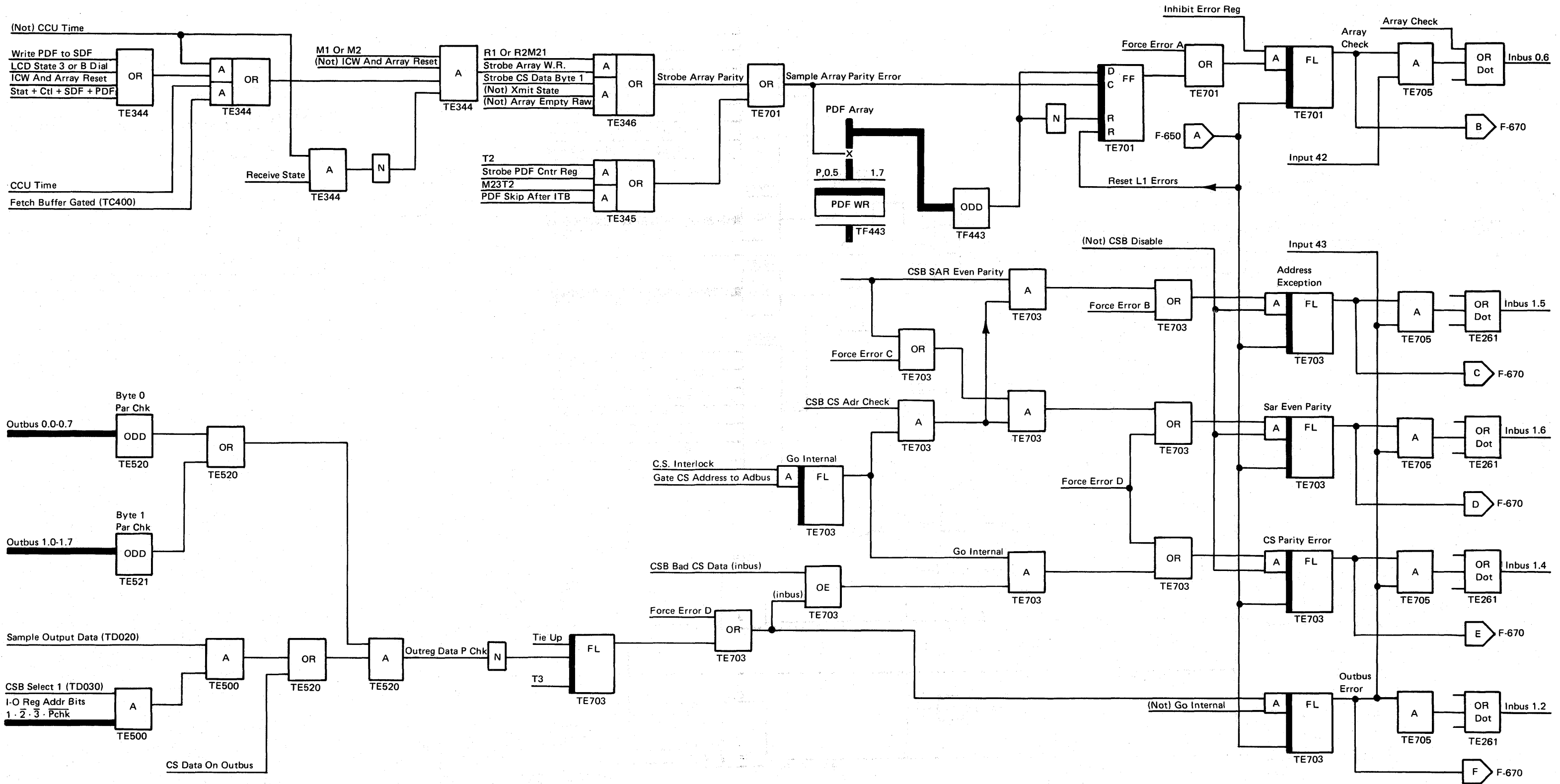
The counter is incremented **4** by the state of a 'reset level 3 interrupt timer' flip-flop and ICW work register 4.5 (last line state/bisync timer control). The level 3 flip-flop **5** is initially reset to zero and ICW work register 4.5 is set to one. Each time the program does an Output X'77' to reset the level 3 timer interrupt (approximately every 100 milliseconds), the flip-flop will change state. If the line is not in transparent transmit mode with internal clocking, the state of the flip-flop is compared with ICW work register 4.5. If the comparison is not equal at tag time, the counter is incremented **6** and the state of ICW work register 4.5 is complemented. The counter is incremented until the count is all ones (timeout). Any further change to the counter is inhibited until a set one-second or three-second timeout signal is generated.

If the bisync line is in transmit transparent mode and uses internal modem clocking, characters transmitted are counted to generate two SYN characters every 56 to 84 characters. The counter in this case is incremented each time ICW work register 12.4 (PDF address bit 8) changes state.

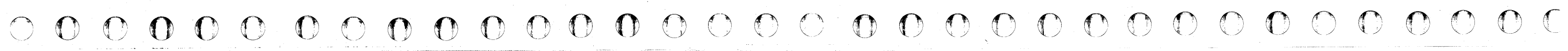
SCANNER LEVEL 1 INTERRUPTS



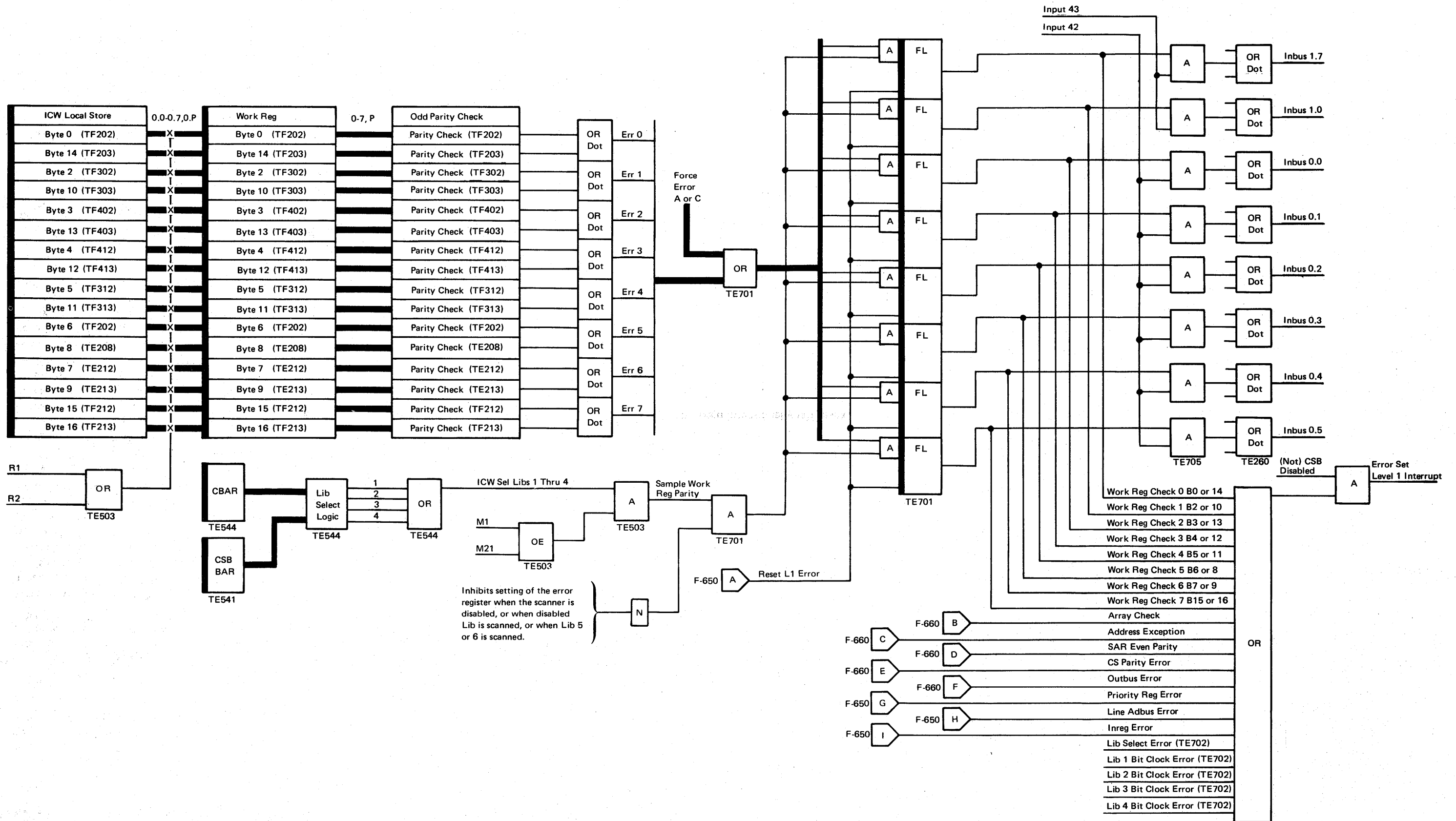
SCANNER LEVEL 1 INTERRUPTS (PART 2)



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SCANNER LEVEL 1 INTERRUPTS (PART 3)



COMMUNICATION SCANNER SERVICE AIDS

Sync Generation

To generate a sync for scoping type 3 communication scanner circuits, the following techniques and hints are provided:

- A line interface and its ICW and PDF are accessed by the scanner periodically to check for bit service requests.
- Most actions and changes in the ICW, PDF, and line interface registers occur at bit service scan time. The exceptions can occur at any scan time with an L2 bid or at cycle steal CCU time.
- Most IFT routines wrap data in scanner wrap mode or diagnostic wrap mode with the first line (840, 940, etc.) as the receive line and the second line (842, 942, etc.) as the transmit line. These addresses can be changed by selecting Routine X741 of the IFTs. See the *IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes D99-3705E* for the IFT X741 stop codes and the actions required to change the line addresses.
- The MST-1 latch card is used to AND conditions together for sync generation. The latch card will accept up to 5 inputs ANDed by using both circuits on the card in tandem. Connect pin M (output of upper latch) to pin D (input of lower latch) and connect sync points needed to AND inputs of upper and lower latches. All sync points in this service-aid are minus active. However, the latch card will accept plus inputs also (see 1-201). Wire pin M of the bottom latch to the external sync hub of the scope and sync plus. The latches are not used for scoping, just the ANDing circuits before the latches. Note that pins J, K, and L are not included in the summation to pin M.



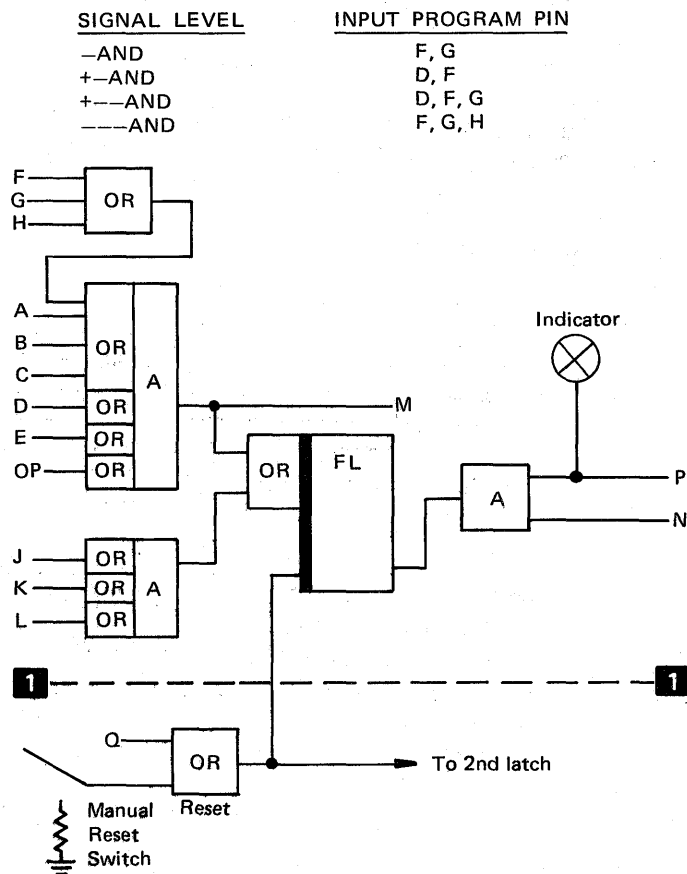
The indicator latch card must be plugged onto the MST-1 board with the component side of the card toward the right. If the card is plugged on upside down, or is plugged into the card side of the board, circuit damage will result.

- All IFTs that test the transmit and receive line control circuits and the data wrap functions (IFTs X741 and above) are structured around, and refer to, the state transfer diagrams (TD006 thru TD009). See pages F-400, F-430, F-470, and F-510 for details on these diagrams. These diagrams should be referred to on any IFT error stop where a state transition is checked or data and status is tested after the state transition.

- The IFTs provide an address useable with address compare sync to generate a sync close to the state transition under test.

MST-1 CE Indicator Latch Card

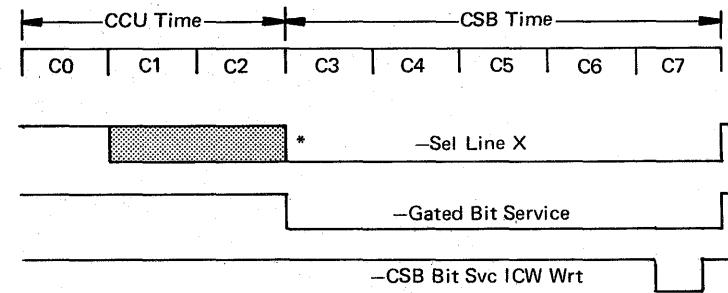
The minus active signal levels and input pins to be used for this service-aid are shown below. A complete list of all active signal levels and other information on the latch card can be found on 1-201.



Note: The CE Indicator Card contains two sets of circuitry as shown above line 1-1

1. Sync For Scoping ICW

To scope an ICW for a particular line, sync on 'sel line X' from the LIB (Vx 048) ANDed with CSB time. Scope the output of the work register for the bits needed.

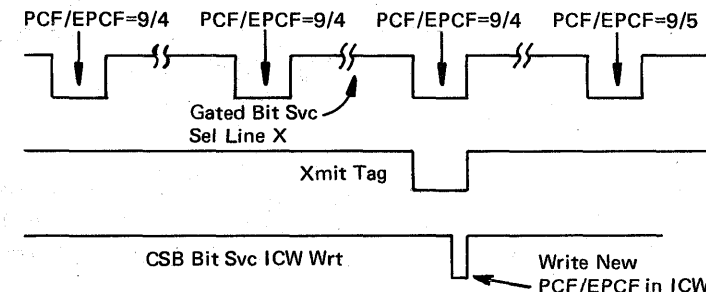


*SEL LINE will be active at C1-C2 if the CCU time is not used for Input/Output or Cycle Steal.

2. Sync For State Transition

To see a particular state transition, sync on 'sel line X' from the LIB (Vx 048) ANDed with 'PCF state X' 'EPCF state X' 'tag time,' and 'gated bit svc'. The address of the line under test can be determined from the IFT stop information or from the user.

Example 1: To see state transition 18 on page F-400, sync on 'sel line X' (Vx 048) ANDed with 'PCF state 9' (TF505), 'EPCF state 4' (TF825), and 'tag time' (TF422). The PDF conditions could be scoped with the conditions to set the new PDF/EPCF of 9/5 (TF324). The new PCF/EPCF state can only be seen as new ICW bits to be written back to ICW local store at CSB bit service write time during this tag bit service. At the next CSB scan of the line address, the decode of the new PCF/EPCF can be checked.



Example of State Transition 18

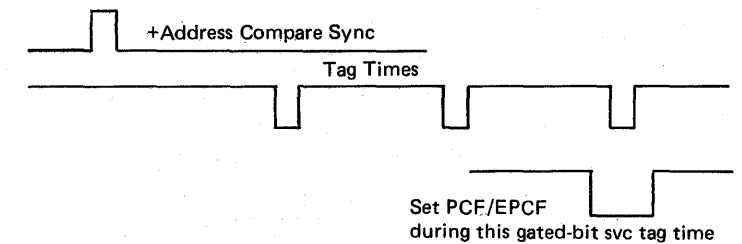
3. Sync For State Transition Using IFT Generated Sync

This technique provides a more reliable sync for IFT error loops. See section 3.3 of the *IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes D99-3705E*.

The diagnostic routines that check for state transitions use a common subroutine to wait for the state transition under test. At the branch to the subroutine, the diagnostic loads register X'18' with the address of a data area that contains the number of character times the subroutine waits for the expected PCF/EPCF change. This character count is prior to the branch and link instruction that branches to the wait subroutine. When an error stop occurs on a type 3 communication scanner IFT that checks a PCF/EPCF state change, display register X'18' and note the address displayed. Display storage using the address from register X'18'. The data in the storage location will be the number of characters the subroutine will wait for the state change. Restart the IFT with the "Loop on First Error" and "Bypass Error Stop" sense switches set. Dial the address from register X'18' into the STORAGE ADDRESS/REGISTER DATA switches BCDE (1-100) and sync the scope externally on 'address compare sync point', 01A-B3 P2S09 (see 1-200). Display on the scope 'BSC or SDLC transmit tag' or 'receive state' ANDed with 'tag time'. Tag time alone occurs for both transmit and receive lines depending on whether the line under test is in transmit or receive state. Delay to the tag is specified by the count in register X'18'. This is the tag time when the state transition should occur. Refer to the particular state transfer referenced by the IFT error stop to see the conditions that should produce the state change. Using the second level diagrams for setting new PCF and EPCF states (F-590 thru F-600), scope to find the error. The IFTs also check for the new character set in the SDF and in some cases the status bits in the ICW after the state change. The same scoping technique as above will apply for these failure stops.

Address Compare Sync from IFT.

Example 2: Assume the IFT routine waits 3 character times before expecting a state change under test. Delay sync to the 3rd tag time to see new ICW bits being stored for new PCF/EPCF.



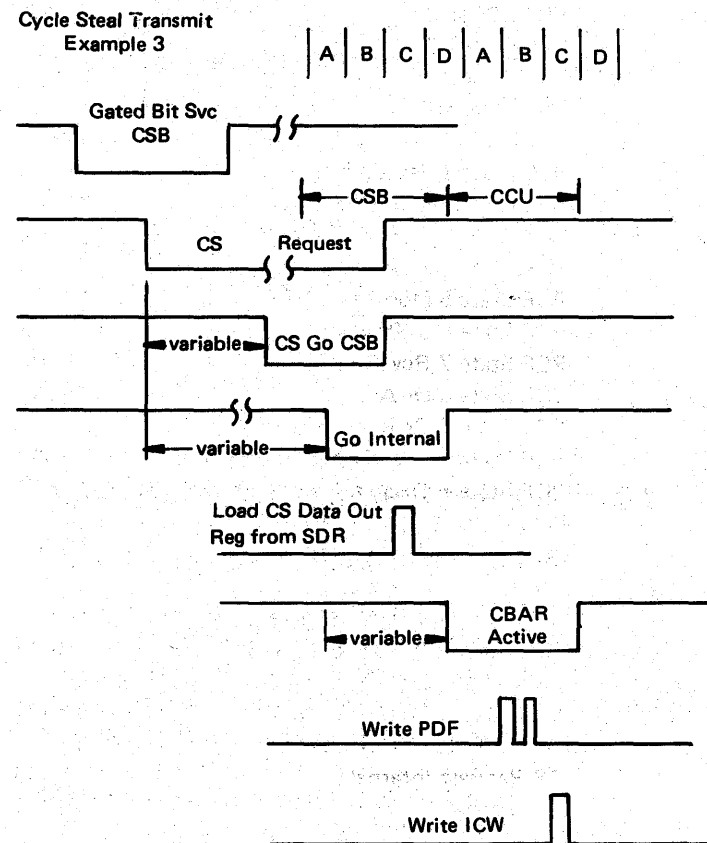
The address and data from register X'18' display is valid only when the error stop occurs while waiting for a state transition or while checking conditions after a state transition. If a level 1 error occurs, the data in the register X'18' will not be useable.

COMMUNICATION SCANNER SERVICE AIDS (PART 2)

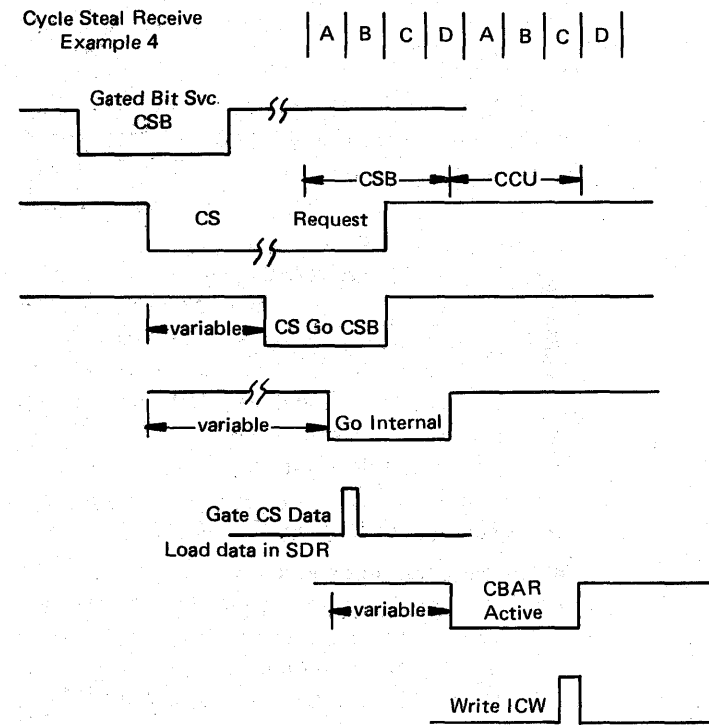
4. Sync For Cycle Steal (See F-450 and F-460)

Generating a sync to scope cycle steal circuits is complicated by the asynchronous timings of a cycle steal operation. A beginning sync is 'cycle steal request latch' ANDed with 'gated bit service' and 'sel line X'. If there is no interference from cycle steal priority of other scanner or instruction cycles, then the 'go internal' latch will be set during the next CSB time. During this CSB time, the actual cycle steal to storage occurs. If there is a delay because of priority, then the cycle steal will occur during a later CSB time. During the following CCU time, if no output instruction is being executed, 'CBAR active' latch is set and data or cycle steal count and cycle steal address are updated in the ICW. The key latches are 'cycle steal request', 'go internal', and 'CBAR active'.

For a cycle steal transmit operation, sync on 'gated bit svc' (TF625) ANDed with 'CS request latch' (TE240), and 'sel line X' (Vx048). Connect 'go internal' (TE241) to sync delay and scope the data as it transfers from storage to the cycle-steal data-out register, connect 'CBAR active' (TE544) to sync delay and scope the data into the PDF array, the CSAR update, and the new cycle steal byte count. See example 3.



For a cycle steal receive operation, sync on 'gated bit svc' (TF625) ANDed with 'CS request latch' (TE240) and 'sel line X' (Vx048). Connect 'go internal' (TE241) to sync delay and scope the data to storage. Connect 'CBAR active' (TE544) to sync delay and scope the CSAR update and the new cycle-steal byte count. See example 4.



5. ICW Bit Errors

Scoping the picking or dropping of a bit in the ICW can be simplified by setting the machine in a continuous panel register display or store operation (see 1-200). Sync the scope on register-in or register-out decodes and check the input and output of the ICW work register and the ICW. Assume a bit pick problem with ICW byte 2. Set up the control panel for an Output X'45' with zeros as data and jumper the continuous store pin (01A-B3P2J06) to ground. Sync the scope on Output X'45' (0XA-E3S2P13). TE502 and observe the outreg bus bits and the new ICW bits as input to the ICW during CCU Time (TF300).

To check the data path from the ICW work register to the In register, execute a control panel Output X'40' with the line under test as data (fetch buffer). Set up a continuous input and scope In register inputs with the input 'X' decode as a sync.

6. IFT Hints

- The following general registers have assigned uses in the IFTs as follows:
 - Reg '11' Line under test
 - Reg '14' Address of the line generating L2 interrupts
 - Reg '15' Bits in error
 - Reg '18' Special use for sync generation
- Check the heading of the routine where an error stop occurs for sequences and data used in the test. Check the entire routine error stops for help in understanding the error.
- The IFTs use common subroutines to set mode, wait for a state change, and test for wrap data.
- The IFTs test the beginning state transfers before using them to build toward later state transfers.
- All routines that test for state transfers (X740 thru X79A) operate in scanner wrap mode (Diag 0, bit 5.5 on). Wrap routines X7A0 thru X7A6 operate in diagnostic wrap (wrap in the line set). Wrap routine X7A8 is a manual intervention routine that allows the selection of transmit and receive lines and the mode of wrap. This routine may be run in scanner wrap mode and then in line-set wrap mode to isolate a trouble to the LIB cables and bit-clock circuits. The scanner wrap mode does not depend on any LIB circuits being active but the line set wrap does. See the second level diagram of scanner wrap (F-700).
- The basic transmit and receive functions are tested in scanner wrap mode before cycle steal mode is tested. Basic cycle steal circuits are tested before the transmit functions with cycle steal are tested. Receive functions with cycle steal are tested last along with LRC and CRC accumulation functions.
- All ICW positions are tested in ICW test mode for set and reset functions. ICW test mode causes the ICW array to be used as a storage unit. All changes to the ICW array by the scanner control logic are inhibited in ICW test mode.
- Scanner problems that result in a level 1 error only when running IFTs can be run with level 1 errors masked off to force an error stop in the IFTs so the routine may be looped for scoping. With level 1 errors masked off, set the "loop on error" option and scope the problem using previous techniques. The IFT error stop may occur later than when the level 1 error would occur and this fact must be considered when analyzing the failure. The level 1 errors are masked off as follows:

Return the program to the DCM halt 80FX, (FFFF in the STORAGE ADDRESS/REGISTER DATA switches BCDE, function 6, and interrupt or start). Manually store FFFF in storage location 0730. Restart the IFTs with all routines requested for the scanner under test. An error stop should occur in routine X717 indicating that a level 1 interrupt did not occur when expected. Bypass this error and con-

tinue until an error occurs in the IFT. Analyze the stop using the *IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes D99-3705E* and display the error by looping and scoping using the techniques listed in this service aid or other applicable procedures. The level 1 interrupts will remain masked off until storage location 0730 is cleared manually or the IFTs are completely re-loaded (load key depressed). When the IFT error stop is eliminated, reset the storage flag at 0730 and rerun all the IFTs to prove correction of level 1 errors. If the IFTs do not fail with level 1 errors masked off, the problem could be a parity bit pick or drop problem or a false level 1 error.

Type 3 Communication Scanner Scope Points

-CSB Time	TE404	E3L2D02
-CCU Time	TE404	E3L2B05
-Gated Bit Svc	TF625	E2D2U03
-Bisync Pwrd	TF501	E2J2M09
-CSB Bit Svc ICW Wrt Time	TE400	E3L2P02
-SDLC Xmt Tag	TF827	E2P2P05
-BSC Xmt Tag	TF827	E2P2U07
-EPCF State 0	TF804	E2E2S08
-EPCF State 1	TF804	E2E2S02
-EPCF State 2	TF804	E2E2G13
-EPCF State 3	TF804	E2E2U10
-EPCF State 4	TF825	E2P2B12
-EPCF State 5	TF804	E2E2G07
-EPCF State 6	TF804	E2E2G10
-EPCF State 8	TF816	E2B2U02
-Xmt State	TF505	E2J2J04
-Receive State	TF505	E2J2J05
-Tag Time	TF422	E2H2J06
-PCF State 1 Set Mode	TF505	E2J2G05
-PCF State 2 Mon DSR	TF505	E2J2P10
-PCF State 3 Mon RI DSR	TF505	E2J2M12
-PCF State 4 Mon Phase	TF505	E2J2U12
-PCF State 5 Mon Phase DSR	TF505	E2J2G08
-PCF State 6 In Phase	TF505	E2J2D11
-PCF State 7 Rcv	TF505	E2J2P06
-PCF State 8 Or A	TF505	E2J2U04
-PCF State 9 Or B	TF505	E2J2U13
-PCF State E Xmt Cont	TF505	E2J2S03
-PCF State F Disable	TF505	E2J2D07
-Sel Line 0 (Type 1 LIB)	Vx-048	X1F2B11
-Sel Line 1 (Type 1 LIB)	Vx-048	X1F2D11
+Addr Compare Test Pin		
(Sync from panel switches)	CU004	01A-B3P2S09
CSB Timings (CSB Time, CCU Time	TE404	
RI, W2, etc)	TE405	
Input Gating (Input 41, etc)	TE501	
Output Gating (Output 41, etc)	TE502	
-CS Request Internal	TE240	E3K2U04
-Go Internal	TE241	E3K2G10
-CBAR Active	TE544	E3H2S13

SCANNER WRAP MODE

DIAGNOSTIC MODE 0 (ICW BIT 5.5)

Scanner Wrap

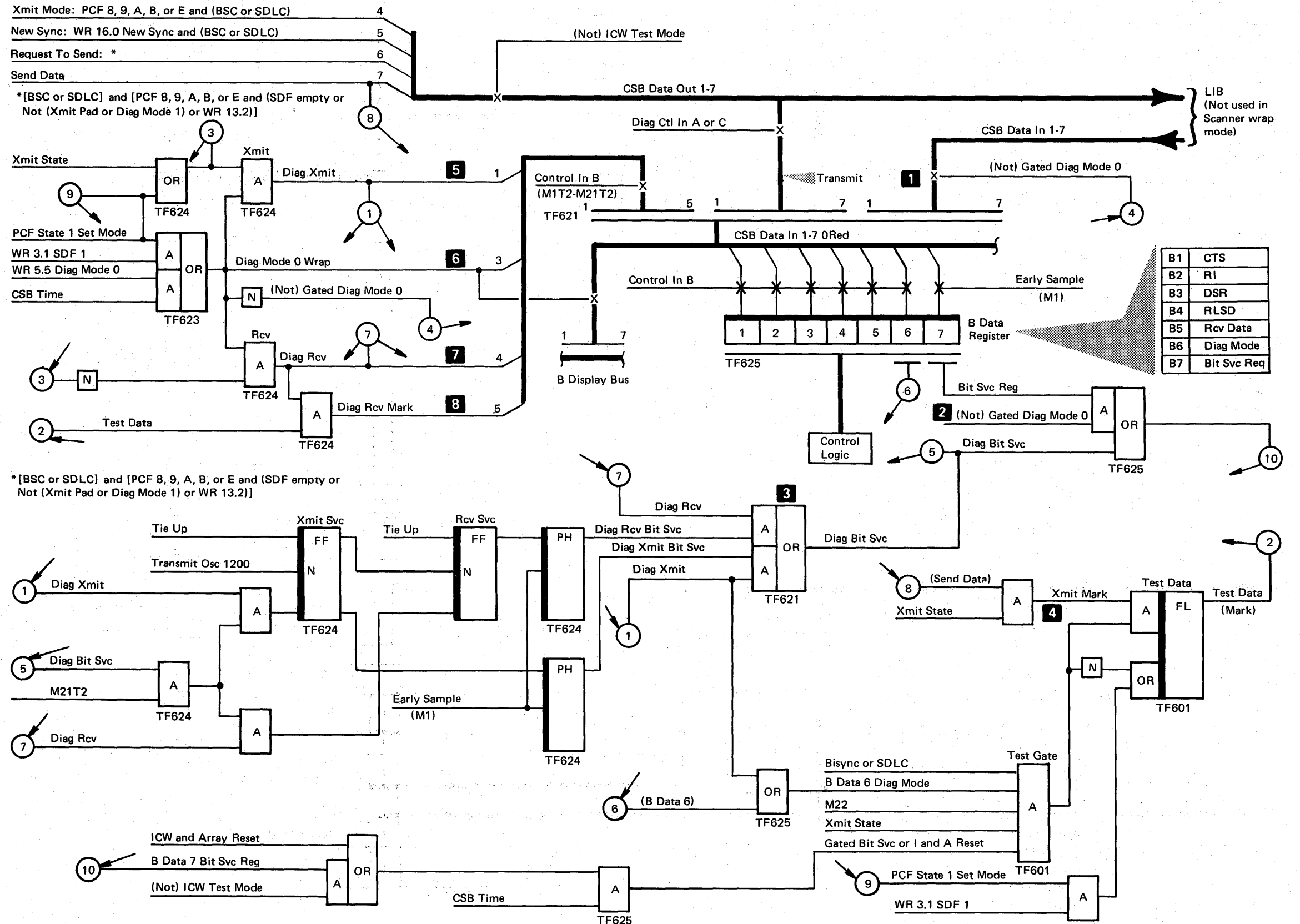
The scanner wrap mode provides an internal-scanner line-wrap capability. This mode allows the control program to test most of the scanner registers, scanner data flow, scanner control logic, and the 'CSB data out' lines without using LIB hardware.

Setup

1. Select one line interface to act as a transmit line and one other line interface on the same scanner to act as a receive line.
2. The control program executes an Output X'40' instruction to load ABAR with the receive interface address.
3. The control program executes an Output X'46' instruction with bit 0.1 on to set ICW bit 3.1 (SDF 1) and other bits according to NRZI and Diag 1.
4. The control program executes an Output X'45' instruction to set the PDF to X'1' (set mode) that sets ICW bit 5.5 (diagnostic mode 0) for the receive line.
5. Repeat steps 2 thru 4 using the transmit interface address.
6. After the receive and transmit lines have been put into "scanner wrap mode", the control program may simulate all normal line functions.

Operation

1. Since 'gated diag mode 0' inhibits the 'CSB data in 1-7' lines **1** and 'bit svc req' **2**, the scanner uses the 1200 bps oscillator to generate a 'diag bit svc' **3** for both the receive and transmit lines.
2. When the transmit address is being scanned:
 - 'Send data' bits are buffered in the scanner 'test data' latch under control of 'diag bit svc' **4**.
 - 'Diag Xmit' **5** is set in B data register 1 to simulate CTS to the control logic.
 - 'Diag mode 0 wrap' **6** is set in B data register 3 to simulate DSR to the control logic.
3. When the receive address is being scanned:
 - 'Diag rcv' **7** is set in B data register 4 to simulate RLSO to the control logic.
 - 'Diag rcv mark' **8** (from the 'test data' latch) is set in B data register 5 to simulate the receive data bit to the control logic.



DIAGNOSTIC WRAP

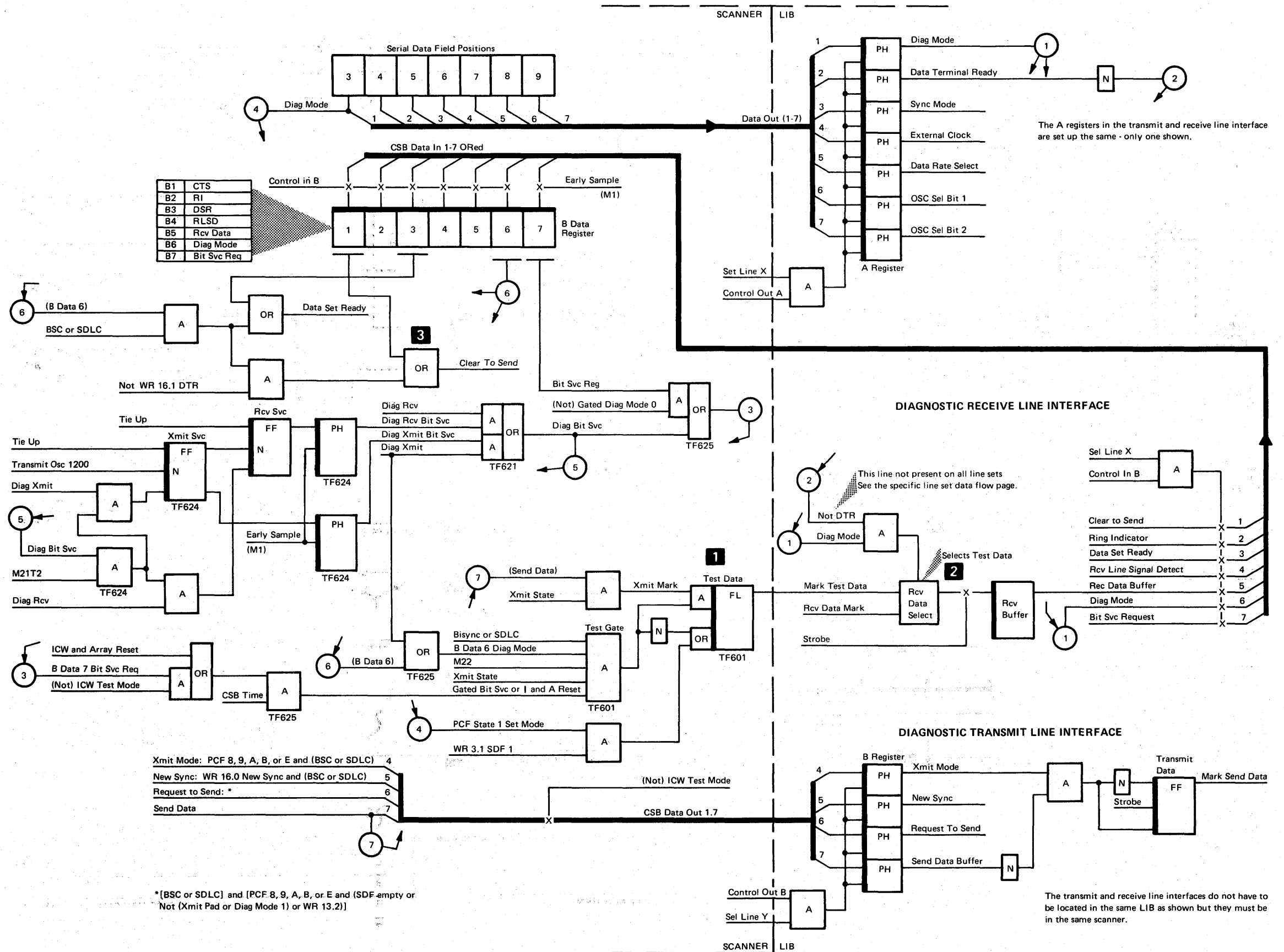
- Provides a means of testing and locating troubles in the type 3 scanner line control logic and line-interface receive logic.
- Provides a method of on-line program testing.
- Can be performed on-line without affecting the operation of lines *not* in diagnostic mode.

SETUP

- Set any one line interface per type 3 scanner to act as a transmit line and any one or more line interfaces in the same scanner to act as receive lines.
- Set Mode is issued to all diagnostic receive line interfaces first, then to the diagnostic transmit line. The SDF field must be set as follows:
 - SDF 3 (Diagnostic Mode) - set to 1.
 - SDF 4 (Data Terminal Ready) - reset to 0.
 - SDF 5 (Sync Mode) - set to 1 for synchronous mode
 - SDF 6 (External Clock) - reset to 0.
 - SDF 7 (Data Rate Select) - set to 0 for 1200 bps set to 1 for 2400 bps
 - SDF 8 and 9 (Oscillator Select 1,2) - Select an available internal oscillator bit rate. The rate must be the same for the transmit and receive line interfaces.

OPERATION

1. After the Set Modes are issued, the affected line interfaces can be exercised through any sequence of point-to-point or multipoint operations.
2. Data bits clocked to the transmit line interface 'send data buffer' are also clocked into the 'test data' latch in the type 3 scanner. **1**
3. As each receive line interface (in diagnostic mode) is scanned, the 'test data' bit is strobed into the 'receive buffer' instead of the 'receive data mark'. **2**
4. When the 'diagnostic mode' bit is a 1 in the B data register (B6) during scan time, the type 3 scanner simulates the active states of:
 - 'Data Set Ready' and 'Clear to Send'. Clear to Send is not simulated **3** active if WR 16.1 DTR is on.



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TYPE 3 CHANNEL ADAPTER

INTRODUCTION

The type 3 channel adapter is a modified type 2 CA that enables the 3705 to be attached to:

- System/370 Model 158 and Model 168 tightly-coupled multiprocessor systems as a symmetric shared I/O device.
- Single processors as an I/O device with an alternate path capability.

Since the type 3 CA is a modified type 2 CA, the description of the Type 2 CA in Section 9 is applicable to the type 3 CA and is not repeated in this section. This section covers the difference between the Type 2 CA and the Type 3 CA: the two-processor switch in the type 3 CA. This section contains those modifications made to the type 2 CA operation. Appropriate references to this section have been added to the associated area in Section 9.

The type 3 channel adapter logic board may be located in the 01A-A4 position of the basic 3705 or the 02A-A4 position of the first expansion frame. The logic pages use the pseudo board location of W4 for the type 3 CA.

Each type 3 CA contains two channels: interface A and interface B. Interface A and interface B are enabled and disabled separately by their own enable/disable switches. Both interfaces may be enabled simultaneously. (This differs from the type 2 CA where enabling interface A disabled interface B.) However, channel operations can only occur over one interface at a time.

Two enable/disable switches and two enable lights are mounted on the 3705 control panel. The two enable/disable switches may alternately be located on a remote configuration console in which case blank buttons are mounted in the switch positions on the 3705 control panel.

NEUTRAL STATE

The channel adapter is in the neutral state when it is operational, not switched to either channel interface, and not removed from either channel interface by means of the disable switch.

SWITCHED STATE

The channel adapter is in the switched state when it is switched (has allegiance) to either interface A or interface B.

- As an example, the CPU attached to the channel A interface automatically switches the channel adapter from the neutral state to the switched state (with allegiance to interface A) by executing a channel program.
- The channel adapter continually monitors channel B interface and responds to any channel B initiated initial selection sequence by:
 1. Trapping Select Out and suspending completion of the selection sequence by not returning Op In! to the channel B interface until the CA returns to the neutral state.
 2. Responding with the control unit busy channel tag sequence.
- The channel adapter switches from the switched state to the neutral state when the channel A interface operation terminates.

DISABLED STATE

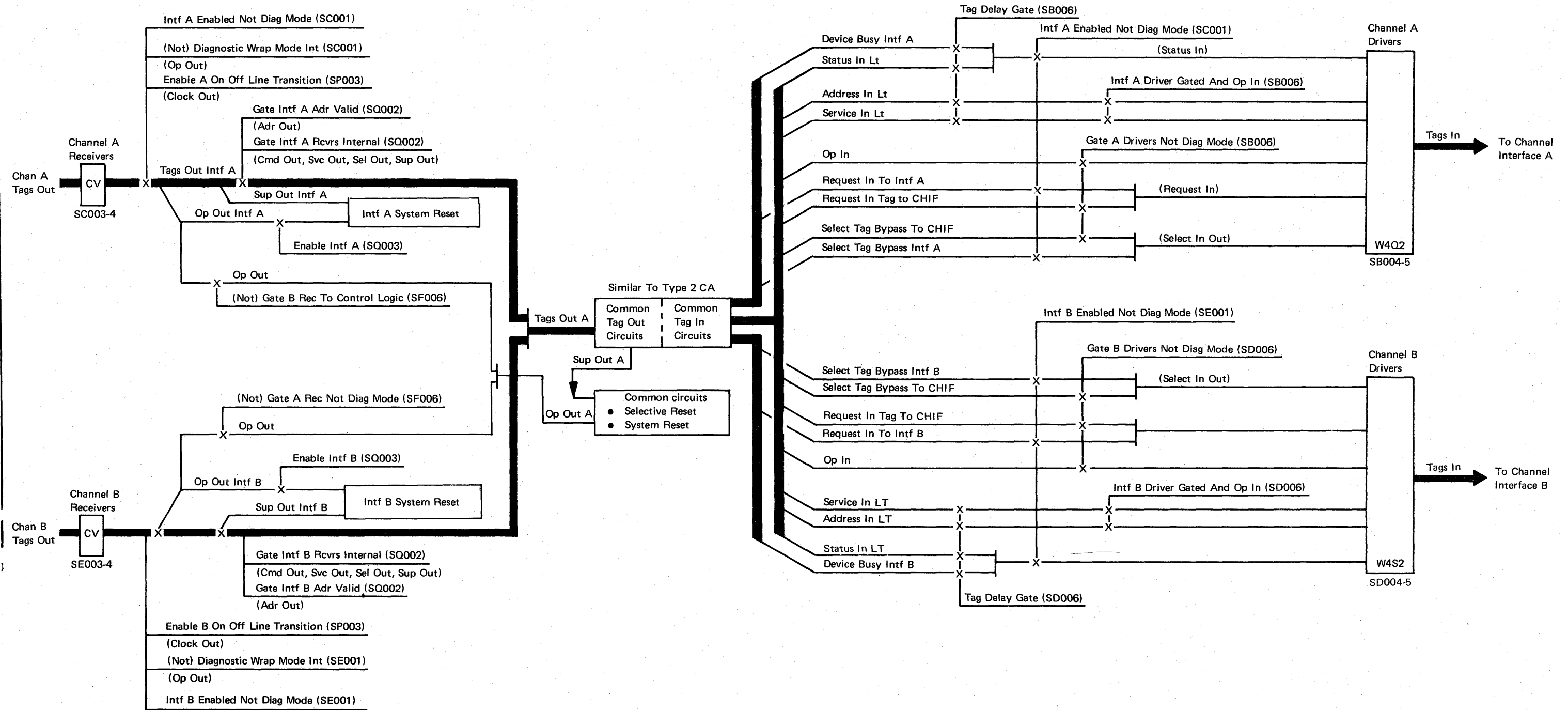
Manually setting the enable/disable switch to the disable position makes the 3705 appear not-operational to the associated channel (condition code 3).

When the channel is executing an I/O operation over one interface (interface A for example), an initial selection attempt by the channel attached to channel B interface of the same type 3 CA causes the channel adapter to present a Busy status to the channel B interface. When the I/O operation on interface A that caused the busy state has terminated, the channel adapter notifies the channel B interface that the busy state has ended by presenting an asynchronous Device End.

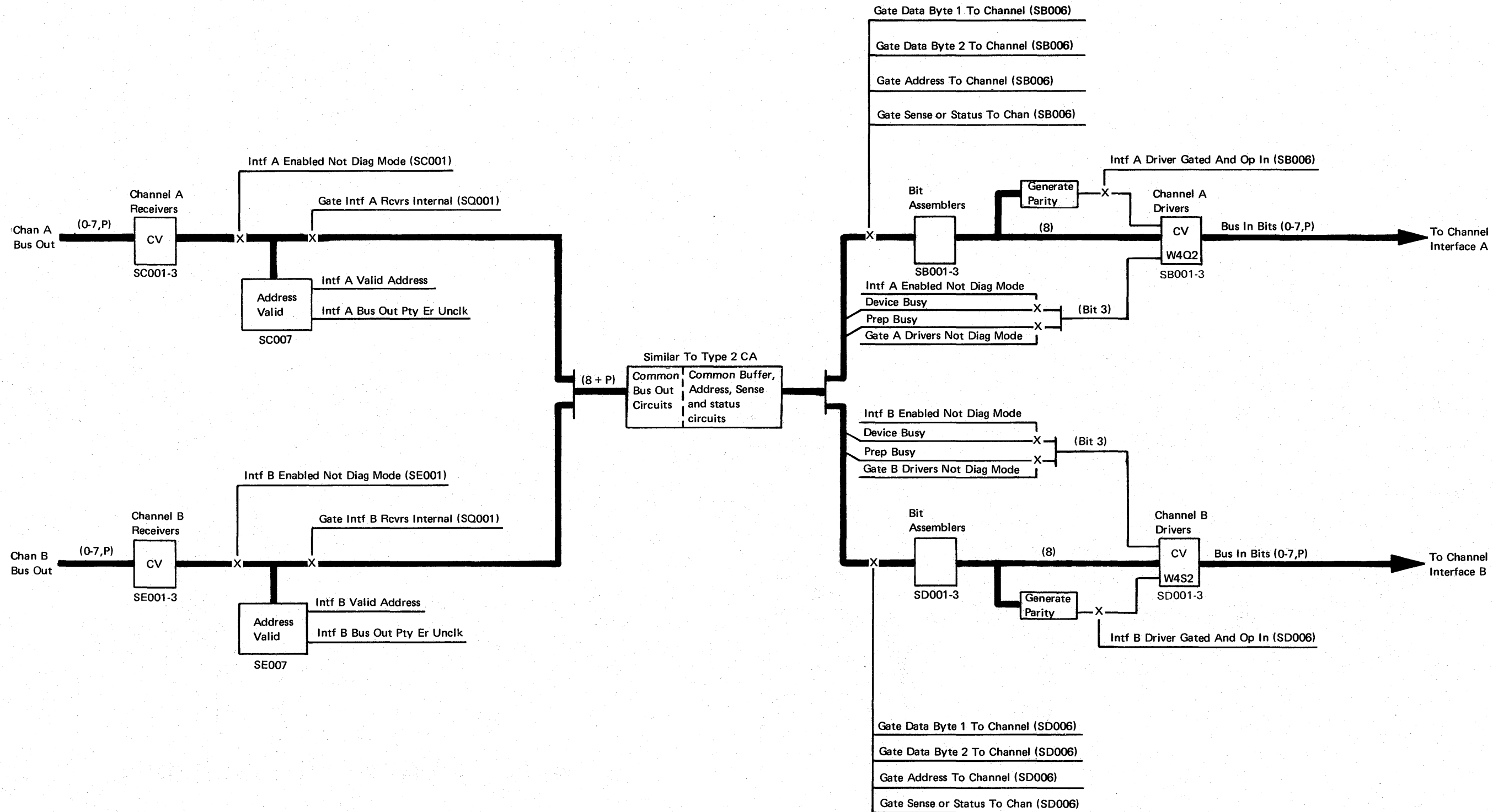
MAINTENANCE PROGRAMS

The type 3 CA uses all the IFT and OLT programs provided for the type 2 CA. In addition, the type 3 CA uses a new OLT (T3705BF) to test the channel adapter's ability to (1) present Busy, (2) remember that Busy had been presented, and later (3) present Device End. OLT T3705BF, in addition to all other type 2 CA IFTs and OLTs, are supported by OLTEP running under OS/VS1, OS/VS2, and DOS/VS. No tests are executable under VTAM because TOLTEP does not support IFT and OLT testing of a channel-attached 3705. 'System Test/370' can configure and test the type 3 CA.

TYPE 3 CA TAG LINES DATA FLOW



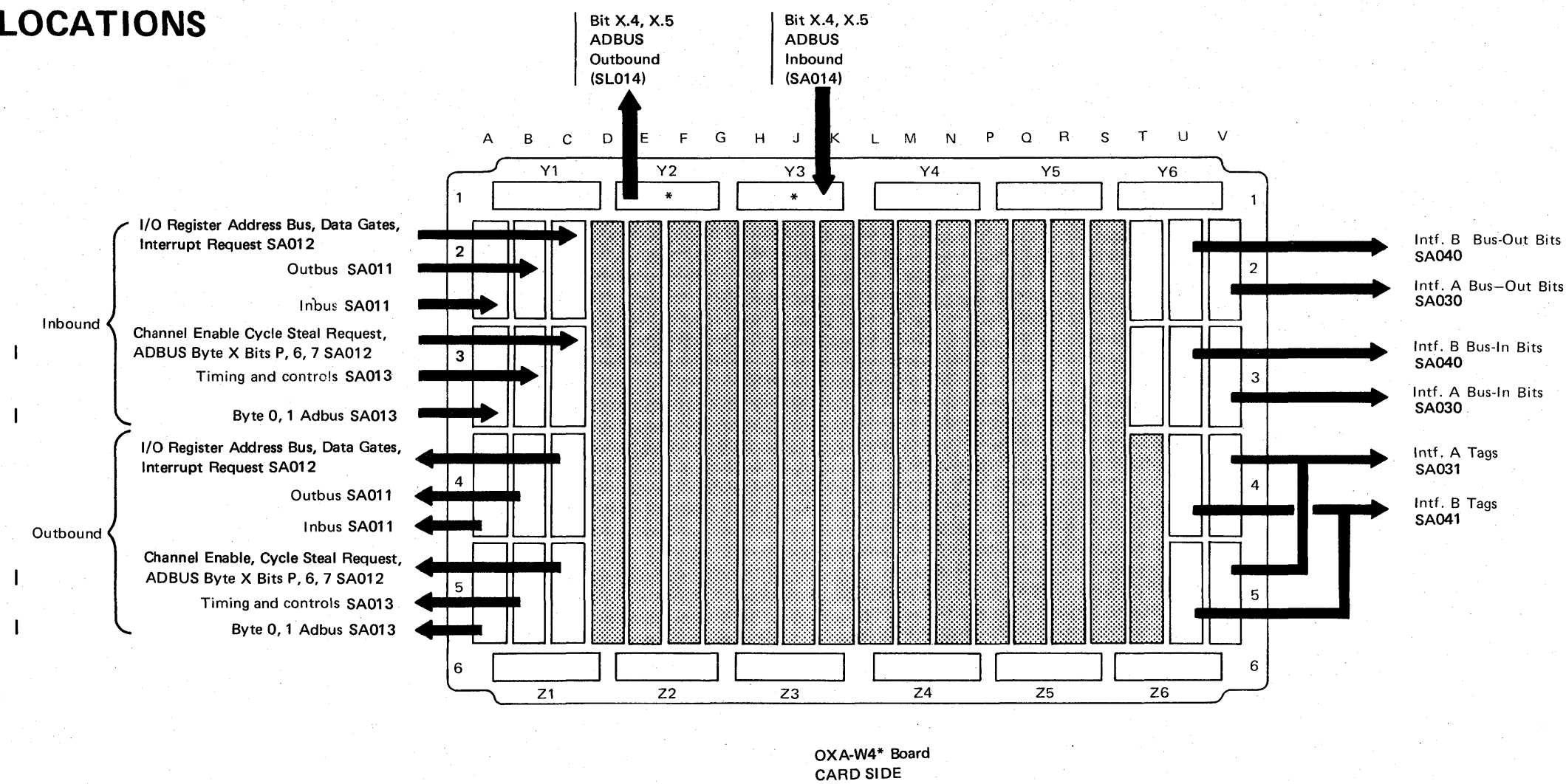
TYPE 3 CA BUS LINES DATA FLOW



CARD FUNCTIONS AND LOCATIONS

Card Loc.	First ALD Page	Function
W4T2	SR011	Cycle Steal Adr Reg Byte X (Models J-L only)
W4T4	SB011	Intf. A and B Select-Out relays
W4Q2	SB001	Interface A Drivers
W4P2	SC001	Interface A Receivers Diagnostic Registers
W4S2	SD001	Intf. B Drivers
W4R2	SE001	Intf. B Receivers
W4N2	SF001	Channel Tag Clock Tag Control Tag Control Powering
W4M2	SG001	Cycle Steal Control Channel Buffer Control Data Transfer Control Control Command Enable
W4L2	SH001	Input/Output Decode Adapter Select Jumpering CW Count Register CWAR valid latches CW Command Decode Diagnostic Wrap Mode Latch
W4K2	SJ001	Interrupt Requests Channel Command Decode
W4J2	SK001	Sense and Status Latches and Gates
W4H2	SL001	Byte 0 of CWAR Data Buffer CSAR CCU Outbus Buffer
W4G2	SM001	Byte 1 of CWAR Data Buffer CSAR CCU Outbus Buffer
W4F2	SN001	CA Check Register Cycle Steal Rate Jumpering Active latch End Busy latch CE Remb latch Increment CSAR Burst Mode latch Error latches
W4E2	SP001	Intf. A Control Logic Intf. B Control Logic Intf. A and B Transition Enable Controls Reset Generation
W2D2	SQ001	Intf. A and B Bus Out Selection Intf. A and B Tag Out Selection Type 3 CA Clock and System Reset

Note:
W4Q2 and S2 can be swapped
W4P2 and R2 can be swapped
W4H2 and G2 can be swapped



OXA-W4* Board
CARD SIDE

*Y2 and Y3 cables are present in Models J-L, only.

*W4 is the pseudo board location for the Type 3 channel Adapter. The actual board location is OXA-A4.

CHANNEL 1 INTERFACE A ENABLE/DISABLE SWITCH

Used to enable and disable channel interface 1A.

Once the enable/disable switch has been thrown to its opposite state, the channel adapter changes state (goes online or offline) when all of the following conditions have been satisfied concurrently:

- The clock-out tag line is inactive, indicating that the CPU is in a wait state.
- The channel adapter is not executing a command on that interface.
- Command chaining is not indicated for that interface.
- Select Out is not active on that interface.
- Device End is not pending in that interfaces 'device end' latch.
- An Input X'58' instruction is not being executed to examine the state of the 'enable' latch.

If the DIAGNOSTIC CONTROL switch is in one of the four STORAGE TEST positions and the START push button is pressed, any interface that is enabled is disabled abruptly. The channel interface enabled light stays on until the CPU drops 'clock out', even though the interface is disabled. No channel can become enabled.

NOTE: Be sure the channel is disabled before performing storage test operations.

CHANNEL 1 INTERFACE B ENABLED LIGHT

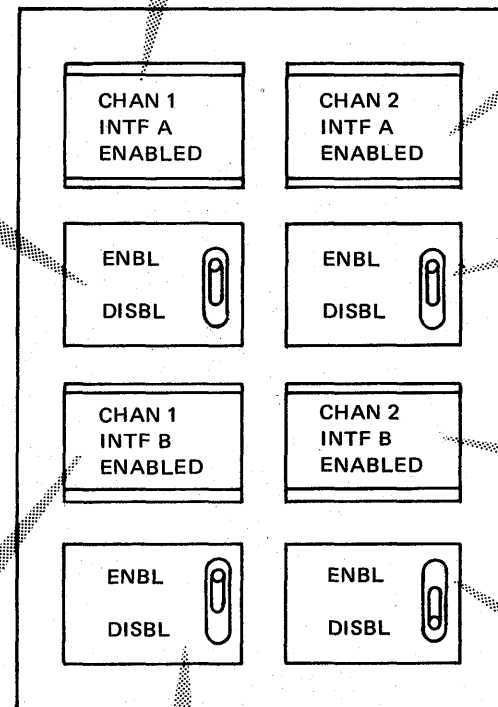
- Turned on when interface 1B is enabled.
- Turned off when interface 1B is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.

CHANNEL 1 INTERFACE A ENABLED LIGHT

- Turned on when interface 1A is enabled.
- Turned off when interface 1A is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.



CHANNEL 1 INTERFACE B ENABLE/DISABLE SWITCH

Used to enable and disable channel interface 1B. The comments for the channel 1 Interface A enable/disable switch apply for this switch too.

CHANNEL 2 INTERFACE A ENABLED LIGHT

- Turned on when interface 2A is enabled.
- Turned off when interface 2A is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.

CHANNEL 2 INTERFACE A ENABLE/DISABLE SWITCH

Used to enable and disable channel 2 interface A. The comments for the channel 1 interface A enable/disable switch apply for this switch too.

CHANNEL 2 INTERFACE B ENABLED LIGHT

- Turned on when interface 2B is enabled.
- Turned off when interface 2B is disabled.

NOTE: The light stays on when the 3705 is in hard stop, even though the adapter is disabled.

CHANNEL 2 INTERFACE B ENABLE/DISABLE SWITCH

Used to enable and disable channel 2 interface B. The comments for the channel 1 interface A enable/disable switch apply for this switch too.

NOTE: This control panel layout only applies if the 3705 contains two type 3 channel adapters and the enable-disable switches are not installed in a remote attachment. Blank gray buttons would replace the two enable-disable switches in this case. See E-040 for control panel configurations when the type 3 CA is used with the type 1 CA, type 2 CA, type 4 CA, and the remote program loader.

OUTPUT X'59' INSTRUCTION

The 3705 control program uses this instruction for OLT diagnostic purposes.

The bit definitions are:

Byte 0 Bit 0 - Set Interface A Busy

When set to 1, an Output X'59' sets:

- 'Force A busy' latch
- 'Intf B sw' latch
- 'Long allegiance chnl B' latch

When channel A initiates an initial-selection sequence, the CA sets the 'intf A busy' latch. This causes a control unit busy sequence during which Busy status is presented to channel A. When the CA is switched to interface A, the CA initiates a service cycle sequence to present Device End status and the 'intf A busy' latch is reset.

Byte 0 Bit 1 - Set Interface B Busy

When set to 1, an Output X'59' causes the same operation to interface B as described above for interface A.

Byte 0 Bit 4 - Reset Interface A Busy

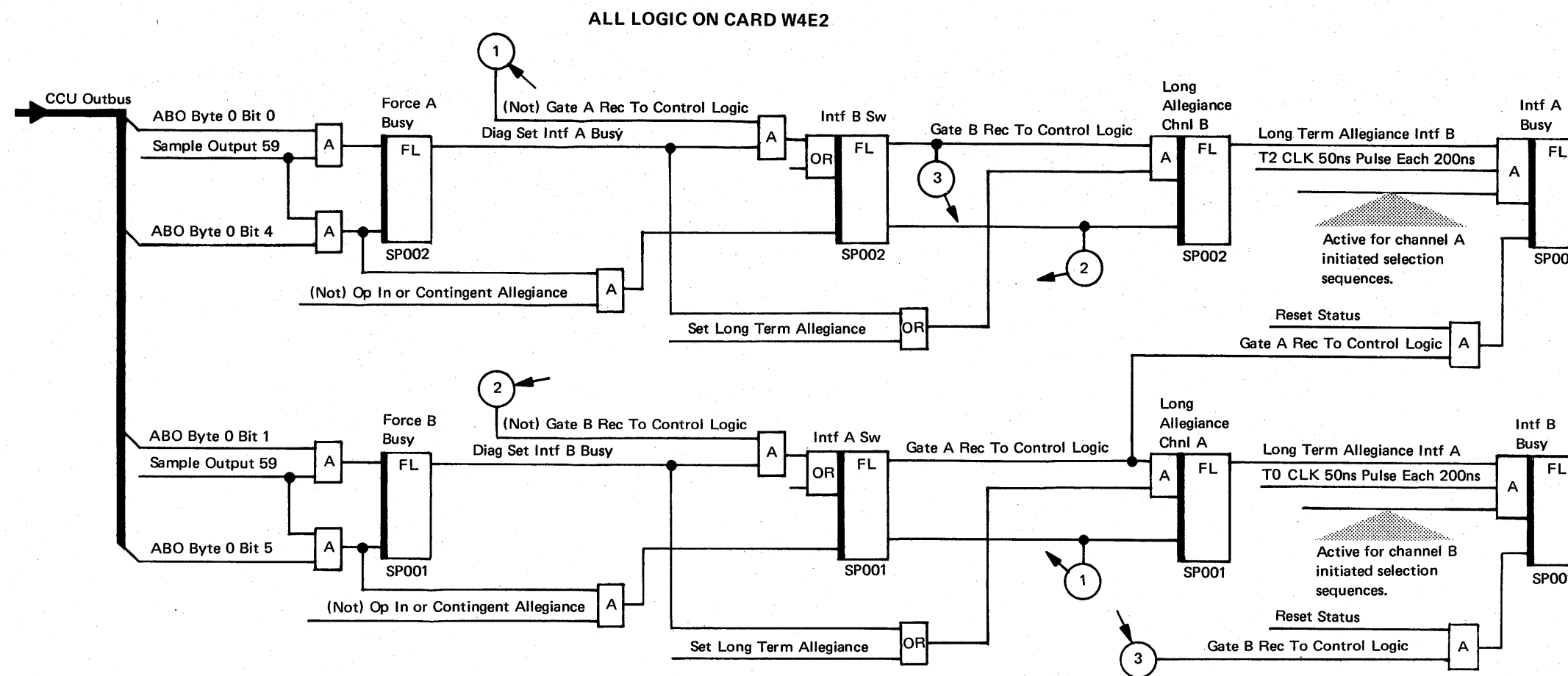
When set to 1, an Output X'59' removes the interface A busy condition by resetting:

- 'Force A busy' latch
- 'Intf B sw' latch
- 'Long allegiance chnl B' latch

Byte 0 Bit 5 - Reset Interface B Busy

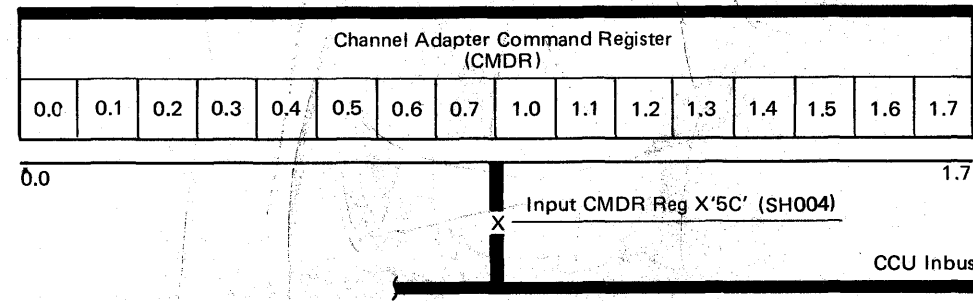
When set to 1, an Output X'59' removes the interface B busy condition by resetting:

- 'Force B busy' latch
- 'Intf A sw' latch
- 'Long allegiance chnl A' latch



INPUT X'5C' INSTRUCTION

The 3705 control program uses this instruction to transfer the contents of the channel adapter command register into a CCU general register.



- Notes:
- The Test I/O command is set into the command register (CMDR) without resetting the previous command.
 - The 3705 control program determines that a control command (invalid command) was issued by the channel by the fact that byte 1 bit 4 is on when none of the command bits are on in Register X'5C'. (See 9-311 for the control command operation.)

LOGIC REFERENCE

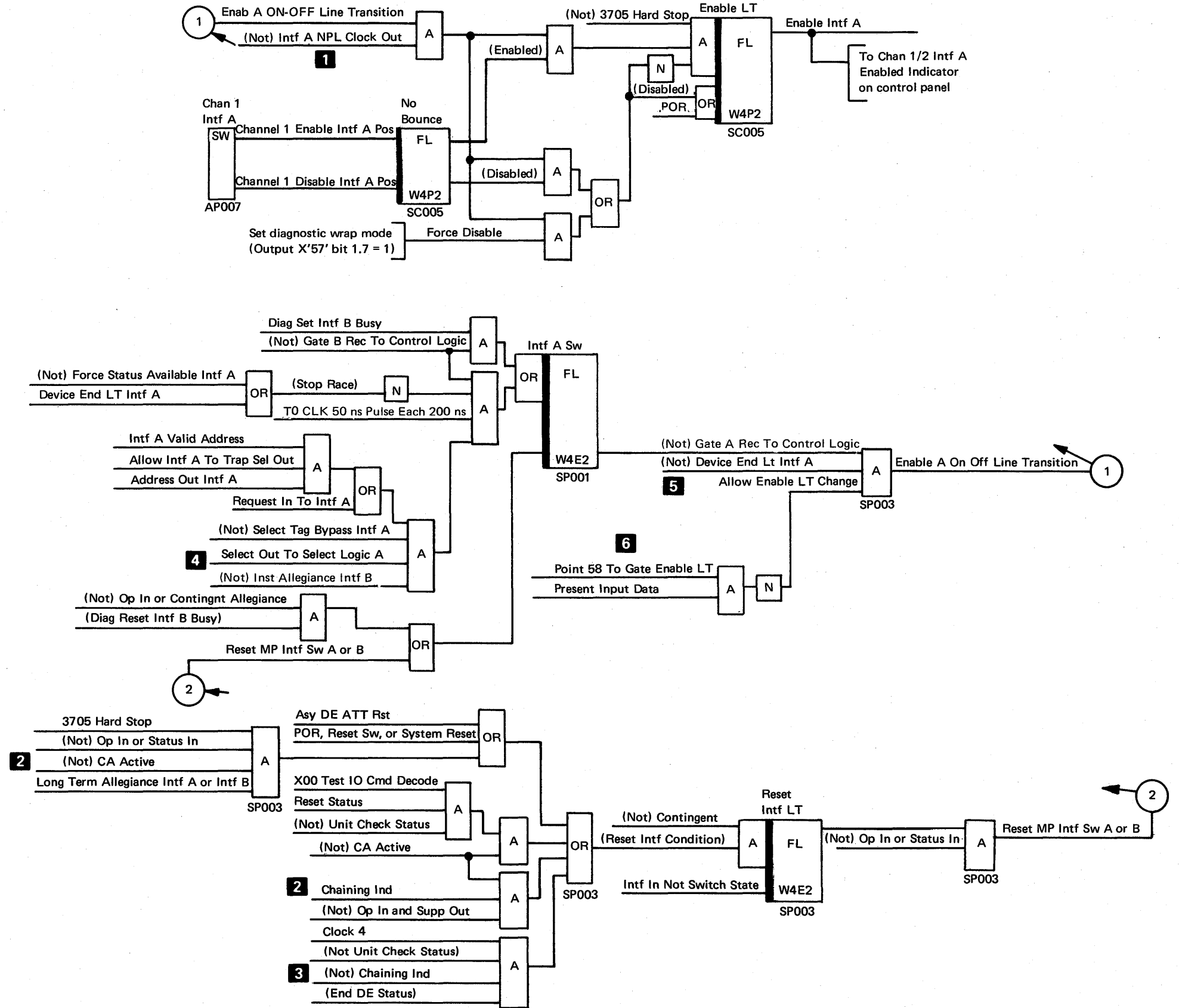
Bit	Card	Logic page	Line name
0.0	W4K2	SJ003	Channel Test I/O
0.1	W4K2	SJ003	Channel Write command
0.2	W4K2	SJ003	Channel Read command
0.3	W4K2	SJ003	Channel No-Op command
0.4	W4K2	SJ003	Channel Sense command
0.5	-----	-----	-----
0.6	W4K2	SJ003	Channel Write Break command
0.7	-----	-----	-----
1.0	W4L2	SH005	Out Ctrl Wd.
1.1	W4L2	SH005	Out Stop Ctrl Wd.
1.2	W4L2	SH005	In Ctrl Wd.
1.3	W4L2	SH005	TIC CW
1.4	W4K2	SJ006	Channel Control command
1.5	W4D2	SQ003	Switched To Interface A
1.6	W4D2	SQ003	Switched To Interface B
1.7	W4K2	SJ003	Channel Write IPL command

ENABLE OR DISABLE TYPE 3 CA INTERFACE

The type 3 CA, unlike the type 2 CA, can have two CPU channel interfaces simultaneously enabled. However, simultaneous operation over the two interfaces is not possible. Either type 3 CA interface may be independently enabled or disabled by means of two toggle switches. These toggle switches may be located on the 3705 control panel. When the System/370 multiprocessing system provides for the remote attachment of these enable/disable switches, the switches may be mounted on a central CPU configuration console, or remote switching console.

Once the enable/disable switch has been thrown to its opposite state, the channel adapter changes state (goes online or offline) when all of the following conditions have been satisfied concurrently:

- The clock-out tag line is inactive, indicating that the CPU is in a wait state. **1**
- The channel adapter is not executing a command on that interface. **2**
- Command chaining is not indicated for that interface. **3**
- Select Out is not active on that interface. **4**
- Device End is not pending in that interface's 'device end' latch. **5**
- An Input X'58' instruction is not being executed to examine the state of the 'enable' latch. **6**



TYPE 3 CA SELECTION FROM A NEUTRAL STATE

The type 3 CA is in the neutral state when the following conditions simultaneously exist:

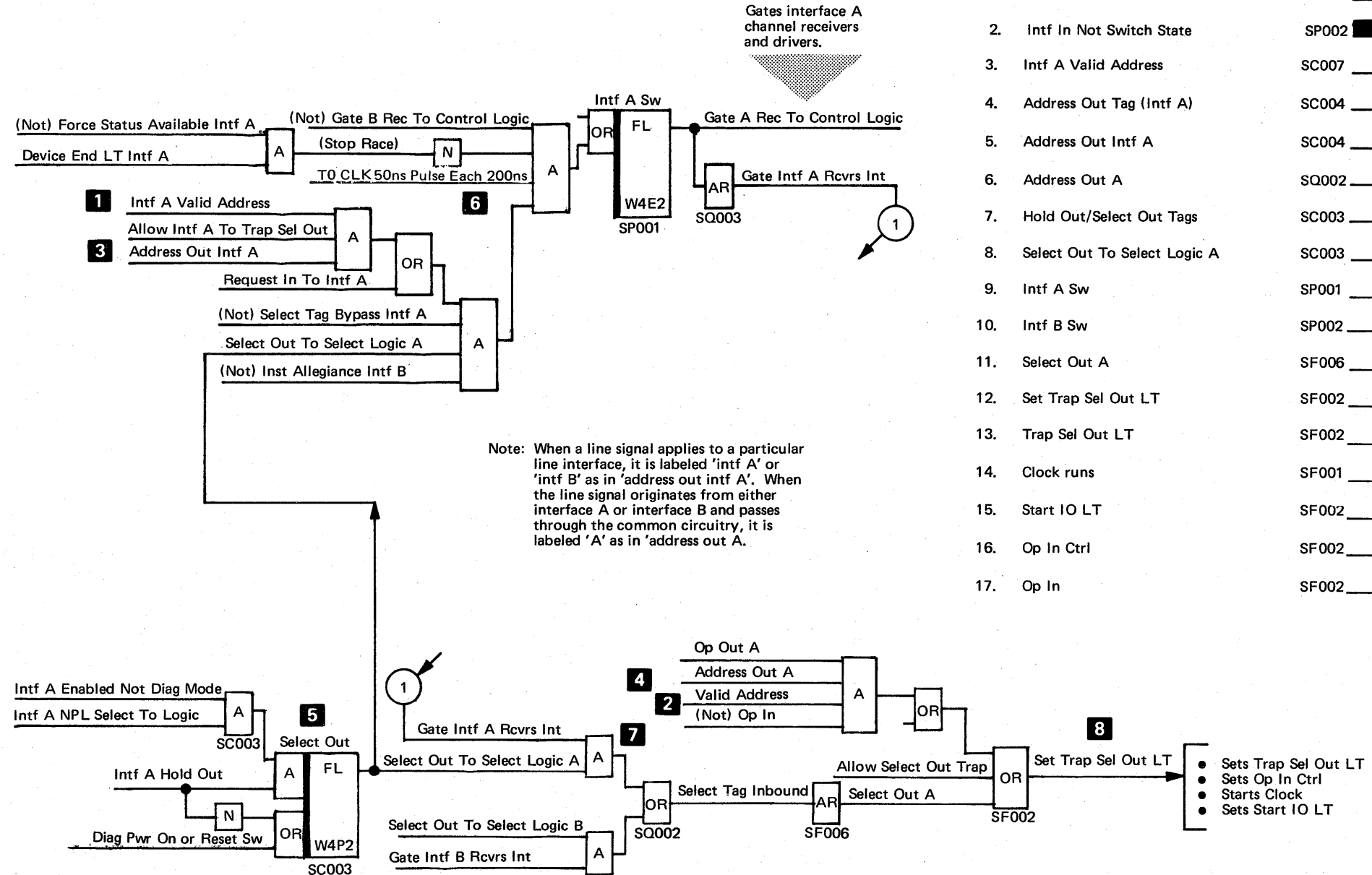
- CA is operational.
- CA is not switched to either channel interface.
- CA is not disabled from either channel interface by the enable-disable switches.

When in the neutral state, the first attached channel to initiate an initial selection sequence selects the type 3 CA by the following operation:

1. Channel A starts an initial selection sequence by placing the address on channel A bus out.
2. The CA determines that the address matches the address assigned to interface A and raises 'intf A valid address' **1** and 'valid address'. **2**
3. When the channel raises the Address Out tag, the CA, in the 'not switched state', raises 'address out intf A' **3** and 'address out A'. **4**
4. When the channel raises the Hold Out and Select Out tags, the CA raises 'select out to select logic A'. **5**
5. The CA sets the 'intf A Sw' at T0 clock pulse. **6**

Note: If both channel interface A and channel interface B started their initial selection sequences so that 'select out to select logic A' and 'select out to select logic B' became active simultaneously, the clock pulse determines which interface is selected. If T2 occurs before T0, the T2 pulse selects interface B. If T0 occurs before T2, the T0 pulse selects interface A.

6. With the CA switched to interface A, the CA gates 'select out to select logic A' to the common circuit 'select out A'. **7**
7. The CA common circuitry raises 'set trap sel out LT' which raises 'Op In' and begins the start IO operation. **8**



When a type 3 CA interface is selected by a channel initial-selection sequence or a channel adapter service cycle sequence (request in), the selection switches the channel adapter to interface B (for example) and places the channel adapter in an instantaneous allegiance state to prevent channel A interface from selecting the channel adapter. The channel adapter always enters the instantaneous allegiance state from the neutral state because the channel adapter doesn't know whether it will return to the neutral state (no additional channel communication required) or to the long term allegiance state (additional data transfer and/or ending status required to complete the channel command). If the channel A interface attempts to select the channel adapter while the channel adapter is in the instantaneous allegiance state, the channel adapter:

- Inhibits setting the interface A switch.
- Inhibits setting the interface A busy latch

Traps select out and inhibits completion of the initial selection sequence until one of the following occurs:

1. The channel adapter passes from instantaneous allegiance to the neutral state with the following results:
 - a. The channel adapter switches to channel A interface (with the suspended-selection sequence) and enters the instantaneous allegiance state.
 - b. The channel adapter completes the suspended-selection sequence without giving the device busy indication.
2. The channel adapter passes from the instantaneous allegiance state to the long term allegiance state with the following results:
 - a. The channel adapter interface for the suspended-selection sequence sends the control-unit-busy sequence to the channel A interface.
 - b. The channel adapter interface for the suspended-selection sequence remembers the busy status and requests a service cycle (request in) to present Device End status when the long term allegiance state passes to the neutral state.

Instantaneous Allegiance Passes To Neutral

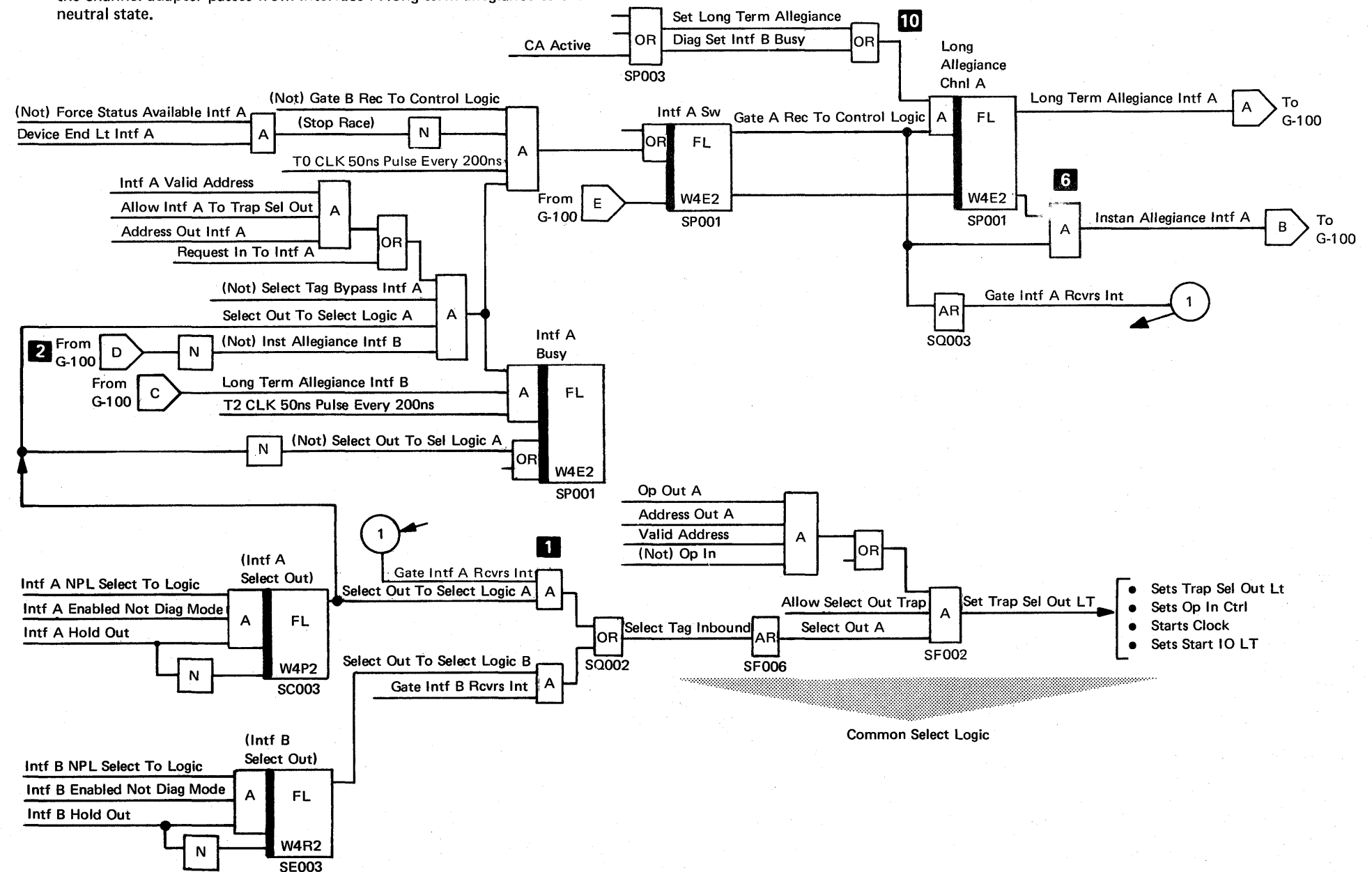
In this example, the channel adapter is in the instantaneous allegiance state having been switched to interface B. The channel attached to interface A starts an initial selection sequence by sending Address Out, Hold Out, and Select Out.

1. 'Select out to select logic A' for interface A can not be gated to the common select logic because the channel adapter is switched to interface B. **1**
2. The instantaneous allegiance state of interface B inhibits the picking of 'intf A sw' and 'intf A busy' latches. **2**
3. Because the channel adapter is switched to interface B, 'Op In' (from the common logic) can not be sent to the channel attached to interface A. This suspends the initial selection sequence for interface A until (in this example) 'intf B sw' resets after the status has been presented to the channel on interface B. **3**
4. The reset of 'intf B sw' drops 'instan allegiance intf B' **4** and raises 'intf in not switch state'. **5**
5. The fall of 'instan allegiance intf B' **2** picks 'intf A sw' which switches the channel adapter to interface A and puts the channel adapter in instantaneous allegiance state. **6**
6. The channel adapter gates 'select out to select logic A' to the common select logic **1** which results in Op In tag being sent to the channel attached to intf A. This resumes the initial selection sequence.

Instantaneous Allegiance Passes To Long Term Allegiance

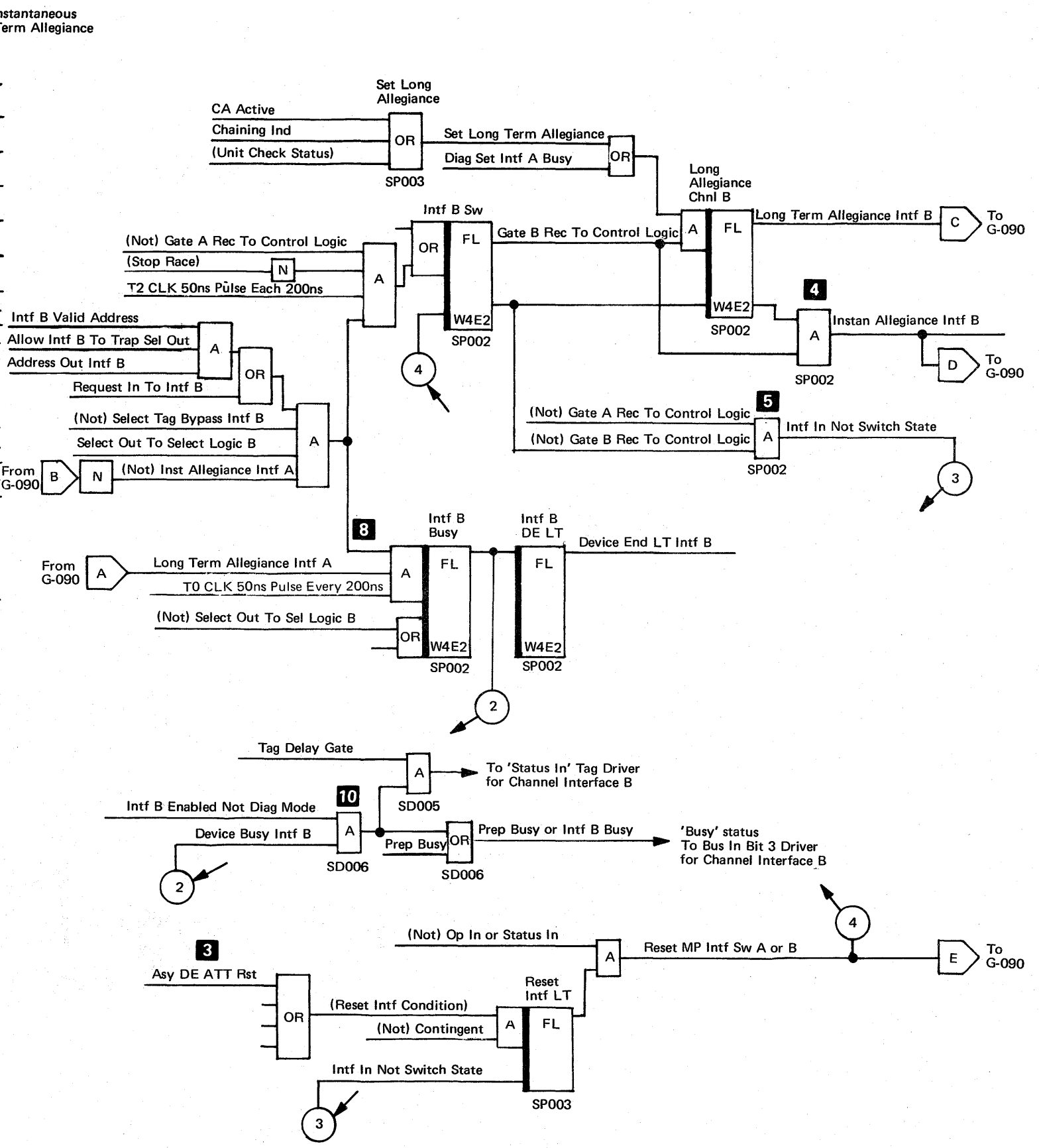
In this example the channel attached to interface B starts another initial selection sequence while the channel adapter is in instantaneous allegiance to interface A. The channel adapter traps select out and inhibits the completion of the initial selection sequence as described above.

1. The command received during the interface A Start IO requires a data transfer, therefore, 'CA active' picks the 'long allegiance chnl A' latch. **7**
2. This drops 'instan allegiance intf A' which picks 'intf B busy' latch. **8**
3. The channel adapter interface B sends the Status In tag with the Busy bit 3 on bus in as a control-unit-busy sequence. **10**
4. The channel adapter sets 'intf B DE' latch to remember that a busy status was given to the channel and that Device End status must be presented when the channel adapter passes from interface A long term allegiance to the neutral state.



- Sets Trap Sel Out Lt
- Sets Op In Ctrl
- Starts Clock
- Sets Start IO LT

INSTANTANEOUS ALLEGIANCE STATE, PART 2



LONG TERM ALLEGIANCE STATE

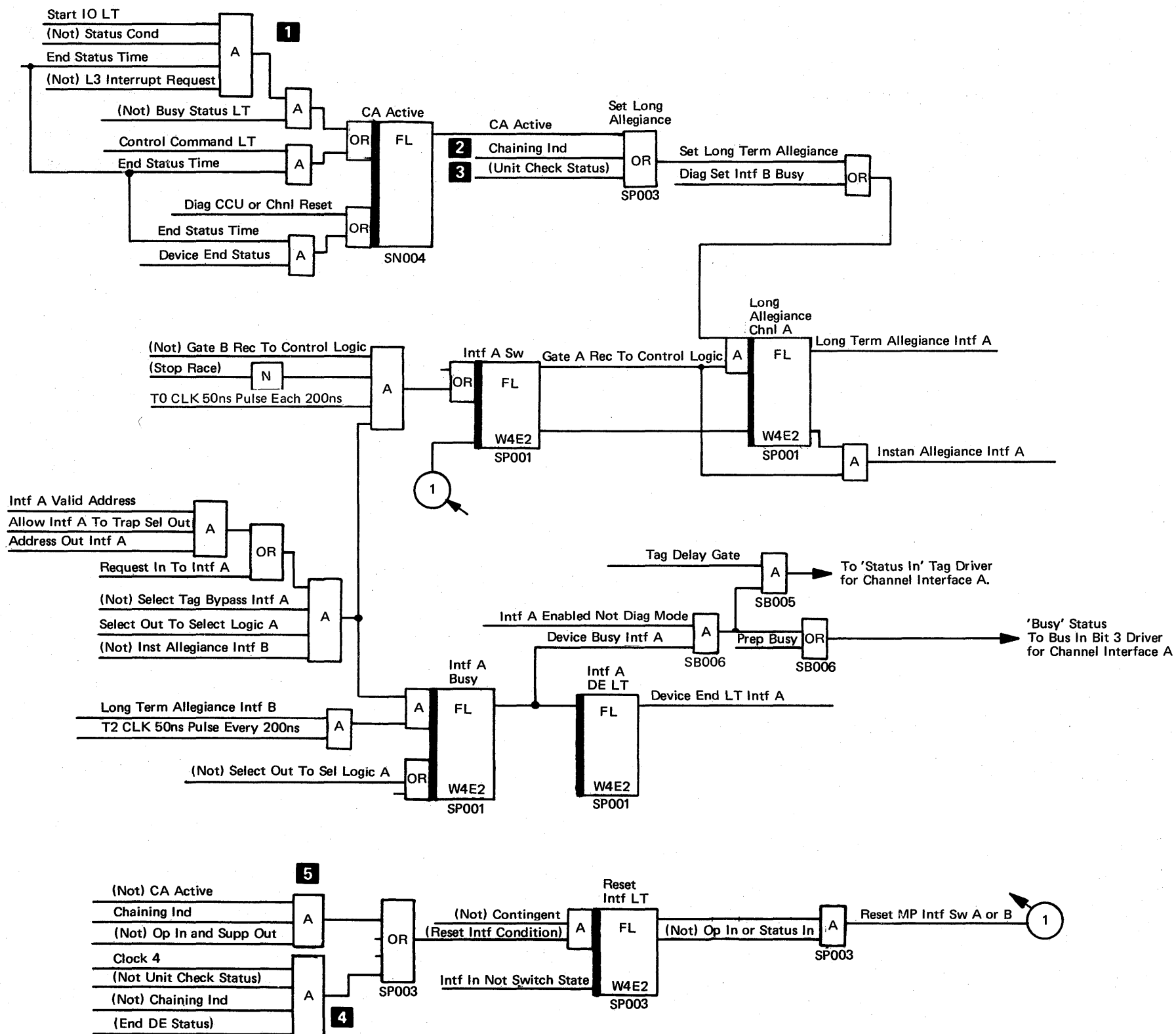
When the channel adapter is in the instantaneous allegiance state, the channel adapter sets the long term allegiance state when:

- The channel accepts an all-zero initial status for a channel command that must have data and/or ending status transferred over the interface. **1**
- Command chaining is indicated. **2**
- Unit check is presented as either initial or final status. **3**

The channel adapter interface passes from long term allegiance to the 'not switched state' when:

- The channel accepts Device End for the last command executed under a particular start IO instruction. **4**
- The command chaining indication is suppressed following the channel's acceptance of Device End but before a reselection sequence occurs. **5**

A channel initiated initial-selection sequence over the interface opposite the one to which the channel adapter owes long term allegiance results in the channel adapter presenting a device busy status by means of the control-unit busy sequence.



1.	Intf B Sw	SP002	████████████████████
2.	Long Term Allegiance (Intf B)	SP002	████████████████████
3.	Intf In Not Switch State	SP002	────────────────────────
4.	Operational Out Intf A	SC003	████████████████████
5.	Intf A Valid Adr	SC007	██████████ 6
6.	Address Out Tag (Intf A)	SC004	██████████ 14
7.	Address Out Intf A	SC004	6 ██████████ 6
8.	Hold Out/Select Out (Intf A)	SC003	██████████ 14
9.	Select Out To Select Logic A	SC003	8 ██████████ 8
10.	Intf A Busy	SP001	5,7,9 ██████████ 9
11.	Intf A DE LT	SP001	10 ██████████████████
12.	Bus In Bit 3	SB002	10 ██████████ 10
13.	Tag Delay Gate	SB006	10 ██████████ 10
14.	Status In Tag	SB005	10,13 ██████████ 10

CONTINGENT STATE

If the type 3 CA ends a channel command with Unit Check (error condition), the channel adapter enters a contingent state with long term allegiance to the interface over which the Unit Check was presented. When in the contingent state, the channel adapter ensures that the same channel path is available for use by a Sense command that the channel could issue after the I/O operation with the Unit Check has ended. The contingent state ends when:

- The channel adapter decodes a command other than Test IO or NO-OP.
- The channel adapter detects a system or selective reset on the interface to which the adapter is switched.
- A 3705 hard stop occurs.

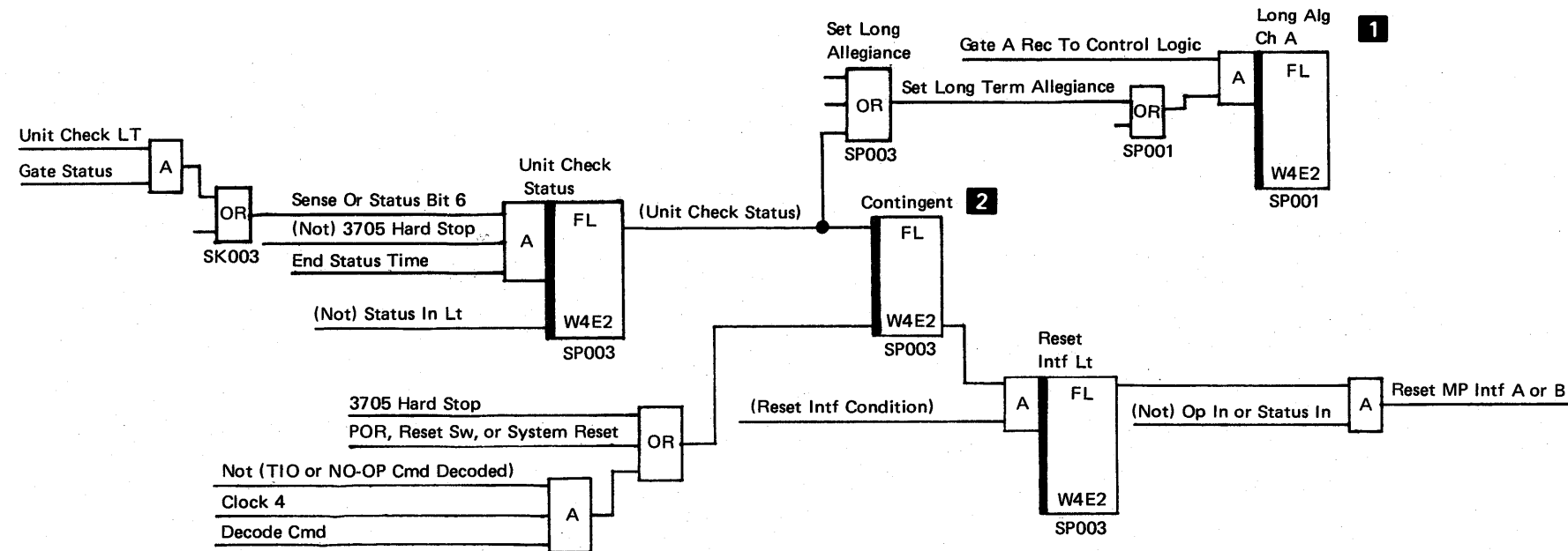
A Halt IO to the interface in the contingent state does not affect the contingent state.

In this example, the channel adapter has set the 'unit check' latch while in instantaneous allegiance to interface A. As the CE, DE, UC status is presented to the channel, status bit 6 (Unit Check) sets the (unit check status) latch which:

- Sets the switched interface to the long term allegiance state. **1**
- Sets the 'contingent' latch. **2**

The active state of the 'contingent' latch inhibits the set of the 'reset intf' latch, therefore, the channel adapter remains switched to interface A. If the interface A channel issues:

- A Sense command to retrieve the sense data, the 'contingent' latch resets and the normal sense operation proceeds.
- Any command other than the Sense, Test IO, or NO-OP, the 'contingent' latch resets and the Unit Check sense data resets.
- A Test IO or NO-OP command, the 'contingent' latch is not reset and the sense data may be obtained by the channel issuing a sense command as the next command.



1. Intf A Sw	SP001	[Bar]
2. Instan Allegiance (Intf A)	SP001	[Bar] 6
3. Unit Check LT (common)	SK003	[Bar] CLK
4. (Unit Check Status) (common)	SP003	[Bar] 3,15 CLK
5. Contingent LT (common)	SP003	[Bar] 4 CLK 4,14
6. Long Allegiance Intf A	SP001	[Bar] 1,4
7. Address Out Intf A	SC004	[Bar] 11
8. Hold Out/Select Out (Intf A)	SC003	[Bar] 12
9. Trap Sel Out	SF002	[Bar] T2,7,8
10. Start IO	SF002	[Bar] 9 15, CLK 4
11. Op In (common)	SF002	[Bar] 15, CLK 9 17
12. Address In To Chnl (Intf A)	SB004	[Bar] 7,11 CLK
13. Command Out (Intf A)	SC004	[Bar] 12 12 Sense Cmd
14. Sense LT	SJ003	[Bar] CLK 2,13 All Zeros
15. Status In Lt (common)	SF003	[Bar] CLK 10,13
16. Status In Tag (Intf A)	SB005	[Bar] 15 Delay, 15 15
17. Service Out (Intf B)	SQ002	[Bar] 16 16 16
18. CA Active (common)	SN004	[Bar] CLK, 10,15

ASYNCHRONOUS DEVICE END

Busy Status Initiated Device End

When the type 3 CA has given a Busy status (due to the channel adapter's long term allegiance to the opposite interface), the channel adapter will present an asynchronous Device End over the interface on which the Busy indication was given. This notifies the channel that the channel adapter has terminated its long term allegiance to the opposite interface. The channel adapter logic generates, presents or stacks this asynchronous Device End without any 3705 control program intervention.

In this example, the channel adapter is in the long term allegiance state having been switched to interface B. During this long term allegiance, the channel attached to interface A attempted to select the channel adapter and the channel adapter returned a Busy status to the channel. The channel adapter remembers the busy condition by means of the 'intf A DE' latch.

When the operation on interface B has terminated, the channel adapter resets 'intf B switch' and the channel adapter goes in the 'intf in not switch state'. The channel adapter then sets the 'force status available' latch which activates:

- 'Status bit 5'. This generates Device End status on bus in to the channel at status in time.
- 'Request in tag to CHIF'. The Request In tag can not be presented to the channel because the channel adapter is not switched to either interface. Therefore, the channel adapter sets the 'force req in A' latch (G-140) which presents Request In to the channel A interface during this not-switched state.

When the channel presents Select Out to interface A, the channel adapter picks 'intf A Sw'. The channel adapter then:

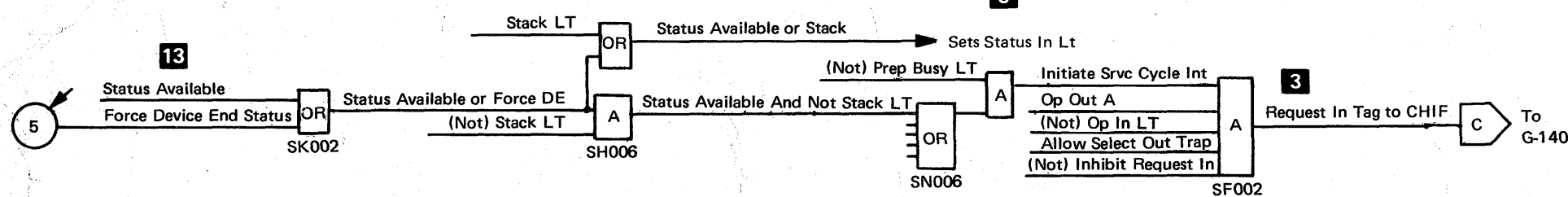
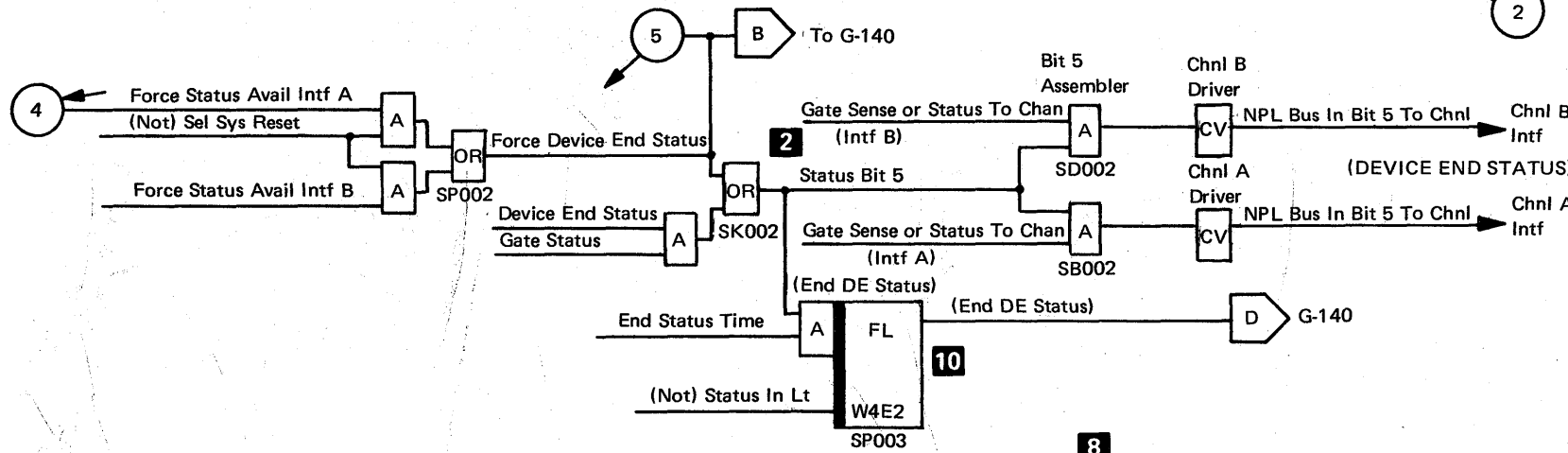
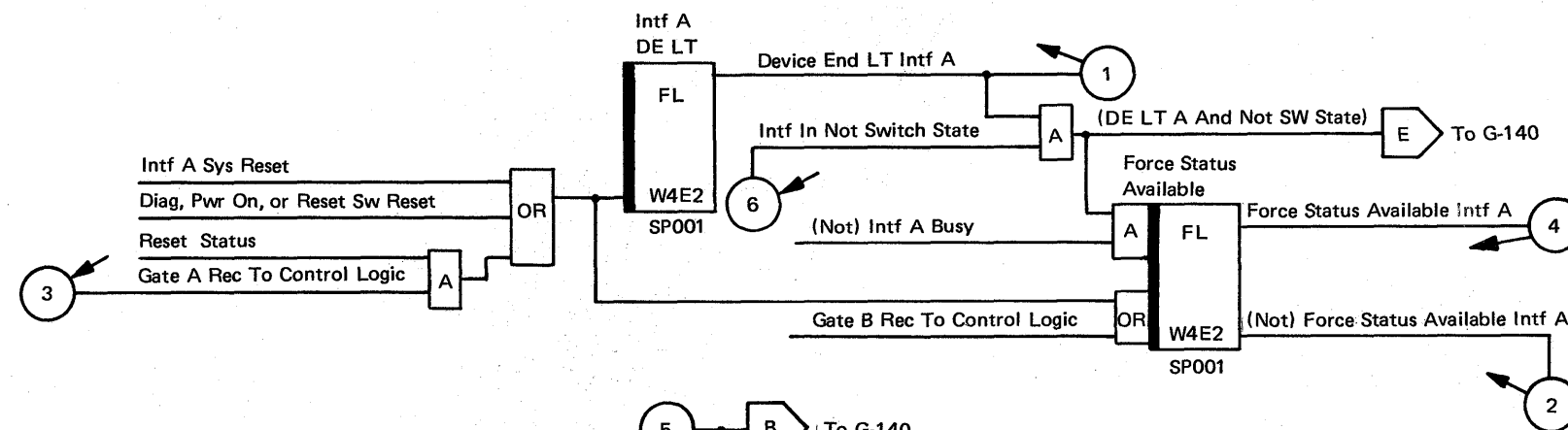
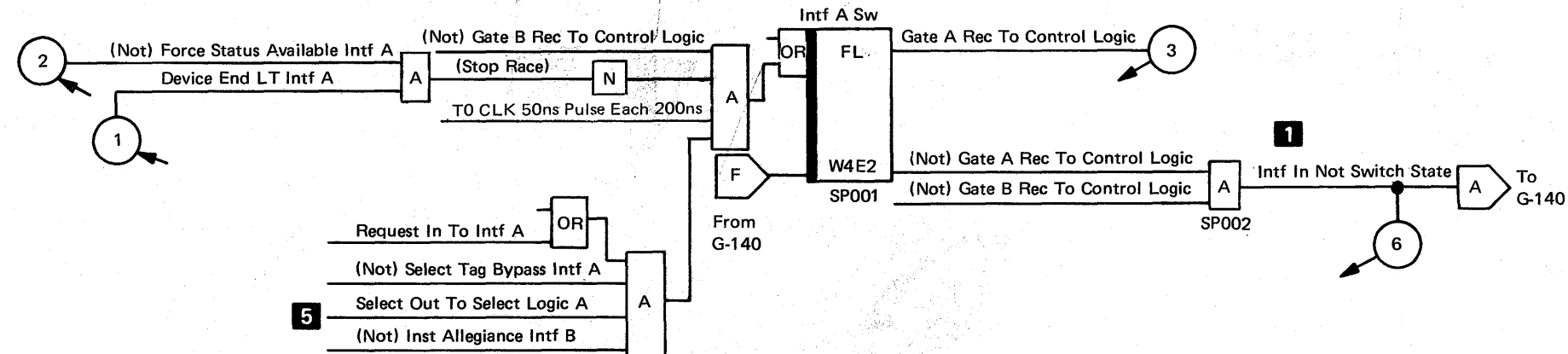
- Gates the channel interface A receivers and drivers.
- Goes into instantaneous allegiance to interface A.
- Traps select out. (G-140)
- Sets the (async status switch) latch. (G-140)
- Sets the 'status in' latch. The channel adapter places Device End status on bus in and raises the Status In tag.
- Sets the (end DE status) latch that sets the 'reset intf' latch. (G-140)
- Resets the (async status switch) to set the 'assemble DE ATT rst' latch. (G-140). This sets the 'reset intf' latch which resets the 'intf A switch' and puts the channel in the not-switched state.

Control Program Initiated Device End

The 3705 control program may initiate an asynchronous Device End by executing Output X'57' with byte 0 bit 3 set to 1 (Set IPL Device End). The channel adapter offers the Device End to both attached interfaces by raising both request-in tag lines. The first channel to raise Select Out is given the Device End status.

Device end status activates:

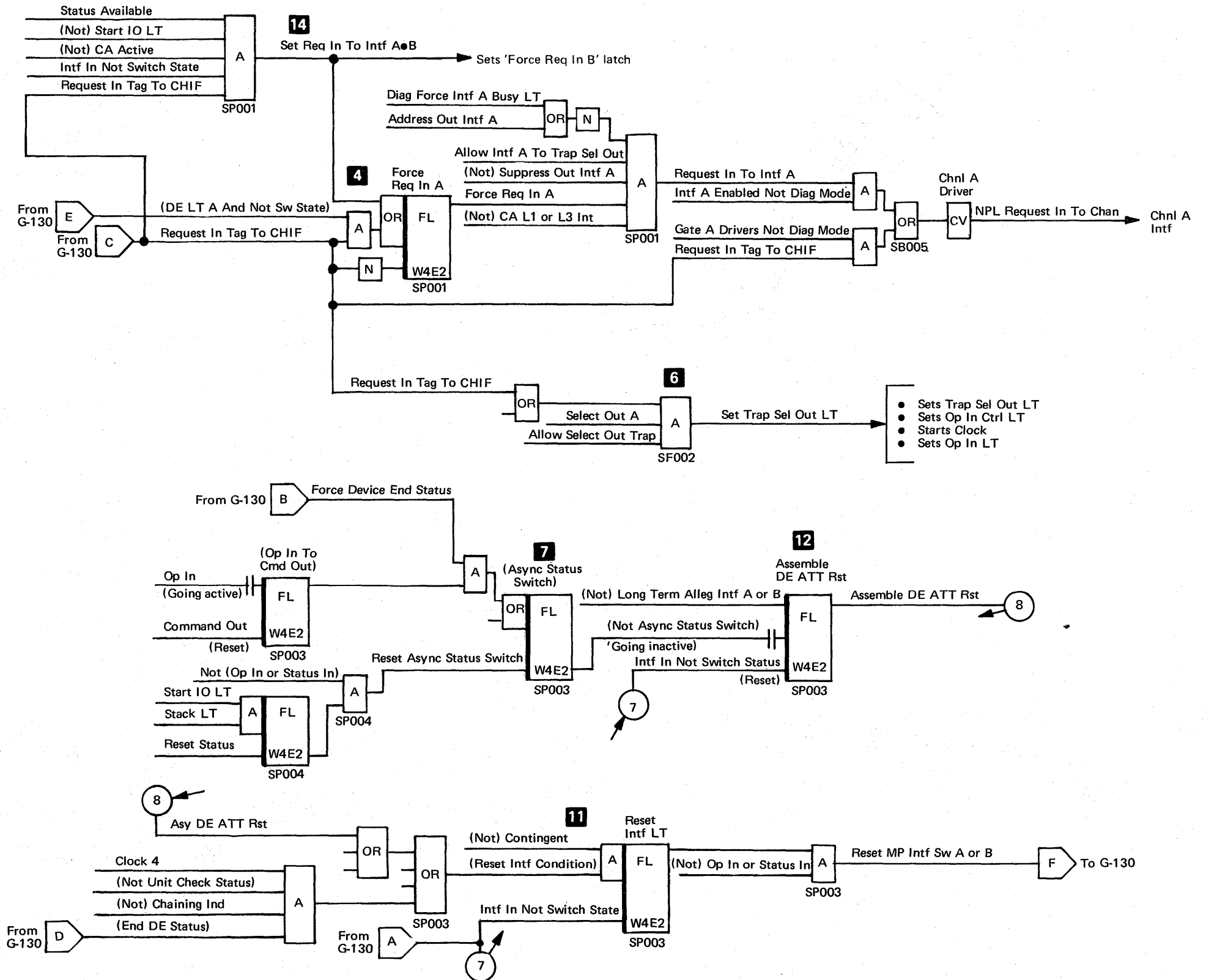
- 'Status available' which raises 'request in tag to CHIF' and then 'set req in to intf A and B' (G-140). This sets the 'force req in A' latches for interface A and interface B and presents Request In tag to both interfaces.
- 'Status bit 5'. This presents the Device End status to the channel interface that first selected the channel adapter.



ASYNCHRONOUS DEVICE END, PART 2

1. Intf B Switch	SP002	32
2. Long Term Allegiance (Intf B)	SP002	1
3. Intf In Not Switch State	SP002	1,14 14
4. Operational Out (Intf A)	SC003	NOTE
5. Intf A DE LT	SP001	19,27
6. Force Status Available (Intf A)	SP001	3,5 5
7. Status Bit 5 (common)	SK002	6 6
8. Initiate Service Cycle (common)	SF002	6 6
9. Request In Tag To CHIF (common)	SF002	8 21
10. Force Req In A	SP001	5,9 9
11. Request In To Intf A	SP001	10 10
12. Hold Out/Select Out (Intf A)	SC003	24 28
13. Select Out To Select Logic A	SC003	12 12 12
14. Intf A Switch	SP001	11,13 32
15. Instan Allegiance Intf A	SP001	14 14
16. Select Out A	SF006	13,14 12
17. Set Trap Sel Out LT (common)	SF002	9,16, 9
18. Trap Sel Out LT (common)	SF002	T2,17 16
19. Clock runs (common)	SF001	18 26 29
20. Op In Ctrl (common)	SF002	18 19,27
21. Op In (common)	SF002	CLK 1,20 16,19
22. (Op In To Cmd Out LT) (common)	SP003	21 26
23. Async Status Switch (common)	SP003	6,21 21,27
24. Address In LT (common)	SF003	20 26
25. Tag Delay Gate (Intf A)	SB006	ADR IN Tag 20 21,28
26. Command Out (Intf A)	SC004	24
27. Status In LT (common)	SF003	Proceed, 6,26 19
28. Status In Tag (Intf A)	SB005	25,27 27
29. Service Out (Intf A)	SQ002	27 28
30. (End DE Status) (common)	SP003	7,19 27
31. Assemble DE ATT Rst (common)	SP003	Not Long Alleg, 23 3
32. Reset Intf LT (common)	SP003	19,30 3

Note: Intf A DE LT became active during a previous selection attempt while the channel adapter was in long term allegiance to interface B.



ASYNCHRONOUS ATTENTION STATUS

The type 3 CA generates an asynchronous Attention status when the 3705 control program executes an:

- Output X'57' with byte 0 bit 0 set to 1 (Set IPL Attention) while in IPL phase 3.
- Output X'55' with byte 0 bit 6 set to 1 (Set Prog Requested Attention) when the channel adapter has its level 3 interrupt request pending. (The channel adapter waits until its level 3 interrupt request is reset before generating the Attention status.)

The channel adapter offers the Attention status to both attached interface by raising both interface Request In tags. The first channel to raise Select Out is given the Attention Status.

In this example, the 3705 control program executed an Output X'55' with byte 0 bit 6 set to 1 to set the 'attention request' latch. The channel adapter presents the status for interface B, resets the status latches and resets 'intf B switch'. The channel adapter then sets the 'attention' latch. If there is no L3 interrupt request nor hard stop, the channel adapter raises 'status available' **1** which activates:

- 'Request in tag to CHIF'. **2** The Request In tag can not be presented to the channel because the channel adapter is not switched to either interface. Therefore, the channel adapter sets the 'force req in A' and 'force req in B' latches **3** which presents Request In to both channels during this not-switched state.

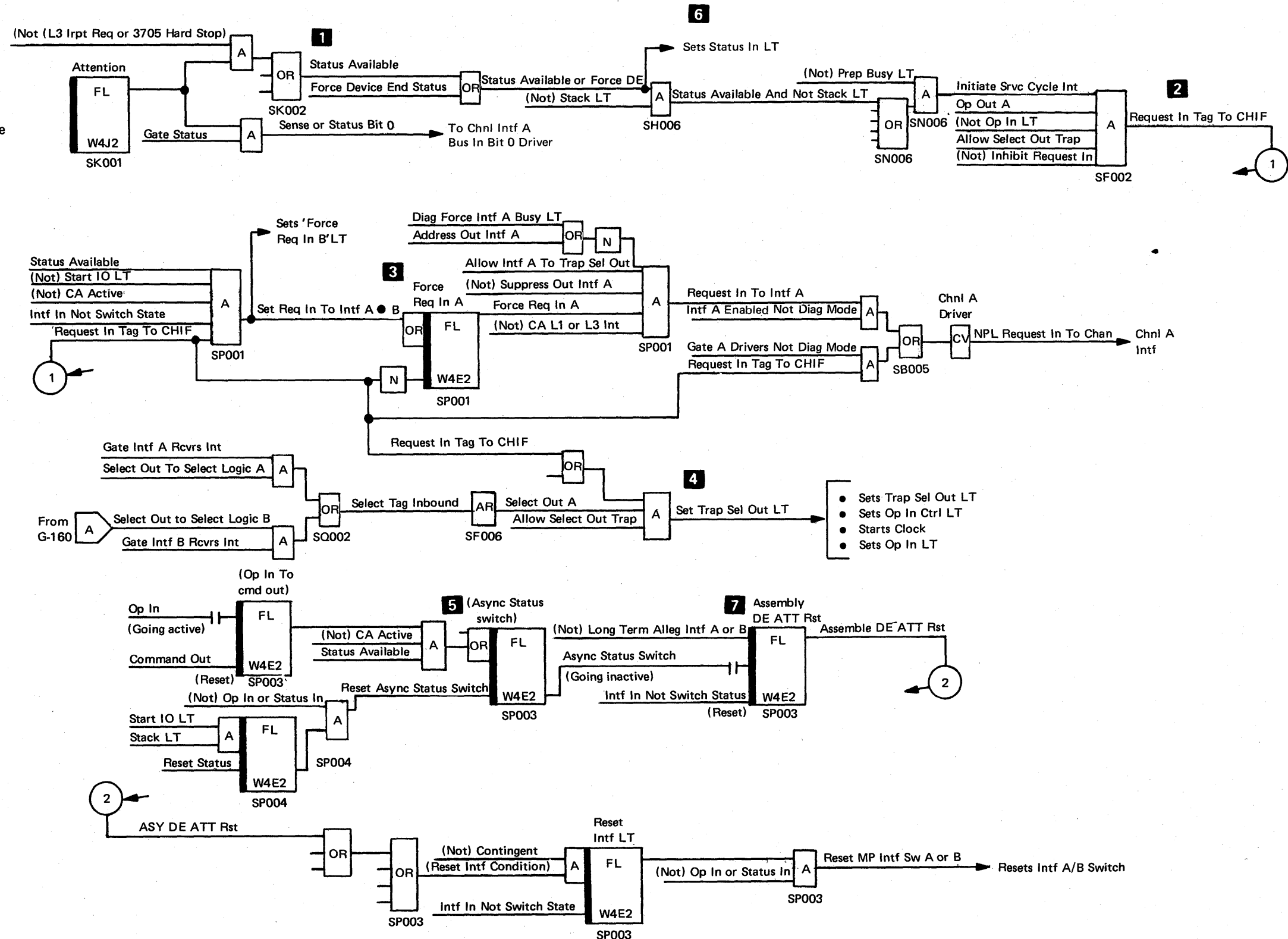
If channel interface A presents Select Out before channel interface B, the channel adapter switches to interface A and:

- Gates the channel interface A receivers and drivers.
- Goes into instantaneous allegiance to interface A.
- Traps select out. **4**
- Sets the (async status switch) latch. **5**
- Sets the 'status in' latch. **6** The channel adapter places Attention on bus in and raises the Status In Tag.
- Resets the (async status switch) to set the 'assemble DE ATT rst' latch. **7** This sets the 'reset intf' latch which resets the 'intf A switch' and puts the channel in the not-switched state.

If channel interface B presents Select Out during the interface A selection sequence that presents the Attention status, the channel adapter bypasses the interface B Select Out to the next unit.

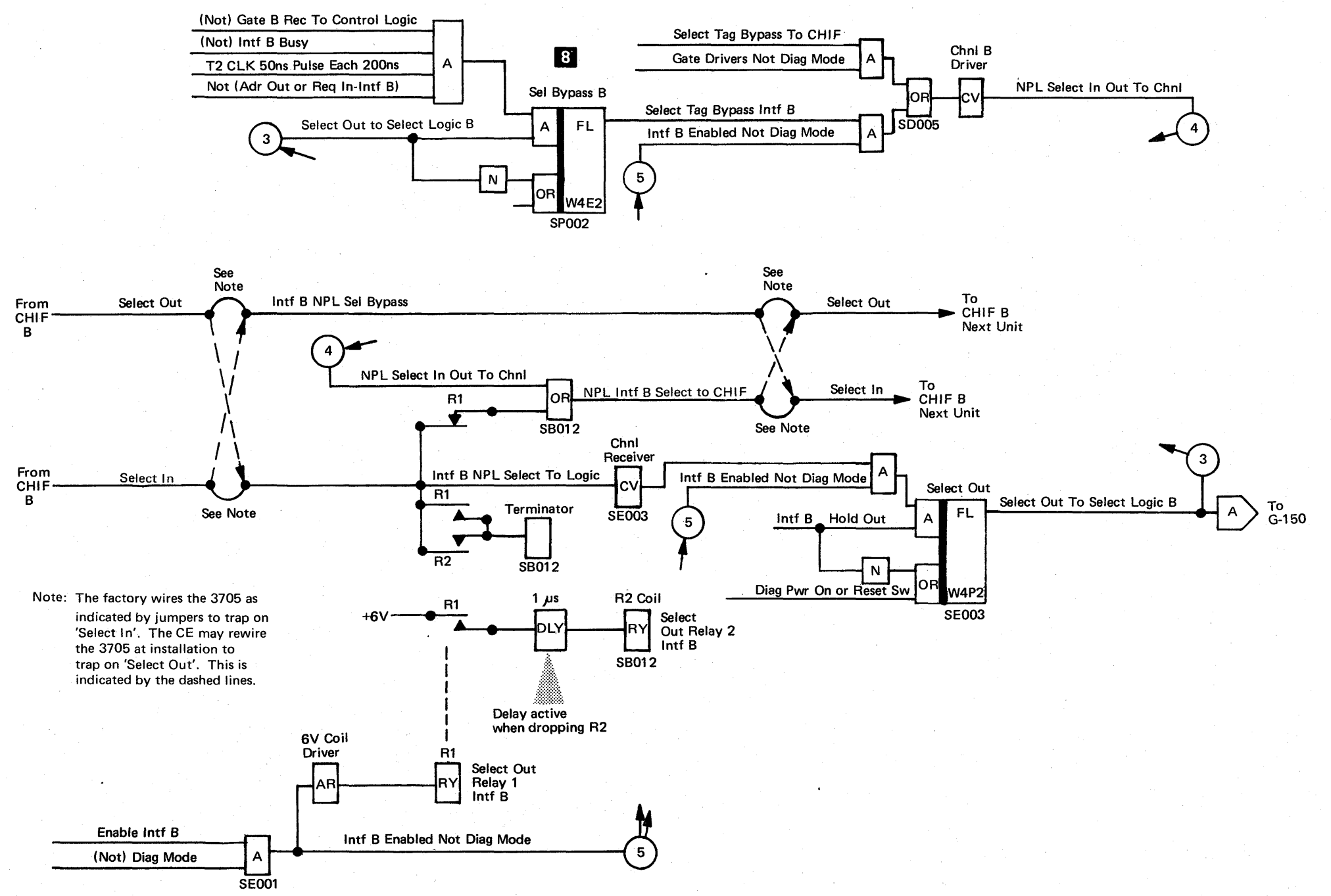
When the channel adapter switches allegiance to interface A, the common logic OP In signal resets 'request in tag to CHIF' which drops Request In tag from both interfaces. The 'select out to select logic B' signal now sets the 'sel bypass B' latch. **8** (G-160). This propogates the 'select in out to chnl' signal to the next unit on the channel B interface.

If the 3705 control program initiates an asynchronous Attention while a tagged Device End is pending for either interface A or B, the channel adapter presents the combined Attention-Device End status if the channel to which the Device End is tagged raises Select Out first.



ASYNCHRONOUS ATTENTION STATUS, PART 2

1. Intf B Switch	SP002	36
2. Intf In Not Switch State	SP002	1,18 18 1,18
3. Op Out A (common)	SF006	Intf B Intf A/B Intf A Intf A/B
4. CA L3 Interrupt (common)	SJ001	
5. Attention LT (common)	SK001	ATT Req and 31 23,31
6. Status Available (common)	SK002	4,5 5
7. Initiate Service Cycle (common)	SF002	6 6
8. Request In Tag To CHIF (common)	SF002	3,7,25 25
9. Set Req In To Intf A and B	SP001	2,6,8 2
10. Force Req In A	SP001	9 9
11. Request In To Intf A	SP001	4,10 10
12. Force Req In B	SP002	9 9
13. Request In To Intf B	SP002	4,12 12
14. Hold Out/Select Out (Intf A)	SC003	29 31
15. Select Out To Select Logic A	SC003	14 14 14
16. Hold Out/Select Out (Intf B)	SE003	Chnl B
17. Select Out To Select Logic B	SE003	Sel In Out To Chnl B 16 16
18. Intf A Switch	SP001	11,15 36
19. Instan Allegiance Intf A	SP001	18 18
20. Select Out A (common)	SF006	15,18 Intf A 15
21. Set Trap Sel Out LT (common)	SF002	8,20 8
22. Trap Sel Out LT (common)	SF002	T2,21 20
23. Clock runs (common)	SF001	22 30 34
24. Op In Ctrl (common)	SF002	22 23,31
25. Op In (common)	SF002	CLK 1,24 20,24
26. (Op In To Cmd Out) (common)	SP003	25 30
27. Async Status Switch (common)	SP003	6,26 25,31
28. Sel Bypass B	SP002	13,17 17
29. Address In Tag (Intf A)	SB004	Tag Dly Gate,24 23
30. Command Out (Intf A)	SC004	29
31. Status In LT (common)	SF003	Intf B Proceed,6,30 Intf A 23
32. Bus In To CHIF A	SB001	Address Attn Bit 0 5
33. Status In Tag (Intf A)	SB005	Tag Dly Gate,31
34. Service Out (Intf A)	SQ002	31
35. Assemble DE ATT Rst (common)	SP003	Not Long Alleg,27 2
36. Reset Intf LT (common)	SP003	2 35 2



SYSTEM RESET

When the channel gives a system reset (Operational Out drops when Suppress Out is down), the type 3 CA may be in one of three states: switched to interface A, switched to interface B, or the not-switched state. The flowchart summarizes the action the channel adapter takes for each state if the channel attached to interface A gives a system reset. The operation for a system reset from the channel attached to interface B is identical.

Channel Adapter Switched To Interface A

A system reset to interface A activates 'intf A sys reset' **1** as well as 'system reset'. **2** These lines reset the channel adapter except for those interface B latches that are reset by 'intf B sys reset'. When the channel removes the system reset, the 'sel sys reset' latch **3** picks causing a level 3 interrupt request and resets the 'intf A switch' latch to return the channel adapter to a not-switched state.

Channel Adapter Switched To Interface B

A system reset to interface A when the channel adapter is switched to interface B activates 'intf A sys reset'. **1** This resets the pending Device End that is tagged for interface A.

Channel Adapter In The Not-Switched State

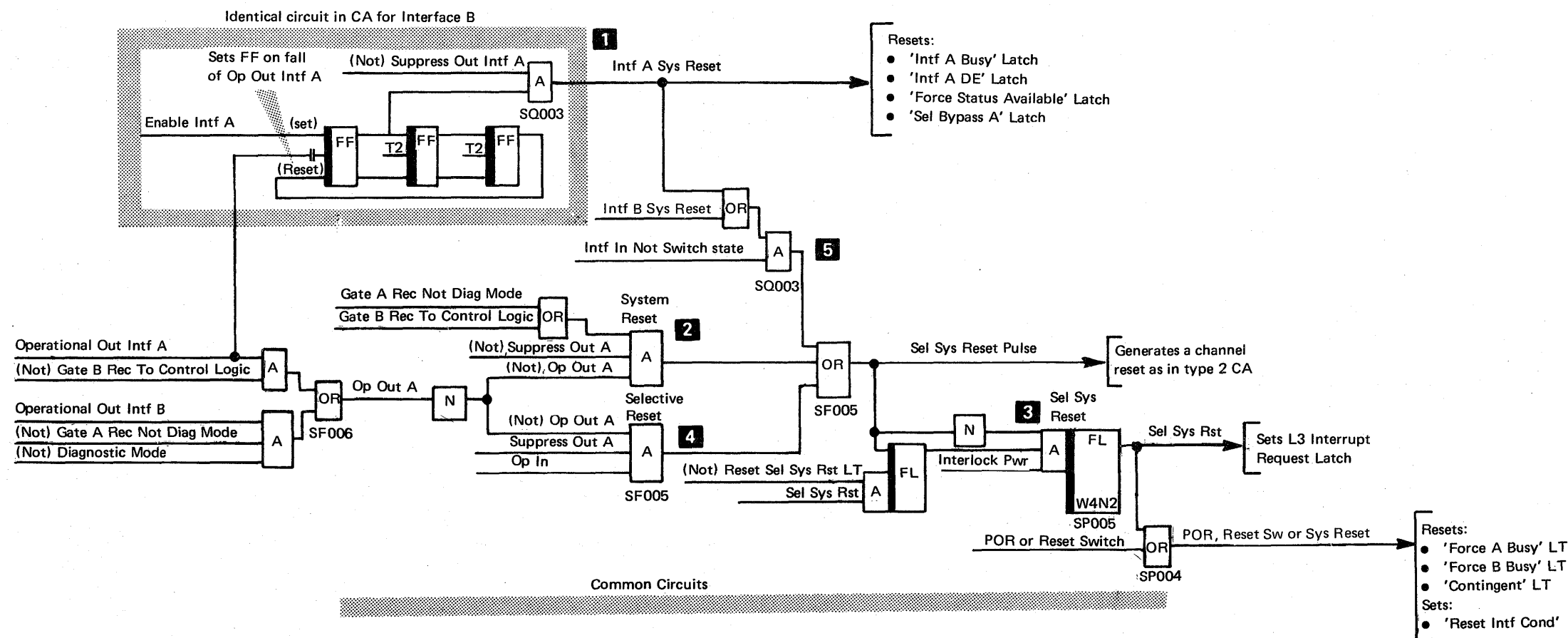
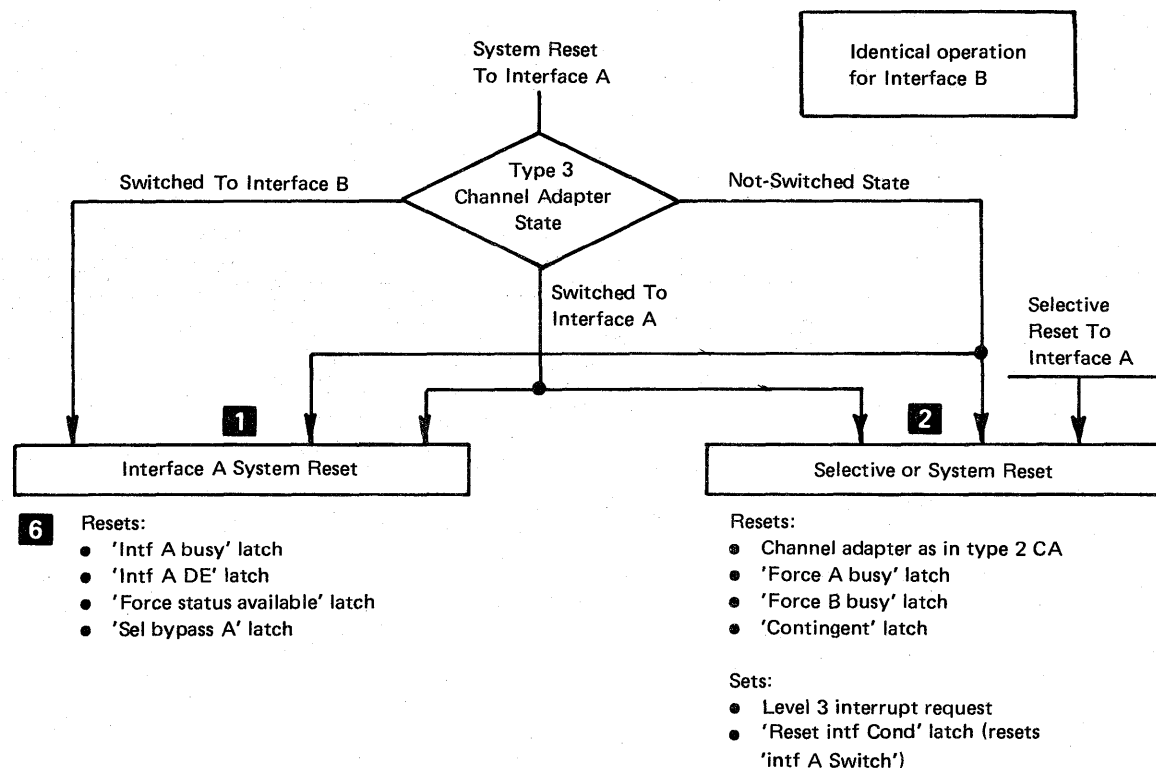
Since there can not be any outstanding command, the only interface activity reset by a system reset to interface A is:

- A pending Attention or Device End status that is not tagged for interface A.
- A pending Device End (due to a previous device Busy) tagged for interface A. **6** A pending Device end (due to a previous device Busy) for interface B is not reset.

The system reset activates 'intf A sys reset' **1** which activates 'sel sys reset pulse' by means of 'intf in not switch state'. **5** When the channel removes the system reset, the 'sel sys reset' latch **3** causes a level 3 interrupt request.

SELECTIVE RESET

The channel adapter recognizes a selective reset (Operational Out drops when Suppress Out is up) when 'op in' is active. **4** This activates 'sel sys reset pulse' giving the same resets that the system reset did.



TYPE 4 CHANNEL ADAPTER

INTRODUCTION

The type 4 channel adapter (CA) provides improved throughput over the type 1 CA when operating with a type 3 scanner. The type 4 CA is a type 1 CA that has been modified to operate in EB (extended buffer) mode and CS (cycle steal) mode as well as in the type 1 CA mode (non-EB mode). Since the type 4 CA is a modified type 1 CA, the description of the type 1 CA in Section 8 is applicable to the type 4 CA and is not repeated in this section. This section covers the differences between the type 4 CA and the type 1 CA.

EP/NCP Burst Size Options

The emulation program user chooses, through an EP generation option, the number of bytes of data the EP is to pass to the channel adapter each time the appropriate type 4 CA level 3 interrupt occurs. The user has a choice of 4, 8, 16, or 32 bytes that determines the buffer size within the EP.

NCP-5 has no generation option to control the amount of data passed to the channel adapter; it always transfers four bytes or less in non-EB/CS mode. The maximum cycle steal transfer for ACF/NCP/VS will be the sysgened buffer size. See the NCP sysgen manual GC30-3008 for buffer-size options.

Main Differences Between Type 4 CA and Type 1 CA

- **EB mode**
The type 4 CA uses a separate 9 X 32 EB local-store data-buffer array for EB inbound and outbound data transfers.
When in EB mode, the type 4 CA can transfer a maximum of 32 bytes of data across the channel during each data transfer burst with program intervention required only before and after each burst.
Good parity is not set into the EB local store by a power-on reset or the RESET pushbutton. The 3705 control program must assure good parity is set in the EB local store before it is accessed.
EB mode is reset by a power-on reset, the RESET pushbutton, a CA diagnostic reset, a system reset, an Output X'62' with bit 0.7-1, an Output X'6C' with bit 0.0=0, or when the not-initialized state is entered. It is *not* reset by a selective reset.
- **CS mode**
When in cycle steal mode, the first two bytes (addresses 0 and 1) of the 9 X 32 EB local-store data-buffer array are used as the cycle-steal buffer register for CS inbound and outbound data transfers.
When in CS mode, the type 4 CA can transfer a maximum of 256 bytes of data across the channel during each data transfer burst with program intervention required only before and after each burst.
EB and CS modes are mutually exclusive. An Output X'6C' with bits 0.0 (EB mode) and 0.1 (CS mode) on will default to EB mode.
- **Expanded BSC Control Character Recognition**
The type 4 CA, when in EB or CS mode and the ESC (emulator subchannel) mode is enabled, recognizes the following BSC control characters when they are in the inbound data stream from the host CPU:
 - ETB and ETX-CA stops the inbound data transfer and requests a level 3 interrupt.
 - DLE-STX sequence-CA stops monitoring the transparent data.

- **SYN**—when the CA detects (n)* consecutive SYN characters, the CA stops the inbound data transfer and requests a level 3 interrupt.
- **Non-EB/CS mode**
The type 4 CA uses the same 4 X 18 non-EB/CS local store array as the type 1 CA. The type 4 CA uses it for non-EB inbound/outbound-data transfers and for Address In and emulator subchannel Status In presentation to the channel.
- **Initial Selection 'short control unit busy' status**
Any start I/O to the ESC address when the type 4 CA has disconnected from the channel because of the 4, 8, or 16 byte burst jumpering receives a Status In of X'70' (control unit busy). See H-220 or H-270.
- **Multiple Type 4 CAs**
When multiple type 4 CAs are installed in a 3705, they share the same input/output codes so the 3705 control program must select the desired CA. See Output X'67' on page H-120.
- **Automatic selection between multiple type 4 CAs by level 3 interrupt priority**
The priority selection circuits in each CA assign a priority level to each type 4 CA level 3 interrupt, compare the priorities in the multiple CAs, and then select the CA with the highest priority for servicing. The 3705 control program has control over when to 'prime' this priority select circuit and when the CA selection is made (see H-230).
- **IPL and ROS implementation**
 - One type 4 CA
Uses the type 1 CA ROS and IPL sequencing.
 - Type 4 CA installed with either a type 2 CA or a type 3 CA
Uses the Dual ROS and IPL sequencing.
 - Two type 4 CAs with an IPL source switch use the type 1 CA ROS. The two type 4 CAs can be attached to the same or different host processors. An IPL source switch on the control panel (see E-040 configuration **2** or **7**) allows either, but never both, type 4 CAs to accept an IPL command over its NSC (native subchannel) address. The type 4 CA not selected by the IPL source switch cannot recognize its NSC address and passes Select Out if the host CPU executes a start I/O command for its NSC address (SIO ends with condition code 3). The channel addresses of both native subchannels should be *outside* the emulator sub-channel address range (see PA050 for exceptions). The type 4 CA not selected will not recognize the I/O register addresses (input/output codes) except for the selection output (see Output X'67' on H-120), the L3 priority sequence, and the automatic 'program requested interrupt' function (see Output X'67' on H-120).
 - Multiple (2-4) Type 4 CAs without an IPL source switch.
Uses N-Channel ROS.
Any type 4 CA in a configuration containing two, three or four type 4-CAs can accept an IPL command. A special Sense command status is used to break contention if two or more CPUs simultaneously try to IPL the 3705.

* Value of (n) is determined by the 3705 control program.

An IPL attempt by a CPU must consist of a Sense command, command-chained to a Write IPL command. If an IPL is in progress from any type 4 CA when a CPU attempts an IPL, the 3705 N-channel ROS returns an ending status of 'CE, DE, UE' to the Sense command. The unit exception breaks the command chaining and the Write IPL command is not executed by the CPU channel. This CPU program enters a timeout period waiting for an asynchronous device-end from the 3705 to indicate that the IPL operation has been completed. If the asynchronous device-end does not occur prior to the timeout completion, this CPU program assumes the IPL in progress was not successful and executes a Write IPL command that is not chained from a Sense command.

When an IPL operation is successfully completed, the control program just loaded returns an asynchronous device-end to all channels attached to the 3705 except the channel over which the IPL occurred. This 'DE' signals the CPU programs associated with these channels that the 3705 has just completed the transition from a not-ready state to a ready state.

- **Remote Program Loader (RPL) 3705-II only**
From one to three type 4 CAs can be located in the 3705 with the RPL. See 2-000 for all combinations and E-030 for all board locations. The RPL requires a RPL ROS while the channel adapter combination, requires a different ROS as previously defined (IPL source switch installed). The RPL logic selects which ROS is loaded at IPL phase II time.

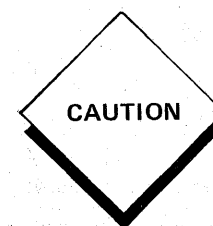
Enabling Type 4 CA NSC Address

Upon powering up, the type 4 CA that the IPL source switch selects will accept commands over its NSC address. If it is desired to enable the other type 4 CA's NSC address instead, the following steps must be performed:

1. Disable the line interfaces that are enabled.
2. Set the IPL switch to the channel position desired.
3. Press the RESET pushbutton, then the LOAD pushbutton.

The type 4 CA attached to the channel that the IPL source switch selected when the RESET and LOAD pushbutton were depressed will now accept commands over its NSC address.

Changing the IPL switch position without powering up or without following the above procedure has no effect on which type 4 CA will accept commands over its NSC address.



When operating with a type 1 or type 4 CA in an NCP (PEP included) environment, do not attempt to disable a channel interface unless the 3705 network has been quiesced or a system reset has occurred. If this procedure is not followed, the NCP may, while disabled, attempt to send asynchronous status which inhibits the CA1 or 4 from becoming enabled again.

Note: With N-Channel ROS all enabled type 4 CAs will accept commands over their NSC addresses.

Type 4 CA Configurations

Up to two type 4 CAs can be installed in a 3705-1; one in the basic frame and one in the first expansion frame. Up to four type 4 CAs can be installed in a 3705-II; one in the basic frame, the second in either the basic frame or the first expansion frame, and the third and fourth in the first expansion frame (see E-030). A type 4 CA can be combined with a type 2 or type 3 CA for operation in partitioned emulation mode. In this case, the Type 4 CA handles data transfers for lines in emulation mode and the type 2 or type 3 CA handles data transfers for lines in network control mode. Multiple type 4 CAs can be used in a PEP System with the enabled NSC(s) handling the NCP data transfers and the ESC addresses handling the EP data transfers. The channel adapters in a PEP system can be attached to the same or different CPUs. A type 4 CA cannot be combined with a type 1 CA or a type 1 Scanner.

Type 4 CAs can have a two-channel switch but whenever two channel adapters are located in the same frame, neither adapter can have a two-channel switch. Up to three type 4 CAs can be combined with the remote program loader.

The type 4 CA can be attached to a selector, byte multiplexer, or block multiplexer channel of a system/370 or to a byte multiplexer channel of a system/360.

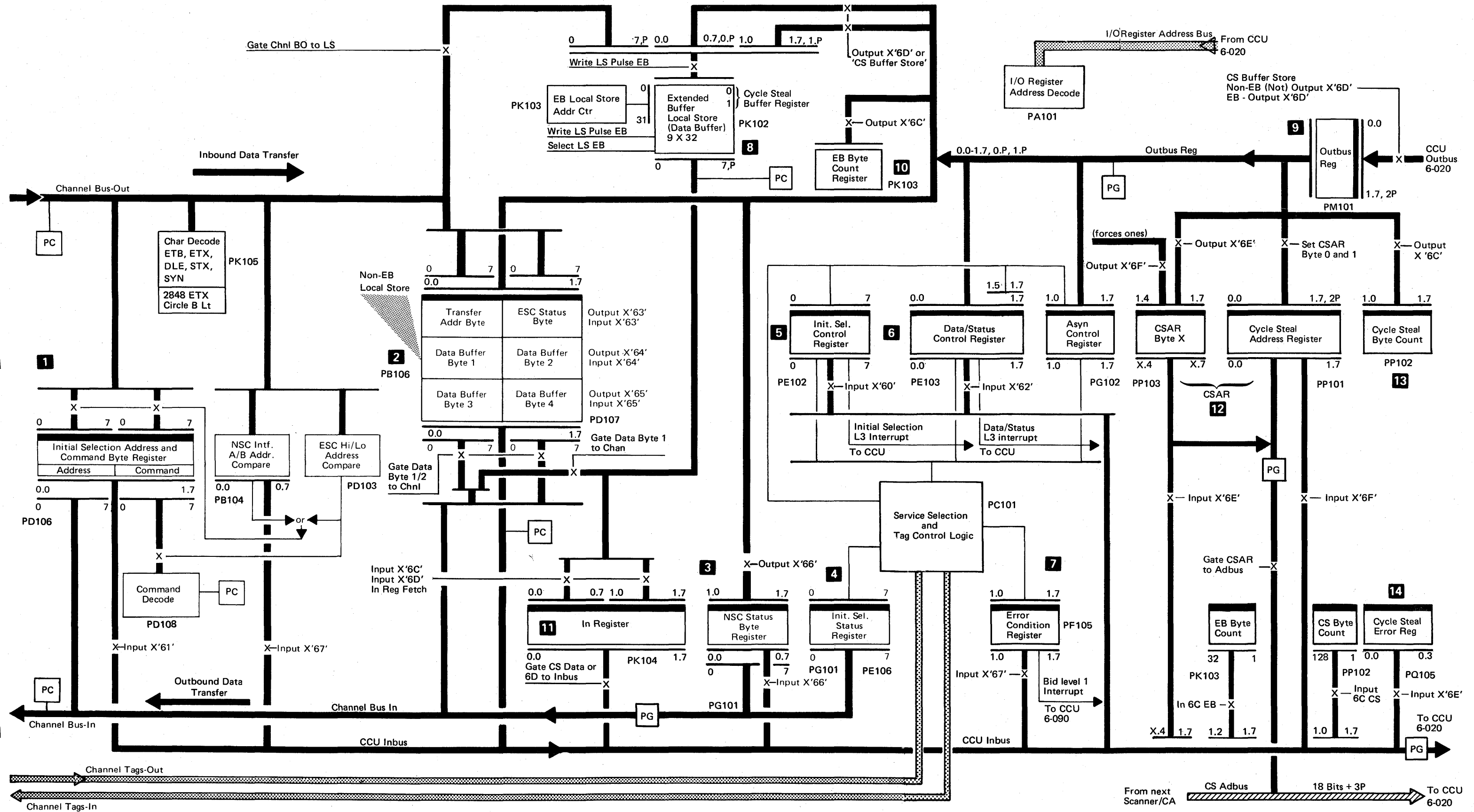
CE Burst Length Jumper Option

Depending on which CPU model the CA4 is attached to, the CE installs jumpers to select a burst size of 4, 8 or 16 bytes. If no jumpers are installed, the burst will be the byte count set up by the control program, up to 32 bytes in EB mode and up to 256 bytes in CS mode. If a burst size of 4, 8 or 16 bytes is chosen the CA4 will transfer the number of bytes specified by the plugging option, disconnect from the channel to allow other channel activity to occur then reconnect to transfer another burst of data. This disconnecting and reconnecting will continue until the full byte count has been transferred.

EXAMPLE: (Assume the CA4 is plugged for 8 byte burst length)

1. The control program sets up a 32 byte EB mode transfer.
2. The CA4 transfers 8 bytes, then disconnects from the channel interface.
3. The CA4 reconnects to the channel, transfers 8 more bytes, then disconnects.
4. Step 3 is repeated two more times.
5. The CA4 interrupts the control program indicating all 32 bytes have been transferred. The interrupt occurs only after the full byte count (32 in this example) has been transferred. The burst length jumpering option is transparent to the control program. The duration that the CA 4 will disconnect from the channel is also a plugging option see CA4 logic page PA049 for burst-length and duration of delay between bursts plugging information.

TYPE 4 CA DATA FLOW



TYPE 4 CA DATA FLOW (PART 2)

1 INITIAL SELECTION ADDRESS AND COMMAND REGISTER

This register contains the I/O device address byte and command byte presented to the channel adapter during initial selection. The register can be accessed by Input X'61' which should be executed only if the type 4 channel adapter initial or data/status level 3 interrupt request is set. See H-050 for Input X'61' description. This register is referred to as the SIO register in the ALD's.

2 LOCAL STORE (NON-EB MODE)

The local store provides buffering for the I/O address byte used in all data and status transfer sequences initiated by the 3705. Buffering for up to four bytes of data for inbound and outbound data transfers in non-EB mode is provided here also.

The control program loads or accesses the I/O device address and the emulation status byte with Output X'63' and Input X'63' respectively. The data bytes are transferred with X'64' or X'65' instructions, see chart below.

NON-EB MODE

Data Byte	Data Transfer	
	Out	In
1	X'64'	X'64'
2	X'64'	X'64'
3	X'65'	X'65'
4	X'65'	X'65'

3 NSC STATUS BYTE REGISTER

The current status of the NSC is maintained in this register and gated over the channel interface during NSC status transfer sequences. The control program should set the NSC status by executing an Output X'66' instruction. The control program has access to this register with the Input X'66' instruction.

4 INITIAL SELECTION STATUS REGISTER

The status byte is generated and presented to the channel from this register during initial selection sequences except under the following conditions.

- An initial selection sequence occurs for the native mode subchannel before the NSC status byte provided by the control program has been accepted. The NSC status byte from the NSC status register is presented instead of the hardware generated status.
- An initial selection sequence occurs for an emulation address when the control program has signaled that an ESC status transfer sequence is required and has signaled that ESC Test I/O status is available. The ESC status byte provided by the program is presented instead of hardware generated status.

5 INITIAL SELECTION CONTROL REGISTER

The information in this register identifies the event causing the type 4 channel adapter initial level 3 interrupt request to be set. The register can be accessed by Input X'60', which should be executed only if the interrupt request is set.

6 DATA/STATUS CONTROL REGISTER

The information in this register controls and identifies events that cause the type 4 channel adapter data/status level 3 interrupt request to be set. The register can be accessed by Input X'62', which should be executed only if the interrupt request is set. The control program can perform various control functions by setting or resetting bits in this register with an Output X'62' instruction. The instruction should be executed only when the control program is servicing a type 1 or 4 CA level 3 interrupt request.

7 ERROR/CONDITION REGISTER

The error/condition register is a collection of latches that are set when the CA detects an error or an occurrence of specific asynchronous conditions. The 3705 control program has access to this register with an Input X'67' instruction, (see page H-110). The errors indicated by the error/condition register cause type 4 CA error interrupts (see page H-380).

8 EXTENDED BUFFER LOCAL STORE

The extended buffer local store provides for buffering up to 32 bytes of data for inbound and outbound data transfers when in extended-buffer mode. The first two data bytes are transferred to the In register by an Input X'6C'. The Input X'6D' instruction transfers the two bytes in the In register to a CCU general register before loading the In register with the next two bytes from the EB local store. Sixteen Input X'6D' instructions are required to transfer the data in the entire extended buffer. All 32 bytes of data for an outbound data transfer are loaded into the EB local store, two per instruction, by Output X'6D' instructions.

9 OUTBUS REGISTER

The outbus register buffers two data bytes for loading into the EB local store. The even data byte is loaded from the outbus register to the EB local store, followed by the odd data byte to the next sequential EB local store address.

10 EB BYTE COUNT REGISTER

This register buffers the requested byte count (up to 32) for inbound or outbound data transfers when in EB mode.

11 EB IN REGISTER

This register receives the even, then odd, data bytes from the EB local store for transfer to the CCU.

12 CYCLE STEAL ADDRESS REGISTER

The byte X register and the cycle steal address register contain the address bits of the storage data buffer location for the first data byte to be transferred to or from storage by cycle stealing. The byte X register contains the four high order address bits and the cycle steal address register contains the 16 low order address bits. The two registers combined form the CSAR. The CCU updates CSAR to the next sequential half-word storage address at the completion of a cycle steal transfer.

13 CYCLE STEAL BYTE COUNT

This register buffers the requested CS byte count (up to 256 bytes) for inbound or outbound data transfers when in CS mode.

14 CYCLE STEAL ERROR REGISTER

This register is set by the following errors:

- CS outbus error—the type 4 CA sets this bit during a cycle steal operation when data from storage contains incorrect (even) parity.
- CS inbus error—the type 4 CA sets this bit when the CCU raises 'bad data' to signal that the CCU has received bad data (even parity) from the type 4 CA on a cycle-steal data transfer.
- CS address bus error—the type 4 CA sets this bit when the CCU raises 'SAR even parity' to signal that the CCU has received incorrect parity on the CS address bus.
- CS address exception—the type 4 CA sets this bit when the CCU raises 'address error' to signal that the CCU has received an address from the type 4 CA that is beyond the storage capacity of the 3705 or that points to a protected area of storage.

The type 4 CA requests a level 1 interrupt when any of these bits are set.

CARD FUNCTIONS AND LOCATIONS

Card Loc	ALD Page	Function
E4F2	PA101	I/O Decodes
	PA102	I/O Feedback-Level 1 Bid
	PA103	Basic Clocking
	PA104	Inbus Dot Byte 0
	PA105	Inbus Dot Byte 1
	PA106	Inbus Byte 0
	PA107	Inbus Byte 1
	PA108	Selected Latch and L3 Bids
E4P2	PB101	Channel Intf Tags and Controls
	PB102	Channel Intf A Receivers
	PB103	Interface A Control
	PB104	Channel Address Jumping and Channel Parity Check
	PB105	Non-EB/CS Local Store Byte 0 Assembler
	PB106	Non-EB/CS Local Store Byte 0
	PB107	Interface B Address
E4N2	PC101	Channel Tags Control and Tag Clock
	PC 102	Channel Tags Control-Start I/O, and Operational In
	PC103	Channel Tags Control and Tag In Latches
	PC104	Channel Tags Control-Stack, Chaining, Stop, or Halt I/O
	PC105	Channel Tags Control, Enable, and Selective System Reset
	PC106	Channel Tag Control Powering
E4M2	PD101	Channel Bus-Out Repower
	PD102	Low Address Jumpers
	PD103	Low Address Logic
	PD104	High Address Jumpers
	PD105	High Address Logic
	PD106	Start I/O Adr Reg and Command Reg
	PD107	Non-EB/CS Local Store Byte 1
	PD108	Command Decode
	PD109	CCU Outbus Inversion
	E4L2	PE101
PE102		Initial Selection Control
PE103		Service Transfer Control
PE104		Byte Transfer Count (Non-EB/CS)
PE105		Service Transfer
PE106		Initial Status Generation
PE107		OR Dots Byte 0
E4K2	PF101	Input/Output Control
	PF102	Assembler and Non-EB/CS Local Store Cntl
	PF103	NSC Control
E4T2	PG101	RN Asynchronous Information Error Latches
	PG102	NSC Status Register Asynchronous Interrupt Control
E4Q2	PH101	Intf A Bus-In Drivers Bits 0,1,2
	PH102	Intf A Bus-In Drivers Bits 3,4,5
	PH103	Intf A Bus-In Drivers Bits 6,7,P
	PH104	Intf A Tag-In Drivers Op In, Adr In, and Service In
PH105	PH105	Intf A Tag-In Drivers Sel In, Req In, and Status In
	PH106	Select Out Relay Driver and Control Gating
	PH107	Bus-In Error Latch and Reset Generation
E4T4	PJ101	Intf A Select Out Relays
	PJ102	Intf B Select Out Relays

*Y2 and Y3 cables are present on Models J-L, only.

To/From the CCU, Remote Program Loader, scanner, or other channel adapter.

To/From a scanner or other channel adapter.

Note: Internal board connections exist between this group of cables and corresponding groups above-i.e. Inbus lines connect to CCU Inbus lines.

Denotes the location of terminator cards for the last OXA-A4 board installed. See PA001.

The IPL SELECT switch cable attaches to the pin side of the Z2 connector on the O1A-E4 board. See PA060.

OXA-E4BOARD (Card Side)**

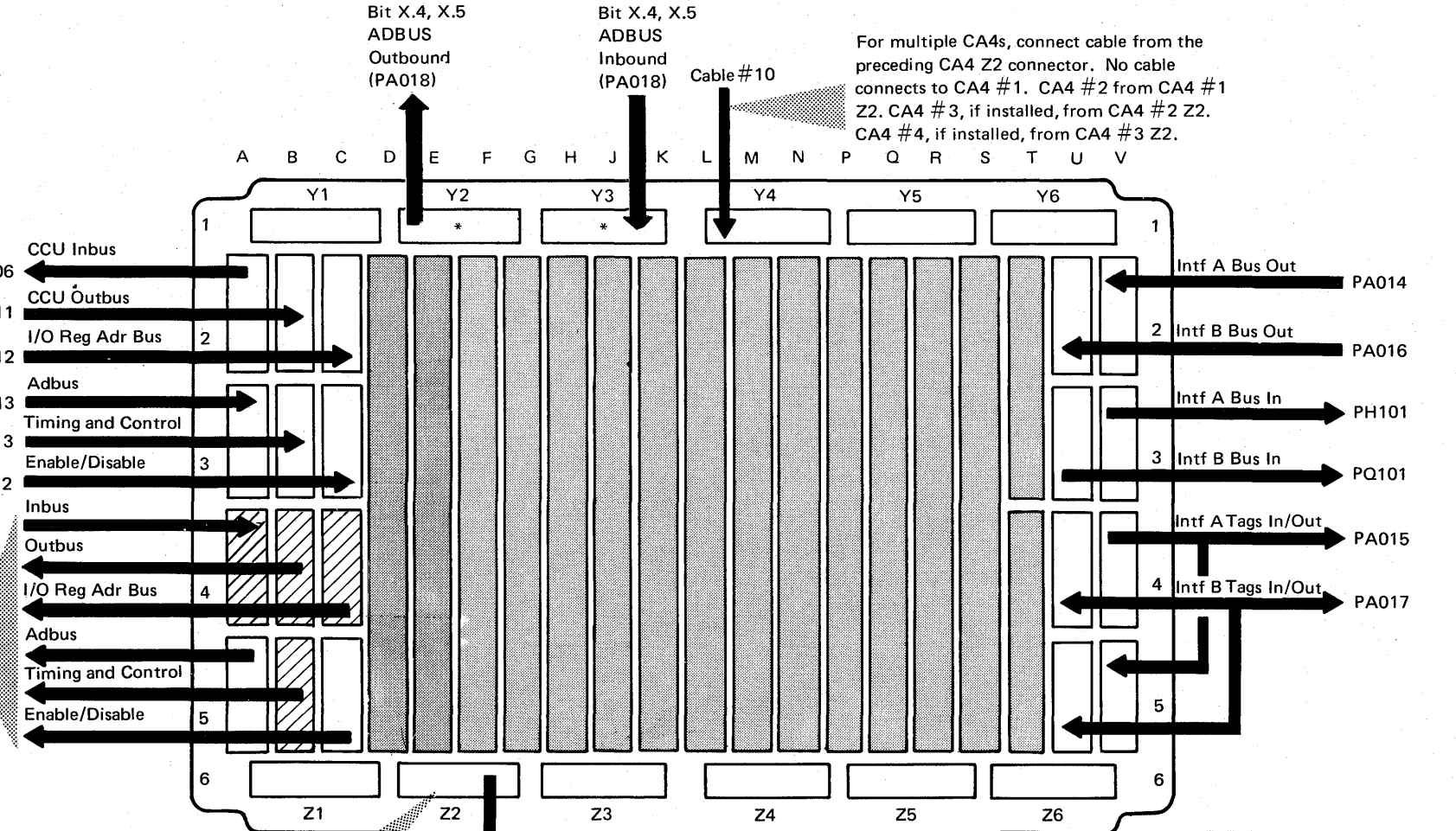
For multiple CA4s connect cable to the next CA4 Y4 connector. No cable comes from the last CA4. CA4 #1 to CA4 #2 Y4 connector. CA4 #2 to CA4 #3 Y4 connector, if installed. CA4 #3 to CA4 #4 Y4 connector, if installed. See PA060.

**E4 is the psuedo board location for the type 4 CA. The actual board location is OXA-A4, O1A-B1 or O2A-B4.

Card Loc	ALD Page	Function
E4J2	PK101	CCU Outbus Register Byte 0 and Channel Bus Out Repowering
	PK102	Extended Buffer Local Store and Assembler
	PK103	EB Local Store Address Counter and Count Control
	PK104	EB Local Store to Inbus
	PK105	BSC Control Character Recognition and Detect all zeros on CCU Outbus Byte 0
	PK106	Burst Length Jumping
	PK107	EB Local Store to Drivers
E4H2	PL101	BSC Character Recognition Control
	PL102	I/O Decodes and Extended Buffer Mode Lt
	PL103	Extended Buffer Controls
	PL104	Burst Length Controls and Force Short CU Busy
	PL105	Both Local Store Gate Controls and Local Store Cycle Reset

Card Loc	ALD Page	Function
E4G2	PM101	CCU Outbus Byte 1 Repower, Zero Detect, and Priority Sample Generation
	PM102	CA L3 Priority Determination and Gating
	PM103	Priority to next CA
	PM104	Priority Control Logic Repowering
E4D2	PP101	CS Address Register
	PP102	CS Counter and Count Compare
	PP103	CS Byte X and Adbus Gating
	PP104	CS Byte 0 and 1 Gating to Inbus
	PP105	Force 1 to Byte X and Repowering
	PP106	Initial Sel Rst Control and Svc Sel Rst Control
E4E2	PQ101	CS Sequencing Control
	PQ102	CS Buffer Control and Odd Byte Transfer Control
	PQ103	CS Decodes and Inbus Gating
	PQ104	CS Mode Latch Counter and Byte X Control
	PQ105	CS Check Latches
	PQ106	Repowering

Card Loc	ALD Page	Function
E4R2	PR101	Intf B Bus Out Receivers Bits 0-3
	PR102	Intf B Bus Out Receivers Bits 4-7
	PR103	Intf B Bus Out Rcvr Bit P and Tags Out Rcvr Op Out, Select Out
	PR104	Intf B Tags Out Rcvr Adr Out, Cmd Out, Svc Out, and Supp Out
	PR105	Enable B Latch
	PR106	Intf B NSC Address Valid
E4S2	PS101	Intf B Bus-In Drivers Bits 0,1,2
	PS102	Intf B Bus-In Drivers Bits 3,4,5
	PS103	Intf B Bus-In Drivers Bits 6,7,P
	PS104	Intf B Tag-In Drivers Op In, Adr In and Service In
	PS105	Intf B Tag-In Drivers Sel In, Req In, and Status In
	PS106	Select Out Relay Driver and Control Gating
PS107	Bus-In Error Latch and Reset Generation	



INPUT AND OUTPUT INSTRUCTIONS

The type 4 channel adapter relies on the 3705 control program to use input and output instructions to control data transfers. The control program initiates channel data and status transfers, and transfers data between the CA and the CCU with input and output instructions.

Each input or output instruction addresses an external register. The input instructions gate the external register to CCU general registers via the CCU Inbus. Output instructions gate CCU general registers to CA registers via the CCU Outbus. The 'I/O register address bus' is decoded in the type 4 CA.

Executing an Input or Output X'60', X'61', X'62', X'63', X'64', X'65', X'66', X'6C', X'6D', X'6E', or X'6F' when the CA is actively handling a data or status transfer sequence causes an in/out check to occur; see H-380.

CONTROL PANEL ACCESS TO CA REGISTERS

Type 4 CA registers X'60' through X'66' should be accessed from the control panel with Input or Output instructions only when either of the type 4 CA level 3 interrupts are pending.

To ensure that this interrupt remains pending, the 3705 should be in either Program Stop or Hard Stop mode before these instructions are executed from the control panel.

If these conditions are not met, the following occurs:

- If the type 4 CA is in the process of a data or status transfer sequence and an Input or Output X'60' through X'66' or X'6C' through X'6F' is initiated from the control panel, the type 4 CA hardware:
 - Causes a type 4 CA level 1 interrupt request.
 - Sets the type 4 CA In/Out instruction accept latch.
 - Gates X'0000' onto the CCU Inbus to be displayed in display B if the instruction is an Input.
 - Does not recognize Output instructions.
- If the type 4 CA is not transferring data or status and a type 4 CA level 3 interrupt request is not pending, one of the following occurs:
 - For Input X'60', X'61', or X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the CA is being selected by the host CPU channel, the CCU may sample invalid data from the type 4 CA. The data in display B should be considered invalid.
 - For Output X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the type 4 CA is being selected by the host CPU channel, a type 4 CA channel bus in check and a type 4 CA level 1 interrupt request may be set or a CPU data check may be detected at the host CPU.

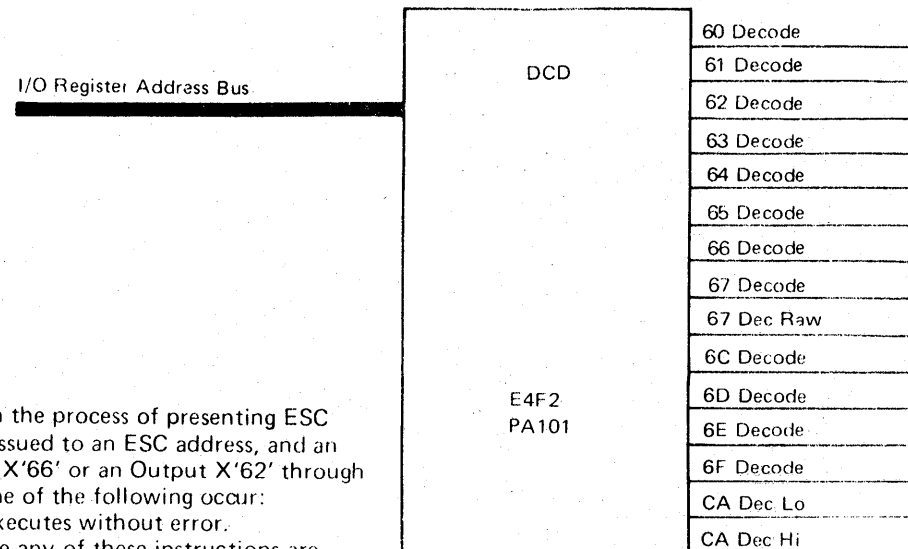
- If the type 4 CA is in the process of presenting ESC status to a Test I/O issued to an ESC address, and an Input X'60' through X'66' or an Output X'62' through X'66' is executed, one of the following occur:
 - The instruction executes without error.
 - If at the same time any of these instructions are being executed, the type 4 CA is being selected by the host CPU channel, either a type 4 channel bus in check, a type 4 CA local store, a level 1 interrupt request, or a CPU data check may occur.

Input and Output X'67' can be executed from the 3705 control panel without causing an error.

LOADING DATA INTO THE EXTENDED BUFFER FROM THE CONTROL PANEL

Simulate the following instructions from the control panel using the procedures on Page 1-160:

- Input X'6C'
Output X'6C' 8000 (data in ADDRESS/DATA switches A-E)
- Input X'6D'
Output X'6D' This steps the EB byte counter by 2.
- Output X'6D'
Output X'6D'
Output X'6D'
Output X'6D'
Output X'6D'
Input X'6C'
Input X'6D'
- Input X'6D'
Input X'6D'
- XXXXX (data in ADDRESS/DATA switches A-E). This data is loaded into EB LS data buffers 2 and 3. Repeat the Output X'6D' for each two data bytes desired. The data in the ADDRESS/DATA switches may be changed. *Do not* perform another Input X'6D' until you have loaded the number of bytes desired. The 31st and 32nd data bytes are loaded into EB LS data buffers 0 and 1 (the EB byte counter goes from 11111 to 00000). Resets EB byte counter. The first Input X'6D' transfers the 31st and 32nd data bytes loaded from the control panel to the inbus. The second Input X'6D' transfers the first two data bytes loaded. Consecutive Input X'6D's transfer the data bytes in the same sequence as they were loaded by consecutive Output X'6D's.



I/O Reg Bus Bits								Decode
0	1	2	3	4	5	6	7	
OP Reg Bits								
1.4	0.1	0.2	0.3	1.0	1.1	1.2	1.3	
X	1	1	0	0	0	0	0	60
X	1	1	0	0	0	0	1	61
X	1	1	0	0	0	1	0	62
X	1	1	0	0	0	1	1	63
X	1	1	0	0	1	0	0	64
X	1	1	0	0	1	0	1	65
X	1	1	0	0	1	1	0	66
X	1	1	0	0	1	1	1	67
X	1	1	0	1	1	0	0	6C
X	1	1	0	1	1	0	1	6D
X	1	1	0	1	1	1	0	6E
X	1	1	0	1	1	1	1	6F

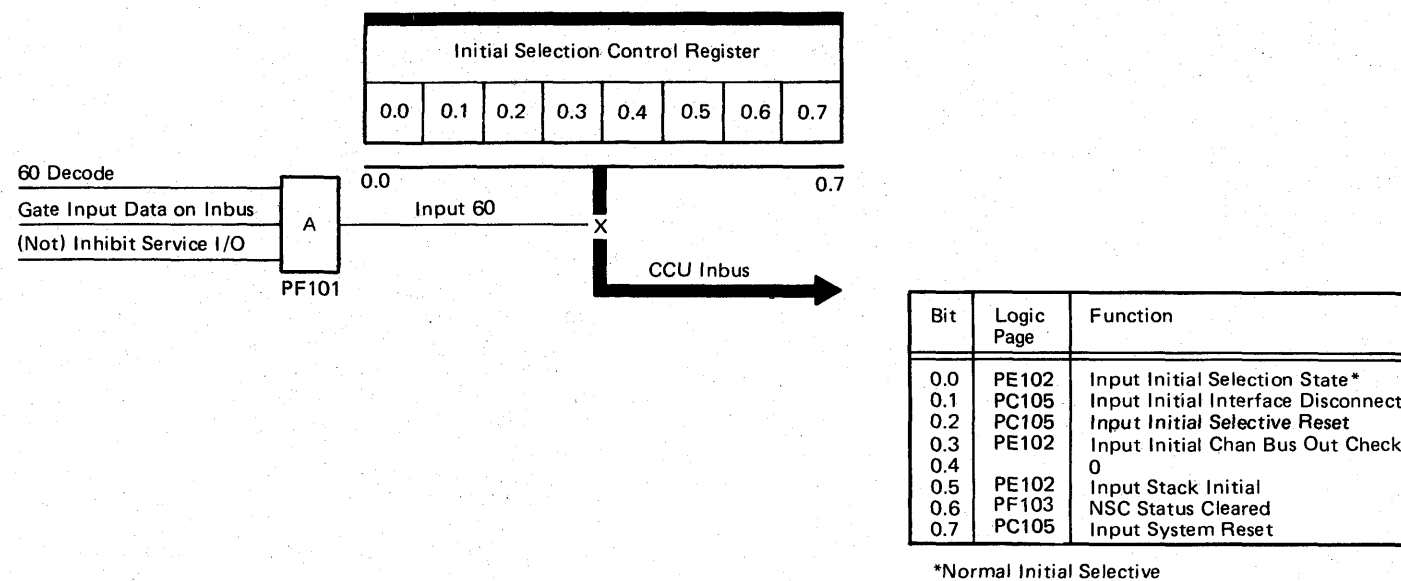
Op Reg bit 1.4: 1 for Input
0 for Output

INPUT X'60' INSTRUCTION

Input X'60' transfers the contents of the initial selection control register into a CCU general register. The 3705 control program uses this instruction to determine the exact cause of a type 4 CA initial selection level 3 interrupt.

An Output X'60' resets the initial selection control register and the L3 interrupt request resulting from the initial selection.

The type 4 CA and type 1 CA Input X'60' instructions are identical.



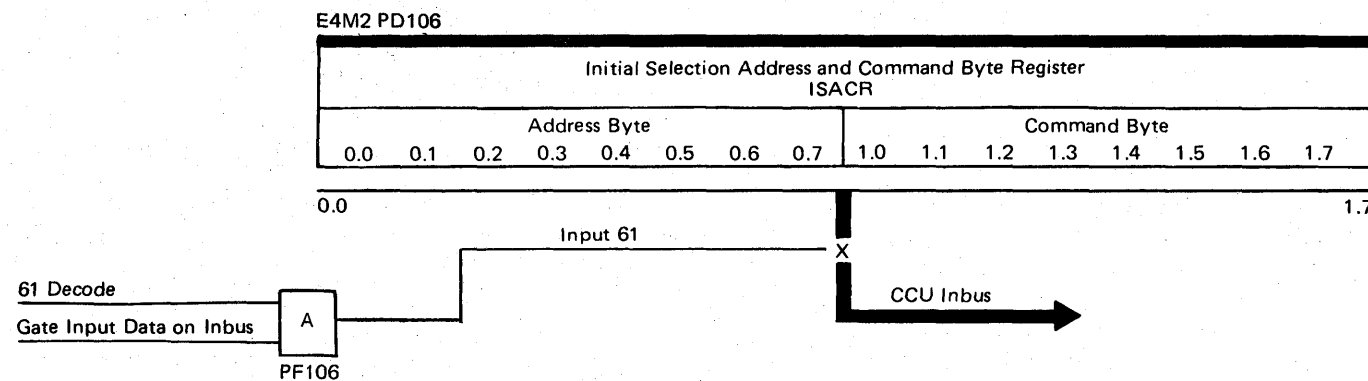
INPUT X'61' INSTRUCTION

Input X'61' transfers the contents of the initial selection address and command byte register into a CCU general register. During an initial selection sequence, a type 4 CA initial selection level 3 interrupt is requested, and the 3705 control program must investigate the subchannel address and command causing the interrupt. Byte 0 is the address to which the command in byte 1 was issued.

The 3705 control program must store the address and command because the host CPU can send the CA a new command before the 3705 control program has completed the previous one when in ESC mode. The 3705 control program must also control the CA action for each command.

An Output X'61' instruction has no effect on the channel adapter.

The type 4 CA and type 1 CA Input X'61' instructions are identical.



OUTPUT X'62' INSTRUCTION

This instruction initiates inbound and outbound data transfers and status presentations. The 3705 control program uses this instruction to control CA4 action and, when not in EB or CS mode, to specify the number of bytes of data to transfer across the channel interface on a channel data transfer.

Non-EB/CS Mode				EB or CS Mode		
Byte Count	1.5	Bits		SYN Chars	Bits	
		1.6	1.7		1.6	1.7
1	0	0	1	1	0	1
2	0	1	0	2	1	0
3	0	1	1	3	1	1
4	X	0	0	4	0	0

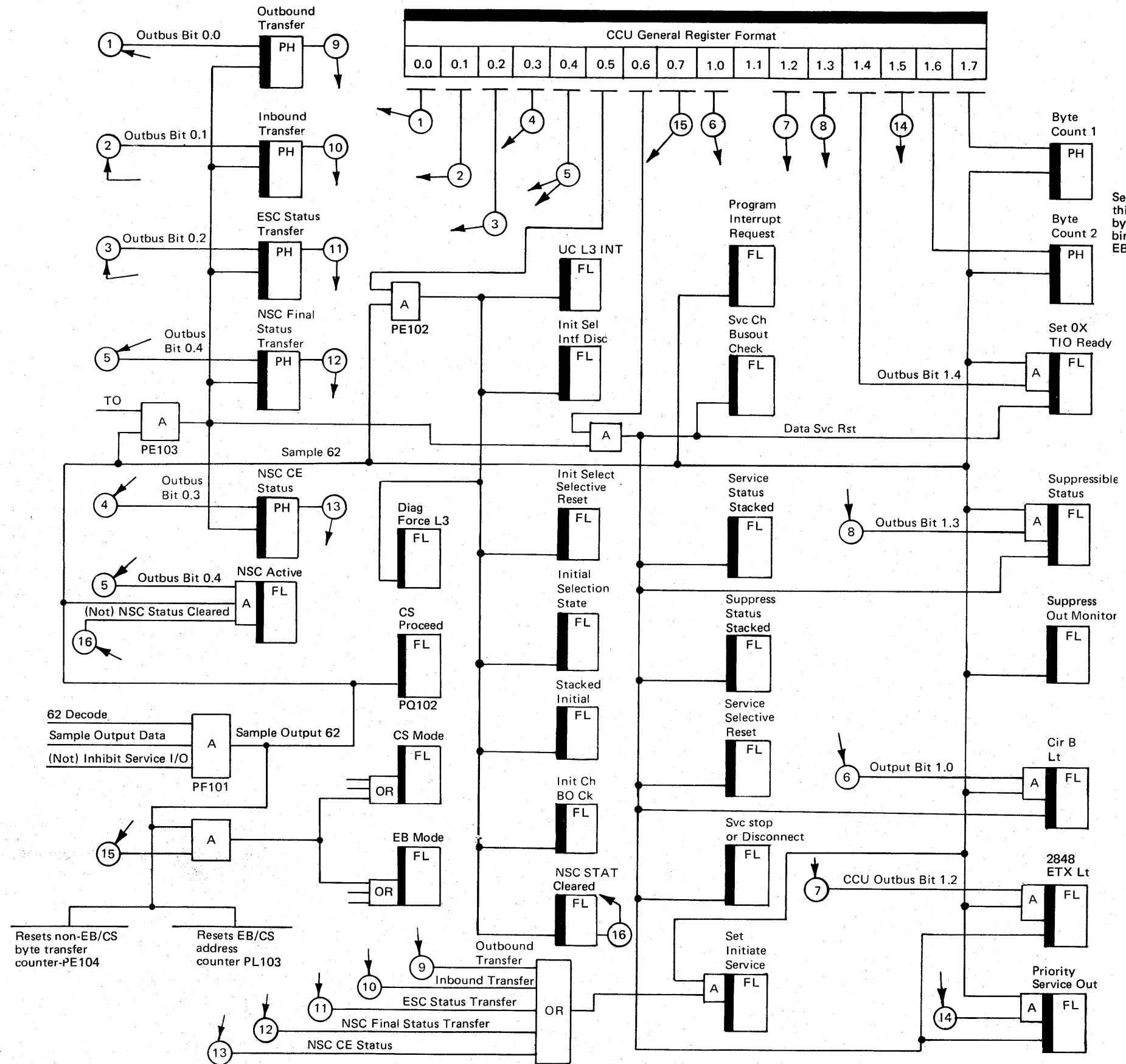
X This bit may be on or off for a byte count of four.

Summary of Output X'62' bit definitions and ALD locations

Bit	Card LOC	ALD Page	Function
0.0*	E4L2	PE103	1 = set; 0 = rst outbound transfer
0.1*	E4L2	PE103	1 = set; 0 = rst inbound transfer
0.2*	E4L2	PE103	1 = set; 0 = rst ESC status transfer
0.3*	E4L2	PE103	1 = set; 0 = rst NSC channel end status
0.4*	E4L2	PE103	1 = set; 0 = rst NSC final status transfer
	E4K2	PF103	Set NSC active
0.5	E4K2	PF103	Reset NSC status cleared
	E4G2	PM103	Reset force initial selection L3 interrupt
	E4L2	PE102	Reset initial channel bus out check
	E4L2	PE102	Reset stacked initial
	E4L2	PE102	Reset initial selection state
	E4N2	PC105	Reset Unit Check L3 interrupt
0.6	E4N2	PC105	Reset initial selection interface disconnect
	E4N2	PC105	Reset initial selection selective reset
	E4K2	PF104	Reset monitor for 2848 ETX
	E4K2	PF104	Reset monitor for circle B
	E4L2	PE106	Reset OX TIO ready
	E4L2	PE105	Reset service channel bus-out check
0.7	E4L2	PE105	Reset service status stack
	E4N2	PC104	Reset suppressible status
	E4N2	PC105	Reset service selective reset
	E4N2	PC105	Reset svc stop or disconnect
	E4N2	PC104	Reset suppress status stack
	E4N2	PC104	Reset suppress status stack
1.0	E4H2	PL102	Resets EB Mode
1.1	E4E2	PQ104	Resets CS Mode
1.2	E4K2	PF104	Set monitor for circle B
1.3	E4N2	PC104	Set suppressible status
1.4	E4L2	PE106	Set OX TIO ready
1.5	E4G2	PM102	Set Priority Outbound Data Xfer Seq
1.6	E4L2	PE104	Byte count 2
1.7	E4L2	PE104	Byte count 1

EB or CS Mode—number of SYN characters

*Any of these bits with 'Sample 62' set Initiate Service, E4L2, PE014



See the chart on this page for the byte count combinations for non-EB mode.

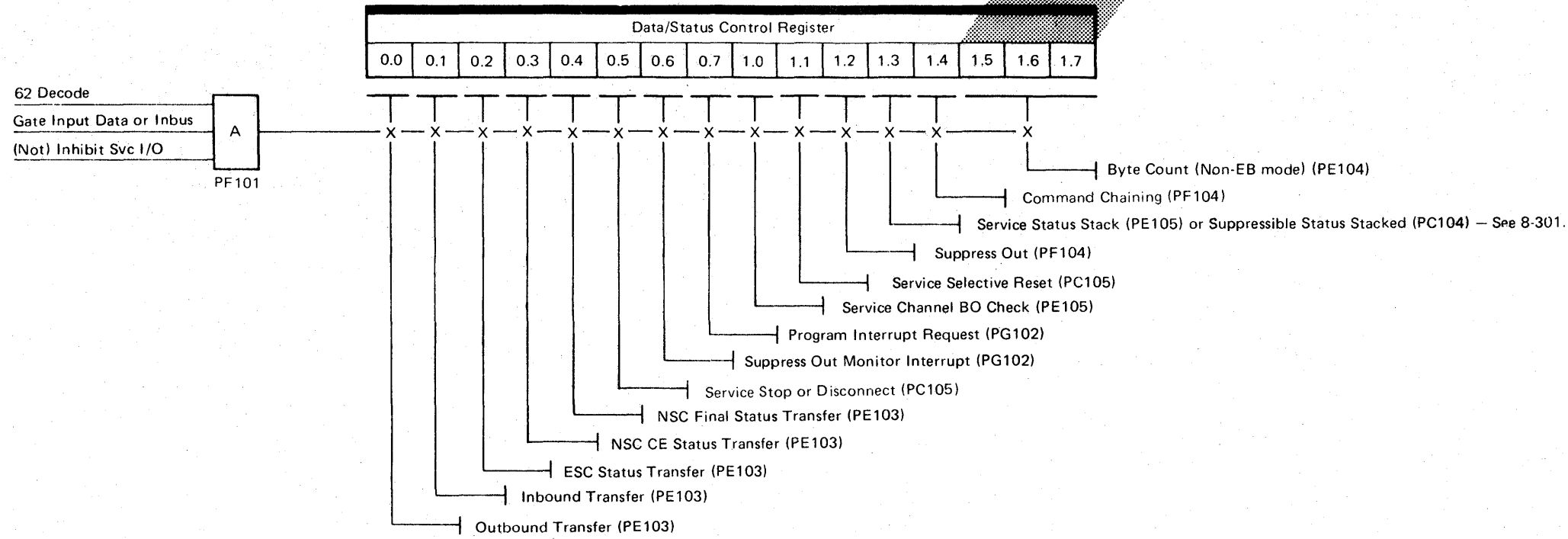
INPUT X'62' INSTRUCTION

This instruction transfers the contents of the data/status control register into a CCU general register. The 3705 control program uses this instruction to determine the exact cause of a type 4 CA data/status level 3 interrupt. The type 4 CA and type 1 CA Input X'62' instructions are identical.

Non-EB/CS mode

Count transferred to the CCU

Count	Bits		
	1.5	1.6	1.7
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0



OUTPUT AND INPUT X'63' INSTRUCTIONS

The 3705 control program uses the Output X'63' instruction to load the subchannel address (byte 0) and ESC status byte (byte 1) into the non-EB/CS local store buffer. The CA identifies itself to the channel by gating byte 0 onto the channel bus in, during the address transfer and gates byte 1 onto the channel bus-in to transfer the ESC status to the host CPU. (NSC address and status take a different path, see page 8-170.)

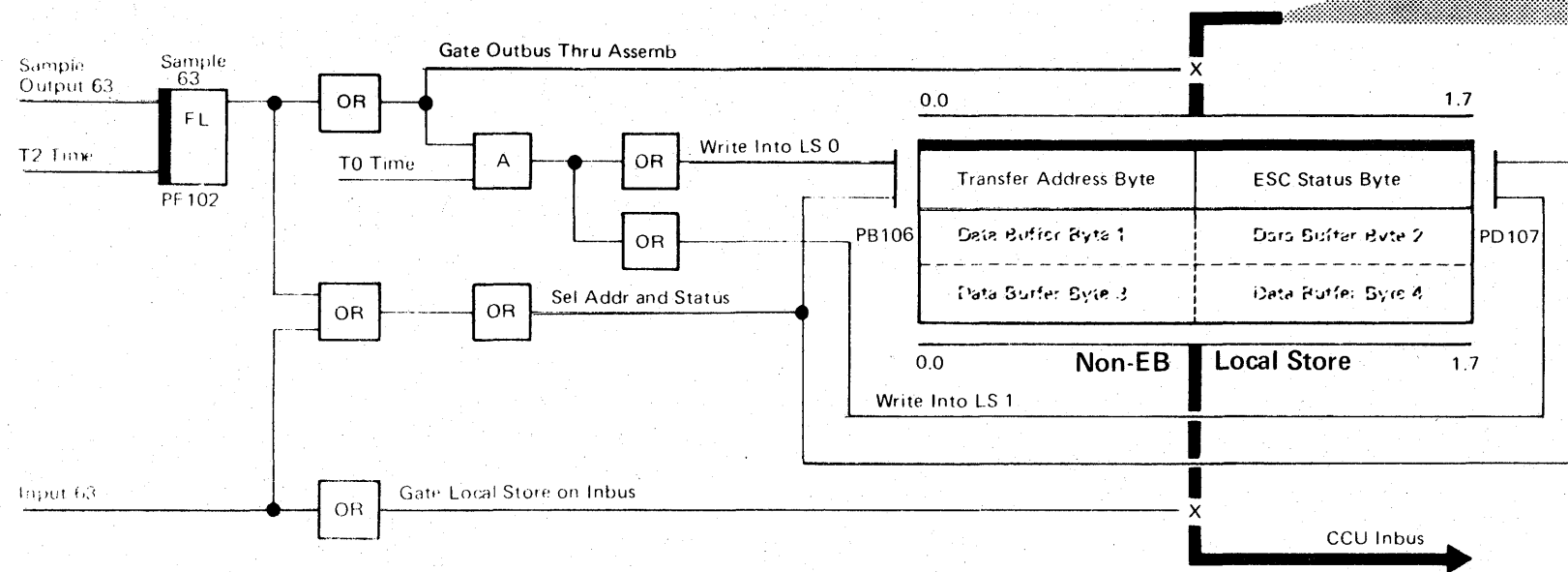
The 3705 control program must ensure that the correct address and status bytes are stored in the register. Otherwise, incorrect channel operation occurs.

With the Input X'63' instruction, the 3705 control program can determine the last subchannel address provided to the host CPU. The level 3 interrupt request latch should be set for this instruction to execute.

The type 4 CA and type 1 CA Output X'63' and Input X'63' instructions are identical.

CCU Outbus Bit Definitions

Bits	Definition
0.0-0.7	Subchannel address
1.0	Attention
1.1	Status modifier (SM)
1.2	Control unit end (CUE)
1.3	Busy
1.4	Channel end (CE)
1.5	Device end (DE)
1.6	Unit check (UC)
1.7	Unit exception (UE)



OUTPUT AND INPUT X'64' INSTRUCTION

1

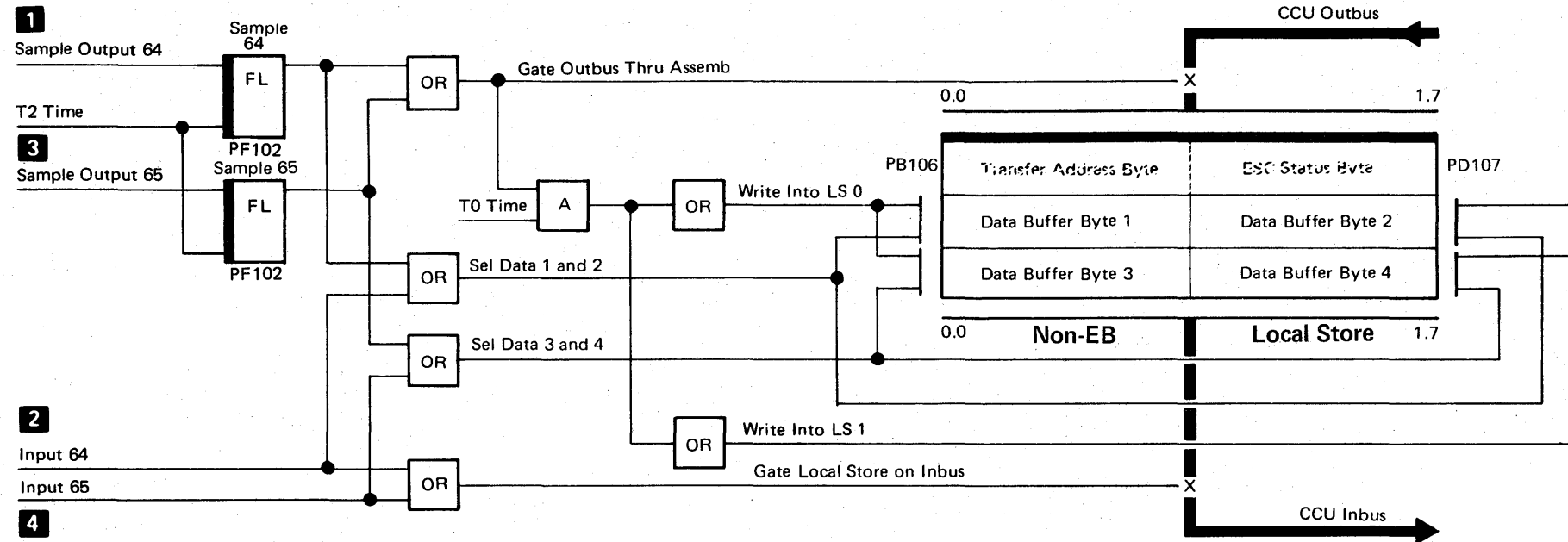
Output X'64' instruction loads non-EB/CS data buffer byte 1 and non-EB/CS data buffer byte 2 with the first two data bytes to be transferred across the channel to the CPU. These two data bytes are transferred to the CPU one byte at a time during an outbound data transfer.

The type 4 CA and type 1 CA Output X'64' instructions are identical.

2

Input X'64' transfers into a CCU general register the two data bytes that were received from the channel and stored in non-EB/CS data buffer byte 1 and non-EB/CS data buffer byte 2.

The type 4 CA and type 1 CA Input X'64' instructions are identical.



OUTPUT AND INPUT X'65' INSTRUCTION

3

Output X'65' instruction loads non-EB/CS data buffer byte 3 and non-EB/CS data buffer byte 4 with the second two bytes to be transferred across the channel to the CPU. These two data bytes are transferred to the CPU one byte at a time during an outbound data transfer.

The type 4 CA and type 1 CA Output X'65' instructions are identical.

4

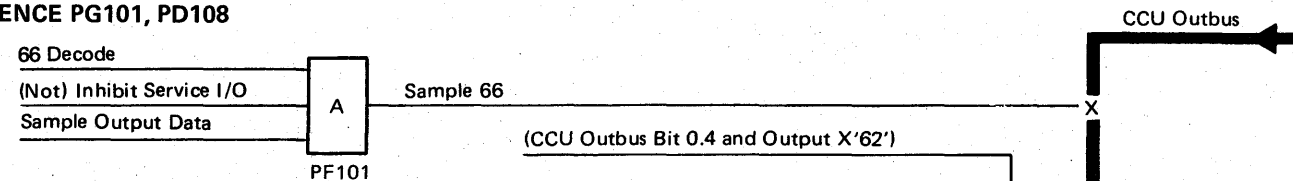
Input X'65' transfers into a CCU general register the two data bytes that were received from the channel and stored in non-EB/CS data buffer byte 3 and non-EB/CS data buffer byte 4.

The type 4 CA and type 1 CA Input X'65' instructions are identical.

OUTPUT X'66' INSTRUCTION

The Output X'66' instruction loads the final status byte to be presented to the channel into the NSC Status Byte Register. Output X'66' bit 0.4=1 sets NSC Long Busy. (See PF103).

LOGIC REFERENCE PG101, PD108

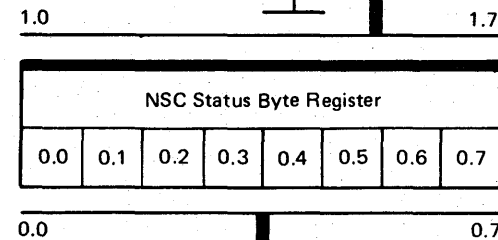
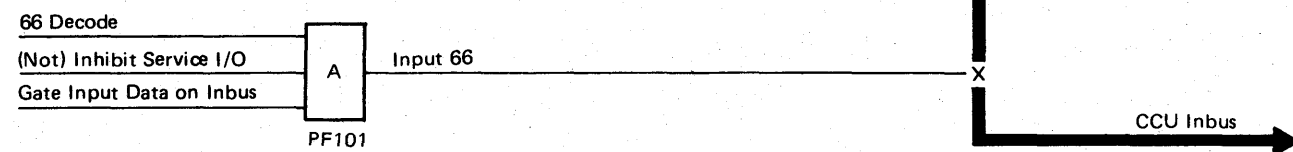


The type 4 CA and the type 1 CA Output X'66' instructions are identical.

INPUT X'66' INSTRUCTION

The Input X'66' instruction transfers the contents of the NSC status byte register into a CCU general register and forces byte 1, bits 0-7 to zeros. This instruction should be used only for diagnostic purposes and should not be used when the CA is on-line with an interface enabled.

The type 4 CA and type 1 CA Input X'66' instructions are identical.



NSC STATUS BYTE REGISTER BIT DEFINITIONS

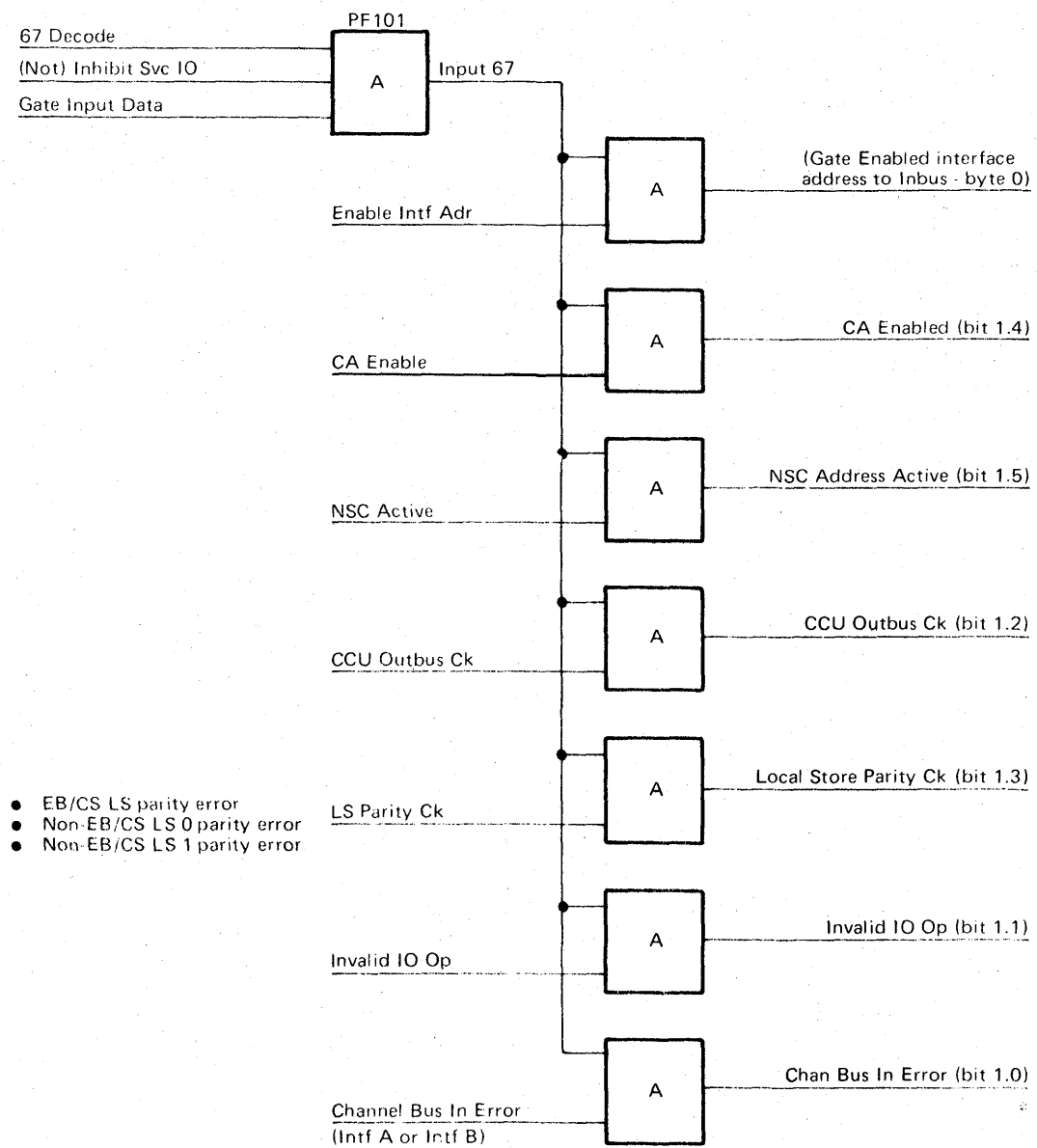
- Bit 0.0 – Attention
- Bit 0.1 – Status Modifier
- Bit 0.2 – 0
- Bit 0.3 – 0
- Bit 0.4 – Channel End (CE)
- Bit 0.5 – Device End (DE)
- Bit 0.6 – Unit Check (UC)
- Bit 0.7 – Unit Exception (UE)

INPUT X'67' INSTRUCTION

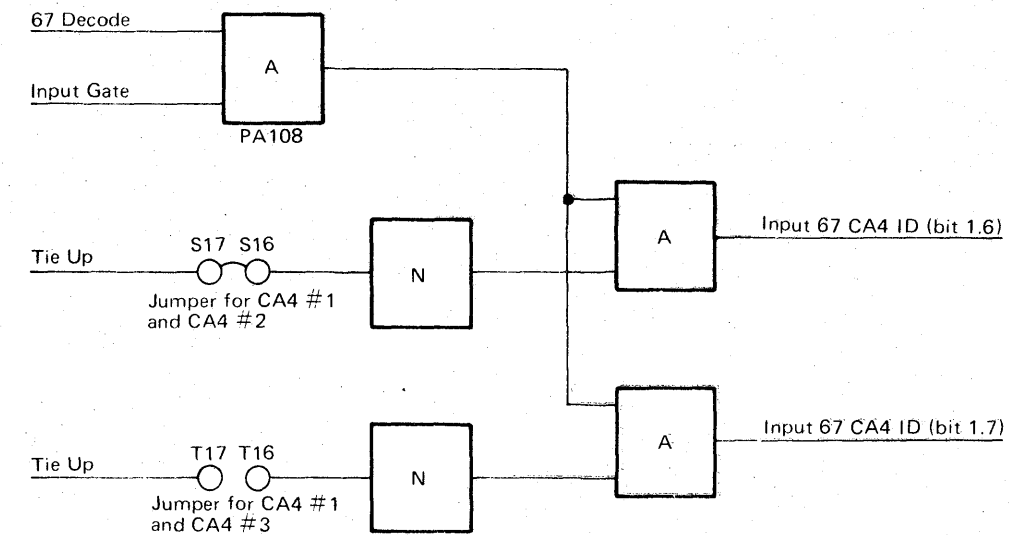
The Input X'67' transfers the error condition register (H-380) and the hardware address of the NSC channel interface address to the CCU.

Summary of Inbus bits during Input X'67':

Bit	Card Loc	Logic Page	Function
0.0.0.7	E4P2	PB104	NSC hardware address intf A
0.0.0.7	E4P2	PB107	NSC hardware address intf B
1.0	E4Q2	PH107	Chan bus in error
1.1	E4K2	PF105	Invalid I/O Op
1.2	E4K2	PF105	CCU outbus check
1.3	E4K2	PF105	Local store parity check
1.4	E4K2	PF104	CA enabled
1.5	E4K2	PF104	NSC address active
1.6-1.7	E4K2	PA108	00 - Type 4 CA #1 selected 01 - Type 4 CA #2 selected 10 - Type 4 CA #3 selected 11 - Type 4 CA #4 selected



- EB/CS LS parity error
- Non-EB/CS LS 0 parity error
- Non-EB/CS LS 1 parity error



OUTPUT X'67' INSTRUCTION

The Output X'67' instruction sets or resets the various control latches. The 3705 control program must execute an Output X'67' instruction to enable the CA interface before the CA can transfer data to or from the channel.

Selection Between Multiple Type 4 CAs

This instruction selects the CA4 specified by CCU outbus bits 0.5, 0.6, and 0.7 and resets the 'selected latch' on the CA4s not specified; therefore multiple CA4s cannot be selected at the same time. This instruction is then performed in the selected CA4. Outbus bit 0.5 must not be a one for subsequent Output X'67' instructions unless a non-selected CA4 is to be selected.

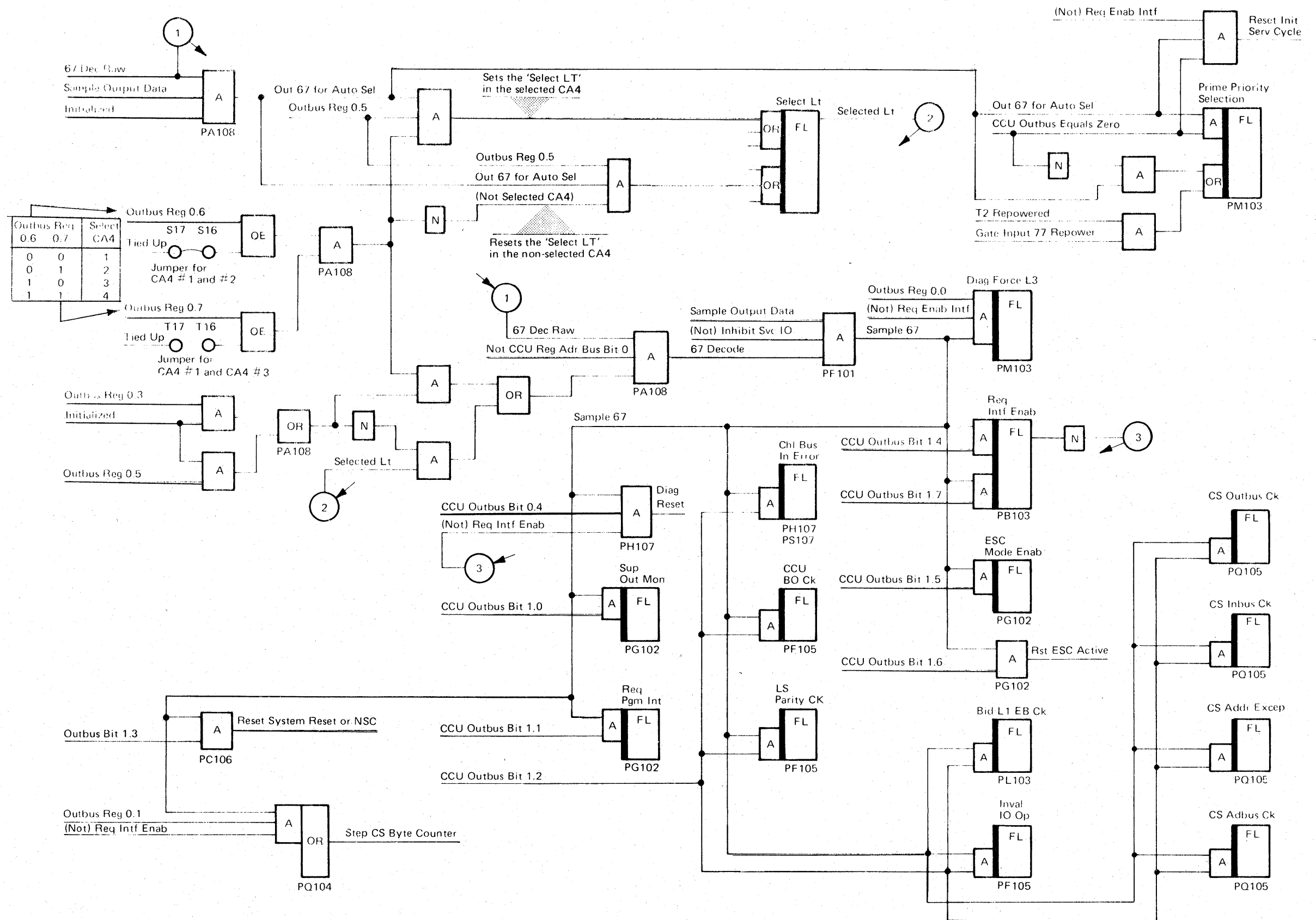
The control program can execute this instruction to a non-selected CA4 (bits 0.6, 0.7) by setting outbus bit 0.3 to one. The status of each CA4's 'selected latch' is not changed but the Output X'67' instruction is performed in the non-selected CA4 (to request a "program requested interrupt" for example). Bits 0.3 and 0.5 are mutually exclusive and both should never be on during the same output X'67' instruction.

Priming L3 Interrupt Priority Selection

An Output X'67' instruction, with all outbus bits zero, primes the CA4 priority selection circuit in the selected CA4 and forces a diagnostic data/status interrupt if appropriate.

Summary of Outbus bits during Output X'67'

Bit	Card Loc.	ALD Page	Function
0.0	E4G2	PM103	Diagnostic force initial selection interrupt
0.1	E4E2	PQ104	Diagnostic force byte transfer cycle steal mode
0.2			Not Used
0.3	E4F2	PA108	Perform Output X'67' on CA4 specified by bits 0.6 and 0.7
0.4	E402	PH107	Diagnostic reset
0.5	E4F2	PA108	0= Leave current CA4 selected 1= Select CA4 specified by bits 0.6 and 0.7
0.6, 0.7	E4F2	PA108	00 = Select CA4 #1 01 = Select CA4 #2 10 = Select CA4 #3 11 = Select CA4 #4
1.0	E4T2	PG102	Set suppress out monitor int
1.1	E412	PG102	Set request program interrupt
1.2	E4K2	PF105, PH107, PS107, PL103, PQ105, FQ105, PQ105, PQ105	Reset invalid I/O Op Reset local store parity check Reset CCU outbus check Reset channel bus in error (interface A) Reset channel bus in error (interface B) Reset bid level 1 EB check Reset CS outbus check Reset CS inbus check Reset CS address exception Reset CS adbus check
1.3	E4N2	PC106	Reset 'system reset' or 'NSC'
1.4	E4P2	PB103	Request interface enable
1.5	E4T2	PG102	Set ESC mode enable
1.6	E412	PG102	Reset ESC active
1.7	E4P2	PG103	Reset interface enable



INPUT X'6C' INSTRUCTION

(Type 4 CA Extended Buffer/Cycle Steal Mode Control Register)

The Input X'6C' instruction transfers to a specified CCU general register the states of the 'extended buffer mode' latch, 'cycle steal mode' latch, 'character-monitor control' latches, 'DLE remember' latch, and the byte count of the data transferred in extended byte or cycle steal mode.

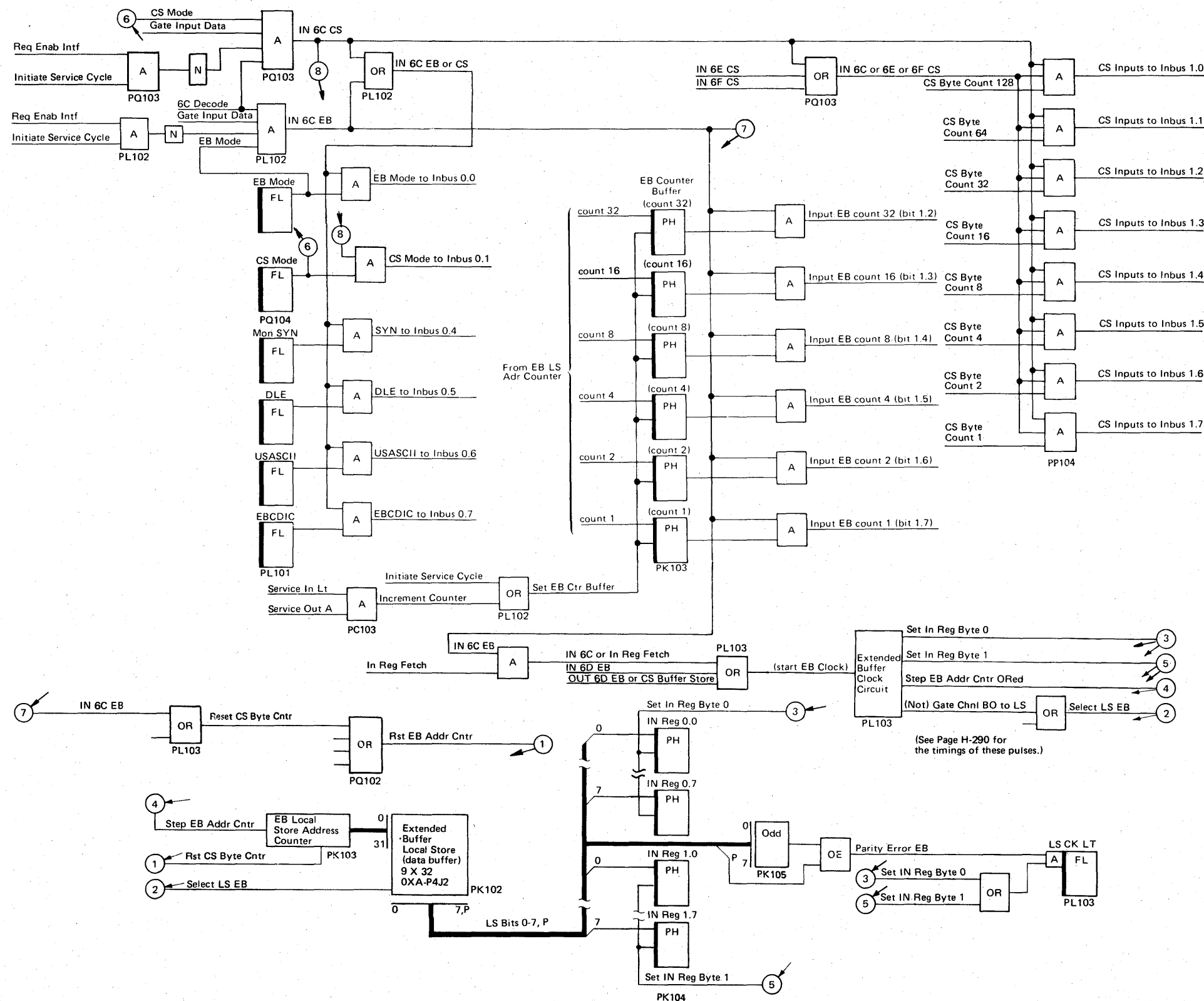
The Input X'6C' instruction resets the EB/CS local store address counter to address 0, then loads In register byte 0 with data byte 0 from EB/CS local store address 0. The 'step EB address counter' pulse advances the EB/CS local store address counter to 1 and then loads In register byte 1 with data byte 1 from that address. The EB/CS local store address counter then advances to address 2 so that the first Input X'6D' can continue loading the In register from sequential addresses. The data is buffered in the In register until the next Input X'6D' transfers it to a specified CCU general register.

Each byte of data from the EB/CS local store is parity checked and a parity error forces a level 1 interrupt.

Summary of CCU Inbus bits during Input X'6C'

Bit	Card Loc	ALD Page	Function
0.0	E4H2	PL102	Extended Buffer Mode
0.1	E4E2	PQ104	Cycle Steal Mode
0.2			0
0.3			0
0.4	E4H2	PL105	SYN monitor control latch
0.5	E4H2	PL101	DLE remember latch
0.6	E4H2	PL101	USASCII monitor control latch
0.7	E4H2	PL101	EBCDIC monitor control latch
1.0			0
1.1			0
1.2	E4J2	PK103	Transferred byte count-bit 32
1.3	E4J2	PK103	Transferred byte count-bit 16
1.4	E4J2	PK103	Transferred byte count-bit 8
1.5	E4J2	PK103	Transferred byte count-bit 4
1.6	E4J2	PK103	Transferred byte count-bit 2
1.7	E4J2	PK103	Transferred byte count-bit 1
1.0	E4D2	PP104	Transferred byte count-bit 128
1.1	E4D2	PP104	Transferred byte count-bit 64
1.2	E4D2	PP104	Transferred byte count-bit 32
1.3	E4D2	PP104	Transferred byte count-bit 16
1.4	E4D2	PP104	Transferred byte count-bit 8
1.5	E4D2	PP104	Transferred byte count-bit 4
1.6	E4D2	PP104	Transferred byte count-bit 2
1.7	E4D2	PP104	Transferred byte count-bit 1

EB Mode
CS Mode
(All zeros = 256)



OUTPUT X'6C' INSTRUCTION

(Type 4 CA Extended Buffer/Cycle Steal Mode Control Register)

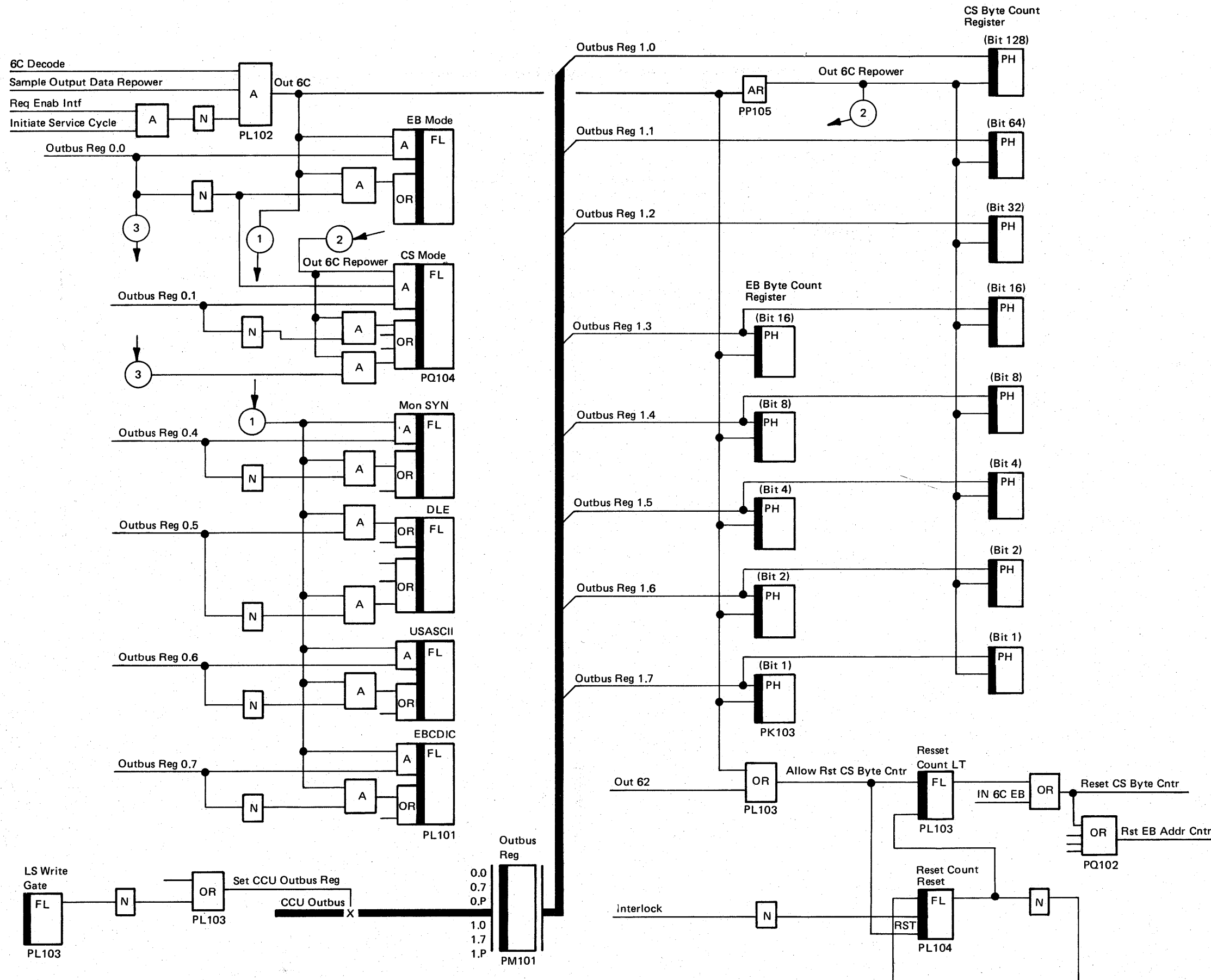
The Output X'6C' instruction sets or resets the 'EB mode' latch, the 'CS mode' latch, and various character-monitor or remember control latches. When outbus bit 0.0 is a one, the CA4 sets the 'EB mode' latch, inhibits any set of the 'CS mode' latch, and resets the 'CS mode' latch if it was on. This instruction also sets the EB and CS byte count registers with the number of bytes to be transferred during a data transfer and resets the EB local store address counter and CS byte counter to 0.

Summary of CCU Outbus bits during Output X'6C'

Bit	Card Loc	ALD Page	Function
0.0	E4H2	PL102	1 = Set, 0 = Reset-extended buffer mode
0.1	E4E2	PQ104	1 = Set, 0 = Reset-cycle steal mode
0.2			0
0.3			0
0.4	E4H2	PL105	1 = Set, 0 = Reset SYN monitor control latch
0.5	E4H2	PL101	1 = Set, 0 = Reset DLE remember latch
0.6	E4H2	PL101	1 = Set, 0 = Reset USASCII monitor control latch
0.7	E4H2	PL101	1 = Set, 0 = Reset EBCDIC monitor control latch
1.0			0
1.1			0
1.2			0
1.3	E4J2	PK103	Requested byte count-bit 16
1.4	E4J2	PK103	Requested byte count-bit 8
1.5	E4J2	PK103	Requested byte count-bit 4
1.6	E4J2	PK103	Requested byte count-bit 2
1.7	E4J2	PK103	Requested byte count-bit 1
1.0	E4D2	PP102	Requested byte count-bit 128
1.1	E4D2	PP102	Requested byte count-bit 64
1.2	E4D2	PP102	Requested byte count-bit 32
1.3	E4D2	PP102	Requested byte count-bit 16
1.4	E4D2	PP102	Requested byte count-bit 8
1.5	E4D2	PP102	Requested byte count-bit 4
1.6	E4D2	PP102	Requested byte count-bit 2
1.7	E4D2	PP102	Requested byte count-bit 1

EB Mode

CS Mode



INPUT X'6D' INSTRUCTION

(Type 4 CA Extended Buffer/Cycle Steal Mode Data Buffer Bytes)

The 3705 control program uses the Input X'6D' instruction to transfer data to a specified CCU general register from the In register and then to reload the In register with data from the EB/CS local store data buffer.

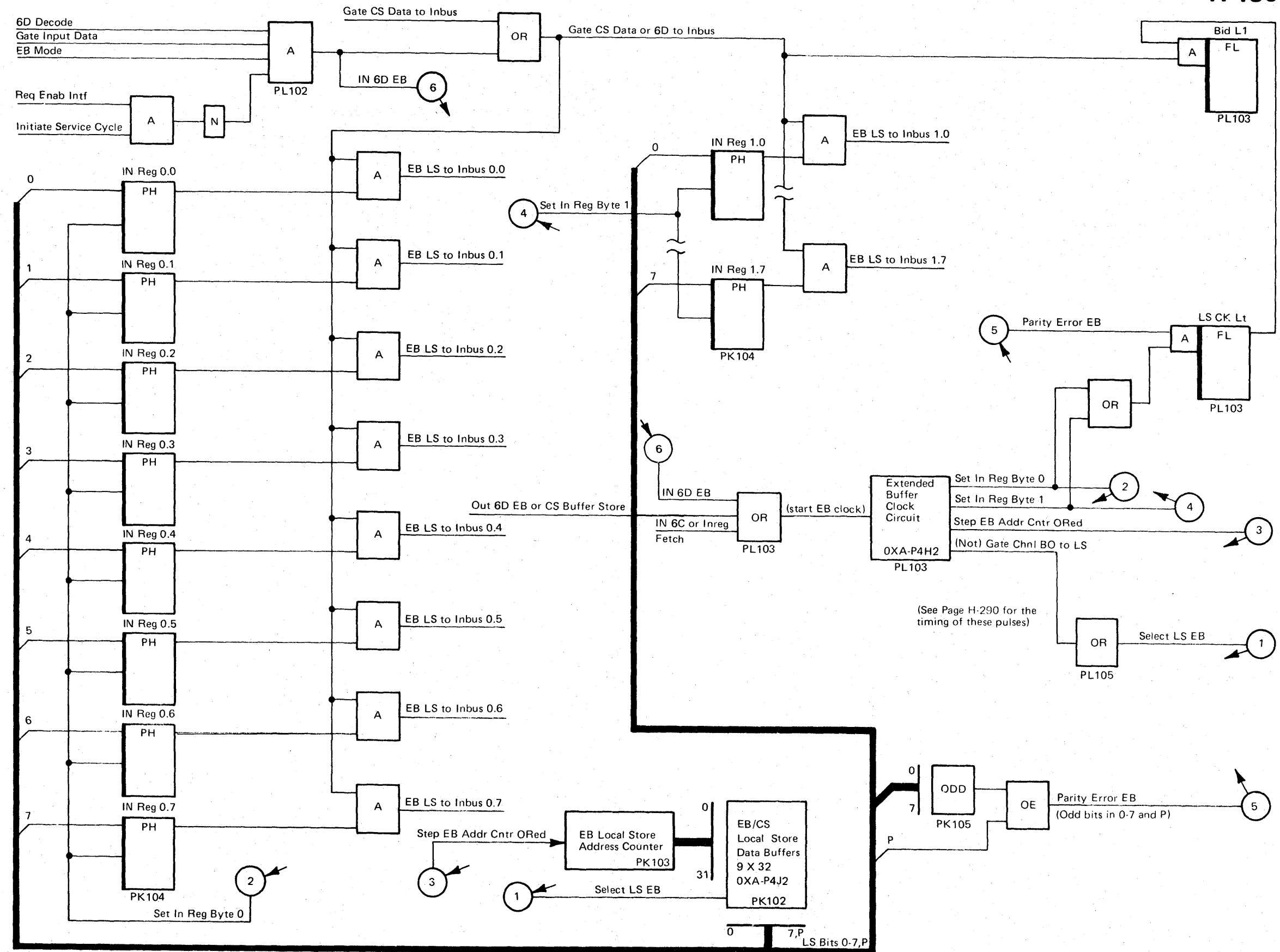
The Input X'6C' instruction loads the In register with two data bytes from EB/CS local store data buffer addresses 0 and 1. After a one cycle delay, the first Input X'6D' instruction transfers these to a specified CCU general register. The EB clock then loads In register byte 0 with data byte 0 from the next sequential EB/CS local store address. The EB clock increments the EB/CS local store address and then loads In register byte 1 with data byte 1 from the incremented address. The EB clock increments the address to the next sequential address. The In register buffers these two data bytes until the next Input X'6D' transfers them to the CCU. Sixteen Input X'6D' instructions are required to transfer the entire EB/CS local store data buffer. The 3705 control program must allow a delay of at least one cycle between successive Input X'6D' instructions to give the CA4 hardware enough time to load the In register (see H-290).

Each Input X'6D' loads the In register with two data bytes. If an inbound-data transfer sends an odd number of bytes, the last data character and the contents of the next EB/CS local store address will be loaded into the In register. The 3705 control program uses the transferred byte count to know that the last data byte was not part of this data transfer.

Each byte of data from the EB/CS local store is parity checked and a parity error forces a level 1 interrupt.

Summary of CCU Inbus bits during Input X'6D'

Bit	Card Loc	ALD Page	Function
0.0	E4J2	PK 104	EB data buffer even byte-bit 0
0.1	E4J2	PK 104	EB data buffer even byte-bit 1
0.2	E4J2	PK 104	EB data buffer even byte-bit 2
0.3	E4J2	PK 104	EB data buffer even byte-bit 3
0.4	E4J2	PK 104	EB data buffer even byte-bit 4
0.5	E4J2	PK 104	EB data buffer even byte-bit 5
0.6	E4J2	PK 104	EB data buffer even byte-bit 6
0.7	E4J2	PK 104	EB data buffer even byte-bit 7
1.0	E4J2	PK 104	EB data buffer odd byte-bit 0
1.1	E4J2	PK 104	EB data buffer odd byte-bit 1
1.2	E4J2	PK 104	EB data buffer odd byte-bit 2
1.3	E4J2	PK 104	EB data buffer odd byte-bit 3
1.4	E4J2	PK 104	EB data buffer odd byte-bit 4
1.5	E4J2	PK 104	EB data buffer odd byte-bit 5
1.6	E4J2	PK 104	EB data buffer odd byte-bit 6
1.7	E4J2	PK 104	EB data buffer odd byte-bit 7

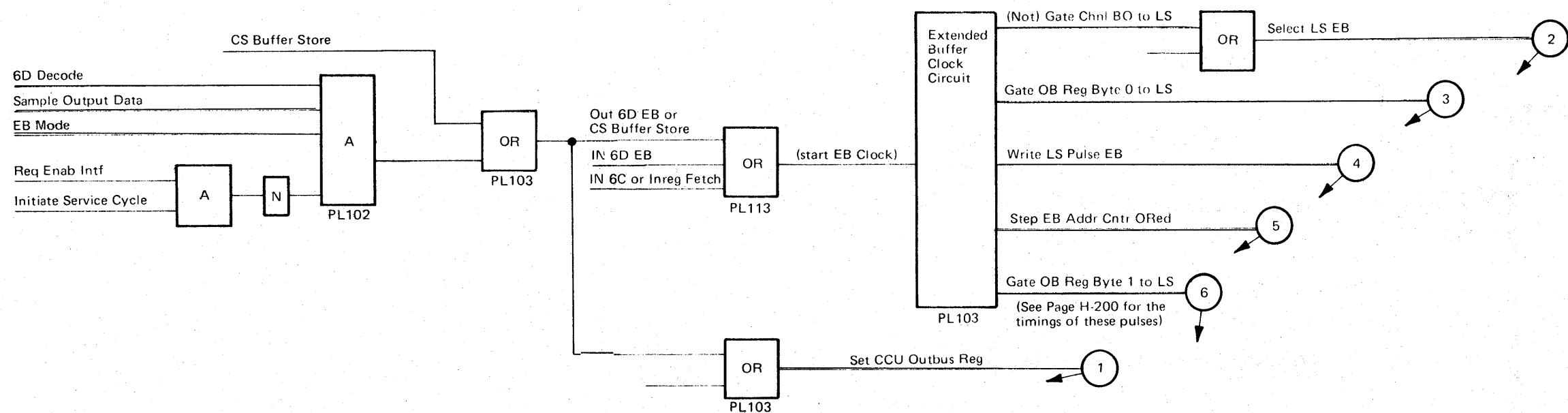


OUTPUT X'6D' INSTRUCTION

(Type 4 CA Extended Buffer/Cycle Steal Mode Data Buffer Bytes)

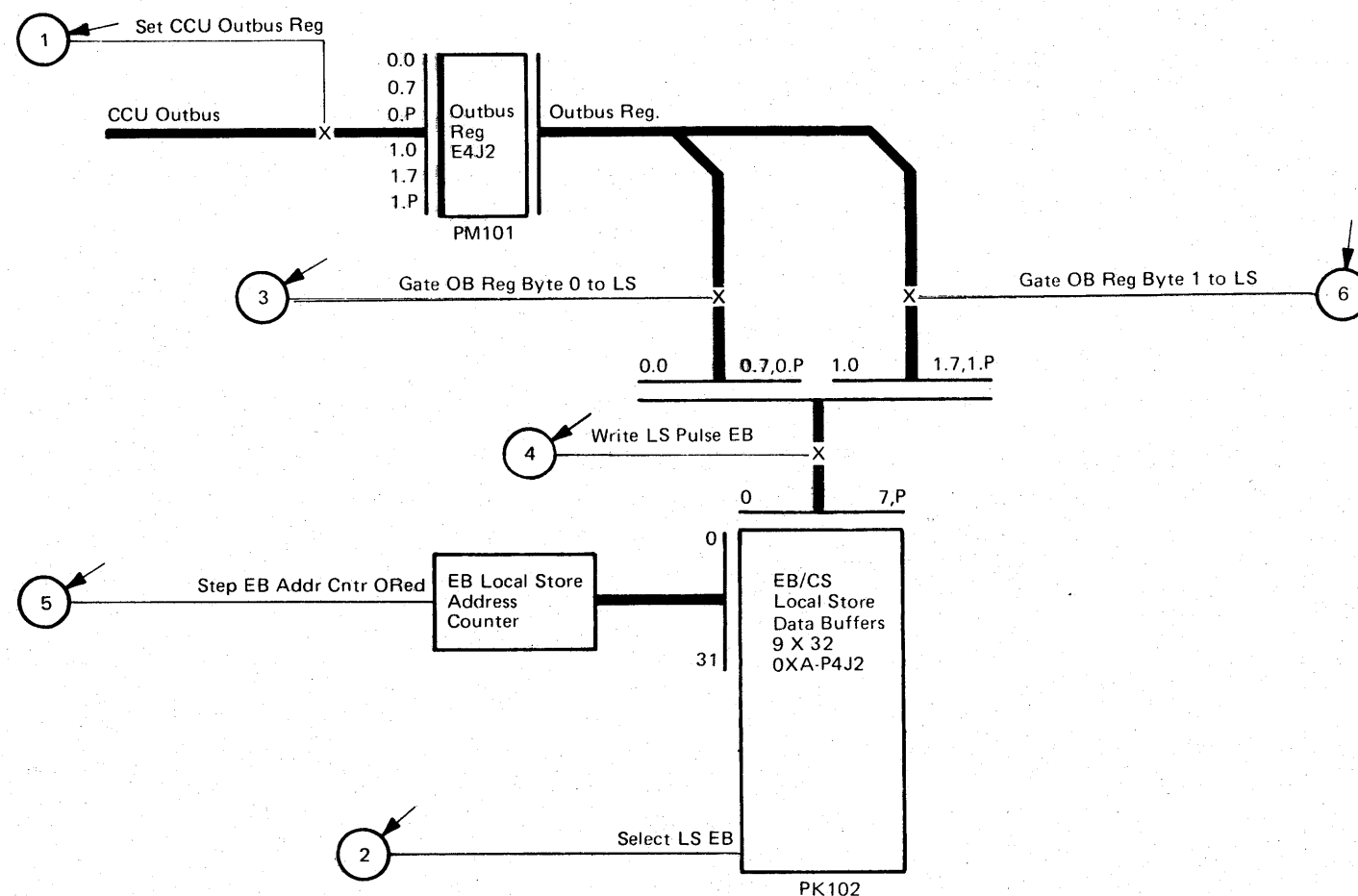
The control program uses the Output X'6D' instruction to load the EB/CS local store data buffers with data for an outbound data transfer.

The data is buffered in the outbus register until it can be written into the EB/CS local store data buffer. A previous Output X'6C' instruction had reset the EB/CS local store address counter to 0 so that the data may be loaded sequentially beginning with address 0. The EB clock generates the gating and write pulses to load data byte 0 into the EB/CS local store, increment the EB/CS local store address counter by 1, then load data byte 1. Each Output X'6D' instruction thus loads two data bytes in sequential addresses. Sixteen Output X'6D' instructions are required to fill the EB/CS local store. The 3705 control program must allow a delay of at least one cycle between successive Output X'6D' instructions to give the CA4 hardware enough time to load the EB/CS local store data buffers (see H-200).



Summary of CCU Outbus bits during Output X'6D'

Bit	Card LOC	ALD Page	Function
0.0	E4J2	PK 102	EB data buffer even byte--bit 0
0.1	E4J2	PK 102	EB data buffer even byte--bit 1
0.2	E4J2	PK 102	EB data buffer even byte--bit 2
0.3	E4J2	PK 102	EB data buffer even byte--bit 3
0.4	E4J2	PK 102	EB data buffer even byte--bit 4
0.5	E4J2	PK 102	EB data buffer even byte--bit 5
0.6	E4J2	PK 102	EB data buffer even byte--bit 6
0.7	E4J2	PK 102	EB data buffer even byte--bit 7
1.0	E4J2	PK 102	EB data buffer odd byte--bit 0
1.1	E4J2	PK 102	EB data buffer odd byte--bit 1
1.2	E4J2	PK 102	EB data buffer odd byte--bit 2
1.3	E4J2	PK 102	EB data buffer odd byte--bit 3
1.4	E4J2	PK 102	EB data buffer odd byte--bit 4
1.5	E4J2	PK 102	EB data buffer odd byte--bit 5
1.6	E4J2	PK 102	EB data buffer odd byte--bit 6
1.7	E4J2	PK 102	EB data buffer odd byte--bit 7



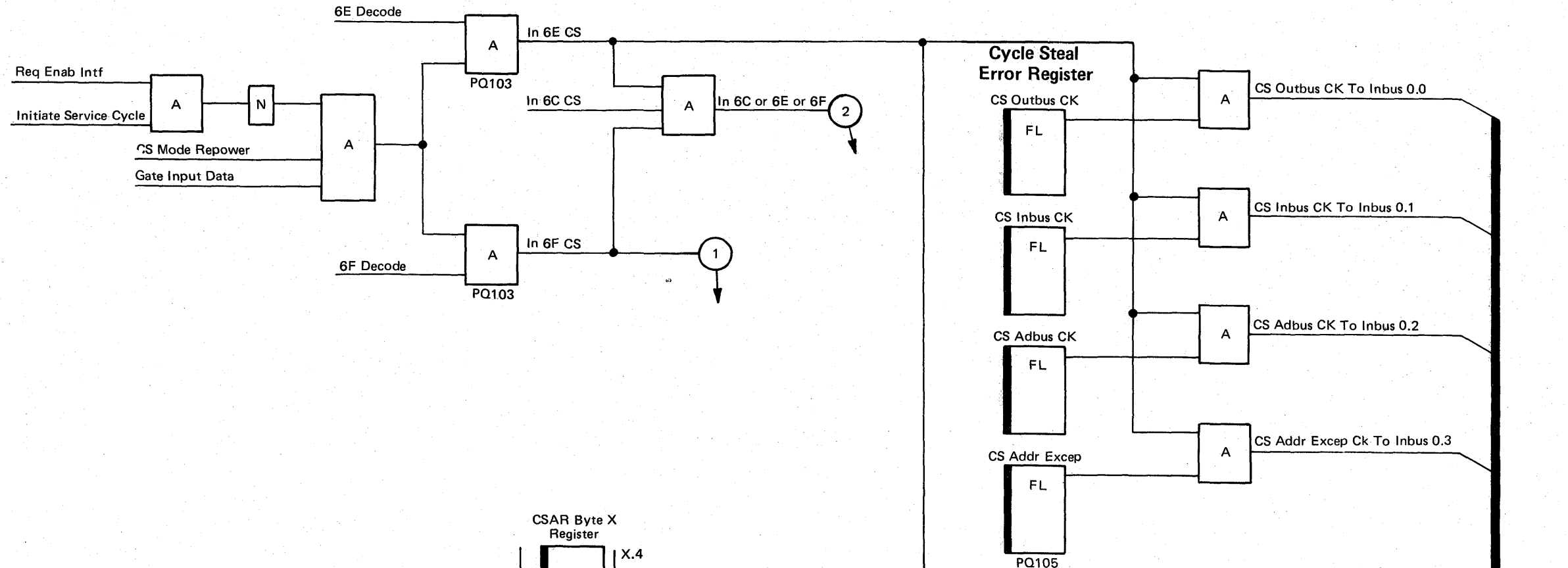
INPUT X'6E' AND X'6F' INSTRUCTIONS

INPUT X'6E' (CS ERROR REGISTER AND CS BYTE X)

The 3705 control program uses the Input X'6E' instruction to transfer the contents of the 'cycle steal error register' (see H-380) and the 'CSAR byte X register' to a specified CCU general register.

Summary of CCU Inbus bits during Input X'6E'

Bit	Card Loc	ALD Page	Function
0.0	E4E2	PQ105	Cycle Steal Outbus Error
0.1	E4E2	PQ105	Cycle Steal Inbus Error
0.2	E4E2	PQ105	Cycle Steal Adbus Error
0.3	E4E2	PQ105	Cycle Steal Address Exception
0.4			0
0.5			0
0.6			0
0.7			0
1.0			0
1.1			0
1.2			0
1.3			0
1.4	E4D2	PP103	CSAR Bit X.4
1.5	E4D2	PP103	CSAR Bit X.5
1.6	E4D2	PP103	CSAR Bit X.6
1.7	E4D2	PP103	CSAR Bit X.7

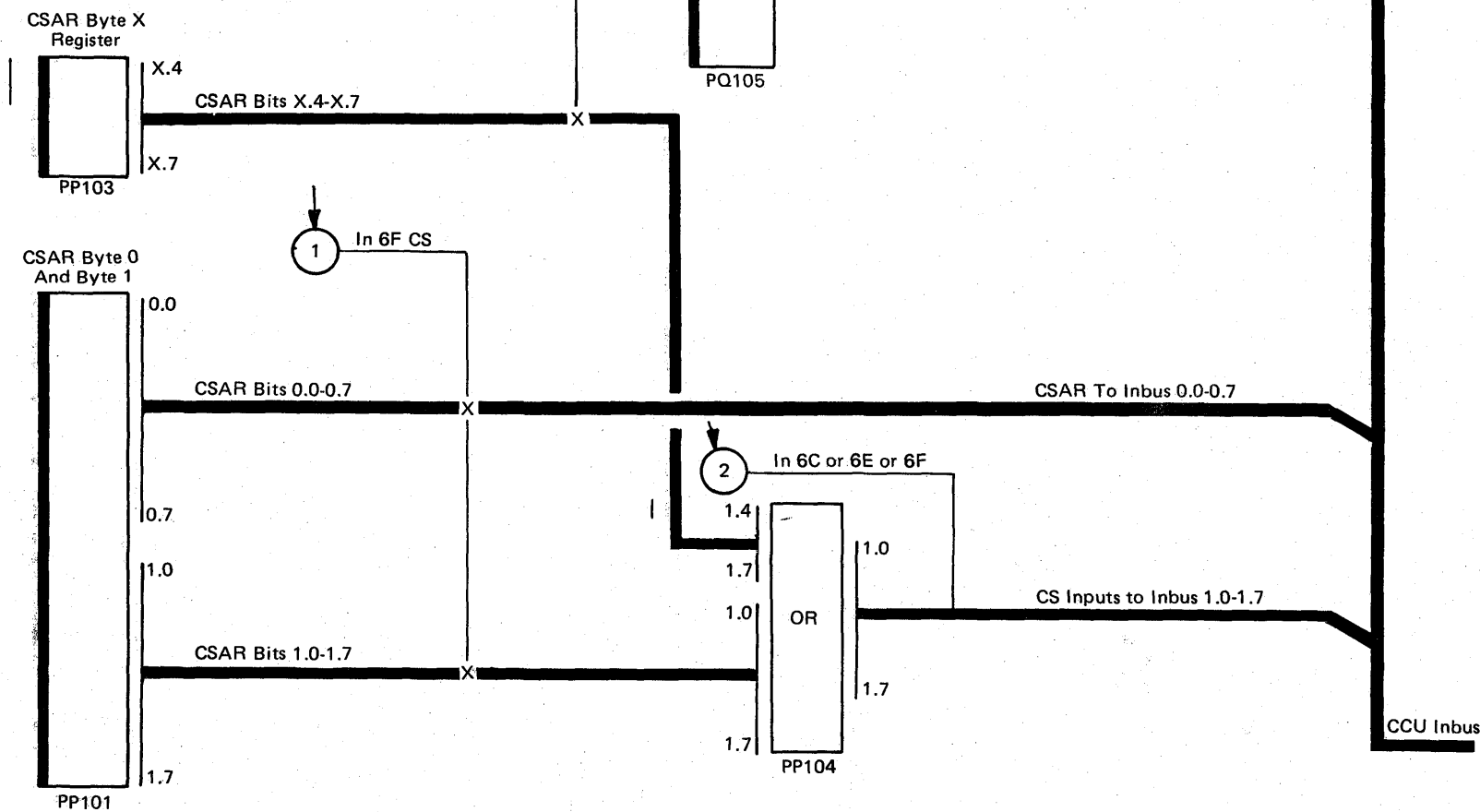


INPUT X'6F' (CSAR BYTE 0 AND BYTE1)

The 3705 control program uses the Input X'6F' instruction to transfer the contents of CSAR byte 0 and 1 to a specified CCU general register.

Summary of CCU Inbus bits during Input X'6F'

Bit	Card Loc	ALD Page	Function
0.0	E4D2	PP104	CSAR Bit 0.0
0.1	E4D2	PP104	CSAR Bit 0.1
0.2	E4D2	PP104	CSAR Bit 0.2
0.3	E4D2	PP104	CSAR Bit 0.3
0.4	E4D2	PP104	CSAR Bit 0.4
0.5	E4D2	PP104	CSAR Bit 0.5
0.6	E4D2	PP104	CSAR Bit 0.6
0.7	E4D2	PP104	CSAR Bit 0.7
1.0	E4D2	PP104	CSAR Bit 1.0
1.1	E4D2	PP104	CSAR Bit 1.1
1.2	E4D2	PP104	CSAR Bit 1.2
1.3	E4D2	PP104	CSAR Bit 1.3
1.4	E4D2	PP104	CSAR Bit 1.4
1.5	E4D2	PP104	CSAR Bit 1.5
1.6	E4D2	PP104	CSAR Bit 1.6
1.7	E4D2	PP104	CSAR Bit 1.7



OUTPUT X'6E' AND X'6F' INSTRUCTIONS

OUTPUT X'6E' (CSAR BYTE X)

The 3705 control program uses the Output X'6E' instruction to set the extended address bits in the CSAR byte X register. Output X'6F' must first be executed to set CSAR bytes 0 and 1 since it also resets CSAR byte X. Output X'6E' is then executed if the storage address is above 64 K (CSAR bits X.4, X.5, X.6 or X.7=1).

Summary of CCU Outbus bits during Output X'6E'

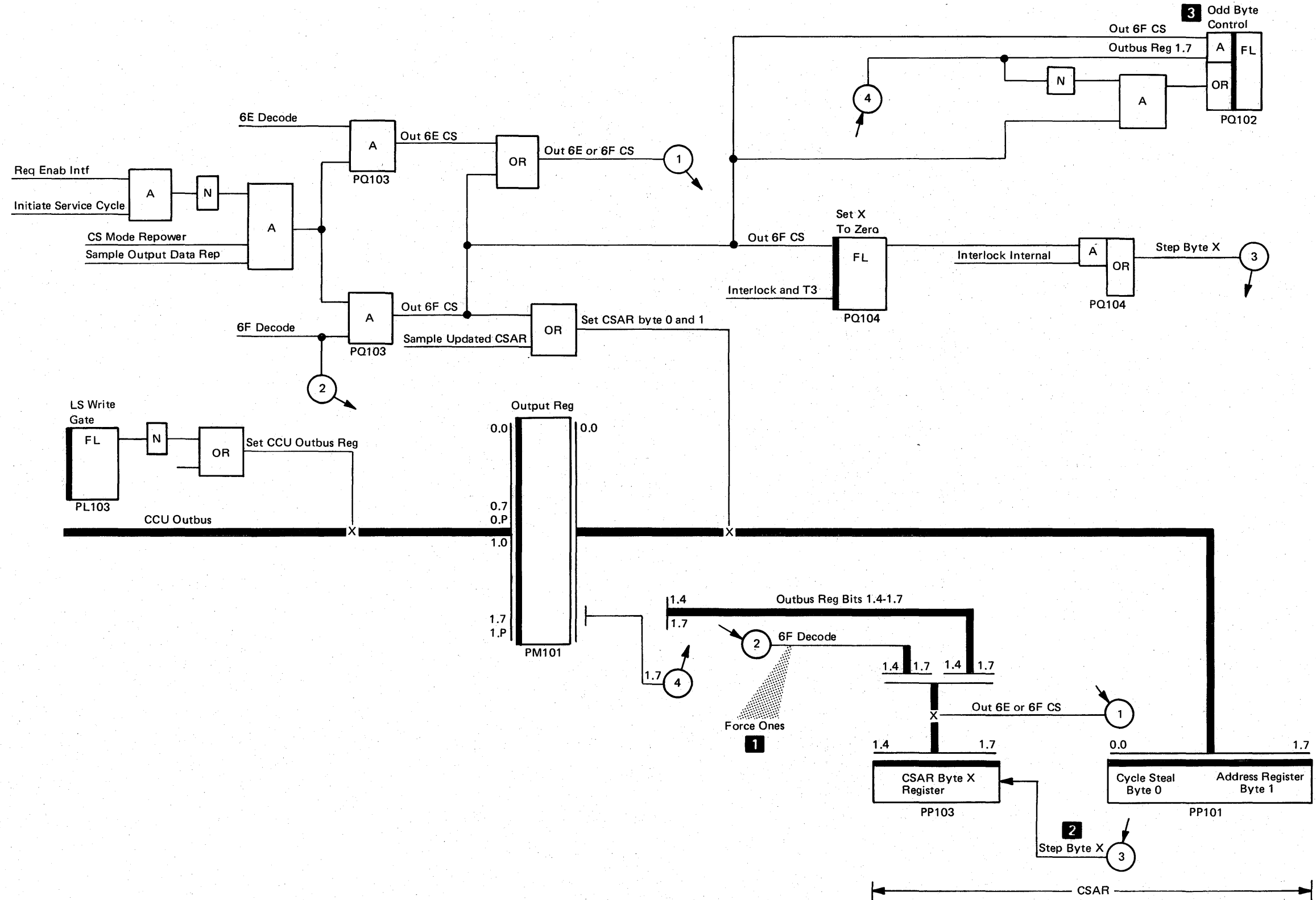
Bit	Card Loc	ALD Page	Function
0.0			0
0.1			0
0.2			0
0.3			0
0.4			0
0.5			0
0.6			0
0.7			0
1.0			0
1.1			0
1.2			0
1.3			0
1.4	E4D2	PP103	CSAR Bit X.4
1.5	E4D2	PP103	CSAR Bit X.5
1.6	E4D2	PP103	CSAR Bit X.6
1.7	E4D2	PP103	CSAR Bit X.7

OUTPUT X'6F' (CSAR BYTE 0 AND BYTE 1)

The 3705 control program uses the Output X'6F' instruction to set the storage address (for the first data buffer byte involved in a cycle-steal data transfer) in CSAR bytes 0 and 1. Output X'6F' resets CSAR byte X by (1) forcing ones into CSAR bits X.4-X.7 **1** and (2) stepping CSAR byte X from X'F' to X'0' **2**. Resetting CSAR byte X enables the control program to set up CSAR using only Output X'6F' if the storage address is not above 64 K. Output X'6F' also sets/resets the 'odd byte control' latch **3** depending upon the state of outbus reg bit 1.7 (CSAR bit 1.7).

Summary of CCU Outbus bits during Output X'6F'

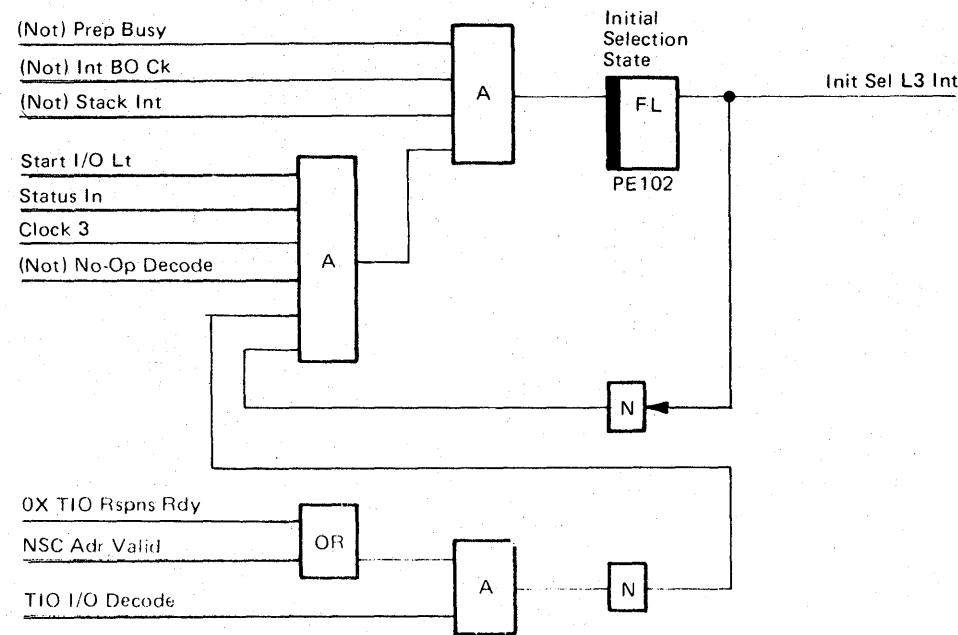
Bit	Card Loc	ALD Page	Function
0.0	E4D2	PP101	CSAR Bit 0.0
0.1	E4D2	PP101	CSAR Bit 0.1
0.2	E4D2	PP101	CSAR Bit 0.2
0.3	E4D2	PP101	CSAR Bit 0.3
0.4	E4D2	PP101	CSAR Bit 0.4
0.5	E4D2	PP101	CSAR Bit 0.5
0.6	E4D2	PP101	CSAR Bit 0.6
0.7	E4D2	PP101	CSAR Bit 0.7
1.0	E4D2	PP101	CSAR Bit 1.0
1.1	E4D2	PP101	CSAR Bit 1.1
1.2	E4D2	PP101	CSAR Bit 1.2
1.3	E4D2	PP101	CSAR Bit 1.3
1.4	E4D2	PP101	CSAR Bit 1.4
1.5	E4D2	PP101	CSAR Bit 1.5
1.6	E4D2	PP101	CSAR Bit 1.6
1.7	E4D2	PP101	CSAR Bit 1.7



OUTBOUND DATA TRANSFERS—EB MODE

Outbound data transfers result from channel Read commands that direct the transfer of data from 3705 storage to the host CPU. When the CA4 is in EB mode, the 3705 control program must execute an Output X'6D' for each two data bytes that are to be transferred to the channel whether the CA4 is in ESC or NSC mode.

CA DECODES THE COMMAND AND REQUESTS AN INTERRUPT



The 3705 control program responds to the initial select level 3 interrupt with the following instructions.

Instruction	General Register Bits		Indication or Function
	Byte 0	Byte 1	
Input X'77'	0000 0000	1000 10X0	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected = 1 type 4 CA #2 selected
Input X'61'	address	command	Byte 0 = address Byte 1 = command
Input X'60'	1000 0000	0000 0000	Normal initial selection (Note 1)
At this point the control program queues the control block for this line on the priority data-service-out queue. After all control blocks ahead of this one are serviced, the following sequence is performed.			
Output X'63'	address	xxxx xxxx	Byte 0 = transfer address Byte 1 = all zeros
Output X'6C'	1000 0000	1000 0111	0.0 = set extended buffer mode 1.3-1.7 = 0111 to transfer seven data bytes out (Note 2) Resets EB adr counter to adr 00
Output X'6D'	data	data	Byte 0 = data for EB LS adr 00 Byte 1 = data for EB LS adr 01
Minimum of one cycle delay between successive Output X'6D's			
Output X'6D'	data	data	Byte 0 = data for EB LS adr 02 Byte 1 = data for EB LS adr 03
Minimum of one cycle delay between successive Output X'6D's			
Output X'6D'	data	data	Byte 0 = data for EB LS adr 04 Byte 1 = data for EB LS adr 05
Minimum of one cycle delay between successive Output X'6D's			
Output X'6D'	data	xxxx xxxx No data	Byte 0 = data for EB LS adr 06 Byte 1 = Contents are loaded into EB LS adr 07
Minimum of one cycle delay between Output X'6D' and Output X'62'			
Output X'62'	1000 0010	0000 0100	0.0 = outbound data transfer 0.6 = reset data/status interrupt 1.5 = set priority outbound-data transfer sequence EB
Output X'67'	0000 0000	0100 0000	1.1 = set program interrupt (to block initial select interrupts)

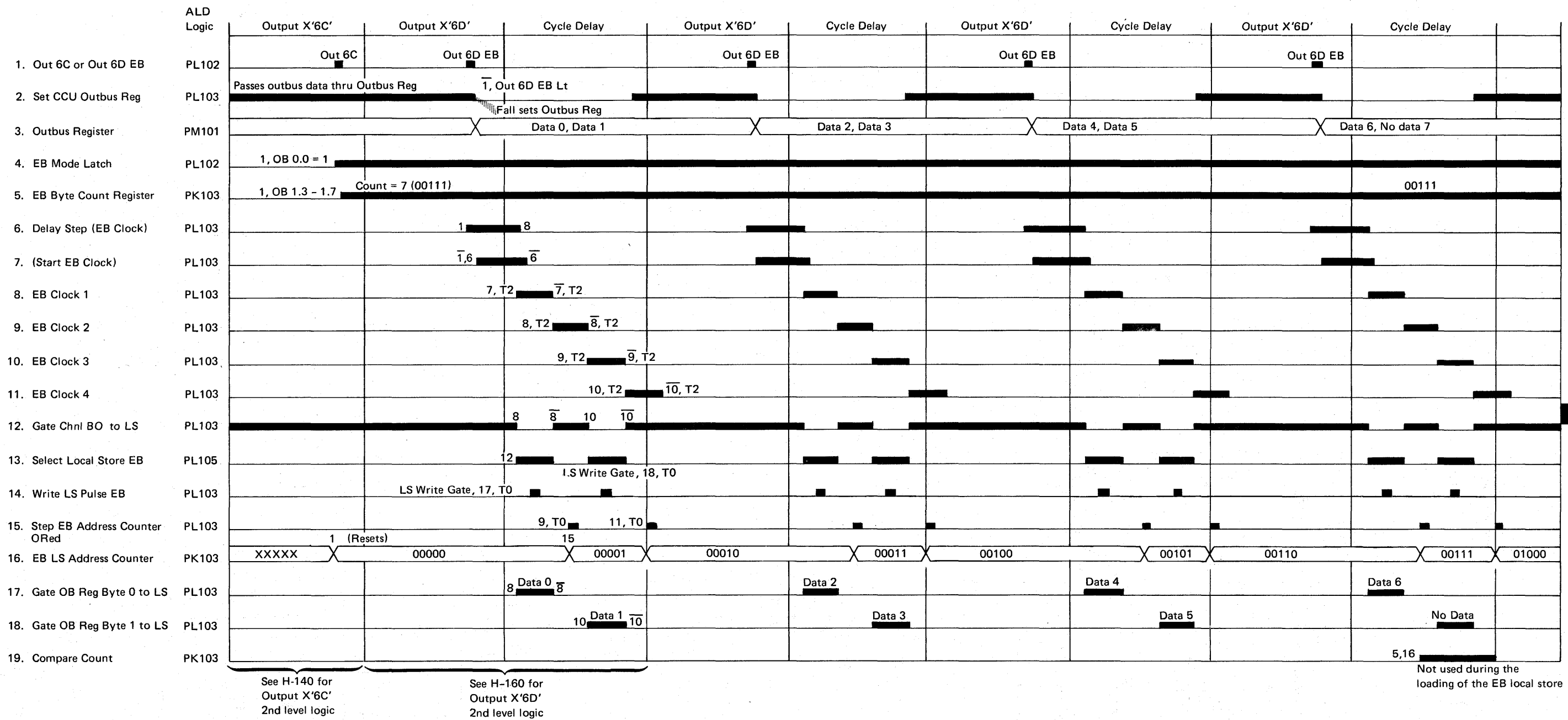
Loads seven data bytes into the EB local store (data buffer) starting at address 00 plus the "no data" contents of general register byte 1 into address 07. See H-200 for a sequence chart for this operation.

Outbound transfer initiates a channel data service cycle. See H-220 for a sequence chart for this operation and the channel service cycle.

- Notes: 1. Other bits may be transferred to the CCU during this input. If other bits are on, the 3705 control program must take action differently from the normal initial selection.
2. From one to thirty-two bytes of data may be transferred to the channel. The number of Output X'6D's depends on the number of bytes of data to be transferred.

OUTBOUND DATA TRANSFERS—EB MODE (PART 1)

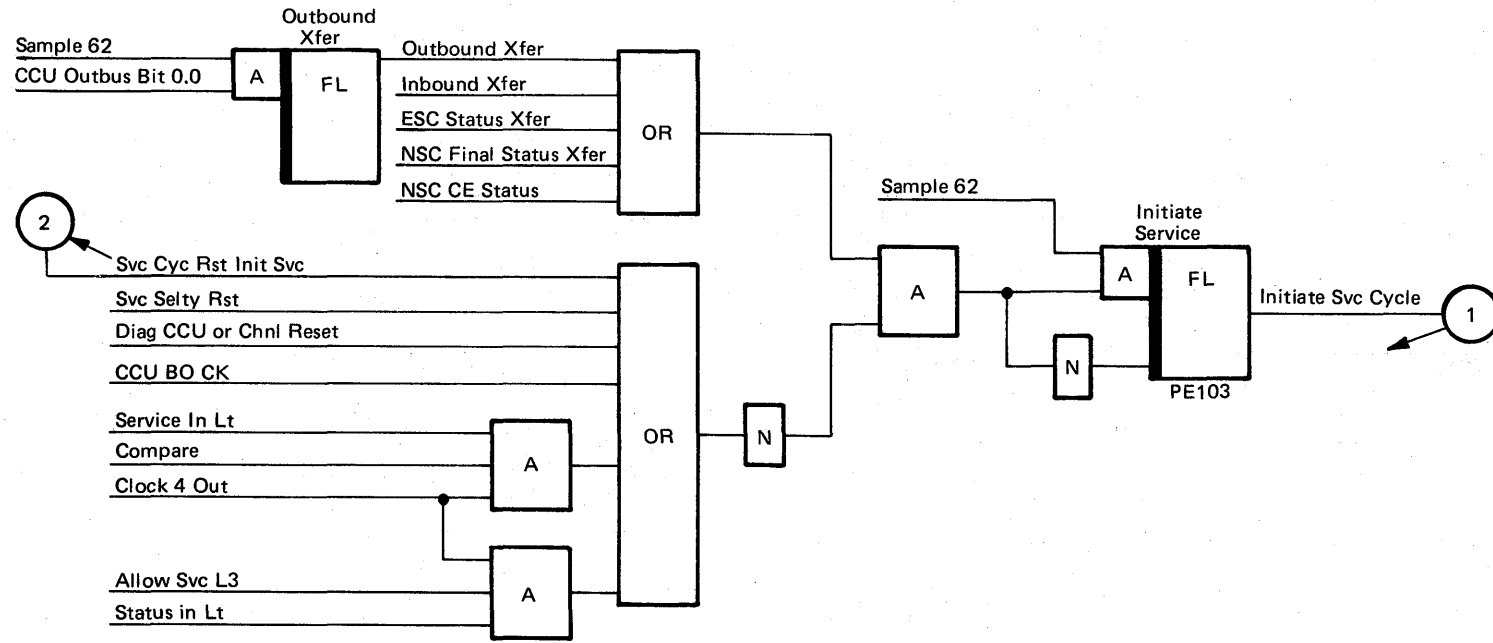
Sequence Chart for Loading the EB Local Store (Data Buffer)



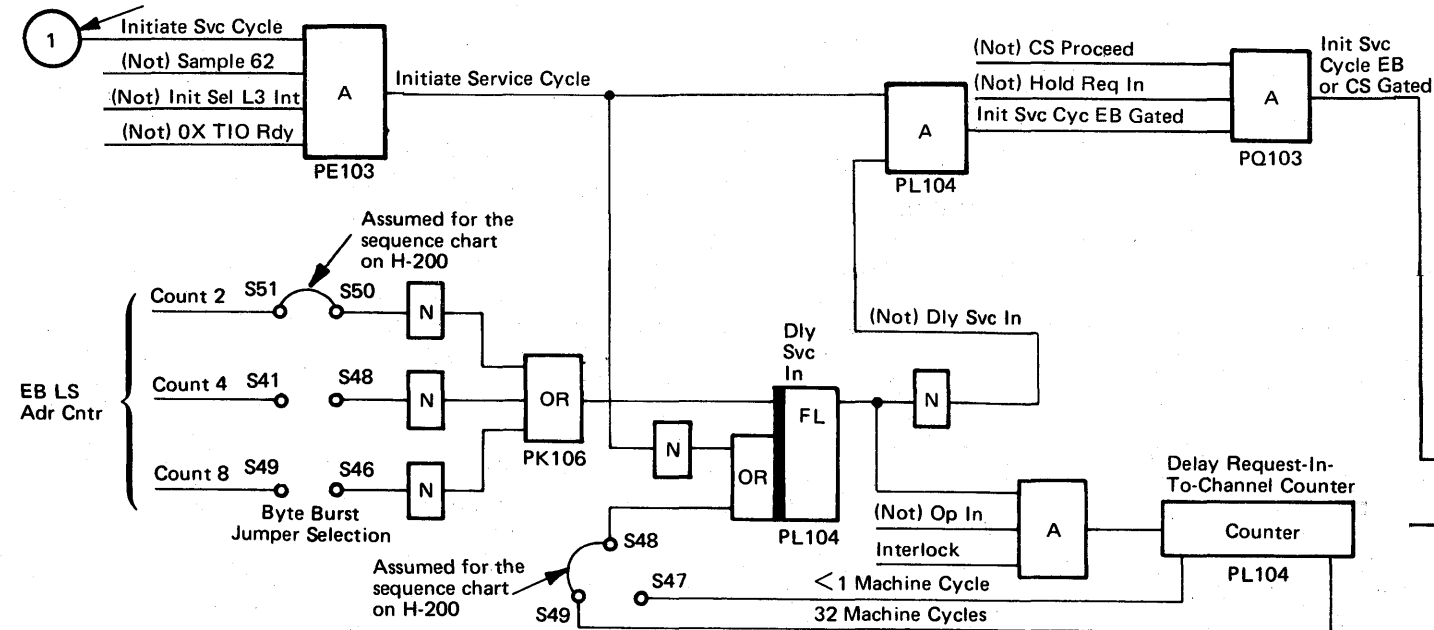
OUTBOUND DATA TRANSFERS—EB MODE (PART 2)

CA to Channel Data Transfer—See H-220 for Sequence Chart

The Output X'62' instruction starts a channel service cycle so that the data loaded into the EB/CS local store can be transferred to the channel.

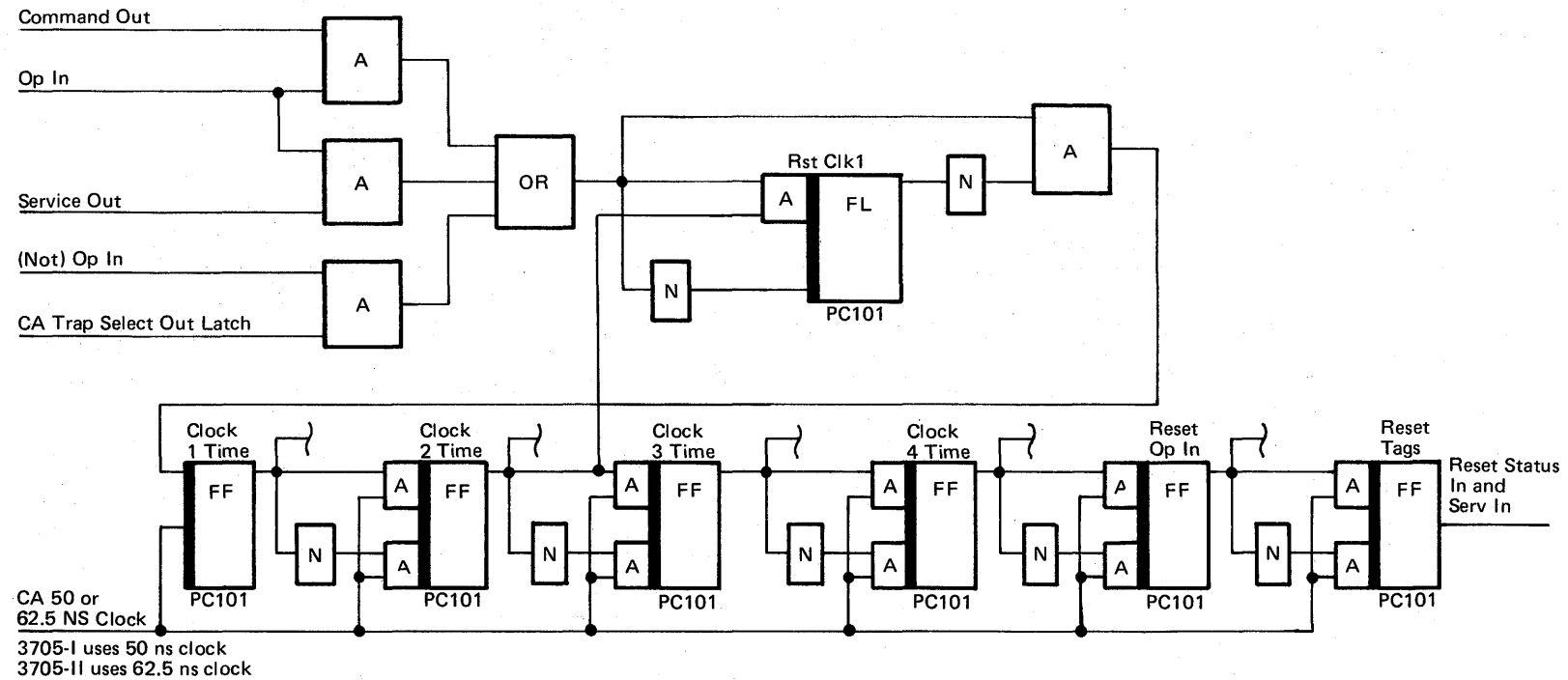


The CA4 sends Request In to the channel to start the service cycle.

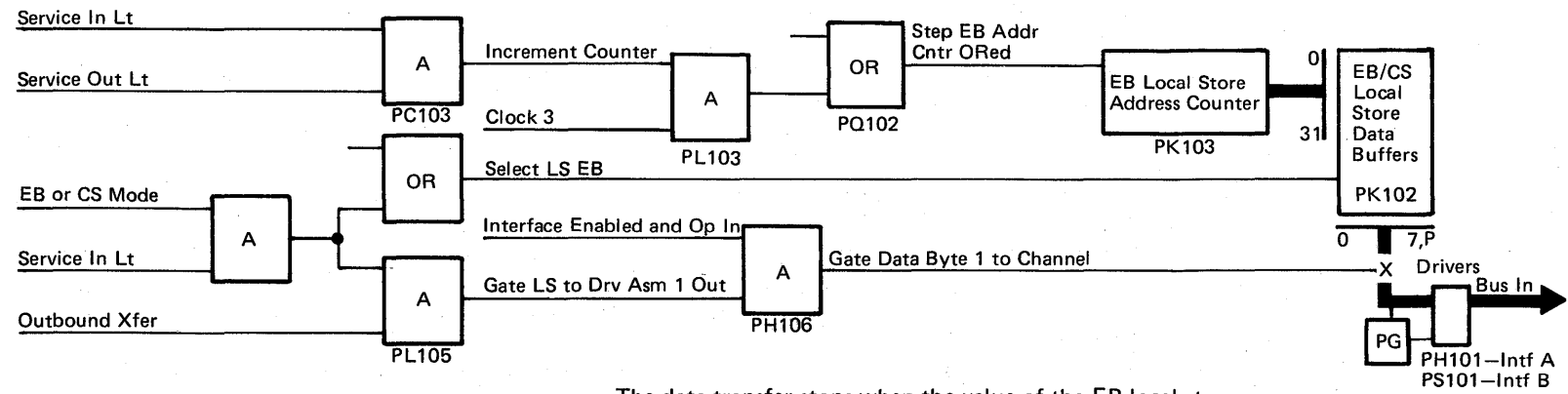


The type 4 CA provides the capability of transferring 4, 8, 16, or 32 byte bursts of data—the selection made by a CE-installed jumper. The EB address counter steps as each data byte transfers to the channel. 'Count 2' falls after four data bytes have been transferred ('count 4' after eight, 'count 8' after sixteen) to set the 'delay service in' latch. This latch is not set for a thirty-two byte burst. Op In resets to drop the CA off the channel and a delay counter starts. A CE-installed jumper selects how much delay occurs before the CA raises Request In to continue transferring data to the EB channel.

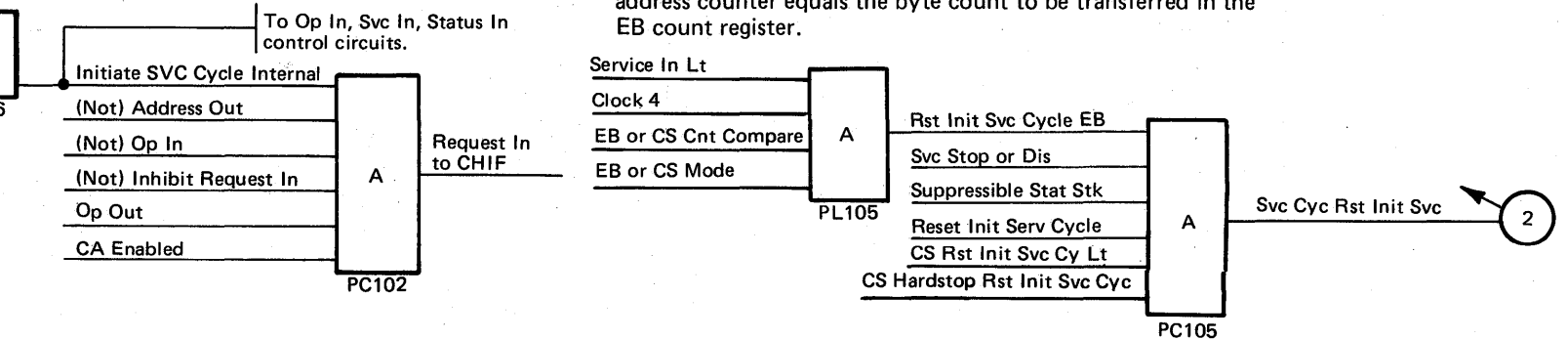
The channel tag clock operates each time the channel and the CA start a data transfer. The clock synchronizes the CA and the channel to handle the data transfer.



Service In causes the next data byte to be read out of the EB/CS LS data buffer to the channel and then increments the EB address counter.



The data transfer stops when the value of the EB local store address counter equals the byte count to be transferred in the EB count register.

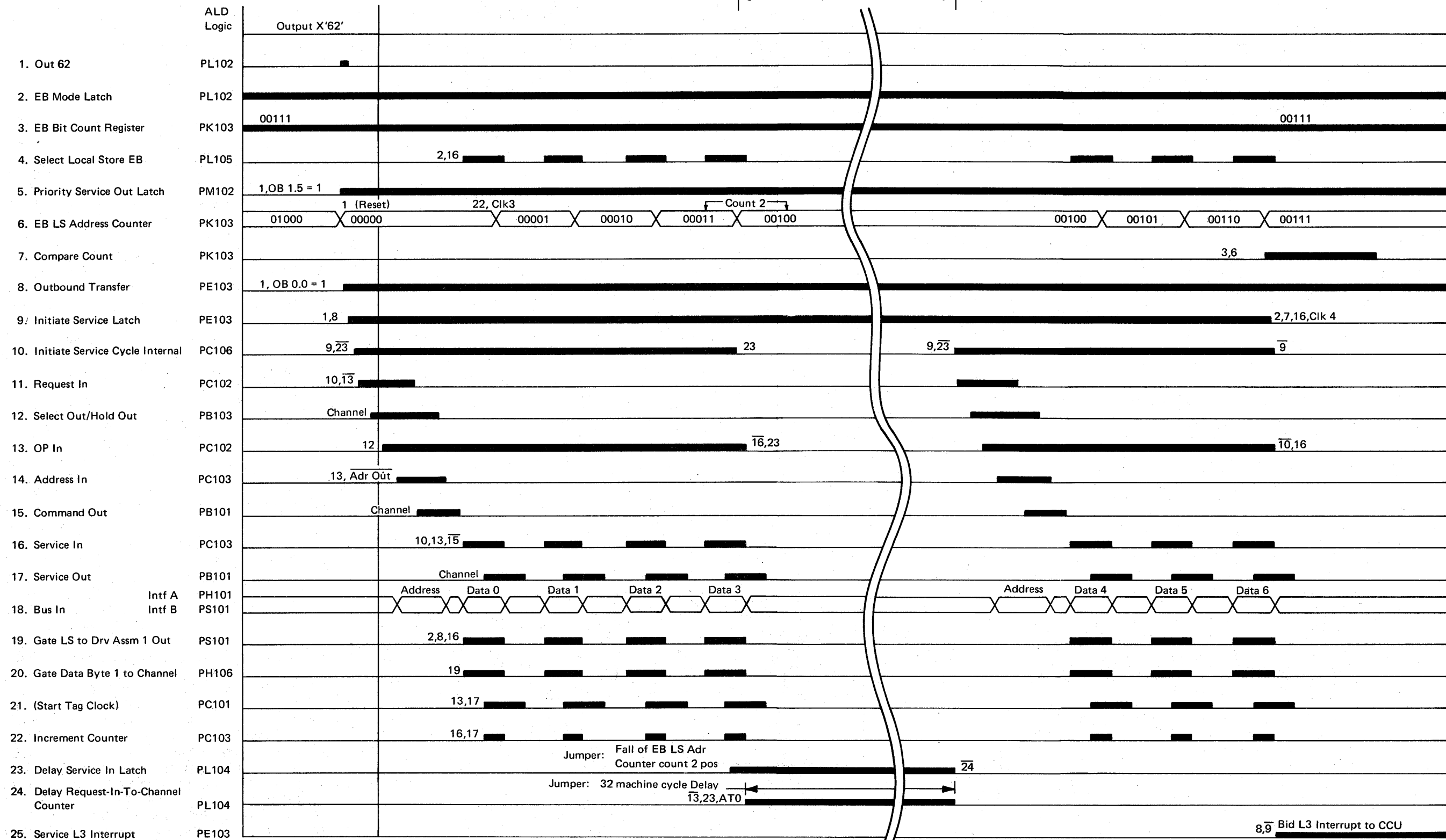


OUTBOUND DATA TRANSFERS-EB MODE (PART 3)

Sequence Chart for the Channel Service Cycle

Continued from H-200

Any Start I/O to this channel interface during this delay of Service In receives an initial selection status of X'70' (CCU Busy).



This sequence continues into the automatic CA4 selection by priority sequence chart on H-240 that is applicable if multiple Type 4 CAs are installed. If only one Type 4 CA is installed, the operation is the same as for the Type 1 CA (See Page 8-330 for the control program response to the level 3 data/status interrupt).

Automatic CA4 Selection by Priority—Multiple Type 4 CAs

When multiple type 4 CAs are installed, the automatic-selection circuit automatically selects the CA4 with the highest priority interrupt request. The control program must execute an Output X'67' with all zeros in the specified general register to set the 'prime priority select' latch **1**. When the next Input X'77' is executed, the highest priority CA is selected **2**. If the priorities were equal, the automatic-selection circuit selects the first CA4 with an equal priority that receives the 'selected from previous CA' signal **3**.

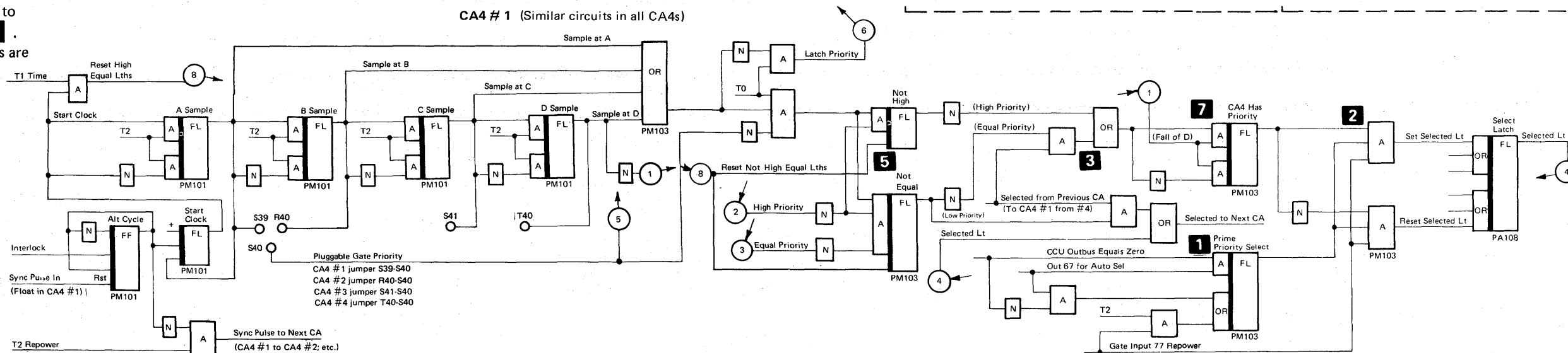
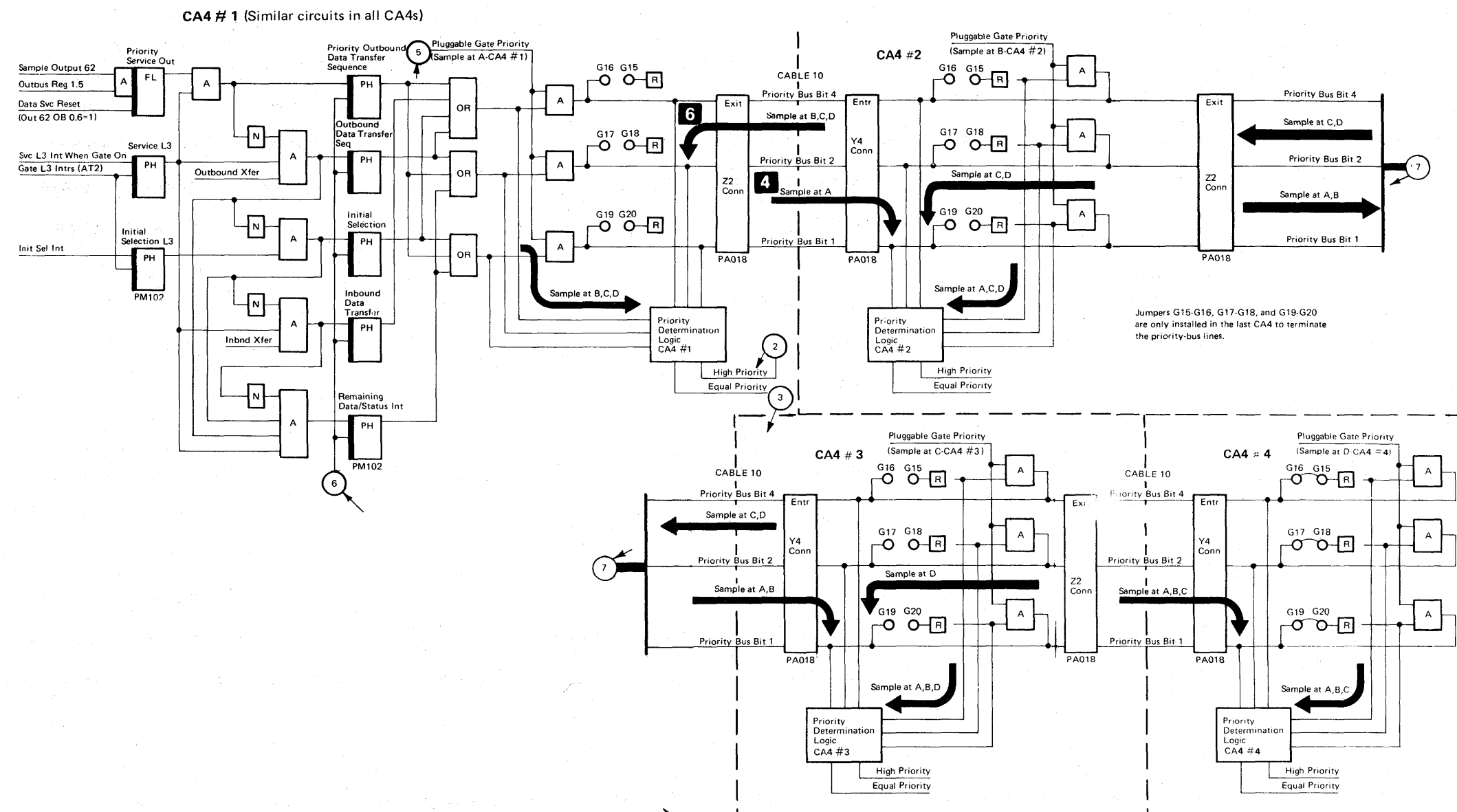
The control program can assign a higher level priority to an Outbound Data Transfer Sequence by setting bit 1.5 to 1 when executing Output X'62' to set the Outbound Sequence.

The automatic-selection circuit assigns priority bits to all L3 interrupts according to this table:

L3 Interrupt	Priority 4	Bus 2	Bits 1
Priority Outbound Data Transfer Seq.	1	1	1
Outbound Data Transfer Seq.	1	1	0
Initial Selection Interrupt	1	0	1
Inbound Data Transfer Seq.	1	0	0
Remaining Data Status Interrupts	0	1	1

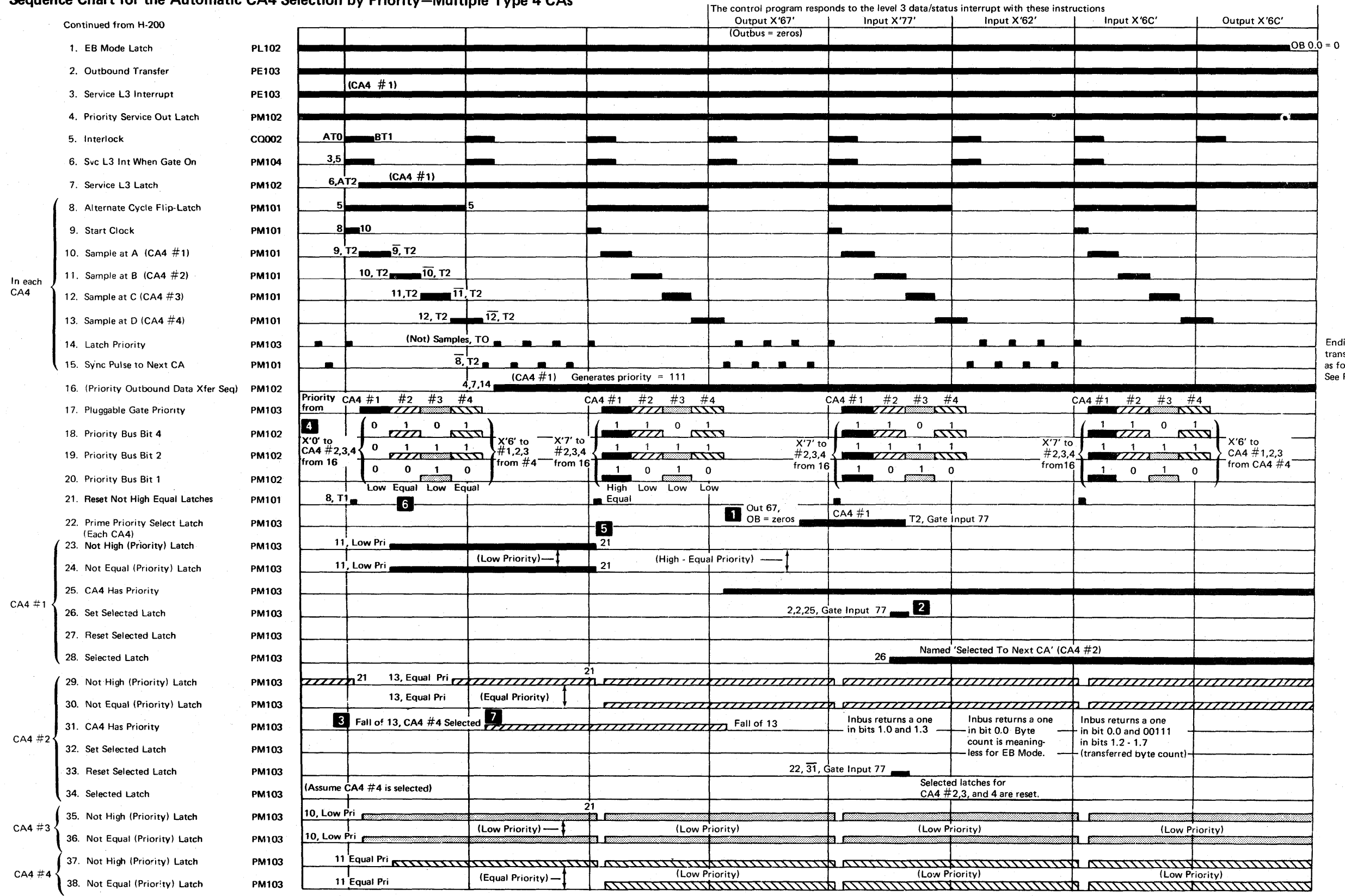
At 'sample at A' time, CA4 #1 sends its L3 interrupt state to the other CA4s via the priority bus **4**. Each of these CA4s compares its priority with the CA4 #1 priority and sets its appropriate 'not high' and/or 'not equal' priority latches. Once set, these latches remain on until reset by the 'reset not high equal latches' pulse **5**. At 'sample at B' time, CA #2 sends its L3 interrupt state to the other CA4s **6**. Each of these CA4s (#1, #3, and #4) compares its priority with the CA #2 priority and sets its appropriate 'not high' and/or 'not equal' priority latches. Some of these 'not high' and/or 'not equal' priority latches may have been set at 'sample at A' time. At 'sample at C' time, CA4 #3 sends its L3 interrupt state to CA4 #1, 2, and 4 and at 'sample at D' time, CA4 #4 sends its L3 interrupt state to CA4 #1, 2, and 3 with the subsequent setting of the appropriate 'not high' and/or 'not equal' priority latches.

At the fall of 'sample at D' time, each CA4 interrogates the states of its 'not high' and 'not equal' priority latches as well as the state of the 'selected from previous CA' line to determine whether to set its 'CA4 has priority' latch **7**. This sampling occurs continuously but the select latches are set or reset by this circuit only by the next Input X'77' instruction.



OUTBOUND DATA TRANSFERS — EB MODE (PART 5)

Sequence Chart for the Automatic CA4 Selection by Priority—Multiple Type 4 CAs



The control program responds to the level 3 data/status interrupt with these instructions
 Output X'67' (Outbus = zeros) Input X'77' Input X'62' Input X'6C' Output X'6C'

Ending an outbound transfer is the same as for the type 1 CA. See Page 8-340.

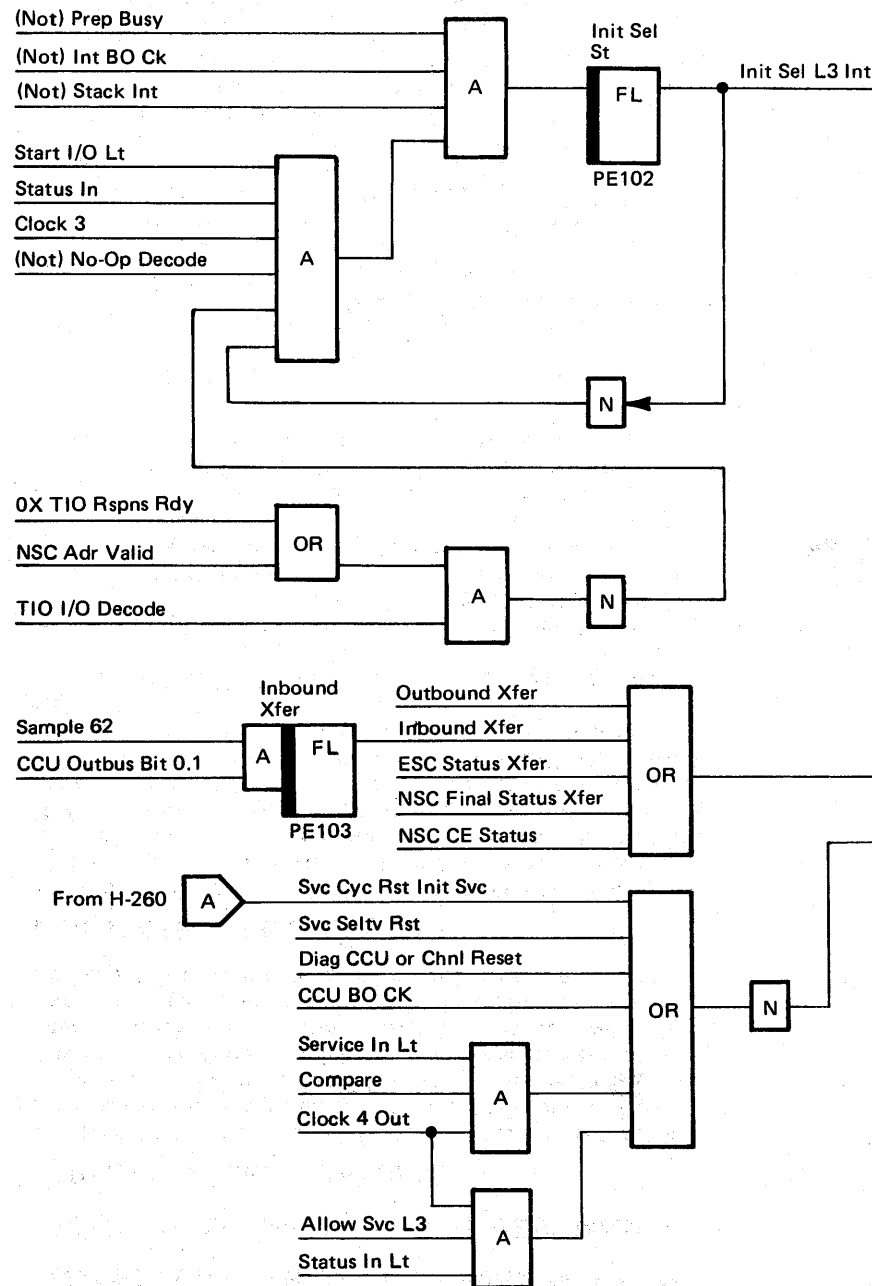


INBOUND DATA TRANSFERS—EB MODE

Inbound data transfers result from commands that require the passing of data from the host CPU to 3705 storage.

When the commands are decoded, they request an initial selection level 3 interrupt so that the 3705 control program can determine what action to take to service the command. The commands start an initial selection sequence as shown on 8-170.

CA REQUESTS AN INITIAL SELECTION LEVEL 3 INTERRUPT



CONTROL PROGRAM RESPONDS TO THE INTERRUPT

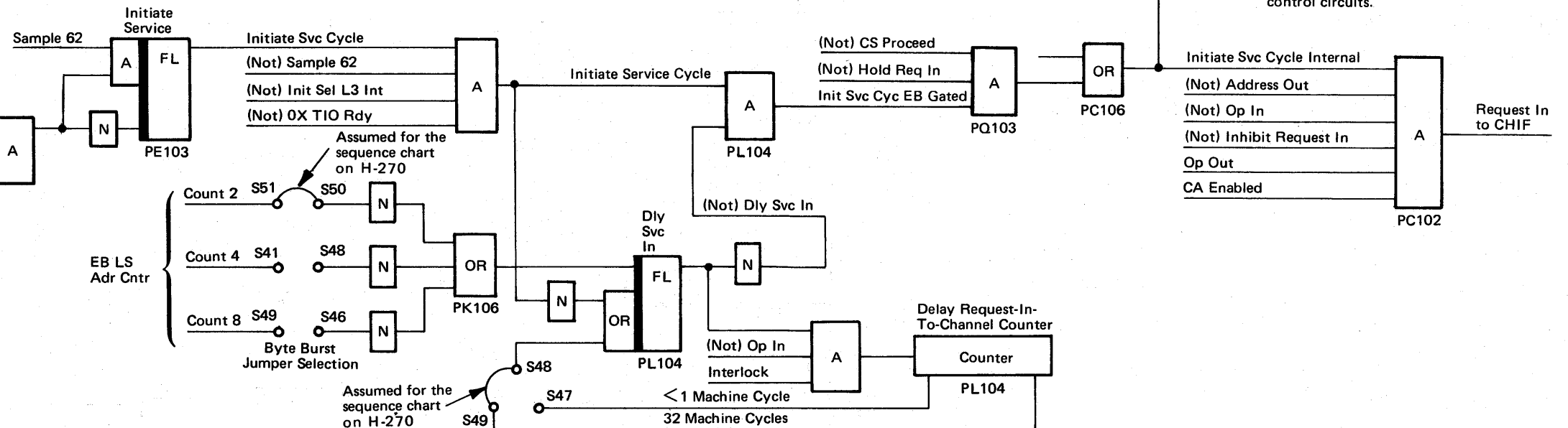
The 3705 control program responds to the initial selection level 3 interrupt with the following sequence of instructions.

Instruction	General Register Bits		Indication or Function
	Byte 0	Byte 1	
Input X'77'	0000 0000	1000 10x0	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected = 1 type 4 CA #2 selected
Input X'60'	1000 0000	0000 0000	0.0 = Normal initial selection (Note)
Input X'61'	Address	Command	Byte 0 = subchannel address Byte 1 = command
Output X'60'	xxxx xxxx	xxxx xxxx	Resets initial selection level 3 interrupt.
At this point the control program queues the control block for this line on the data-service-in queue. After all the control blocks ahead of this one, on the queue, are serviced the following sequence is performed.			
Output X'63'	Address	xxxx xxxx	Byte 0 = address Byte 1 = all zeros
Output X'6C'	1000 1001	0000 1000	0.0 = set extended buffer mode 0.4 = set SYN monitor control latch 0.7 = set EBCDIC monitor control latch 1.3-1.7 = 1000 to transfer eight data bytes Resets EB adr counter to adr 00
Output X'62'	0100 0010	0000 0000	0.1 = inbound data transfer 0.6 = reset data/status control 1.6-1.7 = request byte count limit for consecutive SYNs. 01 = 1; 10 = 2; 11 = 3; 00 = 4.

Note: If other bits are on during this input, the 3705 control program must take appropriate action to service the condition indicated by the bit.

See H-270 for a sequence chart for this operation and the channel service cycle.

The Output X'62' instruction initiates a channel service cycle to transfer the data from the host CPU to the CA EB/CS local store.



The type 4 CA provides the capability of transferring 4, 8, 16, or 32 byte bursts of data—the selection made by a CE-installed jumper. The EB address counter steps as each data byte transfers to the EB local store. 'Count 2' falls after four data bytes have been transferred ('count 4' after eight, 'count 8' after sixteen) to set the 'delay service in' latch. This latch is not set for a thirty-two byte burst. Op In resets to drop the CA off the channel and a delay counter starts. A CE-installed jumper selects how much delay occurs before the CA raises Request In to continue transferring data to the EB local store.

INBOUND DATA TRANSFERS—EB/CS MODE (PART 2)

BSC Control Character Recognition in ESC Mode

ETB and ETX (EBCDIC or USASCII)

The type 4 CA, when in EB/CS mode and the ESC (emulator sub-channel) mode is enabled, recognizes BSC control characters ETB and ETX and sets the 'svc stop or disc' latch 1. This resets the 'initiate service cycle' latch and causes a CA4 data/status L3 interrupt. An Input X'62', executed when the level 3 interrupt is serviced, transfers bit 0.5 (service stop) to a specified CCU general register for 3705 control program use.

DLE-STX (EBCDIC or USASCII)

The type 4 CA, when in EB/CS mode and the ESC mode is enabled, recognizes the DLE-STX control-character sequence (indicating the start of transparent data) and resets the EBCDIC, USASCII, and DLE monitor latches 2 to prevent monitoring the transparent data. An Input X'6C', executed when the level 3 interrupt is serviced, transfers zeros for USASCII and EBCDIC monitor control bits 0.6 and 0.7 to a specified CCU general register for 3705 control program use.

If the DLE control character is the last character of one inbound-data transfer sequence, bit 0.5 ('DLE remember' latch) will be on in a specified CCU general register after the Input X'6C' instruction is performed. The 3705 control program must set the 'DLE remember' latch (bit 0.5=1) when the Output X'6C' instruction is executed for the next inbound-data transfer sequence for the subject address. If an STX control character is the first character of the next inbound-data transfer sequence, the EBCDIC, USASCII, and DLE monitor latches are reset to prevent monitoring the transparent data for ending characters.

SYN (EBCDIC or USASCII)

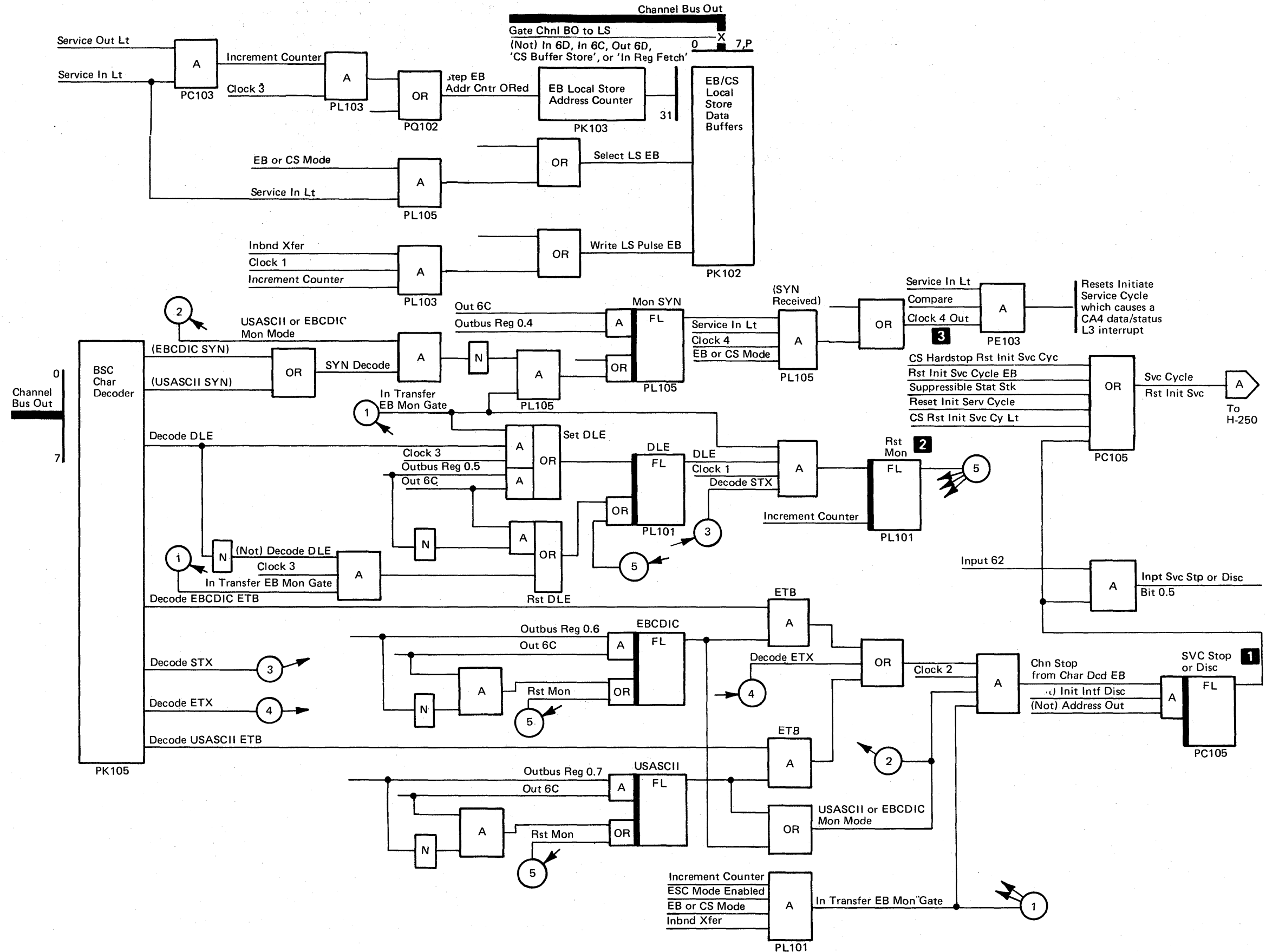
Some programs use SYN characters as time fill characters. The type 4 CA recognizes these consecutive SYN characters as "fill" characters and frees the channel to service other devices.

The type 4 CA, when in EB/CS mode and the ESC mode is enabled, monitors for SYN characters if the 'monitor SYN' latch is on. The Output X'62' that requested the inbound-data transfer sequence also sets the non-EB/CS byte-transfer count with the number of consecutive SYN characters that are to be received before the CA4 disconnects from the channel. When the number of consecutive SYN characters received from the channel equals the number in the non-EB/CS byte-transfer count, the CA4 resets the 'initiate service cycle' latch and causes a CA4 Data/status L3 interrupt 3. An Input X'6C', executed when the level 3 interrupt is serviced, transfers bit 0.4 ('SYN monitor control' latch) to a specified CCU general register for 3705 control program use.

A non-SYN character resets the 'monitor SYN' latch and monitoring for SYN characters ceases and normal controls for terminating the sequence take over.

BSC Control Character	EBCDIC Hex	USASCII Hex
STX	02	02
ETX	03	03
DLE	10	10
SYN	32	16
ETB	26	17

USASCII monitor mode ignores channel bus out bit 0 when decoding the control characters.

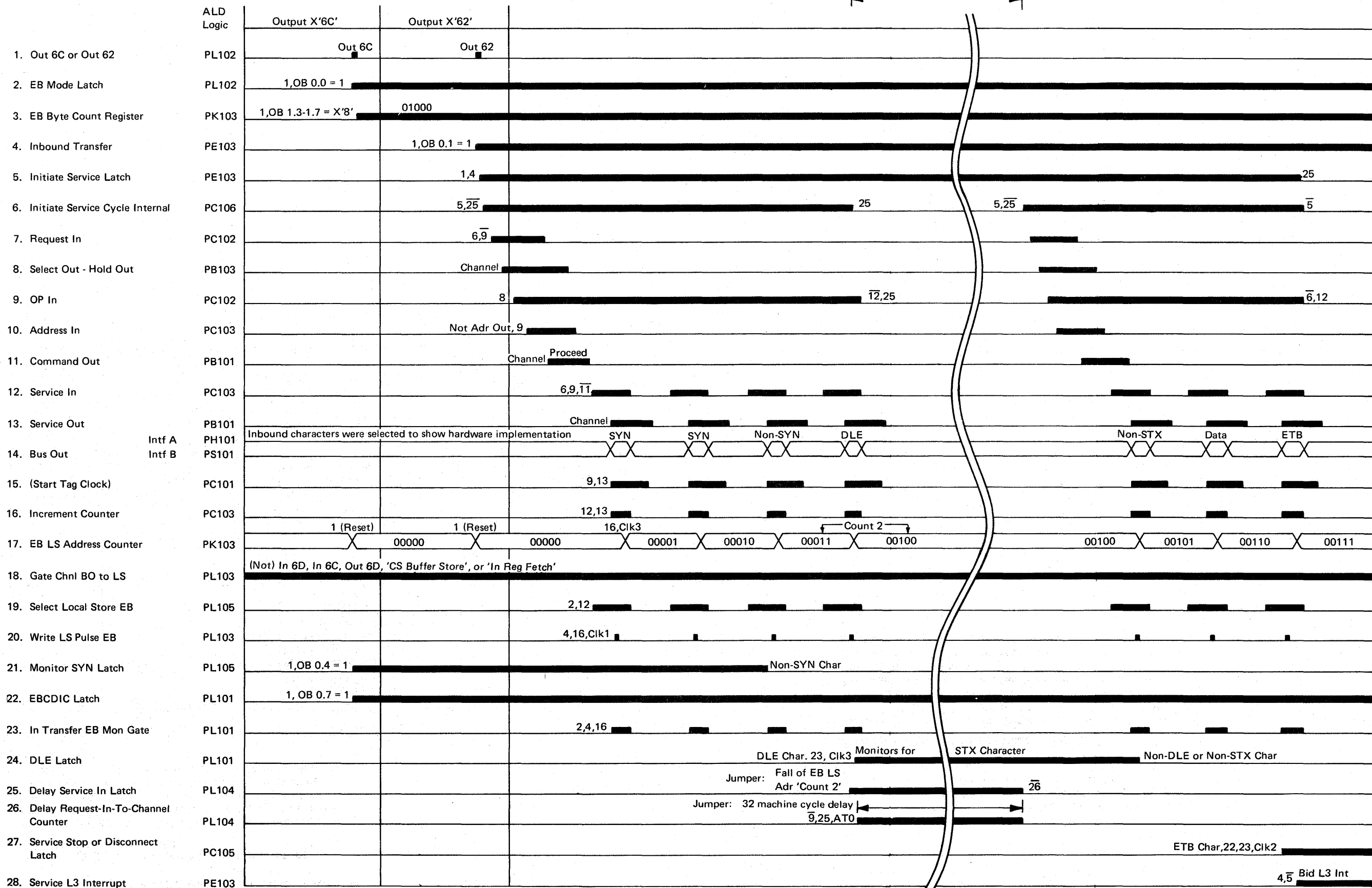


Increment Counter
ESC Mode Enabled
EB or CS Mode
Inbnd Xfer

INBOUND DATA TRANSFERS—EB MODE (PART 3)

Sequence Chart for the Channel Service Cycle

Any Start I/O to this channel interface during this delay of Service In receives an initial selection status of X'70' (CCU Busy).



This sequence continues to H-290 for the sequence of transferring the data now in the EB/CS local store data buffers to a CCU general register.

See H-140 for Output X'6C' 2nd level logic

INBOUND DATA TRANSFERS—EB MODE (PART 4)

Transferring Data From the EB/CS Local Store to the CCU General Register

In response to the type 4 CA data/status level 3 interrupt, the 3705 control program must execute the following instructions. The 3705 control program uses the transferred byte count from the Input X'6C' instruction to determine how many Input X'6D' instructions are required to input all the data—four in this example.

Instruction	General Register Bits		Indication or Function
	Byte 0	Byte 1	
Input X'77'	0000 0000	1001 0000	1.0 = type 4 CA L3 Interrupt 1.3 = selected type 4 CA data/status interrupt 1.6 = 0 type 4 CA #1 selected
Input X'63'	Address	0000 0000	Byte 0 = subchannel address Byte 1 = all zeros
Input X'62'	0100 0100	0000 0XXX	0.1 = inbound data transfer 0.5 = service stop condition—the control program should end the channel command 1.5-1.7 not used for EB mode
Input X'6C'	1000 0001	0000 0111	0.0 = extended buffer mode 0.7 = EBCDIC monitor control latch 1.2-1.7 = 7 transferred byte count—EB mode
Minimum of one cycle delay after Input X'6C'			
Input X'6D'	0011 0010	0011 0010	Byte 0 = SYN character Byte 1 = SYN character
Minimum of one cycle delay after Input X'6D'			
Input X'6D'	XXXX XXXX	0001 0000	Byte 0 = non-SYN character Byte 1 = DLE character
Minimum of one cycle delay after Input X'6D'			
Input X'6D'	YYYY YYYY	ZZZZ ZZZZ	Byte 0 = non-STX character Byte 1 = data character
Minimum of one cycle delay after Input X'6D'			
Input X'6D'	0010 0110	WWWW WWWW	Byte 0 = ETB character Byte 1 = non-data
Minimum of one cycle delay after Input X'6D'			
Output X'6C'	0000 0000	0000 0000	0.0 = reset extended buffer mode 0.7 = 0 reset EBCDIC monitor control latch.

See H-290 for a sequence chart for this operation.

If the ETB character had not ended the data transfer (as in our example) by a service stop, the 3705 control program would continue the data transfer after the eight data bytes were transferred to a CCU general register by repeating the sequence starting on H-270.

Ending an Inbound-Data Transfer—EB Mode

The ending of an inbound-data transfer in EB mode is identical to that of the type 1 CA except for the type 4 CA recognition of the BSC control characters as described on page H-260.

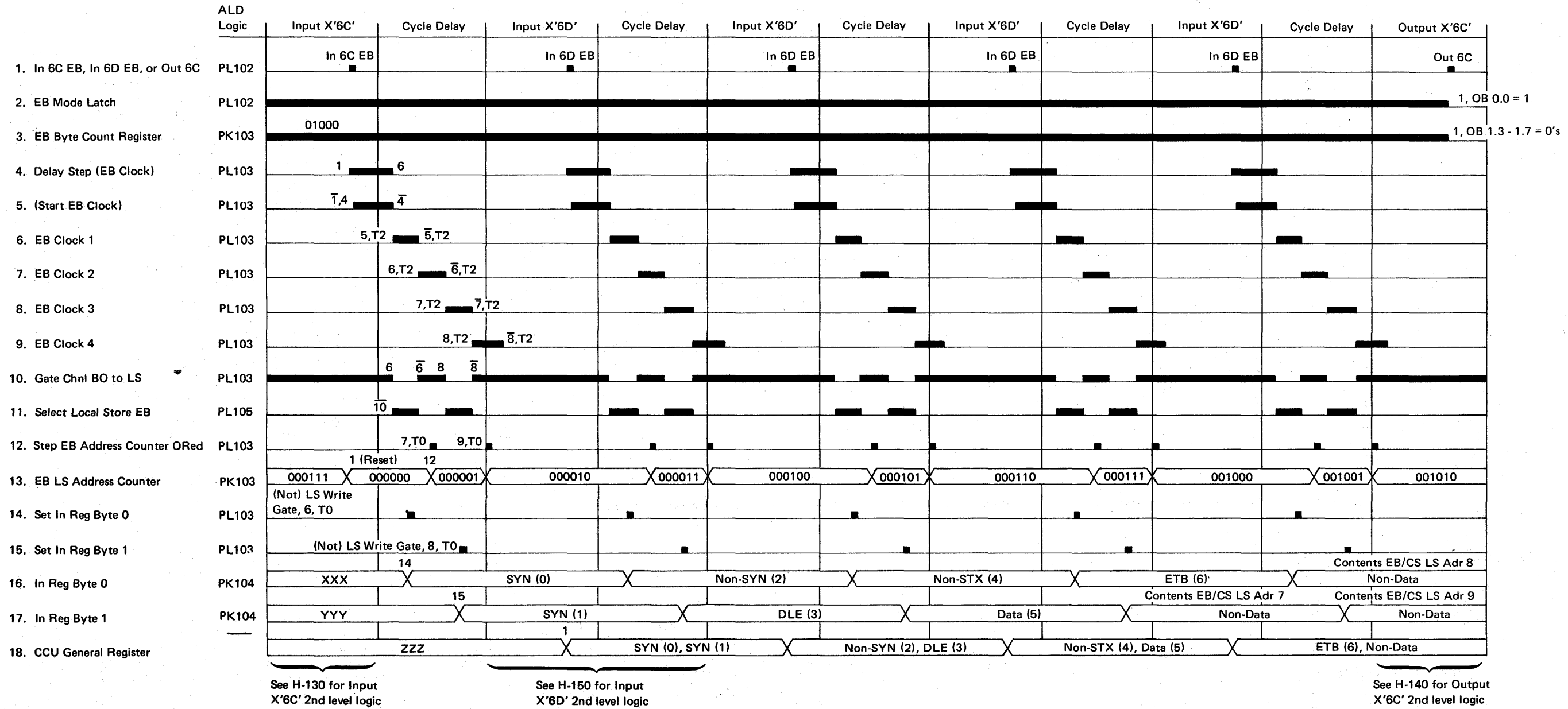
See page 8-280 for endings other than the recognition of the BSC control characters.

See page 8-290 (ESC) for endings caused by the recognition of the BSC control characters (as in the example).

INBOUND DATA TRANSFERS—EB MODE (PART 5)

Sequence Chart for Inputting the EB/CS Local Store (Data Buffer)

Continued from H-270



CYCLE STEAL OPERATION—OUTBOUND DATA TRANSFERS

Introduction

During an outbound data transfer, the CA4 transfers data from CCU storage to the EB/CS local-store data buffers by cycle stealing. Only EB/CS local-store data buffer addresses 0 and 1 are used during cycle stealing. Cycle stealing always transfers the two data bytes obtained from storage to the EB/CS local-store data buffers. However, if the starting address in CSAR is an odd address, the CA4 only transfers byte 1 to the channel. All subsequent data is transferred two bytes at a time unless the outbound data transfer ends by only transferring byte 0.

The CA4 cycle steals two data bytes to EB/CS local-store data buffers 0 and 1 then raises 'Request In' to request a channel service cycle to transfer these two bytes to the channel. The CA4 then blocks 'Service In' while the CA4 cycle steals two more data bytes. The CA4 then allows 'Service In' to transfer these two data bytes to the channel. This operation continues until the number of bytes transferred equals the specified CS byte count and a data/status level 3 interrupt is requested.

The CA4 removes the hold on Request In and a channel service cycle transfers data 0 and then data 1 to the channel. If an odd starting address had initially been loaded into SAR by Output X'6F', the 'odd byte control' latch 10 would have also been set. This latch steps the 'EB address counter' and the 'byte 0 control' latch so the first Service In transfers data byte 1 instead of data byte 0. In either case, the signal 'in full or out empty' 11 restarts the cycle steal operation for the next two bytes of data. The CA4 does not disconnect from the channel while cycle stealing the next two bytes of data. The CA4 does block Service In 12 until the cycle steal operation is completed.

Every time Service In transfers a data byte to the channel, the CA4 steps the 'CS byte counter' 13. When the number of data bytes actually transferred equals the desired byte count, the CA4 resets the initiate service cycle latch 14 and requests a data/service level 3 interrupt 15.

Initializing the Cycle Steal Operation

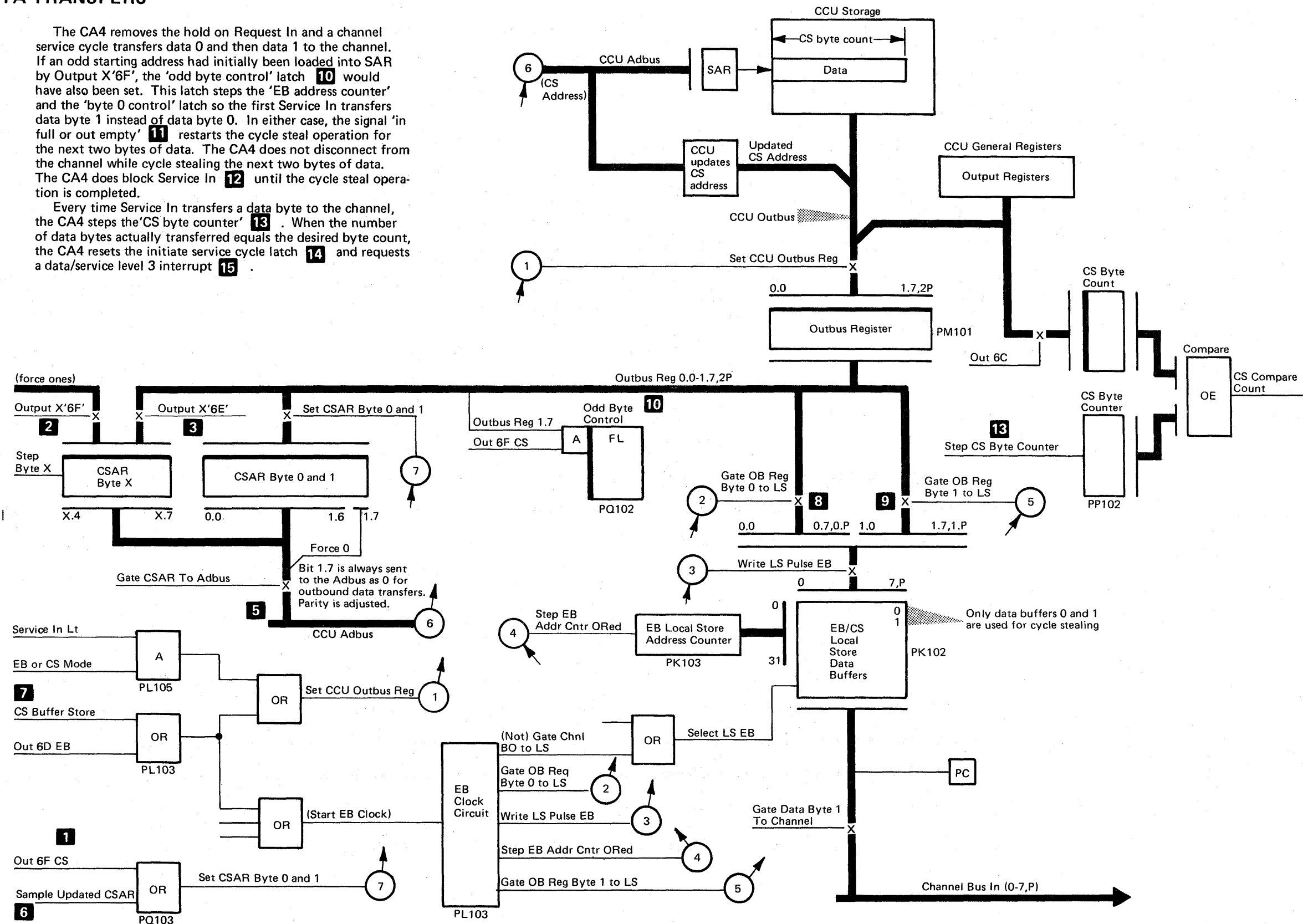
The 3705 control program executes an:

- Output X'6C' to load the 'CS byte count' register with the desired number of data bytes to be passed during the channel transfer and to set 'CS mode'.
- Output X'6F' to load CSAR byte 0 and 1 with the storage address of the location containing the first byte of data to be transferred by cycle stealing 1. CSAR byte X is forced to ones and then stepped to zeros to save executing Output X'6E' if the extended address bits are zeros. 2
- Output X'6E' to load CSAR byte X if the extended address bits X.4-X.7 are not zeros. 3
- Output X'62' to set (1) outbound data transfer, (2) the 'priority outbound-data transfer sequence' (if desired) and (3) the 'CS proceed' latch to start the cycle steal operation.

Details of Cycle Stealing Operation

The key numbers in the paragraphs below refer to the data flow diagram on this page and/or the CS sequence chart on H-320.

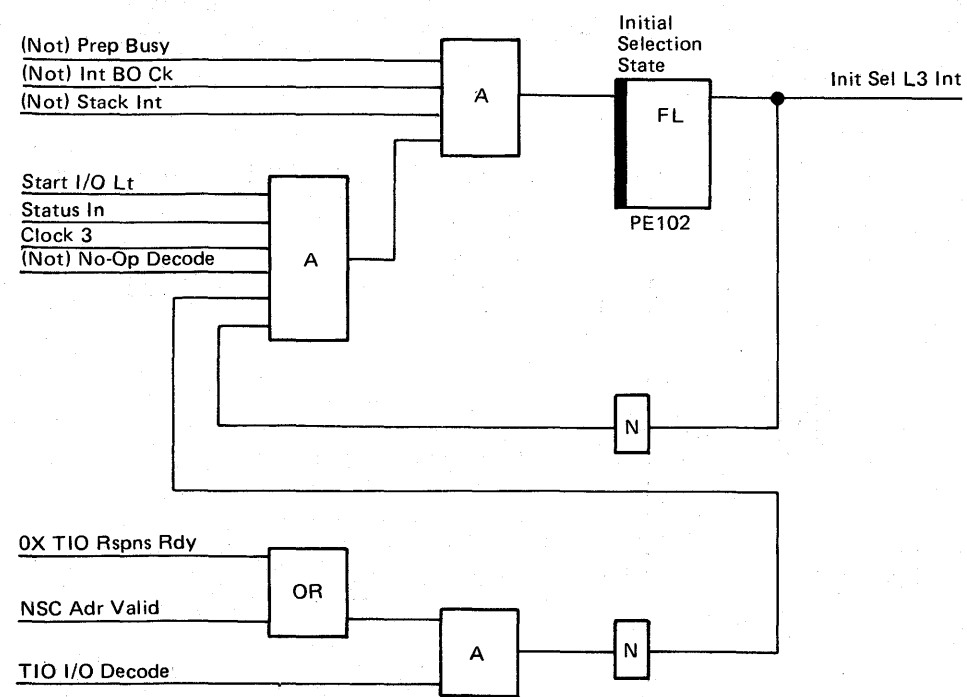
Once 'CS proceed' is active, the CA4 blocks Request In 4. After the CA4 has bid for a cycle-steal machine cycle and the CCU responds with 'go channel 1', the CA4 gates the address in CSAR 5 (on a half-word boundary) to SAR so the CCU can obtain the half word of data during the cycle steal machine storage read. The CCU increments the address by two and places it on the 'CCU outbus'. The CA4, unlike CA2, CA3, or the type 3 scanner, does not update CSAR but reloads CSAR with the updated address from the CCU 6. 'CS buffer store' 7 signals the CA4 to load data byte 0 into EB/CS LS buffer address 0 8 and data byte 1 into buffer address 1 9 and then reset the 'EB LS address counter'.



OUTBOUND DATA TRANSFERS—CS MODE

Outbound data transfers result from channel Read commands that direct the transfer of data from 3705 storage to the host CPU. When the CA is in cycle steal mode, the CA4 does not require control program intervention (once cycle stealing has been initialized) until the channel data transfer has been completed and the CA4 requests a level 3 interrupt. The fetching of data from CCU storage is automatically done by the cycle steal hardware whether the CA4 is in ESC or NSC mode.

CA DECODES THE COMMAND AND REQUESTS AN INTERRUPT



The 3705 control program responds to the initial select level 3 interrupt with the following instructions.

Instruction	General Register Bits		Indication or Function
	Byte 0	Byte 1	
Input X'77'	0000 0000	1000 10X0	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected = 1 type 4 CA #2 selected
Input X'60'	1000 0000	0000 0000	Normal initial selection (Note 1)
Input X'61'	address	command	Byte 0 = address Byte 1 = command
Output X'63'	address	0000 0000	Byte 0 = transfer address Byte 1 = all zeros
Output X'6C'	0100 0000	0000 0111	0.1 = set cycle steal mode 1.0-1.7 = X'03' to transfer three data bytes out (Note 2) Resets EB adr counter to adr 00
Output X'6F'	address	address	Byte 0 = CSAR byte 0 Byte 1 = CSAR byte 1 Resets CSAR byte X Sets 'odd byte control' latch if CSAR bit 1.7=1
Output X'6E'	0000 0000	0000 XXXX	Byte 0 = all zeros Byte 1 bits 4-7 = extended address bits for CSAR byte X
Output X'62'	1000 0100	0000 0100	0.0 = outbound data transfer 0.5 = reset 'initial select state' 1.5 = set priority outbound-data transfer sequence Sets 'CS proceed' latch to start the cycle steal operation

Initial Selection Address In and Status In Response

This instruction is not needed if the extended address bits X.4, X.5, X.6 and X.7 are zeros.

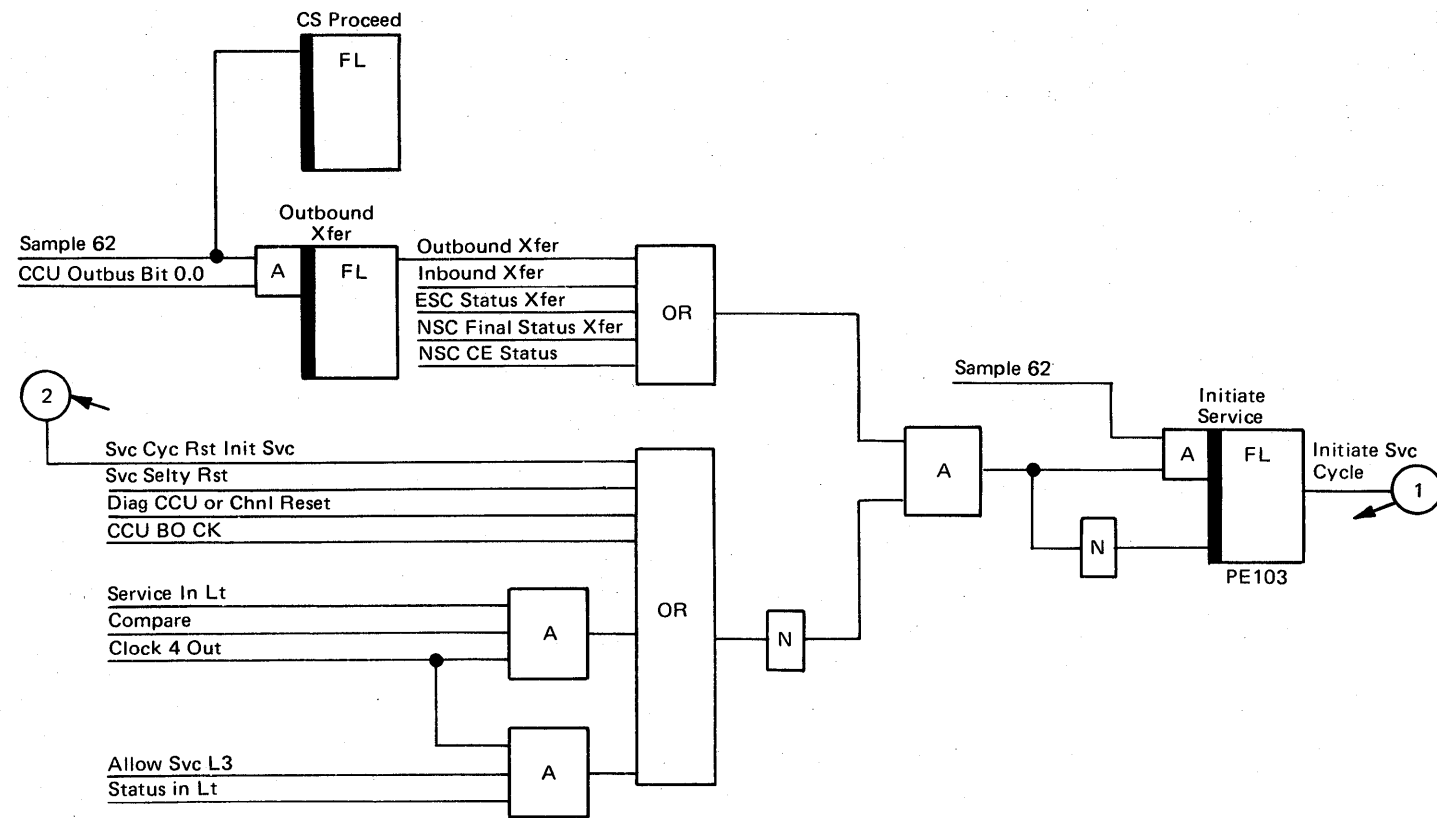
Outbound transfer initiates a channel data service cycle. See H-330 for a sequence chart for this operation and the channel service cycle.

- Notes:
1. Other bits may be transferred to the CCU during this input. If other bits are on, the 3705 control program must take action differently from the normal initial selection.
 2. From 1 to 256 bytes of data may be transferred to the channel.

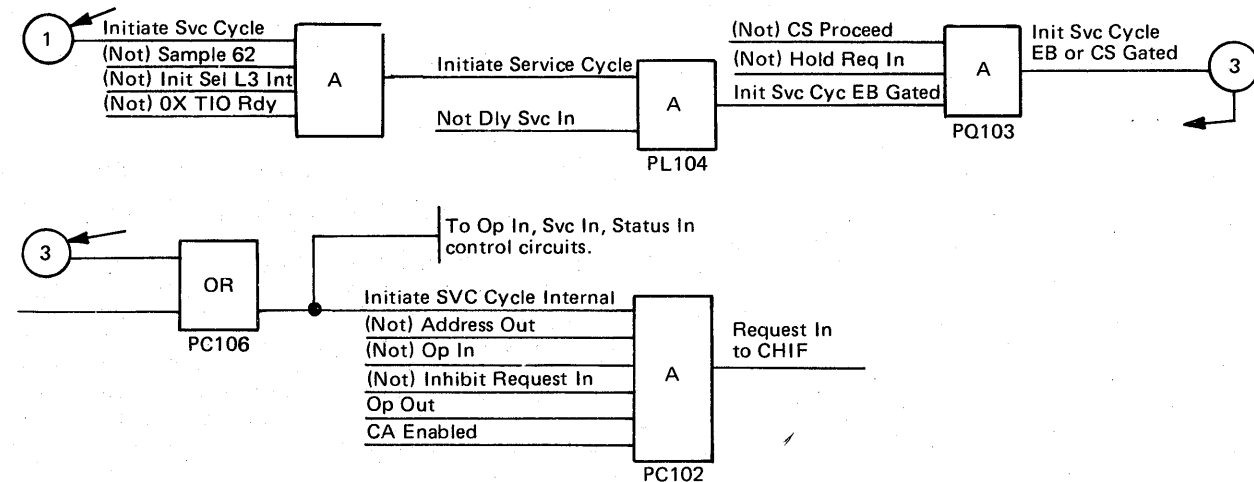
OUTBOUND DATA TRANSFERS—CS MODE (PART 2)

CA to Channel Data Transfer—See H-300 for Sequence Chart

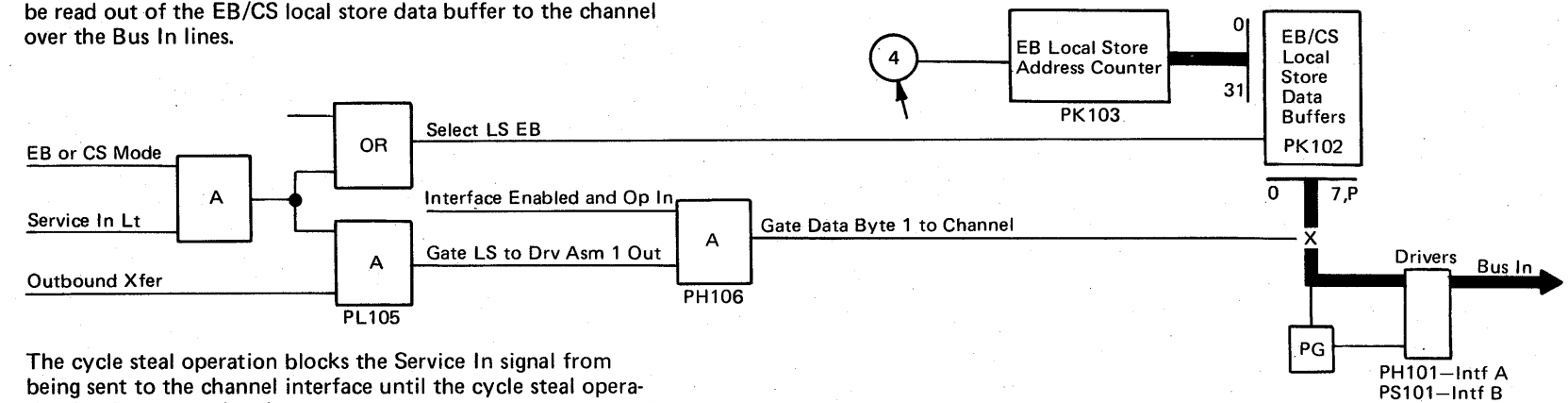
The Output X'62' instruction starts (1) a cycle steal operation that loads two bytes of data into the EB/CS local store and (2) a channel service cycle so that the data loaded into the EB/CS local store can be transferred to the channel.



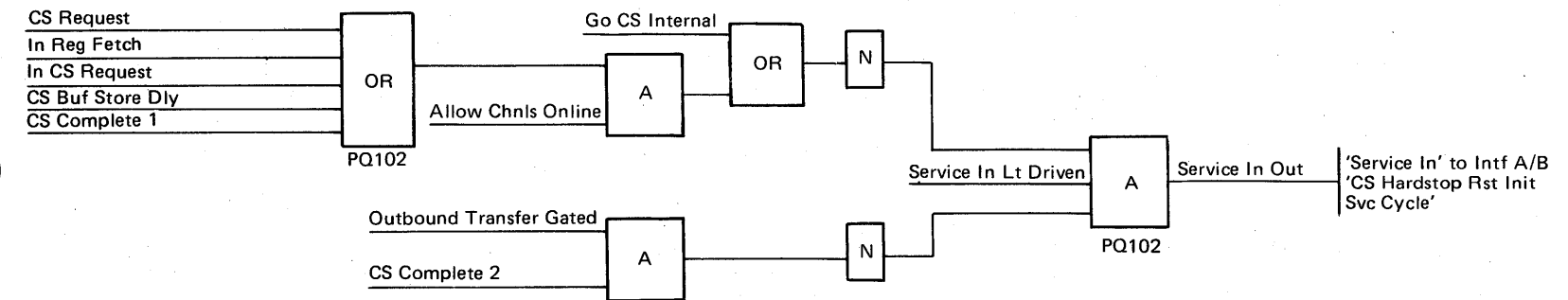
The CA4 sends Request In to the channel to start the service cycle.



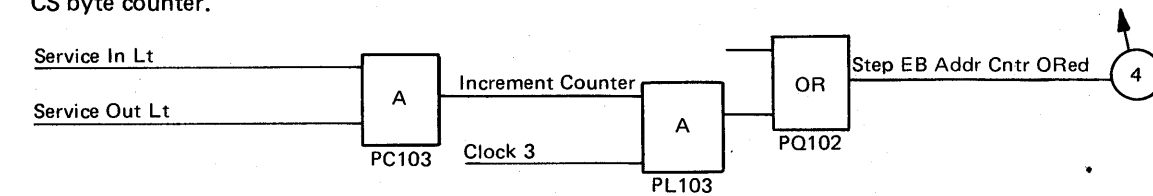
When the Service In latch is set, it causes the next data byte to be read out of the EB/CS local store data buffer to the channel over the Bus In lines.



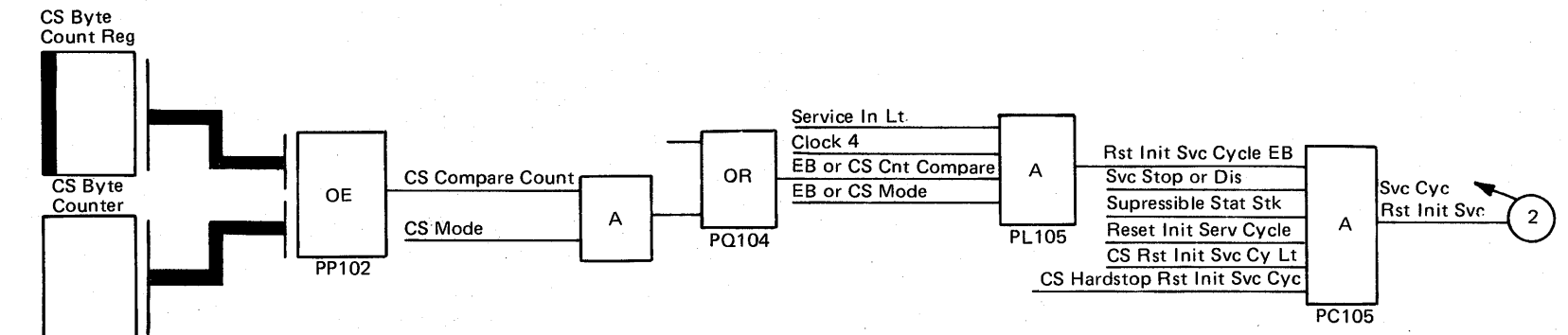
The cycle steal operation blocks the Service In signal from being sent to the channel interface until the cycle steal operation has been completed.



When the channel returns Service Out, the channel tag clock operates to synchronize the CA and channel. Service Out also increments the EB local store address counter and steps the CS byte counter.

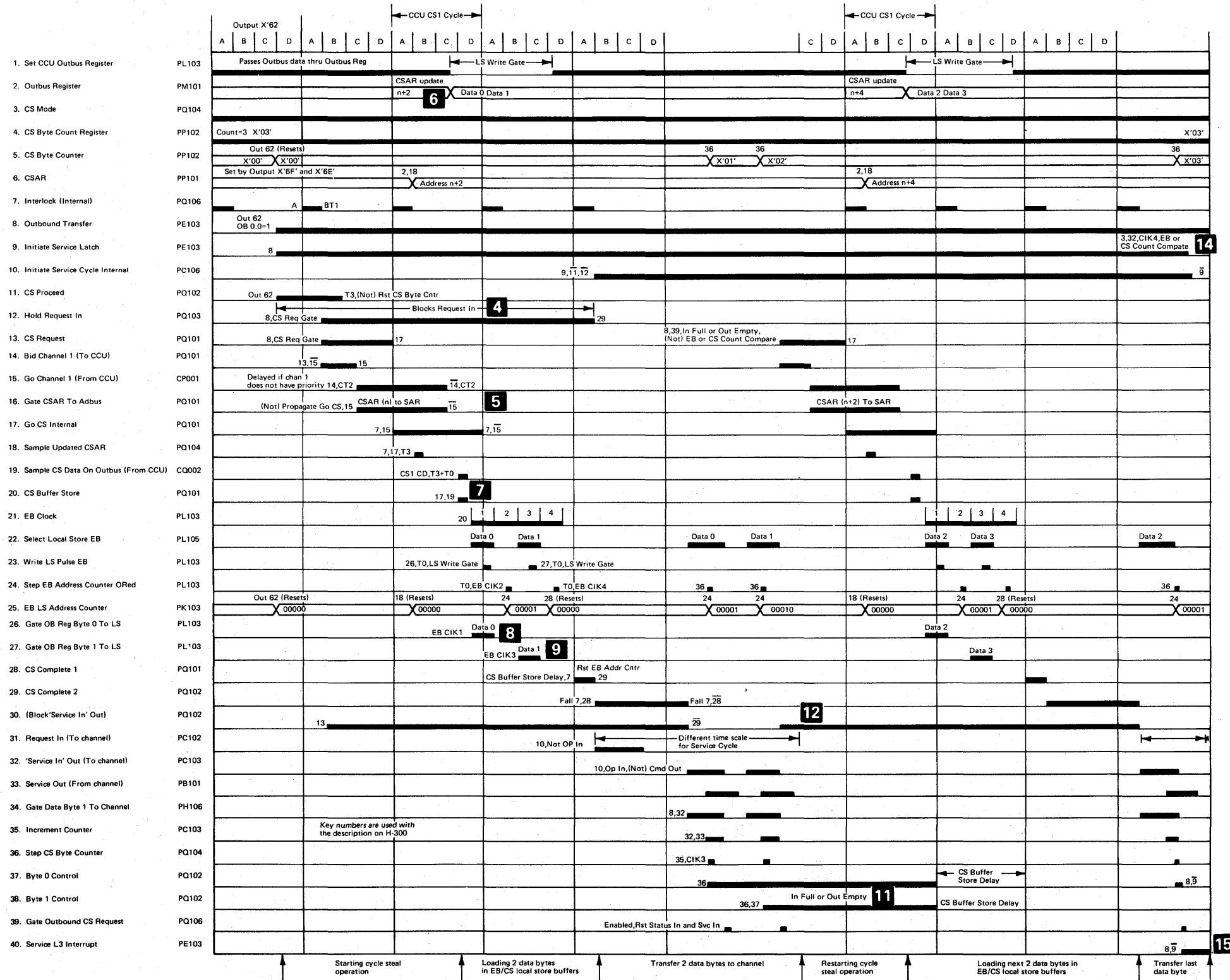


The data transfer stops when the value of the CS byte counter equals the byte count to be transferred in the CS byte count register.



OUTBOUND DATA TRANSFERS—CS MODE (PART 3)

CS SEQUENCE CHART—OUTBOUND



This sequence continues into the automatic CA4 selection by priority sequence chart on H-240 that is applicable if two type 4 CAs are installed. If only one type 4 CA is installed, the operation is the same as for the type 1 CA (See page 8-330 for the control program response to the level 3 data/status interrupt).

CYCLE STEAL OPERATION—INBOUND DATA TRANSFERS

Introduction

During an inbound data transfer, the CA4 transfers data from the EB/CS local-store data buffers to CCU storage by cycle stealing. Only EB/CS local-store data buffer addresses 0 and 1 are used during cycle stealing. Cycle stealing always transfers the two data bytes obtained from the EB/CS LS data buffers to storage. However, if the starting address in CSAR is an odd address, the CCU stores data byte 1 (from the channel) and rewrites storage byte 0 in storage. All subsequent data is transferred two bytes at a time unless the inbound-data transfer ends by only transferring data byte 0. In this case, the CCU stores data byte 0 (from the channel) and rewrites storage byte 1 in storage.

The CA4 raises 'Request In' to start a data service cycle so that the channel can transfer one or two data bytes to the EB/CS LS data buffer. The CA4 then starts a cycle steal operation that loads the In register with the contents of the EB/CS LS data buffers 0 and 1. The CA4 requests that the CCU take a cycle-steal machine cycle to store the data in the In register at the address sent to the CCU over the Adbus and whether to store byte 0, byte 1 or bytes 0 and 1. The CCU updates the address and sends it back to the CA4 where it is loaded into CSAR. During the cycle steal operation, the CA4 blocks the 'Service In' signal from being sent to the channel. Once the cycle steal operation is completed, 'Service In' is sent "out" to the channel and the channel resumes transferring two more data bytes to the EB/CS LS data buffer. This operation continues until a BSC ending control character is detected in the data from the channel or the number of data bytes received equals the specified CS byte count and then the CA4 requests a level 3 interrupt.

Initializing the Cycle Steal Operation

The 3705 control program executes an:

- Output X'6C' to load the 'CS byte count' register with (1) the expected number of data bytes to be received during the channel transfer or (2) a byte count in excess of the expected number of data bytes where a BSC ending control character normally ends the data transfer. Output X'6C' sets 'CS mode' and also sets the BSC monitor control latches if they are desired.
- Output X'6E' to load CSAR byte X if the extended address bits X.4-X.7 are not zeros **3**. CSAR byte X is forced to ones and then stepped to zeros to save executing Output X'6E' if the extended address bits are zeros **2**.
- Output X'6E' to load CSAR byte X if the extended address bits X.6 and X.7 are not zeros **3**.
- Output X'62' to set (1) inbound data transfer and (2) the 'CS proceed' latch to start the cycle steal operation.

Details of the Cycle Stealing Operation

The key numbers in the paragraphs below refer to the data-flow diagram on this page and/or the CS sequence chart on H-360.

The CA4 raises 'Request In' to start a data service cycle. The example illustrated in the CS sequence chart on H-360 assumes that the address in CSAR points to an odd boundary, therefore Output X'6F' sets the 'odd byte control' latch **4**.

This latch steps the EB address counter to 1 and sets 'byte 0 control' so that the first data byte transferred by the channel is loaded in EB/CS LS data buffer 1. The CA4 (1) steps the CS byte counter to one (2) turns on 'byte 1 control' to indicate that the buffer is full, (3) turns on 'CS request' to bid for a CS1 machine cycle, and (4) blocks sending 'Service In' to the channel. 'In reg fetch' **5** resets the EB LS address counter to 0 and starts the EB clock. This loads the contents of buffer 0 (old data) into In register byte 0 and data byte 1 (STX) from buffer 1 into In register byte 1 **6**.

The CCU returns 'go chan 1' when the next machine cycle will be a CS1 machine cycle. The CA4 then sends all 20 bits of the address from CSAR to SAR over the CS abus **7** and sends 'store byte 1' to signal the CCU that only data byte 1 is to be stored. The CA4 gates the In register contents to SDR (storage data register) byte 1 from which data byte 1 is stored.

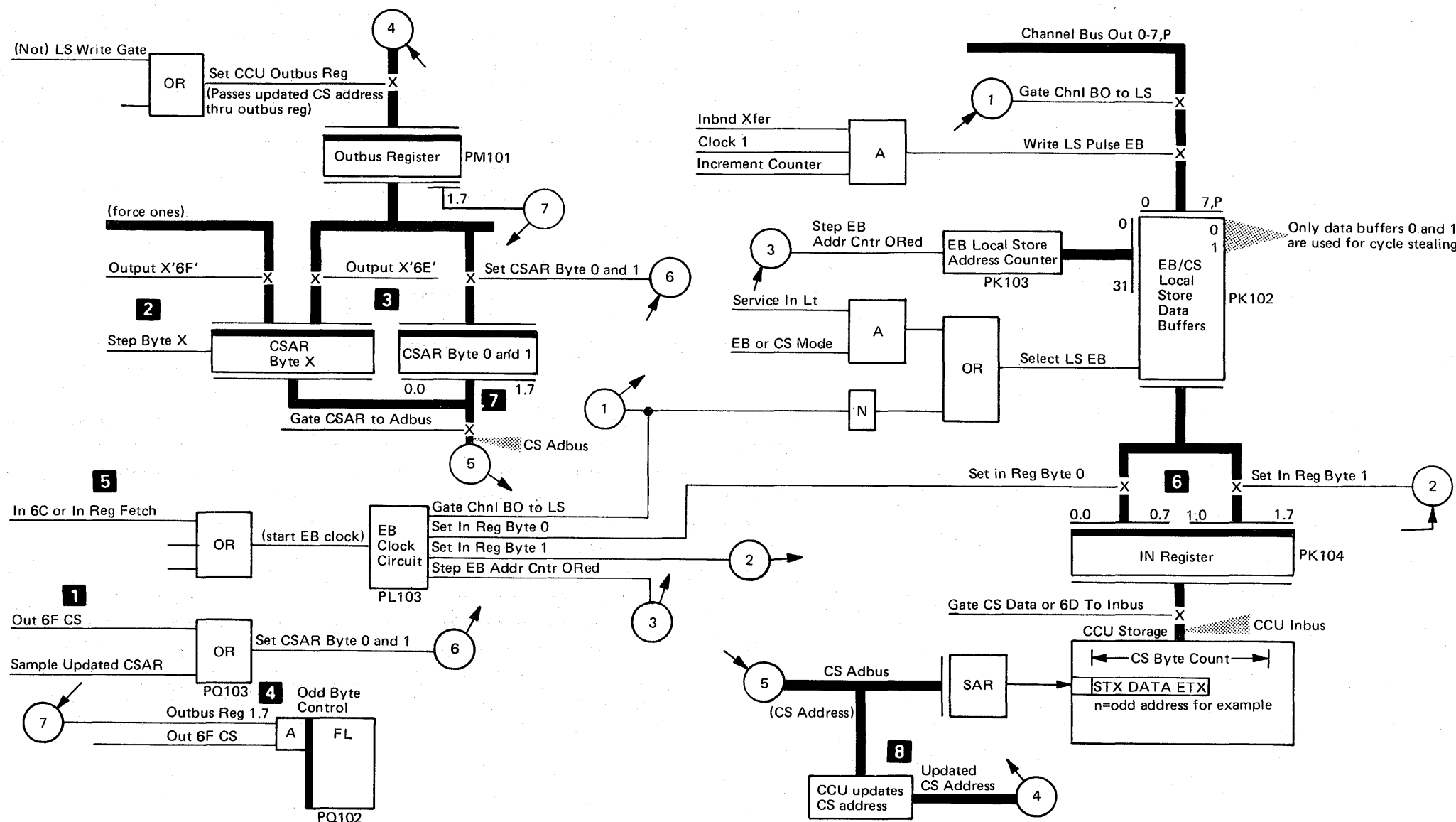
The CCU updates the address to an even address by incrementing by one or two **8** (depending on how many bytes were stored) and returns the address (16 bits) over the CCU outbus. The CA4 then loads the updated address into CSAR bytes 0 and 1. Since byte X of the updated address is not returned, the CA4 must update CSAR byte X if a carry from bit 0.0 to X.7 occurred during the CCU update. The CA4 knows a carry occurred if the updated address on the CCU outbus equals zero when sampling the updated CSAR and steps CSAR byte X.

The CA4 sends 'Service In' to the channel **9** when the cycle steal operation has been completed. The data service cycle resumes and the channel transfers the next two data bytes to EB/CS LS data buffers 0 and 1. This service cycle operation is the same operation that occurs when the starting CS address is even and the 'odd byte control' latch is off. Aside from loading two data bytes instead of one, this service cycle and cycle

steal operation is identical to that described above except that 'store byte 0' and 'store byte 1' signals are both sent to the CCU when the CSAR address is sent to SAR **10**.

The CA4 monitors the data transferred from the channel for BSC ending control characters ETB or ETX when in ESC mode and the monitor control latches are set. If either of these ending characters is detected **11** on the channel Bus Out, the CA4 sets the 'service stop or disconnect' latch that resets the 'initiate service' latch stopping the service cycle and requests a level 3 interrupt. (See H-260). **12**

Every time Service Out transfers a data byte from the channel, the CA4 steps the 'CS byte counter'. When the number of data bytes received equals the desired count in the 'CS byte count' register, the CA4 raises 'reset initiate service cycle EB' that resets the 'initiate service cycle' latch stopping the service cycle and requests a level 3 interrupt.

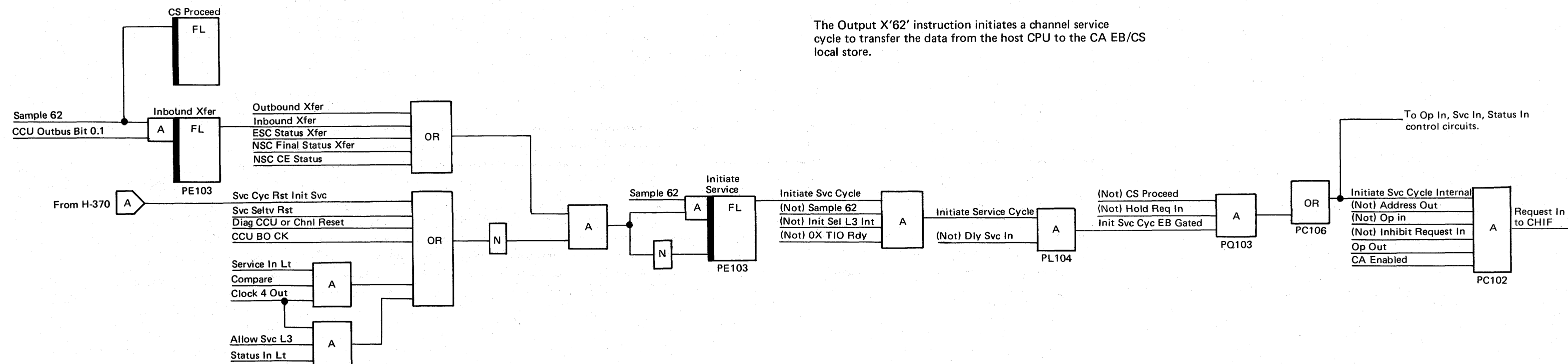
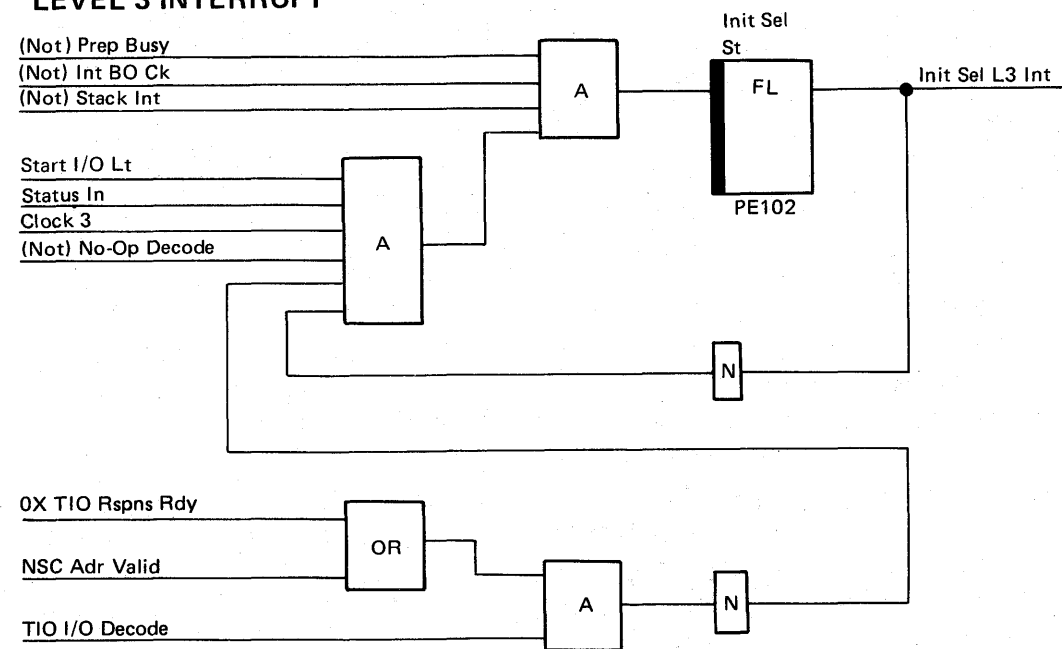


INBOUND DATA TRANSFERS—CS MODE

Inbound data transfers result from commands that require the passing of data from the host CPU to 3705 storage.

When the commands are decoded, they request an initial selection level 3 interrupt so that the 3705 control program can determine what action to take to service the command. The commands start an initial selection sequence as shown on 8-170.

CA REQUESTS AN INITIAL SELECTION LEVEL 3 INTERRUPT



CONTROL PROGRAM RESPONDS TO THE INTERRUPT

The 3705 control program responds to the initial selection level 3 interrupt with the following sequence of instructions.

Instruction	General Register Bits		Indication or Function
	Byte 0	Byte 1	
Input X'77'	0000 0000	1000 1000	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected
Input X'60'	1000 0000	0000 0000	Normal initial selection*
Input X'61'	Address	Command	Byte 0 = subchannel address Byte 1 = command
Output X'63'	Address	0000 0000	Byte 0 = address Byte 1 = all zeros
Output X'6C'	0100 1001	0000 1000	0.1 = set cycle steal mode 0.4 = set SYN monitor control latch 0.7 = set EBCDIC monitor control latch 1.0-1.7 = X'08' to transfer eight data bytes Resets EB adr counter to adr 00
Output X'6F'	Address	Address	Byte 0 = CSAR byte 0 Byte 1 = CSAR byte 1 Resets CSAR byte X Sets 'odd byte control' latch if CSAR bit 1.7=1
Output X'6E'	0000 0000	0000 XXXX	Byte 0 = all zeros Byte 1 bits 4-7 = extended address bits for CSAR byte X
Output X'62'	0100 0110	0000 0000	0.1 = inbound data transfer 0.5 = reset initial selection 0.6 = reset data/status control 1.6-1.7 = 0; check for 4 SYN chars Sets 'CS proceed' latch to start the cycle steal operation

Initial selection Address In and Status In response

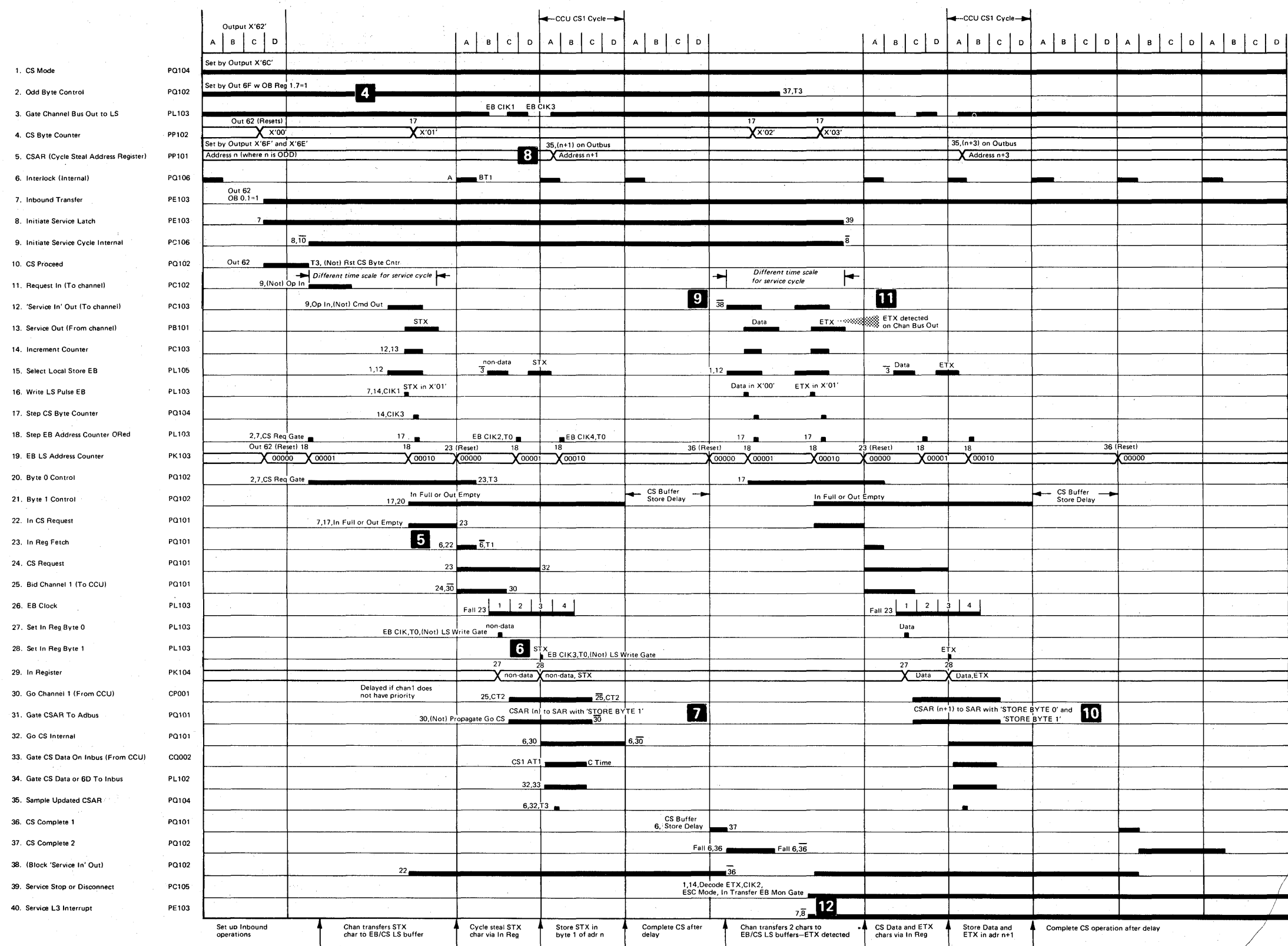
This instruction is not needed if the extended address bits X.4, X.5, X.6 and X.7 are zeros.

Inbound transfer initiates a channel data service cycle 'CS proceed' initiates a cycle steal operation. See H-360 for the combined sequence of operation assuming the CS begins on an odd byte address.

*If other bits are on during this input, the 3705 control program must take appropriate action to service the condition indicated by the bit..

The Output X'62' instruction initiates a channel service cycle to transfer the data from the host CPU to the CA EB/CS local store.

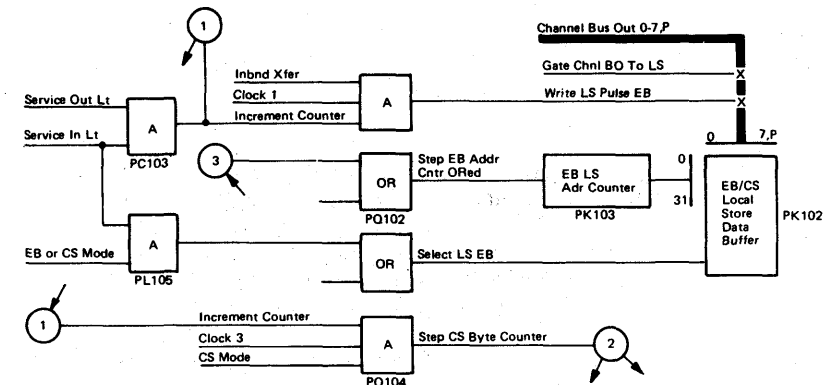
INBOUND DATA TRANSFERS—CS MODE (PART 2)
CS SEQUENCE CHART—INBOUND



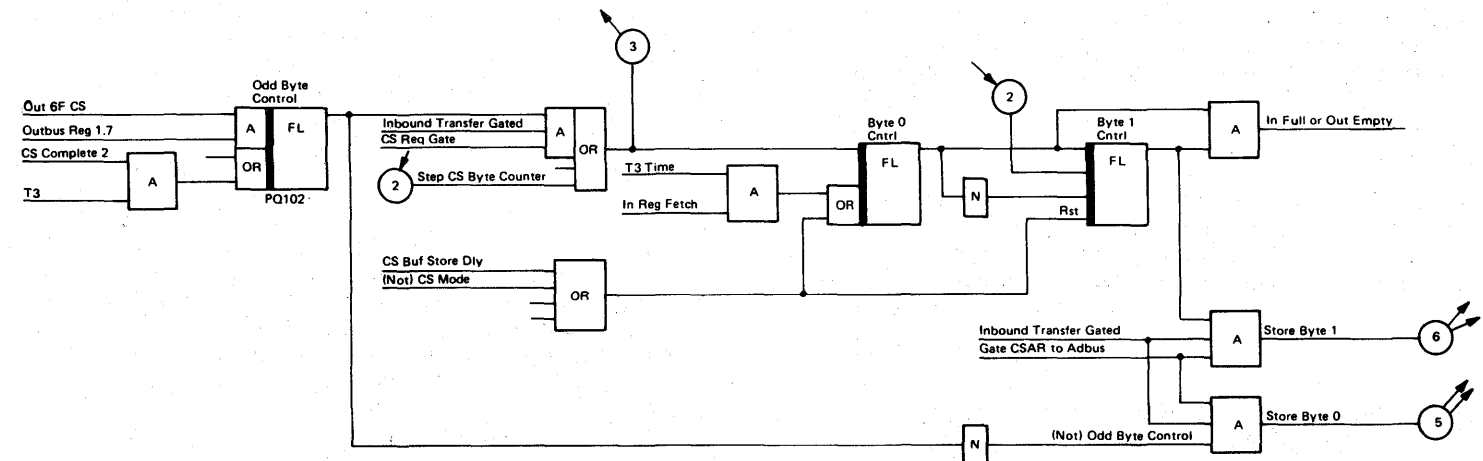
INBOUND DATA TRANSFERS—CS MODE (PART 3)

See H-360 Sequence Chart

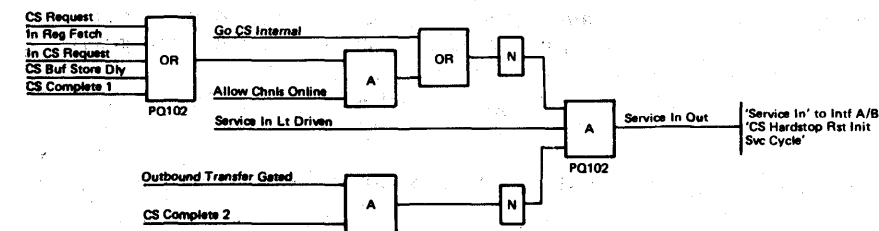
When the channel returns Service Out in response to Service In, the channel tag clock operates to synchronize the CA4 and channel. The CA4 writes the data byte on channel Bus Out into the EB/CS LS data buffer and then steps the EB local-store address counter.



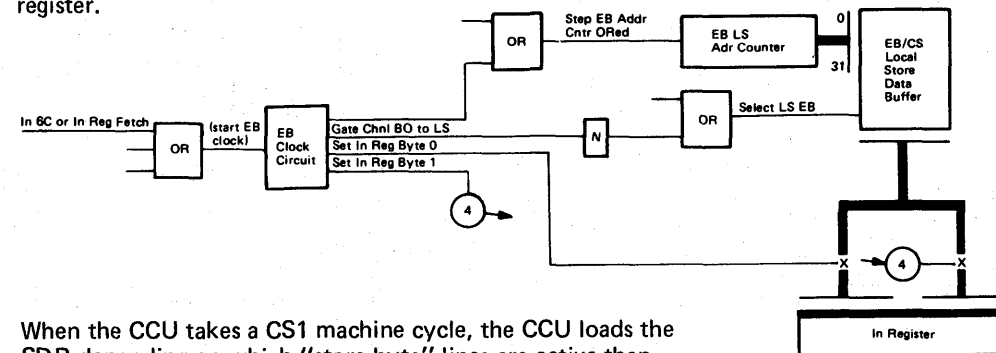
In our example the starting address in CSAR is odd, therefore the 'odd byte control' latch had set the 'byte 0 control' latch and had stepped the EB address counter to 1. When the first data byte is written into the EB/CS LS data buffer, the CA4 steps the CS byte counter and sets the 'byte 1 control' latch. This indicates that the data buffers are filled and signals for a cycle steal operation.



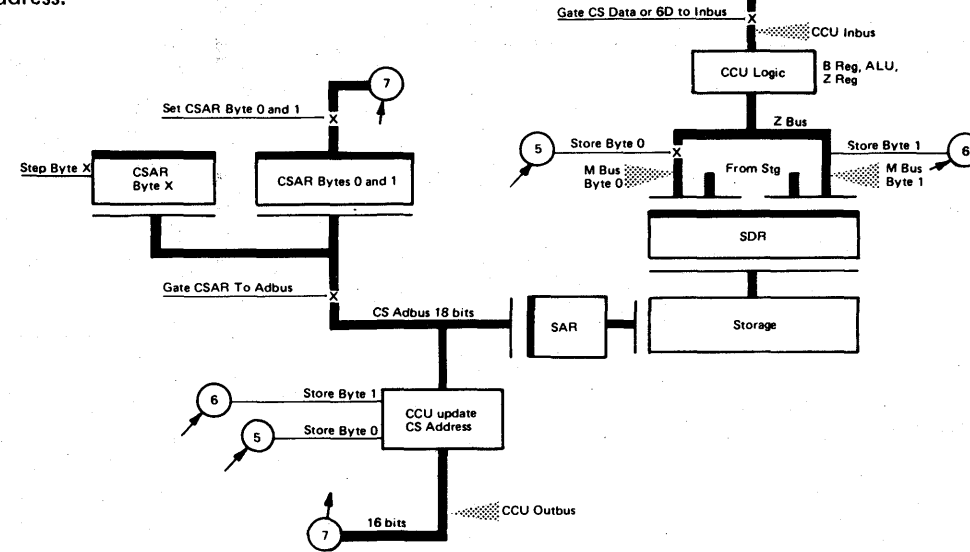
The cycle steal operation blocks the Service In signal from being sent to the channel interface until the cycle steal operation has been completed.



'In reg fetch' starts the EB clock that provides the timing pulses to load the data bytes from buffer 0 then buffer 1 into the In register.

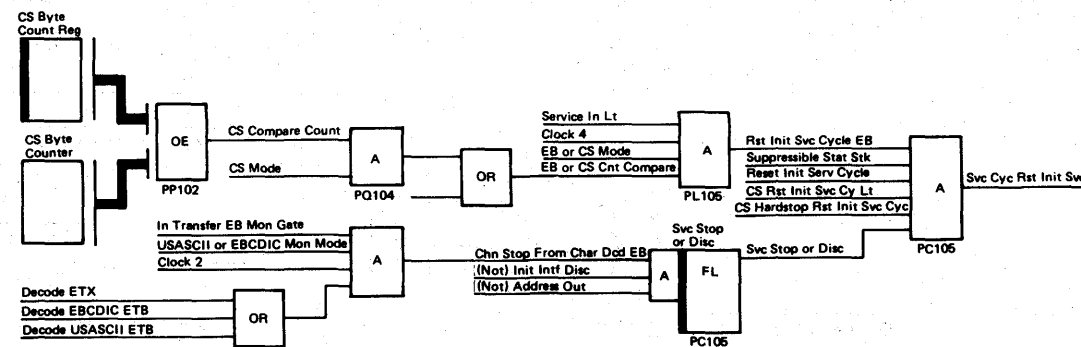


When the CCU takes a CS1 machine cycle, the CCU loads the SDR depending on which "store byte" lines are active then stores the SDR contents into the storage location addressed by the CSAR address.



The CCU updates the address and returns it to CSAR.

The service cycle operation resumes after the cycle steal operation is completed. This service-cycle cycle-steal routine keeps repeating (without any normal program interrupts) until (1) the CA4 detects an ETX or ETB character in the data transferred from the channel provided the CA4 is in ESC mode and the monitor control latches are set (see H-260), or (2) the CA4 has received the number of data bytes equal to the desired count in the 'CS byte count' register. Either condition resets the initiate service latch that stops the service cycle operation and requests a level 3 interrupt.



The type 4 channel adapter requests a level 1 interrupt whenever:

- A channel 'Bus-In' check occurs.

The channel adapter hardware detects bad parity in the data byte being sent across the channel to the CPU.

The control program should respond to the interrupt with an Input X'67' instruction to transfer the contents of the error condition register to the CCU. Bit 1.0 should be transferred if a channel 'Bus-In' check occurred.

- An in/out instruction accept check occurs.

An in/out instruction accept check (invalid I/O op) occurs if the control program executes an Input or Output X'60' through X'66' or X'6C' through X'6F' instruction while the CA is actively handling any data or status transfer sequence. When the control program responds to the level 1 interrupt with an Input X'67', bit 1.1 is transferred to the CCU.

- A 'CCU Outbus' check occurs.

When bad parity is detected on the 'CCU Outbus', the CA requests a level 1 interrupt. Bit 1.2 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.

- A local store check occurs.

Bad parity being gated from the local store registers causes a level 1 interrupt request. Bit 1.3 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.

- An EB local store check occurs.

Bad parity being gated from the EB local store during Input X'6C' or Input X'6D' sets the 'local store check' latch. The next Input X'6D' instruction causes a level 1 interrupt request. Bit 1.3 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.

- CS outbus check occurs.

When bad parity is detected on the 'CCU Outbus' during a cycle steal data transfer, the CA requests a level 1 interrupt. Bit 0.0 is returned to the CCU from the 'CS error register' when the control program executes an Input X'6E' instruction in response to the interrupt.

- CS inbus check occurs.

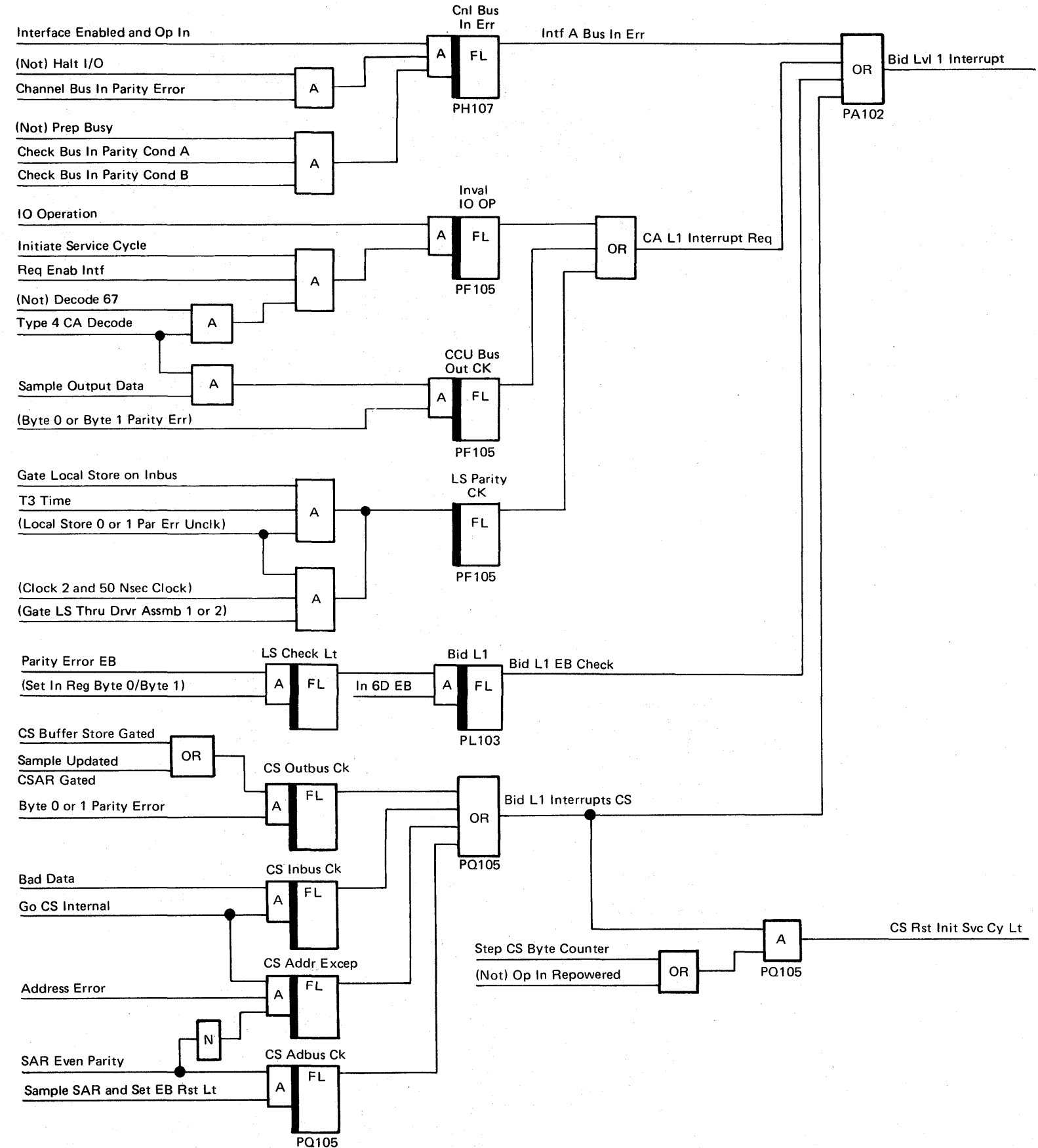
When the CCU raises 'bad data' to signal that the CCU has detected even parity on the 'CCU inbus' during a cycle-steal data transfer, the CA requests a level 1 interrupt. Bit 0.1 is returned to the CCU from the 'CS error register' when the control program executes an Input X'6E' instruction in response to the interrupt.

- CS address bus check occurs.

When the CCU raises 'SAR even parity' to signal that the CCU has detected incorrect parity (even) on the 'CS adbus' during a cycle-data transfer, the CA requests a level 1 interrupt. Bit 0.2 is returned to the CCU from the 'CS error register' when the control program executes an Input X'6E' instruction in response to the interrupt.

- CS address exception occurs.

When the CCU raises 'address error' without 'SAR even parity' to signal that the CCU has received an address from a type 4 CA that is beyond the storage capacity of the 3705 or that points to a protected area of storage, the CA requests a level 1 interrupt. Bit 0.3 is returned to the CCU from the 'CS error register' when the control program executes an Input X'6E' instruction in response to the interrupt.



INITIAL SELECTIVE RESET, INITIAL INTERFACE DISCONNECT AND SERVICE SELECTIVE RESET—SELECTOR CHANNEL CONTROLS

The 'gate 60 or reset' FL is to prevent losing a second interrupt while the CA4 is handling a previous interrupt.

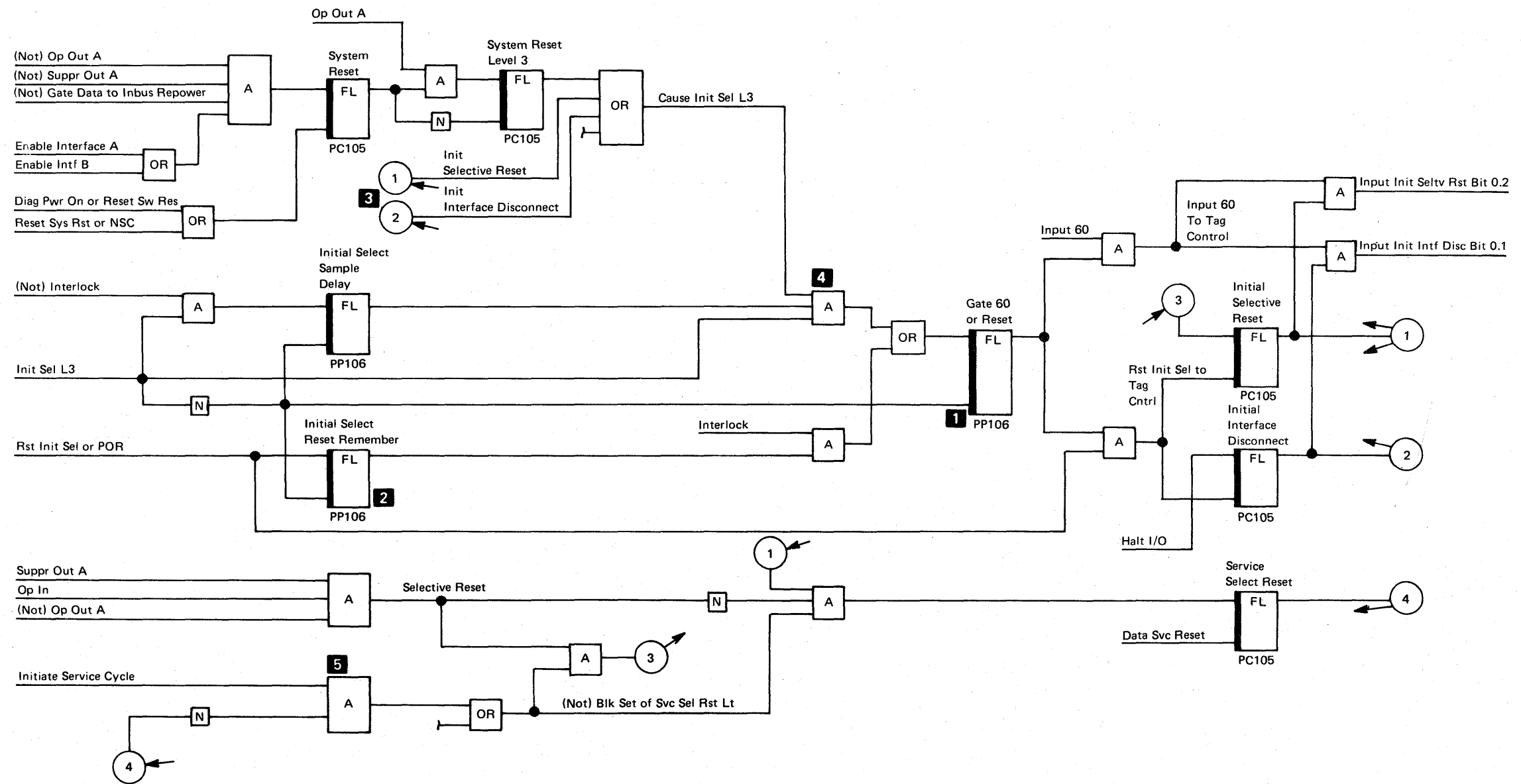
During a normal initial select L3 interrupt (not caused by selective reset or halt I/O), the 'gate 60 or reset' FL **1** is reset, which:

- Prevents either inputting or resetting the 'initial selective reset' FL or 'initial interface disconnect' FL.
- Prevents the 'service selective reset' FL from being set.

If selective reset or halt I/O occurs during a normal initial select L3 interrupt, their respective latch will be set and after the original initial select is reset **2**, the two latches can be inputted and/or reset.

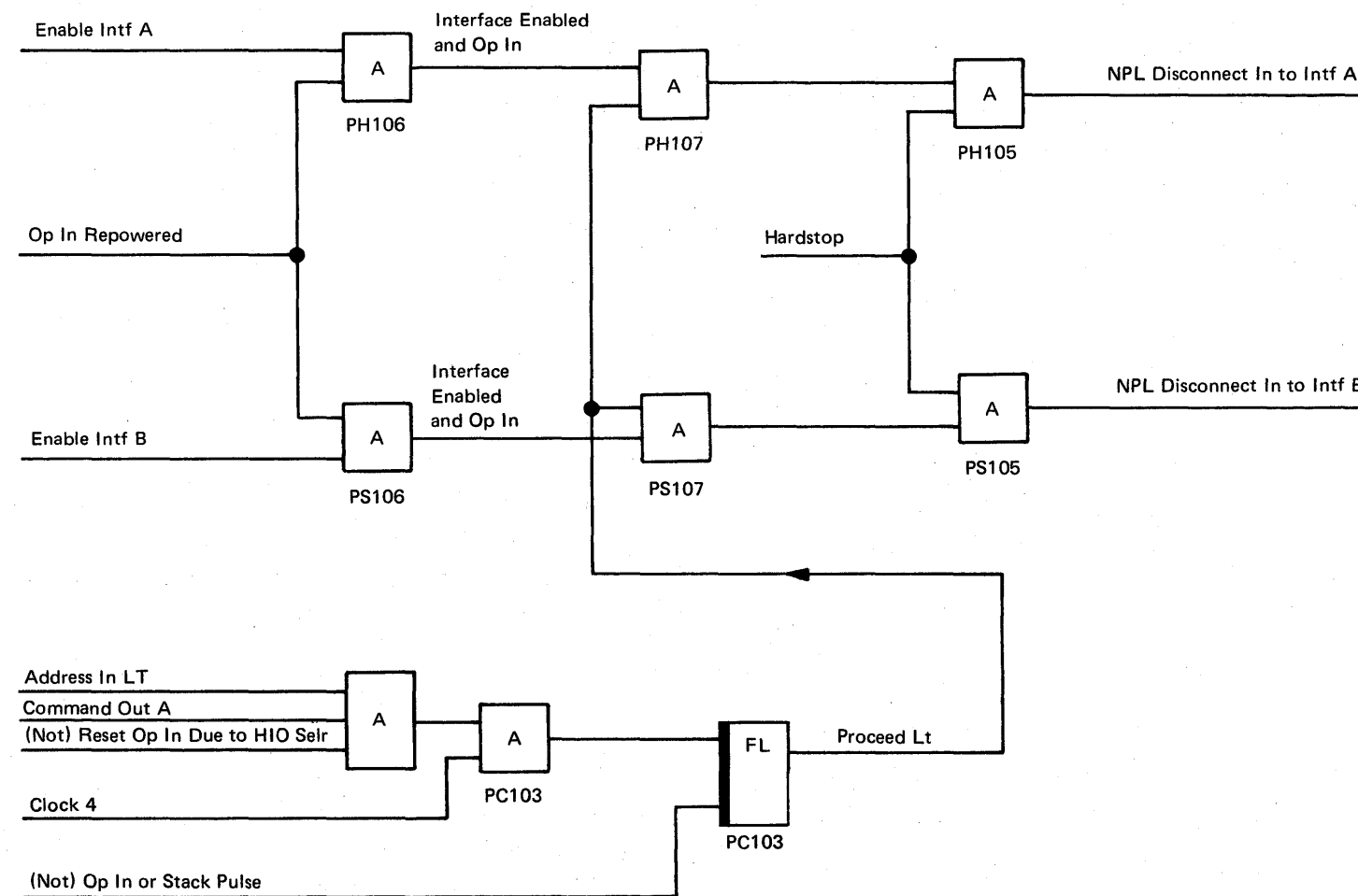
If the initial select L3 interrupt is caused by a selective reset or Halt I/O **3** (no initial select L3 interrupt was in progress), the two latches can be inputted or reset **4**.

The service selective reset can only be set when the CA4 is transferring data over the channel (initiate service cycle active) **5**.



DISCONNECT IN-SELECTOR CHANNEL

Disconnect In is gated to the channel interface (A or B) when a hardstop condition occurs and the CA4 is actively operating with the channel.



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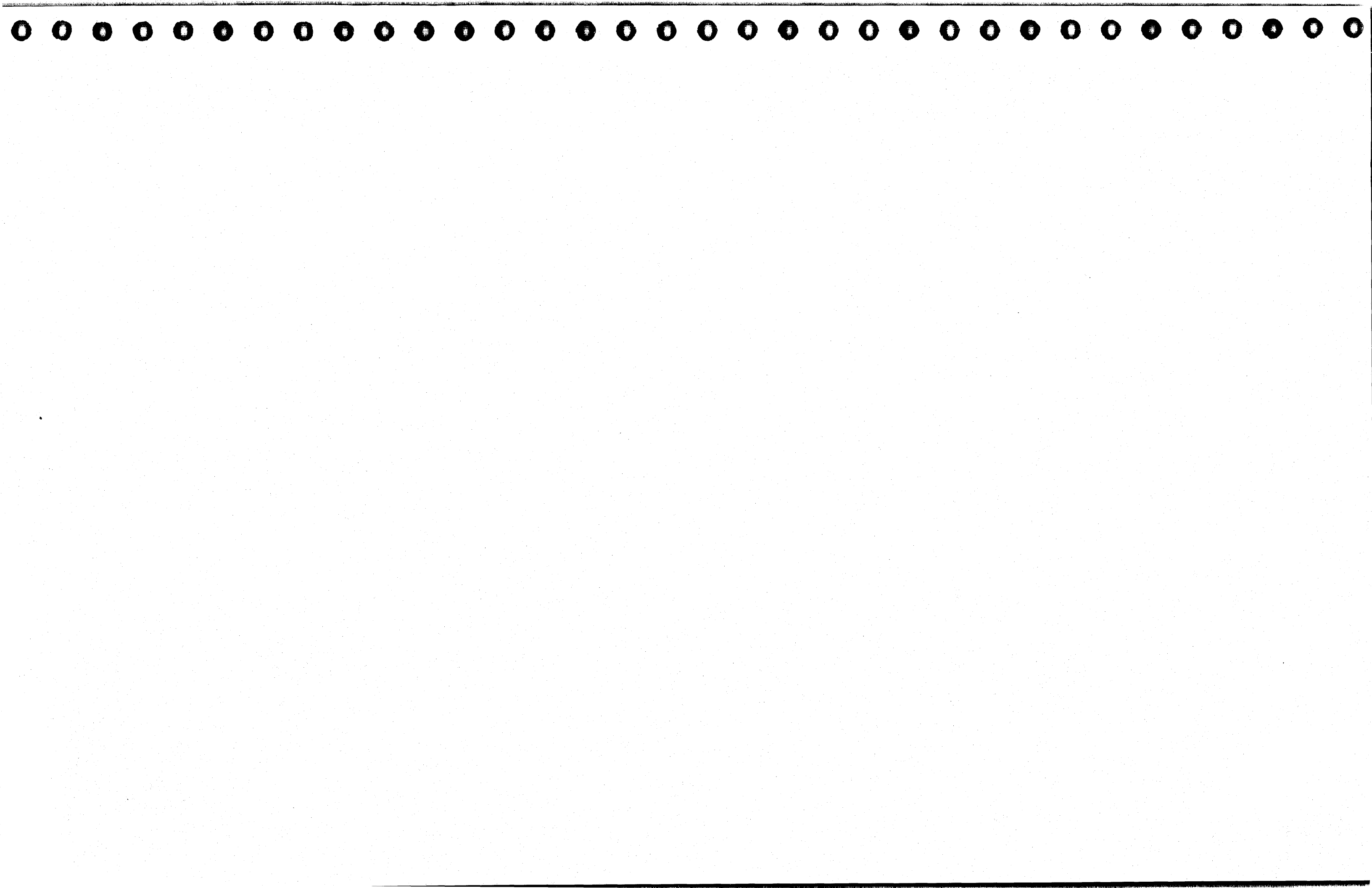
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3705 Communications Controller Theory-Maintenance

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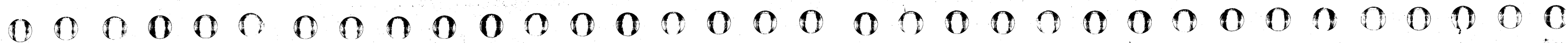
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front cover through iv	iii, iv	iii, iv
vii through x	vii, viii	vii, viii
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	C-010 through C-020	F-110 through F-130
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	C-231, C-235 (added)	F-340, F-341 (F-341 added)
	C-236, C-241 (C-236 added)	F-356 through F-395
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	C-246, C-248 (C-248 added)	x-1 through x-8
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	x-1 through x-8	

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Summary of Changes

This Technical Newsletter incorporates information on the IBM Type 3HS Communication Scanner and three new IBM line sets designed for use with the IBM 3705 Communications Controller. Information is provided on the type 1N line set which is available for attachment to a CCITT X.21 interface (nonswitched – World Trade only), and on type 1GA and 1TA line sets which are available for use with type 3HS scanner (at line speeds up to 230,400 bps).

Note: Please file this cover letter at the back of the manual to provide a record of the changes.





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(Volume I)
ix, x
7-200, 7-210
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(Volume II)
X-1 through X-8

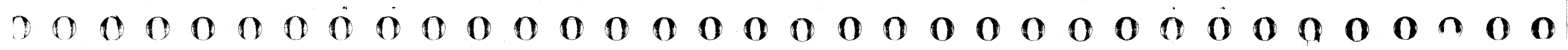
(Volume III)
vii, viii
D-000, D-010
D-140 through D-240
D-300 through D-370
D-371 through D-450 (removed)
D-500 through D-670 (added)
E-020 through E-021
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This Technical Newsletter incorporates information on the 3705-II Modified Power System.

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3705 Communications Controller Theory – Maintenance

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vii, viii	vii, viii	C-246, C-247A (added)
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A technical change to the text or to an illustration is indicated by a vertical line to the left of the change.

Summary of Changes

This Technical Newsletter incorporates information on the type 1R line set which is available for attachment to a CCITT X.21 interface (switched). Information on the consolidation of line set functions for line set 1D is also included.

Note: Please file this cover letter at the back of the manual to provide a record of the changes.

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