IBM

System/370 Model 145 Reference Summary

S229-2239-1

IBM Corporation, Field Support Documentation, Dept 927,
Rochester, Minnesota 55901

PREFACE

This publication is primarily intended for customer engineers servicing System/370 Model 145.

Second Edition (September 1972)
This is a major revision of, and makes S229-2239-0 obsolete.

Address any comments concerning the contents of this publication to: IBM, Field Support Documentation, Dept 927, Rochester, Minnesota 55901

CONTENTS

INDEX

BRANCH AND MODULE SWITCH WORD

Wordtype "0"

	C0								C1								C2								C3							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	Branch and Module Switch				Branch Hinh				Branch Source						Branch Source Dest		Module								Next Address				Branch Low			
									Word				Byte																			
0000	0	0	0	0	0				See LS/EXT Addr. Forms				0																0			
0001					1								1		S-B														1			
0010					S1								2		T-B														70			
0011					S0								3		L-B														NZ			
0100					S2																								S3			
0101					S4																								S5			
0110					S6																								S7			
0111					SH																								BL			
1000					B0																								B0			
1001					B1																								B1			
1010					B2																								B2			
1011					B3																								B3			
1100					B4																								B4			
1101					B5																								B5			
1110					B6																								B6			
1111					B7																								B7			

BRANCH WORD

Wordtype "1"

	C0								C1								C2								C3							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	Branch				Branch High				Branch Source *						K HI-LO			S/R	S/R Source		K				Next Address				Branch Low			
									Word				Byte																			
0000					0				See LS/EXT Addr. Forms				0		MS			OR	Branch source										0			
0001	0	0	0	1	1								1		L		DK	A-,	S										1			
0010					S1								2		H				P										Z0			
0011					S0								3		ST				GA										NZ			
0100					S2																								S3			
0101					S4																								S5			
0110					S6																								S7			
0111					SH																								BL			
1000					B0																								B0			
1001					B1																								B1			
1010					B2																								B2			
1011					B3																								B3			
1100					B4																								B4			
1101					B5																								B5			
1110					B6																								B6			
1111					B7																								B7			

Module

Notes: When K HI-LO=00, no set/reset occurs, and C2 is used as the module portion of the address, which is set into M2 (N2) Also, during module switching, T register bits 0 and 1 replace the two low-order bits (C3, B2-3) in setting M3(N3), B2-3

The branch source field can address the A local store on an external register. The branch-source byte is set into the A-reg

When DK (C2 bit 0=1) is on, the Diagnostic Key will be set if the OR function is designated, and reset if the A-function is designated

GA FUNCTION CHARTS

Set/Reset Controls for Selector Channels
(Set Retry Holdup Also)

h (K Field)	Set GAL GA, OR, K0h	Reset GAL GA, A-, K0h	Set GAH GA, OR, Kh0	Reset GAH GA, A-, Kh0
1	Set Poll Control (Soft)	Reset Poll Control	Set Channel 1	Channel Reset
2	Set Poll Control (Hdwr)	Reset Retry Holdup	Set Channel 2	Chain Reset
3	Set Command Retry		Set Channel 3	Machine Reset
4			Set Channel 4	
5	Set Count Ready	Start I/O Reset	Set Channel Loaded	Reset Channel Loaded
6	Set Protect Check	Set Control Check	Set CC	Diag Buffer Shift
7	Set Program Check	WLR Sample	Set PCI	Reset Interrupts
8	Set Interrupt Latch	Set DCC Mode	Diag Block Share Req	Reset DCC Mode and Diag Block Share Req
9	Set Select Out	Reset Sel Out and Primed	Set Diag Stat	Reset Diag Stat and Interrupt Latch
A	Set Sup Out	Reset Sup Out	*Set Channel Primed	Set Channel Tried
B	Bus-In to GR		*Set Data Out	
C	Set Op Out	Reset Op Out and Diag Set GR Full	*Set Command Out	Set Addr Out
D	Interface Control Check	Diag Serv Signal	*Set Service Out	Reset PCI
E	Set Diag Mode	Reset Diag Mode	*Set Halt I/O	Reset Halt I/O
F				

*Also Set Retry Holdup

h	Set GAL	Reset GAL	Set GAH	Reset GAH
K Field	GA, OR, K0h	GA, A-, K0h	GA, OR, Kh0	GA, A-, Kh0
1	Set Increment Length	Reset FCS	Set IFA Channel Gate	Reset Command
2	Set Prog Check	Reset PCI	Set Channel 2 Gate	Overrun
3	Set Prot Check	Reset Trap Req	Set Channel 3 Gate	Machine Reset
4	Set Channel Control Check	Reset CCW0 and		Reset Orientation
5	Set Allow Restart	WLR	Set Write Clock Gate	Latch
		Reset Lo Prior Req		
6		Chain End Reset	Set CS,CR,In Latches	Reset Count Ready,
7	Set Contingent Con	Reset Contingent	Set CS,CR,Out Latches	In,Out
8	Set Allow IDA	Con	Set MS,CR,In Latches	Set Halt I/O
9	Set Channel Busy	Reset Channel Busy	Set MS,CR,Out Latches	CE End Op SS
A	Set Interrupt Latch	Reset Interrupt Latch	Set Control Pulse	Diag Index
				Diag Raw Data Pulse
B	Set CUB	Reset CUB	Diag Read Data	Set Diag Read Gate
C	Set DCC	Reset DCC	Diag Clock Gap Sense	Bit Ring Advance
D	Set Low Prior Req	Rst H/L Comp,CC Er	Diag Data Gap Sense	Set Diag Mode Latch
E	Set IFA Inhibit Traps	Rst IFA Inh Traps	Set Data Field Latch	Reset Diag Mode
F				Latch

GA FUNCTION CHARTS

HH	Set GA Straight GA or KHH	Reset GA Straight
11	Set Diag Block Share Cycle - All Channels	Not Used
22	Reset Diag Block Share Cycle Latch - All Channels Reset Blk MPX UCW Latch	Not Used
33	Diag Check Reset All Channels	Not Used
44	Set Diagnostic Function Latch and Diag Reset Exp L/S	Not Used
66	Reset UCW Scan Latch All Channels Allow Trap Latch Set/Reset	Not Used
88	Set UCW Scan Latch All Channels Block Trap Latch Set/Reset	
FF	Reset Diagnostic Function Latch	Not Used

BRANCH AND LINK OR RETURN WORD

Wordtype "2"

	C0			C1				C2	C3		
	0 1 2 3	4	5 6 7	0 1 2 3 4 5 6 7				0 1 2 3 4 5 6 7	0 1 2 3	4	5 6 7
	Branch and Link or Return	Link Rtn	Branch High	Link Address: LS or EXT	Y	X	Space	K/Module	Next Address		Branch Low
0000		Link	0	LS				Bal – C3 Bit 4 controls this field- IFP, K is inserted into the PRegister- IFMS, this field provides a module address	Bal	P	0
0001		Rtn	1	EXT						MS	1
0010	0010		S1					Return – This K field provides a reset for the HRegister, A Bit of C2=1 causes the corresponding bit of H to be reset	Return	-	Z0
0011			S0							Use NA	10
0100			S2								S3
0101			S4								S5
0110			S6								S7
0111											11
1000											
1001											
1010											
1011											
1100											
1101											
1110											
1111											

WORD MOVE WORD VERSION "0"

Wordtype "3"

	C0								C1								C2				C3							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
	Word Move				Version	Branch High			LS or EXT	Destination Y			X			Spare	Source *				Mask				Next Address				Stop	Branch Low			
0000					0	0			LS								See LS/EXT Address Forms													0			
0001						1			EXT																					1			
0010						S1																								Z0			
0011	0	0	1	1		S0																											
0100						S2																								S3			
0101						S4																								S5			
0110						S6																								S7			
0111																																	
1000																																	
1001																																	
1010																																	
1011																																	
1100																																	
1101																																	
1110																																	
1111																																	

VERSION "0"

Note: * The source cannot specify an external register. SPTL, however, can be specified by C2, 80-3

WORD MOVE WORD VERSION "1"

Wordtype "3"

	C0								C1								C2								C3							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	Word Move				Version	Branch High			LS or EXT	Source Y			Source X			Source Spare	Destination				Mask				Next Address					Branch Low		
0000						0																								0		
0001					1	1			LS EXT								See LS/EXT Address Forms												Stop	1		
0010						S1																								Z0		
0011	0	0	1	1		S0																										
0100						S2																								S3		
0101						S4																								S5		
0110						S6																								S7		
0111																																
1000																																
1001																																
1010																																
1011																																
1100																																
1101																																
1110																																
1111																																

VERSION "1"

STORAGE WORD, NON K-ADDRESSABLE

Wordtype "4" to "7"

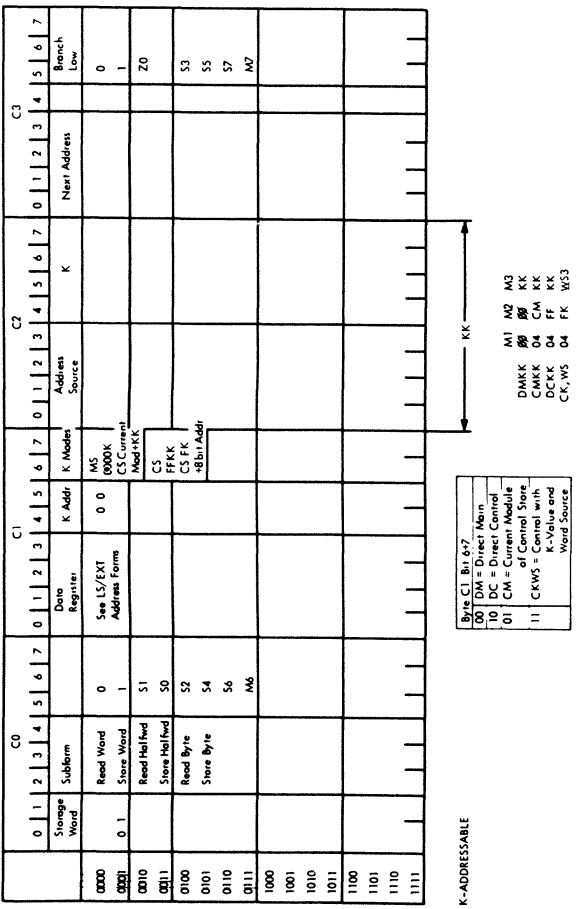
	C0			C1			C2			C3		
	0 1	2 3 4	5 6 7	0 1 2 3	4 5	6 7	0 1 2 3	4 5	6 7	0 1 2 3	4	5 6 7
	Storage Word	Subform	Branch High	Data Register	K or Inc/Dec	Stat Set	Address Source	Modes	Special Stat Set	Next Address		Branch Low
0000		Read Word	0	See LS/EXT	K-Addr	—	See LS/EXT	CS 16 Bit Addr			—	0
0001	0 1	Store Word	1	Address Forms	No Addr Update	S,2	Address Forms	MS	TA		Dec Cnt	1
0010		Read Halfwd	S1		+	S45			TB			Z0
0011		Store Halfwd	S0		-	Z6		CPU Pro	Feat, LS			SDC (0) /VAL
0100		Read Byte	S2									S3
0101		Store Byte	S4						TH	Alternate for store, the above are used with Read.		S5
0110			S6						Upd Only			S7
0111			M6						Feat, LS			M7
1000												
1001												
1010												
1011			Subform for special stat Set=Feature local store									
1100		Read Key										
1101		Store Key										
1110												
1111												

NON K-ADDRESSABLE

Note:
1. S45S and Z6 stat sets are on the low byte of the count while S2 is on both bytes. (S2 is set/reset in this case).
2. The address and the count must be in even-odd LS words when Dec count is specified.
3. M6 and M7 refer to bits 6 and 7 of the low order byte of the data address after updating.
4. Stat sets of TA, TB, or TH causes T0,1,2,3, to be reset.
5. The update constant is implied as follows:
   For word operations - 4
   For Halfword operations - 2
   For byte operations - 1
   If TH is specified, then the number of bits in T0-T3 specify the constant. If the cycle is a selector share, then the constant comes from the selector flags regardless of special stat set field.
6. A zero is forced for branch low when SDC is specified.
7. The S or P register cannot be the destination of an updated storage address.
8. CPU Protect normally active.
   NOP Suppresses CPU Protect.

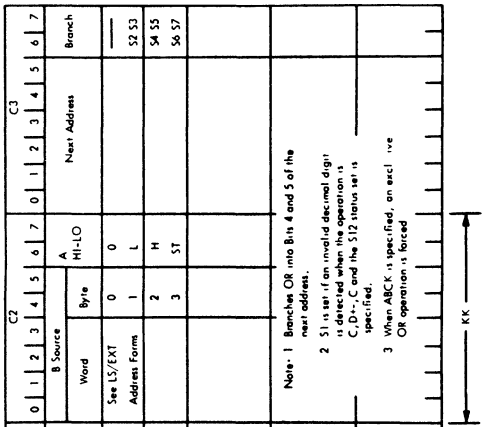
STORAGE WORD, K-ADDRESSABLE

Wordtype "4" to "7"



ARITHMETIC WORD 10 BYTE VERSION

Wordtype "8" to "B"



ARITHMETIC WORD, FULLWORD VERSION

Wordtype "8" to "B"

	C0				C1				C2				C3	
	0 1	2 3	4 5 6 7		0 1 2 3 4 5	6 7	0 1 2 3 4 5	6 7						
	Arith OP Form	Form	Operation		A Source	Stat Set	B Source		Shift		Next Address	Branch		
					Word	A Input			Word	B Input				
0000		A=A/K	$C^{S0=0}_{S0=1}$ +0		See LS/EXT	0	—		See LS/EXT	4	No Shift			—
0001		Z=A/B	C -1		Address Forms	16	S1,2		Address Forms	8	(R4,0)			S2 S3
0010	1 0	A=A/B	C + - C			24	I24			12	(R4,S0)			S4 S5
0011		B=A/B				32	Z24			32	(R4,TH)			S6 S7
0100														
0101														
0110														
0111														
1000														
1001														
1010														
1011														
1100														
1101														
1110														
1111														

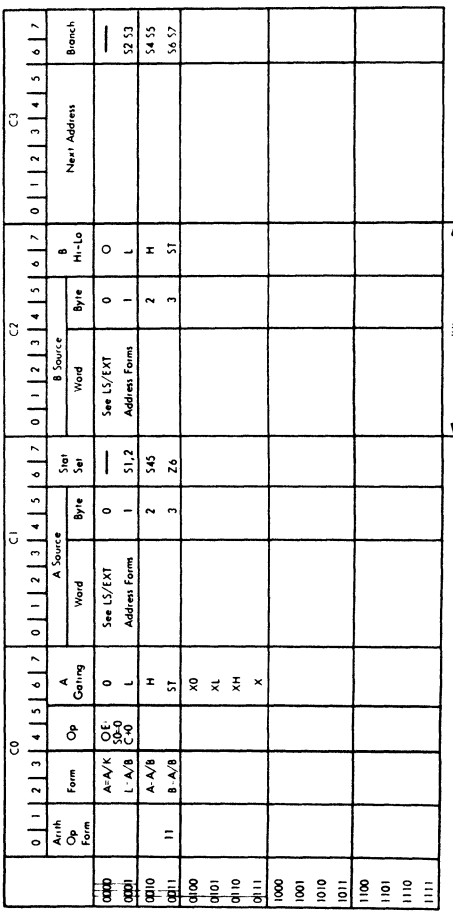
Notes:
1. When the stat set Z24 is specified S2 and S3 are set on the 24 bit result and only 24 bits are stored
2. When doing a right shift, the automatic set/reset of S0 is disabled.
3. I24 specified 24 bits add with no status sets, S0 or S3 are not set/reset regardless of the specified operation when I24 is the status set
4. The S or P register is not allowed as the destination of a full word arithmetic operation.

KK

FULLWORD VERSION

SYMBOL	OPERATION
,A,	AND
,OR,	OR
,OE,	EXCLUSIVE OR
+	TRUE ADD
-	COMPLEMENT ADD
,D + -,	DECIMAL ADD
+ -	BINARY ADD
,A-,	COMPLEMENT AND

Wordtype "C" to "F"



ARITHMETIC WORD, 10/11 INDIRECT BYTE VERSION

Wordtype "B" to "F"

	C0			C1			C2			C3	
	0 1 2 3 4 5 6 7			0 1 2 3 4 5 6 7			0 1 2 3 4 5 6 7			0 1 2 3 4 5 6 7	
	Arith Op Form	Form	Operation or Op/AXHL	A Source		Stat Set	B Source		A/B HI-LO	Next Address	Branch
				Word	A0A1		Word	B0B1			
0000		A=A/K		See LS/EXT	No Action		See LS 'EXT	No Act.	O		
0001		Z=A/B		Address Forms	No Action	S1 2	Address Forms	No Act.	L		S2 S3
0010	1 0	A=A/B			+ TA	S45	Bits 6 and 7 of the T Reg Specify the Byte Address	+ TB	H		S4 S5
0011	or 1 1	B=A/B	,OE,		- TA	Z6		- TB	ST		S6 S7
0100			+ 0	Bits 4 and 5 of the T Reg Specify the Byte Address							
0101			+ 1								
0110			$C^{S0=0}$ + 0								
0111			,A,								
1000			,OR,								
1001			C + - C								
1010			C,D +-,C								
1011			ABCK								
1100		Z=A/K	- 0								
1101			- 1								
1110			$C^{S0=1}$ - 1								
1111			,A,								

10, 11 INDIRECT BYTE VERSION

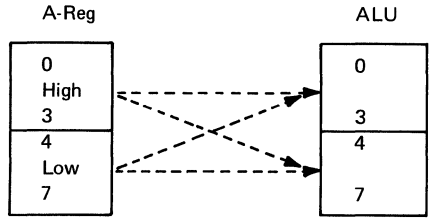
BRANCH SYMBOLS

0	Insert 0
1	Insert 1
B0–B7	Insert value of specified bit
BH	Insert 1 if branch source bits 0–3 ≠ 0
BL	Insert 1 if branch source bits 4–7 ≠ 0
I0	Force return I-cycles
I1	Force return I-cycles if no interrupt
M6	Insert M6 value after address update
M7	Insert M7 value after address update
NZ	Insert 1 if branch source bits 0–7 ≠ 0
S0–S7	Insert value of specified S-register bit
Z0	Insert 1 if S4 and S5 = 1
TH	Special – M3 bits 2 and 3 replaced by T-register bits 0 and 1, then module switch
AB	If TA or TB is decrementing, branch when 00. If TA or TB is incrementing, branch when 11

STAT SET SYMBOLS

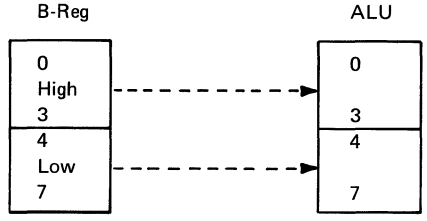
S2	Storage word – S2 set to 1 if count ≠ 0, otherwise S2 set to 0
S12	S1 – binary byte OPS: S1 set to 1 if carry out of bit 1 of result. Binary fullword OPS: S1 set to 1 if carry out of byte 0, bit 1. Decimal ops: S1 set to 1 if an invalid decimal digit detected. S2 – Set to 1 if result ≠ 0
S45	Arith ops: S4 = 1 if bits 0–3 of Z-bus = 0 S5 = 1 if bits 4–7 of Z-bus = 0 Storage word ops: Same except test made on low byte of count field after update
Z6	Same as S45 stat set except S4 depends on bits 0–5
Z24	Arith fullword OPS: If the low 24 bits of result ≠ 0, S2 set to 1, otherwise S2 unchanged. S3 set to 1 if carry out of bit 0, byte 1. Only low 24 bits of result gated to destination
I24	Arith ops: Inhibits set of any S-reg bits. Only low 24 bits of result gated to destination. In shift operations, the high four bits of result set to 0 regardless of shift type

ALU ENTRY GATING



A-Entry Gating

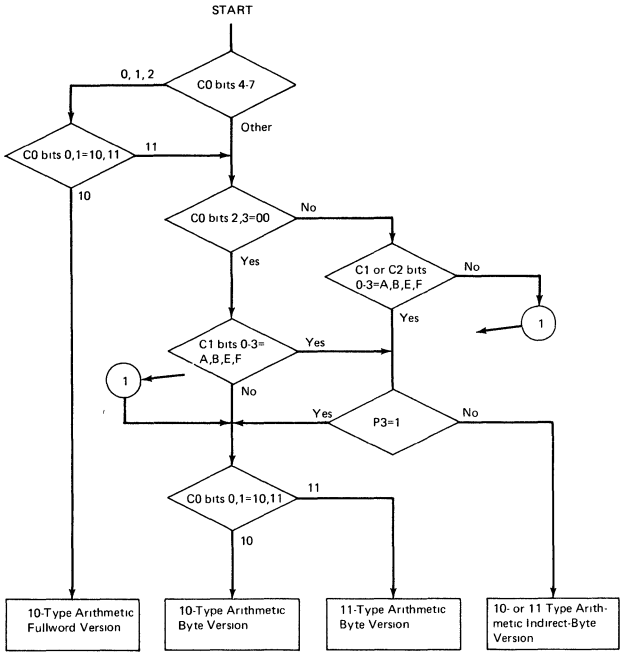
BS	Straight
BS0	Block High and Low
BSH	Gate High; Block Low
BSL	Gate Low; Block High
BSX	Cross High and Low
BSXH	Cross; Gate High; Block Low
BSXL	Cross; Gate Low; Block High



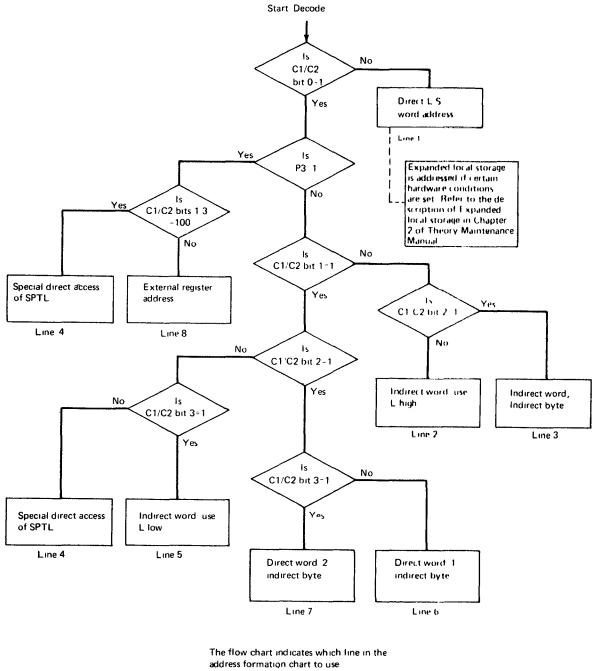
B- Entry Gating

BS	Straight
BSO	Block High and Low
BSH	Gate High; Block Low
BSL	Gate Low; Block High

ARITHMETIC WORD CHART SELECTION



CONTROL WORD CHART SELECTION



The flow chart indicates which line in the address formation chart to use

ADDRESS FORMATION CHART

Line No	Byte C1 or C2 0	1	2	3	P3	Defines	Local Storage or External Word * Address Decode 0	1	2	3	4	5	6	7	Byte* 0	1
1	0	X	X	X	X	Direct Local Storage Word Address	0	Note 1	P5	P6	P7	C1 or C2 1	2	3	C1 or C2 4	5
2	1	0	0	X	0	Indirect Local Storage Word Address	0	0	P1	P2	L0	L1	L2	Note 2	C1 or C2 4	5
3	1	0	1	X	0	Indirect Word – Indirect Byte	0	0	P1	P2	L0	L1	L2	Note 2	T4 or T5 T6	T7
4	1	1	0	0	X	Special External Register Set S P T L									C1 or C2 4	5
5	1	1	0	1	0	Indirect Local Storage Word Address	0	0	P1	P2	L4	L5	L6	L7	C1 or C2 4	5
6	1	1	1	0	0	Direct Word 1 – Indirect Byte	0	0	P5	P6	P7	C1 or C2 1	2	3	T4 or T5 T6	T7
7	1	1	1	1	0	Direct Word 2 – Indirect Byte	0	0	P5	P6	P7	C1 or C2 1	2	3	T4 or T5 T6	T7
8	1	X	X	X	1	External Registers 8 groups of seven words	0	0	P0	P1	P2	C1 or C2 1	2	3	C1 4	5
									X-Line			Y Line				

Note 1 **Refer to the Expanded local-storage description in Chapter 2 of Theory-Maintenance Manual**

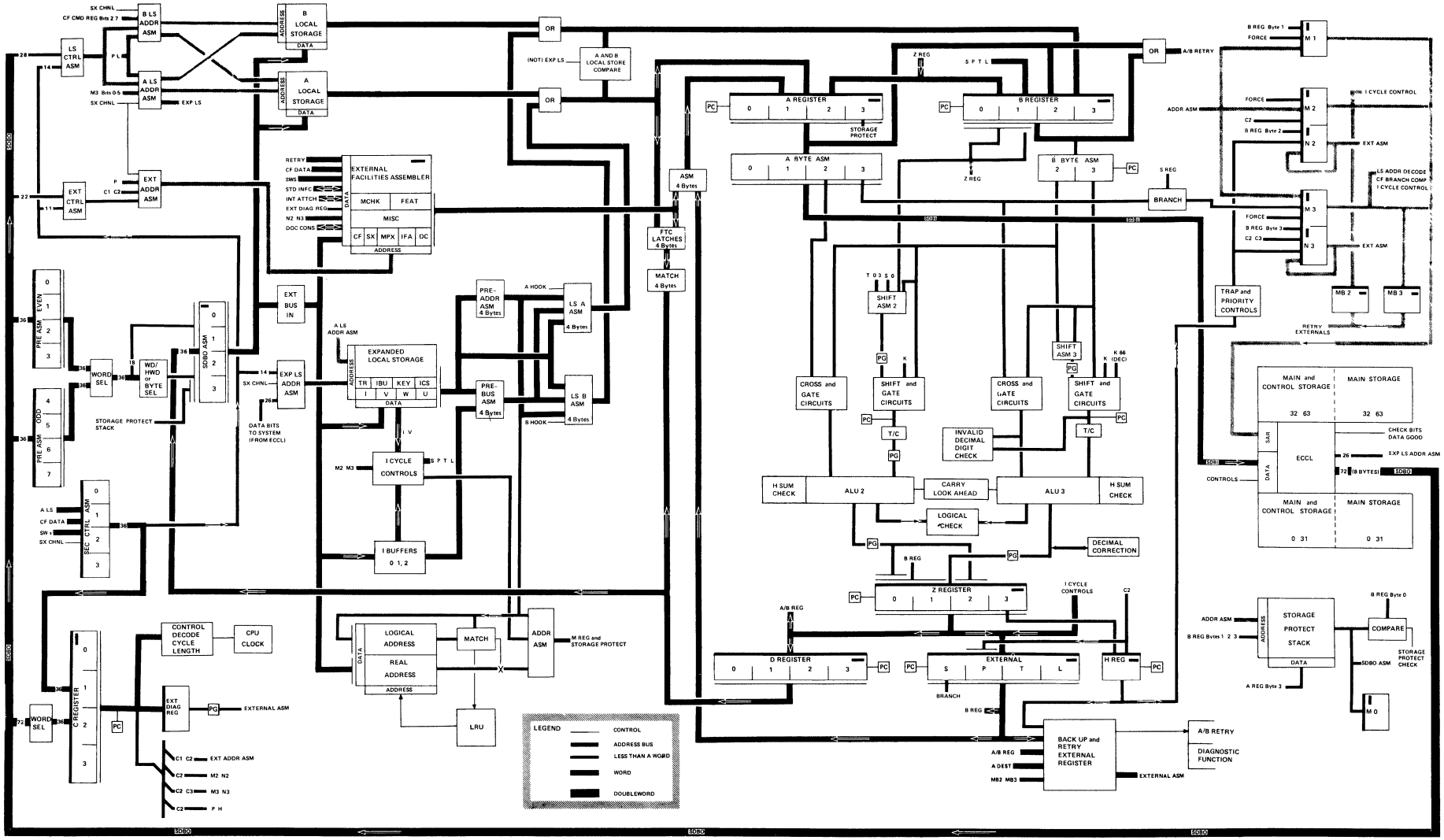
Note 2 C1 or C2 bit 3 is ORed with bit 3 of the L-register

For source addressing, C1 bits apply to A local storage, Expanded local storage, or External registers

For source addressing, C2 bits apply to B local storage, or Expanded local storage

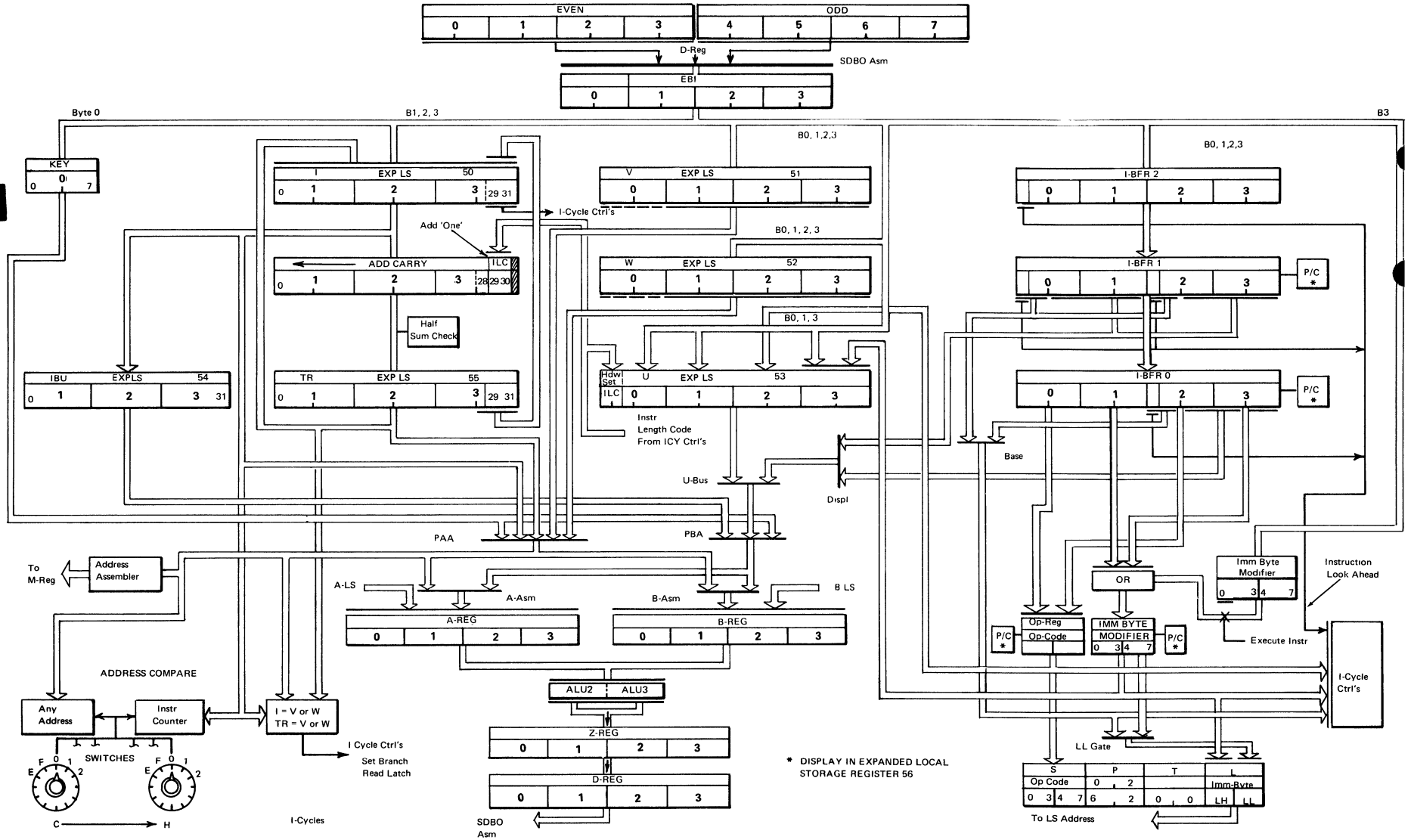
For destination addressing, C1 and C2 bits apply to A and B local storage, Expanded local storage, or External registers

3145 CPU DATA FLOW



2

I-CYCLES DATA FLOW



EXPANDED LOCAL STORAGE

I-CYCLE STATUS REGISTER

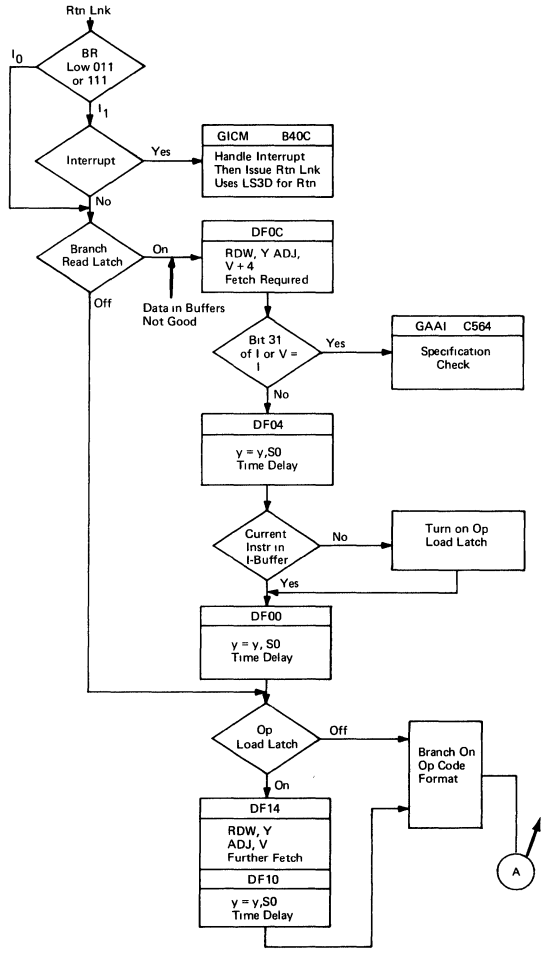
Definition of Exp LS 56	
ICS Byte 2	
0	BR Read Latch
1	Op Load Latch
2	Op L2
3	Op L1
4	Prefetch Required
5	Prefetch Inhibit
6	FLP Long
7	Op Br to DF
ICS Byte 3	
0	I Buffer 0 Parity Check Latch
1	I Buffer 1 Parity Check Latch
2	Half Adder Check Latch
3	IMM Byte Modifier Parity Check
4	X = 0
5	B = 0
6	Set Control Address
7	Low Bit

EXP LS 56 (ICS) is intended for use only as a manual display and can't be accessed via microcode.

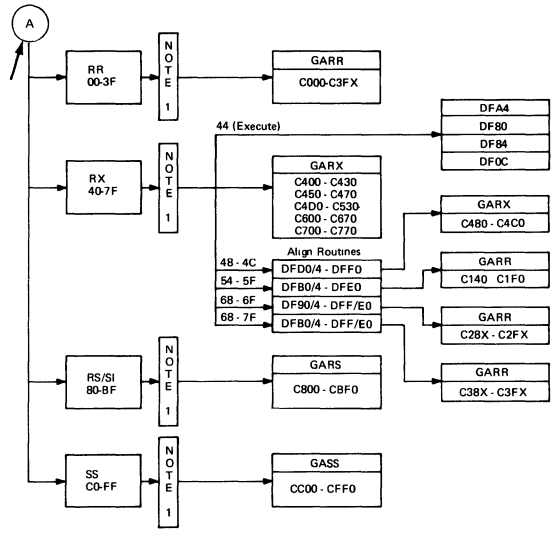
When in I-cycles (DF Module) the line generate address is functionally overridden during addresses DF00 and DF10.

If both index and base indicators are off, double indexing will take place.

I-CYCLES



I-CYCLES



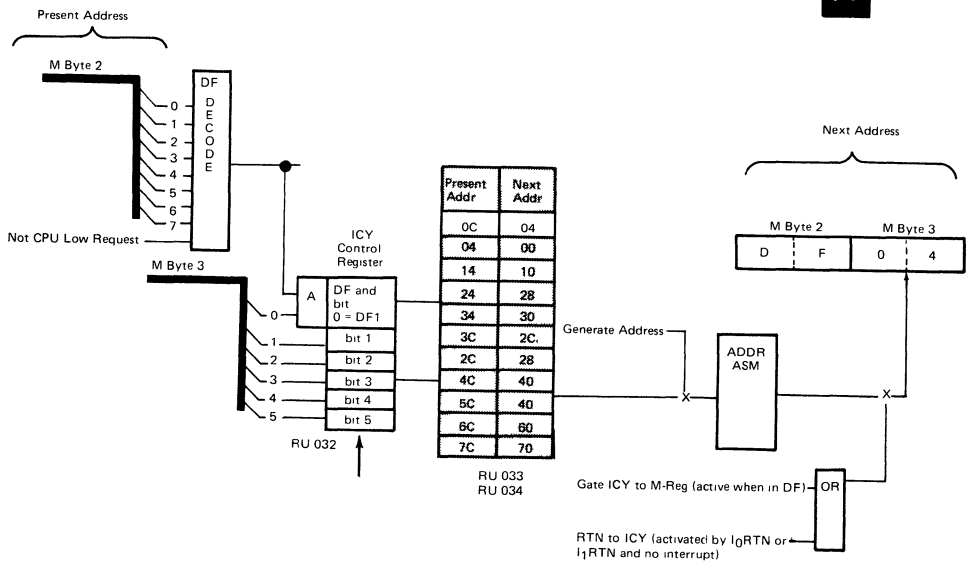
Instruction	Without Prefetch	With Prefetch
RR (Not FP Long)	DF20	DF34 - DF30
RR (FP Long)	DF24 - DF28	DF3C - DF2C - DF28
RX (Double Index)	DF4C - DF40	DF58 - DF40
RS,SI,RX (Not Double Index)	DF48	DF58
SS	DF6C - DF60	DF7C - DF70

PSW LOCATIONS

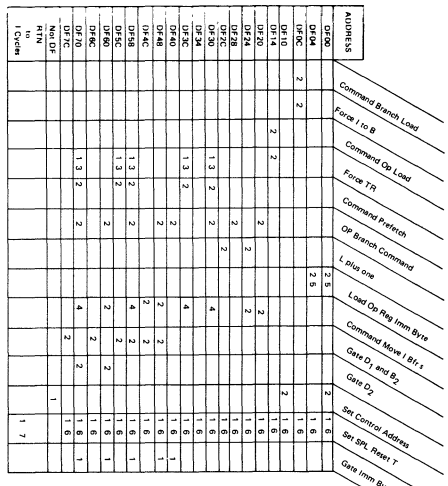
3145 Models

System Mask		Key		OWMP		Interrupt Code	
0	7	8	11	12	15	16	31
External 10		EXP LS 50 Byte 0		EXP LS 53 Byte 1			

ILC		CC		Program Mask			Instruction Address	
32	33	34	35	36	37 38	39	40	63
EXP LS 53		EXP LS 53		EXP LS 53			EXP LS 50	
Byte 0 Bit 0, 1		Byte 0 Bit 2, 3		Byte 0 Bits 4-7			Bytes 1, 2, 3	



ICY CTRL REG BITS					CONTROL LINE	FUNCTION
1	2	3	4	5		
0	0	–	1	–	Command Branch Load	Load I-bfr 0 (I-Bfr 1 in next cycle)
0	0	–	1	–	Force I	Gate I-Reg to B (and Address Adjust)
0	0	1	0	1	Command OP Load	Load I-Bfr 1 (I-Bfr 2 in the next cycle)
0	0	1	0	1	Force TR	Gate TR-Reg to B (and Address Adjust)
–	1	1	–	0	Command Prefetch	Activate prefetch
1	0	1	1	–		Force TR to ADR ADJ Asm
0	1	1	1	–		(and B if DF 30 or DF 3C)
–	1	–	–	0	OP Branch Command	Use Op-Reg to define the next Cxxx address; or go
1	–	–	–	0		to the Align Routine
0	1	0	–	1	L plus one	Force bits 7 and P of data being gated to L-Reg to be inverted for FLP long
0	0	0	–	–	Load OP, IMM Byte	Initial load of Op and IMM Byte
–	1	0	0	–	Command Move I-Bfr	Used with I-Reg to activate the set
1	0	0	1	–		or reset of the I–Bfr's
1	–	–	1	–	Gate D_1 and B_2	Used to gate the correct base or displacement
1	1	–	0	–	Gate D_2	field from the I-Bfr's 0 and 1 to L - low or B-Reg
0	0	–	–	0	Set Control Address	Set next address for ICY sequence



1. These controls are not the result of the Control Register decode
2. The Control line is activated by the corresponding address.
3. This line is activated by Command prefetch.
4. The set/reset of the I-Bfrs is also controlled by Command Prefetch.
5. This control line is activated, but not used.
6. From DF00 Through DF7C SPTL is controlled by I-Cycles. DFE0 or DFF0 will activate this control line again to restore SPTL after an align.
7. Set P, set LL.

ECCL BOARD LAYOUT

ECCL Board Layout

V	U	T	S	R	Q	P	N	M	L	K	J	H	G	F	E	D	C	B	A
DCPL	Basic System Card	1862 SQ232	1862 SQ226	1862 SQ244	1862 SQ238	6031 SQ261 SQ262	1860 SQ301 SQ273	1863 SQ271 SQ273	1861 SQ290 SQ292	1859 SQ280 SQ287	6031 SQ251 SQ257	1862 SQ208	1862 SQ202	1862 SQ220	1862 SQ214	1865 SQ312	1864 SQ401 SQ404	1866 SQ407 SQ410	DCPL
		SDR Bits	SDR Bits	SDR Bits	SDR Bits	Read Check Bit Gen	Parity Out Gen	Synd Gen # 1	Error Type Decoder	Syndrome Decoder	Write Check Bit Gen	SDR Bits	SDR Bits	SDR Bits	SDR Bits	Delay Line # 1	Storage Address Reg	BSM Clock	
		0 1 32 33	8 9 40 41	16 17 48 49	24 25 56 57							4 5 36 37	12 13 44 45	20 21 52 53	28 29 60 61				
		1862 SQ235	1862 SQ229	1862 SQ247	1862 SQ241			1863 SQ275 SQ277				1862 SQ211	1862 SQ205	1862 SQ223	1862 SQ217	1865 SQ315			
DCPL		SDR Bits	SDR Bits	SDR Bits	SDR Bits			Synd Gen #2				SDR Bits	SDR Bits	SDR Bits	SDR Bits	Delay Line #2			DCPL
		2 3 34 35	10 11 42 43	18 19 50 51	26 27 58 59							6 7 38 39	14 15 46 47	22 23 54 55	30 31 62 63				

- Storage size The main storage capacity within the CPU frame may be any of the following

CPU Model	Program Storage	Control Storage
3145FED	114,688 Bytes (112K)	32K (See Note)
3145GE	163,840 Bytes (160K)	32K
3145GFD	212,992 Bytes (208K)	32K
3145 H	262,114 Bytes (256K)	32K
3145HG	393,216 Bytes (384K)*	32K
3145 I	524,288 Bytes (512K)*	32K

* Main storage capacity above 256K bytes is contained in a 3345 main storage frame When a main storage frame is attached, it contains the low-order storage addresses

NOTE The 3145 has movable control storage boundary that allows up to 64K (65,536) bytes of control storage, depending on the feature installed The additional control storage capacity above 32K is at the expense of main storage The storage boundary is determined at the time that the microprogram is compiled

Voltage Locations On Phase 2 I STG Array Boards

Voltages are applied to EACH card. Each card occupies two connector positions

+7V	B09	-3	B06
+2V	B04	GND	D08/B13
+1.25V	D03		

DATA BIT LOCATION CHART

Upper Board

V	U	T	S	R	Q	P	N	M	L	K	J	H	G	F	E	D	C	B	A
	34	32	42	40	50	48	58	56	C1	C8	38	36	46	44	54	52	62	60	Addr Buffer Card
Term Card	35 (34)	33 (32)	43 (42)	41 (40)	51 (50)	49 (48)	59 (58)	57 (56)	C2 (C1)	C0 (C8)	39 (38)	37 (36)	47 (46)	45 (44)	55 (54)	53 (52)	63 (62)	61 (60)	

Wiring Side

Lower Board

V	U	T	S	R	Q	P	N	M	L	K	J	H	G	F	E	D	C	B	A
	2	0	10	8	18	16	26	24	C16	C32	6	4	14	12	22	20	30	28	Addr Buffer Card
Term Card	3 (2)	1 (0)	11 (10)	9 (8)	19 (18)	17 (16)	27 (26)	25 (24)	C4 (C16)	CT (C32)	7 (6)	5 (4)	15 (14)	13 (12)	23 (22)	21 (20)	31 (30)	29 (28)	

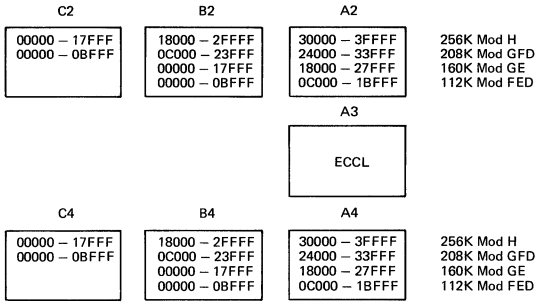
Wiring Side

NOTES

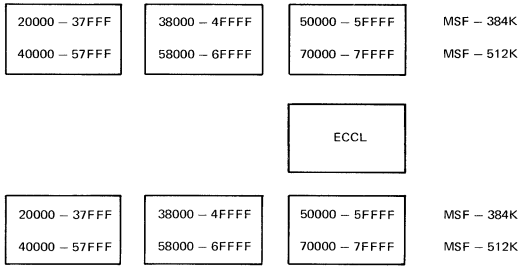
1. The 24K BSM has two bits per card for 18 cards in lower rows
2. The 48K BSM has one bit per card for 36 cards
3. 24K BSM jumper P/N 2637601 (red)
4. 48K BSM jumper P/N 2637602 (yellow)

3145 CPU BSM ADDRESSING

(Without 3345 Attached)

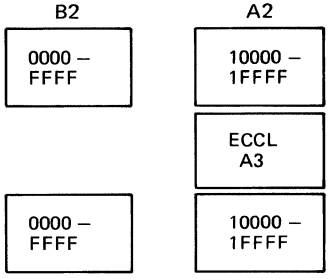


(With 3345 Attached)



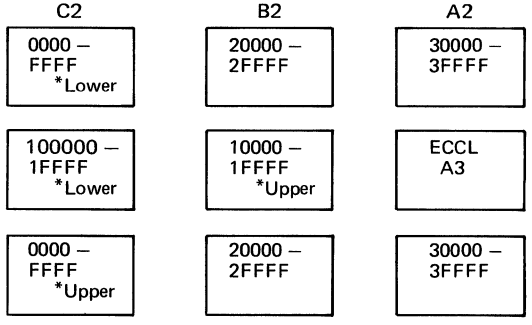
MAIN STORAGE FRAME - 128K

(384K Total Storage)



3345 MAIN STORAGE FRAME 256K

(512K Total Storage)



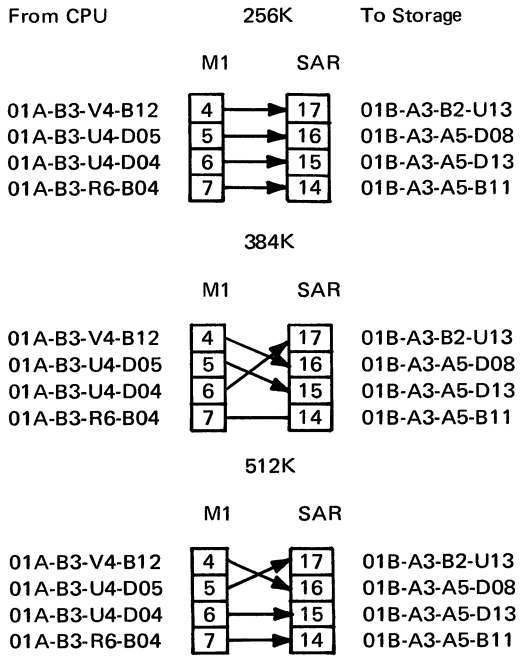
COMMON TEST POINTS

ALL ARRAY CARDS

Data Out	B05
Data Out	B03 (If 2 Bit Card)
Data In	D11
Data In	J02 (If 2 Bit Card)
Set Pulse	D04
Reset Pulse	D05
Select at Array Board	A5 B05

CPU

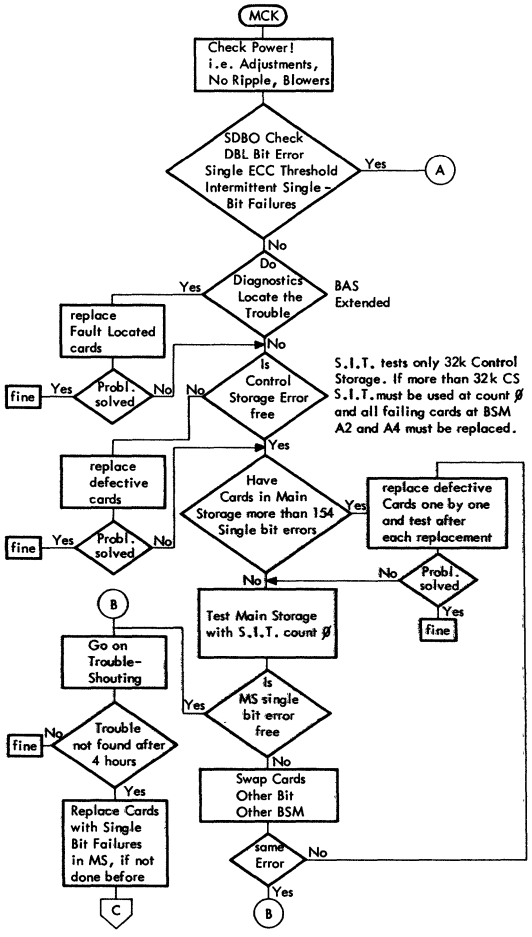
SAR Bits 15, 16, and 17



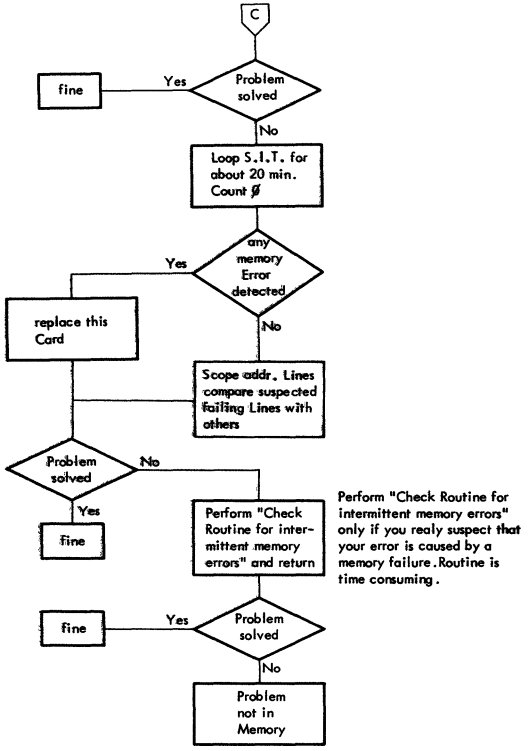
NOTE: SAR bits 16 and 17 are tied up (inactive) in the MSF ECC board.

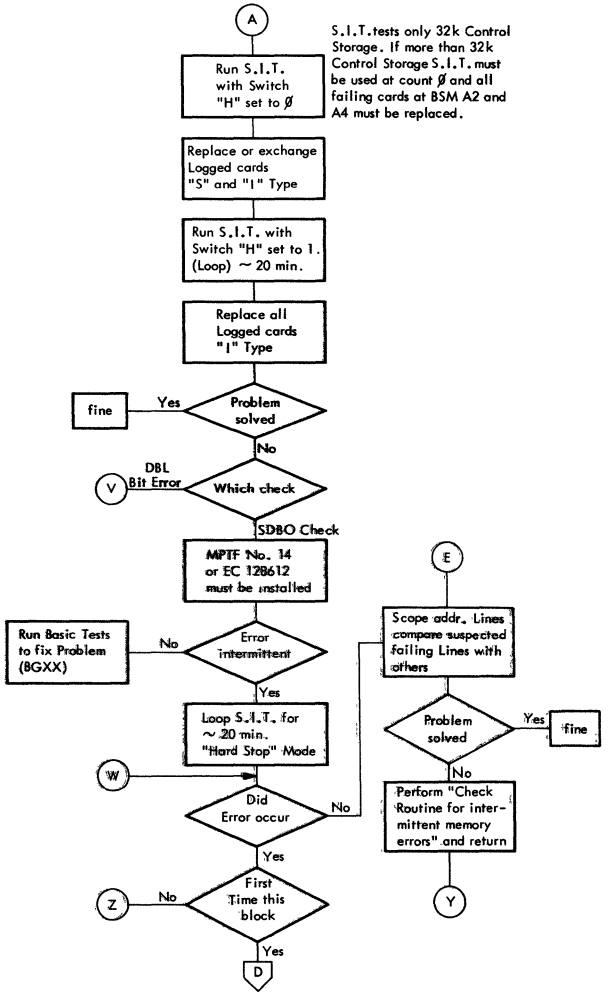
MEMORY TROUBLESHOOTING PROCEDURE

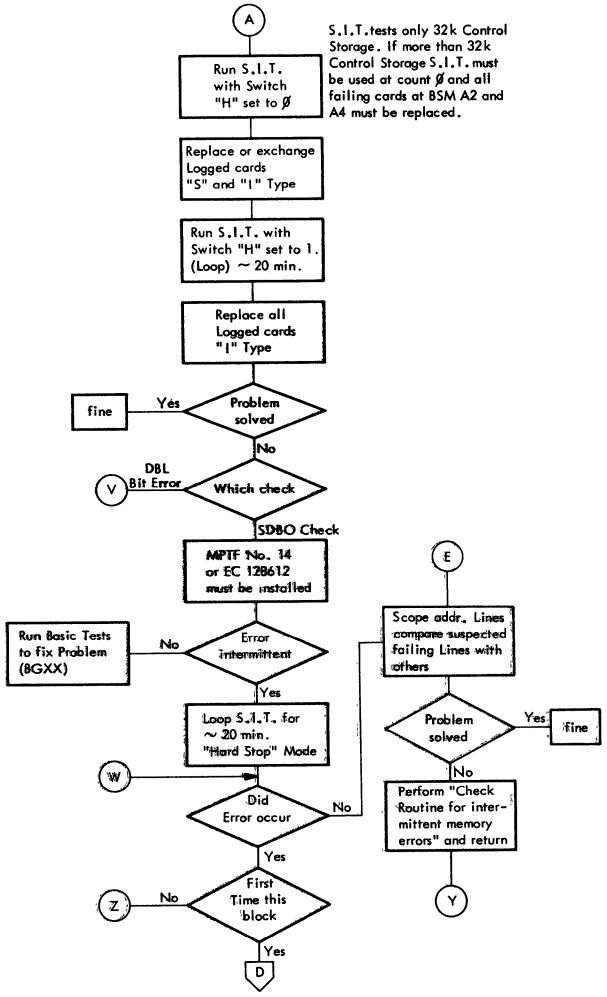
This is the 3145 troubleshooting procedure for machine checks when memory errors cannot be excluded

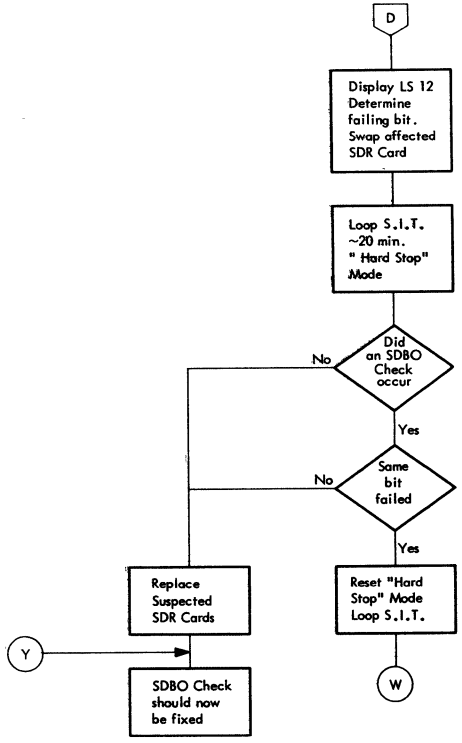


NOTE S I T test is in MBAO test after EC 128820

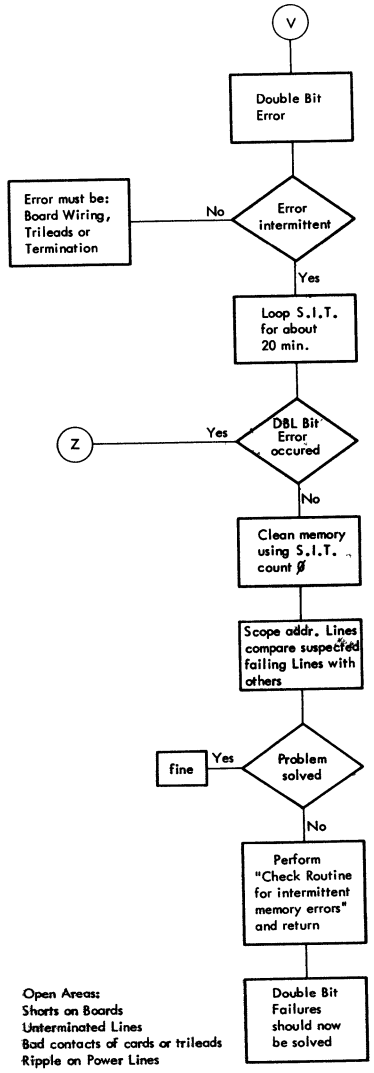




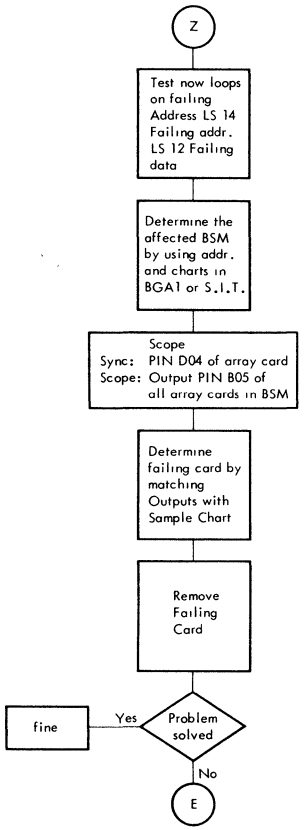




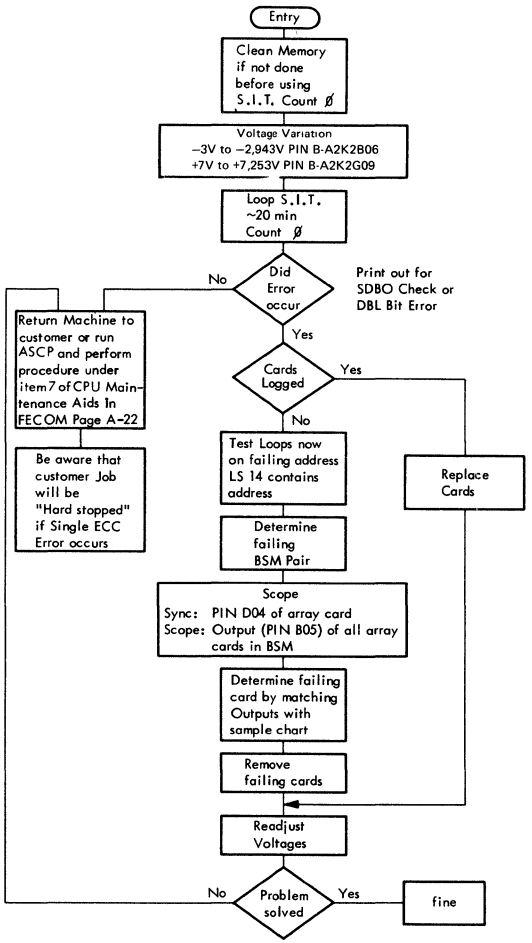
Open Areas:
Read Generator
(can be swapped with write Generator)
Unterminated Lines
Shorts on Boards
Bad contact of Card or Trilead
Ripple on Power Lines



Open Areas:
Shorts on Boards
Unterminated Lines
Bad contacts of cards or trileads
Ripple on Power Lines



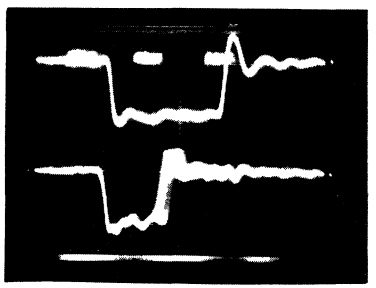
Check Routine for Intermittent Memory Errors

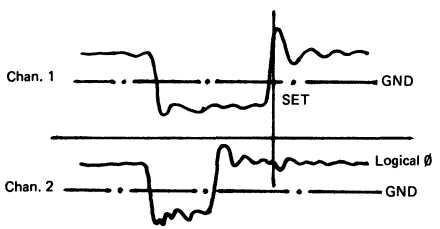


EXAMPLE CHART FOR ARRAY CARD OUTPUTS OF PHASE 2 I MEMORY

Sync· PIN D04 "SET"
Probe: PIN B05 "Data out"

Example 1 Good Output Zeros read

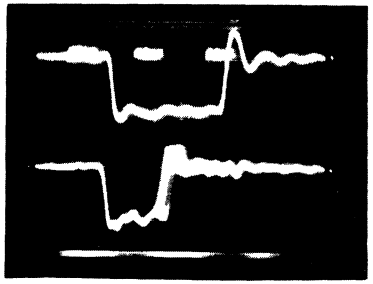


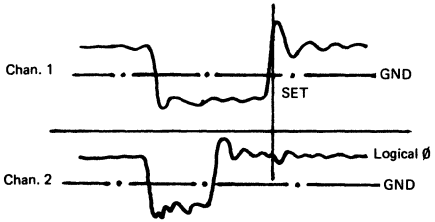


EXAMPLE CHART FOR ARRAY CARD OUTPUTS OF PHASE 21 MEMORY

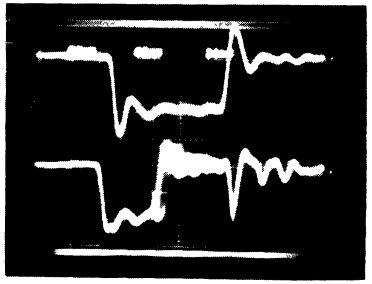
Sync: PIN D04 "SET"
Probe: PIN B05 "Data out"

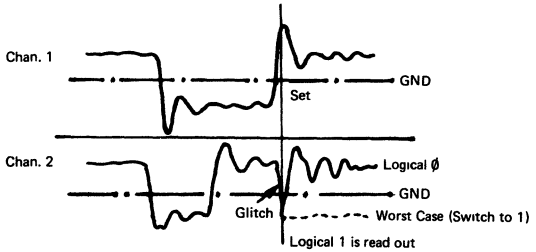
Example 1: Good Output Zeros read

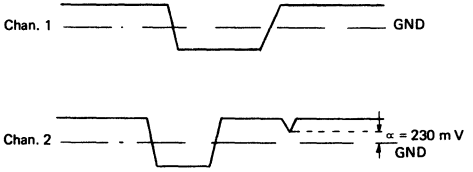




Example 2: Failing Output (Glitch) Zeros read



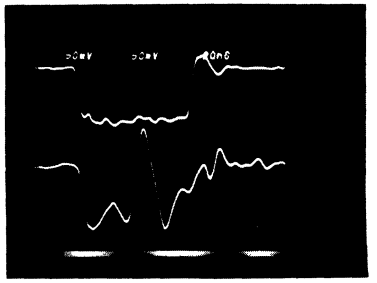




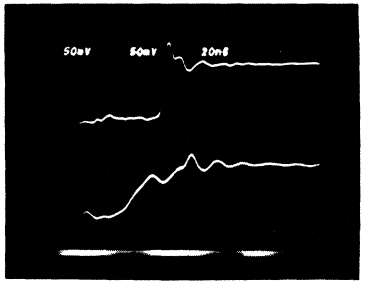
If under voltage variation "∝" is 230 m V or less card must be replaced.

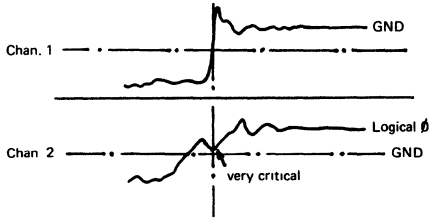
EXAMPLE CHART FOR ARRAY CARD OUTPUTS OF PHASE 21 MEMORY

Example 3: Failing Output (Bad slope) Zeros read



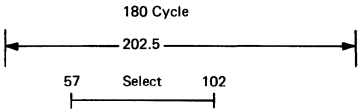
This spike has no effect.



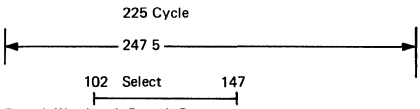


Cards with bad slopes must be replaced.

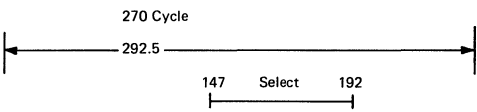
CYCLE LENGTH



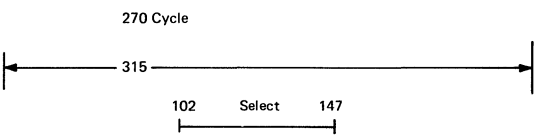
Branch Word W/O Branch Source
Move Word
Bal Word
Arithmetic Words (Byte Version)



Branch Word with Branch Source
Return Word
Arithmetic Word (Fullword or Decimal)
Storage 1 Cycle – Read



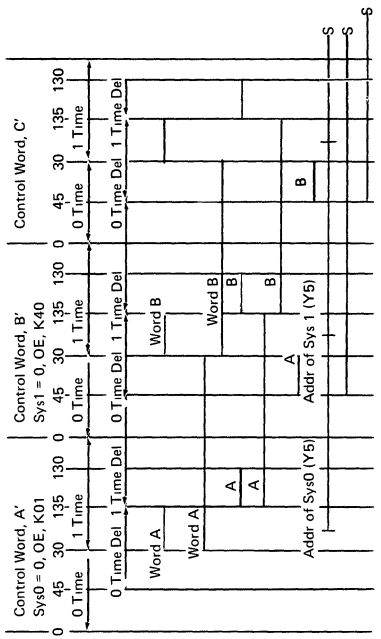
Storage 2 Cycle



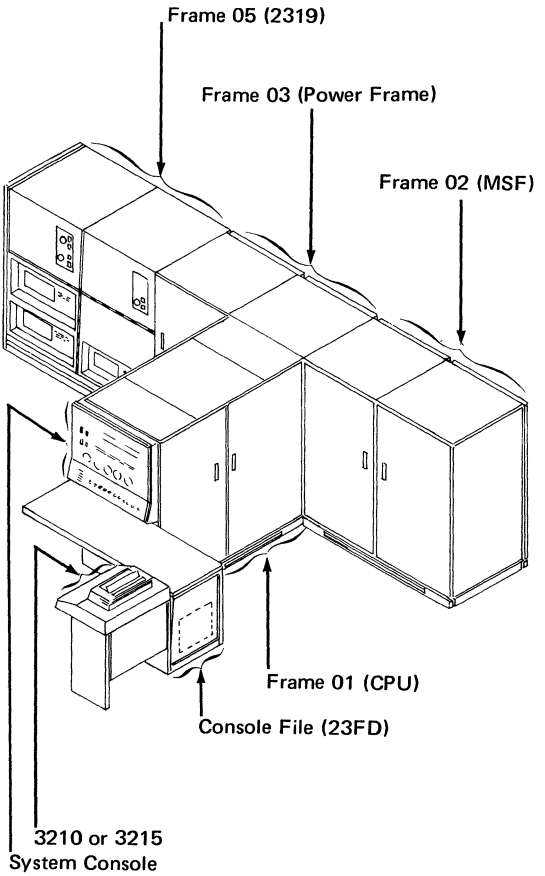
Storage 1 Cycle – Write

LOCAL STORAGE TIMING CHART

EXTERNAL DESTINATION TIMING CHART



NOTE Word A cycle is the destination time of Word A-1.
Word B cycle is the destination time of Word A
Word C cycle is the destination time of Word B


Frame 05 (2319)
Frame 03 (Power Frame)
Frame 02 (MSF)
Frame 01 (CPU)
Console File (23FD)
3210 or 3215
System Console

GATE LAYOUTS

	A	B	C
1	Backup Regs Stg Protect TOD Clock Sel Ch (Common)	Selector Channel 1 or Integrated File Adapter	M, N, MB Regs Traps and Priorities Branch Controls Interval Timer
2	Selector Channel 2 *SX4	External Assemblers Diagnostic Reg	A, B, Z, D, Regs ALU FTC Latches A, B Assemblers
3	Selector Channel 3 *SX4	External Assemblers	ALU Controls SPTL C Reg Decode Display Assembler
4	Console File MPX Channel System Reg Printer/KBD Manual Controls	C Reg SDBO Secondary Ctrl Asm LS 'A' Array Cards	LS Controls LS 'B' Array External Addressing Ctrls

'A' GATE (CARD SIDE)

* Several cards for Selector Channel 4 are in A2 and A3 boards

	A	B	C
1	Selector Channel 4 Direct Control	3215 Printer/Keyboard Channel to Channel	Clock Comparator and CPU Timer
2	Phase 21 Stg (Control Stg and High Main Stg)	Phase 21 STG (112 or 160K)	Phase 21 STG (208 or 256K)
3	ECC	Address-Adjust Circuits I.V.W.U. I.BU, TR Regs. Logical Regs.	Channel Ctrls LRU Reg CPU ADDR ADJ CTRLS I-Cycle Ctrl. Op Code and I Buffers
4	Phase 21 Stg (Control Stg and High Main Stg)	Phase 21 STG (112 or 160K)	Phase 21 STG (208 or 256K)

'B' GATE (CARD SIDE)

Board 01F-A1
(Behind Console)

Console Lamp Drivers Console-File Interface Drivers Printer/Keyboard Magnet Drivers & Lamp Drivers

Board 03A-A2
(Below CE Power Panel)

Under-Over Voltage Detect Power Sequence Relays Thermal/CB Detect Indicator Driver for Power Panel

Board 02A-A3

3345 ECC

Board 05A-A3

2319 IFA Mixer Board

CPU CLOCK INFORMATION

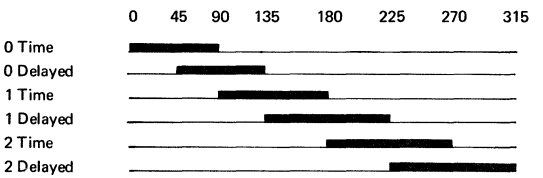
2

CLOCK CARD LOCATIONS	
A GATE	**B GATE**
A1 - K2	A1 - C4
A2 - C4	
A3 - C4	B3 - V3
A4 - Q4	
	C3 - J2
B1 - C4*	
B2 - M2	
B3 - H4	
B4 - K2	
C1 - G2	
C2 - J2	
C3 - G4	
C4 - E2	

PIN LOCATIONS OF TIMING PULSES ON EACH CLOCK CARD	
+0 Time–	G05
-0 Time–	J07
+0 Delayed–	D11
-0 Delayed–	G07
+1 Time–	B13
-1 Time–	J09
+1 Delayed–	J02
-1 Delayed–	J13
+2 Time–	J12
-2 Time–	G13
+2 Delayed–	D04
-2 Delayed–	G12
OSC Sync Point	G10

*B1-B4 if IFA

CLOCK TIMING CHART



CYCLE TIME FOR CONTROL WORDS

202.5 ns
247.5 ns
292.5 ns
315.0 ns

Note: Cycle times in the logic pages appear as 180, 225, 270 cycles– A delay of 22.5 nanoseconds is added to each of these cycles to obtain the cycle times of 202.5 to 292.5. Two delays are added to obtain the 315-cycle time. Refer to the control-word section for details on cycle times for each word type.

TRAP LOCATIONS AND ROUTINES

OPERATION	H-REGISTER BIT	TRAP ADDRESS	ROUTINE
Selector share cycles	None	None	
Machine check without I/O	H0	– –	
a. Normal		D000	GHEC
b. H0 is already on		D004	GHEC
c. One or more machine checks have already occurred (SYSO, Bit 2=1)		D008	GHEC
d. H0 and SYSO Bit 2 are already on		D00C	GHEC
Machine check with I/O	H0	– –	
a. Normal		D010	GHEC
b. H0 is already on		D014	GHEC
c. One or more machine checks have already occurred (SYSO, Bit 2=1)		D018	GHEC
d. H0 and SYSO Bit 2 are already on		D01C	GHEC
Retry	H1	– –	
a. Normal		D200	GHRT
b. H1 is already on		D204	GHRT
c. A retry trap operation is in progress (SYSO, Bit 1=1)		D208	GHRS
d. H1 and SYSO Bit 1 are already on		D20C	GHRS
CPU High	H2	– –	
a. Set IC		D300	GKCC
b. CA Trap		D304	GKCC
c. Address Contents		D308	GKCC
d. System Reset		D30C	GRST
IFA	H3	– –	
a. Mini-Op End		D128	GPBH
b. Error End		D12C	GPCG
c. Index		D124	GPCE
d. Gated Attn		D120	GPBK
Selector Channels 1, 2, 3 No IFA	H3	--	
a Exceptional Status Trap		D120	GSES
b. Chaining (CC or CD)		D124	GSTR
c. UCW Handling		D128	GSTR
d. Unused		D12C	GSTR
Selector Channels 2, 3 with IFA	H4	– –	
a. Exceptional Status Trap		D100	GSES
b. Chaining (CC or CD)		D104	GSTR
c. UCW Handling		D108	GSTR
d. Data (unchained)		D10C	GSTR

OPERATION	H-REGISTER BIT	TRAP ADDRESS	ROUTINE
Multiplexer	H5	D400	GMSR
IFA	H6	– –	
a. Return Low		D480	GPBK
b. Unused		D484	
c. Unused		D488	
d. Diagnostic		D48C	GPDO
Store/Display	H7	– –	
a. Store/Display		D840	GKAD
CPU Low without I/O	None	– –	
a. Spare		– –	
b. Storage Protect		D804	GICM
c. Address Check		D808	GICM
d. Address Adjust Exception		D80C	GGST
CPU Low with I/O	None	– –	
a. Spare		– –	
b. Storage Protect		D814	GMDR
c. Address Check		D818	GMDR
d. Spare		– –	
Scan/Clear	None	– –	
a. Scan Storage		D380	CSTS
b. Clear Storage		D384	CSTS
Single-Cycle Allow I/O and Soft CA Match	None	DC00	GKCC

H-Reg Bit	Blocks Trap Request for H-Reg Bit
H0	None
H1	H2, 3, 4, 5, 6, 7
H2	H2
H3	H3, 4, 5, 6
H4	H4, 5, 6
H5	H5, 6
H6	H6
H7	H7

FEATURE CODE LISTING

ACC Code	Feature
SC1	Sel Channel 1 Common
SC2	Sel Channel 2 Common
SC3	Sel Channel 3 Common
SC4	Sel Channel 4 Common
SPF	Integrated File Adapter
S4DC	Sel Channel 4 Common or Direct Control
SPK	Console SELECTRIC I/O 3210 1
DPK	Console SELECTRIC I/O 3210 2
MPK	Console Matrix Printer 3215
RC1	Real Time Channel 1
RC2	Real Time Channel 2
SB1	Sel Channel 1 (Buffered)
SB2	Sel Channel 2 (Buffered)
SB3	Sel Channel 3 (Buffered)
SB4	Sel Channel 4 (Buffered)
S75	Main Storage 208K
S08	Main Storage 256K
S09	Main Storage 384K or Greater System Storage
S10	Main Storage 512K
P05	Storage Protect up to 128K
DCT	Direct Control
TDC	Time-of-Day Clock
CHC	Channel to Channel
P02	Storage Protect Less Than 512
P08	Storage Protect 128K to 256K
P09	Storage Protect 256K to 384K
P10	Storage Protect 384K to 512K
S02	Main Storage 32K
S03	Main Storage 64K
S04	Main Storage 112K
S05	Main Storage 128K
S06	Main Storage 160K
BAS	Basic
MMA	C40/M21 Adapter
MM7	M21 Con & 256K MS
NP05	No Storage Protect up to 128K
SBC	Word Buffer, Common
SDPK	Console SELECTRIC 1 or 2
SNDK	Console SELECTRIC 1 or 2
NSC1	No Sel Channel 1
1CN2	Sel Channel 1 No Channel 2
2CN3	Sel Channel 2 No Channel 3
3CN4	Sel Channel 3 No Channel 4
NSPF	No System Prime File (IFA)
NSPK	No Console Sel I/O
NDPK	No Console Sel I/O Dual

ACC Code	Feature
NNPK	No Console Matrix Printer
1BN2	Sel Channel 1 Buff No Channel 2
2BN3	Sel Channel 2 Buff No Channel 3
3BN4	Sel Channel 3 Buff No Channel 4
NS75	No Main Storage 208K
NS08	No Main Storage 256K
NS09	256K or Less System Storage
NS10	No Main Storage 512K
NSX4	No Sel Channel 4
NSX3	No Sel Channel 3
NSX2	No Sel Channel 2
SUN2	Sel Channel 1 Unbuffered w/o Sel Channel 2
SF2U	Sel Channel 1 Unbuffered or IFA with Sel Channel Unbuffered w/o Sel Channel 3
SF2B	Sel Channel 1 Buffer or IFA with Sel Channel 2 Buffer w/o Sel Channel 3
SF3U	Sel Channel 1 Unbuffered or IFA with Sel Channel 2 and 3 Unbuffered w/o Sel Channel 4
SF3B	Sel Channel 1 Buffer or IFA with Sel Channel 2 and 3 Buffer w/o Sel Channel 4
SU14	Sel Channel 1 and 2 and 3 and 4 Unbuffered
SB14	Sel Channel 1 and 2 and 3 and 4 Buffer
MNSD	MPK and No Sel Channel 4 and No Direct Ctrl
DCN4	Direct Ctrl and No SX Channel 4
SBN2	Sel Channel 1 Buffer w/o Sel Channel 2
DSNM	Direct Ctrl or Common SX Channel 4 and No MPK and No CPT
DBNM	Direct Ctrl or SX Channel 4 Buffer and No MPK and No CPT
CPT	CPU Timer and Comparator
MNCP	Console Matrix Printer 3215 and No CPT
CMPK	Console Matrix Printer 3215 and CPT
CBNM	CPT and SX Channel 4 Buffer or DCT and No MPK
CSNM	CPT and SX 4 Common or DCT and No MPK
CNM4	CPT and No MPK and No DCT and No SX 4
NCPT	No CPU Timer and Comparator
SPNC	SPF and Any SX Channel and No CPT
S68	Storage Protect 160K to 256K
CNMB	CPT and No MPK and No DCT and No SX 4 Buffer
4BDM	MPK and DC or SX 4 Buffer
MNBD	MPK and No DC and Either No SX 4 Buffer or SX 4 Unbuffered

Acc Code	Feature
CNDB	CPT and No DC and No SX 4 Buffer
MNDC	MPK, and No DCT
DNMC	DCT, and No MPK, and No CPT
NDMC	No DCT, and No MPK and No CPT
CDNM	CPT and DCT, and No MPK
CNDM	CPT and No DCT and No MPK
DNCP	DCT and No CPT
NCPD	No CPT and No DCT
CPND	CPT and No DCT
CPDC	CPT and DCT
NP08	No Storage Protect 128K to 256K
NP09	No Storage Protect 256K to 384K
NP10	No Storage Protect 384K to 512K
NP20	No Storage Protect greater than 512K
NDCT	No Direct Control
NTDC	No Time-of-Day Clock
NCHC	No Channel-to-Channel
NP02	No Storage Protect Less Than 512K
MDPK	Console Matrix Printer and Console SELECTRIC I/O 2
SCPF	Sel Channel System Prime File Common
SC2F	Sel Channel 2 and System Prime File
SB2F	Sel Channel 2 Buffered and System Prime File
NCPF	No Sel Channel 2 and System Prime File
CHMP	Console Matrix Printer and Channel-to-Channel Adapter
SBPF	Sel Channel 1 Buffer or SPF
NBPF	No Buffer Sel Channel and System Prime File
NSDM	No SX 4 and No DCT and No MPK and No CPT
S4DM	SX 4 or Direct Control and MPK
DCMP	Direct Control and MPK
NDCM	No Direct Control and No MPK
PFNB	SX 1 Unbuffered or SPF
SC12	Sel Channel 1 and 2
SB12	Sel Channel Buffered 1 and 2
DC4B	Direct Control or SX Channel 4 Buffer
N4DC	No SX 4 and No DCT, No CPT
NB2F	No Sel Channel 2 Buffer and SPF
SMPK	Console Matrix Printer or Console
S1NB	Sel Channel 1 No Buffer
S2NB	Sel Channel 2 No Buffer
S3NB	Sel Channel 3 No Buffer
S4NB	Sel Channel 4 No Buffer
SBN2	Selector Buffered No Channel 2
SCN2	Selector Common No Channel 2

ACC Code	Feature
DBNC	Direct Ctrl or SX Channel 4 Buffer and No CPT
DBCP	Direct Ctrl or SX Channel 4 Buffer and CPT
CNMP	CPT and No MPK
SF1U	SX Channel 1 Buffer and No SX Channel 2 or SX Channel 1 Unbuffered or SPF and SX Channel 2 Unbuffer
IECC	Internal Error Correction Only

NOTE: See ALD A5000 for Feature B/M numbers or additions.

3145 ALD Version Codes	
Code	**Feature**
000	Basic
001	Matrix Printer (3215)
003	IFA
004	Selector Channel (Word Buffer)
005	Selector Channel (No Word Buffer)

List of Development Terms That May Appear in the Logics

Previous		Present	
SPF	System Prime File	IFA	Integrated File Adapter
LDF	Load Diag File	CF	Console File
Director		ISC	Integrated Storage Control

370 CORELOAD FEATURE PART NUMBER

Part Number	Description	
1953006	370 Coreload	
1953011	371 Coreload	Used for 3145 with multiple 370 coreloads
1953012	372 Coreload	
1953013	373 Coreload	
2646858	Honeywell Emulator (HONY)	
2646859	Honeywell with Stg Protect (HONYSP)	
2646866	RCA Emulator (RCA)	
2646877	ICL 1900 Emulator	
1953007	Basic CPU	
1953008	Extended Group Disk 1	
1953009	Extended Group Disk 2	
1953010	Extended Group Disk 4	
1953020	Extended Group Disk 3	
1795611	Alt Printer Addr 09	
1993036	3210 Mod 1 Adapter (SPK)	
1993528	Floating Point Arith (FLT PT)	
1993567	Direct Control (DC)	
1993576	Selector Channel 1 (CHNL 1)	
1993687	3210 Mod 2 Adapter (DPK)	
1993715	3215 Mod 1 Adapter (MPK)	
1993756	Integrated File Adapter (SPF)	
1993757	Selector Channel 2	(CHNL –)
1993758	Selector Channel 3	
1993759	Selector Channel 4	
1994587	64K Main Storage	(MEM ––– K)
1994588/ 2641161	112K Main Storage	
1994589/ 2641163/2646778	160K Main Storage	
1994590 2641165	208K Main Storage	
1994591 2641167/2646779	265K Main Storage	
1994720	Channel Buffer Common (BFRCHNL)	
2630246	Keyboard Printer Addr 09 (PKAD09)	
2630254	MSF Adapter 128K (MEMA128K)	
2630255	MSF Adapter 256K (MEMA256K)	
2630260	1401/1440/1460 Compatibility (CS14XX)	
2630261	14XX/7010 Combined (CSCOMB)	
2630262	32 MPX Sub Channels	(UCW –––)
2630263	64 MPX Sub Channels	
2630264	128 MPX Sub Channels	
2630265	256 MPX Sub Channels	

370 CORELOAD FEATURES PART NUMBER (Cont'd)

Part Number	Description
2630279	Block Multiplex Channel (BLK MPX)
2637208	Austrian/German Keyboard
2637209	Belgian/France Keyboard
2646791	English Keyboard
2637210	Danish/Norwegian Keyboard
2637211	Finnish/Swedish Keyboard
2637212	Italian Keyboard
2637213	Spanish Keyboard
2637214	United Kingdom Keyboard
2637215	Portuguese Keyboard
2641656	16 UCWs Group 01
2641657	32 UCWs Group 02
2641658	48 UCWs Group 03
2641659	64 UCWs Group 04
2641660	80 UCWs Group 05
2641661	96 UCWs Group 06
2641662	112 UCWs Group 07
2641663	128 UCWs Group 08
2641664	144 UCWs Group 09 (BMGRP —)
2641665	160 UCWs Group 10
2641666	176 UCWs Group 11
2641667	192 UCWs Group 12
2641668	208 UCWs Group 13
2641669	224 UCWs Group 14
2641670	240 UCWs Group 15
2641671	256 UCWs Group 16
2641672	272 UCWs Group 17
2641673	288 UCWs Group 18
2641674	304 UCWs Group 19
2641675	320 UCWs Group 20
2641676	336 UCWs Group 21
2641677	352 UCWs Group 22
2641678	368 UCWs Group 23
2641679	384 UCWs Group 24
2641680	400 UCWs Group 25
2641681	416 UCWs Group 26
2641682	432 UCWs Group 27
2641683	448 UCWs Group 28
2641684	464 UCWs Group 29
2641685	480 UCWs Group 30
2641686	496 UCWs Group 31
2641687	512 UCWs Group 32
2641864	Keyboard Printer Addr 1F (PKAD1F)
2641810	Comparator Clock and CPU Timer (CPT)

ALD PAGE INDEX

Indicators

Switches and Pushbuttons

ALD PAGE INDEX (Cont'd)

Registers

ALD PAGE INDEX (Cont'd)

S REG BITS 0,1,3	RS115
S REG BITS 2,4-7	RS214
S RETRY REG	RR114
SYSTEM REG BYTE 0	RS011
SYSTEM REG BYTE 1	RS011
SYSTEM REG BYTE 2	RS013
TA REG	PD011
TE REG	PD015
TI REG	PD021
TT REG	PD014
T REG BITS 0-3	RT012
T REG BITS 4-7	RT014
T RETRY REG	RR134
Z REG BYTE 0 BITS 0-3	AL144
Z REG BYTE 0 BITS 4-7	AL134
Z REG BYTE 1 BITS 0-3	AL124
Z REG BYTE 1 BITS 4-7	AL114
Z REG BYTE 2 BITS 0-3	AL144
Z REG BYTE 2 BITS 4-7	AL134
Z REG BYTE 3 BITS 0-3	AL124
Z REG BYTE 3 BITS 4-7	AL114

Functional Units

A BYTE ASM CTRLS	BA011
A BYTE ASM B ENTRY	BA015
A BYTE ASM BYTE 0 BITS P-7	BA021 BA022
A BYTE ASM BYTE 1 BITS P-7	BA023 BA024
A BYTE ASM BYTE 2 BITS P-7	BA025 BA026
A BYTE ASM BYTE 3 BITS P-7	BA027 BA028
A BYTE CTRLS S/R	BA013
ACB M REG COMP	MC013
ACB REG BYTE 0	MC015 MC017
ACB REG BYTE 1	MC016
ALU FUNCTION CTRLS	AC011
ALU GATE BA2 & BA3 HI & LO TO ALU 2 & 3	BK011
ALU BUS BYTE 3 BITS 0-7	AL113 AL123
ALU BUS BYTE 2 BITS 0-7	AL133 AL143
ALU HI INPUT ASM CTRLS	BB111
ALU LO INPUT ASM CTRLS	BB121
ALU A SW CTRLS & ALU S/R	AC014
ALU A SW GATE CTRLS	AC012
ALU A INPUT PARITY GATES	AM011 AM012
ALU 2 A INPUT BITS 4-7	AL131 AL132
ALU 2 A INPUT BITS 0-3	AL141 AL142
ALU 3 A INPUT BITS 4-7	AL111 AL112
ALU 3 A INPUT BITS 0-3	AL121 AL122
ALU CARRY-IN LATCHES	AM014
ALU CARRY & COMPL CTRLS	AC013
ALU 16 BIT CARRY LOOKAHEAD	AM015
ALU PARITY PREDICT & 4BIT HS CHECK	AL117 AL127
ALU PARITY PREDICT & 4BIT HS CHECK	AL137 AL147
ALU LOGICAL CHECK	AD011
ALU HS ERROR LATCHES	AM013
ALU DECIMAL CTRLS	AD012
ALU 2 4BIT HS TRANSMITTS & CARRIES	AL135 AL145
ALU 3 4BIT HS TRANSMITTS & CARRIES	AL115 AL125
ALU 4BIT GROUP CARRY COLLECTION FS	AL116 AL126
ALU 4BIT GROUP CARRY COLLECTION FS	AL136 AL146
A-REG BYTE 0 BITS P-4	RA111 RA112
A-RLG BYTE 0 BITS 5-7	RA121
A-REG BYTE 1 BITS P-4	RA122 RA131
A-REG BYTE 1 BITS 5-7	RA132
A-REG BYTE 2 BITS P-4	RA141 RA162
A-REG BYTE 2 BITS 5-7	RA151
A-REG BYTE 3 BITS P-4	RA152 RA161
A-REG BYTE 3 BITS 5-7	RA162
B BYTE ASM CTRLS	BA012
B BYTE CTRLS SYR	BA013
B BYTE ASM 2B INPUT ASM BITS P-7	BB112 BB123
B BYTE ASM 3B INPUT ASM BITS P-7	BB113 BB122

ALD PAGE INDEX (Cont'd)

ALD PAGE INDEX (Cont'd)

C-REG BYTES 0-3 BIT P	RC111
C-REG BYTES 0-3 BIT 0	RC121
C-REG BYTES 0-3 BIT 1	RC131
C-REG BYTES 0-3 BIT 2	RC141
C-REG BYTES 0-3 BIT 3	RC151
C-REG BYTES 0-3 BIT 4	RC161
C-REG BYTES 0-3 BIT 5	RC171
C-REG BYTES 0-3 BIT 6	RC181
C-REG BYTES 0-3 BIT 7	RC191
C REG BYTE 0 DECODE 1-2	DC011 DC012
C REG BYTE 0 DECODE 3-4	DC013 DC014
C REG BYTE 1 DECODE 0-7	DC022 DC022
C REG BYTE 2 DECODE P-7	DC023
C REG BYTE 2 BITS 4-7 BFR	BK012
DESTINATION BYTE CTRLS	KD011-KD015
DISPLAY ASM BYTE 0	PB011-PB015
DISPLAY ASM BYTE 1	PB021-PB025
DISPLAY ASM BYTE 2	PB031-PB035
DISPLAY ASM BYTE 3	PB041-PB045
D-REG BYTE 0 BITS P-4	RA115 PA116
D-REG BYTE 0 BITS 5-6	RA125
D-REG BYTE 1 BITS 0-5	RA126 RA135
D-REG BYTE 1 BITS 6-7	RA136
D-REG BYTE 2 BITS P-4	RA145 RA146
D-REG BYTE 2 BITS 5-7	RA155
D-REG BYTE 3 BITS 0-5	RE156 RA165
D-REG BYTE 3 BITS 6-7	RA166
DIRECT CTRL INTERFACE	WR071
DIRECT CTRL INTERF BUS TAG	JA021-JA151
DIAG REG	RD021
DIAG CTRLS	RD022
DIAG MANUAL CTRL	KD111 KD112
DOC CTRL INTERFACE	WP011 WP012
DOC CONSOLE HD WR CYCLE CTRL	PD012 PD013
DOC CONSOLE WP DATA REG	PD015
DOC CONSOLE KEYBOARD INTERFACE	PD021 PD022
DOC CONSOLE MAGNET DRIVER	PD031-PD121
DOC CONSOLE PRINTER SW & CTRLS	PA361-PA381
EPSW A B REG	RM812
EXT ASM GATES	BE111 BE121
EXT ASM GATES	BE151 BE161
EXT ASM BYTE 0 BITS P-2	BE112 BE113
EXT ASM BYTE 0 BITS 3-7	BE114 BE122
EXT ASM BYTE 0 BIT 7	BE123
EXT ASM BYTE 1 BITS P & 0	BE132
EXT ASM BYTE 1 BITS 3 & 4	BE124
EXT ASM BYTE 1 BITS 1 & 5	BE133
EXT ASM BYTE 1 BITS 6 & 7	BE134
EXT ASM BYTE 2 BITS P-2	BE142 BE143
EXT ASM BYTE 2 BITS 3-6	BE146 BE152
EXT ASM BYTE 2 BIT 7	BE153
EXT ASM BYTE 3 BITS 2-4	BE153 BE154
EXT ASM BYTE 3 BITS P & 0	BE162
EXT ASM BYTE 3 BITS 1 & 5	BE163
EXT ASM BYTE 3 BITS 6 & 7	BE164
EXT BUS IN DRIVERS BYTE 0	RC211 RC212
EXT BUS IN DRIVERS BYTE 1	RC221 RC222
EXT BUS IN DRIVERS BYTE 2	RC231 RC232
EXT BUS IN DRIVERS BYTE 3	RC241 RC242
EXT CTRL ASM MISC	DE001 DE002
EXT CTRL ASM MISC	DE003 DE004
EXT CTRL ASM MISC	DE005 DE006

ALD PAGE INDEX (Cont'd)

EXT CTRL ASM SOURCE DECODE	DE011 DE012
EXT CTRL ASM SOURCE DECODE	DE013 DE014
EXT CTRL ASM SOURCE DECODE	DE015 DE016
EXT INTERRUPT-REG P-0	RM813
EXT DECODE BFR	RR119 RR129
EXT DECODE BFR	RR139 RR149
EXT DESTINATION DECODE	DE021 DE023
EXT DESTINATION ADDRESS LT	DE022 DE024
EXT DEST X DECODE	DE026
EXT DEST Y DECODE	DE025 DE027
EXT FEATURE SOURCE DECODE	DF011-DF016
EXT INTERRUPT REG	JA011 JA012
EXP EXT ASM BYTE 0 BITS P-2	BF112 BF113
EXP EXT ASM BYTE 0 BITS 3-6	BF114 BF122
EXP EXT ASM BYTE 0 BIT 7	BF123
EXP EXT ASM BYTE 1 BITS P&0	BF122
EXP EXT ASM BYTE 1 BITS 2-4	BF123 BF124
EXP EXT ASM BYTE 1 BITS 1&5	BF133
EXP EXT ASM BYTE 1 BITS 6&7	BF134
EXP EXT ASM BYTE 2 BITS P-2	BF142 BF143
EXP EXT ASM BYTE 2 BITS 3-6	BF144 BF152
EXP EXT ASM BYTE 2 BIT 7	BF153
EXP EXT ASM BYTE 3 BITS P&0	BF162
EXP EXT ASM BYTE 3 BITS 2-4	BF153 BF154
EXP EXT ASM BYTE 3 BITS 1&5	BF163
EXP EXT ASM BYTE 3 BITS 6&7	BF164
FTC ERROR BITS P-1	RA125 RA156
FTC ERROR BITS 6-7	RA166
FLUSH THRU CHECK ERROR	RE025
FTC ERROR 1 & S/R	RA116
FTC ERROR 2	RA126 RA127
FTC ERROR 3	RA136 RA137
FTC ERROR 4	RA146 RA147
FTC ERROR 5	RA157
FTC ERROR 6	RA167
H-REG BITS 0-7	RH022 RH023
H-REG BACK-UP REG	RR125
H-REG PARITY CHECK	RH021
I/O REQUEST	RH032
K ASM BITS 0-7 LATCHES	BK015
K ASM FORCE BITS P,5-7	BK014
L-REG BITS P-7	RL011
L-REG BACK-UP REG	RR144
LS CONTROLS	MB111 RC092
LS GATES BYTES 0-3	LC011
LS A DEST ADDR LT X	LA212
LS A DEST ADDR LT Y	LA222
LS A B FAST X ADDRESS	LA011-LA018
LS A FAST Y ADDRESS	LA111-LA117
LS A SLOW X ADDR ASM	LA211
LS A SLOW Y ADDR ASM	LA221
LS B DEST ADDR LT X	LA232
LS B DEST ADDR LT Y	LA242
LS B FAST Y ADDRESS	LA121-LA127
LS B SLOW X ADDR ASM	LA231
LS B SLOW Y ADDR ASM	LA241
LS MISC X ADDRESS CTRLS	LA021-LA024
LS MISC Y ADDRESS CTRLS	LA031-LA034
LS 64 X 18 MONO BUFFER	LA311-LA347
LS SEL CHAN ADDR FORCE	BB012
LS A B COMPARE ERROR 1&2	RA117 RA127
LS A B COMPARE ERROR 3&4	RA137 RA147
LS A B COMPARE ERROR 5&6	RA157 RA167

2

ALD PAGE INDEX (Cont'd)

MANUAL STORE DISPLAY	KM011-KM031
MASK A-REG 4 INTRA REG	RJ011
MASK B-REG 4 INTRA REG	RJ012
MCK-REG CTRLS	RE011-RE015
MCK-REG A BYTE 0 BITS P-7	RE021 RE022
MCK-REG A BYTE 1 BITS P-7	RE022-RE024
MCK-REG A BYTE 2 BITS P-7	RE031-RE033
MCK-REG A BYTE 3 BITS P-7	RE034-RE036
MCK COUNTER	RE053
MCK-REG B BYTE 0 BITS P-7	RE041-RE045
MCK-REG B BYTE 1 BITS P-7	RE046-RE051
MCK-REG B BYTE 3	RE052
MEMORY CTRL	MS011-MS015
M-REG DATA GATES A&B	RM111 RM114
M-REG DATA GATES A&B	RM114-RM124
M-REG SET-RESET CTRLS	RM112 RM113
M-REG SET-RESET CTRLS	RM122
M-REG LATE SET-RESET CTRLS	RM123
M-REG DUP CHECK ASM	RM061-RM064
M-REG DUP CHECK	RD024
MB REG BYTE 3 BITS P-3	PM013
MB-REG BYTE 2 BITS P-7	RM035
M1 REG	MC011 MC022
M2 REG BYTE 1 CTRL	MC014
M2-REG BACK-UP	RR135
M2-REG PRE ASM P-7	RM021
M2-REG BYTE 2 BITS P-3	RM031 RM033
M2-REG BYTE 2 BITS 4-7	RM032
M3-REG BITS P,0,2	RM041 RM043
M3-REG BITS 1,3	RM044
M3-REG BITS 6-7	RM052
M3 BITS 4-5 ASM A	RM214 RM215
M3 BITS 4-5 ASM B	RM224 RM225
M3-REG PARITY GEN & CHECK	RM065
M3-REG BACK-UP	RR145
MPX INTERFACE	WA011
MPX CHANNEL TAGS & REG & DECODE	FA011-FA151
M2-REG BYTE 2BITS P-2	RM033

NOTE: I-Cycle HDV RUXXX and RVXXX

NOTE: ECC board logics are the SQXXX pages. One set of logics serve internal and external storage. The entry and exit pages differ, and have separate page numbers, ie,

SQ800 – Internal SQ130 – Internal
SQ805 – External SQ145 – External

NOTE: Power logics for:

Stage I	Stage II
YE	YB - Power logic pages
YD	YA - Voltage detection board pages

	SYSTEM CHECKS																	SYSTEM CHECKS																			
	(R)	(R)	(R)	○	(R)	○	(R)	(R)	(R)	(R)	(R)	(R)	(R)	○	○	○	(R)	○	(R)	(R)	(R)	○	○	(R)	○	(R)	(R)	(R)	(R)	○	○	○	○	○	○	○	○
IND NAME	CPU	RETRY	CLOCK SYNC		DIAGN STOP		M REG COMP	SAR	SDBI	SDBO PARITY	STOR BYTE MARKS CHECK	STOR CTRL LINES	STOR PROT				SEL CHAN		HDW	ECC DBL BIT	BUSY			I CYCLE HDW		ADDR X LATE LRU INVALID	MULTI MATCH	NO MATCH								POWER	THERM
DRIVER	PL142	PL152	PL142		PL 142		PL141	PL142	PL142	PL142	PL142	PL151	PL142				PL142		PL151	PL151	PL151			PL151		PL152	PL151	PL151								YD612	YD612
SOURCE	RE011	RS011	RE045		KF025		RE046	RE041	RE041	RE041	RE041	RE051	RE043				GA111		RE051	RE051	RE051			RE051		RE044	RE044	RE044								YD721	YD721

	CPU STATUS																		CONSOLE FILE								CONSOLE FILE REGISTERS									
	○	○	○	○	○	○	○	○	○	(A)	○	○	○	(A)	○	○	○	(A)	(R)	(R)	(R)	(R)	(R)	(R)	○	○	○	(A)	○	○	○	○	○	○	○	○
IND NAME	EXE CPLT	ADR COMP MATCH	CLOCK STOP	CORR	STOR 1	TRAP 1 CYCLE	TRAP 2	I	SHARE	SNG ECC THLD	EC MODE	CS ADR	ADR X LATE MODE	TOD CLOCK INVLD	LOG PRES	SNG ECC	CF PWR ON	IMPL REQD	DATA	CMND REG	DISK ADR REG	BYTE CNTR	PAUSE	CPU CLOCK START			CNTR MATCH	P	0	1	2	3	4	5	6	7
DRIVER	PL141	PL141	PL141	PL141	PL141	PL152	PL161	PL152	PL152	PL161	PL141	PL152	PL152	PL151	PL141	PL151	PL141	PL141	PL161	PL161	PL161	PL161	PL161	PL161			PL161	PL162	PL162	PL162	PL162	PL162	PL162	PL162	PL162	PL162
SOURCE	KM024	KM024	PM021	PM022	KM024	KM024	RE053	RU054	JG032	RE062	RE011	RE053	RM074	CT112	RS011	RE051	KF042	RS013	KF042	KF036	KF036	KF071	KF022	KF022			KF071	KF035	KF072	KF072	KF072	KF072	KF072	KF072	KF072	KF072

POWER ON YE280

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IND NAME	SYS	MAN	WAIT	TEST	LOAD
DRIVER	PL132	PL132	PL132	PL132	PL132
SOURCE	PM021	KM024	KM024	PM021	RS013

Position 3 Control Register

C REG	MICROPROGRAM CONTROL REG BYTE 0				P	MICROPROGRAM CONTROL REG BYTE 1	P	MICROPROGRAM CONTROL REG BYTE 2	P	MICROPROGRAM CONTROL REG BYTE 3
	WORD TYPE 0	1	2	3				NOTE IF STOR 1 CYCLE OFF C REG = NEXT CONTROL WORD IF STOR 1 CYCLE ON C REG = CURRENT CONTROL WORD		
RC111	RC121	RC131	RC141	RC151	RC161	RC171	RC181	RC191	RC111	RC131	RC131	RC141	RC151	RC161	RC171	RC181	RC191	RC111	RC121	RC131	RC141	RC151	RC161	RC171	RC181	RC191	RC111	RC121	RC131	RC141	RC151	RC161	RC171	RC181	RC191

2

Position 4 MB 2, MB 3, N2, N3

MB REG	STORAGE BACKUP ADR REG BYTE 2								P	STORAGE BACKUP ADR REG BYTE 3								N REG	NEXT CONTROL WORD ADR REG BYTE 2	P	NEXT CONTROL WORD ADR REG BYTE 3															
	NOTE IF NOT IN STOR 1 CYCLE MB REG = ADDRESS OF LAST CONTROL WORD EXECUTED IF IN STOR 2 CYCLE (AFTER STOR 1 CYCLE ON) MB REG = BYTE 2 and 3 OF DATA ADDRESS																		NOTE IF TRAP 1 CYCLE OFF N REG = NEXT CONTROL WORD ADDRESS IF TRAP 1 CYCLE ON N REG = LINK ADDRESS FOR TRAP															
RM035	RM035	RM035	RM035	RM036	RM035	RM035	RM035	RM035	RM073	RM073	RM073	RM073	RM073	RM051	RM051	RM052	RM052	RM033	RM033	RM033	RM033	RM034	RM034	RM034	RM034	RM034	RM045	RM045	RM045	RM045	RM045	RM051	RM051	RM052	RM052

Position 5 B-Register

B REG	B REGISTER BYTE 0								P	B REGISTER BYTE 1								P	B REGISTER BYTE 2	P	B REGISTER BYTE 3															
																			NOTE B-REGISTER BYTES 0 1 = INPUT TO Z REG BYTES 0-1 B-REGISTER BYTES 0 3 = B SOURCE INPUT TO ALU/OUTPUT FROM B LOCAL STORAGE																			
RA113	RA113	RA113	RA114	RA114	RA114	RA123	RA123	RA123	RA124	RA124	RA142	RA133	RA133	RA133	RA134	RA134	RA134	RA143	RA143	RA143	RA144	RA144	RA144	RA153	RA153	RA153	RA154	RA154	RA154	RA163	RA163	RA163	RA164	TA164	RA164

Position 6 Z-Register

Z REG	Z REGISTER BYTE 0								P	Z REGISTER BYTE 1								P	Z REGISTER BYTE 2	P	Z REGISTER BYTE 3															
																			NOTE Z-REG BYTES 0 3 OUTPUT OF ALU IN PRESENT CYCLE Z-REG BYTES 0 3 INPUT TO SPTL REGS AND D REG																			
AL147	AL144	AL144	AL144	AL144	AL134	AL134	AL134	AL134	AL127	AL124	AL124	AL124	AL124	AL114	AL114	AL114	AL114	AL137	AL144	AL144	AL144	AL144	AL134	AL134	AL134	AL134	AL117	AL124	AL124	AL124	AL124	AL114	AL114	AL114	AL114

Position 7 D-Register

D REG	D REGISTER BYTE 0								P	D REGISTER BYTE 1								P	D REGISTER BYTE 2	P	D REGISTER BYTE 3															
																			NOTE D REGISTER BYTES 0 3 = OUTPUT FROM Z REGISTER IN LSST CYCLE																			
RA115	RA115	RA115	RA115	RA116	RA116	RA125	RA125	RA125	RA125	RA126	RA126	RA135	RA135	RA135	RA135	RA136	RA136	RA145	RA145	RA145	RA145	RA146	RA146	RA155	RA155	RA155	RA155	RA156	RA156	RA165	RA165	RA165	RA165	RA166	RA166

Position 8 MC Register (MCKA External Address 06)

MCKA	LS A SORC ADR	LS B SORC ADR	LS A DEST ADR	LS B DEST ADR	DEST BYTE CTRL	LA A,B DEST ADR	LS CTRL ASM	C REG PTY	P	ACB REG PTY	COMP LS COMP	FLUSH THRU	H REG PTY		P REG PTY	T REG PTY	L REG PTY	P	ALU 2 HALF SUM	ALU 2 HALF SUM	ALU LOGL	B REG SHIFT	A REG SHIFT	B REG SHIFT	Z REG PTY	D REG PTY	P	EXT DEST X	EXT ESDT Y	TXT SORC Y	EXT CTRL AMS	INTV TIMER PTY	S REG DUP	TOD CLOCK	CS ADR
RE022	RE021	RE021	RE021	RE021	RE022	RE021	RE021	RE021	RE022	RE023	RE023	RE023	RE023		RE024	RE024	RE024	RE036	RE031	RE031	RE032	RE031	RE033	RE033	RE033	RE033	RE036	RE035	RE035	RE035	RE035	RE034	RE034	RE034	RE034

Position 3 S,P,T,L Registers

S REG	TRUE CPMT	BIT 1 CARRY	Z = 0	BIT 0 CARRY	Z HI ZERO	Z LO ZERO	GENERAL PURPOSE	P REG	LOCAL STORAGE OR EXTERNAL ADDRESSING: A EXP LS	P HIGH			B EXP LS	P LOW			T REG	T HIGH: 0	1	2	3	T A: 2	1	T B: 2	1	L REG	LOCAL STORAGE INDIRECT ADDRESSING: L HIGH				L LOW			
RS116	RS115	RS115	RS124	RS115	RS214	RS214	RS214	RS214	RP011	RP011	RP011	RP011	RP011	RP012	RP012	RP012	RP012	RP014	RT012	RT012	RT012	RT012	RT013	RT013	RT013	RT013	RL011	RL011	RL011	RL011	RL011	RL011	RL011	RL011	RL011

Position 4 System Register

SYS REG 0	MACH IRPT PEND	RETRY RTNE	MACH CHK MARK	3210 MOD 2	LOG PRES	SUB BLOCK MODE	SELR I/O OP	LS CS MODE	SYS REG 1	ADR CNTS	CPU IRPT FORCE	SAR IRPT FORCE	PSW RST		SYS CTRL IRPT	TIMER IRPT FORCE		SYS REG 2	SYS CLEAR	IMPL	CNSL FILE WAIT	CE MODE	01 PWR RST 10 SUB LOAD 11 SYS LOAD			INST PROC	H REG	MACH CHECK	RETRY	CPU HIGH	NO IFA: SX1 IFA	SX4 SX2,3	MPX	IFA	DOCM A/D
RS011	RS011	RS011	RS011	RS011	RS011	RS011	RS011	RS011	RS012	RS012	RS012	RS012	RS012	N/A	RS012	RS012	N/A	RS013	RS013	RS013	RS013	KM012	RS013	RS013	N/A	RS013	RH025	RH022	RH022	RH022	RH022	RH022	RH022	RH023	RH023

Position 5 Chan Interface, See Notes 2 and 4 (Page 5-12)

FTO	CYL	HEAD	DIFF	CTRL	CUA LD	SPF TAGS			FTI	128	64	32	16	8	4	2	1	FBO	FILE BUS-OUT								FDR	FILE DATA REGISTER							
GTO	OP-O	SEL)	ADR-O	CMD)	SERV-O	DATA-O	SUP-O	TAGS	GTI	OP I	ADR-I	STAT I	SERV-I	SEL I	DATA I	REQ I	DISC I	GO	SELECTOR CHANNEL BUS OUT								GR	SELECTOR CHANNEL DATA REGISTER							
MTO	OP-O	SEL O	ADR-O	CMD-O	SERV O	IRPT	SUP-O	OUT	MTI	OP I	ADR-I	STAT I	SERV-I	SEL-I	REQ-I	TRAP	DISC I	MBI	MULTIPLEX CHANNEL BUS IN								MBO	MULTIPLEX CHANNEL BUS-OUT							
JK114	JK112	JK112	JK112	JK112	JK112	JK112	JK112	JK112	JK214	WF101	WF101	WF101	WF101	WF101	WF101	WF101	WF101	JK311	JK311	JK311	JK311	JK311	JK311	JK311	JK311	JK311	JK412	JK411	JK411	JK411	JK411	JK411	JK412	JK412
GB612	GB313	GB213	GB312	GB312	GB113	GB113	GB212	GB612	GB622	GB621	GB621	GB621	GB621	GB621	GB621	GB621	GB621	GB082	GB082	GB082	GB082	GB082	GB082	GB082	GB082	GB082	GB611	GB611	GB611	GB611	GB611	GB611	GB611	GB611
FA013	FA013	FA013	FA013	FA013	FA013	FA013	FA013	FA013	FA012	FA012	FA131	FA131	FA131	FA141	FA141	FA012	FA141	FA111	FA111	FA111	FA111	FA121	FA121	FA121	FA121	FA131	FA014	FA014	FA014	FA014	FA014	FA014	FA014	FA014

Position 6 Chan Word A, See Notes 3 and 4 (Page 5-12)

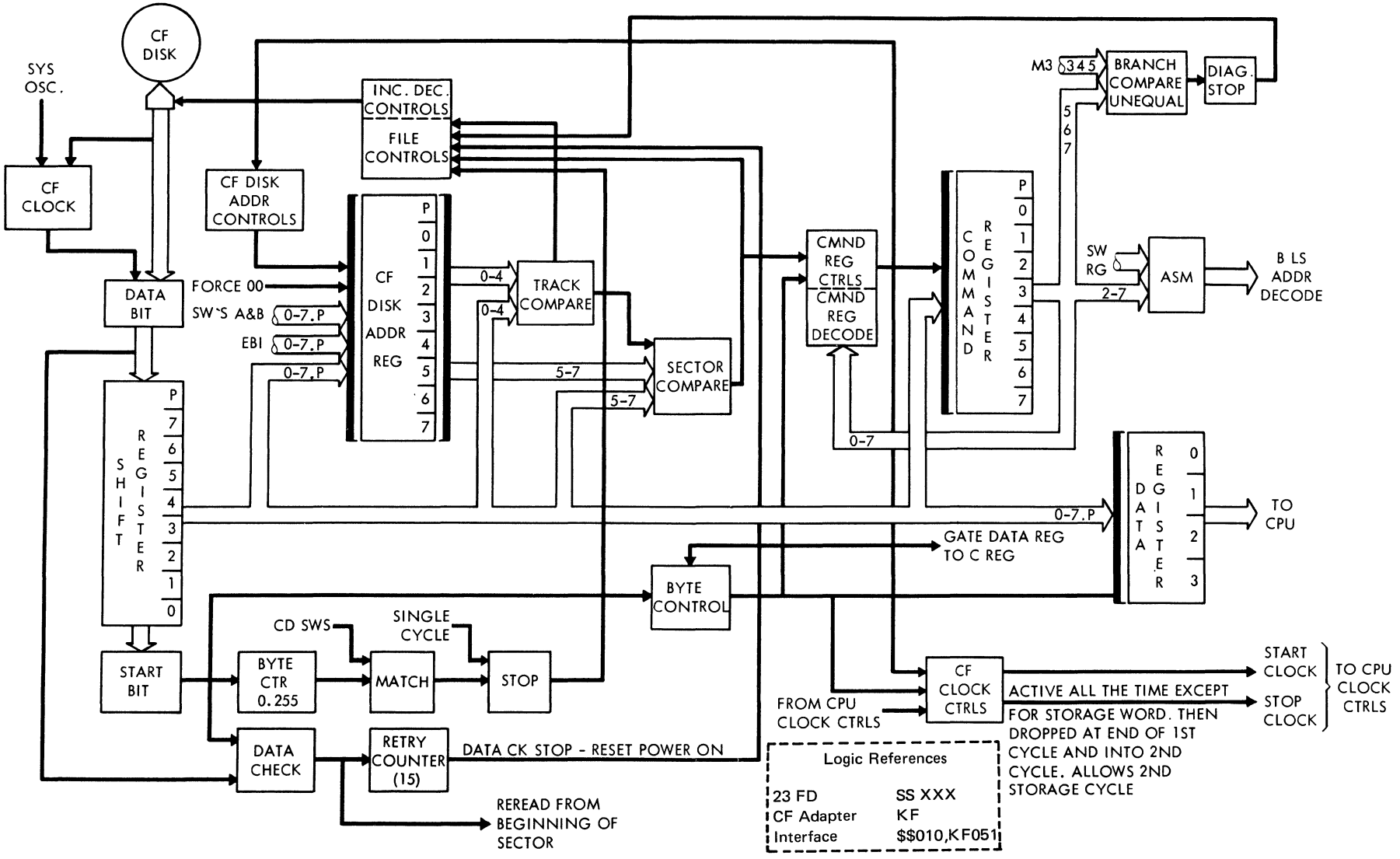
FFL GE	CD	CC	SLI	SKIP	ALLOW HALT	IN IN FWD	CS CT READY IN BWD	OUT	FCS GE	PCI	IL	PROG CHK	PROT CHK	DATA CHK	CTRL CHK	INTF CHK	CHAIN CHK	FST GS	CHAN BUSY	IRPT LTH	CUE POLL CTRL	CUB PRIME	DCC MODE	CMD RETRY	GATE A	GATE B	FGL GL	COUNT READY	COUNT ZERO	GR FULL	IRPT CND	SHARE ERROR		POSITION CODE	
JK114	JK111	JK111	JK111	JK111	N/A	JK512	JK512	JK512	JK214	JK111	JK513	JK212	JK212	JK212	JK212	JK212	N/A	JK314	JK313	JK313	JK313	JK313	N/A	N/A	JK313	JK313	JK414	JK512	JK512	JK511	JK416	JK513	N/A	JK612	JK612
GB611	GB712	GB712	GB712	GB712	GB313	GB412	GB412	GB412	GB621	GB721	GB411	GB411	GB411	GB411	GB412	GB114	GB513	GB631	GB213	GB213	GB313	GB211	GB213	GB513	GB633	GB643	GB641	GB413	GB413	GB311	GB413	GB412	N/A	GB711	GB711

Position 7 Chan Word B, See Notes 3 and 4 (Page 5-12)

FDS	BUSY	DISK STATUS: ON LINE	UNSAFE	PACK CHNG	EOC	MULTI MOD	SEEK ICPTL	FHC GBF	HEAD CYLINDER SWITCHES: 128	64	32	16	8	4	2	1	FED GCT	CE INLINE DISPLAY REGISTER: BFR CTL CK		CD REQ	BFR PTN	GCL: 0	1	2	3	FMOD	MODULE SELECTED: 0	1	2	3	SELECTED MODULE: 4	5	6	7
										BF 6	BF-5	BF-4	BF 3	BF 2	BF 1	BF 0															GDL-0	GDL-1	GBP	0	1	2	3
JK114	WF101	WF101	WF101	N/A	WF101	WF101	JK511	WF101	JK214	WF102	WF102	WF102	WF102	WF102	WF102	WF102	WF102	JK314	JK312	JK312	JK312	JK312	JK312	JK312	JK312	JK312	JK414	JK611	JK611	JK611	JK611	JL511	JK511	JK511	JK511
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	GC621	N/A	GC311	GC311	GC311	GC311	GC312	GC312	GC312	GC632	GC513	N/A	GC413	GC412	GC412	GC412	GC412	GC412	N/A	N/A	GC414	GC414	N/A	GC411	GC411	GC411	GC411

Position 8 Chan Word C, See Notes 3 and 4 (Page 5-12)

GB-0		SEL CHAN BUFFER BYTE 0							FCH GB 1	COUNTER HIGH: 32K	16K	8K	4K	2K	1K	512	256	FCL GB 2	COUNTER LOW: 128	64	32	16	8	4	2	1	FOP GB-3	ADR: READ	WRITE	MARK	SRCH	INDEX: SCAN	START	FORMAT	SKIP
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	JK211	JK211	JK211	JK211	JK211	JK211	JK211	JK211	JK211	JK311	JK311	JK311	JK311	JK311	JK311	JK311	JK311	JK311	SEL CHAN BUFFER, BYTE 2				SEL CHAN BUFFER, BYTE 3			
GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC115	GC114	GC114	GC114	GC114	GC114	GC114	GC114	GC114	GC114	JK412	JK411	JK411	JK411	JK411	JK411	JK411	JK412	JK412
																											GC114	GC114	GC114	GC114	GC114	GC114	GC114	GC114	GC114


CF DISK
SYS OSC.
CF CLOCK
INC. DEC. CONTROLS
FILE CONTROLS
CF DISK ADDR CONTROLS
DATA BIT
FORCE 00
SW'S A&B
EBI
0-7.P
0-7,P
CF DISK ADDR REG
P 0 1 2 3 4 5 6 7
0-4
TRACK COMPARE
5-7
SECTOR COMPARE
CMND REG CTRLS
CMND REG DECODE
COMMAND REGISTER
M3
3 4 5
BRANCH COMPARE UNEQUAL
DIAG. STOP
5 6 7
SW RG
2-7
ASM
B LS ADDR DECODE
SHIFT REGISTER
P 7 6 5 4 3 2 1 0
START BIT
BYTE CTR 0.255
CD SWS
SINGLE CYCLE
MATCH
STOP
BYTE CONTROL
GATE DATA REG TO C REG
DATA REGISTER
0 1 2 3
TO CPU
DATA CHECK
RETRY COUNTER (15)
DATA CK STOP - RESET POWER ON
REREAD FROM BEGINNING OF SECTOR
FROM CPU CLOCK CTRLS
CF CLOCK CTRLS
START CLOCK
STOP CLOCK
TO CPU CLOCK CTRLS
ACTIVE ALL THE TIME EXCEPT FOR STORAGE WORD. THEN DROPPED AT END OF 1ST CYCLE AND INTO 2ND CYCLE. ALLOWS 2ND STORAGE CYCLE
Logic References
23 FD SS XXX
CF Adapter KF
Interface $$010,KF051

CONTROL COMMANDS

Command	Mnemonic	Hex
Compact Data Mode	MODE=DATA	00/10
File Pause	FILEPAUSE	00/11
Byte Check	NOP	02/12
Diagnostic Mode 3	MODE=D3	03/13
M-Register Duplicate Check	STP=M-DUP	04/14
S-Register Duplicate Check	STP=S-DUP	05/15
ALU Check	STP=ALU	06/16
C-Register Parity Check	STP=C-PTY	07/17
Advance Byte Counter by +17	BYTCTR + 17	08/18
Diagnostic Stop	DIAG=STOP	09/19
Force Parity CFDA/CMMD Regs	CMD&ADR-P	0A/1A
Error Check	STP=NO-CK	0B/1B
Diagnostic Mode 1	MODE=D1	0C/1C
Diagnostic Mode 2	MODE=D2	0D/1D
Diagnostic Mode Normal	MODE=NORM	0E/1E
Reset CF Checks	RST-CHKS	0F/1F
File End	FILE-END	40/50
File Wait	FILEWAIT	41/51
Sector End	SEND	42/52
Conditional Sector End	SEND-IFMM	44/54
Set CFDA No Sector End	SET-CFDA	4A/5A
Extra Bit Check	EXTRA-BIT	4C/5C
Shift-Register Parity	SHIFT-PTY	4D/5D
Block Stop Bit	NO-STPBIT	4E/5E
Odd-Even Byte Check	INVRTBIT3	4F/5F

OPERATION COMMANDS

Command	Mnemonic	Hex
CFDR to C-Register	C=R	20
CFDR to C-Register and Execute	C=R,X	30
Disk to C-Register	C=LR	60
Disk to C-Register and Execute	C=LR,X	70
Disk to C-Register and Execute C-Register in Compare Mode	C=LR,mmm	78 to 7F
Execute C-Register with Direct Local Store Addressing, CFDR Data	X,LS	80
Execute C-Register with Direct Local Store Addressing, Disk Data	LR,X,LS	C0

CONSOLE-FILE DISK ADDRESS (CFDA) BYTE

- First byte read in any sector
- Contains sector address (track and sector)
- Address range is 00 to FF (256 sectors)

	CFDA Byte Format							
		Track				Sector		
Bit	0	1	2	3	4	5	6	7
Bit Value	16	8	4	2	1	4	2	1
Hex Value	8	4	2	1	8	4	2	1

COMPARE MODE

When an operation's command is decoded, bit 4 is checked. When bit 4 is 1, the command is performed in compare mode. Compare mode is applicable only to commands 0010, 0011, 0110, 0111 (20, 30, 60, 70).

Execution of the word in the C-register results in setting up the next control word address in the M (N) register even though that address is not used to access the next control word.

M3 bits 3, 4, and 5 are frequently set according to the result of branch testing. Bits 5, 6, and 7 in a command byte specifying compare mode are compared to M3 bits 3, 4, and 5 so that setting of M3 bits 3–5 can be checked. To use comparison checking, the diagnostic programmer must set up the command byte bits 5–7 so that the next control word address is checked. Bits 5–7 of the command byte correspond to M3 bits 3–5 as follows.

Command Byte Bits	M3 Bits
567	345
000	000
001	001
010	010
111	111

If a mismatch occurs in compare mode checking, the diagnostic stop latch sets. The file and CPU operations stop, and the system diagnostic stop check indicator turns on. If the command byte bits 5–7 match M3 bits 3–5, the console file operation continues.

Function	Rate Switch	A/B Switch	C/D Switch	Diag/CF Control	Purpose
Read	Proc	T/S	XX	Read	Begin Reading from Selected Track/Section
Recycle	Proc	T/S	XX	Recycle	Recycle Selected Track/Sector
CE Mode	N/A	N/A	N/A	CE Mode	Continuous Power to File Independent of CPU Operation
Byte Counter Match	CF Byte Count Hdstp	T/S	Byte Count	Read	Hardstop Match on a Byte Count Value in Diagnostics Using CF Load/Execute in a Given Track/Sector
Byte Counter Sync	Proc	T/S	Byte Count	Recycle	Sync on a Given Byte Count in Diagnostics Using CF Load/ Execute Within a Track/Sector

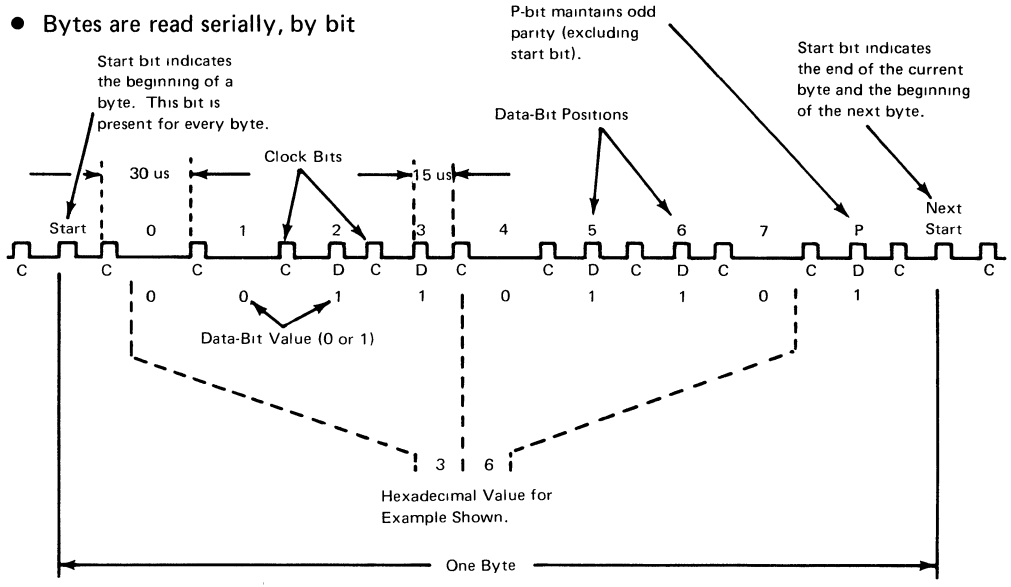
CF ERROR CHECKS

The action that occurs when a CF error is detected depends upon the settings of the diagnostic/console file control and check control switches. Results for each combination of switch settings are shown in the following chart.

	CF Error Conditions and Results				
Switch	Diag CF/Control Switch	Read or Process		Recycle	
	Check Control Switch	Process	Hard Stop	Process	Hard Stop
Check Condition	Byte Cntr Cmnd Reg Disk Addr Reg Pause	Stop	Stop	Restart	Stop
	CPU Clock Start	Stop	Stop	Restart	Stop
	Data Checks Even-Odd Check Out of Sync/ Missing Bit Extra-Bit Check Shift-Reg Parity Error	16 Retries	Stop (Read) 16 Retries (Process)	16 Retries	Stop
	Diagnostic Stop (See 3145 MDM Diag 1-41)	Stop	Stop	Restart	Stop

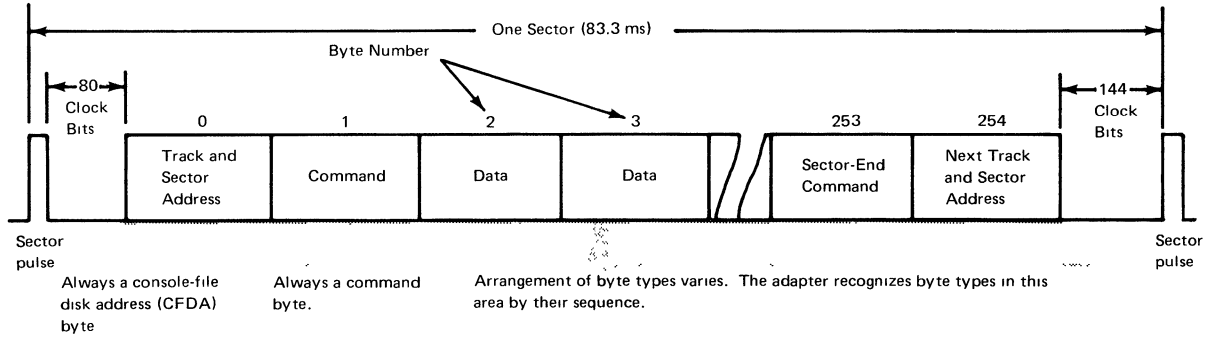
BYTE FORMAT

- Ten-Bit Positions For Each Byte
- Bytes are read serially, by bit



Sector Format

- Maximum of 255 Bytes per Sector



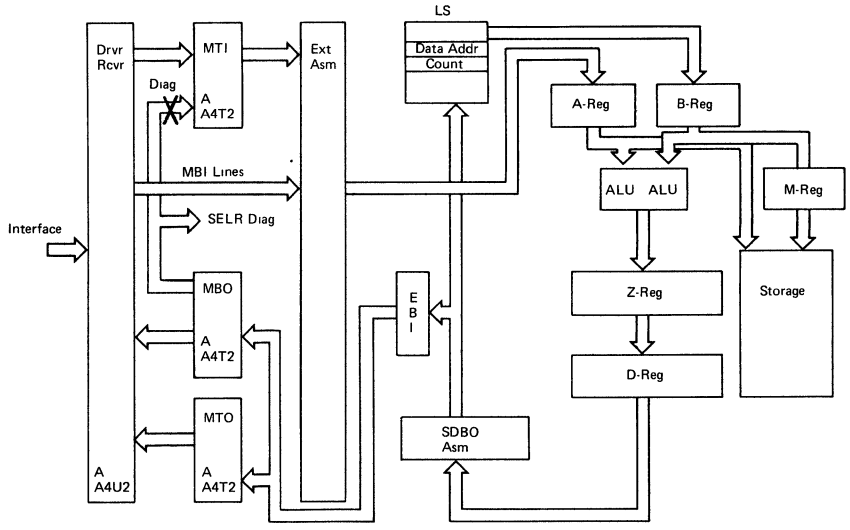
Word MPX	Byte 0 MTO	Byte 1 MTI	Byte 2 MBI	Byte 3 MBO
	0 Operational-out	0 Operational-in	B	B
	1 Select-out	1 Address-in	U	U
	2 Address-out	*2 Status-in signal	S	S
	3 Command-out	*3 Service-in signal		
	4 Service-out	4 Select-in	I	O
	5 Interrupt	5 MPX-request in	N	U
	6 Suppress-out	6 MPX or Cons Req In		T
	7 MPX check	7 Disconnect-in		

Note:

Bits 2 and 3 of MTI are logical functions of the interface 'service-in' and 'status-in' lines.

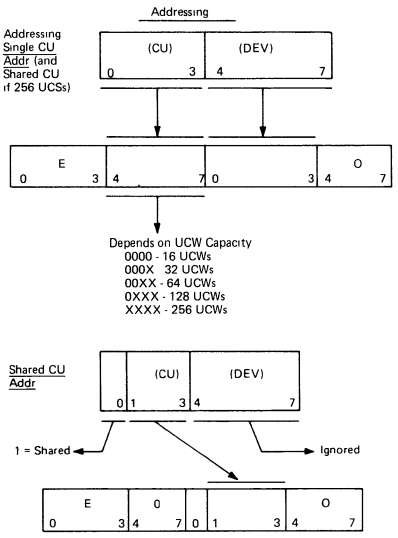
*Bits 2-3

00 = Op-in up
01 = Service-in up
10 = Status-in up
11 = Operational-in down



TERMINATOR PART NUMBERS

	System/360	System/370
Bus —	5440649	2282675
TAG —	5440650	2282676



Format

Word	CS Address	Byte 0	Byte 1	Byte 2	Byte 3
1	EXX0	Flag and Ops	UCW/Chan Stat	Count Hi	Count Lo
2	EXX4	Key	Data Address		
3	EXX8	Key	Next CCW Address		
4	EXXC	Dev Addr	Not Used		

Flags and Ops		UCW Status	Channel Status
0	Data Chaining	Active Bit	PCI
1	Cmd Chaining	IL	IL
2	Sili Bit	Prog Check	Prog Check
3	Skip or Status Next	Prot Check	Prot Check
4	PCI	Status Queued	Chan Data Ck
5	Reserved	Chan Control Ck	Chan Ctrl Ck
6	(1) Output (0) Input	Int Ctrl Check	Int Ctrl Ck
7	(1) Decrem (0) Increm		

Flags and Ops Bits 3 and 6

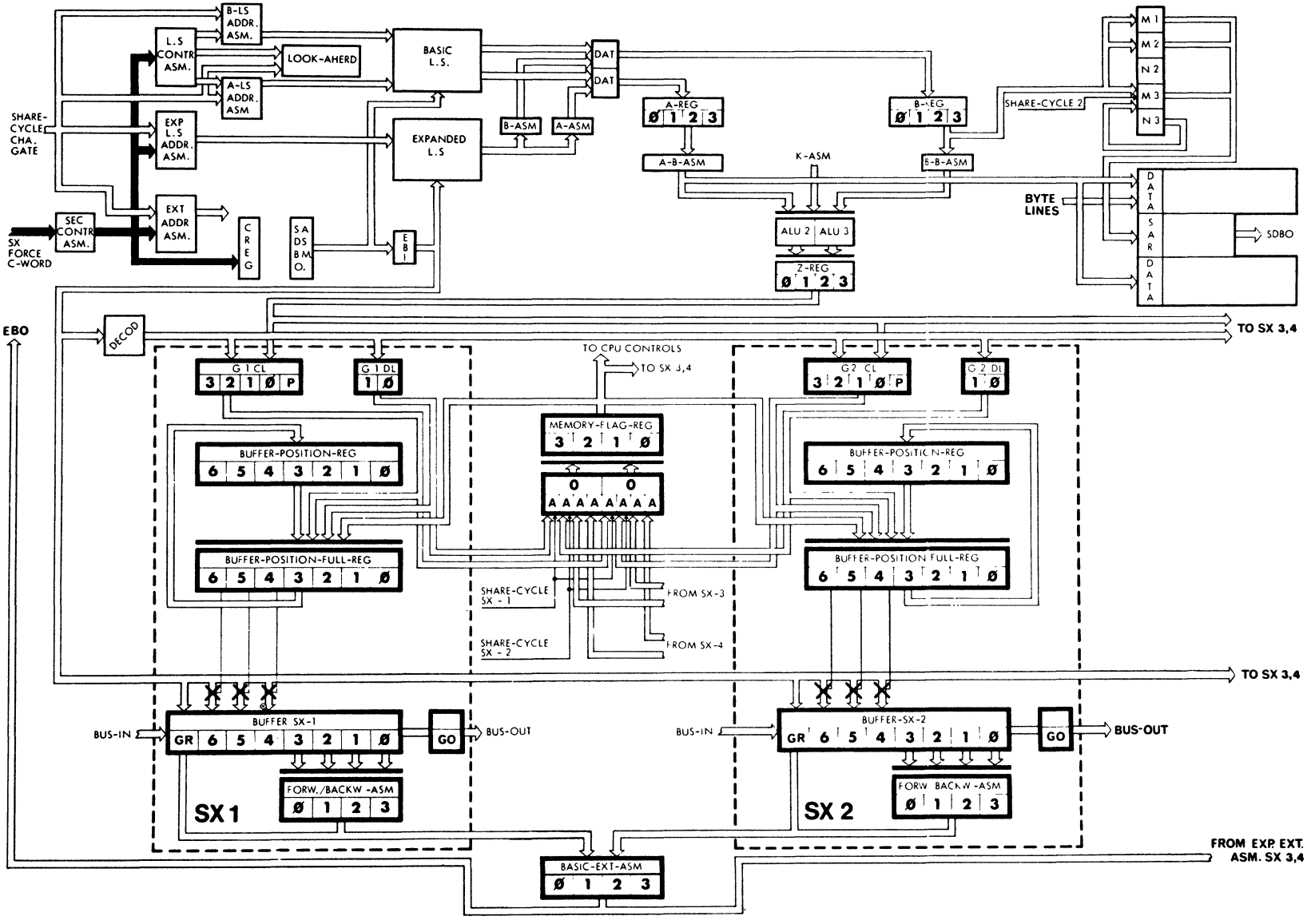
Bit 3	6	Specify
0	0	Input
0	1	Output
1	0	Status Next or Skip
1	1	Stop or Count Zero

UCW Status Bits 4 and 7

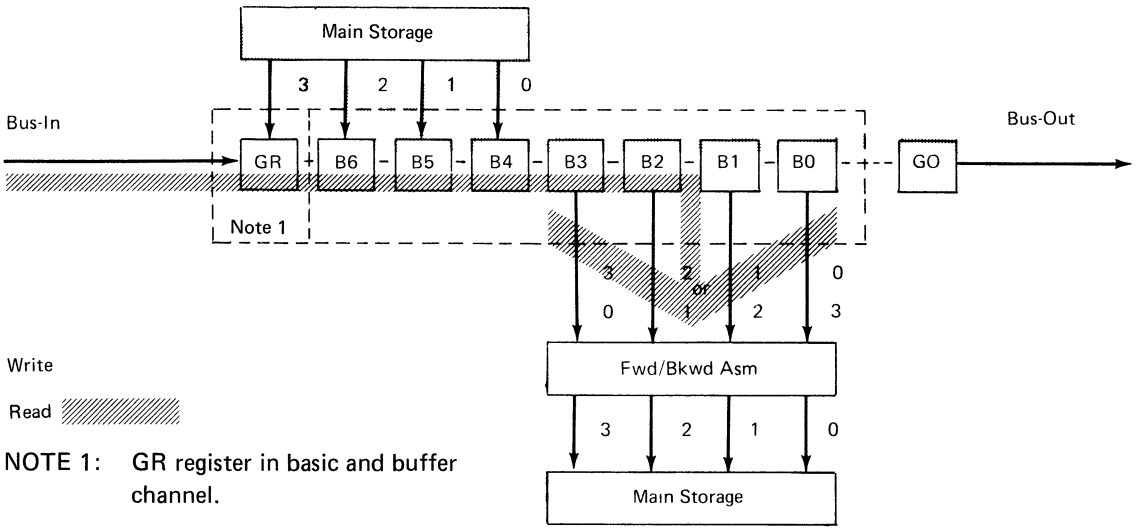
Bit 4	7	Specify
0	0	Handling Data
0	1	Status Next
1	0	Status Stacked
1	1	IB Full

Column ID	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
UNIT/UCW ADDRESSES	00	10	20	30	40	50	60	70	80	90	A0	B0	C0	D0	E0	F0
	01	11	21	31	41	51	61	71	81	91	A1	B1	C1	D1	E1	F1
	02	12	22	32	42	52	62	72	82	92	A2	B2	C2	D2	E2	F2
	03	13	23	33	43	53	63	73	83	93	A3	B3	C3	D3	E3	F3
	04	14	24	34	44	54	64	74	84	94	A4	B4	C4	D4	E4	F4
	05	15	25	35	45	55	65	75	85	95	A5	B5	C5	D5	E5	F5
	06	16	26	36	46	56	66	76	86	96	A6	B6	C6	D6	E6	F6
	07	17	27	37	47	57	67	77	87	97	A7	B7	C7	D7	E7	F7
	08	18	28	38	48	58	68	78	88	98	A8	B8	C8	D8	E8	F8
	09	19	29	39	49	59	69	79	89	99	A9	B9	C9	D9	E9	F9
	0A	1A	2A	3A	4A	5A	6A	7A	8A	9A	AA	BA	CA	DA	EA	FA
	0B	1B	2B	3B	4B	5B	6B	7B	8B	9B	AB	BB	CB	DB	EB	FB
	0C	1C	2C	3C	4C	5C	6C	7C	8C	9C	AC	BC	CC	DC	EC	FC
	0D	1D	2D	3D	4D	5D	6D	7D	8D	9D	AD	BD	CD	DD	ED	FD
	0E	1E	2E	3E	4E	5E	6E	7E	8E	9E	AE	BE	CE	DE	EE	FE
	0F	1F	2F	3F	4F	5F	6F	7F	8F	9F	AF	BF	CF	DF	EF	FF
									These Addresses Share UCW 00	**These Addresses Share UCW 01**	**These Addresses Share UCW 02**	**These Addresses Share UCW 03**	**These Addresses Share UCW 04**	**These Addresses Share UCW 05**	**These Addresses Share UCW 06**	**These Addresses Share UCW 07**

Column ID	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
16 UCW s, any other address up to 7F folds into A	A	A	A	A	A	A	A	A	When there are 128 UCW s or less, the columns of addresses above are reserved for shared UCW addressing The note in **bold type** relates the column of addresses to the correct UCW							
32 UCW s, any other address up to 7F folds into A or B		A	B	A	B	A	B									
64 UCW s, any other address up to 7F folds into A, B, C, or D				A	B	C	D									
128 UCW s, no address folding																
256 UCW s There are 256 unique UCW addresses No folding permitted - No shared unit addresses - All valid unshared																


B-LS ADDR. ASM.
L.S CONTR ASM.
LOOK-AHERD
BASIC L.S.
A-LS ADDR. ASM
SHARE-CYCLE CHA. GATE
EXP L.S ADDR. ASM.
EXPANDED L.S
B-ASM
A-ASM
DAT
DAT
A-REG
B-REG
SHARE-CYCLE 2
M 1
M 2
N 2
M 3
N 3
A-B-ASM
K-ASM
B-B-ASM
BYTE LINES
DATA
SAR
DATA
SDBO
SEC CONTR ASM.
SX FORCE C-WORD
EXT ADDR ASM.
CREG
SADSBMO.
EBI
ALU 2
ALU 3
Z-REG
EBO
DECOD
TO SX 3,4
TO CPU CONTROLS
TO SX 3,4
G 1 CL
G 1 DL
G 2 CL
G 2 DL
MEMORY-FLAG-REG
BUFFER-POSITION-REG
BUFFER-POSITION-FULL-REG
SHARE-CYCLE SX - 1
SHARE-CYCLE SX - 2
FROM SX-3
FROM SX-4
TO SX 3,4
BUS-IN
BUFFER SX-1
GO
BUS-OUT
FORW./BACKW -ASM
SX 1
BUS-IN
BUFFER-SX-2
GO
BUS-OUT
FORW BACKW -ASM
SX 2
BASIC-EXT-ASM
FROM EXP. EXT. ASM. SX 3,4

Selector Channel Buffer Data Flow



NOTE 1: GR register in basic and buffer channel.

C-Register Share Words (With Buffer)

	C0		C1		C2		C3	
	0123	4567	1234	4567	0123	4567	0123	4567
Output	0100	0000	1011	1000	0000	1100	0000	1000
In Fwd	0100	1000	1000	1000	0000	1100	0000	1000
In Bwd	0100	1000	1000	1100	0000	1100	0000	1000
Skip	0100	1000	1000	0100	0000	1110	0000	1000

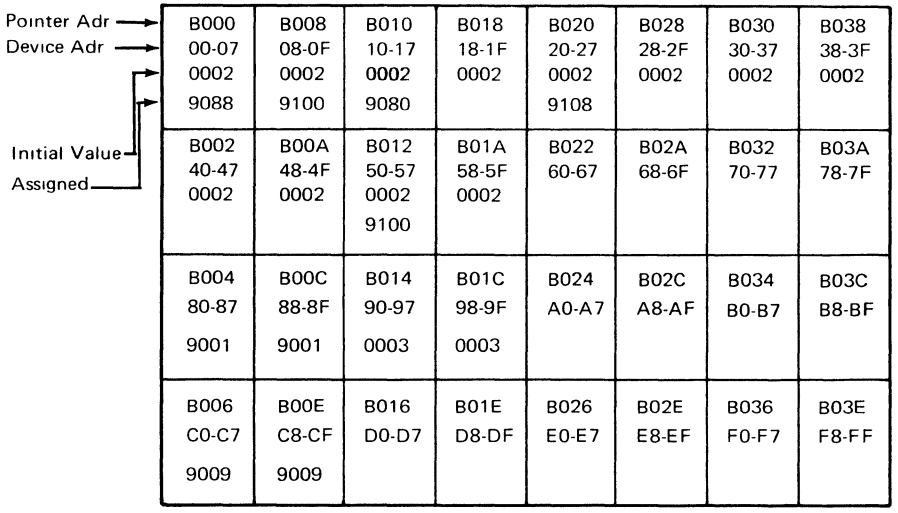
C-Register Share Words (Without Buffer)

	C0		C1		C2		C3	
	0123	4567	0123	4567	0123	4567	0123	4567
Output	0110	0000	1011	1000	0000	1100	0000	1000
In Fwd	0110	1000	1011	1000	0000	1100	0000	1000
In Bwd	0110	1000	1011	1100	0000	1100	0000	1000
Skip	0110	1000	1011	0100	0000	1110	0000	1000

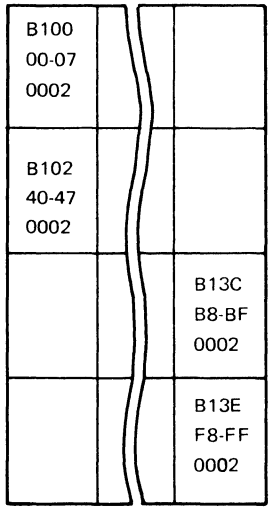
NOTE: These words are hardware forced into the C-register on a share cycle.

STANDARD DEVICE ADDRESSES

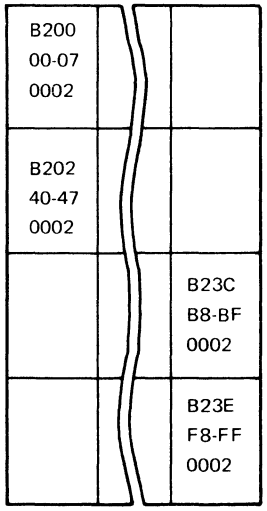
I/O Unit	Address
1052/2150 System Console (1)	01F
1052/2150 System Console (2)	21F
1052/2150 System Console (3)	009
1052/2150 System Console (4)	209
1052/2150 System Console (5)	309
2301 Drum Storage (1)	1CD
2301 Drum Storage (2)	2CD
2303 Drum Storage (1)	197
2303 Drum Storage (2)	297
2305 FHSF Model 1	1F0
2305 FHSF Model 1	2F0
2305 FHSF Model 2	1D0
Model 2	2D0
2311 Disk Storage Drive (1)	190
2311 Disk Storage Drive (2)	191
2311 Disk Storage Drive (3)	192
2311 Disk Storage Drive (4)	193
2311 Disk Storage Drive (5)	290
2311 Disk Storage Drive (6)	291
2311 Disk Storage Drive (7)	292
2311 Disk Storage Drive (8)	293
2314/2319 Direct Access Stg (1)	130
2314/2319 Direct Access Stg (2)	131
2314/2319 Direct Access Stg (3)	132
2314/2319 Direct Access Stg (4)	133
2314/2319 Direct Access Stg (1)	230
2314/2319 Direct Access Stg (2)	231
2314/2319 Direct Access Stg (3)	232
2314/2319 Direct Access Stg (4)	233
2400 Tape (1)	180
2400 Tape (2)	181
2400 Tape (3)	182
2400 Tape (4)	183
2400 Tape (5)	184
2400 Tape (6)	280
2400 Tape (7)	281
2400 Tape (8)	282
2400 Tape (9)	283
2400 Tape (10)	284
2540 Card Read Punch (Reader) (1)	00C
2540 Card Read Punch (Punch) (1)	00D
2540 Card Read Punch (Reader) (2)	20C
2540 Card Read Punch (Punch) (2)	20D
1442-N1 Card Read Punch (1)	00A
1442-N1 Card Read Punch (2)	20A
1403 Printer (1)	00E
1403 Printer (2)	20E
1443 Printer (1)	00B
1443 Printer (2)	20B
3211 Printer (1)	00C
3211 Printer (2)	20C
3330 Disk Storage (1)	150
3330 Disk Storage (1)	250
3330 Disk Storage (2)	151
3330 Disk Storage (2)	251
3330 Disk Storage (3)	152
3330 Disk Storage (3)	252
3330 Disk Storage (4)	153
3330 Disk Storage (4)	253
3505 Card Reader 1	00D
3525 Card Punch 1	00D
3505 Card Reader 2	20C
3525 Card Punch 2	20D



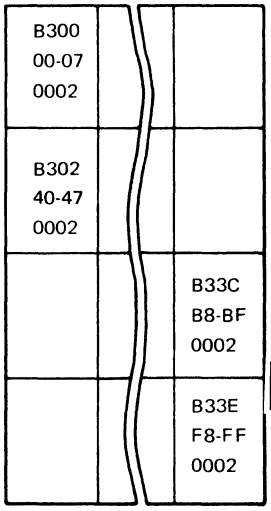
UCW Pointer Table Channel 1



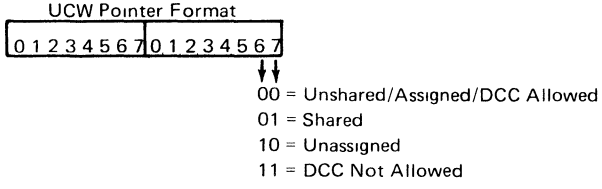
Channel 2



Channel 3

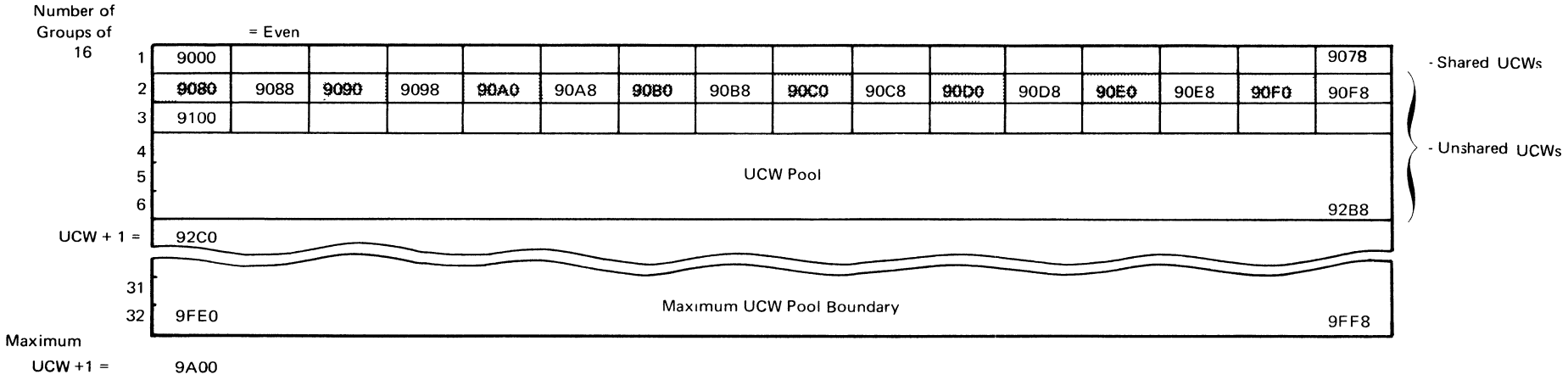


Channel 4



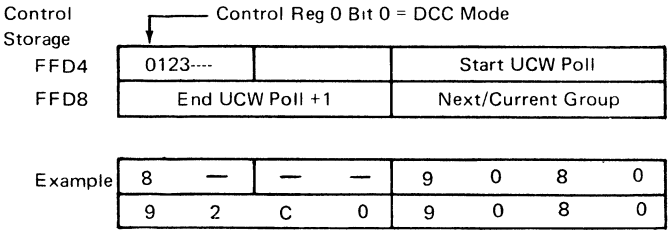
Note: See the appendix section of the FETM manual for details of the Block Multiplex Plug card.

UCW POOL

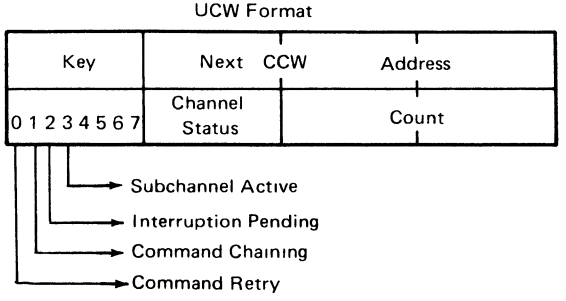


4

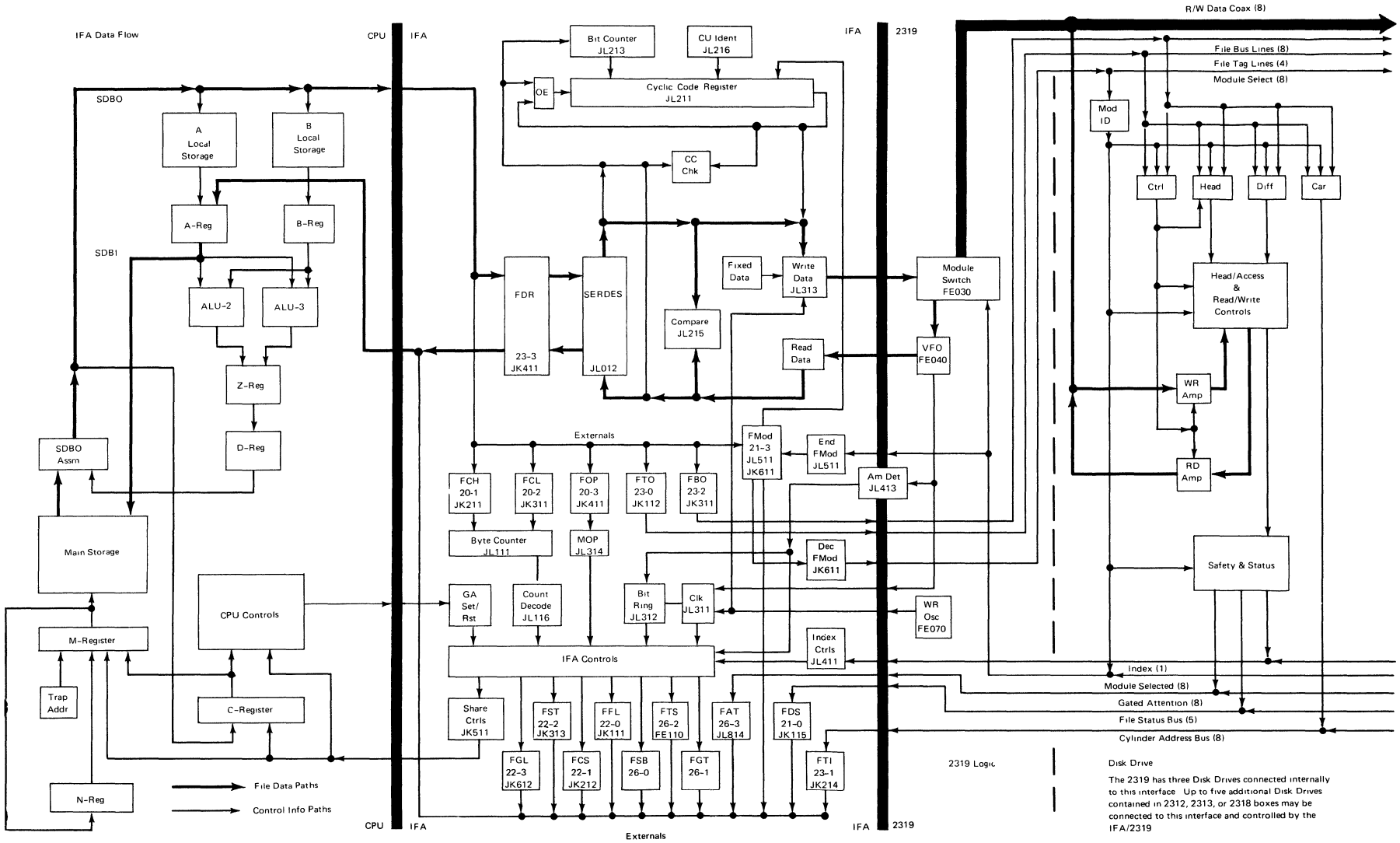
UCW ASSIGNMENT REGISTERS



UCW FORMAT



IFA DATA FLOW



5

IFA IN-LINE TESTS

Select	Test
0	Read Single Track
1	Restore Seek
2	Write Single Track
3	Disk Speed
4	Read Full Cylinder
5	Restore Seek
6	Write Full Cylinder
7	Cylinder Address Register
8	Chaining Test
9	Forward-Backward Seek
A	Write Single Track
B	Sequential Seek
C	Chaining Test
D	Backward-Forward Seek
E	Write Full Cylinder
F	Unsafe Condition

The specified test is performed once by the diagnostic controls and then a 200-millisecond time-out is taken to allow the customer's program to regain control. The test is repeated at the end of the time-out if the IFA control unit is not busy. The diagnostic operation normally stops with errors indicated on the CE panel. The error indications can be disabled to allow scoping or other observation of the operating conditions.

WARNING

*In-line diagnostics should not be running when customer performs an IPL.

*In-line diagnostics affect customer's throughput. Record test results and analyze offline. Use FD test box whenever possible.

SPECIAL CONDITION INDICATIONS

HEX	INDICATION
01	No Record Found.
02	Return to Head 00 Failed.
02	Failed to detect index at maximum interval (Test 3)
04	Return to Cylinder 000 Failed.
04	Index pulses occurring to close together. (Test 3)
08	Seek 2nd Pass Failed (Dif not = Sw)
08	Index pulses occurring too far apart. (Test 3)
08	CAR failed to restore to original address. (Test 7)
09	CAR failed to reset to 00.
0A	CAR failed to load to FF.
0B	CAR failed to load to value in CE head/cylinder switches.
0C	Seek Fwd/Bkwd Diff of Sw Failed.
0C	Index trap occurred before head conditioning. (Test 3)
0E	Write Test not Allowed (Def/Alt)
0F	Head Selected not Equal to Switches.
10	No module selected.
11	Machine check during inline.
13	An R0 key field was detached.
FF	Gated attention failed to reset.

UNSAFE TEST INDICATIONS

HEX	INDICATION
06	Unsafe indicator set.
07	EOC indicator set.
0A	Both unsafe and EOC set.
A1	Failed to set EOC with advance to head-20
B-	Force multiple head select (Y4 + Y8).
C-	Force read and erase gates.
D-	Force write gate without erase gate.
E-	Force erase gate and seek start.
-2	Failed to reset Unsafe at index (with head-tag and bus-out 1).
-4	Failed to set Unsafe indicator.
-8	Unsafe set at entry of force test.

GENERAL STATUS INDICATIONS

HEX	INDICATION
21	Drive Read/Write Failure.
to	Bit-0 = 0
3F	Bit-1 = 0
	Bit-2 = 1
	Bit-3 Write Current Failure.
	Bit-4 Data Check Occurred.
	Bit-5 Missing Address Mark.
	Bit-6 High Compare Detected.
	Bit-7 Low Compare Detected.
41	Control Unit failure.
to	Bit-0 = 0
7F	Bit-1 = 1
	Bit-2 Channel Data or Control Check.
	Bit-3 Data or Command Overrun.
	Bit-4 Cyclic Code Hardware Error.
	Bit-5 Write Track Overrun.
	Bit-6 Bus-Out Parity Error.
	Bit-7 Serializer/Deserializer Error.
81	Disk status displayed.
to	Bit-0 = 1
FF	Bit-1 Off Line
	Bit-2 Unsafe.
	Bit-3 Busy.
	Bit-4 Pack change.
	Bit-5 EOC detected.
	Bit-6 Multi-module selected.
	Bit-7 Seek incomplete.

RECOMMENDED TEST SEQUENCE

No.	Test Operation
7	Cylinder Address Register Test
3	Disk Speed Test
0	Read Single Track Test
4	Read Full Cylinder Test
F	Unsafe Condition Test
2,A	Write Single Track Test
6,E	Write Full Cylinder Test
1,5	Restore Seek Test

IFA SENSE INFORMATION

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
0	Command Reject	Data Check in Count Field	Unsafe	Busy		
1	Intervention Required	Track Overrun		Online		
2	Bus-Out Parity	End of Cylinder	Serdes Check	Unsafe	Disk	Overflow
3	Equipment Check	Invalid Sequence	Selected Status	Write Current Sense	Drive	Incomplete
4	Data Check	No Record Found	Cyclic Code Check	Pack Change	Physical	Information
5	Overrun	File Protected	Unselected File Status	End of Cylinder	Identifi-cation	
6	Track Cond Check	Missing Address Marker		Multi-Module Select		
7	Seek Check	Overflow Incomplete		Seek Incom-plete		

Byte 4

Hex Value	Physical Drive
00	A
01	B
02	C
03	D
04	E
05	F
06	G
07	H
0F	Not Defined

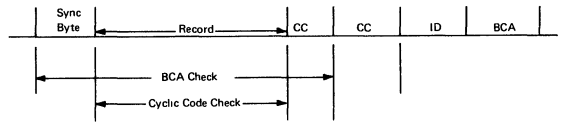
Byte 5

Hex Value	Interrupted Condition
06	Read Command in Progress
05	Write Command in Progress
25	Srch KD Equal – Record Equal to This Point
45	Srch KD High – Record Equal to This Point
65	Srch KD Equal or High – Record Equal to This Point
55	Srch KD (Any Type) Record Low to This Point
	Srch KD Equal – Record Unequal to This Point
75	Srch KD High or High/Equal – Record High to This Point

IFA INFORMATION

Sync Bytes

0D Home Address
0B R0 Count Field
0E RN Count Field
0A All Key Fields
09 All Data Fields



Byte Counter Decode

26 Set Gate Last Request Latch to Stop The Share Sycles for Write and Search OPs
25 Set End Data Field Latch for Read OPs
24 Cyclic Code
23 Cyclic Code
22 Drive Identifier
21 BCA (Bit Count Appendage)
20 Trap (D128) Mini Op End
15 Turn Off Erase Gate
0 Load Byte Counter and New Mini Op from FCH, FCL and FOP
1 Cmmd Overrun Gate (Interface Cntl Check)
0-7 Control Addr Mark Bytes

5

Commands

Command Type	Command Name	Hex Code Single Track	Hex Code Multi-Track
Control	Seek (BB CC HH)	07	–
	Seek Cylinder (CC HH)	0B	–
	Seek Head (HH)	1B	–
	Recalibrate	13	–
	No Operation	03	–
	Set File Mask	1F	–
	Space Count	0F	–
	Restore (2321 only)	17	–
Sense	Test I/O	00	–
	Sense I/O	04	–
Read	Read Data	06	86
	Read Key-Data	0E	8E
	Read-Count-Key-Data	1E	9E
	Read Home Address	1A	9A
	Read R0	16	96
	Read Count	12	92
	Read IPL	02	–
Write	Write Data	05	–
	Write Key-Data	0D	–
	Write-Count-Key-Data	1D	–
	Write Home Address	19	–
	Write R0	15	–
	Write (Special) Count–Key–Data	01	–
	Erase	11	–
Search	Search Equal ID	31	B1
	Search High ID	51	D1
	Search Equal-Hi-ID	71	F1
	Search Equal Key	29	A9
	Search High Key	49	C9
	Search Equal-Hi Key	69	E9
	Search Equal HA	39	B9
	Search Equal Key Data	2D	AD
	Search High Key Data	4D	CD
	Search Hi-Eq Key Data	6D	ED
	Continue Scan Equal	25	A5
	Continue Scan High	45	C5
	Continue Scan Hi Eq	65	E5
	Continue Scan, No Compare	55	D5
	Continue Scan, Set Compare	75,35	F5,B5

Seek Address

Type	Cell Number Byte 0	Cell Number Byte 1	Cylinder Number Byte 2	Cylinder Number Byte 3	Head Number Byte 4	Head Number Byte 5
2314	0	0	0	0-202	0	0-19

File Protection

The significance of the file mask bits is:

B0 B1
- 0 0 Inhibit Write Home Address and Write R0
- 0 1 Inhibit all write commands
- 1 0 Inhibit Write Home Address - Inhibit Write R0 - Inhibit Write Count, Key, and Data
- 1 1 Permit all write commands

B3 B4
- 0 0 Permit all seek and restore commands
- 0 1 Permit Seek CCHH and HH CCWs
- 1 0 Permit Seek HH CCW
- 1 1 Inhibit all seek commands

B2 B5 B6 B7
0 0 0 0

Status Byte

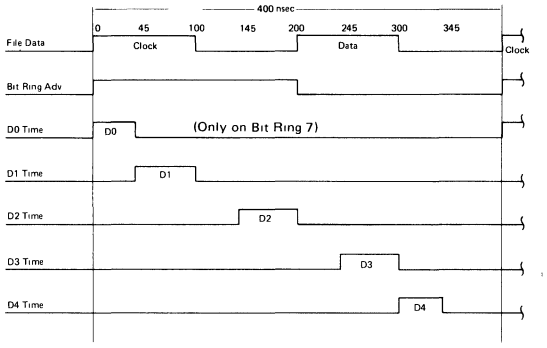
Bit	Name	Note
0	Attention	Not Used
1	Status Modifier	Used with Search and Control Unit Busy.
2	Control Unit End	The control unit has finished an operation.
3	Busy	Indicates addressed access mechanism is moving; or used in conjunction with Status Modifier to indicate Control Unit Busy.
4	Channel End	The control unit has received all the data from the channel needed to do the operation called for and the channel is freed.
5	Device End	Indicates that an access mechanism is free to be used.
6	Unit Check	Indicates that a control unit or programming error or device hardware check has been detected.
7	Unit Exception	End-of-File.

CONTROL WORDS FORCED FOR IFA SHARE CYCLE

	MS	CS
Output	60680C08	60B84008
Input	68B80C08	68B84008
Skip	68B40E08	68B44208

NOTE: These control words are hardware forced into the C-reg.

IFA CLOCK



IFA LOCAL STORAGE ASSIGNMENTS

Word Addr	Word Name	Word Assignments Byte 0	Byte 1	Byte 2	Byte 3
28	FD	Protect Key	Main Storage Data Address		
29	FC*	Flag	CCW Op	Main Storage Count	
2A	FM	Protect Key	CCW Address		
2B	FM	Unit Address	Prev Op Algm	File Mask Algm	Byte Read Area
2C	FA	Cylinder No	Head Number	Control Storage Addres	
2D	FB			Control Storage Count	
2E	FS	Work Area (R)	Work Area (KL)	Work Area (DL)	Work Area (DL)
2F	FL	Mini Op Link Word			

BYTE DETAIL*

FC0	Flag	FC1	CCW Op	FW1	Prev Op Algm	FW2	File Mask Algm
0	Chain Data	0	Multitrack	0	Rd or Sch HA	0	Inh Set FM
1	Com Chain	1	Search Ht	1	Wr or Sch HA	1	Allow Wr HA, R0
2	SLI	2	Search Eq	2	Allow Wr Data	2	Inh Wr Count
3	Skip	3	Count	3	Allow Wr KD	3	Inh Wr K and D
4	PCI	4	Key	4	Allow Wr CKD	4	Inh Seek, Recal
5	Zero	5	Data	5	Search ID	5	Inh Seek Cyl
6	Cyl Overflow	6	Read	6	Search Key	6	Inh Seek Head
7	Zero	7	Write/Search	7	Rd C or Sch ID	7	Index Passed

5

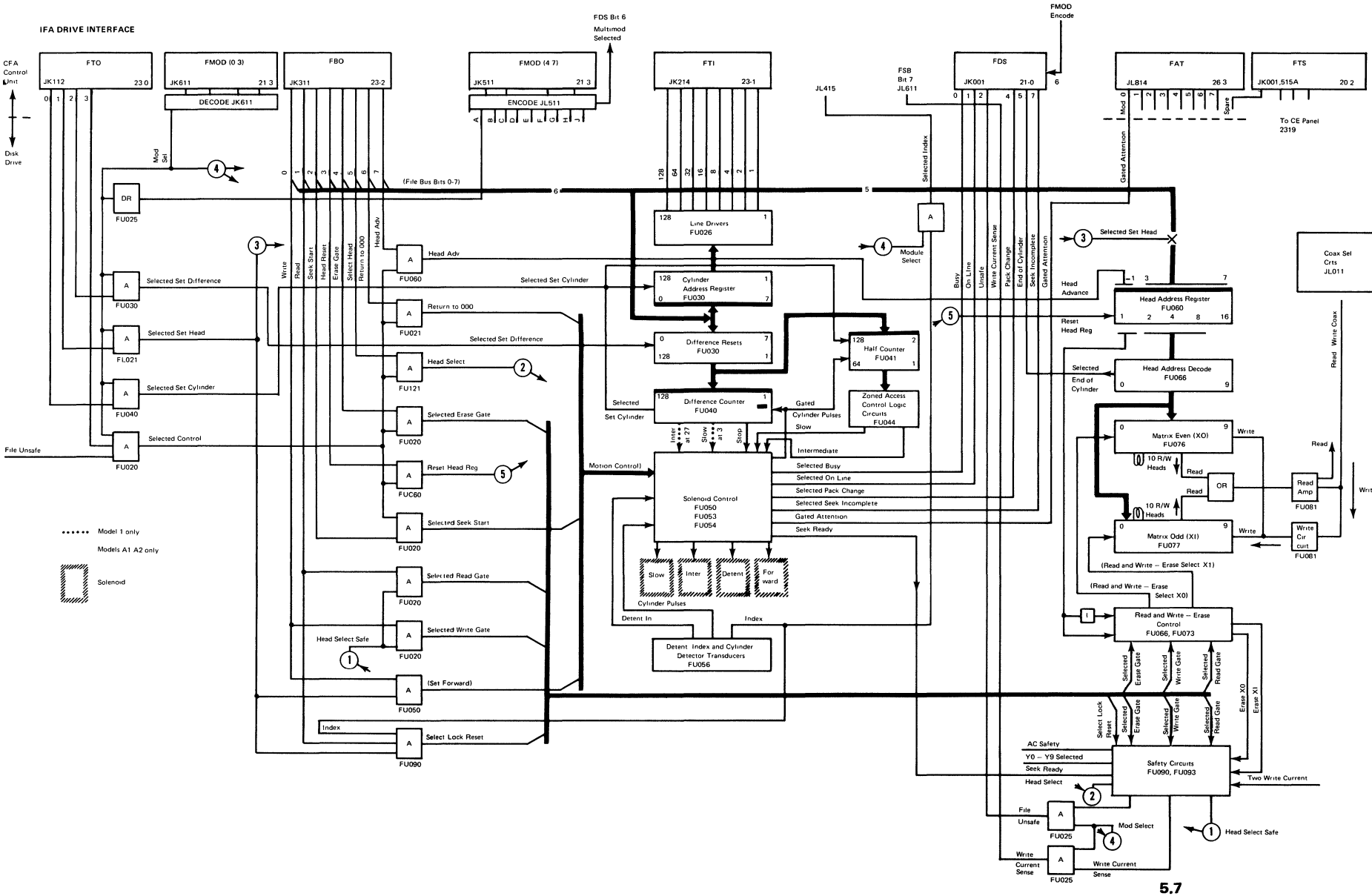
IFA CS AREA

Word Addr	Word Assignments Byte 0	Byte 1	Byte 2	Byte 3
F900	FTAG Register Save Area			
F904	Interrupt Buffer			
F908	Interrupt Buffer			
F90C	Interrupt Buffer			
FFA0			Index Trap Link for FL	
FFA4	I Cycles CAW Backup			
FFA8		FF85 Save Area	CU No. Drive No	Cu No. Max Dr No
FFAC	Sense 0	Sense 1	Sense 2	Sense 5
FFF0	Bit 0=Seek Dir		Head Save Area	Flag
FFF4	Cylinder No	Cylinder No	Head No	Head No
FFF8	Record No	Key Length	Data Length	Data Length
FFFC	Record Overflow Link Word			

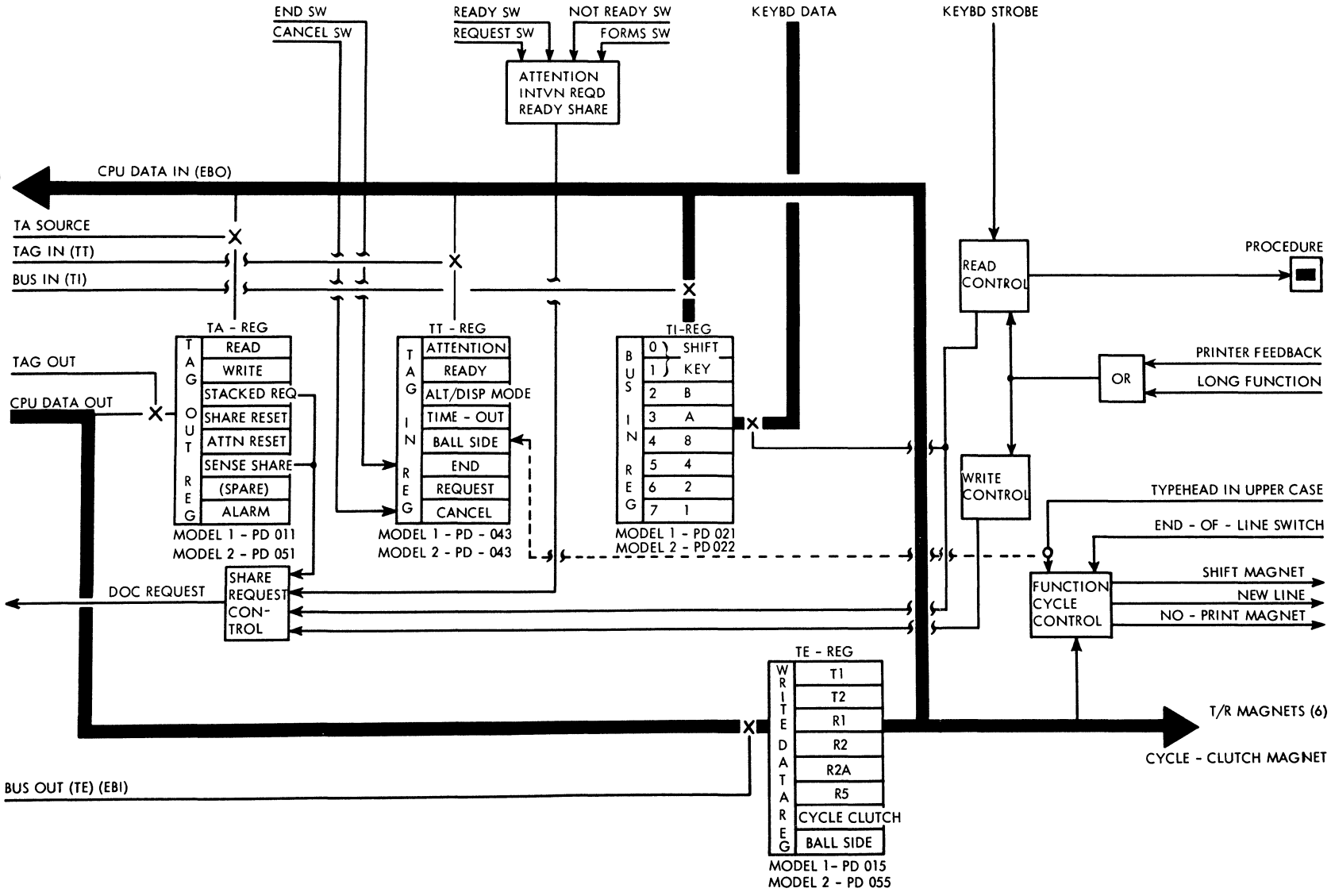
IFA: Module Input Lines

	Bus Line Tag Line	Conversion in Storage Module	Function During: Control Cycle	Set Cyl	Set Head	Set Diff	Set Hail Ctr
FBO	File Bus 0	A 128	Write Gate	Cyl 128	Fwd Latch	Not 128	64
	FBO 1	A 64	Read Gate	Cyl 64	Sel Lock Reset	Not 64	32
	FBO 2	A 32	Seek Start	Cyl 32		Not 32	16
	FBO 3	A 16	Reset Hd Reg	Cyl 16	Hd Addr 16	Not 16	8
	FBO 4	A 8	Erase Gate	Cyl 8	HA 8	Not 8	4
	FBO 5	A 4	Select Hd	Cyl 4	HA 4	Not 4	2
	FBO 6	A 2	Return to 00	Cyl 2	HA 2	Not 2	1
	FBO 7	A 1	Hd Advance	Cyl 1	HA 1	Not 1	—

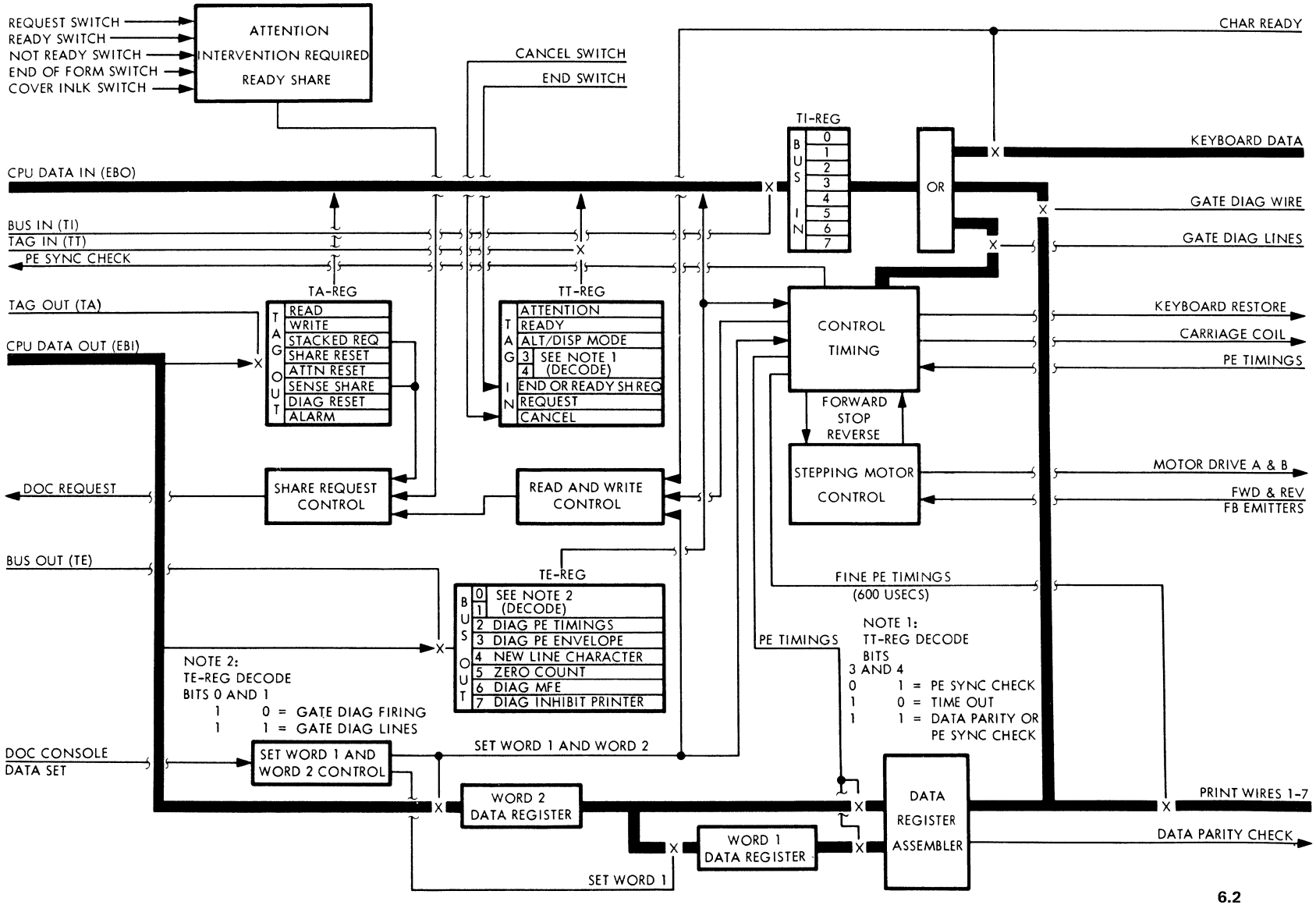
FTO Tag Lines	
Control	Bit 3
Set Cyl	Bit 0
Set Hd	Bit 1
Set Diff	Bit 2


IFA DRIVE INTERFACE
CFA Control Unit
Disk Drive
FTO
JK112
23 0
FMOD (0 3)
JK611
21 3
DECODE JK611
FBO
JK311
23-2
FMOD (4 7)
JK511
21 3
ENCODE JL511
FDS Bit 6
Multimod Selected
FTI
JK214
23-1
JL415
FSB Bit 7 JL611
FDS
JK001
21-0
FMOD Encode
FAT
JLB14
26 3
FTS
JK001,515A
20 2
To CE Panel 2319
Mod Set
(File Bus Bits 0-7)
Selected Index
Gated Attention
DR
FU025
Line Drivers FU026
Module Select
Selected Set Head
Coax Sel Crts JL011
Head Adv
FU060
Selected Set Difference
Selected Set Cylinder
Cylinder Address Register FU030
Head Advance
Head Address Register FU060
Return to 000
FU021
Difference Resets FU030
Half Counter FU041
Reset Head Reg
Selected Set Head
FL021
Head Address Decode FU066
Selected End of Cylinder
Selected Set Cylinder
FU040
Head Select
FU121
Difference Counter FU040
Zoned Access Control Logic Circuits FU044
Gated Cylinder Pulses
Slow
Intermediate
Selected Erase Gate
FU020
File Unsafe
Selected Control
FU020
Reset Head Reg
FUC60
Motion Control
Solenoid Control FU050 FU053 FU054
Selected Busy
Selected On Line
Selected Pack Change
Selected Seek Incomplete
Gated Attention
Seek Ready
Matrix Even (XO) FU076
10 R/W Heads
Read
Write
OR
Read Amp FU081
Matrix Odd (X1) FU077
Write Cr cuit FU081
Read Write Coax
Selected Seek Start
FU020
Slow
Inter
Detent
For ward
Cylinder Pulses
(Read and Write — Erase Select X1)
(Read and Write — Erase Select X0)
Selected Read Gate
FU020
Detent In
Index
Detent Index and Cylinder Detector Transducers FU056
Read and Write — Erase Control FU066, FU073
Head Select Safe
Selected Write Gate
FU020
(Set Forward)
FU050
Index
Select Lock Reset
FU090
Selected Erase Gate
Selected Write Gate
Selected Read Gate
Erase X0
Erase X1
AC Safety
Y0 — Y9 Selected
Seek Ready
Head Select
Safety Circuits FU090, FU093
Two Write Current
File Unsafe
FU025
Mod Select
Head Select Safe
Write Current Sense
FU025
Write Current Sense
Models A1 A2 only
Model 1 only
Solenoid

IFA LATCHES


END SW
CANCEL SW
READY SW
REQUEST SW
NOT READY SW
FORMS SW
ATTENTION
INTVN REQD
READY SHARE
KEYBD DATA
KEYBD STROBE
CPU DATA IN (EBO)
TA SOURCE
TAG IN (TT)
BUS IN (TI)
TA - REG
TAG OUT REG
READ
WRITE
STACKED REQ
SHARE RESET
ATTN RESET
SENSE SHARE
(SPARE)
ALARM
MODEL 1 - PD 011
MODEL 2 - PD 051
TT - REG
TAG IN REG
ATTENTION
READY
ALT/DISP MODE
TIME - OUT
BALL SIDE
END
REQUEST
CANCEL
MODEL 1 - PD - 043
MODEL 2 - PD - 043
TI-REG
BUS IN REG
0 SHIFT
1 KEY
2 B
3 A
4 8
5 4
6 2
7 1
MODEL 1 - PD 021
MODEL 2 - PD 022
TAG OUT
CPU DATA OUT
DOC REQUEST
SHARE REQUEST CON-TROL
READ CONTROL
PROCEDURE
PRINTER FEEDBACK
OR
LONG FUNCTION
WRITE CONTROL
TYPEHEAD IN UPPER CASE
END - OF - LINE SWITCH
FUNCTION CYCLE CONTROL
SHIFT MAGNET
NEW LINE
NO - PRINT MAGNET
TE - REG
WRITE DATA REG
T1
T2
R1
R2
R2A
R5
CYCLE CLUTCH
BALL SIDE
MODEL 1- PD 015
MODEL 2 - PD 055
T/R MAGNETS (6)
CYCLE - CLUTCH MAGNET
BUS OUT (TE) (EBI)

3215 CONTROL AND DATA FLOW



Alter	Display	Address Range	Storage Area
AM	DM	0 Through 7FFFF	Main Storage
AK	DK	0 Through 7FFFF	Storage Keys
AS	DS	0 Through FFFF	Control Storage
AL	DL	00 Through 7F	Local Storage
AC	DC	0 Through F	Control Registers
AG	DG	0 Through F	General Registers
AF	DF	0, 2, 4, 6	Floating Point Regs
AP	DP	----	Current PSW
T	T		Test
AV	DV	0 Through FFFFFF	Virtual Storage
ST		Store Status Prog Status Stored in MS	No Printing

NOTES:

1. Expanded local storage (40 through 7F) can be displayed but not altered.

2. The T mnemonic can be used to correct minor mechanical typewriter problems between customer jobs without the necessity of loading the micro-diagnostic disk. Refer to GKTM routine.

3. When AM/DM is used, it is not necessary to type a six-digit address. Example: To alter memory location 0-type AM0; then carriage-return.

4. If a mistake is made while typing in data, instead of trying to determine which byte to alter, type in AM to the nearest word and use the space bar to get the correct byte. Each pressing of the space bar causes the character in storage to be printed.

PRINTER–KB SENSE INFORMATION

Bit	Meaning
0	Command Reject
1	Intervention Required
2	Bus-Out Check
3	Equipment Check
4-7	Not Used

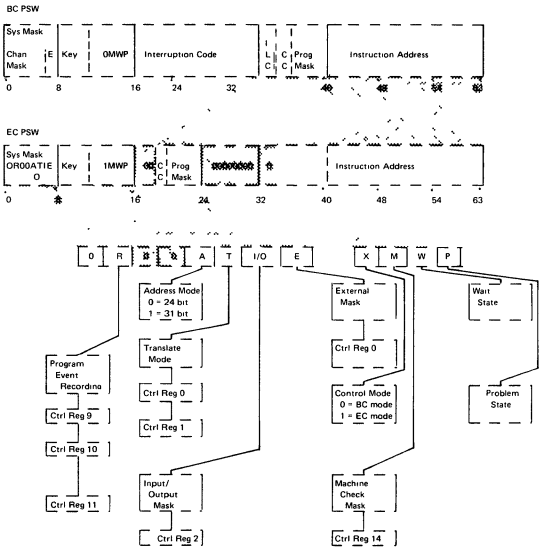
CONSOLE PRINTER VALID ADDRESSES

FIRST PRTER	SECOND PRTER
1F	09
1F	1E
09	08

(370 Coreload
Any other address must be ordered by RPQ.)

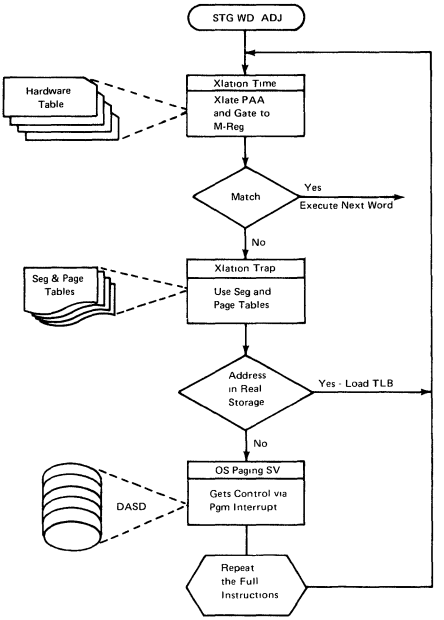
NOTES

PSW FORMAT

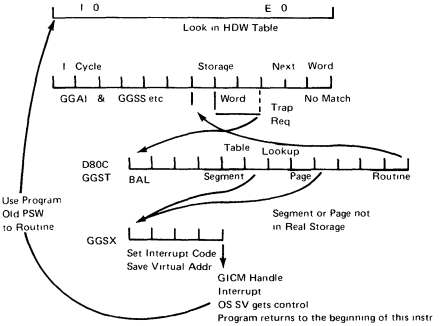

BC PSW
Sys Mask
Chan Mask
E
Key
0MWP
Interruption Code
Prog Mask
Instruction Address
0
8
16
24
32
40
48
EC PSW
Sys Mask
OR00ATIE O
Key
1MWP
Prog Mask
Instruction Address
0
16
24
32
40
48
54
63
0
R
A
T
I/O
E
X
M
W
P
Address Mode 0 = 24 bit 1 = 31 bit
Translate Mode
Ctrl Reg 0
Ctrl Reg 1
Program Event Recording
Ctrl Reg 9
Ctrl Reg 10
Ctrl Reg 11
Input/ Output Mask
Ctrl Reg 2
External Mask
Ctrl Reg 0
Control Mode 0 = BC mode 1 = EC mode
Machine Check Mask
Ctrl Reg 14
Wait State
Problem State

7

ADDRESS TRANSLATE PROCESS OVERVIEW

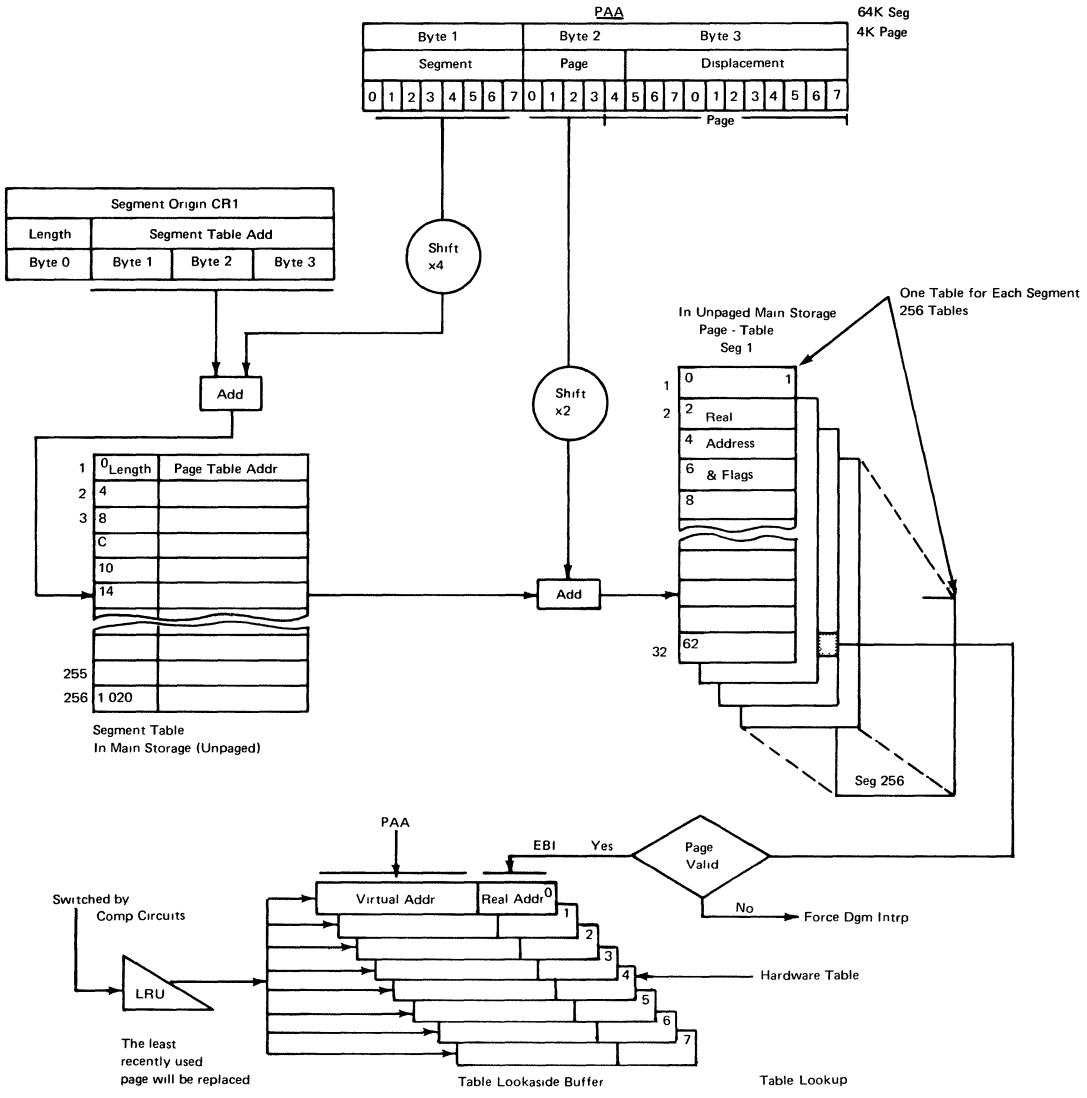


7



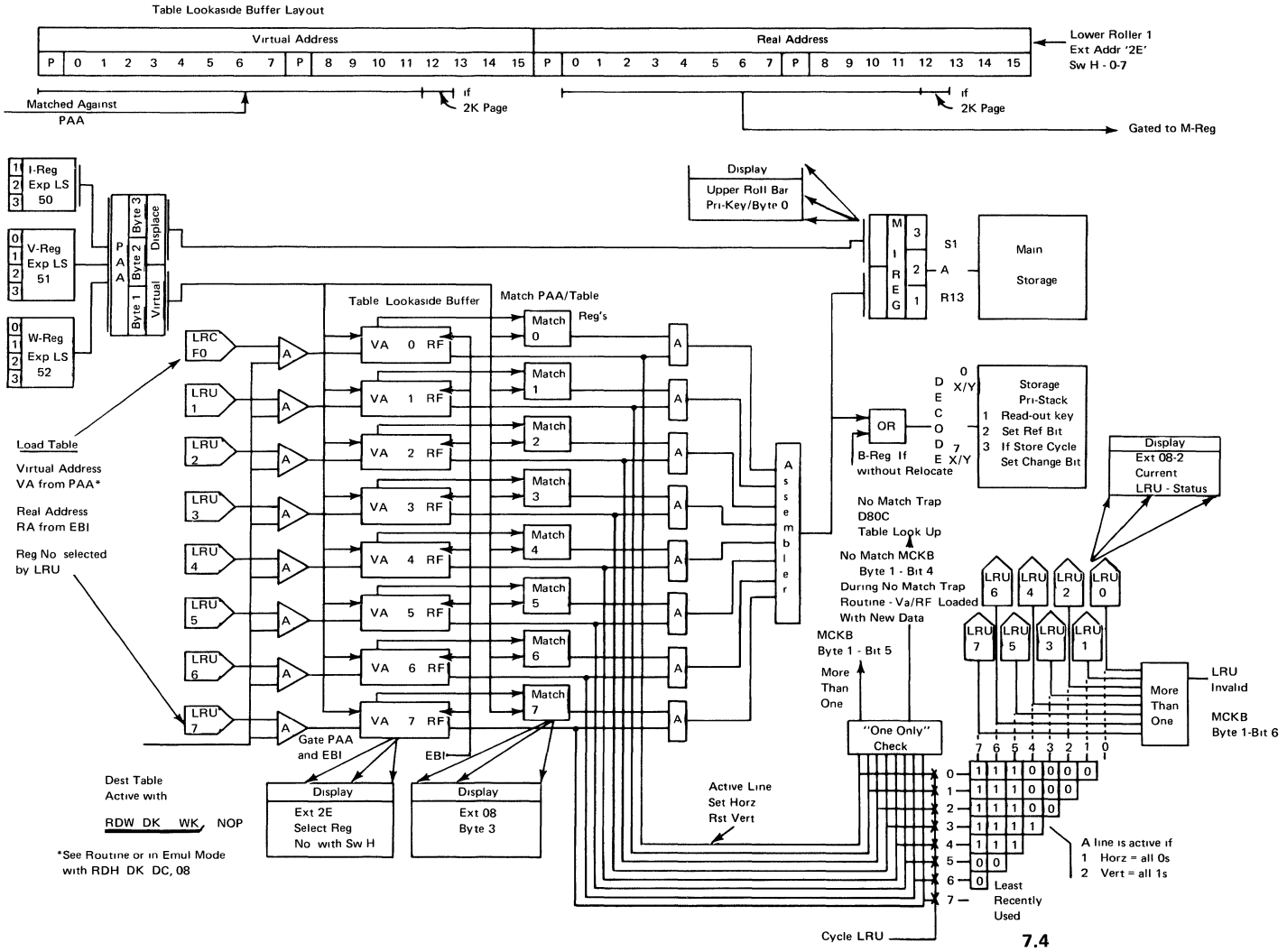
* NOTE
Multiple instructions are checked to make sure that every required address in in real Storage This check is made at the beginning of the E 0

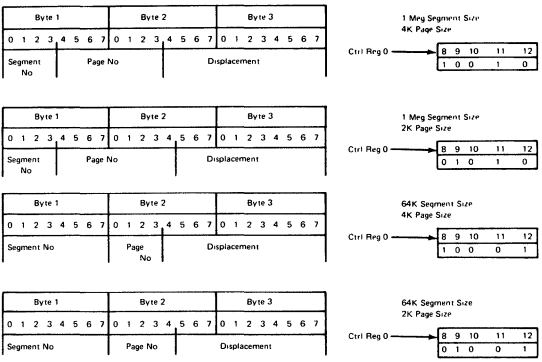
Segment and Page Table Lookup



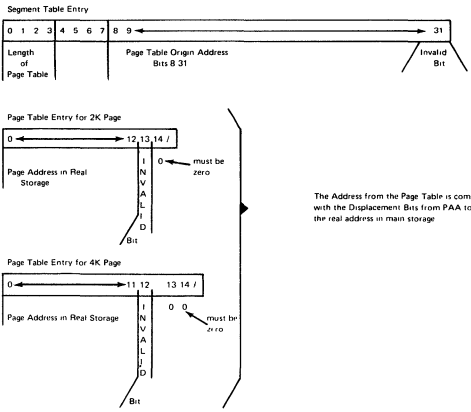
ADDRESS TRANSLATE PROCESS

Table Lookaside Buffer (TLB) Operation



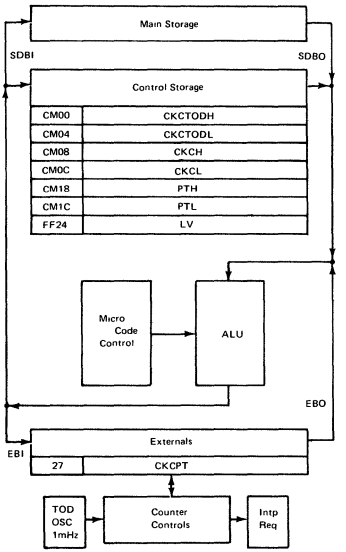


Expanded LS Regs I (L50) V (L51) W (L52) TR (L55)
Page and Segment Size Options



7

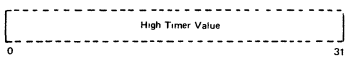
CLOCK COMPARITOR CPU TIMER (CPT)
Optional Feature

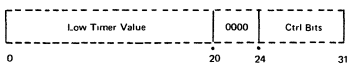


Microcode (GGCT) sets and updates control storage registers The assembled current module (cm) is used for the registers

CKCTODH and CKCTODL contains the set Clock Comparitor value

CKCH and CKCL contains the calculated difference between set clock comparitor value and TOD and is decremented by microcode

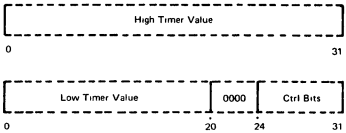




Control Bits

Bit 0
Bit 1 PT Last Interval
Bit 2 CKC Least
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7

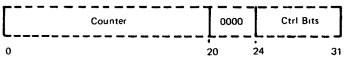
PTH and PTL contains the CPU Timer value that is decremented by the microcode



Control Bits

Bit 0	CKC Run
Bit 1	CKC Last Interval
Bit 2	
Bit 3	
Bit 4	
Bit 5	
Bit 6	
Bit 7	

LV is the last interval value CKCPT (Ext 27)



Decrements at one microsecond rate with borrow causing an update to CS registers
(Not operating in manual or alter display mode)

Control Bits

Bit 0	CKC Submask
Bit 1	PT Submask
Bit 2	Error Bit
Bit 3	Manual Mode
Bit 4	CKC Interrupt
Bit 5	PT Interrupt
Bit 6	Update Latch
Bit 7	Destination to counter was blocked

7

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Condition Code
Branch and Save	BASR	0D	RR	R1, R2	Store the current virtual instruction address in the GPR specified by the R1 field Replace the current PSW address with data from the RZ GPR	Operation	Unchanged
Branch and Save	BAS	4D	Rx	R1, D2 (X2, B2)	Store the current virtual instruction address in the GPR specified by the R1 field Replace the current PSW address with the data specified by the D2 (X2, B2) storage location	Operation	Unchanged
Compare Logical Characters Under Mask	CLM	BD	RS	R1, M3, D2 (B2)	OPR 2 compared to OPR 1 under mask Both operands unchanged	Operation Protection Addressing	0 = Bytes Equal or Mask is Zero 1 = First Oper Low 2 = First Oper High
Compare Logical Long	CLCL	0F	RR	R1, R2	Oper 1 Compared to OPR 2. Regs must be even/odd pairs Even regs contain field sources. Odd regs contain field lengths and padding character Operation terminates on mismatch. Shorter operand extended with padding character.	Operation Protection Addressing Specification	0 = Oper are equal or field lengths are 0 1 = First Oper Low 2 = First Oper High
Insert Characters Under Mask	ICM	BF	RS	R1, M3, D2 (B2)	OPR 1 selected bytes replaced by OPR 2 under mask OPR 2 unchanged.	Operation Protection Addressing	0 = All Inserted Bits 0, or Mask o 1 = First Bit of Inserted Field One 2 = First Bit of Inserted Field Zero
Load Control	LCTL	B7	RS	R1, R3 D2 (B2)	OPR 2 loaded in control regs R1 to R3 in ascending order Starting reg specified by OPR1, ending reg by OPR 3 Wrap-around possible	Operation Priv Oper Protection Addressing Specification	Unchanged
Load Real Address	LRA	B1	Rx	R1, D2 (X2 B2)	Virtual address specified by X2 D2 B2 is translated to a real address and inserted into the GPR specified by R1	Operation Priv Oper Addressing Translation Specification	0 = Translation available 1 = Seg Table Entry Invalid 2 = Page Table Entry Invalid 3 = Seg or Page Table Length Violation

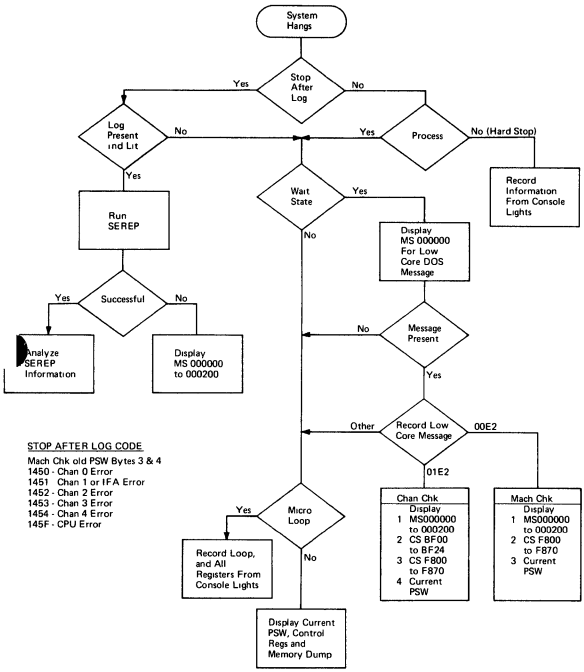
Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Condition Code
Monitor Call	MC	AF	SI	D1, B1 I2	Monitor class specified in bits 12-15 of instruction are matched against Ctrl Reg 8 mask bits. If match occurs, D1, B1 field is stored into Location '9C'	Operation Specification	Unchanged Note. New Program Interrupt = 40
Move Long	MVCL	0E	RR	R1, R2	Opr 2 into Opr 1 if no overlap. Regs must be even/odd pairs. Even regs contain field sources Odd regs contain field lengths and padding character Padding is used if Opr 2 shorter than Opr 1.	Operation Protection Addressing Specification	0 = Opr 1, Opr 2 counts equal 1 = Opr 1 Count Low 2 = Opr 1 Count High 3 = Destructive Overlap, No Movement
Purge TLB (Table Lookaside Buffer)	PTLB	B2 0D	2-Byte Op Code	B1 D1	The addresses in the Table Lookaside Buffers are made invalid	Operation Priv Oper	Unchanged
Reset Reference Bit	RRB	B2 13	2-Byte Op Code	B1 D1	The reference bit associated with the B1 D1 real address is set to zero The condition code is set to reflect the previous status of the reference and change bits.	Operation Priv Oper Addressing	0 = Ref Bit 0, change Bit 0 1 = Ref Bit 0, Change Bit 1 2 = Ref Bit 1, Change Bit 0 3 = Ref Bit 1, Change Bit 1
Set Clock	SCK	B204	SI	D1 (B1)	Eight byte field of OPR 1 replaces value of time of day day clock. Clock secure switch must be depressed	Operation Priv Oper Protection Addressing Specification	0 = Clock Value Set 1 = Clock Value Secure 2 ---------- 3 = Clock Not Operational
Set Clock Comparator	SCKC	B2 06	2-Byte Op Code	B1 D1	The double word at the B1 D1 address is stored into control storage at the current module location XX00, (CKCTOD)	Operation Priv Oper Addressing Specification Protection	Unchanged
Set CPU Timer	SPT	B2 08	2-Byte Op Code SI	B1 D1	The double word at the B1 D1 address is stored into control storage at the current module location XX/8 (PT)	Operation Priv Oper Addressing Specification	Unchanged

8

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Condition Code
Shift and Round Decimal	SRP	F0	SS	D1, (L1, B1) D2 (B2) I3	Opr 1 shifted in direction and by number of digits specified by Opr 2. Opr 2 Bit 26=1= Right Shift Opr 2 Bit 26=0= Left Shift On right shift operation, Opr 1 is rounded by factor (I3)	Operation Protection Addressing Data Decimal OFLO	0 = Result = Zero 1 = Result < Zero 2 = Result > Zero 3 = Overflow
Start I/O Fast Release	SIOF	9C	SI	D1 (B1)	Bit 15 of instr must be a 1 executed as normal SIO when not in BLK-MPX mode. Opr 1 (16-31) specify the chan, subchan and I/O device. Nonchained immed commands on certain channels result in cond code 0 Cond code 0 set by certain channels even though addressed device is not avail or command is invalid	Priv Oper	0 = I/O Op Initiated, Channel Proceeding 1 = CSW Stored 2 = Chan/Subchan Busy 3 = Not Operating
Store Channel ID	STIDC	B203	SI	D1 (B1)	Opr 1 identifies chan for which info (4 bytes) will be stored in loc 168. Info is in format Bit 0-3 Chan Type 0000 Selector 0001 Byte Multiplexer 0010 Block Multiplexer Bits 4-15 Chan Mod No Bits 16-31 Length in bytes of longest I/O extended log-out stored by chan	Operation Priv Oper	0 = Chan ID Stored Correctly 1 = CSW Stored 2 = Chan Activity Prohibited Storing ID 3 = Not Operational
Store Characters Under Mask	STCM	BE	RS	R1, M3, D2 (B2)	Bytes of Opr 1 selected by mask placed contiguously at addr specified by Opr 2	Operation Protection Addressing	Unchanged
Store Clock	STCK	B205	SI	D1 (B1)	Current value of time-of-day clock is stored at the loc spec by Opr 1.	Operation Protection Addressing	0 = Clock in Set State 1 = Clock in Not Set State 2 = Clock in Error State 3 = Clock Not Operational

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Condition Code
Store Control	STCTL	B6	RS	R1, R3, D2 (B2)	Set of control regs starting with Opr 1 through Opr 3 is stored at loc designated by Opr 2 Wraparound possible.	Operation Priv Oper Protection Addressing Specification	Unchanged
Store Clock Comparator	STCKC	B2 07	2 Byte Op Code SI	B1 D1	The CKCTOD register, at the current module location (xx00) is stored at the doubleword specified by the B1 D1 address.	Operation Priv Oper Addressing Specification	Unchanged
Store CPU ID	STIDP	B202	SI	D1 (B1)	Info indentifying CPU (8 bytes) is stored at addr specified by Opr 1 Info is in format Bits 0-7 Zero (Reserved) 8-31=CPU Serial No 32-47=CPU Mod Number 48-63=Length in bytes of longest mach chk logout CPU can store	Operation Priv Oper Protection Addressing	Unchanged
Store CPU Timer	STPT	B2 09	2-Byte Op Code SI	B1 D1	The PT register, at the current module location (XX18) is stored at the doubleword specified by the B1 D1 address.	Operation Priv Oper Addressing Specification	Unchanged
Store, Then AND System Mask	STNSM	AC	SI	(D1 B1) I2	The current systems mask is ANDed with the Mask bits from the instruction (used to reset system mask bits) The old value system mask bits are stored at the D1 B1 address.	Operation Priv Oper Protection	Unchanged
Store, Then OR System Mask	STOSM	AD	SI	(D1 B1) I2	The current systems mask is ORed with the Mask bits from the instruction (used to set system mask bits) The old value system mask bits are stored at the D1 B1 address.	Operation Priv Oper Protection	Unchanged

INFORMATION RETRIEVAL UNDER DOS/360



8

CONTROL REGISTERS

CR	Bit	Function	Sys Rst
0	0	Block Multiplex Mode	0
	24	Timer Mask	1
	25	Interrupt Key Mask	1
	26	External Signal Mask	1
2	0-31	Channel Masks	1
14	0	Hard Stop Mode	1
	1	Synchronous MCEL Mask	1
	2	I/O Extended Logout Mask	0
	4	Recovery Report Mask	0
	6	External Damage Report Mask	1
15	8-31	MC Extended Log Pointer	200

Mask Bit(s)	Interrupt Type and Cause	Machine Check
PSW 13 and R **	System Recovery • CPU error corrected by retry • Intermittent single-bit processor or control-storage error corrected.	Soft
PSW 13 and E **	Interval Timer Damage	Hard *
PSW 13 and E **	Time of Day Clock Damage	Hard *
PSW 13	System Damage • Irreparable hardware malfunction.	Hard
PSW 13	Instruction Processing Damage One of the following occurs during instruction execution: • Unretryable CPU error. • Uncorrectable CPU error. • Multiple-bit processor or control storage error. • Storage-protect key failure.	Hard

* Occurs after current instruction is completed.
** R = Control Reg 14 bit 4
E = Control Reg 14 bit 6

CPU-INDEPENDENT LOGOUT

Locations 232-511 of main storage are reserved for logout. A logout to this area occurs when any type of machine-check interruption is taken.

Dec.	Hex.	
232 236	E8 EC	**Machine-Check Interruption Code**
240 244	F0 F4	
248	F8	00000000 **Failing-Storage Address**
252	FC	**Region Code**
256 260 264 268	100 104 108 10C	**Fixed Logout Area** Note· When CHECK CONTROL is set to STOP AFTER LOG, the I/OEL pointer is ignored and channel logouts are stored, starting at 256.
340 344 348	154 158 15C	
352 356 360 364 368 372 376 380	160 164 168 16C 270 174 178 17C	Floating-Point Register Save Area
384 388 392 396	180 184 188 18C	General-Register Save Area
436 440 444	1B4 1B8 1BC	
448 452 456 460	1C0 1C4 1C8 1CC	Control-Register Save Area
500 504 508	1F4 1F8 1FC	
512 516	200 204	Machine-Dependent Logout (192 bytes)

8

MACHINE CHECK INTERRUPT CODE

Main
Storage
E8-EF

Bit	Abbr	Definition
0	SD	System Damage
1	PD	Instruction Processing Damage
2	SR	System Recovery
3	TD	Timer Damage
4	CD	Time-of-Day Clock Damage
5	ED	*
////	////	//
7	AC	*
8	W	*
////	////	//
14	B	Backup
15	D	Delayed
16	SE	Storage Error Uncorrected
17	SC	Storage Error Corrected
18	KE	Key in Storage Error Uncorrected
////	////	//
20	WP	PSW MWP Bits Valid
21	MS	PSW Masks and Key Valid
22	PM	PSW Program Mask and CC Valid
23	IA	PSW Instruction Address Valid
24	FA	Failing Storage Address Valid
25	RC	Region Code Valid
////	////	//
27	FP	Floating Point Registers Valid
28	GR	General Registers Valid
29	CR	Control Registers Valid
30	LG	Logout Valid
31	ST	Storage Logical Validity
////	////	//
48-63		Machine Check Extended Logout Length

NOTE: Bits 0-8 Subclass
Bits 14-15 Time of Interruption Occurrence
Bits 16-18 Storage Error Type
Bits 20-31 Machine Check Code Validity Bits
* Bits not Used by Model 145

8

MODEL 145 MACHINE DEPENDENT LOG

CS Build Area F804

Model 145 Machine Dependent Log					
Word Name	**Byte 0**	**Byte 1**	**Byte 2**	**Byte 3**	**Original Location**
Retry Counts	Note 1				CS FF84
MCKA	MCKA0	MCKA1	MCKA2	MCKA3	EXT 07
MCKB	MCKB0	MCKB1	MCKB2	MCKB3	EXT 06
ABRTY	ABRTY0	ABRTY1	ABRTY2	ABRTY3	EXT 18
SPTLB	SRTY	PRTY	TRTY	LRTY	EXT 19
HMRTY		HRTY	MRTY2	MRTY3	EXT 1A
CPURTY	BYTDST	RTYFLG	LSDST	EXTDST	EXT 1B
Control	(Control Word in Error)				
SYSREG	SYS0	SYS1	SYS2	H-REG	EXT 05
I-REG	KEY REG	Instruction Counter			EXP LS 50
U-REG	ILC CC Prog Mask	AMWP	Op Code	Immed Byte	EXP LS 53
W-REG	(First Operand Address)				EXP LS 52
V-REG	(Second Operand Address)				EXP LS 51
X-REG	(CPU Working Area)				LS 11
R-REG	(CPU Working Area)				LS 15
Y-REG	(CPU Working Area)				LS 16
Q-REG	(CPU Working Area)				LS 17
IBU-REG					EXP LS 54
TR-REG					EXP LS 55
(Spare)					
SN-Reg					EXP LS 78
PN-REG					EXP LS 79
WK-REG					EXP LS 7A
NP					EXP LS 7B
DM-REG	(Adjustment Factor)				LS 3A
RW-REG	(Address Adjustment Working)				LS 3B
CPU-REG					
PSWCTL-REG			MSKA	MSKB	EXT 10

F870

Note 1 — Stop After Log ID for SEREP

Retry Counts — Interruption Code in old mck PSW=145F=CPU

Byte 0 — Log present and CPU check light

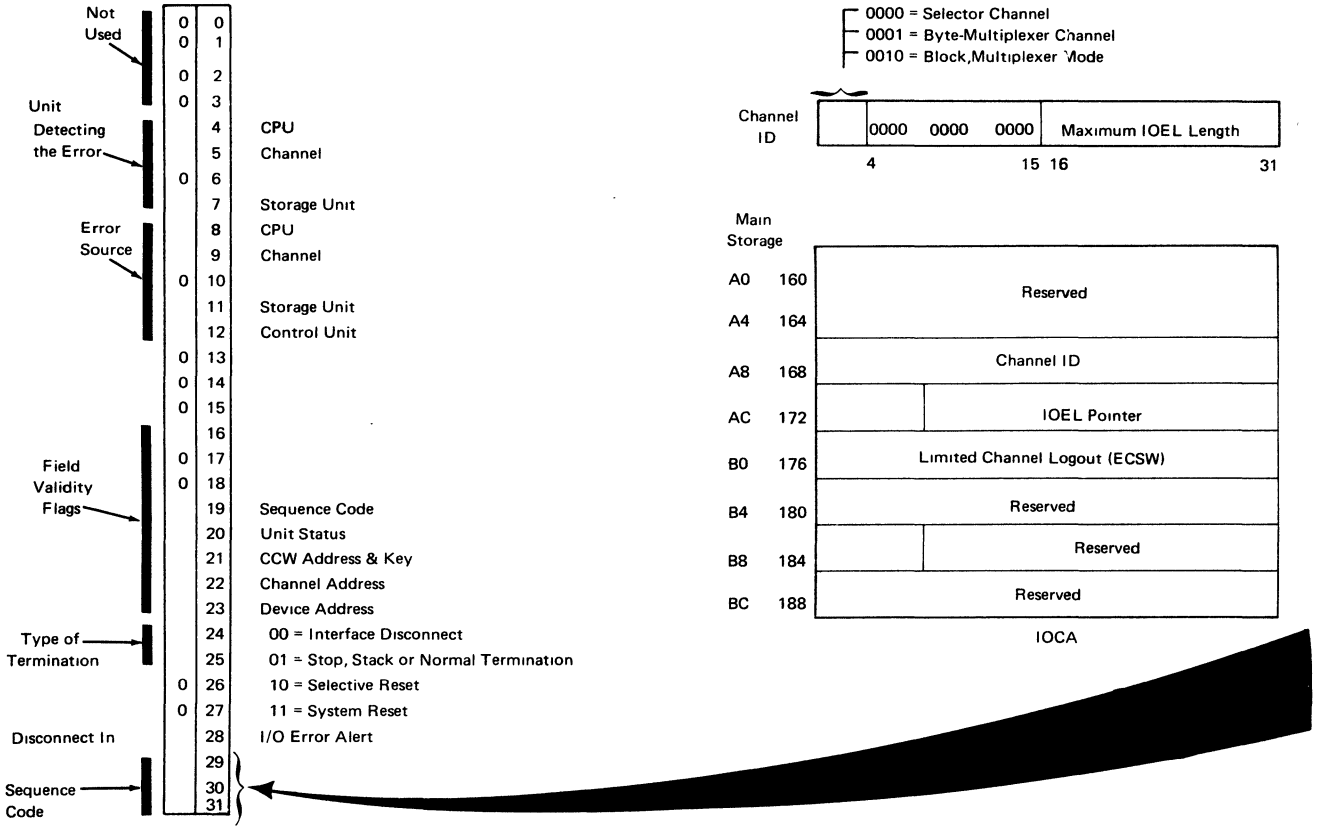
Bits 0-3 — Zero
Bits 4-7 — Retry Attempts for Current Instruction

Bytes 1 and 2 — Zeros

Byte 3 — Number of Instructions Retried

8

NOTES



SEQUENCE CODES

- 000 Error during execution of TIO.
- 001 Error during initial selection. Command-out has been sent.
- 010 Command has been accepted by the device, no data has been transferred.
- 011 At least one data byte has been transferred, or channel idle state.
- 100 The command in the current CCW has either not been sent or not accepted by the device.
- 101 Polling Data transfer--unpredictable.

8

MPX CHANNEL MACHINE DEPENDENT LOG

CS Build Area BF00

BF24 F804 F810

F82C

MPX Channel Machine Dependent Log

Word Name	Byte 0	Byte 1	Byte 2	Byte 3	Original Location	
MA	Note 1	Unit Addr	UCW Address		LS 18	
MBS	Int Buffer ADDR	Status	Seq No.		LS 19	
MC	Key	Next CCW Addr			LS 1B	
MCKA	MCKA0	MCKA1	MCKA2	MCKA3	EXT 07	
MCKB	MCKB0	MCKB1	MCKB2	MCKB3	EXT 06	MPX
MPX	MTO	MTI	MBI	MBO	EXT 0E	
DOC	TI	TA	TT	TE	EXT 0F	
MD			Catalog No.		LS 1C	
MF	Flags, Ops	UCW/CHAN STATUS	Count		LS 1D	
(Spare)						
Retry Counts	Note 2				CS FF84	
ABRTY	ABRTY0	ABRTY1	ABRTY2	ABRTY3	EXT 18	
SPTLB	PRTY	DRTY	TRTY	LRTY	EXT 19	
HMRTY		HRTY	MRTY2	MRTY3	EXT 1A	
CPURTY	BYTDST	RTYFLG	LSDST	EXTDST	EXT 1B	
Control Word	(Control Word in Error)					
SYS REG	SYS0	SYS1	SYS2	H-REG	EXT 05	
I REG	KEY REG	Instruction Counter			EXP LS 50	CPU
U REG	ILC CC Prog Mask	AMWP	Op Code	Immed Byte	EXP LS 53	
(Spare)						
(Spare)						
(Spare)						
(Spare)						
(Spare)						

Note 1 MA-REG
Byte 0
Bit 0 = 1 MPX Log Valid
Bit 0 = 0 MPX Log Invalid

Note 2 Retry Counts
Byte 0
Bits 0-3 Zero
Bits 4-7 Retry Attempts for Current Instruction
Byte 1 and 2 Zeros
Byte 3 Number of Instructions Retried
Stop after I/O Log Start Address

Catalog Numbers (IFCC Only)

M1 = No-Op-in time out
M2 = Status-in time-out
M3 = No-address-in time-out
M4 = Address in bad parity/no address match
M5 = No-status-in time-out
M6 = Op-in time-out
M7 = Bad parity status-in
M8 = Time-out in data loop, inbound tag sequence bad
M9 = Disconnect-in
MA = Bad parity on status
MB = Service-in – expected status-in

a Op in failed to fall
b No SVC or STA signal
c Both inbound tags up

1C = False share request from doc-console
2F = Select-in during chaining

Catalog number byte/bit significance

M* Primary number

0	1	2	3	4	5	6	7

1 = Share trap
1 = Chaining

M = 0 = Initial selection or burst mode

SELECTOR CHANNEL/BLOCK MULTIPLEX CHANNEL DEPENDENT LOG

CS Build Area BF00

BF24 F804 F810

F82C

Selector Channel /Block Multiplex Channel Dependent Log

Word Name	Byte 0	Byte 1	Byte 2	Byte 3	Original Location	
GBS	Log Length Note 1	GBF	GCT	GBD	EXT 31 (SX2)	
GSTAT	GF	GE	GS	GL	EXT 32 (SX2)	
GTAG	GTO	GTI	GO	GR	EXT 33 (SX2)	
MCKA	MCKA0	MCKA1	MCKA2	MCKA3	EXT 07	
MCKB	MCKB0	MCKB1	MCKB2	MCKB3	EXT 06	
GDRL						SX
GD	CHANNEL WORKING REGISTERS				LS20 (SX2)	
GC	CHANNEL WORKING REGISTERS				LS21 (SX2)	
GM	CHANNEL WORKING REGISTERS				LS22 (SX2)	
GW			Catalog No.		LS23 (SX2)	
Retry Counts	Note 2				CS FF84	
ABRTY	ABRTY0	ABRTY1	ABRTY2	ABRTY3	EXT 18	
SPTLB	SRTY	PRTY	TRTY	LRTY	EXT 19	
HMRTY		HRTY	MRTY2	MRTY3	EXT 1A	CPU
CPURTY	BYTDST	RTYFLG	LSDST	EXTDST	EXT 1B	
Control Word	(Control Word in Error)					
SYS REG	SYS 0	SYS 1	SYS 2	H-REG	EXT 05	
I REG	KEY REG	Instruction Counter			EXP LS 50	
U REG	ILC CC Prog Mask	AMWP	Op-Code	Immed Byte	EXP LS 53	
(Spare)						
(Spare)						
(Spare)						
(Spare)						
(Spare)						

Note 1 Only when log is in ms
GBS
Byte 0 = 28 Only SX Log Valid
Byte 0 = 4C SX and CPU Log Valid

Note 2
Retry Counts
Byte 0
Bits 0-3 Zero
Bits 4-7 Retry Attempts for Current Instruction
Bytes 1 and 2 Zeros
Byte 3 Number of Instructions Retried

Catalog Numbers

00 – Indeterminate
01 – Automatic Selection Failed
02 – Halt Stop Will Not Set
03 – Microcode Select Failed on Halt
04 – Interface Disconnect Failed
05 – Selective Reset Failed
06 – Address Check on Channel-Initiated Selection
07 – Short Busy on Chaining
08 – Poll Control will not set (soft)
09 – Address Parity Error on Ctrl Unit Initial Selection
0A – Disconnect-In Received
0B – Hard Set of Poll Control Failed
0C – Unused
0D – Unsuccessful Microprogram Retry
0E – Select-In on Chaining
0F – Status-In Parity Error

IFA EXTENDED LOGOUT

IFA Extended Logout

Word Name	Byte 0	Byte 1	Byte 2	Byte 3	Original Location	
FBAK	Log Length Note 1	FCH	FCL	FOP	EXT 20	
FSTAT	FFL	FCS	FST	FGL	EXT 22	
FTAG	FTO	FTI	FBO	FDR	EXT 23	
MCKA	MCKA0	MCKA1	MCKA2	MCKA3	EXT 07	
MCKB	MCKB0	MCKB1	MCKB2	MCKB3	EXT 06	IFA
FDRL						
FD	Protect	Data Address			LS28	
FC		Count			LS29	
FM	Protect	CCW Address			LS2A	
FW	Unit Address				LS2B	
Retry Counts	Note 2					
ABRTY	ABRTY0	ABRTY1	ABRTY2	ABRTY3	EXT 18	
SPTLB	SRTY	PRTY	TRTY	LRTY	EXT 19	
HMRTY		HRTY	MRTY2	MRTY3	EXT 1A	
CPURTY	BYTDST	RTYFLG	LSDST	EXTDST	EXT 1B	
Control Word	(Control Word In Error)					CPU
SYS REG	SYS0	SYS1	SYS2	H-REG	EXT 05	
I REG	KEY REG	Instruction Counter			EXP LS 50	
U REG	ILC CC Prog Mask	AMWP	Op Code	Immed Byte	EXP LS 53	
(Spare)						
(Spare)						
(Spare)						
(Spare)						
(Spare)						

Note 1
FBAK Byte 0 = 28 Only IFA Log Valid
Byte 0 = 4C IFA and CPU Log Valid

Note 2
Retry Counts
Byte 0
Bits 0-3 Zero
Bits 4-7 Retry Attempts for Current Instruction
Bytes 1 and 2 Zeros
Byte 3 Number of Instructions Retried

Table 1	Control-Storage Mode	Main-Storage Mode	CR 14 Bit 4	PSW Bit 13
Initialized by Pwr On Reset or System Reset with Enable Clear	Threshold	Quiet	0	0
Initialized by System Reset	Threshold	Quiet	No Change	No Change
Initialized by Recovery Management Support (RMS)	No Change	No Change	1	1
Hardware Threshold count exceeded for Control Storage	Set to QUIET by hardware. Operator message presented by RMS and a record logged to SYS1. LOGREC	No Change	No Change	No Change

Table 2 Instruction Format (83--BDDD)	Control-Storage Mode	Main-Storage Mode	CR 14 Bit 4	PSW Bit 13
MODE ECC, RECORD, MAIN B+D=000008	No Change	Record	No Change	No Change
MODE ECC, QUIET, MAIN B+D=00000C	No Change	Quiet	No Change	No Change
MODE ECC, RECORD, CONT B+D=000010	Record	No Change	No Change	No Change
MODE ECC, QUIET, CONT B+D=000018	Quiet	No Change	No Change	No Change
MODE ECC, THRHOLD, CONT B+D=000014	Threshold	No Change	No Change	No Change

Table 1 outlines the modes of taking machine-check interruptions for recovery reports without taking into account the operator mode commands.

Table 2 outlines how the mode commands affect the modes of taking machine-check interruptions for recovery reports Note that in record mode for main and control storage, only intermittent single-bit failures result in a machine-check interruption. The microprogram tests the failing storage location (main or control) to see whether the single-bit failure is solid or intermittent; if the failure is solid, the machine returns to processing instructions and no machine-check interruption is taken.

SWITCHES	LABEL	FUNCTION
CE 1	POWER ON	Performs the same function as the console power-on key (initiates a power-on sequence)
CE 2	CK RESET	This is a momentary position of switch CE2 that resets the power check circuits (picks K12) The power check circuits must be reset after each power malfunction before power can be reapplied to the system
	ERROR OVERRIDE	Bypasses all malfunctions that cause a power-check condition by providing a return path for relay, K12 The power-check conditions bypassed are thermal trip, undervoltage detect, CB trip, and MG check This position of CE2 switch can be used as a trouble shooting aid by enabling power turn-on under a power check condition. By using the error override capability along with CE6 switch (REG TEST position) when a CB trip is apparent, maintenance personnel can monitor the regulator sequence lights and find which regulator(s) are not supplying proper output voltages When the switch is at ERROR OVERRIDE, the CE panel power check light is lit and the console POWER check light is lit to indicate that a CE switch is at a test mode position
	NORMAL	Allows the power check circuits to function in their normal manner. CE2 switch should be maintained at this position during normal running operations
CE 3	BLOWER OFF	Enables turning off the blowers prematurely after a power-down sequence has been started (The blowers normally operate for five minutes after powering-down the system)
	MG HOLD	Keeps the MG set running after the system has been powered down (Bypasses the system power-off switch control over the MG set)
	MG PWR OFF CONTROLLED	Allows the MG to be turned off with the system when the power-off switch is activated
CE 4	NORMAL	Allows the power on switches to control system power in the regular manner CE4 switch must be at NORMAL in order for the system to operate
	POWER OFF	Performs the same function as the console power0off key (intitiates a power-off sequence) Disables the operation of both the console power on and CE panel power on switches Anytime the CE 4 switch is at POWER OFF, the console power check light is lit This switch can be used to prevent power from being applied to the system while it is being serviced
CE 5	I/O HOLD	Allows the 24V dc control to the I/O units to be maintained after the system is powered-down Anytime CE5 switch is at I/O HOLD, the CE panel power check light is lit and the console power light is turned on.
	NORMAL	Allows the I/O devices turn-on procedure to function under control of the system power-on operation CE5 switch should be kept at NORMAL for all regular operations
	I/O OFF	Inhibits the turn-on of I/O devices over the channel. Anytime CE5 is at I/O OFF, the power-on complete light does not light If CE5 is switched to I/O OFF after power-on is complete, the channel I/Os will drop and the power-on complete light will turn off To bring the I/Os up again, press POWER OFF, then POWER ON
CE 6	LAMP TEST	Causes all CE panel lights to glow The CE6 switch can be operated to LAMP TEST at any time without affecting system operation
	REG TEST	Provides a means for checking all regulators outputs by means of the regulator sequencing lights If a CB power check is indicated, one can use the CE2 switch in the ERROR OVERRIDE position along with REG TEST and detect the regulator(s) that are not providing the indicated output (Associated regulator indicator is off)
	NORMAL	Provides no function CE6 switch should be kept at NORMAL during all regular system operations

POWER SUPPLIES

Regulator Turn-On Sequence

Stage I:

All IFA Regs	206*	105
111	207*	107
112	208*	101
110	102	109
205*	104	

Stage II:

All IFA Regs	206*	201*	Parallel Bring-Up
406	207*	202*	
407	208*	401	
405	403	402	
205*	404		

* Main Storage Frame

	Stage I Logic Page	Stage II Logic Page
Trouble Shooting Flowchart	YD011	YA009
Power-On Flowchart	YE011	YB010
Power-Off Flowchart	YE015	YB014
Power-On Sequence and Timing Chart	YE070	YB070
Second Level Sequencing	YE072	YB072
Regulator Sequence Chart and Feature Tie-Down Chart	YD001	YA001
AC Voltage Changeover Chart Form 208-230	YE040	YB040
Second Level Power Check Circuits	YE073	YB073
Under Voltage Detection	YE074	YB074
AC Power Control	YE110	YB110
50-60-400 Hz Distribution	YE140	YB140
MG Phase Rotation Detection	YE111	YB112
MG Output and Controls	YE170	YB170
MG, Power and Fan Information	Section 11 of Combination Manual	Section 11 of Combination Manual
Voltage Checks Refer to Installation Instructions		
03A-A2 Board Sequence Panel	YD Logics	YA Logics
3145 MSF Logics	YE400 through YE460	
3145 MSF 208V and 400Hz	YE150	YB150
Regulator Card Pot Location	YE058	YB058
Metering	YE155	YB155
EPO	YE200	YB200
Power Component Layout Charts	YE016	YB015
Power Frame - CPU Interface Connector Pin Chart	YE030	YB030
Power Frame - MSF Interface Connector Chart	YE031	YB031
Relay and Contactor Component Location Chart	YE050	YB050
Regulator and MG Component Location and P/Ns	YE051	YB051
CB and CP Location Charts and P/N	YE052	YB052
CE Switches Location and P/N	YE052	YB052
Fuse Location Chart and P/Ns	YE052	YB052
Terminal Block Location Chart	YE053	YB053
Diode Rectifier Location Chart and P/N	YE054	YB054
Resistor Location Chart and P/Ns	YE055	YB055
Capacitor Location Chart and P/Ns	YE056	YB056

RELAY FUNCTION & LOCATION CHART

Relay No.	Function	Location	
		Stage I	Stage II
		Refer to Logic Page YE050	Refer to Logic Page YB050
K1	MG Phase Rotation		
K4	EPO Control		
K5	I/O Group I EPO		
K6	I/O Group II EPO		
K7	I/O Group III EPO		
K8	I/O Group IV EPO		
K9	I/O Group V EPO		
K11	MG Check		
K12	Power Check		
K14	Power On		
K15	MG Start Control		
K16	MG Power Contactor		
K20	Time Delay		
K21	MG Hold		
K22	400 Hz Power Control		
K26	400 Hz Contactor		
K27	AC Contactor		
K28	Heads Extended Control		
K29	60 Hz Citation Power Control		
K30	Blower Control Contactor		
K31	Seq I Detect		
K32	Seq 2 Detect		
K33	24V 2nd Seq Control		
K34	Reg UV Control		
K35	I/O Power Hold		
K38	I/O Group I Power Control		
K39	I/O Group 2 Power Control		
K40	I/O Group 3 Power Control		
K41	I/O Group 4 Power Control		
K42	I/O Group 5 Power Control		
K44	Stepper Sw I/O Group p		
K45	Stepper Sw I/O Group 2		
K46	Stepper Sw I/O Group 3		
K47	Stepper Sw I/O Group 4		
K48	Stepper Sw I/O Group 5		
K53	Console File AC		
K55	Console File Start		
K57	CPU Metering		
K58	SPF Metering		
K60	MG Overvoltage Reed		
K151	Power Reset		
K154	Console File DC		

INITIAL REGULATOR ADJUSTMENT FOR POWER UP PROCEDURE

Use this procedure when you are not able to power sequence or get memory voltages or when TR401-V2, TR202-V2, TR102-V2 or V4 circuit breakers trip. After initial settings and power sequences up properly, all regulators must be properly adjusted.

Tri-level Regulator

Power Up Procedure

A Tri-level regulator is +1.25, -3.00 and 7 volts (on B-gate CPU stage 1 and 2 for memory).

Go to CE Over-ride Mode

*Trip Bias Circuit Breaker Single Handle

CP104 — Stage I
CP404 — Stage II
CP203 — MSF

Pull Start Wires off of +1.25, -3. Regs 103 E11 Stage I CPU
201 E11 MSF
404 E 9 Stage II CPU

+7V. Regs 106 E12 Stage I CPU
402 E12 Stage II CPU
202 E12 MSF

Set all 2V Regs to 2.171V. (*Note:* If not adjusted to 2.171, other supplies will have to supply more current and perhaps will trip breakers.)

B-Gate and MSF	A2K2B04	=	2.171V
B-Gate and MSF	B2K2B04	=	2.171V
B-Gate and MSF	C2K2B04	=	2.171V
MSF Only	C3K2B04	=	2.171V

*Now put Bias Breaker that was previously tripped to the on position. Leave start wires off.

Measure DC Outputs	Stage I MSF	Stage II	
+1.25 A2K2D03 for	.31V	0V	Initial Volt.
- 3.00 A2K2B06	.6V	0V	Initial Volt.
+7.00 A2K2G09	1.5V	1.5V	Initial Volt.

Power Down!
Put respective start wires back.
Bias breaker is on.
Power up adj +1.25, -3, and +7 volts.

(If not at this initial value, adjust by varying voltage adjustment potentiometer. If unattainable, replace regulator card. If that does not fix it, replace the regulator.)

9

POWER-ON SEQUENCE

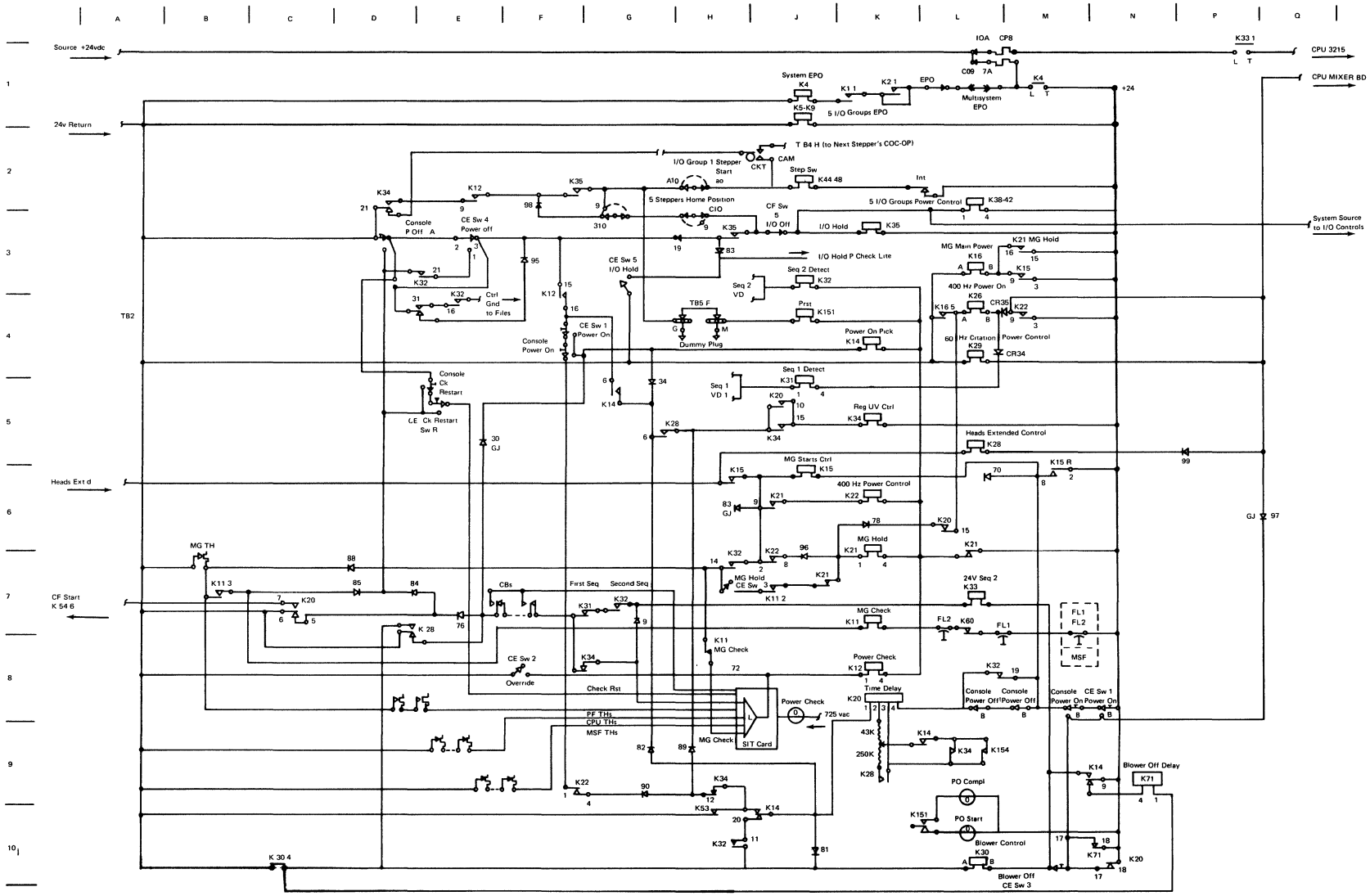
Initial power-on sequence on the 3145 requires 208 vac three-phase 60 Hz 100 amp service. Assuming all AC CBs are made, and there are no thermals or circuit protectors tripped, the following write-up is a sequential description of a normal power-on sequence.

Initial Power-On Sequence

Action	Result	Diagram Coordinate
1. Phase rotation input correct	Pick K1	Not Shown
2. K1 points and EPO okay	Pick K4	J1
K4 contacts supply +24vdc to Seq Circuits		M1
3. +24vdc and all I/O group EPO okay (For Initial power K11, which is a reed relay, MG check must be picked by depressing either the console power-off key or the check reset key.)	Pick K11	K7
(Circuit is through diode 85 CK reset console power Off)		E5 D3
The +24vdc to the K11 pick coil is fed through a K60 n/c point. K60 is the overvoltage detect relay and should be down.	K60 n/c	L7
4. K11 and all thermals and auxillary CB contacts not tripped will satisfy the inputs to the SLT card located at (H9). This will permit the pick of K12.		K8
5. Depress the power-on key	POW Key Pick K14	F4 K4
6. K14 points (G5)	Pick K15	J6

Action	Result	Diagram Coordinate
7. K15 points (M4) K16 is the contactor that allows the 208v input to the motor generator. This allows the motor generator to start. To start the generator with no load, a time delay of 15 seconds is activated. This is a function of time delay relay K20. K20 received a pick from K14 points at (H9), but will not actually transfer its points for 15 seconds.	Pick K16 CONDITION K20	M4 K8
8. K20 points (L6) K21 provides a hold for K16 (M3).	Pick K21	K7
9. K21 points (J6) K22 drops the time delay relay K20 by opening K22 points at (F9)	Pick K22	K6
10. K22 points (M4)	Pick K26 K28 K29	L4 400 Hz to System Starts Regs L5 Heads Ext Ctrl L4 AC Power to 3210
11. K28 points (G5) pick K20 time delay for second time. The points of K20 will not transfer for 15 seconds.	CONDITION K20	K9
K26 points	Pick K27	(Not Shown) 400 Hz to File Motors and Blowers
12. All first seq regs at 60% K31 is picked by a multi-input comparator card that ANDs voltage detection from all regulators.	Pick K31	J4 First Seq Complete
13. K31 points start seq 2 regulators. When the seq 2 regulators reach 60%, the voltage detect circuit is satisfied. Its output will . . .	Pick K32	J3 Second Seq Complete

Action	Result	Diagram Coordinate
14. K31 and K32 points closed at (G7) K33 points at (P1) +24v to CPU and 3215.	Pick K33	L7
15. K20 points transfer (J5) The K34 points at (G8) have been interlocking the power check circuits at (J9). Since sequence 1 and 2 are now complete, undervoltage detection is activated by opening the K34 points. K34 points (H9) drop K20.	Pick K34	K5 Reg UV Control
16. K34 points (D2) This circuit requires all SIO stepper switches to be in home position. K38-42 come up together and allow I/O sequencing to start.	Pick K35	K3
	Pick K38-42	L3
17. K44-K48 come up sequentially. K44 starts stepping. When it completes, it starts K45, etc. When the sequence of the stepper switches is complete . . .	Pick K151	J4 Power on Reset
K151 points (not shown) and provide: 1. CPU clock start. 2. Start console file. 3. Power-on complete.	Pick K53 Pick K154	Console File AC Console File DC


Source +24vdc
24v Return
Heads Ext d
CF Start K 54 6
TB2
IOA CP8
C09 7A
K33 1
CPU 3215
CPU MIXER BD
System Source to I/O Controls
GJ 97
99
+24
System EPO
K4
K1 1
K2 1
EPO
Multisystem EPO
K5-K9
5 I/O Groups EPO
T B4 H (to Next Stepper's COC-OP)
I/O Group 1 Stepper Start ao
CKT
CAM
Step Sw
K44 48
Int
A10
5 Steppers Home Position
CIO
CF Sw 5
I/O Off
I/O Hold
K35
5 I/O Groups Power Control
K38-42
K34
K12
K35
Console P Off A
CE Sw 4 Power off
Ctrl Gnd to Files
I/O Hold P Check Lite
CE Sw 5 I/O Hold
Seq 2 Detect
Seq 2 VD
Prst
K151
TB5 F
Dummy Plug
MG Main Power
K16
K21 MG Hold
K15
400 Hz Power On
K26
CR35
K22
60 Hz Citation
Power Control
K29
CR34
Power On Pick
K14
Console Power On
CE Sw 1 Power On
Console Ck Restart
CE Ck Restart Sw R
Seq 1 Detect
K31
Seq 1 VD 1
K20
Reg UV Ctrl
K34
Heads Extended Control
K28
MG Starts Ctrl
K15 R
400 Hz Power Control
K22
MG Hold
K21
MG Hold CE Sw
K11 2
24V Seq 2
K33
MG TH
K11 3
K20
K 28
CBs
First Seq
Second Seq
K31
K32
MG Check
K11
FL1
FL2
K60
MSF
CE Sw 2
Override
Check Rst
PF THs
CPU THs
MSF THs
Power Check
K12
Time Delay
725 vac
SIT Card
43K
250K
K28
K154
PO Compl
PO Start
K151
Blower Control
K30
Blower Off CE Sw 3
Blower Off Delay
K71
Console Power Off
Console Power On
CE Sw 1
K 30 4

START LINE TIPS

Start lines are a low-cost and low-noise method of starting regulators in a controlled sequential manner as compared in the past to separates DC-controlled contactors which are noisy and costly It is important for customer engineers to know how to manipulate regulators when problems occur

		Typical Reg 5 CPU	MSF	Normal Running Voltage Across Start Line
MST Dual Start Lines are	E8-E11*	101,102, 103,104, 105,107	201	05v
MST Single Lever +7v,+6v are	E12-E14	106,108, 402,401	202	05v
Phase Control Regs +2v are	E8-03A2 D08	110,111, 112,405, 406,407	207,208, 205,206	Open
Phase Control Regs +1 25/-3 are	E8*-03A2 D08	403,404		.05v

* Short to ground (AC Frame) to turn on
Pull any E8 slipon connector off to turn on a +2v supply.
Do not short to ground, but put a jumper between E12 and E14.
Float about seven volts above ground.

11 - 13vdc

If DC distributor, DC bulk input (MST regs E1 and E2) and DC bias 18-20vdc are all present. Then if a problem exists it will usually show up as an improper start signal

SYSTEM CHECK LIST

Troubleshooting Action

DC Voltage At Gate

If no voltage is present from a regulator:
- Check the wiring, especially the sense leads.
- Check for bulk voltage at regulator terminals E1 and E2.
- Check for bias voltage at regulator.
- With an oscilloscope, check for an output increasing then turning off, indicating either an overcurrent or an overvoltage. An overcurrent usually indicates a problem in the system, not in the regulator. An overvoltage usually indicates a bad regulator.

  Since the regulators are somewhat dependent on each other, a problem on one can cause an overcurrent or an overvoltage on another.

  It is important to find the problem that occurred first.

AC Ripple Voltage At Gate

If the ripple voltage is greater than the values listed, the regulator is probably oscillating. This can be caused by:

- Wrong sense load connection at the gate.
- Bad sense caps at the gate.
- Another regulator could also be oscillating.
- A bad regulator itself.

AC Ripple Frequency At Gate

If there is any ripple voltage at the gate, it should have a frequency of 2.4kHz. If it is about 1mHz or higher along with a high ripple voltage, the regulator could be oscillating. Refer to the preceding step.

AC Ripple Voltage At Bulk: E1 to E2 at Regulator

If the ripple voltage is greater than the values listed, a regulator could be oscillating. (The bad regulator could be on another transformer). Voltage peaks should be within 0.2v of each other.

AC Ripple Frequency At Bulk: E1 to E2 at Regulator

Voltage peaks should be 0.4 milliseconds apart (2.4kHz) if one peak is missing a diode could be bad.

Remote Start Noise (DC) At Regulator

When the system is running, the DC voltage shift including noise spikes should be less than 150mv. If this is too high, check the sequencing circuitry.

DC Start-Up Voltage At Gate

The +7v, 1.25v, and -3v for the memory have controlled start up ramp voltages. If they have input power but no start signal, the output voltages are:
+7v is approximately +1.5vdc.
+1.25v is approximately 0.35vdc.
-3v is approximately -0.6vdc.

DC Start-Up Voltage At Remote Start Points At Regulator

Without the start signal, the remote start points at the regulator will be between +4v to +16v. When the start line closes, the voltage should go to overvoltage. Refer to "Remote Start Noise (DC At Regulator)."

Sense Point Noise Shots

In some systems, noise shots have been seen when equipment such as typewriters are turned on. In some cases, these noise shots have fired the overvoltage circuits in a regulator, turning it off.

AC Input Current Waveform Symmetry OCR

Refer to "Procedure For Isolating The Improper SCR Firing Sequence Condition On 2v-250A Regulator."

AC Input Current Balance

Refer to the preceding step.

OCR Reset Pulse

Refer to 2v (250A and 290A) Reset Pulse Adjustment. There is no adjust for the OCR Dual.

OCR Gate Pulse

The gate pulse for all OCRs is approximately 12 microseconds wide with an amplitude of three to five volts. The pulses should occur every 0.4 milliseconds. The pulses should be stable and have no ringing or extra pulses.

Overvoltage Levels

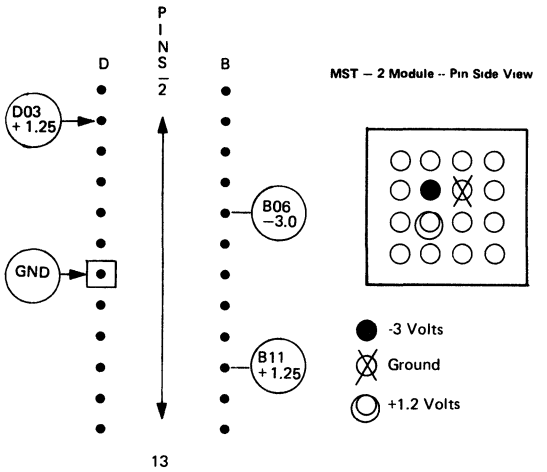
The overvoltage levels are listed so it can be determined if a regulator went over voltage and activated its protection circuit.

Voltage Codes

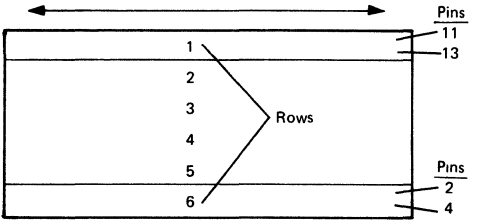
Code	Min Up Level (Volts)	Min Down Level (Volts)
B	2.5 to 2.1	1.9 to 1.5
C	2.5 to 2.1	1.4 to 1.0
D	1.9 to 1.6	1.4 to 1.0
E	2.0 to 1.6	0.9 to 0.6
F	4.0 to 3.5	0.5 to 0.3
G	2.5 to 2.1	0.5 to 0.3
H	2.0 to 1.6	0.5 to 0.3
J	1.5 to 1.1	0.5 to 0.3
L	0.7 to 0.5	0.4 to 0.2
T	0.3	-0.3
Z	-1.0	-1.5

Block Characters

C	Control line of PH
CD	Controlled data line of PH
J	Set line. See flip flop
K	Reset line. See flip flop
R	Reset line
S	Set line
T	Complement line. See flip flop
U	Unloaded output
X	Nonlogical line (Exm bias)
*	Indicated off board connection or labeled load resistor



Upper and Lower Row Tri-Lead Locations



MST Board (Wiring Side)

Upper row (1) are pins 11 and 13
Lower row (6) are pins 2 and 4

9

Voltage Locations On Phase 2 I STG Array Boards

Voltages are applied to EACH card. Each card occupies two connector positions

+7V	**B09**	**-3**	**B06**
+2V	**B04**	**GND**	**D08/B13**
+1.25V	**D03**		

4-Wide Card Socket

D	B
J	G
P	M
U	S

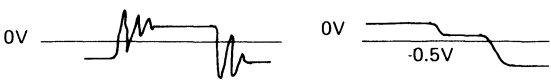
Wiring Side

VOLTAGE LEVELS - SCOPING INFORMATION

1. MST voltage swing is approximately +0.4v to −0.4v. Depending on the load, this signal will vary slightly.
2. Scope probes must always be grounded.
3. Lamp driver +2.0 is the up level; +0.3v is the down level.
4. Interface line +3.0 is the up level; 0.0v is the down level.
5. All lines longer than twelve inches must be terminated (a 90 resistor is used). These resistors may be on an MST card or may be terminated with a PLOT (plug on terminator). In the FEALDs, a terminator on the MST card is shown by an asterisk on an input line to a logic page and a note at the bottom of the page.

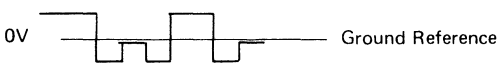
Example: −1 time buffered − RT011 BB6* −

A PLOT is another terminator that plugs into the tri-lead cable. PLOTs are shown in the ZA and ZB logic pages. Missing PLOT can be detected by an excessive amount of oscillation on a signal level.



Note: Missing PLOTs cause the machine to be very sensitive to noise.

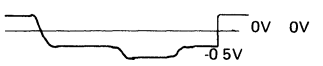
6. Bad levels may appear to come from the external assemblers (BE and BF logic) because of spare inputs. Spare inputs are left floating. This causes the output to appear like a bad level.



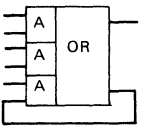
The output signal should not be gated anywhere during the time the signal does not pass through ground. Also, there should be a note on the logic page involved.

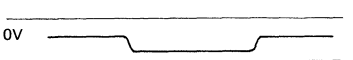
9

7. Examples of outputs from correctly operating nets that may look as if they are double-terminated.

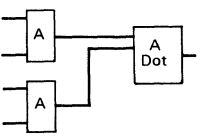


The above waveforms are typical outputs of an A0 type circuit. The double hump on the negative swing indicates that two input AND circuits are active.

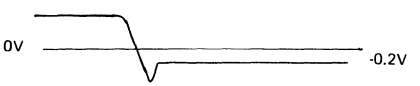




The above waveform is typical of A dot AND Ckt. With two nets tied together, the positive signal will pull up a negative signal.



8. The following is an example of a double-terminated net output.



9

Special Note

- Signal lines cannot be tied down to -3V or ground
- Signal lines should not be tied up to +1.2V directly
- Signal lines can be tied up to +1.2V through a resistor network located on each board's clock card location pins B07 or B08.

Pulling Cards With Power On

Most cards in the A & B gates can be pulled out and extended or swapped without dropping power. Exceptions to this are:

1. Local-Storage Cards 01A-B4–M2,P2,01A–C4–B2,C2
2. Storage-Protect Cards–01A–A1–H4,J4,K4, L4
3. Phase 21 Memory Cards
4. ECC Board Cards 01B-A3
5. Memory Select Card 01A-C1F2

Note:

1. It may be necessary to IMPL after a card is extended or swapped.
2. Board covers should not be left open for an extended period of time.
   (Possible false errors or thermal checks.)

MISCELLANEOUS PART NUMBERS

Tools and Test Equipment:

Digitec* 251 Meter	P/N 453585
Console File Gram Gauge	P/N 2200154
Console File Pressure Pad	P/N 2200343
Console File Alignment Disk	P/N 2200345
MG Converter Text Box	P/N 2637491
IFA Diagnostic Wrap Tool	P/N 1994492
Interface Wrap Cable (Direct Ctrl)	P/N 2227492

PARTS

48K Array Fast	P/N 8211171/5854407
48K Array Slow	P/N 8212700/5857299
24K Array	P/N 5858912
48KA Array Fast	P/N 8211171/5854407
48KA Array Slow	P/N 8214216
24KA Array Slow	P/N 8214216
90A Terminator	P/N 817123
Console Ind Red	P/N 5499810
Console Ind Clear	P/N 5499812
Console Ind Amber	P/N 5499811
Air Filter (Gate)	P/N 1994488
Air Filter (Mixer Board)	P/N 5357064

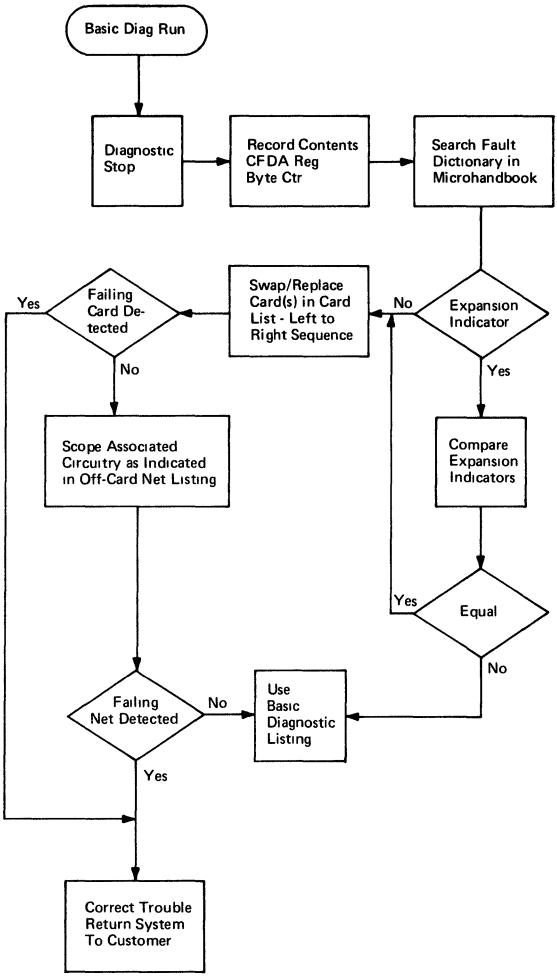
* United Systems Corporation

TERMINATOR PART NUMBERS

9

	System/360	System/370
Bus —	5440649	2282675
TAG —	5440650	2282676

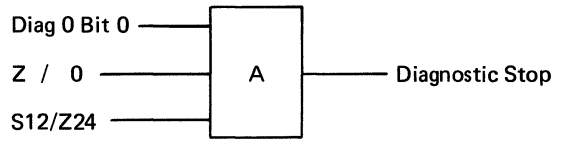
BASIC DIAGNOSTIC FLT



Note. To Loop All Basics, Set Switch H = F

10

BASIC DIAGNOSTIC INFORMATION



Expansion Indicators

RWDP:	BIT	MEANING
	0-3	Not Used
	4	R=1 if start console file key red
	5	W=1 if start console file key white
	6	D=1 if diagnostic stop on
	7	P=1 if console file power on

CPUCK:	BIT	MEANING
	0-3	Not Used
	4	M-reg compare
	5	Any machine check
	6	SAR reg parity
	7	Clock sync

CFCKS:	BIT	MEANING
	0	Not Used
	1	Data
	2	Command reg
	3	Disk address reg
	4	Byte Ctr
	5	Pause
	6	Clock start
	7	Counter match

STATS:	BIT	MEANING
	0-3	Not used
	4	Clock stop
	5	Execute complete
	6	Store one cycle
	7	IMPL requested

ABRTY Reg *	Bit	Group Gate 1	Group Gate 2	Group Gate 3
Byte 0	0	Force System Reset Trap	Force S-Reg Dup Check A	**Diag I-Reg and Buffer Gating
	1	Force Alter Display Trap	Force S-Reg Dup Check B	**Enable Generate Address
	2	Force Set IC Trap	Force Ext XY Check	**Enable
	3	Force Control Word Address Trap	Force Dest Byte Control Check	Spare
	4	Force Instruction Ctr Match	Force ALU Logical Check	Allow PAA Hold
	5	Spare	Force LS Source/Dest X Check	Spare
	6	Force Scan Storage Trap	Force LS Source/Dest Y Check	Allow RF Read Out
	7	Force Clear Storage Trap	Force B-Reg Shift Check	Allow Set No Match and Force LRU Inv
Byte 1	0	Spare	Force Clock Control Check	Spare
	1	Block DF Trap Inhibit	Force M-Reg Dup Check 1	Spare
	2	Allow Ext Interrupt Reg Set	Force M-Reg Dup Check 2	Spare
	3	Force Word Move Stop	Force M-Reg Dup Check 3	Spare
	4	Start Switch Reset	Force M-Reg Dup Check 4	Spare
	5	Block Reset CPU - Low	Force M-Reg Dup Check 5	Spare
	6	Spare	Force M-Reg Dup Check 6	Spare
	7	Force LS Address Check	Spare	Spare
Byte 2	0	Simulate Int Timer, TOD Enable CK	Force Clock Sync Ck A-A1 & A-B1	Spare
	1	MPX Diagnostic Control	Force Clock Sync Ck A-A2 & A-B2	Spare
	2	Spare	Force Clock Sync Ck A-A3 & A-B3	Spare
	3	Force TOD Clock Error	Force Clock Sync Ck A-A4 & A-B4	Spare
	4	Diagnostic Parity Mode (P2I)	Force Clock Sync Ck B-A1 & A-C1	Spare
	5	Diagnostic Ripple Mode (P2I)	Force Clock Sync Ck B-B3 & A-C2	Spare
	6	Spare	Force Clock Sync Ck A-C3	Spare
	7	Spare	Force Clock Sync Ck B-C3 & A-C4	Spare
Byte 3	0	Spare	Spare	Spare
	1	Spare	Spare	Spare
	2	Spare	Spare	Spare
	3	Reset Process Stop Latch	Reset Process Stop Latch	Reset Process Stop Latch
	4	Diag Control SAR (STG)	Diag Control SAR (STG)	Diag Control SAR (STG)
	5	Invert Z-Reg Parity Bits	Invert Z-Reg Parity Bits	Invert Z-Reg Parity Bits
	6	Block A-Local Storage	Block A-Local Storage	Block A-Local Storage
	7	Stop on Machine Check	Stop on Machine Check	Stop on Machine Check

*Note: Use inverted logic for diagnostic functions.
**Note: Also gated by early Group Gate 3.

Flags in LS390

0 Cannot Single Cycle
1 Test Search
2 Last Test
3 Overlay
4 No Loop SSW.
5 Feature Test
6 1 = Read 0 = Write
7 Main Storage Print

Sense Switches in LS3B0

0 Print Exp-Act Rslts
T Loop Test
2 Loop Section
3 Test Step
4
5 Print Bypass
6 Tight Loop
7

LS3B1 = Section

LS3B2 / LS3B3H Test Number

Flags in LS3B3L

4 Already In Test
5
6 Cycle Each Test
7 Retry Flag

Flags in LS3E0

0 No New Line
1 Retain Overlay

Direct and Indirect Access

LS Adr	P Low	P High
00-07	0	0
08-0F	1	0
10-17	2	2
18-1F	3	2
20-27	4	4
28-2F	5	4
30-37	6	6
38-3F	7	6

P low settings are for direct access.
P high settings are for indirect access.

	0	1	2	3
00		Common Work		
01		Area		
02				
03		Undefined		
04				
05		Work		
06				
07		Area		
08				
09				
0A				
0B				
0C				
0D				
0E				
0F		Sys Reset Link		
10		Section		
11				
12		Work		
13				
14		Area		
15	5 5	5 5	5 5	5 5
16	F F	F F	F F	F F
17	F F	F F	F F	F F
18		Actual Results		
19		Field For		
1A		Extended		
1B		CPU FLT		
1C		Common Work Area		
1D		Used By Both		
1E		Monitor and		
1F		Tests		

		Selector		
		Channels		
30	FLT Table Pointer			
31	Backup Pointer for Text Loop			
32	Setup Area Pointer			
33	Test Number Link Register			
34	Monitor Work Register			
35	Monitor Work Register			
36	Monitor Work Register			
37	Monitor Work Register			
38	Print Message Link			
39	Flags	Search	Test	Ident
3A	Monitor		Link	
3B	Flags Section		Alpha Dec Flags	
3C	Current Test Link			
3D	Error Flags			
3E	Flags	Flags Err Cor		Feat 3
3F	Section Link		Reg	

Sense Switches in LS3B0

0 Print Exp-Act Rslts
1 Loop Test
2 Loop Section
3 Test ID
4
5 Print Bypass
6 Print Errors
7 Print Instructions

Flags in LS3E1

0
1 *EX1 was run
2 *EX2 was run
3 *EX3 was run

Flags in LS390

0 Cannot Single-Cycle
1 Test Search
2 Last Test
3 Overlay
4 No Loop SSW
5 Feature Test
6 1 = Read 0 = Write
7 Main Storage Print

Flags in LS3B3L

4 Already In Test
5
6 Cycle Each Test
7 Retry Flag

Flags in LS3E0

0 No New Line
1 Retain Overlay
2 Log Failing Test
3 Log Present
4 Extint Bit 1
5 Print Section Message
6 Printer 2 Reset
7 Restart Manuals

DIAGNOSTIC TEST LISTING

Basic Test Sections

BA	Console File and CPU Functions
BC	Local Storage
BE	CPU Functions
BG	Program and Control Storage
BJ	CPU Functions
BL	3210 Console Printer
BM	3215 Console Printer

Extended Test Sections

EA	Microdiagnostic Monitor	
EA	External Registers	
EC	Machine Check Register	
ED	I-Cycles	
EE	Address Adjust	
EF	MPX Channel	
EG	Trapping and Priorities	
EJ	Selector Channel 1	Use EJ listing when trouble shooting.
EK	Selector Channel 2	
EL	Selector Channel 3	
EM	Selector Channel 4	
EN	Selector Channel Common	
EQ	Storage Protect	
EW	Retry Registers	
EY	Timers - HRT and TOD	
SB	Integrated File Adapter	

Manual Tests

MA	Console Test
MB	Storage Analyzation
MD	Manual Operation of Console Printer
ME	I/O Exerciser
BU	Manual Console File Test

NOTES

EXTERNAL ASSIGNMENT CHART

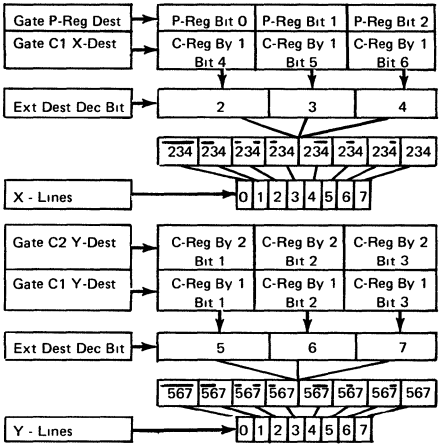
Word Address	Word Name	Byte 0	Byte 1	Byte 2	Byte 3	X Y Line
00	RTY	MB 2	MB 3	ECNT	RCNT	0 0
01	NO REG	NOREG0	NOREG1	NOREG2	NOREG3	0 1
02	DIAG	DIAG0	DIAG1	FEAT2	FEAT3	0 2
03	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	0 3
04	SPTL *	S REG	P REG	T REG	L REG	0 4
05	SYS *	SYS0	SYS1	SYS2	H REG	0 5
06	MCKB *	MCKB0	MCKB1	MCKB2	MCKB3	0 6
07	MCKA	MCKA0	MCKA1	MCKA2	MCKA3	0 7
08	CPU	MODE	CFDAR	LRUM	MATCH	1 0
09	CFDR	CFDR	CFDR	CFDR	CFDR	1 1
0A	ACB	ACB0	ACB1	XXXXXXXX	XXXXXXXX	1 2
0B	SW	SW0	SW1	SW2	SW3	1 3
0C	SPTL *	S REG	P REG	T REG	L REG	1 4
0D	SYS *	SYS0	SYS1	SYS2	H REG	1 5
0E	MPX	MTO	MT1	MBT	MBO	1 6
0F	DOC	TI	TA	TT	TE	1 7
10	PSWCTL			MSKA	MSKB	2 0
11	CTCAX	CTCAX0	CTCAX1	CTCAX2	CTCAX3	2 1
12	MISC	EXTINT				2 2
13	CTCAY	CTCAY0	CTCAY1	CTCAY2	CTCAY3	2 3
14	SPTL *	S REG	P REG	T REG	L REG	2 4
15	SYS *	SYS0	SYS1	SYS2	H REG	2 5
16	IN	INTA	INTB	SER2	SER3	2 6
17	DC	DCB0	DCHI	TSBO	DCHI	2 7
18	ABRTY	ABRTY0	ABRTY1	ABRTY2	ABRTY3	3 0
19	SPTLB	SRTY	PRTY	TRTY	LRTY	3 1
1A	HMRTY		HRTY	MRTY2	MRTY3	3 2
1B	CPURTY	BYDST	RTYFLG	LSDST	EXTDST	3 3
1C	SPTL *	S REG	P REG	T REG	L REG	3 4
1D	SYS *	SYS0	SYS1	SYS2	H REG	3 5
1E	PIR	PIR0	PIR1	PIR2	PIR3	3 6
1F	PIRM	PIRM0	PIRM1	PIRM2	PIRM3	3 7

Word Address	Word Name	Byte 0	Byte 1	Byte 2	Byte 3	X Y Line	
20	GBUF FBAK	GB0 FWB	GB1 FCH	GB2 FCL	GB3 FOP	4 0	
21	GBS FCND	GSP FDS	GBF FHC	GCT FED	GBD FMOD	4 1	
22	GSTAT FSTAT	GF FFL	GE FCS	GS FST	GL FGL	4 2	SX1/IFA
23	GTAG FTAG	GTO FTO	GTI FTI	GO FBO	GR FDR	4 3	
24	SPTL *	S REG	P REG	T REG	L REG	4 4	
25	SYS *	SYS0	SYS1	SYS2	H REG	4 5	
26	FERR	FSB	FGT	FTS	FAT	4 6	IFA
27	CKCPT	CKCPT 0	CKCPT 1	CKCPT 2	CKCPT 3	4 7	
28	GBUF	GB0	GB1	GB2	GB3	5 0	
29	GBS	GSP	GBF	GCT	GBD	5 1	SX4/IFA
2A	GSTAT	GF	GE	GS	GL	5 2	
2B	GTAG	GTO	GTI	GO	GR	5 3	
2C	SPTL *	S REG	P REG	T REG	L REG	5 4	
2D	SYS *	SYS0	SYS1	SYS2	H REG	5 5	
2E						5 6	
2F						5 7	
30	GBUF	GB0	GB1	GB2	GB3	6 0	
31	GBS	GSP	GBF	GCT	GBD	6 1	SX2
32	GSTAT	GF	GE	GS	GL	6 2	
33	GTAG	GTO	GTI	GO	GR	6 3	
34	SPTL *	S REG	P REG	T REG	L REG	6 4	
35	SYS *	SYS0	SYS1	SYS2	H REG	6 5	
36	TODH	TODH0	TODH1	TODH2	TODH3	6 6	
37						6 7	
38	GBUF	GB0	GB1	GB2	GB3	7 0	
39	GBS	GSP	GBF	GCT	GBD	7 1	SX3
3A	GSTAT	GF	GE	GS	GL	7 2	
3B	GTAG	GTO	GTI	GO	GR	7 3	
3C	SPTL *	S REG	P REG	T REG	L REG	7 4	
3D	SYS *	SYS0	SYS1	SYS2	H REG	7 5	
3E	TODL	TODL0	TODL1	TODL2	TODL3	7 6	
3F						7 7	

may not be used as a destination

NOTES:
1. Shaded bytes may not be used as a destination
2. * — Not flush-through checked
3. x — Roller display
4. Both MCKA and MCKB are set to zero when MCKA is used as a destination in a word-move-word with the NOREG as the source

EXTERNAL ADDRESS LINE DECODING



EXTERNAL GATING TO A-REGISTER

Gate	Word Addr	External Assembler	Word Addr	Expanded External Assembler
Gate Ext Group A'	0B	Switches A-H		CPC Asm
	09	CF-DATA-REGISTER		
Gate Ext Group,B'	00	MB2,MB3,ECNT, RCNT	26	IFA (word 26)
	02	DIAG0,DIAG1, FEAT2,FEAT3	36	TODH0,TODH1, TODH2,TODH3
	0A	ACB0,ACB1	3E	TODL0,TODL1, TODL2.TODL3
Gate Ext Group,C'	18	ABRTY0,ABRTY1, ABRTY2,ABRTY3	IE	PIR (Spare)
	19	SRTY,PRTY,TRTY, LRTY	IF	PIRM (Spare)
	IA	HRTY,MRTY2,MRTY3		
	IB	BYTDST, RTYFLG, LSDST,EYDST		
Not Gate Ext Group ABC'	20-23	IFA or SX1	10	EPSWA,EPSWB, MSKA,MSKB
	30-33	SX2	11	CTCAX0,CTCAX1, CTCAX2,CTCAX3
	06	MCKB	12	EXTINT,EC,SER1
	07	MCKA	13	CTCAY0,CTCAY1, CYCAY2,CYCAY3
	0E	MTO,MTI,MBI,MBO	08	MODE,CFDAR, LRUM,MATCH
	0F	TI,TA,TT,TE	17	DCBO,DCHI,TSBO,DCBI
	05	SYS0,SYS1,SYS2, H-REG		
	16	INTA,INTB,SER2,SER3		

Byte	Bit	RTY - 00
0	0 1 2 3 4 5 6 7	MB2 0-7-Address Back-up for M2 Reg RM035 Displayed in Upper Roller Position 4
1	0 1 2 3 4 5 6 7	MB3 0-7-Address Back-up for M3 Reg Bits 0-3 RM073 Bits 4-5 RM223 Bits 6-7 RM052 Displayed in Upper Roller Position 4
2	0 1 2 3 4 5 6 7	ECNT 0-7-Maintains a Single-Bit Correction Count for Both the Main and Control Storages RE061 RE062
3	0 1 2 3 4 5 6 7	RCNT 0-7-Maintains a Retry Count When: — A Trap Request is Present — The CPU is in the Trap 1 Cycle RH031

Bytes	NOREG - 01
0-3	Fullword facility that is used to Zero Out Other Locations. When a NO REG is specified, the associated destination is set to all zeros.

Byte	Bit	DIAG - 02
0	0	Z/0 Stop or Preserve RD021
		Bad Parity
	1	Multifunction Bit
	2	Force Z-Reg Parity Bits
	3 Diag 0	Suppress All Traps
	4	Diagnostic Group Gate 1
	5	Diagnostic Group Gate 2
	6	Diagnostic Group Gate 3
	7	Diagnostic Group Gate Delayed Pulse
1	0	Selector Channel RD024
		Force Trap Bit 4
	1	Selector Channel RD023
		Force Trap Bit 5
	2	Selector Channel 4 RD021
		Priority Request (H4)
	3 Diag 1	H3 Trap Request
	4	Selector Channel Check Indicator
	5	Spare
	6	Spare
	7	Diagnostic Key (Display Only)
2	0	Main Storage Size: RD051
	1	1 = 112K 4 = 256K
	2	2 = 160K 5 = 384K
	3 Feat 2	3 = 208K 6 = 512K
	4	IFA
	5	Channels (IFA Counts as 1 Channel)
	6	00 = 1 01 = 2 10 = 3 11 = 4
	7	Word Buffer
3	0	Spare RD052
	1	3215
	2	Second SELECTRIC
	3 Feat 3	Spare
	4	CPU Timer
	5	Spare
	6	Spare
	7	Direct Control

Byte	Bit	Ext Address 03
		This facility is not used on the 3145.

Byte	Bit		SPTL - 04 (Also 0C,1C,2C,3C,14,24,34)
0	0		True/Complement Addition
	1		Decimal = 1 if Invalid Digit; Binary = 1 Carry-Out of Bit One
	2		Equals 1 if Z-Bus Not Zero
	3	S	Carry-Out of Bit Zero
	4		ALU Result 0-3 = 0
	5		ALU Result 4-7 = 0
	6		General Purpose Stats
	7		RS125 RS225
1	0		Expanded LS A Source
	1		Used with L-Reg to Form Indirect LS Address
	2		
	3	P	External Address if C1 Bit 0 = 1
	4		Expanded LS B Source
	5		Used With C1,C2 to Form Direct LS Address
	6		
	7		RP011 RP012
2	0		TH - Mask for Store Word Function
	1		
	2		
	3	T	
	4		TA - Byte Pointer for Indirect Byte A Source
	5		
	6		TB - Byte Pointer for Indirect Byte B Source
	7		RT012 RT013
3	0		LH - L High The L-Reg holds intermediate byte operand(s).
	1		
	2		
	3	L	
	4		LL - L Low
	5		
	6		
	7		RL011

Byte	Bit		SYS - 05 (Also 0D,1D,2D,3D,15,25,35)
	0		Machine-Check Interrupt Pending
	1		Retry Routine
	2		Machine Check Mark
0	3	Sys 0	DOC Console (2)
	4		LOG Present
	5		Sub-Block Protection Mode
	6		Selector Channel Start I/O Latch
	7		Force Module 0 to Local Storage
			Control Storage (LSCS) RS011
	0		Enable Clear Switch
	1		IMPL
	2		Console-File Wait Bit
1	3	Sys 1	Meter Switch in CE Mode
	4-5		00 = Unassigned
			01 = Power On Reset
			10 = Subsystem Load
			11 = System Load
	6		Error In Stop Word
	7		Instruction Processing Lath RS012
	0		Address Contents
	1		CPU Interruption Force
	2		SAR Interruption Force (Monitor)
2	3	Sys 2	PSW Restart
	4		EVR Latch
	5		System Control Interruption
	6		Timer Interruption Force
	7		Reserved For Priority Interrupt RS013
	0		Machine Check Priority Operation
	1		Retry Priority Operation
	2		CPU High-Priority Operation
3	3	H-Reg	SX 1,2, and 3, or IFA High-Priority Operation
	4		SX2,3 (If IFA Installed)
			SX4 Only (If Installed)
	5		Multiplexer Channel
	6		IFA Low-Priority Operation
	7		Store/Display and Logout RH022

Byte	Bit	MCKB 06
0	0	Storage Address Check
	1	SDBI Parity Check
	2	SDBO Parity Check
	3	Store Parity Check
	4	Spare
	5	Store Protect Parity Check
	6	Clock Sync Check A
	7	Clock Sync Check B
		RE041 RE045
1	0	M-Reg Compare Check A
	1	M-Reg Compare Check B
	2	M-Reg Compare Check C
	3	M-Reg Compare Check D
	4	Addr Xlate No Match
	5	Addr Xlate Multimatch
	6	Addr Xlate LRU Invalid
	7	Any Machine Check
		RE011 RE043
		RE044 RE046
2	0	I-Cycle Hardware
	1	
	2	Control Line Parity Check
	3	ECC Busy Check
	4	ECC Hardware Check
	5	Double ECC Error
	6	Data or Check Bit Failure
	7	Data Bit Failure
		RE051
3	0	CT
	1	C32
	2	C16
	3	C8
	4	C4
	5	C2
	6	C1
	7	C0
		RE052

Byte	Bit	MCKA 07
0	0	LS A Source Address Check
	1	LS B Source Address Check
	2	LS A Destination Address Check
	3	LS B Destination Address Check
	4	Destination Byte Control Check
	5	LS A, B Destination Address Compare
	6	LS Control Assembler Check
	7	C-Register Parity Check
		RE021
		RE022
1	0	ACB Register Parity Check
	1	LS Compare Check
	2	Flush Through Check
	3	H-Register Parity Check
	4	Spare
	5	P-Register Parity Check
	6	T-Register Parity Check
	7	L-Register Parity Check
		RE023
		RE024
2	0	ALU 2 Halfsum Check
	1	ALU 3 Halfsum Check
	2	ALU Logical Check
	3	B-Register Shift Check
	4	A-Register Parity Check
	5	B-Register Parity Check
	6	Z-Register Parity Check
	7	D-Register Parity Check
		RE031
		RE032
		RE033
3	0	External Destination X-Compare
	1	External Destination Y-Compare
	2	External Source Y-Check
	3	External Control Assembler Parity Check
	4	Interval Timer Parity Check
	5	S-Register Duplicate (Compare) Check
	6	Time-of-Day Clock Parity Check
	7	Control Storage Address Check
		RE041
		RE034

Byte	Bit	CPU 08
0	0 1 2 3 4 5 6 7	Hard Stop Latch Register 14 Bit 0 Enable I-Cycle and ADR/ADJ Ctrl and EXPLS Enable Hardware Retry Mode Full Recording Mode MS Single ECC Errors Full Recording Mode CS Single ECC Errors Threshold Mode CS Single ECC Errors Reserved Reserved RM811
1	0-7	Track and Sector Address - CFDA Console File KF031
2	0-7	LRUM Least Recently Used ADR/ADJ Table Register MT215
3	0-7	Match ADR/ADJ Table Reg Matches Preaddress Asm MT332

Byte	Bit	CFDR - 09
0-3		CF Data Register KF014-017

(RM811, KF031, MT215, MT332)

Byte	Bit	ACB OA
0	0 1 2 3 4 5 6 7	Spares ACB0 Compared with M1 Bits 4-7 on all Main Storage Accesses
1	0 1 2 3 4 5 6 7	Compared with M2 Bits 0-4 for all Storage Accesses (Bits 0 and 1 May Be Altered for Control Storage Accesses) ACB1 5 = 0 Internal Storage Only 67 = 00 = 16K Bound 01 = 32K Bound 10 = 48K Bound 11 = 64K Bound 5 = 1 Ext Storage 67 = 00 = 128K Ext Storage 01 = 256K Ext Storage
2	0-7	Spare
3	0-7	Spare

(MC015-016)

Byte	Bit	Sw - 0B
0	0-7	Rotary Switches A and B
1	0-7	Rotary Switches C and D
2	0-7	Rotary Switches E and F
3	0-7	Rotary Switches G and H PA011,PA041,PA211,PA241

Byte	Bit		MPX - 0E	
0	0 1 2 3 4 5 6 7	MTO	Operation Out Select Out Address Out Command Out Service Out Interrupt Suppress Out Spare	FA013
1	0 1 *2 *3 4 5 6 7	MTI	Operation In Address In Status In Service In Select In MPX Request In MPX or Console Request In Disconnect In	*Bits 23 —— 00 = Operation In-Up 01 = Service In-Up 10 = Status In-Up 11 = Operation In-Up FA011 FA012
2	0-7	MBI	MPX Channel Bus-In Data	FA111 FA121
3	0-7	MBO	MPX Channel Bus-Out Data	FA014

Byte	Bit		DOC - 0F
0	0-7	TI	Hold the Documentary Console Bus-In Data PD025
1	0 1 2 3 4 5 6 7	 TA 	Read Latch Write Latch Stacked Request Share Request Attention Reset Alarm Sense Share Set Spare PD041
2	0 1 2 3 4 5 6 7	 TT 	Attention Ready Spare Cycle Intlk Spare End Console Request Cancel PD043
3	0-7	TE	Holds the Documentary Console Bus-Out Data PD042

Byte	Bit	PSWCTL 10	
0	0		Reserved
	1		Mask PER
	2		Reserved
	3	EPSWA	Priority Mask
	4		Reserved
	5		Translation Mode
	6		I/O Master Mask
	7		External Master Mask
			RJ011
1	0		Reserved
	1		Reserved
	2		Reserved
	3	EPSWB	Reserved
	4		EC Mode
	5		Machine Check Mask
	6		Machine Check Mask
	7		Wait
			Problem Bit
			RJ012
2	0		Timer Mask
	1		Ext Int Key Mask
	2		External Signal Mask
	3	MSKA	Reserved
	4		Reserved
	5		Reserved
	6		Reserved
	7		Reserved
			RJ011
3	0		MPX Channel Mask
	1		Sel Channel 1 Mask
	2		Sel Channel 2 Mask
	3	MSKB	Sel Channel 3 Mask
	4		Sel Channel 4 Mask
	5		Reserved
	6		Reserved
	7		Reserved
			RJ012

Byte	Bit	MISC - 12	
0	0-7	Extint	External Interrupt Signals BE071
1	0-7		Reserved
2	0-7	EC Level	Last Two Digits of Micro EC Level RD061
3	0-7	Serial 1	First Two Digits of Machine Serial No. RD072

CHANNEL TO CHANNEL FEATURE

Byte	Bit	CTCAX - 11 and CTCAY - 13
0	0 1 2 3 4 5 6 7	Command Check Intervention Required Buffer Check Equipment Check Selection Check Sequence Check Status Generation Check HIO or Selective Reset BF001 BF002
1	0 1 2 3 4 5 6 7	Ready Latch Select Propagate Side Selected Sequence Counter 1 Sequence Counter 2 Sequence Counter 3 Sequence Counter 4 Sequence Counter 5 BF002 BF001
2	0 1 2 3 4 5 6 7	Disconnect Status Parity Bit Predict Attention Latch Busy Bit Channel End Device End Unit Check Unit Exception BF001 BF002
3	0 1 2 3 4 5 6 7	Stack Status Latch Write Command Read Command Control Command Sense Command End-of-File Command Spare Enable Compatibility (Ext 11)/Data-In Mode (Ext 13) BF002 BF001

NOTE: Odd parity not maintained in these externals. Refer to XX—— logics.

	Byte	Bit	IN - 16
INTA	0	0	Spare
		1	Spare
		2	Timer
		3	External Signal
		4	System Control
		5	CPU Signal 0
		6	CPU Signal 1
		7	Process Stop
INTB	1	0	MPX Channel
		1	Selector Channel 1
		2	Selector Channel 2
		3	Selector Channel 3
		4	Selector Channel 4
		5	I/O Interrupt
		6	Timer Update
		7	External
Ser 2	2	0-7	Middle Two Digits of Machine Serial No.
Ser 3	3	0-7	Last Two Digits of Machine Serial No.

(RJ011-012, BE161)

Byte	Bit		DC - 17
0	0-7	DCBO	Direct Control Bus-Out
1	0		Direct Control Hold-In
	1-7	DCBI	Unused
2	0-7	TSBO	Timing Signal Bus-Out
3	0-7	DCHI	Direct Control Bus-In

JA021-023

Byte	Bit	ABRTY - 18 (Retry)
0	0-7	
1	0-7	Contains source data of A- or B-register for retry. Word Type A = A/B A-Reg Saved B = A/B B-Reg Saved
2	0-7	
3	0-7	(RR111-144)

Byte	Bit	SPTLB - 19 (Retry)
0	0-7	S-Reg Backup
1	0-7	P-Reg Backup
2	0-7	T-Reg Backup
3	0-7	L-Reg Backup (RR114-144)

Byte	Bit	HMRTY - 1A (Retry)
0	0-7	Spare
1	0-7	HRTY H-Reg Backup RR125
2	0-7	MRTY 2 M-Reg (Byte 2) Backup RR135
3	0-7	MRTY 3 M-Reg (Byte 3) Backup RR145

Byte	Bit	CPURTY - 1B (Retry)	
0	0-3	BYDST	Spare
	4		Dest Byte 0
	5		Dest Byte 1
	6		Dest Byte 2
	7		Dest Byte 3 (RR116-118)
1	0	RTYFLG	Error in Stg 2 Cycle
	1		Type 1 Error
	2		Type 2 Error
	3		Type 3 Error
	4		Ext Dest (0 = LS Dest)
	5		Stg Word
	6		Trap 2 Cycle Error
	7		Unretriable (RR012)
2	0		Spare
	1-3	LSDST	LS Y-Addr
	4-6	LSDST	LS X-Addr
	7		Exp LS Dest (RR136)
3	0		Spare
	1-3	EXTDST	External Y-Addr
	4-6	EXTDST	External X-Addr
	7		Spare (RR136-148)

Byte	Bit	Spare - 1E

Byte	Bit	Spare - 1F

Byte	Bit	G1BUF (SX1 Only) 20,28,30 & 38		
0	0 1 2 3 4 5 6 7	GB0	Fwd = B0 Bkwd = B3	GC611
1	0 1 2 3 4 5 6 7	GSP	Spare Spare Spare Spare Spare Spare Spare Spare	
2	0 1 2 3 4 5 6 7	GF	Chain Data Command Chain Sup Length Ind Skip Allow Halt Input Fwd Input Bkwd Output	GB712 GB412
3	0 1 2 3 4 5 6 7	GT0	Operational Out Select Out Address Out Command Out Service Out Data Out Suppress Out Spare	GB313 GB213 GB312 GB312 GB113 GB113 GB212

Selector Channel Logics

GA Pages Common to All Channels
GB and GC = Channel 1
GF and GG = Channel 2
GK and GL = Channel 3
GP and GQ = Channel 4

Byte	Bit	G1BS (SX1 Only) 21,29,31,39		
0	0 1 2 3 4 5 6 7	GB1	Fwd = B1 Bkwd = B2	GC621
1	0 1 2 3 4 5 6 7	GBF	Spare BF 6 BF 5 BF 4 BF 3 GB 2 BF 1 BF 0	GC311 GC312
2	0 1 2 3 4 5 6 7	GE	Prog Ctrl Interrupt Incorrect Length Program Check Protection Check Data Check Chan Ctrl Check Intf Ctrl Check Chaining Check	GB712 GB411 GB412 GB114 GB513
3	0 1 2 3 4 5 6 7	GTI	Operational In Address In Status In Service In Select In Data In Request In Disconnect In	GB211

Selector Channel Logics

GA Pages Common to All Channels
GB and GC = Channel 1
GF and GG = Channel 2
GK and GL = Channel 3
GP and GQ = Channel 4

Byte	Bit	G1STAT (SX1 Only) 22,2A, 32,3A		
0	0 1 2 3 4 5 6 7	GB2	Fwd = B2 Bkwd = B1	GC631
1	0 1 2 3 4 5 6 7	GCT	Buffer Ctrl Check Count Through 0 Chain Data Request Buffer Partition GCL 0 GCL 1 GCL 2 GCL 3	GC513 GC412 GC413 GC413 GC412
2	0 1 2 3 4 5 6 7	GS	Channel Loaded Interrupt Latch Poll Control Channel Primed DCC Mode Command Retry Gate A/Share Req* Gate B/Trap Req* *(Diag)	GB213 GB213 GB313 GB211 GB213 GB513 GB652
3	0 1 2 3 4 5 6 7	GO	Channel Bus Out Channel Bus Out	GB082

Selector Channel Logics

GA Pages Common to All Channels
GB and GC = Channel 1
GF and GG = Channel 2
GK and GL = Channel 3
GP and GQ = Channel 4

Byte	Bit	G1TAG (SX1 Only) 23,2B,33,3B		
0	0 1 2 3 4 5 6 7	GB3	Fwd = B3 Bkwd = B0	GC641
1	0 1 2 3 4 5 6 7	GBD	Spare GDRL 6 GDRL 7 GB P GB 0 GB 1 GB 2 GB 3	GC414 GC411
2	0 1 2 3 4 5 6 7	GL	Count Ready Count Zero GR Full Interrupt Cond Share Error Spare Position Code	GB413 GB414 GB311 GB413 GB412 GB711
3	0 1 2 3 4 5 6 6	GR	Communication with Data Flow (Data, Command, Address, Status)	GB611

Selector Channel Logics

GA Pages Common to All Channels
GB and GC = Channel 1
GF and GG = Channel 2
GK and GL = Channel 3
GP and GQ = Channel 4

Byte	Bit	FBAK - 20 (IFA Only)		
0	0-7	FWB	Spare	
1	0	FCH	32K	File Counter High (JK211)
	1		16K	
	2		8K	
	3		4K	
	4		2K	
	5		1048	
	6		512	
	7		256	
2	0	FCL	128	File Counter Low (JK311)
	1		64	
	2		32	
	3		16	
	4		8	
	5		4	
	6		2	
	7		1	
3	0	FOP	*Op Code (Read)	(JK411-412)
	1		*Op Code (Write)	
	2		Address Mark (Omit)	
	3		Search	
	4		Scan	
	5		Index Hold	
	6		Format	
	7		Skip	

Byte	Bit	FCND - 21 (IFA Only)
0	0	Busy
	1	On-Line
	2	Unsafe
	3	FDS Spare
	4	Pack Change
	5	End of Cylinder
	6	Multimodule Selected (JL511)
	7	Seek Incomplete (WF101)
1	0	FHC Diagnostic, Head/Cylinder (CE Panel)
	1	
	2	
	3	
	4	
	5	
	6	
	7	(FE110)
2	0	FED Diagnostic Error Display (CE Panel)
	1	
	2	
	3	
	4	
	5	
	6	
	7	(JK312)
3	0	Module Select Gate
	1	FMOD Module Select (JK611)
	2	
	3	
	4	Module not Selected
	5	Physical Module Selected (JL511)
	6	
	7	

Byte	Bit	FFL - 22 (IFA Only)	
0	0		Chain Data
	1		Command Chain
	2		Sup Length Ind
	3	FFL	Skip
	4		Spare
	5		Input
	6		Control Store Count Ready
	7		Output (JK111 and JK512)
1	0		Prog Controlled Intrpt (JK111)
	1		Incorrect Length (JK513)
	2		Program Check
	3	FCS	Protection Check (JK212)
	4		Channel Data Check
	5		Channel Ctrl Check
	6		Interface Ctrl Check (JK214)
	7		Spare
2	0		Channel Busy
	1		Interrupt Latch
	2		Control Unit End
	3	FST	Control Unit Busy
	4		Block CE Mode
	5		Spare
	6		Spare
	7		Spare (JK313-315)
3	0		Main Store Count Ready
	1		Count Zero (JK512)
	2		FDR Full
	3	FGL	Interrupt Condition JK416
	4		Share Cycle Error
	5		Retry Code 0
	6		Retry Code 1 JK612
	7		Retry Code 2

Byte	Bit	FTAG - 23 (IFA Only)
0	0	Set Cylinder Tag
	1	Set Head Tag
	2	Set Difference Tag
	3	FTO Control Tag
	4	CUA Load
	5	Spare-A
	6	Spare-B
	7	Spare-C (JK112)
1	0	128
	1	64
	2	32
	3	FTI 16 — Cylinder
	4	8 — Address
	5	4 — Register
	6	2
	7	1 (JK214)
2	0	128; (Write Gate)
	1	64; (Read Gate)
	2	32; Seek Start
	3	FBO 16; Rst Head Req
	4	8; (Erase Gate)
	5	4; Select Head
	6	2; Return to 000
	7	1; Head Advance (JK311)
3	0	
	1	
	2	
	3	FDR — File
	4	— Data
	5	— Register
	6	
	7	(JK411-412)

Byte	Bit	FERR - 26 (IFA Only)		
0	0		CC Hardware Error	JL015
	1		Track Overrun (Wr)	JL613
	2		Bus-Out Parity Check	JL611
	3	FSB	Serdes Check	JL013
	4		Data Check	JL811
	5		Data/Cmd Overrun	JL513
	6		Missing Addr Mark	JL014
	7		Write Current Error	JL611
1	0		Command Overrun	JL513
	1		Erase Gate	JL412
	2		High Compare }	JL215
	3	FGT	Low Compare }	
	4		Error Timeout	JL611
	5		Selected Gated Attn	JL811
	6		Contingent Connect	JK513
	7		Spare	
2	0		Test Sel Sw 0	
	1		Test Sel Sw 1	
	2		Test Sel Sw 2	
	3	FTS	Test Sel Sw 3	
	4		CE Error Disable	
	5		CE Mode Latch JL514	
	6		Allow CE Mode Sw	
	7		Gated Attn Spare WF101 (FE110)	
3	0		Gated Attention 7	(FAT ext has, in addition to attention usage, a multiple use in diagnostic mode. FBO bits 5,6,and 7 gate the diagnostic assembler.)
	1		Gated Attention 6	
	2		Gated Attention 5	
	3	FAT	Gated Attention 4	
	4		Gated Attention 3	
	5		Gated Attention 2	
	6		Gated Attention 1	
	7		Gated Attention 0	(JL814)

FAT - DIAGNOSTIC USAGE

Diagnostic Address 0

0	No-Op	JL314
1	Read Data Op	
2	Write Data Op	
3	Write Gap Op	
4	Compare Read Data	JL215
5	Read Buffer 0	JL012
6	Read Buffer 7	
7	Serial Data	JL014

Diagnostic Address 1

0	Counter Pos 128	JL112
1	Counter Pos 64	
2	Counter Pos 32	
3	Counter Pos 16	
4	Counter Pos 8	JL111
5	Counter Pos 4	
6	Counter Pos 2	
7	Counter Pos 1	

Diagnostic Address 2

0	Count 0 Gate	JL116
1	Count Decode 1	
2	Count Decode 2	
3	Count Decode 3	
4	Count Decode 7	
5	BCA Time	JL216
6	Data Gate	JL117
7	Orientation Latch	JL014

Diagnostic Address 3

0	Count Decode 20	JL116
1	Count Decode 21	
2	Count Decode 22	
3	Count Decode 23	
4	Count Decode 24	
5	Count Decode 25	
6	Count Decode 26	
7	Count Decode 15	

Diagnostic Address 4

0	Read Gate	JL412
1	Write Gate	
2	Wr Clock Gate	
3	Standard Index	JL411
4	Block Clock Bits	JL313
5	Serialized Data	
6	Write Sync Gate	JL117
7	Write Zero	

Diagnostic Address 5

0	Bit Ring 3	JL312
1	CC Register Pos 0	JL211
2	CC Register Pos 15	JL212
3	BCA Position 1	JL213
4	BCA Position 128	
5	Address Mark 1	JL413
6	Read Sync Gate	
7	Head Condition	JL411

Diagnostic Address 6

0	IFA High Trap Req	JL611
1	IFA Low Trap Req	JL612
2	Force Trap Bit-4	
3	Force Trap Bit-5	
4	Error Timeout	JL612
5	Control Tag A	JL512
6	Spare	
7	Spare	

Byte	Bit	CKCPT - 27
0	0-7	CKCPTO Bits 0-7
1	0-7	CKCPT1 Bits 8-15
2	0 1 2 3 4 5 6 7	CKCPT2 Bits 16-19 Not Used
3	0 1 2 3 4 5 6 7	CKC Submask PT Submask Error Bit CKCPT3 Manual Mode Control CKC Interrupt Bits PT Interrupt Update Latch Not Used (CCxxx)

Byte	Bit	TLB - 2E
0	0-7	VA Bits 0-7
1	0 1 2 3 4 5 6 7	VA Bits 8-12 Not Used (MT311-344)
2	0 1 2 3 4 5 6 7	RA Bits 0-7
3	0 1 2 3 4 5 6 7	RA Bits 8-12 Not Used (MT111-132)

Byte	Bit	TODH - 36
0	0-7	TODHO Bits 0-7
1	0-7	TODHI Bits 8-15
2	0-7	TODH2 Bits 16-23
3	0-7	TODH3 Bits 24-31 CT211-CT317

Byte	Bit	TODL - 3E
0	0-7	TODL0 Bits 32-39
1	0-7	TODL1 Bits 40-47
2	0-3	TODL2 Bits 48-51
	4 5 6 7	Not Used (CT211-CT317)
3	0 1 2	Spare
	3	TODL2 Microprogram Patch (CT317)
	4 5 6 7	Spare

EXPANDED LOCAL STORAGE MAP

NOTE: Expanded local storage may be altered from the printer keyboard with the CE key on.

EXPLS	Word Name	Byte 0	Byte 1	Byte 2	Byte 3	X and Y Line
50	I	Key		I-Register		X2 Y0
51	V			V-Register		X2 Y1
52	W			W-Register		X2 Y2
53	U			U-Register		X2 Y3
54	IBU			IBU-Register		X2 Y4
55	TR			TR-Register		X2 Y5
56	ICS	I-Cycle Control Display				X2 Y6
		57 through 5F unassigned				
60	G2DRL		DATA ADDR (SX 2)			X4 Y0
61	G2DBRL		BACKUP DATA ADDR			X4 Y1
62						X4 Y2
63						X4 Y3
64	G3DRL		DATA ADDR (SX 3)			X4 Y4
65	G3DBRL		BACKUP DATA ADDR			X4 Y5
66						X4 Y6
67						X4 Y7
68	G1DRL		DATA ADDR (SX 1)			X5 Y0
69	G1DBRL		BACKUP DATA ADDR			X5 Y1
6A						X5 Y2
6B						X5 Y3
6C	G4DRL		DATA ADDR (SX 4)			X5 Y4
6D	G4DBRL		BACKUP DATA ADDR			X5 Y5
6E						X5 Y6
6F						X5 Y7
		70 through 77 unassigned				
78	SN					X7 Y0
79	PN					X7 Y1
7A	WK		Working Register			X7 Y2
7B	NP	PAA byte 1,2	Latched	Control	Control	X7 Y3
7C	DK			Real Addr Reg		X7 Y4
7D	SS					X7 Y5
7E						X7 Y6
7F						X7 Y7

NOTE: Mode register bit 1 must be on to display EXPLS.

LOCAL STORAGE

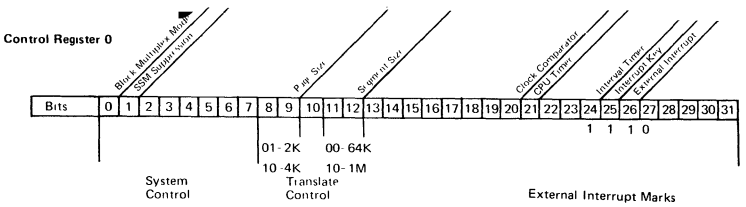
Word Name	LS Location	Byte 0	Byte 1	Byte 2	Byte 3	X and Y Line
	00		General Register 0			X0 Y0
	01		General Register 1			X0 Y1
	02		General Register 2			X0 Y2
	03		General Register 3			X0 Y3
	04		General Register 4			X0 Y4
	05		General Register 5			X0 Y5
	06		General Register 6			X0 Y6
	07		General Register 7			X0 Y7
	08		General Register 8			X1 Y0
	09		General Register 9			X1 Y1
	0A		General Register A			X1 Y2
	0B		General Register B			X1 Y3
	0C		General Register C			X1 Y4
	0D		General Register D			X1 Y5
	0E		General Register E			X1 Y6
	0F		General Register F			X1 Y7
AX	10		SRTN Temp Link			X2 Y0
DI	11		Alter/Display Log Link			X2 Y1
RTX	12		Retry Link			X2 Y2
DTX	13		Translate Link			X2 Y3
X	14		Working			X2 Y4
R	15		Working			X2 Y5
Y	16		Working			X2 Y6
Q	17		Working			X2 Y7
MA	18					X3 Y0
MBS	19					X3 Y1
MX	1A					X3 Y2
MC	1B					X3 Y3
MD	1C					X3 Y4
MF	1D					X3 Y5
MW	1E					X3 Y6
CX	1F	CPU	Link	Register		X3 Y7

LOCAL STORAGE (Continued)

	Word Name	IFA Name	LS Location	Byte 0	Byte 1	Byte 2	Byte 3	X and Y Line
SX 2	GD		20					X4 Y0
	GC		21				Count	X4 Y1
	GM		22		Protect CCW Address			X4 Y2
	GW		23					X4 Y3
SX 3	GD		24					X4 Y4
	GC		25				Count	X4 Y5
	GM		26		Protect CCW Address			X4 Y6
	GW		27					X4 Y7
SX 1	GD	FD	28					X5 Y0
	GC	FC	29				Count	X5 Y1
	GM	FM	2A		Protect CCW Address			X5 Y2
	GW	FW	2B					X5 Y3
SX 4	GD	FA	2C					X5 Y4
	GC	FB	2D				Count	X5 Y5
	GM	FS	2E		Protect CCW Address			X5 Y6
	GW	FL	2F					X5 Y7
			30		Floating-Point Register 0			X6 Y0
			31		Floating-Point Register 0			X6 Y1
			32		Floating-Point Register 2			X6 Y2
			33		Floating-Point Register 2			X6 Y3
			34		Floating-Point Register 4			X6 Y4
			35		Floating-Point Register 4			X6 Y5
			36		Floating-Point Register 6			X6 Y6
			37		Floating-Point Register 6			X6 Y7
	SO		38					X7 Y0
	PM		39		P E Control P.E Code Group Alter Mask			X7 Y1
	DM		3A		Adjustment Factor			X7 Y2
	RW		3B		Address Adjustment Working			X7 Y3
	DP		3C		IFA Low-Priority Link			X7 Y4
	LNK		3D		I-Cycle Link			X7 Y5
	P4X		3E		SX-4 Link Register			X7 Y6
	P3X		3F		SX-1, 2, 3, Link Register			X7 Y7

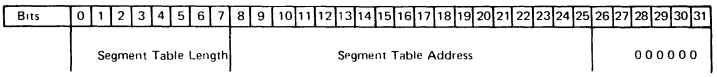
Note Words 28 through 2F are shown with Selector Channel designations.

Control Register 0



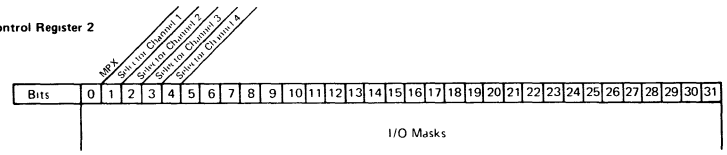
Reset to 00 00 00 E0

Control Register 1

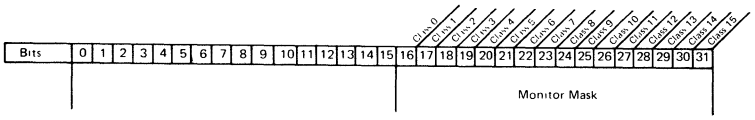


Reset to 00 00 00 00

Control Register 2

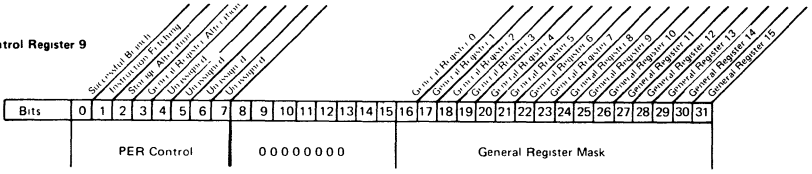


Control Register 8

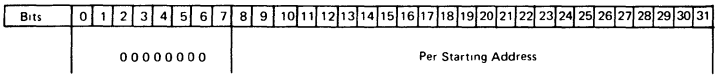


Reset to 00 00 00 00

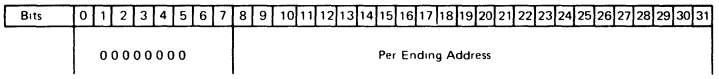
Control Register 9



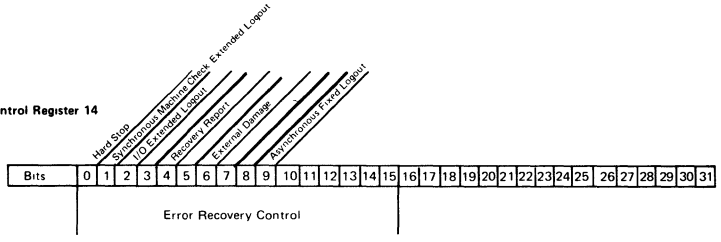
Control Register 10



Control Register 11

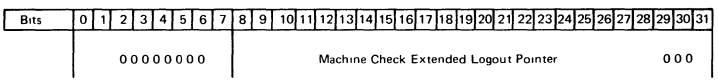


Control Register 14



Reset to C2 00 00 00

Control Register 15



Reset to 00 200 Hex

Control Register Assignments

	0	8	16	24	31
0	Sys Ctrl	XLate Ctrl	Ext Intp Masks		
1	Seg Tb L	Segment Table Origin Addr			
2	I/O Mask				
3	Reserved				
4	Reserved				
5	Reserved				
6	Unassigned				
7	Unassigned				
8	Monitor Mask				
9	Per Ctrl	00000000	Per GR Alt Mask		
10	00000000	PER Starting Address			
11	00000000	PER Ending Address			
12	Unassigned				
13	Unassigned				
14	Error Recov Ctrl				
15	00000000	MCEL Address			

Control registers are located in control storage locations F480-F4BC

Class	Code	Interrupt Address BC	Interrupt Address EC	Function
External	1005	1A	86	CPU Timer
	1004			Clock Comparator
	0040			External Interrupt Key
	0080			Interval Timer
	*00XX			Direct Control
Supervisor Call	**XXXX	22	8A	
Program	01-0F	2A	8E	(See System/360 Principles of Operation)
	10			Segment Translation Exception
	11			Page Translation Exception
	12			Translation Specification
	40			Monitor Call
	80			#PER
Machine Check		EA	EA	See Error Handling (Machine Check Logout)
I/O	***XXXX	3A	BA	

*Code is bit significant by External interrupt signals

**Code is dependent on the I-field of the supervisor call instruction

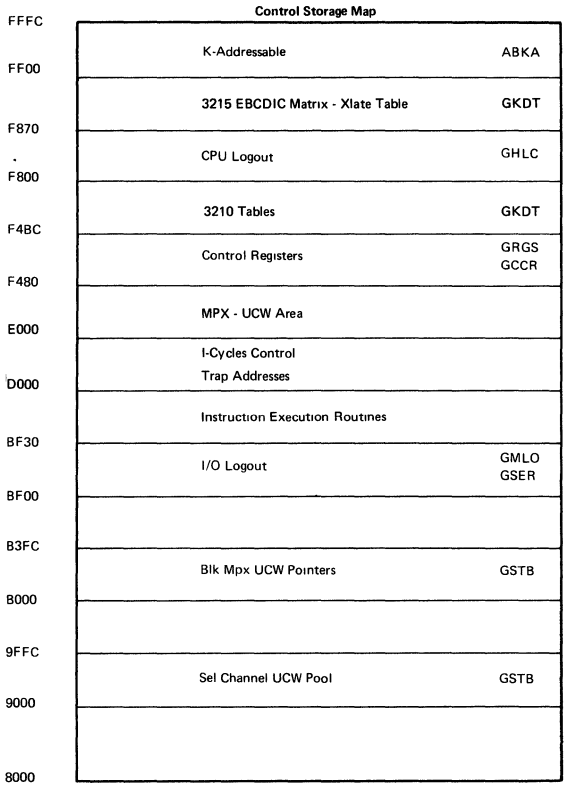
***Code is dependent on I/O device address

#PER interrupt concurrent with another program interrupt or 80 with another interrupt code to yield resultant interrupt code.

Dec	Hex	Permanent Storage Assignment
0	00	Init Prog Load PSW or PSW Restart New PSW
8	08	
16	10	Init Prog Load CCW 1 or PSW Restart Old PSW
24	18	Init Prog Load CCW 2
32	20	External Old PSW
40	28	Supervisor Call Old PSW
48	30	Program Old PSW
56	38	Machine Check Old PSW
64	40	Input/Output Old PSW
72	48	Channel Status Word
76	4C	Channel Address Word
80	50	Unassigned
84	54	Timer
88	58	Unassigned
96	60	External New PSW
104	68	Supervisor Call New PSW
112	70	Program New PSW
120	78	Machine Check New PSW
		Input/Output New PSW

Dec	Hex	Permanent Storage Assignment
128	80	Unassigned
132	84	0000000000000000 | Ext Int Code
136	88	0000000000000 | ILC | SCV Int Code
140	8C	0000000000000 | ILC | Prog Int Code
144	90	00000000 | Translation Exc Addr
148	94	00000000 | Mon C1 | No.PER Code | 00000000
152	98	00000000 | PER Prog Event Addr
156	9C	00000000 | Monitor Code
160	A0	Unassigned
164	A4	
168	A8	Channel ID
172	AC	00000000 | IOEL Pointer
176	B0	Limited Channel Logout (ECSW)
180	B4	Unit St | Chan St | Count
184	B8	Key | Flag | I/O Address
188	BC	CCW Address
192	C0	Unassigned
196	C4	
200	C8	
204	CC	
208	D0	
212	D4	
216	D8	Reserved
220	DC	
224	E0	Reserved
228	E4	
232	E8	Machine Check Int Code
236	EC	
240	F0	Unassigned
244	F4	
248	F8	00000000 | Failing Storage Addr
252	FC	Region Code
256	100	CPU Independent Logout

CONTROL STORAGE MAP



DIRECT ADDRESSABLE CONTROL STORAGE MAP

	0 1 2 3	4 5 6 7	8 9 A B	C D E F
0X	Misc Mach Definition	Misc Mach Definition	ACB Setting | First Ctrl Stg Addr	Last Main Storage Addr
1X				
2X			LEX List Pointer	
3X	Ex Instruction Ctr	Addr of First Inst RO		
4X	CPU Working	CPU Working	CPU Working	CPU Working
5X	CPU Working	CPU Working		
6X	Doc 1 Status Unaddr UCW Addr	Doc 1 Sense	Doc 2 Status Unaddr UCW Addr	Doc 2 Sense
7X	Timer Working Backup	Timer Working Backup	Timer Working Backup	Addr Contents Link
8X	Retry Return Word	Retry Counts and Marks	MCKA Reg Backup	MCKB Reg Backup
9X	ABRTY Reg Backup	SPTLB Reg Backup	HMRTY Reg Backup	CPURTY Reg Backup
AX	SX1 Cmd Retry or Integrated File Adapter	SX4 Cmd Retry or Integrated File Adapter	Integrated File Adapter	Integrated File Adapter
BX	SX2 Cmd Retry	SX3 Cmd Retry	Chan Interrupt Buffers	Chan Interrupt Buffers
CX	Retry Working	Retry Working	MCK Working	MCK Working
DX		Blk MPX | Blk MPX UCW Start	Blk End | MPX UCW Current	
EX				
FX	IFA Count Area 0	IFA Count Area 1	IFA Count Area 2	IFA Count Area 3

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