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Systems

DOS/VSE Linkage Editor Logic

Program Number 5745-SC-LNK

IBM

Summary of Amendments

Edition SY33-8556-3 documents:

Support of Fixed Block Architecture (FBA) disk devices

Fourth Edition (February, 1979)

This is a major revision of, and obsoletes SY33-8556-2 and Technical Newsletters SN33-8785 and SN33-9218.

This edition applies to the IBM Disk Operating System/Virtual Storage Extended, DOS/VSE, and to all subsequent releases until otherwise indicated. Changes are continually made to the information herein; before using this publication in connection with the operation of IBM systems, consult the latest IBM System/370 Bibliography, GC20-0001, for the editions that are applicable and current.

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PREFACE

This Program Logic Manual (PLM) is a guide to the IBM Disk Operating System/Virtual Storage Extended (DOS/VSE), Linkage Editor program. It supplements the program listings by providing descriptive texts and flowcharts.

For overall system control logic description, this PLM is to be used with six other PLMs:

DOS/VSE Supervisor Logic, SY33-8551

DOS/VSE Error Recovery and Recording Transients Logic, SY33-8552

DOS/VSE Logical Transients and Dump Phases Logic, SY33-8553

DOS/VSE System Serviceability Aids Logic, SY33-8554

DOS/VSE Initial Program Load and Job Control Logic SY33-8555

DOS/VSE Librarian Logic, SY33-8557

Publications that aid in the use of this manual are:

OS/VS, DOS/VSE and VM/370 Assembler Language, GC33-4010

Guide to DOS/VSE Assembler, GC33-4024

DOS/VSE System Control Statements, GC33-5376

DOS/VSE Operating Procedures, GC33-5378

Publications related to the subject of this manual are:

DOS/VSE System Management Guide, GC33-5371

DOS/VSE Data Management Concepts, GC24-5138

DOS/VSE Macro User's Guide, GC24-5139

DOS/VSE Macro Reference, GC24-5140

DOS/VSE System Generation, GC33-5377

DOS/VSE Messages, GC33-5379

DOS/VSE LIOCS Volume 1, SY33-8559

Titles and abstracts of the other related publications are listed in the IBM System/370 Bibliography, GC20-0001.

PUBLICATION ORGANIZATION

This manual consists of five major sections:

- Introduction to the Linkage Editor.
- Method of Operation, describing the program function, the structure of object modules as input, I/O flow and storage layout.
- Program Organization, describing in detail the library record formats, the control flow and various features of the program.
- General and detailed charts showing the logic flow of the linkage editor program. General charts are identified by two-digit numerals such as 01, detailed flowcharts by letters such as AA through ZZ.
- Appendixes which include a label list, phase-to-module and message cross references for use in analyzing program errors, a brief description of the system residence organization, and the linkage editor External Symbol Dictionary (ESD) processing and map.

In this publication, system and component names as listed below should be read as indicated:

System/component name	To be read as
DOS/VS	DOS/VSE (see Note below)

Note: Unless that name explicitly refers to DOS/VS Release 34 or an earlier DOS/VS release.

FIGURES

CHARTS

General Charts

Detail Charts

INTRODUCTION

All programs to be executed in the DOS/VS environment must be link-edited and stored in the core image library before they can be executed. The core image library is either on SYSRES (the system core image library) or on SYSCLB (a private core image library). The linkage editor program accomplishes the link edit function operating in one of three modes:

1. Catalog mode. An object module is link-edited and permanently stored in the core image library. The core image directory of cataloged phases is updated in this mode of operation.

2. Load and execute mode. An object module is link-edited for temporary storage in the core image library and is immediately executed.

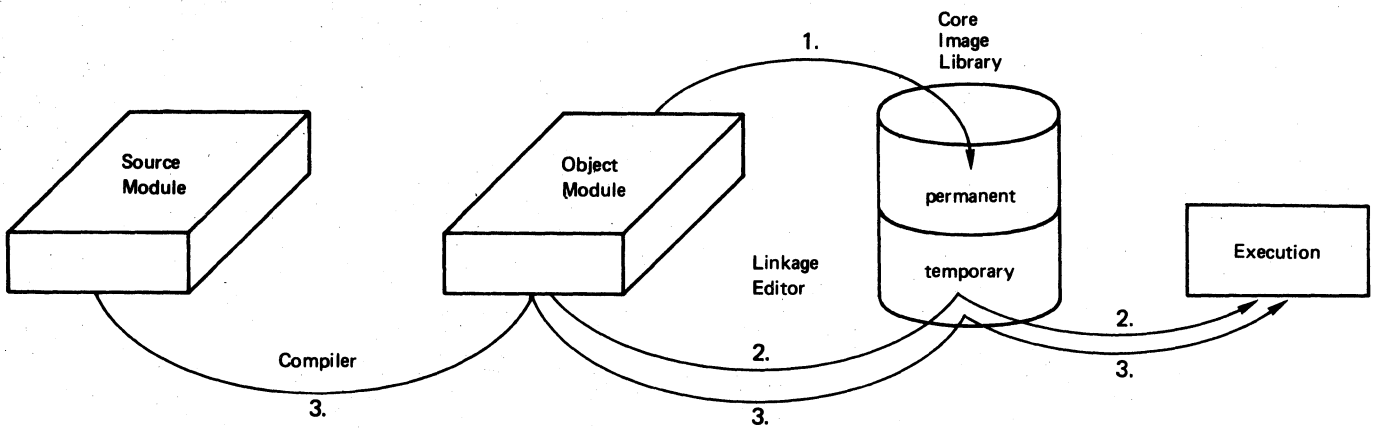
3. Assemble and execute mode. A source module is assembled or compiled. The object module (output) is link-edited for temporary storage in the core image library and is immediately executed.

Note: When operating in catalog mode, the core image directory for linked phases is updated. A reenterable program can be cataloged as eligible to be loaded into the shared virtual area (SVA eligible). Phases resident in the SVA can be shared concurrently by programs running in different partitions.

Job control calls the linkage editor program when a // EXEC LNKEDT control statement is read.

For updating the core image library directory, control is given to $MAINDIR. If OPTION CATAL was specified, the directory for cataloged phases is updated. If OPTION LINK was specified, the link area of the directory is updated. After either one of these functions is completed, control is returned to the linkage editor and then passed on to job control.

The linkage editor program can run in either the background or a foreground partition. If it runs in the foreground, you must assign a private core image library (SYSCLB). In the background partition, the linkage editor defaults to the system core image library if no private core image library is assigned. The linkage editor issues a diagnostic message and terminates abnormally when you assign the private core image library across partitions.



PROGRAM FUNCTION

The linkage editor prepares programs for execution on DOS/VS. Input for the linkage editor are the relocatable modules produced by the language translators. The linkage editor processes these modules into program phases which may be immediately executed or cataloged into the core image library.

The linkage editor control cards direct the program to read an input module(s) and to form phases from the control section within the modules. Figure 1 shows how phases can be formed. The linkage editor relocates the origin of each control section in the phase, assigns each phase an area of storage and a transfer address, and modifies the contents of the address constants in the phase.

Sample of a 2-module input resulting in a 3-phase output

Language Translator Output	Linkage Editor Output
Module A	Phase 1
ESDs TXT-CSECTA TXT-CSECTB TXT-CSECTC RLDs	CSECTA CSECTB
Module B	Phase 2
ESDs TXT-CSECTD TXT-CSECTE TXT-CSECTF TXT-CSECTG RLDs	CSECTC CSECTD CSECTE
	Phase 3
	CSECTF CSECTG

Figure 1. Example of a Module-Phase Relationship

The relocation factor for each control section is determined and saved by building a table called the control dictionary. This table contains the linkage editor phase definitions and the module ESD items. When complete, the table provides sufficient information for determining the location of each control section and for resolving any references between control sections.

The module TXT items are then built into phase blocks. The RLD items (address constants) are modified and inserted into the text. A transfer address is determined for each phase. Unresolved address constants will appear as zero RLD items in relocatable phases.
The linkage editor will also accept as input phases retrieved by the CSERV program from the core image library. The purpose of this function is to allow recataloging of an already link-edited phase to a different core image library.

OBJECT MODULES AS INPUT

The input to the linkage editor consists of object modules and linkage editor control cards. Each module is the output of a complete language translator run. It consists of dictionaries and text for one or more control sections.

The dictionaries contain the information necessary for the linkage editor to resolve references between different modules. The text consists of the actual instructions and data fields of the module.

Six card types can be produced, by the language translators or by the programmer, to form a module. They appear in the following order:

Card Type	Definition
ESD	External symbol dictionary
SYM	Ignored by linkage editor
TXT	Text
RLD	Relocation list dictionary
REP	Replacement to text made by the programmer
END	End of module

The external symbol dictionary contains control section definitions and intermodule references. When the linkage editor has the ESDs from all modules, it can relocate the sections and resolve the references. Five types of entries are defined in the control dictionary.

ESD Type	Definition
SD	Section definition: provides control section name, assembled origin and length. Generated by a named START or a named CSECT in a source module.
WX	Generated by Weak External Reference (WXTRN), which has a function similar to EXTRN, except that WXTRN suppresses AUTOLINK. The linkage editor treats WX as an ER, NOAUTO.
PC	Private code: provides assembled origin and length for an unnamed control section.
LD/LR	Label definition: specifies the assembled address and the associated SD of a label that may be referred to by another module. The LD entry is termed LR (Label Reference) when the entry is matched to an ER entry.
ER	External reference: specifies the location of a reference made to another module. ER is generated by EXTRN or a V-type address constant in a source module.
CM	Common: indicates the amount of main storage to be reserved for common use by different phases. CM is generated by CCM in a source module.

The relocation list dictionary identifies portions of text that must be modified on relocation (address constants).

When the linkage editor reads a module, it stores ESDs in its control dictionary, writes TXT and REP items in core image blocks in the library, and writes RLD items on an RLD file. Each item that is identified by the language translators with an ESID number is re-identified by the linkage editor with a control dictionary number to avoid duplication of identification between modules. For the ESD processing, see Appendix E.

I/O FLOW

The I/O flow for the linkage editor program consists of:

- Input from:

  SYSLNK - the system link library
  SYSRLB - a private relocatable library
  SYSRES - the system relocatable library on SYSRES
  SYS001 - the I/O Workfile

- Output to:

  SYSLST - the list device
  SYSLOG - the logging device
  SYSRES - the system CIL on SYSRES
  SYSCLB - a private core image library

Figure 2 shows the I/O flow of the linkage editor.

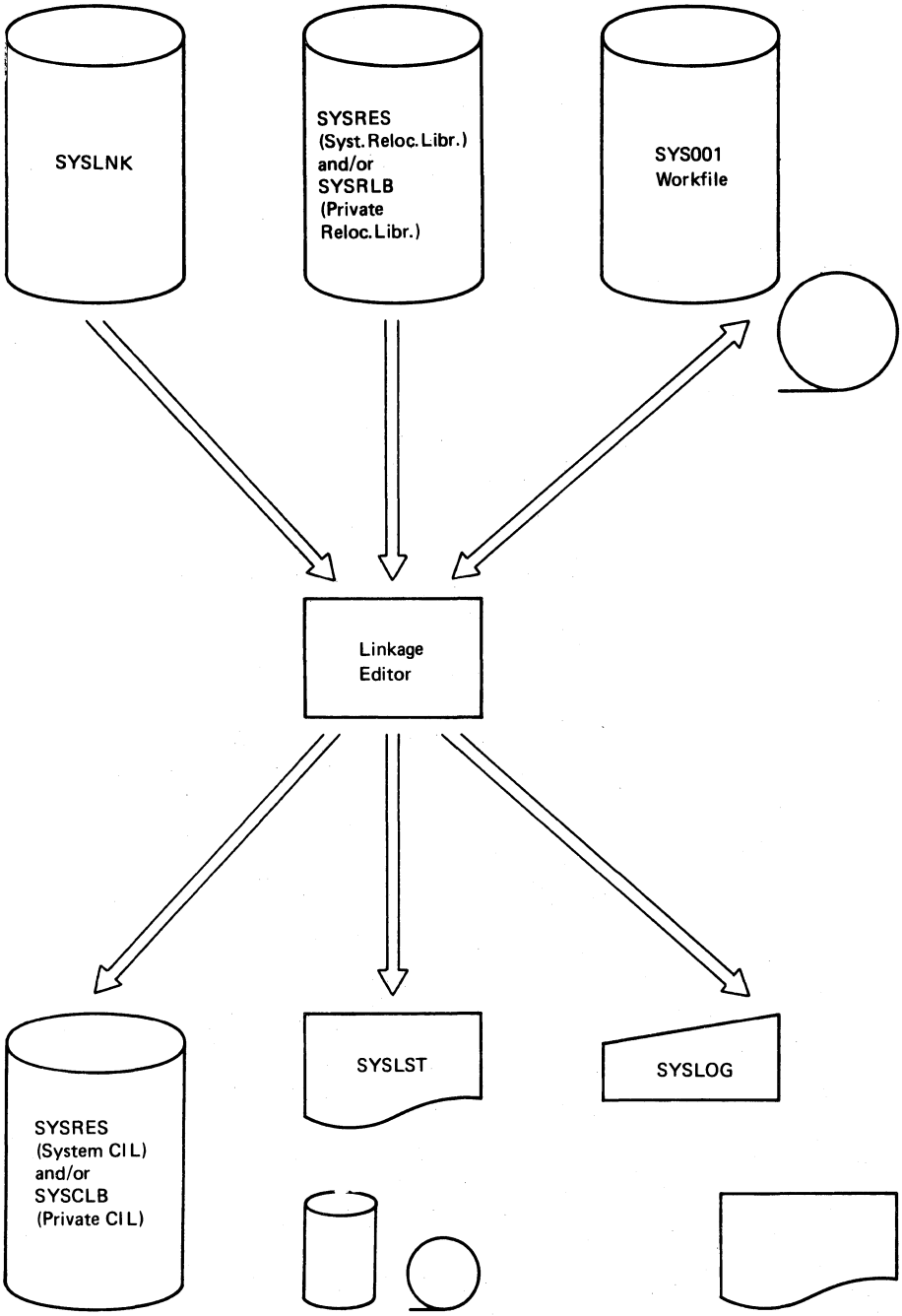


Figure 2. Linkage Editor I/O Flow

STORAGE LAYOUT

Addresses in Col. "Start at approx." are relative to the beginning of partition.

Start at approx.	Addressed by	Description	Length approx.
0	IJBLNK	Part of linkage editor permanent in storage	19K
19K	IJBINL VCATND	INL-CSECT, used only during initialization, thereafter overlaid by I/O-areas	4K
		Aligned on 1K	
19K	AWKARE	I/O-area for core image lib	1K
		Aligned on 2K (page-boundary)	
20K	RLDIRAR1	2 I/O-areas for reading directory of	2K
22K	RLDIRAR2	relocatable library (used alternately)	2K
24K	IOAREA1	I/O-area for reading from SYS001	0,5K
		Aligned on 2K (page-boundary)	
26K-320 bytes		Save-area for 1 record of a member in the relocatable library (handling spanned records: already read part of the record is moved before the part being read by a new read-command)	320 bytes
26K	FRMBUF	I/O-area for reading member of relocatable library Also used as I/O-area during initialization (reading library descriptor records)	2K
28K	FLNBUF	I/O-area for reading from SYSLNK (default-size=1K, may be changed by user)	1K or ?K
29K	LTMINE	Workarea (called Linkage Table) for processing ESD-numbers during processing an object module (i.e. only till the next END card)	1200 bytes
		Will be overlaid by status-table when calling $LIBSTAT	13 bytes
30K +176 bytes	CDENT1	Workarea (called control dictionary) containing information about all phases and ESD-items. Size will vary, as big as necessary 20 bytes for each ESD-item 40 bytes for each phase	?
30K+?	CTLDAD	Workarea (called stowtable) containing information about all phases as interface table for $MAINDIR or $MAINDIF. Size will vary, max. 2K 12 bytes for control-information 30 bytes for each phase	?
30K+?	WRKMAIN	Workarea used by $MAINDIR or $MAINDIF (approx. 24K, for exact value consult $MAINDIR or $MAINDIF)	24K
54K+?		END OF USED STORAGE	

When calling $LIBSTAT overlaying at

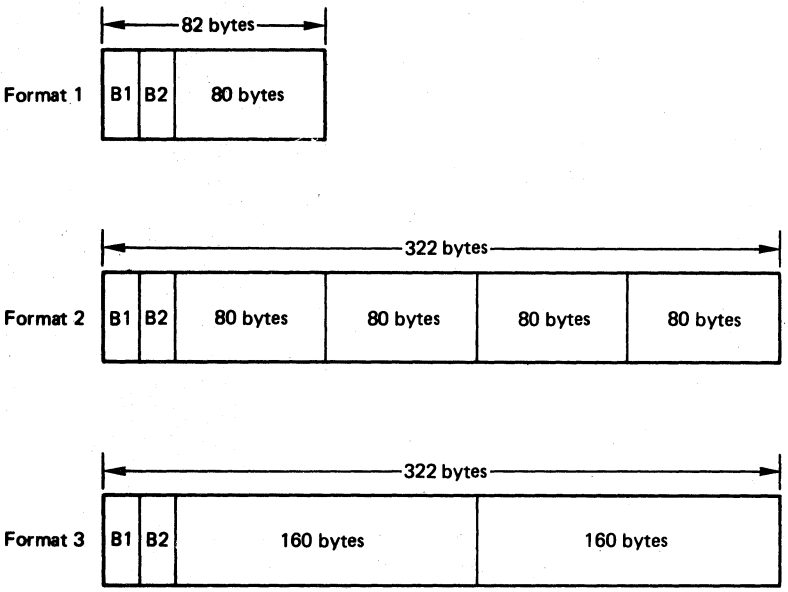
29K	LTMINE	Workarea (called status-table) as interface for $LIBSTAT	13 bytes
19K+ 16 bytes		Workarea used by $LIBSTAT (approx. 4K, for exact value consult $LIBSTAT)	4K

PROGRAM ORGANIZATION

LIBRARY FORMATS

SYSLNK AND RELOCATABLE LIBRARIES

The Linkage Editor reads data from SYSLNK in three different formats (format 1, 2 and 3) and from the Relocatable Library in a unique format (format 3).



B1 (1 byte) – Number of records per block (either 1, 2 or 4)
B2 (1 byte) – Record length (either 80 or 160)

Figure 3. Block Format on SYSLNK and Relocatable Library

Format 3 is the only one accepted from the Relocatable Library. (Refer to the DOS/VS Librarian Logic for a detailed description.)

The Linkage Editor recognizes different item types (ESD, TXT, RLD, REP, END). Only one item type can be contained in each individual record.

The Linkage Editor control statements ACTION, INCLUDE, ENTRY and PHASE each occupy a complete block, i.e. only one record per block will be accepted.

For a private relocatable library, Figure 4 shows an example of a logical block consisting of a set of physical blocks.

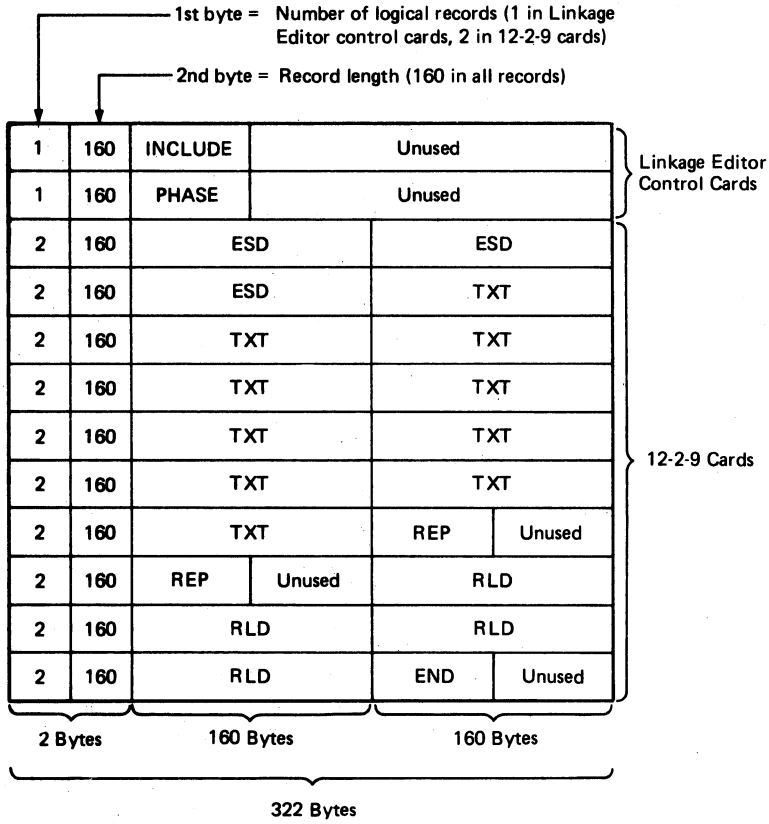


Figure 4. Example of a logical block on SYSRLB

Physical Description of SYSLNK and Relocatable Libraries

For CKD devices, the physical record is identical with the logical block. For FBA devices, this is not true. For the FBA records of SYSLNK, the SAM format is used. The control interval is 1K by default. The user may change this value by specifying a different size in the EXTENT card.

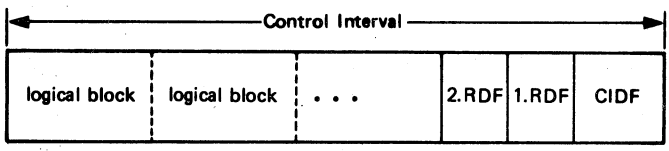


Figure 5. SAM-Format for SYSLNK on FBA

CIDF Control interval definition field (4 bytes; first two bytes containing address of free space, last two bytes containing length of free space)

RDF Record definition field (3 bytes)

1. RDF: 1. Byte: bit 1=0 only 1 block
   bit 1=1 (X'40')
   more than one block in this C.I.
   last two bytes: length of block

2. RDF: last two bytes: number of blocks in this C.I.

For the relocatable library on an FBA device, no special format is used. The first logical block of a member starts on a physical block boundary. The next logical blocks are written sequentially, regardless of 'physical block' boundaries ("spanned records", i.e. part of a logical may be in one physical block and the rest of it in the next physical block).

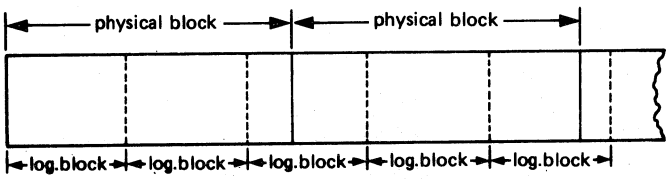


Figure 6. Spanned records for SYSRLB on FBA

CORE IMAGE LIBRARY

The logical record of the core image library has a size of 1024 bytes. It contains executable code and at the end of the phase some RLD information, whenever the phase is relocatable. For CKD devices, the records are unblocked and the physical record is the same as the logical record. For FBA devices with a blocksize of 512 bytes, the unit-of-transfer will always be two physical blocks = 1024 = one logical record.

WORKFILE SYS001

The logical record for the workfile SYS001 has a size of 240 bytes. In the first 16 bytes, it contains the standard information of a RLD card, in the rest, it contains the variable information of four RLD cards. For CKD devices, the records are unblocked and the physical record is the same as the logical record. For FBA devices, two logical records are blocked together in one physical block.

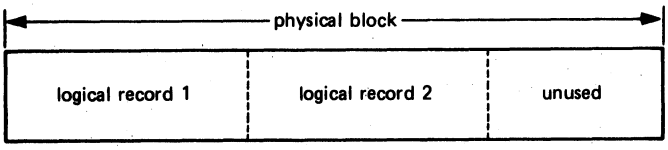


Figure 7. Blocked records for SYS001 on FBA

CONTROL FLOW

The linkage editor is a single phase program divided into ten CSECTs. The CSECT names and their functions are the following:

IJBINL Entry point for calling program, used for initialization and processing ACTION cards (afterwards overlaid by I/O-areas), (Chart 01).

IJBLNK Contains subroutines and constants, besides subroutine ALNKOF, which reads input and gives control to the appropriate CSECT (Chart 02). See also the chapter on subroutines.

IJBFIN Reads input, if SYSLNK or a Relocatable Library is on FBA (Chart 03).

IJBESD Processes ESD-cards (Charts 04, 05).

IJBOTH Processes TXT, REP, RLD, END-cards (Chart 06).

IJBSCN Processes INCLUDE, PHASE, ENTRY cards (Chart 07).

IJBCTL Post-processes PHASE, ENTRY cards (Chart 08).

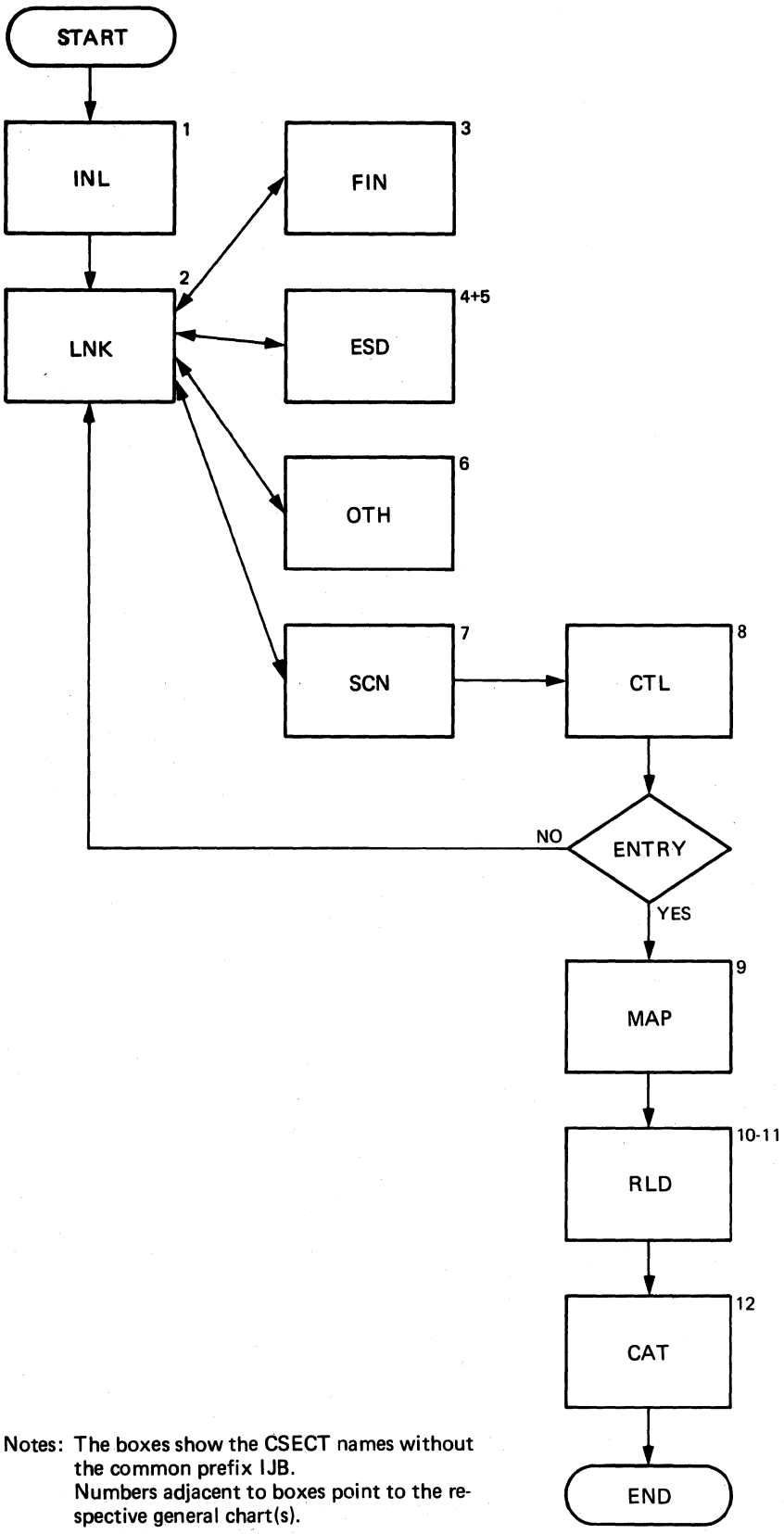
After ENTRY-card:

IJBMAP Prints linkage editor map (Chart 09) (Figure 19).

IJBRLD Processes RLD-items read from SYS001 (written by IJBOTH) (Charts 10, 11).

IJBCAT Updates directory of Core Image Library (calling $MAINDIR or MAINDIF). Prints status report (calling $LIBSTAT), returns to caller (Chart 12).

Figure 8 shows how these CSECTS are connected in the program.



Notes: The boxes show the CSECT names without the common prefix IJB.
Numbers adjacent to boxes point to the respective general chart(s).

Figure 8. Linkage Editor Control Flow

CONTROL DICTIONARY (CD)

The control dictionary is an internal linkage editor table used to store phase and external symbol dictionary (ESD) information. All information necessary for relocation is contained in the control dictionary.

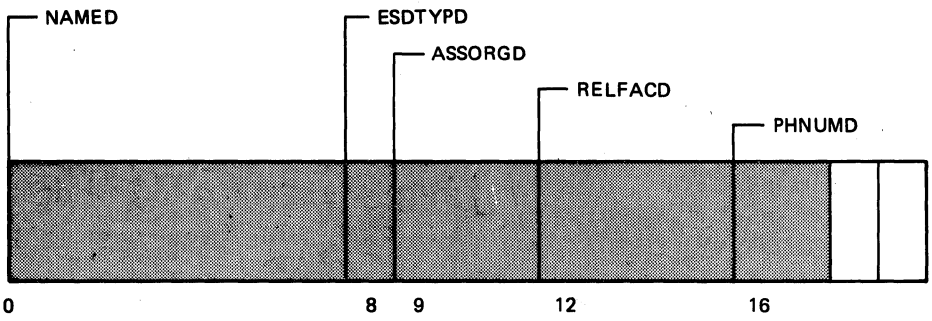
The control dictionary is composed of a variable number of 20- and 40-byte entries. Each phase entry is 40 bytes long and is handled as if it consisted of two 20-byte entries by the routines scanning the control dictionary (except for when it is scanned for a section definition entry). All other types of entries are 20 bytes long.

The control dictionary starts on the first fullword boundary after the linkage table. Location CDENTI contains the address of the first entry. Location CTLDAD contains the address of the last entry in the control dictionary. Refer to Figure 9 for the format of the control dictionary entries.

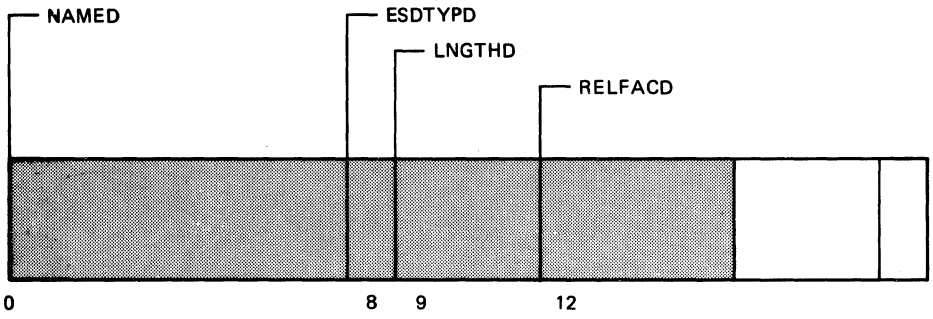
FORMAT OF CD ENTRIES

Layout of Control Dictionary entries for ESD items

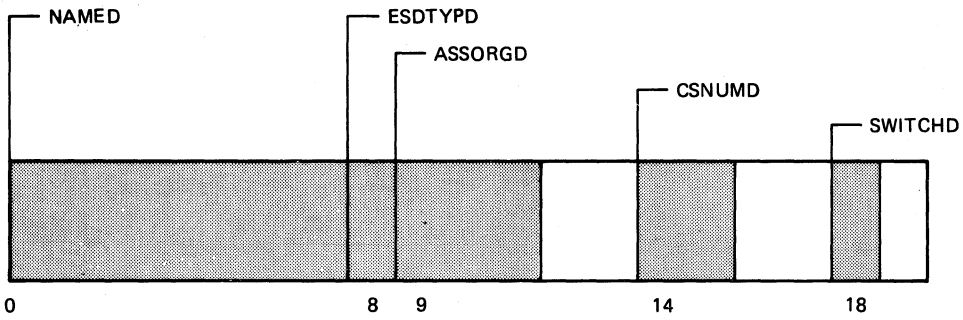
Type of ESD item:
(see section 'Object Modules as Input' above)



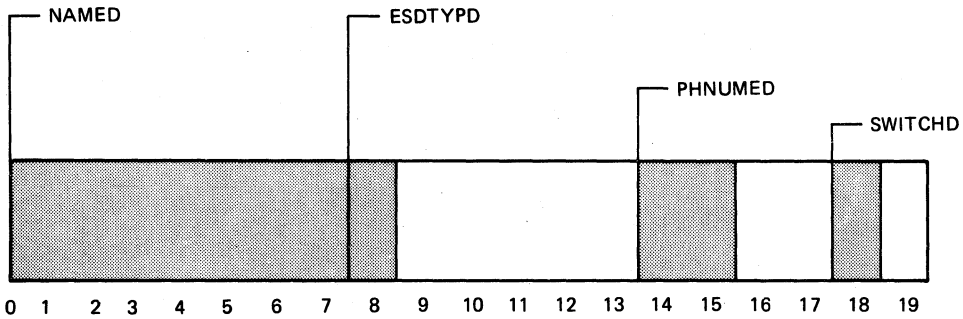
SD - section definition
or
PC - private code



CM - common storage



LD - label definition
or
LR - label record

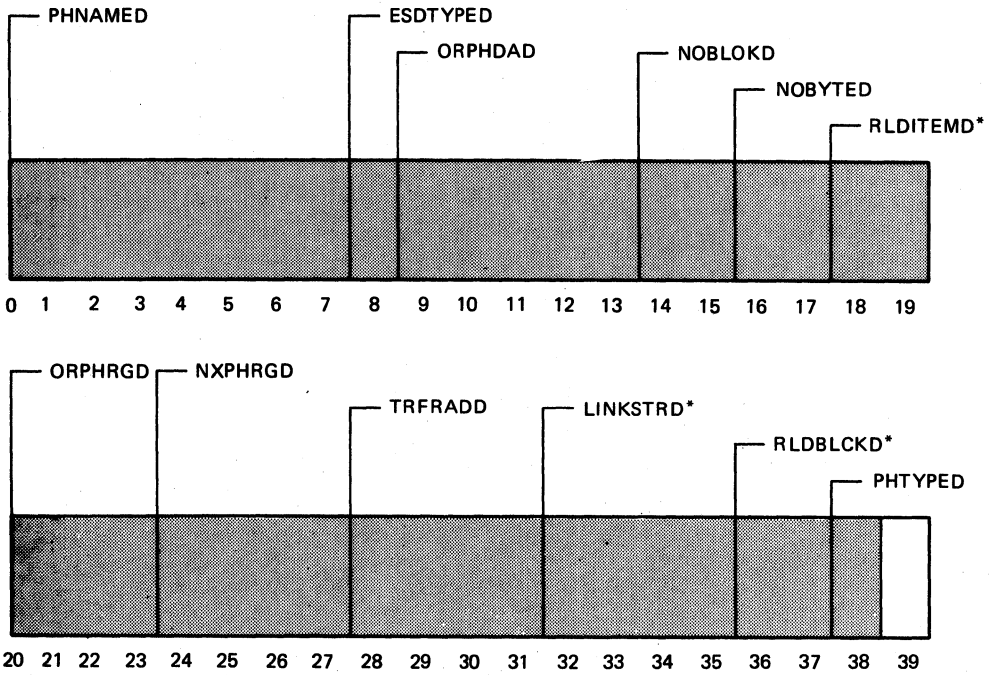


ER - external reference
or
WX - weak external reference

Byte 19 is reserved for future use.

Figure 9. Format of Control Dictionary Entries (Part 1 of 2)

Layout of Control Dictionary entries for a phase



Byte 39 is reserved for future use.
*Only used for relocatable phases. Otherwise the content is zero.

Figure 9. Format of Control Dictionary Entries (Part 2 of 2)

USE OF CD ENTRY FIELDS

Each control dictionary entry is first built in a fixed location in IJBLNK and is called "current entry". The current phase control dictionary entry starts at label CPHENT and the current ESD entry at label CESDENT. The current ESD entry is added to the control dictionary at label ELBINT in the ESD processor. The current phase entry is moved to the control dictionary at label MOVENTRY after the next phase card or the ENTRY card has been read.

In IJBMAP the location CPHENT is used to save a phase entry during a search for ESD entries belonging to the phase that is being processed. References to control dictionary information are sometimes to the current entry and sometimes to the control dictionary itself. Therefore, in the following description of the control dictionary fields, the name of the corresponding current field between parentheses is added to the control dictionary name of the field.

This CD Field	Contains
NAMED (NAME)	the name of the ESD item.
ESDTYPD (ESDTYP)	the type of ESD item. The representation of different ESD items is shown below.
ASSORGD (ASSORG)	the assembled origin of SD, PC, LD, or LR.
LNGTHD (LNGTH)	the length of the CM.
RELFACD (RELFAC)	• in the case of an SD or PC the relocation factor. The relocation factor is calculated by subtracting the assembled origin from the next possible phase origin NXPHRGD (NXPHRG). • in the case of a CM the absolute address of the next start of the CM.
CSNUMD (CSNUM)	a pointer to the SD or CM

containing the entry symbol of the LD or LR. If the SD or CM pointed to by an LD or LR has already been processed the LD or LR is called "assigned". If not, LD or LR is called "unassigned". In the case of an unassigned LD or LR this field contains the ESID number of the SD or CM as a pointer. In the case of an assigned LD or LR this field contains the control dictionary number of the SD or CM.

ESD Item	Representation
Section Definition (SD)	X'00'
Private Code (PC)	X'04'
Common (CM)	X'05'
Label Definition (LD)	X'01'
Label Reference (LR)	X'03'
External Reference (ER)	X'02'
Weak External (WX)	X'02'

PHNUMED (PHNUME) the phase number of the phase in which the ER or WX was encountered.

PHNUMD (PHNUM) the phase number of the phase containing the SD or PC.

SWITCHD (CSWITCH)

Bit	On	Off
0-4	Unused	
5*	No AUTOLINK necessary	AUTOLINK necessary
6	ER is a weak external	ER is a normal external reference
7	LD/LR unassigned	LD/LR assigned

*This bit is always set if bit 6 is on and also after AUTOLINK was not successful.

PHNAMED (PHNAMEC) the phase name.

ESDTYPED (ESDTYPC) X'07' to classify the control dictionary entry as a phase entry

ORPHDAD (ORPHDA) the disk address of the first text block of the phase in the format CCHHR for CKD devices. For FBA devices, the first four bytes contain the physical block number (relative to the device, not to the library); the fifth byte is unused.

NOBLOKD (NOBLOK) the number of text blocks.

NOBYTED (NOBYTE) the number of bytes in the last text block.

RLDITEMD (RLDITEMS) the number of RLD items.

ORPHRGD (ORPHRG) the load address of the phase. The first byte must be X'00' (see note below).

NXPHRGD (NXPHRG) the highest phase address. This field is initialized with the contents of ORPHRG. Every time an SD or PC is encountered the field NXPHRGD is aligned on a double word boundary and the length of the control section is added to it.

TRFRADD (TRFRAD) the transfer address of the phase. The first byte must be X'00' (see note below).

LINKSTRD (LINKSTRT) the starting address of the partition into which the program is link edited.

RLDBLCKD (RLDBLCKS) the number of extra RLD blocks. Extra RLD blocks must be added if, after the text of a relocatable phase, RLD information is stored for use by the relocating loader and the remaining space in the last text block is not sufficient.

PHTYPED (PHTYPE) an indication as to the type of phase.

Type of Phase	Representation
Self relocating	X'80'
Relocatable	X'40'
SVA eligible	X'20'
Not relocatable	X'00'

Note: Most of the routines scanning the control dictionary handle it as if it consisted of fixed length (20-byte) entries. The value X'00' in the first bytes of the ORPHRGD and TRFRADD fields, prevents the second half of a phase entry to be interpreted as an ESD entry since the displacements of ORPHRGD and TRFRADD correspond to those of NAMED and ESDTYPD. Because of the type mask X'00' for an SD, an exception has been made for routines searching the control dictionary for an SD.

LINKAGE TABLE

The linkage table is an internal linkage editor mechanism used to link the ESID number supplied by the language translator output to the corresponding control dictionary number that belongs to a control dictionary entry.

The linkage table is composed of a variable number of fixed 3-byte entries up to a maximum of 400. It is built separately for each object module. When an END card is processed, signalling the end of a module, the table is reset to zeros. Location LTMINE contains the address of the first item in the linkage table minus 3 bytes. LNKTAD contains the address of the last item in the linkage table plus 3 bytes.

Linkage Table

Control Dictionary Number	ESD Type
2 Bytes	1 Byte

USE OF THE LINKAGE TABLE AND CONTROL DICTIONARY

The linkage table is designed to associate text and RLD information with the proper relocation attribute from the control dictionary. The following steps are taken in processing text:

1. Get the ESID number and calculate the linkage table entry.
2. Go to the linkage table.
3. Extract the control dictionary number field of the linkage table, and calculate the control dictionary entry location.
4. Go to the control dictionary entry.
5. Extract the relocation factor.
6. Add the relocation factor to the assembled origin of the text to be loaded.
7. Substitute the result of the calculation in step 6 (the load origin) for the language translator supplied assembled origin (for the text).
8. Calculate the block of the core image library to which this text belongs (next available block).
9. Get the proper core image block.
10. Put the text into the core image block.

Note: If a TXT card on P-pointer points to a negative control dictionary number, that control section is skipped. If the R-pointer points to a negative control dictionary number, that control section is needed (CSECT is not in this phase in real storage).

THE AUTOLINK FEATURE

This feature tries to locate a module in the private (if assigned) and system relocatable libraries for any unresolved ERs found in the preceding phase. The signal that indicates a phase has finished processing is either a new phase card or an ENTRY card. When the signal is detected, autolink is attempted unless the feature has been suppressed by a NOAUTO phase card, action card option, or by WXTRN.

Examples of Autolink with LIOCS

Whenever a DTF macro is expanded during a language translator run, an ER is generated with a label corresponding to a label of a LIOCS module. The label of the ER is used as the search argument in autolink. The autolink processing searches first the private (if assigned), then the system relocatable directories for the corresponding label. The directory entry contains the disk address of the module in the relocatable libraries. The module is the macro expansion, and is then treated as an include statement.

Linkage Editor Fundamental Calculations: For the examples in this presentation:

- The symbol A/O represents the assembled origin.

- The symbol R/F represents the relocation factor.
- The symbol L/O represents the load origin.
- The symbol P/O represents the phase origin.

Example 1: The A/O provided by the language translator is added to an R/F determined by the phase origin information. If the phase is not relocated when it is loaded into main storage the result, the L/O, is the main storage address that is the physical location of this text, RLD item, or control section.

A/O + R/F = L/O

Example 2: The assembled origin of the CSECT being processed is subtracted from the address that is the next possible phase origin. This results in the relocation factor for that control section.

P/O - A/O = R/F

Example 3: The address of the next available control dictionary entry is calculated by adding the length of the last entry to the address of the last entry.

Example 4: The current linkage table entry plus 3 equals the next linkage table entry.

SUBROUTINES IN IJBLNK

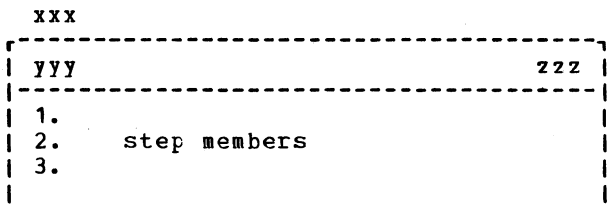
The first CSECT (IJBLNK) of the linkage editor program contains most of the subroutines used by other linkage editor CSECTs. After processing any of these subroutines, control is returned to the calling routine if not indicated otherwise. A list containing the subroutine names of this CSECT, the main entry points, descriptions of the routines' functions, and the appropriate flowcharts is shown below:

Sub-routine	Entry point	Function	Chart
RDS000	RDS000	Reads input from SYSLNK or the relocatable library.	AA
LTESID	LTESID	Note: Input to this routine is an ESID number supplied by the language translators. Inspects the control dictionary by taking the following actions: • If the control dictionary number is zero, the ESID number has not yet been processed. The routine then returns to the address in the link register. • If the control dictionary number is negative, the ESD item is bypassed and the routine returns to link register plus 4. Addresses of the linkage table entry and the control dictionary number are supplied. • If the control dictionary number is positive, the routine returns to register plus 8. Relocation factor (for SD/PC), control dictionary number and address of the control dictionary are supplied.	AB
SRCHCD	SRCHCD	Searches the control dictionary for a matching label.	AC
	SRPCOD	Entry at SRPCOD continues the search after a matching label has been found.	
CNVHEX	CNVHEX	Converts EBCDIC input to hexadecimal output.	AC
PRINT	PRINT	Prints messages and map onto SYSLST.	AD
LOGMSG	LOGMSG	Prints error message onto SYSLOG.	AD
PRTLST	PRTLST	Prepares for printing the linkage editor diagnostics of input.	AD
SPACE1	SPACE1	Spaces one line on SYSLST.	AD
AD1DSK	AD1DSK	Updates the disk address to the next record.	AE
UPDSKAD	UPDSKAD	Updates the disk address to the first record on the next track.	
XTPHNO	XTPHNO	Extracts the phase number from SD, PC, LD, or LR control dictionary entries.	AF
	XTPHGT	Entry XTPHGT is used if the entry is known to be a SD or PC.	

ABTERR	ABTERR	Gives control to IJBRLD for abnormal termination error handling.	AF
CDSIZE	CDSIZE	Checks for control dictionary overflow.	AF
WRITE	WRITE READC1	Reads or writes core image blocks.	AG
	DISKRDWR DISKIO	Executes the I/O by means of EXCP.	
	FDISKIO	Entry if I/O for FBA.	
ALNKPR	ALNKPR	Initializes for the scanning of the relocatable directory for AUTOLINK. Extracts unresolved ERs from the control dictionary in collating sequence. Gives control to the INCLUDE processor and, after the modules have been included, passes control to ALNKOF.	AG
ALNKOF	ALNKOF RDNEXT	Reads the input stream and diagnoses the type of card to pass control to the appropriate CSECT.	AH
	RDEXEC	Entry at RDEXEC skips reading of card.	
CANCL	CANCL	Cancel routine. If necessary, sets the new supervisor cataloged bit in COMREG off.	AH
ERROR	ERROR	Sets up to print non-termination error messages. If the calling routine sets the RETRN bit in ERRSW, the ERROR routine returns to the calling routine. If the RETRN bit is off, return is to RDNEXT or to ALNKPR if the error occurred during AUTOLINK.	AI
NOTCTL	NOTCTL	Converts input cards (containing 12-2-9 in the first column) to machine printable format.	AI
DERDAD	DERDAD	Provides a core image block containing a specified storage address for a work area. If the space in the work area is required for a next block, the current block is written back to the CIL.	AK

General Charts Conventions:

1. A unit of programming, routine, CSECT, or phase, is contained in one box like this:



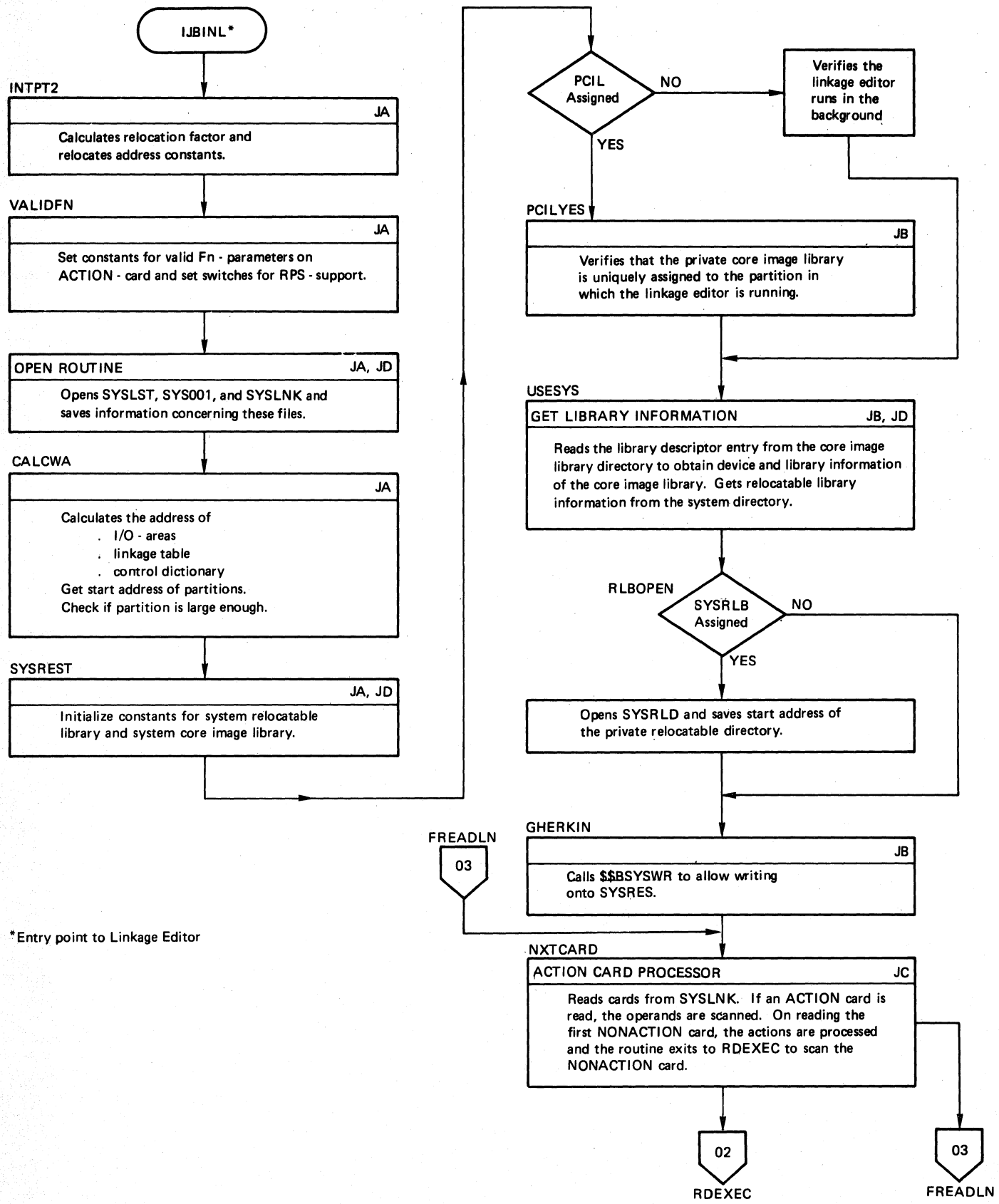
where: xxx marks the label and routine name
yyy says briefly what the routine does
zzz is the reference to the detail chart(s).
The step numbers are given from 1 to n within this routine only.

2. On-page connectors are such:

3. Off-page connectors are such:

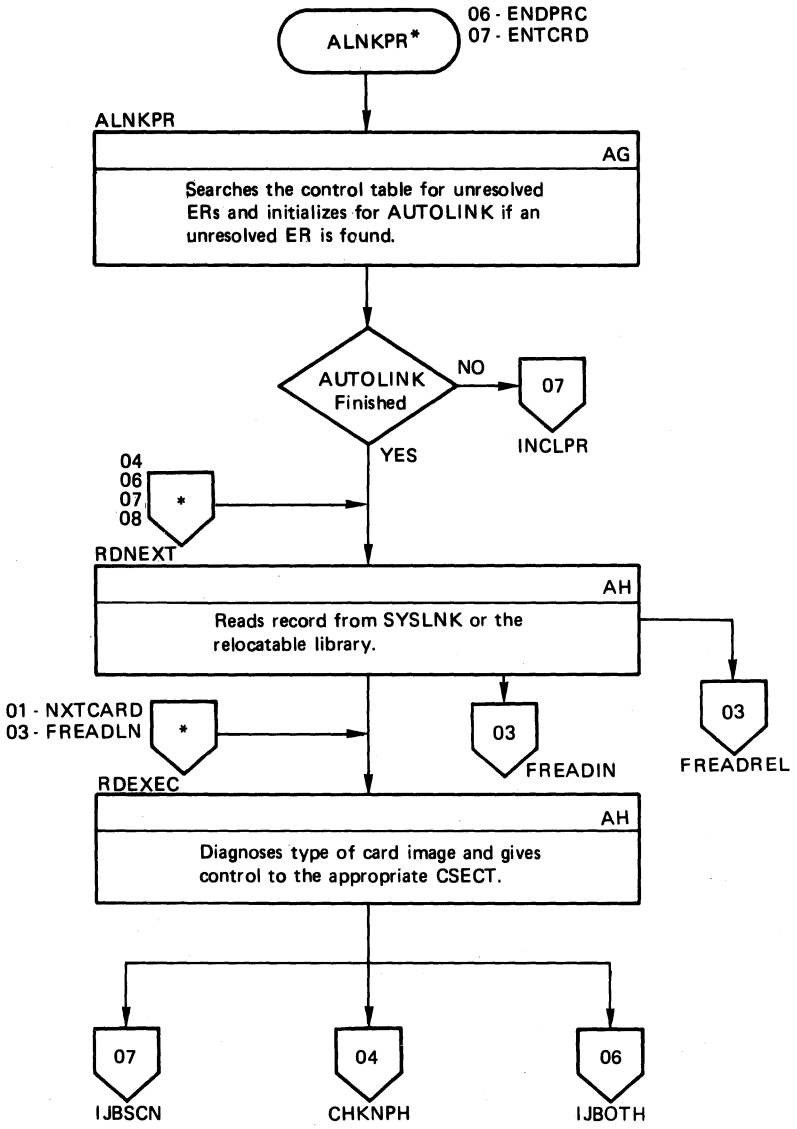
where: the number in the frame marks the chart from which we come or to which we go,
the word above (incoming) or below (outgoing) marks the label (routine) on that chart,
the number under the word marks the step within the routine to which we go if it is not step 1.

Chart 01. IJBINL and FBAINL Initialization



*Entry point to Linkage Editor

Chart 02. IJBLNK - Subroutines



Note: The flowcharts AA-AF and AJ-AK describe the less important subroutines.

Chart 03. IJBFIN - Processing FBA device input

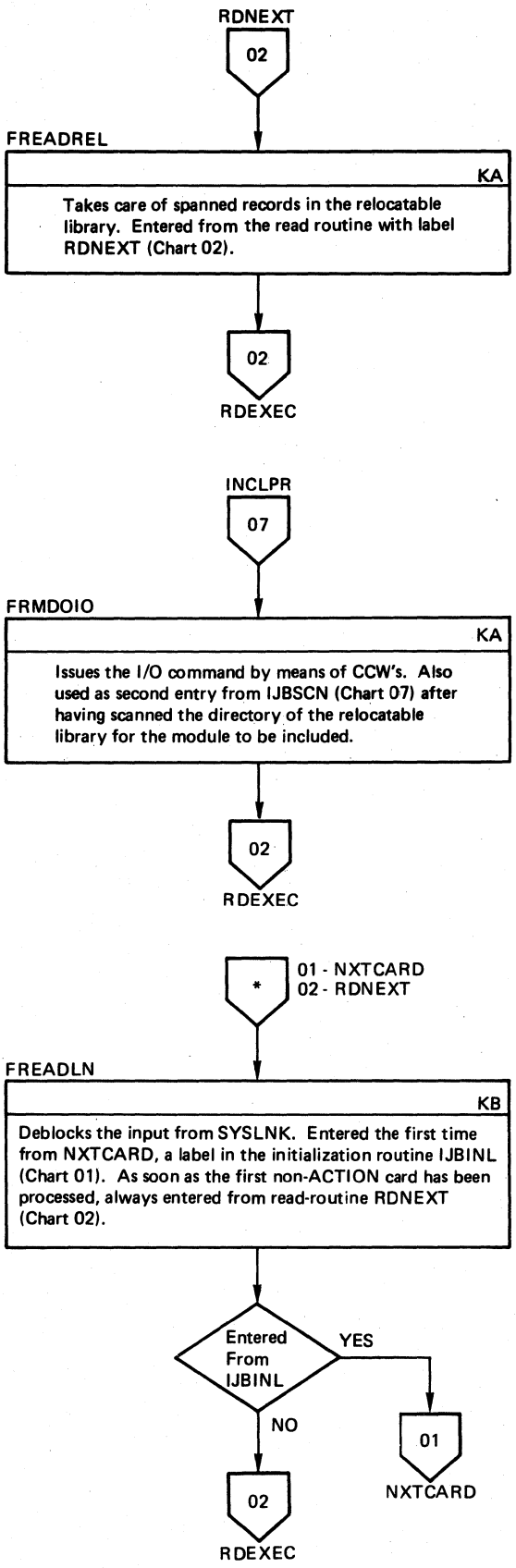


Chart 04. IJBESD - ESD Processing

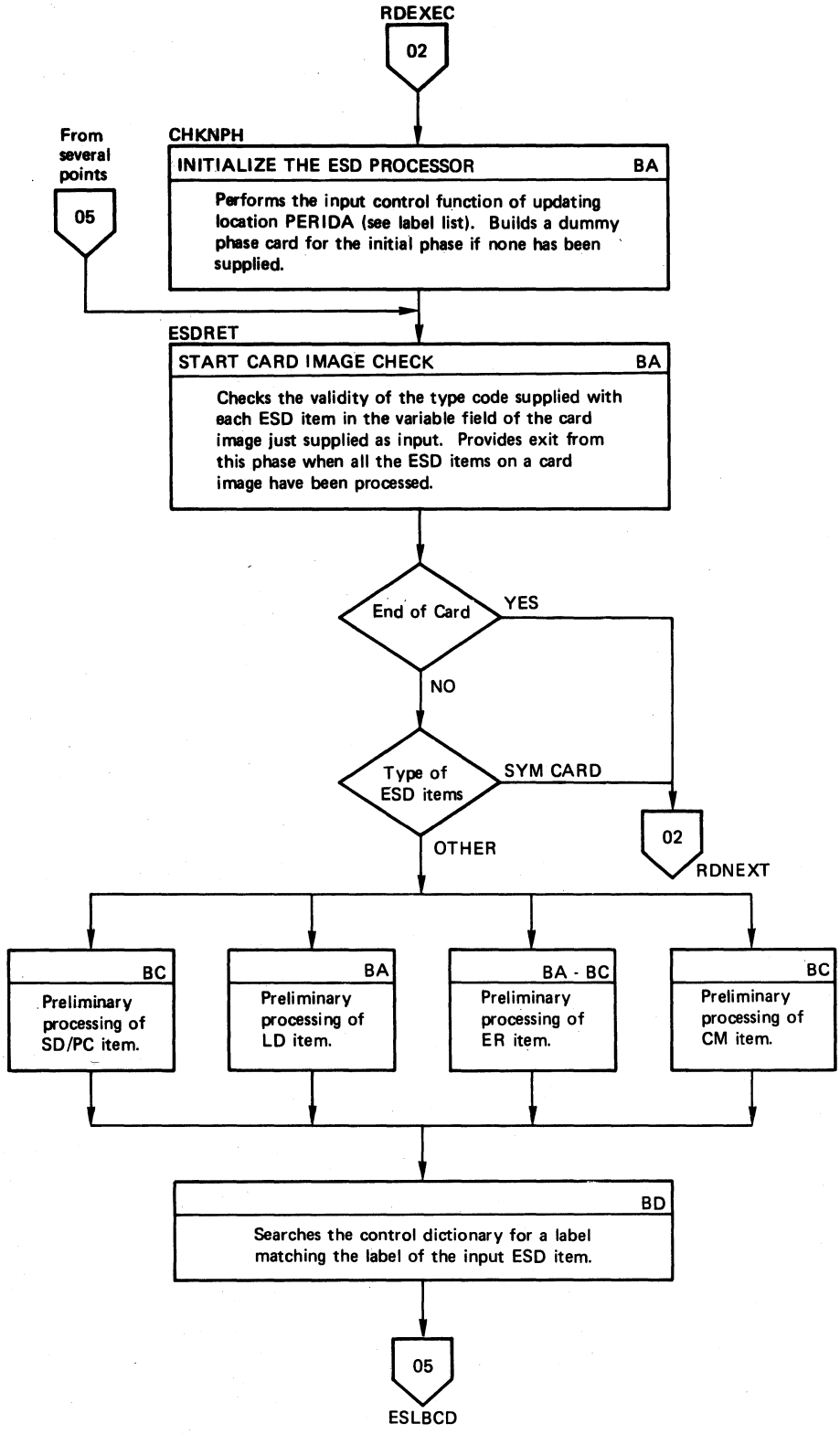


Chart 05. IJBESD - ESD Processing

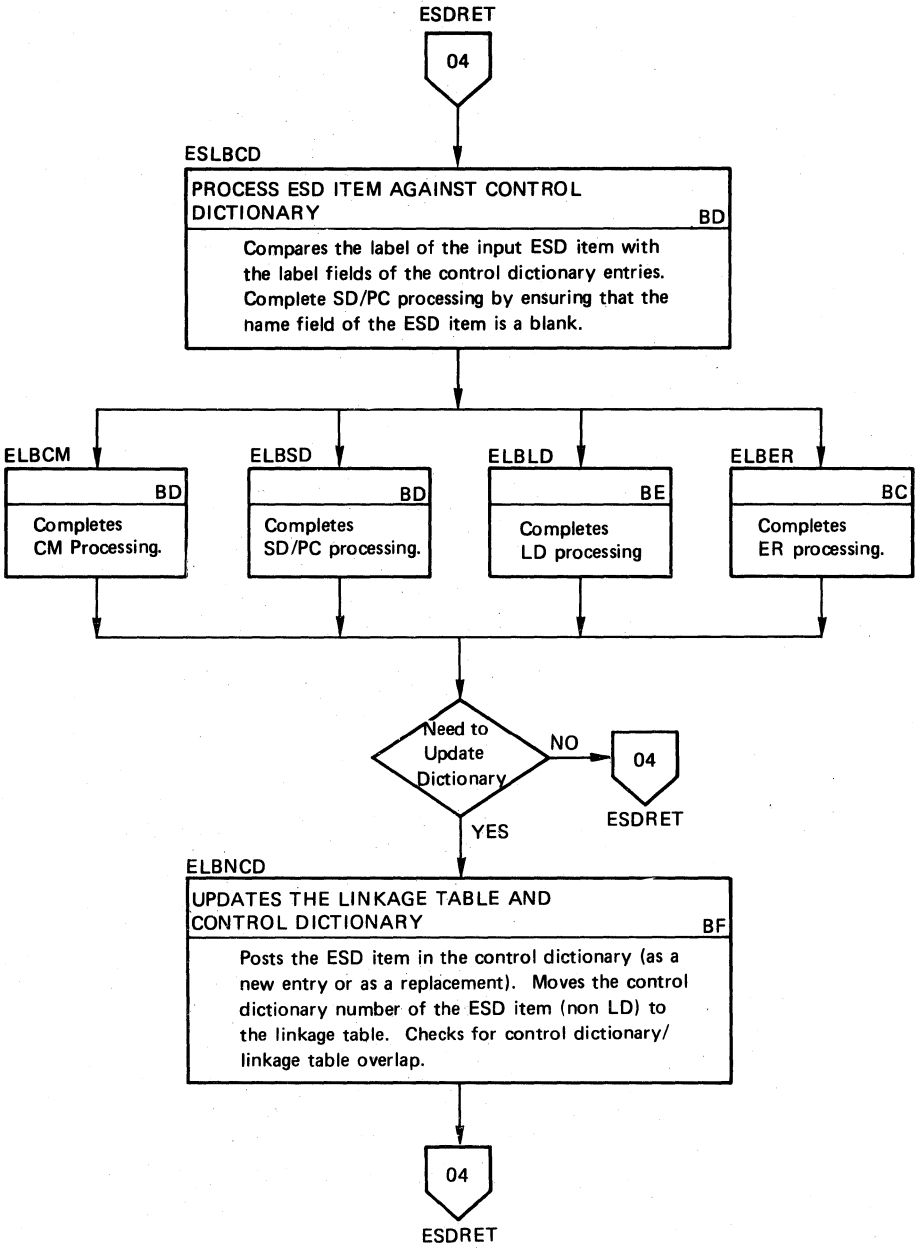


Chart 06. IJBOTH - TXT, REP, RLD, and END Processing

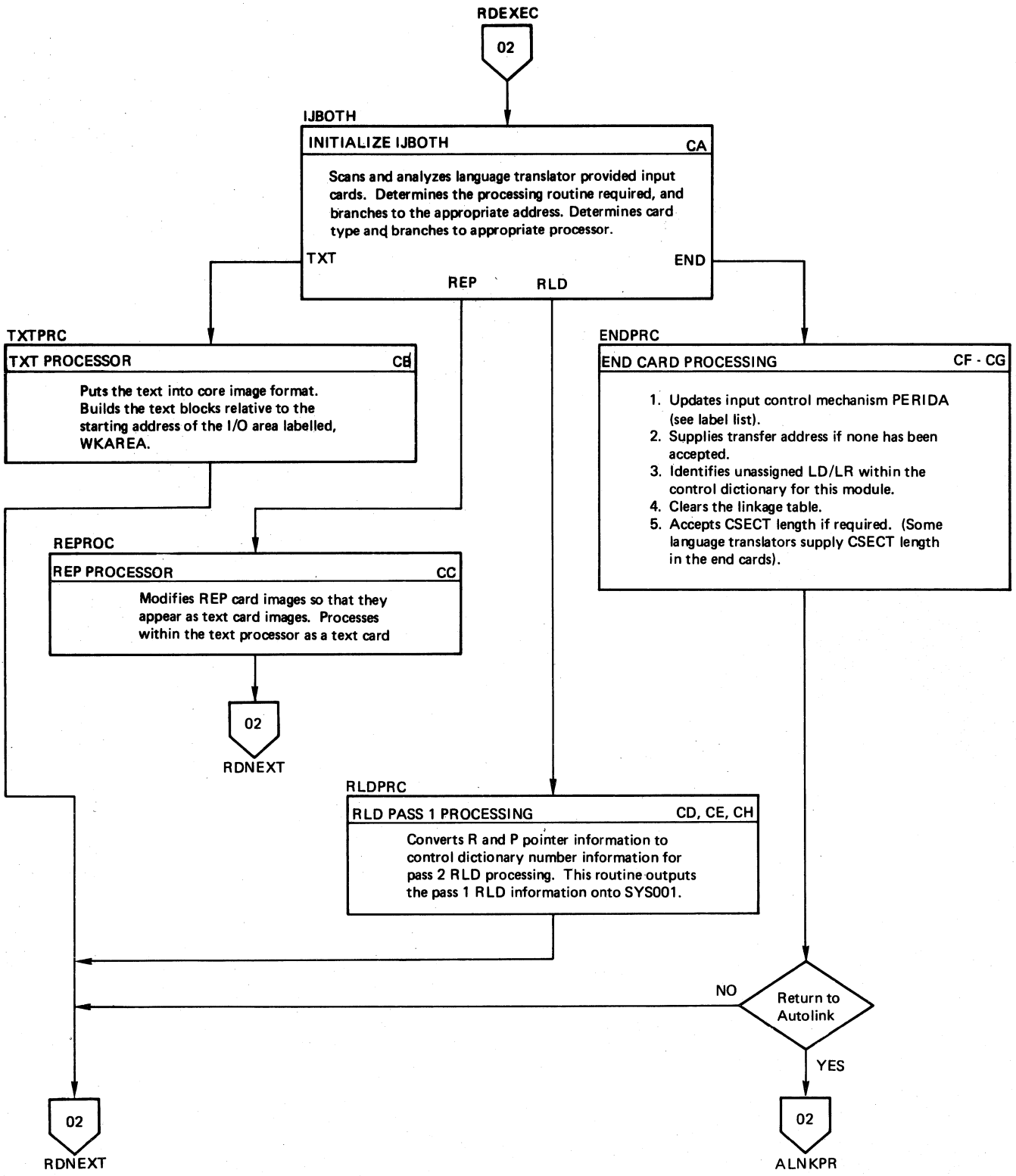


Chart 07. IJBSCN - Control Statement (INCLUDE, PHASE, and ENTRY) and Scan Processing

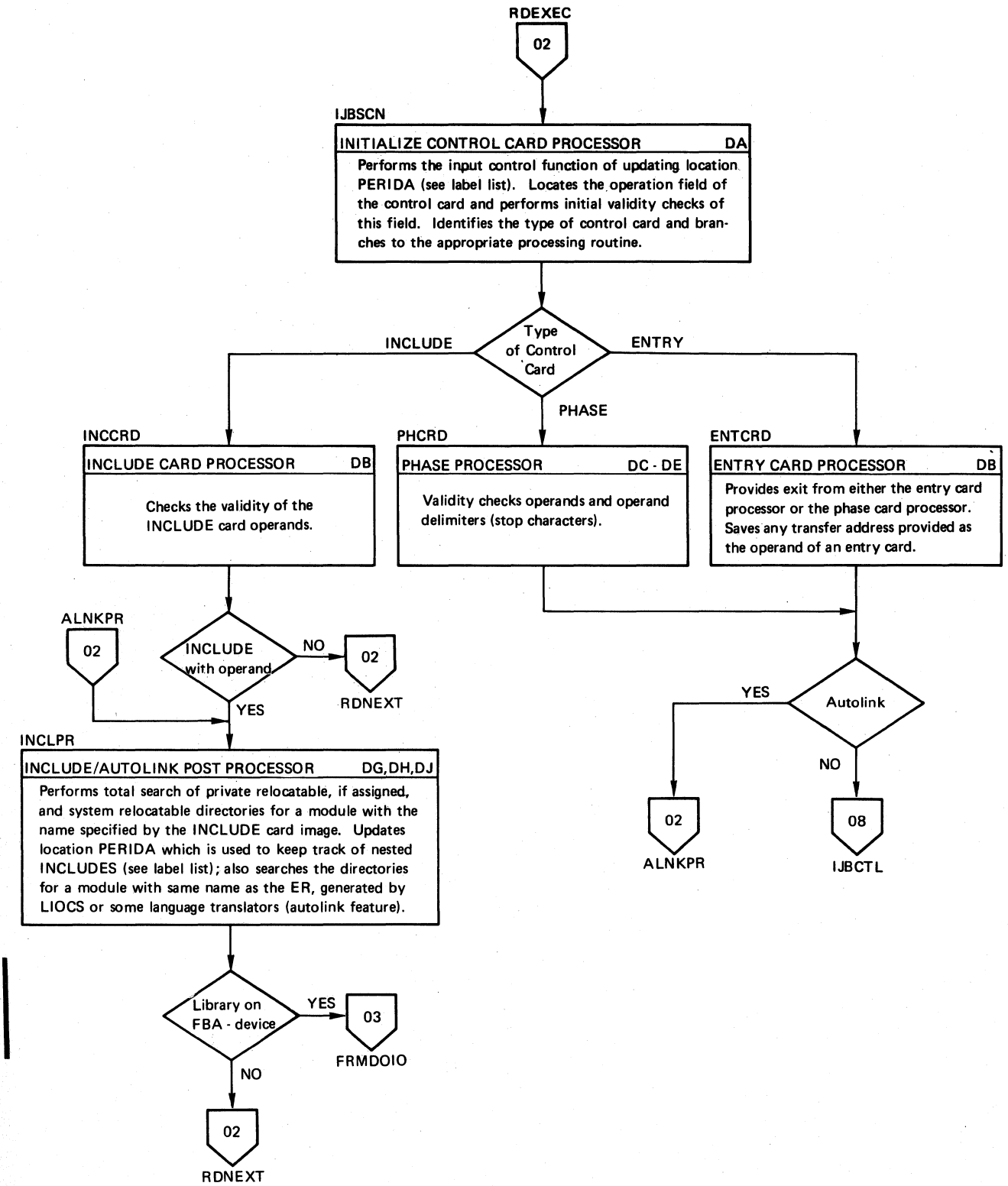


Chart 08. IJBCTL - PHASE and ENTRY Statement Processing

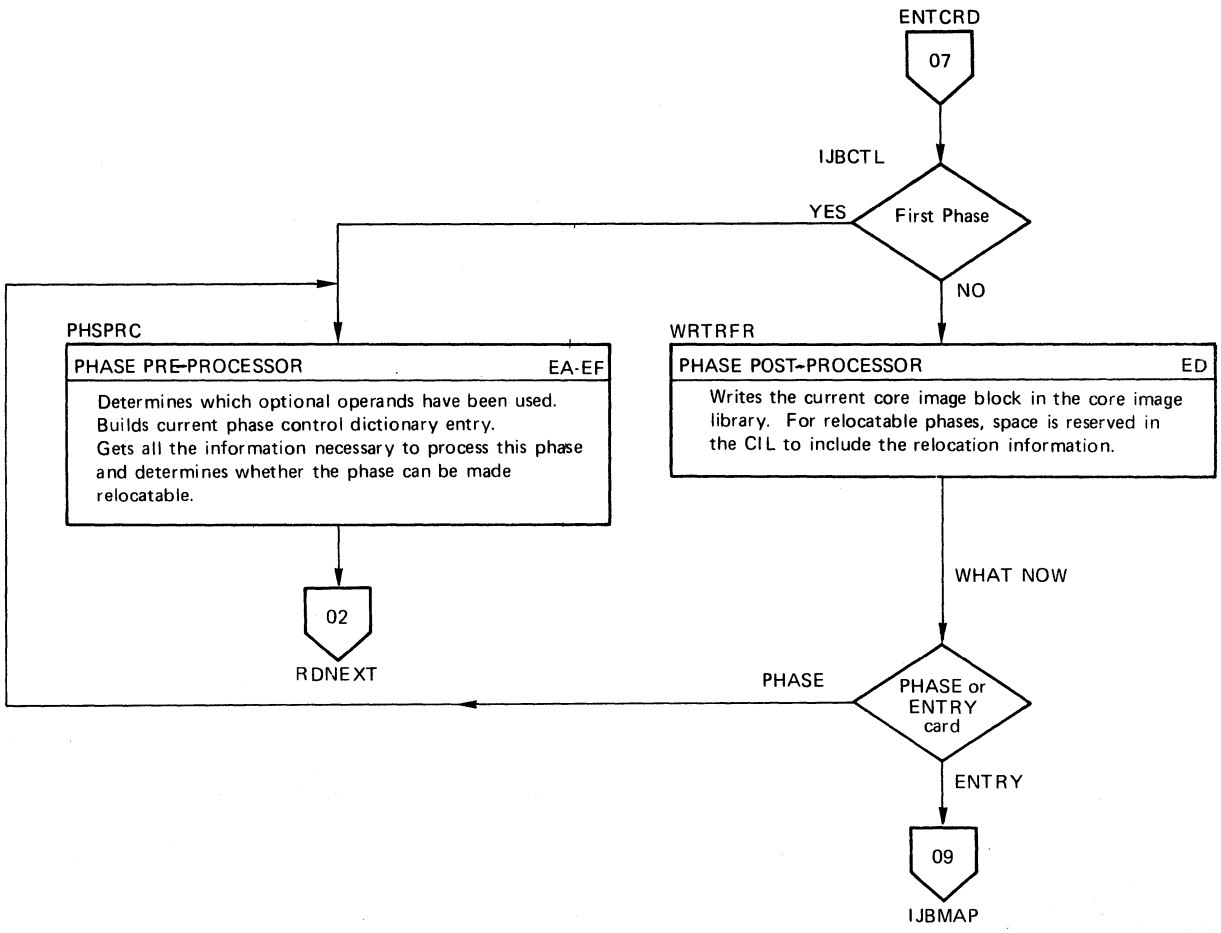


Chart 09. IJBMAP - Print Map

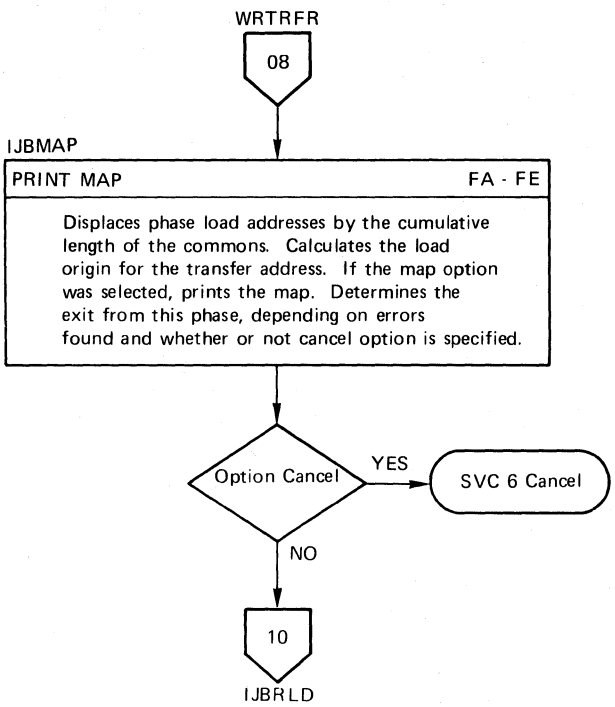


Chart 10. IJBRLD - RLD Processing

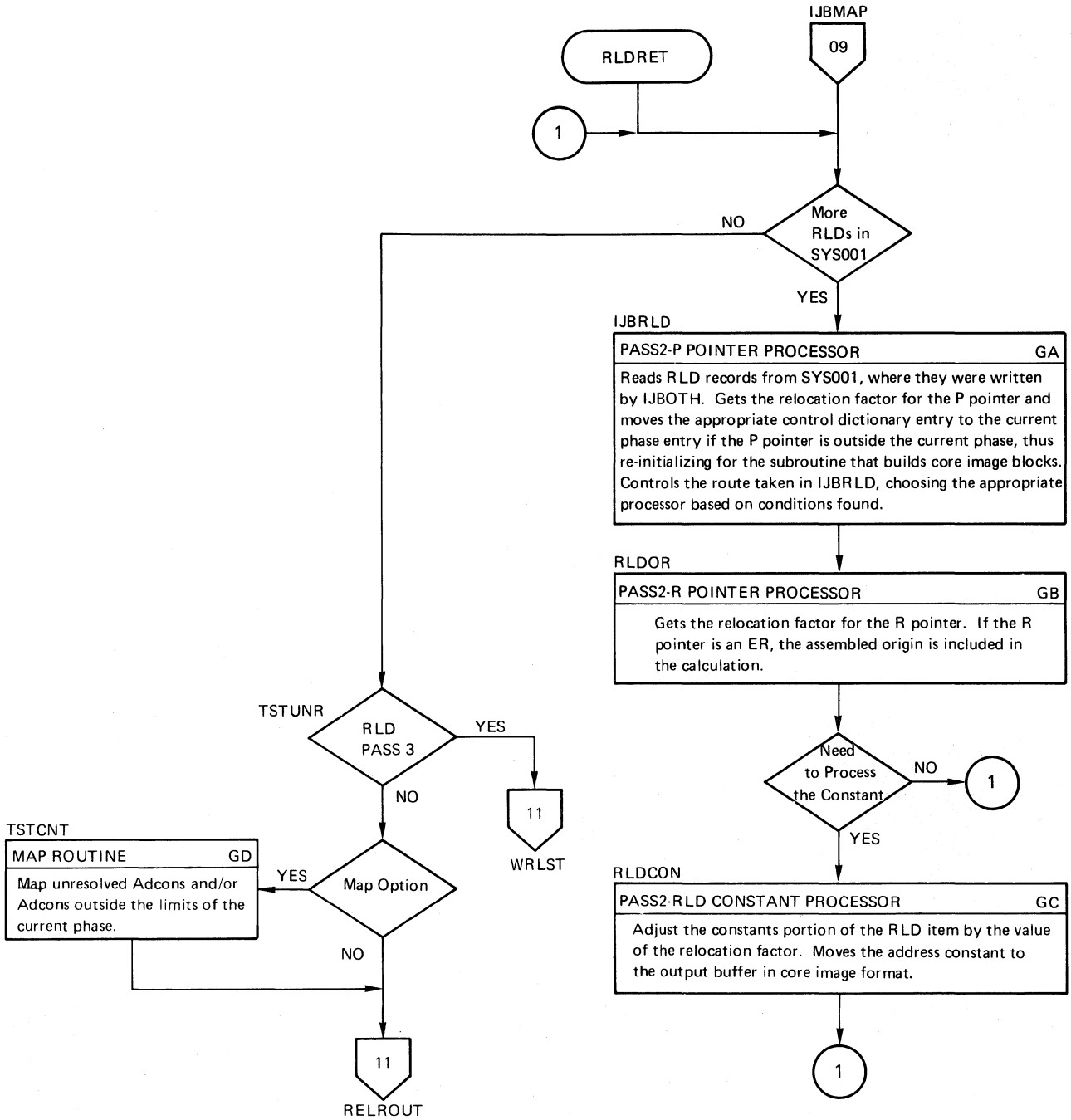


Chart 11. IJBRLD - RLD Processing

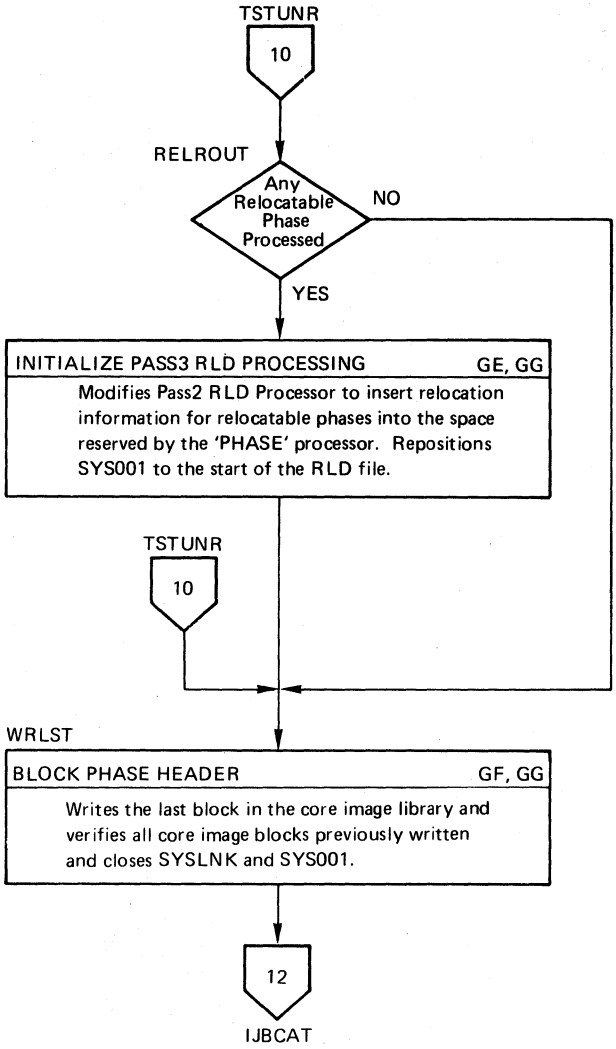
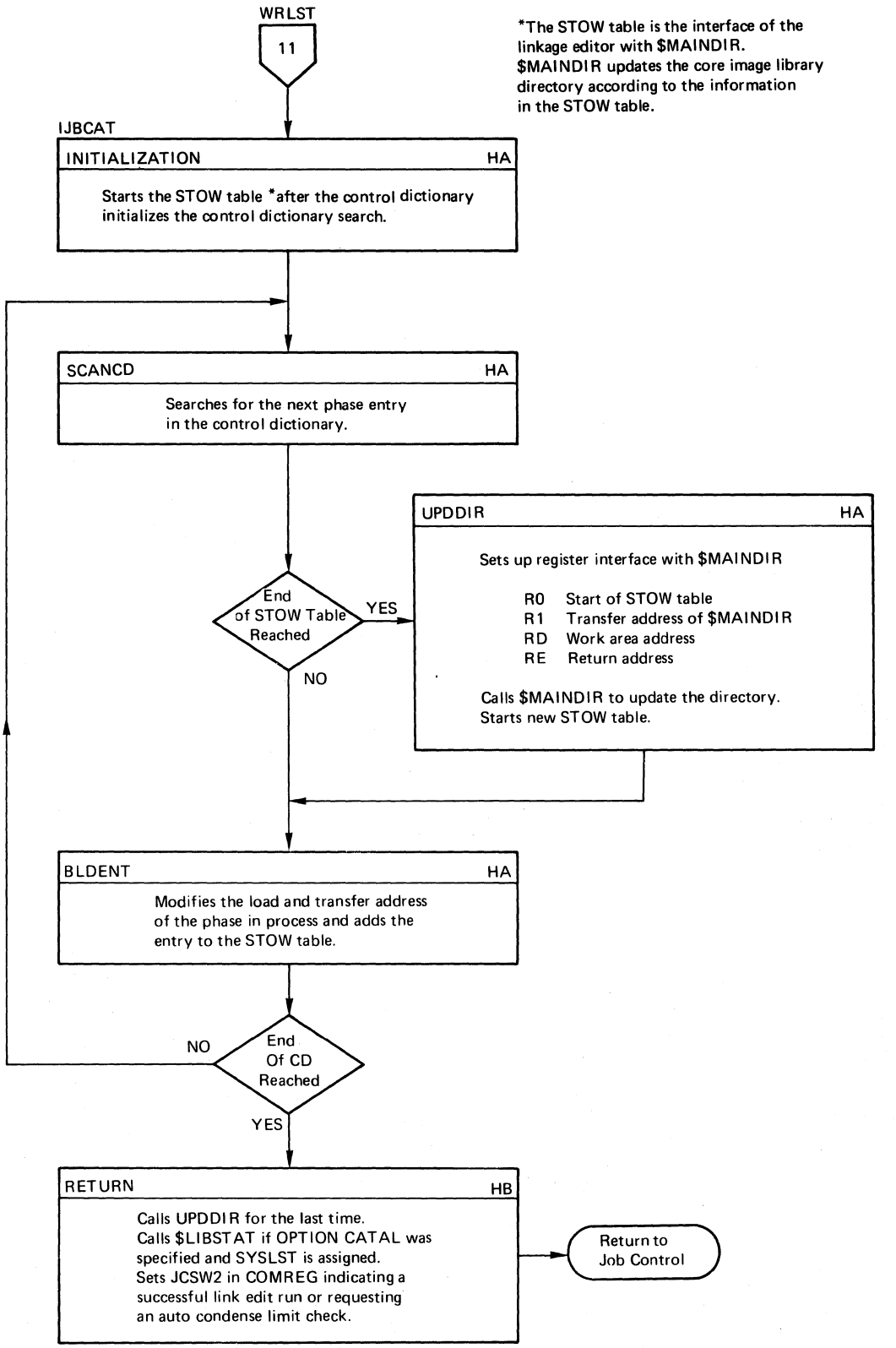
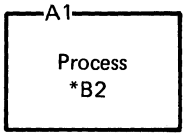


Chart 12. IJBCAT - Catalog Routine



DETAIL CHARTS

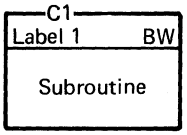


DESCRIPTION

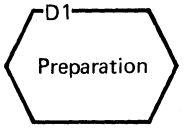
A group of program instructions that perform a processing function of the program. The label, if any, is shown above the block.

*B2

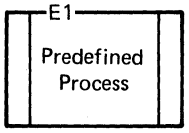
If any additional explanation is required, its location on the chart is identified by an asterisk and the block ID.



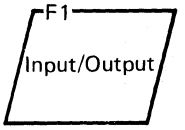
Description of a subroutine. The starting label of the routine appears above the stripe. If the subroutine is documented in detail on another flowchart, the ID of this flowchart is also shown.



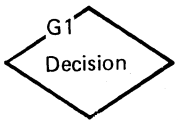
An instruction, or group of instructions, that changes portions of a routine or initializes a routine for given conditions.



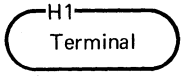
A group of operations not detailed in the flowcharts in this manual, such as user's routines.



Any function of an input/output device or program, usually branching to an I/O routine to perform the function stated in the block.



Points where the program branches to alternate processing, based upon variable conditions such as program switch settings and test results.



The beginning, end or point of interruption in a program.

On-page connector. An entry from or an exit to another function on the same flowchart. The number in the connector identifies the corresponding entry or exit on the chart.

Filinp

Off-page connector, an entry from, or an exit to, a given point on another flowchart. The characters in the connector identify the chart and block. The corresponding label, if any, is placed outside the connector. For multiple entries and exits, an asterisk appears in the connector and the characters are listed nearby.

EXAMPLE

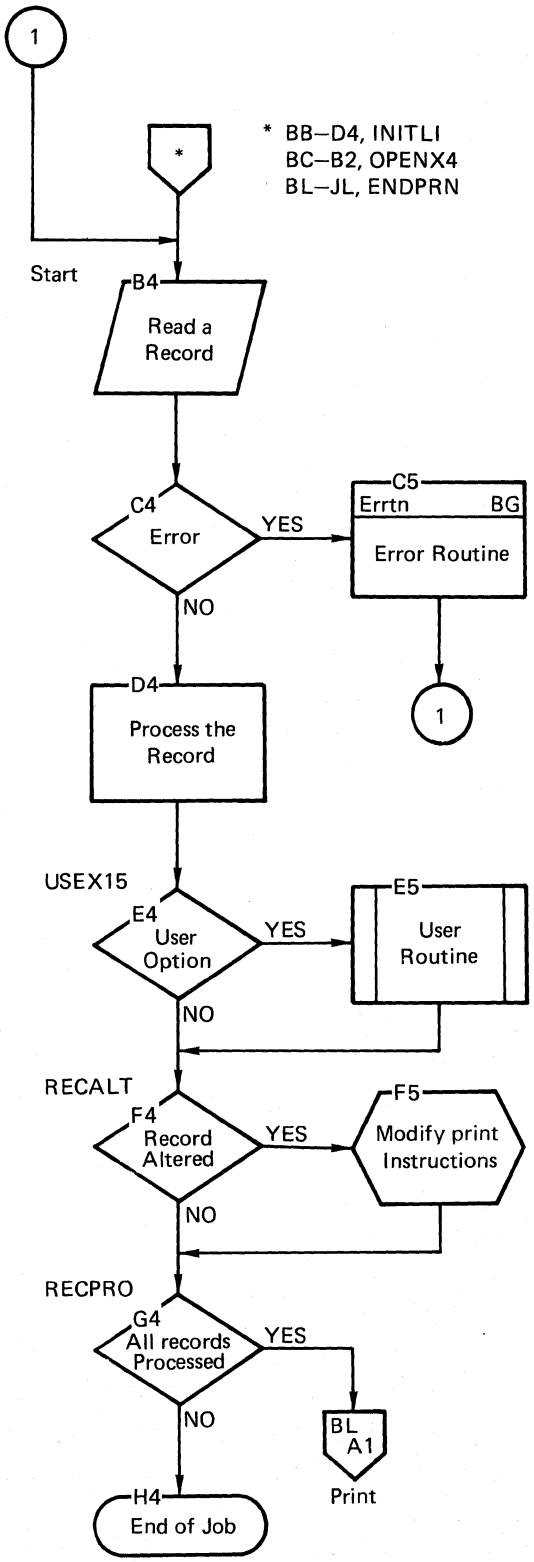


Chart AA. IJBLNK - Read SYSLNK Subroutine. Refer to Chart 02

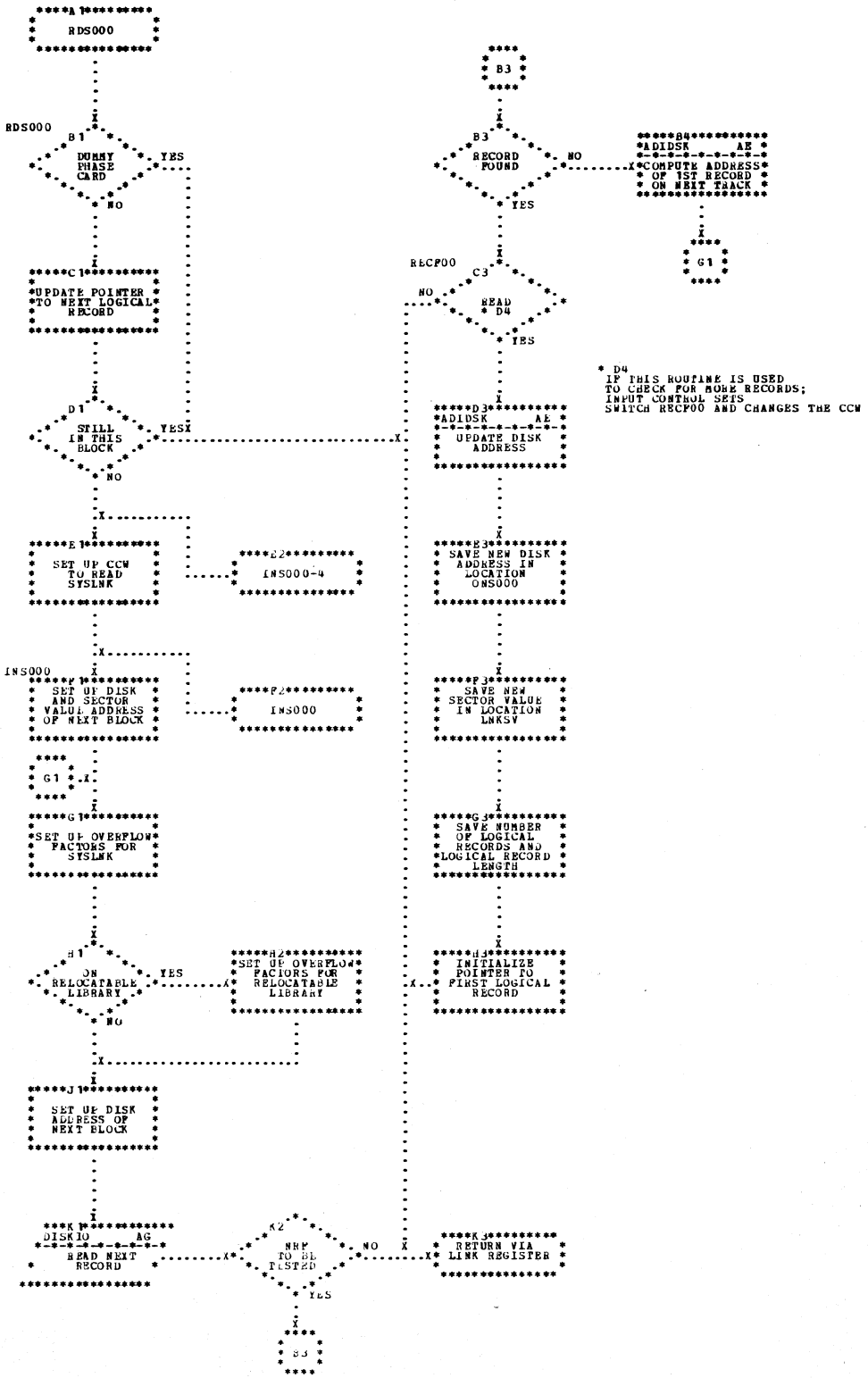


Chart AB. IJELNK - Control Dictionary Search Subroutine. Refer to Chart 02

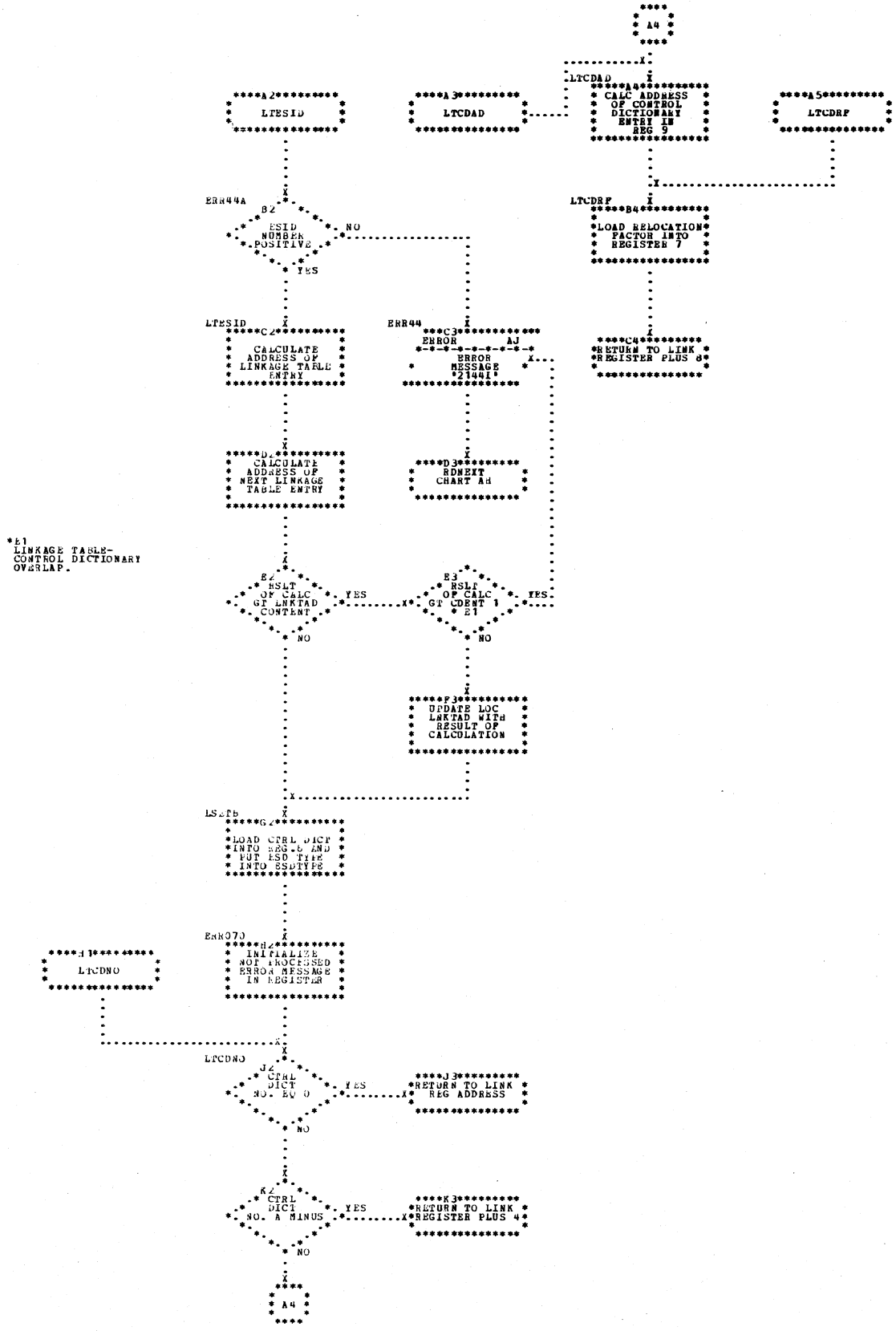


Chart AC. IJBLNK - Label Search and Convert to Binary Subroutines. Refer to Chart 02

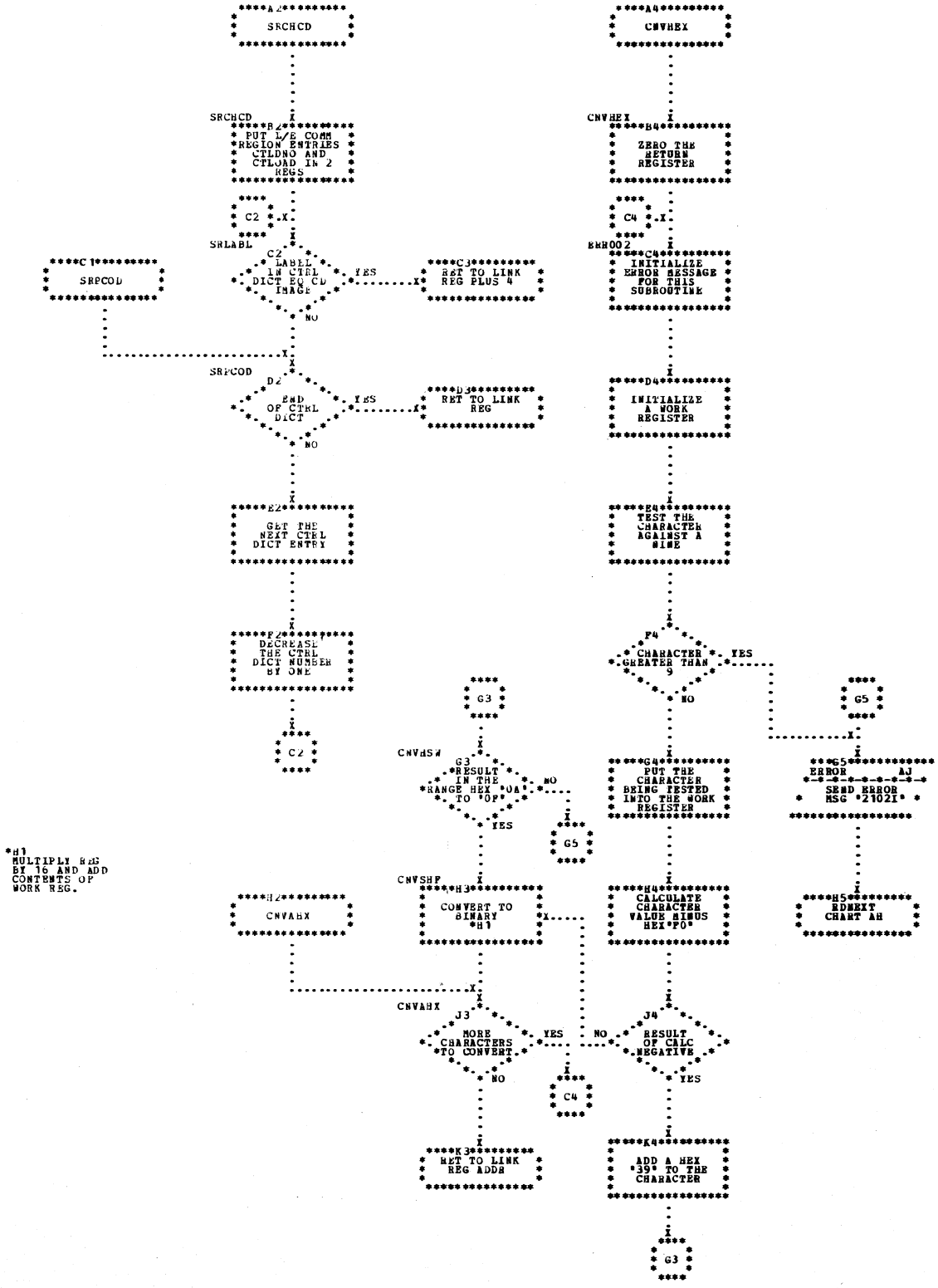


Chart AD. IJBLNK - Print Subroutines. Refer to Chart 02

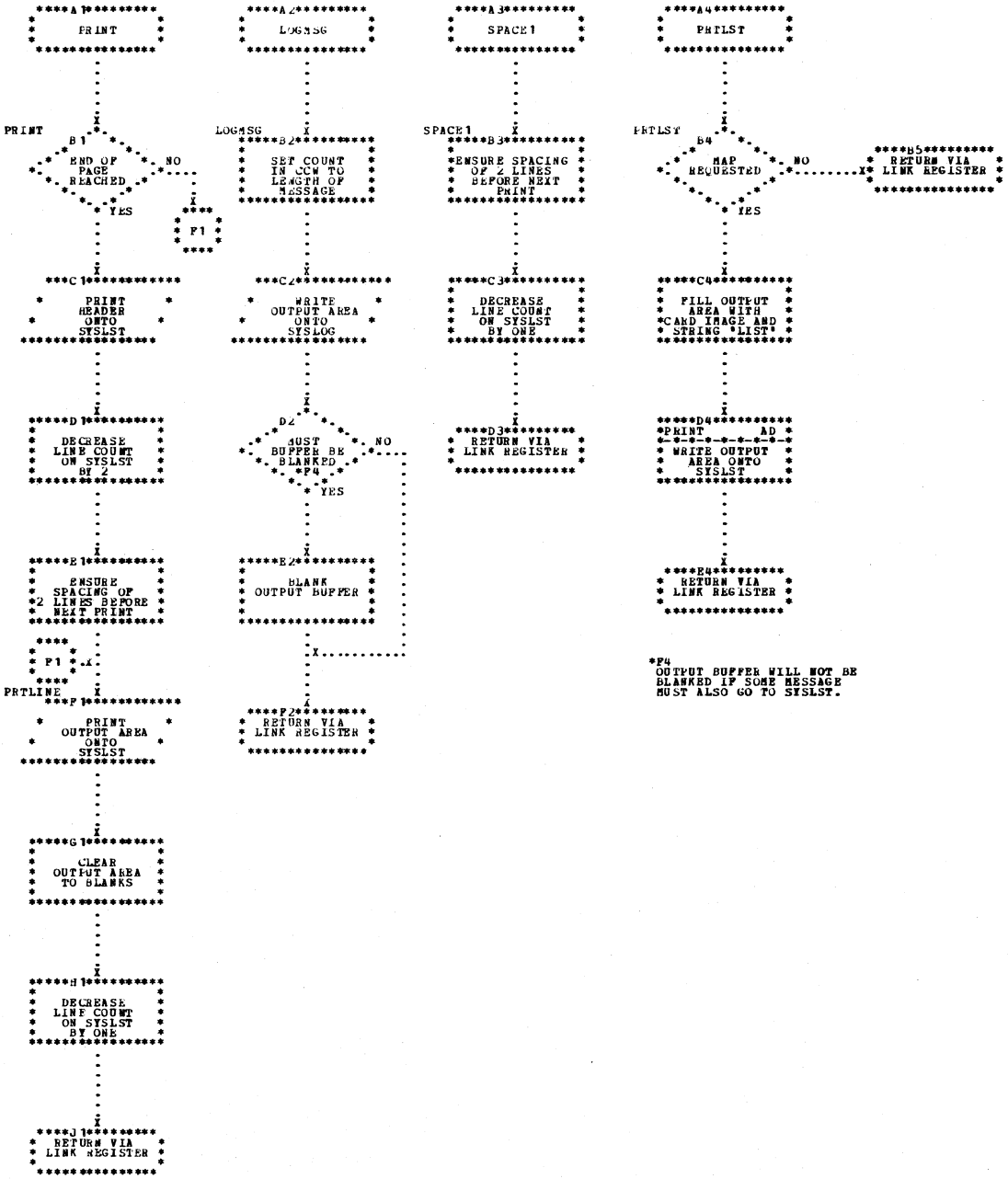


Chart AE. IJBLNK - Input Pointer to Address to be Updated. Refer to Chart 02

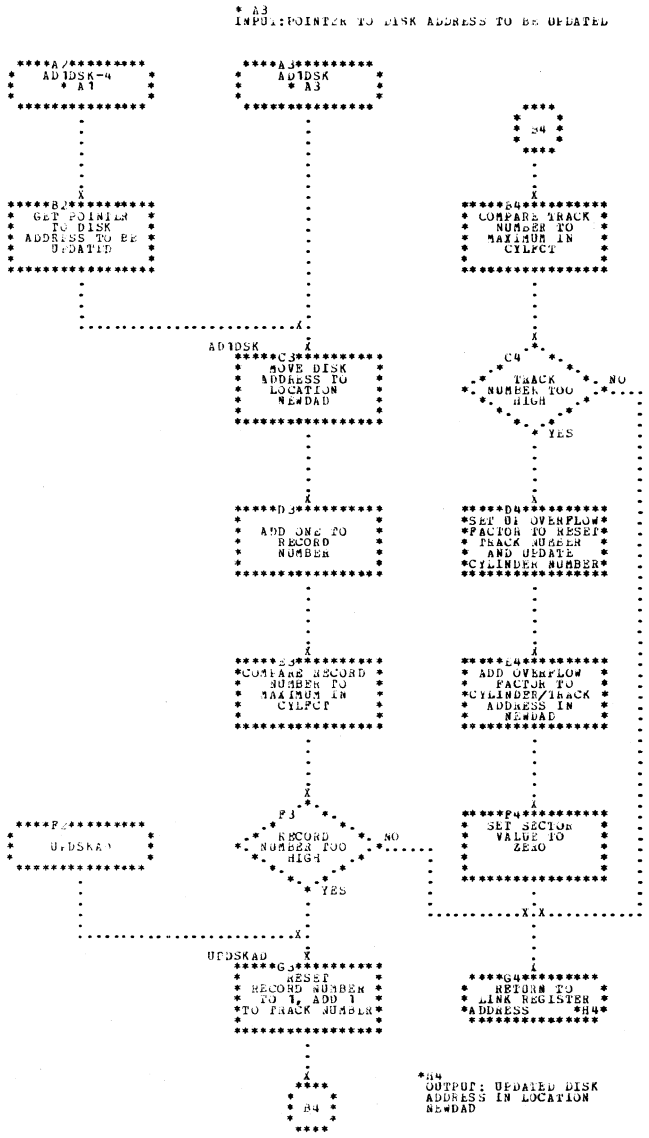
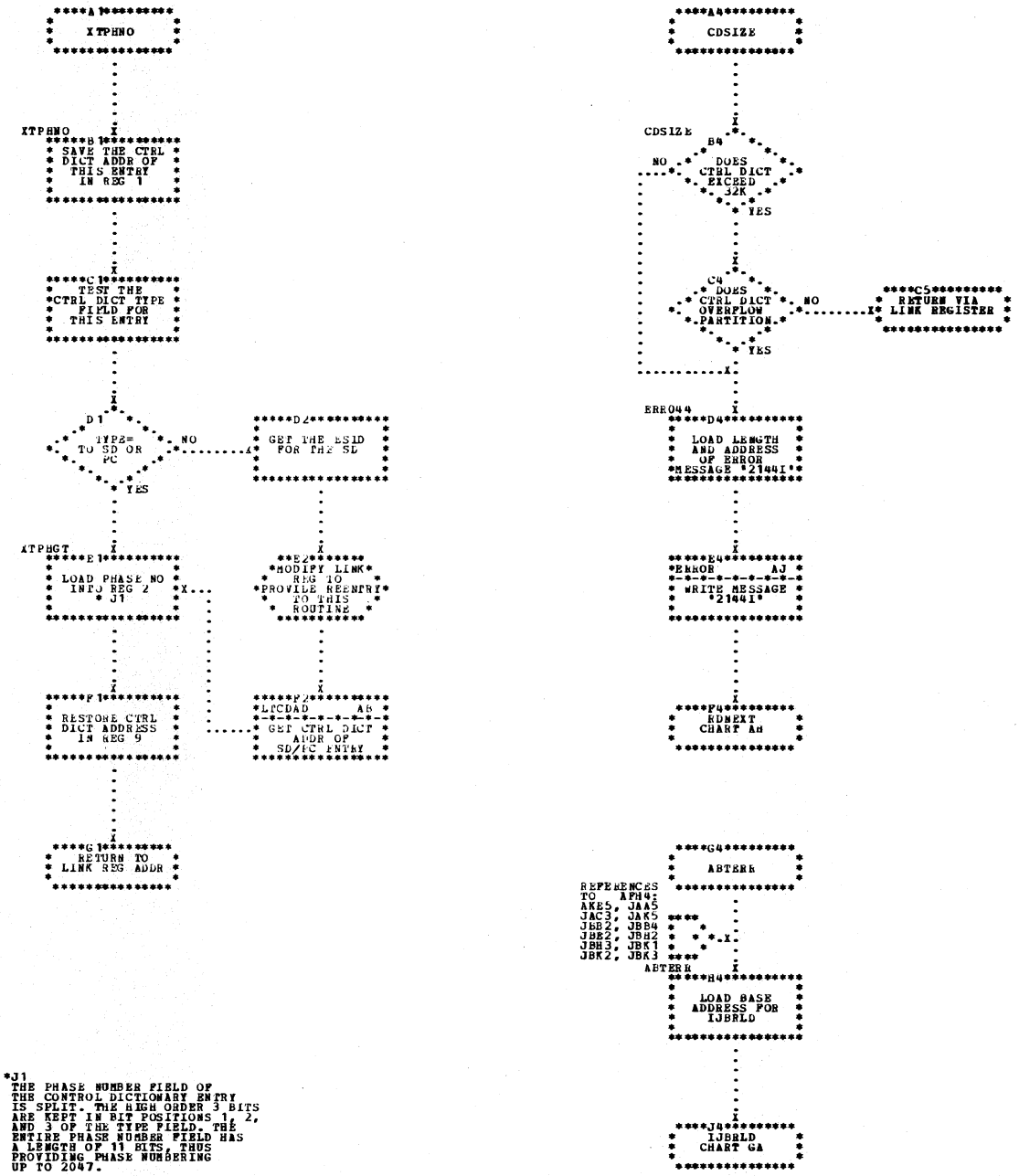


Chart AF. IJBLNK - Extract Phase Number, Overflow Test, and Phase Load Subroutines
Refer to Chart 02



*J1
THE PHASE NUMBER FIELD OF THE CONTROL DICTIONARY ENTRY IS SPLIT. THE HIGH ORDER 3 BITS ARE KEPT IN BIT POSITIONS 1, 2, AND 3 OF THE TYPE FIELD. THE ENTIRE PHASE NUMBER FIELD HAS A LENGTH OF 11 BITS, THUS PROVIDING PHASE NUMBERING UP TO 2047.

Chart AG. IJBLNK - Read/Write and Autolink Processing Subroutines. Refer to Chart 02

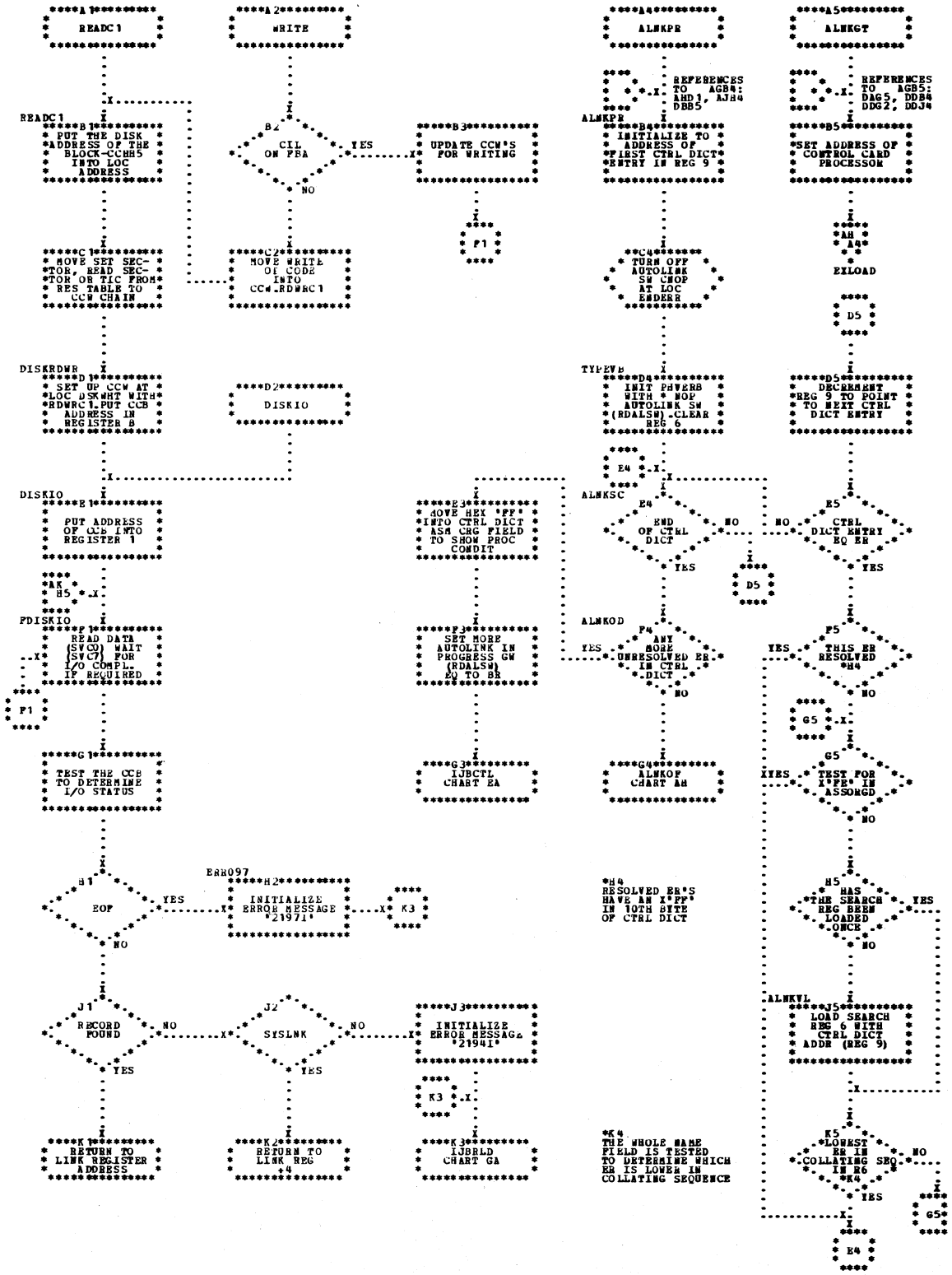


Chart AH. IJBLNK - Read Input Stream. Refer to Chart 02

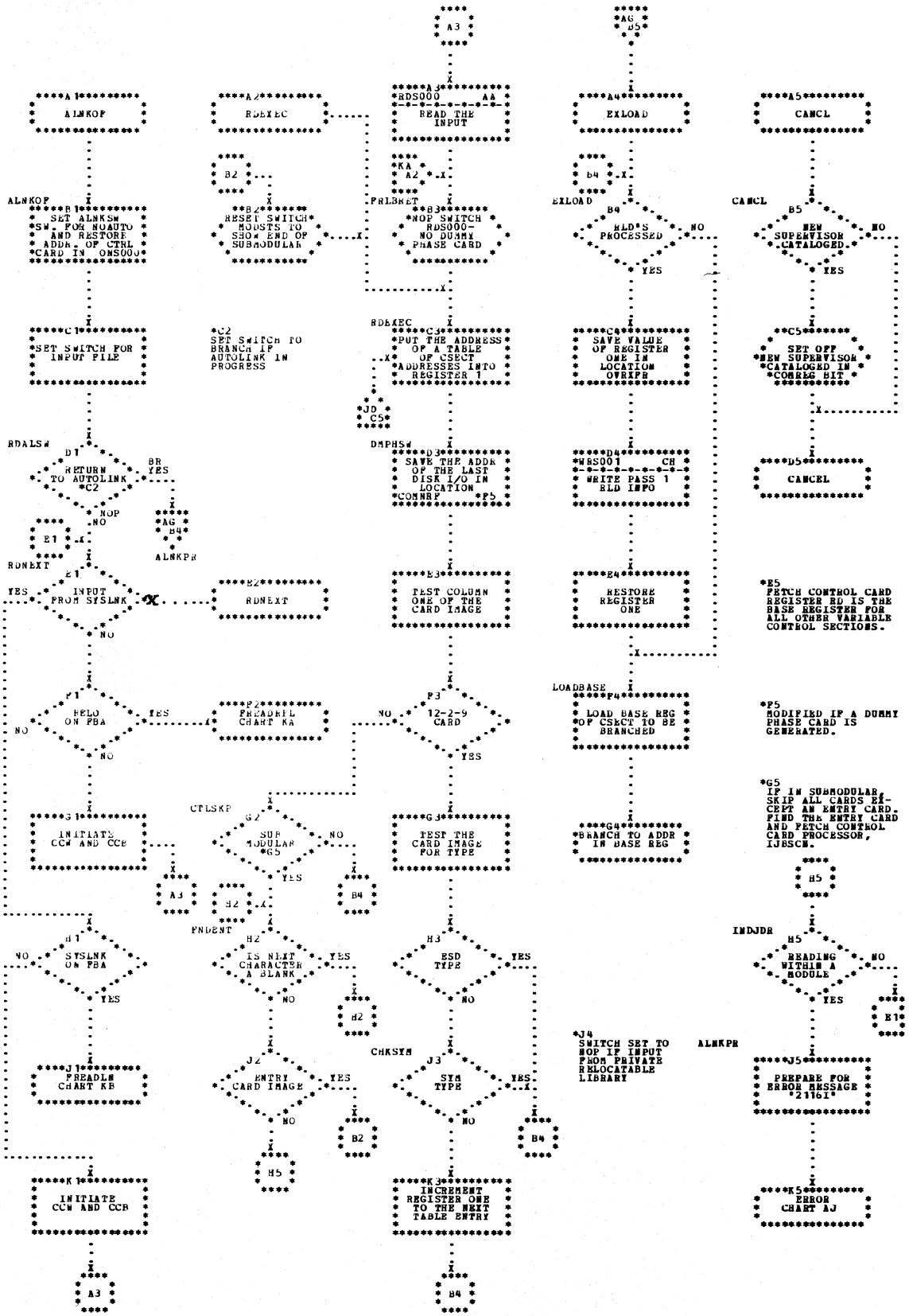


Chart AJ. IJBLNK - Non-Abort Error and Overlay Subroutines. Refer to Chart 02

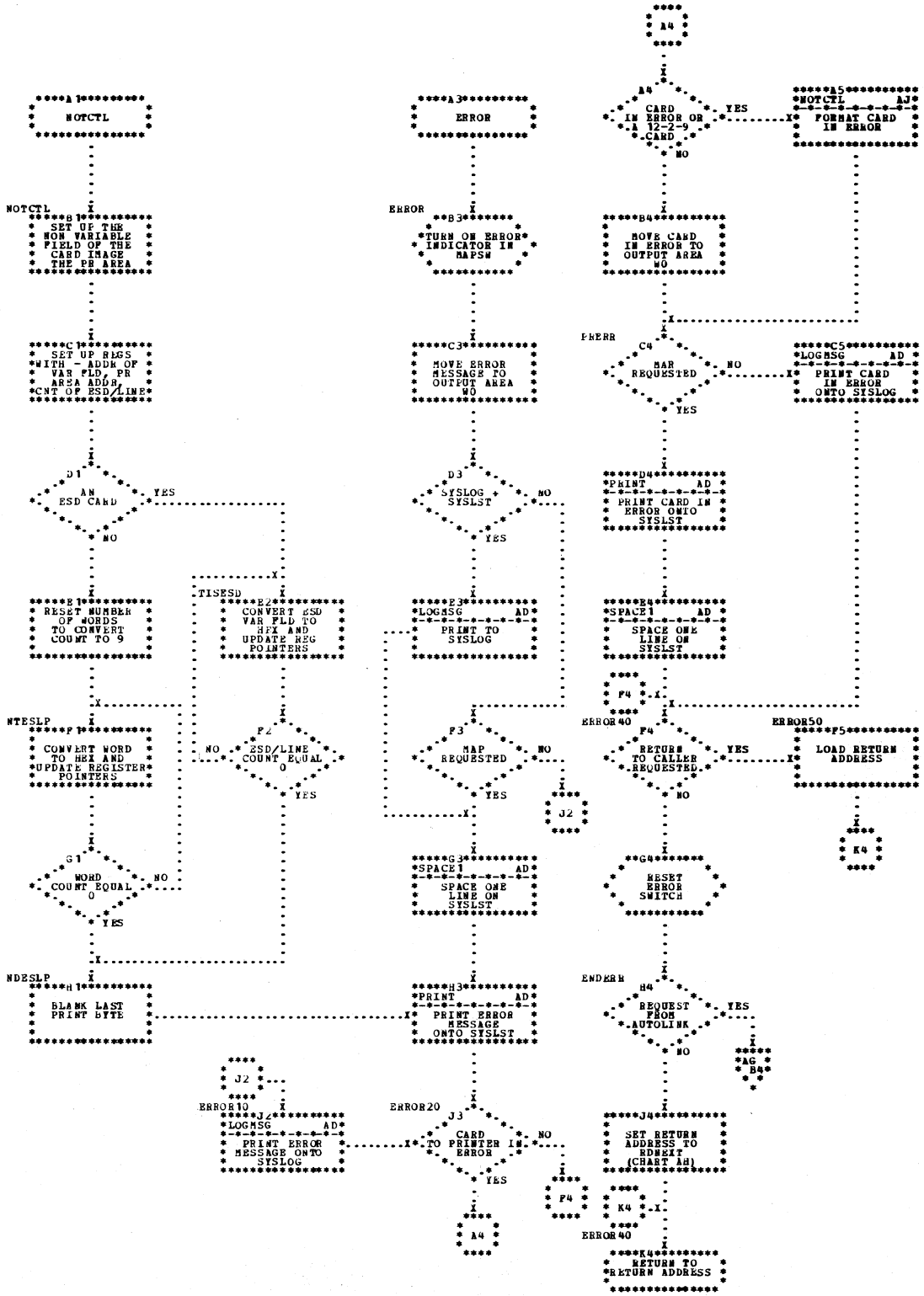


Chart AK. IJBLNK - Core Image Block Building Subroutine. Refer to Chart 02

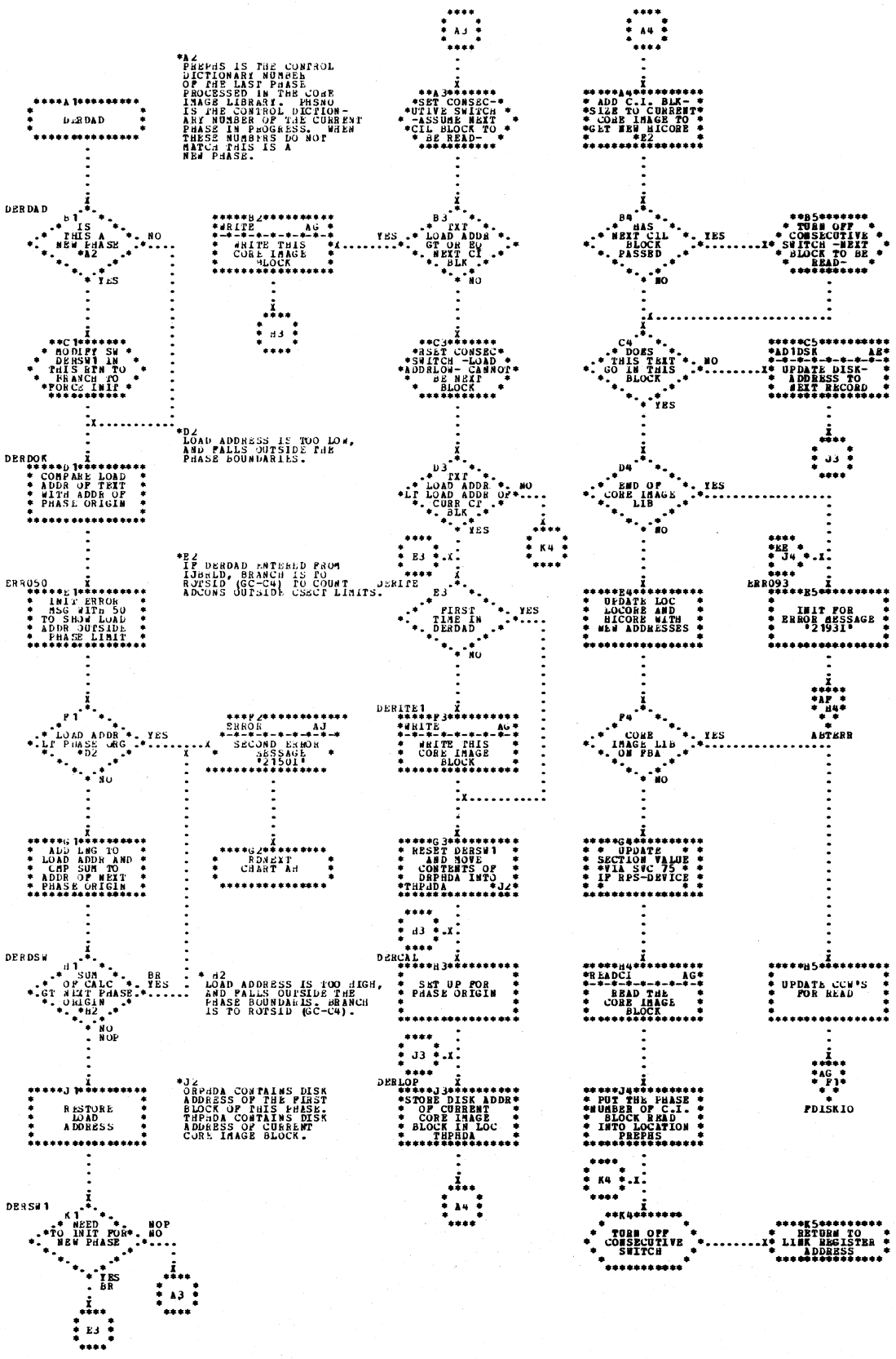


Chart BA. IJBESD - Initialize ESD Processor and ESD Processor Card Image Check (Part 1 of 3). Refer to Charts 04 and 05

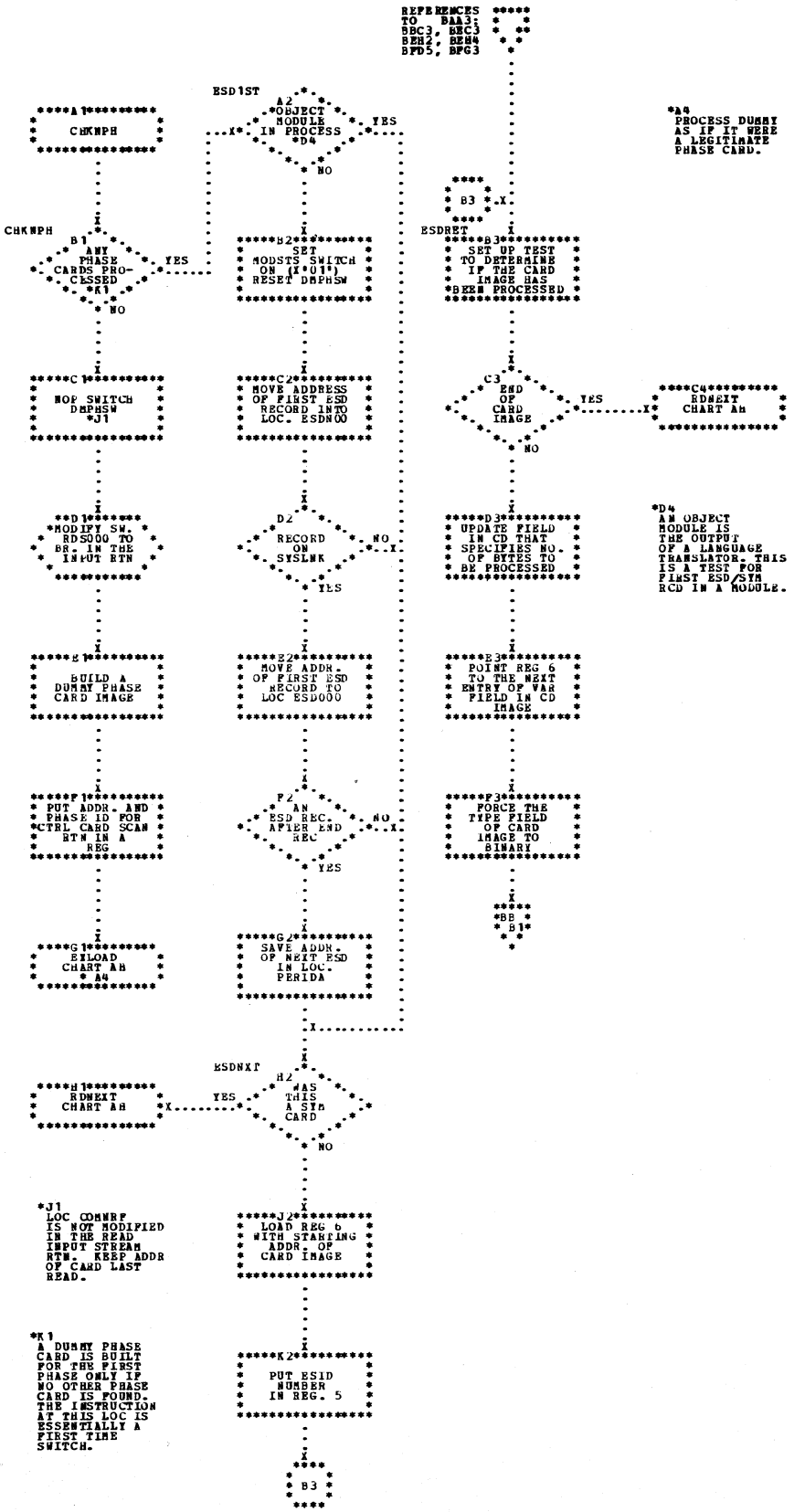


Chart BB. IJBESD - ESD Processor Card Image Check (Part 2 of 3)
Refer to Charts 04 and 05

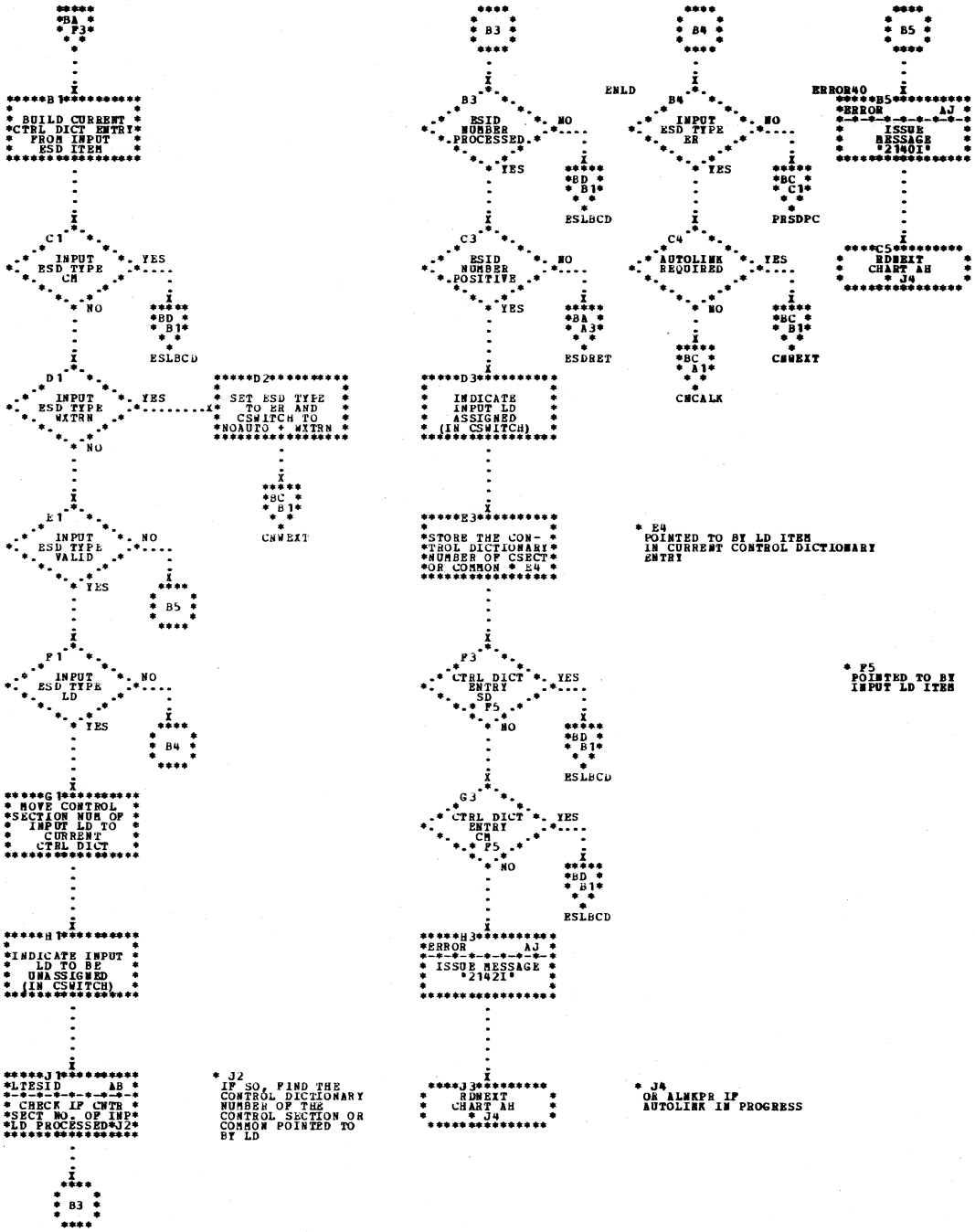


Chart BC. IJBESD - ESD Processor Card Image Check (Part 3 of 3)
Refer to Charts 04 and 05

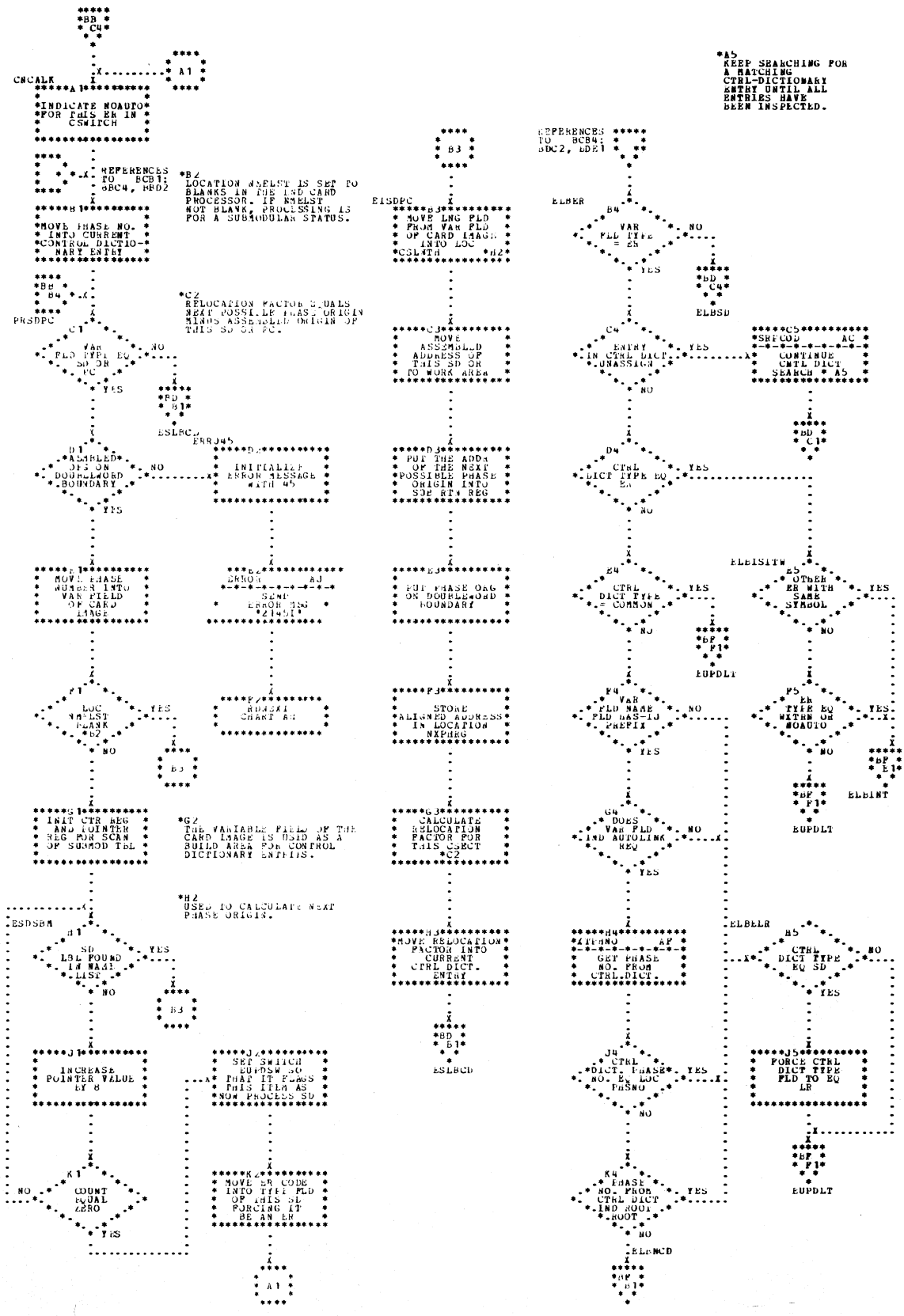


Chart BD. IJBESD - Process ESD Item against Control Dictionary and SD Processor
Refer to Charts 04 and 05

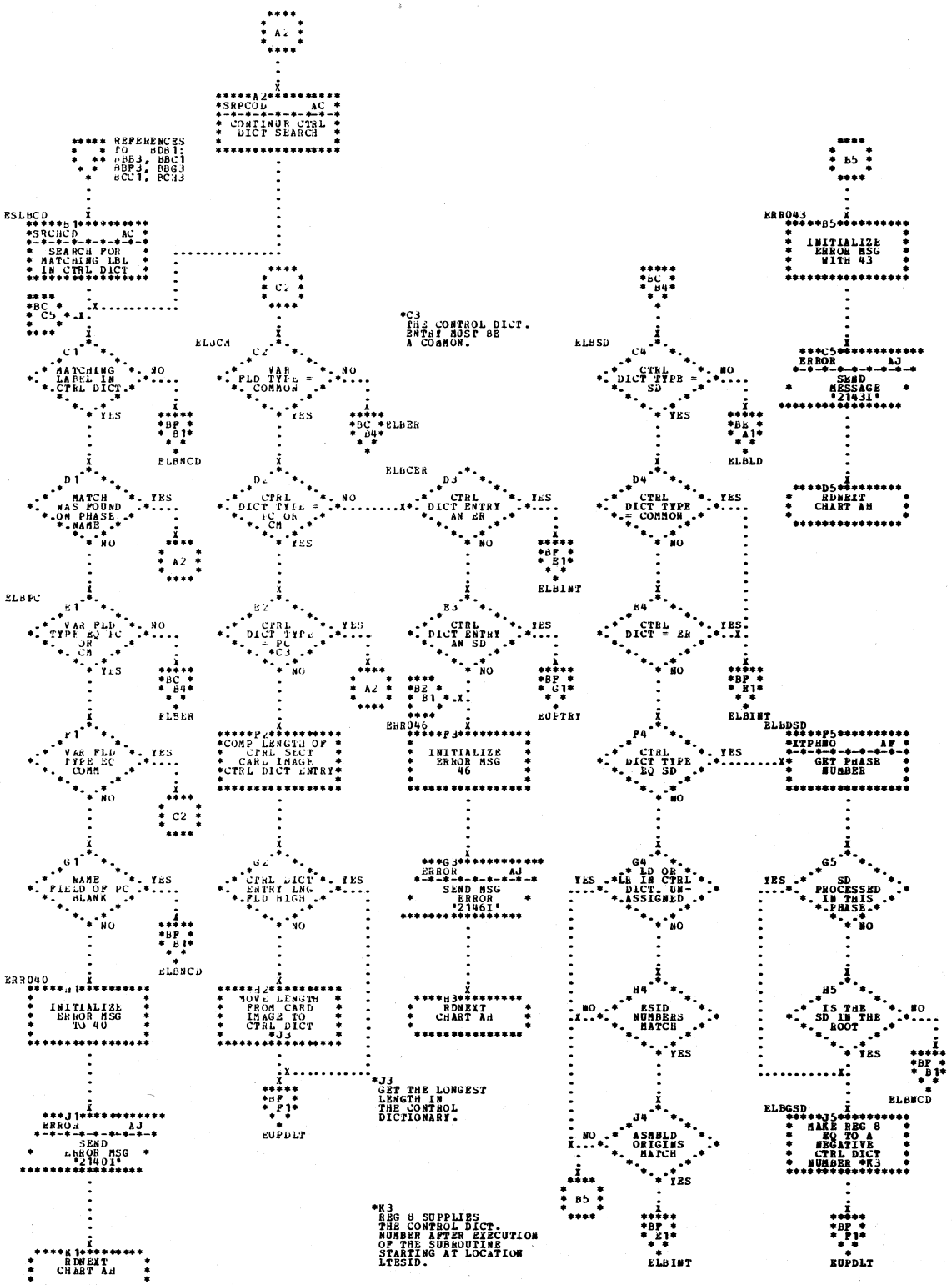


Chart BE. IJBESD - ESD Processor (LD/IR). Refer to Charts 04 and 05

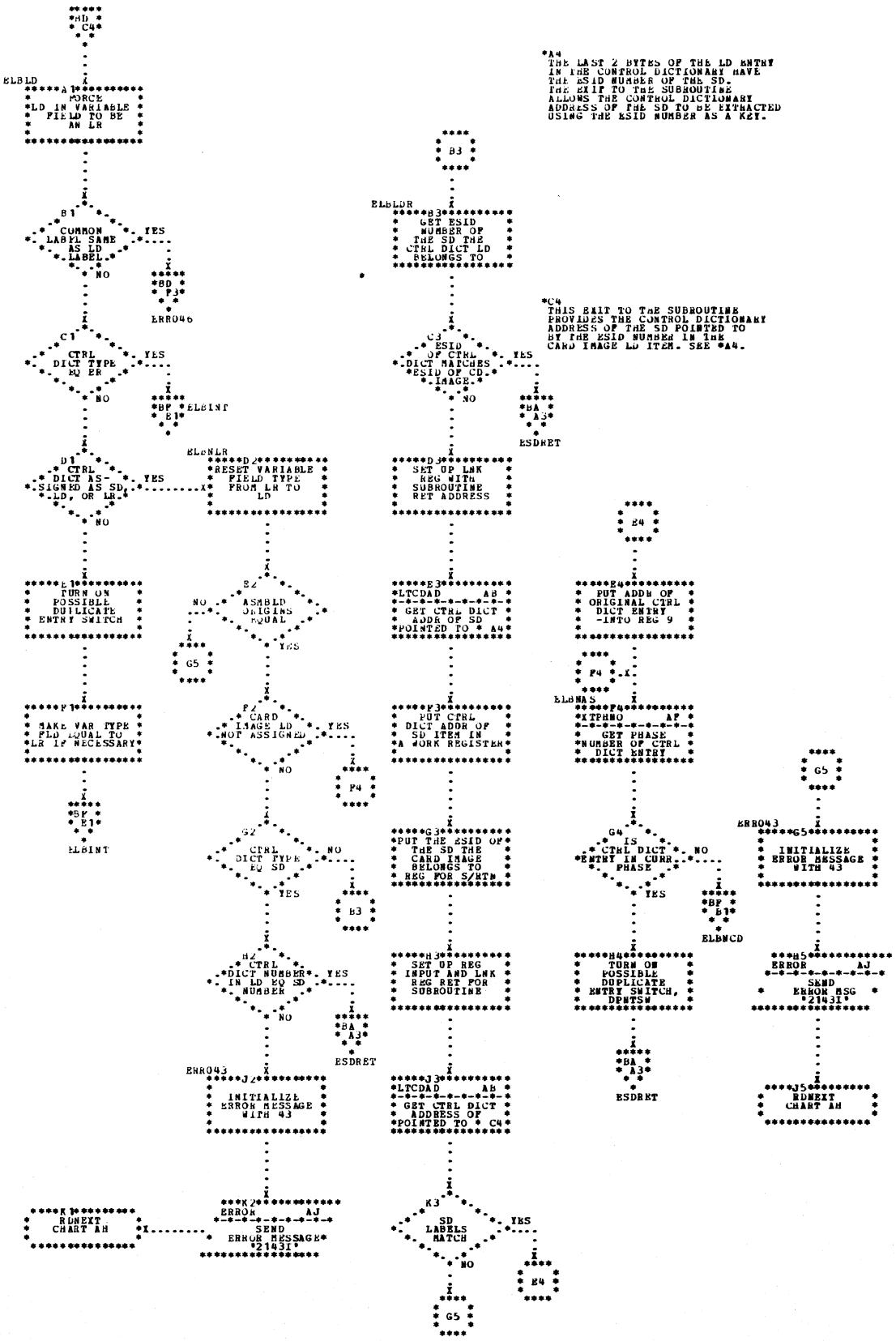


Chart BF. IJBESD - ESD Processor Update Linkage Table and Control Dictionary
Refer to Charts C4 and 05

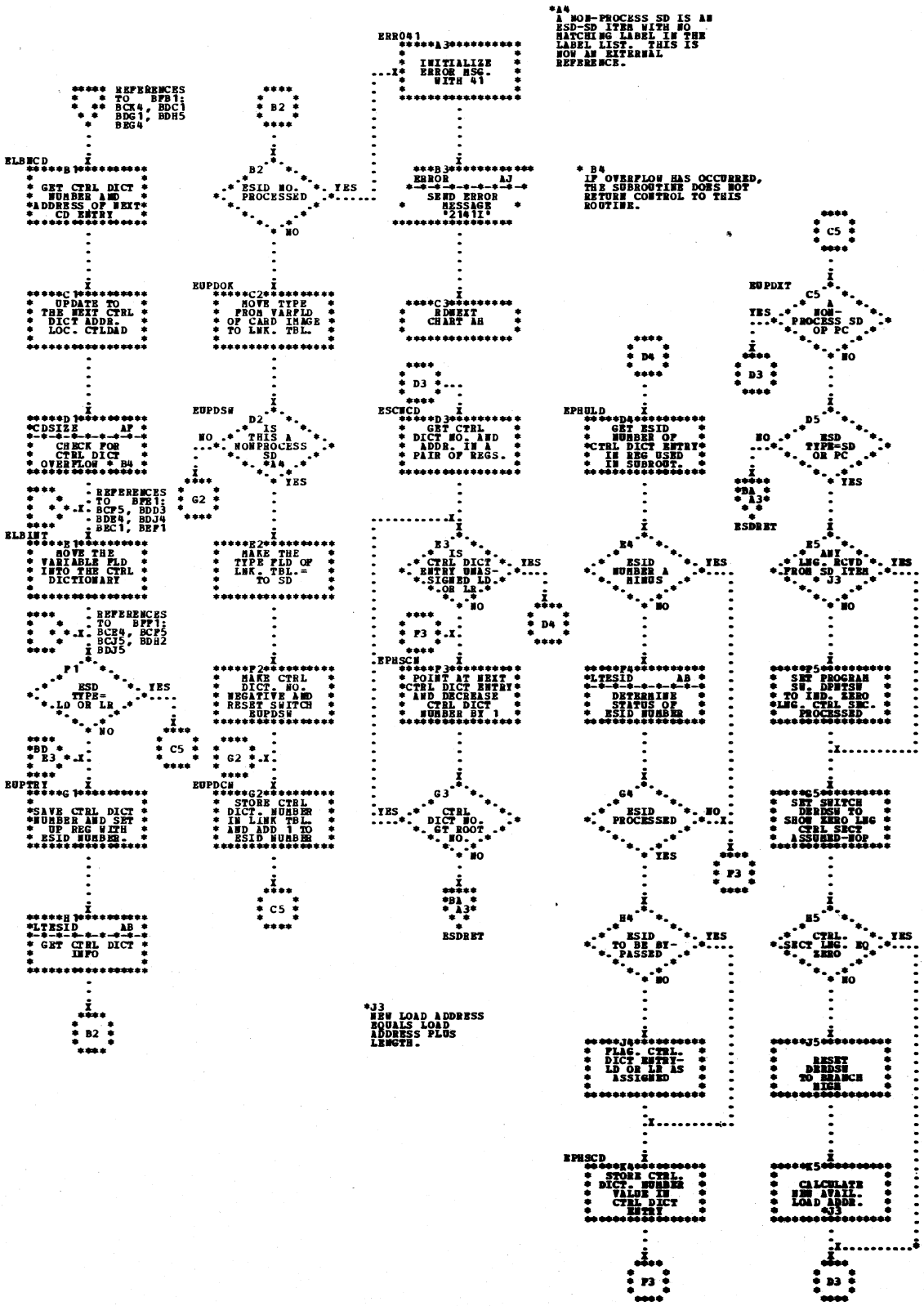


Chart CA. IJBOTH - Initialization Refer to Chart 06

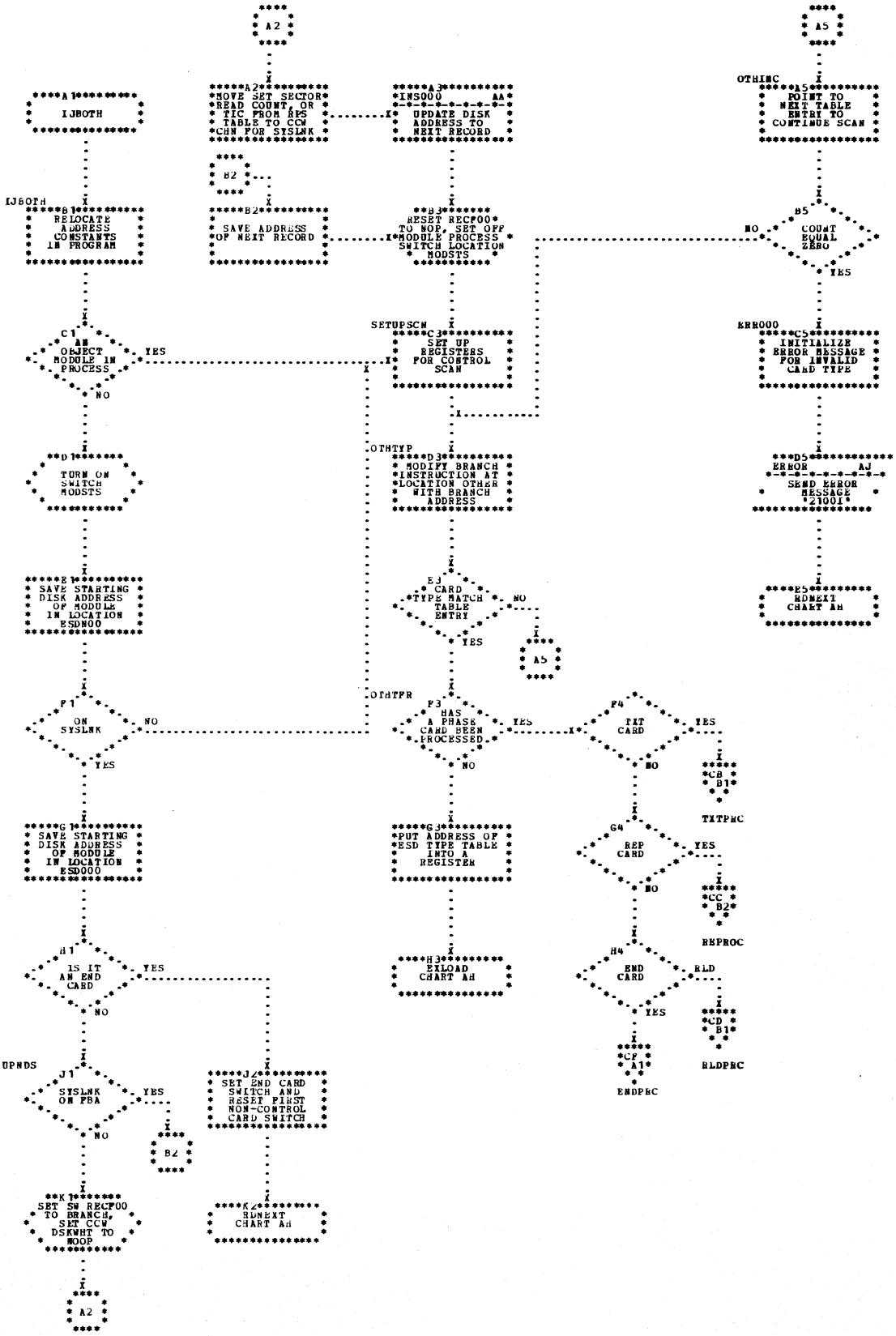


Chart CB. IJBOTH - Text Processor Refer to Chart 06

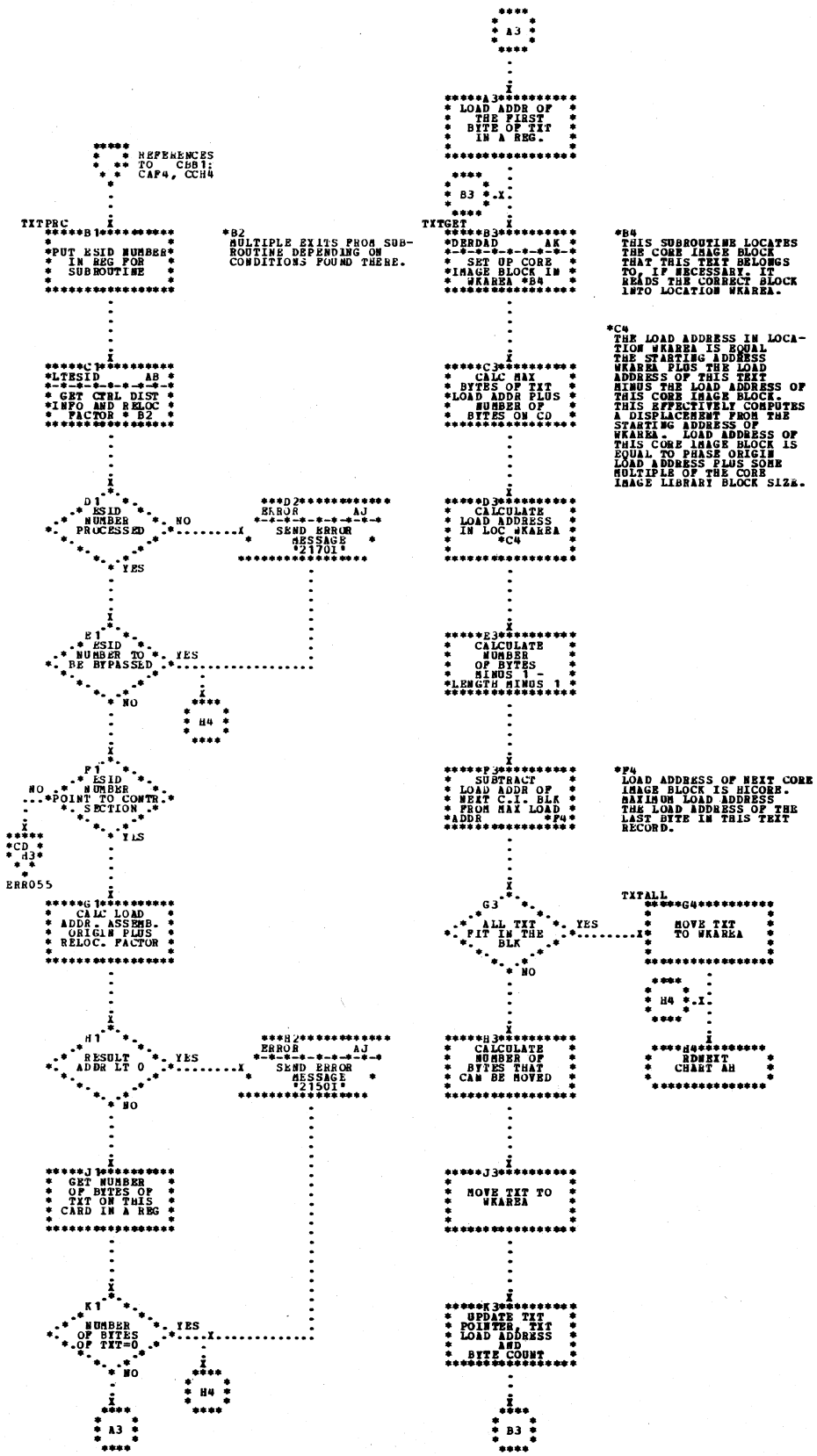


Chart CC. IJBOTH - REP Processor. Refer to Chart 06

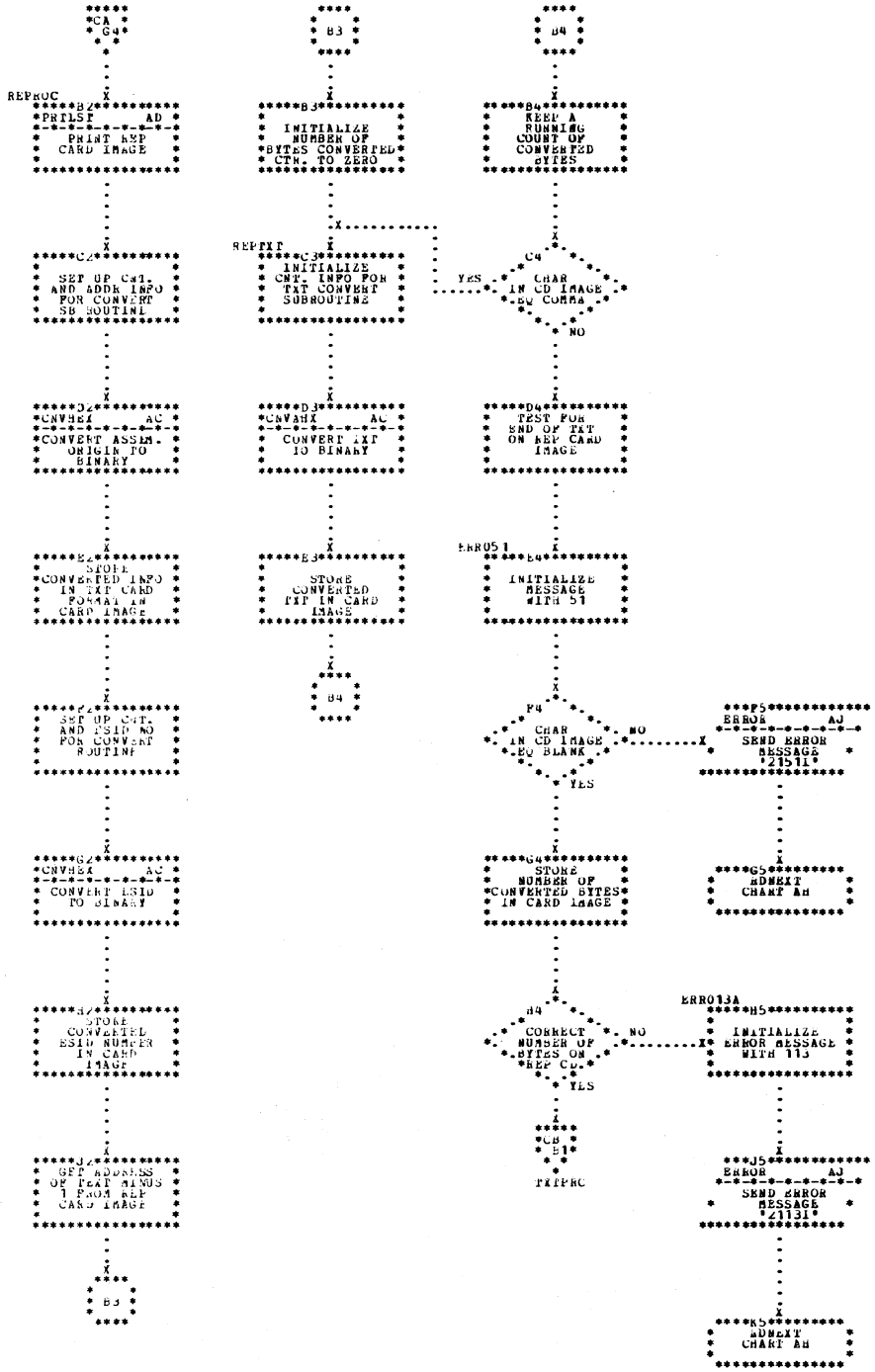


Chart CD. IJBOTH - RLD Pass 1 Processing (Part 1 of 2). Refer to Chart 06

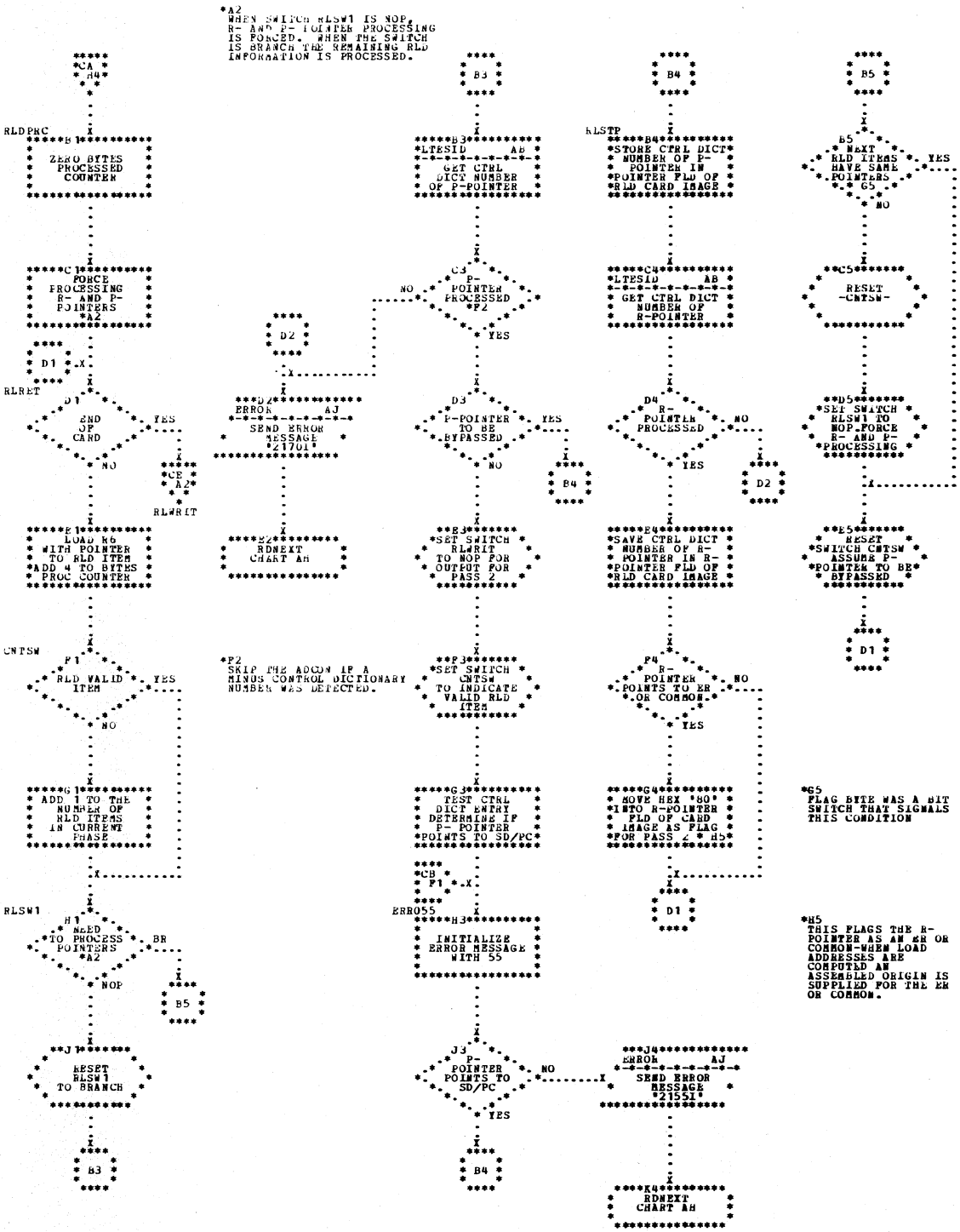


Chart CE. IJBOTH - RLD Pass 1 Processing (Part 2 of 2). Refer to Chart 06

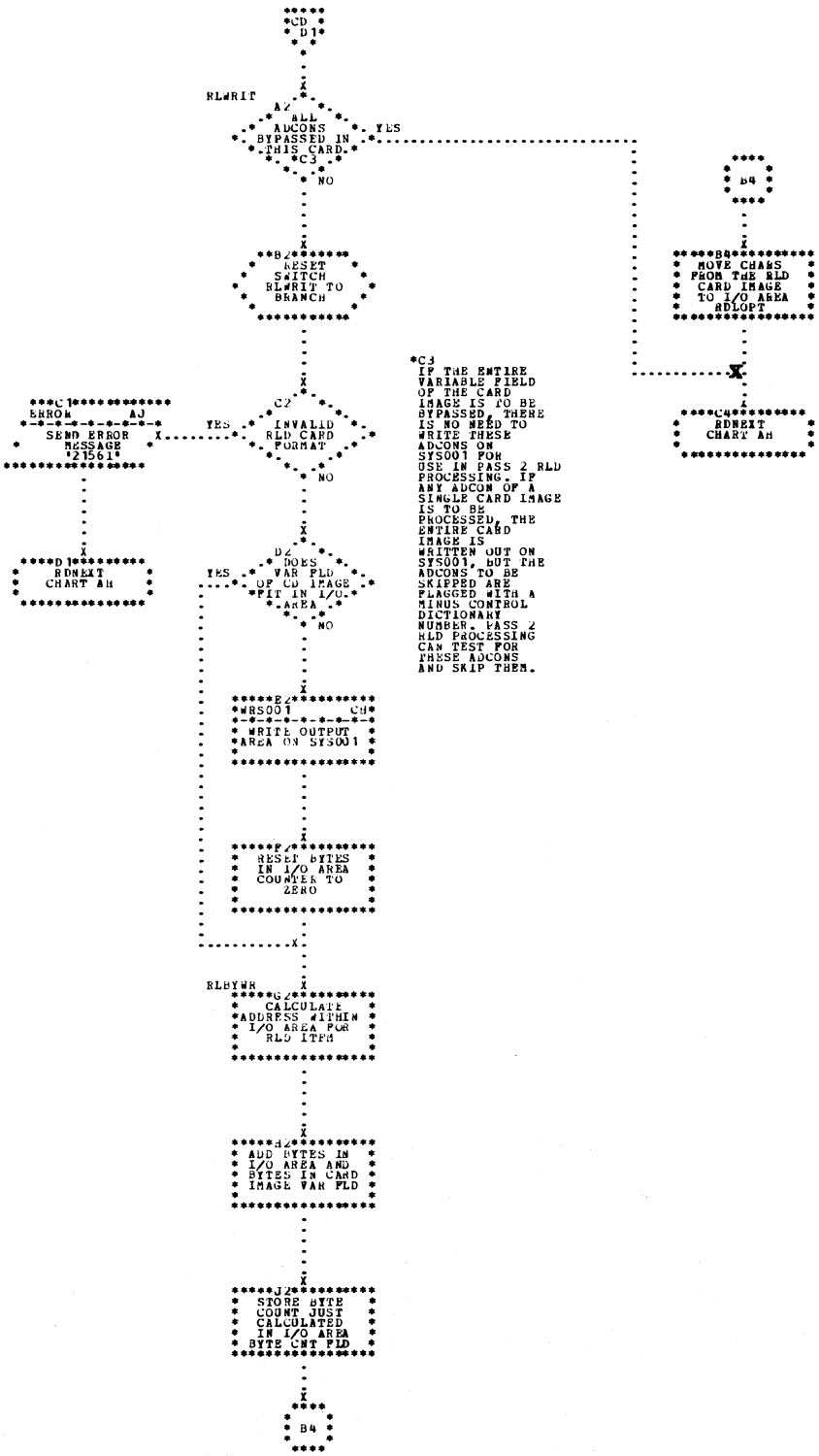


Chart CF. IJBOTH - End Processor (Part 1 of 2). Refer to Chart 06

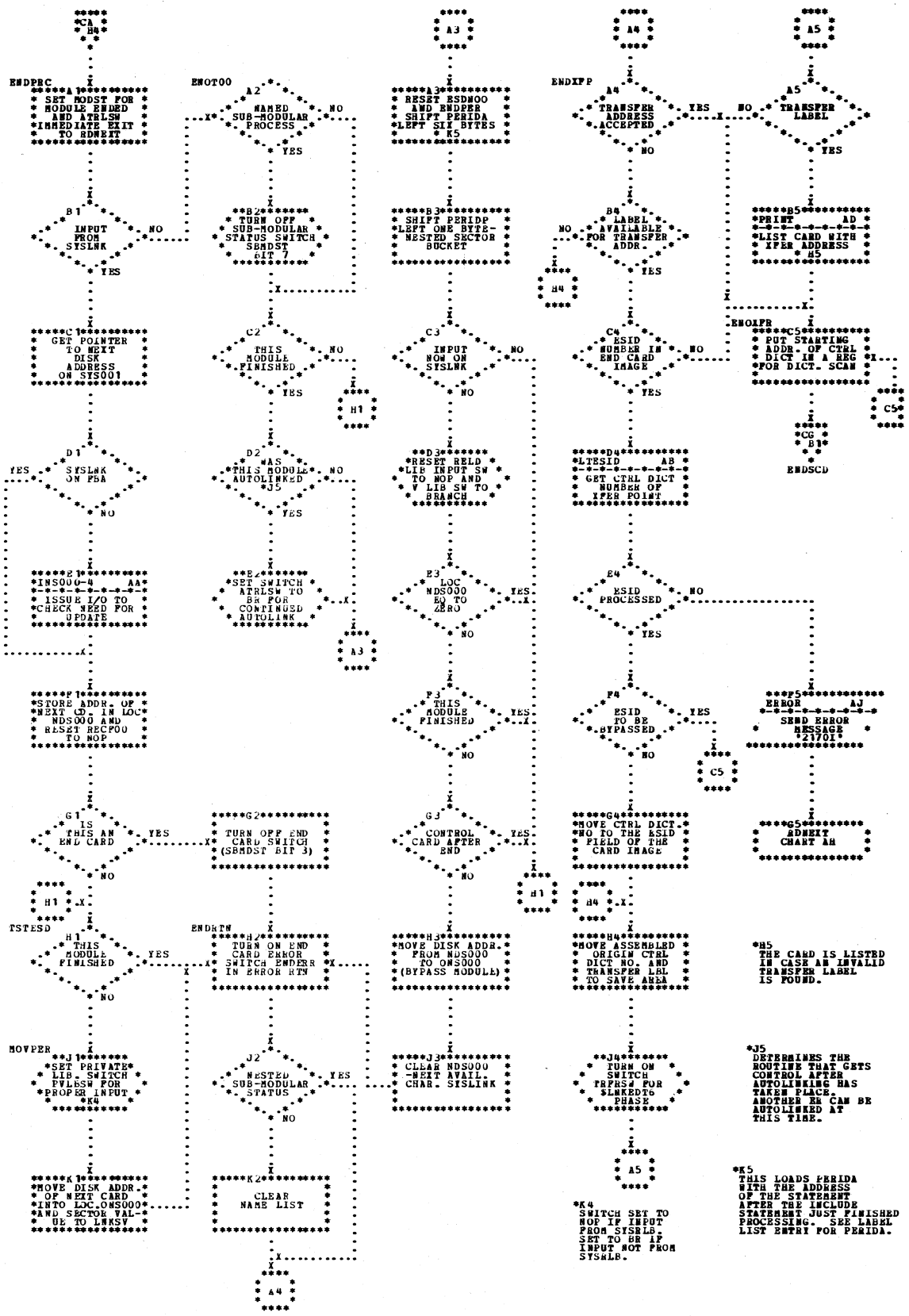


Chart CG. IJEOTH - End Processor (Part 2 of 2). Refer to Chart 06

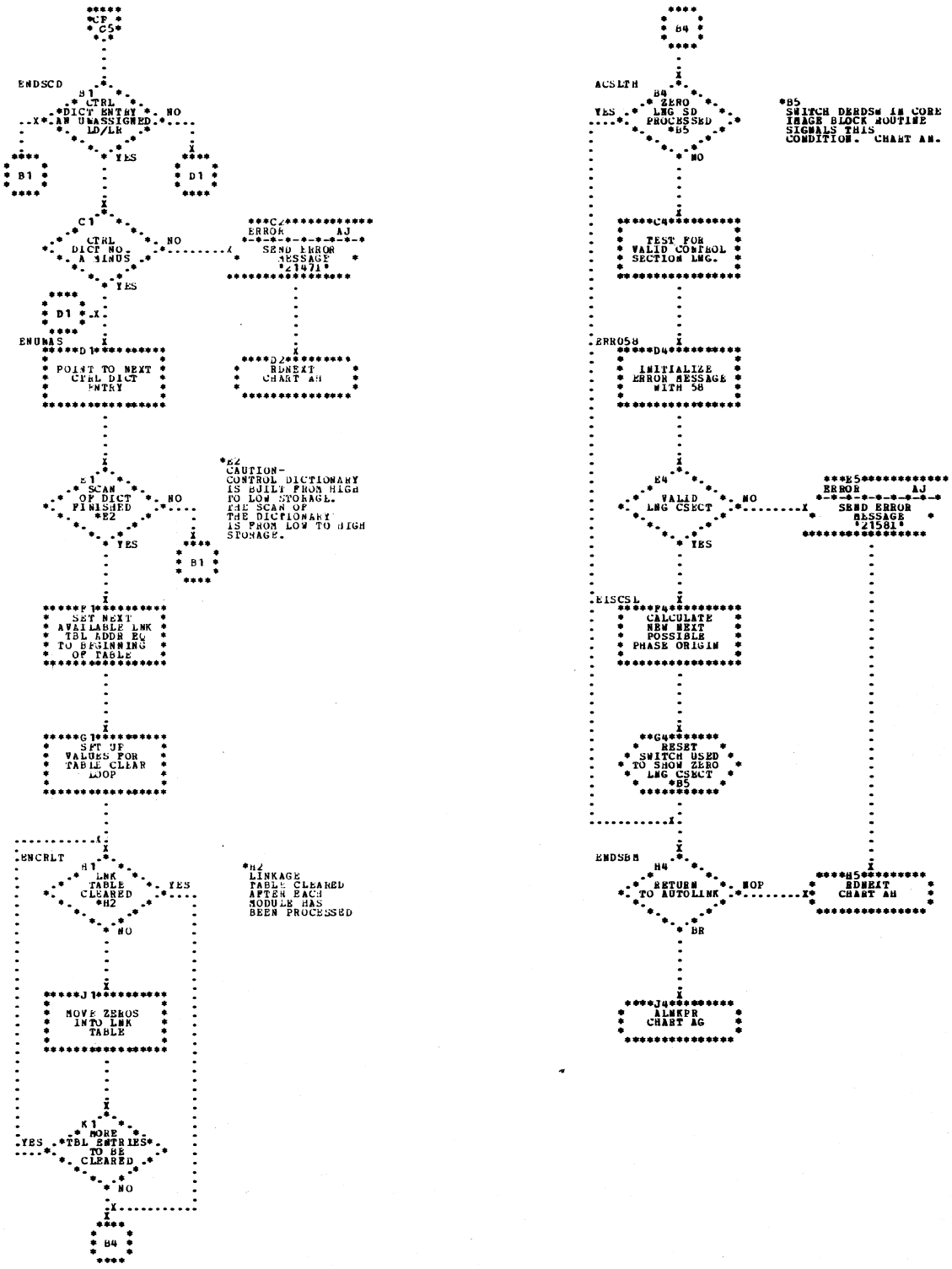


Chart CH. IJBOTH - Write SYSC01 Subroutines. Refer to Chart 06

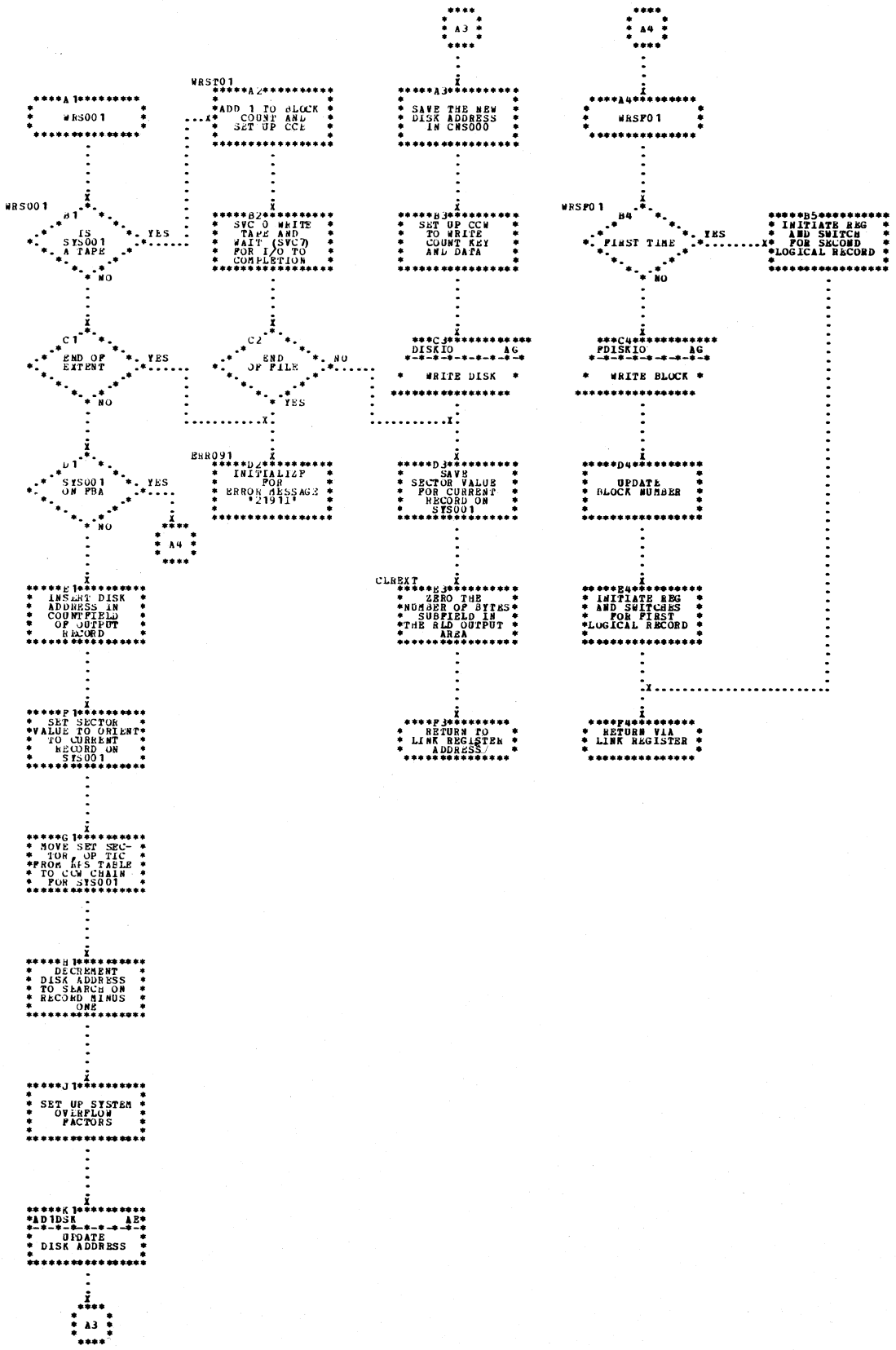


Chart DA. IJBSCN - Initialize Control Card Processor. Refer to Chart 07

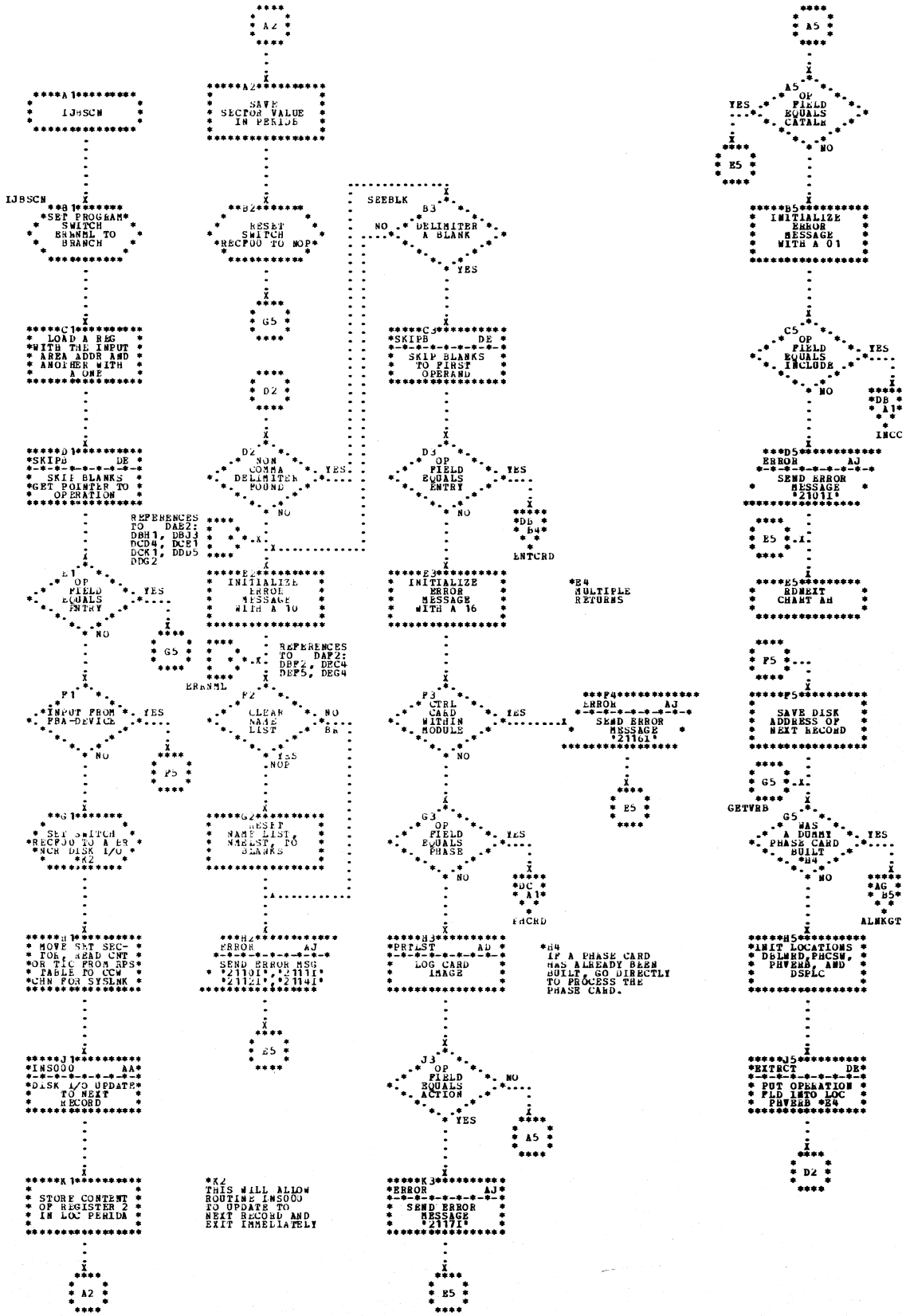


Chart DB. IJBSCN - INCLUDE Card Processor and Entry Card Processor, Refer to Chart 07

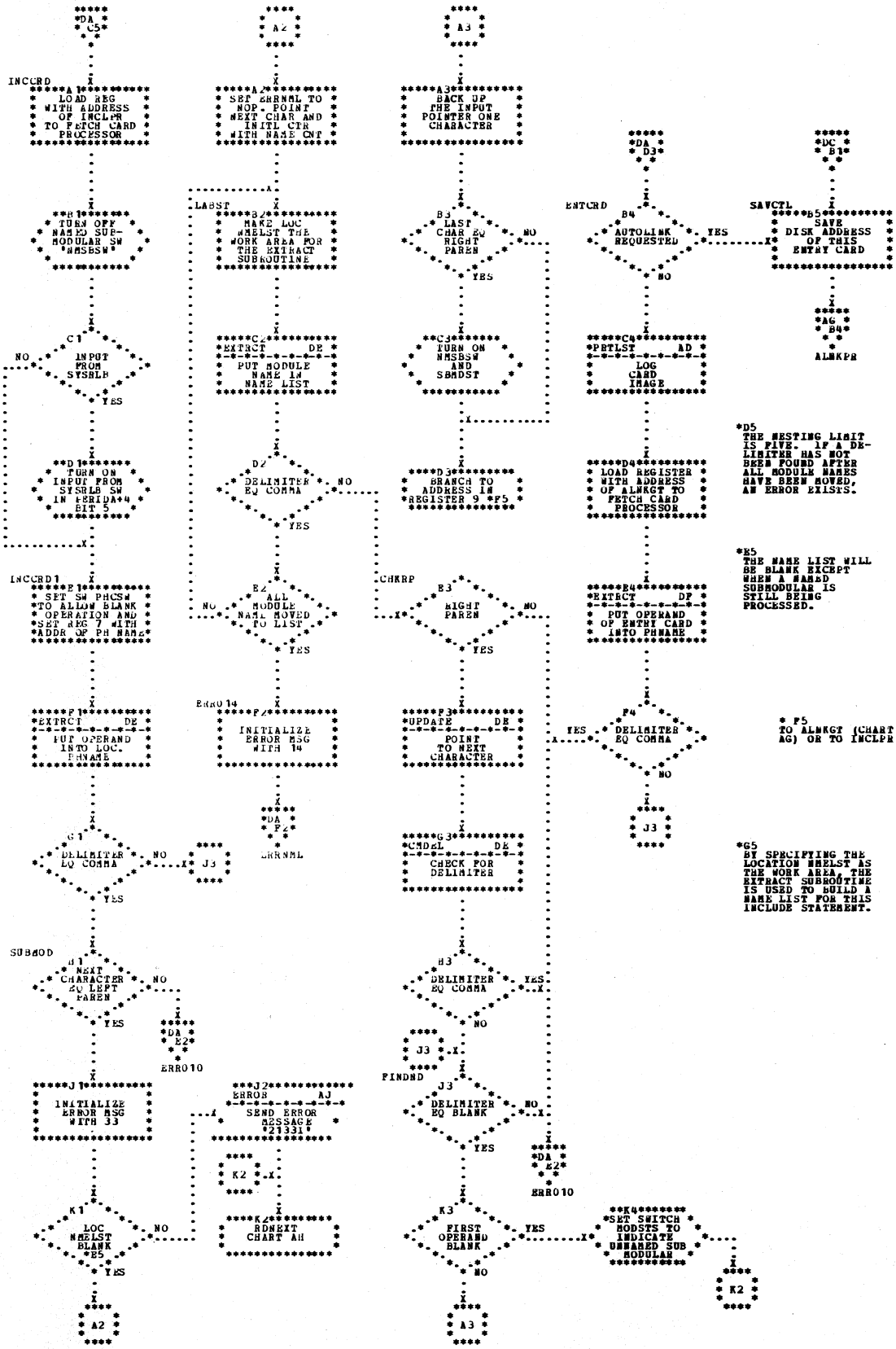


Chart DC. IJBSCN - Phase Card Processor (Part 1 of 2). Refer to Chart 07

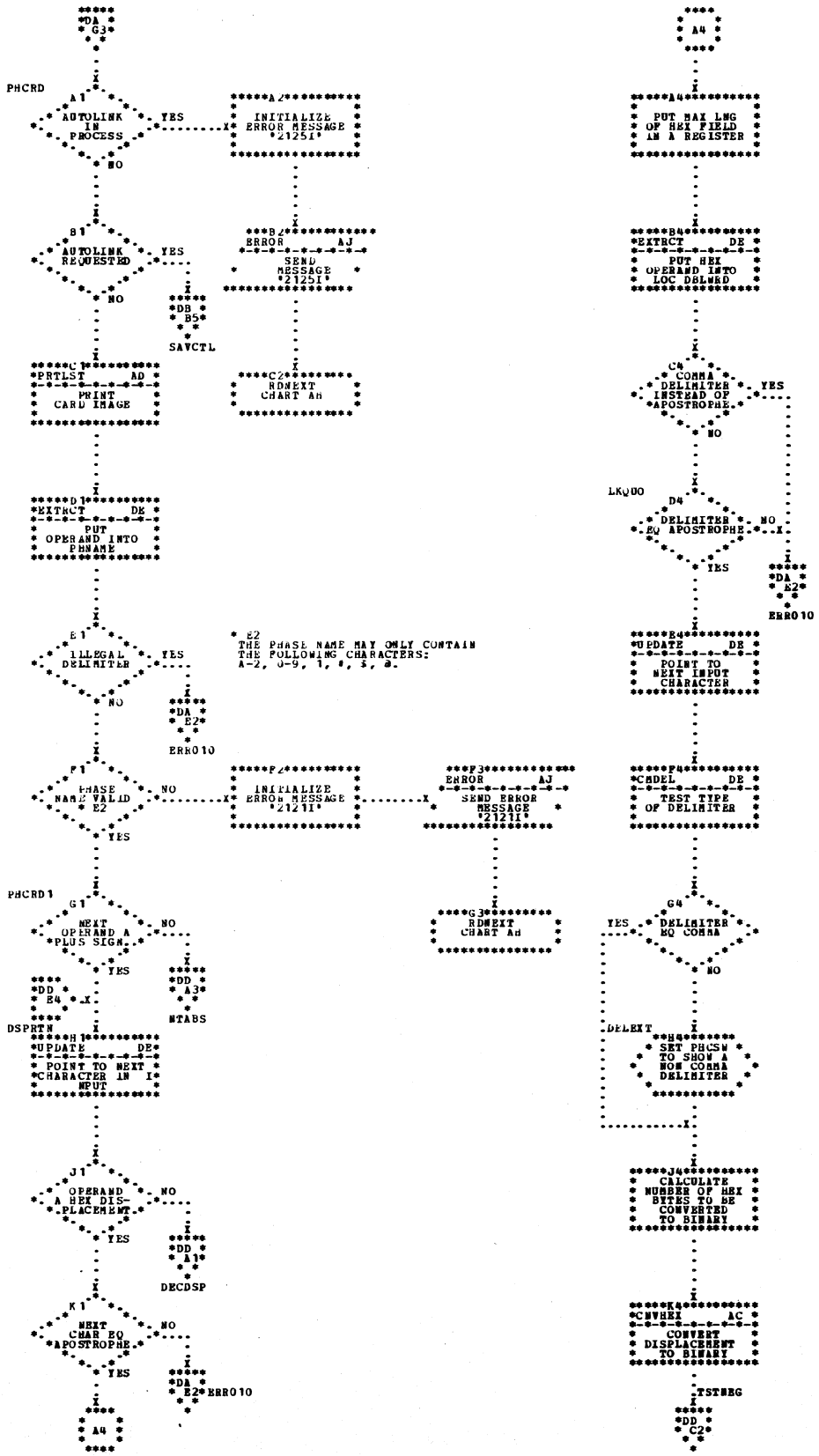


Chart DD. IJBSCN - Phase Card Processcr (Part 2 of 2). Refer to Chart 07

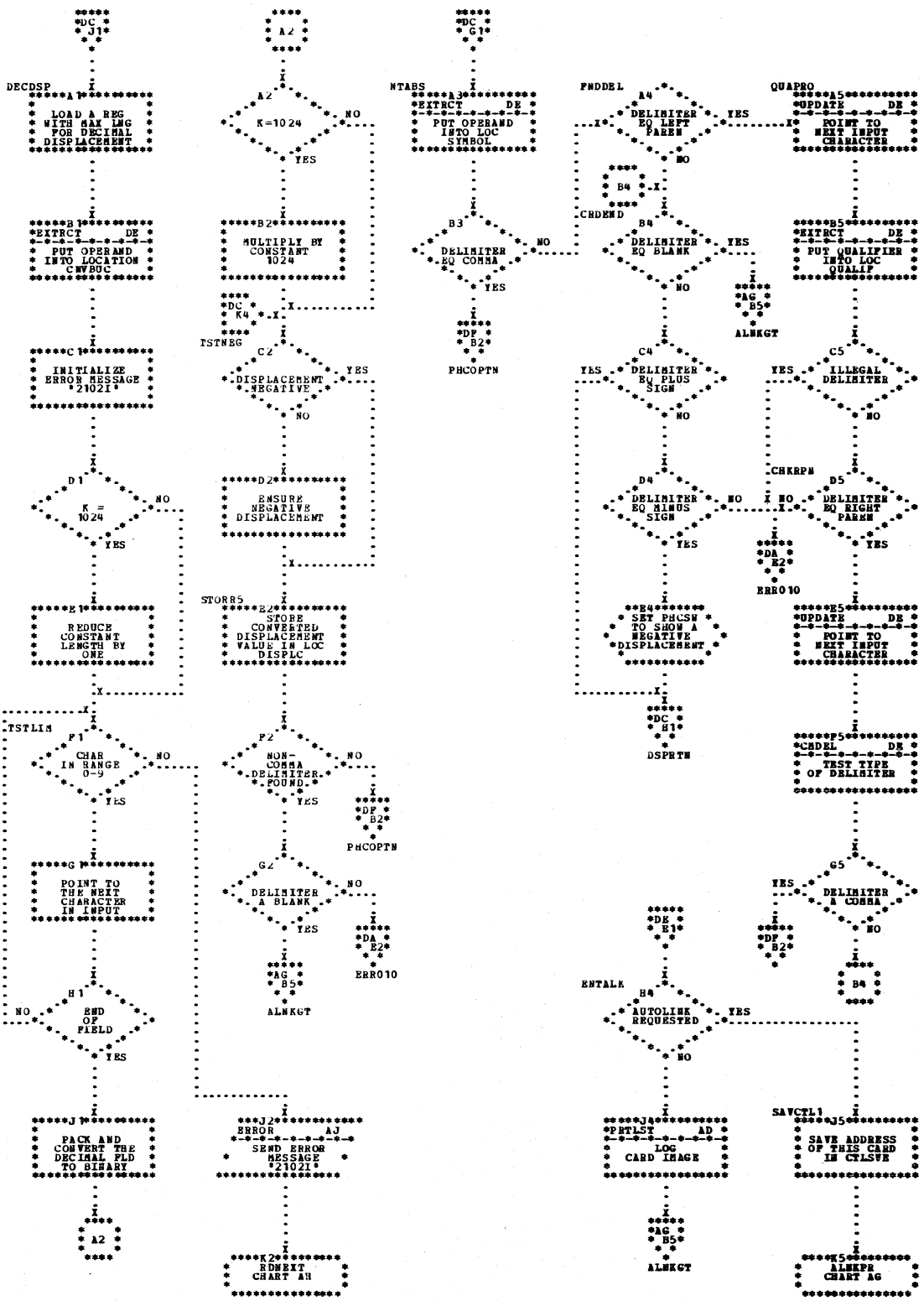


Chart DE. IJBSCN - Skip Blanks and Extract Field Subroutines (Part 1 of 2)
Refer to Chart 07

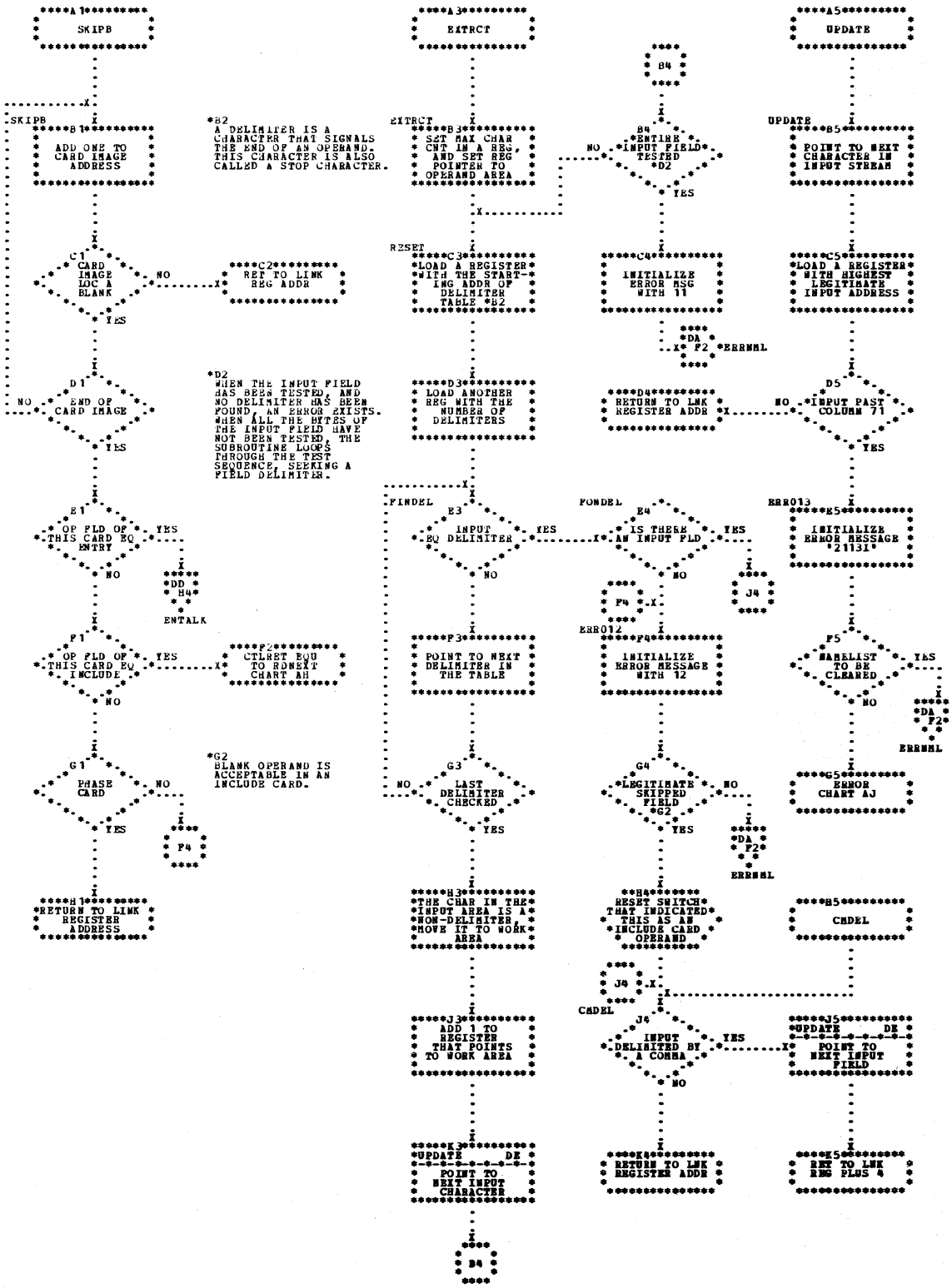


Chart DF. IJBSCN - Skip Blanks and Extract Field Subroutines (Part 2 of 2)
Refer to Chart 07

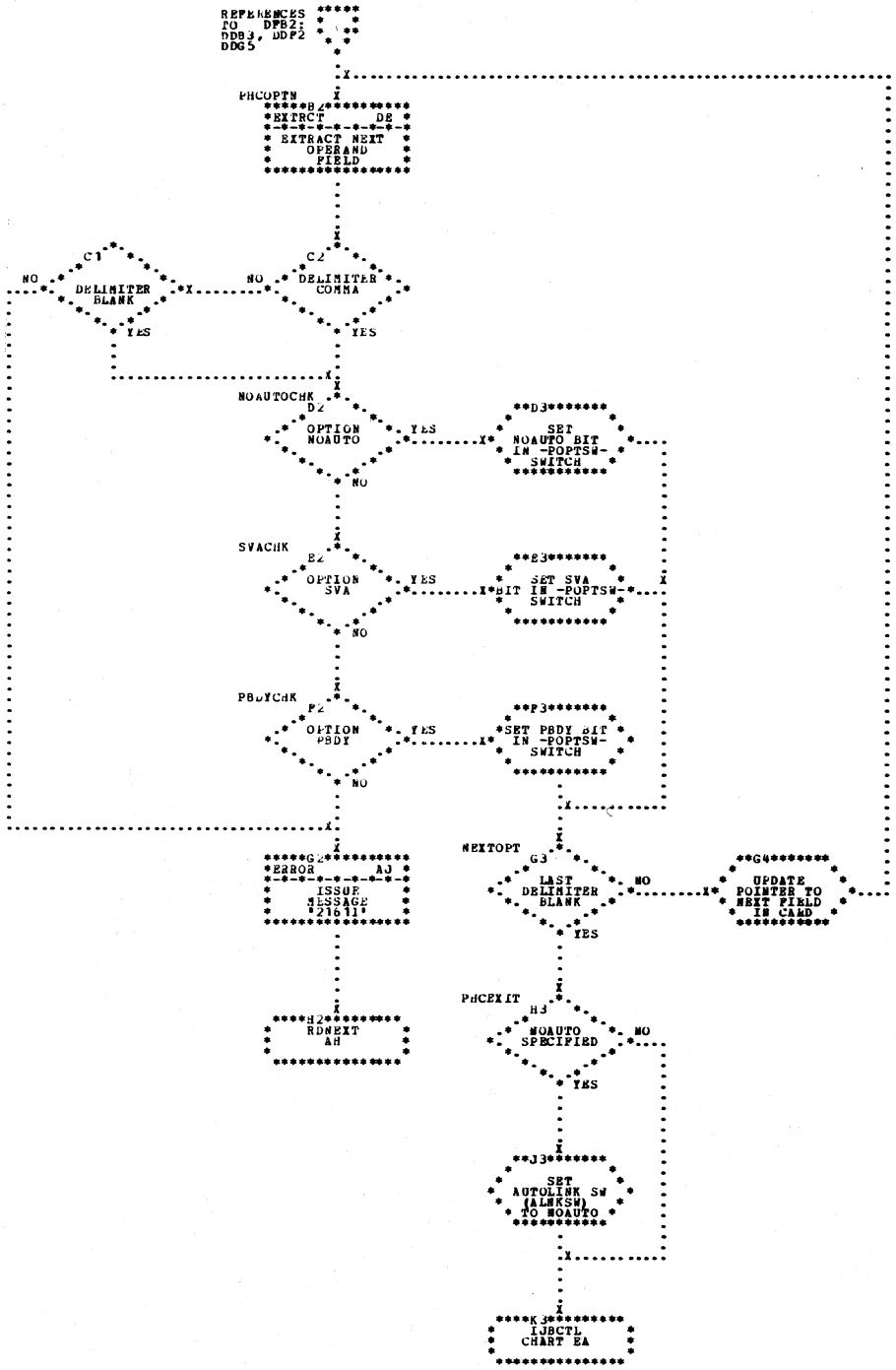


Chart DG. IJBSCN - Phase Card Option Processor (Part 1 of 2). Refer to Chart 07

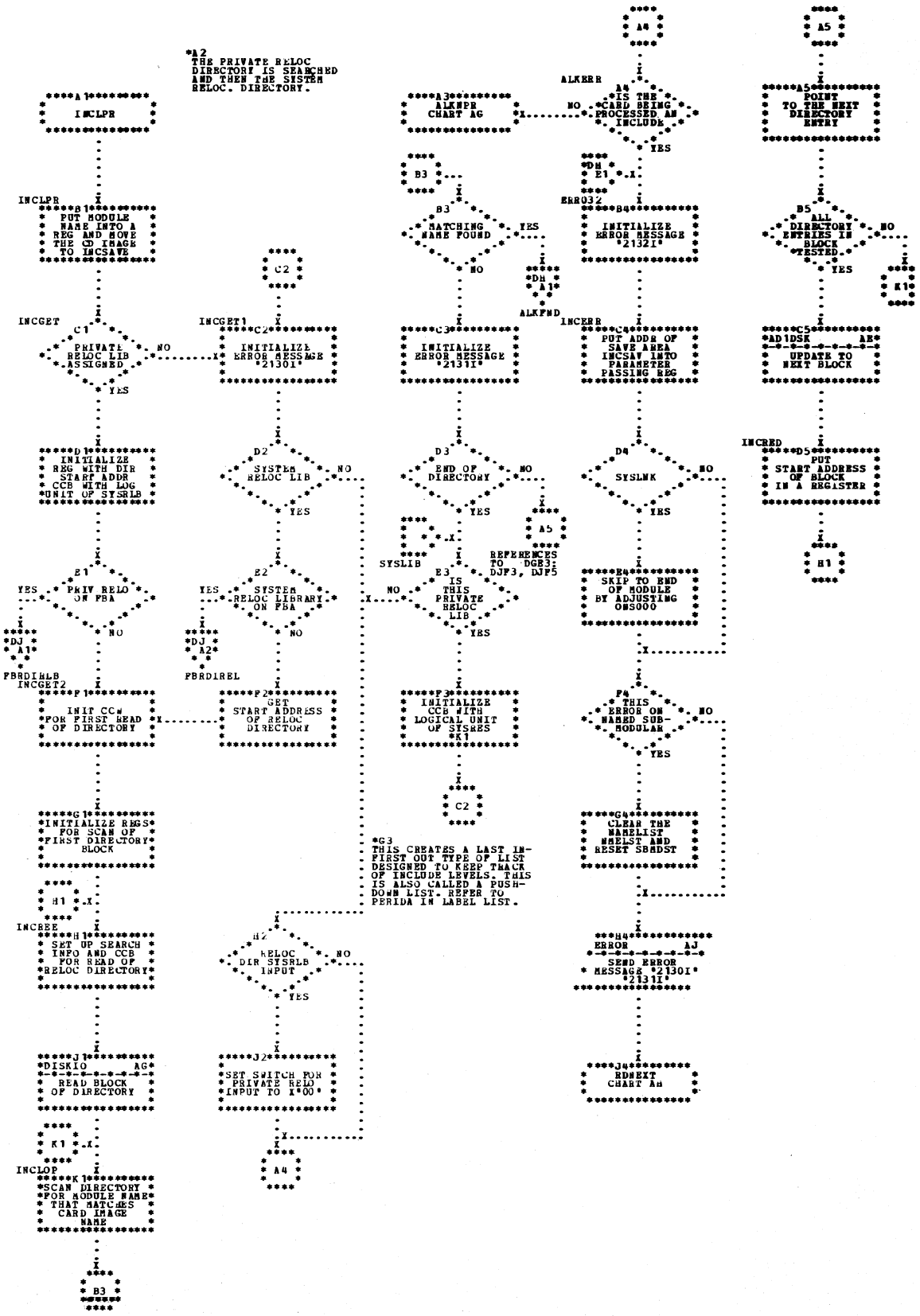


Chart DH. IJBSCN - Phase Card Option Processor (Part 2 of 2). Refer to Chart 07

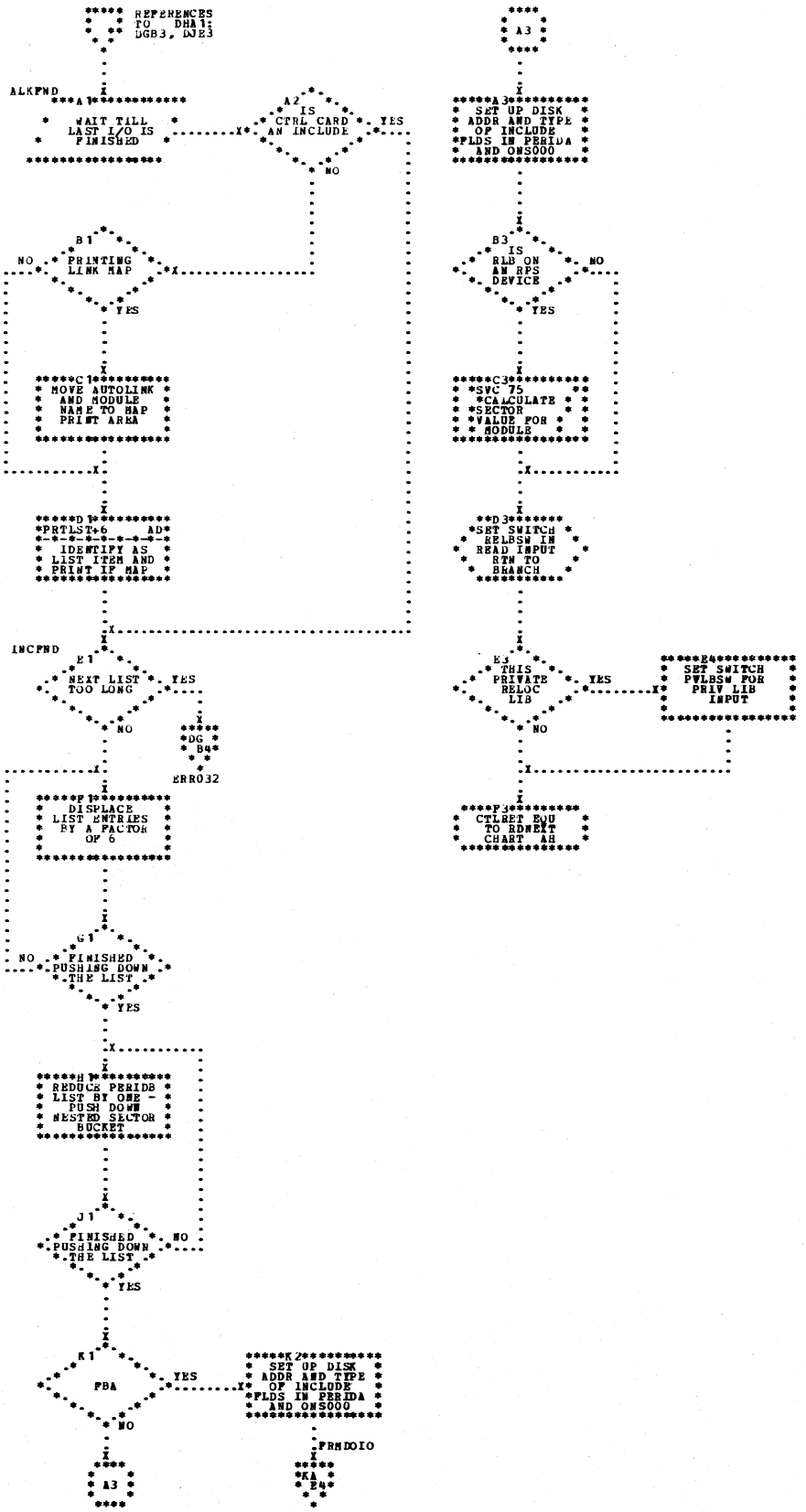


Chart DJ. IJBSCN - Scanning Directory if Relocatable Library on FBA. Refer to Chart 07

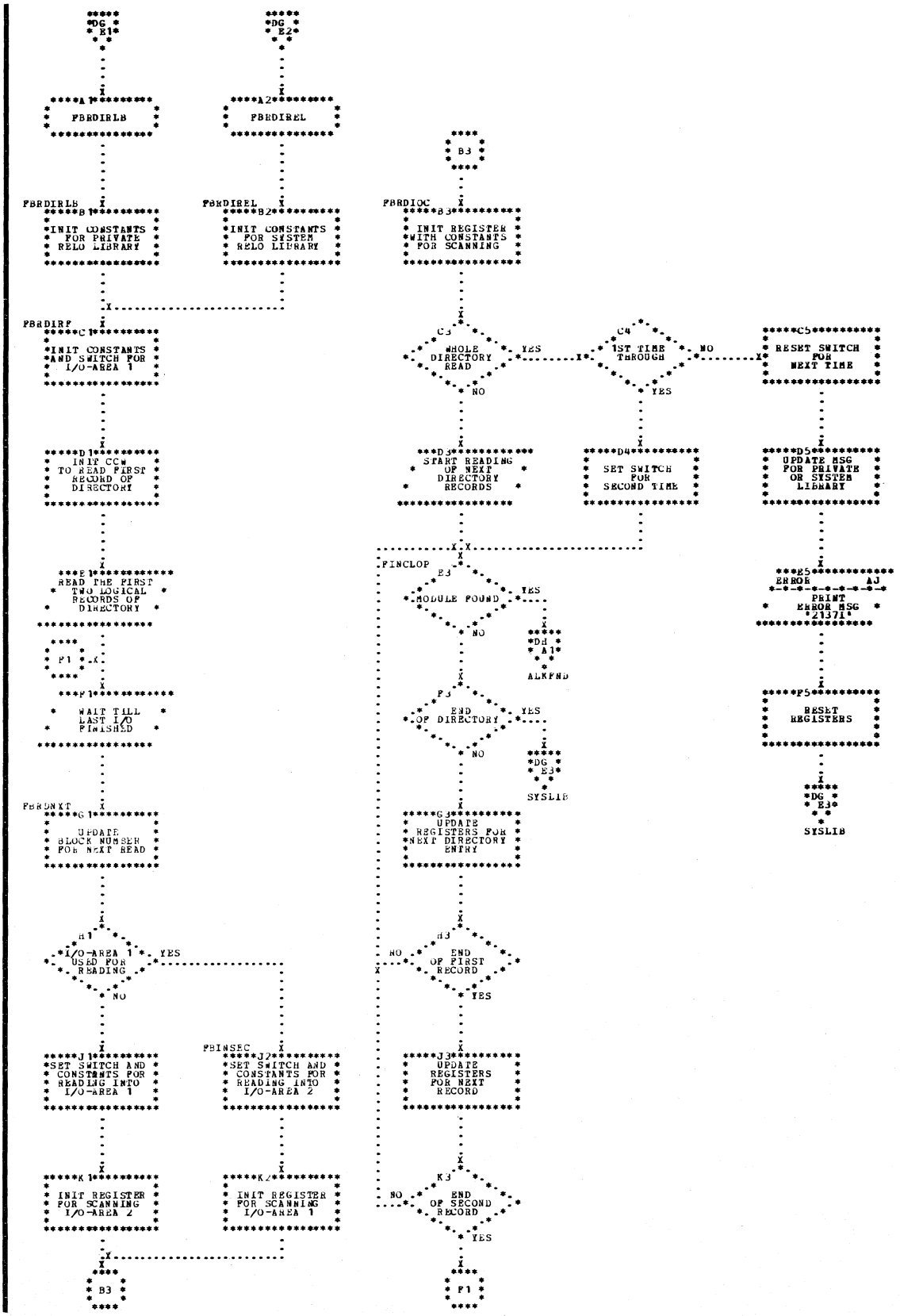


Chart EA. IJBCTL - Phase/Entry Processor (Part 1 of 6). Refer to Chart 08

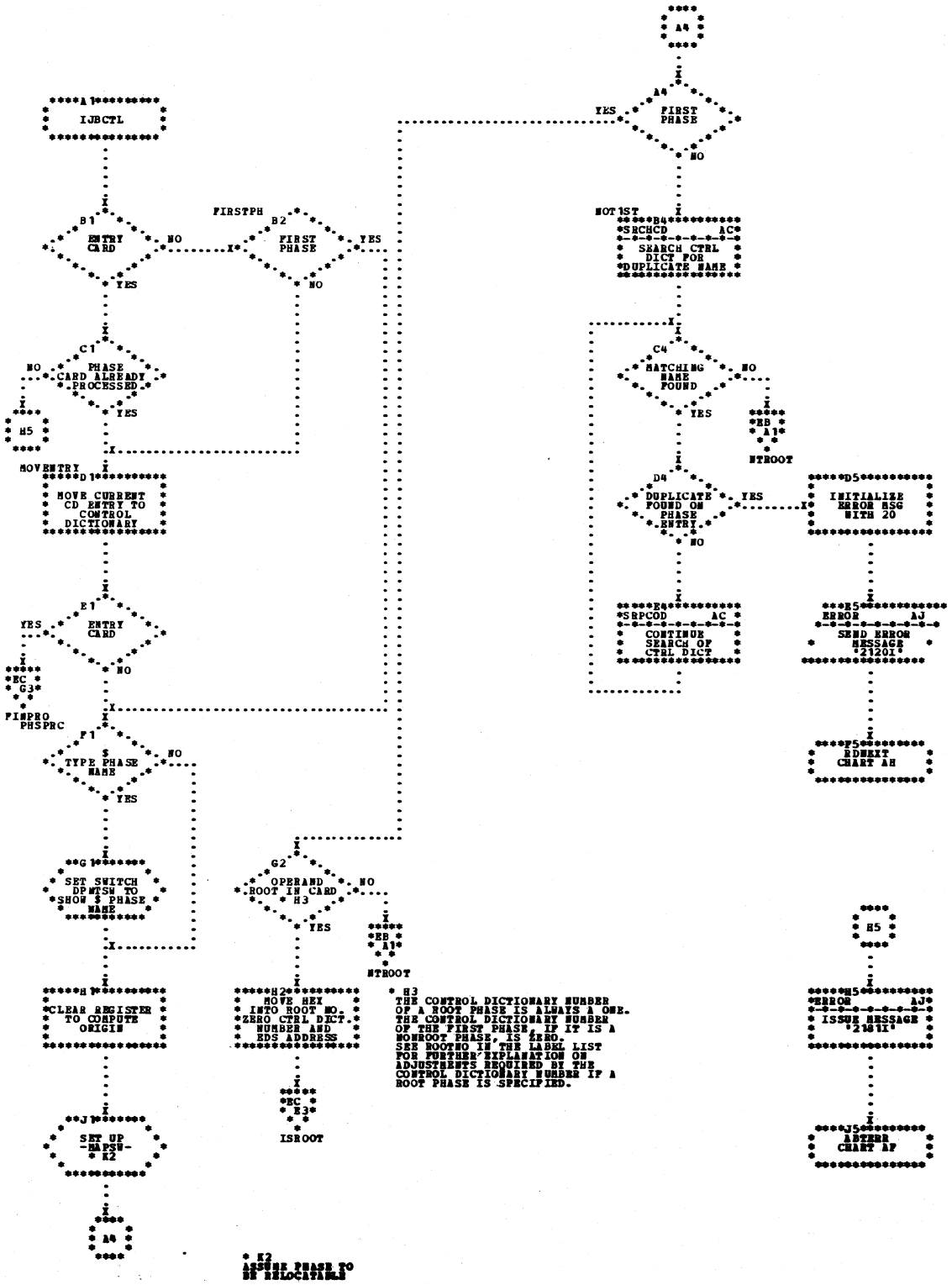


Chart EB. IJBCTL - Phase/Entry Processor (Part 2 of 6). Refer to Chart 08

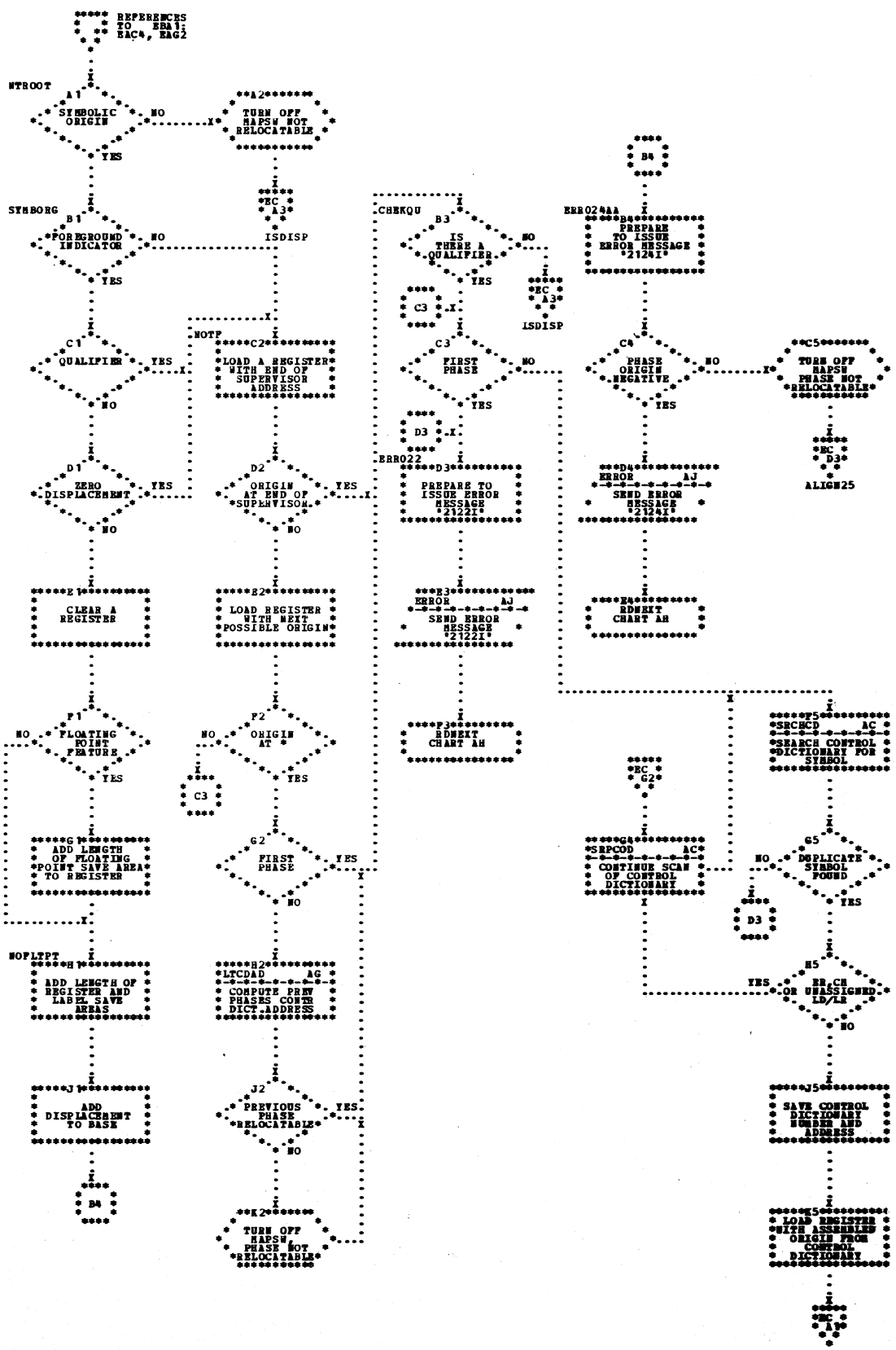


Chart EC. IJBCTL - Phase/Entry Processor (Part 3 of 6). Refer to Chart 08

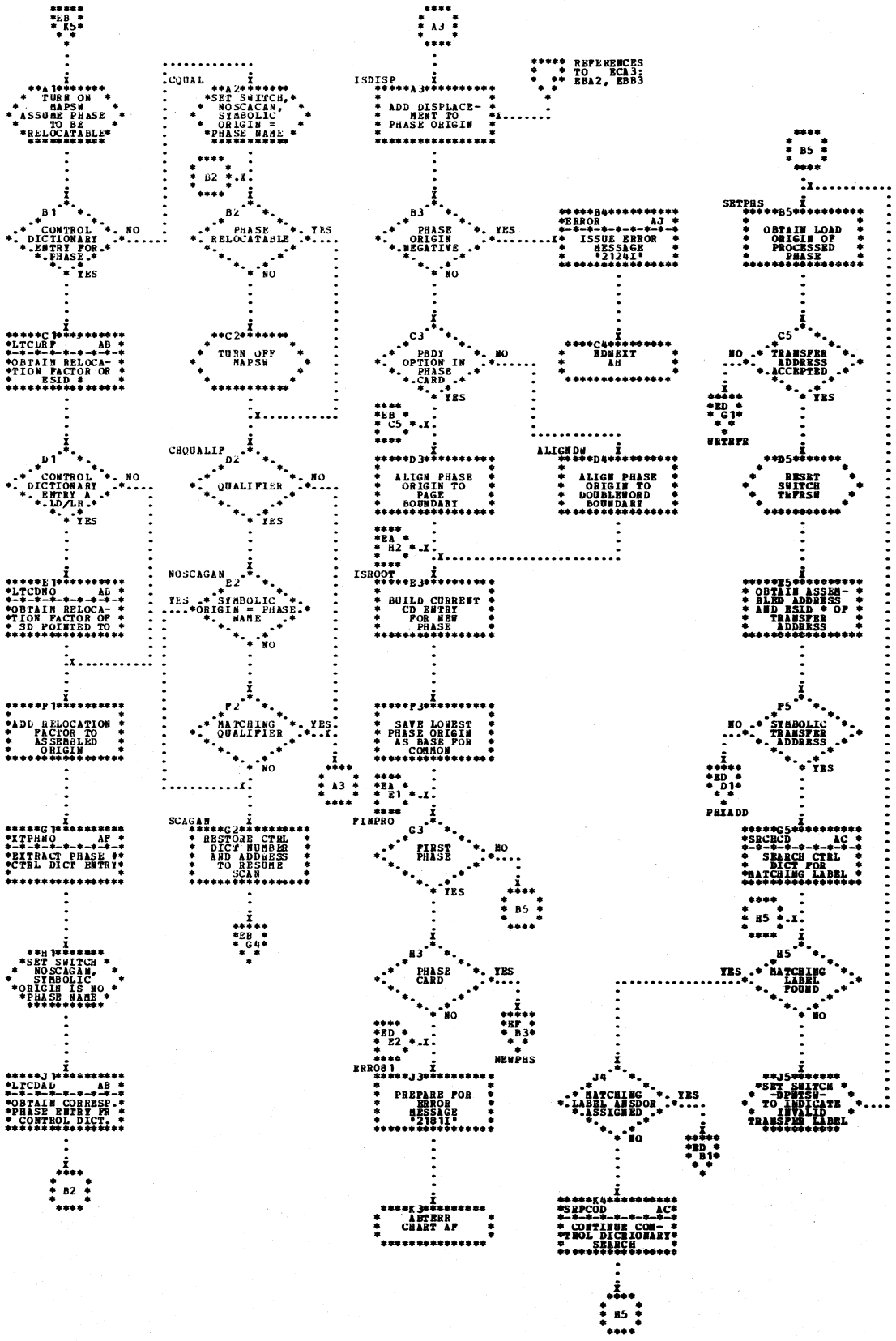


Chart ED. IJBCTL - Phase/Entry Processor (Part 4 of 6). Refer to Chart 08

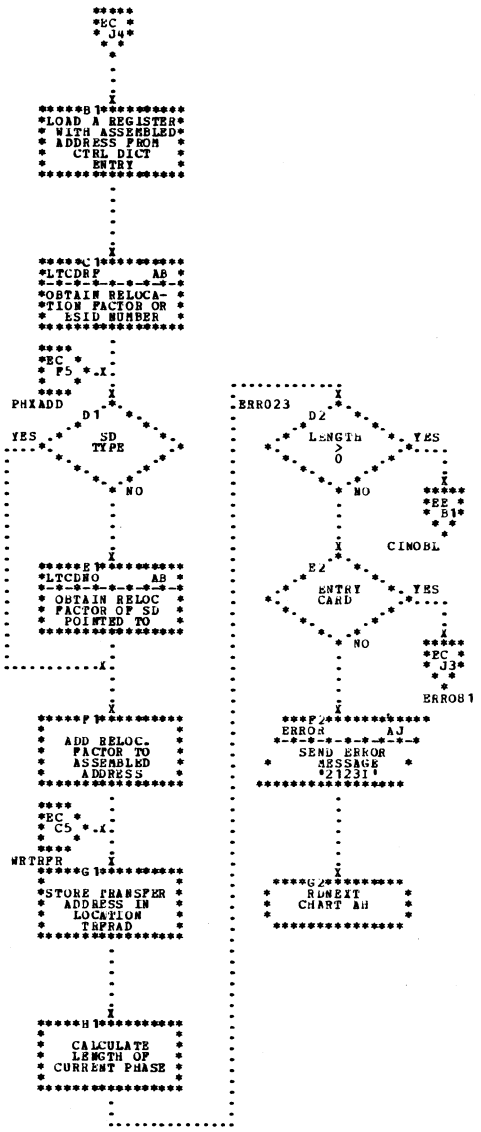


Chart EE. IJBCTL - Phase/Entry Processor (Part 5 of 6) Refer to Chart 08

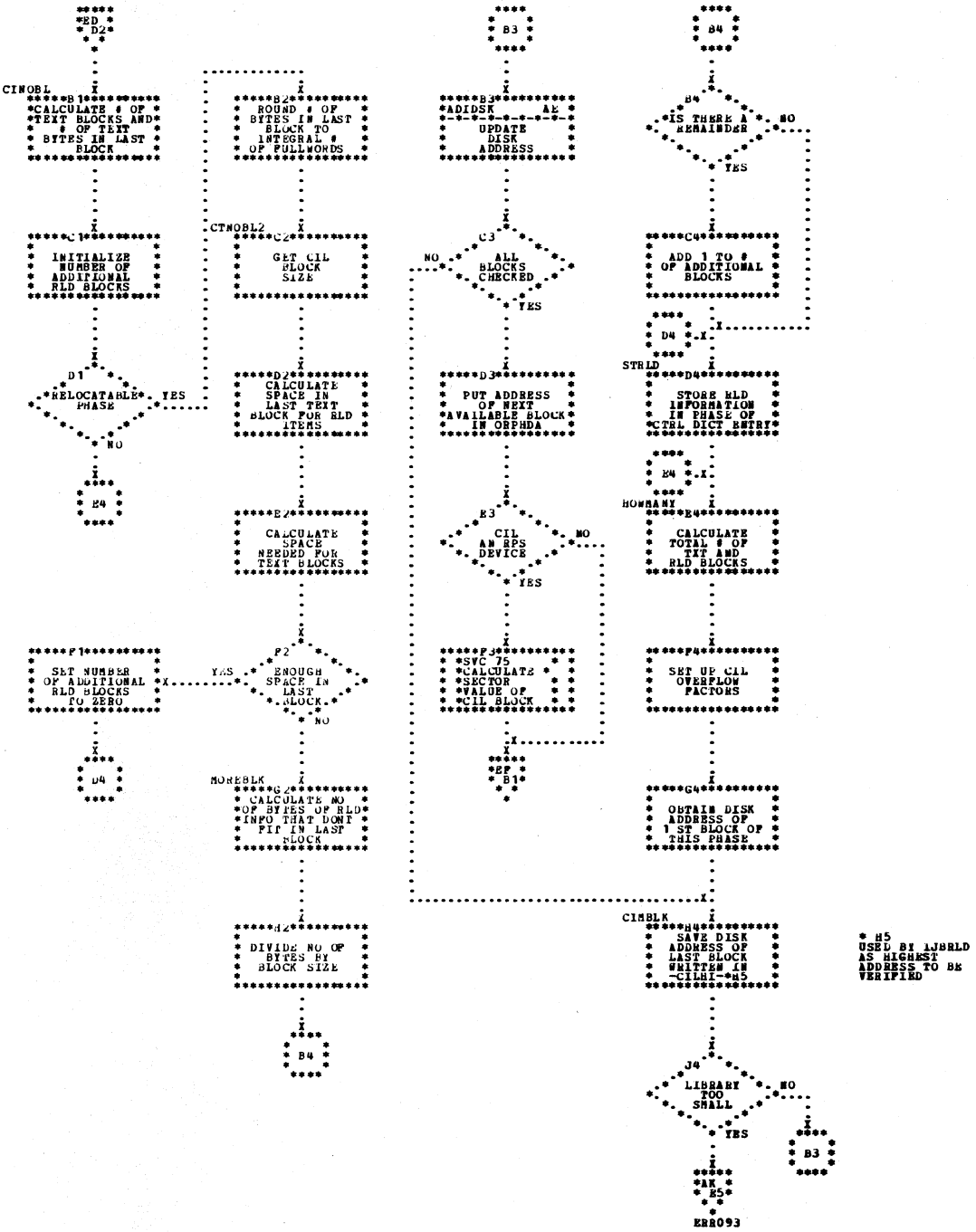


Chart EF. IJBCTL - Phase/Entry Processor (Part 6 of 6). Refer to Chart 08

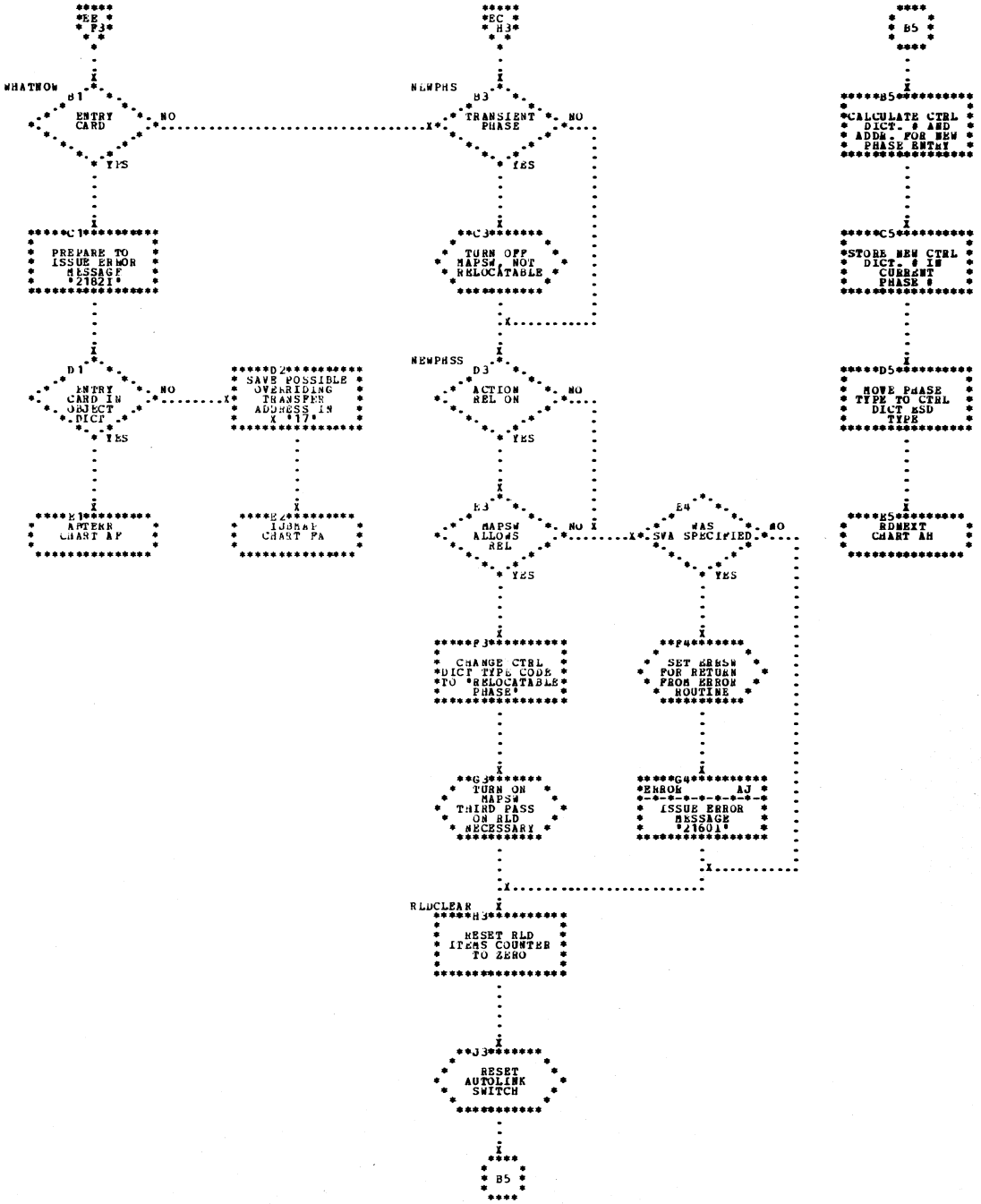


Chart FA. IJBMAP - Print Map (Part 1 of 5). Refer to Chart 09

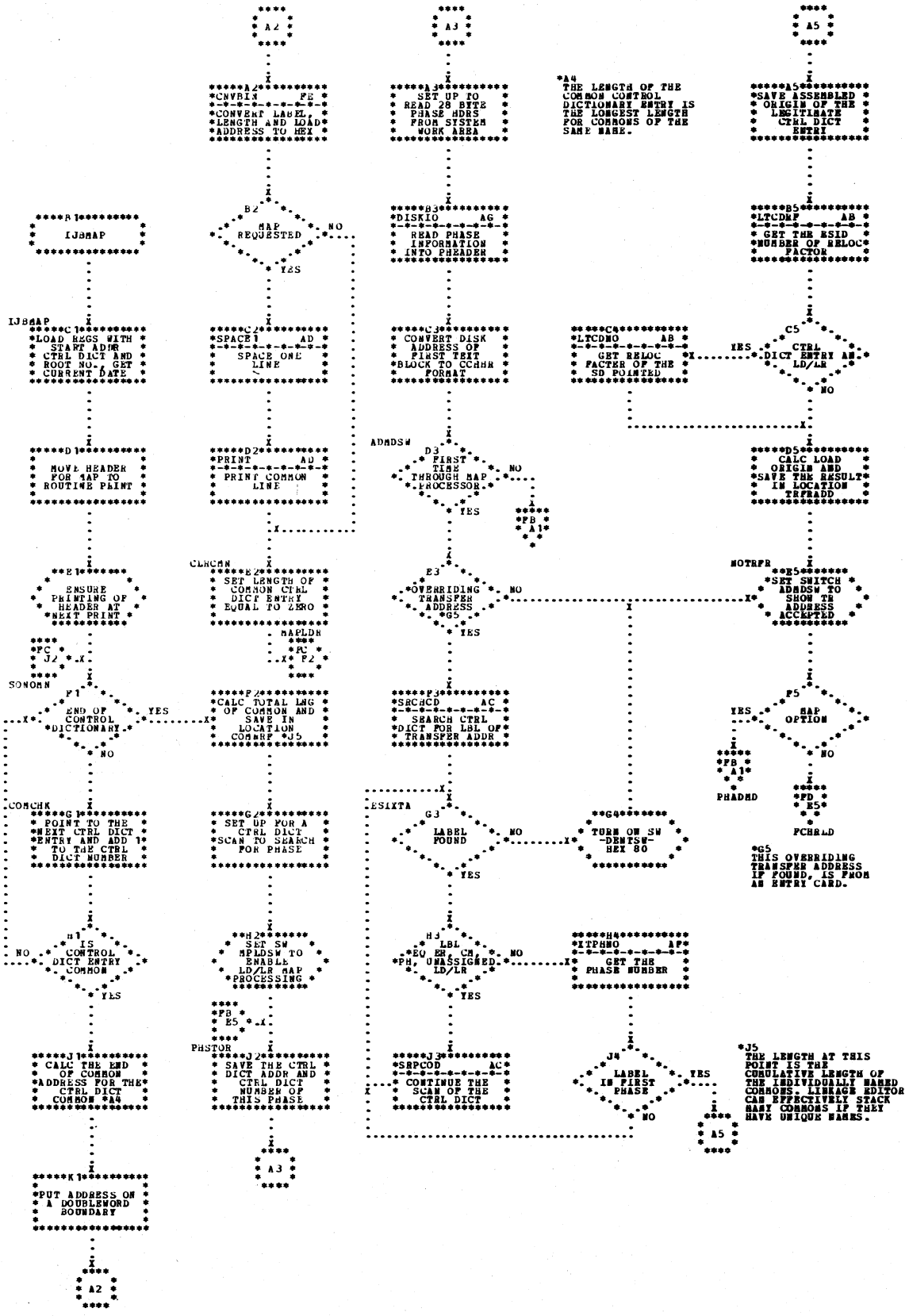
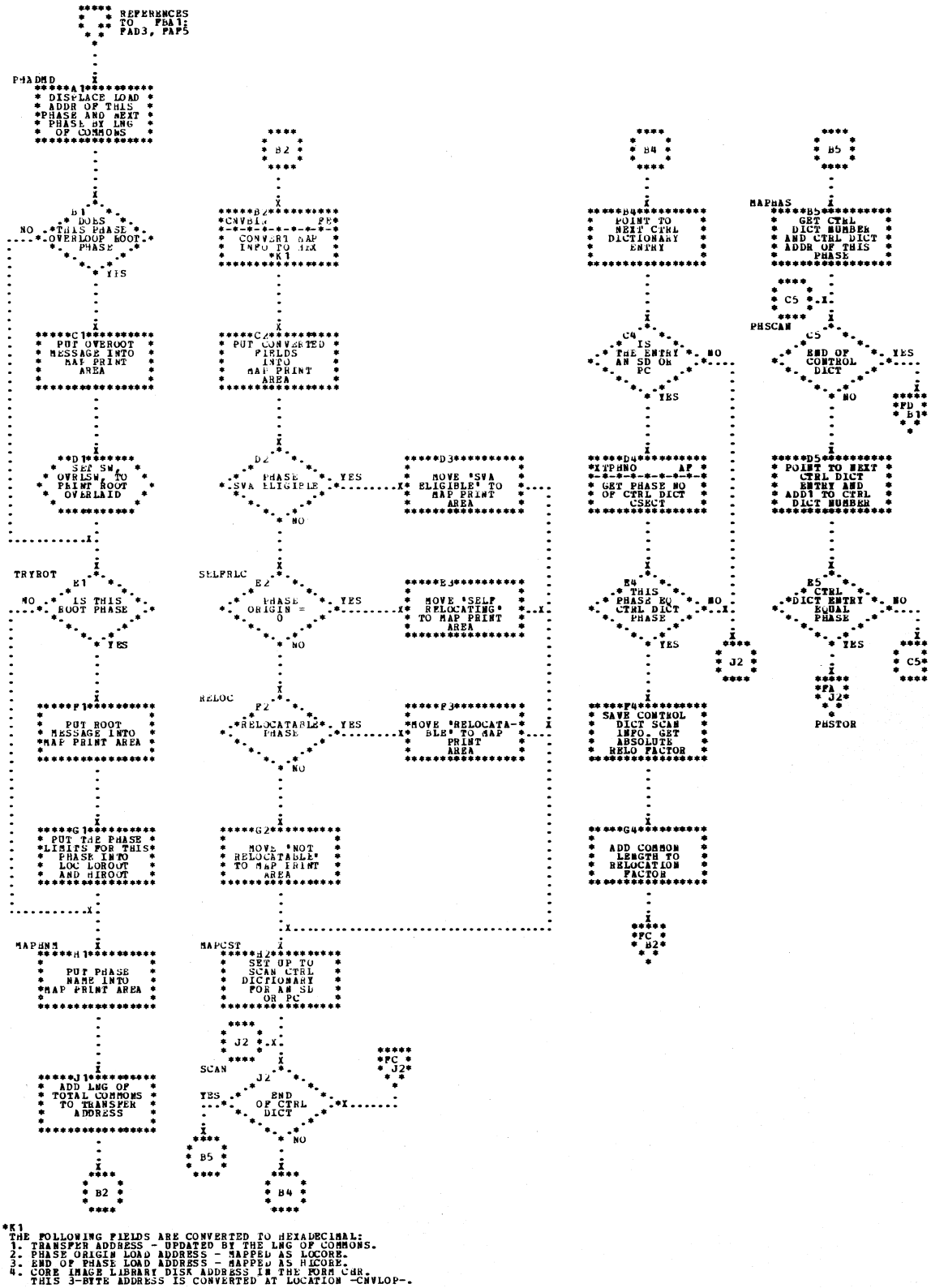


Chart FB. IJBMAP - Print Map (Part 2 of 5). Refer to Chart 09



*K1
THE FOLLOWING FIELDS ARE CONVERTED TO HEXADECIMAL:
1. TRANSFER ADDRESS - UPDATED BY THE LNG OF COMMONS.
2. PHASE ORIGIN LOAD ADDRESS - MAPPED AS LOCORE.
3. END OF PHASE LOAD ADDRESS - MAPPED AS HICORE.
4. CORE IMAGE LIBRARY DISK ADDRESS IN THE FORM CHR.
THIS 3-BYTE ADDRESS IS CONVERTED AT LOCATION -CNVLOP-.

Chart FC. IJEMAP - Print Map (Part 3 of 5). Refer to Chart 09

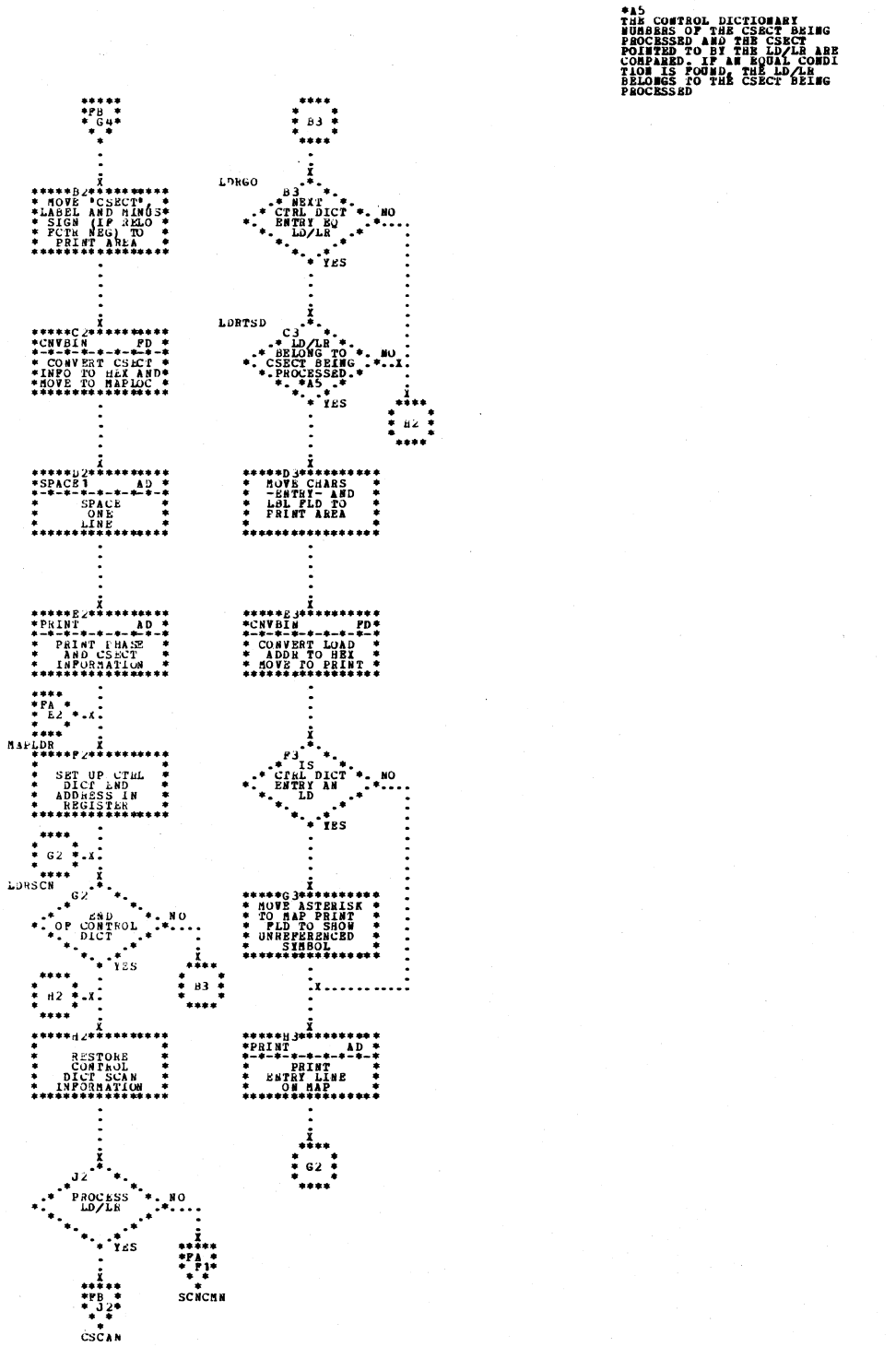


Chart FD. IJBMAP - Print Map (Part 4 of 5). Refer to Chart 09

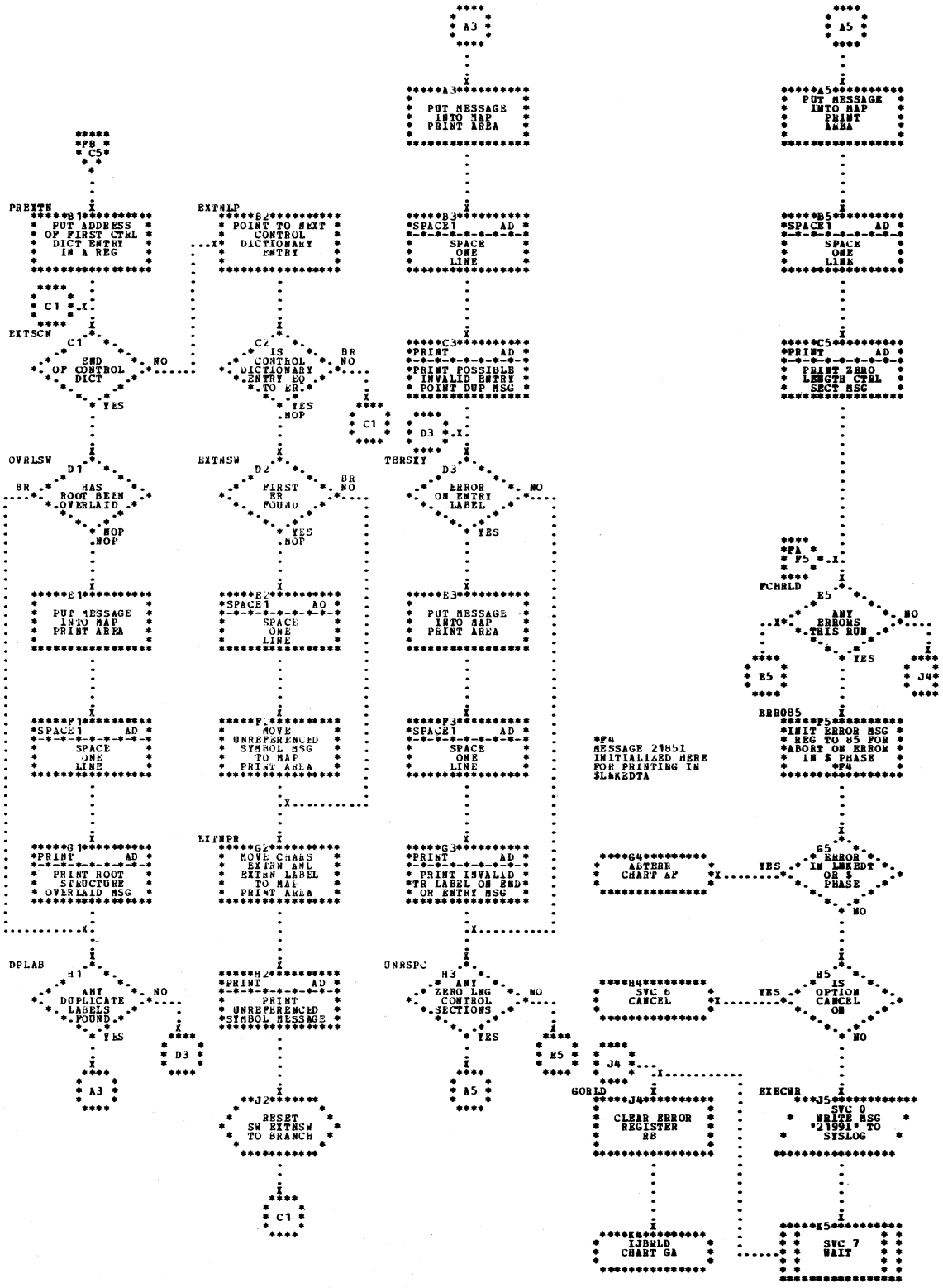


Chart FE. IJBMAP - Print Map (Part 5 of 5). Refer to Chart 09

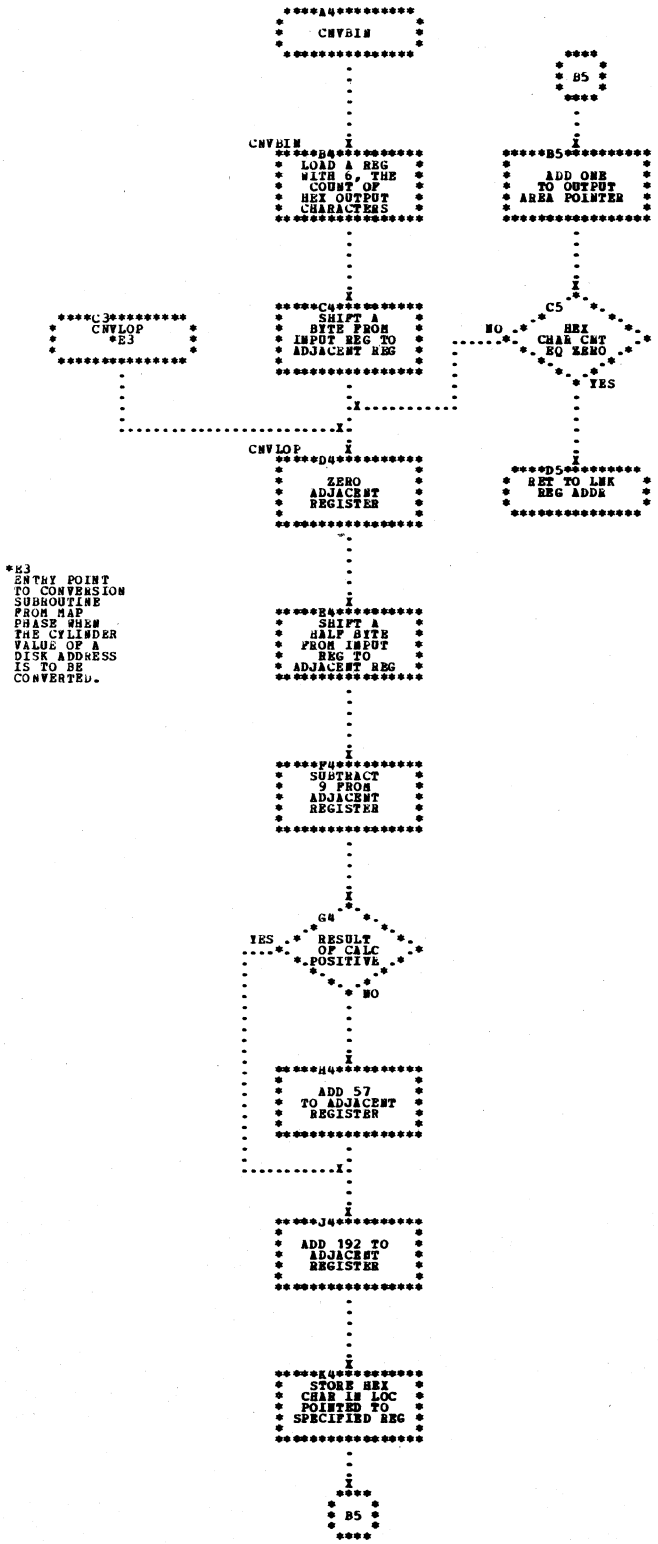


Chart GA. IJBRLD - Pass 2 P-Pointer Processing. Refer to Chart 10

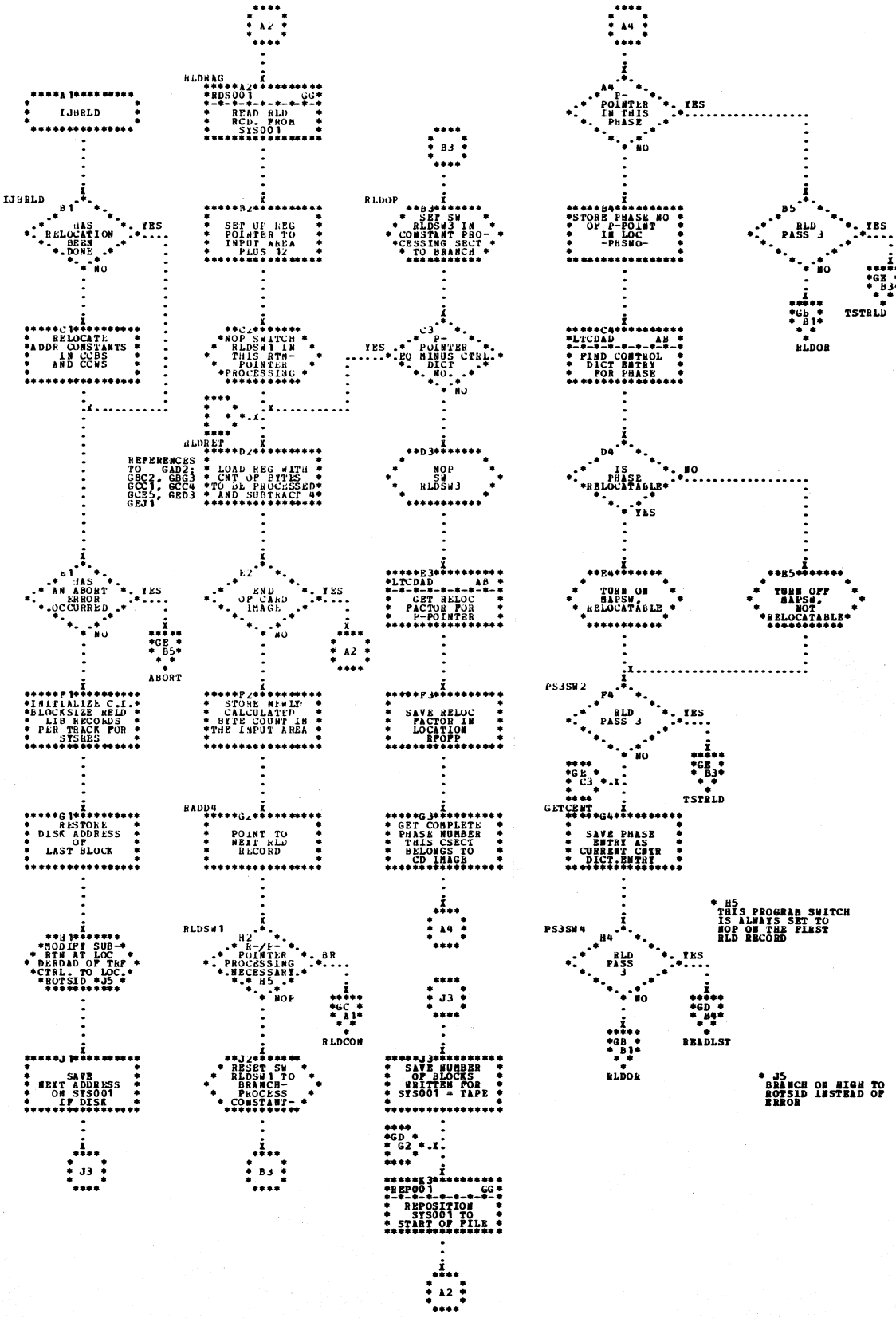


Chart GB. IJBRLD - Pass 2 R-Pointer Processing. Refer to Chart 10

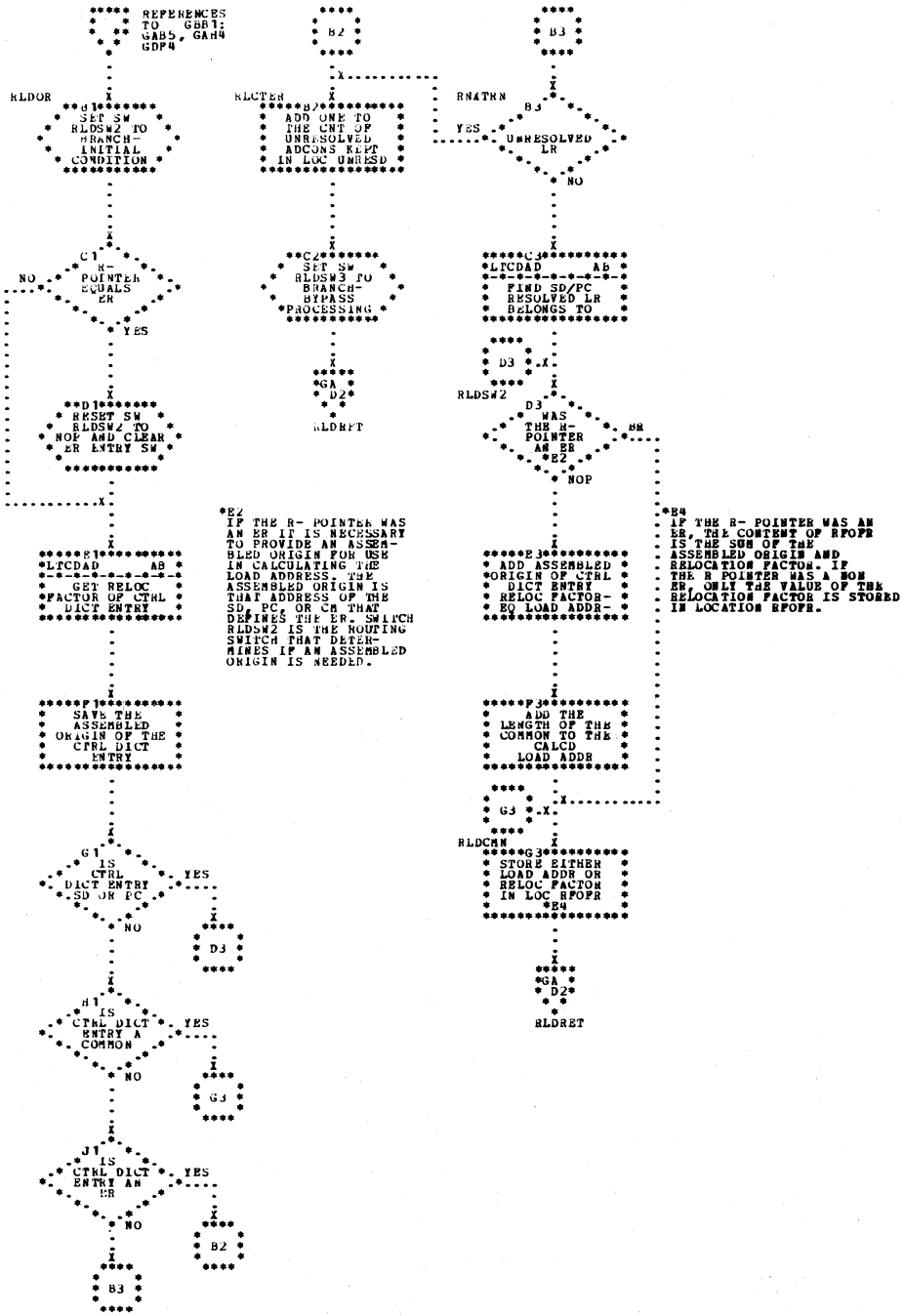


Chart GC. IJBRLD - Pass 2 RLD Constant Processing. Refer to Chart 11

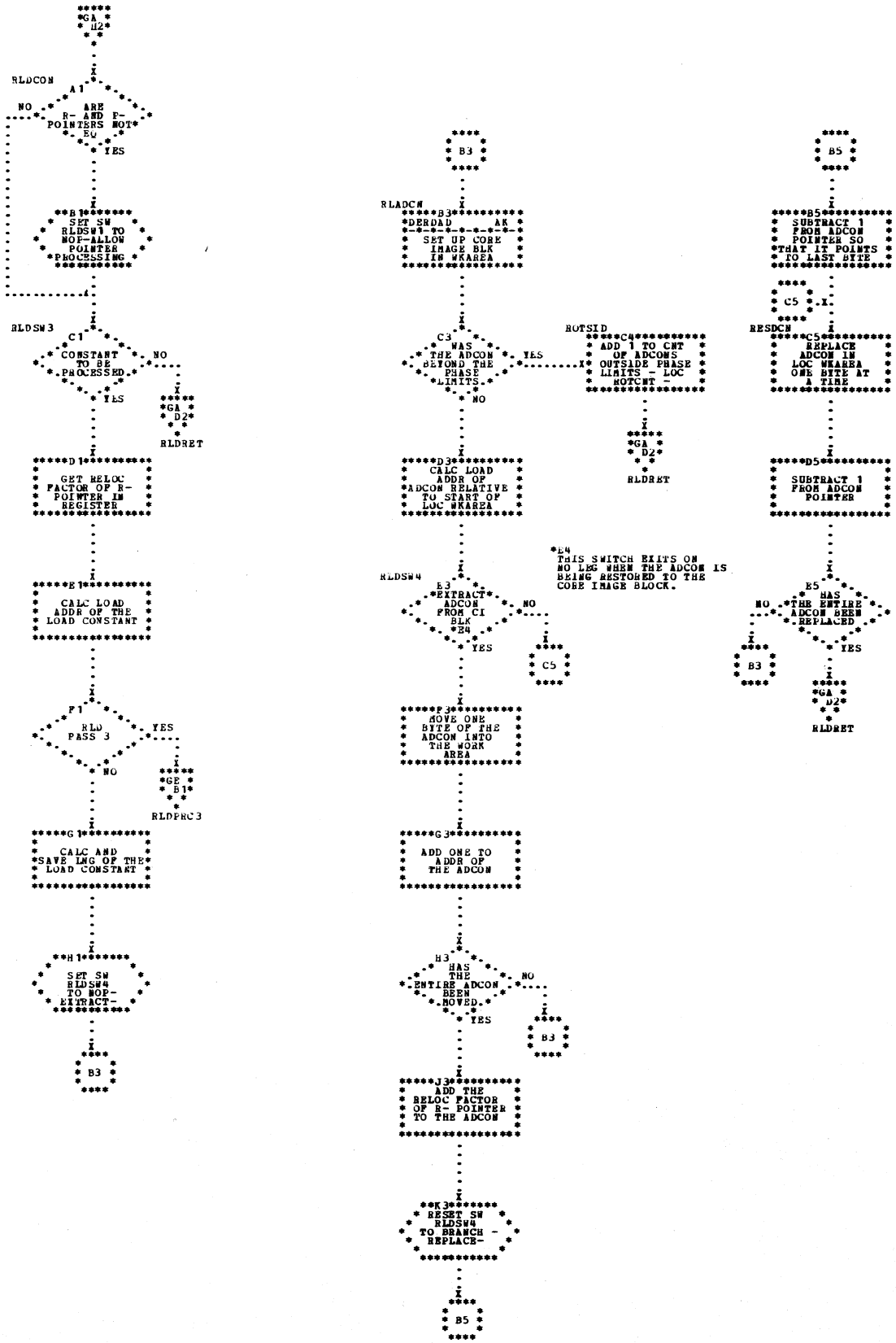


Chart GD. IJBRLD - Pass 3 RLD Constant Processing. Refer to Chart 11

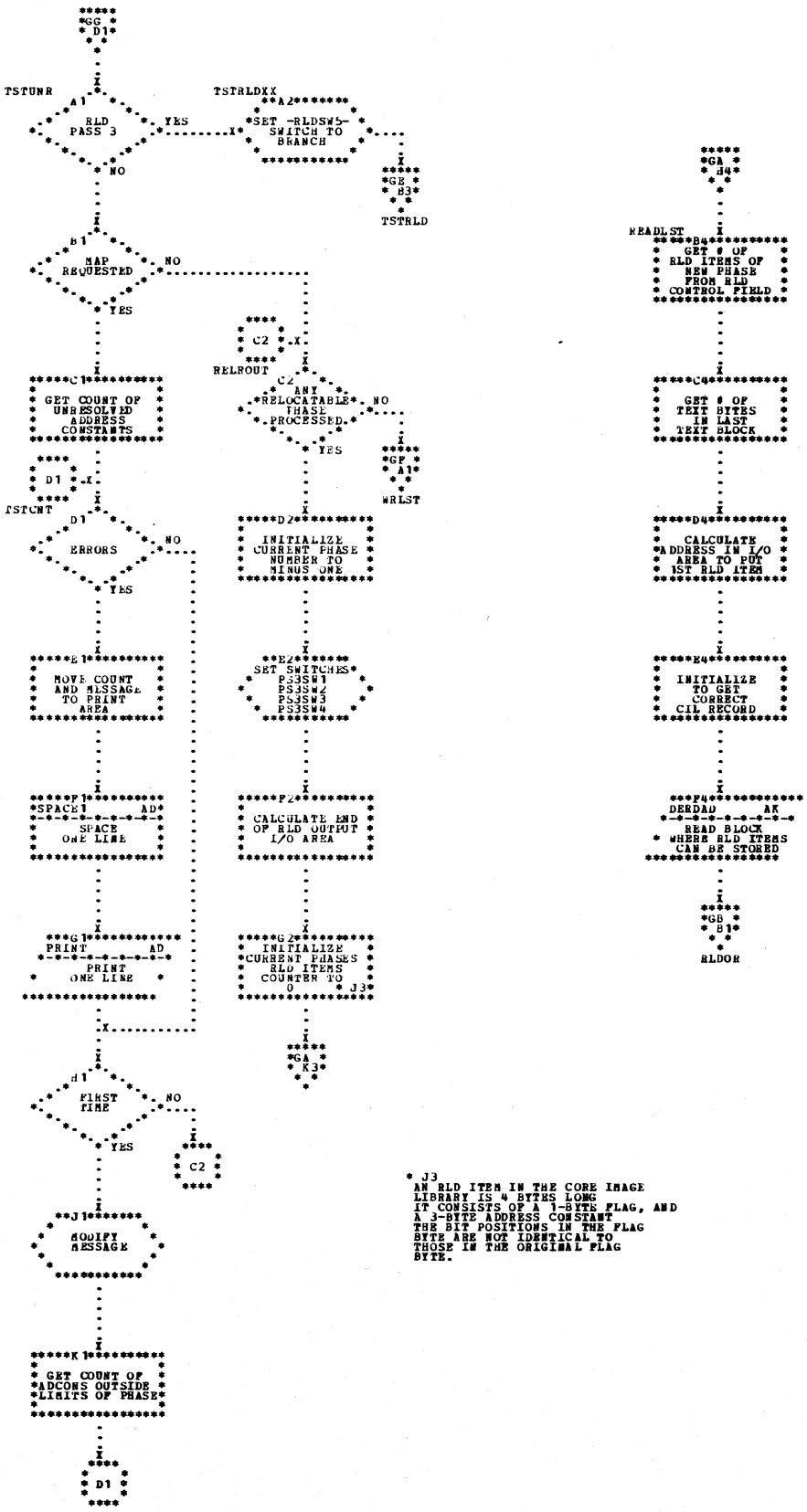


Chart GE. IJBRLD - Pass 2 Abort and Map Routines. Refer to Chart 11

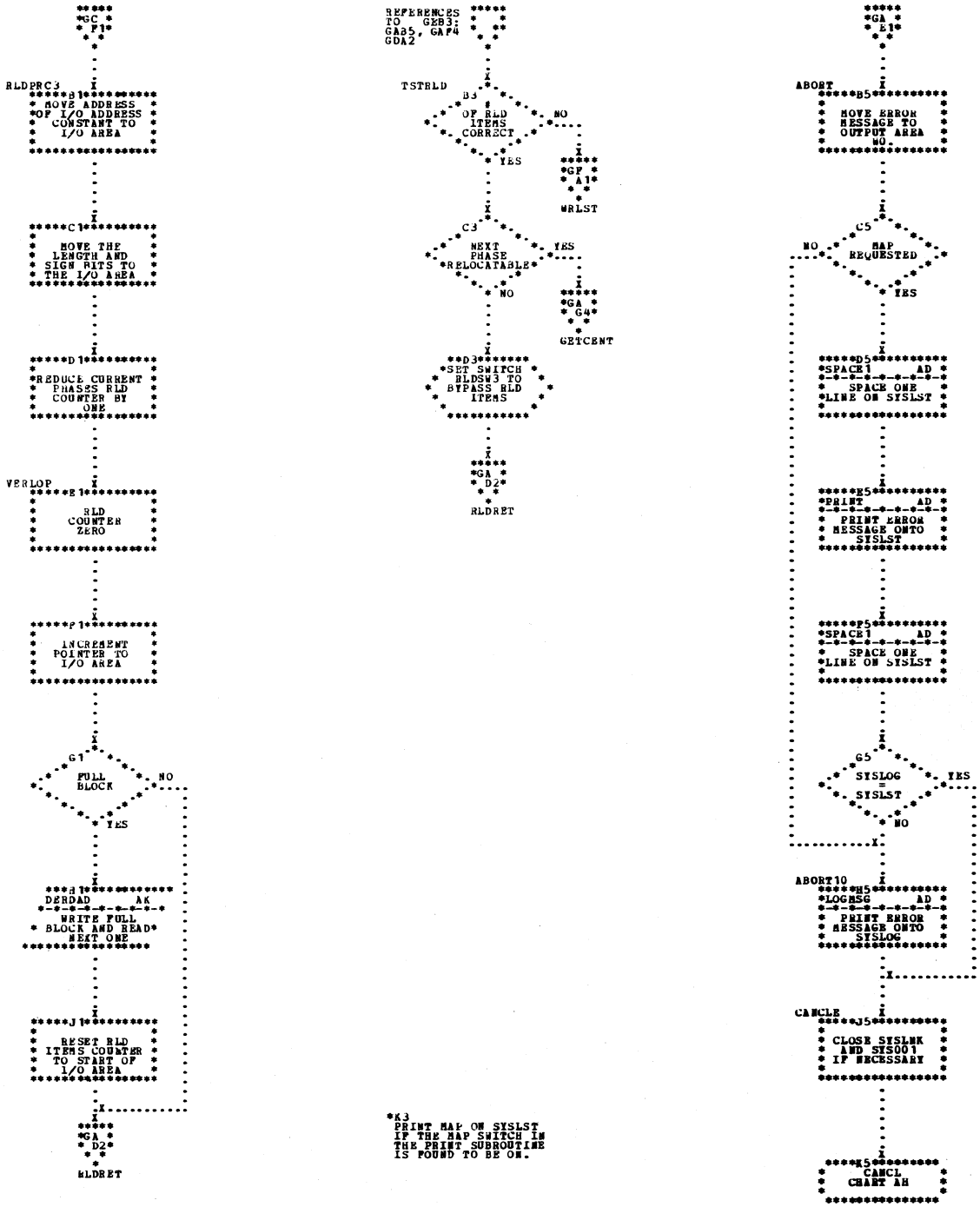


Chart GF. IJBRLD - Pass 2 Block Phase Header. Refer to Chart 11

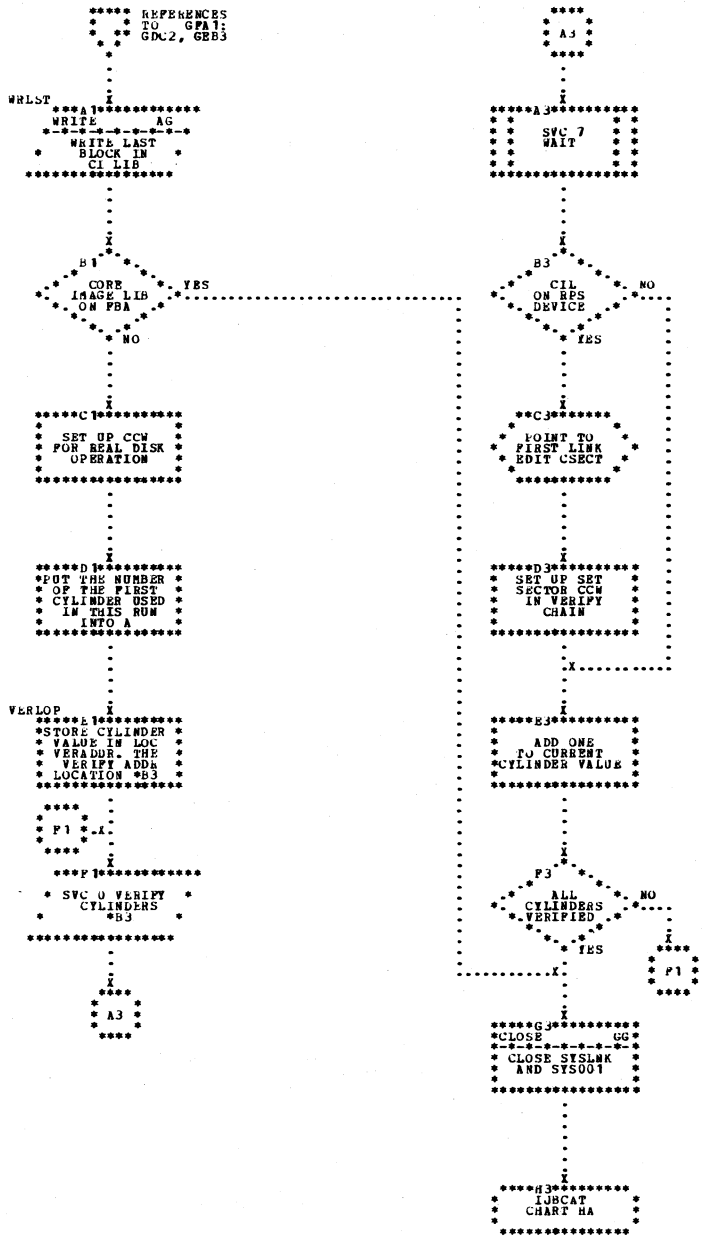


Chart GG. IJBRLD - Pass 2 Subroutines. Refer to Chart 11

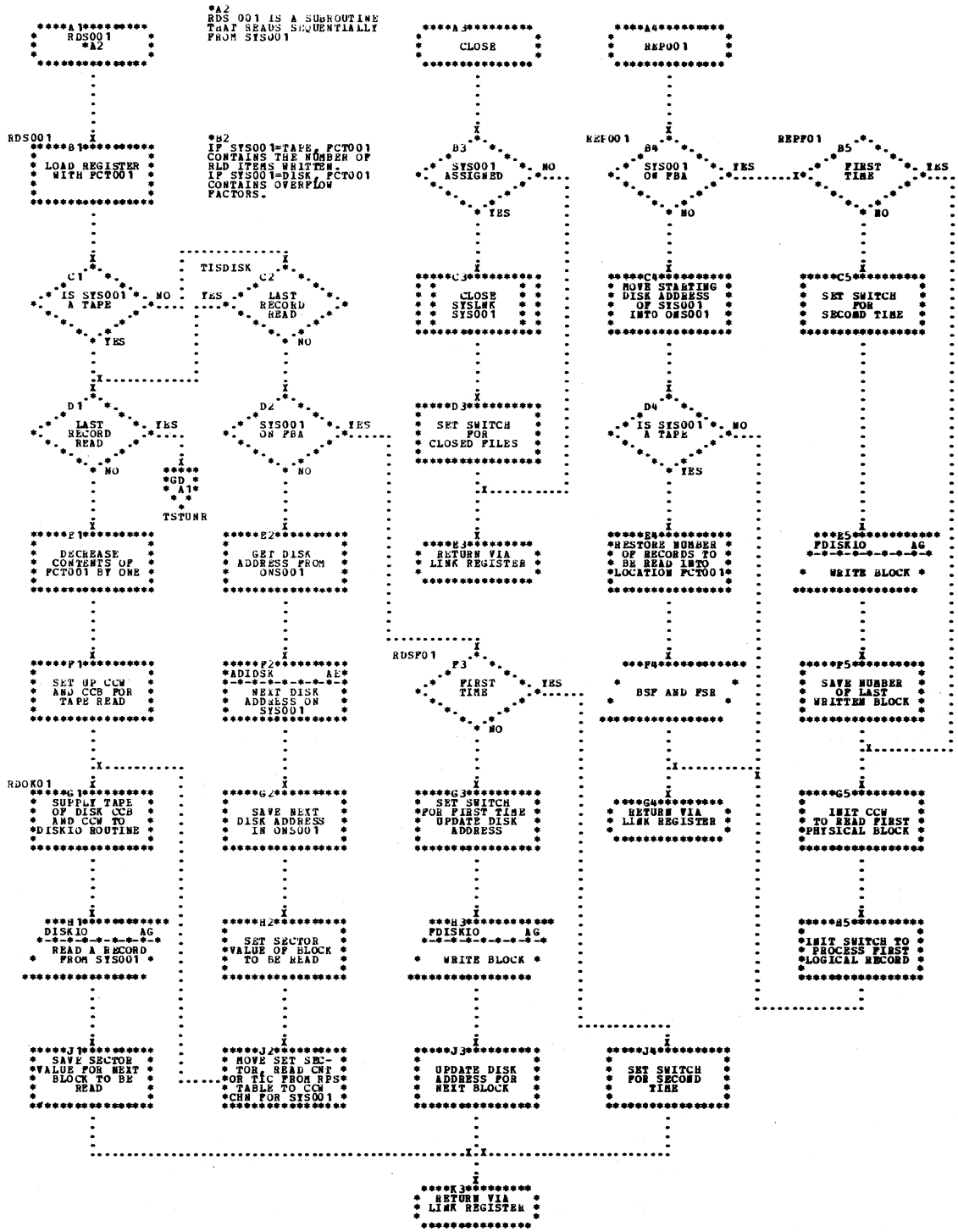


Chart HA. IJBCAT - Update CIL Directory (Part 1 of 2). Refer to Chart 12

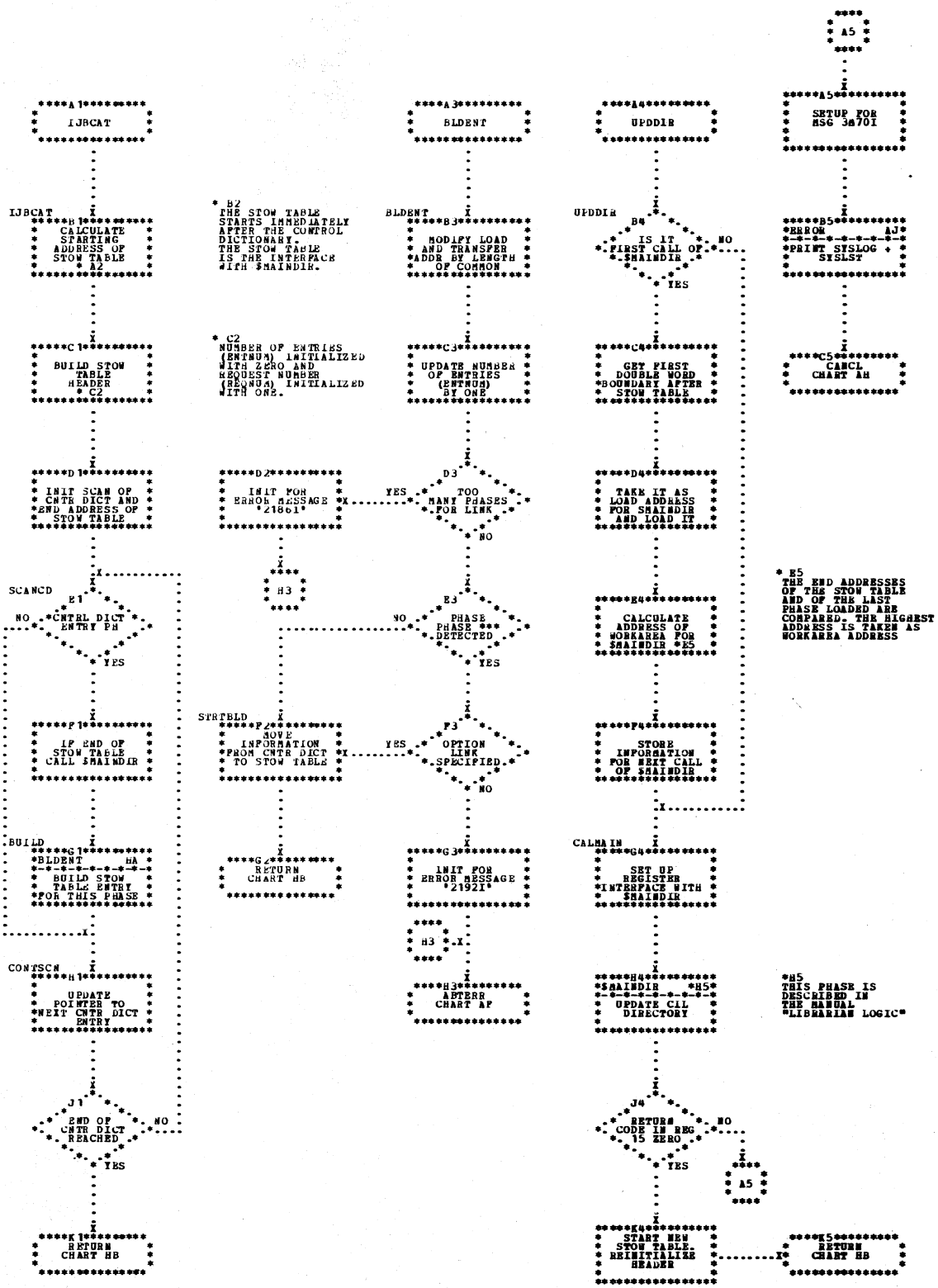


Chart HB. IJBCAT - Update CIL Directory (Part 2 of 2). Refer to Chart 12

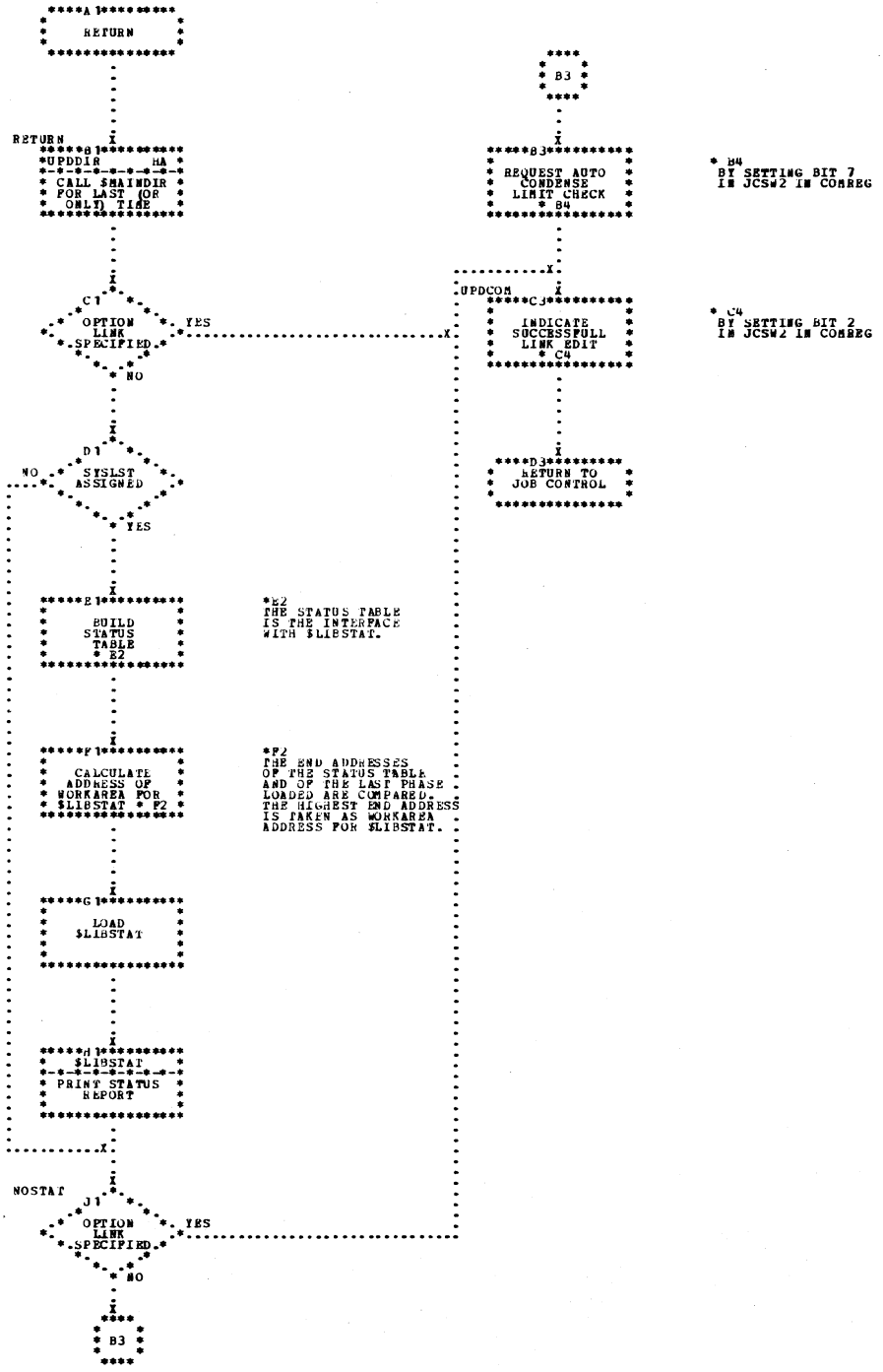


Chart JA. IJBINL - Initialization (Part 1 of 2). Refer to Chart 01

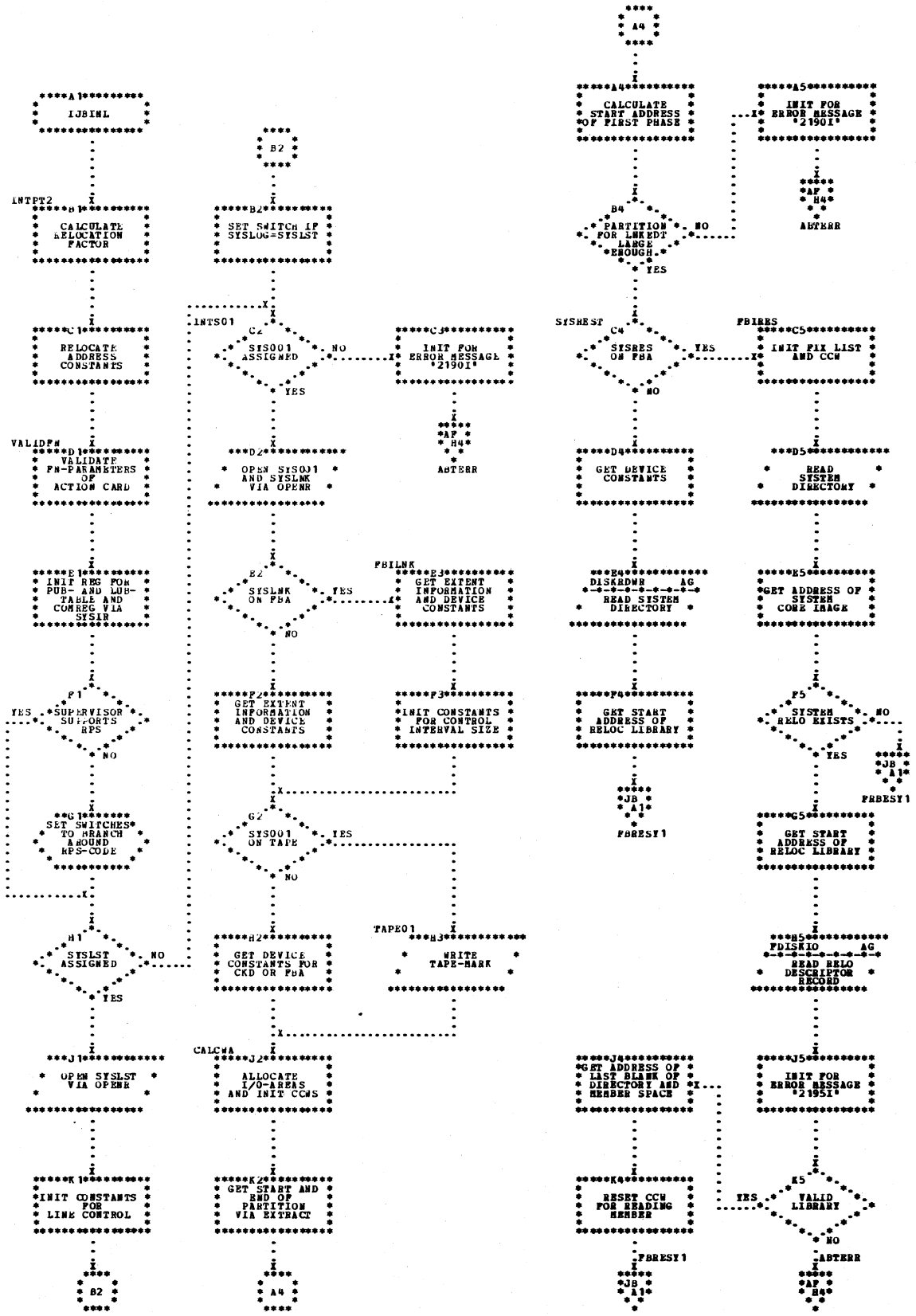


Chart JB. IJBINL - Initialization (Part 2 of 2). Refer to Chart 01

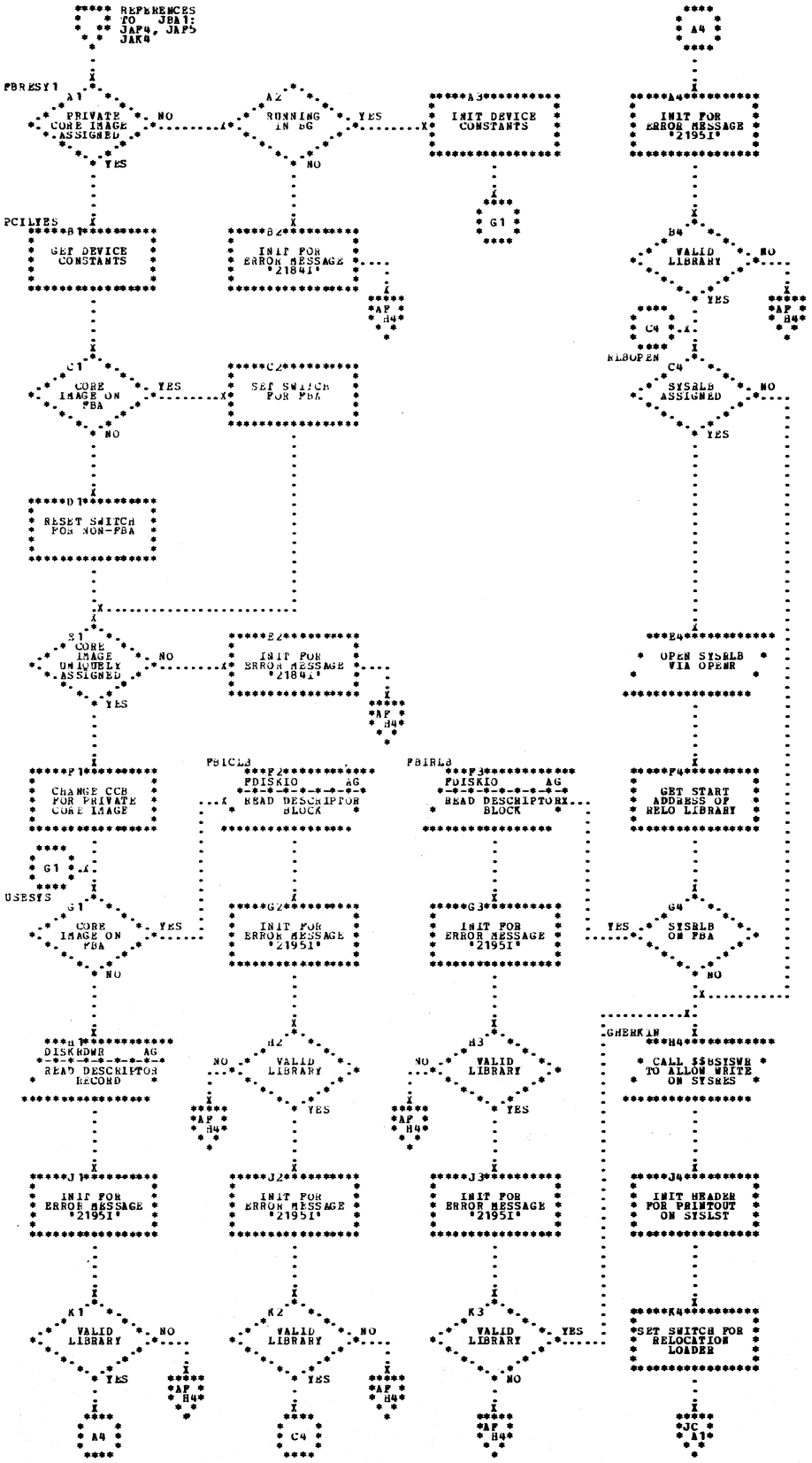


Chart JC. IJBINL - Action Processor (Part 1 of 2) Refer to Chart 01

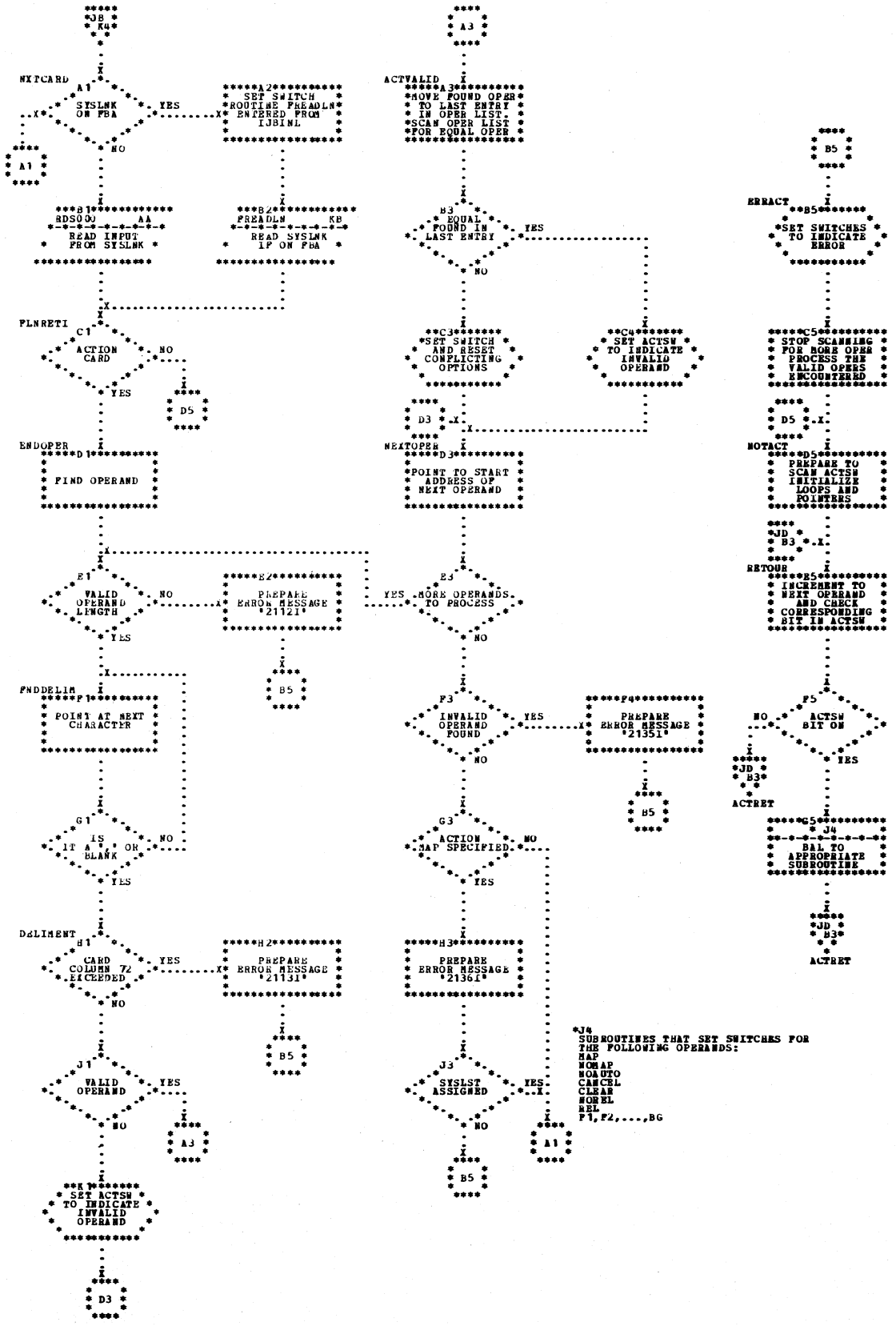


Chart JD. IJBINL - Action Processor (Part 2 of 2) Refer to Chart 02

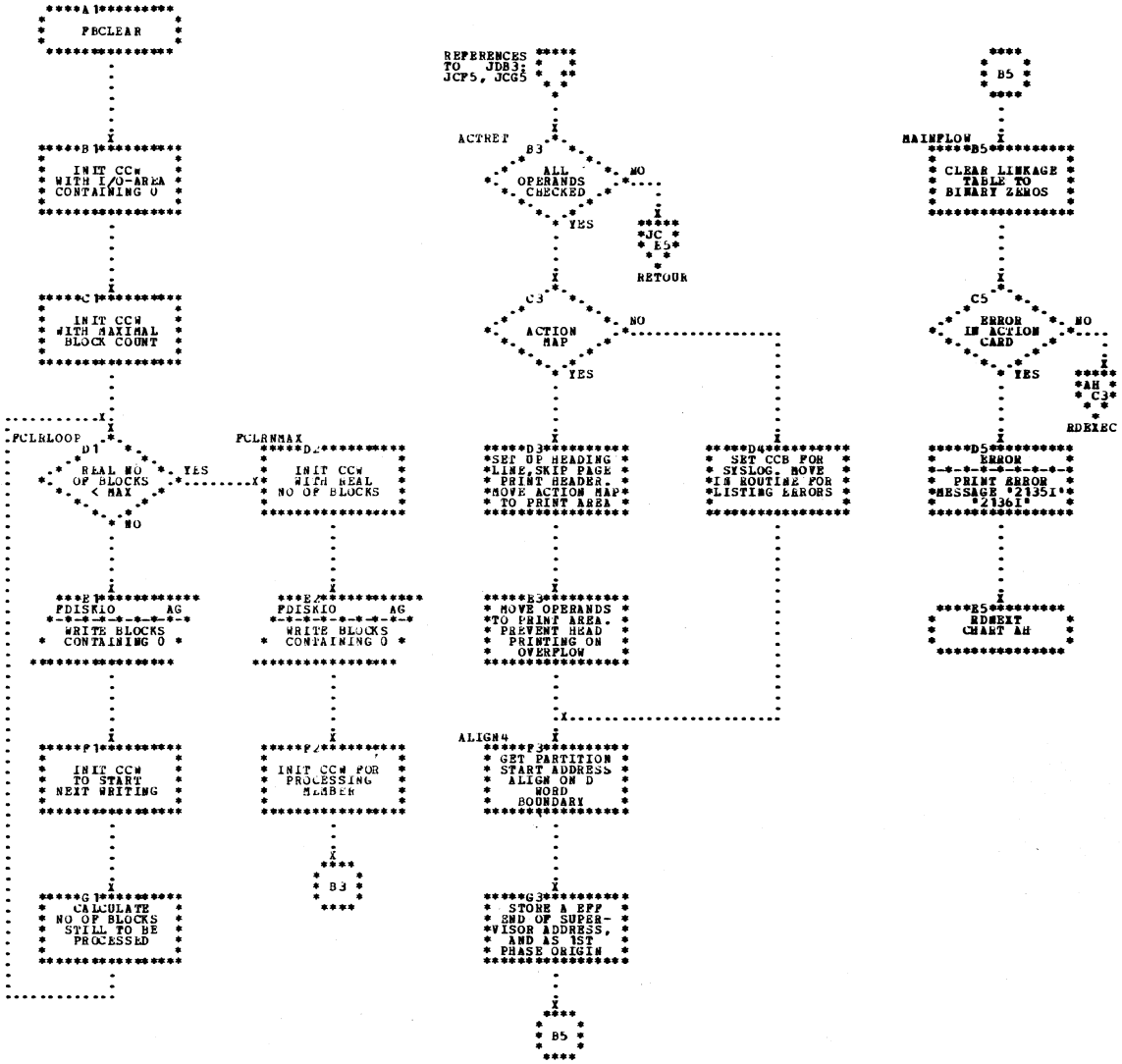


Chart KA. IJBFIN - Process Input from FBA-Relocatable Library. Refer to Chart 03

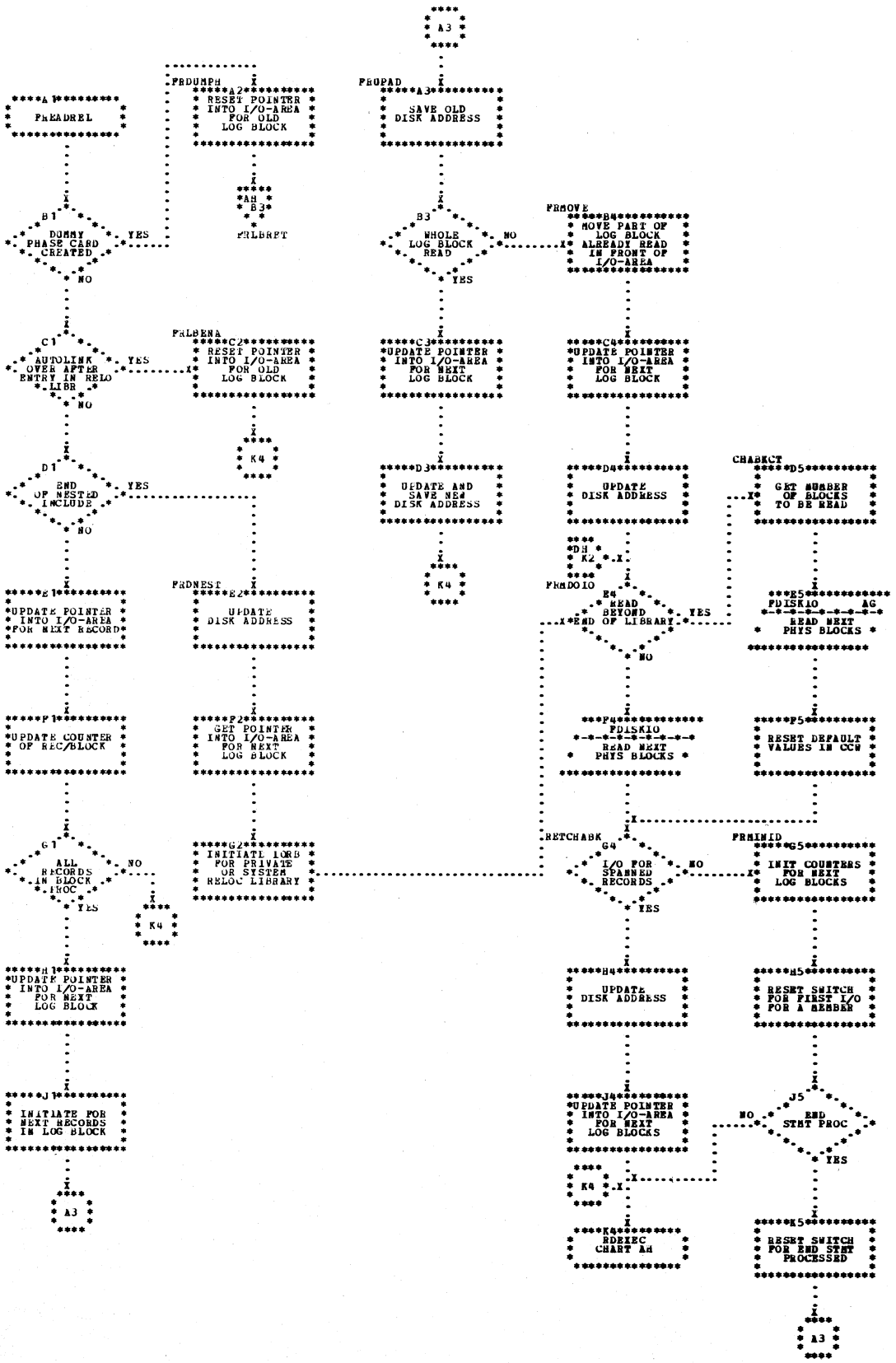
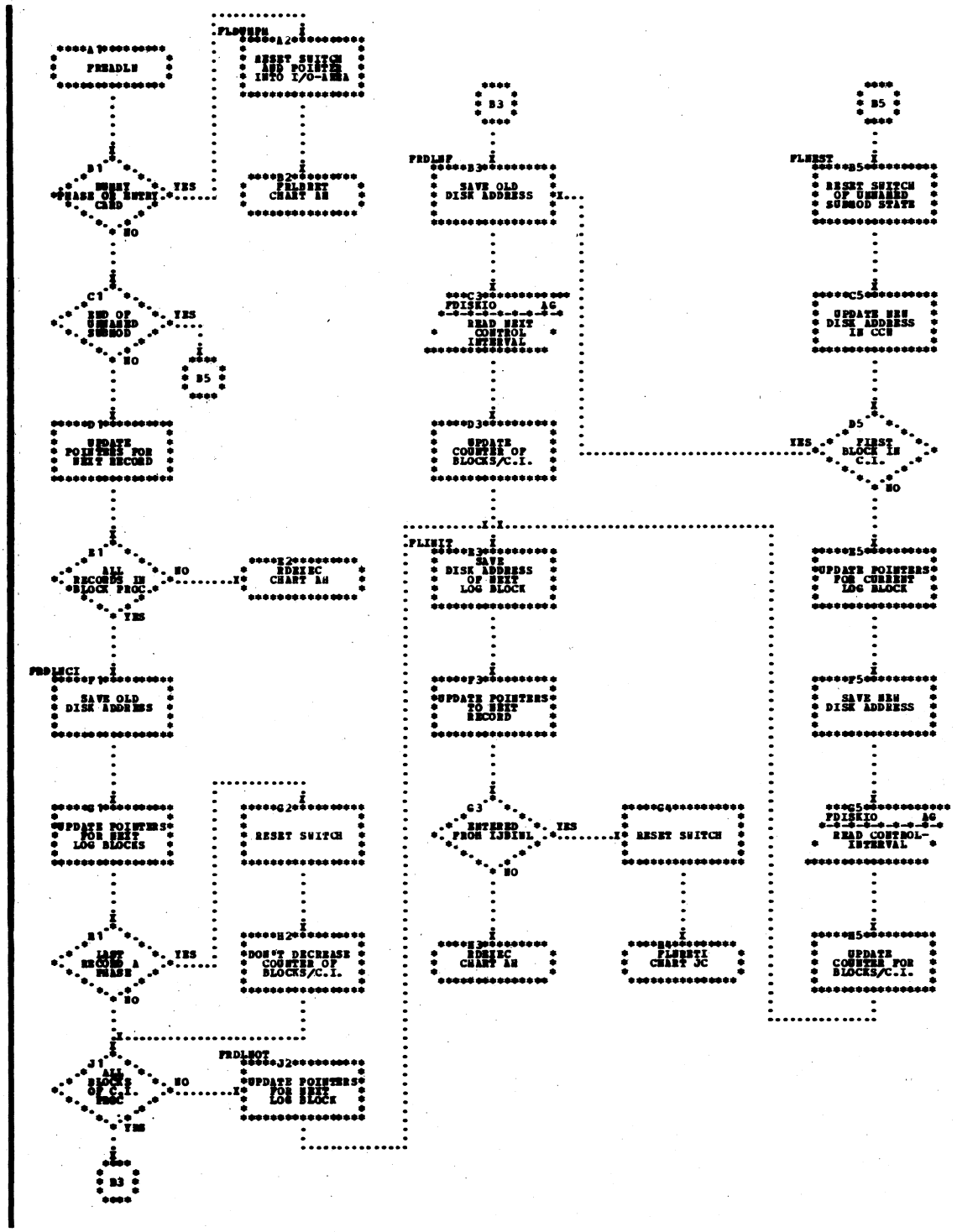


Chart KB. IJBFIN - Process Input from FEA-SYSLNK Refer to Chart 03



APPENDIX A: LABEL LIST

This label list has two parts: One lists the entry labels and summarizes the function of the CSECTs the labels lead to; the other one lists all the labels occurring in the flowcharts.

Part 1: Entry Labels

Label	CSECT	Chart
ABORT		GE
	Beginning of non-recoverable error handling subroutine.	
ABTERR		AF
	Gives control to IJBRLD so that abort error processing can continue. Entered when non-recoverable errors are found.	
ACSLTH		CG
	Some compilers supply control section length in the END card. This routine processes the control section length for this special case.	
ADMDSW	IJBMAP	FA
	Program switch to indicate first time through the MAP processor.	
ALNKPR	IJBLNK	AG
	Starting address of the autolink processor, which is entered whenever a phase has finished processing and autolink has been requested.	
CDSIZE	IJBLNK	AF
	Starting label of a subroutine to check for control dictionary overflow.	
CHKNPH	IJBESD	BA
	Beginning of the ESD processor phase, IJBESD (see "Appendix E" for a detailed description of this phase).	
CINOBL	IJBCTL	EE
	Number of core image blocks required by this phase is equal to number of bytes loaded, divided by block size. Add one block for any remainder.	
CNCALK	IJBESD	BC
	The instructions starting at this label cancel autolink. The NOAUTOL switch in CSWITCH (current CIL entry) is set to indicate that no autolink should be attempted on this ER, either because autolink has already been tried or because autolink should not be performed.	
CNVHEX	IJBLNK	AC
	Label at the beginning of a subroutine that converts hexadecimal to binary notation.	
COMCHK	IJBMAP	FA
	Beginning of common (CM) processing in the MAP processor. The cumulative length of discretely named commons is calculated at this point in the program.	
DECDSP	INBSCN	DD
	Beginning of decimal displacement processing for the operand of a phase card.	
DEBLAD	IJBLNK	AK
	Beginning of subroutine that builds core image blocks. Basically, this subroutine: 1. Ensures that the text is within the limits of the phase; 2. Finds the core image block the text belongs in; 3. Reads the core image block required by the text into the I/O area.	
DEBLSW	INBLNK	AK
	Program switch that forces continued processing when a zero length control section is found by the ESD processor (Chart BE).	
DMPHSW	IJBLNK	AH
	Program switch initialized as an MVC instruction. Modified to an effective NOP by the ESD processor (Chart BA) when a dummy phase card is to be built. By the NOP modification, the disk address of the ESD card not yet processed is retained in location COMNRF for use after the phase processing is finished. (Dummy phase cards are treated as actual phase cards.)	
DSPRTN	IJBSCN	DC
	Beginning of displacement operand	

Label	CSECT	Chart
	processing.	
ELBCM	IJBESD	ED
	Beginning of CM (common) processing. Whenever both the ESD item in the card image and the control dictionary entry are commons with matching labels, this routine puts the common with the longest length in the control dictionary. If commons with different labels are found, this routine posts the new common in the control dictionary. The map processor of the linkage editor calculates a total length of commons, which adjusts the phase origin.	
ENDRTN	IJBOTH	CF
	Tests SBMDST to determine it the name list should be cleared. (See SBMDST in label list.)	
ENDSBM	IJBOTH	CG
	Program switch providing an exit from the END card processor. The switch is assembled in the NOP state, initialized to branch by the END card processor, and reset to NOP by the END card processor if the module being processed has been autolinked.	
ENDSCD	IJBOTH	CG
	Searches control dictionary for unassigned LD/LRs, and ensures that the control dictionary number for such items is negative.	
ENTALK	IJBSCN	DD
	Provides an exit from the $LNKEDT4 phase of the linkage editor when a blank ENTRY card is found.	
ENTCRD	IJBSCN	DB
	Beginning of the entry card processor. Note: At this time, a blank operand field would be detected in the skip blanks subroutine. (See SKIPB and ENTALK in the label list.)	
ERRACT	IJBINL	JC
	Common error exit from the action processor. Error messages are initialized in the action processor, but are actually issued during the execution of another initialization routine (see Chart AC).	
ERRNML	IJBSCN	LA
	Program switch initialized to branch. However, it an error occurs on an include card and the include card has created a name list,	

Label	CSECT	Chart
	ERRNML is set to NOP. This allows the name list to be cleared before card error processing.	
ESDRET	IJBESD	BA
	Common entry point when the processing of an ESD item is finished. Instructions starting at this label determine if any more ESD items are in the variable field of the card image.	
ESLBCD	IJBESD	BD
	Beginning at this label, the ESD processor searches the control dictionary for a label that corresponds to the label of the ESD item in the current control dictionary entry.	
EXLOAD	IJBLNK	AH
	1. Entry point from the autolink routine (Chart AJ) when the control card processing phase is to be loaded. 2. Entry point from the ESD processor when a dummy phase card has been built and a control card processing phase is to be loaded. 3. Entry point from the initialize IJBOTH routine when the ESD processing phase is to be loaded.	
FCHBLD	IJBMAP	FD
	Entry point when NOMAP option is found.	
INCLOP	IJBSCN	DG
	Beginning of the relocatable directory scan for autolink, include, and terminal processing. The scan looks for a module with a name that matches the card image name field.	
ISDISP	IJBCTL	EC
	Processing when the phase card operand is a displacement.	
ISROOT	IJBCTL	EC
	Processing when the phase card operand is ROOT.	
LABST	IJBSCN	DB
	Builds the name list of control sections from the operand field of an INCLUDE card. These control sections subsequently build a phase (see NMELST in the label list).	
LTCDNO	IJBLNK	AB
	Entry point to the control dictionary search subroutine when a test for control dictionary number assignment is required by the calling	

Label	CSECT	Chart
	routine. The control dictionary number was available, but because its status was undetermined, entry is made to this subroutine.	
LTESID	IJBLNK	AB
	Beginning of the subroutine that finds control dictionary number, control dictionary address, or relocation factor, using the ESID number from the language translator and the linkage table constructed by the linkage editor. LTESID is the entry point when the ESID number is supplied.	
MAPCST	IJBMAP	FB
	Sets up for a scan of the control dictionary, searching for control sections that belong to the phase previously identified in this routine.	
MAPHAS	IJBMAP	FB
	Beginning of a control dictionary scan that searches for phase entries.	
MAPLDR	IJBMAP	FC
	Sets up for scan of control dictionary that searches for LD/LRs.	
NMELST		*
	A list of control sections specified by the name list operand of an INCLUDE card. The list is blank except when a named submodule is still being processed.	
NMSBSW		*
	Supplies the information in byte 4 of location PERIDA during INCLUDE card processing in the IJBSCN phase. Resets to zero during the execution of the control card scan in the IJBSCN phase. Bit 6 is set to one during initial INCLUDE card processing, and Bit 1 is set during phase post processing (autclink mode).	
NOBLOK		*
	Label in control dicticnary entry.	
NOBYTE		*
	Label in control dicticnary entry.	
CRPHDA		*
	Label in control dicticnary entry.	
CRPHRG		*
	Label in control dicticnary entry.	

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* Listing only

Label	CSECT	Chart
PERIDA		*

The location labeled PERIDA is a 36-byte input control area used by the linkage editor program to:

- obtain the address of the next card image to be processed after the END card;
- determine the point at which processing is finished for an object module;
- maintain control over the nesting of include statements by functioning as last-in, first-out list to establish processing priorities.

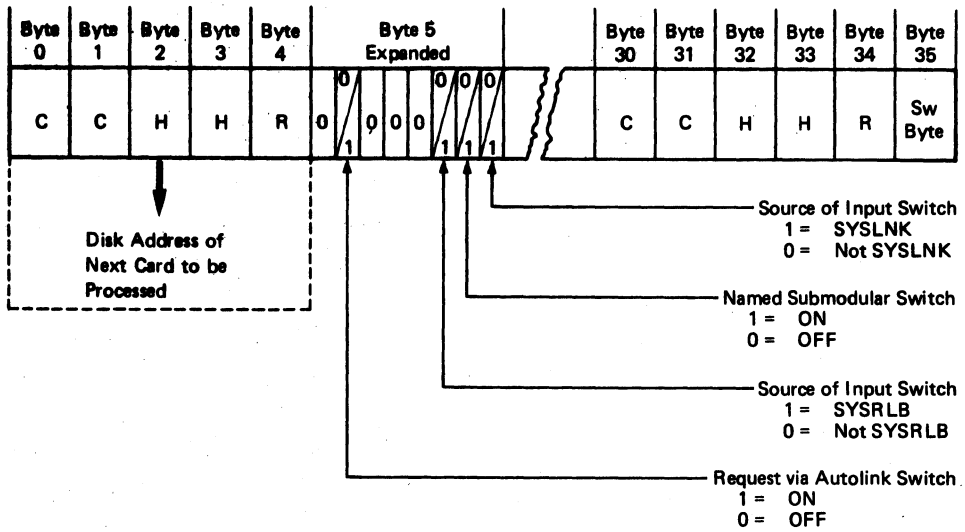
Location PERIDA is used in conjunction with either location ESD000 or ESDN00 (see label list) depending on the input device being used at this time. ESD000 or ESDN00 is loaded with the disk address of the first ESD card image of the object module. PERIDA is loaded with the disk address of the card image that follows the control card image. The linkage editor program compares the disk address in location PERIDA with the address in either ESD000 or ESDN00. Input control is based on the result of the comparison made at END card time. Possible results and corresponding input control actions are:

- The address in PERIDA is equal to or higher than the address in ESD000. Process the card image sequentially following the END card.
- The address in PERIDA is lower than the address in ESD000. Get the address of next card image to be processed from PERIDA.
- The address in PERIDA is lower than the address in ESDN00. Get the address of the next card image to be processed from PERIDA.
- The address in PERIDA is equal to or higher than the address in ESDN00. Effectively shift PERIDA left six bytes. Get the address of the next card image to be processed from the updated PERIDA.

Before the comparison is made and the appropriate actions are taken at END card time, the linkage editor program ensures that a value is available for PERIDA (see RECF00 in this list). Location PERIDA establishes processing priority by functioning as a last-in, first-out list for up to five levels of include (nest depth). The list is built during

the execution of the include card processor (Chart DB). Figure 10 illustrates the physical structure of PERIDA and Figure 11 illustrates how this location functions as a last-in, first-out list.

Note: If all five levels of include are used, the last 6-byte segment of PERIDA contains the address of the card image following the first INCLUDE statement.



Note: Input from system relocatable library if byte 5 bits 5 and 7 are both 0.

Figure 10. PERIDA Layout

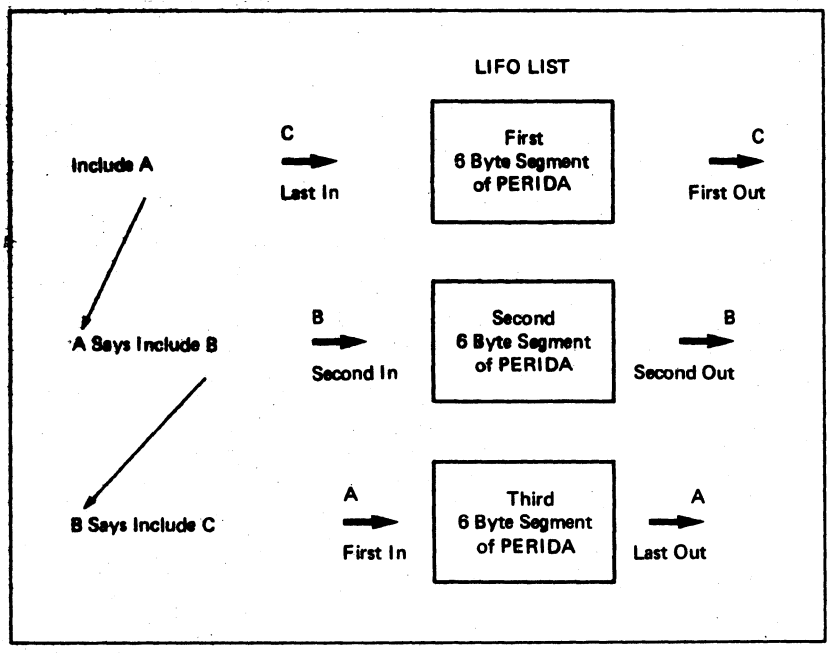


Figure 11. Last-In, First-Out List (LIFO)

Label	CSECT	Chart
PHADMD	IJBMAP	FB
	Adjusts load address of the phase by the cumulative length of the discretely named commons.	
PHCRD	IJBSCN	DC
	Beginning of the phase processor in the IJBSCN phase. This part of the phase processor performs two basic functions: 1. Determines which optional operand has been used. 2. Validity checks the phase card image.	
PHSTOR	IJBMAP	FA
	Reinitializes the phase information in location PHEADR (see label list).	
PVLESW	IJBLNK	AH
	Switch set to NOP by END and INCLUDE card processors if input is from SYSRLB.	
QUAPRO	IJBSCN	DD
	Beginning of qualifier processing for the operand of a phase card.	
RDALSW	IJBLNK	AH
	Switch set to branch if Autolink is in operation.	
RECF00	IJBLNK	AA
	Program switch set to branch and reset to NOP by either the ESD processor (Chart BA) or the END card processor (Chart CF). The ESD processor ensures that the correct disk address is in location PERIDA (see label list) by branching to the read SYSLNK subroutine at location INS000 after the CCW has been set to NOP. The disk address of the next card image is located by updating the disk until a record is found. Register 2 supplies the correct disk address for location PERIDA. The END card processor used the same technique to locate the disk address of the next card to be processed (put into location NDS000). RECF00 is set to branch to prevent updating beyond the proper disk address.	
RELESW	IJBLNK	AH
	Program switch that tests for input from the relocatable library. Sets (branch) in the include processor and resets (NOP) in the END card processor.	
RLDPRC	IJBOTH	CC
	Beginning of RLD pass 1 processing.	
RLDRAG	IJBRLD	GA
	Reads RLD information, supplied by pass 1, from SYS001.	
RLDSW1	IJBRLD	GA
	Program switch set to branch within this phase, whenever pointer processing is finished.	
RLDSW2	IJBRLD	GB
	Program switch initialized to branch, calculates load address (assembled origin of control dictionary entry plus relocation factor) when set to NOP in this phase.	
RLDSW3	IJBRLD	GC
	Initialized to NOP. Set to branch within this phase whenever R and P pointers indicate wrong phase.	
RLDSW4	IJBRLD	GC
	Program switch initialized to NOP, indicating the ADCON is to be extracted from the core image block. If the switch is set to branch, the ADCON is replaced in the core image block.	
RLSW1	IJBOTH	CD
	Program switch set and reset within IJBOTH phase. Setting (NOP or branch) determines if the R and P pointers are to be processed. Several RLD items can habe the same R and P pointers. Only the first set of identical R and P pointers are processed.	
RLWRIT	IJBOTH	CE
	Program switch set to NOP in the pass 1 RLD processor when the RLD is to be processed in the pass 2 RLD processor. If the switch is set to branch (initial condition), the RLD is ignored.	
ROOTNO		*
	This location contains a zero when the first phase is not specified root, and a one when it is a root. The value in ROOTNO is either added to or subtracted from the control dictionary number. • Subtracted - when the control dictionary number is used to obtain a control dictionary entry address. (C/D NO - ROOTNO) X16 = DISPLACEMENT CDENT1 + DISPLACEMENT = ENTRY ADDRESS	

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* Listing only

Label	CSECT	Chart
	• Added - when a root phase has been specified, a one is added for each control dictionary entry.	
SBMDST		*
	A program switch that indicates when NMELST should be cleared (Bit 7) or an END card has been read (Bit 3). Bit 7 is turned on when a named submodule (INCLUDE NAME, (CSECT)) is found. At the same time, a bit switch in location PERIDA (see label list) is turned on. The apparent duplication of switches is necessary because the first 5-byte segment of PERIDA is a variable, which depends on nested levels of INCLUDEs. At END card time, a test is made of the bit switch in location PERIDA. If bit 6 of byte 4 in PERIDA is on, turn off bit 7 in SBMDST. The switch in PERIDA can then be tested. If bit 6 of byte 4 in PERIDA is off, do not change the status of SBMDST. The bit switch has already been moved to some other 5-byte segment of PERIDA. The linkage editor program can then test SBMDST to determine if the END card being processed is part of the module named in the INCLUDE statement (bit 7 in SBMDST off). The name list (NMELST) is cleared at END card time, except when a named submodule still being processed.	
SRCHCD	IJBLNK	AC
	Beginning of a subroutine that finds the last duplicate label in the control dictionary.	
SRPCOD	IJBLNK	AC
	Tests for end of control dictionary. Entry point for the label-search subroutine.	
TRFRAD		*
	Label in control dictionary entry.	
TSTCNT	IJBRLD	GD
	Sets up MAP information (number of ADCONS outside the phase limits) in a test register. If the register is zeroed, there is no MAP information. If the content is nonzero, MAP information is to be printed.	
UPDSKAD	IJBLNK	AE
	Updates the disk address to the first record on the next track.	
VERLOP	IJBRLD	GF
	Beginning of a loop that reads and verifies all core image blocks written by linkage editor. All verification occurs at this point, rather than after each individual write operation.	
XTPHNO	IJBLNK	AF
	Beginning of a subroutine that extracts the phase number from the control dictionary.	

Part 2: All Labels

As there is only one phase, $LNKEDT, in this program, "CSECT" here indicates the CSECT of the general phase.

Label	CSECT	Location	Label	CSECT	Location
ABORT	IJBRLD	GEB5	DERITE	IJBLNK	AKE3
ABORT10	IJBRLD	GEH5	DERITE1	IJBLNK	AKF3
ABTERR	IJELNK	AFH4	DERLOP	IJBLNK	AKJ3
ACSLTH	IJBOTH	CGB4	DERSW1	IJBLNK	AKK1
ACTRET	IJEINL	JDB3	DISKIO	IJBLNK	AGE1
ACTVALID	IJBINL	JCA3	DISKRDWR	IJBLNK	AGD1
ADMDSW	IJEMAP	FAD3	DMPHSW	IJBLNK	AHD3
AD1DSK	IJBLNK	AEC3	DPLAB	IJBMAP	FDH1
ALIGNDW	IJBCTL	ECD4	DSPRTN	IJBSCN	DCH1
ALIGN4	IJBINL	JDF3			
ALKERR	IJBSCN	DGA4	EISCSL	IJBOTH	CGF4
ALKFND	IJBSCN	DHA1	EISDPC	IJBESD	BCB3
ALNKOD	IJELNK	AGF4	ELBCER	IJBESD	BDD3
ALNKOF	IJBLNK	AHB1	ELBCM	IJBESD	BDC2
ALNKPR	IJEINK	AGB4	ELBDSD	IJBESD	BDF5
ALNKSC	IJBLNK	AGE4	ELBELR	IJBESD	BCH5
ALNKVL	IJBLNK	AGJ5	ELBER	IJBESD	BCB4
			ELBGSD	IJBESD	BDJ5
BLDENT	IJBCAT	HAB3	ELBINT	IJBESD	BFE1
BUILD	IJBCAT	HAG1	ELBISITW	IJBESD	BCE5
			ELBLD	IJBESD	BEA1
CALCWA	IJEINL	JAJ2	ELBLDR	IJBESD	BEB3
CALMAIN	IJBCAT	HAG4	ELBNAS	IJBESD	BEF4
CANCL	IJBLNK	AHB5	ELBNCD	IJBESD	BFB1
CANCLE	IJBRLD	GEJ5	ELBNLR	IJBESD	BED2
CDSIZE	IJBLNK	AFB4	ELBPC	IJBESD	BDE1
CHABKCT	IJEFIN	KAD5	ELBSD	IJBESD	BDC4
CHEKQU	IJBCTL	EBB3	ENCRLT	IJBOTH	CGH1
CHKNPH	IJEESL	BAB1	ENDERR	IJBLNK	AJH4
CHKRP	IJBSCN	DBE3	ENDOPER	IJBINL	JCD1
CHKRPN	IJBSCN	DDD5	ENDPRC	IJBOTH	CFA1
CHKSYM	IJBLNK	AHJ3	ENDRTN	IJBOTH	CFH2
CHQUALIF	IJBCTL	ECD2	ENDSBM	IJBOTH	CGH4
CIMBLK	IJBCTL	EEH4	ENDSCD	IJBOTH	CGB1
CINOBL	IJBCTL	EEB1	ENDXFP	IJBOTH	CFA4
CLRCMN	IJBMAP	FAE2	ENLD	IJBESD	BBB4
CLREXT	IJBOTH	CHE3	ENOT00	IJBOTH	CFA2
CMDEL	IJBSCN	DEJ4	ENOXFR	IJBOTH	CFC5
CNCALK	IJBESL	BCA1	ENTALK	IJBSCN	DDH4
CNTSW	IJBOTH	CDF1	ENTCRD	IJBSCN	DBB4
CNVAHX	IJBLNK	ACJ3	ENUNAS	IJBOTH	CGD1
CNVBIN	IJBMAP	FEB4	EPHSCD	IJBESD	BFK4
CNVHEX	IJBLNK	ACB4	EPHSCN	IJBESD	BFF3
CNVHSW	IJBLNK	ACG3	EPHULD	IJBESD	BFD4
CNVLOP	IJBMAP	FED4	ERRACT	IJBINL	JCB5
CNVSHF	IJBLNK	ACH3	ERRNML	IJBSCN	DAF2
COMCHK	IJBMAP	FAG1	ERROR	IJBLNK	AJB3
CONTSCN	IJBCAT	HAH1	ERROR10	IJBLNK	AJJ2
CQUAL	IJBCTL	ECA2	ERROR20	IJBLNK	AJJ3
CRDEND	IJBSCN	DDB4	ERROR40	IJBESD	BBB5
CTLSKP	IJBLNK	AHG2	ERROR40	IJBLNK	AJF4
CTNOBL2	IJBCTL	EEC2	ERROR40	IJBLNK	AJK4
			ERROR50	IJBLNK	AJF5
DECDSP	IJBSCN	DDA1	ERR000	IJBOTH	CAC5
DELEXT	IJBSCN	DCH4	ERR002	IJBLNK	ACC4
DELIMENT	IJBINL	JCH1	ERR012	IJBSCN	DEF4
DERCAL	IJBLNK	AKH3	ERR013	IJBSCN	DEE5
DERDAD	IJBLNK	AKB1	ERR013A	IJBOTH	CCH5
DERDOK	IJBLNK	AKD1	ERR014	IJBSCN	DBF2
DERDSW	IJBLNK	AKH1	ERR022	IJBCTL	EBD3
			ERR023	IJBCTL	EDD2

Label	CSECT	Location	Label	CSECT	Location
ERR024AA	IJBCTL	EBB4	FNDDEL	IJBSCN	DDA4
ERR032	IJBSCN	DGB4	FNDDELIM	IJBINL	JCF1
ERR040	IJBESD	BDH1	FNDENT	IJBLNK	AHH2
ERR041	IJBESD	BFA3	FONDEL	IJBSCN	DEE4
ERR043	IJBESD	BDB5	FRDLNCI	IJBFIN	KBF1
ERR043	IJBESD	BEG5	FRDLNF	IJBFIN	KBB3
ERR043	IJBESD	BEJ2	FRDLNOT	IJBFIN	KBJ2
ERR044	IJBLNK	AFD4	FRDNEST	IJBFIN	KAE2
ERR045	IJBESD	BCD2	FRDUMPH	IJBFIN	KAA2
ERR046	IJBESD	BDF3	FRLBENA	IJBFIN	KAC2
ERR050	IJBLNK	AKE1	FRLBRET	IJBLNK	AHB3
ERR051	IJBOTH	CCE4	FRMDOIO	IJBFIN	KAE4
ERR055	IJBOTH	CDH3	FRMINID	IJBFIN	KAG5
ERR058	IJBOTH	CGD4	FRMOVE	IJBFIN	KAB4
ERR070	IJBLNK	ABH2	FRUPAD	IJBFIN	KAA3
ERR081	IJBCTL	ECJ3			
ERR085	IJBMAP	FDF5	GETCENT	IJBRLD	GAG4
ERR091	IJBOTH	CHD2	GETVRB	IJBSCN	DAG5
ERR093	IJBLNK	AKE5	GHERKIN	IJBINL	JBH4
ERR097	IJBLNK	AGH2	GORLD	IJBMAP	FDJ4
ERR44	IJBLNK	ABC3			
ERR44A	IJBLNK	ABB2	HOWMANY	IJBCTL	EEE4
ESCNCD	IJBESD	BFD3			
ESDNXT	IJBESD	BAH2	IJBCAT	IJBCAT	HAB1
ESDRET	IJBESD	BAB3	IJBMAP	IJBMAP	FAC1
ESDSBM	IJBESD	BCH1	IJBOTH	IJBOTH	CAB1
ESD1ST	IJBESD	BAA2	IJBRLD	IJBRLD	GAB1
ESIXTA	IJBMAP	FAG3	IJBSCN	IJBSCN	DAB1
ESLBCD	IJBESD	BDB1	INCCRD	IJBSCN	DBA1
EUPDCN	IJBESD	BFG2	INCCRD1	IJBSCN	DBE1
EUPDOK	IJBESD	BFC2	INCERR	IJBSCN	DGC4
EUPDSW	IJBESD	BFD2	INCFND	IJBSCN	DHE1
EUPDXT	IJBESD	BFC5	INCGET	IJBSCN	DGC1
EUPTRY	IJBESD	BFG1	INCGET1	IJBSCN	DGC2
EXECWR	IJBMAP	FDJ5	INCGET2	IJBSCN	DGF1
EXLOAD	IJBLNK	AHB4	INCLOP	IJBSCN	DGK1
EXTNLP	IJBMAP	FDB2	INCLPR	IJBSCN	DGB1
EXTNPR	IJBMAP	FDG2	INCRED	IJBSCN	DGD5
EXTNSW	IJBMAP	FDD2	INCREE	IJBSCN	DGH1
EXTRCT	IJBSCN	DEB3	INDJDR	IJBLNK	AHH5
EXTSCN	IJBMAP	FDC1	INS000	IJBLNK	AAF1
			INTPT2	IJBINL	JAB1
FBICLB	IJBINL	JBF2	INTS01	IJBINL	JAC2
FBILNK	IJBINL	JAE3	ISDISP	IJBCTL	ECA3
FBINSEC	IJBOTH	DJJ2	ISROOT	IJBCTL	ECE3
FBIRES	IJBINL	JAC5			
FBIRLB	IJBINL	JBF3	LABST	IJBSCN	DBB2
FBRDIOC	IJBOTH	DJB3	LDRGO	IJBMAP	FCB3
FBRDIREL	IJBOTH	DJB2	LDRSCN	IJBMAP	FCG2
FBRDIRF	IJBOTH	DJC1	LDRTSD	IJBMAP	FCC3
FBRDIRLB	IJBOTH	DJB1	LKQUO	IJBSCN	DCD4
FBRDNXT	IJBOTH	DJG1	LOADBASE	IJBLNK	AHF4
FBRESY1	IJBINL	JBA1	LOGMSG	IJBLNK	ADB2
FCHRLD	IJBMAP	FDE5	LSETB	IJBLNK	ABG2
FCLRLOOP	IJBINL	JDD1	LTCDAD	IJBLNK	ABA4
FCLRNMAX	IJBINL	JDD2	LTCDNO	IJBLNK	ABJ2
FDISKIO	IJBLNK	AGF1	LTCDRF	IJBLNK	ABB4
FINCLOP	IJBOTH	DJE3	LTESID	IJBLNK	ABC2
FINDEL	IJBSCN	DEE3			
FINDND	IJBSCN	DBJ3	MAINFLOW	IJBINL	JDB5
FINPRO	IJBCTL	ECG3	MAPCST	IJBMAP	FBH2
FIRSTPH	IJBCTL	EAB2	MAPHAS	IJBMAP	FBE5
FLDUMPH	IJBFIN	KBA2	MAPHNM	IJBMAP	FBH1
FLINIT	IJBFIN	KBE3	MAPLDR	IJBMAP	FCF2
FLNEST	IJBFIN	KBB5	MOREBLK	IJBCTL	EEG2
FLNRETI	IJBINL	JCC1	MOVENTRY	IJBCTL	EAD1

Label	CSECT	Location
MOVPER	IJECTH	CFJ1
NDESLP	IJEINK	AJH1
NEWPHS	IJECTL	EFB3
NEWPHSS	IJECTL	EFD3
NEXTOPER	IJEINL	JCD3
NEXTOPT	IJESCN	DFG3
NOAUTOCHK	IJESCN	DFD2
NOFLTPT	IJECTL	EBH1
NOSCAGAN	IJECTL	ECE2
NOSTAT	IJECAT	HBJ1
NOTACT	IJEINL	JCD5
NOTCTL	IJEINK	AJB1
NOTF	IJECTL	EBC2
NOTRFR	IJEMAP	FAE5
NOT1ST	IJECTL	EAB4
NTABS	IJESCN	DDA3
NTESLP	IJEINK	AJF1
NTROOT	IJECTL	EBA1
NXTCARD	IJEINL	JCA1
OTHINC	IJECTH	CAA5
OTHTFR	IJEOTH	CAF3
OTHTYP	IJECTH	CAD3
OVRLSW	IJEMAP	FDD1
PBDYCHK	IJESCN	DFF2
PCILYES	IJEINL	JBB1
PHADMD	IJEMAP	FBA1
PHCEXIT	IJESCN	DFH3
PHCOPTN	IJBSCN	DFB2
PHCRD	IJESCN	DCA1
PHCRD1	IJESCN	DCG1
PHSCAN	IJEMAP	FBC5
PHSPRC	IJBCTL	EAF1
PHSTOR	IJEMAP	FAJ2
PHXADD	IJECTL	EDD1
PRERR	IJEINK	AJC4
PREXTN	IJEMAP	FDB1
PRINT	IJEINK	ADB1
PRSDPC	IJBESD	BCC1
PRTLINE	IJEINK	ADF1
PRTLST	IJEINK	ADB4
PS3SW2	IJERLD	GAF4
PS3SW4	IJERLD	GAH4
QUAPRO	IJESCN	DDA5
RADD4	IJERLD	GAG2
RDALSW	IJBINK	AHD1
RDEXEC	IJEINK	AHC3
RDNEXT	IJBINK	AHE1
RDOK01	IJERLD	GGG1
RDSF01	IJERLD	GGF3
RDS000	IJEINK	AAB1
RDS001	IJERLD	GGB1
READC1	IJEINK	AGB1
READLST	IJERLD	GDB4
RECF00	IJEINK	AAC3
RELOC	IJEMAP	FBF2
RELROUT	IJERLD	GDC2
REPF01	IJERLD	GGB5
REPROC	IJECTH	CCB2
REPTXT	IJBOTH	CCC3
REP001	IJERLD	GGB4
RESDCN	IJERLD	GCC5
RESET	IJBSCN	DEC3
RETCHABK	IJBFIN	KAG4
RETOUR	IJBINL	JCE5
RETURN	IJBCAT	HBB1
RLADCN	IJBRLD	GCB3
RLBOPEN	IJBINL	JBC4
RLBYWR	IJBOTH	CEG2
RLCTER	IJBRLD	GBE2
RLDCLEAR	IJBCTL	EFH3
RLDCMN	IJBRLD	GBG3
RLDCON	IJBRLD	GCA1
RLDOP	IJBRLD	GAB3
RLDOR	IJBRLD	GBB1
RLDPRC	IJBOTH	CDB1
RLDPRC3	IJBRLD	GEB1
RLDRAG	IJBRLD	GAA2
RLDRET	IJBRLD	GAD2
RLDSW1	IJBRLD	GAH2
RLDSW2	IJBRLD	GBD3
RLDSW3	IJBRLD	GCC1
RLDSW4	IJBRLD	GCE3
RLRET	IJBOTH	CDD1
RLSTP	IJBOTH	CDB4
RLSW1	IJBOTH	CDH1
RLWRIT	IJBOTH	CEA2
RNXTRN	IJBRLD	GBB3
ROTSID	IJBRLD	GCC4
SAVCTL	IJBSCN	DBB5
SAVCTL1	IJBSCN	DDJ5
SCAGAN	IJBCTL	ECG2
SCAN	IJBMAP	FBJ2
SCANCD	IJBCAT	HAE1
SEEBLK	IJBSCN	DAE3
SELFRLC	IJBMAP	FBE2
SETPHS	IJBCTL	ECB5
SETUPSCN	IJBOTH	CAC3
SKIPB	IJBSCN	DEB1
SONOMN	IJBMAP	FAF1
SPACE1	IJBLNK	ADB3
SRCHCD	IJBLNK	ACB2
SRLABL	IJBLNK	ACC2
SRPCOD	IJBLNK	ACD2
STORR5	IJBSCN	DDE2
STRLD	IJBCTL	EED4
STRTBLD	IJBCAT	HAF2
SUBMOD	IJBSCN	DBH1
SVACHK	IJBSCN	DFE2
SYMBORG	IJBCTL	EBB1
SYSLIB	IJBSCN	DGE3
SYSREST	IJBINL	JAC4
TAPE01	IJBINL	JAH3
TERSXY	IJBMAP	FDD3
TISDISK	IJBRLD	GGC2
TISESD	IJBLNK	AJE2
TRYROT	IJBMAP	FBE1
TSTCNT	IJBRLD	GDD1
TSTESD	IJBOTH	CFH1
TSTLIM	IJBSCN	DDF1
TSTNEG	IJBSCN	DDC2
TSTRLD	IJBRLD	GEB3
TSTRLDXX	IJBRLD	GDA2
TSTUNR	IJBRLD	GDA1
TXTALL	IJBOTH	CEG4
TXTGET	IJBOTH	CBB3

Label	CSECT	Location
TXTPRC	IJBOTH	CBB1
TYPEVB	IJEINK	AGD4
UNRSPC	IJBMAP	FDH3
UPDATE	IJESCN	DEB5
UPDCOM	IJBCAT	HBC3
UPDDIR	IJECAT	HAB4
UPDSKAD	IJEINK	AEG3
UPNDS	IJBOTH	CAJ1
USESYS	IJEINI	JBG1
VALIDFN	IJBINL	JAD1
VERLOP	IJBRLD	GEE1
VERLOP	IJBRLD	GFE1
WHATNOW	IJBCTL	EFB1
WRLST	IJBRLD	GFA1
WRSF01	IJBOTH	CHB4
WRST01	IJBOTH	CHA2
WRS001	IJBOTH	CHB1
WRTRFR	IJBCTL	EDG1
XTPHGT	IJBLNK	AFE1
XTPHNO	IJBLNK	AFB1

APPENDIX B: PHASE TO MODULE CROSS REFERENCE

Phase:	Module:
$LNKEDT	IJBLE1

APPENDIX C: ERROR MESSAGES CROSS REFERENCE

Message	CSECT	Chart
2100I	IJBOTH	CA
2101I	IJBSCN	DA
2102I	IJBLNK	AC
	IJBSCN	DD
2110I	IJBSCN	DA
2111I	IJBSCN	DA
2112I	IJBSCN	DA
	IJBINL	JC
2113I	IJBOTH	CC
	IJBINL	JC
	IJBSCN	DE
2114I	IJBSCN	DA
2116I	IJBSCN	DA
	IJBLNK	AH
2117I	IJBSCN	DA
2120I	IJBCTL	EA
2121I	IJBSCN	DC
2122I	IJBCTL	EB
2123I	IJBCTL	ED
2124I	IJBCTL	EB, EC
2125I	IJBSCN	DC
2130I	IJBSCN	DG
2131I	IJBSCN	DG
2132I	IJBSCN	DG
2133I	IJBSCN	DB
2135I	IJBINL	JC, JD
2136I	IJBINL	JC, JD
2137I	IJBINL	JC, JD
2140I	IJBESD	BB, BD
2141I	IJBESD	BF
2142I	IJBESD	BB
2143I	IJBESD	BD, BE
2144I	IJBLNK	AB, AF
2145I	IJBESD	BC
2146I	IJBESD	BD
2147I	IJBOTH	CG
2150I	IJBLNK	AK
	IJBOTH	CB
2151I	IJBOTH	CC
2155I	IJBOTH	CD
2156I	IJBOTH	CE
2158I	IJBOTH	CG
2160I	IJBCTL	EF
2161I	IJBSCN	DF
2170I	IJBOTH	CB, CD, CF
2181I	IJBCTL	EA, EC
2182I	IJBCTL	EF
2184I	IJBINL	JB
2185I	IJBMAP	FD
2186I	IJBCAT	HA
2190I	IJBINL	JA
2191I	IJBOTH	CH
	IJBINL	JA
2192I	IJBCAT	HA
2193I	IJBLNK	AK
2194I	IJBLNK	AG
2195I	IJBINL	JB
2197I	IJBLNK	AG
2199I	IJBMAP	FD

APPENDIX D: SYSTEM RESIDENCE ORGANIZATION

Component		Starting Disk Address			Number of Tracks (Alloc.)	R = Required O = Optional
		CC	HH	R		
IPL Record	(Phase $$A$IPL1)	00	00	1	1	R
IPL Record		00	00	2		R
System Volume Label		00	00	3		R
User Volume Label		00	00	4		O
System Directory	Record 1	00	01	1	1	R
	Record 2	00	01	2		R
	Record 3	00	01	3		R
	Record 4	00	01	4		R
IPL Records (Phase $$A$PLBK)		00	01	5		R
Core Image Directory	Cataloged Phases	00	02		*	R
	Linked Phase					
Core Image Library Members		X	Y+1	1	*	R
Relocatable Directory		Z+1	00	1	*	O
Relocatable Library Members		X	Y+1	1	*	O
Source Statement Directory		Z+1	00	1	*	O
Source Statement Library Members		X	Y+1	1	*	O
Procedure Directory		Z+1	00	1	*	O
Procedure Library Members		X	Y+1	1	*	O
Label Information Area		Z+1	00	1	Device dependent	R

* Allocation Dependent on User Requirements
X = Ending CC of the Preceding Directory
Y = Ending HH of the Preceding Directory
Z = Ending CC of the Preceding Library

Figure 12. System Residence Organization on CKD

Component	Starting Disk Address Block Number	Number of Blocks	R=Required O=Optional
IPL Records (Phase $$A$IPL0)	0	1	R
System Volume Label[1]	1	1	R
System Directory	2	1	R
IPL Retrieval Program (Phase $$A$PLBF)	3	7	R
Core Image Directory	10	*	R
Core Image Library Members	X+1	*	R
Relocatable Directory	Y+1	*	O
Relocatable Library Members	X+1	*	O
Source Statement Directory	Y+1	*	O
Source Statement Library Members	X+1	*	O
Procedure Directory	Y+1	*	O
Procedure Library Members	X+1	*	O
Label Information Area	Y+1	200 [2]	R

* = Allocation dependent on user requirements
X = Last block of preceding directory
Y = Last block of preceding library

[1] Optional user volume labels if written will be in the same block following the system volume label.

[2] Using the Restore program you may allocate a label information area different than the default size of 200 blocks.

Figure 13. System Residence Organization on FBA

Notes to Figure 12

The disk device can be an IBM 2314, an IBM 2319 or an IBM 3333/3330/3330-11/3340/3350. The organization of SYSRES is as follows:

IPL

This area contains the initial program load (IPL) bootstrap program, which causes the IPL retrieval program to be read from SYSRES and loaded into real storage.

System Volume Label

The volume label (VOL1 label) contains the address of the volume table of contents (VTOC) established when the pack was initialized.

User Volume Label

The user volume label area is provided for any additional standard volume labels (VOL2-VOL8 labels). This area can extend from record 4 through the end of track 0.

System Directory

This area contains the system (master) directory. Record 1 contains the location of the core image directory and the address of the label information area. Records 2, 3, and 4 contain the starting addresses of the relocatable directory, source statement directory, and procedure directory, respectively. Record 5 contains the IPL retrieval program.

Core Image Directory

This directory consists of two or more tracks, depending on the allocation specified by the user. The directory is in two parts: The first is the directory of cataloged phases; the second is the directory of linked phases.
Each directory entry describes one phase in the core image library and contains such information as the phase name, loading address, number of blocks, type of phase, entry point, starting disk address in the core image library, and the number of text bytes in the last block. The entries are sorted in alphanumeric sequence.
The first entry in the directory is called the library descriptor entry. This contains such informations as the number of directory tracks, library cylinders, active phases, directory blocks available, and library blocks available.
Thereafter, the entries have a length varying from 14 bytes to 34 bytes (depending on the specifications in the PHASE statement). Entries are grouped in blocks of 256 bytes, plus an 8-byte key for the highest phase name in the block.

Core Image Library

The core image library consists of one or more complete cylinders, depending on the allocation specified by the user.

Relocatable Directory

This directory consists of one or more tracks, depending on the allocation specified by the user. It contains two types of information:

1. System directory information for the relocatable directory and library. This information occupies the first five entries of the first record in the relocatable directory.

2. An entry that describes each module (the output of a complete language translator run) in the relocatable library and contains: the module name, total number of text-record blocks required to contain this module, starting disk address of the first text-record of this module, and change level identification.

Relocatable Library

The relocatable library consists of one or more complete cylinders, depending on the allocation specified by the user. The number of modules and the size of each module to be contained in this library dictate the number of tracks

that must be allocated.

Source Statement Directory

This directory consists of one or more tracks, depending on the allocation specified by the user. It contains two types of information:

1. System directory information for the source statement directory and library. This information occupies the first five entries of the first record in the source statement directory.

2. An entry that describes each book (a sequence of source language statements in a compressed card image format, accessed by a single name) in the source statement library and contains: a sublibrary prefix, the book name, starting disk address of the first block of this book, total number of blocks required to contain this book in the source statement library, and change level information.

Source Statement Library

The source statement library consists of one or more complete cylinders depending on the allocation specified by the user. The number of blocks and the size of each book to be contained in this library dictates the number of tracks that must be allocated.

Procedure Directory

This directory consists of one or more tracks depending on the allocation specified by the user. It contains two types of information:

1. System directory information for the procedure directory and procedure library. This information occupies the first five entries of the first record in the procedure library.

2. An entry that describes each procedure (a set of control statements in card image format) catalogued in the procedure library and contains: the name of the procedure, the starting disk address of the procedure, the number of blocks occupied in the procedure library and a version and modification level.

Procedure Library

The procedure library consists of one or more complete cylinders, depending on the allocation specified by the user. Each procedure consists of one or more consecutive 80-byte blocks, containing control statements (one card image per block).

Label Information Area

The label information area contains standard, partition standard, and user label information for all partitions. This area is allocated 2 cylinders on the 3333/3330/3330-11, 2 cylinders on the 2314/2319, 3 cylinders on the 3340, or 1 cylinder on the 3350. Job Control stores label information found in job control statements here. The label information area follows the last library and ends the SYSRES file.

Volume Table of Contents

Following the label information area, the use of the remaining areas on the disk pack is left to the user's discretion. However, the volume table of contents (VTOC) must be contained on the same physical disk pack as the SYSRES file. (A VTOC is required on every disk pack.) The VTOC is most frequently the last cylinder before the alternate track area. The location and length of the VTOC are determined when the pack is initialized.

The VTOC is a file describing the organization of the disk pack. It contains the VTOC identifier (format 4 label)

that contains the starting and ending addresses of the VTOC, a format 5 label that is not used by DOS/VS, and format 1, 2, and 3 labels that identify and describe all files on the pack. More specific information on label formats is contained in the DOS/VS DASD Labels, GC33-5375.

Alternate SYSRES Layout

The relocatable library, the source statement library, and the procedure library are shown as optional areas of the SYSRES file because these libraries are not essential for system operation. If desired, the relocatable and source statement libraries can be defined as private libraries; a private library for the procedure library is not supported. A private core image library can also be defined, but the system core image library must always be included on the SYSRES file.

PRE-PROCESSING

1. For each ESD item produced by a language translator, an input control dictionary entry is built at a fixed location in storage. In some cases this input control dictionary entry will be moved to the control dictionary during processing.

2. The input ESD type field is validated.

   - If it is a weak external, the ESD type field in the input control dictionary entry is set to ER and the NOAUTOL and WXTRN bits in CSWITCH are turned on.

   - If it is invalid, an error condition exists, the whole ESD card is ignored, and the next ESD card is processed.

3. Further pre-processing depends on the input ESD type.

   - For LD ESD input
     Each input LD ESD item has a pointer (ESID) to the linkage table control section. This pointer is used to determine whether an input ESD item has already been processed. The check is made by locating the corresponding linkage table entry and investigating the control dictionary number stored in this entry.
     If the number is:

zero	the ESD item pointed to by the LD has not yet been processed. The LD is then marked unassigned in CSWITCH of the input control dictionary entry.
negative	the entry is ignored and the next ESD item is processed.
positive	an entry already exists for the ESD item pointed to by LD. If the existing entry is of the type SD or CM, the LD is marked assigned, and the control dictionary number of the SD or CM is stored in the input control dictionary entry. If the entry is not of the type SD or CM an error condition exists.

   - For ER ESD input
     If NOAUTO has been requested for the phase being processed, the NOAUTOL bit in CSWITCH is set on. Otherwise, CSWITCH remains off.

   - For SD or PC ESD input
     Requirements:
     (1) The assembled origin must be aligned on a double word boundary.
     (2) PC must be unnamed.

     The relocation factor is calculated by subtracting the assembled origin from the storage address (NXPHRG).

     For a normal INCLUDE the pre-processing is finished at this stage.

     For a submodular INCLUDE the name list of included CSECTs is scanned for a name identical to the name of the input control dictionary entry. If the names match, pre-processing is finished. If not, the ESD type field in the input control dictionary entry is changed to ER and a switch is set to ensure that the control dictionary number in the linkage table is given a negative value.

     Note: A negative control dictionary number in the linkage table entry is a signal for the ESD processor to ignore LDs belonging to this section definition, and for the text processor to ignore the corresponding text cards.

PROCESSING

1. The control dictionary is scanned for an entry with the same name as the input ESD item.

   This scan starts at the end of the control dictionary and proceeds towards the beginning until either a match occurs or the beginning of the control dictionary is reached. If a match occurs, the control dictionary entry is called a duplicate.

   The scan continues if the duplicate is a phase entry.

2. If no duplicate is found, the input control dictionary entry is added to the end of the control dictionary.

3. If the input ESD is an SD, PC, CM, or ER, an entry is made in the linkage table.

4. If a duplicate was found, the action taken by the ESD processor depends on the relationship between input and duplicate. Use Figures 14 - 18 to determine the different actions taken by the ESD processor.

A summary of all possible ESD processing actions is shown in Fig. 14. The actions are named A1 - Err-46. To find out the appropriate action(s) taken during input processing of CM, ER, SD, or LD use Fig. 15, 16, 17, 18 respectively. The upper part of these figures shows the various conditions which exist (Y), not exist (N), or can be ignored (-), while the lower part indicates the actions taken (X).

Name	Description
A1	Ignore input control dictionary entry.
A2	Add input control dictionary entry to the end of the control dictionary.
A3	Replace duplicate with the input control dictionary entry.
A4*	Add the linkage table entry pointing to the last entry added to the control dictionary.
A5*	Add the linkage table entry pointing to the duplicate.
A6	Change duplicate LD to LR.
A7	Continue scan of the control dictionary.
A8	Save length of longest CM in the control dictionary.
A9	Give control dictionary number in linkage table a negative value.
A10	Change input LD to LR.
A11	Set 'Possible Duplicate Entry' switch.
Err-40	Print error message '2140I' and go to RDNEXT.
Err-43	Print error message '2143I' and go to RDNEXT.
Err-46	Print error message '2146I' and go to RDNEXT.

* If a submodular INCLUDE was used and the name list of included SDs does not contain an SD, the control dictionary number in the linkage table is given a negative value.

Figure 14. ESD Processing Actions

Duplicate = SD	Y	N	N	N	N
= PC	N	Y	N	N	N
= CM	N	N	Y	N	N
= LD/LR	N	N	N	N	Y
= ER	N	N	N	Y	N
A3	-	-	-	X	-
A4	-	-	-	-	-
A5	X	-	X	X	-
A7	-	X	-	-	-
A8	-	-	X	-	-
Err-46	-	-	-	-	X

Figure 15. Process Input CM

Duplicate = SD, LD, or LR	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	N	N	Y
= LD	-	-	N	N	N	N	Y	Y	Y	Y	N	N	N	N	-
= CM	N	N	N	N	N	N	N	N	N	N	Y	N	N	N	N
= ER	N	N	N	N	N	N	N	N	N	N	N	Y	Y	Y	N
Duplicate unassigned *	N	N	N	N	N	N	N	N	N	N	-	-	-	-	Y
Name = 'IJ..' or 'IBM..'	Y	Y	Y	Y	Y	N	Y	Y	Y	N	-	-	-	-	-
Name = 'IBM..'	N	Y	-	-	N	-	-	-	N	-	-	-	-	-	-
NOAUTO for input	N	N	Y	N	N	-	Y	N	N	-	-	-	Y	N	-
Duplicate in current phase	N	N	-	Y	N	-	-	Y	N	-	-	N	Y	Y	-
Duplicate in ROOT phase	N	-	-	-	Y	-	-	-	Y	-	-	-	-	-	-
A2	X	X	-	-	-	-	-	-	-	-	-	-	-	-	-
A3	-	-	-	-	-	-	-	-	-	-	-	X	-	X	-
A4	X	X	-	-	-	-	-	-	-	-	-	-	-	-	-
A5	-	-	X	X	X	X	X	X	X	X	X	X	X	X	-
A6	-	-	-	-	-	-	-	X	X	X	X	-	-	-	-
A7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X

* SD is to be considered assigned

Note: Weak externals are processed like ERs for which NCAUTO is requested.

Figure 16. Process Input ER

Duplicate = SD	N	N	N	N	Y	Y	Y	Y	N	N	N	N	N	N	N	N	N
= CM	Y	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
= LD or LR	N	N	N	N	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y
= ER	N	Y	Y	Y	N	N	N	N	N	N	N	N	N	N	N	N	N
Duplicate unassigned	-	-	-	-	-	-	-	-	N	N	N	Y	Y	Y	Y	Y	Y
Input and duplicate ESIDs agree	-	-	-	-	-	-	-	-	-	-	-	N	N	N	Y	Y	Y
ASSORGs agree	-	-	-	-	-	-	-	-	-	-	-	-	-	-	N	N	N
Duplicate in current phase	-	-	Y	N	Y	N	N	N	-	Y	N	-	Y	N	-	Y	N
Name = 'IBM..'	-	N	Y	Y	-	Y	N	N	N	Y	Y	N	Y	Y	N	Y	Y
Duplicate in ROOT phase	-	-	-	-	-	-	-	N	Y	-	-	-	-	-	-	-	-
A2	-	-	-	X	-	X	X	-	-	-	X	-	-	X	-	-	X
A3	X	X	X	-	-	-	-	-	-	-	-	-	-	-	-	-	X
A4	-	-	-	X	-	X	X	-	-	-	X	-	-	X	-	-	X
A5	X	X	X	-	X	-	-	X	-	-	-	-	-	-	-	-	X
A9	-	-	-	-	-	X	-	-	X	-	-	-	-	-	-	-	-
Err-43	-	-	-	-	-	-	-	-	-	X	X	-	X	X	-	X	X

Figure 17. Process Input SD

Duplicate = SD, LD, or LR	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
= CM	Y	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
= LD or LR	N	N	N	N	-	-	-	-	-	Y	Y	Y	Y	Y	Y	Y	N	N	N	N
= ER	N	Y	Y	Y	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
Duplicate unassigned **	-	-	-	-	N	N	N	N	N	N	N	N	N	N	N	Y	-	-	-	-
Input unassigned	-	-	-	-	-	-	-	-	Y	Y	N	N	N	N	N	N	-	N	N	N	N
Input points to duplicate SD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Y	N	N	N
Input and duplicate point to same C/E entry	-	-	-	-	-	-	-	-	-	-	Y	N	N	N	N	N	-	-	-	-	-
Names of C/D entries agree	-	-	-	-	-	-	-	-	-	-	-	N	N	N	Y	Y	-	-	-	-	-
Name of Input and Dupl = 'IBM..'	-	N	Y	Y	N	Y	Y	-	-	-	N	Y	Y	-	-	-	-	N	Y	Y
Duplicate in current phase	-	-	Y	N	-	N	Y	N	Y	-	-	N	Y	N	Y	-	-	-	N	Y
Input and duplicate ASSORGs agree	-	-	-	-	-	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y	-	Y	Y	Y	Y
A1	-	-	-	-	-	-	-	-	-	X	X	-	-	-	-	X	-	X	-	-	-
A2	-	-	-	X	-	X	-	X	-	-	-	X	-	X	-	-	-	-	X	-	
A3	-	X	X	-	-	-	-	-	-	-	-	-	-	-	-	-	X	*-	-	-	-
A10	-	X	X	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A11	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	X	X	-	-	-	-
Err-43	-	-	-	-	-	X	-	X	-	-	-	X	-	X	-	-	-	-	X	-	X
Err-46	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

* Action A3 is performed retaining the ESD type of the Duplicate
** SD is to be considered assigned

Figure 18. Process Input LD

POST-PROCESSING

- For ER, LD/LR, or CM ESD input the next ESD item is selected for processing.
- For SD or PC ESD input

  1. The control dictionary is scanned for unassigned LDs or LRs pointing to the input item.
  2. The control dictionary entries found during the previous scan are updated. This is done by storing in the control dictionary entry the control dictionary number found in the linkage table entry (that corresponds to the input item).
  3. The storage address (NXPHRG) is updated by adding the length of the control section to it.

  Note: If the length of the control section is provided in the END card, CSECT IJBOTH performs action 3.

For a detailed description of the Linkage Editor Map refer to:
DOS/VS Serviceability Aids and Debugging Procedures, GC33-5380.

Input List

```
JOB  NO NAME   06/28/77                          LINKAGE EDITOR DIAGNOSTIC OF INPUT

ACTION TAKEN  MAP REL
LIST   INCLUDE IJBSL1
LIST   PHASE DSERV,*,NOAUTO
LIST   INCLUDE  FBAEXCP
LIST   INCLUDE  IJJCPDV1
LIST   INCLUDE  ,(IJBDS050)
LIST   PHASE DSERVC,*,NOAUTO
LIST   INCLUDE  ,(IJBDSC)
LIST   PHASE DSERVF,*,NOAUTO
LIST   INCLUDE  ,(IJBDSF)
LIST   PHASE DSERV1,*,NOAUTO
LIST   INCLUDE  ,(IJBDS141)
LIST   PHASE DSERV2,DSERV1,NOAUTO
LIST   INCLUDE  ,(IJBDS250)
LIST   PHASE DSERV2F,DSERV1,NOAUTO
LIST   INCLUDE  ,(IJBDS25F)
LIST   PHASE DSERV3,DSERV1,NOAUTO
LIST   INCLUDE  ,(IJBDS350)
LIST   PHASE DSERV4,DSERV1,NOAUTO
LIST   INCLUDE  ,(IJBDS450)
LIST   PHASE DSERV5,DSERV1,NOAUTO
LIST   INCLUDE  ,(IJBDS550)
LIST   PHASE DSERV3F,DSERV1,NOAUTO
LIST   INCLUDE  ,(IJBDS35F)
LIST   PHASE DSERV6,DSERV1,NOAUTO
LIST   INCLUDE  ,(IJBDS650)
LIST   ENTRY
  |
  |
  |
  V
```

Figure 19. Linkage Editor Map (Part 1 of 3)

Format A

PHASE	XFR-AD	LOCORE	HICORE	DSK-AD	ESD TYPE	LABEL	LOADED	REL-FR
DSERV	01DEEC	01C078	01E877	011 05 09	CSECT	FBA	01C078	01C078
					* ENTRY	FBAEXCP	01C088	
					* ENTRY	FBAOPEN	01C994	
					* ENTRY	FBACLOSE	01CB78	
					* ENTRY	LASTADDR	01C988	
					* ENTRY	REGSV06	01CD84	
					* ENTRY	CCBADDR	01CDE4	
					* ENTRY	CCWADDR	01CDE8	
					* ENTRY	REGSV7F	01CE04	
					CSECT	IJJCPDV1	01DBE0	01DBE0
					ENTRY	IJJCPDV2	01DBE0	
					CSECT	IJBDS050	01DEA8	003808
					* ENTRY	R3564	01DEB2	
					ENTRY	IJJCPD3	01E360	
DSERVC	01E878	01E878	01EBD9	011 06 09	CSECT	IJBDSC	01E878	003808
DSERVF	01EBE0	01EBE0	01EE73	011 06 0A	CSECT	IJBDSF	01EBE0	003808
DSERV1	01EE78	01EE78	01F9FF	011 06 0B	CSECT	IJBDS141	01EE78	003808
					* ENTRY	STATTAB	01F9AE	
DSERV2	01EE78	01EE78	01F7BF	011 07 03	CSECT	IJBDS250	01EE78	002C80
DSERV2F	01EE78	01EE78	01FDDF	011 07 06	CSECT	IJBDS25F	01EE78	002338
DSERV3	01EE78	01EE78	01F2FF	011 07 0A	CSECT	IJBDS350	01EE78	0013D0
DSERV4	01EE78	01EE78	01F25F	011 08 01	CSECT	IJBDS450	01EE78	000F48
DSERV5	01EE78	01EE78	01F16F	011 08 02	CSECT	IJBDS550	01EE78	000B60
DSERV3F	01EE78	01EE78	01FC5F	011 08 03	CSECT	IJBDS35F	01EE78	000868
DSERV6	01EE78	01EE78	01F21F	011 08 07	CSECT	IJBDS650	01EE78	000580

Format A appears as the Linkage Editor Map if Core Image Library on CKD.
DSK-AD contains CCC HH RR in hexadecimal format.

Figure 19. Linkage Editor Map (Part 2 of 3)

Format B

PHASE	XFR-AD	LOCORE	HICORE	DSK-AD	ESD TYPE	LABEL	LOADED	REL-FR
DSERV	01EB84	01E878	01F49F	00006209	CSECT	IJJCPDV1	01E878	01E878
					ENTRY	IJJCPDV2	01E878	
					CSECT	IJBDS050	01EB40	002800
					* ENTRY	R356A	01EB4A	
					ENTRY	IJJCPD3	01EF80	
DSERVC	01F4A0	01F4A0	01F7D9	00006217	CSECT	IJBDSC	01F4A0	002800
DSERVF	01F7E0	01F7E0	01FA7B	00006219	CSECT	IJBDSF	01F7E0	002800
DSERV1	01FA80	01FA80	02C58F	00006221	CSECT	IJBDS141	01FA80	002800
					* ENTRY	STATTAB	02053E	
DSERV2	01FA80	01FA80	0203C7	00006227	CSECT	IJBDS250	01FA80	001CF0
DSERV2F	01FA80	01FA80	02C997	00006233	CSECT	IJBDS25F	01FA80	0013A8
DSERV3	01FA80	01FA80	01FF07	00006241	CSECT	IJBDS350	01FA80	000490
DSERV4	01FA80	01FA80	01FE7F	00006245	CSECT	IJBDS450	01FA80	000008
DSERV5	01FA80	01FA80	01FD77	00006247	CSECT	IJBDS550	01FA80	-0003F8
DSERV3F	01FA80	01FA80	02085F	00006249	CSECT	IJBDS35F	01FA80	-0006F0
DSERV6	01FA80	01FA80	01FE47	00006257	CSECT	IJBDS650	01FA80	-0014D0

Format B appears as the Linkage Editor Map of Core Image Library on FBA.
DSK-AD contains block number in decimal format.

Figure 19. Linkage Editor Map (Part 3 of 3)

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DOS/VSE Linkage Editor Logic

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