IBM Field Engineering

Maintenance Diagrams

Restricted Distribution

2091 Processing Unit--Volume 5

MSCE, PSCE, MC Operations; Power

Y22-6675-1

PREFACE

This is one of five volumes of the IBM 2091 Processing Unit, Field Engineering Maintenance Diagrams Manual (FEMDM). The organization of the FEMDM, the general content of each volume, and the form numbers of the five volumes are:

Title	Contents
Volume 1 - Diagnostic Techniques, ECAD's (Form Y22-6671)	DIAGNOSTIC TECHNIQUES Diagrams 1-1 to 1-XX ERROR CONDITIONS Diagrams 2-1 to 2-XX
Volume 2 - Data Flow; I, FXP, FLP, Functional Units (Form Y22-6672)	DATA FLOW Diagram 3-1 System Data Flow 3-2 I Unit Data Flow 3-3 Fixed Point Data Flow 3-4 Floating Point Data Flow 3-5 MSCE Data Flow 3-6 PSCE Data Flow 3-7 MC Data Flow 3-8 PSCE Storage Channel (SC) Data 3-9 System Control Panel 3-10 PSCE Control Panel FUNCTIONAL UNITS Diagrams 4-1 to 4-XX I Unit 4-100 to 4-1XX Fixed Point Unit 4-200 to 4-2XX Floating Point Unit
Volume 3 - MSCE, PSCE, MC, Functional Units (Form Y22-6673)	FUNCTIONAL UNITS (Cont'd) 4-300 to 4-3XX MSCE 4-400 to 4-4XX PSCE 4-500 to 4-5XX MC
Volume 4 - I, FXP, FLP Operations (Form Y22-6674)	OPERATIONS 5-1 to 5-XX I Unit Operations 5-100 to 5-1XX Fixed Point Operations 5-200 to 5-2XX Floating Point Operations
Volume 5 - MSCE, PSCE, MC Operations; Power (Form Y22-6675)	OPERATIONS (Cont'd) 5-300 to 5-3XX MSCE Operations 5-400 to 5-4XX PSCE Operations 5-500 to 5-5XX MC Operations POWER SUPPLIES 6-1 to 6-XX

Diagrams contained in this manual are referenced from the seven 2091 Field Engineering Theory of Operation Manuals (FETOM's). References to FEMDM diagrams take the form "Diagram 5-103"; references to figures in a FETOM take the form "Figure 3-22." The seven 2091 FETOM's are:

IBM 2091 Processing Unit, FE Theory of Operation Manuals:

System Introduction, Instruction Processor, Form Y22-6622

Power Supplies and Control, Form Y22-6623

Console and Maintenance Features, Form Y22-6624

Fixed Point Execution Element, Form Y22-6625

Main Storage Control Element, Form Y22-6626

Peripheral Storage Control Element, Form Y22-6627

Floating Point Execution Element, Form Y22-6628

Other FE Manuals containing information pertinent to the 2091 are:

2091 Processing Unit, FE Maintenance Manual, Form Y22-6659

2091 Processing Unit, 2395 Processor Storage, FE Installation Manual, Form Y22-6634

Advanced Solid Logic Technology Packaging, Tools, Wiring Change and Repair Procedures, FE Theory-Maintenance Manual, Form Y22-6620

Solid Logic Technology, Packaging, Tools, Wiring Change Procedure, FE Theory of Operation Manual, Form Y22-2800

Component Circuits -- SLT (Solid Logic Technology), SLD (Solid Logic Dense), ASLT (Advanced Solid Logic Technology), FE Theory of Operation Manual, Form Z22-2798 -- IBM Confidential

Power Supplies -- SLT (Solid Logic Technology), SLD (Solid Logic Dense), ASLT (Advanced Solid Logic Technology), FE Theory of Operation Manual, Form Y22-2799

Second Edition

This edition Form Y22-6675-1, is a major revision of and obsoletes, Form Y22-6675-0. Diagrams 5-309, 5-427 through 5-436, and 5-519 have been added. Diagrams 6-10, 6-12, and 6-14 have been deleted. Major changes have been made to Diagrams 5-403 through 5-407, 5-516, and 6-9. Minor changes have been made to most of the remaining diagrams. Changed or new diagrams are indicated by a page date of 3/68 and by a vertical line to the left of the diagram number on the Contents page.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest FE Publications Systems Sequence Listing for revisions or contact the local IBM branch office.

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ABBREVIATIONS

A	AND
AC	Address Check
Acc	Access; Accumulator
Acpt	Accept
Acptng	Accepting
Addr	Address
Adr	Address
Adv	Advance
AE	Address Exception
ALD	Automated Logic Diagram
Altr	Alteration
Amt	Amount
AOC	Array Out Counter
AR	Amplifier
Arg	Argument
Arg Wd	Argument Doubleword
AS	Accept Stack
ASLT	Advanced Solid Logic Technology
ATI	Auxiliary Tape Input
Avail	Available
B	Bit
BAB	Byte Address Buffer
BAC	Buffer Address Counter
BAL	(Mnemonic)Branch and Link (RX)
BALR	(Mnemonic) Branch and Link (RR)
BAR	Byte Address Register
BB	Bank Bit
BC	(Mnemonic) Branch on Condition; Bus Control
BCR	(Mnemonic) Branch on Condition (RR)
BCQT	Branch on Condition Quick Trigger
BCT	(Mnemonic) Branch on Count (RX)
BCTR	(Mnemonic) Branch on Count (RR)
BCU	Bus Control Unit
BCUNCONT	Unconditional Branch Trigger
Bd	Board
Bdy	Boundary
Bfr	Buffer
BIA	Branch In Array
BIAT	Back in Array Trigger
BOM	Basic Operating Memory
Br	Branch
BRT	Branch Trigger
BSM	Basic Storage Module
Bsy	Busy
BXH	(Mnemonic) Branch on Index High (RS)
BXLE	(Mnemonic) Branch on Index Low or Equal (RS)
BXQT	Branch on Index Quick Trigger
BZ	Busy
BZTP	Busy-to-Priority
BZTPSCE	Busy-to-PSCE
BZTR	Busy-to-Request
CAB	Channel Address Bus
CAR	Console Address Register;
CAR	Channel Address Register
CAW	Channel Address Word
C BACKL8 T	Condition Back Less than Eight Trigger
C BIA T	Conditional Back in Array Trigger
CBR	Console Buffer Register
CC	Command Counter; Condition Code
CCC	Common Channel Control
CCW	Channel Command Word
CD	Chain Data
CDB	Common Data Bus
CDBI	Console Data Bus In
CDBO	Console Data Bus Out
Ch	Channel
Chan	Channel
Ch Fr	Channel Frame
Chk	Check
Ck	Check
Chn	Chain
CIn	Carry In
CLC	(Mnemonic) Compare Logical (SS)
Clk	Clock
CM	Conditional Mode; Console Mode; Cripple Mode
Cncl	Cancel
Cndl	Conditional
Cnt	Count
CO	Conditional Op
Comp	Compare; Comparator
Cond	Condition
COut	Carry Out
CPA	Carry Propagate Adder
CPC	Cyclic Program Counter
CPE	Central Processing Element
Cpr	Computer
CPU	Central Processing Unit
C QUICK T	Conditional Quick Trigger
CR	Control Register
Crip	Cripple
CSA	Carry Save Adder
CSW	Channel Status Word
Ctl	Control
Ctr	Counter
Ctrl	Control
CV	Converter
CVB	(Mnemonic) Convert to Binary (RX)
CVD	(Mnemonic) Convert to Decimal (RF)
CXR	Console Auxiliary Register
D	Displacement
Dbl	Double
DC	Data Check; Display Check
Dcd	Decode
Dcdr	Decoder
Des	Designation
Det	Detection; Detector
DG	Display Gate
Diag	Diagnose
DIG	Data Ingate
Disp	Displacement
Dist	Distributor
Div	Divide
Dly	Delay, Delayed
Dlyd	Delayed
DM	Diagnostic Monitor
DOG	Data Outgate
DPC	Display Parity Check
Dsbl	Disable
Dt	Data
DW	Doubleword
DWC	Doubleword Counter
DWCR	Doubleword Count Register
EBA	Ending Byte Address
EBAR	Ending Byte Address Register
EBCDIC	Extended Binary Coded Decimal Interchange Code
EC	Engineering Change
ECAD	Error Check Analysis Diagram
ED	(Mnemonic) Edit (SS)
EDMK	(Mnemonic) Edit and Mark (SS)
EMS	Extended Main Storage (Same as LCS)
Eq	Equals
Err	Error
EX	(Mnemonic) Execute (RX)
Excpn	Exception
Exce	Execute
Exp	Exponent
FAU	Floating Point Add Unit
FE	Field Engineering
FEMDM	Field Engineering Maintenance Diagram Manual
FETOM	Field Engineering Theory of Operation Manual
FIFO	First-In, First-Out
Fir	First
FIWADFO	First-In-With-Available-Data, First-Out
FIWAMFO	First-In-With-Available-Memory, First-Out
FLA	Floating Point Area
FLB	Floating Point Buffer
FLBB	Floating Point Buffer Bus
Fld	Field
FLEU	Floating Point Execution Unit
FLIU	Floating Point Instruction Unit
FLOS	Floating Point Op Stack
FLP	Floating Point
FLR	Floating Point Register
FLRB	Floating Point Register Bus
FLU	Floating Point Unit
FMDU	Floating Point Multiply/Divide Unit
FP	Fetch Protect
FPA	Floating Point Area
Frm	Frame
Frac	Fraction
FS	False Start
FSB	Fixed Store Bus
Fth	Fetch
Fwd	Forward; Forwarding
FXA	Fixed Point/VFL Area
FXB	Fixed Point Buffer
FXEU	Fixed Point Execution Unit
FXIU	Fixed Point Instruction Unit
FXOS	Fixed Point Op Stack
FXP	Fixed Point

Objectives:

1. Priority decision is made each processor cycle.
2. Determines what information is to be gated to SAB during following cycle.

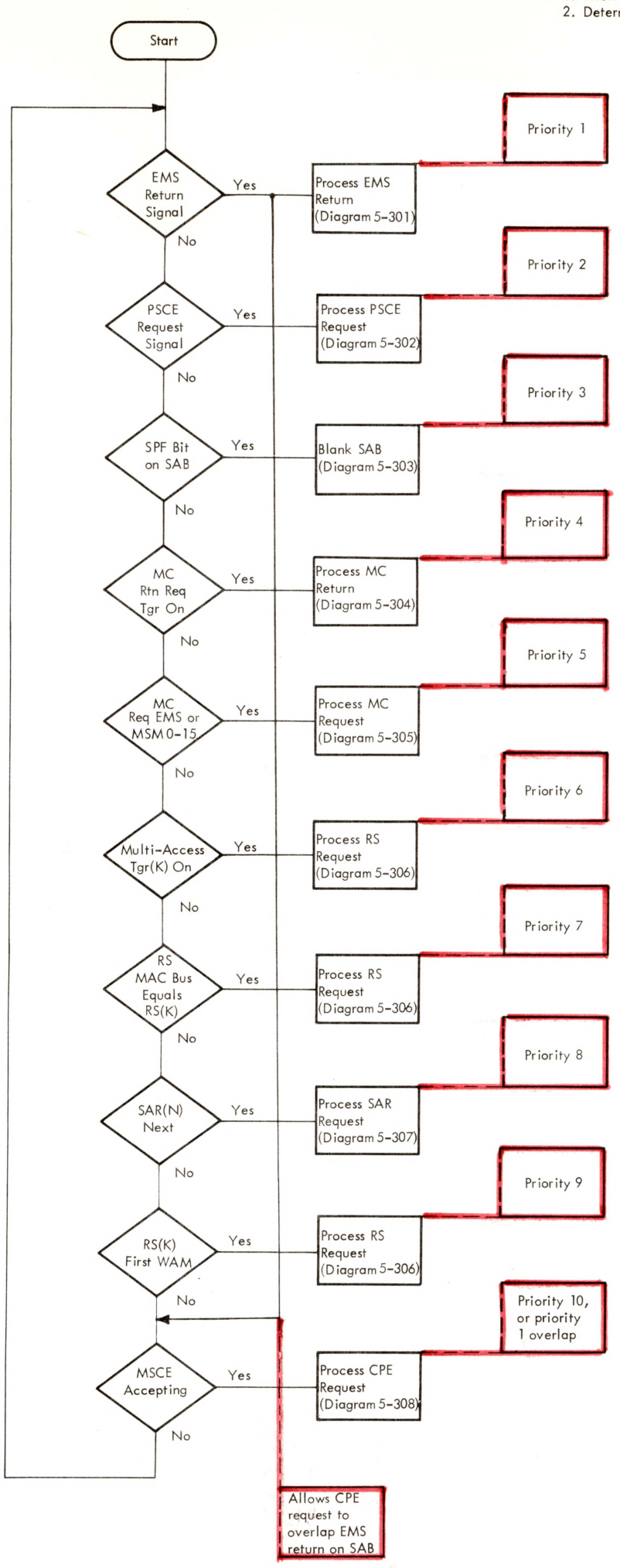


DIAGRAM 5-300. PRIORITY CYCLE (SIMPLIFIED)

Objectives:

1. EMS module is selected during CPE or MC fetch to EMS.
2. PSCE sends EMS return signal to MSCE.
3. EMS return bit is set in AS.
4. When bit is in AS position 8, sink address is gated from PSCE to CPE or MC via SB and sink address decoder.
5. When bit is in AS position 9, fetched data are gated from PSCE to CPE or MC via SBO.

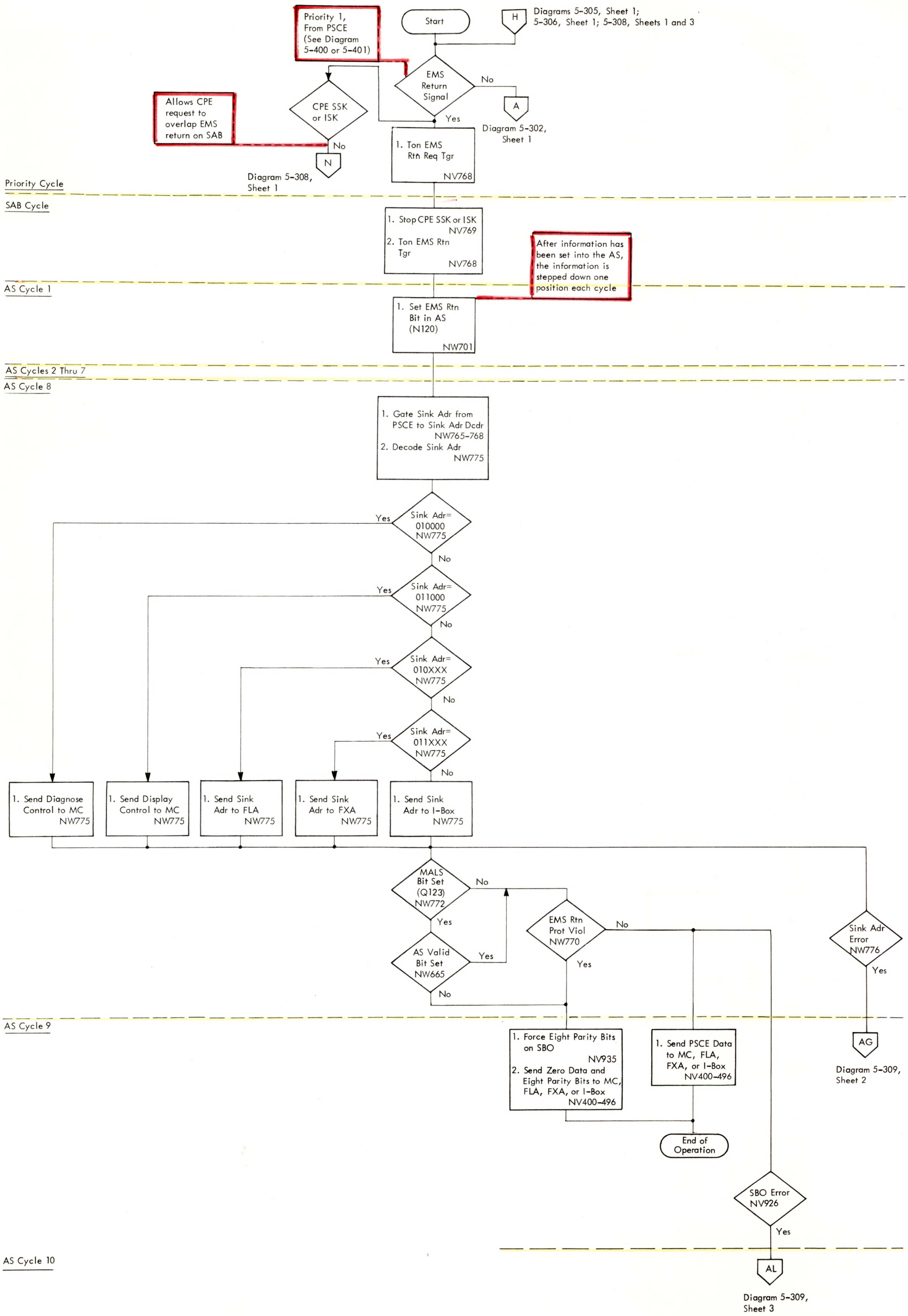


DIAGRAM 5-301. EMS RETURN (PRIORITY 1) (SHEET 1 OF 2)

EMS Return to FLA

No.	Note	Signal Name	ALD No.	Machine Cycles 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
					Pri	SAB	AS 1	AS 2	AS 3	AS 4	AS 5	AS 6	AS 7	AS 8	AS 9								
1	A	EMS Return	NT484																				
2		EMS Rtn Req Tgr	NV768	1 · Clk	$\overline{1}$ · Clk																		
3		Stop CPE SSK or ISK	NV769		2	$\overline{2}$																	
4		EMS Rtn Req Dly Tgr	NV768		3 · Clk	$\overline{3}$ · Clk																	
5		EMS Rtn Tgr	NV768			4 · Clk	$\overline{4}$ · Clk																
6		EMS Rtn Dly Tgr	NV768			5 · Clk	$\overline{5}$ · Clk																
7		AS 1 EMS Rtn Tgr	NW701				6 · Clk	$\overline{6}$ · Clk															
8		AS 1 EMS Rtn Lth	NW701				7 · Clk	$\overline{7}$ · Clk															
9		AS 2 EMS Rtn Tgr	NW701					8 · Clk	$\overline{8}$ · Clk														
10		AS 2 EMS Rtn Lth	NW701					9 · Clk	$\overline{9}$ · Clk														
11		AS 3 EMS Rtn Tgr	NW702						10 · Clk	$\overline{10}$ · Clk													
12		AS 3 EMS Rtn Lth	NW702						11 · Clk	$\overline{11}$ · Clk													
13		AS 4 EMS Rtn Tgr	NW702							12 · Clk	$\overline{12}$ · Clk												
14		AS 4 EMS Rtn Lth	NW702							13 · Clk	$\overline{13}$ · Clk												
15		AS 5 EMS Rtn Tgr	NW738								14 · Clk	$\overline{14}$ · Clk											
16		AS 5 EMS Rtn Lth	NW738								15 · Clk	$\overline{15}$ · Clk											
17		AS 6 EMS Rtn Tgr	NW738									16 · Clk	$\overline{16}$ · Clk										
18		AS 6 EMS Rtn Lth	NW738									17 · Clk	$\overline{17}$ · Clk										
19		AS 7 EMS Rtn Tgr	NW738										18 · Clk	$\overline{18}$ · Clk									
20		AS 7 EMS Rtn Lth	NW771										19 · Clk	$\overline{19}$ · Clk									
21		AS 8 EMS Rtn Tgr	NW771											20 · Clk	$\overline{20}$ · Clk								
22		AS 8 EMS Rtn Lth	NW771											21 · Clk	$\overline{21}$ · Clk								
23		AS 9 EMS Rtn Tgr	NW771												22 · Clk	$\overline{22}$ · Clk							
24		EMS Rtn Sink Adr Bits 1-5+P	NT747, NU048,049																				
25		EMS Rtn Sink Adr Lths	NW763,764											24 · Clk	$\overline{24}$ · Clk								
26		SA Bits 0-5+P	NW765-768											21-25	$\overline{21}$								
27	B	FLB Sink Adr Bits 3-5	NW775											26	$\overline{26}$								
28	C	Typical PSCE Data Bit (Bit 0)	NS022																				
29	C	Typical SBO Lth (Bit 0)	NV400												28 · Clk	$\overline{28}$ · Clk							

Notes:

A. Assume that the I-Box has sent a fetch request to the PSCE via the MSCE, and that EMS data are to be fetched and sent to the FLA.
B. An FLA sink address is decoded since data are being fetched for the FLA.
C. Since the skew latches for all bit positions of the SBO function similarly, only one latch is shown.

DIAGRAM 5-301. EMS RETURN (PRIORITY 1) (SHEET 2 OF 2)

PSCE Request

Objectives:

1. PSCE reserves desired MSM.
2. When MSM is available, PSCE request is gated to SAB.
3. MSM is selected, and store or fetch operation is performed.
4. For fetch operation, sink address is sent to PSCE one cycle ahead of fetched data.

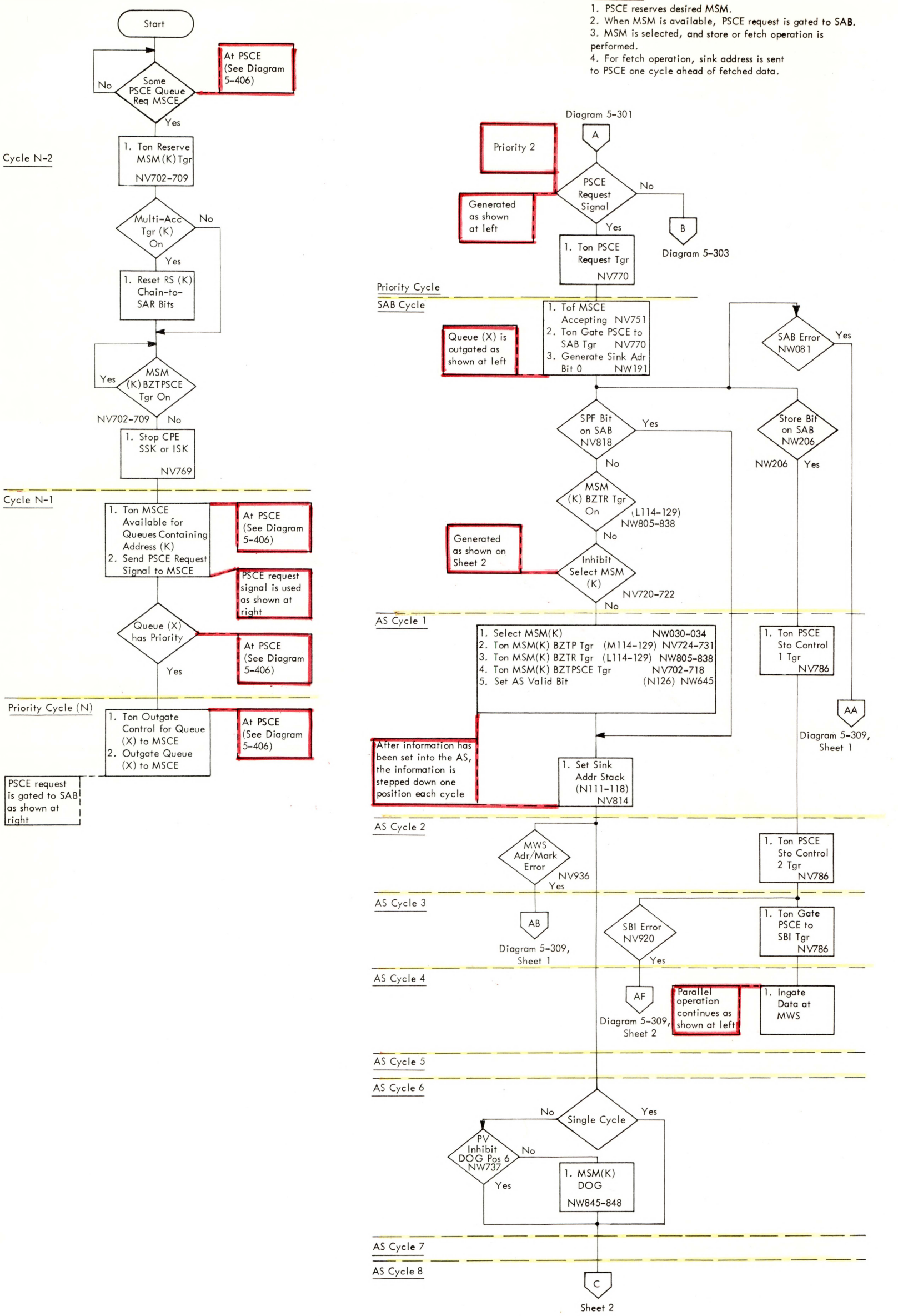


DIAGRAM 5-302. PSCE REQUEST (PRIORITY 2) (SHEET 1 OF 3)

AS Cycle 8

Sheet 1

C

1. Send Source/ Sink Adr to PSCE (Q111-118) NW775

Sink Adr Error NW776

Yes

AG

Diagram 5-309, Sheet 2

AS Cycle 9

Single Cycle

Yes

No

1. MSM(K)DOG NW845-848

No

PV Inhibit DOG Pos 9 NW762

Yes

PV Tgr 1 On NW762

Yes

No

1. Send MWS Data to PSCE NV400-496

Data are not ingated by PSCE during store operation

SBO Error NV926

Yes

Data are not ingated by PSCE during store operation

1. Force Eight Parity Bits on SBO NV935
2. Gate Zero Data and Eight Parity Bits to PSCE NV400-496

AS Cycle 10

1. Tof MSM(K) BZTPSCE Tgr NV702-718

AM

Diagram 5-309, Sheet 3

AL

Diagram 5-309, Sheet 3

AS Cycle 11

AS Cycle 12

1. Tof MSM(K) BZTP Tgr (M114-129) NV724-731

AS Cycle 13

1. Tof MSM(K) BZTR Tgr (L114-129) NW805-838

End of Operation

Inhibit Select

Start

RS(K) Decode Mem (K) NW471-475

No

Yes

Mem (K) BZTP (M114-129) NV724-731

Yes

No

Mem (K) Reserved NV700-718

Yes

No

RS (K) Chained to SAR NW420-429

Yes

No

(D115-117, E115-117, F115-117, G115-117)

MC Decode Mem (K) NW475

No

Yes

Mem (K) BZTP (M114-129) NV724-731

Yes

No

Mem (K) Reserved NV700-718

Yes

No

Mem (K) Reserved NV700-718

No

Yes

Gate PSCE to SAB NV770

Yes

No

Gate RS to SAB (J114-117) NV754-764

Yes

No

Gate MC to SAB NV766

Yes

No

Used as shown on Diagrams 5-302, Sheet 1; 5-305, Sheet 1; 5-306, Sheet 1; 5-307, Sheet 1; 5-308, Sheet 3

1. Inh Select Mem (K) NV720-722

DIAGRAM 5-302. PSCE REQUEST (PRIORITY 2) (SHEET 2 OF 3)

PSCE Store to MSM 0

No.	Note	Signal Name	ALD No.	Machine Cycles 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
									Pri	SAB	AS1	AS2	AS3	AS4	AS5	AS6	AS7	AS8	AS9	AS10	AS11	AS12	AS13
1	A	Reserve MSM 0	NU036																				
2		Reserve MSM 0 Tgr	NV702	1·Clk						$\overline{1}$·Clk													
3		MSM 0 Reserved-Inh Select	NV742	2·$\overline{9}$					9														
4	B	MSM 0 Busy-to-PSCE Tgr	NV702																				
5		MSM 0 Available to PSCE	NV742			2·$\overline{4}$				4													
6		PSCE Req	NT817																				
7		PSCE Req Tgr	NV770					6·Clk	$\overline{6}$·Clk														
8		PSCE Req Dly Tgr	NV770					7·Clk	$\overline{7}$·Clk														
9		Gt PSCE to SAB Tgr	NV770						8·Clk	$\overline{8}$·Clk													
10		Gt PSCE to SAB Dly Tgr	NV770						9·Clk	$\overline{9}$·Clk													
11	B	MSM 0 Busy-to-Request Tgr	NW805																				
12		Select MSM 0	NW031						5·$\overline{11}$·$\overline{Clk}$	Clk													
13	C	Typical AS1 Tgr (Adr Bit 11)	NW606																				
14	C	Typical AS1 Lth (Adr Bit 11)	NW606							13·Clk	$\overline{13}$·Clk												
15	C	Typical AS2 Tgr (Adr Bit 11)	NW606								14·Clk	$\overline{14}$·Clk											
16	C	Typical AS2 Lth (Adr Bit 11)	NW606								15·Clk	$\overline{15}$·Clk											
17	C	Typical AS3 Tgr (Adr Bit 11)	NW607									16·Clk	$\overline{16}$·Clk										
18	C	Typical AS3 Lth (Adr Bit 11)	NW607									17·Clk	$\overline{17}$·Clk										
19	C	Typical AS4 Tgr (Adr Bit 11)	NW607									18·Clk	$\overline{18}$·Clk										
20	C	Typical AS4 Lth (Adr Bit 11)	NW607									19·Clk	$\overline{19}$·Clk										
21	C	Typical AS5 Tgr (Adr Bit 11)	NW607										20·Clk	$\overline{20}$·Clk									
22	C	Typical AS5 Lth (Adr Bit 11)	NW607										21·Clk	$\overline{21}$·Clk									
23	C	Typical AS6 Tgr (Adr Bit 11)	NZ802											22·Clk	$\overline{22}$·Clk								
24	C	Typical AS6 Lth (Adr Bit 11)	NZ802											23·Clk	$\overline{23}$·Clk								
25	C	Typical AS7 Tgr (Adr Bit 11)	NZ802												24·Clk	$\overline{24}$·Clk							
26	C	Typical AS7 Lth (Adr Bit 11)	NZ802												25·Clk	$\overline{25}$·Clk							
27	C	Typical AS8 Tgr (Adr Bit 11)	NZ803													26·Clk	$\overline{26}$·Clk						
28	C	Typical AS8 Lth (Adr Bit 11)	NZ803													27·Clk	$\overline{27}$·Clk						
29	C	Typical AS9 Tgr (Adr Bit 11)	NZ803														28·Clk	$\overline{28}$·Clk					
30	C	Typical AS9 Lth (Adr Bit 11)	NZ803														29·Clk	$\overline{29}$·Clk					
31	C	Typical AS10 Tgr (Adr Bit 11)	NZ803															30·Clk	$\overline{30}$·Clk				
32	C	Typical AS10 Lth (Adr Bit 11)	NZ803															31·Clk	$\overline{31}$·Clk				
33		PSCE Sto Ctrl 1 Tgr	NV786							10·Clk	$\overline{10}$·Clk												
34		PSCE Sto Ctrl 1 Lth	NV786							33·Clk	$\overline{33}$·Clk												
35		PSCE Sto Ctrl 2 Tgr	NV786								34·Clk	$\overline{34}$·Clk											
36		PSCE Sto Ctrl 2 Lth	NV786								35·Clk	$\overline{35}$·Clk											
37		Gt PSCE to SBI Tgr	NV786									36·Clk	$\overline{36}$·Clk										
38	D	Typical PSCE Bit (Bit 0)	NS086																				
39	D	Typical PSCE SDB Tgr (Bit 0)	NV281									38·Clk	$\overline{38}$·Clk										
40	D	Typical SBI Bit (Bit 0)	NV200									37·39	$\overline{37}$										
41	E	MSM 0 DOG	NW845																				
42		SA Bits 0-5+P	NW765-768																				
43		PSCE Sink Adr Bits 0-5+P	NW765, 775															42	$\overline{42}$				

Notes:
A. Assume that PSCE is requesting MSM 0.
B. Assume that MSM 0 was selected by a previous request.
C. Since the triggers and latches for all bit positions of the AS function similarly, only one bit is shown being stepped down through the AS.
D. Since all PSCE bits are handled similarly, only one bit is shown.
E. The MSM 0 DOG is generated to gate the stored data onto the SBO to be parity checked.

DIAGRAM 5-302. PSCE REQUEST (PRIORITY 2) (SHEET 3 OF 3)

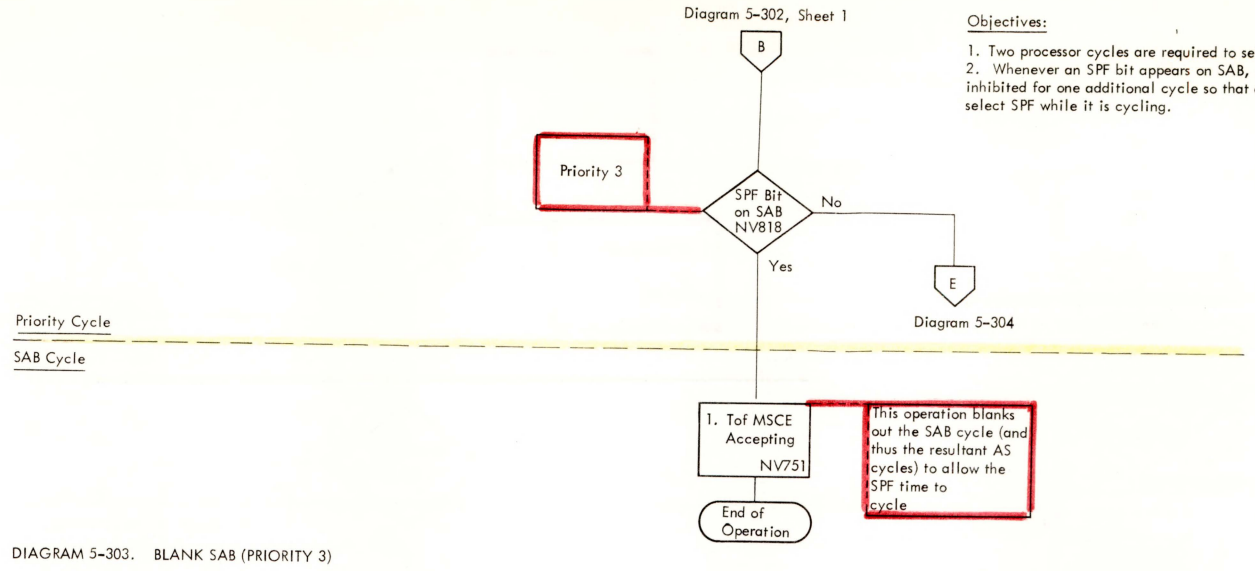
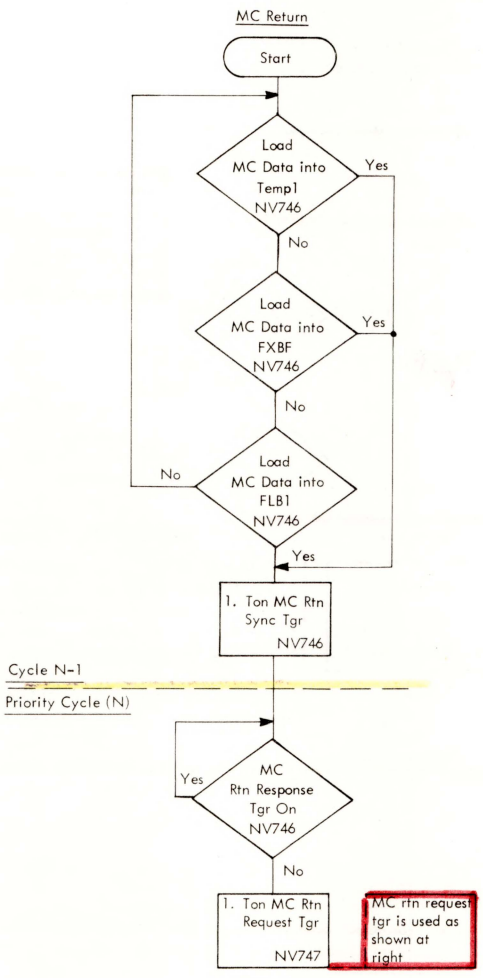


DIAGRAM 5-303. BLANK SAB (PRIORITY 3)

Objectives:

1. Two processor cycles are required to set a storage key into protect storage.
2. Whenever an SPF bit appears on SAB, gating of other requests to SAB is inhibited for one additional cycle so that an attempt will not be made to select SPF while it is cycling.



Objectives:

1. MC initiates loading of CPE buffer by sending control signal to MSCE.
2. MC return bit is set in AS.
3. When bit is in AS position 8, initiating control signal generates sink address which is supplied to CPE via SB and sink address decoder.
4. When bit is in AS position 9, data are gated from MC to CPE via SBO.

DIAGRAM 5-304. MC RETURN (PRIORITY 4)

MC Request

Objectives:

1. MSCE checks to make certain that desired MSM/PSCE is available.
2. MC request is gated to SAB.
3. MSM/PSCE is selected, and store or fetch operation is performed.
4. For fetch operation, a control signal (instead of a sink address) is sent to MC one cycle ahead of fetched data.

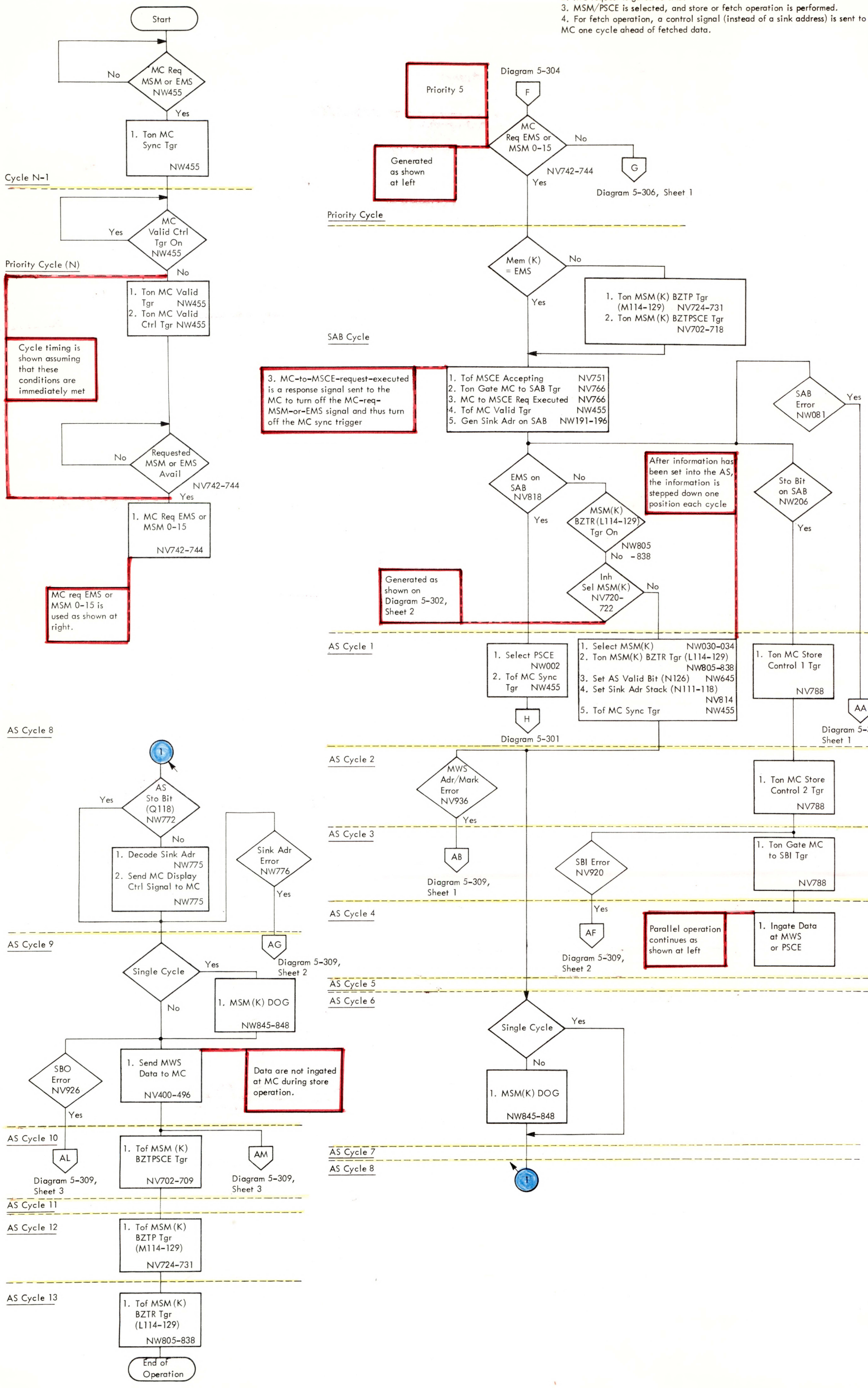


DIAGRAM 5-305. MC REQUEST (PRIORITY 5) (SHEET 1 OF 2)

MC Fetch From MSM 0

No.	Note	Signal Name	ALD No.	Machine Cycles 1	2	3 Pri	4 SAB	5 AS1	6 AS2	7 AS3	8 AS4	9 AS5	10 AS6	11 AS7	12 AS8	13 AS9	14 AS10	15 AS11	16 AS12	17 AS13	18	19	20
1		MC Req MSM or EMS	NY963																				
2		MC Sync Tgr	NW455	1 · Clk				$\overline{1}$ · Clk															
3		MC Valid Tgr	NW455	2·$\overline{4}$ · Clk			4·12 · Clk																
4		MC Valid Ctrl Tgr	NW455	3 · Clk				$\overline{2}$·$\overline{3}$ · Clk															
5	A	MC MSM 0	NW475																				
6	B	MSM 0 Busy-to-Priority	NV724			10 · Clk																	
7	B	MSM 0 Busy-to-Request	NW805																				
8		MSM 0 Available to MC	NV742		3·5·$\overline{6}$ 6																		
9		MC Req EMS or MSM 0-3	NV742		8 $\overline{8}$																		
10	C	Set Gate MC to SAB Tgr	NV766			9 · Clk $\overline{9}$ · Clk																	
11		Gate MC to SAB Tgr	NV766			10 · Clk $\overline{10}$ · Clk																	
12		MC Response Tgr	NV766				11 · Clk $\overline{11}$ · Clk																
13	D	SAB SA Bit 1, 2, P Tgrs	NW191, 192, 196			11 · Clk $\overline{11}$ · Clk																	
14	E	Select MSM 0	NW031			5·$\overline{7}$ · $\overline{\text{Clk}}$ Clk																	
15	F	Typical AS 1 Tgr (Adr Bit 11)	NW606																				
16	F	Typical AS 1 Lth (Adr Bit 11)	NW606				15 · Clk $\overline{15}$ · Clk																
17	F	Typical AS 2 Tgr (Adr Bit 11)	NW606					16 · Clk $\overline{16}$ · Clk															
18	F	Typical AS 2 Lth (Adr Bit 11)	NW606					17 · Clk $\overline{17}$ · Clk															
19	F	Typical AS 3 Tgr (Adr Bit 11)	NW607						18 · Clk $\overline{18}$ · Clk														
20	F	Typical AS 3 Lth (Adr Bit 11)	NW607						19 · Clk $\overline{19}$ · Clk														
21	F	Typical AS 4 Tgr (Adr Bit 11)	NW607							20 · Clk $\overline{20}$ · Clk													
22	F	Typical AS 4 Lth (Adr Bit 11)	NW607							21 · Clk $\overline{21}$ · Clk													
23	F	Typical AS 5 Tgr (Adr Bit 11)	NW607								22 · Clk $\overline{22}$ · Clk												
24	F	Typical AS 5 Lth (Adr Bit 11)	NW607								23 · Clk $\overline{23}$ · Clk												
25	F	Typical AS 6 Tgr (Adr Bit 11)	NZ802									24 · Clk $\overline{24}$ · Clk											
26	F	Typical AS 6 Lth (Adr Bit 11)	NZ802									25 · Clk $\overline{25}$ · Clk											
27	F	Typical AS 7 Tgr (Adr Bit 11)	NZ802										26 · Clk $\overline{26}$ · Clk										
28	F	Typical AS 7 Lth (Adr Bit 11)	NZ802										27 · Clk $\overline{27}$ · Clk										
29	F	Typical AS 8 Tgr (Adr Bit 11)	NZ803											28 · Clk $\overline{28}$ · Clk									
30	F	Typical AS 8 Lth (Adr Bit 11)	NZ803											29 · Clk $\overline{29}$ · Clk									
31	F	Typical AS 9 Tgr (Adr Bit 11)	NZ803												30 · Clk $\overline{30}$ · Clk								
32	F	Typical AS 9 Lth (Adr Bit 11)	NZ803												31 · Clk $\overline{31}$ · Clk								
33	F	Typical AS 10 Tgr (Adr Bit 11)	NZ803													32 · Clk $\overline{32}$ · Clk							
34	F	Typical AS 10 Lth (Adr Bit 11)	NZ803													33 · Clk $\overline{33}$ · Clk							
35		MSM 0 DOG	NW845																				
36		MC Display Mem Rtn Ctrl	NW775																				
37	G	Typical SBO Lth (Bit 0)	NV400																				

Notes:

A. Assume that MC is requesting MSM 0.
B. Assume that MSM 0 was selected by a previous request.
C. This trigger is set only if the MC request has priority.
D. Assume that MC request is for a fetch operation.
E. MSM 0 is selected at the end of the SAB cycle and remains selected until the end of AS cycle 13.
F. Since the triggers and latches for all bit positions of the AS function similarly, only one bit is shown being stepped down through the AS.
G. Since the skew latches for all bit positions of the SBO function similarly, only one latch is shown.

DIAGRAM 5-305. MC REQUEST (PRIORITY 5) (SHEET 2 OF 2)

Objectives:

1. Outgating of RS requests is controlled by: (1) multi-access triggers, (2) multi-access codes, and (3) RS priority and MSM/PSCE availability.
2. When an RS request is gated to SAB, requested MSM/PSCE is selected (unless previously selected, during multi-access) and appropriate store or fetch operation is performed.
3. For fetch operation, sink address is sent to CPE or sink control signal is sent to MC one cycle ahead of fetched data.

Priority 6

Turned on as shown on Diagrams 5-306, Sheet 1 and 5-307, Sheet 1

G — Diagram 5-305, Sheet 1

Multi-Access Tgr (K) On NV791-798 — No / Yes

Priority 7

Generated when an RS that contains a multi-access code is gated to the SAB

RS MAC Bus Equals RS (K) ' NW437-441 — No / Yes

L — Diagram 5-307, Sheet 1

Priority 9

Generated as shown on Diagram 5-308, Sheet 6

Diagram 5-307, Sheet 1 — M

RS(K) First WAM NV754-764 — No / Yes

N — Diagram 5-308, Sheet 1

Stop Multi-Access NV797 — Yes / No

L — Diagram 5-307, Sheet 1

Stop Multi-Access NV797 — Yes / No

Priority Cycle

SAB Cycle

1. Tof MSCE Accepting NV751

1. Tof MSCE Accepting NV751

1. Tof MSCE Accepting NV751

1. Tof Multi-Access Tgr (K) NV791-797

1. Reset RS(K) Chain-to-SAR Bits (D,E,F, G115-117) NW420-429

1. Ton Multi-Access Tgr(K) NV791-797

Used as shown at upper left

EMS on SAB NV818 — No / Yes

1. Ton MSM(K) BZTP Tgr (M114-129) NV724-731
2. Ton MSM(K) BZTPSCE Tgr NV702-718

1. Ton Gate RS(K) to SAB Tgr (J114-117) NV754-764
2. Reset RS(K) Chain-to-SAR Bits (D, E, F, G115-117) NW420-429

MAC on SAB = K NV795 — Yes

Any Reserve Tgr On NV700-718 — Yes / No

Priority 1-6 NV751 — Yes / No

Inhibit Multi-Access — Yes

Signal from MC

Generated as shown on Diagram 5-302, Sheet 2

EMS on SAB NV818 — No / Yes

MSM(K) BZTR Tgr On (L114-129) NW805-838 — No

Inhibit Select MSM(K) — No

Pseudo Select NW034 — Yes

Test and Set Bit on SAB NW207 — No

SDB(N) Designation on SAB NV781-783 — Yes

Allow Tof SAR Busy NV774 — No / Yes

1. Reset RS Chain-to-SAR(N) Bits (D,E,F,G115-117) NW420-429

After information has been set into AS, the information is stepped down one position each cycle

SAB Error NW081 — Yes

AA — Diagram 5-309, Sheet 1

AS Cycle 1

1. Ton Multi-Access Tgr(K) (H111-114) NV791-798

Used as shown above

1. Select PSCE NW002

H — Diagram 5-301

1. Select MSM(K) NW030-034
2. Ton MSM(K) BZTR Tgr (L114-129) NW805-838
3. Set AS Valid Bit (N126) NW645
4. Set Sink Adr Stack (N111-118) NV814

1. Set Allow Compare Bit NW608

Allows I-Box to load another store request into SAR(N)

1. Tof SAR(N) Busy in I-Box NV772-776

The allow compare bit is used in AS positions 1-5 to enable CPE-AS address compares for detecting multi-access situations on subsequent fetch requests from the CPE

1. Ton SDB(N) Store Control 1 Tgr NV781-783

AS Cycle 2

1. Ton SDB(N) Store Control 2 Tgr NV781-783

MWS Adr/ Mark Error NV936 — Yes

AB — Diagram 5-309, Sheet 1

AS Cycle 3

SBI Error NV920 — Yes

AF — Diagram 5-309, Sheet 2

1. Ton Gate SDB(N) to SBI Tgr NV781-783
2. Reset SDB(N) Full Bit (K127-129) NW230-232

AS Cycle 4

Parallel operation continues as shown at left

1. Ingate Data at MWS or PSCE

AS Cycle 5

AS Cycle 6

P — Sheet 2

DIAGRAM 5-306. RS REQUEST (PRIORITY 6, 7, OR 9) (SHEET 1 OF 2)

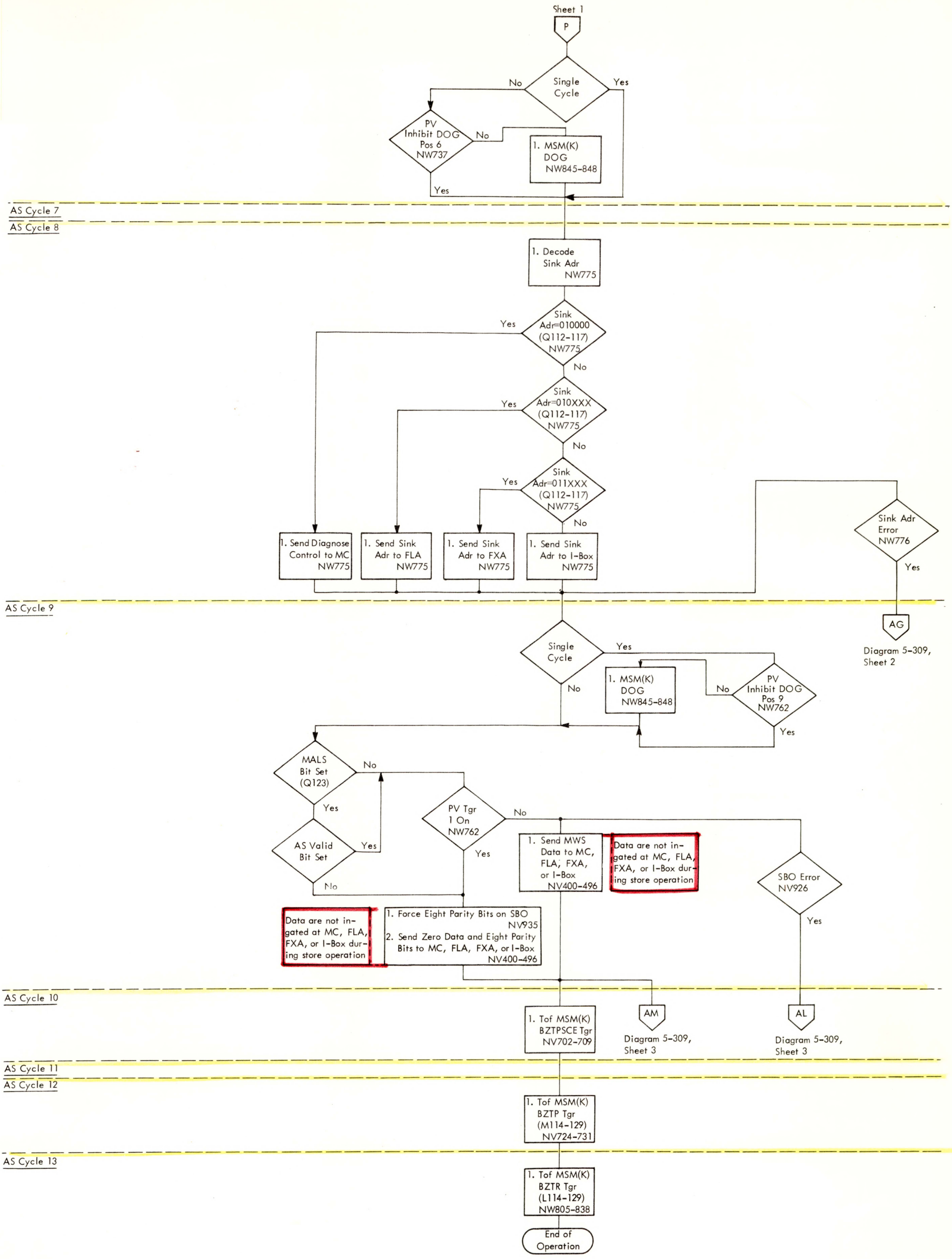


DIAGRAM 5-306. RS REQUEST (PRIORITY 6, 7, OR 9) (SHEET 2 OF 2)

Objectives:

1. SAR requests to different storage locations are outgated on first-in-with-available-data, first-out (FIWADFO) basis.
2. SAR requests to same storage location are outgated in first-in, first-out (FIFO) order.
3. When a SAR has priority, it is gated to SAB if an RS position is empty during gate-out cycle.
4. Requested MSM/PSCE is selected if available, and store or fetch operation is performed.
5. If requested MSM/PSCE is busy, SAR request is rejected into RS and then reinitiated when MSM/PSCE is available and RS posttion has priority (Diagram 5-306, Priority 9).

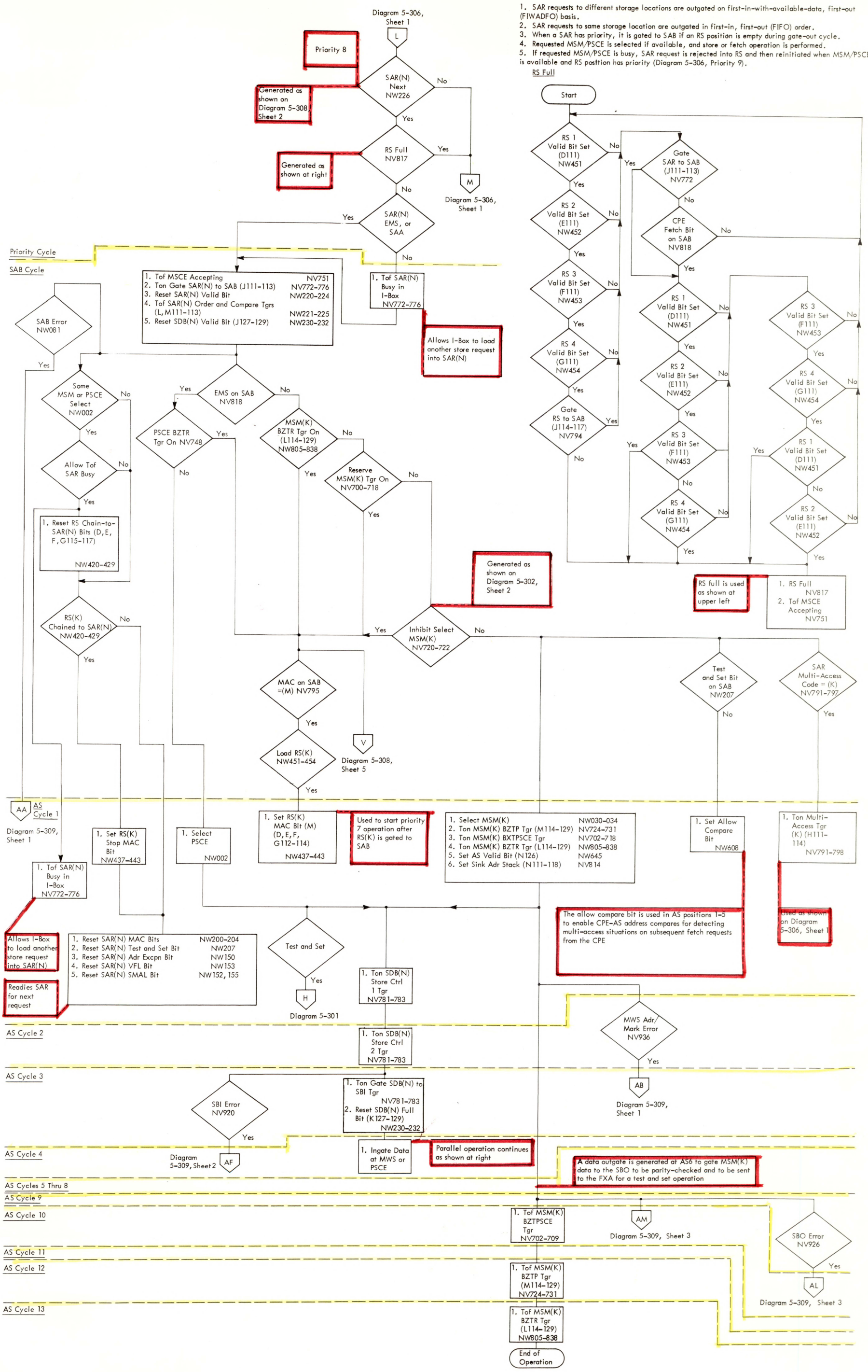


DIAGRAM 5-307. SAR REQUEST (PRIORITY 8)

Diagrams 5-301, Sheet 1; 5-306, Sheet 1

N

MSCE Accepting

No → H → Diagram 5-301

Yes

Priority 10, or priority 1 overlap

Objectives:

1. Issuing of CPE requests is controlled by MSCE accepting circuit in I-Box.
2. When CPE issues store request, request is loaded into a SAR until data have been loaded into corresponding SDB and SAR has priority. Store operation is then performed as shown on Diagram 5-307.
3. When CPE issues fetch request, MSM/PSCE is selected if available, and data are fetched and sent to CPE. If requested MSM/PSCE is not available, request is loaded into RS and then reinitiated when MSM/PSCE is available, as shown on Diagram 5-306.

Priority Cycle

SAB Cycle

1. I-Box Sends Request to SAB

Store Bit on SAB NW206

No

Yes

Test and Set Bit on SAB NW207

Yes

CPE Adr Comp with some SAR NW103-105

Yes

Some SAR Valid NW220-224

Yes

CPE Fetch Bit on SAB NV818

No

Yes

RS 1 Chained to SAR (D115-117) NW422

No

Yes

RS 2 Chained to SAR (E115-117) NW424

No

Yes

RS 3 Chained to SAR (F115-117) NW426

No

Yes

RS 4 Chained to SAR (G115-117) NW428

No

Yes

RS 1 Chained to SAR (D115-117) NW422

No

Yes

RS 2 Chained to SAR (E115-117) NW424

No

Yes

RS 3 Chained to SAR (F115-117) NW426

No

Yes

RS 4 Chained to SAR (G115-117) NW428

No

Yes

SAB Error NW081

Yes

AA

Diagram 5-309, Sheet 1

MSCE accepting is used as shown at upper left

1. Stop I-Box Storage Req NV819
2. Tof MSCE Accepting NV751

Shown on Diagram 4-303(R). Operate as follows:

Ingate	Adr Comp	Set
1	2	1C2
2	1	1C2
2	3	2C3
3	2	2C3
3	1	3C1
1	3	3C1

Shown on Diagram 4-303(R). Operate as follows:

Valid	Ingate	Set
2	1	1A2
3	2	2A3
1	3	3A1

SAR Cycles (Data Dependent Timing)

1. Load Store Request into SAR(N)
2. Set SAR(N) Valid Bit NW220-224

SAR(N) Test and Set Bit Set NW207

Yes

SDB(N) Full Bit Set (K127-129) NW230-232

No

PSW can be stored only via SDB 1

Yes

I-Box Store PSW

No

1. Load PSW into SDB 1 NV010-089

FXA Select SDB(N)

Yes

1. Load FSB Data into SDB(N) NV010-089

No

FLA Select SDB(N)

Yes

1. Ton SDB(N) Busy Tgr (H127-129) NV895-897

Sr Tag Reg(N) = 0000 (H, J, K123-126) NV883-890

Yes

No

Sr Tag Reg(N) = Bus Tag Reg NV883-890

No

Yes

Bus tag is loaded into bus tag reg each cycle (K119-122) NV881

1. Load CDB Data into SDB(N) NV010-089
2. Tof SDB(N) Busy Tgr (H127-129) NV895-897

No

SDB(N) Busy Tgr On (H127-129) NV895-897

No

1. Load Sr Tag into Sr Tag Reg(N) (H, J, K123-126) NV883-890

Source tag is loaded into source tag reg each cycle until FLA selects SDB(N)

S

T

Sheet 2

SAR(N) Conditional Bit Set NW151

Yes

In conditional operation, SDB(N) can be loaded only if an activate signal is received (Sheet 2)

1. Ton Appropriate Comp Tgrs (1C2, 2C3, 3C1) (M111-113) NW221-225

Used as shown on Sheet 2

1. Ton Appropriate Order Tgrs (1A2, 2A3, 3A1) (L111-113) NW221-225

No

CPE SMAL Bit

Yes

No

CPE Adr Comp with SAR(N) NW103-105

Yes

No

SAR(N) SMAL Bit Set NW152, 155

Yes

No

MALS Data Not Needed

Yes

1. SMAL Comp Data Not Needed NW156

Inhibits setting SAR MAC bits, RS MAC bits, and RS chain-to-SAR bits

No

Select PSCE NW002

Yes

1. Reject EMS Request NV815

U

Sheet 3

DIAGRAM 5-308. CPE REQUEST (PRIORITY 10, OR PRIORITY 1 OVERLAP) (SHEET 1 OF 6)

SAR Cycles
(Data Dependent Timing)

Sheet 1

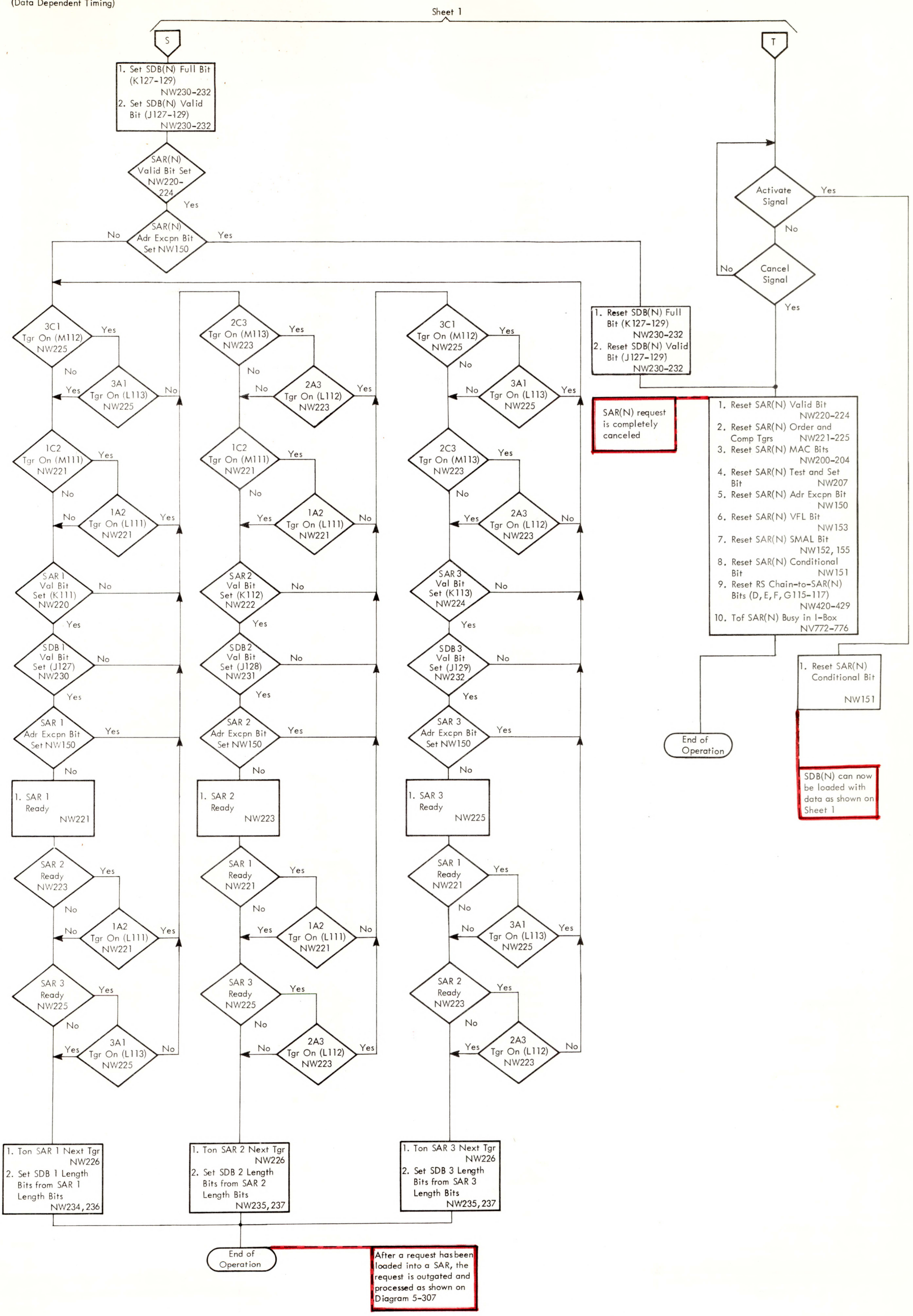


DIAGRAM 5-308. CPE REQUEST (PRIORITY 10, OR PRIORITY 1 OVERLAP) (SHEET 2 OF 6)

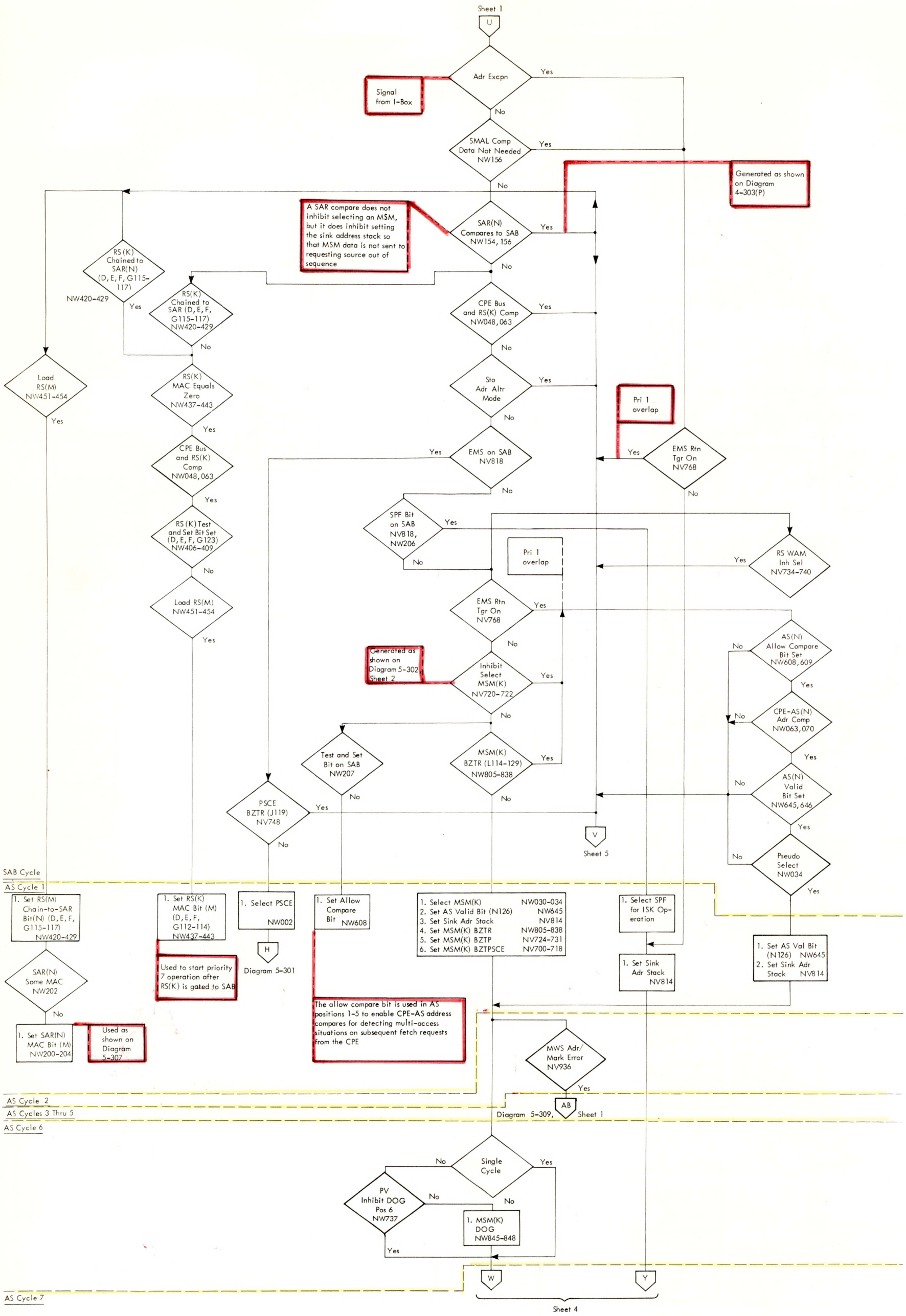


DIAGRAM 5-308. CPE REQUEST (PRIORITY 10, OR PRIORITY 1 OVERLAP) (SHEET 3 OF 6)

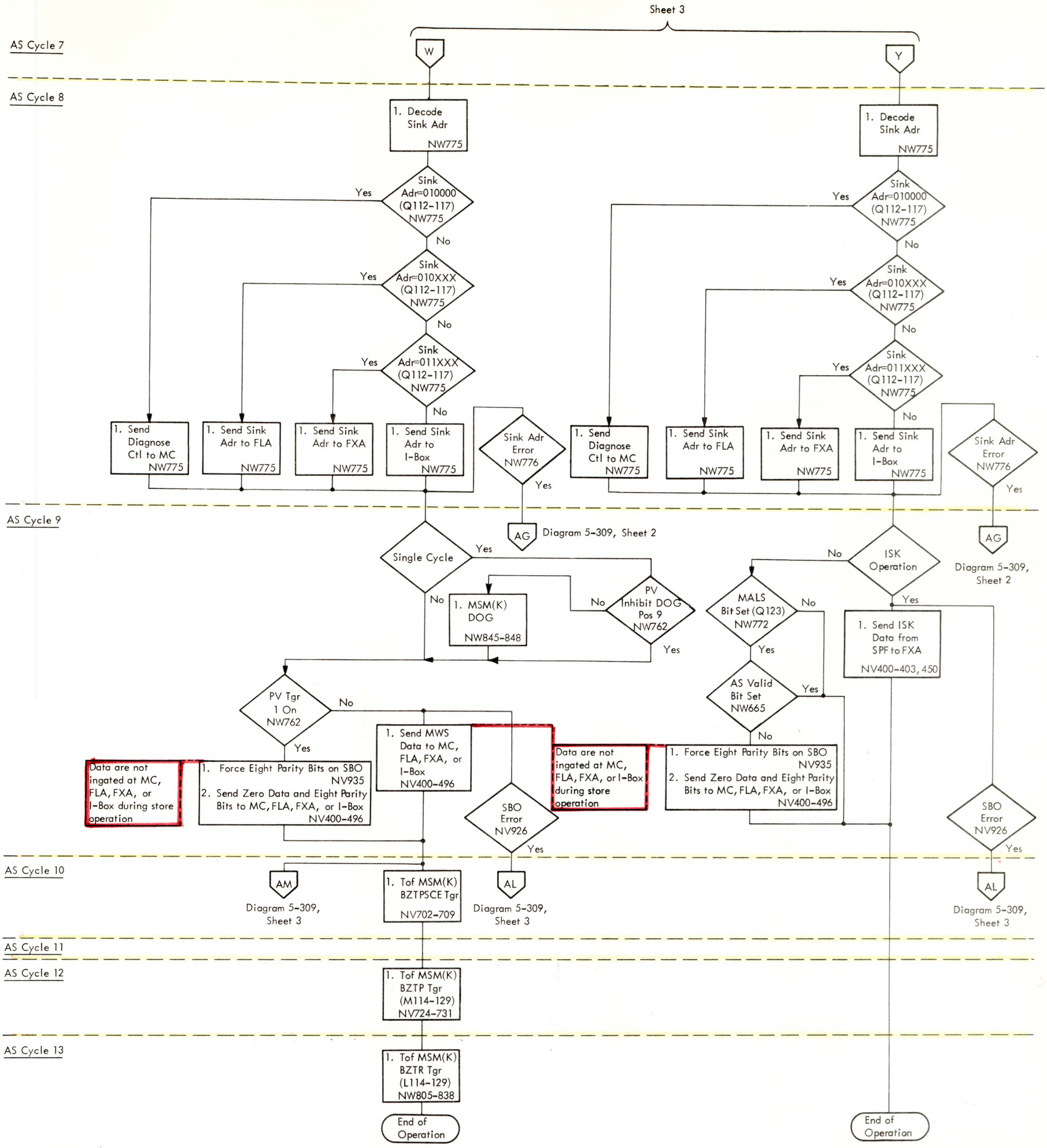
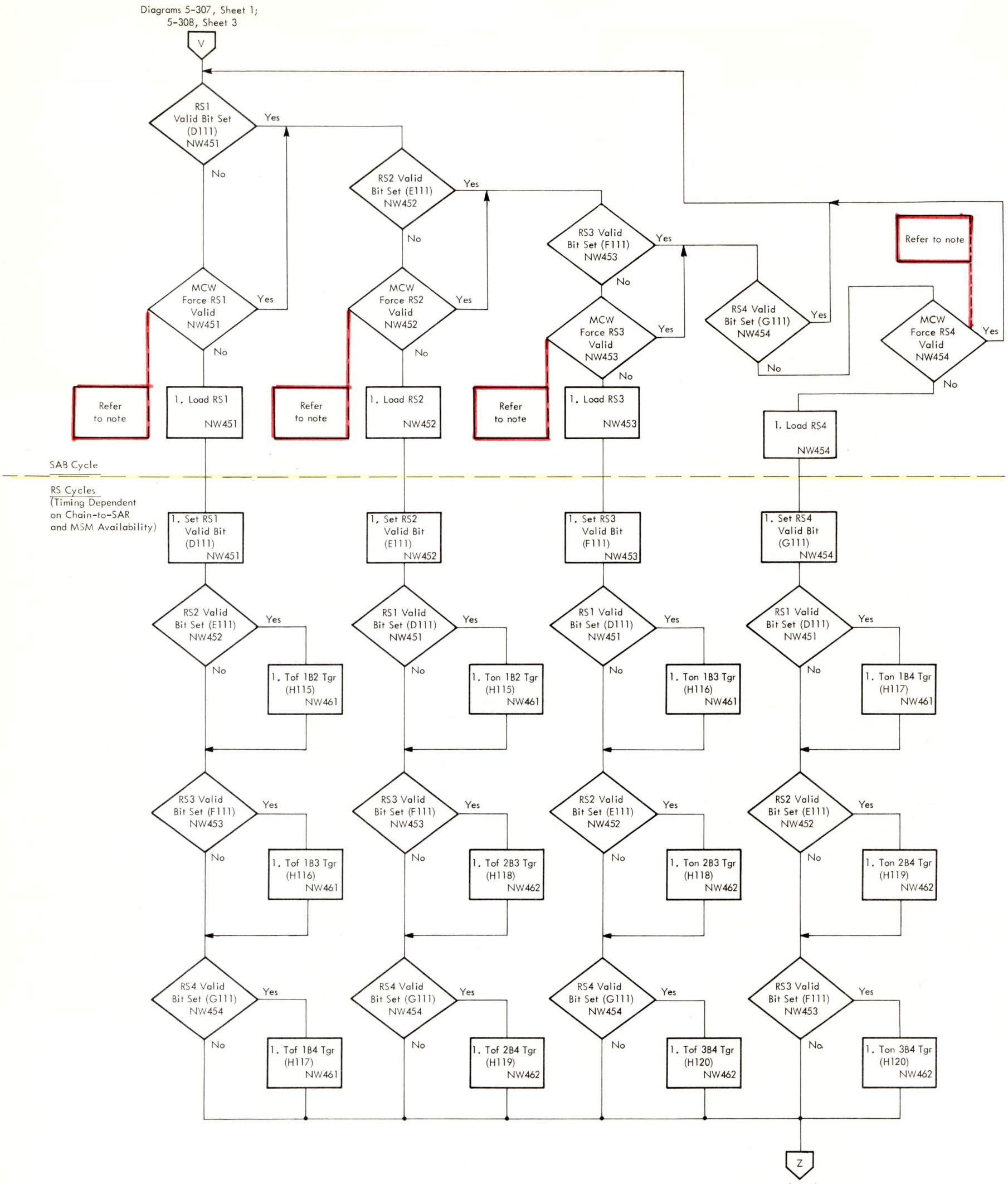


DIAGRAM 5-308. CPE REQUEST (PRIORITY 10, OR PRIORITY 1 OVERLAP) (SHEET 4 OF 6)



Note: MCW bits 25, 30, and 31 can be used to select the next RS position to be loaded:

MCW Bits 25	30	31	Enable Loading	Inhibit Loading (MCW Force Valid)
0	0	0	RS1-4 (Normal Operation)	-
1	0	0	RS1	RS2-4
1	0	1	RS2	RS1,3,4
1	1	0	RS3	RS1,2,4
1	1	1	RS4	RS1-3

DIAGRAM 5-308. CPE REQUEST (PRIORITY 10, OR PRIORITY 1 OVERLAP) (SHEET 5 OF 6)

RS Cycles (cont)
(Timing Dependent on Chain-to-SAR and MSM Availability)

Sheet 5

Z

RS1 Valid Bit Set (D111) NW451 — No / Yes

RS1 Chain-to-SAR(N) Bit Set (D115-117) NW422 — Yes / No

MSM(K) BZTP Tgr On (M114-129) NV724-731 — Yes / No

Reserve MSM(K) for PSCE Tgr On NV700-718 — Yes / No

1. Inhibit Select MSM(K) NV720-722

Sto Available for RS2 NV757 — No / Yes

1B2 Tgr On (H115) NW461 — No / Yes

Sto Available for RS3 NV760 — No / Yes

1B3 Tgr On (H116) NW461 — No / Yes

Sto Available for RS4 NV763 — No / Yes

1B4 Tgr On (H117) NW461 — No / Yes

1. RS1 First WAM NV754

RS2 Valid Bit Set (E111) NW452 — No / Yes

RS2 Chain-to-SAR(N) Bit Set (E115-117) NW424 — Yes / No

MSM(K) BZTP Tgr On (M114-129) NV724-731 — Yes / No

Reserve MSM(K) for PSCE Tgr On NV700-718 — Yes / No

1. Inhibit Select MSM(K) NV720-722

Sto Available for RS1 NV754 — No / Yes

1B2 Tgr On (H115) NW461 — Yes / No

Sto Available for RS3 NV760 — No / Yes

2B3 Tgr On (H118) NW462 — No / Yes

Sto Available for RS4 NV763 — No / Yes

2B4 Tgr On (H119) NW462 — No / Yes

1. RS2 First WAM NV757

RS3 Valid Bit Set (F111) NW453 — No / Yes

RS3 Chain-to-SAR(N) Bit Set (F115-117) NW426 — Yes / No

MSM(K) BZTP Tgr On (M114-129) NV724-731 — Yes / No

Reserve MSM(K) for PSCE Tgr On NV700-718 — Yes / No

1. Inhibit Select MSM(K) NV720-722

Sto Available for RS1 NV754 — No / Yes

1B3 Tgr On (H116) NW461 — Yes / No

Sto Available for RS2 NV757 — No / Yes

2B3 Tgr On (H118) NW462 — No / Yes

Sto Available for RS4 NV763 — No / Yes

3B4 Tgr On (H120) NW462 — No / Yes

1. RS3 First WAM NV760

RS4 Valid Bit Set (G111) NW454 — No / Yes

RS4 Chain-to-SAR(N) Bit Set (G115-117) NW428 — Yes / No

MSM(K) BZTP Tgr On (M114-129) NV724-731 — Yes / No

Reserve MSM(K) for PSCE Tgr On NV700-718 — Yes / No

1. Inhibit Select MSM(K) NV720-722

Sto Available for RS1 NV754 — No / Yes

1B4 Tgr On (H117) NW461 — Yes / No

Sto Available for RS2 NV757 — No / Yes

2B4 Tgr On (H119) NW462 — Yes / No

Sto Available for RS3 NV760 — No / Yes

3B4 Tgr On (H120) NW462 — Yes / No

1. RS4 First WAM NV763

End of Operation

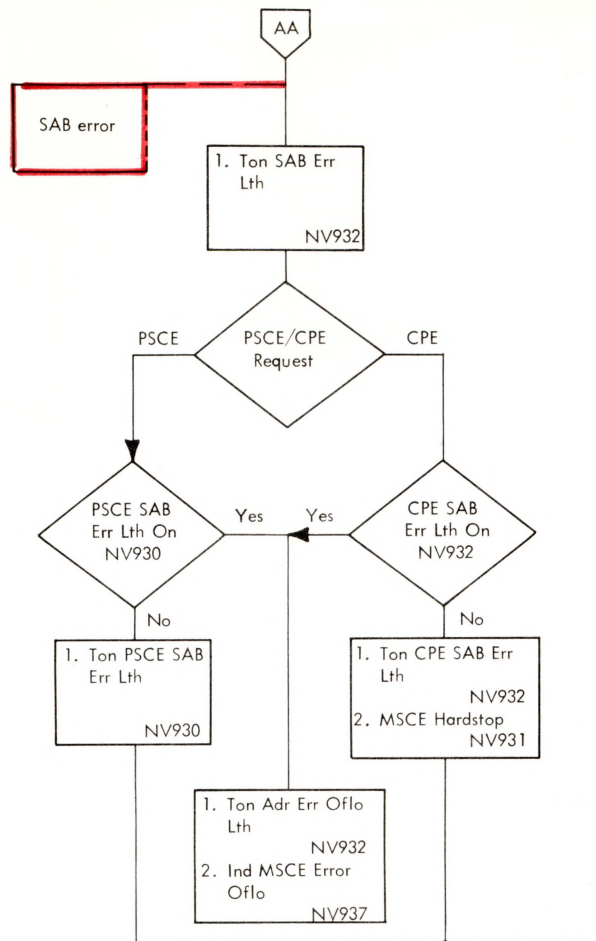
After a request has been loaded into the RS, the request is outgated and processed as shown on Diagram 5-306 (Priority 9)

DIAGRAM 5-308. CPE REQUEST (PRIORITY 10, OR PRIORITY 1 OVERLAP) (SHEET 6 OF 6)

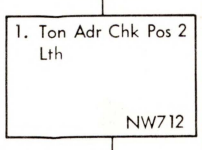
SAB Cycle	Address Check	Data Check	Address/Data Check	Snapshot Register

AS Cycle 1

Diagrams 5-302, Sheet 1; 5-305, Sheet 1; 5-306, Sheet 1; 5-307; 5-308, Sheet 1

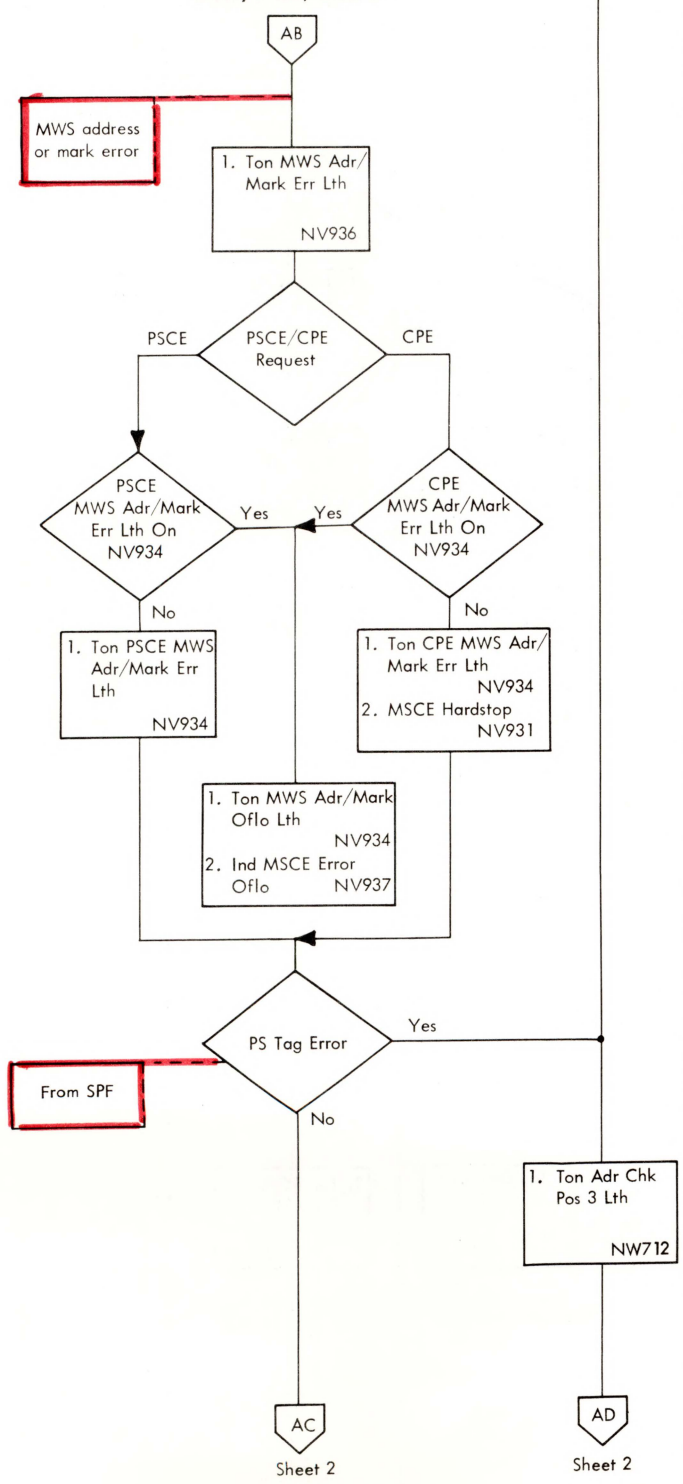


AS Cycle 2



AS Cycle 3

Diagrams 5-302, Sheet 1; 5-305, Sheet 1; 5-306, Sheet 1; 5-307; 5-308, Sheet 3



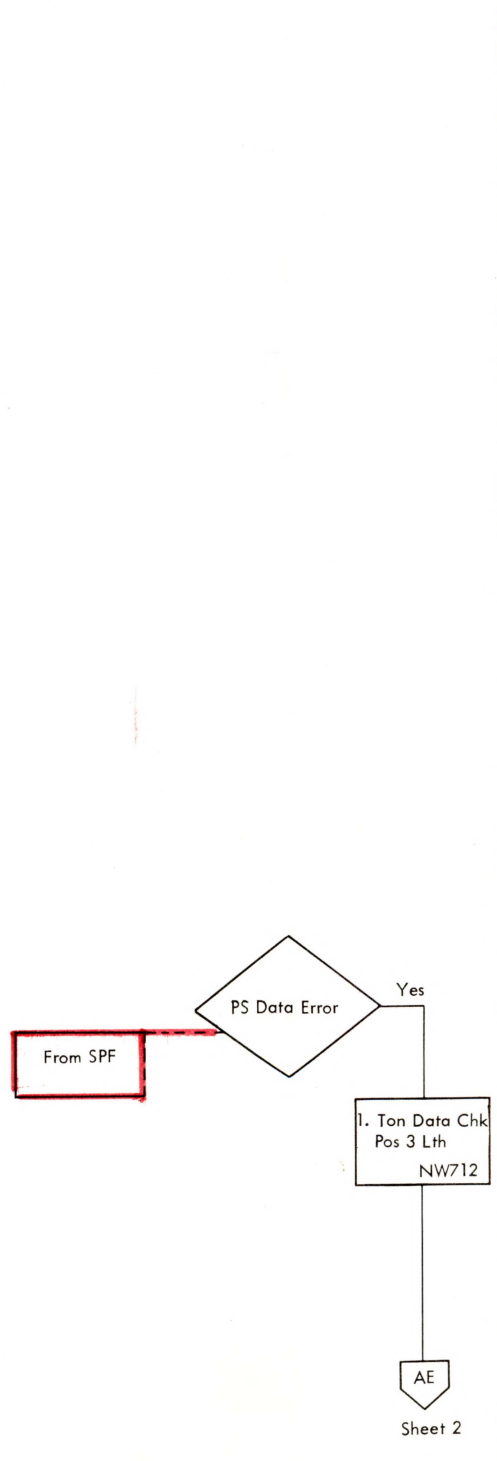


DIAGRAM 5-309. ADDRESS CHECK AND DATA CHECK (SHEET 1 OF 3)

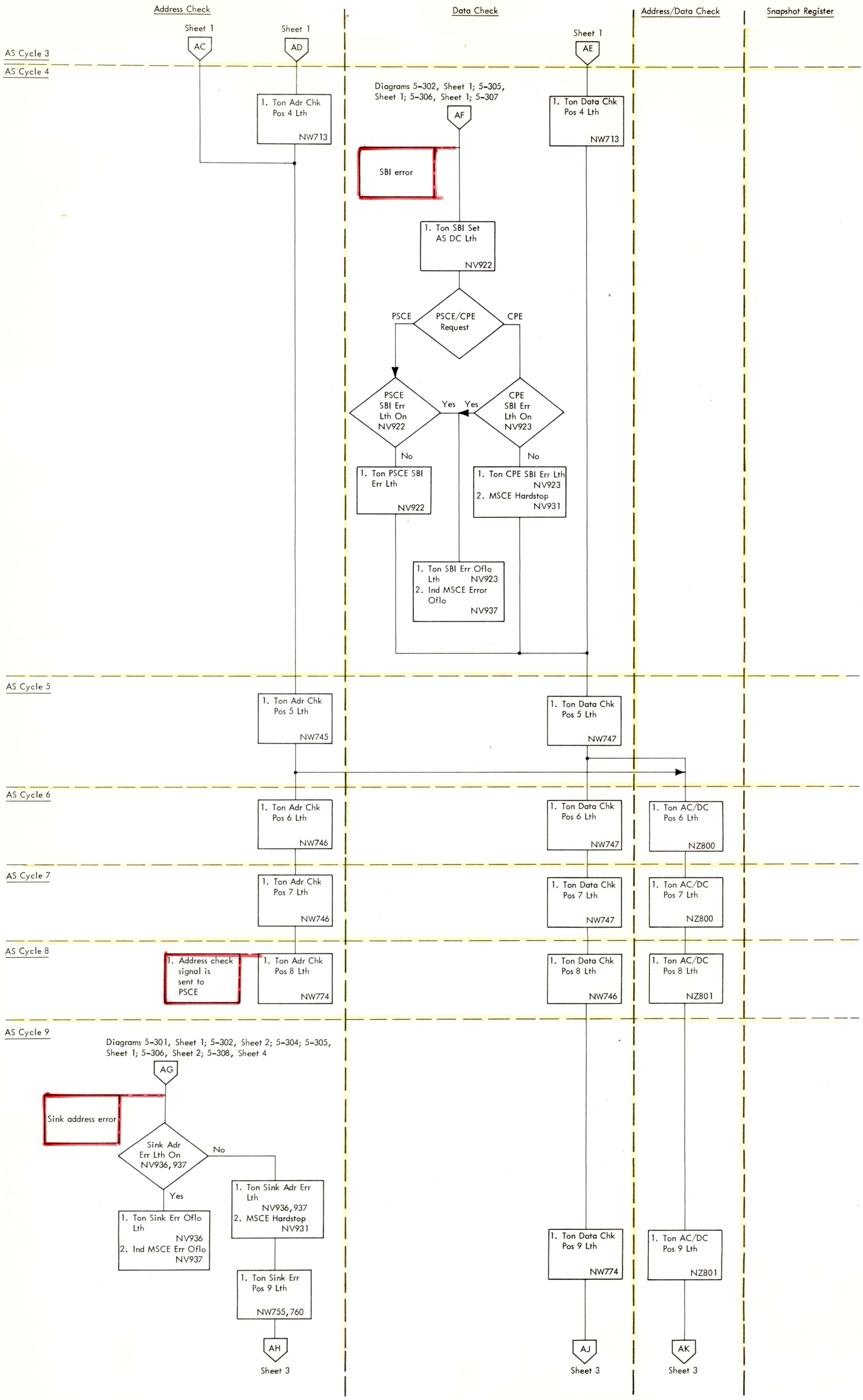


DIAGRAM 5-309. ADDRESS CHECK AND DATA CHECK (SHEET 2 OF 3)

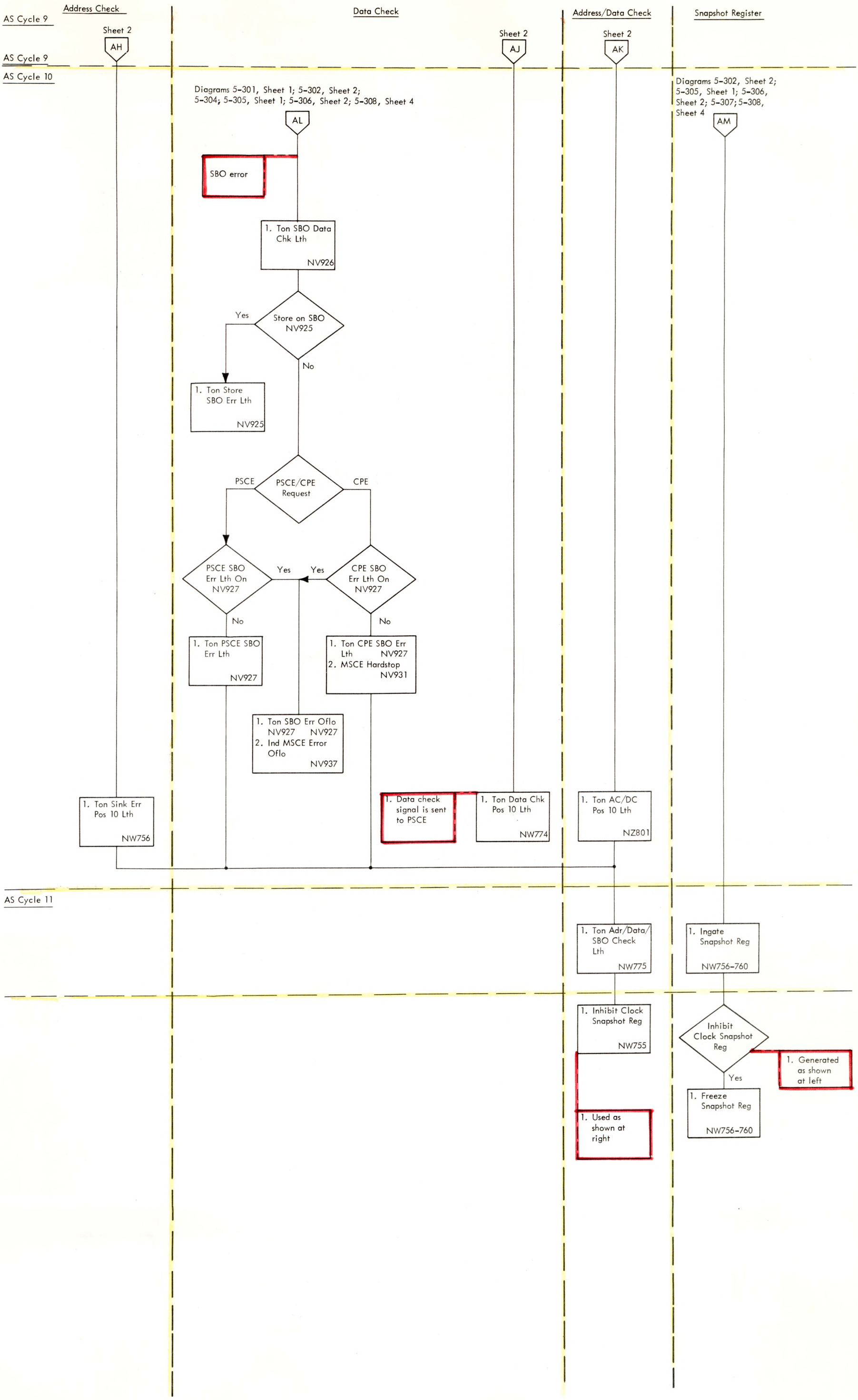


DIAGRAM 5-309. ADDRESS CHECK AND DATA CHECK (SHEET 3 OF 3)

Objectives:

1. Pass CPE request address information through the backup buffer and set into the request buffer.
2. Hold the request in the backup buffer if the request buffer is full; move the current request into the request buffer as the earlier request is loaded into a Q Register
3. Request use of the CPE address Bus from input priority. (The CPE request Tgr enters the request into input priority).
4. Re-enter the request in input priority each succeeding cycle if the priority decoder does not respond to the input request.
5. Prepare to load the request in the Q (via the CPE address bus) when a response is received from input priority.

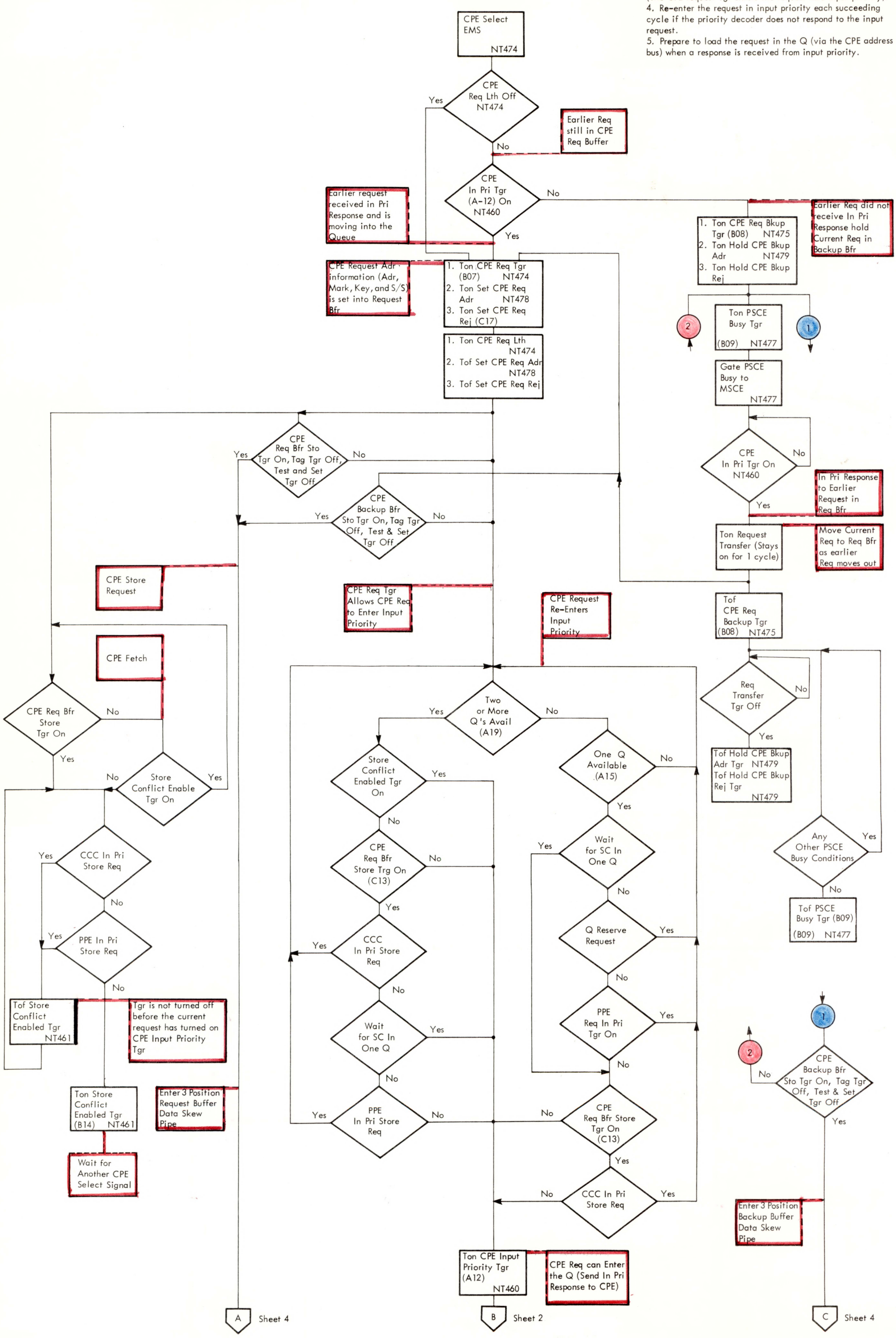
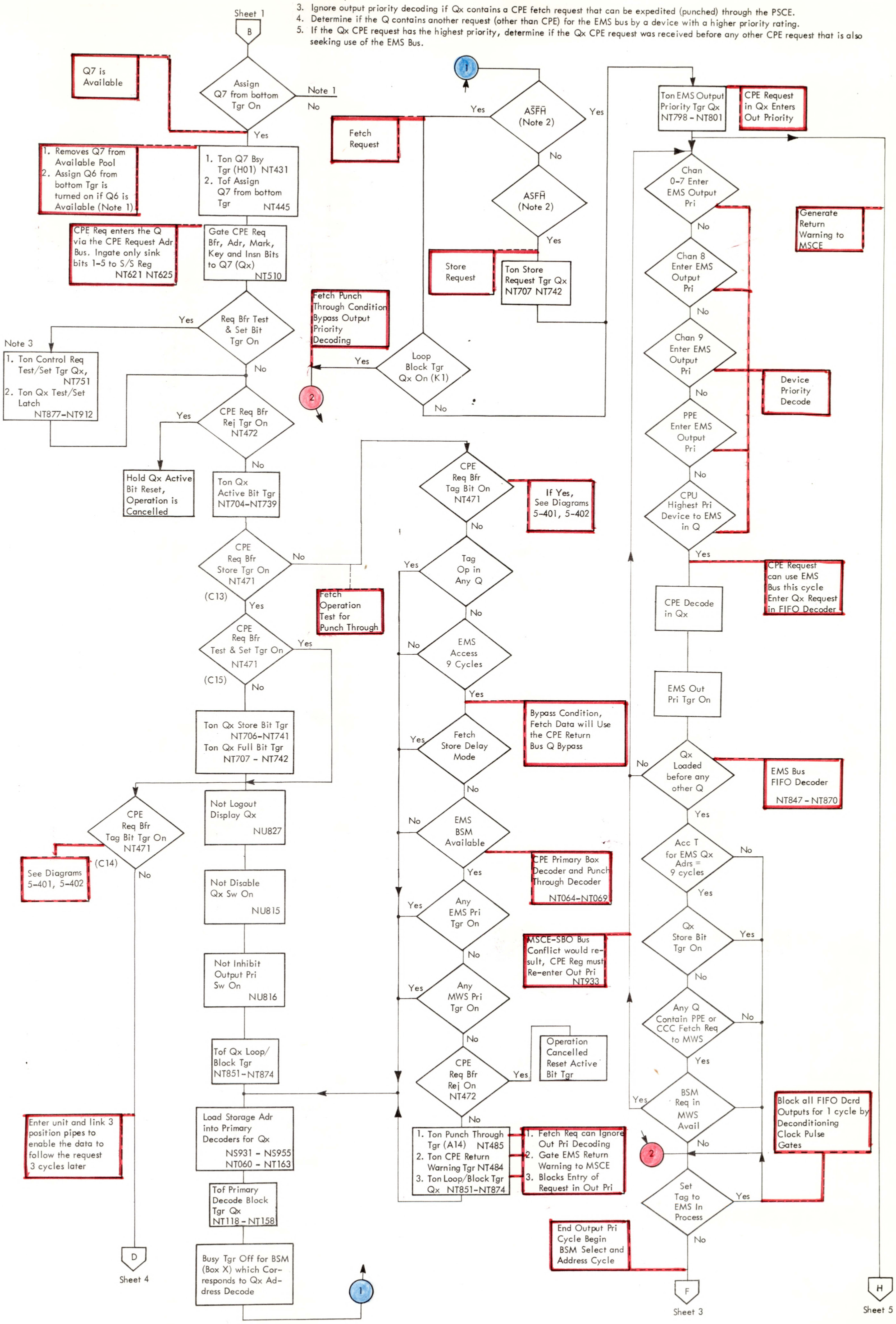


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 1 OF 12)

Output Priority Cycle

Objectives:

1. Load the request address information in the highest numbered available Q register.
2. Turn on the assigned Q (Qx) active bit to indicate that Qx contains a pending request; turn on the store and full bits if Qx contains a CPE store request.
3. Ignore output priority decoding if Qx contains a CPE fetch request that can be expedited (punched) through the PSCE.
4. Determine if the Q contains another request (other than CPE) for the EMS bus by a device with a higher priority rating.
5. If the Qx CPE request has the highest priority, determine if the Qx CPE request was received before any other CPE request that is also seeking use of the EMS Bus.



Notes:

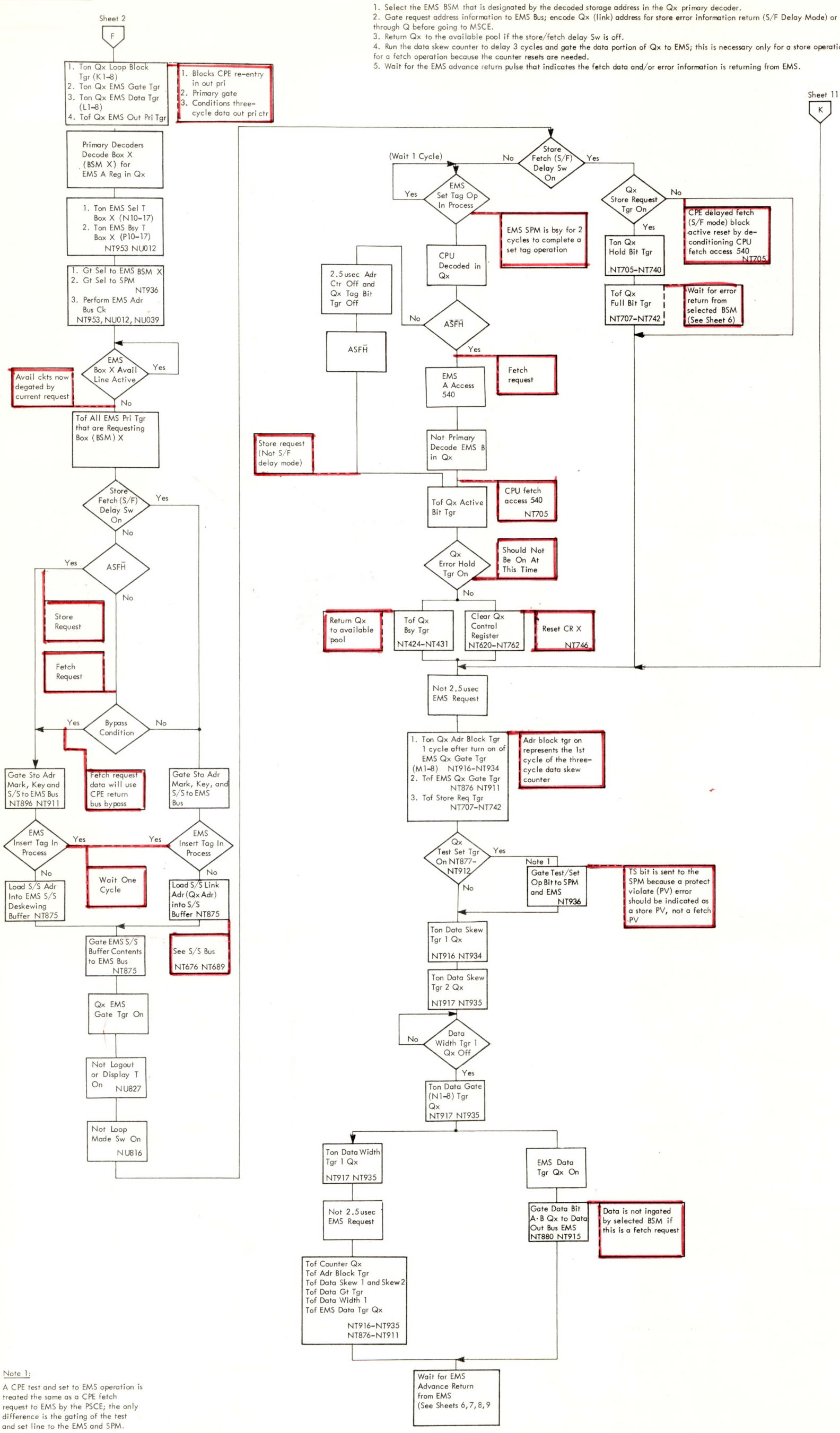
1. All CPE requests are assigned Q's searching from the bottom up (Q7 through Q0). Any Q that is not disabled, not reserved, and not busy is available. If Q7 is available, its assign from bottom Tgr is on Refer to Sheet 12.
2. Each Queue (Q) contains four control bits: A = Active, S = Store, F = Full, H = Hold. On and Off combinations of these bits determine the type and state of a request in the Q. For example: Active On, Store On, Full On, and Hold Off (ASFH) represents a store request, before the request is sent to storage.
3. (See Note 1 on Sheet 3).

DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 2 OF 12)

Select and Address Cycle

Objectives:

1. Select the EMS BSM that is designated by the decoded storage address in the Qx primary decoder.
2. Gate request address information to EMS Bus; encode Qx (link) address for store error information return (S/F Delay Mode) or if fetch data will pass through Q before going to MSCE.
3. Return Qx to the available pool if the store/fetch delay Sw is off.
4. Run the data skew counter to delay 3 cycles and gate the data portion of Qx to EMS; this is necessary only for a store operation, but is not blocked for a fetch operation because the counter resets are needed.
5. Wait for the EMS advance return pulse that indicates the fetch data and/or error information is returning from EMS.



Note 1:

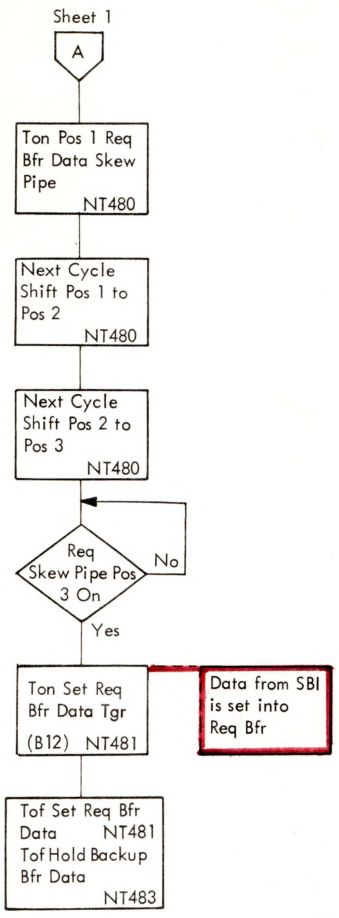
A CPE test and set to EMS operation is treated the same as a CPE fetch request to EMS by the PSCE; the only difference is the gating of the test and set line to the EMS and SPM.

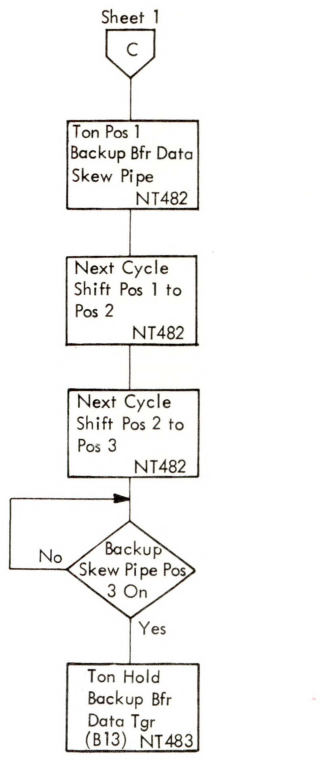
DIAGRAM 5-400.CPE STORE/FETCH REQUEST TO EMS (SHEET 3 OF 12)

CPE Request and Backup Buffer

3 Cycle Data Skew Pipes

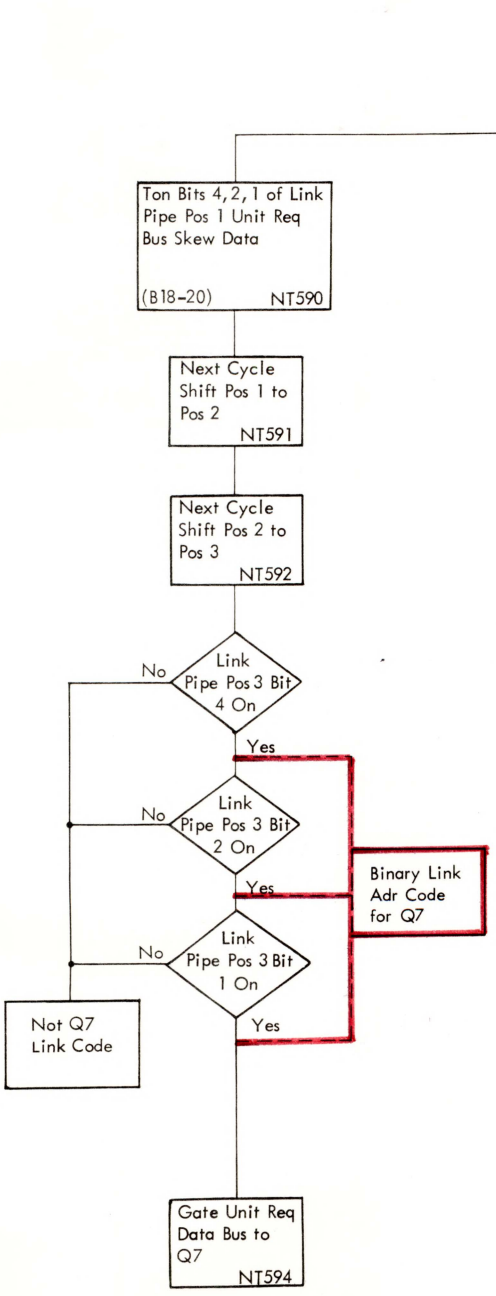
Objectives:
1. Set CPE store request data, from the system SBI or CPE backup buffer, into the CPE request buffer 3 cycles after the request address information is set in the buffer.
2. Hold the CPE store request data in the CPE backup buffer, 3 cycles after the request information arrives, only if the request buffer was full when the request arrived.





CPE Store Request Unit and Link 3 Cycle Pipes

Objectives:
1. Encode the designated Q link address (determined by "Assign Qx from bottom" tgr and designated unit code as CPE store request information enters Qx.
2. Enter the unit and link codes in their respective pipes.
3. After a 3-cycle delay:
a. Gate store data from the CPE request buffer (as determined by the unit pipe) to the unit request bus.
b. Gate the unit request bus to Qx (Q7 for this example, as determined by the link pipe).



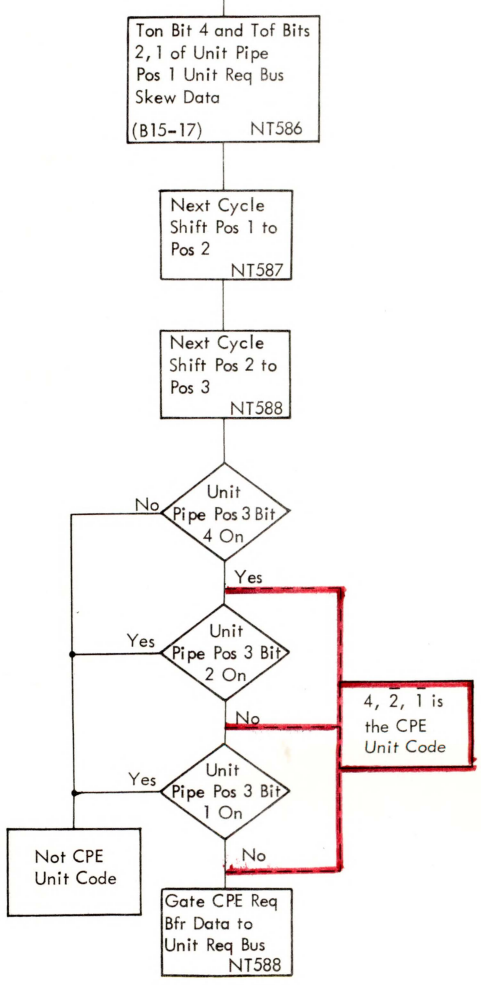


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 4 OF 12)

Fetch Request 9 Cycle Access Return Warning Generation

Objectives:

1. Determine if the Qx CPE fetch req was received before any CPE req in any other Q reg.
2. Send a return warning signal to the MSCE during the output priority cycle if EMS is a 9 cycle access storage and the PSCE CE panel S/F delay switch is off.
3. If the S/F delay mode Sw is on, start the 7 position CPE Q return pipe; send the EMS return warning after a 2 cycle delay.

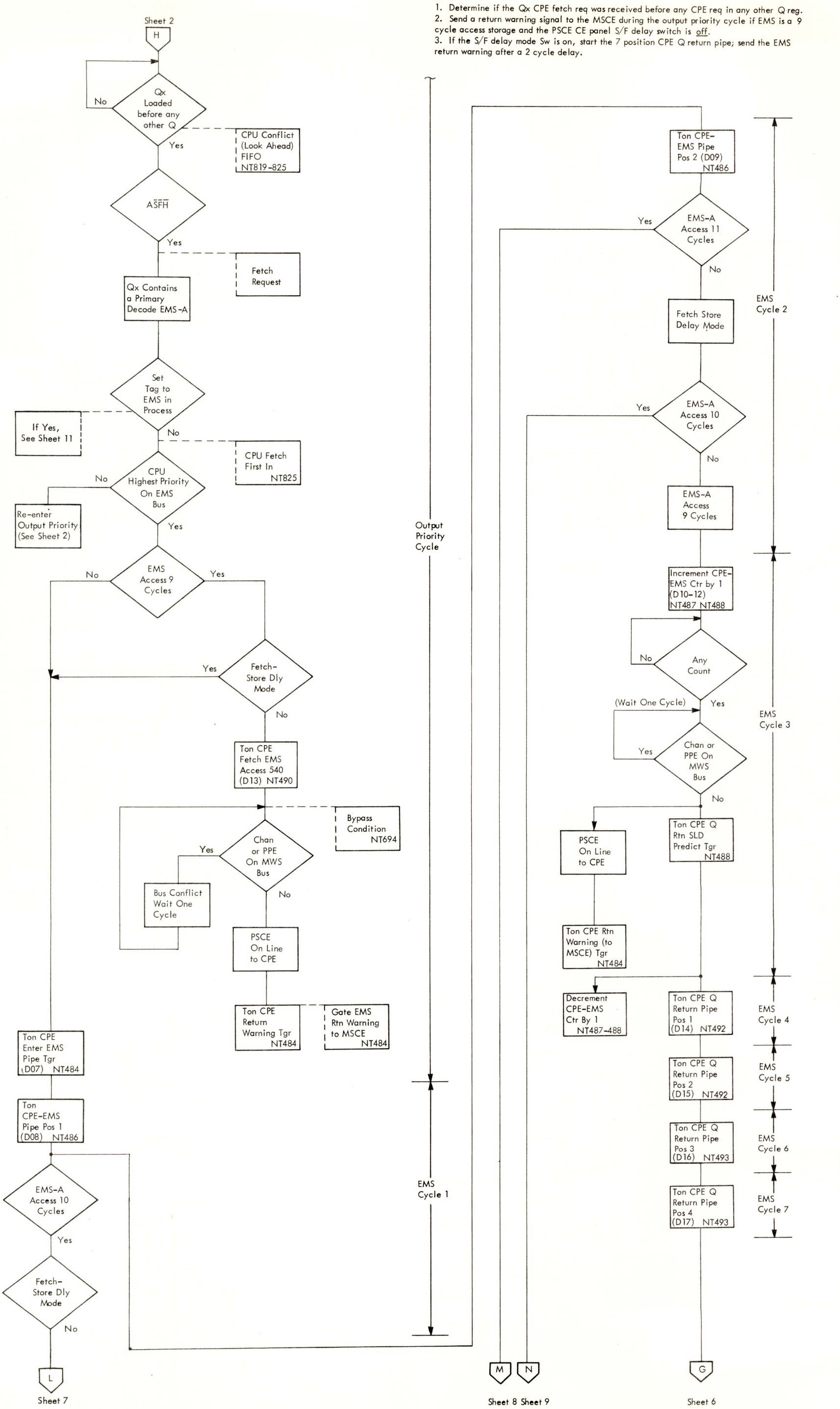


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 5 OF 12)

EMS Advance Return
9 Cycle Access

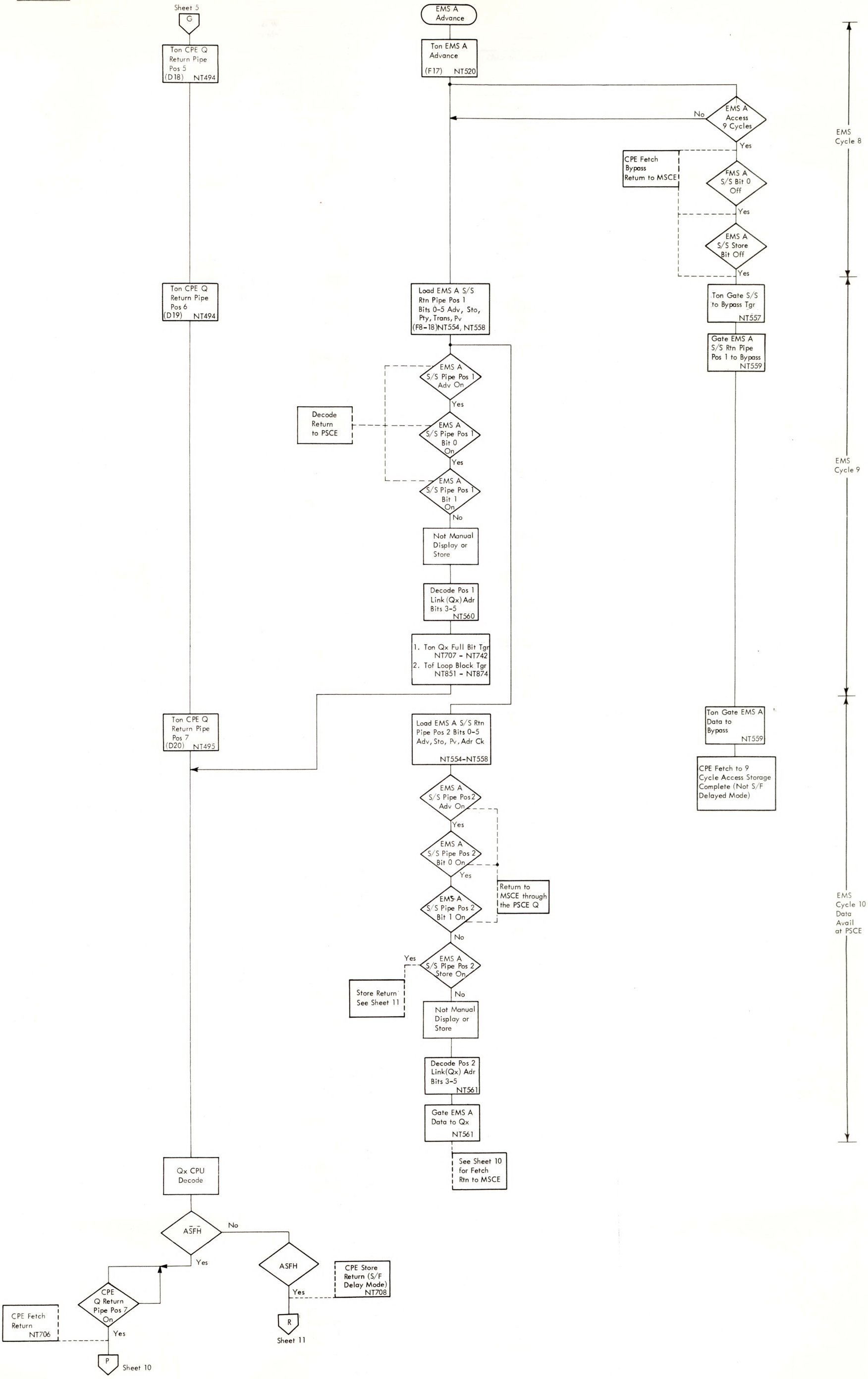


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 6 OF 12)

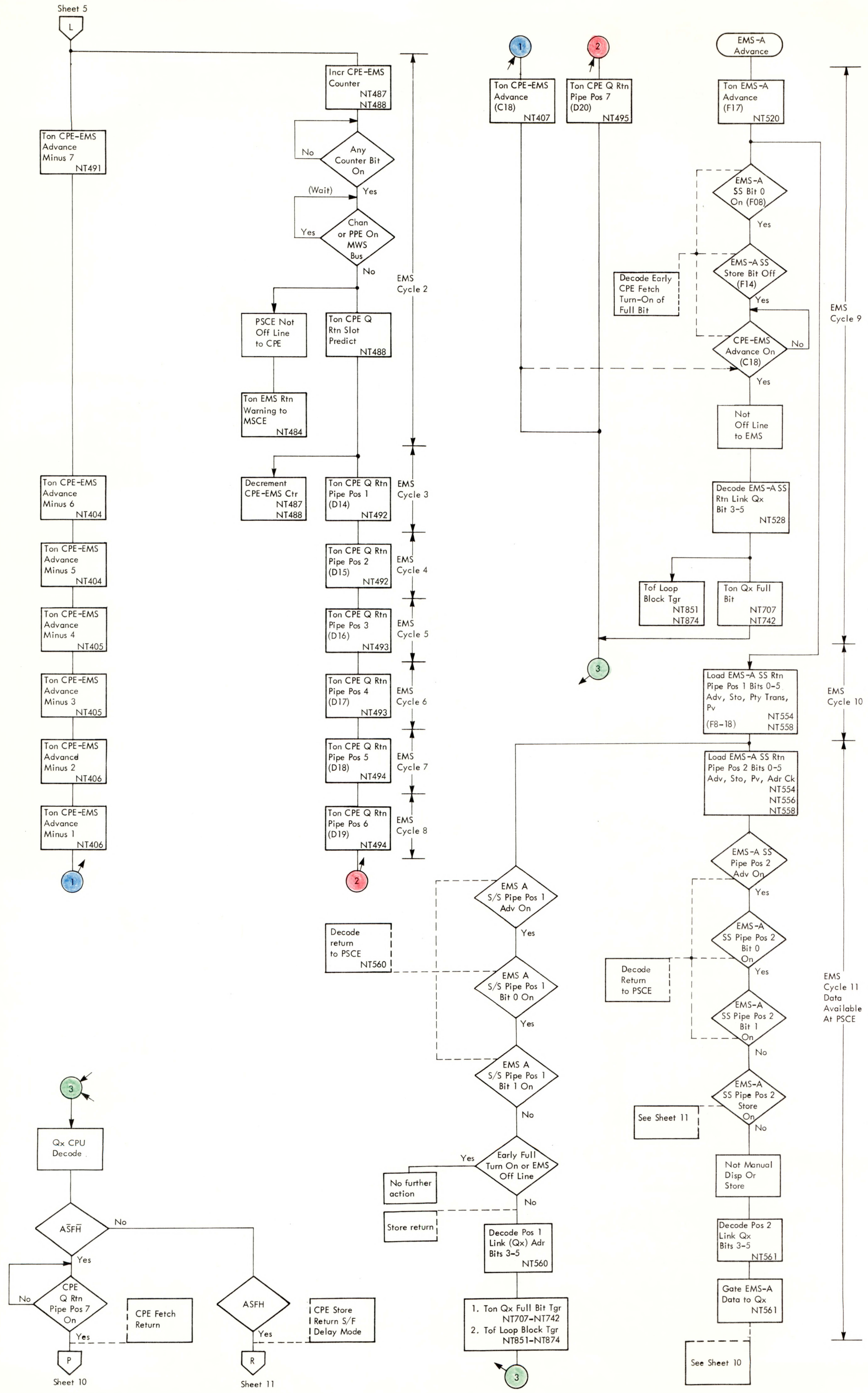


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 7 OF 12)

EMS Advance Return,
11 Cycle Access (In or Out of S/F Delay Mode)

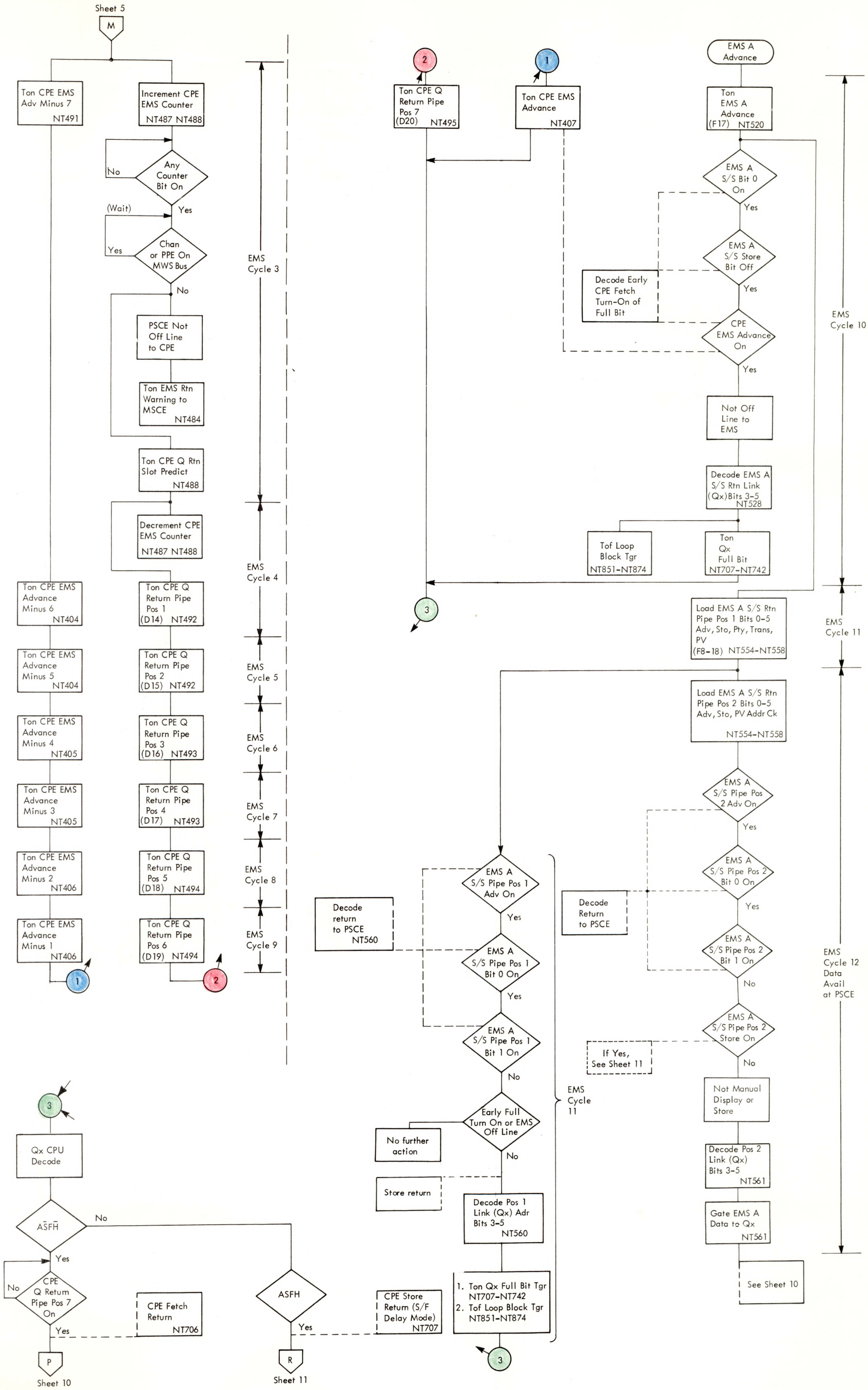


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 8 OF 12)

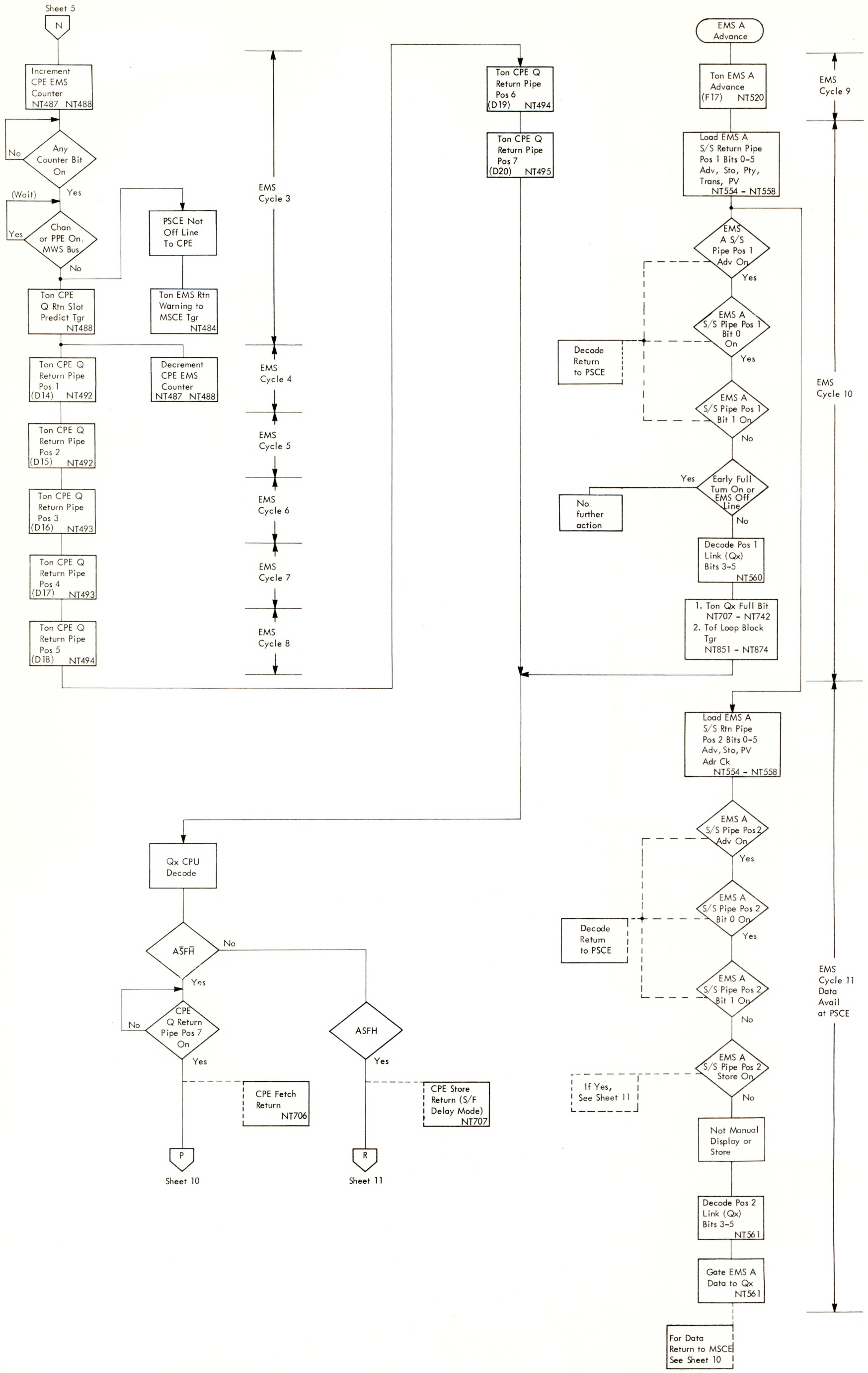
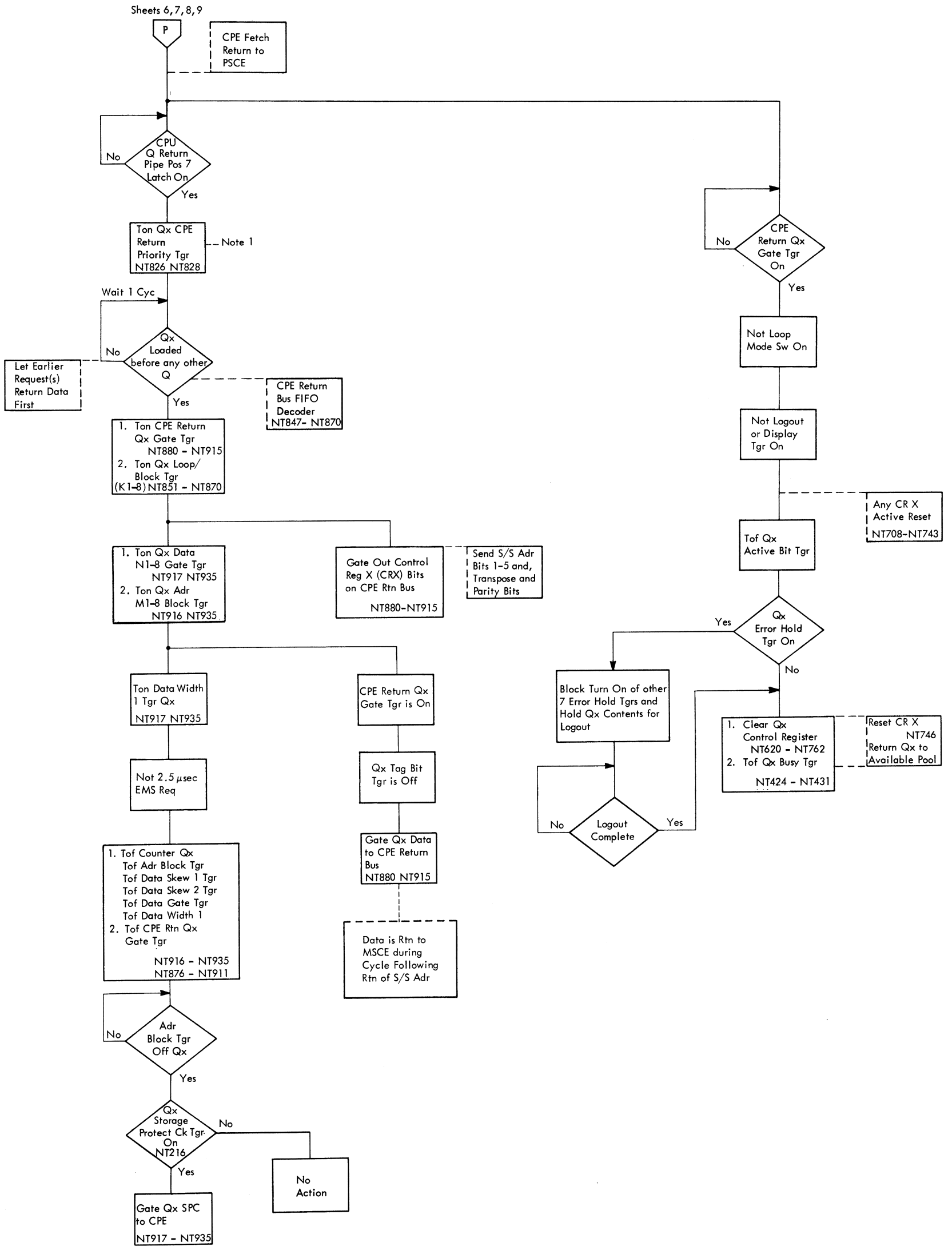


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 9 OF 12)

CPE Delayed Fetch Return to MSCE

Objectives:

1. Determine if CPE request in Qx was loaded into Qx before any other CPE request in another Q register (first-in first out decoder).
2. Send the CPE request source/sink (S/S) address to the MSCE sink decoder to coincide with the EMS return bit "dropping out" of the MSCE accept stack position 8.
3. Gate the fetch data to the CPE return bus one cycle after the S/S address; data is forwarded to the CPE via the SBO in MSCE during the time "slot" reserved by the EMS return bit leaving in the accept stack.
4. Clear the Qx outgate and control triggers and return Qx to the available pool.



Note 1
There is no need to enter the device decoder because no other device can use the CPE return bus to MSCE; a MSCE SBO conflict was considered before the return warning was sent.

DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 10 OF 12)

CPE Delayed Store (Reset Active)

Objectives:
1. Enter CPE store return (error information) in output priority for unit return bus; the request is represented by the Qx hold bit. (Information gated to the unit return bus is not ingated by any device, the sequence is performed to reset the Qx active condition.)
2. Determine if CPE request in Qx was loaded before any other CPE request in another Q register (FIFO Decoder).
3. Clear the Qx control register and return conditions were returned by the storage unit.
4. Run the 3 cycle data skew counter to generate ending resets.

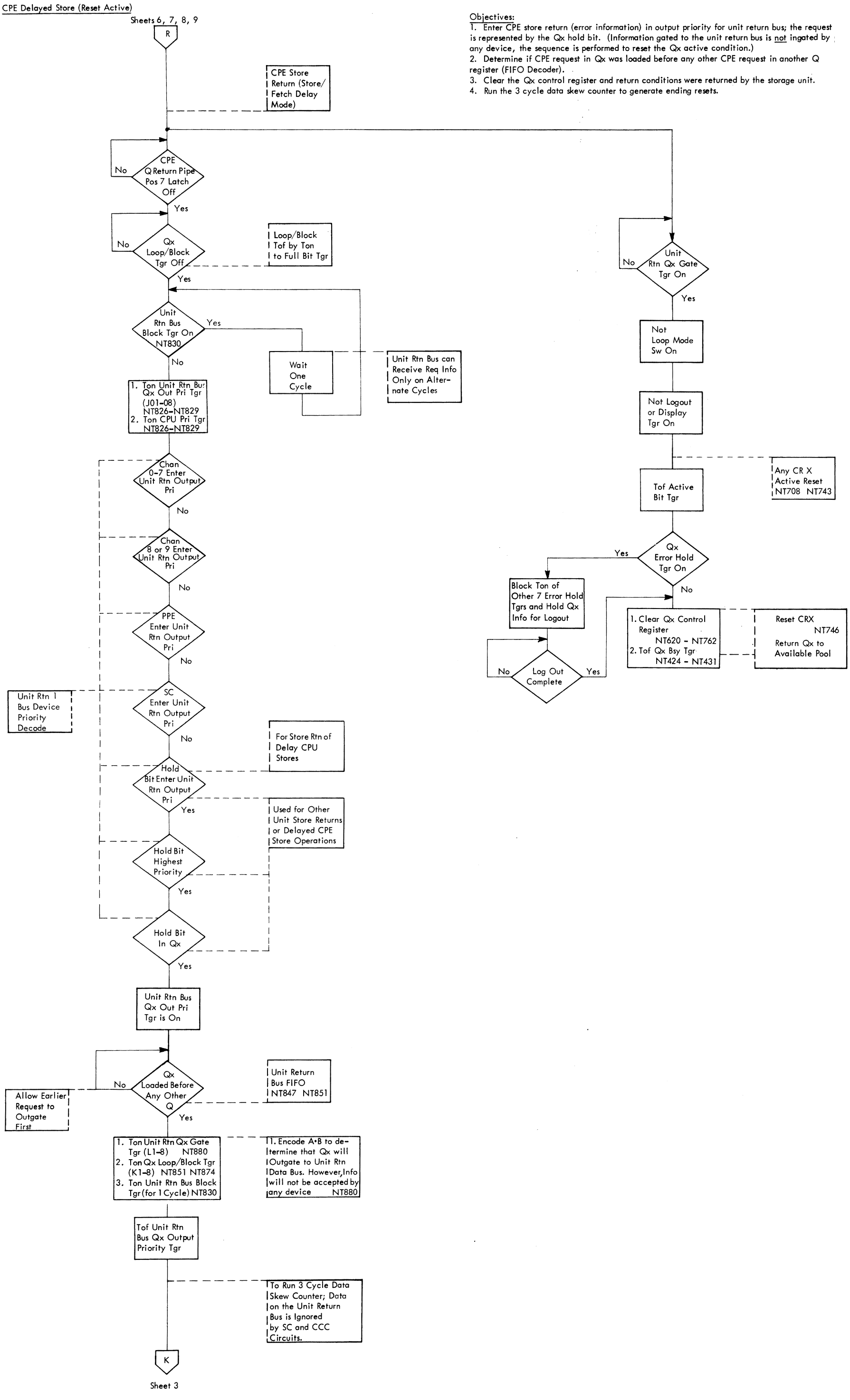
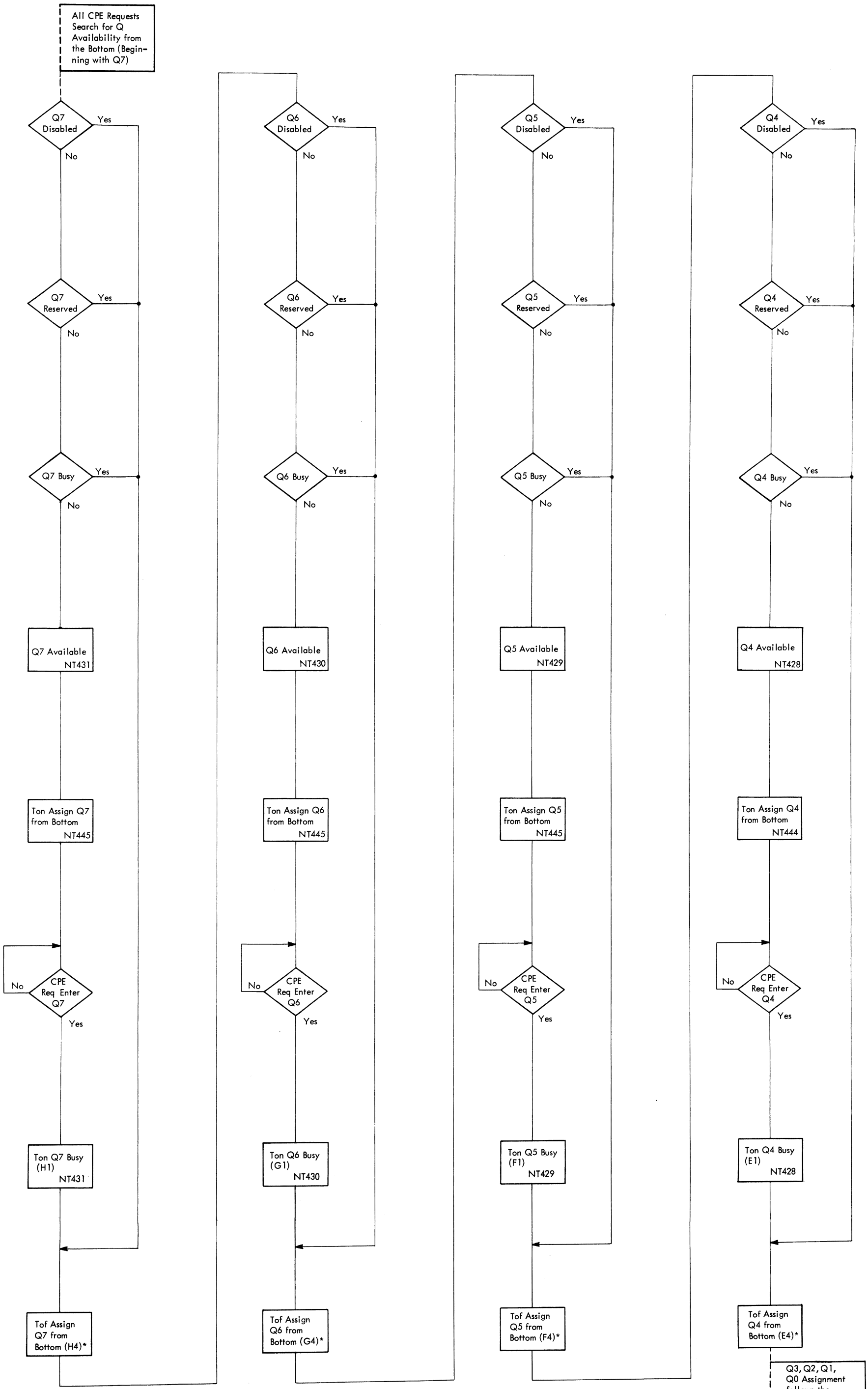


DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 11 OF 12)



* Refer to display - select switch at W42 on CE panel to modify these lamps for use as "bottom" indicators.

DIAGRAM 5-400. CPE STORE/FETCH REQUEST TO EMS (SHEET 12 OF 12)

CPE Select Signal and Input Priority

Objectives:

1. Pass CPE insert tag request address information through the backup buffer and set into the request buffer.
2. Hold the request in the backup buffer if the request buffer is full; move the current request into the request buffer as the eqrlier request is loaded into the Q.
3. Request use of the CPE address bus from input priority. (The CPE request trigger enters the request into input priority.)
4. Re-enter the request in input priority during the next cycle if the priority decoder did not respond to the input request.
5. Prepare to load the request in the Q when a response is received from input priority.

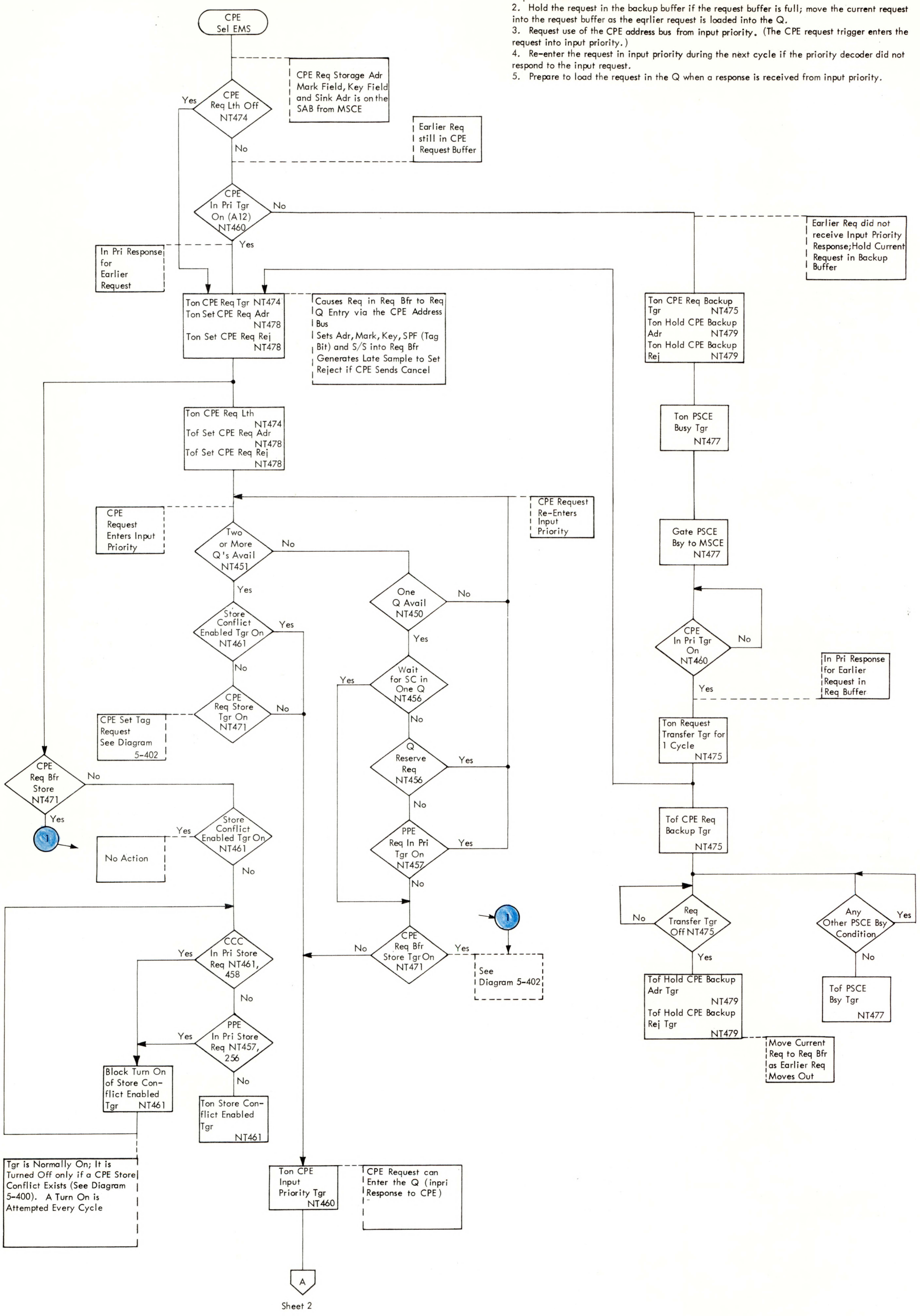
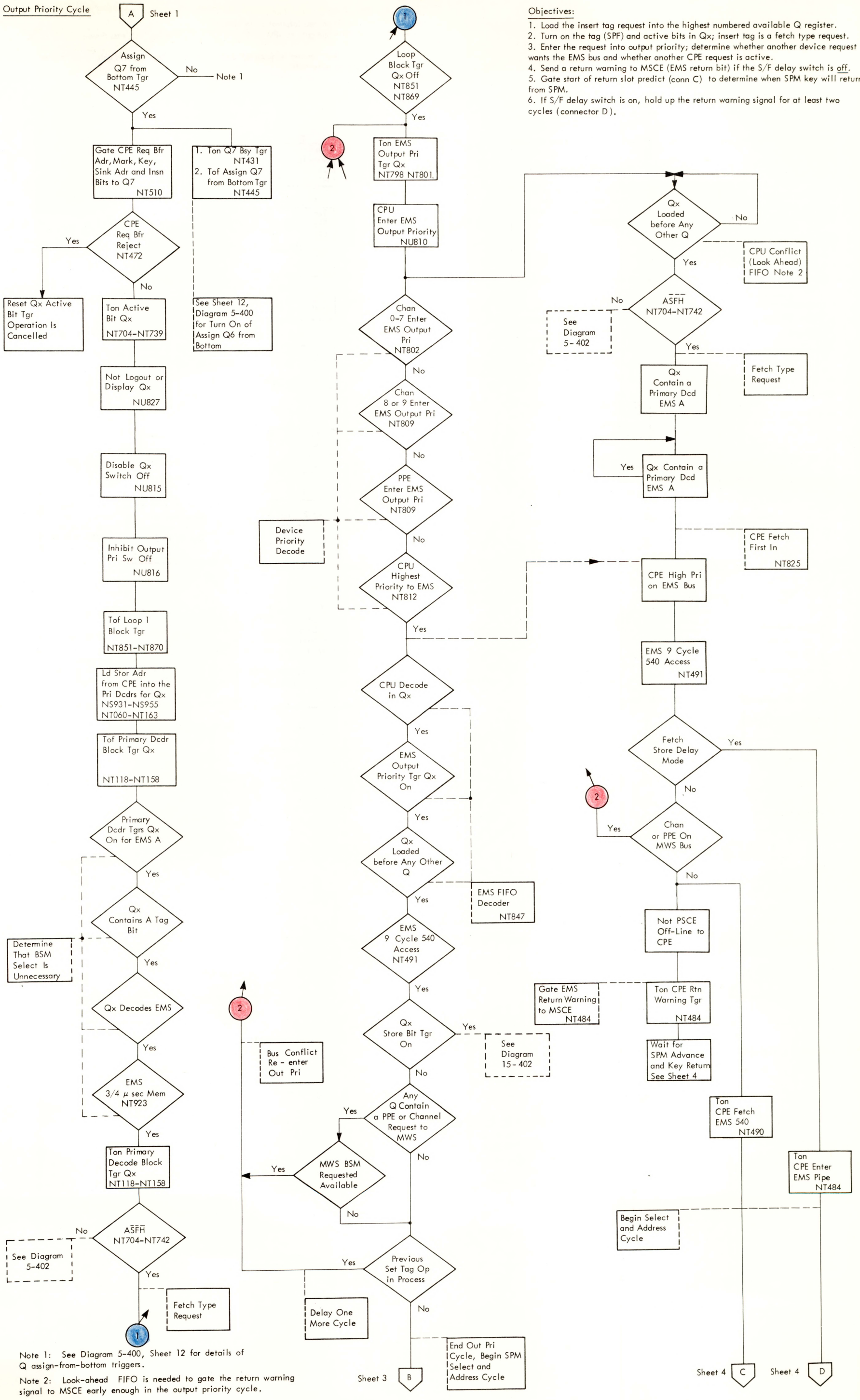


DIAGRAM 5-401. CPE INSERT KEY (TAG) REQUEST TO EMS (SHEET 1 OF 5)

Output Priority Cycle



Objectives:

1. Load the insert tag request into the highest numbered available Q register.
2. Turn on the tag (SPF) and active bits in Qx; insert tag is a fetch type request.
3. Enter the request into output priority; determine whether another device request wants the EMS bus and whether another CPE request is active.
4. Send a return warning to MSCE (EMS return bit) if the S/F delay switch is off.
5. Gate start of return slot predict (conn C) to determine when SPM key will return from SPM.
6. If S/F delay switch is on, hold up the return warning signal for at least two cycles (connector D).

DIAGRAM 5-401. CPE INSERT KEY (TAG) REQUEST TO EMS (SHEET 2 OF 5)

Select and Address Cycle

Objectives:
1. Send a select to the SPM only (not EMS).
2. Gate insert key request address information to SPM.
3. Encode Qx link address and gate to SPM in the S/S field; the SPM key will pass through the Q on its way to the MSCE.
4. Run three-cycle data skew counter (sequencer) to generate resets (the outgated data is not ingated by EMS because the EMS is not selected).
5. Wait for SPM advance and key return.

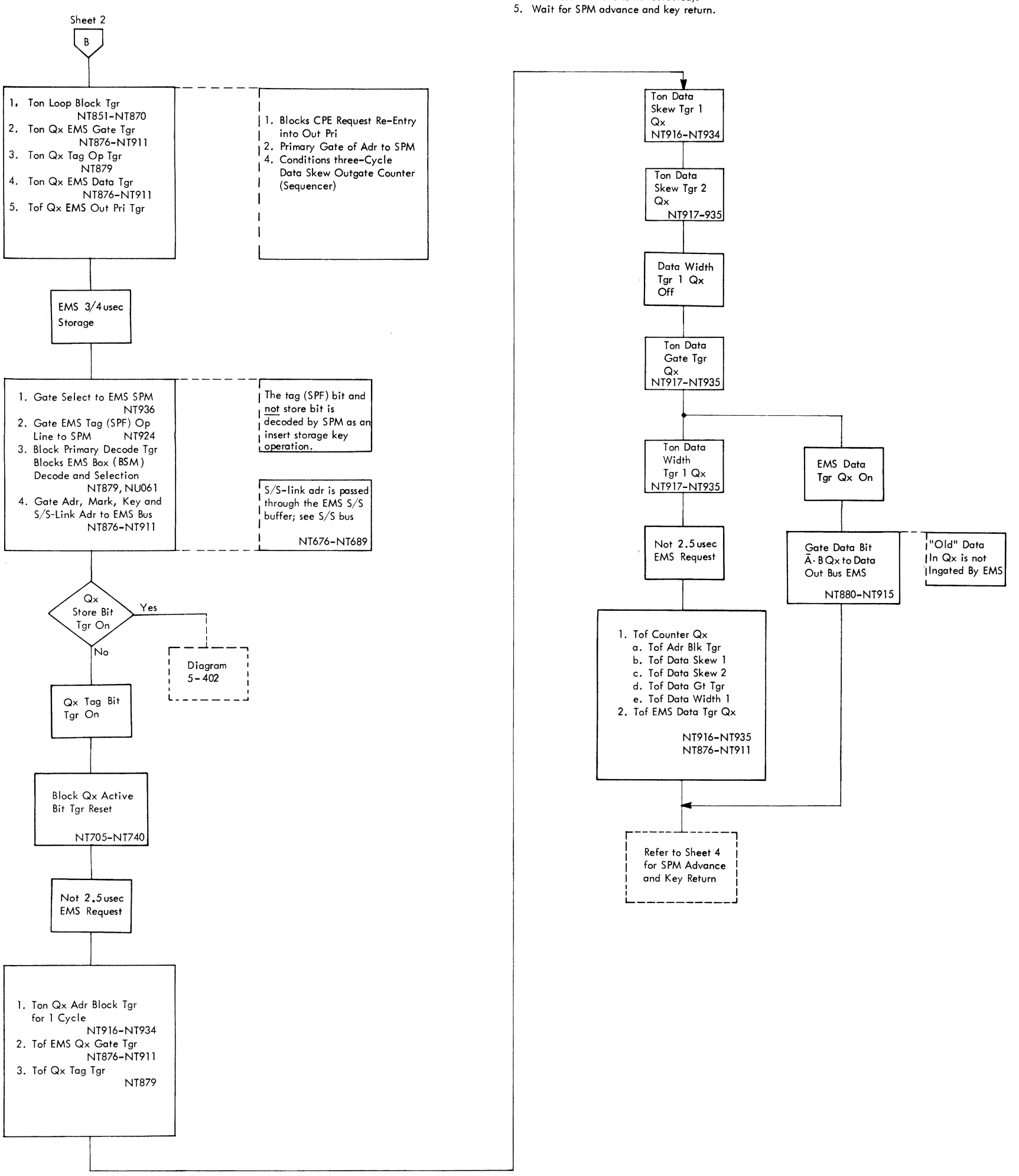
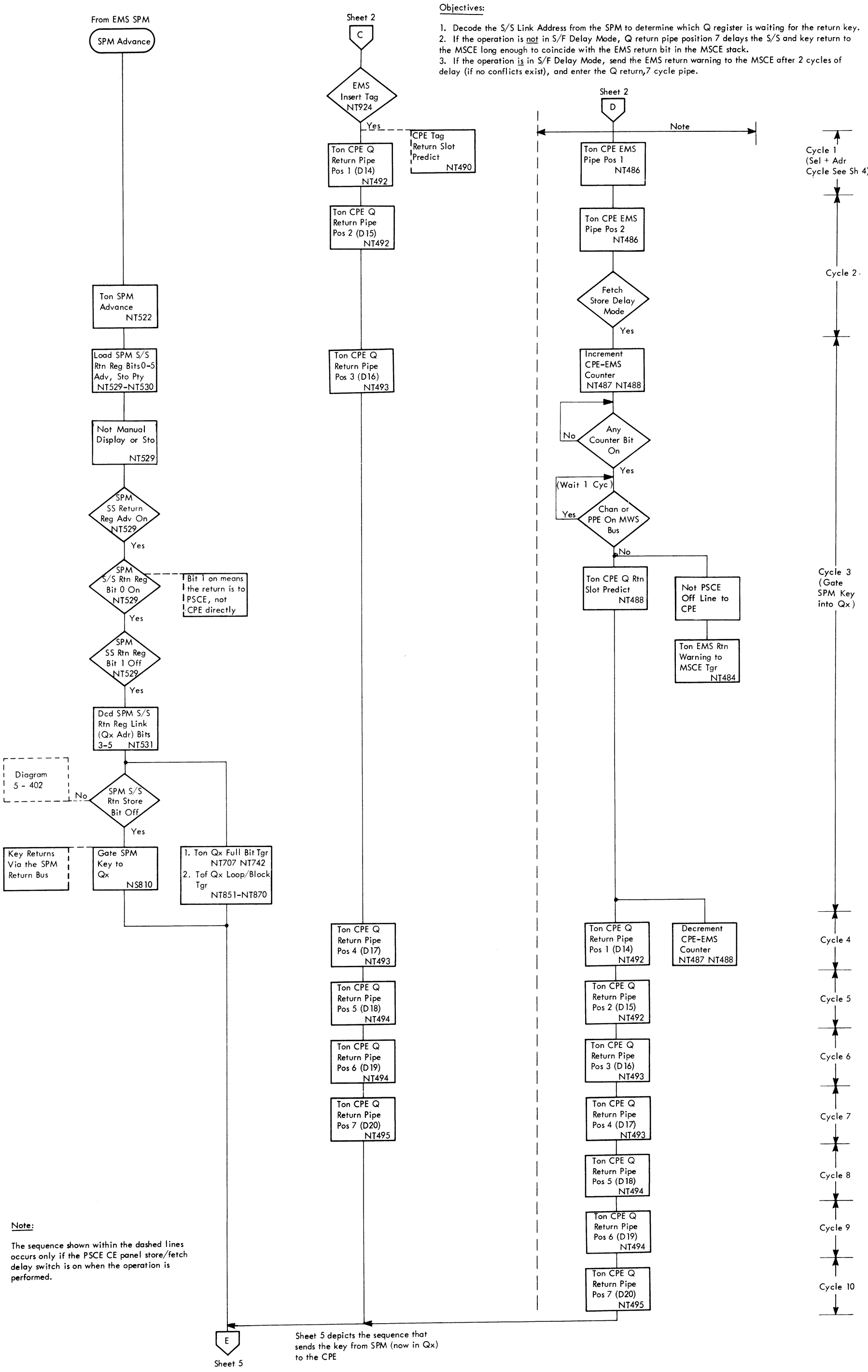


DIAGRAM 5-401. CPE INSERT KEY (TAG) REQUEST TO EMS (SHEET 3 OF 5)

Insert Key (Fetch) Return to the PSCE

Objectives:

1. Decode the S/S Link Address from the SPM to determine which Q register is waiting for the return key.
2. If the operation is not in S/F Delay Mode, Q return pipe position 7 delays the S/S and key return to the MSCE long enough to coincide with the EMS return bit in the MSCE stack.
3. If the operation is in S/F Delay Mode, send the EMS return warning to the MSCE after 2 cycles of delay (if no conflicts exist), and enter the Q return,7 cycle pipe.



Note:

The sequence shown within the dashed lines occurs only if the PSCE CE panel store/fetch delay switch is on when the operation is performed.

DIAGRAM 5-401. CPE INSERT KEY (TAG) REQUEST TO EMS (SHEET 4 OF 5)

Insert Key Return to the MSCE

Objectives:

1. When Q return pipe position 7 is on, enter the Qx CPE insert tag request into FIFO decoder to determine whether it is the "oldest" CPE request in the Queue.
2. Send the S/S address to the MSCE.
3. After 1 cycle, gate the key to CPE via the SBO in MSCE in the time "slot" reserved by the EMS return bit in the MSCE accept stack.
4. Clear the Qx control register if no errors are present (in S/F delay mode) and return Qx to the available pool.

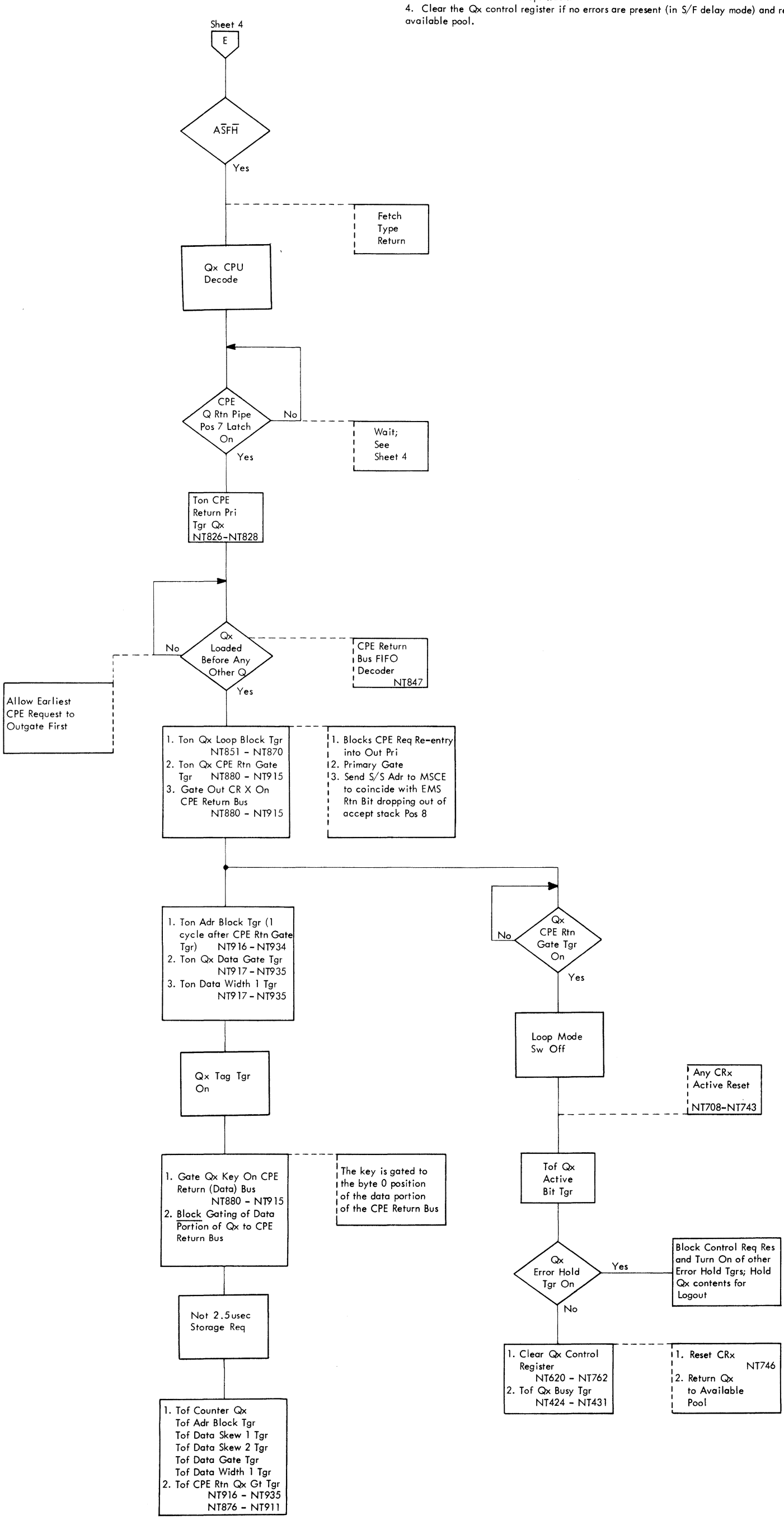
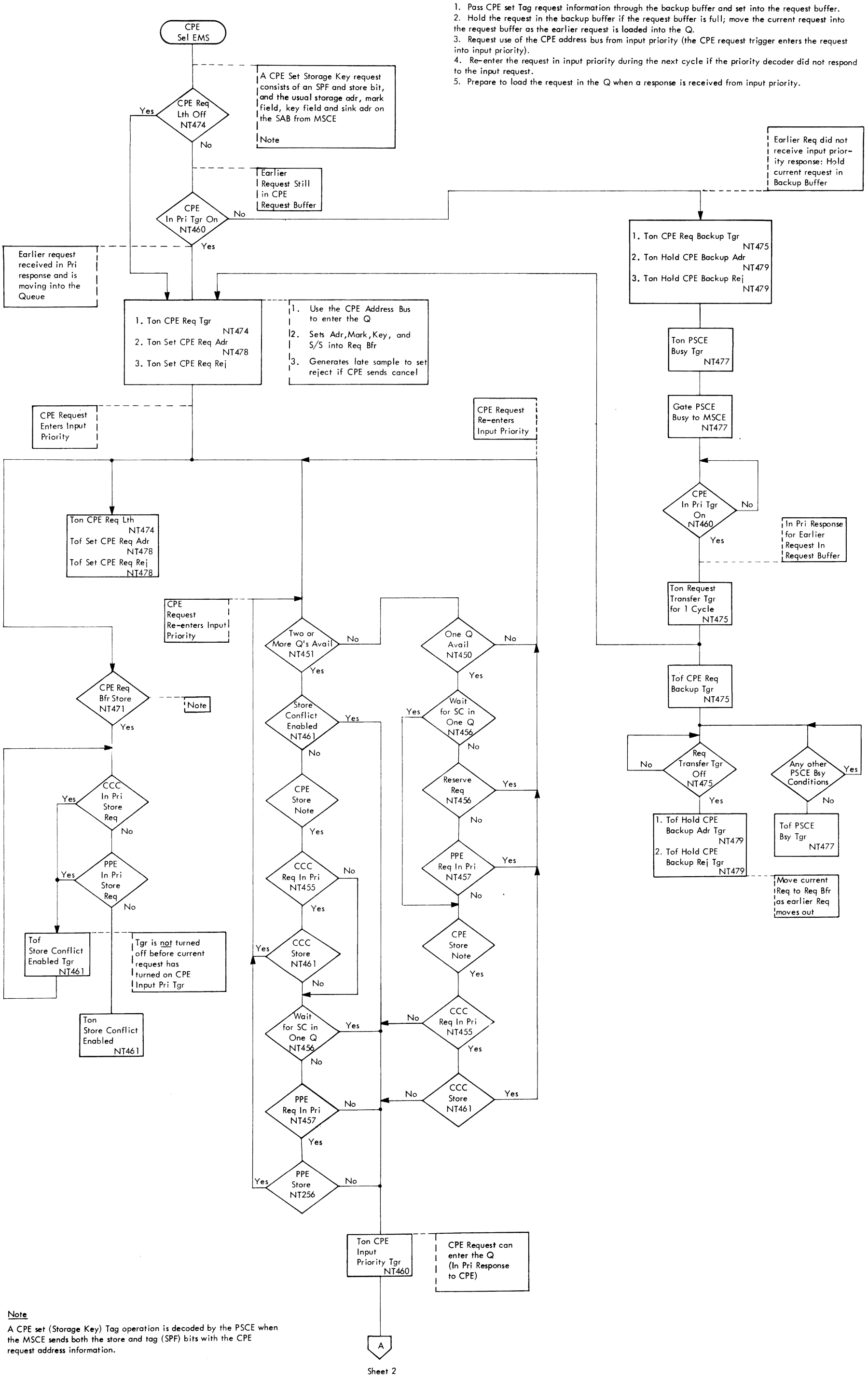


DIAGRAM 5-401. CPE INSERT KEY (TAG) REQUEST TO EMS (SHEET 5 OF 5)

CPE Select Signal and Input Priority

Objectives:

1. Pass CPE set Tag request information through the backup buffer and set into the request buffer.
2. Hold the request in the backup buffer if the request buffer is full; move the current request into the request buffer as the earlier request is loaded into the Q.
3. Request use of the CPE address bus from input priority (the CPE request trigger enters the request into input priority).
4. Re-enter the request in input priority during the next cycle if the priority decoder did not respond to the input request.
5. Prepare to load the request in the Q when a response is received from input priority.



Sheet 2

Note

A CPE set (Storage Key) Tag operation is decoded by the PSCE when the MSCE sends both the store and tag (SPF) bits with the CPE request address information.

DIAGRAM 5-402. CPE SET KEY (TAG) REQUEST TO EMS (SHEET 1 OF 3)

Sheet 1

Input Priority Cycle
Output Priority Cycle

A

Assign Q7 from Bottom Tgr NT445

No — Note

Yes

S/S Bits are Loaded into S/S Register NT620 NT655

Gate CPE Req Bfr Adr, Mark, Key, Sink Adr and Inst Bits to Q7 NT510

1. Ton Q7 Busy (H01) NT431
2. Tof Assign Q7 from Bottom Tgr NT445

See Sheet 12, Diagram 5-400 or turn on of Assign Q6 from Bottom

CPE Req Bfr Reject NT472

Yes

No

Reset Qx Active Bit Tgr Operation is Cancelled

Ton Active Bit Qx NT704 NT739

CPE Req Bfr Store Tgr On NT471

Should be on for a Set Tag Operation

Yes

CPE Req Bfr Test & Set Tgr On NT471

No

1. Ton Sto Bit Tgr Qx NT706 - NT741
2. Ton Full Bit Tgr Qx NT707 - NT742

Not Logout or Display Qx NU827

Disable Qx Switch Off NU815

Inhibit Output Pri Sw Off NU816

Tof Loop/ Block Tgr NT851 - NT870

Load Storage Adr from CPE into the Pri Dcdr for Qx NS931 - NS955 NT060 - NT163

Tof Primary Decode Block Tgr Qx NT118 NT158

Primary Dec Tgrs Qx on for EMS A

Yes

Qx Contain A Tag Bit

Determing That BSM Select is Unnecessary

Yes

SPF Bit from MSCE

Qx Decode EMS

Yes

1

1

EMS 3/4 μsec MEM NT923

Ton Primary Decode Block Tgr Qx NT118 - NT158

Yes

See Diagram 5-401

$A\bar{S}\bar{F}\bar{H}$ NT704 NT742

No

$AS\bar{F}\bar{H}$ NT704 NT742

Yes

Store Type Request

Ton Qx Store Request Tgr NT707-NT742

Loop Block Tgr Qx Off NT851 NT869

CPE Set Tag Request In Qx Enters Output Priority

Ton Qx EMS Output Pri Tgr Qx NT798-NT801

CPU Enter EMS Output Pri NT810

Yes

Chan 0-7 Enter EMS Output Pri NT802

No

Chan 8 or 9 Enter Output Pri NT809

No

PPE Enter EMS Output Pri NT809

Device Priority Decode

No

CPU Highest Priority to EMS NT812

Yes

CPU Decode in Qx

Yes

EMS Output Pri Tgr Qx On

Yes

Qx Loaded Before Any Other Q

No

EMS Bus FIFO Decoder NT847 NT870

Yes

1. Blocks CPE Request Re-entry into Out Pri
3. Primary Gate for Adr to SPM

1. Ton Qx Loop/Block Tgr NT851 NT911
2. Tof EMS Output Priority Tgr NT798 NT801
3. Ton Qx EMS Gate Tgr NT876 NT801
4. Ton Qx Tag Op Tgr NT879
5. Ton Qx EMS Data Tgr NT876 NT911

Not EMS 3/4usec Storage NT923

1. Gate Select to the EMS SPM NT936
2. Gate EMS Tag Op Line to SPM (SPF Line) NT924
3. Block EMS Box (BSM) Decode and selection (using Tag Op Tgr) NT899 NU061
4. Gate Adr Mark, Key and Source/ Sink Adr to EMS Bus NT876 - NT911

Run 3 cycle data skew counter, but EMS is not selected and will not ingate

The SPF and Store Bits are used by SPM to determine this is a Set Storage Key Operation

C

Sheet 3

2

Note: Refer to Diagram 5-400, Sheet 3 for details of Q assign from bottom triggers

Objectives:

1. Load the set tag request into the highest numbered available Q Reg.
2. Turn on the tag (SPF), store, active, and full bits in Qx.
3. Enter the request in to output priority; determine whether another device request wants the EMS Bus and whether another CPE request is active.
4. Select the SPM only (not EMS) and gate out address information; encode the Qx link address if error info will return to Qx.
5. Turn on the Qx hold bit if errors will return to Qx.
6. Block output priority 1 cycle for all other requests because SPM for entire EMS will be busy for a total of 2 cycles.
7. Reset the active bit and the rest of the control register if errors will not return to the Q (not S/F delay mode).

Sheet 3

B

2

Store Fetch Delay Sw On NU816

No

Yes

Previous Set Tag In Process NT924

Yes

No

Gate S/S Buffer Contents to EMS NT875

Store Request Tgr On

Yes

Should be on for Set Tag Op

Hold Bit On Prevents Reset of the Qx Active Bit Tgr

1. Ton Qx Hold Bit Tgr NT705 - NT740
2. Tof Qx Full Bit Tgr NT707 - NT740

Gate S/S Bfr Contents to EMS NT685

Encode Qx Link Adr & Gate Into S/S Buffer NT685

Qx Tag Bit and Store Bit Tgrs On

EMS 3/4 μsec Storage NT923

Block Output Priority Decision for Other Ops (during Tag Adr Cyc) by deconditioning clock to FIFO Decoders NT851 NT869

Set Tag Operation requires 2 cycles to complete; entire EMS is busy for this period

EMS Qx Gate Tgr On

Hold Bit Qx Off

No

Block Active Bit Reset

Yes

No

Release Q0 - Q7

Yes

EMS 2.5 μsec Adr Counter Off NT923

CPE Tag Op Error Rtn (S/F Delay Mode)

Qx Full Bit Tgr On

Yes

Yes

Unit Return Qx Gate Tgr On

No

Loop Mode Sw Off NU816

Not Logout or Display Tgr On NU827

Any CR X Active Reset NT708 NT743

Tof Qx Active Bit Tgr NT704 NT739

Yes

Hold Qx Info for Logout

Qx Error Hold Tgr On

No

1. Clear Qx Control Register NT620 - NT762
2. Tof Qx Busy Tgr NT424 - NT431

1. Reset CR X NT746
2. Return Qx to Avail Pool

If this is the active bit reset sequence after the set tag request is sent to EMS, wait for SPM Advance (See Sheet 3)

DIAGRAM 5-402. CPE SET KEY (TAG) REQUEST TO EMS (SHEET 2 OF 3)

Set Tag Error Return (S/F Delay Mode)

Objectives:
1. Decode the S/S Link Address from SPM to determine which Q register is waiting for the return.
2. Enter the set tag error return into output priority for the unit return bus; the request is represented by the Qx hold bit (the output priority sequence is performed to reset the Qx active condition).
3. Determine if the Qx CPE request was loaded before any other CPE request in the Q.
4. Clear the Qx control register and return Qx to the available pool if no errors were returned by SPM.
5. Run the three-cycle data skew counter to generate ending resets.

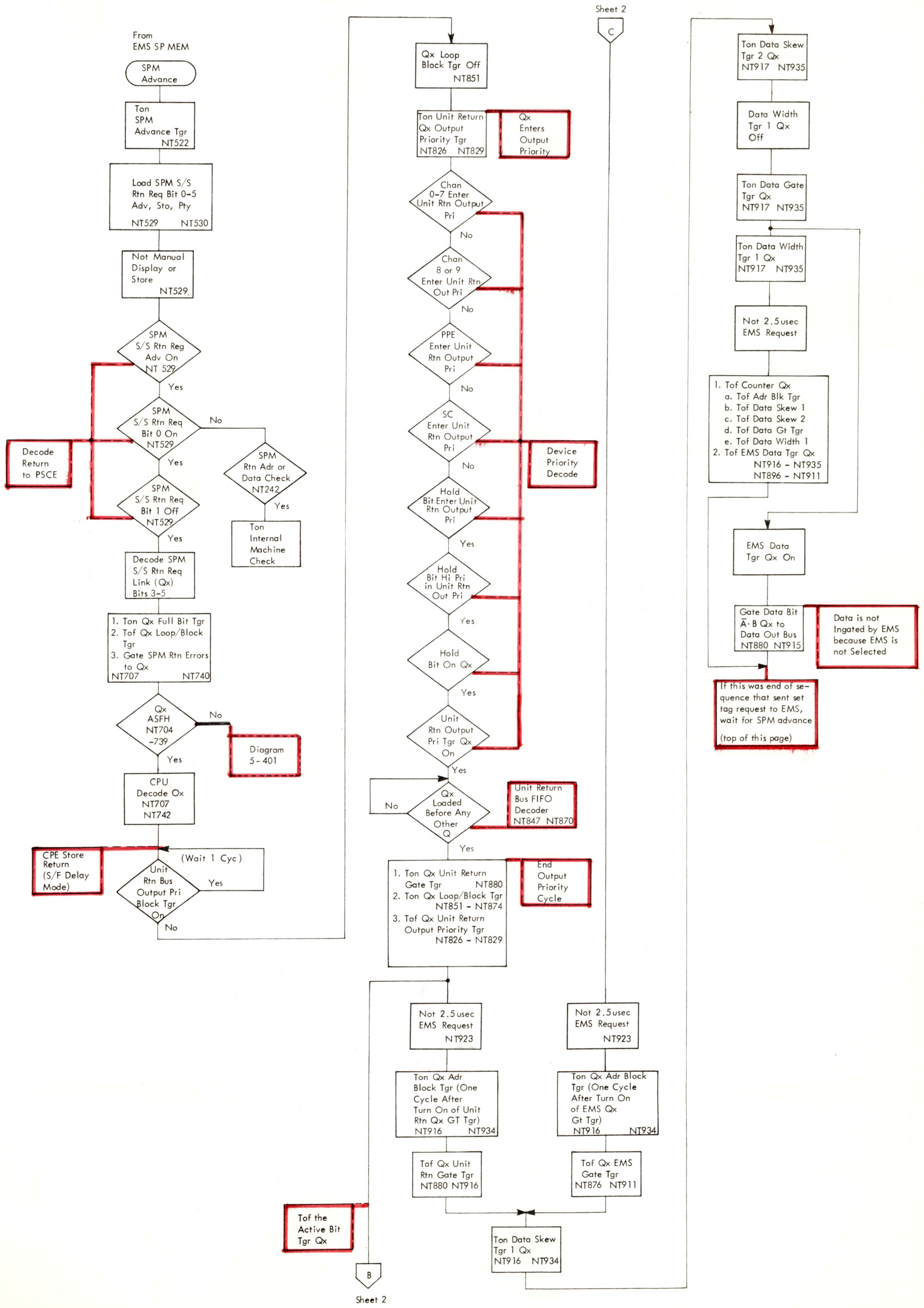


DIAGRAM 5-402. SET KEY (TAG) REQUEST TO EMS (SHEET 3 OF 3)

Start Channel
Reserve Q
Start Storage Request

SIO, Sel Chan X, and I/O Adr from CPU, NU171, 180, 259

Not CCC manual or DC gate

CPU Gate

Gate I/O Adr (Via UAB) and Select to Chans

Not SIO Intlk On (C25)

Ton SIO Sync NU175

Is Selected Chan in Operation NU263 (H24)

No

Yes

Set Hi Sample NU259

Decode I/O Adr Bits 0-4 (from UAB) NU186

Selected Chan Designated High Spd

No

Yes

Low spd operation See Diag 4-404

Pref1 Mode

No

Yes

Hi In Use Ctr > 4

Yes

No

Hi In Use Ctr > 3

No

Pref2 mode

1

1

Max Number Hi Chans in Use; Do SIO Low Speed Chan Sequence (See Diagram 5-404)

Set Chan X Hi Cond (H23) NU261

Not Rel Hi Gate On

Increment Hi in Use Counter (D22-24) NU315

Pref1 Mode

Yes

No

Pref2 mode

Ton Rsv 2 Tgrs 1 and 2 NU317

Pref2 mode only

Ton Reserve Request NU317

Rsv Resp Lth Off

No

Yes

Rsv Req or Resp On

Yes

No

Ton SIO Gate (C22) NU175

1. Ton SIO Interlock (C25)
2. Allow SIO Sync Reset NU176

Sel Chan Hi Cond NU261

No

Yes

Ton SIO Busy Gate (C23) NU175

1. Ton SIO Interlock (C25)
2. Allow SIO Sync Reset NU176

Prefetch 2 mode only

Allow Rsv Resp Lth to Set (1 Cycle) NU223

Reset Rsv 2 Tgr 1 NU317

Rsv 2 Tgr 2 On

No

Yes

Reset Reserve Request NU317

Rsv Resp Lth Reset

Reset Rsv 2 Tgr 2 NU317

On only one cycle

Send Rsv Req to In Pri NU317-NT456 (C26)

One or More Q Avail

No

Yes

Not Wait for SC In One Q

U Rtn Bus Return Cycle

Yes

No

Assign Qx from Top

Ton Qx Reserved (A-H02) NT424-NT431

Ton Reserve Priority (Send Rsv Resp to CCC) (A07) NT466

Sheet 3

H

Sheet 2

E

Ton Allow SIO (C24) NU176

See Diagram 5-408

Is this an IPL

Yes

No

Gate 240ns IPL Pulse to Channels NU173

Gate SIO to Chans NU171

Wait for control word fetch request

2

Chan Send CPU Release

Yes

No

Gate Release to CPU NU170

SIO from CPU Inactive

No

Yes

1. Reset SIO Interlock
2. Reset Allow SIO
3. Reset SIO Busy Gate

NU176-NU175

Cond Code from Chan = 00 NU170

Yes

No

Set Sel Chan X In Operation (H24) NU263

2

SIO Busy Gate

Yes

No

End Operation

Force Channel End NU177

To release sequence terminate operation

A

Sheet 4

Storage Req from Sel Chan NU263

No

Yes

Yes

SIO (or IPL)

No

Chan X Rel Tgr On

If Yes, (See sheet 5)

No

Chan X Rel/Resp Pri Tgr On

Yes

No

IF1 Resp Cycle

Yes

No

Set Chan X Req Sync NU240

Higher Priority Sync Tgr On

Yes

No

In Pri Resp Latch Off

No

Yes

B

Sheet 2

Notes:
1. Chan X reference pages are for channel 1

DIAGRAM 5-403. START I/O HIGH SPEED CHANNEL (SHEET 1 OF 4)

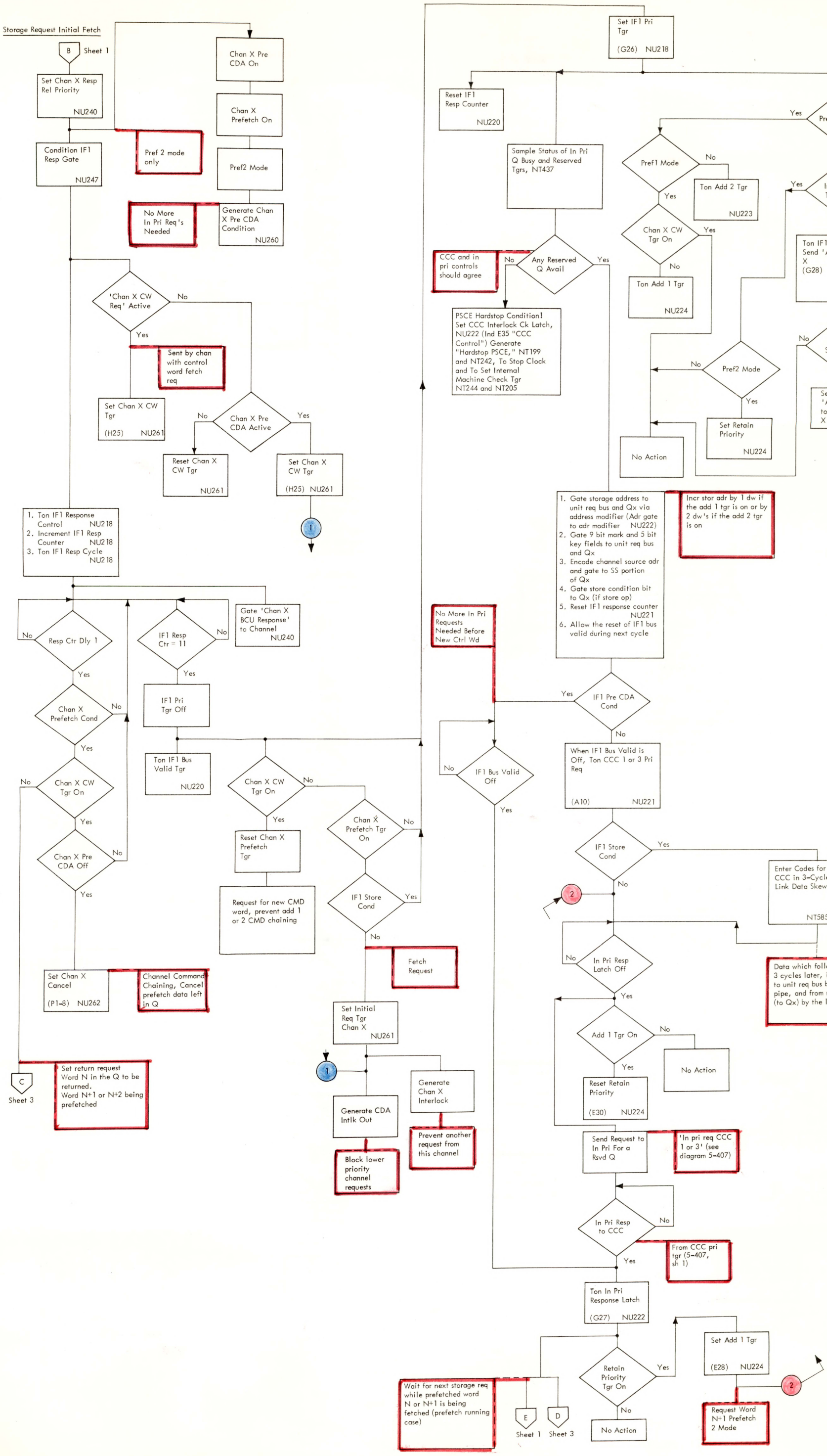


DIAGRAM 5-403. START I/O HIGH SPEED CHANNEL (SHEET 2 OF 4)

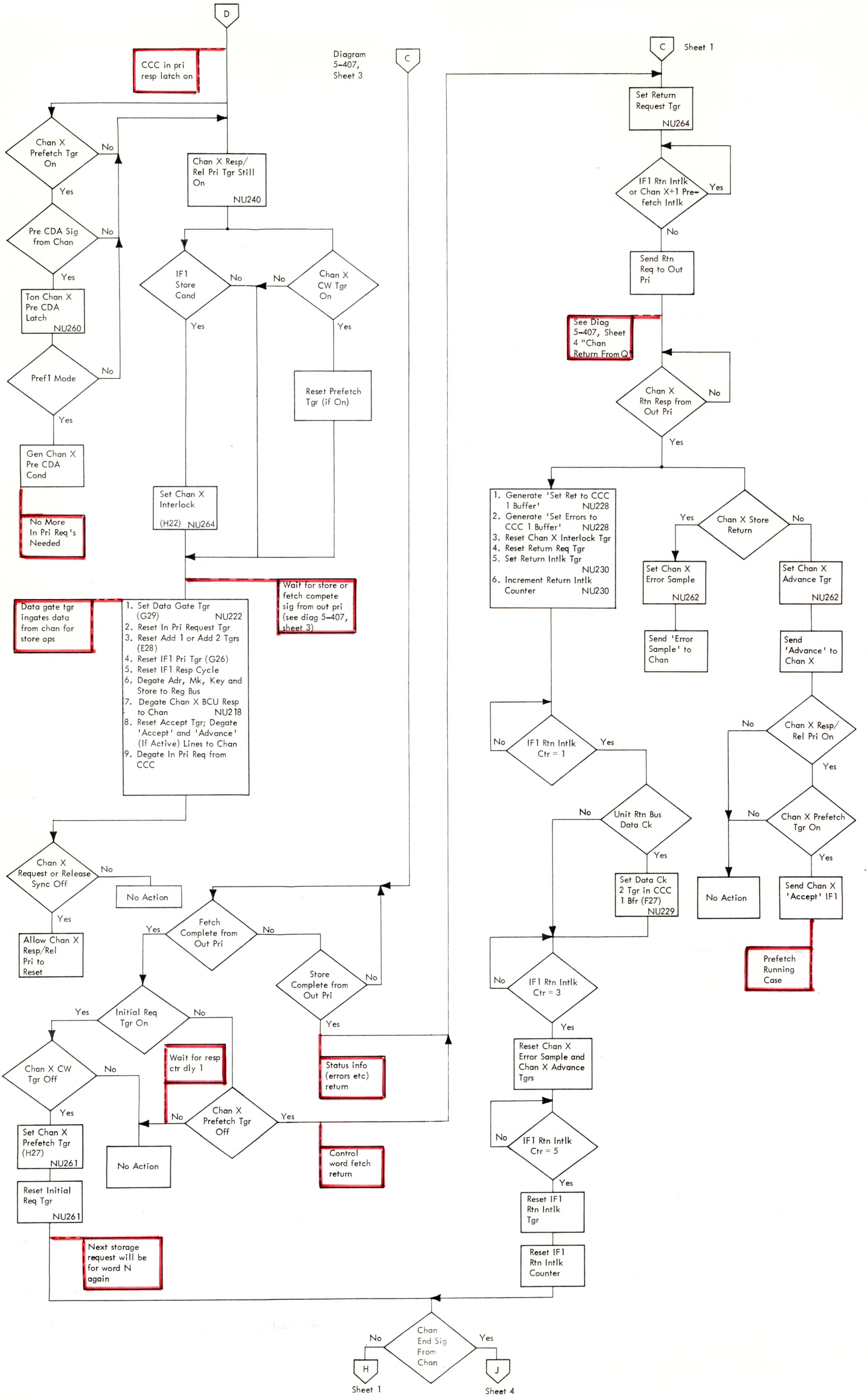


DIAGRAM 5-403. START I/O HIGH SPEED CHANNEL (SHEET 3 OF 4)

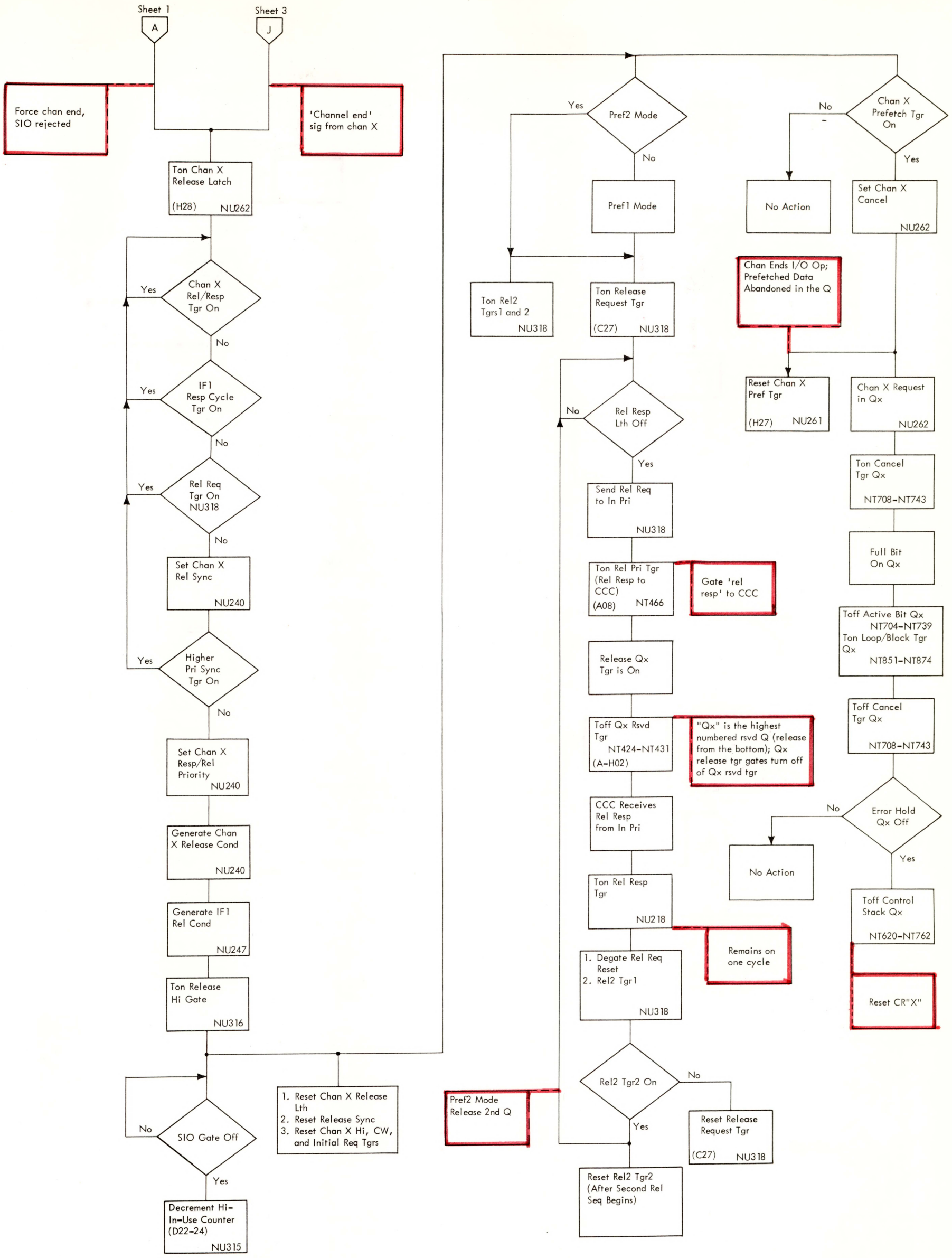


DIAGRAM 5-403. START I/O HIGH SPEED CHANNEL (SHEET 4 OF 4)

SIO
Reserve Q

SIO, Sel Chan X, and I/O Adr from CPU
NU171, 180, 259

Not CCC Manual or DC Gate

CPU Gate

Gate I/O Adr (Via UAB) and Select to Chans

Not SIO Intlk On (C25)

Ton SIO Sync
NU175

Is Selected Chan In Operation (H24) NU263
No
Yes

Yes: Rsv Req or Resp On
No

Ton SIO Busy Gate (C23)
NU175

Chan will generate CC = 10

Ton SIO Gate
(C22) NU175

1. Ton SIO Interlock (C25)
2. Allow SIO Sync Reset
NU176

1. Ton SIO Interlock (C25)
2. Allow SIO Sync Reset
NU176

Decode I/O Adr Bit 0-4 from UAB
NU186

High speed op (See Diag 5-406)

Sel Chan Designated Low Speed
No
Yes

Increment Lo-In-Use Counter by 1
(D25-28) NU315

Low Q-Rsvd Ctr = 0 NU322
No
Yes

Reserved ctr is assumed to be ahead of the low-in-use ctr

Lo-In-Use Ctr = Lo-Q-Rsvd Ctr and <3
No
Yes

Maximum No of Q's Rsvd for Lo Speed Op is Optional, either 2 or 3

Ton Reserve Request Tgr (C26)
NU317

1 or more Q's Avail (A15-20)
No
Yes

Unit Rtn Bus Return Cycle
Yes
No

Not Wait for SC In One Q

Ton Rsv Pri Tgr (Send Rsv Resp to CCC)
NT466

Assign Qx from Top

Ton Qx Reserved (A-H02)
NT424-NT431

Reserve Response Arrives in CCC

1. Ton Rsv Resp Latch (On 1 Cyc) NU223
2. Increment Lo Q Rsvd Ctr (E22-23) NU315
3. Increment Lo Q Avail Ctr (E24-25) NU315

Sheet 4
G

Ton Allow SIO
(C24) NU176

See Diagram 5-408

Is this an IPL
Yes
No

Gate 240ns IPL Pulse to Channels
NU173

Gate SIO to Chans
NU171

Wait for control word fetch request

2

Chan Send CPU Release
Yes
No

Storage Req from Sel Chan NU263
No
Yes

Gate Release to CPU
NU170

Cond Code from Chan = 00 NU170
Yes
No

SIO from CPU Inactive
No
Yes

1. Reset SIO Interlock
2. Reset Allow SIO
3. Reset SIO Busy Gate
NU176-NU175

Set Sel Chan X In Operation
(H24) NU263

2

SIO Busy Gate
Yes
No

End Operation

Force Channel End IF1
NU177

B
Sheet 4

A
Sheet 2

Notes:
1. Channel X references are for channel 1

DIAGRAM 5-404. START I/O LOW SPEED CHANNEL (SHEET 1 OF 4)

Storage Request

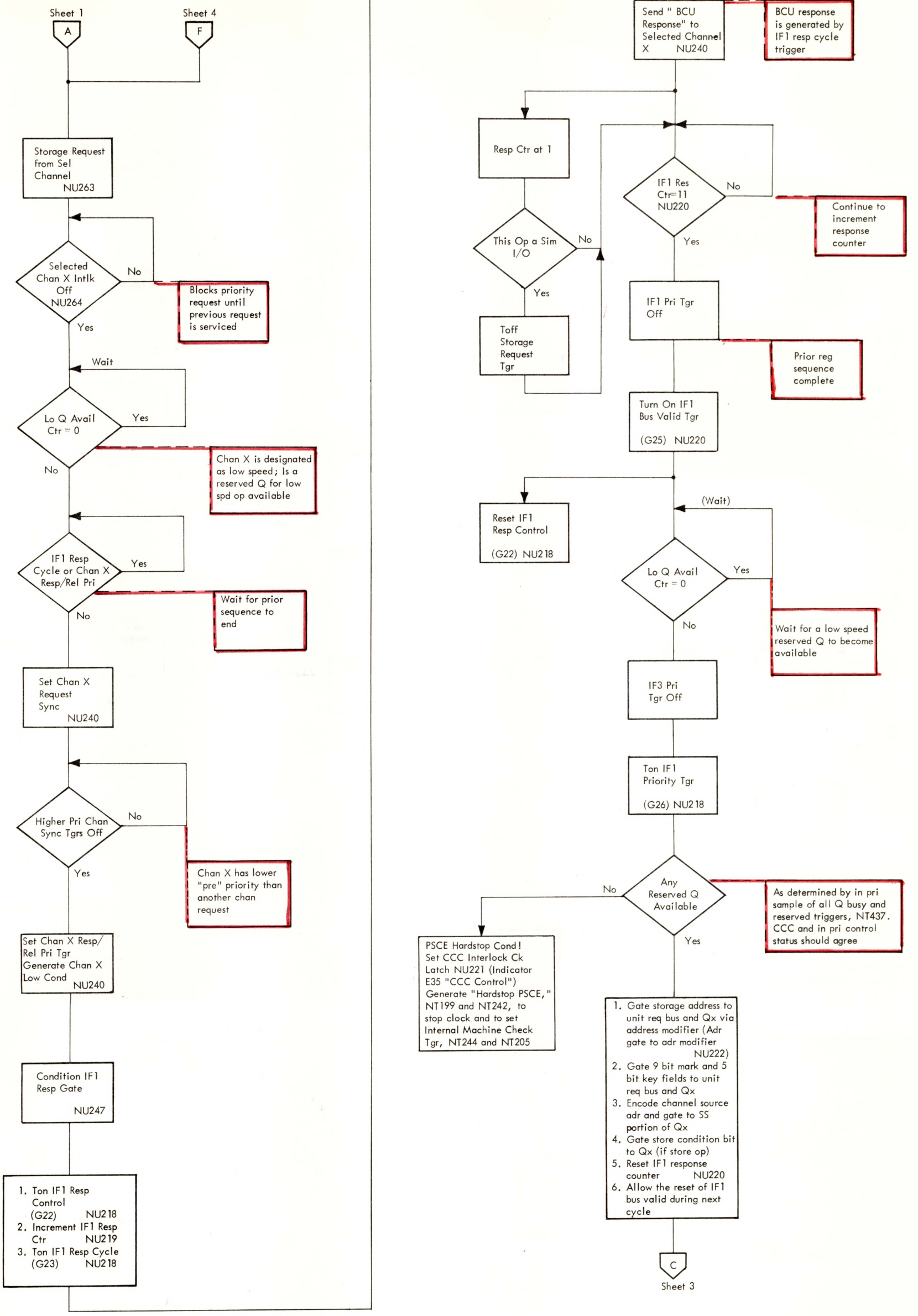


DIAGRAM 5-404. START I/O LOW SPEED CHANNEL (SHEET 2 OF 4)

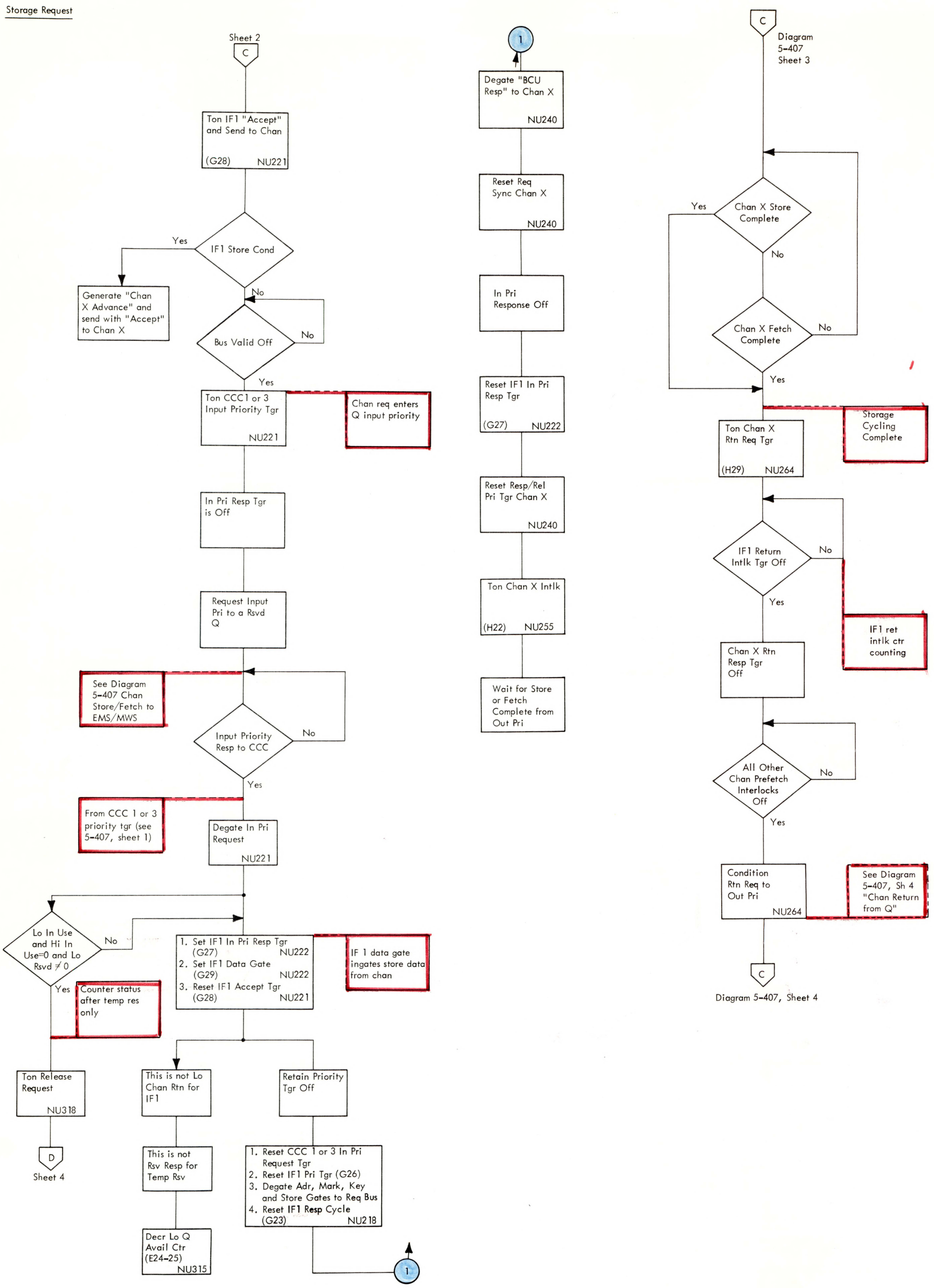
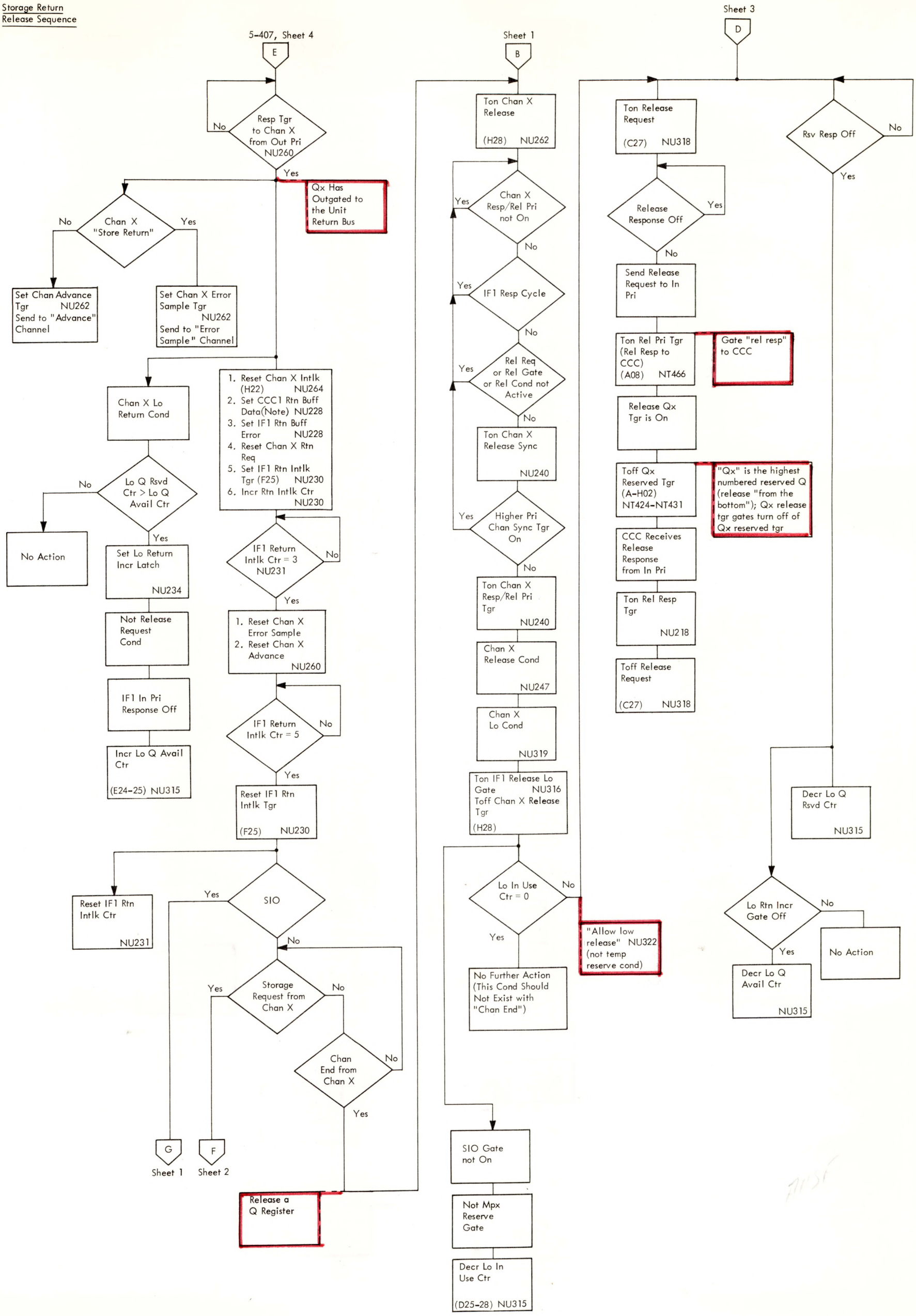


DIAGRAM 5 - 404 START I/O LOW SPEED CHANNEL (SHEET 3 OF 4)

Storage Return
Release Sequence



Note: Information set into the CCC1 return buffer is unconditionally gated to the channel via the SDBO.

DIAGRAM 5-404. START I/O LOW SPEED CHANNEL (SHEET 4 OF 4)

SIO Sequence
Accept Storage Requests
Determine Sub-channel

Objectives:

1. Accept SIO from CPU and generate 'allow SIO' to start sequence in channel 0.
2. Process storage requests for control words during SIO sequence.
3. Send 'BCU response' and 'Accept' to the channel for each storage request sequence.
4. Gate release and condition code to CPU.
5. Determine if a selector or multiplex sub-channel is in operation.

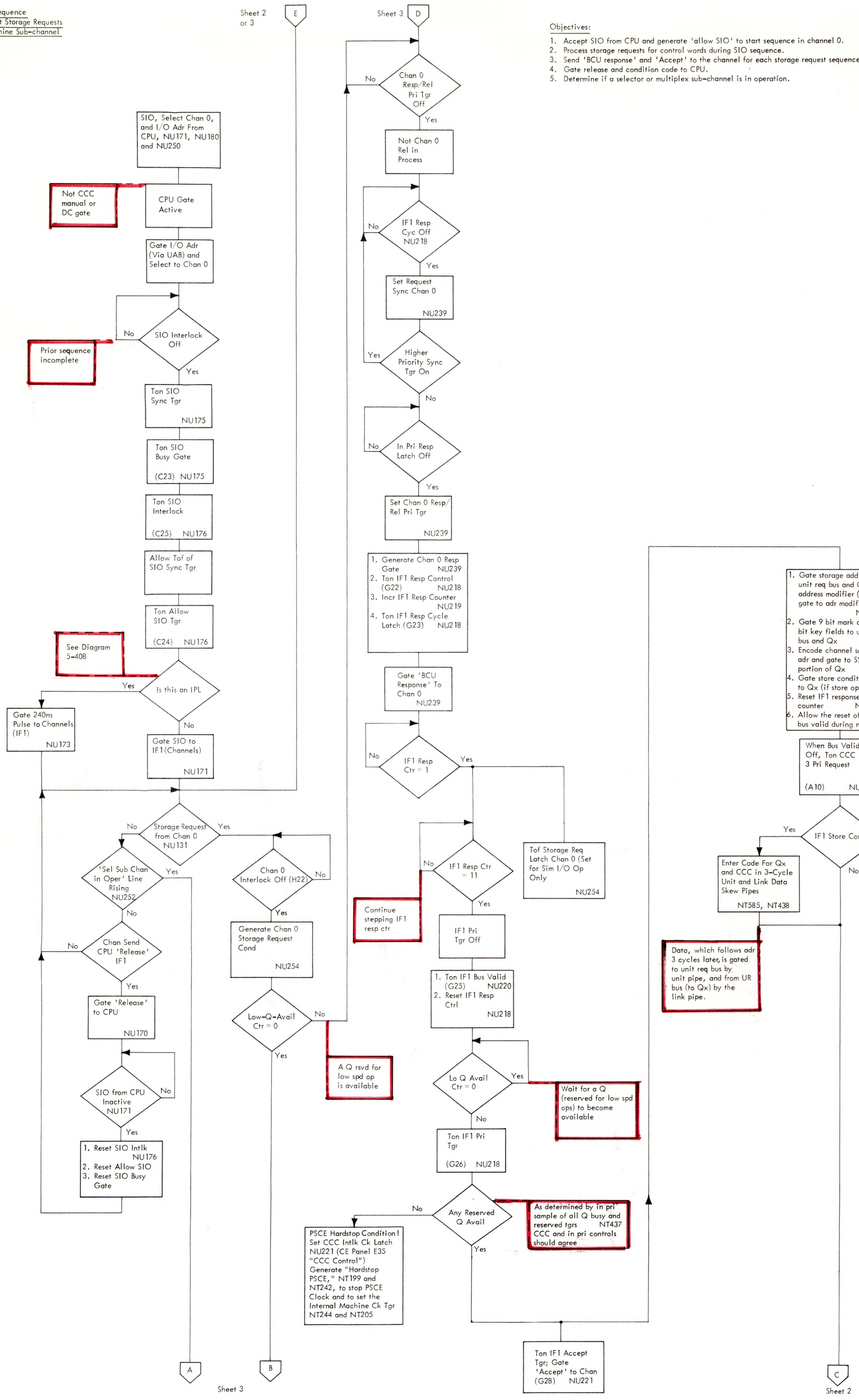
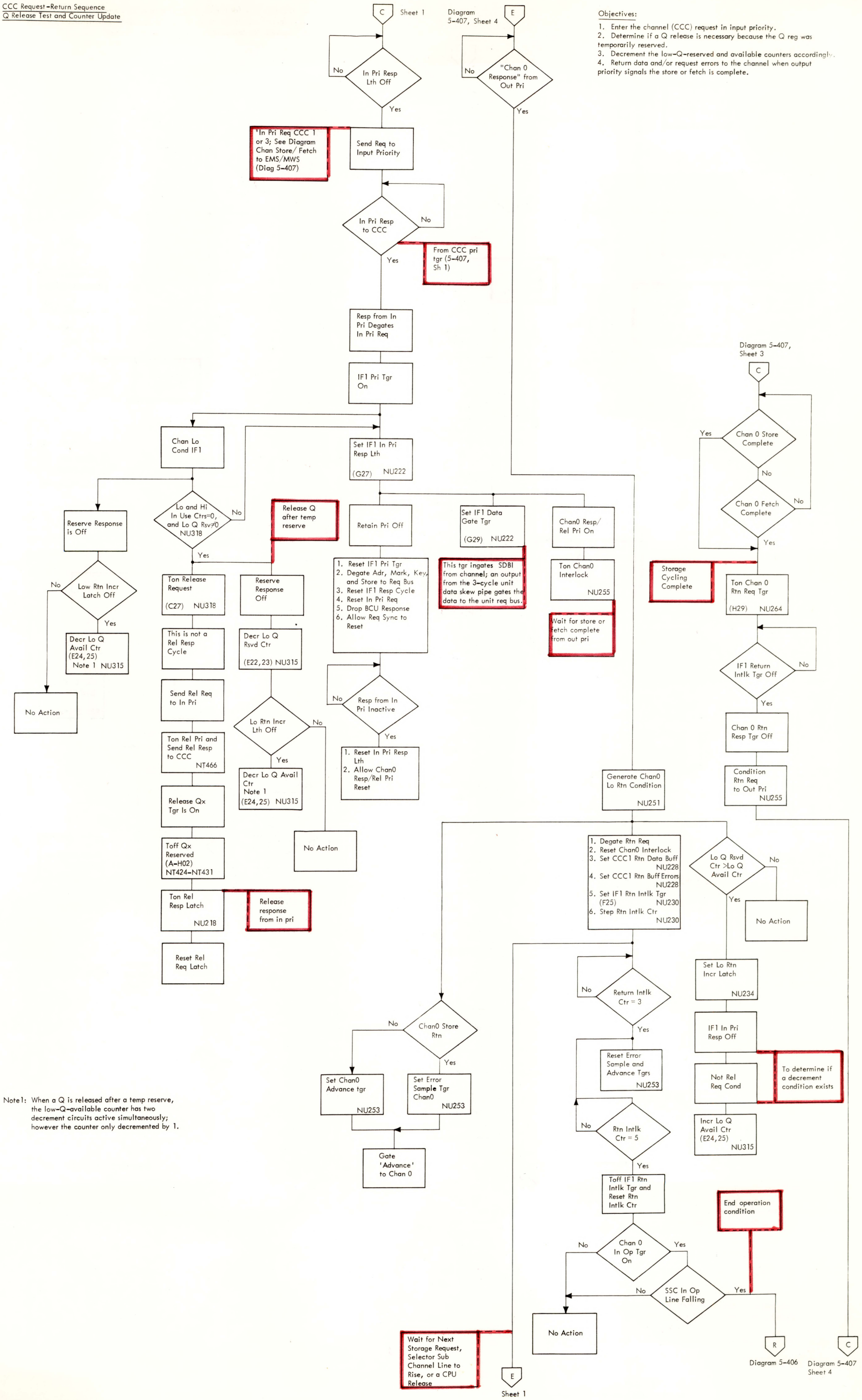


DIAGRAM 5-405. START I/O MULTIPLEXOR CHANNEL (SHEET 1 OF 3)

CCC Request-Return Sequence
Q Release Test and Counter Update

Objectives:

1. Enter the channel (CCC) request in input priority.
2. Determine if a Q release is necessary because the Q reg was temporarily reserved.
3. Decrement the low-Q-reserved and available counters accordingly.
4. Return data and/or request errors to the channel when output priority signals the store or fetch is complete.

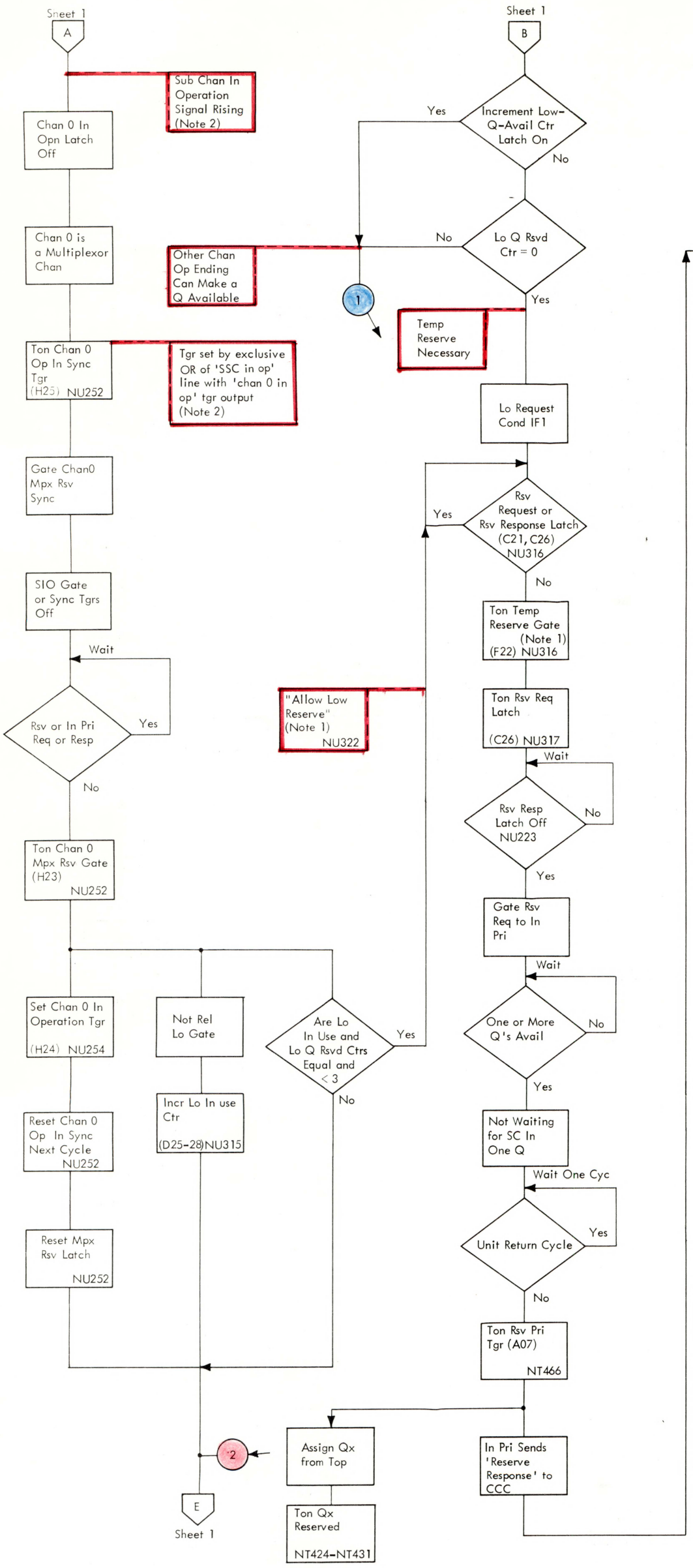


Note 1: When a Q is released after a temp reserve, the low-Q-available counter has two decrement circuits active simultaneously; however the counter only decremented by 1.

DIAGRAM 5-405. START I/O MULTIPLEXOR CHANNEL (SHEET 2 OF 3)

Objectives:

1. Reserve a Q (if none are reserved) for any mpx channel storage request during SIO.
2. Reserve a Q for the duration of a selector sub-channel I/O operation.
3. Reserve a Q temporarily for multiplex sub-channel storage requests if no Q is reserved (for low speed) when request is received.



Note 1: The temporary reserve gate circuitry is used to start a non-temporary Q reserve sequence when the multiplexor channel reserve gate is on; this is only a design convenience.

Note 2: Because any one of four sel sub-channels can control the 'SSC in op' line, the Chan 0 op sync tgr is turned on by the OE only when the SSC in op line first becomes active, and when it finally goes inactive.

DIAGRAM 5-405. START I/O MULTIPLEXOR CHANNEL (SHEET 3 OF 3)

Diag 5-405 Sheet 2

Objectives:

1. Release a reserved Q
2. Turn off channel 0 operation
3. Decrement lo in use, lo Q available and lo Q reserved counters.

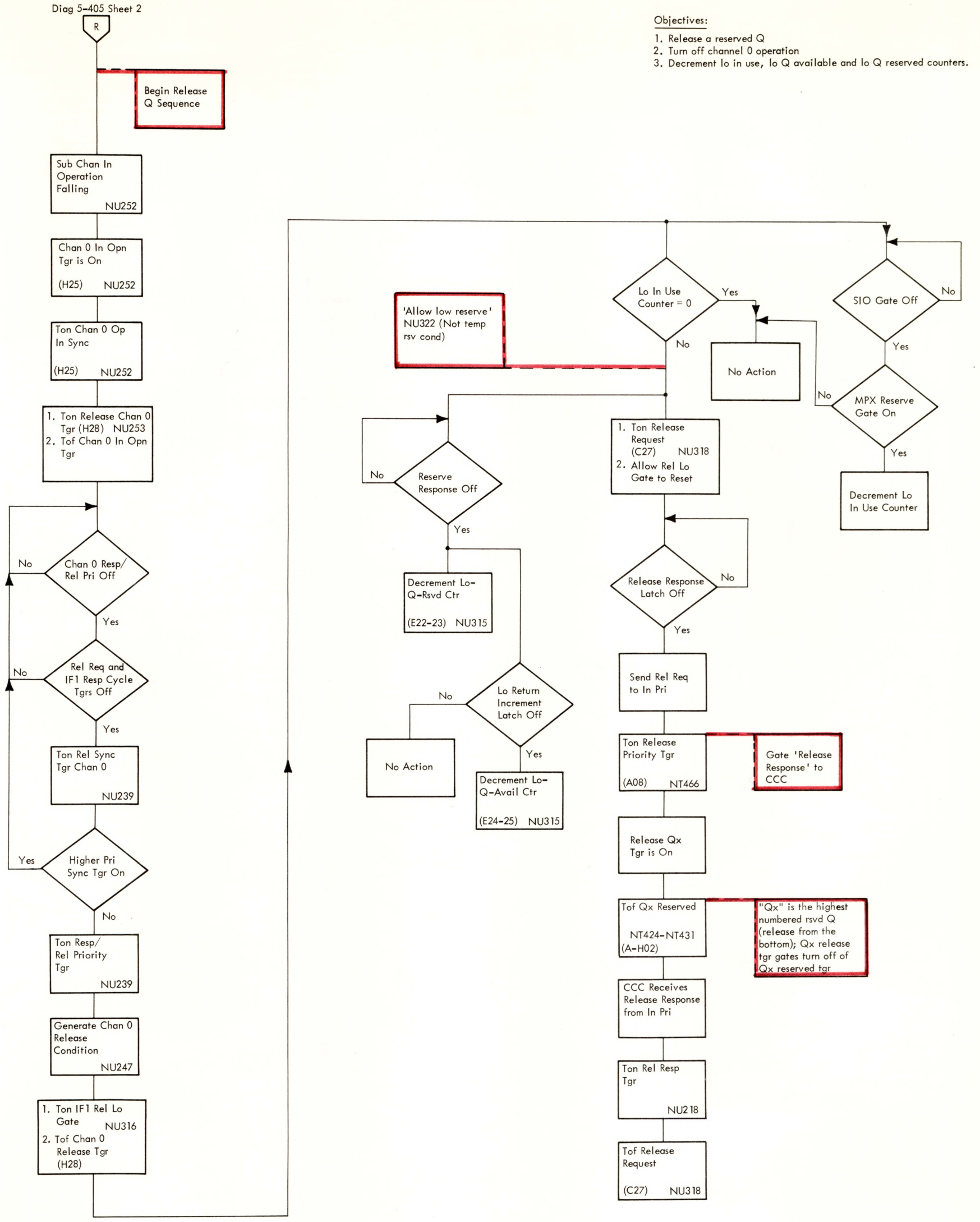


DIAGRAM 5-406. MULTIPLEXOR SELECTOR SUB-CHANNEL RESERVE/RELEASE

Enter Input Priority
Load Request in Qx
EMS Request Output Priority

Objectives:
1. Enter channel request into input priority.
2. Establish CCC input priority to the queue.
3. Assign request to a Q from reserved pool.
4. Encode unit and link 3 cycle pipes.
5. Load storage request into Q and turn on control bits.
6. Enter EMS request into output priority and obtain output priority. (See sheet 2 for MWS request)
7. Select EMS, BSM and outgate address info.
8. Outgate Q data to EMS or MWS bus 3 cycles after address information.

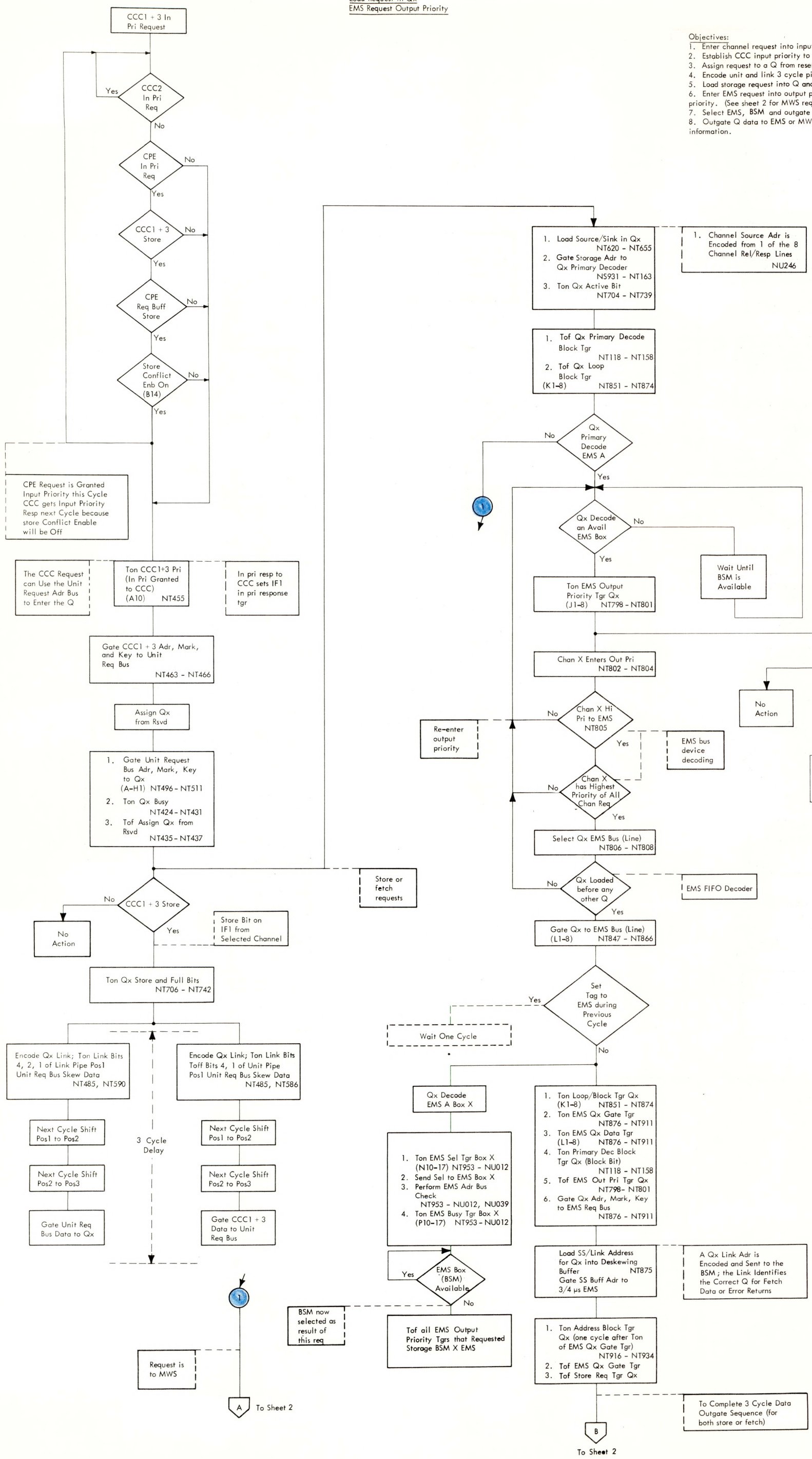
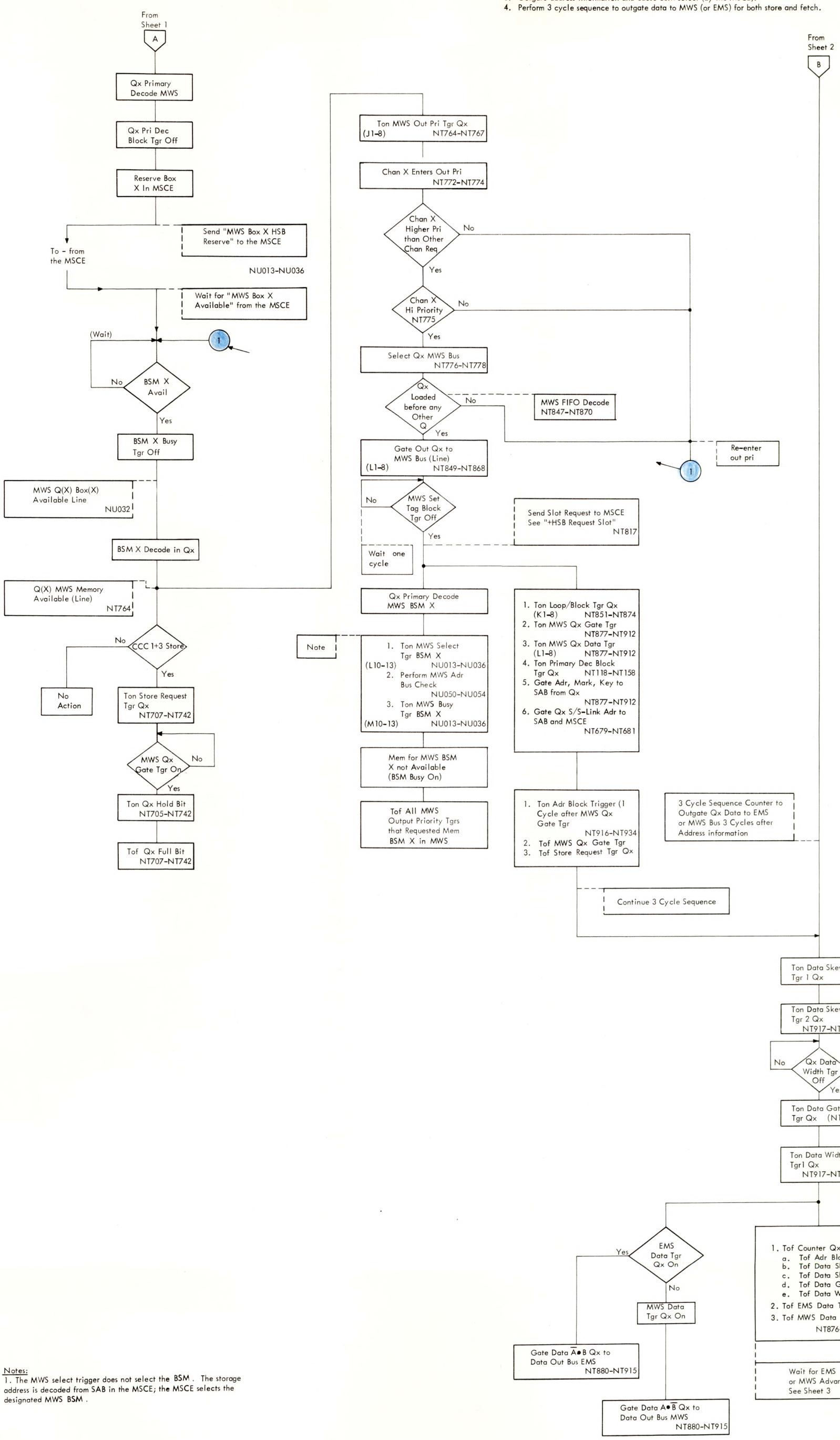


DIAGRAM 5-407. CHANNEL STORE/FETCH TO EMS/MWS (SHEET 1 OF 4)

MWS Request Output Priority
3 Cycle Sequence

Objectives:

1. Send reserve to the MSCE for an MWS BSM.
2. Enter request into output priority when MSCE returns 'BSM available.'
3. Outgate address information and cause BSM select (by the MSCE).
4. Perform 3 cycle sequence to outgate data to MWS (or EMS) for both store and fetch.



Notes:
1. The MWS select trigger does not select the BSM . The storage address is decoded from SAB in the MSCE; the MSCE selects the designated MWS BSM .

DIAGRAM 5-407. CHANNEL STORE/FETCH TO EMS/MWS (SHEET 2 OF 4)

EMS or MWS Return from Storage

Objectives:

1. Decode S/S to determine which Q register full bit to turn on.
2. Decode S/S one cycle later to determine which Q register receives returning data.
3. Decode Q register control bits to generate store or fetch return signal.

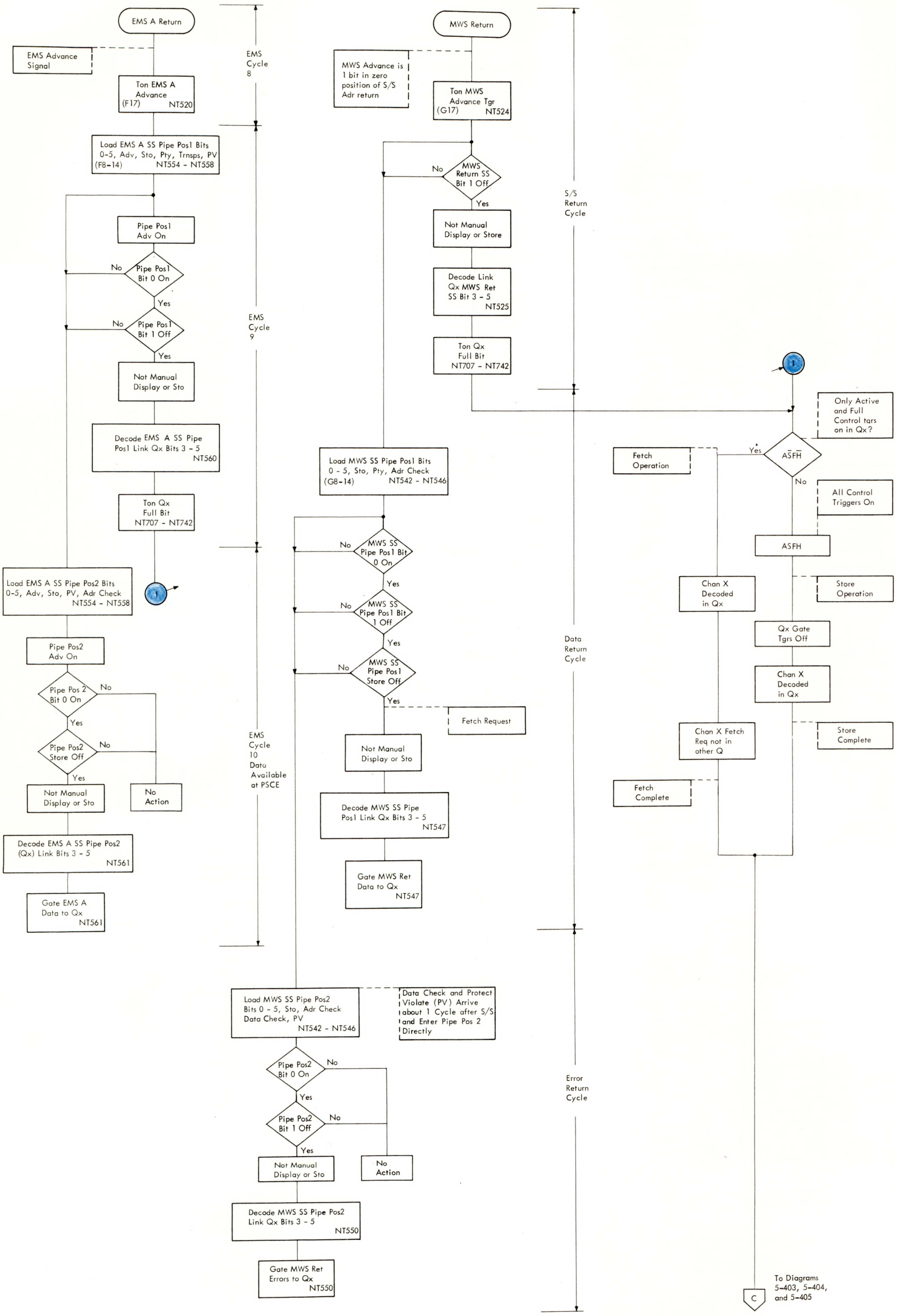


DIAGRAM 5-407. CHANNEL STORE/FETCH TO MWS/EMS (SHEET 3 OF 4)

Channel Return from Queue

Objectives:
1. Decode store or fetch complete condition begins sequence for return of errors or data from Q to the CCC .
2. Obtain output priority for use of the unit return bus from Qx to the CCC.
3. Send a response to the CCC .
4. Send a store signal only when returning errors.
5. Gate address errors, data errors, SP violation, invalid adr, or fetched data to the CCC.

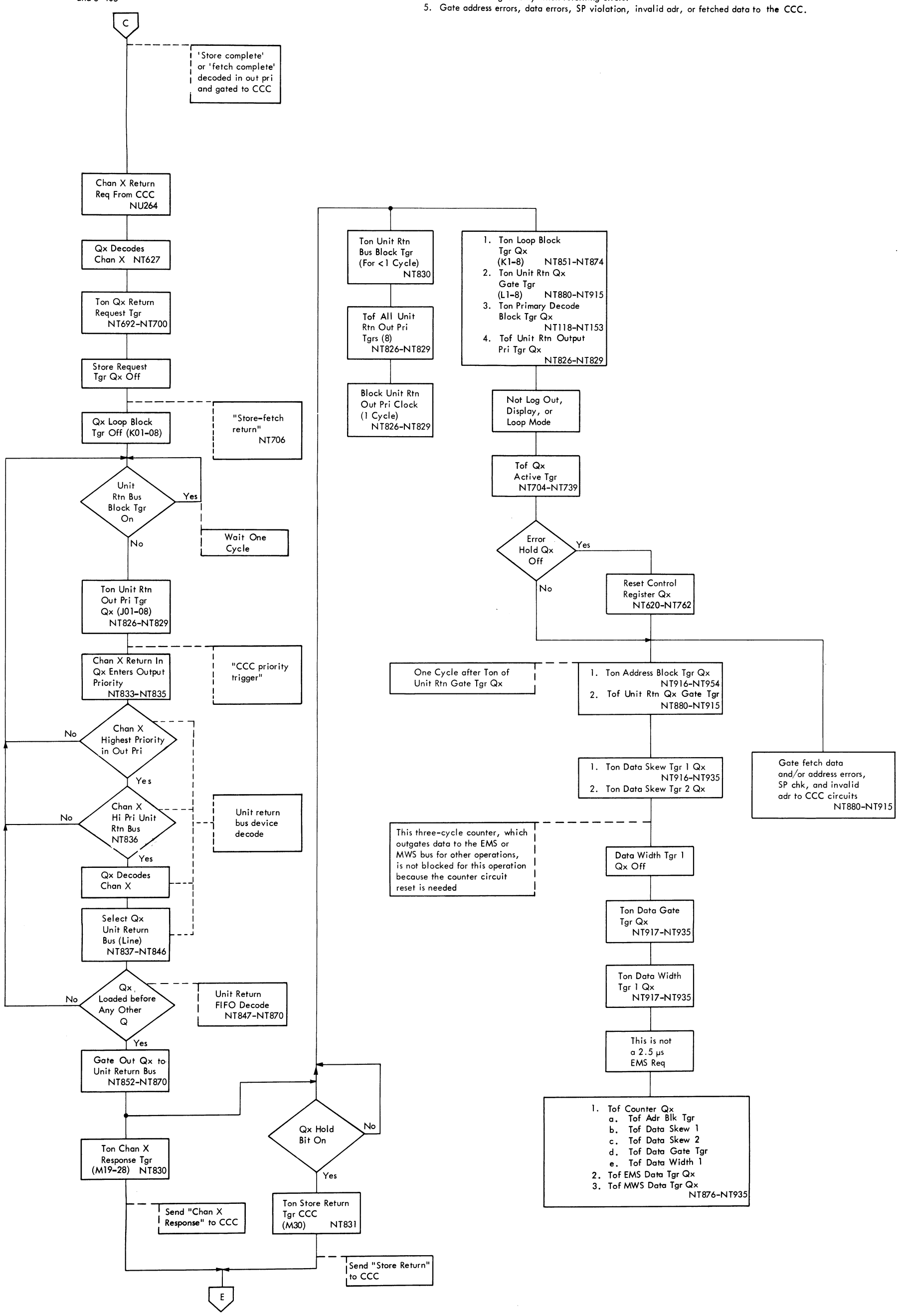


DIAGRAM 5-407. CHANNEL STORE/FETCH REQUEST TO EMS/MWS (SHEET 4 OF 4)

Objectives:

1. Show the generation of the 240 ns IPL pulse to channel.
2. Show the tie-in of IPL to the start I/O flow charts.

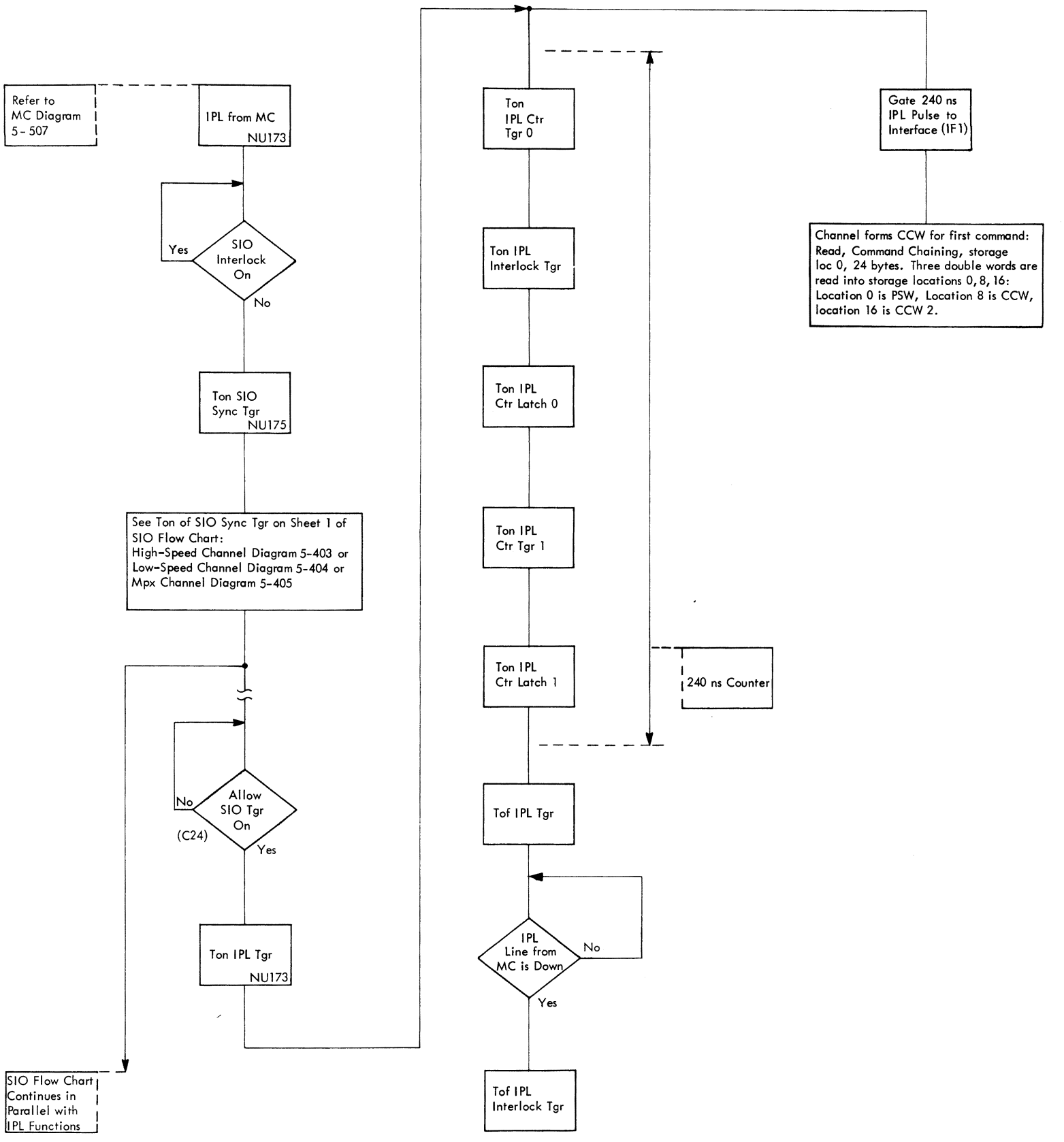


DIAGRAM 5-408. INITIAL PROGRAM LOAD (IPL)

Objectives:

1. Check for channel availability, no interrupts pending, no errors on, to select the storage channel (Channel 6).
2. Gate the CAW into a Q and then transfer the CAW into the A register.
3. Check for any error conditions, which will bring up terminate immediate.
4. Bring up release and turn on CC bits if Start I/O is unsuccessful.

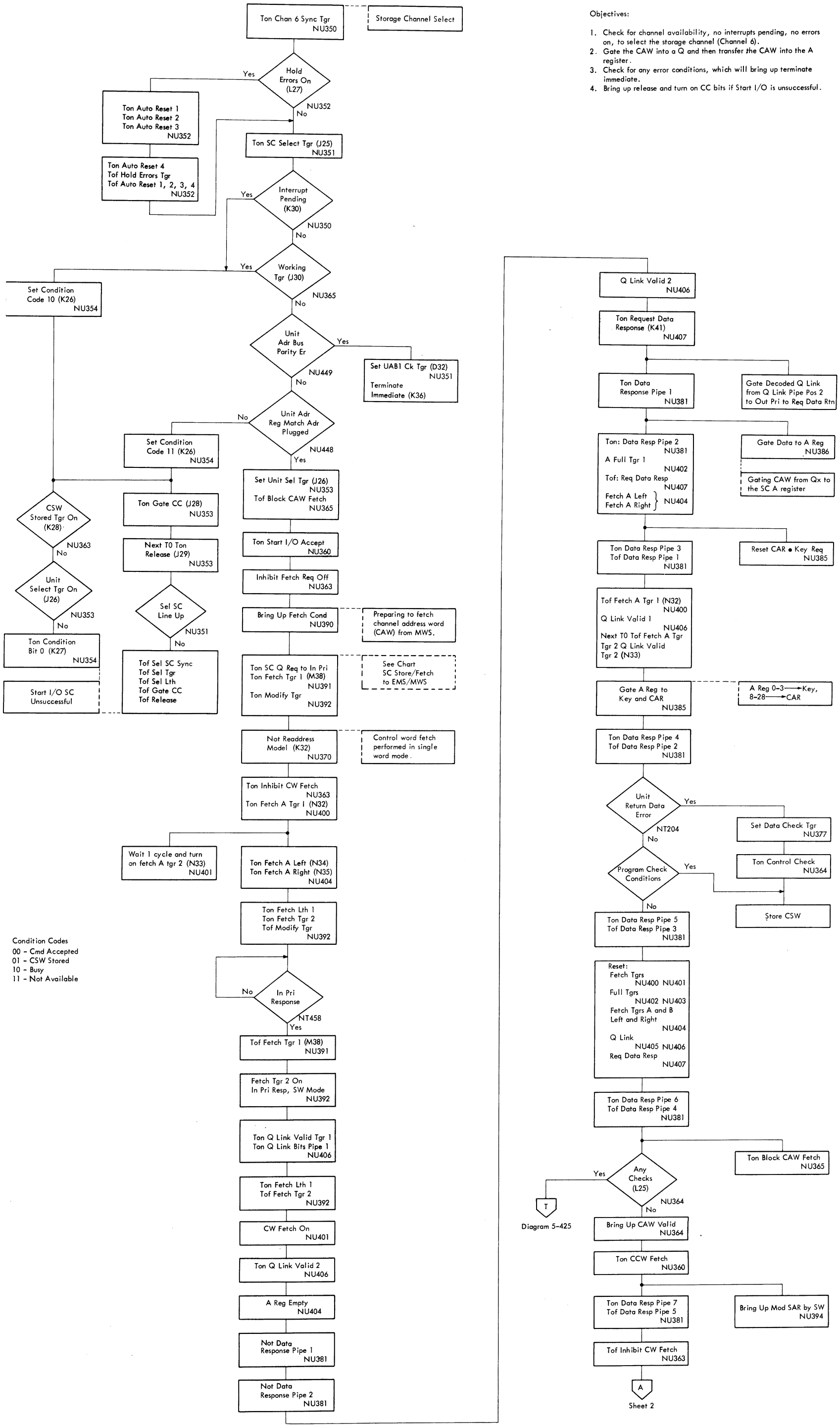


DIAGRAM 5-409. START I/O STORAGE CHANNEL (SHEET 1 OF 3)

Objectives:

1. Perform CCW fetch, for 1st CCW, using address in CAR for fetch address. Command specifies a position or position and skip operation.
2. Increment CAR by 8 bytes (1 double word) for next CCW or PAW
3. Gate CCW into a Q and then into the "A" register for distribution to other storage channel registers.
4. Check for type of operation. This operation is set up to fetch a PAW.
5. Release CPU, PSCE will process operation.

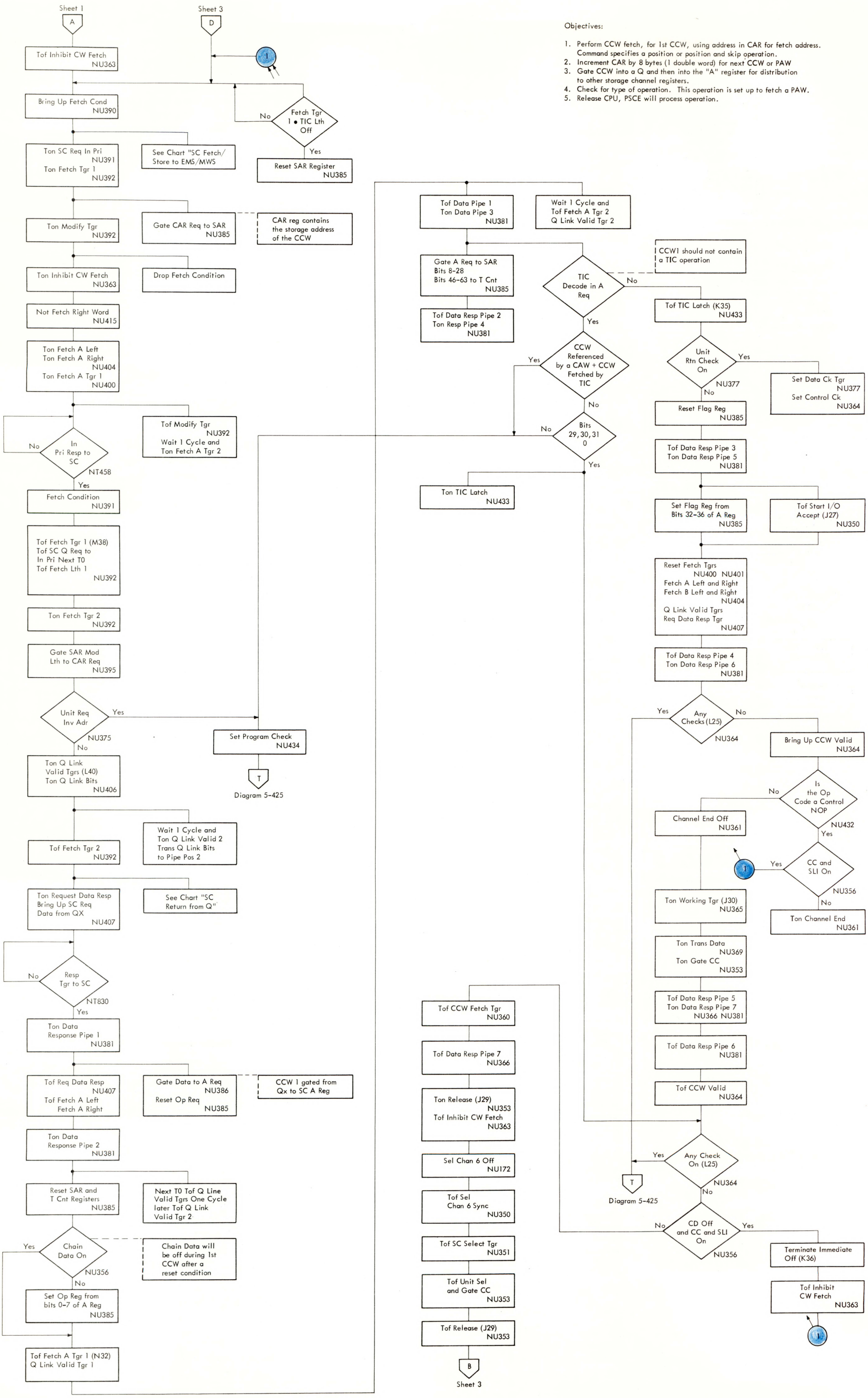


DIAGRAM 5-409. START I/O STORAGE CHANNEL (SHEET 2 OF 3)

Objectives:

1. Fetch the PAW (Position Address Word) using the address in the SAR.
2. Transfer data into a Q, to the "A" register, then bits 8-29 to PAR, and bits 48-61 into the displacement field.
3. Check for valid address, data check, protect check or for a position program check. Any of these will cause terminate immediate.
4. Go to fetch the next CCW.

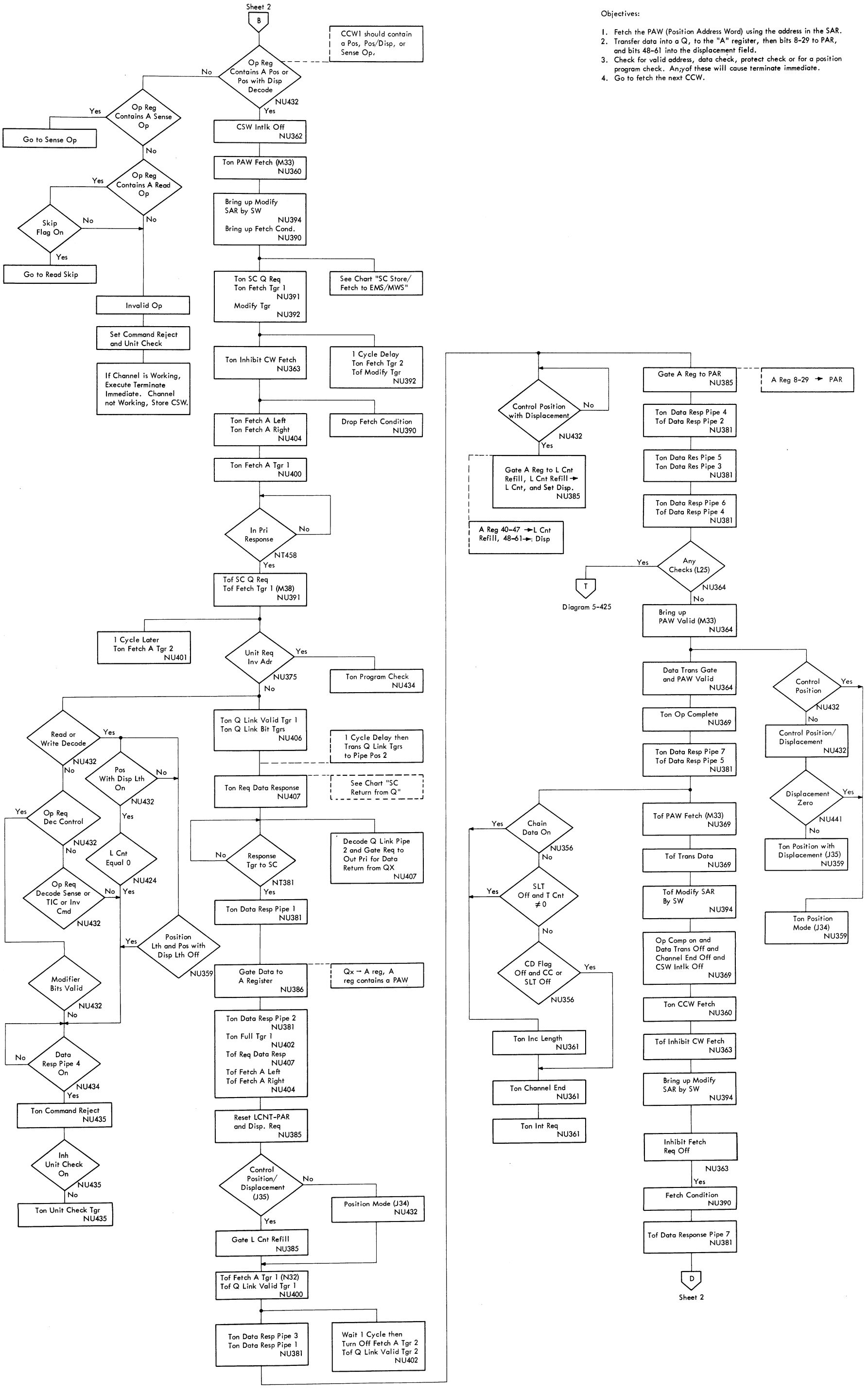


DIAGRAM 5-409. START I/O STORAGE CHANNEL (SHEET 3 OF 3)

Objectives:

1. Enter SC request into input priority.
2. Assign SC request to Q from available pool (Qx), encode unit and link 3 cycle pipes.
3. Load SC request into Qx and turn on control bits, also enter request into output priority.
4. Send reserve to MWS BSM.
5. Turn off control bits.

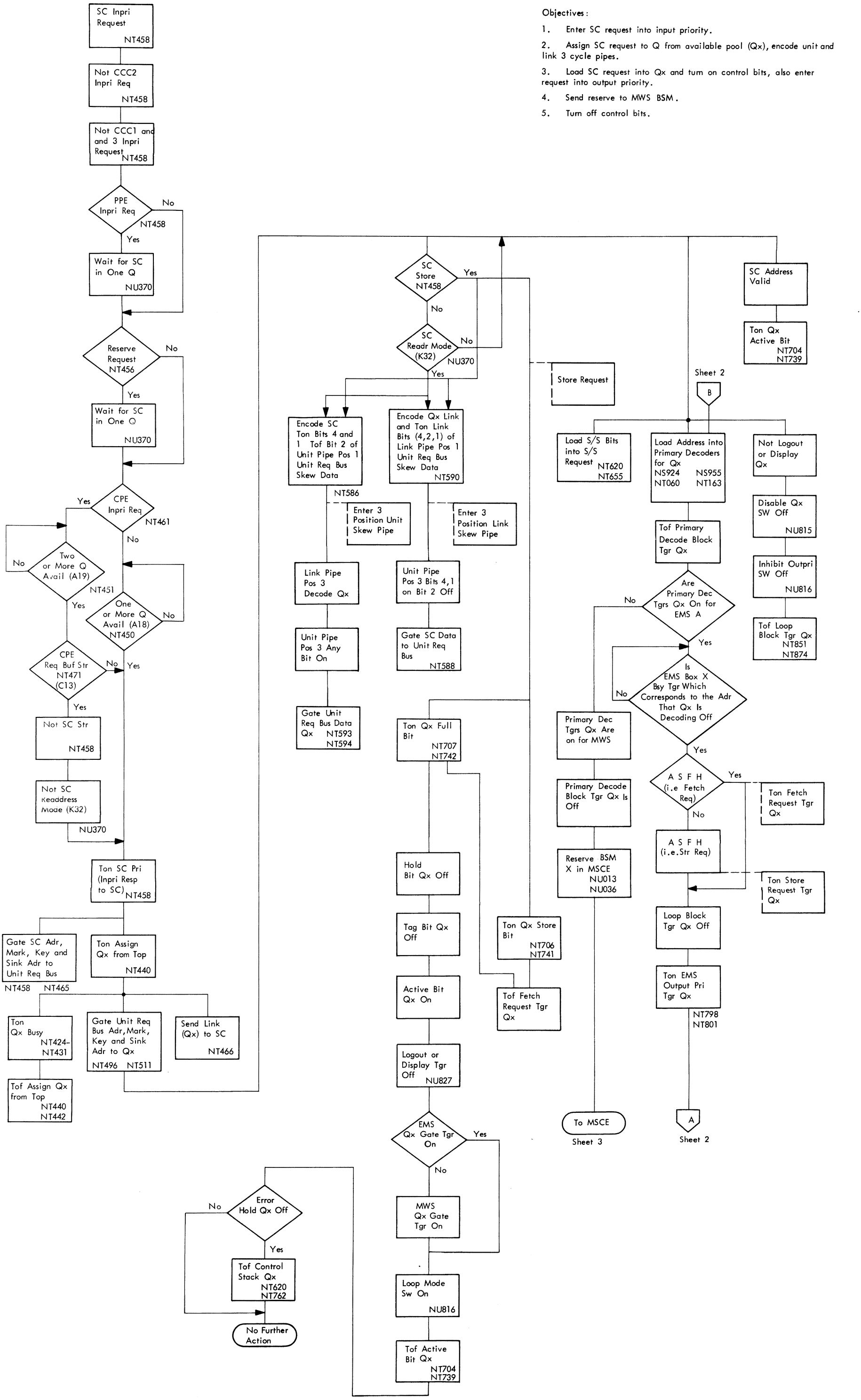


DIAGRAM 5-410. SC FETCH-STORE TO EMS/MWS (SHEET 1 OF 4)

Objectives:

1. SC request to EMS output priority decoding.
2. SC to EMS request select BSM and outgate address information.
3. Three cycle skew counter to outgate Qx data to EMS or MWS bus 3 cycles after address information.

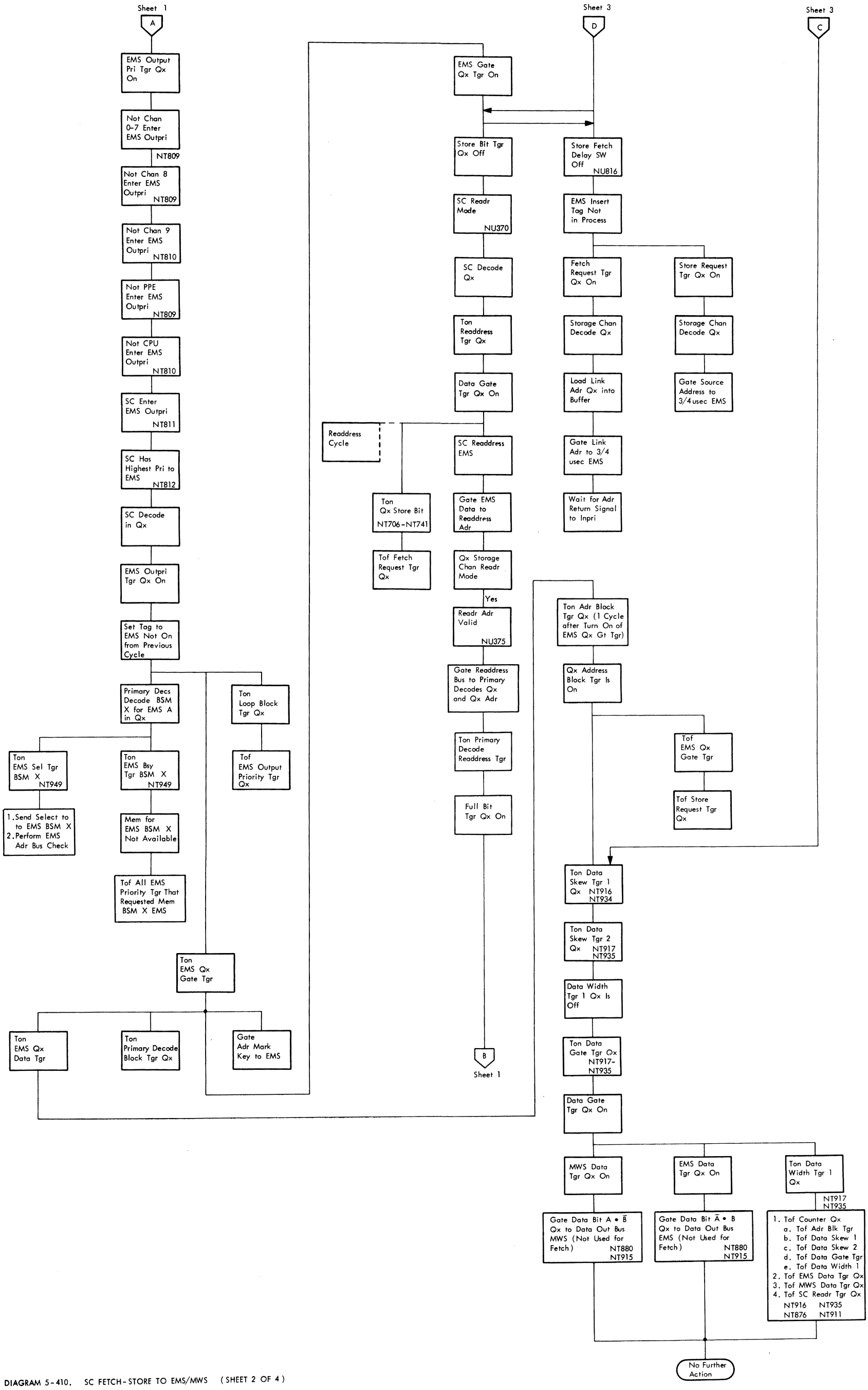
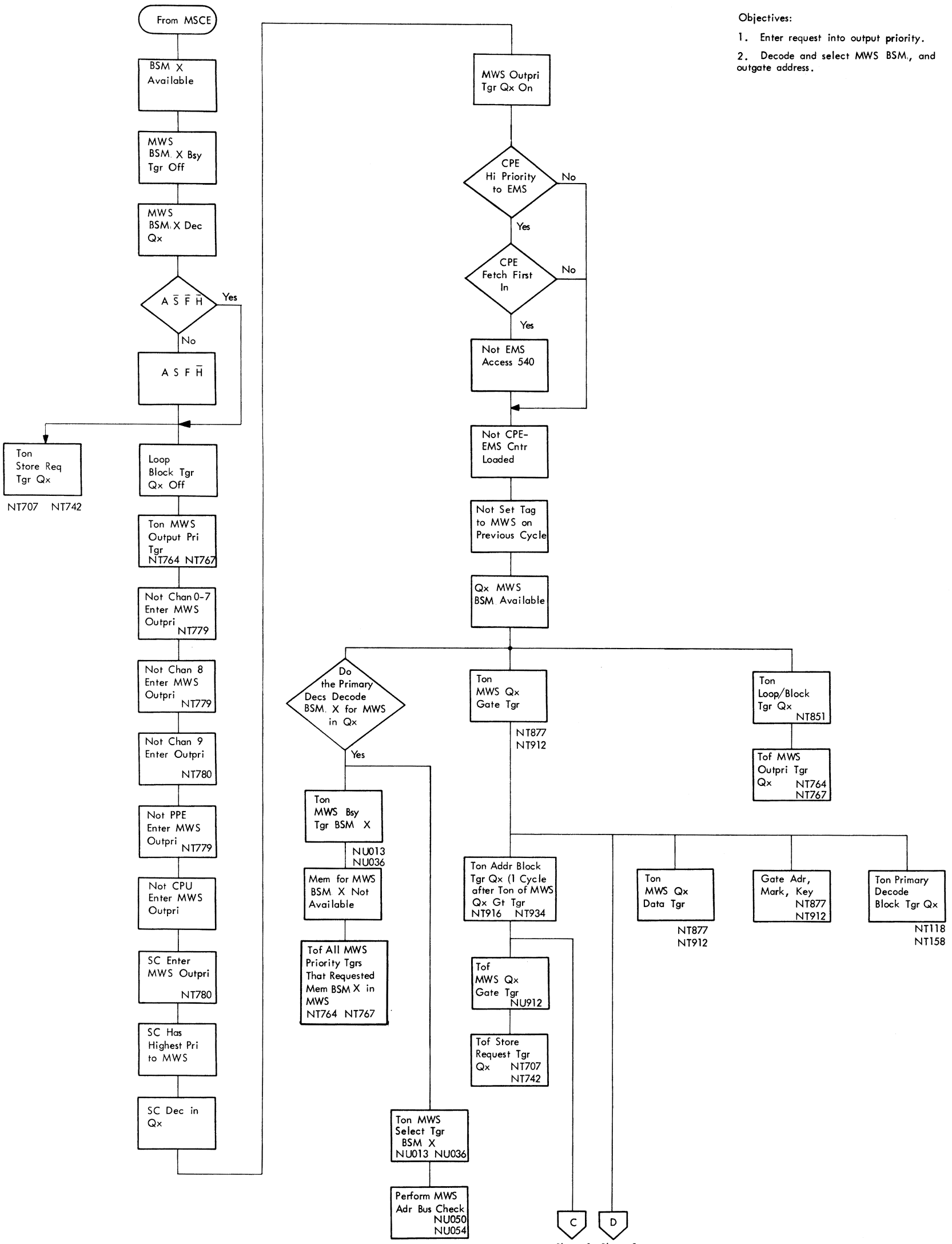


DIAGRAM 5-410. SC FETCH-STORE TO EMS/MWS (SHEET 2 OF 4)

Objectives:

1. Enter request into output priority.
2. Decode and select MWS BSM., and outgate address.



Sheet 2 Sheet 2

DIAGRAM 5-410. SC FETCH-STORE TO EMS/MWS (SHEET 3 OF 4)

Objectives:

1. EMS store or fetch return to Qx.
2. MWS store or fetch return to Qx.

EMS-A Advance

Ton EMS - A Advance NT520

Load EMS A S/S Pipe Pos 1 Bits 0 - 5 Adv, Sto Pty, Trnsp, PV NT554 NT558

EMS A S/S Pipe Pos 1 Advance On NT554

EMS A S/S Pipe Pos 1 Bit 0 On NT555

EMS A S/S Pipe Pos 1 Bit 1 Not On NT555

Not Manual Display or Store NU796

Decode EMS A S/S Pipe Pos 1 Link (Qx) Bits 3-5 NT560

Ton Qx Full Bit NT707 NT742

See "SC Return from Q"

Tof Fetch Req Tgr Qx

Load EMS A S/S Pipe Pos 2 Bits 0-5, Adv, Sto, PV, Adr Check NT554 NT556 NT558

EMS A S/S Pipe Pos 2 Adv On NT554

EMS A S/S Pipe Pos 2 Bit 0 On NT555

EMS A S/S Pipe Pos 2 Bit 2 On

Gate EMS A Return Errors to SC

EMS A S/S Pipe Pos 2 Store Not On NT554

Not Manual Display or Store NU796

Decode EMS A S/S Pipe Pos 2 Link (Qx) Bits 3-5 NT561

Gate EMS A Data to Qx NT561

See "SC from Q"

EMS Cycle 8

EMS Cycle 9

EMS Cycle 10 Data Available at PSCE

MWS Return (S/S Bit Pos 0 Is 1)

Ton MWS Advance Tgr NT524

Not MWS Return S/S Bit 1 NT543

Not Manual Display or Store NU796

Decode Link (Qx) MWS Return S/S Bits 3-5 NT525

Ton Qx Full Bit NT707 NT742

Tof Fetch Request Tgr Qx

See "SC Return from SC"

Load MWS S/S Pipe Pos 1 Bits 0-5 Sto, Pty, Adr Ck, Pr NT542 NT546

MWS S/S Pipe Pos 1 Bit 0 On NT542

MWS S/S Pipe Pos 1 Bit 1 Off NT543

MWS S/S Pipe Pos 1 Store Off NT542

Not Manual Display or Store

Decode MWS S/S Pipe Pos 1 Link (Qx) Bits 3-5 NT547

Gate MWS Return Data to Qx NT547

Load MWS S/S Pipe Pos 2 Bits 0-5, Sto, Adr Ck, Data Ck, PV NT542 NT546

MWS S/S Pipe Pos 2 Bit 0 On NT542

MWS S/S Pipe Pos 2 Bit 2 On NT544

Gate MWS Errors to SC NT550

MWS S/S Pipe Pos 2 Bit 1 Off

Not Manual Display or Store NU796

Decode MWS S/S Pipe Pos 2 Link (Qx) Bits 3-5 NT550

See "SC Return from Q"

Gate MWS Return Errors to Qx NT550

S/S Return Cycle

Data Return Cycle

Error Return Cycle

DIAGRAM 5-410. SC FETCH-STORE TO EMS/MWS (SHEET 4 OF 4)

Objectives:

1. SC return request enters output priority.
2. Complete device and FIFO decode.
3. Turn off control bits and activate SC complete.

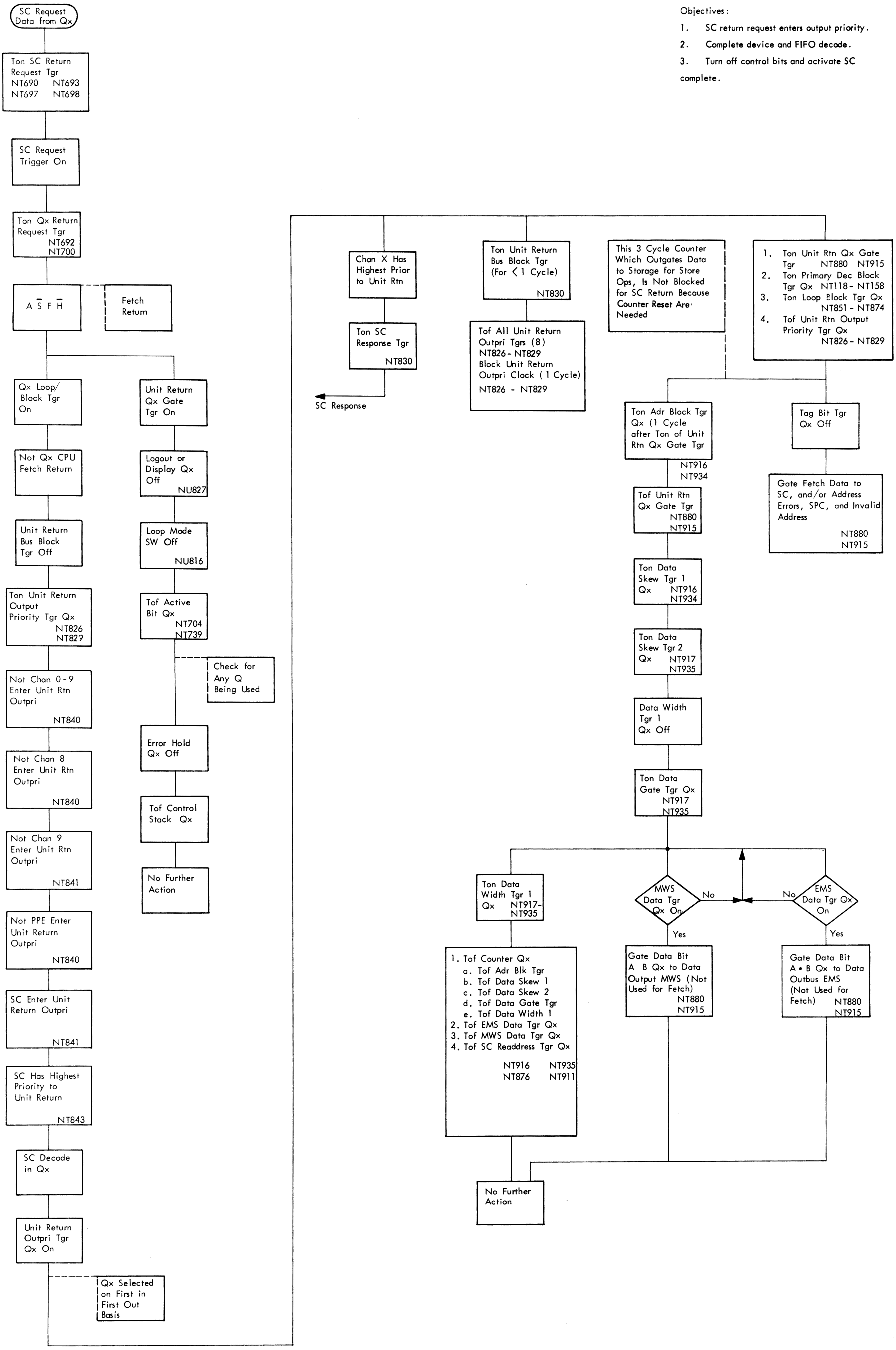


DIAGRAM 5-411. SC RETURN FROM QUEUE

Objectives:

1. On an interrupt to store the CSW.
2. To logout 6 doublewords of SC data and store the CSW.

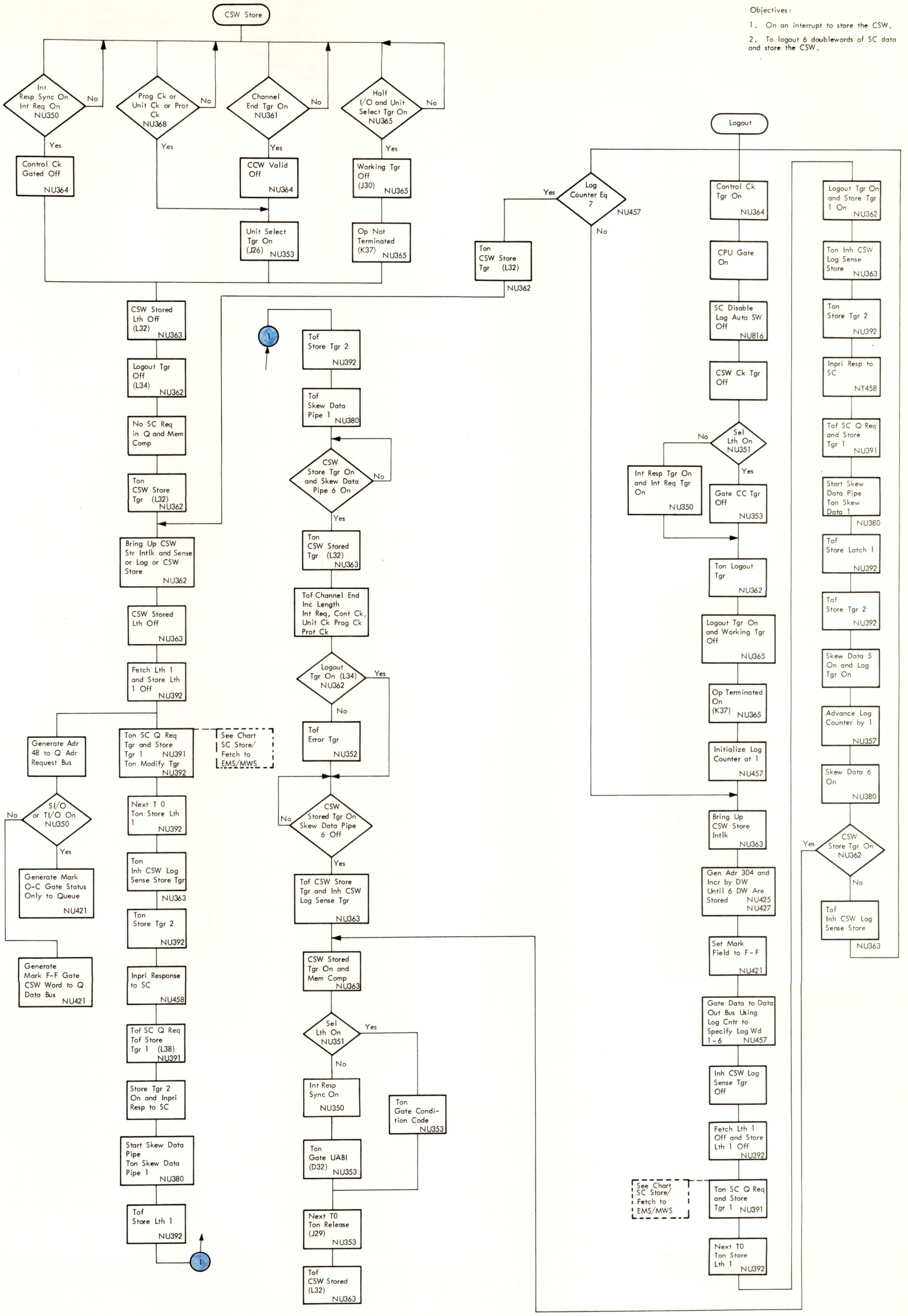
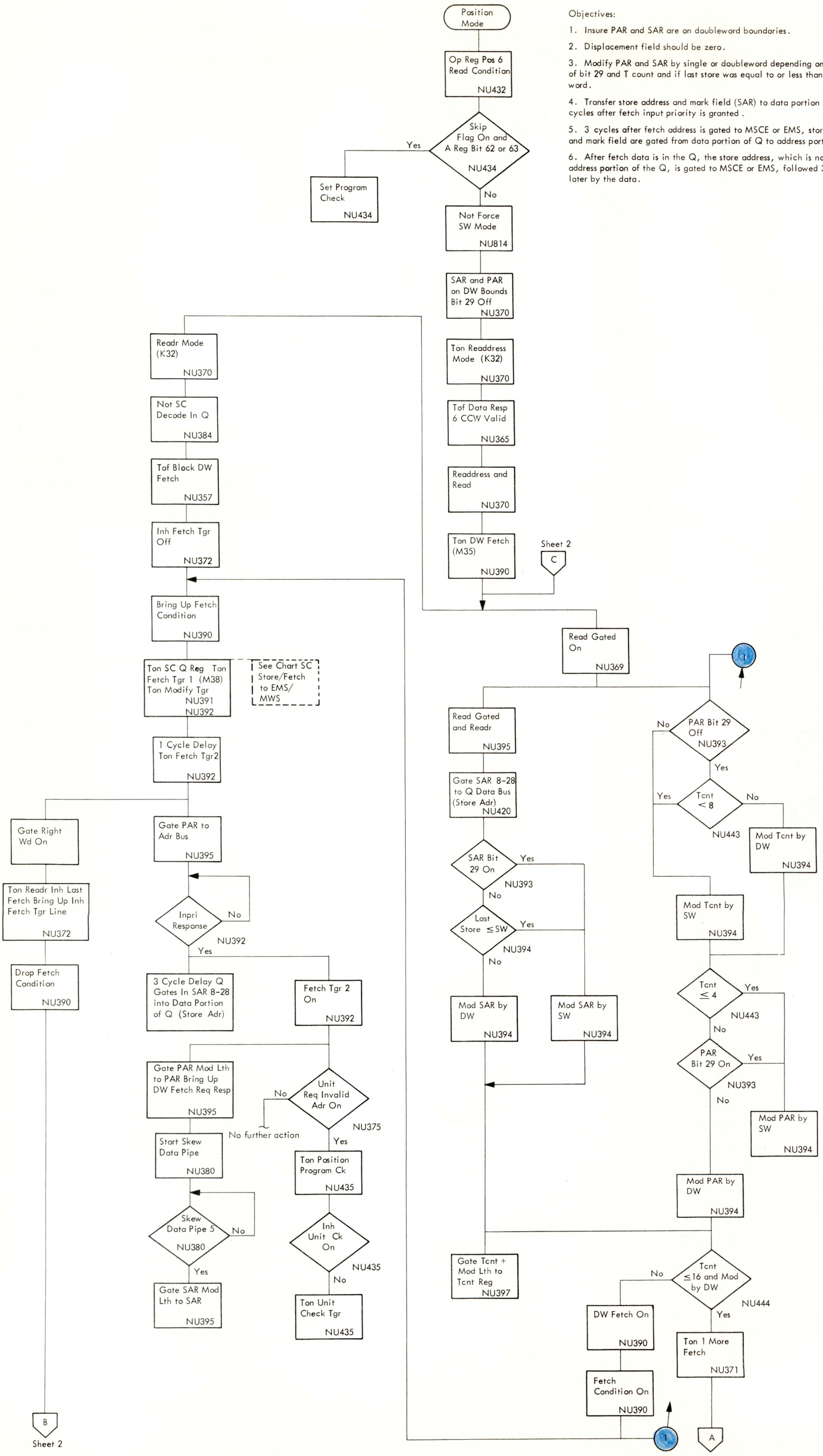


DIAGRAM 5-412. SC CSW STORE AND SC LOGOUT



Objectives:

1. Insure PAR and SAR are on doubleword boundaries.
2. Displacement field should be zero.
3. Modify PAR and SAR by single or doubleword depending on status of bit 29 and T count and if last store was equal to or less than a single word.
4. Transfer store address and mark field (SAR) to data portion of Q 3 cycles after fetch input priority is granted.
5. 3 cycles after fetch address is gated to MSCE or EMS, store address and mark field are gated from data portion of Q to address portion of Q.
6. After fetch data is in the Q, the store address, which is now in the address portion of the Q, is gated to MSCE or EMS, followed 3 cycles later by the data.

DIAGRAM 5-413. SC READ POSITION MODE READDRESS (SHEET 1 OF 2)

Objectives:

1. Bring up readdress last fetch condition.
2. Bring up Op complete.

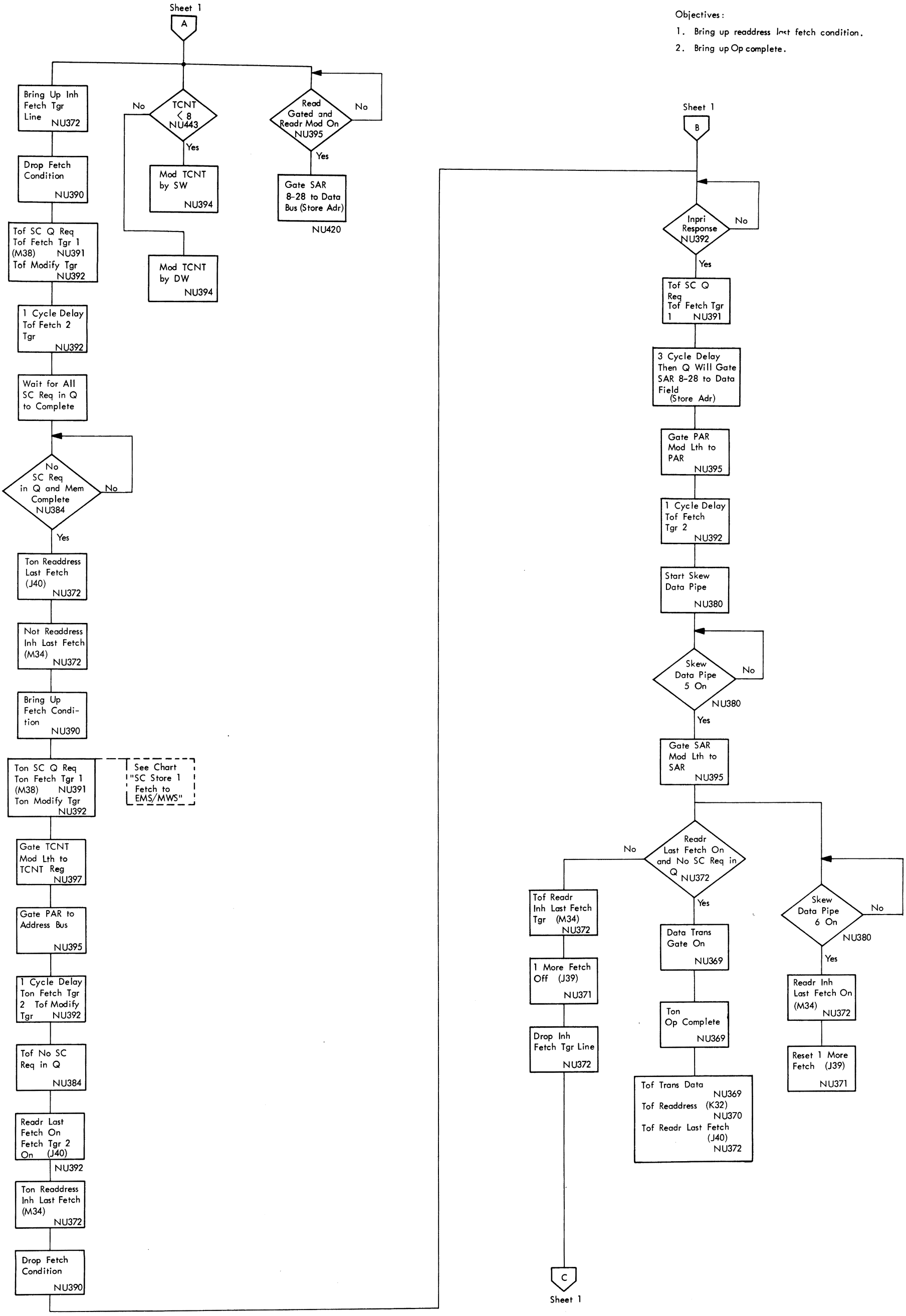


DIAGRAM 5-413. SC READ POSITION MODE READDRESS (SHEET 2 OF 2)

Objectives:

1. Insure PAR and SAR are on doubleword boundaries.
2. Displacement field should be zero.
3. Modify PAR and SAR by single or doubleword depending on status of bit 29 and T count and if last store was equal to or less than a singleword.
4. Transfer store address and mark field (PAR) to data portion of Q 3 cycles after fetch input priority is granted.
5. Three cycles after fetch address is gated to MSCE or EMS, store address and mark field are gated from data portion of the Q to the address portion of the Q.
6. After fetch data is in Q, the store address which is now in the address portion of the Q, is gated to MSCE or EMS, followed 3 cycles later by the data.

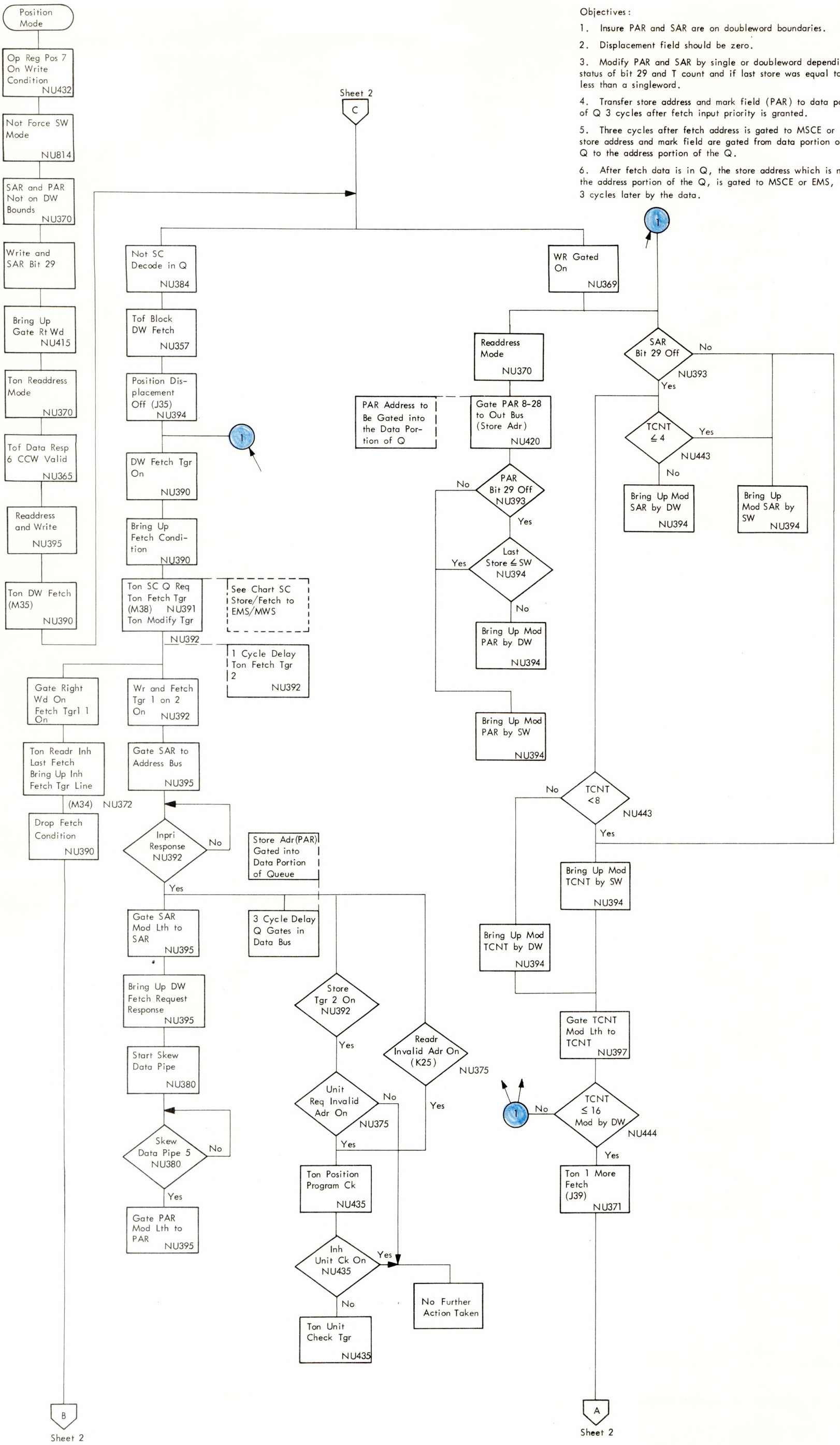


DIAGRAM 5-414. SC WRITE POSITION MODE READDRESS (SHEET 1 OF 2)

Objectives:

1. Bring up readdress last fetch condition.
2. Bring up op complete.

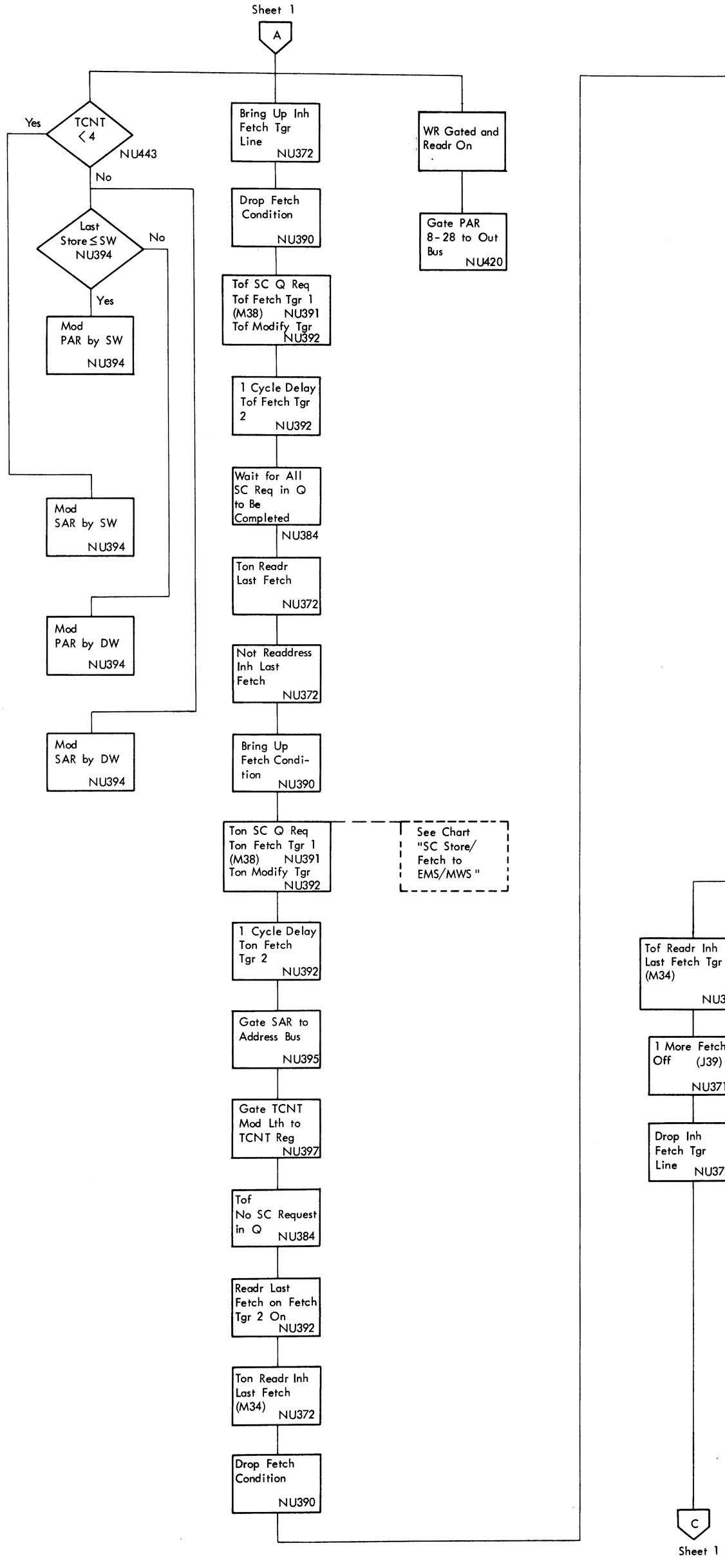
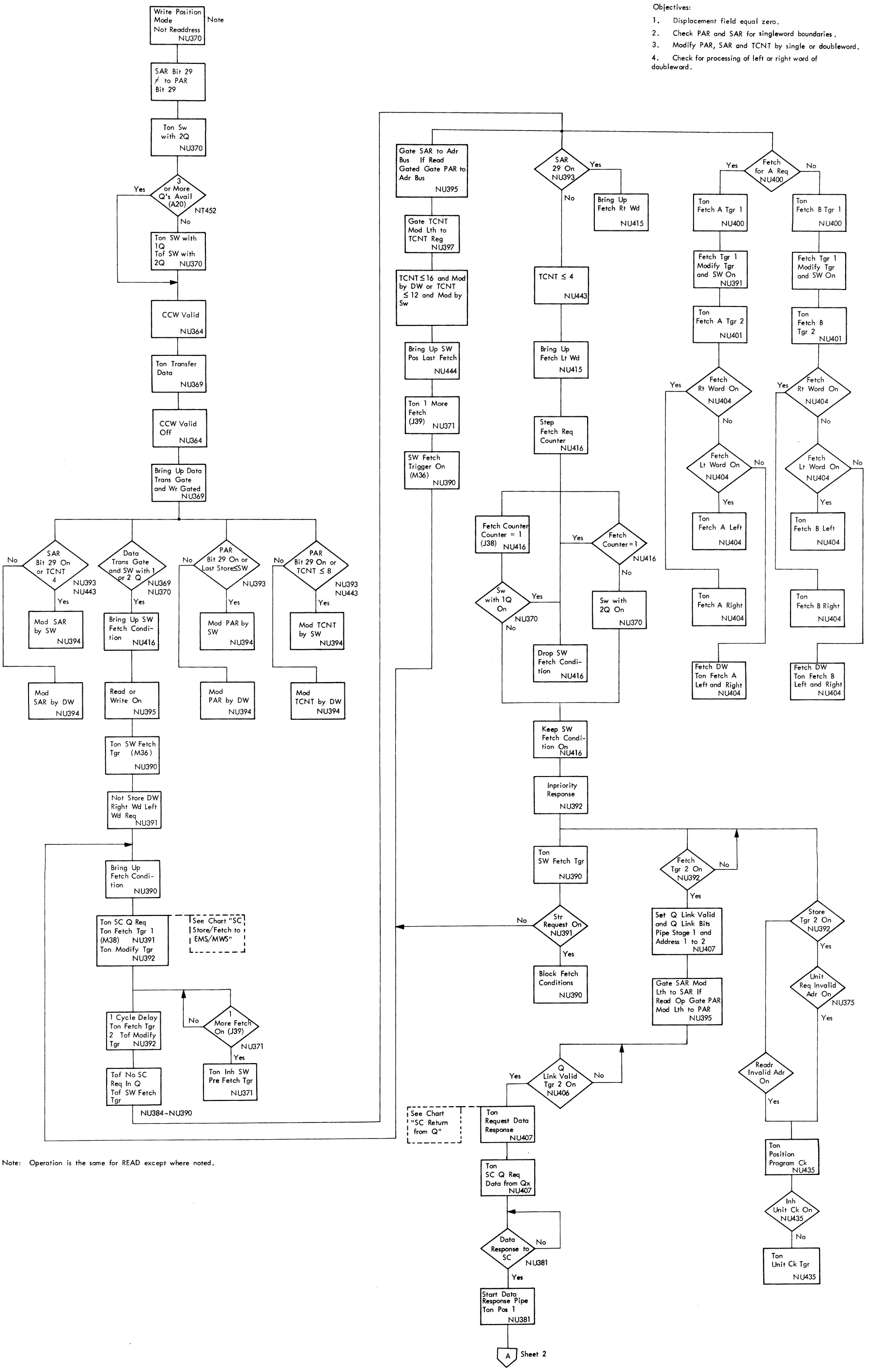


DIAGRAM 5-414. SC WRITE POSITION MODE-READDRESS (SHEET 2 OF 2)

Objectives:

1. Displacement field equal zero.
2. Check PAR and SAR for singleword boundaries.
3. Modify PAR, SAR and TCNT by single or doubleword.
4. Check for processing of left or right word of doubleword.



Note: Operation is the same for READ except where noted.

DIAGRAM 5-415. SC WRITE/READ POSITION MODE - NOT READDRESS (SHEET 1 OF 3)

Objectives:

1. Gate fetched word into A or B register.
2. Bring up store request.

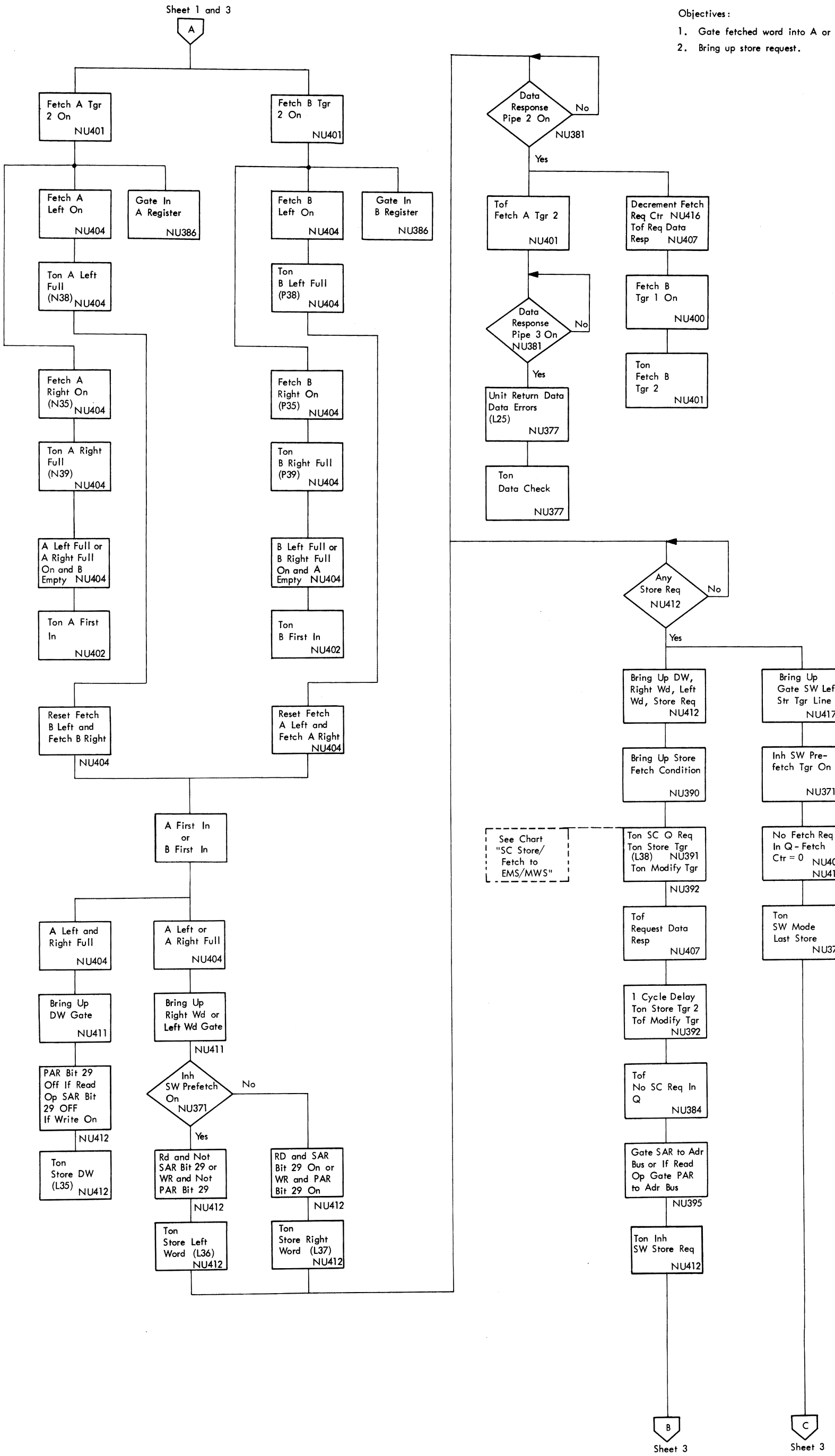


DIAGRAM 5-415. SC WRITE/READ POSITION MODE - NOT READDRESS (SHEET 2 OF 3)

Objectives:

1. Bring up conditions to store the correct portion of the doubleword.

2. If this is last store, bring up op complete. If this is not last store repeat operation.

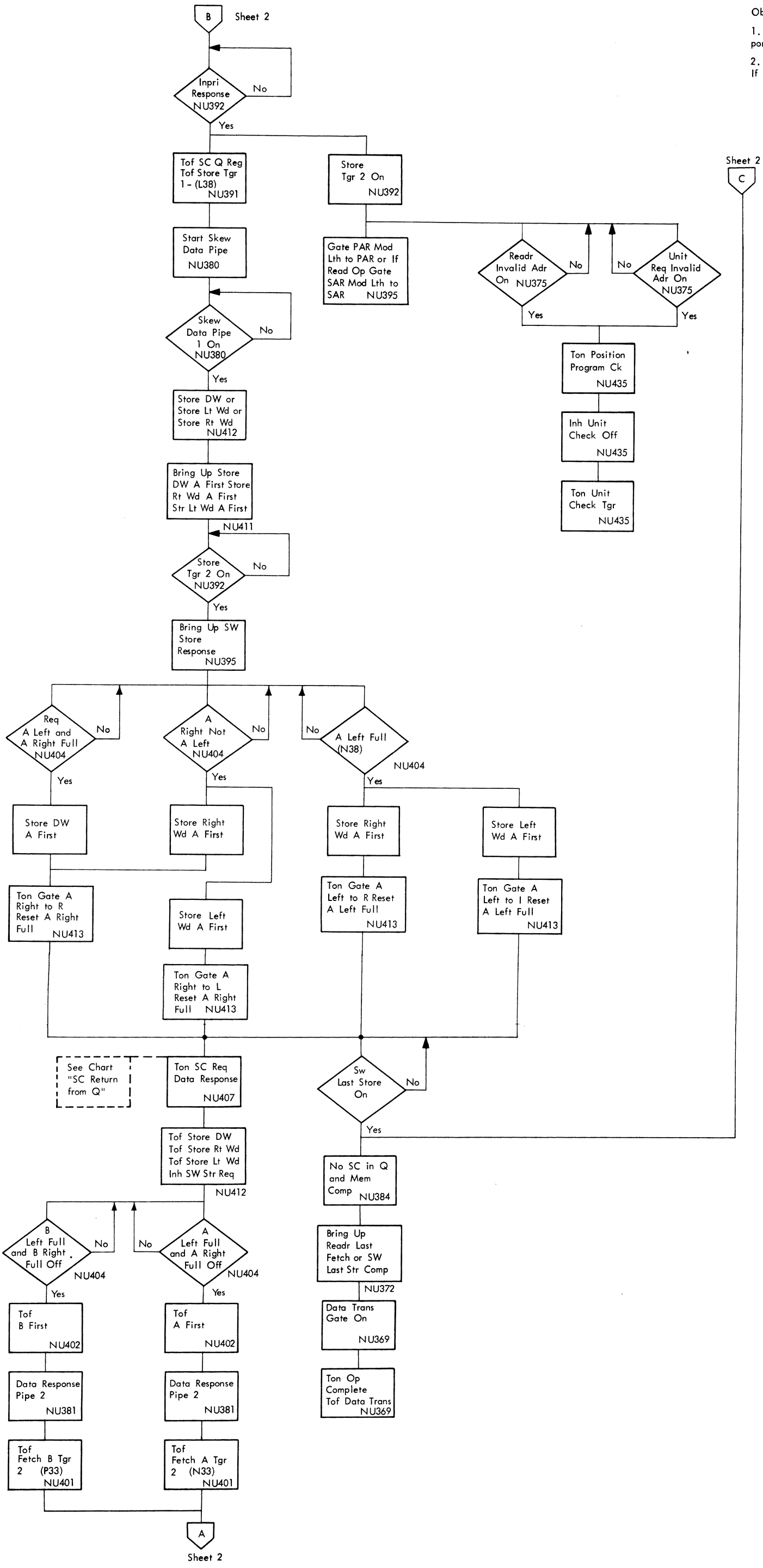
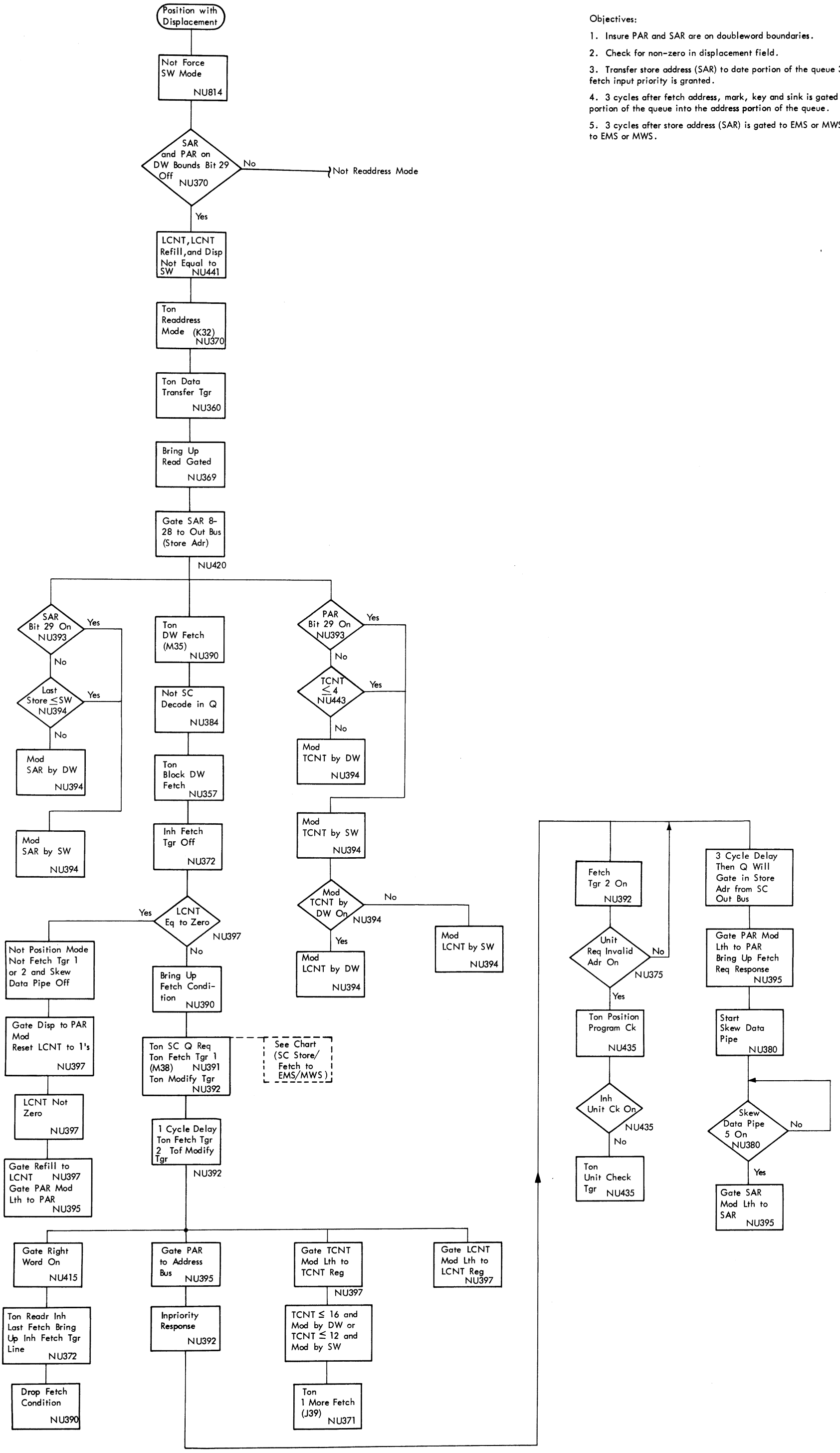


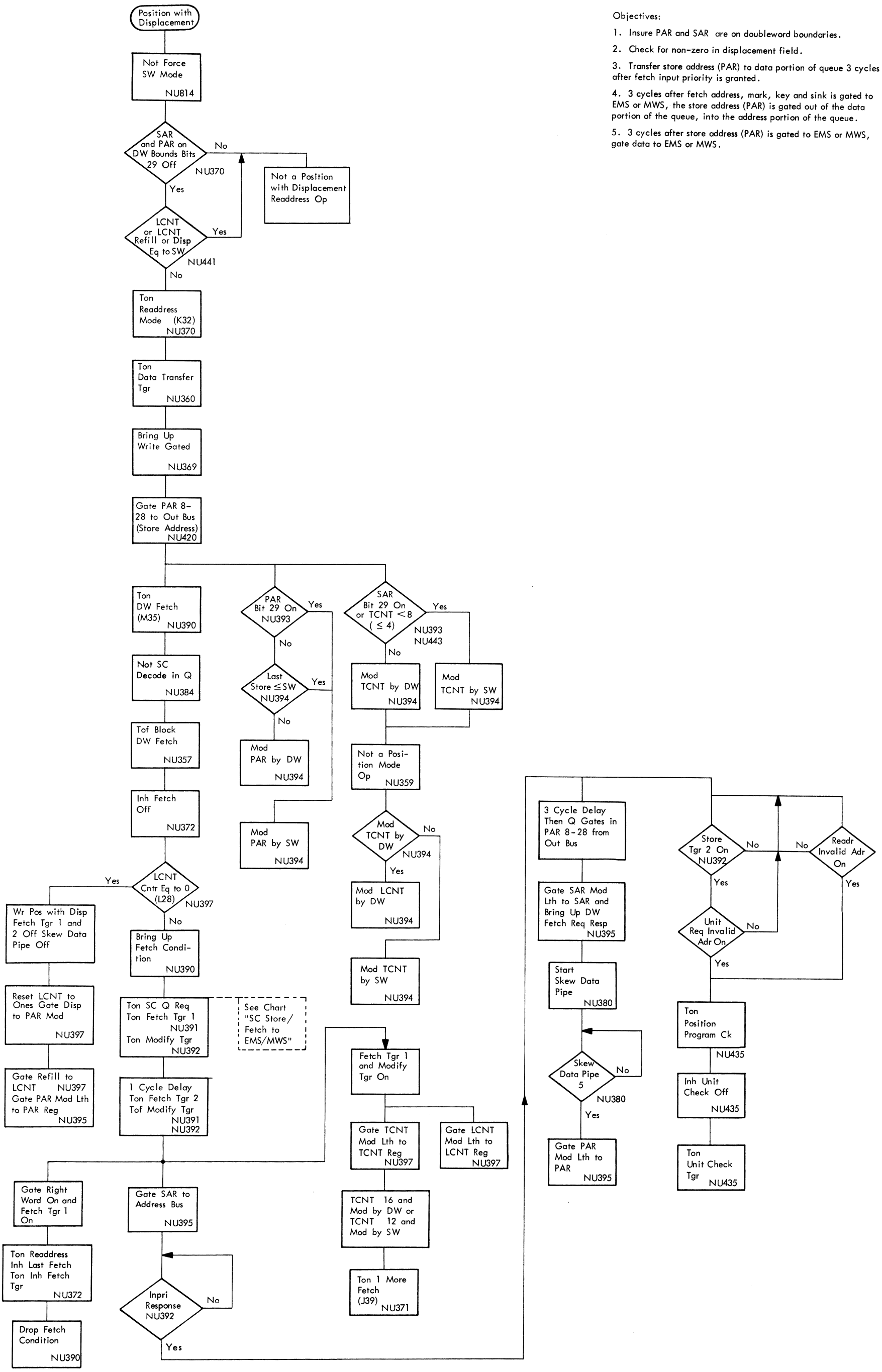
DIAGRAM 5-415. SC WRITE/READ POSITION MODE - NOT READDRESS (SHEET 3 OF 3)



Objectives:

1. Insure PAR and SAR are on doubleword boundaries.
2. Check for non-zero in displacement field.
3. Transfer store address (SAR) to date portion of the queue 3 cycles after fetch input priority is granted.
4. 3 cycles after fetch address, mark, key and sink is gated out of data portion of the queue into the address portion of the queue.
5. 3 cycles after store address (SAR) is gated to EMS or MWS, gate data to EMS or MWS.

DIAGRAM 5-416. SC READ POSITION MODE WITH DISPLACEMENT-READDRESS



Objectives:

1. Insure PAR and SAR are on doubleword boundaries.
2. Check for non-zero in displacement field.
3. Transfer store address (PAR) to data portion of queue 3 cycles after fetch input priority is granted.
4. 3 cycles after fetch address, mark, key and sink is gated to EMS or MWS, the store address (PAR) is gated out of the data portion of the queue, into the address portion of the queue.
5. 3 cycles after store address (PAR) is gated to EMS or MWS, gate data to EMS or MWS.

DIAGRAM 5-417. SC WRITE POSITION MODE WITH DISPLACEMENT-READDRESS

Objectives:

1. Displacement field not zero.
2. Check PAR and SAR for single or doubleword boundaries.
3. Modify PAR and SAR by a single or a doubleword.
4. Check conditions for fetching right or left word of doubleword.

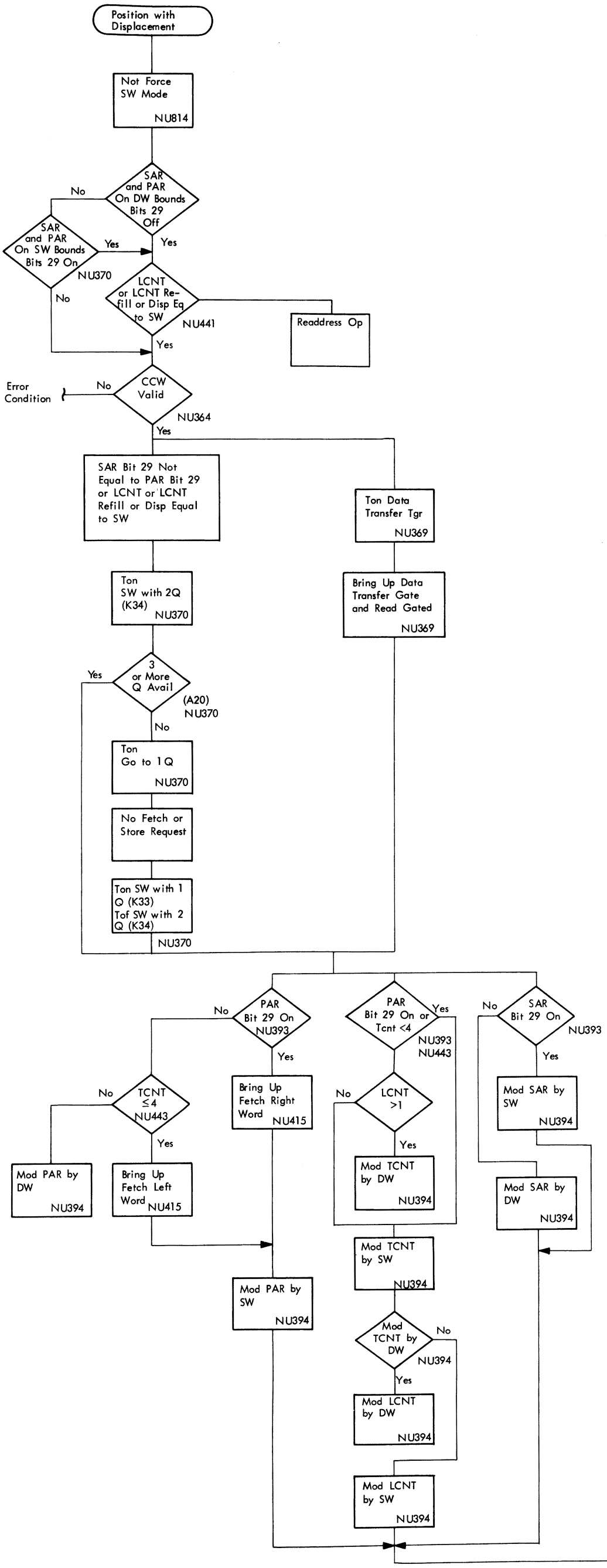


DIAGRAM 5-418. SC READ PM WITH DISPLACEMENT - NOT READDRESS (SHEET 1 OF 3)

Objectives:

1. Bring up conditions to fetch word to A or B register.
2. Bring up conditions to store left word, right word or doubleword.

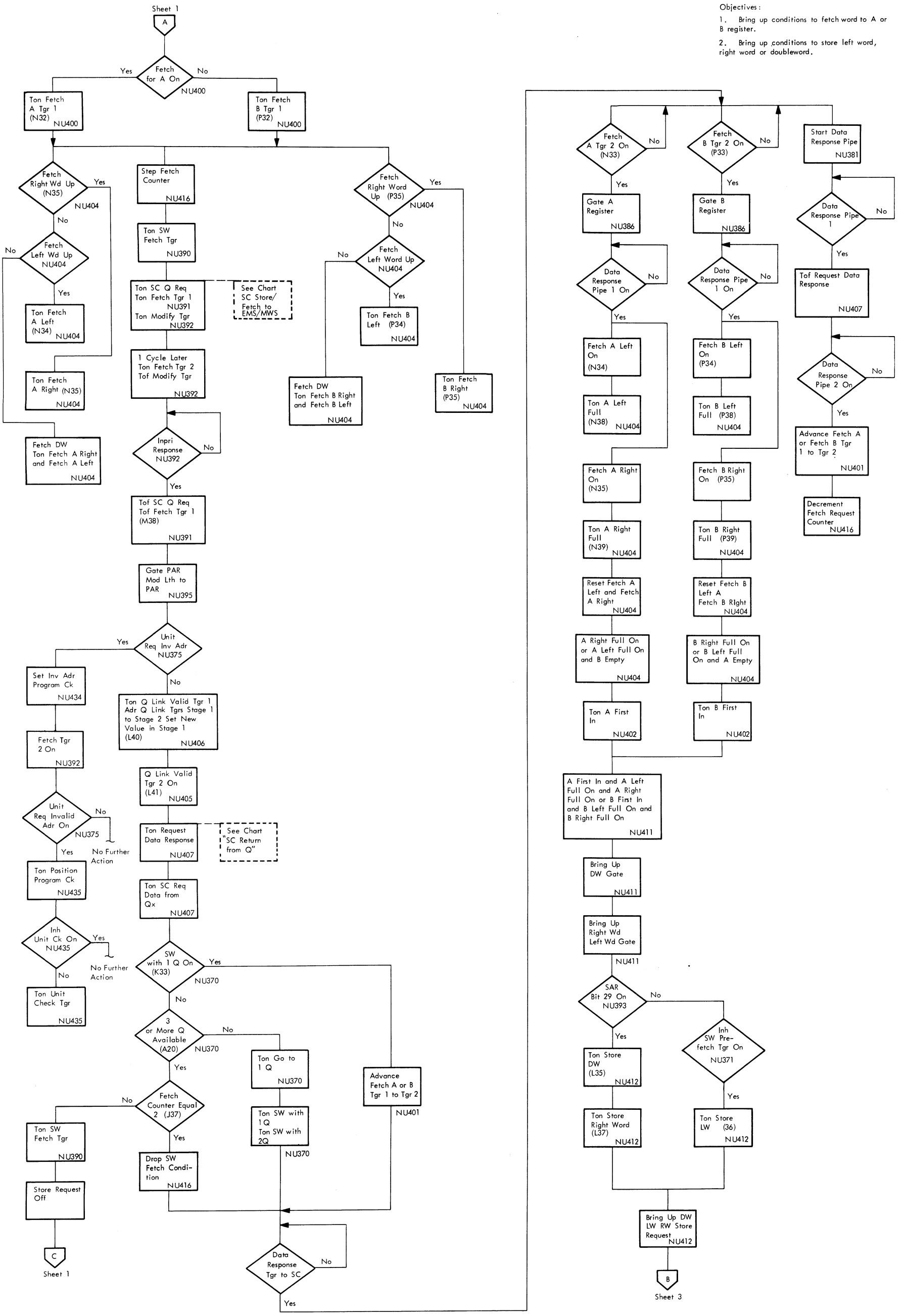


DIAGRAM 5-418. SC READ PM WITH DISPLACEMENT - NOT READDRESS (SHEET 2 OF 3)

Objectives:

1. Bring up store, and gate proper word to storage.
2. If this is last store or fetch bring up op complete.

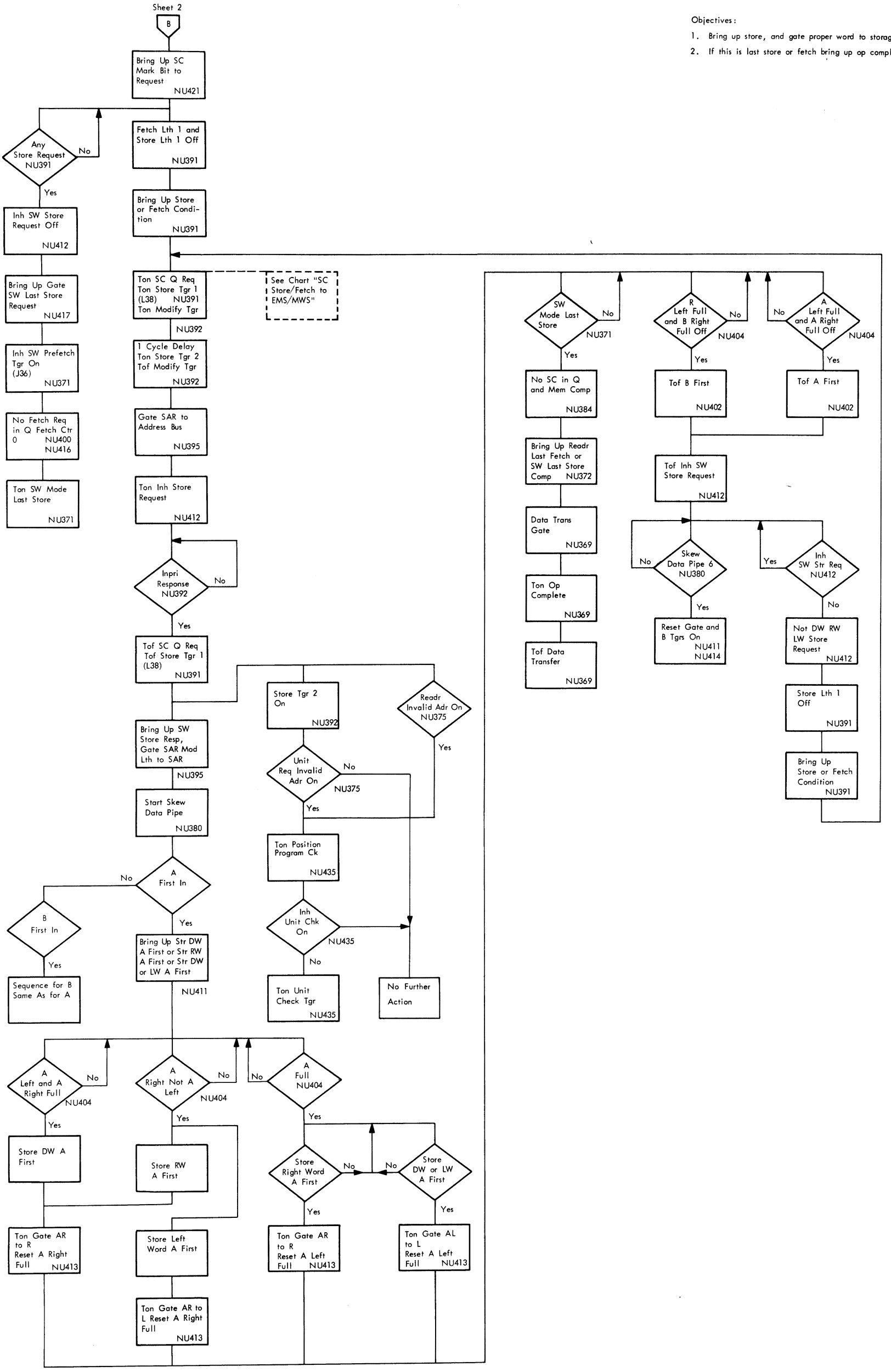


DIAGRAM 5-418. SC READ PM WITH DISPLACEMENT- NOT READDRESS (SHEET 3 OF 3)

Objectives:

1. Displacement field not zero.
2. Check PAR and SAR for single or double word boundaries.
3. Modify PAR and SAR by single or double word.
4. Check conditions for fetching right or left word of double word.

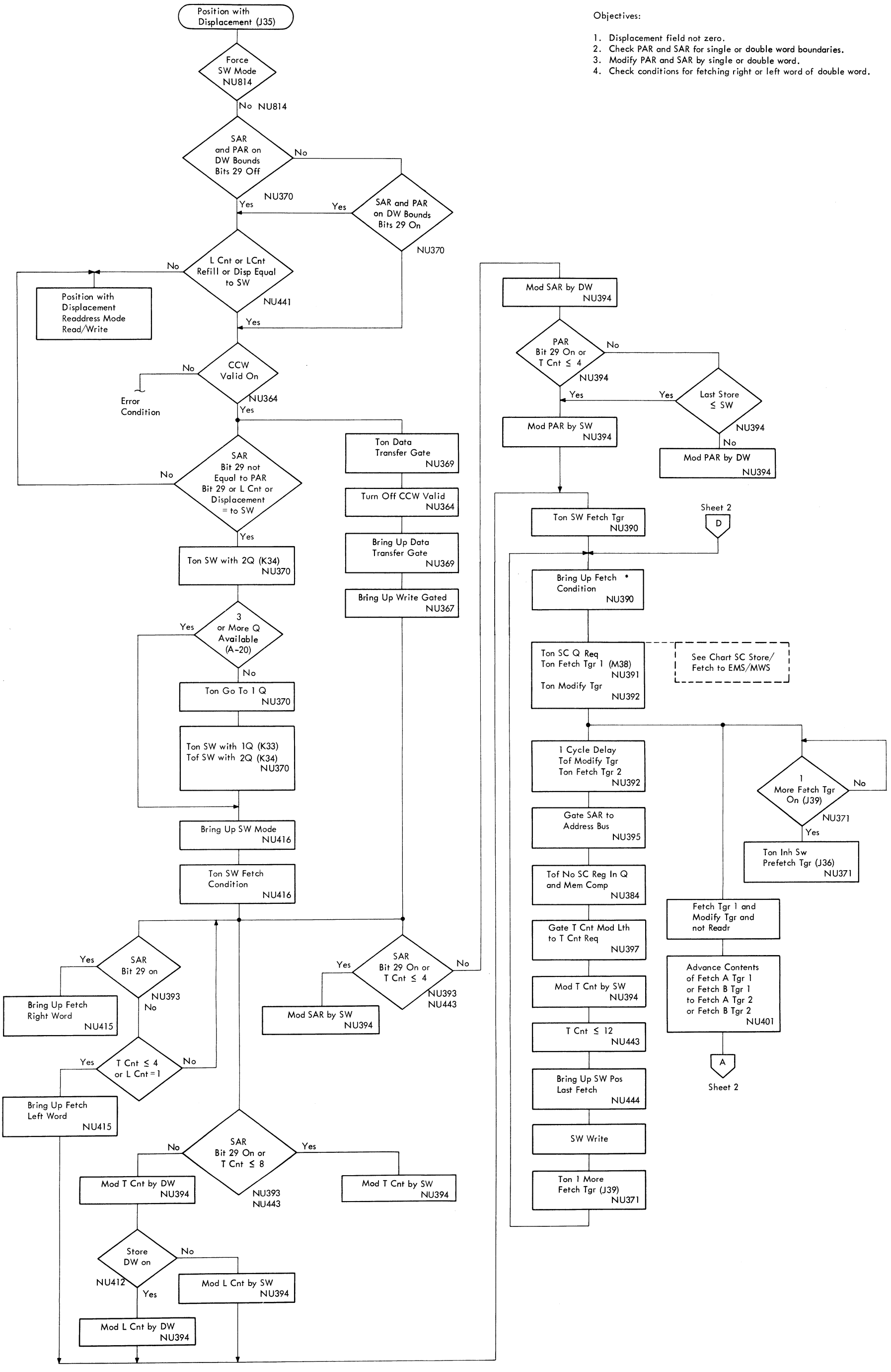


DIAGRAM 5-419. SC WRITE PM WITH DISPLACEMENT - NOT READDRESS (SHEET 1 OF 3)

Objectives:

1. Bring up conditions to fetch word to A or B register.
2. Bring up conditions to store left word, right word or double word.

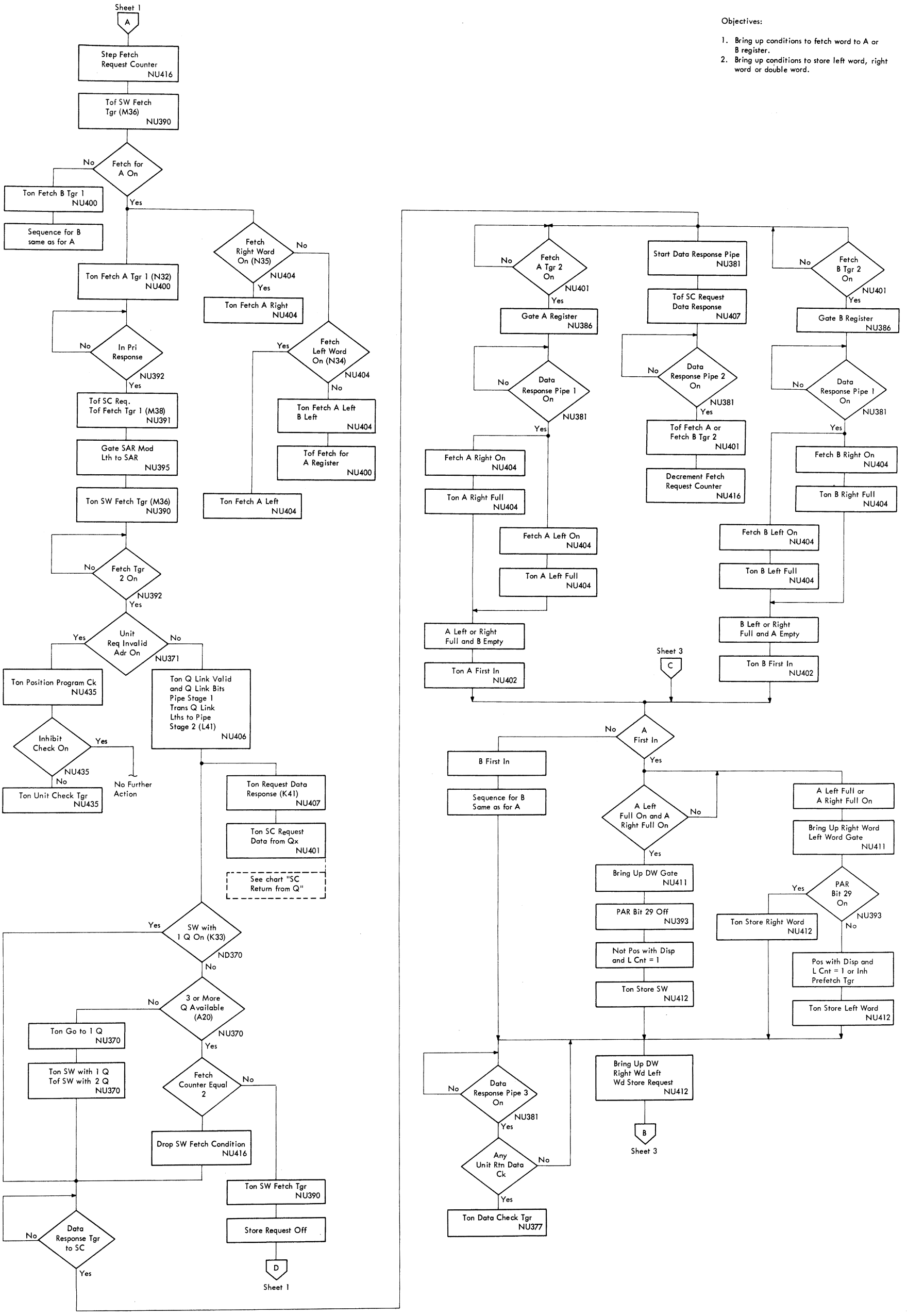


DIAGRAM 5-419. SC WRITE PM WITH DISPLACEMENT - NOT READDRESS (SHEET 2 OF 3)

Objectives:

1. Bring up store, and gate proper word to storage.
2. If this is last store or fetch bring up op complete.

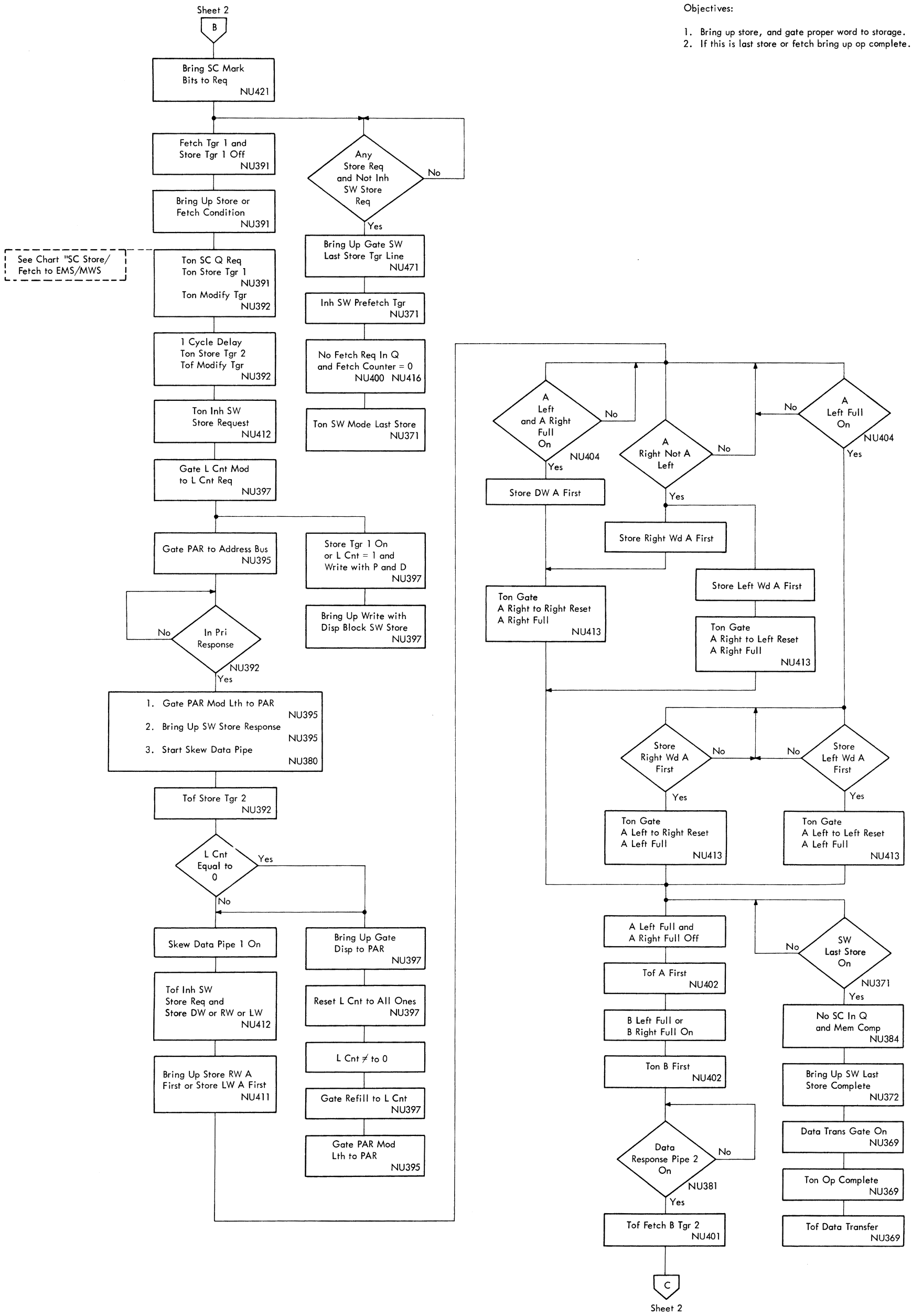


DIAGRAM 5-419. SC WRITE PM WITH DISPLACEMENT - NOT READDRESS (SHEET 3 of 3)

Objectives:

1. To store eight bytes of sense data.

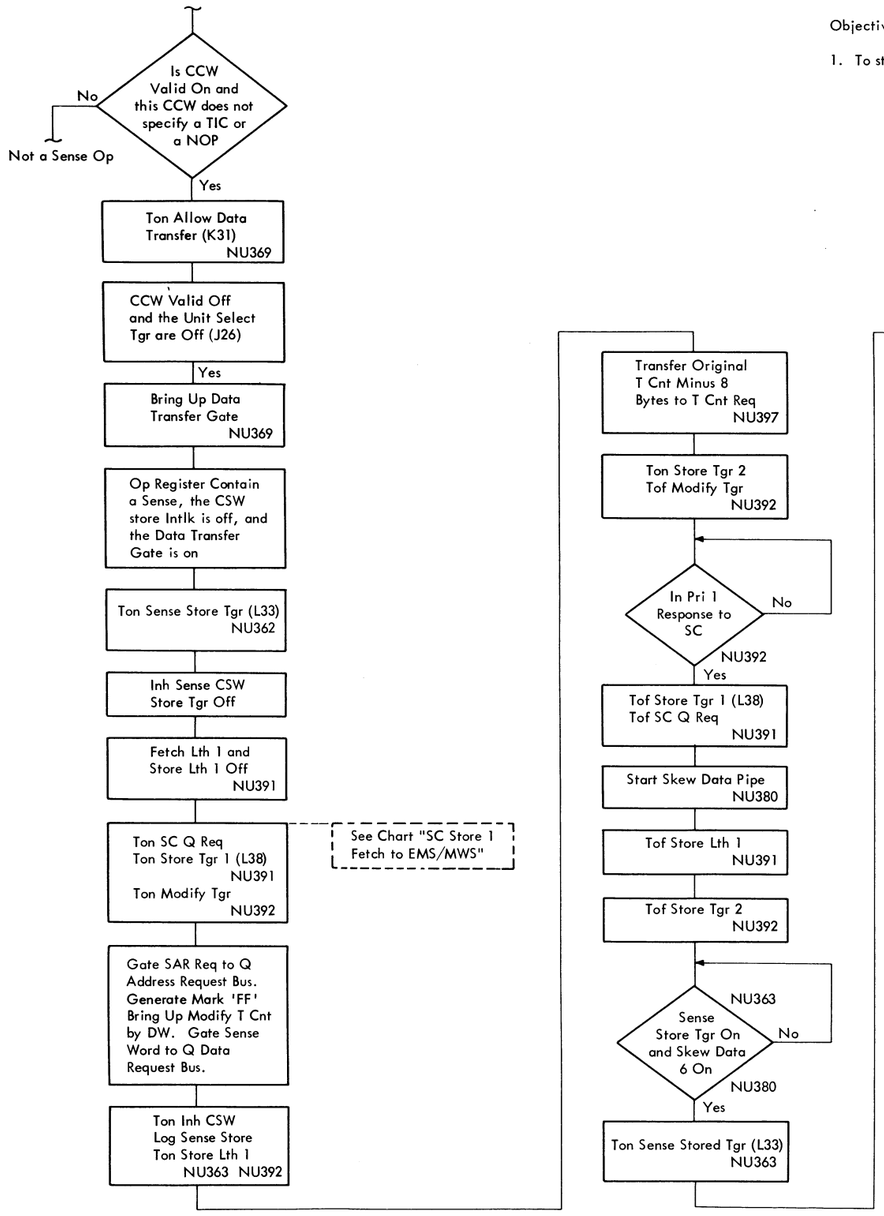


DIAGRAM 5-420. SC SENSE OPERATION

Objectives:

1. To check status of the storage channel.
2. Set the appropriate condition code bits.

Condition Codes

00 - Cmd Accepted
01 - CSW Stored
10 - Busy
11 - Not Available

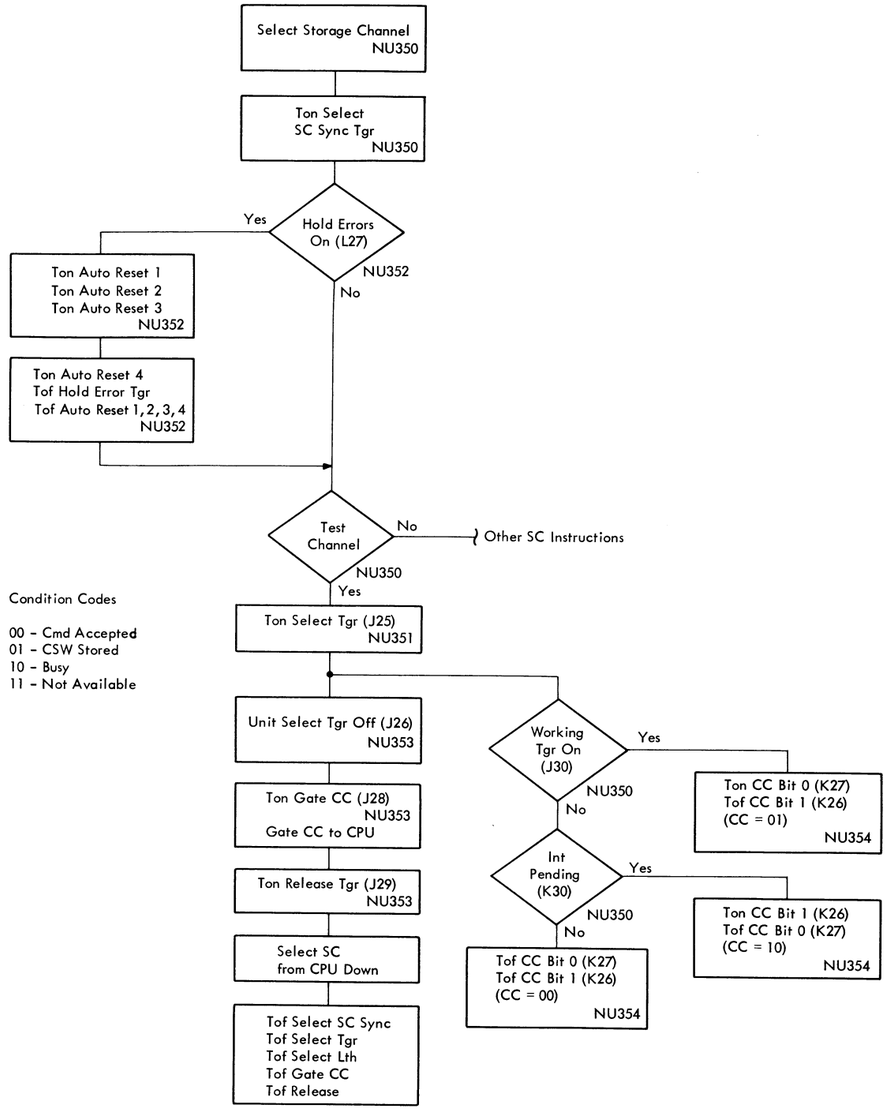


DIAGRAM 5-421. SC TEST CHANNEL

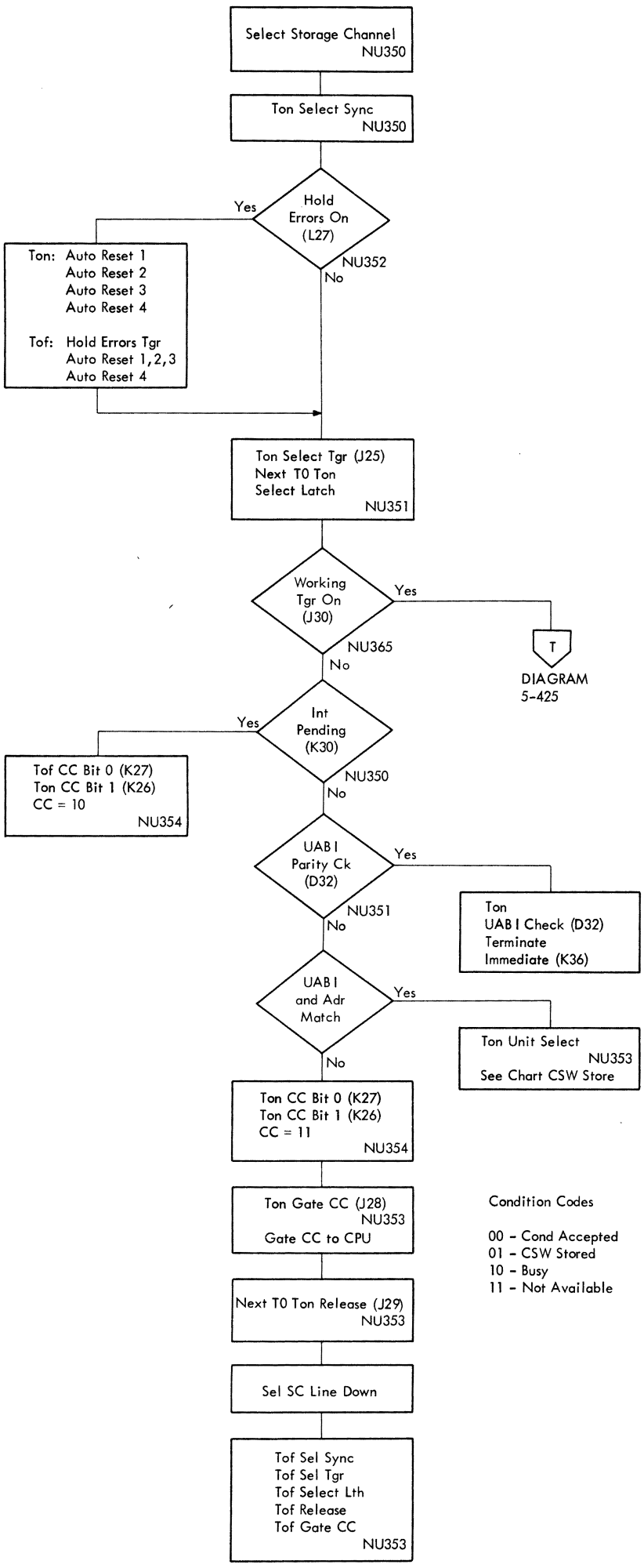


DIAGRAM 5-422. SC HALT I/O - SC NOT WORKING

Objectives

To terminate the current operation and set the appropriate condition code.

Objective:

To gate error returns from EMS and MWS to storage channel.

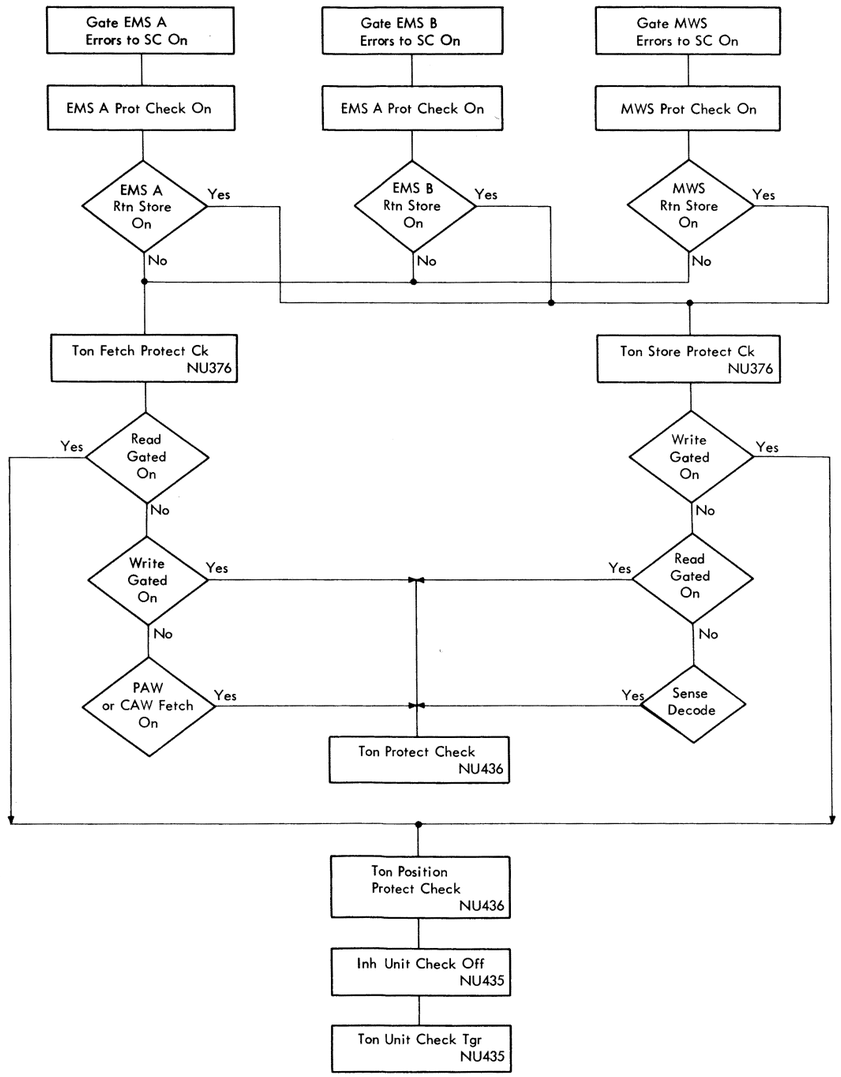


DIAGRAM 5-423. SC PROTECT CHECK AND POSITION PROTECT CHECK

Objectives:

To test for conditions that will turn on program check trigger.

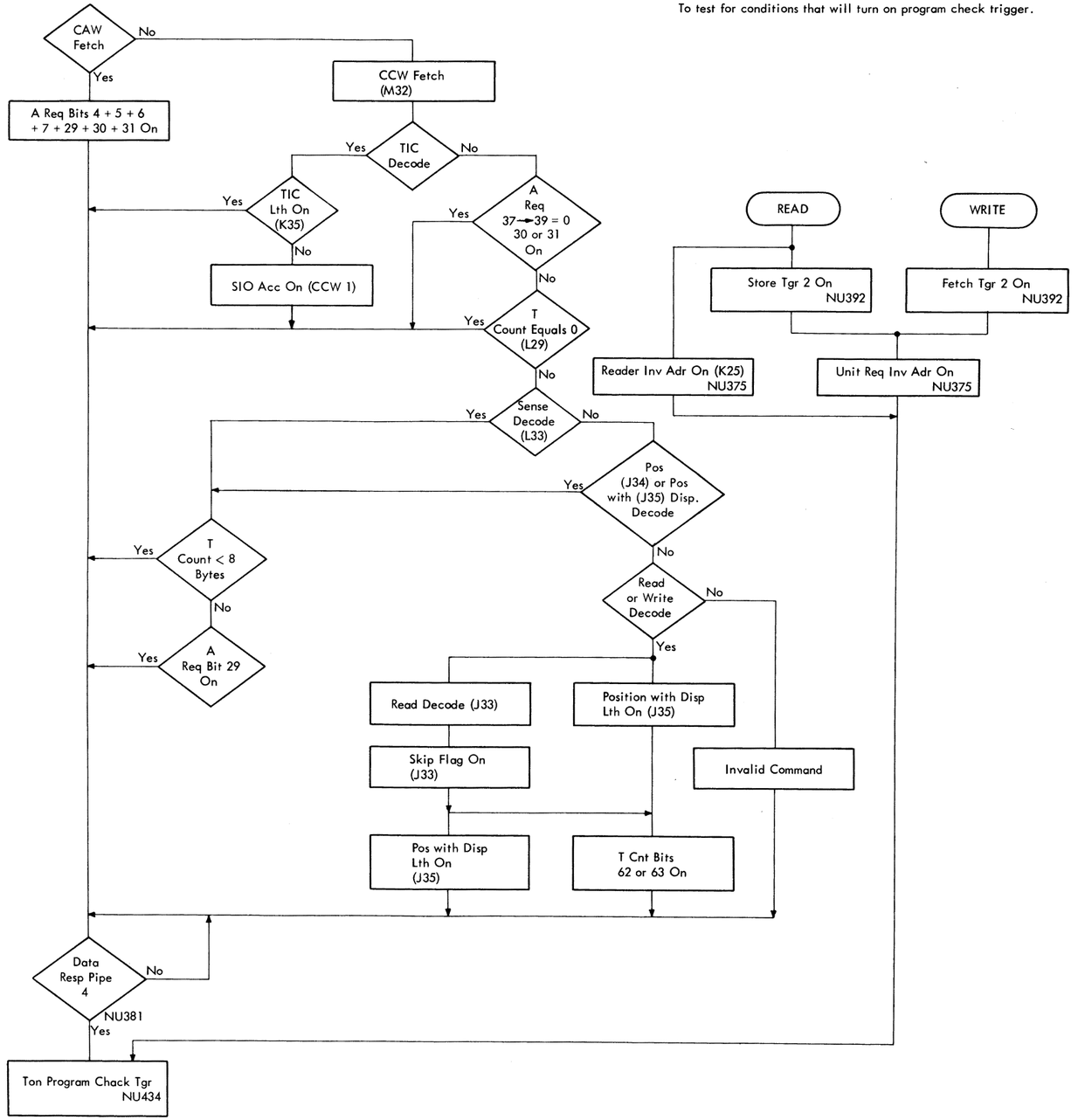
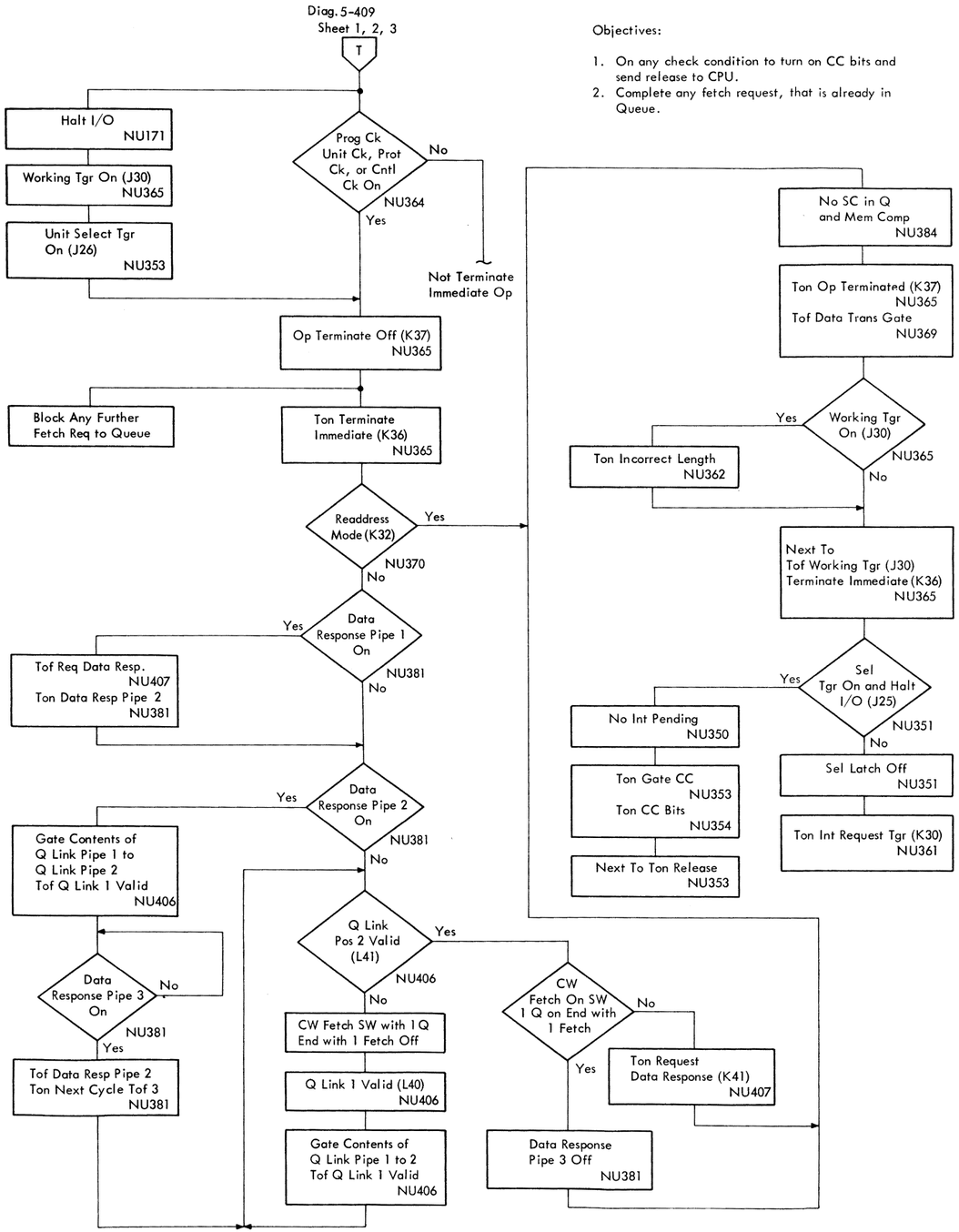


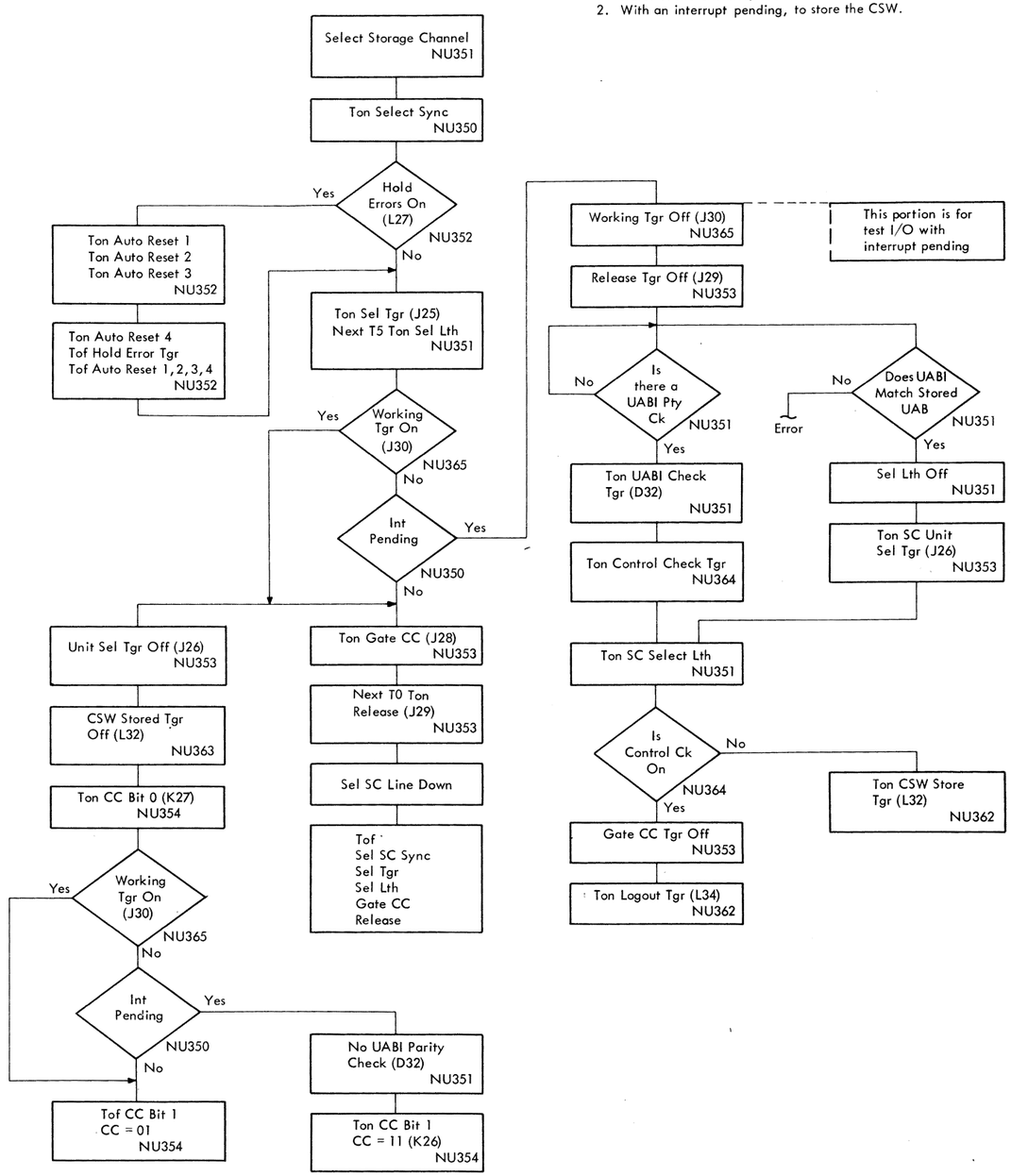
DIAGRAM 5-424. SC PROGRAM CHECK



Objectives:

1. On any check condition to turn on CC bits and send release to CPU.
2. Complete any fetch request, that is already in Queue.

DIAGRAM 5-425. SC TERMINATE IMMEDIATE



Objectives:

1. To set the condition code in PSW to indicate the status of the channel, sub-channel and device.
2. With an interrupt pending, to store the CSW.

DIAGRAM 5-426. SC TEST I/O AND TEST I/O CLEAR INTERRUPT

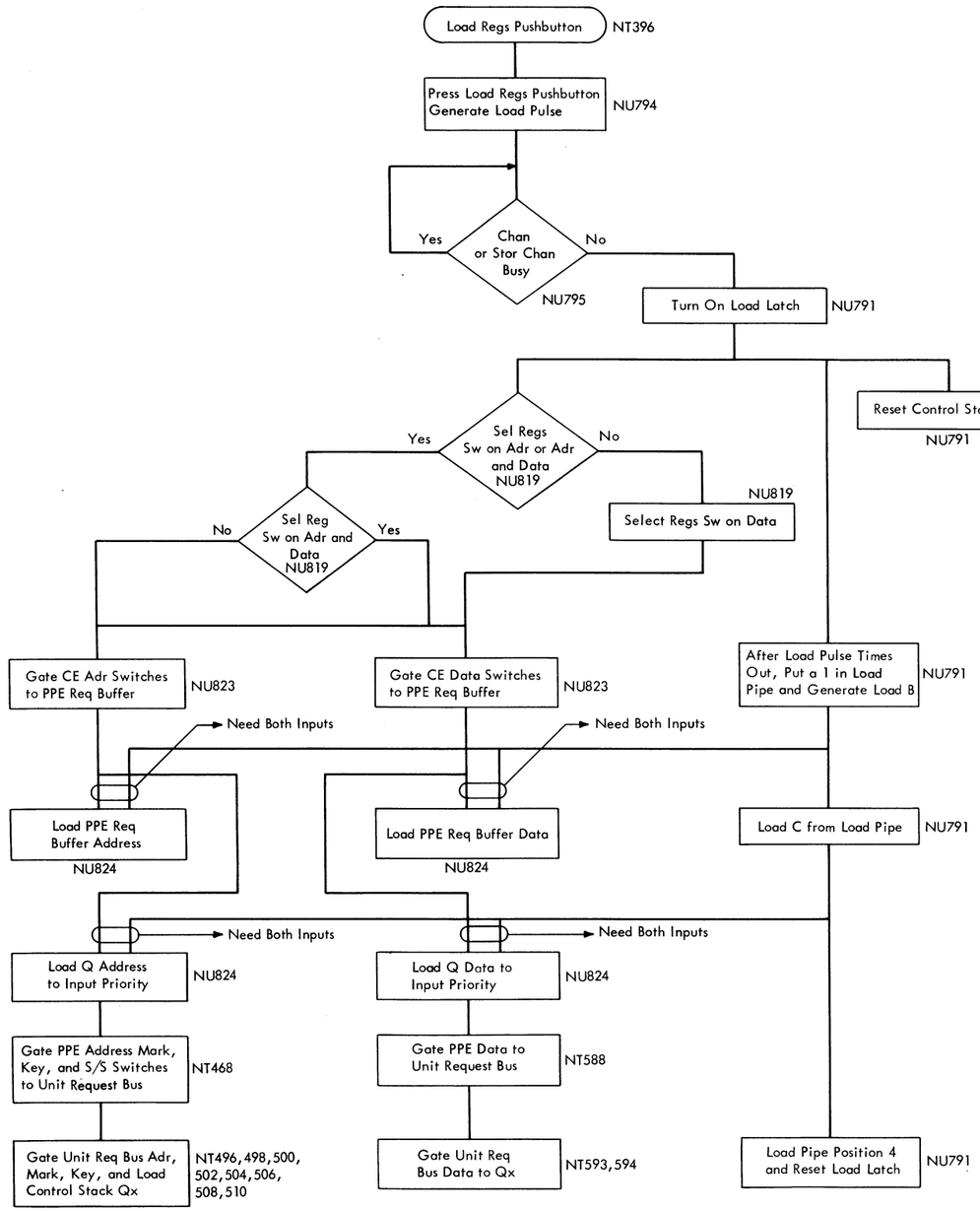
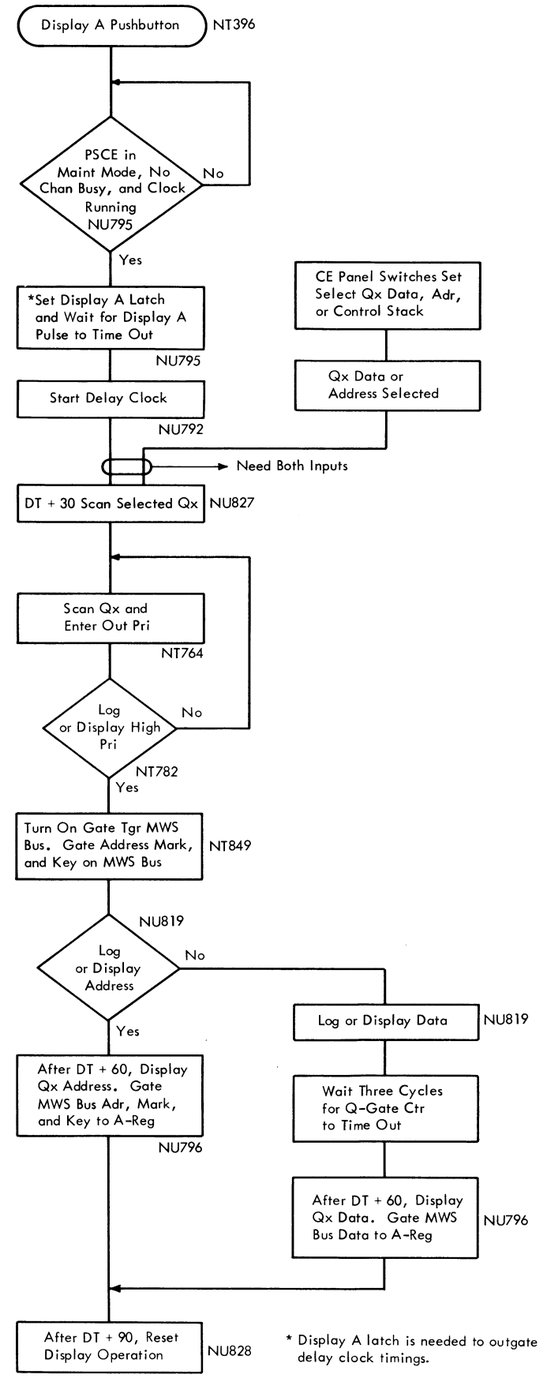
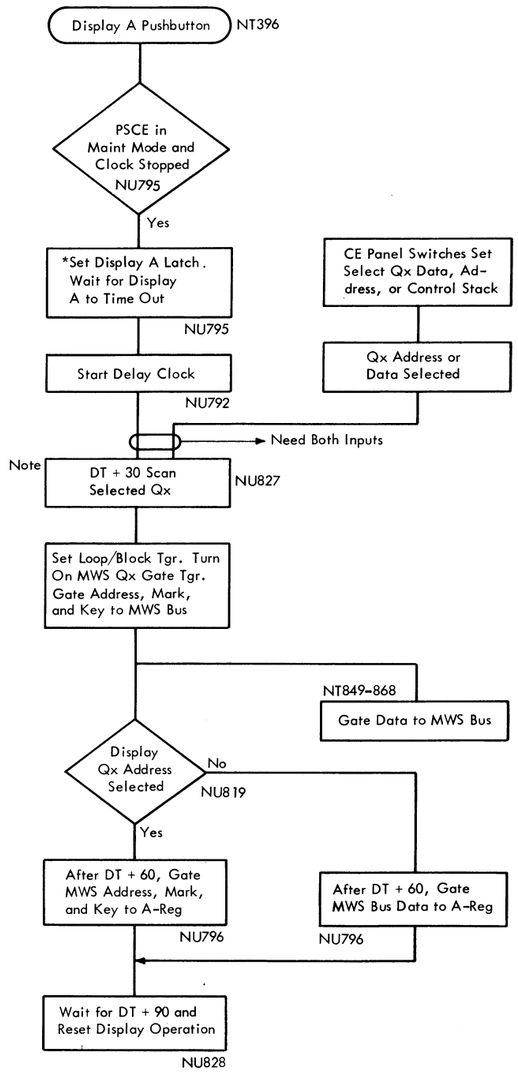


DIAGRAM 5-427. MANUAL LOAD QX DATA OR ADDRESS



* Display A latch is needed to outgate delay clock timings.

DIAGRAM 5-428. MANUAL DISPLAY QX DATA OR ADDRESS (CLOCK RUNNING)



Note: 'Q select' and 'DT + 30' activate scan to activate log or display operation and block the L/B tgr reset. These conditions activate 'set L/B tgr' NU056 and 058. Log out or display enters priority at NU056. Priority is granted on NT782. 'Select Q MWS bus' is activated on NT783. 'Gate Q to MWS bus' is activated on NT849.

* Display A latch is needed to outgate delay clock timings.

DIAGRAM 5-429. MANUAL DISPLAY QX DATA OR ADDRESS (CLOCK STOPPED)

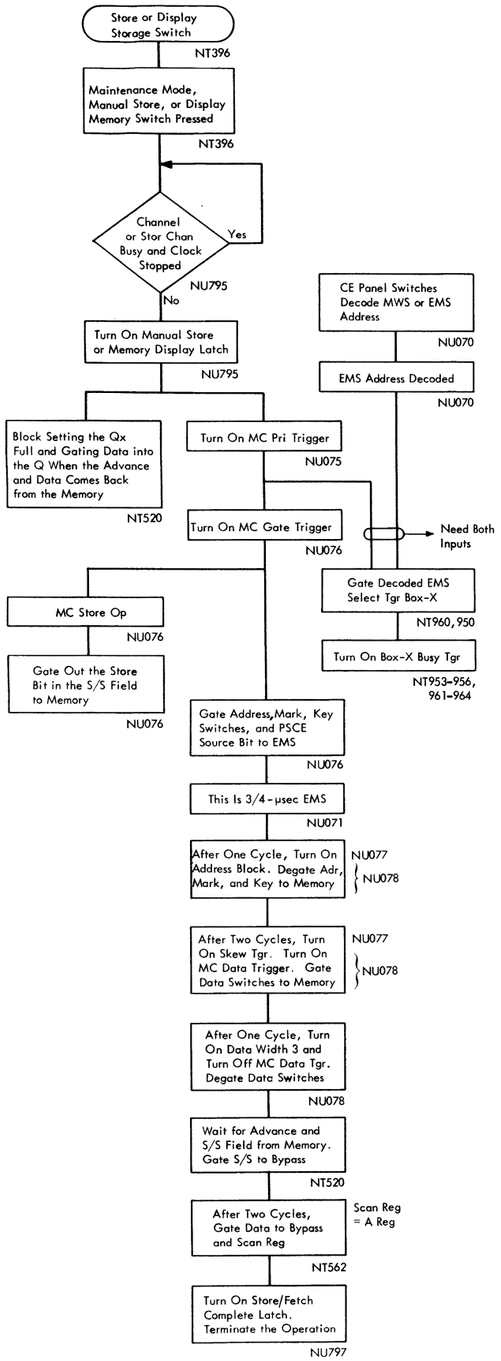


DIAGRAM 5-430. MANUAL STORE OR DISPLAY EMS

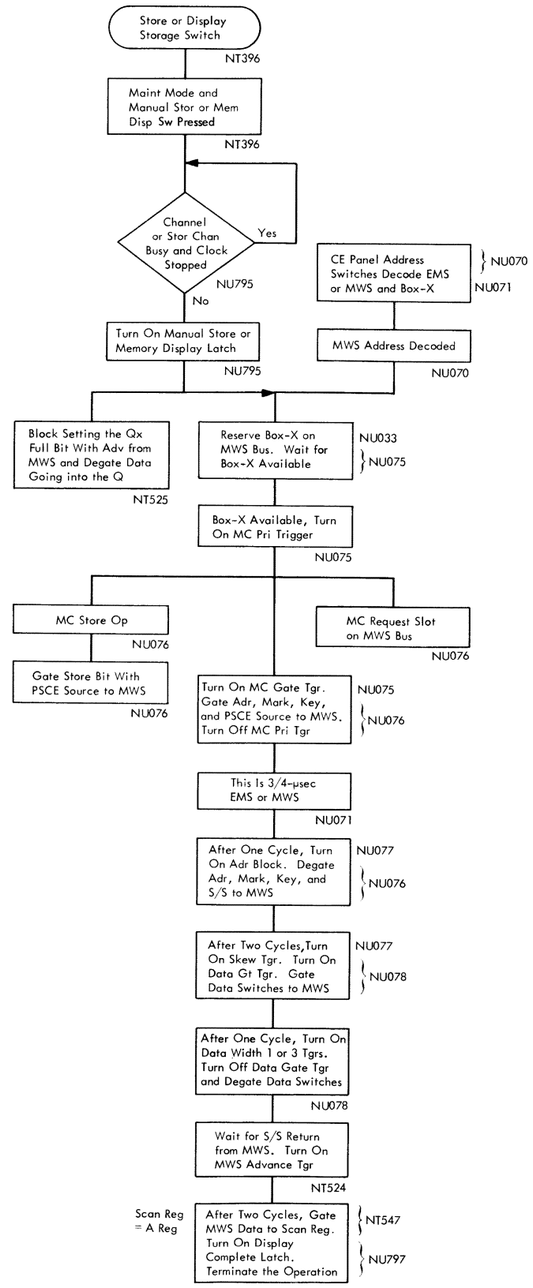


DIAGRAM 5-431. MANUAL STORE OR DISPLAY MWS

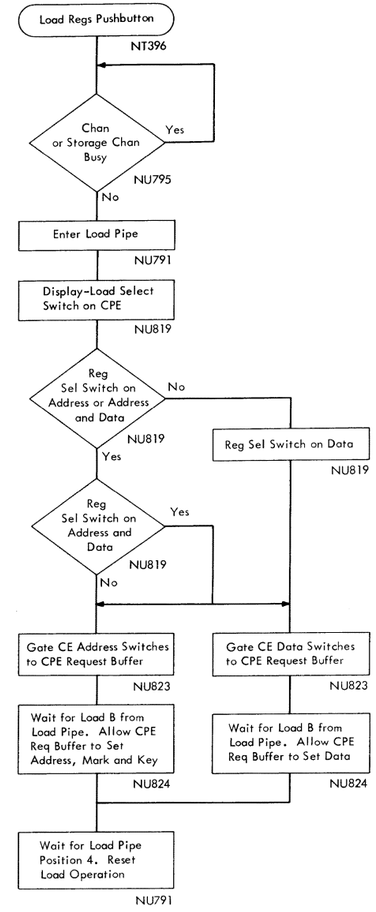


DIAGRAM 5-432. MANUAL LOAD CPE REQUEST BUFFER ADDRESS AND DATA

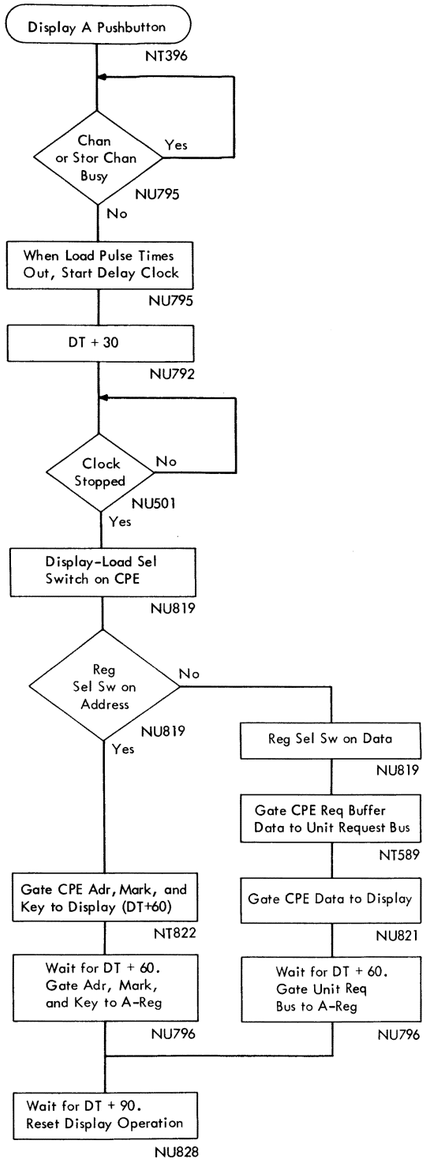


DIAGRAM 5-433. MANUAL DISPLAY CPE REQUEST BUFFER ADDRESS AND DATA

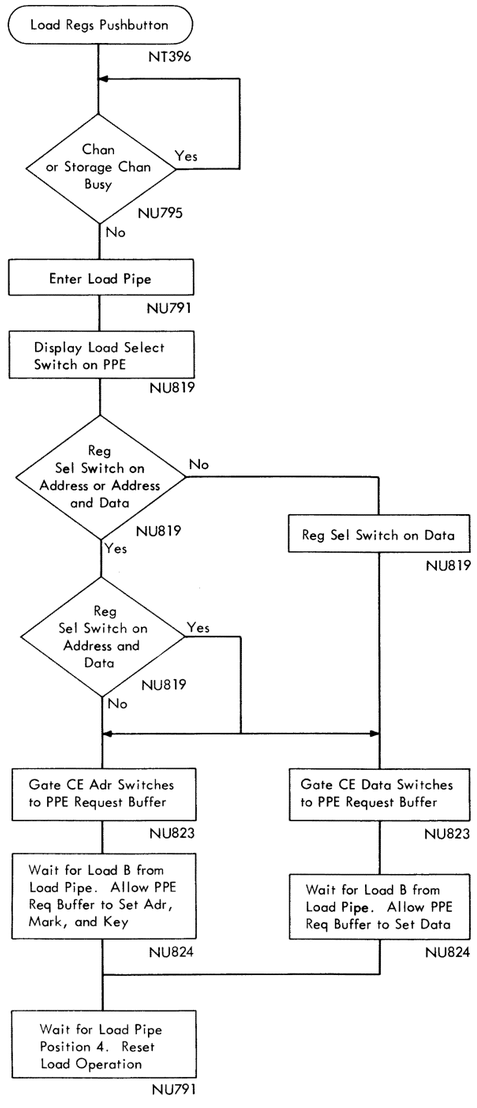


DIAGRAM 5-434. MANUAL LOAD PPE REQUEST BUFFER ADDRESS AND DATA

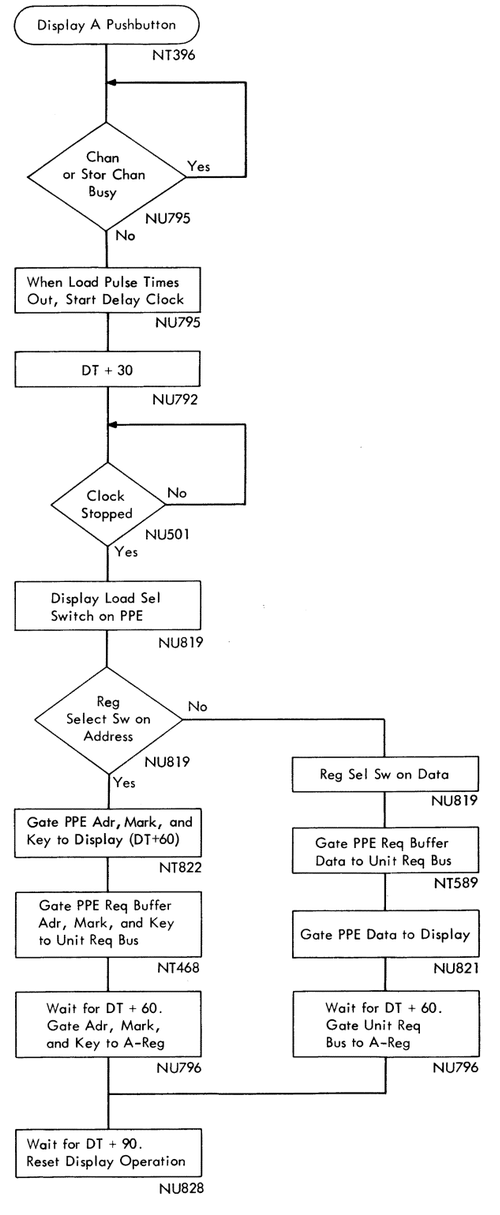


DIAGRAM 5-435. MANUAL DISPLAY PPE REQUEST BUFFER ADDRESS AND DATA

Input Priority, Q Status and Priority Control

Functional Units

Link Pipe for Unit Request Bus Skew Data - NT590-NT592
A three-bit, three-cycle shifter that pipelines a link (Q address). This pipeline works in conjunction with the unit pipe described below. Whenever a unit gains Q input priority for a store, the assigned queue is coded and entered into this pipeline. Three cycles later, the output of this pipeline determines the queue into which data will be gated.

Unit Pipe For Unit Request Bus Skew Data - NT586-588
A three-bit, three-cycle shifter that pipelines a coded unit identity. Whenever a unit (CCC2, CCC1 or 3, PPE, CPE, SC) gains queue input priority for a store, a code for that unit is entered into this pipeline and three cycles later, the output of the pipeline determines whose data is to be gated to the queue.

Control Triggers

Two pools of queues are maintained by input priority: an available pool and a reserved pool. When a queue is reserved, it transfers from the available pool to the reserved pool. Conversely, when a queue is released, it transfers from the reserved pool to the available pool. A queue is available if it is not disabled, not reserved, and not busy.

Any CCC Priority - NT456
Any CCC interface has gained queue input priority.

Assign Qx from Bottom - NT443-445
Qx is the next queue to be assigned from the available pool to a CPE request.

Assign Qx from Reserved - NT435-437
Qx is the next queue to be assigned from the reserved pool to a channel request.

Assign Qx from Top - NT440-442
Qx is the next queue to be assigned from the available pool to a PPE or storage channel request.

CCC1 or 3 Priority - NT455
CCC interfaces 1 or 3 have gained Q input priority.

CCC2 Priority - NT454
CCC interface 2 has gained Q input priority.

CPE Priority - NT460
CPE has gained Q input priority.

Manual Load Q Address - NT468
Controls Q input address gating when manually loading a queue from the CE panel.

Manual Load Q Data - NT593
Controls Q input data gating when manually loading a queue from the CE panel.

MCW Qx Disable - NT420-423
Provides a synchronous input to 'Qx disabled' trigger from an active MCW.

One or More Q Available - NT450
One or more queues occupy the available pool.

One Q Available - NT450
Exactly one queue occupies the available pool.

PPE or SC Priority - NT459
PPE or storage channel has gained Q input priority.

PPE Priority - NT457
PPE has gained Q input priority.

Qx Busy - NT424-431
Qx contains a request in process.

Qx Disabled - NT420-423
Prevents Qx from entering input and output priority.

Qx Reserved - NT424-431
Qx is reserved for channel requests (but not storage channel).

Release Priority - NT466
CCC release of a reserved queue has gained priority.

Release Qx - NT432-434
Qx is the next queue to be released from the reserved pool.

Reserve Priority - NT466
CCC request to reserve a queue has gained input priority.

SC Priority - NT458
Storage channel has gained Q input priority.

Store Conflict Enabled - NT461
Store conflict is enabled on the Q unit request data bus. A store conflict is defined as the concurrence of a CPE store request and a CCC or PPE store request.

Tag Block - NT462
When EMS is 2.5 usec, only one set tag operation is allowed to occupy the queue at one time. The tag block trigger prevents PPE or CPE from gaining input priority when a set tag occupies the queue and EMS is 2.5 usec.

Three Q Available - NT452
Exactly three queues occupy the available pool.

Two or More Q Available - NT451
Two or more queues occupy the available pool.

Two Q Available - NT451
Exactly two queues occupy the available pool.

Input Priority, Storage Returns

Functional Units

EMS-A Return S/S Pipe - NT554-558
A 12-bit, 2-cycle shifter that pipelines source/sink and check signals that return from EMS-A.

EMS-B Return S/S Pipe - NT566-570
A 12-bit, 2-cycle shifter that pipelines source/sink and check signals that return from EMS-B.

MWS Return S/S Pipe - NT542-546
An 11-bit, 2-cycle shifter that pipelines source/sink and check signals that return from MWS.

SPM Return S/S Register - NT529-530
A nine-position register that holds the source/sink returning from the storage protect memory on set or insert tag instructions to EMS.

Control Triggers

Block 2.5 Simulated EMS Advance - NT521
When EMS is 2.5 usec and being simulated, this trigger prevents the EMS advance triggers from turning on for more than one cycle per memory select.

EMS-A Advance Trigger - NT520
Defines the cycle during which the EMS-A source/sink return bus is valid.

EMS-B Advance Trigger - NT521
Defines the cycle during which the EMS-B Source/sink return bus is valid.

Gate EMS-A Data to Bypass - NT559
Gates EMS-A data to the Q bypass for memory display and EMS-A access 540 returns to CPE.

Gate EMS-A S/S to Bypass - NT557
Gates EMS-A return source/sink to the Q bypass for memory display and EMS-A access 540 returns to CPE.

Gate EMS-B Data to Bypass - NT571
Gates EMS-B data to the Q bypass for memory display and EMS-B access 540 returns to CPE.

Gate EMS-B S/S to Bypass - NT569
Gates EMS-B return source/sink to the Q bypass for memory display and EMS-B access 540 returns to CPE.

MWS Advance Trigger - NT524
Defines the cycle during which the MWS source/sink return bus is valid for PSCE.

SPM Advance Trigger - NT522
Defines the cycle during which the EMS storage protect memory source/sink return bus is valid.

2.5 EMS-A Advance - NT520
When EMS is 2.5 usec, this latch delays the turn-on of the EMS-A advance trigger until the advance signal falls.

2.5 Key Advance Latch - NT522
When EMS is 2.5 usec, this latch delays the turn-on of the SPM advance trigger until the key advance signal falls.

Input Priority, CPE to EMS

Functional Units

Backup Buffer Data Skew Pipe Position 1-3 - NT482
A one-bit, three-cycle shifter that pipelines CPE backup buffer store conditions in order to hold the incoming skewed data at the proper time.

CPE Backup Buffer - Sink Address and Instruction - NT469-472
A 12-bit register that receives the following bits from MSCE and presents these bits to the CPE request buffer:

Sink Address 1-5
Store
Sink Address Parity
Tag
Test and Set
Transpose
Reject (2)

CPE-EMS Advance Pipe Position 1-8 - NT404-407, 491
Predicts CPE-EMS not 540 advances by extending the CPE-EMS pipe to 27-32 cycles.

CPE-EMS Counter Bits 4, 2, 1 - NT487-488
Contains the number of CPE fetches to EMS not 540 that have not yet sent a CPE return warning to MSCE. Incremented seven cycles prior to an EMS not 540 advance for CPE. Decremented during the cycle that a return warning is sent to MSCE for EMS not 540 returns.

CPE-EMS Pipe Position 1-2 - NT486
A duplication of positions 1-2 of the CPE-EMS pipe in output priority. Whenever CPE fetches from an EMS (access not 540) a bit enters this pipeline. Used for EMS access of 600 or 660.

CPE-Q-Return Pipe Position 1-7 - NT492-495
A one-bit, seven-cycle shifter that predicts the cycle that priority should be made in order to return to CPE from the queue.

CPE Request Buffer - Sink Address and Instruction - NT469-472
A 12-bit register that receives the 12 bits described for the CPE backup buffer and presents these bits to the queue.

Request Buffer Data Skew Pipe Position 1-3 - NT480
A one-bit, three-cycle shifter that pipelines CPE request buffer store conditions in order to hold the incoming skewed data at the proper time.

Control Triggers

Allow Alternate Busy - NT476
Allows alteration of PSCE busy signal to MSCE when less than three queues are available.

Alternate Binary Trigger - NT476
A binary trigger that generates alternate busy signals under control of the allow alternate busy trigger.

CPE Enter EMS Pipe - NT484
CPE will gain Q output priority on this cycle for a fetch to an EMS whose access is not 540.

CPE-Q-Return Slot Predict - NT488
Assigns slots on the CPE return bus to queue returns to CPE.

CPE Request Backup - NT475
A CPE select for EMS has been received from MSCE while the CPE request buffer is full. The select is in the CPE backup buffer waiting for transfer to the CPE request buffer.

DIAGRAM 5-436. PSCE TRIGGER LIST (SHEET 1 OF 4)

CPE Request Transfer - NT475
Transfers a CPE select for EMS from the backup buffer to the request buffer.

CPE Request Trigger - NT474
A CPE select for EMS has been received from MSCE and is waiting in the CPE request buffer for entry into the queue.

EMS Return Warning to MSCE - NT484
Signals MSCE that data will be returned from PSCE for CPE in ten cycles.

Hold Backup Address - NT479
Causes the CPE backup buffer (address, mark, key, sink address) to hold its contents.

Hold Backup Data - NT483
Causes the CPE backup buffer (data) to hold its contents.

Hold Backup Reject - NT479
Causes the CPE backup buffer reject bit to hold.

PSCE Busy to MSCE - NT477
A signal from PSCE to MSCE which stops MSCE from issuing CPE selects for EMS to PSCE.

Punchthrough - NT485
This is a CPE punchthrough cycle thereby allowing an incoming CPE request to bypass output priority and select an EMS directly.

Set Request Address - NT478
Causes the CPE request buffer (address, mark, key, sink address) to hold its contents.

Set Request Data - NT481
Causes the CPE request buffer (data) to hold its contents.

Set Request Reject - NT478
Causes the CPE request buffer reject bit to hold.

Simulate CPE Request - NT474
Generates a simulated CPE select to EMS when in simulate CPE mode.

Output Priority Control Stack

Active Bit, CRx - NT704, 709, 714, 719, 724, 729, 734, 739
Qx contains a request in process.

Cancel Trigger, Qx - NT708, 713, 718, 723, 728, 733, 738, 743
The CCC wants to cancel the pre-fetched data for the channel in Qx.

EMS S/S Parity Error Trigger - NT689
This trigger indicates even parity of the source/sink address bits 0-5, store, and parity which are gated out on the EMS bus.

Fetch Request, Qx - NT694, 695, 701, 702
Qx contains a fetch request.

Full Bit, CRx - NT707, 712, 717, 722, 727, 732, 737, 742
Qx contains data or error information.

Hold Bit, CRx - NT705, 710, 715, 720, 725, 730, 735, 740
Qx is being held as a sink for any memory errors detected during a delayed store.

MWS S/S Parity Error Trigger - NT682
This trigger indicates even parity of the source/sink address bits 0-5, store, and parity which are gated out on the MWS bus.

Parity Bit, CRx - NT747, 748, 759, 760
The parity bit CRx is parity for the seven-bit source/sink address.

Return Request, Qx - NT692, 693, 699, 700
Qx contains a device requesting return of data and/or errors.

SC, Channel, and PPE Request Triggers - NT690, 691
The device request triggers indicate that the respective device wants data and/or errors returned from the queue.

Source/Sink Register Bits 0-5, Qx - NT620, 655
Contents of this register identify the requesting device contained in Qx.

Store Bit, CRx - NT706, 711, 716, 721, 726, 731, 736, 741
The device in Qx is requesting a store or delayed store.

Store Request Trigger Qx - NT707, 712, 717, 722, 727, 732, 737, 742
When on, the store request trigger Qx keeps the store request line up during first cycle thereby generating one of the functions to set the corresponding control register hold bit.

Tag Bit, CRx - NT708, 713, 718, 723, 728, 733, 738, 743
Qx contains a tag operation.

Test and Set Bit, CRx - NT751, 752, 761, 762
The test and set bit in the control stack indicates an instruction from CPU to be executed by the memory.

Transpose Bit, CRx - NT749, 750, 757, 758
The transpose bit has no meaning for the PSCE. It is received from and returned to CPU with the source/sink address.

Output Priority, Address and Data Gate Control

Address Block Trigger, Qx - NT916, 918, 920, 925, 927, 929, 934
Terminates the address and CR gates to EMS and MWS, the data gate for unit return bus, and the CR and/or key gates for CPU return bus.

CPE-EMS Pipe - NT770, 791, 796
Initial section of a variable length pipe (12-17 stages). A CPE fetch to EMS that is not 540 access will cause an input to the pipe.

CPU Return Priority Triggers Q0-Q7 - NT826, 828
Allows Qx to enter priority for CPU returns.

CPU Return Qx Gate Trigger - NT880, 885, 890, 895, 900, 905, 910, 915
Qx has been selected to gate out on the CPU return bus.

Data Skew Trigger 1, Qx - NT916, 918, 920, 925, 927, 929, 934
Delays the turn on of the data trigger which generates the data out gates.

Data Skew Trigger 2, Qx - NT917, 919, 921, 922, 925, 928, 930, 935
Further delays the turn on of the data trigger, which generates the data out gates.

Data Trigger, Qx - NT917, 919, 921, 922, 926, 928, 930, 935
Allows the gate out of data on the EMS or MWS request buses or on the CPU return bus.

DIAGRAM 5-436. PSCE TRIGGER LIST (SHEET 2 OF 4)

Data Width Trigger 1, Qx - NT917, 919, 921, 922, 926, 928, 930, 935
Delays the turn off of the data gate, thereby controlling the data gate width.

Data Width Trigger 2, Qx - NT917, 919, 921, 922, 926, 928, 930, 935
Trigger not used.

Data Width Trigger 3, Qx - NT917, 919, 921, 922, 926, 928, 930, 935
Trigger not used.

EMS Data Trigger, Qx - NT876, 881, 886, 891, 896, 901, 906, 911
Controls the skew and width of the address and data gates to EMS for Qx. Generates coded gate bits $\overline{A}$ B that control outgating of Q data to EMS.

EMS Gate Trigger, Qx - NT876, 881, 886, 891, 896, 901, 906, 911
Qx has been selected to gate out on the EMS request bus.

EMS Priority Triggers Q0-Q7 - NT798, 801
Allows Qx to enter priority for EMS.

EMS Source/Sink Buffer - NT875
The buffers allow timing adjustment of the source/sink address to the storage distribution element (3/4 usec EMS).

Logout or Display Trigger, Qx - NT878, 883, 888, 893, 898, 903, 908, 913
Allows logout of address and data at their respective times.

Loop Block Trigger Q0-Q7 - NT851, 857, 863, 869
Prevents Qx from entering output priority.

MWS Bit Trigger, Qx - NT879, 884, 889, 894, 899, 904, 909, 914
The MWS bit trigger delays the decoded MWS bit to the end of address time. The trigger controls EMS tag available, gate key unit return, and MWS tag reserve.

MWS Data Trigger, Qx - NT877, 882, 887, 892, 897, 902, 907, 912
Enables the generation of coded gate bits A $\overline{B}$ that control outgating of Q data to MWS.

MWS Gate Trigger, Qx - NT877, 882, 887, 892, 897, 902, 907, 912
Qx has been selected to gate out on the MWS request bus.

MWS Priority Triggers Q0-Q7 - NT764, 767
Allows Qx to enter priority for MWS.

Occurrence Triggers - NT871, 874
These triggers indicate the loading order of the eight queues.

Response Trigger (One per Device) - NT830
Defines the unit to which data will be returned from the Q on the next cycle.

SC Readdress Trigger - NT878, 883, 888, 893, 898, 903, 908, 913
Allows re-address for Qx during data time to EMS or MWS.

Set Tag Block Trigger - NT790
Blocks MWS bus one cycle after a set tag was gated out.

Store Bit Trigger, Qx - NT879, 884, 889, 894, 899, 904, 909, 914
The store bit trigger delays the store bit from the control stack and holds it to the end of first cycle. The trigger controls the set tag and insert tag to EMS and MWS and also the turn on of the SC readdress trigger.

Store Return Trigger to CCC - NT831
Indicates to the CCC, that on the next cycle, errors will be returned from the Q on the unit return bus.

Tag Bit Trigger, Qx - NT879, 884, 889, 894, 899, 904, 909, 914
The tag bit trigger delays the tag bit from the control stack and holds it to the end of the first cycle. The trigger controls the tag operations.

Test and Set Trigger, Qx - NT877, 882, 887, 892, 897, 902, 907, 912
Sends test and set signal to MWS or EMS during address time.

Unit Return Bus Block Trigger - NT830
Allows gate-out on the unit return bus on alternate cycles.

Unit Return Qx Gate Trigger - NT880, 885, 890, 895, 900, 905, 910, 915
Qx has been selected to gate out on the unit return bus.

Unit Return (CCC Return) Priority Triggers Q0-Q7 - NT826, 828
Allows Qx to enter priority for unit returns.

Output Priority, Storage Bus Selection

Block Decode Trigger - NT938
This trigger is not used.

Box Group Triggers - NT937, 938
These triggers are not used.

EMS Box Busy Reset Trigger (Box 0-31) - NT953, 956, 961, 964, 969, 972, 977, 980, 985, 988, 993, 996, NU001, 004, 009, 012
The function of this trigger is to establish a platform for a busy trigger reset after an EMS box goes from busy to not busy.

EMS Box Busy Trigger (Box 0-31) - NT953, 956, 961, 964, 969, 972, 977, 980, 985, 988, 993, 996, NU001, 004, 009, 012
This trigger indicates to the Q, from the time the select trigger comes on until the memory goes from busy to not busy, that requests to this box cannot be expedited.

EMS Select Box Trigger (Box 0-31) - NT953, 956, 961, 964, 969, 972, 977, 980, 985, 988, 993, 396, NU001, 004, 009, 012
This trigger indicates to EMS that some device is going to store in or fetch from some address in the BSM selected. This trigger also allows an EMS bus address check, comparing the BSM selected with the four low-order address bits.

EMS Select Error (1-3) - NU039
This trigger indicates discrepancies between the outgated address to EMS and the BSM selected.

MWS Box Busy Reset Trigger (Box 0-15) - NU013, 018, 019, 024, 025, 030, 031, 036
This trigger establishes a platform for a busy trigger reset when MWS is being simulated.

MWS Box Busy Trigger (Box 0-15) - NU014, 017, 020, 023, 026, 029, 032, 035
Indicates to the Q, from the time the select trigger comes on until the memory goes from busy to not busy, that requests to this box cannot be expedited.

MWS Select Box Trigger (Box 0-15) - NU014, 017, 020, 023, 026, 029, 032, 035
Allows a MWS bus address check, comparing the BSM selected with the four low-order address bits.

MWS Select Error Check - NU052
Indicates discrepancies between the outgated address to MWS and the BSM selected.

Tag Complete Triggers - NT939, 940
These triggers are not used.

Output Priority, Logout and Maintenance Mode

Allow Clock Trigger - NU501
Allows the ten basic clock pulses to be distributed to the PSCE.

EMS Simulate Full Trigger, Qx - NU079, 082
Upon selection of EMS, this trigger establishes a platform that causes a simulated set full bit signal with the occurrence of counter reset Qx.

End Single Cycle Trigger - NU501
Generates a platform to reset the allow clock trigger.

Maintenance Console Address Block Trigger - NU077
Controls the falling of the address gate for 3/4 usec memory.

Maintenance Console Gate Trigger - NU076
Enables the MC address gate until the end of the memory display or store pushbutton signal.

Maintenance Console Priority Trigger - NU075
Establishes a platform for the MC address cycle.

MC Data Skew Trigger 1 - NU077
Delays the turn-on of the data trigger which generates the data outgates.

MC Data Skew Trigger 2 - NU077
Further delays the turn-on of the data trigger, which generates the data outgates.

MC Data Trigger - NU078
Allows gate-out of data from the switches on the EMS, MWS, and unit return buses.

MC Data Width Trigger 1 - NU078
Delays the turn-off of the data gate, thereby controlling the data gate width.

MC Data Width Trigger 2 - NU078
Generates a platform to turn on data width trigger 3.

MC Data Width Trigger 3 - NU078
Resets the data trigger which causes the fall of the data gate.

MWS Simulate Full Trigger, Qx - NU079, 082
When MWS has been selected by output priority, this trigger establishes a platform that causes a simulated set full bit signal with the occurrence of counter reset Qx.

Priority Trigger for Logout - NU056
Allows logout or display to enter priority on the MWS bus until logout or display becomes high priority.

Scan Trigger - NU056
Resets the logout priority trigger when the Q gate trigger turns on, and keeps it reset until the scan is completed.

Single Cycle Trigger - NU501
Establishes a platform to set the end single cycle trigger and prevents the allow trigger from being set a second time by one single cycle pulse.

Stop PSCE Clock Trigger - NU501
Stops the ten basic clock pulses generated by the ring from being distributed to the PSCE.

Synchronizing Trigger - NU501
Generates a stable platform to set the single cycle trigger.

CCC, Channel Instruction Controls

Allow SIO Trigger - NU176
Gates the start I/O or IPL to the channels at the appropriate time. The instruction is suppressed until a queue has been reserved, if a queue is required.

IPL Counter Triggers and Latches - NU174
A two-position counter that provides the timing for the IPL pulse width.

IPL Interlock Trigger - NU173
Prevents more than one IPL pulse from occurring per IPL operation.

IPL Trigger - NU173
Provides a 240 usec IPL pulse at the channels.

Manual HIO Trigger - NU173
Simulates a halt I/O instruction to the PSCE when the HIO switch is depressed.

Manual SIO Trigger - NU173
Simulates a start I/O instruction to the PSCE when the SIO switch is depressed.

SIO Busy Gate Trigger - NU175
Provides a gate for the duration of a SIO or IPL if the selected channel is already in operation or if the selected channel is the storage channel or a multiplexer channel. Under these conditions, the SIO gate trigger is suppressed.

SIO Gate Trigger - NU175
Provides a one cycle gate during a start I/O or IPL, to initiate the queue reserve sequence if required, make the high or low-speed channel determination, and increment the appropriate in-use counter.

SIO Interlock Trigger - NU176
Prevents more than one SIO gate or sync from occurring per start I/O.

SIO Sync Trigger - NU175
Synchronizes the start I/O instruction line from CPU, direct control feature, manual SIO, or IPL. Provides a stable signal to the SIO control triggers, SIO gate and SIO busy gate.

CCC, Common Storage Request and Response Cycle Controls

Add 1 Trigger - NU224
Increments the current channel storage address by 1 when required during prefetch operation.

Add 2 Trigger - NU223
Increments the current channel storage address by 2 when required during prefetch operations.

Data Gate Trigger - NU222
Gates the data from the required interface to the unit request data bus during channel store operations.

IF1 Accept Trigger - NU221
Notifies a channel that its storage request has been accepted by the PSCE to prevent the channel from reissuing the same storage request.

IF1 Bus Valid Latch - NU220
The storage address from the requesting channel on interface 1 is valid in the PSCE.

IF1 Input Priority Response Latch - NU222
The storage request from a channel on interface 1 has been entered into a queue.

IF3 Input Priority - NU222
The storage request from a channel on interface 3 has been entered into a queue.

IF1 Priority Trigger - NU218
The current input priority request will service a channel on interface 1.

IF3 Priority Trigger - NU218
The current input priority request will service a channel on interface 3.

IF1 Response Control Trigger - NU218
Gates the increment pulses to the interface 1 response counter.

IF1 Response Counter Triggers and Latches - NU219, 220
Delays the input priority request until the storage address from the requesting channel is valid in the PSCE.

IF1 Response Cycle Trigger - NU218
The CCC is in the process of responding to a channel storage request on interface 1. This trigger is on from the time a channel is given response priority until the channel request is entered into a queue.

Input Priority Trigger - NU221
A request to enter input priority for the purpose of setting a channel storage request from interface 1 or 3 into a queue.

Retain Priority - NU224
Prevents interface 1 priority trigger from resetting until two successive input priority requests have been made during a prefetch 2 initial request operation.

CCC, Channel Priority

Channel X (0-5 and 7) Release Sync Triggers - NU239, 245
Synchronizes the channel X end signal to provide a stable signal to enter the queue release priority network.

Channel X (0-5 and 7) Request Sync Triggers - NU239, 245
Synchronizes the storage request line from the channel to provide a stable signal to enter the response priority network.

Channel X (0-5 and 7) Response/Release Priority Triggers - NU239, 245
The given channel has priority over all others on interface 1 to either initiate the response cycle sequence or the queue release sequence.

CCC, Multiplexer Channel Control Triggers

Channel X (0 or 7) Multiplexer Reserve Trigger - NU252, 306
During the rise of the 'selector subchannel in operation' signal, this trigger initiates the queue reserve sequence.

Channel X (0 or 7) Op In Sync Trigger - NU252, 306
Synchronizes the rise or fall of the 'selector subchannel in operation' signal. This signal is used within CCC to determine when a multiplexer channel is going into or out of operation.

Channel X (0 or 7) Simulate Multiplex Op In Trigger - NU252, 306
During manual simulate operations, this trigger is used to simulate the 'selector subchannel in operation' signal.

CCC, High-Speed Channel Control Triggers

Channel X (1-5) Cancel Trigger - NU262, 271, 280, 289, 298
Notifies output priority controls to cancel any outstanding storage requests for this channel in the queue. The channel has either terminated or made a control word request during the prefetch condition.

Channel X (1-5) Control Word Trigger - NU261, 270, 279, 288, 297
Defines a storage request by the channel as a non-data fetch request. Requests by the channel for either the channel address word (CAW) or a channel command word (CCW) will set the control word trigger.

Channel X (1-5) Fetch Complete Gate - NU259, 268, 277, 286, 295
Allows the channel to examine the channel X fetch complete signal generated by output priority controls.

Channel X (1-5) High Trigger - NU261, 270, 279, 288, 297
All storage requests from the channel for the current operation will be treated by the CCC as high-speed for purposes of queue reservation and data prefetching or storing.

Channel X (1-5) Initial Request Trigger - NU261, 270, 279, 288, 297
Defines the initial or start-up condition during a prefetch operation. The duration covered is from the first data fetch request until the prefetch running condition.

Channel X (1-5) Pre-CDA Trigger - NU260, 269, 278, 287, 296
The channel is in the portion of a chain data operation that does not require any storage requests to be entered into the queue. All outstanding data has already been prefetched.

Channel X (1-5) Prefetch Trigger - NU261, 270, 279, 288, 297
Covers the period defined as the prefetch running condition. The current data word requested by the channel has been prefetched by the PSCE during a prior channel storage request.

CCC, High, Low, or Multiplexer Channel Control Triggers

Channel X (0-5 and 7) Advance Trigger - NU253, 262, 271, 280, 289, 298, 307
Generates a pulse to notify the channel that data requested by the channel is available on the storage bus.

DIAGRAM 5-436. PSCE TRIGGER LIST (SHEET 3 OF 4)

Channel X (0-5 and 7) Error Sample Trigger - NU253, 262, 271, 280, 289, 298, 307
Generates a pulse to notify the channel that any errors incurred during a store request are available on the error bus.

Channel X (0-5 and 7) In Operation Trigger - NU254, 263, 272, 281, 290, 299, 308
During a 2860 operation, this trigger means that the channel has accepted a SIO instruction and has not yet sent a channel X end signal. During a 2870 operation, it means a selector subchannel is in operation.

Channel X (0-5 and 7) Interlock Trigger - NU255, 264, 273, 282, 291, 300, 309
Prevents a channel X storage request signal from entering response priority until its previous request has been serviced.

Channel X (0-5 and 7) Manual Store Trigger - NU254, 263, 272, 281, 290, 299, 308
Latches the store switch setting during a simulate SIO to channel X. It then provides the store or fetch signal during channel X simulated storage requests.

Channel X (0-5 and 7) Release Trigger - NU253, 262, 271, 280, 289, 298, 307
Records channel X end signal until the queue release sequence for this channel is completed.

Channel X (0-5 and 7) Return Request Trigger - NU255, 264, 273, 282, 291, 300, 309
A request to output priority controls to transfer data and/or errors residing in a queue for channel X to the CCC return buffer.

Channel X (0-5 and 7) Storage Request Trigger - NU254, 263, 272, 281, 290, 299, 308
Coupled with the request generation, this trigger simulates storage requests from channel X during simulate I/O operations.

CCC Data Return Controls

IF1 Address Check Trigger - NU228
Provides buffering to interface 1 for any address parity error detected on a channel storage request.

IF1 Data Check Trigger - NU229
Provides buffering to interface 1 for any data parity error detected on a channel storage request.

IF1 Invalid Address Check Trigger - NU229
Provides buffering to interface 1 for any invalid address error detected on a channel storage request.

IF1 Protect Check Trigger - NU229
Provides buffering to interface 1 for any storage protect violation detected on a channel storage request.

Return Interlock Counter Triggers and Latches - NU231
A three-position counter that determines the duration of each return in the CCC return buffer.

Return Interlock Trigger - NU230
Prevents any further store or fetch returns from entering the CCC return buffer until the current return has timed out.

CCC, Queue Reserve/Release Controls

High-In-Use Counter Triggers and Latches - NU232, 233
A three-position counter which records the number of channel operations defined as high speed which are currently in operation.

Low-In-Use Counter Triggers and Latches - NU323, 324
A four-position counter which records the number of channel operations defined as low speed which are currently in operation.

Low Q Available Counter Equals 0 Latch - NU316
Provides a fast 'low-Q-available counter not equal to zero' signal to suppress additional temporary reserves.

Low Q Available Counter Triggers and Latches - NU234, 235
A two-position counter which records the number of queues reserved for low-speed channel operations currently unoccupied by a channel storage request.

Low Q Reserved Counter Triggers and Latches - NU314
A two-position counter which records the number of queues currently reserved for low-speed channel operations.

Low Return Increment Latch - NU234
Latches a data return condition to provide a gate to increment the low queue available counter.

Temp Reserve Gate Trigger - NU316
Allows a queue to be reserved for those operations that require a queue for the duration of a storage request only. Provides the gate to examine the low queue reserve criteria for multiplexer channel reserve operations.

Release High Gate Trigger - NU316
Provides the gate to examine the queue release criteria for a high-speed channel ending operation.

Release Low Gate Trigger - NU316
Provides the gate to examine the queue release criteria for a low-speed channel ending operation.

Release Request Trigger - NU318
A request to enter input priority for the purpose of releasing a previously reserved queue.

Release Response Latch - NU218
Latches a one-cycle response signal from input priority to notify the CCC that a previously reserved queue has been released.

DIAGRAM 5-436. PSCE TRIGGER LIST (SHEET 4 OF 4)

Release 2 Trigger 1 and Trigger 2 - NU318
Prevents the reset of the release request trigger until two queues have been released during a release sequence for a high-speed channel operation in prefetch 2 mode.

Reserve Request Trigger - NU317
A request to enter input priority for the purpose of reserving a queue.

Reserve Response Latch - NU223
Latches a one-cycle response signal from input priority to notify the CCC that a queue has been reserved.

Reserve 2 Trigger 1 and Trigger 2 - NU317
Prevents the reset of the reserve request trigger until two queues have been reserved during a reserve sequence for a high-speed channel operation in prefetch 2 mode.

PPE, Interface Control

Address Gate Check - NT263
Generates a gate of the proper duration to outgate an address check signal to the PPE when an address check occurs.

Cancel - NT262
Turned on if a cancel is received by the PSCE from the PPE. If a store operation was initiated by this request, the operation is turned into a fetch and data is returned to the PPE.

Insert Tag - NT256
Turned on when an insert tag instruction has been requested by the PPE and remains on until a new PPE instruction is received by the PSCE.

Left/Right - NT257
In Mod 50 mode, this trigger indicates that a single word bit was present in the request address and is used to outgate the left or right half of a doubleword to the PPE.

PPE Counter Positions 1, 2, 4, 8 - NT260, 261
A four-position counter used in the generation of interface lines of the proper duration to the PPE.

PPE Data Check Queue - NT264
Set when a queue is outgated to the PPE return buffer if a data check associated with a PPE request was stored in the error queue.

PPE Data Check Unit - NT264
Set when a data check is detected as a queue is outgated to the PPE return buffer.

PPE Store - NT256
Set when a store operation has been requested by the PPE. Remains on until a new PPE instruction has been received by the PSCE.

Pre-Gate Control - NT257
Used to start the gating in Mod 50 mode of the left or right word to the PPE in anticipation of SLT logic delay.

Program Gate - NT263
Outgates to the PPE, a store protect violate (SPV) signal of the proper duration when an SPV has been detected.

Request Busy - NT257
Turned on during the receipt of a request from the PPE and remains on until the return sequence has been completed by the PPE.

Request Counter Control - NT257
Indicates that the PPE counter is being stepped because of a request from the PPE.

Request Input Priority - NT259
Turned on when the proper information is contained in the PPE request buffer and turned off with a response from input priority.

Request Latch - NT258
Used in Mod 50 mode to remember a plus state request from the PPE.

Response Trigger - NT258
Informs the PPE that the present request has been accepted by the PSCE.

Return Counter Control - NT263
Turned on with the receipt of a response from output priority and used to control stepping of the PPE counter during the return sequence.

Set Tag - NT256
Set when a set tag operation has been requested by the PPE. Remains on until a new PPE instruction has been received by the PSCE.

Sync Trigger 1 - NT258
Turned on with the receipt of a request and a clock to synchronize the request from the PPE to the PSCE clock timing.

Sync Trigger 2 - NT258
Used in conjunction with sync trigger 1 in the final step of synchronizing the request from PPE.

Test and Set - NT256
Turned on when a test and set instruction has been received by the PSCE from the PPE and remains on until a new PPE instruction is received by the PSCE.

PSCE Error Triggers

Refer to Diagram 1-1 in IBM 2091 Processing Unit, Volume 1, Diagnostic Techniques, FEMDM, Form Y22-6671, for a description of the PSCE error triggers.

Objective:
Reset Check Indicators, CPU Controls, On-Line Channels and Control Units.

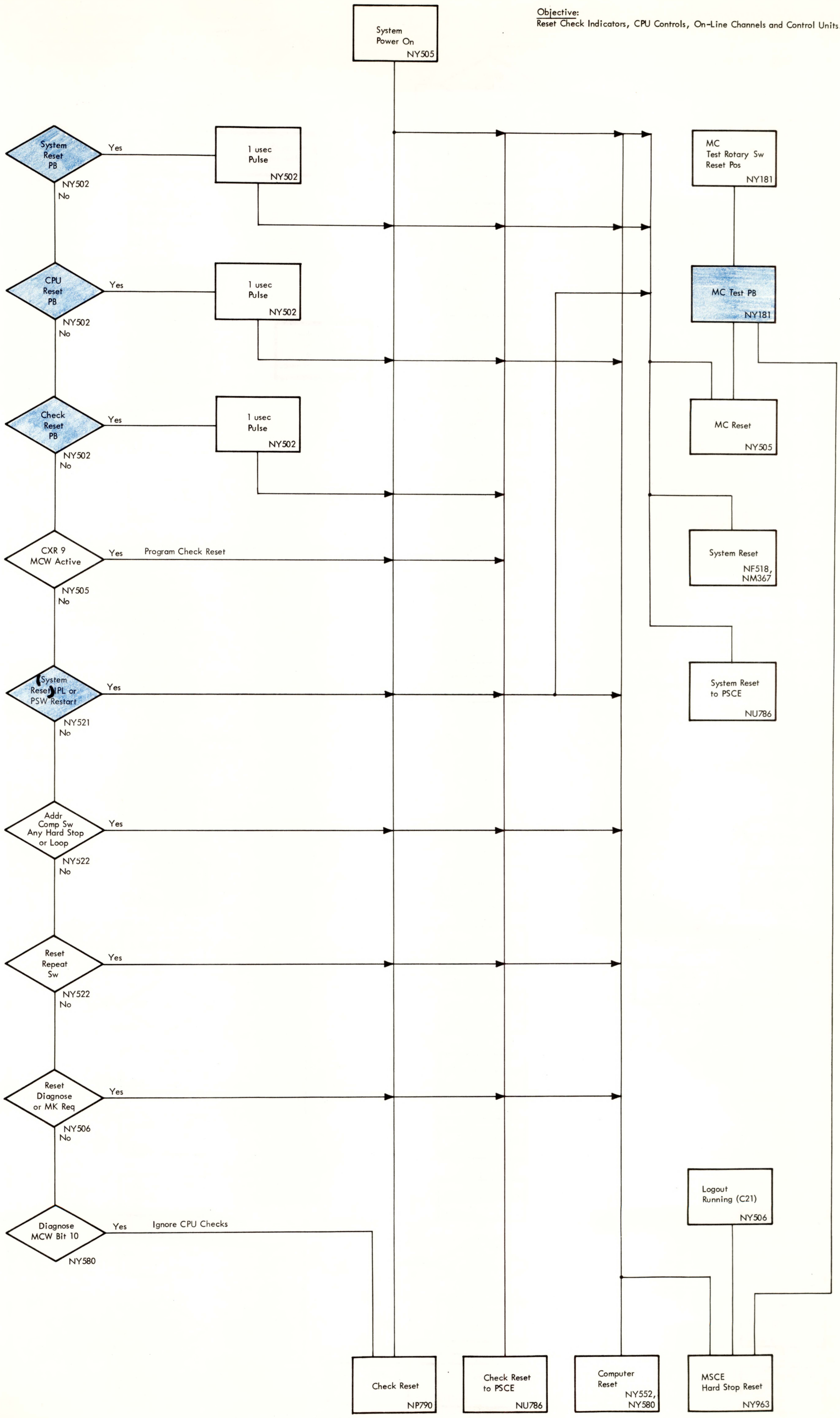
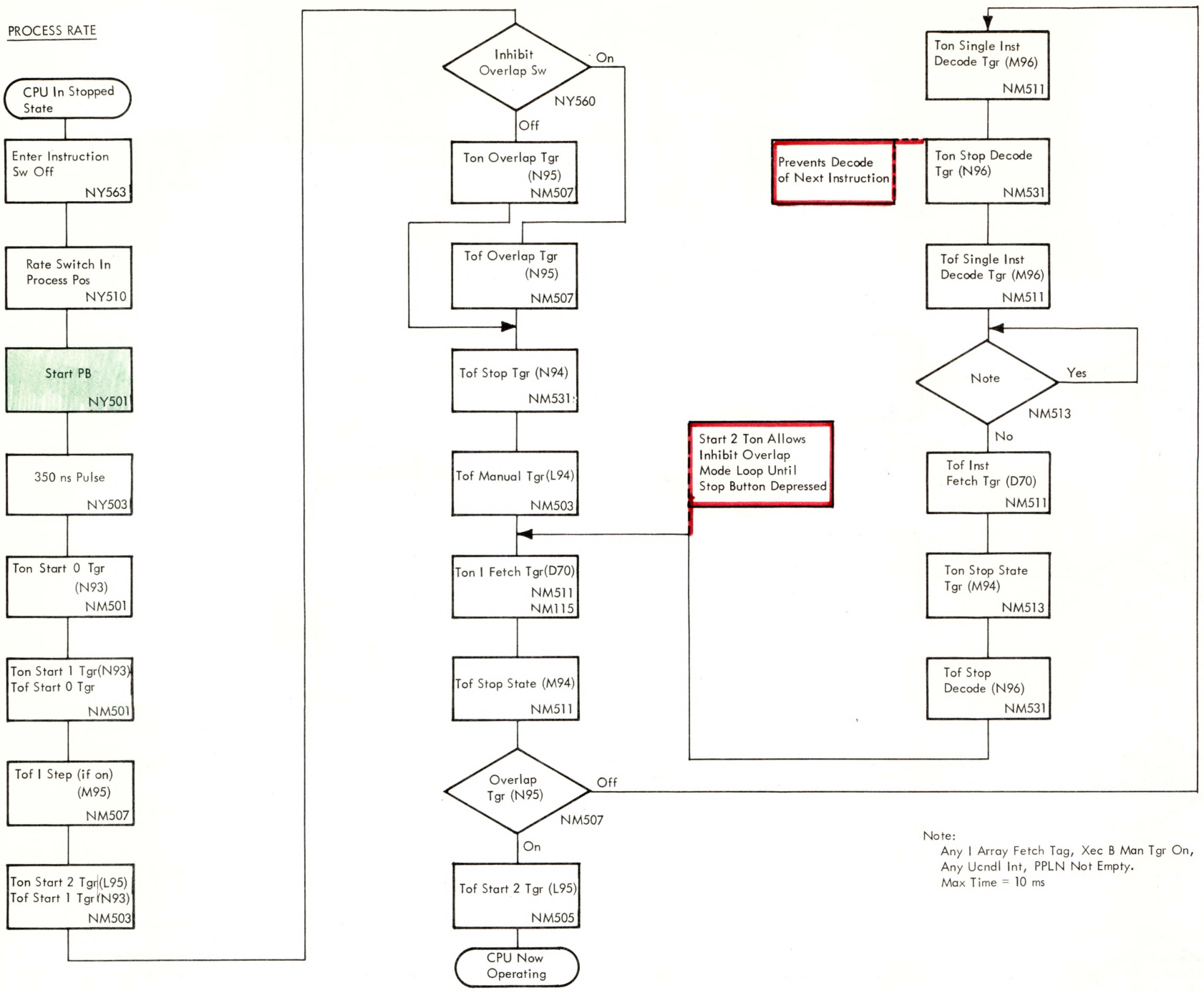


DIAGRAM 5-500. SYSTEM, COMPUTER, AND CHECK RESETS

PROCESS RATE

Objective:

To put CPU in operating state (rate switch in process, enter instruction switch off, inhibit overlap switch on or off).



Note:
Any I Array Fetch Tag, Xec B Man Tgr On, Any Ucndl Int, PPLN Not Empty.
Max Time = 10 ms

MULTI STEP OR INSTRUCTION STEP

Objective:

To perform instructions at multi or instruction step rate.

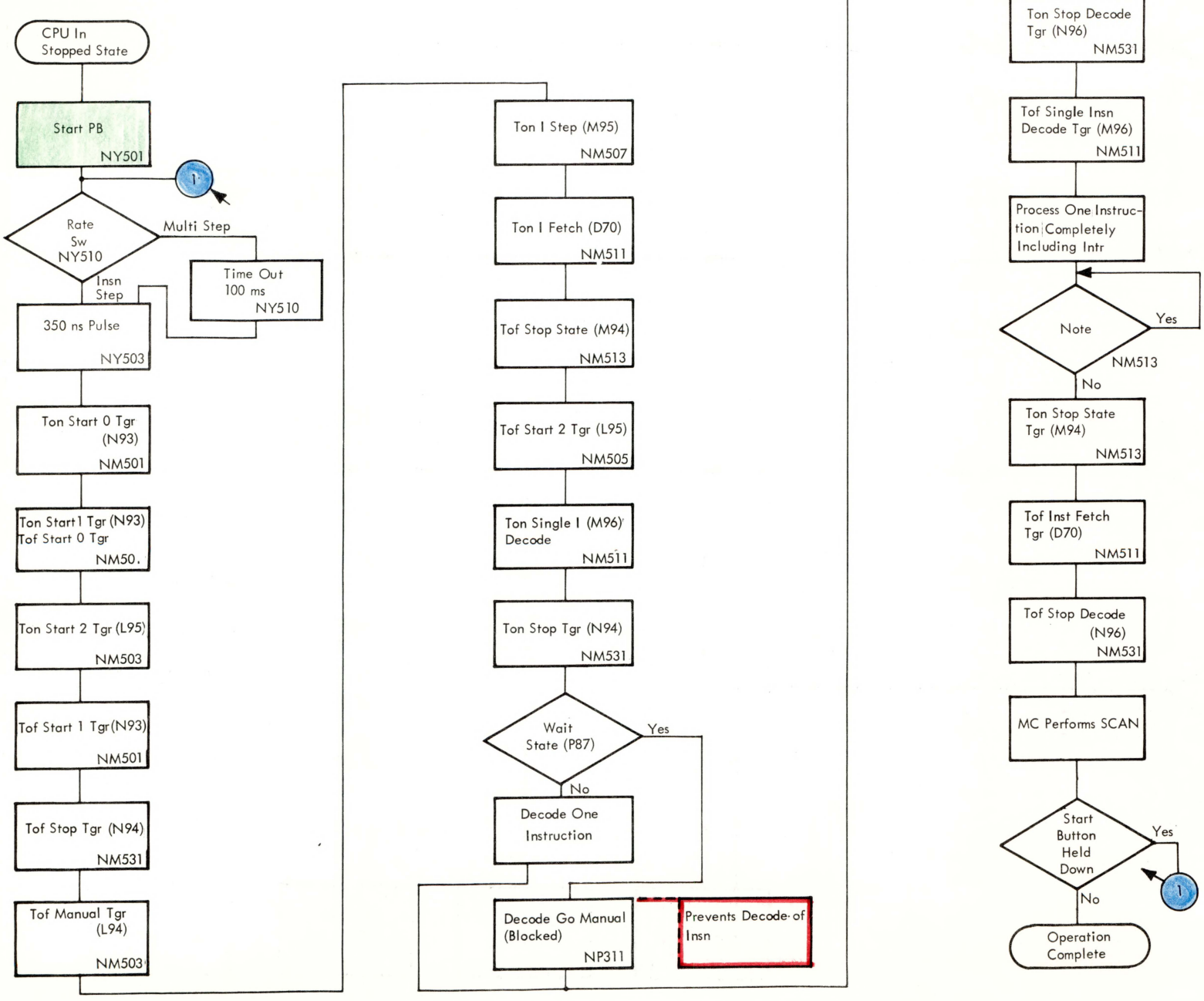
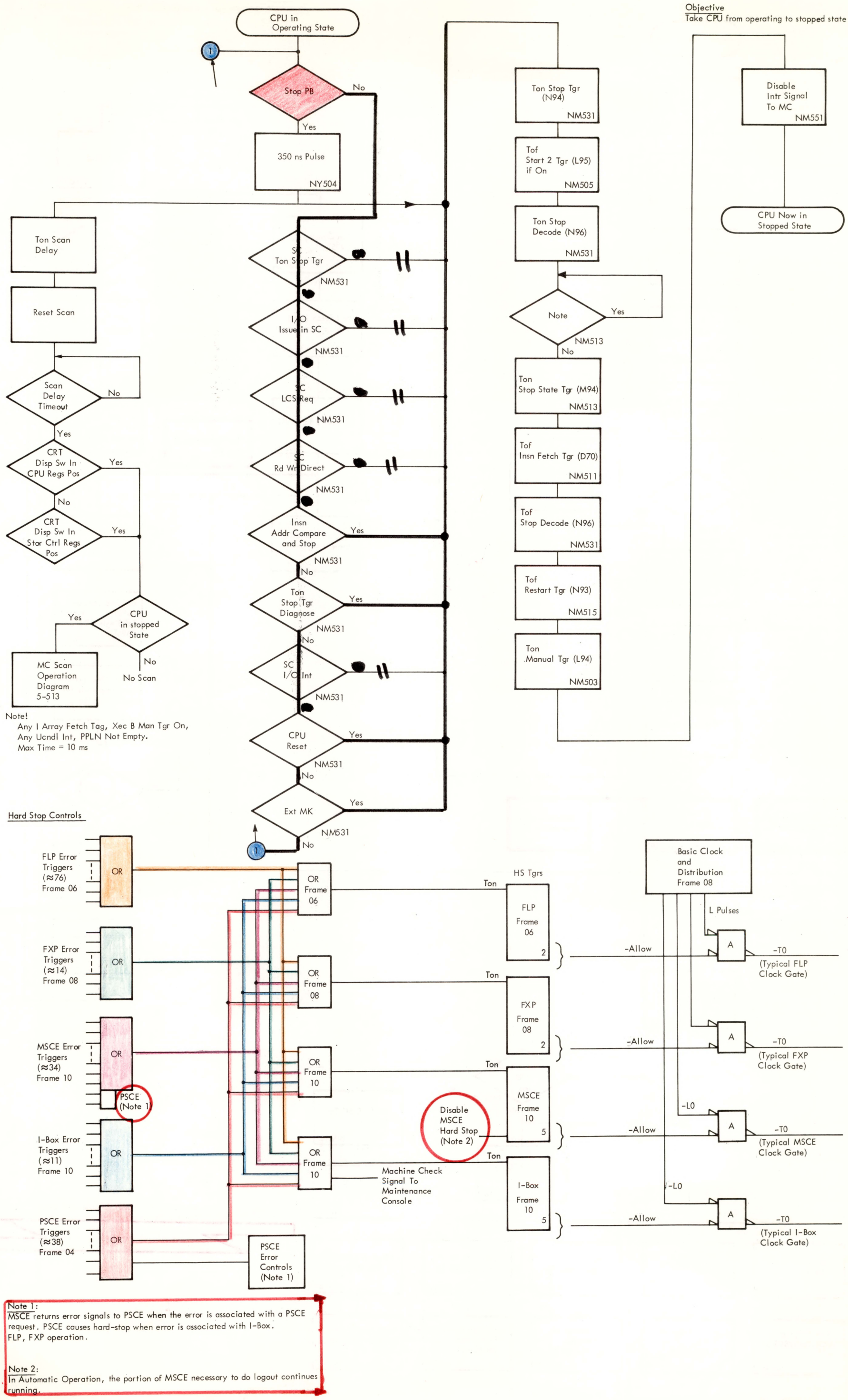


DIAGRAM 5-501. START SEQUENCE

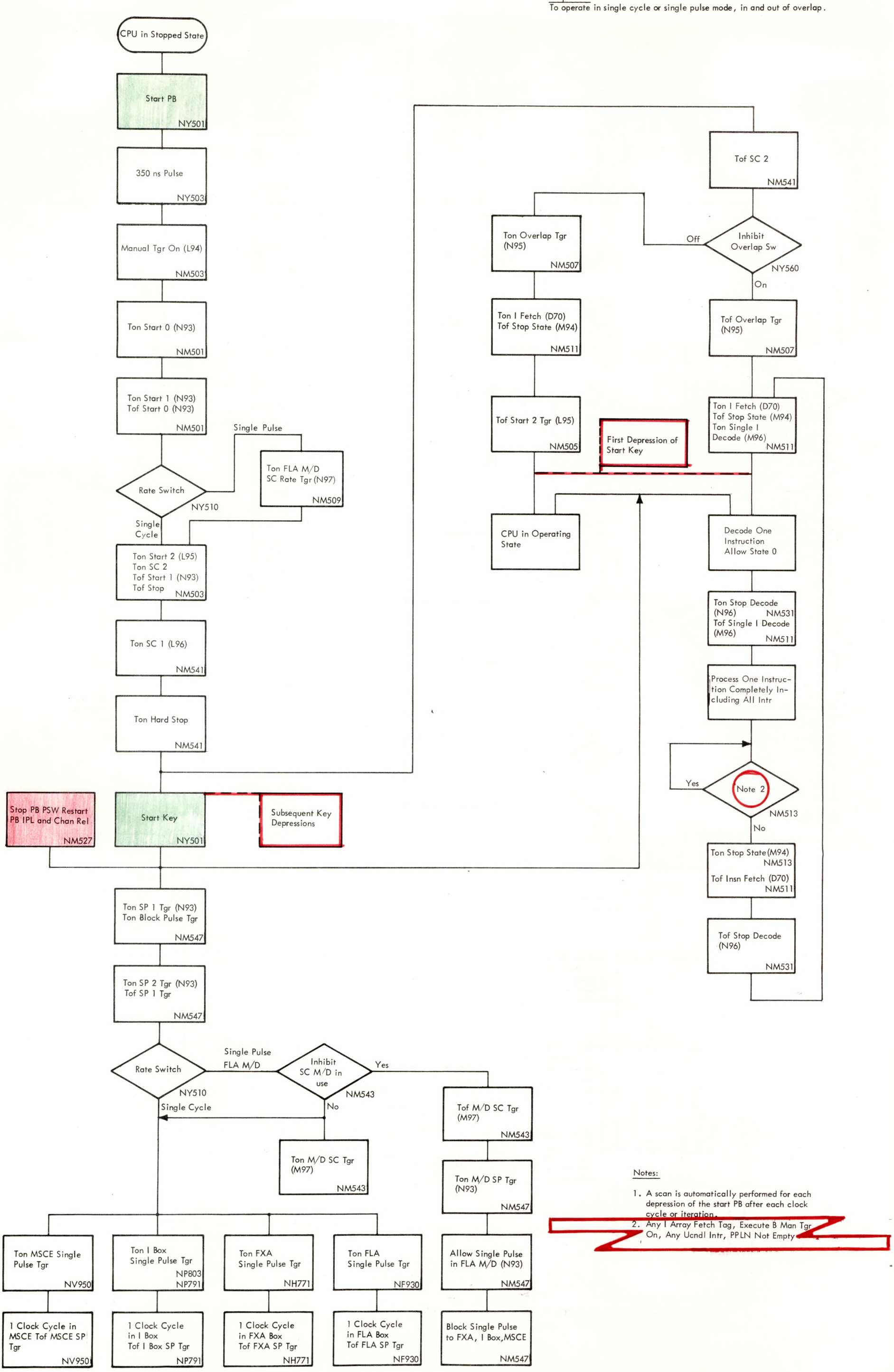


Note 1:
MSCE returns error signals to PSCE when the error is associated with a PSCE request. PSCE causes hard-stop when error is associated with I-Box. FLP, FXP operation.

Note 2:
In Automatic Operation, the portion of MSCE necessary to do logout continues running.

DIAGRAM 5-502. STOP SEQUENCE

Objective:
To operate in single cycle or single pulse mode, in and out of overlap.



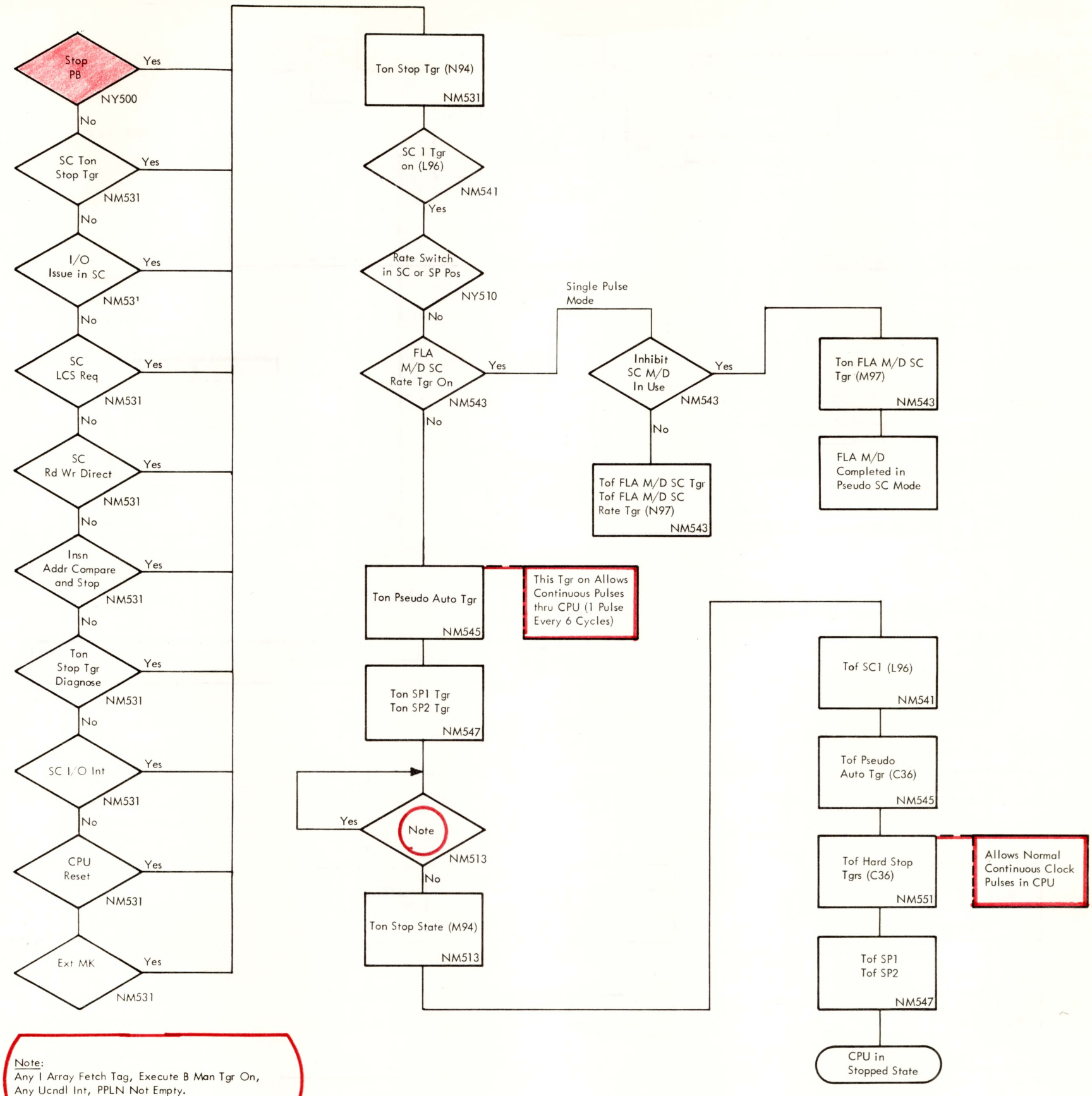
Notes:

1. A scan is automatically performed for each depression of the start PB after each clock cycle or iteration.
2. Any I Array Fetch Tag, Execute B Man Tgr On, Any Ucndl Intr, PPLN Not Empty

DIAGRAM 5-503. SINGLE CYCLE OPERATION (SHEET 1 OF 2)

Objective:

Return system clock to normal after single cycle or single pulse operation.



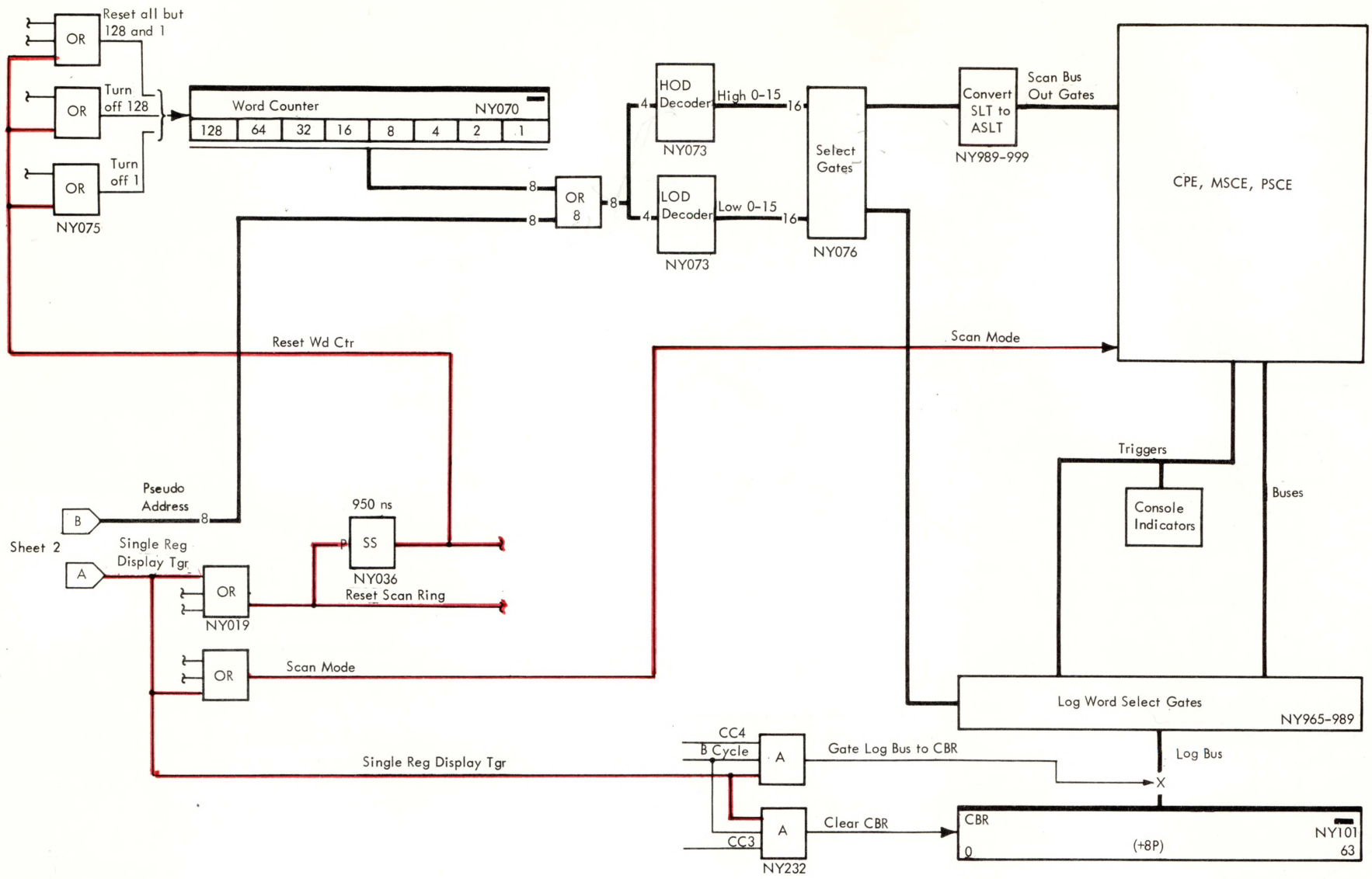
Note:
Any I Array Fetch Tag, Execute B Man Tgr On,
Any Ucndl Int, PPLN Not Empty.
Max Time = 10 ms.

DIAGRAM 5-503. SINGLE CYCLE OPERATION (SHEET 2 OF 2)

Objective:

Display in CBR the contents of a GPR, an FPR, or an unaddressable register.

Single Register Display, Data Flow



Single Register Display

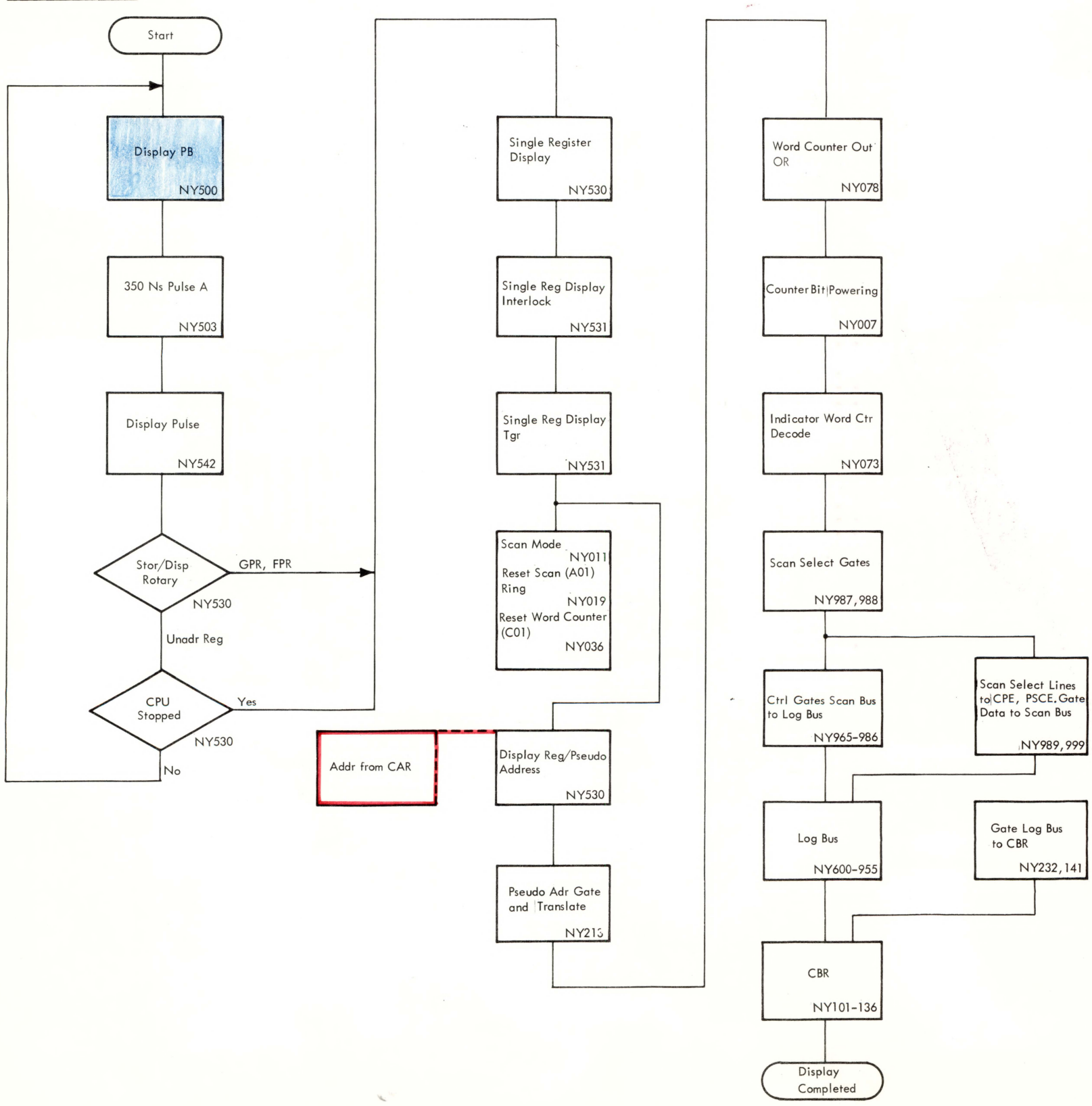


DIAGRAM 5-504. DISPLAY IN CBR (SHEET 1 OF 3)

	Sel Reg	Input Address Keys 28	29	30	31	Hex	Output (Pseudo Address) HO Digit 128	64	32	16	LO Digit 8	4	2	1	Hex
FLP	0	0	0	0	0	0	0	0	0	0	0	1	1	1	07
	2	0	0	1	0	2	0	0	0	0	1	0	0	0	08
	4	0	1	0	0	4	0	0	0	0	1	0	0	1	09
	6	0	1	1	0	6	0	0	0	0	1	0	1	0	0A
Gen	0	0	0	0	0	0	0	0	1	0	1	1	0	0	2C
	1	0	0	0	1	1	0	0	1	0	1	1	0	1	2D
	2	0	0	1	0	2	0	0	1	0	1	1	1	0	2E
	3	0	0	1	1	3	0	0	1	0	1	1	1	1	2F
	4	0	1	0	0	4	0	0	1	1	0	0	0	0	30
	5	0	1	0	1	5	0	0	1	1	0	0	0	1	31
	6	0	1	1	0	6	0	0	1	1	0	0	1	0	32
	7	0	1	1	1	7	0	0	1	1	0	0	1	1	33
	8	1	0	0	0	8	0	0	1	1	0	1	0	0	34
	9	1	0	0	1	9	0	0	1	1	0	1	0	1	35
	10	1	0	1	0	A	0	0	1	1	0	1	1	0	36
	11	1	0	1	1	B	0	0	1	1	0	1	1	1	37
	12	1	1	0	0	C	0	0	1	1	1	0	0	0	38
	13	1	1	0	1	D	0	0	1	1	1	0	0	1	39
	14	1	1	1	0	E	0	0	1	1	1	0	1	0	3A
	15	1	1	1	1	F	0	0	1	1	1	0	1	1	3B

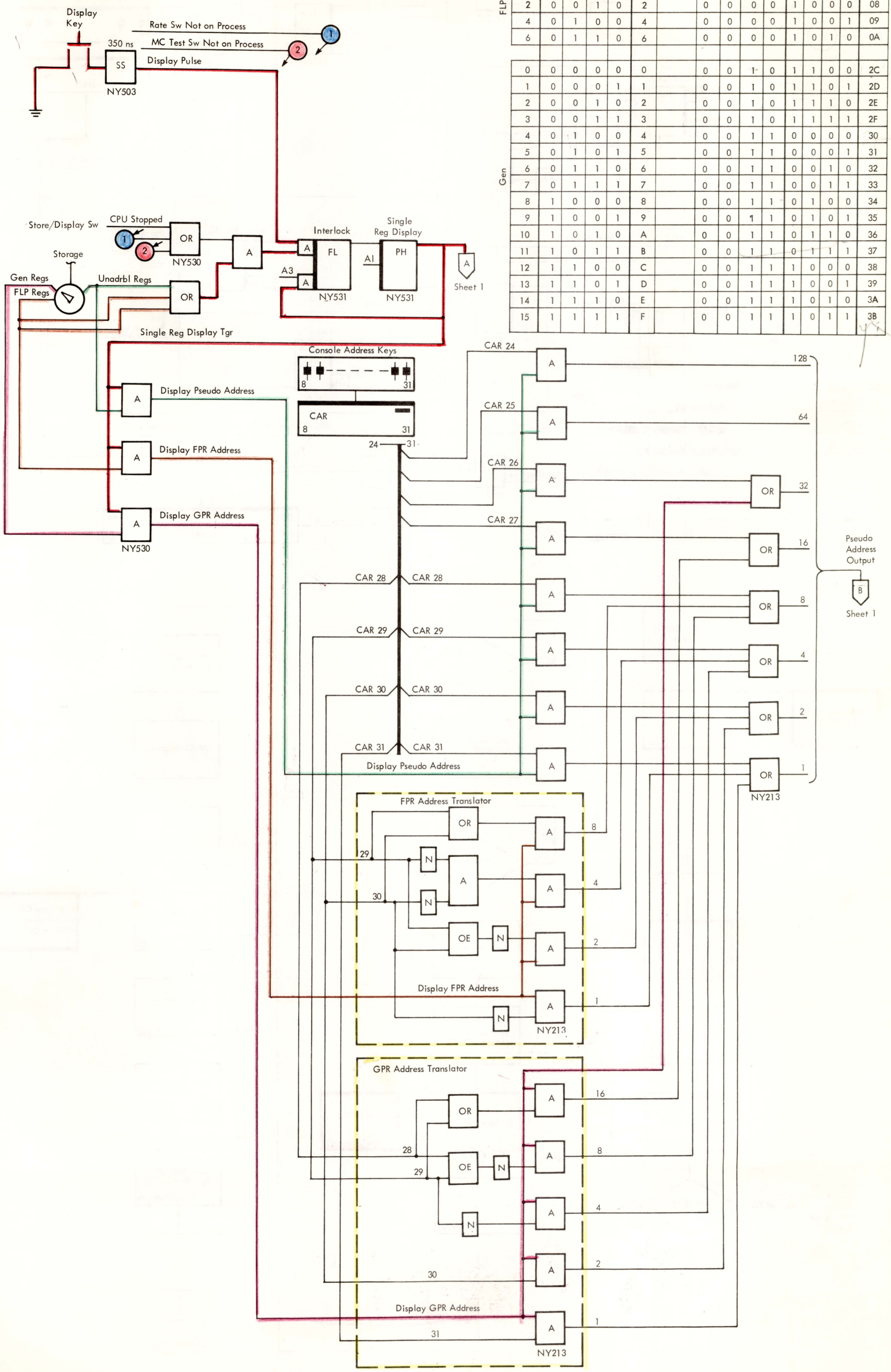
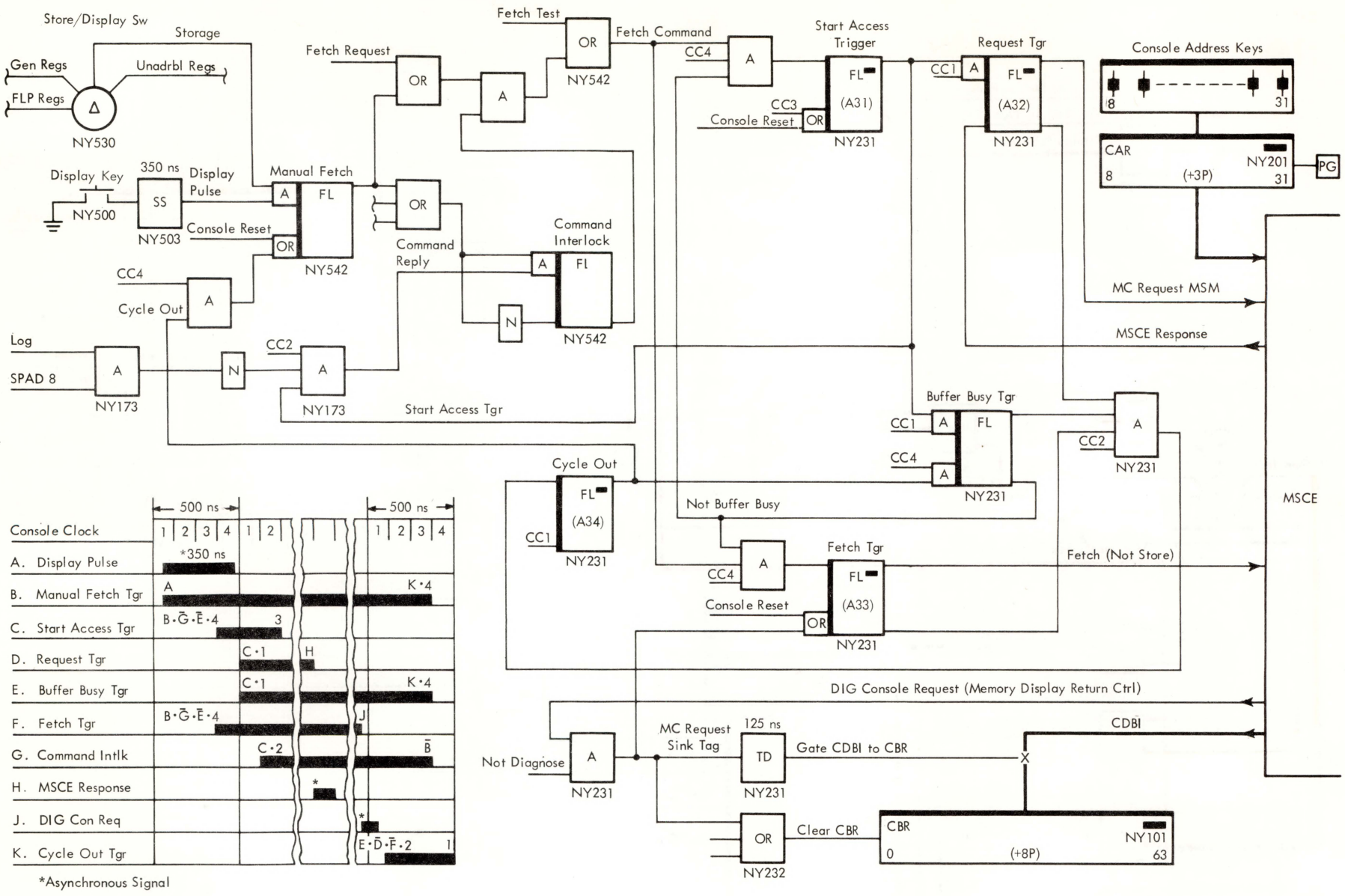


DIAGRAM 5-504. DISPLAY IN CBR (SHEET 2 OF 3)

Objective:
Display in CBR the contents of a selected storage location.

Storage Display In CBR



Storage Display

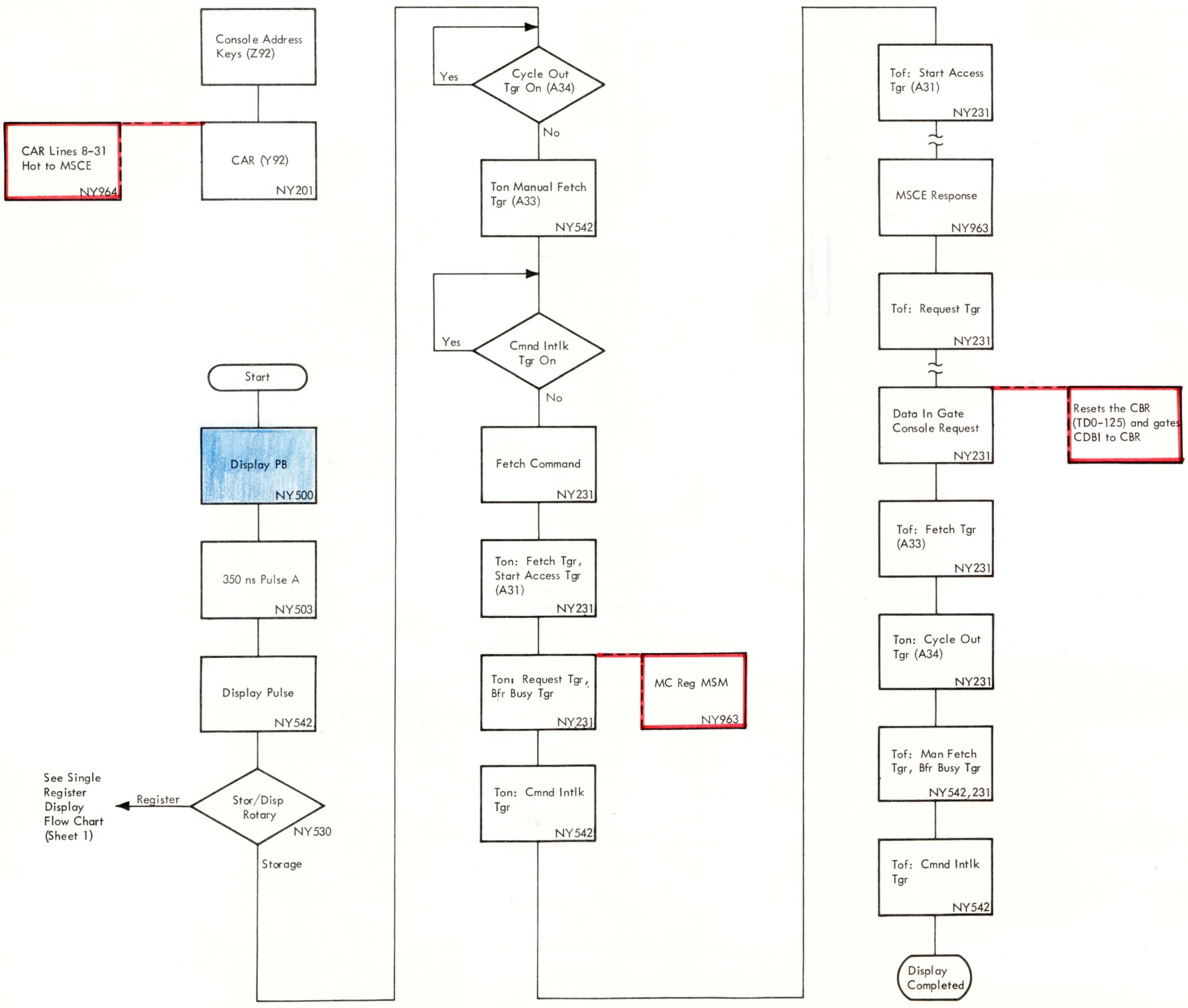
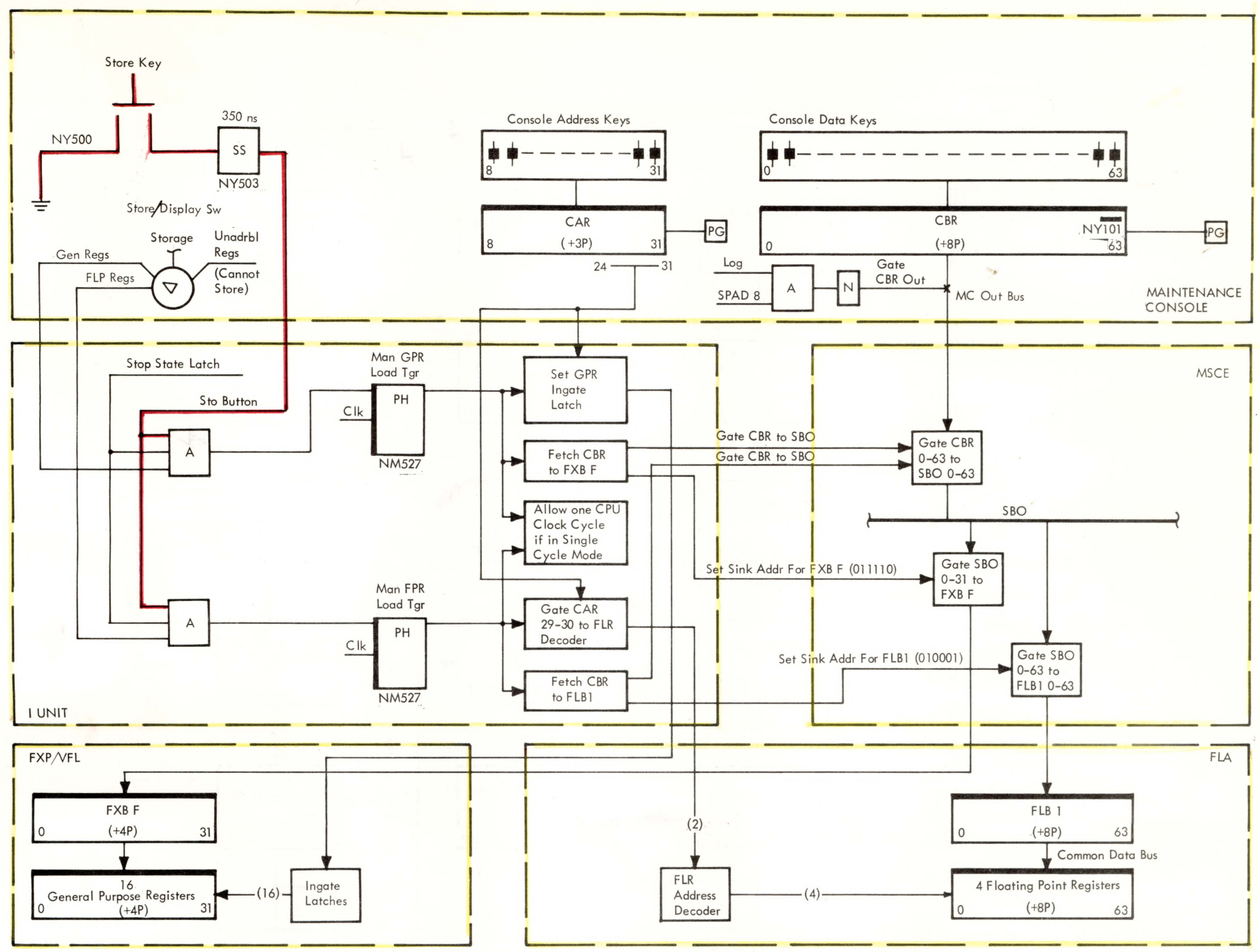


DIAGRAM 5-504. DISPLAY IN CBR (SHEET 3 OF 3)

Store Into GPR or FPR



Store Into GPR

Objective:
Store data from CBR into a selected GPR.

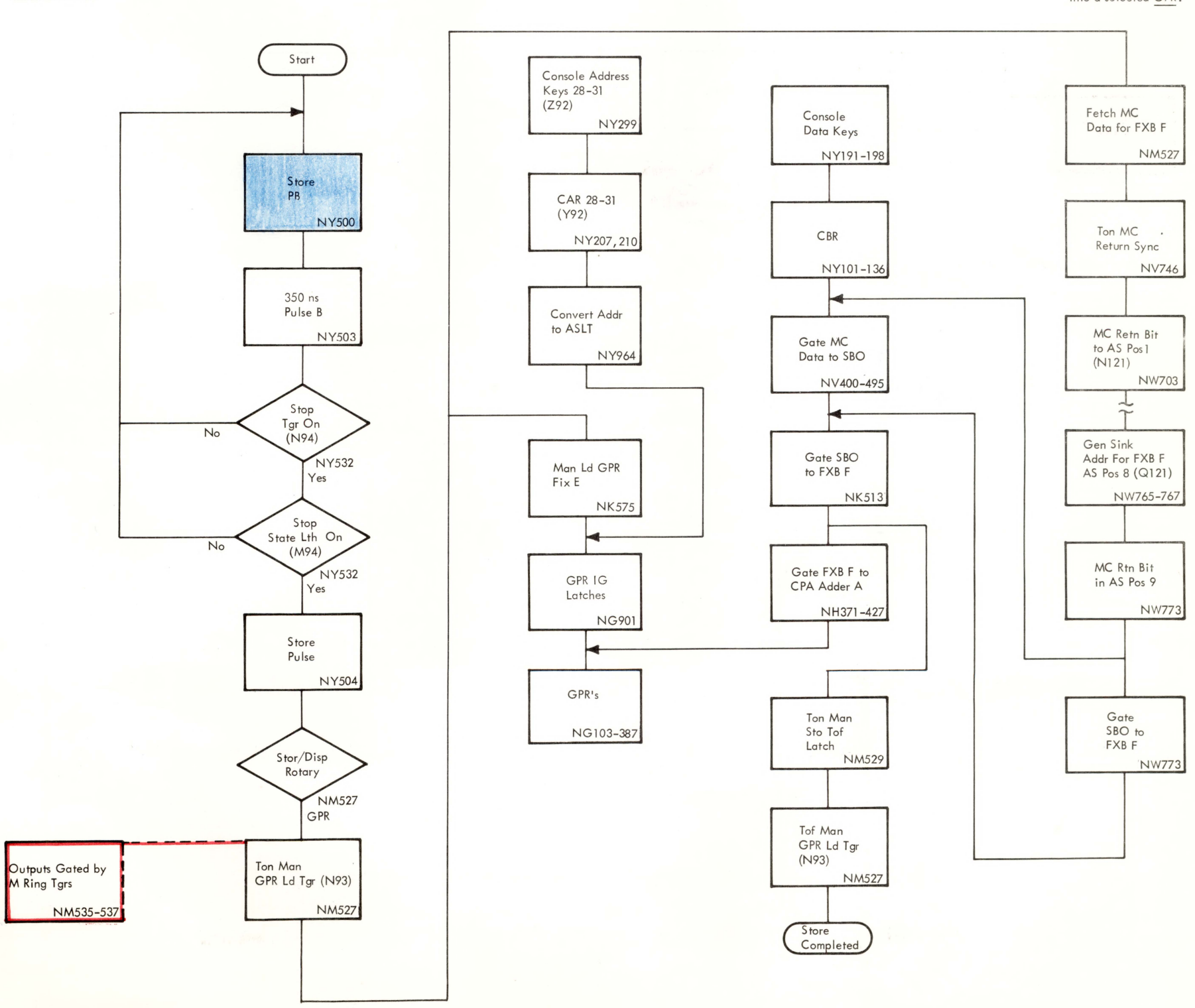


DIAGRAM 5-505. STORE (SHEET 1 OF 3)

Objective:
Store data from CBR into a selected FLR.

Store Into FPR

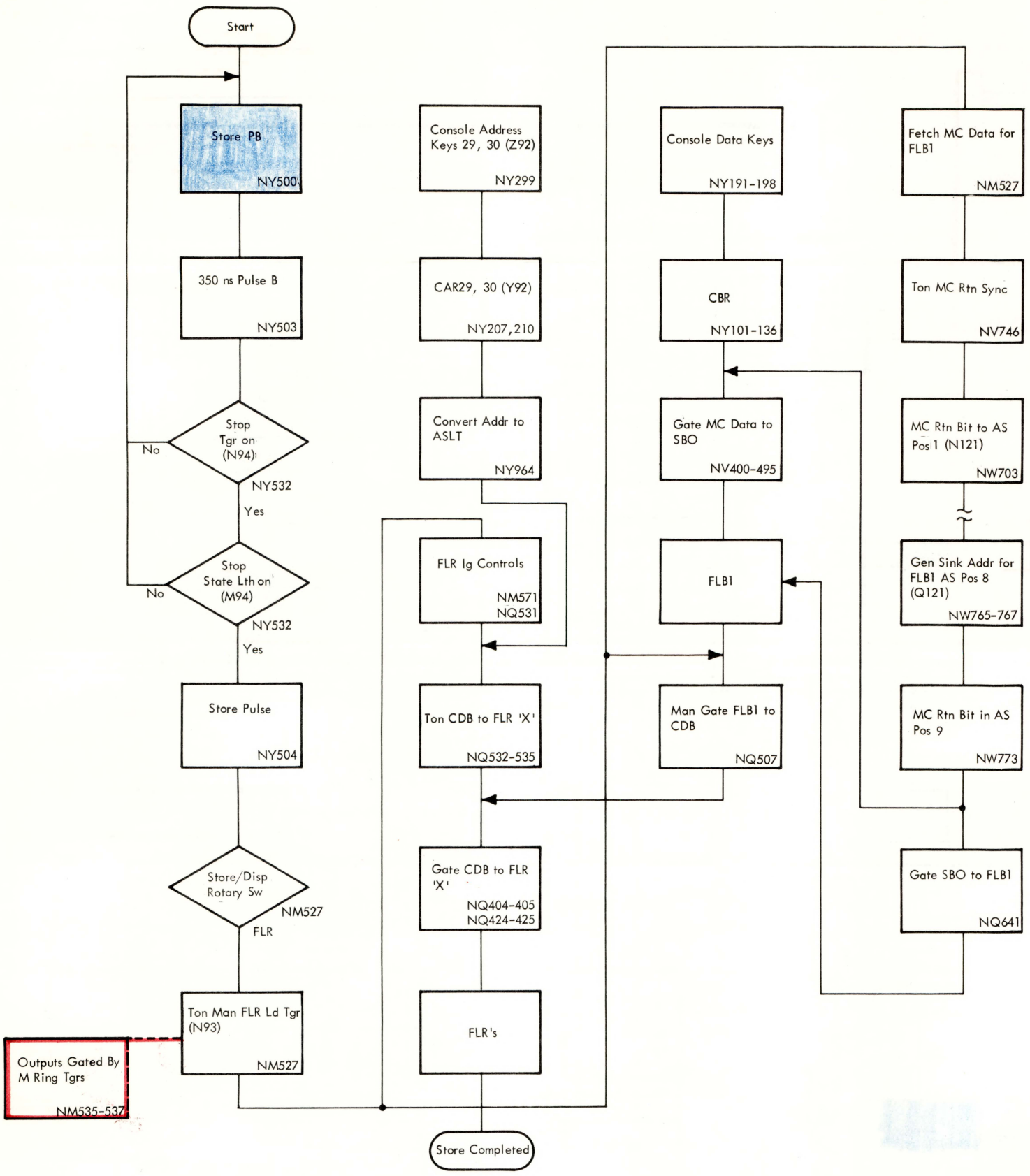
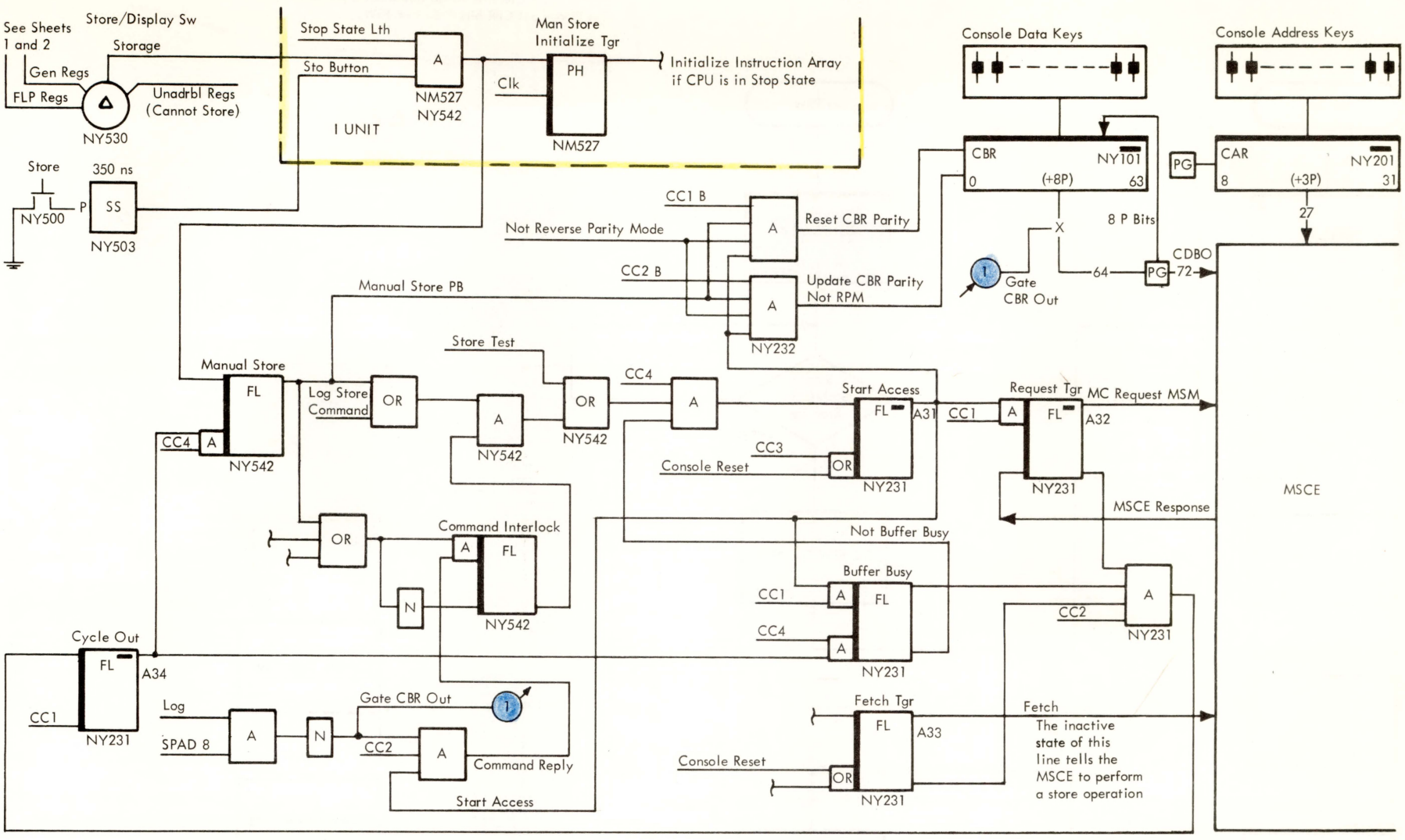


DIAGRAM 5-505. STORE (SHEET 2 of 3)

Store Into Storage



Objective:

Store contents of CBR into MWS or EMS.

Store Into Storage

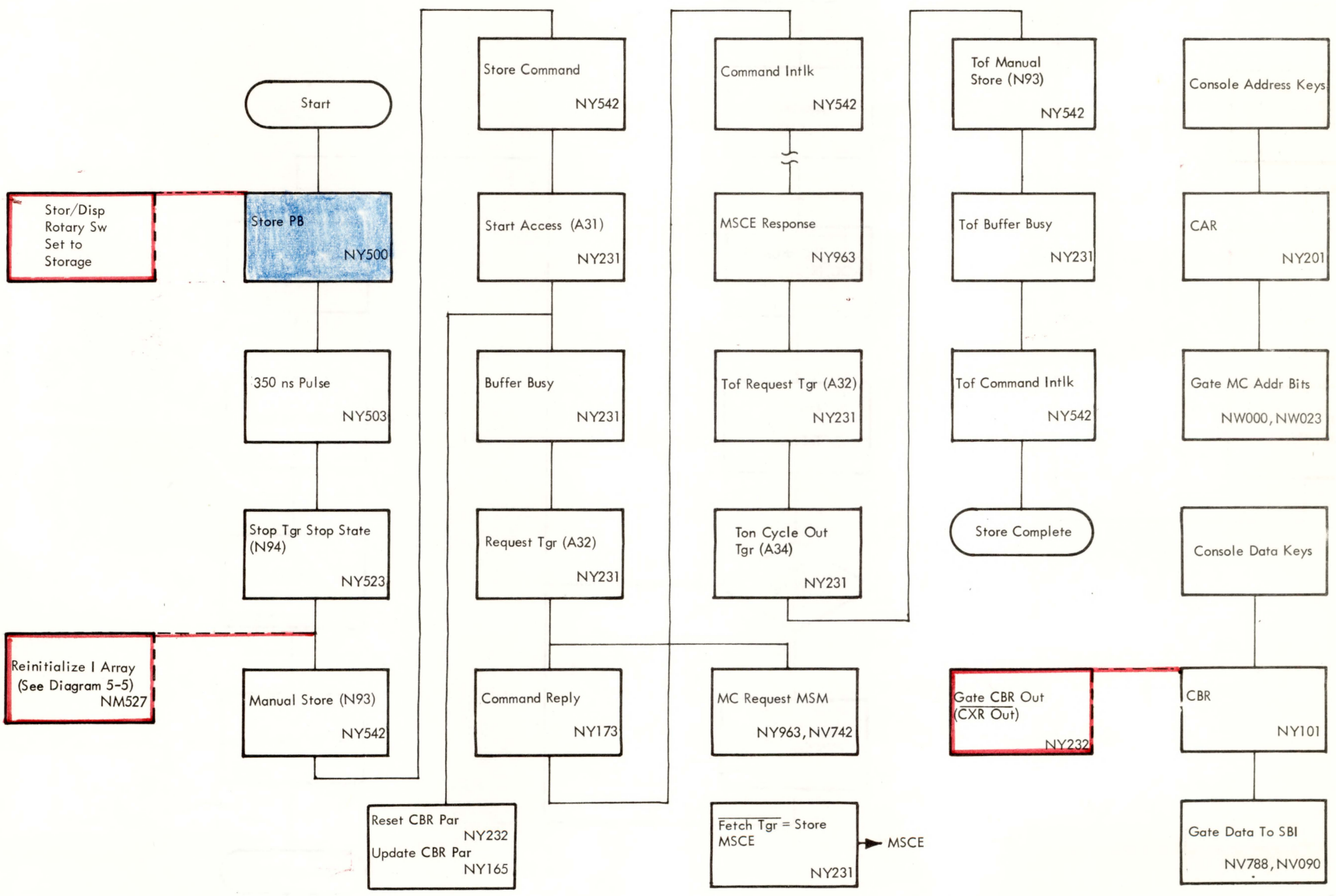


DIAGRAM 5-505. STORE (SHEET 3 OF 3)

Objective:
Set IC - Set CBR bits 40-63 into address portion of PSW.
Set PSW - Set CBR bits 0-63 into PSW.

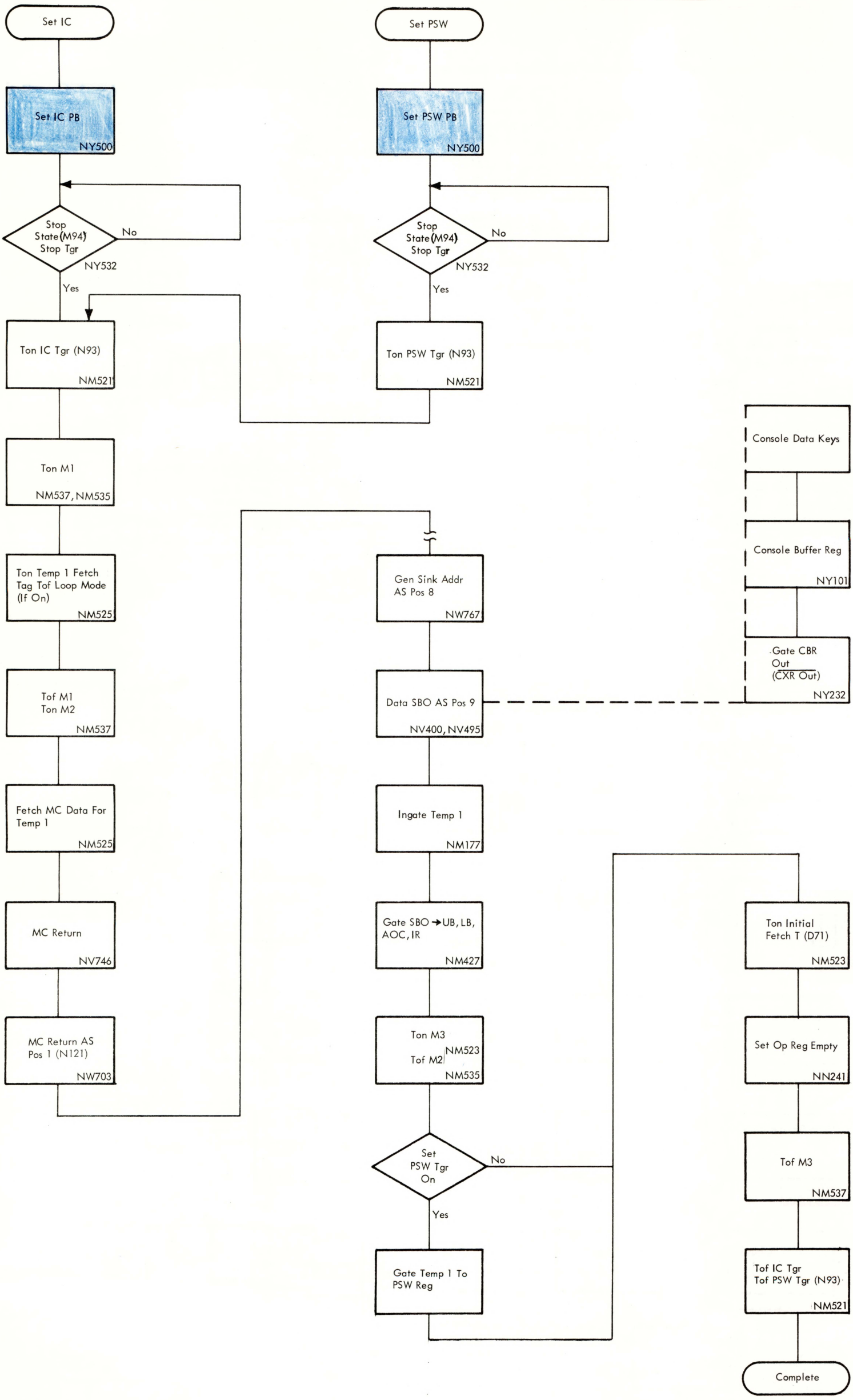


DIAGRAM 5-506. SET IC, SET PSW

Objectives:
Load 3 double words into MWS starting at location 00000 by use of load pushbutton.

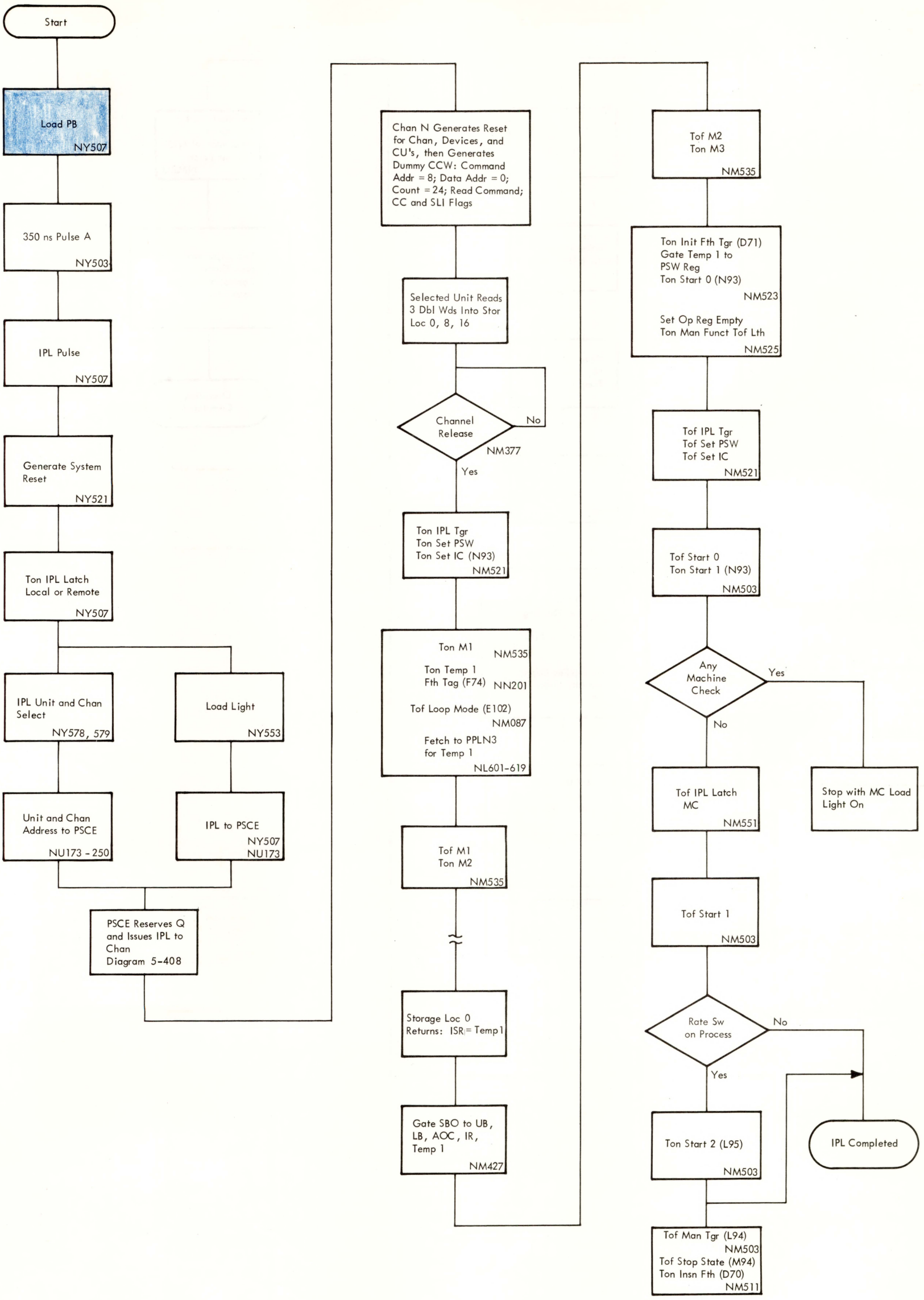


DIAGRAM 5-507. INITIAL PROGRAM LOAD

Objectives:
1. Fetch PSW to I Box from MWS location 00000.
2. Initialize I Box from this PSW and start processing.

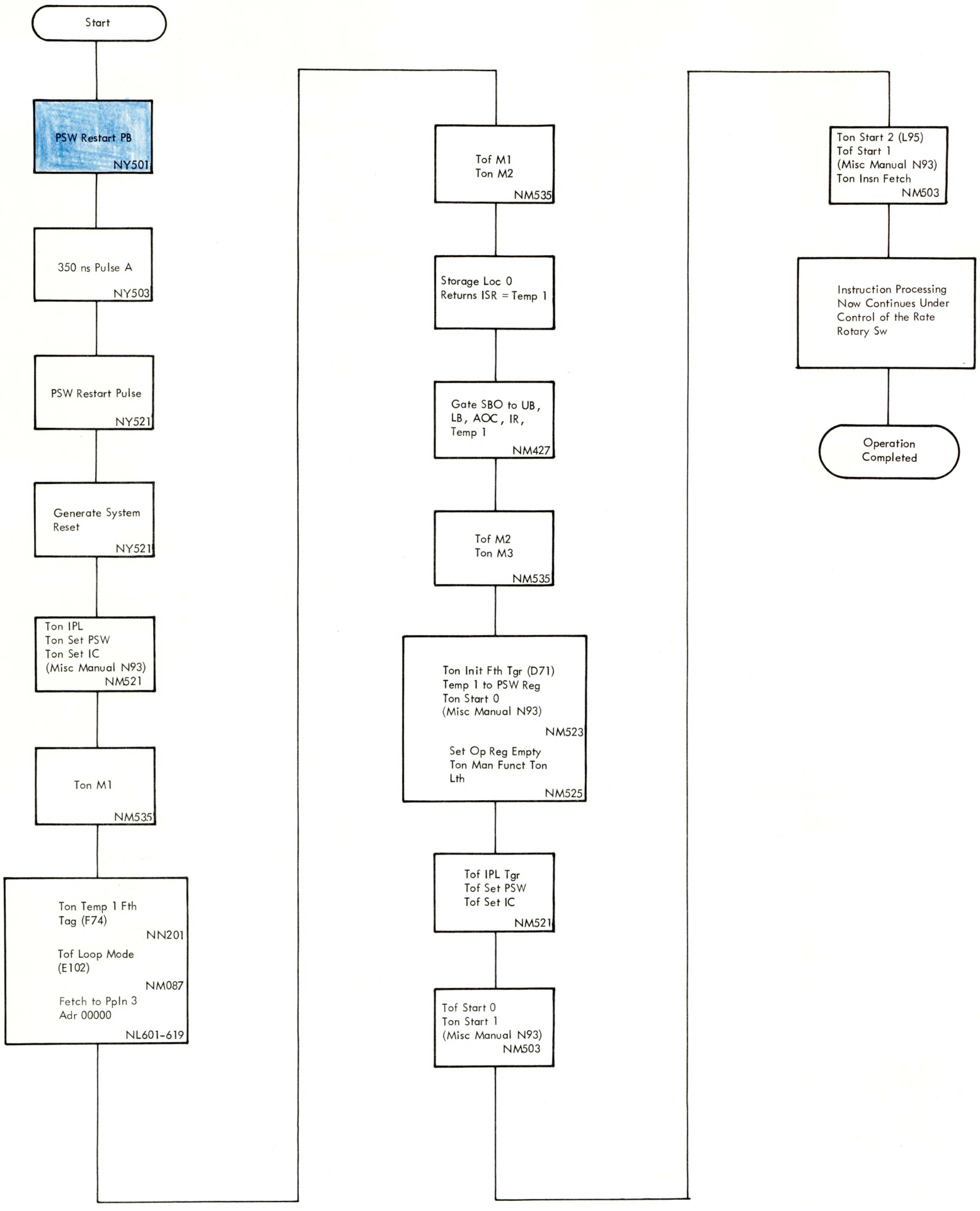


DIAGRAM 5-508. PSW RESTART

Objectives:
1. Execute instruction left justified in CBR.
2. Execute instruction in storage location specified by CBR 40-63.

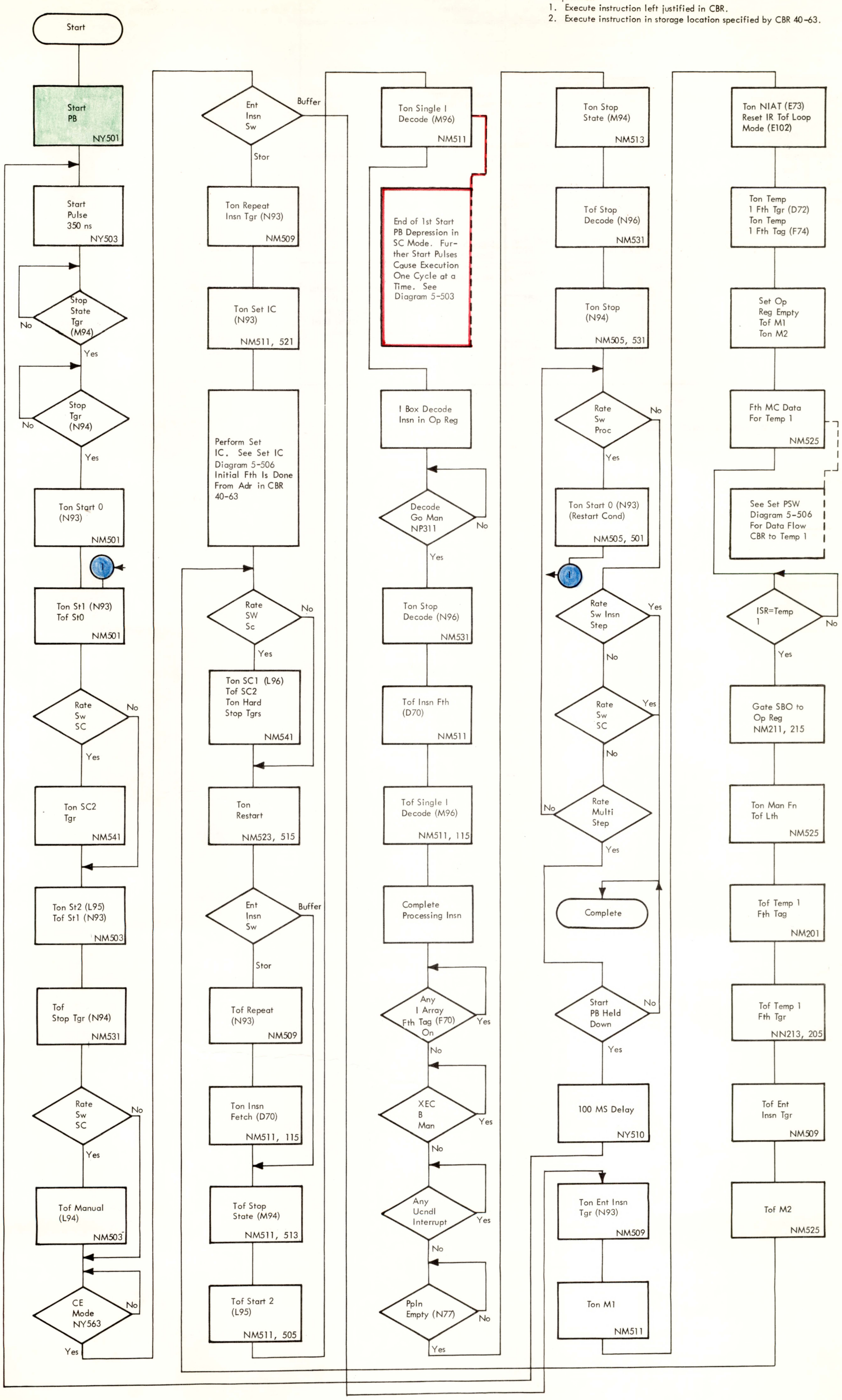


DIAGRAM 5-509. ENTER INSTRUCTION

Address Compare Switch Position		Start Key Action	Address Compare Condition	Action on Compare Condition	Action on CPC Equals 0
PROCESS		Normal CPU Start	MC Addr Keys Equal Address of Insn in Op Register	Scope Sync Only	CPC not Loaded or Stepped
Soft Stop	Insn			Scope Sync and Normal Stop	
	MSCE Store		MC Addr Keys Equal MSCE Storage Address on Store Operation (Can be MWS or EMS Req)		
	PSCE		PSCE Address Keys Equal Any Address Passing Through PSCE		
CPC Hard Stop	Insn	Computer Reset,* Set CPC/MCW Counter from CPC Switches, Load PSW Operation, Start	MC Addr Keys Equal Address of Insn in Op Reg	Scope Sync, Start Stepping CPC/MCW Counter (One Step per CPU Cycle)	Hard Stop
	MSCE Store		MC Addr Keys Equal MSCE Storage Address on Store Operation (Can be MWS or EMS Req)		
	PSCE		PSCE Address Keys Equal Any Address Passing Through PSCE		
CPC Loop	Insn		MC Addr Keys Equal Address of Insn in Op Reg		Hard Stop, Computer Reset*, Set CPC/MCW Counter from CPC Switches, Load PSW Operation, Start
	MSCE Store		MC Addr Keys Equal MSCE Storage Address on Store Operation (Can be MWS or EMS Req)		
	PSCE		PSCE Address Keys Equal Any Address Passing Through PSCE		

*On PSCE switch positions, PSCE is also reset.

DIAGRAM 5-510. ADDRESS COMPARE (SHEET 1 OF 2)

Objective: To show the Address Compare function of the MC.

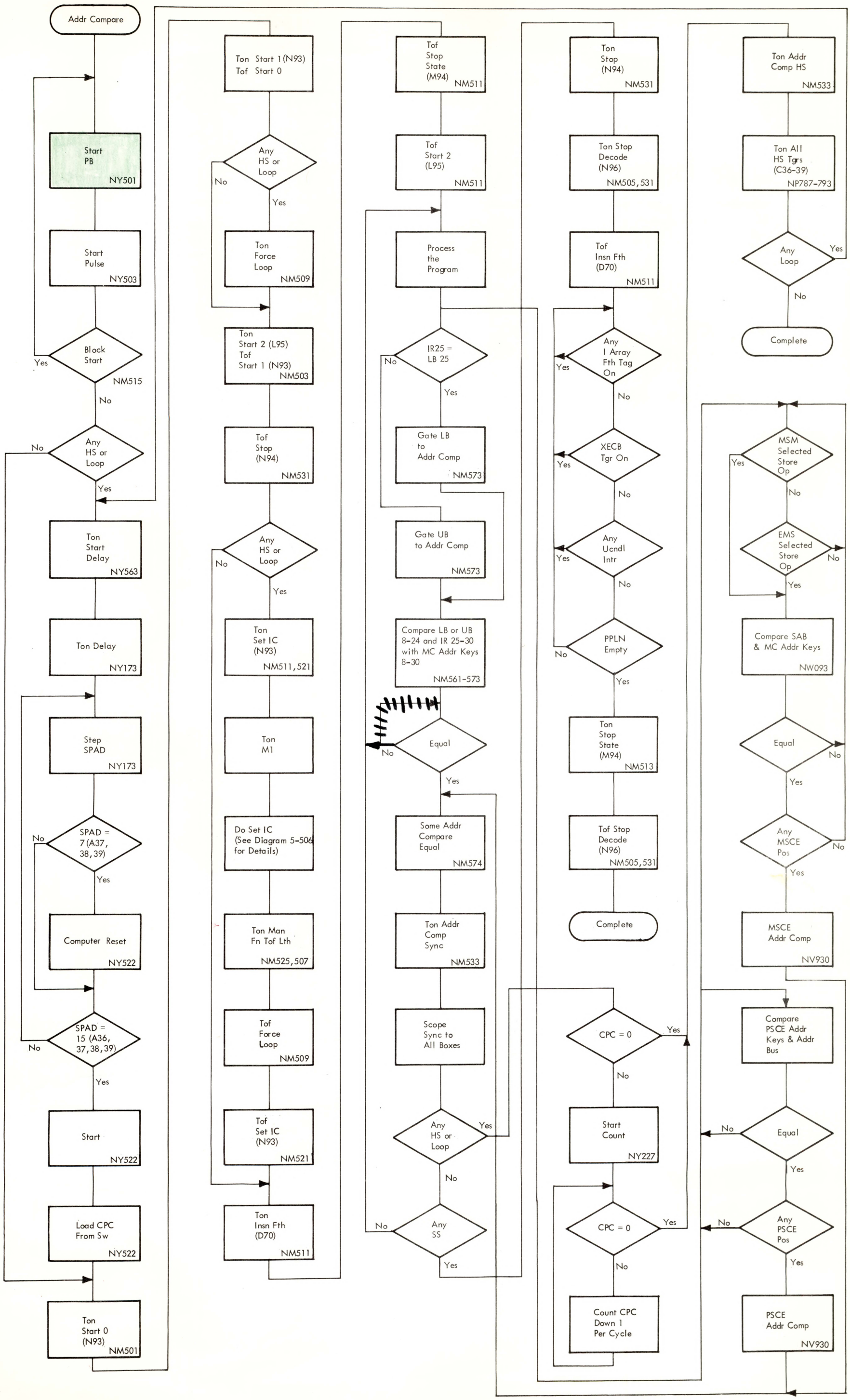
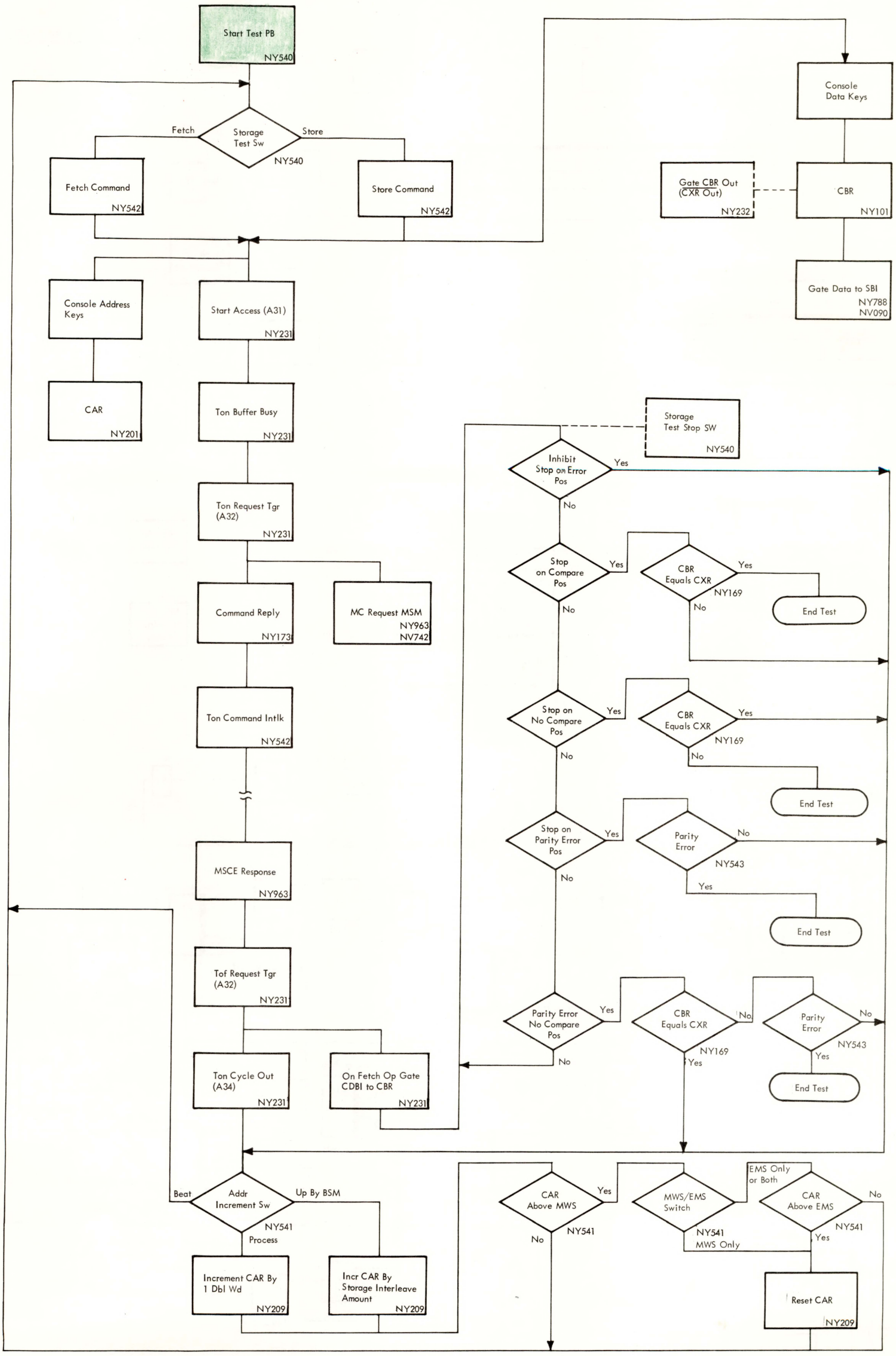


DIAGRAM 5-510. ADDRESS COMPARE (SHEET 2 OF2)

Objective:

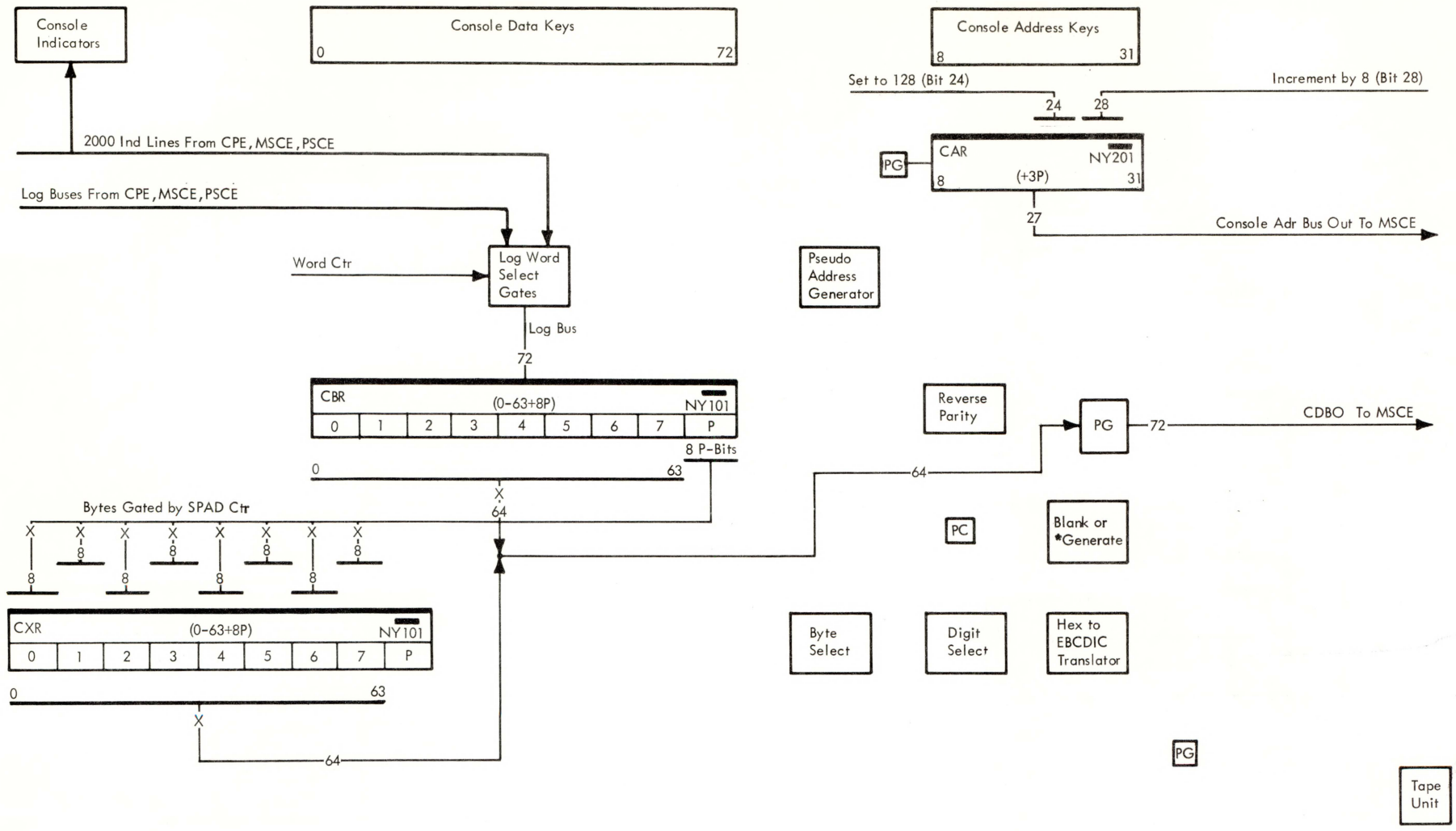
To manually load or fetch data to or from part or all of MWS or EMS and to check parity of such data.

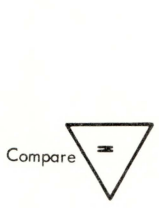


Note:
On compare or no compare, comparand is set into CBR and then set into CXR before test is begun.

DIAGRAM 5-511. STORAGE TEST

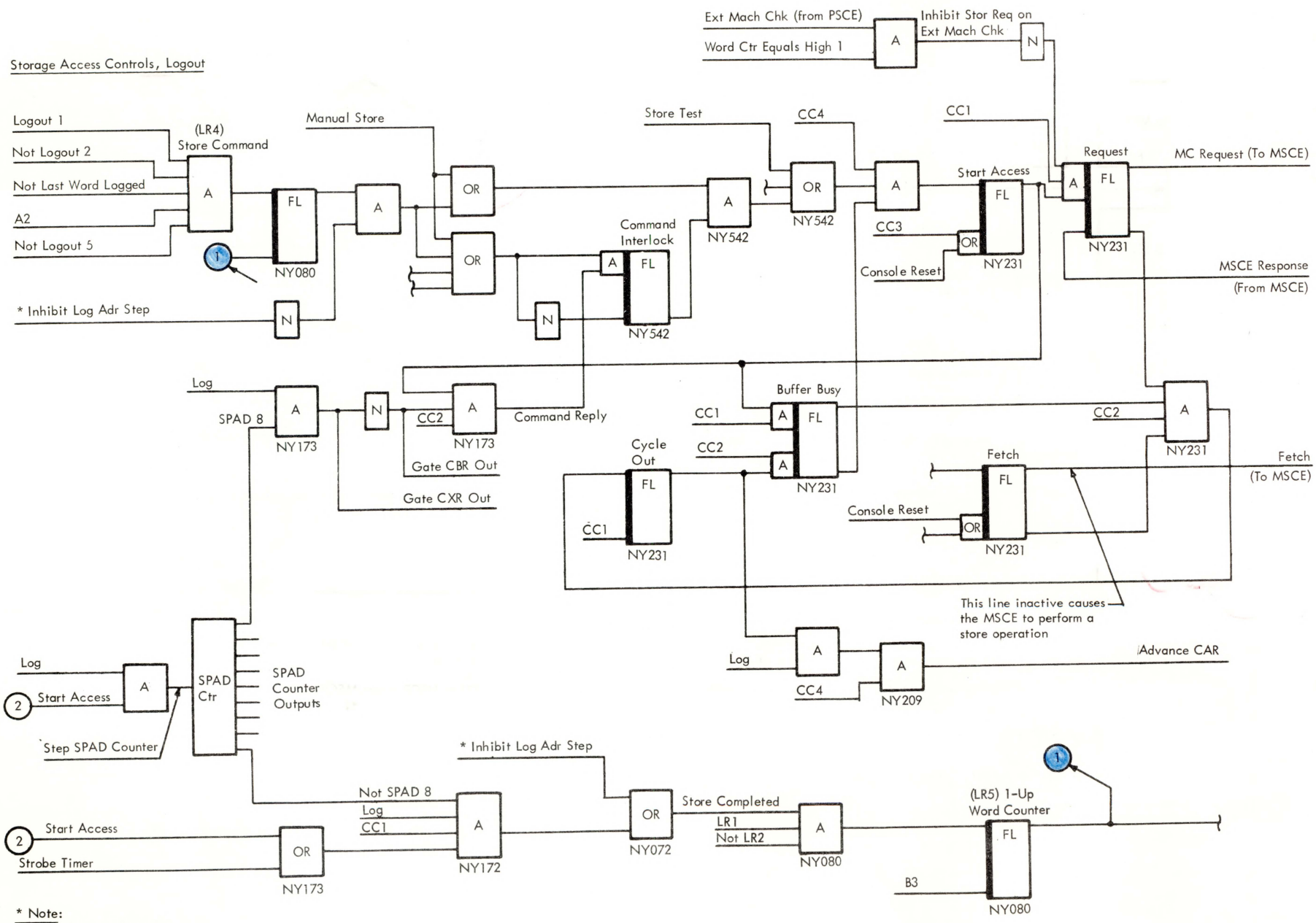
Logout Data Flow





LOG/SCAN CONTROLS	
Log Ring	– 6 Tgrs
SPAD Ctr	– 4 Tgrs
Word Ctr	– 8 Tgrs
Scan Ring	– 18 Tgrs
Command Ctr	– 3 Tgrs
Format Ring	– 16 Tgrs
Byte Ctr	– 3 Tgrs
Buffer Addr Ctr	– 12 Tgrs

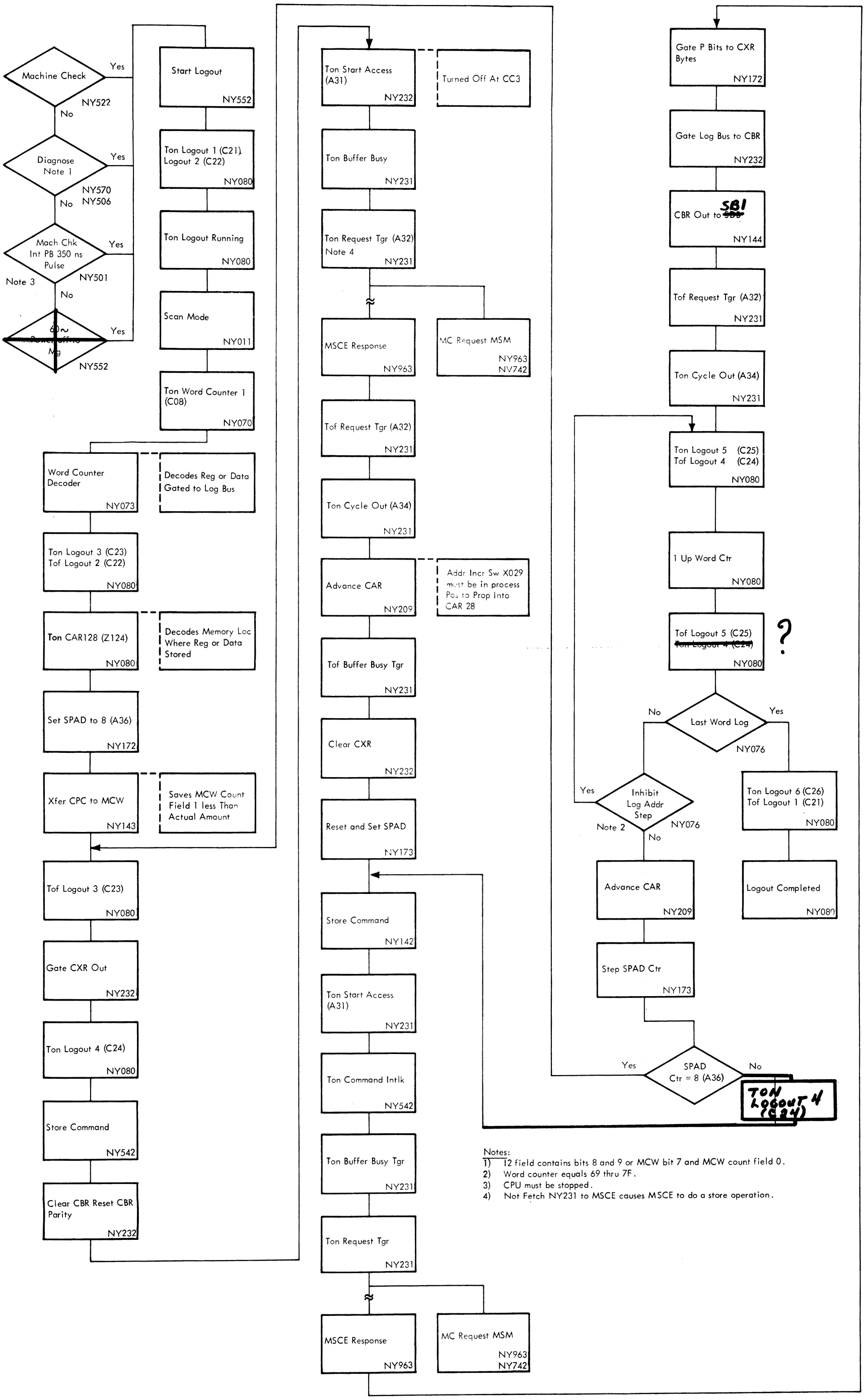
Storage Access Controls, Logout



* Note:
Active when word counter equals 69 to 7F.

DIAGRAM 5-512. LOGOUT (SHEET 1 OF 2)

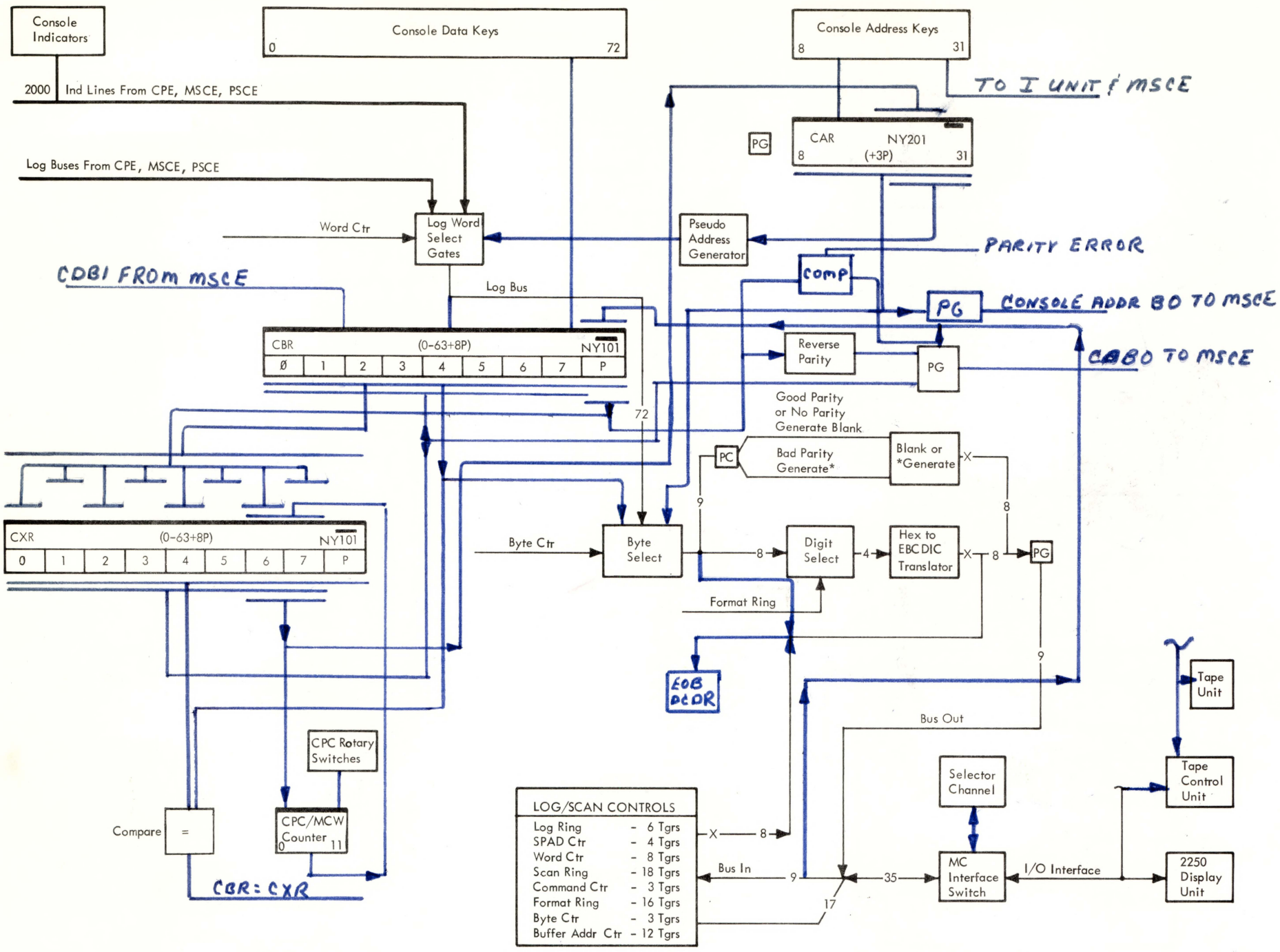
Objective:
To store 189 double words of machine status information into sequential storage locations starting at Hex 80.



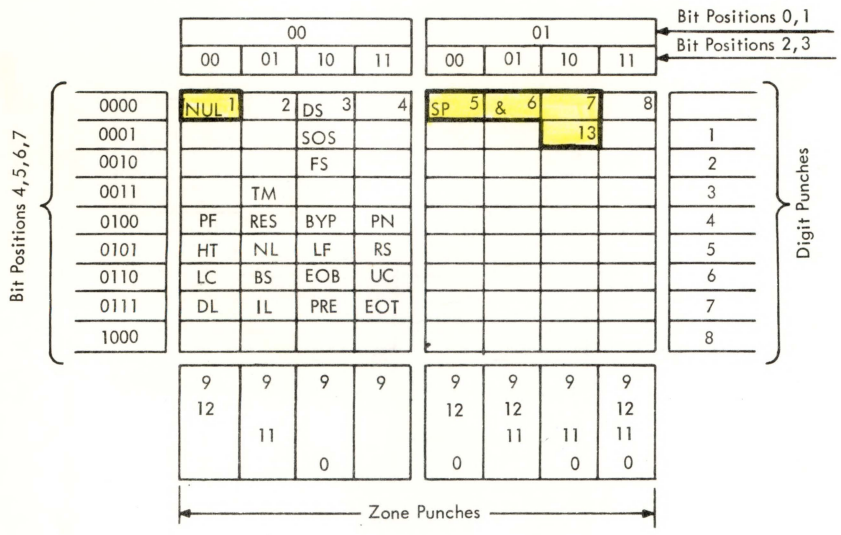
Notes:
1) 12 field contains bits 8 and 9 or MCW bit 7 and MCW count field 0.
2) Word counter equals 69 thru 7F.
3) CPU must be stopped.
4) Not Fetch NY231 to MSCE causes MSCE to do a store operation.

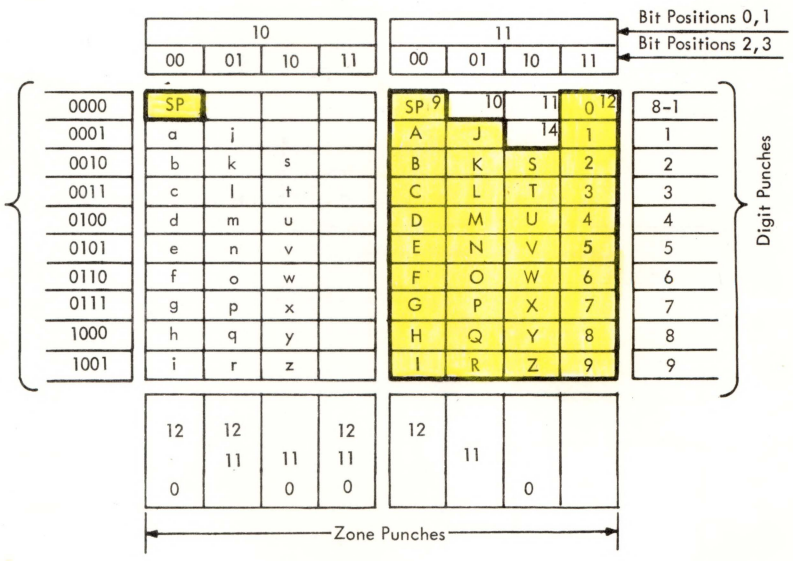
DIAGRAM 5-512. LOG OUT (SHEET 2 OF 2)

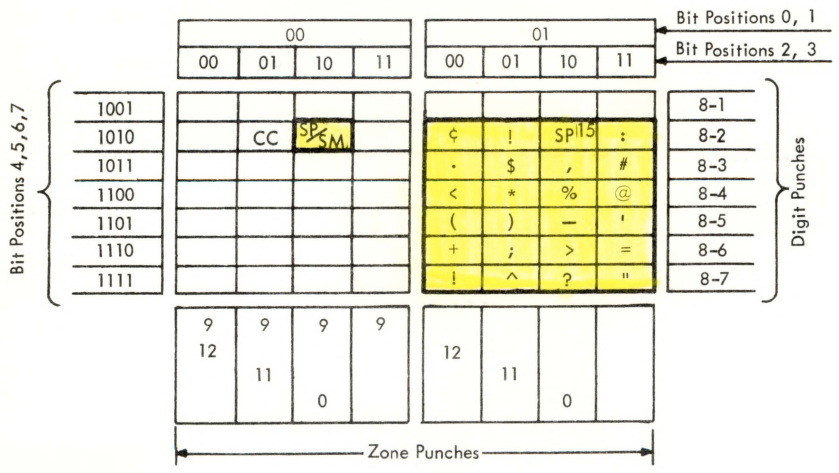
CRT Register Display Data Flow

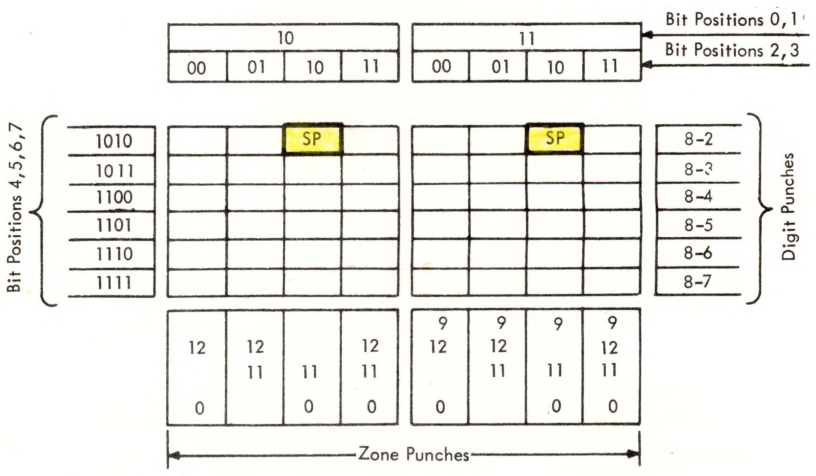


EBCDIC - 2250 Character Set









1 12-0-9-8-1
2 12-11-9-8-1
3 11-0-9-8-1
4 12-11-0-9-8-1
5 No Punches
6 12
7 11
8 12-11-0
9 12-0
10 11-0
11 0-8-2
12 0
13 0-1
14 11-0-9-1
15 12-11

Note:

Heavy outlines show 2250 character set

Control Characters

NUL	Null	BS	Backspace	EOB	End of Block
PF	Punch Off	IL	Idle	PRE	Prefix
HT	Horizontal Tab	CC	Cursor Control	PN	Punch On
LC	Lower Case	DS	Digit Select	RS	Reader Stop
DL	Delete	SOS	Start of Significance	UC	Upper Case
TM	Tape Mark	FS	Field Separator	EOT	End of Transmission
RES	Restore	BYP	Bypass	SM	Set Mode
NL	New Line	LF	Line Feed	SP	Space

DIAGRAM 5-513. CRT DISPLAY, CPE OR BUS REGISTERS (SHEET 1 OF 7)

Objective:
To display contents of CPU or storage control registers on CRT.

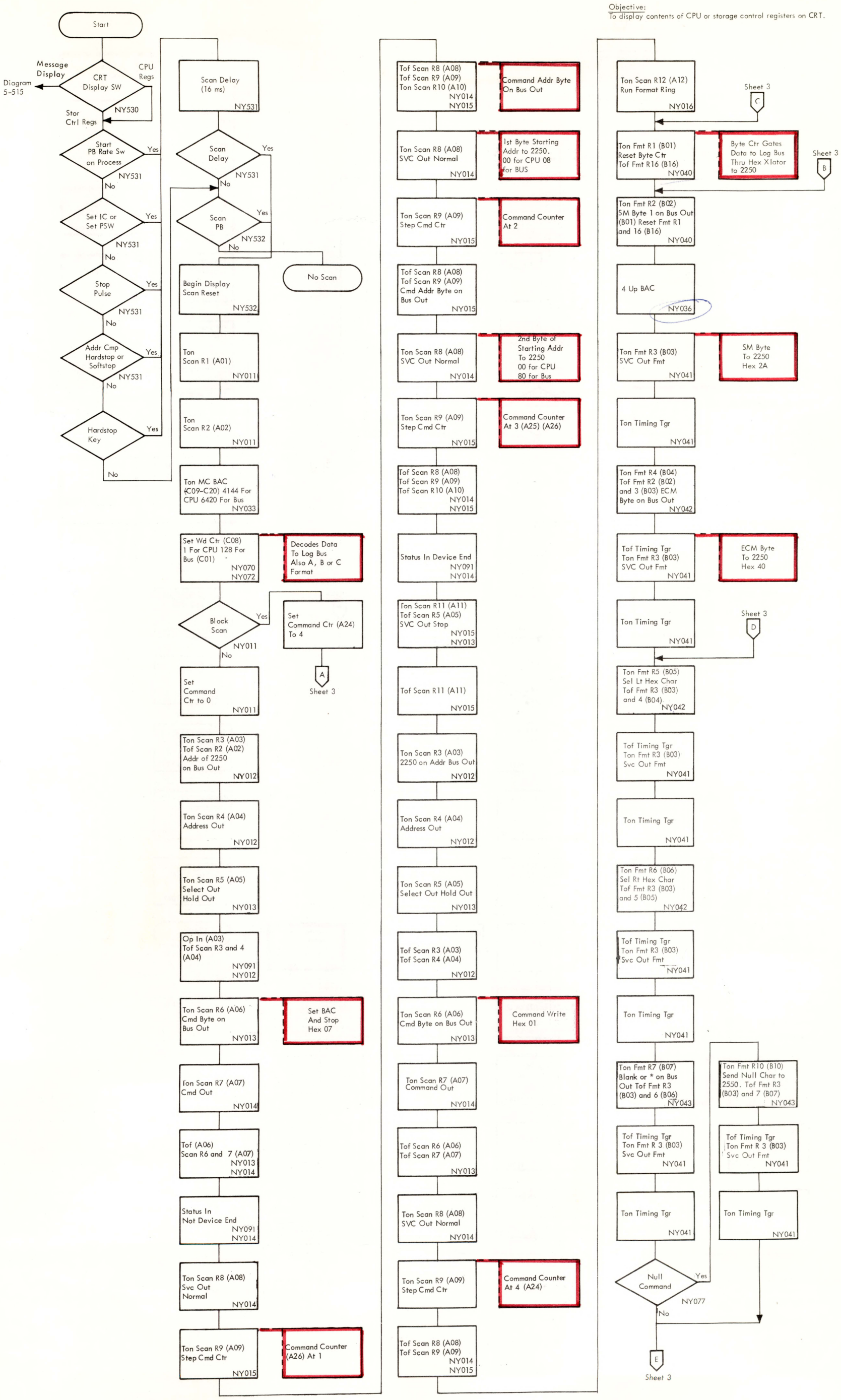


DIAGRAM 5-513. CRT DISPLAY, CPE OR BUS REGISTERS (SHEET 2 OF 7)

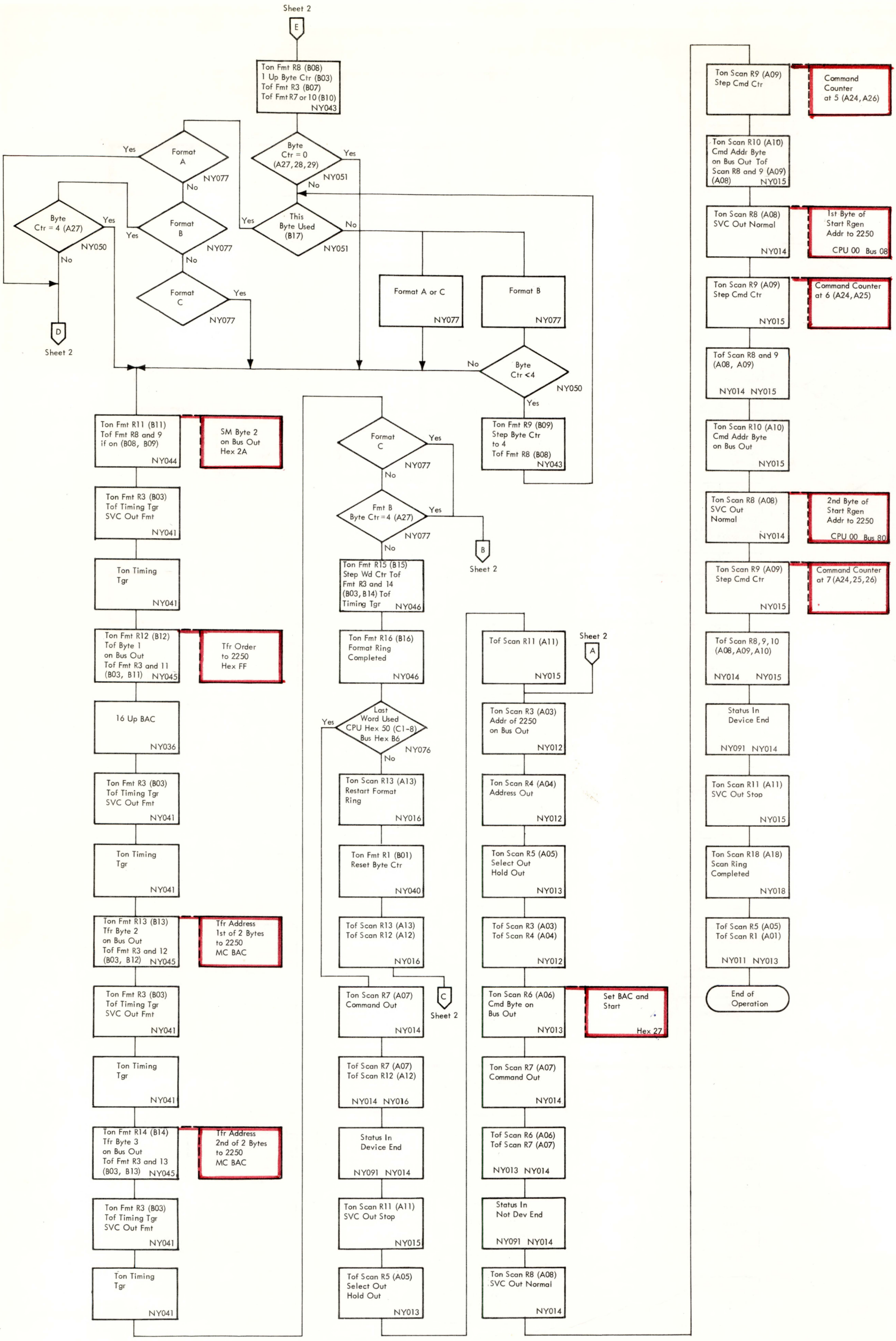


DIAGRAM 5-513. CRT DISPLAY, CPE OR BUS REGISTERS (SHEET 3 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC	Interface Signals 2250	Notes
Initial Selection	Scan Key or CPU Stop	1		16	Op Out	—	Scan mode to CPU or Bus. Set MC BAC*
	SR 1 (Scan Ring 1)	1,2	0	16	Op Out Note: Operational Out remains active as long as CRT Display rotary switch is not off.	—	Set Word Ctr to 1 for CPU scan or to 128 (Hex 80) for bus scan. Set Cmnd Ctr to 0 if block scan is off, or to 4 if block scan is on.
	SR 2	1,3	0	16	2250 Adr on Bus Out	—	Reset SR 18. Set Bus Gate Triggers if Bus display
	SR 3	1,3,4	0	16	2250 Adr on Bus Out Address Out	— —	
	SR 4	1,3,4,5	0	16	2250 Adr on Bus Out Address Out Sel Out/Hold Out	— — —	
	Operational In	1,5	0	16	Sel Out/Hold Out — Op In	—	
Send 'Set Buffer Address and Stop' Command to 2250	Address In	1,5,6	0	16	Sel Out/Hold Out — Op In — Adr In — 2250 Adr on Bus In Cmnd on Bus Out	—	Command is 'Set BAC and Stop' (Hex 07)
	SR 6	1,5,6,7	0	16	Sel Out/Hold Out — Op In — Adr In — 2250 Adr on Bus In Cmnd on Bus Out Command Out	— — —	
	Not Address In	1,5	0	16	Sel Out/Hold Out — Op In	—	
	Status In, Not Chan End, Not Dev End	1,5,8	0	16	Sel Out/Hold Out — Op In — Status Byte on Bus In — Status In Service Out	— —	
	Not Status In	1,5,8,9	1	16	Sel Out/Hold Out — Op In Service Out	— —	Step Command Counter
Send Command Address (2 bytes)	SR 9 Delayed	1,5,10	1	16	Sel Out/Hold Out — Op In Cmnd Adr Byte on Bus Out	— —	
	Service In	1,5,10,8	1	16	Sel Out/Hold Out — Op In Cmnd Adr Byte on Bus Out — Service In Service Out	— — —	First byte of starting address to 2250. First byte is high-order byte. Complete address: CPU Scan, 0000; Bus Scan, 2176 (Hex 0880).
	Not Service In	1,5,10,8,9	2	16	Sel Out/Hold Out — Op In Cmnd Adr Byte on Bus Out Service Out	— — —	Step Command Counter
	SR 9 Delayed	1,5,10	2	16	Sel Out/Hold Out — Op In Cmnd Adr Byte on Bus Out	— —	
	Service In	1,5,10,8	2	16	Sel Out/Hold Out — Op In Cmnd Adr Byte on Bus Out — Service In Service Out	— — —	Second byte of starting address to 2250
	Not Service In	1,5,10,8,9	3	16	Sel Out/Hold Out — Op In Cmnd Adr Byte on Bus Out Service Out	— — —	Step Command Counter
	SR 9 Delayed	1,5	3	16	— Op In	Sel Out/Hold Out —	
Ending Sequence (Receive Status Byte)	Status In, Chan End, Device End	1,5,11	3	16	Sel Out/Hold Out — Op In Service Out	— —	
	Not Status In	1	3	16	— Op In		
Initial Selection	Not Op In	1,3	3	16		2250 Adr on Bus Out —	
	SR 3	1,3,4	3	16		2250 Adr on Bus Out — Address Out —	
	SR 4	1,3,4,5	3	16		2250 Adr on Bus Out — Address Out — Sel Out/Hold Out —	
	Operational In	1,5	3	16	Sel Out/Hold Out — Op In	—	
Send 'Write' Command to 2250	Address In	1,5,6	3	16	Sel Out/Hold Out — Op In — Address In Cmnd Byte on Bus Out	— —	Command is 'Write' (Hex 01)
	SR 6	1,5,6,7	3	16	Sel Out/Hold Out — Op In — Address In Cmnd Byte on Bus Out Command Out	— — —	
	Not Address In	1,5	3	16	Sel Out/Hold Out — Op In	— 	
	Status In	1,5,8	3	16	Sel Out/Hold Out — Op In — Status In — Status Byte on Bus In Service Out	— —	
	Not Status In	1,5,8,9	4	16	Sel Out/Hold Out — Op In Service Out	— —	Step Command Counter
	Reset SR 8, SR 9	1,5	4	16	Sel Out/Hold Out — Op In	— 	
	Service In	1,5,12	4	16	Sel Out/Hold Out — Op In — Service In	— 	Start Format Ring

Scan Ring

1 Scan Run
2 Counter Reset
3 2250 Address
4 Address Out
5 Sel/Hold Out
6 Command Byte
7 Command Out
8 Service Out
9 Step Cmnd Ctr
10 Command Address
11 Service Out Stop
12 Run Format Ring

Command Counter

0 Set BAC and Stop Cmnd
1 Write starting adr (byte 1)
2 Write starting adr (byte 2)
3 Write Command
4 Start Regen (set BAC and Start)

Format Ring

16 Format Ring Completed

* Buffer Address Counter (BAC):
CPU Scan, set to 4144 (Hex 1030)
Bus Scan, set to 6420 (Hex 1914)

DIAGRAM 5-513. CRT DISPLAY, CPE OR BUS REGISTERS (SHEET 4 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC	Interface Signals 2250	Notes
Send SM and ECM Bytes to 2250	SR 12	1,5,12	4	1,16	—— Op In —— Service In	Sel Out/Hold Out ——	Reset Byte Counter
	FR 1 (Format Ring 1)	1,5,12	4	2	—— Op In —— Service In	Sel Out/Hold Out —— SM Byte on Bus Out ——	BAC incremented by 4 (FR 2)*
	FR 2	1,5,12	4	2,3	—— Op In —— Service In	Sel Out/Hold Out —— Service Out —— SM Byte on Bus Out ——	Send SM Byte to 2250 (Hex 2A)
	Not Service In	1,5,12	4	2,3,T	—— Op In	Sel Out/Hold Out —— Service Out —— SM Byte on Bus Out ——	
	Timing Trigger	1,5,12	4	4,T	—— Op In	Sel Out/Hold Out —— ECM Byte on Bus Out ——	
	Service In	1,5,12	4	4,3	—— Op In —— Service In	Sel Out/Hold Out —— ECM Byte on Bus Out —— Service Out ——	Send ECM Byte to 2250 (Hex 40)
	Not Service In	1,5,12	4	4,3,T	—— Op In	Sel Out/Hold Out —— ECM Byte on Bus Out —— Service Out ——	

*BAC is incremented by 20 in two steps, first by 4 and then by 16.

Send Left Hex Char to 2250	Timing Trigger	1,5,12	4	5,T	—— Op In	Sel Out/Hold Out —— Left Hex Char on Bus Out ——	
	Service In	1,5,12	4	5,3	—— Op In —— Service In	Sel Out/Hold Out —— Service Out —— Left Hex Char on Bus Out ——	
	Not Service In	1,5,12	4	5,3,T	—— Op In	Sel Out/Hold Out —— Service Out —— Left Hex Char on Bus Out ——	
Send Right Hex Char to 2250	Timing Trigger	1,5,12	4	6,T	—— Op In	Sel Out/Hold Out —— Right Hex Char on Bus Out ——	
	Service In	1,5,12	4	6,3	—— Op In —— Service In	Sel Out/Hold Out —— Service Out —— Right Hex Char on Bus Out ——	
	Not Service In	1,5,12	4	6,3,T	—— Op In	Sel Out/Hold Out —— Service Out —— Right Hex Char on Bus Out ——	
Send Blank or Asterisk to 2250	Timing Trigger	1,5,12	4	7,T	—— Op In	Sel Out/Hold Out —— Blank or Asterisk on Bus Out ——	
	Service In	1,5,12	4	7,3	—— Op In —— Service In	Sel Out/Hold Out —— Service Out —— Blank or Asterisk on Bus Out ——	
	Not Service In	1,5,12	4	7,3,T	—— Op In	Sel Out/Hold Out —— Service Out —— Blank or Asterisk on Bus Out ——	
Send Null Character to 2250	Timing Trigger	1,5,12	4	10,T	—— Op In	Sel Out/Hold Out —— Null on Bus Out ——	
	Service In	1,5,12	4	10,3	—— Op In —— Service In	Sel Out/Hold Out —— Service Out —— Null on Bus Out ——	
	Not Service In	1,5,12	4	10,3,T	—— Op In	Sel Out/Hold Out —— Service Out —— Null on Bus Out ——	
One-up Byte Counter	Timing trigger and blank or asterisk on bus out, or timing trigger and null on bus out	1,5,12	4	8,T	—— Op In	Sel Out/Hold Out ——	
Set Byte Counter to 4	FR 8, Format B, byte counter less than 4, this byte not used	1,5,12	4	9	—— Op In	Sel Out/Hold Out ——	

Scan Ring

1 Scan Run
5 Sel/Hold Out
12 Run Format

Command Counter

4 Start Regen Cmnd (Set BAC and Start)

Format Ring

1 Reset Byte Ctr
2 Set Mode Cmnd 1
3 Service Out Format
4 ECM Command
5 Sel Left Hex Char
6 Sel Right Hex Char
7 Blank or Asterisk
8 Step Byte Counter
9 Byte Ctr to 4
10 Null on Bus Out
11 Set Mode Cmnd 2
12 Transfer
13 Transfer Adr 1
16 Format Completed
T Timing Trigger

DIAGRAM 5-513. CRT DISPLAY, CPE OR BUS REGISTERS (SHEET 5 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC	Interface Signals 2250	Notes
Send Transfer Order and two address bytes to 2250	FR 8 or 9	1,5,12	4	11	—— Op In	Sel Out/Hold Out —— SM Byte on Bus Out ——	
	Service In	1,5,12	4	11,3	—— Op In —— Service In	Sel Out/Hold Out —— SM Byte on Bus Out —— Service Out ——	Send SM Byte to 2250 (Hex 2A)
	Not Service In	1,5,12	4	11,3,T	—— Op In	Sel Out/Hold Out —— SM Byte on Bus Out —— Service Out ——	
	Timing trigger	1,5,12	4	12,T	—— Op In	Sel Out/Hold Out —— Transfer Byte 1 on Bus Out ——	BAC Incremented by 16 (FR12)
	Service In	1,5,12	4	12,3	—— Op In —— Service In	Sel Out/Hold Out —— Transfer Byte 1 on Bus Out —— Service Out ——	Send Transfer Order to 2250 (Hex FF)
	Not Service In	1,5,12	4	12,3,T	—— Op In	Sel Out/Hold Out —— Transfer Byte 1 on Bus Out —— Service Out ——	
	Timing trigger	1,5,12	4	13,T	—— Op In	Sel Out/Hold Out —— Transfer Byte 2 on Bus Out ——	
	Service In	1,5,12	4	13,3	—— Op In —— Service In	Sel Out/Hold Out —— Transfer Byte 2 on Bus Out —— Service Out ——	Send transfer address (first of two bytes) to 2250. MC BAC is stored in 2250 storage. First byte is high order; second is low order.
	Not Service In	1,5,12	4	13,3,T	—— Op In	Sel Out/Hold Out —— Transfer Byte 2 on Bus Out —— Service Out ——	
	Timing trigger	1,5,12	4	14,T	—— Op In	Sel Out/Hold Out —— Transfer Byte 3 on Bus Out ——	
	Service In	1,5,12	4	14,3	—— Op In —— Service In	Sel Out/Hold Out —— Transfer Byte 3 on Bus Out —— Service Out ——	Send transfer address (second of two bytes) to 2250. This is the low-order eight bits of MC BAC.
	Not Service In	1,5,12	4	14,3T	—— Op In	Sel Out/Hold Out —— Transfer Byte 3 on Bus Out —— Service Out ——	
One-up Word Counter, Restart Format Ring	Timing trigger	1,5,12	4	15,T	—— Op In	Sel Out/Hold Out ——	Step Word Counter
	Not timing trigger	1,5,12	4	16	—— Op In	Sel Out/Hold Out ——	Format ring completed
	FR 16	1,5,13	4	16	—— Op In	Sel Out/Hold Out ——	Restart format ring
	SR 13	1,5,12	4	1	—— Op In	Sel Out/Hold Out ——	Run format ring. Reset byte counter.
One-up Word Counter (Last Word Used)	Timing trigger	1,5,12	4	15,T	—— Op In	Sel Out/Hold Out ——	Last Word Count: CPU, 80 (Hex 50) Bus, 182 (Hex B6)
	Not timing trigger	1,5,12	4	16	—— Op In	Sel Out/Hold Out ——	
Signal End of Data to 2250	Service In	1,5,12,7	4	16	—— Op In —— Service In	Sel Out/Hold Out —— Command Out ——	Command Out causes 2250 to drop Service In and send Status In with Channel End and Device End
Ending Sequence	Not Service In	1,5	4	16	—— Op In	Sel Out/Hold Out ——	
	Status In, Chan End, Device End	1,5,11	4	16	—— Op In —— Status Byte on Bus In —— Status In	Sel Out/Hold Out —— Service Out ——	
	SR 11	1,11	4	16	—— Op In —— Status Byte on Bus In —— Status In	Service Out ——	
	Not Status In	1	4	16	—— Op In		
Send Start Regeneration Command to 2250	Not Operational In	1,3	4	16		2250 Adr on Bus Out ——	
	SR 3	1,3,4	4	16		2250 Adr on Bus Out —— • Address Out ——	
	SR 4	1,3,4,5	4	16		2250 Adr on Bus Out —— Address Out —— Sel Out/Hold Out ——	
	Operational In	1,5	4	16	—— Op In	Sel Out/Hold Out ——	
	Address In	1,5,6	4	16	—— Op In —— Address In	Sel Out/Hold Out —— Cmnd Byte on Bus Out ——	Command Byte: Set Buffer Address and Start (Hex 27)
	SR 6	1,5,6,7	4	16	—— Op In —— Address In	Sel Out/Hold Out —— Cmnd Byte on Bus Out —— Command Out ——	

Scan Ring

1 Scan Run
3 2250 Address
4 Address Out
5 Sel/Hold Out
6 Command Byte
7 Command Out
8 Service Out
11 Service Out Stop
12 Run Format
13 Restart Format

Command Counter

4 Start Regen Command (Set BAC and Start)

Format Ring

3 Service Out Format
11 Set Mode Cmnd 2
12 Transfer
13 Transfer Adr 1
14 Transfer Adr 2
15 Step Word Counter
16 Format Completed
T Timing Trigger

DIAGRAM 5-513. CRT DISPLAY, CPE OR BUS REGISTERS (SHEET 6 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC — 2250	Notes
Send Start Regeneration Command to 2250 (continued)	Not Address In	1,5	4	16	Sel Out/Hold Out — — Op In	
	Status In, Not Chan End, Not Device End	1,5,8	4	16	Sel Out/Hold Out — — Op In — Status In — Status Byte on Bus In Service Out —	
	Not Status In	1,5,8,9	5	16	Sel Out/Hold Out — — Op In Service Out —	Step Command Counter
Send Command Address (2 Bytes) to 2250	SR 9 Delayed	1,5,10	5	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte on Bus Out —	
	Service In	1,5,10,8	5	16	Sel Out/Hold Out — — Op In — Service In Cmnd Adr Byte on Bus Out — Service Out —	First byte of start regeneration address to 2250. First byte is high-order byte. Complete Address: CPU Scan, 0000 Bus Scan, 2176 (Hex 0880).
	Not Service In	1,5,10,8,9	6	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte on Bus Out — Service Out —	Step Command Counter
	SR 9 Delayed	1,5,10	6	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte (2) on Bus Out —	
	Service In	1,5,10,8	6	16	Sel Out/Hold Out — — Op In — Service In Cmnd Adr Byte (2) on Bus Out — Service Out —	Second byte of start regeneration address to 2250
	Not Service In	1,5,10,8,9	7	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte (2) on Bus Out — Service Out —	Step Command Counter
	SR 9 Delayed	1,5	7	16	Sel Out/Hold Out — — Op In	
Ending Sequence (End of Scan)	Status In, Chan End, Device End	1,5,11	7	16	Sel Out/Hold Out — — Op In — Status Byte on Bus In — Status In Service Out —	
	SR 11	1,5,11,18	7	16	Sel Out/Hold Out — — Op In — Status Byte on Bus In — Status In Service Out —	
	SR 18	11,18	7	16	— Op In — Status Byte on Bus In — Status In Service Out —	
	Not Status In	18	7	16		End of Operation

Scan Ring

1 Scan Run
2 Counter Reset
3 2250 Address
4 Address Out
5 Sel/Hold Out
6 Command Byte
7 Command Out
8 Service Out
9 Step Cmnd Ctr
10 Command Address
11 Service Out Stop
12 Run Format
13 Restart Format
18 Scan Ring Completed

Command Counter

0 Set BAC and Stop Cmnd
1 Write starting adr (byte 1)
2 Write starting adr (byte 2)
3 Write Command
4 Start Regen Command (Set BAC and Start)
5 Start Regen Adr (byte 1)
6 Start Regen Adr (byte 2)
7 Unused

Format Ring

1 Reset Byte Ctr
2 Set Mode Cmnd 1
3 Service Out Format
4 ECM Command
5 Sel Left Hex Char
6 Sel Right Hex Char
7 Blank or Asterisk
8 Step Byte Counter
9 Byte Ctr to 4
10 Null on Bus Out
11 Set Mode Cmnd 2
12 Transfer
13 Transfer Adr 1
14 Transfer Adr 2
15 Step Word Counter
16 Format Completed
T Timing Trigger

DIAGRAM 5-513. CRT DISPLAY, CPE OR BUS REGISTERS (SHEET 7 OF 7)

CRT Storage Display Data Flow

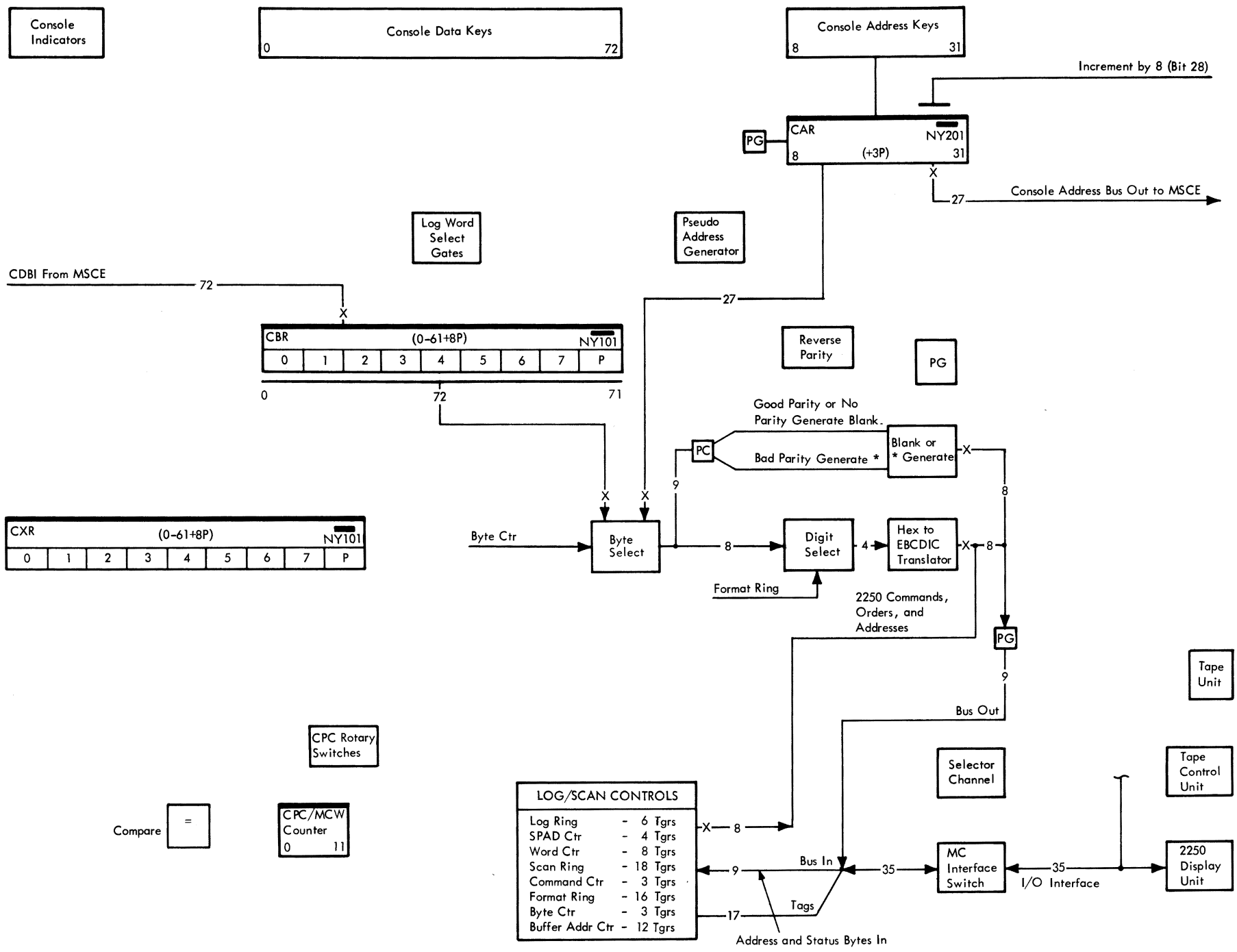


DIAGRAM 5-514. CRT STORAGE DISPLAY (SHEET 1 OF 7)

Objective

To display 16 doublewords of MWS or EMS on CRT.

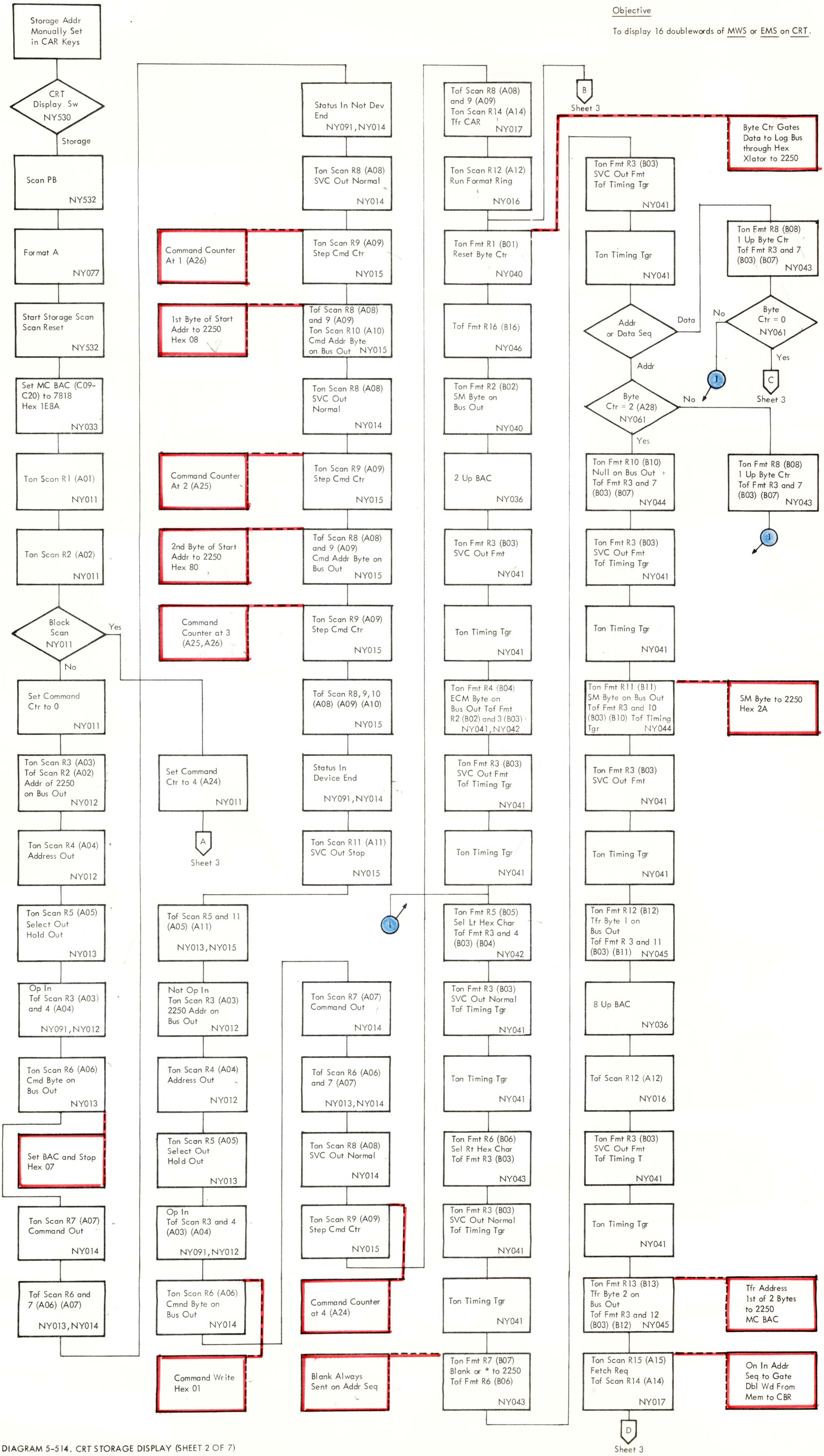


DIAGRAM 5-514. CRT STORAGE DISPLAY (SHEET 2 OF 7)

Sheet 2

D

Ton Fmt R 3 (B03) Svc Out Fmt Tof Timing Tgr NY041

Ton Timing Tgr NY041

Ton Fmt R 14 (B14) Tfr Byte 3 on Bus Out Tof Fmt R 3 and 13 (B03, B13) NY045

Tfr Address 2nd of 2 Bytes to 2250 MC BAC

Ton Fmt R 3 (B03) Svc Out Fmt Tof Timing Tgr NY041

Tfr Address 1st of 2 Bytes to 2250 MC BAC

Ton Timing Tgr NY041

Ton Fmt R 15 (B15) 1 Up Wd Ctr Tof Fmt R 3 + 14 (B03-B14) Tof Timing T NY046

Stor Display Blocks Stepping Word Ctr

Ton Fmt R 16 (B16) Fmt R Completed Tof Fmt R 15 (B15) NY046

Tfr Address 2nd of 2 Bytes to 2250 MC BAC

Display Fetched Completed NY173

Fetched Dbl Wd in CBR - CAR Incr 1 Dbl Wd SPAD Incr 1

Ton Scan R 16 (A16) Mem Display Data Seq NY016

Ton Scan R 12 (A12) Run Fmt R NY016

Stor Display Blocks Stepping Word Ctr

B Sheet2

Brought Up By (A36-39) SPAD = 16 Hex (0000) (A36-39)

C Sheet2

Ton Fmt R 11 (B11) SM Byte on Bus Out Tof Fmt R 8 (B08) Tof Timing Tgr NY044

SM Byte to 2250 Hex 2A

Ton Fmt R 3 (B03) Svc Out Fmt NY041

Ton Timing Tgr NY041

Ton Fmt R 12 (B12) Tfr Byte 1 on Bus Out Tof Fmt R 3 & 11 (B03, B11) NY045

8 Up BAC NY036

Tof Scan R 12 (A12) NY016

Ton Fmt R 3 (B03) Svc Out Fmt Tof Timing Tgr NY041

Ton Fmt R 13 (B13) Tof Fmt R 3 & 12 (B03) (B12) Tfr Byte 2 on Bus Out NY045

Ton Fmt R 3 (B03) Svc Out Fmt Tof Timing Tgr NY041

Ton Timing Tgr NY041

Ton Fmt R14 (B14) Tfr Byte 3 on Bus Out Tof Fmt R3 and 13 (B03, B13) N0Y045

Ton Fmt R 3 (B03) Svc Out Fmt Tof Timing Tgr NY041

Ton Timing Tgr NY041

Ton Fmt R 15 (B15) 1 Up Wd Ctr Tof Fmt R 3 and 14 (B03) (B14) Tof Timing Tgr NY041, NY046

Ton Fmt R 16 (B16) Fmt R Completed Tof Fmt R 15 NY046

Yes

Last Word Fetched NY172

No

Ton Scan R 14 (A14) Tfr CAR Tof Scan R 16 (A16) NY017

Ton Scan R 12 (A12) Run Format R NY016

B Sheet 2

Ton Scan R 18 (A18) Scan R Completed NY018

Ton Scan R 7 (A07) Command Out NY014

Tof Scan R 7 (A07) NY014

Status In Device End NY091 NY014

Ton Scan R11 (A11) SVC Out Stop NY015

Tof Scan R 5 (A05) NY013

Sheet 2

A

Tof Scan R 11 (A11) NY015

Not Op In NY091

Ton Scan R 3 (A03) Addr of 2250 on Bus Out NY012

Ton Scan R 4 (A04) Addr Out Tof Scan R 18 NY012, NY018

Ton Scan R 5 (A05) Select Out Hold Out NY013

Op In Tof Scan R 3 and 4 (A03) (A04) NY012 NY091

Ton Scan R 6 (A06) Cmd Byte on Bus Out NY016

Set BAC and Start Hex 27

Ton Scan R 7 (A07) Command Out NY014

Tof Scan R 6 (A06) and 7 (A07) NY013, NY014

Status In Not Dev End NY091, NY014

Ton Scan R 8 (A08) Svc Out Normal NY014

Ton Scan R 9 (A09) Step Command Ctr NY015

Command Counter at 5 (A24) (A26)

Ton Scan R 10 (A10) Tof Scan R 8 and 9 (A08) (A09) Cmd Addr Byte on Bus Out NY015

Ton Scan R 8 (A08) Svc Out Normal NY014

1st Byte of Start Regen Adder to 2250 Hex 08

Ton Scan R 9 (A09) Step Command Ctr NY015

Command Counter At 6 (A24) (A25)

Tof Scan R 8 (A08) and 9 (A09) NY014, NY015

Mem Cmd Address Byte 2 NY015

Ton Scan R 8 (A08) Svc Out Normal NY014

2nd Byte of Start Regen Addr to 2250 Hex 80

Ton Scan R 9 (A09) Step Command Ctr NY015

Command Counter at 7 (A24, 25, 26)

Tof Scan R 8,9, 10 (A08) (A09) (A10) NY014, NY015

Status In Device End NY091, NY014

Ton Scan R 11 (A11) Svc Out Stop NY015

Ton Scan R 18 (A18) Scan R Complete Tof Scan R 1 and 5 NY018

Tof Scan R 11 (A11) NY015

End of Operation

DIAGRAM 5-514. CRT STORAGE DISPLAY (SHEET 3 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC — 2250	Notes
Initial Selection	Scan Key or CPU Stop	1		16	Op Out ——	Set BAC to 7818 (Hex 1E8A)
	SR 1 (Scan Ring 1)	1,2	0	16	Op Out —— Note: Operational Out remains active as long as CRT Display rotary switch is not off.	Set Command Counter to 0, or set to 4 if block scan switch is on. Set Word Counter to 0.
	SR 2	1,3	0	16	2250 Adr on Bus Out ——	Reset SR 18 if on
	SR 3	1,3,4	0	16	2250 Adr on Bus Out —— Address Out ——	
	SR 4	1,3,4,5	0	16	2250 Adr on Bus Out —— Address Out —— Sel Out/Hold Out ——	
	Operational In	1,5	0	16	Sel Out/Hold Out —— —— Op In	
Send 'Set Buffer Address and Stop' Command to 2250	Address In	1,5,6	0	16	Sel Out/Hold Out —— —— Op In —— Adr In —— 2250 Adr on Bus In Cmnd on Bus Out ——	
	SR 6	1,5,6,7	0	16	Sel Out/Hold Out —— —— Op In —— Adr In —— 2250 Adr on Bus In Cmnd on Bus Out —— Command Out ——	
	Not Address In	1,5	0	16	Sel Out/Hold Out —— —— Op In	
	Status In, Not Chan End, Not Device End	1,5,8	0	16	Sel Out/Hold Out —— —— Op In —— Status Byte on Bus In —— Status In Service Out ——	
	Not Status In	1,5,8,9	1	16	Sel Out/Hold Out —— —— Op In Service Out ——	Step Command Counter
Send Command Address (2 bytes)	SR 9 Delayed	1,5,10	1	16	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out ——	
	Service In	1,5,10,8	1	16	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— —— Service In Service Out ——	First byte of starting address to 2250. First byte is high-order byte. Complete address is 2176 (Hex 0880).
	Not Service In	1,5,10,8,9	2	16	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— Service Out ——	Step Command Counter
	SR 9 Delayed	1,5,10	2	16	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out ——	
	Service In	1,5,10,8	2	16	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— —— Service In Service Out ——	Second byte of starting address to 2250
	Not Service In	1,5,10,8,9	3	16	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— Service Out ——	Step Command Counter
	SR 9 Delayed	1,5	3	16	Sel Out/Hold Out —— —— Op In	
Ending Sequence (Receive Status Byte)	Status In, Chan End, Device End	1,5,11	3	16	Sel Out/Hold Out —— —— Op In Service Out ——	
	Not Status In	1	3	16	Sel Out/Hold Out —— —— Op In	
Initial Selection	Not Operational In	1,3	3	16	2250 Adr on Bus Out ——	
	SR 3	1,3,4	3	16	2250 Adr on Bus Out —— Address Out ——	
	SR 4	1,3,4,5	3	16	2250 Adr on Bus Out —— Address Out —— Sel Out/Hold Out ——	
	Operational In	1,5	3	16	Sel Out/Hold Out —— —— Op In	
Send 'Write' Command to 2250	Address In	1,5,6	3	16	Sel Out/Hold Out —— —— Op In —— Address In Cmnd Byte on Bus Out ——	Command is 'Write' (Hex 01)
	SR 6	1,5,6,7	3	16	Sel Out/Hold Out —— —— Op In —— Address In Cmnd Byte on Bus Out —— Command Out ——	
	Not Address In	1,5	3	16	Sel Out/Hold Out —— —— Op In	
	Status In	1,5,8	3	16	Sel Out/Hold Out —— —— Op In —— Status In —— Status Byte on Bus In Service Out ——	
	Not Status In	1,5,8,9	4	16	Sel Out/Hold Out —— —— Op In Service Out ——	Step Command Counter
	SR 9	1,5,8,9,14	4	16	Sel Out/Hold Out —— —— Op In Service Out ——	
	Reset SR 8, SR 9	1,5,14	4	16	Sel Out/Hold Out —— —— Op In	
	SR 14	1,5,14,12	4	16	Sel Out/Hold Out —— —— Op In	Start Format Ring

Scan Ring

1 Scan Run
2 Counter Reset
3 2250 Address
4 Address Out
5 Sel/Hold Out
6 Command Byte
7 Command Out
8 Service Out
9 Step Cmnd Ctr
10 Command Adr
11 Service Out Stop
12 Run Format Ring
14 Storage Display, Transfer CAR

Command Counter

0 Set BAC and Stop Cmnd
1 Write Starting Adr (byte 1)
2 Write Starting Adr (byte 2)
3 Write Command

Format Ring

16 Format Ring Completed

DIAGRAM 5-514. CRT STORAGE DISPLAY (SHEET 4 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC — 2250	Notes
Send SM and ECM Bytes to 2250	SR 12	1,5,12,(14 or 16) See Note	4	1,16	Sel Out/Hold Out — — Op In — Service In	Reset Byte Counter. Begin sequence to transfer CAR or CBR to 2250 storage.
	FR 1 (Format Ring 1)	1,5,12,(14 or 16)	4	2	Sel Out/Hold Out — — Op In — Service In SM Byte on Bus Out —	BAC incremented by 2 (FR 2)*
	FR 2	1,5,12,(14 or 16)	4	2,3	Sel Out/Hold Out — — Op In — Service In Service Out — SM Byte on Bus Out —	Send SM Byte to 2250 (Hex 2A)
	Not Service In	1,5,12,(14 or 16)	4	2,3,T	Sel Out/Hold Out — — Op In Service Out — SM Byte on Bus Out —	
	Timing Trigger	1,5,12,(14 or 16)	4	4,T	Sel Out/Hold Out — — Op In ECM Byte on Bus Out —	
	Service In	1,5,12,(14 or 16)	4	4,3	Sel Out/Hold Out — — Op In ECM Byte on Bus Out — Service Out — — Service In	Send ECM Byte to 2250 (Hex 41)
	Not Service In	1,5,12,(14 or 16)	4	4,3,T	Sel Out/Hold Out — — Op In ECM Byte on Bus Out — Service Out —	
Send Left Hex Char to 2250	Timing Trigger	1,5,12,(14 or 16)	4	5,T	Sel Out/Hold Out — — Op In Left Hex Char on Bus Out —	
	Service In	1,5,12,(14 or 16)	4	5,3	Sel Out/Hold Out — — Op In — Service In Service Out — Left Hex Char on Bus Out —	
	Not Service In	1,5,12,(14 or 16)	4	5,3,T	Sel Out/Hold Out — — Op In Service Out — Left Hex Char on Bus Out —	
Send Right Hex Char to 2250	Timing Trigger	1,5,12,(14 or 16)	4	6,T	Sel Out/Hold Out — — Op In Right Hex Char on Bus Out —	
	Service In	1,5,12,(14 or 16)	4	6,3	Sel Out/Hold Out — — Op In — Service In Service Out — Right Hex Char on Bus Out —	
	Not Service In	1,5,12,(14 or 16)	4	6,3,T	Sel Out/Hold Out — — Op In Service Out — Right Hex Char on Bus Out —	
Send Blank or Asterisk to 2250	Timing Trigger	1,5,12,(14 or 16)	4	7,T	Sel Out/Hold Out — — Op In Blank or Asterisk on Bus Out —	
	Service In	1,5,12,(14 or 16)	4	7,3	Sel Out/Hold Out — — Op In — Service In Service Out — Blank or Asterisk on Bus Out —	
	Not Service In	1,5,12,(14 or 16)	4	7,3,T	Sel Out/Hold Out — — Op In Service Out — Blank or Asterisk on Bus Out —	
Send Null Character to 2250 (Null sent following third byte of address)	Timing Trigger	1,5,12,(14 or 16)	4	10,T	Sel Out/Hold Out — — Op In Null on Bus Out —	
	Service In	1,5,12,(14 or 16)	4	10,3	Sel Out/Hold Out — — Op In — Service In Service Out — Null on Bus Out —	
	Not Service In	1,5,12,(14 or 16)	4	10,3,T	Sel Out/Hold Out — — Op In Service Out — Null on Bus Out —	
One-up Byte Counter	Timing trigger and blank or asterisk on bus out, or timing trigger and null on bus out	1,5,12,(14 or 16)	4	8,T	Sel Out/Hold Out — — Op In	

Scan Ring

1 Scan Run
5 Sel/Hold Out
12 Run Format
14 Sto Disp, Trf CAR
16 Sto Disp, Trf CBR

Command Counter

3 Write Command
4 Start Regen Cmnd (Set BAC and Start)

Format Ring

1 Reset Byte Ctr
2 Set Mode Cmnd 1
3 Service Out Format
4 ECM Cmnd
5 Sel Left Hex Char
6 Sel Right Hex Char
8 Step Byte Ctr
16 Format Completed
T Timing Trigger

Note: SR 14 is on when Format Ring is transferring CAR to 2250. SR 16 is on when Format Ring is transferring CBR (storage data) to 2250.

* BAC is incremented by 10 in two steps, first by 2 and then by 8.

DIAGRAM 5-514. CRT STORAGE DISPLAY (SHEET 5 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC — 2250	Notes
Send Transfer Order and Two Address Bytes to 2250	FR 8 and Byte Ctr 0 or FR 8, FR 14 (Addr Seq) and Byte Ctr 2	1,5,12,(14 or 16)	4	11	— Op In Sel Out/Hold Out — SM Byte on Bus Out —	
	Service In	1,5,12,(14 or 16)	4	11,3	— Op In — Service In Sel Out/Hold Out — SM Byte on Bus Out — Service Out —	Send SM Byte to 2250 (Hex 2A)
	Not Service In	1,5,12,(14 or 16)	4	11,3,T	— Op In Sel Out/Hold Out — SM Byte on Bus Out — Service Out —	
	Timing Trigger	1,5,12,(14 or 16)	4	12,T	— Op In Sel Out/Hold Out — Transfer Byte 1 on Bus Out —	FR 12 turns off SR 12. BAC Incremented by 8 (FR 12)
	Service In	1,5,(14 or 16)	4	12,3	— Op In — Service In Sel Out/Hold Out — Transfer Byte 1 on Bus Out — Service Out —	
	Not Service In	1,5,(14 or 16)	4	12,3,T	— Op In Sel Out/Hold Out — Transfer Byte 1 on Bus Out — Service Out —	
	Timing Trigger	1,5,(15 or 16)	4	13,T	— Op In Sel Out/Hold Out — Transfer Byte 2 on Bus Out —	FR 13 turns on SR 15 and turns off SR 14. SR 14 resets SR 16 (see note).
	Service In	1,5,(14 or 15)	4	13,3	— Op In — Service In Sel Out/Hold Out — Transfer Byte 2 on Bus Out — Service Out —	Send transfer address (first of two bytes) to 2250. MC BAC is stored in 2250 storage. First byte is high order; second is low order.
	Not Service In	1,5,(14 or 15)	4	13,3,T	— Op In Sel Out/Hold Out — Transfer Byte 2 on Bus Out — Service Out —	
	Timing Trigger	1,5,(14 or 15)	4	14,T	— Op In Sel Out/Hold Out — Transfer Byte 3 on Bus Out —	
	Service In	1,5,(14 or 15)	4	14,3	— Op In — Service In Sel Out/Hold Out — Transfer Byte 3 on Bus Out — Service Out —	Send transfer address (second of two bytes) to 2250. This is the low-order eight bits of MC BAC.
	Not Service In	1,5,(14 or 15)	4	14,3,T	— Op In Sel Out/Hold Out — Transfer Byte 3 on Bus Out — Service Out —	
One-up Word Counter, Format Ring Complete	Timing Trigger	1,5,(14 or 15)	4	15,T	— Op In Sel Out/Hold Out —	Actual stepping of the word counter is blocked on storage display
	Not Timing Trigger	1,5,(14 or 15)	4	16	— Op In Sel Out/Hold Out —	
End of Address Sequence Restart Format Ring	Fetch Request	1,5,15	4	16	— Op In — Service In Sel Out/Hold Out —	
	Fetch Completed	1,5,15,16	4	16	— Op In — Service In Sel Out/Hold Out —	Fetched double word is set into the CBR. CAR is incremented by one double word. The SPAD counter is incremented by 1.
	SR 16	1,5,12,16	4	16	— Op In — Service In Sel Out/Hold Out —	Begin data sequence to transfer CBR to 2250 storage
End of Data Sequence, Restart Format Ring	FR 16	1,5,12,14	4	16	— Op In Sel Out/Hold Out —	Set SR 12. Restart format ring. Begin address sequence to transfer CAR to 2250 storage.
End of Data Sequence, Last Word Fetched	FR 16 and Last Word Fetched	1,5,18	4	16	— Op In Sel Out/Hold Out —	'Last Word Fetched' condition is brought up when SPAD equals 0000
	Service In	1,5,18,7	4	16	— Op In — Service In Sel Out/Hold Out —	Command Out causes 2250 to drop Service In and send Status In with Channel End and Device End
Ending Sequence	Not Service In	1,5,18	4	16	— Op In Sel Out/Hold Out —	
	Status In, Chan End, Device End	1,5,18,11	4	16	— Op In — Status Byte on Bus In — Status In Sel Out/Hold Out — Service Out —	
	SR 11	1,11,18	4	16	— Op In — Status Byte on Bus In — Status In Service Out —	
	Not Status In	1,18	4	16	— Op In	

Scan Ring

1 Scan Run
5 Sel/Hold Out
11 Service Out Stop
14 Sto Disp, Trf CAR
15 Fetch Request
16 Sto Disp, Trf CBR
18 Scan Ring Completed

Command Counter

4 Start Regen Cmnd (Set BAC and Start)

Format Ring

3 Service Out Format
11 Set Mode Cmnd 2
12 Transfer
13 Transfer Address 1
14 Transfer Adr 2
15 Step Word Counter
16 Format Completed
T Timing Trigger

Note: SR 14 is on when Format Ring is transferring CAR to 2250.
SR 16 is on when Format Ring is transferring CBR (storage data) to 2250.

DIAGRAM 5-514. CRT STORAGE DISPLAY (SHEET 6 OF 7)

Operation	Event	Scan Ring	Command Counter	Format Ring	Interface Signals MC — 2250	Notes
Send Start Regeneration Command to 2250	Not Operational In	1,3,18	4	16	2250 Adr on Bus Out —	
	SR 3	1,3,4	4	16	2250 Adr on Bus Out — Address Out —	
	SR 4	1,3,4,5	4	16	2250 Adr on Bus Out — Address Out — Sel Out/Hold Out —	
	Operational In	1,5	4	16	Sel Out/Hold Out — — Op In	
	Address In	1,5,6	4	16	Sel Out/Hold Out — — Op In — Address In Cmnd Byte on Bus Out —	Command Byte: Set Buffer Address and Start (Hex 27)
	SR 6	1,5,6,7	4	16	Sel Out/Hold Out — — Op In — Address In Cmnd Byte on Bus Out — Command Out —	
	Not Address In	1,5	4	16	Sel Out/Hold Out — — Op In	
	Status In, Not Chan End, Not Device End	1,5,8	4	16	Sel Out/Hold Out — — Op In — Status In — Status Byte on Bus In Service Out —	
	Not Status In	1,5,8,9	5	16	Sel Out/Hold Out — — Op In Service Out —	Step Command Counter
Send Command Address (2 bytes) to 2250	SR 9 Delayed	1,5,10	5	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte on Bus Out —	
	Service In	1,5,10,8	5	16	Sel Out/Hold Out — — Op In — Service In Cmnd Adr Byte on Bus Out — Service Out —	First byte of start regeneration address to 2250. First byte is high-order byte. Complete address is 2176 (Hex 0880).
	Not Service In	1,5,10,8,9	6	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte on Bus Out — Service Out —	Step Command Counter
	SR 9 Delayed	1,5,10	6	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte (2) on Bus Out —	
	Service In	1,5,10,8	6	16	Sel Out/Hold Out — — Op In — Service In Cmnd Adr Byte (2) on Bus Out — Service Out —	Second byte of start regeneration address to 2250
	Not Service In	1,5,10,8,9	7	16	Sel Out/Hold Out — — Op In Cmnd Adr Byte (2) on Bus Out — Service Out —	Step Command Counter
	SR 9 Delayed	1,5	7	16	Sel Out/Hold Out — — Op In	
Ending Sequence (End of Scan)	Status In, Chan End, Device End	1,5,11	7	16	Sel Out/Hold Out — — Op In — Status Byte on Bus In — Status In Service Out —	
	SR 11	1,5,11,18	7	16	Sel Out/Hold Out — — Op In — Status Byte on Bus In — Status In Service Out —	
	SR 18	11, 18	7	16	— Op In — Status Byte on Bus In — Status In Service Out —	
	Not Status In	18	7	16		End of Operation

Scan Ring

1 Scan Run
3 2250 Address
4 Address Out
5 Sel/Hold Out
6 Command Byte
7 Command Out
8 Service Out
9 Step Command Counter
10 Command Address
11 Service Out Stop
18 Scan Ring Completed

Command Counter

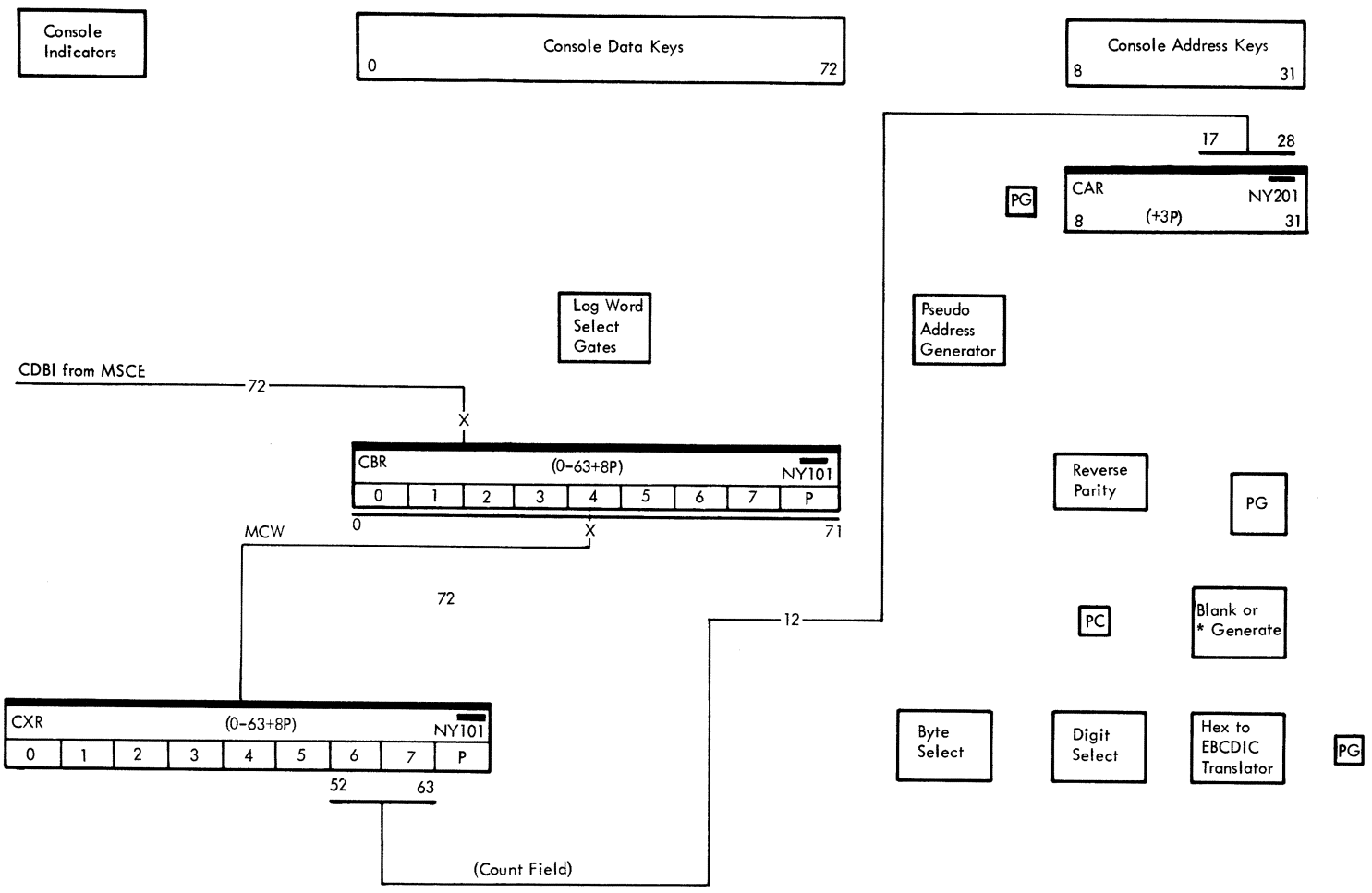
4 Start Regen Cmnd (Set BAC and Start)
5 Start Regen Adr (byte 1)
6 Start Regen Adr (byte 2)
7 Unused

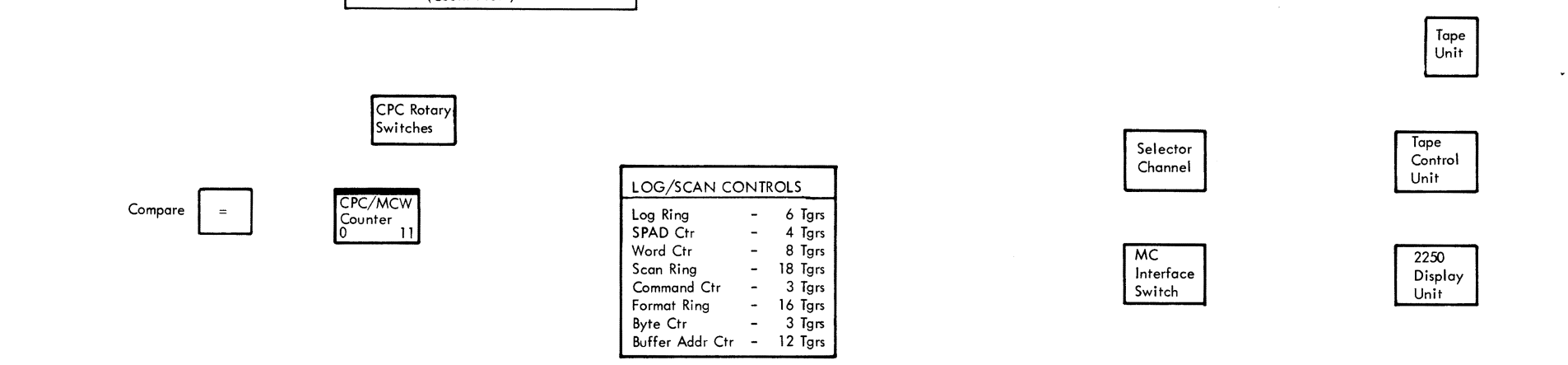
Format Ring

16 Format Completed

DIAGRAM 5-514. CRT STORAGE DISPLAY (SHEET 7 OF 7)

MCW Data Flow Preceding Message Display





Message Display (Data Flow)

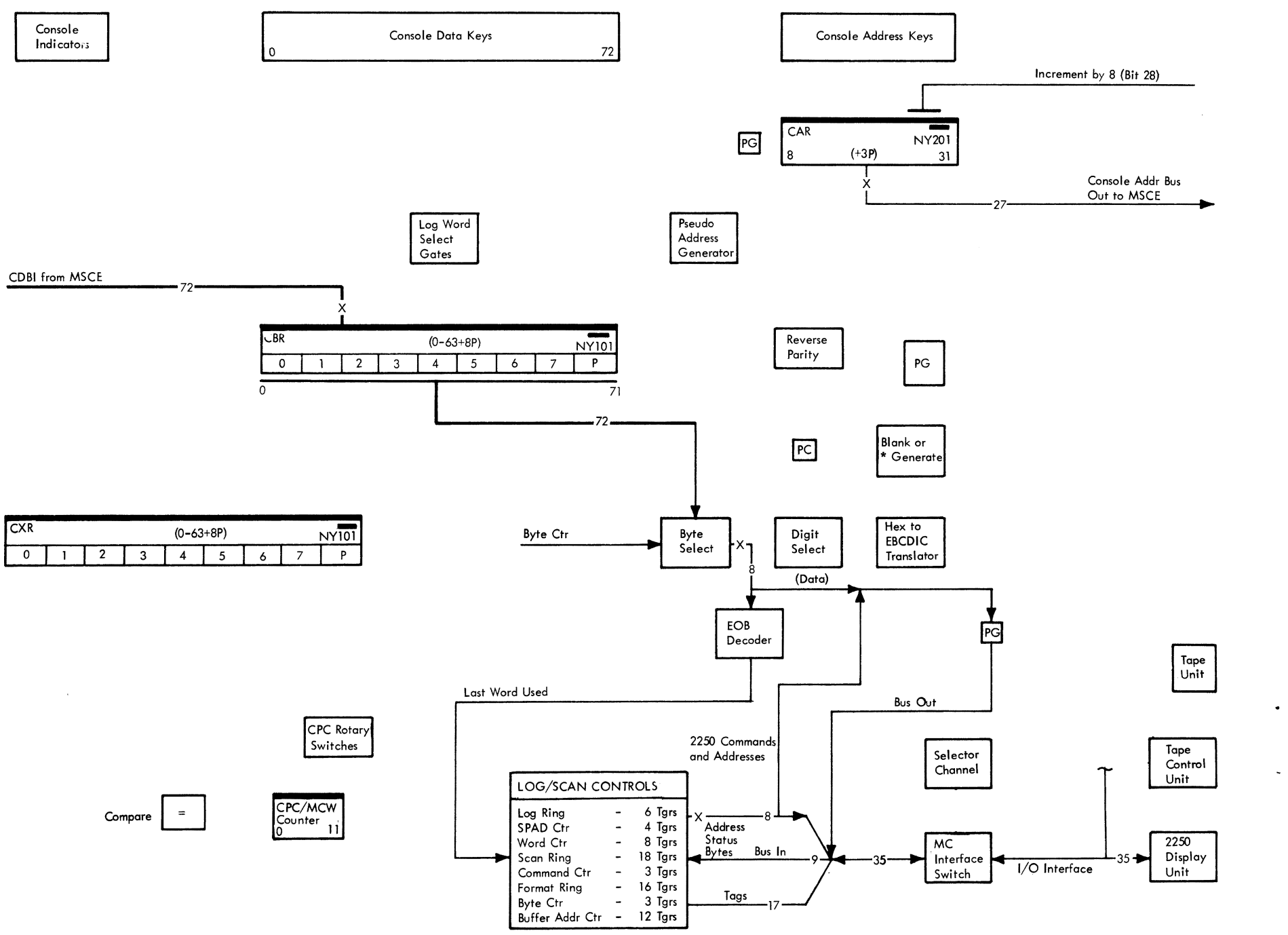


DIAGRAM 5-515. CRT MESSAGE DISPLAY (SHEET 1 OF 6)

Objective:
Transfer an EBCDIC message from MWS to 2250 Buffer and Display it on CRT by use of Diagnose Instruction.

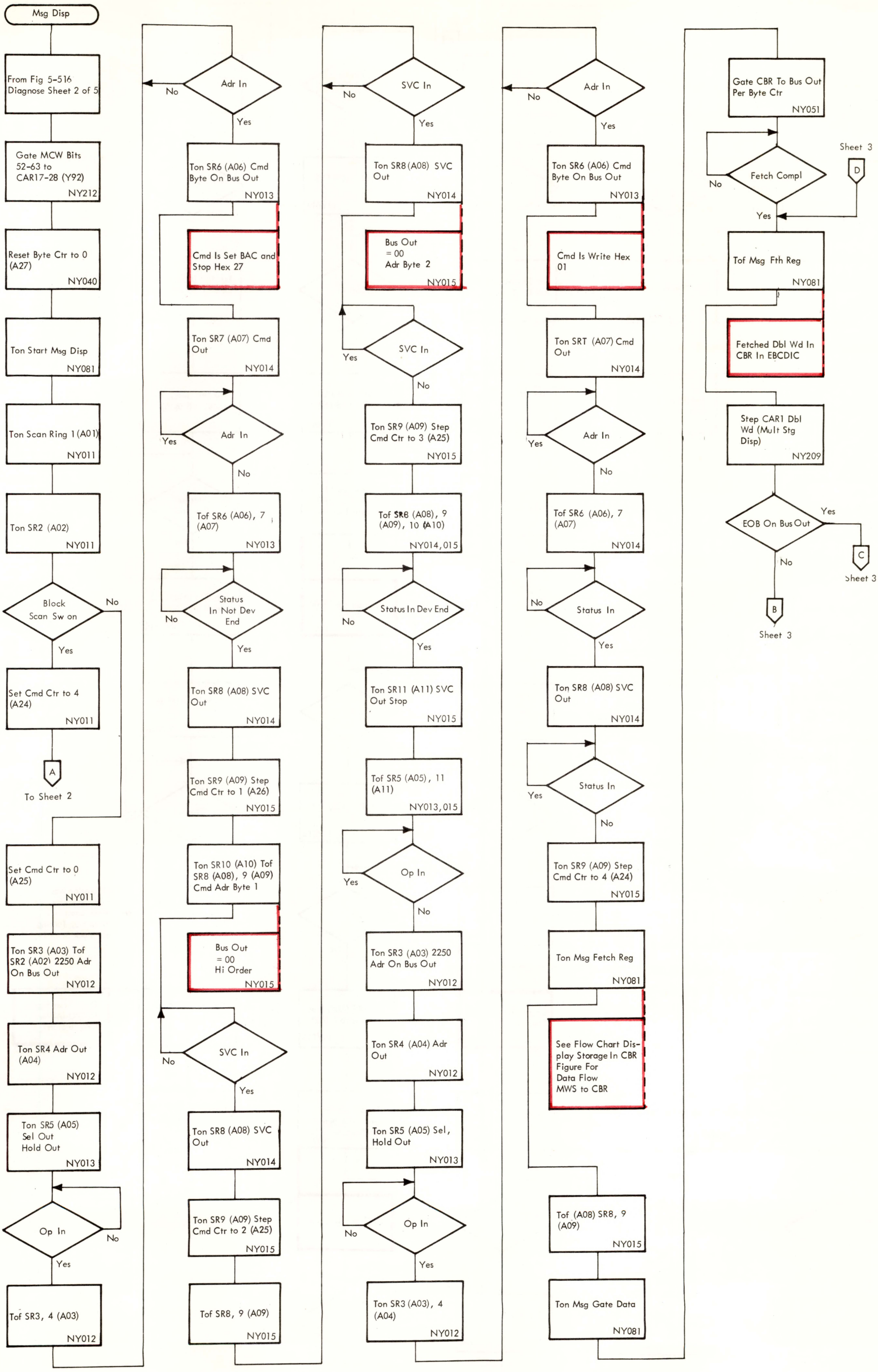


DIAGRAM 5-515. CRT MESSAGE DISPLAY (SHEET 2 OF 6)

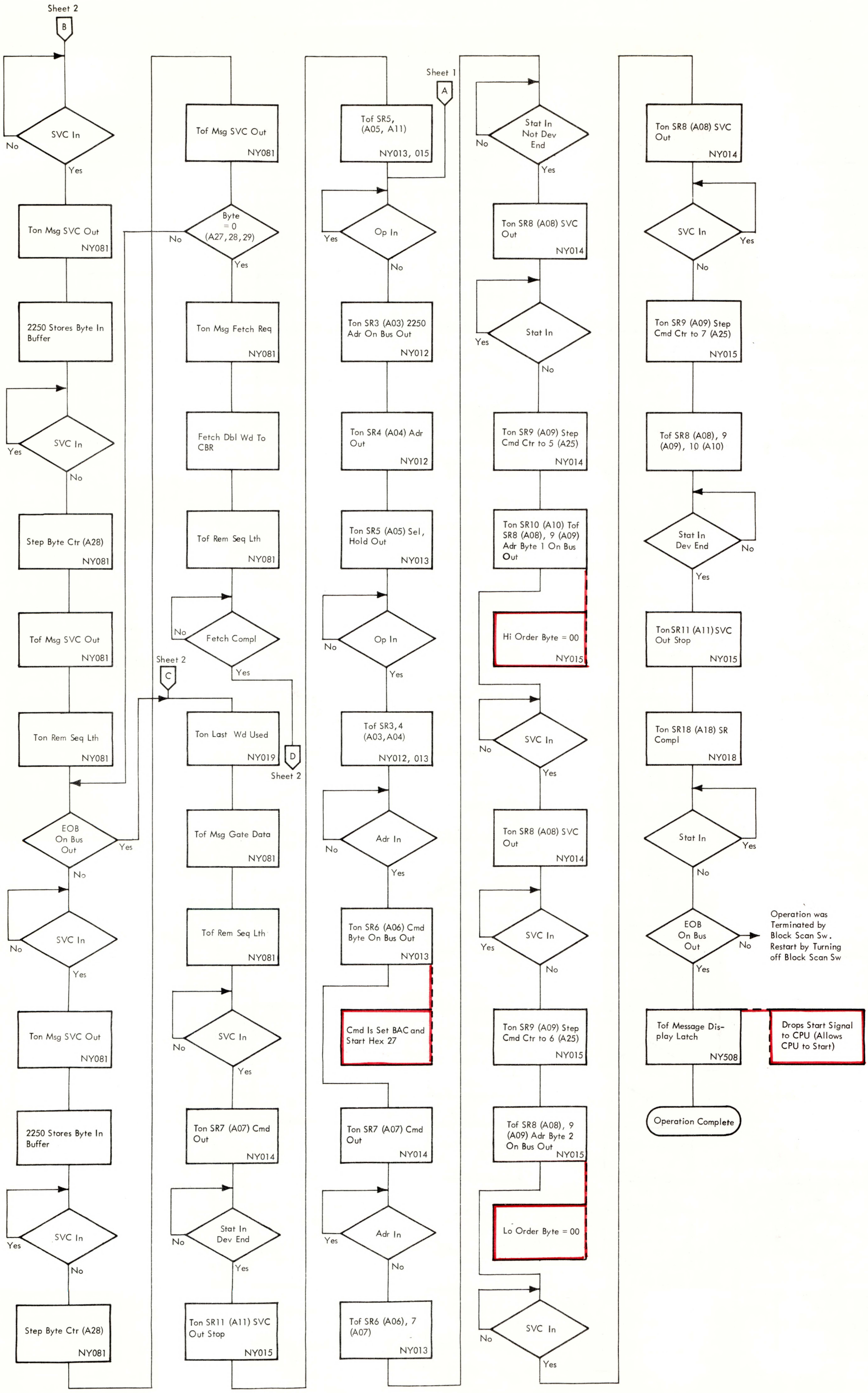


DIAGRAM 5-515. CRT MESSAGE DISPLAY (Sheet 3 OF 6)

Operation	Event	Scan Ring	Command Counter	Message Display Triggers	MC Interface Signals 2250	Notes
Diagnose Instruction	I2 Field contains bit 8 and not bit 9				Op Out —— Note: Operational Out remains active as long as CRT Display rotary switch is not off.	CRT Display Rotary Switch must be in the 'Message Display' position
	MCW is fetched and set into the CBR					
	MCW is transferred from CBR to CXR. MCW should be all zeros except for the count field (52-63)					CXR bits 52-63 are transferred to CAR bits 17-28
Initial Selection	Start Message Display (From Diagnose Instruction)	1		SMD		Reset Scan Ring and Byte Counter. Start Scan Ring.
	SR 1 (Scan Ring 1)	1,2	0			Set Command Counter to 0, or set to 4 if block scan switch is on
	SR 2	1,3	0		2250 Adr on Bus Out ——	
	SR 3	1,3,4	0		2250 Adr on Bus Out —— Address Out ——	
	SR 4	1,3,4,5	0		2250 Adr on Bus Out —— Address Out —— Sel Out/Hold Out ——	
	Operational In	1,5	0		Sel Out/Hold Out —— —— Op In	
Send 'Set Buffer Address and Stop' Command to 2250	Address In	1,5,6,7	0		Sel Out/Hold Out —— —— Op In —— Adr In —— 2250 Adr on Bus In Cmnd on Bus Out ——	
	SR 6	1,5,6,7	0		Sel Out/Hold Out —— —— Op In —— Addr In —— 2250 Adr on Bus In Cmnd on Bus Out —— Command Out ——	
	Not Address In	1,5	0		Sel Out/Hold Out —— —— Op In	
	Status In, Not Chan End, Not Device End	1,5,8	0		Sel Out/Hold Out —— —— Op In —— Status Byte on Bus In —— Status In Service Out ——	
	Not Status In	1,5,8,9	1		Sel Out/Hold Out —— ---- Op In Service Out ——	Step Command Counter
Send Command Address (2 bytes)	SR 9 Delayed	1,5,10	1		Sel Out/Hold Out —— ---- Op In Cmnd Adr Byte on Bus Out ——	
	Service In	1,5,10,8	1		Sel Out/Hold Out ——	First byte of starting address to 2250. First byte is high-order byte. Complete address is 0000.
	Not Service In	1,5,10,8,9	2		Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— Service Out ——	Step Command Counter
	SR 9 Delayed	1,5,10	2		Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out ——	
	Service In	1,5,10 8	2		Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— —— Service In Service Out ——	Second byte of starting address to 2250
	Not Service In	1,5,10,8,9	3		Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— Service Out ——	Step Command Counter
	SR 9 Delayed	1,5	3		Sel Out/Hold Out ---- —— Op In	
Ending Sequence (Receive Status Byte)	Status In, Chan End, Device End	1,5,11	3		Sel Out/Hold Out —— —— Op In Service Out ——	
	Not Status In	1	3		—— Op In	
Initial Selection	Not Operational In	1,3	3		2250 Adr on Bus Out ——	
	SR 3	1,3,4	3		2250 Adr on Bus Out —— Address Out ——	
	SR 4	1,3,4,5	3		2250 Adr on Bus Out —— Address Out —— Sel Out/Hold Out ——	
	Operational In	1,5	3		Sel Out/Hold Out —— —— Op In	
Send 'Write' Command to 2250	Address In	1,5,6	3		Sel Out/Hold Out —— —— Op In —— Address In Cmnd Byte on Bus Out ——	Command is 'Write' (Hex 01)
	SR 6	1,5,6,7	3		Sel Out/Hold Out —— —— Op In —— Address In Cmnd Byte on Bus Out —— Command Out ——	
	Not Address In	1,5	3		Sel Out/Hold Out —— —— Op In	
	Status In	1,5,8	3		Sel Out/Hold Out —— —— Op In —— Status In —— Status Byte on Bus In Service Out ——	

Scan Ring

1 Scan Run
2 Counter Reset
3 2250 Address
4 Address Out
5 Sel/Hold Out
6 Command Byte
7 Command Out
8 Service Out
9 Step Cmnd Ctr
10 Command Adr
11 Service Out Stop

Command Counter

0 Set BAC and Stop Cmnd
1 Write Starting Adr (byte 1)
2 Write Starting Adr (byte 2)
3 Write Command

Message Display Triggers

SMD Start Message Display

DIAGRAM 5-515. CRT MESSAGE DISPLAY (SHEET 4 OF 6)

Operation	Event	Scan Ring	Command Counter	Message Display Triggers	Interface Signals (MC / 2250)	Notes
Send 'Write' Command to 2250 (continued)	Not Status In	1,5,8,9	4		— Op In Sel Out/Hold Out — Service Out —	Step Command Counter
	SR 9	1,5,8,9	4	MFR	— Op In Sel Out/Hold Out — Service Out —	Fetch request for double word addressed by CAR
	Reset SR 8, SR 9	1,5	4	MFR	— Op In Sel Out/Hold Out —	
Fetch first double word of message	MFR	1,5	4	MFR, MGD	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Gate CBR byte selected by byte counter directly to Bus Out. Reset 'Remember Sequence' if on.
	Fetch Complete	1,5	4	MFR, MGD	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Set fetched double word into CBR. Advance CAR by one double word.
Send first data byte of any word to 2250	Service In	1,5	4	MFR, MGD, MSO	— Op In — Service In Sel Out/Hold Out — CBR Byte on Bus Out — Service Out —	
	MSO	1,5	4	MGD, MSO	— Op In — Service In Sel Out/Hold Out — CBR Byte on Bus Out — Service Out —	Data byte set into 2250 storage. Fetch Request reset.
	Not Service In	1,5	4	MGD, MSO, SBC	— Op In Sel Out/Hold Out — CBR Byte on Bus Out — Service Out —	Step Byte Counter
	SBC	1,5	4	MGD, SBC, RS	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Reset Message Service Out. Set Remember Sequence Latch.
	Not MSO	1,5	4	MGD, RS	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Reset Step Byte Counter Latch
Send remaining data bytes of any word to 2250	Service In	1,5	4	MGD, RS, MSO	— Op In — Service In Sel Out/Hold Out — CBR Byte on Bus Out — Service Out —	
	MSO	1,5	4	MGD, RS, MSO	— Op In — Service In Sel Out/Hold Out — CBR Byte on Bus Out — Service Out —	Data byte set into 2250 storage
	Not Service In	1,5	4	MGD, RS, MSO, SBC	— Op In Sel Out/Hold Out — CBR Byte on Bus Out — Service Out —	Step Byte Counter
	SBC	1,5	4	MGD, RS, SBC	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Reset Message Service Out
	Not MSO	1,5	4	MGD, RS	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Reset Step Byte Counter Latch
Byte Counter Zero. Fetch next double word of message.	SBC, Byte Counter Zero	1,5	4	MGD, RS, SBC, MFR	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Turn on Message Fetch Request
	MFR	1,5	4	MGD, MFR	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Reset Remember Sequence Latch. Fetch double word addressed by CAR
	Fetch Complete	1,5	4	MGD, SBC	— Op In Sel Out/Hold Out — CBR Byte on Bus Out —	Set fetched double word into CBR. Advance CAR by one double word.
Sense EOB. Stop data transfer.	SBC, EOB on Bus Out	1,5	4	RS, SBC, LWU	— Op In Sel Out/Hold Out — CBR Byte (EOB) on Bus Out —	Set Last Word Used Latch. Reset Message Gate Display.
Signal End of Data to 2250	Service In	1,5,7	4	LWU	— Op In — Service In Sel Out/Hold Out — Command Out —	Send Command Out
Ending Sequence	Not Service In	1,5	4	LWU	— Op In Sel Out/Hold Out —	
	Status In, Chan End, Device End	1,5,11	4	LWU	— Op In — Status Byte on Bus In — Status In Sel Out/Hold Out — Service Out —	
	SR 11	1,11	4	LWU	— Op In — Status Byte on Bus In — Status In Service Out —	
	Not Status In	1	4		— Op In	

Scan Ring

1 Scan Run
5 Sel/Hold Out
7 Command Out
8 Service Out
9 Step Command Counter
11 Service Out Stop

Command Counter

4 Start Regen Command (Set BAC and Start)

Message Display Triggers

MGD Message Gate Data
RS Remember Sequence
MSO Message Service Out
SBC Step Byte Counter
MFR Message Fetch Request
LWU Last Word Used

DIAGRAM 5-515. CRT MESSAGE DISPLAY (SHEET 5 OF 6)

Operation	Event	Scan Ring	Command Counter	Message Display Triggers	Interface Signals MC — 2250	Notes
Send Start Regeneration command to 2250	Not Operational In	1,3	4	LWU	2250 Adr on Bus Out ——	
	SR 3	1,3,4	4	LWU	2250 Adr on Bus Out —— Address Out ——	
	SR 4	1,3,4,5	4	LWU	2250 Adr on Bus Out —— Address Out —— Sel Out/Hold Out ——	
	Operational In	1,5	4	LWU	Sel Out/Hold Out —— —— Op In	
	Address In	1,5,6	4	LWU	Sel Out/Hold Out —— —— Op In —— Address In Cmnd Byte on Bus Out ——	Command Byte: Set Buffer Address and Start (Hex 27).
	SR 6	1,5,6,7	4	LWU	Sel Out/Hold Out —— —— Op In —— Address In Cmnd Byte on Bus Out —— Command Out ——	
	Not Address In	1,5	4	LWU	Sel Out/Hold Out —— —— Op In	
	Status In, Not Chan End, Not Device End	1,5,8	4	LWU	Sel Out/Hold Out —— —— Op In —— Status In —— Status Byte on Bus In Service Out ——	
	Not Status In	1,5,8,9	5	LWU	Sel Out/Hold Out —— —— Op In Service Out ——	Step Command Counter
Send Command Address (2 bytes) to 2250	SR 9 Delayed	1,5,10	5	LWU	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out ——	
	Service In	1,5,10.8	5	LWU	Sel Out/Hold Out —— —— Op In —— Service In Cmnd Adr Byte on Bus Out —— Service Out ——	First byte of start regeneration address to 2250. First byte is high-order byte. Complete address is 0000.
	Not Service In	1,5,10,8,9	6	LWU	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte on Bus Out —— Service Out ——	Step Command Counter
	SR 9 Delayed	1,5,10	6	LWU	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte (2) on Bus Out ——	
	Service In	1,5,10,8	6	LWU	Sel Out/Hold Out —— —— Op In —— Service In Cmnd Adr Byte (2) on Bus Out —— Service Out ——	Second byte of start regeneration address to 2250
	Not Service In	1,5,10,8,9	7	LWU	Sel Out/Hold Out —— —— Op In Cmnd Adr Byte (2) on Bus Out —— Service Out ——	Step Command Counter
	SR 9 Delayed	1,5	7	LWU	Sel Out/Hold Out —— —— Op In	
Ending Sequence (End of Scan)	Status In, Chan End, Device End	1,5,11	7	LWU	Sel Out/Hold Out —— —— Op In —— Status Byte on Bus In —— Status In Service Out ——	
	SR 11	1,5,11,18	7	LWU	Sel Out/Hold Out —— —— Op In —— Status Byte on Bus In —— Status In Service Out ——	
	SR 18	11,18	7	LWU	—— Op In —— Status Byte on Bus In —— Status In Service Out ——	
	Not Status In	18	7	LWU		End of Operation

Scan Ring

1 Scan Run
3 2250 Address
4 Address Out
5 Sel/Hold Out
6 Command Byte
7 Command Out
8 Service Out
9 Step Command Ctr
10 Command Address
11 Service Out Stop
18 Scan Ring Completed

Command Counter

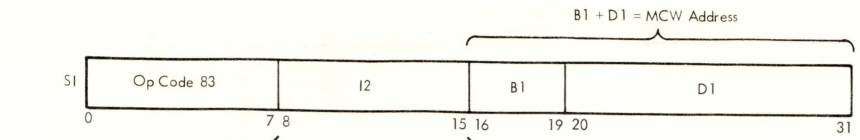
4 Start Regen Cmnd (Set BAC and Start)
5 Start Regen Adr (byte 1)
6 Start Regen Adr (byte 2)
7 Unused

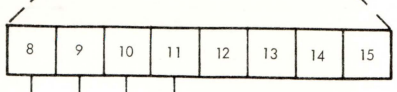
Message Display Triggers

LWU Last Word Used

DIAGRAM 5-515. CRT MESSAGE DISPLAY (SHEET 6 OF 6)

Diagnose Instruction





Bits 8 and 9 work together

Activate Channel Select Line (See Note)

12	13	14	15	
0	0	0	0	- MPX Chan
0	0	0	1	- Chan 1
0	0	1	0	- Chan 2
0	0	1	1	- Chan 3
0	1	0	0	- Chan 4
0	1	0	1	- Chan 5
0	1	1	0	- Stor Chan
0	1	1	1	Unused
1	1	1	0	Unused
1	1	1	1	- No Chan

Activate All Channel Select Lines (See Note)

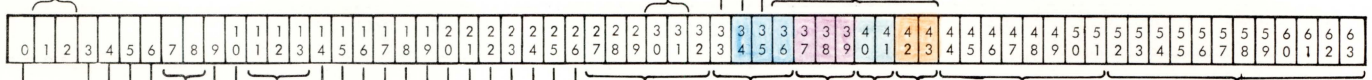
Controls Gating of MCW Bits 33-43
0 = CPU Data Path Controls
1 = PSCE Data Path Controls

Note: When bit 11 is a 1, all channel diagnostic select lines are active. When bit 11 is a 0, bits 12-15 control channel selection. Action taken by the selected channel(s) is controlled by MCW bits 11-13.

0	0	Exit from Diagnose; MCW to CBR to CXR
0	1	MCW to CBR to CXR, and action on count depending on: MCW Bits 7 8: 0 0 = No other action; 0 1 = Hard Stop and Interrupt; 1 0 = Soft Stop and Log Out; 1 1 = Hard Stop and Log Out and Interrupt
1	0	Messeage Display (MCW should be all zeros: otherwise MC may attempt additional functions.)
1	1	Immediate Logout MCW to CBR (no gate to CXR)

Maintenance Control Word

SAA
- 00 No Action
- 01 Invert EMS Bank Bit
- 10 Switch HOLAB and HOMAB
- 11 Invert HOLAB and Switch with HOMAB



- Request Stack Select - MCW Bit 25=1
- Inhibit (Disable) Q Output Priority
- Unused
- Disable PSCE Punchthrough
- Q Register Inhibit Controls

1_2 Bit 10=1

- Count Field
- Error Generate Bits
- FLP Sink/Source Register Controls
- SDB/SAR Pair Controls
- FXP and FLP Storage Buffer Controls
- FXP and FLP Op Stack Controls

1_2 Bit 10=0

- Inhibit Overlap
- SAA Force Adr Exception
- Disable Interval Timer
- Suppress Address Exception
- Disable Multiaccess
- Action on MCW Count
- Check Reset
- Ignore CPE Errors
- Channel Diagnostic Lines
- Reverse Mark Parity
- Force MSM Addr Parity and Key Checks
- Sink Address Parity Invert
- Op Stage Parity Invert
- FXP Error Generate
- FLP Error Generate Controls -- MCW Bit 25=0
- FLP Pulse Stop
- Gate Request Stack Select
- Suppress Instruction Fetch
- Q Store and Fetch Delay
- Allow Q Output Priority
- Q Hold On Error
- PSCE Halt On Error
- 1 Box Adder Error Generate

Data Path Control Fields Decoding

MCW Bits 25-30-31 Code	MCW Bits 41 or 42 and 43 Code	MCW Bits 34 to 36 or 37 to 39 Code	MCW Bits 34 to 36* FLP Op Stk Buffer	MCW Bits 34 to 36* FXP Op Stk Buffer	MCW Bits 37 to 39 FLP Stor Buffer	MCW Bits 37 to 39 FXP Stor Buffer	MCW 40 and 41 SDB/SAR Reg Pair	MCW Bits 42 and 43 FLP Add SI/SO Reg Pair	MCW Bits 42 and 43 FLP M/D and SI/SO Reg Pair
Req Stack 1 — 100	00	000	FL0S0	No Action	No Action	No Action	No Action	No Action	No Action
Req Stack 2 — 101	01	001	FL0S1	FX0S1	FLB1	FXBA	SDB1	A1	M/D1
Req Stack 3 — 110	10	010	FL0S2	FX0S2	FLB2	FXBB	SDB2	A2	M/D2
Req Stack 4 — 111	11	011	FL0S3	FX0S3	FLB3	FXBC	SDB3	A3	No Action
No Action — 000	—	100	FL0S4	FX0S4	FLB4	FXBD	—	—	—
	—	101	FL0S5	FX0S5	FLB5	FXBE	—	—	—
	—	110	FL0S6	FX0S6	FLB6	FXBF	—	—	—
	—	111	FL0S7	No Action	No Action	No Action	—	—	—

Note:
The buffer or register pair designation as specified by the code in the respective MCW data path control field refers to the buffer or register pair that will honor the next request.

* If MCW bit 33 is on, the code specified in MCW bits 34 to 36 refers only to the FLP Op stack; and when it is off, the code refers only to the FXP Op stack.

DIAGRAM 5-516. DIAGNOSE AND MCW (SHEET 1 OF 5)

Objectives:
To decode and execute the Diagnose Instruction (83).

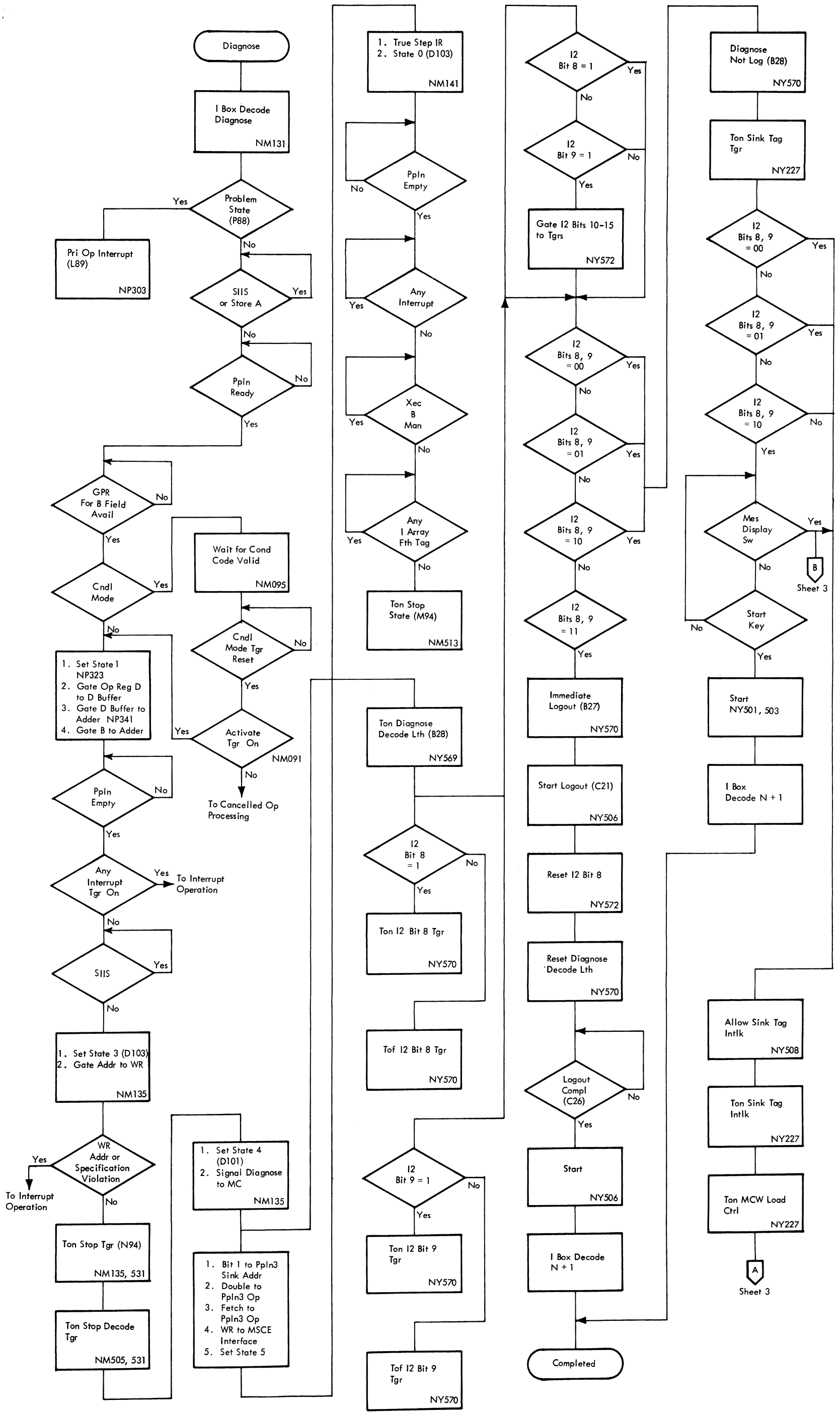


DIAGRAM 5-516. DIAGNOSE AND MCW (SHEET 2 OF 5)

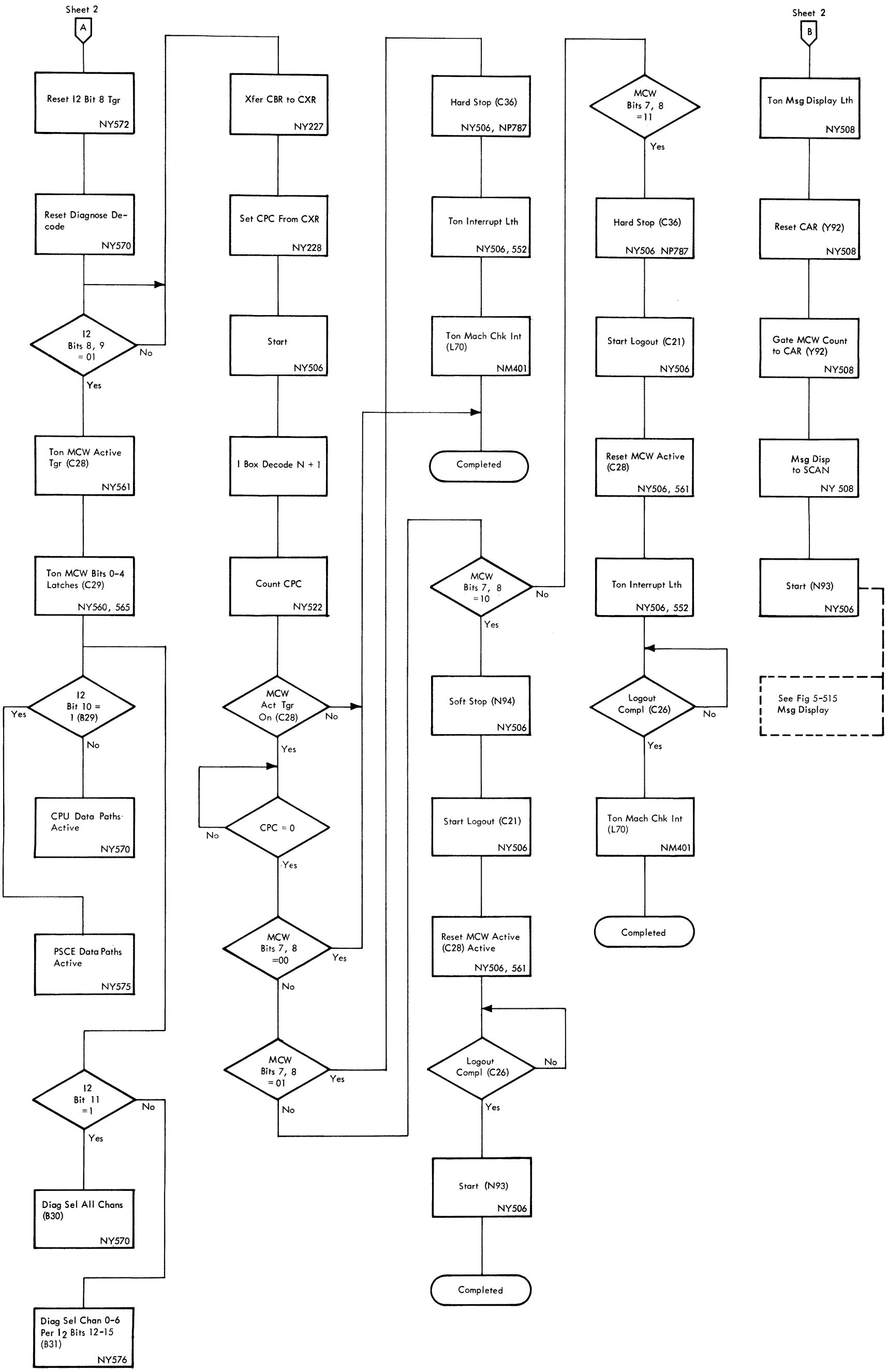


DIAGRAM 5-516. DIAGNOSE AND MCW (SHEET 3 OF 5).

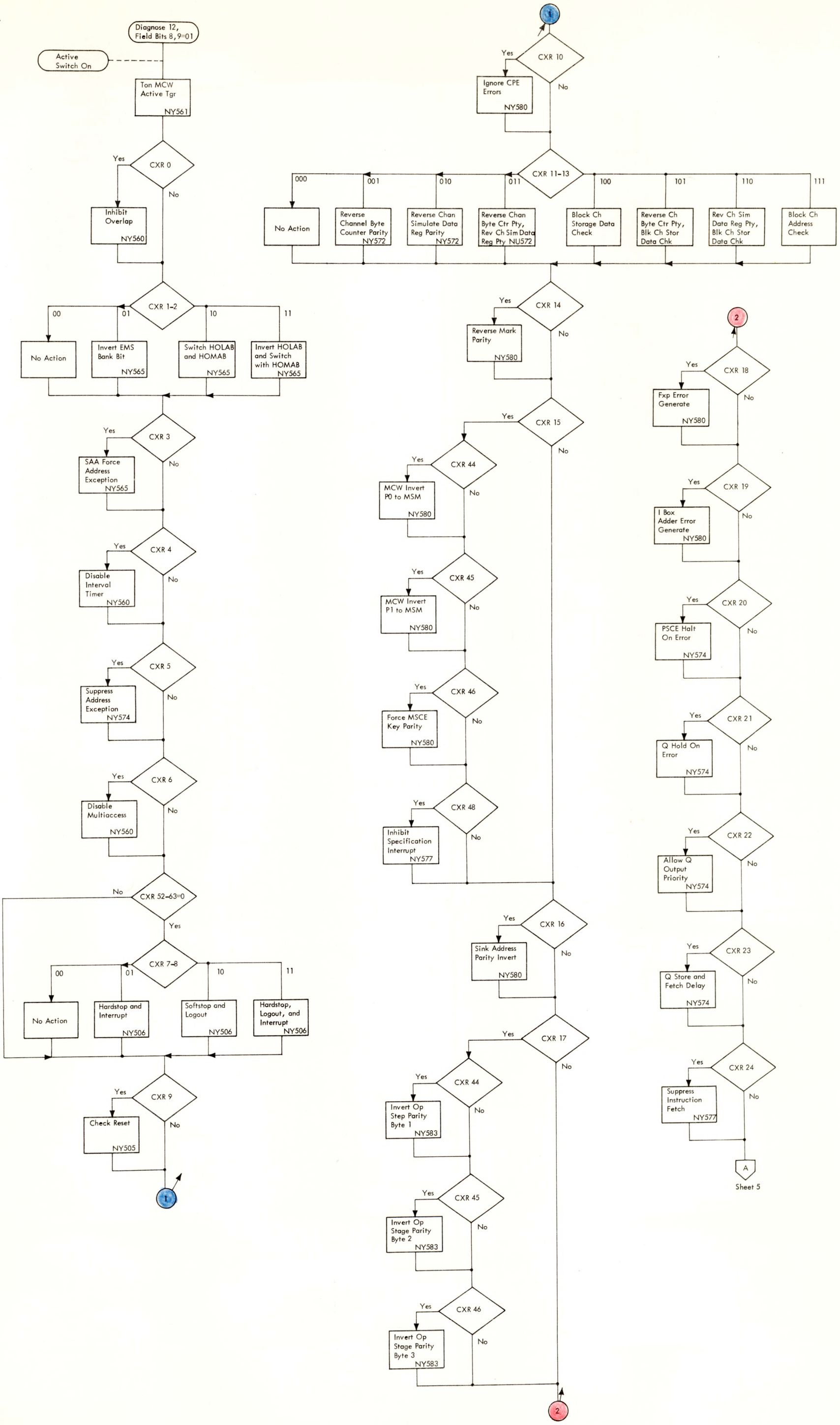


DIAGRAM 5-516. DIAGNOSE AND MCW (SHEET 4 OF 5)

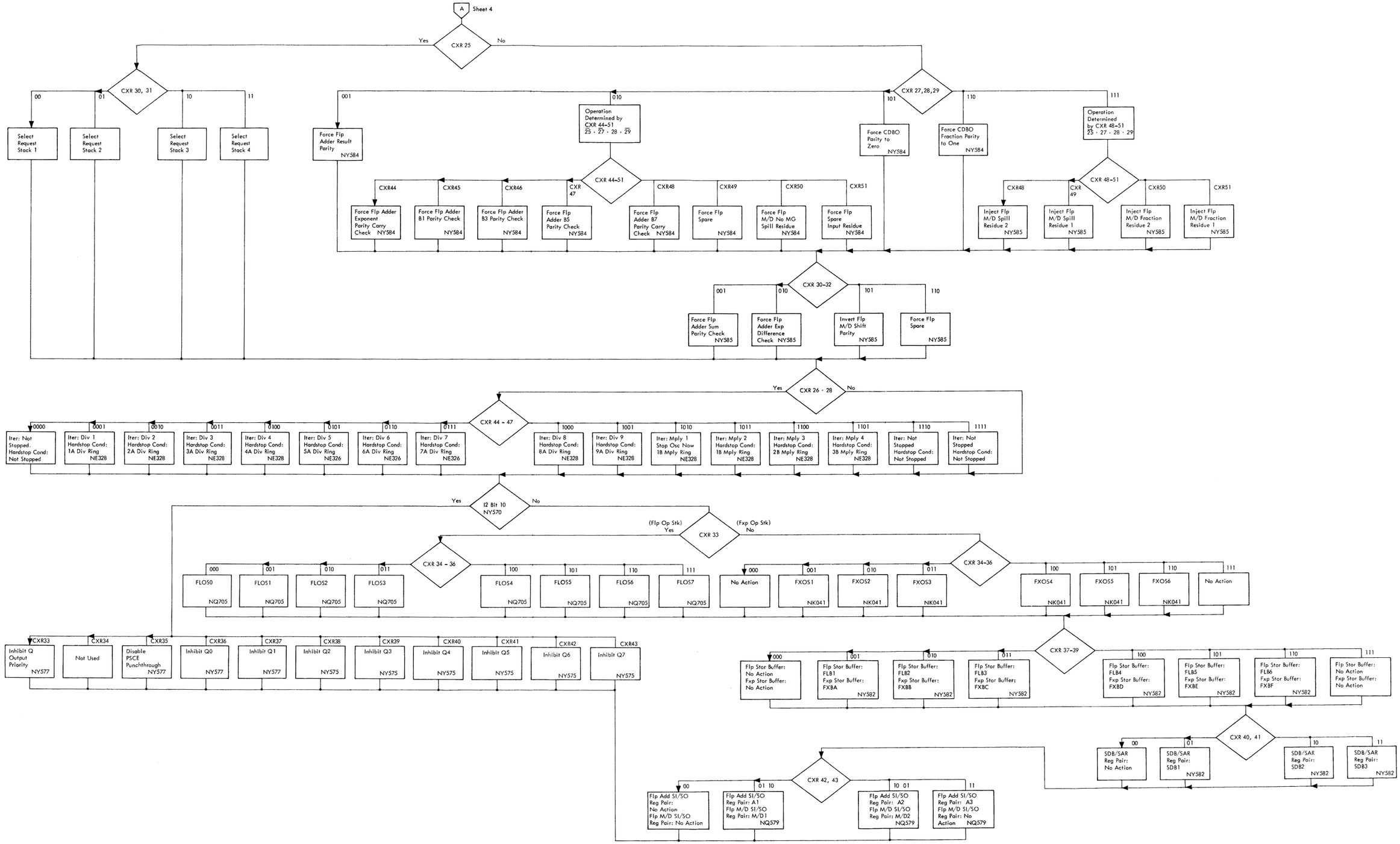


DIAGRAM 5-516. DIAGNOSE AND MCW (SHEET 5 OF 5)

Objective:
To read or backspace one record on MC Tape Unit.

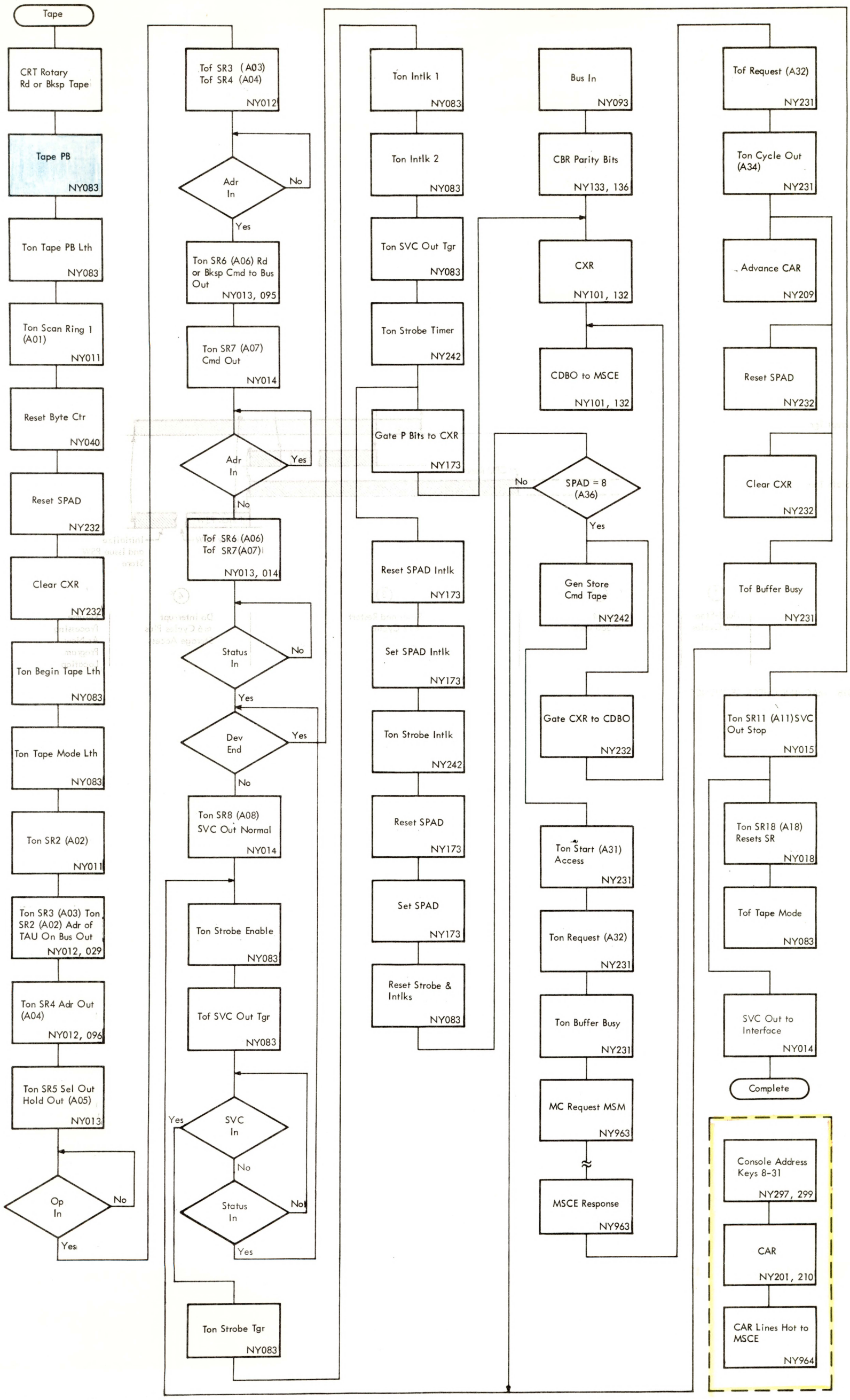


DIAGRAM 5-517. MC TAPE OPERATIONS

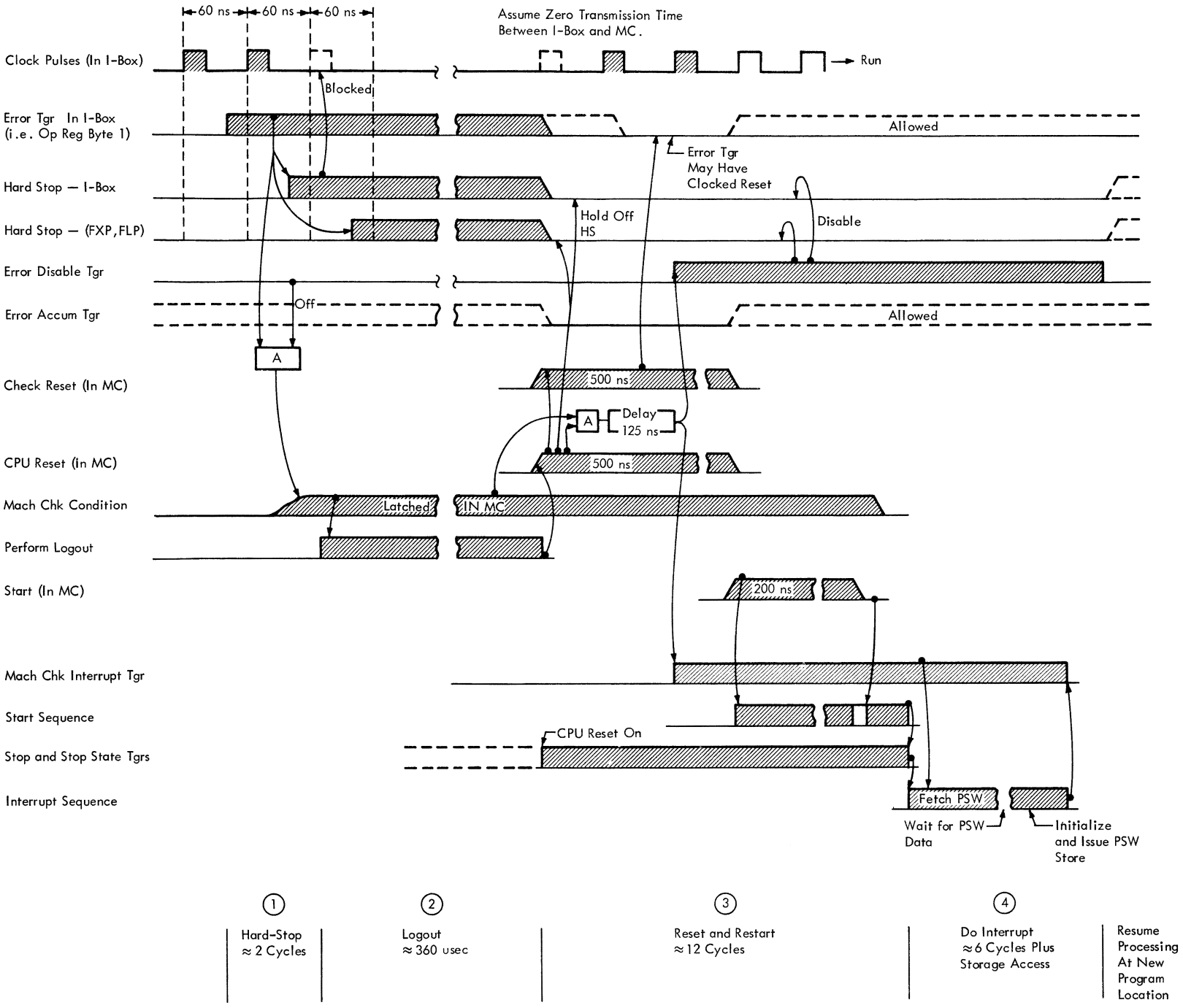


DIAGRAM 5-518. MACHINE CHECK SEQUENCE

Frame 10 Manual Control Triggers

Address Compare Hardstop Trigger - NM533
Turned on when any address compare is found and the MC address compare rotary is on any hardstop or loop position. It controls the turn on of all hardstop triggers for CPU.

Address Compare Sync Trigger - NM533
Turned on by any address compare between the console address keys and I box instruction address or MSCE store address or between PSCE address bus and PSCE address keys. The trigger provides an oscilloscope sync pulse to the I, E, F boxes and the MC.

Address Compare Trigger - NM533
A timing trigger that synchronizes the CPC = 0 to the address compare hardstop or loop function.

Block Pulse Trigger - NM547
This trigger is used in conjunction with the SP1 and SP2 triggers.

Enter Instruction Trigger - NM509
Provides control for performing the enter instruction (buffer) function of the MC.

Error Accumulation Trigger - NM551
Indicates that one or more machine check errors have occurred during a time when the Error Disable Trigger was on or PSW bit 13 was not a one.

Error Disable Latch and Trigger - NM549
Inhibits turning on any hardstop triggers because of machine check errors during an interrupt sequence or during single cycle operation.

Error Disable Turn Off Trigger - NM549
Reset the Error Disable Trigger. It is activated by exit from single cycle mode or by the completion of an interrupt.

FLA M/D SC Rate Trigger - NM543
Turned on with the first start PB depression when the rate switch is in the single pulse position. It controls the clock pulse gating to allow only the FLA M/D units to see a pulse during FLA M/D operations.

FLA M/D SC Trigger - NM543
Turned on when the FLA M/D Rate Trigger is on and a FLA M/D unit is in use. It controls the turning on of the FLA M/D unit single pulse trigger in the E box.

Force Loop Trigger - NM509
Turned on by the address compare function of the MC to control the various looping sequences.

I Box IPL Trigger - NM521
Turned on by IPL and PSW restart to control the I box functions of these operations.

Instruction Step Trigger - NM507
Provides control for the instruction step and multi-step positions of the rate switch.

Manual FLR Load Trigger - NM527
Turned on by a manual FLR store operation from the MC. It controls the M ring and various gating lines to complete the operation.

Manual Function Turn Off Latch - NM507
Provides a reset for the enter instruction, repeat instruction, force loop, set IC, set PSW and I box IPL triggers.

Manual GPR Load Trigger - NM527
Turned on by a manual store into a GPR from the MC. It controls the M ring and various gating lines for completing the operation.

Manual Store Initialize Trigger - NM527
Turned on by a manual store into storage from the MC. It controls starting the M ring and gating the functions of the operation.

Manual Store Turn Off Latch - NM529
Turned on by manual store initialize, manual GPR load or manual FLR load. Its function is to turn off the trigger that turned it on at the proper time during the operation.

Manual Trigger - NM503
On during single cycle mode to disable the interrupt signal to the MC.

M0 Turn On Latch - NM537
Controls the resetting of the M1, M2, M3 triggers.

M1, M2, M3 Triggers - NM535
These three triggers are used in manual operations as a timing ring to sequence various gating and controls.

Overlap Trigger - NM507
Turned on when the inhibit overlap switch is not active to allow the CPU to operate in the overlap mode.

Pseudo Auto Trigger - NM545
Turned on when leaving single cycle mode (rate switch off single cycle position). It forces continuous clock pulses to all execution units until normal Stop State is achieved with all single cycle controls off.

Repeat Instruction Trigger - NM509
Provides control for performing the enter instruction (storage) function of the MC.

Restart Trigger - NM515
Turned on by enter instruction (storage or buffer) to sequence the restarting of CPU each time the instruction is executed.

Set IC Trigger - NM521
Turned on by set IC, IPL, set PSW and PSW restart to control the various I box functions associated with these operations.

Set PSW Trigger - NM521
Turned on by IPL, set PSW and PSW restart to control the I box functions of these operations.

Single Cycle 1 Trigger - NM541
This trigger is the basic control for single cycle operation, controlling the gating of a single clock cycle to the execution areas.

Single Cycle 2 Trigger - NM541
This trigger is the first sequence point upon entering single cycle mode.

Single Instruction Decode Trigger - NM511
Turned on when doing a non-overlap operation (perform one instruction completely before decoding the next). Non-overlap is active during inhibit overlap (switch), instruction step, multi-step and enter instruction. The single instruction decode trigger inhibits decoding an instruction while a previous instruction is being executed.

SP1 and SP2 Triggers - NM547
These two triggers are timing triggers used to control the gating of a single clock cycle to all execution units when in single cycle mode.

DIAGRAM 5-519. MC TRIGGER LIST (SHEET 1 OF 3)

Start 0 Trigger - NM501
The first trigger in the start sequence. Turned on by the Start PB pulse or any start or restart condition arising from the various manual or programmed functions. Turned off by a clock pulse.

Start 1 Trigger - NM503
The second trigger in the start sequence. Synchronizes the Start 0 Trigger to various functions in the starting sequence. Turned off by a clock pulse.

Start 2 Trigger - NM505
The final step in the starting sequence. This trigger takes the CPU out of stop state. The start 2 trigger is a logical sequence point for single cycle, instruction step, overlap and enter instruction operations.

Stop Decode Trigger - NM531
Turned on when the single instruction decode trigger is on to inhibit decoding an instruction until the preceding instruction has been completely processed. It is also turned on to inhibit decoding after an address compare soft stop condition has been detected.

Stop Trigger - NM531
Turned on by any condition which is to result in stopping CPU operation. It is the first trigger in the stopping sequence.

Stop State Trigger - NM513
Turned on when CPU stop trigger is on, all execution and I box pipelines are empty, and no unconditional interrupts are pending. The stop state trigger signals the cessation of all CPU processing.

Frame 1 Control Triggers and Lines

Any Pushbutton Trigger - NY503
Turned on by MC pushbutton. Fires 350 ns, 500 ns, or 152 ns singleshots to start operation of selected pushbutton.

Backspace Command - NY013
Brought up by depressing backspace switch on MC, tape mode and scan ring 6. Forces bits 2, 5, 6 and 7 on bus out. This is a backspace record command to TAU.

Begin Message Display - NY081
Turned on by diagnose instruction I2 field bits 8 and 9 = 10, CRT rotary switch on message display position, brings up message display to scan. Starts the scan ring and resets the byte counter to zero.

Buffer Busy Trigger - NY231
Turned on by start access. Acts as interlock to prevent another start access, and controls ending sequence in MC store and fetch operations.

CE Mode - NY555
Brought up by key switch on MC. Enables CE meter; disables customer meter. Allows MCW to Queue, MCW Active, Block Scan, Inhibit Multi-access to MSCE, Inhibit Overlap, Disable Interval Timer, Hardstop, conditions of Continuous Repeat, and Enter Instruction.

Clear CXR - NY231, NY227
Brought up by tfr CXR pushbutton, logout and diagnose. Resets CXR. Starts CPC clock during diagnose.

Command Interlock Trigger - NY542
Turned on by manual store or fetch, or log store command. Prevents initiating another store or fetch while there is one outstanding.

Continuous Repeat - NY561
Switch on MC in repeat position and any of several pushbuttons held down, will repeat their operation every 16 ms.

CPC Clock - NY227
Set from MCW count field or CPC load rotary switches. Controls number of machine cycle during MCW operation or after address compare.

CPC Enable Trigger - NY522
Turned on by SPAD 15. Controls start and load CPC when address compare rotary switch is in hardstop and loop position.

Cycle Out Trigger - NY231
Turned on by fall of request trigger. Turns off manual fetch or store, and command interlock. Signals the end of manual fetch or store operations.

Data Display Bus - NY056
ORing of log bus, CBR, or CAR data bits to hex to EBCDIC translator, to be gated to 2250 on CRT display operations.

Delay Interlock Trigger and Start Delay - NY563
Turned on when using SPAD as counter during address compare loop or when using repeat or repeat and reset switches.

Delay Trigger - NY173
Turned on by start delay trigger. Reset by SPAD equals 15. Gates the stepping of SPAD.

Diagnose Not Log - NY570
I2 field of diagnose instruction 8 and 9 = 00, 01, or 10. Brings up MCW sink tag turn on.

End of Message - NY081
Line brought up by EOB decode, message display of diagnose instruction.

EOB Decode - NY081
During diagnose message display a byte containing hex 26 will bring up EOB. EOB is decoded off the bus from CBR to bus out, after byte counter is stepped, but before byte is sent to the 2250.

Fetch Trigger - NY231
Turned on by fetch command and not buffer busy. Initiates a fetch to MSCE.

Fetch Command - NY542
Line brought up by storage test fetch, or manual display, or scan ring 15 (storage scan), or message display (diagnose).

Fetch Complete - NY173
Line brought up after each doubleword fetch from storage is complete during storage display (scan), or message display (diagnose). Turns on scan ring 16. Resets message fetch request during message display.

Format A - NY077
Register display (scan), register having more than 36 bits. Decoded by word counter. Register must begin in bit location 0.

Format B - NY077
Register display (scan), register having more than 9 bits and equal to or less than 36 bits. Only 2 registers per doubleword allowed. First register must begin in bit location 0, second register must begin in location 36, but may be unused.

Format C - NY077
Register display (scan), register equal to or less than 9 bits, first register must begin in location 0, the second in bit location 9, the third in location 18, etc. Only 1 register per register position allowed and no unused register positions may exist between used position.

Gate Data Trigger - NY081
Used on message display to gate CBR to bus out to 2250, under control of the byte counter.

Gate LB Trigger, Gate UB Trigger - NY088
Gate UB register or LB register to IC portion of PSW indicators in the MC. The IC is valid only after a scan has been done.

Hardstop Bit 8 - NY506
MCW bit 8 turned on during diagnose instruction when MCW active, I2 field bits 8 and 9 = 01. Causes hardstop to occur when CPC goes to zero.

I2 Field, Bits 8 through 15 - NY576
Controls diagnose instruction functions: logout, hardstop, soft stop, interrupt, message display, and diagnose channel select.

Immediate Logout - NY570
Diagnose instruction I2 field bits 8 and 9 = 11. Exit from diagnose.

Ingate Trigger - NY231
Turned on during a display operation, by the 'DIG Console request' line from MSCE. This signal from MSCE tells the MC to prepare to receive request data.

Inhibit Log Address Step - NY076
On logout brought up by word counter equal to hex 69 through 7F. Prevents advance of CAR.

Interlock 1 Trigger, Interlock 2 Trigger - NY083
On MC tape operations provides timing pulses for data service cycle.

Interrupt Trigger - NY552
Turned on by machine check, and machine check not masked in PSW. Also by diagnose instruction with MCW active, MCW bit 8 or 26, and CPC equal zero.

IPL Local Trigger - NY507
Turned on by load pushbutton on MC. Starts initial load routine.

IPL Pulse - NY507
Result of IPL pushbutton and 350 ns pulse. Causes system reset and sets IPL trigger.

Instruction Register Triggers - NY089
Bits 25 through 31 turned on when doing a CPU register scan. Forms PSW IC lights to MC. Bit 25 provides gating for UB or LB.

Last Word Fetched - NY172
During a logout, turned on when 8 doublewords have been fetched. On CRT storage display, brought up by SPAD = 16 hex 0000, indicating that 16 doublewords have been fetched.

Last Word Logged - NY085
During a logout brought up by Hi 12 and Low 1. The last word decoded by the word counter.

Last Word Used Trigger - NY019
On CPU or bus scan, turned on by last word, bus display hex B8, or last word CPU display hex 50, decoded by word counter. Also turned on by message EOB.

Load CPC - NY522
Brought up by any address compare hardstop or loop and SPAD = 15.

Load MCW Trigger - NY227
Turned on during diagnose instruction when sink tag interlock trigger on.

Log Trigger - NY506
Turned on by diagnose instruction logout, machine check interrupt, or CPC = 0 and MCW active. To initiate logout.

Log Completed - NY506
Turned on by diagnose logout completed. Brings up start pulse.

Log Store Completed - NY172
Brought up by log and start access or log and strobe timer on a tape operation. Turns on log ring 5.

Log Ring - NY080
- Log Ring 1 - Logout running
- Log Ring 2 - Set word counter
- Log Ring 3 - Set CAR to 128
- Log Ring 4 - Store command
- Log Ring 5 - One up word counter
- Log Ring 6 - Logout completed

Manual Fetch Trigger - NY542
Turned on by store/display switch on MC in storage position and depressing display pushbutton. Initiates manual display.

MCW Active Trigger - NY561
Turned on by diagnose instruction I2 field bits 8 and 9 = 01.

MCW Latched Bits 0-4 - Bit 0-NY560, Bits 1-3-NY565, Bit 4-NY560
Turned on during diagnose instruction MCW active trigger and CXR bits 0 through 4. Used to prevent MCW bits 0 through 4 from being destroyed when logout occurs.

MCW Load Control Trigger - NY227
Turned on during diagnose instruction by MCW sink tag interlock trigger. Transfers MCW to CXR.

MCW Sink Tag Trigger - NY227
Turned on during diagnose instruction with I2 field bits 8 and 9 equal to anything but 11.

MCW Sink Tag Interlock Trigger - NY227
Brought up during diagnose instruction by message display switch on or L2 field bits 8 and 9 = 00, 01 or 11. This turns on MCW load control.

Message Display Latch - NY508
Turned on during diagnose instruction with I2 field bits 8 and 9 = 10 and CRT display switch set to message display.

Message Fetch Request Trigger - NY081
Turned on during diagnose instruction message display, when byte counter equals 0. Initiates a fetch for a doubleword from storage.

Message Service Out Trigger - NY081
Turned on during diagnose instruction service cycle. Gates data to the 2250 under control of the byte counter.

MSB Gate to PSCE - NY084
Brought up during logout or scan operations when word counter decodes a PSCE address.

MSB Scan - NY084
Brought up during logout or scan operations when word counter decodes PSCE address.

MSB Response Trigger - NY084
Turned on by MSB response indicating PSCE has accepted fetch request during logout or scan.

Multistep Time Out - NY510
Three 33 ms singleshots give approximately 100 ms delay between start pulses during multistep operation while start pushbutton is depressed.

Null Command - NY077
Line brought up during CPU or bus display when 2250 decodes SM order on an odd address, or data title consists of an odd number of full bytes or an even number of bytes where the right hex character of the last byte is not displayed.

PSCE Data Paths Active - NY575
Brought up by diagnose instruction I2 field bit 10 on and MCW active, or MCW to Queue switch and MCW active. Activate PSCE data paths.

PSW Restart Pulse - NY501
Brought up by depressing PSW restart pushbutton on MC. Initiates system reset and loads PSW from location 0000 and starts instruction fetching and execution.

PSW Restart or IPL T1, T2 - NY521
Turned on sequentially by PSW restart or load pushbutton to bring up system reset and PSW restart CPU, or set IPL latches.

Read Command - NY013
Brought up by tape mode, read switch, and scan ring 6. Places bit 6 on bus out.

Recycle Timer Trigger - NY506
Turned on by diagnose instruction logout or a machine check interrupt, or diagnose hardstop and interrupt. Brings up a start pulse.

Remember Sequence Trigger - NY081
Brought up during diagnose message display by the first step byte counter after a storage fetch to synchronize the message out trigger.

Request Trigger - NY231
Turned on by the start access trigger for either a store or fetch command from MC to storage. It signals a request to MSCE for a storage module.

Reset Buffer Address Counter Trigger - NY036
Used during scan to control incrementing the BAC by 20 bytes or 10 bytes depending on the type of scan.

Reset Card Data Latches - NY018
Turned on by service out card reader (scan ring 17) and not service in. Resets card data latches and scan ring 17.

Reset Format Ring A and B - NY019
This line is activated by system reset, new card from card reader, single register display or scan reset.

Reset Scan Ring - NY019
Same as reset format ring.

Right Hex Character Used - NY076
On CRT (scan) display operations, this line indicates, by word counter decode, that the right half of byte to be processed will be used.

Run CPC Trigger - NY227
This trigger controls the counting of the cyclic program counter. It is turned on by an address compare hardstop or loop operations or by a diagnose instruction which has the MCW loaded into the CXR.

Scan Trigger - NY532
Turned on by scan pushbutton on the MC to initiate a scan operation.

Scan Delay - NY531
A 16 ms singleshot brought up with CRT rotary switch in bus or CPU register position and start pushbutton, or set IC or PSW, or address compare stop, or hardstop pushbutton, or stop pushbutton. Initiates a scan.

Scan Mode - NY011
This control line is activated for logout, single register displays, and CPU and bus scan operations.

Service Out Trigger - NY083
This trigger provides the service out to the TAU on MC tape operations.

Set Even Trigger - NY046
This trigger is used during CRT scan for setting the format ring triggers.

Set IPL Latches - NY521
Brought up as a result of load pushbutton on MC and 350 ns pulse Initiates load routine.

Single Register Display Trigger - NY531
Turned on by store/display rotary switch in FLP register, GPR, or unaddressable register position, and depressing display pushbutton on MC.

Single Register Display Interlock Trigger - NY531
Holds single register display trigger on until reset by single register display reset.

Soft Stop - NY506
Line brought up during diagnose instruction by CXR bit 7, not bit 8, MCW active trigger on and MCW active switch off. Brings up stop signal line to MSCE.

SPAD 15 End Delay - NY172
Brought up by SPAD equal to 15. Used on address compare loop and on continuous repeat operations.

Start Access Trigger - NY231
This trigger is used to initiate all storage fetches or stores from the MC. It will be active on storage test, manual storage display, manual store, message display, scan storage, MC tape operation, and storing on logout.

Start Count - NY522
Line brought up by diagnose instruction or by address compare with address compare switch in any address compare hardstop or loop position. Starts CPC counting.

Start Delay Trigger - NY563
Turned on by address compare loop or by continuous repeat switch to begin stepping SPAD and repeat operation being performed.

DIAGRAM 5-519. MC TRIGGER LIST (SHEET 2 OF 3)

Start Logout - NY552
Line brought up by logout pushbutton on MC, diagnose logout, or external machine check and stop line to initiate a logout operation.

Start Signal Line - NY504
Line brought up by start, auto start, or single pulse, to either start or continue operations.

Start SPAD - NY561
Line brought up when the repeat switch in on to start stepping the SPAD counter. In repeat mode, the operation of any pushbutton depressed is repeated under control of the SPAD counter.

Start Test Latch - NY540
Turned on by start test pushbutton to initiate a storage, fetch test or store test, determined by setting of store/fetch switch on MC.

Step Byte Counter Trigger - NY081
This trigger is used on diagnose message display. It is stepped during the data service cycle to gate out the eight bytes from the CBR to the bus out to the 2250.

Stop Interlock - NY530
Line brought up by single cycle or single pulse, or CPU in stop state with stop trigger on, or MC test switch not in process. A condition to start scan automatically.

Stop Line - NY532
This line is activated when the I-box stop trigger and stop state trigger are both on. In its active state, it controls various functions, such as manual display, IPL, set PSW, etc.

Storage End Inhibit CAR Advance Trigger - NY541
This trigger is turned on when the CAR has stepped to the end of storage (either MWS or EMS) during storage test. It signals the end of storage and inhibits further stepping of CAR. CAR is reset and operation repeats starting at location 0.

Store Command - NY542
This line signals a MC store operation to storage. It is activated by storage test, store, MC tape operation, manual store or logout.

Strobe Trigger - NY083
This trigger is used on MC tape operations. Its function is to gate various lines in the data cycle to move data from the bus in to the CXR in preparation for storing into storage.

Strobe Enable Trigger - NY083
This trigger is used in MC tape operations. It acts as a timing trigger in the data cycle and precedes the strobe trigger in sequence.

Strobe Timer and Strobe Timer Interlock Trigger - NY242
These two triggers are used on MC tape operations. They provide timed pulses used to step SPAD in order to control gating the bus in into the CXR bytes.

Tape Begin Trigger - NY083
This trigger is used on MC tape operations. It is turned on at the beginning of the operation and is used to control the reset of SPAD, clear CXR, and turns on tape mode trigger.

Tape Mode Trigger - NY083
This trigger is turned on by tape begin trigger and remains on throughout the MC tape operation. It gates read or backspace command, TAU address, and bus in to MC.

Tape or Message Start - NY083
This line is used on MC tape operations or diagnose message displays. It starts the scan ring and resets the byte counter to zero.

Tape Pushbutton Trigger - NY083
This is the integrating latch to provide a starting point in the MC tape operation.

This Byte Used - NY051
This line is used during scan. It is a result of word counter decoding, and controls the operation of the format ring.

Timing Trigger - NY041
This trigger is used in the scan operation. Its function is to synchronize the service-in, service-out data cycle to the 2250.

Transfer CXR and Transfer CBR to CXR Trigger - NY501
These triggers latch the transfer CBR to CXR pushbutton pulse of the MC in order to time the operation.

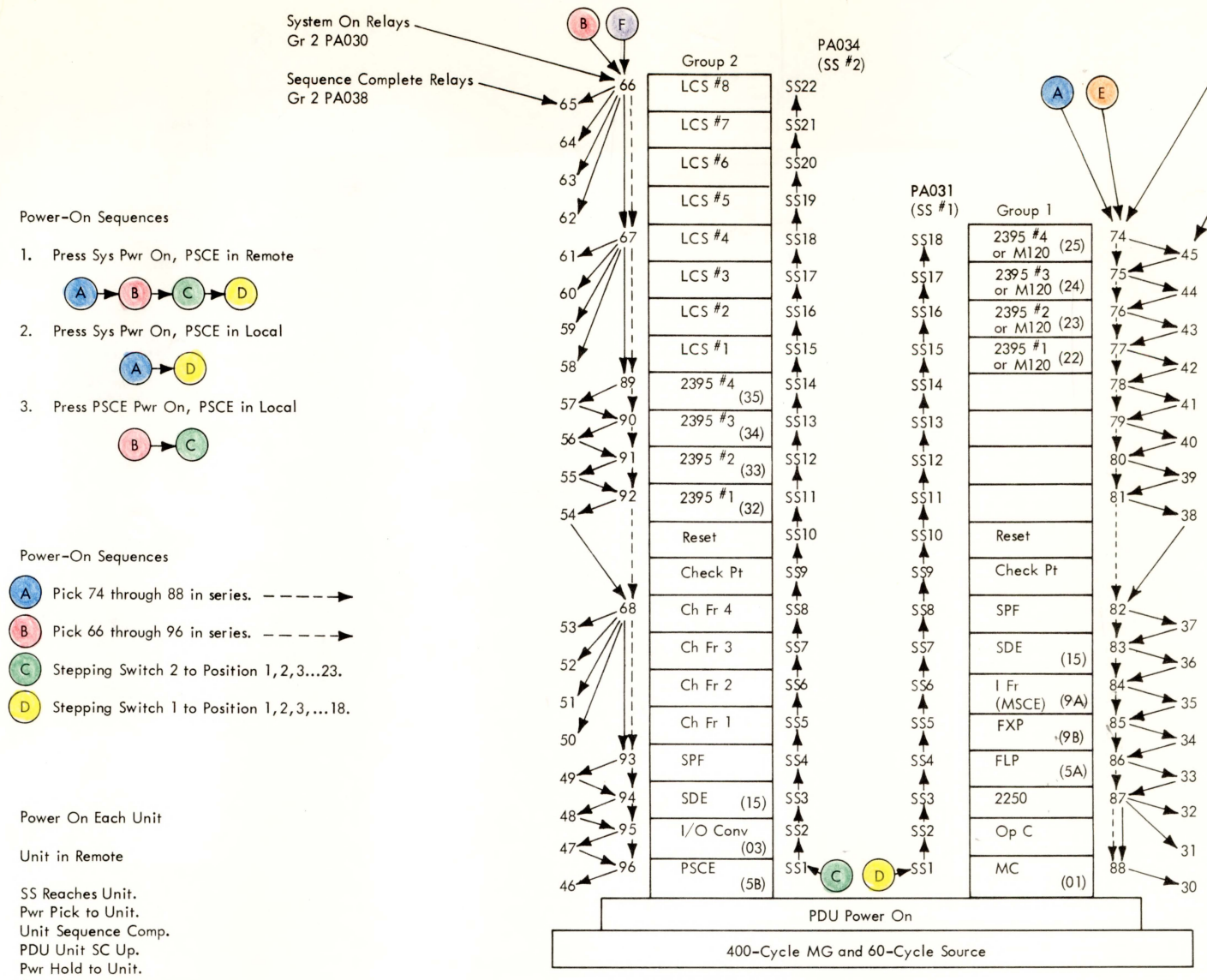
150 ns Pulse - NY504
A 150 ns singleshot fired by external interrupt pushbutton to initiate an external interrupt.

1 usec Pulse - NY502
1 usec pulse comes up when system reset, computer reset, or check reset pushbuttons on MC are depressed. Initiates resets.

DIAGRAM 5-519. MC TRIGGER LIST (SHEET 3 OF 3)

Gen	General; Generate
GP Acpt	General Purpose Register Accept
GPR	General Purpose Register
Gr	Group
Gt	Gate
Gtd	Gated
GWFCDB	Go When Full Common Data Bus
GWFFLBB	Go When Full Floating Buffer Bus
HIO	(Mnemonic) Halt I/O (SI)
HPMS	High Performance Main Storage
HOD	High Order Digit
HS	Half Sum
HSB	High Speed Bus
HW	Halfword
I	Instruction
I-Box	Instruction Processor
IC	(Mnemonic)Insert Character (RX); Instruction Count
IDR	Immediate Data Register
IF	Instruction Fetch
IFT	Instruction Fetch Trigger
Ig	Ingate
ILC	Instruction Length Code
IMRT	Instruction from Memory Request Trigger
Incr	Increment
Ind	Indication; Indicator
Inh	Inhibit
Init	Initialize
In Pri	Input Priority
Insn	Instruction
Int	Internal
Intr	Interrupt
Inv	Invalid
I/O	Input/Output
IOC	I/O Channel
IPL	Initial Program Load
IR	Instruction Register
IRCTR	Instruction Register Counter
ISK	(Mnemonic) Insert Storage Key (RR)
ISR	Instruction Sink Register
IWC	Indicator Word Counter
K	Thousand
L	Operand Length
LA	(Mnemonic) Load Address (RX)
Last	Last Trigger
LB	Lower Bound; Loop Block
LBCTR	Lower Bound Counter
L Cnt	Length Count
LCS	Large Capacity Storage (Same as EMS)
Ld	Load
LM	(Mnemonic) Load Multiple (RS)
LO	Low Order
LOD	Low Order Digit
LPSW	(Mnemonic) Load PSW (SI)
LSN	Load Multiple (LM), Store Multiple (STM), and NOXCM Instructions
Lth	Latch
MA	Multi-Access
MAC	Multi-Access Code
MALS	Multi-Access Link Suppressed
Man	Manual
MAR	Memory Address Register (Same as SAR)
MAT	Multi-Access Trigger
MC	Maintenance Console; Megacycle; Marginal Checking
Mcand	Multiplicand
MCW	Maintenance Control Word
M/D	Multiply/Divide
MDR	Memory Data Register (Same as SDR)
Mem	Memory
MG	Motor Generator; Multiple Gate
MOP	Multiple Operation
Mplr	Multiplier
Mple	Multiple
Mod	Modifier
Mply	Muliply
MS	Main Storage (Same as MWS)
MSB	Medium Speed Bus
MSC	Monolithic Storage Cell
MSCE	Main Storage Control Element
MSM	Main Storage Module
MTBF	Mean Time Between Failures
Mul Dec	Multiplier Decoder
MVC	(Mnemonic) Move (SS)
MVN	(Mnemonic) Move Numerics (SS)
MVO	(Mnemonic) Move with Offset (SS)
MVZ	(Mnemonic) Move Zones (SS)
MWS	Main Working Storage (Same as MS)

N	Inverter
NC	Mnemonic AND (SS)
Neg	Negative
NIAT	New Instruction Address Trigger
No.	Number
N Op	No Operation
Norm	Normalize
NOXCM	(Mnemonic) NC (AND) OC (OR) XC (Exclusive OR) CLC (Compare Logical) MVC (Move) MVZ (Move Zone) MVN (Move Numeric)
Ns	Nanosecond
NSI	Next Sequential Instruction
NUBAT	New Upper Bound Address Trigger
OC	(Mnemonic) OR (SS)
Oflo	Overflow
Og	Outgate
Olap	Overlap
Op	Operation
Opnd	Operand
OR	Outring (Line Name Only)
Out Pri	Output Priority
Ord	Order
Osc	Oscillator
Ovrd	Override
Ovrlp	Overlap
P	Parity; Position; Priority
PA	Propagate Adder
PACK	(Mnemonic) Pack (SS)
Par	Parity
PAR	Position Address Register
PAW	Position Address Word
PC	Parity Check
PDU	Power Distribution Unit
PG	Parity Generate
PH	Polarity Hold
PK	Protection Key
PM	Program Mask; Protect Memory (Same as PS)
Pos	Position; Positive
PPE	Peripheral Processor Element
PPln	Pipeline
Prec	Precision
Pred	Predict
Pri	Primary; Priority
Prob	Problem
Prog	Program
Prop	Propagate
Prot	Protect; Protection
PS	Protect Storage (Same as PM); Power Supply
PSCE	Peripheral Storage Control Element
PSW	Program Status Word
Ptrn	Pattern
Pty	Parity
PUMO	(Mnemonic) PACK (Pack) UNPK (Unpack) MVO (Move with Offset)
PV	Protection Violation
Pwd	Powered
Q	Queue
Qx	Queue (any number)
R	Ready
Rd	Read
RDD	(Mnemonic) Read Direct (SI)
Rdy	Ready
Rec	Record
Reg	Register
Rel	Release
Req	Request
Res	Reset; Residue
Resd	Reserved
Resp	Response
Rgen	Regenerate; Regeneration
RI	Read In
R/L	Remote/Local
RO	Read Out
RR	(Instruction Format) Both Operands from GPR's
RS	Request Stack; (Instruction Format) One Operand from a GPR, the Other from Storage
Rslt	Result
Rsrvtn	Reservation
Rt	Right
Rtn	Return
RUA	Register Unavailable for Address Generation
RUM	Register Unavailable for Modification



Power-On Sequences

1. Press Sys Pwr On, PSCE in Remote

2. Press Sys Pwr On, PSCE in Local

3. Press PSCE Pwr On, PSCE in Local

Power-On Sequences

A — Pick 74 through 88 in series. - - - - →

B — Pick 66 through 96 in series. - - - - →

C — Stepping Switch 2 to Position 1, 2, 3...23.

D — Stepping Switch 1 to Position 1, 2, 3, ...18.

Power On Each Unit

Unit in Remote

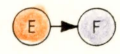
SS Reaches Unit.
Pwr Pick to Unit.
Unit Sequence Comp.
PDU Unit SC Up.
Pwr Hold to Unit.
Step SS.

Unit in Local

SS Reaches Unit
PDU Unit SC Up.
Step SS.

Power Down Sequences

1. Press Sys Power Off, PSCE in Remote



2. Press Sys Power Off, PSCE in Local

3. Press PSCE Pwr Off, PSCE in Local

Power-Off Sequences

E — Drop 74 through 30 in Series. Unit in Remote ——→. Unit in Local - - -→.

F — Drop 66 through 46 in Series. Unit in Remote ——→. Unit in Local - - -→.

Power Off Each Unit

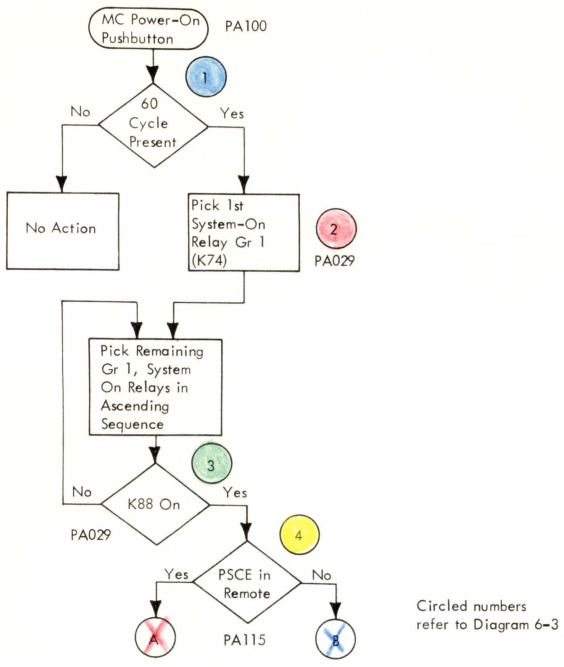
Unit in Remote

Unit Sys-On Relay Down.
Unit Power Down.
PDU Unit SC Down.
Next Unit Sys-On Down.

Unit in Local

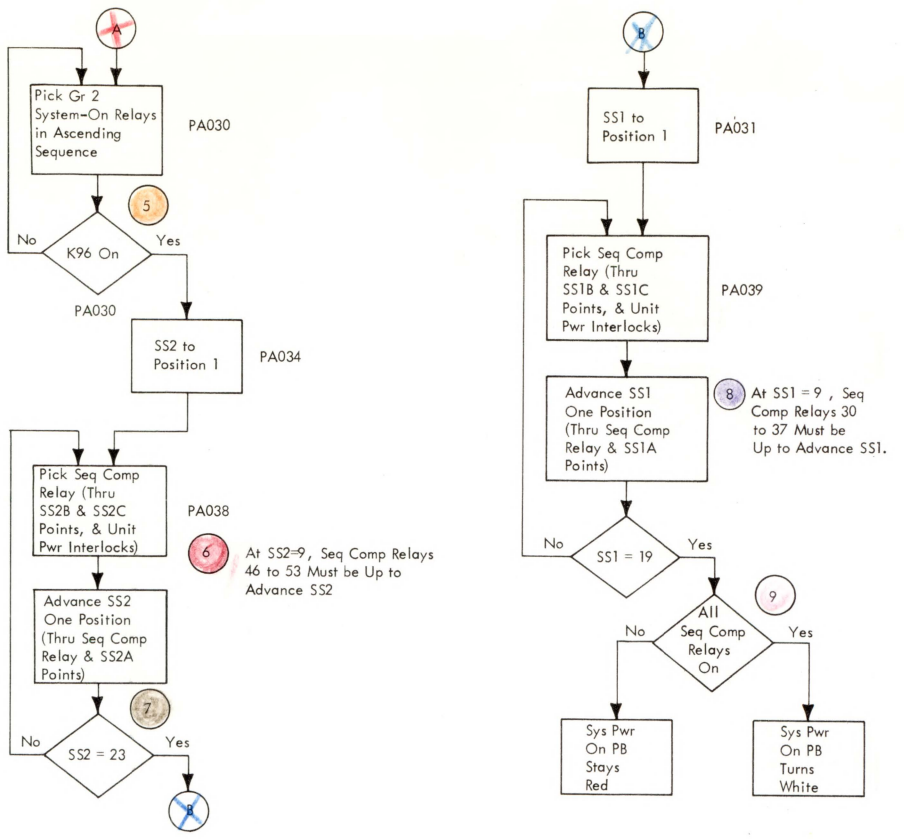
Sys-On Relay Down.
Next Unit Sys-On
Relay Down.

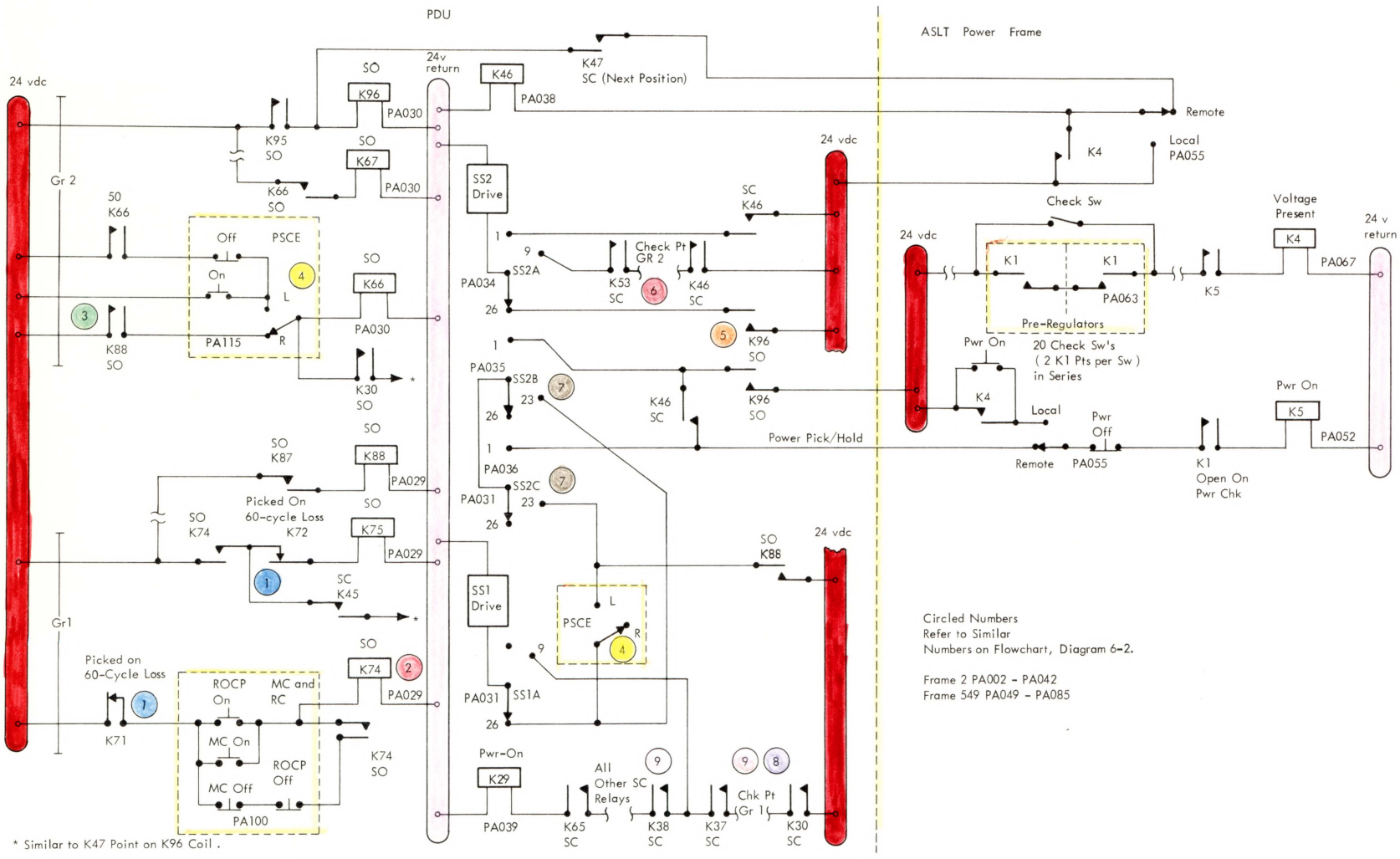
DIAGRAM 6-1. POWER-ON AND-OFF SEQUENCES



Circled numbers refer to Diagram 6-3

DIAGRAM 6-2. SYSTEM POWER-ON SEQUENCE



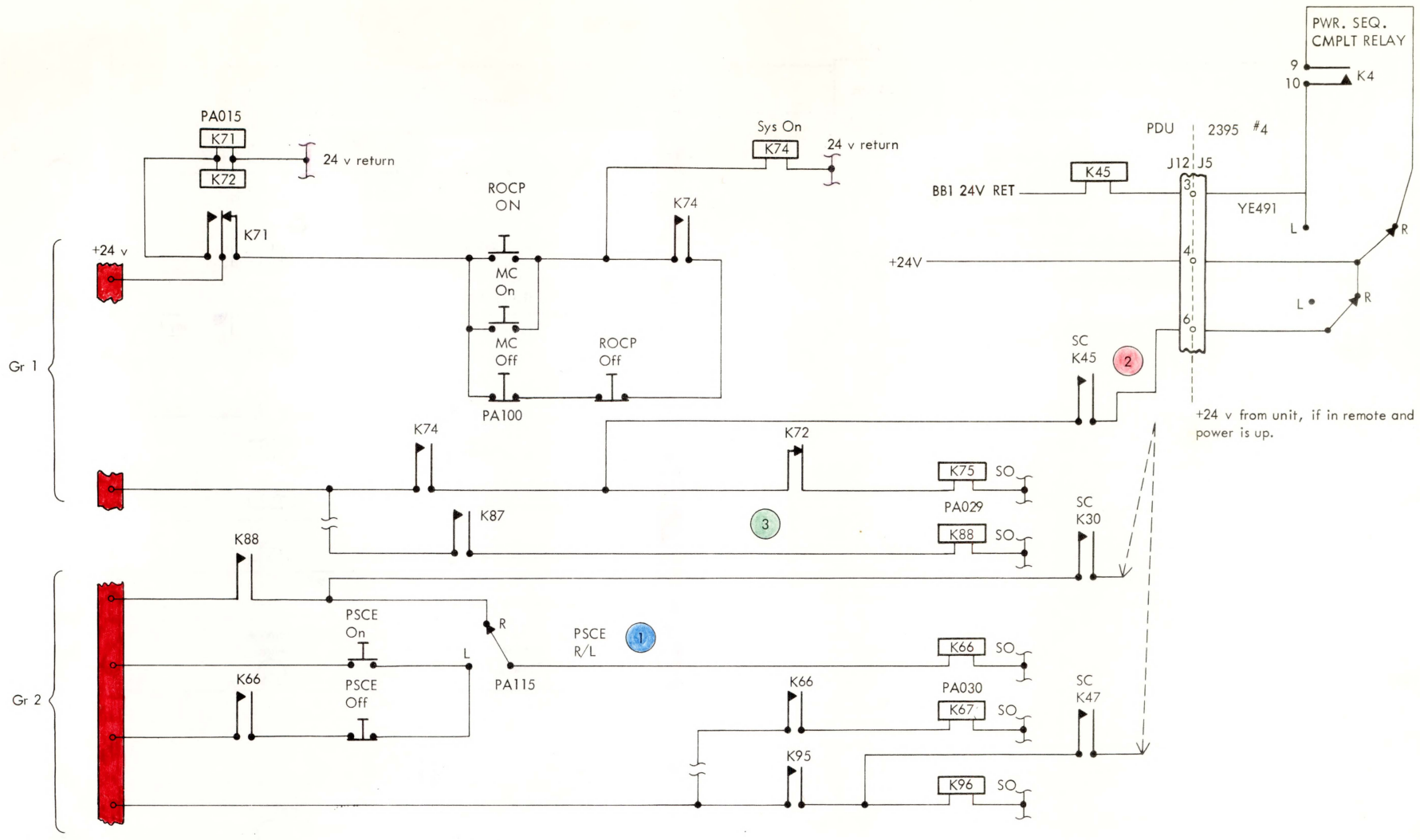


Circled Numbers
Refer to Similar
Numbers on Flowchart, Diagram 6-2.

Frame 2 PA002 - PA042
Frame 549 PA049 - PA085

* Similar to K47 Point on K96 Coil.

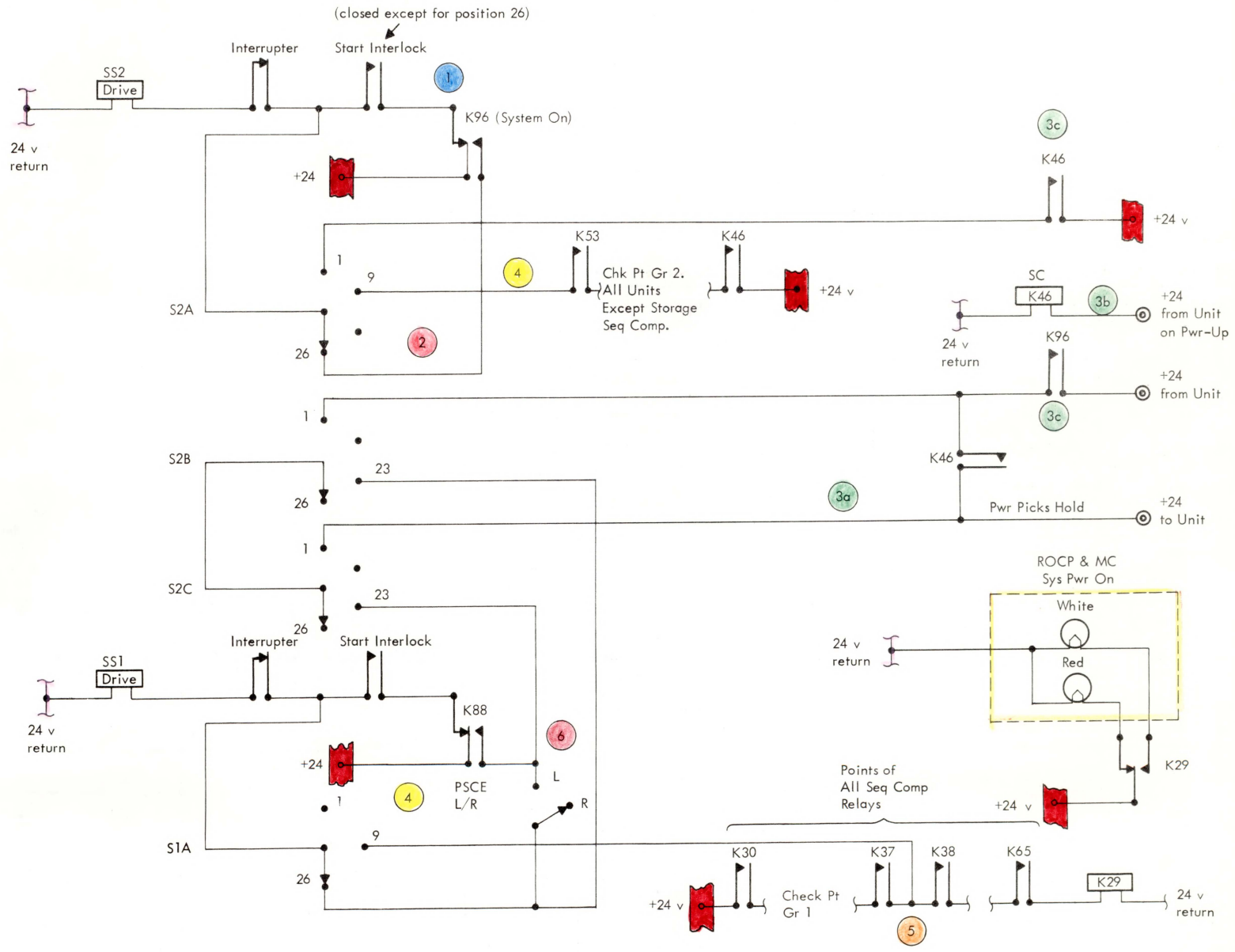
DIAGRAM 6-3. SYSTEM POWER-ON, ASLT FRAME



Sequences are shown on Diagram 6-1

1. PSCE Remote/Local switch isolates or joins groups 1 and 2.
2. On power-down sequences, the system on relay for a unit is not dropped until the prior unit has sequenced down. (Units following LCS or Channels do not wait.)
3. When a 60-cycle power loss is detected, K71 and K72 are picked. The system-on relays for all high-speed storage units are dropped immediately; storage power goes down. The remainder of the system then sequences down normally if time permits.

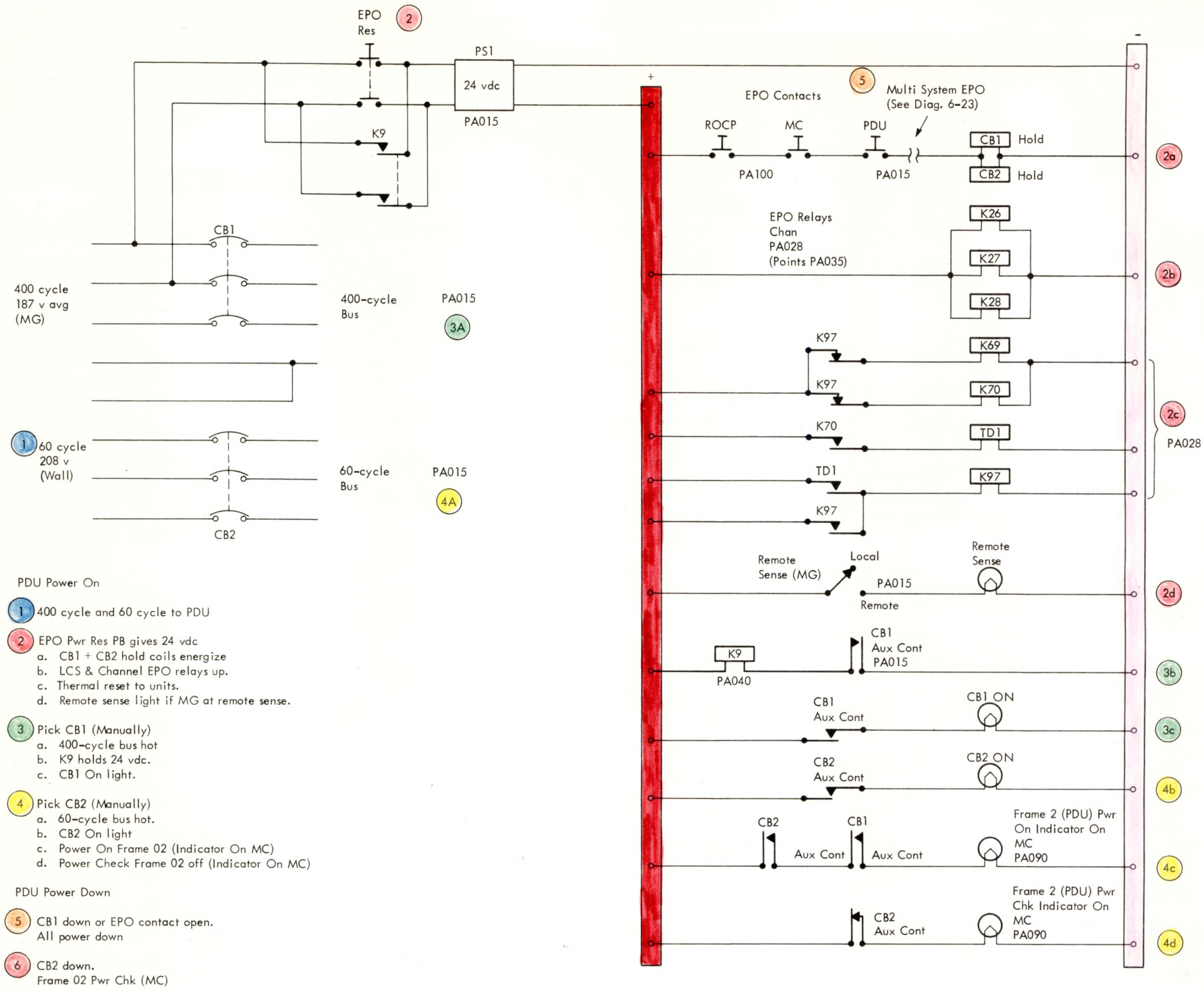
DIAGRAM 6-4. SYSTEM-ON RELAYS; PICKS AND HOLDS



Sequences are shown on Diagram 6-1.

1. System on down steps switch to position 26 (start).
2. System on up steps switch to position 1.
3a. Stepping switch in unit position, sends power pick to unit.
3b. Unit powers up and then picks sequence complete in PDU.
3c. SC up sends power hold to unit and steps switch to next position.
4. Position 9 both switches checks that all units except storage are up before storage.
5. All units up picks K29 and changes system power on light from red to white.
6. PSCE L/R switch isolates or joins groups 1 and 2. If switch in remote, stepping switch 2 must go to position 23 before switch 1 can start stepping.

DIAGRAM 6-5. STEPPING SWITCH OPERATION



PDU Power On

1 400 cycle and 60 cycle to PDU

2 EPO Pwr Res PB gives 24 vdc
- a. CB1 + CB2 hold coils energize
- b. LCS & Channel EPO relays up.
- c. Thermal reset to units.
- d. Remote sense light if MG at remote sense.

3 Pick CB1 (Manually)
- a. 400-cycle bus hot
- b. K9 holds 24 vdc.
- c. CB1 On light.

4 Pick CB2 (Manually)
- a. 60-cycle bus hot.
- b. CB2 On light
- c. Power On Frame 02 (Indicator On MC)
- d. Power Check Frame 02 off (Indicator On MC)

PDU Power Down

5 CB1 down or EPO contact open.
All power down

6 CB2 down.
Frame 02 Pwr Chk (MC)

DIAGRAM 6-6. PDU POWER, ON AND OFF

Table 1 --

PDU 400-Cycle CB's and Contactors

Power Frame - Unit	CB - Page	K - Page
01 - MC	16 PA016	19 PA016
03 - I/O Converter	19 PA022	22 PA022
5A - FLP	~~35~~ 34 PA016	
5B - PSCE	~~37~~ 35 PA022	
9A - I-MSCE	36 PA017	
9B - FXP	~~39~~ 37 PA016	
13-15 GR1	17 PA017	20 PA017
13-15 GR1	18 PA017	21 PA017
15 - SDE GRII	20 PA022	23 PA022
15 - SPF GRII	21 PA022	24 PA022
22 - 2395/M120	38 PA020	
23 - 2395/M120	40 PA020	
24 - M120	42 PA020	
25 - M120	44 PA020	
32 - 2395	39 PA023	
33 - 2395	41 PA023	
34 - 2395	43 PA023	
35 - 2395	45 PA023	

Table 2 --

PDU 60-Cycle CB's and Contactors

Power Frame - Unit	CB - Page	K - Page
2250	9 PA016	
01 - MC	10 PA017	19 PA016
03 - I/O Converter	11 PA022	22 PA022
13 - 15 Dist	10 PA017	20 PA017
13 - 15 SPF	10 PA017	21 PA017
15 - SDE GRII	11 PA022	23 PA022
15 - SPF GRII	11 PA022	24 PA022
22 - M120	22 PA019	
22-M120	5 PA021	
23-M120	23 PA019	
23 - M120	6 PA021	
24-M120	24 PA019	
24 - M120	7 PA023	
25-M120	25 PA019	
25 - M120	8 PA023	
32 - 2395	26 PA021	
33 - 2395	27 PA021	
34 - 2395	28 PA021	
35 - 2395	29 PA021	

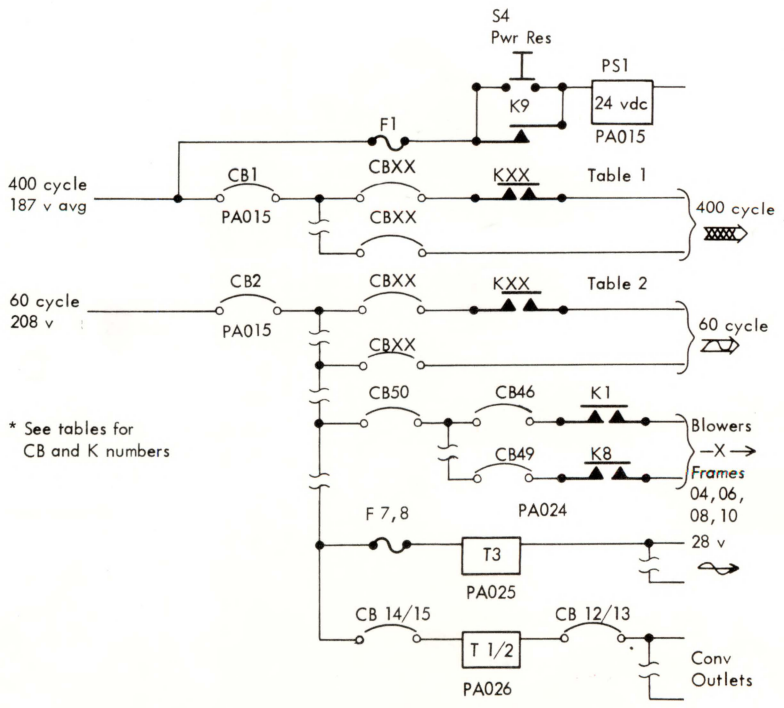


DIAGRAM 6-7. POWER THROUGH PDU

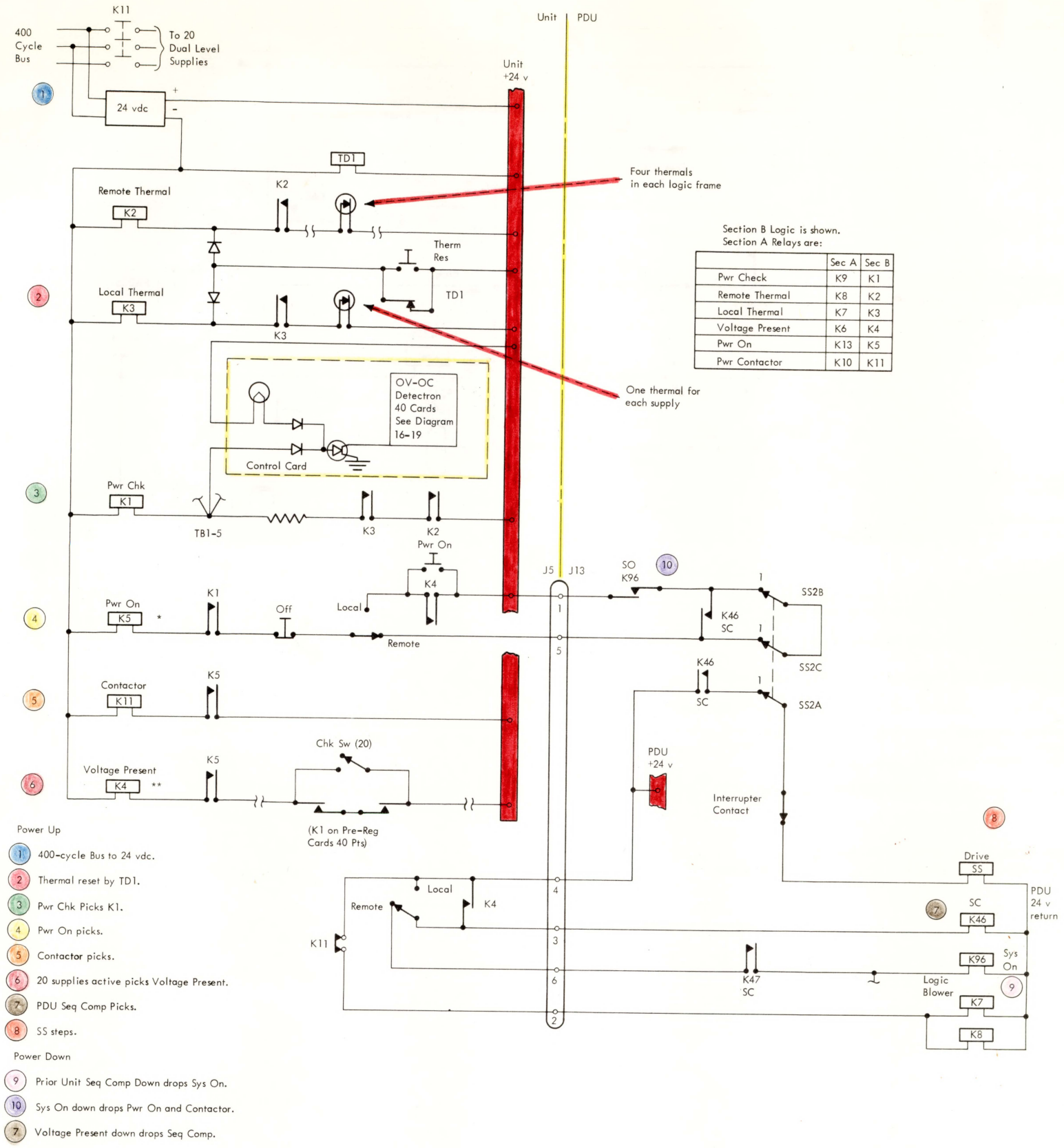


DIAGRAM 6-8. ASLT - PDU INTERFACE

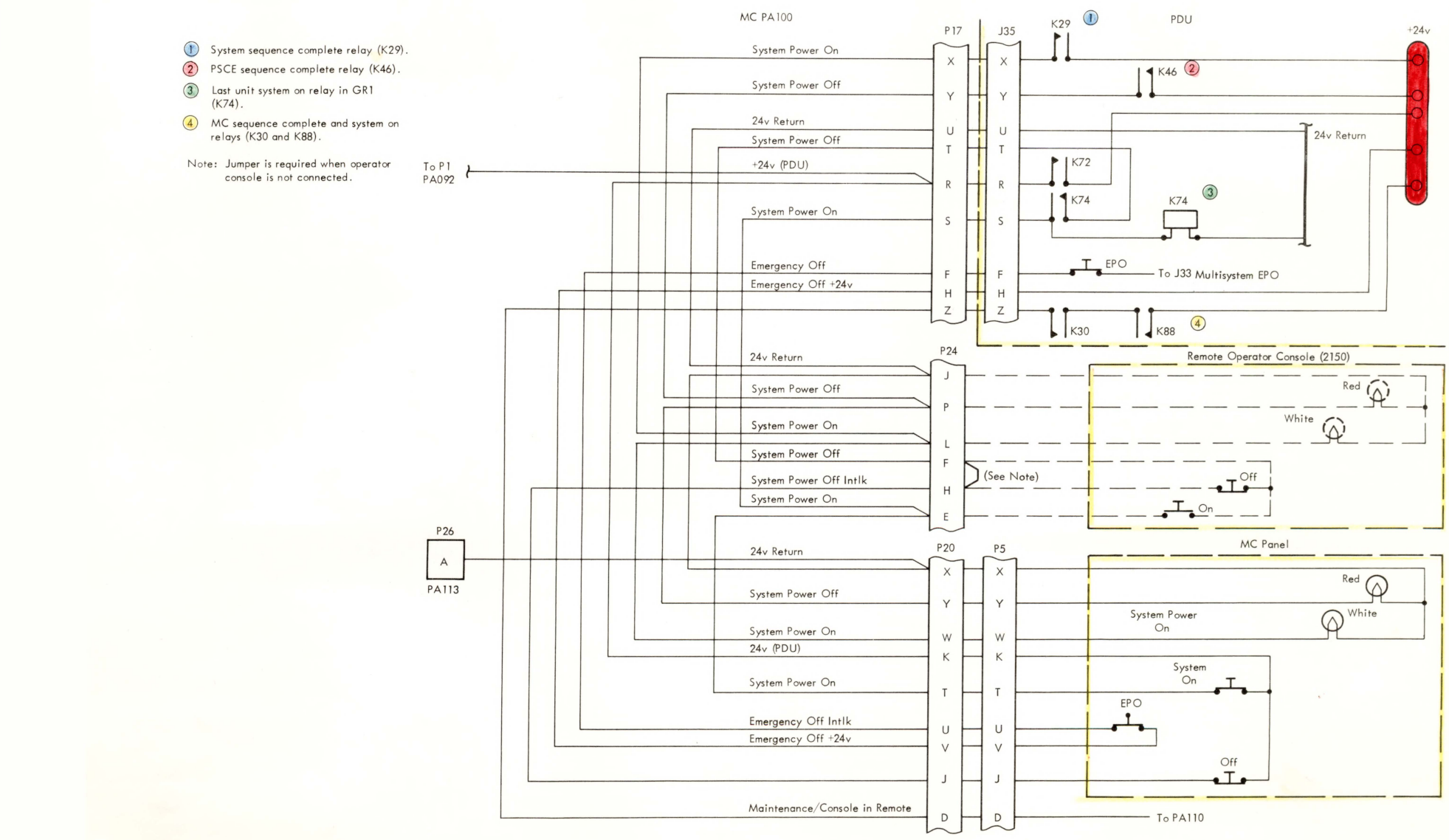
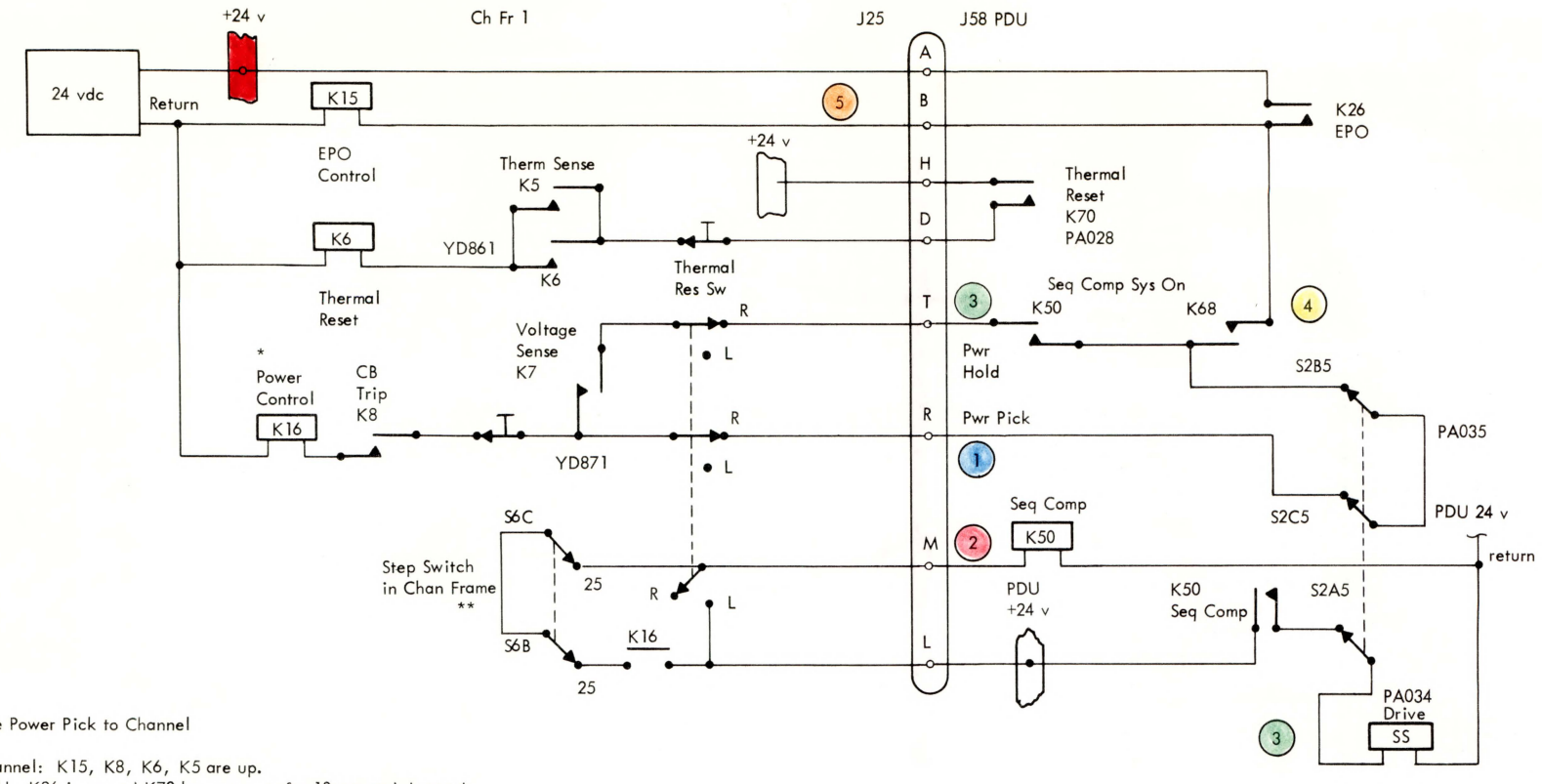


DIAGRAM 6-9. MC - PDU INTERFACE



Before Power Pick to Channel

In channel: K15, K8, K6, K5 are up.
In PDU: K26 is up and K70 has come up for 10 sec and dropped.

Power Up

(1) PDU stepping switch reaches unit and picks K16 starting channel power up. When channel sequence is complete K7 is up and the channel stepping switch has reached position 25.

(2) Channel stepping switch picks PDU sequence complete relay for channel.

(3) Sequence complete sends Power Hold to channel and steps PDU stepping switch to next position.

Power Down

(4) Channel frame system on relay (K68) is dropped by prior unit sequence complete relay down.

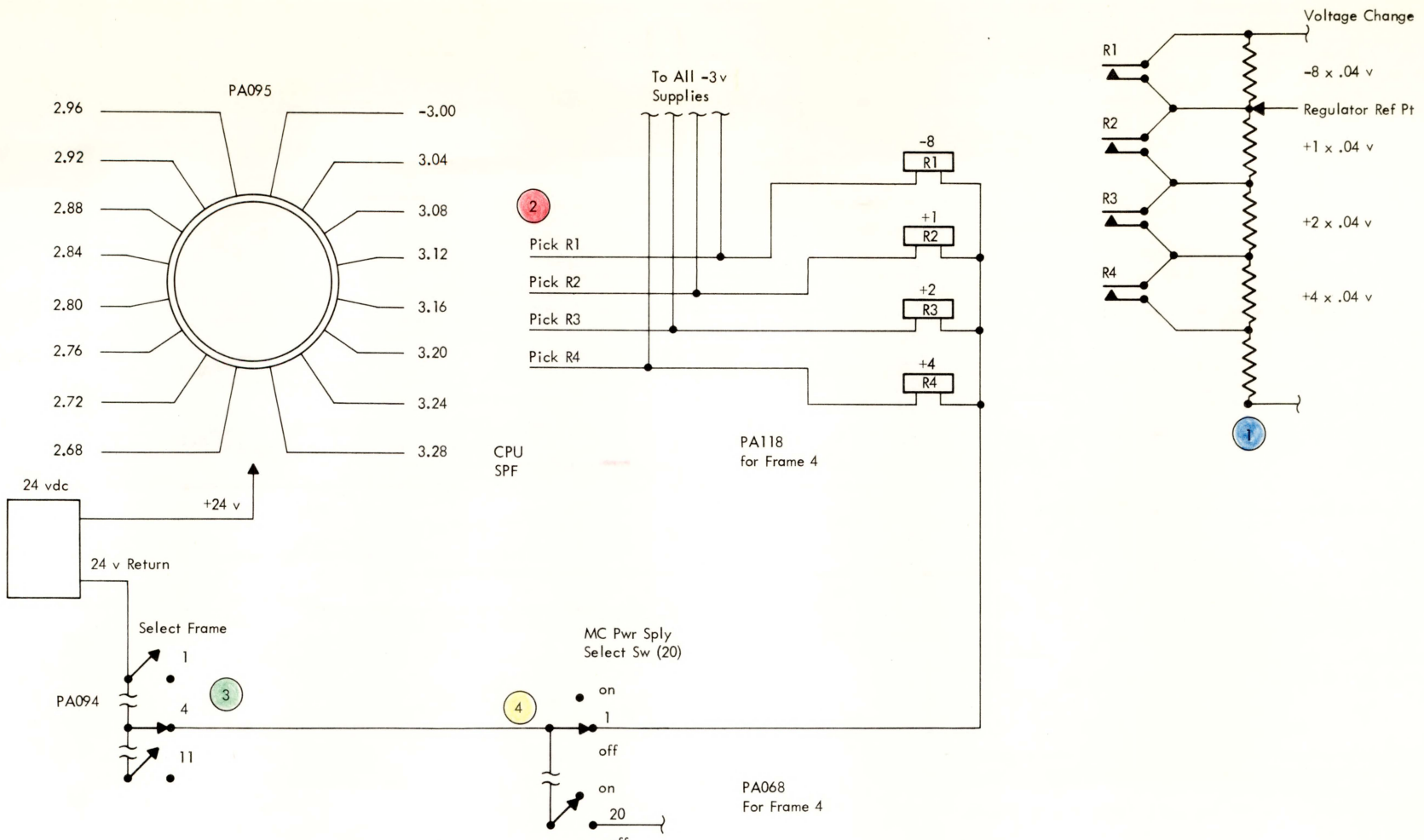
(3) K68 down drops K16 in channel and channel power goes down.

(2) K16 down drops sequence complete (50) in PDU. K50 down drops system on relay for next unit.

EPO Power Down

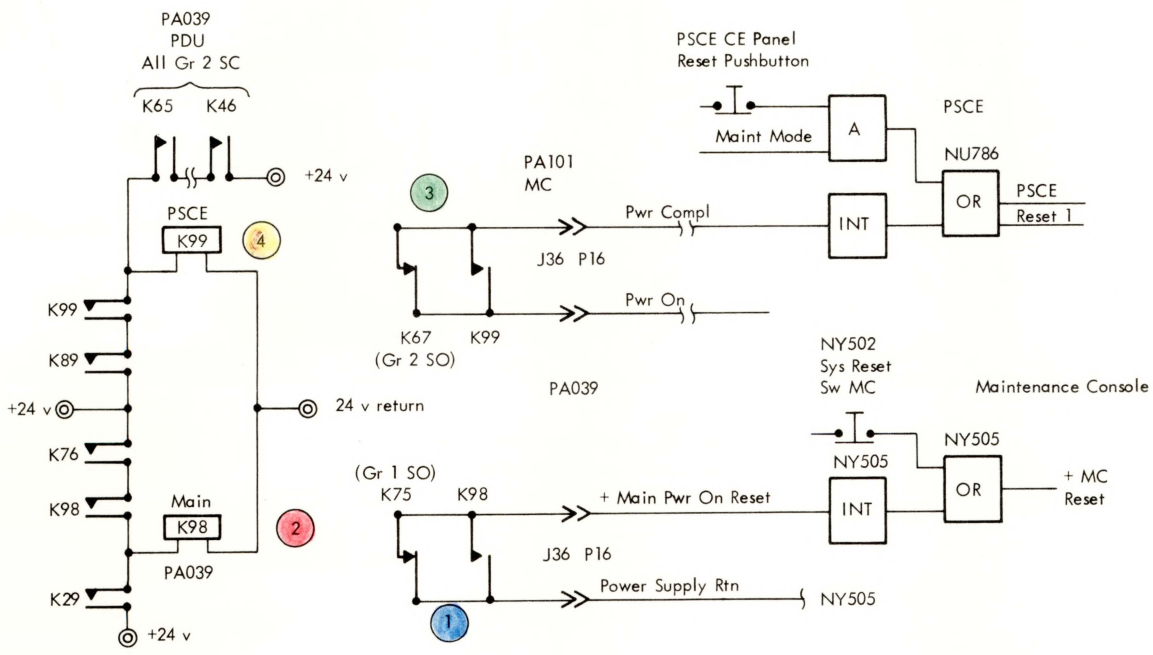
(5) Any EPO switch open causes PDU 24 vdc to go down and K26 drops. K26 down drops K15 in the channel frame. K15 down drops all channel power.

DIAGRAM 6-11. CHANNEL-PDU INTERFACE



1. Voltage is varied by shorting out selected resistors in the voltage regulator reference voltage circuit. Each relay when picked changes the output voltage by the value shown to the right of the resister it shorts out.
2. Each rotary switch delivers +24 v to the coils of the selected relays at all supplies controlled by the switch.
3. The frame is selected by a switch in the 24 v return line.
4. Further selection (supply within frame) may be done by switch on selected frame. Switch ON prevents margining from maintenance console.

DIAGRAM 6-13. MARGINAL CHECKING, INCREMENTAL



System Power-On Reset

1. Reset is delivered when this circuit is open.
2. The circuit is opened at the start of power on sequence when K75, a group 1 Sys-On relay, comes up. The circuit remains open, and the reset is held, until K29 comes up and picks K98. This occurs at the end of the power up sequence as a result of all SC relays, group 1 and group 2, being up.

PSCE Power-On Reset

3. Reset is delivered when this circuit is open.
4. The circuit is opened at the start of a system, or group 2 only, power on sequence when K67, a group 2 Sys-On relay, comes up. The circuit remains open, and the reset is held, until K99 is picked as a result of all group 2 SC relays being up at the end of the power on sequence.

DIAGRAM 6-15. POWER ON RESET

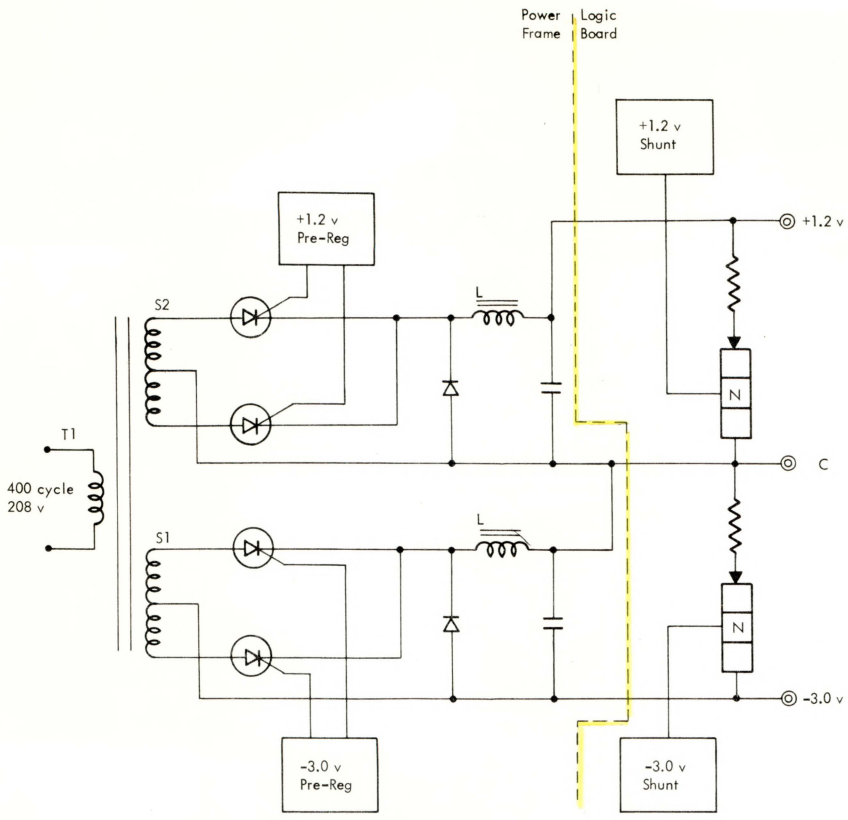


DIAGRAM 6-16. DUAL VOLTAGE SUPPLY, POWER FLOW AND REGULATION

In the Power Frames

Two SCR give full wave rectification of the output of each of the center-tapped secondaries.

Pre-regulation (slow response) is accomplished by controlling the SCR gates so that each conducts during only part of its possible half cycle of conduction.

When the SCR are not conducting current is fed to the load through the diodes connected between the SCR cathodes (supply positive) and the center tap of the transformer (supply negative). Power is supplied by the collapsing field of the filter choke and by energy stored in the capacitors.

On Each Logic Board

Fast response regulation is achieved by control of power transistors which shunt the load.

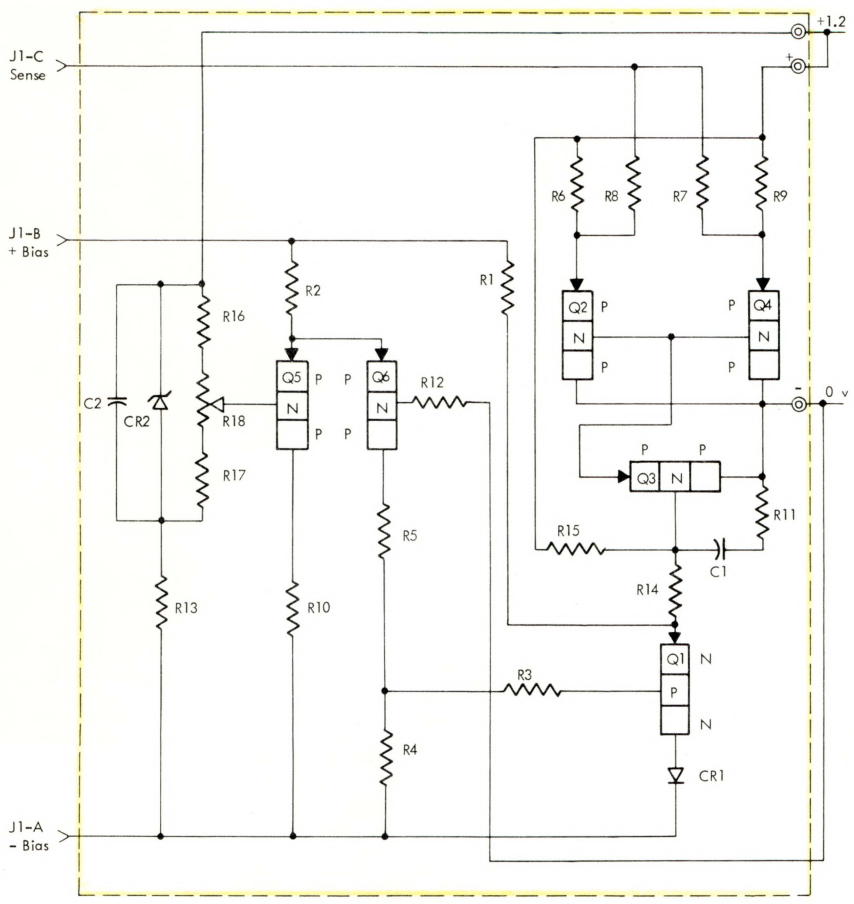


DIAGRAM 6-17. +1.2 V SHUNT REGULATOR

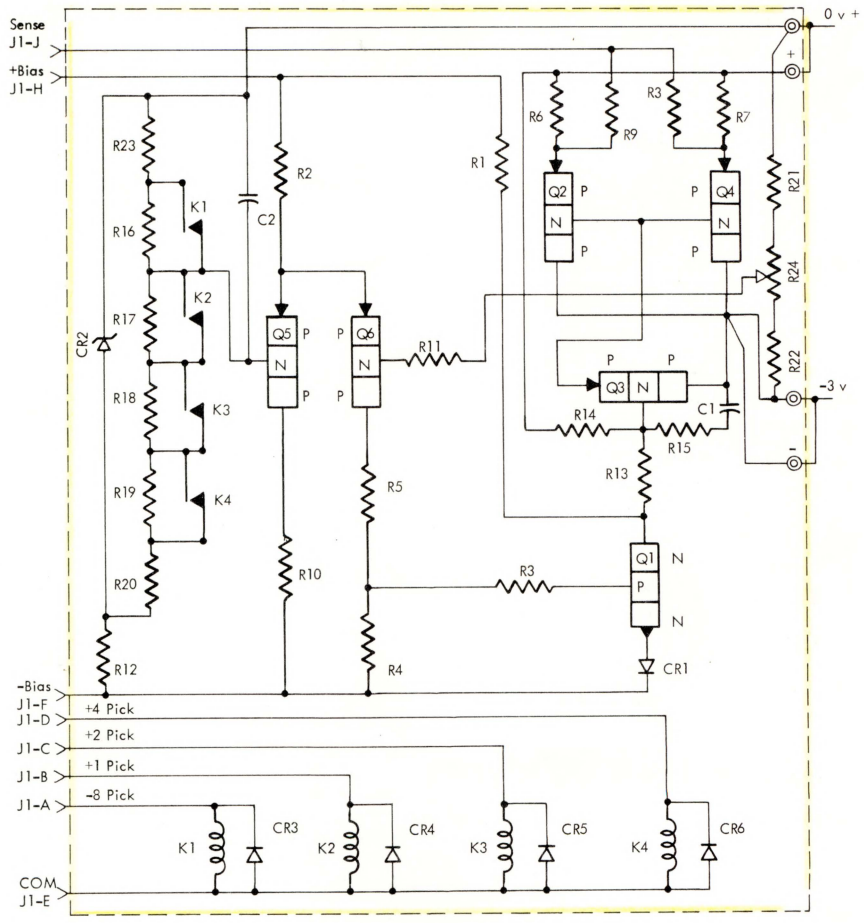
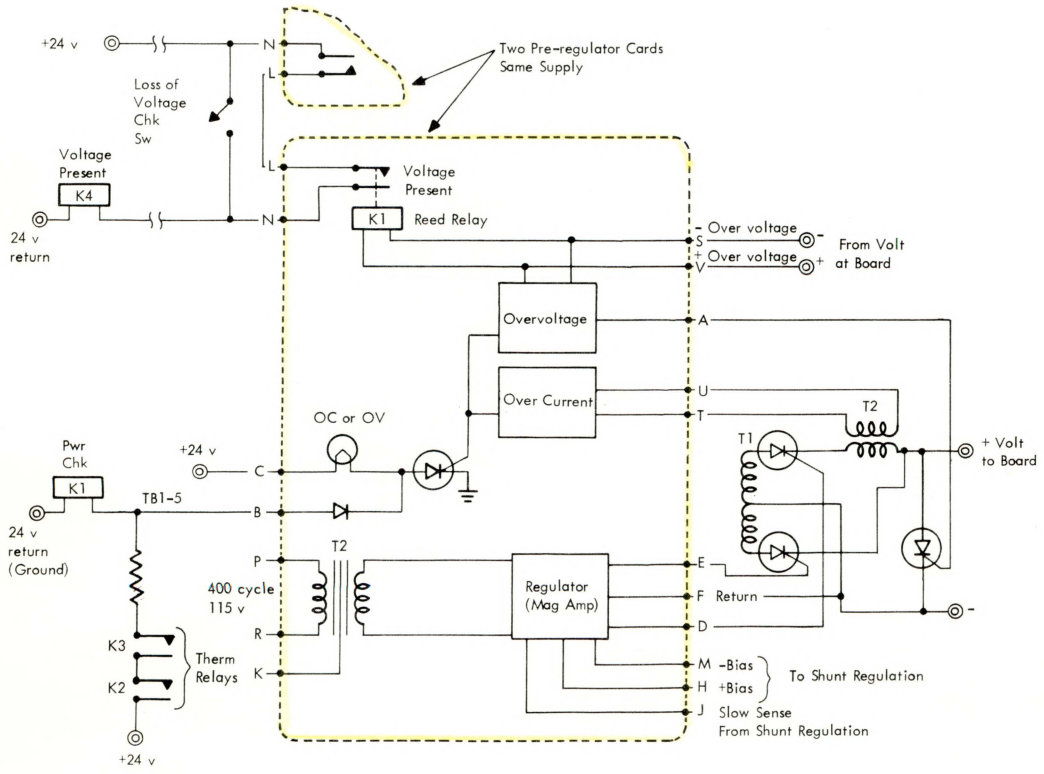


DIAGRAM 6-18. -3.0 V SHUNT REGULATOR



L-N	Closed circuit indicates that voltage controlled by card is present at board.
C	24 v to card lights indicator for overvoltage or overcurrent indication.
B	Ground, to drop power check relay, on overvoltage or overcurrent detection of voltage controlled by card.
P-R	Power input for regulator.
K	Ground on T2 core.
S-V	Voltage controlled by card fed back from board to card. Used to detect voltage present and over voltage conditions.
A	Signal from over voltage detector shorts out supply.
U-T	Signal proportional to current in main SCR. Used in over current detection.
E-D	Gates to main SCR. Timing controlled by regulator to give voltage regulation.
F	Return path for SCR gate signals.
M-H	Positive and negative bias voltages developed on card and delivered to shunt.
J	Signal proportional to current drawn by power transistor in shunt. Delivered to card to control preregulation.

DIAGRAM 6-19. CONTROL CARD, CONTACTS AND FUNCTIONS

6-16
6-17
6-18
6-19 (3/68)

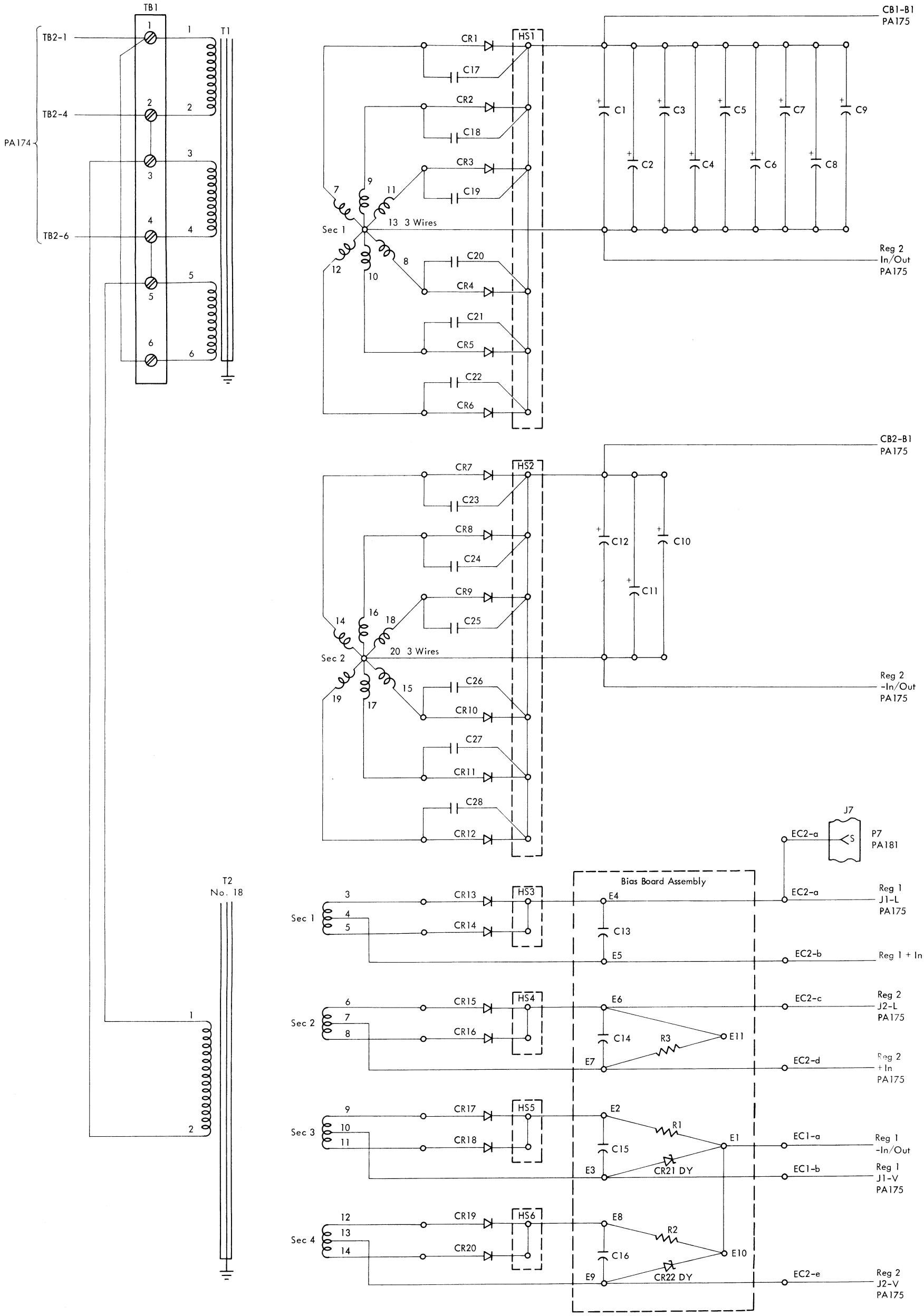
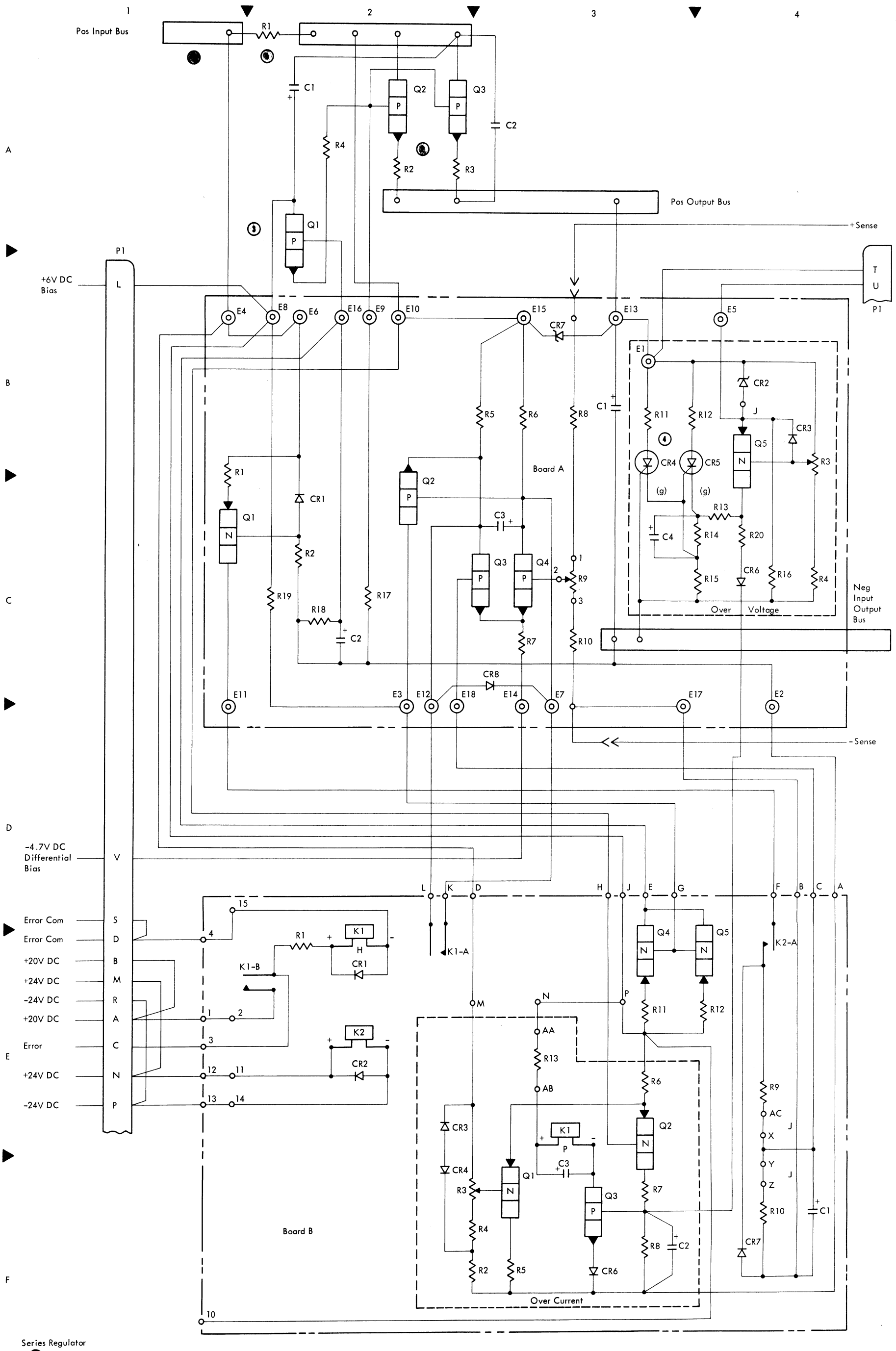


DIAGRAM 6-20. SPF BULK SUPPLY



Series Regulator

- Bulk supply dc voltage
- Series pass transistors
- Driver transistor
- O/V protective device CR4
- Series sampling resistor

DIAGRAM 6-21. SPF SERIES REGULATOR

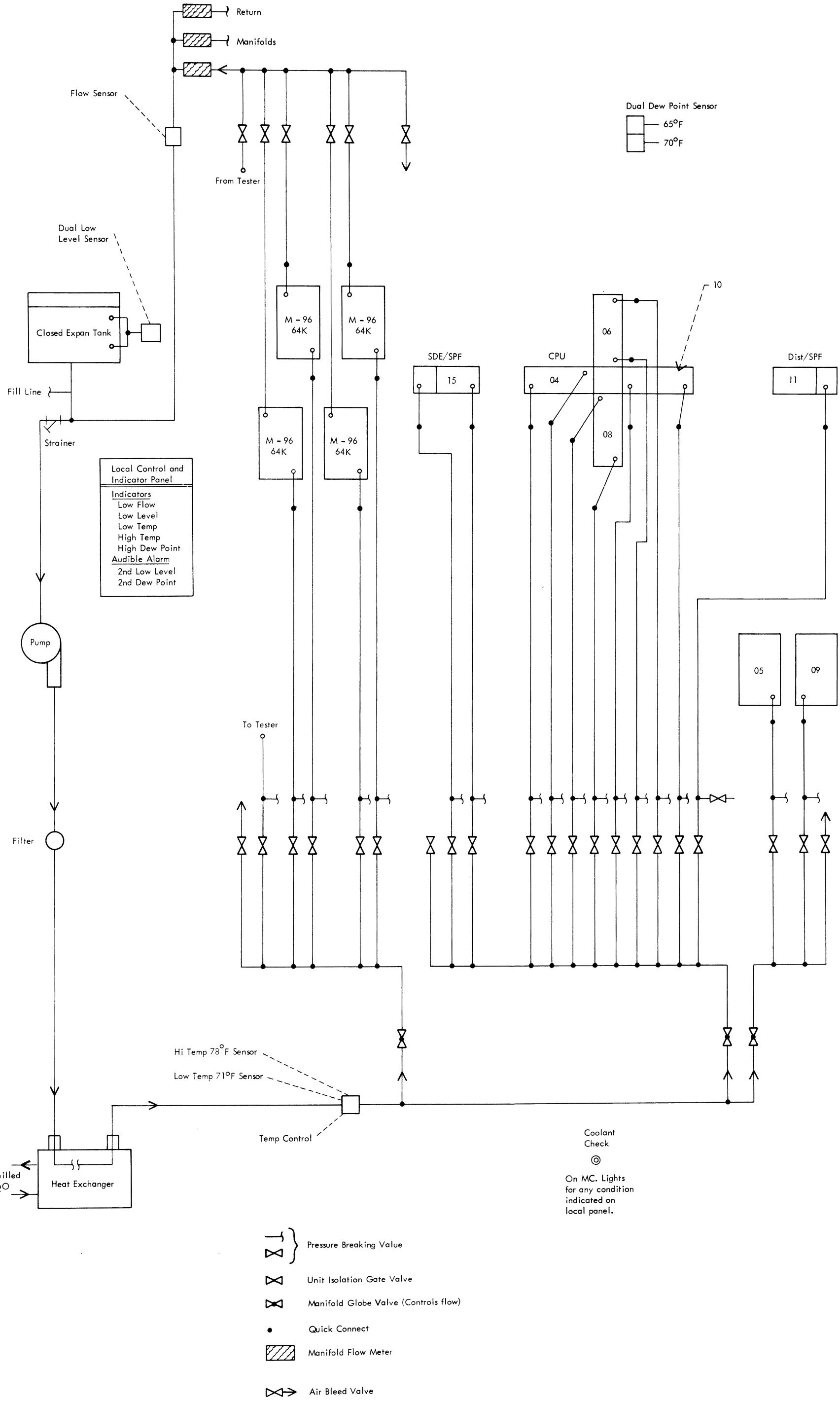


DIAGRAM 6-22. TYPICAL LIQUID COOLING SYSTEM (91JK)

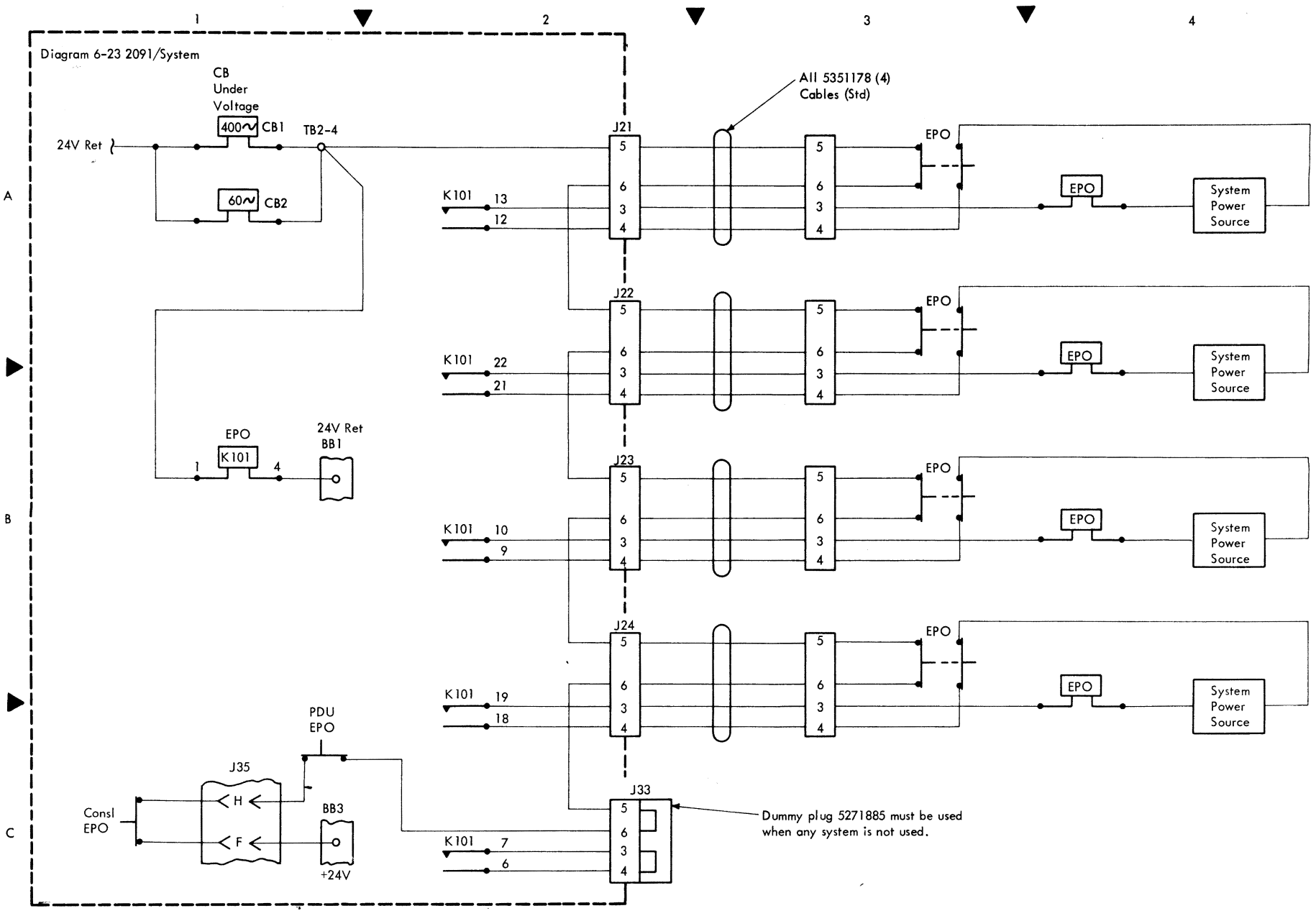
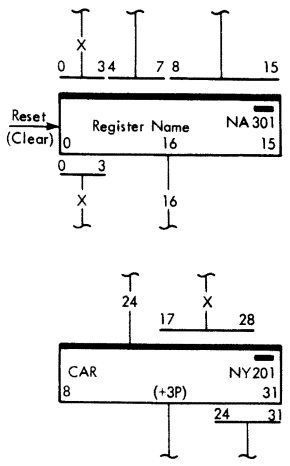


DIAGRAM 6-23. MULTI-SYSTEM EPO

RX	(Instruction Format) One Operand from a GPR, the Other from an Indexed Storage Location
S0	State Zero
SA	Sink Address
SAA	Storage Address Alteration
SAB	Storage Address Bus
SAP	Storage Address Protection
SAR	Storage Address Register (Same as MAR); Store Address Register
SB	Sink Address Bus
SBI	Storage Bus In
SBO	Storage Bus Out
SC	Single-Cycle; Storage Channel; Sequence Complete
Sc	Source
SDB	Storage Data Buffer
SDE	Storage Distribution Element
SDR	Storage Data Register (Same as MAR)
Sel	Select
SERR	CPE Status Recording Program
SEVA	Systems Evaluation Program
S/F	Store/Fetch
Sh	Shift
Shftr	Shifter
SI	(Instruction Format) One Operand from Storage, the Other Is Immediate
SIAT	Store Into Array Trigger
SIIS	Store into Instruction Stream
SIO	(Mnemonic) Start I/O (SI)
SIT	Store Interlock Trigger
SK	Storage Key
Sk	Sink
S/L	Short/Long Precision
SLA	(Mnemonic) Shift Left Single (RS)
SLCB	Save Loop Close B Register
SLC	Save Loop Close
SLCIR	Save Loop Close Instruction Register
SLDA	(Mnemonic) Shift Left Double (RS)
SLCX	Save Loop Close - X Register
SLI	Suppress-Length-Indication
SLT	Save Loop Target; Solid Logic Technology
SM	Storage Module
SMAL	Suppress Multi-Access Link
Sng	Single
SO	Storage Operand
SP	Storage Protect; Single Pulse
SPAD	Select Parity and Display Counter
SPAR	Storage Protect Address Register
SPC	Storage Protect Check
SPF	Storage Protect Feature
SPM	(Mnemonic) Set Program Mask (RR); Storage Protect Memory
SP91	Protect Storage for System/360 Model 91
Sr	Source
SRA	(Mnemonic) Shift Right Single (RS)
SRDA	(Mnemonic) Shift Right Double (RS)
SS	Snapshot Register; Storage-to-Storage; Stepping Switch
S/S	Source/Sink
SSC	Selector Subchannel
SSK	(Mnemonic) Set Storage Key (RR)
SSM	(Mnemonic) Set System Mask (SI)
ST	(Mnemonic) Store (RX)
Stat	Station
STC	(Mnemonic) Store Character (RX)
Stg	Stage; Storage
Stk	Stack
Sto	Store; Storage
STOOP	Storage Operation
Stor	Store; Storage
Stp	Stop
STR	Source Tag Register
Sup	Suppress
SVC	(Mnemonic) Supervisor Call (RR)
SVIR	Save Instruction Register
SVR1	Save R1 Register
Sw	Switch; Switch Enabled
SW	Single Word
Syl	Syllable
Sync	Synchronize
Sys	System
T	Time
TAT	Time Address Trigger
Tbl Wd	Table Word
TCH	(Mnemonic) Test Channel (SI)
T/CT	True/Complement Trigger
TD	Time Delay
Temp	Temporary
TERMT	Terminate Trigger
TFMT	Temporary Fetch Made Trigger
Tgr	Trigger
TI	Terminate Immediate
TIO	(Mnemonic) Test I/O (SI)
TM	(Mnemonic) Test under Mask (SI)
Tof	Turn Off
Ton	Turn on
Tot	Total
TR	(Mnemonic) Translate (SS)
Trans	Transpose
Trnsps	Transpose
TRT	(Mnemonic) Translate and Test (SS)
TS	(Mnemonic) Test and Set (SI); Timing Stack
T&S	Test and Set
U1	Unit 1
U2	Unit 2
UB	Upper Bound
UABI	Unit Address Bus In
UABO	Unit Address Bus Out
UBCTR	Upper Bound Counter
UCC	Unit Communications Control
Ucndl	Unconditional
Uncond	Uncondition
UNPK	(Mnemonic) Unpack (SS)
Val	Valid
Var	Variable
VFL	Variable Field Length
VFLEU	Variable Field Length Execution Unit
Viol	Violate; Violation
WAM	With Available Memory
WC	Word Counter
Wd	Word
Wd Bdy	Word Boundary
WR	Working Register
WRD	(Mnemonic) Write Direct (SI)
XC	(Mnemonic) Exclusive OR (SS)
Xec	Execute
XOR	Exclusive OR
ZAP	(Mnemonic) Zero and Add (SS)
ZET	Zero Test Unit
1A2	SAR 1 Loaded after SAR 2
1B2	RS 1 Loaded before RS 2
1B3	RS 1 Loaded before RS 3
1B4	RS 1 Loaded before RS 4
1C2	SAR 1 Address Compares with SAR 2 Address
2A3	SAR 2 Loaded after SAR 3
2B3	RS 2 Loaded before RS 3
2B4	RS 2 Loaded before RS 4
2C3	SAR 2 Address Compares with SAR 3 Address
3A1	SAR 3 Loaded after SAR 1
3B4	RS 3 Loaded before RS 4
3C1	SAR 3 Address Compares with SAR 1 Address

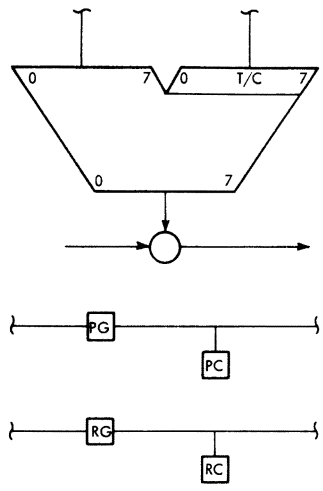
LEGEND

1. Data Flow Diagrams



Register, Counter

Heavy line indicates input side of a functional unit that can store information. A partial transfer of contents is shown by numbered input/output lines. An input or output line connected directly to the register denotes a complete transfer of contents. An X placed in an input or an output line means that a gating condition is required to activate the transfer path. A number in a transfer path denotes the number of lines. A bar in the upper right corner means that the status of register positions is shown in indicator lights. An ALD page reference is given under the indicator bar. The bottom line within a register gives either the register position numbers or a single number indicating register size. Where register position numbers are given, a symbol such as (+3P) indicates that the register also contains 3 parity bits.



Adder, Incrementer

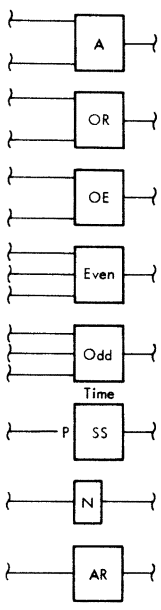
Notches across top divide logical inputs. T/C indicates that the associated input can be entered in either true or complement form.

Functional or Switching OR

Parity Generate, Parity Check

Residue Generate, Residue Check

2. Positive Logic Diagrams



AND
The output is active only when all inputs are active.

OR
The output is active if one or more inputs is active.

Exclusive OR
The output is active only when one input is a active and the other is not.

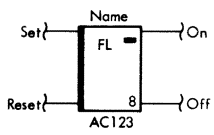
Even
The output is active only when an even number of inputs is active.

Odd
The output is active only when an odd number of inputs is active.

Singleshot, Time Delay, Oscillator

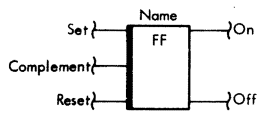
Inverter, or Negator
The output is active only when the input is not active.

Amplifier, Signal Mode Converter



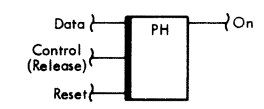
Flip Latch

Input side is denoted by thick line. Bar means that an indicator is connected to this latch. The number in the lower right corner means that this symbol represents 8 actual flip latches in the machine. An ALD page reference may be given below the block. A set input activates the on output and deactivates the off output; a reset input activates the off output and deactivates the on output. The device holds its outputs between active inputs. Simultaneous set and reset inputs activate both on and off outputs until one input is deactivated.



Flip-Flop

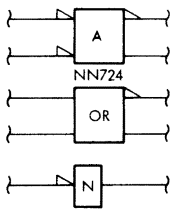
Same as flip latch except that an active complement input causes the device to switch to the opposite state. Also, on and off outputs can never be active simultaneously: Simultaneous set and reset inputs are equivalent to a complement input.



Polarity Hold

The PH output follows the data input when the control (release) input is activated. Between control inputs, the PH holds the previously sampled state of the data line. The reset input (when used) deactivates the output.

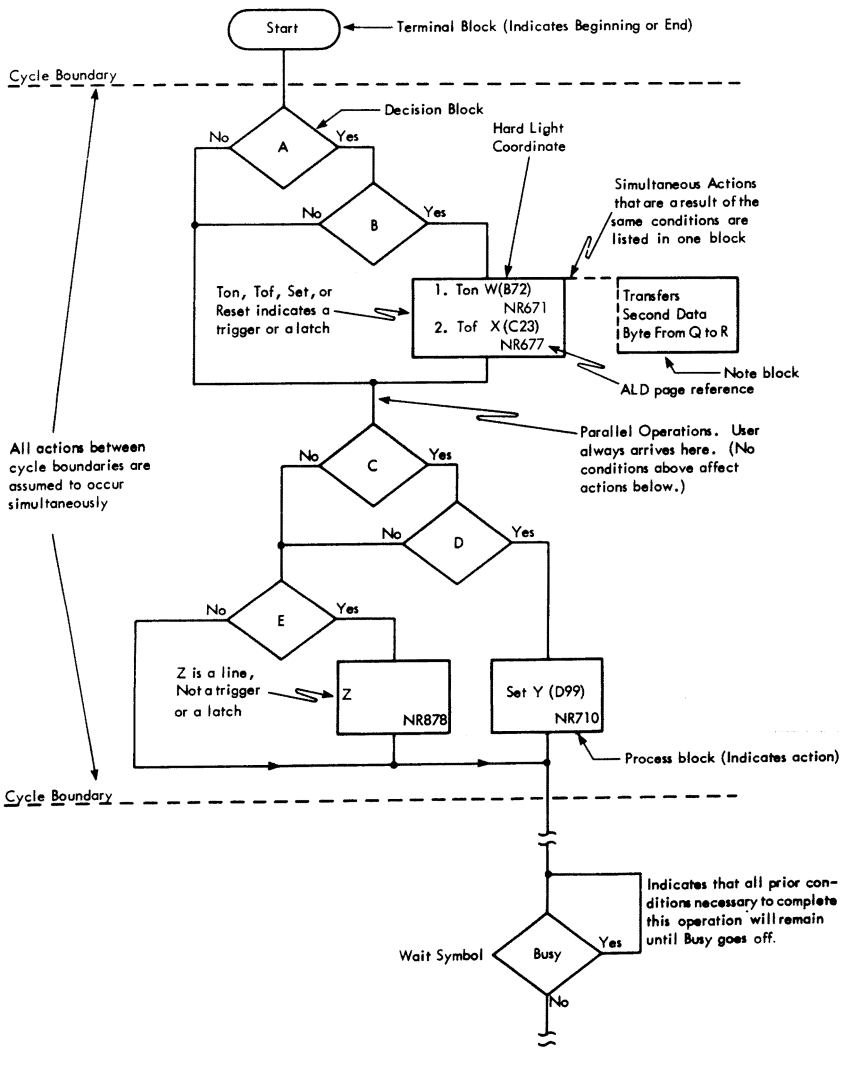
3. Simplified Logic Diagrams



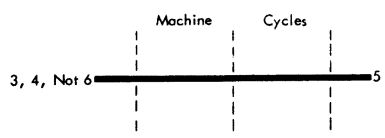
Input wedges mean that the more negative line level is required to activate the circuit; output wedges mean that the more negative line level is present when the circuit is activated. Lack of wedges indicate the more positive level. Blocks may have more than one output line. All line titles are preceded by + or - to indicate line level.

Note: Additional SLD symbology used only on ECAD's is shown in Volume 1.

4. Flowcharts

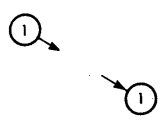


5. Timing Charts



Heavy bar indicates active state. Numbers at beginning and end of the bar identify the signal(s) (also on the same chart) that activate and deactivate this line. "Not" preceding a number means that the deactive signal conditions this line.

6. General



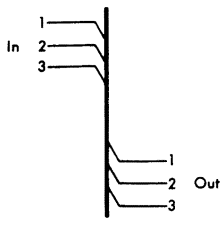
On-Page Connector

Indicates connection between two points on the same diagram. Arrow leaving symbol points to symbol with the same number.

Off-Page Connector

Indicates connection between two points located on separate pages. Where the connection is between two pages of a multipage diagram, a reference such as "Sheet 2" is given instead of a diagram number.

Text Reference Point (Reference from FETOM)



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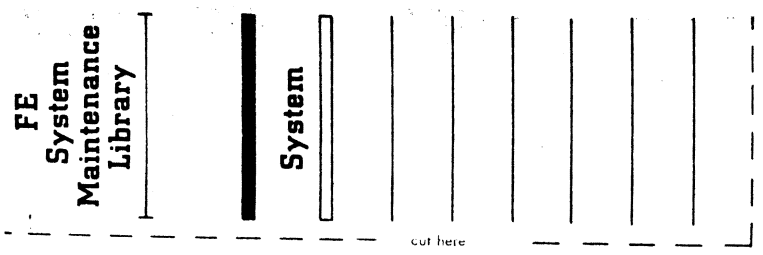

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