IBM **Field Engineering Handbook**

IBM Confidential

System/360 Model 40

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IBM® Field Engineering Handbook

System/360 Model 40

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Third Edition
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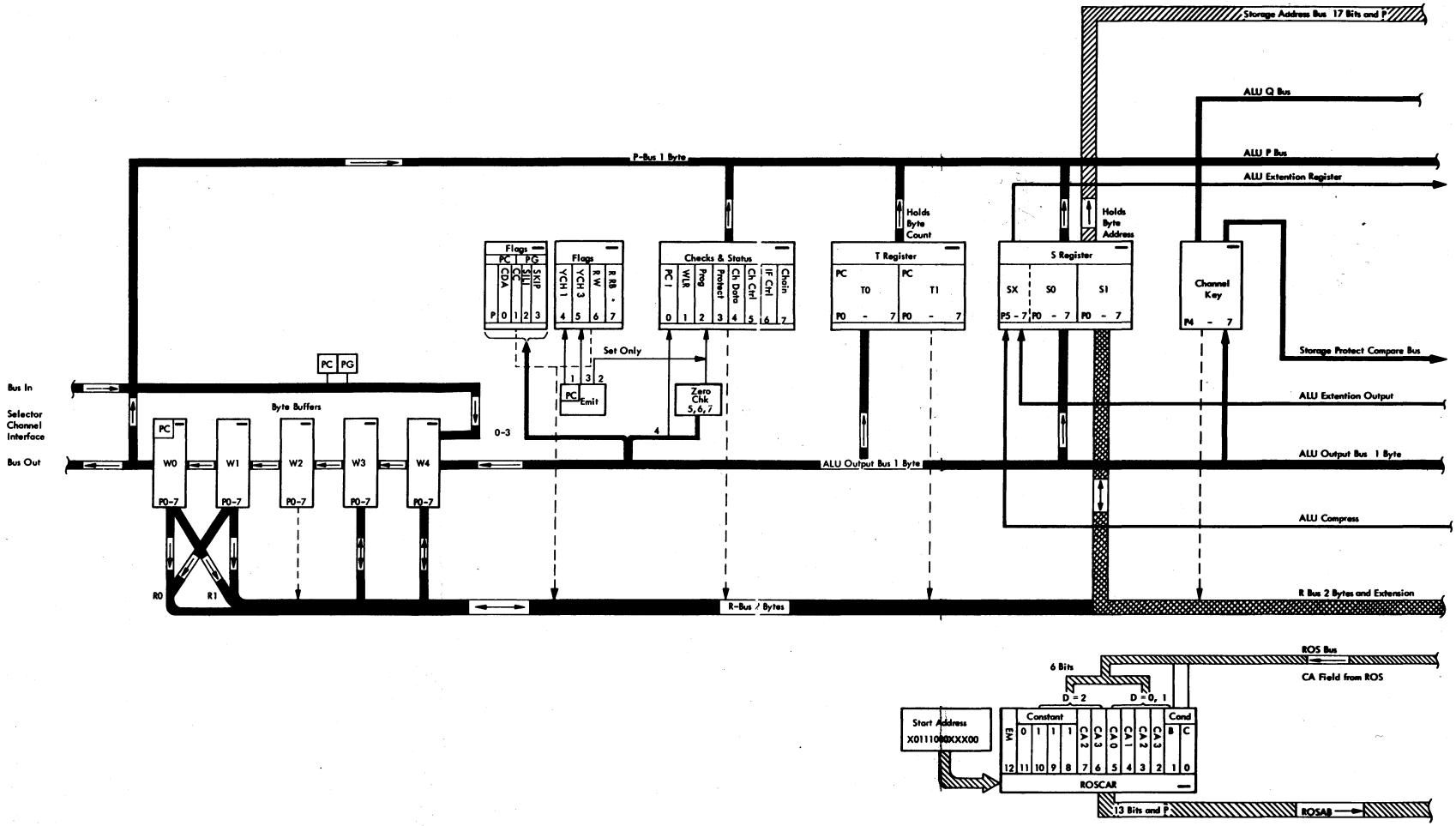
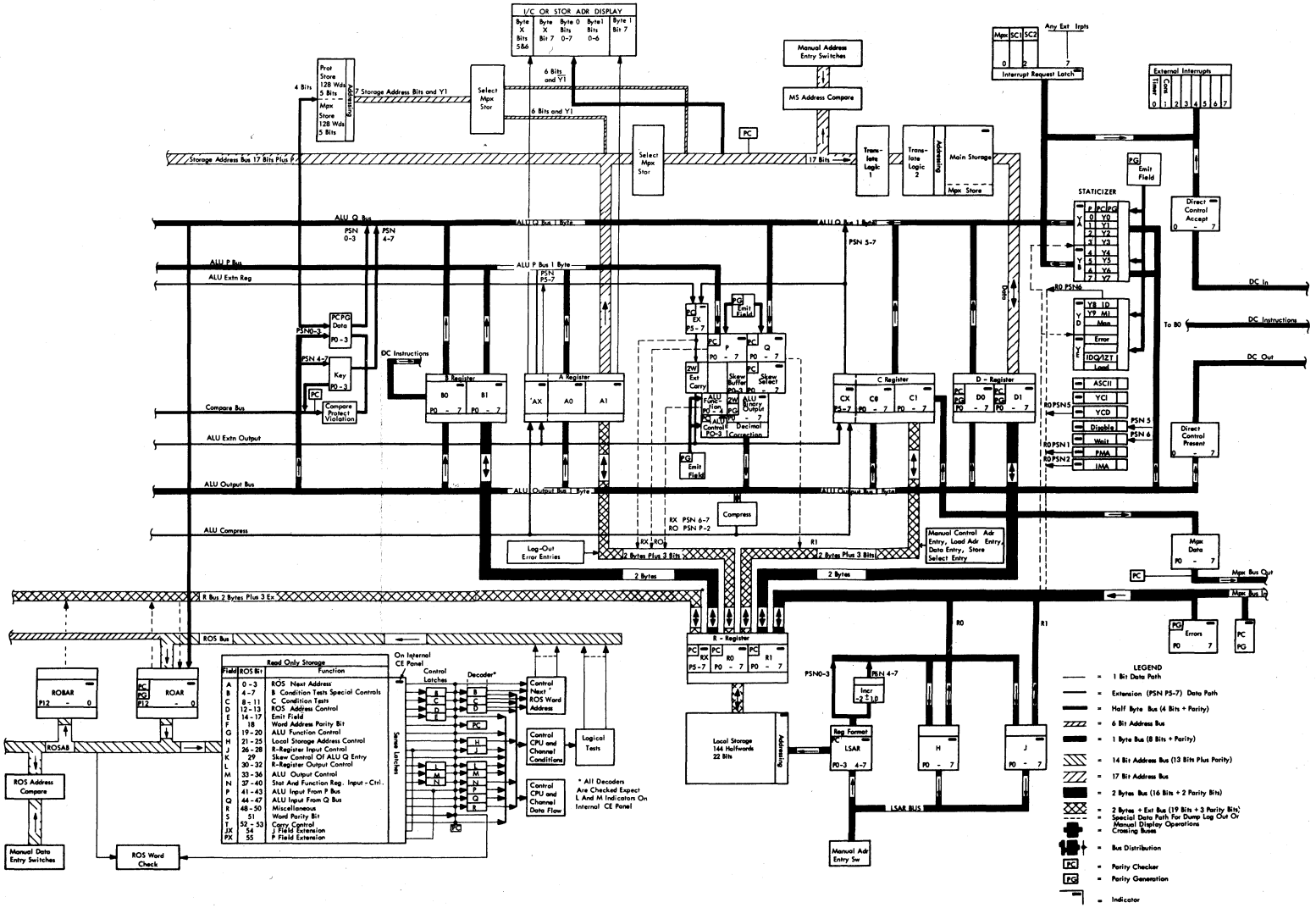



I/C OR STOR ADR DISPLAY
Manual Address Entry Switches
MS Address Compare
Any Ext Irpts
Interrupt Request Latch
External Interrupts
Storage Address Bus 17 Bits Plus P
Select Mpx Stor
Trans-late Logic 1
Trans-late Logic 2
Addressing
Main Storage
Mpx Store
STATICIZER
Direct Control Accept
Direct Control Present
ALU Q Bus
ALU P Bus
ALU Extn Reg
Compare Bus
ALU Extn Output
ALU Output Bus
ALU Compress
Key
Compare Protect Violation
I Register
A Register
C Register
D Register
Skew Buffer
Skew Select
Binary Output
Decimal Correction
Log-Out Error Entries
Compress
Manual Control Adr Entry, Load Adr Entry, Data Entry, Store Select Entry
R - Register
Local Storage 144 Halfwords 22 Bits
Reg Format
LSAR
LSAR BUS
Manual Adr Entry Sw
ROS Bus
ROBAR
ROAR
ROSAB
ROS Address Compare
Manual Data Entry Switches
ROS Word Check
Read Only Storage
Control Latches
Decoder*
Sense Latches
Control Next ROS Word Address
Control CPU and Channel Conditions
Control CPU and Channel Data Flow
Logical Tests
* All Decoders Are Checked Expect L And M Indicators On Internal CE Panel
LEGEND
1 Bit Data Path
Extension (PSN P5-7) Data Path
Half Byte Bus (4 Bits + Parity)
6 Bit Address Bus
1 Byte Bus (8 Bits + Parity)
14 Bit Address Bus (13 Bits Plus Parity)
17 Bit Address Bus
2 Bytes Bus (16 Bits + 2 Parity Bits)
Bus Distribution
Parity Checker
Parity Generation
Indicator

A GATE WIRING SIDE

	D	C	B	A
1	Local Stor Stor Prot Not +6 Marginal	LSAR Log Out Stor Prot	Main Stor Controls Clock Checking	Mpx Channel
2	Data Flow 1	Data Flow 0	ROS 2	ROS 1
3	Console Entries	ALU	Interval Timer ALU	ROS Address Comp Stats

Hinge

B GATE WIRING SIDE

	D	C	B	A
1	1052 (Y1)	1052 (X1)	Sel Chan 2	
2	Sel Chan Common	Sel Chan 1	Sel Chan 2	
3	Sel Chan 1	Sel Chan 1	Sel Chan 2	Direct Control

Hinge

ALD LOCATIONS

ALU Circuits

Carry	AM201 - AM251
Connect	AM001 - AM071
Decimal Correct	AV202 - AC212
Decimal Fill	AV001 - AV201
Parity Generation	AM431
Right Shift	AM101 - AM151
Sum	AM001 - AM071

Console Lamps and Switches

Console Check Lamps	PA161 - PA162
Console Display Lamps	PA101 - PA152
Internal CE Panel	PA201 - PA206
Meter	PA091
Push Switches	PA021 - PA051
Rotary Switches	PA041 - PA071
Roller Switches	PA031
Toggle Switches	PA001 - PA021, PA081
Wiring Diagrams	PA540 - PA906

Control Circuits

Clock	KC001 - KC081
Dump - Undump	KM121
LS R/W	KM001
MS Address Compare	KH101
MS R/W	KM101
Program Interrupt	KM131
ROS Address Compare	KH111

Error Check Latches

Control Check	KH401
Early Check	KH401
Late Check	KH401
Master Check	KH401
Halt	KH142
Halt State	KH161
System Reset	KH141
Trap	KM001

Local Storage LT011

Registers

A	RA001 - RA171
B	RB031 - RB171
C	RC001 - RC171
D	RD021 - RD171
Ex	RE001
Function	KP001
H	RH031 - RH071
J	RJ031 - RJ071

Register (Continued)

LSAR	RL001 - RL471
P	RP001 - RP071
Q	RQ001 - RQ071
R	RR001 - RR071
ROAR	RX001 - RX111
ROBAR	RX201 - RX311
SKEW	AQ011 - AQ041
SP DATA	KU001
SP KEY	KU011
TIMER	KT011

tOS Control Fields

A	RX051 - RX091
B	DR071 - DR072
C	DR111
D	DR131
E	DR171
G	KP021
H	DS021 - DS081
J	DR275 - DR282
K	AQ001
L	DR321 - DR323
M	DR361 - DR363
N	DR401
P	DR431
Q	DR471
R	DR501
T	AM311

ROS Conditional Branches

CPU B Condition	DR751
CPU C Condition	DR752
I-O B Condition	FL001
I-O C Condition	FL011

Staticisers

ASC II	RX112
Enable	RH171
IDQ	AM441
IMA	KU051
IZT	AM441
PMA	KU051
Wait	KH171
YA	RY011 - RY041
YB	RY041 - RY071
YCD	AM321
YCI	AM321
YD	RY111
YE	RY121

Selector Channel

1401-1410 Compatibility Circuits	GB507

Storage Circuits

Timing	MA011 - MA041
Dec to Bin Translator	MB001 - MB004
Parity Check	MB005
Address Powering	MB011 - MB041
X/Y Decoders	MB051 - MB081
X/Y Terminator Gate	MB091
X Gates and Drivers	MB101 - MB251
Y Gates and Drivers	MB261 - MB411
Strobe Drivers MC011	MC011
Data Bit Powering	MC021
Sense Amplifiers	MC031 - MC084
Z driver	MC091 - MC171
Reference	MC181 - MH020
Timing Charts	MJ000 - MJ010
M7 Storage Controls	MX010
Address to Storage	MX020
Data to Storage	MX030
Data From Storage	MX040

Storage Protect	L4111

1052

Printer	PF040
Keyboard	PF050
Switches and Lamps	PF070
Timing	PF110
Circuits	PG011 - PG801

1401-1410 Compatibility

R/W Load Mode Buffer Controls SC1	GB507 - GB509
1401 Compatibility - ROSCAR and ROSAB Bit 12	GD500
SC1 Data Out Translator	GW510
SC1 Data Out Parity Correction	GW511
SC1 Buffer W0 Output to IF	GW512
SC1 Data In Translator	GW513
SC1 Data In Detect Invalid 1410 Characters	GW514
SC1 Bus In Switching 1401-1410 Translators	GW515
SC2 1410 R/W Load Mode Buffer Controls	HB507 - HB508
SC2 1410 Mode Controls	HB509
SC2 Data Out Translator	HW510
SC2 Data Out Parity Correction	HW511
SC2 Data In Translator	HW513
SC2 Data In Detect Invalid Character	HW514
1401 Compatibility Controls ROBAR Bit 12 Address Translator Control	RX003

MPX CHANNEL ALD INDEX

Channel Control Latches

Channel Error (checks) Latches

Channel Interface Lines

1401-1410 Compatibility Circuits	GB507
1401-1410 Compatibility - Data Out Translator	GW510
B Gate Clock Circuits	GX501
B Gate Terminators	GS506
Channel IMA	GA508
M Field Controls	GE532
Memory Address Bus	GA501
Memory Address Bus Parity Checker	GA505
Reinterpret Latches and Controls	GE501
ROSAB	GD501
SC1 A and D Field Controls	GE591
SC1 Address in Latch	GG531
SC1 Address Out	GG513
SC1 B and C Conditions	GE571
SC1 Buffer Data Check	GG543
SC1 Bus In Terminators	GG501
SC1 Bus In to W4 Latch	GG522
SC1 Bus Out Interface Drivers	GG503
SC1 Chaining Boundary and Program check	GF505
SC1 Chaining Check	GG523
SC1 Channel Control Check	GG543
SC1 Channel End	GG521
SC1 Channel Priorities	GB506
SC1 Channel Resets	GE581
SC1 Channel Select	GE581
SC1 Check Latches	GG543
SC1 Command Latches - Read, Write and Read Backward	GF502
SC1 Command Out	GG523
SC1 Count and W Buffer Agree	GB503
SC1 Data Operation Latch	GG523
SC1 Data Service Request	GB505
SC1 Flags --CDA-CMD CHNG-SKIP-SILI	GF501
SC1 Flags YCH3 and YCH1	GF502
SC1 Halt Latch	GG513
SC1 In Tag Latch	GG531
SC1 Inhibit Bus In	GG522
SC1 Inhibit Select Out	GG513
SC1 Interface Control Check	GG543
SC1 Interface Control Line Drivers	GG504
SC1 Interface Free	GG512
SC1 Interface Line Control Terminators	GG502
SC1 Interrupt Request	GF503
SC1 J Field Controls	GE511
SC1 L Field Controls	GE521
SC1 M Field Decoder for Reinterpret	GE541
SC1 Operational In	GG513

SC1 Operational Out	GG513
SC1 P Register Entry Bus	GP501
SC1 R Register Entry Bus	GR501
SC1 ROSCAR	GC501
SC1 ROSCAR Address Forcing	GB505
SC1 S Register (Channel Memory Address Reg)	GS501
SC1 Select Latches	GF506
SC1 Select Out and Hold Out	GG511
SC1 P Field Decoder	GE561
SC1 Service In	GG522
SC1 Service Out	GG524
SC1 Start Latch	GG531
SC1 Status In Latch	GG531
SC1 Status Type Decoding	GG532
SC1 Suppress Out	GG512
SC1 T Equals 0	GG521
SC1 T Equals W Compare	GB504
SC1 T Register (Count)	GT501
SC1 Tag Check	GG543
SC1 Tag Register	GU501
SC1 W Buffer Flag Latches	GF504
SC1 W Buffer Registers	GW501
SC1 W Buffer Registers Full and Empty	GB501
SC1 W Equals 0	GG521
SC1 WLR Latch	GG521
SC2 A and D Field Controls	HE591
SC2 Address In Latch	HG531
SC2 Address Out	HG513
SC2 B and C Conditions	HE571
SC2 Buffer Data Check	HG543
SC2 Bus In Terminators	HG501
SC2 Bus In to W4	HG522
SC2 Bus Out Interface Drivers	HG503
SC2 Chaining Boundary and Program Check	HG505
SC2 Chaining Check	HG523
SC2 Channel Control Check	HG543
SC2 Channel End	HG521
SC2 Channel Priorities	HG506
SC2 Channel Resets	HE581
SC2 Channel Select	HE581
SC2 Check Latches	HG543
SC2 Command Latches - Read, Write and Read Backward	HF502
SC2 Command Out	HG523
SC2 Count and W Buffer Agree	HB503
SC2 Data Operation Latch	HG523
SC2 Data Service Request	HB505
SC2 Flags - CDA-CMD CHNG-SKIP-SILI	HF501
SC2 Flags YCH3 and YCH1	HF502

SC2 Halt Latch	HG513
SC2 In Tag Latch	HG531
SC2 Inhibit Bus In	HG522
SC2 Inhibit Select Out	HG513
SC2 Interface Control Check	HG543
SC2 Interface Control Line Drivers	HG50(
SC2 Interface Free	HG512
SC2 Interface Line Control Terminators	HG502
SC2 Interrupt Request	HG503
SC2 J Field Controls	HE511
SC2 L Field Controls	HE521
SC2 M Field Decoder for Reinterpret	HE541
SC2 Operational In	HG513
SC2 Operational Out	HG513
SC2 P Field Decoder 8-15	HE561
SC2 P Register Entry Bus	HP501
SC2 R Register Entry Bus	HR501
SC2 ROSCAR	HC501
SC2 ROSCAR Address Forcing	HB505
SC2 S Register (Channel Memory Address Reg)	HS501
SC2 Select Latches	HF506
SC2 Select Out and Hold Out	HG511
SC2 Service In	HG522
SC2 Service Out	HG524
SC2 Start Latch	HG531
SC2 Status In Latch	HG531
SC2 Status Type Decoding	HG532
SC2 Suppress Out	HG512
SC2 T Equals 0	HG521
SC2 T Equals W Compare	HB504
SC2 T Register (Count)	HT501
SC2 Tag Check	HG543
SC2 Tag Register	HU501
SC2 W Buffer Flag Latches	HF504
SC2 W Buffer Registers	HW501
SC2 W Buffer Registers Full and Empty	HB501
SC2 W Equals 0	HG521
SC2 Latch WLR	HG521

ROS GENERATED ADDRESSES
(shown in hex)

005 System Reset, Load Button
402 Manual Display Button
403 Manual Store Button
400 Start Button

*002 Diagnostic Select Switch - Main Storage Validate
006 Diagnostic Select Switch - Dump/Undump
**005 Diagnostic Select Switch - CPU Check
009 Diagnostic Select Switch - Main Storage Worst Pattern
00A Diagnostic Select Switch - Main Storage Addressing
00C Diagnostic Select Switch - Local Storage Worst Pattern
00D Diagnostic Select Switch - Local Storage Addressing
00F Log-Out Pushbutton

001 Dump
404 TRAP during Read Phase
405 TRAP during Write Phase

*Y0, Y2 Stats set by diagnostic select switch and start key
**Y0, Y3 Stats set by diagnostic select switch and start key

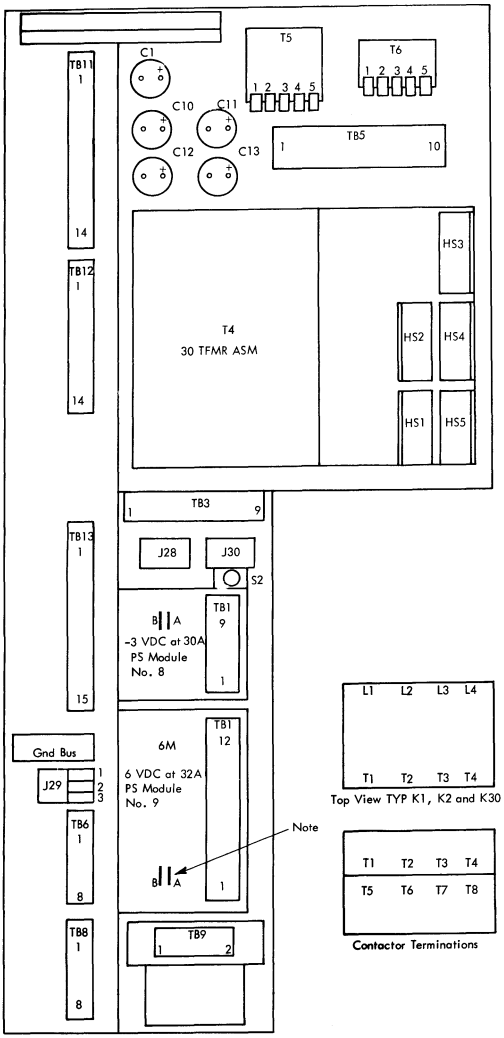
Selector Channel:

700 1 Byte Data Service
704 2 Byte Data Service
708 Terminal Status
710 Status after Address-In
718 Skip Count Equal to 1
71C Skip Count Greater than 1

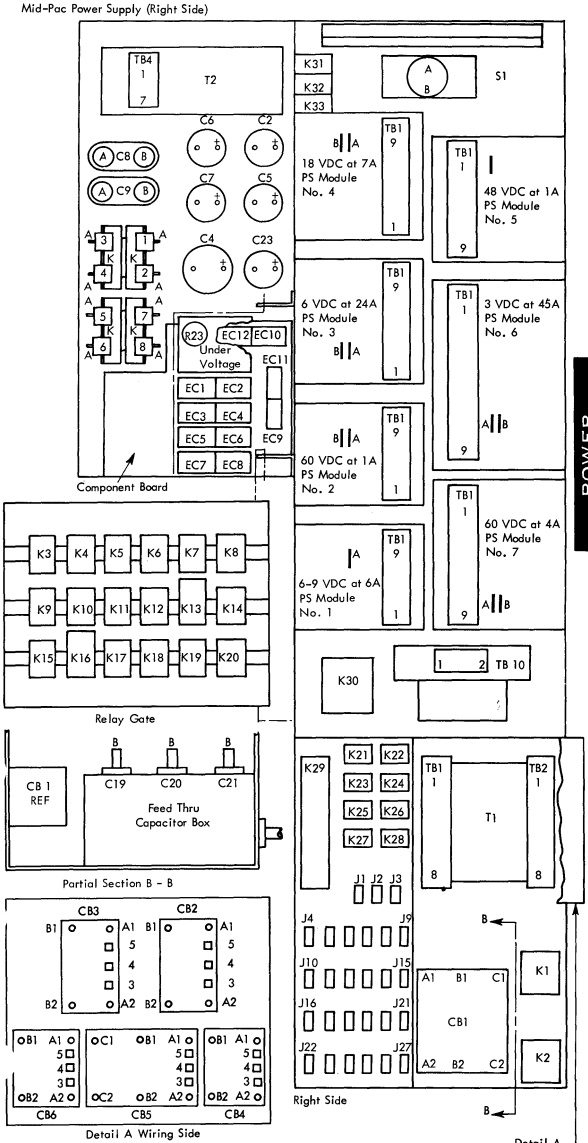
Special ROS Tapes:

010 All 0's tape
020 All 1's tape
05A ROS data check

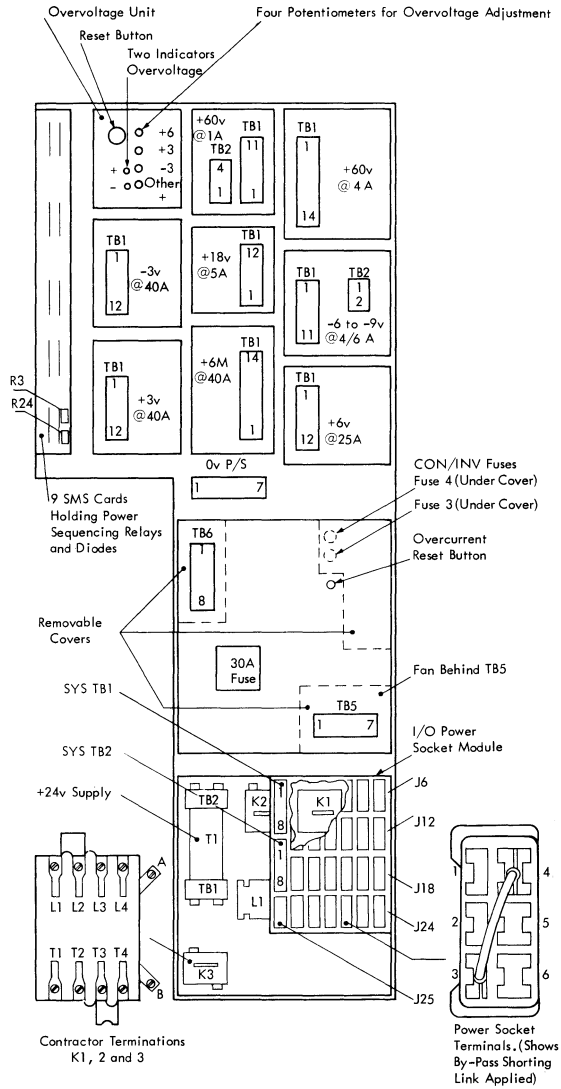
Mid-Pac Power Supply (Gate Side)



Mid-Pac Power Supply (Right Side)



Note: A Indicates Amplifier Card, B Indicates Overvoltage Card


Overvoltage Unit
Four Potentiometers for Overvoltage Adjustment
Reset Button
Two Indicators Overvoltage
+6
+3
-3
Other
+60v @1A
TB1
TB2
+60v @ 4 A
+18v @5A
-3v @40A
-6 to -9v @4/6 A
+6M @40A
+3v @40A
+6v @25A
0v P/S
R3
R24
9 SMS Cards Holding Power Sequencing Relays and Diodes
CON/INV Fuses
Fuse 4 (Under Cover)
Fuse 3 (Under Cover)
TB6
Overcurrent Reset Button
Removable Covers
30A Fuse
Fan Behind TB5
SYS TB1
TB5
I/O Power Socket Module
SYS TB2
+24v Supply
J6
J12
J18
J24
J25
K1
K2
K3
T1
L1
A
B
L1 L2 L3 L4
T1 T2 T3 T4
Contractor Terminations K1, 2 and 3
Power Socket Terminals. (Shows By-Pass Shorting Link Applied)

Mid-Pac Power-On Sequence

Insert wall plug.

If CB 1 is made, the following occurs:

Power to 24v supply

Pick KB through EPO switch N/C

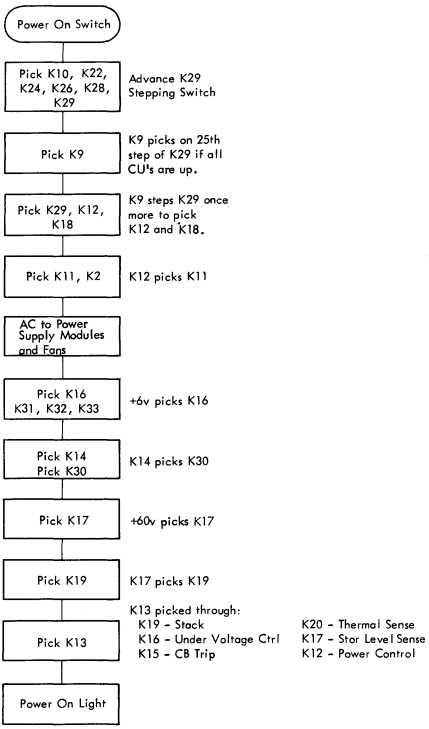
Pick K1 if CB 6 is made. Convenience outlets receive power.

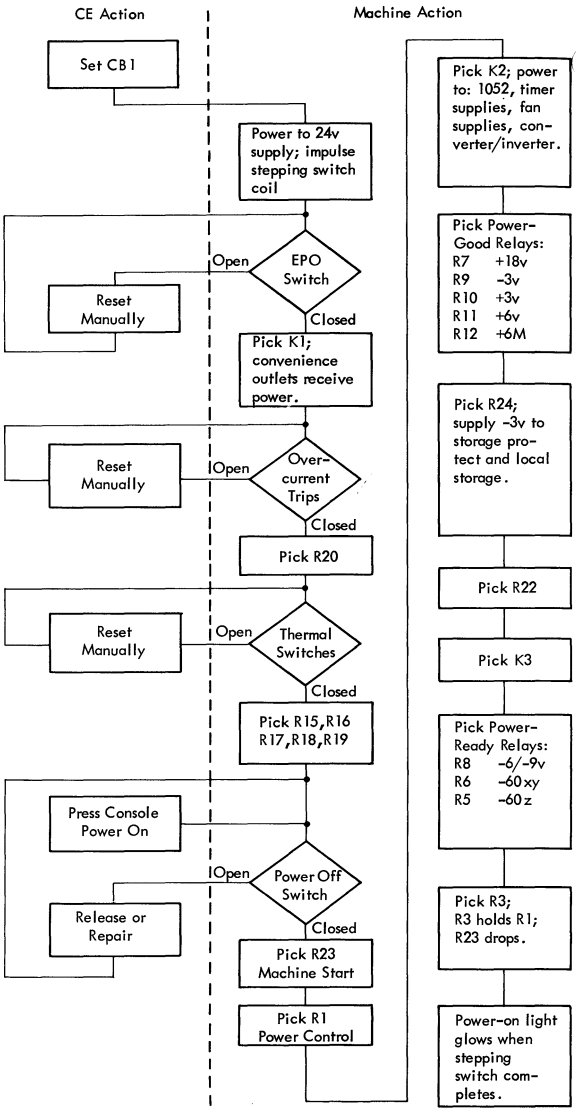
Pick K21, K23, K25, K27

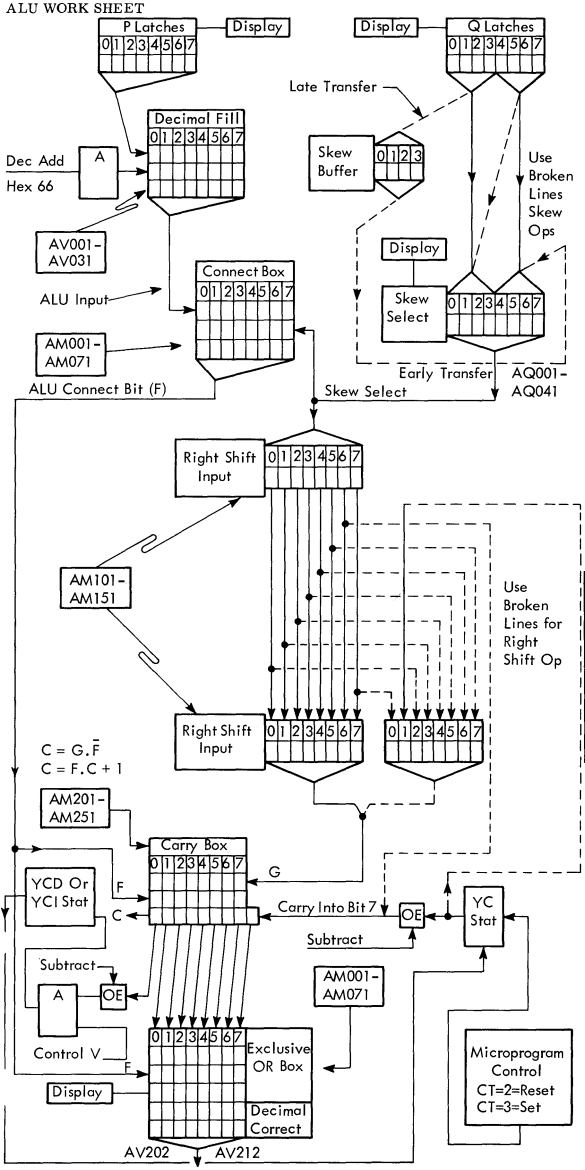
Pick K15 through K8 N/O point and power supplies overcurrent N/C points

Pick K3, K4, K5, K6, K7 through associated thermal points and K18 N/C

Pick K20 through K3, K4, K5, K6, K7 N/O points




CE Action
Machine Action
Set CB1
Power to 24v supply; impulse stepping switch coil
Open
EPO Switch
Reset Manually
Closed
Pick K1; convenience outlets receive power.
Reset Manually
Open
Over-current Trips
Closed
Pick R20
Reset Manually
Open
Thermal Switches
Closed
Pick R15,R16 R17,R18,R19
Press Console Power On
Open
Power Off Switch
Release or Repair
Closed
Pick R23 Machine Start
Pick R1 Power Control
Pick K2; power to: 1052, timer supplies, fan supplies, converter/inverter.
Pick Power-Good Relays:
R7 +18v
R9 -3v
R10 +3v
R11 +6v
R12 +6M
Pick R24; supply -3v to storage protect and local storage.
Pick R22
Pick K3
Pick Power-Ready Relays:
R8 -6/-9v
R6 -60xy
R5 -60z
Pick R3; R3 holds R1; R23 drops.
Power-on light glows when stepping switch completes.


P Latches
0 1 2 3 4 5 6 7
Display
Display
Q Latches
0 1 2 3 4 5 6 7
Late Transfer
Decimal Fill
0 1 2 3 4 5 6 7
Dec Add
Hex 66
A
Skew Buffer
0 1 2 3
Use Broken Lines Skew Ops
AV001-AV031
Display
Connect Box
0 1 2 3 4 5 6 7
ALU Input
Skew Select
0 1 2 3 4 5 6 7
AM001-AM071
Early Transfer
AQ001-AQ041
ALU Connect Bit (F)
Skew Select
Right Shift Input
0 1 2 3 4 5 6 7
AM101-AM151
Use Broken Lines for Right Shift Op
Right Shift Input
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
C = G.F̄
C = F.C + 1
AM201-AM251
Carry Box
0 1 2 3 4 5 6 7
G
YCD Or YCI Stat
F
C
Carry Into Bit 7
OE
YC Stat
Subtract
Subtract
A
OE
AM001-AM071
0 1 2 3 4 5 6 7
Exclusive OR Box
Control V
F
Display
Decimal Correct
Microprogram Control
CT=2=Reset
CT=3=Set
AV202
AV212

ALU Control Signals and Functions

	ALU Control Bits	Logical Operation		Active Control Signals												Connect Box Function	Right Shift Function	YC Stat Conditions	YCI or YCD Stat Conditions
		Abb	Meaning	K	L	M	N	H	J	S	W	X	Y	V	U	(F)	(G)		
*P	0 0000	OR	P + Q	K	L	M									U	P or Q	Zero Output	No effect on Bit 7	Not affected
#	1 0001	AND	P · Q	K											U	P and Q	Zero Output	No effect on Bit 7	Not affected
	2 0010	DSQ	P - Q (Decimal)	K			N	H		S			Y	V	U	Equivalent P Q	Inverse of Q	YC OFF gives carry to Bit 7	Set if NO carry Bit 0
*P	3 0011	SUQ	P - Q (Binary)	K			N			S			Y	V	U	Equivalent P Q	Inverse of Q	YC OFF gives carry to Bit 7	Set if NO carry Bit 0
	4 0100	P	Pass P	K	L										U	Pass P	Zero Output	No effect on Bit 7	Not affected
*P	5 0101	AND	P · Q	K											U	P and Q	Zero Output	No effect on Bit 7	Not affected
P	6 0110	DSP	Q - P (Decimal)	K			N	H		S		X		V		Equivalent P Q	Q	YC OFF gives carry to Bit 7	Set if NO carry Bit 0
	7 0111	SUP	Q - P (Binary)	K			N			S		X		V		Equivalent P Q	Q	YC OFF gives carry to Bit 7	Set if NO carry Bit 0
	8 1000	PNQ	P · $\overline{Q}$		L											P · $\overline{Q}$	Zero Output	No effect on Bit 7	Not affected
P	9 1001	Q	Pass Q	K		M										Pass Q	Zero Output	No effect on Bit 7	Not affected
P	10 1010	XOR	Exclusive OR (P Q)		L	M										P Q Exclusive OR	Zero Output	No effect on Bit 7	Not affected
	11 1011	QNP	$\overline{P}$ · Q			M										$\overline{P}$ · Q	Zero Output	No effect on Bit 7	Not affected

* Direct function

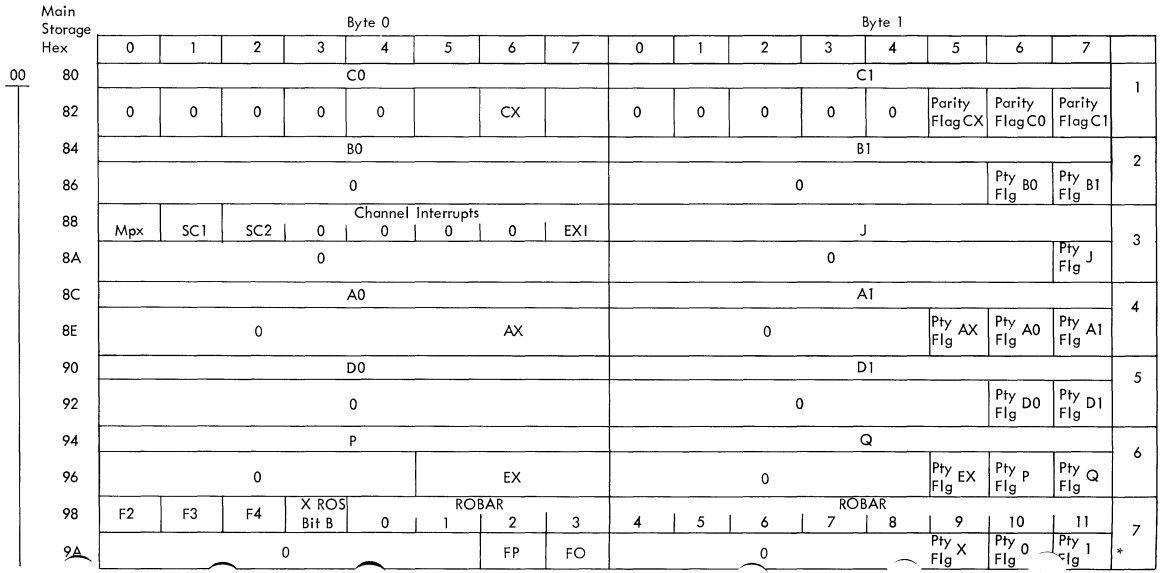
\# Gives function check

ALU Control Signals and Functions (cont'd)

				K	L	M	N	H	J	S	W	X	Y	V	U				
P	12 1100	RSH	1 bit rt Shift of Q								W	X		V	U	Zero Output	Q shifted two positions right	YC ON gives right shift output Bit 1	Set if there is carry Bit 0
	13 1101	LSH	1 bit left shift of Q									X		V	U	Zero Output	Q	YC ON gives carry to Bit 7	Set if there is carry Bit 0
	14 1110	DAD	P + Q (Decimal)		L	M		N	J			X		V	U	P Q Exclusive OR	Q	YC ON gives carry to Bit 7	Set if there is carry Bit 0
*P	15 1111	ADD	P + Q (Binary)		L	M						X		V		P Q Exclusive OR	Q	YC On gives carry to Bit 7	Set if there is carry Bit 0

* Direct function
# Gives function check

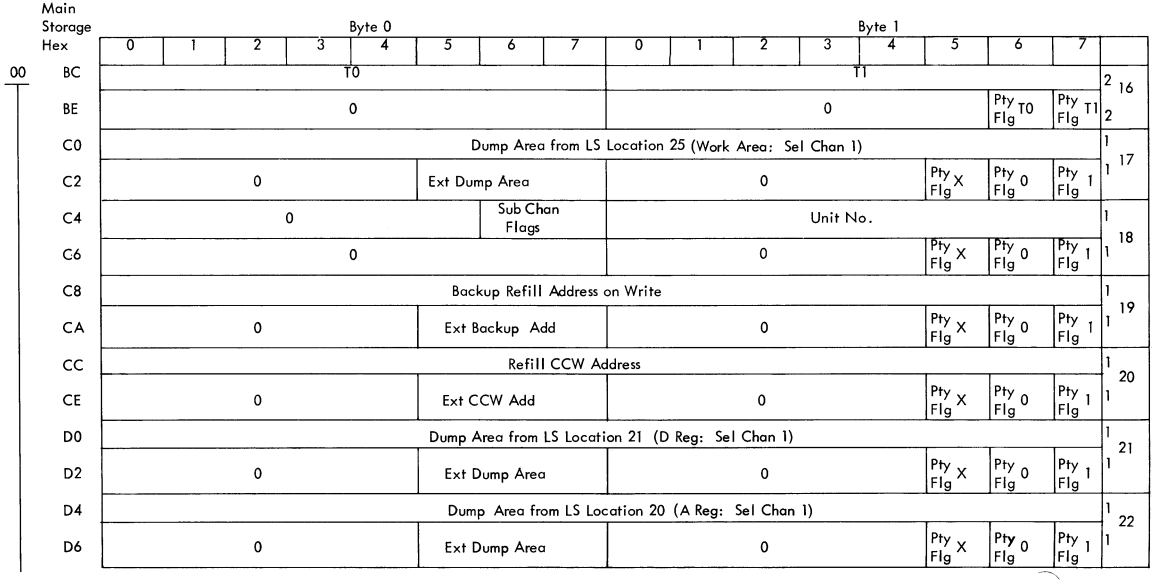
MAIN STORAGE ALLOCATIONS



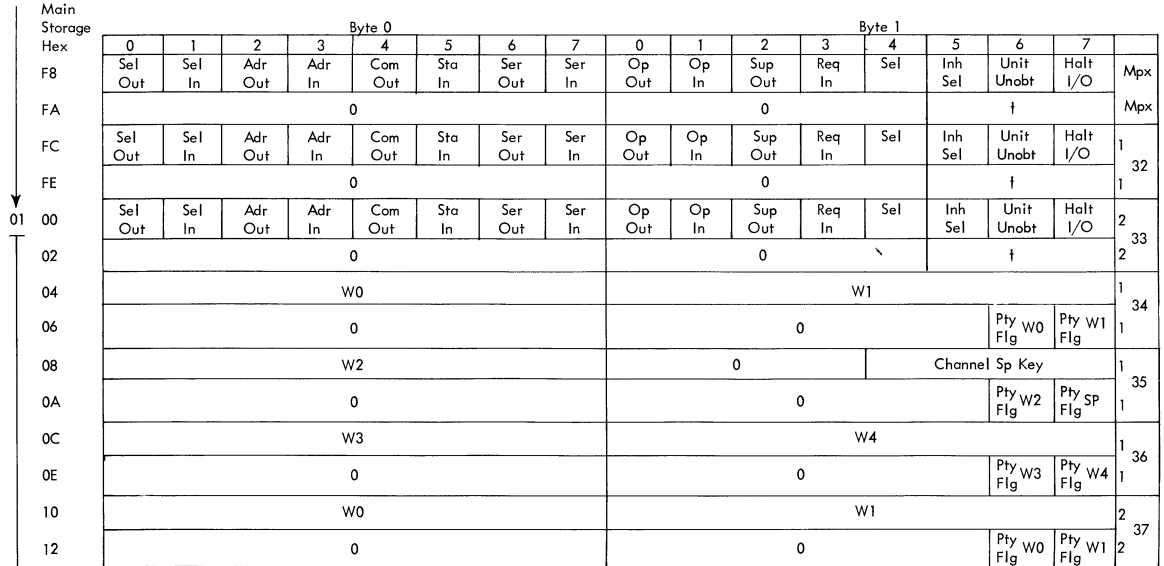
00

9C	R0 Pty Chk	PSA	ISA	I/O State	... Pty Chk	YCD	Y8	Early Check	ALU 2-Wire Checks Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	8
9E	0						ROS Data Chk	ROS Adr Chk	0					Pty X Flg	Pty 0 Flg	Pty 1 Flg	**
A0	D1 Pty Chk	P Pty Chk	Q Pty Chk	J Dcdr Chk	Stat Pty Chk	LS Read Pty Chk	P Dcdr Chk	Q Dcdr Chk	ALU Fun Chk	2 Wire I-P Car	SPLS Data Chk	SQ Sel Chk	2 Wire O-P Car	EX Pty Chk	ROAR Check	Late Check	9
A2	0							MSAB Pty Chk	0					Pty X Flg	Pty 0 Flg	Pty 1 Flg	***
A4	H								B Dcdr Chk	C Dcdr Chk	D Dcdr Chk	H Incr Dcdr Chk	H Des Dcdr Chk	N Dcdr Chk	H Load Dcdr Chk	Ctrl Check	10
A6	0								0					1	Pty H Flg	Pty 1 Flg	****
A8	Y0	Y1	Y2	Y3	SQ 0	SQ1	SQ2	SQ3	Y4	Y5	Y6	Y7	0	0	0	YC1	11
AA	0								0							Pty Y Flg	
AC	Instruction Buffer LS Loc 43								SPLS Data				Key				12
AE	0								0						Pty 0 Flg	Pty SP Flg	
B0	S0								S1								1 13
B2	0					SX			0					Pty SX Flg	Pty S0	Pty S1	1
B4	T0								T1								1 14
B6	0								0						Pty T0 Flg	Pty T1 Flg	1
B8	S0								S1								2 15
BA	0					SX			0					Pty SX Flg	Pty S0	Pty S1	2

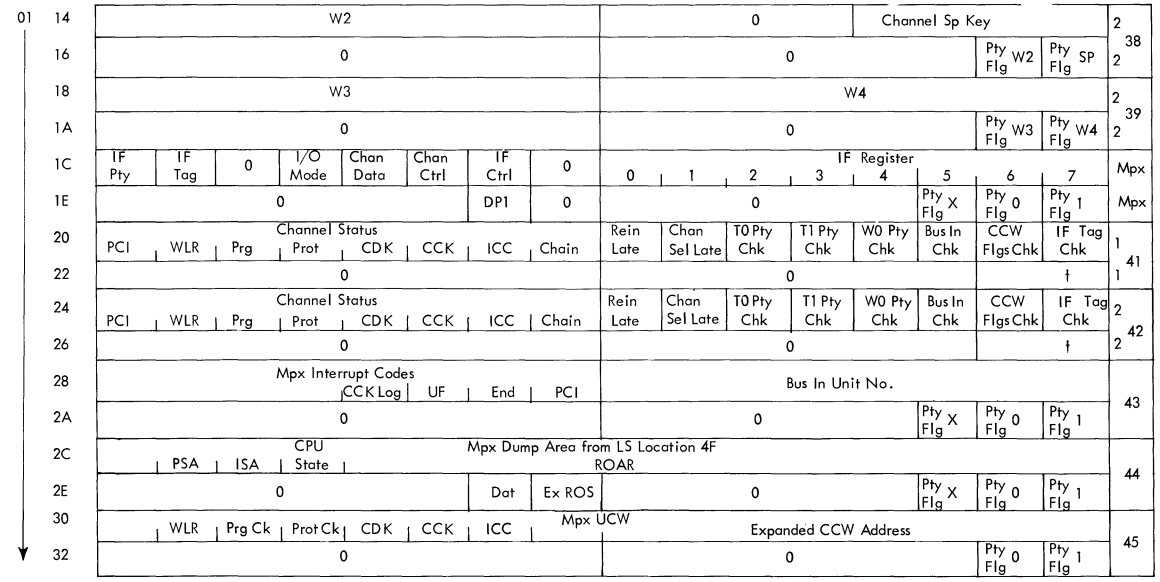
LOGOUT

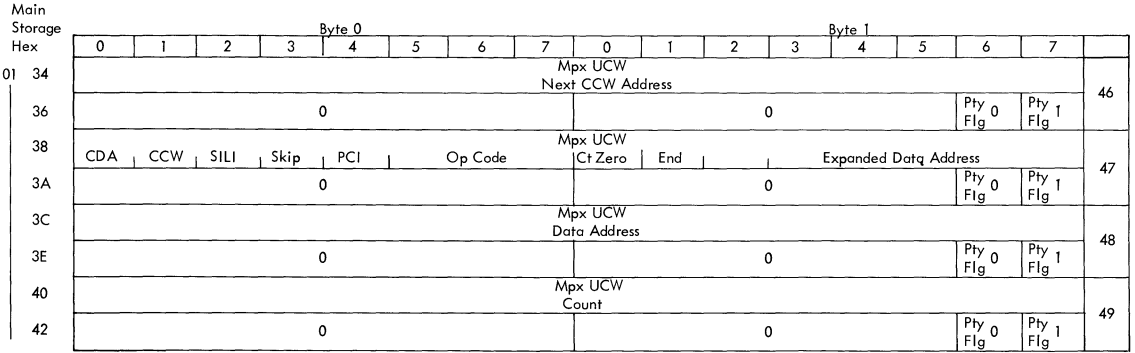

Main Storage Hex
Byte 0
Byte 1
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
00
BC T0 T1 2 16
BE 0 0 Pty Flg T0 Pty Flg T1 2
C0 Dump Area from LS Location 25 (Work Area: Sel Chan 1) 1 17
C2 0 Ext Dump Area 0 Pty Flg X Pty Flg 0 Pty Flg 1 1
C4 0 Sub Chan Flags Unit No. 1 18
C6 0 0 Pty Flg X Pty Flg 0 Pty Flg 1 1
C8 Backup Refill Address on Write 1 19
CA 0 Ext Backup Add 0 Pty Flg X Pty Flg 0 Pty Flg 1 1
CC Refill CCW Address 1 20
CE 0 Ext CCW Add 0 Pty Flg X Pty Flg 0 Pty Flg 1 1
D0 Dump Area from LS Location 21 (D Reg: Sel Chan 1) 1 21
D2 0 Ext Dump Area 0 Pty Flg X Pty Flg 0 Pty Flg 1 1
D4 Dump Area from LS Location 20 (A Reg: Sel Chan 1) 1 22
D6 0 Ext Dump Area 0 Pty Flg X Pty Flg 0 Pty Flg 1 1

Addr								
D8	Dump Area from LS Location 35 (Work Area: Sel Chan 2)						2	23
DA	0	Ext Dump Area	0	Pty Flg X	Pty Flg 0	Pty Flg 1	2	
DC	0	Sub Chan Flags	Unit No.				2	24
DE	0		0	Pty Flg X	Pty Flg 0	Pty Flg 1	2	
E0	Backup Refill Address on Write						2	25
E2	0	Ext Dump Area	0	Pty Flg X	Pty Flg 0	Pty Flg 1	2	
E4	Refill CCW Address		0				2	26
E6	0	Ext Dump Area	0	Pty Flg X	Pty Flg 0	Pty Flg 1	2	
E8	Dump Area from LS Location 31 (D Reg: Sel Chan 2)						2	27
EA	0	Ext Dump Area	0	Pty Flg X	Pty Flg 0	Pty Flg 1	2	
EC	Dump Area from LS Location 30 (A Reg: Sel Chan 2)						2	28
EE	0	Ext Dump Area	0	Pty Flg X	Pty Flg 0	Pty Flg 1	2	
F0	Channel Flags: CDA | CC | SILI | Skip | Ch Y3 | Ch Y1 | Write | Rd Back		Chaining Boundary Flags: 0 | 1 | 2 | 3 | 4	Buffer Count: 0 | 1 | =			1	29
F2	0		0	†			1	
F4	Channel Flags		Chaining Boundary Flags	Buffer Count			2	30
F6	0		0	†			2	



Main Storage Hex	Byte 0								Byte 1									
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7		
F8	Sel Out	Sel In	Adr Out	Adr In	Com Out	Sta In	Ser Out	Ser In	Op Out	Op In	Sup Out	Req In	Sel	Inh Sel	Unit Unobt	Halt I/O	Mpx	
FA	0								0					†			Mpx	
FC	Sel Out	Sel In	Adr Out	Adr In	Com Out	Sta In	Ser Out	Ser In	Op Out	Op In	Sup Out	Req In	Sel	Inh Sel	Unit Unobt	Halt I/O	1	32
FE	0								0					†			1	
01 00	Sel Out	Sel In	Adr Out	Adr In	Com Out	Sta In	Ser Out	Ser In	Op Out	Op In	Sup Out	Req In	Sel	Inh Sel	Unit Unobt	Halt I/O	2	33
02	0								0					†			2	
04	W0								W1								1	34
06	0								0						Pty Flg W0	Pty Flg W1	1	
08	W2								0				Channel Sp Key				1	35
0A	0								0						Pty Flg W2	Pty Flg SP	1	
0C	W3								W4								1	36
0E	0								0						Pty Flg W3	Pty Flg W4	1	
10	W0								W1								2	37
12	0								0						Pty Flg W0	Pty Flg W1	2	


01
14 W2 | 0 | Channel Sp Key | 2
16 0 | 0 | Pty Flg W2 | Pty Flg SP | 2 38
18 W3 | W4 | 2
1A 0 | 0 | Pty Flg W3 | Pty Flg W4 | 2 39
1C IF Pty | IF Tag | 0 | I/O Mode | Chan Data | Chan Ctrl | IF Ctrl | 0 | IF Register 0 1 2 3 4 5 6 7 | Mpx
1E 0 | DP1 | 0 | 0 | Pty Flg X | Pty Flg 0 | Pty Flg 1 | Mpx
20 Channel Status: PCI | WLR | Prg | Prot | CDK | CCK | ICC | Chain | Rein Late | Chan Sel Late | T0 Pty Chk | T1 Pty Chk | W0 Pty Chk | Bus In Chk | CCW Flgs Chk | IF Tag Chk | 1
22 0 | 0 | † | 1 41
24 Channel Status: PCI | WLR | Prg | Prot | CDK | CCK | ICC | Chain | Rein Late | Chan Sel Late | T0 Pty Chk | T1 Pty Chk | W0 Pty Chk | Bus In Chk | CCW Flgs Chk | IF Tag Chk | 2
26 0 | 0 | † | 2 42
28 Mpx Interrupt Codes: CCK Log | UF | End | PCI | Bus In Unit No. | 43
2A 0 | 0 | Pty Flg X | Pty Flg 0 | Pty Flg 1
2C CPU State: PSA | ISA | Mpx Dump Area from LS Location 4F ROAR | 44
2E 0 | Dat | Ex ROS | 0 | Pty Flg X | Pty Flg 0 | Pty Flg 1
30 Mpx UCW: WLR | Prg Ck | Prot Ck | CDK | CCK | ICC | Expanded CCW Address | 45
32 0 | 0 | Pty Flg 0 | Pty Flg 1



Nomenclature:

Mpx	Multiplex Channel
1	Selector Channel 1
2	Selector Channel 2
†	Parity is not generated for these transfers

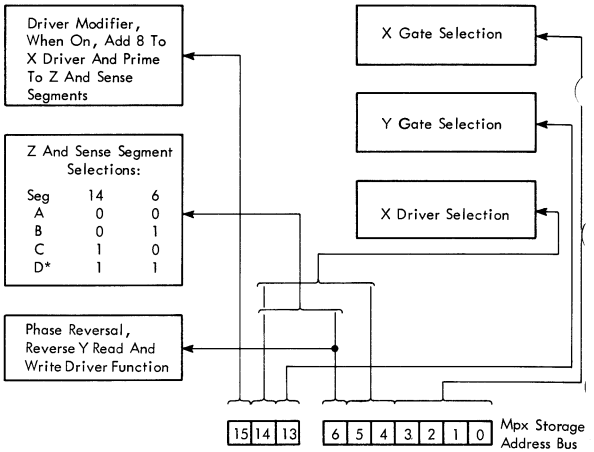
Parity flags indicate parity status of associated byte. If the flag is set, then the byte had incorrect parity.

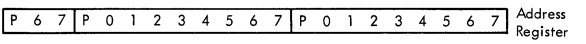
* Flags are Exclusive OR of parity bits of bytes X, 0 and 1 respectively with

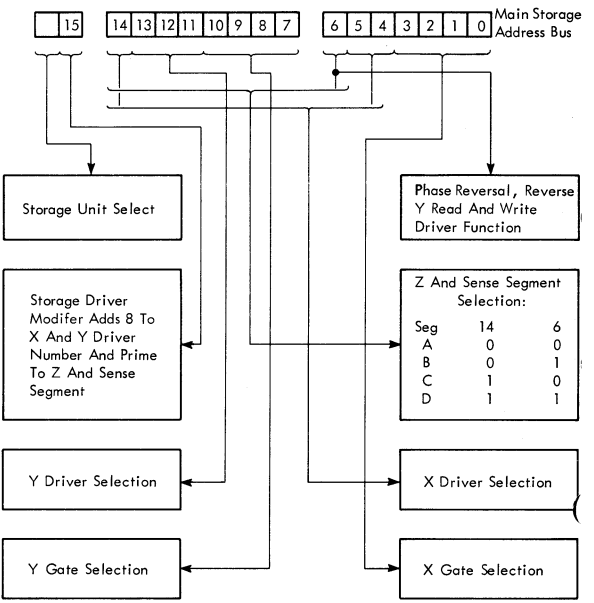
Byte X	Byte 0	Byte 1	
$\overline{\text{LSAR}}$ Pty Chk	F1	$\overline{\text{ROBAR}}$ Pty	*
Ex 2W Chk	RX Pty Chk	D/Y8 Chk	**
0	D0 Chk	SPLS Key Chk	***
Byte 1 Only: R Decr Chk			****

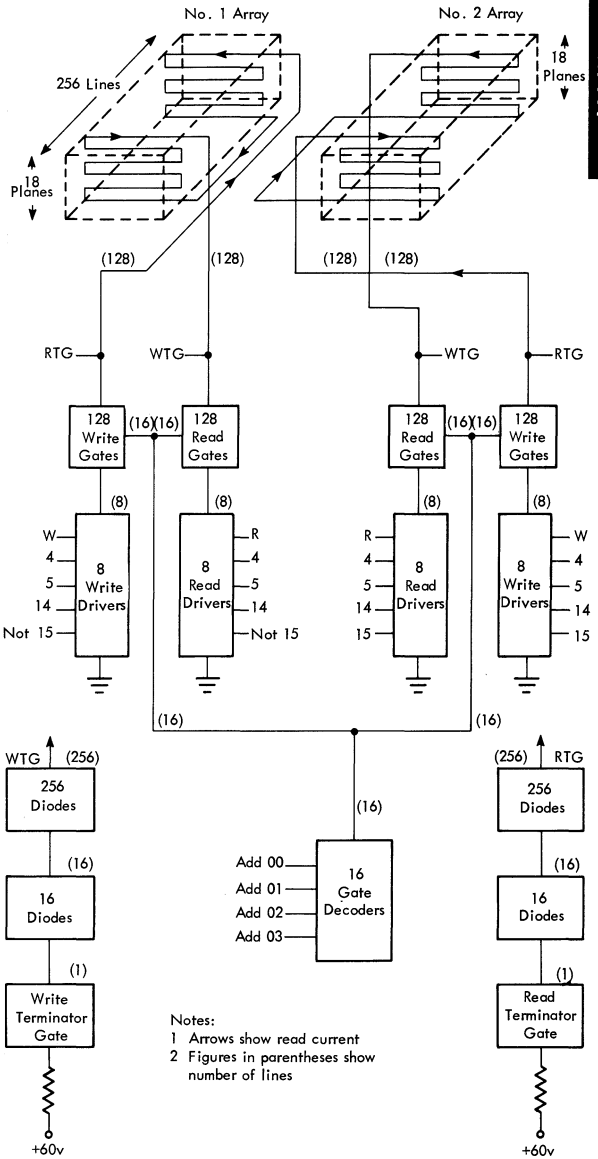
STAT FUNCTIONS

	Y0	Allow MAT on PMA
	Y1	Use Multiplex Storage
YA		
	Y2	
		Condition Code or Selected Channel (CPU or I/O State)
	Y3	
	Y4	
	Y5	General Purpose
YB		
	Y6	
	Y7	
	Y8ID	Inhibit Dump
YD		
	Y9MI	Maskable Interrupt
	Y12ERR	Stop on Error
YE	Y14IZT/IDQ	Integrated Zero Test or Invalid Decimal Digit on Q Bus
	Y15 LOAD	IPL in Progress

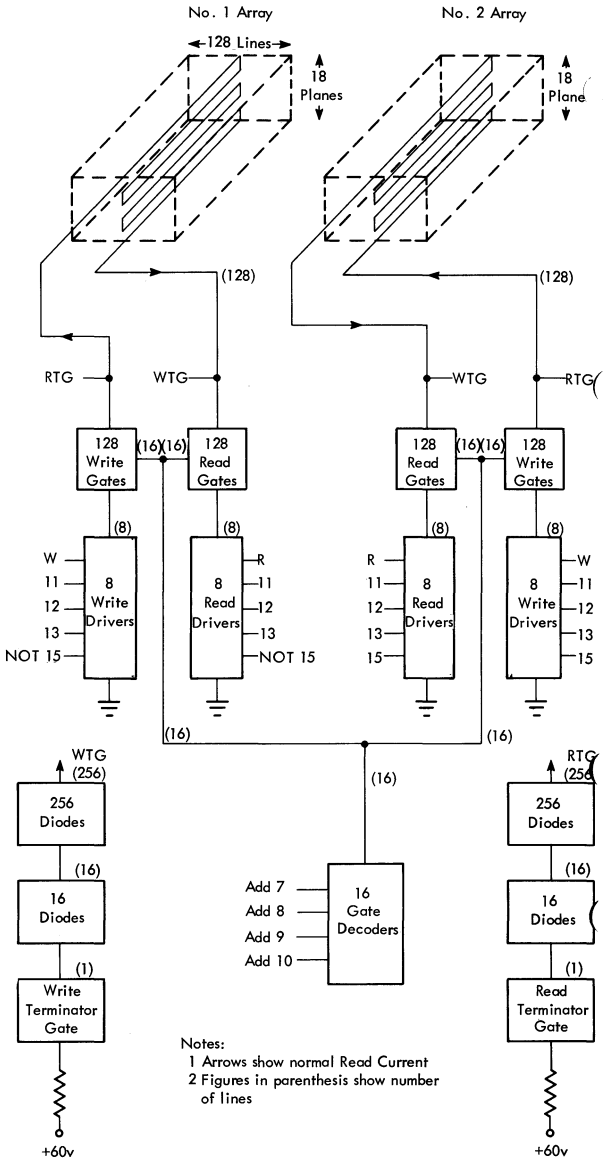

Driver Modifier, When On, Add 8 To X Driver And Prime To Z And Sense Segments
X Gate Selection
Y Gate Selection
X Driver Selection
Z And Sense Segment Selections:
Seg 14 6
A 0 0
B 0 1
C 1 0
D* 1 1
Phase Reversal, Reverse Y Read And Write Driver Function
15 14 13
6 5 4 3 2 1 0
Mpx Storage Address Bus


P 6 7 P 0 1 2 3 4 5 6 7 P 0 1 2 3 4 5 6 7
Address Register

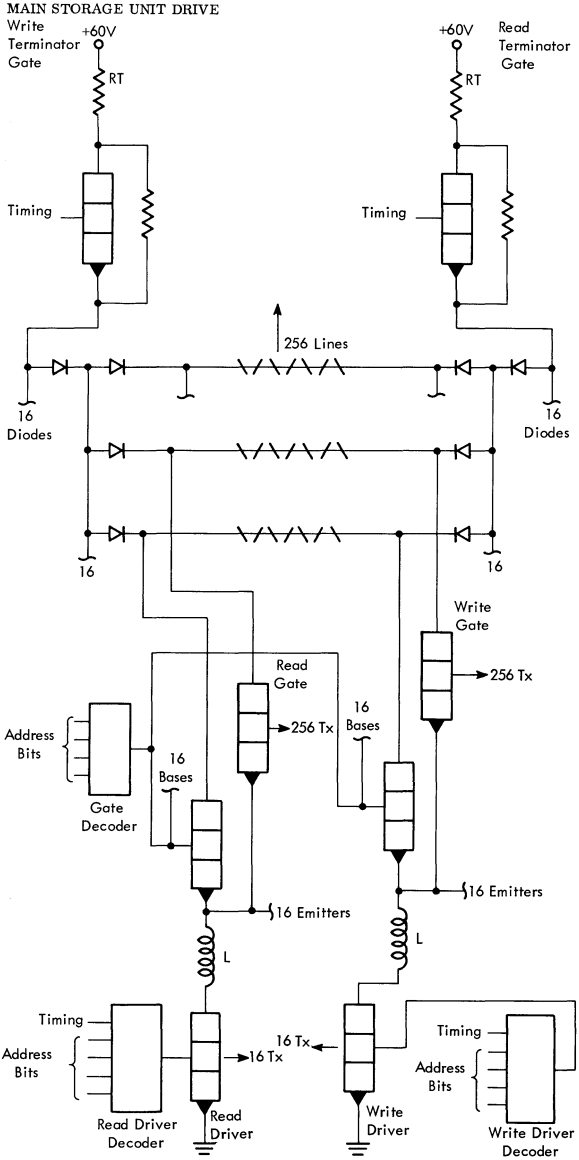

15
14 13 12 11 10 9 8 7
6 5 4 3 2 1 0
Main Storage Address Bus
Storage Unit Select
Phase Reversal, Reverse Y Read And Write Driver Function
Storage Driver Modifer Adds 8 To X And Y Driver Number And Prime To Z And Sense Segment
Z And Sense Segment Selection:
Seg 14 6
A 0 0
B 0 1
C 1 0
D 1 1
Y Driver Selection
X Driver Selection
Y Gate Selection
X Gate Selection

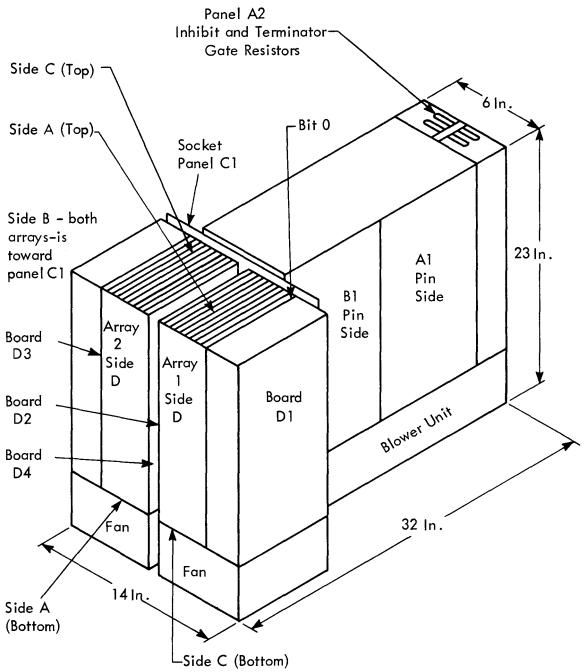


Notes:
1 Arrows show read current
2 Figures in parentheses show number of lines



Notes:
1 Arrows show normal Read Current
2 Figures in parenthesis show number of lines

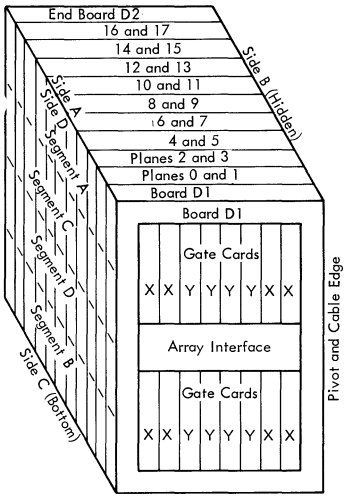

MAIN STORAGE UNIT DRIVE
Write Terminator Gate
+60V
RT
Timing
+60V
Read Terminator Gate
RT
Timing
256 Lines
16 Diodes
16 Diodes
16
16
Write Gate
256 Tx
Read Gate
256 Tx
16 Bases
Address Bits
16 Bases
Gate Decoder
16 Emitters
16 Emitters
L
L
Timing
Address Bits
16 Tx
16 Tx
Timing
Address Bits
Read Driver Decoder
Read Driver
Write Driver
Write Driver Decoder



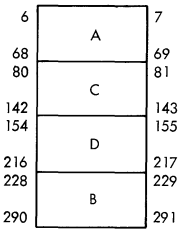
Dimensions are approximate

Cables are color coded as follows:
- blue
- white sense-inhibit lines
- black
- gray - 8 wires to terminator gates
- black and brown - gate decode lines
- black and orange - read-write drivers
- purple - bump circuits

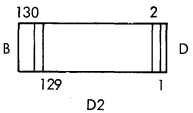
STORAGE ARRAY END BOARD D1



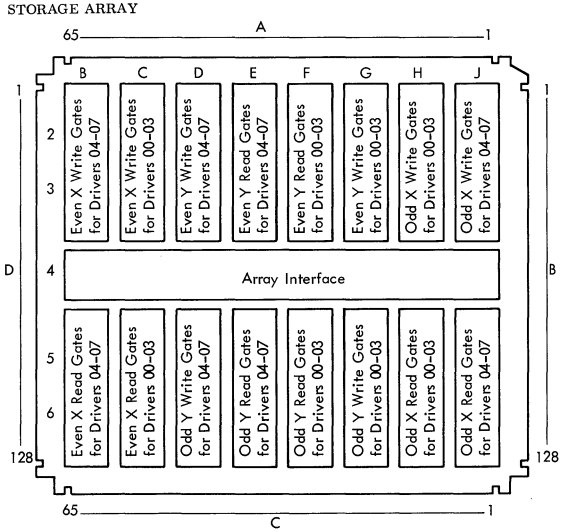
X Lines (9 Ohms)



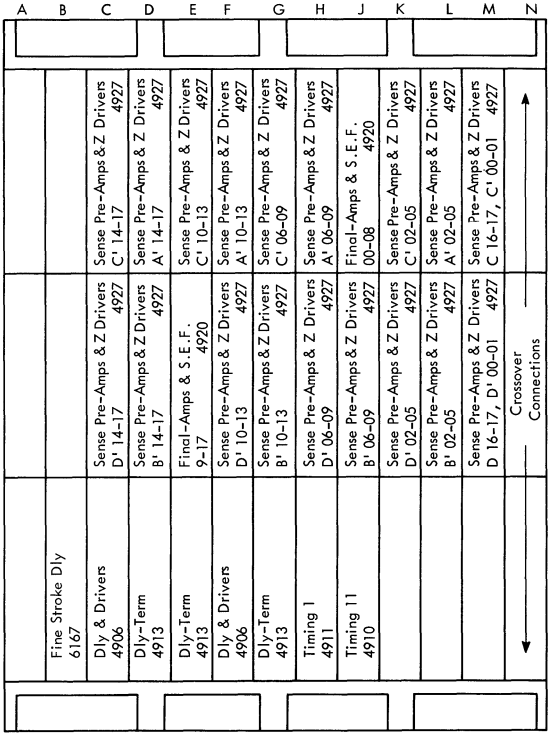
Y Lines



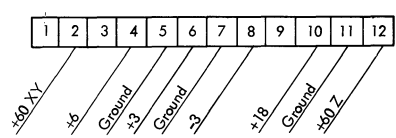
STORAGE ARRAY



BOARD A1 -- CARD SIDE



TB1 Voltage Terminal Board



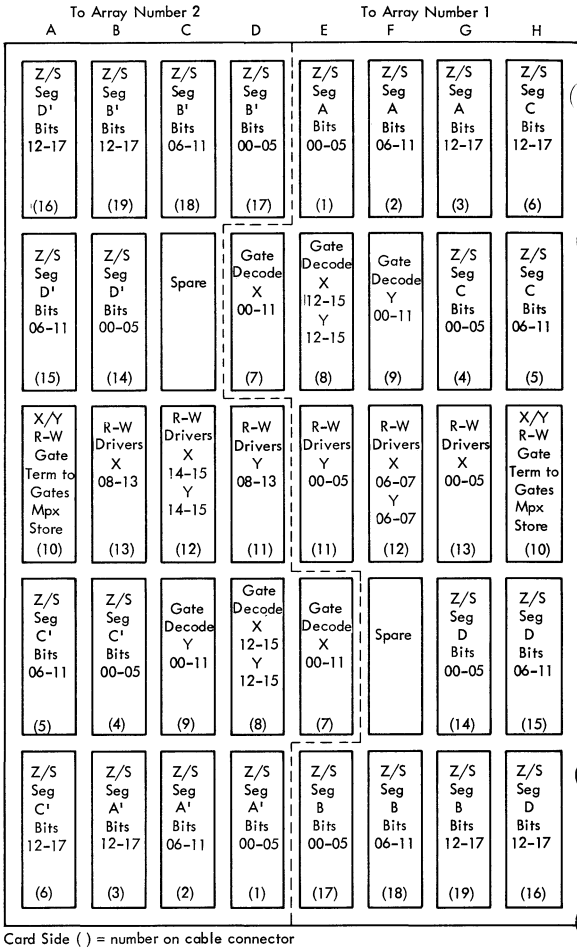
Voltage tolerance at TB1 under dynamic conditions is ± 2 percent.

BOARD B1 -- CARD SIDE

8	7	6	5	4	3	2	1
	← Crossover Connections →						
	Z Timing & Z Clamp 4926		Sense Pre-Amps & Z Drivers B 16-17, B' 00-01 4927		Sense Pre-Amps & Z Drivers A 16-17, A' 00-01 4927		
			Sense Pre-Amps & Z Drivers D 12-15 4927		Final Amplifiers & S.E.F. 9-17 4920		
	Z Timing & Z Clamp 4926		Sense Pre-Amps & Z Drivers B 12-15 4927		Sense Pre-Amps & Z Drivers C 12-15 4927		
T6-B	Data-In Powering 00-17 4900		Sense Pre-Amps & Z Drivers D 8-11 4927		Sense Pre-Amps & Z Drivers A 12-15 4927		
	Data-Out Powering 00-17 4915		Sense Pre-Amps & Z Drivers B 8-11 4927		Sense Pre-Amps & Z Drivers C 8-11 4927		
			Sense Pre-Amps & Z Drivers D 4-7 4927		Sense Pre-Amps & Z Drivers A 8-11 4927		
T7-B	Drivers 4904		Sense Pre-Amps & Z Drivers B 4-7 4927		Sense Pre-Amps & Z Drivers C 4-7 4927		
	Address Bit Powering 4909		Final-Amplifiers & S.E.F. 0-8 4920		Sense Pre-Amps & Z Drivers A 4-7 4927		
	Address Bit Powering 4909		Sense Pre-Amps & Z Drivers D 0-3 4927		Sense Pre-Amps & Z Drivers C 0-3 4927		
T8-B	Multiplex Store 4914		Sense Pre-Amps & Z Drivers B 0-3 4927		Sense Pre-Amps & Z Drivers A 0-3 4927		
	Y Gate Decoders 4905		X Gate Decoders 4905		Terminator Gates & Z Clamp 4912		
	Drivers 4904		Drivers 4904		Drivers 4904		

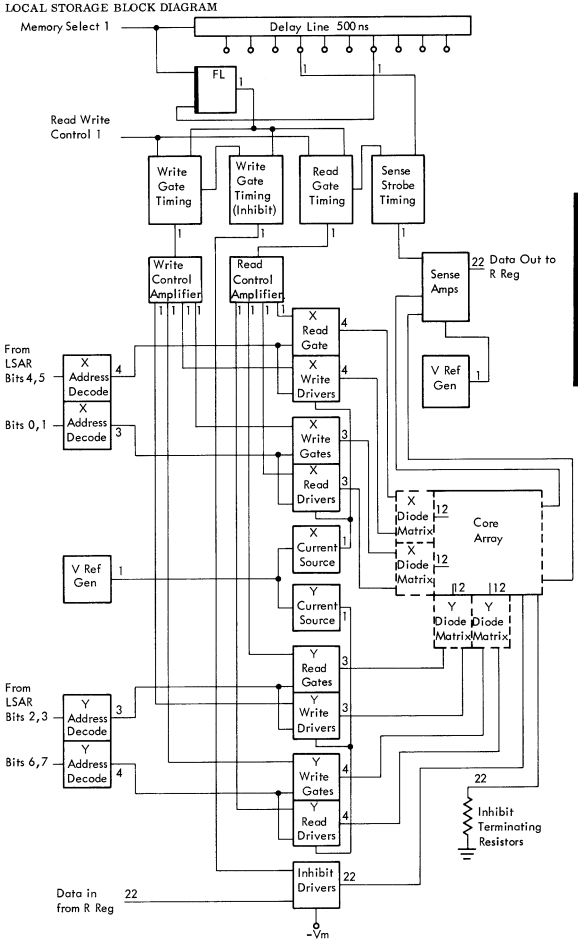
A B C D E F G H J K L M N

SOCKET PANEL C1



Card Side ( ) = number on cable connector

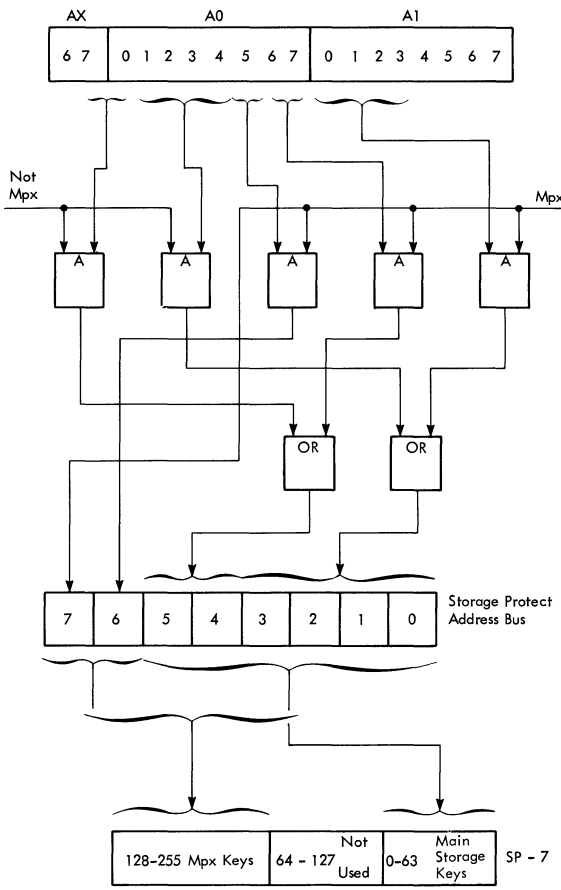
LOCAL STORAGE BLOCK DIAGRAM



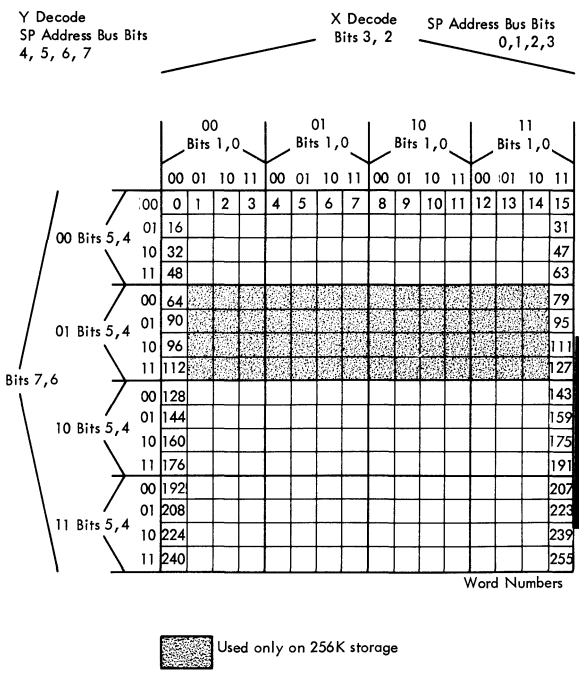
Hex	Dec		Hex	Dec	
00	00		40	64	
01	01		41	64	Work Area
02	02		42	66	Undefined
03	03	Work	43	67	Insn Buffer
04	04	Area	44	68	Sys Mask, Stor Prot
05	05		45	69	
06	06		46	70	Prog Mask, IC0-7
07	07		47	71	IC 8-23
08	08		48	72	Start I/O Switch
09	09	Work	49	73	
0A	10	And	4A	74	
0B	11	Logout Area	4B	75	
0C	12		4C	76	
0D	13		4D	77	
0E	14		4E	78	
0F	15		4F	79	
10	16	Decoded	50	80	Decoded To
		To Above			Above
1F	31	Locations	5F	95	Locations
20	32	Selector	60	96	
21	33	Channel 1	61	97	
22	34		62	98	
23	35	UCW	63	99	
24	36	(See Page 96)	64	100	
25	37		65	101	
26	38		66	102	
27	39	Mpx Working Space	67	103	Unassigned
28	40		68	104	
29	41	(See Page 93)	69	105	
2A	42	Interrupt Buffer	6A	106	
2B	43		6B	107	
2C	44		6C	108	
2D	45	Unassigned	6D	109	
2E	46		6E	110	
2F	47		6F	111	
30	48	Selector	70	112	
31	49	Channel 2	71	113	
32	50	UCW	72	114	
33	51		73	115	
34	52		74	116	
35	53		75	117	
36	54		76	118	
37	55	Unassigned	77	119	Unassigned
38	56		78	120	
39	57		79	121	
3A	58		7A	122	
3B	59		7B	123	
3C	60		7C	124	
3D	61		7D	125	
3E	62		7E	126	
3F	63		7F	127	

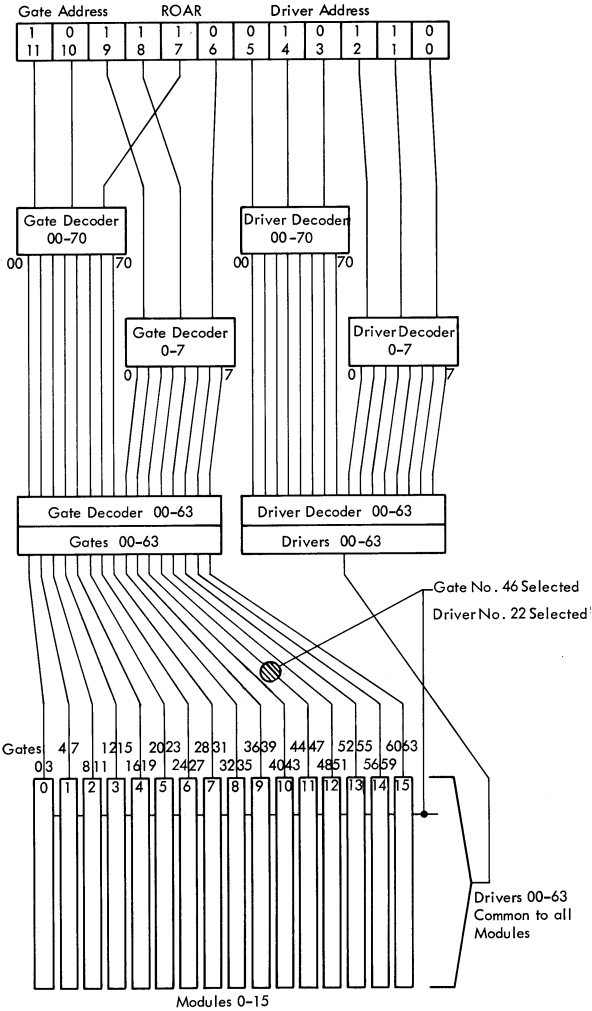
Hex	Dec		Hex	Dec	
80	128		C0	192	Floating Point
81	129		C1	193	Register 0
82	130		C2	194	
83	131		C3	195	
84	132		C4	196	Floating Point
85	133		C5	197	Register 2
86	134	Decoded	C6	198	
87	135	To	C7	199	
88	136	Right	C8	200	Floating Point
89	137	Block	C9	201	Register 4
8A	138		CA	202	
8B	139	→	CB	203	
8C	140		CC	204	Floating Point
8D	141		CD	205	Register 6
8E	142		CE	206	
8F	143		CF	207	
90	144	Decoded Above	DO	208	Decoded To Above Locations
9F	159		DF	223	
A0	160		E0	224	0
A1	161		E1	225	
A2	162		E2	226	
A3	163		E3	227	1
A4	164		E4	228	
A5	165		E5	229	2
A6	166	Decoded	E6	230	
A7	167	To	E7	231	3
A8	168	Right	E8	232	Fxp
A9	169	Block	E9	233	Regs 4
AA	170		EA	234	
AB	171	→	EB	235	5
AC	172		EC	236	
AD	173		ED	237	6
AE	174		EE	238	
AF	175		EF	239	7
B0	176		F0	240	
B1	177		F1	241	8
B2	178		F2	242	
B3	179		F3	243	9
B4	180		F4	244	
B5	181		F5	245	Fxp 10
B6	182		F6	246	Regs
B7	183	Decoded	F7	247	11
B8	184	To	F8	248	
B9	185	Right	F9	249	12
BA	186	Block	FA	250	
BB	187		FB	251	13
BC	188		FC	252	
BD	189	→	FD	253	14
BE	190		FE	254	
BF	191		FF	255	15

STORAGE PROTECT ADDRESSING

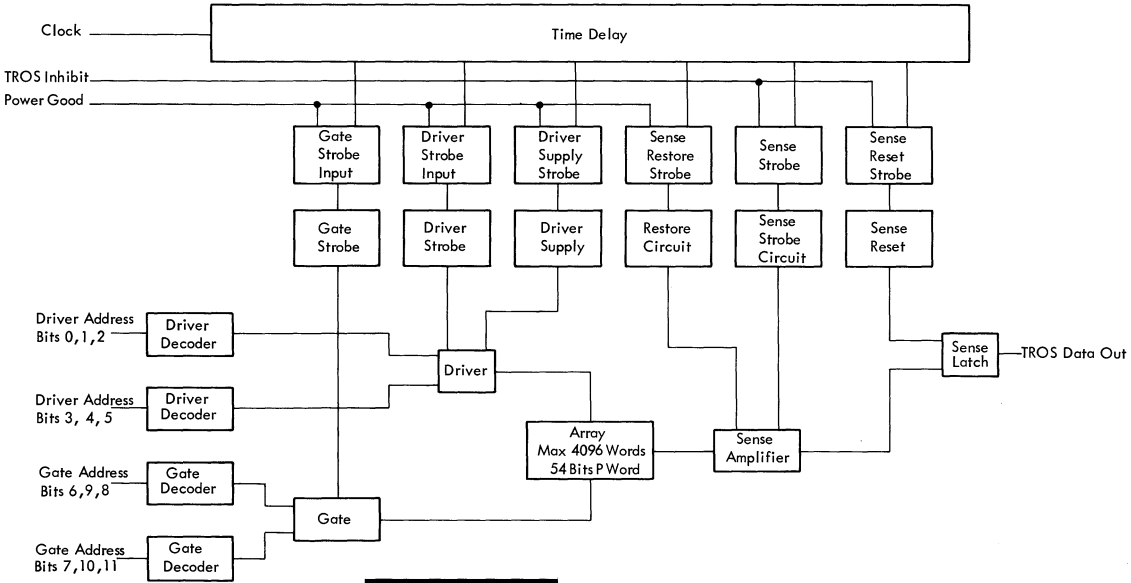


Storage Protect Address Decode Diagram

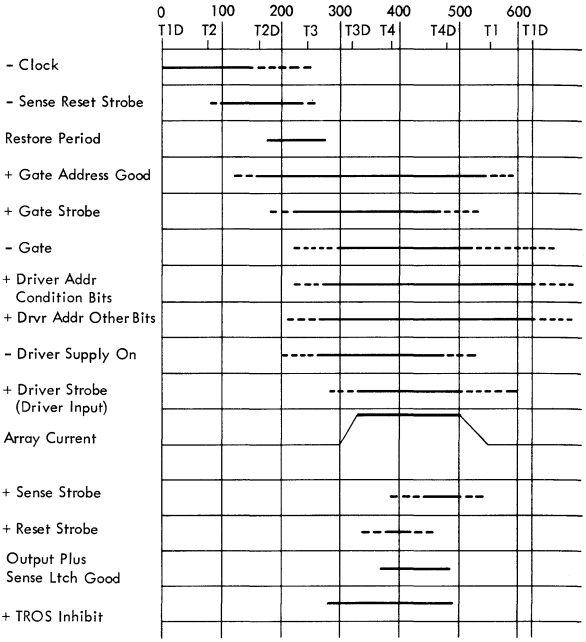


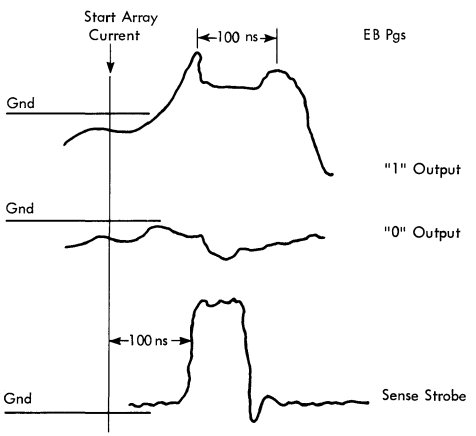

Gate Address
ROAR
Driver Address
1 11
0 10
1 9
1 8
1 7
0 6
0 5
1 4
0 3
1 2
1 1
0 0
Gate Decoder 00-70
00
70
Driver Decoder 00-70
00
70
Gate Decoder 0-7
0
7
Driver Decoder 0-7
0
7
Gate Decoder 00-63
Gates 00-63
Driver Decoder 00-63
Drivers 00-63
Gate No. 46 Selected
Driver No. 22 Selected
Gates 0 3 4 7 8 11 12 15 16 19 20 23 24 27 28 31 32 35 36 39 40 43 44 47 48 51 52 55 56 59 60 63
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Drivers 00-63 Common to all Modules
Modules 0-15

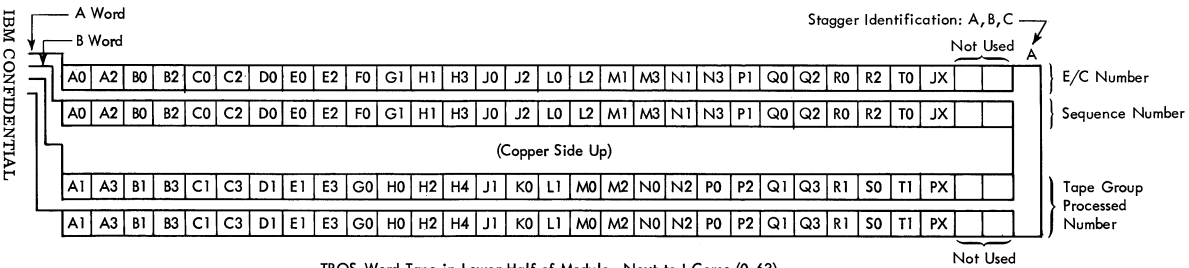
TF 3LOCK DIAGRA



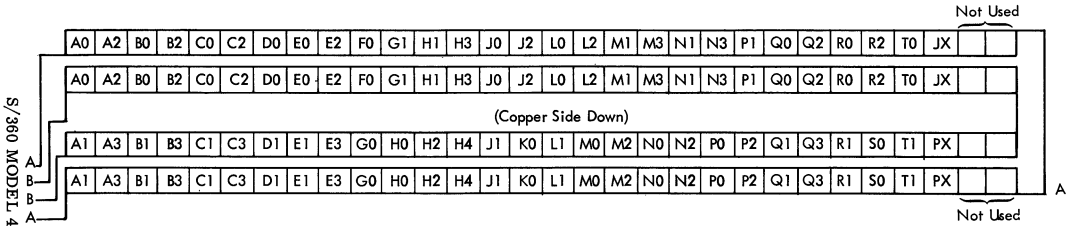
SENSE CURRENT WAVE FORMS





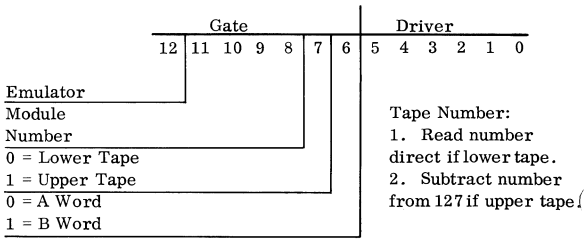


TROS-Word Tape in Lower Half of Module, Next to I Cores (0-63)



TROS-Word Tape in Upper Half of Module (64-127)

TROS Address Decode



Stagger Class = $\frac{\text{Tape number}}{3}$

Remainder of 0 = A
1 = B
2 = C

All FOSSL micro-orders are listed with signal name and ALD sheet number in the CE ROS Field Charts, classified by Field. To avoid searching through the complete list for an unfamiliar micro-order and hardware reference a linking diagram is given below.

The link box corresponds line for line with CAS boxes but indicates the ROS field producing each CAS statement and in most cases the order in which they appear.

Thus if an arithmetic function is suspected, the link box in the corresponding line shows G in the arithmetic function position permitting immediate reference to CG field in the ROS Control Field Chart which gives an ALD sheet, signal name, conditions and other hardware references.

Location of ROS Fields Causing CAS Statements

This Address	XX	005	This Address
Emit (3 Formats). . . E	CE,CN,CK	CT	Carry
Arithmetic . . . . A	CP,CG,CQ (CK)	CM	
LSAR L	CH		
Data Transfer . . . D	CJ CL		
Control . . . C or S	CR	RBD	
Next ROS Address . . R	CB	CC	Condition

Symbols inside the box are ROS fields.

CA Field

ROS Bits 0-3

Part of Next ROS Word Address Under CB and CD Field Control (ROS Address is Shown Under CD Field)

Sense Latches EB181
A-Field Entry RX051

Edge Char.	Micro-Order	Bits	Dec. Order	Function	ALD
Not applicable		XXXX	-	CA ROAR PSN 5-2 when CB = 0-13 AND CD = Not 2	RX091
				CA ROAR PSN 9-6 when CB = 0-13 AND CD = 2, or CB = 15	RX011
				CA not used when CB = 14	-

CB Field

ROS Bits 4-7

Forms PSN1 of Next ROS Address by Testing Specified Conditions With CD = 0 or 2 in CPU or I-O State. (ROS Address is Shown Under CD Field). Issue Special Controls when CD = 1 or 3

CPU State, CD Field = 0 or 2

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Branch Condition	ALD	
R	0	0000	CB0	No Output (ROAR PSN1 is Reset to 0)	DR751	
R	1	0001	CB1	Set PSN1 of ROAR to 1	DR751	
R	YCD	0010	CB2	Direct Carry	RX111	
R	L2 $\neq$ 0	0011	CB3	LSAR PSN6 or 7 non zero (Test at T2 Del. same cycle)	DR751	
R	ALU $\neq$ 0	0100	CB4	ALU output non zero (Test at T2 Del. same cycle)	RX111	
R	Y0	0101	CB5	Storage Protect Primer Stat = 1	DR751	
R	Y2	0110	CB6	Condition Register PSN0 = 1	DR751	
R	Y4	0111	CB7	General-Purpose Stat Y4 = 1 (Not REINT or ROSCAR in control)	DR751	
R	YCH3			(REINT or ROSCAR in control) channel general stat YCH3	GE571	HE571
R	Y6	1000	CB8	General-Purpose Stat Y6 = 1 (Not REINT or ROSCAR in control)	DR751	
R	SI (7)			(REINT or ROSCAR in control) Bit 7 of S-Register	GE571	HE571
R	FXPTO	1001	CB9	Fixed Point Overflow (Test at T2 Del. same cycle)	RX111	
R	ALU7	1010	CB10	ALU output PSN7 = 1 (Test at T2 Del. same cycle)	DR751	
R	IZT	1011	CB11	Integrating Zero Test	DR751	
R	CBY			(REINT or ROSCAR in control) chaining boundary in buffer (output ops)	GE571	HE571
R	IDQ	1100	CB12	Invalid Decimal digit on ALU entry Q	DR751	
R	ASCII	1101	CB13	ASCII Stat	DR751	
R	Minus	1110	CB14	Q Bus PSN4-7 = 11 or 13	DR751	
R	FNB	1111	CB15	Special Control for function branch (see CD Field)	RX011	

CB Field

I-O State, CD Field = 0 or 2

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Branch Condition	ALD	
R	0	0000	CB0	No Output (ROAR PSN1 is Reset to 0)	DR571	
R	1	0001	CB1	Set PSN1 of ROAR to 1	DR571	
R	YCD	0010	CB2	Direct Carry	RX111	
R	ADR-1	0011	CB3	Address In Latch Gated by Y2, Y3	FL001	
R	ALU $\neq$ 0	0100	CB4	ALU output non zero (Test at T2 Del. same cycle)	RX111	
		0101	CB5	Not Used (CPU only)		
R	Halt	0110	CB6	Manual Stop Latch	FL001	
R	Y4	0111	CB7	(Not REINT or ROSCAR in control) Gen. Stat Y4 = 1	DR571	
R	YC113			(REINT or ROSCAR in control) Channel Gen. Stat Y3 = 1	GE571	HE571
R	Y6	1000	CB8	(Not REINT or ROSCAR in control) Gen. Stat Y6 = 1	DR751	
R	SI (7)			(REINT or ROSCAR in control) LS bit of S register	GE571	HE571
R	Load	1001	CB9	Load button (console)	FL001	
R	ALU7	1010	CB10	ALU output bit 7 (Test at T2 Del. same cycle)	DR751	
R	SVC-1	1011	CB11	(Not REINT or ROSCAR in control) Service In AND NOT Command Out or Service Out)	FL001	
R	CBY			(REINT or ROSCAR in control) chaining boundary in buffer (output ops)	GE571	HE571
R	SOΩCO	1100	CB12	Service Out or Command Out	FL001	
		1101	CB13	Not Used (CPU only)		
		1110	CB14	Not Used (CPU only)		
R	FNB	1111	CB15	Special Control for Function Branch	RX011	

CB Field

CD = 1

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Branch Condition	ALD MPX	ALD SC1	ALD SC2
R	ADR-0	0000	CB0	Set Address Out	FB001	GG511	HG511
R	CMD-0	0001	CB1	Set Command Out	FB001	GG523	HG523
R	SVC-0	0010	CB2	Set Service Out	FB011	GG524	HG524
R	Sel	0011	CB3	Set Select Logic to stop interface sequence	FBQ31	GG511	
R	ISO	0100	CB4	Inhibit Select Out	FB031	GG512	HG512
R	1→IR	0101	CB5	Set Interrupt Request	FB021	GF503	HF503
R	0→IR	0110	CB6	Reset Interrupt Request	FB021	GF503	HF503
R	CL-CH	0111	CB7	Clear channel	FK051	GE571	HE571
R	⌐OP-O	1000	CB8	Reset Operational Out	FB021	GG513	HG513
R		1001	CB9	Unused	-	-	-
R	ICC	1010	CB10	Set Interface Control Check; Force Error Stat Y12 and force Log-Out	KC081	GG543	HG543
R	REINT	1011	CB11	Reinterpret conditions as shown in CB, CC, CL and CM fields. Remains effective until Restore (Rest) is called		GE571	HE571
R	Dump	1100	CB12	Turn on Dump Control when stat Y10 = 1	FJ021	-	-
R	HIO	1101	CB13	Halt device on interface	FB021	GG531	HG531
		1110	CB14	Unused	-	-	-
R	FNB	1111	CB15	Special control for Function Branch	RX011	RX011	RX011

The B Condition is set to zero whenever CB = 0-14 and CD = 1 or 3 (EXCEPT UNDUMP)

CB Field

CD = 3, CPU and MPX and SC

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Special Controls	ALD CPU/MPX	SC1	SC2
						GE591	HE591
R	STAN	0000	CB0	SC Channel Analyse Status, Force 4-way branch on result	JA114		
R	DC-IN	0001	CB1	Timing Line In for Direct Data Accept	KC081		
R	Log	0010	CB2	Start Log-Out	KM131	GE591	HE591
R	SSM	0011	CB3	Set External Mask with ALU bit 7 with bit 1 for Channel 1 and bit 2 for Channel 2	KH171		
R	SWEA	0100	CB4	Set ASCII, Wait and Enable with ALU bits 4, 5 and 6	KC081		
R	STPC1	0101	CB5	Stop T Clock	KH161		
R	Manual	0110	CB6	Define Normal Stop Loop		GG511	HG511
R	0 SL0	0111	CB7	Reset Select Out gated by Y2, Y3	RX112		
R	Edit	1000	CB8	If Q bus = 001000XY set next ROS address bit 1 and 0 to XY If Q bus = 001000XY set next ROS address bit 1 and 0 to 11	RX112		
R	SMSC	1001	CB9	Set 1401 Emulator Selector Channel Latch (Y2, Y3 gated)	RX003		
R	DAT	1010	CB10	Enable/Disable Dec. Address Translator (1401 Emulator)	RX003		
R		1011	CB11	Unused	-		
R		1100	CB12	Unused	-		
R	SUP-O	1101	CB13	Set Suppress Out gated by Y2, Y3		GG512	HG512
R	Undump	1110	CB14	Restore ROAR for next cycle	RX011		
R	FNB	1111	CB15	Function Branch	RX011		

The B condition is set to zero whenever CB = 0-14 and CD = 1 or 3 (EXCEPT UNDUMP)

CC Field

ROS Bits 8-11

CPU State

Sense Latches EB201
Decoder DR111
Decoder Check DS011

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Condition ANDed with CPU/I-O States to form ROS next Address bit 0	ALD
R	0	0000	CC0	No output (ROAR PSN0 is reset to zero	
R	1	0001	CC1	Set PSN0 of ROAR to 1	DR752
R	YCD	0010	CC2	Direct Carry	DR752
R	L4 ≠	0011	CC3	LSAR PSN4, 5, 6 or 7 non zero (Test at T2 Del. same cycle)	DR752
R	ALU ≠ 0	0100	CC4	ALU output non zero (Test at T2 Del. same cycle)	RX113
R	Y1	0101	CC5	MPX Store Address Stat Y1 = 1	DR752
R	Y3	0110	CC6	Condition register PSN 1 = 1	DR752
R	Y5	0111	CC7	General-Purpose stat Y5 = 1	DR752
R	YCH1			(Reinterpret or ROSCAR in control) General-Purpose Channel Stat YCH1	GE571 HE571
R	Y7	1000	CC8	General-Purpose Stat Y7 = 1	DR752
R	CH = WR			(Reinterpret or ROSCAR in control) Channel Command Write Channel Read/Write Stat = 1	GE571 HE571
R	ALU6	1001	CC9	ALU output PSN6 = 1 (Test at T2 Del. same cycle)	RX111
R	ALU0	1010	CC10	ALU output PSN0 = 1 (Test at T2 Del. same cycle)	RX111
R	CDA			(Reinterpret or ROSCAR in control) Data Chaining Indicator	GE571 HE571
R	Q0 ≠	1011	CC11	Q bus PSN0-3 non zero (Test at T2 Del. same cycle)	DR752
R	PRI	1100	CC12	Program Interrupt	DR752
R	YCI	1101	CC13	Indirect Carry	RX111
R	SAT	1110	CC14	Invalid Storage (Memory) Address (IMA) or Protected Storage (Memory) violation (PMA, YM)	DR752
R	QPTY	1111	CC15	Test Q bus for bad parity (Test at T2 Del. same cycle)	DR752

CC Field

I-O State

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Condition ANDed with CPU/I-O States to form ROS Next Address Bit 0	ALD MPX	ALD SC1	ALD SC2
R	0	0000	CC0	No output (ROAR PSN0 is reset to zero	DR752	DR752	DR752
R	1	0001	CC1	Set PSN0 of ROAR to 1	DR752	DR752	DR752
R	YCD	0010	CC2	Direct Carry	FL011	GE571	GE571
R	IR	0011	CC3	Test Interrupt Request Latch (gated by Y2, Y3)	RX113	RX113	RX113
R	ALU ≠ 0	0100	CC4	ALU output non zero (Test at T2 Del. same cycle)	FL011	GE571	HE571
R	DU/IF	0101	CC5	Unit Unobtainable or I-F Free (Gated by Y2, Y3)	DR572		
R	MSC	0110	CC6	Is 1401 Emulator Latch = 1		GE571	HE571
R	Y5	0111	CC7	General-Purpose Stat Y5 = 1 (Not REINT or ROSCAR in control)	DR752		
R	YCH1			Selector Channel General-Purpose Stat Y1 (REINT called or ROSCAR in control)		GE571	HE571
R	Y7	1000	CC8	General-Purpose Stat Y7 = 1 (Not REINT or ROSCAR in control)	DR752		
R	CH = WR			Selector Channel Read-Write Stat; Write = 1 (REINT called or ROSCAR in control)		GE571	HE571
R	HLD ≠ 1	1001	CC9	Set Direct Control Accept Register on absence of Hold line	FL011		
R	CDA	1010	CC10	Selector Channel Data Chaining Indicator (CDA Flag and cnt. = 0 and not Chaining Boundary)		GE571	HE571
R	STA-I	1011	CC11	Status In gated by Y2, Y3	FL011		
		1100	CC12	Not Used (CPU State only)			
R	BU I	1101	CC13	Selector Channel Buffer empty (gated by Y2, Y3)		GE531	HG531
R	SAT	1110	CC14	Invalid Storage Address (IMA) or Protected Storage Violation (PMA, YM)	DR752		
R	OP-I	1111	CC15	(MX) Operational In and no (Status In or Address In) gated by Y2, Y3	FL011		

CD Field

ROS Bits 12, 13

ROS Address Control, CB Field Interpretation

Sense Latches EB211
Ctrl Latch & Dec. DR131
Decoder Check DS011

Conditions	Source of ROS Address Bits											
	11	10	9	8	7	6	5	4	3	2	1	0
CD = XX CB = 15	D0	D1	A0	A1	A2	A3	0	Q0	Q1	Q2	Q3	
CD = 0 and CB = 0-14	X0	X1	X2	X3	X4	X5	A0	A1	A2	A3	B Cond	C Cond
CD = 2 and CB = 0-14	X0	X1	A0	A1	A2	A3	X6	X7	X8	X9	B Cond	C Cond
CD = 1 and CB = 0-14	X0	X1	X2	X3	X4	X5	A0	A1	A2	A3	0	C Cond
CD = 3 and CB = 0-13	X0	X1	X2	X3	X4	X5	A0	A1	A2	A3	0	C Cond
CD = 3 and CB = 14	UNDUMP (RESTORE INTERRUPTED CPU ROS ADDRESS INTO ROAR)											

X Bits are unchanged from last ROS address
D Bits are from ROS CD Field
A Bits are from ROS CA Field
Q Bits are from Q bus

CE Field

ROS Bits 14-17 Emit Field

Sense Latches EB211
Control Latch DR171

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Provide 4 bit Binary Patterns for Control	ALD
E	0000	0000	CE0		
E	0001	0001	CE1	1. Data source for Local Storage address formation controlled by CH Field	RLXXX
E	0010	0010	CE2		
E	0011	0011	CE3		
E	0100	0100	CE4	2. Data source for set or reset of stats controlled by CN Field, SC only:- bit 2 sets but cannot reset Program Check	RYXXX
E	0101	0101	CE5		
E	0110	0110	CE6		
E	0111	0111	CE7		
E	1000	1000	CE8	3. Data source for setting the ALU Function Register controlled by CN = 15	RPXXX
E	1001	1001	CE9		
E	1010	1010	CE10		
E	1011	1011	CE11	4. Data source for ALU P or Q inputs controlled by CP or CQ field	RPXXX RQXXX
E	1100	1100	CE12		
E	1101	1101	CE13		
E	1110	1110	CE14		
E	1111	1111	CE15		

CF Field

ROS Bit 18

Sense Latch EB221
F Field Entry RX001

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ROS Word Address Parity Bit (Current)	ALD
		0	-	Odd Parity compared with ROAR parity (ROS address CK) ≠	RX001
		1	-	Even Parity compared with ROAR parity (ROS address CK) ≠	RX001

≠ Checks if correct word has been read out

CG Field

ROS Bits 19-20

Sense Latches EB221
G-Field Entry KP021

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ALU Function Control	ALD
A	?	00	CG0	Indirect Function if Y8 = 0 and not REINT or ROSCAR in control Function Register F set to emit value seé fields CN, CE	KP021 KP023
A	Ω			Direct 'OR' function if Y8 = 1 or REINT called or ROSCAR in control. Function register = 0000	
A	.	01	CG1	Direct logic function 'AND' P and Q Function register = 0101	KP023/32
A	-	10	CG2	Direct arithmetic function 'MINS', P-Q Function register = 0011	KP023/32
A	+	11	CG3	Direct arithmetic function 'PLUS', P + Q Function register = 1111	KP023/32

CH Field

ROS Bits 21-25 CPU, MX, SC

Sense Latches EB231
Decoder DS021
Decoder Check DS081

Left Edge Char.	Micro-Order Left	Micro-Order Right	Right Edge Char.	Bits	Dec. Order	Function - Local Storage Address Control	ALD
L	BE→L			00000	CH0	Load LSAR from source BE and use	DS0XX
L				00001	CH1	Not used	-
L	H→L	L→H		00010	CH2	Use H-Register	DS0XX
L				00011	CH3	Not used	-
L	AE→L	L→J		00100	CH4	Load LSAR from source AE, use, load J-register	DS0XX
L	BE→L	L→J		00101	CH5	Load LSAR from source BE, use, load J-register	DS0XX
L	QE→L	L→J		00110	CH6	Load LSAR from source QE, use, load J-register	DS0XX
L	J→L	L→J		00111	CH7	Use J-register	DS0XX
						Decrement = 1	
L	BE→L	INT	C	01000	CH8	Selector Channel only. Allow other channel to break in	HB506
L				01001	CH9	Not used	-
L	H→L	L-1→H		01010	CH10	Use H-register and decrement by 1	DS0XX, CC001
L				01011	CH11	Not used	-
L	AE→L	L-1→J		01100	CH12	Load LSAR as for AE, use, decrement by 1, load J	DS0XX, CC001
L	BE→L	L-1→J		01101	CH13	Load LSAR as for BE, use, decrement by 1, load J	DS0XX, CC001
L	QE→L	L-1→J		01110	CH14	Load LSAR as for QE, use, decrement by 1, load J	DS0XX, CC001
L	J→L	L-1→J		01111	CH15	Use J-register and decrement by 1	DS0XX, CC001

					Increment = 1	
L	BE→L	REST	C	10000 CH16	Selector Channel only. If ROSCAR in control, restore control to ROAR. If ROAR in control reset the REINTERPRET control.	GG512
L				10001 CH17	Not used	-
L	H→L	L+1→H		10010 CH18	Use H-register and increment by 1	DS0XX, CC001
L				10011 CH19	Not used	-
L	AE→L	L+1→J		10100 CH20	Load LSAR as for AE, use, increment by 1, load J	DS0XX, CC001
L	BE→L	L+1→J		10101 CH21	Load LSAR as for BE, use, increment by 1, load J	DS0XX, CC001
L	QE→L	L+1→J		10110 CH22	Load LSAR as for QE, use, increment by 1, load J	DS0XX, CC001
L	J→L	L+1→J		10111 CH23	Use J-register, and increment by 1	DS0XX, CC001
					Increment = 0	
L	JE→L	L→J		11000 CH24	Load LSAR from source JE, use, load J-register	DS0XX
L	JE→L			11001 CH25	Load LSAR from source JE, and use	DS0XX
L	AE→L			11010 CH26	Load LSAR from source AE, and use	DS0XX
L				11011 CH27	Not used	-
L	AE→L	L→H		11100 CH28	Load LSAR from source AE, use, Load H-register	DS0XX
L	BE→L	L→H		11101 CH29	Load LSAR from source BE, use, Load H-register	DS0XX
L	QE→L	L→H		11110 CH30	Load LSAR from source QE, use, Load H-register	DS0XX
					Increment = 2	
L	J→L	L-2→J		11111 CH31	Use J-register, and decrement by 2	CC001, DS071

LSAR Load Definitions E = Emit field, J = J-register, Q = Q bus

LSAR PSN SOURCE	0	1	2	3	4	5	6	7	COMMENT
QE	E0	E1	E2	Q0	Q1	Q2	Q3	E3	Q bus load for FNB
AE	0	1	0	0	E0	E1	E2	E3	
BE	0	0	0	0	E0	E1	E2	E3	CPU state
BE	0	0	1	0	E0	E1	E2	E3	I-O state MPX or SCI
BE	0	0	1	1	E0	E1	E2	E3	I-O state SC2
JE	J0	J1	J2	J3	J4	J5	E2	E3	J-register Modification

Notes

Address XX01XXXX is invalid
10XXXXXX and 11XXXXXX are equivalent
On 'Increment' a carry is not propagated from bit position 4 to bit position 3

CJ Field

ROS Bits 26-28 Y10 = 0 JX = 0 (ROS Bit 54)

Sense Latches EB241
Decoder DR275
Decoder Check DR282

Edge Char.	Micro-Order	Bits	Dec. Order	Function - R Bus Input Control	ALD	
D	Z	0000	CJ0	Zeros with good parity	-	
D	A	0001	CJ1	A register. Storage address	DR281	
D	B	0010	CJ2	R register. Bytes B0, B1 with good parity to RX	DR281	
D	C	0011	CJ3	C register. Bytes CX, C0, C1	DR281	
D	D	0100	CJ4	Storage data register D, bytes D0, D1 with good parity to RX	DR281	
D	HJ	0101	CJ5	Local store address registers, H to R0, J to R1 good parity to RX	DR281	
D	LStor	0110	CJ6	Local store output (see CL field)	KM001	
D	CIB	0111	CJ7	(MPX) Channel Input Bus Y2, Y3 = 00	DR275	DR278
				(SC1) Status to R0 and checks to R1, Y2, Y3 = 01	GE512	
				(SC2) Status to R0 and checks to R1, Y2, Y3 = 10	HE512	
				Timer value to R0, R1 (clock reset to zero when sampled)		

CJ Field

Y10 = 0 JX = 1 (ROS Bit 54) Reinterpret

Edge Char.	Micro-Order	Bits	Dec. Order	Function - R Bus Input Control	ALD
D	CST	0000	CJ0	Channel Flag register to R0, Chaining Boundary Flags to R1 (0, 4). Count Control to R1 (5, 7)	GE511
D	S	0001	CJ1	Channel S register (byte address)	GE511
D	T	0010	CJ2	Channel T register (byte count)	GE511
D	W01	0011	CJ3	Buffer bytes 0, 1 to R0, R1 (RD/BK latch = 0) Buffer bytes 0, 1 to R1, R0 (RD/BK latch = 1)	GE511
D	W2	0100	CJ4	Buffer byte W2 to R0, Channel Store Protect Key to R1 (4, 7) bits 0 to 3 MUST = 0	GE511
D	W34	0101	CJ5	Buffer bytes 3, 4 to R0, R1	GE511
D		0110	CJ6	Not used	-
D		0111	CJ7	Not used	-

CJ Field

Y10 = 1 JX = 0 (Manual state)

Edge Char.	Micro-Order	Bits	Dec. Order	Function - R Bus Input Control	ALD
D		000	CJ0	No operation	-
D	BAS	001	CJ1	Manual binary address switches	DR282
D	LAS	010	CJ2	a. LOAD Unit Address switches 1. Unit Address 8 bits - R1 2. Channel Select bits R0 positions 5, 6, 7 b. Storage Select rotary switch This switch encoded to give a three-bit field inserted into R0 positions 1, 2, 3 defined as follows: 000 = STOR PROTECT 0 001 = IC - Instruction Counter 100 = MS - Main Storage 011 = FP - Floating Point Registers 010 = GP - General Purpose Registers 101 = PSW - Program Status Word	DR282
D	BDS	011	CJ3	Manual binary data switches	DR281
D	CIT	100	CJ4	Channel input interface tags selected by Y2, Y3	GE512
		101	CJ5	Not used	
D	LStor	110	CJ6	Local store output (see CL field)	KM001
		111	CJ7	Not used	-

CK Field

ROS Bit 29

Sense Latch EB251
F-Register KP001

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Skew Control	ALD
A		0	CK0	No SKEW	AQ001
A	*	1	CK1	SKEW (See Note)	AQ001
				Note. Causes the ALU operation to incorporate a 4 bit shift on the Q bus. Q bus positions 0-3 are shifted into skew buffer. Q bus positions 4-7 are shifted into ALU input positions 0-3. Old contents of skew buffer are used for ALU input positions 4-7. When 'Load F' occurs, CK is loaded into F4.	KP001

NOTE: The asterisk calling for a Skew operation can appear either in an arithmetic statement (edge char. A) or in an emit statement (edge char. E) for a Load F micro-order (see CN field)

CL Field

ROS Bits 30-32

Edge Char.	Micro-Order	Bits	Dec. Order	Function - R Bus Output Control	ALD
D	Z	000	CL0	No destination, parity ignored	(KH025)
D	LStor	001	CL1	Local store input (Call Write limited to 100 microseconds continuous)	(KM001)
D	S	010	CL2	Selector Channel S Register	(HE521)
D	HJ	011	CL3	R0 to H, R1 to J (not REINT called or ROSCAR in control)	(RJ0XX)
D	W34			Selector Channel buffers 3 and 4 (if REINT called or ROSCAR	(HE521)
D				in control)	
D	A	100	CL4	To Register A	(RAXXX)
D	B	101	CL5	To Register B	(RBXXX)
D	C	110	CL6	To Register C	(RCXXX)
D	D	111	CL7	To Register D	(RDXXX)

If CM and CL both call for a transfer, the ALU bit transfer over-rides the byte that it concerns in the A, B, C & D registers only, but the other byte or bytes of the R bus transfer take place normally. The CL transfer to D over-rides the main storage input to D if both occur in 'READ' cycle 2. If IMA or PMA and YM occurs M-D takes priority.

The cases are:

ALU→D R →D M →D	ALU→D R →D M Lost	(One byte over-written by ALU)	R →D M →D	Valid with R→D M Lost	ALU→D M →D Not Permitted

CM Field

ROS Bits 33-36

CPU, MX and SC

Sense Latch, Control Latch and Decoder: EB261, EB271, DR36X, KU081

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ALU Output Control	ALD	
A	Z	0000	CM0	Result has no destination	-	
A	AX	0001	CM1	OR of ALU0-ALU6 to AX6; ALU7 to AX7; EX is lost	RA002	
A	A0	0010	CM2	ALU output to A0; EX to AX	RA071	
A	A1	0011	CM3	ALU to A1; EX is lost	RA171	
A	Data	0100	CM4	ALU to Direct Data Out; EX is lost	JA005	
A	CFL			(REINT or ROSCAR in control) ALU to Channel Flags; EX is lost	GE541	HE541
		0100	CM5	Not used (unless REINT called or ROSCAR in control)	-	
A	W4			(REINT or ROSCAR in control) ALU to buffer W4; EX is lost	GE541	HE541
A	B0	0110	CM6	ALU to B0; EX is lost	RB071	
				(REINT or ROSCAR in control) ALU to T0; EX is lost	GE541	HE541
A	B1	0111	CM7	ALU to B1; EX is lost	RB171	
A	T1			(REINT or ROSCAR in control) ALU to T1; EX is lost	GE541	HE541
A	SP	1000	CM8	ALU to Storage Protect keys EX is lost	KU041	
A	CSP			(REINT or ROSCAR in control) ALU to Storage Protect Keys; EX is lost	GE541	HE541
A	CX	1001	CM9	OR of ALU0-ALU6 to CX6; ALU7 to CX7; EX is lost	RC001	
A	SI			(REINT or ROSCAR in control) ALU to SI; EX is lost	GE541	HE541
A	C0	1010	CM10	ALU to C0; EX to CX	RC001	
A	S0			(REINT or ROSCAR in control) ALU to S0; EX to SX	GE541	HE541
A	C1	1011	CM11	ALU to C1; EX is lost	RC171	
A	SX			(REINT or ROSCAR in control) or of ALU0-ALU6, to SX6, ALU7 to SX7, EX is lost	GE541	HE541
A	Y	1100	CM12	ALU to YA and YB stats; EX is lost	RY001	
		1101	CM13	Not used	-	
A	D0	1110	CM14	ALU to D0; EX is lost	RD051	
A	D1	1111	CM15	ALU to D1; EX is lost	RD151	

CN Field

ROS Bits 37-40

CPU, MX and SC

Latches and Decoder DR401
ALU Function Dec. KP0X1
ALU Control Register KP02X

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Control Set/Reset Stats and ALU Free from CE Field Values	ALD
E		0000	CN0	No operation	RY001
E	→YA	0001	CN1	Set stats Y0-3 with Emit field	DR401
E	YA.┐	0010	CN2	Stats Y0-3 ANDed with 'NOT' emit (Reset stats with Emit ones)	DR401
E	YA Ω	0011	CN3	Stats Y0-3 ORed with Emit field (Set stats with Emit ones)	DR401
E	→YB	0100	CN4	Set stats Y4-7 with Emit field	DR401
E	YB.┐	0101	CN5	Stats Y4-7 ANDed with NOT Emit (Reset stats with Emit ones)	DR401
E	YB Ω	0110	CN6	Stats Y4-7 ORed with Emit field (Set stats with Emit ones)	DR401
E	YD.┐	0111	CN7	Stats Y8-11 ANDed with NOT Emit (Reset stats with Emit ones)	DR401
E	YD Ω	1000	CN8	Stats Y8-11 ORed with Emit field (Set stats with Emit ones)	DR402
E	YE.┐	1001	CN9	Stats Y12-15 ANDed with NOT Emit (Reset stats with Emit ones)	DR402
E		1010	CN10	Forces ROS decoder check for diagnostic use (no FOSSL statement)	DR363
E	YCH Ω	1011	CN11	(SC only) YCH1, YCH3 ORed with Emit (Set stats with Emit ones) CE2, Prog. Check, CE4 unused	DR402
E	YCH.┐	1100	CN12	(SC only) YCH1, YCH3 ANDed with NOT Emit (Reset stats with Emit ones) CE2, 4 unused	DR402
E		1101	CN13	Not used	-
E		1110	CN14	Not used	-
E	0000, OR	1111	CN15	ALU indirect function P OR Q ≠ F register = 0000	DR402 KP01X
E		1111	CN15	ALU indirect function ALU decoder check ≠ F register = 0001	KP001

(Continued on Next Page)

CN Field (Continued)

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Control Set/Reset Stats and ALU Free from CE Field Values	ALD
E	0010, DSQ	1111	CN15	ALU indirect function P MINUS Q (Dec) F register = 0010	KP001
E	0011, SUQ	1111	CN15	ALU indirect function P MINUS Q (Bin) F register = 0011	KP001
E	0100, P	1111	CN15	ALU indirect function PASS P ONLY ≠ F register = 0100	KP001
E	0101, AND	1111	CN15	ALU indirect function P AND Q ≠ F register = 0101	KP001
E	0110, DSP	1111	CN15	ALU indirect function Q MINUS P (Dec) F register = 0110	KP001
E	0111, SUP	1111	CN15	ALU indirect function Q MINUS P (Bin) F register = 0111	KP001
E	1000, PNQ	1111	CN15	ALU indirect function P AND (NOT Q) ≠ F register = 1000	KP001
E	1001, Q	1111	CN15	ALU indirect function PASS Q ONLY ≠ F register = 1001	KP001
E	1010, XOR	1111	CN15	ALU indirect function Exclusive OR of PO ≠ F register = 1010	KP001
E	1011, QNP	1111	CN15	ALU indirect function PASS (NOT P) and Q ≠ F register = 1011	KP001
E	1100, RSH	1111	CN15	ALU indirect function RIGHT SHIFT Q (Half Q) F register = 1100	KP001
E	1101, LSH	1111	CN15	ALU indirect function LEFT SHIFT Q (2 Q) F register = 1101	KP001
E	1110, DAD	1111	CN15	ALU indirect function P PLUS Q (Dec) F register = 1110	KP001
E	1111, ADD	1111	CN15	ALU indirect function P PLUS Q (Bin) F register = 1111	KP001
E	*	1111	CN15	ALU indirect function SKEW is applied to that function which has an asterisk to the right of it	AQ001

≠ These functions are logic functions and do not alter the YC1 or YCD carry latches
Direct ALU functions affect the direct YCD carry latch
Indirect ALU functions affect the indirect YCI carry latch
'Load F' and 'Use Indirect' may be given in the same cycle in which case the new function can be executed

CP Field

ROS Bits 41-43 PX = 0 (ROS Bit 55) CPU and MX

Sense Latch EB281
Decoder DR431

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ALU Input to P Bus	ALD
A	Z	000	CP0	Zeros, good parity to P and EX ≠	RP001
A	AX	001	CP1	AX to P, zeros to EX	RP001
A	A0	010	CP2	A0 to P, AX to EX	RP001
A	A1	011	CP3	A1 to P, zeros to EX unless CQ = 4 ≠	RP001
A	B0	100	CP4	B0 to P, zeros to EX unless CQ = 4 ≠	RP001
A	B1	101	CP5	B1 to P, zeros to EX unless CQ = 4 ≠	RP001
A	E0	110	CP6	Emit field and 4 zeros (Emit 0000) to P, zeros to EX unless CQ = 4 ≠	RP001
A	0E	111	CP7	4 zeros and Emit field (Emit 0000) to P, zeros to EX unless CQ = 4 ≠	RP001

≠ ALU extension is reset to zero unless CQ = 0100 (C0)

CP Field

PX = 1 (ROS Bit 55) SC only

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ALU Input to P Bus	ALD SC1	ALD SC2
A		000	CP0	Not used	-	-
A		001	CP1	Not used	-	-
A	S0	010	CP2	S0 to P, SX to EX	GE561	HE561
A	S1	011	CP3	S1 to P, zeros to EX	GE561	HE561
A	T0	100	CP4	T0 to P, zeros to EX	GE561	HE561
A	T1	101	CP5	T1 to P, zeros to EX	GE561	HE561
A	CSB	110	CP6	Channel Status byte to P, zeros to EX	GE561	HE561
A	W0	111	CP7	Channel Buffer W0 byte to P, zeros to EX	GE561	HE561

CQ Field

ROS Bits 44–47

Sense Latches EB291
Decoder DR471
Decoder Check DS015

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ALU Input Control to Q Bus	ALD
A	Z	0000	CQ0	Zeros, good parity to Q and EX unless CP = 2	RQ0XX
A	B0	0001	CQ1	B0 to Q, zeros to EX, unless CP = 2	RQ0XX
A	B1	0010	CQ2	B1 to Q, zeros to EX, unless CP = 2	RQ0XX
A	CX	0011	CQ3	CX to Q, zeros in Q0, 5, CX6, 7 ORed to Q6; zeros to EX	RQ0XX
A	C0	0100	CQ4	C0 to Q, CX to EX	RQ0XX
A	C1	0101	CQ5	C1 to Q, zeros to EX unless CP = 2	RQ0XX
A	D0	0100	CQ6	D0 to Q, zeros to EX unless CP = 2	RQ0XX
A	D1	0111	CQ7	D1 to Q, zeros to EX unless CP = 2	RQ0XX
A	E0	1000	CQ8	Emit field and 4 zeros (Emit 0000) to Q zeros to EX unless CP = 2	RQ0XX
A	0E	1001	CQ9	4 zeros and emit field (Emit 0000) to Q zeros to EX unless CP = 2	RQ0XX
A	Y	1010	CQ10	YA and YB stats to Q, zeros to EX unless CP = 2	RQ0XX
A	Data	1011	CQ11	Direct Data to Q, zeros to EX unless CP = 2	RQ0XX
A	CHI	1100	CQ12	Channel Interrupts to Q, zeros to EX unless CP = 2	RQ0XX
A	EXI	1101	CQ13	External Interrupts to Q, zeros to EX	RQ0XX
A	SP	1110	CQ14	CPU Storage Protect key to Q0, 3 MX Channel key to Q4, 7, zeros to EX unless CP = 2 (REINT or ROSCAR in control) Storage Protect bus to Q4, 7 and channel key unless CP = 2 To Storage Protect bus unless CP = 2	RQ0XX
A		1111	CQ15	Not used	

CR Field

ROS Bits 48-50

Sense Latches EB301
Decoder DR501
Decoder Check DR501

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ALU Miscellaneous Controls	ALD
S		000	CR0	No operation	DR501
S	READ	001	CR1	Call Main Storage READ	KM101
S	WRITE	010	CR2	Call Main Storage WRITE	KM101
C	TRAP	011	CR3	TRAP on IMA or (PMA, YM) ≠	KM001
C	IOS	100	CR4	Set I-O State (effective in cycle defined)	DR501
C	CPU	101	CR5	Reset I-O State	DR501
C	0→SK	110	CR6	Reset skew buffer (effective after current use of Skew) Y10 = 0	AQ001
C	0→ERR			Modify by Y10 = 1 to give reset errors	KH141
C	ADCMP	111	CR7	Set Address Compare	KH142

≠ TRAP during READ phase : ROS Address 10100
TRAP during WRITE phase : ROS Address 10101

CS Field

ROS Bit 51

Parity Bit of Current ROS Word to Give an Odd Number of Bits for ROS Word

Sense Latch EB301
S-Field Entry DR601

Edge Char.	Micro-Order	Bits	Dec. Order	Function - ROS Word Parity Bit	ALD
Not applicable		0	-	Odd parity	DR601
Not applicable		1	-	Even parity	DR601

CT Field

ROS Bits 52, 53

Sense Latches EB311
T-Field Entry AM311

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Carry Control	ALD
		00	CT0	No operation	-
C	M	01	CT1	(1401 Emulator only) extend ROS address	RX003
C	0	10	CT2	Reset Carry (Direct or Indirect according to ALU function specified)	AM311
C	1	11	CT3	Set Carry (Direct or Indirect according to ALU function specified)	AM311

Extension Field ROS Bits 54, 55

Edge Char.	Micro-Order	Bits	Dec. Order	Function - Extend Fields J and P	ALD Sense Latch	ALD Decoder
D		54	-	JX Bit Extend J Field (Ref. J Field)	EB311	DR275
A		55	-	PX Bit Extend P Field (Ref. P Field)	EB311	DR431

CYCLING ONE MAIN STORAGE ADDRESS WITH PREDETERMINED DATA

1. Set diagnostic switch to Main Storage Pattern.
2. Set to Stop on ROS 024 Hex.
3. System Reset and Start.
4. Enter 01 in H Register.
5. Turn off Y2.
6. Set Address in A Register.
7. Data to B1. B0 equal to FF.
8. Switch to Process.
9. Start.

CYCLING ALL MAIN STORAGE ADDRESSES WITH PREDETERMINED DATA

1. Set diagnostic switch to Main Storage Address.
2. Set to Stop on ROS 024 Hex.
3. System Reset and Start.
4. Enter 01 in H Register.
5. Set Y0, Y4, and Y5.
6. Data to B0 and B1.
7. Switch to Process.
8. Start.

CLEARING MAIN STORAGE TO ZEROS

Main Storage will be set to zeros if stat Y3 is set before starting the address test diagnostic. The machine will end up with a micro-program stop.

CYCLING ONE LOCAL STORAGE ADDRESS WITH PREDETERMINED DATA

1. Set diagnostic switch to Local Storage pattern.
2. Set to Stop on ROS 029 Hex.
3. System Reset and Start.
4. Set Address to be cycled in H Register.
5. Turn off Y0 and turn on Y4.
6. Set data in C Register.
7. Switch to Process.
8. Start.

SYNC POINTS

1. Sync MS latch -- sync pulse generated when the address on SAB equals the address key contents. A-D3H6-D13 (ALD-KH124)
2. Sync ROS -- sync pulse generated when the address on ROSAB equals the data key contents. A-D3H6-D12 (ALD-KH142)

SYNC POINTS (continued)

3. Sync ROS and MS -- sync pulse generated when conditions 1 and 2 and 2 are both satisfied. A-D3H6-D10 (ALD-KH124)

UTILITY PROGRAM

Card 1 PSW and 2 CCW's
Card 2 Device Exerciser

Program is not relocatable
Cards are punched in EBCDIC card code
Cards are loaded using IPL

Card 1 (Loader)

(PSW)	Card Col 01	01	04	00	00	00	00	0D	08
(CCW1)	Card Col 09	02	00	00	48	80	00	00	04
(CCW2)	Card Col 17	02	00	0D	03	00	00	00	4C

Card 2 (Exerciser)

Card Col 01	00	00	0D	08	00	00	00	00	00	D2
Card Col 11	01	00	4A	0D	24	9C	00	XX	XX	47
Card Col 21	70	0D	0E	9D	00	XX	XX	47	70	0D
Card Col 31	16	47	F0	0D	08	-	-	0D	28	-
Card Col 41	-	YY	00	0D	30	00	00	00	IF	ZZ
Card Col 51	ZZ———		51—	thru—		80—				——ZZ

XX XX is Unit Address

YY is Command Code

ZZ is Data

	Type of Check			
	Early Chk (except LS Rd)	Ctrl Chk	Late Chk	LS Rd Chk MS Protect Key Chk MS Protect Data Chk Stats (Early Chk)
Error detected in Microblock:	A	A	A	A
ROBAR indicates Microblock:	A	A	A	B
ROAR indicates Microblock:	B	B	B	C
Sense Latches set by Microblock:	A	A	B	B

Microblock A — Microblock B — Microblock C

SCOPING WITH CHECK RESTART

Problem: Machine fails on B or C condition branching; conditions are lost using Repeat on ROS.

Solution: If failure is on CPU checkout, use Check Restart. When a machine check is encountered, a machine check interrupt occurs and CPU checkout is again initiated.

Scope Sync: Sync on ROS Addr Compare; check ALD KH101 and KH111 for correct location. Set ROS Addr in data keys of CAS block you wish displayed.

IPL (READ) ROUTINE

Problem: Machine fails either in Mpx channel or in an I/O device but failure does not result in a hardstop.

Solution: Single cycle through IPL to determine problem ahead. If scoping loop is desired, set CAS block address in data keys and use Loop on ROS.

Push IPL. Machine will go through address set in data keys and loop back to start of IPL. Examples follow:

Sync: Scope can be synced on various latches: ADD, ADI, CMO, etc.

Key Addr: Address in Hex

a.	ADO and SLO	5D2
b.	ADI	5E4
c.	CMO	5C9 - Command in C1
d.	STI	57F - Initial sel status

For variations of IPL loops, refer to page 29 of FE Maintenance Manual System/360 Model 40, Form 223-2841.

SIO SCOPING ROUTINE

Problem: Machine fails in Mpx Channel or I/O device on some command other than read. The IPL routine cannot be used.

Solution: Refer to page 28 in Maintenance Manual. Enter program loop "Single Cycling on Mpx Channel", via console keys. If failure is occurring during data service (CPU dumped), Check Restart is necessary to force a machine check interrupt.

Sync: Possible sync points are: MS and ROS Addr Compare, various latches (CMO, STC, etc).

Selector Channel: Consider the SIO sense command loop (Maintenance Manual page 28).

INITIATING A 24-BYTE DATA SERVICE
USING THE CARD READER

1. Stop on ROS at 6F9.
2. IPL the card reader; -- machine will stop at 6F9.
3. Single cycle through data service. Data can be seen in C1 when SVI goes off; the main storage address is in the storage address lights.
4. Return to Process Mode.
5. To read another card, push IPL.

DATA SERVICE USING THE 1052

1. Set the load unit rotary switches to the address of the 1052.
2. Stop on ROS address 554.
3. Press load key.
4. When CPU stops at address 554, alter the CCW (in main storage 0000 - 0007) to the following:
   0000 = 0Ä
   0000 - 0003 = Main storage address where data is to be stored
   0006 - 0007 = Byte count of data to be entered from 1052 (hex 84 = decimal 132)
5. Depress START.
6. When PROCEED lights on 1052, enter data. If data is to be printed on the 1403, enter only characters that the 1403 can print.

STOP AT BEGINNING OF START I/O MICROPROGRAM

1. Stop on ROS with 555 in data keys.
2. AND ROS Address Stop with Main Storage Address Stop (SIO instruction address).

REWIND TAPES FROM CONSOLE

1. IPL Device with ROS Stop at 44C.
2. Record contents of D Register.
3. Store 07 (Hex) at MS Addr 0000.
4. Restore D register.
5. Push START.

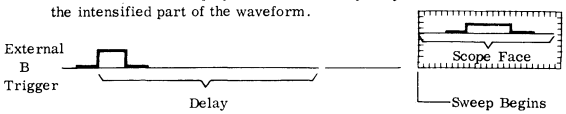
MULTIPLE-ENTRY CAS BLOCKS

Some CAS blocks in CPU checkout are used several times. Failure in a CAS block is not limited to the first time it is used. To determine in which loop it occurs Stop on ROS at the suspected address and single-cycle through it. If no error occurs, return rat(switch to PROCESS and push START. Continue this routine until it is determined in which loop the suspected CAS block fails.

OSCILLOSCOPE DELAYED SWEEP

Usual method: Sweep occurs at the end of the delay.

1. Connect the external sync to time base B.
2. Set the horizontal display control to B intensified by A.
3. Turn the A time base stability-triggering level controls fully clockwise.
4. Adjust the time base B stability-triggering control in the normal manner for a trace.
5. Adjust the time base A time/cm control and the delay time multiplier until the desired part of the waveform is intensified. (Make certain time base B is greater than time base A.)
6. Set the horizontal display control to A delayed by B to see the intensified part of the waveform.

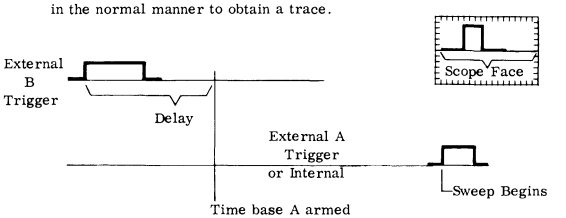


Occasionally, when the usual method is used, a jittery trace or unstable waveform on the scope results. In these instances another sync method may be used to stabilize the trace.

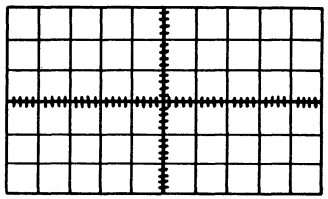
Jittery trace method: double sync is used.

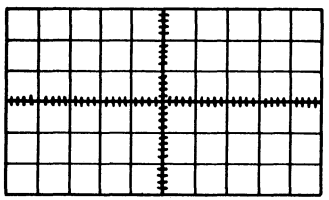
The sweep occurs as a result of a time base A triggering pulse, internal or external, after the time base B delay is completed.

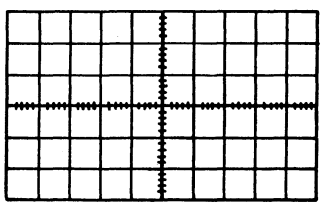
1. Set up the scope as in the usual method.
2. Connect the second external trigger to the time base A trigger input and, if external trigger is used, set the triggering mode control to external; if not, set the triggering mode control to internal.
3. Adjust the time base A stability-triggering level control in the normal manner to obtain a trace.

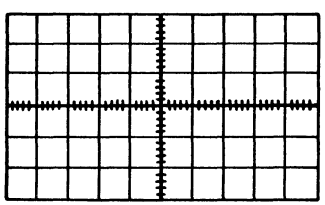


Use these reticules to save important or unusual pulses for future reference.

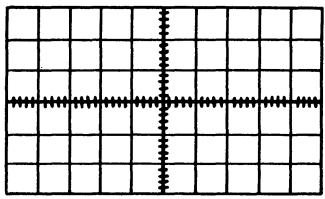


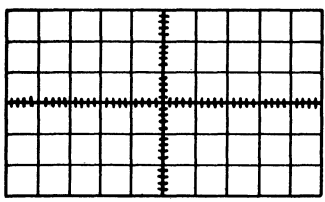


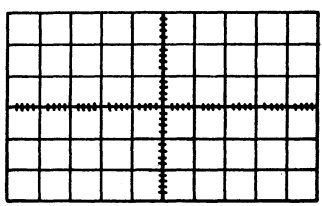


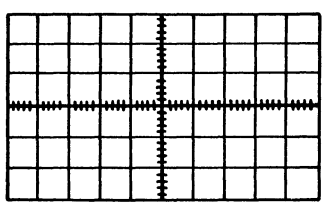


Use these reticules to save important or unusual pulses for future reference.

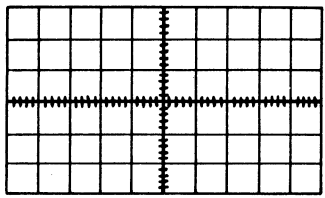


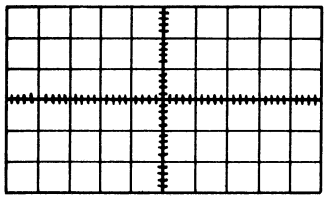


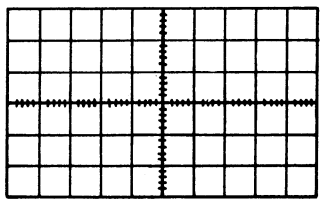


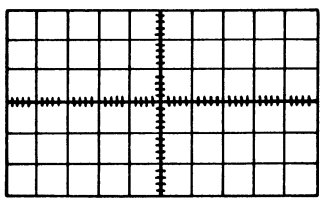


Use these reticules to save important or unusual pulses for future reference.



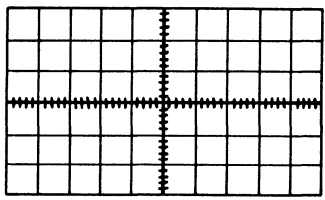


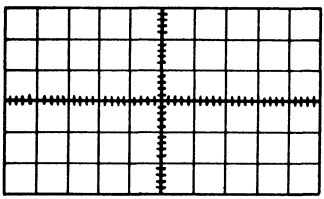


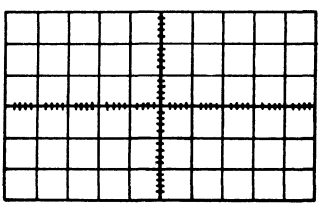


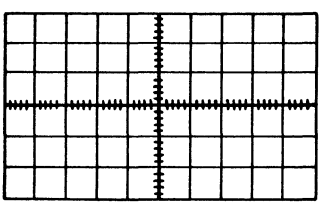
SCOPE NOTES

Use these reticules to save important or unusual pulses for future reference.

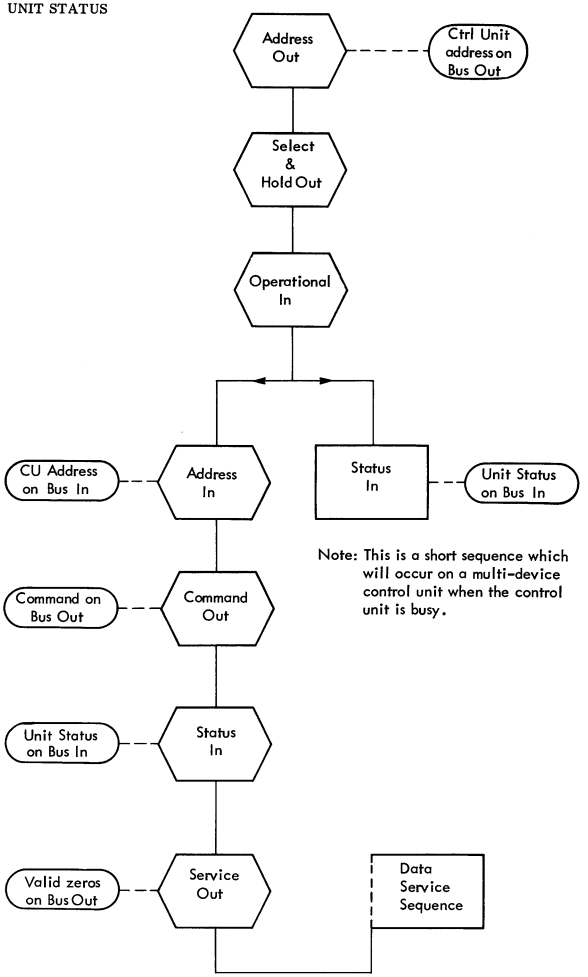






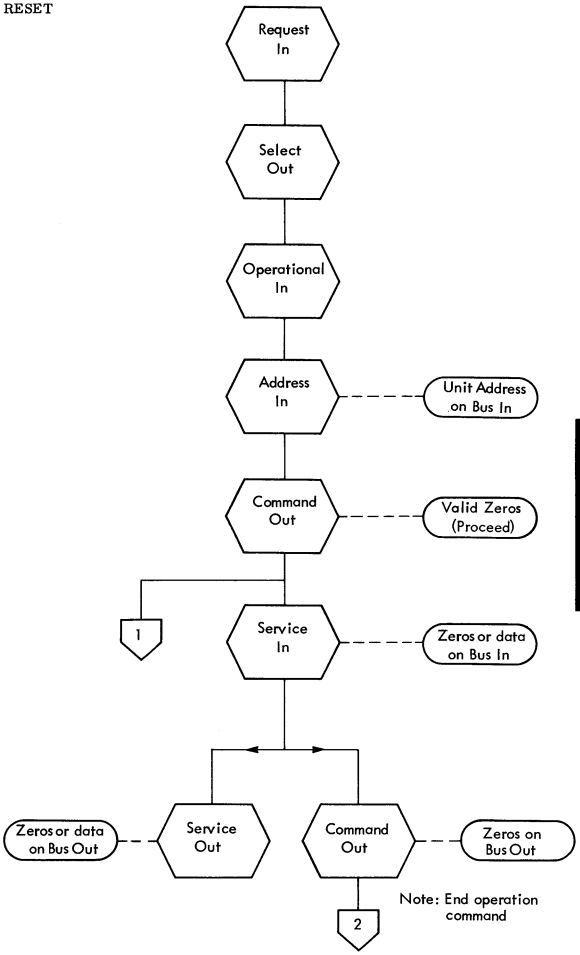


INITIAL SELECTION
UNIT STATUS

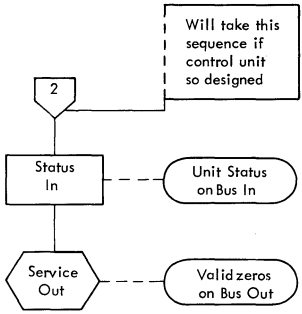


Note: This is a short sequence which will occur on a multi-device control unit when the control unit is busy.

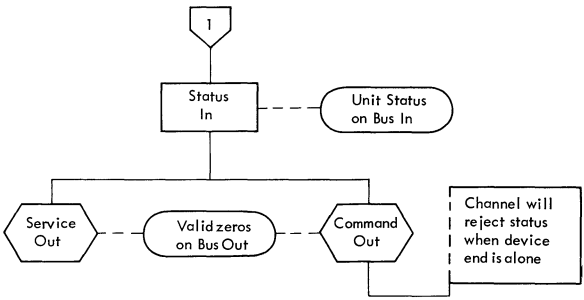
DATA SERVICE (MULTIPLEX OPERATION)
ENDING SEQUENCES
RESET



A. From Command Out

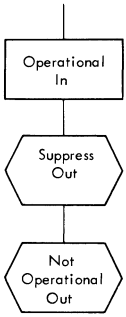


B. Normal Ending

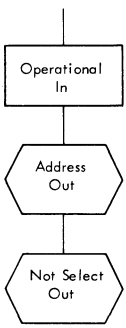


RESET

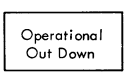
A. Selective Reset



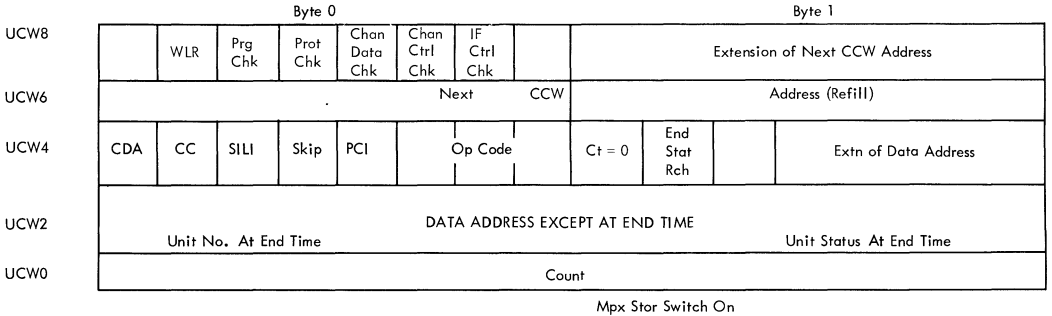
B. Interface Disconnect (Halt I/O)



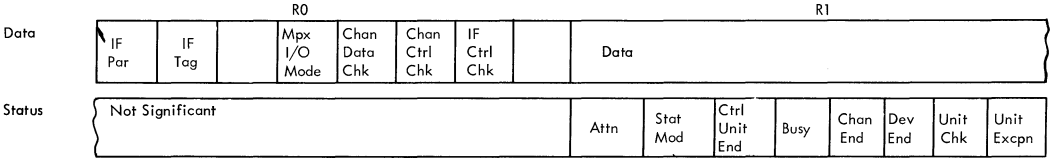
C. General Reset



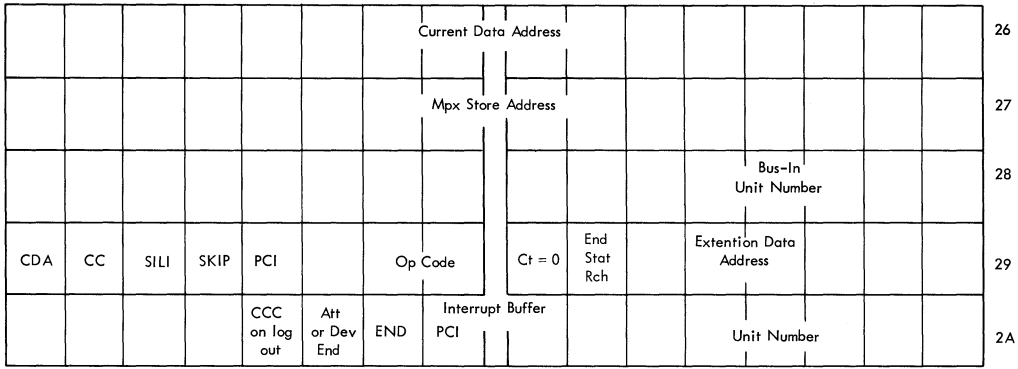
Unit Control Word in Multiplex Storage



R Bus Format for Multiplex Channel Operations



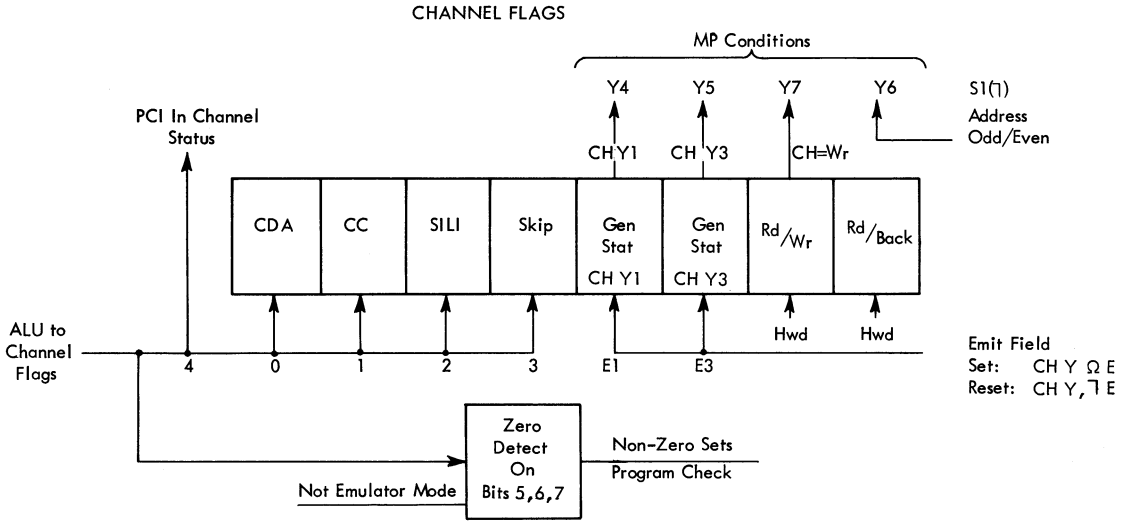
Mpx Local Storage Working Space

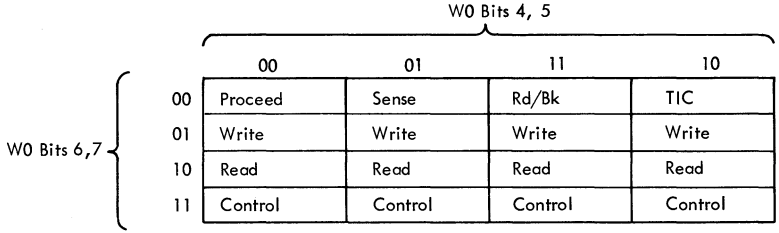


Op Codes

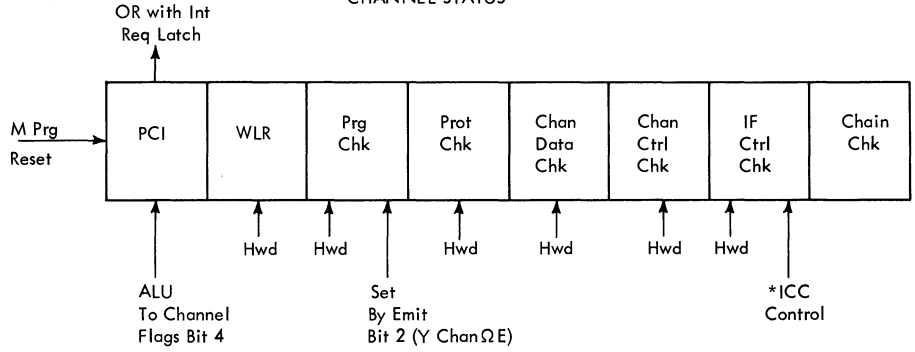
010	Write or Control
100	Read or Sense
101	Read Backwards
110	Read Skip
111	Read Back Skip

FORMATS

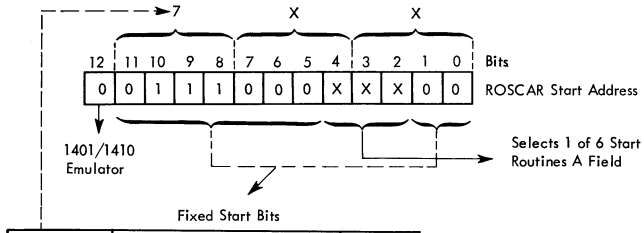

CHANNEL FLAGS
MP Conditions
Y4
Y5
Y7
Y6
S1(1)
Address
Odd/Even
PCI In Channel
Status
CH Y1
CH Y3
CH=Wr
CDA
CC
SILI
Skip
Gen
Stat
CH Y1
Gen
Stat
CH Y3
Rd/Wr
Rd/Back
Hwd
Hwd
ALU to
Channel
Flags
4
0
1
2
3
E1
E3
Emit Field
Set: CH Y Ω E
Reset: CH Y, ⌐ E
Zero
Detect
On
Bits 5,6,7
Non-Zero Sets
Program Check
Not Emulator Mode



CHANNEL STATUS



FORCED START ADDRESS



Hex Addr	Channel Routine	CAS
700	1 Byte Data Service	QB401
704	2 Byte Data Service	QB411
708	Terminal Status In	QB511
710	Status In After Addr In	QB451
71C	Skip and Count > 1	QB421
718	Skip and Count = 1	QB421

DATA IN LOCAL STORE

		SC1	SC2
0	Dump A Register (Chaining)	20	30
1	Dump D Register	21	31
2	Refill CCW Address	22	32
3	Refill CCW Addr on Write	23	33
4	0—5 ZEROS | 6 7 Flags | 0——7 Unit No.	24	34
5	Working Space	25	35

Codes		Sub-Channel
0	0	Free
0	1	Hwd Error Interrupt
1	0	Busy
1	1	Interrupt Pending

Multiplex Channel Error Checking

IF Tag	IF Ctrl	IF Pty	Chan Data	Chan Ctrl	Cause of Error
X	X			X	More than one In or Out tag or tag sequence check
	X			X	Time Out, unit failed to respond in time or raised an incorrect tag
	X	X		X	Parity check on Bus-in caused by address in or status in
		X	X	X	Parity check on Bus-in caused by service in
				X	Any CPU check occurring while the microprogram and data flow are being used as a Mpx Channel

Selector Channel B Error Checking

IF Tag	IF Ctrl	Bfr Data	Chan Data	Chan Ctrl	
X	X				More than one In tag
X				X	More than one Out tag
	X	X	X		W0 parity error
			X		Bus-in parity
				X	CPU check while CPU is being used by selector channel
				X	T or flag register parity
	X				Set by microprogram

Notes

CUT ALONG DOTTED LINE

IBM Field Engineering Handbook, System/360--Model 40, Form Z22-2852-2

From _____ Office No. _____

Circle one of the comments and explain in the space provided:

Suggested Addition (page ___) Suggested Deletion (page ___) Error (page ___)

Explanation:

Suggestions from IBM employees giving specific solutions intended for award considerations should be submitted through the IBM Suggestion Plan.

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