Diagnostic Engineering Publication

IBM POUGHKEEPSIE
April 15, 1964

1410/7010

Subject: Diagnostic Program CS43C, CS44B, and CS46B
1410 Memory Reliability Tests

Sequence Number 125 (CS43), 127 (CS44), 129 (CS46)
Replaces CS43B, CS44A, and CS46A

These programs require system control cards only.

* 235 Pages

Release Sheet:	1	
Writeup:	44	(Common to all three)
Summary:	4	(Common to all three)
Listing:	66	(CS43C)
Listing:	58	(CS44B)
Listing:	62	(CS46B)

** 353 Cards No. 001-353 (CS43C)
300 Cards No. 001-300 (CS44B)
319 Cards No. 001-319 (CS46B)

This release covers a correction to CS43 only. An error existed in the 60K test section causing an address above 59999 to be used. CS44 and CS46 remain unchanged and are therefore not re-released.

Enclosures: * Pages
Card Deck for CARD ONLY SYSTEMS (as punched by UP51)
8 Cards-Card Loader (1-7) and 1 Core Clear
** Cards No. Data Cards
1 Card Execute Card

Distribution: X 1410 with 40K, 60K, 80K or 100K memory only.
7010
Other

CS43C
CS44B
CS46B

1410 MEMORY RELIABILITY TESTS

April 15, 1964

CONTENTS OF THE CS-- SERIES

2.01.00.0 TEST DESCRIPTION

00.1 MODIFICATIONS

This release obsoletes and replaces CS43A, CS44A, and CS46A.

00.2 DESCRIPTION

The purpose of these programs is to provide a comprehensive test of the 1411 Memory hardware with emphasis on a clear presentation of Memory failures in the 1410 system.

This Memory Test package is released as three programs. Only two of these three are required for checking upper and lower Memory of any one 1410 model 3, 3A, 4, 4A, 5, 5A, or 100K installation.

CS43 - Tests upper Memory and is capable of being used on any of the following four sizes: 40K, 60K, 80K, or 100K.

CS44 and CS46 - Test lower Memory and are designed to be used on and test 40K, 60K and/or 80K and/or 100K Memories, respectively.

For reference -

Program	Model Size For Which Designed	Resident Location	*Objective Test Area	*Memory Size Digit
CS43	3, 4 or 5 or 100K	00001-19999	20000-39999	3
			40000-59999	5
			40000-79999	7
			40000-99999	9
CS44	3 (40K)	20000-39999	00001-19999	3
CS46	4 (60K) or 5 (80K) or (100K)	40000-59999	00001-39999	5, 7, or 9
			00001-19999	3

* See Operating Hints and Comments, 2.01.03.1.

2.01.00.0 TEST DESCRIPTION (Cont'd)

Each program proceeds automatically to run a series of nineteen tests of Memory function. It starts the sequence with a simple "ones" discrimination test and proceeds through graduated complexity tests of alternate plane discrimination, "checkerboard" discrimination, complemented checkerboards, and finishes with half-select core beat tests.

The programs assume that the central processing unit and the instructions sets are functioning normally.

Each of the nineteen tests, called Sections, are described as follows:

Section 1 Ones Discrimination - This test checks the ability of Memory to set "all" bits on. Character patterns of group marks (CBA8421 bits up, word mark bit down) are loaded into all O.T.A. (Objective Test Area) addresses and checked for correct set.

Characters used: ‡,(---‡)

Section 2 Zeros Discrimination - This test checks the ability of Memory to reset "all" bits off. Character patterns of word mark blanks (CBA8421 bits down, word mark bit up) are loaded into all O.T.A. addresses and checked for correct set.

Characters used: v̄,(WMBL)

Section 3 Alternate Plane Discrimination - This test checks for any interaction between adjacent planes by loading and checking character patterns which set alternate bit planes to one and remaining planes to zero.

Characters used: V̄,(WM-V)

Section 4 Alternate Plane Discrimination - Reserved - This test is the complement of Section 3 in that alternate plane set characters are inverted, loaded and checked.

Characters used: !,(---!)

2.01.00.0 TEST DESCRIPTION (Cont'd)

Section 5 Memory Address Placement - This test loads five position numeric addresses at XXXX4 and XXXX9 addresses in Memory and checks that each is correctly stored. This section is a test to determine whether all objective test area positions can be selectively loaded and addressed.

The next twelve sections attempt to exert worst case condition. Each is described as employing a checkerboard. This is simply a descriptive term for the method in which data bit patterns are arranged physically within the boundaries of the X and Y axis of the first bit plane. The arrangement is made with prime consideration of the physical location per address of the paired sense line windings. The remaining bit planes are set to minimize or maximize interplane noise in one of three ways down through the array: alternately on and off in pairs (2D), all on or all off (In-Line), or alternately on and off (Alternate). (See Appendix A)

Section 6 Two-Dimensional Plane Checkerboard Discrimination - This test loads and checks the basic X-Y checkerboard with data bits set alternately on and off in pairs.

Characters used: ¥C, (WM-C) and @, (---@)

Section 6C Two-Dimensional Plane Complemented Checkerboard - Using the pattern load set from Section 6, this test complements one character at a time and checks it and its corresponding in-line address contents for error-free regen set and inhibit after read-out.

Section 7 Two-Dimensional Plane Checkerboard Discrimination - Reversed - This test is the complement of section 6 in that the checkerboard is inverted, loaded and checked.

Characters used: @, (---@) and ¥C, (WM-C)

Section 7C Two-Dimensional Plane Complemented Checkerboard - Reversed - Using the pattern load set from Section 7 this test is virtually the same as Section 6C.

2.01.00.0 TEST DESCRIPTION (Cont'd)

Section 8 In-Line Plane Checkerboard Discrimination - This test loads and checks the checkerboard with data bits arranged in-line (e.g., all bits up or all bits down).

Characters used: ‡ , (---‡) and $\overset{V}{b}$, (WMBL)

Section 8C In-Line Plane Complemented Checkerboard - Using the pattern load set from Section 8, this test is virtually the same as Section 6C.

Section 9 In-Line Plane Checkerboard Discrimination - Reversed - This test is the complement of Section 8 in that the checkerboard is inverted, loaded and checked.

Characters used: $\overset{V}{b}$, (WMBL) and ‡, (---‡)

Section 9C In-Line Plane Complemented Checkerboard - Reversed - Using the pattern load set from Section 9, this test is virtually the same as Section 6C.

Section 10 Alternate Plane Checkerboard Discrimination - This test loads and checks the checkerboard with data bits arranged alternately set to one and zero.

Characters used: $\overset{V}{V}$, (WM-V) and !, (---!)

Section 10C Alternate Plane Complemented Checkerboard - Using the pattern load set from Section 10, this test is virtually the same as Section 6C. t

Section 11 Alternate Plane Checkerboard Discrimination - Reversed - This test is the complement of Section 10 in that the checkerboard is inverted, loaded and checked.

Characters Used: !,)---!) and $\overset{V}{V}$, (WM-V)

2.01.00.0 TEST DESCRIPTION (Cont'd)

Section 11C Alternate Plane Complemented Checkerboard - Reversed - Using the pattern load set from Section 11, this test is virtually the same as Section 6C.

Section 12 Half Select Core Beat - All Ones - This test is designed to check all objective test area bit cores exposed to sustained half select for "resistance" to status change. The test is executed by resetting all OTA characters to word mark-blanks, then "beating" a specific address or addresses with group marks (all ones) for an extended length of time. Upon completion of the specific number of beats (1000 as released), each bit of each character of each address along the X and Y line involved in the beat operation is interrogated for bit pickup. This operation is repeated 99 times in order to check all objective test area X and Y lines.

Characters used: $\overset{v}{b}$, (WMBL) and ‡, (---‡)

Note: If desired, the number of beats may be increased to any value up to 99999. To modify this counter, see Operating Hints and Comments, 2.01.03.5.

Section 13 Half Select Core Beat - All Zeros - This test is the complement of Section 12 in that the OTA characters are set to group marks, beating is done with word mark-blanks (all zeros), and interrogation is made for bit dropout.

Characters used: ‡, (---‡) and $\overset{v}{b}$, (WMBL)

Upon completion of each section, a short typeout (s-01, S-02, S-03 . . . . S-13) is executed to provide visual verification of the intended sequence of test operation.

2.01.00.0 TEST DESCRIPTION (Cont'd)

00.3 EQUIPMENT (Area of Machine Required)

Units - 1411 Model 3, 3A, 4, 4A, 5, 5A or special 100K
Processing Unit
Card or Tape Input capabilities
Typewriter and/or Printer Output capabilities
See Operating Hints and Comments, 2.01.03.6
for Tape Output Capabilities.

Memory Locations -
CS43 - Resides in 00001-19999 area.
CS44 - Resides in 20000-39999 area.
CS46 - Resides in 40000-59999 area.

00.4 CARD DECK

Each of the CS tests use standard seven-card L1 loaders, a core clear card, and one execute card.

Program Test Cards: (as punched out by UP51)

CS43 - 353
CS44 - 300
CS46 - 319

00.5 EC LEVEL OF MACHINE

None Applicable.

2.01.01.0 LOADING PROCEDURES

In all cases, the following CPU console switches should be set as follows during program loading:

Check Control Switch - Normal
Print Control Switch - Normal

01.1 CARD

Load Program Deck(s) in Reader.
Depress Start Button.
Depress End of File Button.

Clear Memory from console.
Set Mode Switch to Display.
Depress Start.
Enter Address 00000.
Set Mode Switch to Alter.
Depress Start.
Enter RL%1100011$. (Channel 1)
Set Mode Switch to Run.
Depress Computer Reset.
Depress Start.

01.2 TAPE

Use Program tape file generated by TC50.
Place file-protected tape on Drive No. 0 of Channel 1.

Clear Memory from console.
Set Mode Switch to Display.
Depress Start.
Enter Address 00000.
Set Mode Switch to Alter.
Depress Start.
Enter RL%B000011$. (Channel 1)
Set Mode Switch to Run.
Depress Computer Reset.
Depress Start.

2.01.02.0 OPERATING PROCEDURES

These programs may be executed in either of two Check Control modes: Normal or Restart. The recommended conditions under which each mode should be used are as follows:

Normal - During Scheduled Maintenance time and/or prior to execution test runs of CPU reliability and error-detection programs.

* See also Operating Hints and Comments, 2.01.03.10.

Restart - When exclusive memory errors are known to exist or suspected.

02.1 NORMAL CHECK CONTROL MODE

Console Switch Setting:

Check Control Switch - Normal
Print Control Switch - Normal

This mode is prescribed for post-power-on usage since either a CPU and/or Memory failure will cause an immediate fail-safe machine halt.

If from the standard "E" stop printout it can be ascertained that the error was a definite or suspected Memory failure, the program should be computer reset and started again. If CPU trouble appears evident, load the CPU programs. If in doubt, try again.

02.2 RESTART CHECK CONTROL MODE

Console switch settings:

Check Control Switch - Restart
Print Control Switch - Inhibited

This mode is prescribed for usage during periods when exclusive memory failures are known or suspected so that data error stops

2.01.02.0 OPERATING PROCEDURES (Cont'd)

can be bypassed. In this way, the program is allowed to compile and indicate an uninterrupted overall analysis as to the what, where, how many, and frequency of errors within the objective test area of Memory.

Note: Known or suspected "C" bit pick or drop failures will not be detected by either the standard "E" stop printout or the program's standard Immediate Error Indication printout while the machine is set to this mode, unless a "C" bit checking facility is installed. If this "C" bit checking facility is not available, set the Print Control Switch to Normal, so that at least "E" stop printouts are executed.

2.01.02.0 OPERATING PROCEDURES (Cont'd)

02.3 TEST ALTERATION DIGIT SWITCHES (TADS)

TADS are addressable character positions in Memory which when loaded with a numeric one (1) cause the program to perform a specific added and/or special function.

Each TAD function, when set to 1, is as follows:

TAD 0	Bypass Normal and Error Typeouts	01000	21000	41000
TAD 1	Repeat Section	01001	21001	41001
TAD 2	Halt on Error (not used in the CS series)	01002	21002	41002
TAD 3	Repeat Program	01003	21003	41003
TAD 4	Automatic Section Selection	01004	21004	41004
TAD 5	Suppress Tabulation of Errors	01005	21005	41005
TAD 6	Error Table Output	01006	21006	41006
TAD 7	Print Immediate Errors and Table on Printer	01007	21007	41007
TAD 8	Bypass Sections 6-11 Discrimination	01008	21008	41008
TAD 9	Bypass Sections 6C-11C Complements	01009	21009	41009
TAD 10	Repeat Error Address	01010	21010	41010
TAD 11	Not Used	01011	21011	41011
TAD 12	Bypass Stack Regen Check	01012	21012	41012

TAD's 0-3 maintain standard function compatibility with all other new format 1410 diagnostic programs. TAD's 4-12 are functions exclusive to the CS series memory tests. See Operating Hints and Comments, 2.01.03.2.

During normal mode operation, all TADS should be set to a not 1 state. This scheme is based on the premise that if no errors are encountered or known to exist, no TAD functions are required.

Any TAD can be set to 1 or reset to Not 1 using the simple and efficient Standard Internal Program Alter Routine.

2.01.03.0 OPERATING HINTS AND COMMENTS

03.1 MEMORY SIZE AND OBJECTIVE TEST AREA DESIGNATION

The Standard System Control Card contains a location reserved for the memory size, or more appropriately, the objective test area limit designation. This location must be entered and is specified by a single numeric digit. The program interrogates this digit periodically and sets its own limits as to how much memory it is to test.

The specific digits used to designate each size and/or objective test area are as follows:

3 = 40K, one 20K OTA Block
5 = 60K, one or two 20K OTA Blocks (CS43, one - CS46, two)
7 = 80K, two 20K OTA Blocks
9 = 100K, two or three 20K OTA Blocks (CS43, three - CS46, two)

Note 1 - Bear in mind that 1410 memories, larger than 40K, are composed of two distinct arrays. The first 40K is located in the B frame. The remaining 20K or 40K or 60K portion is in the Z frame. With reference to the table on Page 003, notice that CS43 resides in the B frame and has four optional operating modes: 40K, 60K, 80K, and 100K. When set to 40K mode, it checks the upper half of the B frame. But when set to 60K, 80K or 100K mode, the Z frame only is tested. Conversely, CS46 resides in the Z frame and tests the B frame only. This scheme of operation is known as the "remote bank test method" and is quite effective for checking 1410 memories larger than 40K.

Note 2 - CS 43 and CS44 must not specify a memory size digit greater than the memory size on which the program is used.

As an example, CS43 used on a 40K system must specify a digit 3 only. If a 5, 7, or 9 were used, the program would be stopped immediately by a B Channel check.

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

If the memory size digit is to be set from the Control Card, punch a 3, 5, 7, or 9 in column No. 14 of program test deck card No. 001.

If the memory size digit is to be set or changed while the program is in memory, display and alter the location as desired within each program at the following locations:

For: CS43 - 01257
CS44 - 21257
CS46 - 41257

03.2 EFFECTIVE TAD USAGE

TAD 0 - Bypass Typeouts

This TAD, when set to a 1, will suppress all Immediate Error and Section Complete Indications. Standard program entrance and exit messages and program misusage messages will not be affected by TAD 0. This TAD can be effective in reducing execution time for a large quantity of error indications and for eliminating interruptions of scope tracing.

Note: TAD 6, set to 1, over-rides TAD 0 and allows section complete indications.

TAD 1 - Repeat Section

This TAD, when set to a 1, will permit constant repetition of any section within the program. It can be effective for locking the test within any specific section, thereby providing closer observation of solid and/or intermittent error conditions. See Section Repetition, 2.01.03.4.

TAD 2 - Halt On Error

This TAD is not used within any of the CS series programs.

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

TAD 3 - Repeat Program

This TAD, when set to a 1, will cause the program to repeat the entire sequence of section tests following the completion of Section 13.

TAD 4 - Automatic Section Selection

This TAD, when set to a 1, allows immediate entrance to any specific section within the program. It is particularly effective as a time saver since it bypasses the necessity of executing any and all sections that lie sequentially ahead of the section desired.
See Selection of "C" Sections, 2.01.03.3.

TAD 5 - Bypass Tabulation of Errors

This TAD, when set to a 1, suppresses the normally unconditional recording of errors into the Error Frequency Table. This TAD is quite effective as a time saver when table recording is not desired and when the prime consideration is to remove as many interrupting peripheral program operations as possible during scope tracing.

TAD 6 - Error Table Output

This TAD, when set to a 1, causes the Error Frequency Table to be printed upon the completion of each Section. The function of this TAD is particularly effective for providing an overall picture of what is failing and where since it shows a complete frequency distribution of recorded errors.*

* See Error Frequency Table, 2.01.05.4 and 2.01.05.5.

TAD 7 - Table and Errors on Printer

This TAD, when set to a 1, causes all Immediate Error Indications and the Error Frequency Table to be sent to an on-line ready printer. This TAD is an extremely effective time saver for obtaining "instantaneous" output of immediate error indications

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

and/or the summary table. If and when this TAD is set, an internal program routine inspects the Standard System Control Card for both a Channel 1 or 2 designation and the printer's appropriate Buffer size. If it finds neither specified, a message to this effect will be executed and the output information will be sent to the console typewriter instead. Also, if this TAD is set and the printer is not ready or not on line, the program will "hang". See Tape Output, 2.01.03.6.

TAD 8 - Bypass Discrimination Sections 06, 07, 08, 09, 10, 11

This TAD, when set to a 1, causes each of the discrimination sections to be bypassed. This TAD can be helpful for savings program execution time if discrimination sections are error free. This special purpose TAD allows closer concentration on the "C" (Complement Checkerboard) sections which by their very nature are more complex and exert more stress on memory than do the discrimination tests. Another effective function of this TAD is that of allowing immediate entrance to and/or repetition of any exclusive "C" section if TAD 4 and /or TAD 1 are set to 1.

TAD 9 - Bypass Complement Checkerboard Sections 06C, 07C, 08C, 09C, 10C, 11C

This TAD, when set to a 1, performs just the opposite function to TAD 8. All of the "C" sections are bypassed. This special function may be used for closer concentration on errors detected within the discrimination sections so that repetition of a section can be held within the discrimination segment only.

TAD 10 - Repeat Error Address

This TAD, when set to a 1, causes an infinite repetition (until manually stopped) of a single character data move into the first encountered address found to have contained a bit pick or drop error. This function permits a programmed execution of the tightest loop available within the CS tests and may be quite effective for line checking at time of error detection.

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

TAD 11 - This TAD has no assigned function.

TAD 12 - Bypass Stack Regen Check

This TAD, when set to a 1, suppresses the normal post-complement regen check of all in-line characters not involved in the complement operation. This function is extremely effective in reducing execution time for each of the "C" sections. This, in turn, is most helpful for shortening execution time while deriving limits during "schmoo" curve plotting.

03.3 AUTOMATIC SECTION SELECTION

To select any Section -

Set TAD 4 to a 1.
Reset and restart the program.
Wait for message, AUTO SECT SEL
ENTER 2 DIGIT SECTION #
Depress Inquiry.
Enter two numeric digits corresponding to the Section desired (e.g., 04, 08, 13, etc.).
Depress Inquiry Release.

To select an exclusive "C" section -

Set TAD 4 and TAD 8 to a 1.
Repeat same procedure as above.

03.4 SECTION REPETITION

To repeat any Section -

Set TAD 1 to a 1.

To repeat any one of sections 06, 07, 08, 09, 10 or 11 exclusively -

Set TAD 1 and TAD 9 to a 1.

To repeat any one of sections 06C, 07C, 08C, 09C, 10C or 11C exclusively -

Set TAD 1 and TAD 8 to a 1.

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

03.5 BEAT COUNTER FOR SECTIONS 12 AND 13

The number of "beats" each address receives in Section 12 and 13 has been preset at a specific location to a nominal value of 01000.

This count may be increased to any value up to 99999 if desired. The location of this counter within each program is as follows:

For:	CS43,	19490-19494
	CS44,	36804-36808
	CS46,	57736-57740

03.6 TAPE OUTPUT OF ERROR TABLE AND IMMEDIATE ERRORS

It is recognized that there may be some 1410 installations not equipped with printers on line. In view of this possibility and in consideration of saving valuable machine time for error output, the following changes may be made directly to the CS series programs to allow this output to be sent to tape as an alternate to the printer.

The Immediate Error Indications for all Sections (except Section 05) are written from one location, and the Error Frequency Table from another.

In order to keep changes to a minimum, the specifications of channel and buffer size could be designated in the same manner and location on the Standard System Control Card as is done for printer output.

This leaves only the tens and units order of the X control field for each of the two write instructions requiring a change. The tens order, since it specifies the type of output unit, must be changed from a "2" (for printer) to a "U" or a "B" (for tape). The units order of the X control field may be changed to any tape drive number. If left unchanged, the output would be sent to Tape Drive No. 0.

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

The location of the tens and units order of the X control field for the Immediate Error Indication write to printer instruction within each program is as follows:

For:	CS43,	05190-05191
	CS44,	24495-24496
	CS46,	44682-44683

The location of the tens and units order of the X control field for the Error Frequency Table write to printer instruction within each program is as follows:

For:	CS43,	08125-08126
	CS44,	27118-27119
	CS46,	47413-47414

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

03.7 ERROR-FREE EXECUTION TIME PER SECTION

Timings: Apply to all programs.
Are given in seconds.
Are approximate observed durations as taken on a 1410 ACC.
For Sections 06C, 07C, 08C, 09C, 10C and 11C are reduced by about 65 per cent when TAD 12 is set to a 1,in 60K, 80K, and 100K mode.

Section	40K Mode	60K Mode	80K Mode	100K Mode
S-01	16	Same	32	60
S-02	16	as	32	60
S-03	16	40K	32	60
S-04	16	Mode	32	60
S-05	5	(For	10	12
S-06	16	CS43)	32	60
S-06C	62		180	250
S-07	16		32	60
S-07C	62		180	250
S-08	16		32	60
S-08C	62		180	250
S-09	16		32	60
S-09C	62		180	250
S-10	16		32	60
S-10C	62		180	250
S-11	16		32	60
S-11C	62		180	250
S-12	65		98	150
S-13	65		98	150
Approx. Totals	11'20"		27'	

Note: CS46 timings for modes greater than 40K correspond in all cases to those specified under 80K, mode.

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

03.8 SELECTIVE OTA (Objective Test Area) BLOCK CHECKING

The CS series tests are written to check one, two, or three 20K objective test area blocks of memory contingent upon the program used, the memory size available, and the memory size digit specified.
(See Reference Table in Test Description, 2.01.00.2).

It has been anticipated that there may be occasions when the operator may desire to concentrate memory checking upon a specific 20K block in the array other than those normally capable of exclusive objective testing. Employing the following change with the appropriate program, memory size available, and memory size digit allows completely selective and exclusive checking of any 20K block in the objective test area.

The upper and lower memory tests use a standard objective test area "starting address" of 20000 or 40000 and 00000, respectively. By changing two single digit constants within the program, the OTA starting address for CS43 may be changed from 40000 to 60000 or 80000. The OTA starting address for CS46 may be changed from 00000 to 20000.

See Table Guide on next page.

2.01.03.0 OPERATING HINTS AND COMMENTS (Cont'd)

Since the previously described changes are not applicable to all programs and memory sizes, the following is a tabulated guide to the Permissible Change Options and the 20K block that will be checked as a result of the change.

Program	40K Mode *MSD = 3	60K Mode MSD = 5	80K Mode MSD = 7	100K Mode MSD = 9
CS43	** X	X	6- (60000-79999)	8 - (80000-99999)
CS44	X	X	X	X
CS46	X	2 - (20000-39999)	X	X

*MSD = Memory Size Digit

**X = No Change Options Permissible

A few examples of application are as follows:

Program Used:	CS43
Memory Size Available:	80K
Normally Checks:	20000-39999 if MSD = 3
	40000-59999 if MSD = 5
	40000-79999 if MSD = 7
	40000-99999 if MSD = 9
Desire to Check:	60000-79999 only
Set MSD:	to a 7_y
Change Constants:	from $\overset{y}{4}$ to $\overset{y}{6}$

Program Used:	CS46
Memory Size Available:	60K or 80K or 100K
Normally Checks:	00001-19999 if MSD = 3
	00001-39999 if MSD = 5
Desire to Check:	20000-39999 only
Set MSD:	to a 5
Change Constants:	from $\overset{y}{0}$ to $\overset{y}{2}$

2.01.03.0 OPERATING HINTS AND COMMENTS (continued)

The two single digit constants reside in the following locations within each program:

For CS43 - 15966 and 16017

For CS46 - 54554 and 54593

Summary notes of importance -

a. Do not attempt to make use of this special purpose function unless it is thoroughly understood.

b. The described changes are applicable to 60K, 80K, and 100K memory installation usage only and are effective only when executing Sections 01-04 and 06-11C.

c. Do not punch changes to the constants directly into the program deck. These changes should be made on a manual basis only and used only when Memory problems are observed to be localized to a specific area or special purpose bias checking is being performed.

03.9 "SCHMOO" CURVE PLOTTING

The worst case Sections 06 through 11C are the most effective to use for this purpose. Before plotting, run one complete error-free program pass at nominal voltage in Normal Mode. Then, employing the automatic section selection feature, start the execution sequence at Section 06 or 08 or 10 and let run through 11C. If error free, raise or lower X-Y voltage as required, reset program, and repeat execution sequence. Continue this procedure until error-free voltage limit is reached.

Note: TAD 12 may be used here to substantially reduce the execution running time of the "C" sections.

03.10 "QUICK RUN" MODE

This new feature has been included in order to provide a very simple but effective test of very short duration so that a certain level of confidence can be had on the selectivity & accessibility of all of the objective test area of memory.

This mode is called for by manual input of a $ (Dollar Sign) following the typeout "OPTION?" during TC50 Diagnostic Tape Input Control. (SEE TC50 WRITEUP FOR DETAILS.) The Dollar Sign sets up conditions which, when recognized by each memory program, cause Section 05 only to be executed. This is particularly effective as a time saver for a quick and simple memory check.

Note: This mode uses Section 05 alone and checks only for correct address selection and placement of numerical data. Only a full run of all sections will subject memory to the full spectrum of varied character and worst case conditions.
If memory trouble is definite or suspected, run the entire test. Do not enter Quick Run Mode only.

Typical typeouts during Quick Run Mode if error-free:

```
CS43B
TESTS 40000-79999  AREA OF
80K MEMORY
QUICK RUN
S-05
PASS 001 -  CS43
```

If execution is not error-free, reset and restart the program. In this way, Quick Run Mode will be blocked and the full section sequence of tests will be executed.

2.01.04.0 PROGRAM STOPS AND RESTARTS

04.1 NORMAL HALTS

There are two normal halts within each program. They will stop the program only if a manual reset and program restart had been made. Their only function is to permit the operator to set or reset two manual switches, as specified by typeouts preceding the halt, on the CE console.

The printed messages preceding each halt are shown for reference.

```
R  IF PARITY ERRORS EXIST -
R  SET CHECK CONTROL SWITCH TO RESTART
R  SET PRINT CONTROL SWITCH TO INHIBIT

S  ----- ----- -----, b ---- --------
```

The above normal halt follows the three-line message executed after the program is reset and restarted. It occurs only onee. Any subsequent resets and restarts will bypass both the message and the halt.

Depress Start to continue.

```
R  RESET CHK & PRINT CNTRL SW TO NORMAL

S ---- ---- ---- , b ----- --------
```

The above normal halt follows the single-line message executed prior to program exit. It serves to remind and permit the operator to reset the machine to normal program loading status before loading any subsequent program.

04.2 ERROR HALTS

None programmed.

Any halts occurring within Normal Mode will be of the standard "E" stop printout type. It will be the operator's responsibility to determine whether they are of CPU or data check nature. Program retry may be made in either Normal or Restart Check Control Mode.

2.01.04.0 PROGRAM STOPS AND RESTARTS (continued)

04.3 PROGRAM RESTART PROCEDURES

For CS43 - Depress Computer Reset.
Depress Start.

For CS44 -
CS46 -

Depress Computer Reset.
Set Mode Switch to Address Set.
Depress Start
Enter Address 22000 (for CS44)
42000 (for CS46)
Set Mode Switch to Run.
Depress Start.

2.01.05.0 PRINTOUTS

05.1 NORMAL TYPEOUT INDICATIONS

CS43@ or CS44@ or CS46@

The above identifies the program under test.
It is indicated only once.

(CS43) TESTS 20000-39999 AREA OF
or Tests 40000-x9999 AREA OF
(CS44) or TESTS 00001-x9999 AREA OF
(CS46)

The above serves as a reminder to identify the portion of memory being tested.
It is indicated only once.

40K, or 60K, or 60K, 80K, or 100K Memory

The above identifies the size and/or objective test area of memory being tested. This is presumed to have been designated by a single 3, 5, 7, or 9 digit, respectively, within the appropriate position on the standard System Control Card.
It is indicated only once.

2.01.05.0 PRINTOUTS (continued)

TAD STATUS -

The above serves to identify the status of each TAD assignment. It is indicated on program entrance and each time the program is reset and restarted. The example shows all TAD's down. Any TAD up would appear as numeric 1 in its respective position.

ENTER MEMORY SIZE DIGIT 3, 5, 7, or 9

The above is executed only if the memory size digit designation is missing or incorrect within the Standard System Control Card. The typeout is a request for this digit.
The operator should immediately do the following:

Depress Inquiry Request
Enter through the keyboard a 3, 5, 7, or 9
Depress Inquiry Release

For reference: 3 = 40K
5 = 60K
7 = 80K
9 = 100K

See Also Operating Hints and Comments, 2.01.03.1.

QUICK RUN

The above serves to indicate that an abbreviated memory check has been called for by TC50 and that Section 05 only will be executed.
See Operating Hints and Comments, 2.01.03.10

2.01.05.0 PRINTOUTS (continued)

S-01
S-02
-
-
-
S-13

The above serves to indicate when and which section was completed.

PASS 001-CS43 or PASS 001-CS44 or 46

The above serves to indicate: when, which and the total number of program passes completed.

IF PARITY ERRORS EXIST -
SET CHECK CONTROL SWITCH TO RESTART
SET PRINT CONTROL SWITCH TO INHIBIT

The above three-line message is executed only if the program had been reset and started again. It serves to remind the operator how to make the transition from Normal to Restart Mode.
It is indicated only once.

RESET CHK & PRINT CNTRL SW TO NORMAL

The above is executed unconditionally prior to program exit if the program had been reset and started again. It serves to remind the operator to restore the machine to Normal Status Mode before subsequent program loading is made.

AUTO SECT SEL
ENTER 2 DIGIT SECTION #

The above two-line message is executed whenever the program is reset and restarted and TAD 4 is set to 1. It serves to remind the operator that automatic section selection has been called for and that the program is waiting for him to designate the specific section he wants. He does so as follows: (See next page)

Depress Inquiry Request
Enter through the keyboard two numerics
(such as 03, 08, 12, etc.)
Depress Inquiry Release

Note: See Operating Hints and Comments, 2.01.03.2, for selection of "C" Sections.

NO ERRORS TABULATED

The above indicates that no bit pick or drop errors had been encountered and/or recorded into the error frequency table. It is executed as each section is completed and when TAD 6 is set to 1.

NO TABULATION PERFORMED

The above indicates that no bit pick or drop errors had been recorded into the error frequency table for either of the two following reasons:

1. Error table recording is not done in Section 5.

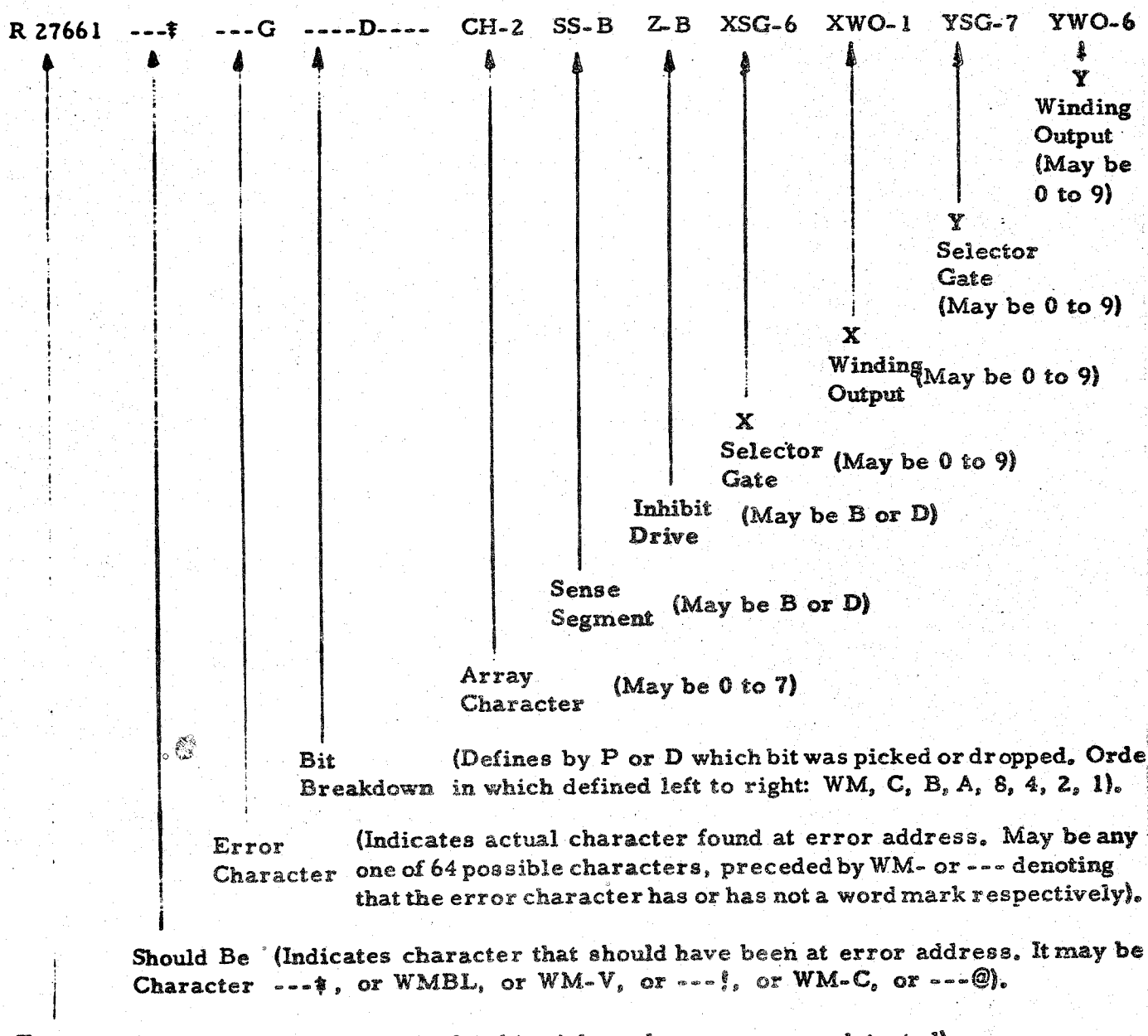
2. Error table recording has been intentionally bypassed.

   Note: If the typeout is executed as a result of this second condition, poor usage of TAD 5 and 6 is being made. TAD 6 is calling for output of the error table but has been nullified by TAD 5 which suppresses error recording.

2.01.05.0 PRINTOUTS (continued)

05.2 ERROR TYPEOUT INDICATIONS

The following is a typical format example of an Immediate Error Indication executed when encountered in all Sections (except Section 05).



2.01.05.0 PRINTOUTS (continued)

The following are typical examples of Immediate Error Indications executed when encountered in all sections (except Section 05).

R 38234 ---≠ WM-≠ P------- CH-3 SS-B Z-B XSG-3 XWO-4 YSG-8 YWO-2

The above is interpreted as follows:

38234	Address in which error was detected.
---≠	Character at that address should have been a not work mark-group mark.
WM-≠	Character found at that address was a word mark-group mark.
P-------	The bit breakdown indicates that a "Word Mark" bit was picked.
CH-3	Array character in which error address resides is 3.
SS-B	Sense Segment in which the error bit resides is B.
Z-B	Inhibit Drive in which the error address resides is B.
XSG-3	X Selector Gate for the error address is 3.
XWO-4	X Winding Output for the error address is 4.
YSG-8	Y Selector Gate for the error address is 8.
YWO-2	Y Winding Output for the error address is 2.

2.01.05.0 PRINTOUTS (continued)

R 14995 WMBL WM-1 -------P CH-1 SS-D Z-D XSG-9 XWO-5 YSG-4 YWO-9

The above is interpreted as follows:

14995	Address in which error was detected.
WMBL	Character at that address should have been a word mark-blank.
WM-1	Character found at that address was a word mark-1.
-------P	The bit breakdown indicates that a "1" bit was picked.
CH-1	Array character in which error address resides is 1.
SS-D	Sense Segment in which the error bit resides is D.
Z-D	Inhibit Drive in which error address resides is D.
XSG-9	X Selector Gate for the error address is 9.
XWO-5	X Winding Output for the error address is 5.
YSG-4	Y Selector Gate for the error address is 4.
YWO-9	Y Winding Output for the error address is 9.

2.01.05.0 PRINTOUTS (continued)

R 34567 WM-V WM-/ -----D-- CH-3 SS-D Z-D XSG-6 XWO-7 YSG-4 YWO-5

The above is interpreted as follows:

34567	Address in which error was detected.
WM-V	Character at that address should have been a word mark-V.
WM-/	Character found at that address was a word mark-slash.
-----D--	The bit breakdown indicates that a "4" bit was dropped.
CH-3	Array Character in which error address resides is 3.
SS-D	Sense Segment in which the error bit resides is D.
Z-D	Inhibit Drive in which error address resides is D.
XSG-6	X Selector Gate for the error address is 6.
XWO-7	X Winding Output for the error address is 7.
YSG-4	Y Selector Gate for the error address is 4.
YWO-5	Y Winding Output for the error address is 5.

2.01.05.0 PRINTOUTS (continued)

R 28777 ---! ---K ----D--- CH-2 SS-B Z-B XSG-7 XWO-7 YSG-8 YWO-7

The above is interpreted as follows:

28777	Address in which error was detected.
---!	Character at that address should have been a not word mark-exclamation point.
---K	Character found at that address was a not word mark-K.
----D---	The bit breakdown indicates that an "8" bit was dropped.
CH-2	Array Character in which error address resides is 2.
SS-B	Sense Segment in which the error bit resides is B.
Z-B	Inhibit Drive in which error address resides is 7.
XSG-7	X Selector Gate for the error address is 7.
XWO-7	X Winding Output for the error address is 7.
YSG-8	Y Selector Gate for the error address is 8.
YWO-7	Y Winding Output for the error address is 7.

2.01.05.0 PRINTOUTS (continued)

R 55000 WM-C WM-L ---D---- CH-5 SS-B Z-B XSG-0 XWO-0 YSG-5 YWO-0

The above is interpreted as follows:

55000	Address in which error was detected.
WM-C	Character at that address should have been a word mark-C.
WM-L	Character found at that address was a word mark-L.
---D----	The bit breakdown indicates that an "A" bit was dropped.
CH-5	Array Character in which error address resides is 5.
SS-B	Sense Segment in which the error bit resides is B.
Z-B	Inhibit Drive in which error address resides is B.
XSG-0	X Selector Gate for the error address is 0.
XWO-0	X Winding Output for the error address is 0.
YSG-5	Y Selector Gate for the error address is 5.
YWO-0	Y Winding Output for the error address is 0.

2.01.05.0 PRINTOUTS (continued)

R 74789 ---@ ---* --P----- CH-7 SS-D Z-D XSG-8 XWO-9 YSG-4 YWO-7

The above is interpreted as follows:

74789	Address in which error was detected.
---@	Character at that address should have been a word mark-at sign.
---*	Character found at that address was a not word mark-asterisk.
--P-----	The bit breakdown indicates that a "B" bit was picked.
CH-7	Array Character in which error address resides is 7.
SS-D	Sense Segment in which the error bit resides is D.
Z-D	Inhibit Drive in which error address resides is D.
XSG-8	X Selector Gate for the error address is 8.
XWO-9	X Winding Output for the error address is 9.
YSG-4	Y Selector Gate for the error address is 4.
YWO-7	Y Winding Output for the error address is 7.

2.01.05.0 PRINTOUTS (continued)

Section 05 Error Typeouts -

The following are possible examples of immediate error indications encountered in Section 5 only. These errors are not table recordable or address repeatable.

A-$\overset{Y}{3}$5004, C-$\overset{Y}{1}$5004

The above is interpreted as follows:

A-$\overset{Y}{3}$5004 Address in which error was detected in one or more positions between 35000-35004.

C-$\overset{Y}{1}$5004 Contents found at that address did not match the address.

A-$\overset{Y}{1}$9584, C-$\overset{Y}{1}$9

The above is interpreted as follows:

A-$\overset{Y}{1}$9584 Address in which error was detected in one or more positions between 19580-19584.

C-$\overset{Y}{1}$9 Contents found at that address did not match the address. In addition, either the third or fourth position character was invalid since the typeout was cut off short. This condition also indicates problems other than those of addressing since bit pick and drop problems exist.

05.3 ERROR ADDRESS REPETITION

REPEATING ERROR ADDR- 27661 XWO-1 XWO-6

The above is a typical format example of an Address Repetition message executed when TAD 10 is set to a 1 and following the first detection of a pick or drop error.

The message informs the observer that the program is entering the closed loop and provides the address, the X winding output and the Y winding output.

2.01.05.0 PRINTOUTS (continued)

05.4 ERROR FREQUENCY TABLE

If and when TAD 6 is set to 1 and errors have been encountered, a complete multi-line printout is made immediately after each section (so long as TAD 6 remains up) pointing out the frequency of errors by character, bit plane, selector gate, winding output, sense segment, and inhibit drive all correlated into appropriate drop and pick divisions. TAD 6 may be used at any time or at the completion of all sections.

Tabulation is unconditional (unless suppressed by TAD 5) and is accumulative from one section test to another if the table is not printed. Printing the table, resetting or reloading the program will clear the tabulation fields to initial zeros. Sample printouts are provided on the following pages.

If tabulation for only one section is desired, use the TAD 4 switch feature of immediate automatic section selection.

If it is desired to obtain tabulation data for two or more specific sections, TAD 5 can be used discriminately to suppress error tabulation of any or all sections prior to and/or following the desired sections.

The release versions of these tests select the typewriter for the tabulation output. If it is desired to use the printer instead for this "on line" output, store a 1 in TAD 7.

05.5 EFFECTIVE INTERPRETATION AND USAGE OF TABULATED DATA

The tabulation of errors feature is particularly useful in obtaining an overall picture of what is failing (by matrix definition of character by bit) and at what locations (actual memory addresses decoded into equivalent selector gates, winding outputs, sense segments, and Z drives). All error data is accumulated unconditionally into the tabulation fields (unless suppressed by TAD 5). Regardless of the setting of TAD 0, TAD 6 always overrides any setting of TAD0. Therefore, if many immediate error indications do occur, it is strongly recommended, as a time-saving device, to set both TAD 0 and TAD 6 to 1.

2.01.05.0 PRINTOUTS (continued)

In order to prevent time-consuming printing time of the entire table, a built-in interrogation routine inspects the table each time that printed table output is called for. This routine checks each character line for any recorded errors and informs the table printing routine to print only those character lines, which contain recorded errors.

In addition, another feature has been included to prevent time-consuming repetition of already known information. As mentioned before, recorded error tabulation is uncodditional and is accumulated from one section to another unless called for and printed by TAD 6. If and when the table is printed an automatic table clearance routine resets the fields to zeros prior to the next section test. In this way, the observer will receive table output for only those sections which record errors.

A final point worth mentioning is that although each character line of the table shows a "C" bit division, this division will not contain recorded error totals. Since the 1410 has no instruction that can interrogate the "C" bit exclusively or otherwise, it is impossible to program record "C" bit pick or drop errors into the table. This is also true of the eight position bit breakdown that is included in the Immediate Error Indication typeout. However, the "C" bit position was placed in both output areas in order to maintain continuity, prevent confusion, and in hopes that the desirable instruction would, at some time, be included for Customer Engineering use only.

2.01.05.0 PRINTOUTS (continued)

The following is a typical format example of the Error Frequency Table output:

It contains four basic sub-tables:

1. Character (CH) by Bit Plane (BP) Table.
2. X selector gate (XSG) by Y selector gate (YSG) Table.
3. X winding output (XWO) by Y winding output (YWO) Table.
4. Inhibit Drive (Z) by Sense Segment (SS) Table.

— The Header Line defines the program and section for which the Table is being printed.

— The BP line defines the eight-bit divisions per character line.

— The P defines the Number of picks per bit division.

— The D defines the number of drops per bit division.

CS46-ERRTAB* FOR SECTION -11

BP	P-1-D	P-2-D	P-4-D	P-8-D	P-A-D	P-B-D	P-C-D	P-W-D
CH 0-	0 0 0 0 433	0 0 0 0	0 0 0 0	0 0 0 0	- -	0 0		
CH 1-	0 0 0 0 238	0 0 0 0	0 0 0 0	0 0 0 0	- -	0 0		
CH 2-	0 0 0 0 124	0 0 0 0	0 0 0 0	0 0 0 0	- -	0 0		
CH 3-	0 0 0 0 40	0 0 0 0	0 0 0 0	0 0 0 0	- -	0 0		

— The CH lines identify each Array Character containing recorded error totals.

— The YS line defines the ten Y selector gate divisions per XSG line.

XS YS	P-0-D	P-1-D	P-2-D	P-3-D	P-4-D	P-5-D	P-6-D	P-7-D	P-8-D	P-9-D
G0-	0 0 30	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G1-	0 0 60	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G2-	0 0 82	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G3-	0 0 111	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G4-	0 0 102	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G5-	0 0 91	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G6-	0 0 96	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G7-	0 0 95	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G8-	0 0 70	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
G9-	0 0 98	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0

— The G lines identify each X selector gate containing recorded error totals.

(See third and fourth part of table on next page.)

2.01.05.0 PRINTOUTS (continued)

The W lines identify each X Winding Output containing recorded error totals.

The YW line defines the ten Y winding output divisions per XWO line.

XW YW	P-0-D	P-1-D	P-2-D	P-3-D	P-4-D	P-5-D	P-6-D	P-7-D	P-8-D	P-9-D
W0-	49 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
W1-	0 0 128	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
W2-	0 0 0	0 70 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
W3-	0 0 0	0 0 0	88 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
W4-	0 0 0	0 0 0	0 0 0	51 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
W5-	0 0 0	0 0 0	0 0 0	0 0 0	42 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
W6-	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	92 0 0	0 0 0	0 0 0	0 0 0	0 0 0
W7-	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	147 0 0	0 0 0	0 0 0	0 0 0
W8-	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	110 0 0	0 0 0	0 0 0
W9-	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	58 0 0	0 0 0

	SS	P-B-D	P-D-D
Z BD-		0 0	835 0

The SS line defines the two Sense Segment divisions.

The Z line identifies both Inhibit Drives containing recorded error totals.

2.01.05.0 PRINTOUTS (continued)

The following are typical examples of Error Frequency Tables (preceded by Immediate Error Indications) containing the tabulated errors recorded for the section indicated.

* Note that only those parts of the table that contain recorded pick and drop errors are printed.

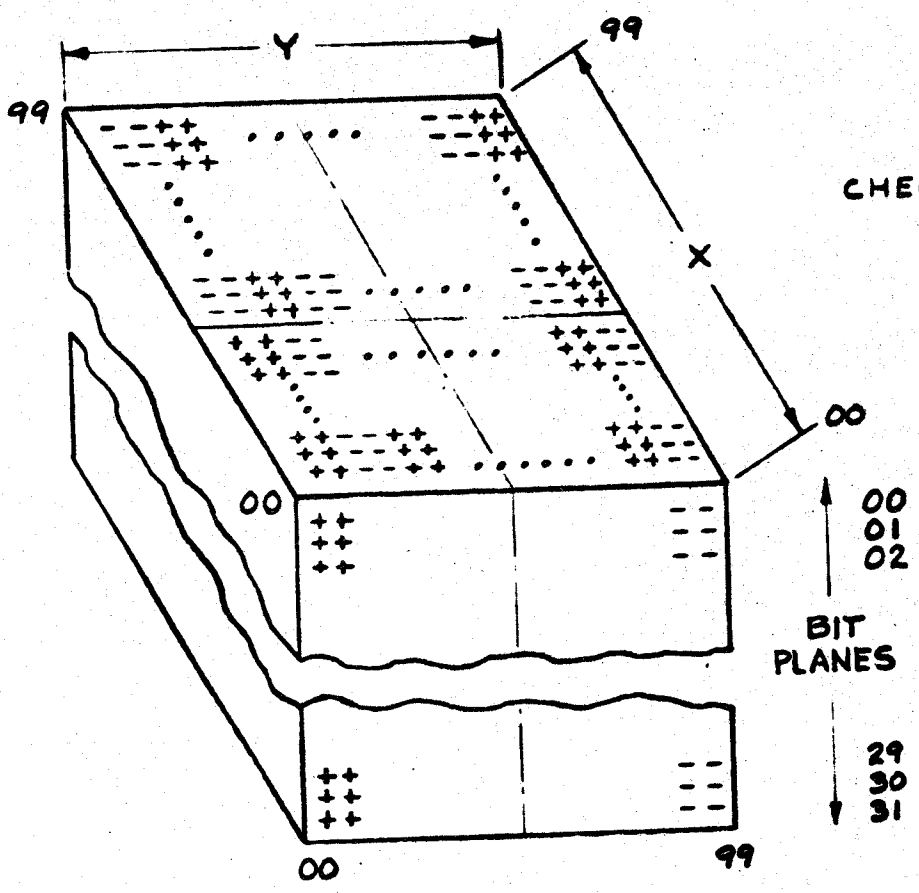
```
16543  WMBL  WM-2  ------P-  CH-1  SS-B  Z-B  XSG-4  XWO-3  YSG-6  YWO-5
17654  WMBL  WM-2  ------P-  CH-1  SS-B  Z-B  XSG-5  XWO-4  YSG-7  YWO-6
18765  WMBL  WM-2  ------P-  CH-1  SS-B  Z-B  XSG-6  XWO-5  YSG-8  YWO-7
19012  WMBL  WM-1  -------P  CH-1  SS-B  Z-B  XSG-1  XWO-2  YSG-9  YWO-0
19123  WMBL  WM-1  -------P  CH-1  SS-B  Z-B  XSG-2  XWO-3  YSG-9  YWO-1
19234  WMBL  WM-1  -------P  CH-1  SS-B  Z-B  XSG-3  XWO-4  YSG-9  YWO-2
19345  WMBL  WM-1  -------P  CH-1  SS-B  Z-B  XSG-4  XWO-5  YSG-9  YWO-3
19456  WMBL  WM-1  -------P  CH-1  SS-B  Z-B  XSG-5  XWO-6  YSG-9  YWO-4

CS44-ERRTAB* FOR SECTION-02
      BP  P-1-D  P-2-D  P-4-D  P-8-D  P-A-D  P-B-D  P-C-D  P-W-D
CH 1-    5  0    3  0    0  0    0  0    0  0    0  0    -  -    0  0
XS YS P-0-D P-1-D P-2-D P-3-D P-4-D P-5-D P-6-D P-7-D P-8-D P-9-D
G1-   0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0
G2-   0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0
G3-   0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0
G4-   0  0  0  0  0  0  0  0  0  0  0  0  1  0  0  0  0  0  1  0
G5-   0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0  0  0  1  0
G6-   0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0  0  0
XW YW P-0-D P-1-D P-2-D P-3-D P-4-D P-5-D P-6-D P-7-D P-8-D P-9-D
W2-   1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0
W3-   0  0  1  0  0  0  0  0  0  0  1  0  0  0  0  0  0  0  0  0
W4-   0  0  0  0  1  0  0  0  0  0  0  0  1  0  0  0  0  0  0  0
W5-   0  0  0  0  0  0  1  0  0  0  0  0  0  0  1  0  0  0  0  0
W6-   0  0  0  0  0  0  0  0  1  0  0  0  0  0  0  0  0  0  0  0
      SS  P-B-D  P-D-D
Z BD-    8  0  0  0
```

The above is an example of an Error Frequency Table executed following the completion of Section 02 while running Program CS44.

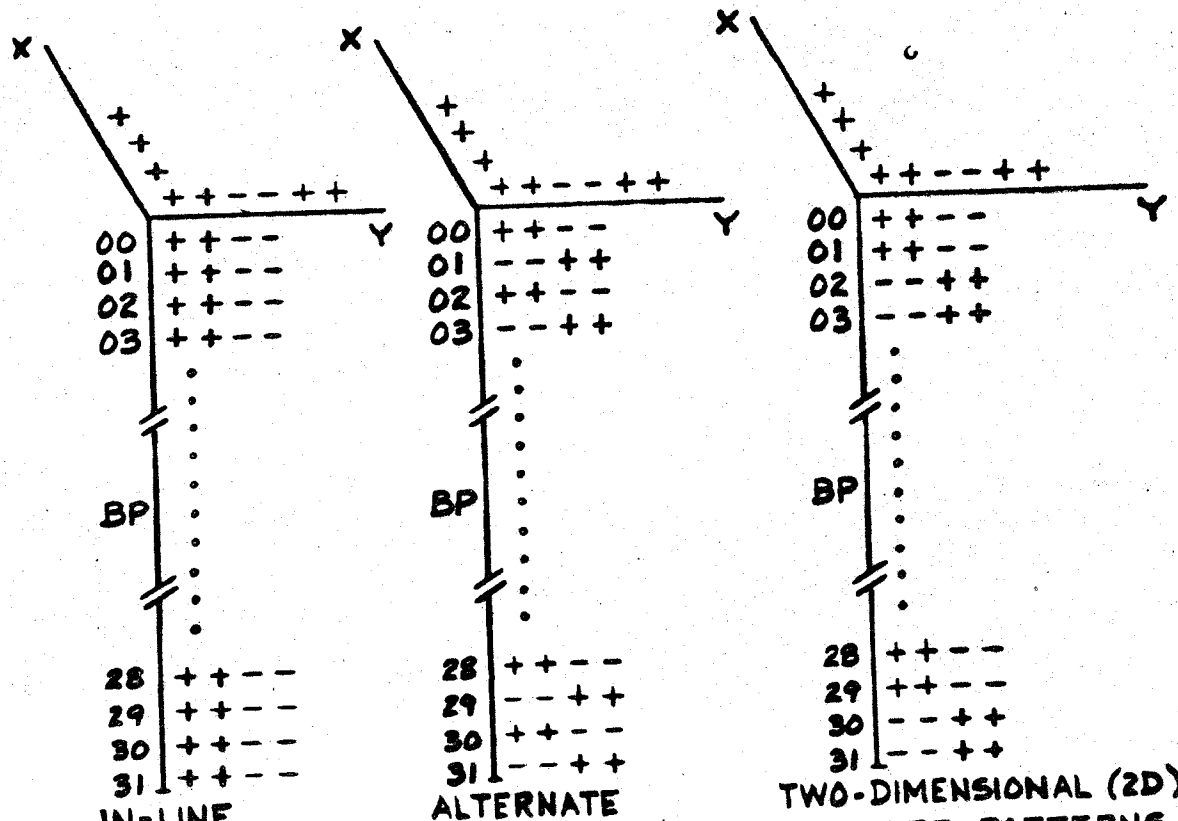
2.01.05.0 PRINTOUTS (continued)

```
12345  WMBL  WM-4  -----P--  CH-1  SS-D  Z-D  XSG-4  XWO-5  YSG-2  YWO-3
13456  WMBL  WM-4  -----P--  CH-1  SS-D  Z-D  XSG-5  XWO-6  YSG-3  YWO-4
17890  WMBL  WM-8  ----P---  CH-1  SS-B  Z-B  XSG-9  XWO-0  YSG-7  YWO-8
19765  WMBL  WM-1  -------P  CH-1  SS-B  Z-B  XSG-6  XWO-5  YSG-9  YWO-7
CS44-ERRTAB* FOR SECTION -12
      BP  P-1-D  P-2-D  P-4-D  P-8-D  P-A-D  P-B-D  P-C-D  P-W-D
CH 1-     1     0  0     0  2     0  1     0  0     0  0     0  -     -  0     0

XS YS  P-0-D  P-1-D  P-2-D  P-3-D  P-4-D  P-5-D  P-6-D  P-7-D  P-8-D  P-9-D
G4-    0  0  0  0  1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0
G5-    0  0  0  0  0  0  1  0  0  0  0  0  0  0  0  0  0  0  0  0
G6-    0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1
G9-    0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0  0  0  0  0

XW YW  P-0-D  P-1-D  P-2-D  P-3-D  P-4-D  P-5-D  P-6-D  P-7-D  P-8-D  P-9-D
WO-    0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0  0  0
W5-    0  0  0  0  0  0  1  0  0  0  0  0  0  0  1  0  0  0  0  0
W6-    0  0  0  0  0  0  0  0  1  0  0  0  0  0  0  0  0  0  0  0

      SS  P-B-D  P-D-D
Z BD-     2     0  2     0
```

The above is an example of an Error Frequency Table executed following the completion of Section 12 while running program CS44.



TYPICAL X-Y
CHECKERBOARD PATTERN
FOR
1411 MEMORY



- TYPICAL BIT PLANE CHECKERBOARD PATTERNS -