

# **IBM** Field Engineering Maintenance Diagrams

## **1130** Computing System Features

## PREFACE

This manual contains maintenance diagrams for the following features of the IBM 1130 Computing System:

Synchronous Communications Adapter  
IBM 2501 Card Reader Adapter  
IBM 1231 Optical Mark Page Reader Adapter

Use the system diagrams at the engineering level of the equipment being serviced when there is a difference between the system diagrams and the maintenance diagrams in this manual.

### **Fourth Edition (May 1970)**

This manual is a complete revision of SY26-4003-2 and obsoletes the previous edition.

Specifications contained herein are subject to change from time to time. Any such change will be reported in subsequent revisions or Field Engineering Supplements.

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LEGEND. . . . . iv

SYNCHRONOUS COMMUNICATIONS ADAPTER

Data Flow

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2501 CARD READER ADAPTER

Data Flow

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Functional Units . . . . . None

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1231 OPTICAL MARK PAGE READER ADAPTER

Data Flow

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Functional Units

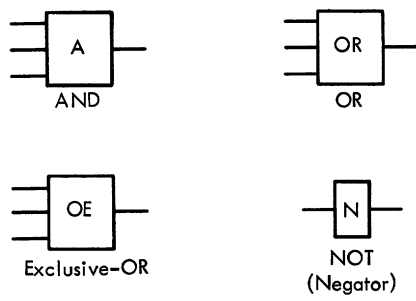
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Operations . . . . . None

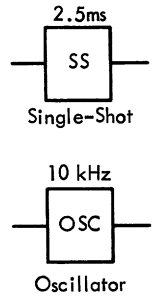
**LEGEND**

In positive logic representation, signal levels are disregarded. The negator (N block symbol) is used to invert logic, not level. Passive elements (such as drivers and pulse shapers) generally are not shown, since they contribute nothing to the logic.

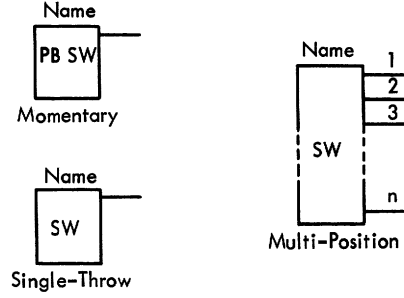
**LOGICAL ELEMENTS**



**TIMING ELEMENTS**



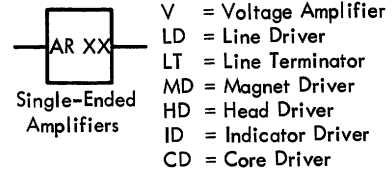
**SWITCHES**



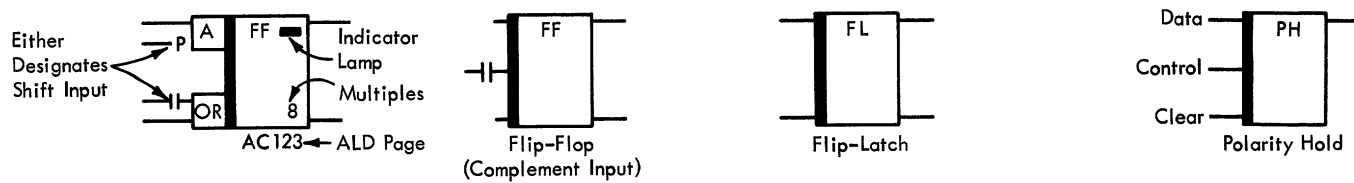
**PASSIVE ELEMENTS**



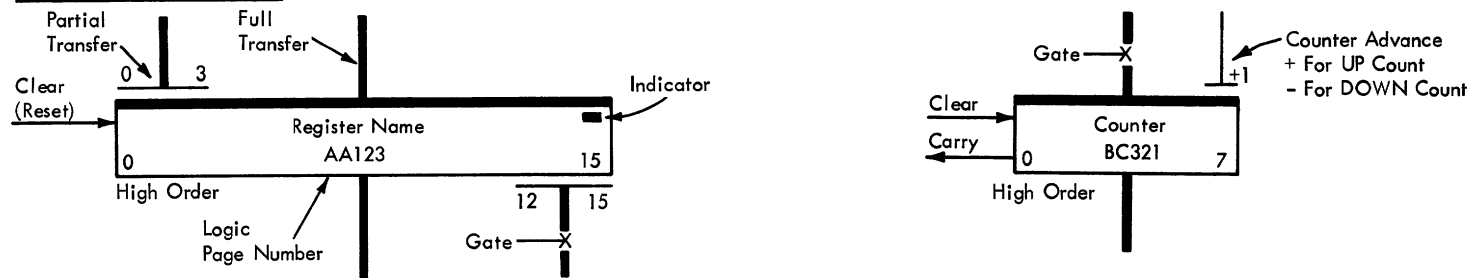
**XX Abbreviations**



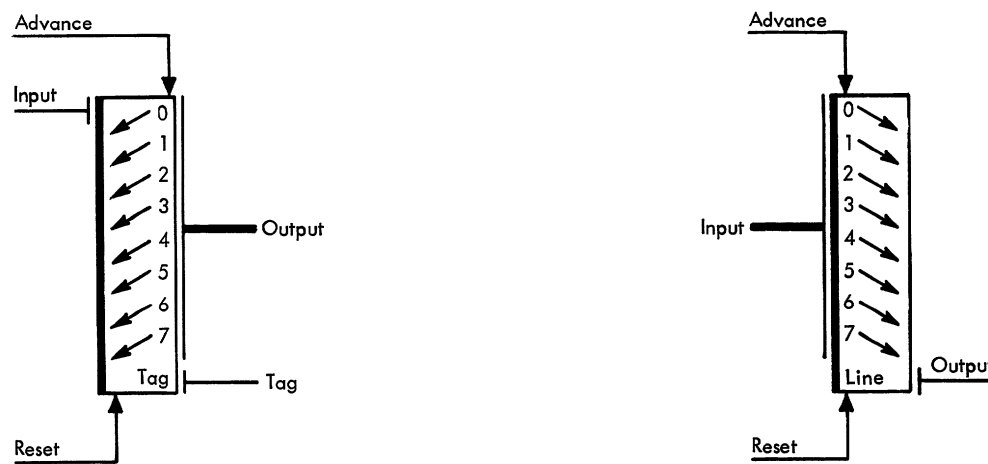
**STORAGE ELEMENTS**



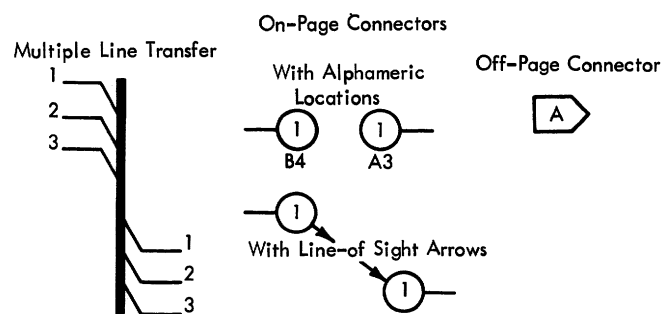
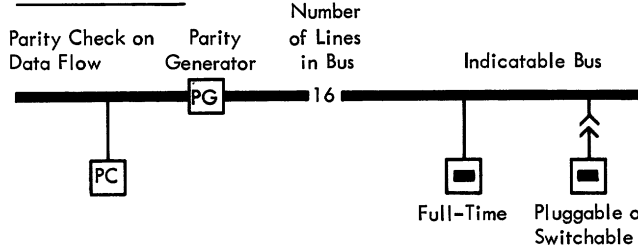
**REGISTERS AND COUNTERS**



**SHIFT REGISTERS**



**MISCELLANEOUS**



A

B

C

D

E

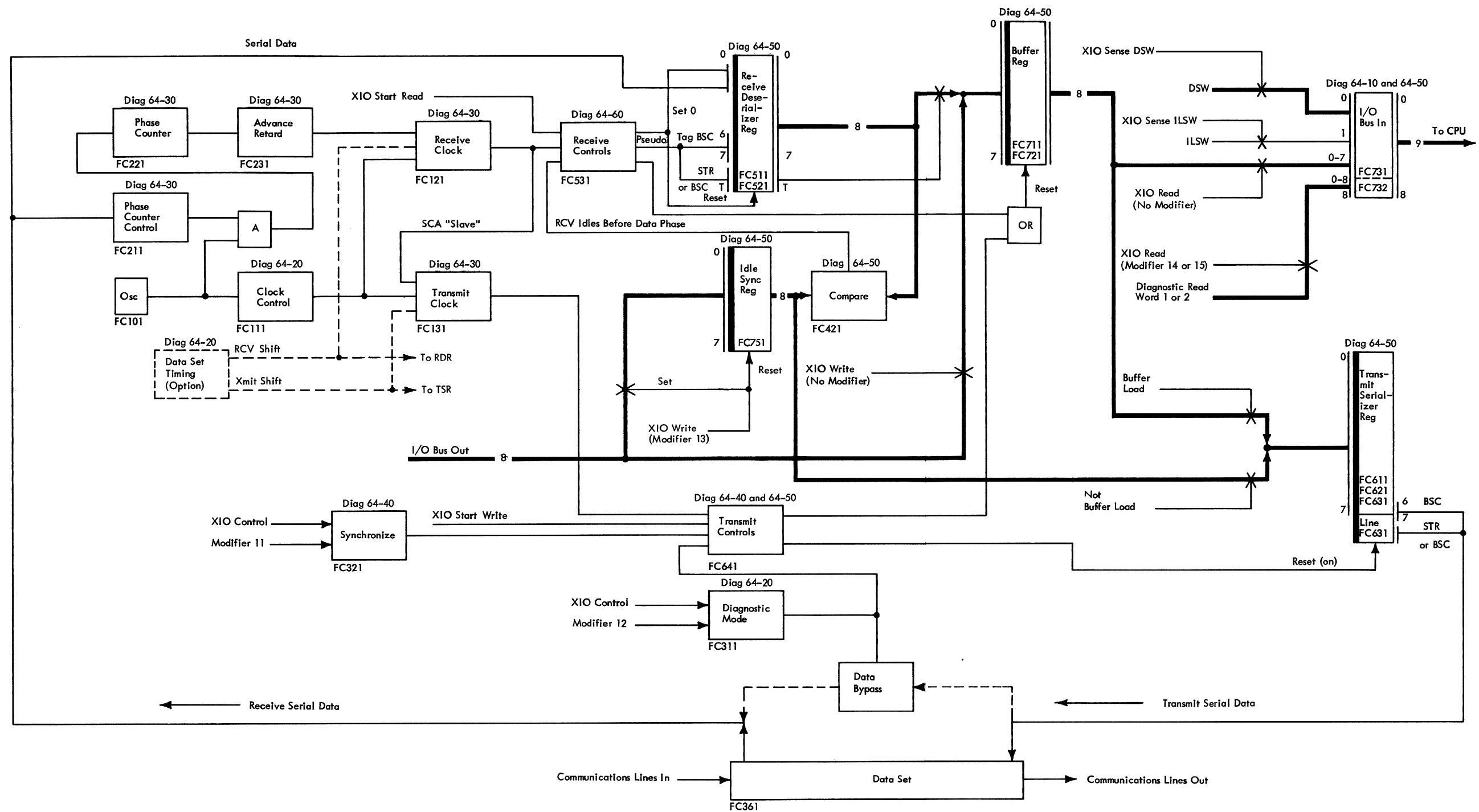


Diagram 63-10. SCA Data Flow and Control



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I/O Bus In 65-20, E8

A

B

C

D

E

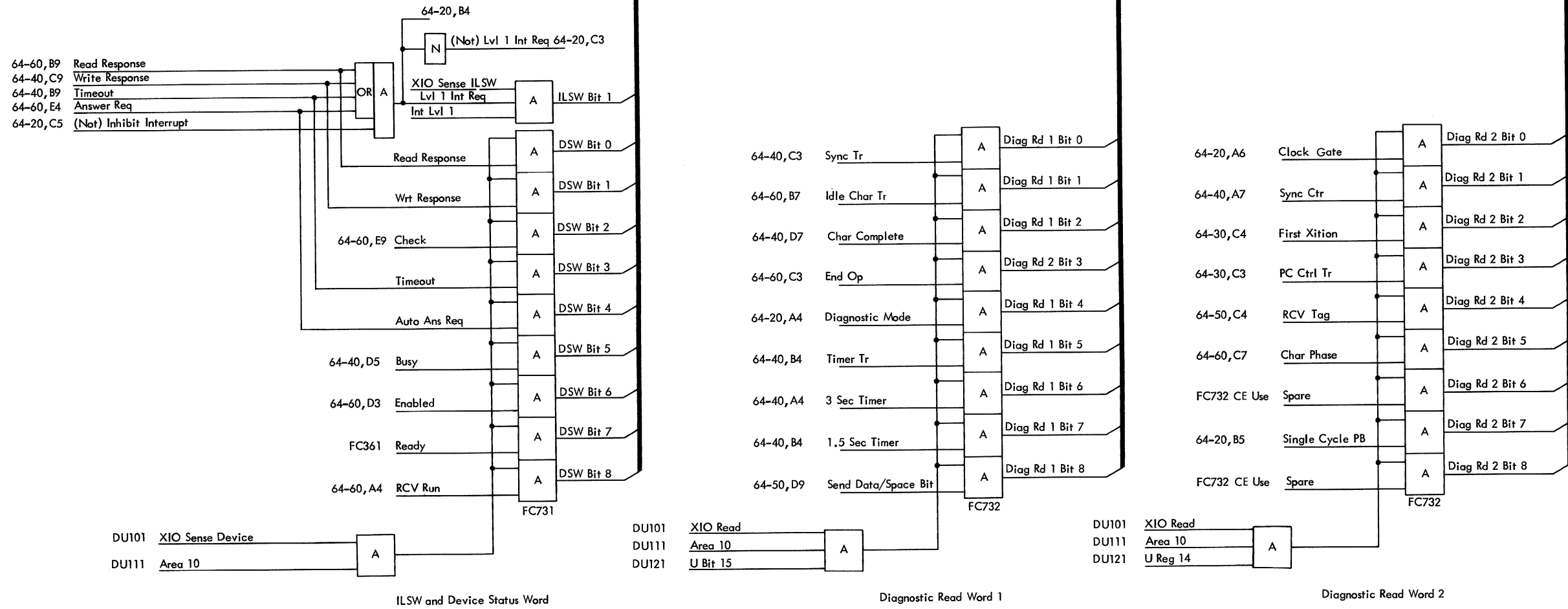
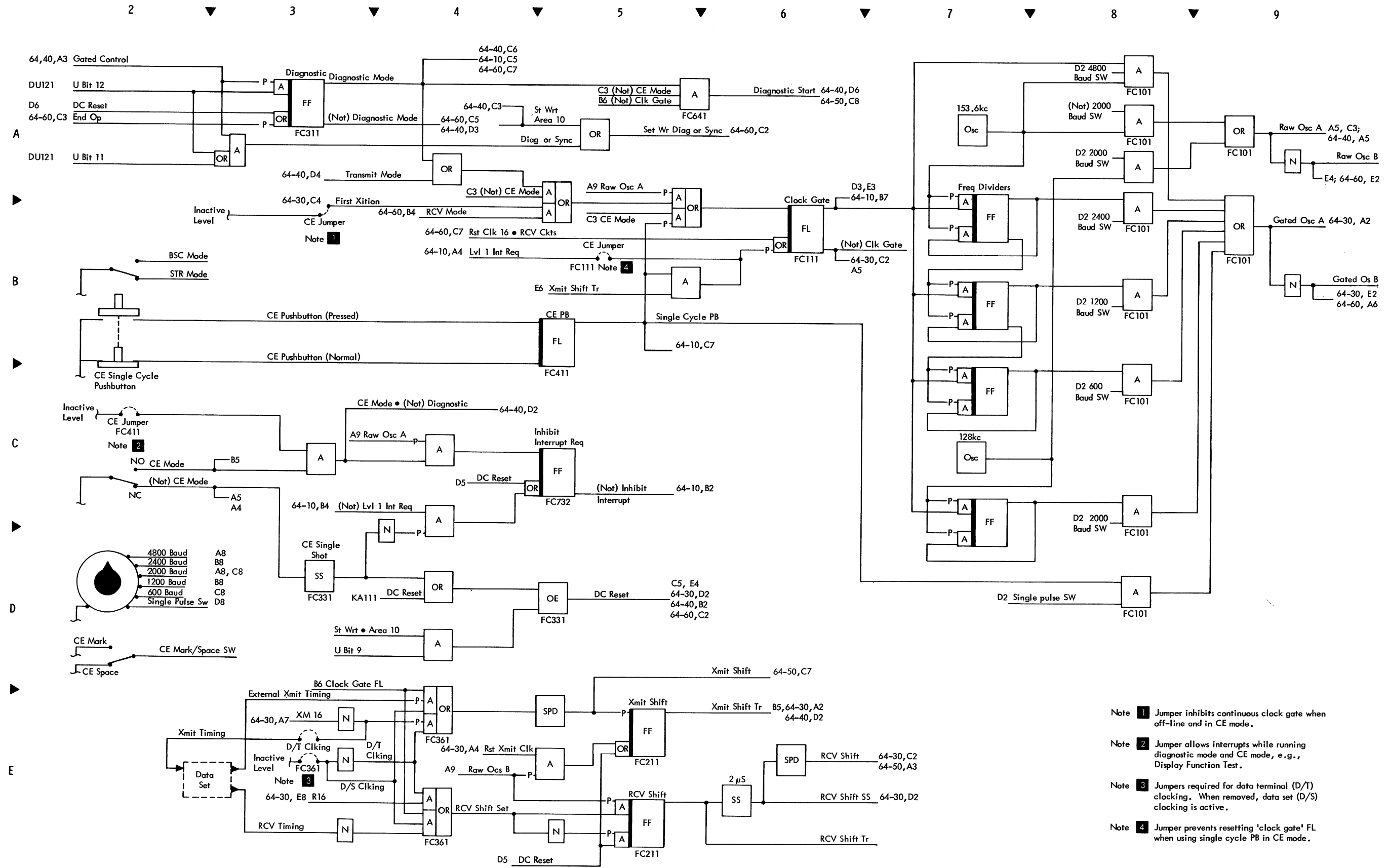


Diagram 64-10. DSW and Diagnostic Read Words 1 and 2

Diagram 64-20. Clock Controls, CE Mode and Switches, and Diagnostic Mode



- Note 1 Jumper inhibits continuous clock gate when off-line and in CE mode.
- Note 2 Jumper allows interrupts while running diagnostic mode and CE mode, e.g., Display Function Test.
- Note 3 Jumpers required for data terminal (D/T) clocking. When removed, data set (D/S) clocking is active.
- Note 4 Jumper prevents resetting 'clock gate' FL when using single cycle PB in CE mode.



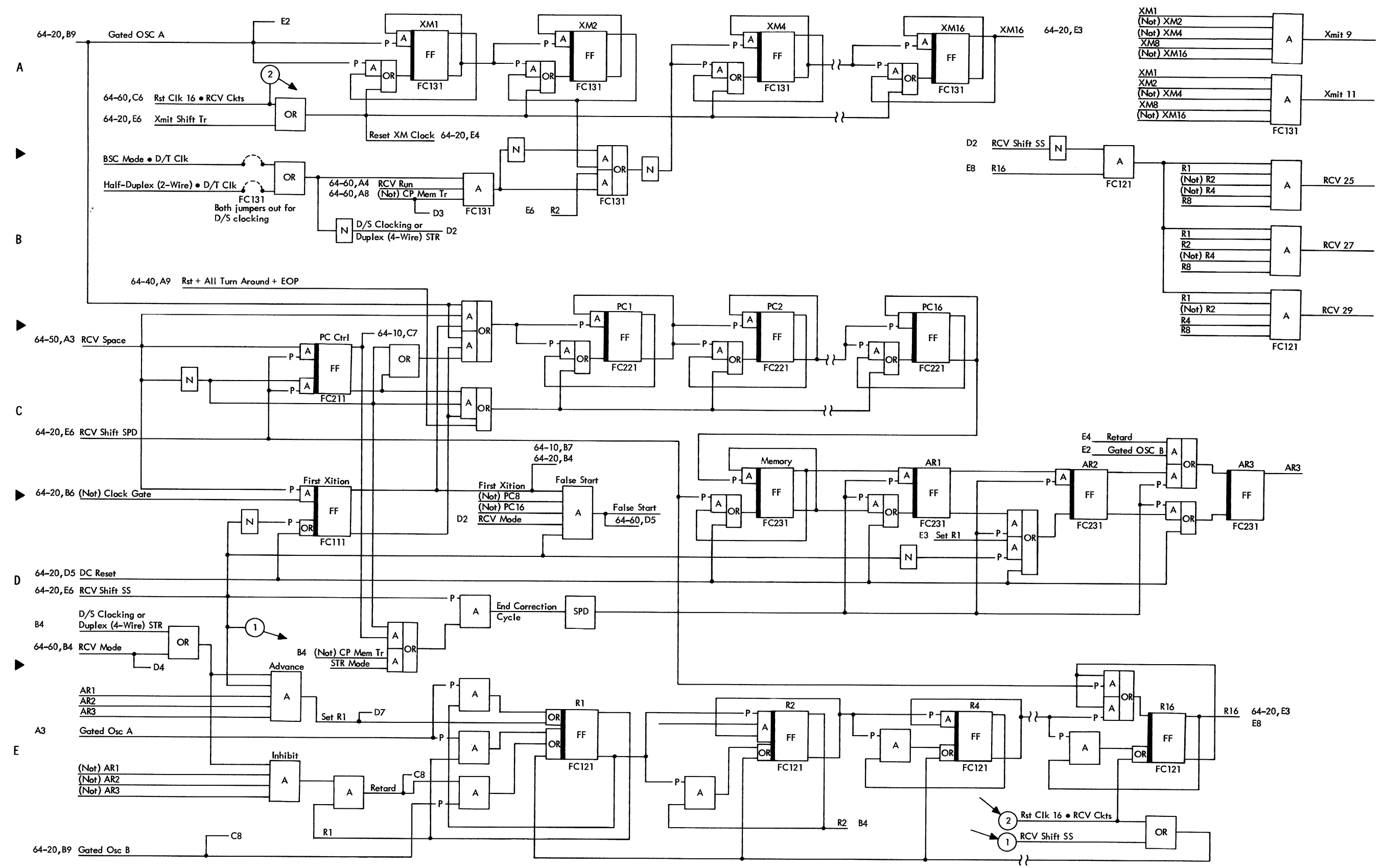
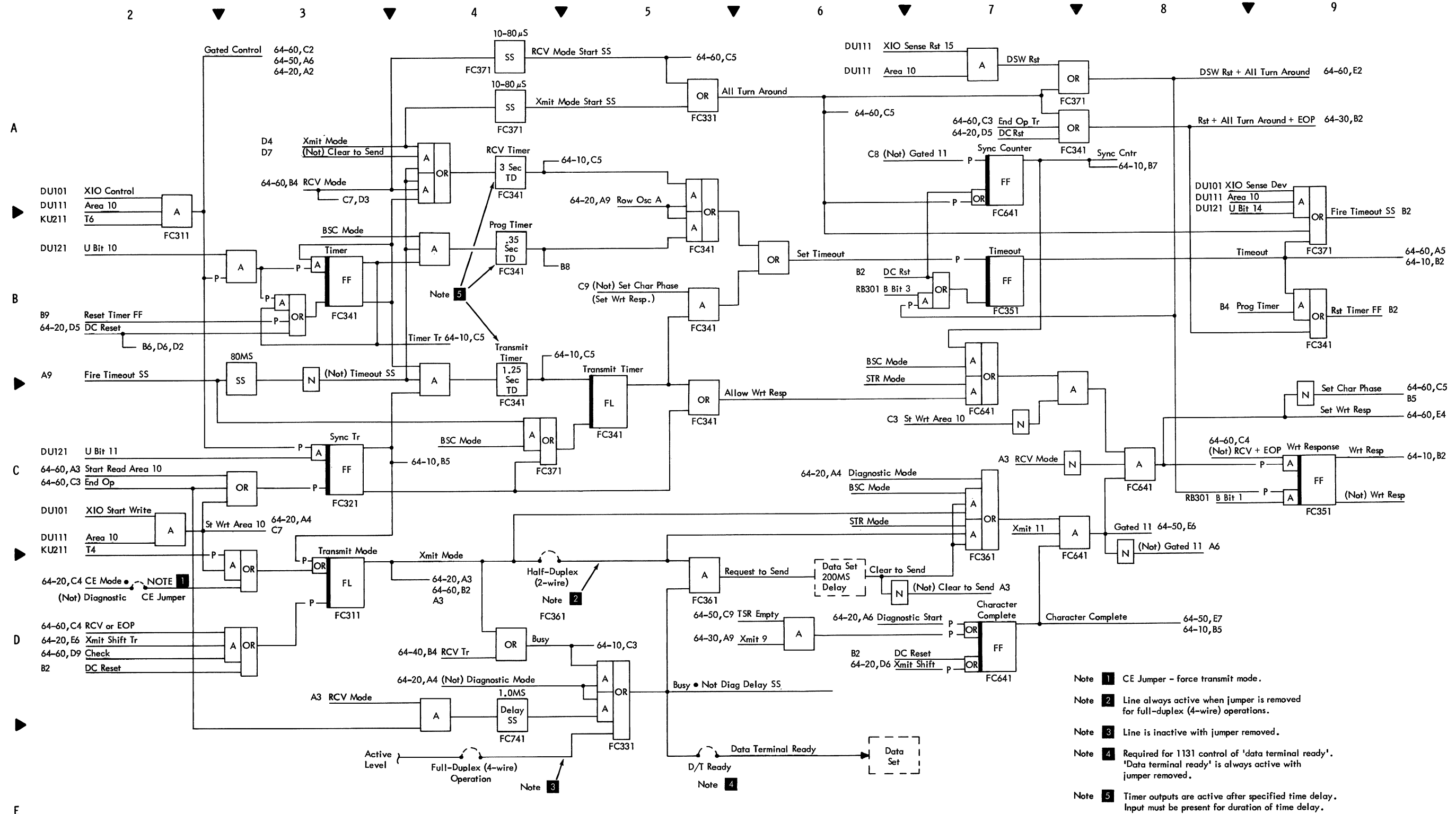
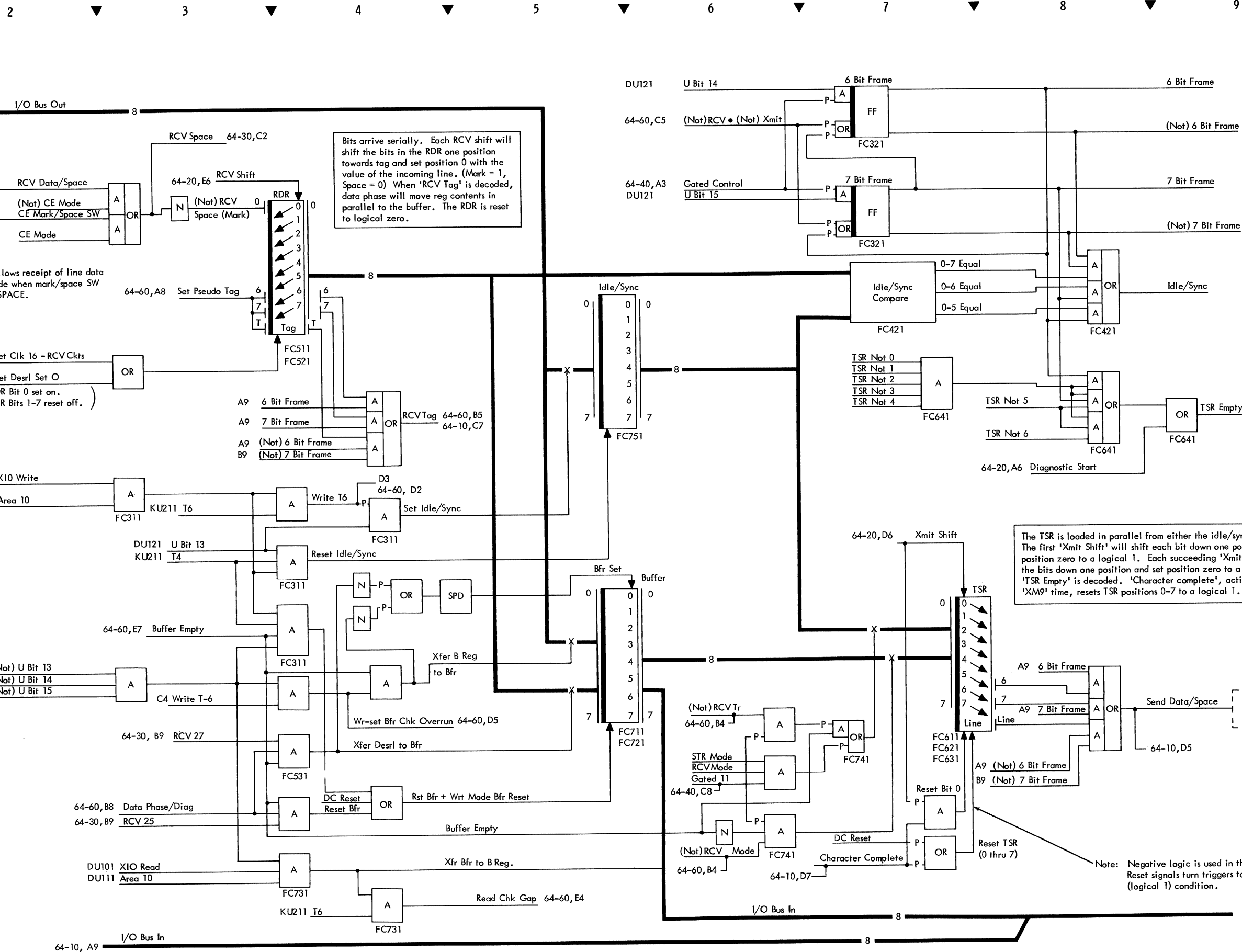


Diagram 64-30. Clocks, Phase Counter, and Advance/Retard

Diagram 64-40. Synchronize and Start Write



- Note 1 CE Jumper - force transmit mode.
- Note 2 Line always active when jumper is removed for full-duplex (4-wire) operations.
- Note 3 Line is inactive with jumper removed.
- Note 4 Required for 1131 control of 'data terminal ready'. 'Data terminal ready' is always active with jumper removed.
- Note 5 Timer outputs are active after specified time delay. Input must be present for duration of time delay.



Bits arrive serially. Each RCV shift will shift the bits in the RDR one position towards tag and set position 0 with the value of the incoming line. (Mark = 1, Space = 0) When 'RCV Tag' is decoded, data phase will move reg contents in parallel to the buffer. The RDR is reset to logical zero.

The TSR is loaded in parallel from either the idle/sync or buffer regs. The first 'Xmit Shift' will shift each bit down one position and set position zero to a logical 1. Each succeeding 'Xmit Shift' will shift the bits down one position and set position zero to a logical 0 until 'TSR Empty' is decoded. 'Character complete', active at the next 'XM9' time, resets TSR positions 0-7 to a logical 1.

Note: Negative logic is used in the TSR. Reset signals turn triggers to the on (logical 1) condition.

Diagram 64-50. Read and Write



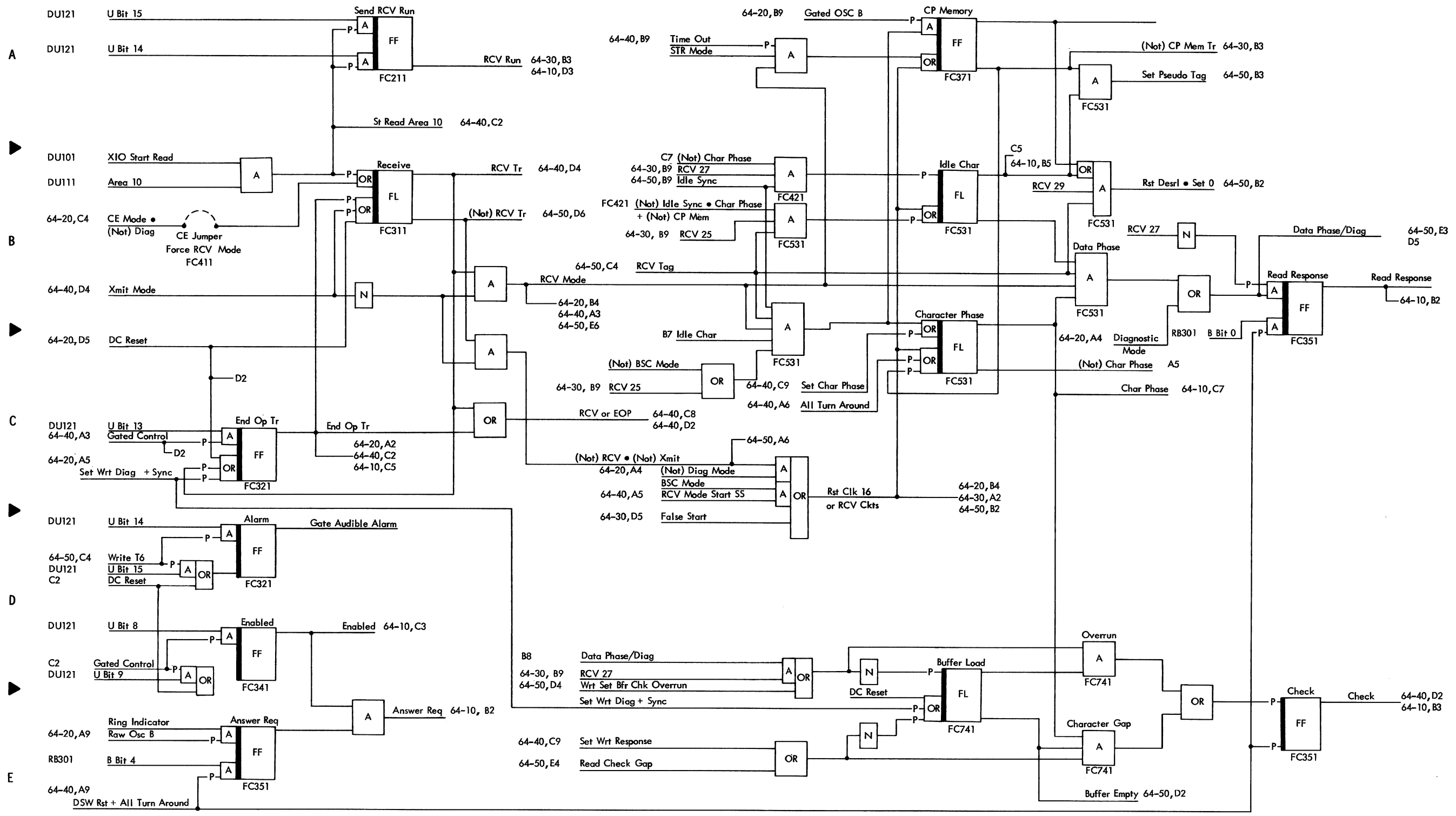
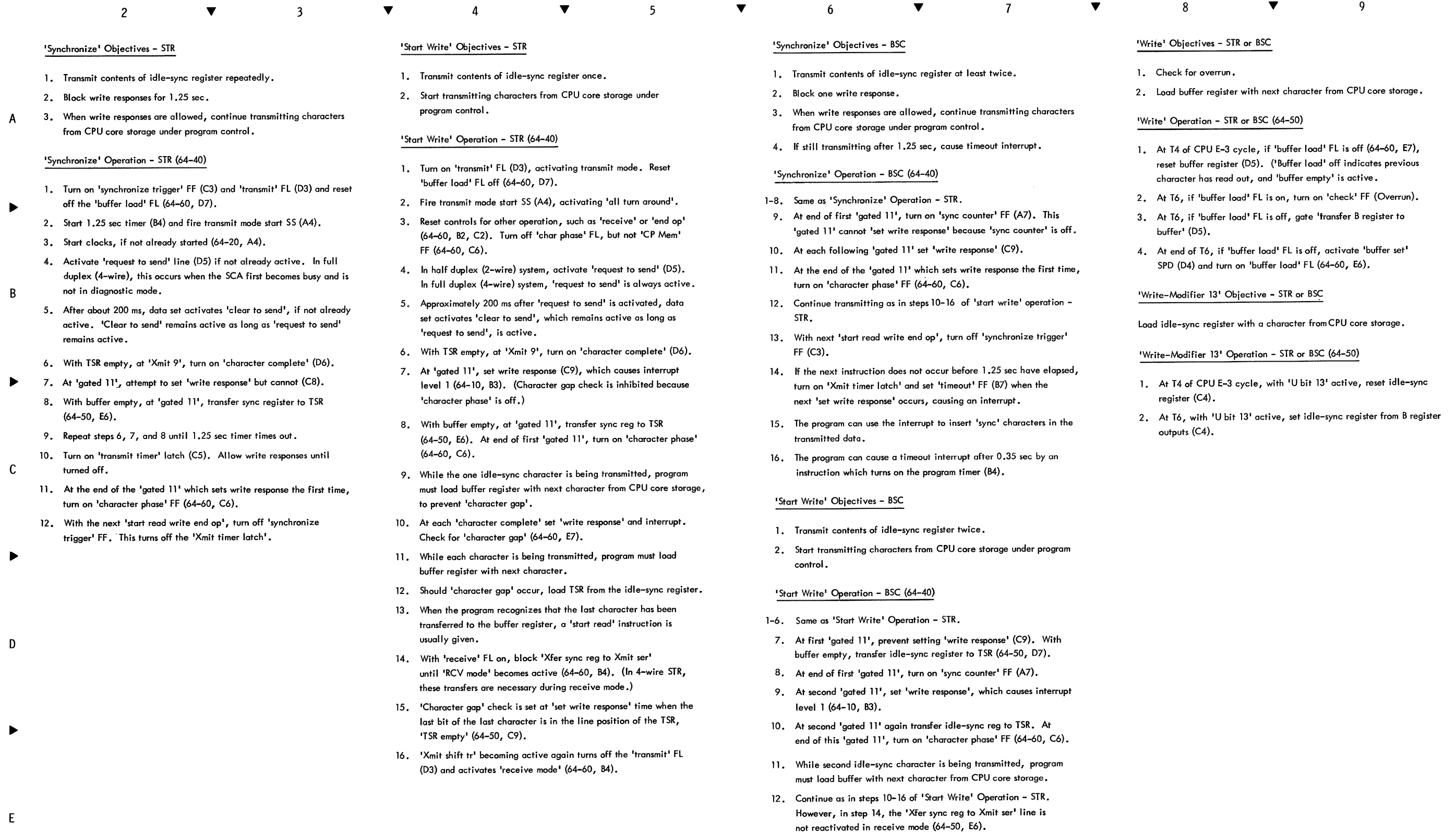


Diagram 64-60. Start Read and Checks

Diagram 65-10. Synchronize, Start Write, and Write (Objectives and Operation)



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'Start Read' Objectives - STR

1. Recognize one idle-sync character and establish 'character phase'.
2. Starting with first non-idle character, receive following characters and set them in buffer register. Idle-sync characters received during 'character phase' are handled as data characters in SCA.

'Start Read' Operation - STR (64-60)

1. Turn on 'receive' FL (B3). If 'transmit' FL is off, activate 'receive mode' immediately. If 'transmit' is on, wait to activate 'receive mode' when 'transmit' turns off.
2. Fire receive mode start SS (64-40, A4). Activate 'all turn around'.
3. Reset controls for other operations. Turn off 'character phase' FL, but not 'CP memory' FF, if they are on (C6 and A6).
4. Start receiving and shifting bits through RDR, comparing RDR with idle-sync register (64-50, B3, B7).
5. If 'CP memory' FF is off (not previously in 'character phase', or else a timeout occurred during the last 'receive mode'):
  - A. With equal idle-sync compare, turn on 'idle character' FL at RCV 27 (B6).
  - B. With 'idle character' on activate 'set pseudo tag' (A7).
  - C. Turn on 'character phase' and 'CP memory' (C6 and A6).
6. If 'CP memory' FF is on (previously in 'character phase' and no timeout occurred during the last 'receive mode'):
  - A. With equal idle-sync compare, turn on 'idle character' FL at RCV 27 (B6).
  - B. Framing was previously completed (tags shifting through RDR).
  - C. With equal idle-sync compare and 'idle character' on, turn on 'character phase' and 'CP memory' at 'tag' time (A7 and C7).
7. On receipt of the first non-idle character, at 'tag' time turn off 'idle character' at RCV 25 (B5).
8. Activate 'data phase' at RCV tag time (B7).
9. With 'buffer load' off and RCV 25, reset buffer register (64-50, E3).
10. At RCV 27, if 'buffer load' is on, set overrun (D8). If 'buffer load' off, transfer RDR to buffer register (64-50, E4).
11. At end of RCV 27, turn on 'buffer load' FL (D8) and 'read response' FF (B8), activating 'level 1 interrupt request'.
12. Continue receiving until 'transmit' or 'end op' instruction turns off 'receive' FL (B3).
13. 'End op' fires the 1.0 ms delay SS to maintain 'busy' for the duration of the SS (64-40, E4).

'Start Read' Objectives - BSC

1. Recognize two successive idle-sync characters to establish 'character phase'.
2. Starting with first non-idle character, receive following characters and set them in buffer register.

'Start Read' Operation - BSC (64-60)

1. Turn on 'receive' FL (B3). If 'transmit' FL is off, activate 'receive mode' immediately. If 'transmit' is on, wait to activate 'receive mode' when 'transmit' turns off.
2. Fire receive mode start SS (64-40, A4). Activate 'all turn around' and 'reset clock T6 and RCV circuits' (C5) stopping clocks.
3. Reset controls for other operations. Turn off 'CP memory' FF and 'character phase' FL (A6 and C6).
4. On first mark to space transition, turn on 'clock gate' FL (64-20, B4) restart clocks. Use first transition circuits to ensure no false start from noise. (64-30, D4).
5. Start receiving and shifting bits through RDR, comparing RDR with idle-sync register. When idle-sync compare is equal turn on 'idle character' FL at RCV 27 (B6).
6. Activate 'set pseudo tag' (A7). Framing is complete.
7. If idle-sync compare is equal at the next RCV tag, turn on 'character phase' and 'CP memory' at RCV 25 (C6 and A6).
8. If idle-sync compare is not equal at the next RCV tag turn off 'idle character' FL at RCV 25 (B5). Do not turn on 'character phase' and 'CP memory'.
9. Continue comparison until idle-sync compare is equal when 'idle character' FL is on. Then turn on 'character phase' and 'CP memory' at RCV 25.
10. Continue receive operation as in steps 7-13 of STR.

'Read' Objectives - STR or BSC

1. Check for character gap.
2. Transfer a received character from the buffer register to CPU core storage.

'Read' Operation - STR or BSC (64-60)

1. During CPU E-3 cycle, transfer buffer to B register (64-50, E5).
2. At T6, if the 'buffer load' FL is off during 'character phase', activate 'character gap' and turn on 'check' FF (E7).
3. At the end of T6, turn off 'buffer load' FL (E6).

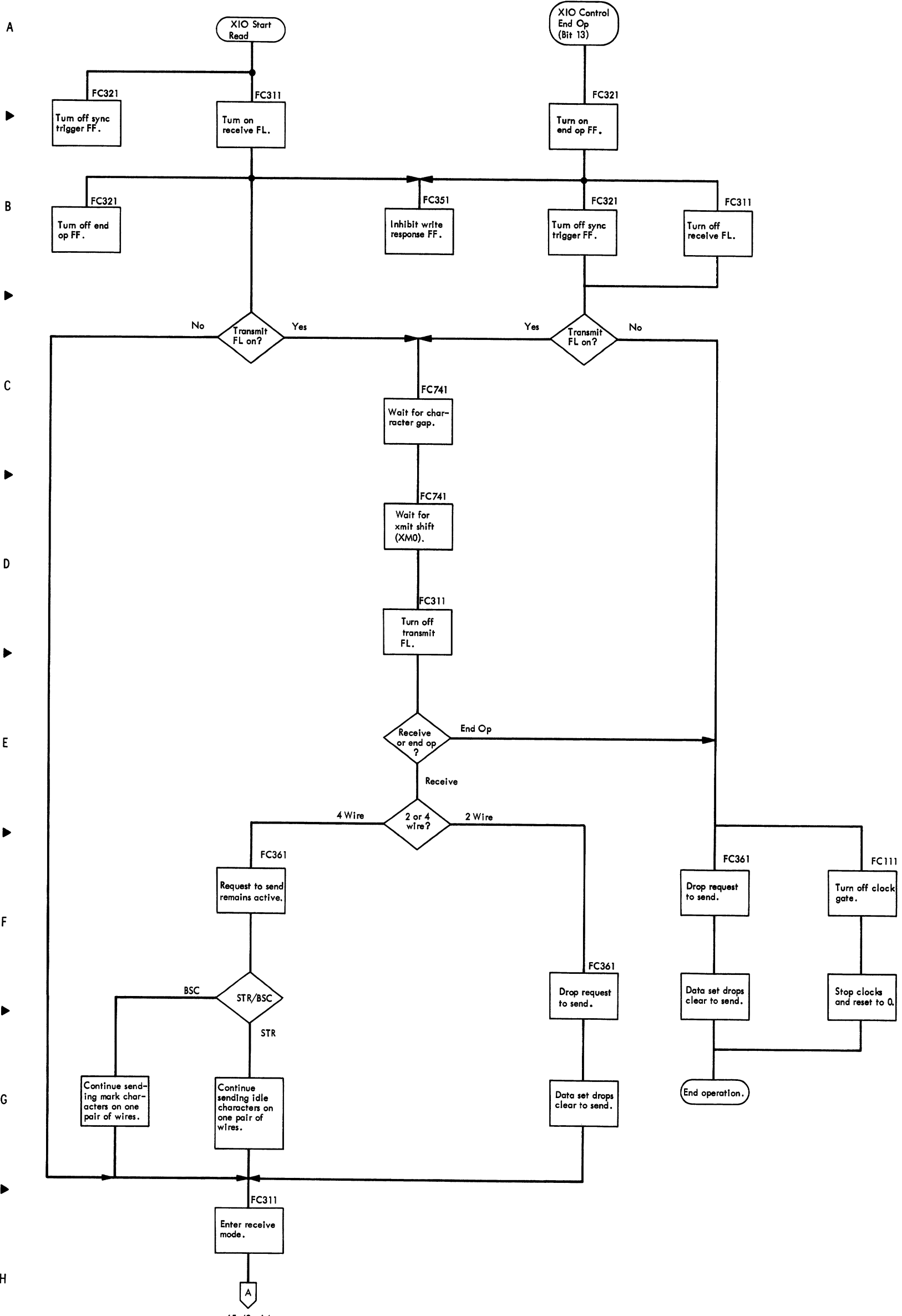
2

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6



65-40, A4

Diagram 65-30. Start Read (Part 1) and End Operation



A  
B  
C  
D  
E  
F  
G  
H

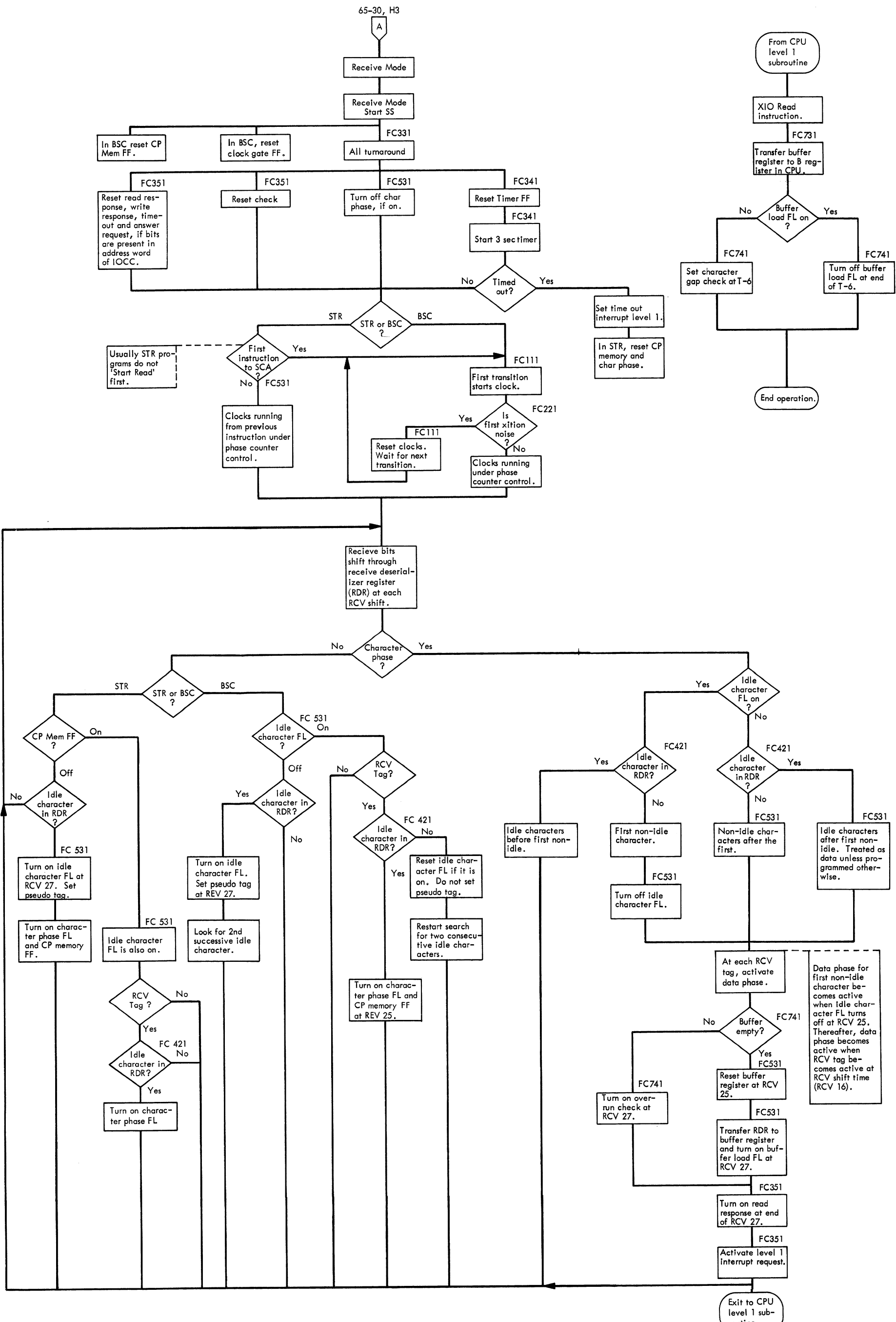


Diagram 65-40. Start Read (Part 2) and Read

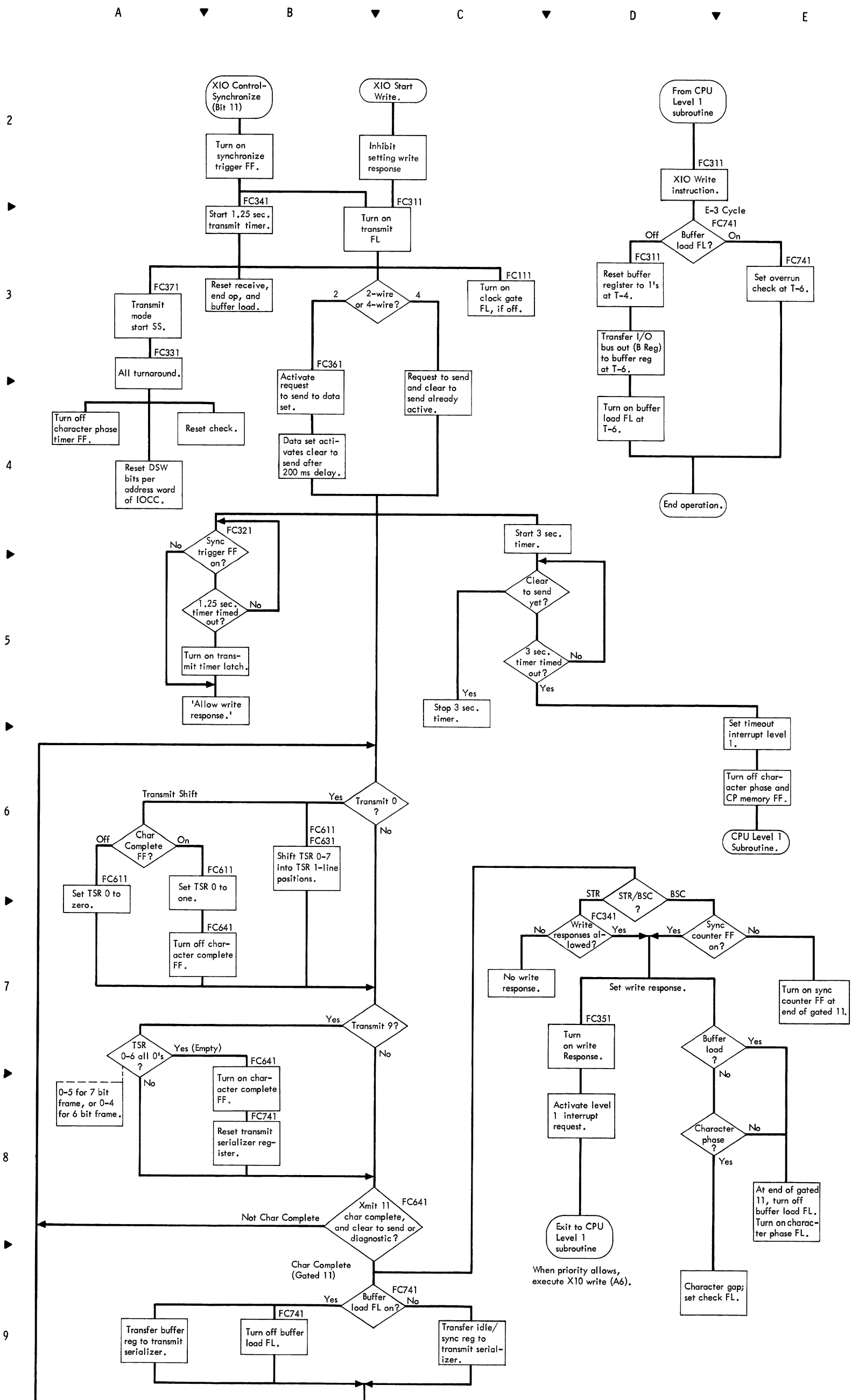
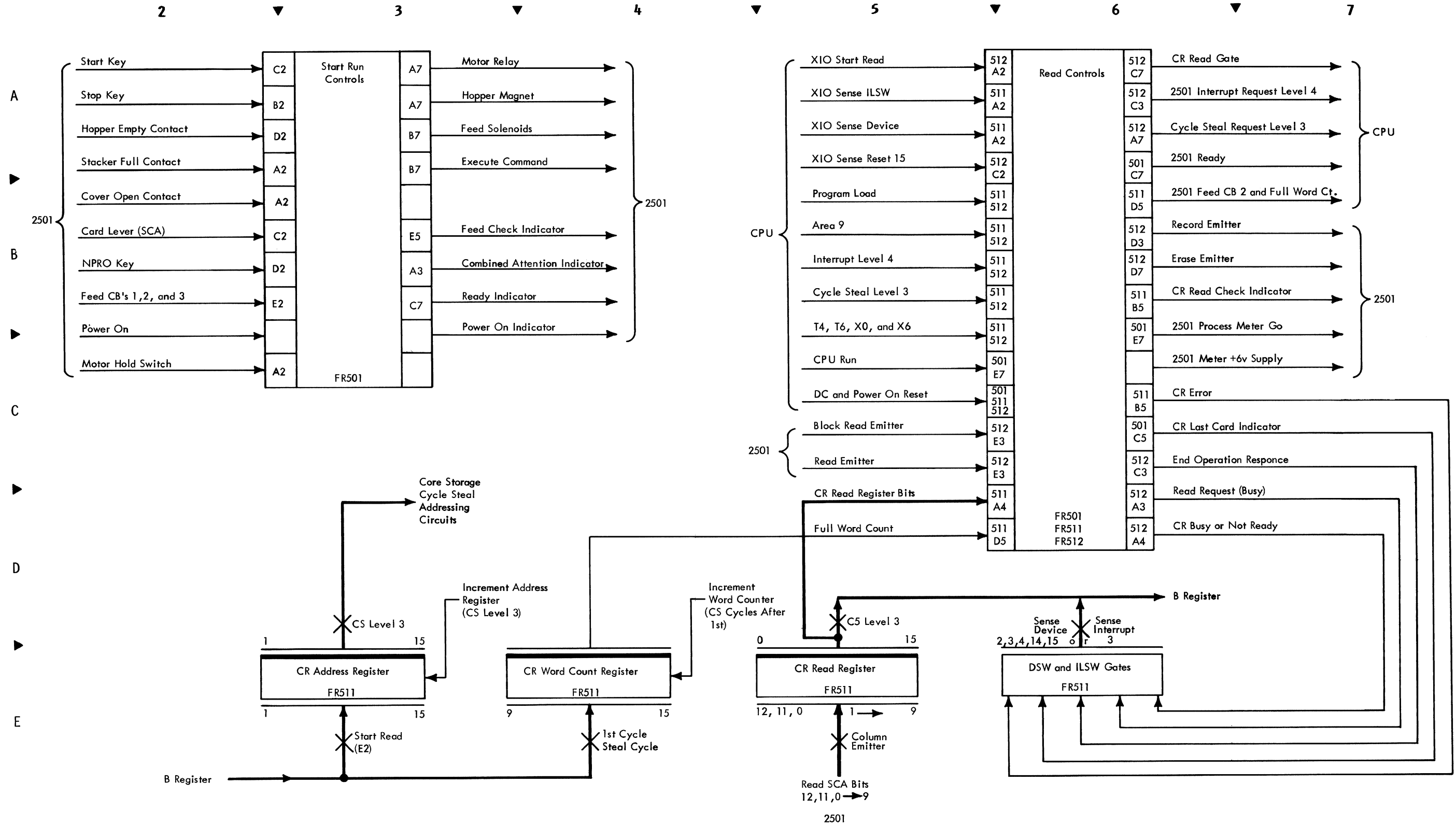


Diagram 65-50. Synchronize, Start Write, and Write

Diagram FR401. 2501 Card Reader Data Flow and Control



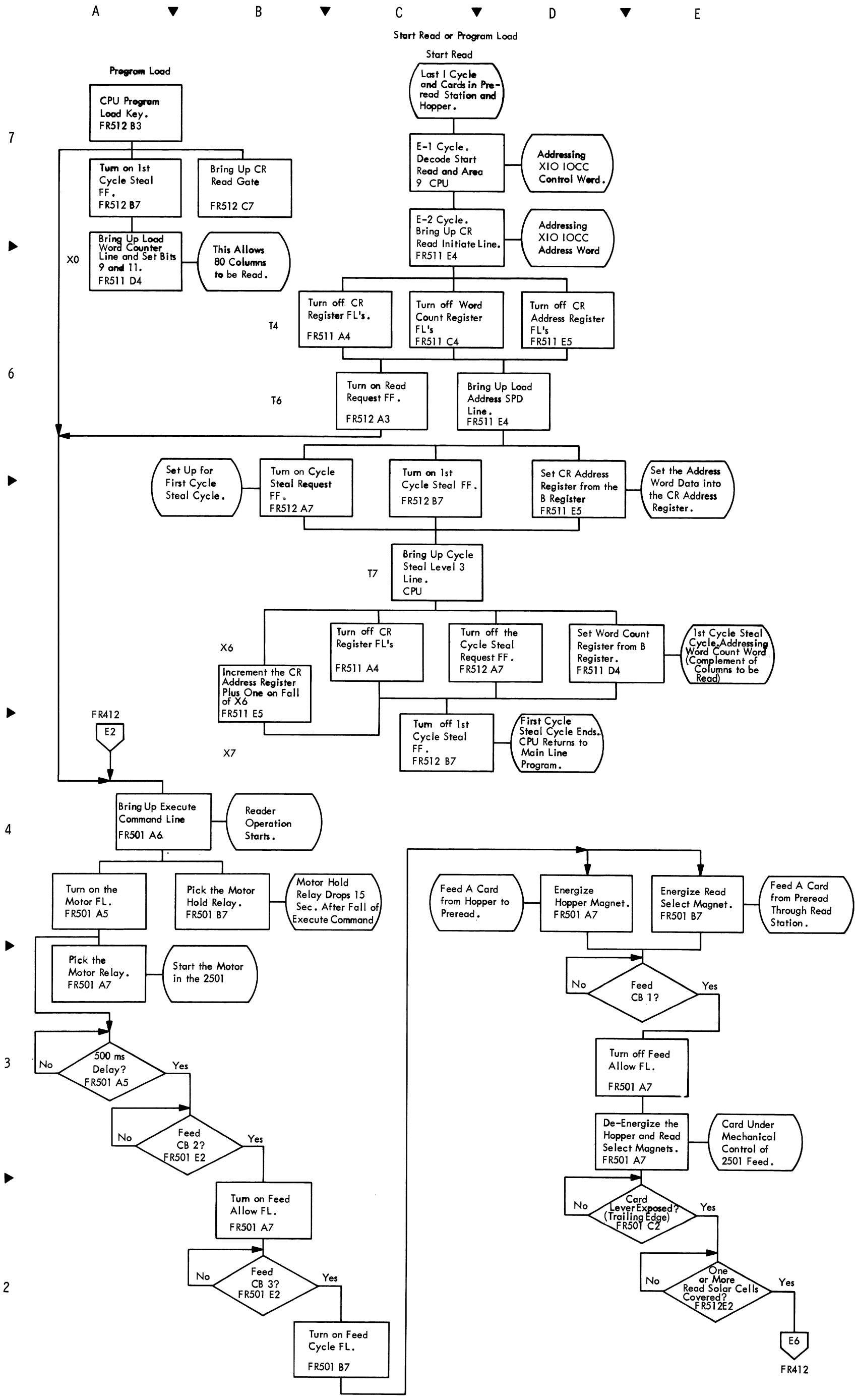


Diagram FR411. 2501 Start Read or Program Load (Part 1 of 2)

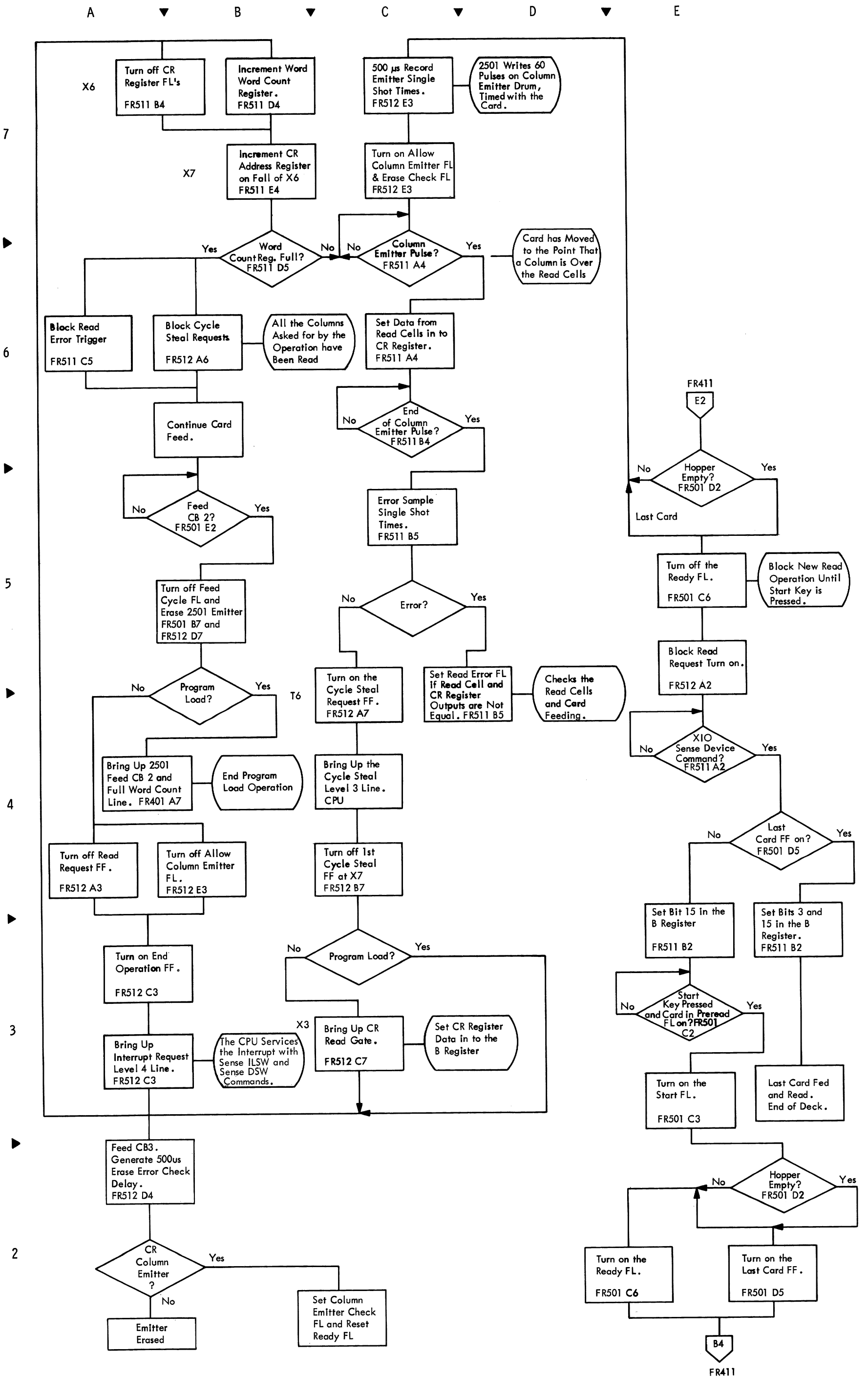


Diagram FR412. 2501 Start Read or Program Load (Part 2 of 2)

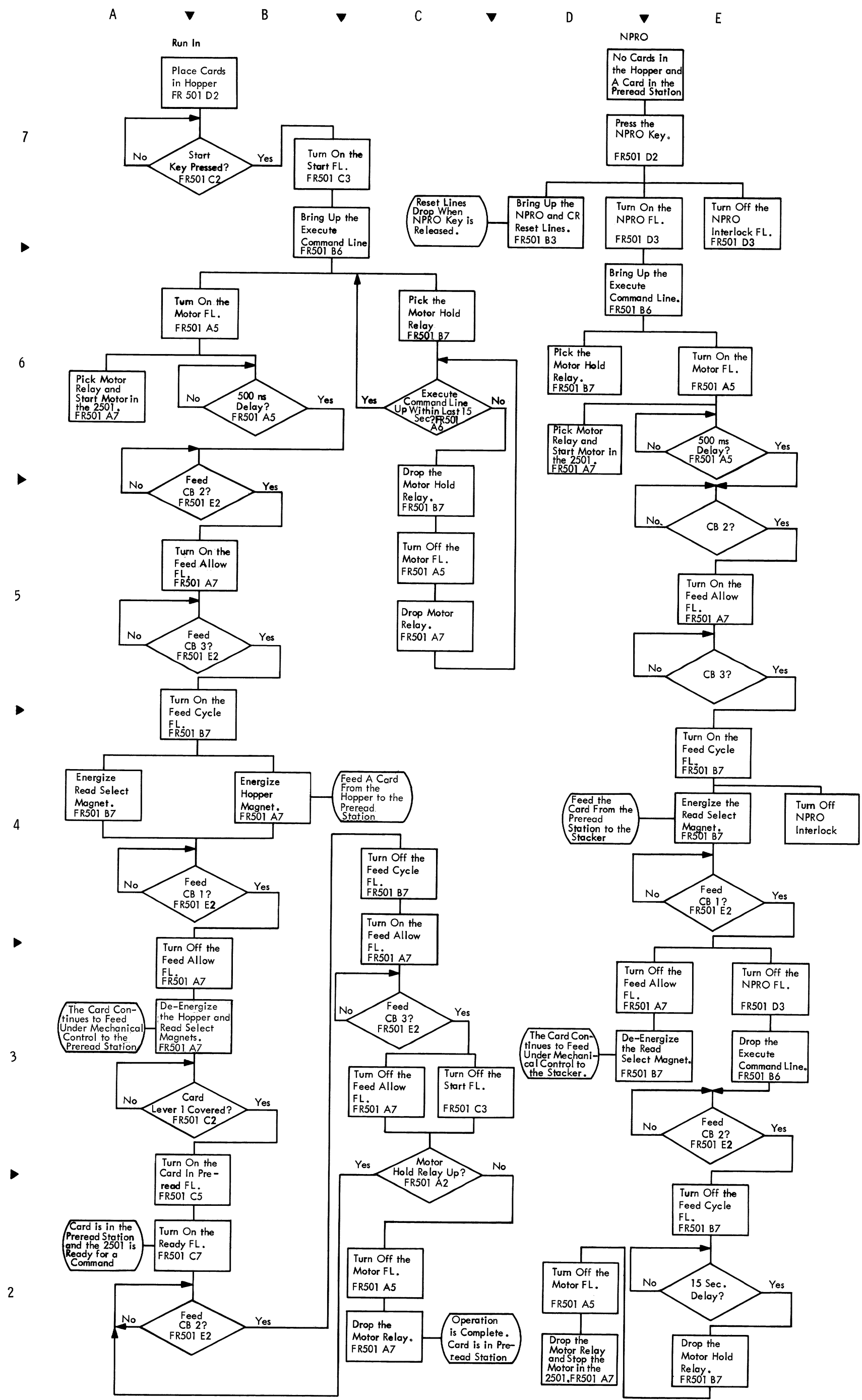


Diagram FR413. 2501 Run In - NPRO

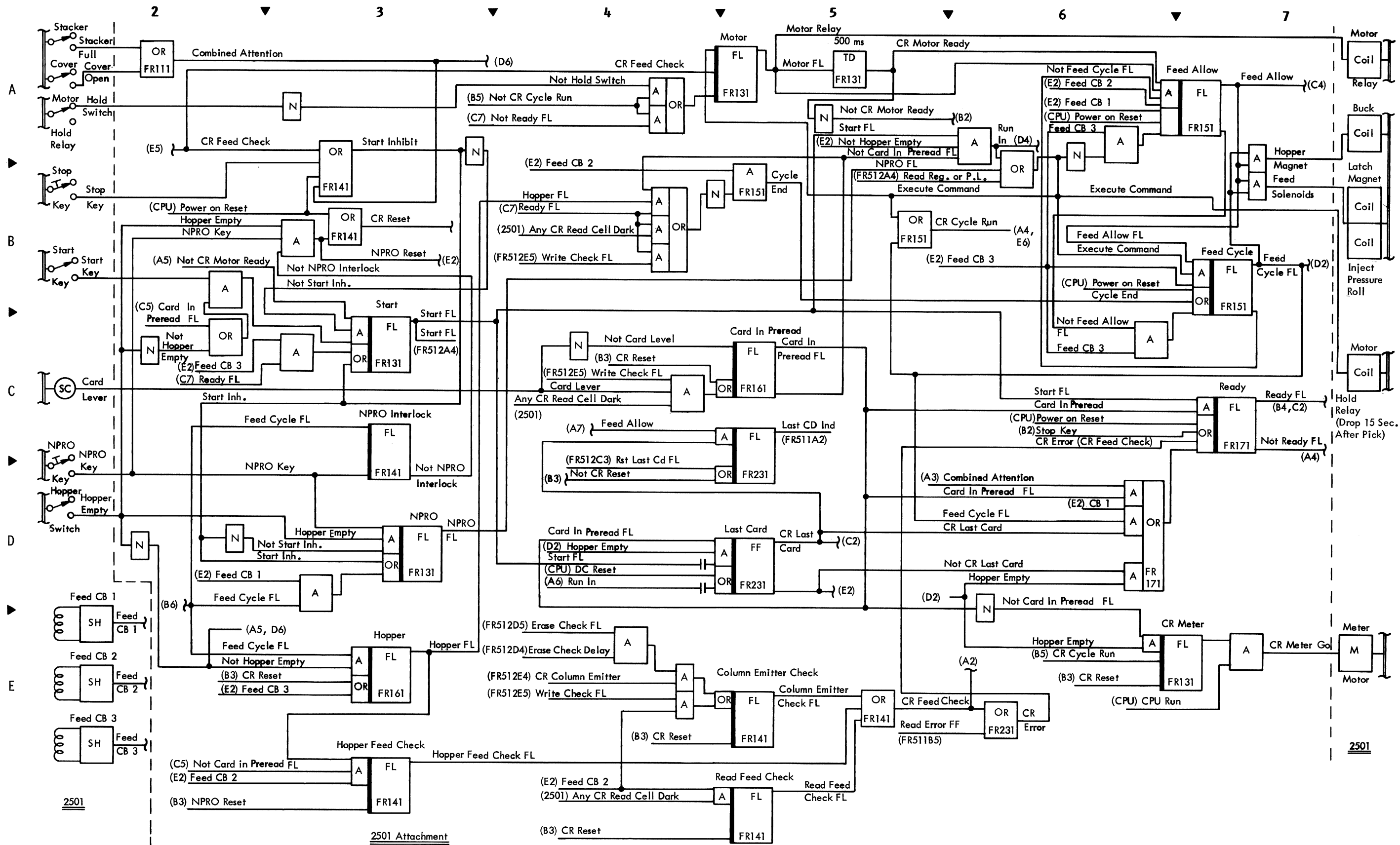
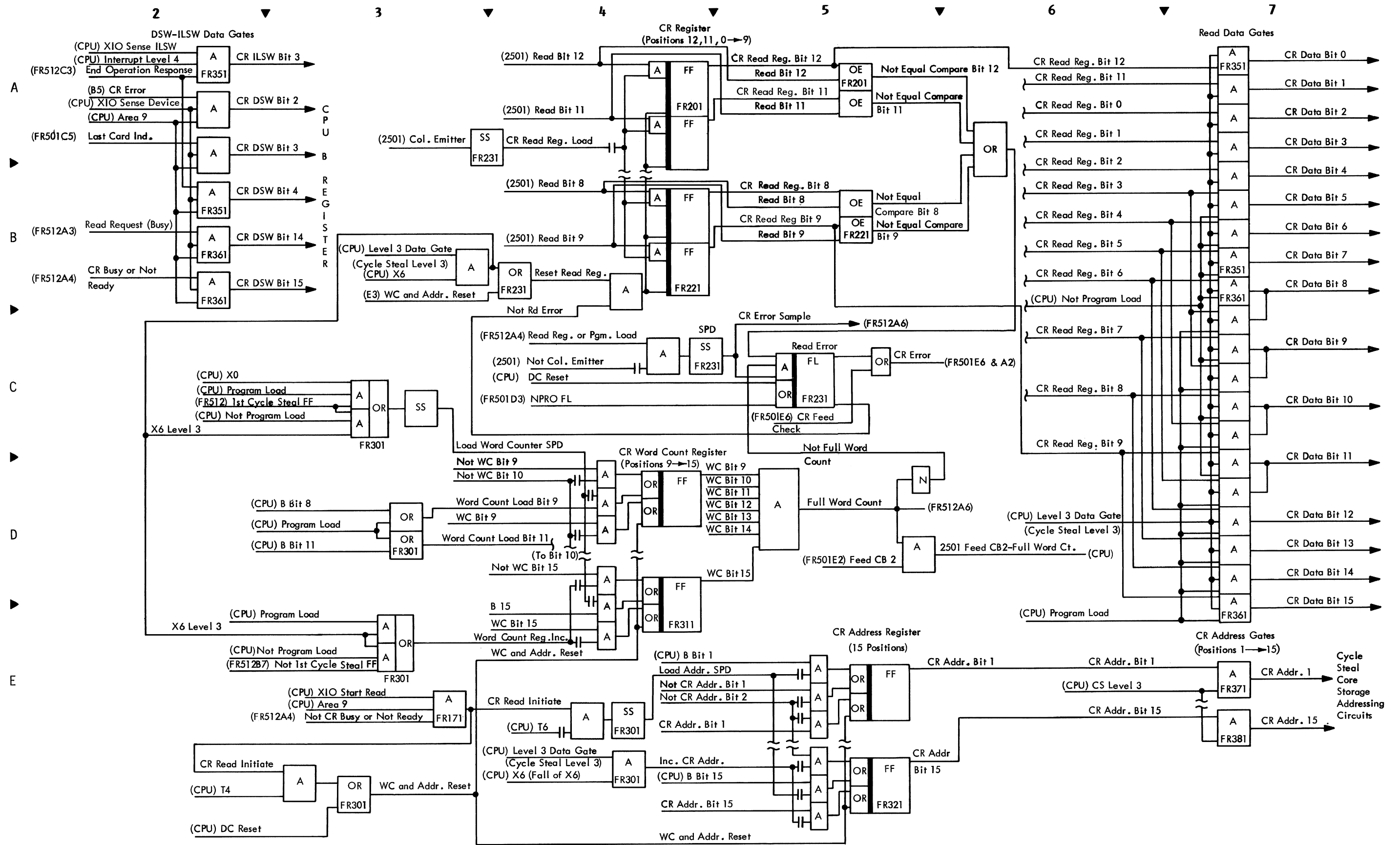


Diagram FR501. 2501 Start-Run

Diagram FR 511. 2501 Read (Part 1 of 2)





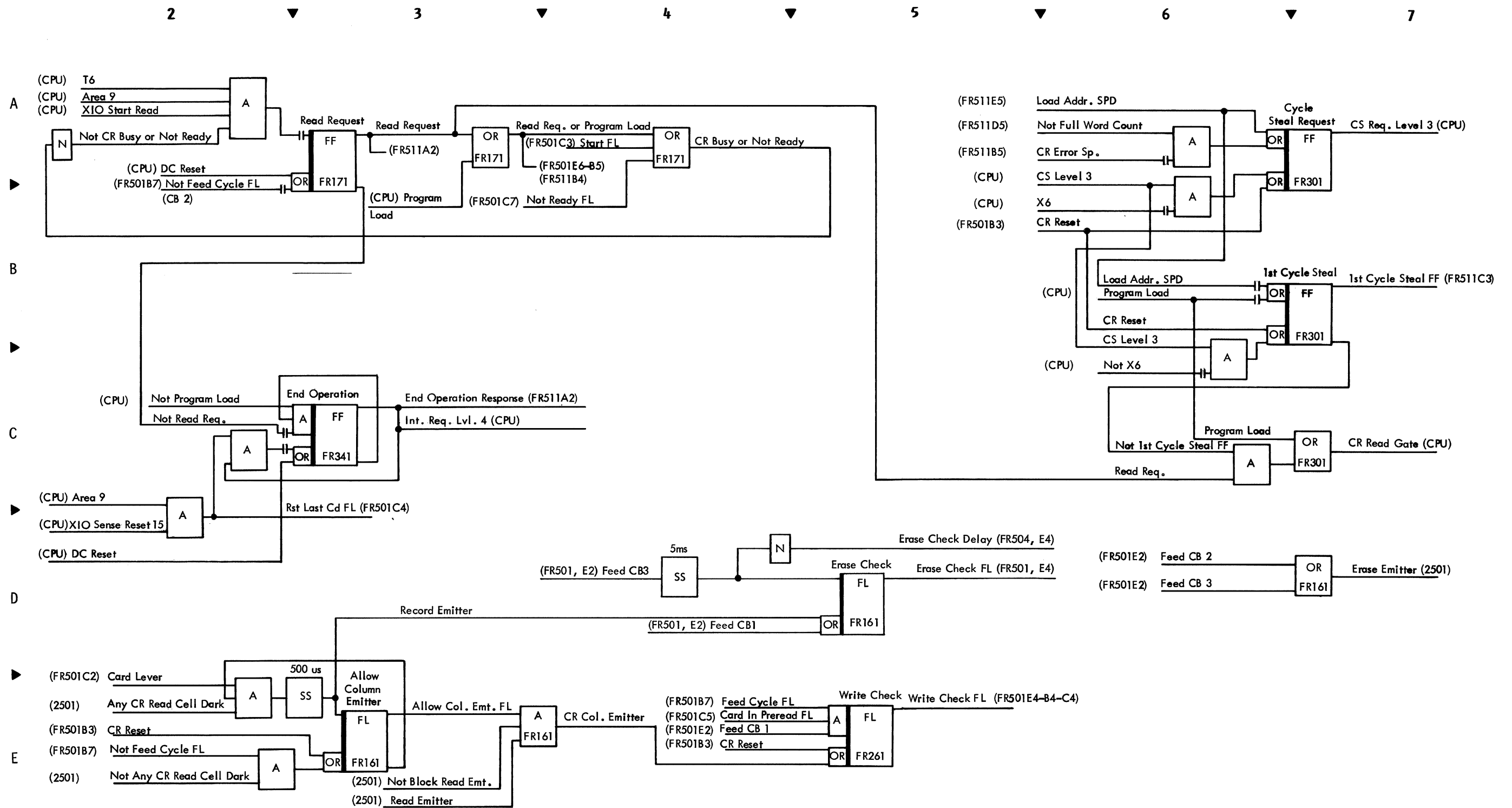
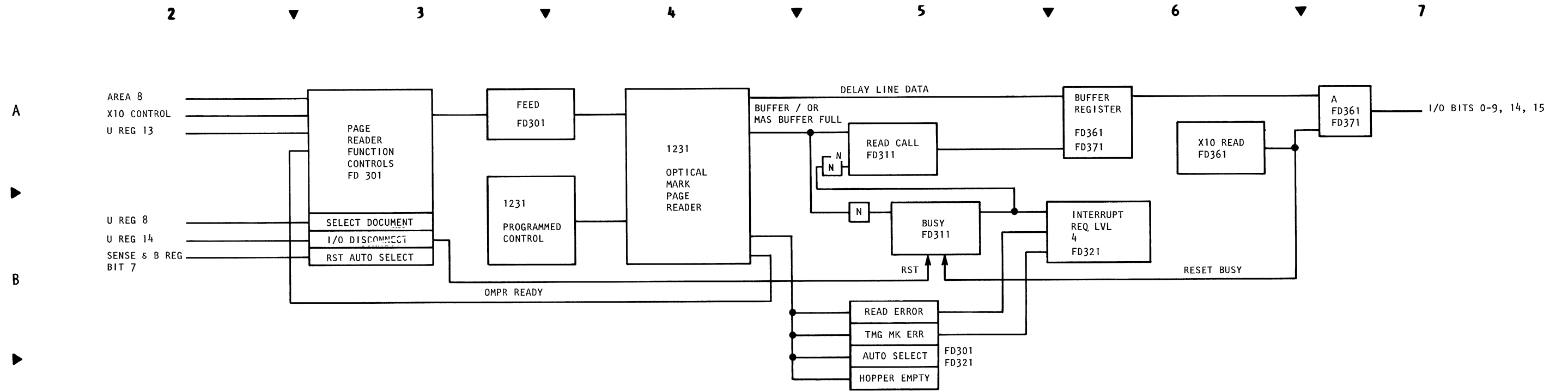


Diagram FR512. 2501 Read (Part 2 of 2)

Diagram 83-10. 1231 Data Flow and Control



B5		15	OMPR IS NOT READY	
C4		14	OMPR READ OP	
D6		13	READ BUSY	
	DSW AND ILSW BITS FOR 1231			
B7		10	CHECK STOP INT. REQ.	
B9		9	OMPR HOPPER IS EMPTY	
A9		FD301	8	OMPR TIMING MARK CHECK BUSY
B9		FD311	7	I/O SELECTED DOCUMENT (Auto Select)
B9		FD321	6	OMPR FEED BUSY
A9			5	OMPR OK TO SELECT DOCUMENT (Enable Select)
C6			4	OMPR OPERATION COMPLETE (End Op)
E6			3	MASTER MARK
C2			2	OMPR READ ERROR
C2		1	TIMING MARK CHECK	
D6		0	OMPR READ RESPONSE	
B9			1231 ILSW BIT 5	

Note: References in left column are co-ordinates for Diagram 84-10.

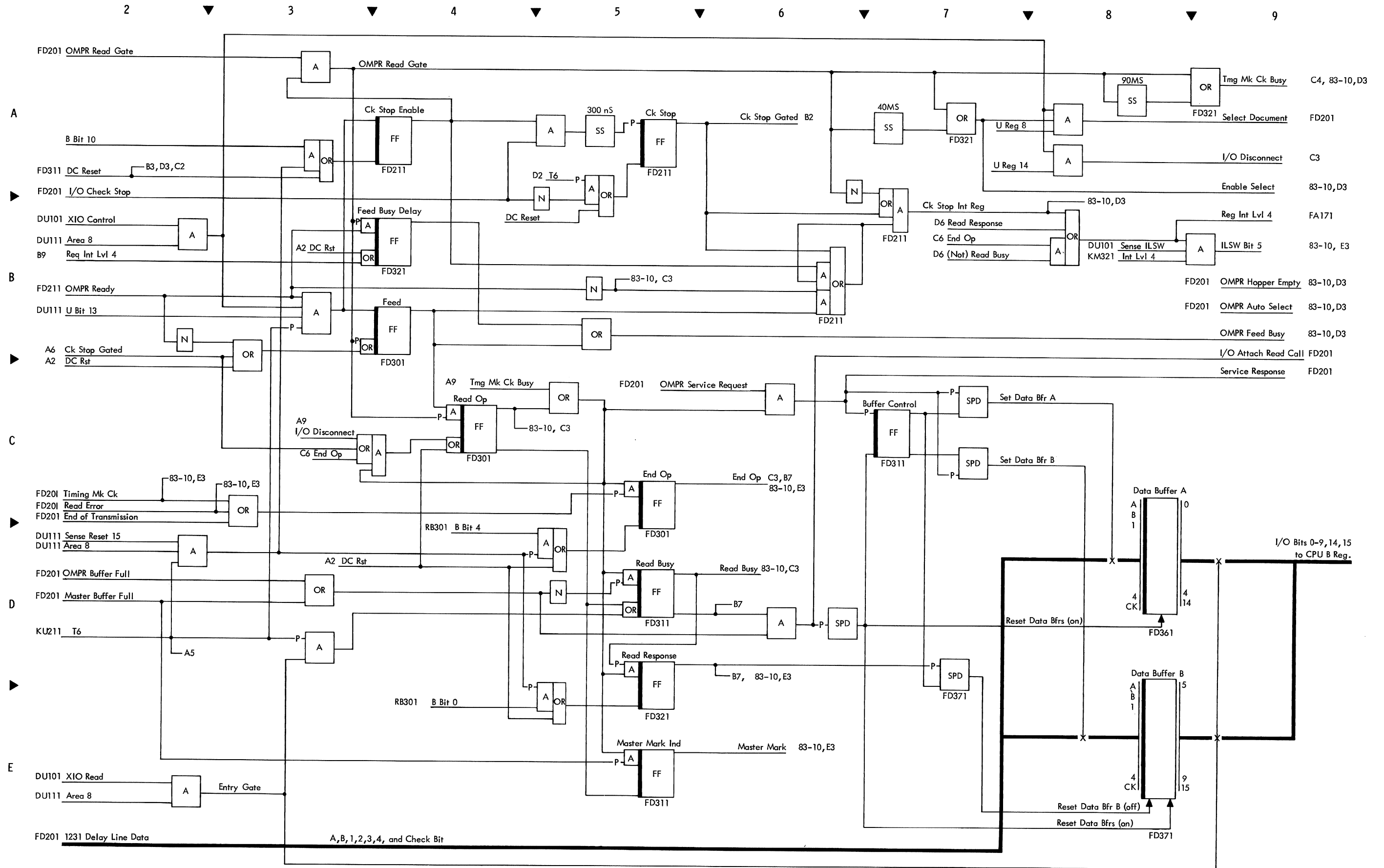


Diagram 84-10. 1231 OMPR Read

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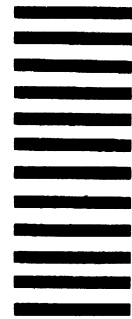
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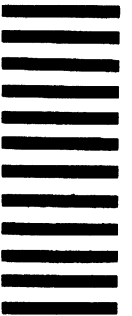
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