HP 3000 Computer Systems

HP 30240A

OfficeShare LAN/3000 Link

Local Area Network Interface Controller

(LANIC)

Installation and Service Manual

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with the user-inserted update information. New editions of this manual will contain new information, as well as updates.

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LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the date of the most recent version of each page in the manual. To verify that your manual contains the most current information, check the dates printed at the bottom of each page with those listed below. The date on the bottom of each page reflects the edition or subsequent update in which that page was printed.

Effective Pages	Date
All.	Nov 1985
2-1	May 1987
A-2/A-3	May 1987

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CONTENTS (continued)

SAFETY CONSIDERATIONS

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING **The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.**

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends on the type of material. Insulators can easily build up charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields.

The resulting damage can range from complete destruction to latent degradation. Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The LANIC card is shipped in a transparent static shielding bag. The card should be kept in this bag at all times until it is installed in the system. Save this bag for storing or transporting the card. When installing the card in the system, do not touch any components. Hold the card by its edges.

WARNING

SAFETY EARTH GROUND - The computer on which this product is installed is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety ground must be provided from the main source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, or before the power cord is removed from the wall receptacle, the AUI cable connector must be removed from the junction panel and insulated from exposed conductive surfaces.

WARNING

At infrequent intervals, exposed metal surfaces of the AUI cable may be subject to transient hazardous voltages due to strong electrical disturbances (such as lightning or disturbances in the electrical utilities power grid) in the area surrounding the network to which this product is connected. These surfaces should be handled with caution when the AUI cable is not connected to a properly grounded HP 3000 Computer System.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of assemblies within the HP 3000 cabinet must be performed only by qualified personnel.

WARNING

This product is not designed for attachment to a network serving an area which contains multiple unconnected power system safety grounds. Before installing this product, verify that all of the power system safety grounds are securely interconnected in the area served by the local network.

WARNING

Do not connect this product to an ungrounded network coaxial cable.

GENERAL INFORMATION

SECTION 1

INTRODUCTION

This manual presents installation and service instructions for the HP 30240A OfficeShare LAN/3000 Link Local Area Network Interface Controller. This section has general information about the HP 30240A OfficeShare LAN/3000 link product, and includes a description and specifications.

GENERAL DESCRIPTION

The HP 30240A OfficeShare LAN/3000 link is an implementation of the IEEE 802.2 and IEEE 802.3 Local Area Network (LAN) standards and is used in HP 3000 computer systems. The HP 30240A allows the HP 3000 to communicate with other HP 3000's over an IEEE 802.3, 0.18-inch baseband Local Area Network (LAN).

The IEEE 802.3 Local Area Networks (LAN's) consist of three major elements: a coaxial cable transmission medium, units to access this medium (Thin Medium Attachment Units, or Thin MAU's), and controllers. For the HP 30240A, the controller is the Local Area Network Interface Controller (LANIC).

The HP 30240A OfficeShare LAN/3000 link is available for use with the HP 3000 Series 39, 40, and 42; and the HP 3000 Series 44, 48 64, and 68. The LANIC and Thin MAU, are the same for all HP 3000 Series; however, two different LANIC cables are offered (see the paragraph "Equipment Supplied").

The LAN/3000 link functions as an intelligent Direct Memory Access (DMA) channel which communicates with the host system via the system I/O backplane. Local intelligent control is provided by a microprocessor and firmware on the LAN Interface Controller (LANIC). An 8-bit Z-80B microprocessor (MPU) on the LANIC handles all the LAN/3000-to-host communication and performs many link-level operations independently of the host. A type 82586 Local Communications Controller (LCC) on the LANIC performs high-speed serial operations, packet address checking, network contention control, packet formatting, and Cyclic Redundancy Check (CRC) generation and checking. The LCC is controlled by the Z-80B through local (card -resident) memory.

The LANIC, besides controlling the other LAN elements, also is the interface with the Local Area Network to the computer system. A typical Local Area Network is shown in Figure 1-1.

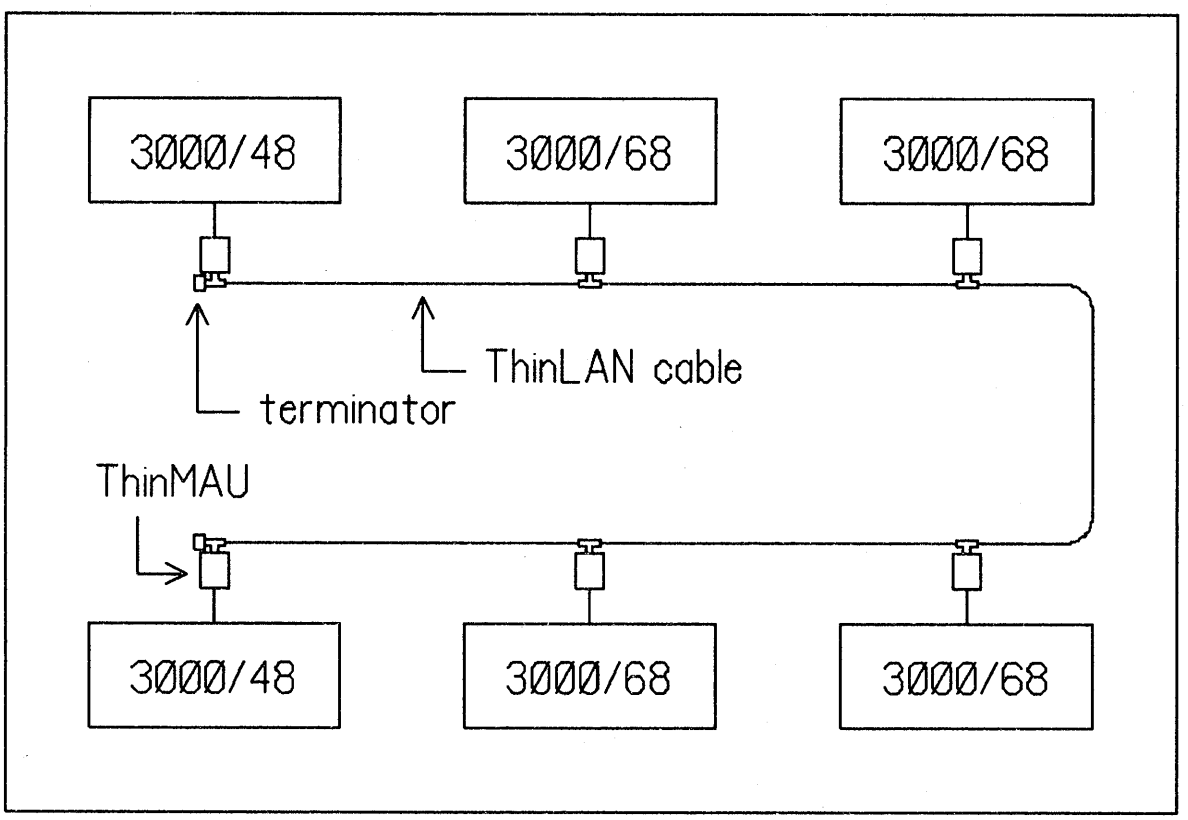


Figure 1-1. Typical Local Area Network (LAN)

Equipment Supplied

Standard equipment supplied with the HP 30240A is listed below:

Standard Equipment

1	Thin Medium Attachment Unit Assembly	28641-60001
1	BNC "T" Connnector.....	1250-0781
1	BNC "T" Boot.....	1252-1154
1	ThinMAU Installation Manual.....	28641-90001
1	LAN/3000 Installation and Service Manual	30240-90001

In addition, one of the following options (depending on the HP 3000 type) adds the following equipment:

Option 300 for the HP 3000 Series 39, 40, and 42

1	Series 4X/6X LAN Interface Controller (LANIC card)	30242-60001
1	Series 39/40/42 LANIC Internal Cable	30241-60002

Option 400 for the HP 3000 Series 44 and 48

1	Series 4X/6X LAN Interface Controller (LANIC card)	30242-60001
1	Series 44/48 LANIC Internal Cable	30241-60003

Option 500 for the HP 3000 Series 64 and 68

1	Series 4X/6X LAN Interface Controller (LANIC card)	30242-60001
1	Series 64/68 LANIC Internal Cable	30241-60003

Option 241 is specified if the Thin MAU is not desired. Option 241 deletes the following standard equipment:

Option 241

Deletes

1	Thin Medium Attachment Unit Assembly	28641-60001
1	BNC "T" Connnector.....	1250-0781
1	BNC "T" Boot.....	1252-1154
1	ThinMAU Installation Manual.....	28641-90001

System Interface

As noted previously, the LAN/3000 link interfaces to the host computer system through the LAN Interface Controller (LANIC). The LANIC functions as an I/O channel and fits into the backplane of HP 3000 Series 39, 40, 42, 44, 48, 64, and 68 computers.

Figure 1-2 shows how the LANIC connects to a Series 39, 40, 42, 44, or 48 computer system. The CPU, Memory, Asynchronous Data Communications Controller (ADCC) or Advanced Terminal Processor (ATP), General Input/Output Controller (GIC), Intelligent Network Processor (INP), and LANIC all physically fit into the backplane (the backplane is called the Intermodule Bus (IMB)).

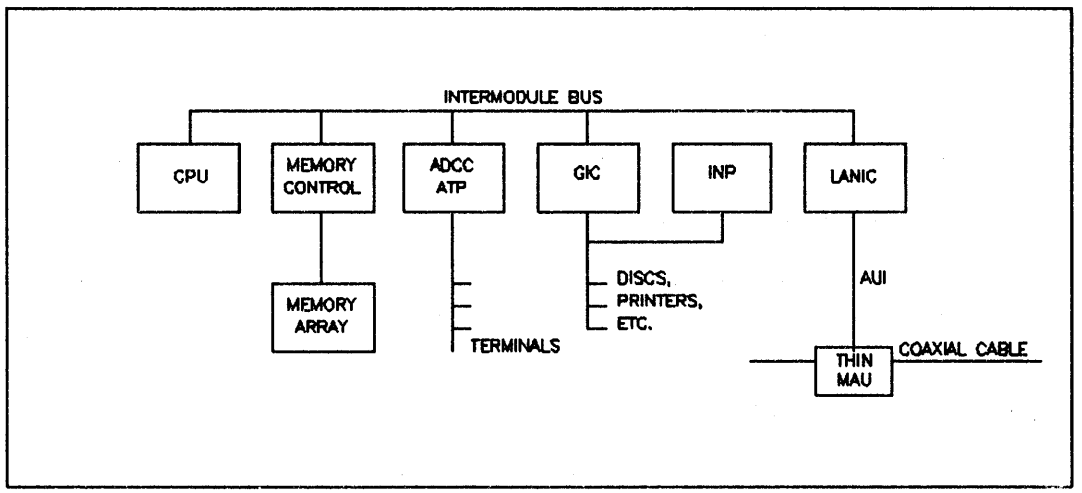


Figure 1-2. HP 3000 Series 39 through 48 System Architecture

The architecture for the Series 64 and 68 computers is significantly different than the other HP 3000 series, as shown in figure 1-3. The CPU and memory fit into the Central System Bus (CSB), and one or more IMBs connect to the CSB via Common Bus Interfaces (CBI's) and IMB Interfaces (IMBI's). I/O DMA operations do not go directly to memory, but are handled by the IMBI.

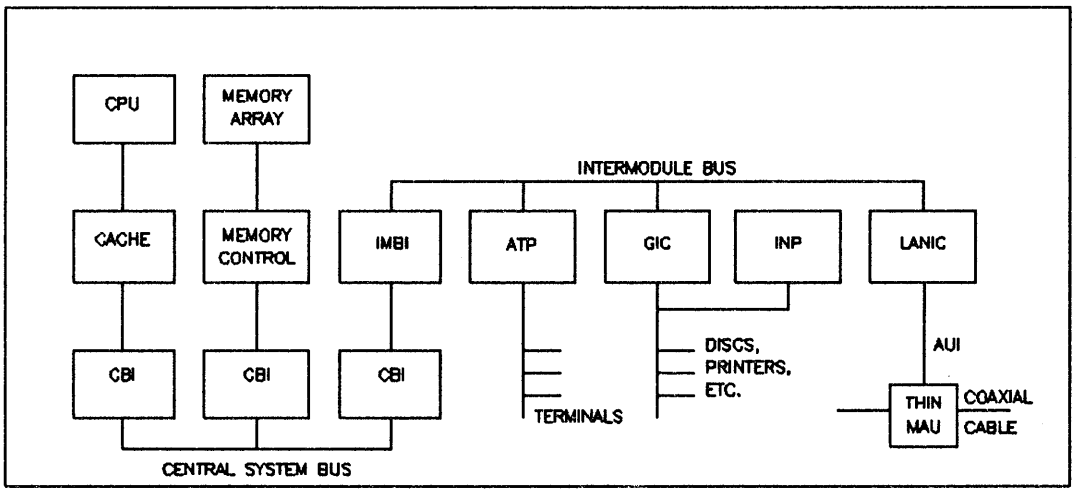


Figure 1-3. HP 3000 Series 64 and 68 System Architecture

Link Address

The last six hexadecimal digits of the link level address for the LANIC are indicated on the board stiffener to the left of the channel address switch (CHAN ADDR) on a label titled "Station Address". The full address is 08 00 09 XX XX XX, where XX XX XX represents the value on the label.

SPECIFICATIONS

Table 1-1 lists the specifications of the HP 30240A LAN/3000 link.

Table 1-1. Specifications

FEATURES

Compatible with IEEE 802.3 Standard for access to 0.18-inch diameter baseband coaxial cable

Carrier-Sense Multiple Access with Collision Detection (CSMA/CD) protocol controls network access using no master node

On-board node self-test that checks the operation of the node hardware including the Thin MAU

Every node on the network cable is accessible by any other node on the network with no store and forward

10 megabit-per-second hardware data transfer rate

Each 185-meter cable segment supports up to 30 nodes

VLSI implementation for reliability and lower cost

Microprocessor off-loads host computer and gathers network statistics

ELECTRICAL CHARACTERISTICS

Data Rate:

Transmitted in bursts of 10 Mbits/sec

Maximum Coaxial Cable Length:

185 meters for one segment

Maximum Distance from Node to Network Trunk:

One meter maximum for external AUI cable.

Required Distance Between T's on Coaxial Cable Trunk:

Each Thin MAU must be located on the coaxial cable at least 0.5 meter apart.

Table 1-1. Specifications (Continued)

LANIC at AUI Connector:

AUI signalling conforms to IEEE 802.3

CO not driven

VP +12V +/-6% @ 0.5A; overcurrent protected @ 1.2A maximum

Interframe spacing = 9.6 usec minimum

Thin MAU at AUI Connector:

AUI signalling conforms to IEEE 802.3

CO terminated but unused

Operating voltage: 8.0V to 13.50V at 360mA maximum

ThinMAU at Coaxial Cable:

Coax signalling compatible with IEEE 802.3 recommended signalling levels

Receiver based collision detection

Compatible with any coaxial cable meeting IEEE 802.3 type 10, base 2 physical specifications

Table 1-1. Specifications (Continued)

LANIC PHYSICAL CHARACTERISTICS

Size: 331 mm long by 285 mm wide by 22.5 mm thick
(13.04 by 11.2 by 0.89 inches)

Weight: 739 grams (26 ounces)

LANIC POWER REQUIREMENTS

Voltage	Current	Power Dissipation
+5V +/-0.5V	4.7A	23.5W
+12V +/-0.6V	0.5A	6.0W (Thin MAU attached)

THIN MAU PHYSICAL CHARACTERISTICS

Size: 152 mm long by 114 mm wide by 25 mm thick
(6.00 by 4.50 by 1.00 inches)

Weight: 0.90 kg (2.0 lbs)

THIN MAU POWER REQUIREMENTS

8.0 to 13.50 volts
0.360 ampere maximum

ENVIRONMENTAL SPECIFICATIONS

Complete environmental specifications are in the
LAN Cable and Accessories Installation Manual
(Manual part number 5955-7680).

INSTALLATION

SECTION 2

INTRODUCTION

This section contains information on installing and verifying proper operation of the LANIC card, part number 30242-60001. Information on installing the ThinMAU is in the *LAN Cable and Accessories Installation Manual, part number 5955-7680.*

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

CURRENT REQUIREMENTS

The LANIC circuit card obtains its operating voltages from the host computer. The current requirements of the card are listed in the power requirements entry of table 1-1.

All HP 3000 Computer systems can supply adequate current to accommodate the LANIC card without the need for any power supply modification. However, it is possible that the +12V supply in the HP 3000 system may be set to a low voltage such that the VP lead on the AUI cable may not provide the minimum voltage specified by IEEE 802.3 (+11.28V). If MAU replacement does not correct an apparent MAU problem, the VP voltage should be checked. This is done by connecting an accurate voltmeter between the +12 and GND test points near the LED's on the LANIC card. This must be done when the MAU is connected to the LANIC and MAU power is on (as indicated by the VP LED). MAU power can be turned on by executing the LANIC self-test. Consult the HP 3000 CE Handbook for instructions on adjusting the +12V power on the HP 3000.

CHANNEL ADDRESS SWITCH

For the LANIC card, the channel address is set by a CHAN ADDR rotary switch, SW2, located on the front edge of the card. See figure 2-1 for the location of SW2. SW2 can be set to any value between 1 and 15, however, ensure that no GICs, ADCCs, or SIBs are set to the same channel number. While it is physically possible to set the address switch to values 1 to 15, you should exercise some caution in your choice of channel number. For instance, in all HP machines, it is assumed that the console has a DRT of 8. Therefore, choosing to make the LANIC channel address of 1 in a 4X, 5X, or in the first IMB of a 6X/7X machine will cause problems. Once you have set SW2 to a value, jot the value down. The formula used to calculate the DRT number from the hardware address is: (IMB# x 128) + (channel# x 8) + device #.

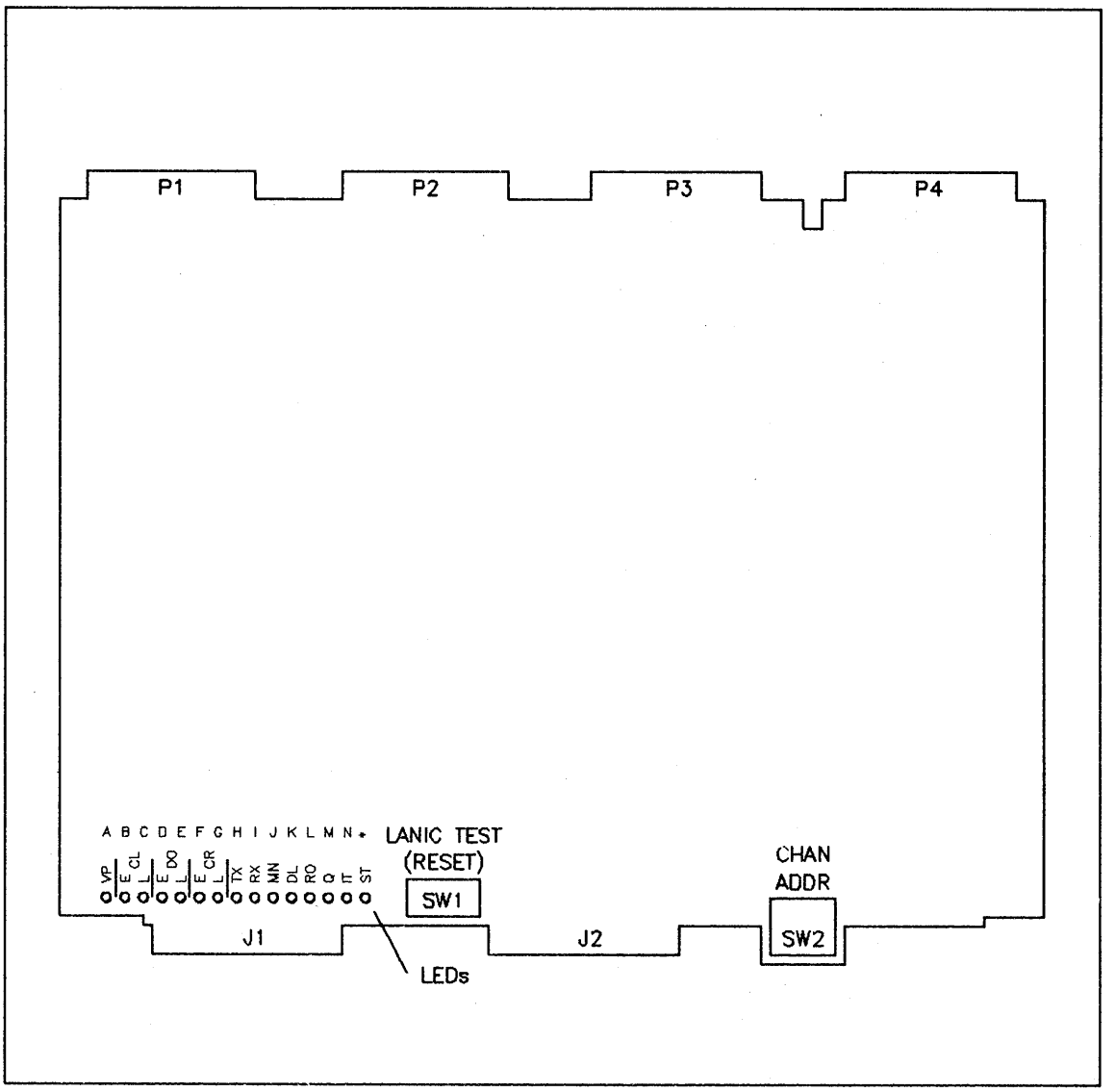


Figure 2-1. LANIC Switch and LED Locations

CABLES

Two cables are used to connect the LANIC to the MAU: an internal LANIC cable and the ThinMAU AUI cable. The LANIC cable has a hood connector on one end and a female 15-pin D connector on the other. A cabling diagram for the LANIC cable is shown in figure 2-2. The AUI cable uses a male 15-pin D connector on one end; the other end is wired directly into the ThinMAU. A cabling diagram for the AUI cable is shown in figure 2-3.

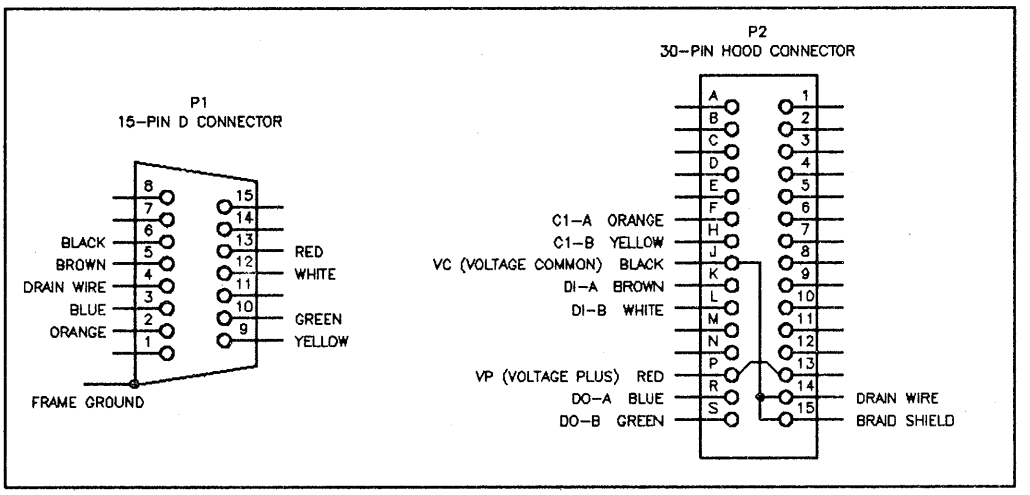


Figure 2-2. LANIC Cable Diagram

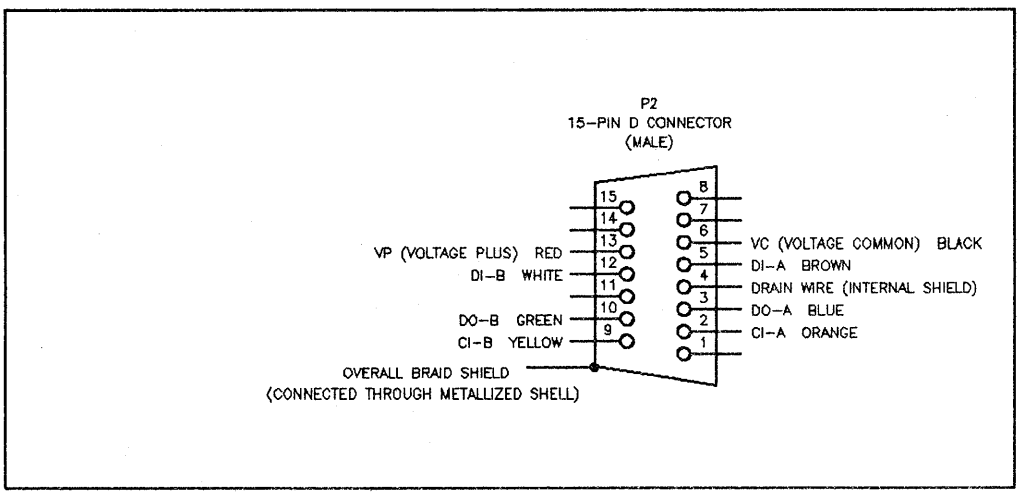


Figure 2-3. AUI Cable Diagram

INSTALLING THE LANIC

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

Install the LANIC as follows:

CAUTION

ALL SYSTEM POWER MUST BE OFF WHEN INSTALLING OR REMOVING ANY DEVICE OR CARD IN THE SYSTEM.

1. Before installing the LANIC, perform a full HP 3000 backup.
2. Shut down MPE.
3. Ensure that SW2 is set to the intended channel address. (It may be useful to obtain an IOMAP of all devices presently on the system. Refer to the *HP 3000 System Operation and Resource Management Reference Manual, part number 32033-90005* for details.)
4. Turn off all system power.
5. Open the door of the I/O section card cage on the back of the HP 3000 Computer system.
6. Insert the LANIC card into a vacant card cage slot as follows:

   The LANIC is considered to be a high-speed channel and, as such, must be configured so that its priority is higher than any GIC. Priority is established by the position of I/O cards in the card cage; the closer to the CPU (or the IMBI in the case of the Series 64 and 68), the higher the priority.

   Series 39, 40, 42. The LANIC can be installed in any slot in the range of 13 through 25. The adding of the LANIC card may require the movement of cards in the card cage to give the LANIC the required relative priority.

   Slots 13 and 14 are unique in the Series 39, 40, and 42 in that they are interdependent upon slot 15 in some situations. Specifically, if either a GIC, SIB, or LANIC occupies slot 13 and/or 14, and if slots 16 through 25 have one or more GICs, SIBs, or LANICs, then a GIC, SIB, or LANIC *MUST* be in slot 15.

   Note that the card in slot 15 need not be identical to the others under consideration. For instance, if a GIC is in slot 13, and a GIC, SIB, or LANIC is in 16 through 25, then any one of the three may be installed in 15.

   If ADCCs are installed in 13 and 14, as is commonly the case, there are no special considerations involving slot 15.

Series 44 and 48. The LANIC can be installed in any slot in the range of 14 through 24 (card cage 1) and any slot in the range of 1 through 7 (card cage 2). The adding of the LANIC card may require the movement of cards in the card cage(s) to give the LANIC the required relative priority.

Series 64 and 68. The LANIC must be installed in the I/O portion of the card cage. The adding of the LANIC card may require the movement of cards in the card cage to give the LANIC the required relative priority.

Special considerations apply to the placement of GICs, SIBs, and LANICs in Series 64 and 68 systems:

Between a GIC, SIB, or LANIC, and the next GIC, SIB, or LANIC, there may be a maximum of nine slots.

The "next" card need not be identical to its neighbor as long as it is one of the three types (GIC, SIB, or LANIC)

As an example, an SIB in slot 10 with a LANIC in slot 21, and GICs in slots 22 and 23, is not legal because there are greater than nine slots between the SIB and the LANIC. (The device cards such as INPs, AIBs, etc., do not matter in this case.)

An SIB in slot 10, LANIC in slot 17, and GIC in slot 22 is legal because there are nine or fewer slots between each card.

Finally, this limitation does not span IMBs. Each IMB must conform only individually.

7. Record the location of the LANIC in the configuration section of the System Support Log.

8. Connect the hood connector of the appropriate LANIC cable (part number 30241-60002 for Series 39, 40, and 42; part number 30241-60003 for Series 44, 48, 64, and 68) to connector J2 of the LANIC card. Connect the other end of the LANIC cable as follows:

   Series 39, 40, 42. Fasten the LANIC cable connecting box to the grounding strip at the bottom of the SPU (system processor unit) frame with the captive thumbscrew attached. Be sure the raised mounting lug is inserted in a hole in the grounding strip. Tighten the thumbscrew securely. Connect the ThinMAU AUI cable to the LANIC cable connector. See figure 2-4.

   Series 44 and 48. Fasten the LANIC cable connector, with its mounting panel attached, to the junction panel on the side of the card cage. Use only cutout numbers 2, 3, 5, 6, 7, or 8 for the LANIC cable. Connect the ThinMAU AUI cable to the LANIC cable connector. See figure 2-5 for details.

   Series 64 and 68. Fasten the LANIC cable connector, with its mounting panel attached, to the junction panel on the side of the card cage. Connect the ThinMAU AUI cable to the LANIC cable connector. See figure 2-6 for details. Note that the junction panel on Series 64 and 68 systems consists of two sets of 24 slots with a cable trough above and below each set. In each set of 24 slots, there are 12 upper and 12 lower slots. The LANIC internal cable should be installed in one of the lowest 12 slots with the ThinMAU AUI cable routed through the lower cable trough.

START UP AND VERIFICATION

For start up and preliminary verification of the LANIC, perform the following:

1. Turn on computer system power.

2. A self-test on the card, will execute at power on. There are 15 LED's on the front edge of the LANIC card (see figure 2-1). The seven LED's on the top are used to indicate activity on the AUI cable. The eight LED's on the bottom are used by self-test.

   The power-on self-test begins with all eight self-test LED's blinking on and off in unison for approximately 10 seconds. Thereafter, the bottom LED (labeled "ST") is lit to indicate that the self-test is in progress, and the remaining seven self-test LED's will perform a binary count, incrementing from 0000001 to 0101110 and executing a self-test for each binary code displayed. Some tests require several seconds to execute, some tests require much less, but the LED's will be lit for at least 100 milliseconds for every test, thus each code will be visible as the LED's increment the count. No binary codes are skipped. The binary codes and the self-tests they represent are listed in Section 4.

   Watch the LED's as the self-test program executes. If the self-test completes with no errors, the ST LED will be on and the other seven LED's will be off (a code of all zeros) for five seconds. After five seconds, the ST LED will go off, and the remaining LED's will reflect activity on the LANIC. If the self-test fails, the code of the test that failed will be displayed for a minimum of 20 seconds. This display will continue until the system accesses the link, while the self-test LED blinks slowly.

   Note that if the self test indicates failure 36H or 46H, this could indicate that the ThinMAU is not connected. Verify that it is connected. If the failures are still indicated, the error could be in the ThinMAU, or the coaxial cable. If the LANIC fails self-test, refer to Section 4 for maintenance procedures, and for further information on the self-test.

3. Start up the system in accordance with the procedures contained in Appendix A of this manual and in the *HP 3000 System Operation and Resource Management Reference Manual, part number 32033-90005.*

4. Run the LAN diagnostic on the LANIC/ThinMAU combination. Refer to the *LAN/3000 Diagnostic and Troubleshooting Guide, part number 30242-90003* for information on running the diagnostic.

RESHIPMENT

If any item of the LAN/3000 link is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the item being shipped.

Pack the item in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

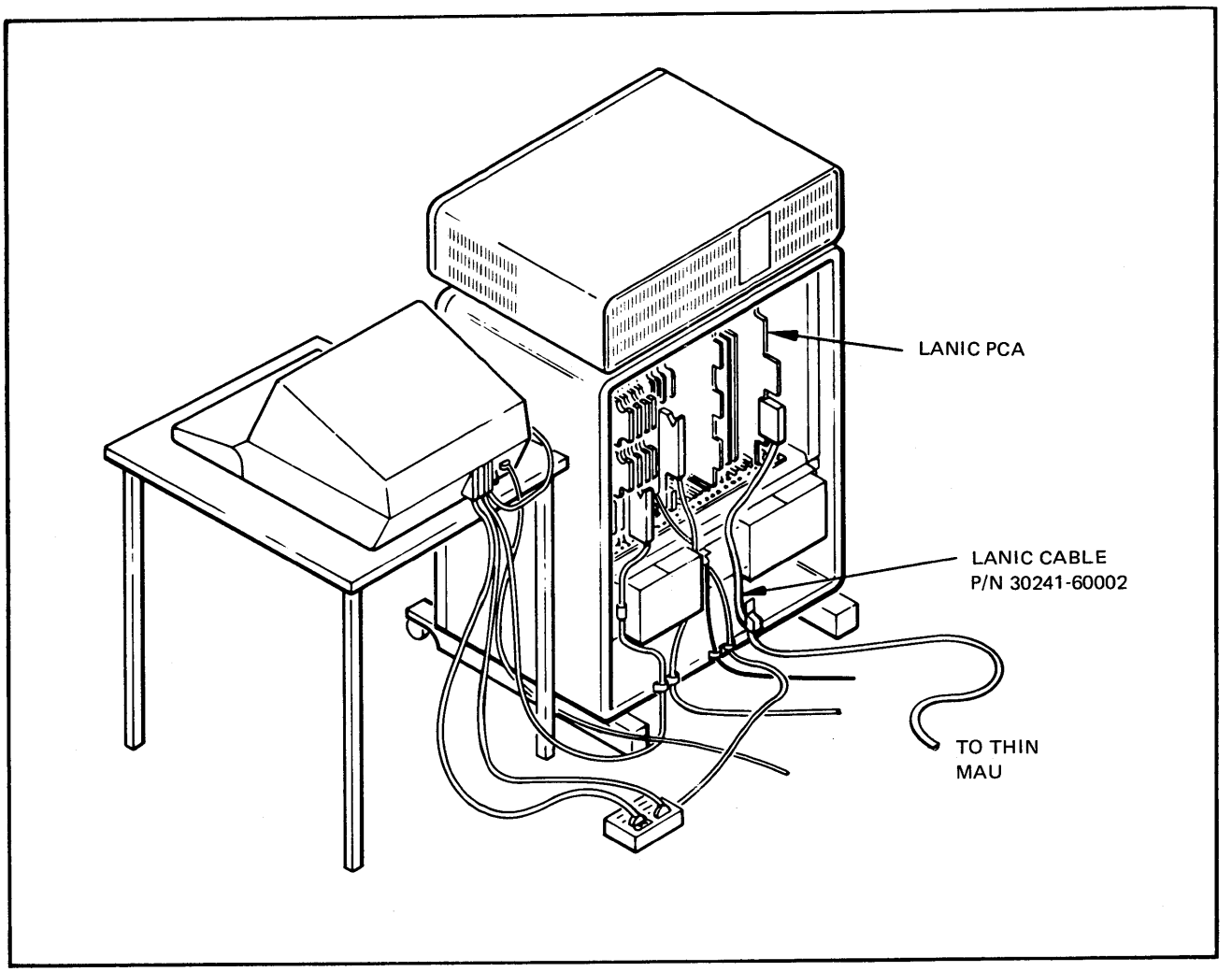


Figure 2-4. Series 39, 40, and 42 LANIC Cabling Detail

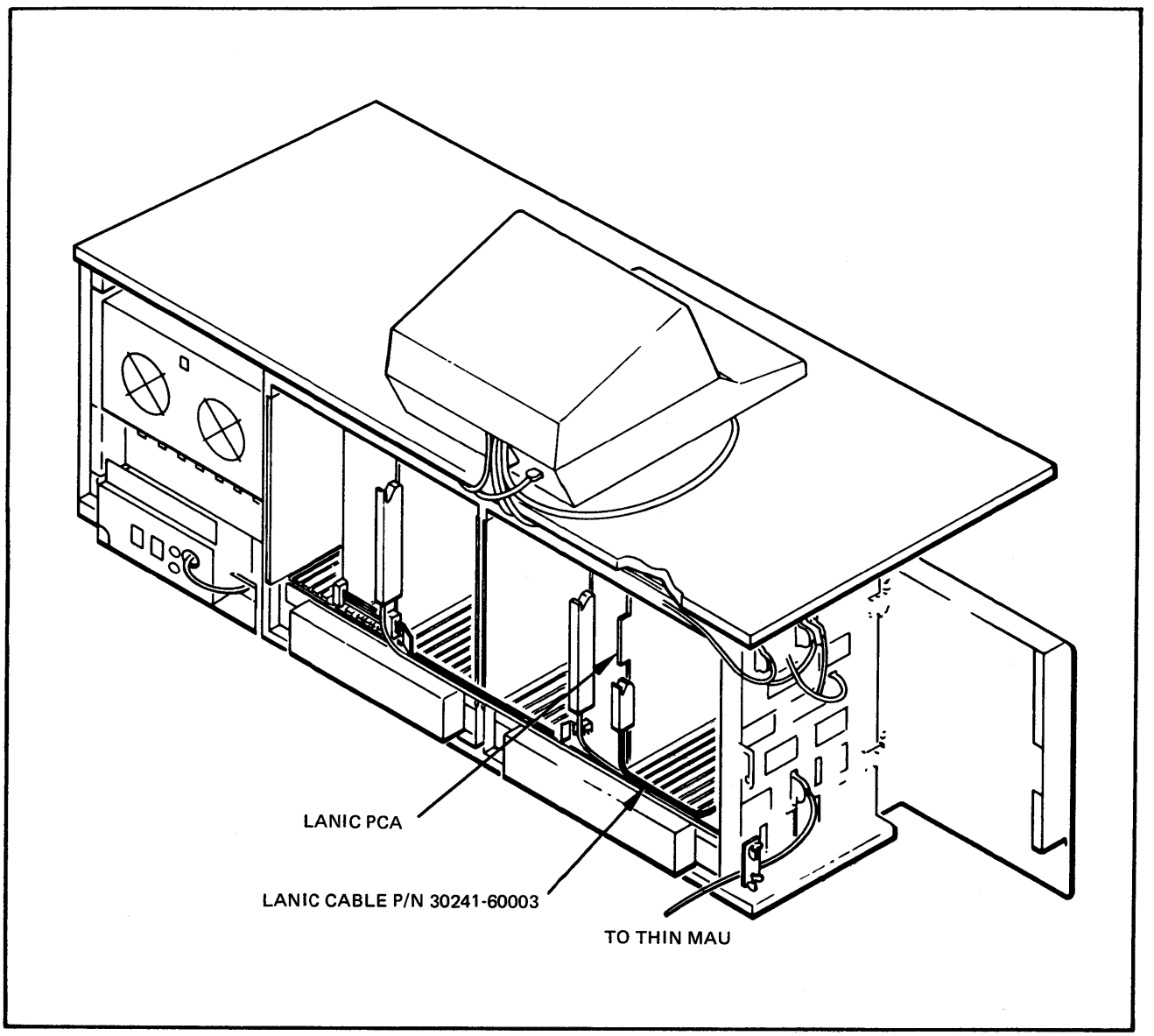


Figure 2-5. Series 44 and 48 LANIC Cabling Detail

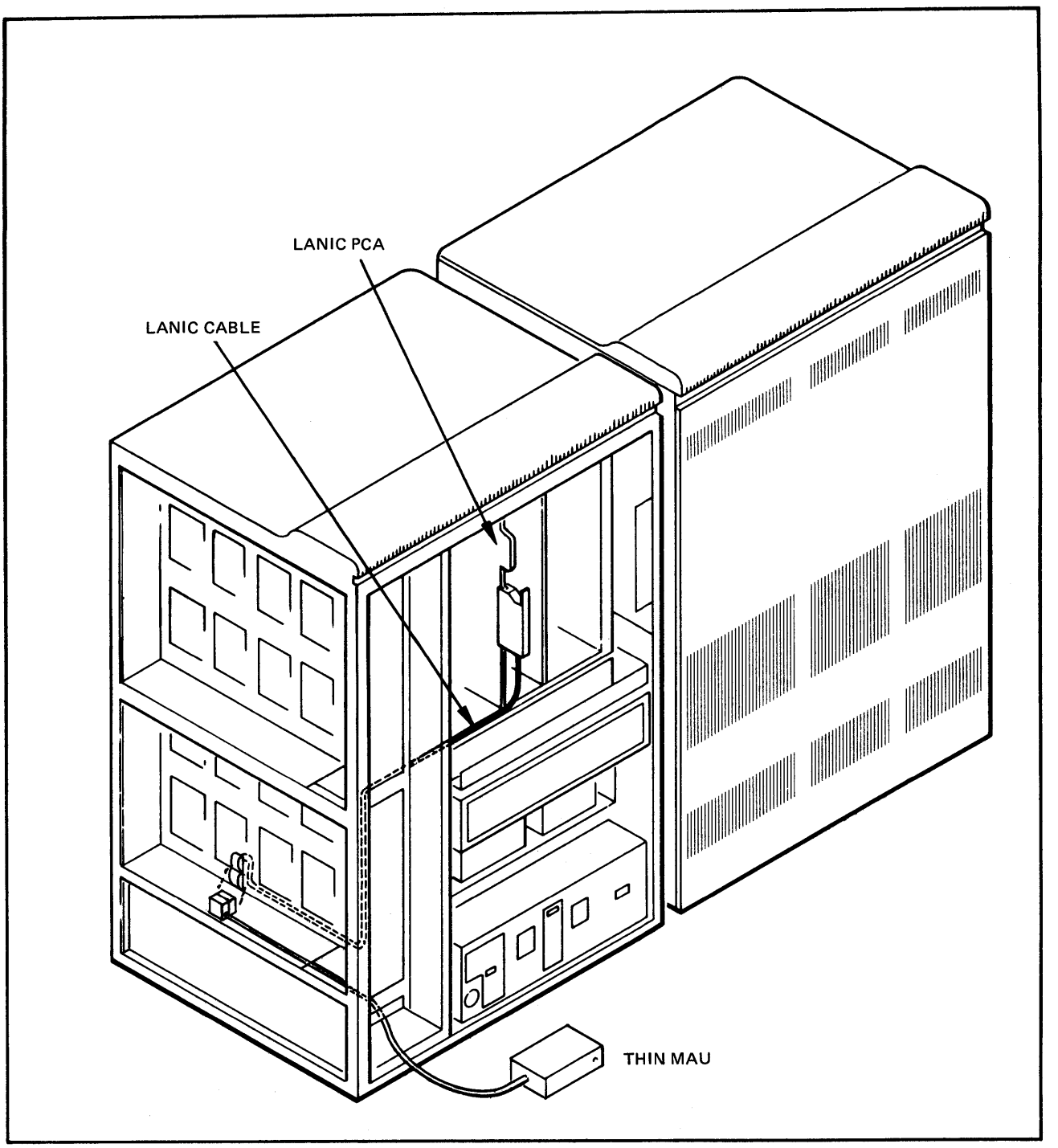


Figure 2-6. Series 64 and 68 LANIC Cabling Detail

PRINCIPLES OF OPERATION

SECTION 3

INRODUCTION

This section has a description of the HP 30240A OfficeShare LAN/3000 Link, Local Area Network Interface Controller (LANIC). The description gives the principles of operation.

FUNCTIONAL DESCRIPTION

The HP 30240A OfficeShare LAN/3000 link is an implementation of the IEEE 802.2 and IEEE 802.3 Local Area Network (LAN) standards and is used to allow HP 3000 computer systems to communicate with other HP 3000's over a Local Area Network (LAN). The IEEE 802.2 Local Area Network standard defines a logical link control protocol, and IEEE 802.3 Local Area Network standard defines a bus utilizing CSMA/CD (Carrier Sense Multiple Access/Collision Detect) as the access method.

The LAN/3000 link functions as an intelligent Direct Memory Access (DMA) channel which communicates with the host system via the system backplane. Local intelligent control is provided by a microprocessor and firmware on the LAN Interface Controller (LANIC).

The LAN/3000 link consists of a LAN Interface Controller (LANIC), and a Thin Medium Attachment Unit (ThinMAU). The ThinMAU attaches to a coaxial cable which connects the various computer systems together on the Local Area Network; and the LANIC provides the interface between the LAN and the computer system.

LAN INTERFACE CONTROLLER (LANIC)

The LANIC is an intelligent DMA channel which communicates with the host system via the system backplane. On the network end of the LANIC, the AUI carries bit-serial data and control information to and from the MAU, which attaches directly to the network coaxial cable. A functional block diagram of the LANIC is shown in figure 3-1.

Host to LANIC Communication.

The host communicates with LANIC through channel registers and data structures stored in system memory. Basic channel communication registers provide for channel identification, interrupt control, and diagnostics. Of primary importance are the Control Register (CR) and Status Register (SR), which provide for the input and output of control and status information. Link-level commands and status are passed via two queue structures stored in system memory shared by the LANIC and the host.

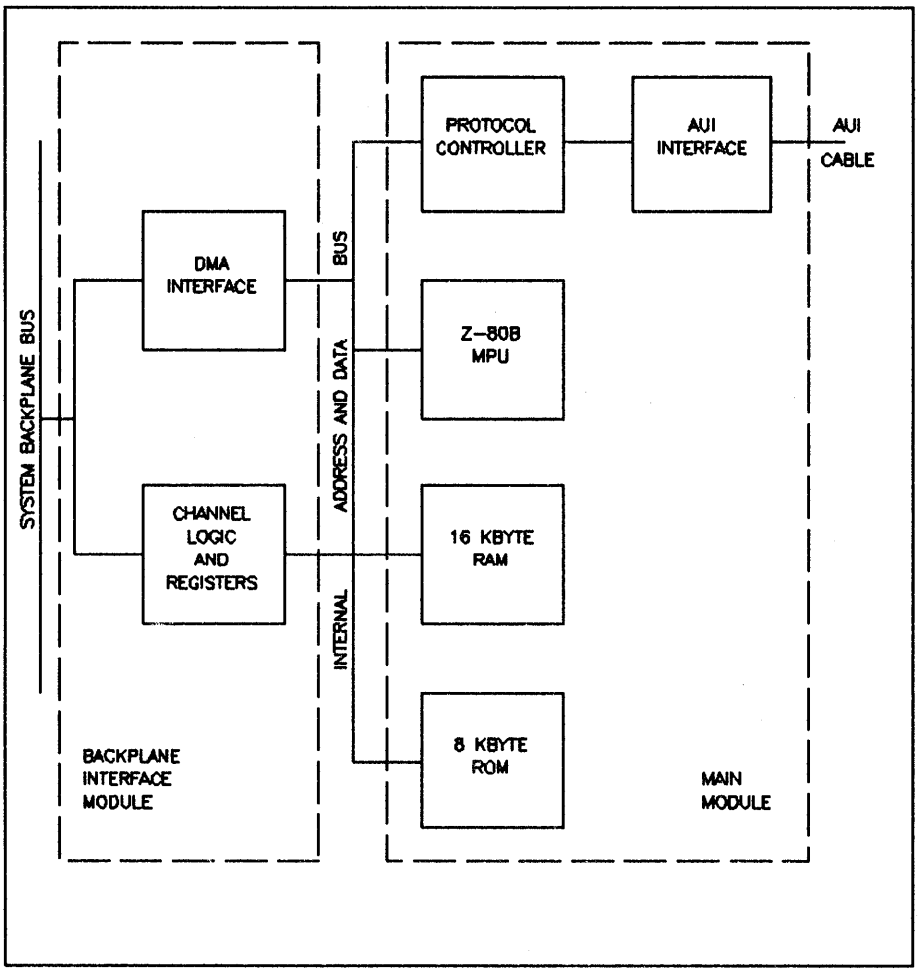


Figure 3-1. LANIC Functional Block Diagram

LANIC MPU and Firmware.

Local intelligent control is provided by a microprocessor (MPU) and firmware on the LANIC card. An 8-bit microprocessor, type Z-80B, handles all the LANIC-to- host communication and performs many link-level operations independently of the host. The MPU also is responsible for performing an on-board self-test to detect and locate hardware faults. The firmware for the MPU resides in both ROM and RAM. The ROM firmware has the self-test, MPU interrupt control, and bootstrap programs. The link-level operational firmware is downloaded into LANIC RAM from system memory.

Local Communications Controller.

The Local Communications Controller (LCC) is a high-performance LSI device that performs most of the data link and physical link functions for the local network architecture. The LCC performs high-speed serial operations, packet address checking, network contention control, packet formatting, and CRC (Cyclic Redundancy Check) generation/checking. The LCC is controlled by the MPU through local memory.

Direct Memory Access.

The LANIC can transfer data directly to and from system memory. Once the host has given the LANIC the location of data buffers in system memory, data is transferred without host intervention. This allows maximum system performance by uploading the task of packet transmission and reception from the host, allowing the host to spend more of its time on other processing.

Firmware Download and Configuration

Although the self-test, diagnostic, and bootstrap firmware are all resident in ROM, the operational firmware must be downloaded from the host into the LANIC local memory. After the firmware is downloaded, control is passed to it and the LANIC is ready to be configured. Configuration comprises the 82586 chip configuration, setting the station address, and initializing the command response queues.

FIRMWARE DOWNLOAD. The host initiates the downloading of firmware from system memory to the LANIC local RAM. The LANIC performs the actual transfer via its DMA facility. After the transfer, the LANIC computes the checksum of the data in local RAM and compares it with the checksum computed by the host. This ensures that the download firmware is transferred correctly. The entire firmware may be downloaded via a sequence of download operations. The host has full control of firmware operation and can suspend firmware execution at any time and dump LANIC memory and hardware status to system memory.

SETTING STATION ADDRESS. The LANIC supports both globally and locally administered addressing. Globally administered addressing is supported by a ROM on the LANIC that has a unique 48-bit address code. This address can be read by the host. Setting the station address is accomplished by a process involving the Duplicate Address Check (DAC) protocol. The host supplies the LANIC with a candidate station address. The LANIC sends an Exchange Identification (XID) packet with this address in the destination field. If any node is using the same station address, it sends the packet back to the LANIC. The LANIC waits for any response to come back before establishing its station address. If the DAC protocol fails, the host is notified to take further action.

QUEUE INITIALIZATION. Once operational, most of the communication between the host and the LANIC is via a pair of queue structures in system memory. One queue, the Command Queue (CQ), is used by the host to send commands to the LANIC. The other queue, the Response Queue (RQ), is used by the LANIC to return status to the host. Each queue is fixed in size with fixed-length entries, however these parameters are programmable when the queues are configured by the host. The head and tail pointers are stored in system memory along with each queue. The host informs the LANIC of new entries in the CQ by means of the READ_QUEUE command. The LANIC informs the host of new RQ entries by means of the system interrupt facility.

Transmit Operation

TYPES OF PACKETS TRANSMITTED. The LANIC can transmit any size packet up to the maximum packet size. Short packets are automatically padded to meet minimum packet length requirements.

TRANSMIT BUFFER MANAGEMENT. The host is responsible for setting aside transmit buffers in system memory. The starting address and length of each buffer is sent to the LANIC via the XMIT request. Each buffer is identified by a unique ID number. When the LANIC has successfully transmitted a transmit buffer, or when it encounters an irrecoverable error, it returns the ID number and status to the host via the Response Queue (RQ). The host must ensure that transmit buffers are frozen in system memory from the time the XMIT request is entered into the CQ until the LANIC returns the buffer ID in the RQ.

QUEUING OF TRANSMIT BUFFERS. The transmit operation requires a number of steps and there in no way to predict when a transmit buffer is actually sent. Transmit buffers queue up in the CQ and in an internal transmit queue. The buffer at the head of the transmit queue is processed when no receive packets are being processed. Even then, there may be a delay due to the CSMA/CD protocol.

TRANSMIT OPERATION EXAMPLE. A transmit frame is assembled by the host in system memory. The host then adds to the CQ an XMIT request containing the address and length of the transmit frame and the ID number. The LANIC will process this command after it completes operations in progress and gets the command from the CQ. The LANIC then copies the contents of the frame buffer from system memory to its local memory. The next phase is undertaken by the 82586 LCC chip. The 82586 handles the CSMA/CD protocol, serializes the data from the local memory buffer, sends it out on the network, and generates the frame check sequence. After the 82586 LCC is finished with the frame, LANIC firmware records the frame completion status and ID number in the RQ.

Receive Operation

TYPES OF PACKETS RECEIVED. The LANIC will only receive packets addressed to its station address (except when promiscuous mode is configured). These packets may be individually addressed, broadcast, or multicast, if the LANIC has been configured for such operation. Packets that are shorter than minimum or longer than maximum are not returned to the host, however, the statistical counters are updated.

RECEIVE BUFFER MANAGEMENT. The host is responsible for setting aside receive buffers in system memory. The starting address and length of each buffer are sent to the LANIC via the RECV command. These buffers are identified via a unique ID number. When the LANIC fills a receive buffer, it returns the ID number to the host via the Response Queue (RQ). From the time that the host enters the buffer descriptor into the CQ until the LANIC returns the ID number in the RQ, the host must ensure that the buffer is frozen in physical memory. Since neither the host nor the LANIC have control over what time a packet arrives, there must be a sufficient number of buffers ready for the LANIC to receive bursts of packets, otherwise packets will be lost. For further information on lost packets, see the paragraph "Receiver Blind Spots".

QUEUING OF RECEIVED PACKETS. Received packets may be queued by the LANIC before being reported to the host. In order to report received packets to the host, the LANIC microprocessor must access system memory. However, it may not be able to do this during a burst of receive packets because the LANIC DMA capability will be saturated with packet transfers to system memory. The microprocessor will update the RQ as soon as a lull in received packet traffic occurs.

RECEIVER BLIND SPOTS. Under certain conditions, the LANIC can fail to receive a packet. The following conditions are necessary for the LANIC to receive a packet at any time:

The receiver must be turned on.
There must be a buffer ready to receive the packet.
The LANIC must be able to write to memory fast enough to prevent losing data.

If any of the above conditions are not met, receive packets will be lost.

RECEIVE OPERATION EXAMPLE. The host allocates one or more receive buffers and enters RECV commands containing the buffer descriptors and IDs into the CQ. The LANIC removes these descriptors from the CQ and puts them on an internal queue, and turns the 82586 LCC receiver on. The LCC prepares for packet reception by taking the first buffer descriptor off the internal queue. The LCC looks at the destination address of all packets on the network. When the destination address matches the LANIC station address, the LCC deserializes the packet and starts writing it to system memory using the current receive buffer descriptor. At the end of the packet, the LCC compares the CRC and re-uses the buffer descriptor if there was an error in packet reception. Otherwise, the LCC records the packet reception, prepares the next buffer descriptor from the internal queue, and interrupts the microprocessor. When the microprocessor acknowledges the interrupt, the LCC adds the status and ID number of the completed packet(s) to the RQ.

Error Management

The LANIC detects command, system, and network errors, takes recovery action when appropriate, and reports status to the host. Command format errors are simply reported to the host, but do not result in any interruption of operations in progress. The LANIC attempts recovery of certain errors, such as MAU jabber, and if recovery is successful, the LANIC reports the recovery to the host for logging, and continues operation. When the LANIC detects a non-recoverable error, such as a system memory error, it aborts all operations in progress, reports the nature of the error to the host via the system interrupt mechanism, and waits for further action by the host.

Self-Test Operation

The LANIC executes a self-contained self-test program on system reset, or under host software control. Additionally, self-test can be initiated via a switch on the card, or by power-on. The LANIC self-test program tests a portion of the LANIC hardware. The self-test result code is displayed visually on the LANIC card (see Section 4), and can be programmatically read by the host via a channel register dedicated to self-test result codes.

System Interrupt

The LANIC can request a host software interrupt via two pseudo-device interrupts. When the host issues the OBII command to the LANIC, the data returned has either a zero or a one in bit 15, corresponding to the interrupting device number. Device number zero corresponds to the interrupt called SINTR0, and device number one corresponds to the interrupt called SINTR1. If both interrupt requests, SINTR0 and SINTR1, are active simultaneously the interrupt code for SINTR0 is returned.

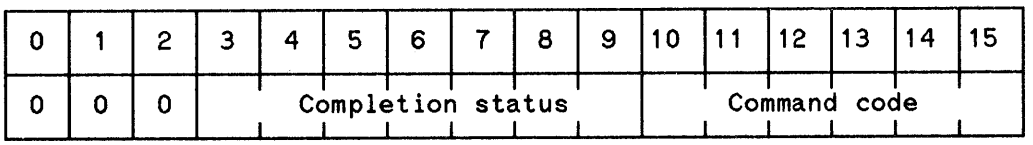
Operation of the LANIC IRQ (Interrupt Request) is as follows:

> If either or both of SINTR0 and SINTR1 are set and the interrupt mask, MASKF, is set, then the channel asserts the IRQ line on the backplane. Eventually, the host detects that IRQ is asserted and invokes the microcode routine to handle interrupts. This microcode performs an IPOLL to determine which channel(s) are requesting, and then an OBII to determine which device on the channel to service. After determining which channel and device to service, the microcode issues a WIOC command to clear SINTR, and dispatches the appropriate software interrupt routine.

SINTR0 SELF-TEST INTERRUPT. The SINTR0 interrupt request is activated by the ROM-based self-test firmware when the self-test sequence completes or whenever an idle self-test failure is detected. The host software reads the STR channel register to determine the type of error detected. A more detailed description of the self-test is contained in Section 4.

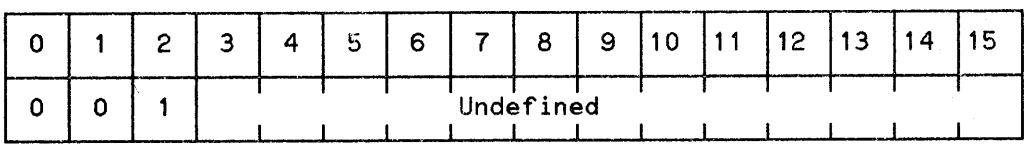
SINTR1 LANIC INTERRUPT. This interrupt is activated by either the ROM-based kernel firmware or by the downloaded operational firmware to signal the host software that some event in the LANIC has occurred. Host software reads the SR channel register to determine what type of event has occurred. The types of events fall into two groups: those related to a command issued to LANIC by the host software, and those resulting from internal LANIC operations.

INTERACTIVE COMMAND COMPLETION. This response is given when the LANIC completes the execution of an interactive command. The command-specific bits of the response code contain status and error codes whose meanings depend on the associated command as shown below.




```
Command code      = Command code originally given
Completion status = See below and paragraph "Self-test"
                    00 - command executed correctly
                    01 - sync between driver and LANIC established
                         (e.g., an all-ones word written into CR)
                    02 - illegal length command
                    03 - command not found
                    04 - command doesn't match length
                    08 - host buffer crosses bank boundary
                    09 - non-word address on download or dump
                    0A - checksum didn't check (DOWNLOAD command)
                    0B - illegal start address (START CODE command)
```

INTERACTIVE COMMAND ACKNOWLEDGEMENT. This response is given after the firmware reads the first word of a multiple-word command from the CR. This response is useful for avoiding the host software busy-wait on CRFULL after the first word of a multiple-word command has been written to the DR. This problem is due to the fact that the first word may not be accepted by the LANIC for several milliseconds, but the succeeding words are handshaken with negligible delay. A command acknowledgement response is not given for a single-word command as it is followed by a command completion response anyway. See below.



BATCH COMMAND COMPLETION. The response shown below is given when the firmware completes the execution of a batch command:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	0	Undefined												

FATAL ERROR RESPONSE. The fatal error response is given when and event occurs that requires the LANIC to be re-initialized. All operations in progress are aborted and pending operations are suspended. The LANIC is in the KERNEL state after giving this response.

LANIC Resets

There are three types of resets on the LANIC: power-on reset, hard reset, and soft reset. The power-on reset is the highest priority and the soft reset is the lowest priority. The resets are nested such that a higher priority reset includes all lower priority resets. Table 3-1 summarizes the LANIC reset operations.

Table 3-1. LANIC Resets and their Effects

AFFECTED FUNCTION	PON	HARDRST	INIT IOCL	SOFTRST
MAUPOWER	OFF	OFF	OFF	OFF
SELFTEST	YES	YES	NO	NO
VISIND	ON	ON	ON	---
MHSEN	OFF	OFF	OFF	OFF
SLVHS	RESET	---	---	---
MASTER H/S	RESET	RESET	RESET	RESET
CRFULL	0	0	0	---
MASKF	0	0	0	---
SINTR0	0	0	0	---
SINTR1	0	0	0	---
Z-80 RESET	PULSE	PULSE	LATCH	NO

POWER-ON RESET. The PON signal on the backplane causes a power-on reset. The entire hardware and firmware state of LANIC is initialized and all LANIC operations on the backplane cease. When the PON goes active, the LANIC enters the SELFTEST state.

HARD RESET. Hard reset aborts all operations in progress on the LANIC, resets all control registers, and forces the LANIC into the SELFTEST state. Self-test is then performed and the internal status of the firmware prior to the reset is unrecoverable. LANIC commands (except further hard resets) must not be issued until the self-test sequence has completed. At the end of the self-test sequence, the LANIC will go to the KERNEL state, waiting for commands from the host.

Hard reset is started by the backplane commands PON, SRST, IOCL, INIT, WREG14, WREG15, and by activating the self-test switch.

The HARDRST clears the channel interrupt mask flip-flop MASKF, clears both SINTR0 and SINTR1 interrupt requests, and illuminates the VISIND visual indicators (LED's). In addition, the master handshake enable flip-flop, MHSEN, is cleared.

SOFT RESET. Soft reset suspends all hardware operations in progress and puts the LANIC into the KERNEL state, waiting for further commands. In this way, most of the LANIC internal state information is preserved. The microprocessor is not reset and information pertaining to the RQ entries remains valid. The firmware is forced to the KERNEL state and communication with the host software is restricted to the CR and SR only.

The soft reset is typically issued when a LANIC failure has been detected by the host (e.g., LANIC is unresponsive). The firmware is thus forced to communicate with the host software. Since self- test has not been performed, diagnostics of the firmware can take place by issuing the MEMORY_DUMP command.

Soft reset can be initiated by the LANIC or by host software. The LANIC hardware initiates soft reset by detecting certain system bus errors. These errors are: system bus timeout, memory parity error, bus parity error, or memory bounds violation. System software can initiate a soft reset by writing register 14 (ABORT register) on the LANIC with bit 15=1.

Z-80 RESET. The IOCL and INIT commands effect a HARDRST, but the microprocessor remains reset. This feature is useful for diagnostics which need to reset the hardware registers without initiating the self-test sequence. The microprocessor remains reset until a normal HARDRST in issued.

POWER-FAIL WARN. When the backplane power-fail warn signal (PFW) is active, the LANIC is prevented from requesting or initiating a system bus master handshake. If the PFW signal becomes active while the LANIC is requesting, but has not yet been acknowledged bus master, then the LANIC backs off from requesting the bus while PFW is active.

Self-Test

The LANIC has a self-test feature that performs tests of internal circuitry and provides a status code indicating the result. Before the execution of each self-test step, the step number is written to the STR and the VISIND registers. When the self-test is complete, the LANIC interrupts the host and enters the KERNEL state where it is ready to accept interactive commands.

MANUALLY INITIATED SELF-TEST. Self-test is manually initiated by the self-test switch on the LANIC card. The location of this switch is shown in figure 2-1 in Section 2.

REMOTELY INITIATED SELF-TEST. Self-test is remotely initiated by the backplane command WREG15, or by the backplane signals PON or SRST (Power On or System Reset).

IDLE SELF-TEST. During operation of the LANIC, various tests of hardware are performed when no other tasks are being processed. If a hardware failure is detected, an error code is placed into the STR register and the host interrupt request is set.

VISUAL INDICATORS. Fifteen light-emitting diodes (LED's) are used on the LANIC card to indicate LANIC activity. The locations of the LED's are shown in figure 2-1 in Section 2. Eight of the LED's are used for self-test results and are described in Section 4; the remaining seven LED's are used for indicating activity on the LANIC card and the LAN network. These LED's are described in the paragraph "LED's", later in this section.

Attachment Unit Interface (AUI) Circuitry

The Attachment Unit Interface (AUI) is the interface between the LANIC board and the Medium Attachment Unit (MAU). The AUI, MAU, and the coaxial trunk cable comprise an *analog network.* The analog network provides the physical connection between Local Area Network (LAN) nodes.

A block diagram of the AUI interface circuitry is shown in figure 3-2. The AUI interface consists of four blocks:

- A type 8023 chip
- Level 1 circuitry
- MAU power control
- AUI activity trace LED's

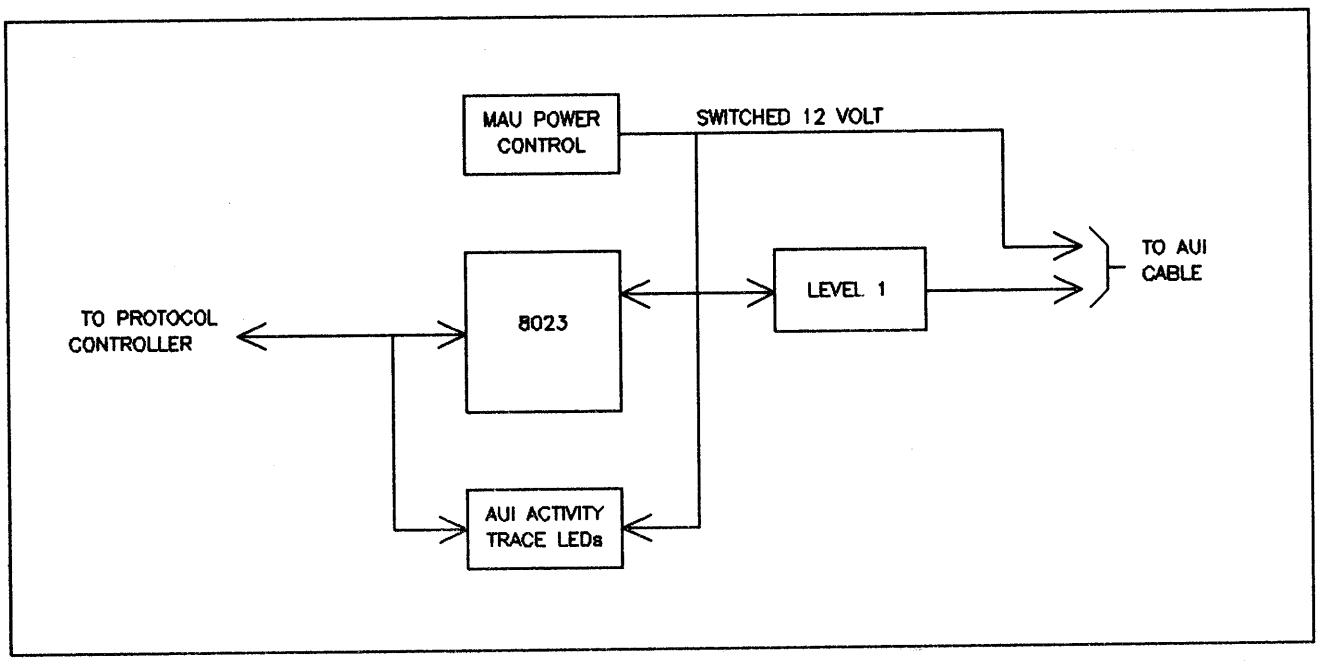


Figure 3-2. AUI Interface Block Diagram

The 8023 chip performs the following functions:

Decodes receive clock
Decodes receive data
Generates transmit clock
Encodes transmit data with clock
Decodes CONTROL IN
Detects carrier present
Loops transmit data to receive data for diagnostics

The AUI side of the 8023 chip consists of two balanced receivers (DATA5IN + CONTROL5IN) and one balanced driver (DATA5OUT). The signals from these circuits are put through a passive balancing network and are then transformer coupled to the AUI pairs.

MAU POWER CONTROL CIRCUIT. The MAU power control circuit provides three functions:

12-Volt Switch

The Z-80B MPU can turn the 12V to the AUI on or off.

12-Volt Current Protect

If the current to the AUI goes above 1.2A, the power control circuit switches the +12V off, thus protecting the LANIC and the system from shorts in the ThinMAU. The Z-80B will detect the fault and attempt to restart MAU power. If the attempt fails, the Z-80B notifies the host system of the fault.

12-Volt Sense

The Z-80B can determine if power to the AUI is on or off. However, it is not able to accurately measure the exact voltage being supplied. The IEEE 802.3 standard requires VP (+12V) to be greater than 11.28 volts. It is possible that the +12-volt power supply may be adjusted low enough such that less than 11.28 volts is present at the LANIC edge under load. If faulty ThinMAU operation is suspected, and ThinMAU replacement has not corrected the problem, the VP voltage should be checked. The VP voltage can be checked by connecting an accurate voltmeter between the +12V and GND test points on the LANIC. If the voltage under load is found to be less than 11.28V, the system +12V power supply must be checked and adjusted to the upper end of the allowable range. If the power supply is already set at the upper end of its range, the LANIC may need to be replaced. Consult the appropriate *CE Handbook* for details.

LED's.

The LANIC uses 15 LED's to monitor activities on the card and the LAN network. The locations of the LED's are shown in Section 2, figure 2-1; the labels and functions of the LED's are shown in figure 3-3.

The seven LED's labeled A through G monitor activity on the AUI interface. The eight LED's labeled H through N and * monitor LANIC MPU activity. A great deal of information about the state of the network and the LANIC and system software can be gained by studying the LED's. They are provided as an aid in problem detection and resolution.

Each of the 15 LED's is labeled with two different labels. The single alphabetic labels are helpful for quick reference to the LED's; the two-letter mnemonics are intended to remind users of the function being indicated by the LED.

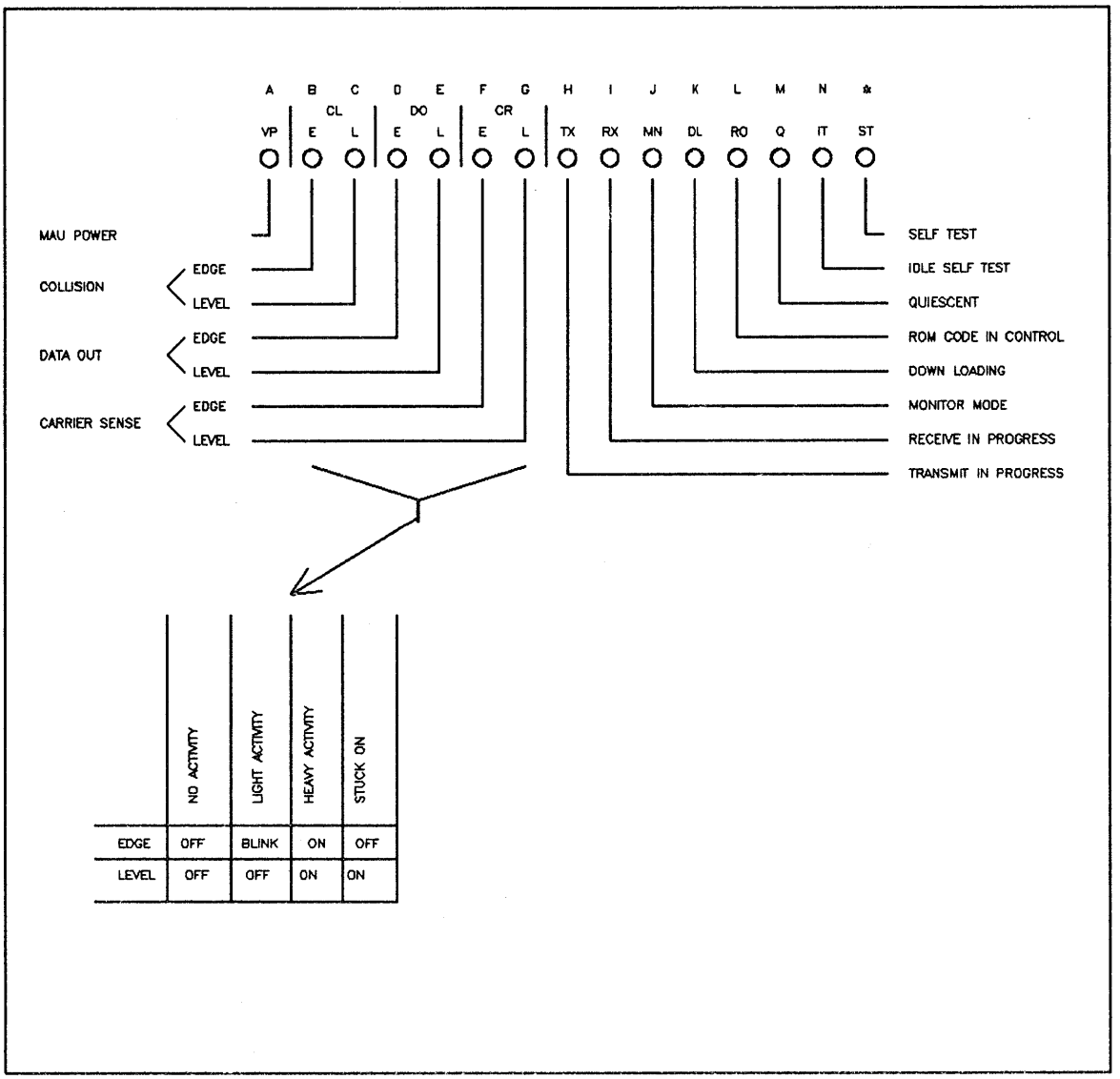


Figure 3-3. LANIC LED's

The meanings of the eight MPU (microprocessor unit) activity monitoring LED's are as follows:

Mnemonic	MPU Activity in Progress
TX	On when the LANIC is processing and transmitting a frame.
RX	On when the LANIC is processing a frame that was received at an address which the LANIC recognized as its own.
MN	On when the LANIC is monitoring all link activity, or is monitoring activity sent to a particular address not its own.
DL	On when the LANIC receives a command from the SPU (system processor unit) to start downloading operating firmware. Off when the SPU commands the MPU to begin to execute the downloaded feature.
RO	On when ROM-resident firmware is being executed by the MPU. Off when downloaded firmware is being executed by the MPU.
Q	On when the MPU is quiescent. During such times, it is checking for activity that requires attention.
IT	On when the MPU is executing an idle test of internal LANIC circuitry. During idle test, the MPU tests hardware on the LANIC that can be exercised without affecting readiness to process frames. The idle test also runs before the node becomes operational on the link.
ST	On when the MPU is executing the ROM-resident self-test, which verifies proper operation of the LAN hardware subsystem. When the ST LED is lit, the other seven MPU activity LED's are interpreted as self-test progress and failure indicators, rather than according to the mnemonics given above. For details of the use of self-test, see Section 4 of this manual and the *LAN/3000 Diagnostic and Troubleshooting Guide, part number 30242-90003*.

The seven AUI activity LED's are intended to be used as aids in determining activity on the network, and whether the source of this activity is this node or some other node on the network. These seven LED's monitor the four functions shown below.

Mnemonic	Function Monitored
DO	Data Out. On when data is transferred from this LANIC to the Data Out AUI pair.
CL	CoLlision Detect. On when a collision is detected by the MAU on this node. Since the HP 28641A ThinMAU detects collisions whether it is transmitting or not, the CL indicator comes on for every collision that occurs on this coaxial cable. The CL indicator does not come on when the MAU sends an SQE heartbeat after transmission.

CR — CaRrier Sense. On when data is detected coming into the node on the Data In AUI pair, or on when the collision function is detecting collisions. The CR indicator does not come on due to SQE heartbeat.

VP — Voltage Plus. This LED indicates the voltage present on this 12-volt supply lead to the MAU.

Each of the indicators for DO, CL, and CR consist of a pair of LED's, labeled *E* and *L*. The pair is driven in such a manner that all conditions of activity from occasional isolated events to continuous events can be distinguished by the unaided eye. This is accomplished in the following manner:

Each time that the event being monitored by an LED pair begins, the *E* LED is turned on and remains on for 6 msec regardless of the length of the event. The *L* LED turns on at the beginning of the event and turns off at the end of the event.

Following this algorithm, a single isolated event of short duration produces a 6 msec blink of the *E* LED, and the *L* LED is on for the length of the event, which is short. Therefore, the *L* LED appears to remain off.

As the frequency of events of short duration increases, the *E* LED appears to be constantly lit, and the *L* LED begins to glow.

When short duration events occur constantly, both the *E* and *L* LED's will appear to be constantly lit.

A single event of very long duration produces a single 6 msec blink of the *E* LED at the beginning of the event, and the *L* LED turns on and stays on for a long time, until the event is completed.

Continuously occurring events of very long duration will cause the *E* LED to blink at the beginning of each event for 6 msec, and the *L* LED will appear to be constantly lit.

Events on a normally-operating network are all of short duration. For instance, a maximum length frame requires only 1.2 msec to transmit; a minimum length frame requires only 51 µsec to transmit. Collisions have a maximum duration of only 49 µsec. For events of short duration such as these, the *E* and *L* LED's can be visualized as a sort of two-column bar graph. Frequency of activity is increasing as the frequency of flashing of the *E* LED increases while the *L* LED is off or very dim. When the *E* LED is always on, the *L* LED indicates further increase in activity by becoming brighter and brighter until it reaches full intensity. This state of the *E* and *L* LED's indicates continuous short events.

To understand the indications given by the DO, CL, and CR LED's, it is necessary to understand how the signals that drive these LED's are related to the signals on the AUI cable.

DO LED PAIR. The event indicated by the DO LED pair is the enabling of the data encoder by the protocol controller on the LANIC. The event begins when the encoder is turned on. While the encoder is on, a continuous stream of encoded data bits is transmitted by the LANIC to the DO AUI pair. The event ends when the data encoder is disabled. When the encoder is disabled, data bits are no longer sent to the DO pair. The transmission of a single frame to the AUI DO pair is one event, and will cause the *E* LED to blink on for 6 msec. The *L* LED will be lit for the length of time required to transmit the data bits to the AUI pair, a maximum of 1.2 msec for a maximum length frame.

CL LED PAIR. The event indicated by the CL LED pair is the occurrence of the Signal Quality Error (Collision) signal on the Control In pair of the AUI cable. When the HP 28641A ThinMAU, whether it is transmitting to the coaxial cable or not, detects a collision on the cable, it sends the SQE signal to the LANIC on the CI pair. SQE is signalled by a 10 MHz signal on the CI pair. The event begins when the first transition is received at the LANIC, and ends 200 nsec after the last transition is received.

The SQE heartbeat, which is a short burst of 10 MHz signal on the CI pair after each transmission by the LANIC on DO, does not cause the *E* LED to blink, although it does cause the *L* LED to light for approximately 1 µsec, which is too short to be seen. Likewise, no collision occurring on the network within 5.3 µsec of cessation of transmission by the LANIC will light the *E* LED. The SQE heartbeat is blocked from triggering the *E* LED so that the CL LED's will indicate the frequency of collisions occurring on the network.

CR LED PAIR. The event indicated by the CR LED pair is the reception of data on the Data In pair in the AUI cable, or the occurrence of the collision event described above. The event begins when the first data transition arrives on the AUI DI pair, or when the collision event begins, whichever occurs first. The event ends 200 nsec after the last data transition on the DI pair, or when the collision event ends, whichever occurs last.

H THROUGH N AND * LED's. When the LANIC has been reset either by power-up of the system or by the operating software, all eight of the MPU activity indicators (LED's H through N and *) will be on continuously. This indicates that the MPU is not executing. Additionally, the VP LED will be off, which indicates that the ThinMAU is not powered. The other AUI activity indicator LED's will all be off.

After the LANIC has successfully passed self-test, and the pass code pattern has been displayed as required, the * LED will be off, and the other seven MPU activity indicator LED's will now indicate the MPU activity. The * LED being off indicates that the H-N LED's are to be interpreted as individual activity indicators according to their two-letter mnemonics. (See the following paragraphs.)

TX, RX, MN, DL, RO, Q, AND IT LED's. When self-test passes, the SPU is interrupted and notified of the event. Between the time that this interrupt is given and the time when the SPU begins to access the LANIC, the RO and Q LED's will be lit. This indicates that the LANIC is executing ROM code and is quiescent, while waiting for the SPU to take control. In addition, the VP LED will be lit, indicating that the MAU is powered. Any activity on the network coaxial cable will be indicated by the state of the CL and CR LED pairs. The LANIC will never transmit in this state, and therefore, the DO LED pair will remain inactive.

When the SPU prepares the LANIC for operation, it first must download the operating firmware from system memory to the LANIC. When this process begins, the DL LED turns on, and the Q and IT LED's will go off. After each download command, the Q LED lights for a few milliseconds. At least seven download commands occur, but they may not be separately distinguishable. However, the pattern that occurs on one working system will occur on all other working systems, so if suspicious, compare the download pattern on the suspected system with a system that works.

After the download is complete, the SPU will instruct the MPU to begin to execute the downloaded firmware. When this occurs, the RO and DL LED's will go off. The Q and IT LED's will turn on.

A short time later the SPU will instruct the LANIC to set its individual address. When this occurs, the LANIC performs a duplicate address check, which is accomplished by transmitting 10 frames to the network with a 500 msec separation between frames. The TX and the DO *E* LED will both come on for each of the 10 frames. In addition, the CR *E* LED will indicate that the frames were sent to the coaxial cable and caused the carrier to come on. If collisions are encountered, the frames will be retried up to 15 times each, with resultant activity indicated by the CL LED's. The RX LED will not light during the duplicate address check due to our own transmission, even though the duplicate address check frame is addressed to the transmitting LANIC. If the RX LED lights during duplicate address checking, it is due either to a duplicate station being detected or to an ordinary frame being address to the LANIC. If a reply to the duplicate address check is received, this will cause the address check to fail, no further check frames will be sent, and the system software will close the link and clear the LANIC, forcing all the LANIC MPU LED's to come on and stay on.

If the duplicate address check passes, the link is opened, and frame transmission and reception will commence. The LED's will indicate activity as it occurs.

During normal network operation, frame transmission causes the LED's to operate in the following manner, assuming that the network and the LANIC were both idle before the transmit request arrived at the LANIC from the SPU:

While idle, the VP, Q, and IT LED's are on.

When the MPU begins processing the transmit command, the Q and IT LED's go off, and the TX LED comes on. The LANIC begins the transmit process by reading the frame from the system to the on-card memory.

Once the frame is in LANIC local memory, and the network is free, the serial transmission process begins. This causes the DO *E* LED to light. The DO *L* LED will also be turned on for the duration of the frame transmission, but this may or may not be visible, depending upon the length of the individual frame being sent.

The serial data reaches the ThinMAU and is transmitted to the coaxial cable. The ThinMAU begins to receive its own signal from the coax, and sends it back down the AUI cable. The LANIC detects data arriving on the DI pair of the AUI cable, and the CR *E* LED is lit. The CR *L* LED will also be lit for the duration of the frame, but this may or may not be visible. If the DO *L* LED is visible, the CR *L* LED will also be visible for approximately the same length of time.

If no collision is occurs, the CR and DO *E* LED's will go off after 6 msec, followed quickly by the transmit LED going off, and the Q and IT LED's coming on. If a collision is encountered, the CL *E* LED will come on, and the frame will be retransmitted up to 15 times. The retransmissions will cause the DO and CR *E* LED's to appear to be on, and the DO and CR *L* LED's will probably appear to be partially lit, with the intensity of the *L* LED's determined by frame length, number of retransmissions required, and the time separation of the retransmissions. The CL LED's will also display behavior similar to the CR and DO LED's if multiple retransmissions are required before the frame is successfully transmitted. In the collision case, it must be remembered that other network activity will also cause the CL and CR LED's to light, and the activity caused by the LANIC will be superimposed on the network activity being displayed by the CR and CL LED's. A little experience at observing the LED's will allow the occurrence of single or multiple collisions to be easily distinguished.

MAINTENANCE

SECTION 4

INTRODUCTION

This section contains general maintenance instructions for the LANIC card. Included is the repair philosophy for the LANIC card and information on the self-test. See the *LAN/3000 Diagnostic and Troubleshooting Guide, part number 30242-90003,* for detailed procedures to be used in troubleshooting networks containing the LAN/3000 link, and for diagnostic procedures to be used in isolating failures in LAN/3000 nodes to the field replaceable assembly.

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

REPAIR PHILOSOPHY

Field repair of the LANIC cards is limited to the replacement of the card itself. To exchange a LANIC card, remove it from the system and prepare it for reshipment to Hewlett-Packard in accordance with the instructions presented in Section 2.

SELF-TEST

A self-test is included in ROM on the LANIC card. The self-test runs at power-on, when the LANIC TEST (RESET) switch on the LANIC card is pressed, or when invoked by the LAN diagnostic.

NOTE

The self-test consists of several tests which check approximately half the circuitry on the LANIC card as well as performing a simple test of the ThinMAU. The LAN/3000 link diagnostic *must* be run to perform a complete test of the LANIC card. See the *LAN/3000 Diagnostic and Troubleshooting Guide, part number 30242-90003* for a description of the diagnostic.

CAUTION

PRESSING THE LANIC TEST SWITCH PERFORMS A HARD RESET ON THE LANIC CARD BEFORE THE SELF-TEST IS INITIATED. NETWORKING OPERATIONS IN PROGRESS WILL BE DISRUPTED BY PRESSING THE RESET SWITCH. ONCE SELF-TEST HAS STARTED, ALLOW IT TO COMPLETE PRIOR TO PRESSING THE SWITCH AGAIN. PRESSING THE SELF-TEST SWITCH WHEN THE LINK IS OPEN OR WHILE SELF-TEST IS ACTIVE HAS A SLIGHT POSSIBILITY OF CRASHING THE SYSTEM.

To run the LANIC self-test, perform the following:

1. Determine that the LANIC is not in use. This can be done by typing

   ```
   :SHOWDEV nn
   ```

   at any terminal on the system, where *nn* is the logical device number of the LANIC. If you see

   ```
   LDEV     AVAIL     OWNERSHIP     VOL. . .etc.
    36      AVAIL
   ```

   or something similar, the LANIC is not in use. If you see

   ```
   LDEV     AVAIL     OWNERSHIP     VOL . . .etc.
    36      UNAVAIL     SYS #1
   ```

   the LANIC is probably in use, and you should do a

   ```
   NETCONTROL NET=xxx;STOP
   ```

   before proceeding.

2. Open the computer card cage door and observe the self-test LEDs (see figure 4-1 for the locations of the LEDs). Note whether the LEDs indicate normal activity or whether the ST/* LED is blinking slowly and LEDs H through N are displaying a steady pattern. If a steady pattern is being displayed by LEDs H through N, make a written record of which LEDs are lit. (This information may be needed later if the problem is intermittent.)

3. Press the LANIC TEST RESET switch (see figure 4-1) to initiate the self-test.

4. Observe the self-test LEDs. Refer to table 4-1 for the meanings of the various LED patterns. If the self-test completes with no errors, the self-test LED (ST/*) will be on and LEDs H through N will be off (a code of all zeros) for a period of five seconds. After five seconds, the ST/* LED will go off and LEDs H through N will reflect activity on the LANIC. If the self-test fails, the code of the test that failed will be displayed by LEDs H through N and the ST/* LED will blink slowly for at least 20 seconds (allowing time for the code to be noted).

5. If the LANIC fails self-test, except as noted below, replace the LANIC card in accordance with the procedures given in Section 2. Re-run the self-test after the new card is installed. If the new card passes self-test and there still appears to be a problem on the network, run the LAN diagnostic (it is possible for the LANIC to pass self-test and still not be functioning properly). The diagnostic tests more of the LANIC card circuitry and also tests the ThinMAU. Refer to the *LAN/3000 Diagnostic and Troubleshooting Guide, part number 30242-90003*, for information on running the LAN diagnostic.

NOTE

The last test of the test sequence (2E, Loopback on Medium) requires that the ThinMAU be connected to the LANIC. If it is not connected to the LANIC, the last test will report a failure. The LANIC, however, may not be defective in this case.

6. If an intermittent problem is suspected, the self-test may be looped by holding the LANIC TEST RESET switch in with an alligator clip. The self-test will then loop until a failure is detected, and will preserve the failure code as described in step 4 as long as the switch remains in.

7. If the self-test completes with no error indications, the LAN/3000 diagnostic must also be run to completely check the LANIC and ThinMAU. Run the diagnostic as described in the *LAN/3000 Diagnostic and Troubleshooting Guide, part number 30242-90003.*

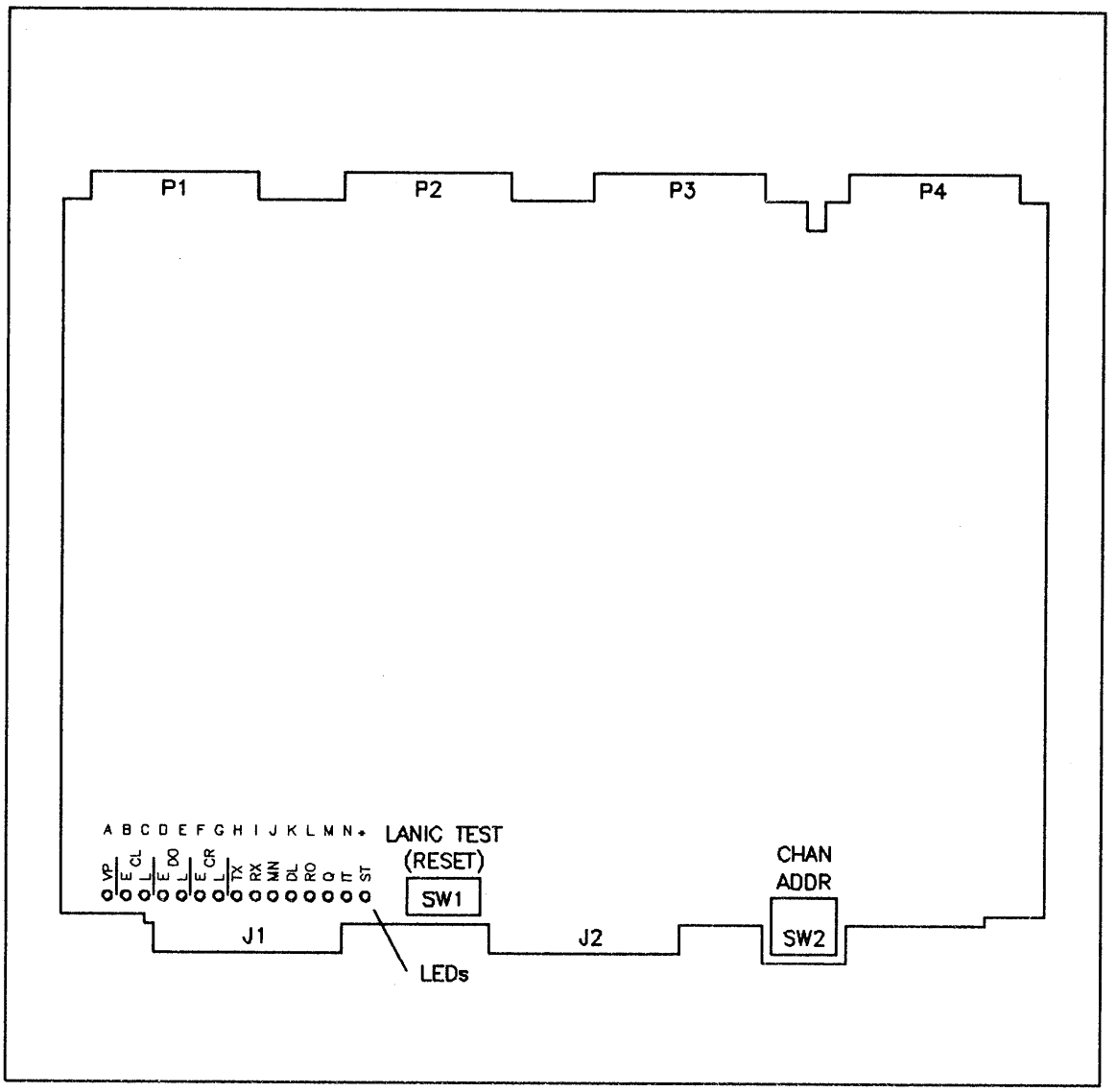


Figure 4-1. LANIC Switch and LED Locations

Table 4-1. Self-Test LEDs and Subtest Descriptions

CODE										
HEX NO.	LED INDICATION								SUBTEST	DESCRIPTION
	H	I	J	K	L	M	N	*		
1	0	0	0	0	0	0	1	1	Z-80	Instruction set
2	0	0	0	0	0	1	0	1	EPROM	Checksum
3	0	0	0	0	0	1	1	1	Station Address PROM	Checksum
4	0	0	0	0	1	0	0	1	High Byte Latch	
5	0	0	0	0	1	0	1	1	Byte RAM Data	Even addresses
6	0	0	0	0	1	1	0	1	Byte RAM Data	Odd addresses
7	0	0	0	0	1	1	1	1	Byte RAM Address	Incrementing addresses
8	0	0	0	1	0	0	0	1	Byte RAM Address	Decrementing addresses
9	0	0	0	1	0	0	1	1	Word RAM	Address tests
A	0	0	0	1	0	1	0	1	Word/Byte Address	Address mapping
B	0	0	0	1	0	1	1	1	Z-80	Memory reference instructions
C	0	0	0	1	1	0	0	1	MDIAG register SYSCON register	Proper state after reset
D	0	0	0	1	1	0	1	1	CTC	Data test
E	0	0	0	1	1	1	0	1	CTC	Mode 0 counting
F	0	0	0	1	1	1	1	1	CTC	Mode 2 counting
10	0	0	1	0	0	0	0	1	CTC	Mode 4 counting
11	0	0	1	0	0	0	1	1	Interrupt PAL	Bit 4 set and cleared
12	0	0	1	0	0	1	0	1	Z-80 interrupt	
13	0	0	1	0	0	1	1	1	Z-80 NMI	Non-Maskable Interrupt
14	0	0	1	0	1	0	0	1	MHSDIS	DMA Handshake Disabled

Table 4-1. Self-Test LEDs and Subtest Descriptions (Continued)

CODE										
HEX NO.	LED INDICATION								SUBTEST	DESCRIPTION
	H	I	J	K	L	M	N	*		
15	0	0	1	0	1	0	1	1	PADDR to BADDR bus	Low 15 bits
16	0	0	1	0	1	1	0	1	ZBANKL register	Low Z-80 bank bit
17	0	0	1	0	1	1	1	1	ZBANKH register	Eight high Z-80 bank bits
18	0	0	1	1	0	0	0	1	Preliminary FIFO	INREADY, ADVREADY, OUTREADY
19	0	0	1	1	0	0	1	1	FIFO Data	BDATA(7)
1A	0	0	1	1	0	1	0	1	FIFO Data	BEA(7,8)
1B	0	0	1	1	0	1	1	1	FIFO Data	BDATA(2:6)
1C	0	0	1	1	1	0	0	1	FIFO Data	BDATA(0,1,13:15)
1D	0	0	1	1	1	0	1	1	FIFO Data	BDATA(8:12)
1E	0	0	1	1	1	1	0	1	FIFO Data	BA(11:15)
1F	0	0	1	1	1	1	1	1	FIFO Data	BA(6:10)
20	0	1	0	0	0	0	0	1	FIFO Data	BA(1:5)
21	0	1	0	0	0	0	1	1	R14	Configuration register
22	0	1	0	0	0	1	0	1	OBII register	Value; Channel number not 0
23	0	1	0	0	0	1	1	1	COMCON register	Values from reset
24	0	1	0	0	1	0	0	1	MAU Power	On/Off (AUI/MAU not required)
25	0	1	0	0	1	0	1	1	R13	CR, CR Full Bit
26	0	1	0	0	1	1	0	1	R15	Selftest Result register

Table 4-1. Self-Test LEDs and Subtest Descriptions (Continued)

CODE										
HEX NO.	LED INDICATION								SUBTEST	DESCRIPTION
	H	I	J	K	L	M	N	*		
27	0	1	0	0	1	1	1	1	82586	Interrupt
28	0	1	0	1	0	0	0	1	82586	Reset
29	0	1	0	1	0	0	1	1	PBUS register addressing	
2A	0	1	0	1	0	1	0	1	82586	RAM addressing
2B	0	1	0	1	0	1	1	1	82586	Diagnose
2C	0	1	0	1	1	0	0	1	8023	Loopback
2D	0	1	0	1	1	0	1	1	82586	Write to FIFOs
2E	0	1	0	1	1	1	0	1	MAU	Loopback on medium

* ST (Self-Test) LED

The final test in table 4-1, the MAU loopback test, sends the following frame on the coaxial cable:

```
DESTINATION ADDRESS = SOURCE ADDRESS = the unique station address
                      of this LANIC, from the station address PROM,
                      and which may also be found on the LANIC'S
                      identifying label

TYPE FIELD:  2 bytes containing the data field length, 1134 bytes

DATA FIELD:  3 SAP bytes - 0, 1, 3EH - identifying this frame as a
             test response frame with null DSAP and SSAP

             31 ASCII bytes = "HP3000_NODE_XXXXXXXXXXXX_TEST._",
             where XXXXXXXXXXXX is the station address in ASCII

             1100 bytes with a binary incrementing pattern
```

Table 4-2. Reporting of Unexpected Results from Self-Test

CODE								
HEX NO.	LED INDICATION INDICATION							DESCRIPTION OF FAILURE
	H	I	J	K	L	M	N	*
7A	1	1	1	1	0	1	0	1	The 82586 failed to clear its command word.
7B	1	1	1	1	0	1	1	1	Self-Test Result register (R15) bit 0 bad.
7C	1	1	1	1	1	0	0	1	Z-80 stack underflow during self-test.
7D	1	1	1	1	1	0	1	1	Unexpected Z-80 Non-Maskable Interrupt (NMI).
7E	1	1	1	1	1	1	0	1	Unexpected Z-80 interrupt.
7F	1	1	1	1	1	1	1	1	The LANIC was reset, but self-test never started, or LED circuitry failed. Certain system resets will freeze the LANIC processor and leave the LEDs in this state. This condition, then, only indicates a LANIC failure at power-on, when the self-test switch is pressed, or when the LANIC diagnostic starts self-test.

* ST (Self-Test) LED

Note that the above codes are displayed *without* the "*" LED flashing.

CONFIGURATION INFORMATION

APPENDIX
A

INTRODUCTION

This appendix describes how to configure MPE to include the OfficeShare LAN/3000 link.

The MPE configuration must be modified when a LANIC card is added to the computer system. Before configuring MPE, install the LANIC card as described in Section 2.

CONFIGURATION DIALOG

The following configuration dialog deals only with configuring a LANIC card into the system. The complete configuration dialog is contained in the *HP 3000 System Operation and Resource Management Reference Manual, part number 32033-90005.*

To begin the configuration dialog, log onto the system as MANAGER.SYS, define the output files as shown below, and initiate a SYSDUMP as outlined in the following steps.

NOTE

Where necessary to distinguish user input from computer output, the user input is underlined. The "Step No." in the dialog below corresponds to the "Step Number" in the dialog contained in the *HP 3000 System Operation and Resource Management Reference Manual, part number 32033-90005.*

It is essential that the LANIC driver, IOLAN0.PUB.SYS be present when the UPDATE or COLDSTART or RELOAD is done. You may verify that the driver is present by typing:

```
:LISTF IOLAN0.PUB.SYS
```

Define the output files and initiate SYSDUMP as follows:

```
:HELLO MANAGER.SYS

:FILE T;DEV=TAPE
:FILE L;DEV=LP
:SYSDUMP *T,*L
```

Step No.	Prompt and Response
1	ANY CHANGES? YES
2	SYSTEM ID=HP 32033v.uu.ff? RETURN
3	MEMORY SIZE? RETURN
4	I/O CONFIGURATION CHANGES? YES
5	LIST I/O DEVICES? NO
6	LIST CS DEVICES? NO
7	HIGHEST DRT = xx.?

xx is the current highest hardware device address that can be assigned. Press RETURN if xx is satisfactory. Otherwise, enter a higher DRT number.

8	LOGICAL DEVICE #?

To specify a device to be added or removed, enter the logical device number (ldev) of that device.

Entering 0 or RETURN ends the I/O Configuration Changes procedure.

The dialog now prints the DEVICE NAME? prompt. Press RETURN.

9	DRT #?

To add a device, enter its DRT entry number. This number is supplied by your C.E. The formula used to calculate the DRT number from the hardware address is:

(IMB# x 128) + (channel# x 8) + device #

To remove a device, enter 0; the dialog returns to the LOGICAL DEVICE #? prompt.

10	UNIT #? 0
11	SOFTWARE CHANNEL #? 0
12	TYPE? 17
13	SUBTYPE? 9
38	DRIVER NAME? IOLAN0

Step No.	Prompt and Response
43	DEVICE CLASSES? Enter a device class name (up to eight alphanumeric characters, beginning with a letter). Multiple class names, separated by commas, may be entered at one time.

The dialog now prints the LOGICAL DEVICE #? prompt described in step 8. If all I/O configuration is complete, press RETURN and the I/O configuration portion of the SYSDUMP dialog will end.

If I/O configuration is not yet complete, enter a logical device number and repeat the above configuration procedure.

46	MAX # OF OPENED SPOOLFILES = xxx ? RETURN
47	LIST I/O DEVICES? NO
48	LIST C/S DEVICES? YES
49	TERMINAL TYPE CHANGES? NO
57	CLASS CHANGES? NO
69	LIST I/O DEVICES? NO
70	ADDITIONAL DRIVER CHANGES? NO

The dialog now prints the I/O CONFIGURATION CHANGES? prompt described in step 4. If all I/O configuration is complete, press RETURN and the dialog continues at step 77. Otherwise, enter YES, and repeat the configuration procedure from step 4.

77	SYSTEM TABLE CHANGES? NO
97	MISC CONFIGURATION CHANGES? NO
112	LOGGING CHANGES? NO
119	DISC ALLOCATION CHANGES? NO
133	SCHEDULING CHANGES? RETURN
134	SEGMENT LIMIT CHANGES? NO
142	SYSTEM PROGRAM CHANGES? NO
144	SYSTEM SL CHANGES? NO

Step No.	Prompt and Response

153 ENTER DUMP DATE? Enter one of the following:

(RETURN)
Copies the modified MPE.

mm/dd/yy
mm/dd/yy is some date in the future. Copies the modified MPE and the current accounting structure (but no files).

mm/dd/yy
where mm/dd/yy is usually the date of the most recent system backup. Copies the modified MPE, the current accounting structure, and any files that were changed on or since the specified date.

0
Copies the entire system (MPE, the current accounting structure, and all files).

154 ENTER DUMP FILE SUBSETS? (RETURN)

155 LIST FILES DUMPED? (RETURN)

156 You are now requested to assign the serial storage device (a tape if you initiated SYSDUMP as shown at the beginning of this dialog) on which you have arranged for the system to be copied.

Once the system has been copied, the following message is printed:

END OF SUBSYSTEM

INDEX

SPECIAL CHARACTERS

A

B

C

D

E

F

G

H

I

L

M

N

P

Q

R

S

T

Z