MANUAL

for

DIGITAL VOLTAGE
SOURCE PROGRAMMER
INTERFACE KIT HP 12661A

FOR
MODEL 2100 SERIES COMPUTERS
(HP PART NO. 12661-90004)

Microfiche No. 12661-90007

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SECTION I

GENERAL DESCRIPTION

1-1. INTRODUCTION.

1-2. The HP 12661A Digital Voltage Source (DVS) Interface Kit provides an interface between Hewlett-Packard Computers and Hewlett-Packard Digital Voltage Sources or other suitable instruments that can utilize the Card's output bit structure.

1-3. The DVS Program Card uses one I/O slot and address and can address up to eight peripheral devices (with octal addresses 0 through 7) in random sequence. The Card will monitor the eight peripheral devices noting the status of each one and provide the computer with an alarm interrupt, if one should fail.

1-4. The standard HP 12661A DVS Interface Kit is wired to interface with saturating (high-level) circuits. The HP 12661A, Option 01 DVS Interface Kit is wired with optional jumpers to interface with non-saturating (low-level) IC logic levels. Input and output specifications for both versions are listed in Table 1-1.

1-5. The HP 12661A DVS Interface Kit consists of the following components:

a. DVS Program Card (HP Part No. 12661-6001 for standard kit) or (HP Part No. 12661-6002 for Option 01).

b. 48-Pin Connector Assembly (HP Part No. 02116-6178).

c. Diagnostic Program Tape (HP Part No. 20436A).

1-6. DESCRIPTION.

1-7. INTERRUPT CAPABILITY.

1-8. The DVS Program Card will recognize two modes of interrupt from the peripheral devices it is programming. One interrupt mode is called Timing (Flag) and sets the Flag Buffer FF. The DVS Program Card is assigned, by software, to recognize interrupts from the Flag line. Up to eight peripherals can be parallel connected to the Flag input. This means the DVS Program Card could cause an interrupt whenever any one of the peripherals has completed the instructions given to it by the computer.

1-9. The second interrupt mode is called Alarms and sets the Alarm Buffer FF. The DVS Program Card is assigned, by software, to recognize interrupts from the Peripheral Status lines. The Status lines are jumpered to an OR gate that can cause an interrupt if one of the Status lines goes down. Program examination of the eight Peripheral Status inputs (see Figure 1-2) will determine the faulty unit only if the unit remains faulty. If the peripheral that caused the alarm returns to normal, the Status Bits return to normal.

1-10. SOFTWARE WORD STRUCTURE.

1-11. The DVS Program Card permits transfer of data between the HP Computer and peripheral devices. Two words are set by the computer for data or control output. The first word contains 16-bits and the second word, 8-bits. One 11-bit word is used to transfer data from the DVS Program Card to the Computer.

1-12. OUTPUT WORDS. Figure 1-1 shows the bit structure of the two output words. The first 3-bits of the second word (0 through 2) are converted by the DVS Program Card to enable a device command line. These bits are decoded by a 4 Line (BCD) to 10 Line (decimal) converter which activates one of eight Command lines. Bit 7 of the second word is called a System Clear Bit and is activated when the computer is initially turned on. It is also possible to activate the System Clear bit if one of the peripheral devices fails. See Section III, System Clear for details.

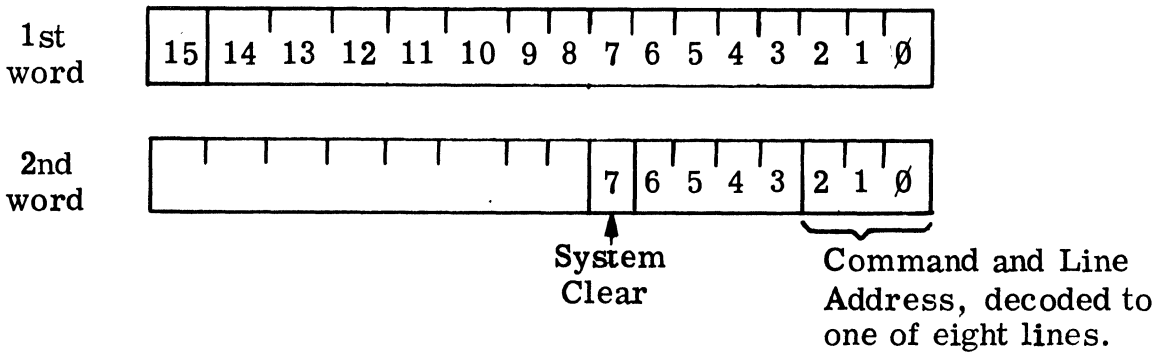


Figure 1-1. Output Word Structure

1-13. INPUT WORD. Figure 1-2 shows the bit structure of the input word.

a. Bits 0 through 7 are input status bits (1-bit per device) which show peripheral device status but do not have storage capabilities.

b. Bits 8 through 12 are not used.

c. Bit 13 is the mode of interrupt requested (see Paragraph 1-8). A "0" indicates the Alarm mode. A "1" indicates the Timing (Flag) mode.

d. Bit 14 is the System Clear Command Status. A "0" indicates the Clear Command is OFF. A "1" indicates the Clear Command is ON.

e. Bit 15 is the interrupt mode that has taken place. A "0" indicates the Alarm mode. A "1" indicates the Timing (Flag) mode.

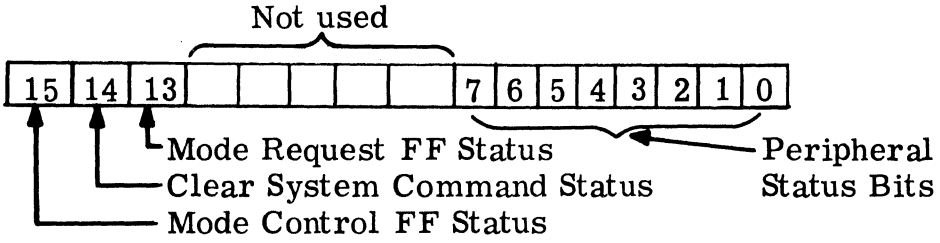


Figure 1-2. Input Word Structure

1-14. The DVS Program Card contains both a Mode Request FF (bit 13) and a Mode Control FF (bit 15). The status of bits 13 and 15 correspond to the state of these FF's. The Mode Request FF can differ from the Mode Control FF when an interrupt is generated. For example; the Alarm mode has been previously set and you decide to change to Timing (Flag) mode. During this mode change a peripheral fails before the change is completed. The Mode Request FF would be set and the Mode Control FF would be reset. The mode of interrupt would not change to Timing (Flag) until the Alarm was cleared or recognized. If the peripheral fails during the transition from Timing (Flag) mode to Alarm mode, the failure will set the Alarm Buffer FF which will cause an interrupt as soon as the mode is changed to Alarm.

Table 1-1. DVS Program Card Specifications.

PERIPHERAL DEVICE INTERFACE LEVELS AND CODING	Level	Coded Data	Logic	Flag
	+V	0	False	Not Busy
	0V	1	True	Busy
OUTPUT CIRCUITS HP 12661A	NPN, emitter grounded, collector thru 22K ohms to +12V. Maximum current to ground = 18 mA.			
HP 12661A, Option 01	NPN, emitter grounded, collector thru 22K ohms to +4.5V. Maximum current to ground = 18 mA.			
INPUT CIRCUITS HP 12661A	Open or +5.5V to +12V = +V (False) Short or -1V to +2.8V = 0V (True)			
HP 12661A, Option 01	Open or +2.5V to +5V = +V (False) Short or -1V to +1V = 0V (True)			
CURRENT REQUIREMENTS	1.42 A (+4.5V) 137 mA (+12V) 60 mA (-2V) 14 mA (-12V)			
DIMENSIONS				
Width	7-3/4 inches (196.8 mm)			
Length	8-11/16 inches (220.7 mm)			
WEIGHT				
Net (Card)	10.5 oz. 298 gm.			
Shipping (Kit)	4 lbs. 1.8 kg.			

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INSTALLATION.

2-2. GENERAL.

2-3. Since the DVS Program Card is designed for use with several different peripheral devices, an interconnecting cable must be prepared for your particular application. Use the 48-pin Connector Kit furnished and wire your cable using Table 2-1 as a guide. If more than one peripheral is to be interfaced with this card, special attention must be given to the distribution of the individual lines as well as the common lines. Figure 2-1 shows one method that can be used to interconnect up to eight power supplies with the DVS Program Card.

2-4. Install the card in the computer as follows:

a. Turn off computer power.

b. Open the computer for access to the I/O cards.

c. Plug the DVS Program Card into the I/O slot assigned for the particular computer system.

d. Pass the interconnecting cable through the slot in the computer and up to the card. Slide the 48-pin connector onto the card and close the computer.

2-5. OPTIONAL JUMPERS.

2-6. The DVS Program Card contains optional jumpers that allow field selection of control logic, output logic levels, output bit capacity, and alarm functions.

2-7. As shipped from the factory for use with both the 12661A and 12661A, Option 01 DVS Interface Kit; the DVS Program Card jumpers are in place or removed as listed below.

Control Jumpers
(Figure 3-1. Sheet 2, in place as shown)

W1	W4
W2	W5
W3	W6

Logic Level Jumpers
(Figure 3-1. Sheets 1, 2, & 3)

W7, W8, W9, W10	12661A	W7A, W8A, W9A, W10A	12661A, Opt. 01

Output Jumpers
(Figure 3-1. Sheet 3, removed as shown)

W11	W13
W12	W14

Alarm Jumpers
(Figure 3-1. Sheet 1, in place as shown)

MC74 0 through 7
MC73 A through D

2-8. CONTROL JUMPERS. These jumpers are for special applications of the card and are not normally changed from standard. Their functions are:

a. W1A. This jumper used in conjunction with W11, W12, W13, and W14. In position W1A, set side of Command Control FF is used as DVS Program Card command line.

b. W2A and W3A. These jumpers reverse the output of the Timer FF (MC77). Used when peripheral device Flag to card is high when busy and low when not busy.

c. W4A. In this position the jumper will inhibit STF and CLF signals to the Flag Buffer and Alarm Buffer FF's. It will also inhibit IOI and IOO signals to the Mode Request FF and would normally be used in conjunction with W5 and W6 to hard wire card for either Alarm or Timing (Flag) mode interrupts.

d. W4 replaced by R71 (470Ω resistor) to +4.5V enables STF and CLF signals to both Flag Buffer and Alarm Buffer FF's at all times. Use of this resistor also enables IOI and IOO signals at all times but is nullified by W5 and W6.

e. W5 and W6. With W6A in position and W5 replaced by R72 (470Ω resistor) to +4.5V, card is hardwired in the Alarm mode of interrupt. With W5A in position and W6 replaced by R73 (470Ω resistor) to +4.5V, card is hardwired in the Timing (Flag) mode of interrupt.

2-9. LOGIC LEVEL JUMPERS. These jumpers are in position W7, W8, W9 and W10 on the 12661-6001 DVS Program Card used in the 12661A DVS Interface Kit. These jumpers are in position W7A, W8A, W9A, and W10A on the 12661-6002 DVS Program Card used in the 12661A, Option 01 DVS Interface Kit.

NOTE

W10 and W10A is the same position (-2V).

2-10. When jumpers W7, W8, W9, and W10 are moved to the "B" position, -12V is applied to the inverter circuits. This requires replacing all inverter NPN transistors with PNP transistors and reversing all associated diodes.

2-11. OUTPUT JUMPERS. These jumpers are not normally used. They can be installed for 24 bits output to a single peripheral device. When these jumpers are installed, the Address Decoder (MC14) must be removed from the card.

a. W11 becomes Bit 0 in second output word (see Figure 1-1).

b. W12 becomes Bit 1 in second output word.

c. W13 becomes Bit 2 in second output word.

d. W14 connects output of Command Control FF to Command 5 output.

It may be necessary to move W1 to its A position for correct polarity of command line to peripheral device.

2-12. ALARM JUMPERS. Eight jumpers numbered 0 to 7 (MC74) are used to connect Alarm interrupt capability to each Peripheral Status input bit. If an Alarm interrupt is not desired on a particular input, remove the jumper. With the Alarm interrupt circuits disconnected, the status of all peripheral devices can still be monitored through program examination of the Peripheral Status inputs.

2-13. Four jumpers lettered A to D (MC73) are used to form an OR circuit that will set the System Clear bit whenever an Alarm condition occurs. Jumpers 0 to 3 must be in place for this option.

2-14. PROGRAMMING.

2-15. In this text, the initials PSI will be used to represent the select code of the DVS Program Card.

2-16. Since the card is program selected by only one select code, simultaneous input and output operations cannot be performed. The card plugs into any of the interface card input/output (I/O) slots of the computer and assumes the lower select code of that slot.

2-17. USE OF COMMAND, FLAG, SFS, AND SFC.

2-18. When outputting a program to a peripheral device, two words are required. The card is first initialized by CLC PSI or CLC Ø. The structure of the two words has been previously specified in Section I, Figure 1-1. After outputting the second word, the following events occur in the sequence given; each one depending upon the event preceding it.

NOTE

Use of CLC Ø will affect other devices being operated under interrupt.

a. The Command line to the appropriate peripheral device goes true (0V).

b. The peripheral device starts its assignment.

c. The peripheral Flag goes Busy (0V).

d. The Command line to the peripheral device goes false (+V).

NOTE

If the peripheral does not have a "Flag", the Command line can be cleared with CLC PSI.

e. Peripheral device finishes assignment and settles or "times out".

f. The peripheral Flag goes Not Busy (+V).

2-19. If an SFS instruction is executed, the next instruction will be skipped only if the device Flag line is high (+V).

2-20. If an SFC instruction is executed, the next instruction will be skipped only if the device Flag line is ground (0V).

NOTE

SFS and SFC are software commands whose only function is to check status of peripheral device Flag. STF or CLF commands do not enable or disable SFS and SFC commands.

2-21. SOFTWARE CONTROL OF INTERRUPT CHANNEL (See Figure 2-2).

2-22. Figure 2-2 is a representation of Software control of the Interrupt Channel. The main points of Figure 2-2 are; how the DVS Program Card is assigned

to the Timing or Alarm mode of interrupt; and once the assignment is made why further instructions have "NO EFFECT" on the interrupt channel.

2-23. To disable the DVS Program Card interrupt capability prior to interrupt mode assignment, a CLC PSI or CLC Ø command is given. If an interupt request occurs during assignment, the card will not interrupt the computer. The interrupt request will be stored in Flag or Alarm Buffer FF's. Once the interrupt mode is assigned, the stored interrupt request will cause an interrupt.

2-24. After the interrupt mode is assigned, either Timing or Alarms, an STF PSI command followed by STC PSI will cause an immediate interrupt. If, instead of the STF PSI command, a CLF PSI command is given, followed by STC PSI, the Timing or Alarm mode is enabled. Once DVS Card Interrupt is on, OTA, B PSI or LIA, B/MIA, B PSI commands have "NO EFFECT" on the interrupt channel. See paragraph 2-33 for a short Example Program.

2-25. The following description follows Figure 2-2 starting with a CLC PSI or CLC Ø command.

CLC PSI or CLC Ø	Interrupt control FF is cleared which disables the interrupt capability and enables the mode of interrupt assignment.

2-26. At this point a decision must be made on which mode of interrupt is desired.

OTA/B PSI or	Mode Request FF is set which assigns the interrupt channel to a Timing Mode.
LIA/B PSI or MIA/B PSI	Mode Request FF is cleared which assigns the interrupt channel to an Alarm Mode.

2-27. After selecting either the Timing mode or Alarm mode, another decision may be made on requesting an immediate interrupt by setting the Flag or Alarm Buffer FF's (STF PSI), or, clearing any previous interrupt requests (CLF PSI). A third choice is possible which is not shown on Figure 2-2. The command STC PSI can be given which will either cause an immediate interrupt or enable the interrupt mode depending on the status of the Flag or Alarm Buffer FF's.

STF PSI	Flag or Alarm Buffer FF is set and a Timing or Alarm interrupt is requested. The next machine cycle will set the Flag FF.

STC PSI	This instruction will cause an immediate interrupt.

2-28. If the decision is made to clear any previous interrupt requests, the Flag or Alarm Buffer FF's must be cleared.

CLF PSI	This instruction clears the Flag or Alarm Buffer FF's which erases a Timing or Alarm interrupt request. At the same time the Flag and Interlock FF's are cleared. If an interrupt request still exists, the next command (STC PSI) will gate it through.
STC PSI	This instruction enables the Timing or Alarm interrupt.

2-29. Once the mode of interrupt has been set, the STC command enables the interrupt and prevents OTA, B PSI or LIA, B/MIA, B PSI commands from altering the mode. These commands are shown on Figure 2-2 as having "NO EFFECT". At this point in the program these commands are used to output or input data between the DVS **Program Card** and computer.

STC PSI	Interrupt Control FF is set which enables interrupt.

2-30. The next choice of commands, as shown on Figure 2-2, have "NO EFFECT" on interrupt mode assignment.

OTA/B PSI or MIA/B PSI or LIA/B PSI then	At this point in program, used to input or output data. See Figures 1-1 and 1-2.
STF PSI	No effect on Flag or Alarm Buffer FF's.
or CLF PSI	The Flag and Interlock FF's are cleared which closes the interrupt priority string. The Flag and Alarm Buffer FF's are not affected.

2-31. If, after assigning the mode of interrupt, an interrupt should occur, it is not necessary to recycle from CLC PSI. The instruction CLF PSI will clear the Flag and Interlock FF's which again enables the interrupt. Upon initiation of an interrupt, the Flag Buffer or Alarm Buffer FF's are cleared and the Interlock FF is set by the Interrupt Acknowledge (IAK) signal. The Interlock FF then prevents additional interrupts until cleared by software (CLF, PSI). A CLF PSI instruction will not clear the Word Sequence FF's. Therefore, a new first word cannot be programmed.

2-32. To clear the Word Sequence FF's it will be necessary to recycle from CLC PSI. The DVS Program Card will now recognize the next OTA/B as a first word.

2-33. PROGRAM EXAMPLE.

2-34. The following sample program illustrates input and output programming through the DVS Program Card using HP Assembler Language.

Label	Operand	Explanation
	CLC PSI, C	Enable interrupt assignment and initialize.
	LIA PSI	Assign interrupt channel to alarms.
	LDA WD1	Load A and B registers with 1st and 2nd
	LDB WD2	word output data from memory storage.
	JSB OUTPT	Jump to output subroutine.
NOTE:	If LIA PSI in the above program were replaced by OTA PSI, the interrupt channel would be assigned to timing.	
OUTPT	NOP	Entry point OUTPUT subroutine.
	CLC PSI	Initialize Word Sequence Counter.
	STC PSI	Disable interrupt mode assignment and Enable interrupt channel.
	OTA PSI	Output 1st data word.
	OTB PSI	Output 2nd data word and command external device to accept the data.
	SFS PSI	Is external device busy?
	JMP * -1	Yes. Jump to previous instruction.
	JMP OUTPT, I	Exit this subroutine.

Table 2-1. DVS Program Card 48-Pin Connections.

Signal	Pin	Signal	Pin
	Input Word		
Status 0	16	Status 5	19
Status 1	T	Status 6	V
Status 2	17	Status 7	18
Status 3	U	Flag	S
Status 4	W		
Output (First Word)			
Bit 0	D	Bit 8	11
Bit 1	5	Bit 9	M
Bit 2	4	Bit 10	N
Bit 3	K	Bit 11	12
Bit 4	9	Bit 12	R
Bit 5	10	Bit 13	14
Bit 6	L	Bit 14	13
Bit 7	E	Bit 15	P
Output (Second Word)			
Bit 3	F	Command 2	C
Bit 4	J	Command 3	7
Bit 5	8	Command 4	3
Bit 6	6	Command 5	A
Bit 7 (System Clear)	15	Command 6	1
Command 0	H	Command 7	B
Command 1	2	Ground	BB, AA, Z, Y 24, 23, 21, 22

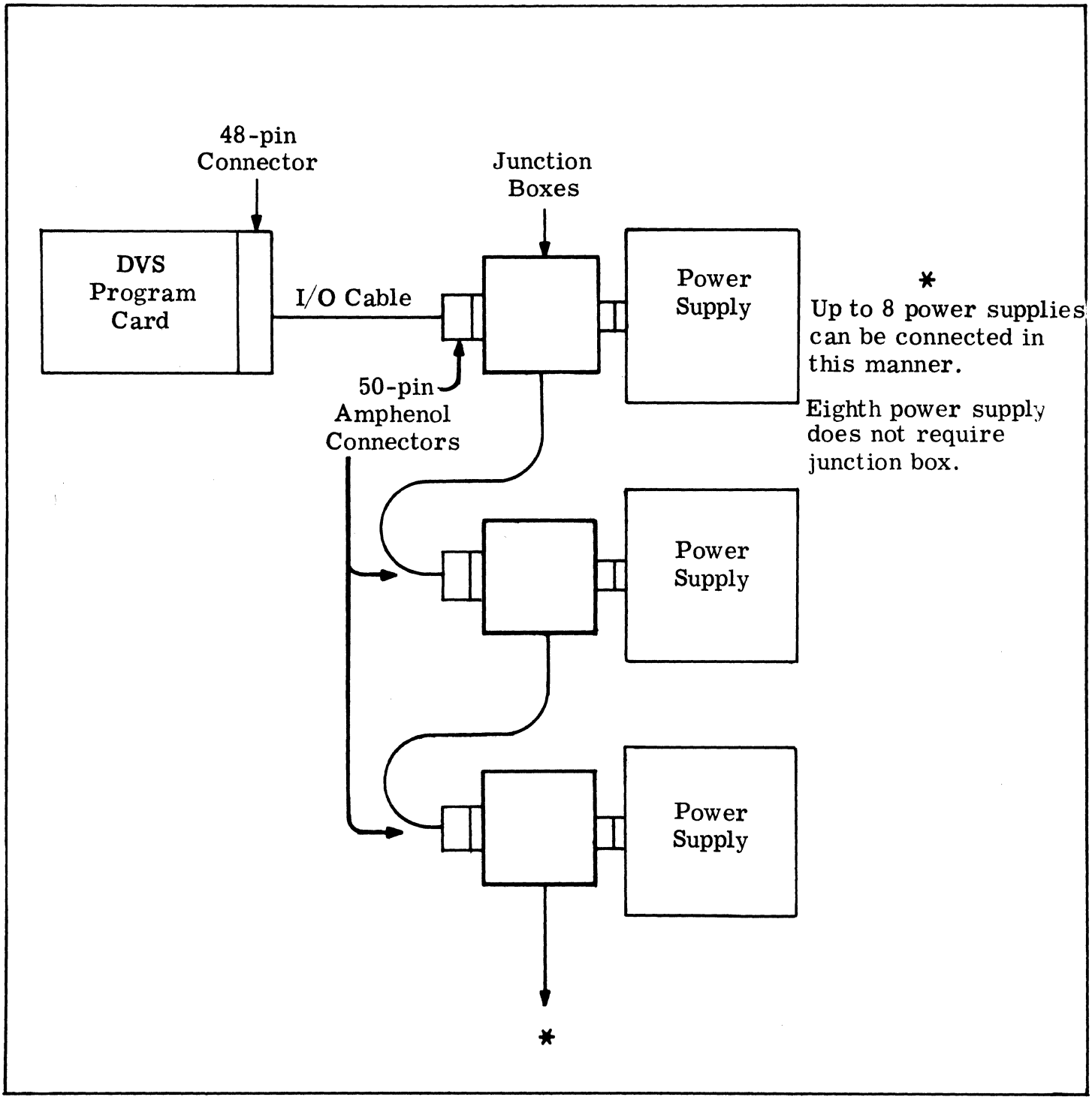


Figure 2-1. Recommended Method of Interconnecting Power Supplies.

The effect of an instruction (XXX PSI) on a flip-flop [XXXX F F] depends on the status of other flip-flops as shown.

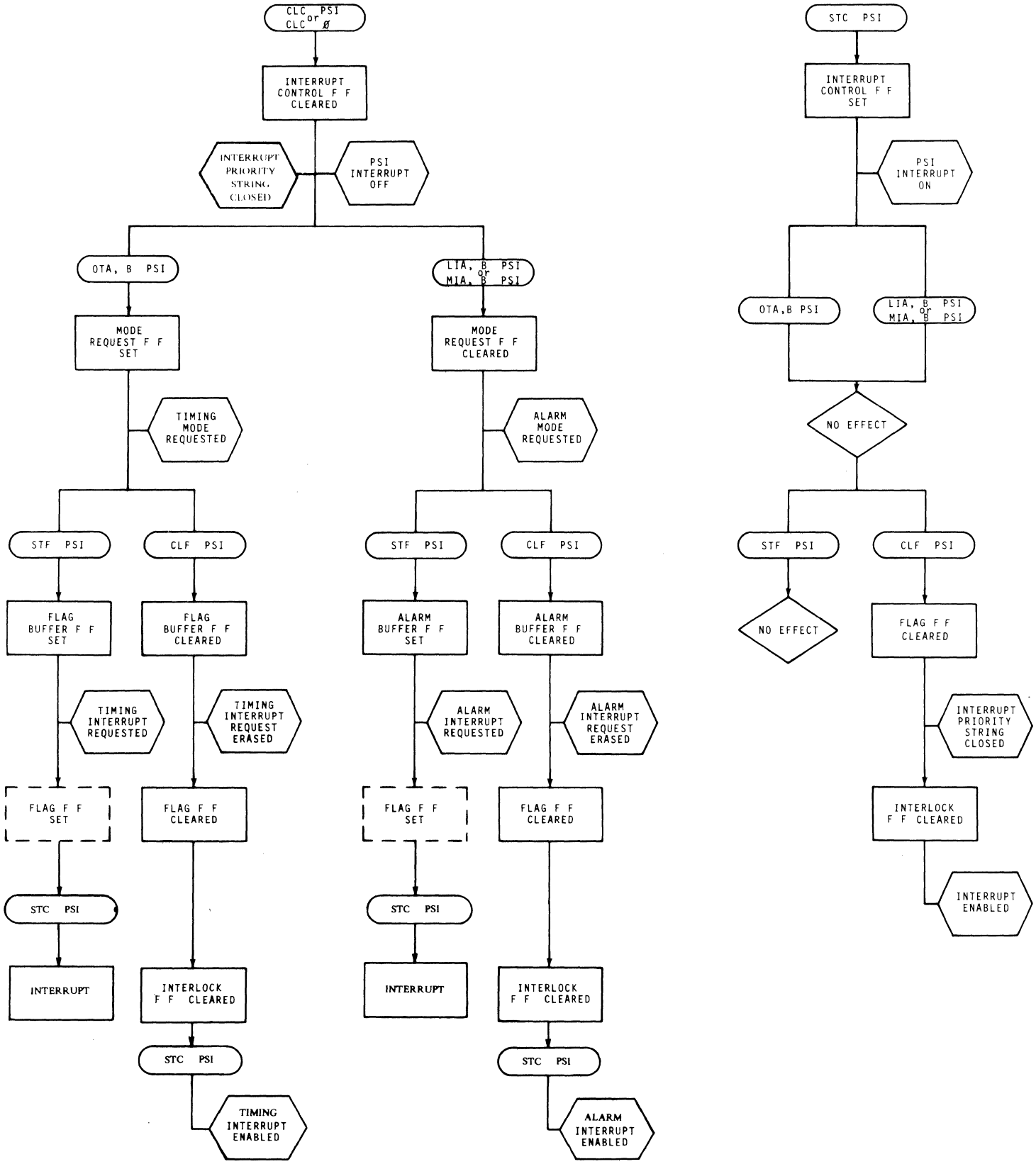


Figure 2-2. Software Control of Interrupt Channel

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section of the Manual is divided into three main parts. Figure 3-1 is the schematic diagram of the DVS Program Card and is divided into three sheets. Control Signals; refer to Sheet 2: Input Operations; refer to Sheet 1: Output Operations; refer to Sheet 3. Located within the main parts are other operations such as Interrupt, Computer Power On, etc. Figure 3-2 is a typical Interrupt System Timing diagram to aid in describing Interrupt Operation. PSI is used in this text to represent the Select Code of the DVS Program Card.

3-3. CONTROL SIGNALS.

3-4. INITIALIZATION.

3-5. Refer to Sheet 2 of Figure 3-1. The DVS Program Card must be initialized by a CLC instruction with a Select Code of ØØ or with the Select Code of the interface card. The IOG and Select Code signals gate through MC15 and MC16 pin 6 to enable the command gates of the card. Output instructions of OTA and/or OTB follow to output 24 data bits from the A and/or B registers.

3-6. When the card is given a CLC instruction through pin 21, Word Sequence FF1 and FF2 are cleared. The reset output terminal for FF2 (pin 6, MC46) goes high (+V). This allows the first IOO signal at pin 20 (caused by the first OTA/B PSI instruction) to be gated through MC46 pin 8 and MC56 pin 6 to the Latch inputs of the First Output Word Registers (Sheet 3). This first IOO signal also sets Word Sequence FF1 by pulling pin 13 MC36 low (0V) which causes pin 11 of MC36 to go high. When the IOO pulse returns to its normally low state, pin 13 of MC36 and pin 12 of MC35 go high. This makes pin 1 of MC46 low, which sets Word Sequence FF2 causing pin 12 of MC46 to go high.

3-7. After the first OTA/B PSI instruction, both Word Sequence FF's are set. The second IOO signal is gated through inverting MC27 pin 11 and MC37 pin 4 to MC46 pin 13. Both inputs (12 and 13) to MC46 are now high which causes pin 11 of MC46 to go low which causes pin 8 of MC56 to go high. The second IOO signal from MC56 pin 8 goes to the Latch inputs of the Second Output Word Registers (Sheet 3). When MC46 pin 11 went low, it pulled pin 12 of MC65 low which set the Command Control FF.

3-8. The first IOO signal to the card, as a result of the first OTA/B instruction, latches the First Word Output Storage Register FF's (see Sheet 3). The first word data (16-Bits) is then available to the peripheral device. The second IOO signal to the card (second OTA/B instruction) latches the Second Word Output Storage Register FF's. The second word data (8-Bits) is then available to the peripheral device and the Address Decoder. The Address Decoder was enabled when the second IOO signal set the Command Control FF. The signal from the Command Control FF, together with the address data bits (second word bits 0, 1, 2 through the Address Decoder), cause a command to be sent to one of the eight possible peripheral devices.

3-9. As the commanded peripheral device is accepting data, it will make the Flag (pin S) low which resets the Command Control FF. When the Command Control FF resets, the Command line returns to its normally high (off) state. When the peripheral device completes its operation, the Flag returns to its normally high (off) state.

3-10. The second IOO signal sets the Command Control FF which, in turn, sets the Status Flag FF (MC77). While the Status Flag is set, MC67 pin 5 is low which disables the SFS PSI instruction (pin 25). SFS to the DVS Program Card means skip the next instruction if the peripheral device Flag Line is high (+V). When the Flag Line goes low, which resets the Command Control FF, the Status Flag FF remains set. When the Flag returns to its high state, the Status Flag FF is reset which makes MC67 pin 5 high and enables the SFS PSI instruction. The Flag Line, in returning to its high state, generates a pulse through MC67 pin 8 that makes MC55 pin 9 low and sets the Flag Buffer FF. This would cause a "Timing (Flag) interrupt" if the interrupt system and channel were enabled and assigned to "Timing".

3-11. To output additional data to the peripheral devices, the card must receive a CLC PSI or CLC Ø command to initialize the word sequence FF's. If the card is not reset with a CLC instruction, then every output instruction (OTA/B) will cause the card to react as if it were a second IOO signal. Erroneous data could then be received by one of the peripheral devices.

3-12. INTERRUPT OPERATION.

3-13. Refer to Figure 3-2. The card will recognize two types of interrupt from the peripheral device it is programming. One interrupt method is called Timing (Flag) and sets the Flag Buffer FF. This interrupt may request an interrupt to the computer program to obtain new data from the computer. The second interrupt method is called Alarms and sets the Alarm Buffer FF. This interrupt is a signal to the computer that one of the peripheral devices has failed. Program examination of the Status inputs (see Figure 1-2) will determine the faulty unit only if the unit remains faulty. If the peripheral that caused the Alarm returns to normal, the Status Bits return to normal.

3-14. TIMING MODE. The interrupt channel may be assigned to a "Timing mode" using the Flag Buffer FF to generate interrupts. A CLC PSI or CLC Ø instruction pulls MC36 pin 5 low which resets the Interrupt Control FF and enables the channel assignment. If the Interrupt Control FF is reset, an IOO signal (from OTA/B instruction) will pull MC25 pin 4 low which sets the Mode Request FF. This makes MC54 pin 2 high which, together with SIR (T5) signal and the Flag FF being reset, sets the Mode Control FF. When the Mode Control FF sets it makes MC25 pin 1 high which allows the Flag Buffer FF to reset on an IAK (Interrupt Acknowledge) signal. In the reset condition, a STF command will set the Flag Buffer FF which pulls pin 9 of MC65 low and sets the Flag FF. A CLF command will gate through MC17 pin 3, pull pin 2 of MC66 low and reset the Flag FF. In this "Timing mode", the Alarm Buffer FF is disabled from the STF, CLF commands and the Flag FF.

3-15. ALARM MODE. The interrupt channel may be assigned to an "Alarm mode" using the Alarm Buffer FF to generate interrupts. If the Interrupt Control FF is not set, an IOI signal (from LIA/B, MIA/B instructions) will pull MC15 pin 11 low which resets the Mode Request FF. This makes MC54 pin 2 low which, together with SIR (T5) signal and the Flag FF being reset, resets the Mode Control FF. When the Mode Control FF resets, it makes MC35 pin 10 high which allows the Alarm Buffer FF to reset on an IAK signal. In the reset condition, a STF command will set the Alarm Buffer FF which pulls pin 9 of MC65 low and sets the Flag FF. A CLF command will gate through MC17 pin 3, pull pin 2 of MC66 low and reset the Flag FF. In this "Alarm mode", the Flag Buffer FF is disabled from the STF, CLF commands and the Flag FF.

3-16. I/O INTERRUPT. To insure that input and output instructions do not assign the interrupt channel to an incorrect mode, the Interrupt Control FF must be set by a STC PSI instruction. With the Interrupt Control FF set, pin 6 of MC36 is low which inhibits MC25 pin 13 and MC17 pin 10. This prevents the IOI and IOO signals from changing the Mode Request and Mode Control FF's which would change the interrupt channel assignment. The STC command will also inhibit pins 4, 11 and 13 of MC26 and pin 2 of MC15 which will stop the STF, CLF instructions from changing the Flag Buffer and Alarm Buffer FF's.

3-17. To generate an interrupt request to the computer, the Interrupt Control FF must be set by a STC PSI instruction; the I/O Interrupt system must be enabled by a STF Ø instruction (IEN High); the Flag FF and appropriate Buffer FF must be set. Then if an interface card (device) of higher priority is not requesting an interrupt (PRH line high) the Interrupt Request FF (IRQ-FF) will be set.

3-18. The IRQ FF output provides the FLG (Flag) signal through pin 9 MC87 and the IRQ signal through pin 13 MC87 to the I/O Address Card. These two high signals cause a Service Request Address to be enabled to the computer.

The Flag signal forms an Interrupt signal which is sent to the computer. The IRQ FF is reset by the ENF signal at time T2 in the computer cycle. This allows a higher-priority device to request an interrupt. If the Flag FF and appropriate Buffer FF are still set and no higher-priority devices have requested an interrupt, the IRQ FF will again be set at time T5 (SIR).

3-19. During Interrupt Phase 4, the computer decrements the P-register by one to ensure that the proper location in the main program will be returned to after the interrupt is processed. (The P-register was incremented by one at time T7 of the last machine phase of the main program by the SPC (Step Program Counter) signal.) Also, the computer places the Service Request Address (which is always equal to the Select Code of the interrupting device) from the I/O Address card into the M-register at time T7. This causes the next instruction to be read from the memory location having the same number as the Service Request Address (Select Code) during the Fetch Phase (Phase 1). This location in memory is referred to as the "interrupt location" and is reserved for that particular device. Example: A device specified by a Select Code of 10 will interrupt to (i.e., cause execution of the contents of) memory location 00010. At time T3 of Phase 4, the interrupt system is inhibited by the false Enable Service Request signal until the Fetch Phase following the execution of the instruction at the interrupt location. This prevents interrupts from occurring until at least one instruction has been executed (except in the case of JMP, I and JSB, I instructions).

3-20. At time T1 of Fetch Phase 1 the I/O Control Card sends an IAK (Interrupt Acknowledge) signal to the DVS Program Card. If the IRQ FF is set, the IAK signal gates through MC57 pin 8 and resets the appropriate Flag or Alarm Buffer FF. Since the set-side output of the Buffer FF is ultimately applied to MC73, resetting the Buffer FF prevents the setting of the IRQ FF and causing another interrupt. The IAK signal also sets the Interlock FF by pulling pin 1 of MC35 low and in so doing, disables the interrupt channel on the DVS Program Card. The Buffer FF's may now be set without generating an interrupt. A CLF PSI instruction will clear the Interlock FF and allow the Buffer FF to initiate another interrupt signal. For the CLF PSI not to clear the Buffer FF, the Interrupt Control FF must be set with a STC PSI instruction.

3-21. At time T2, the ENF signal resets the IRQ FF. The computer fetches the instruction in the interrupt location which will usually be a jump to a subroutine (JSB,I) instruction, although any legal instruction may be placed in the interrupt location. The contents of the P-register plus one is stored in the first location (X) of the subroutine. (Since the previous contents of the first memory location are destroyed when P+1 is stored, the first instruction of the subroutine should always be a no-operation (NOP) instruction or equivalent.) The location of the subroutine (X+1) is placed in the P- and M-registers, and the computer resumes normal subroutine operation. Thus, the instruction at location X+1 is the first instruction of the subroutine to be executed. The

contents of the working registers that were in use in the main program should be stored when entering the subroutine and restored before exit from the subroutine. The exit from the subroutine is made with a JMP,I to location X. This places the address of the interrupted program instruction in the P- and M-registers and normal program operation resumes.

3-22. COMPUTER POWER ON.

3-23. When power is initially applied to the computer, the POPIO(B) and CRS signals are received by the DVS Program Card from the I/O Control Card. These signals establish initial conditions for the operation of the Card and cause the SYSTEM CLEAR signal to appear on the output.

3-24. The POPIO(B) signal (pin 17) performs these functions:

a. Clears the Flag FF.

b. Clears the Flag Buffer FF and Alarm Buffer FF.

c. Clears the Mode Request FF which clears the Mode Control FF and assigns the interrupt channel to the Alarm mode.

d. Sets all output Storage Buffers to Logic "0" (IOBO is held Low during this period).

e. Sets the SYSTEM CLEAR to a Logic "1" (output low).

3-25. The CRS (Control Reset) signal (pin 13) performs these functions:

a. Clears the Interrupt Control FF.

b. Clears both Word Sequence FF's.

c. Clears the Command Control FF.

3-26. SELECT CODE-CARD ADDRESS.

3-27. A program instruction with the Select Code of the DVS Program Card directs an Input/Output Command to the Card. The proper Select Code provides SCL (Select Code Least Significant Digit) and SCM (Select Code Most Significant Digit) signals to the Card. These signals are enabled by the IOB(B) (Input/Output Group Instruction (Buffered)) signal. Refer to Volume Three of the Computer Manuals INPUT/OUTPUT SYSTEM OPERATION, Figure 2-3, to determine the Select Code number for the Interface Card slot used.

3-28. INPUT OPERATIONS.

3-29. DATA INPUT.

3-30. See Sheet 1 of Figure 3-1. The Input Storage Register FF's of the DVS Program Card follow the status of the input lines from the peripheral device. Each Input Storage Register is automatically set to the state of the status line during each computer cycle. These input registers account for 8 of the 11 data bits that may be received by the computer from the Card. The remaining 3 bits are status bits from the Mode Control FF (Bit 15), Mode Request FF (Bit 13), and System Clear (Bit 14).

3-31. The computer accepts data from the Card by an LIA, LIB, MIA, or MIB instruction. These instructions generate an IOI signal (pin 24, Sheet 2) which gates through MC17, MC16 pin 12 to MC97 pin 14 which enables the data bits to the computer.

3-32. ALARMS.

3-33. The eight Input Storage Registers may be used to cause an "Alarm Interrupt" if an alarm condition (peripheral failure) exists on any of the input status lines. The appropriate alarm jumpers (0-7) to MC74 must be in place. When the input status line changes from its high (off) state to its low (on) state, a pulse is generated through MC75 pin 4 that sets the Alarm Buffer FF (MC55 pin 4). This will generate an Alarm interrupt if the interrupt system and channel are enabled and assigned to "Alarms".

3-34. Peripheral Status 0 line will be used as an example to explain how an Alarm pulse is generated. When Status 0 line goes low, transistor Q31 turns off and the input to Input Bit 0 FF (pin 2, MC103) goes high. When the latch pulse from the SIR line is received at pin 13 of MC103 at time T5 in the Computer Cycle, the set output of the FF (Q) goes high. Since the Alarm FF (MC93) is not set, its reset output ($\overline{Q}$) will also be high. These two high outputs will enable the input of MC83 making pin 11 low. If Alarm jumper 0 is in place, pin 6 of MC74 will be low making pin 8 high. Pin 3 of MC75 is high and pin 4 goes low. When MC75 pin 4 goes low, it pulls pin 4 of MC55 low which sets the Alarm Buffer FF.

3-35. After Input Bit 0 FF is set at computer time T5, the input of Alarm 0 FF (pin 2 MC93) is high. The output of Alarm 0 FF will not change, however, until the latch input (pin 13, MC93) receives a positive pulse from the ENF line at time T2 in the next computer cycle. This latch pulse causes the reset output of Alarm 0 FF ($\overline{Q}$) to go low which makes the alarm at pin 11 of MC83 high. Since Alarm 0 FF is now set, the set output (Q) is high and IOBI 0 may be enabled through MC106 by an IOI pulse from an LIA/B PSI or MIA/B PSI instruction.

3-36. Before another Alarm pulse can be generated from the Peripheral Status 0 line, both Input Bit 0 FF and Alarm 0 FF must be reset. These FF's are reset by the input line returning to its normally high state. If the input line again goes low, another alarm pulse will be generated beginning at time T5 and extending to time T2 of the next Computer Cycle.

3-37. OUTPUT OPERATIONS.

3-38. Refer to Sheet 3 of Figure 3-1. The output data bits are transferred from the Computer A or B Register to the DVS Program Card through the IOBO (I/O Bus Output) lines. The IOBO signal levels are -0.5V (Logic "0"), or +2.5V to +4.5V (Logic "1"). There are three types of output circuits: First and Second Word Output Data Storage, Second Word Command Address, and SYSTEM CLEAR. Each of these circuits will be explained.

3-39. FIRST/SECOND WORD OUTPUT.

3-40. First and second word output data storage will be explained using IOBO 3 as an example. A Logic "0" from IOBO 3 (pin 45) is applied to the inputs of both the output storage FF's (First Word Latch input = pin 7, MC43, Second Word Latch input = pin 7, MC33). To transfer the Logic "0" to pin k (first output word bit 3), a positive going latch pulse must be applied to pin 4 of MC43. To transfer the Logic "0" to pin F (second output word bit 3) a positive going latch pulse must be applied to pin 4 of MC33.

3-41. The positive going latch pulses originate from the Word Sequence FF's or the POPIO (B) signal (pin 8, MC37) and are passed through pin 6 or pin 8 of MC56. When the pulse applied to the L input of the latches goes high, the output ($\overline{Q}$) of the latch will reflect the inverse of the input. Since the input (pin 7 MC43 and MC33) is held high by IOBO 3 being low (Logic "0"), the $\overline{Q}$ output (pin 8, MC43 and MC33) will go low when the positive going latch pulse is applied to the L input (pin 4, MC43 and MC33). The $\overline{Q}$ output (pin 8) will "latch" in its low state when the latch pulse (L) goes low. When the $\overline{Q}$ output (pin 8) is low, the output buffer transistor (Q17 or Q11) will be cut off and the output line will go high (+V).

3-42. A POPIO(B) signal will apply latch pulses to all the data output storage registers when all the IOBO lines are Logic "0". This Logic "0" will be transferred to the data output lines.

3-43. A Logic "1" is transmitted to the output data line in the same manner. If IOBO 3 goes high (Logic "1"), the input (pin 7 MC43) will go low. When the Latch pulse (L) goes high, the $\overline{Q}$ output (pin 8) will go high and latch when the latch pulse falls. Since the output is high, transistor Q17 will saturate, causing pin k (Bit 3, first word) to go low (Logic "1", 0V).

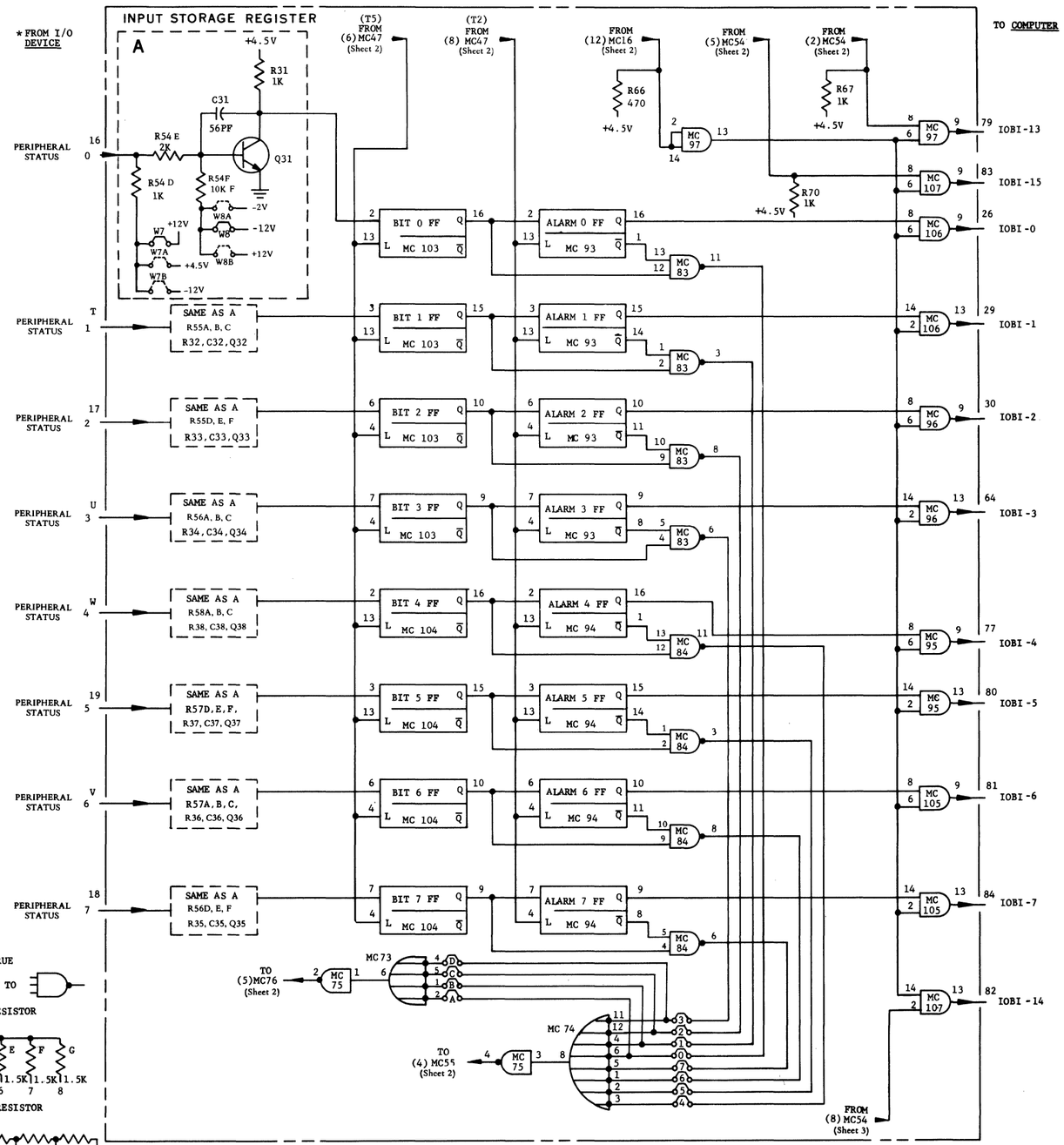
3-44. SECOND WORD COMMAND.

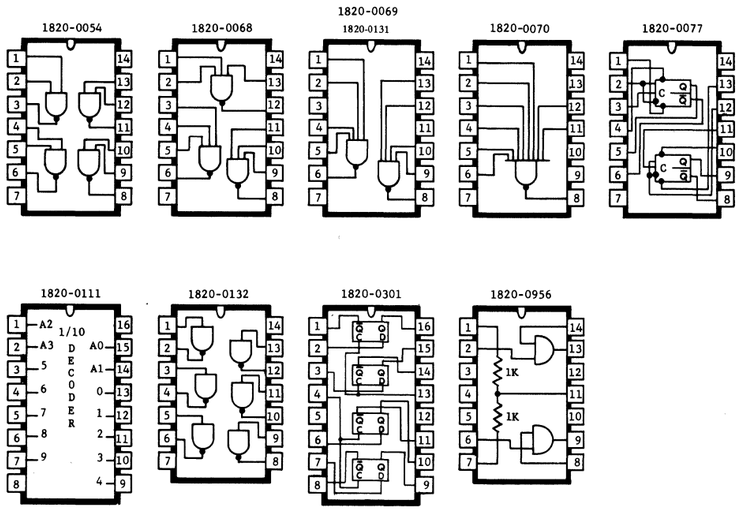
3-45. The command line Address Code (second word output bits 0, 1, 2, see Figure 1-1) is transferred to the input of the Address Decoder the same way second word output data is transferred to the output lines. The Address Decoder is a 4 Line (BCD) to 10 Line (decimal) converter. None of the Command 0 to Command 7 lines can be activated while pin 2 of MC14 is held high since this enables a decimal 8 or higher coded output line. Pin 2 of MC14 is held high while the Command Control FF is clear. When the Command Control FF is set (from the second IOO signal), pin 2 goes low and the binary code from pins 1, 14 and 15 determines which output line is activated. The output command line is held low (Logic "1") during the time the Command Control FF is set. This sends a command signal to the proper peripheral device.

3-46. SYSTEM CLEAR.

3-47. The System Clear output register is similar to the second word data output registers except it has a Reset terminal (pin 13, MC54). If, through a software instruction, IOBO 7 goes high, then pin 12 of MC54 goes low. The second IOO signal (see paragraph 3-7) makes MC46 pin 11 (Sheet 2) low which is applied to pin 11 of MC54. The $\overline{Q}$ output (pin 8, MC54) will go high saturating transistor Q29 which causes the SYSTEM CLEAR line to go low (0V).

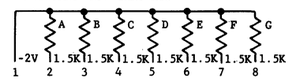
3-48. A System Clear command is also generated by POPIO(B) signals when the computer is initially turned on. Also an Alarm input from the input storage registers through jumpers A-D may generate a System Clear command. The POPIO(B) signal and the alarm pulses are applied to pin 13 of MC54 (Reset terminal). This Reset Command causes pin 8 of MC54 to go high which makes the SYSTEM CLEAR line low (0V).



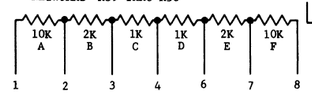


HP NO. 1820-	0054	0068	0069	0070	0071	0077	0111	0132	0301	0956
GND. PIN NO.	7	7	7	7	7	7	8	7	12	5
Vcc PIN NO.	14	14	14	14	14	14	16	14	5	12
Vee PIN NO.	-	-	-	-	-	-	-	-	-	11

1. ALL LOGIC IS POSITIVE-TRUE
2. IS EQUIVALENT TO
3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R59 THRU R63



4. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R39 THRU R58



5. * INDICATES SIGNALS FROM/TO EXTERNAL DEVICE VIA 48-PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM/TO COMPUTER VIA 86-PIN CONNECTOR.

6 POSITION JUMPERS W7A, W8A, W9A FOR 12661A-OPTION 01

Figure 3-1. DVS Card, Schematic Diagram (Sheet 1 of 3)

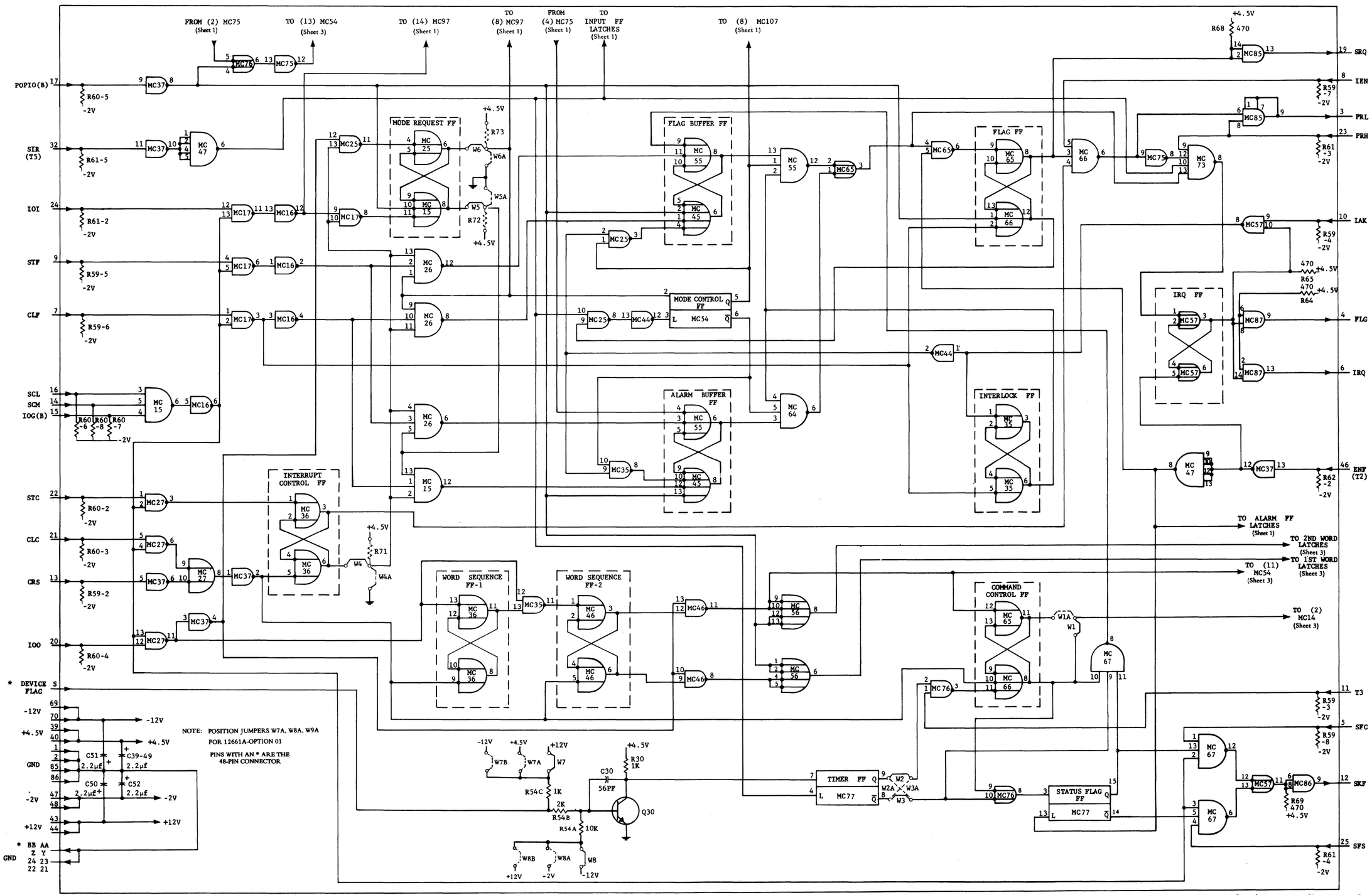
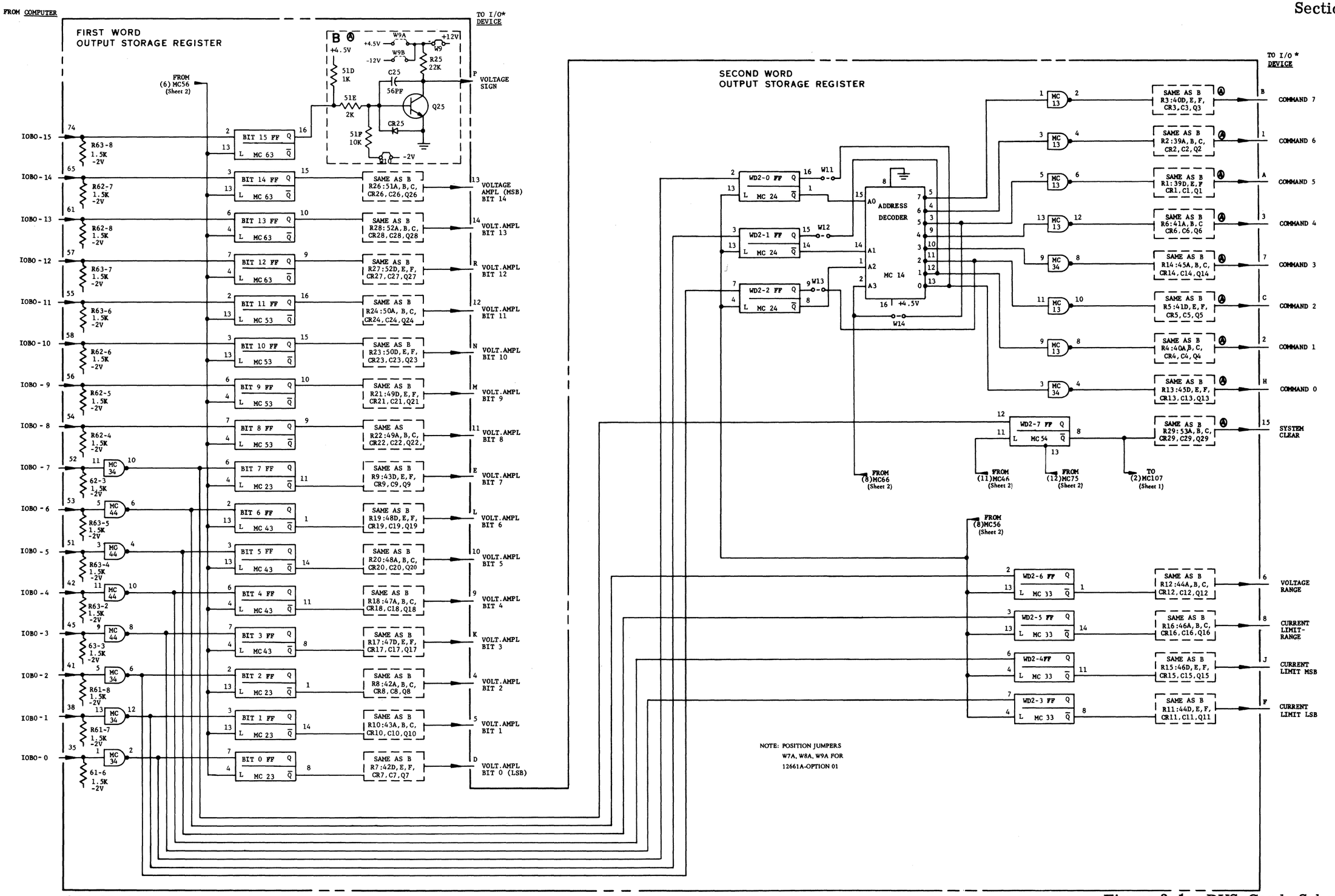
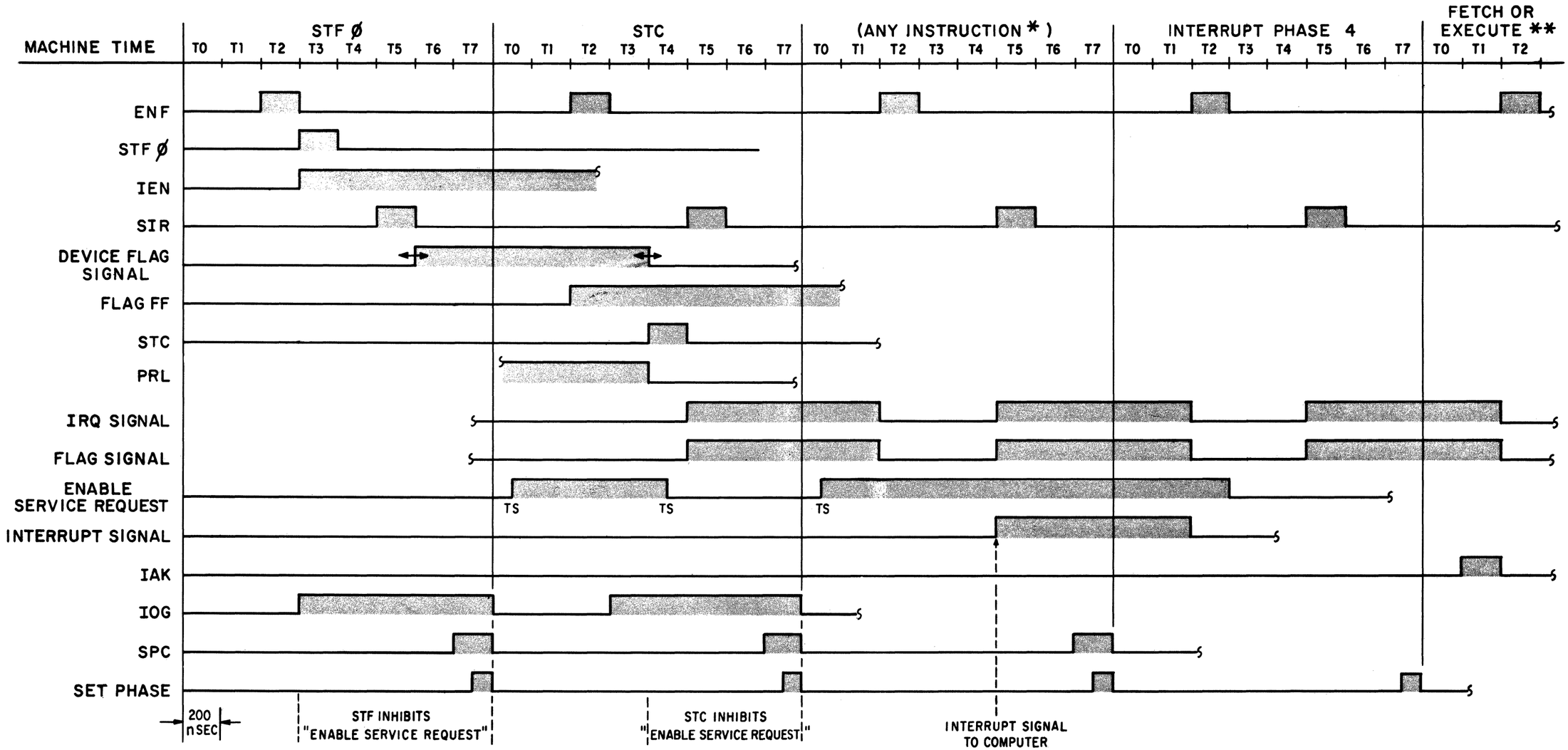


Figure 3-1. DVS Card, Schematic Diagram (Sheet 2 of 3)



A STARTING WITH REVISION CODE B-1031-6, THE CONNECTION OF THE 1K RESISTORS TO THE +4.5V BUS IS OPENED IN THE CIRCUITS FOR COMMANDS 0 THRU 7. REVISION CODE WAS A-902-6.

Figure 3-1. DVS Card, Schematic Diagram (Sheet 3 of 3)



NOTES:

* EXCEPT STF, CLF, STC, CLC, JMP I, AND JSB I.
** EXECUTE IF A SINGLE CYCLE INSTRUCTION.

Figure 3-2. Interrupt System Timing

SECTION IV
MAINTENANCE

4-1. DIAGNOSTIC PROGRAM DESCRIPTION.

4-2. The objective of this program is to check the DVS Program Card and verify that it is operating correctly. This program may also be used for troubleshooting and diagnostic tests on the card. A peripheral device is not required for the tests.

4-3. The program consists of a background control program which contains four task routines. Information controlling message printout and task performance is supplied through the Teleprinter and Switch Register. The first task routine inserts the address of the DVS Program Card into all I/O instructions. The second task routine (INITIAL TEST) checks the Card for initial conditions and POPIO operation. The third task routine (BASIC TEST) checks the flag, control, and interrupt circuitry on the card. The fourth task routine (DATA BUFFER TEST) checks the data buffers and associated discrete circuitry by outputting combinations of 8 bits, 5 bits and 3 bits.

4-4. HARDWARE REQUIREMENTS

4-5. Hardware requirements to test the DVS Program Card are as follows:

a. Any HP Computer (2114, 2115, 2116).

b. Teleprinter (HP 2752A - modified ASR-33 or HP 2754A modified ASR-35) and associated interface register.

c. An input device to enter the program into memory (e.g., HP 2737 A/B Punched Tape Reader) and required interface. (Teleprinter may be used.)

d. Four, 48 pin test plugs wired according to Table 4-1. HP Part No. 01251-0335 (not pre-wired).

e. DVS Program Card with optional jumpers in the following positions

Control Jumpers
(Figure 3-1. Sheet 2, in place as shown)

W1	W4
W2	W5
W3	W6

Logic Level Jumpers
(Figure 3-1. Sheets 1, 2 and 3 as shown or Opt. 01)

W7 or A	W9 or A
W8 or A	W10 (Sheet 3)

Output Jumpers
(Figure 3-1. Sheet 3, removed as shown)

W11	W13
W12	W14

Alarm Jumpers
(Figure 3-1. Sheet 1, in place as shown)

MC74	0 to 7
MC73	A to D

4-6. SOFTWARE REQUIREMENTS.

4-7. Software requirements are as follows:

a. A binary program tape (Diagnostic Test Software HP 20436A).

b. System Input/Output Teleprinter Driver (for example, SIO 8K Memory HP 20305A).

4-8. DIAGNOSTIC TEST PROCEDURE.

4-9. DVS Program Card.

a. Make sure jumpers conform to paragraph 4-5e.

b. Install test plug number 1.

c. Place interface card (with jumpers and plug) in an I/O slot of the computer such that every slot of higher priority has either another I/O card or a priority jumper card in it. If troubleshooting is to be done it is desirable to use an extender card between the computer and the interface card.

4-10. Teleprinter

a. Place the Teleprinter Interface card in an appropriate I/O slot.

b. Connect Teleprinter Interface card to the Teleprinter.

4-11. Teleprinter Driver

a. Load the SIO Teleprinter Driver tape into memory using the Basic Binary Loader.

b. Set Switch register to 000002.

c. Press LOAD ADDRESS.

Table 4-1. Test Connectors

Output Lines Tested				Test Plug No. 1 Pins Shorted	Input Lines Tested	
Command		0		H-S	Flag Line Input	
	Bit	0	(LSB)	D-16	Peripheral Status	0
	Bit	1		5-T		1
	Bit	2		4-17		2
	Bit	3		K-U		3
	Bit	4		9-W		4
	Bit	5		10-19		5
	Bit	6		L-V		6
	Bit	7		E-18		7
				Test Plug No. 2		
	Bit	8		11-16	Peripheral Status	0
	Bit	9		M-T		1
	Bit	10		N-17		2
	Bit	11		12-U		3
	Bit	12		R-W		4
	Bit	13		14-19		5
	Bit	14		13-V		6
	Bit	15	(MSB)	P-18		7
				Test Plug No. 3		
	Bit	3		F-16	Peripheral Status	0
	Bit	4		J-T		1
Second Word	Bit	5		8-17		2
	Bit	6		6-U		3
	Bit	7		15-W		4
				Test Plug No. 4		
Command		0		H-16	Peripheral Status	0
Command		1		2-T		1
Command		2		C-17		2
Command		3		7-U		3
Command		4		3-W		4
Command		5		A-19		5
Command		6		1-V		6
Command		7		B-18		7

d. Set the Teleprinter I/O address into the switch register.

e. Press RUN.

4-12. DVS Program Card Verification Program.

a. Load the program into memory using the Basic Binary Loader.

b. Set switch register to 000100 (this is the starting address).

c. Press LOAD ADDRESS.

d. Press PRESET then RUN.

4-13. PROGRAM OPERATION

4-14. The initial test will give valid results only when immediately following computer power ON or PRESET. POPIO signals from the I/O backplane cause the data buffers to be preset to the proper state. If the INITIAL TEST is performed after the other task routines have been entered, it will cause error printouts. To perform the INITIAL TEST after the other routines have been entered, push PRESET and restart the program at address 100. The INITIAL TEST can be skipped by setting Switch Register Bit 3 up.

NOTE

2114A Computers, push Bit 3 to light.

a. The Teletype will print: 12661A DIAGNOSTIC PROGRAM.

b. The Teletype will print: I/O CHANNEL?

c. The operator must type (using the Teleprinter keyboard) the address (select code) of the DVS Program Card, followed by a line termination (CARRIAGE RETURN, LINE FEED). To skip INITIAL TEST, set switch 3 up and go to step i.

d. The INITIAL TEST starts at this point. All four test plugs are used. The teletype will tell you when to change to the next plug. The Teletype will print: CONNECT PLUG NO. 1 AND PUSH RUN.

e. If an error occurs at any time in the INITIAL TEST, the Teletype will print OUTPUT = XXXXXX INPUT = XXXXXX, and the computer will halt. Refer to ERROR CODES (paragraph 4-18). To continue, you must push RUN. When the first test using plug no. 1 has been completed, the Teletype will print, CONNECT PLUG NO. 2 AND PUSH RUN.

f. When the second test using plug No. 2 has been completed, the Teletype will print, CONNECT TEST PLUG NO.3 AND PUSH RUN.

g. When the third test using plug No. 3 has been completed, the Teletype will print, CONNECT TEST PLUG NO. 4 AND PUSH RUN.

h. At the completion of the INITIAL TEST, the Teletype will print, CONNECT TEST PLUG NO. 1 AND PUSH RUN.

i. The BASIC TEST starts at this point. If an error occurs at any time in the BASIC TEST, the Teletype will print ERROR 0000XX, and the computer will halt. Refer to ERROR CODES (paragraph 4-18). To continue, you must push RUN.

NOTE

If error is not first corrected, subsequent tests may be invalid.

j. At the end of the BASIC TEST and the beginning of the DATA BUFFER TEST, the Teletype will print: DATA BUFFER TEST PLUG NO. 1. PUSH RUN. Since test plug 1 is already installed, it is only necessary to push RUN. If an error occurs at any time in the DATA BUFFER TEST, the Teletype will print, OUTPUT = XXXXXX INPUT = XXXXXX, and the computer will halt. Refer to ERROR CODES (paragraph 4-18). To continue, you must push RUN.

k. The program now goes through the DATA BUFFER TEST routine, printing error messages or instructions. Each of four test routines checks a portion of the Output Buffers by outputting data through jumpers in the test plugs to the Input Buffers and comparing data output with data input.

l. The Teletype will print END OF DATA BUFFER TEST, and the computer will halt. This statement is at the end of the DIAGNOSTIC PROGRAM. If there were no error messages the DVS Program Card is good.

m. To return to the beginning of the program, set Switch 0 up and push RUN. The program will halt with 102000 in the "T" register (2114A- Memory Data Register). To start the program again, push RUN.

4-15. PROGRAM CONTROL

4-16. The program is controled by the Switch Register switches 0 to 4.

Switch 0 Up	Throw this switch up at any time to halt at beginning of program. The program will halt; A, B, and T REGS. = 102000. (2114 - Memory Data Register) Pushing RUN will enter Program Operation at 4-14b.
Switch 1 Up	This switch will cause a halt at the end of error loop test.
Switch 2 Up	This switch will cause the program to loop around error for oscilloscope testing.
Switch 3 Up	This switch will cause program to skip INITIAL TEST.
Switch 4 Up	This switch will cause the program to loop through entire Basic Test.

4-17. Switches 1 and 2 should be used in conjunction. Switch 1 will allow the operator to determine where he is in the program by observing the computer program counter, and let him decide if he wants the next subroutine to loop or not. Both of these aids can be bypassed by keeping the switches off.

4-18. ERROR CODES.

4-19. Initial Test Errors: If the data to the computer from the interface card is not the same as an appropriate comparison number (internal to program), the following code is printed:

OUTPUT = $XXXXXX_8$ INPUT = $XXXXXX_8$

OUTPUT is the comparison number and INPUT represents the initial status of the data buffers. For test plugs 1, 2, and 4, OUTPUT will be 040000, and for test plug 3, OUTPUT will be 040020. If the error is in bits 13, 14, or 15, it should appear for all test plugs. These bits indicate errors as follows:

BITS 13, 15	If both are set it indicates that POPIO is not resetting the Mode Request Flip-Flop (MC 15 pins 8 and 10).
	If Bit 13 is set but Bit 15 is not, there is more than one error. The other errors will be observed in the next tests.
	If Bit 15 is set but Bit 13 is not, this indicates an error not related to POPIO and will be detected in the next tests.
BIT 14	If not set it indicates that POPIO is not resetting the System Clear Flip-Flop (MC 54 pins 8 and 13, MC 75 pins 12 and 13, and MC 76 pins 4 and 6).

4-20. For test plug 3, the System Clear signal is applied to Bit 4. This Bit should follow the pattern of Bit 14. If Bit 14 is set but Bit 4 is not, it is probably a data buffer error which will appear in the Data Buffer Test. If Bit 14 is in error but Bit 4 is set, it could be a data buffer error, or it could indicate failure of MC 107 pins 2, 13 and 14.

4-21. In addition to these bits, the POPIO signal strobes zeros from the I/O bus to both the first and second word latches. An error in these bits may indicate a data buffer error or failure of MC 56 pins 1, 2, 6, 8, 12 and 13.

4-22. Basic Test Errors: If an error occurs during the Basic Test, the Teletype will print the following error code:

ERROR 0000XX

where XX is an octal number between 00 and 45. When an error number is printed, refer to Table 4-2 for an explanation. Some error codes have correspondingly numbered timing diagrams. Use an oscilloscope to determine the state of the test point. Approximately +4.5V equals logic "1" and ground or OV equals logic "0". The notations on the timing diagrams will inform the operator of the procedure used to diagnose the error.

4-23. Data Buffer Test Errors: If an error occurs during the Data Buffer Test, the Teletype will print the following error code:

OUTPUT = $XXXXXX_8$ INPUT = $XXXXXX_8$

If this happens set the switch register to 3757 and press LOAD ADDRESS. Then clear the switch register and set switches 1 and 2 to allow program looping. Press RUN and observe data buffers with an oscilloscope. By noting which input Bit is in error and checking Table 4-1, it can be determined which data buffer circuit is bad. The oscilloscope should be triggered from either a CLC or a CRS command. Refer to the schematic (Figure 3-1 Sheet 2) to determine a convenient pickoff point for the trigger. The data buffer line should be reset following the CRS signal and set following the CLC signal.

4-24. An interrupt from any other I/O device at any time will halt the program. The address of the interrupting device is the last six bits of the T-Register (2114 - Memory Data Register).

4-25. If an error printout occurs and the diagnostic test is continued without first correcting the error, subsequent tests could be invalid.

4-26. Figure 4-1 in Section 4 is the component location of the DVS Program Card. Use it as a guide in locating the IC packs for troubleshooting.

Table 4-2
Error Codes

CODE NUMBERS	EXPLANATION
ØØ	See timing diagram ØØ
Ø1	See timing diagram Ø1
Ø2	See timing diagram Ø2
Ø3	This error should occur as Ø1 or Ø2. See timing diagram Ø2
Ø4	See timing diagram Ø4
Ø5	See timing diagram Ø5
Ø6	In the halt condition check the following: MC76-9; MC66-8, 10, 11; MC65-12, 13 are all high MC76-10; MC66-9; MC65-11 are all low This checks that*CCFF was reset with CLC command.
Ø7	This error should occur as Ø1, Ø2 or Ø6.
1Ø	See timing diagram 1Ø
11	Set switch register to ØØ2642 and press LOAD ADDRESS. Clear switch register then set switches 1 and 2 up and press RUN. See timing diagram 1Ø. Watch closely*(SFFF).
12	See timing diagram 12
13	Set switch register to ØØ2664 and press LOAD ADDRESS. Clear switch register then set switches 1 and 2 up and press RUN. See timing diagram 12. Watch closely*(SFFF).
14	See timing diagram 14
15	This error should occur as 14.
16	See timing diagram 16
17	See timing diagram 17
2Ø	Set switch register to ØØ2772 and press LOAD ADDRESS. Clear switch register then set switches 1 and 2 up and press RUN. See timing diagram 17. Watch closely*(IFF).
21	This error checks as 2Ø. IFF not resetting.
22	This error checked as 2Ø. Watch closely IAK.
23	While computer is halted check that MC36-3 and MC66-4 is low. MC66-3, 5 and 6 should be high.

Table 4-2. (Cont'd)
Error Codes

CODE NUMBERS	EXPLANATION
24	Set switch register to ØØ2752 and press LOAD ADDRESS. Clear switch register then set switches 1 and 2 and press RUN. See timing diagram 16. Watch closely*ICFF.
25	This error checked as 2Ø. Should occur as 17. IFF not setting.
26	This error checked as 2Ø. Should occur as 21. IFF not resetting.
27	This error should occur as 16.
3Ø	This error should occur as 23.
31	In the halt condition check the following: MC55-3, 4, 6; MC45-9, 10, 12, 13; MC35-8, 10; MC64-3, 4, 5; MC65-3, 4; MC54-6 are all high. MC55-5; MC45-8; MC35-9; MC64-6; MC65-1; MC54-2, 5, 3 are all low.
32	This error checked as 2Ø. Should occur as 17. *IFF not setting.
33	This error checked as 2Ø. Should occur as 21. *IFF not resetting.
34	See timing diagram 34
35	See timing diagram 35
36	See timing diagram 36
37	See timing diagram 37
4Ø	See timing diagram 4Ø
41	See timing diagram 41
42	See timing diagram 42
43	See timing diagram 43
44	See timing diagram 44
45	This error should occur as 35 through 44. See paragraph 4-27. SET CONTROL - An additional test loop to check the set control function. See page 4-21. MODE ASSIGNMENT - An additional test loop to check the mode assignment function. See page 4-22.

* CCFF = Command Control Flip Flop
* SFFF = Status Flag Flip Flop
* ICFF = Interrupt Control Flip Flop
* IFF = Interlock Flip Flop

4-27. Error 45 should not occur. At this point the program is creating alarm signals on all eight alarm inputs. Each input has been checked individually (as errors 35 through 44) and should be caught there. If necessary this could be checked as done by looking at all points referenced in Figure 4-12.

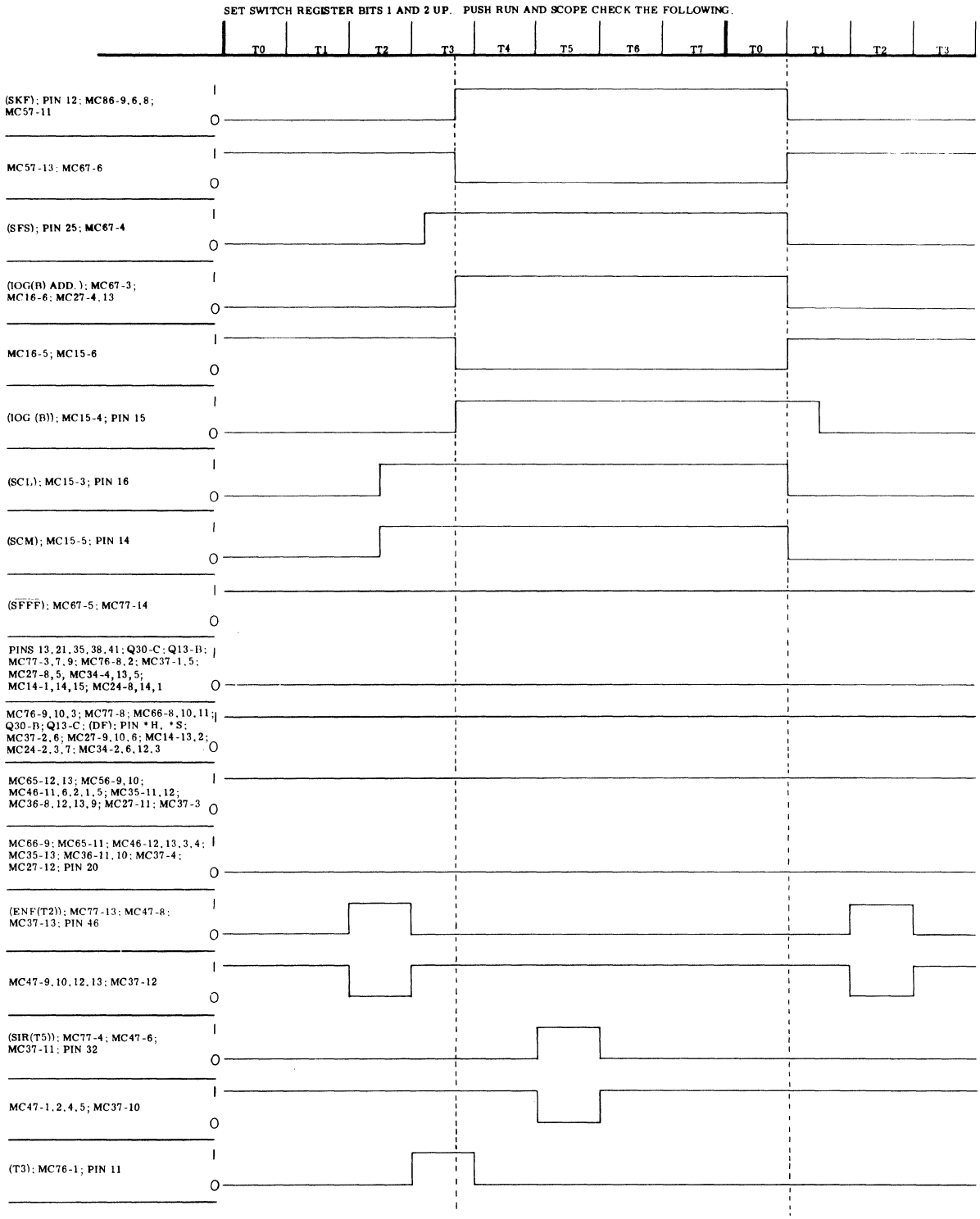


Figure 4-1. Timing Diagram for Error ØØ.

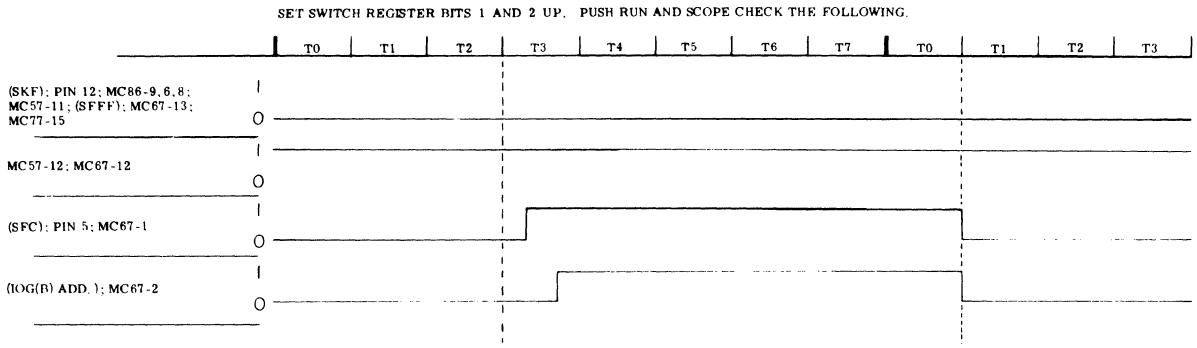


Figure 4-2. Timing Diagram for Error Ø1.

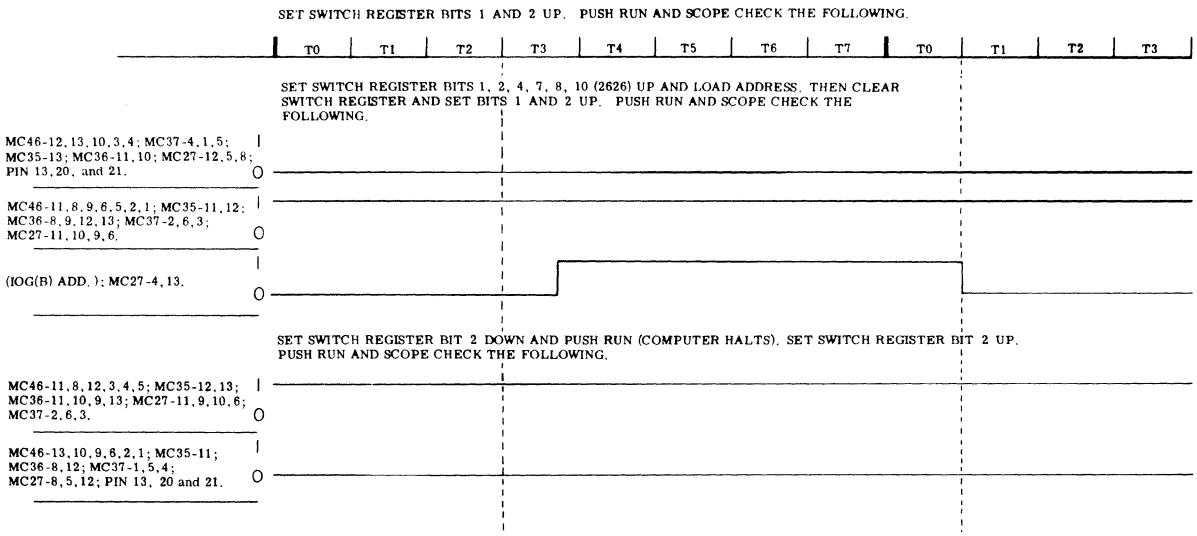


Figure 4-3. Timing Diagram for Error Ø2.

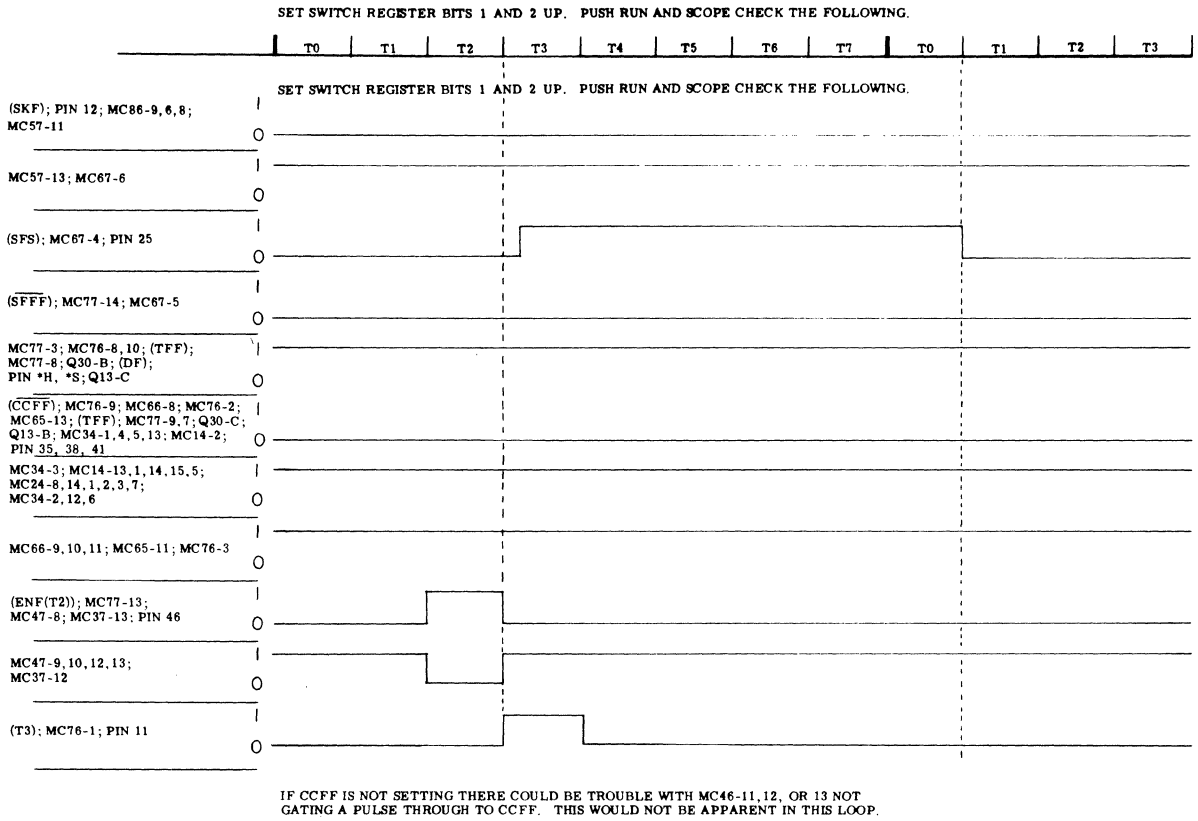


Figure 4-4. Timing Diagram for Error Ø4.

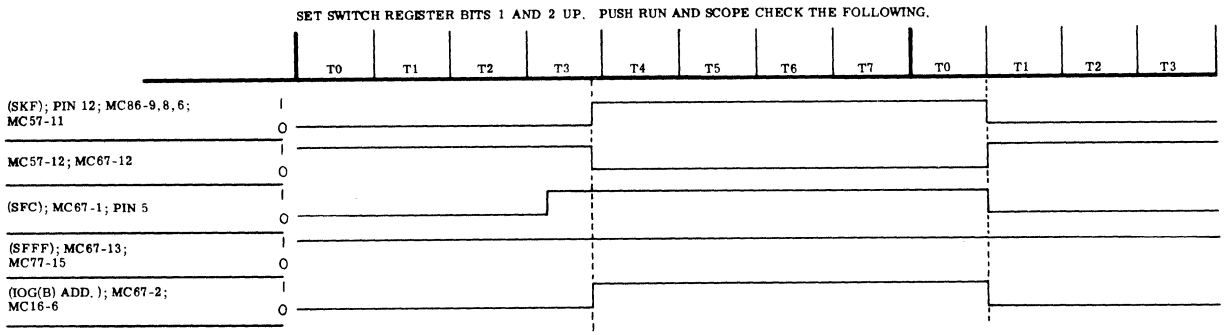


Figure 4-5. Timing Diagram for Error Ø5.

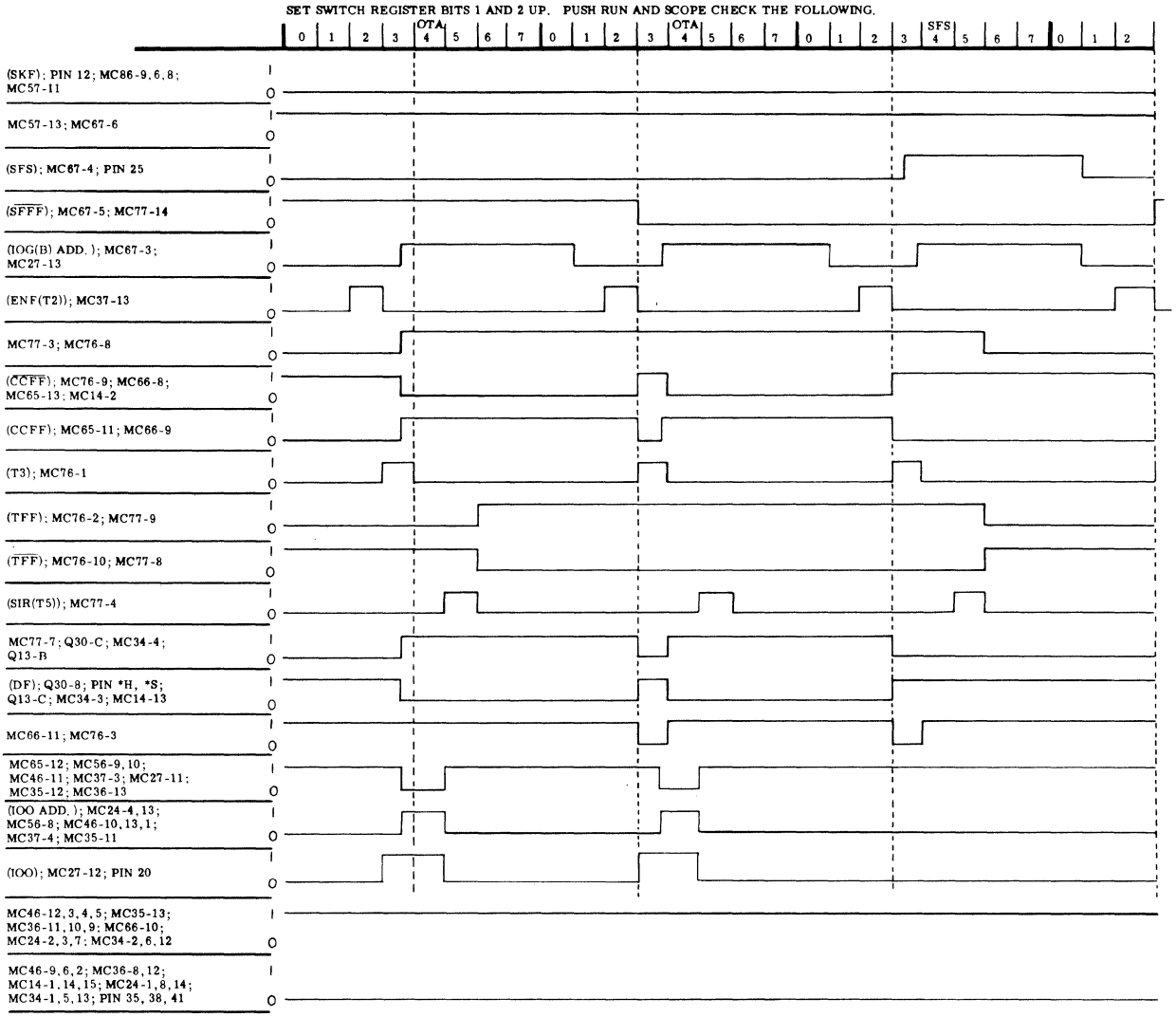


Figure 4-6. Timing Diagram for Error 1Ø.

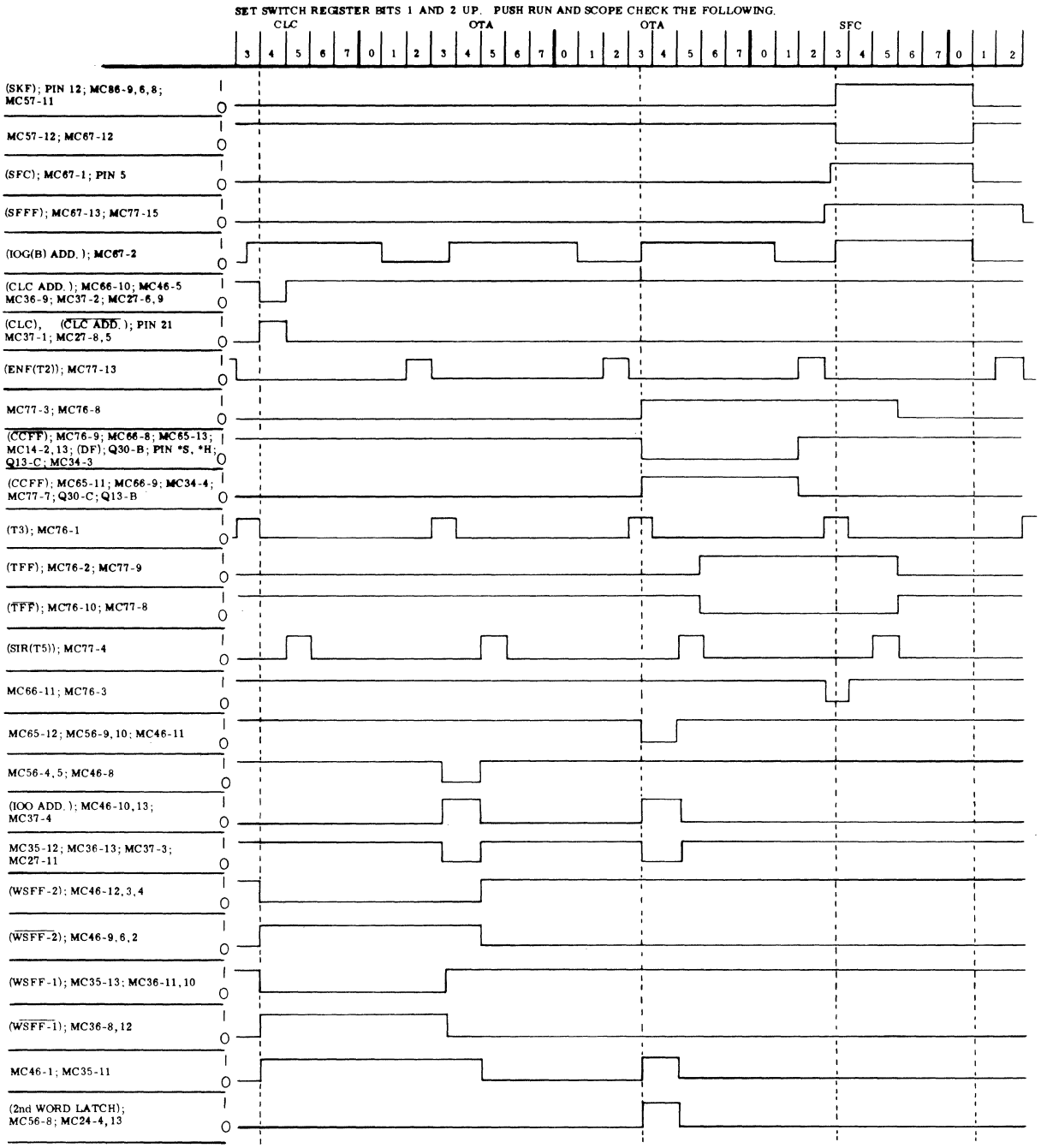


Figure 4-7. Timing Diagram for Error 12.

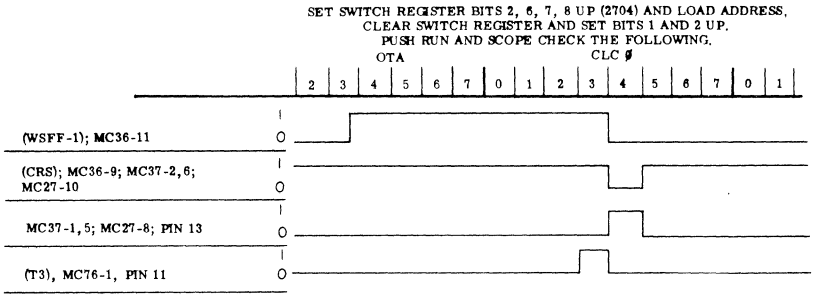


Figure 4-8. Timing Diagram for Error 14.

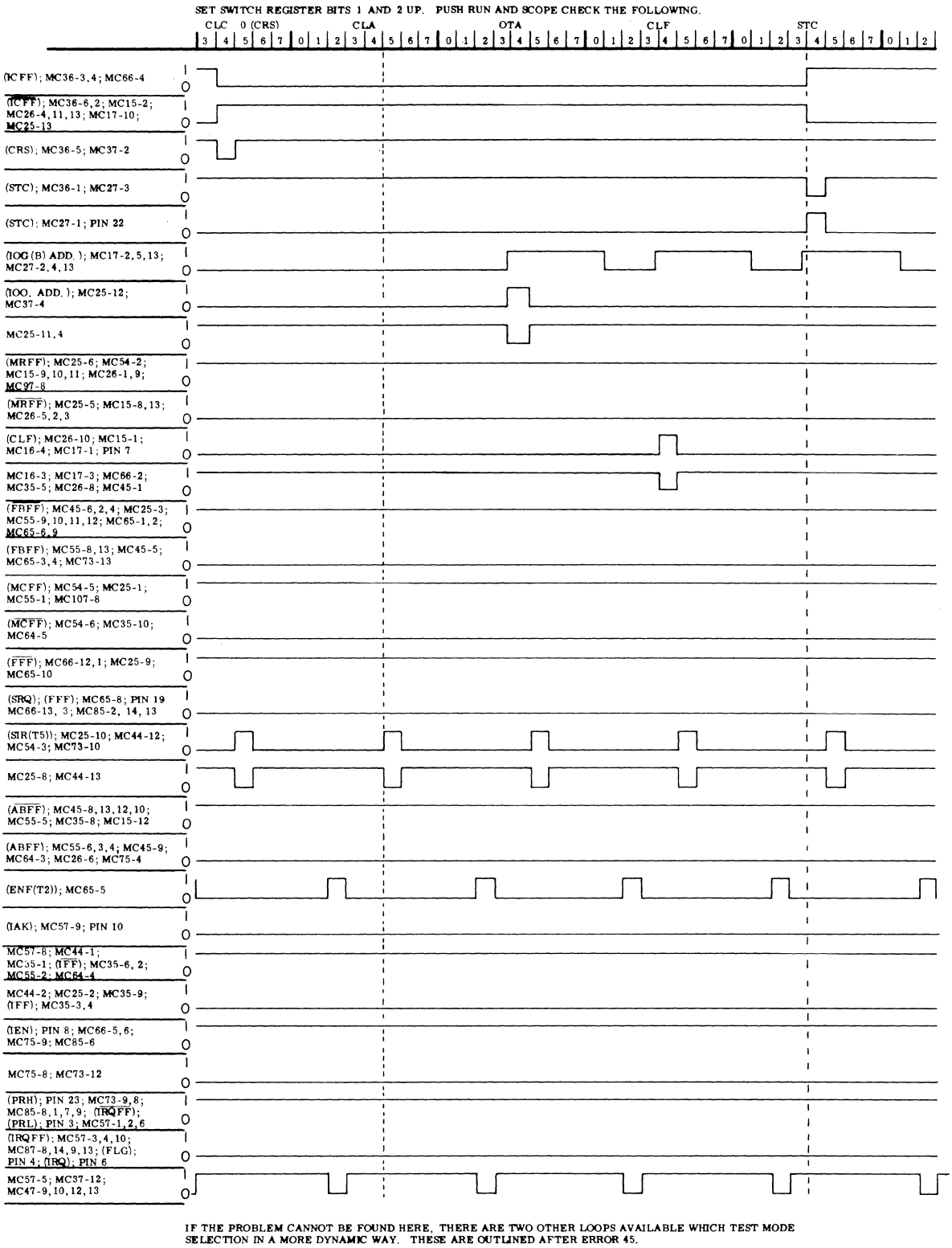


Figure 4-9. Timing Diagram for Error 16.

TIMING DIAGRAM 17

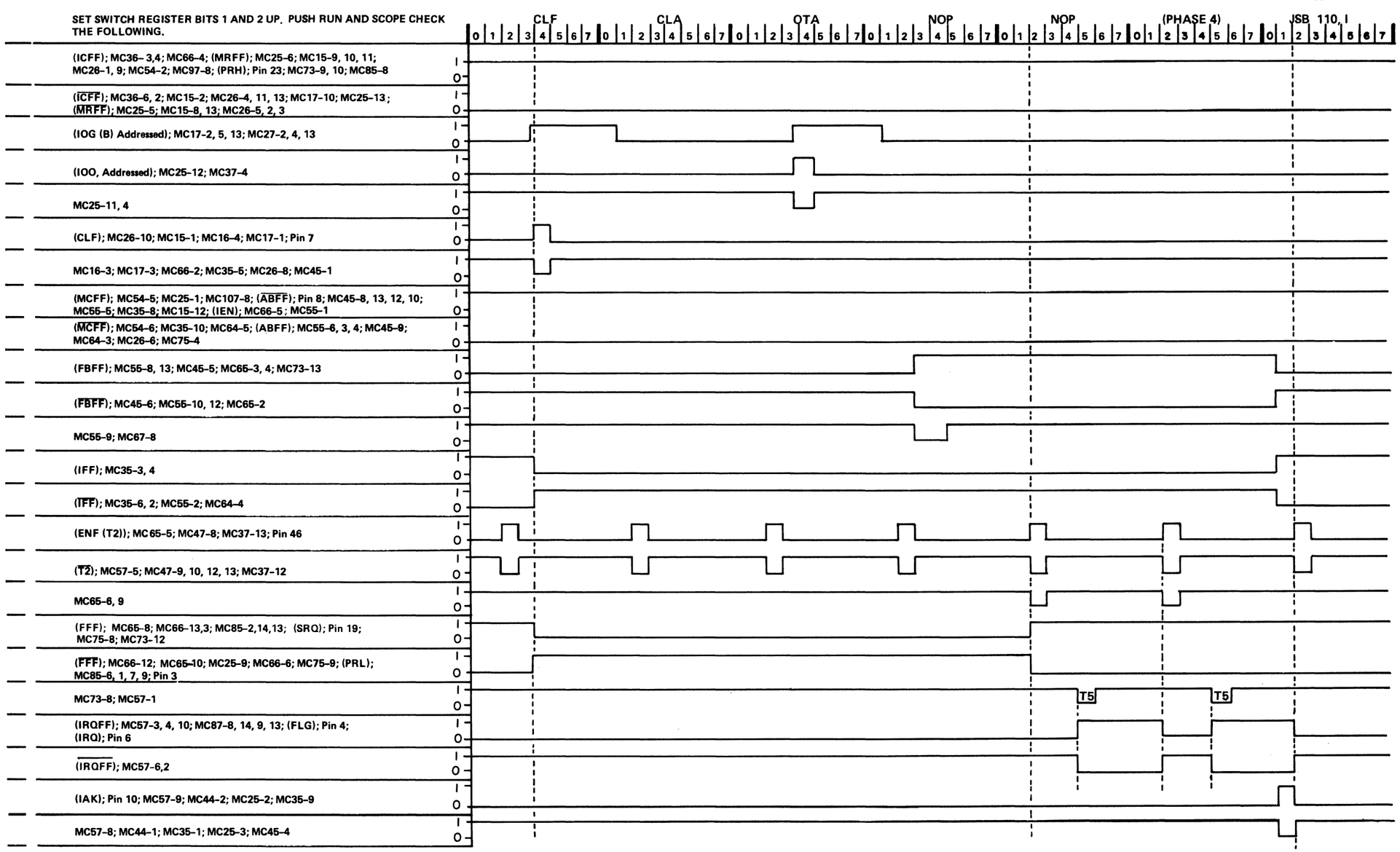


Figure 4-10. Timing Diagram for Error 17.

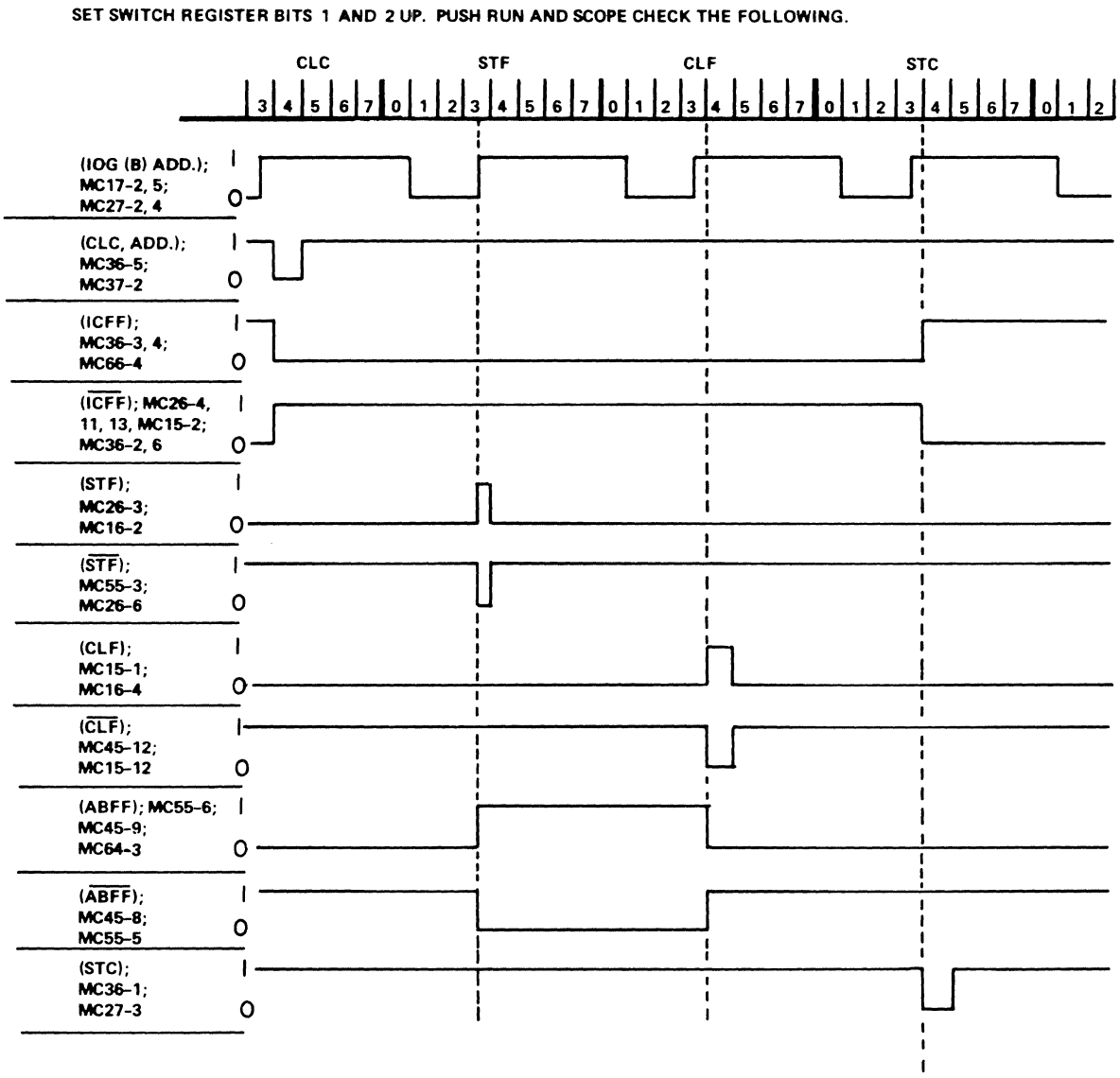
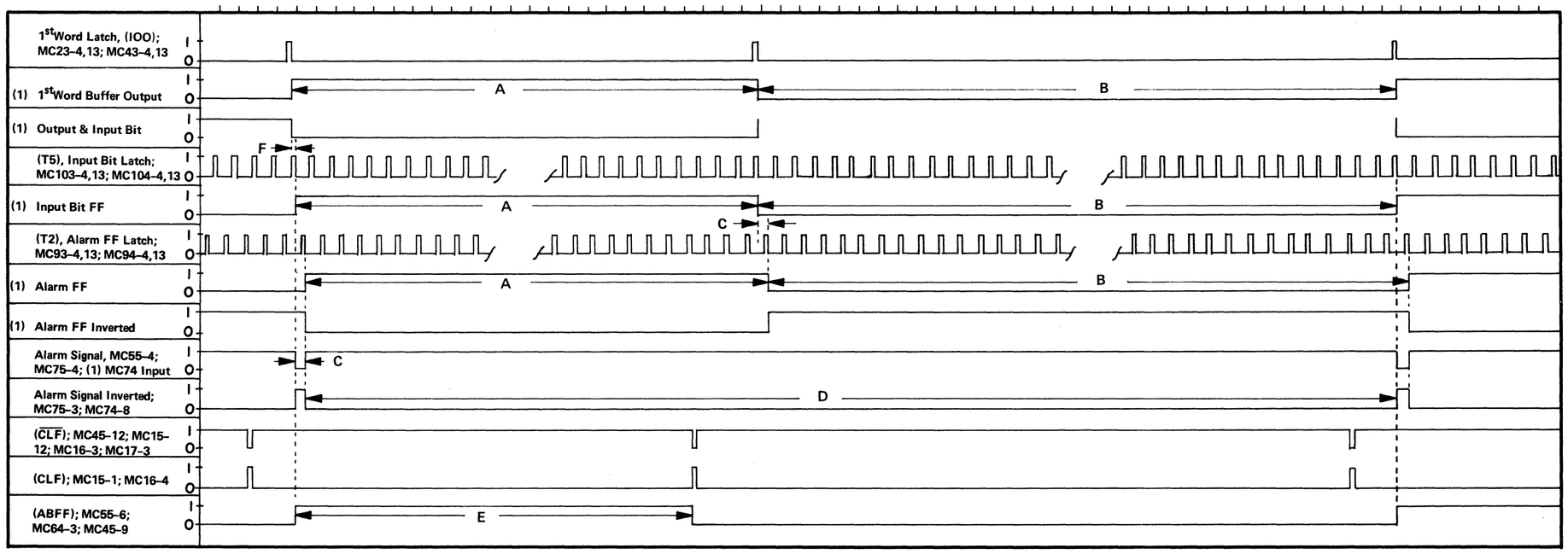


Figure 4-11. Timing Diagram for Error 34.

SET SWITCH REGISTER BITS 1 AND 2 UP AND PUSH RUN. THE ERROR MESSAGE SHOULD REPEAT.
PUSH RUN AGAIN AND SCOPE CHECK THE FOLLOWING.

THIS TEST MAY ALSO BE DONE BY SINGLE CYCLING THROUGH THE LOOP.
THERE ARE 57 CYCLES IN THE LOOP SO SINGLE CYCLING TAKES TIME.
REFER TO TABLES BELOW FOR PIN NUMBERS AND TIMING.
PIN NUMBERS WITH AN ASTRICK (*) ARE THE 48-PIN CONNECTOR.

TIMING DIAGRAMS
35 THROUGH 44



(1)	ERROR NUMBER							
	35	36	37	40	41	42	43	44
1st Word Buffer Output	BIT 0; MC23-8; Q7-B; Q31-C; MC103-2	BIT 1; MC23-14; Q10-B; Q32-C; MC103-3	BIT 2; MC23-1; Q8-B; Q33-C; MC103-6	BIT 3; MC43-8; Q17-B; Q34-C; MC103-7	BIT 4; MC43-11; Q18-B; Q38-C; MC104-2	BIT 5; MC43-14; Q20-B; Q37-C; MC104-3	BIT 6; MC43-1; Q19-B; Q36-C; MC104-6	BIT 7; MC23-11; Q9-B; Q35-C; MC104-7
Output and Input Bit	Q7-C; PIN * D; PIN * 16; Q31-B	Q10-C; PIN * 5; PIN * T; Q32-B	Q8-C; PIN * 4; PIN * 17; Q33-B	Q17-C; PIN * K; PIN * U; Q34-B	Q18-C; PIN * 9; PIN * W; Q38-B	Q20-C; PIN * 10; PIN * 19; Q37-B	Q19-C; PIN * L; PIN * V; Q36-B	Q9-C; PIN * E; PIN * 18; Q35-B
Input Bit Flip-Flop	MC103-16; MC93-2; MC83-12	MC103-15; MC93-3; MC83-2	MC103-10; MC93-6; MC83-9	MC103-9; MC93-7; MC83-4	MC104-16; MC94-2; MC84-12	MC104-15; MC94-3; MC84-2	MC104-10; MC94-6; MC84-9	MC104-9; MC94-7; MC84-4
Alarm Flip-Flop	MC93-16; MC106-8	MC93-15; MC106-14	MC93-10; MC96-8	MC93-9; MC96-14	MC94-16; MC95-8	MC94-15; MC95-14	MC94-10; MC105-8	MC94-9; MC105-14
Alarm FF Inverted	MC93-1; MC83-13	MC93-14; MC83-1	MC93-11; MC83-10	MC93-8; MC83-5	MC94-1; MC84-13	MC94-14; MC84-1	MC94-11; MC84-10	MC94-8; MC84-5
MC 74 Input	MC74-6; MC83-11; MC73-2	MC74-4; MC83-3; MC73-1	MC74-12; MC83-8; MC73-5	MC74-11; MC83-6; MC73-4	MC74-3; MC84-11	MC74-2; MC84-3	MC74-1; MC84-8	MC74-5; MC84-6

TIME PERIOD	NUMBER OF MACHINE CYCLES	TIME (μ SEC) FOR 2114 OR 2115 COMPUTERS	TIME (μ SEC) FOR 2116 COMPUTER
A	29	58.0	46.4
B	49	98.0	78.4
C	5/8	1.25	1.0
D	77 3/8	154.75	123.8
E	25 3/4	51.5	41.2
F	1/8	.250	.200

Figure 4-12. Timing Diagram for Errors 35 through 44.

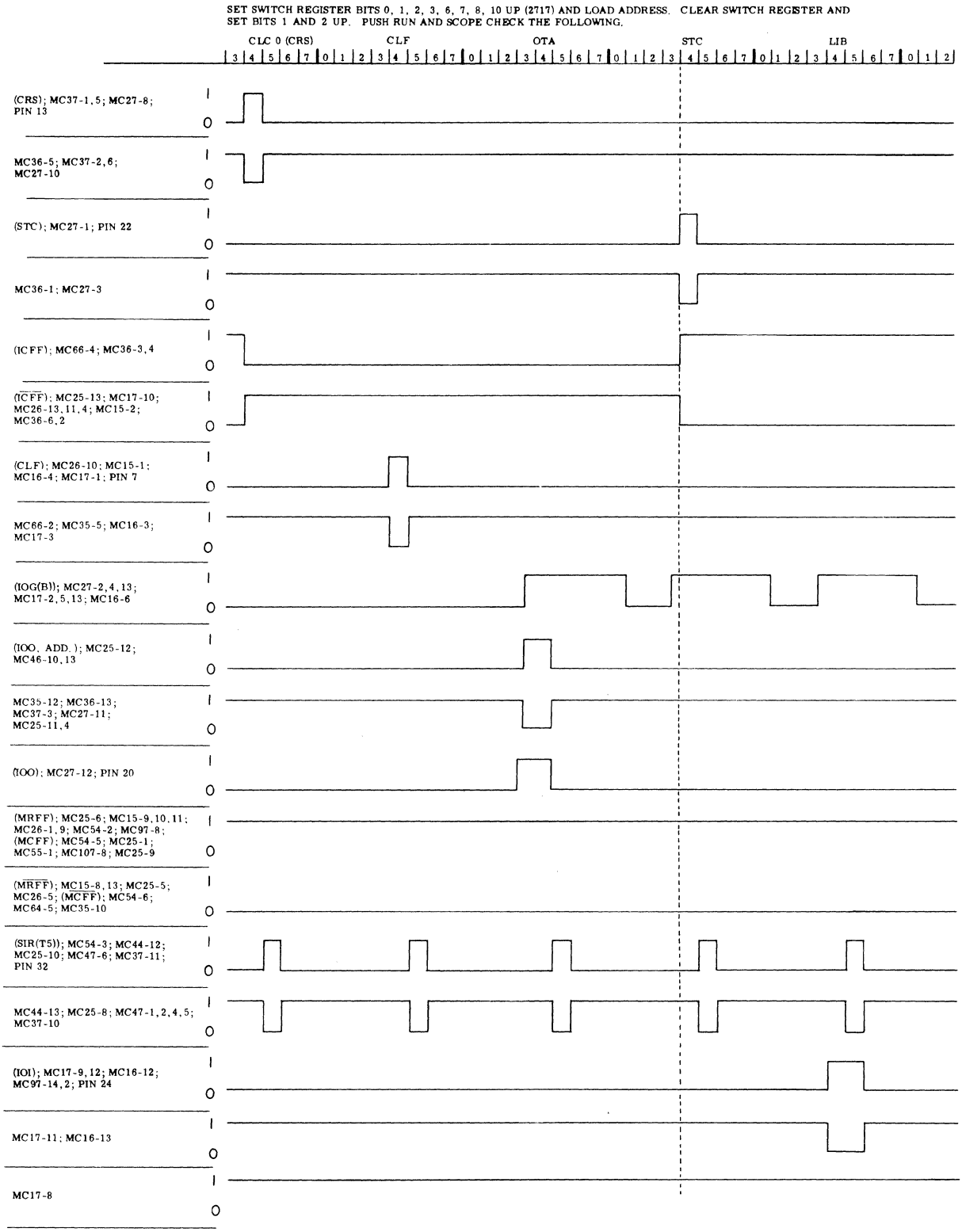


Figure 4-13. Set Control Timing Diagram

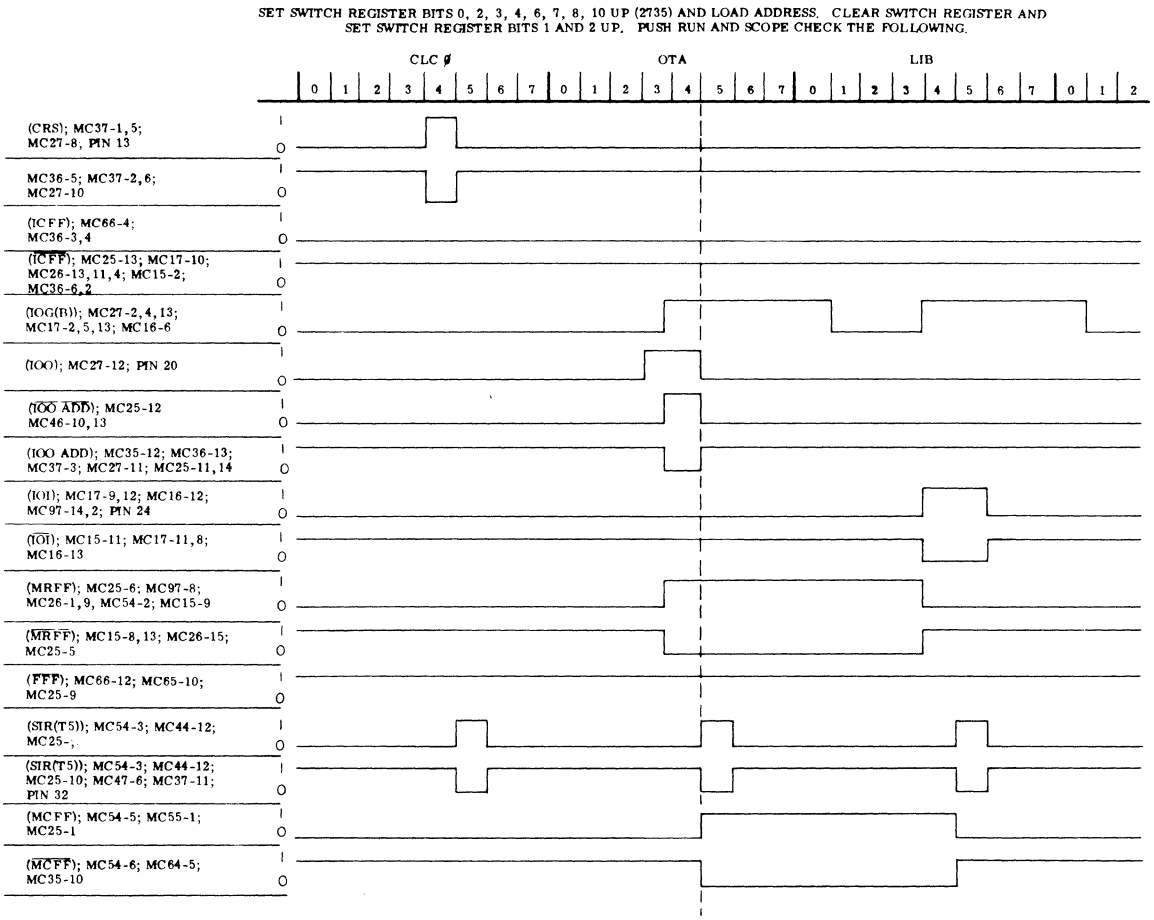


Figure 4-14. Mode Assignment Timing Diagram

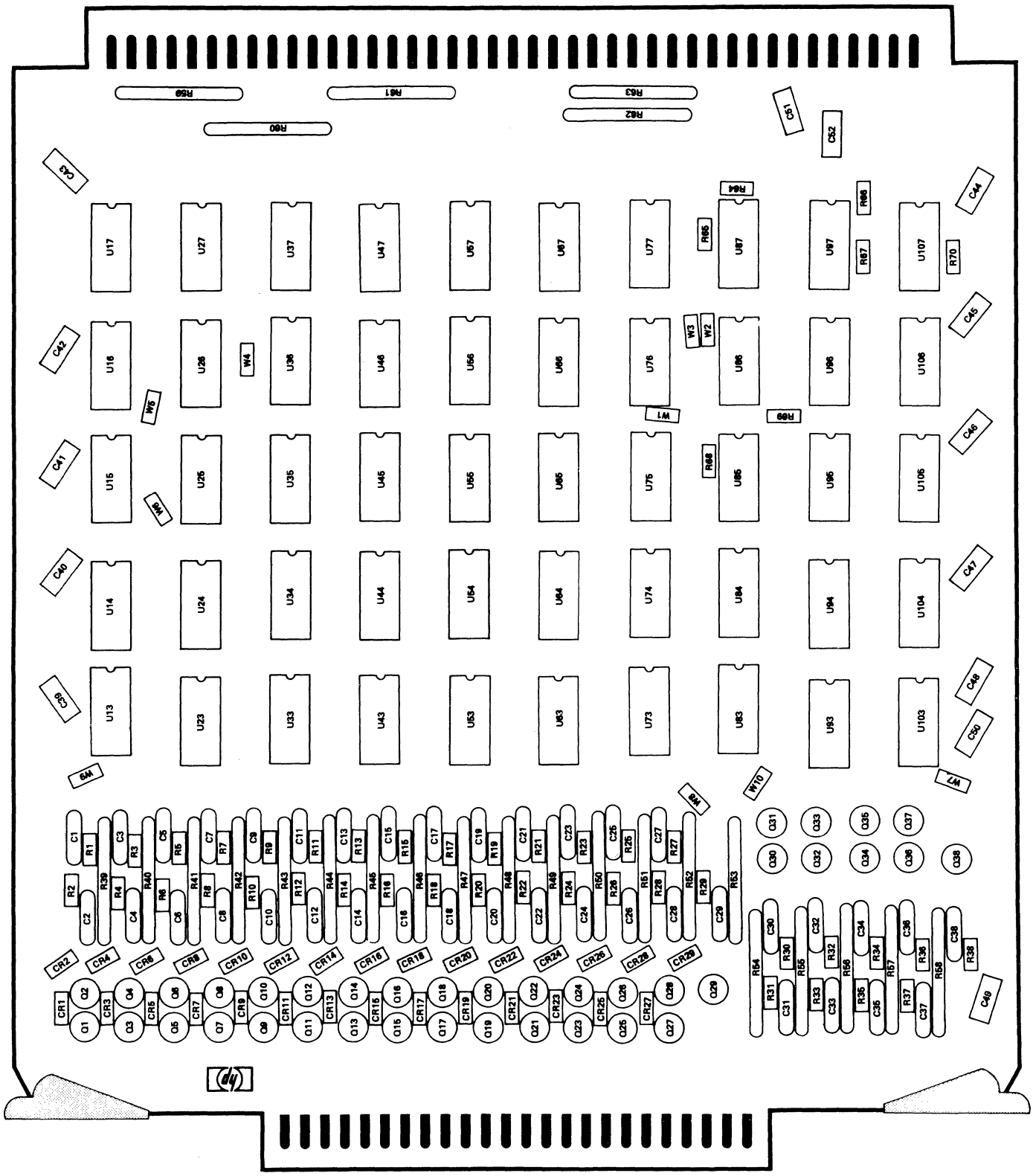


Figure 4-15. DVS Program Card, Parts Location

SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION

5-2. This section contains a list of information for ordering replacement parts. Table 5-1 lists parts alphanumerically by reference designation. It also provides:

a. HP part numbers.

b. A general description of the parts.

c. Typical manufacturer of the part expressed as a five-digit code (a list of manufacturers and their code numbers appears in Table 5-2).

d. Manufacturer's part, stock, or drawing number.

e. Total quantities used.

5-3. ORDERING INFORMATION

5-4. When ordering replacement parts, each part must be identified by the Hewlett-Packard part number. To order a part that is not listed in the tables, include the following information:

a. Instrument model number.

b. Instrument serial number.

c. Description of the part.

d. Function and location of the part.

5-5. Address your order or inquiry to your local Hewlett-Packard Sales and Service Office (listed at the rear of this manual).

5-6. If parts are ordered from the original manufacturer, a complete description should be included with each manufacturer's part number. Many numbers listed are type numbers only, and descriptions are needed to facilitate selection.

REFERENCE DESIGNATORS

A	assembly	F	fuse	P	plug	V	vacuum tube, neon bulb, photocell, etc.
B	motor	FL	Filter	Q	transistor		
BT	battery	J	jack	R	resistor	VR	voltage regulator
C	capacitor	K	relay	RT	thermistor	W	cable
CP	coupler	L	inductor	S	switch	X	socket
CR	diode	LS	loud speaker	T	transformer	Y	crystal
DL	delay line	M	meter	TB	terminal board	Z	tuned cavity, network
DS	device signaling	MK	microphone	TP	test point		
E	misc electronic part	MP	mechanical part	U	integrated circuit		

ABBREVIATIONS

A	amperes	H	henries	N/O	normally open	RMO	rack mount only
AFC	automatic frequency control	HDW	hardware	NOM	nominal	RMS	root-mean square
		HEX	hexagonal	NPO	negative positive zero (zero temperature coefficient)	RWV	reverse working voltage
AMPL	amplifier	HG	mercury			S-B	slow-blow
		HR	hour(s)			SCR	screw
BFO	beat frequency oscillator	Hz	Hertz	NPN	negative-positive-negative	SE	selenium
		IF	intermediate freq			SECT	section(s)
BE CU	beryllium copper	IMPG	impregnated	NRFR	not recommended for field replacement	SEMICON	semiconductor
BH	binder head	INCD	incandescent			SI	silicon
BP	bandpass	INCL	include(s)			SIL	silver
BRS	brass	INS	insulation(ed)	NSR	not separately replaceable	SL	slide
BWO	backward wave oscillator	INT	internal			SPG	spring
				OBD	order by description	SPL	special
CCW	counterclockwise	K	kilo = 1000			SST	Stainless steel
CER	ceramic			OH	oval head	SR	split ring
CMO	cabinet mount only			OX	oxide	STL	steel
COEF	coefficient	LH	left hand				
COM	common	LIN	linear taper	P	peak	TA	tantalum
COMP	composition	LK WASH	lock washer	PC	printed circuit	TD	time delay
COMPL	complete	LOG	logarithmic taper	PF	picofarads = 10^{-12} farads	TGL	toggle
CONN	connector	LPF	low pass filter			THD	thread
CP	cadmium plate			PH BRZ	phosphor bronze	TI	titanium
CRT	cathode-ray tube	M	milli = 10^{-3}	PHL	Phillips	TOL	tolerance
CW	clockwise	MEG	meg = 10^{6}	PIV	peak inverse voltage	TRIM	trimmer
		MET FLM	metal film			TWT	traveling wave tube
DEPC	deposited carbon	MET OX	metallic oxide	PNP	positive-negative-positive		
DR	drive	MFR	manufacturer				
		MHz	mega Hertz	P/O	part of	μ	micro = 10^{-6}
ELECT	electrolytic	MINAT	miniature	POLY	polystrene		
ENCAP	encapsulated	MOM	momentary	PORC	porcelain	VAR	variable
EXT	external	MOS	metalized substrate	POS	position(s)	VDCW	dc working volts
				POT	potentiometer		
F	farads	MTG	mounting	PP	peak-to-peak	W/	with
FH	flat head	MY	"mylar"	PT	point	W	watts
FIL H	Fillister head			PWV	peak working voltage	WIV	working inverse voltage
FXD	fixed	N	nano (10^{-9})				
		N/C	normally closed	RECT	rectifier	WW	wirewound
G	giga (10^{9})	NE	neon	RF	radio frequency	W/O	without
GE	germanium	NI PL	nickel plate	RH	round head or right hand		
GL	glass						
GRD	ground(ed)						

Table 5-2. Code List of Manufacturers

MFR. NO.	MANUFACTURER	ADDRESS
01121	Allen Bradley Co.	Milwaukee, Wis. 53204
01295	Texas Instruments Inc., Semiconductor Components Div.	Dallas, Texas 75231
04404	Hewlett-Packard Company, Automatic Measurement Div.	Palo Alto, Calif. 94306
04713	Motorola Semiconductor Prod. Inc.	Phoenix, Ariz. 85008
07263	Fairchild Camera & Inst. Corp., Semiconductor Div.	Mountain View, Calif. 94040
12040	National Semiconductor	Danbury, Conn. 06810
28480	Hewlett-Packard Company	Palo Alto, Calif. 94304
56289	Sprague Electric Co.	N. Adams, Mass. 01247

APPENDIX A

LISTING
FOR
HP 20436 DIAGNOSTIC PROGRAM
FOR THE
MODEL 12661A
DIGITAL VOLTAGE SOURCE PROGRAMMER
INTERFACE KIT

```
 PAGE 0001

0001                    ASMB,A,L,C
**  NO ERRORS*
```

PAGE 0002 #01

```
0001*
0002*12661A DVS PROGRAM CARD DIAGNOSTIC
0003*
0004*MARCH 14, 1969
0005*
0006*STARTING OCTAL ADDRESS = 100
0007*
0008*THE FOLLOWING SWITCH REGISTER SETTINGS
0009*   ARE USED FOR PROGRAM CONTROL
0010*
0011**BIT 0 = 1 -> HALT AT BEGINNING OF PROGRAM
0012*BIT 1 = 1 -> HALT AT THIS PT. IN PROGRAM
0013*BIT 2 = 1 -> LOOP FOR SCOPE TEST
0014*BIT 3 = 1 -> SKIP INITIAL TURN-ON TEST
0015*BIT 4 = 1 -> LOOP ENTIRE BASIC TEST
0016*
0017*
0018*MAIN PROGRAM
0019*
0020  00100                 ORG 100B        ORIGIN OF ABSOLUTE PROGRAM
0021  00100 124115          JMP 115B,I      MAIN PROGRAM LINKAGE
0022  00105                 ORG 105B
0023  00105 004006           DEF X           FIRST AVAIL MEMORY AFTER PROGRA
0024  00110                 ORG 110B        DEFINES INTERRUPT LINKAGE
0025  00110 003306          DEF ERROR       ILLEGAL INTERRUPT
0026  00111 003440          DEF INTR        LEGAL INTERRUPT
0027  00115                 ORG 115B        MAIN PROGRAM LINKAGE
0028  00115 002000          DEF PAGE2       DEFINES STARTING PT.
0029  02000                 ORG 2000B       PROGRAM STARTING PT.
0030  02000 107700  PAGE2 CLC 0,C          INTERRUPT SYSTEM OFF
0031  02001 016417          JSB EOL         LINE FEED
0032  02002 062164          LDA ML1         PRINT 1ST MESSAGE
0033  02003 066146          LDB MAD1          12661A VERIFICATION
0034  02004 114102          JSB 102B,I          PROGRAM - TTY
0035  02005 016417          JSB EOL         LINE FEED
0036  02006 026013          JMP *+5
0037  02007 062012  P1      LDA *+3         HALT AT BEGINNING
0038  02010 066012          LDB *+2            OF PROGRAM
0039  02011 107700          CLC 0,C
0040  02012 102000          HLT 0           102000
0041  02013 066403          LDB M67         PREPARE
0042  02014 062404          LDA HIS           TRAP
0043  02015 072017          STA *+2             FOR
0044  02016 062405          LDA HI                ILLEGAL
0045  02017 070010          STA 10B                 INTERRUPT
0046  02020 036017          ISZ *-1                   FROM
0047  02021 002004          INA                         ANY
0048  02022 006006          INB,SZB                       DEVICE
0049  02023 026017          JMP *-4
0050  02024 016417  P2      JSB EOL         LINE FEED
0051  02025 062174          LDA ML2         PRINT
0052  02026 066165          LDB MAD2          I/O CHANNEL?
0053  02027 114102          JSB 102B,I      TTY LINKAGE
0054  02030 016417          JSB EOL
0055  02031 062410          LDA RL1         RECEIVE
0056  02032 066406          LDB RAD1          REPLY
0057  02033 114104          JSB 104B,I      TTY LINKAGE KEYBOARD
```

PAGE 0003 #01

```
0058  02034 016417          JSB EOL       LINE FEED
0059  02035 062407          LDA REP1      CHECK FIRST CHARACTER
0060  02036 012411          AND MSK1        FOR VALIDITY
0061  02037 052414          CPA C1        VALID?
0062  02040 026042          JMP *+2       YES.
0063  02041 026024          JMP P2        NO.
0064  02042 062407          LDA REP1      CHECK
0065  02043 001727          ALF,ALF         SECOND
0066  02044 012411          AND MSK1          CHARACTER
0067  02045 052414          CPA C1        VALID?
0068  02046 026050          JMP *+2       YES.
0069  02047 026024          JMP P2        NO.
0070  02050 062407          LDA REP1      GENERATE
0071  02051 012412          AND MSK2        DIGITAL
0072  02052 072615          STA ADDR          VOLTAGE
0073  02053 062407          LDA REP1            SOURCE
0074  02054 001727          ALF,ALF               INTERFACE
0075  02055 012412          AND MSK2                ADDRESS
0076  02056 001721          ALF,ARS
0077  02057 032615          IOR ADDR
0078  02060 072615          STA ADDR      ADDRESS COMPLETE
0079  02061 016437          JSB ADIN      ADDRESS INCLUSION ROUTINE
0080  02062 062216          LDA ML3       PRINT MESSAGE -
0081  02063 066175          LDB MAD3        CONNECT PLUG
0082  02064 114102          JSB 102B,I        NO.1 AND PUSH RUN
0083  02065 016417          JSB EOL       LINE FEED
0084  02066 102000          HLT 0         HALT
0085*
0086  02067 017164          JSB MODE      SWITCH REGISTER STORAGE
0087  02070 063210          LDA BIT3
0088  02071 000010          SLA           SKIP INITIAL TEST?
0089  02072 026127          JMP P3        YES.
0090  02073 016616          JSB ITEST     INITIAL TEST PLUG NO. 1
0091  02074 062264          LDA ML5       PRINT MESSAGE -
0092  02075 066243          LDB MAD5        CONNECT PLUG
0093  02076 114102          JSB 102B,I        NO.2 AND PUSH RUN
0094  02077 016417          JSB EOL       LINE FEED
0095  02100 102000          HLT 0
0096  02101 016616          JSB ITEST     INITIAL TEST PLUG NO. 2
0097  02102 062306          LDA ML6       PRINT MESSAGE -
0098  02103 066265          LDB MAD6        CONNECT PLUG
0099  02104 114102          JSB 102B,I        NO.3 AND PUSH RUN
0100  02105 016417          JSB EOL       LINE FEED
0101  02106 102000          HLT 0
0102  02107 106500  LIB1    LIB 0         INITIAL TEST PLUG NO. 3
0103  02110 062416          LDA C3        COMPARISON IN A
0104  02111 050001          CPA 1         IS INPUT CORRECT?
0105  02112 026114          JMP *+2       YES.
0106  02113 017340          JSB DAT       NO. PRINTOUT ROUTINE
0107  02114 062330          LDA ML7       PRINT MESSAGE -
0108  02115 066307          LDB MAD7        CONNECT PLUG
0109  02116 114102          JSB 102B,I        NO.4 AND PUSH RUN
0110  02117 016417          JSB EOL       LINE FEED
0111  02120 102000          HLT 0
0112  02121 016616          JSB ITEST     INITIAL TEST PLUG NO. 4
0113  02122 062216          LDA ML3       PRINT MESSAGE -
0114  02123 066175          LDB MAD3        CONNECT PLUG
```

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```
0115  02124 114102        JSB 102B,I        NO.1 AND PUSH RUN
0116  02125 016417        JSB EOL       LINE FEED
0117  02126 102000        HLT 0
0118*
0119  02127 016625  P3    JSB BAT       PERFORM BASIC TEST
0120  02130 017164        JSB MODE      SW REG STORAGE
0121  02131 063211        LDA BIT4
0122  02132 000010        SLA           LOOP?
0123  02133 026127        JMP P3
0124  02134 063206        LDA BIT1
0125  02135 000010        SLA           HALT?
0126  02136 102000        HLT 0
0127  02137 017533        JSB DOIC      PERFORM DATA BUFFER TEST
0128  02140 062346        LDA ML8       PRINT MESSAGE -
0129  02141 066331        LDB MAD8        END OF DATA
0130  02142 114102        JSB 102B,I        BUFFER TEST
0131  02143 016417        JSB EOL
0132  02144 102000        HLT 0
0133  02145 026007        JMP P1        JUMP TO BEGINNING
0134*
0135  02146 002147  MAD1  DEF *+1        1ST MESSAGE
0136  02147 030462  MES1  ASC 13,12661A DIAGNOSTIC PROGRAM
      02150 033066
      02151 030501
      02152 020104
      02153 044501
      02154 043516
      02155 047523
      02156 052111
      02157 041440
      02160 050122
      02161 047507
      02162 051101
      02163 046440
0137  02164 000034  ML1   DEC 28
0138*
0139  02165 002166  MAD2  DEF *+1        2ND MESSAGE
0140  02166 044457  MES2  ASC 6,I/O CHANNEL?
      02167 047440
      02170 041510
      02171 040516
      02172 047105
      02173 046077
0141  02174 000014  ML2   DEC 12
0142*
0143  02175 002176  MAD3  DEF *+1
0144  02176 041517  MES3  ASC 16,CONNECT PLUG N0. 1 AND PUSH RUN
      02177 047116
      02200 042503
      02201 052040
      02202 050114
      02203 052507
      02204 020116
      02205 030056
      02206 020061
      02207 020101
      02210 047104
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```
      02211 020120
      02212 052523
      02213 044040
      02214 051125
      02215 047040
0145  02216 000040  ML3   DEC 32
0146*
0147  02217 002220  MAD4  DEF *+1
0148  02220 042101  MES4  ASC 18,DATA BUFFER TEST PLUG NO. 1 PUSH RUN
      02221 052101
      02222 020102
      02223 052506
      02224 043105
      02225 051040
      02226 052105
      02227 051524
      02230 020120
      02231 046125
      02232 043440
      02233 047117
      02234 027040
      02235 030440
      02236 050125
      02237 051510
      02240 020122
      02241 052516
0149  02242 000044  ML4   DEC 36
0150*
0151  02243 002244  MAD5  DEF *+1
0152  02244 041517  MES5  ASC 16,CONNECT PLUG NO. 2 AND PUSH RUN
      02245 047116
      02246 042503
      02247 052040
      02250 050114
      02251 052507
      02252 020116
      02253 047456
      02254 020062
      02255 020101
      02256 047104
      02257 020120
      02260 052523
      02261 044040
      02262 051125
      02263 047040
0153  02264 000040  ML5   DEC 32
0154*
0155  02265 002266  MAD6  DEF *+1
0156  02266 041517  MES6  ASC 16,CONNECT PLUG NO. 3 AND PUSH RUN
      02267 047116
      02270 042503
      02271 052040
      02272 050114
      02273 052507
      02274 020116
      02275 047456
      02276 020063
```

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      02277 020101
      02300 047104
      02301 020120
      02302 052523
      02303 044040
      02304 051125
      02305 047040
0157  02306 000040  ML6   DEC 32
0158*
0159  02307 002310  MAD7  DEF *+1
0160  02310 041517  MES7  ASC 16,CONNECT PLUG NO. 4 AND PUSH RUN
      02311 047116
      02312 042503
      02313 052040
      02314 050114
      02315 052507
      02316 020116
      02317 047456
      02320 020064
      02321 020101
      02322 047104
      02323 020120
      02324 052523
      02325 044040
      02326 051125
      02327 047040
0161  02330 000040  ML7   DEC 32
0162*
0163  02331 002332  MAD8  DEF *+1
0164  02332 042516  MES8  ASC 12,END OF DATA BUFFER TEST
      02333 042040
      02334 047506
      02335 020104
      02336 040524
      02337 040440
      02340 041125
      02341 043106
      02342 042522
      02343 020124
      02344 042523
      02345 052040
0165  02346 000030  ML8   DEC 24
0166*
0167  02347 002350  MAD9  DEF *+1
0168  02350 042522  MES9  ASC 6,ERROR
      02351 051117
      02352 051040
      02353 020040
      02354 020040
      02355 020040
0169  02356 000014  ML9   DEC 12
0170*
0171  02357 002360  MAD10 DEF *+1
0172  02360 047525  MES10 ASC 18,OUTPUT =            INPUT  =
      02361 052120
      02362 052524
      02363 020075
```

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      02364 020040
      02365 020040
      02366 020040
      02367 020040
      02370 020040
      02371 020040
      02372 044516
      02373 050125
      02374 052040
      02375 020075
      02376 020040
      02377 020040
      02400 020040
      02401 020040
0173  02402 000044  ML10  DEC 36
0174*
0175  02403 177711  M67   OCT 177711
0176  02404 070010  HIS   STA 10B
0177  02405 102010  HI    HLT 10B
0178  02406 002407  RAD1  DEF *+1
0179  02407 000000  REP1  OCT 0
0180  02410 000002  RL1   OCT 2
0181  02411 000170  MSK1  OCT 170
0182  02412 000007  MSK2  OCT 7
0183  02413 000017  MSK3  OCT 17
0184  02414 000060  C1    OCT 60
0185  02415 040000  C2    OCT 40000     COMPARISON STORAGE 1,2,4
0186  02416 040020  C3    OCT 40020     COMPARISON STORAGE 3
0187*
0188*LINE FEED, CARRIAGE RETURN
0189*
0190  02417 000000  EOL   NOP           ENTER SUBROUTINE
0191  02420 072430        STA AS1       STORE
0192  02421 076435        STB BS1         A & B
0193  02422 002400        CLA           LINE
0194  02423 006400        CLB             FEED
0195  02424 114102        JSB 102B,I    TTY
0196  02425 062430        LDA AS1       RESTORE
0197  02426 066435        LDB BS1         A & B
0198  02427 126417        JMP EOL,I     EXIT SUBROUTINE
0199  02430 000000  AS1   OCT 0
0200  02431 000000  AS2   OCT 0
0201  02432 000000  AS3   OCT 0
0202  02433 000000  AS4   OCT 0
0203  02434 000000  AS5   OCT 0
0204  02435 000000  BS1   OCT 0
0205  02436 000000  BS2   OCT 0
0206*
0207*ADDRESS INCLUSION ROUTINE
0208*
0209  02437 000000  ADIN  NOP           ENTER ROUTINE
0210  02440 107700        CLC 0,C       INTERRUPT SYSTEM OFF
0211  02441 016610        JSB INCLU     PUT DUPLEX REG ADDR
0212  02442 070000        STA 0           INTO STA INSTRUCTIONS
0213  02443 073427        STA STA1
0214  02444 073435        STA STA2
0215  02445 016610        JSB INCLU     ADDRESS IN STC XX
```

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```
0216  02446 102700          STC 0          DATA
0217  02447 072724          STA STC1
0218  02450 072757          STA STC2
0219  02451 073100          STA STC3
0220  02452 073111          STA STC4
0221  02453 073124          STA STC5
0222  02454 073464          STA STC6
0223  02455 073476          STA STC7
0224  02456 073520          STA STC8
0225  02457 073575          STA STC9
0226  02460 073644          STA STC10
0227  02461 073722          STA STC11
0228  02462 016610          JSB INCLU      ADDRESS IN SFS XX
0229  02463 102300          SFS 0          DATA
0230  02464 072645          STA SFS1
0231  02465 072702          STA SFS2
0232  02466 073214          STA SFS3
0233  02467 073244          STA SFS4
0234  02470 016610          JSB INCLU      ADDRESS IN SFC XX
0235  02471 102200          SFC 0
0236  02472 072660          STA SFC1
0237  02473 072670          STA SFC2
0238  02474 073226          STA SFC3
0239  02475 073257          STA SFC4
0240  02476 016610          JSB INCLU      ADDRESS IN STF XX
0241  02477 102100          STF 0
0242  02500 073455          STA STF1
0243  02501 073461          STA STF2
0244  02502 073475          STA STF3
0245  02503 073516          STA STF4
0246  02504 016610          JSB INCLU      ADDRESS IN CLF XX
0247  02505 103100          CLF 0          DATA
0248  02506 072722          STA CLF1
0249  02507 072756          STA CLF2
0250  02510 072772          STA CLF3
0251  02511 073025          STA CLF4
0252  02512 073044          STA CLF5
0253  02513 073451          STA CLF6
0254  02514 073504          STA CLF7
0255  02515 073517          STA CLF8
0256  02516 016610          JSB INCLU      ADDRESS IN CLC XX
0257  02517 106700          CLC 0          DATA
0258  02520 072630          STA CLC1
0259  02521 072637          STA CLC2
0260  02522 072665          STA CLC3
0261  02523 073450          STA CLC4
0262  02524 073474          STA CLC5
0263  02525 073573          STA CLC6
0264  02526 073641          STA CLC7
0265  02527 000000          NOP
0266  02530 073515          STA CLC9
0267  02531 073717          STA CLC10
0268  02532 016610          JSB INCLU      ADDRESS IN CLC XX,C
0269  02533 107700          CLC 0,C        DATA
0270  02534 073110          STA CLCF1
0271  02535 073123          STA CLCF2
0272  02536 016610          JSB INCLU      ADDRESS IN OTA XX
```

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```
0273  02537 102600          OTA 0
0274  02540 072632          STA OTA1
0275  02541 072635          STA OTA2
0276  02542 072643          STA OTA3
0277  02543 072644          STA OTA4
0278  02544 072666          STA OTA5
0279  02545 072667          STA OTA6
0280  02546 072705          STA OTA7
0281  02547 072723          STA OTA8
0282  02550 072737          STA OTA9
0283  02551 072755          STA OTA10
0284  02552 072774          STA OTA11
0285  02553 073016          STA OTA12
0286  02554 073046          STA OTA13
0287  02555 073162          STA FLAG
0288  02556 016610          JSB INCLU      ADDRESS IN OTB XX
0289  02557 106600          OTB 0          DATA
0290  02560 073076          STA OTB1
0291  02561 073112          STA OTB2
0292  02562 073126          STA OTB3
0293  02563 073574          STA OTB4
0294  02564 073642          STA OTB5
0295  02565 073643          STA OTB6
0296  02566 073720          STA OTB7
0297  02567 073721          STA OTB8
0298  02570 073761          STA OTB9
0299  02571 073762          STA OTB10
0300  02572 016610          JSB INCLU      ADDRESS IN LIB XX
0301  02573 106500          LIB 0          DATA
0302  02574 072107          STA LIB1
0303  02575 072617          STA LIB2
0304  02576 072725          STA LIB3
0305  02577 072740          STA LIB4
0306  02600 073077          STA LIB5
0307  02601 016610          JSB INCLU      ADDRESS IN LIA XX
0308  02602 102500          LIA 0
0309  02603 073577          STA LIA1
0310  02604 073646          STA LIA2
0311  02605 073724          STA LIA3
0312  02606 073163          STA ALRM
0313  02607 126437          JMP ADIN,I
0314*
0315*INCLUSION SUBROUTINE
0316*
0317  02610 000000  INCLU NOP          ENTER SUBROUTINE
0318  02611 162610        LDA INCLU,I  LOAD I/O INSTRUCTION 0
0319  02612 032615        IOR ADDR       ADD TO IT SC ADDRESS
0320  02613 036610        ISZ INCLU    INCREMENT PROGRAM
0321  02614 126610        JMP INCLU,I  EXIT SUBROUTINE
0322  02615 000000  ADDR  OCT 0        ADDRESS STORAGE
0323*
0324*INITIAL TEST
0325*
0326  02616 000000  ITEST NOP          ENTER SUBROUTINE
0327  02617 106500  LIB2  LIB 0        READ DATA IN
0328  02620 062415        LDA C2       PLACE COMPARISON IN A
0329  02621 050001        CPA 1        IS INPUT CORRECT?
```

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```
0330  02622 126616          JMP ITEST,I   YES. EXIT
0331  02623 017340          JSB DAT       NO. PRINTOUT ROUTINE
0332  02624 126616          JMP ITEST,I   EXIT SUBROUTINE
0333*
0334*BASIC TEST ROUTINE
0335*
0336  02625 000000  BAT   NOP             BASIC TEST ROUTINE
0337  02626 067305        LDB ERR2        INITIALIZE
0338  02627 077304        STB ERR1          ERROR NUMBER
0339  02630 106700  CLC1  CLC 0           DISABLE INTERRUPT
0340  02631 017212        JSB STAF1       PERFORM STATUS FLAG ROUTINE
0341  02632 102600  OTA1  OTA 0           ADDRESS DVSI 0 WITH 1ST WORD
0342  02633 017212        JSB STAF1       FLAG ROUTINE 1ST WORD
0343  02634 003000        CMA
0344  02635 102600  OTA2  OTA 0           2ND WORD WRONG ADDRESS TO DVSI
0345  02636 017242        JSB STAF2       FLAG ROUTINE 2ND WORD
0346  02637 106700  CLC2  CLC 0           CLEAR WSFF
0347  02640 017212        JSB STAF1       FLAG ROUTINE TO CHECK CLC
0348  02641 017272        JSB ERAD        INCREMENT ERROR MESSAGE
0349*
0350*ADDRESS PSI 2ND WORD SFS CHK
0351  02642 002400  EN1   CLA
0352  02643 102600  OTA3  OTA 0           ADDRESS DVSI
0353  02644 102600  OTA4  OTA 0             WITH 2ND WORD
0354  02645 102300  SFS1  SFS 0           IS STATUS FLAG CLEAR?
0355  02646 026650        JMP *+2         NO.
0356  02647 017306        JSB ERROR       YES. SFS-SKIP-FLAG TEMP SET
0357  02650 017164        JSB MODE        STORE SWITCH REGISTER
0358  02651 063207        LDA BIT2
0359  02652 000010        SLA             LOOP?
0360  02653 026642        JMP EN1         YES.
0361  02654 063206        LDA BIT1        NO.
0362  02655 000010        SLA             HALT?
0363  02656 102000        HLT 0           YES.
0364  02657 017272        JSB ERAD        NO. INCREMENT ERROR MESSAGE
0365  02660 102200  SFC1  SFC 0           IS STATUS FLAG SET?
0366  02661 026663        JMP *+2         NO.
0367  02662 017306        JSB ERROR       YES. SFC-SKIP-FLAG CLEAR-ERROR
0368*
0369*ADDRESS PSI 2ND WORD SFC CHK
0370  02663 017272        JSB ERAD        INCREMENT ERROR MESSAGE
0371  02664 002400  EN2   CLA
0372  02665 106700  CLC3  CLC 0
0373  02666 102600  OTA5  OTA 0           ADDRESS DVSI
0374  02667 102600  OTA6  OTA 0             WITH 2ND WORD
0375  02670 102200  SFC2  SFC 0           IS STATUS FLAG SET?
0376  02671 017306        JSB ERROR       NO. SFC-NO SKIP-FLAG TEMP SET
0377  02672 017164        JSB MODE        YES.
0378  02673 063207        LDA BIT2
0379  02674 000010        SLA             LOOP?
0380  02675 026664        JMP EN2         YES.
0381  02676 063206        LDA BIT1        NO.
0382  02677 000010        SLA             HALT?
0383  02700 102000        HLT 0           YES.
0384  02701 017272        JSB ERAD        NO. INCREMENT ERROR
0385  02702 102300  SFS2  SFS 0           IS STATUS FLAG CLEAR?
0386  02703 017306        JSB ERROR       NO. SFS-NO SKIP-FLAG CLEAR-ERROR
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0387*
0388*CHECK CRS COMMAND
0389  02704 002400  EN3    CLA
0390  02705 102600  OTA7   OTA 0
0391  02706 106700         CLC 0
0392  02707 017164         JSB MODE       STORE SWITCH REGISTER
0393  02710 063207         LDA BIT2
0394  02711 000010         SLA            LOOP?
0395  02712 026704         JMP EN3        YES.
0396  02713 063206         LDA BIT1       NO.
0397  02714 000010         SLA            HALT?
0398  02715 102000         HLT 0          YES.
0399  02716 017212         JSB STAF1      NO. STATUS FLAG ROUTINE
0400*
0401*CHECK FLAG MODE ASSIGNMENT
0402  02717 002400  P4     CLA
0403  02720 017164         JSB MODE       STORE SWITCH REGISTER
0404  02721 106700         CLC 0          ENABLE ASSIGNMENT
0405  02722 103100  CLF1   CLF 0          INITIALIZES INTERLOCK
0406  02723 102600  OTA8   OTA 0          ASSIGN FLAG INTERRUPT
0407  02724 102700  STC1   STC 0          DISABLE ASSIGNMENT
0408  02725 106500  LIB3   LIB 0          TEST ICFF WITH ALARM ASSIGN
0409  02726 017164         JSB MODE       STORE SWITCH REGISTER
0410  02727 063207         LDA BIT2
0411  02730 000010         SLA            LOOP?
0412  02731 026717         JMP P4         YES.
0413  02732 063206         LDA BIT1       NO.
0414  02733 000010         SLA            HALT?
0415  02734 102000         HLT 0
0416*
0417*CHECK ALARM MODE ASSIGNMENT
0418  02735 002400  P5     CLA
0419  02736 106700         CLC 0          ENABLE ASSIGNMENT
0420  02737 102600  OTA9   OTA 0
0421  02740 106500  LIB4   LIB 0          ASSIGN ALARM INTERRUPT
0422  02741 017164         JSB MODE       STORE SWITCH REGISTER
0423  02742 063207         LDA BIT2
0424  02743 000010         SLA            LOOP FOR SCOPE CHK?
0425  02744 026735         JMP P5         YES.
0426  02745 063206         LDA BIT1       NO.
0427  02746 000010         SLA            HALT TO CHK MCFF,MRFF?
0428  02747 102000         HLT 0
0429*
0430*INTERRUPT AND INTERLOCK TEST
0431  02750 017272         JSB ERAD       INCREMENT ERROR MESSAGE
0432  02751 017425         JSB IBAD       PREPARE ILLEGAL INTERRUPT
0433  02752 102100         STF 0          ENABLE INTERRUPT SYSTEM
0434  02753 106700  P6     CLC 0          ENABLE INTERRUPT ASSIGNMENT
0435  02754 002400         CLA
0436  02755 102600  OTA10  OTA 0          ASSIGN FLAG INTERRUPT
0437  02756 103100  CLF2   CLF 0          CLEAR FBFF
0438  02757 102700  STC2   STC 0          ILLEGAL INTERRUPT
0439  02760 017164         JSB MODE
0440  02761 102100         STF 0          ENABLE INTERRUPT SYSTEM
0441  02762 063207         LDA BIT2
0442  02763 000010         SLA            LOOP?
0443  02764 026753         JMP P6         YES.
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```
0444  02765 063206         LDA BIT1      NO.
0445  02766 000010         SLA           HALT?
0446  02767 102000         HLT 0         YES.
0447  02770 017272         JSB ERAD      INCREMENT ERROR MESSAGE
0448  02771 017433         JSB IOK       PREPARE LEGAL INTERRUPT
0449  02772 103100 CLF3    CLF 0         CLEARS INTERLOCK AND FLAG
0450  02773 002400         CLA
0451  02774 102600 OTA11   OTA 0         2ND WORD TO DVSI SETS FBFF
0452  02775 000000         NOP
0453  02776 000000         NOP
0454  02777 000000         NOP
0455  03000 017306         JSB ERROR     SHOULD HAVE JUMPED IN INTERRUPT
0456  03001 000000         NOP
0457  03002 102100         STF 0         ENABLE INTERRUPT SYSTEM
0458  03003 017164         JSB MODE      STORE SWITCH REGISTER
0459  03004 063207         LDA BIT2
0460  03005 000010         SLA           LOOP?
0461  03006 026772         JMP CLF3      YES.
0462  03007 063206         LDA BIT1      NO.
0463  03010 000010         SLA           HALT?
0464  03011 102000         HLT 0         YES.
0465  03012 017272         JSB ERAD      INCREMENT ERROR MESSAGE
0466  03013 017425         JSB IBAD      PREPARE ILLEGAL INTERRUPT
0467  03014 006400         CLB
0468  03015 002400 P7      CLA
0469  03016 102600 OTA12   OTA 0         SHOULD SET FBFF NO INTERRUPT
0470  03017 000000         NOP
0471  03020 000000         NOP
0472  03021 102100         STF 0         ENABLE INTERRUPT SYSTEM
0473  03022 006011         SLB,RSS
0474  03023 017272         JSB ERAD      INCREMENT ERROR MESSAGE
0475  03024 017433         JSB IOK       PREPARE LEGAL INTERRUPT
0476  03025 103100 CLF4    CLF 0         CLEARS INTERLOCK TO INTERRUPT
0477  03026 000000         NOP
0478  03027 000000         NOP
0479  03030 017306         JSB ERROR     ERROR NO INTERRUPT WHEN FBFF SET
0480  03031 000000         NOP
0481  03032 000000         NOP
0482  03033 102100         STF 0         ENABLE INTERRUPT SYSTEM
0483  03034 017164         JSB MODE      STORE SWITCH REGISTER
0484  03035 067207         LDB BIT2
0485  03036 004010         SLB           LOOP?
0486  03037 027015         JMP P7        YES.
0487  03040 063206         LDA BIT1      NO.
0488  03041 000010         SLA           HALT?
0489  03042 102000         HLT 0
0490  03043 017272         JSB ERAD      INCREMENT ERROR MESSAGE
0491  03044 103100 CLF5    CLF 0         CLEARS INTERLOCK
0492  03045 002400         CLA
0493  03046 102600 OTA13   OTA 0         ASKS FOR INTERRUPT
0494  03047 000000         NOP
0495  03050 000000         NOP
0496  03051 000000         NOP
0497  03052 017306         JSB ERROR     SHOULD HAVE JUMPED IN INTERRUPT
0498  03053 000000         NOP
0499  03054 102100         STF 0         ENABLE INTERRUPT SYSTEM
0500  03055 017164         JSB MODE      STORE SWITCH REGISTER
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```
0501  03056 063207          LDA BIT2
0502  03057 000010          SLA              LOOP?
0503  03060 027044          JMP CLF5         YES.
0504  03061 063206          LDA BIT1         NO.
0505  03062 000010          SLA              HALT?
0506  03063 102000          HLT 0
0507*
0508*FLAG CONTROL AND ALARM CONTROL TEST
0509  03064 063162          LDA FLAG         PREPARE FLAG
0510  03065 073452          STA ASSGN          ASSIGNMENT
0511  03066 002400          CLA
0512  03067 017446          JSB CONTR        PERFORM FLAG CONTROL ROUTINE
0513  03070 063163          LDA ALRM         PREPARE ALARM
0514  03071 073452          STA ASSGN          ASSIGNMENT
0515  03072 002400          CLA
0516  03073 017446          JSB CONTR        PERFORM ALARM CONTROL ROUTINE
0517*
0518*ALARM OPERATION CHECK
0519  03074 107700          CLC 0,C          DISABLE INTERRUPT SYSTEM
0520  03075 006400          CLB
0521  03076 106600  OTB1    OTB 0            PREPARE WSFF FOR 2ND WORD
0522  03077 106500  LIB5    LIB 0            ASSIGN ALARM INTERRUPT
0523  03100 102700  STC3    STC 0            DISABLE ASSIGNMENT
0524  03101 102100          STF 0            ENABLE INTERRUPT SYSTEM
0525  03102 063150          LDA OTBUF        LOAD A WITH ADDRESS OF 1ST ALARM
0526  03103 072431          STA AS2          STORE A
0527  03104 017272  ALMSB   JSB ERAD
0528  03105 017433  LUP     JSB IOK          PREPARE LEGAL INTERRUPT
0529  03106 062431          LDA AS2
0530  03107 164000          LDB 0,I          LOAD ALARM INTO B
0531  03110 107700  CLCF1   CLC 0,C          INITIALIZE INTERLOCK,BUFFER,WSFF
0532  03111 102700  STC4    STC 0            DISABLE ASSIGNMENT
0533  03112 106600  OTB2    OTB 0            OUTPUT ALARM
0534  03113 000000          NOP
0535  03114 000000           NOP               SHOULD INTERRUPT
0536  03115 000000          NOP                 AND JUMP +2
0537  03116 017306          JSB ERROR        ERROR-DID NOT INTERRUPT
0538  03117 000000          NOP
0539  03120 000000          NOP
0540  03121 102100          STF 0            ENABLE INTERRUPT SYSTEM
0541  03122 017425          JSB IBAD         PREPARE ILLEGAL INTERRUPT
0542  03123 107700  CLCF2   CLC 0,C          INITIALIZE INTERLOCK,BUFFER,WSFF
0543  03124 102700  STC5    STC 0            DISABLE ASSIGNMENT
0544  03125 006400          CLB
0545  03126 106600  OTB3    OTB 0            INITIALIZE DATA BUFFERS
0546  03127 000000          NOP
0547  03130 000000          NOP
0548  03131 017164          JSB MODE         STORE SWITCH REGISTER
0549  03132 102100          STF 0            ENABLE INTERRUPT SYSTEM
0550  03133 063207          LDA BIT2
0551  03134 000010          SLA              LOOP?
0552  03135 027105          JMP LUP          YES.
0553  03136 063206          LDA BIT1         NO.
0554  03137 000010          SLA              HALT?
0555  03140 102000          HLT 0            YES.
0556  03141 062431          LDA AS2          NO. LOAD A WITH ALARM ADDRESS
0557  03142 164000          LDB 0,I          LOAD B WITH ALARM
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0558  03143 006007          INB,SZB,RSS   IS B AT TERMINATING VALUE?
0559  03144 126625          JMP BAT,I     END OF BASIC TEST EXIT
0560  03145 002004          INA           NO. INCREMENT ALARM ADDRESS
0561  03146 072431          STA AS2
0562  03147 027104          JMP ALMSB     LOOP WITH NEXT ALARM
0563*
0564  03150 003151  OTBUF    DEF *+1       ALARM
0565  03151 000001  A1       OCT 1           OUTPUT
0566  03152 000002  A2       OCT 2             BUFFER
0567  03153 000004  A3       OCT 4
0568  03154 000010  A4       OCT 10
0569  03155 000020  A5       OCT 20
0570  03156 000040  A6       OCT 40
0571  03157 000100  A7       OCT 100
0572  03160 000200  A8       OCT 200
0573  03161 177777  A9       OCT 177777    TERMINATION
0574  03162 102600  FLAG     OTA 0
0575  03163 102500  ALRM     LIA 0
0576*
0577*SWITCH STORAGE ROUTINE
0578*
0579  03164 000000  MODE     NOP           ENTER SWITCH STORAGE ROUTINE
0580  03165 072430           STA AS1       STORE A
0581  03166 102501           LIA 1         EACH BIT FROM
0582  03167 073205           STA BIT0       THE SWITCH REGISTER
0583  03170 001300           RAR              IS ROTATED TO LEAST
0584  03171 073206           STA BIT1          SIGNIFICANT POSITION
0585  03172 001300           RAR                 AND IS STORED IN ITS
0586  03173 073207           STA BIT2              RELATIVE LOCATION
0587  03174 001300           RAR
0588  03175 073210           STA BIT3
0589  03176 001300           RAR
0590  03177 073211           STA BIT4
0591  03200 063205           LDA BIT0      HALT AT BEGINNING
0592  03201 000010           SLA             OF PROGRAM?
0593  03202 026007           JMP P1        YES.
0594  03203 062430           LDA AS1       NO. RESTORE A
0595  03204 127164           JMP MODE,I    EXIT SUBROUTINE
0596  03205 000000  BIT0     OCT 0         SWITCH
0597  03206 000000  BIT1     OCT 0           REGISTER
0598  03207 000000  BIT2     OCT 0             STORAGE
0599  03210 000000  BIT3     OCT 0
0600  03211 000000  BIT4     OCT 0
0601*
0602*STATUS FLAG 1ST WORD ROUTINE
0603*
0604  03212 000000  STAF1    NOP           ENTER SUBROUTINE
0605  03213 017272           JSB ERAD      STORE ERROR ADDRESS AND ADD ONE
0606  03214 102300  SFS3     SFS 0         IS STATUS FLAG CLEAR?
0607  03215 017306           JSB ERROR     NO.SFS-NO SKIP-STAT FLAG CLEAR
0608  03216 017164           JSB MODE      STORE SWITCH REGISTER
0609  03217 063207           LDA BIT2
0610  03220 000010           SLA           LOOP?
0611  03221 027214           JMP SFS3      YES.
0612  03222 063206           LDA BIT1      NO.
0613  03223 000010           SLA           HALT?
0614  03224 102000           HLT 0         YES.
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0615  03225 017272          JSB ERAD       INCREMENT ERROR MESSAGE
0616  03226 102200  SFC3    SFC 0          IS STATUS FLAG SET?
0617  03227 027231          JMP *+2        NO.
0618  03230 017306          JSB ERROR      YES. SFC-SKIP-FLAG CLEAR-ERROR
0619  03231 017164          JSB MODE       STORE SWITCH REGISTER
0620  03232 063207          LDA BIT2
0621  03233 000010          SLA            LOOP FOR SCOPE TEST?
0622  03234 027226          JMP SFC3       YES.
0623  03235 063206          LDA BIT1       NO.
0624  03236 000010          SLA            HALT?
0625  03237 102000          HLT 0          YES.
0626  03240 002400          CLA
0627  03241 127212          JMP STAF1,I    EXIT SUBROUTINE
0628*
0629*STATUS FLAG 2ND WORD ROUTINE
0630*
0631  03242 000000  STAF2 NOP              ENTER SUBROUTINE
0632  03243 017272          JSB ERAD       INCREMENT ERROR MESSAGE
0633  03244 102300  SFS4    SFS 0          IS STATUS FLAG CLEAR?
0634  03245 027247          JMP *+2        NO.
0635  03246 017306          JSB ERROR      YES. SFS-SKIP-FLAG SET-ERROR
0636  03247 017164          JSB MODE       STORE SWITCH REGISTER
0637  03250 063207          LDA BIT2
0638  03251 000010          SLA            LOOP?
0639  03252 027244          JMP SFS4       YES.
0640  03253 063206          LDA BIT1       NO.
0641  03254 000010          SLA            HALT?
0642  03255 102000          HLT 0          YES.
0643  03256 017272          JSB ERAD       NO. INCREMENT ERROR
0644  03257 102200  SFC4    SFC 0          IS STATUS FLAG SET?
0645  03260 017306          JSB ERROR      NO. SFC-NO SKIP-FLAG SET-ERROR
0646  03261 017164          JSB MODE       YES.
0647  03262 063207          LDA BIT2
0648  03263 000010          SLA            LOOP?
0649  03264 027257          JMP SFC4       YES.
0650  03265 063206          LDA BIT1       NO.
0651  03266 000010          SLA            HALT?
0652  03267 102000          HLT 0          YES.
0653  03270 002400          CLA
0654  03271 127242          JMP STAF2,I    EXIT SUBROUTINE
0655*
0656* INCREMENT ERROR NUMBER ROUTINE
0657*
0658  03272 000000  ERAD    NOP            INCREMENT/ERROR STORE ROUTINE
0659  03273 072430          STA AS1        STORE A
0660  03274 076435          STB BS1        STORE B
0661  03275 063304          LDA ERR1       LOAD CURRENT ERROR
0662  03276 073337          STA ERDAT      STORE
0663  03277 002004          INA            INCREMENT ERROR
0664  03300 073304          STA ERR1       STORE NEW NUMBER
0665  03301 062430          LDA AS1        RESTORE A
0666  03302 066435          LDB BS1        RESTORE B
0667  03303 127272          JMP ERAD,I     EXIT
0668  03304 000000  ERR1    OCT 0          ERROR STORAGE
0669  03305 000000  ERR2    OCT 0          INITIAL ERROR
0670*
0671*ERROR PRINTOUT ROUTINE
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0672*
0673  03306 000000  ERROR NOP           ERROR SUBROUTINE
0674  03307 063207        LDA BIT2
0675  03310 000010        SLA
0676  03311 027336        JMP E1
0677  03312 103100        CLF 0         DISABLE INTERRUPT SYSTEM
0678  03313 063337        LDA ERDAT     LOAD ERROR NUMBER IN A
0679  03314 001700        ALF           PACK
0680  03315 012413        AND MSK3        ERROR
0681  03316 017406        JSB .2NUM         NUMBER
0682  03317 076353        STB MES9+3          AND
0683  03320 063337        LDA ERDAT             STORE
0684  03321 001727        ALF,ALF                 IT IN THE
0685  03322 001222        RAL,RAL                   ERROR
0686  03323 017406        JSB .2NUM                   MESSAGE
0687  03324 076354        STB MES9+4
0688  03325 001700        ALF
0689  03326 001222        RAL,RAL
0690  03327 017406        JSB .2NUM
0691  03330 076355        STB MES9+5
0692  03331 062356        LDA ML9       BASIC TEST
0693  03332 066347        LDB MAD9        ERROR
0694  03333 114102        JSB 102B,I        MESSAGE
0695  03334 063337        LDA ERDAT
0696  03335 102000        HLT 0
0697  03336 127306  E1    JMP ERROR,I   EXIT
0698  03337 000000  ERDAT OCT 0          ERROR NUMBER STORAGE
0699*
0700*DATA BUFFER ERROR PRINTOUT
0701*
0702  03340 000000  DAT   NOP           OUTPUT/INPUT PRINTOUT ROUTINE
0703  03341 076436        STB BS2       STORE B
0704  03342 072433        STA AS4       STORE A
0705  03343 001700        ALF           PACK
0706  03344 012413        AND MSK3        OUTPUT
0707  03345 017406        JSB .2NUM         WORD
0708  03346 076365        STB MES10+5         AND
0709  03347 062433        LDA AS4               STORE
0710  03350 001727        ALF,ALF                 IT IN
0711  03351 001222        RAL,RAL                   THE
0712  03352 017406        JSB .2NUM                   ERROR
0713  03353 076366        STB MES10+6                   MESSAGE
0714  03354 001700        ALF
0715  03355 001222        RAL,RAL
0716  03356 017406        JSB .2NUM
0717  03357 076367        STB MES10+7
0718  03360 062436        LDA BS2       PACK
0719  03361 001700        ALF             INPUT
0720  03362 012413        AND MSK3          WORD
0721  03363 017406        JSB .2NUM           AND
0722  03364 076377        STB MES10+15          STORE
0723  03365 062436        LDA BS2                 IT IN
0724  03366 001727        ALF,ALF                   THE
0725  03367 001222        RAL,RAL                     ERROR
0726  03370 017406        JSB .2NUM                     MESSAGE
0727  03371 076400        STB MES10+16
0728  03372 001700        ALF
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0729  03373 001222          RAL,RAL
0730  03374 017406          JSB .2NUM
0731  03375 076401          STB MES10+17
0732  03376 062402          LDA ML10        PRINT ERROR MESSAGE
0733  03377 066357          LDB MAD10         OUTPUT =        INPUT =
0734  03400 114102          JSB 102B,I
0735  03401 016417          JSB EOL         LINE FEED
0736  03402 102000          HLT 0           HALT AFTER ERROR
0737  03403 062433          LDA AS4         RESTORE A
0738  03404 066436          LDB BS2         RESTORE B
0739  03405 127340          JMP DAT,I       EXIT SUBROUTINE
0740*
0741*PACK TWO ASCII NUMBERS SUBROUTINE
0742*
0743  03406 000000  .2NUM NOP              ENTER SUBROUTINE
0744  03407 072434          STA AS5         STORE A
0745  03410 001323          RAR,RAR         FORMAT
0746  03411 001300          RAR               FIRST
0747  03412 012412          AND MSK2            NUMBER
0748  03413 032414          IOR C1
0749  03414 001727          ALF,ALF
0750  03415 070001          STA 1           STORE IT IN B REG
0751  03416 062434          LDA AS5         FORMAT
0752  03417 012412          AND MSK2          SECOND
0753  03420 032414          IOR C1              NUMBER
0754  03421 030001          IOR 1           PACK BOTH
0755  03422 070001          STA 1             NUMBERS INTO B
0756  03423 062434          LDA AS5         RESTORE A
0757  03424 127406          JMP .2NUM,I     EXIT SUBROUTINE
0758*
0759*
0760  03425 000000  IBAD  NOP              ILLEGAL INTERRUPT ROUTINE
0761  03426 063432          LDA ERJMP       STORE ERROR
0762  03427 070000  STA1  STA 0               ROUTINE IN DVSI ADDRESS
0763  03430 002400          CLA
0764  03431 127425          JMP IBAD,I      EXIT SUBROUTINE
0765  03432 114110  ERJMP  JSB 110B,I      IBAD STATEMENT
0766*
0767*
0768  03433 000000  IOK   NOP              LEGAL INTERRUPT ROUTINE
0769  03434 063437          LDA SBOK        STORE LEGAL JUMP
0770  03435 070000  STA2  STA 0               ROUTINE IN DVSI ADDRESS
0771  03436 127433          JMP IOK,I       EXIT SUBROUTINE
0772  03437 114111  SBOK  JSB 111B,I      IOK STATEMENT
0773*
0774*
0775  03440 000000  INTR  NOP              LEGAL JUMP ROUTINE
0776  03441 063440          LDA INTR        EQUIVALENT
0777  03442 002004          INA               TO A
0778  03443 002004          INA                JMP *+2
0779  03444 073440          STA INTR             IN DVSI ADDRESS
0780  03445 127440          JMP INTR,I      EXIT TO NEW ADDRESS
0781*
0782*
0783  03446 000000  CONTR NOP              INTERRUPT CONTROL SUBROUTINE
0784  03447 002400          CLA               USING STF AND STC TO TEST
0785  03450 106700  CLC4  CLC 0
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0786  03451 103100  CLF6   CLF 0
0787  03452 102621  ASSGN  OTA 17        ASSIGNS FLAG OR ALARM MODE
0788  03453 017272        JSB ERAD       INCREMENT ERROR MESSAGE
0789  03454 017425        JSB IBAD       PREPARE ILLEGAL INTERRUPT
0790  03455 102100  STF1   STF 0         NO INTERRUPT CONTROL NOT SET
0791  03456 000000        NOP
0792  03457 000000        NOP
0793  03460 102100        STF 0          ENABLE INTERRUPT SYSTEM
0794  03461 102100  STF2   STF 0         TO RESET FBFF IF INTERRUPTS
0795  03462 017272        JSB ERAD       INCREMENT ERROR MESSAGE
0796  03463 017433        JSB IOK        PREPARE LEGAL INTERRUPT
0797  03464 102700  STC6   STC 0         SHOULD INTERRUPT (INTERLOCK SET)
0798  03465 000000        NOP
0799  03466 000000        NOP
0800  03467 017306        JSB ERROR
0801  03470 000000        NOP
0802  03471 102100        STF 0          ENABLE INTERRUPT SYSTEM
0803  03472 017272        JSB ERAD       INCREMENT ERROR MESSAGE
0804  03473 017425        JSB IBAD       PREPARE ILLEGAL INTERRUPT
0805  03474 106700  CLC5   CLC 0         ENABLES STF
0806  03475 102100  STF3   STF 0         SETS FBFF
0807  03476 102700  STC7   STC 0         INTERLOCK STILL SET NO INTERRUPT
0808  03477 000000        NOP
0809  03500 000000        NOP
0810  03501 102100        STF 0          ENABLE INTERRUPT SYSTEM
0811  03502 017272        JSB ERAD       INCREMENT ERROR MESSAGE
0812  03503 017433        JSB IOK        PREPARE LEGAL INTERRUPT
0813  03504 103100  CLF7   CLF 0         CLEARS INTELOCK SHOULD INTERRUPT
0814  03505 000000        NOP
0815  03506 000000        NOP
0816  03507 017306        JSB ERROR      FBFF CLEAR? INTERLOCK SET?
0817  03510 000000        NOP
0818  03511 000000        NOP
0819  03512 102100        STF 0          ENABLE INTERRUPT SYSTEM
0820  03513 017272        JSB ERAD       INCREMENT ERROR
0821  03514 017425        JSB IBAD       PREPARE ILLEGAL INTERRUPT
0822  03515 106700  CLC9   CLC 0         ENABLES STF
0823  03516 102100  STF4   STF 0         SETS FBFF
0824  03517 103100  CLF8   CLF 0         CLEARS FBFF, INTERLOCK
0825  03520 102700  STC8   STC 0         SHOULDNT INTERRUPT
0826  03521 000000        NOP
0827  03522 017164        JSB MODE       STORE SWITCH REGISTER
0828  03523 102100        STF 0          ENABLE INTERRUPT SYSTEM
0829  03524 063207        LDA BIT2
0830  03525 000010        SLA            LOOP?
0831  03526 027515        JMP CLC9       YES.
0832  03527 063206        LDA BIT1       NO.
0833  03530 000010        SLA            HALT?
0834  03531 102000        HLT 0          YES.
0835  03532 127446        JMP CONTR,I    EXIT SUBROUTINE
0836*
0837*DATA BUFFER TESTS
0838*
0839  03533 000000  DOIC   NOP           DATA OUT/IN COMPARE ROUTINE
0840  03534 107700        CLC 0,C        DISABLE INTERRUPT SYSTEM
0841  03535 062242        LDA ML4        PRINT MESSAGE -
0842  03536 066217        LDB MAD4         DATA BUFFER TEST PLUG NO.1
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0843  03537 114102          JSB 102B,I        PUSH RUN
0844  03540 016417          JSB EOL           LINE FEED
0845  03541 102000          HLT 0
0846  03542 067755          LDB LOOP3         TEST LOOP CONDITION
0847  03543 077765          STB LOOP
0848  03544 065740          LDB INIT1         LOAD INITIAL
0849  03545 075743          STB COMPR           OUTPUT FOR COMPARISON
0850  03546 075742          STB OUT              AND STORE
0851  03547 065745          LDB COND1         FIRST TEST CONDITION
0852  03550 077623          STB COND
0853  03551 017570          JSB START         EXECUTE 1ST TEST
0854  03552 062264          LDA ML5           PRINT MESSAGE -
0855  03553 066243          LDB MAD5            CONNECT PLUG NO. 2
0856  03554 114102          JSB 102B,I             AND PUSH RUN
0857  03555 016417          JSB EOL           LINE FEED
0858  03556 102001          HLT 1             HALT TO CONNECT PLUG NO. 2
0859  03557 067755          LDB LOOP3         TEST LOOP CONDITION
0860  03560 077765          STB LOOP
0861  03561 065740          LDB INIT1         LOAD INITIAL OUTPUT
0862  03562 075743          STB COMPR           FOR COMPARISON - STORE
0863  03563 117776          JSB TST2,I        SET UP END PTS AND CONTROL, TEST
0864  03564 067756          LDB COND2         SECOND TEST CONDITION
0865  03565 077623          STB COND
0866  03566 017570          JSB START         EXECUTE 2ND TEST
0867  03567 027625          JMP SUBIC         JUMP TO TEST 3,4 ROUTINE
0868*
0869*
0870  03570 000000  START NOP               DATA BUFFER SUBROUTINE
0871  03571 027757        JMP PT2           CLEAR DATA BUFFERS
0872  03572 065742  PT1   LDB OUT           PLACE OUTPUT WORD IN B REG
0873  03573 106700  CLC6  CLC 0             DISABLE INTERRUPT
0874  03574 106600  OTB4  OTB 0             OUTPUT B TO DVSI
0875  03575 102700  STC9  STC 0             DISABLE MODE ASSIGNMENT
0876  03576 017766        JSB DELAY         TIME DELAY FOR BUFFERS TO SETTLE
0877  03577 102500  LIA1  LIA 0             PLACE IOBI WORD IN A REG
0878  03600 031751        IOR MSK4          MASK BITS 15,14,13
0879  03601 072432        STA AS3
0880  03602 017164        JSB MODE          CHECK SWITCH REGISTER
0881  03603 063207        LDA BIT2
0882  03604 000010        SLA               LOOP FOR SCOPE TEST?
0883  03605 027757        JMP PT2           YES.
0884  03606 063206        LDA BIT1          NO.
0885  03607 000010        SLA               HALT TO SET SW REG?
0886  03610 102000        HLT 0             YES.
0887  03611 066432        LDB AS3           LOAD INPUT IN B
0888  03612 061743        LDA COMPR         LOAD OUTPUT COMPARISON IN A
0889  03613 055743        CPB COMPR         OUTPUT = INPUT?
0890  03614 027616        JMP *+2           YES.
0891  03615 017340        JSB DAT           NO. ERROR PRINTOUT
0892  03616 061743        LDA COMPR
0893  03617 051746        CPA END1          IS THIS THE LAST TEST?
0894  03620 127570        JMP START,I       YES. EXIT SUBROUTINE
0895  03621 002004        INA               NO. NEXT OUTPUT WORD
0896  03622 071743        STA COMPR
0897  03623 071742  COND  STA OUT           1ST OR 2ND TEST CONDITION
0898  03624 027572        JMP PT1           NEXT OUTPUT
0899*
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0900*
0901  03625 062306  SDOIC LDA ML6       PRINT MESSAGE -
0902  03626 066265        LDB MAD6        CONNECT PLUG NO. 3
0903  03627 114102        JSB 102B,I        AND PUSH RUN
0904  03630 016417        JSB EOL
0905  03631 102003        HLT 3           HALT TO CONNECT PLUG NO. 3
0906  03632 067753        LDB LOOP1       TEST LOOP CONDITION
0907  03633 077765        STB LOOP
0908  03634 065741        LDB INIT        SET UP AND
0909  03635 075744        STB CPR           STORE 1ST
0910  03636 075742        STB OUT             OUTPUT FOR
0911  03637 075743        STB COMPR             COMPARISON
0912  03640 065742  PT3   LDB OUT         LOAD
0913  03641 106700  CLC7  CLC 0             AND
0914  03642 106600  OTB5  OTB 0                OUTPUT
0915  03643 106600  OTB6  OTB 0                  2ND WORD
0916  03644 102700  STC10 STC 0           DISABLE MODE ASSIGNMENT
0917  03645 017766        JSB DELAY       TIME DELAY FOR BUFFERS TO SETTLE
0918  03646 102500  LIA2  LIA 0           PLACE IOBI WORD IN A REG
0919  03647 072432        STA AS3         STORE INPUT
0920  03650 017164        JSB MODE        CHECK SWITCH REGISTER
0921  03651 063207        LDA BIT2
0922  03652 000010        SLA             LOOP FOR TESTING?
0923  03653 027757        JMP PT2         YES.
0924  03654 063206        LDA BIT1        NO.
0925  03655 000010        SLA             HALT?
0926  03656 102000        HLT 0           YES.
0927  03657 066432        LDB AS3         LOAD INPUT IN B
0928  03660 061744        LDA CPR         LOAD OUTPUT COMPARISON IN A
0929  03661 055744        CPB CPR         OUTPUT = INPUT?
0930  03662 027664        JMP *+2         YES.
0931  03663 017340        JSB DAT         NO. ERROR PRINTOUT
0932  03664 061743        LDA COMPR
0933  03665 031751        IOR MSK4
0934  03666 051747        CPA END2        IS THIS THE LAST TEST?
0935  03667 027701        JMP FINIS       YES.
0936  03670 002004        INA             NO. INCREMENT COMPARISON
0937  03671 071743        STA COMPR
0938  03672 031752        IOR MSK5        MASK BIT 4
0939  03673 071744        STA CPR         STORE IN OUTPUT COMPARISON
0940  03674 065743        LDB COMPR       SHIFT COMPARISON
0941  03675 005020        BLS,BLS           OUTPUT FROM POSITIONS
0942  03676 005000        BLS                 0-4 TO 3-7 AND STORE
0943  03677 075742        STB OUT               IN OUTPUT LOCATION
0944  03700 027640        JMP PT3         NEXT OUTPUT
0945  03701 062330  FINIS LDA ML7         PRINT MESSAGE -
0946  03702 066307        LDB MAD7        CONNECT PLUG NO. 4
0947  03703 114102        JSB 102B,I        AND PUSH RUN
0948  03704 016417        JSB EOL
0949  03705 102007        HLT 7           HALT TO CONNECT PLUG NO. 4
0950  03706 067754        LDB LOOP2       TEST LOOP CONDITION
0951  03707 077765        STB LOOP
0952  03710 065741        LDB INIT        SET UP AND STORE
0953  03711 075742        STB OUT           1ST OUTPUT WORD
0954  03712 061753        LDA CMPBF       LOAD ADDRESS OF 1ST
0955  03713 071764        STA ADCMP         COMPARISON WORD AND STORE
0956  03714 165764  PT5   LDB ADCMP,I     LOAD OUTPUT COMPARISON INTO B
```

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```
0957  03715 075744          STB CPR
0958  03716 065742          LDB OUT        LOAD
0959  03717 106700  CLC10   CLC 0            AND
0960  03720 106600  OTB7    OTB 0              OUTPUT
0961  03721 106600  OTB8    OTB 0                2ND WORD
0962  03722 102700  STC11   STC 0          DISABLE MODE ASSIGNMENT
0963  03723 017766          JSB DELAY      TIME DELAY FOR BUFFERS TO SETTLE
0964  03724 102500  LIA3    LIA 0          PLACE IOBI WORD IN A REG
0965  03725 072432          STA AS3        STORE INPUT
0966  03726 017164          JSB MODE
0967  03727 063207          LDA BIT2
0968  03730 000010          SLA            LOOP FOR TEST?
0969  03731 027757          JMP PT2        YES.
0970  03732 063206          LDA BIT1       NO.
0971  03733 000010          SLA            HALT?
0972  03734 102000          HLT 0          YES.
0973  03735 066432          LDB AS3        LOAD INPUT IN B
0974  03736 061744          LDA CPR        LOAD OUTPUT COMPARISON IN A
0975  03737 055744          CPB CPR        OUTPUT = INPUT?
0976  03740 027742          JMP *+2        YES.
0977  03741 017340          JSB DAT        NO. ERROR PRINTOUT
0978  03742 065742          LDB OUT
0979  03743 055750          CPB END3       IS THIS THE LAST DATA WORD?
0980  03744 127533          JMP DOIC,I     EXIT SUBROUTINE
0981  03745 006004          INB            NO. INCREMENT
0982  03746 075742          STB OUT          AND STORE
0983  03747 061764          LDA ADCMP      NEXT
0984  03750 002004          INA              COMPARISON
0985  03751 071764          STA ADCMP          WORD
0986  03752 027714          JMP PT5        NEXT OUTPUT
0987*
0988  03753 027640  LOOP1   JMP PT3
0989  03754 027714  LOOP2   JMP PT5
0990  03755 027572  LOOP3   JMP PT1
0991  03756 117776  COND2   JSB TST2,I     CALL TEST2
0992*
0993  03757 006400  PT2     CLB            LOOP ENTRY POINT
0994  03760 106700          CLC 0
0995  03761 106600  OTB9    OTB 0            TO CLEAR THE
0996  03762 106600  OTB10   OTB 0              DATA BUFFERS
0997  03763 000000          NOP
0998  03764 000000          NOP
0999  03765 027572  LOOP    JMP PT1
1000*
1001*
1002  03766 000000  DELAY   NOP            ENTER SUBROUTINE
1003  03767 072432          STA AS3        STORE A
1004  03770 063775          LDA TIME       LOAD TIME DELAY
1005  03771 034000          ISZ 0          COUNT TO TIME
1006  03772 027771          JMP *-1          THEN CONTINUE
1007  03773 062432          LDA AS3        RESTORE A
1008  03774 127766          JMP DELAY,I
1009  03775 177760  TIME    OCT -20
1010*
1011*
1012  03776 004000  TST2    DEF TEST2      TEST2 LINKAGE
1013  04000                 ORG 4000B      ORIGIN OF TEST2
```

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```
1014  04000 000000  TEST2 NOP             ROUTINE TO SHIFT IOBO BITS
1015  04001 065743        LDB COMPR         FROM POSITIONS 0-7 TO
1016  04002 005727        BLF,BLF             POSITIONS 8-15
1017  04003 075742        STB OUT         STORE IOBO IN OUTPUT STORAGE
1018  04004 006400        CLB
1019  04005 126000        JMP TEST2,I     EXIT
1020*
1021  04006         X     EQU *           FWAM - 1ST WD AVAIL MEM.
1022*
1023  01740               ORG 1740B       DATA STORAGE
1024  01740 160000  INIT1 OCT 160000
1025  01741 120000  INIT  OCT 120000      INITIAL VALUE IOBO
1026  01742 000000  OUT   OCT 0           IOBO OUTPUT WORD STORAGE
1027  01743 000000  COMPR OCT 0
1028  01744 000000  CPR   OCT 0
1029  01745 071742  COND1 STA OUT
1030  01746 160377  END1  OCT 160377
1031  01747 160037  END2  OCT 160037
1032  01750 120007  END3  OCT 120007      TERMINATING VALUE 3 BITS
1033  01751 160000  MSK4  OCT 160000
1034  01752 000020  MSK5  OCT 20          BIT 4 MASK
1035*
1036  01753 001754  CMPBF DEF *+1
1037  01754 160001  D1    OCT 160001
1038  01755 160002  D2    OCT 160002
1039  01756 160004  D3    OCT 160004
1040  01757 160010  D4    OCT 160010
1041  01760 120020  D5    OCT 120020
1042  01761 120040  D6    OCT 120040
1043  01762 120100  D7    OCT 120100
1044  01763 120200  D8    OCT 120200
1045  01764 000000  ADCMP OCT 0
1046*
1047*
1048                      END
**  NO ERRORS*
```

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