

CHAPTER 8 Q10CMS - COLOR MONITOR SUBBOARD -

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8.1 General

This sub board is mounted on the main board via connectors CN9 and CN10 provided on the main board (Q10 SYM board), and used as an interface board for connection with a high resolution color monitor.

With this board, it is possible to draw a picture in piccell units and display 640 dots x 400 dots x 7 colors in specified color on the color monitor.

The output connector from QX-10 to the color monitor is the same CN4 as that at use of green monitor.

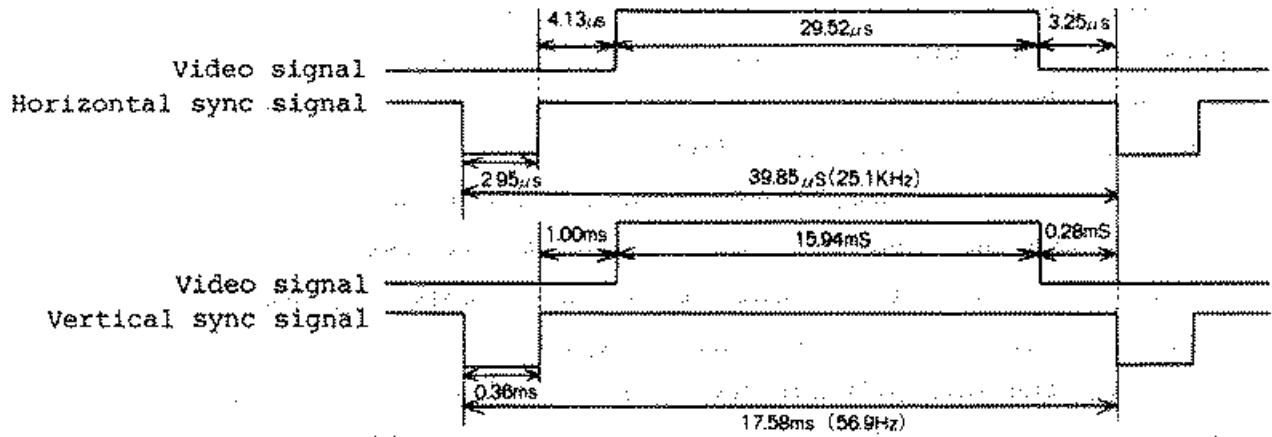
Connector CN5 on the rear panel can be used without modification for the light pen input.

When this sub board is mounted, pin definition of CN4 is different from that when the green monitor sub board (Q10 GMS or Q10 GGS board) is mounted, and it is not possible to display on the green monitor.

8.2 Specifications

Output signal	:	RGB separate output
		Video signal: TTL level positive polarity
		Horizontal sync signal: TTL level negative polarity
		Vertical sync signal: TTL level negative polarity
Scanning frequency:	Horizontal:	25.1 kHz
	Vertical :	56.9 Hz
Resolution	:	Horizontal: 640 dots
		Vertical : 400 lines

Signal timing:



NRZ signal of video signal DOT CLOCK 21.679 MHz, TTL level

Fig. 8-1

8.3 Block diagram

The block diagram of Q10 CMS board is shown in Fig. 8-2. GDC μ PD7220 is used as a display controller as in the green monitor sub board (Q10 GMS or Q10 GGS).

The GDC μ PD7220 assigns I/O addresses 2CH - 2DH and 38H - 3BH as I/O channels for the CPU.

The video memory has three color planes based on control by the GDC μ PD7220, each of which is used as memories for R, G and B. This reserves a large capacity without applying load to the CPU memory space.

Further, the GDC μ PD7220 has the calculating function for plotting or drawing pictures, enabling high speed processing.

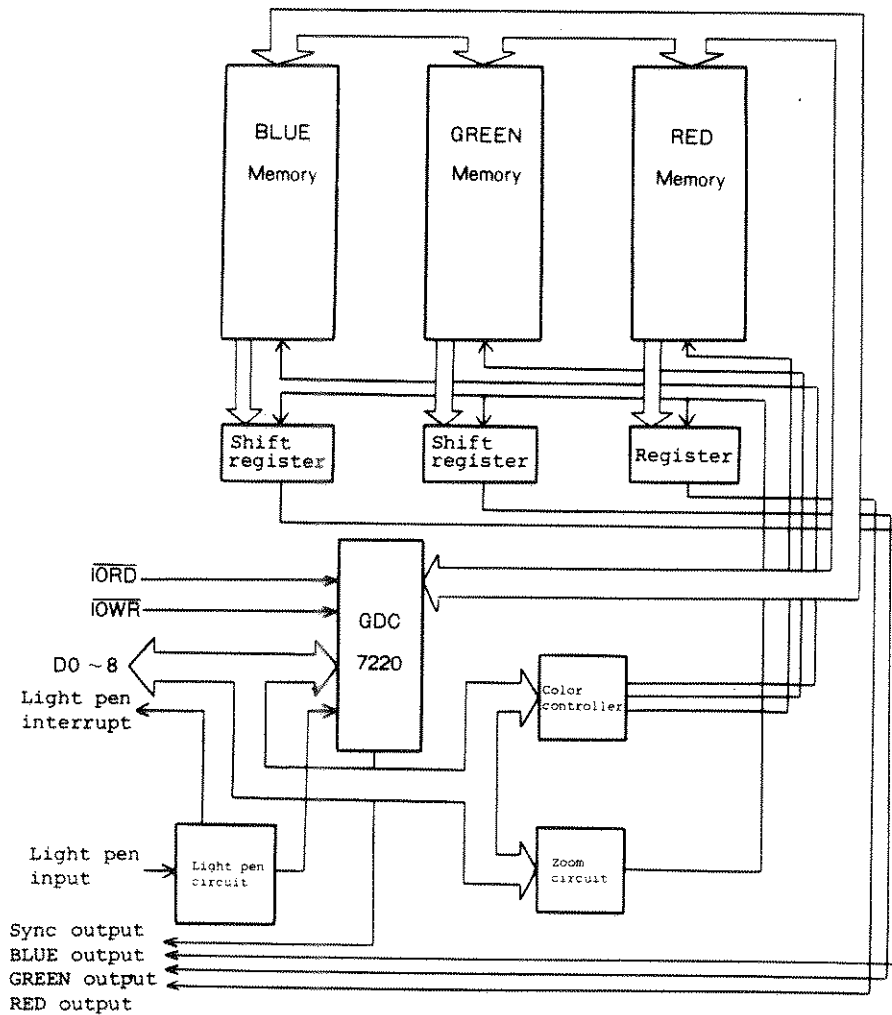


Fig. 8-2 Q10 CMS board block diagram

8.4 Configuration of video memory

The video memory exists in three planes for each color of R, G and B. One data consists of 16 bits. The memory of each color is 16K x 16 bits when the 16 kbit dynamic RAM is used, and 64 x 16 bits when the 64 kbit dynamic RAM is used.

Neutral tints can be expressed by writing the same capacity for more than two memory planes. In this case, memory banking is necessary for each color plane. Switching of these banks is performed by the color control register mapped in the I/O address 2DH. Corresponding memory planes will be connected to the GDC μ PD7220: blue if the contents of 2DH are 01H, green if 02H, and red if 04H.

However, when more than two of these low order three bits are set to 1, two or more memory planes will be selected causing contention for the bus. Therefore, when two or more memory planes are selected, they must be selected one by one.

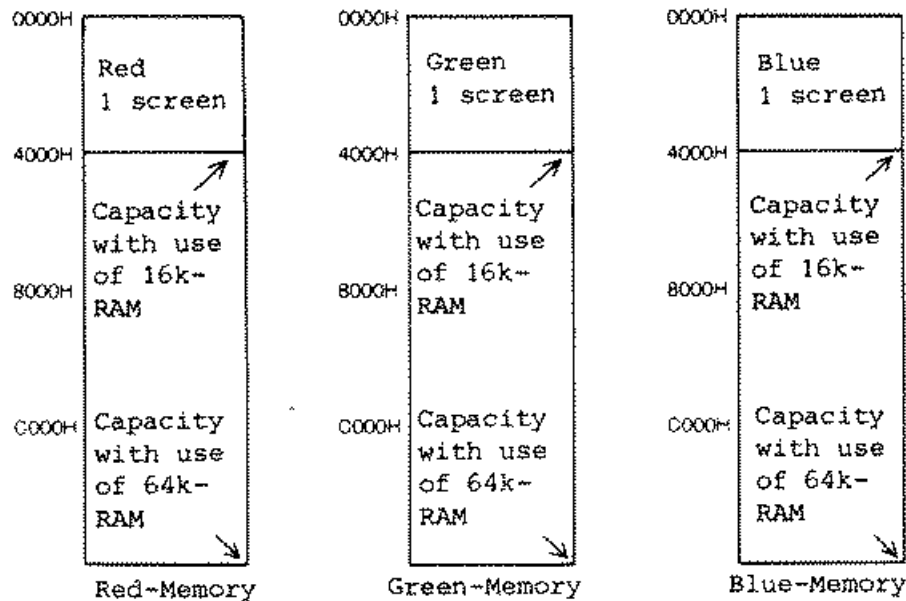


Fig. 8-3 Video memory map

The relationship between the memory address and raster is as shown in Fig. 8-4.

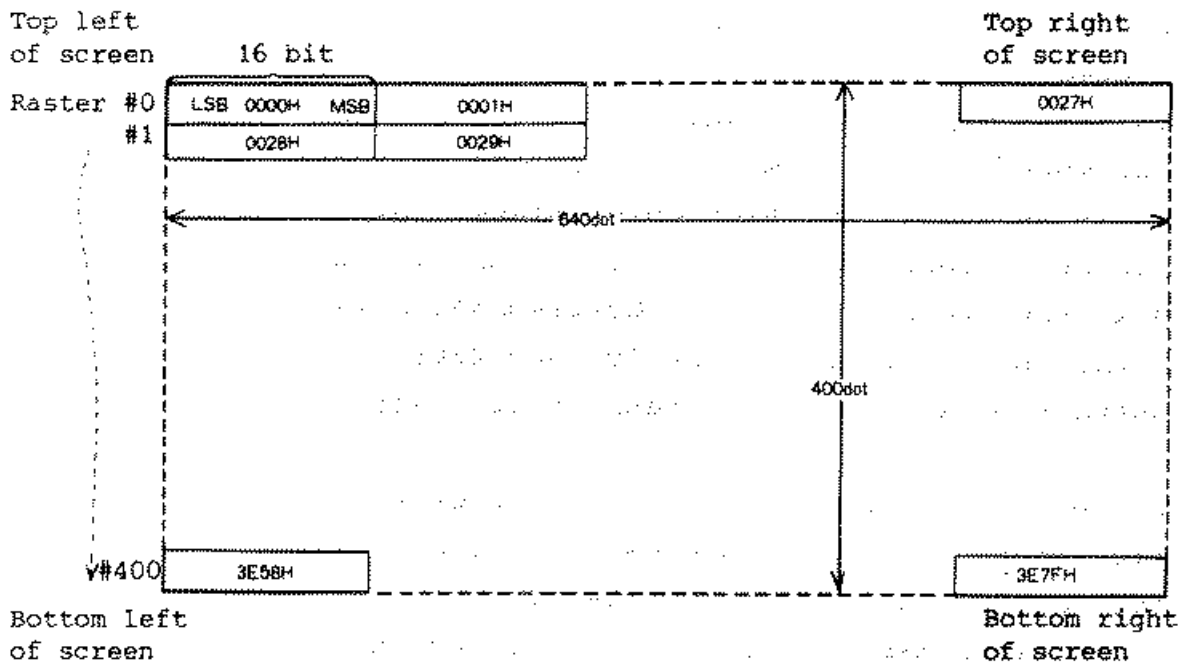


Fig. 8-4 Memory address and raster
(at non-zoom, start address = 0000H)

8.5 Sync signal

Horizontal and vertical sync signals are generated from the GDC μ PD7220. The scanning frequency is set by the SYNC command for GDC. In the case of QX-10, the type of monitor sub board is discriminated by reading the data of I/O port 2CH in IPL at switching power on, and the scanning frequencies for green monitor and color monitor are set by the software. As shown in Fig. 8-5, the D-type flip-flop is used in the sync signal output circuit so that the output polarity of sync signal can be selected for each monitor to be used by changing the jumper wires.

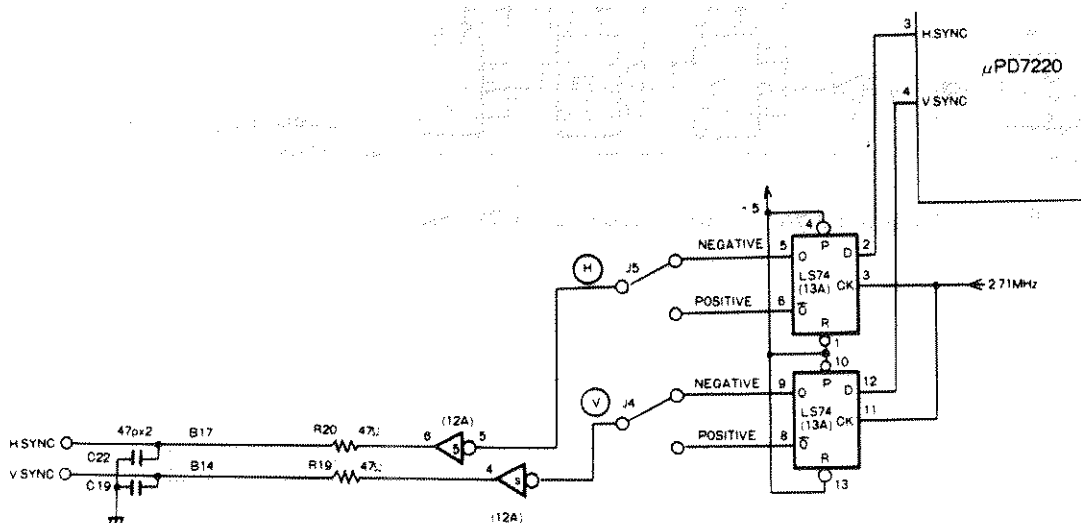


Fig. 8-5 Horizontal/vertical sync signal output circuit

8.6 Clock supply circuit

Fig. 8-6 shows the clock supply circuit on the Q10 CMS board. At the 2CCLK terminal of GDC μ PD7220, the original oscillation frequency 21.679 MHz of the oscillation module (CR1) is divided into eight by three flip-flops assigned to the 2-divider and supplied as a clock of 2.71 MHz.

The original oscillation frequency 21.679 is used as a dot clock of video signal, enabling drawing of pictures at the high speed of 0.046 μ sec/dot.

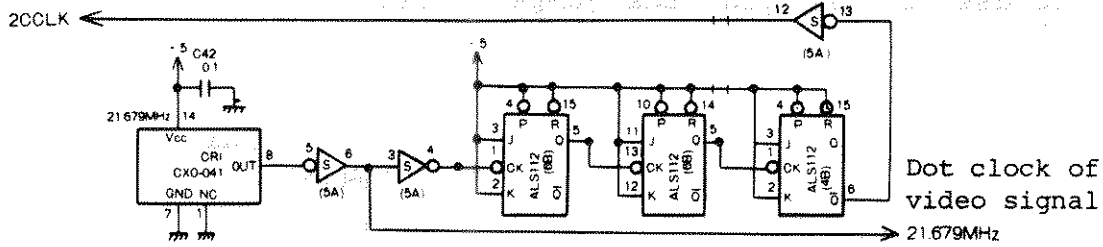


Fig. 8-6 Video signal dot clock 21.679 MHz

8.7 Video memory interface circuit

8.7.1 $\overline{\text{RAS}}/\overline{\text{CAS}}$ signal supply circuit

This color monitor sub board uses a 16K-bit or 64K-bit dynamic RAM for memory planes for each color of red, green and blue. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals required by this dynamic RAM are supplied by the circuit shown in Fig. 8-7.

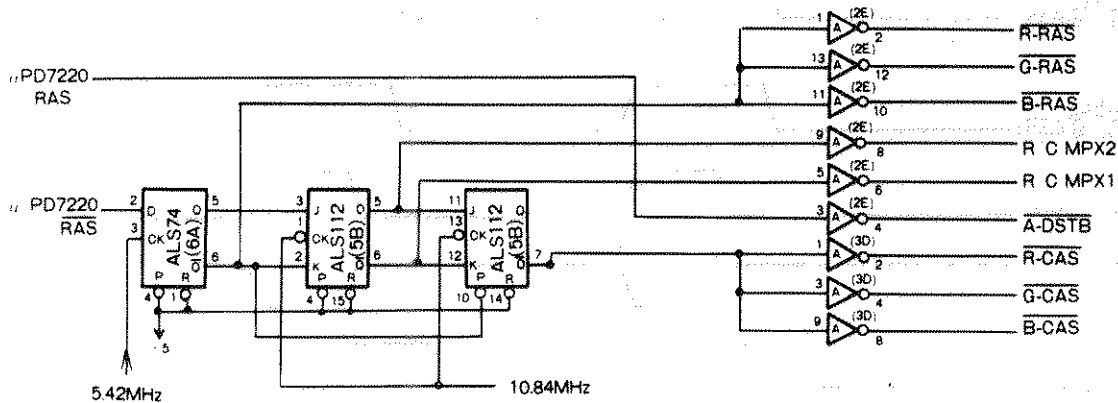


Fig. 8-7 $\overline{\text{RAS}}/\overline{\text{CAS}}$ signal supply circuit

The $\overline{\text{RAS}}$ signal for the color plane is supplied to the $\overline{\text{RAS}}$ signal terminal (pin 6) of GDC μPD7220 after being delayed 1/4 clock of 2CCLK (0.092 μsec) by the D-type flip-flop ALS74 (6A) which has 5.42 MHz as a clock. The $\overline{\text{CAS}}$ signal is supplied after being delayed more 1/4 clock (0.37 μsec) against the $\overline{\text{RAS}}$ signal.

In addition, this circuit also supplies the multiplex signal and $\overline{\text{ADSTB}}$ signal for the address multiplexer ALS573 (4C and 5C) for the video memory.

Fig. 8-8 shows the timing chart of these signals.

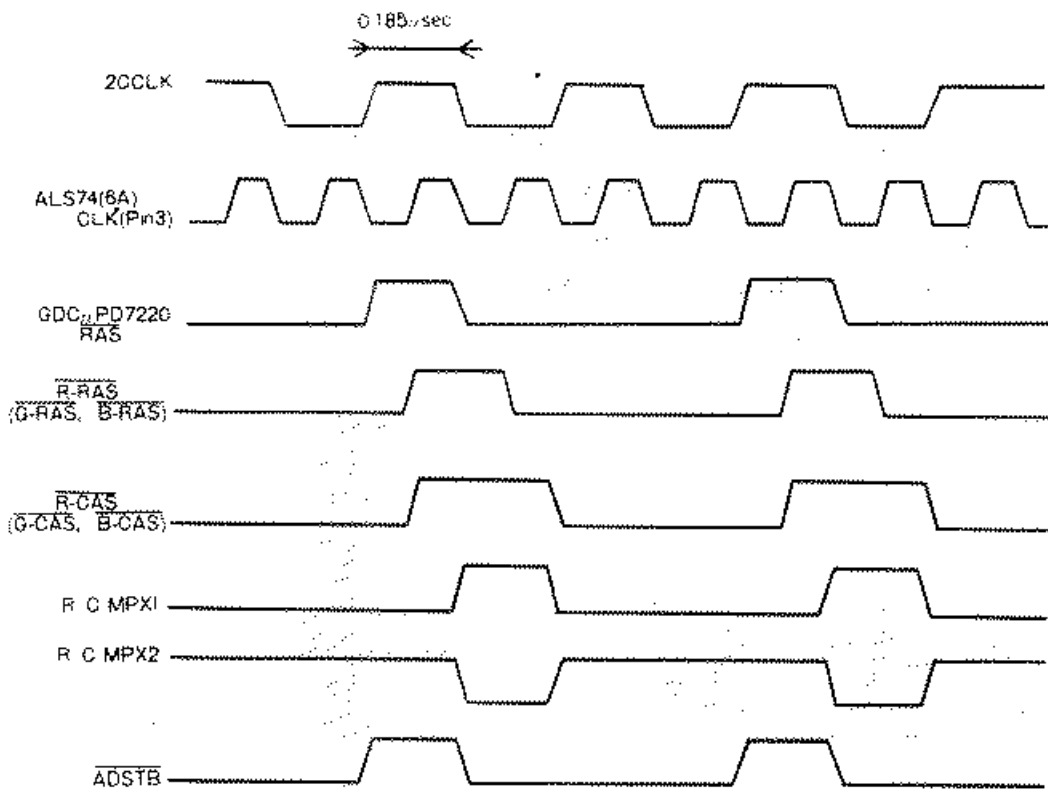


Fig. 8-8 $\overline{\text{RAS}}/\overline{\text{CAS}}$ signal timing

8.7.2 Video data read circuit

At the picture drawing (R/M/W) cycle of GDC μ PD7220, the video memory contents are read by the GDC μ PD7220. Fig. 8-9 shows the video data read circuit. Fig. 8-10 shows the read timing.

As the $\overline{\text{DBIN}}$ signal of the GDC μ PD7220 becomes low level when the video data is read, and the inputs to one end of each NAND gate of IC 3E become high level. The inputs to the other end of these NAND gates are memory plane select signals, only one of which is set to high level.

Then, as the output of the NAND gate whose two inputs are high level becomes low level, the G2 terminal of the 3-state buffer LS541 on the output data bus of any one of the memory planes selected becomes low active. On the other hand, data bus DB3 is connected to the G1 terminal of this 3-state buffer LS541.

DB3 becomes 0 when the READ command is executed. So, the G1 terminal becomes low level, too, the data of LS541 is output, and the GDC μ PD7220 is enabled to read the video memory.

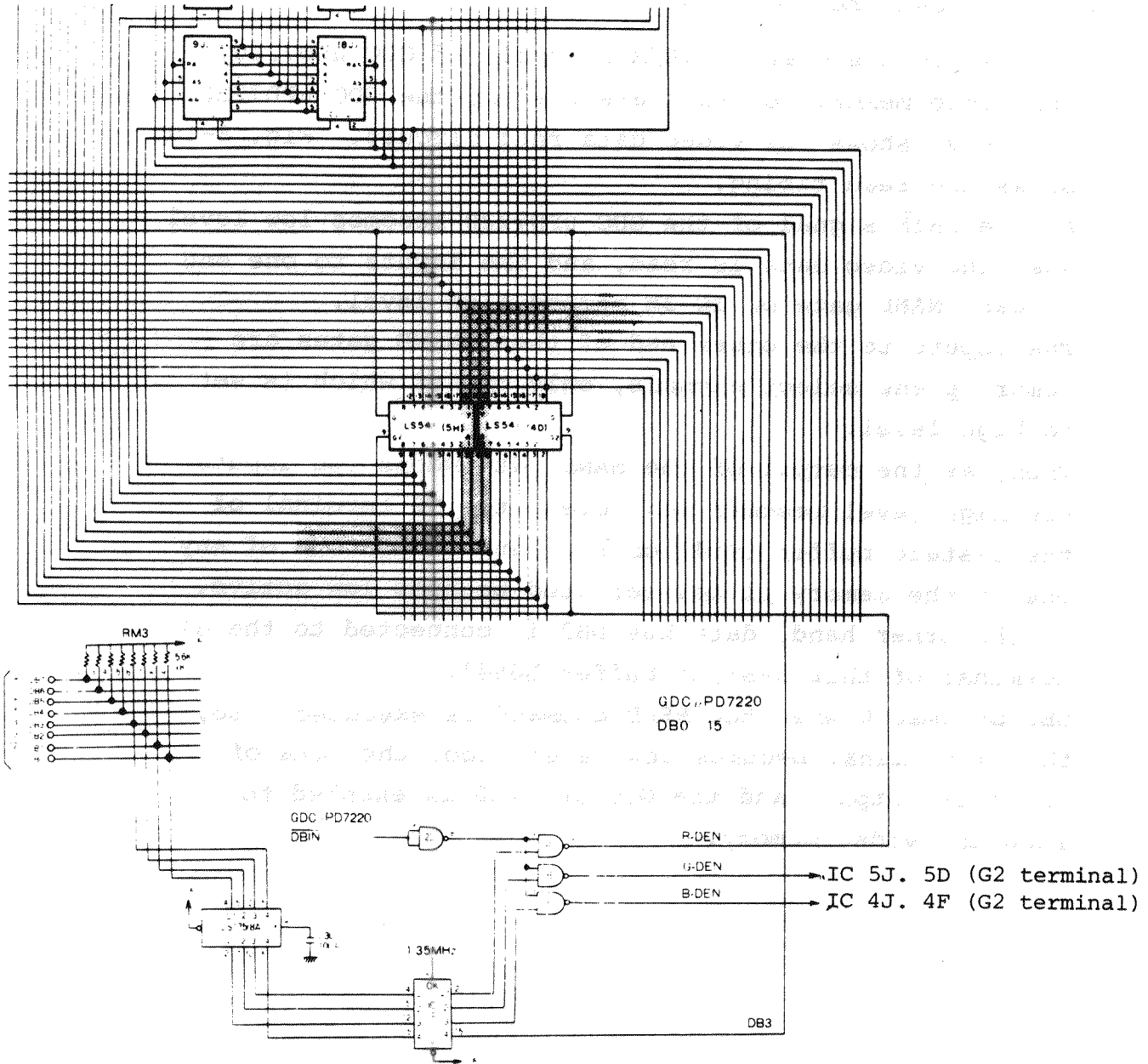


Fig. 8-9 Video data read circuit

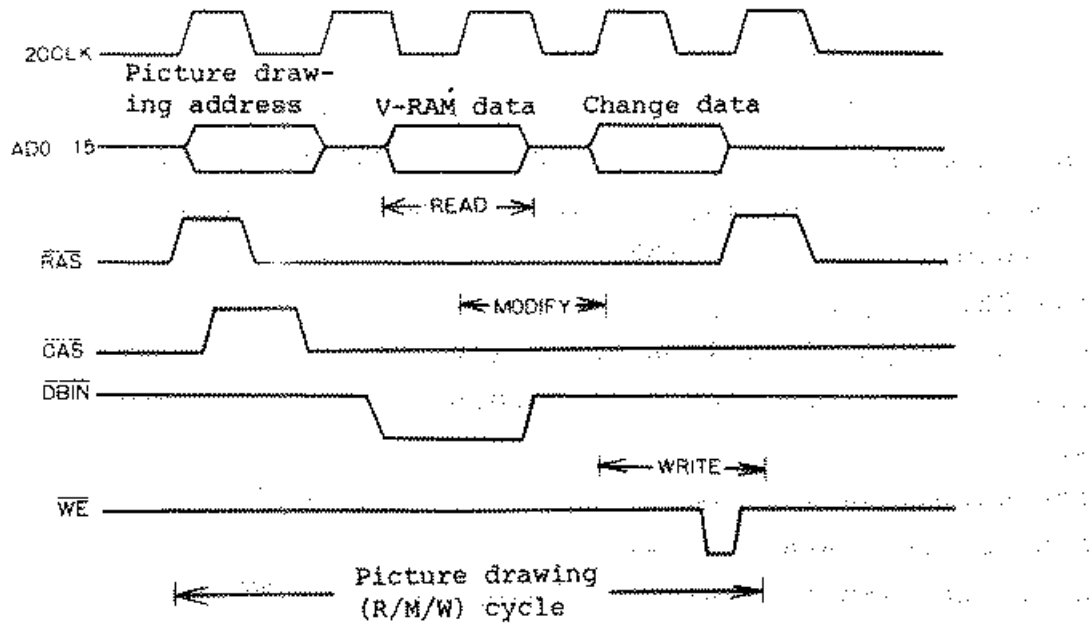


Fig. 8-10 Picture drawing (R/M/W) cycle

8.7.3 Video data write circuit

As shown in Fig. 8-10, the timing of writing data in the video memory is delayed by 2.25 clocks of 2CCLK from the trailing edge of $\overline{\text{DBIN}}$ signal. The circuit to supply this write ($\overline{\text{WE}}$) signal is shown in Fig. 8-11. The $\overline{\text{DBIN}}$ signal output from the GDC μPD7220 is coupled to the D-type flip-flop LS175 (1B) having 2CCLK as a clock, where the signal is delayed by 2 clocks of 2CCLK.

The output is applied to the next stage J-K flip ALS112 (3B), where it is further delayed by 1/4 clock of 2CCLK, and the output is supplied as a $\overline{\text{WE}}$ signal.

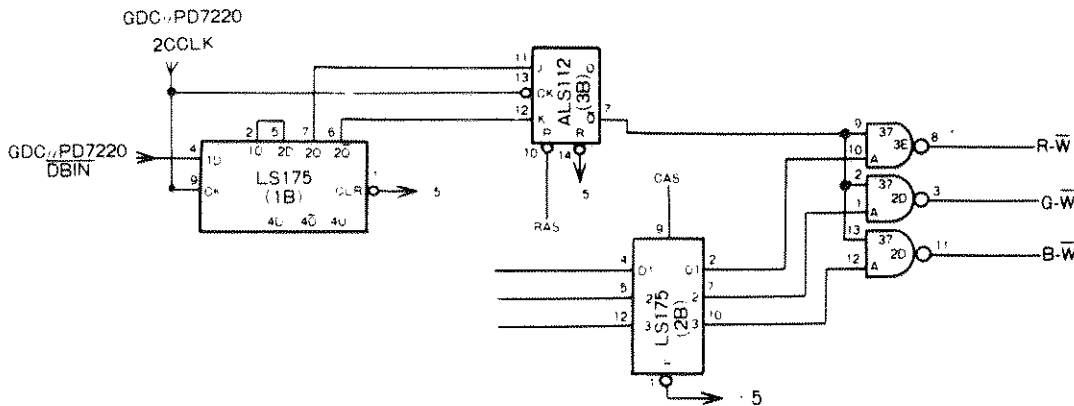


Fig. 8-11 Video data write circuit

8.8 Video data output circuit

When a display address is supplied to the video memory during the display cycle of the GDC μ PD7220, the display data is output from the video memory onto the address data bus line.

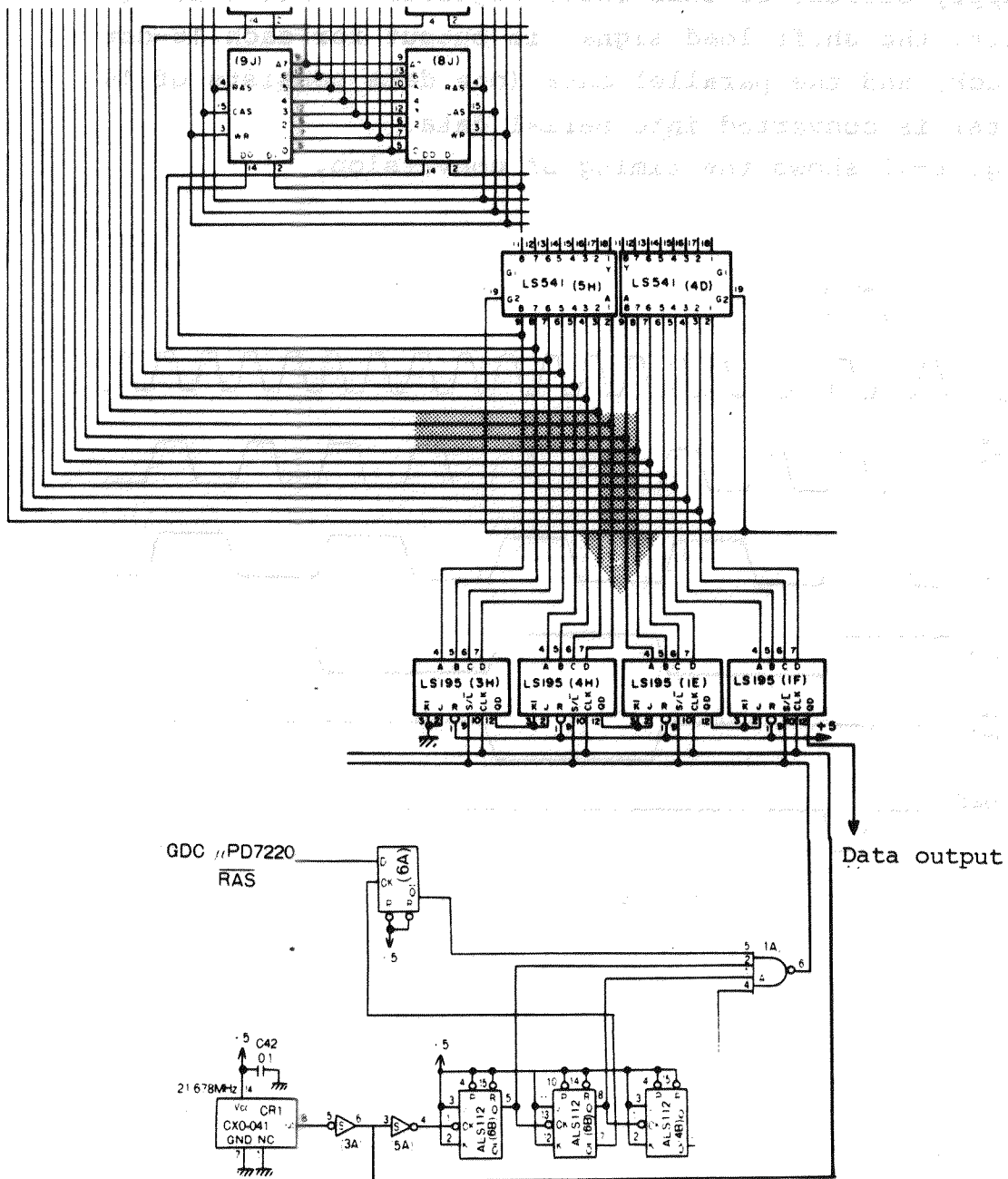


Fig. 8-12 Shift load signal supply circuit

For displaying these parallel data on the CRT, it is necessary to convert them into serial data. The shift register LS195 is inserted onto the address data bus line to make parallel-to-serial conversion of the video data.

The circuit shown in Fig. 8-12 is the shift load signal supply circuit of this shift register. With this circuit, the shift load signal is output for each 16-dot clock, and the parallel data (one data consists of 16 bits) is converted into serial data.

Fig. 8-13 shows the timing of conversion.

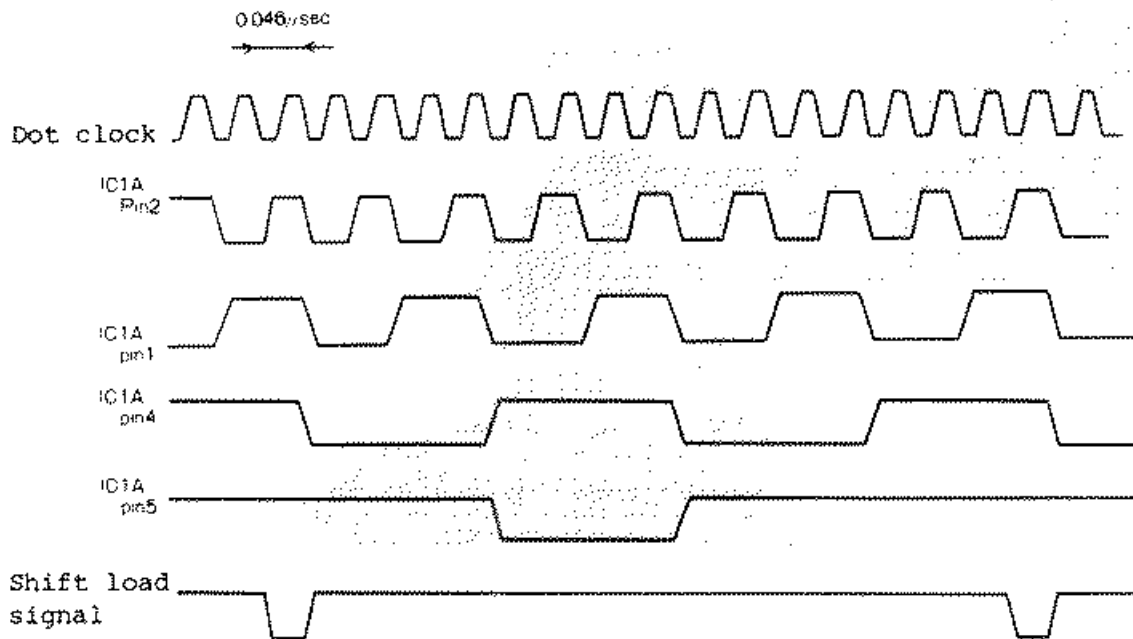


Fig. 8-13

8.9 Video signal conversion circuit

The video data output from the shift register of each memory plane is applied to the D-type flip-flop ALS574 (3A).

The ALS574 (3A) uses 21.679 MHz as a clock, which provides a dot clock of video data. On the other hand, the signal indicating the blanking period is generated from the $\overline{\text{BLANK}}$ signal terminal of the GDC μPD7220 . As shown in Fig. 8-14, this $\overline{\text{BLANK}}$ signal is ANDed with the data of each memory plane, disabling display during the blanking period.

The video data is finally transmitted via the transistor (2SC1384) driven with +5 V and output to the color monitor as an NRZ (Non-Return to Zero) signal of TTL level.

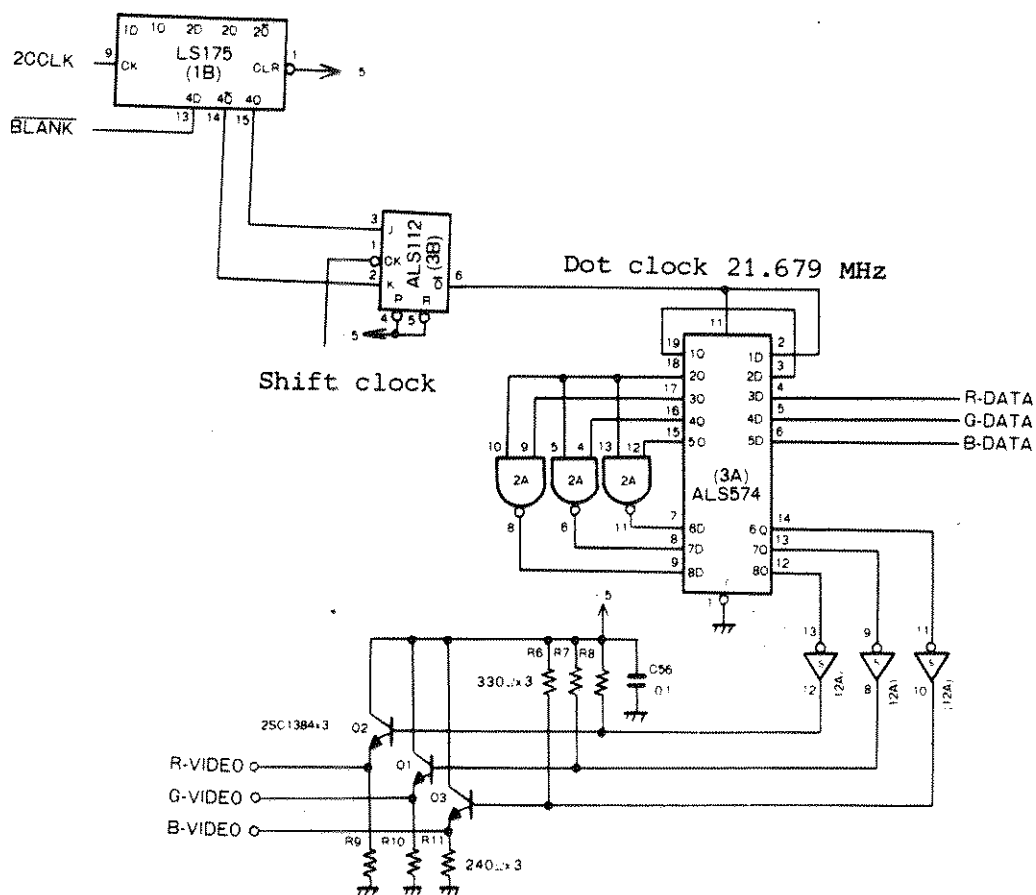


Fig. 8-14