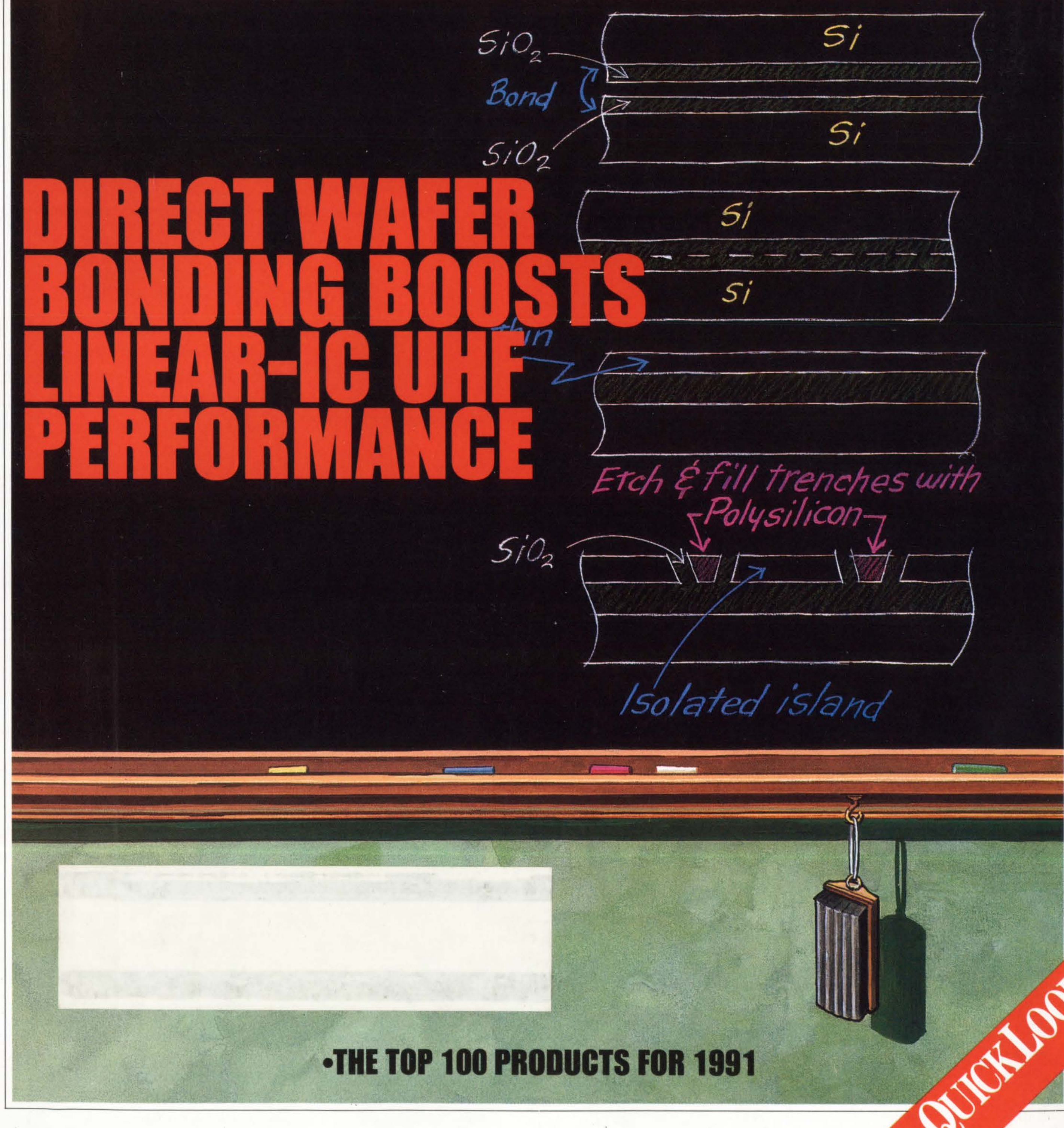
CREATE VHDL TEST BENCHES TO VERIFY DESIGNS

OPTOELECTRONIC SENSOR CUTS SYSTEM COSTS

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

ELECTRONIC DESIGN®

A PENTON PUBLICATION U. S. $10.00 DECEMBER 19, 1991

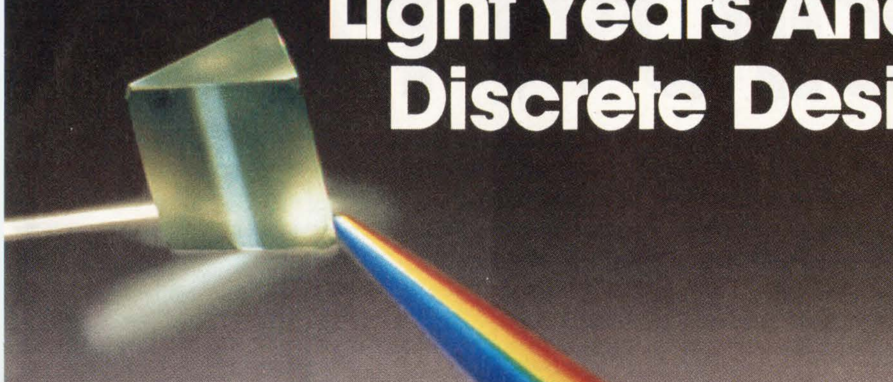


DIRECT WAFER BONDING BOOSTS LINEAR-IC UHF PERFORMANCE

•THE TOP 100 PRODUCTS FOR 1991

QUICKLOOK

New Switched Integrator IC Light Years Ahead of Discrete Designs!



Unique IC Beats Discrete Designs

When you need to convert low-level current signals to precision voltage outputs, try our unique ACF2101dual switched integrator. It's the only complete IC solution on the market, with ***Difet***® op amps, 100pF capacitors, HOLD and RESET switches, and output multiplexers on a single chip.

ACF2101 eliminates problems often encountered with discrete integrator circuits, including leakage current errors, noise pickup, and charge injection. The resulting performance is several magnitudes better than discretes, plus it saves on board space and requires fewer parts!

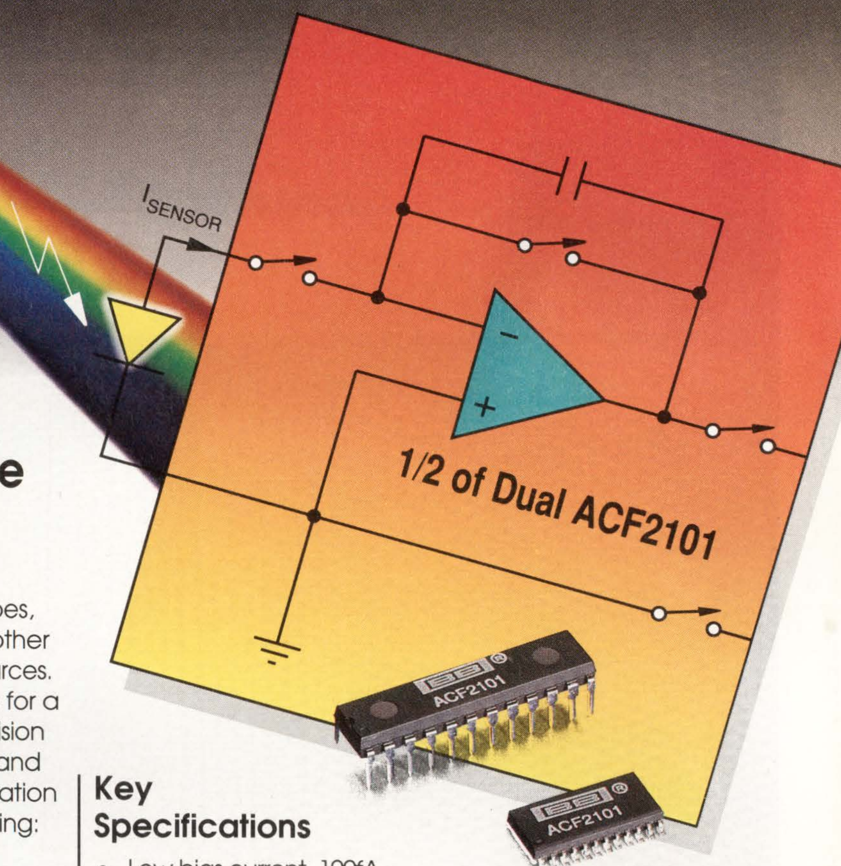
* USA OEM prices only

Difet® Burr-Brown Corp.

Direct Photodiode Interface

ACF2101 interfaces directly to phototubes, photodiodes, and other low-level current sources. It's your best choice for a wide range of precision medical, scientific, and industrial instrumentation applications, including:

- Airport luggage scanners
- Blood gas analyzers
- Chemical analyzers
- CT scanners
- Digital X-ray equipment
- Electrometers
- Nuclear particle detectors
- Pulse oximeters



Key Specifications

- Low bias current, 100fA
- Low noise, 10μVrms
- Wide dynamic range, 120dB
- Low charge transfer, 0.1pC
- ≤100μA inputs
- Two complete integrators
- –40/+85°C
- $18* in 100s

Free Samples Fast

Contact your local Burr-Brown sales representative for evaluation samples and data sheets, or call **1-800-548-6132** for immediate assistance.

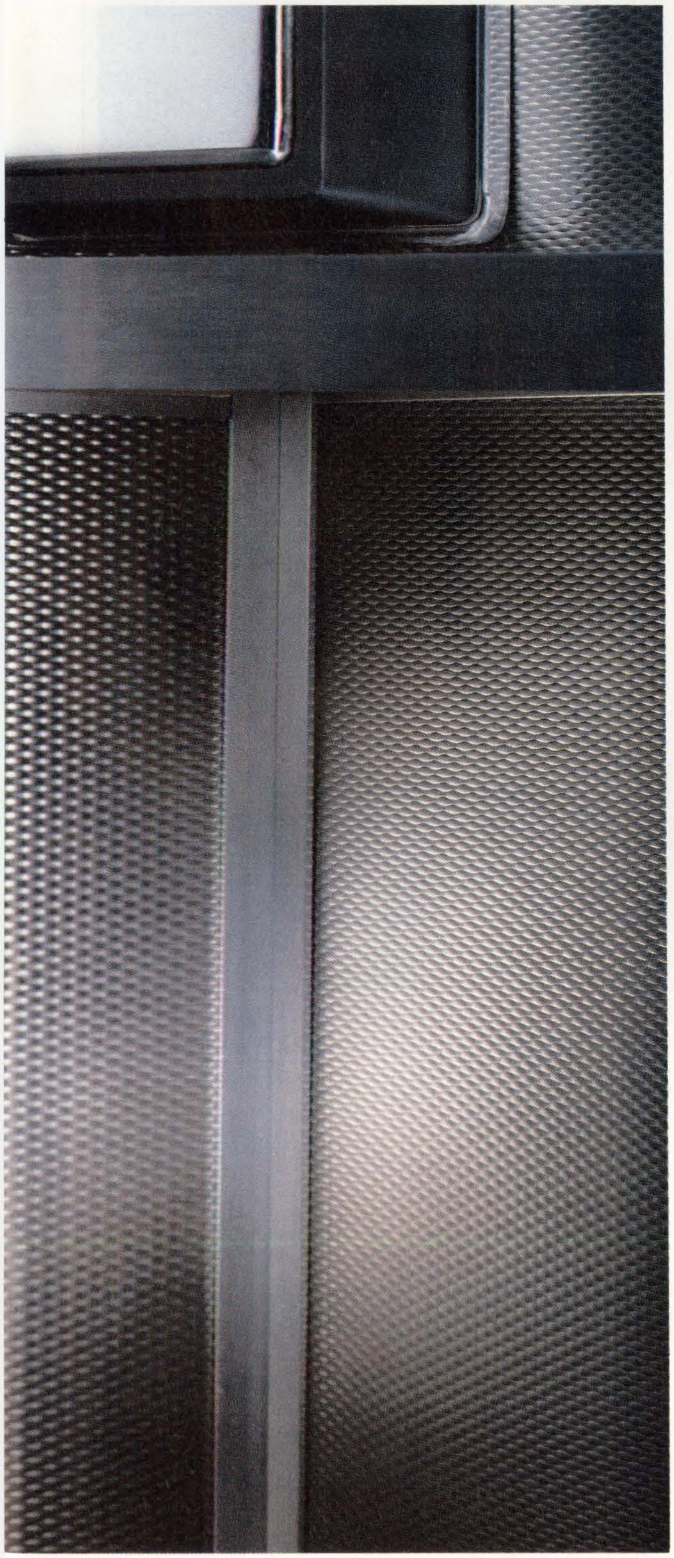
Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734

BURR-BROWN®

CIRCLE 182 FOR U.S. RESPONSE CIRCLE 183 FOR RESPONSE OUTSIDE THE U.S.

The Yellow Page

s Of CMOS PLDs.



Let your fingers do the you-know-what through our PLD databook, and see what we mean. In it you'll find everything you'll ever need in a CMOS PLD. Available now and in quantity from AMD.

Which shouldn't surprise you, coming from the undisputed leader in programmable logic. After all, we invented the PAL® device and the 22V10, and established them as industry standards in programmable logic. In fact, we sell more programmable logic devices than all of our competitors combined.

What's more, we offer the widest variety of CMOS PLDs of any vendor. Everything from our high speed, high density MACH™ Family, to low density commodity parts. Even PLDs for specialized applications.

All of which are supported by the design, test, and programming tools you're already familiar with, through our FusionPLD℠ program.

Our new Submicron Development Center in Sunnyvale represents our commitment to innovation and performance in CMOS technology. That's where we continue to develop CMOS PLDs with the highest systems performance.

In short, everything from A to Z in CMOS PLDs is always right at your fingertips. So reach for your AMD databook, and place an order today. Or call **1-800-222-9323** for more information.

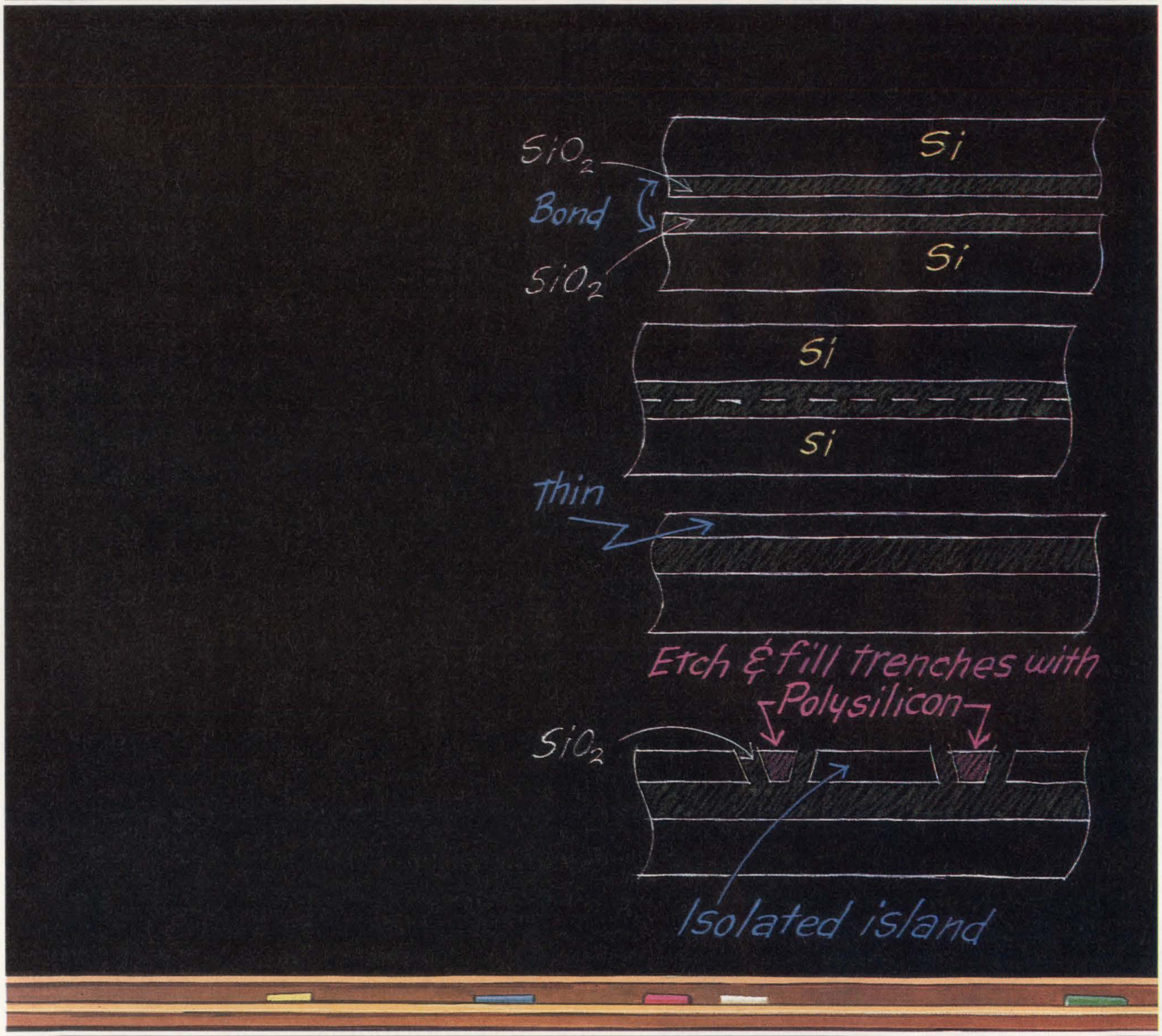
Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088

CIRCLE 84 FOR U.S. RESPONSE **CIRCLE 85 FOR RESPONSE OUTSIDE THE U.S.**

DECEMBER 19, 1991 VOL. 39, NO. 24

ELECTRONIC DESIGN



Jesse H. Neal Editorial Achievement Awards:
1967 First Place Award
1968 First Place Award
1972 Certificate of Merit
1975 Two Certificates of Merit
1976 Certificate of Merit
1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
1989 Certificate of Merit

COMING NEXT ISSUE
- Special Report: 1992 Technology Forecast
- Exploring the foundations of future technology advances in:
  - Digital semiconductors
  - Analog, power, and mixed-signal semiconductors
  - Optoelectronic devices and systems
  - Multichip packaging
- Networks' key role in concurrent engineering
- Assessing the impact of multichip-module design automation
- Future developments in:
  - CISC and RISC microprocessors
  - Magneto-optical disk drives
  - Computer boards
  - Power supplies
  - Passive components
  - Displays
  - Test probes
  - Electromagnetic interference
  - Instrument accuracy
  - Micromachined devices
- PLUS:

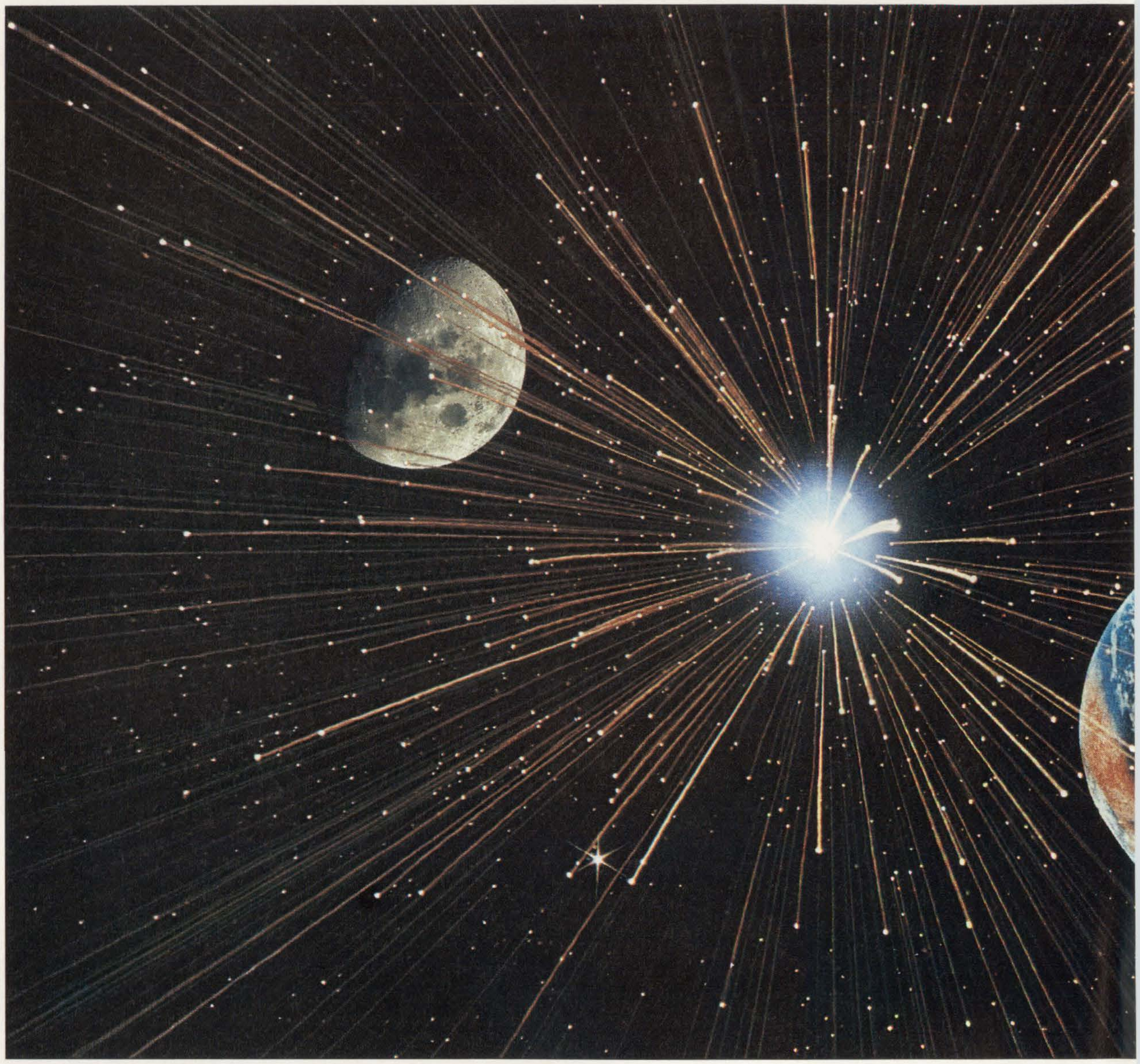
Ideas for Design
Pease Porridge
Technology Advances
QuickLook

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi monthly by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $85 U.S., $160 Canada, $230 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204.

For subscriber change of address and subscription inquiries, call (216) 696-7000.

POSTMASTER: Please send change of address to ELECTRONIC DESIGN, Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543.

Challenging the limits of is the core of our success.



For NCR, it's defined by the very things that drive our industry. The changing technology that is the core of what we do. And people who join you in a partnership and provide service that actually exceeds customer expectation.

Because our designers avidly pursue new ideas, they can help make the complex a bit simpler.

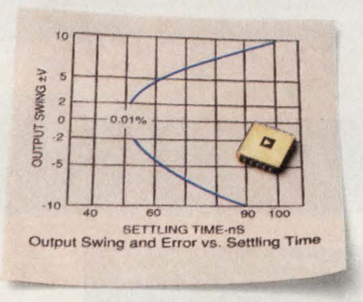
And when your challenge is to design a system that goes beyond known boundaries – they will provide myriad resources to help you push that design to the limit.

Those resources include industry-leading products like mixed-signal ASICs, Ethernet and SCSI, already considered standards. Or, when your latest design requires a custom solution, these products become the cores for unique devices – providing ever-increasing levels of integration in ever-decreasing space. Moreover, because you can design systems at higher levels of abstraction… you're free to explore a universe of limitless applications… and still save time, money and reduce the

North American Sales Headquarters
1731 Technology Drive, Suite 600
San Jose, California 95110
1-800-334-5454

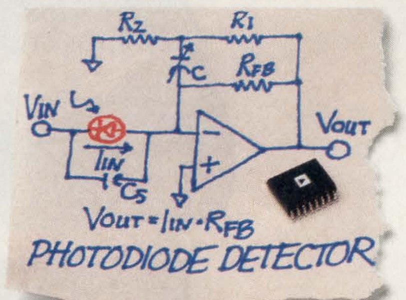
European Sales Headquarters
Westendstrasse 193
8000 Munchen 21
Germany
48-89-57931-199

Whether you fax it, fire it, send it, measure it, wire it, compute it, The Analog family of



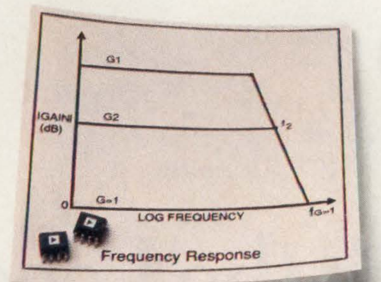
Precision

With the AD840, AD841 and AD842, there's no need to trade speed for accuracy. All three settle to 0.01% within 100 ns (840/842) and 110 ns (841) – critical in data acquisition and instrumentation applications – and offer low offset voltages and drifts, and fast slew rates.



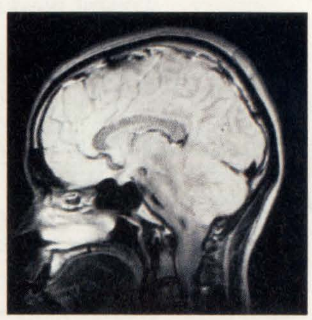
FET Input

For op amps requiring low input current, the OP-42, OP-44, AD845 and AD843 are all remarkably fast – slew rates are 58, 120, 100 and 250 V/μs, respectively. In addition, they offer offset voltages of less than 1 mV and extremely low current noise.



Transimpedance Amplifiers

The OP-160, OP-260, AD844, AD846, AD9617 and AD9618 all utilize a current feedback architecture to achieve slew rates from 450 to 2000 V/μs without compromising stability – even in hostile environments. Other benefits include low power dissipation and high unity-gain bandwidth.

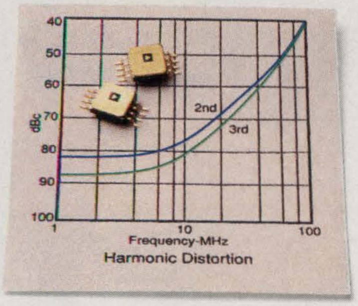


If whatever it is you're trying to do involves high-speed op amps, Analog Devices is the company to call. With our current products and new introductions, we have the broadest line of high-speed op amps available. A line that gives you the right combination of speed, precision, noise and price. So chances are, we've got exactly what you need for

Authorized North American Distributors: *Alliance Electronics* 505-292-3360 · *Allied Electronics* 817-595-3500 · *Anthem Electronics* 408-453-1200 · *BBD Electronics, Inc.* 416-821-7800 · *Bell Industries*

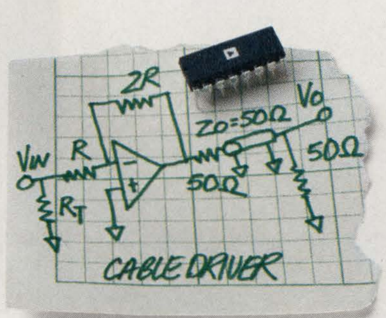
shoot it, launch it, land it, test it, display it or air it, we've got it.

high-speed op amps.



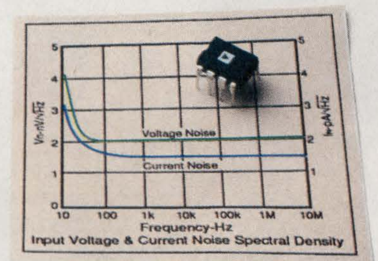
Buffers

If you're looking for extremely low distortion buffers, look at the specs of the AD9620 and AD9630 – distortion at 20 MHz: − 73 dBc and − 66 dBc, respectively; fast settling time: less than 8ns to 0.02%; and extremely low noise: 2.2 nV/$\sqrt{\text{Hz}}$.



General Purpose

With the right combination of speed, precision, power dissipation and high output drive capability, the AD827, AD829, AD847, AD848, AD849 and OP-64 are ideal general purpose solutions. And they're ideally priced solutions – most singles are under $3, and duals are under $5.



Low Noise

It used to be you had to choose between speed or low noise. But with the AD829, you get both. It features voltage noise of 2 nV/$\sqrt{\text{Hz}}$ and current noise of 1.5 pA/$\sqrt{\text{Hz}}$ with a 50 MHz unity-gain bandwidth. Those specs, combined with the low price of $2.95/100s, make it ideal for both audio and video applications.

whatever application you're working in. Call us at 1-800-262-5643, or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106, for a complete high-speed op amp selection guide and a *free copy of our SPICE model library.*

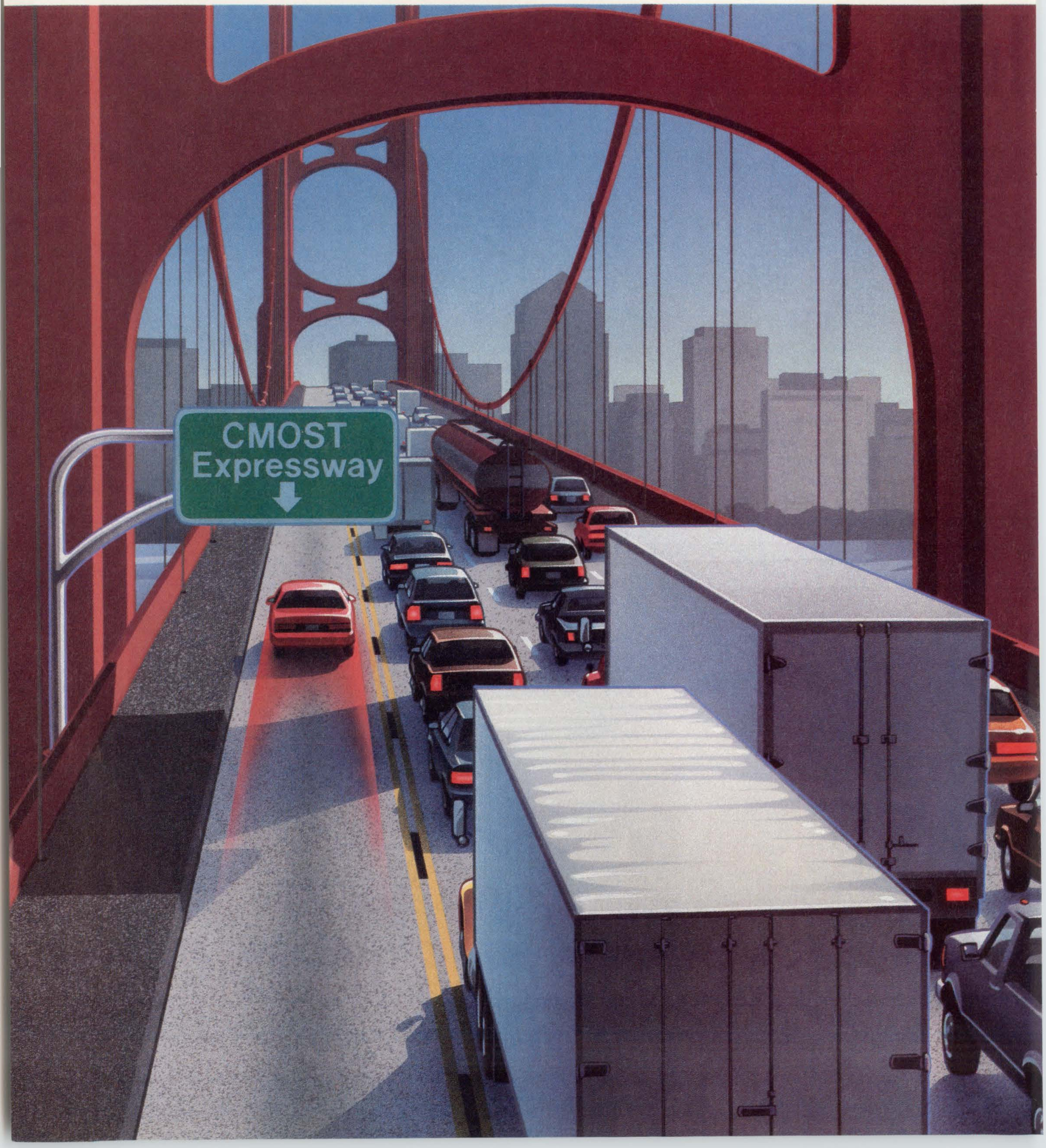
ANALOG DEVICES

Analog Devices, One Technology Way, Norwood, MA 02062-9106. Distribution, offices and applications support available worldwide.

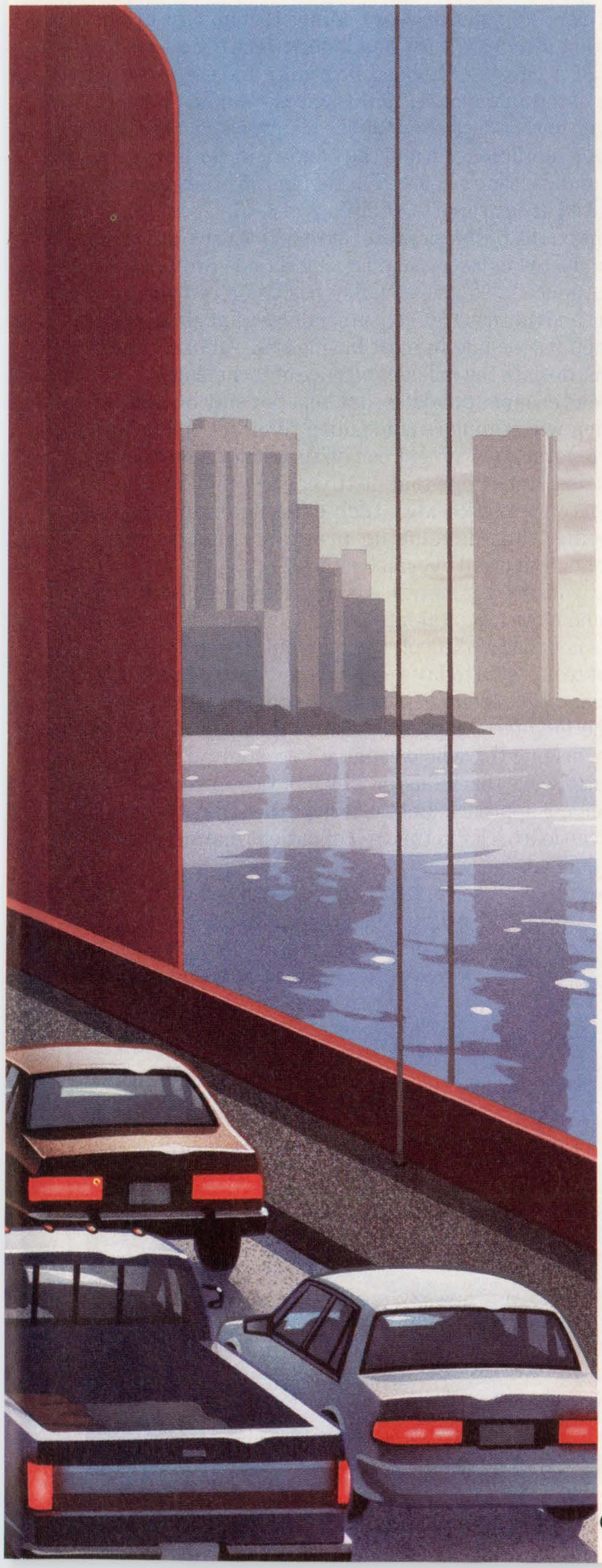
213-826-6778 • *Future Electronics* 514-694-7710 • *Hall-Mark Electronics* 214-343-5000 • *Newark Electronics* 312-784-5100 • *Pioneer Standard* 216-587-3600 • *Pioneer Technologies Group* 1-800-227-1693

CIRCLE 88 FOR U.S. RESPONSE **CIRCLE 89 FOR RESPONSE OUTSIDE THE U.S.**

Toshiba SRAMs Move Yo



u Into The Fastest Lane.



BiCMOS technology shifts our speedy, powerful SRAMs into high gear. Who'd have thought you could speed past your competitors' designs at 10-12ns access times? Toshiba, of course. Our new, faster SRAMs are helping the latest generation of high performance applications get a quick start. The range of uses for these parts include 32-bit workstations, fast cache, buffer memory and telecommunications. You can probably add a few ideas of your own.

We at Toshiba are fond of establishing new speed limits.

Toshiba's CMOS-based SRAMs are no slouches, either. Our new 1Mb, 15ns SRAM is more than 25% quicker than anyone else's. It's available in a x16 configuration to fit into today's wider applications. The revolutionary pinout has been used to reduce wire lengths and cut noise. And it's based on the same 0.7 micron process as our 4Mb DRAM, so it will be following another established leader on Toshiba's CMOST Expressway.

Now, we wouldn't want you to think there are just a few densities and organizations to choose from. You can also light a fire under your design with 10ns 256K BiCMOS, or 10ns 64K BiCMOS organized in x4 or x8. You choose. And ultimately, you win.

Of course, if your design doesn't require such breathtaking speed, Toshiba also offers 1Mb SRAMs at 80-100ns, or Pseudo Static RAM up to 4Mb.

When you're ready to really get moving on your next design, call Toshiba.

Toshiba CMOS keeps any project running smoothly.

For technical literature, call 1-800-321-1718.

In Touch with Tomorrow

TOSHIBA

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

MST-90-047

CIRCLE 166 FOR U.S. RESPONSE   CIRCLE 167 FOR RESPONSE OUTSIDE THE U.S.

EDITORIAL

HERE'S TO A BETTER 1992

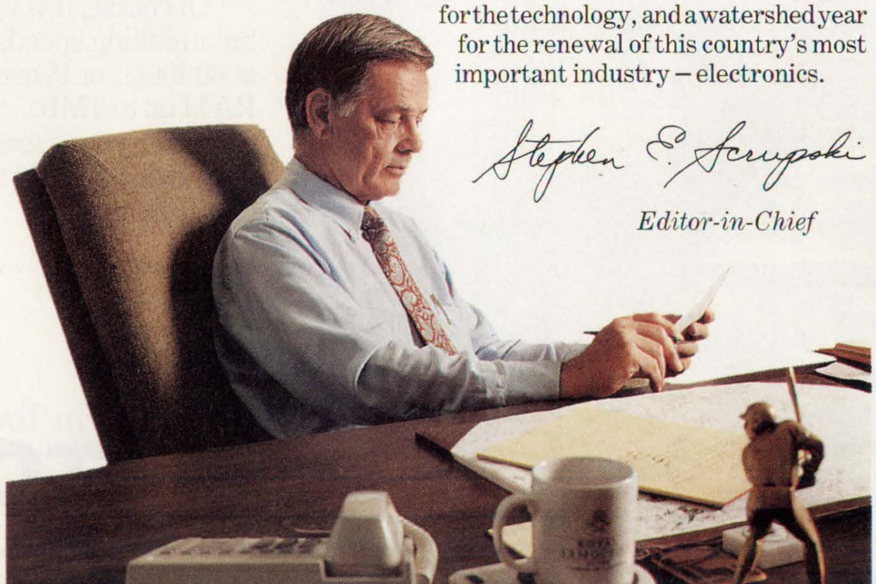
Looking back on 1991, technology continued to exhibit outstanding gains in all areas. This issue contains our annual look at the top 100 products covered by Electronic Design this year (selected from the 1000-plus covered throughout the year). Many technology breakthroughs are included on this list. Among the top headliners were the all-analog memory device from Information Storage Devices, introduced to the industry on Electronic Design's cover of the January 31, 1991 issue; the Analog Devices accelerometer IC on the cover of the August 8, 1991 issue; the Star Semiconductor DSP chip of the October 10, 1991 issue; and the bonded-wafer linear ICs from Harris Semiconductor on this issue's cover. These, plus 96 other groundbreaking products, are revisited in our report beginning on p. 47.

This past year, though, gains on the business side of electronics were anything but outstanding. The semiconductor industry seldom saw its book-to-bill ratio break through the 1.00 level; reduced defense spending has triggered waves of layoffs; general unemployment and the resulting consumer uncertainty in all types of purchases has undercut capital spending in most businesses. All in all, there aren't many encouraging signs, despite the quickening pace of technology.

In the face of such widespread economic malaise, our best bet may be that the upcoming presidential election will stimulate some deep thinking inside both political parties on what the federal government can do to kickstart our struggling high-technology industries. Let's hope that next year's presidential candidates recognize the importance of the high-tech establishment to this country's economic well-being, thus developing programs that set up a framework for growth in productivity and overall business.

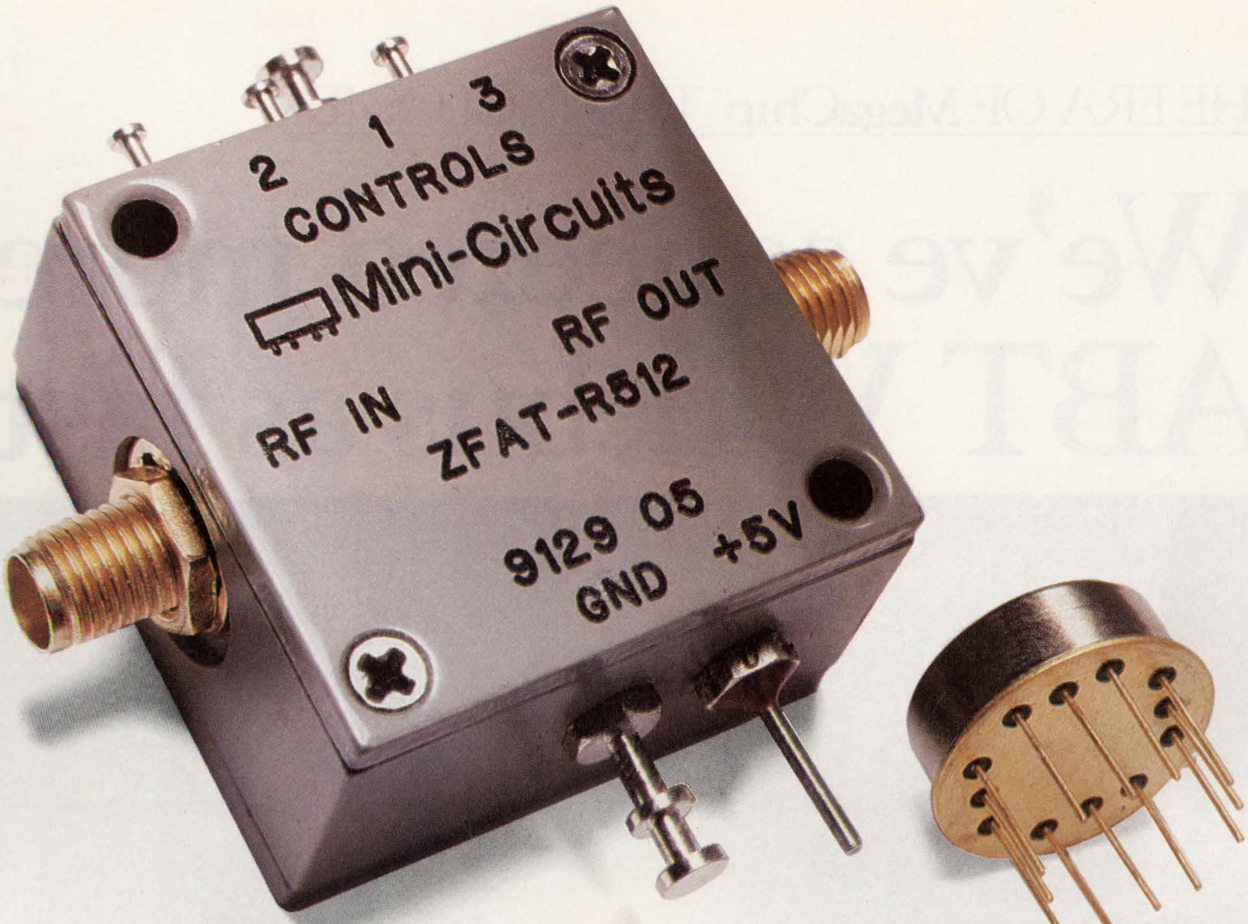
The capital-gains-tax issue will surely generate some heated discussion. The electronics industry is more and more a capital-intensive business, for design as well as for manufacturing. It's not all that difficult to figure out: If you want productivity increases, you've got to invest in today's – and tomorrow's – productivity-enhancing tools. And the federal government must act to stimulate such capital investment. However, it's the *long-term* capital investors that will make this industry a potent force again, driving the whole country's economy. The quick-buck decade of the 1980s did not serve this industry well, nor does a short-term, quarterly bottom-line management approach. Let's also hope those days are over; the U.S. electronics industry can learn a lot in the area of patient market growth from its counterparts in Asia and Europe.

With the right tools and incentives in place, 1992 can be another banner year for the technology, and a watershed year for the renewal of this country's most important industry – electronics.



Stephen E. Scrupski

Editor-in-Chief



PRECISION TTL-CONTROLLED ATTENUATORS

up to 35dB
10 to 1000MHz

FROM **$59⁹⁵**

TOAT-R512 ZFAT-R512 Accuracy		TOAT-124 ZFAT-124 Accuracy		TOAT-3610 ZFAT-3610 Accuracy		TOAT-51020 ZFAT-51020 Accuracy	
(dB)	(+/-dB)	(dB)	(+/-dB)	(dB)	(+/-dB)	(dB)	(+/-dB)
0.5	**0.12**	**1.0**	**0.2**	**3.0**	**0.3**	**5.0**	**0.3**
1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

Price $ (1-9 qty) TOAT $59.95/ZFAT $89.95
bold faced values are individual elements in the units

Finally...precision attenuation accurate over 10 to 1000MHz and -55°C to +100°C. Standard and custom models are available in the TOAT(pin)- and ZFAT(SMA)-series, each with 3 discrete attenuators switchable to provide 7 discrete and accurate attenuation levels.

The 50-ohm components perform with 6μsec switching speed and can handle power levels typically to +10dBm. Rugged hermetically-sealed TO-8 units and SMA connector versions can withstand the strenuous shock, vibration, and temperature stresses of MIL requirements. TOAT pin models are priced at only $59.95 (1-9 qty); ZFAT SMA versions are $89.95 (1-9 qty).

Take advantage of this striking price/performance breakthrough to stimulate new applications as you implement present designs and plan future systems. All units are available for immediate delivery, with a one-yr. guarantee, and three-sigma unit-to-unit repeatability.

finding new ways...
setting higher standards

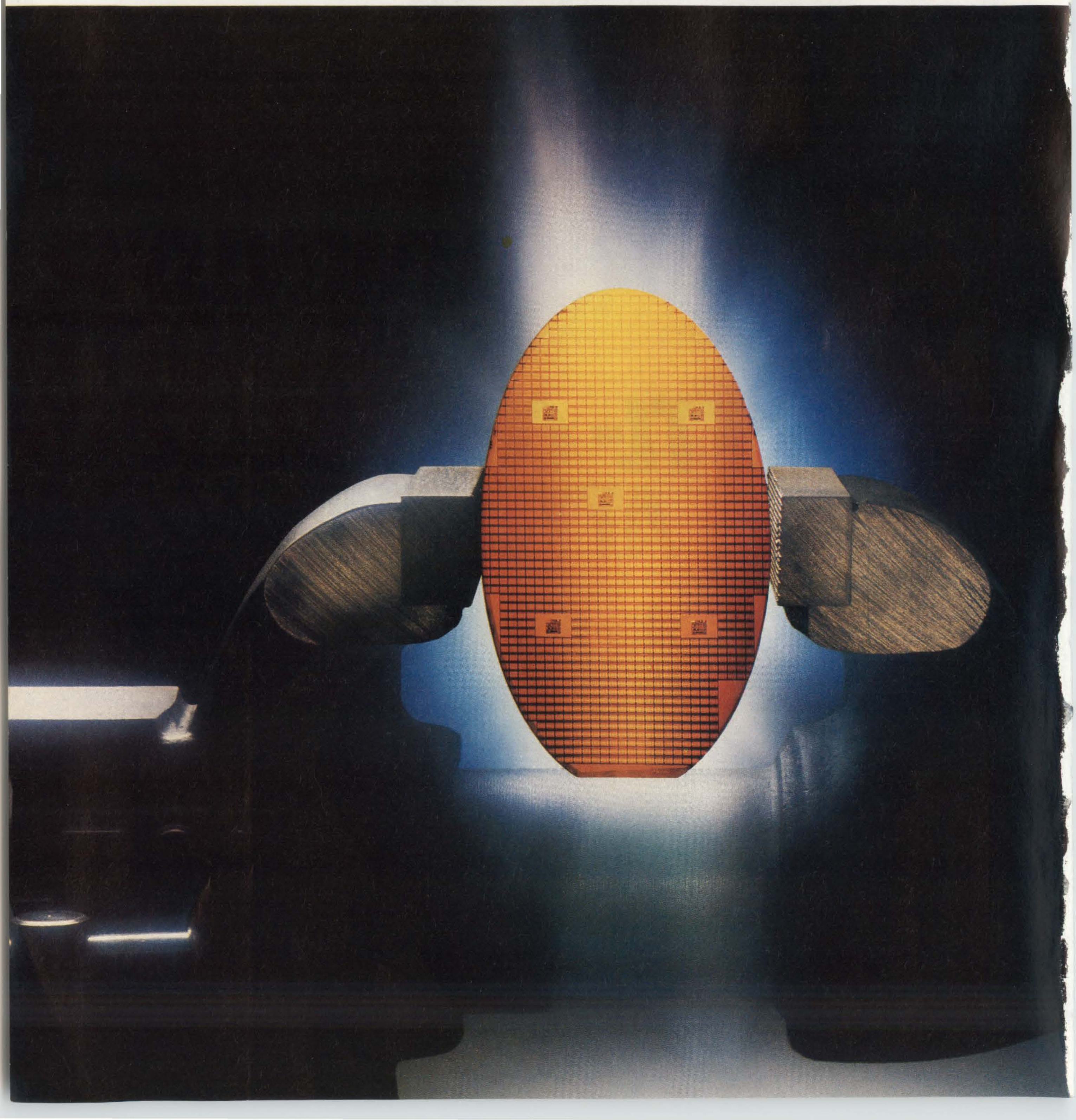
Mini-Circuits WE ACCEPT AMERICAN EXPRESS AND VISA

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

CIRCLE 130 FOR U.S. RESPONSE **CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.** F 140 REV. A

IN THE ERA OF MegaChip™ TECHNOLOGIES

We've squeezed more ABT Widebus as fast



speed from our logic. as 4.1 ns!

With our new Advanced BiCMOS interface logic (ABT) family, you get the speed, drive and low power you need to optimize the performance of processors operating at 33 MHz and above.

Fabricated in our 0.8-micron BiCMOS process, this new family delivers maximum speeds down to 4.1 ns over recommended operating conditions. Typical performance of the devices is in the 2.5- to 3.0-ns range.

Other critical performance parameters are as impressive. Drive capability is 32 to 64 mA. Static power consumption is typically 2 mA (I_{CCH}, I_{CCZ}) and 30 mA (I_{CCL}). Ground bounce is less than 800 mV typ.

All this in Widebus

Our ABT family, a second-generation advance of our leadership BiCMOS (BCT) family, includes versions of our 16-, 18- and 20-bit-width Widebus™ functions.

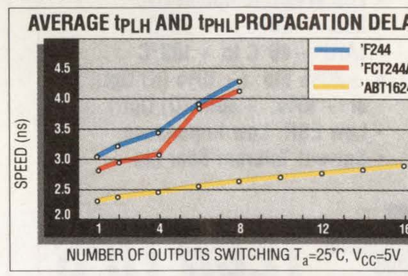
Among the many ABT Widebus functions released is the 'ABT16244, a 16-bit buffer and line driver. It exhibits much greater stability of propagation delay *(see chart)*, which results in a lower derating factor across the number of outputs switched.

Also in volume production are the Widebus 'ABT16245 16-bit bidirectional bus transceiver and the 'ABT16543 and 'ABT16952 16-bit bidirectional registered bus transceivers.

As in our successful Advanced CMOS Logic (ACL) Widebus family, these devices come in our leadership surface-mount shrink small-outline package (SSOP) that gives you twice the number of I/Os as a standard small-outline package in the same space.

Unique additions included

There are also new devices in our ABT Widebus family featuring greater density and functionality. Our 'ABT16500A is a good example. An 18-bit registered transceiver, it combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.



TI's speed advantage: *In a one-to-one comparison, a TI 'ABT16244 16-bit Advanced BiCMOS driver proves to be much faster and more stable than Advanced Bipolar and standard CMOS octal drivers.*

To complement our full line of Widebus products, our ABT family will include at least 39 octal buffers/drivers, flip-flops, transceivers and registered transceivers.

Squeeze more out of your system with a free sample 'ABT16500A: Call 1-800-336-5236, ext. 3009

To learn firsthand how our new ABT family can boost the performance of your bus-interface designs, get a free 'ABT16500A transceiver and data sheet. Just complete and mail the return card or call the number above.

TEXAS INSTRUMENTS

08-1139

TRACKING TRENDS IN T&M

The end of the year is always a good time to sit down and reflect. In the electronics test and measurement area, this year-end introspection uncovers two trends. One involves the VXIbus backplane and how it's being used, perhaps in a different way than some people had expected. The other concerns the impact Windows 3.0 is having on test and measurement.

JOHN NOVELLINO
TEST & MEASUREMENT

When VXIbus was introduced about four years ago, some people saw it as an eventual replacement for IEEE-488 rack-and-stack instruments. The comparison was inevitable. Here was a standard that allowed you to buy instruments-on-a-card from different manufacturers and integrate them in a high-performance test system. The standard was also designed for computer control; the modules themselves had no front panels. Moreover, the size and weight advantages over IEEE-488 devices were significant, as were the performance increases. But VXIbus hasn't replaced IEEE-488 and probably won't in the near future.

The problem is that VXIbus instruments are still somewhat expensive. A test engineer must have a serious need for the size, weight, and performance advantages of VXI to justify switching to the new standard. And integrating a VXIbus system isn't an easy task.

As a result, the use of VXIbus instruments by engineers who develop their own test systems seems to be growing slower than initially predicted. However, VXIbus seems to be thriving in another area: automatic test equipment. In recent months, at least five ATE manufacturers – GenRad, Giordano Associates, Hewlett-Packard, Hilevel, and Schlumberger – have introduced VXI-based systems to test various devices and boards. The match seems to be ideal. The VXIbus offers not only high performance but also flexibility. OEMs can create high-performance testers whose configurations can readily be customized for specific applications and upgraded as a user's needs change.

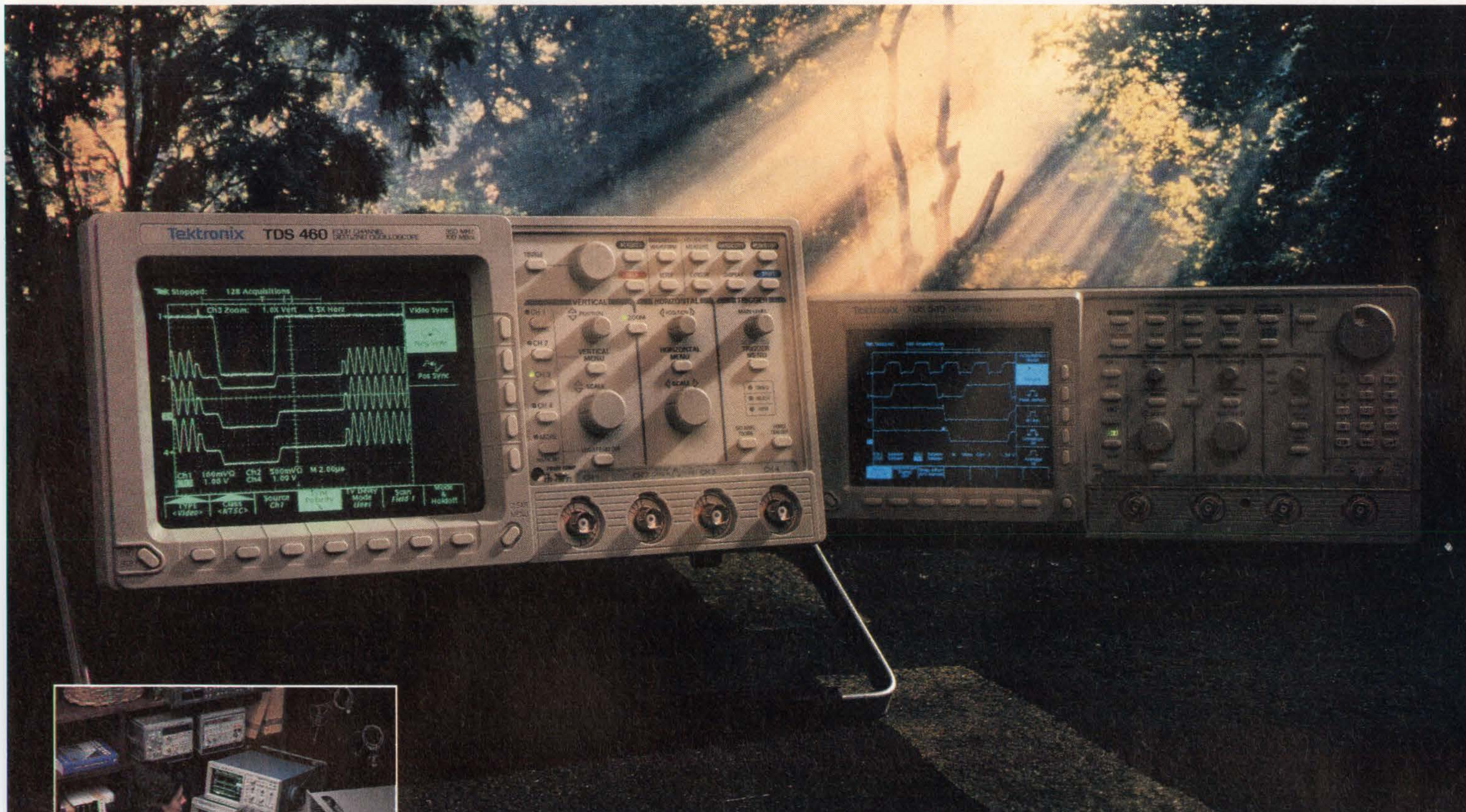
Another important trend in test and measurement is the increasing use of Microsoft Windows-based user interfaces to program and execute tests. Software is an integral part of any new test system. Today, it sometimes seems that there are as many software products aimed at test applications being introduced as there are hardware products. In particular, many manufacturers are incorporating Windows 3.0 into their systems. The software offers some features that may change the way measurements are made and analyzed.

Teradyne recently added a Windows 3.0 graphical user interface to the Victory 2.0 boundary-scan test software. Fluke's Hydra Data Logger applications software can now be used with Windows 3.0. Last month, IOtech and National Instruments announced Windows-based drivers for their IEEE-488 data-acquisition hardware. Both drivers take the form of a dynamic link library, a standard method for integrating a library into a Windows 3.0 application or end-user program. Additional products are scheduled for introduction within the next several weeks.

The dynamic link library and the dynamic data exchange features of Windows 3.0 will change the way engineers perform test and measurement tasks. With these functions, users can share data among different Windows packages, enhancing Windows' multifunction capability. Users can easily cut and paste code from one program to another and quickly transfer acquired data into popular spreadsheet programs or other software for analysis. In addition, the new Visual Basic and C for Windows languages make it much easier to write programs in Windows.

As more Windows-based measurement software in introduced, test programming and analysis will become a modular process. Rather than being tied down to one large acquisition package and one analysis package, engineers will be able to select modules that fill specific needs and quickly build a custom test and measurement program.

Tek's new encore TDS 400. Extraordinary 4-channel power. Ordinary 2-channel price.

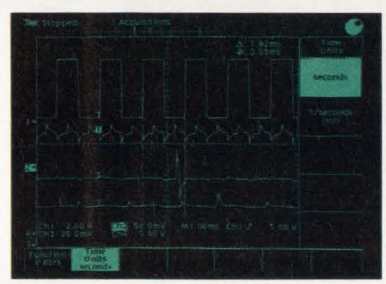


Tek's new TDS 400 Series oscilloscopes make TDS performance from 150 MHz to 350 MHz more portable and affordable than ever.

Now you can pick up where Tek's breakthrough TDS 500 Series left off — with a compact, versatile new series that puts the TDS platform's 4-channel acquisition, multiprocessing and intuitive operation within easy reach of digital, analog and electro-mechanical design, production test, field service, and many other demanding tasks.

For the usual price of *two* channels, you can now have:

- 100 MS/s sampling on each of four channels.
- On-the-fly signal processing with up to 12-bit vertical resolution.
- Record lengths to 30,000 points.
- Video trigger option with back-porch clamp and dial-up line/field selection.
- 22 time-saving automatic measurements.
- The unique graphical user interface that lets most TDS manuals stay shrink-wrapped on the shelf.



Call 1-800-426-2200 Ext. TDS4, for more information on either the new TDS 400 or the recently-announced TDS 500 Series — with up to 4 channels, 1 GS/s sampling and 500 MHz bandwidth — and for the number of your nearest Tek sales office. We'll put you through to all the right channels, fast!

CIRCLE 164 FOR U.S. RESPONSE
CIRCLE 165 FOR RESPONSE OUTSIDE THE U.S.

Tektronix
Test and Measurement

3GA-188087-0

FILTERS

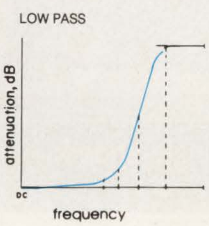
F132-1 REV. A

dc to 3GHz from $11^{45}

lowpass, highpass, bandpass

• less than 1dB insertion loss • greater than 40dB stopband rejection • surface-mount • BNC, Type N, SMA available • 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • rugged hermetically-sealed pin models • constant phase • meets MIL-STD-202 tests • over 100 off-the-shelf models • immediate delivery

low pass, Plug-in, dc to 1200MHz



Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
PLP-5	DC-5	8-10	10-200
PLP-10.7	DC-11	19-24	24-200
PLP-21.4	DC-22	32-41	41-200
PLP-30	DC-32	47-61	61-200
PLP-50	DC-48	70-90	90-200
PLP-70	DC-60	90-117	117-300
PLP-90	DC-81	121-137	167-400
PLP-100	DC-98	146-189	189-400
PLP-150	DC-140	210-300	300-600
PLP-200	DC-190	290-390	390-800

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
PLP-250	DC-225	320-400	400-1200
PLP-300	DC-270	410-550	550-1200
PLP-450	DC-400	580-750	750-1800
PLP-550	DC-520	750-920	920-2000
PLP-600	DC-680	840-1120	1120-2000
PLP-750	DC-700	1000-1300	1300-2000
PLP-800	DC-720	1080-1400	1400-2000
PLP-850	DC-760	1100-1400	1400-2000
PLP-1000	DC-900	1340-1750	1750-2000
PLP-1200	DC-1000	1620-2100	2100-2500

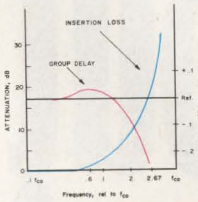
Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600
SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

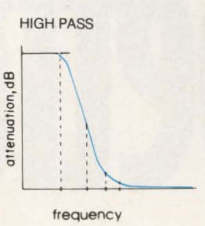
Flat Time Delay, dc to 1870MHz



Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	2fco X̄	2.67fco X̄
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

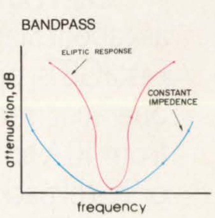
high pass, Plug-in, 27.5 to 2200MHz



Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Passband Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1
PHP-50	DC-20	20-26	41-200	1.5:1
PHP-100	DC-40	40-55	90-400	1.8:1
PHP-150	DC-70	70-95	133-600	1.8:1
PHP-175	DC-70	70-105	160-800	1.5:1
PHP-200	DC-90	90-116	185-800	1.6:1
PHP-250	DC-100	100-150	225-1200	1.3:1
PHP-300	DC-145	145-170	290-1200	1.7:1
PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70MHz



Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95, BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

finding new ways ...
setting higher standards

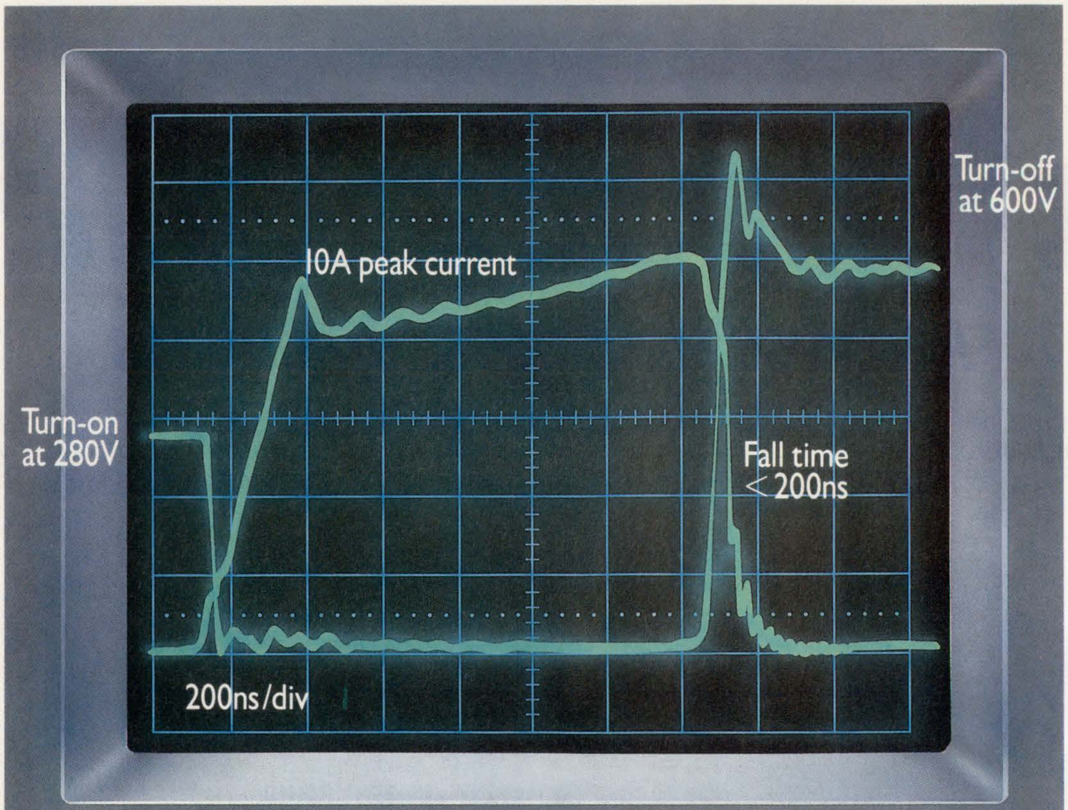
Mini-Circuits™

WE ACCEPT AMERICAN EXPRESS AND VISA

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661
Distribution Centers/NORTH AMERICA 800-654-7949 • 417-335-5935 Fax 417-335-5945 EUROPE 44-252-835094 Fax 44-252-837010

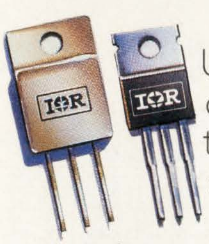
CIRCLE 128 FOR U.S. RESPONSE **CIRCLE 129 FOR RESPONSE OUTSIDE THE U.S.**

F132-2 REV. A



UltraFast IGBT IRGBC30U switching 10A in a single-ended forward converter at 50kHz.

IGBTs Without A Trace of Competition.



IR announces Ultra Fast IGBTs: our 600V power transistors that switch faster and run cooler than any you've ever used.

Forget about bipolar. Put these breakthrough devices in your high-voltage, high-current, medium-frequency applications and get performance unparalleled for the price.

Which should come as no surprise. IR IGBTs build on the same proprietary technology that made IR's HEXFETs® world leaders.

Call 1 (213) 640-6534 and ask about Standard, Fast or Ultra-Fast IGBTs, optimized for your operating frequency. And available from 10A to 70A, in commercial or hi-rel packages.

We'll be happy to arrange a screening.

IOR International Rectifier

WORLD HEADQUARTERS: 233 KANSAS ST., EL SEGUNDO, CA 90245, U.S.A. (213) 772-2000. TWX 910 348-6291, TELEX 472-0403. EUROPEAN HEADQUARTERS: HURST GREEN, OXTED, SURREY RH8 9BB, ENGLAND TELEPHONE (0883) 713215, TELEX 95219

CIRCLE 122 FOR U.S. RESPONSE   CIRCLE 123 FOR RESPONSE OUTSIDE THE U.S.

SUPERCOMPUTER SMASHES ALL SPEED RECORDS

By combining 16 CPUs, the Y-MP C90 supercomputer from Cray Research Inc., Eagan, Minn., operates at four times the speed of the company's previously fastest system. The company says that its parallel-vector system is now the industry's fastest. Each CPU has four double-width memory ports and a memory bandwidth of more than 250 Gbytes/s. This leads to a peak performance of 1 GFLOPS for each CPU. A 16-GFLOPS system is achieved by combining 16 of these CPUs with 2 Gbytes of main memory. The high performance is attained by using 64-way parallelism and a dual-vector pipeline. The pipeline allows each of the 16 CPUs to deliver two vector results for every clock cycle. An optional solid-state disk has a storage capacity of up to 16 Gbytes and offers a bandwidth of 7.2 Gbytes/s. *RN*

SUPER-COOLED 6-BIT ADC IC SAMPLES AT 14 GHZ

By operating at 4.2K (the temperature of liquid helium), a monolithic 6-bit analog-to-digital converter can operate at a mind-boggling 14 gigasamples/s—the world's fastest, according to its developer Hypres Inc., Elmsford, N.Y. Moreover, 5-effective-bit (5-eb) accuracy has been obtained on 2-GHz sine waves, and 4- and 3-eb accuracy on 4- and 8-GHz sine waves, respectively. Aperture uncertainty time (jitter) is estimated to be a mere 5 ps. And power dissipation is a minuscule 10 mW, thanks to an architecture that uses one periodic comparator per bit of resolution. That power usage would be considered low even for a 6-bit, 40-MHz ADC. This superconducting IC is built from Josephson-junction devices called SQUIDs (Superconducting Quantum Interference Devices), which are made with a 10-layer, thin-film niobium process that can be deposited on any flat substrate, such as a silicon or gallium-arsenide IC. The converter's design expands easily to provide 8- or even 10-bit resolution (conventional flash ADCs need $2^n - 1$ comparators per bit, where n is the resolution in bits). Hypres' next step will be to add a 1-kbit shift-register storage element to the converter chip to form a transient digitizer that can sample at 20 Gsamples/s. Such a circuit can become the heart of a sampling oscilloscope or a radar receiver. Hypres has already built 16-bit shift registers clocking at 11.5 GHz. The ADC IC was developed for the Strategic Defense Initiative Organization under a contract with Rome Laboratories at Hanscom Field, Bedford, Mass. *FG*

WAFER-BONDED SILICON ON INSULATOR ARRIVES

Before the end of next year, expect Analog Devices Inc., Norwood, Mass., and Unitrode Corp., Merrimack, N.H., to introduce wafer-bonding processes for high-speed analog-IC designs to improve existing product lines. Thus, the two firms will join Harris Semiconductor in the wafer-bonded silicon process arena *(see "Linear ICs Attain 8-GHz npns, 4-GHz pnps," p. 35)*. Analog Devices, which will start with high-speed op amps, plans to buy its wafers already bonded from Japan's Shinitsu. Shinitsu's complementary-bipolar (CB) process, designed specifically for bonded wafers, provides npn and pnp transistors with f_ts greater than 4 and 3 GHz, respectively. Unitrode will go for high-speed switching-regulator controllers, using wafers from their joint development and manufacturing program with Motorola Inc., Phoenix, Ariz.

One key element in Unitrode's decision to go to bonded wafers is to simultaneously increase the speed and packing density of its present products. As a result, Unitrode's first products from the bonded wafers may be on a non-complementary, bipolar process. But the process' vertical npns will still sport f_ts beyond 1 GHz. Moreover, the pnps from the CB process that will follow the non-complementary bipolar process should have similar f_ts. Additional information on next-generation analog and mixed-signal IC processes, particularly CB processes using wafer bonding, will be available in our Jan. 9, 1992 Technology Forecasting issue. *FG*

CB PROCESS BUILDS 10-GHZ NPNS, 4-GHZ PNPS

In a major switch, AT&T Microelectronics is now ready to offer its junction-isolated CBIC-V process to merchant-market IC users in various standard-product and ASIC forms. The process offers npn transistors with an f_t of 10.2 GHz, and more-difficult-to build vertical pnp transistors with an f_t of 4.3 GHz. AT&T has used this manufacturable process internally for several years to build transmitters, receivers, and clock-recovery circuits for glass-fiber transmission systems. AT&T will start with a family of analog and mixed-signal (metal-mask programmable) tile arrays, discrete quad-transistor arrays, and ultra-fast comparators, all due early next year. These will be followed by a family of wideband amplifiers in late spring. The summer will see high-speed buffers, transimpedance amplifiers, and analog switches and multiplexers. Sampling amplifiers will appear later in the year.

Three quad-transistor arrays holding four npns, four pnps, and a pair of each will be first off the process. Offset voltages will match within 1 mV, and betas (current gains) will match within ±2.5%. The comparators can handle ±5 V, have propagation delays below 1 ns, and are 8-bit accurate. The op amps, which will offer bandwidths reaching to 500 MHz and 15-ns settling times to within 0.01%, need just 250 mW of power. The analog arrays will offer macros with performance similar to the standard products. For additional information, call 1-800-372-2447, ext. 823 (in Canada, 1-800-553-2448, ext. 823) *FG*

LINK TRANSFERS 100 MBYTES/S MINUS HOST BUS

Direct data transfers of up to 100 Mbytes/s can be achieved on DT-Connect II, a 32-bit interconnect scheme. The new standard, from Data Translation, Marlboro, Mass., eliminates the host computer from the data-acquisition or image-processing loop. This lets time-critical data bypass the bottleneck in the host bus. Data acquired from an I/O board can be transferred at 25 MHz to other boards for immediate processing and analysis through DT-Connect II. The standard enables time-critical, compute-intensive applications to be performed on a PC/AT or compatible system. Up to five I/O, processor, or memory boards can be tied together on DT-Connect II.

The free specification is an extension of the company's previous interconnect scheme, DT-Connect. The new version is logically and electrically backward-compatible with its predecessor. Because the standard's 32-bit modes are symmetrical, any board can transfer data to and from any other board within the connection. For example, processors can talk to other processors, and data-acquisition boards can interface with frame grabbers, etc. A broadcast mode lets any board send data to multiple processor boards for parallel processing. With additional lines for interrupts and general communications, processor boards can exchange timing and control information, independent of the host. For more information, contact Data Translation at (508) 481-3700. *RN*

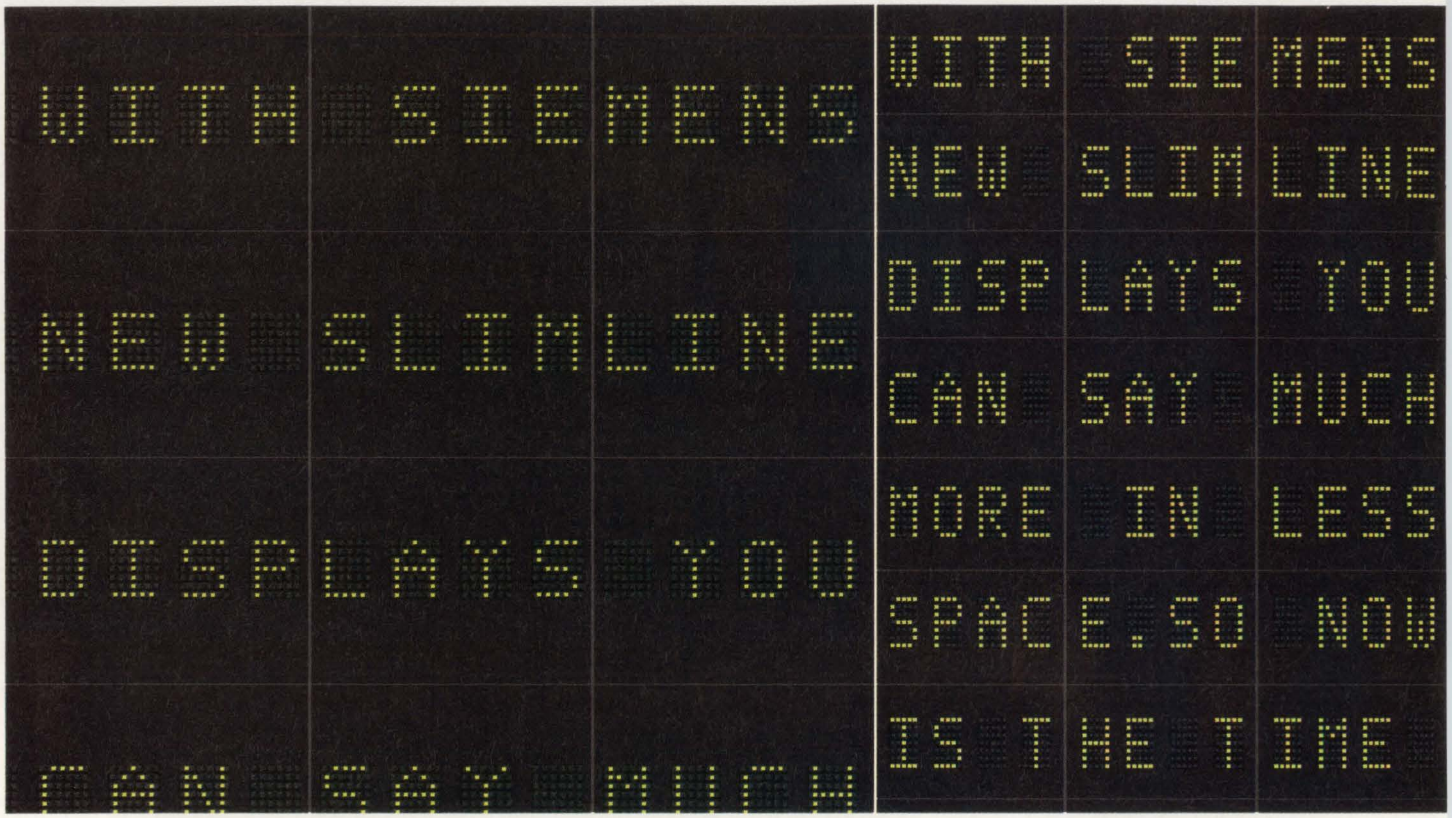
TRIPLE VIDEO ADC HAS 30-MHZ SCAN RATE

A scanning rate of 30 MHz makes a video analog-to-digital converter the fastest such device, according to its developer. Intended to handle TV's three color components, the SDA 9205-2 from Siemens AG, Munich, Germany, integrates three 8-bit video ADCs on a chip. The device permits oversampling, which means it uses a scan rate of more than twice the signal frequency. External antialiasing filtering can be simplified, thanks to internal digital filtering. The new Siemens converter, developed at the company's facilities in Villach, Austria, features internal clamping and separately selectable scanning data formats that conform to the CCIR/Rec. 601/656 international standard. To accommodate the three converters on one chip, the SDA 9205-2 uses CMOS for high speed and high integration density at low power consumption. With a signal-to-noise ratio of 46 dB, the device is suitable for digital image processing in PCs, TV sets, and video recorders, as well as studio equipment and video printers. The chip is supplied in a plastic leaded chip carrier PLCC-68 package. Samples are available now. *JG*

TRANSISTOR FOR PCN BASE STATIONS DEVELOPS 32 W

An output power 50% higher than any previous level of the company's transistor types promises to turn Philips Semiconductors' 32-W LXE18300X into a new standard for transmitting transistors. Aimed at personal-communications-network (PCN) base stations, the bipolar transistor will give a big boost to the power needed to service mobile phones in densely populated areas, particularly during peak hours. The common-emitter device also has a high power gain—typically 10 dB—to reduce the transmitter's amplification stages. The LXE18300X is a microwave silicon power transistor that works as a high-performance amplifier in class-AB transmitters. The output power is 32 W for 1-dB compression, measured at 1.85 GHz at a 24-V supply and 300 mA of collector current. Intermodulation distortion is below –30 dBc at an average output power of 15 W. Efficiency is a high 44%. Besides reducing end-user equipment running costs, the device allows operation with a junction temperature of only 98°C, which lengthens the device's operating life. Samples of the transistor, which comes in an FO-91 hermetically sealed metal ceramic envelope, are available now. *JG*

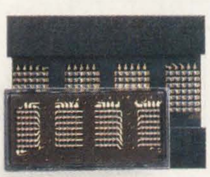
SIEMENS



We Admit This Test Of Our Slimline Display Is Stacked In Our Favor.

Our new LED dot matrix Intelligent Display® has proven once again why Siemens is at the forefront of display device technology. And has left the competition at a loss for words.

Because its package size is 60% smaller, the Siemens SLx2016 Slimline allows you to say a lot more, in a lot less space. The Slimline family features a .4-inch package height, rather than the .8-inch height industry standard, while keeping a .19-inch character height. Plus, our displays are X *and* Y stackable, to give you maximum flexibility in your design.



The SLx2016 is the first in a series of Siemens Slimline Intelligent Displays, all of which will give you on-board display drivers with control logic and easy addressability.

And it's available now, in four bright colors including red, yellow, green, and High-Efficiency Red.

So if you're looking for the slimmest Intelligent Display available, compare us to the competition. You'll see that they just don't stack up.

For more information, call (408) 725-3423, FAX (408) 725-3439, or write:
Siemens Components, Inc.
Optoelectronics Division
19000 Homestead Road
Cupertino, CA 95014-0799

Distributors: Advent Electronics, Inc., Hall-Mark, Insight Electronics, Marshall, Summit, Western Microtechnology.

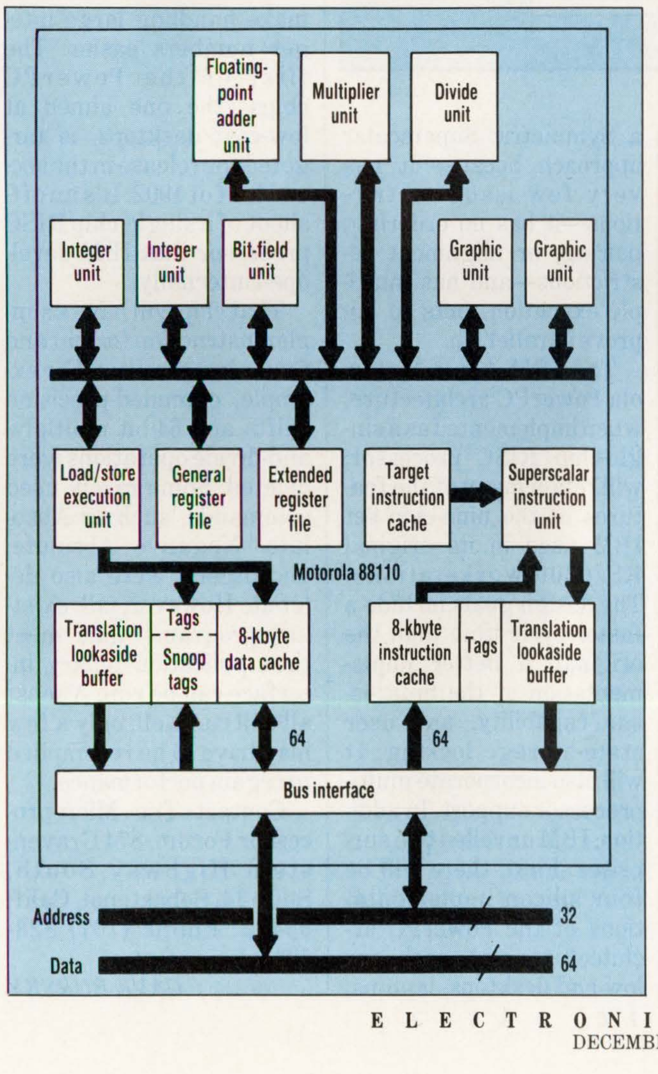
CIRCLE 154 FOR U.S. RESPONSE **CIRCLE 155 FOR RESPONSE OUTSIDE THE U.S.**

HIGHLY INTEGRATED RISC CPUS SIMPLIFY SYSTEM DESIGN, DELIVER 60-90+ MIPS

As developers create newer generations of top-performing reduced-instruction-set computers, the architectural directions for RISC chips converge to a common set of features. The latest highly integrated RISC CPU chips discussed at last month's Microprocessor Forum in Burlingame, Calif., bear out that observation.

Designers of the 64-bit SuperSparc biCMOS processor, developed jointly by Sun Microsystems Inc., Mountain View, Calif., and Texas Instruments Inc., Dallas, Texas; the 64-bit M88110 CMOS processor developed by Motorola Inc., Austin, Texas; and the R4000 from MIPS Computer Systems Inc., Sunnyvale, Calif., appear to have discussed these devices at length, judging from the similarity of their features. Also released at the conference were the first architectural details of the joint IBM-Apple-Motorola PowerPC processors.

Both the TI-Sun and Motorola processors employ dual integer units along with on-chip IEEE-compatible floating-point units, dual caches, and JTAG test ports *(see the figures)*. Furthermore, each processor will be supported by a second-level cache control chip that addresses up to 1 Mbyte of second-level cache. A quick perspective of the R4000, described in a previous issue of ELECTRONIC DESIGN, positions the chip as being similar to the SuperSparc chip but containing only one integer unit and smaller caches of 8 kbytes each for both data and instructions.



However, that's where the similarities between the chips ends. The one observable high-end difference is that Motorola's RISC chip also includes a graphics coprocessor that enables the processor to perform interactive 3D rendering without a separate graphics engine. As the actual implementation details surface, it's clear that designers took radically different approaches.

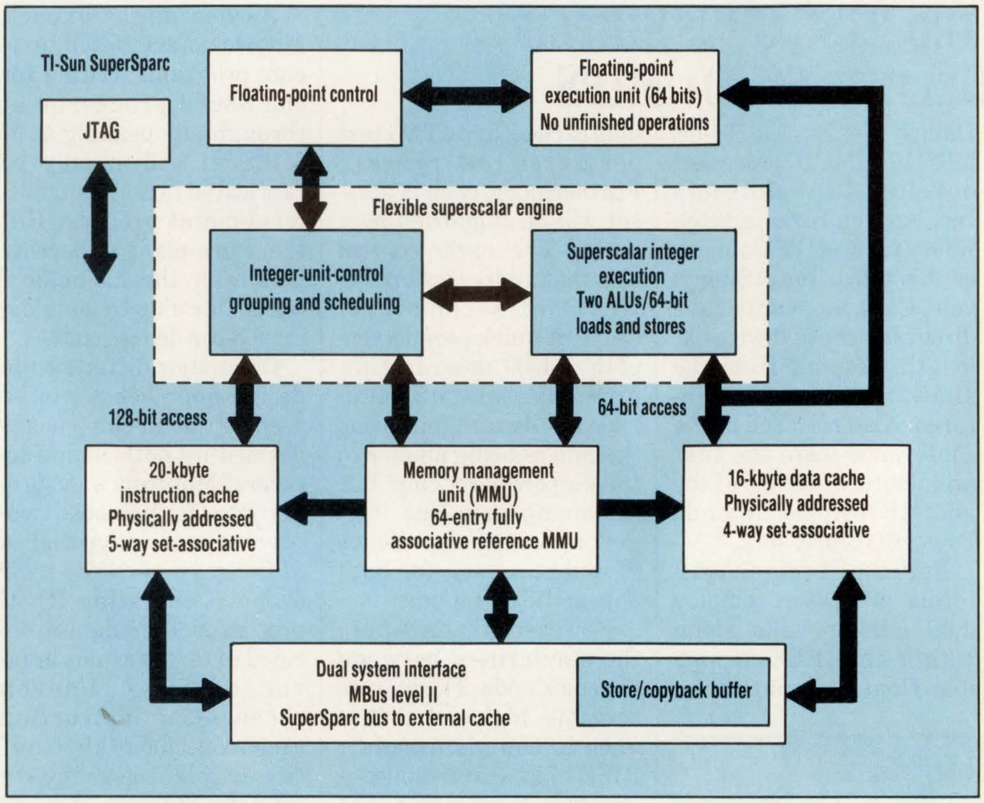
Because the SuperSparc was designed as a high-end upgrade to existing Sparc systems, the chip includes a direct MBus II interface, which includes the 64-bit-wide data path. With the highly parallel architecture, three instructions can be issued every cycle. Overall performance is about three times that of a SparcStation 2 system (60 to 80 MIPS). Initial versions of the 3.1-million-transistor chip will be implemented with TI's 0.8-μm biCMOS triple-level-metal process. The chip will execute old Sparc binaries as well as binaries compiled for the SuperSparc pipeline.

As one might expect, Motorola's 88110 will execute programs written for the 88000 processor at throughputs peaking at 97 MIPS. It will initially be fabricated in a 1-μm triple-level-metal process. But there are plans underway to shrink the 1.3-million-transistor chip by employing 0.8-μm design rules.

One major difference in design approaches can be seen in the on-chip caches defined by both manufacturers. Motorola's designers opted for balanced two-way set-associative caches of 8 kbytes each for their second-generation RISC processor. TI designers decided to tip the scales in favor of large uneven caches—the instruction cache contains 20 kbytes of five-way set-associative memory; the data cache 16 kbytes of four-way set-associative memory.

The SuperSparc's cache employs nearly 1 million more transistors than the cache of the 16-kbyte M88110. To move data quickly into and out of the caches, TI employs a 128-bit-wide internal bus for its instruction cache and a 64-bit bus for the data cache. Motorola's caches both employ 64-bit internal interfaces. Furthermore, both TI-Sun and Motorola employ 64-bit external data interfaces to secondary off-chip caches, while MIPS designers opted for a 128-bit-wide interface to speed cache updates.

In the area of floating-point math, the FPU on the SuperSparc performs double-precision 64-bit calculations. The FPU on Motorola's processor can execute 80-bit extended double-precision operations, as well as the single- and double-



precision calculations. A three-stage pipeline in the 88110 enables the processor to issue both Multiply and Add instructions on every clock. Although that causes a three-clock latency for all precisions, it reduces data-dependency stalls and allows the FPU to achieve a maximum throughput of 64 MFLOPS. In addition, a radix-8 divider minimizes the time for division operations. The SuperSparc FPU also has a three-cycle latency and delivers a throughput similar to that of the M88110.

Integer operations are approached with different resolutions as well. TI employs dual 32-bit ALUs that can be concatenated to form a 64-bit ALU, while Motorola opted for wider data paths and has dual 64-bit ALUs that produce 80-bit-wide results. The general register files supporting the ALUs include four 80-bit-wide read ports and two 80-bit write ports. A history buffer on Motorola's processor records the machine state so that if an instruction fault occurs, the entire state of the processor can be backed up to the previous instruction. True speculative execution is performed by the 88110 on branches, which accelerates execution flows.

The SuperSparc and M88110 perform dynamic grouping and scheduling—on the SuperSparc, groups of up to three instructions can be formed from the next three instructions after the program counter value. The size of the group that will execute simultaneously is based on dependency and resource requirements. Motorola designers dubbed their architecture a Symmetric Superscalar approach because it has very few issue restrictions—it has no ordering, pairing, or alignment restrictions—and has multiple execution units to improve parallelism.

The IBM-Apple-Motorola PowerPC architecture, when implemented as a single-chip RISC processor, will retain many of the features of the nine-chip set IBM used in its original RS/6000 workstations. The design goals include a faster cycle time than the original, a better implementation of the multi-issue capability, and user state-storage locking. It will also incorporate multiprocessor support. In addition, IBM unveiled two surprises. First, there will be four silicon implementations of the PowerPC architecture, one each for low-end desktops, laptops, high-end desktops as well as file servers.

Second, to simplify the architecture to fit on one chip, several features were deleted. They included a few floating-point instructions, especially those for double-precision operations. Several pieces of the architecture were also modified to simplify the fabrication. Furthermore, several instructions were extended to multi-cycle execution rather than keep them at single-cycle execution. Instructions that were removed can be emulated by a trap to a subroutine, which then executes that instruction. Operations on 64-bit data can be done, and several new instructions were added to make handling large integer numbers easier. The first of the PowerPC chips—the one aimed at low-cost desktops, is targeted for release in the second half of 1992. It's an offshoot of a single-chip RISC processor that IBM developed internally.

That chip will have a simpler instruction format and fewer instructions. For example, extended-precision shifts and 64-bit multiply-and-divide operations were deleted. Some rarely used commands, such as Absolute, Negative Absolute, and others, were also deleted. However, all existing programs that meet the application binary interface can be run. Almost all will run well; only a few may have to be recompiled to regain performance.

Contact The Microprocessor Forum, 874 Gravenstein Highway South, Suite 14, Sebastopol, Calif. 95472. Phone (707) 823-4004.

DAVE BURSKY

HIGH-SPEED SERIAL BUS LOOKS TO TAP INDUSTRIAL APPLICATIONS

A four-year quest to pack as much computing power as possible into the smallest physical volume has led London, England-based Psion plc to develop a robust and novel high-speed serial data-transmission bus architecture that looks to find a place on the industrial shop floor. The bus, which can operate with a wide range of peripheral devices, is part of Psion's series 3 palm-top computer introduced last fall.

Psion claims that the 6.5-by-3-by-0.9-in. computer is the most powerful palm-top computer available *(see the photograph)*. This claim rests partly on the use of a proprietary multitasking operating system running on a static version of the Nippon Electric Corp V-30H processor, which is equivalent to Intel Corp's 80C86 16-bit CPU.

Colly Meyers, Psion's technical director, says that the development started from a conviction that Flash EPROMs would be the ideal solution for data storage for a range of pocket, hand-held and notebook computers.

Series 3 sports 256 kbytes of user memory and 384 kbytes of ROM in which are embedded operating-system and user applications. What gives the palm-top computer its true power and makes it interesting is the technology Psion invented, which allows an almost unlimited ability to read and write from solid-state memory cartridges with many megabytes of data-storage capacity.

At the heart of the system is the SIBO bus, which was devised so Psion could use solid-state disks (SSDs)—high-capacity, high-integrity, low-power and physically rugged solid-state memory cartridges. SIBO can also provide connectivity with a wide range of peripherals, such as bar-code and magnetic-card readers, voice-recognition and processing systems, radio pagers, and RS-232 communications devices including modems.

Although developed specifically for Psion's own portable computers, both the transmission system and the SSDs are sufficiently physically and electrically robust to survive the rigors of environments such as factory floors and delivery trucks. Psion plans to share SIBO technology with third parties and is already working with five companies who want to use the system in such applications as test and measurement, production machinery, and commercial data collection.

The SIBO bus features a "hot-insertion" capability, which allows the insertion and removal of SSDs and peripherals while the host system is fully powered. "Since most of the applications envisioned for our system are event-driven and are therefore multitasking, it is imperative that devices could be connected and disconnected without affecting running programs," Meyers further explains.

The SSDs are matchbook-sized cartridges measuring 63 by 52 by 6 mm. The cartridges are metal-cased and are fully screened. They use either Flash EPROM, ROM, or battery-backed static RAM. In the two years that Psion has made them, data capacity has kept pace with semiconductor memory chip technology. Now Psion is selling SSD cartridges—Meyers calls them "packs"—with capacities of 1 Mbyte of RAM and 2 Mbytes of Flash EPROM. Meyers promises that those figures will be quadrupled by mid-1992. All SSDs, including the Flash-EPROM-based version, use a file structure that's compatible with the MS-DOS.

The SIBO bus is a bi-directional synchronous system designed to run at a maximum rate of 5.12 Mbit/s. "That's a theoretical design limit," Meyers says. In the company's current products, the bus is normally operated at a maximum clock rate of 3.84 MHz to address memory cartridges, and at a clock rate of 1.536 MHz to address peripherals.

The series 3 is based on two out of a series of eight ASIC chips. The two chips, ASIC-2 and -5, are master and slave on the link, respectively, *(see the diagram)*. The ASIC-5 slave is a multipurpose generic I/O chip that can be mask-programmed to identify the type of device in which it is installed—one of three or four types of memory cartridge or a specific type of peripheral. Four variants have been made so far. The slave also assigns an address to the memory by which it can be recognized on a single bus. In its design, Psion allowed for a total of 32 different device-type identifiers and 32 bus addresses. Versions destined for use in SSDs also administer the filing system, simulating a file-allocation table (FAT) required by MS-DOS.

The master chip, ASIC-2, is a serial link controller. It contains an on-chip crystal oscillator, which can be made to run at frequencies between 2 and 20 MHz, from which a clock signal can be derived at rates dependent on the system requirements. The chip sets up and controls eight separate virtual channels, each of which can be addressed independently, and if necessary at different clock rates. Four of the channels are used to address SSD memory cartridges and

CIRCLE 91

four are used with peripheral devices—although the last four channels can also be used to access SSDs and for writing.

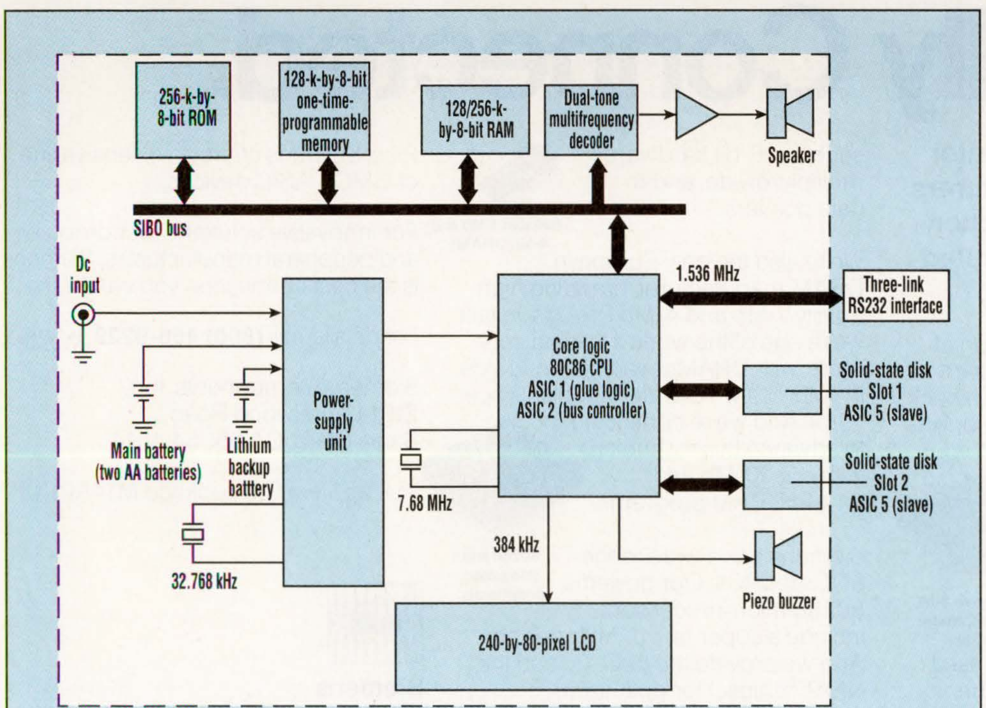
A newer version of ASIC-2, now nearing production, also has the equivalent of a slave device on-chip so that a pair can provide a high-speed, bi-directional, time-multiplexed serial link that's capable of transferring data at 1.5 Mbits/s. That version will be offered to third parties.

Prime use for this device is on an adapter card that can be added to desk-top computers or other processor systems. The first product of this type due for launch in the next month or so will be a card for IBM-compatible PCs. Meyers explains that this card will serve several functions. On the one hand, it will allow a four-slot Psion SSD drive to be used with a PC either as an external device or to replace a standard floppy-disk drive. That will allow data to be transferred from the PC to Psion's machines by swapping SSDs.

More importantly, the PC card will include a port for the Psion 1.5-Mbit/s serial link. Interconnecting this link with a similar port on a portable computer allows the PC to be read from and to write to SSDs directly without the SSDs being removed from the portable terminal. The eight virtual channels on each card can each be used to collect or load data from a separate memory pack through this high-speed link at rates of up to 100 kbytes/s. The number of packs that can be addressed over a single bus is limited only by the 32-address limit imposed by the I/O circuits—so four such cards can be used in a single PC.

Physically, the link comprises six wires: ground, clock, data, and three power lines. Power lines carry 5.5 V, which are dropped through a diode within the SSDs to provide the 5-V main power supply for the memory chips. Next is a 17-V line. A regulator built into the SSD reduces that to the 12.5 V the Flash chips need for erasure. The third power line is used to sustain RAM chips while the SSD is plugged into its host, bypassing the lithium back-up battery that keeps memory alive away from the computer. The arrangement is similar for peripherals, except that one of the unwanted power lines is replaced with an additional signal line that can carry a an interrupt signal from the peripheral device to switch the computer's CPU out of standby.

Hot insertion is handled by using a specially designed connector in the SSDs. The connector is a female plug with its contacts staggered to ensure that when it is plugged into the host, the ground connection is made first, followed by the signal lines, and then the power rails. "On the system side, the designer can use a standard 0.1-in. flat-pin male connector," Meyers says. He adds that these types of connectors are good for tens of thousands of make-break insertions. These connectors are also less susceptible to dirt and electrical noise than multiway parallel connectors.



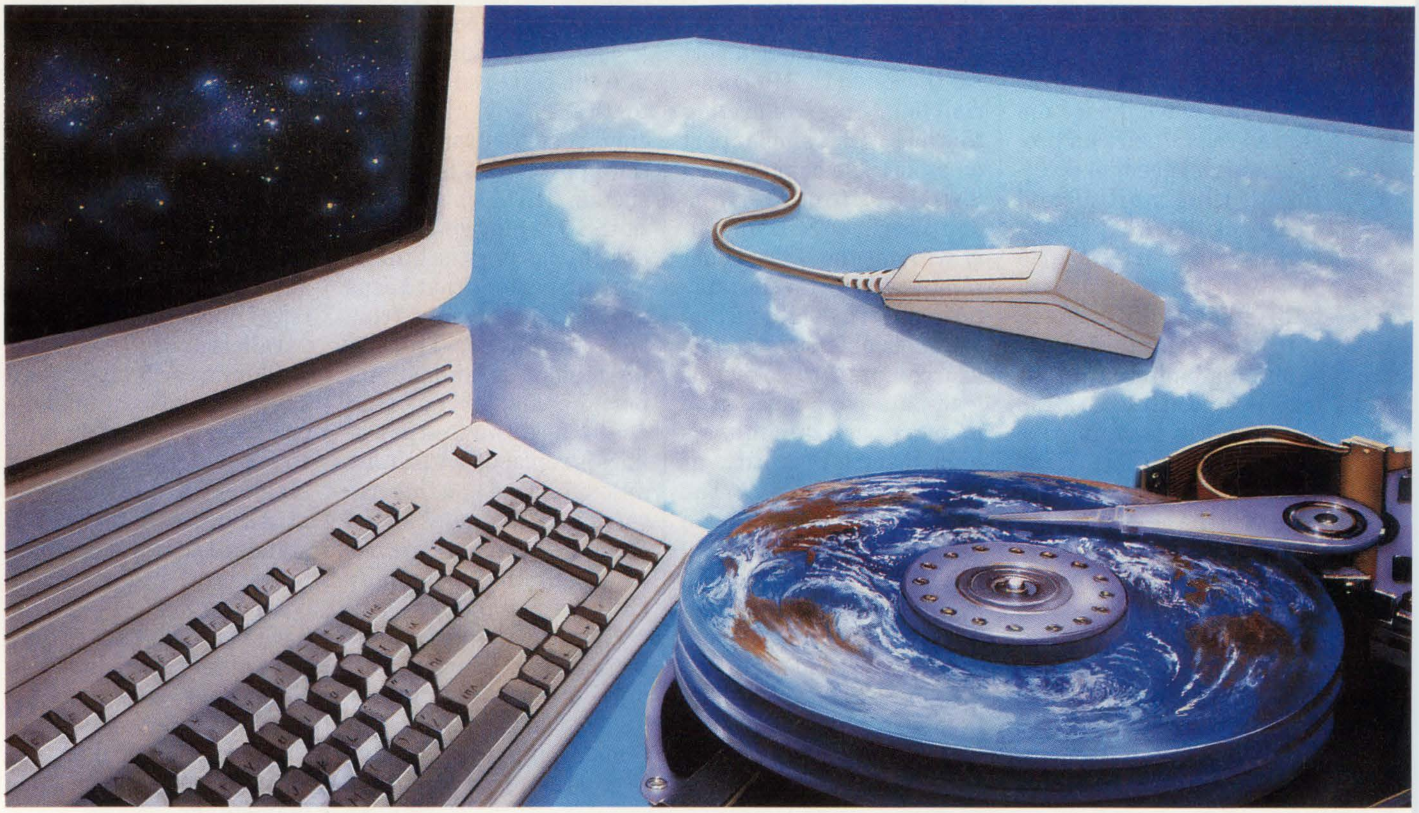
Plug-in cards on the market using solid-state memories are compatible with the Personal Computer Memory Card International Association (PCMCIA) standard that was adopted by several other pocket-computer makers—a standard that Psion's card does not adhere to. However, Psion does not see its approach competing with the PCMCIA standard and believes that it is more complementary.

"The PCMCIA standard calls for a parallel connector that's really an extension of the standard IBM-compatible PC internal bus," says Meyers. That means that a PCMCIA cartridge is placed right in the machine's memory map, and makes memory access faster than Psion's serial system. However, Meyers points out that the standard is defined especially for IBM-compatible machines, whereas Psion's can be used with virtually any processor or microcontroller architecture.

For more information, contact Psion plc at Alexander House, Frampton St., London, NW8 8NQ England, or call 44 (0)81 262 5580.

PETER FLETCHER

SIEMENS



Globally Connected.

Siemens provides computer and peripheral manufacturers with a worldwide connection for state-of-the-art integrated circuits.

Siemens is building on a tradition of innovation with state-of-the-art technology in the workplace. And we back it with worldwide service and support, providing a global partner for all your system designs.

Innovative 8-bit microcontroller designs.

For applications such as laptop PCs, printers and disk drives, which require lower power consumption, we offer CMOS 8-bit microcontrollers based on the 8051 architecture. Like the SAB80C537, with advanced features such as 16-bit hardware multiply/divide, and 8 data pointers.

Reliable 1-Mb and 4-Mb DRAMs.

We're also the only European DRAM manufacturer, providing high-quality 1-Mb and 4-Mb DRAMs. In fact, we're one of the world's leading suppliers, with DRAMs available worldwide, in volumes which have doubled since 1989. And we're continuing to advance this technology with our 16-Mb and 64-Mb DRAM programs.

80286 and integrated peripherals.

Siemens has a wide range of ICs for PCs. Our powerful 80286 microprocessors include a super-fast 16 MHz design. And we provide the 82C206 and the NEAT™ chipset for optimized, low-cost solutions.

Plus, Siemens offers an extensive line of CMOS ASIC devices.

For innovative solutions for computer and peripheral manufacturers, Siemens is the best connection you can make.

For details, call **(800) 456-9229**, or write:

Siemens Components, Inc.
2191 Laurelwood Road
Santa Clara, CA 95054-1514

Ask for literature package M14A013.

Siemens
World Wise, Market Smart.

CIRCLE 152 FOR U.S. RESPONSE
CIRCLE 153 FOR RESPONSE OUTSIDE THE U.S.

FROM OP AMPS AND ASICS TO ATE PIN DRIVERS, A NEW DI WAFER-BONDING PROCESS UPS THE SPEED AND BANDWIDTH OF PRECISION LINEAR ICS.

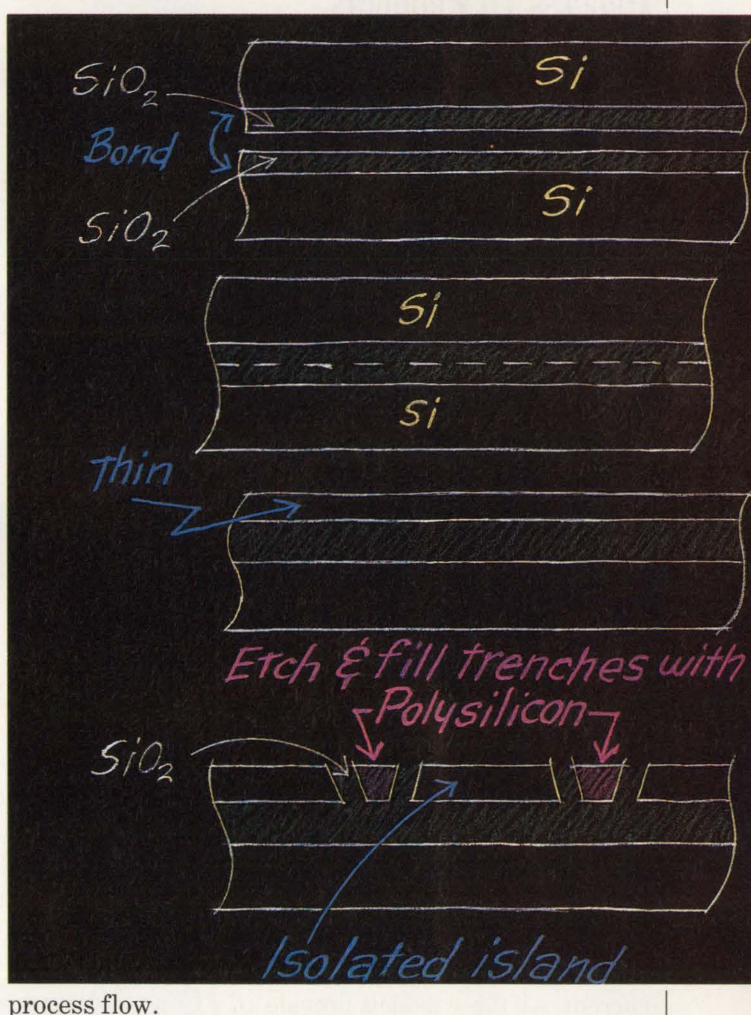
LINEAR ICS ATTAIN 8-GHZ NPNS, 4-GHZ PNPS

FRANK GOODENOUGH

By using a multi-disciplinary team of marketing, process-and-IC design, and manufacturing members, Harris Semiconductor becomes the first to move direct wafer bonding, one of the newer silicon-on-insulator (SOI) technologies, into the merchant-market linear-IC arena. The team's process designers have also unleashed UHF-1, a UHF complementary-bipolar IC technology, on these bonded wafers. The UHF-1 process is targeted at making analog ICs (particularly amplifiers and other linear circuits) which require not only fast npn transistors, but also fast pnp transistors.

SOI processes, which are semiconductor processes using dielectric isolation (DI), have been around since the early 1960s. In such processes, individual or groups of transistors are galvanically isolated from each other and from the semiconductor (usually silicon) substrate wafer by a true-dielectric layer, such as silicon dioxide. SOI processes make possible higher-performance devices than are obtainable with conventional junction-isolated (JI) processes.

However, multiple problems occur with conventional DI/SOI processes, not the least of which is a wafer-diameter limit of four inches, making them unsuitable for the mass production of ICs, which in turn means lower IC costs. In addition, the DI/SOI process requires device-specific wafers. That is, each type of IC must have a wafer specifically designed for it after the IC itself is designed *(see "A brief review of SOI technologies and their advantages," p. 40).* The fabrication of the basic wafer becomes part of the IC fabrication process, but is outside the standard process flow.



To combat these problems, Harris Semiconductor's designers developed the wafer-bonding technology and the UHF-1 process along with it *(see the opening illustration, this page).* The UHF-1 process features vertical npn transistors sporting f_ts of 8 GHz, while the f_ts of its vertical pnp siblings attain a high of 4 GHz. Moreover, these unity-gain frequencies are achieved at operating voltages between 1 and 10 V, and even at collector currents under 1 mA.

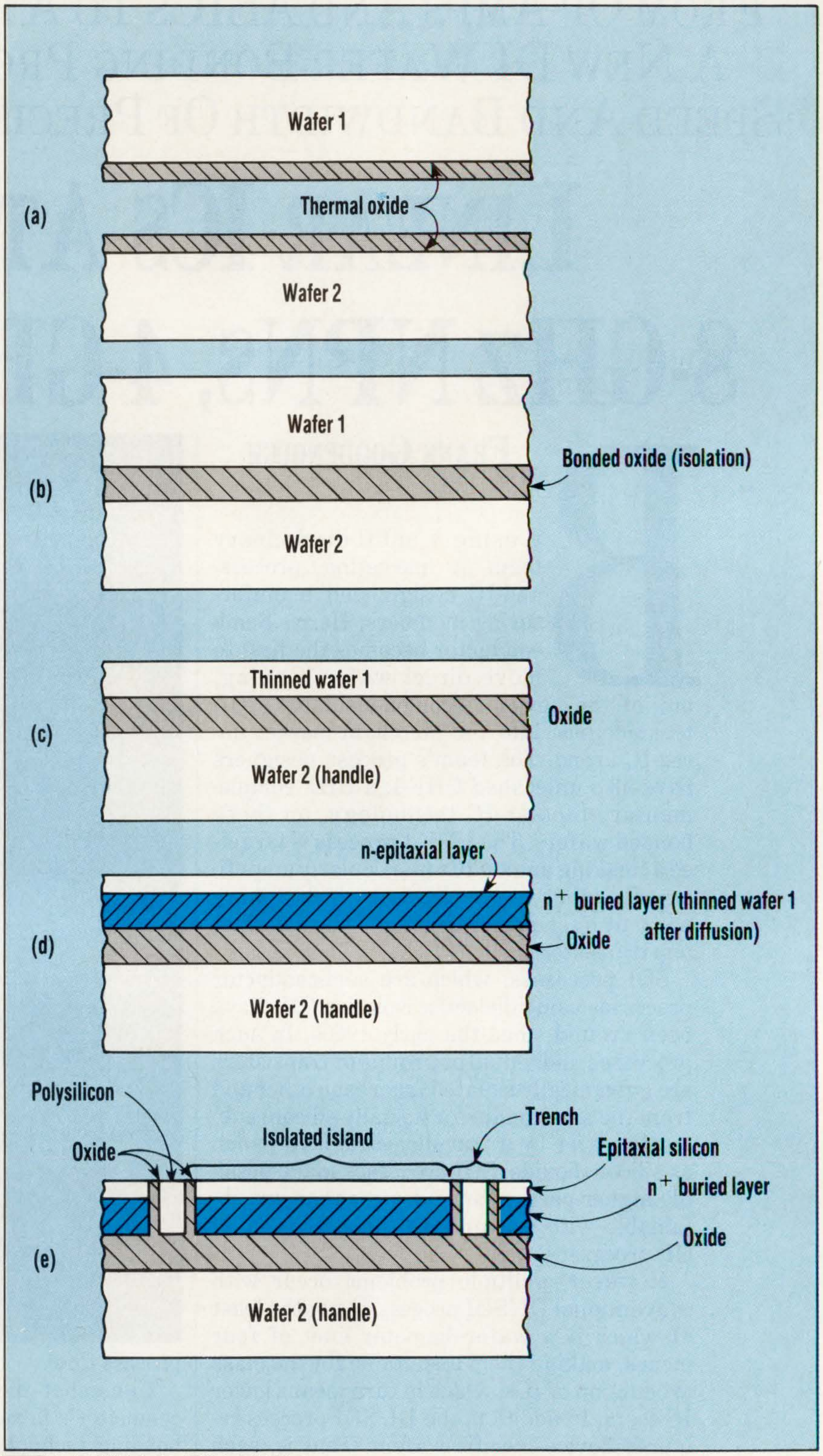
As their first shot out of the box, the team's chip designers started standard-product op-amp and ATE pin-driver IC families, as well as five-transistor arrays containing discrete devices. Harris has also created an analog tile-array family and an analog cell library on the wafer-bonded UHF-1. All of these first products offer performance, and/or features, equal or superior to those of any competitive ICs.

Process To Products

The HFA1100/1120/1130 op amps from the UHF-1 process are its flagship products. These unity-gain-stable current-feedback IC op amps offer the widest bandwidths for a monolithic device. They feature a 2500-V/μs typical slew rate, 850-MHz 3-dB bandwidth, and 11-ns settling time to within 0.1% for a 2-V step *(Table 1)*.

A quick look at their specifications gives a strong indication of where these op amps will find homes. They will be used to handle fast analog pulses (pulses containing information in their amplitude), and handle baseband video waveforms plus IF and RF signals. The built-in voltage clamps are needed in various applications, such as driving flash and other video-speed ADCs. By providing specifications for distortion, third-order intercept, noise figure, and 1-dB compression, these op amps are ready for the designer of systems processing RF signals.

All three op amps are available in 8-pin DIPs and SOICs. The HFA1100 is offered in the standard pinout, with pins 1, 5, and 8 uncommitted. The HFA1120 has the ability to trim the 6-mV offset voltage, through zero at pin 5, by adjusting the bias current. All three models provide an internal clamp to ensure fast recovery from saturation due to signal transients. The HFA1100/1120 clamp at the supply rails. The HFA1130's negative and positive limits of its clamp voltage can be set by the user (with pins 5 and 8, respectively). The negative limit can be set between –5 and +3.5 V; the positive



1. BONDED WAFERS **and their oxide-isolated islands of silicon are produced by growing oxide on a pair of wafers (a). Next, the wafers are clamped together in a hot oxygen atmosphere and a chemical bond forms between them (b). One of the wafers is then thinned by lapping (c). After that, a diffusion is driven into the thinned wafer, lowering its resistance, and an epitaxial layer is grown on it (d). Finally, vertical trenches are etched to the oxide layer, the trench sides are oxidized, and the trenches are filled with polysilicon (e).**

limit can be set between –3.5 and +5 V.

A fourth device, the HFA1110 closed-loop buffer, is aimed at applications similar to those of the op amps and has similar specifications. However, it not only drops into the socket of standard video-speed buffers for a gain of +1, but the user can also pin-strap it to provide a gain of –1 and +2 without the need to use any external resistors. The gain of +2 configuration is particularly useful for the 6-dB loss that occurs when driving a doubly terminated transmission line.

In the near future, the HFA1105 op-amp family will arrive with 300-MHz bandwidths and 1000-V/μs slew rates, at quiescent currents under 10 mA.

TABLE 1: HFA1100/1120/1130 OP AMP SPECIFICATIONS

Specification	Units	Value
Input		
Offset voltage	mV	6
Transfer		
–3-dB bandwidth with V_{out} = 0.2 V pk-pk	MHz	500, (850 t)
Gain flatness to 100 MHz	dB	0.14
Gain flatness to 30 MHz	dB	0.01
Output		
Output voltage/current	V/mA	±2.8/±40
2nd-harmonic distortion at 30 MHz, V_{out} = 2 V pk-pk	dBc	–50(t)
3rd-harmonic distortion at 30 MHz, V_{out} = 2 V pk-pk	dBc	–67(t)
3rd-order intercept at 100 MHz	dBm	32
1-dB compression at 100 MHz	dBm	15
Transient response		
Slew rate, gain = +2, V_{out} = 5 V pk-pk	V/μs	2000
Settling time to 0.1% for a 2-V step	ns	11(t)
Power supply		
Voltage range	V	±4.5 to ±5.5
Quiescent current	mA	24

All specifications are maximums or minimums at 25°C unless noted typical (t).
Conditions are a supply voltage of ±5 V, closed-loop gain of +1, feedback of 510 Ω, and a load of 100 Ω and 0 pF.

SPEEDY DRIVERS

Hundreds of IC pin drivers lie at the heart of today's high-speed VLSI test systems. Each pin in these systems is driven by such a driver. For example, a 256-pin tester can test ICs with up to 256 pins. It also requires 256 drivers that produce the actual test signal applied to the digital IC being tested.

A pin-driver IC has one digital-data input, which commands the output to swing to either a logic high or a logic low. A pair of analog inputs set the voltage levels associated with the high and low states. An additional digital input puts the drivers in what's called the high-Z mode by disconnecting their output from the device under test (DUT) in 3 ns.

One such driver developed on the HF-1 process is the HFA5250. This device achieves maximum 1-, 3-, and 5-V rise and fall times of 0.75 ns, 1.2 ns, and 1.5 ns, respectively, while driving a load of 50 Ω. The IC achieves 50-MHz data rates required for compatibility with today's fastest logic testers. Its output swing of +8 to –3 V tests all common logic families.

If you want to design and build your own circuits with UHF-1 technology, there are three possible alternatives. If you want to stay with a discrete board-level design, you can build a circuit using one or more of the HFA3XXX series of transistor arrays to be available in the following five configurations: HFA3096 (3 npns, 2 pnps), HFA3046 (3 npns, 1 npn differential pair), HFA3127 (5 npns), and HFA3128 (5 pnps).

Each transistor in an array is dielectrically isolated from every other transistor and all three leads are brought out to the pins of the 16-pin DIPs and SOICs. They can be wired up exactly like discrete transistors with significant savings in board space and parasitic wiring capacitance. Matching characteristics are also significantly superior to those of two or more discrete transistors.

TABLE 2: COMPARING THE UHF-1 PROCESS WITH CONVENTIONAL PROCESSES

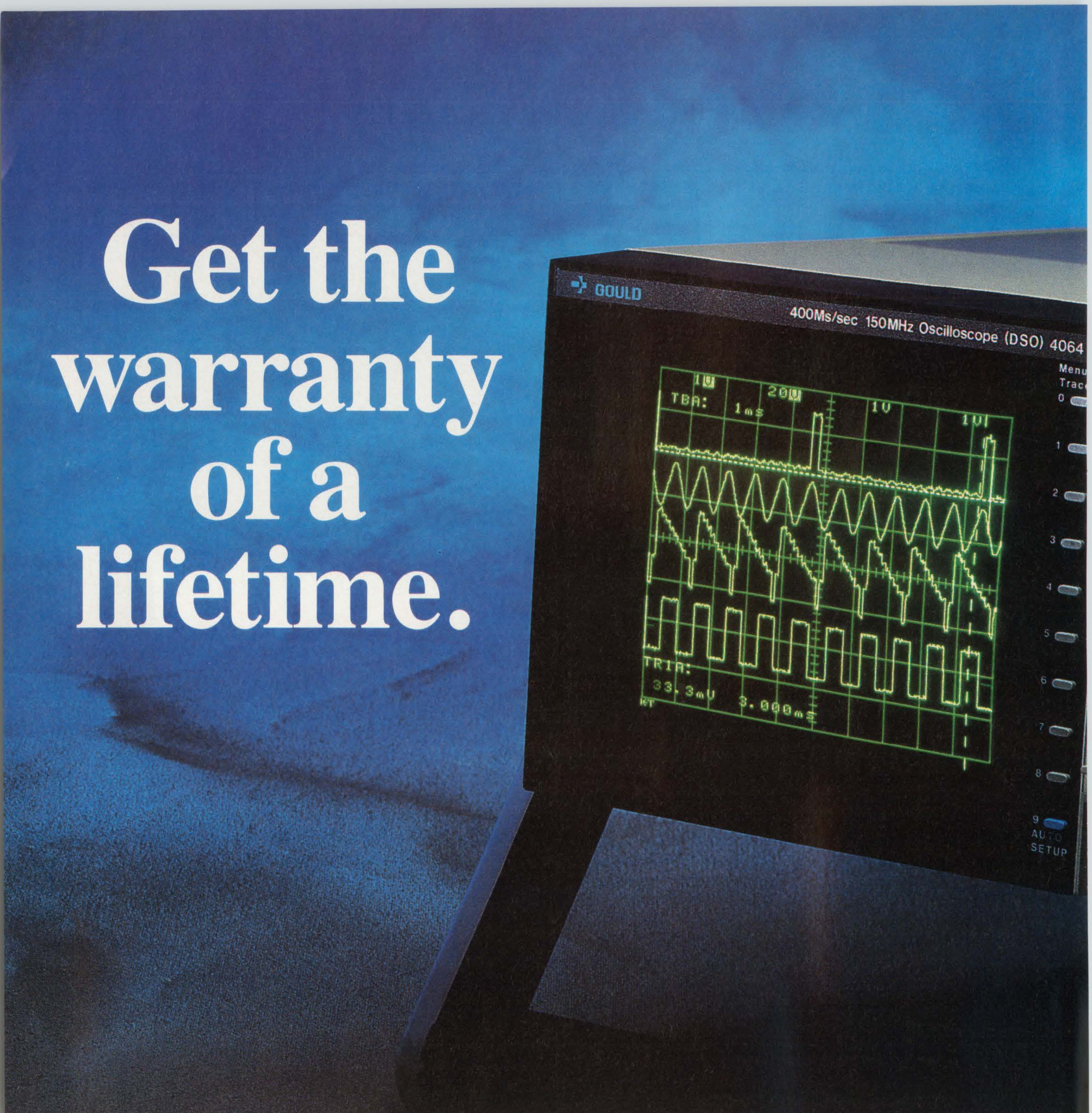
Process	Units	UHF-1		X		Y	
		npn	pnp	npn	pnp	npn	pnp
Beta (β)		150	100	110	40	175	180
f_t	GHz	8	4	4	2	0.650	0.600
βV_{CEO}	V	12	12	18	14	36	36
Practical operating voltage	V	10		11		32	
Early voltage (V_A)	V	60	40	40	11	60	55
$\beta \times V_A$	V	9000	4000	4400	440	10,000	10,000

On the other hand, if you're ready to become an IC designer, or have already tried your hand at it and want to try the UHF-1 process, you can move to the HTA3000 tile array, or jump to the HDI3000 Device-Level Design System. In either case, you have access to today's highest-performance analog ASIC technology. The HTA3000 contains over 600 transistors of various sizes, equally divided between npns and pnps. They're distributed evenly over the array's ten identical tiles. Both the HTA3000 and the HDI3000 are supported by Harris' Bipolar Analog FASTRACK Design System, which provides schematic capture, simulation, and routing. You can design at the transistor level on the array, and/or take advantage of the macros, which range from op amps and buffers to sampling amplifiers and references.

HOW IT'S DONE

To achieve wafer bonding, Harris takes two wafers and grows thermal oxide (typically 0.5-μm thick for high-speed analog ICs) on one surface of each wafer *(Fig. 1a)*. The wa-

Get the warranty of a lifetime.



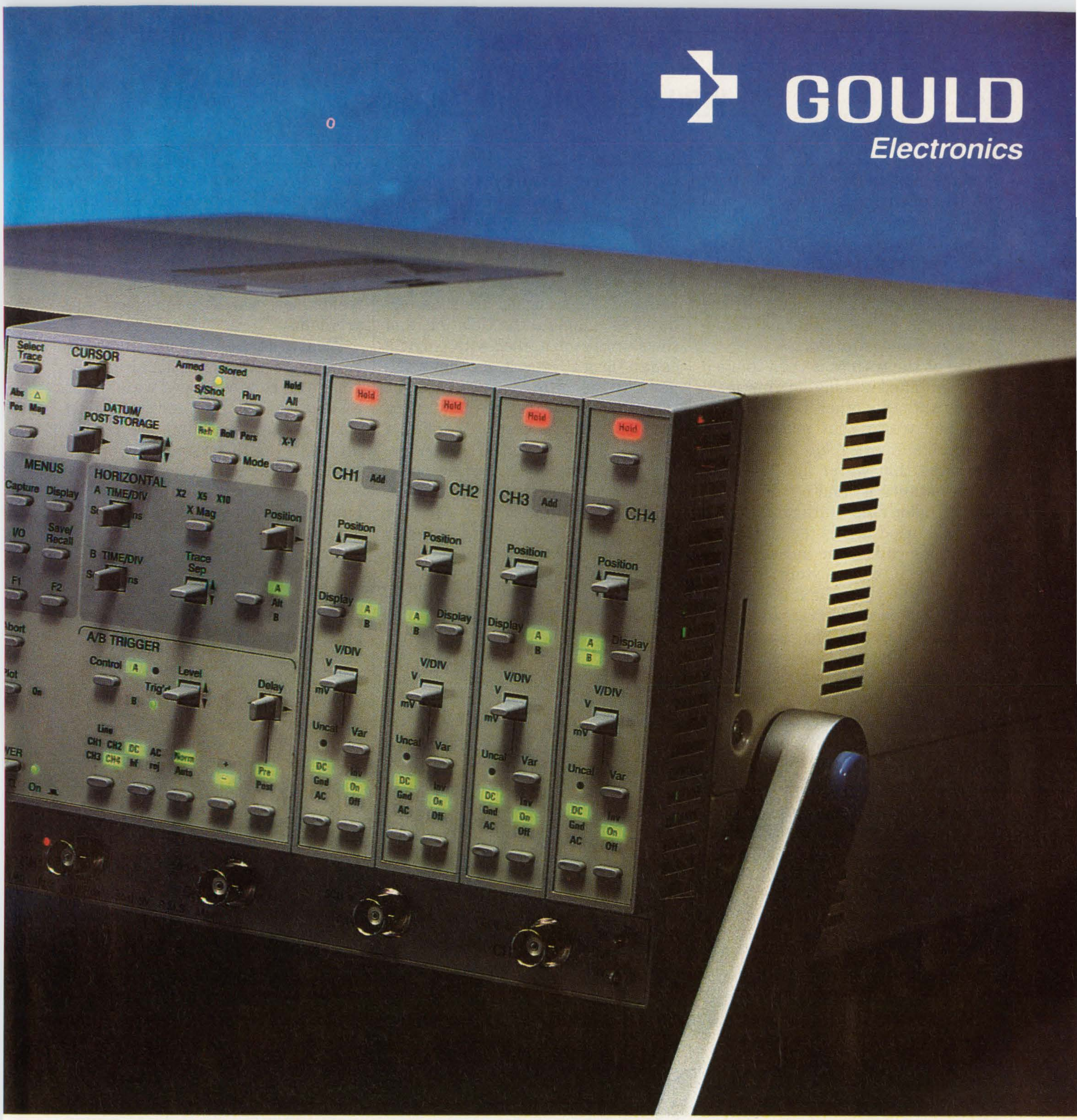
At Gould, we're so sure about the reliability of our new 4060 family of high-performance digital storage oscilloscopes, we back them with the longest warranty in the industry. You're fully covered for as long as we manufacture the product—or five years—whichever is longer.

How can we make that promise? With complete confidence.

Because we control quality every step of the way. Everything from our ASIC and advanced surface-mount technology to our sophisticated burn-in process is designed to provide you with the most reliable DSO made.

And the high performance you need for both repetitive and transient signal capture.

Available in 2- and 4-channel versions, the 4060 gives you 400MS/sec sampling at a 150MHz



bandwidth, 8–bit resolution, on-screen signal measurement and analysis, plus glitch capture. What's more, you can get IEEE-488.2 and RS-423 interfaces, and an integral 4-color pen plotter or thermal array printer for instant hardcopy. Our intuitive push-button panel makes everything strikingly simple to use.

In fact, about the only thing we haven't built into the 4060 series is a high price. It's about half of what you're used to paying.

And you'll find the same advantages across Gould's entire line of new oscilloscopes.

For an on-site demonstration, and details regarding the warranty, call Gould at (216) 328-7000. You'll be glad you did for years to come.

CIRCLE 112 FOR U.S. RESPONSE

CIRCLE 114 FOR RESPONSE OUTSIDE THE U.S.

Yes! ☐ Rush me a free 4060 brochure
☐ Have a Gould representative call to arrange a demonstration
☐ Send me a free DSO catalog

Name: ____________________

Title: ____________________

Company: ____________________

Street: ____________________

City: __________ State: ______ Zip: ______

Telephone: ____________________

Send to: Gould Inc., Test and Measurement Group, 8333 Rockside Road, Valley View, Ohio 44125.
Fax: (216) 328-7400.

ED 12/91

fers are next clamped together with the oxide surfaces in contact and heated in an oxygen atmosphere to about 700°C (the exact temperature is proprietary). A continuous atomic bond forms between the wafers with a strength equal to that of the strength in a typical thermal-oxide-to-silicon bond *(Fig. 1b)*.

One of the wafers is then thinned by a combined etching-lapping technique, and the other becomes the "handle" wafer that provides mechanical support *(Fig. 1c)*. Harris turns the thin wafer into selective low-resistance n^+ and n^- silicon, via two diffusion steps, ultimately forming the buried layers (or as they're sometimes called, the buried collectors) of the IC's transistors *(Fig. 1d)*. A layer of n-type epitaxial silicon is then grown on the surface of the future buried layers *(Fig. 1d, again)*. The UHF-1's transistors are built into and on this epitaxial layer. These are the basic bonded wafers, ready for the lithography and standard IC process flow.

At this point, reactive-ion etching (RIE) divides the wafer into dielectrically isolated islands of silicon, with the size and shape required for a specific IC. RIE forms narrow vertical trenches from the surface of the epitaxial layer to the oxide layer. The walls of the trenches are then oxidized to complete the isolation, and their centers are filled with polysilicon to form a flat surface that's planar with the top of the epitaxial layer *(Fig. 1e)*. The wafer can now carry out its primary mission: Building a high-performance linear IC on the UHF-1 process. It should be noted that neither these wafers, nor the wafer-bonding technology, is limited to just analog ICs. In fact, increasing oxide thickness and trench width adapts the technology to high-voltage ICs, such as SLICs (subscriber-line interface circuits) connected to every phone line and off-line power-control chips.

This wafer-bonding process isn't as simple as the previous description sounds, though. In wafer-bonding work first tried by IBM about six years ago and followed up by Harris and others, some early wafers looked like the rippled potato chips used for party dips, and voids in the oxide bond caused the die to fall apart (delaminate) when diced. However, Harris, thanks to proprietary techniques, was able to solve these problems.

What are the advantages of wafer bonding over conventional Harris DI? To start, any bonded wafer built to take the UHF-1 process can be used for any IC needing the UHF-1 process (prior to the trenching operation), or potentially for other processes. Wafers of 5 and 6 in. can be built, rather than 4-in. wafers, making the process more cost-effective. Moreover, the narrow trenches raise packing densities significantly. The shallow construction minimizes the heat required to drive in (diffuse) the buried layer, which eliminates thermal effects.

In a conventional DI process, those effects would have made it impossible to achieve the transistor's mix of performance features. The shallow construction also permits a

A BRIEF REVIEW OF SOI TECHNOLOGIES AND THEIR ADVANTAGES

Junction-isolated (JI) IC semiconductor processes suffer from a number of dc and ac problems. Every new design thus represents a series of compromises and sometimes presents designers with mind-boggling challenges. These challenges, though severe for digital circuits, are often exacerbated by orders-of-magnitude for high-speed analog ICs and high-voltage ICs, regardless of application. As a result, early on, process designers developed several technologies offering multiple dielectrically isolated (DI), individual, active, and passive devices on one chip. The DI and silicon-on-sapphire (SOS) processes developed by Harris represent the first two, and until recently, the only silicon-on-insulator (SOI) processes readily available. In the Harris DI processes, oxide tubs completely enclose islands of monocrystalline silicon from a wafer. The tubs are formed by etching and lapping. In the SOS process, transistor-quality, monocrystalline silicon is grown epitaxially on sapphire wafers.

SOI processes, regardless of type, offer IC designers many advantages. Much like a chip-and-wire hybrid, virtually any kind of active or passive device in the process engineer's bag of tricks can be included in the same IC without the usual compromises. That is, the op-amp designer can have fast vertical pnps with performance approaching that of the processes' npns. The transistors' f_ts are limited only by the inherent lower mobility of p-type devices. The analog-IC designer can also call for JFETs, Zener diodes, Schottky diodes, and non-voltage-sensitive oxide capacitors. Speed is inherently superior to ICs built on JI processes due to lower parasitic capacitance between devices and between the collector of the transistors and the substrate wafer. In addition, this capacitance isn't modulated by collector voltage. The reduced capacitance also increases the speed-power product of ICs built on SOI processes because this capacitance need not be charged.

All JI IC transistors contain parasitic silicon-controlled rectifiers, which can cause latch-up if inadvertently triggered by transients or by the application of excessive dc voltage. SOI processes completely eliminate such parasitic problems. In fact, SOI processes can achieve device-to-device breakdown voltages exceeding 2000 V. Because virtually all of these parasitics become worse as the junction temperature is raised or if the IC is subjected to ionizing radiation, ICs built on SOI processes tend to have superior performance at high temperature and to offer resistance to such radiation.

More guaranteed good news.

Good news travels fast.

Because now you can get the industry's longest warranty on the fastest digital storage oscilloscope in its class.

The new Gould 465 portable DSO.

The 465 gives you 100MHz bandwidth with a full 200MS/sec sampling on two channels—which is up to 20 times faster than similarly priced DSOs. Combined with 2GS/sec equivalent time sampling, the 465 excels at capturing both repetitive and transient signals.

That's in addition to all the advanced features packed into this small DSO, like automatic on-screen measurements, persistence mode, glitch capture, IEEE-488.2 (SCPI) and RS-423 interfaces, and a built-in 4-color pen plotter. All intuitively simple to use.

And like the rest of Gould's new line of DSOs, the 465 is warranteed as long as Gould manufactures the product—or a full five years—whichever is longer.

For an on-site demonstration, and details regarding the warranty, call Gould today at (216) 328-7000. You'll like what you see. Guaranteed.

Yes! ☐ Rush me a free 465 brochure
☐ Have a Gould representative call to arrange a demonstration
☐ Send me a free DSO catalog

Name: ____________________

Title: ____________________

Company: ____________________

Street: ____________________

City: ____________ State: ______ Zip: ______

Telephone: ____________________

Send to: Gould Inc., Test and Measurement Group, 8333 Rockside Road, Valley View, Ohio 44125. Fax: (216) 328-7400.

ED 12/91

CIRCLE 113 FOR U.S. RESPONSE

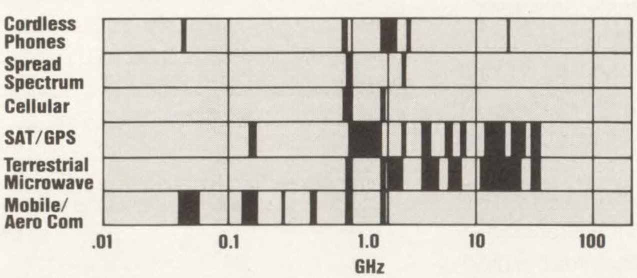
CIRCLE 115 FOR RESPONSE OUTSIDE THE U.S.

RF/MICROWAVE COMPONENTS ACROSS THE COMMUNICATIONS SPECTRUM

Semiconductors to Supercomponents

When it comes to high performance, high volume, and high frequency, no one matches Avantek. For over 25 years, we've been the leader in developing new levels of circuit performance for communications systems across the spectrum. Avantek provides cost effective solutions for the most particular design requirements. Our product line is continuously growing both in process and application leadership. We offer both Si and GaAs based products providing the best performance/price choice for any high-frequency design. Discreet devices, ICs, hybrids, or system subassemblies, Avantek has the broadest line of standard components—literally thousands—for kilohertz to Gigahertz applications, and lightwave components too.

- Surface-mount plastic integrated circuits
- Low-noise amplifiers
- High-power amplifiers
- Active and passive mixers
- DRO, VCO, and YIG tuned oscillators
- Limiters
- Attenuators
- Switches
- Frequency converters
- Multiplexers



We Can Help Today

Your local Avantek sales engineer is an *engineer*, trained and experienced in critical RF/microwave design-in situations and uniquely qualified to support you. Ready to provide design literature, CAD modeling software, or prototype samples. Backed by application engineering teams, your Avantek sales engineer makes the design-in process fast, reliable, confident, and affordable.

The Largest RF/Microwave Component Distribution Network

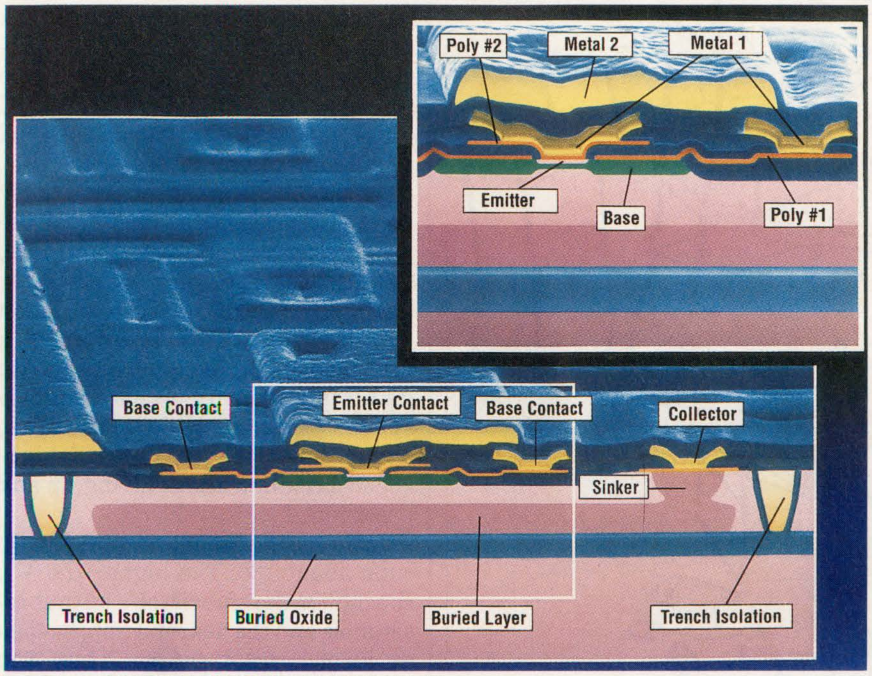
With over 20 major stocking locations, and a worldwide transshipment operation, Avantek delivers millions of parts every month. We meet the demands of the most demanding JIT program, or supply a critical single prototype with the same matchless service and support. Call us today to hear how we can support your great designs.

Call 1-800-AVANTEK

AVANTEK

CIRCLE 90

BONDED-WAFER HIGH-PERFORMANCE LINEAR ICs



2. THE SHALLOW STRUCTURE of the UHF-1 transistors, made possible by wafer bonding, permits the diffusion of a sinker between the collector and the buried layer.

low-resistance sinker to be diffused, connecting the collector contact to the buried layer and lowering collector resistance *(Fig. 2)*. In high-voltage applications, the shallow construction helps remove the heat from of the chip. In addition, parasitic capacitance is lower (half that of a JI process), increasing the slew rate and thus full-power bandwidth.

As noted earlier, the UHF-1 process was designed specifically to go on trench-isolated SOI wafers. However, the primary mission of its developers was to come up with a process that could build the fastest-slewing and widest-bandwidth *precision* linear ICs. Bipolar transistors and their processes are truly application-specific. The npn transistors used on fast SRAMs differ from those on ECL chips, and the transistors needed for top-of-the-line analog ICs, regardless of speed or bandwidth, must differ significantly from those used in either of the SRAM and ECL digital applications.

PARAMETER OPTIMIZATION

For starters, today's applications still demand an operating voltage of at least 10 V. But the analog-IC designer also demands optimization of three device parameters: beta (β) or current gain, the Early voltage (V_A), and the product of beta and the Early voltage ($\beta \times V_A$). Yet the last two parameters are rarely talked about outside the hallowed halls of analog IC and process designers.

Both β and V_A degrade as the transistor designer attempts to raise the device's f_t. The use of transistors, each of which are individually oxide-isolated, helps Harris' designers achieve the speed as well as precision performance required for npn and pnp transistors when compared with transistors made from today's fastest JI complementary-bipolar processes *(Table 2)*.

Note the superiority in both V_A and the β-V_A product of UHF-1 transistors over those of process X, which offers half the f_t at about the same operating voltage. Note also that the f_t of UHF-1 is 6 to 12 times that of process Y, but process Y's V_As, and its β-V_A product, are about the same as that of UHF-1.

But what's the big deal with Early voltage and the product of it with beta? If you're an analog circuit designer who enjoys designing "neat"

BONDED-WAFER HIGH-PERFORMANCE LINEAR ICs

circuits, it will give you some compassion for linear-IC designers stuck with a process based on compromises. In addition, if you decide to someday use UHF-1 in its ASIC guise, that will start you on the road to thinking like an IC designer.

In the simplest terms, the Early voltage represents a function of the practical, and therefore non-infinite, output resistance of a transistor at its collector and its ability to function as a current source. Maintaining a high beta-V_A product helps eliminate gain stages, helps produce higher-speed, faster-settling amplifiers, and permits the creation of high-speed circuits without giving up any precision.

In an IC, the V_A of an npn typically runs about 130. The higher the V_A, the higher the transistor's output resistance and the nearer it approaches an ideal current source. Thus, the better it biases an amplifier or acts as an amplifier's active load in a typical analog IC. A differential-pair amplifier with an active load can have very high gain, but only if its transistors have sufficient V_A. For example, the gain of a classic npn differential-pair transistor with a pnp active load is the product of the npn-pair's transconductance and the parallel combination of the output resistance (V_A/collector current) of the npn and the pnp transistors.

The core circuit of most high-speed op amps uses a cascode configuration with a common-emitter stage in series with a common-base stage. Both its open-circuit voltage gain and its collector resistance represent direct functions of the transistor's beta-V_A product.

UHF-1 offers more than just high speed and gain. Its speed-power product permits it to build tomorrow's products at the collector currents of today's fastest linear ICs. Alternatively, it can build versions of today's high-speed ICs that operate with quiescent currents of only a fraction of those required by existing devices. For example, dropping the collector current of an npn transistor that's operating at an f_t of 8 GHz by a factor of 100, say from 1 mA to 10 μA, still leaves the designer

BONDED-WAFER HIGH-PERFORMANCE LINEAR ICs

with an f_t of an amazing 1 GHz, high enough to create some very fast, micropower op amps.

The UHF-1 process also offers n-channel JFETs with an f_t of 4 GHz, a buried Zener diode, oxide capacitors, laser-trimmable thin-film nichrome resistors, and double-metal interconnects. The JFET makes possible analog multiplexers, sample-and-hold amplifiers (SHAs), and low-bias-current, low-current-noise op amps for integrators and current-to-voltage converters. The buried Zener diode builds high-quality references. The oxide capacitors not only stabilize op amps, but can also store the SHAs' samples. The thin-film resistors create fast ICs offering dc precision. Finally, the double metal cuts die size and helps minimize parasitic capacitance, while its polysilicon emitters increase emitter efficiency *(Fig. 2, again)*.□

PRICE AND AVAILABILITY

The HFA1100/1120/1130 family of current-feedback op amps and the HFA1110 closed-loop buffer come in 8-pin plastic and ceramic DIPs and 8-pin SOICs. They're rated for commercial-, extended-industrial, and military-temperature ranges. Pricing for all four in plastic DIPs starts at $9.95 each in 100-unit lots. They will be available in March 1992, with the lower-power family due out about a month later. CIRCLE 511

The HFA5250 ATE pin-driver IC comes in a 28-pin SOIC and in die form. It's rated for the commercial-temperature range. Pricing for the SOIC version begins at $48 each in 1000-unit lots. Small quantities will be available in February 1992. CIRCLE 512

The HFA3XXX family of transistor arrays come in 16-pin plastic and ceramic DIPs and are rated for the commercial-, extended-industrial, and military-temperature range. Pricing in quantities of 100 for the SOICs and plastic DIPs starts at $3.05 each. Small quantities will be available in April 1992. CIRCLE 513

Typically, non-recurring engineering (NRE) costs for the HTE3000 tile array run under $100,000, and for the HDI3000 Device Level Design System about $130,000. CIRCLE 514

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; 1-(800) 4-HARRIS, ext. 1047 CIRCLE 515

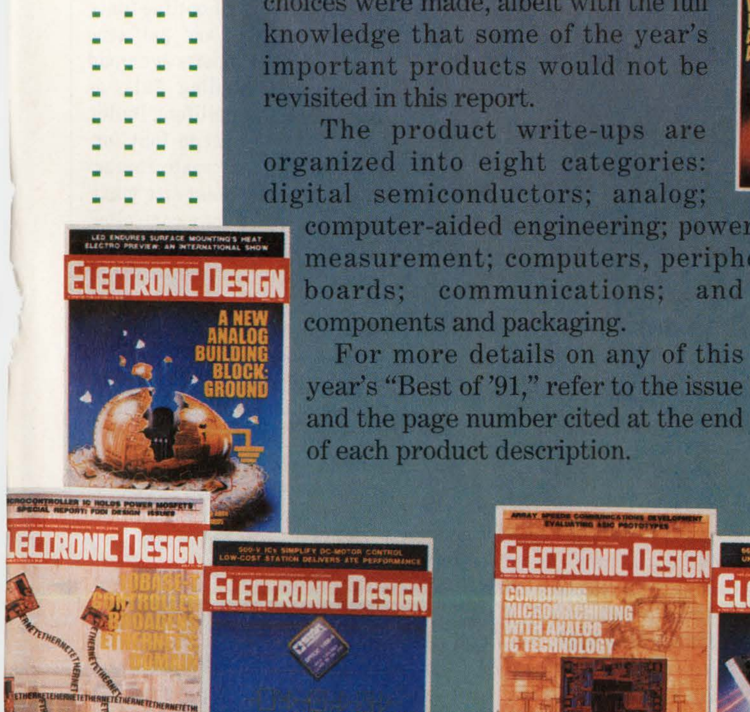
HOW VALUABLE?	CIRCLE
HIGHLY	526
MODERATELY	527
SLIGHTLY	528

The Best of '91

The following pages contain ELECTRONIC DESIGN's editors' selections of the top 100 products reported by the magazine during 1991. Of this year's Top 100, 23 were cover stories in ELECTRONIC DESIGN, as is shown by some of the covers illustrated on this page. Because our basic criterion for cover treatment is true, ground-breaking innovation, those 23 were obvious choices for the list. The remaining 77 were more difficult to select—we had to sift through a thousand or so excellent products that appeared in our pages during the year. Nevertheless, the choices were made, albeit with the full knowledge that some of the year's important products would not be revisited in this report.

The product write-ups are organized into eight categories: digital semiconductors; analog; computer-aided engineering; power; test and measurement; computers, peripherals, and boards; communications; and components and packaging.

For more details on any of this year's "Best of '91," refer to the issue and the page number cited at the end of each product description.



DIGITAL SEMICONDUCTORS

COMBO CPU AND DSP CHIP PERFORMS A SEA OF TASKS

Working from different downloaded control programs, the 1.1-million-transistor, 100-MIPS Swordfish processor can quickly switch its function from serving as, say, a laser-printer controller to a fax-modem processor, data modem, or an image processor. Thus, it could replace many separate dedicated controllers. The processor, which runs from a 25-MHz external clock, has a full 64-bit internal architecture with two four-stage integer pipelines. An on-chip IEEE-754-compatible double-precision floating-point unit (FPU) has its own pipeline, so both integer and floating-point computations can be done in parallel. *Electronic Design, February 14, p. 41.*

NATIONAL SEMICONDUCTOR CORP., *2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; (408) 721-6816.* **Circle 601**

BUILD SCSI RAID SYSTEMS TO BOOST DATA AVAILABILITY

Raid architectures, which are storage subsystems based on redundant arrays of inexpensive disks, offer higher I/O throughputs to keep up with fast processors. With Raid, data is also better protected against drive failures, and large "virtual" disk drives can effectively be created. The industry's first commercial chip sets for building small and large Raid systems include a 16-bit-wide, fast SCSI-2 controller (the 53C916), and a bus extender (the 53C932) to build 32-bit-wide and fast SCSI channels. At 10 MHz and with 32-bit words, the SCSI channel has four times the throughput of the fiber-optic I/O channels used on mainframes. For larger drive-array systems, up to 90 drives, the company has four additional new chips, plus the 53C916, to supplement the 53C916. *Electronic Design, March 14, p. 35.*

NCR CORP., *1635 Aeroplaza Dr., Colorado Springs, CO 80916; (719) 596-5612.* **Circle 602**

FAST BUS LINKS CPUs, DSPs FOR MULTIMEDIA SYSTEMS

By adding a new system bus, bottlenecks in most DSP systems can be overcome. The bus, dubbed Media Link, forms a high-speed interconnection that permits DSP chips, a host processor, and I/O peripherals to communicate, independent of the host-system bus. As a result, multiple processors can be interconnected to form systems that can add processing power or I/O functions, much as memory is added to a computer. A custom chip, the Media-Link Controller (MLC), transfers 16-bit-wide data at sustained rates of 66 Mbytes/s. The first version of the chip matches the control signals of a host Intel 80386 32-bit processor, or the Texas Instruments 32-bit TMS320C31 floating-point DSP chip. The on-chip logic permits a direct connection to the processor through a simple interface. *Electronic Design, May 9, p. 135.*

SPECTRUM SIGNAL PROCESSING INC., *3700 Gilmore Way, No. 301, Burnaby, British Columbia, V5G 4M1 Canada; (604) 438-7266.* **Circle 603**

COMBINATION RAM/PLD OPENS NEW APPLICATIONS

Data storage cells (registers or memory blocks like FIFOs, dual-port RAMs, or even standard static RAMs) are typically implemented inefficiently on most PLDs. However, the H5110 intelligent data buffer, a CMOS PLD chip, incorporates dedicated but configurable blocks of RAM, thus improving utilization efficiency. The chip includes four blocks of RAM. Every block is organized as 64 words by 9 bits and is configurable either as an independent block or combined in any mix to form deeper or wider memory blocks. Each 64-word block can serve as a dual-port RAM or two 32-by-9 single-port RAMs. Control logic associated with each block enables users to configure the memory function. *Electronic Design, May 23, p. 138.*

PLUS LOGIC INC., *1255 Parkmoor Ave., San Jose, CA 95126; (800) 253-7587.* **Circle 604**

IN-SYSTEM PROGRAMMABLE LOGIC KEEPS DELAYS SHORT

Except for RAM-based FPGAs, which must be loaded with their configuration data each time the system powers up, current alternatives can't be reconfigured in a system that's being upgraded or fixed. A family of in-system programmable large-scale-integration (ispLSI) logic arrays fills this reconfiguration gap. The ispLSI chips use 0.8-μm CMOS EEPROM technology that's also employed on the company's high-speed GAL programmable-logic devices. The chips run at system speeds up to 70 MHz, and have an input-to-output propagation delay (including I/O buffers) of just 15 ns through one logic level. The submicron process produces chips with 2000 to 8000 equivalent PLD gates, and 32 to 96 I/O leads. *Electronic Design, June 27, p. 137.*

LATTICE SEMICONDUCTOR CORP., *5555 N.E. Moore Ct., Hillsboro, OR 97124; (503) 681-0118.* **Circle 605**

X-TERMINALS EVOLVE TO NEXT LEVEL: NO ENCLOSURE

An X-terminal controller board designed with one of two new ASICs, the DDI-4029 or DDI-4129, replaces many other chips and reduces the board size so that it can be placed directly inside the monitor housing, eliminating the need for a separate enclosure. The differences between the parts involve resolution and clock rate. The 4129 supports color resolutions up to 1280 by 1024 pixels and a dot/pixel clock rate up to 120 MHz, while the 4029 supports color resolutions up to 1024 by 1024 pixels and a dot/pixel clock rate up to 80 MHz. The 4129's higher clock speed is needed to maintain higher refresh rates and resolution levels. *Electronic Design, July 25, p. 165.*

DOCTOR DESIGN INC., *5415 Oberlin Dr., San Diego, CA 92121; (619) 457-4545.* **Circle 606**

CHIP SET ADDRESSES LOW-COST WORKSTATIONS

A new motherboard logic chip set, called microCORE, packs all of the base-level functionality for Sparc-based workstations into just two to four VLSI chips. By carefully tuning the system architecture to optimize the chips' functionality, the chip set's designers have compressed the control for a monochrome system into two chips (including the video support), and for a color system into four chips. With the TM5610 System Controller Unit (SCU) and the TM5620 I/O Controller (IOC), designers can build a system with equivalent functionality to a 25-, 33-, or 40-MHz Sparcstation SLC. *Electronic Design, July 25, p. 45.*

TERA MICROSYSTEMS INC., *5200 Great America Pkwy., Suite 250, Santa Clara, CA 95054; (408) 987-5600.* **Circle 607**

ASIC PUSHES LASER PRINTER TO ITS LIMIT

With the RIDA (raster image device accelerator) ASIC, a laser printer can run at its rated engine speed and support a much faster engine. The chip accelerates the creation of outline fonts, line-art graphics, and half-tone images. RIDA supports even-odd and nonzero winding fills, as well as Type 1, Intellifont, Bullet, TrueType, and Speedo font formats. It also can create characters with a 1000-point size maximum. As a hard-copy controller, it offers fast page composition, even at resolutions above 300 by 300 dots/in. Because RIDA is accessed through the host bus, an existing board design can be modified by adding a daughtercard containing RIDA. *Electronic Design, September 12, p. 159.*

DESTINY TECHNOLOGY CORP., *300 Montague Expwy., Suite 150, Milpitas, CA 95035; (408) 262-9400.* **Circle 608**

80X86-COMPATIBLE FAMILY OUTPACES ORIGINAL CPUs

The Super386 ChipSystem Architecture consists of four 32-bit microprocessors, two math coprocessors, and an all-in-one "PC-on-a-chip" CPU. Two 32-bit processors, the 38600SX and DX, are pin-compatible with Intel microprocessors but deliver about

DIGITAL SEMICONDUCTORS

10% higher throughput. The other two 32-bit CPUs, the 38605SX and DX, include a 512-byte on-chip instruction cache for about 40% higher throughput than the equivalent-speed original 80386. On one chip, the F8680 PC-on-a-chip combines a 16-bit CPU that delivers 80286-equivalent throughput with a 4-stage pipeline, direct support for memory cards, a 26-bit address space, CGA graphics control for CRT or flat panels, and other features. *Electronic Design, September 26, p. 53.*

CHIPS AND TECHNOLOGIES INC., *3050 Zanker Rd., San Jose, CA 95134; (408) 434-0600.* **Circle 609**

PARALLEL-PROCESSING DSP CHIP DELIVERS TOP SPEED

A single-chip DSP with a multiprocessor architecture, supported by easy-to-use development tools, may open up wide areas of signal-processing-system design to DSP implementations. The Sproc 1400 has a multiprocessor architecture optimized for real-time performance and can handle real-time signal bandwidths of 250 kHz when clocked at 50 MHz. A shared central memory unit, which is surrounded by four independent general-signal processors, consists of 1024 words (24 bits wide) of RAM for data storage and a similar-sized RAM for code storage. Development tools, which are based on a signal-flow design approach, can automatically generate the code that controls and configures the chips. *Electronic Design, October 10, p. 43.*

STAR SEMICONDUCTOR CORP., *25 Independence Blvd., Warren, NJ 07059; (908) 647-9400.* **Circle 610**

CONTROLLER CHIP TIES IN MEMORY CARDS

The MB86301 IC reduces the amount of logic needed to connect a memory card to a host system on a motherboard or adapter card. The chip supports various semiconductor memory-card types, including SRAM, flash, UV EPROM, EEPROM, and ROM cards. It's compatible with the 68-pin memory-card standards from the Personal Computer Memory Card International Association and the Japan Electronic Industry Development Association. The chip offers a 26-bit memory address space and can handle memory cards with datapath widths ranging from 8 to 16 bits. It ties into host processors with 8-to-16-bit data buses, and includes byte-swap logic to adapt to both Intel- or Motorola-style buses. *Electronic Design, September 26, p. 168.*

FUJITSU MICROELECTRONICS INC., *IC Div., 3545 N. First St., San Jose, CA 95134; (408) 922-9405.* **Circle 611**

SECOND-GENERATION MAX BOOSTS DENSITY FIVEFOLD

The Max 700 family of ultraviolet-erasable programmable-logic devices gives designers from 4000 to 40,000 available gates. Logic-propagation delays are as short as 15 ns from one input, through the array, and to an output. To achieve the short delays and permit global clock speeds of 70 MHz, designers developed a low-skew programmable interconnect array that keeps skew to less than 2 ns. An enhanced macrocell supports complex logic functions with up to 32 product terms. The macrocell includes a new logic structure called parallel logic expanders, which permit complex logic functions to be implemented without incurring significant additional gate delays. *Electronic Design, May 5, p. 145.*

ALTERA CORP., *2610 Orchard Pkwy., San Jose, CA 95134; (408) 984-2800.* **Circle 612**

CUSTOM MEMORY CHIPS BOOST CACHE HIT RATES

With the concurrent-writeback cache architecture, system designers can achieve write hit rates of 99.8% and read hit rates of 96% for 80386- or 80486-based systems. The Simulcache chip set achieves such high hit-rate levels by optimizing for zero-wait-state performance on CPU writes and reads. Concurrency enables the CPU to read and write back to the cache while the cache simultaneously performs "housekeeping" tasks in the background. The chip set consists of a controller and dedicated cache-RAM chips. Initial versions of the chip set support CPUs running at 25 to 33 MHz with zero-wait-state memory access. *Electronic Design, April 25, p. 115.*

MOSEL CORP., *914 W. Maude Ave., Sunnyvale, CA 94086; (408) 733-4556.* **Circle 613**

CHIP SET COMPRESSES, TRANSFERS VIDEO DATA

Transferring video data to computers often requires high-speed channels, due to the large quantity of data involved. However, with a two-chip set, real-time video-data transfers over networks becomes economical and practical. The Bt291 is the RGB-to-YCrCb compressor, while the Bt294 decompresses the YCrCb data back to RGB data. The video-net converters conform to CCIR 601 and SMPTE RP-125 standards. The chips permit video sources and displays, such as cameras, tape decks, and monitors, to be connected to computers through real-time digital interfaces. *Electronic Design, March 28, p. 145.*

BROOKTREE CORP., *9950 Barnes Canyon Rd., San Diego, CA 92121; (619) 452-7580.* **Circle 614**

SMART CONTROLLER RESTARTS SYSTEMS

The Micro Softener chip can prevent microprocessor systems from crashing by maintaining the current state of the CPU in battery-backed-up memory. It can also initiate an emergency call for help to a remote system so that diagnostic software can be downloaded. Embedded in the chip is power monitoring logic, a watchdog timer, a nonvolatile controller, an address decoder, bootstrap ROM, parallel I/O ports, a dual-ported register file, and an interrupt controller. Versions of the DS53XX Softener—the DS5340, 5311, 5396 and 5303—will be available for the 8086-compatible high-integration NEC V40, the Motorola 68HC11, the Intel 80C196, and the Hitachi HD6301/6303. *Electronic Design, January 31, p. 118.*

DALLAS SEMICONDUCTOR CORP., *4350 South Beltwood Pkwy., Dallas, TX 75244-3292; (214) 450-0400.* **Circle 615**

FPGAs MIRROR MASKED GATE-ARRAY ARCHITECTURE

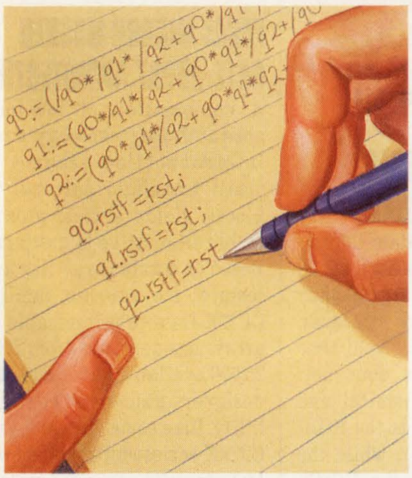
A combination of low-impedance antifuse technology, a novel interconnection scheme, and small transistor-pair building blocks yields a field-programmable alternative to gate arrays. Based on a gate-array-like architecture, the six-chip family of CP20K field-programmable gate arrays has densities from 2200 to 20,000 available gates, and offers designers gate-array configurability. Like some gate arrays, the CP20K series chips include many I/O pins and can efficiently implement small blocks of memory. The arrays also permit automatic or interactive place-and-route tools to interconnect the elements. The interactive tools allow the user to maximize performance and improve gate utilization. The chips include an IEEE 1149.1-compatible JTAG (Joint Test Automation Group) interface. *Electronic Design, November 21, p. 63.*

CROSSPOINT SOLUTIONS INC., *5000 Old Ironsides Dr., Santa Clara, CA 95054; (408) 998-1834.* **Circle 616**

CHIPS RENDER WORKSTATION GRAPHICS INEXPENSIVELY

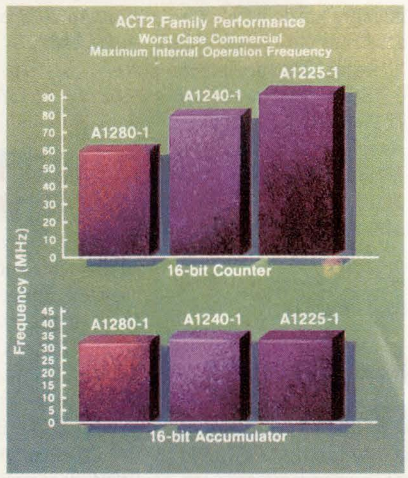
A chip set that comprises five 0.8-μm CMOS ICs delivers high-end workstation graphics with architectures that are designed to ease system scaling. The five chips are the GC1201 bit-block-transfer unit and 3D vector processor, CG1201 frame-buffer controller, CG1203 video controller, CG1204 depth buffer with shading processor, and the CGT1205 pixel accelerator. A low-end system with eight bit planes and a 4096-by-2048-pixel frame buffer could be built with as few as three of the chips (not counting RAM), drawing 3D vectors at 35

You Design Actel F
You Do A PLD. But T



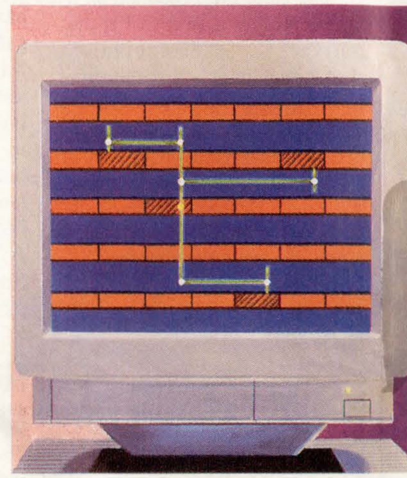
Use PLD Tools.

You design Actel FPGAs using the same tools as you would a PLD: ABEL,™ CUPL,™ LOG/iC™ and PGADesigner.™ But that's where the similarity ends.



Fast. Fast. Fast.

Our FPGAs are real speed demons. Whatever application you may be working on, our parts will give you the kind of performance you're looking for.



100% Automatic Place And Route.

Coupled with your PLD tools, Actel's Action Logic™ System (ALS) software lets you create your own FPGAs—using a 386 PC or workstation—right at your own desk. With Auto Place and Route that's proven in thousands of applications.

Announcing A Simple Way To Get From PLDs To FPGAs.

If you're a PLD designer with an interest in fast, flexible FPGAs, but you think you don't have time to learn new design techniques, we'd like to change your mind.

First of all, you don't have to give up your existing PLD design tools or Boolean equations. Actel's ALES™ 1 program translates the output of PLD tools like CUPL™ and LOG/iC™ into logic optimized for our ACT™ devices. ABEL™ 4.0 includes optimization for Actel devices. Entire FPGA designs can be developed with PGADesigner.™

Actel devices offer everything you want in an FPGA. Like high I/O and flip-flop counts. And 100% automatic place and route gets you to market fast.

Once your FPGA is designed, our Action Logic™ System (ALS) converts the captured design into a completed device in minutes. To give you true, high-density, field-programmable, channeled gate arrays.

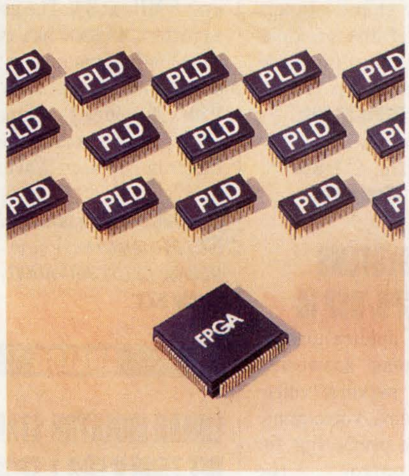
Other FPGA manufacturers fall short on design verification. Our exclusive Actionprobe® diagnostic tools, give you 100% observability of internal logic signals. So you don't have to give up testability for convenience.

It's never been easier to make your innovative designs a reality. We offer you a complete family of powerful FPGAs, like the A1010 and A1020, available in 44, 68 and 84 pin PLCC versions and implementing up to 273 flip-flops or up to 546 latches. And the first member of our ACT 2 family, the power-

GAs The Same Way
e Similarity Ends There.

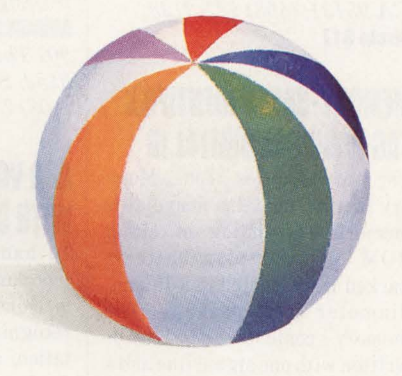
More Flexibility And Capacity.

Designing with Actel FPGAs gives you more freedom than you ever imagined. More gates. More flip-flops. More I/O. In fact, our new A1280 is the largest FPGA in the world.



Small Footprint.

Actel FPGAs give you far more gates per square inch. As much as ten times as many as the densest PLDs. That can save a lot of real estate.



More Fun.

Designing Actel FPGAs is so simple that you'll have more time to do the things that made you want to become an engineer in the first place. Or just relaxing. You've earned it.

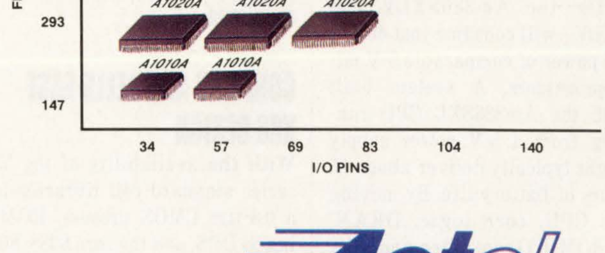
ful A1280. With 8,000 gates, up to 998 flip-flops, and 140 I/O pins, it's the highest capacity FPGA today. And our A1240-1 is the fastest. In the A1240-1, 16-bit counters run at 75 MHz, 16-bit accumulators at 33 MHz. Enough capacity and speed to handle almost any application.

The FPGA Design Guide

The superior speed, capacity, and auto place and route capabilities of our FPGAs are made possible by Actel's revolutionary PLICE® antifuse programming element. The advanced technology that makes our family of FPGAs an ideal way to unleash your engineering creativity.

Call **1-800-228-3532** for your free FPGA Design Guide.

Broad Family With High Capacity



Risk-Free Logic Integration

CIRCLE 80 FOR U.S. RESPONSE **CIRCLE 81 FOR RESPONSE OUTSIDE THE U.S.**

DIGITAL SEMICONDUCTORS

ns/pixel. Bit-block transfers (bitBLT) would go as fast as 18 ns/pixel. An upgraded system, using all five chips, would speed shading, hidden-surface removal, and pixel movement. *Electronic Design, March 28, p. 39.*

YAMAHA CORP. OF AMERICA, *Systems Technology Div., 981 Ridder Park Dr., San Jose, CA 95131; (408) 437-3133.*
Circle 617

MEMORY-BASED IDENTIFIER TAG PROVIDES DIGITAL ID

The DS199X series "Touch Memory family" contains nonvolatile memories consisting of either ROM or ROM plus battery-backed RAM, sealed in a 16-mm-diameter steel package. The memory's contents can be read or written with one signal line and a ground connection. The Touch Memory could serve as an identifier on a pc board or other product. However, unlike a bar code, the DS199X devices can be updated. Similar to a button-battery case, the steel shell has two isolated sections: one for ground and the other (the lid) for signal. On-chip data storage will range from 64 bits to 4096 bits—as much as 100 times the amount of data in a bar code. *Electronic Design, July 25, p. 153.*

DALLAS SEMICONDUCTOR CORP., *4401 South Beltwood Pkwy., Dallas, TX 75244-3292; (214) 450-0448.*
Circle 618

CONFIGURABLE 3-V CPU BOOSTS BATTERY LIFE

New 3-V versions of the Am386 CPUs—the Am386SXLV and DXLV—will consume just 45% of the power of comparable 5-V microprocessors. A system built with the Am386SXL CPU running from a 5-V power supply might typically deliver about 4.5 hours of battery life. By moving the CPU, core logic, DRAM, EPROM, I/O controller, and VGA controller to operate from 3-V power supplies, the battery life can be extended to about 6 hours. The new chips will also include an equivalent to the system-management mode (SMM) that Intel has in its SL version of the microprocessor. In addition, four new active-low signals—System Management Interrupt, SMI Address, SMI Ready, and I/O Instruction Break Fault—are added to the Am386 CPU pinout. However, they don't add new pins because the chip designers could use four of the previous CPU's no-connect pins. *Electronic Design, November 7, p. 119.*

ADVANCED MICRO DEVICES INC., *901 Thompson Pl., P.O. 3453, Sunnyvale, CA 94088; (408) 732-2400.* **Circle 619**

ADD VOICE TO SYSTEMS WITH COMBO CPU/DSP IC

To handle such applications as tape-less telephone answering machines, voice servers, voice-recognition systems, voice annotation, and voice prompting for appliance control, the NS32AM160 combines a core CPU from the company's 32000 series of general-purpose processors with a 16-bit integer vector subprocessor designed specifically for DSP applications. The chip also holds RAM and ROM, a real-time clock with 2-ms resolution, a watchdog timer, and an 8-bit pulse-width modulator. In addition, there are dual clock generators (for the active and standby modes), an interrupt controller, a dynamic-RAM controller, codec clock-generation and interface circuitry (for TP5512 or compatible codecs), and I/O lines. *Electronic Design, November 7, p. 129.*

NATIONAL SEMICONDUCTOR CORP., *2900 Semiconductor Dr., M/S 16-320, P.O. Box 58090, Santa Clara, CA 95052-8090; (408) 721-4429.*
Circle 620

CORE CPU AND CELLS EASE X86 DESIGN

With the availability of the V-series standard-cell libraries in a 0.8-μm CMOS process, ROM-based DOS, and the core 8088/86-compatible central processors, designers can roll their own custom DOS-compatible application processor. The processors are based on the V20 and V30HL core CPUs that form the heart of the V-series microprocessors. Processors using the core CPUs can run at voltages as low as 3 V and operate over the −40 to +85°C industrial-temperature range. The fully-static CMOS-logic CPU core draws 6 mA/MHz at 5 V, and 4 mA/MHz at 3 V. Its top frequency is 8 MHz at 3 V. The processors execute a 4-clock bus cycle and have a minimum instruction execution time of just 125 ns. Besides V20/V30 modes, the chips also include an 8088-emulation mode. *Electronic Design, November 21, p. 157.*

NEC ELECTRONICS INC., *401 Ellis St., Mountain View, CA 94039; (415) 960-6000.*
Circle 621

ANALOG

LINEAR ISOLATOR STANDS OFF 7500 V FOR 1 SECOND

The IL300 linear optocoupler, when combined with an op amp, produces an isolation amplifier with excellent linearity—better than 12 bits, for example, when coupled with an OP-07 class op amp. The isolator can withstand 7500 V ac peak for 1 second, or 6250 V ac peak for 1 minute at 60 Hz. Rise and fall times typically run 1.75 μs each. The device uses an infrared LED, which irradiates two p-i-n photodiodes: One diode supplies the output, while the second provides negative feedback to generate a control signal for the LED's drive current. *Electronic Design, January 10, p. 184.*

SIEMENS COMPONENTS INC., *19000 Homestead Rd., Cupertino, CA 95054; (408) 725-3543.* **Circle 622**

IC HOLDS 16 SECONDS OF AUDIO WITHOUT POWER

A solid-state device that essentially replaces magnetic tape as a direct analog recording medium employs an extension of EEPROM technology. Called direct analog storage (DAS), the device stores analog levels—samples of the input waveform—rather than binary bits in the memory cells. Signal-to-noise ratio is 40 dB, 3-dB bandwidth is 3400 Hz, and total harmonic distortion is 2% at 1 kHz. It stores 16 seconds of better-than-telecom-quality audio. After a signal is stored, the IC can be powered-down or removed from the circuit without losing the recorded signal. The chip is complete: If it's connected to 5 V with a microphone, a speaker, and a few other parts, you have a record-playback system. *Electronic Design, January 31, p. 39.*

INFORMATION STORAGE DEVICES INC., *2841 Junction Ave., Suite 204, San Jose, CA 95134; (800) 825-4473.*
Circle 623

PROCESS AND DESIGN BRING FAST, LOW-COST OP AMPS

Two types of fast, low-cost op amps—the LT1122 and the LT1190 family—result from improved non-complementary processes for linear ICs. The LT1190 family, built on a conventional (non-complementary) 18-V bipolar process, contains three video-bandwidth op amps and two video-bandwidth gain blocks with high-impedance differential inputs. The LT1120 FET op amp is constructed on a conventional 40-V bipolar process. It uses polysilicon to produce one of the fastest-settling op amps with a JFET input. Driving 1000 Ω, all five members of the LT1190 family slew at 450 V/μV, which translates into a full-power bandwidth of 24 MHz for a 6-V pk-pk output swing from a $\pm$5-V supply. *Electronic Design, February 14, p. 119.*

LINEAR TECHNOLOGY CORP., *1630 McCarthy Blvd., Milpitas, CA 95035; (800) 637-5545.*
Circle 624

ANALOG MULTIPLIER IC COVERS DC-200 MHZ

The EL2082 is a two-quadrant, current-mode multiplier that extends full-power bandwidth to 150 MHz while maintaining accuracy. The device uses current steering to achieve its wide signal bandwidth. Its front-end resembles that of a current-feedback amplifier. An input current between 0 and $\pm$1 mA produces

ANALOG

a linearly related output current of 0 to ±2 mA, ±0.4%. One resistor, connected between a voltage signal and the current input, converts the voltage signal to a current. Applying 0 to +2 V at the gain-control input varies the current gain through the chip from zero to maximum. The result is a gain-control range of at least 50 dB with a calibrated accuracy within 5%. *Electronic Design, February 28, p. 35.*
ELANTEC INC., *1996 Tarob Ct., Milpitas, CA 95035; (408) 945-1323, ext. 234.*
Circle 625

SINGLE-SUPPLY OP AMPS RUN OFF ONE RAIL EASILY

The TLE2425 sets up a virtual ground that allows an op amp, with its power pins connected between a positive supply rail and ground, to handle bipolar input signals—those that swing plus and minus with respect to ground. This 2.5-V, 20-mA voltage source also lets inverter-connected, single-supply op amps handle positive input voltages without clipping. The three-terminal TO-92 packaged IC, with its input pin connected to +5 V and the common pin to common, provides an output that's a well-regulated ±20 mA of 2.5 V—a virtual-ground reference of 2.5 V. *Electronic Design, April 11, p. 55.*
TEXAS INSTRUMENTS INC., *Literature Response Center, P.O. Box 809066, Dallas, TX 75380-9066; (214) 997-3389.*
Circle 626

20-BIT DELTA-SIGMA ADCs VIE FOR INTEGRATOR JOBS

Two companies have each come up with a family of delta-sigma converters for classic dc-measurement applications that can handle multiplexed inputs. Both Crystal Semiconductor's 16-bit CS5505/07 and 20-bit CS5506/08 delta sigmas and Analog Devices' 20-bit AD7710/11/12 easily provide sampled-data rates of 20 Hz. Application areas range from process control to laboratory and medical instrumentation to automatic test equipment and weighing scales. The AD7710/11/12 have added signal conditioning in the form of a programmable-gain amplifier and current sources for sensor excitation. Both families' low-power, single-supply requirement lend them to 4-to-20-mA process-control loops as well as portable instruments. *Electronic Design, April 25, p. 93.*
CRYSTAL SEMICONDUCTOR CORP., *P.O. Box 17847, Austin, TX 78760; (512) 445-7222.*
Circle 627
ANALOG DEVICES INC., *Application Engineering, 181 Ballardvale St., Wilmington, MA 01887; (617) 937-1428.*
Circle 628

INTEGRATOR IC CONVERTS PICOAMPERES TO VOLTS

The ACF2101, a switched integrator (the chip actually holds two identical integrators) is basically a form of sample-and-hold amplifier. The current source is connected to the summing point of a very low bias-current op amp operating as an integrator. The chip's 100-pF oxide capacitor integrates the input current. The IC was developed for the front-ends of CAT scanners that contain 500 to 1000 X-ray detectors. Each detector's output is a photodiode—a current source. Maximum full-scale current is 100 μA, and dynamic range with a fixed integration time is 120 dB. *Electronic Design, June 13, p. 132.*
BURR-BROWN CORP., *P.O. Box 11300, Tucson, AZ 85734; 1-(800) 548-6132, electronic bulletin board: (602) 741-3978 (300/1200/2400 8,N,1).*
Circle 629

LOW-VOLTAGE MICROPOWER OP AMPS COME OF AGE

Three different op amps now offer less speed, lower power, and the ability to operate from lower-voltage supply rails. The CMOS MAX406 from Maxim Integrated Products Inc. has a maximum quiescent current of just 1.2 μA. Advanced Linear Devices (ALD) Inc. offers the CMOS quad ALD4706 that needs just 50 μA per op amp. And from Signetics Corp. comes the NE5234, a bipolar quad that can slew at 0.5 V/μs, while needing a huge 700 μA of quiescent current per op amp. All three op amps work with potentials of less than 2 V between their plus and minus power-supply pins, making them ideal in various low-power applications. Each of the three op amps is unique and fills its own application niche. For example, the MAX406 op amp won't oscillate, regardless of load and capacitance. The ALD4706 op amp is a standard cell in an ASIC library. And the output signal from the NE5234 op amp doesn't invert when the common-mode voltage exceeds the power-supply rail. *Electronic Design, June 13, p. 135.*
ADVANCED LINEAR DEVICES INC., *1180F Miraloma Way, Sunnyvale, CA 94086-4606; (408) 720-8737* **Circle 630**
MAXIM INTEGRATED PRODUCTS INC., *120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600* **Circle 631**
SIGNETICS CORP., *811 E. Arques Ave., Sunnyvale, CA 94088-3409; (408) 991-4566.*
Circle 632

IC OP AMP USES ±175-V RAILS, PUTS OUT ±60 mA

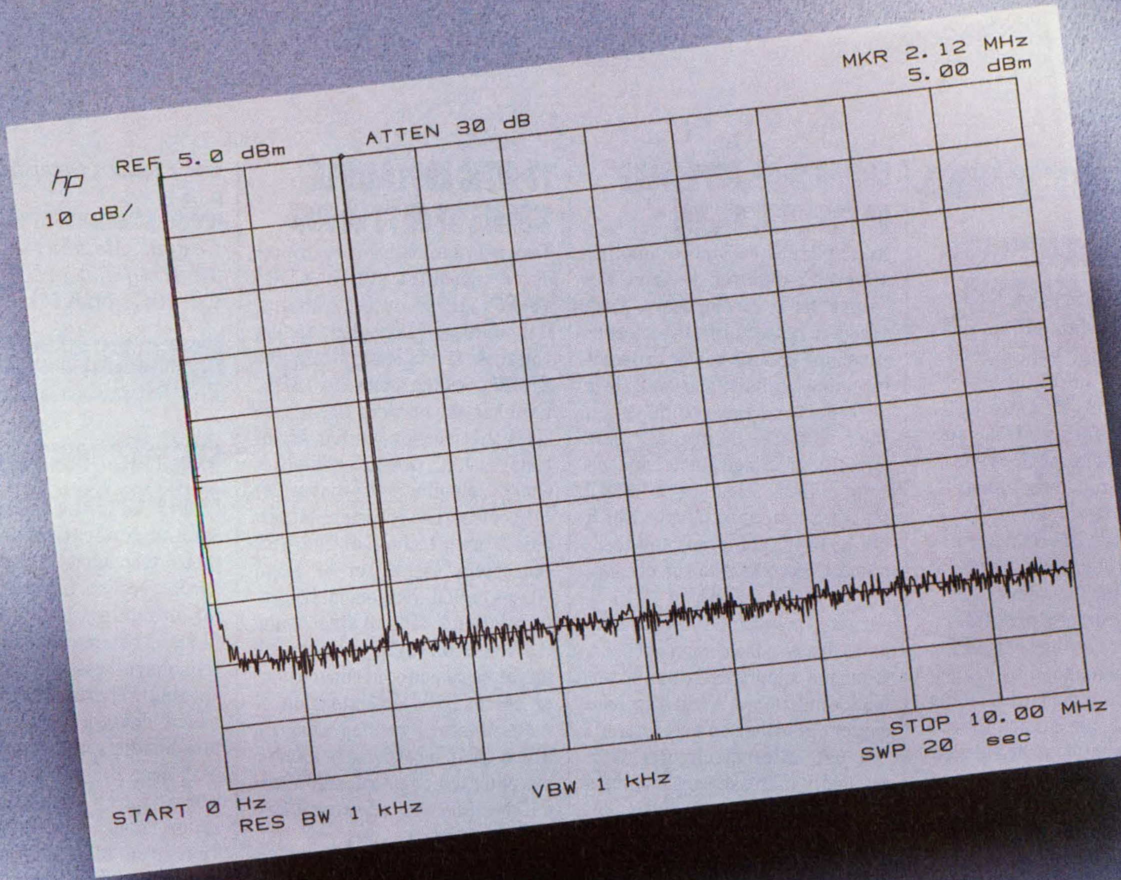
The PA41 is a high-voltage IC op amp that takes 350 V between its supply pins and swings its output within 12 V of both rails. It uses the AT&T high-voltage BCDMOS mixed-signal array, the ALA501, which is fabricated on a dielectrically isolated (DI) process. This process puts small-signal bipolar and CMOS devices on a chip with 350-V (operating voltage) DMOS transistors, and provides 1000 V of isolation between transistors with silicon dioxide. The PA41, which comes in a TO-3 package, puts out 60 mA continuously, and has a minimum open-loop gain of 94 dB. It was developed to drive piezoelectric micropositioners for small mirrors, which are used to aim and focus "Star Wars" laser beams. *Electronic Design, June 27, p. 47.*
APEX MICROTECHNOLOGY CORP., *5980 N. Shannon Rd., Tucson, AZ 85741; (602) 742-8600.* **Circle 633**

MIXED-SIGNAL CELLS USE BREADBOARD, SIMULATION

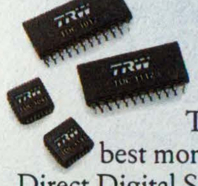
Each member of a family of CMOS ICs, which includes op amps, comparators, 555-type timers, and bandgap voltage references, is part of a growing mixed-signal standard-cell library that also includes standard CMOS logic, n-channel and p-channel MOS transistors, diodes, resistors, and capacitors. Users can start with a breadboard or with Spice simulation on a 286-based PC (preferably a 386-based PC), using the company's library of Spice macromodels. The models can be used with Spice for either of two purposes: to assist in the design of a low-volume or very simple circuit for pc-board mounting (using standard parts), or to assist in the design of a chip. *Electronic Design, July 25, p. 159.*
ADVANCED LINEAR DEVICES INC., *1180 Miraloma Way, Sunnyvale, CA 94086-4606; (408) 720-8737.* **Circle 634**

AIRBAGS BOOM WHEN IC ACCELEROMETER SEES 50 G

The need for a reliable, low-cost, 0-to-±50-g IC accelerometer to actuate automotive airbags spurred the development of the ADXL50. The device's sensor is built with surface micromachining and combines all of the signal-conditioning circuitry on the chip, which is just 120 mils on a side. The sensor consists of a variable differential air capacitor whose plates are etched from a 2-μm-thick polysilicon film. The capacitor plates are simple cantilever beams supported 1 μm above the chip, in free space, by polysilicon anchors. The accelerometer's proof mass (the effective mass whose inertia transforms an acceleration along an input axis into a force) moves relative to the rest of the chip when sensing acceleration. The sensor and circuit form a closed, force-balance feedback loop. *Electronic Design, August 8, p. 45.*
ANALOG DEVICES INC., *181 Ballardvale St., Wilmington, MA 01887; (617) 937-1426.*
Circle 635



WE'RE NOT ABOUT TO HAND YOU THE SAME OLD LINE.



TRW is proud to offer the highest performing line of synthesizer D/A converters: the TDC1041, TDC1141, TDC1012 and TDC1112. The absolute best monolithic D/A converters you can buy for Direct Digital Synthesis applications.

And just another example of the affordable, quality products that give TRW its legendary reputation for setting standards.

	12 Bit (high performance)	10 Bit (low cost version)
TTL, 20 Msps	TDC1012 SMD #5962-90596	TDC1041
ECL, 50 Msps	TDC1112 SMD #5962-91652	TDC1141

TRW's proprietary segmented architecture produces incredibly low glitch energy and quick settling time. With low data feedthrough, the result is a spurious free dynamic range as high as 80 dB.

And there's no need for output amplifiers. These D/A converters feature complementary current outputs, each of which drive 1 volt into doubly terminated 50 ohm loads.

The bottom line is that these D/A converters are available and ready to ship.

So when you need a D/A converter you can rely on for DDS, vector and raster graphics, or high resolution video applications, call or write:

TRW LSI Products Inc., P.O. Box 2472, La Jolla, CA 92038 (619) 457-1000, FAX (619) 455-6314 (800) **TRW-LSIP** (800) 879-5747

TRW

TRW LSI Products Inc.

STANDARDS SET. STANDARDS TO BE MET.

CIRCLE 168 FOR U.S. RESPONSE

CIRCLE 169 FOR RESPONSE OUTSIDE THE U.S.

ANALOG

13-BIT DATA-ACQUISITION IC SPORTS 32-WORD FIFO

The LM12458 data-acquisition IC digitizes eight analog voltages and puts out 12-bit-plus-sign words at 90 kHz, storing them in a 32-word FIFO memory. Ready-to-use, menu-driven software simplifies an analog designer's job of learning to "talk digital." The company's ADC1241, a 12-bit-plus-sign (13-bit resolution), sampling, self-calibrating analog-to-digital converter lies at the heart of the LM12458, surrounded by FIFO and instruction memories on the same chip. By permitting the ADC to convert up to 32 voltages without interrupting the host (for example, sequentially digitizing all eight inputs four times), the FIFO reduces the time the host spends servicing the DAS. *Electronic Design, September 26, p. 143.*

NATIONAL SEMICONDUCTOR INC., *2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; 1-(800) 272-9959.* **Circle 636**

8-BIT VOLTAGE-OUTPUT DACs SPORT 11-BIT RESOLUTION

A family of 8-bit voltage-output digital-to-analog converters, the ML2340/41 and ML50/51, give 11 bits of resolution and dynamic range. The key feature is that a 2-bit input word on the gain-control inputs sets the output op-amp gain at 1/4, 1/2, 1, and 2. Thus, changing the gain-control bits from 00 through 01 and 10 to 11 doubles the full-scale output voltage three times. Each doubling essentially adds a bit of resolution and dynamic range to give a final effective resolution and dynamic range of 11 bits. With a 30-ns maximum write time and no hold time, the DACs can keep up with the latest microprocessors. The DACs operate from a single power supply. *Electronic Design, October 24, p. 125.*

MICRO LINEAR CORP., *2092 Concourse Dr., San Jose, CA 95131; (408) 433-5200.* **Circle 637**

DOZING IC OP AMPS WAKE UP FOR INPUT SIGNAL

In applications where amplifiers aren't required to drive the output load continuously, they can save battery life if they consume just enough power to detect incoming signals, and shift to a high-performance mode when they detect a signal. The MC33102, a "Sleep Mode" dual op amp with a standard miniDIP pinout, represents the first of a family of ICs using this new technique. Guaranteed to run off supply rails from ± 2.5 to ± 15 V, each of the MC33102's two op amps draws a maximum of 65 μA from the supply rails under no-load conditions. When the load current of either op amp exceeds 200 μA, internal circuits automatically increase each op amp's operating current to 900 μA. Each op amp can then put ± 13.6 V of 20-kHz audio across 600 Ω without cross-over distortion. *Electronic Design, December 5, p. 49.*

MOTOROLA INC., *Bipolar Analog IC Div., EL340, 2100 E. Elliot Rd., Tempe, AZ 85284; (602) 897-3615, fax: (602) 897-4195.* **Circle 638**

VOLTAGE-CONTROLLED IC AMPLIFIERS SEEK NEW JOBS

Two voltage-controlled amplifiers focus on widely different applications. The SSM-2018 was developed for professional audio equipment, and the AD600/602 for ultrasonic (medical) scanners. The SSM-2018 controls signal levels from dc through the audio-frequency band, while the AD600/602 performs similar functions from dc to well beyond 35 MHz. A dc control voltage can change the gain of the SSM-2018 from −100 dB to over +40 dB. Similarly, a dc control voltage changes the input-to-output gain of both amplifiers in the AD600 from 0 dB to +40 dB and the gain of the amplifier pair in the AD602 from −10 to +30 dB. *Electronic Design, November 7, p. 122.*

ANALOG DEVICES INC., *Semiconductor Div., 181 Ballardvale St., Wilmington, MA 01887; (617) 937-2508.* **Circle 639**

12-BIT IC ADCs SAMPLE SIGNALS AT UP TO 20 MHZ

Two companies have each produced monolithic 12-bit ADCs: The SPT7912 produces 12-bit digital words of sampled analog voltages at 20 MHz, while the AD872 does the same at 10 MHz. Each has one or more 10-bit versions that employ similar architectures. Both converter families employ pipelined, multistep architectures. The proprietary (patented) architecture of the SPT converters use a set of algorithms called "trigonometric interpolation." The 3-step/4-step (10-bit/12-bit) ADI architecture might be considered conventional because it's an extension of most present two-step designs, although it incorporates numerous patented circuit-design innovations. *Electronic Design, October 24, p. 47.*

SIGNAL PROCESSING TECHNOLOGIES INC., *1510 Quail Lake Loop, Colorado Springs, CO 80906; (719) 540-3900* **Circle 640**

ANALOG DEVICES INC., *181 Ballardvale St., Wilmington, MA 01887; (617) 937-1297.* **Circle 641**

LINEAR ICS ATTAIN 8-GHZ NPNs, 4-GHZ PNPs

The first commercial linear ICs to be built by direct wafer bonding, one of the newer silicon-on-insulator (SOI) technologies, are based on a new UHF complementary-bipolar IC technology called UHF-1. It features vertical npn transistors sporting f_ts of 8 GHz, while f_ts of its vertical pnp siblings attain a high of 4 GHz. The company has also created an analog array family and an analog cell library on the wafer-bonded UHF-1. The HFA1100/1120/1130 op amps are unity-gain-stable current-feedback IC op amps, attaining the fastest speeds for a monolithic device. They feature a 2500-V/μs typical slew rate, 850-MHz 3-dB bandwidth, and 11-ns settling time to 0.1% for a 2-V step. A fourth device is the HFA1110 closed-loop buffer, which aims at applications similar to those of the op amps and has similar specifications. *Electronic Design, December 19, p. 35.*

HARRIS SEMICONDUCTOR, *P.O. Box 883, Melbourne, FL 32901; 1-(800) 4-HARRIS, ext. 1047.* **Circle 642**

COMPUTER-AIDED ENGINEERING

SYNTHESIS TOOLS COMPLETE FRONT-TO-BACK EDA SYSTEM

Second-generation logic-synthesis technology completes Cadence Design Systems' toolset for designing ICs, ASICs, and PLDs. The Improvisor and Optivisor synthesis tools, developed as integral parts of a framework-based design-automation system, handle synthesis of designs with over 20k gates and use one library for all simulation, verification, and analysis functions. They also allow timing-driven constraints throughout the entire design cycle. The tools are integrated into the company's Amadeus System Design Series and Opus IC Design Series, operating under the Design Framework II. *Electronic Design, February 28, p. 91.*

CADENCE DESIGN SYSTEMS INC., *555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234.* **Circle 643**

HARDWARE, SOFTWARE SIMULATORS BLEND

Although workstation MIPS ratings are increasing, simulations aren't getting faster because of the limitations of the workstations' cache architectures. A hardware accelerator helps alleviate this bottleneck. The XLProcessor (XLP) is a gate-level accelerator that implements Cadence's XL simulation algorithm in hardware. The XL algorithm powers gate-level simulation in the company's Verilog-XL and VHDL-XL software simulators. XLP can handle designs with up to 1 million gates, and operates at up to 2 million events/s. *Electronic Design, May 23, p. 133.*

CADENCE DESIGN SYSTEMS INC., *555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234.* **Circle 644**

COMPUTER-AIDED ENGINEERING

OPTIMIZE AND RETARGET EXISTING LOGIC DESIGNS

Engineers often need to merge PLDs and standard logic, then retarget the combination into an ASIC. An optimization and remapping tool called Retargeter can simplify that process. The tool can, for instance, merge several existing logic designs, determine the function the group was performing, optimize the design, and retarget that same logic into a field-programmable gate array (FPGA) or an ASIC. It accepts designs as existing net lists (also called wire files), standard EDIF net lists, and PLD JEDEC files. *Electronic Design, May 23, p. 135.*

VIEWLOGIC SYSTEMS INC., *293 Boston Post Rd. West, Marlboro, MA 01752; (508) 480-0881.* **Circle 709**

SPREADSHEET-LIKE TOOL EASES VHDL PROGRAMMING

In the Humtable, a spreadsheet-like tool used to create VHDL models, the first and second columns are the control and object columns. Words in the control column (such as when, and, if) determine whether or not the identifiers in the object column (clk, SO) are control objects or assignment objects. Identifiers or operators in the remainder of the columns define conditions that produce a result assigned to the identifier in the object column. Events are "read" down each column. Humtables are expanded into a native Hum language called Humbase, which is less elegant than VHDL, but easier to use. *Electronic Design, March 14, p. 109.*

LEWIS SYSTEMS INC., *1915 Peters Rd., Suite 113, Irving, TX 75061; (214) 438-2177.* **Circle 645**

TOP-DOWN VHDL TOOLS TAKE GRAPHIC, TEXT INPUTS

A top-down design environment, Logic Workbench TD, performs mixed behavioral-and structural-level simulation of digital ASICs and systems. The design system offers a suite of tools, including an interactive VHDL simulator. A major component is Concept, a compound-capture design-entry tool that gives engineers the flexibility to mix textual and graphical descriptions of their designs at the behavioral, RTL, or structural level in the form of VHDL, block diagrams, truth tables, state machines, or schematics. *Electronic Design, July 11, p. 155.*

VALID LOGIC SYSTEMS, *2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400.* **Circle 646**

SOFTWARE ANALYZES IMPACT OF LAYOUT ON HF BOARDS

The Visula High-Performance Engineering (HPE) software helps analyze the impact of physical layout on high-speed board designs. HPE can directly control the layout process from design rules that govern critical factors, such as path delays, reflection, and crosstalk limits, accounting for pin ordering, impedance characteristics, and route spacings. Entry of critical design parameters controls routing of the board according to such key constraints as minimum and maximum delay per net and crosstalk between nets. The toolset runs on DEC, HP/Apollo, and Sun workstations. *Electronic Design, August 8, p. 124.*

RACAL-REDAC INC., *1000 Wyckoff Ave., Mahwah, NJ 07430; (201) 848-8000.* **Circle 647**

GRAPHICAL DESIGN CAPTURE, MODELING EASE DESIGN

Designers using Analogy's Saber simulator can quickly create schematics and simulation models in a graphical environment with DesignStar. It provides menus, drawing commands, and output formats tailored to analog designs. Voltages and values created during simulation are back-annotated to the schematic for easy access and viewing. The system works with other design software by exporting and importing symbols and drawings through the company's graphical EDIF interface. An analog-HDL model generator eases the creation of simulation models. Pop-up menus provide a means to enter the function of components in standard math equations. *Electronic Design, September 12, p. 182.*

ANALOGY INC., *9205 S. W. Gemini Dr., Beaverton, OR 97005; (503) 626-9700.* **Circle 648**

SOFTWARE WARNS OF MANUFACTURING SNAGS

Engineers can have better control over product cost, quality, and delivery with a tool that alerts users to downstream effects of early design decisions regarding manufacturing. Manufacturing Advisor/PCB identifies parts-related manufacturing problems in pc boards. It also offers a manufacturability "score" in an environment that allows for what-if analysis to test the effect of recommended design alternatives. As components are added, the tool monitors the consumption of placement area. If exceeded, it identifies components that could be mounted in an alternate configuration with a smaller footprint. *Electronic Design, October 10, p. 140.*

MENTOR GRAPHICS CORP., *8005 S. W. Boeckman Rd., Wilsonville, OR 97070-7777; (800) 547-3000.* **Circle 649**

BUILD MIXED-SIGNAL ASICs WITHOUT ANALOG CELLS

A combination of software and silicon called the MSDS (Mixed-Signal Design Solution) lets system designers create a high-performance mixed-signal CMOS ASIC with on-chip testability that's added prior to layout. With the system, the mixed-signal design process more closely resembles digital design. Designers can incorporate custom analog functions into the design and simulate those functions to ensure that they work as specified. The analog functions supported include: filters, oscillators, bandgap references, inverting and noninverting gain stages, voltage regulators, comparators, data converters, and multiplexers. *Electronic Design, September 12, p. 163.*

GOULD AMI, *2300 Buckskin Rd., Pocatello, ID 83201; (208) 234-6679.* **Circle 650**

VHDL DESIGN TOOLS SPAN SPECIFICATION TO TEST

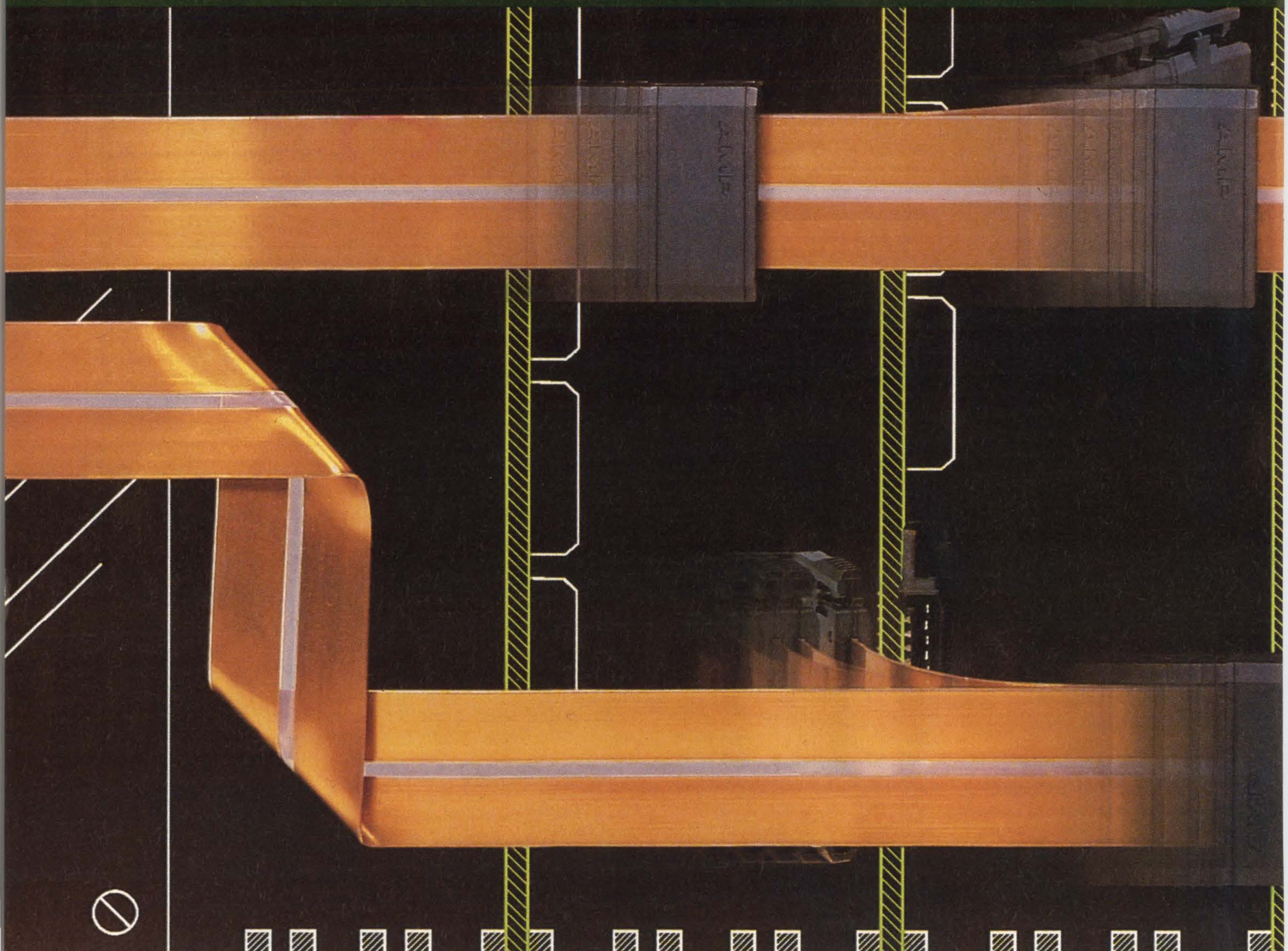
The ASIC Navigator Design System aims at giving users first-time success in both ASICs and systems. ASIC Navigator consists of four components: Logic Assistant, Design Assistant, ASIC Synthesizer, and Test Assistant. With Logic Assistant, users can describe designs in high-level capture methods, including block diagrams, Boolean expressions, bubble diagrams, VHDL, and Verilog statements. Logic Assistant then converts the specification into behavioral VHDL code. Design Assistant evaluates users' partitioning and, for each ASIC and process technology, provides an estimated die size, various packaging options, power consumption, and estimated gate count. ASIC Synthesizer creates random logic and state machines, compiles all of the data paths in the design, and synthesizes the exact-size memory that users specify. Test Assistant helps users select a test architecture for the test strategy, and synthesizes the necessary structures and connects them within the design. *Electronic Design, November 21, p. 167.*

COMPASS DESIGN AUTOMATION INC., *1865 Lundy Ave., San Jose, CA 95131; (408) 434-7943.* **Circle 651**

ONE TOOLSET CREATES FPGAs IN ANY TECHNOLOGY

A set of device-independent FPGA CAD tools, called FPGA Foundry, support technology-transparent design, which is designing without targeting a specific architecture implementation during schematic capture. FPGA Foundry includes a timing estimator, circuit optimizers, device mappers, timing-driven automatic place-and-route capability, a graphical editor, back-annotation, and report-file generation. The tools are built on a device-independent data struc-

Putting high-performance power distribution on the fast track.

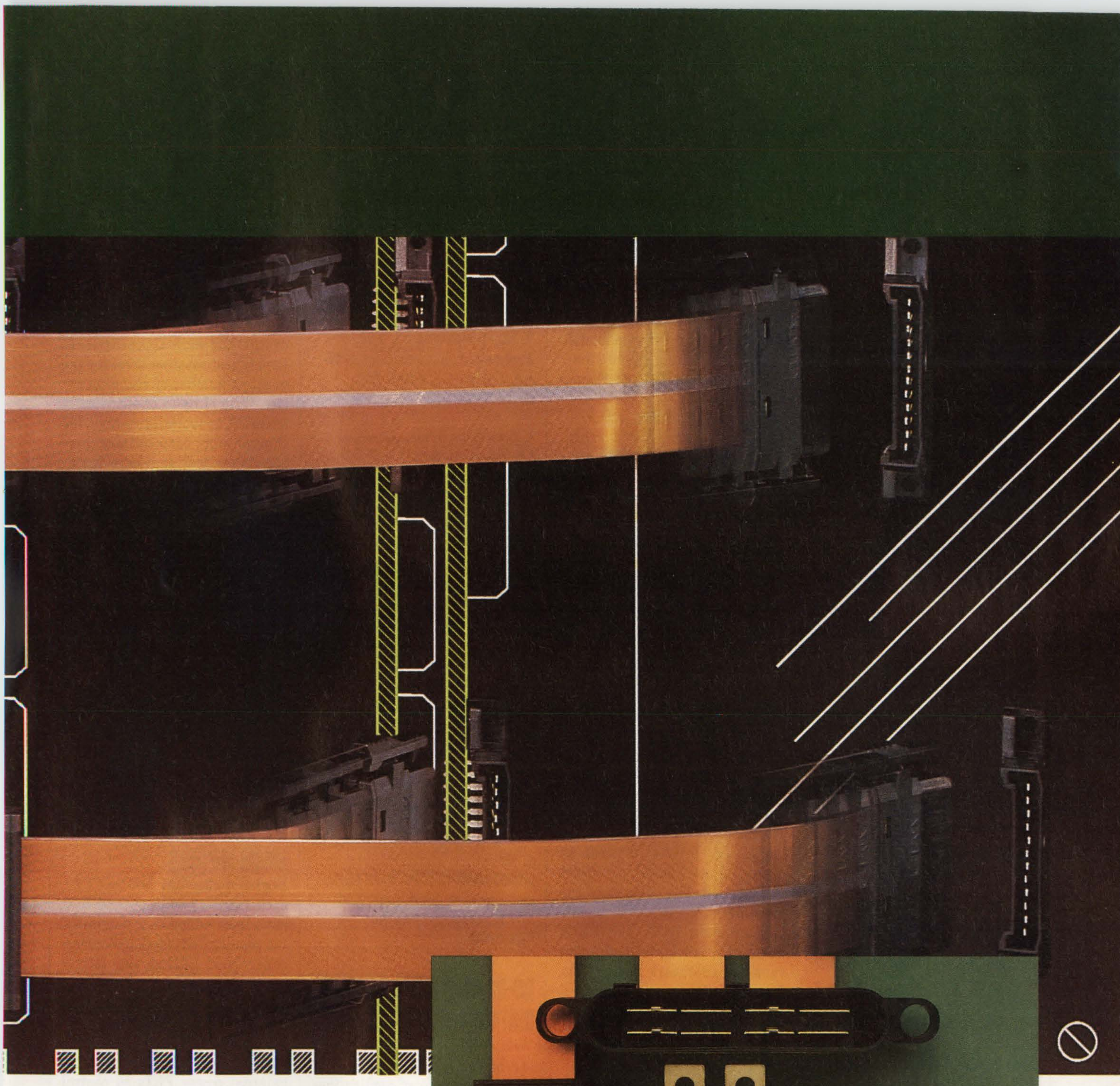


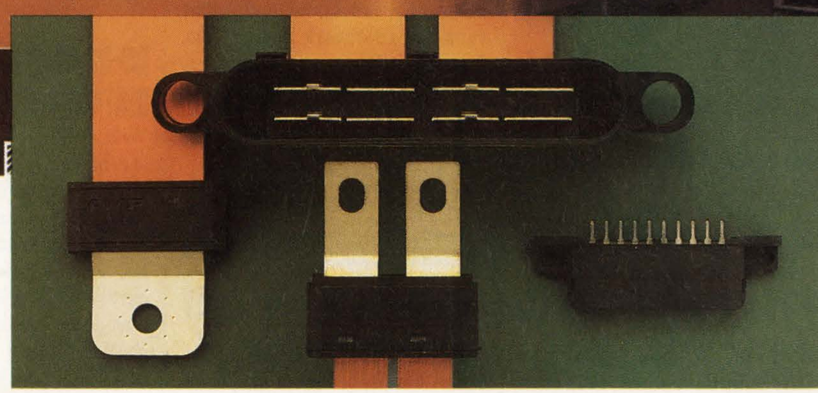
THIS IS AMP TODAY.

Designers of today's high-performance power distribution systems (PDSs) need a practical way to take advantage of the compact size, thermal efficiency, and low inductance of insulated flat copper power cable.

Our newest invention not only makes flat conductors practical, it adds powerful new options to the way you can design your 'flat power' PDS.

AMPOWER Wave Crimp





COMPUTER-AIDED ENGINEERING

ture, which lets them support multiple device architectures while still supporting device-specific features. A software backplane uses a hierarchy of algorithms, cost tables, and routines to perform device-independent place-and-route routines without sacrificing performance or functionality. *Electronic Design, December 5, p. 129.*
NEOCAD INC., *2585 Central Ave., Boulder, CO 80301; (303) 442-9121.* **Circle 652**

HARDWARE ACCELERATOR SPEEDS VHDL SIMULATION

A VHDL simulation accelerator combines the features and flexibility of a software simulator with higher speed and capacity. It accepts VHDL source code as input, and supports about 90% of the language's constructs. The product accelerates simulation speed by 100 to more than 1000 times, depending on the design's size. In addition, the accelerator can go to 50,000 or 100,000 lines of code. Users can set breakpoints on statements, or breakpoint on variable values. They can also trace variables and signals, display traces, single-step, and do all of the things expected from the source-level debug capabilities, user interface, and simulator control of a software simulator. *Electronic Design, June 13, p. 54.*
IKOS SYSTEMS INC., *145 N. Wolfe Rd., Sunnyvale, CA 94086; (408) 245-1900.* **Circle 653**

SPEED VME BOARD DESIGNS THROUGH SIMULATION

With SimuBus, which can simulate a VMEbus and the stimuli that appears on the bus, designers can simulate board operation and also set up a system environment that represents a standard bus in order to build an interface. They also can set up a system-level model for other boards in the system to obtain the bus cycles for those boards. The system may include other boards, such as masters or slaves, on the bus. By setting up this type of environment, a system atmosphere can be created where programmable delays or several different types of boards can be added. SimuBus is controlled by a processor control-language (PCL) file input. PCL uses a C-like language, so designers can do simple modifications to create a given stimulus. *Electronic Design, November 7, p. 133.*
LOGIC AUTOMATION INC., *19500 N.W. Gibbs Dr., Beaverton, OR 97006; (503) 690-6900.* **Circle 654**

SOFTWARE MANAGES CONCURRENT ENGINEERING

TeamNet 2.0 is a software system that supports distributed, concurrent product development across heterogeneous networks. The software supplies designers and project managers with the real-time information and control they need to manage a concurrent design project. Such disciplines as engineering, marketing, manufacturing, and testing can use the system during all stages of the product life cycle. The TeamNet 2.0 software is a Unix-based product that can be hosted on any Sun Microsystems workstation. The tools may run on Unix-based systems, Macintosh systems, DOS- and OS/2-based PCs, and any computer that runs Sun's Network File System. *Electronic Design, January 10, p. 189.*
TEAM ONE SYSTEMS INC., *2700 Augustine Dr., Santa Clara, CA 95054; (408) 986-9191.* **Circle 655**

POWER

2-KW DC SWITCHING SUPPLY BANISHES NOISE AT OUTPUT

Common-mode switching noise often corrupts switching preregulated supplies' outputs. Higher-order common-mode filtering helps mitigate the problem in a pair of 2-kW system dc power supplies. The HP6671A and HP6674A supplies offer the efficiency and compactness of a switching-based power mesh. Outputs are rated at 0 to 8 V and 0 to 220 A for the HP 6671A, and at 0 to 60 V and 0 to 35 A for the HP 6674A. Each has a built-in GPIB interface. Normal-mode noise, which usually is about 50 mV pk-pk maximum for a switching supply, is specified at 7 mV pk-pk for the HP6671A, close to that of a pure linear supply's. *Electronic Design, January 31, p. 111.*
HEWLETT-PACKARD CO., *19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.* **Circle 656**

PHASE MODULATION CUTS LARGE-SWITCHER LOSSES

A controller IC, the ML4818, uses a new topology—phase modulation—to boost efficiency and cut size and cost for 250- to 2500-W switchers. Phase modulation involves zero-voltage switching; the MOSFET switch's drain-to-source voltage is zero when the gate of each n-channel FET is driven positive to turn it on. ML4818, which can operate to over 1 MHz, typically increases the power density of today's switchers by at least 50%. By changing topologies, for example, a 400-W supply now switching at 100 kHz can move to 500 kHz. *Electronic Design, April 25, p. 39.*
MICRO LINEAR CORP., *2092 Concourse Dr., San Jose, CA 95131; (408) 433-5200.* **Circle 657**

DC-DC CONVERTER HANDLES DISTANT 200-A/μS LOADS

With system-clock speeds climbing beyond 50 MHz, and an increasing number of applications featuring pulsed-load current slew rates that exceed 5 to 100 A/μs, today's power supplies can hardly keep up. A family of modular dc-dc converters called TachoMods, based on Vicor's earlier VI-200 family, guarantee that during a 10-to-90% load change, at 200 A/μs, the maximum voltage deviation at the point of load is less than $\pm$5%. The TachoMods eliminate the effects of parasitic inductances by removing capacitance from the converter's output filter. *Electronic Design, May 9, p. 59.*
VICOR CORP., *23 Frontage Rd., Andover, MA 01810; (508) 470-2900.* **Circle 658**

ENERGY-MANAGEMENT CHIP AIDS PC POWER-CONTROL ICs

The bq2001 energy-management unit, a 24-lead biCMOS chip, is a battery-system manager for portable PCs. It determines battery capacity and available charge, and maintains capacity at the highest possible level for the greatest number of recharge cycles. With 11 bytes of electrically erasable, nonvolatile storage, the chip can store basic battery characteristics that can be overridden or rewritten if system characteristics change. The chip operates as a standalone controller when powered directly from a system's dc-charging supply, or as a microprocessor peripheral when it uses the 5-V logic supply. The chip works with battery stacks having nominal voltages of 4.8 to about 12 V. *Electronic Design, June 27, p. 125.*
BENCHMARQ MICROELECTRONICS INC., *2611 Westgrove Dr., Ste. 101, Carrollton, TX 75006; (214) 407-0011.* **Circle 659**

MICROCONTROLLER POWERS SMALL MOTORS

Eight n-channel DMOSFETs, each rated at 300 mA and 6 V, have been added to a version of the popular 68HC05 CMOS microcontroller. Called the model 68HC05H2, the chip opens up new applications by adding power to control—in driving lamps, relays, and small motors, for example. Moreover, the chip can drive external power FETs to control higher voltages and/or currents. In a 44-pin plastic leaded chip carrier, each of the chip's eight power devices can carry up to 300 mA continuously and switch a maximum of 6 V. The current rating drops to 200 mA in a 40-pin plastic DIP or a 42-pin plastic SDIP (a shrink-DIP with the pins on 70-mil centers). Four of the power devices can be on at once to control up to 7.2 W.*Electronic Design, July 11, p. 149.*
MOTOROLA INC., *CSIC Microcontroller Div., 6501 William Cannon Dr., MS OE39, Austin, TX 78735-8598; (512) 891-2035.* **Circle 660**

POWER

ICs BUILD OFF-LINE ISOLATED SWITCHERS

A pair of controller ICs, the LT1103 and LT1105, together build a 100-W, universal, off-line switching-regulator supply with 1% line and load regulation. All that's needed besides the IC are a power MOSFET, a transformer, diodes, and a handful of passive parts. No negative feedback is required across the isolation barrier from output to control circuitry. The controllers can handle voltages limited only by the rating of the power FET. FETs of 1000-V are now available. The LT1103 is rated for control of up to 100 W of power. *Electronic Design, August 22, p. 35.*

LINEAR TECHNOLOGY CORP., *1630 McCarthy Blvd., Milpitas, CA 95035-7487; (408) 432-1900.* **Circle 661**

ICs LEVEL-SHIFT 3-PHASE MOTOR-DRIVE PWM –500 V

A high-voltage motor-drive chip contains just seven pnp transistors, two Zener diodes, and three resistors in an innovative circuit topology. The chip's 20-pin skinny DIP holds only 15 pins, allowing the high-voltage input pins to be spaced wider apart. Thus, those pins can handle 115- or 230-V ac line voltage. When used with two other ICs and power MOSFETs or insulated-gate bipolar transistors (IGBTs), the chip simplifies the drive and speed-control requirements of 1/3-to-1-horsepower brushless dc motors. The new IC comes in two versions: the MDC2125 and the MDC2150. They are differentiated by voltage ratings of 250 V and 500 V, respectively. *Electronic Design, October 10, p. 112.*

MOTOROLA INC., *Discrete & Materials Technology Group, MD Z201, 5005 E. McDowell Rd., Phoenix, AZ 85008; (602) 244-3810.* **Circle 662**

SURFACE-MOUNT 2-W DC-DC CONVERTER SAVES SPACE

The industry's first surface-mounted 2-W dc-dc converter, the PM6501/02, measures just 0.337 in. high by 1.100 in. long by 0.850 in. wide. It replaces a through-hole part that measures 0.475 by 1.3 by 0.8. The SMT part is a full-featured converter for the local-area-network market. Its 9-V output powers the coaxial-transceiver interface IC in Ethernet and Cheapernet applications. The converter's switching frequency is 1.2 MHz, which makes headroom for monolithic ceramic capacitors of just 0.1 μF. *Electronic Design, September 26, p. 172.*

VALOR ELECTRONICS INC., *6275 Nancy Ridge Dr., San Diego, CA 92121-2245; (619) 458-1471.* **Circle 663**

TEST AND MEASUREMENT

DIGITAL SCOPES AIM AT CONFIRMED ANALOG USERS

Two 100-MHz portable digital scopes, the HP 54600A (two channels) and HP 54601A (four channels), take direct aim at analog-user holdouts. With front panels similar to those on analog scopes, the instruments have dedicated knobs to adjust vertical sensitivity, position, time base, horizontal delay, trigger level, and hold-off. Buttons control storage, measurement, and utility functions. Other specs include a 20-Msample/s sampling rate with 8-bit vertical resolution and peak-detection capability; vertical sensitivity of 2 mV to 5 V/div.; and edge, line, and TV triggering. *Electronic Design, March 14, p. 105.*

HEWLETT-PACKARD CO., *Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80901-2197; (800) 752-0900.* **Circle 664**

ICON-BASED SOFTWARE EASES TEST PROGRAMMING

Object-oriented, icon-based programming tools let designers concentrate more on the test at hand and less on programming. The visual engineering environment (VEE) software frees users from the need to know high-level-language syntax, semantics, or rules. Designers link icons into an intuitive block diagram on the display, and the software executes the block diagram. HP VEE-Engine, general-purpose software, analyzes and presents data that has been either collected from a file or generated mathematically. HP VEE-Test, for instrument control, allows data collection from more than 170 HP instruments, as well as from non-HP instruments through direct I/O elements. *Electronic Design, May 9, p. 140.*

HEWLETT-PACKARD CO., *Measurement Systems Operation, P.O. Box 301, Loveland, CO 80539; (800) 752-0900.* **Circle 665**

SCOPES COMBINE DIGITAL POWER WITH EASE OF USE

Digging through multilevel menus can be a chore for designers debugging their latest handiwork. By including an intuitive graphical interface, a pair of full-featured, mid-range digital scopes that introduce the Tektronix Digitizing Scope (TDS) platform are easier to use. The platform is a high-speed acquisition system with advanced triggering and a multiprocessor architecture. In addition, the TDS520 and TDS540 have a 640-by-480 VGA display. The scopes feature a 500-MHz bandwidth, 8-bit vertical resolution, 1% accuracy, and 4-ns glitch capture. The TDS520 digitizes signals at 250 Msamples/s on two channels or 500 Msamples/s on one channel. The TDS540 samples from 250 Msamples/s on four channels to 1 Gsamples/s on one channel. *Electronic Design, June 27, p. 131.*

TEKTRONIX INC., *P.O. Box 19638, Portland, OR 97219-0638; (800) 426-2200.* **Circle 666**

50-MHZ DSO MELDS WITH FULL-FEATURE DMM

A 50-MHz, 25-Msample/s dual-channel digital storage oscilloscope (DSO) is combined with a feature-rich digital multimeter (DMM) and even a limited-function signal source. The 90 Series handheld ScopeMeter's DSO captures waveforms in real-time or equivalent-time sampling modes. In real-time, the 25-Msample/s rate delivers a 40-ns timing resolution. For repetitive signals, the equivalent-time sampling mode allows 400-ps resolution. Rise time is 7 ns, vertical resolution is 8 bits, and record length is 512 samples. The 240-by-240-pixel, 5-in. supertwist LCD screen displays up to four waveforms. *Electronic Design, September 12, p. 167.*

JOHN FLUKE MFG. CO. INC., *P.O. Box 9090, Everett, WA 98206; (206) 347-6100* **Circle 667**

PHILIPS TEST AND MEASUREMENT, *Bldg. TQIII-4 5600 MD, Eindhoven, The Netherlands.* **Circle 668**

TEST STATION DELIVERS ATE-LIKE PERFORMANCE

A new test station, Logic Master ATS, delivers the accuracy and performance of traditional mainframe automated test equipment (ATE) at a fraction of the cost. Clock speeds go to 200 MHz and data rates to 400 Mbits/s. Edge placement is within 50 ps, and accuracy of up to ±100 ps is possible. Other features include programmable slew rates and current loads. Working with a Sun SparcStation host, the system performs digital tests on standard ICs, ASICs, and multichip modules, primarily for low-volume production. *Electronic Design, October 10, p.118.*

INTEGRATED MEASUREMENT SYSTEMS INC., *9525 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-7117.* **Circle 669**

PORTABLE DSO FEATURES 10-BIT RESOLUTION

With its dual 10-bit, 100-Msample/s ADCs, the LeCroy 9430 portable oscilloscope is suitable for a wide range of precision measurement applications. Using its capabilities, operators can increase resolution eightfold (from 10 to 13 bits). And dc accuracy is within a state-of-the-art 1%. Each of the 9430's two channels has a nonvolatile, 50k acquisition memory. These very long memories permit high sample rates on slow time-base settings, as well as horizontal expansion of up to 1000 times. As a result, users can

TEST AND MEASUREMENT

closely examine short-duration glitches. Menus help users call up standard waveform-processing routines, including arithmetic functions and summation averaging. The 9430 also performs 10 standard pulse-parameter measurements. *Electronic Design, January 10, p. 187.*

LECROY CORP., *ITI Div., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 578-6097.* **Circle 670**

DATA-ACQUISITION PACKAGE WORKS WITH 386, 486 PCs

The Viewdac data-acquisition, analysis, and graphics software package takes advantage of 80386- and 80486-based personal computers. A windowing environment makes the software easy to use and increases the operator's efficiency. The software's multitasking capabilities enable users to easily switch from one application to another, and they can acquire, graph, tabulate, manipulate, or create data that other applications are running. Post-acquisition processing can be handled by the built-in interactive data-analysis and graphics functions. Numerous data-acquisition boards are supported, including those from Keithley DAC, Keithley MetraByte, Analog Devices, Burr-Brown, Data Translation, and Markenrich. *Electronic Design, January 10, p. 187.*

KEITHLEY ASYST, *100 Corporate Woods, Rochester, NY 14623; (800) 348-0033 or (716) 272-0070.* **Circle 671**

PULSE GENERATOR FEATURES MODULAR FLEXIBILITY

The Model 9210 GPIB-programmable pulse generator accepts two plug-in output modules with varying combinations of repetition rates, edge-transition times, and output swings. Maximum time resolution is 10 ps with a time-base accuracy of $\pm$(0.5% + 0.2 ns). Amplitude resolution is 5 mV with a dc accuracy of 1%. The Model 9211 output module has a maximum repetition rate of 250 MHz, edge times from 1 ns to 1 ms, and a 5-V pk-pk output into 50 Ω. The Model 9212 features a maximum repetition rate of 300 MHz, edge times from 300 ps to 1 ns, and a 5-V pk-pk output. Operators can set and change parameters using soft keys and menus on a touch-screen CRT, or they can use a numeric keypad and rotary knob. *Electronic Design, April 11, p. 151.*

LECROY CORP., *Signal Sources Div., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 578-6020.* **Circle 672**

EMBEDDED VXI CPU OFFERS RT DISTRIBUTED CONTROL

With the VXIcpu-030 embedded controller, designers can develop distributed VXI systems with real-time control capability. They can also network VXI mainframes with standard worksta-

Looks like you could use our new

Let's face it. When you pick a new microprocessor that takes performance to new heights, it's only natural to wonder what support you'll have.

The EL 3200 is the only completely integrated development system for the i960 CA microprocessor.

Not to worry. Because Applied Microsystems has everything you need to develop your embedded system now. So you'll be up and running to meet tight schedules.

Intel supports us supporting you.

They asked us to back their robust i960™ CA microprocessor with a high

TEST AND MEASUREMENT

tions, PCs, file servers, and terminals. The module is a one-slot, C-size, 68030-based controller that runs the VxWorks real-time operating system from Wind River Systems, Alameda, Calif. The VXIcpu-030 offers complete VXI functionality, GPIB control, and Ethernet capability, and comes with 2 Mbytes of shared RAM. A SCSI port and two serial ports are provided. Options available include eight additional serial ports, an internal hard-disk drive, a 68882 floating-point coprocessor, and extended RAM. It can also act as a message-based commander with full resource-manager capability. *Electronic Design, June 27, p. 156.*
NATIONAL INSTRUMENTS INC., *6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100.*
Circle 673

TIMING LOGIC ANALYZER BOASTS 1-NS RESOLUTION

Designed for hardware debugging, the K1000 portable timing logic analyzer features data-capture rates to 1 GHz, which translates to 1-ns resolution on single-shot timing measurements. The 16-channel analyzer has a 2-ksample data capture memory and a channel-to-channel skew of less than 1 ns. Active probes with a 500-MHz bandwidth ensure that the unit can capture pulses as narrow as 1 ns. The probes' 1-MΩ, 5-pF input impedance allows a 6-ft.-long probe-to-instrument cable. With the K1000's two-level triggering, users can identify a sequence of patterns even if each pattern exists only for 1 ns. Pattern detection is performed by two independent 16-channel, 1-ns word recognizers. *Electronic Design, July 25, p. 171.*
BIOMATION CORP., *19050 Pruneridge Ave., Cupertino, CA 95014; (800) 538-9320.*
Circle 674

FIVE PROCESSORS BOOST DMM'S PERFORMANCE

Microprocessors in test instruments are commonplace—many units have one, two, or three devices controlling operations. However, a new digital multimeter uses five processors to give it an excellent combination of resolution, accuracy, sensitivity, and speed. The Model 2001, housed in a half-rack-size package, performs many measurements other DMMs don't make or don't make directly, such as ac crest factor, peak spikes, and ac peak, average, and true-RMS values. The ac bandwidth is 2 MHz, while a separate frequency measurement capability works to 15 MHz. Users can select 4-1/2- to 7-1/2-digit resolution. Unlike some DMMs, which average multiple 6-1/2-digit readings to extend resolution to 7-1/2 digits, the Model 2001 has true 7-1/2-digit, 28-bit capability. *Electronic Design, December 5, p. 133.*
KEITHLEY INSTRUMENTS INC., *28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115 or (216) 248-0400.*
Circle 675

COMPUTERS

RUN UNIX AND DOS ON SAME 486-BASED PLATFORM

The 33-MHz 486-based Voyager platform runs both DOS and Unix, performing applications under either operating system concurrently, without sacrificing any speed or computing power. The pizza-box-shaped chassis features 8 Mbytes of RAM expandable to 64 Mbytes, 256 kbytes of second-level cache memory, a 64-bit data bus, integrated I/O ports, a built-in Ethernet interface, and an 8514/A-compatible graphics adapter. Internal 3.5-in. hard-disk capacities range from 210 to 500 Mbytes. *Electronic Design, April 11, p. 158.*
TYAN COMPUTER CORP., *612 N. Mary Ave., Sunnyvale, CA 94086; (408) 720-1200.*
Circle 676

68040 VME SBC BOLSTERS PERFORMANCE USING ASICs

The MVME167 VMEbus single-board computer (SBC) is based on Motorola's MC68040 CISC microprocessor. The board, which requires just one slot in a 6U form-factor enclosure, achieves 20 MIPS with its 25-MHz 68040 processor, based on Dhrystone 1.1 measurements. It also has an optimized VME D64-compatible interface that can transfer data at 40 Mbytes/s. It has from 4 to 32 Mbytes of four-way interleaved DRAM, 8 kbytes of nonvolatile RAM for a time-of-day clock with a battery, and 128 kbytes of static RAM. The board consumes 15 to 18 W under typical conditions. *Electronic Design, June 13, p. 143.*
MOTOROLA COMPUTER GROUP, *2900 South Diablo Way, Tempe, AZ 85282; (800) 624-8999, ext. 230.* **Circle 677**

SOLID-STATE "HARD DISK" AIMS AT SPARC SYSTEMS

The TurboSwap accelerated hard-disk card fills the gap between a Sparc-compatible system's main memory and hard-disk drive. It operates nearly as fast as main memory (10-Mbyte/s transfer rate) and has a capacity near that of a typical hard-disk drive (40 or 80 Mbytes). The standard single-wide Sbus card has a maximum latency of less than 1 μs. The board couples application-specific DRAM with advanced data compression, error correction, and a custom software driver to offer data storage at 20% to 25% of the cost of main-memory expansion. The 40-Mbyte board consists of 36 DRAM chips and one 20,000-gate ASIC. *Electronic Design, July 11, p. 39.*
CERAM INC., *2260 Executive Circle, Colorado Springs, CO 80906; (719) 540-8500.*
Circle 678

486-BASED DESKTOP PC RUNS AT 50 MHZ

An Extended Industry Standard Architecture (EISA)-based desktop PC, the Compaq Deskpro 486/50L, uses the Intel 486 processor with an integrated 387-compatible numeric coprocessor running at a clock speed of 50 MHz. The processor has on-chip memory management and an integrated cache-memory controller with 8 kbytes of cache memory. A 256-kbyte second-level cache based on "write-back" technology enables the computer to have a 99% cache hit rate. Three models are available: Model 120 with a 120-Mbyte hard-disk drive; Model 340 with a 340-Mbyte hard-disk drive; and Model 510 with a 510-Mbyte hard-disk drive. All three have 8 Mbytes of 64-bit enhanced-page internal memory (expandable to 104 Mbytes) and advanced VGA graphics for 256-color support. *Electronic Design, July 25, p. 169.*
COMPAQ COMPUTER CORP., *20555 State Hwy. 249, P.O. Box 692000, Houston, TX 77269; (713) 370-0670.* **Circle 679**

DATA-ACQUISITION BOARDS ELIMINATE ALIASING

A pair of PC/AT data-acquisition boards, the DT3831 and the DT3831-G, each with antialiasing features, offer throughputs of 50 and 250 kHz, respectively. The DT3831's total harmonic distortion is 82 dB and signal-to-noise ratio is 71 dB, both at 10 kHz. The DT3831-G's total harmonic distortion is 78 dB, and signal-to-noise ratio is 70 dB, both at 40 kHz. The boards contain real-time error-prevention circuits that add on-the-fly calibration of all combinations of channel range and gains. As a result, rated accuracy is retained throughout the acquisition run to within ±0.5 LSB, even as gain setting changes. *Electronic Design, July 25, p. 175.*
DATA TRANSLATION INC., *100 Locke Dr., Marlboro, MA 01752; (508) 481-3700.*
Circle 680

MINI 486-BASED PC RUNS AT 40 MHZ

Innovative cooling technology keeps the GT486/40 PC's CPU chip cool enough to pump up its rated speed from 33 to 40 MHz. The designers created air-flow paths that carry out heat with two thermostatically controlled, variable-speed fans. The 486's published specifications say that it will run at 33 MHz up to 85°C. The cooling techniques enable the chip to run at 40 MHz and possibly higher speeds. The basic

COMPUTERS

system includes 4 Mbytes of main memory (expandable up to 32 Mbytes), a 2.88-Mbyte floppy-disk drive, a 100-Mbyte hard disk (expandable to 200 or 420 Mbytes), and a color display. *Electronic Design, July 25, p. 34.*
FALCO DATA PRODUCTS INC., *440 Potrero Ave., Sunnyvale, CA 94086; (408) 745-7123.*
Circle 681

VME GETS 10-TIMES SPEED BOOST

With the Autobahn, the VMEbus can now transfer data at 3.2 Gbits/s, a 10-fold increase. The device transfers serial data on two unused VMEbus pins. Autobahn I, slated for early 1992, will transfer data across the bus at 200 Mbytes/s. Autobahn II is scheduled for the end of next year, completing the push to 400 Mbytes/s. The data transfer occurs as a differential serial exchange on two existing, though rarely used, pins of the VMEbus—SERCLK and SERDAT. It can be used with any bus structure containing two spare pins, including Futurebus+. The required ECL serial communications chips were developed by Motorola Semiconductor. National Semiconductor also will supply the chips. *Electronic Design, October 24, p. 27.*
PEP MODULAR COMPUTERS, *600 North Bell Ave., Carnegie, PA 15106; (800) 379-8024.*
Circle 682

RISC PLATFORMS IRON OUT PRICE/PERFORMANCE KINKS

A family of RISC-based workstations—Models 720, 730, and 750—are designed to offer the best of three worlds, computational throughput, graphics, and networking, at cost-effective prices. The 720 is based on a 50-MHz microprocessor, while the other two incorporate 66-MHz processors. The low-end 720 delivers more than 57 MIPS, 17 MFLOPS, and 55 SPECmarks of performance. The 750 delivers 76 MIPS, 22 MFLOPS, and 72.2 SPECmarks, and has four EISA slots available for expansion. Model 730 fills the gap between the 720 and 750. *Electronic Design, March 28, p. 132.*
HEWLETT-PACKARD CO., *Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.* **Circle 683**

INK-JET PLOTTER SPEEDS THROUGH E-SIZE PLOTS

The DesignJet plotter is a large-format monochrome ink-jet plotter that can pump out a 300-dot/in. (dpi), E-size plot in under 6 min., or a 300-dpi, D-size plot in less than 3 min. At the heart of the plotter is a an Intel i860 embedded RISC processor. Suited for small work groups that use CAD software on PCs or workstations, the DesignJet plotter can be used in a time-saving, draft-quality 300-by-150-dpi mode. Users can fine-tune line differentiation and shading by selecting line widths from 0.2 to 12 mm. Roll media that's either 24 or 36 in. can be accommodated. *Electronic Design, November 7, p. 147.*
HEWLETT-PACKARD CO., *19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.* **Circle 684**

PEN-BASED PC STARTS NEW CLASS: PENTOPS

With an electronic stylus pen coupled to a "pentop" computer's keyboard, users can write directly on the computer's flat-panel display and still have the option of using the detachable keyboard to input data. The 5.9-lb. computer is built with custom ASICs to manage power- and I/O-control functions as well as video and memory control. One task of the system's I/O processor is to take raw data, calculate the pen position, then pass that data to the 20-MHz 80386SX CPU. The pentop system also has a send-and-receive fax-modem, 4 Mbytes of RAM (expandable to 8 Mbytes), and a 40-Mbyte hard-disk drive. *Electronic Design, November 21, p. 175.*
MOMENTA CORP., *295 North Bernardo Ave., Mountain View, CA 94043; (415) 969-9376.* **Circle 685**

IBM, SONY AIM OPTICAL DISKS AT DESKTOP

Two 3.5-in. erasable optical disk drives from IBM Corp. and Sony Corp. not only store 128 Mbytes in erasable magneto-optical form, but can read 120 Mbytes from prerecorded optical-ROM (O-ROM) disks similar in format to CD-ROM disks. Each SCSI drive uses highly integrated chips from Advanced Micro Devices (the Am95C96 optical-data disk controller and the Am95C94 advanced burst-error processor). IBM and Sony have developed a split optical-drive head that's smaller and lighter than the heads used in 5.25-in. drives. The drive head detects the bit polarities of magneto-optical disks, as well as the pits used to record data for O-ROM disks. Sony's data-transfer rate is 625 kbytes/s versus 384 kbytes/s for the IBM PS/2 drive. The SMO300 family from Sony has a 40-ms average seek time, compared with 66 ms for the IBM drive. *Electronic Design, July 11, p. 36.*
IBM CORP., *Old Orchard Rd., Armonk, NY 10504.*
Circle 686
SONY CORP. OF AMERICA, *655 River Oaks Pkwy., San Jose, CA 95134; (408) 432-0190.*
Circle 687

X-WINDOW CONTROLLER HANDLES 2K BY 2K

Designed for display subsystems with resolutions from 1280 by 1024 to 2048 by 2048 pixels, the Ω5700 X-Window-based controller fits in one VME slot. The board's main component is the video frame buffer (VFB) that comes with both on- and off-screen memory connected through a 256-Mbyte/s bit-block transfer (BitBLT) ASIC. Double-buffered operation is inherent in the design. Either the entire screen or individual windows can be updated at high speeds through the BitBLT ASIC without visible flickering. The Ω5700 consists of three 6U VME boards that can be assembled in different configurations to supply single- or multiple-display systems at different performance and cost levels. The other two boards are a video windowing controller (VWC), which adds one full-motion video window to the screen, and an i860-based graphics accelerator (GXA). *Electronic Design, October 10, p. 135.*
METHEUS CORP., *OGC Science Park, 1600 NW Compton Dr., Beaverton, OR 97006; (503) 690-1550.* **Circle 688**

GYRO POINTER CONTROLS 3D IMAGES IN FREE SPACE

With a revolutionary gyroscope design, a computer pointer operating in free space can manipulate 3D screen images. Unlike systems that calculate a pointer's position within a confined free-space volume using triangulation techniques and ultrasonic or magnetic sensors, the GyroPoint operates in a space limited only by the length of the cable connecting it to the host computer. And where positioning error in other 3D pointers increases as the pointer approaches the limits of the defined free-space volume, the GyroPoint's accuracy doesn't vary with distance. The device can be used like a mouse on a desktop or be held in mid-air. Weighing just 5 oz., the GyroPoint comes in a plastic housing 3.65-in. long, 1.68-in. wide, and 2.30-in. high. *Electronic Design, November 21, p. 160.*
GYRATION INC., *12930 Saratoga Ave., Bldg. C, Saratoga, CA 95070; (408) 255-3016.*
Circle 689

3D MOUSE FLIES WITHOUT LEAVING THE PAD

The Ice-Cube looks like a typical mouse, yet operates with six degrees of freedom—X, Y, and Z, plus pitch, yaw, and roll. The input device uses the company's patented optical technology to track the X, Y, and yaw positions. The Z, pitch, and roll movements come from a roller built into the top of the device. Moving the roller in a conventional manner handles the Z movements, while a simple left (pitch) or right (roll) tilt tracks either of the final two directions. The Ice-Cube can also operate as a standard X-Y mouse, where it would have four unused directional movements. Those

COMPUTERS

movements can control other functions in such applications as paint programs or games. *Electronic Design, Oct. 10, p. 34.*
Mouse Systems Corp., 47505 Seabridge Dr., Fremont, CA; (415) 656-1117.
Circle 690

0.5-IN. HIGH FLOPPY DRIVE IS TIGHT ON CLEARANCES

The smallest fully compatible 3-1/2-in. floppy-disk drive currently available, the FD05, has a height of just 1/2 in. A major hurdle in its design was the lack of extra space when inserting the disk. Thus, the path the media follows when entering the drive is very specific, with no room for mechanical play. Because the drive is built with dual heads to read the information on either side of the disk, the head-carriage assembly had to be made much thinner. In addition, the drive's sheet-metal cover is thinner than its base by 0.1 mm to provide extra clearance. *Electronic Design, October 24, p. 91.*
TEAC AMERICA INC., *Data Storage Products Div., 7733 Telegraph Rd., Montebello, CA 90640; (213) 726-0303.*
Circle 691

COMMUNICATIONS

CONTROLLER CHIP SUITS TELECOM AND DATACOM

Interfaces to wide-area networks, as well as serial interfaces for local asynchronous terminals, printers, modems, and other peripherals, can be implemented with the SAB 82532, a CMOS serial multiprotocol communications controller. The device offers two independent full-duplex serial channels and can control synchronous and asynchronous data transfers up to 10 and 2 Mbits/s, respectively. The controller has 64-byte transmit and receive first-in, first-out (FIFO) buffers. It also contains an 8/16-bit microprocessor interface for Motorola and Intel bus architectures, and consumes 50 mW at 2 Mbits/s. *Electronic Design, February 28, p. 95.*
SIEMENS AG, *Semiconductor Div., P.O. Box 801709, D-8000 Munich 83, Germany; (089) 4144-3728.* **Circle 692**
SIEMENS COMPONENTS INC., *2191 Laurelwood Rd., Santa Clara, CA 95054; (800) 456-9229.* **Circle 693**

REPEATER INTERFACE IC TAKES ON ETHERNET MEDIA

A **repeater** interface controller (RIC) designed for multimedia Ethernet LANs—the DP83950—manages these types of LANs with diversified equipment and lengthy cable runs, and detects and corrects error transmissions. The RIC, a multiport repeater, integrates 10Base-T transceivers, a transceiver interface, a Manchester encoder/decoder, a system interface, and digital logic on one mixed-signal chip. The device has 13 ports that connect to network segments. Functions replicated in all ports include a port-status register, port-partitioning logic, and a port-state machine. *Electronic Design, March 14, p. 101.*
NATIONAL SEMICONDUCTOR CORP., *2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; (408) 721-7020.* **Circle 694**

IC EXECUTES STILL-PICTURE COMPRESSION ALGORITHMS

The STI140 codec is a single-chip VLSI processor that fully implements the proposed JPEG (Joint Photographic Experts Group) image-compression standard for still-picture image compression/decompression. Designed to compress color still pictures, the codec also has the speed to compress or decompress video at up to 30 color pictures/s. Using quantization and multiple-compression techniques, it obtains 20:1 to 30:1 compression ratios. The device processes complex images at 27-MHz rates, in real time. *Electronic Design, May 23, p. 49.*
SGS-THOMSON MICROELECTRONICS (U.S.), *1310 Electronics Dr., Carrollton, TX, 75006; (214) 466-7404.* **Circle 695**
SGS-THOMSON MICROELECTRONICS (EUROPE), *17 Avenue des Martyrs, 38019 Grenoble, France; 33-7-658-5184.*
Circle 696

CONTROLLER CHIP LINKS PORTABLES TO ETHERNET

The latest Ethernet standard enables transceiver circuits to be integrated with the network-interface controller circuit. Consequently, National Semiconductor combined a network-interface controller, a serial network interface, and a newly developed transceiver for twisted-pair wiring on one chip, the DP83902. Compared to prior multichip solutions, the new Ethernet controller reduces board space by 20% and power consumption by 400%. Moreover, the device provides network-interface control, encoding/decoding, and 10Base-T functions without having to change existing software. *Electronic Design, July 11, p. 43.*
NATIONAL SEMICONDUCTOR CORP., *2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-7020.*
Circle 697

BICMOS ARRAY SPEEDS COMMUNICATIONS DESIGN

A **bipolar-CMOS** 50-MHz analog/digital array lets communications-system designers check out and optimize circuit functions before the chips are committed to production, or even in small production runs. The U3351BM device has both an analog bipolar high-frequency (HF) array and the digital bipolar-CMOS sea-of-gates (SOG) array on the same chip. The HF array has 638 npn and 80 pnp transistors, as well as about 2000 passive components. The SOG array contains 126,375 MOS components and 3625 npn transistors. *Electronic Design, August 8, p. 117.*
TELEFUNKEN ELECTRONIC GmbH, *P.O. Box 3535d, D-7100, Heilbronn, Germany; (0049) 7131-672519, fax: (0049) 7131-672340.* **Circle 698**

MULTIMEDIA CODEC CHIP ADDS VOICE AND MUSIC

Sound quality in multimedia systems usually receives little attention. Two single-chip stereo audio codecs, using delta-sigma data conversion and digital-signal processing, promise to remedy this. The CS4215 codec integrates delta-sigma analog-to-digital and digital-to-analog converters on one chip, as well as microphone and line-level inputs, input and output gain setting, antialiasing and output-smoothing filters, stereo headphone drive, and monitor-speaker drive. The chip has two channels of 16-bit analog-to-digital conversion along with two channels of digital-to-analog conversion. The 4215 can be used in workstations and personal computers because it operates at 5-V. *Electronic Design, September 12, p. 53.*
CRYSTAL SEMICONDUCTOR CORP., *P.O. Box 17847, Austin, TX 78760; (512) 445-7222.*
Circle 699

CHIP SET PUSHES FIBER LINKS TO 1.250 GBPS

Vitesse Semiconductor and AMD Inc. combined their talents to produce a chip set that implements the ANSI X3T9.3 Fiber Channel Standard for fiber-optic point-to-point communications. An upgraded version of AMD's 175-MHz TAXIchip set—the 1.25-GHz G-TAXIchip set—supports the Fiber Distributed Data Interface (FDDI) and the high-performance parallel interface (HIPPI) standards. Implemented in Vitesse's 0.8-μm gallium-arsenide technology, the G-TAXIchip set consists of the VSC7103 multiplexer and VSC7104 demultiplexer, both operating at up to 150 MHz; and the 1.25-GHz VSC7101 transmitter and VSC7102 receiver. AMD's set, dubbed GAAS TAXI, consists of the Am79G358 multiplexer, Am79G359 demultiplexer, Am79G368 transmitter, and Am79G369 receiver. *Electronic Design, September 26, p.149.*
VITESSE SEMICONDUCTOR CORP., *741 Calle Plano, Camarillo, CA 93012; (805) 388-7582.*
Circle 700
ADVANCED MICRO DEVICES INC., *P.O. Box 3453, Sunnyvale, CA 94088-3000; Chris Ciufo, (408) 749-4809.*
Circle 701

COMMUNICATIONS

OPTOCOUPLER ZIPS ALONG AT 50-MBAUD DATA RATE

The HCPL-7101 optocoupler switches signals at a maximum nonreturn-to-zero (NRZ) rate of 50 Mbaud with a typical pulse-width distortion of less than 1 ns, versus 10 to 12 ns for conventional designs. It includes a CMOS driver chip, an AlGaAs LED, and a CMOS detector IC. A CMOS or TTL input signal controls the driver IC that supplies LED current. The detector chip includes a photodiode, a transimpedance amplifier, and a voltage comparator with hysteresis. The 3-state output is CMOS- and TTL-compatible, and is controlled by an output-enable pin. The only external devices required are two ceramic bypass capacitors (0.01 to 0.1 μF). *Electronic Design, September 12, p. 169.*
HEWLETT-PACKARD CO., *Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; 1-800-752-0900.* **Circle 702**

DATA/FAX/VOICE MODEM CHIP SET CUTS LOGIC

The two-chip CL-MD1424AT Communicator modem IC family was designed for multimode communications in laptop and notebook computers. The family provides data-, facsimile-, and voice-transmission capabilities without the need for an external microprocessor, universal asynchronous receiver/transmitter (UART), and other components. With the Communicator, a complete data/fax/voice modem can be created in an area smaller than a business card. The two-chip set offers full-duplex data communication at rates up to 2400 bits/s and facsimile transmission or reception at rates up to 14,000 bits/s. A voice mode allows a PC to emulate a telephone answering machine. A third chip, the CL-MD1424EC, can be added for error-correction and data-compression capabilities. *Electronic Design, Nov. 21, p. 173.*
CIRRUS LOGIC INC., *3100 West Warren Ave., Fremont, CA 94538; (510) 623-8300.*
Circle 703

COMPONENTS

SURFACE-MOUNTED LED LIGHTS UP PC BOARDS

A surface-mounted LED right-angle circuit-board indicator resolves the problems of getting light out of the package by incorporating an optically pure lens that serves as a light pipe. The lens is transfer-molded from a clear epoxy that's specially formulated to withstand the 260°C temperature of infrared soldering without deforming or discoloring. Initially, the device will be offered in AlGaAs red and high-efficiency yellow and green colors, and in 1-, 3-, and 5-mm sizes. The three sizes correspond to the T-3/4 (subminiature), T-1, and T-1-3/4 packages, respectively. *Electronic Design, April 11, p. 137.*
DIALIGHT CORP., *1913 Atlantic Ave., Manasquan, NJ 08736; (908) 223-9400, fax: (908) 223-8788.* **Circle 704**

ECL CLOCK OSCILLATOR IS FIRST WITH ENABLE/DISABLE

The M1900 ECL crystal oscillator offers a tristate enable/disable function that lets the clock be shut off by logic control. The M1900 oscillator's enable/disable function is activated by logic levels on an input pin. An input logic "1" turns off the oscillator and causes the device's output pin to be ECL logic "0". An external ECL signal may then be applied by a tester to the oscillator output node. Because of the wired-OR capability of ECL logic, this achieves the same effect as the HCMOS tristate. The oscillator, available in a four-pin, dual-in-line metal case, comes in frequencies from 10 MHz to 225 MHz. *Electronic Design, May 9, p. 165.*
MF ELECTRONICS CORP., *10 Commerce Dr., New Rochelle, NY 10801; (914) 576-6570.*
Circle 705

SURFACE-MOUNT CIRCUIT PROTECTOR RESETS ITSELF

The remotely resettable, surface-mounted PolySwitch protects electronic systems from overcurrent or short-circuit conditions. It's a more rugged alternative to fuses and is compatible with automated production processes. Unlike fuses, the PolySwitch circuit protectors reset automatically once the fault current is removed. Made of solid-state conductive material, the devices have low series resistance. Five devices are available with current ratings from 0.3 to 1.5 A and voltage ratings from 30 to 60 V dc. All meet UL standards and are taped and reeled to EIA-481 requirements. *Electronic Design, July 11, p. 159.*
RAYCHEM CORP., *300 Constitution Dr., Menlo Park, CA 94025; (800) 2RAYCHEM.*
Circle 706

SOLID-STATE RELAY FAMILY OFFERS 3750-V ISOLATION

By meeting or exceeding domestic and international standards for input-to-output isolation, the 21-product LH1500 family of solid-state relays is a complete lineup of relays rated at 1 A or less. With isolation ratings of up to 3750 V rms, the relays pass FCC 68.302 and other regulatory voltage-surge requirements. Within the relays, a GaAlAs diode is used for actuation control and an integrated monolithic chip supplies switch output. The BCDMOS chip contains a photodiode array, various switch-control circuits, and DMOS switches. *Electronic Design, September 12, p. 181.*
AT&T MICROELECTRONICS, *Dept. 52AL040420, 555 Union Blvd. Allentown, PA 18103; (800) 372-2447.* **Circle 707**

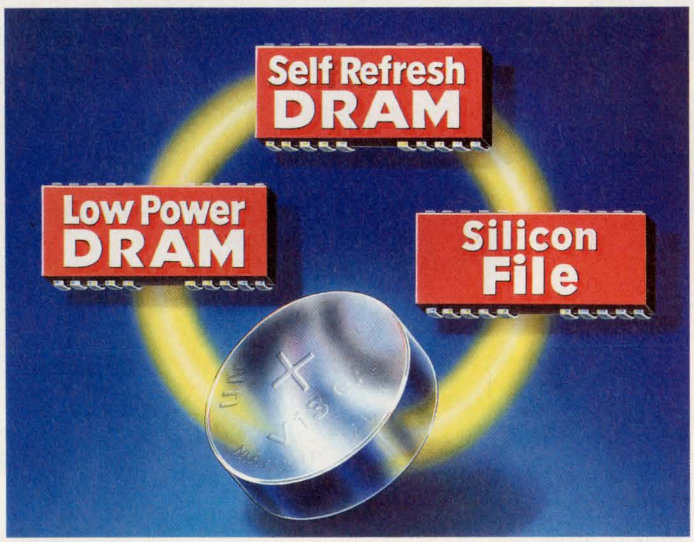
FIBER-OPTIC CONNECTOR CRIMPS ON CABLE

The LightCrimp connector simply crimps onto fiber-optic cable in less than two minutes, with no epoxy, oven, or UV curing. Consequently, extra equipment and overall messiness involved with epoxy-based connections is avoided, and time is saved. All that's required is a two-step crimp, a cleave, and a 30-second polish. The connector uses double-clamping: a front fiber clamp prevents pistoning (in-and-out movement of the fiber due to thermal cycling), and a rear buffer clamp, which increases the termination's tensile strength. Insertion loss is less than 1 dB, using 62.5-μm multimode cable. Durability is 500 cycles. *Electronic Design, June 27, p. 151.*
AMP INC., *P.O. Box 3608, Harrisburg, PA 17105-3608; (800) 522-6752.* **Circle 708**

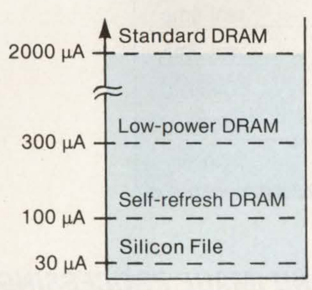
C&C Computers and Communications

Low-power DRAMs

The Low-down on Memory Power



Memory devices are as varied as the applications they are designed for, but in this age of miniaturization and mobility they have one thing in common: power consumption must be rockbottom. Capacity, speed, price or package choice may be your highest priority, but you'll be glad to know that DRAM memories from NEC operate on an absolute minimum power supply.



Based on a 0.7 μm, stacked capacitor process, NEC's 4 Megabit DRAMs offer high access speeds and convenient configurations for a wide range of desktop and portable applications. Competitively priced standard DRAMs have the high capacity required by stationary systems, while low-power DRAMs with a 300 μA data retention current are ideal for laptops and other equipment frequently on the move. NEC's Silicon File, only needs a 30 μA refresh current, and is designed to do duty as a solid-state disk in mainframes, workstations and PCs. Data retention by way of a 3 V battery gives this memory static RAM quality. Another device with extremely low power consumption is the self-refresh DRAM with a byte and word structure and optional parity. Intended for new low-power designs, such as notebook and palm PCs, it requires a mere 100 μA standby current. Compatible as to function, speed and pin assignment, all these DRAMs can also be configured as SIMM modules or memory cards.

CIRCLE 140 FOR U.S. RESPONSE

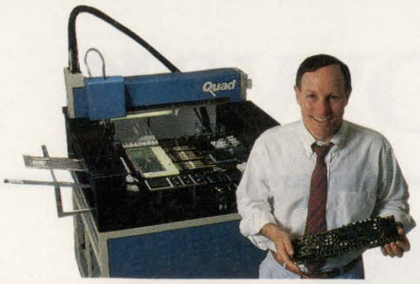
CIRCLE 141 FOR RESPONSE OUTSIDE THE U.S.

For fast answers, call us at:

USA Tel: 1-800-632-3531. Fax: 1-800-729-9288. Germany Tel: 0211-650302. Fax: 0211-6503490. The Netherlands Tel: 040-445-845. Fax: 040-444-580. Sweden Tel: 08-753-6020. Fax: 08-755-3506. France Tel: 1-3067-5800. Fax: 1-3946-3663. Spain Tel: 1-504-2787. Fax: 1-504-2860. Italy Tel: 02-6709108. Fax: 02-66981329. UK Tel: 0908-691133. Fax: 0908-670290. Ireland Tel: 01-6794200. Fax: 01-6794081. Hong Kong Tel: 755-9008. Fax: 796-2404. Taiwan Tel: 02-719-2377. Fax: 02-719-5951. Korea Tel: 02-551-0450. Fax: 02-551-0451. Singapore Tel: 253-8311. Fax: 250-3583. Australia Tel: 03-8878012. Fax: 03-8878014. Japan Tel: 03-3454-1111. Fax: 03-3798-6059.

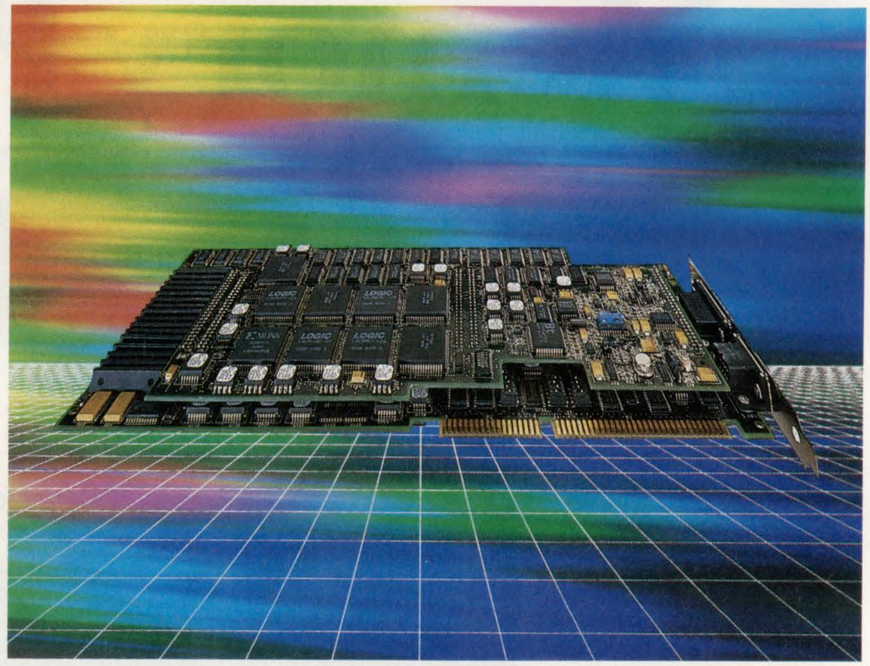
NEC

FASTEST IMAGE PROCESSING ON A SINGLE PC/AT BOARD



"Our DT2867 Integrated Image Processor combines real-time processing and precision image acquisition on a single PC/AT board."

—Fred Molinari, President



Real-Time Processing
- 75 MHz, 16-bit processor
- Simultaneous acquisition and processing

Precision Image Acquisition
- Programmable gain, offset, and reference
- Square pixels

Optional 32-Bit, 25 MFLOP DSP Board
- 10 MHz **DT-*Connect***™ interface to DT2878 Advanced Processor

Extensive Development Software Included
- Subroutines callable from Microsoft C
- Device driver and utilities

Quantity pricing available

FAST 5 day delivery

Call for FREE Catalog

(508) 481-3700

In Canada, call (800) 268-0427

DT2867 Processing Times
Full 640 x 480 image

True Frame Averaging (to 256 frames)	real-time
Histogram	real-time
Math and Logic	real-time
3 x 3 Binary Morphology	.043 sec
3 x 3 Convolution	.043 sec
7 x 7 Convolution	.30 sec

THE LEADER IN DATA ACQUISITION AND IMAGE PROCESSING

DATA TRANSLATION®

World Headquarters: Data Translation, Inc., 100 Locke Drive, Marlboro, MA 01752-1192 USA, (508) 481-3700, Fax (508) 481-8620, Tlx 951646
United Kingdom Headquarters: Data Translation Ltd., The Mulberry Business Park, Wokingham, Berkshire RG11 2QJ, U.K., (734) 793838, Fax (734) 776670, Tlx 94011914
Germany Headquarters: Data Translation GmbH, Im Weilerlen 10, 7120 Bietigheim-Bissingen, Germany 7142-54025, Fax 7142-64042
International Sales Offices: Australia (2) 699-8300; Austria 22-236-7660; Belgium (2) 466-8199; Brazil (11) 240-0598; Canada (416) 625-1907; China (1) 513-7766 x 1222; Denmark 42 274511; Finland (0) 3511800; France (1) 69077802; Greece (1) 361-4300; Hong Kong (5) 448963; India (22) 23-1040; Israel 52-545685; Italy (2) 82470.1; Japan (3) 502-5550, (3) 5379-1971; Korea (2) 718-9521; Malaysia 3-2486788; Netherlands (70) 399-6360; New Zealand (9) 415-8362; Norway (2) 53 12 50; Poland (22) 580701; Portugal (1) 7934834; Singapore 338-1300; South Africa (12) 803-7680/93; Spain (1) 555-8112; Sweden (8) 761 78 20; Switzerland (1) 386-8686; Taiwan (2) 3039836

CIRCLE 104 FOR U.S. RESPONSE   CIRCLE 105 FOR RESPONSE OUTSIDE THE U.S.

Engineers Can Use VHDL To Verify Both The Specification And Implementation Of A Design.

Check Your Designs With VHDL Test Benches

DAVID R. COELHO
Vantage Analysis Systems Inc.,
42808 Christy St., Suite 200,
Fremont, CA 94538;
(510) 659-0901.

Many reasons abound why the VHSIC Hardware Description Language (VHDL) is considered such a powerful language. For instance, it can be used not only to describe a circuit—but to specify stimulus for it, and then to test that circuit's response.

This approach, commonly called a VHDL test bench, can automatically verify the correctness of a design. By combining the test bench with a top-down design methodology, designers can boost productivity and gain increased confidence in their circuits.

The simple example of an RS flip-flop, which is described throughout this article, illustrates how a VHDL test bench is written. Then the methodology used in the flip-flop example can easily be generalized for more complex problems. The RS flip-flop will be simulated both as a behavioral model (the specification) and as a structural model (the implementation). The following code shows the entity declaration for this circuit:

```
ENTITY rsff IS
    PORT    (r,s: IN BIT; q: OUT BIT);
END rsff;
```

The device has two inputs, r and s, and a single output, q. All ports have a data type with two possible values, 0 and 1 (a BIT data type). In an actual design, we would use a more sophisticated value system, such as one that includes an unknown value as a minimum. But it will do for our purposes. The high-level or behavioral VHDL representation of this device is:

```
ARCHITECTURE behavioral OF rsff IS
BEGIN
  PROCESS (r,s)
   BEGIN
     IF (r = '1') AND (s = '0') THEN
       q <= '1' AFTER 7 ns;
     ELSIF (r = '0') AND (s = '1') THEN
       q <= '0' AFTER 5 ns;
     END IF;
  END PROCESS;
END behavioral;
```

In this model, we see that the device is sensitive to changes on either of the inputs, r or s. Because this device uses active-low logic, we'll set the output to 1 when the reset is inactive (high) and the set is active (low).

When the reset is active (low) and the set is inactive (high), we'll clear the output, or set it to 0. In a more

CHECKING CIRCUITS WITH VHDL TEST BENCHES

realistic model, we would likely set the output to unknown if both the inputs were low. For both inputs high, the output is unchanged. Although timing is fixed in this model, a typical approach would be to use generic parameters to provide different timing to each instance of this device.

We must now create test data to ensure that this model operates correctly. The following summarizes the written specification for this device:

- The output is latched to high within 9 ns of a high-to-low transition on the s input.
- The output is latched to low within 9 ns of a high-to-low transition input on the r input.
- The output remains unchanged on low-to-high transitions.
- The output is undefined if both inputs transition from high-to-low within 2 ns.

In this specification, as is the case with typical databook descriptions, circuit operations occur with ranges of times, and device operation is often less than ideal (as in the case of the undefined output here).

To build a test bench laboratory within which to perform the tests must first be built. Here, we'll create a high-level circuit with no inputs or outputs, as shown in this entity declaration:

```
ENTITY rsff_bench IS
END rsff_bench;
```

Next, we declare an architecture with signals that correspond to each of the inputs and outputs of the circuit under study, along with a single component declaration for the circuit itself:

```
ARCHITECTURE test OF rsff_bench IS

  -- circuit under study
  -- single instantiation
  COMPONENT rsff
    PORT (r,s: IN BIT; q: OUT BIT);
  END COMPONENT;

  -- one signal per input/output
  SIGNAL r,s,q: BIT;
```

We then declare an internal signal strobe that will be used for synchronous application of stimulus and strobing of the output, and a constant clk_period that determines the clock period for applying stimulus to the device:

```
-- master clock
SIGNAL strobe: BIT;

-- clock period
CONSTANT clk_period: time:= 20 ns;
```

Now we're ready to describe the architecture for our test bench. First, we need to create a single instantiation for the circuit under study and connect it to the internal signals r,s, and q:

```
-- circuit under test
circuit:rsff PORT MAP(r,s,q);
```

We must also establish a concurrent process that toggles the strobe signal with the proper clock period as specified by the constant clk_period:

```
-- strobe the outputs
strobe <= NOT strobe
  AFTER clk_period / 2;
```

Both application of stimulus to the circuit and the method for testing circuit response must be described. In this flip-flop example, we create a single process check_output that performs both functions. First, let's review the approach to apply stimulus to the circuit:

```
-- check the outputs
check_output : PROCESS (strobe)
  VARIABLE first : boolean := true;
  BEGIN
  IF first THEN
    first := false;

    r <= '1' AFTER (0*clk_period) + 1 ns,
         '1' AFTER (1*clk_period) + 1 ns,
         '0' AFTER (2*clk_period) + 1 ns,
         '1' AFTER (3*clk_period) + 1 ns;

    s <= '0' AFTER (0*clk_period) + 1 ns,
         '1' AFTER (1*clk_period) + 1 ns,
         '1' AFTER (2*clk_period) + 1 ns,
         '1' AFTER (3*clk_period) + 1 ns;
  END IF;
  .
  .
END PROCESS;
```

The process is sensitive to the strobe signal that toggles its value after a delay of clk_period. This process will be activated each half clock period as a result (two-phase clock), or in our example every 10 ns (20 ns/2). The first variable limits the execution of the stimulus portion of this process to occur once during the simulator's startup phase. A fixed set of values are applied to the circuit:

time	r	s
1 ns	1	0
21 ns	1	1
41 ns	0	1
61 ns	1	1

The stimulus is applied 1 ns after the end of a given clock period so that the circuit's output value can settle before applying a new set of inputs. Although the stimulus applied here is quite simple, this same strategy can be utilized for much more com-

CHECKING CIRCUITS WITH VHDL TEST BENCHES

plex circuits as well. The following changes can be considered in more complex situations:

• Read the stimulus values from a data file at simulator run time rather than hardcoding the values as shown above. This data-file approach is superior because the VHDL test bench will be considerably smaller, reducing compile time and simulator memory requirements. More importantly, the stimulus can be changed without forcing a recompilation of the VHDL test bench.

• Place the stimulus code in a separate process because it can increase the readability of the test bench in certain situations. A problem can occur, however, if more than one process accesses a given port. In this case, creating a separate process in VHDL to apply stimulus to the same signal that the response process will later read forces the modeler to create a bus-resolution function. This is because VHDL creates a separate signal driver for every process that accesses an output or input signal. Thus, when more than one process creates drivers to a signal, a bus-resolution function must be applied. Bus-resolution functions are difficult to write and should generally be avoided if possible, especially when writing test benches.

• Apply stimulus that tests bad and good inputs. Test the circuit to make sure that it handles improper inputs in a predictable fashion. In our example, a low input on both the r and s ports might be applied to test the circuit's behavior in the undefined mode.

• Circuit timing is just as important as function. Therefore, tests checking that the circuit operates within the timing constraints required should be created.

• In many cases, an algorithmic approach to generating test data can be used. This approach will be more efficient, and creating large test sets will likely take less effort. A good example of when an algorithmic approach should be used is when generating a thorough set of test vectors for an ALU unit. Here, all possible input values are fed to the ALU for each possible ALU instruction and each output is tested. Because VHDL has arithmetic features built into it, the test bench could "calculate" the expected arithmetic answer to ensure that the ALU worked properly for each test. This type of test bench can generate a large number of test cases (sometimes with 100% coverage of all possible inputs) with a relatively small amount of code.

Now that the stimulus has been described for the circuit, we're ready to test the response of the circuit. The following is the remainder of the check_output process:

```
-- check the outputs
check_output : PROCESS (strobe)
  VARIABLE first : boolean := true;
  BEGIN
  .
  .
  IF strobe = '1' THEN
    ASSERT (NOW /= 0 ns)
      REPORT "RSFF Functional Test" SEVERITY note;

    ASSERT (NOW /= (0 * clk_period) + (clk_period / 2)) OR (q = '1')
      REPORT "q /= 1" SEVERITY error;

    ASSERT (NOW /= (1 * clk_period) + (clk_period / 2)) OR (q = '1')
      REPORT "q /= 1" SEVERITY error;

    ASSERT (NOW /= (2 * clk_period) + (clk_period / 2)) OR (q = '0')
      REPORT "q /= 0" SEVERITY error;

    ASSERT (NOW /= (3 * clk_period) + (clk_period / 2)) OR (q = '0')
      REPORT "q /= 0" SEVERITY error;
  END IF;
  END PROCESS;
```

output of the circuit only at preselected time points.

An alternative approach is to make this process sensitive to the circuit's output (in this case the q signal), and then check the outputs as they're generated. This second approach is more complicated in that many circuits will require a settling time before they produce the final correct outputs.

In our example, the rising edge of the strobe signal is tested. By reviewing the stimulus, we see that the stimulus is applied during the first phase of the clock, and the output is tested during the second phase of the clock.

Once again, we see that the check process is sensitive to the strobe signal, and will check the outputs at each clock period.

This scheme is termed a synchronous test bench, because it tests the

An assertion is used to print the message "RSFF Functional Test" at the start of the simulation. We then test the output after each input test case is applied. The expected results are:

CHECKING CIRCUITS WITH VHDL TEST BENCHES

time	expected
10 ns	1
30 ns	1
50 ns	0
70 ns	0

We selected the test times to occur exactly 9 ns after the application of the stimulus to the circuit. In this way, we perform a check that corresponds to the written specification for the circuit. If any of these tests fail, then an assertion error is generated to report a message like "q/= 0". In most implementations, the simulator would also include additional information, such as the simulation time when the error occurred and in which component or at which line number in the source code, making it easy to diagnose the problem and the test case that failed.

This test bench, much like the stimulus section, hardcodes the actual tests. A better approach would be to read the expected results from a data file.

As mentioned in an earlier discussion on applying stimulus, it's possible to use algorithmic test-generation techniques not only to generate stimulus, but also to generate expected results. This approach can be very powerful and can result in very readable test benches that perform thorough (if not comprehensive) tests of the circuit.

In advanced circuits, the expected results will often be a function of the state of the device. This is particularly true of microprocessor class devices. In these cases, a test bench might be written more easily with a feedback loop that uses the circuit's current outputs to calculate additional tests to apply and to calculate the expected results. For example, an identical set of register values might be fed to a memory-addressing chip with differing addressing modes. Although the same data is fed to the circuit, the outputs will be different because the addressing mode is altered. The results that check code in the test bench could use the addressing mode that was used in the calculations to test the expected results. This type of test bench is typically much more effective because the amount of raw test data required is reduced.

In VHDL, we must also specify which version of a circuit should be used. In addition, we must declare a configuration for the simulation in VHDL terms. In order to test the high-level specification, we created this configuration:

```
CONFIGURATION highlevel OF rsff_bench IS
FOR test
    FOR circuit:rsff
      USE ENTITY work.rsff(behavioral);
    END FOR;
END FOR;
END highlevel;
```

This configuration was labeled highlevel and linked to the rsff_bench entity. The outermost FOR statement chooses the test architecture. In our case, we have only one architecture defined for the rsff_bench entity. Generally, though, we could have several versions of our test bench so VHDL allows us to choose one. Next we select which version of our circuit under study to use. In this case, behavioral version of the rsff entity is chosen for the component circuit.

In some implementations, this configuration information can be created automatically. But as we'll see later, the ability to control which architecture to use for a given entity is a very powerful feature when using test benches.

With this configuration specified, we're ready to feed all of this input to our VHDL simulator. The result from simulating this circuit with the Vantage VHDL simulator is:

```
   Simulation_Control v3.101,
     Vantage Analysis Systems, Inc.

Initializing Simulation_Control...
Preparing rsff_bench for simulation...

**Assertion Note: RSFF Functional Test  (scn/sim)
**Occurred in instance 'rsff_bench' at time 0 fs
  after 0 delta timepoints had been simulated.

The maximum simulation time specified
has been reached.  (simcon/SIM/2)

Halting at time 200 ns, after 26 delta
timepoints have been simulated.  (simcon/SIM/19)
```

If there had been any errors, we would have seen error-severity assertions displayed. When that happens with this implementation, the user can choose whether the simulator should halt execution or continue.

From this output we can quickly determine whether the circuit is operating correctly without manually reviewing the waveform display or a tabular dump of the signal values. The test bench gives us a correct or not-correct check of the circuit operation. In fact, the test bench can be viewed much like a regression test for a hardware system. If the test cases are thorough enough, then we can have confidence that the high-level specification correctly models the circuit according to our written specification.

Now that we have a working specification for our circuit, we need to move on to our implementation. We'll construct this circuit from two primitive devices—a NAND gate and a buffer. The VHDL entity declaration and architecture for the NAND gate is:

```
ENTITY nand_gate IS
    PORT    (a,b: IN BIT; y: OUT BIT);
END nand_gate;

ARCHITECTURE behavioral OF nand_gate IS
```

CHECKING CIRCUITS WITH VHDL TEST BENCHES

```
BEGIN
    y <= a NAND b AFTER 1 ns;
END behavioral;
```

Once again, we're using very simple assumptions in this example. A more realistic model would reflect actual timing rather than unit delay, and would model at a minimum propagation of unknown values. In this case, the NAND gate has two inputs, a and b, and one output, y. The model watches for any changes in either input, and assigns the value "a NAND b" to the output with a delay of 1 ns when either input changes value. The model for the buffer is similar:

```
ENTITY buf_gate IS
    PORT   (a: IN BIT; y: OUT BIT);
END buf_gate;

ARCHITECTURE behavioral OF buf_gate IS
BEGIN
    y <= a AFTER 1 ns;
END behavioral;
```

Here we have one input, a, and one output, y. The input is echoed to the output with a delay of 1 ns whenever the input changes value.

Our next task is to describe an implementation of the RS flip-flop. In this case, we will specify an alternate architecture for the rsff entity using structural VHDL.

As stated earlier, the entity declaration for the rsff circuit has two inputs, r and s, and an output, q. Shown here is the structural architecture for this circuit:

```
ARCHITECTURE structural OF rsff IS
  COMPONENT nand_gate
    PORT (a,b:IN BIT; y: OUT BIT);
  END COMPONENT;

  COMPONENT buf_gate
    PORT (a:IN BIT; y: OUT BIT);
  END COMPONENT;

  SIGNAL qn,qb: BIT;
BEGIN
  b1:buf_gate PORT MAP(qb,q);
  g1:nand_gate PORT MAP(s,qn,qb);
  g2:nand_gate PORT MAP(qb,r,qn);
END structural;
```

We first declare the two components that we will be using, nand_gate and buf_gate. We also declare the interconnecting signals, qn and qb. Finally, we instantiate one buffer, b1 (with an entity type of buf_gate), and two gates, g1 and g2 (with an entity type of nand_gate). They're connected as follows:

- Buffer b1 port a to signal qb, port y to signal q
- Gate g1 port a to signal s, port b to signal qn, and port y to signal qb
- Gate g2 port a to signal qb, port b to signal r, and port y to signal qn

It's clear that this represents a typical RS-latch function.

We must specify which version of a circuit will be used, much like we did for the high-level testing. The configuration for testing our structural version of the RS flip-flop is:

```
CONFIGURATION gates OF rsff_bench IS
FOR test
  FOR circuit:rsff
    USE ENTITY work.rsff(structural);
    FOR structural
      FOR g1,g2:nand_gate
      USE ENTITY work.nand_gate(behavioral);
      END FOR;

      FOR b1:buf_gate
      USE ENTITY work.buf_gate(behavioral);
      END FOR;
    END FOR;
  END FOR;
END FOR;
END gates;
```

This configuration was labeled gates and linked to the rsff_bench entity. The outermost FOR statement chooses the test architecture of the test bench. The next FOR statement chooses the structural version of the rsff entity that's named circuit in our test bench. More work is required for the structural configuration because we must choose which version of each component to use. For gates g1 and g2, we choose the behavioral version of the nand_gate entity. For the b1 component, we select the behavioral version of the buf_gate entity.

Now, we're ready to simulate the structural version of our circuit. No changes were made to the test bench itself. All we did was tell the simulator to use the structural implementation. We could easily use the same test bench to test many versions of our circuit, all without changing or recompiling the test bench. This feature saves us substantial compiler time.

That's because configurations tend to be relatively short and the test bench itself tends to be rather complicated.

We're now ready to review the simulation results from this test run:

Once again, any errors would have been flagged with assertion messages.

The output is almost identical to the high-level simulation except for two additional delta time points, which result from the finer grain of detail in the structural simulation.

David Coelho, a founder, chairman, and executive vice president for Vantage Analysis Systems, holds a BSEE from Stanford University, Calif.

HOW VALUABLE?	**CIRCLE**
HIGHLY	530
MODERATELY	531
SLIGHTLY	532

National Semiconductor

12-BIT DATA ACQUISITION SYSTEM

Now you can have easy access to the analog world.

Unsurpassed integration makes analog design easy.

When crossing the border from analog to digital the last thing you want is excess baggage.

That's why we designed the industry's first +5V 12-bit plus sign Data Acquisition System, the LM12458. A one-chip solution that not only shrinks board space but also reduces design and debug time.

Versatility through software programmability.

Easily configured via software, the LM12458 lets you switch the mux from differential to single-ended mode "on the fly."

What's more, with conversion times of 8.8µs (12-bit plus sign), 4.2µs (8-bit plus sign), and 2.2µs ("watchdog" comparison mode) you get optimized system performance at a throughput rate of 87kS/s min.

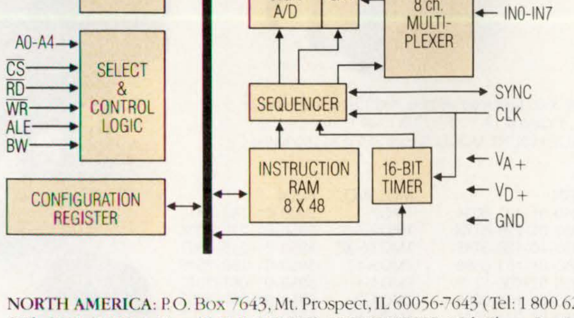
Single +5V Operation.

With single +5V operation, you get all this performance while consuming just 30mW max (50µW in standby mode).

Plus, its self-calibrating architecture ensures high accuracy over time and temperature.

So hurry up and get on board. And gain duty-free passage to the analog world.

System-level integration on a single chip.



FEATURES

- Software-programmable
  - Conversion speeds
  - Resolution
  - Mux
- Configurable for stand-alone operation
- 87kS/s min. throughput rate
- 30mW power consumption @5V
- 50µW standby mode
- 0-5V input
- ±0.5LSB DNL
- 8- or 16-bit wide I/O
- 44-pin PLCC package

Access us with one easy call.

For a free software design kit, call: 1-800-NAT-SEMI, Ext. 143. Or, fax: 1-800-888-5113

National Semiconductor

NORTH AMERICA: P.O. Box 7643, Mt. Prospect, IL 60056-7643 (Tel: 1 800 628 7364, ext. 143; Fax: 1 800 888 5113); **EUROPE:** Industriestraße 10, D-8080 Fürstenfeldbruck, Germany (Tel: 49 8141 103 0; Fax: 49 8141 103 515); **HONG KONG:** 15th Floor, Straight Block, Ocean Center, 5 Canton Rd., Tsimshatsui, Hong Kong (Tel: 852 737 1600; Fax: 852 736 9921); **JAPAN:** 4-15, Nishi-shinjuku, Shinjuku-ku, Tokyo, Japan 160 (Tel: 81 3 3299 7030; Fax: 81 3 3374 4303).

RF TRANSFORMERS

Over 50 off-the-shelf models...
3KHz-800MHz from $3.25

Having difficulty locating RF or pulse transformers with low droop, fast risetime or a particular impedance ratio over a specific frequency range?... Mini-Circuits offers a solution.

Choose impedance ratios from 1:1 to 36:1, connector or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55831 requirements*). Ultra-wideband response achieves low droop and fast risetime for pulse applications. Ratings up to 1000M ohms insulation resistance and up to 1000V dielectric voltage. For wide dynamic range applications involving up to 100 mA DC primary current, use the T-H series. Coaxial connector models are offered with 50 and 75 ohm impedance; BNC standard; request other types. Available for immediate delivery with one-year guarantee.

*units are not QPL listed

case styles
T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

CIRCLE 132 FOR U.S. RESPONSE

CIRCLE 133 FOR RESPONSE OUTSIDE THE U.S.

NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

finding new ways ...
setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

C71 REV. B

CIRCLE 521

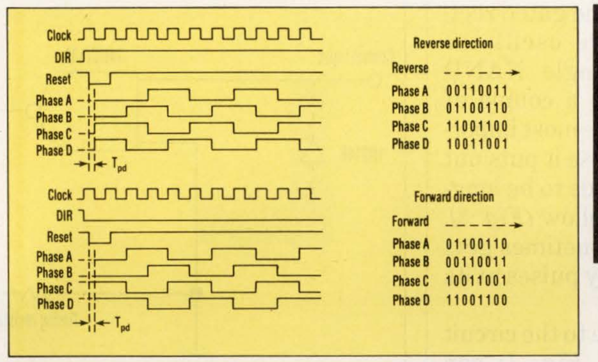
Simplest Driver Yet For Stepper Motors

CHARLES HO
Jet Propulsion Lab, Section 357, 4800 Oak Grove Dr., M/S 18-104,
Pasadena, CA 91109; (818) 354-7666.

Stepper motors of the permanent magnet type consist of two parts: an assembly of permanent magnets distributed around the circumference of a rotor shaft, and a surrounding ring of electromagnets attached to the stationary housing of the motor. Energizing the electromagnets with the proper polarities, in the proper sequence, generates a rotating magnetic field pattern. The permanent magnets try to align themselves with the rotating field pattern, producing torque.

A great many different circuits have been developed for energizing electromagnets (ELECTRONIC DESIGN, *May 10, 1990, p. 103., and May 23, 1991, p. 120)*. The main advantage of this circuit is its extreme simplicity. It consists of just two flip-flops, two gates, four Darlingtons, five resistors, and a capacitor.

Different magnetic polarity sequences are needed to drive the stepper motor in the forward and reverse directions *(Fig. 1)*. As shown, each driving phase has a 50% duty cycle. For forward motion, phase A leads phase B by 90°; whereas the opposite is true for reverse motion. Note that phase C is always simply the complement of phase A, and D is the complement of B.



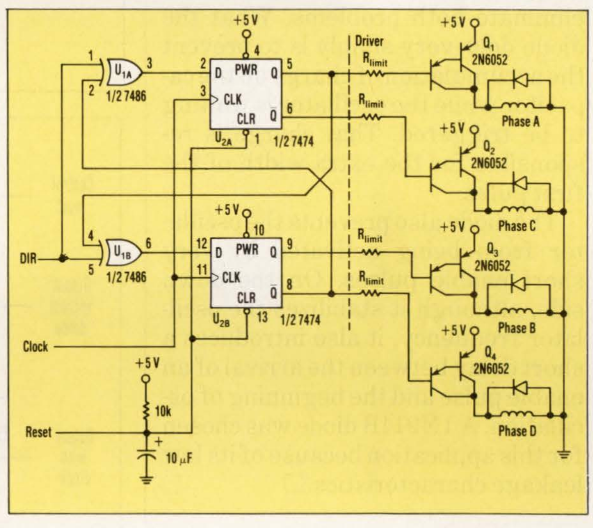
1. THE magnetic polarity sequences required to drive a permanent magnet stepper motor are shown here in both truth table and timing diagram form. The phases all have a 90° duty cycle.

The equations for forward motion, which give the next set of phases in terms of the current ones, can be written from inspection of the truth tables of Figure 1 as:

$\text{Phase A}(t+1) = \overline{\text{Phase B}}$
and
$\text{Phase B}(t+1) = \text{Phase A}.$

Similarly, the equations for reverse motion are:

$\text{Phase A}(t+1) = \text{Phase B}$
and
$\text{Phase B}(t+1) = \overline{\text{Phase A}}.$



2. SIMPLICITY is epitomized in the logic portion of this driver circuit, which consists of just two ICs—a dual flip-flop and a dual XOR gate. The resistors in series with the Darlington inputs should be chosen to limit the current sinking of the 7474 outputs.

By adding a direction variable, DIR, general equations valid for both directions of motion can be written as follows:

$\text{Phase A}(t+1) = \text{Phase D}(t) :+: \text{DIR}$
and
$\text{Phase B}(t+1) = \text{Phase A}(t) :+: \text{DIR},$

where :+: denotes the exclusive-OR (XOR) operation; Phase D, we recall, is the complement of Phase B; and the variable DIR is a logic ZERO for the forward direction and a ONE for reverse.

By setting up the drive equations in this way, they can be readily implemented by a D-type flip-flop, which is described by the equation:

$Q(t+1) = D$ *(Fig. 2)*.

Each output of the type 7474 flip-flops in that diagram can sink up to 16 milliamperes—more than enough current to drive a pnp Darlington power transistor, such as the 2N6052 type used in the present implementation.□

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

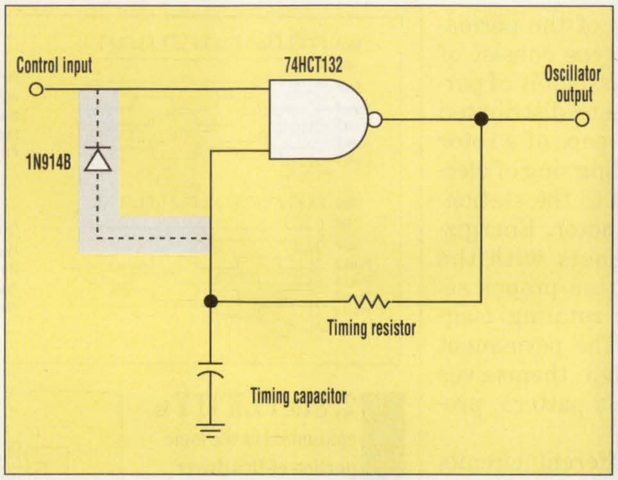
CIRCLE 522 DIODE STABILIZES GATED OSCILLATOR

M. RAILESHA
World Friends, Design Group, 53 Sadras East, Kalpakkam 603102, Tamilnadu, India; (4117)-508.

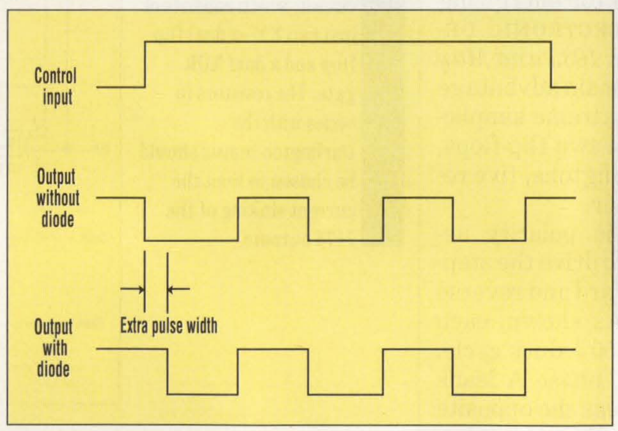
Popular as it is, the gated rectangular - wave oscillator based on a single NAND gate does have a couple of weaknesses *(Fig. 1)*. The most important is that the first pulse it puts out after being enabled tends to be longer than the ones that follow *(Fig. 2)*. The second is that it sometimes gets triggered by short stray pulses at its enable input.

Adding a single diode to the circuit *(dashed connections, Fig. 1)* can eliminate both problems. What the diode does very simply is to prevent the accumulation of charge on the capacitor while the oscillator is waiting to be triggered. That charge is responsible for the extra width of the first pulse.

The diode also prevents the oscillator from being activated by very short enable pulses. On the down side, although it stabilizes the oscillator frequency, it also introduces a short delay between the arrival of an enable pulse and the beginning of oscillation. A 1N914B diode was chosen for this application because of its low leakage characteristics.□



1. THE FIRST pulse from this gated oscillator removes any accumulated charge from the capacitor. Thus, it tends to be longer than the others. Adding a low-leakage diode (dashed connections) to the circuit prevents charge from accumulating and hence stabilizes the pulse width.



2. THE elongated pulse, which typically occurs without the diode (middle trace), is corrected when the diode is added (bottom trace). Note that the diode also adds a slight delay to the start of oscillation.

IFD WINNER

IFD Winner for July 11, 1991

Don Schendel, Motorola Inc., 6220 Roosevelt, P.O. Box 9040, Scottsdale, AZ 85252; (602) 441-6752. His idea: *"Build a Single Amp Component."*

IFD Winner for July 25, 1991

M.J. Salvati, Flushing Communications, 150-46 35th Ave., Flushing, NY 11354; (718) 358-0932. His idea: *"Probe Drives Low-Impedance Inputs."*

CIRCLE 523 GETTING REAL-WORLD DATA INTO SPICE

MICHAEL A. WYATT
Honeywell Inc., 13350 U.S. Hwy. 19N, M.S. 931-4, Clearwater, FL 34624; (813) 539-5653.

Entering real-world signals into Spice programs can be a nightmare. Spice has no facilities for accepting external stimulus waveforms and only limited ability to generate them internally. Nevertheless, it's possible to capture waveforms in the laboratory with a data-acquisition card and input them into Spice using an extension of the method described in a previous Idea For Design by Donald B. Herbert *("Create Spice Noise Sources,"* ELECTRONIC DESIGN, *Aug. 8, p. 99)*.

The Basic program presented here *(see program listing)* features a data-capture routine followed by a

Spice PWL (piece-wise linear) file-creation routine. The data-capture routine is based upon the PC-compatible PCL-711 PC-Multilab card from B&C Microsystems, Sunnyvale, Calif. Note that the number of samples is limited to 3995—the maximum number of PWL data points allowed by PSpice from MicroSim Corp. To determine the effective sampling rate of the system, simply read the PC's clock time before and after data collection, subtract the former from the latter, and divide the difference into the number of data samples.

The Basic program opens a file and creates a Spice-compatible .SUBCKT with a single PWL voltage source and a shunt resistor as its only circuit elements. Spice-compatible PWL voltage and time points are created by incrementing through the captured DTA% data array, converting the 12-bit data into equivalent voltages and computing the data sample time. A .MOD extension is appended to the file name to signify that it's a model file.

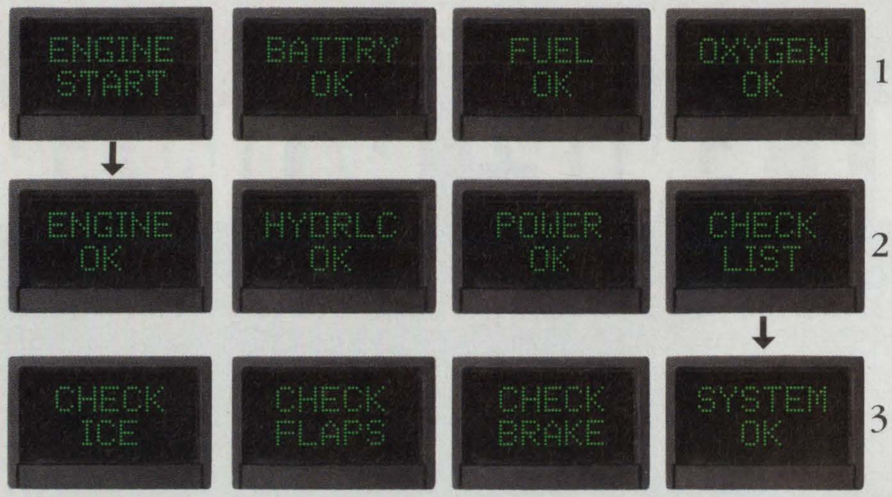
To use the newly captured data, a Spice net list should be created using the subcircuit definition *Xname +node -node INPUT*. In that definition, *INPUT* is the default name of the PWL subcircuit, and *+node* and *-node* are the connections for the PWL voltage source VIN within subcircuit *INPUT*. The model file containing the subcircuit can be called from Spice by using the .LIB command; for example, .LIB PWLDATA.MOD. That enables Spice to bring the subcircuit and PWL data into its net list from the model file PWLDATA.MOD.

The author will supply a copy of the program to anyone sending him a self-addressed stamped diskette carrier and a preformatted, 1.2-megabyte, 5-1/4-in. diskette.□

```
CLS
PRINT "*****************************************************************"
PRINT "*               SPICE DATA CAPTURE PROGRAM                      *"
PRINT "*  This program is used to capture data for use in SPICE        *"
PRINT "*  simulations with the PWL voltage source stimulus             *"
PRINT "*               Mike Wyatt  Aug 23, 1991                        *"
PRINT "*****************************************************************"
PRINT
PRINT
'
'          This program uses the PCL-711 PC-Multilab Card
'          From B&C Microsystems 355 W. Olive Ave.
'          Sunnyvale, CA. 408-730-5511
'
'          Use the PCL-711 12 Bit A/D on Address &H220
'          Analog Data channel 0
'
'                      ****** SET UP VARIABLES *****
DIM DTA%(3995)         'SET DATA ARRAY TO 3995 {PSPICE PWL LIMIT 3995 PTS}
PORT% = &H220          'SET PORT ADDRESS TO Hex 220
CH% = 0                'SET A/D CHANNEL ADDRESS TO 0
'
'                      ***** INPUT DATA LENGTH & DELAY ****
100                    'START OF INPUT
INPUT "NUMBER OF SAMPLES ? {1 - 3995} ", N    'PSPICE PWL LIMIT 3995 PTS
PRINT
IF N > 3995 OR N < 1 THEN 100 ELSE N% = N
INPUT "DELAY ? {1 - 32767} ", D               'DELAY VARIABLE
PRINT
IF D > 32767 OR D < 1 THEN 100 ELSE DELAY% = D
'
'                      ***** START OF DATA COLLECTION *****
TI = TIMER             'INITATE TIMER
OUT PORT% + 11, 6      'SET UP PCL-711 A/D
DUMMY = INP(PORT% + 4) 'READ DUMMY VARIABLE, CLEAR DRDY
OUT PORT% + 10, CH%    'SET UP CHANNEL ADDRESS {ADDRESS = 0}
'
T1 = TIMER             'READ START TIME
FOR LP1 = 1 TO N%      'COLLECT N 12 BIT WORDS LOOP N% TIMES
OUT PORT% + 12, 0      'TRIGGER A/D
200 DH% = INP(PORT% + 5)   'READ HIGH BYTE
IF DH% > 15 THEN 200   'CHECK DATA READY
DL% = INP(PORT% + 4)   'READ LOW BYTE
DTA%(LP1) = DH% * 256 + DL% - 2048     'STORE 12 BIT DATA AS DTA%(#)
FOR X = 0 TO DELAY%    'SAMPLE DELAY TIMER START
NEXT X                 'SAMPLE DELAY TIMER END
NEXT LP1               'COLLECT NEXT 12 BIT WORD
T2 = TIMER             'READ STOP TIME
T = T2 - T1            'COMPUTE ELASPED TIME
KV = 5 / 2048          'PCL-711 A/D GAIN CONSTANT {Vin=+-5v}
PRINT
IF T <= 0 THEN PRINT "ERROR IN READING TIMER" ELSE PRINT "SAMPLE RATE = "; N% / T
300 PRINT
INPUT "ENTER Y to Accept Data, N to Rerun Data, Q to Quit ? ", A$
IF A$ = "Y" OR A$ = "y" THEN 400
IF A$ = "N" OR A$ = "n" THEN 100
IF A$ = "Q" OR A$ = "q" THEN 1000 ELSE 300
'
'               **** DATA COLLECTION END ****
'
'
'               **** CREATE SPICE COMPATIBLE PWL FILE ****
'
'          See Reference Electronic Design 9/8/91 pg 99
'          Create Spice Noise Sources by D. Herbert
'
400 PRINT
INPUT "ENTER FILE NAME {8 Char Max} ? ", NAM$   'FILENAME FOR PWL DATA
IF LEN(NAM$) > 8 THEN 400
NAM$ = NAM$ + ".MOD"          'ADD .MOD TO FILENAME
OPEN NAM$ FOR OUTPUT AS #1    'OPEN FILE FOR OUTPUT
PRINT #1, ".SUBCKT INPUT 2 1"  'CREATE .SUBCKT INPUT
PRINT #1, "*SOURCE NODES + -"
PRINT #1, "VIN 2 1 PWL("      'CREATE VIN PWL VOLTAGE SOURCE
FOR I = 1 TO N%               'LOOP FOR N% DATA POINTS
TSAMPLE = T * (I - 1) / N%    'COMPUTE SAMPLE TIME
VOLTAGE = KV * DTA%(I)        'COMPUTE SAMPLE VOLTAGE
PRINT #1, "+";                'SPICE LINE CONTINUE PARAMETER
PRINT #1, USING " ##.###^^^^"; TSAMPLE;     'PRINT SAMPLE TIME
PRINT #1, USING " ##.###^^^^"; VOLTAGE      'PRINT SAMPLE VOLTAGE
NEXT I
PRINT #1, "+)";               'LAST DATA POINT
PRINT #1, " "
PRINT #1, "R 2 1 1000MEG"     'ADD 1000MEG SHUNT RESISTOR TO SATISFY SPICE
PRINT #1, ".ENDS INPUT"       'END SUBCKT INPUT
CLOSE #1                      'CLOSE FILE
600 PRINT : PRINT "SAMPLE RATE (HZ) ="; N% / T
PRINT "ELASPED TIME = "; T
PRINT
INPUT "ENTER Y for another data collection, Q to quit ", A$
IF A$ = "y" OR A$ = "Y" THEN 100
IF A$ = "Q" OR A$ = "q" THEN 1000 ELSE 600
1000 END
```

Send in Your Ideas for Design
Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.


CONDITIONED
"FRONT END" POWER
RUGGED AC-DC OFF LINE SOURCES
True N+1 current sharing for loads to kilowatts.
.99 power factor correction–provides 25% more usable power with low harmonic distortion.
Line isolation/EMI suppression to D0160B and Mil-Std-461 (including CE01, CE03, RE02).
Surge/spike protection per Mil-Std-704D and Mil-Std-1399.
INPUT
ADJ
CTRL
OUTPUT
28 V
DC OUTPUTS
24 to 300V available
(including 28V, 48V, 155V, 270V)
AC INPUTS
1ϕ and 3ϕ available
POWER BUS
LOCAL DC TO DC CONVERTERS
NEW
PB Series
IDEAL FOR USE
WITH DISTRIBUTED POWER
DC-DC CONVERTERS AND SYSTEMS
Features include 600 watt low profile 2″ high package; lightweight, unpotted designs; environmental performance to Mil-Std-810D; –55°C to +85°C operation without derating; extended MTBF greater than 350,000 hours...
Call toll free for additional technical information and application assistance 1-800-421-8181 (in California 805/484-4221)
ARNOLD MAGNETICS
ARNOLD MAGNETICS CORPORATION
4000 Via Pescador, Camarillo, California 93012 • Phone: (805) 484-4221 • Fax: (805) 484-4113
CIRCLE 92 FOR U.S. RESPONSE
CIRCLE 93 FOR RESPONSE OUTSIDE THE U.S.



AN APPLICATIONS EXAMPLE.
While the following example is for aircraft, it could apply to any air, land, sea or space system.

SEQUENCE ONE: The four-pushbutton display reads "ENGINE START," "BATTERY OK," "FUEL OK," OXYGEN OK." The operator selects "ENGINE START."

SEQUENCE TWO: The four-pushbutton display now changes to read "ENGINE OK," "HYDRLC OK," "POWER OK," "CHECK LIST." The operator selects "CHECK LIST."

SEQUENCE THREE: The four-pushbutton display now reads "CHECK ICE," "CHECK FLAPS," "CHECK BRAKE," "SYSTEM OK." In this manner, the designer can program in as many sequences as required.

Design flexibility: The programmable display system.

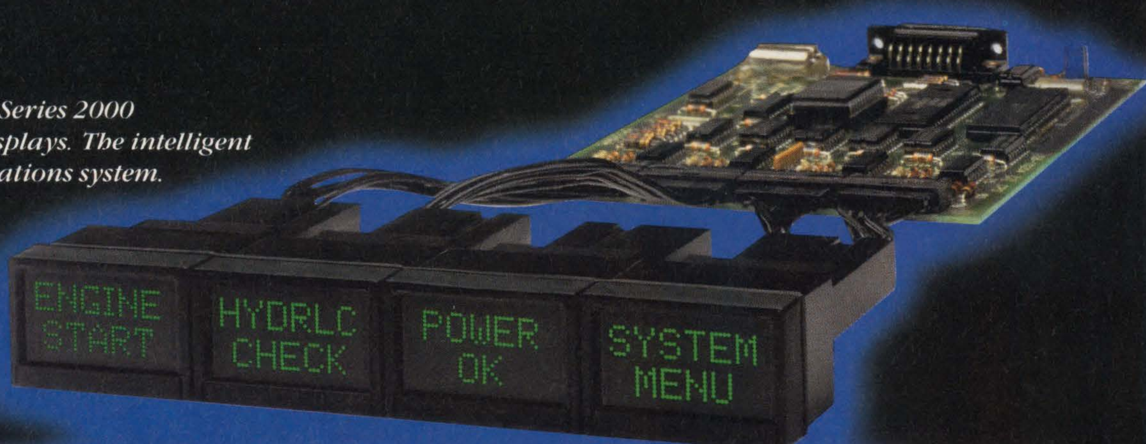
Vivisun Series 2000, now the leading programmable display pushbutton system, interfaces the operator with the host computer. The user-friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence with no errors and no wasted time.

They also simplify operator training as well as control panel design. One Vivisun Series 2000 programmable display system can do the work of 50 or more dedicated switches. In short, Vivisun Series 2000 gives the design engineer more control over the design.

Contact us today.

AEROSPACE OPTICS INC.
3201 Sandy Lane, Fort Worth, Texas 76112
(817) 451-1141 • Telex 75-8461 • Fax (817) 654-3405

Vivisun Series 2000 programmable displays. The intelligent communications system.



SERIES
VIVISUN 2000™

CIRCLE 82 FOR U.S. RESPONSE
CIRCLE 83 FOR RESPONSE OUTSIDE THE U.S.

ELECTRONIC DESIGN

QUICK LOOK

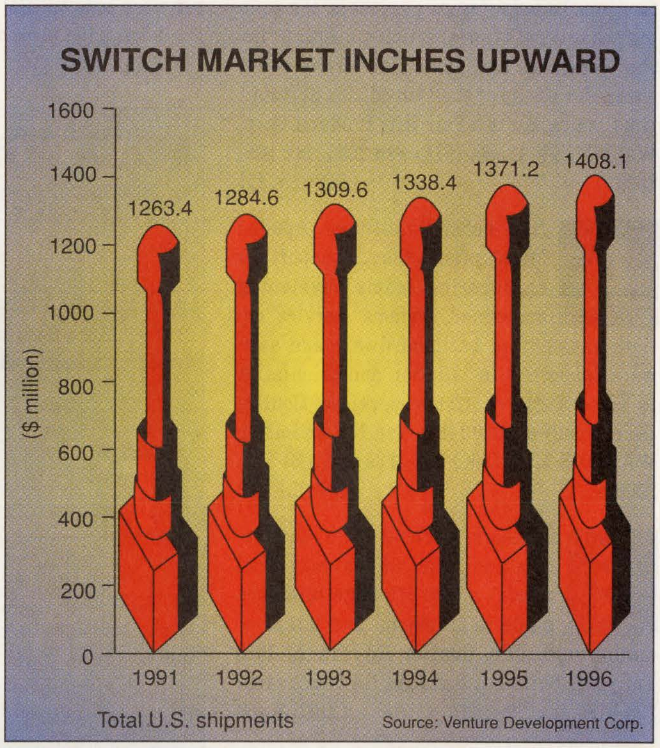
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Beset by mergers and acquisitions, the switch industry is eking out profits from narrow margins. "Everybody has the same switches," says Murray Klapfish, vice president at Venture Development Corp., a market research company in Natick, Mass. As a result, vendors are trying to capitalize on every competitive advantage, putting terminals in customer sites for placing and tracking orders. Increasing use of just-in-time manufacturing will continue to benefit switch users, Klapfish points out.

In terms of volume, the switch market shows good growth—the number of switches sold more than doubled between 1985 and 1990, from 801.5 million switches six years ago to 1.906 billion last year. But an aggressive price war has wilted profits, with total dollar value increasing just 1.8% to $1.24 billion in 1990. U. S. vendors have lost revenues because of low-cost switches made offshore, according to Venture Development's report, *The Market for Switches in the Electronics Industry*, second edition.

Outside of cutthroat pricing among vendors supplying in volume, the switch picture has some bright spots. For example, vendors are becoming involved in customers' design processes, supplying subassemblies and system integration. Vendors also have an edge if they support electronic data interchange with just-in-time manufacturing. Demand is strong for switches in medical gear; as the U. S. population ages, that demand should stay strong.



TALES FROM THE SKUNK WORKS

Past columns have discussed the composition of a skunk works and the attributes of the people who can make one work. These are the fundamentals, fuzzy as they may seem. A skunk works does not lend itself to formalism, procedure, and rules; it is subtle and dependent on people. The unorthodoxy of a skunk works makes some people uncomfortable.

We fear that trusting individuals in important matters leads to irresponsibility, discrimination, or worse. What of Vietnam, the Contra affair, banking debacles, and decades of expensive technology playpens and marketing mistakes? What of career risk and accountability to the stockholders? Traditional managers resist assigning their people to a skunk works and losing control.

Large organizations and the government—with inspiring exceptions like H. Ross Perot and Norman Schwarzkopf—often try to avoid trusting people. Conversely and despite recent problems, the Japanese generally trust personal relationships and work in teams. Here we correct breach of law; there they punish violation of trust. Independent of talent and character, we presume that technique, process, and procedure can make us competitive.

A skunk works requires that we distinguish a diversity of people by ability and integrity. It is a serious business endeavor, not a technology sandbox. The skunk works exists only to provide a business advantage for the corporation and extraordinary value for customers. The burden of freedom is responsibility and the skunk works is accountable in all dimensions.

Members of a skunk works team are responsible to each other, to their leader, and to the company for delivering as promised by *their* plan. When the budget is depleted, there is no more. If a milestone is missed, the program is jeopardized. One person's failure may cause the team to fail. In return for accepting grave responsibility, the skunk works is allowed to work unmolested. The alternative to dramatically increasing our creativity is unpleasant, I think. We are, despite excellent technology and a few notable exceptions, losing our leadership in high tech. Companies are going out of business even in growth markets. With boring consistency we are driven from the lucrative markets that we create. Now experts advise exiting the manufacture of computers. Our choice is radical change or continued decline.

John D. Trudel, the Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300.

QUICKLOOK

OFFERS YOU CAN'T REFUSE

A revised catalog covers the Fair-Rite product line of soft ferrite materials, components, and accessories for application in EMI suppression, high-frequency power magnetics, trandsducers, chokes, and broadband transformers. To help design engineers, the catalog has several tutorial articles, magnetic design formulas, and other soft ferrite references. For a copy of the 11th edition Soft Ferrite Catalog, contact Fair-Rite Products Corp., Wallkill, NY 12589; (914) 895-2055; fax 895-2629. CIRCLE 451

A free booklet describes Applied Microsystems Corp.'s support for engineering teams developing embedded systems. Service options range from basic hardware and software support to installation and orientation to comprehensive system services. Contact the company at 5020 148th Ave. NE, Redmond, WA 98073-9702; (800) 343-3639 or (206) 882-2000. CIRCLE 452

Engineers working with data-acquisition applications may find helpful a free 120-page reference guide to industrial and lab automation with PCs. Contact Advantech, 1310 Tully Rd., Suite 115, San Jose, CA 95122; (408) 293-6786; fax 293-4697. CIRCLE 453

A free demo disk is available for a schematic entry program for circuit diagrams. SuperCAD includes a large library, netlister, and dot matrix printer output. Contact Mental Automation, 5415 136th Place SE, Bellevue, WA 98006; (206) 641-2141. CIRCLE 454

EasyPlot, a plotting package developed at MIT Lincoln Laboratory, offers fast graphs and sophisticated data analysis. For a free working demo, contact Spiral Software, 6 Perry St., Suite 2, Brookline, MA 02146; (617) 739-1511; fax 739-4836. CIRCLE 455

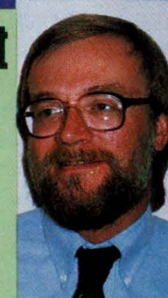
A 368-page illustrated catalog, besides covering LeCroy instrumentation products, includes technical data sheets and specifications, application notes, and examples. Also included is a tutorial with a glossary on using research instrumentation. The 1992 Research Instrumentation Catalog is available free from Lecroy Research Systems Div., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 425-2000. CIRCLE 456

HOT PC PRODUCTS

With Back & Forth Professional, PC users can switch between up to 20 programs at once. As a result, a user can press a key or click a mouse to shift between a word processor, spreadsheet, database, graphics program, and terminate-and-stay resident (TSR) utilities. The program includes calculators that use no additional memory. The program takes up only 23 to 33k of memory, 1k if loaded into high memory. Back & Forth works with CGA, EGA, Hercules, VGA, Super VGA, and 1024-by-768 video modes. The software runs on IBM PCs, XTs, ATs, and PS/2, and a network version is available. Back and Forth has a list price of $69.95. Contact Progressive Solutions, 177 East 79th St., New York, NY 10021; (212) 794-9341. CIRCLE 457

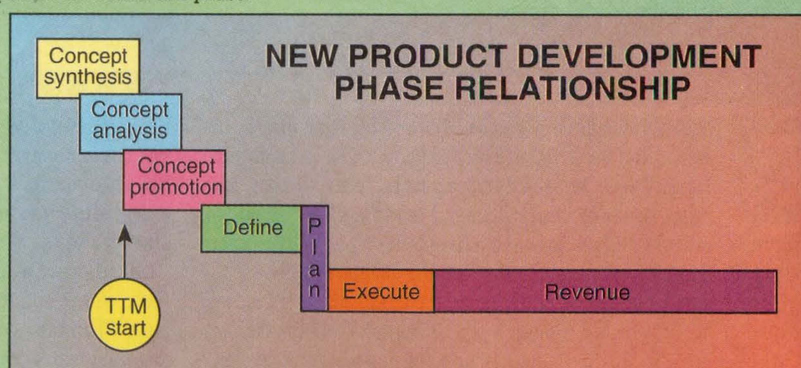
KMET'S KORNER

...Perspectives on Time-to-Market



BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

The previous column defined the point where measurement of time to market begins. Now let's consider the implications of starting the measurement ahead of concept promotion. Successfully promoting an idea within an organization scales in proportion to how familiar decision makers are with the concept—that is, familiar items are easier to promote than less familiar ones. Along the same lines, advancing familiar ideas, supported by development and market data, is generally easier than pushing something new. Using previously introduced concepts behind me-too-with-a-twist, next-generation, derivative, and first-of-a-kind product development classifications helps foster an understanding of potential complications within this phase.

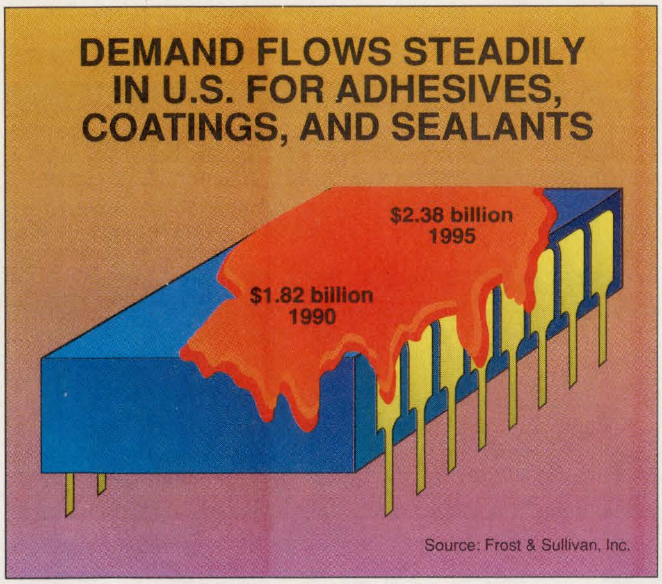


Measuring how long it takes for ideas to transit the promotion phase within the organization becomes extremely important. Many new product development organizations suffer significant degradation in time-to-market performance and don't even know it!

A second benefit of making the measurement—removing the idea analysis log jam—results as well. This happens because measurement surfaces the quantity of ideas present in just about every product development environment. Once quantity becomes known, it is necessary for those doing the evaluation of ideas to create effective filters to improve selection of concepts with high quality while reducing the total number of those in process.

The fact remains that the time to transit the concept promotion phase within most any organization is measured not in days or months, but in years. As such and in proportion to other phases that lead to the revenue phase, it consumes precious time. Including this time interval in time-to-market measurement will likely alter organizational behavior. It can lead to reducing overall the time to market of products selected for development.

QUICKLOOK



QUICK REVIEWS

Engineering managers and designers in the U. S. are facing the challenge of innovating in the marketplace. To do that, people have to be in charge. That's the assertion of William B. Rouse, author of *Design for Success: A Human Centered Approach to Designing Successful Products and Systems.* The book outlines design philosophies and methods for developing complex systems with a primary goal of supporting people. In Rouse's view, the purpose of design is not to mobilize technology to achieve operational objectives. Rather, design should be oriented toward integrating technology and other resources to support people in ways that help them do their jobs.

As Rouse explains, the first goal in human-centered design is that it should enhance human abilities, taking advantage, for example, of people's excellent pattern-recognition abilities. Not surprisingly, the second goal is that it should help overcome human liabilities—the human tendency to make errors, for instance. Third, such design should foster user acceptance. Design must directly address users' preferences and concerns.

Within Rouse's framework are four design issues: formulating the right problem, designing an appropriate solution, developing it to perform well, and assuring user satisfaction. User-centered design and user-friendly systems aren't new ideas, of course. But few people know how to put these concepts to work. Rouse presents a framework of design procedures that address design issues step by step. Still, Rouse's framework is intended to support and enhance engineering judgment, not replace it. The book's case studies make concrete the rather abstract ideas in human-centered design. In one case study, the problem was information overload experienced by aircraft pilots. The design of an intelligent cockpit involved interviewing 10 fighter pilots about having advanced technology in the cockpit and incorporating these results in later design phases.

William B. Rouse is chairman and chief scientist of Search Technology. Rouse is adjunct professor of industrial and systems engineering at the Georgia institute of Technology. He received his doctorate in systems engineering from the Massachusetts Institute of Technology.

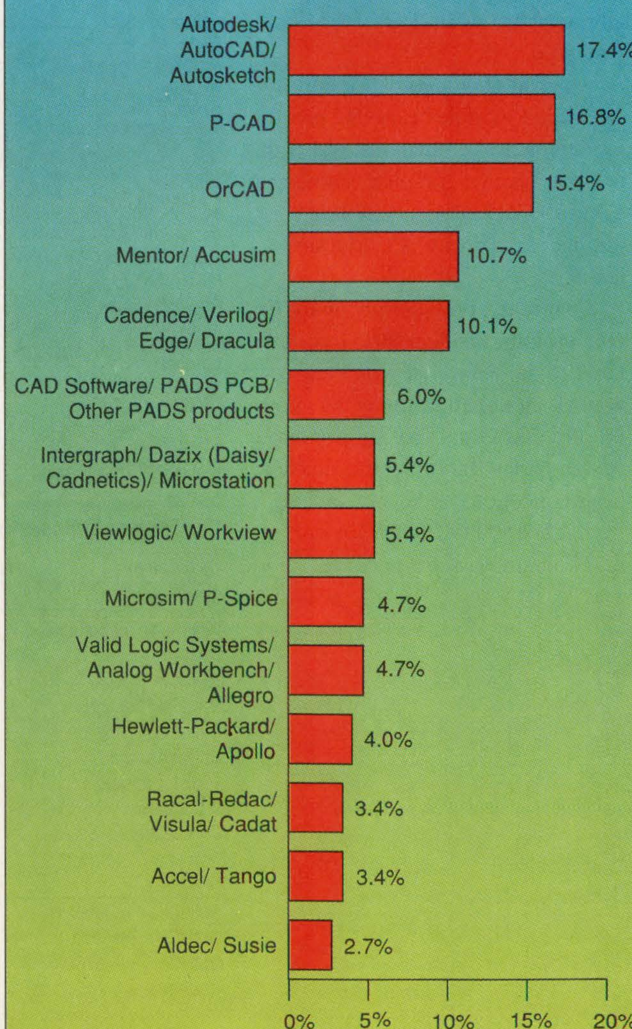
Design for Success, amply illustrated, lists for $44.95. The 270-page book is published by John Wiley & Sons, 1991. New York; (800) 225-5945, ext. 2497. (ISBN 0-471-52483-2).

QUICK NEWS

Fascination with how things work and a resulting interest in math and science may lead to an engineering career. Thinking along these lines, some 20,000 engineers will visit classrooms across the U. S. from February 16 to 22 to encourage students to take the math and science courses they need to prepare for enginering careers. Thirteen engineering societies sponsor the National Engineers Week for 1992, along with funding from 10 corporations,. The event's honorary chairman is Jack D. Kuehler, president of IBM Corp. Engineers who wish to participate can request a Discover E kit from National Engineering Week, P. O. Box 1270, Evans City, PA 16033; (412) 772-0950.

CAD/CAE SURVEY

WHICH CAD/CAE SOFTWARE WOULD YOU CONSIDER FOR FUTURE PURCHASE?



Source: a survey of Electronic Design readers by the Adams Co., Palo Alto, Calif.; (415) 325-9822

BEST OF THE '90s

NKK backs you with over 1,001,250 different toggle, rocker, pushbutton, slide, lighted, keypad, keylock, rotary and DIP rotary switches — including the best new ideas of the '90s. See them all in the pages of our new 456-page switch catalog. For your free copy, call (602) 991-0942 or FAX (602) 998-1435.

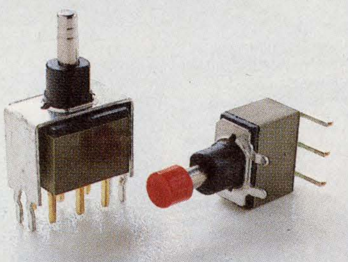
NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260

nkk switches

WORLD'S SMALLEST

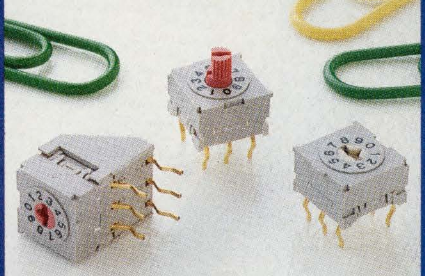
NKK introduces the surface mount G3T with patented STC contacts, gull-wing terminals. VPS or infrared reflow solderable.

EASY DOES IT



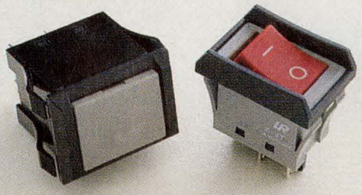
Washable M2B subminiature pushbuttons feature very-light-touch, snap-acting contacts. Straight, right angle, vertical PC terminals.

ULTRA-MINI

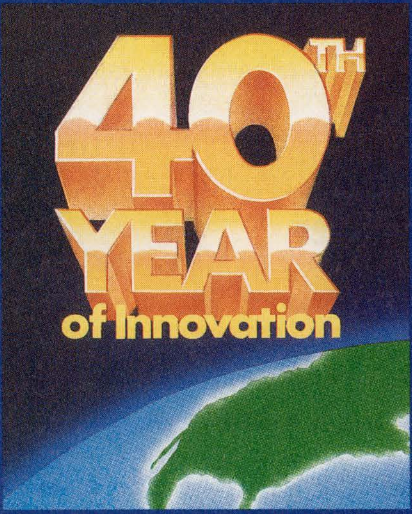


New ND switch is half the size of ordinary binary coded DIP rotaries. Washable and universal footprint pattern.

TV STAR



JW rockers & JP pushbuttons. High inrush current resistance protects against contact welding. TV-8 (16 Amp) + TV-5 (10 Amp) Rated.



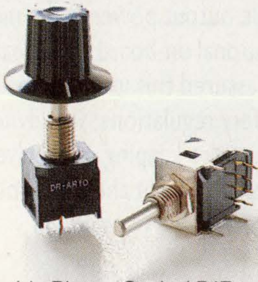
WORTH A MILLION

Million operations from unique LED illuminated JB keypad switch. Red, green or yellow LED options.

DOUBLE DUTY

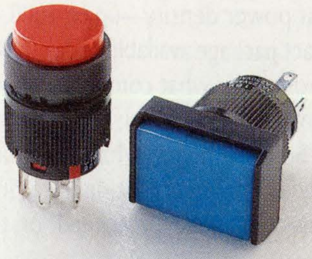
Logic-level for PCB or power rating for snap-in panel mounting, from very low-profile UB pushbuttons with full-face LED illumination.

TURNING POINT



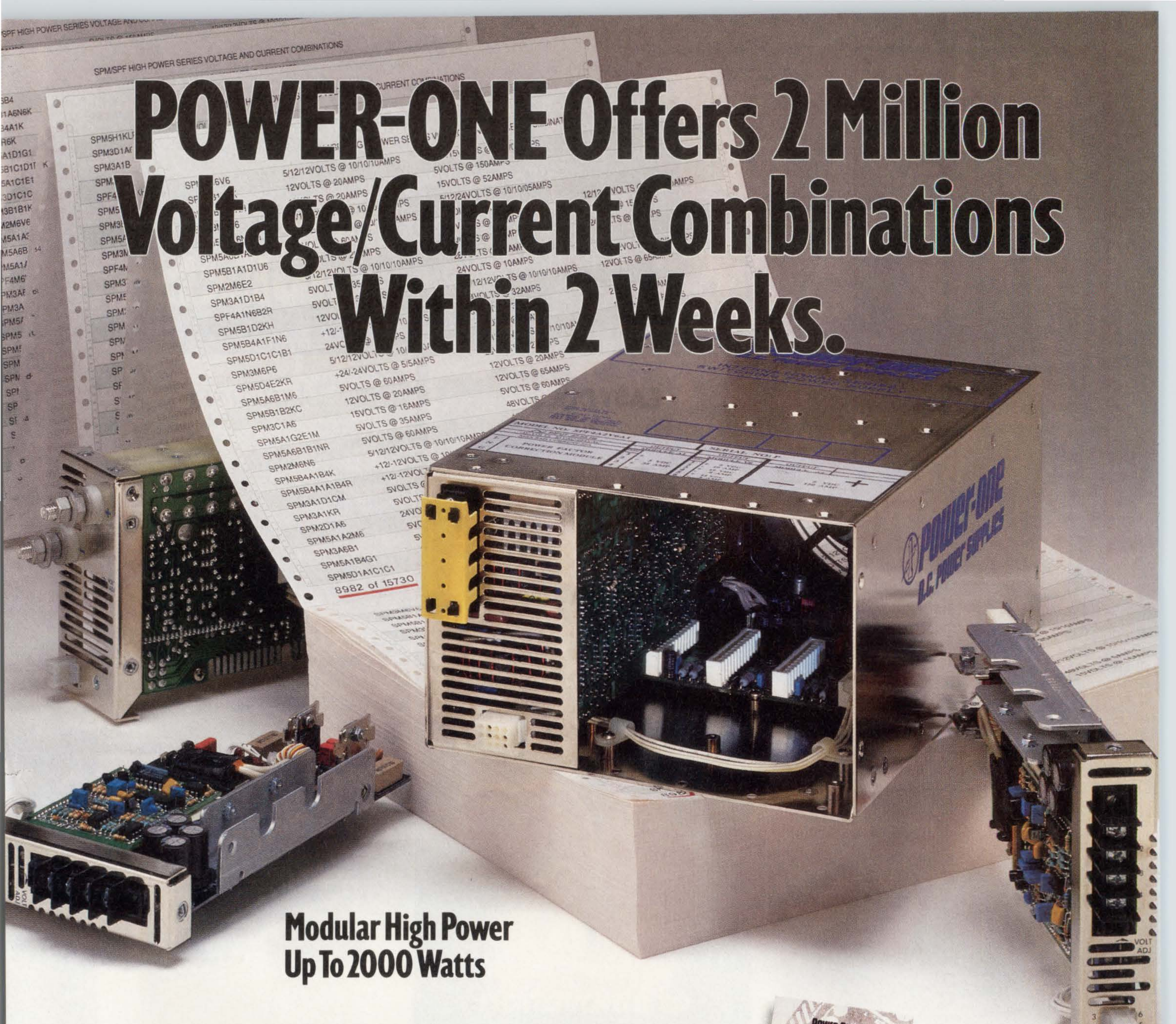
Washable Binary Coded DIP rotary DR-A switch can be PC or panel mounted. Crisp operation. Right angle or straight terminals.

100,000 CHOICES



YB pushbutton yields literally 100,000+ part numbers with variations in mounting, illumination, circuitry and color.

POWER-ONE Offers 2 Million Voltage/Current Combinations Within 2 Weeks.



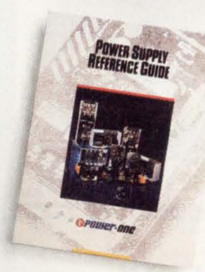
Modular High Power Up To 2000 Watts

You're in the initial stages of design. You need a prototype and you're facing a deadline. You also need a power supply with specific voltage/current outputs. And you need it fast!

That's where POWER-ONE's fully modular SPM High Power Series comes in. Single, dual, or triple output modules enable you to specify up to 15 DC outputs...from stock. With delivery time as little as two weeks.

And there's more. The incredibly versatile SPM represents the industry's highest power density—up to 2000 watts of multiple output power in the most compact package available today. There's even an optional on-board UPS capability. And no matter what configuration you require, be assured this internationally recognized power supply will meet the toughest safety regulations, worldwide.

So remember....whatever your requirements, we're keeping our shelves stocked for those urgent, limited-quantity deliveries. You'll get the exact voltage/current combination you need, on time. Every time.



Get Complete Details Today. Call our Toll Free LITERATURE HOT-LINE for our Sensational New Tutorial and Product Catalog! (800) 678-9445

"Innovators in Power Supply Technology"

POWER-ONE
D.C. POWER SUPPLIES

POWER-ONE, INC.
740 Calle Plano • Camarillo, CA 93012-8583
Phone: (805) 987-8741 • FAX: (805) 388-0476

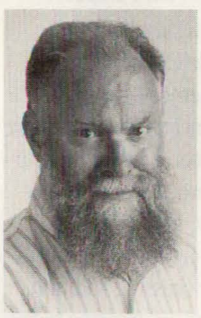
CIRCLE 146 FOR U.S. RESPONSE   CIRCLE 147 FOR RESPONSE OUTSIDE THE U.S.

PEASE PORRIDGE

WHAT'S ALL THIS PSRR VS. FREQUENCY STUFF, ANYHOW?

Recently a reader asked me about the shape of the curve of an op amp's PSRR (power-supply rejection ratio) versus frequency. He observed that any curve of CMRR (common-mode rejection ratio) versus frequency which is the same as the gain versus frequency curve is probably an error or a foolish piece of bad data taking.

How about PSRR curves? Is a PSRR versus frequency curve in error if it's the same curve as the gain curve? In general, the answer is no. If the curves appear the same, they probably really are the same. Here's why: Every op amp has one (or more) capacitors that roll off the amplifier's gain versus frequency. At one end, the main "Miller" capacitor's voltage moves as far as the output voltage. At the other end, the capacitor is referenced to one of the power supplies – sometimes the minus supply, sometimes the plus supply. In the old days of vacuum-tube amplifiers, the main roll-off capacitor was sometimes actually referred to ground (refer to the old Philbrick K2-W, etc.). So if there was some motion on the minus or plus 300-V supply, the output had no direct path to cause it to move.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

But in the solid-state era, very few op amps are referenced to ground – the minus or the plus supply is the place where the compensation capacitor is referred to.

Please look into the 1976 article by James Solomon in the *IEEE Journal of Solid-State Physics*, VOL SC-9, No. 6 (also reprinted as Appendix 1 in the *NSC Linear Applications Data Book*, 1986-1990). Mr. Solomon confirms that most op amps will indeed have a PSRR that's similar to the A_V versus frequency, at least for one of the supplies.

Are there any exceptions, any amplifiers for which the PSRR is better than the gain? If you take an LM301A and connect it with 30 pF from pin 1 to pin 8, and then add 30 pF from pin 5 to ground, that can help cancel out or neutralize the ac PSRR.

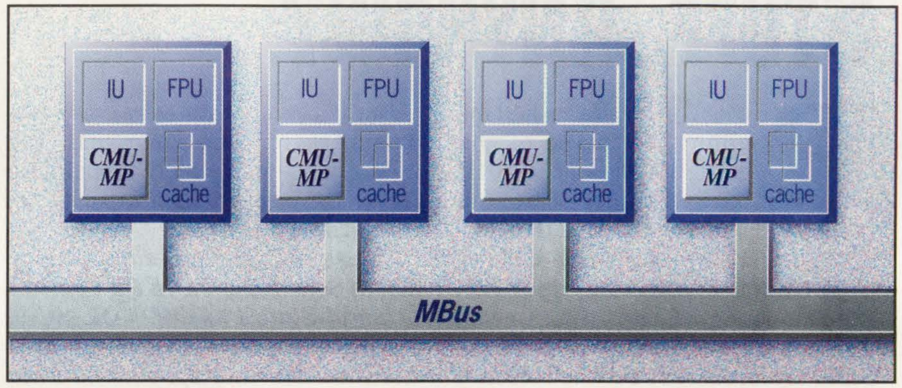
If you take an LM308, you might damp it with 30 pF from pin 1 to pin 8. OR, you might connect a 100-pf capacitor from pin 8 to ground. That would yield a much better PSRR versus frequency curve than the normal Miller-integrator scheme with capacitance from pin 8 to pin 1.

There are also some other amplifiers where the PSRR can be made very large at high frequencies. Noise gain damping can often be advantageous. So, in a case where you have problems, *thinking* is the order of the day, followed by *measuring*.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

Address:
Mail Stop C2500A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

A REVOLUTIONARY ADVANCE IN SPARC MULTIPROCESSING.



SPARC multiprocessing is now enabled. Now you can design-in multiple high-performance SPARC chipsets. Our revolutionary Multiprocessing Cache Controller and Memory Management Unit (CMU-MP/CY7C605) provides memory management facilities and a unique cache architecture for higher performance. Our complete SPARC chipset solution shortens your time to market.

The industry's first integrated SPARC® multiprocessing solution — the CY7C605 Multiprocessing Cache Controller/MMU.

High-performance systems designers have migrated to RISC in a race for performance. Just as rapidly, there is a movement to multiprocessing, which represents the most cost-effective way to load more power into a single system.

Multiprocessing RISC design is not simple. There are substantial technological challenges, particularly in the area of multi-level memory systems.

Now we offer a breakthrough to help you implement multiprocessing systems rapidly.

Cache coherency without stealing processor cycles — a leap in performance.

Maintaining cache coherency is one of the biggest problems to solve in shared memory multiprocessing systems.

This approach solves it.

Pin compatible with our CY7C604 Uniprocessing Cache Controller/MMU, this new device lets you cascade to build cache size to 256K.

It is the only VLSI solution that performs concurrent bus snooping and processor execution.

Our unique dual cache tag directories provide for simultaneous bus snooping and processor access to cache. No other cache management unit provides dual tags on-chip.

As a result, your system maintains cache coherency without stealing execution cycles from the microprocessor.

You get multiprocessing with the most efficient cache coherency protocol available, allowing data to pass from CPU to CPU in a single clock cycle. That translates directly to higher performance systems.

MBus compliant.

MBus compliance means you have a SPARC-standard, plug-and-play route to even more powerful, higher revving systems.

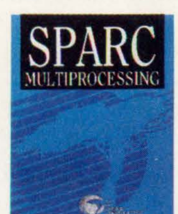
An integrated part of the industry's highest performance SPARC chipset.

Our chipset approach simplifies the complexities of multiple CPUs working together in a shared memory system.

This VLSI solution means you don't have to design and pay for boards full of logic to accomplish fast multiprocessing.

It is all available now.

For more information on the industry's most complete multiprocessing solution, please call for our literature package today.



Multiprocessing Information Hotline: 1-800-952-6300.*
Ask for Dept. C3V.

CYPRESS SEMICONDUCTOR

ADDING LIGHT SENSORS TO MIXED-SIGNAL CELL LIBRARY CREATES SENSOR CHIP WITH INTEGRATED SUPPORT CIRCUITRY.

INTELLIGENT OPTOELECTRONIC SENSOR CUTS DESIGN COSTS

MILT LEONARD

Although using discrete devices and multichip modules is traditionally the best way to combine light-sensing capability with digital-logic and analog signal-processing functions, this approach results in the need for costly custom packages. Now, with a family of intelligent optoelectronic sensors from Texas Instruments, designers can overcome these disadvantages.

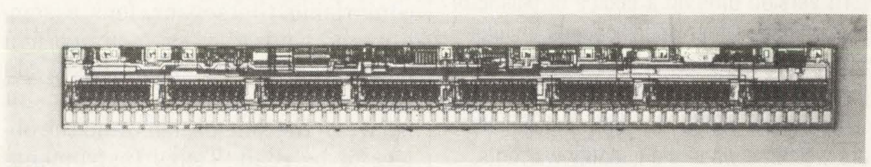
Texas Instruments' integrated devices combine light-sensing cells with cells for op amps, comparators, data converters, transmission gates, and timing and control logic, on the same piece of silicon. Compared to the multichip module approach, the company's intelligent sensors require less design effort and use less circuit-board space in terms of both footprint area and circuit traces.

The first sensor spawned by the Texas Instruments's LinBiCMOS design methodology is the TSL214, a 64-by-1-element imager *(Fig. 1)*. The sensor portion of the device consists of 64 charge-mode pixels arranged in a 64-by-1 linear array. The device is sensitive to light wavelengths ranging from 350 nm to 1200 nm. Each of its pixels measures 120 μm by 70 μm, and is situated on 125-μm centers.

The device's integrated support circuitry, formed by 2500 equivalent gates, includes a 64-bit static shift register, and an analog buffer with sample-and-hold capability for the analog output over a full clock period. Each sensor cell is capable of 4-bit resolution. The TLS214 sensor has extendible data I/O for expanding the number of sensors as required.

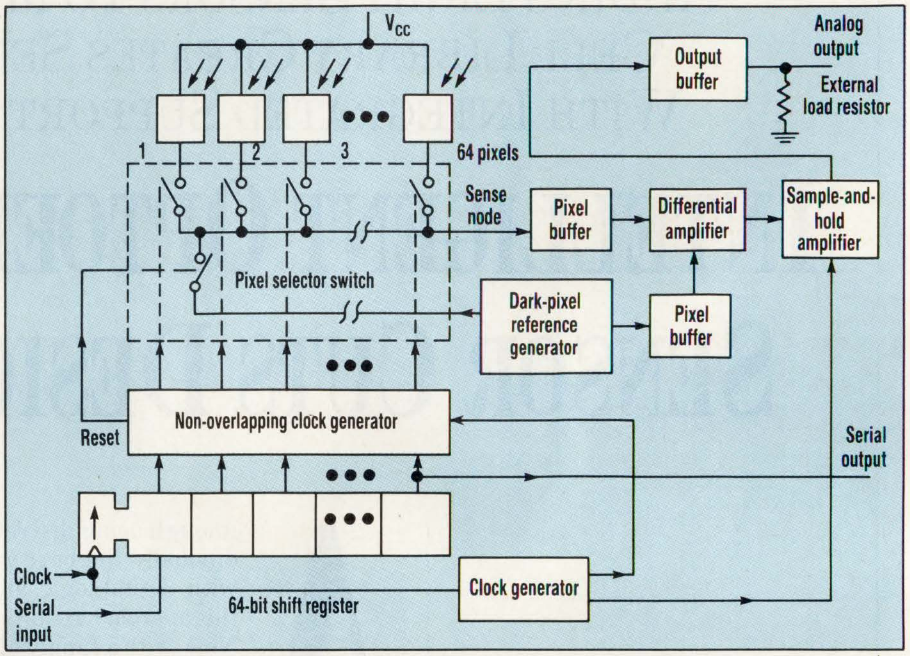
Aside from connections to a 5-V power source and ground, the TSL214 only requires a 500-kHz shift-clock signal and a start-integration-pulse signal to operate *(Fig. 2)*. The clock signal controls charge-transfer, pixel-output, and internal reset operations.

The sensor's serial input is a user-supplied pulse that defines the end of the



1. A LINEAR ARRAY of 64 light-sensing cells on the TSL214 sensor is located along the bottom edge of a 0.320-by-0.036-in. chip. The eight multiplexers for sequencing the pixels are located just above the pixel array. Across the top of the bar are a trimming network for setting the amplifier gain, clock-generator circuits, bond pads, and the dark-reference pixel. The bar is packaged in a 14-pin DIP, though seven pins have no internal connection to the chip.

INTELLIGENT PHOTOSENSOR



2. TI'S MIXED-SIGNAL TECHNOLOGY allows the digital shift register and clock circuits to share the same chip with the analog buffer and amplifier functions. The only user-supplied inputs required are the clock source and the serial input pulse, which initiates the pixel output sequence. The serial output pin supplies a carry pulse to another cascaded TSL214.

integration period and starts the pixel output sequence. This signal, which appears at the analog output pin, is a series of 2-V pulses from illuminated pixels.

The serial output pin provides a carry pulse to the serial input of another TSL214 sensor, allowing a cascading arrangement. A non-overlapping clock generator prevents cross-talk between sensor cells by ensuring that one cell is turned off before an adjacent cell in turned on.

The sensor is available in a clear plastic 14-pin DIP for use with lenses and light sources supplied by the user. The TSL214 can also be supplied as a complete reader assembly comprising the sensor, lens assembly, and source LEDs mounted in a plastic carrier. The plastic assembly assures correct physical alignment between the sensor, lens, and the object to be read. Texas Instruments also offers an evaluation package that includes the TSL214, clock generator, the serial-input pulse source, and lens assembly.

Target applications for the new optoelectronic sensor include linear encoding, bar-code readers, edge detection for applications involving paper handling, and level sensing, and low-resolution contact imaging. Additional standard products being developed include a quadrant sensor and a light-to-voltage converter.

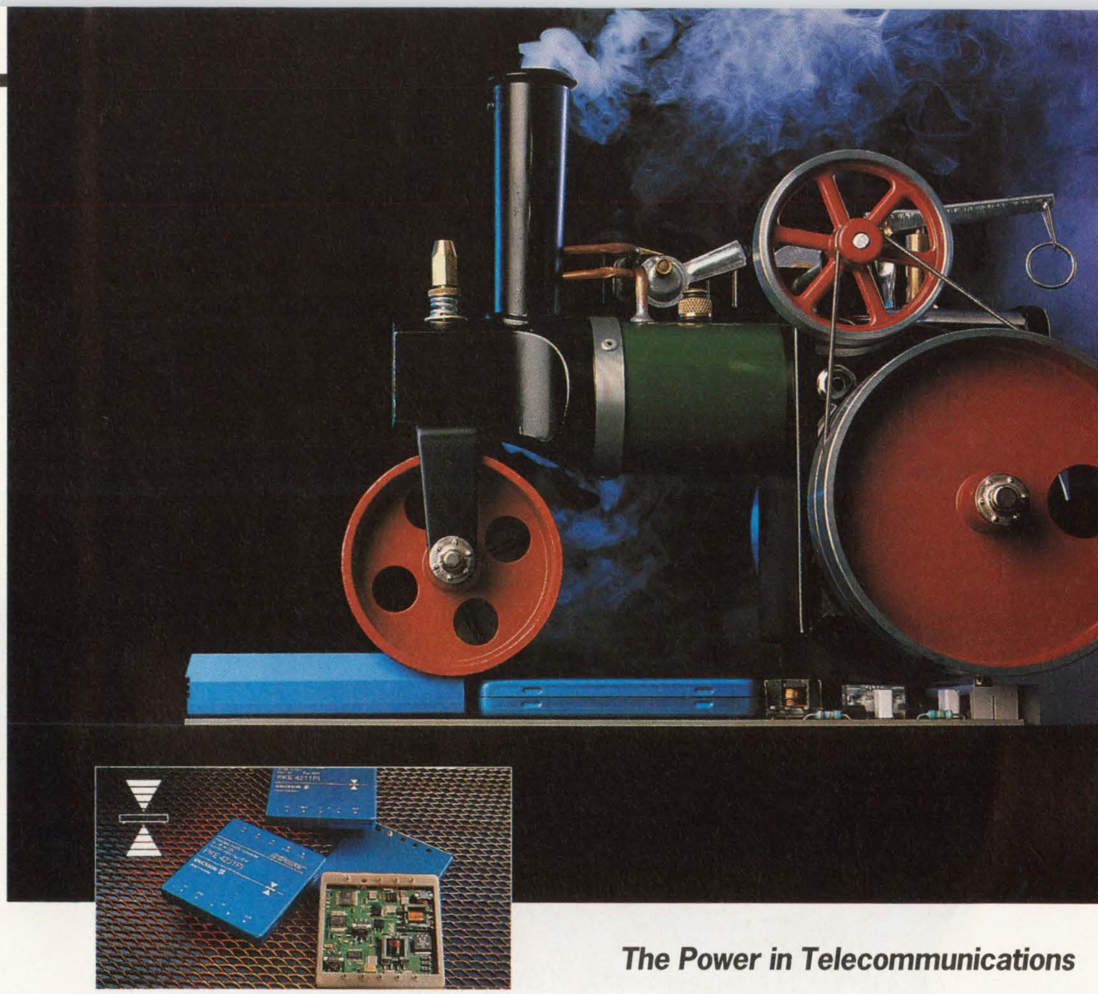
Texas Instruments says that its LinBiCMOS technology allows for many combinations of imager cell topology, cell size, and peak-wavelength response. A number of clear-epoxy package options for custom applications are also available, including multichip approaches. These multichip approaches are still needed in some applications for their advantages in optical isolation.□

PRICE AND AVAILABILITY

The TSL214 optoelectronic sensor is available four to six weeks after receipt of order for $6.50 each in quantities of 1000.

Texas Instruments, Inc., 8360 LBJ Freeway, Center 2, Dallas, Texas 75243; Nelda Burnside, (214) 997-3772. **CIRCLE 516**

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546



The Power in Telecommunications

The squeeze is on

Slimming is an obsession in the electronics industry as engineers face the task of making thinner cards to fit even more functions into standard racks. Once again Ericsson can help.

The new PKE is a 25-30 W DC/DC converter squeezed into a slim package little more than half the height of its predecessor, the internationally acclaimed PKA converter. The PKE is only 10.7 mm (0.42") high and has the same 3"x3" industry-standard footprint and pin out.

Having set the standard for DC/DC converters in 1983, Ericsson's new series represents a remarkable leap forward in power supply technology. The PKE needs no power derating over its entire ambient temperature range of -45 to +85 °C. Quite simply, no one else achieves this in so little space. And you can choose from versions with one, two or three regulated outputs.

Perhaps most surprisingly, performance is in no way compromised by the size reduction. In fact, the PKE is even better than the PKA. A wide input voltage of 38 to 72 VDC is complemented by 1500 VDC isolation, 80-85% typical efficiency and two million hours MTBF at +45 °C ambient.

The PKE converter from Ericsson - slim, compact and beautifully formed. Squeeze in the time to call us for more information.

Please send me your latest information

Name

Company

Job Title

Address

Telephone

Fax

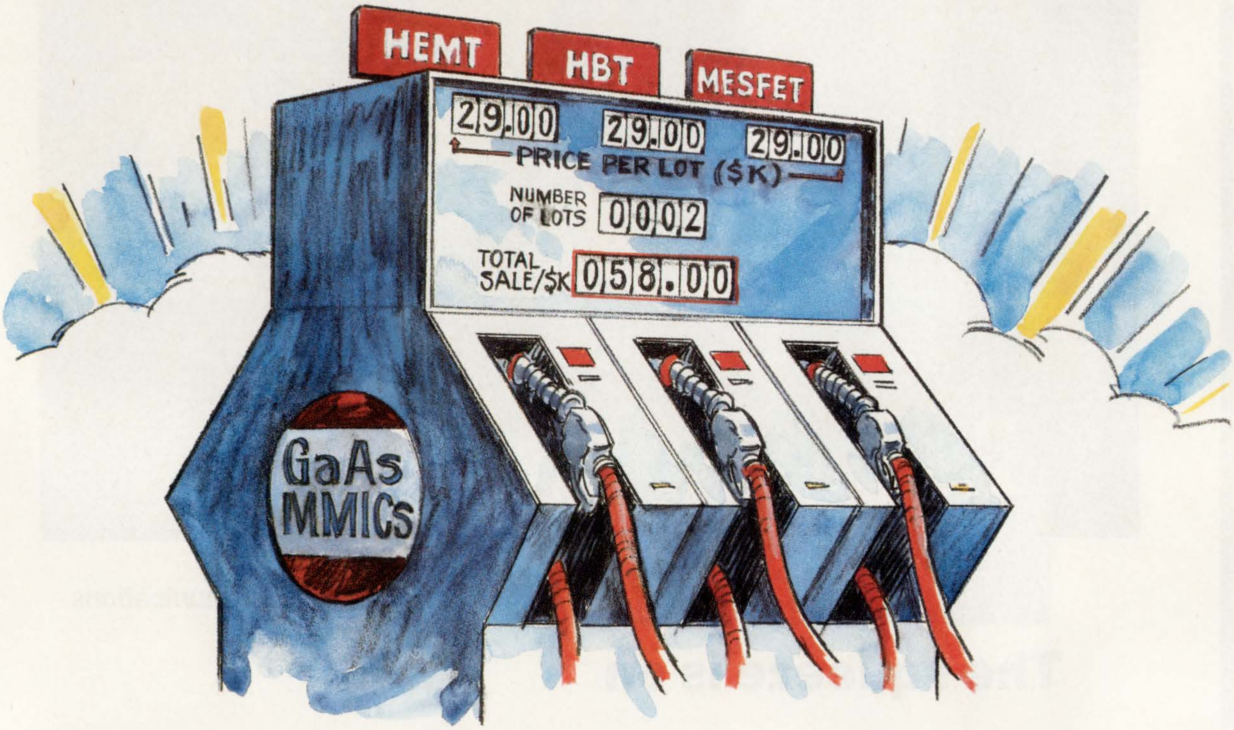
France: **Ericsson Components Europe,** Guyancourt, Tel: +33-1-30 64 85 00 Fax: +33-1-30 64 11 46
Germany: **Ericsson Components Europe,** Neu-Isenburg, Tel: +49-6102-200 50 Fax: +33-6102-20 05 33
Great Britain: **Ericsson Components Europe,** Coventry, Tel: +44-203-55 36 47 Fax: +44-203-22 58 30
Hong Kong: **Ericsson Components,** East Asia, Wanchai, Tel: +852-5-75 66 40 Fax: +852-834 53 69
Italy: **Ericsson Components Europe,** Milano, Tel: +39-2-33 20 06 35 Fax: +39-2-33 20 06 41
Norway: **Ericsson Components A/S,** Oslo, Tel: +47-2-65 01 90 Fax: +47-2-64 41 38
Sweden: **Ericsson Components AB,** Stockholm, Tel: +46-8-757 43 84 Fax: +46-8-757 44 21
United States: **Ericsson Components Inc,** Richardson, TX, Tel: +1-214-997-6561 Fax: +1-214-680-1059

CIRCLE 108 FOR U.S. RESPONSE

ERICSSON

CIRCLE 109 FOR RESPONSE OUTSIDE THE U.S.

Premium GaAs at Regular Prices



If you're considering powering your MMIC-based system with conventional MESFETs, STOP! TRW can drastically increase the performance — and mileage — of your MMIC investment.

In our MMIC foundry, we're producing premium GaAs HEMT and HBT MMICs for prices comparable to what you're now paying for MESFETs. Which means you could be using high performance, low noise HEMTs or high efficiency HBTs — without paying more at the pump.

What's more, TRW GaAs MMICs include performance-enhancing backside vias and air bridges — at no extra charge.

Our GaAs prices are level because our fabrication efficiency is high. We've achieved nearly 85% process commonality among our HEMT, HBT, and MESFET technologies. So we can use one flexible fabrication line to pump out all three types of MMICs.

We also keep costs down with computer-aided manufacturing, statistical process control, and the MMIC industry's most highly automated on-wafer dc and RF probe testing techniques.

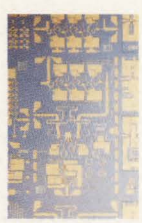
For more information on our affordable, high octane MMICs, please call: **1-800-GETMMIC.**

MMIC Foundry Services Manager
TRW Electronics & Technology Division
One Space Park
Redondo Beach, CA 90278
FAX: 310.812.7011

A sample of our current GaAs prices:

Technology	Price*
0.2 μm HEMT	$29 K
2.0 μm Emitter HBT	$29 K
0.5 μm MESFET	$29 K

*Prices are for processing six 3-inch wafers per our established PCM yield specifications. Masks, rule checks, design rules, die testing and special requirements will be quoted on request. All prices are subject to change without notice.



44 GHz HEMT Downconverter

TRW

TRW is the name and Mark of TRW Inc.
Printed in U.S.A.

CIRCLE 184 FOR U.S. RESPONSE

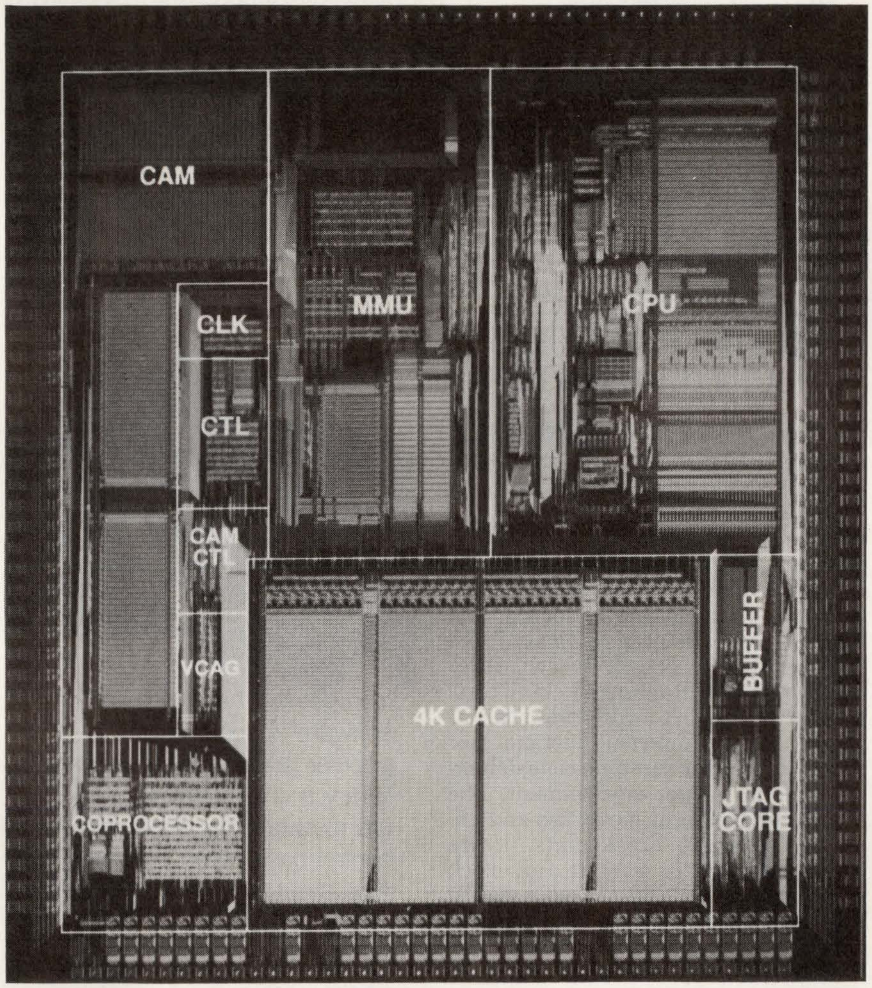
CIRCLE 185 FOR RESPONSE OUTSIDE THE U.S.

CONFIGURABLE RISC PROCESSORS SOLVE EMBEDDED NEEDS

DAVE BURSKY

An enhanced set of features over the earlier ARM2 processor and the smallest commercially available 32-bit RISC CPU core make the ARM60 and ARM600 processors very attractive for embedded control and computing applications. The enhanced CPUs from VLSI Technology are also implemented in low-power static CMOS logic rather than dynamic CMOS logic. As a result, their power drain is considerably reduced compared with that of the ARM2. Also available as part of a standard-cell library are the CPU cores of the ARM60 and 600. With those cores, system designers can create their own optimized processor.

The ARM60 processor is a direct upgrade of the ARM2, providing 32-bit rather than 26-bit addressing, and four extra internal registers. The static CMOS implementation lowers both operating and static quiescent currents to just 1.5 mA/MHz and 10 μA, respectively. When running at 20 MHz, the chip delivers a throughput of about 11 MIPS. A 100-lead package houses the ARM60. For applications that require a pin-compatible upgrade of the ARM2, the company offers the ARM61, an 84-lead version of the ARM60.



For higher performance needs, the ARM600 combines the CPU core with 4 kbytes of cache, an 8-word-deep write buffer with dual address tags, an on-chip memory-management unit (MMU), and a coprocessor interface. The on-chip MMU has been optimized for use with object-oriented programming (OOP) and has resources such as concurrent garbage collections, persistent-object store clients, and virtual-memory clients. With these features OOP software runs more efficiently since the MMU can more easily manipulate the address and permission mapping, and more easily move objects in and out of memory.

When running at 25 MHz, the ARM600 (VY86C00) has a throughput of more than 15 MIPS while dissipating less than 500 mW. The 370-by-330 mil CPU is much smaller than most other full-featured RISC processors, and, as a result, it can take on cost-sensitive applications. The chip is housed in a 160-lead plastic quad-sided flat package or a 144-lead plastic pin-grid array.

Besides the CPUs, VLSI Technology has a trio of support chips available that were used with the previous ARM2 and AMR3 processors. The VY86C110 memory controller features ROM access, DRAM refresh, and address translation. Providing both stereo and either color or monochrome video outputs, the VY86C310 includes triple 4-bit digital-to-analog converters, and delivers pixel data at up to 24 MHz.

To ease testing of either CPU, the AMR60 and 600 include IEEE 1149-compatible (JTAG) boundary-scan test ports. Thus, larger systems that incorporate the ARM processors can easily be tested.

In lots of 10,000, the VY86C060 and 061 processors sell for $26.75 and $23.40 apiece, respectively, and are sampling. The more complex VY86C600 processor sells for $65.25 apiece, also in lots of 10,000. It's also available in sample quantities. Production for both CPUs starts in the first quarter.

VLSI Technology Inc., 1109 McKay Dr., M/S 22, San Jose, CA 95131; John Haller, (408) 434-7877. **CIRCLE 461**

DEBUGGING TOOL WORKS WITH C186/C188 DEVICES

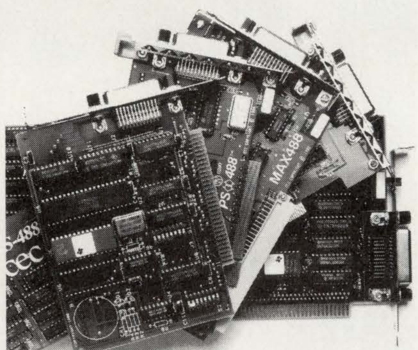
A series of low-cost, source-level, run-time debugging tools are the first products in a total development solution for embedded systems using the Intel 80C186/C188EA, XL, EB, and EC microprocessors. CodeTAP C186 consists of a target access probe, an RS-232 communications adapter, the Validate/Soft-Scope III windowed source- and assembly-level debugger, and customer support. The CodeTAP technology complements full-featured emulators. It offers designers a fully transparent window into the internal functioning of the processor for run-time code debugging in the target environment. The system offers eight hardware and unlimited software breakpoints. Users can single-step or run at full clock speed up to 20 MHz with no wait states. The system, which runs on PC hosts, supports Intel, Microsoft, and Microtec Research C compilers and provides users easy access to high-level data structures, arrays, and dynamic variables. Other products being developed include a high-performance emulator and software for solving real-time and system-integration problems. CodeTAP C186 costs $5995.

Applied Microsystems Corp., 5020 148th Ave. N.E., Redmond, WA 98073-9702; (206) 822-2000. CIRCLE 462

DUAL HEADS BOOST TESTER THROUGHPUT

Two improvements to the Polaris test system—dual test-head and parallel test capability—significantly increase system throughput. The second test head, which can be added to existing systems, ensures that there is always a device under test, without having to wait for a device handler to reload the single test head. The Polaris timing refresh mechanism maximizes this benefit by reloading all timing information into all pins simultaneously in less than 1 ms. Meanwhile, the parallel test capability uses the system's tester-per-pin architecture and software flexibility to test up to eight devices in parallel on one test head, or 16 devices on two heads. Running as an application on the host Sparcstation, the parallel test program reduces test costs by 60% to 80%. Prices for the second test head start at $465,000.

Megatest Corp., 1321 Ridder Park Dr., San Jose, CA 95131; (408) 437-9700. CIRCLE 463



12-MHZ VXI GENERATOR FEATURES FLEXIBILITY

A broad feature set adds flexibility to a 12-MHz VXI-based function/pulse generator. The Model 1378 combines a high-precision source of sine, triangle, square, and pulse functions synthesized from the VXI Clk10 reference or an external signal with an open-loop analog function generator. Other waveforms available are square complement, dc, pulse complement, and external width. Modes include continuous, triggered, gated, and burst. A variety of trigger sources can be accessed through an external BNC connector, all VXI TTLTRG lines, or by software command. Output is 10 V pk-pk into 50 Ω or 20 V pk-pk into greater than 50 kΩ. The unit can supply or sink up to 100 mA. The 2-slot, C-size, message-based module is compatible with the Standard Commands for Programmable Instruments remote programming format. The Model 1378 costs $3295 and is available 4 to 6 weeks after ordering.

Wavetek San Diego Inc., 9045 Balboa Ave., San Diego, CA 92123; (800) 874-4835. CIRCLE 464

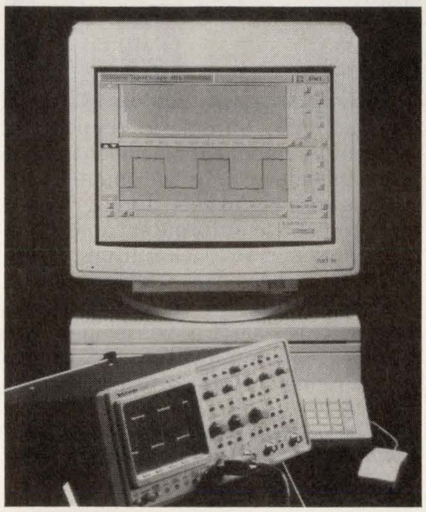
DISASSEMBLER ANALYZES BOUNDARY-SCAN DATA

Designers incorporating boundary-scan test paths on their digital boards can use the PF 8683/36 disassembler to simplify and speed up verification and debugging of the boundary-scan test vectors. The package, which includes a hardware adapter and software that runs on the PM 3580 logic analyzer family, conforms to the IEEE-1149.1 boundary-scan standard. The package stores up to 32 kbits of scan data. The disassembler compresses time-stamped data into 16-bit blocks from either the Test Data In or Test Data Out ports, as required. The data is disassembled into the familiar IEEE-1149.1 instructions. The hardware adapter lets users filter out and count repetitive states, which might otherwise fill the memory. The counter value is then displayed in the state data. Data on non-boundary-scan parts is captured synchronously with the data from the boundary-scan devices. The PF 8683/36 disassembler costs $2500.

John Fluke Manufacturing Co., P. O. Box 9090, Everett, WA 98206-9090; (206) 347-6100. CIRCLE 465

SOFTWARE CONTROLS DSOs THROUGH A MACINTOSH

The SuperScope/488 data-acquisition-and-analysis software package offers a transparent interface between Macintosh computers and digital storage oscilloscopes (DSOs). No programming is required; intuitive dialog boxes allow users to create an oscilloscope-like front panel



and configure the DSO to transfer data and measurements to the computer for display, calculation, or disk storage.

The software acts like a virtual instrument, complete with display, vertical scaling, and timebase controls that control the scope. Also, SuperScope/488 is an integrated analysis and presentation package with a built-in text editor. A library of analysis features augment those found in DSOs. Included are trigonometric and logarithmic operations and statistics, and digital-signal processing functions, such as FFTs, infinite-impulse-response filtering, and histograms. The software's initial release supports a number of popular DSOs and digitizers from Hewlett-Packard, IOtech, LeCroy, Nicolet, and Tektronix.

SuperScope/488 is available immediately at a price of $1280, which includes the SuperScope application software and the SuperScope 488 instrumentation library for DSOs.

GW Instruments Inc.*, 35 Medford St., Somerville, MA 02143-9938; (617) 625-1322.* **CIRCLE 466**

■ *JOHN NOVELLINO*

BENCHTOP TESTER OFFERS PIN PROGRAMMABILITY

A benchtop ASIC tester performs verification and characterization on ECL and CMOS devices. The ETS370 Engineering Test Station has a 25-MHz bidirectional data rate and 50-MHz clock rate. The tester can be configured with up to 512 pins in 16-pin increments. It features programmable timing generators, with 500-ps resolution and per-pin programmability of stimulus, tri-state, real-time compare, dynamic mask, and data acquisition. The ETS370 is user-interface and device-under-test board compatible with other members of the ETS family and the high-end Topaz V 110-MHz, 544-pin tester. A 256-pin system with 16 globally assignable timing generators costs less than $95,000. Included are a 33-MHz, 80486-based PC, system software, a high-speed interface, a dc parametric measurement unit, and a programmable power source.

Hilevel Technology Inc., 31 Technology Dr., Irvine, CA 92718; (714) 727-2100. **CIRCLE 467**

SOFTWARE AUTOMATES BOARD FIXTURE DESIGN

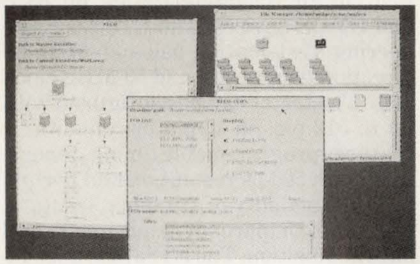
Running under a Windows environment, the Pronto Fixture software package uses CAD/CAM and Gerber data to automate the design, documentation, and fabrication of bed-of-nails test fixtures. A specialized graphical editing system allows users to accurately position test probes, even on densely loaded boards. Additional graphics help users debug the test fixture and program. The software generates files to perform automatic drilling, wiring, and receptacle installation. It also identifies surface-mount devices and other conditions that do not allow probing, and automatically corrects probe nail placement. The package minimizes expensive close-centered and top-access probe nails. The package is user programmable and can read virtually any CAD/CAM, Gerber, or tester-generated fixturing files. Pronto Fixture with one CAD link costs $4500. A universal version costs $6000.

UniSoft Corp., 94 High St., Milford, CT 06460; (203) 876-1077. **CIRCLE 468**

GRAPHICAL INTERFACE IMPROVES CONCURRENT-ENGINEERING SOFTWARE

A graphical user interface (GUI) enhances the newest release of TeamOne's TeamNet concurrent-engineering environment for distributed configuration and data management. The TeamNet software provides version control by transparently tracking product development done with any tool running on computer with Sun's Network File System (NFS). TeamNet 3.0's graphical interface, which is based on X-Windows, improves process control and conflict-resolution mechanisms for concurrent development.

Interactive file-merge capabilities allow for a visual side-by-side comparison of conflicting file changes via the new X-Windows graphical interface. The TeamNet 3.0 software also has virtual-copy abilities that perform such functions as creation of work areas and check-in of changes 2 to 10 times faster than the previous version of TeamNet



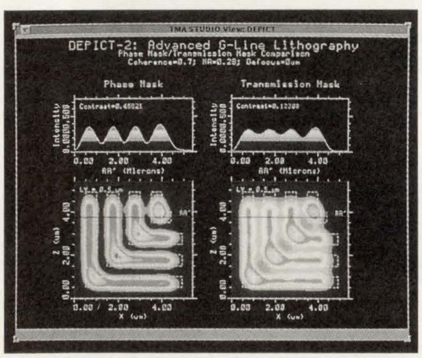
software. In addition, license-management headaches are cured with a floating-license system designed for heterogeneous environments. Organizations can license the exact amount of TeamNet software that the group needs and have it available instantly to any user on the network.

TeamNet 3.0 is shipping now. Licenses cost $3000, and support an average of two concurrent users each.

***TeamOne Systems Inc.**, 710 Lakeway Dr., Sunnyvale, CA 94086; (408) 730-3500.* **CIRCLE 469**

■ *LISA MALINIAK*

DEVICE SIMULATOR HAS 2D AERIAL IMAGING



Version 9103 of the Depict-2 software that models deposition, etching, and photolithography includes such enhancements as a 2D, aerial-imaging model and simulation of lithography using high numerical-aperature (High NA) lenses. With the 2D aerial-imaging model, Depict-2 can simulate the 2D image intensity produced by photomasks with pattern information in both lateral directions illuminated by partially coherent light. Also, users can more accurately simulate photoresist exposure with the High NA model, which accounts for oblique wave-propagation effects during optical-projection lithography over thin-film substrates of arbitrary reflectivity. Version 9103 of the Depict-2 software is available now. Pricing for the workstation-based tool starts at $28,000.

Technology Modeling Associates Inc., Third Floor, 300 Hamilton Ave., Palo Alto, CA 94301; (415) 327-6300. **CIRCLE 470**

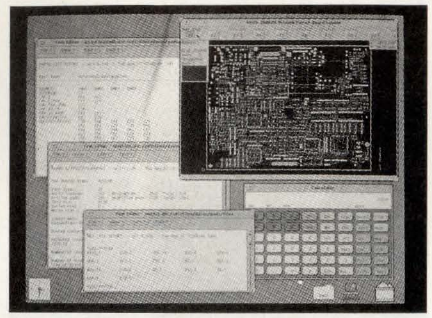
SOFTWARE EASES IC AND SYSTEM MODELING

Creating models for ICs and systems is made easier with the Mobic 6.0 logic-modeling tool from Aldec. The Mobic compiler, an expert system, accepts Boolean logic equations and produces optimized assembly-language code for execution in Aldec's Susie simulator. The code is compact, executing ten times faster than IC models written in high-level modeling languages like VHDL. The Susie-Mobic combination is aimed mainly at system-level designers. For example, engineers can create a block diagram of a system, describe each block with Boolean equations, and verify the functional behavioral interactively. The compiler comes with hard-copy examples of various IC models. Mobic 6.0 is available now for $995. Also available now, Susie 6.0 costs $1995. Both products run on PCs.

Aldec, 3525 Old Conejo Rd., Suite 111, Newbury Park, CA 91320; (805) 499-6867. **CIRCLE 471**

UNIX-BASED PCB TOOLS HAVE ENDLESS CAPACITY

Unlimited design capacity is one feature of Pads-2000/UX, a workstation version of the Pads-2000 pc-board design system that includes all the necessary tools to create a pc board and generate the engineering and manufacturing documentation. The system has a 1-



µm database, automatic copper fill, automatic component placement with a place-and-shove algorithm, support for circuits with high-speed design rules, a push-and-shove autorouter, and multiple approaches to track routing. In addition, designers can rotate pads and components in 1/10th-degree increments. Pads-2000/UX will ship on the Sun Sparcstation by the end of the year. Pricing for the software is set at $19,995.

CAD Software Inc., 119 Russell St., Suite #6, Littleton, MA 01460; (508) 486-8929. **CIRCLE 472**

TOOLKIT HELPS USERS BUILD VHDL MODELS

VHDL model developers can make their jobs easier with the Std_DevelopersKit software tool from the VHDL Consulting Group. The software is a collection of five VHDL-subroutine packages, each designed to provide a foundation for building simulator-independent, interoperable models. For instance, one package contains a methodology for building timing into VHDL models from the macrocell through the systems level, while another package has more than 300 routines for modeling digital architectures. In addition, the kit comes with a VHDL model-development guidebook with information accumulated from years of working to establish methods for model validation. The Std_DevelopersKit will run on any VHDL-1076-compliant simulator. Source-code licenses are available immediately, starting at $35,900.

VHDL Consulting Group, 974 Marcon Blvd., Suite 260, Allentown, PA 18103; (215) 266-9791. **CIRCLE 476**

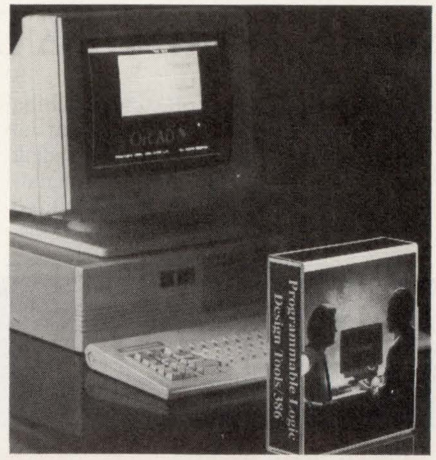
PCB PLACEMENT TOOL ENSURES ROUTABILITY

Engineers can use the Allegro Placement Evaluator to optimize their pc boards, hybrids, or mulitchip modules (MCMs) for routing and manufacturing. Placement Evaluator analyzes designs with up to 48 signal layers. A placement is tested for routability as soon as components are placed on the design. Using display grid cells, it identifies congested areas and highlights potential trouble spots where nets are likely to contribute to congestion. The software uses router parameters, feature sizes, actual spacing, and electrical constraints to display a density report as a color map that's overlaid on the routing channels. Each color on the map represents a density range. Engineers can find problem areas early in the design cycle, which speeds routing time and decreases via counts. Placement Evaluator is shipping today with the Allegro 5.0 pc-board design system, which includes an enhanced version of the Insight router. Allegro 5.0 runs on DEC, IBM, and Sun workstations, and cost between $12,500 and $50,000, depending on configuration.

Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. **CIRCLE 477**

UPGRADED PLD TOOLS SUPPORT MACH DEVICES

Programmable Logic Design Tools/386, an upgraded version of OrCAD's Release IV PLD tools, uses the native address mode of the 80386 and 80486 microprocessor to increase speed and memory capacity. Designing with many of the advanced PLD technologies, such as AMD's MACH product family, requires this increased performance. PLD Tools/386 supports certified models of the MACH110 and 210 devices as part of the more than 2400 total devices it supports. In addition, the tools have increased flexibility for use with the company's schematic-design software. For instance, the software let users create their own variations of symbols or create completely



new symbols. PLD Tools/386 is shipping now for $695. It runs on 80386- and 80486-based PCs. The price includes one year of free technical support, access to OrCAD's bulletin-board service, and a one-year subscription to the company's newsletter.

OrCAD, 3175 N.W. Aloclek Dr., Hillsboro, OR 97124-7135; (503) 690-9881. **CIRCLE 478**

3.5-IN. HARD-DISK DRIVE HOLDS 1 GBYTE

By using eight platters, Toshiba has boosted the unformatted capacity of its 3.5-in. hard-disk drive up to 1 Gbyte (867 Mbytes formatted). The MK-438FB disk drive is suited for workstations, multiuser systems, file servers, along with disk-array subsystems.

To reduce design-in time and ensure compatibility, the drive features a SCSI-II interface with Virtual SCSI, a concept developed by Toshiba. Virtual SCSI is a SCSI interface that can be downloaded from a host and that supports custom implementations.

For maximum performance and throughput, the disk drive features up to 512 kbytes of cache memory. The unit boasts 12.5-ms average seek time, a disk transfer rate of up to 25 Mbits/s, average latency of 8.33 ms, and a SCSI-bus transfer rate of 10 Mbytes/s. The drive's mean-time-between-failure (MTBF) rating is 200,000 power-on hours. The MK-438FB is available now for $2295.

***Toshiba America Information Systems Inc.**, Disk Products Div., 9740 Irvine Blvd., Irvine, CA 92718; (714) 583-3000.* **CIRCLE 474**

■ *RICHARD NASS*

VECTOR CARD WORKS WITH DECSTATION-5000

Designed for use with DECstation-5000 workstations, the SuperCard-5000 consists of a system unit, interface cable, and single-slot TurboChannel interface card. The vector-processing

subsystem is built with either one or two 40-MHz i860 processors, up to 16 Mbytes of on-board memory, and daughterboard options for direct I/O functions. Data is transferred to the subsystem across the TurboChannel or through I/O ports. The system comes with an software-specific-language (SSL) vector processing library that offers more than 225 signal-processing functions in an industry-standard format. Compilers for C and Fortran generate i860 code so that applications can be downloaded directly. The unit sits right on top of the DECstation. Priced around $20,000, depending on the configuration, the SuperCard-5000 will ship in January.

CSP Inc., 40 Linnell Circle, Billerica, MA 01821; (617) 272-6020. **CIRCLE 475**

ELECTRONIC DESIGN

Chairman and CEO: Sal F. Marino
President and COO: Daniel J. Ramella
President, Electronics Group: James D. Atherton
Advertising Sales Staff
Publisher: Paul C. Mazzacano
Hasbrouck Heights, NJ; (201) 393-6060
San Jose, CA; (408) 441-0550
National Sales Manager: Andrew M. Dellins
San Jose, CA; (408) 441-0550
General Manager, European Operations: John Allen
Four Seasons House
102B Woodstock Rd., Witney, Oxford OX8 6DY England
Phone: 0993-778-077 FAX: 44-993-778-246
Hasbrouck Heights: Judith L. Miller, Robert Zaremba
Sales Support Supervisor: Betsy Tapp
611 Route #46 West, Hasbrouck Heights, NJ 07604;
Phone: (201) 393-6060 TWX: 710-990-5071
Boston: Ric Wasley
400 Fifth Ave., Waltham, MA 02154;
Phone: (617) 890-0891 FAX: (617) 890-6131
Colorado: Lou Demeter (408) 441-0550
Chicago/Midwest: Russell Gerches
Sales Assistant: Susan Johnson
2 Illinois Center Bldg., Suite 1300
Chicago, IL 60601; (312) 861-0880
FAX: (312) 861-0874
Arizona: James Theriault (408) 441-0550
Los Angeles/Orange County/San Diego: Ian Hill
Sales Coordinator: Debi Neal
16255 Ventura Blvd., Suite 300
Encino, CA 91436; (818) 990-9000
FAX: (818) 905-1206
Pacific Northwest: Bill Giller (408) 441-0550
San Jose:
Lou Demeter (408) 441-0550
Bill Giller (408) 441-0550
James Theriault (408) 441-0550
Sales Administrator: Amber Hancock
2025 Gateway Pl., Suite 354
San Jose, CA 95110; (408) 441-0550
FAX: (408) 441-6052 or (408) 441-7336
Texas/Southeast: Bill Yarborough
12201 Merrit Dr., Suite 220, Dallas, TX 75251;
(214) 661-5576 FAX: (214) 661-5573
Direct Connection Ad & DAC Sales Representative:
Jeanie Griffin (201) 393-6080
Canada: Tony Chisholm
Action Communications
135 Spy Court, Markham, Ontario L3R 5H6
Phone: 416-477-3222 FAX: 416-477-4320
Netherlands: W.J.M. Sanders, S.I.P.A.S.
Oosterpark 6-P.O. Box 25
1483 DeRyp, Holland Phone: 02997-1303
Telex: 13039 SIPAS NL Telefax: (02997)-1500
France, Belgium, Spain: Claude Bril
IMS Paris, c/o IDG Communications France
Cedex 65, 92051 Paris la Defense—France
Phone: 33 149 047 900 FAX: 33 149 047 878
Germany, Austria, Switzerland: Friedrich Anacker
InterMedia Partners GmbH
Katernberger Strasse 247, 5600 Wuppertal 1
West Germany Phone: 02-02-711-091/92
Hong Kong: Tom Gorman, China Consultant Intl.
Guardian Hse, Ste 905
32 Oi Kwan Road, Happy Valley, Hong Kong
Phone: 852 833 2181 FAX: 852 834 5620
Israel: Igal Elan, Elan Marketing Group
22 Daphna St., Tel Aviv, Israel
Phone: 972-3-6952967 FAX: 972-3-268020
Toll Free in Israel only: 177-022-1331
Italy: Cesare Casiraghi, Casiraghi Cesare, S.A.S.
Via Cardano 81 1, 22100 Como, Italy
Phone: 39 31 536 003 FAX: 39 31 536 007
Japan: Hirokazu Morita, Japan Advertising Communications
New Gunza Buiding 3-13
Gunza 7-chome, Chuo-Ku, Tokyo 104 Japan
Phone: 011-81-3-3571-8748 FAX: 011-81-3-511-8710
Korea: Young Sang Jo, Business Communications Inc.
K.P.O. Box 1916, Midopa Building 146,
Dangju-Dong, Chongo-Ku, Seoul, Korea
Phone: 011-82-2-739-7840 FAX: 011-82-2-732-3662
Singapore, Australia, New Zealand: Omer Soker
Media Development Ltd., 17B Washington Plaza
230 Wanchai Road, Hong Kong
Phone: 834-5978 FAX: 893-9411
Taiwan: Tomung Lai, United Pacific International
No. 311 Nanking E. Rd., Sec. 3
Taipei, Taiwan R.O.C. Phone: 011-886-27-150-751
FAX: 011-886-27-169-493
United Kingdom: John Maycock
Huttons Buildings, 146 West St.
Sheffield, England S1 4ES Phone: 742-759186

ELECTRONIC DESIGN

DIRECT CONNECTION ADS

New Products/Services Presented By The Manufacturer.
To Advertise, Call JEANIE GRIFFIN At 201/393-6080

High Performance

DAC-Per-Pin™

Device Programmers

Programs virtually every device available today with a certified programmer from the leading U.S. supplier of hardware/software device tools. The Allpro starts at **$1295** and is fully upgradeable to 88 pins.

We Have the Best Products on The Market.

For more information,
call: 1-800-331-7766
or (305) 974-0967.

LOGICAL DEVICES, INC.

LOGICAL DEVICES — CIRCLE 407

SIMPLIFY BOARD LAYOUT

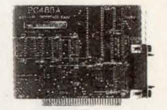
MICRO/Q 1000 ceramic decoupling capacitors share board mounting holes with IC pins to simplify board design. Now add more active devices with increased density in the same space, or design the same package on a smaller board.

Send for your free information.

ROGERS CORPORATION
2400 S. Roosevelt St.
Tempe, AZ 85282. Phone: (602) 967-0624

ROGERS CORP. — CIRCLE 408

LOW COST INTERFACE CARDS FOR PC/XT/AT



RS-485/422 Card [PC485A] $95*/125*
- Serial Async. Communication up to 4,000ft; 2 or 4 wires; NS16450 UART
- COM1-4; Max. Baud Rate 56KB; **High speed version (256KB) - $165**
- **Dual drivers/receivers;Handles 64 devices;** Compatible with most comm S/W
- DB9 or phonejack; **Sample programs included;** Optional sourcecode - **$150**

Dual-Port RS-485/422[PC485B] $175*
- Two independent channels/UARTs; 2 or 4 wire operation. Max. Baud 56KB
- Dipswitch configurable as COM1-4 (IRQ2-7); On board terminator resistor
- Optional version protected with TRANSZORBs (transient voltage supressors) and Poly Switches (auto reset electronic fuses)

Digital I/O & Counter[PCL720] $175*
- 32 Digital Input & Output channels; Output: sink 24mA/source 15mA
- Timer/ Counter (8253 chip); Selectable Clock Sources (2MHz, 1MHz, 500KHz, 250KHz) Breadboard area

IEEE-488 Card[PC488A/C] $145*/295*
- Includes **DOS Device Driver** and sample Communication program in **BASIC**
- Additional sample programs in **C, Pascal & Assembly - $ 50**
- **Selectable IRQ (1-6); DMA** channel **1** or **2;** Up to **four boards** per computer
- I/O Addresses and Control registers compatible with NI's **GPIB-PCIIA**
- PC488C card version with Built-In Bus Analyzer hardware and software

Stepper Motor Card [PCL838] $395*
- Capable of independent and simultaneous control of up to **3 stepper motors**
- **Programmable speed** from 1 to 10,000 pps; Steps per command 1 to 65535
- **DIP switch selectable** I/O port base address and wait state; 24 bit TTL I/O port
- Crystal based timing; **All control signals opto-isolated**

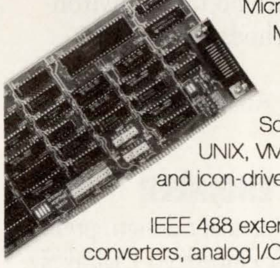
MC / VISA / AMEX — * *U.S. list price only.*

B&C MICROSYSTEMS INC.
750 N. PASTORIA AVE., SUNNYVALE, CA 94086 USA
Tel: (408) 730-5511 Fax: (408) 730-5521

B&C MICROSYSTEMS — CIRCLE 409

IEEE 488.2

Hardware for IBM PC/AT, Micro Channel, Sun, Macintosh, DEC, and NeXT.



Software for DOS, UNIX, VMS, menu-driven and icon-driven environments.

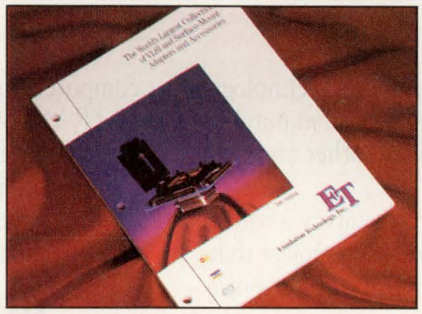
IEEE 488 extenders, analyzers, converters, analog I/O, and digital I/O.

Call for your free IEEE catalog

IOtech

IOtech, Inc. • 25971 Cannon Road
Cleveland, Ohio 44146 • (216) 439-4091

IOTECH — CIRCLE 410



Free Catalog

The World's Largest Collection of Adapters & Accessories for VLSI/Surface Mount Devices

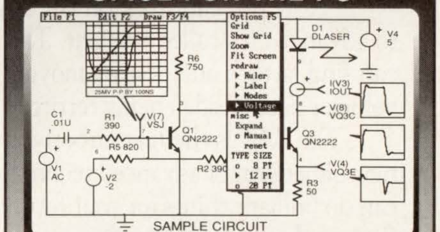
- Emulator Pods & Adapters
- Debug Tools
- Programming Adapters
- Socket Converters
- Debugging Accessories
- Prototyping Adapters
- Custom Engineering

Emulation Technology, Inc.
2344 Walsh Ave. Santa Clara, CA 95051
Phone: 408-982-0660 FAX: 408-982-0664

EMULATION TECHNOLOGY — CIRCLE 411

Analog Circuit Simulation

SPICE FOR THE PC



- Schematic Entry • SPICE Simulation
- Model Libraries • Waveform Graphics

Intusoft has it all at an Affordable Price!

INTEGRATED, EASY TO USE SIMULATION ENVIRONMENT, FEATURING: A powerful SPICE (IsSPICE) simulator performing AC, DC, Transient, Noise, Fourier, Distortion, Sensitivity, Monte Carlo, and Temperature analyses, Extensive model libraries, Schematic entry, and Waveform processing. Starting at $95 for IsSPICE, complete systems are available for $815.

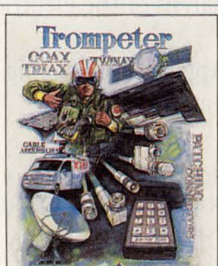
Call Or Write For Your Free Demo and Information Kit!

intusoft

P.O. Box 710 San Pedro, CA 90733-0710

Tel. 213-833-0710 — *Fax 213-833-9658*

INTUSOFT — CIRCLE 412



COAX/TWINAX/TRIAX INTERCONNECT COMPONENTS AND ACCESSORIES

Trompeter's 80-page **T18 Catalog! 1000+** interconnect components and cables. Indexes for **Broadcast, Telecom** and **Military** applications and a quick Reference Product Guide. Technical paper **"Electronic Systems Wiring and Cable".** Cable Tables expanded to 800+ cables. **Our newest products!** Quality connectors, patching products, cables and cable assemblies. **New look! Easier to use!**

Trompeter Electronics, Inc.
31186 La Baya Drive,
Westlake Village, CA 91362-4047
Phone (818) 707-2020 Fax (818) 706-1040

TROMPETER — CIRCLE 414

CUPL

PLD/FPGA Design Software

Now Featuring Mach™ Support

Get the popular CUPL development software with the newest and latest features for PLD/FPGA logic design and shorten your time to market. CUPL's powerful "C-Like" syntax allows you to develop custom logic design quickly. CUPL starts at $495.

Call your order in TODAY - Start customizing Tomorrow!

1-800-331-7766
or (305) 974-0967.

LOGICAL DEVICES, INC.

LOGICAL DEVICES — CIRCLE 413

JDR Microdevices®

2233 Samaritan Lane, San Jose, CA 95124

Prototype Cards

Decode and buffering circuitry supported. Bus pins silk-screened on both sides for easy wiring; all holes plated through.

JDR-PR2 8-Bit Card ***$29.95***
JDR-PR1 8-Bit Card w/o decode .. ***$27.95***
JDR-PR10 16-Bit Card w/decode . ***$34.95***
Part kits available

Extender Cards

EXT-8088 8-Bit for 8088 .... ***$29.95***
EXT-80286 16-Bit for 286/386 .... ***$39.95***
EXT-16 16-Bit for Microchannel ***$69.95***

Call for a free 84-pg. catalog
800-538-5000

Key Code 1527

JDR MICRODEVICES® — CIRCLE 415

INDEX OF ADVERTISERS

ADVERTISER	READER SERVICE U.S. / OUTSIDE U.S.	PAGE NUMBER
ACCEL Technologies	401	108
Actel	80, 81	50-51
	172, 173	67
Advanced Micro Devices	84, 85	2-3
Aerospace Optics	82, 83	88
AMP	86, 87	58-59
Analog Devices	88, 89	10-11
	186, 187	61
Applied Microsystems	94, 95	64-65
Arnold Magnetics	92, 93	87
Avantek	90	42, 43
B&C Microsystems	409	109
Burr-Brown	182, 183	1
Capital Equipment Corp.	96, 97	102
Cascade Microtech	174-175, 176-177	31**
Chronology Corp.	406	108
Cirrus Logic	◊	9
Coilcraft	98, 99	85
Cybernetic Micro Systems	100, 101	14
Cypress Semiconductor	◊	96
Data Delay Devices	102, 103	8
Data Translation	104, 105	72
EG&G Vactec	106, 107	106
Emulation Technology	411	109
Ericsson Components	108, 109	99
Fortron/Source	110, 111	95
Gould Test & Measurement	112,113	38-39*
	114, 115	41*
Headland Technology	116, 117	46
Hewlett-Packard Co.	118-119	29*
	178, 179	53
Illinois Capacitor	120, 121	18
International Rectifier	122, 123	22
Intusoft	412	109
IOtech	410	109
ITAC Systems	124, 125	103
JDR Microdevices	415	109
Lambda Electronics	126, 127	48A-48D*
Linear Technology	180, 181	Cover IV
Logical Devices	407	109
Mini-Circuits Laboratory, a Div. of Scientific Components Corp.	130, 131	15
	128, 129	20-21
	132, 133	82
	134, 135	Cover III
National Instruments	136, 137	25
National Semiconductor	◊	80-81
NCR Microelectronics	138, 139	6-7
NEC	140, 141	71
NKK Switches	◊	93*
Nohau	402	108
Noise Laboratory	403	108
OKI Semiconductor	◊	91*
OrCAD	142, 143	Cover II
Philips Discrete Products	91	31*
Philips Test & Measurement	◊	29**
Pico Electronics, Inc.	144, 145	45, 107
Power-One	146, 147	94*
Programmed Test Sources	148, 149	63
Rogers Corp.	408	109
Siemens Components	154, 155	26
	152, 153	34
Sipex	156, 157	77*
Spectrol	158-159, 160-161	98
T-Cubed Systems	404	108
Tektronix	164, 165	19
	162, 163	32
Texas Instruments	◊	16-17
Toshiba America	166, 167	12-13*
Trompeter Electronics	414	109
TRW	168, 169	55
TRW Electronics & Technology	184, 185	100
Vicor	170, 171	75
Yokogawa	150, 151	105**
Z-World Engineering	405	108

* Domestic Advertiser Only

** International Advertiser Only

The advertisers index is prepared as an extra service. Electronic Design does not assume any liability for omissions or errors.

SPDT switches with built-in driver

ABSORPTIVE or REFLECTIVE dc to 5GHz

Truly incredible... superfast 3nsec GaAs SPDT reflective or absorptive switches with built-in driver, available in pc plug-in or SMA connector models, from only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' latest innovative integrated components?

Check the outstanding performance of these units... high isolation, excellent return loss (even in the "off" state for absorptive models) and 3-sigma guaranteed unit-to-unit repeatability for insertion loss. These rugged devices operate over a -55° to +100°C span. Plug-in models are housed in a tiny plastic case and are available in tape-and-reel format (1500 units max, 24mm). All models are available for immediate delivery with a one-year guarantee.

finding new ways ...
setting higher standards

SPECIFICATIONS (typ)

	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	——	20	——	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) 19.95 ZYSW-2-50DR (SMA) 59.95		

Mini-Circuits

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

CIRCLE 134 FOR U.S. RESPONSE **CIRCLE 135 FOR RESPONSE OUTSIDE THE U.S.**

F141 REV.