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July 7, 1994

Special Report

Power ICs: weighing the benefits of integration pg 68

A CAHNERS PUBLICATION

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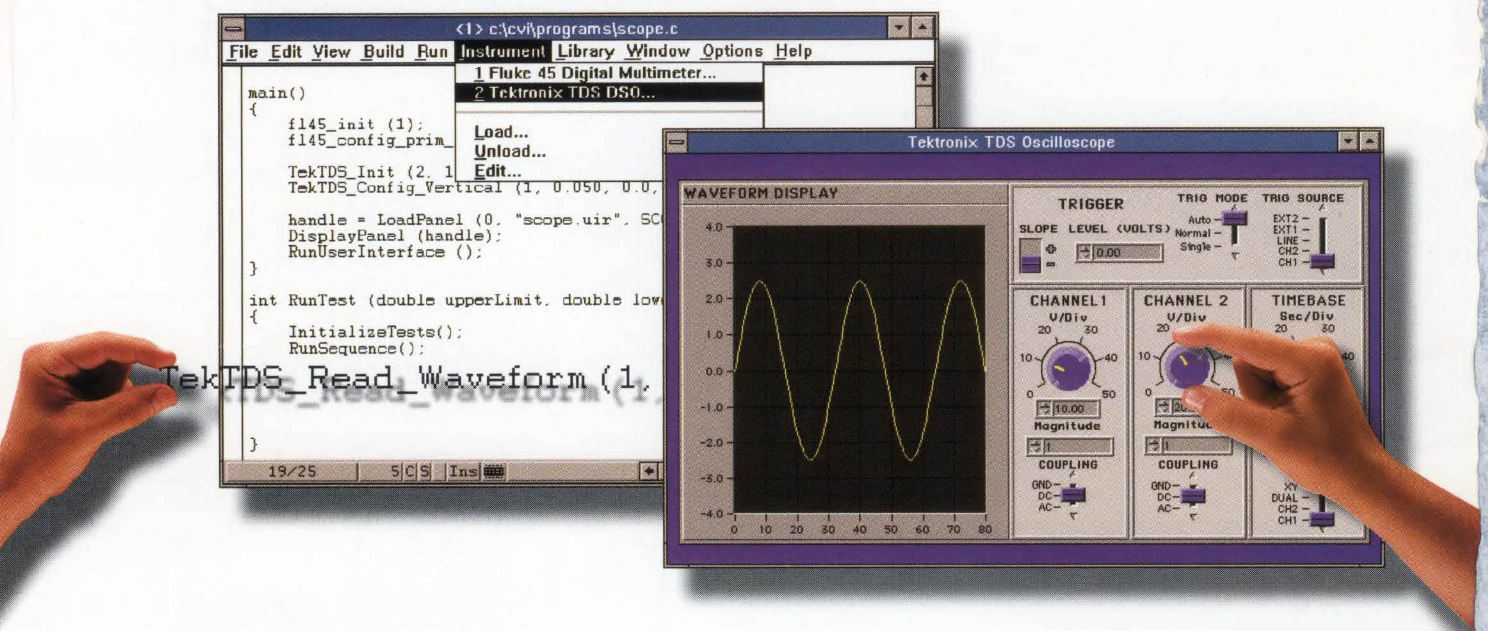

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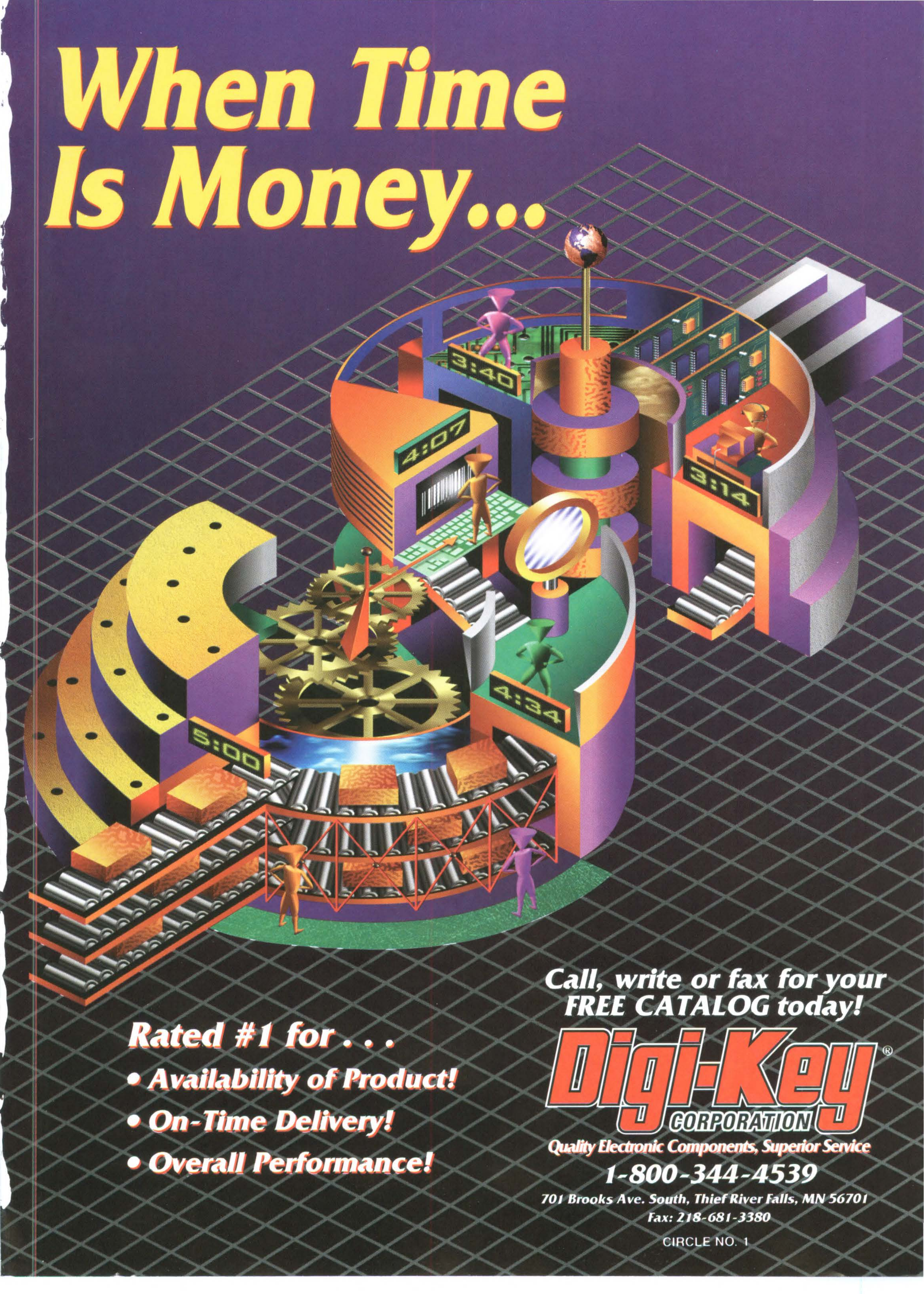
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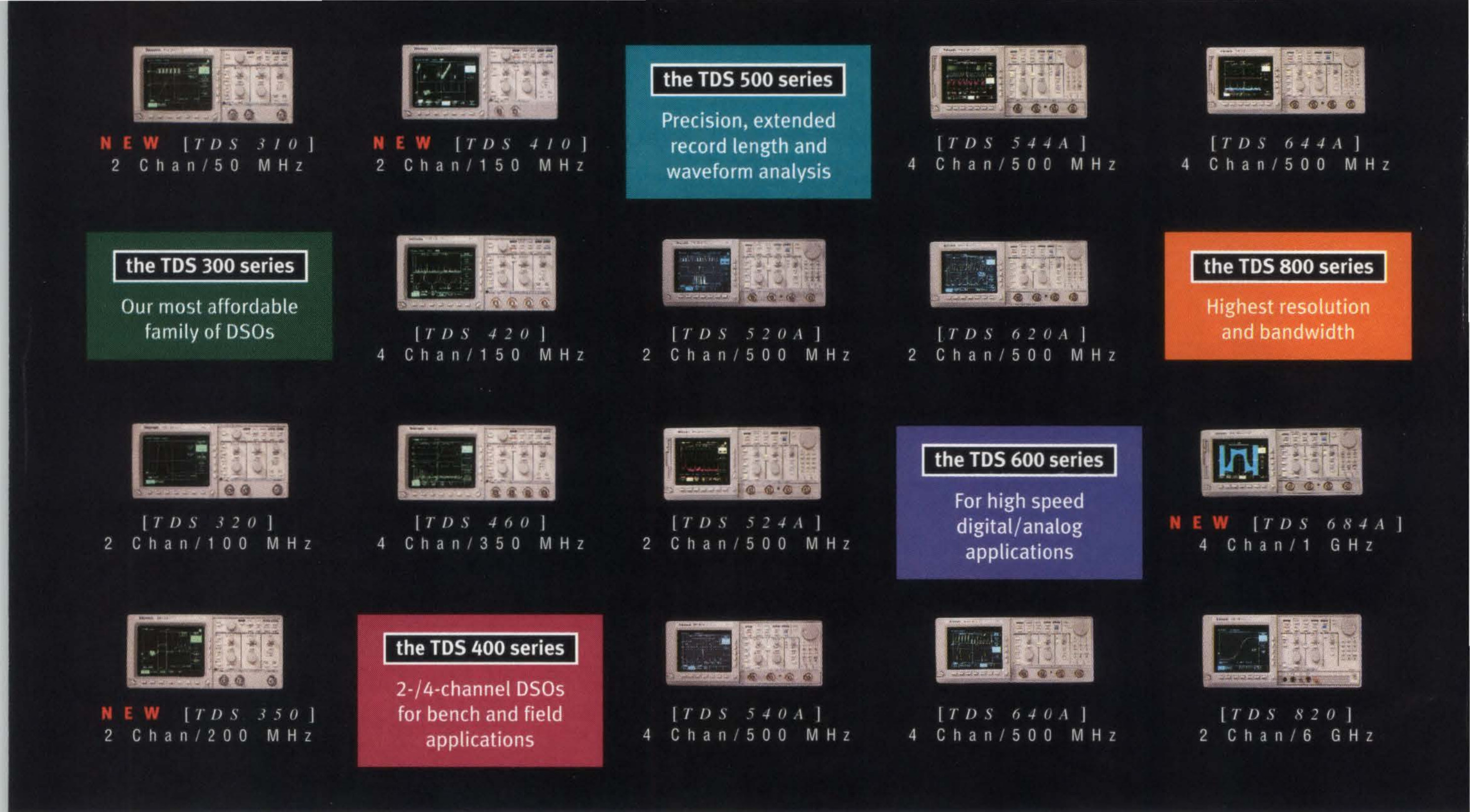

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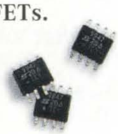

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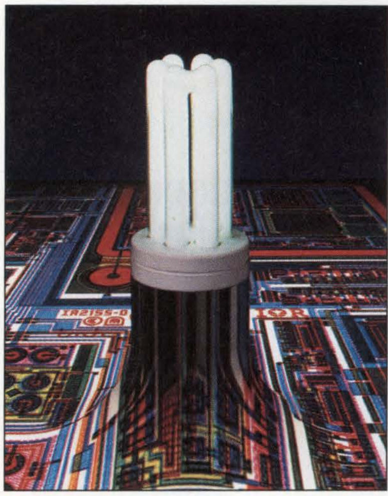

On the cover: With the advent of process technologies that can integrate virtually everything but the load itself, the capabilities of ICs for power actuation and switching seems almost limitless. See our Special Report, beginning on **pg 68.** (Photo courtesy International Rectifier; concept and computer graphics, Jon Walker, The Dartford Group)

Continued on page 7

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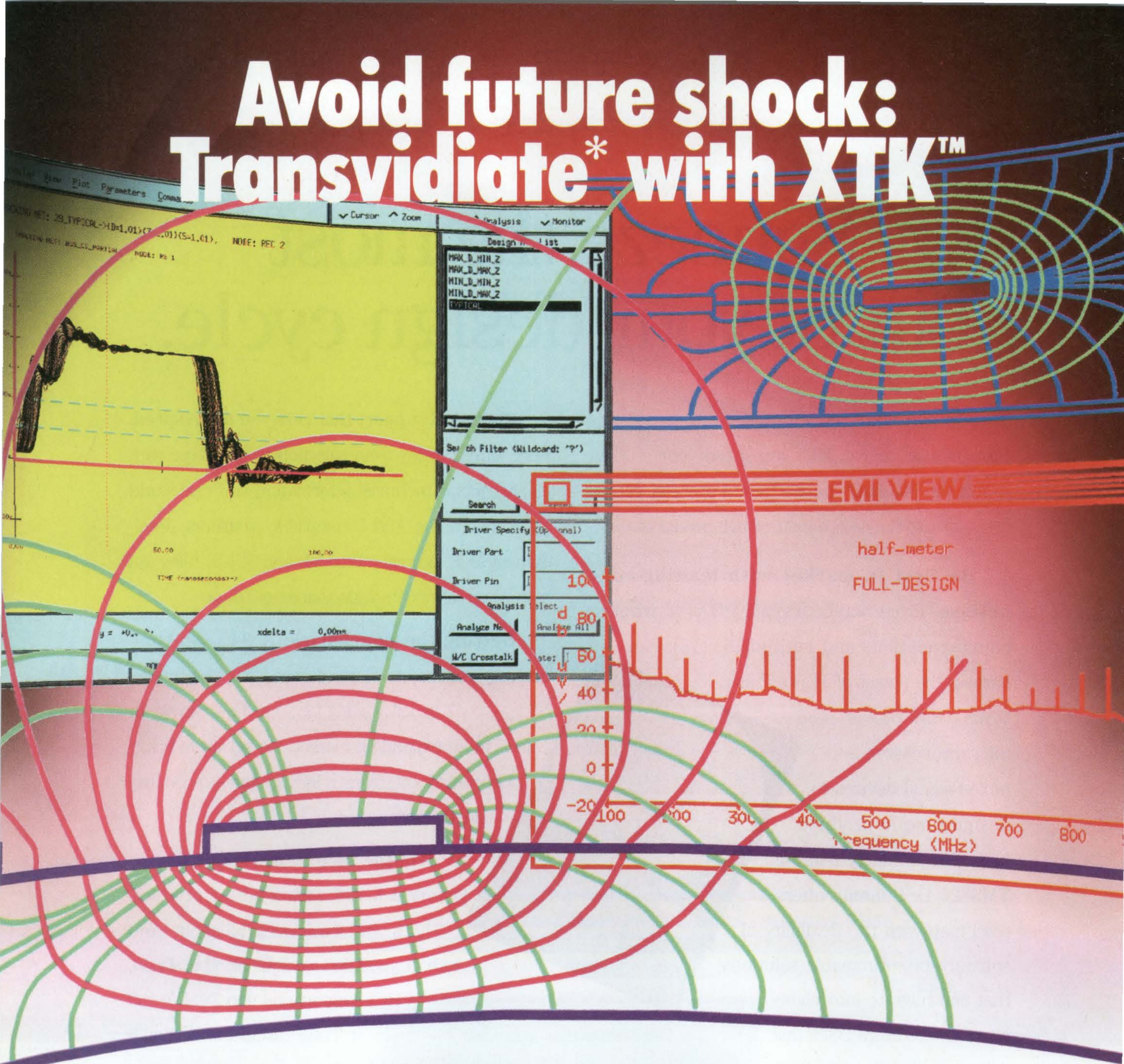

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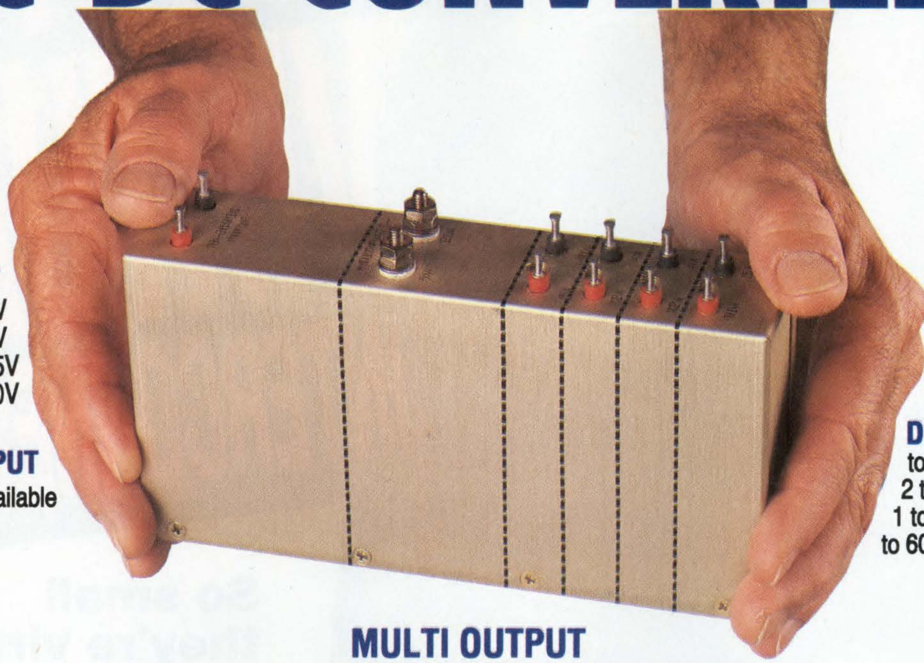

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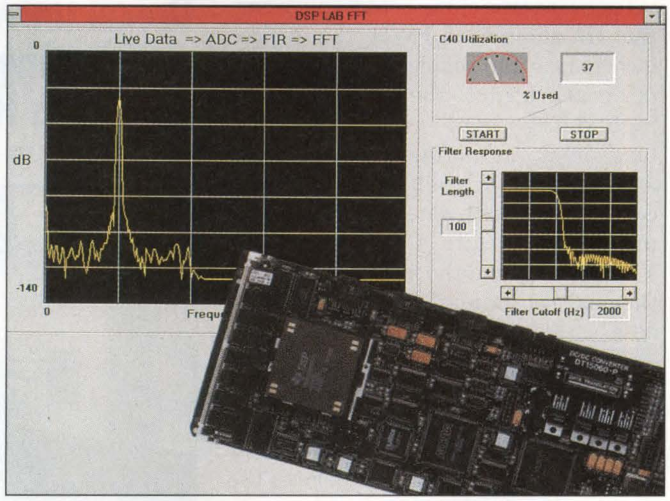
EDITED BY FRAN GRANVILLE

Data-acquisition board houses eight delta-sigma ADCs

Delta-sigma ADC technology results in admirably low noise, good immunity from aliasing, and exceptional differential linearity—traits that data-acquisition designers seek avidly. But unlike successive-approximation ADCs, which have dominated data acquisition for two decades, delta-sigma converters don't lend themselves to multiplexed operation. When you use delta-sigma ADCs, unless you can tolerate very low conversion rates, you need an ADC for each channel. On the other hand, even though their outputs correspond to voltages that appeared at their analog inputs milliseconds earlier, delta-sigma ADCs can track signals that change quite rapidly: Units are available that convert audio-bandwidth signals with 16-bit resolution.

Now, Data Translation has introduced an ISA bus board, the DT3818, that contains eight delta-sigma ADCs driven from a common clock, which you can set to over 10,000 frequencies. The ADCs and everything else on the board run under the control of a Texas Instruments (TI) TMS320C40 DSP. Each ADC can make 1000 to 52,000 16-bit conversions/sec. Inherent in the delta-sigma architecture is a "brick-wall" filter whose passband and stopband track the conversion rate. At 48,000 conversions/sec, the ADCs' –3-dB frequency is 24 kHz; noise and artifacts above 26 kHz are attenuated by at least 80 dB. The phase shift through the ADCs matches within ±0.1°.

Each channel's full-scale range is ±10V. The inputs are differential with an input impedance of 100 MΩ in parallel with 100 pF and a CMRR of more than 80 dB. Also on the board are two 16-bit delta-sigma DACs, 24 digital I/O lines, three counter timers, and channel-gain-list hardware. The DT3818 costs $4995. The DT3814, which contains two delta sigma ADCs and no DACs but is otherwise identical, costs $1995. The DSP Lab developers kit, which includes Spectron Microsystems' Spox V1.4 DSP operating system, TI's DSP development tools, diagnostic routines, and sample programs with source code, costs $2995 ($1995 without the TI compiler).



Eight delta-sigma ADCs under the control of a C40 DSP give Data Translation's DT3818 data-acquisition board, a member of the company's Fulcrum series, exceptionally low noise and excellent differential linearity.

—by Dan Strassberg

Data Translation Inc, Marlboro, MA, (508) 481-3700.

Circle No. 548

3V RS-232C IC architecture reduces supply current

To provide both low power and ±5V RS-232C performance from a 3V supply, Maxim Integrated Products' MAX3241 uses a proprietary low-dropout output stage that comprises a voltage doubler instead of a more power-hungry voltage tripler. The IC's maximum supply current of 1 mA is 20 times less than that of ICs based on voltage triplers. In addition to its lower supply current, the three drivers/five receivers serial port requires only four small, inexpensive 0.1-μF external capacitors, and the company guarantees the device to run at data rates up to 120 kbps while maintaining ±5V RS-232C output levels.

The company uses voltage doublers in its standard 5V RS-232C products, but 3V operation requires a different output stage. To use the lower power voltage doubler, designers came up with a patent-pending low-dropout stage that enables the doubler to operate from a 3V supply. The voltage drop from the output of the doubler to the output of the transmitters is only about 50 mV. The new output stage also improved signal skews, allowing operation at data rates far above the guaranteed 120-kbps data rate.

The IC has two extra outputs for the fourth and fifth receivers that are active in the shutdown mode but that draw only 1 μA of current when transmitting. You can use these extra receivers to monitor external devices, such as a modem, without forward-biasing the protection diodes in circuitry that's disconnected from V_{CC}.

The MAX3241 operates with input voltages from 3 to 5.5V and comes in 28-pin SSOPs and SOICs ($3.16). Future ICs that will use the doubling architecture include the 3232 and 3222 ($1.85 each), which have two drivers and two receivers. The 3222 also has two active receivers in shutdown. Another future device, the 3242 ($3.16), has the same number of drivers and receivers as the 3241 but requires 1-μF capacitors and has a lower maximum supply current of 500 μA.—by Anne Watson Swager

Maxim Integrated Products, Sunnyvale, CA, (408) 737-7600. **Circle No. 549**

Power switchers fit in 3-pin packages

In just 3-pin TO-220 or D-pack power-transistor packages, Power Integrations' TOPSwitch family implements all the functions for a switching power supply. For off-line flyback, forward, and boost-PFC power-supply applications, the ICs combine a high-voltage N-channel MOSFET with a voltage-mode switching power-supply controller. These generic PWM power switches offer a duty cycle proportional to the inverse of the control pin's current. In addition to PWM, the devices incorporate the following functions to drive and control the power stage: a high-voltage bias-current source, a bias-shunt regulator/error amplifier, an oscillator, a bandgap reference, a controlled turn-on gate driver, and self-protection circuits. Controlled MOSFET turn-on and the source-connected thermal tab minimize EMI and filter cost.

To fit all of these functions into one package, the company designed four patented circuits: a temperature-compensated trimmable current source for the oscillator; a circuit that derives the start-up bias current from the drain pin to avoid having to make a separate connection to the rectified line input; the use of the MOSFET's on-resistance as the sense resistor for the current-limit function; and a circuit that combines the feedback-input, compensation, and bias-supply pins.

The resultant design provides the control pin with seven functions: a bias-supply current input; an internal-supply bypass pin to provide the instantaneous peak currents for the gate drive; a feedback-signal input; compensation node; a 5.7V voltage-reference output; an externally triggered shutdown/reset pin; and an auto-restart time-capacitor node (the same capacitor as the one for compensation). The first milliamp into the control pin provides the supply current necessary to run the IC continuously. Any additional current becomes the feedback current for duty-cycle control. Between 1.2 and 2.5 mA, the duty cycle stays at the maximum value of 70% and then decreases linearly to the minimum of approximately 1.5% at 6.5 mA.

The 10-part family comprises five PWR-TOP10X devices with breakdown voltages of 350V (for 100/110V-ac off-line operation) and 2 to 10Ω $R_{DS(ON)}$. The other five PWR-TOP20X devices have breakdown voltages of 700V (for 85 to 265V-ac off-line operation) and 3 to 18Ω $R_{DS(ON)}$. Some of each group of five are available now, and the others will be available in August. Prices range from $1 (10,000) for the TOP100 to $1.92 for the TOP204.

—by Anne Watson Swager

Power Integrations, Mountain View, CA, (415) 960-3572. **Circle No. 550**

Drexel University engineering labs purchases HP equipment

First-year Drexel University engineering students learn how to measure input impedance using an oscilloscope and function generator from HP.

Hewlett-Packard Co has installed 150 of its test-and-measurement instruments in Drexel University's engineering labs. Drexel (Philadelphia) will use the equipment to teach students real-world problem-solving skills. Part of the project comes from a 5-year, $2.1-million grant from the Engineering and Science Education Directorate of the National Science Foundation. The directorate designated Drexel the lead project in a 10-institution, $4.5-million effort to improve undergraduate engineering education in the United States.

With the equipment, Drexel created 30 lab stations. Each station includes a computer, an HP 54600A digitizing oscilloscope with an FFT module, an HP 33120A function generator, an HP 34401A 6½-digit multimeter, and an HP 53131A universal counter.

—by Fran Granville

Hewlett-Packard Co, Palo Alto, CA, (800) 452-4844. **Circle No. 551**

DC/DC converter topology quiets output

Boosting single-cell voltages to 3 or 5V is one design challenge, but providing a quality, regulated output is another. To meet both, Micro Linear's ML4890 combines a high-efficiency (85%) switching boost circuit with a low-dropout linear regulator. The switching circuit raises the low input to an intermediate voltage that activates the linear regulator, which lowers and smoothes the output. The result is a converter that boosts a battery voltage as low as 0.9V to 5, 3.3, or 3V with output ripple of 2 mV p-p. A 2 to 5.5V adjustable version is also available.

Placing the low-dropout regulator on the same IC as the switching regulator allows the device to use a patent-pending feedback technique that maintains a minimal voltage across the low-dropout regulator's pass transistor. This technique produces high efficiency over a wide range of load demands and allows for maximum ripple rejection over the operational frequency of the switcher.

The ML4890 delivers up to 100 mA and holds its output to within 5% of the desired voltage. Maximum quiescent and shutdown current are 100 and 8 μA, respectively. The device requires three external components—one inductor and two capacitors. Samples are available now; production quantities will be available in September. In 8-pin SOICs, the converter costs $2.95 (1000).—by Anne Watson Swager

Micro Linear Corp, San Jose, CA, (408) 433-5200. **Circle No. 552**

ATM terminal-controller ICs handle 25 to 155 Mbps

Fujitsu Microelectronics has introduced terminal-controller ICs to suit asynchronous-transfer-mode (ATM) network-interface cards for PCs, high-end workstations, and server applications.

The ITC-25 controller IC targets 25-Mbps PC add-in cards, and the ITC-51/155 suits high-bandwidth applications using 155-Mbps synchronous-optical-network (SONET) STS-3c and synchronous-digital-hierarchy (SDH) STM-1, and 51-Mbps SONET STS-1 interfaces.

Both ICs provide as many as 4096 user-definable virtual channels, on-chip support for ATM adaptation layer 5, and 64 levels of traffic shaping covering

peak and sustainable cell rates. In addition, both ICs include interfaces to serial EEPROM for configuration storage, and to EPROM or flash memory for diskless workstations and remote downloading.

A key architectural feature of both controllers is the decoupling of bus and network activity. Local buffer memory—DRAM for the ITC-25 and SRAM for the ITC-51/155—achieves this decoupling, and each chip includes an appropriate interface.

The ITC-25 features physical-level framing compatible with IBM's 25.5-Mbps PHY specification, and a multiplexed ISA/PCMCIA-compliant 8/16-bit slave interface. The ITC-51/155 version incorporates a PCI-compliant 32-bit master/slave interface.

The company expects prices to be less than $30 (10,000) for the ITC-25 and less than $60 for the ITC-51/155. Samples are due in September.

Fujitsu has also announced plans for a range of transceiver ICs (MB580/2/3) that will interface directly with these communication controllers and with the company's network-termination controllers. Samples are due in the fourth quarter.—by Brian Kerridge

Fujitsu Microelectronics, Maidenhead, UK, (628) 76100. **Circle No. 553**

IEEE P1394 working group selects Inmos technology

The IEEE P1394 working group for a serial-bus interface standard has adopted the Inmos DS-Link bit-level encoding mechanism. (Inmos is a member of the SGS-Thomson Microelectronics group.) The serial bus supports isochronous real-time transmission of data required by multimedia applications. The DS-Link serial technology operates at 100 to 200 Mbps and allows the encoding of clock and data signals to provide a high skew tolerance and reliable asynchronous transmission. DS-Links also allows you to multiplex any number of software, or virtual, channels between any number of devices.

SGS-Thomson Microelectronics, Lincoln, MA, (617) 259-0300.

Circle No. 554

AT&T rings up first DSP chip with built-in flash

Flash memory translates into quick code updates, which is the intention behind AT&T's FlashDSP 1616. This device has replaced the DSP1616-x30's 12k-word ROM with the equivalent amount of flash memory. System-design prototyping time can be reduced considerably, because instead of waiting eight weeks for AT&T to turn the ROM version, the flash memory can be updated in seconds.

From a technology standpoint, the difficulty of integrating flash memory into a DSP chip is related to being able to obtain an access time fast enough to keep up with the DSP engine. When designing a flash-memory cell, tradeoffs can be made between high-performance reads or writes. AT&T opted to tweak the cell's design to obtain 10-nsec access times, which is adequately fast to feed the DSP.

For $20,000, AT&T supplies a hardware-development system, a demo board, software tools, and three FlashDSP 1616 devices. The software tools include the algorithms you'll need to program and erase the on-chip flash memory. To modify the flash memory, the chip's IEEE-standardized JTAG port delivers the actual commands.

—by Markus Levy

AT&T Microelectronics Customer Response Center, Allentown, PA, (800) 372-2447, fax (610) 778-4106.

Circle No. 555

Flash gets smart via voltage requirements

Using 0.6-μm technology, Intel's new flash-memory device provides system designers with flexibility to choose a variety of supply voltages. The 16-Mbit 28F016SV (SV signifies SmartVoltage technology) dynamically adapts to 5 or 12V for program and erase operations and 3.3 or 5V for reads.

Special input-voltage-sensing circuitry for both V_{CC} and V_{PP} detects the system supply and internally switches the device's voltage source. Although the 28F016SV still maintains a separate program/erase voltage pin, the device can operate from a single 5V supply. In this mode, similar to all single-supply flash devices, the 28F016SV utilizes an on-chip charge pump. The system designer has the option of providing 12V on this pin, essentially doubling program and erase performance. The separate pin provides additional merit for data security, which prevents accidental erase or program. This gives the system control for switching off the supply, either 5 or 12V, when not performing program or erase operations.

To accommodate low-power systems, the device performs 120-nsec reads at 3.3V. However, if faster reads are a priority, the 28F016SV can perform 5V reads at 70 nsec. The 56-lead TSOP chip costs $69 (10,000).—by Markus Levy

Intel Corp, Santa Clara, CA, (800) 468-8118. **Circle No. 556**

PCI bus controller chip makes debut

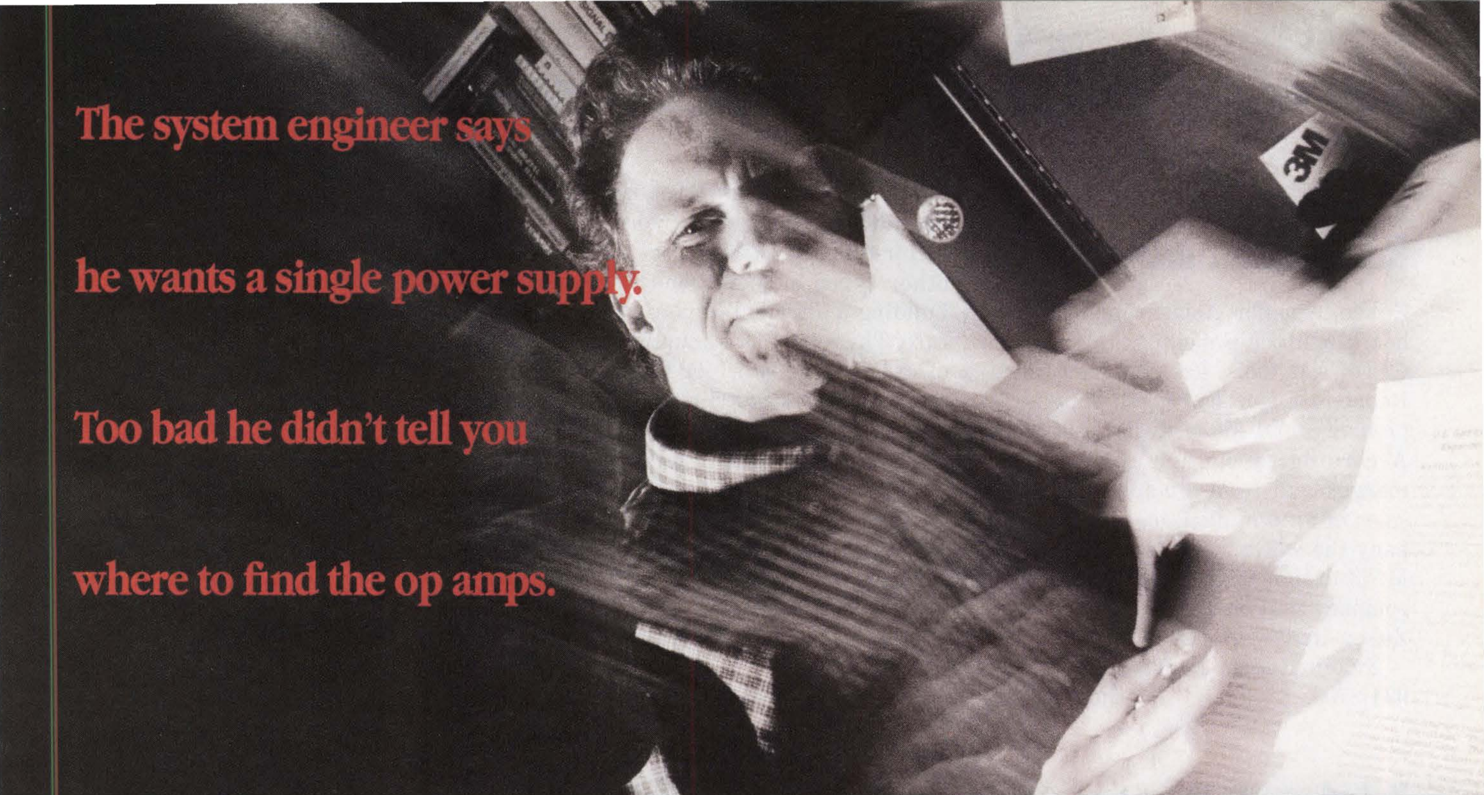
Designers trying to create add-in cards for the PCI local bus can now use a single-chip, general-purpose PCI bus interface controller. The chip, the S5933, is the first in a planned family of such devices from Applied Micro Circuits Corp. Future family members will have interface options that reduce the 160-pin package size of the parent part.

The device provides bus-master or -slave operation and passes data to and from the PCI bus in three ways. It offers a pass-through mode that allows direct access to the bus and peripheral hardware resources. Data can also pass through 32-byte FIFO buffers, allowing burst transfers. The third option allows the use of mailboxes for exchanging information such as status and control commands.

To provide a user's device ID and BIOS memory, the device offers two interfaces to nonvolatile memory. One interface is a byte-wide port for flash or ROM, and the other is a serial port for EEPROM. The chip allows the use of serial devices as large as 2048 bytes; byte-wide devices can be as large as 64 kbytes.

Samples of the S5933 will be available in July, and production is scheduled for late in the year. The part costs $39.95 (1000).—by Richard A Quinnell

Applied Micro Circuits Corp, San Diego, CA, (800) 755-2622. **Circle No. 557**



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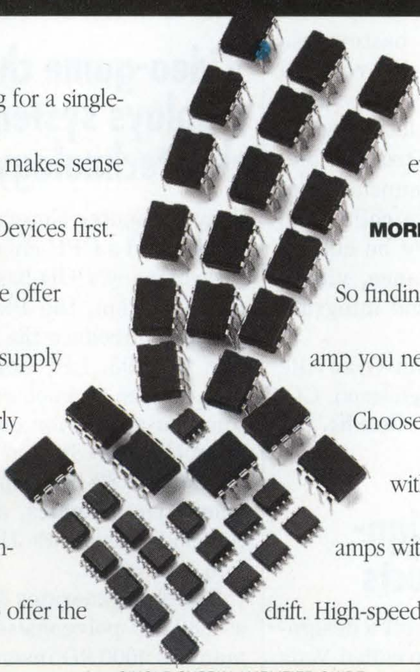

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	Single	Dual	Quad					Input	Output	(µV)	(nV/√Hz)	(mA)	(mA)	(MHz)	
OP	113	213	413		•	•	•			75	4.7	±40	1.75	3.4	Lowest noise and drift
OP	183	283		•	•	•	•			1000	10	±25	1.5	5	5 MHz from +3 to +36V
OP	90	290	490	1.6	•	•	•			150	60	+13/-7	0.015	0.02	Precision micro power
OP		291	491		•	•		•	•	700	21	±10	0.35	3	Low power R-R I/O
OP		292	492		•	•	•			800	15	±8	1.4	4.5	Low cost
OP		295	495	•	•	•	•		•	300	45	±18	0.15	0.075	Accuracy and output drive
AD	820	822		•	•	•	•		•	400	16	±30	0.8	1.9	FET Input
SSM		2135			•	•	•			1000	4.7	±40	1.75	3.5	Excellent for audio
AMP04					•	•	•			150	25	±15	0.7	0.3	Easy-to-use +5V inst. amp
AD626				•	•	•		>		250	250	15	0.23	0.1	Low cost diff. amp

CIRCLE NO. 93

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Zuken and Racal-Redac merge

Zuken, a major Asian supplier of pc-board, multichip modules (MCM), and CAD/CAM tools, has acquired Racal-Redac, a major European supplier of pc-board and MCM-design software. According to the new company, the merger will have a combined annual sales of $150 million, making the company the world leader in pc-board and MCM-design tools. Outside Japan, the company will operate under the name Zuken-Redac.—by Doug Conner

Zuken-Redac, Mahwah, NJ, (201) 934-8700. **Circle No. 558**

Teledyne Brown to demonstrate laser-diode correctors

Teledyne Brown Engineering will demonstrate its laser-diode corrector assemblies at the Optical Engineering Instrumentation show on July 24 through 29 in San Diego.

The laser-diode-beam corrector captures 85% of the diode output and converts it into a 0.7-mm-diameter circular beam with diffraction-limited performance. With these correctors, laser-diode performance exceeds that of helium neon lasers in a more compact and economical package, according to the company. In addition, laser diodes use 20 to 30 times less power than helium neon lasers. Applications for the laser diodes include point-of-sale and inventory-control scanners, laser-disk read-and-write subsystems, fiber optics, and traditional optical-metrology functions.—by Fran Granville

Teledyne Brown, Huntsville, AL, (800) 933-2091, ext 2402. **Circle No. 559**

Report analyzes power-distribution trends

The Darnell Group market-research company has published *Trends in Power Distribution*, a report quantifying market sizes and product needs for the distributed-power-architecture market. The 120-pg, $2500 publication includes 60 tables and 30 graphs. It provides 5-year growth estimates for high-density dc/dc converters, power-factor-corrected ac/dc front ends, and other types of power electronics for building a distributed-power architecture. The report also quantifies the use of central, in-shelf, per-function, and on-board power distribution.

—by Fran Granville

The Darnell Group, Norco, CA, (909) 279-6684. **Circle No. 560**

California begins trial of Racom's contactless smart cards

Three California cities—Gardena, Los Angeles, and Torrance—have begun field tests of an automatic-fare-collection system on public buses. The trials are using contactless smart cards from Racom Systems Inc. The cards, called In-Charge cards, automatically debit bus fares while a user boards a bus; the user simply waves the card in front of the fare-collection terminal.

The credit-card-sized, batteryless cards act as 2-way radios that respond to commands from the bus-fare-collection system. The test will later involve automatic vehicle location, transfer and receipt printing, voice annunciation of stops, and passenger data collection. The system will ultimately be able to monitor vehicle performance, videotape security problems, and integrate onboard electronics.

—by Fran Granville

Racom Systems Inc, Englewood, CO, (303) 771-2077. **Circle No. 561**

GenRad spin off specializes in design-automation products

GenRad Inc recently spun off a design-automation products group called Veda design automation (VEDA). The new company, based in Fareham, UK, will focus on providing high-performance VHDL simulation to the electronic-design-automation market. VEDA's strategic focus will include concentrating on the supply of VHDL design and simulation products for top-down electronics system design. VEDA will also address system behavior and ASIC and pc-board design. VEDA launched its Vital VHDL simulator in January.—by Anne Coyle

Veda Design Automation, Fareham, UK, +44 (0329) 822240. **Circle No. 562**

Natural MicroSystems forms global group

Natural MicroSystems has formed a not-for-profit entity called the Global Organization for Multi-Vendor Integration Protocol Inc (GO-MVIP). MVIP vendors include Brooktrout, Lindon, Mitel, Natural MicroSystems, Rhetorex, and Scott Instruments. Aculab Ltd sponsored the group's first conference in London on March 24. The group's goal is to provide a "single, local venue at which to meet and exchange ideas and information," according to Alan Pound of Aculab. The companies are making plans for a fourth annual developers' conference, which will take place on October 18 through 20 in Toronto. —by Fran Granville

Natural MicroSystems, Natick, MA, (508) 650-1365. **Circle No. 563**

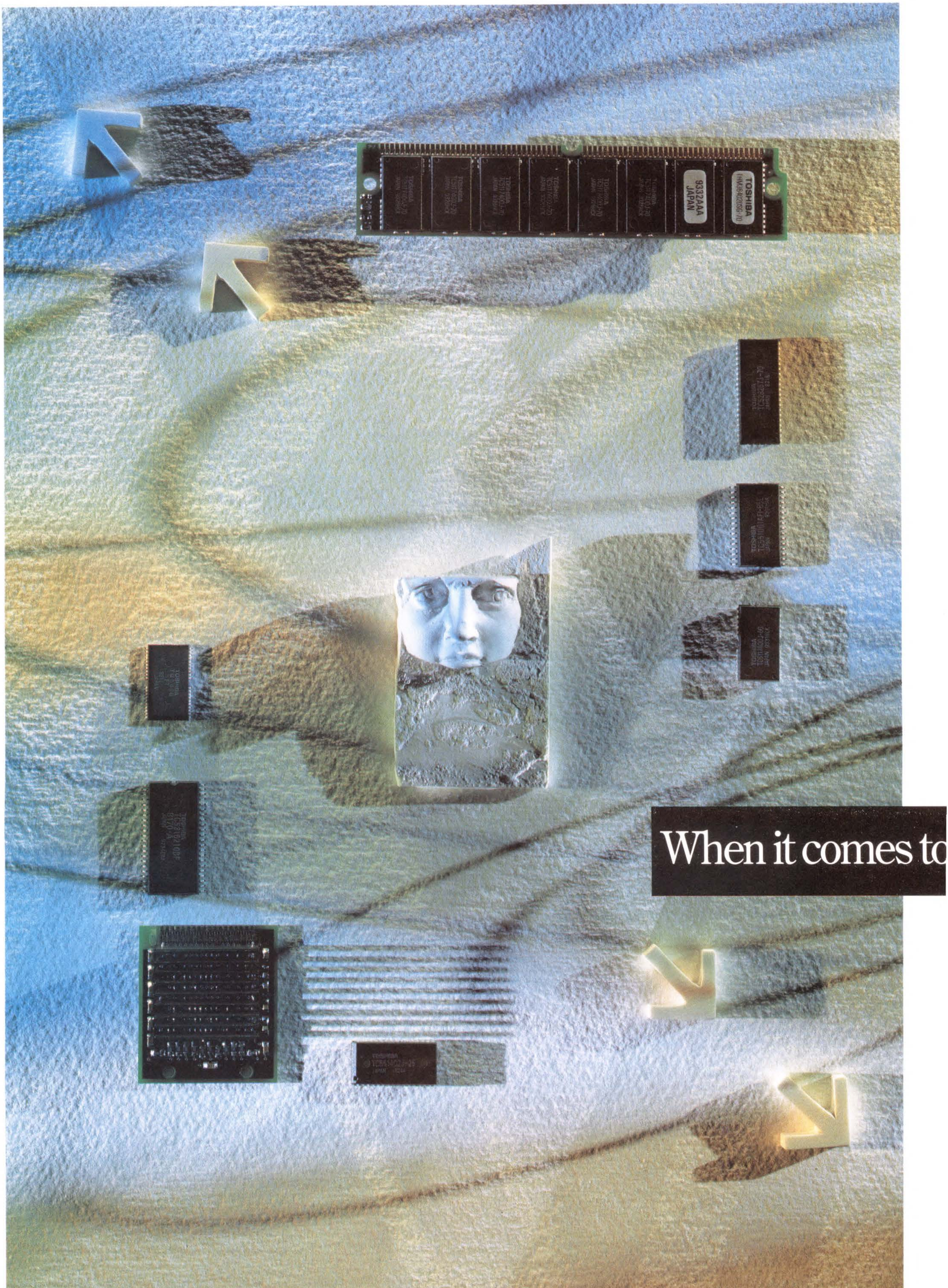
Video-game chip employs system-on-a-chip technology

Sony Computer Entertainment recently unveiled a CPU chip that will power the company's CD-based home video-game station, the PlayStation. Sony plans to introduce the PlayStation system in 1995. LSI Logic Corp, which uses 0.5-μm technology to develop systems-on-a-chip for customers, developed the PlayStation CPU. The chip contains a 32-bit Mips RISC μP, 3D geometric graphics, and high-resolution video from its JPEG decompression subsystem.

The chip generates 3D images as fast as 360,000 polygons/sec and moves as many as 4000 2D images in a field. The result is high-speed simultaneous movement of characters and high-quality backgrounds generated at 60 fields/sec, which is equivalent to TV transmission. LSI Logic has also employed system-on-chip technology to develop a laser-printer controlller and an asynchronous-transfer-mode chip.

—by John Gallant

LSI Logic Corp, Milpitas, CA, (408) 433-8000. **Circle No. 564**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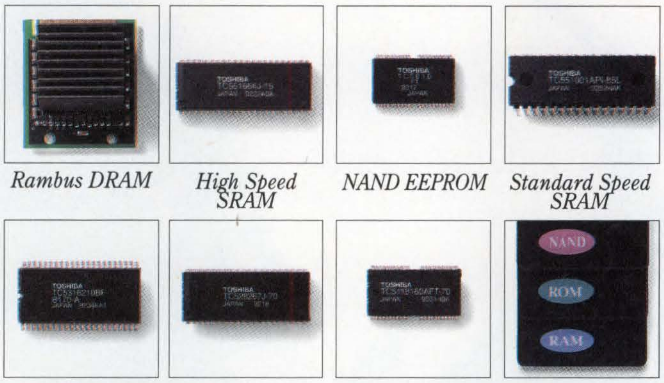

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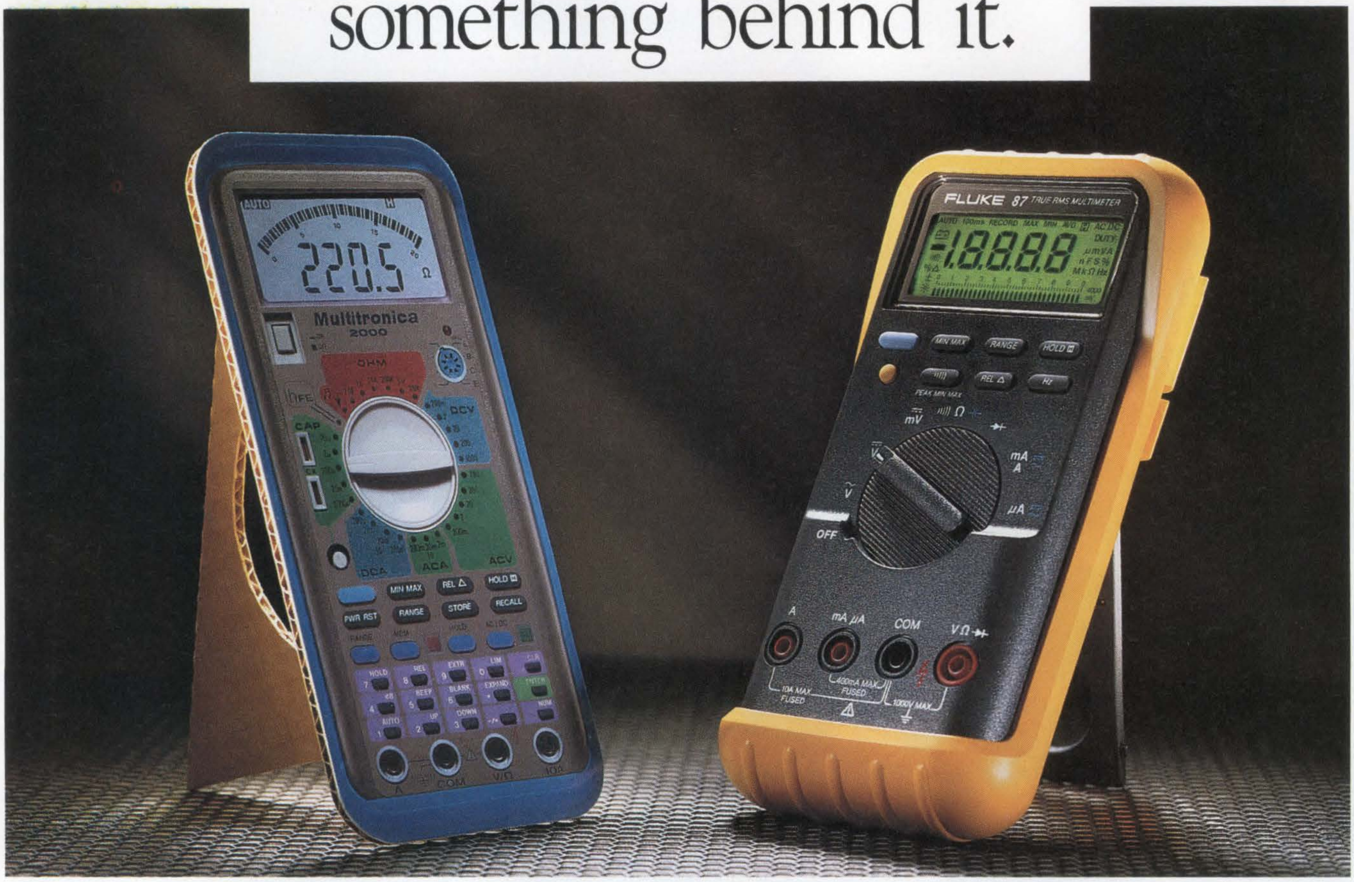

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Tools of the trade

In a letter in the May 26 issue of *EDN*, Ed Sutter wonders, "How do so many emulator vendors stay in business?" Well, as a profitable emulator vendor, I'm delighted to report that bugs are still rampant in embedded systems, and engineers will (quite rightly) buy whatever tool is needed to cure their products' ills as efficiently as possible.

No tool is really essential. I can pound in nails with the heel of my shoe if I choose not to invest in a hammer. Watch engineers working in a lab. How often do you see one remove insulation with his teeth because strippers aren't close at hand? Even Sutter's logic analyzer is not really needed for debugging embedded systems—why not use a scope and tediously move the probe across the data bus to determine what the program is doing?

Emulators offer some critical debugging assets that no other tool provides. Some are obvious, like extensive breakpoint capability—stop the code when exactly this event occurs. Real-time trace is much like the display on Sutter's logic analyzer, but emulators are typically far more closely coupled to a source-level debugger, giving a perfect correlation between source code and what's in the trace buffer. Emulation memory, tied so tightly to the source debugger, makes downloading code a breeze while preserving the debugging links to the source.

While all emulator vendors like to tout how "nonintrusive" their products are, intrusive emulation is a critical feature. Suppose the code doesn't work. Patch it! What's the value of that I/O port when we hit the breakpoint? Read it! Will altering the queue pointers fix the circular buffer code? Try it! Emulators are the only tools that combine nonintrusive program execution with the ability to make changes at will.

One of my personal frustrations is that emulators are more and more regarded as software-development tools only, when in fact there is no easier way to fix a prototype computer board than with an ICE. If the board doesn't work, plug in an emulator and ask it to display ROM repeatedly. Then use a scope to check for chip selects and the like. I/O broken? Use the ICE to read ports and construct scope loops. Is the A/D linear? Without writing a single line of code, use the ICE to read and display the converter as you ramp its input.

A logic analyzer, scope, or any other tool only lets you watch the system crash and maybe (perhaps if you burn enough incense...if the gods are smiling...if the you paid your taxes) figure out why the system is dead. An emulator lets you run controlled, repeating tests to quickly isolate problems to a specific component.

Yes, we emulator vendors benefit from our customers' mistakes and miseries. It's a synergistic relationship, though: Our tools reduce their angst and ultimately increase both our profits and their profits.

Jack Ganssle, President
Softaid
Columbia, MD

One more

I want to congratulate you on the March 3 *EDN* article "User-interface prototypes help you design products real people can operate" (pg 51). It was quite interesting and educational at the same time...only one thing was missing—us. Virtual Prototypes Inc is a leading supplier of software tools for developing real-time graphical human/machine interfaces (HMIs). VPI's tools are designed to make the development and deployment of graphical HMIs a straightforward task. Our technology, called "virtual prototyping," addresses three basic HMI design needs: rapid prototyping, automatic code generation and retargeting for operation and embedded systems, and real-time simulation and training.

Claire Champeau
Marketing and Communications Coordinator
Virtual Prototyping Inc
Montreal, Quebec, Canada

Sound off

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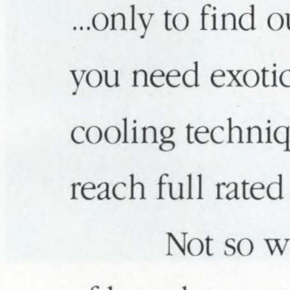

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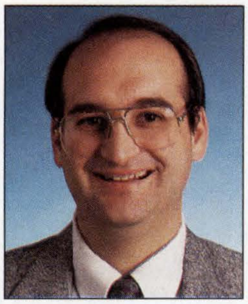

EDN's readers often tell me about problems they've had with suppliers. Sometimes EDN can help, and sometimes we can't. Recently, Creigh Shank, a principal consultant at Cox and Associates, contacted me regarding problems his company was experiencing with a PC component vendor over a 3-month period. It seems that several of the motherboards and graphics controllers supplied by this vendor had failed, and Shank was getting nowhere fast with his appeals to the vendor for help. Shank's solution was to send 67 letters to various electronics and computer magazines explaining his problems in detail. He also sent a copy of his letter to the vendor along with a list of the magazines he'd contacted.

Shank's gambit worked. Apparently, the vendor is now paying a lot of attention to the problems and is solving them to Shank's "full satisfaction," as he stated in a follow-up letter.

This story, one that repeats often in our industry, is a prime example of how you can be effective in achieving your personal and corporate goals. You do that simply by taking matters into your own hands and acting.

All relationships have problems. You should expect them and not be put off by them. When problems do occur, the real test of the relationship is what you do in response to the problem. If the problems are sufficiently large, you may choose to terminate the relationship. However, that choice discards the investment you've made in the relationship, which may be very large indeed.

You may try to work the problems out. This was Shank's first move. In his case, this approach seemed not to work, though many times it does.

Finally, Shank used what I call the "two-by-four approach." When you can't get the other party's attention, you must sometimes resort to using the figurative equivalent of a big piece of wood (a two-by-four) to whack the other person on the head and get his or her attention. Note that I'm not advocating physical violence here, nor am I advocating overreacting. I am advocating assertive action to solve problems.

Take a look at the problems plaguing you at the moment. Write them down. Then write down some actions you can take to creatively and assertively attack each of these problems. Griping and whining don't solve problems. Actions do.

Steven H Leibson
Editor-in-Chief

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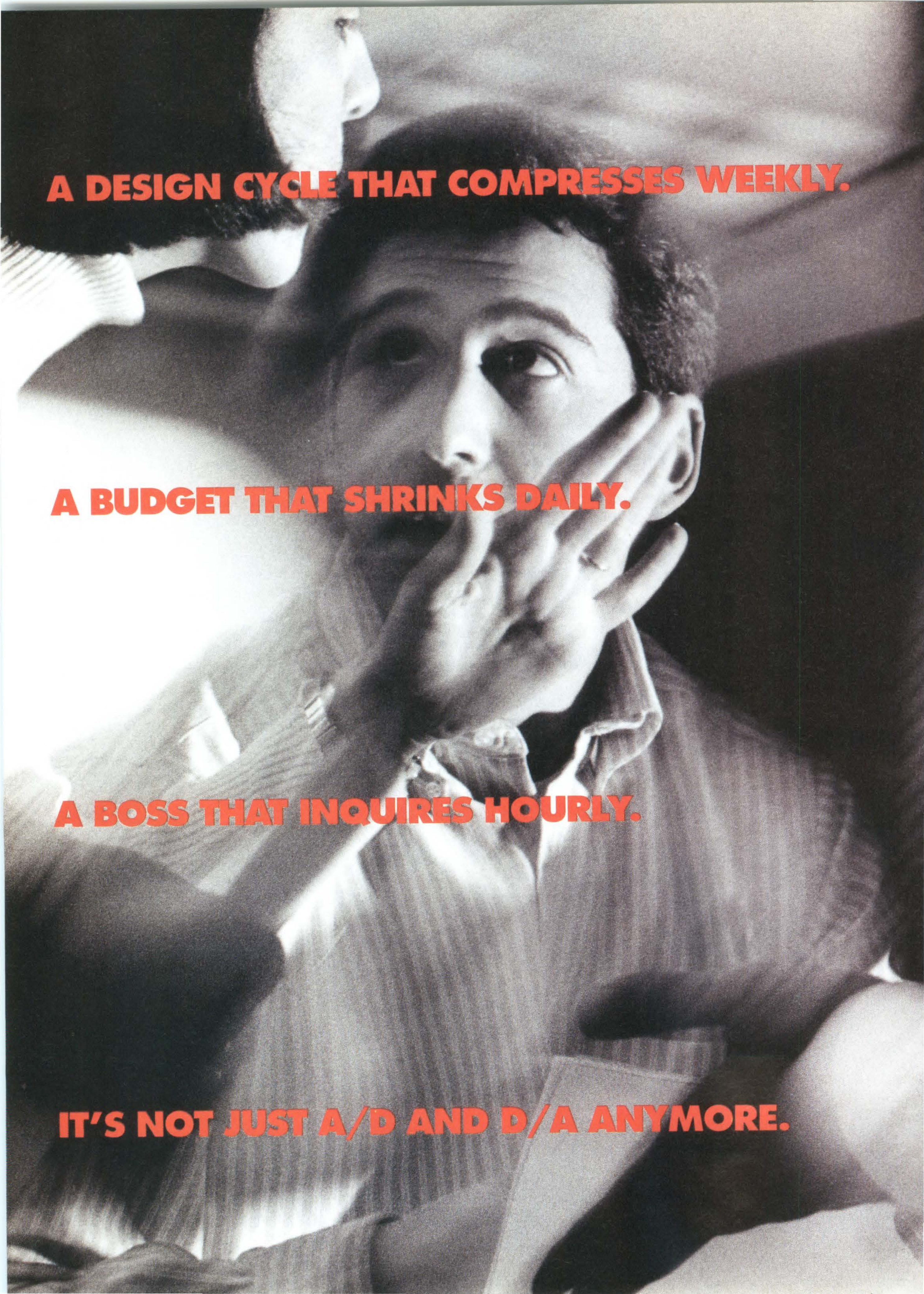
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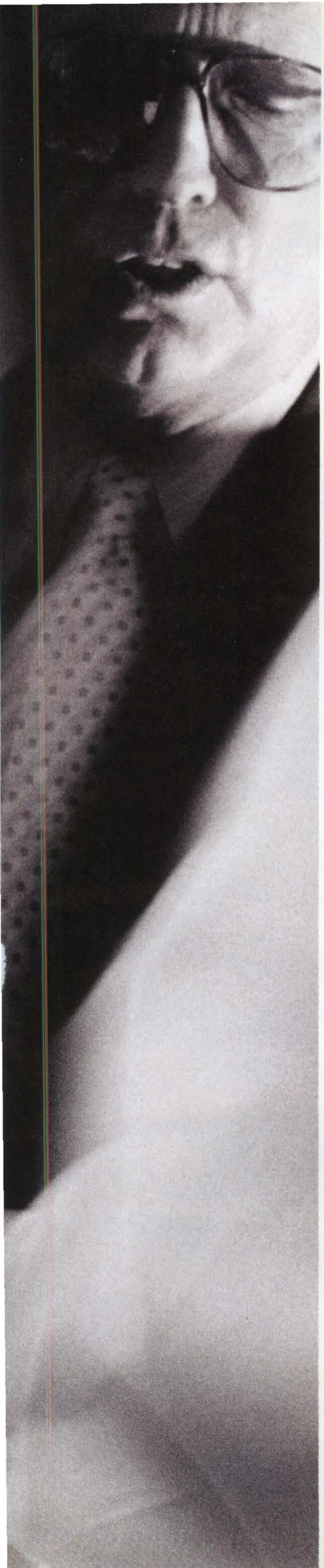

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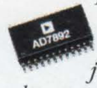

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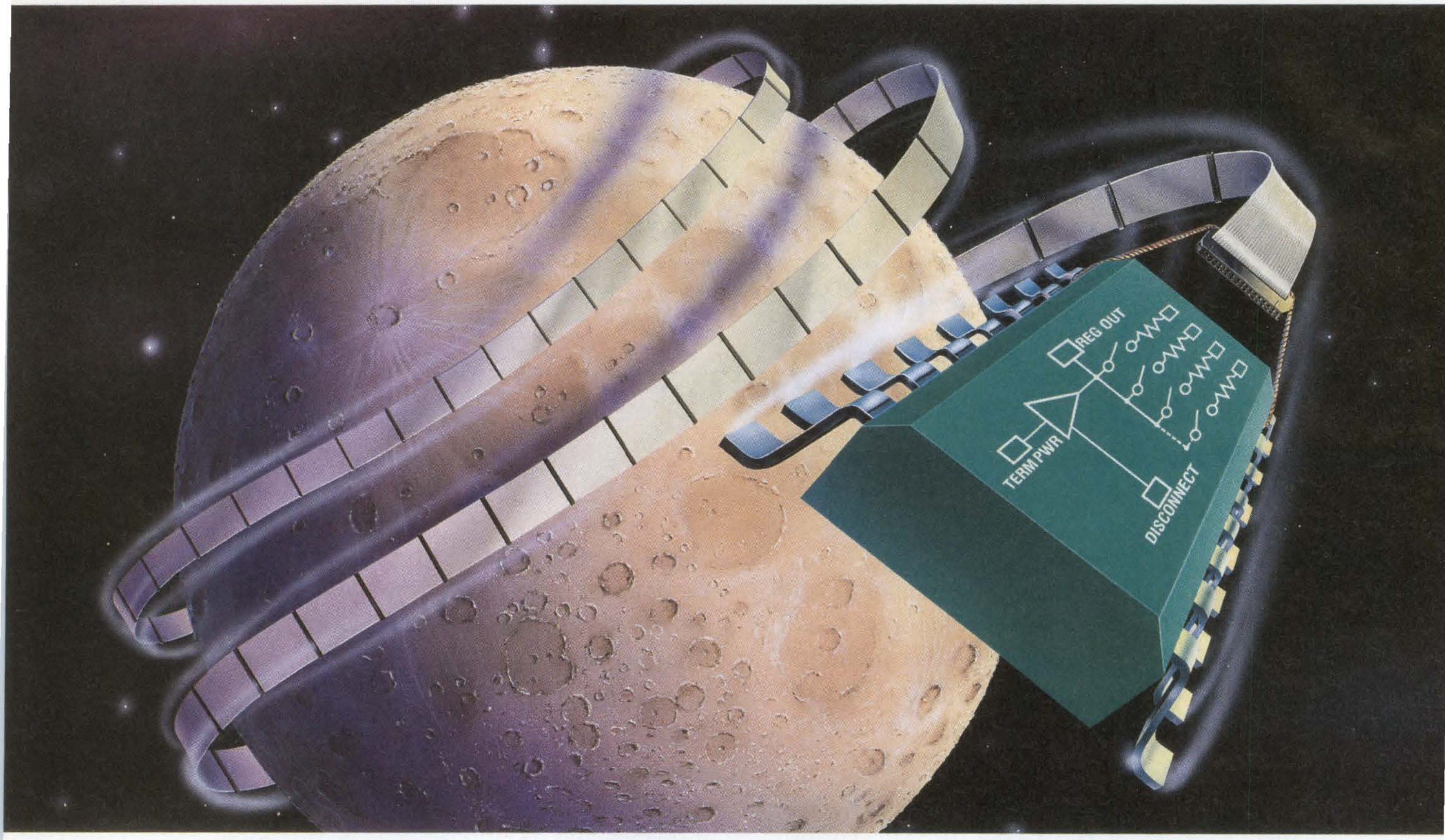

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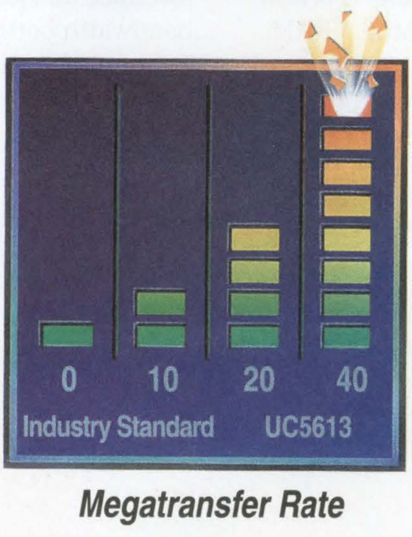

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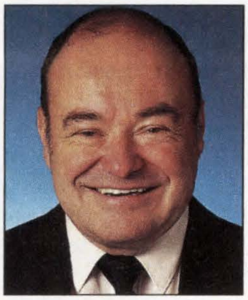
Low-power ASICs save board space and time to market

JOHN GALLANT, Technical Editor



The relentless demand for low power has driven vendors to offer ASICs with reduced power consumption. Some of these devices have such large densities that even a full-blown version must offer thermal management.

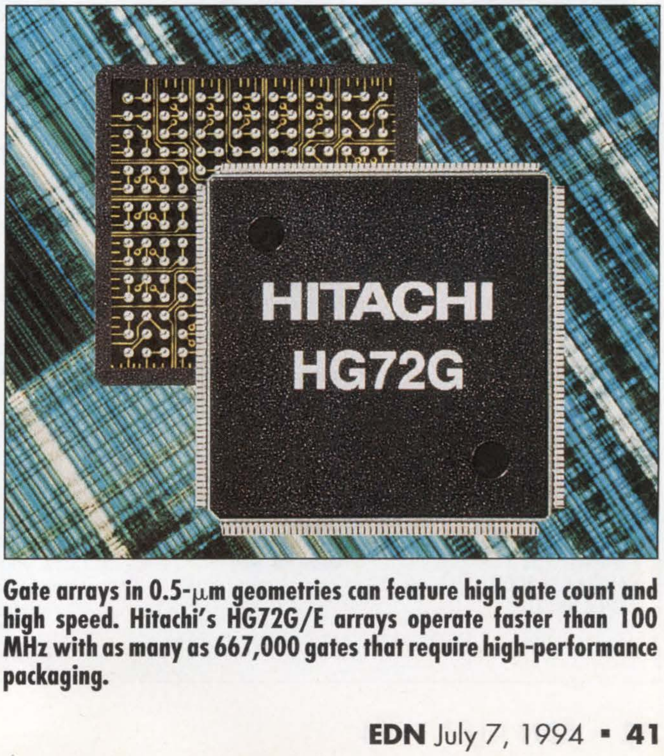
It seems like everyone is demanding low-power consumption from their ICs these days. The reasons are manifold. Battery-operated devices, such as laptop and palmtop computers and personal digital assistants, require low current drain to increase time between battery charges. Cellular and cordless phones also demand power-conserving features to preserve battery life.

In addition, ASIC density, which formerly ranged from 25,000 to 50,000 gate equivalents, has grown in recent years to 500,000 to 1 million gate equivalents. The high gate counts can stress an ASIC's thermal properties. Therefore, thermal management has become another critical reason for demanding low power consumption from an ASIC. Dense designs using high clock frequencies place severe demands on the thermal-dissipation capabilities of a package.

The most widely used method for achieving low power from an ASIC is to lower the supply voltage from 5 to 3.3V. All things being equal, the voltage reduction can achieve approximately 60% in power savings. The lower voltage, however, means an approximately 50% lower operating speed. The lower speeds help reduce EMI because the lower voltage produces longer rise and fall times for I/O logic levels than those produced in higher-voltage devices. In addition, an ASIC operating from a 3V supply can use a much less expensive package for thermal considerations.

Three flavors of ASIC

Low-voltage ASICs come in three varieties: gate arrays, embedded gate arrays, and standard cells. Gate arrays employ a sea-of-gates architecture in which the gates are prediffused to achieve turnaround in a few weeks for large quantities. Standard cells employ gates that are not prediffused, which allows them to include large macrocells, such as RAM, ROM, and μP cells. Because standard cells require more masking procedures to manufacture, their turnarounds are longer than those of standard gate arrays. An embedded array, a compromise between a gate array and a standard cell, allows embedding of some large



Gate arrays in 0.5-μm geometries can feature high gate count and high speed. Hitachi's HG72G/E arrays operate faster than 100 MHz with as many as 667,000 gates that require high-performance packaging.

LOW-POWER ASICs

macrocells into a standard gate array.

Some vendors, such as American Microsystems Inc (AMI) and NCR, offer a 3V characterization for their basic 5V ASIC families. AMI's base gate arrays, the AMI8GxS family, use a 0.8-μm CMOS process employing a sea-of-gates architecture. The arrays use double or triple metallization and are available in 5 or 3V. NCR offers the VS500 standard-cell family, which employs a 0.75-μm technology. The family allows 5 and 3.3V I/O and core cells for mixed-voltage applications. The family has more than 700 digital core cells.

How to estimate power

How do you estimate the power consumption of an ASIC? Many vendors quote a power factor for a single gate's power dissipation. For CMOS processes, the power factor depends on the operating frequency, so vendors measure it in microwatts per megahertz per gate (μW/MHz/gate). In bipolar processes, the power dissipation is constant with frequency, so the vendors measure it the power factor in microwatts per gate (μW/gate). The power factor is different for core cells and I/O buffers, so you must take a weighted average of the total power factors a data sheet provides to achieve an average value.

If you employ CMOS devices, you can break your design into blocks of logic based on switching frequency once you achieve a weighted average for the power factor. You can calculate the dynamic power consumption by multiplying each block of gates or cells by the power factor and then by the operating frequency. You then sum the power for each block to achieve the total power consumption.

Motorola's H4CPLUS 3V metal CMOS gate arrays suit mixed 3 and 5V applications. A unique interface design permits chip-to-chip communications at 200 MHz with low power dissipation.

Unfortunately, this method gives you only a ballpark figure because actual power consumption depends on other factors, such as the output pads' load capacitance and frequency. You must also weigh a device's static power consumption. To achieve a more accurate estimate of power consumption, you must develop a netlist for your design and let a simulator give you a power estimate based on test vectors. Tools from electronic-design-automation vendors, such as Cadence, Cascade, Mentor Graphics, and Synopsys, can estimate power consumption. If the test vectors are complete, the power estimates are usually conservative; actual prototypes should yield lower power levels.

Mixed-voltage I/O is popular

Most low-voltage ASICs have mixed-voltage I/O pads and fixed 3 or 5V cores. Mixed-voltage I/Os allow the device to communicate with inexpensive 5V devices, such as DRAMs. Motorola's 0.6-μm H4CPlus series of gate arrays features current-mode transceiver-logic buffers, which provide a self-terminating I/O method and CMOS chip-to-chip interface speeds exceeding 200 MHz. The arrays have dual V_{DD} rails to power the

MANUFACTURERS OF LOW-POWER ASICs

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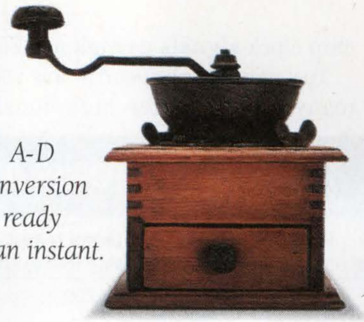

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LOW-POWER ASICs

output buffers for 3.3 or 5V or mixed-voltage levels. You can embed analog PLLs in two corners of the die for on-chip clock signals as high as 125 MHz.

To achieve high speed at low voltages, many vendors offer high-density 3V families with 0.5-μm processes. Hitachi, IBM, LSI, NEC, Toshiba, and VLSI all provide ASICs in 0.5-μm

TABLE 1—LOW-POWER ASICs

Company	Model	Maximum usable gates	Power dissipation (μW/MHz/gate)	Internal gate delay (psec)	Supply voltage (V)	Price	Features
American Microsystems Inc Circle No. 307	AM18Gx (0.8 μm)	432,180 and 324,526	3.2 at 5V	200	2.7 to 5.5	Not specified	2- and 3-level metallization; automatic test-pattern generation, includes scan macros; 3 to 5 and 5 to 3V level shifters; selectable 1- to 16-mA output-current drivers, synchronous single-port RAMs to 1k×32 bits; maximum of 528 bond pads
AT&T Microelectronics Circle No. 326	HL400C (0.5 μm)	500,000	2	330	2.7 to 3.6	Not specified	Standard cell library has 400 kbits of RAM, 80C196 μC, UART, and DMA controller; supports 5V, LVTTL, GTL, and PECL I/O ports; system clock speeds greater than 120 MHz; IEEE 1149.1 boundary-scan macrocell; 3-layer metallization
Fujitsu Circle No. 310	CG51, CE51 (0.5 μm)	490,000	1.2	210	3.3	NRE starts at $65,000	3-layer metallization; maximum, system clock speed= 100 MHz; automatic test-pattern generation, JTAG IEEE 1149.1 boundary scan; internal PLL clocks and embedded RAM or ROM
Hitachi Circle No. 311	HG72G/E (0.5 μm)	39,000 to 500,000	1.2	200	3.3	NRE starts at $70,000	System clock speed >100 MHz; ball-grid array with 672 I/O pins; on-chip PLL clocks and maximum metallized memory of 256 kbits
IBM Microelectronics Circle No. 312	CMOS 5L	1.2 million	1 to 1.5	Not specified	3.3	$200,000 NRE (includes place and route)	4-layer metallization; >100 MHz operation; logic-sensitive scan design generates test vectors; 625-pin ball-grid array; 25 embedded arrays, including RAM
LSI Logic Circle No. 313	LCB500K (0.5 μm)	1.5 million	Not specified	065 at 3.3V	3.3 and 2.4	NRE starts at $30,000	System clock speeds >200 MHz; cell- and gate-array-based; 4-layer metallization; 160 kbits of RAM and 350 cells; PECL, GTL, and PCI interfaces
Mitsubishi Circle No. 327	0.5-μm CMOS ASIC	1 million	1.3	170	3.3	Not specified	2- or 3-layer metallization; programmable-current output buffers; 256-kbit RAM with 3.7-nsec access time
Motorola Circle No. 315	H4CPLUS (0.6 μm)	13,000 to 295,000	3 at 5V, 1 at 3V	28 at 5V, 42 at 3V	3.3 and 5	NRE ranges from $35,000 to $200,000	Current-mode logic-transceiver logic buffers permit CMOS chip-to-chip interfaces >200 MHz; customer-defined array allows large diffused blocks, such as RAMs; 3-layer metallization
NCR Corp Circle No. 316	VS500 (0.75 μm)	200,000 (180 core-cell functions)	3.55 at 5V, 1.45 at 3.3V	280	3 and 5	Not specified	Global clock tree synthesis to minimize skew; output slew-rate control; IEEE 1149.1 JTAG boundary-scan functions, including test-access-port controller; power simulation provides early identification of thermal characteristics

Table continued on pg 46

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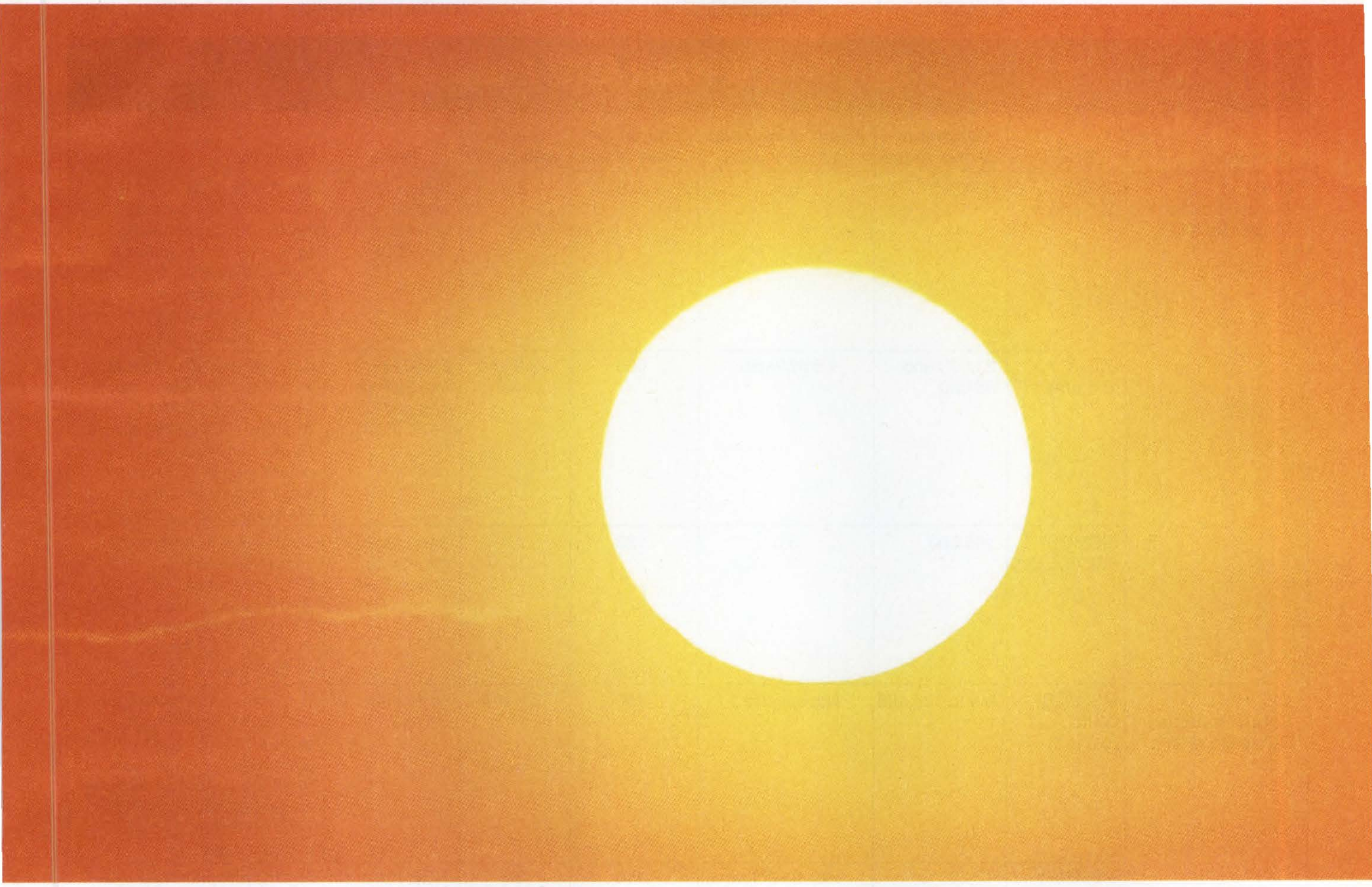

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geometries. LSI's LCB500K cell-based technology can achieve I/O frequencies from 100 to 500 MHz having as many as 1.5 million gates. The large densities require packages with large pin counts and many power and ground pins to prevent ground bounce when many outputs switch simultaneously.

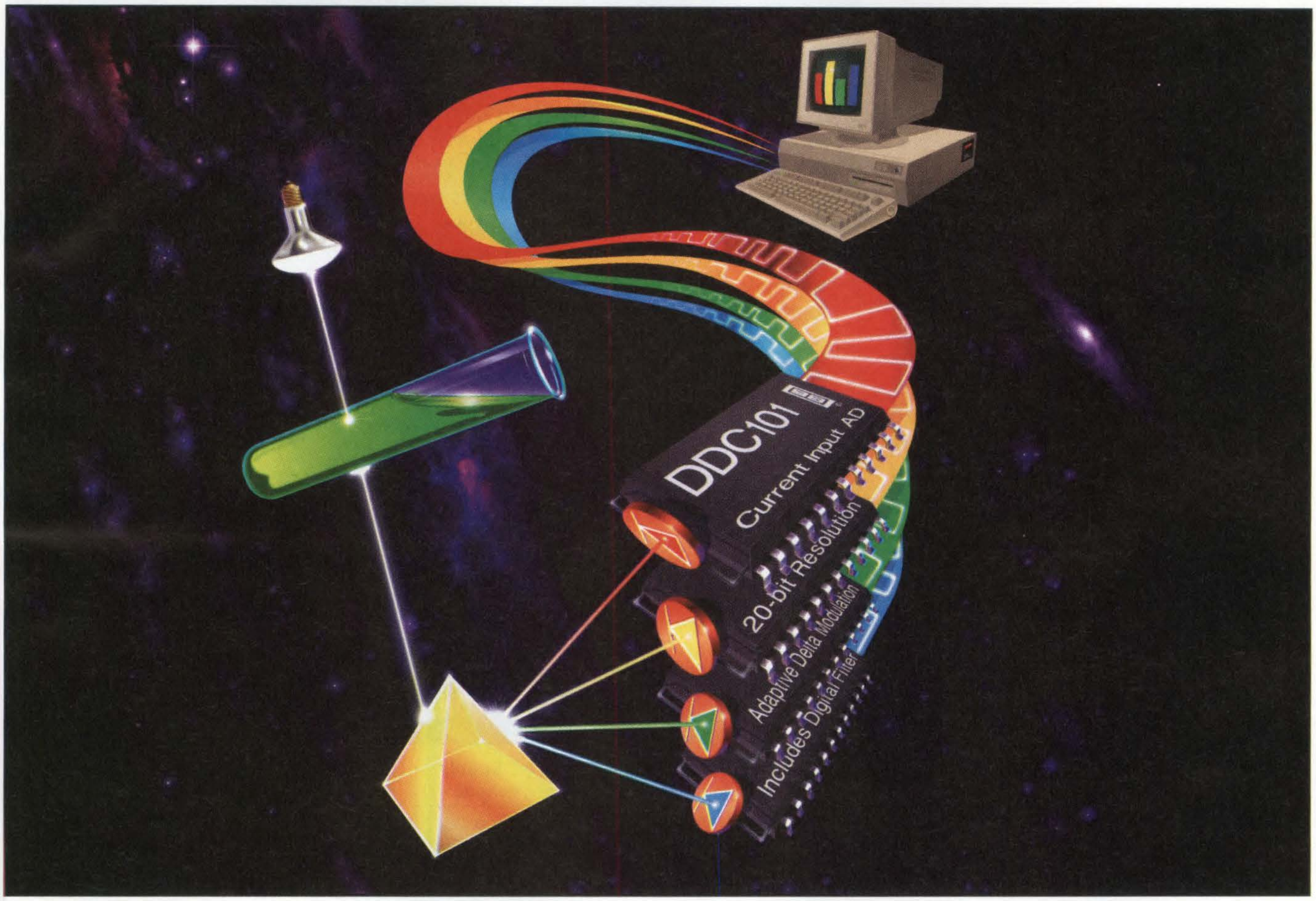
Automatic test makes life easy

Traditional test methodologies become impractical at such large densities. LSI Logic has developed an automatic JTAG builder that generates IEEE 1149.1 test vectors. The automatic-test capabilities can insert a boundary-scan/test-access-port controller, generate tests for boundary-

TABLE 1—LOW-POWER ASICs (CONT)

Company	Model	Maximum usable gates	Power dissipation (μW/MHz/gate)	Internal gate delay (psec)	Supply voltage (V)	Price	Features
NEC Electronics Inc Circle No. 317	CB-C8 (0.5 μm)	600,000	0.8	130	3.3	208-pin PQFP with 64 kbits of RAM: $50 (10,000)	64 kbits of RAM and 256 kbits of ROM; 300 macro functions include analog components and data-path-compiled macros; GTL-bus interface and on-chip PLL; 440 I/O pads having 124-μm-pitch; 5V-tolerant I/O pins
	ECL-8 (0.5 μm)	23,000 and 68,000	1.5 mW/gate	050	–3.3 and –5.2	68,000 gates in a 364-pin ceramic QFP: $770 (5000)	Supports an output frequency as fast as 1.2 GHz; embedded self-timed RAM; cell structure=10 npn transistors, 16 resistors, one capacitor; 4-GHz toggling frequency; supported by Synopsys and Cadence design software
	BiCMOS-8CL (0.5 μm)	165,000	3.3	180	3.3	$441 (3000) for 447-pin plastic PGA	Operates at 150-MHz I/O frequency; 10KH ECL, 100K ECL; low-voltage TTL and GTL interfaces; 8-nsec 256× 8-bit BiCMOS RAM; on-chip PLL; 3- or 4-layer metallization
Oki Semiconductor Circle No. 318	MSM33S-0000 (0.8 μm)	6.5 to 135,168	Not specified	250	3 and 5	NRE starts at $33,000	Automatic test-vector generation using scan macros; clock-skew management guarantess <1-nsec skew; slew-rate-controlled outputs; megacells, such as UARTs, SCSI controller, and JTAG boundary scan
	MSM10R-0000 (0.5 μm)	12,230 to 541,632	Not specified	110	3.3	NRE starts at $98,000	624 I/O pins having a 100-μm pitch; 3-layer metallization; megacells include RAM, ROM, UARTs, and SCSI controller; clock-skew management of 0.5 nsec; IEEE 1149.1 JTAG boundary scan
SMOS Circle No. 319	SLA2-0000 (0.65 μm)	10,700 to 100,000	1.6 at 3V	280 at 5V, 45 at 3V	3 and 5	NRE starts at $15,000	System clock speeds >100 MHz; I/O-level shifting to handle mixed-voltage supplies; 128 to 368 I/O pads; RAM and high-density megacells, including UARTs and embedded Z80 μP
	SLA100L (2 μm)	6400	0.3	8.5 nsec at 1.5V	0.9 to 3	NRE ranges from $15,000 to $25,000	2-layer metallization; 178 I/O pads; 4- and 8-mA output current at 5V
	SLA100X (2 μm)	1224 to 6200	0.3 at 1.5V	8.5 nsec at 1.5V	0.9 to 3	NRE ranges from $15,000 to $25,000	On-chip level shifters from 1.5 to 3 and from 3 to 5V; 2-layer metallization; 24- or 48-mA output drive current at 5V
Synergy Circle No. 320	System Elements family (1.2 μm)	500 to 3500 cells (70,000 gate equivalents)	Programmable at 350 to 1200 μW/cell	70	5	Not specified	Bipolar and BiCMOS with transistor trench isolation for f_t=17 GHz, mixed-signal designs with more than 20 analog blocks, including PLLs and DACs; 2-level ECL structures

Table continued on pg 48



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scan logic, and automatically generate boundary-scan description logic. The builder uses the JTAG cells in the ASIC libraries. The 500,000-gate, 3.3V library includes RAM, ROM, FIFO buffers, delay-line memories, PLAs, and content-addressable memory. The library is also available in a 2.4V version for internal and I/O macrocells.

VLSI's 0.5-μm FlexArray and cell-based designs have both SRAM and ROM compilers for as much as 128 kbits of memory. Cell-based designs can use a functional-system-block library that comprises embedded processors, serial communications controllers, SCSI controllers, and host interfaces. A typical 2-input NAND gate operating at 3V with a fan-out of 2 has a 190-psec propagation delay and a 1.1-μW/MHz/gate power factor.

LOOKING AHEAD

Vendors are relentlessly pushing to lower process geometries to achieve higher gate densities and lower feature levels. Attendant with this push is the drive to maintain low-voltage power supplies and, consequently, lower power consumption. But changing a fabrication facility to achieve lower geometries is a pure financial decision. It costs about $500 million to put a new fabrication facility in place. Therefore, many vendors want to reap some benefits from existing facilities before investing in a new one.

Nevertheless, companies are going forth with fabrication investments. For example, American Microsystems Inc will bring a 0.6-μm facility on-line by the fourth quarter to produce a family of 3V-only gate arrays. IBM has already approved a 0.25-μm fabrication facility for higher-density arrays operating at 2.5V. The new family will feature five layers of metallization, shallow trench isolation, and stacked vias. These low voltage ASICs are increasingly interfacing to low-level interfaces, such as Gunning transceiver logic, low-voltage TTL, and PCI.

The packaging issue for these high-density, low-voltage gate arrays has gotten out of hand. Ball-grid arrays seem to be popular, but ceramic pin-grid arrays, plastic flat packages, ceramic flat packages, tape automated bonding, and plastic leaded chip carriers all come with myriad pin counts and are vying for position. Your choice depends on cost and thermal demands (**Ref 1**).

TABLE 1—LOW-POWER ASICs (CONT)

Company	Model	Maximum usable gates	Power dissipation (μW/MHz/gate)	Internal gate delay (psec)	Supply voltage (V)	Price	Features
Texas Instruments Circle No. 322	TGC1000 at 5V, TGC1000LV at 3V (0.7 μm)	16,000 to 455,000	0.8 at 3V	270 at 5V, 360 at 3V	5 or 3.3	NRE starts at $20,000 for the TGC1000 series	2- or 3-layer metallization; sea-of-gates architecture with digital PLL operating as fast as 100 MHz at 5V and 60 MHz at 3V; CMOS base cell operates as low as 2.7V; supports mixed-voltage I/O levels; automatic test-pattern generation using level-sensitive scan design
Toshiba Circle No. 323	TC180 Series (0.5 μm)	30,000 to 315,000 (TC183G)	2.2	230	3.3 and 5	NRE: $114,600	Gate array (TC183G), embedded array (TC183E), standard cell (TC183C); 3.3 and 5V I/Os; 2- or 3-layer metallization; embedded blocks include RAM and multipliers; 628 I/O pads
	TC170 series (0.7 μm)	22,000 to 194,000 (TC170G)	4.4	270	5	$15 for 45,000 gates	2-layer metallization, less power than previous 0.8-μm, 5V ASICs; gate array (TC170G), standard cell (TC170C), libraries compatible with TC180 series
VLSI Circle No. 324	FlexArray (0.5 μm)	800,000	1.1	190	3.3	Not specified	2- and 3-layer metallization, cell-based libraries contain large functional-system blocks; supports system-clock rate as fast as 200 MHz; 672 pins on a taped ball-grid array; GTL- and PCI-compliant I/O interfaces; IEEE 1149.1 boundary scan

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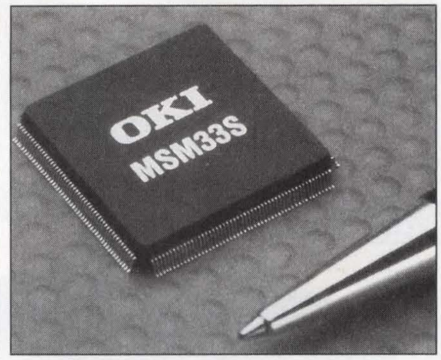

Oki Semiconductor's 0.8-μm MSM33s0000 sea-of-gates architecture features slew-rate-controlled outputs, which can be configured as 3 or 5V, TTL, or 3-state having a 2- to 24-mA driver.

Hitachi recently introduced a 0.5-μm CMOS gate and embedded array having raw gate counts ranging from 52,000 to 667,000. The HG72G/E family operates faster than 100 MHz and has 500,000 usable gates and as many as 500 I/O pins. Despite advances in low-power operation, such ASICs can dissipate 15 to 20W. Hitachi has developed a ball-grid-array package with as many as 672 I/O pins to handle these high-density applications. The HG72G/E family offers on-chip PLL clocks and a maximum metallized memory storing 256 kbits.

Table 1 highlights some representative low-power ASICs. Although the gate densities are high, many of today's EDA tools and package technologies limit the practical density of designs. Many times you can achieve a power savings by breaking up a design into multiple ASICs and using more than one less expensive package. EDN

Reference

1. Pivin, David P, "Pick the right package for your next ASIC design," *EDN*, February 3, 1994, pg 91.

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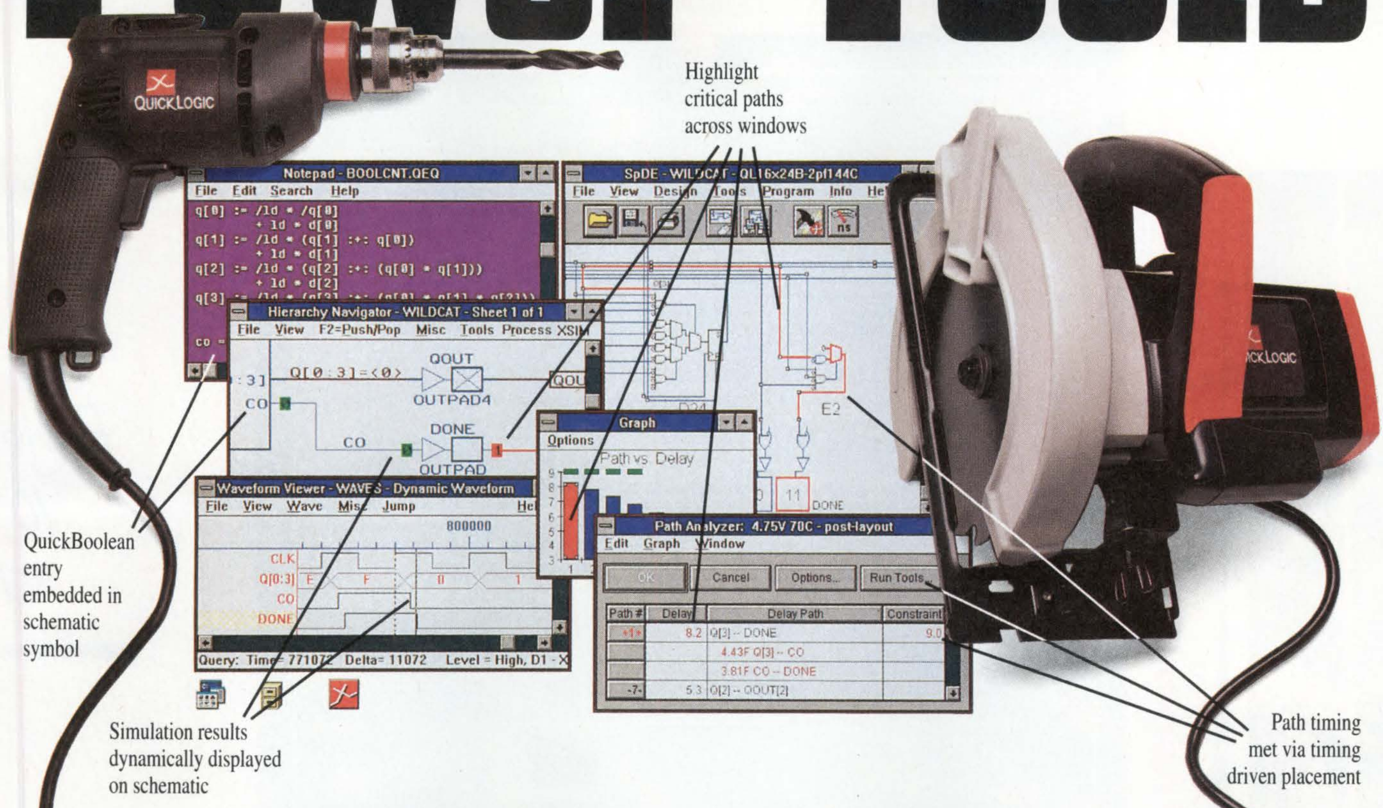

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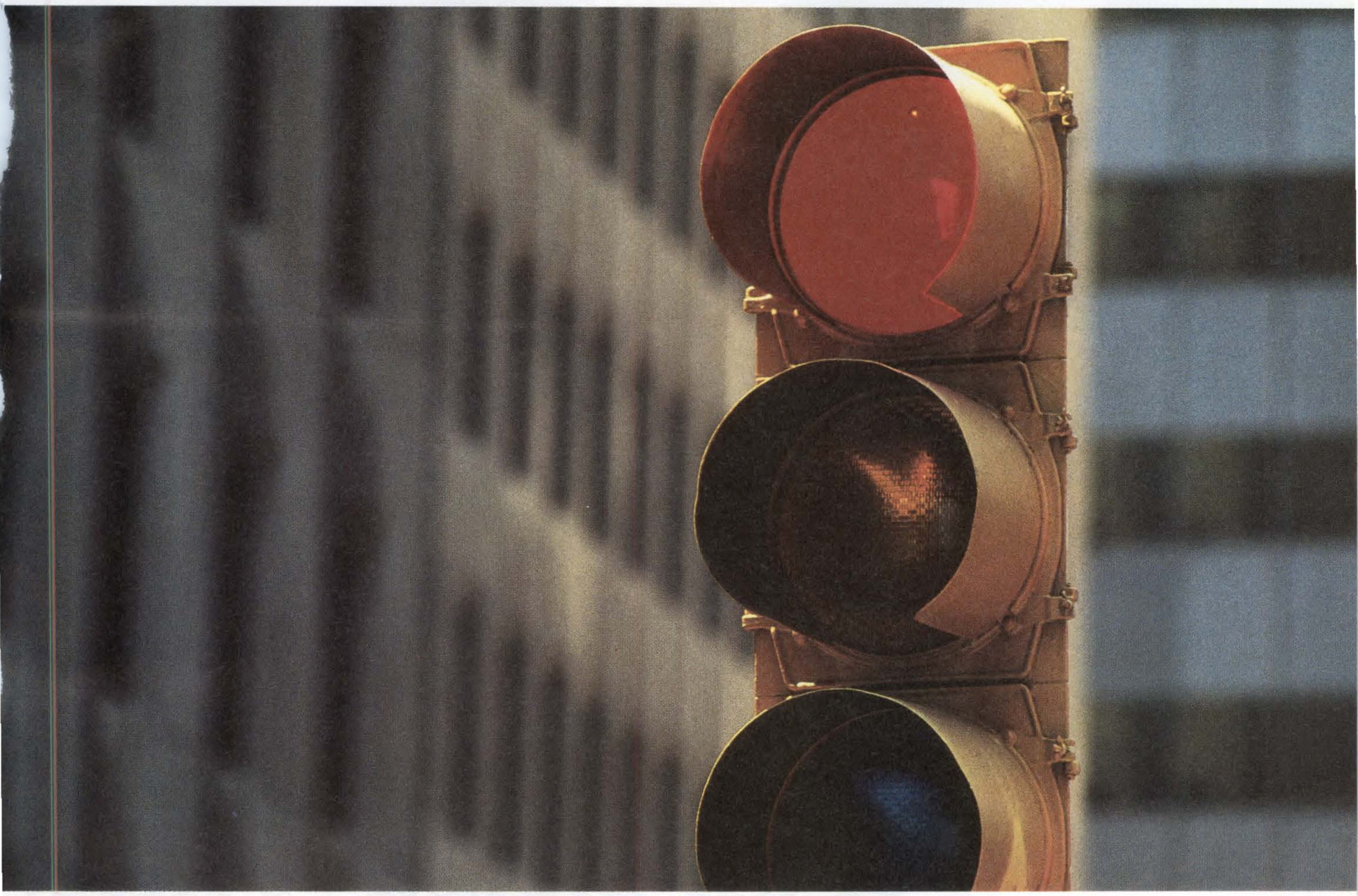

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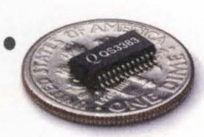

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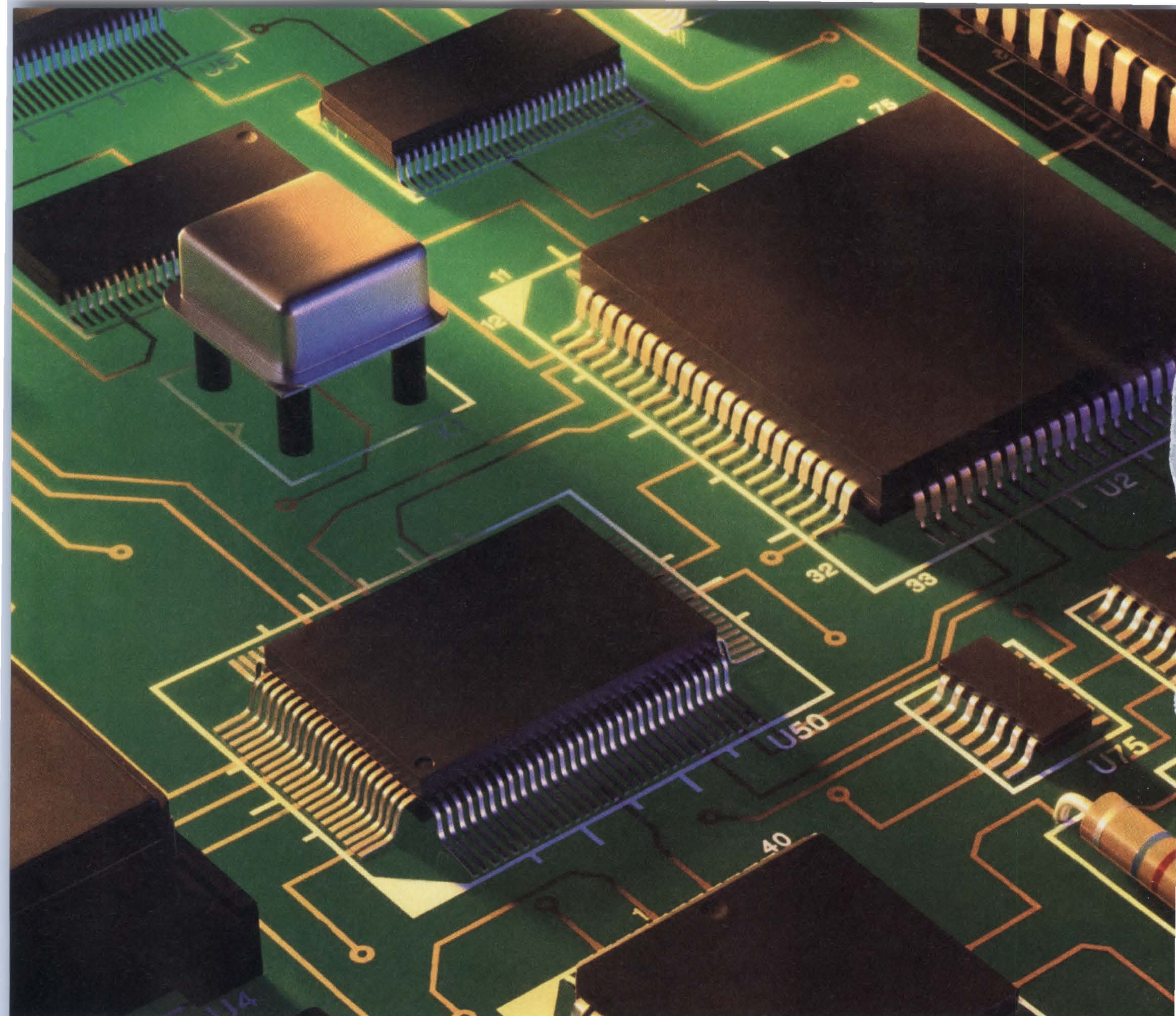

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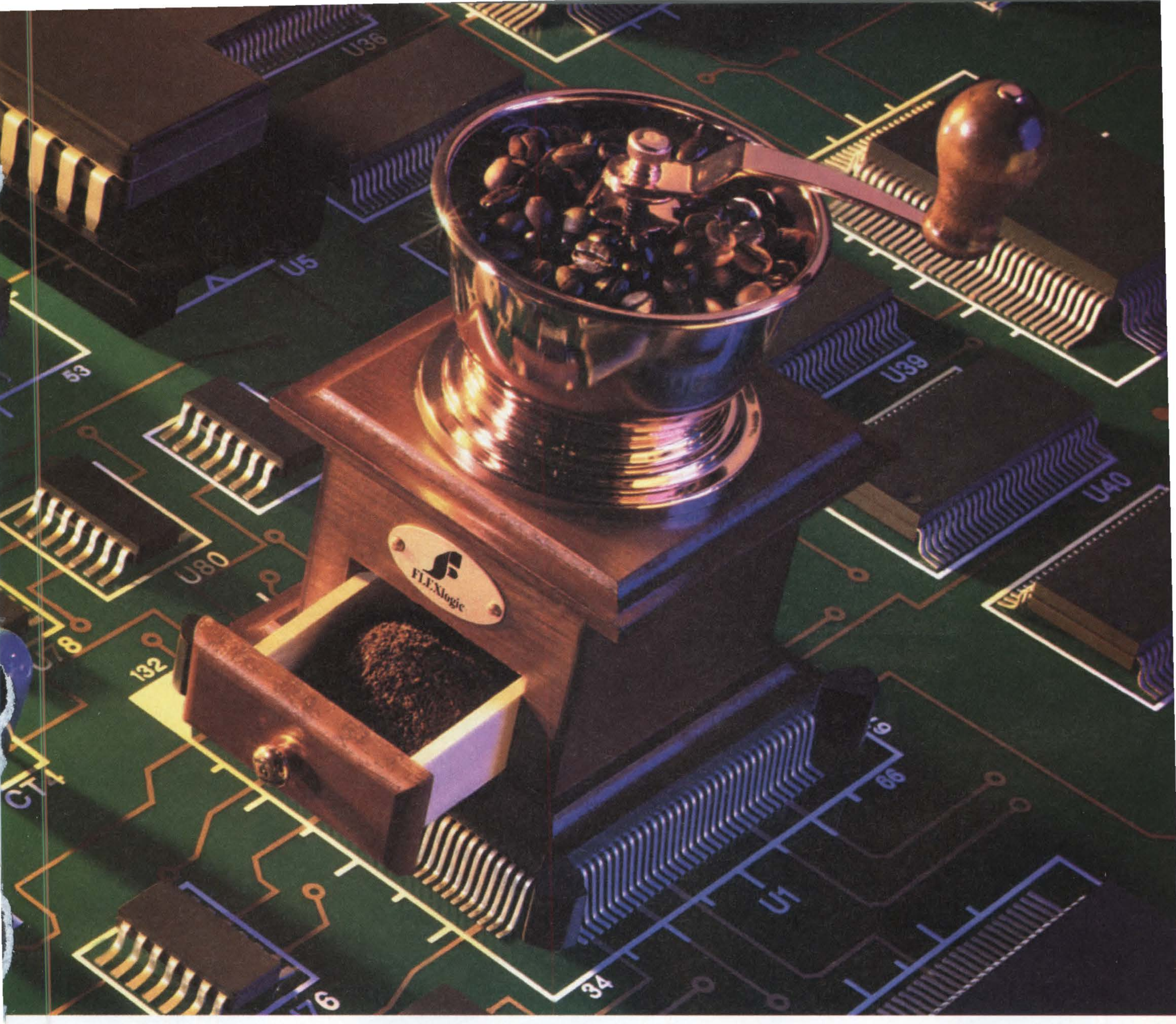
iFX740	40	10ns	50	1mA/MHz
iFX730	30	10ns	30	1mA/MHz



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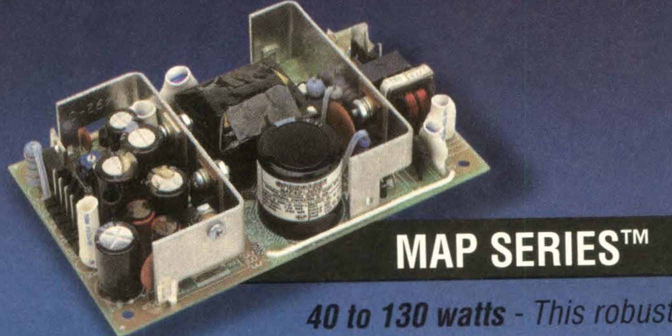

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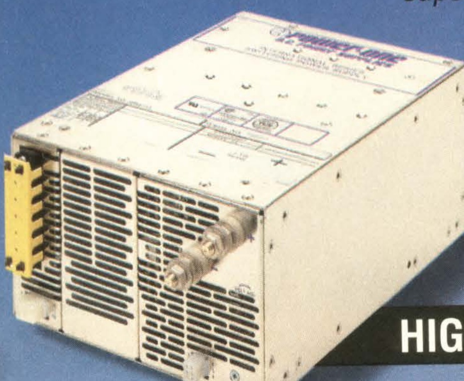

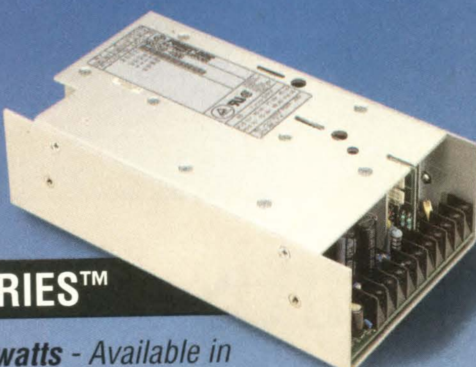

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CIRCLE NO. 124

SURFACE-MOUNT POWER MAGNETICS

Isolated innovation marks movement toward miniature magnetics

RICHARD A QUINNELL, Technical Editor

Hampered by fundamental physical limits and manufacturing constraints, the magnetics industry is slowly joining the trend toward surface-mount designs. Standardization, however, remains a distant dream.

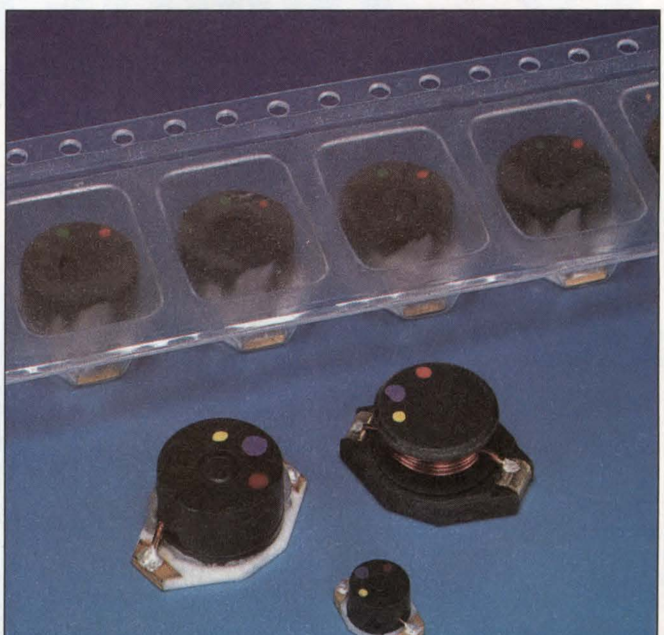
Nearly every segment of the electronics industry has struggled to adapt to surface-mount technology. One of the last holdouts, the magnetic component used in power conversion, is finally adapting, and innovative products are beginning to appear. Surface-mount power magnetics form an immature technology, however, and designers should proceed carefully when selecting components. They should also keep their expectations modest.

Compared with the progress that other electronic components have made toward surface mount, magnetics are only now emerging from the dark ages. Offerings are limited, standardization is nonexistent, and components are still relatively bulky. But such a comparison is a bit unfair, because magnetic components suffer from some fundamental limitations that other components don't face.

Consider, for example, the component's bulk. Before surface-mount technology became widespread, devices such as resistors, capacitors, and semiconductors were a given size, mainly based on packaging. The functional portion of the component could be as low as 20% of the package's total volume. The ubiquitous $^1/_4$W resistor, for example, was widely used because it was inexpensive, not because designs needed the power rating. As circuits shrank, reducing the resistor's size was relatively easy. Even ICs have seen much of their size decrease because of packaging innovations, not die shrinks.

As a result of the relative ease with which other components shrank, designers have come to expect similar strides in magnetic components. They have been disappointed. Yet there are a number of significant reasons as to why progress has been slow. These reasons include both manufacturing and physical limitations.

Most magnetic component manufacturers are small to midsized companies with tools



Surface-mount power magnetics such as the DT and DO series from Coilcraft, shown here, are making some strides toward compactness. Ultimately, however, such devices are limited in how small they can become by their core dimensions.

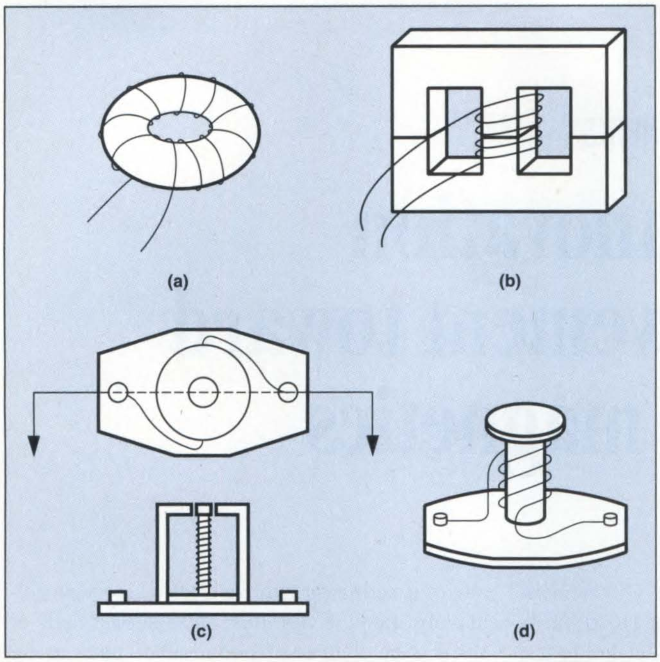


Fig 1—Surface-mount inductors can have an open- or a closed-core design. The toroid (a), double-E (b), and pot (c) cores form closed magnetic paths, reducing the generation of EMI. The open-core design (d) can handle more current but can interfere with sensitive components.

designed for producing traditional component sizes. Most equipment for producing magnetic cores, for example, has an absolute machining tolerance of 0.1 mm to 0.5 mm (0.005 to 0.020 in.). That tolerance is fine for components that are larger than 10 mm (0.4 in.). It represents an intolerable variability when creating a product that must be shorter than 1.2 mm (0.05 in.) to fit inside a PCMCIA card. But the smaller companies remain reluctant to retool because the resulting capital expenditure represents a significant portion of their resources.

Such problems are readily solved, however, if there is enough money waiting for those that take the risk. The market is not yet at that point. The emergence of a substantial, uniform market for small magnetic components or the assistance of a large customer is needed to change the manufacturing situation. What will not change so readily are the physical limits that keep magnetic components relatively large.

Physics prevents small magnetics

The physical limits stem from the energy-storage capacity of magnetic devices. The energy (W) stored in a component with inductance (L) carrying an instantaneous current (I) is:

$$W = {}^{1}\!/_{2} LI^2.$$

If the inductor is a solenoid of height (h) and core cross-sectional area (A), its inductance value is approximately:

$$L=\mu N^2A/h, \quad (1)$$

where μ=the core inductance and N= the number of turns of wire around the core. The magnetic field strength (B) inside the core is:

$$B=\mu NI/h. \quad (2)$$

Magnetic cores have an upper limit on the field strength they can contain that, in turn, limits the energy the inductor can store. Solving Eq 2 for I and combining with Eq 1, you can calculate the energy storage as:

$$W=B^2Ah/2\mu.$$

The volume (A×h) of core material used, therefore, sets an upper limit on the energy an inductor can store.

The energy-storage needs of power-converter circuits, then, determine the minimum size surface-mount magnetic components can achieve. You have some flexibility in that you can trade increased core area for decreased height, thus shrinking the magnetic component's profile. There must be enough height to accommodate the wire turns, however, so even this tradeoff has its limits.

LOOKING AHEAD

Designers' major complaint about surface-mount power magnetics, their lack of standards, is unlikely to be corrected anytime soon. For many magnetics suppliers, their competitive edge is the uniqueness of their products. Once their products are designed in, the manufacturers are ensured of a customer. A move toward standardization threatens their existence.

That situation could change if the market demands standardized products. There are some indications that such demands are growing, but the market remains small. The most likely candidate for growing the small standard-magnetic-component market is the PCMCIA card. It has the potential of forming a large demand for low-cost, widely available magnetics; that is, standardized products.

The designer's other complaint, size, is more likely to see industry activity, although that activity will remain sporadic without a concurrent move toward standardization. Magnetics manufacturers are interested in finding new designs and methods; they just can't afford to take too much risk on their own. With the help of large customers, however, they will continue to create options in small magnetic components. Progress will be slow, that's all.

Increase f, lower L

Another option is to raise the switching frequency (f) in your power-conversion circuit. The size inductor you need is inversely proportional to the switching frequency. Increasing switching frequency has its drawbacks, however.

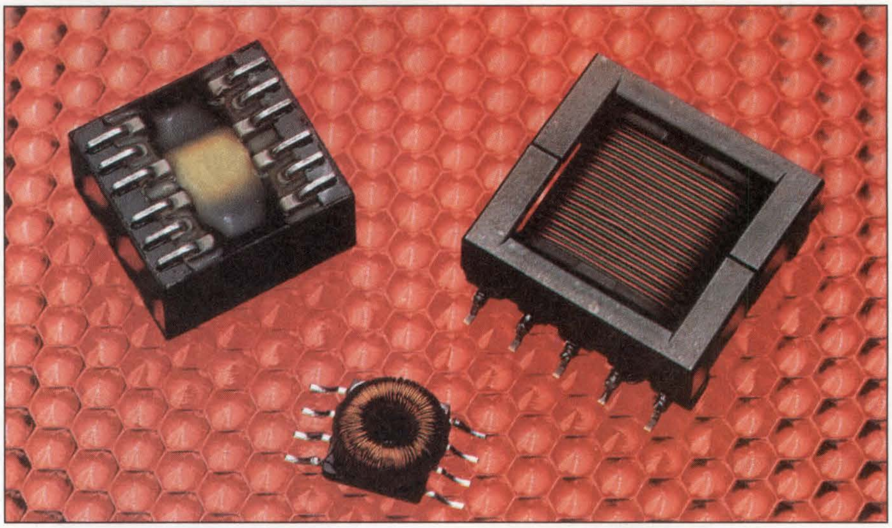
SURFACE-MOUNT POWER MAGNETICS

In addition to generating additional EMI, higher frequencies increase ac losses in the inductor. These losses come from two effects: eddy currents and skin effects.

Eddy currents are electrical currents induced in the magnetic core material by the changing fields within the core. The currents circulate around the magnetic field path, dissipating energy as heat within the core material. The size of the currents depends on the changing magnetic field's frequency and the core material's conductivity. Proper selection of core material will limit eddy-current losses.

The skin effect refers to the tendency of high-frequency currents to remain near the surface of conductors. Because the current occupies only a portion of a wire's cross section, the wire's effective resistance increases with frequency. The solution is to use stranded wire when winding the coil, thus increasing the conductor's surface area for the same total volume. Winding small coils with fine stranded wire, however, can prove to be a costly alternative.

If you can't change your design to reduce your inductor needs, you're stuck with the core-volume limit. This limit is the major reason why surface-mount power magnetics have lagged behind other components in size reduction. All is not lost, however. There have been innovations in the industry, and several manufacturers have developed unique structures to reduce component size.



A number of different core types are available in surface-mount form. Not all have the flat surfaces needed for automatic pick-and-place assembly, however. (Photo courtesy of GFS Manufacturing)

Two of the most common configurations for power magnetic components are the toroid and the double-E core (**Fig 1a** and **b**). Both are available in surface-mount versions from a variety of manufacturers. More recently, structures such as pot core (**Fig 1c**) have become available in products such as the Coilcraft DT series. Coilcraft has also created an open-core product (**Fig 1d**), the DO series, to provide increased current-handling capability.

Open-core structures are smaller

The open-core structure of the DO series provides several attributes that allow for a greater energy-storage capability than do the more common structures. Because the magnetic field path passes through air, which does not saturate, the device can carry more current before saturating. In addition, the structure allows the use of thicker wire than is feasible with shapes like the toroid or double-E core, which have windows in the core material that thick wire would rapidly fill. The thicker wire offers less resistance, hence introducing less loss into the power conversion.

A family of axial inductors from GFS Magnetics also uses the open-core structure. These inductor blocks are intended for in-line filters in power conversion circuits and offer low dc-resistance. A 10 μH inductor can handle as much as 4A-dc current, and inductors as large as 1 mH are available.

The drawback of the open-core structure these two devices use is a greater tendency to generate EMI. By allowing the field to pass through the open air, the open-core structure runs the risk of having the field interact with other parts on the circuit board. Closed cores constrain the inductor's magnetic field to reside almost entirely within the core.

Coiltronics has made use of planar magnetics to produce an innovation in

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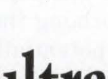

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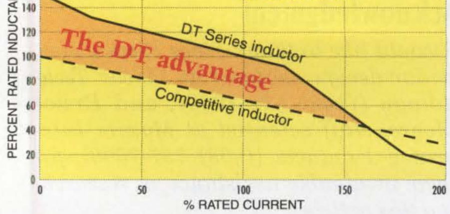
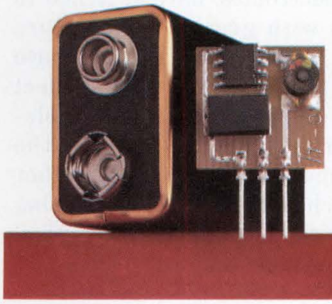


zero or low current. This "swinging" inductance characteristic is especially desirable in converters that have varying load currents. It eliminates the need to



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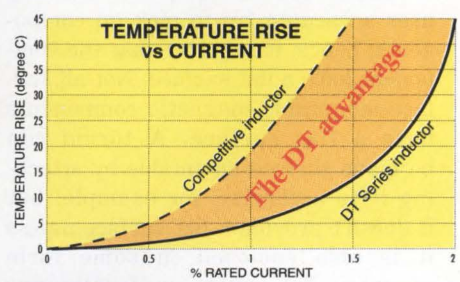

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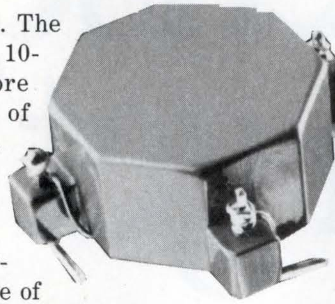
SURFACE-MOUNT POWER MAGNETICS

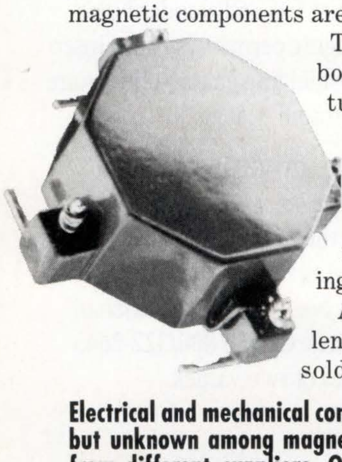


closed-core design. The company offers a 10-µH double-E core inductor capable of handling 600 mA (peak) yet only 1.19 mm high. The device uses the traces on a multilayer pc board in place of wire for the coil, increasing the coil density. The device, dubbed MicroPower, is the first in a family of low-profile parts that the company will slowly develop as standard products.

Manufacturing challenges remain

Even though the industry is producing some small components, surface-mount magnetics are far from a mature product. You still have some factors to consider that may affect your design's manufacturability. Also, surface-mount power magnetics present some significant manufacturing challenges.

One challenge involves the pick-and-place equipment that automatically positions components on a circuit board for soldering. Such equipment typically uses a vacuum tip to pick up components; hence, it requires that the component have a flat surface. Not all surface-mountable magnetic components have a flat surface. A toroid can be made surface-mountable by attaching it to a carrier, for example, but it doesn't provide a flat surface unless it is also enclosed in some form of case. Yet many surface-mount magnetic components are not enclosed. This forces the board manufacturer to place these components by hand, increasing your design's manufacturing cost.



Electrical and mechanical compatibility is all but unknown among magnetic components from different suppliers. One exception is the Octa-Pac series from Coilcraft. GFS Manufacturing offers the Power-Pac series, a compatible part, shown here.

Another challenge lies in the soldering methods for surface-mount circuit boards. The most common method uses a heated chamber or IR radiation to melt solder attached to both the board and the components, causing the two solder volumes to flow together. This reflow-soldering technique requires heating the assembly to 220 to 250°C for approximately 30 sec.

The problem is, most magnetic components are made of materials that are rated only at 130 to 150°C continuous exposure. The brief excursion to higher temperatures risks damaging such things as the enamel insulation used in coil windings. The high temperature also risks deforming the plastics used in the cases, potentially causing the component to lift from the pc board during soldering.

To combat this problem, some magnetic-component manufacturers, such as Pico Electronics, have switched to materials with greater temperature tolerance. Other manufacturers have designed their components to deflect the heat away from sensitive elements, providing resistance to the brief temperature excursion. Either way, you should check your soldering process with the magnetics manufacturer to ensure that the parts will survive.

A final manufacturing challenge comes from the limited selection of surface-mount magnetic components available. You may be forced to go with a custom design in order to meet your circuit's needs, with the attendant development cost. Even if you can use a stock value, you still face one of the custom component's drawbacks: a sole-source supplier. Magnetic-component suppliers each have their own techniques and product styles. Rarely do two manufacturers offer devices that are both electrically and mechanically similar.

Limited standardization

One exception is the Octa-Pac series from Coiltronics. This design has been popular enough that other manufacturers have begun to copy it. GFS Magnetics, for example, has introduced its Power-Pac series, a pin-compatible equivalent to the Octa-Pac.

Such exceptions are rare, however. Many magnetics manufacturers attract and retain their customers by offering unique capabilities. Changing from their unique designs to industry-standard products would force them to invest in equipment and tooling without the guarantee of customers. There is little internal motivation to follow that approach, nor are there any magnetics-industry groups that can impose standards. Only a large customer or great demand for uniform products will drive them to standardization.

As a result, innovation in surface-mount power magnetics continues to occur on a sporadic and disjointed basis. So, if the devices that are available don't meet your needs, don't expect the industry to offer alternatives soon. Change comes slowly on its own. Your best bet is to work with a supplier to develop the product you need. Magnetics manufacturers are glad to help find innovative answers to your surface-mount magnetics needs, if they're not in it alone. EDN

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1. Nelson, Carl, "LT1070 Design Manual," *Application Note 19*, Linear Technology, June 1986.

2. "Careful inductor selection optimizes low-power dc/dc converters," *Maxim Engineering Journal*, V4, Maxim Integrated Products, 1991.

Acknowledgment

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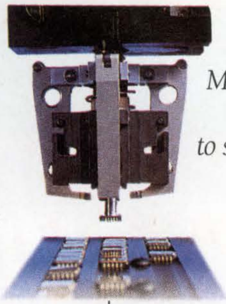

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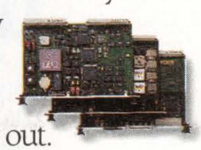

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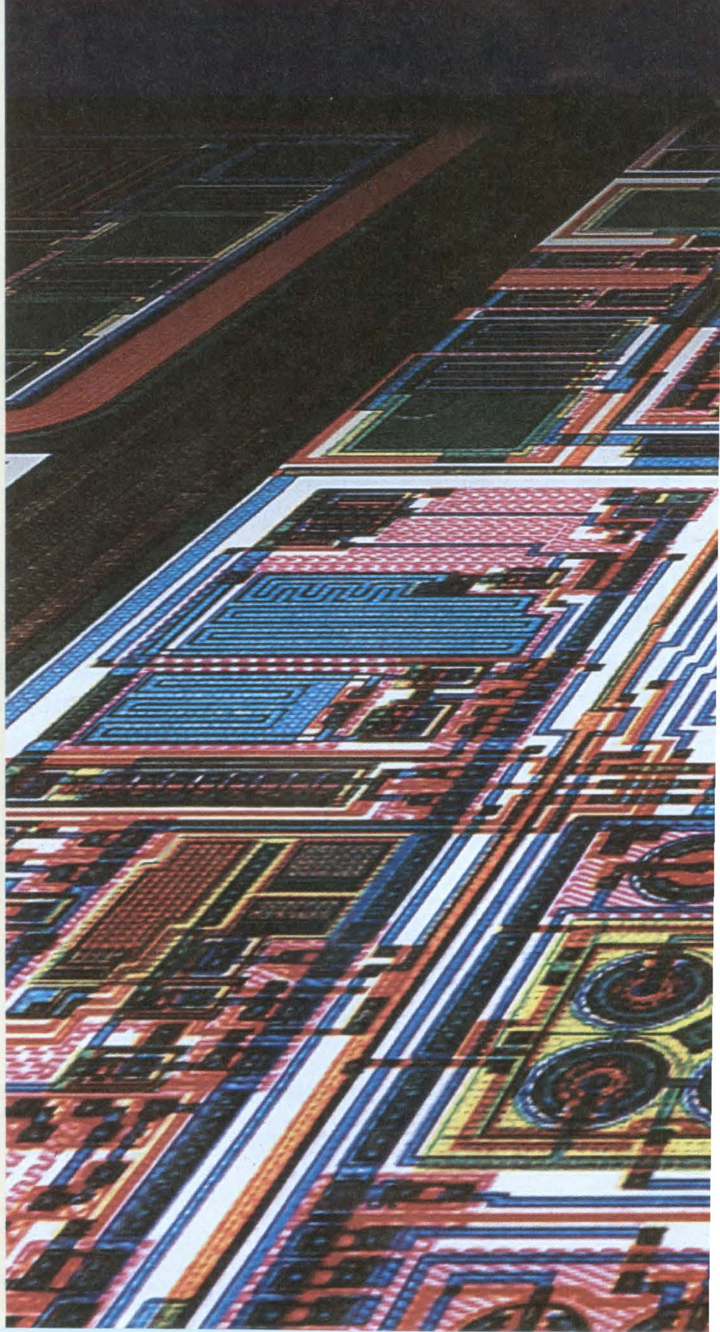

With the advent of process technologies that can integrate virtually everything but the load itself, the current capabilities of ICs for power actuation and switching seem almost limitless. The potentially integrated functions include logic and control, sometimes implemented by a fully functional microcontroller (μC); protection; diagnostic feedback; and, finally, a power-output stage. Whether you call it "smart" or "intelligent" power, the technical feasibility of combining these functions into one IC using some mixture of bipolar, CMOS, and DMOS (double-diffused MOS) structures is proven. (See **box**, "Combining power with memory and a μC.")

However, once manufacturers started reaching this technological peak, some of them also started backing down the hill. While the concept of a complex IC that can perform every necessary function is allur-

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POWER ICs

ing, the cost and complexity of these ICs greatly narrow their applications. As a result of some disappointing sales, some vendors have backpedaled, now mainly offering custom devices and few if any standard products. Others have concentrated on improving their process technology and have forged ahead producing even more highly integrated devices, again mainly on a custom basis. These companies have lowered costs by carefully targeting their products and services for high-volume markets and by working closely with customers to deliver specific high-performance ICs.

Still other vendors, even those that have the bipolar, CMOS, and DMOS (BCD) technology to produce high levels of integration, are trying an intermediate approach. (See **box**, "Taking the middle ground.") The overall result is a power-IC business that involves both custom products and a diverse category of standard products for specific markets and for the general industrial market. Because of this diversity, many of these products are proprietary, although a few compatible sources, particularly of simple driver ICs, do exist. Spice models also become more rare as ICs increase in complexity.

Tackling the definition

Just what constitutes a "power IC" varies from manufacturer to manufacturer, depending on their product portfolios and points of view; that is, whether they approach the market from a discrete-transistor or an IC perspective. Some define power ICs by their functions—whether the IC actually includes the power transistor itself—others, by the ICs' voltage and current levels, and still others by the ICs' general involvement in controlling power. Even the nomenclature of power ICs is mind-boggling: There are Smart SIPMOS, SmartMOS, and PowerPlus, to name a few.

The result is confusion. To eliminate further confusion, avoid trying to define a power IC explicitly, and instead think of how semiconductors involved with controlling power fit into a general framework (**Fig 1**). The **figure** shows two independent paths of devices, beginning with discrete power transistors and driver ICs. As integration increases, each device adds functions until the transistor and driver combine into one. **Fig 1** focuses not on what manufacturers label these parts but on the parts' internal functions. That's because names can be extremely misleading; a simplistic name like "switch," for example, can obscure the part's sophistication.

While **Fig 1** puts the products and nomenclature into perspective, the **boxes** describe some devices that constitute this framework and some emerging applications. However, before jumping too quickly into the details, take a general look at the power-IC business in which strong market forces affect vendors' approaches and thus the products available. Also, consider one key design decision: to use discrete transistors and drivers or to use an IC that combines the two.

Vendors offer a wide range of products, but several manufacturers carefully tune those products to high-volume markets. Because of the trend in the 1980s for vendors to produce ICs with higher and higher levels of integration, many vendors have focused their power-product portfolios on two market segments: automotive and computer peripheral. The most successful of these ICs

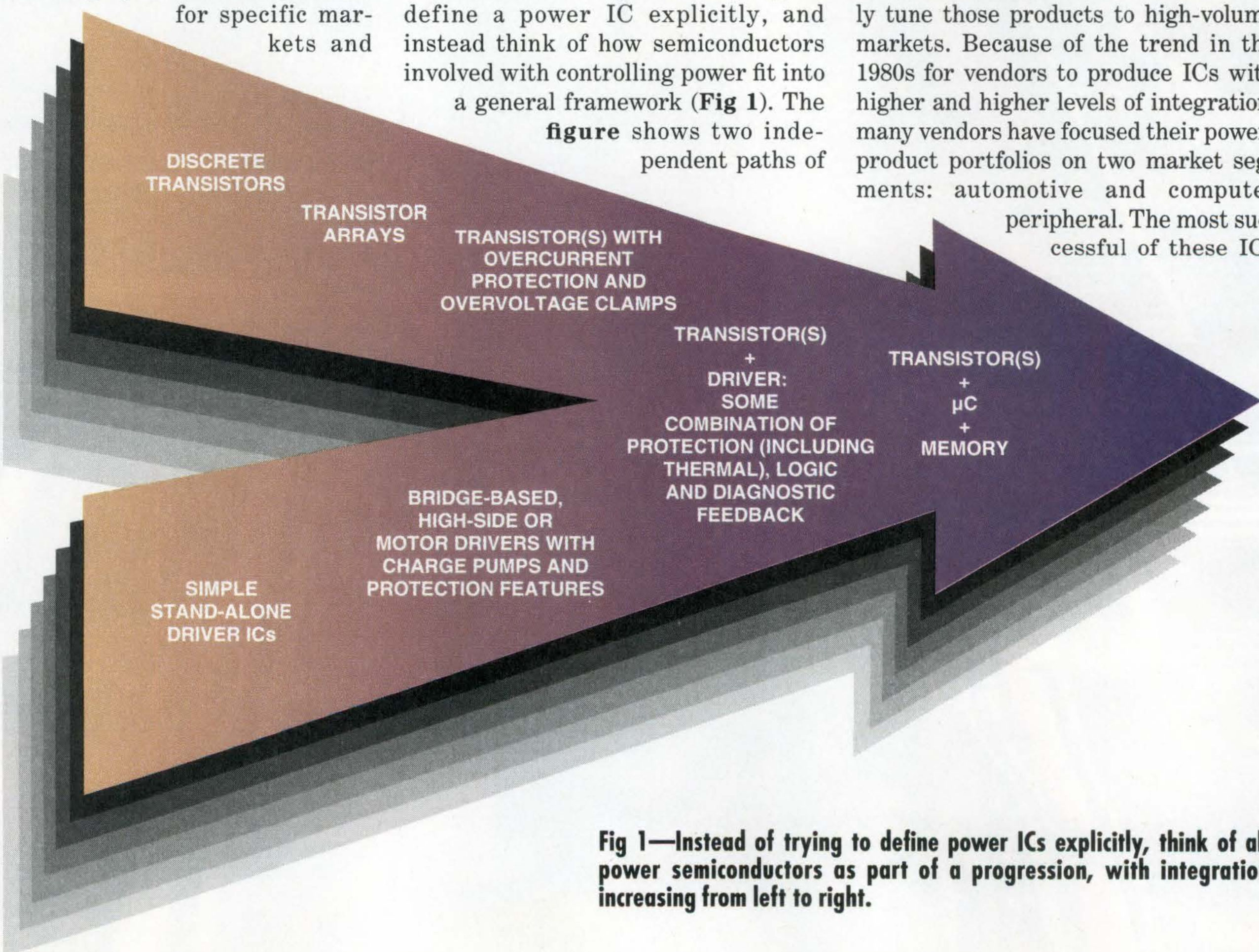


Fig 1—Instead of trying to define power ICs explicitly, think of all power semiconductors as part of a progression, with integration increasing from left to right.

COMBINING POWER WITH MEMORY AND A μC

Combining power devices with a microcontroller (μC) and memory currently represents the highest level of integration. To date, a number of manufacturers, including Motorola, Philips, SGS Thomson, and Texas Instruments, have demonstrated this capability, as the material in **Ref 1** shows. In 1990, Motorola integrated its 8-bit 68HC05 core with 96 bytes of RAM and 2064 bytes of user ROM and 240 bytes of ROM for test functions.

More recently, SGS Thomson unveiled its third-generation BCD3 process with which the company can combine an ST6 8-bit μC with a DMOS H-bridge power stage, driver and interface functions, a charge pump, and thermal protection. Using BCD3, the company can also integrate EEPROM, making the IC configurable by hardware and software. This "programmable power device," or "power PLD," contradicts the notion that "high integration means narrow application." With the SGS Thomson technology, you can potentially use a highly integrated device for a variety of applications.

TI's Prism process technology physically joins DMOS power switches with μC cores, memories, and analog. Prism tackles this joining through a modular design methodology that minimizes the number of mask steps to only those required for each IC; a power-only device takes six to eight mask steps, for example, and a fully featured product takes 16 to 18. Harris Semiconductor also uses a semicustom cell-based approach to build power ASICs.

While this technology is extremely impressive, taking advantage of it requires a close working relationship with the vendor, so that the vendor is essentially providing a custom IC. SGS Thomson provides demonstration ICs to show what users can accomplish with the BCD3 process.

Detractors of this approach, including other vendors who've been unsuccessful selling many of the massive ICs they've built, always cite cost as the limiting factor.

Samples of SGS Thomson's H081 demonstration IC cost \$10 each. Other devices with similar performance to this IC should cost around \$5 to \$6 each in OEM quantities.

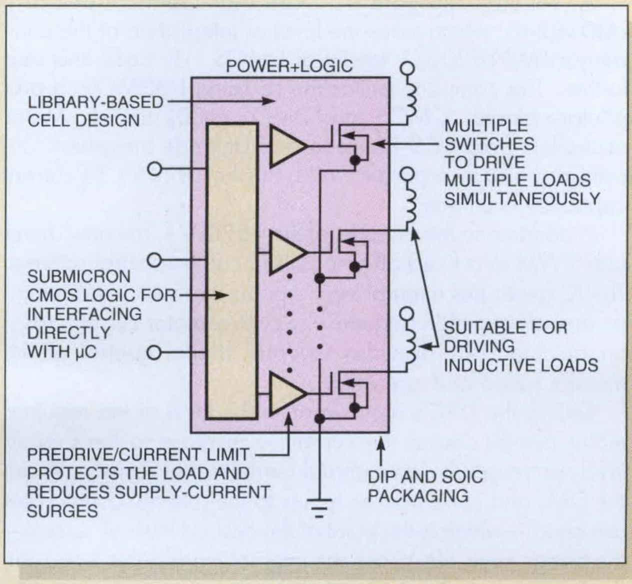
TAKING THE MIDDLE GROUND

With the Power+Logic family, Texas Instruments attempts to strike a balance between power elements, logic functions, and protection features. The company uses the same 60V Prism process to produce these ICs as it does to produce its highly integrated ICs. (See **box**, "Combining power with memory and a μC.") The Power+Logic family suits power-switching applications that require multiple power channels and onboard logic but do not require the advanced fault detection and reporting of highly integrated, intelligent-power ICs.

The first three logic devices in the family—the TPIC6259 8-bit addressable latch, the 6273 octal D-type latch, and the 6595 8-bit shift register—emerged two years ago in standard DIP and SOIC packages. The parts feature multiple independent DMOS power transistors with typical on resistances of 1.3Ω and avalanche energy of 75 mJ. Continuous output current is 250 mA, pulsed output current is 1.5A, and typical quiescent current is 15 μA. The devices include 45 or 50V output-voltage clamps for inductive load switching.

TI is now releasing the second round of family members, which offer the same three logic functions with their currents scaled down to drive arrays of lamps and LEDs. Typical specifications for the 6B259, 6B273, and 6B595 are 5Ω $r_{DS(ON)}$, 30-mJ avalanche energy, 150-mA continuous current, and 500-mA current limit. Prices for all of the devices in the Power+Plus logic family range from \$0.77 to \$1.89 (1000).

The company also uses its Prism process and methodology to produce the Power+Arrays family, ICs that combine two to seven multiple-DMOS power transistors. Current ratings range from 1 to 7.5A of continuous current; $r_{DS(ON)}$ ranges from 0.5Ω to 90 mΩ. The newest low-current arrays come in standard SOIC packages. Prices range from \$1.12 to \$2.42 (1000).



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implemented precise functions for specific needs. One such example is the "combo" disk-drive IC, which combines the spindle and voice-coil motor drives, making smaller drives possible. Many of these specialized products, particularly automotive ones, with typical 60V and 4A ratings, have spilled over into the general industrial market, starting out as custom ICs and eventually becoming standard offerings.

Although the automotive and disk-drive markets are huge, numerous other products target the more fragmented industrial markets. (See **box**, "Fully integrated H-bridges combine PWM.") Also, emerging high-volume markets are pushing the development of power ICs with high voltage and current requirements. The foremost example is the integration of high-voltage structures—generally greater than 100V—with logic-level circuitry. (See **box**, "High-voltage power ICs surge.") Many vendors of these ICs are targeting the market for electronic ballasts for fluorescent bulbs because of its potential volume in commercial applications.

In addition to these strong market influences on IC development, the **box**, "MOSFET drivers enable Class D audio amplifiers," provides a notable example of integrated ICs' effect on a previously unwieldy application.

Regardless of the end use of a power circuit, one principle is common: Users of power components must choose between relatively simple and flexible functions performed well on the one hand and complex—but *conceptually* simple—ICs on the other. The magic of simple functions is that you can quickly and easily configure them in the real world and make any necessary future design changes. The allure of a complex IC is its design simplicity: One IC can do everything.

No one would dispute that drivers and discrete power transistors can produce the most flexible designs. Two developments contribute to this flexibility: the wide availability of discrete transistors, particularly power MOSFETs, and the increasing numbers and types of drivers, particularly MOSFET drivers. Regardless of the driver you select, you can independently select a MOSFET based on the design's speed and efficiency. Vendors of these MOSFETs also continue to make dramatic improvements in the devices' efficiency. The on-resistance ($r_{DS(ON)}$) of state-of-the-art TO-220-packaged N-channel MOSFETs is less than 10 mΩ at 60V. A similarly packaged, state-of-the-art P-channel device has an on-resistance of around 45 mΩ.

Integrated power transistors just can't compete with discrete transistors on the basis of $r_{DS(ON)}$ alone. There is a tradeoff between specific on-impedance—a measure of $r_{DS(ON)}$ vs die area—of discrete transistors and ICs. Most power ICs have higher specific on-impedances than do discrete devices, simply because of fabrication differences that result in the ICs' larger power structures.

Just as discrete transistors' on-resistance has come down, so has that of inte-

FULLY INTEGRATED H-BRIDGES COMBINE PWM

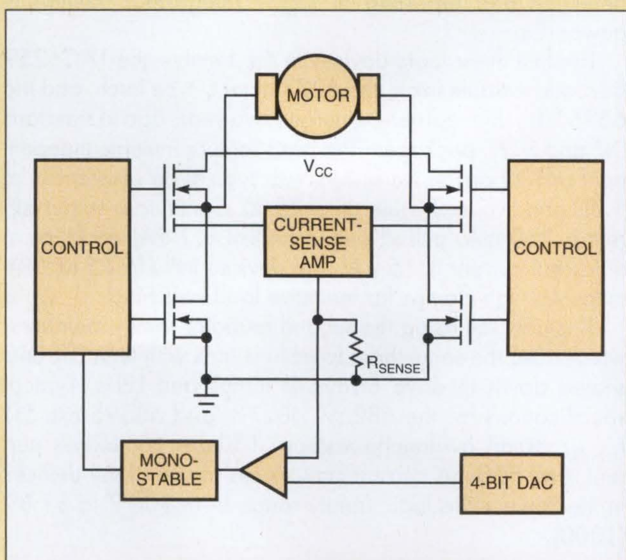
Although it seems that most highly integrated power ICs are geared toward the automotive industry, vendors do develop many ICs—specialized motor controllers and drivers, in particular—for many computer-peripheral and industrial applications. Some of these drivers now integrate PWM to drive bidirectional stepper and dc motors.

A recent example is National Semiconductor's LMD18245, which takes the level of integration of the company's LMD18200/1 family of DMOS H-Bridges one step further. The company builds the IC using LMDMOS, a proprietary bipolar, CMOS, and DMOS (BCD) process. Motor controllers from SGS Thomson and Unitrode Integrated Circuit Corp also incorporate PWM, but the 18245's 3A current capability is unique.

In addition to the features of the 18200/1, the new driver uses PWM in a fixed off-time pulsed current-control scheme. The IC generates internal logic signals that switch the bridge on and off at a high frequency to control motor current. Also, an on-chip DAC provides external digital control of the motor's speed and operation.

Setting the DAC's input word to the level of the required motor current causes the current to increase to the desired level, as sensed by an external current-sense resistor. When the DAC and current-sense inputs to the internal comparator are equal—which is the point of the desired level of current—the bridge shuts off. When the internal monostable times out, the bridge turns back on, and the current again begins to increase to the selected trigger point. Using this high-frequency chopping action, the IC maintains the DAC-selected current level in the motor.

Other features include typical $r_{DS(ON)}$/switch of 0.3Ω, high-impedance current sensing, thermal shutdown, current limiting, and undervoltage lockout. In a 15-lead TO-220 package, the IC costs \$8.45 (1000).



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grated transistors. However, until vendors develop processes that allow for using the same compact DMOS structures in integrated devices that they use in discrete transistors, the two devices' on-resistance numbers will never match because of economic reasons. An IC requires two to four times more die area than does a discrete transistor to achieve the same on-resistance; such a large die area makes ICs too expensive to produce. The on-resistance numbers also depend on vendors' proprietary processes and voltages.

Using discrete transistors also provides two other advantages: reduced size and increased protection. Discrete transistors are undergoing a dramatic shrinkage. For example, Sil-

HIGH-VOLTAGE POWER ICs SURGE

One of the newest abilities of power ICs is integrating high-voltage structures with logic-level circuitry. Some 20 semiconductor companies worldwide, including AT&T Microelectronics, Harris Semiconductor, International Rectifier, Power Integrations, and SGS Thomson, are pursuing high-voltage control applications. One of the high-volume markets driving much of this work is the electronic ballast for fluorescent lighting.

Applying IC technology to electronic ballasts is hot for two reasons: a worldwide drive for energy efficiency is causing a boom in the fluorescent-lighting industry, and real money, in the form of utility-company subsidies to consumers, is behind the increased-efficient-energy effort.

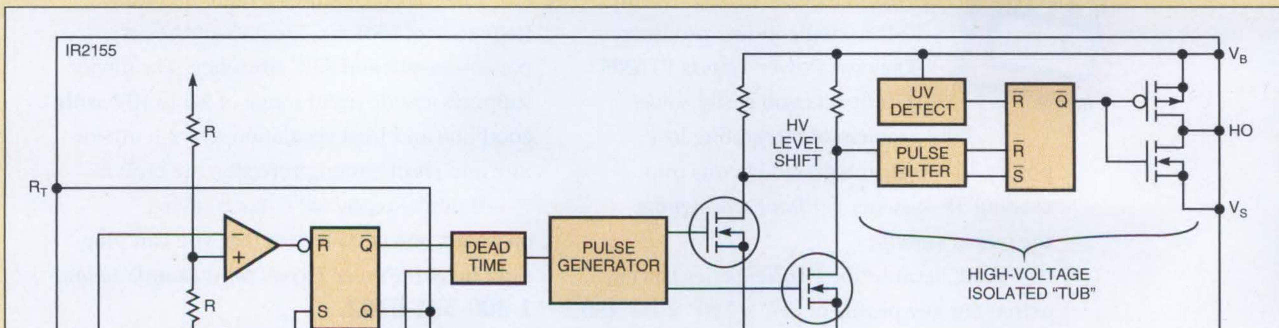
On the technical side, high-voltage IC technology has progressed to the point at which vendors can build low-cost ICs that can compete with existing electronic-ballast designs. These designs typically use a pulse transformer and discrete transistors. Using an IC eliminates the need for a transformer, thus easing the design, increasing efficiency, and reducing the design's size.

A recent example of a low-cost approach for this application is International Rectifier's IR2155 (see "High-voltage ICs displace magnetic components for electronic ballasts," *EDN*, March 31, 1994, pg 73). The IC costs $0.098 (50,000).

In addition to its high-voltage floating section, the IC integrates a number of other useful features. First, the IC self-oscillates at a frequency set by an external R and C, similar to a 555 timer. The IC also has internal circuitry that provides a nominal 1-μsec dead time between alternating high- and low-side output for driving half-bridges. Finally, the IC operates directly from the ac line using an on-chip shunt regulator that generates 15V via a low-watt dropping resistor.

In addition to electronic-ballast applications, high-voltage technologies are also propelling the design of ICs that can work from ac line voltages for all types of applications. For example, a new family of switching-power-supply ICs from Power Integrations shows a significant level of integration and cost reduction. In 3-pin TO-220 packages, devices in the TOPSwitch family integrate a high-voltage N-channel MOSFET with a CMOS PWM controller, including a 100-kHz oscillator and various protection circuits. The off-line ICs work from 85 to 265V-ac voltages and produce regulated dc outputs. Prices are as low as $1 (10,000).

Still other developments include SGS Thomson's BCD-Offline, which extends the company's line of BCD processes to higher voltages by incorporating grounded-source lateral DMOS transistors and insulated-gate bipolar transistors that operate at 500 to 700V. Products undergoing qualification or under development include a full-custom fluorescent-lamp driver and half-bridge driver for appliance motors.



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iconix recently announced Lite Foot, a power MOSFET that is even smaller than the successful Little Foot family. The Lite Foot family, which features performance similar to that of its predecessor, comes in an 8-pin TSSOP package. Manufacturers of discrete transistors have also found inexpensive ways to add protection features, such as overcurrent protection and output-voltage clamps.

Driver types multiply

The second boost to flexibility of discrete-transistor-and-driver designs is the increasing number and types of drivers, particularly MOSFET drivers. The term "MOSFET driver" refers to a wide range of devices. They all provide a buffer between the analog control circuitry and the true power world, inputting relatively anemic signals and actually driving MOSFETs that can require high peak currents. These drivers suit a wide range of applications, including motor controls, power supplies, UPS systems, automobile braking systems, air-bag deployment, and industrial control.

Classes of MOSFET drivers include generic FET drivers that have one output to drive one MOSFET, usually optimized for low-side switching. More complex devices include bridge-based drivers, such as totem-pole, half-bridge, full-bridge, and 3-phase drivers. These bridges are difficult to work with and require designs that prevent shoot-through currents and maintain the refresh on the upper floating supply. One benefit of integration in high-side and bridge-based drivers is the charge pump, which pumps the ground-based supply to the necessary floating-supply voltage to drive the gate at 10 to 15V higher than the upper MOSFET source.

Although these drivers lack a power transistor, they can still implement protection. A separate driver can sense overcurrent with feedback from a series shunt resistor. Some drivers can also sense insufficient gate-drive voltage—a form of undervoltage protection—to prevent the MOSFET from operating in its potentially destructive linear region.

ICs add speed and thermal protection

Clearly, using discrete transistors with many of the available driver ICs

MOSFET DRIVERS ENABLE CLASS D AUDIO AMPLIFIERS

Using a MOSFET driver IC to implement a Class D audio amplifier may seem unusual, but higher integration and faster switching speeds are blending the two. Instead of a motor, the driver's load becomes a speaker and a lowpass filter, and an audio input replaces the motor's control signal. In essence, the same PWM scheme that controls a motor or a switching power supply instead drives a speaker. Harris Semiconductor is championing this idea using its HIP4080 MOSFET driver ($3.50 (1000)).

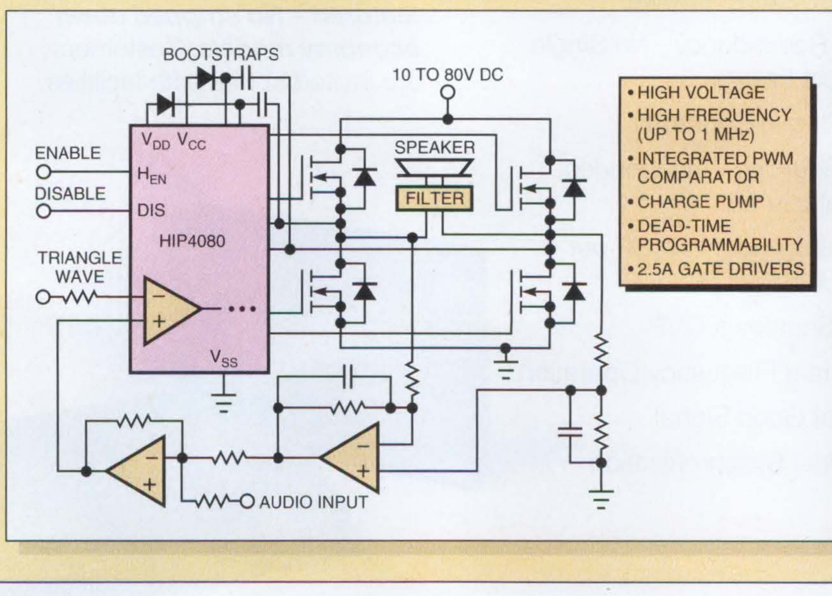
The HIP4080 H-bridge driver handles 80V at 2.5A while switching into a 1000-pF load at 1 MHz. Typical rise and fall times are 10 nsec. Propagation delays are typically in the 50-nsec range. Other features include a 95V-dc bootstrap-supply maximum voltage, and an integrated charge pump/bootstrap to maintain the upper switch-bias supply.

The driver's speed and propagation delays are the biggest factors driving its application in Class D amplifiers. The 1-MHz speed eases the design of the filter, and the 50-nsec propagation delays—difficult to achieve using discretes—reduce factors that cause audio distortion. Miniaturization, efficiency, and a simpler design are also key benefits of the Class D approach. The design is less cumbersome than that of discretes because a bridge-based scheme requires an upper drive, which is difficult to implement with discretes.

Any Class D amplifier requires a control block to perform PWM of the control signal. The performance of the amplifier in the **figure** is analogous to that of a switching power supply. The circuit first modulates the control signal to some high-frequency level and uses this PWM signal to drive the bridge. The filter then strips the PWM carrier from the bridge's output, leaving only the audio signal.

During a 1993 power-application seminar, Harris demonstrated the use of the 4080 in a 70W audio amplifier that fit in a 5.25×3.5-in. pc board. The design required only small heat sinks. The amplifier's efficiency was around 90%.

A promising application of Class D amplifiers is noise cancellation. Harris and Noise Cancellation Technologies (Stamford, CT) are working jointly on ICs similar to the 4080 to implement active-noise-cancellation products for automotive and industrial applications.



presents formidable competition to the all-in-one IC approach. However, the advantages of ICs involve more than just combining circuitry into less space. Integrated power and driver ICs can do things that drivers and discrete transistors often cannot. For example, ICs that integrate the driver and power transistor or transistors can boast all the protection features of discrete transistors, including thermal protection, which discrete transistors can't easily implement. (See **box**, "Integrating temperature sensing and serial communication.")

Thermally protecting a discrete transistor is possible, but it requires additional components. For example, Siemens accomplishes this task with the TempFET line by including a sensor along with the FET in a TO-220 or -218 package. To the user, this extra component is transparent. But, aside from this exception, ICs can add thermal protection without additional components. Implementing these protection features in an IC results in lower circuit overhead and power losses, particularly when the IC is sensing overcurrent conditions.

The ability to indicate to other systems via diagnostic feedback that a fault condition exists is another advantage of ICs. According to Siemens, a

INTEGRATING TEMPERATURE SENSING AND SERIAL COMMUNICATION

One of the biggest advantages of integrating a power switch with control and logic circuitry is that it eases a design's ability to sense temperature and implement a fast shutdown. Although thermistors can sense a power transistor's temperature, integrated ICs offer much shorter delays and can more quickly shut off the overtemperature transistor.

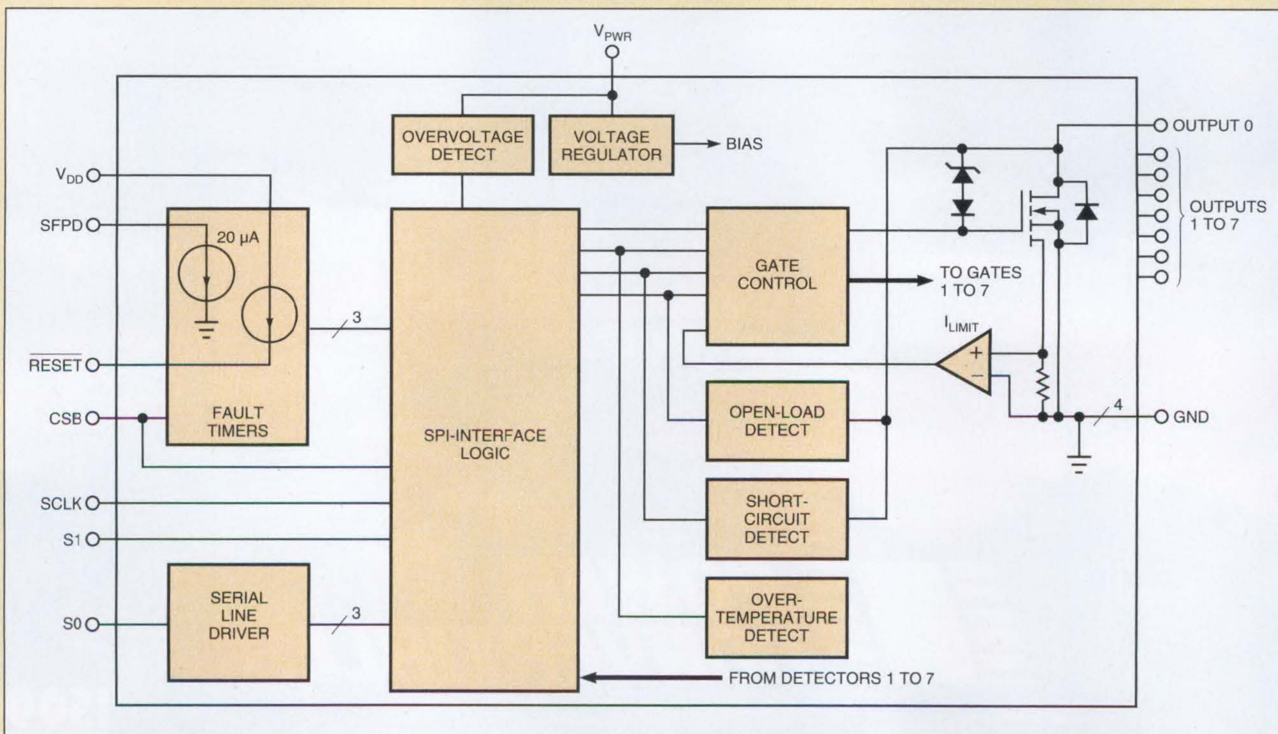
Motorola's MC33298 octal serial switch (OSS) demonstrates this capability along with a high level of integration, including multiple output drivers and a serial interface. This integrated lowside switch also serves as an example of a device that a company conceived, specified, designed, and developed for the automotive industry but that's now available as a standard part.

A key aspect of the IC is that it can sense the temperature and independently implement shutdown of each of the eight channels. Other fault-detection features include open-load detection, overvoltage detection and shutdown, and short-circuit detection and shutdown with one automatic retry per write cycle.

The serial interface exemplifies the diagnostic features available in complex ICs and allows the IC to communicate directly with a microcontroller (μC). You can also daisy-chain four of these switches and use the same four serial lines from the μC to control all 32 outputs.

Key specifications of the device include typical $r_{DS(ON)}$ of 35 mΩ at 25°C and power-supply voltage of 13V. Sleep-mode supply current drops to a maximum of 50 μA (when V_{DD}<2V).

The IC can control inductive loads (with output voltages clamped to 60V) and incandescent loads (with 3 to 6A output currents). The MC33298 costs $5.74 (1500+). It comes in 20-pin DIP and 24-pin SOIC packages.



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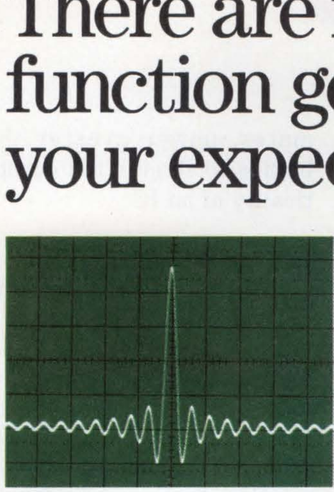

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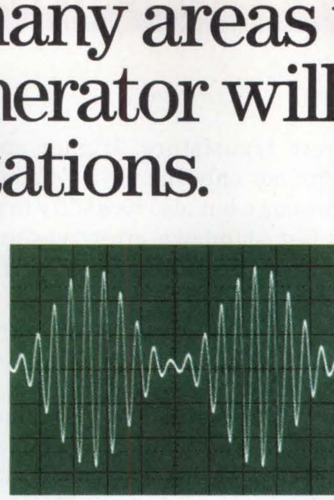

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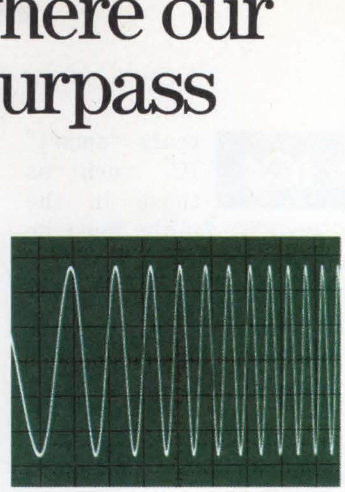

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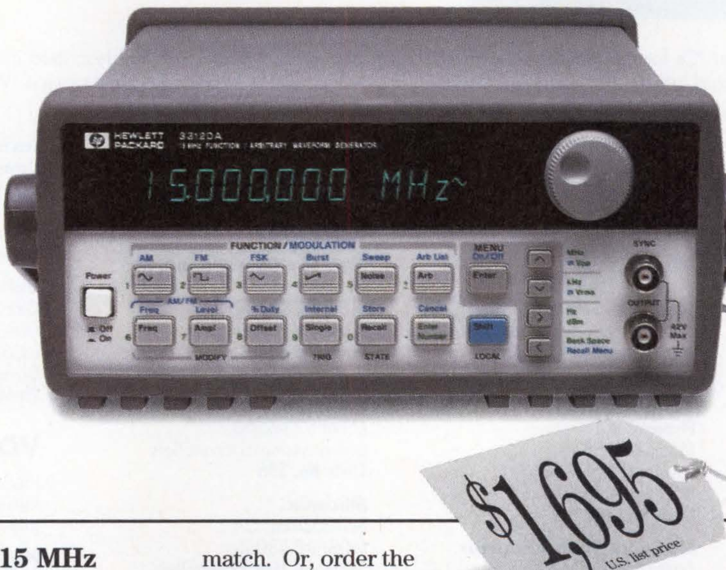

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POWER ICs

truly "smart" IC, such as those in the company's ProFET family, must be able to indicate its status, including short-circuit, undervoltage, and overvoltage conditions. The ProFET family of high-side switches, which now includes 2-channel devices that sell for around $2 (10,000) each, includes diagnostic feedback; CMOS- and TTL-compatible inputs and status outputs; and ESD, overtemperature, overcurrent, and short-circuit protection.

An IC also has a speed advantage because it lacks the parasitics associated with the drive and packaging of discrete transistors. Higher speed benefits not only the device's general performance but also its ability to perform fast shutdown after sensing an overcurrent or overtemperature fault condition.

Ultimately, integrated power devices brush up against limits to usable output power. Handling too much power in an IC becomes uneconomical because of package constraints and excessive dissipation. Just as with the debate of integration itself, packing too much power into an IC eventually gets too expensive because of the larger die sizes such an IC requires. According to some estimates, power greater than 100W begins to stretch the economic practicality of an IC.

Sorting through the costs

Ultimately, determining the appropriate design approach requires emphasizing total system costs and any indirect savings an integrated design may produce. For example, by increasing switching frequencies, ICs can reduce the size and cost of other components. Reducing the number of discrete components may increase a design's reliability and decrease its size and component count. Eventually, you have to compare the cost of the exact

MANUFACTURERS OF POWER ICs

For free information on the power ICs for motion control and switching applications such as those described in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in *EDN*.

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Merrimack, NH
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For more information on the power ICs available from all of the vendors listed in this box, you need only circle one number on the postage-paid reader service card.

Circle No. 363

POWER ICs

functions you need with the extra circuitry necessary to implement them. When control, protection, and feedback circuitry costs start mounting, it makes sense to take a step or two up the integration scale. EDN

Reference

1. Kerridge, Brian, "Intelligent power ICs: Auto applications drive up single chip's IQ," *EDN*, March 17, 1994, pg 27.

Acknowledgment

Thanks to Dean Henderson of Harris Semiconductor, Randy Frank of Motorola, and Arnold Alderman of International Rectifier for useful discussions.

You can reach Technical Editor Anne Swager at (215) 645-0544.

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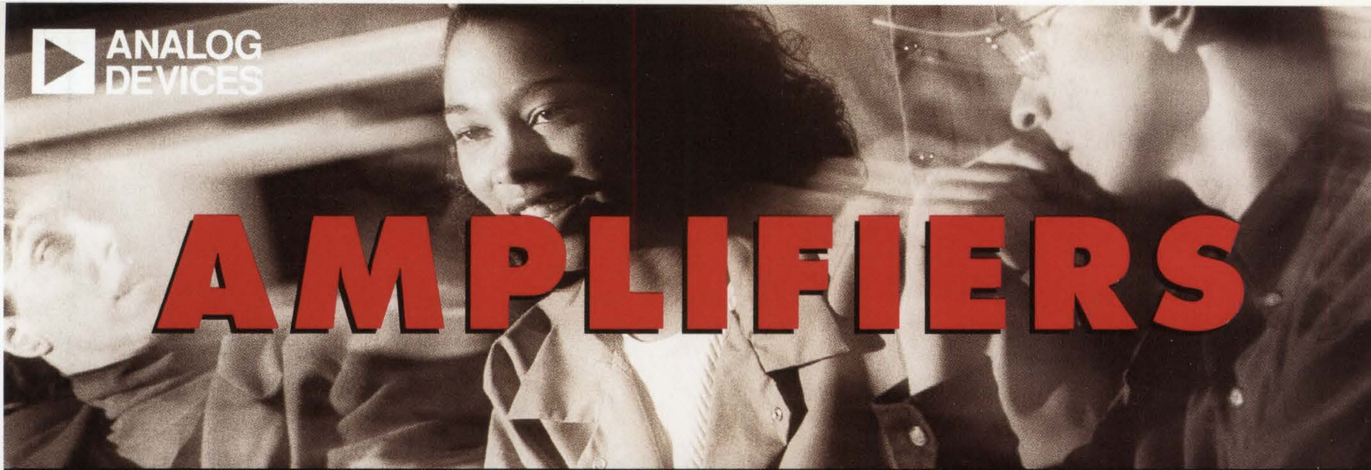
LOOKING AHEAD

Vendors and users are bringing designs down to earth after a decade of thinking the sky's the limit on integration. However, technology doesn't change at an even pace, and highly complex power ICs will no doubt find their way into more and more products.

Companies are working on technology to combine BCD processes to better compete with discrete approaches. For example, Siliconix recently unveiled a line of power MOSFETs that uses a patented vertical-trench structure. If the company could combine such vertical structures with CMOS and bipolar structures (it already has a BCD process), many of the cost and performance tradeoffs between discrete and integrated transistors would disappear. None of these developments happen overnight, however. Work on the trench MOSFET began in 1987.

Another interesting development is SGS Thomson's BCD3 technology, which can integrate EEPROM. In the future, processes that combine programmability with power may provide the necessary design flexibility to tip the scale toward more complex power ICs.

For now, most of the action seems to be in medium-level integration, with an emphasis on keeping costs down and efficiently implementing functions, whether that means using a discrete transistor with protection or using a more complex control IC.



NOBODY DOES AMPLIFIERS LIKE ANALOG DEVICES

IN THIS ISSUE

Whatever your application, ADI has the ideal amplifier for you. And they're available from national distributors and local sales offices nearby. In this issue you'll find our newest amplifiers, with performance and prices to meet the most demanding applications.

High-Speed
High-speed amplifiers for video, high-definition imaging and graphics, office equipment, communications systems, and test and measurement instrumentation.

Precision
From the inventors of the OP-07 come new circuits that combine superior ac/dc specifications, high common-mode rejection, and low gain error.

Single-Supply
If you're designing 3 V or 5 V systems, you need amplifiers specifically designed and tested for low-voltage applications. Choose from the industry's largest selection of true single-supply amplifiers.

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For medical imaging systems or advanced audio equipment, ADI has a low-noise, low-distortion amplifier to fit your needs, at a price you can afford.

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Why build your own instrumentation amplifier when ADI has a full selection ready to go, all with high accuracy and prices to beat discrete designs.

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The industry's best SPICE models covering over 392 devices are yours for the asking. The diskette includes macromodels of amplifiers, references, multipliers, analog switches, and more.

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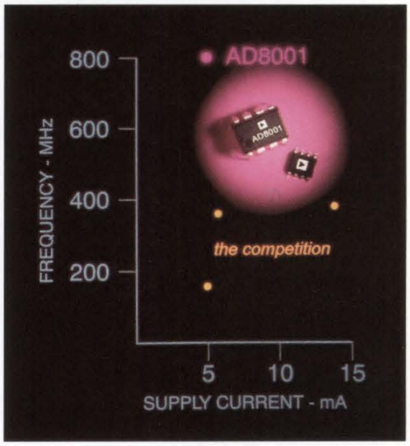
Our team is on your team. For assistance call on our factory or field applications engineers. With over twenty-five years of analog experience, we're here to help. 1-800-ANALOG-D.

LEADERS IN HIGH SPEED

FASTEST AMP ON 50 mW

Introducing the industry's fastest op amp on 50 mW. The new AD8001 800-MHz unity-gain monolithic amplifier uses just 5 mA of supply current. It can process high-speed video signals in HDTV equipment, professional cameras and graphics workstations. Video-specific parameters include 0.1 dB gain flatness to 100 MHz, 0.01% differential gain, 0.025° differential phase (G = +2, R_L = 150 Ω).

Other specifications include 1,200 V/µs slew rate and 10 ns settling of 2 V steps to within 0.1%. A single AD8001 can provide 70 mA of output current and drive up to six back-terminated (75 Ω load) cable lines. Full power bandwidth is 125 MHz with 5 V p-p signal swings. The AD8001's worst harmonic component at 20 MHz is -60 dB, and voltage noise at 10 kHz is only 2 nV/$\sqrt{\text{Hz}}$.



The AD8001 is packaged in an 8-pin plastic DIP or SO-8 and operates from –40°C to +85°C. Military grades will be available with operation from –55°C to +125°C. Prices begin at $2.75 in 1,000s.

CIRCLE 1

LOW-POWER 110-MHz BUFFER RUNS COOL

The 110-MHz BUF04 slews at 3,000 V/µs and consumes only 6.9 mA. At ±5 V, you can reduce power to one-third with full ±15 V performance. Closed-loop design provides low offset and great gain accuracy, and ±10 V signals settle to within 0.1% in 60 ns. Best of all, the BUF04 is packaged in low-profile SO-8 and 8-pin DIPs.

Applications include a/d converter buffering, video cable driving, pulse detection, pro-audio d/a converters, and more. The BUF04 operates from ±5 V to ±15 V supplies over temperatures from –40°C to +125°C.

BUF04 KEY SPECS

Parameter	Min	Typ	Max	Units
GBW		110		MHz
Slew Rate	2,000	3,000		V/µs
Supply Current		6.9	8.5	mA
Voltage Noise Density		4		nV/$\sqrt{\text{Hz}}$
Offset Voltage		0.3	1	mV
Gain Linearity		0.005		%

Prices, from $3.71 in 1,000s.

1 Specifications with ±15 V supply operation

CIRCLE 2

WIDE BAND OP AMPS FOR VIDEO, IMAGING, AND COMMUNICATIONS

These new high-speed op amps provide optimal price/performance in a wide range of video-speed applications. They excel at driving heavy capacitive loads. Some are specified for operation on single +3 V to +5 V supplies, others use common ±5 V and ±15 V dual supplies.

AMPS WITH LOW ΔG/ΔØ

If you need high output drive, try the AD811. It's a high-performance video amplifier with superb video specs to preserve signal fidelity in high-definition TV systems. The AD811 delivers high output drive of 100 mA for efficient line driving. It's specified over a wide power supply range of ±4.5 V to ±18 V and uses just 16.5 mA of power supply current.

Other family members include the AD810 and AD812, ideal for broadcast-quality applications. The AD810 is a low-power version that consumes just 6.8 mA in normal mode, while a DISABLE feature further reduces power to only 2.1 mA. The versatile and low-cost dual AD812, runs on a single +3 V or +5 V supply, or from ±5 V or ±15 V supplies. Package options include 8-pin plastic DIPs, 16- and 20-pin SOICs, 8-pin Cerdips, or 20-pin LCCs.

CIRCLE 3

TRIPLE VIDEO AMP WITH FAST DISABLE

The triple AD813 packs three current-feedback op amps, each with its own independent 80 ns disable function. It offers unprecedented gain flatness for high-quality computer video and broadcast video gear. Operation is from either single +3 V to +5 V, or ±5 V to ±15 V supplies. Supply current is a low 3.5 mA (+3 V) and it delivers 100 MHz of unity gain (–3 dB) bandwidth.

For video muxing, CCD-based equipment, and RGB line driver applications, nothing matches the AD813. It operates from –40°C to +85°C and comes in small 14-pin DIP or narrow body SOIC packages.

CIRCLE 4

LOW-COST, GENERAL-PURPOSE AMPLIFIERS

The AD817 is optimized for applications that require unity-gain stable operation. Its counterpart, the AD818 is tailored for gains of magnitude equal to or greater than +2 or –1. The AD818, with low differential phase and gain errors, is great for video cameras and pro video equipment. As an ADC buffer or line driver, the AD817 excels with its combination of high output current and unlimited capacitive load drive.

CIRCLE 5

HIGH-SPEED FET-INPUT

The AD843 and AD845 FET-input op amps combine excellent ac and dc performance with low power consumption. The dc performance of these unity-gain stable op amps is perfect for high-speed data acquisition systems. Their low input bias current and offset voltage can reduce errors in high-speed active filters, integrators, peak detectors, and current-to-voltage converter circuits.

Dynamic performance is equally impressive. They have low total harmonic distortion for high-speed sample/hold circuits, ADCs, and DSP front-end circuits. They also have industry-standard pinouts and can upgrade system performance. Both op amps operate from ±15 volt supplies with five performance grades specified over commercial, extended, and military temperature ranges.

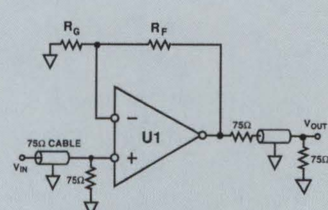
CIRCLE 6

VIDEO LINE DRIVING MADE EASIER

The figure below depicts a video line driver circuit and provides a list of recommended products with associated resistor values. When using a current feedback op amp for U1, closed-loop bandwidth largely depends on the value of the feedback resistor R_F.

Attenuation of the circuit's open-loop response, especially when driving a load value <250 Ω, will also affect its bandwidth. Gain resistance (R_G) is typically set for stable operation at G = 2. Low values of R_G and R_F will minimize the circuit's feedback time constant and nonlinear behavior. The use of 1% metal-film resistors ensures the widest possible 0.1 dB bandwidth. To achieve even wider bandwidths, you can reduce the magnitude of R_F, but you run the risk of increasing signal peaking. Use maximum supply voltages and limit amplifier loads to minimize signal distortion.

With the exception of the AD8001, which operates from ±5 V supplies, the products in the chart below are characterized with ±15 V supplies. Bandwidth is a measure of gain flatness at 0.1 dB.



MODEL	0.1dB BW (MHz)	ΔG (%)	Δϕ (°)	RF/RG (Ω)
AD8001	110	0.01	0.025	750
AD811	35	0.01	0.01	649
AD812	40	0.05	0.02	715
AD813	50	0.03	0.06	681
AD818	55	0.005	0.045	1,000

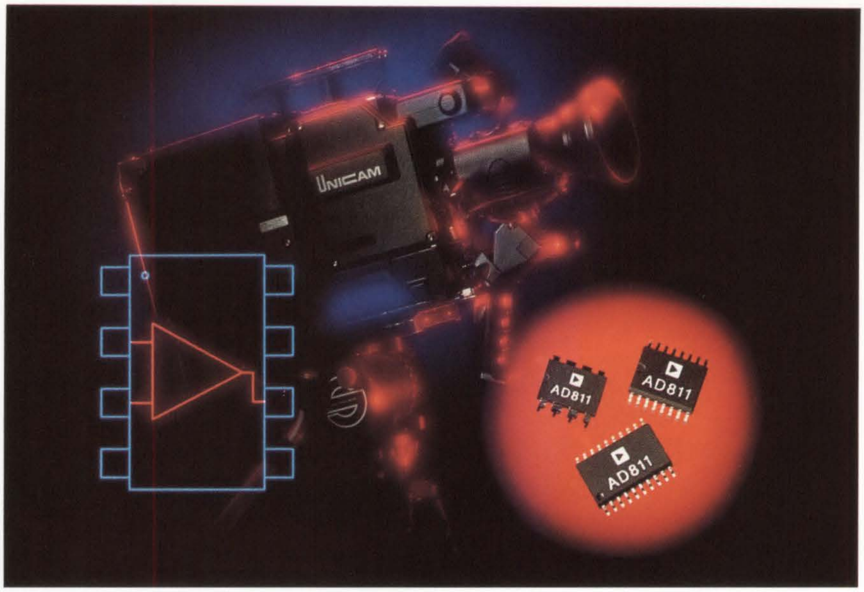
HIGH SPEED QUAD WITH PRECISION

The OP467, with four fast op amps in one package, has the fastest slew rate (170 V/µs) and settling time (≤200 ns to 0.01%) among quads. In multichannel systems, it can save space, reduce power and cost, and increase reliability. It's unity-gain stable and can drive high-capacitance loads up to 1,600 pF.

Besides its speed, it offers a low 200 µV offset. Use the OP467 in high-speed instrumentation and test equipment, high-speed detectors, laser scanners, sonar arrays, and other applications that need speed, accuracy, and a wide ±5 to ±15 V operating range. It's housed in 14-pin plastic DIP, cerdip, 16-lead SOL, and 20-contact LCC surface-mount packages. CIRCLE 7

IMPROVED EL2020

The ADEL2020, a superior second source, will improve performance with less power drain and lower cost. Low differential gain and phase errors make it ideal for low-power video applications. The ADEL2020 is available in either plastic DIP or SOIC packages specified over the -40°C to +85°C industrial temperature range. CIRCLE 8

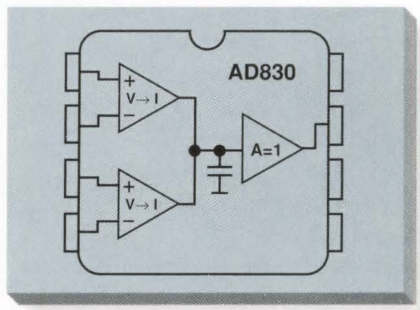


AN AMPLIFIER WITH A DIFFERENCE

The AD830 wideband amplifier rejects high-frequency common-mode voltage noise in differential line receiver applications. It handles differential signals, system grounds, and low-distortion high-frequency amplification. With >±50 mA full-output-current drive, it's useful for driving heavy loads. And its output clamping is great for driving ADCs.

Other benefits include balanced impedance inputs, symmetrical circuit behavior for gain of either +1 or –1, and low sensitivity to source resistance.

The AD830 uses ±15 V and ±5 V supplies, but its special offsetting capability allows it to perform with single supplies from +10 to +30 V. Packages include 8-pin plastic miniDIP, cerdip, and SOIC. CIRCLE 9



MODEL	AD810	AD811	AD812	AD813	AD817	AD818	AD843	AD845	OP467	AD830	UNITS
Channels	Single	Single	Dual	Triple	Single	Single	Single	Single	Quad	Single	
Supply Voltages	±5, ±15	±5, ±15	+3 to ±15	+3 to ±15	+5 to ±15	+5 to ±15	±15	±15	±5, ±15	±5, ±15	Volts
Feedback	Current	Current	Current	Current	Voltage	Voltage	Voltage	Voltage	Voltage	Voltage	
BW, 0.1 dB (G=+2)	30	35	40	50	16	55	—	—	—	15	MHz
BW, -3 dB (G=+1)	80	140	145	125	50	130 (+2)	34	16	28	100	MHz
Slew Rate	1,000	2,500	1,600	450	350	500	250	100	170	530	V/µs
Settling Time (0.01%)	125	65	40 (0.1%)	40 (0.1%)	70	80	135	350	200	35 (0.1%)	ns
ΔGain Error	0.02	0.01	0.02	0.03	0.04	0.005	0.025	0.04	—	0.05	%
ΔPhase Error	0.04	0.01	0.02	0.06	0.08	0.045	0.025	0.02	—	0.08	°
V_n (10 kHz)	2.9 (1 kHz)	1.9 (1 kHz)	3.5	3.5	15	10	19	18	6 (1 kHz)	27	nV/√Hz
Max V_{OS}	6	3	5	5	2	2	2	1.5	0.5	±3	mV
Min Output Current	40	100 (typ)	40	50	50	50	50	50 (typ)	50 (typ)	±50	mA
Max Supply Current	8	18	5.5	5.5	7.5	7.5	13	12	10	14.5	mA
Prices in 1,000s	$2.08	$2.85	$2.48	$3.74	$1.52	$1.69	$3.70	$2.76	$4.86	$2.42	USD
	CIRCLE 3	CIRCLE 3	CIRCLE 3	CIRCLE 4	CIRCLE 5	CIRCLE 5	CIRCLE 6	CIRCLE 6	CIRCLE 7	CIRCLE 9	

1.800.262.5643

LOW-POWER PRECISION FAMILY

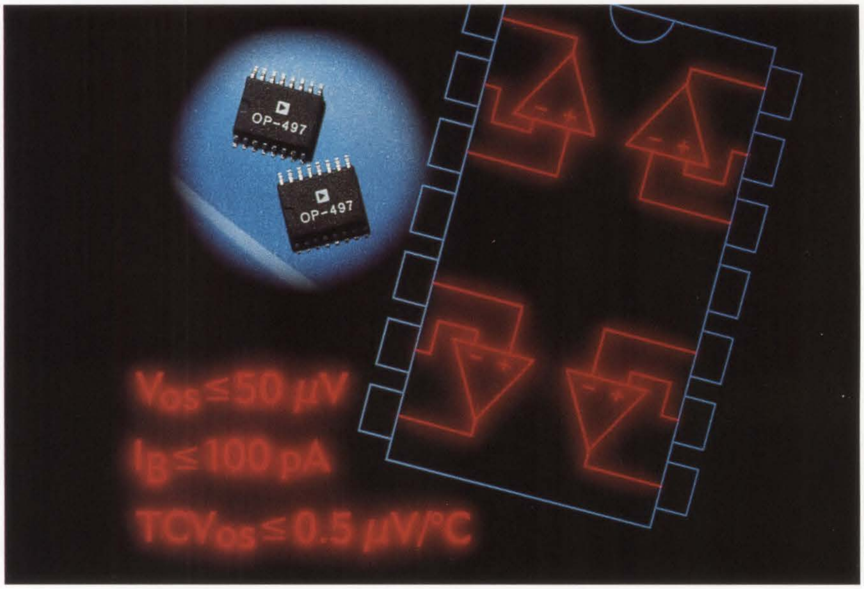
When your design demands precision and low power, nothing beats the OP97 family. The OP97 (single) OP297 (dual) and OP497 (quad) are great for designs that need very low bias currents.

The OP97 family is ideal for sample-and-hold circuits, peak detectors, and logarithmic amplifier designs that exhibit low leakage current. Thermocouples, strain gages and other industrial equipment need the OP97's accuracy over wide temperature ranges. Unlike conventional FET-input op amps, these ICs use a unique current cancellation circuit to keep bias current low over the entire temperature range.

The family combines low power consumption with guaranteed accuracy. Maximum voltage offset at 25°C is only 50 µV (with only 0.5 µV/°C drift) and bias current is 100 pA. Minimum open-loop gain is 2 kV/mV. Combined, these specs can eliminate the need for offset trims and additional gain stages.

Battery and low-powered systems will benefit from the OP97 family's low supply current: 625 µA (max) per channel. Wide supply voltages range from ±2 V to ±20 V. Packaging options include 8- and 14-pin DIPs and cerdips, 8- and 16-pin SOICs, and 20-contact LCCs.

CIRCLE 10



WHAT'S BETTER THAN THE OP-07?

The OP177 is today's industry standard for ultrahigh precision. Maximum offset voltage is only 10 µV, with less than 0.1 µV/°C V_{OS} drift, eliminating external V_{OS} trimming and increasing system accuracy over temperature. Other guaranteed specifications include minimum 130 dB CMRR and 120 dB PSRR.

This low-noise, bipolar-input op amp is a good alternative to chopper-stabilized amplifiers. The OP177 provides chopper-type performance without high noise, low frequency chopper spikes, external capacitors, and limiting common-mode input voltage range. The OP177 is available in 8-pin plastic, cerdip and SO-8 packages. Cerdip and 20-lead LCC devices are guaranteed over extended and military temperature ranges.

CIRCLE 11

DUALS AND QUADS TOO

The dual OP200 and quad OP400 offer great performance over temperature and use very little power. For example, the OP200's input offset voltage is typically 25 µV with only 0.2 µV/°C drift from –55°C to +125°C. Its supply current (per amplifier) is a scant 570 µA. Industry standard DIP, SOL and LCC packages are available.

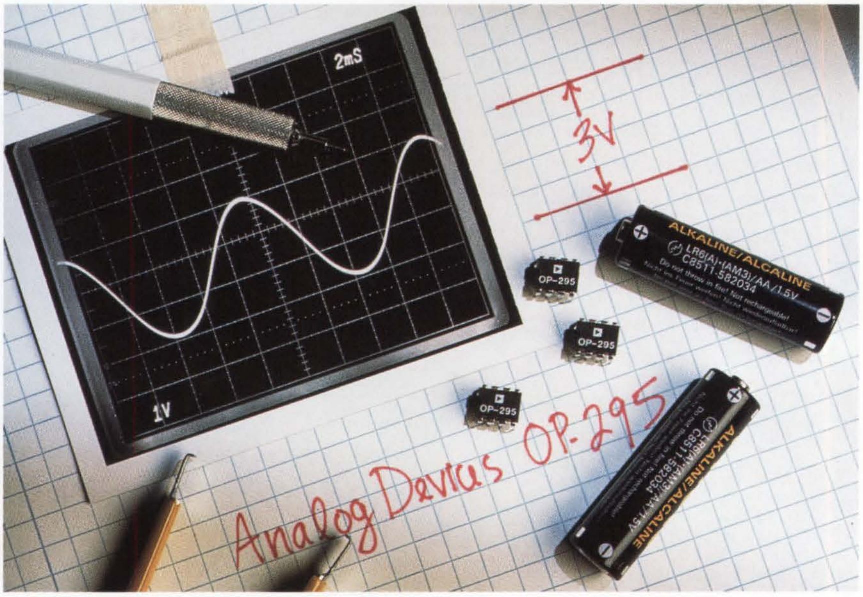
CIRCLE 12

MODEL	OP97	OP297	OP497	OP177	OP200	OP400	UNITS
Channels	Single	Dual	Quad	Single	Dual	Quad	
Offset Voltage (V_{OS})	25	50	50	10	75	150	µV, max
V_{OS} Drift	0.6	0.6	0.5	0.1	0.5	1.2	µV/°C, max
Offset Current (I_{OS})	0.1	0.1	0.1	1	1	1	nA, max
Input Bias Current	±0.1	±0.1	0.1	1.5	2	3	nA, max
Voltage Noise @ 1kHz	14	17	15	(118)	11	18	$nV/\sqrt{Hz}$ (nV_{RMS})
Current Noise	20	20	20	(8)	400	600	$fA/\sqrt{Hz}$ (pA_{RMS})
CMRR	132	120	120	130	120	120	dB, min
PSRR	132	120	120	120	-	-	dB, min
Input Voltage Range	±14	±14	±14	±13.5	±13	±13	V
Bandwidth (G=+1)	900	500	500	600	500	500	kHz
Supply Current	600	625	625	2,000	725	725	µA, max
Prices in 1,000s	$1.00	$2.50	$4.04	$0.95	$2.48	$4.50	USD
	CIRCLE 10	CIRCLE 10	CIRCLE 10	CIRCLE 11	CIRCLE 12	CIRCLE 12	

FOR INFORMATION

SINGLE-SUPPLY AMPLIFIERS DELIVER TOP PERFORMANCE AT LOW COST. INDUSTRY'S BROADEST PRODUCT LINE

Nobody has a broader product portfolio of single-supply amplifiers for low-power and battery-powered gear. These are just a few of the products we've recently introduced.



LOW-COST DUALS AND QUADS OUTPERFORM CMOS AMPS

The dual OP292 and quad OP492 single-supply op amps are low in cost and outperform comparably priced CMOS devices. These 4 MHz, 4 V/µs amplifiers combine the qualities of complementary bipolar—low noise, precision and output drive capability —with the low cost of CMOS devices. With +5 V supplies, the OP292 guarantees 2.4 mV maximum (500 µV typ) offset over our new HOT temperature range (–40°C to +125°C), at no additional cost.

Unlike competitive ICs, the inputs of these amplifiers can swing well below ground with output swings to ground. The OP292 and OP492 draw less than 1.4 mA per channel, excellent for multichannel battery-powered applications. Both amps feature low voltage and current noise: 15 nV/$\sqrt{\text{Hz}}$ and 0.7 pA/$\sqrt{\text{Hz}}$, and channel separation (at 1 kHz) is 100 dB.

Applications that can take advantage of the OP292 and OP492 include disk drives, mobile phones, multichannel industrial and servo control systems, modems, fax machines, pagers, and power supply monitoring circuits. Packaging options include 8- and 14-pin plastic DIPs or surface-mount narrow-body SOICs. USD prices for the OP292 and OP492 start at $1.32 and $2.16, respectively.

CIRCLE 13

3-V TO 30-V RAIL-TO-RAIL

The dual OP295 and quad OP495 3-V single-supply op amps are the industry's highest accuracy, lowest power true rail-to-rail amplifiers. Their low 30 µV offset, combined with a high gain of 1,000 V/mV, makes them ideal for portable instrumentation. On a 3 V supply, they drive a 10 kΩ load from 2.90 V to within only 2 mV of ground—perfect for process and motor control circuitry.

For driving coax cable, large FETs, or other capacitive loads, the OP295 and OP495 offer stability with loads up to 300 pF. They can supply over ±25 mA to the load on ±15V supplies (±18 mA at +5 V), with a typical gain-bandwidth product of 75 kHz.

The OP295 uses less power than CMOS chips, gives exceptionally low voltage offset drift (typically 1 µV/°C), and requires only 50% of the quiescent current of the closest competitive product.

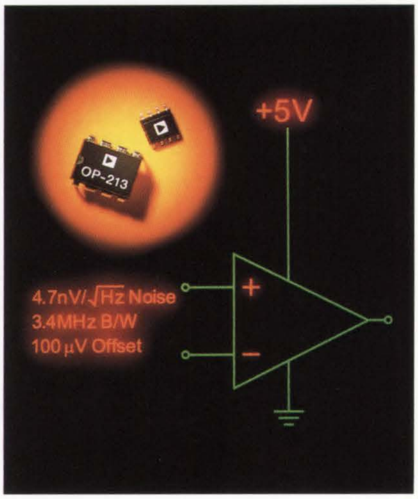
The OP295 and OP495 are specified from -40°C to +125°C and packaged in plastic DIPs and SOICs. Die are also available. USD prices in 1,000s begin at $1.98 and $3.56, respectively.

CIRCLE 14

HIGH PRECISION AT +5 V

The OP113, OP213 and OP413 are single, dual and quad single-supply precision amplifiers. Operating from +5 V to ±15 V, these op amps feature low noise (4.7 nV$\sqrt{\text{Hz}}$),3.5 MHz bandwidth, 75 µV offset voltage, and drift of just 0.2 µV/°C. Applications include automotive, process control, portable instruments, and pressure/strain gages. Packaging options range from 8-lead SOIC and plastic DIP to 16-lead SOL packages. USD prices in 1,000s begin at $1.47 (single), $2.21 (dual) and $4.92 (quad).

CIRCLE 15

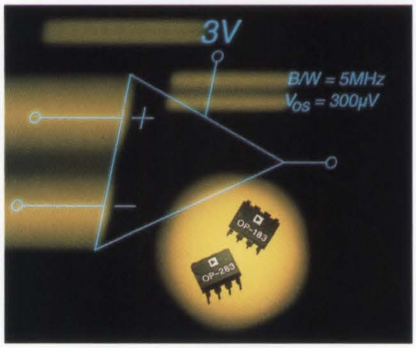


1.800.262.5643

SINGLE-SUPPLY FET

The AD820 (single) and AD822 (dual) are precision, low-power, FET-input op amps that operate from a single +3 to +36 V range, or with dual supplies from ±1.5 to ±18 V. Their outputs swing from rail to rail (within 10 mV) and their inputs can swing 0.2 V below ground. The JFET input stage maintains low bias current (≤10 pA at 25°C, B grade), with offsets as low as 900 µV max over temperature (–40°C to +85°C) and 25 nV/√Hz noise at 10 Hz.

Though the quiescent current drain is only 620 µA, both the AD820 and AD822 will drive loads of up to 15 mA and 350 pF. They both have a unity gain bandwidth of 1.8 MHz and 3 V/µs slew rate. A 3-volt version is optimized for low-power operation from –40°C to +85°C at no extra cost. The AD820 and AD822 are available in 8-pin plastic DIPs and SOICs.
CIRCLE 16



INDUSTRY'S FASTEST 3 V SINGLE-SUPPLY AMP

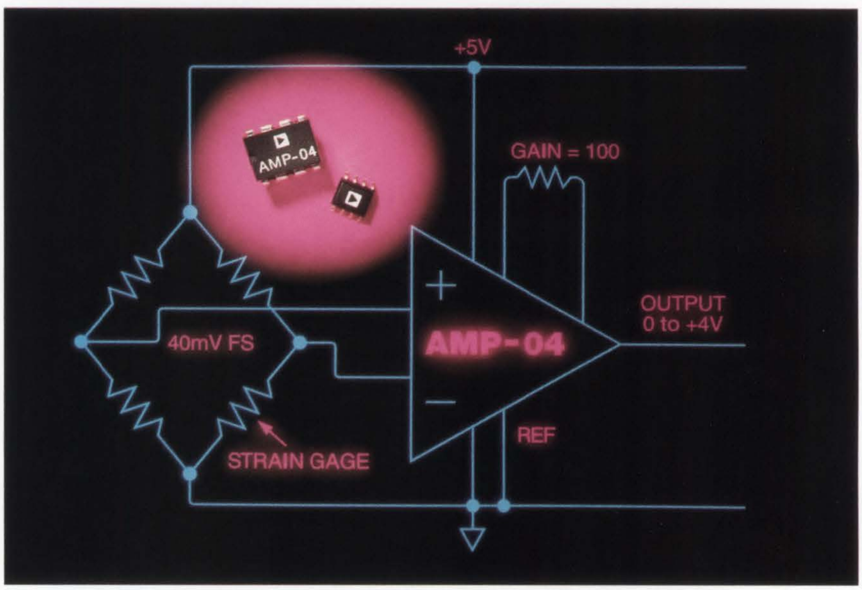
If your 3 V system needs a gain bandwidth product greater than 1 MHz, select the OP183 or OP283. They combine 5 MHz bandwidth with low noise for use in low voltage applications, such as ADC buffering, filtering, servo control and audio for portable computers.

These two amps are thoroughly specified for +3 V, +5 V and ±15 V supply operation. Unlike competing 3 V devices that specify only typical performance characteristics, the OP183 and OP283 guarantee low offset, high gain, and input and output ranges that include ground. Noise is typically a low 10 nV/√Hz, and both amplifiers can sink and source 25 mA—even with a 3 V supply.

Both devices are specified from –40°C to +85°C and are available in 8-lead plastic DIPs and SO-8 packages. Prices for the OP183 and OP283 (in 1,000s): $1.42 and $2.15, respectively.
CIRCLE 17

SINGLE-SUPPLY INSTRUMENTATION AMPLIFIERS FEATURE SINGLE-SUPPLY, HIGH ACCURACY, LOW COST

When accuracy, space and cost are your concern, one of these three in-amps will provide the lowest cost solution—especially when compared with the time to design and implement an equivalent circuit.

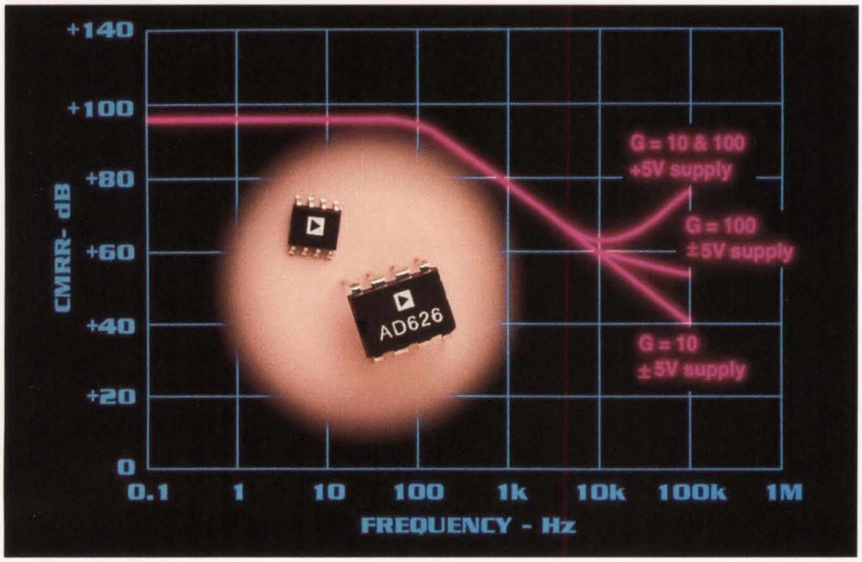


SINGLE SUPPLY IN-AMP

Specified for operation from +5 to ±15 volts, the AMP04 precision in-amp packs accuracy in a small SO-8 footprint for those difficult single-supply designs. The AMP04 can eliminate the need for a separate gain stage to isolate low-level differential signals from high-level common-mode signals. Gain is easily programmable from 1 to 1,000 with a single resistor.

The AMP04 has an input offset current of 1 nA for direct connection to strain gages and high-impedance transducers. Guaranteed max specs include 3 µV/°C offset drift, 150 µV offset voltage, and 0.005% gain nonlinearity, while requiring only 700 µA of supply current. A unique feature of the AMP04 is that it doesn't exhibit common-mode swing limiting at high gain, unlike "triple-amp" designs (see sidebar).

The AMP04 precision in-amp is specified for operation from -40°C to +85°C. Package options include an 8-pin plastic DIP, 8-pin SOIC, or 8-pin cerdip. USD prices (in 1,000s) begin at $4.55. CIRCLE 18



LOW-COST IN-AMP REPLACES DISCRETE DESIGNS

The AD620 high-accuracy in-amp replaces discrete designs with less overall error, lower power use, and reduced board space. It allows for gains from 1 to 1,000 set by a single external resistor. Noise is low (0.28 µV p-p, 0.1 to 10 Hz and 9 nV/$\sqrt{\text{Hz}}$ at 1 kHz); bandwidth is 120 kHz (G = 100). With guaranteed-maximum 50 µV voltage offset, 0.6 µV/°C drift, 1 nA input bias current, and 40 ppm nonlinearity—and minimum 93 dB CMR (G = 10)—it's ideal for weigh scales, transducer interfaces and ECG circuits. The supply range is a wide ±2.3 V to ±18 V, at 1.3 mA (maximum). Prices in 1,000s begin at \$3.27 USD.

CIRCLE 19

SINGLE-SUPPLY DIFFERENTIAL AMP

The AD626 is a single-supply, low-power differential amplifier with on-chip gains of 10 and 100 V/V (externally set). Its supply range is +2.4 to +10 V single, ±1.2 to ±6 V dual, drawing less than 290 µA of current. Uses include current sensing and sensor interfacing, especially in battery and portable applications. Its common mode range, 6 (V_S – 1 V), exceeds the supply; for +5 volt supply, CMR = 90 dB and the output range is +30 V to +4.7 V (minimum). Its inputs are overload protected (50 V continuous), and the internal attenuation network includes RFI filters. Prices (1,000s) start at \$2.85 USD.

CIRCLE 20

EXTEND COMMON-MODE SWING LIMITATIONS AT HIGH GAIN

In traditional three op amp in-amp designs, common-mode voltage (CMV) range is limited at high gain. For example, the in-amp circuit below (Figure A) is designed for a gain of 1001 with a CMV of 10 volts, but there's a problem. Amplifier B must swing to 15.01 volts in order for the circuit's output to swing to 10.01 volts. Operating from a +15 V supply, an op amp cannot handle this swing range. The output will saturate before reaching the supply rails.

The single-chip AMP04 in Figure B, operating at the same common-mode conditions, does not exhibit this limitation. None of its internal nodes reach signal levels that are high enough to cause amplifier saturation. In addition, the AMP04 maintains a gain accuracy of 0.5%, provides high input impedance (4 x 10^9), and features 105 dB of CMRR at a gain of 1,000.

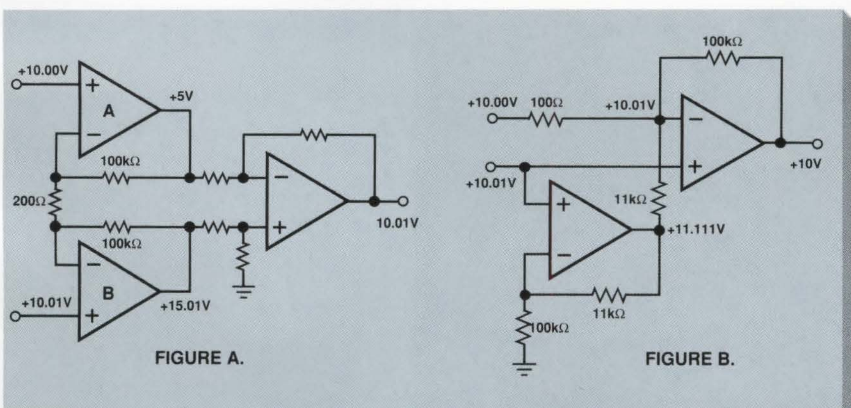
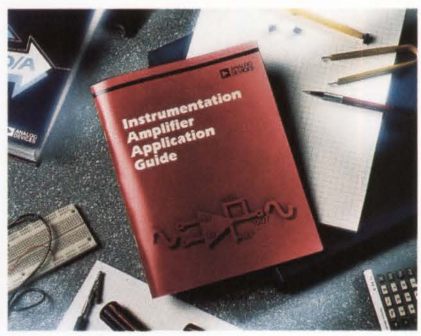


FIGURE A. FIGURE B.



Instrumentation Amplifier Guide

CIRCLE 21

The AD797 features the industry's lowest voltage noise and distortion. It's an excellent choice for use in audio preamplifiers, FFT and spectrum analyzers, and IR and ultrasound imaging: $V_n = 0.9\ nV/\sqrt{Hz}$ and remains flat over the full 8 MHz bandwidth (Gain = 10) at 1 kHz. Total harmonic distortion is -120 dB at 20 kHz. Settling time is 800 ns to 16-bit accuracy.

Many dc specifications are guaranteed, including a maximum 60 µV voltage offset with 0.6 µV/°C drift, 300 nA (200 nA typical) input offset current, and 2 µA input bias current. The AD797 features a fast 20 V/µs slew rate and a gain-bandwidth product of 110 MHz (Gain = 1,000). Full-power bandwidth is 280 kHz at 20 Vp-p. Output current drive is typically 50 mA, permitting the use of low-value gain-setting resistors to curb resistor noise.

AD797 operates from ±5 to ±15 V supplies over the -40°C to +85°C industrial and -55°C to +125°C military temperature ranges. Packages include 8-pin plastic DIP, SOIC and cerdip. Prices start at $3.36 (1,000s).

CIRCLE 22

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The OP275 features 0.0006% total harmonic distortion plus noise and $6\ nV/\sqrt{Hz}$ voltage noise density. Input offset voltage is guaranteed at <1 mV allowing the OP275 to be used in dc coupled or summing applications without adding noisy offset adjustment circuitry. Dynamic characteristics include 22 V/µs slew rate and 9 MHz gain-bandwidth product. In addition, the OP275 uses less than 5 mA of supply current, even with ±22 volt supplies.

For professional audio console designs, the small SO-8 package combined with the low power can save many square inches of board space and many watts of power, resulting in cooler operation and greater density.

Its companion, the OP176 has the same attributes with greater output swing and output short-circuit protection, at much lower power than NE5534, plus it's stable at unity gain.

Both the OP176 and OP275 are specified over the -40°C to +85°C extended industrial temperature range and are available in 8-pin plastic DIP or SOIC packages. The SOIC package is offered in 2,500 piece spools for high volume handling. Prices for the OP176 and OP275 begin at $.88 and $1.08, respectively in 1,000s.

CIRCLE 23

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THD + N	(98)	0.001	0.0006	(dB) %
Offset Voltage	0.8	1	1	mV, max
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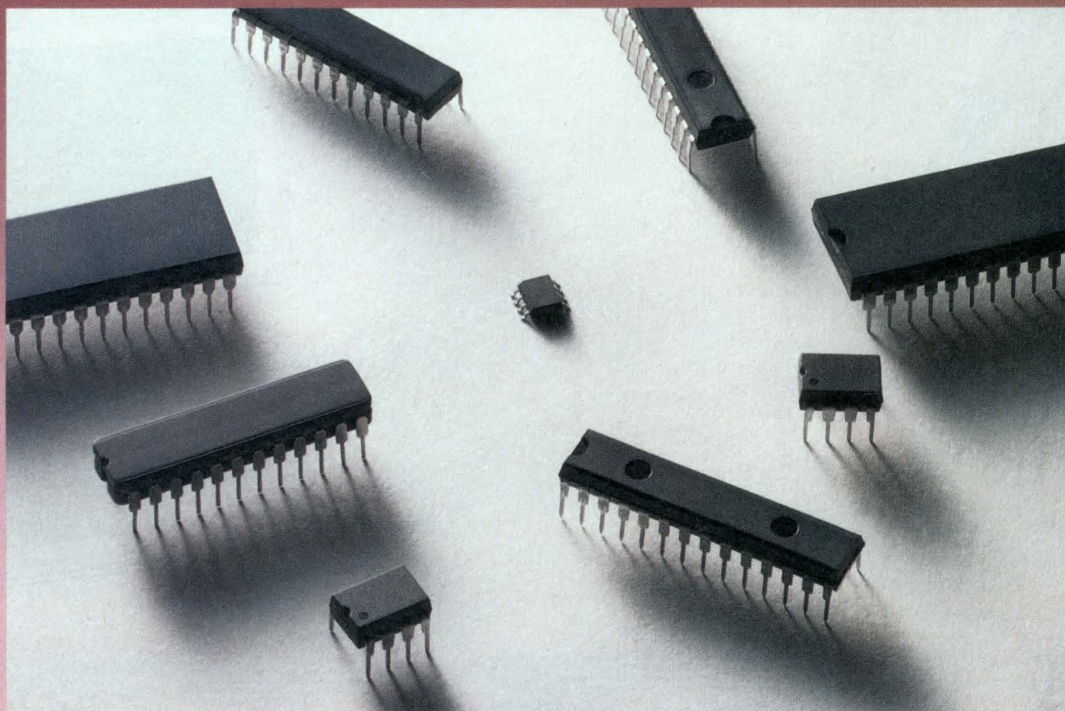

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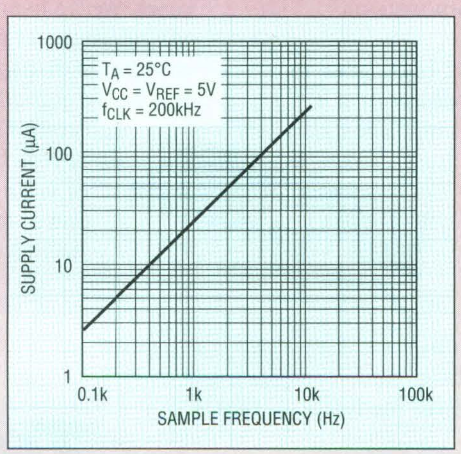

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CIRCLE NO. 190

Biasing corrects position-sensing photodiode

Yishay Netzer, Consultant, Yuvalim, Israel

..An integrator powers the light source in **Fig 1**'s position-sensing circuit, eliminating errors arising from variations in the source's intensity. This circuit's accuracy is essentially that of the sensor itself, beating designs that use a more complex analog divider.

Amplifiers IC_{1A} and IC_{1B} convert the two detector currents from D_1, a photosensitive strip, into voltages in the conventional manner. IC_{2B} subtracts these two voltages to derive the output signal V_O. V_O is proportional to the position of the spot cast by the light source upon D_1.

IC_{2A} integrates these two voltages along with a current from a regulated 5V source, driving the light source via Q_1. This closed-loop scheme supplies illumination proportional to the sum of the two input currents, providing a fixed-scale factor for the signals supplied to the difference amplifier, IC_{2B}. Using a monolithic resistor network for all the 10-kΩ resistors in the circuit enhances temperature stability. (DI #1452)

EDN

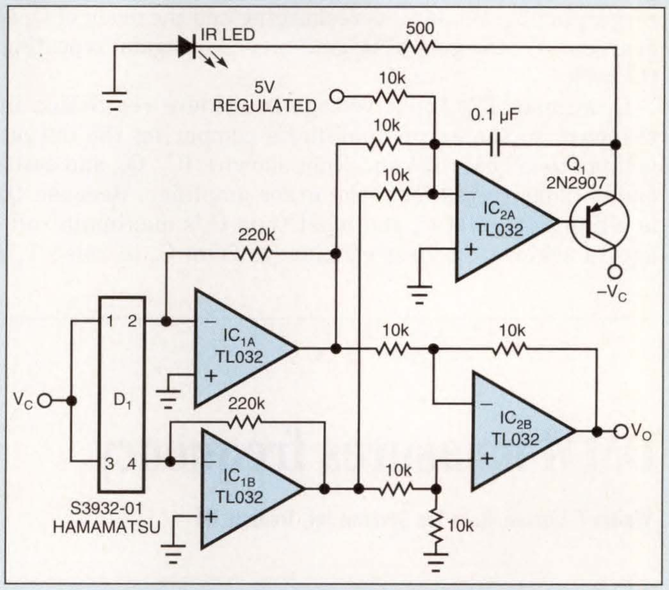

Fig 1—A closed-loop integrator powers the light source of this position-sensing circuit, providing a fixed-scale factor for the signals supplied to the circuit's difference amplifier.

To Vote For This Design, Circle No. 328

Clean switcher powers 16-bit A/D converters

Patrick Kevin Garner, Advanced Technology Systems, McLean, VA

The low-noise switcher in **Fig 1** works much like a TV's horizontal-deflection circuit to provide clean power for a 16-bit A/D converter.

In operation, Q_3 is a logic-level gate-drive MOSFET driven by the same 100-kHz square wave that clocks the A/D converter. When Q_3 turns off, the primary of T_1 resonates with C_3 and flies back to 25V. Energy then transfers to the transformer's secondary. When the flyback voltage attempts to go

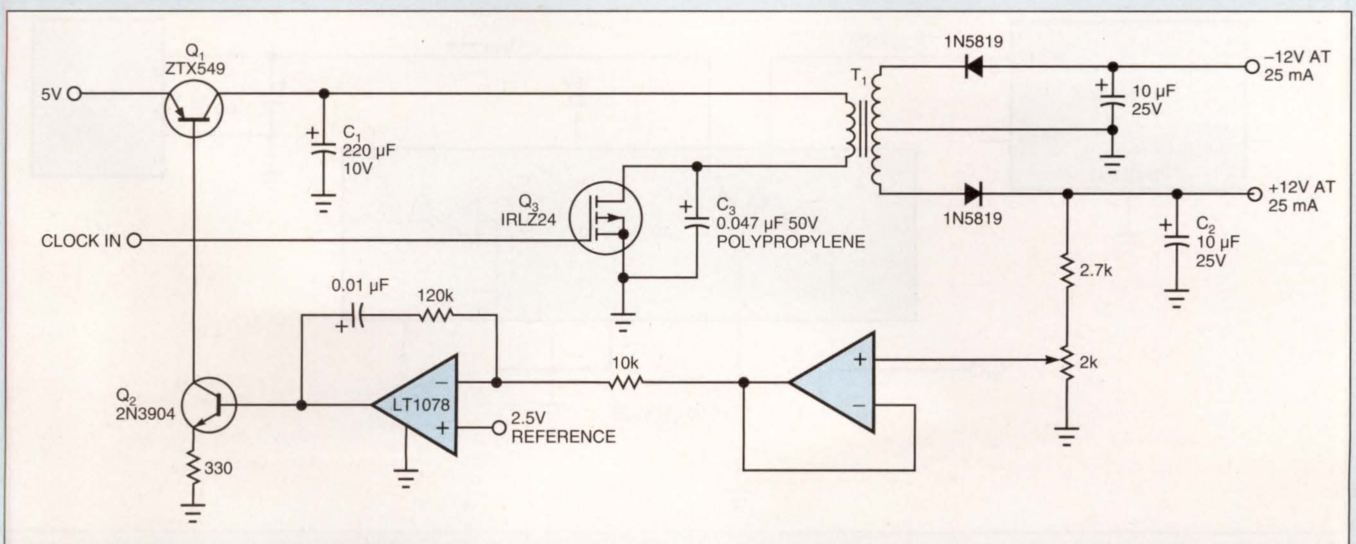

Fig 1—This resonant switcher provides clean power for high-resolution A/D converters.

below ground, the integral body diode of the power MOSFET Q_3 clamps the flyback voltage, causing excess resonant energy in the transformer to flow back through its primary, recharging C_1. While C_1 is recharging and the drain of Q_3 is nearly at 0V, the gate of Q_3 gets turned on again, repeating the cycle.

Q_1 adjusts T_1's input voltage to achieve regulation in response to the error amplifier's comparing the output voltage to a 2.5V reference (not shown). IC_1, Q_2, and associated components form the error amplifier. Because Q_1 is a linear regulator, you must trim C_3's maximum voltage to achieve the best efficiency. Trim C_3 to raise T_1's input voltage to above 4V. At 4.5V, 70% efficiency is possible.

T_1's construction is not critical. The primary consists of seven turns of 24 AWG, and the secondary has 12 turns of 24 AWG with the ground tap at six turns. The core is a Philips E187 3C85, and the gap in the outer legs of the core measures 2 mils. The primary's inductance should be around 12 μH. C_3 must be a high-quality, low-inductance electrolytic, suitable for switching supplies. (DI #1451) EDN

To Vote For This Design, Circle No. 329

DMM measures frequency

Walter P Sjursen, Base Ten Systems Inc, Trenton, NJ

The circuit in **Fig 1** uses two ICs, a few passive components, and a standard DMM to measure frequency. In the circuit, a switched-capacitor network, analog switch IC_2 and capacitor C_1, simulates a frequency-dependent resistor.

The network's resistance is the inverse of the input frequecy, f_{IN}, multiplied by C_1's value. If the circuit applies a constant voltage (V_{REF}) across the frequency-dependent resistor, then the current through the resistor is directly proportional to the frequency.

TABLE 1—CONVENIENT C_1 VALUES

Frequency range (kHz)	**C1** (μF)
0 to 0.1	1
0 to 1	0.1
0 to 10	0.01
0 to 100	0.001

IC_1 supplies this 10V reference voltage. Capacitor C_2 is a lowpass filter and should be much larger than C_1. **Table 1** contains values for C_1 that provide convenient scale factors. (DI #1448) EDN

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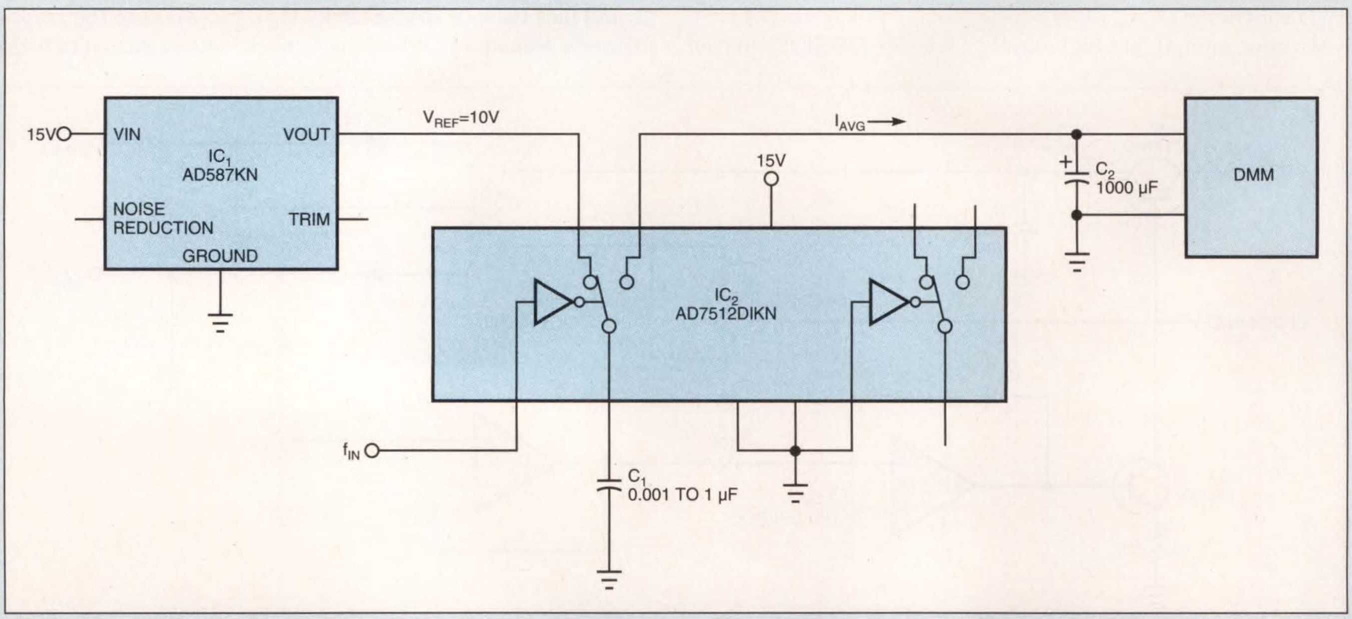
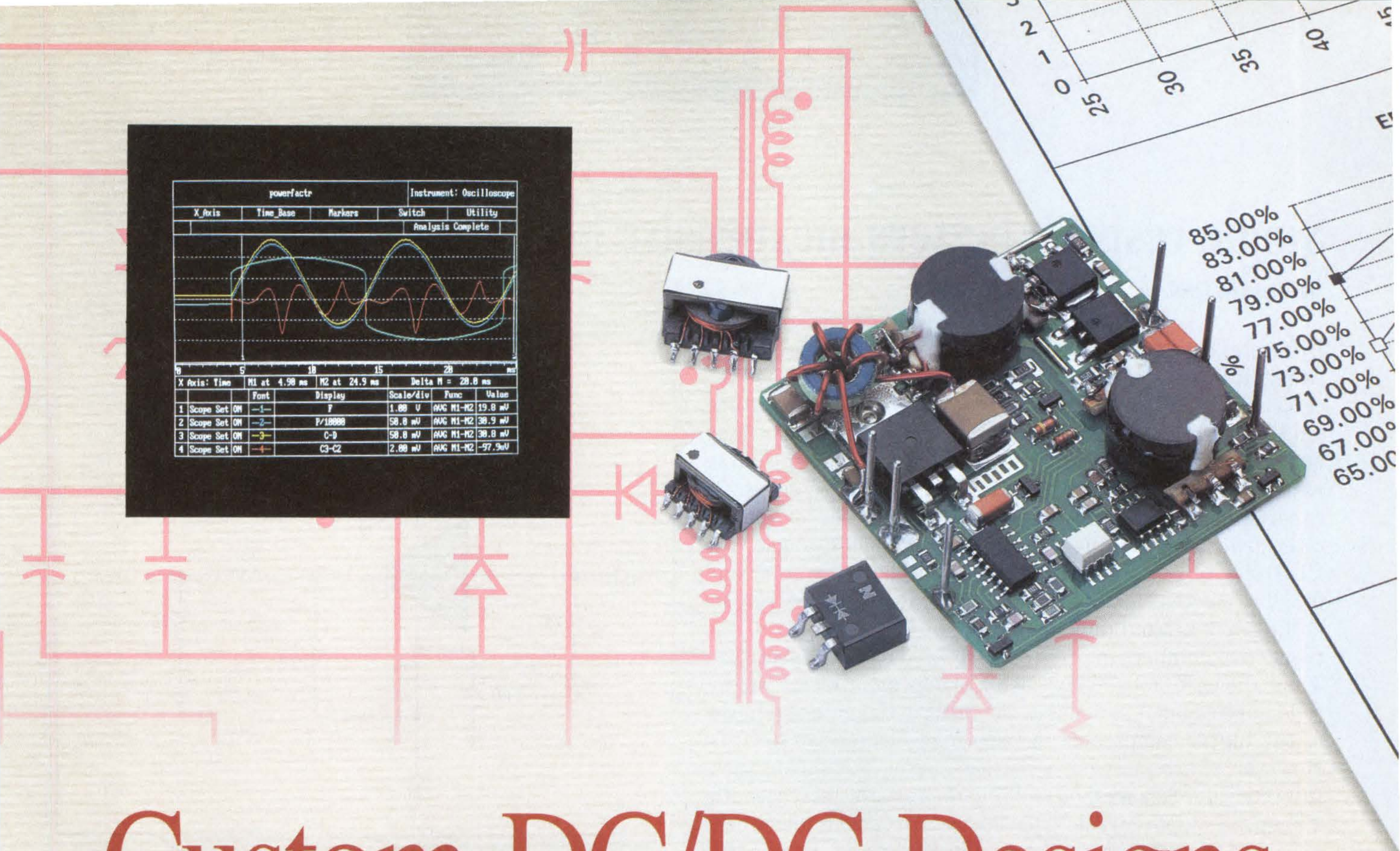


Fig 1—Because a switched-capacitor network can simulate a frequency-dependent resistor, this circuit allows a common DMM to measure frequency.



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CIRCLE NO. 78

Single resistor betters inexpensive buffer

Jim Riphahn, Comlinear Corp, Fort Collins, CO

Differential gain and phase are important video characteristics, and video-equipment manufacturers welcome any low-cost method of improving these parameters. **Fig 1** shows one simple method using a low-power, low-cost, closed-loop buffer with a total circuit cost of around $1.60, including resistors and bypass capacitors. Because output-stage drive capabilities affect differential gain and phase, low power often translates into degraded numbers. For example, the CLC109's typical differential gain and phase are 0.7% and 0.03°, respectively, while driving a 150Ω load. However, by adding a 1-kΩ pulldown resistor on the output pin, the respective numbers improve to 0.05% and 0.01°, respectively. Thus, the cost of a single resistor brings an order-of-magnitude improvement and makes the differential gain and phase of the buffer comparable to much more expensive devices. However, if low power is a sensitive issue, you should carefully consider this method. Adding the resistor increases **Fig 1**'s typical supply current from 3.5 to 7.5 mA. This idea works equally well with video op amps. (DI #1553) EDN

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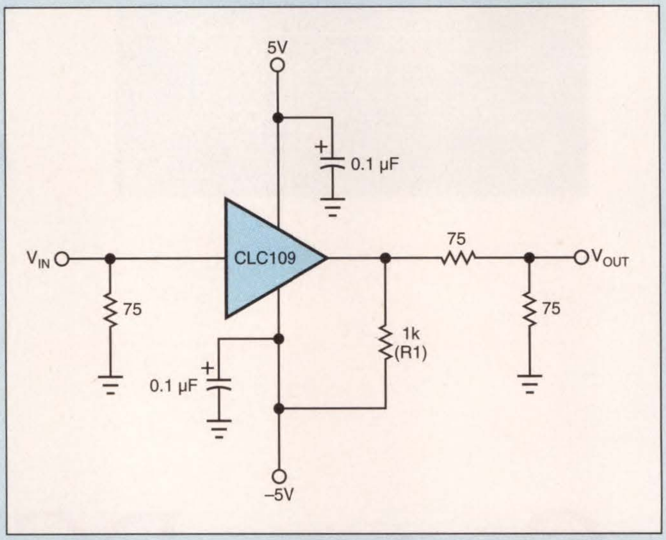

Fig 1—Adding a 1-kΩ pulldown resistor to an inexpensive, low-power buffer's output decreases typical differential gain and phase errors from 0.7% and 0.03° to 0.05% and 0.01°, respectively.

12-bit converter upgrades µC's ADC

John Wettroth, Maxim Integrated Products, Sunnyvale, CA

BBS

The simple circuit in **Fig 1** and an accompanying software routine let you easily substitute a multichannel 12-bit ADC for the 8-bit ADC internal to the 87C752 µC. A single assembly can then implement both the low- and high-performance version of a system. A socket lets you plug in the external ADC when you need it; otherwise, you plug in the network of 10 100Ω resistors. At power-up, the µC executes a routine that looks for the external con-

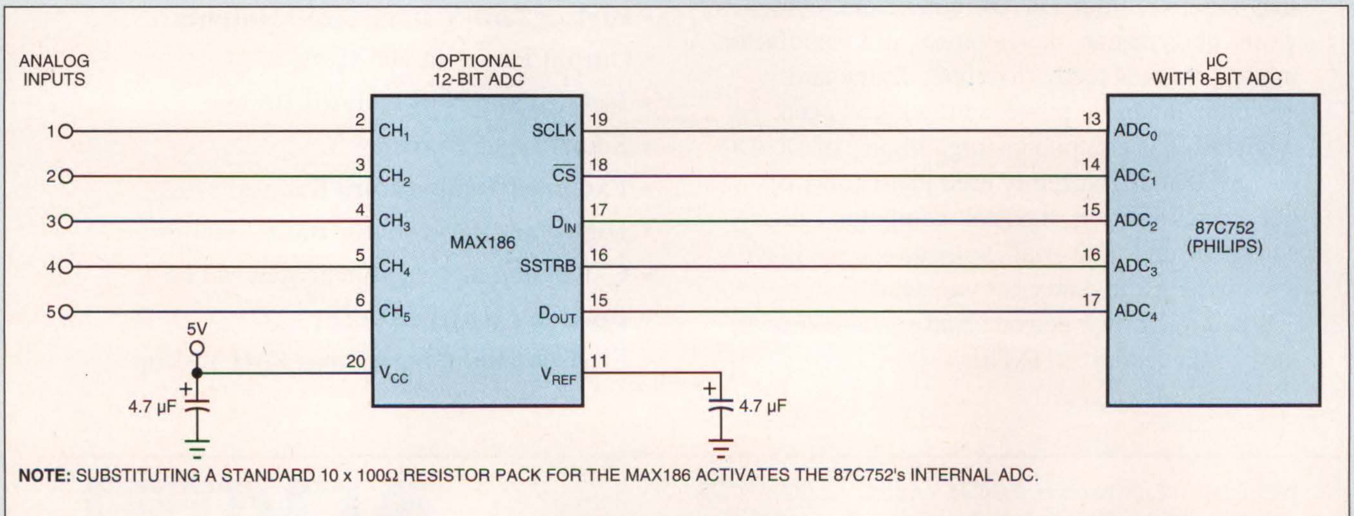

Fig 1—This circuit and corresponding software allow you to switch easily between using a µC's internal 8-bit ADC and using a more accurate 12-bit ADC.

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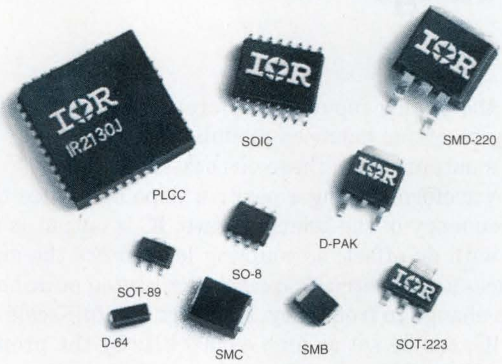

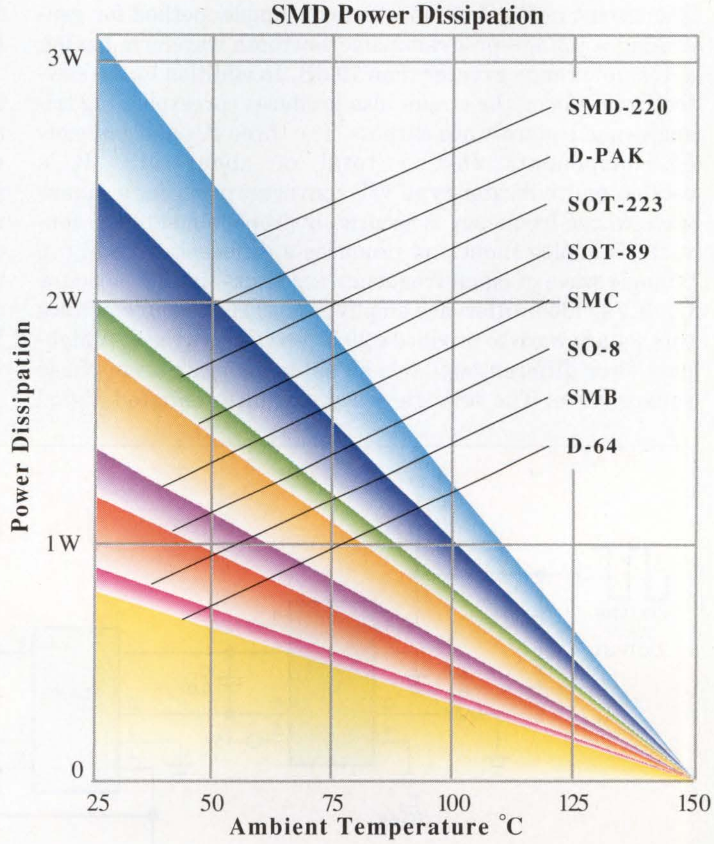

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CIRCLE NO. 109

verter. If the converter is present, the µC uses the external ADC. If the converter is absent, the 8-bit ADC takes over. The µC internally handles all conversion results as 12-bit values.

This idea relies on the fact that the 87C752's five ADC input pins can also serve as the bidirectional pins of an 8051 port (Port 1). The resistor network connects the internal ADC directly to the applied analog inputs. Alternatively, replacing the network with the external ADC connects those inputs to corresponding channels on that converter, and the µC's ADC input pins (now acting as a bidirectional port) serve as a digital interface to the converter.

The assembly-language software routine attached to **EDN BBS /DI_SIG #1554** determines the presence of an external converter by triggering a conversion and noting whether the converter's busy flag (SSTRB) goes low. If it does, the µC sets an internal global flag (AD12) that tells it to use the external-converter routines for each subsequent conversion. This action is transparent to the calling routine. The conversion result, returned as bytes ADHI and ADLO, has the same format in either an internal- or external-ADC case, except the four LSBs are 0 for 8-bit converter data.

The µC's full-scale range is 5V, but the MAX186 ADC sets it full-scale input range with an internal reference of 4.096V. Software resolves the incompatibility in this example, but you can also use a different ADC, such as the MAX188, with an external 5V reference. (DI #1554)

To Vote For This Design, Circle No. 332

Sawtooth generator spans a 70-dB range

Paul Hendricks, Analog Devices, Wilmington, MA

The circuit in **Fig 1** demonstrates a simple method for generating a voltage-programmable sawtooth waveform having a dynamic range greater than 70 dB. In addition to the sawtooth waveform, the circuit also produces corresponding triangle- and square-wave outputs. The three ICs and associated components cost a total of about \$13. IC_1's astable-multivibrator-type V/F converter produces a square wave whose frequency is accurately proportional to the converter's analog input and produces a differential 1.8 V p-p triangle wave of equal frequency across its timing capacitor C_T. IC_2's video-difference amplifier level shifts and amplifies this square wave to produce a 20 V p-p triangle wave. A high-pass filter differentiates this signal to generate an in-phase square wave. The triangle wave and differentiated signal drive the analog input and reference-comparator inputs of IC_3's gain-of-one balanced modulator.

IC_3's output under these circumstance is a 20 V p-p sawtooth waveform having a positive slope and twice the original frequency of the triangle wave. IC_1's output is a square wave with dc offset; ac coupling level-shifts the signal and produces a symmetrical square wave having no dc level shifts with a change in frequency. Although the full-scale frequency of IC_1 can be set as high as 500 kHz by the proper selection of R_S and C_T, the sawtooth waveform output begins to degrade above 50 kHz due to the bandwidth limitations of IC_3. (DI #1557)

To Vote For This Design, Circle No. 333

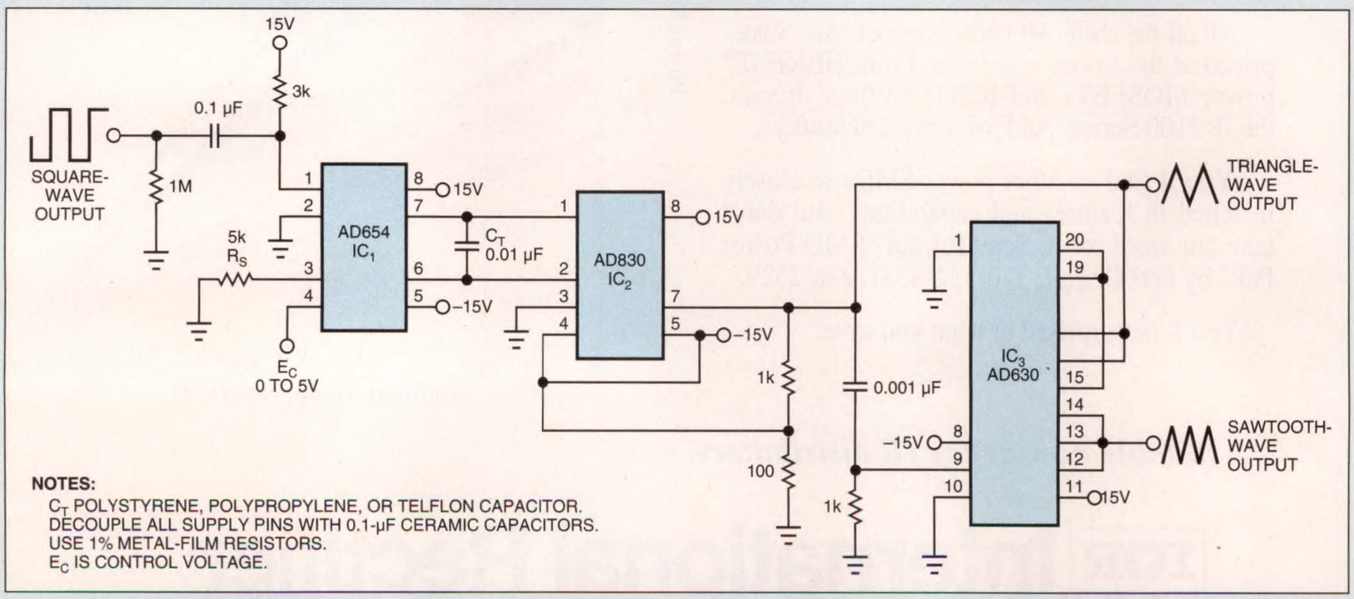

Fig 1—Three ICs and accompanying components produce a programmable sawtooth waveform with a 70-dB dynamic range and produce corresponding square and triangle waves.

10-octave audio generator speeds tests

Wayne Sward, Consultant, Bountiful, UT

BBS

Testing the frequency response of an audio device typically requires a sine-wave oscillator, an ac voltmeter or an oscilloscope, and an operator to record the response of the device at several frequencies across the audio band. Complicating this test is the inability of many audio oscillators to maintain a constant output level as the frequency varies, particularly when switching between frequency ranges.

To speed testing, the circuit in **Fig 1** generates a composite audio signal comprising 10 sine waves of 10 different equal-amplitude frequencies across the audio band. Values stored in EPROM determine the frequencies. Driving an audio device-under-test with this circuit allows you to test that device's responses quickly by connecting its output to an audio-spectrum analyzer. A quick check of frequency response requires only a few seconds. The output amplitude at the LINE output is 1V rms, and harmonics are all below –20 dB.

IC_1 generates a 128-kHz clock, which R_1 adjusts, to drive counter IC_2. The count from IC_2 addresses successive locations in EPROM IC_3. The EPROM contains the data values to generate the 10 octaves of equal-amplitude sine waves (see listing in **EDN BBS /DI_SIG #1559)**. In this case, the frequencies are 1 octave apart from 31.3 Hz to 16 kHz. IC_4 and IC_5 latch the 8-bit data from IC_3. The latched values drive IC_6, an 8-bit DAC.

The first amplifier of IC_7, a quad op amp, converts the current output of IC_6 to a voltage. The next two amplifiers filter the resulting signal, removing all frequencies above 20 kHz. The signal then goes through a level control and pad resistors to permit connection to the line or microphone inputs of the audio device. The signal also goes through the last section of IC_7 to an inverse RIAA filter. This filter compensates for the magnetic phono input of an audio amplifier, resulting in an overall flat frequency response of the test setup.

Two 9V batteries power the circuit. Voltage regulator IC_8 provides 5V power for IC_1 through IC_5. The resistors between –9V and each of the LM324 outputs prevent crossover distortion. All of the ICs are low-power to increase battery life. (DI #1559) EDN

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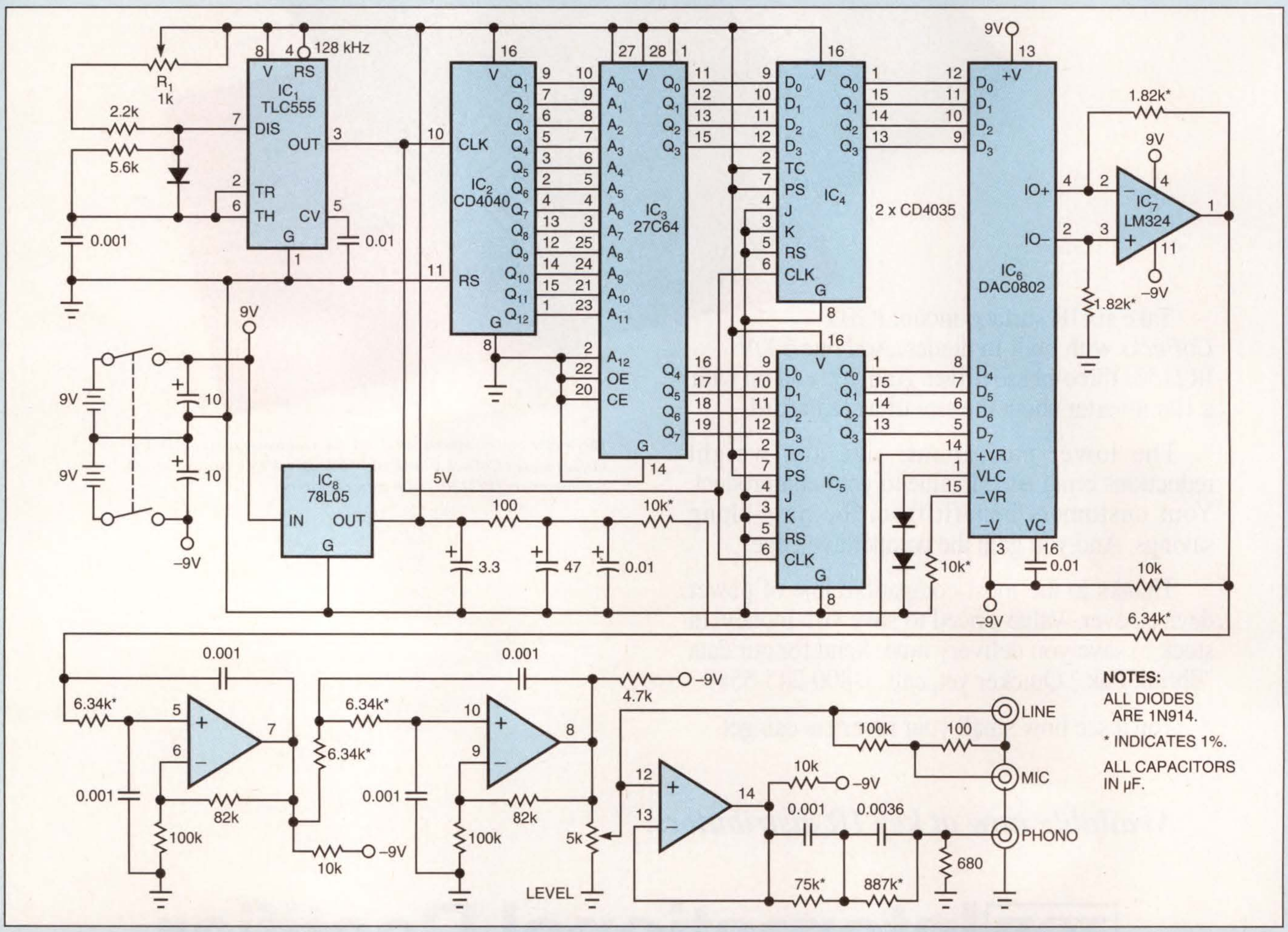

Fig 1—To speed testing of audio equipment, this circuit generates a composite audio signal comprising 10 frequencies of equal amplitude that span 10 octaves from 31.3 Hz to 16 kHz.

Envelope tracker quells jitter

Roger C Whipple, Hazeltine Corp, Braintree, MA

Fig 1's envelope tracking circuit solves the problem of receiving ac-coupled NRZ data over a coaxial data link. Because the spectral content of the NRZ data approaches dc (even with alternate frame inversion), the signal tends to integrate in any ac-coupled stage preceding the zero-crossing detector, despite the low cutoff frequencies. Thus, the dc level of the received data wanders, changing the relative switching point at the comparator.

The system input determines the data pattern, which can have frequencies that beat with the data frame rate, causing the data's envelope to have large excursions. After passing through a transmission medium, the signal is band-limited and has slow edges. Since the zero-crossing detector on the receiving end switches as the data crosses the reference-signal input, the apparent switching point moves if the reference is fixed but the data isn't. This movement can add a considerable amount of jitter to the output signal.

The envelope tracking circuit compensates for this problem by creating a reference voltage that is always centered between the local excursions of the data. The circuit uses the filtered average of positive and negative peak detectors as the reference voltage. The circuit itself is simple; C_1 charges on positive peaks through R_1 and D_1, and C_2 charges on negative peaks through R_2 and D_2. R_3 and R_4 determine the time constant of the discharge and provide the mean value to the reference pin. C_3 provides some noise immunity and should be near the comparator pin. The data rate determines the specific component values. The values chosen here work well with data rates from 0.5 to 1.5 Mbps. R_1 and R_2 determine the charge-time constant, which should be at least an order of magnitude shorter than the discharge-time constant controlled by R_3 and R_4.

Other factors that determine component selection are the drive capability of the input source, which must be able to charge the capacitors through the 390Ω resistors, and the amplitude of the input signal, which must be greater than two diode drops. **Fig 1**'s values are optimum for a signal of about 3V p-p biased at about 2.5V. You may have to reverse the polarity of C_2 if the input is not biased above ground. Circuit performance is not sensitive to any of the component values. (DI #1558)

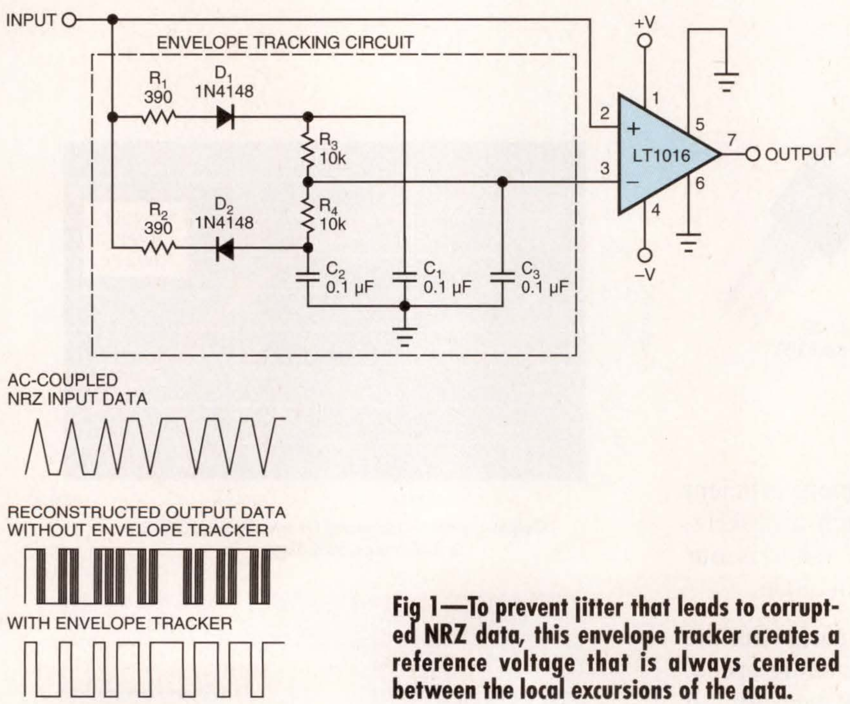

Fig 1—To prevent jitter that leads to corrupted NRZ data, this envelope tracker creates a reference voltage that is always centered between the local excursions of the data.

To Vote For This Design, Circle No. 335

IC diodes help deduce junction temperature

Edward S Brinkman, Cincinnati Electronics Corp, Mason, OH

A simple method for directly measuring an IC's temperature uses the device's input-protection diodes as temperature sensors. Static-discharge protection diodes are common features in many modern IC input structures, and their location on the IC makes them ideal as noninvasive temperature sensors.

Fig 1 shows the typical input structure for a CMOS IC and the measurement setup. One protection diode is forward-biased with a current source and suitable supply voltage greater than V_{DD}. The device under test can be fully operational if the selected input is normally tied to logic HIGH. For a logic LOW input, substitute a current sink and find a voltage supply less than V_{SS}. Other IC process technologies may also have accessible diode structure.

The ideal diode equation

$$V=(nKT/q)*(I/I_0+1))$$

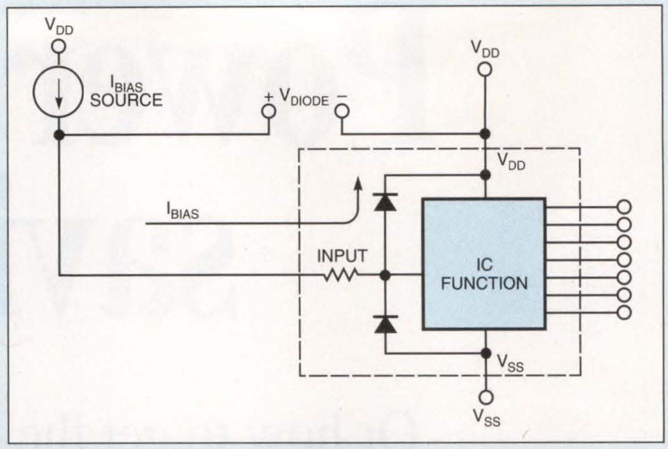

Fig 1—Using one of an IC's input-protection diodes as a sensor allows you to directly determine the junction temperature.

indicates the diode's temperature dependence. In practice, the voltage-temperature relationship is not quite linear, particularly over a large temperature range. Forward-bias currents from 10 μA to 1 mA have worked successfully with diode temperature sensors. Using the higher end of this range is recommended to avoid errors from device input current and the V_{DIODE} meter impedance; use lower bias current when the IC's input structure includes a significant series resistance. The performance of the I_{BIAS} constant-current generator is not critical. It is best to measure the volts-vs-temperature (V-T) slope of at least one representative device rather than relying on the above equation alone because of process-related departure from ideal behavior.

For a given process lot, the slope of the diode's V-T curve demonstrated consistent temperature-rise measurements within 1 or 2°C over a 100° span. Slope values of –2 to –2.4 mV/°C are typical for silicon. The intercept point on the V-T curve is less repeatable among devices, so if only lot sample data is available, a second measurement at a known temperature is recommended (ie, room temperature with the device's power off).

A word of caution: older CMOS ICs suffer from parasitic SCR latch-up when the input-protection diodes are driven into conduction. The results of this condition can be catastrophic. Modern CMOS designs are free from latch-up, with input diodes conducting tens of milliamps or more.

Also beware of problems due to noise, crosstalk from adjacent pins, and ground bounce. Also, the hottest spot on the chip may not necessarily be near the bond pad, and temperatures could be higher elsewhere. (DI #1555) EDN

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Low-power interrupt updates real-time clock

Yongping Xia, EBT Inc, Torrance, CA

Some µP-based systems need a real-time clock. The µP's built-in timer can do the work, but it usually requires several milliamps of current to keep the timer running. If the main power drops, the clock requires a backup battery to operate. The size of the backup battery depends mainly on how long the clock must run without main power supply and how much current the µP draws. Usually, during the main power supply's dropping period, the only task the µP should perform is to update the real-time clock.

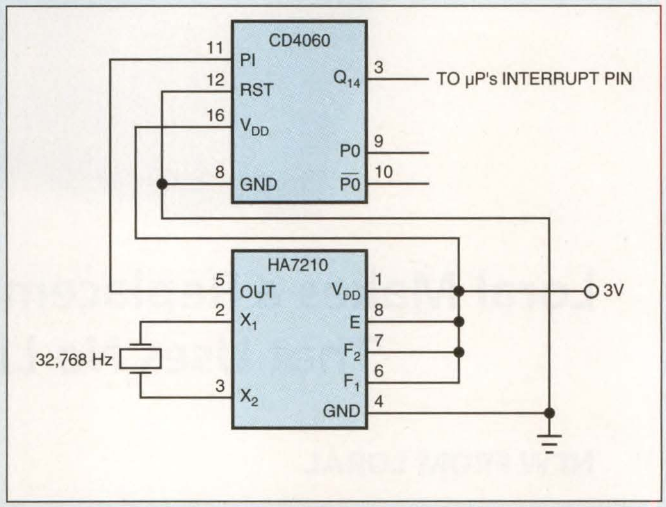

Fig 1—A further way to conserve power during main power-down conditions, is to generate a low-power interrupt that awakens the µP from sleep mode to update its real-time clock quickly.

However, there is an alternative way to run the real-time clock. Most CMOS-based µPs have stop or sleep modes in which the µP consumes only a few microamps of current. Instead of running all the time, the µP goes into stop or sleep mode if it detects a main power drop. Under these conditions, you can use an external interrupt source to awaken the µP and cause it to update the real-time clock and then return to sleep mode. Because the real-time-clock update takes only a short time, the µP still spends most of its time in sleep mode.

Fig 1's circuit provides an interrupt every 0.5 sec. The HA7210 (Harris Semiconductor, Melbourne, FL) low-current crystal oscillator consumes about 4 µA with a 32,768-Hz crystal. The CD4060 14-stage binary counter divides the output signal from the HA7210 down to a 0.5-sec square wave and consumes 7 µA more. You can set the µP to positive- or negative-edge-trigger interrupt mode. If the average µP current is 9 [mu]A, the total current with the interrupt circuit is around 20 µA. (DI #1556) EDN

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LINEAR TECHNOLOGY DESIGN NOTES

Source Resistance Induced Distortion in Op Amps

Design Note 84

William H. Gross

Introduction

Almost all op amp data sheets have Typical Characteristic Curves that show amplifier total harmonic distortion (THD) as a function of frequency. These curves usually show various gains and output levels but almost always the input source resistance is low, typically 50Ω. In some applications, such as active filters, the source impedance will be much larger. If the input impedance of the op amp is nonlinear with voltage, the resulting distortion will be significantly higher than the values indicated in the data sheet.

Test Circuit

It is quite easy to evaluate source resistance induced distortion. Connect the amplifier as a unity-gain buffer operating on ±15V supplies. Feed a low distortion $20V_{P-P}$ signal to the noninverting input through a source resistor and measure the output signal distortion. The setup is shown in Figure 1. The readings at 1kHz and 10kHz were recorded for various values of source resistance from 100Ω to 100k. The measured results for several op amps are plotted in Figures 2 and 3.

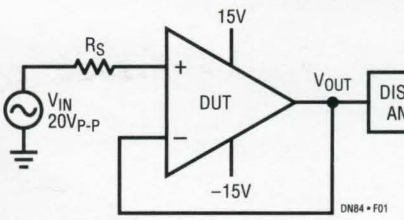

Figure 1

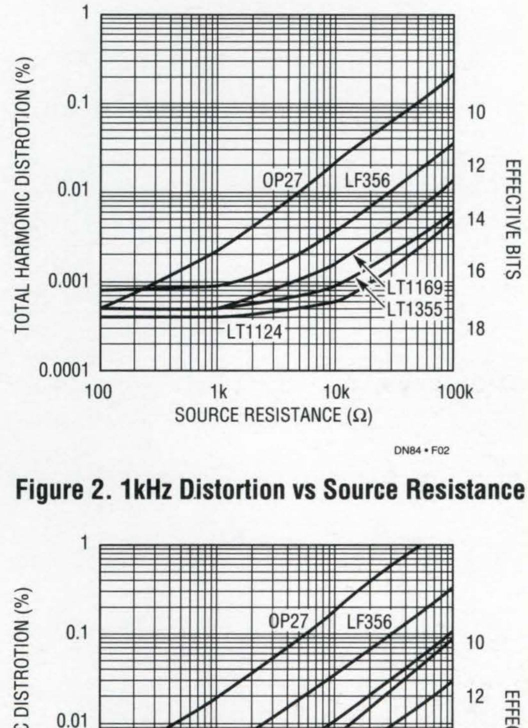

Figure 2. 1kHz Distortion vs Source Resistance

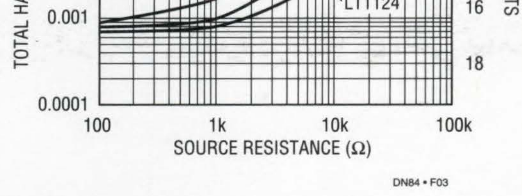

Figure 3. 10kHz Distortion vs Source Resistance

Results

Unfortunately there is no easy way to predict which amplifiers will have the lowest source resistance induced distortion from the data sheets. There are two main causes of the distortion: nonlinear input resistance and nonlinear input capacitance. At first thought, one would not expect the small input capacitance of an op amp to cause distortion at a few kHz. But a 10k source is loaded 0.01% by 1pF at 1.6kHz! Therefore a change in input capacitance of 1pF will cause measurable distortion at 1kHz. For lowest distortion we want an amplifier with low input capacitance as well as very high (and constant) input resistance.

FET input op amps have the highest input resistance but they also have a significant nonlinear input capacitance. The LF356 is a typical FET input op amp; the distortion is 5 to 20 times worse with a 10k source compared with a low source resistance. The LT1169 is a new dual FET input op amp with very low input capacitance (1.5pF) and therefore has about three times lower distortion than the LF356.

The OP27 is a popular high speed precision op amp that has very low distortion when driven from a 50Ω source. Unfortunately the input bias current cancellation circuit works well only at very low frequencies; at 1kHz the input resistance is very nonlinear. The distortion from the OP27 is 50 times worse with a 10k source than with a 100Ω source. The LT1124 is a dual low noise precision op amp that uses a different input bias current cancellation circuit. The LT1124 has the least source resistance induced distortion at 1kH of any of the op amps tested. The LT1355 is a member of a new family of low power, high slew rate op amps that have outstanding high frequency performance. The LT1355 has the least source resistance induced distortion at 10kHz of any op amp tested.

Figure 4 shows a 20kHz Butterworth active filter as might be used for anti-aliasing or band limiting in a data acquisition system. Figure 5 shows the frequency response of the circuit. Note that for signals well below the cutoff frequency, the capacitors have no effect and the op amp sees a 6.2k source resistance. Distortion was measured with several op amps in the circuit to confirm the data shown in Figures 2 and 3. Table 1 shows the results of the best op amps.

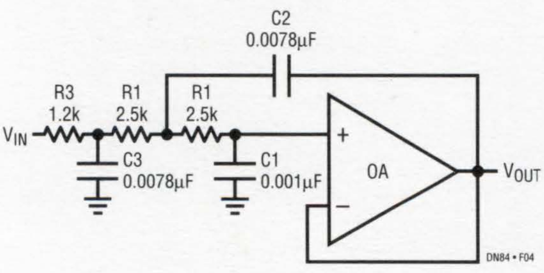

Figure 4

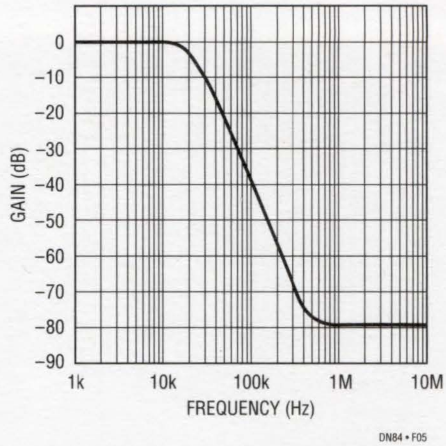

Figure 5. Filter Frequency Response

Table 1. Filter Distortion

Amplifier	100Hz	1kHz	2kHz	5kHz	10kHz
LT1124	0.0004%	0.0005%	0.0008%	0.0021%	0.0090%
LT1355	0.0005%	0.0006%	0.0010%	0.0035%	0.0052%
LT1169	0.0005%	0.0012%	0.0024%	0.0080%	0.0100%

Source resistance induced distortion usually limits the dynamic range of unity-gain RC active filters. An interesting high performance alternative is the LTC1063 and LTC1065. These fifth order, switched-capacitor lowpass filters are not only smaller and easier to use, their distortion is less than 0.01% even with 10k source resistance.

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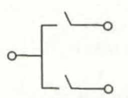

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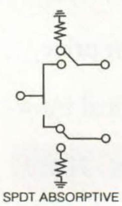

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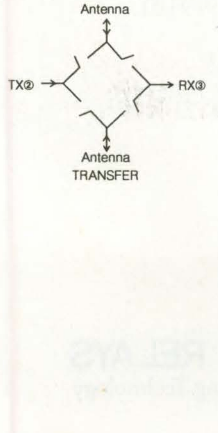

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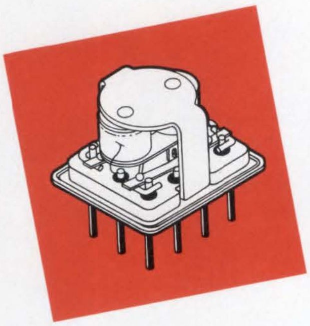

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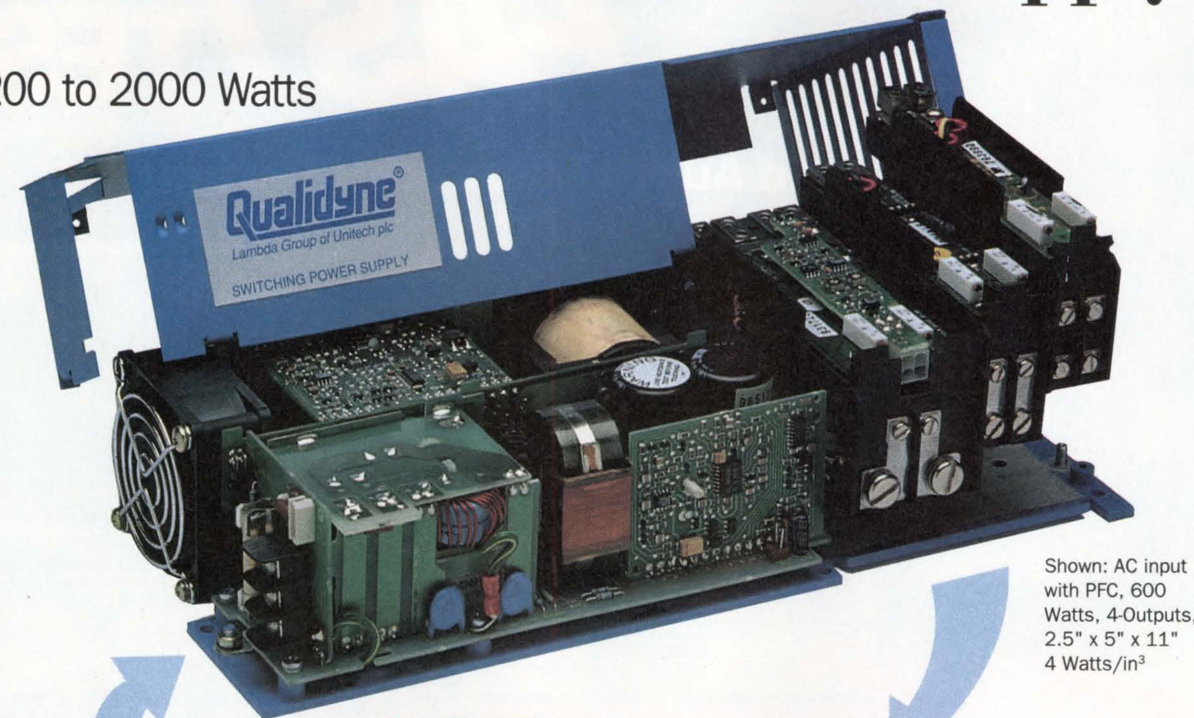

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[1]Sample suite of GPIB programmed audio measurements included 1) noise measurement (20Hz-22kHz bandpass), 2) 31 point single tone frequency response sweep over 20Hz-22kHz range, and 3) 11 point distortion sweep over 20Hz-22kHz range.
[2]*FAST*TEST uses multi-tone stimulus and analysis to make the same measurements listed above.

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CIRCLE NO. 94

Break the performance bottlenecks in today's multiprocessor designs

Brian Bennett, AST Research Inc

New operating-system and device-driver software for symmetric multiprocessing hardware make interrupt distribution the least important hardware-design consideration. You achieve better performance by developing an efficient bus protocol and increasing concurrency.

Early efforts to supply additional processing power by adding CPUs to a common bus resulted in a simple master-slave relationship between CPUs, called "asymmetrical multiprocessing." Though this architecture was simple, it soon reached a "premature" bottleneck because of poor task distribution among processors. The architectural limitations occur in both software and hardware. Early operating-system (OS) software neither could run in multiprocessor systems nor could take full advantage of the increased processing power.

Additionally, most I/O drivers were "single-threaded," which limited their execution to a single dedicated I/O processor. Initially, this was not a major problem because "asymmetrical hardware" typically did not allow all processors access to all system resources. In general, asymmetric hardware dedicates a single processor to I/O functions. The performance of this single I/O processor can, and often does, become the system bottleneck as it reaches its performance limits. Both the asymmetric hardware and single-threaded software pose barriers to system performance. Thus, asymmetric machines exhibit limited scalability because adding processors does not benefit a system that is limited by the performance of one of its processors.

The solution to this bottleneck was to redesign both the hardware and the software, which led to today's symmetric multiprocessors (SMPs) coupled with multithreaded software. An "SMP" is a system in which all processors are identical and all resources—specifically, all the memory and I/O space and interrupts—are equally accessible. While the symmetrical nature of SMP hardware eliminates any architectural barriers, the software must still efficiently divide the tasks among processors.

SMPs have been slow to catch on because they require software to provide a performance advantage over asymmetrical multiprocessing architectures. That is, without "symmetric" software, SMP hardware performs at the same level as an asymmetrical multiprocessor.

Fixed vs dynamic interrupt allocation

In an asymmetrical multiprocessor system, one processor typically performs all the I/O and, hence, fields all the I/O interrupts, performs the low-level I/O functions, and passes interrupts to the processor elements as needed. One of the most controversial issues in an SMP design is how to distribute the interrupts to the system processors. Generally, you can use one of two implementations: fixed or dynamic (lowest priority) distribution.

From a strictly hardware perspective, fixed distribution—the (programmable) assignment of interrupts to specific processors—offers the advantage of simplicity. Furthermore, by repeatedly assigning a specific interrupt to a given processor, that processor is more likely to have the interrupt-service routine (ISR) in its cache. In this scenario, a CPU (say, CPU A), which has just serviced the interrupt can more quickly and more efficiently handle the interrupt while using less precious system-bus bandwidth than some other CPU (say, CPU B). However, if enough time passes, newer data and instructions may overwrite the contents of CPU A's cache, thus destroying the benefit of sending the interrupt to the same processor. The down side to this approach is that CPU B may be "less busy" and better able to service the interrupt.

Dynamic distribution relies on interrupt-control hardware to route the interrupt to the lowest priority processor. The hardware does this in the hope of assigning the additional workload of the ISR to the least busy processor (the one executing the lowest priority task). This assignment increases a system's scalability by more evenly distributing the workload.

To ascertain the performance impact of interrupt distribution, ask a more fundamental question: What does the OS do within an ISR when the ISR processes an interrupt? Today's ISRs are small routines that identify the source of an interrupt (when multiple devices share an interrupt), perform any housekeeping necessary to re-enable the interrupt, and pass a deferred-procedure call (DPC) to the system via a system-process queue. (**Fig 1**). The next available processor that takes a job from the process queue also handles the interrupt.

In light of this information, coupled with the relative infrequency of interrupts as a percentage of bus-cycle time, you can deduce that the interrupt-distribution method is relatively benign as far as system performance goes. In fact, an asymmetrical interrupt distribution in which one processor services all interrupts is technically acceptable. The asymmetric architecture might, however, make a product difficult to sell. Today's interrupt-handling solutions are based more around cost factors and software support than around the performance merits of the hardware mechanisms that distribute the interrupts.

System-bus bandwidth

An architecturally superior SMP machine can eliminate the previous system bottleneck, but three new bottlenecks appear: software scalability; limitations of the backbone, or common multiprocessor bus; and limitations of the I/O subsystem. These design tradeoffs are not specific to SMP design, but they become more prominent as you add processors.

Designers generally ask two questions when evaluating a backbone bus for SMP systems:

- 1) What is the clock speed?
- 2) What is the data-bus width?

However, the answers to these questions may not be the best measure of relative performance and usable bandwidth. The overall best number to evaluate a multiprocessor bus is the sustainable bandwidth because it reflects not only the bus speed and data-bus width, but also the bus-protocol efficiency. Although a high number is generally better, it comes with a cost and other tradeoffs.

Designers should expend no more cost than necessary to provide a design that balances system- and I/O-bus requirements. What good is a 400-Mbyte/sec sustained throughput on a system bus if an application requires an I/O data rate of 40 Mbytes/sec, and the I/O bus operates at only 33 Mbytes/sec? In this example, a user would pay extra for system-bus bandwidth without realizing the benefit. Unfortunately, the variety of applications, each with differing I/O-bandwidth requirements, makes this tradeoff more of an art than a science.

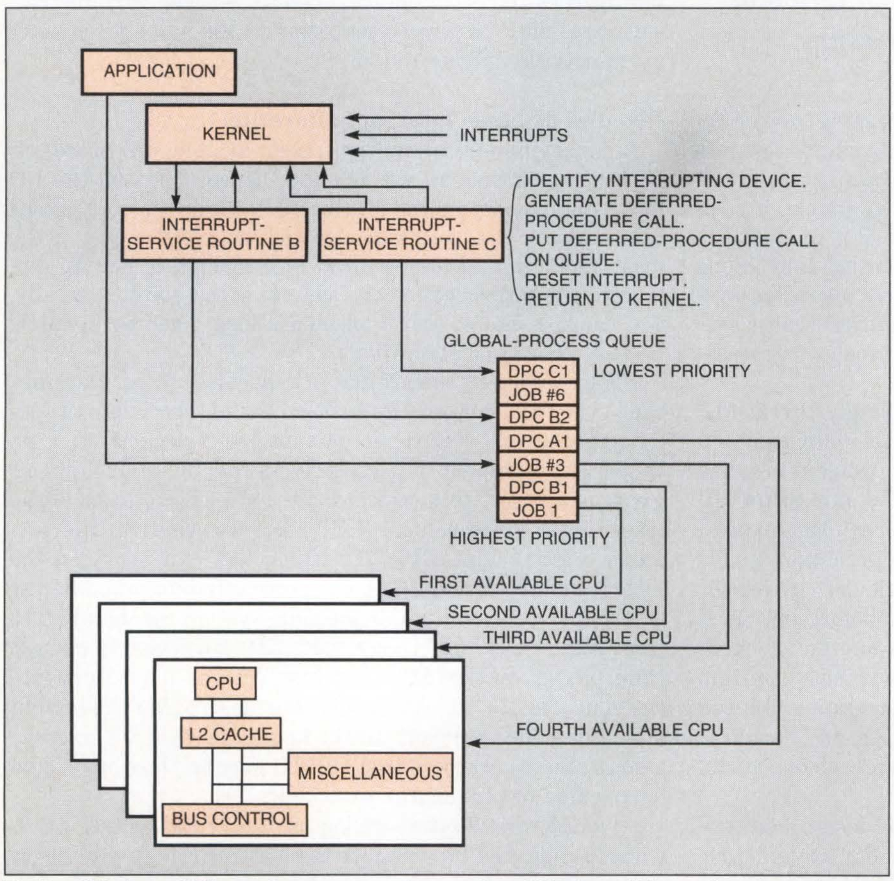

Fig 1—Windows NT keeps interrupt-service routines (ISRs) small by performing only minimal processing at the ISR level. Instead, the ISR generates a deferred-procedure call (DPC), which the system queue manages.

Benefits of improving protocol

Aside from increasing the bus speed and data width, a more efficient use of system-bus bandwidth can yield significant gains. For a fixed memory-access time, increasing the bus speed may provide little gain: Instead of waiting five clocks at 25 MHz, you can wait 10 clocks at 50 MHz. For systems with separate address and data buses, you can pipeline accesses on the bus so that CPUs can simultaneously access multiple memory banks.

Interleaving memory boards on cache-line boundaries allows concurrent memory accesses. Pipelining increases sustainable throughput for a 33-MHz, 267-Mbyte/sec bus from 107 to 214 Mbytes/sec (**Fig 2**). Because of the probabilistic nature of cache-line interleaving, you may realize on an average only half of this gain. Thus, you can achieve a 50% increase in bus throughput with little added complexity—the ability of the memory to register two addresses plus some minor control logic.

Memory pipelining improves bus efficiency but requires a simpler memory design than does a split-transaction protocol. Because μPs can pipeline the address bus, pipelining becomes a natur-

SYMMETRIC MULTIPROCESSORS

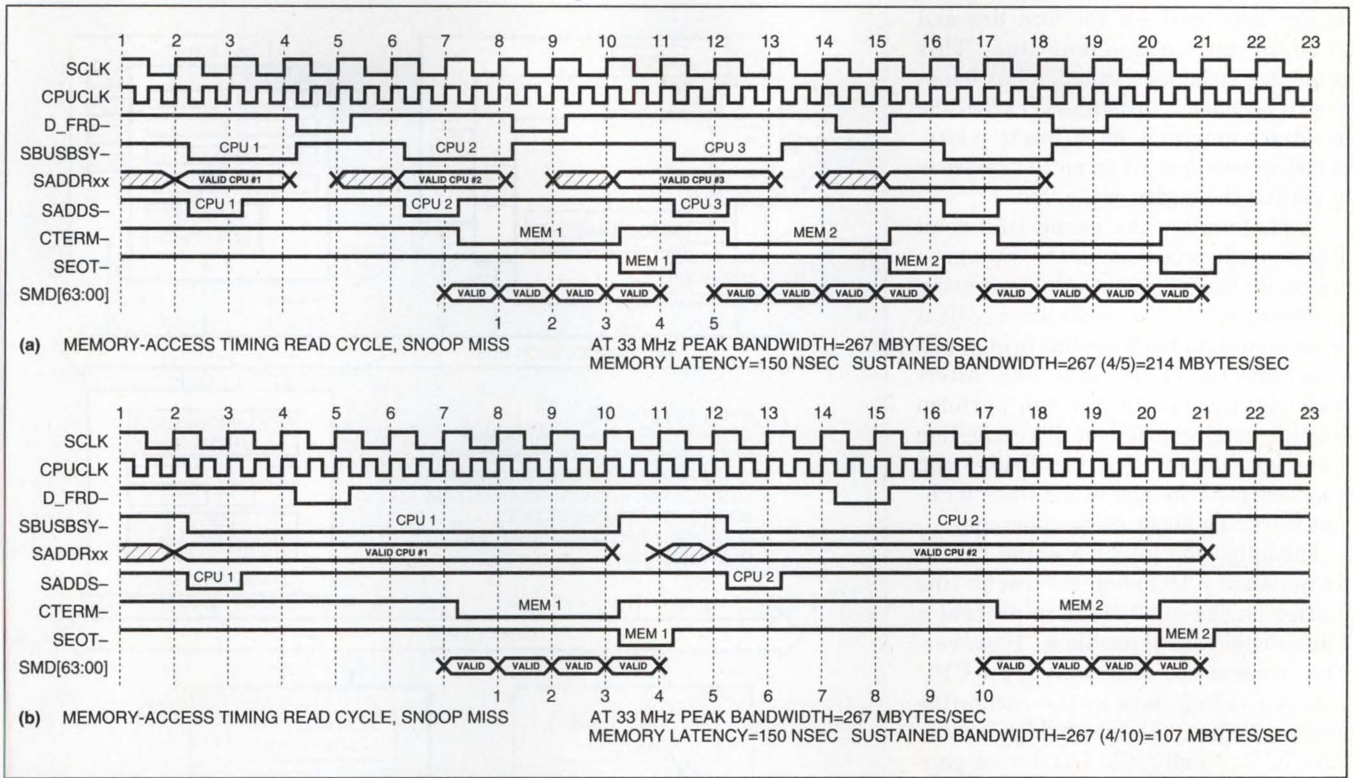

Fig 2—A pipelined system bus (a) achieves a significant increase in throughput over a nonpipelined system (b).

al extension from the CPU to the system bus in SMP systems.

Another way to address long-latency accesses is to use a split-transaction-protocol bus that can reconnect and transfer data. Though you can also use the split-transaction mechanism to access multiple memory modules, the relative speed of memory response usually does not warrant adding such complexity to the memory boards.

A split transaction typically provides the most benefit for long-latency accesses such as those that occur when the processor accesses an I/O controller through an I/O bridge. When the processor writes to such I/O devices, a posted-write buffer usually can eliminate any write latency, but read operations can still take a long time. In general, an I/O-bus bridge contains the logic to be a system bus master. To add the split-transaction capability, you need only to add control logic.

Although many designers recognize the need for split transactions to minimize the bus use on long-latency I/O-bus cycles, many do not see a need to support the split transactions to main memory. The memory references are fast enough to justify this decision, but this unnecessary bus limitation may preclude the bus architecture from supporting future directory-based cache architectures with a scalable-coherent-interface (SCI) topology. A bus that implements SCI correctly has no performance penalty compared with a non-split-transaction bus. Memory boards need only monitor the signal D_FRD to know that they are not responding to the current access (**Fig 2**). Memory actions are then similar to the actions the memory takes when responding to a snoop-hit-dirty condition.

I/O-subsystem bus bridge

Several multiprocessor systems offer dual-bus bridges to provide multiple paths to I/O resources. Whether or not you choose a multiple-I/O-bridge architecture, you must optimize this interface. When speaking of performance and I/O buses, the magic word is "concurrency." Concurrency can take many forms in any multiprocessor. For example, an SMP can have several concurrent events occurring in the system (**Fig 3**).

To obtain the highest performance possible from the bus bridge, it must have cache-line buffers to enable it to transfer data to or from the I/O bus *concurrent* with activity on the multiprocessor bus. Cache-line buffers offer many performance benefits. First, they allow concurrent operations; the system and the I/O bus operate simultaneously. Second, cache-line buffers package the I/O bus' (usually) smaller data width into the full data-bus width and thus consume fewer system-bus cycles. Third, cache-line buffers allow the bus bridge to burst an entire cache line, eliminating any idle time between burst data as the faster multiprocessor bus waits for the next data from the I/O bus.

Cache-line buffers allow transfer of a full cache line over the bus bridge, which raises two issues: What if the I/O device needs to transfer only a few bytes of data, and what if the transfer starts or ends in the middle of a cache line? You solve these problems in one of two ways: Some architectures allow only full cache-line transfers. In this case, you have no choice except to let the bus bridge perform a read-for-ownership cycle and then write the new data into the cache line. When the I/O device proceeds to the next cache line, the buffer must cast out the first line and read in the subsequent line. This approach consumes valuable bus bandwidth because a "worthless" cache-line read accompanies each burst write, which is needless when an I/O device is updating the entire cache line.

Additionally, the cache-line read causes each processor in the system to snoop its cache, potentially decreasing performance. These reads are needless when new data from the bus bridge will overwrite the *entire* cache line. Alternatively, the bus bridge can perform partial-word transfers until a cache-line boundary occurs. The bus bridge can then burst-write the cache lines without worrying about cache coherency.

Initially, you might assume that it is necessary to snoop the cache-line buffer on the bus bridge to prevent a cache-coherency problem. However, the problem can occur only if the CPU starts reading data in the cache-line buffer before the bus bridge transfers it. Typically, the I/O device generates an interrupt to the system when the I/O operation is complete. If the CPU starts to read data before this interrupt, the data might be stale whether or not it is buffered in a bus bridge. However, if the interrupt has a separate path from the data, the interrupt can "bypass" the data in the bus bridge (**Fig 4**).

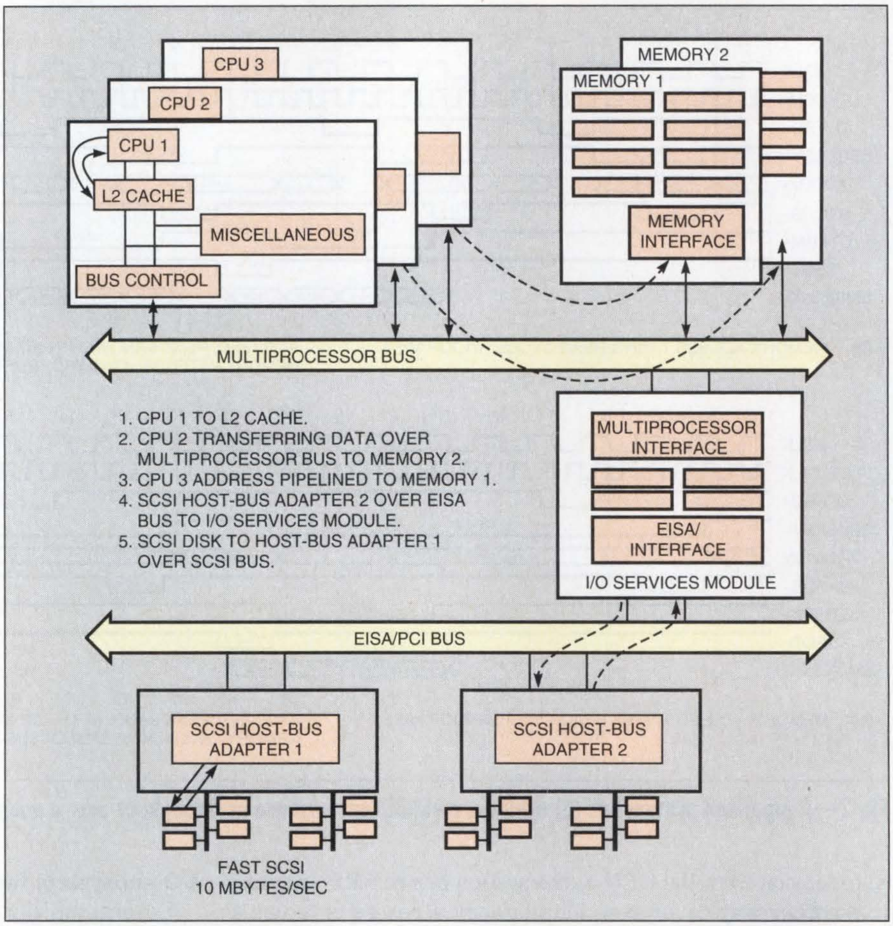

Fig 3—Increasing system concurrency is one key to maximizing performance.

Separate interrupt and data paths open a small "window" that can be a major problem (and would then require snooping of the bus bridge). If the CPU attempts to use I/O data before the bus bridge transfers the last byte and if the bus bridge lacks a snoop feature, the CPU gets stale data. You can prevent this problem by forcing the bus bridge to empty the data buffers before transferring the interrupt vector. Thus, it is not necessary to snoop the bus bridge.

When the bus bridge is transferring a new cache line to memory, the CPU cache could hold the same cache line as "modified" data. Because this data is "old," a mechanism should tell the CPU to snoop and invalidate without write-back. This scheme eliminates the need for the bus bridge to wait for the snoop results and the write-back of any modified data from the CPUs.

Avoiding deadlock

A system employing bus bridges for concurrent operation must avoid deadlock. Deadlock occurs when a CPU attempts to access the I/O bus at the same time that an I/O device attempts to access the system bus, such as for main-memory access.One of these bus masters needs to back off, but which one? A system employing a standard PC I/O bus, such as EISA, may not have a choice: There is no graceful back-off mechanism.

For single-CPU systems, implementing a single back-off signal would work fine. However, multiple CPUs complicate the situation. To avoid stopping all processors, each needs a separate back-off signal. Using one signal line is better because the bus bridge tends to be a pin-limited board. Using a deferred response is undesirable because it requires the bus bridge to store several requests while filling the cache-line buffers from the I/O device. Such a scheme is possible but costly and provides little performance gain.

A preferable design is to have processors that are requesting access to the bus bridge monitor the signal line IOBUSBSY. The bus bridge asserts this signal before it grants the bus to the I/O device, thus allowing one possible simultaneous write to access the I/O bus before granting the I/O bus to the I/O device. To accomplish this, when initiating an operation, each CPU must first decode its own address and monitor IOBUSBSY. This technique keeps unnecessary back-off cycles off the system bus.

Partial vs full cache-line transfers

Some designs simplify the memory interface and the bus protocol by allowing only full cache-line transfers. This approach eliminates the need for logic to perform the read-merge-write operations for writing partial words to memory. (The read-merge-write is needed to generate correct ECC bits for a 32-bit word.) Because most transactions are cache-line operations, this approach may at

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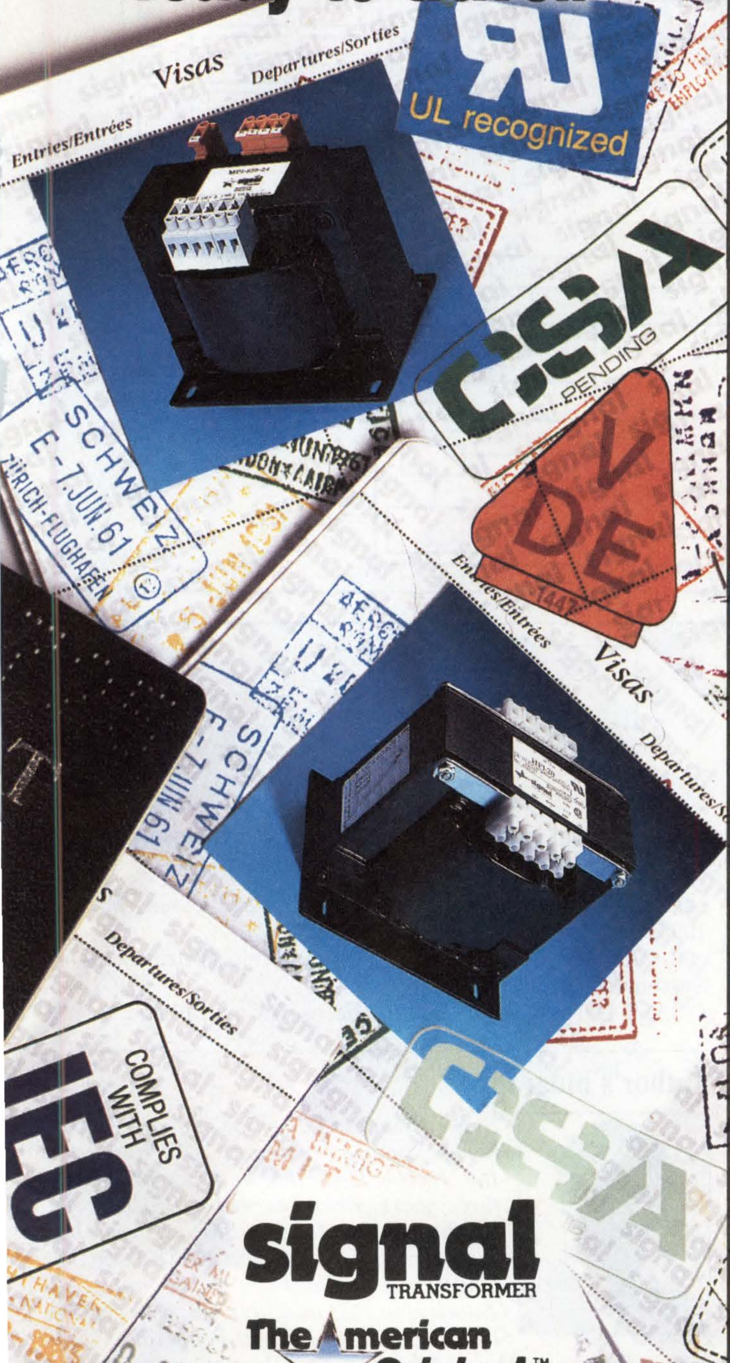

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Size	L	W	H	ML (mtg)*	MW (mtg)*	WGT
200VA	3.750" 95.3 mm	4.203" 106.6 mm	3.720" 94.5 mm	3.250" 82.6 mm	2.800" 71.1 mm	6.22 lbs 2.82 kg
250VA	4.125" 104.8 mm	3.898" 99.0 mm	4.000" 101.6 mm	3.625" 92.1 mm	2.601" 66.1 mm	6.76 lbs 3.07 kg
300VA	4.125" 104.8 mm	4.223" 107.3 mm	4.000" 101.6 mm	3.625" 92.1 mm	2.915" 74.0 mm	7.80 lbs 3.54 kg
400VA	4.125" 104.8 mm	4.805" 122.0 mm	4.000" 101.6 mm	3.625" 92.1 mm	3.505" 89.0 mm	9.82 lbs 4.46 kg
650VA	5.250" 133.3 mm	4.430" 112.5 mm	4.800" 121.9 mm	4.500" 114.3 mm	3.415" 86.7 mm	14.83 lbs 6.73 kg
900VA	5.250" 133.3 mm	5.197" 132.0 mm	4.800" 121.9 mm	4.500" 114.3 mm	4.205" 106.8 mm	19.84 lbs 9.01 kg

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Mechanical Dimensions

Size	L	W	H	ML (mtg)*	MW (mtg)*	WGT
2000VA	7.500" 190.5 mm	5.600" 142.2 mm	6.560" 166.6 mm	5.750" 146.1 mm	4.350" 110.5 mm	41.3 lbs 18.71 kg
2750VA	7.500" 190.5 mm	6.230" 158.2 mm	6.560" 166.6 mm	5.750" 146.1 mm	4.980" 126.5 mm	48.0 lbs 21.77 kg
3500VA	7.500" 190.5 mm	7.330" 186.2 mm	6.560" 166.6 mm	5.750" 146.1 mm	6.080" 154.4 mm	62.4 lbs 28.30 kg

first glance appear optimal. But this approach can limit performance when interfacing to a bus bridge. Unless you can guarantee that all I/O-subsystem read operations will begin and end on cache-line boundaries *and* will contain only full cache-line operations, the bus bridge will need to perform a "read-for-ownership" cycle to acquire the cache line before writing the data from the I/O device. Once the I/O device writes new data into the cache line, the bus bridge must then write the cache line back to main memory. Thus, the bus bridge consumes *twice* the I/O-bus bandwidth on the system bus. (That is, when transferring data from the I/O bus at 33 Mbytes/sec, the bus bridge needs 33 Mbytes/sec of "read-for-ownership" cycles and 33 Mbytes/sec of cache-line write cycles.)

This design may lose additional performance because it requires two cache snoops: one when the bus bridge reads the cache line and one when it writes the cache line back. However, you could eliminate snooping on cache-line write-back operations.

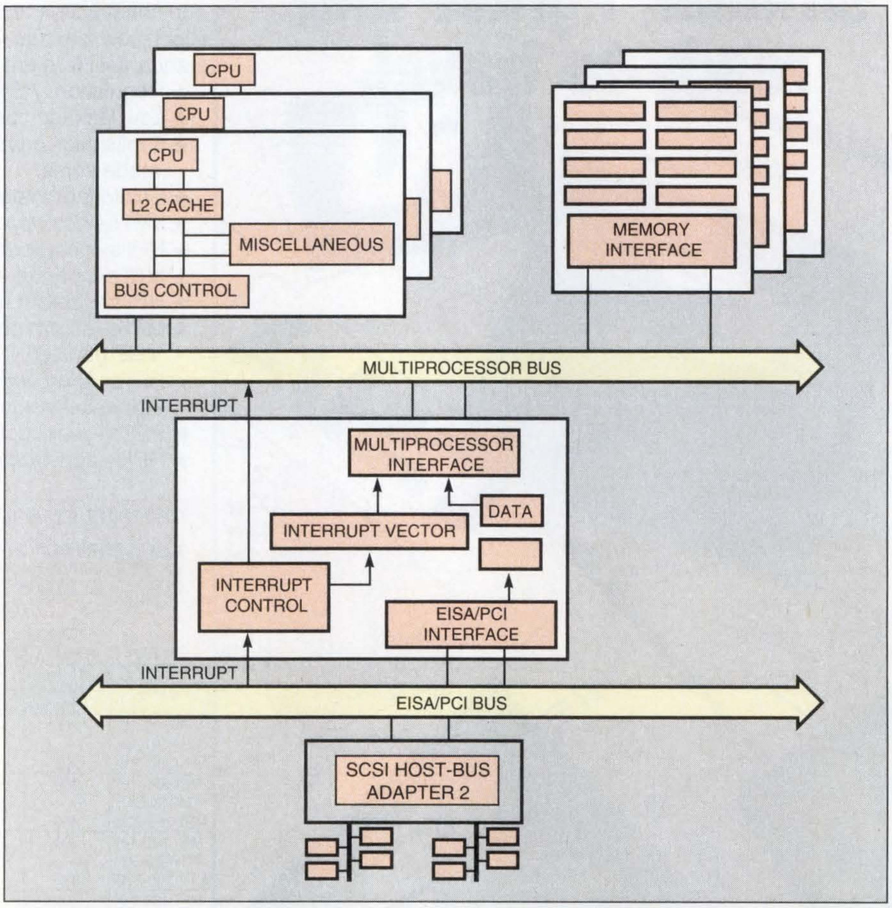

Fig 4—Snooping into a bus bridge that contains cache-line buffers is unnecessary if your design ensures that the device interrupt cannot "bypass" the device data.

Software is the key to scalability

Contention for common resources, such as system memory and I/O, cause delays that degrade processor performance, which, in turn, limits hardware scalability. Improved bus throughput, faster memory, and larger caches help mitigate the impact of bus contention, but the software also plays a significant role. The software's scalability lies in its ability to break tasks into subtasks, or "threads," which can execute independently.

Threads differ from traditional "processes" in that they carry less machine context and, therefore, do not overburden a system with context saving and restoring. Building the OS kernel from these threads spreads the work of the OS across several processors. "Single-threaded" software, on the other hand, executes whole tasks on one processor. Early I/O drivers, for instance, executed almost entirely at the ISR level and as single, whole tasks. Thus, they required a major OS rewrite to define threads that could execute in parallel. The finer these threads, the more benefit a design derives from multiple processors.

The point of diminishing returns sets in when the time spent in task synchronization offsets the benefit of smaller threads and when more semaphore accesses cause increased bus use and, in turn, decreased performance. EDN

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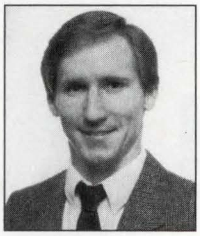
Author's biography



Brian Bennett is a senior engineer in the Server Systems group at AST Research Inc, Irvine, CA,where he has worked for three years. Brian earned a BSEE from California Polytechnic State University (San Luis Obispo), and an MSEE from the University of Southern California (Los Angeles) in 1981 and 1991, respectively. He is working on an MBA at Pepperdine University (Malibu, CA). In his spare time, he enjoys skydiving, rock climbing, and bronco riding.

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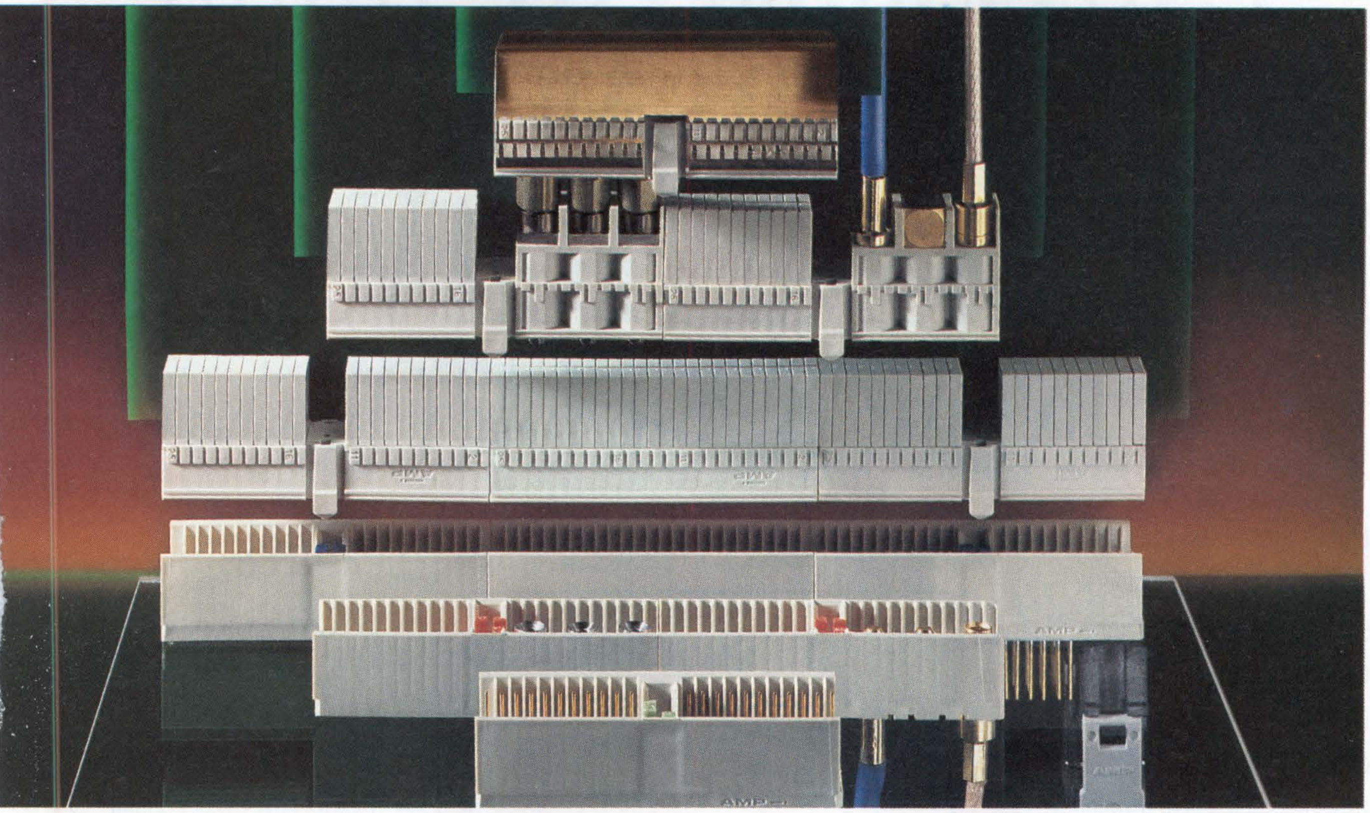

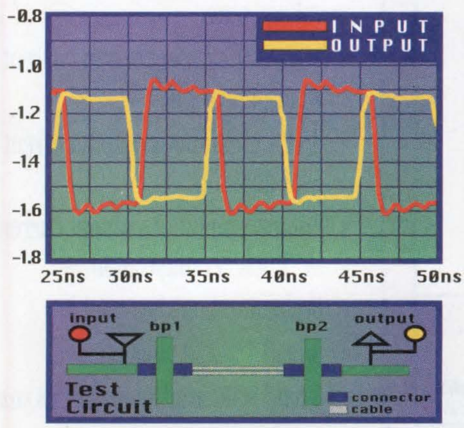

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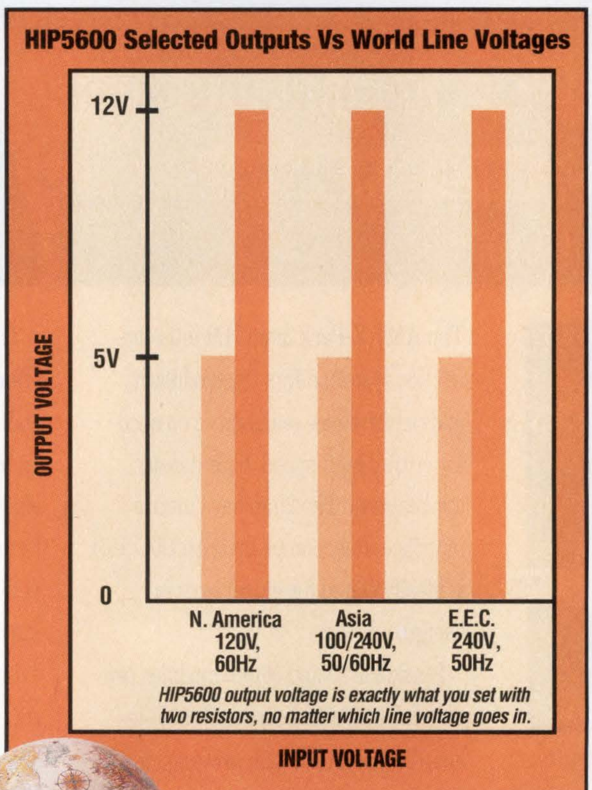

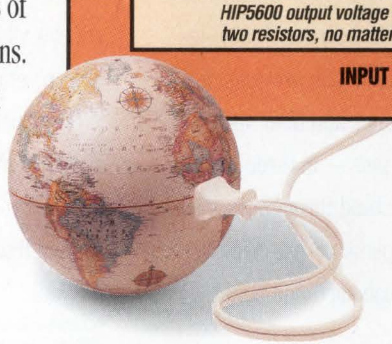

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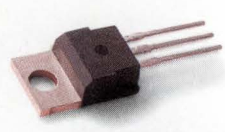

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CIRCLE NO. 32

To see spectrum-analysis detail fast, match sweep time to measurement

Morris Engelson, Tektronix Inc

In spectrum analysis, slower sweep speeds provide improved detail. If you understand some basics, however, you can choose a sweep speed that provides needed detail without wasting time.

A spectrum analyzer's sweep time (T) depends on the frequency span to be displayed (S), the resolution bandwidth (B), the video-filter bandwidth (V), the signal-intercept or detector function (D), and the vertical-display setting (VD). (Some secondary factors that also affect the sweep time, such as the digital-storage sample rate, are not discussed here.) The sweep time increases directly with the span and inversely with the video-filter bandwidth and the square of the resolution bandwidth. The peak-detector function in the 10-dB/div logarithmic vertical mode usually provides the fastest sweep and the minimum measurement time. In addition, you can achieve faster sweep times by accepting reduced measurement accuracy or by using accessory items such as a preamplifier.

The abbreviated block diagram of **Fig 1** relates spectrum-analyzer operating functions to circuits. The frequency-sweep width of the first local oscillator determines the span. The swept mixed signal is translated after the bandpass filter that determines the resolution, or signal separation. After the resulting spectrum is detected, it is amplified in a lowpass "video-filter" amplifier prior to display on the CRT. The two most critical functions are the predetection resolution-filter bandwidth (B) and the postdetection video-filter bandwidth (V).

The relationships among the key parameters are well understood and have been discussed in literature. However, the discussion is spread out over many publications and sometimes appears as a footnote to a different main topic. This article provides a complete picture of accuracy/sweep-time tradeoffs by summarizing and integrating the scattered information.

Span, time, and bandwidth

Ref 1 shows that for spectrum analyzers whose bandwidth is specified at the –3-dB points (for example, those made by Hewlett-Packard) the span (S), resolution bandwidth (B), and sweep time (T) are related by the formula $S/TB^2=0.5$. For spectrum analyzers that specify resolution bandwidth at the –6-dB points (those made by Tektronix,

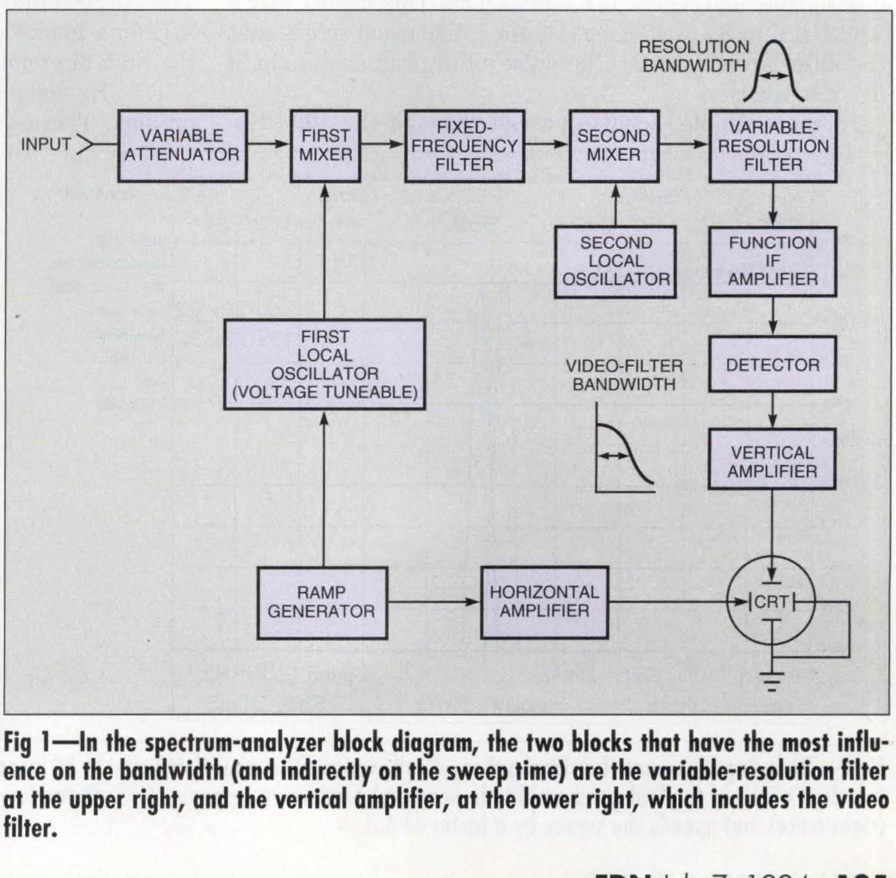

Fig 1—In the spectrum-analyzer block diagram, the two blocks that have the most influence on the bandwidth (and indirectly on the sweep time) are the variable-resolution filter at the upper right, and the vertical amplifier, at the lower right, which includes the video filter.

for example), the relationship is $S/TB^2=0.22$. The two formulas are identical when you consider that the resolution bandwidth defined at the –6-dB points, $B_{6\text{-dB}}=1.5B_{3\text{-dB}}$ (the resolution bandwidth defined at the –3-dB points), and $0.5/0.22=1.5^2$. This relationship holds for the normal spectrum-analyzer default setting where the video-filter bandwidth is equal to or greater than the resolution bandwidth. Real spectrum analyzers sweep about 25% slower than the theory predicts. Thus, for the Tektronix 2784 spectrum analyzer at a 100-MHz span and 100-kHz resolution, the actual time is 57 msec, whereas the computed sweep time is 45 msec. Similar results will be found for other settings and other spectrum analyzers.

The above is based on the assumption that amplitude must be measured accurately. Sweep time can be significantly reduced when amplitude-measurement accuracy is not critical. As **Refs 1** and **2**) show, a slight degradation in amplitude accuracy permits a sweep-time improvement of up to 5 times; if you can accept an amplitude-accuracy loss of about 3 dB, a 10-times sweep-time reduction is frequently possible.

The spectrum-analyzer circuit following the detector is known as the video filter. The video filter's bandwidth—when it is wider than the resolution bandwidth that precedes the detector—is not a factor in determining the sweep time. A relatively narrow video bandwidth, however, does affect sweep time, because the video filter must faithfully reproduce the amplitude of a pulse of duration t=BT/S (**Ref 2**).

In the previous example, S=100 MHz, B=100 kHz, and T=45 msec, so t=45 μsec. To determine the bandwidth of a lowpass filter that will faithfully reproduce the amplitude of this pulse, remember that for a simple RC filter, the product of rise time and bandwidth equals 0.35. This means that a 7.8-kHz filter has a 45-μsec rise time. The usual rule is that the filter output reaches the pulse's full peak amplitude in five rise times.

In the example, a pulse passed through the 100-kHz-bandwidth filter has more than 10 rise times to reach its final value. Thus, a 100-kHz video-filter bandwidth is more than sufficient to reproduce the output of a 100-kHz resolution filter without need for a change in sweep time. This is not the case for a much narrower video-filter bandwidth, such as 10 kHz.

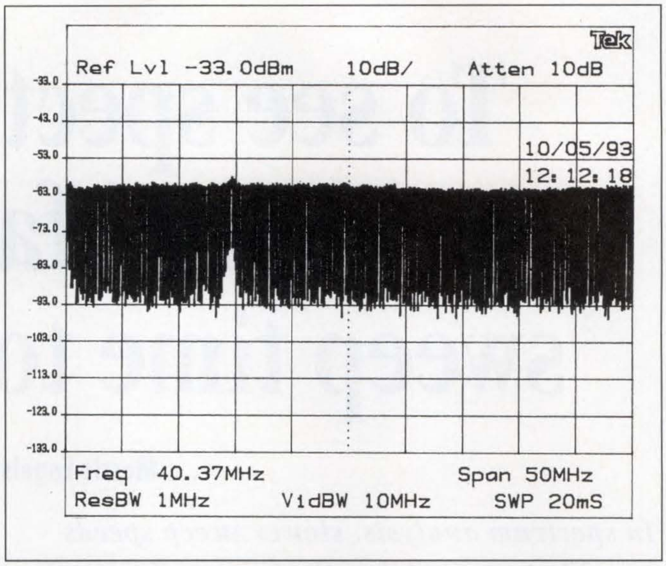

Fig 3—Mixing a sine wave with pulses yields a spectrum in which the presence of the sine wave is barely discernible.

Automatic settings emphasize accuracy

The sweep time on the Tektronix 2782 spectrum analyzer slows to 200 msec when the video bandwidth is reduced to 10 kHz for a 100-kHz resolution and 100-MHz span. At t=BT/S, the video filter must reproduce a 200-μsec pulse, which yields a 1.75-kHz video bandwidth for one time constant at a 0.35 product. The usual convention is that you need about five time constants to reproduce a pulse shape properly. A 10-kHz video-filter bandwidth fits this profile at 10/1.75=5.7 time constants.

Sweep time (T), span (S), resolution bandwidth (B), and video-filter bandwidth (V) are changed in steps rather than continuously. Also, different instruments may use different filter types or numbers of sections. Therefore, actual spectrum-analyzer settings may differ from each other or from theoretically calculated values. Actual settings approximate those shown in **Table 1.** Note that the 3- and 6-dB bandwidth relationships are the same when you take into account that the 6- and 3-dB bandwidths differ by a factor of 1.5.

These are the default values that the spectrum analyzer is preset to follow. **Ref 1** shows that a sweep-time reduction of up to 10 times compared with default settings is sometimes possible

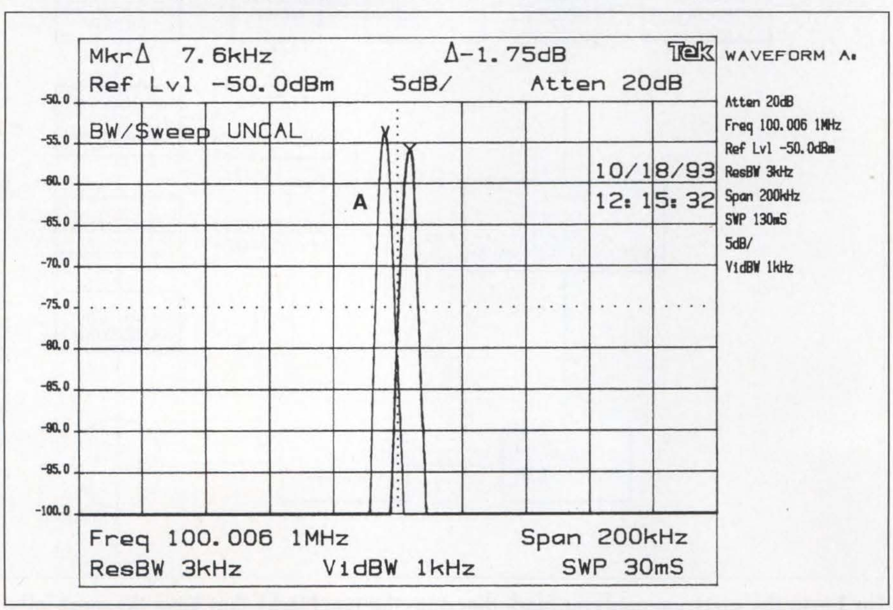

Fig 2—Reducing the sweep time from a theoretically correct 130 msec (left trace) to 30 msec (too fast a sweep to yield good amplitude accuracy) produces a response 1.75 dB too low (right trace), but speeds the sweep by a factor of 4.3.

SPECTRUM ANALYSIS

with only a minor loss in amplitude-measurement accuracy. You can achieve good accuracy at higher sweep speeds by manually setting T, B, and V independently of each other, although the instrument will show an error message when you violate the preset relationships in this way.

Fig 2 illustrates some of this discussion. A span of 200 kHz with 3-kHz resolution bandwidth and 1-kHz video-filter bandwidth provides a spectrum display of a 100-MHz sine wave at a 130-msec sweep time. The sweep time computed from the formula for 6-dB-bandwidth-based spectrum analyzers is in good agreement at 133 msec. The second trace, showing a lower-amplitude display, was obtained at a 30-msec sweep time. The 2782 spectrum analyzer is no longer amplitude-calibrated, as indicated by the UNCAL error message near the upper left corner of the screen. An amplitude comparison shows that the absolute amplitude level is in error by 1.75 dB, which would be unacceptable in many applications. Note, however, that if you don't need to measure the amplitude accurately, these settings reduce the measurement time by a factor of 130/30=4.3.

Table 1—How spectrum-analyzer sweep time varies with bandwidth

Bandwidth definition	6 dB	3 dB
V≥B	$T=S/0.22B^2$	$T=S/0.50B^2$
V<B	T=S/0.50BV	T=S/0.33BV

Note: These formulas are approximate. A different type of derivation shows a 3-dB bandwidth relationship of S/TBV=0.55 (**Ref 5**). Whatever the assumptions, however, the results are similar.

Detector function

Sweep-time limitations discussed so far are determined by how fast a signal can be swept through a filter. The filter bandwidth is the dominant sweep-speed factor when the instrument is set to respond to the peak level of the signal. This is not the case for quasi-peak (QP) and average-signal measurements.

The QP detector, used for EMI measurements, is extremely slow. There are two ways to reduce the measurement time for such measurements. One way is to use the much faster peak detector instead of the QP detector. This is perfectly legal because peak-detector results always show a level at least as high as QP results. Hence, a device that fails interference- acceptance limits in QP also fails in peak-detection mode. The incentive for using the QP mode is that some devices fail acceptance testing in peak but are perfectly all right in QP. Therefore, when measurement time is important, it is a good idea to use peak as the primary measurement mode and retest in QP when a peak measurement is out of spec (**Refs 3** and **4**).

Sometimes, the signal characteristics are such that the QP detector can be swept much faster than normal with very little degradation in amplitude accuracy. As discussed in **Ref 3**, by avoiding QP whenever possible and by using a faster-than-normal sweep for some signals, you can achieve speed increases of 10 times or more in most measurements that require the use of QP.

Averaging, no matter how it is done, requires a certain amount of time. You cannot perform averaging measurements as fast as peak measurements. However, you can save much time by choosing an optimum averaging technique based on the application and accuracy requirements. Several procedures discussed in **Refs 4**, **5**, and **6** are summarized below.

To speed averaging, try a log display

A common averaging procedure is to set the spectrum analyzer for a narrow video-filter bandwidth. However, sweep time is inversely proportional to video bandwidth. Consequently, the greater the degree of averaging, the longer the sweep takes. In theory, to obtain a correct average value, the averaging should be performed in the linear

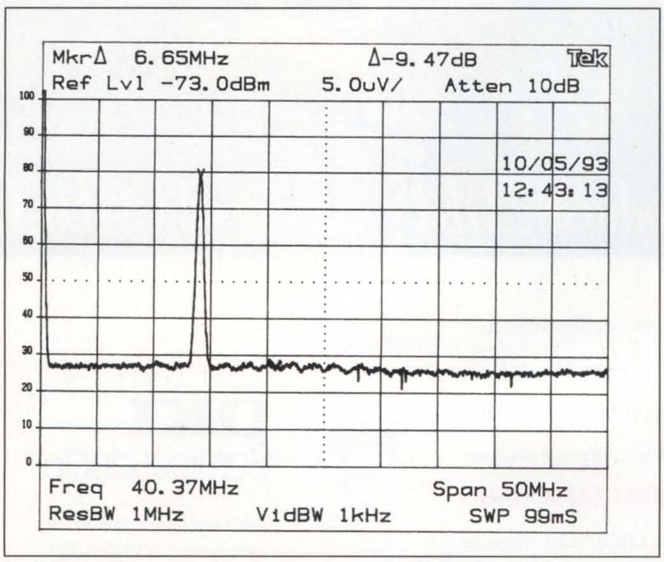

Fig 4—Reducing the video-filter bandwidth to 1 kHz reduces the amplitude of the pulse spectrum by averaging, and the sine wave shows at 9.47 dB above the averaged pulse-spectrum level. The sweep time increased to 99 msec compared with Fig 3's 20 msec, however.

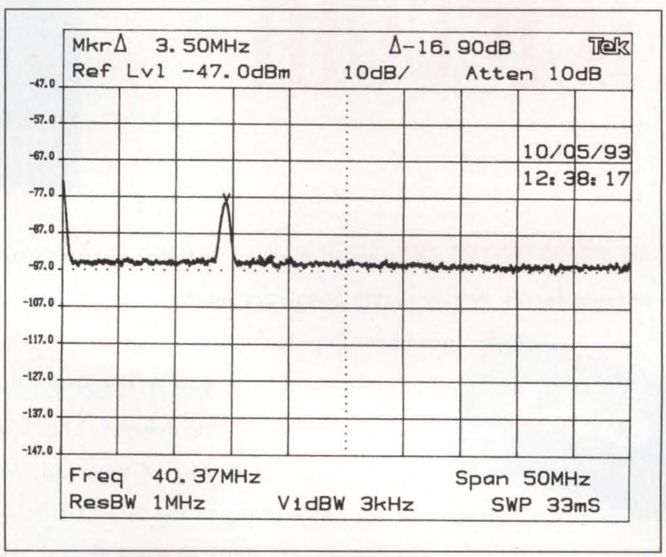

Fig 5—This trace, which was taken at 10 dB/div in log mode, shows an improved signal ratio of 16.9 dB. This was obtained at a video-filter bandwidth of 3 kHz and a sweep time of 33 msec.

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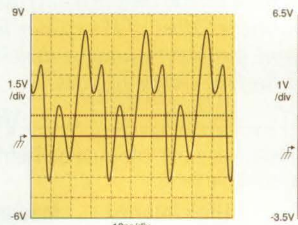

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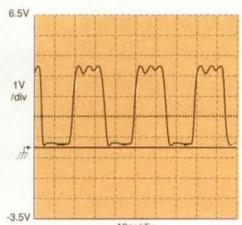

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SPECTRUM ANALYSIS

vertical mode. Nevertheless, averaging a logarithmically compressed signal is almost as accurate as linear processing, and the video bandwidth can be five or more times as wide (**Refs 4** and **5**). Log-mode averaging, therefore, significantly reduces measurement time at a small cost in accuracy.

The plots in **Figs 3** and **4** illustrate the improvement in averaging by using a logarithmic display. **Fig 3** shows a combination of pulsed and continuous-wave signal spectra. The sine wave is barely discernible within the pulse-spectrum distribution. In **Fig 4**, reducing the video-filter bandwidth to 1 kHz reduces the amplitude of the pulse spectrum by averaging, and the sine wave shows at 9.47 dB above the averaged pulse-spectrum level. The sweep time increases to 99 msec compared with **Fig 3**'s 20 msec. **Fig 5**, which was taken at 10 dB/div in log mode, shows an improved signal ratio of 16.9 dB. This was obtained at a video-filter bandwidth of 3 kHz and a sweep time of 33 msec. Thus, a 10-dB/div log display produces better averaging than does the linear mode (16.9 vs 9.47 dB), yet the video bandwidth is wider and the sweep time is less by a factor of three.

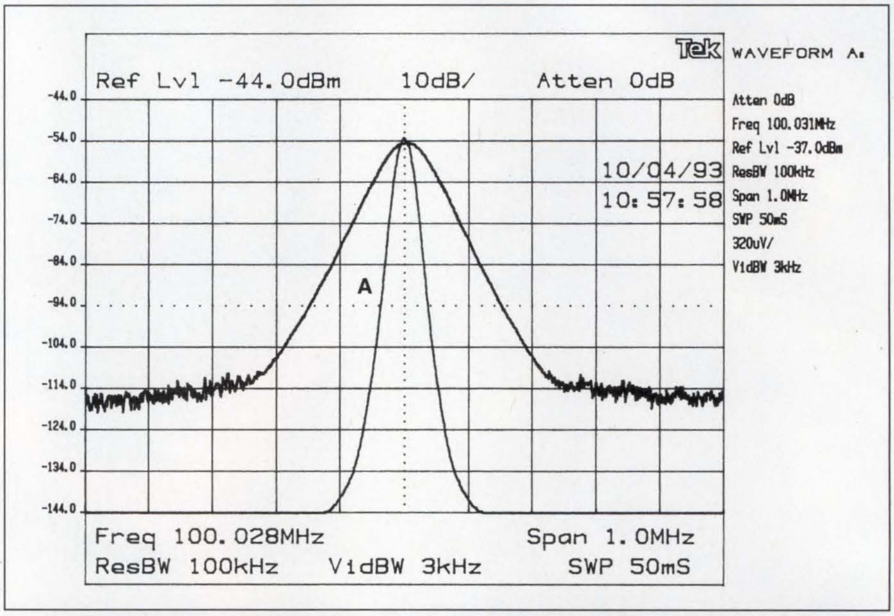

Fig 6—The same sine-wave signal spectrum appears wider in the (outer) logarithmic-mode display than in the (inner) linear display.

Although video-filter averaging is the usual procedure, most spectrum analyzers also provide various means of averaging spectra digitally. Sometimes the digital processing is more effective or faster than the analog technique of using a narrow video filter. One way to save measurement time is to use digital and analog video-filter averaging simultaneously. For the Tektronix 2794 spectrum analyzer, for example, 100 msec of digital averaging is equivalent to using a 5-kHz-wide video filter (**Ref 6**). Thus, at a 50-MHz span, 100-kHz resolution bandwidth, and 10-kHz video-filter bandwidth, the sweep time is 100 msec, as computed from S/TBV=0.5. Simultaneously performing digital and video-filter averaging to achieve the equivalent of a 5-kHz video bandwidth takes no extra time. The combination of 10-kHz video and 5-kHz digital filtering provides a bandwidth of less than 4 kHz without increasing the measurement time.

Additional factors

As noted previously, a logarithmic display permits faster signal averaging than is possible in the linear vertical mode. Indeed, the logarithmic vertical mode permits a faster sweep than a linear display even at wide video bandwidth, because the width and rise time of the previously discussed t=BT/S pulse increase as the spectrum is compressed in the logarithmic display. Note in **Fig 6** how the same sine-wave signal spectrum appears wider in the (outer) logarithmic-mode display than in the (inner) linear display.

Finally, note an important relationship between measurement sweep time and signal-detection sensitivity. Pulling a small sine-wave signal out of noise requires a very narrow resolution bandwidth, which results in a long sweep time. An input-signal preamplifier increases the signal level so that a wider bandwidth and less measurement time do the job (**Ref 7**). EDN

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Author's biography

Morris Engelson is a fellow of the IEEE. He is a consultant with JMS in Portland, OR, and is affiliated with Tektronix Inc in nearby Beaverton. Engelson holds bachelor's and master's degrees in EE and is a certified electromagnetic-compatibility engineer. Most of his career has been spent in designing spectrum analyzers and in developing techniques for measuring radio-frequency signals.

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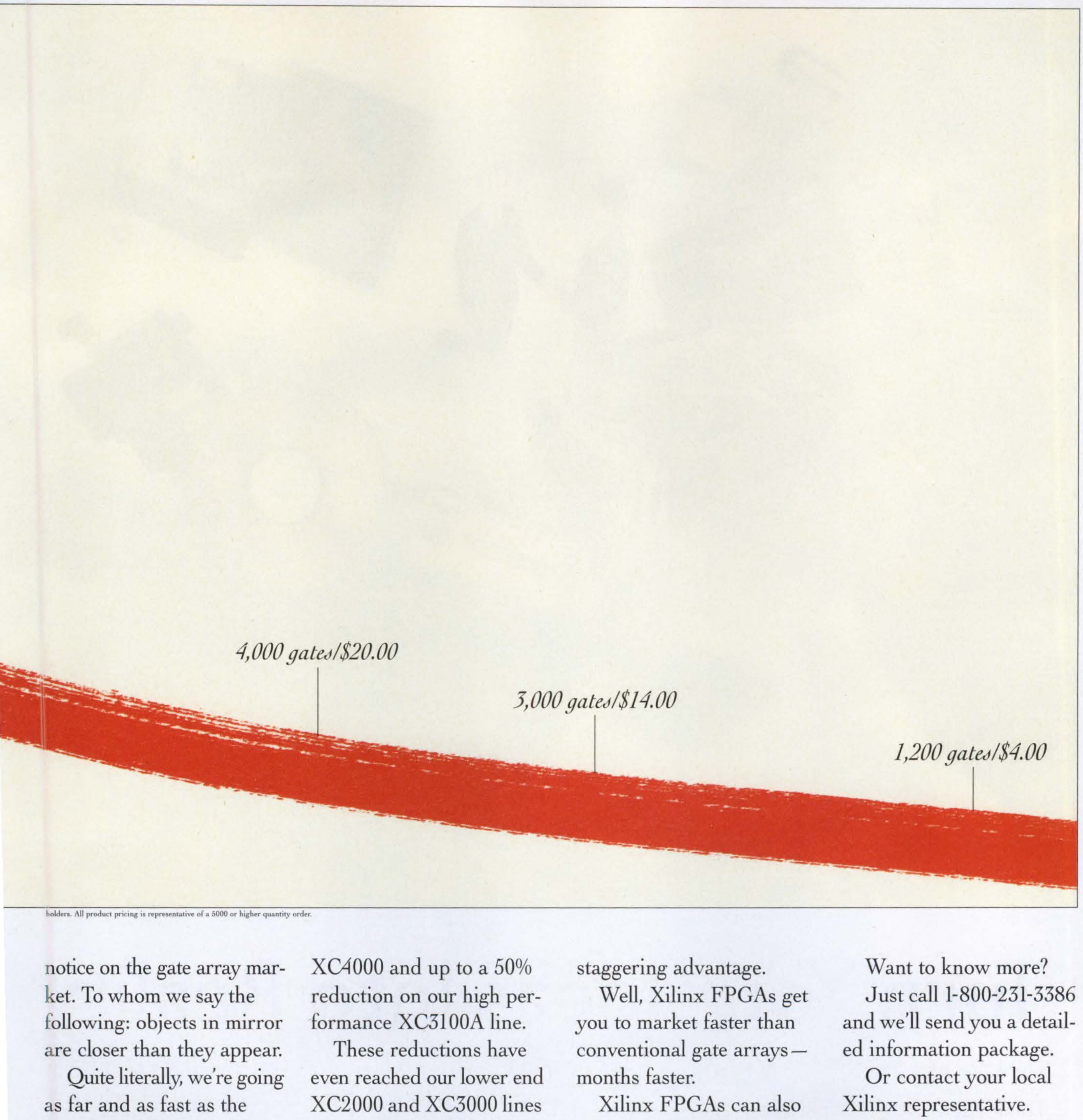

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Weigh the benefits of fuzzy-logic vs classical control in a disk-drive spindle

Brian P Tremaine, Seagate Technology

You can apply fuzzy- and classical-control techniques to any servo-control loop. Which technique you use depends heavily on the nonlinearities in a system.

A furor is raging over whether you should use fuzzy-logic or classical-control tools to analyze a complex servo-control system. Fuzzy-logic advocates claim it eliminates the need for a mathematical system description, while classical-control advocates claim fuzzy logic's lack of analysis tools makes it undesirable. To observe these extreme views, compare the classical- and fuzzy-control analysis of a disk-drive dc spindle motor. The comparison uses a C program, which simulates the plant and classical feedback-control signal.

The FIDE (fuzzy inference-development) program from Aptronix Inc compiles the plant program to simulate a fuzzy controller. The spindle-motor example shows that even a basic system can have nonlinearities, which preclude linear analysis. However, knowledge of the system equations can aid the design of a fuzzy controller.

The dc spindle motor, driver electronics, and digital transducers comprise the system's plant and are inherently nonlinear. The driver develops only positive torque, which is a common practice in disk-drive applications. Therefore, the motor depends only on coulomb friction to decelerate. The plant's nonlinearities include saturation of the error signal, torque control in only one quadrant, and quantization of the transducer signals from the output control voltage. Therefore, linear-analysis methods do not apply for either the classical or fuzzy set of control tools. This analysis compares the differences between a classical proportional plus integral (PI) controller and a fuzzy controller.

The plant model (**Fig 1**) is a dc 3-phase, 12-pole spindle motor along with the driver electronics. The output circuitry comprises three half-bridge drivers with current-sense feedback. The input to the driver is an analog voltage, which generates the spindle motor current through a current amplifier having a gain of gm (amps/volt). When the input voltage equals some reference voltage, the current command is zero, and the output stages are off. During this time, coulomb friction decelerates the motor. Maximum current drive occurs when the input voltage is at 0V. The motor resistance, supply voltage, and the back EMF from the motor limit the maximum current drive to the motor.

Simulator doesn't model current control

The current-control loop around the motor and the current amplifier typically have a bandwidth several orders of magnitude greater than the motor's velocity bandwidth. There-

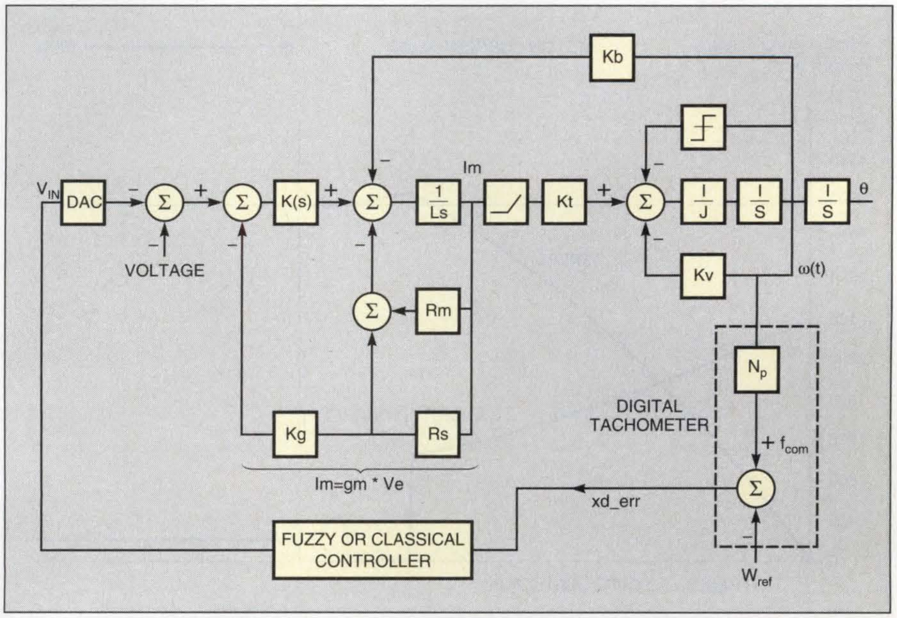

Fig 1—The block diagram of the plant for a 3-phase, 12-pole spindle motor comprises a current amplifier driving the motor and half-bridge output drivers with current-sensing feedback.

FUZZY AND CLASSICAL CONTROL

fore, the plant simulation doesn't include the dynamics of the current-control loop in **Fig 1**. Instead, the plant model calculates the maximum available current and drives the motor using a current source, which is equal to either the commanded current or the maximum available current, whichever is smaller.

The classical-control analysis applies linearization to the nonlinear plant to design a proportional PI controller. The linear model does not predict the correct simulated transient response. The simulated plant model calculates motor speed in rad/sec, position in rad, and a digital encoder pulse, called f_{com}. A digital tachometer and digital phase detector use the f_{com} signal, which occurs nine times/revolution of the motor (N_p=9). The linearized transfer function of the motor and current driver in continuous time is:

$$H(s)=(gm\cdot Kt/Jm)/(s+Kv/Jm),\ \text{rad/sec}\cdot V, \qquad \textbf{(1)}$$

where gm=0.5 A/V, transconductance; Kt=1.05 oz-in./A, torque constant; Kv=0.001 oz-in./sec, viscous constant; and Jm=752E–6 oz-in.-sec^2, inertia.

The equation represents the transfer function from the input voltage to the motor's radial velocity output. Because the tachometer's outputs are discrete, the continuous-time representation is converted to discrete time using the z-transform. The transform involves an approximation because the sample interval is at a fixed motor rotation ($2\pi/N_p$) and not at a fixed sample time. As a practical matter, the discrete system is often analyzed assuming T is a fixed sample time. Although we make this approximation, linearizing the system and assuming a fixed sample time completely ignores the real system's nonlinearity. Stability of the linearized system does not ensure global stability of the real system. An appropriate Lyaponov function could determine a nonlinear system's degree of stability. Finding such a Lyaponov function is difficult, however.

You can derive a difference equation directly from **Eq 1** by assuming a small time increment, as follows:

$$(\omega(t+dt)=(1-dt\cdot(Kv/Jm))\cdot\omega(t)+(gm\cdot Kt\cdot dt/Jm)\cdot v(t). \qquad \textbf{(2)}$$

If dt=T and t=kT, then **Eq 2** becomes

$$(\omega(kT+T=(1-T\cdot(Kv/Jm))\cdot\omega(kT)+(gm\cdot Kt\cdot T/Jm)\cdot v(kT).$$

Noting that the z-transform of ω(kT+T is $\omega(z)\cdot z$, the overall transfer function is

$$H(z)=gm\cdot Kt\cdot T/Jm)/(z-(1-T\cdot Kv/Jm)),\ \text{rad/sec}\cdot V. \qquad \textbf{(4)}$$

Digital tachometer provides feedback

Regardless of whether the controller is classical or fuzzy, you must measure the spindle speed for feedback control. **Fig 1** includes a block diagram labeled "digital tachometer" showing the measurement of the spindle speed, ω(t). The output of this block is xd_err, a digital word representing speed error.

The digital tachometer counts the period of the f_{com} pulse with 1-μsec resolution (t_i). You subtract the final count from a reference count of 1880. The tachometer then truncates the count to fall within –128 to +127 counts to generate the xd_err signal. If the time interval is T_t and the average velocity over an f_{com} period is w_{avg}, then $w_{avg}(T_t)$ is the average velocity over the time interval:

$$\omega_{avg}(T_t)=2\cdot\pi/(N_p\cdot T_t). \qquad \textbf{(5)}$$

This equation is nonlinear in the variable T_t. To linearize the equation, you can write a Taylor series around the reference velocity ω_{ref} and the reference period T_t. You linearize a function using a Taylor series about an equilibrium point. If you linearize f(x,t about the point x0, then the first tw terms of the Taylor series are

$$f(x,t)=f(x0,t)+f'(x0,t)(x-x0),$$

where f' denotes the derivative wit respect to x. Applying this to **Eq** yields

$$\omega_{avg}(T_t)=\omega_{ref}-(\omega_{ref}/T_{ref})*(T_t-T_{ref}). \qquad \textbf{(7}$$

Because $\omega_{avg}(T_t)$ is the average veloci over the period T_t, you can express th equation in terms of the velocity at t beginning and the end of the period, follows:

$$\omega_{avg}(k)=(1/2)\cdot(\omega(k)+\omega(k-1)). \qquad ($$

Combining **Eqs 7** and **8** yields

$$(\omega(k)-\omega_{ref}+(\omega(k\text{-}1)-\omega_{ref})-2'(\omega_{ref}/T_{ref})\cdot t_t-T_{ref}). \qquad ($$

Denoting the difference between w a ω_{ref} as ω_e and measuring the time int val in terms of t_i reduces **Eq 9** to

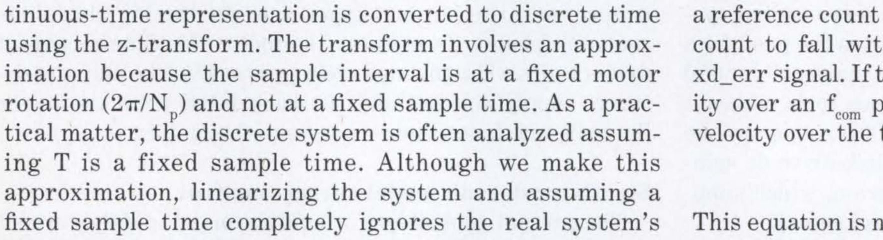

Fig 2—Driving a spindle motor from a dead stop to a final spindle speed using a classical proportional integral (PI) controller shows a severe target overshoot. The integrator shuts off the motor current at Point 2 to allow the motor to settle using coulomb friction.

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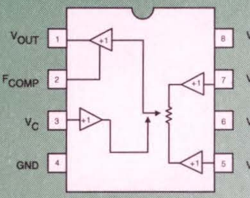

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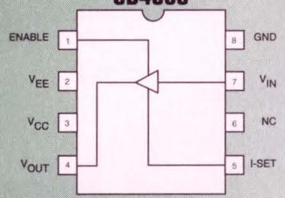

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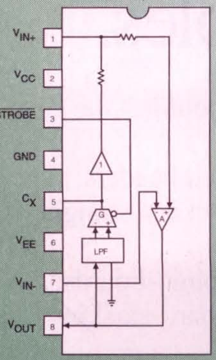

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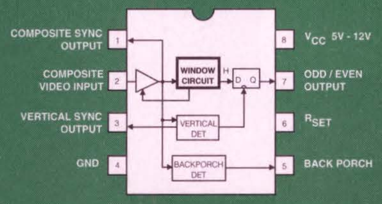

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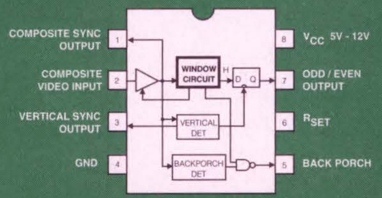

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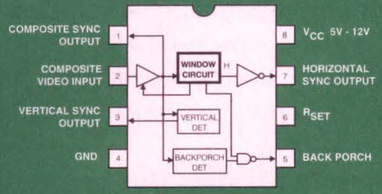

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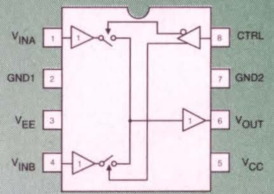

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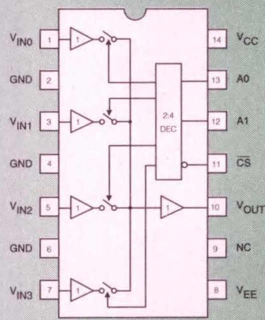

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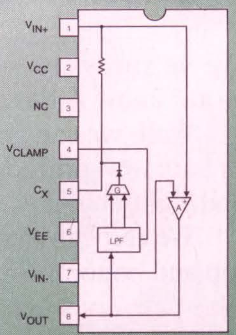

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FUZZY AND CLASSICAL CONTROL

$$\omega e(k)+\omega e(k-1=-2\cdot(\omega_{ref}/T_{ref})\cdot t_i\cdot d(k), \quad \textbf{(10)}$$

where d(k) is the digital count of the time interval.

The z-transform for **Eq 10** is the transfer function of the digital tachometer, as follows:

$$\omega e(z)+\omega e(z)/z=-2\cdot(\omega_{ref}/T_{ref})\cdot(T_t-t_i\cdot d(z).$$
$$D(z)=d(z)/\omega e(z)=-T_{ref}/(2\cdot\omega_{ref}\cdot t_i))\cdot 1+z)/z.$$

If the motor velocity is significantly different from the reference frequency (ω_{ref}), the Taylor series expansion is no longer accurate. In addition, if the velocity is low, the sample time is long, and the phase delay of D(z) is long.

The plant-transfer function in **Eq 1** has a maximum phase delay of 90°. Even when you represent **Eq 1** in discrete form (**Eq 4**), the closed-loop bandwidth is sufficiently below the Nyquist frequency, 1/T, that the phase delay caused by sampling is small. Therefore, you can stabilize the plant using only proportional feedback from the tachometer. However, the speed error is not exactly zero. Offsets in the driver stage and motor running torque relative to the driver input requires a speed error to counteract the offsets.

To force the speed error to zero, classical feedback-control systems sum the speed error and the time integral of the speed error (PI) to generate the feedback-control law. The control-law calculation for a discrete time system follows:

$$\text{Vint}(k)=\text{Vint}(k-1+k_i\cdot \text{xd\_err}(k); \quad \textbf{(13)}$$

$$\text{Vout}(k)=k_p\cdot \text{xd\_err}(k)+\text{Vint}(k), \quad \textbf{(14)}$$

where xd_err is the digital word representing speed error. **Eq 13** is the difference equation for the digital integrator, and **Eq 14** is the linear sum of the speed error and time integral of the speed error. You can combine **Eqs 13** and **14** into a transfer function in the z-domain for the equivalent digital controller, C(z), as follows:

$$C(z)=\text{Vout}(z)/\text{xd\_err}(z)=kp+ki\cdot z/(z-1).$$

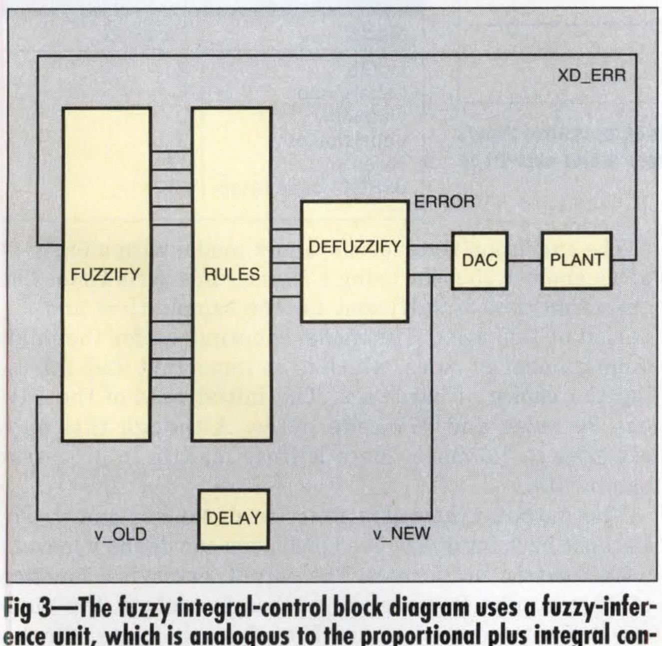

Fig 3—The fuzzy integral-control block diagram uses a fuzzy-inference unit, which is analogous to the proportional plus integral control of classical methods.

The open-loop gain of the linearized system is

$$H(z)\cdot C(z)\cdot D(z),\ Gol(z)=D(z)\cdot((k_p+k_i)\cdot gm\ K_t\cdot T/J_m)\cdot (z-k_p)/(k_p+k_i))/[z-(1-T\cdot Kv/Jm))\cdot(z-1)]. \quad \textbf{(17)}$$

Substituting some of the system parameters into **Eq 17** yields open-loop poles as z1=1, and z2=0.99. The digital tachometer produces a pole at z=0 and a zero at z=–1. The ratio of the integral gain to proportional gain determines the zero at $z=1/(1+k_i/k_p)$.

The linearized model predicts closed-loop poles that are well-damped for small k_i/k_p and under-damped for large k_i/k_p. This result is in contrast to the simulation results (**Fig 2**) and highlights the fact that nonlinearities in a system can invalidate the use of linear methods.

Fig 2 shows a plot of the simulated spindle speed using a

```
$ SPINDLE disk drive spindle PI control
$ brian tremaine 6 July 1993, revised 1 Jan. 1994
fiu tvfi (min max) ;

>xd_err "bits":-128()127 [
    Neg_Large (@-128,255, @-64,0),
    Neg_Med   (@-128,0,   @-64,255, @0,0),
    Zero      (@-64,0,    @0,255,   @64,0),
    Pos_Med   (@0,0,      @64,255,  @127,0),
    Pos_Large (@64,0,     @127,255)];

>v_old "bits":0()255 [
    Neg_Large (@0,255,   @64,0),
    Neg_Med   (@0,0,     @64,255,  @128,0),
    Zero      (@64,0,    @128,255, @192,0),
    Pos_Med   (@128,0,   @192,255, @255,0),
    Pos_Large (@192,0,   @255,255) ];

<error "bits": 0()255* (
      Neg_Large = 0.0,
      Neg_Med =   8,
      Zero =      128,
      Pos_Small = 248,
      Pos_Large = 255 );

<v_new "bits": 0()255* (
      Neg_Large = 0.0,
      Neg_Med =   64,
      Zero =      128,
      Pos_Med =   192,
      Pos_Large = 255 );
$
if xd_err is Neg_Large                               then v_new is Neg_Large;
if xd_err is Neg_Med                                 then v_new is Neg_Large;
if xd_err is Zero and v_old is Pos_Large             then v_new is Pos_Large;
if xd_err is Zero and v_old is Pos_Med               then v_new is Pos_Med;
if xd_err is Zero and v_old is Zero                  then v_new is Zero;
if xd_err is Zero and v_old is Neg_Med               then v_new is Neg_Med;
if xd_err is Zero and v_old is Neg_Large             then v_new is Neg_Large;
if xd_err is Pos_Med and v_old is Pos_Med            then v_new is Pos_Large;
if xd_err is Pos_Med and v_old is Zero               then v_new is Pos_Med;
if xd_err is Pos_Med and v_old is Neg_Med            then v_new is Zero;
if xd_err is Pos_Med and v_old is Neg_Large          then v_new is Neg_Med;
if xd_err is Pos_Large                               then v_new is Pos_Large;
$
if xd_err is Neg_Large                               then error is Neg_Large;
if xd_err is Neg_Med                                 then error is Neg_Med;
if xd_err is Zero                                    then error is Zero;
if xd_err is Pos_Med                                 then error is Pos_Small;
if xd_err is Pos_Large                               then error is Pos_Large;
end
```

Fig 4—The listing for the fuzzy controller of the spindle disk drive is compiled with Aptronix's FIDE (fuzzy inference development) program.

FUZZY AND CLASSICAL CONTROL

		V_OLD				
		NEG_LARGE	NEG_MED	ZERO	POS_MED	POS_LARGE
	NEG_LARGE	NL/NL	NL/NL	NL/NL	NL/NL	NL/NL
	NEG_MED	NL/NM	NL/NM	NL/NM	NL/NM	NL/NM
XD_ERR	ZERO	NL/ZR	NM/ZR	ZR/ZR	PM/ZR	PL/ZR
	POS_MED	NM/PM	ZR/PM	PM/PM	PL/PM	/PM
	POS_LARGE	PL/PL	PL/PL	PL/PL	PL/PL	PL/PL

OUTPUT LEGEND: v_new/error
NL = NEG_LARGE
NM = NEG_MED
ZR = ZERO
PM = POS_MED
PL = POS_LARGE

Fig 5—The rule table for the fuzzy integral controller contains redundant rows of rules that can be condensed into fewer rules for the fuzzy-inference unit to follow.

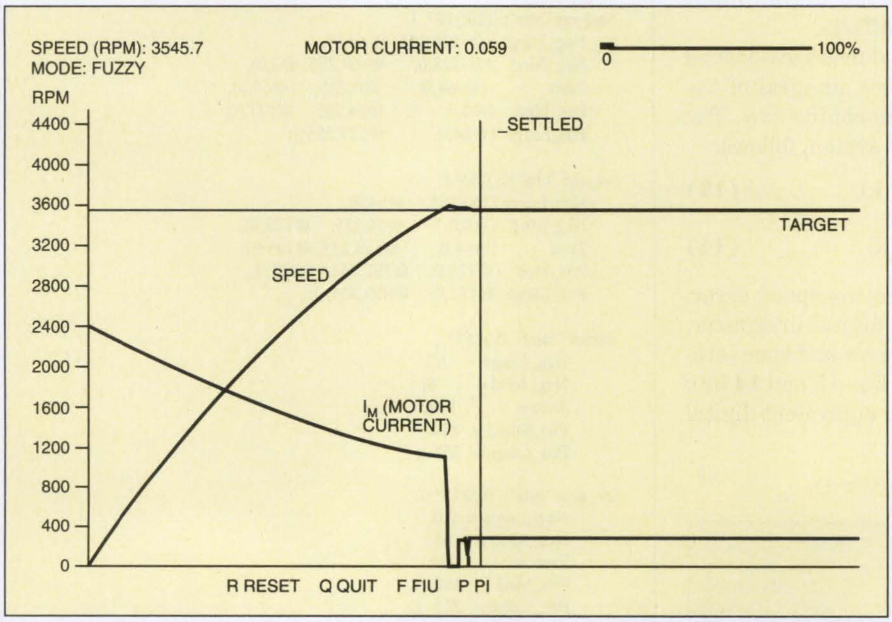

Fig 6—The spin-up of the spindle motor from a dead stop using fuzzy integral control shows less overshoot than with a classical PI controller. The integrator reduces motor current to zero when the system is over speed to cause deceleration.

classical PI controller with a nonlinear plant. In **Eqs 13** and **14**, k_i=3/2048, and k_p=48/2048. The speed overshoots the target and slowly decays with a linear ramp to the target speed value. From time t=0 until Point 1, the speed error is negative, and the integrator continues to accumulate until it saturates. Not until the speed error begins to go positive does the integrator begin to come out of saturation. At Point 2 the integrator has recovered enough to allow the control voltage to command zero current. From Point 2 until Point 3 the only deceleration is due to coulomb friction. Beyond Point 3, the system settles to a steady state value.

Fuzzy control uses different control blocks

Fuzzy integral control analyzes the spindle motor using a fuzzy-inference unit (FIU) (**Fig 3**). This analysis block is analogous to the proportional plus integral control block of the classical method. Because an FIU has no memory, fuzzy control accomplishes the integral function by using the feedback from the FIU's output to its input. The FIU has the FIDE listing shown in **Fig 4**. The inputs to the FIU are the speed error (xd_err) and previous output integral count (V_old). The outputs of the FIU are proportional count (error) and integral count (V_new). **Fig 5 shows** a table representation of the FIU rules. The control law is a summation of both outputs

$$\text{Vout}=16\cdot(\text{error}-128)/255+3$$
$$(\text{v\_new}-128)/255+3.$$

Fig 6 shows a plot of motor speed and current for spin-up from a dead stop. The steady state speed nearly equals the commanded speed, as in the integral controller. However, the fuzzy method improves transient response, decreases overshoot, and provides faster settling. A classical PI system involves a tradeoff between overshoot and settling time. The fuzzy-system rules and membership functions effectively implement "anti-windup" integral control. When xd_err is positive, (over speed) the integral term (v_new) is forced positive to zero the spindle-motor current immediately to cause deceleration.

Table 1 details the fuzzy model:

Table 1—The fuzzy model

Model	Fuzzy PI
Inputs	2
Labels/input	5
Outputs	2
Labels/output	5
Rules	17
68HC11 code bytes	717

The execution time for the above model with a 68HC11 μP is about 1.25 msec using a 50-nsec bus cycle time. The execution time is sufficient for the sample time and f_{com} period of 1.88 msec. The model is optimized for the minimum number of rules, which is an important step affecting the choice of hardware. The initial pass of the FIU has 30 rules and 877 code bytes. Although this pass executes in 1.6 msec, there is little margin in processor bandwidth.

The output v_new is a function of xd_err and v_old. Because each input has five labels, you can define v_new as a 5×5 matrix, or 25 rules. The output, error, is a function of xd_err only. Because xd_err has five labels, five rules can define the output, error. Therefore, there are 30 rules for the the first pass. In the last row of **Fig 5**, when xd_err

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FUZZY AND CLASSICAL CONTROL

is Pos_Large, V_new is Pos_Large, regardless of v_old. This condition lets you replace five rules with one rule: "If xd_err is Pos_Large, then v_new is Pos_Large." Modifications such as these can reduce the number of rules from 30 to 17.

In comparing a classical PI servo-control loop with a fuzzy-control loop for a dc spindle motor, the plant and the tachometer have inherent nonlinearities that preclude applying linear stability theory, regardless of the control method. Knowledge of classical PI servo-control principles helps with the design of a fuzzy controller. The performance in terms of the spin-up settling time and the transient response is superior using the fuzzy system compared with the classical PI controller when there are severe nonlinearities.

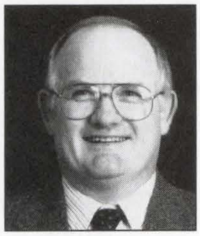
The C source code for both the FIDE fuzzy modules and the plant model is available from the author. In addition to the PI controller, you can also use the Aptronix bulletin-board system to access source and executable simulation code for proportional control, PLL control, and dual-phase and tachometer loops for classical and fuzzy control. EDN

References

1. Kosko, B, *Neural Networks and Fuzzy Systems: A Dynamical Systems Approach to Machine Intelligence*, Prentice Hall, 1992.

2. Franklin, G, D Powel, and M Workman, *Digital Control of Dynamic Systems*, Second Edition, Addison Wesley, 1990.

Author's biography



Brian P Tremaine is a senior engineering director for Seagate Technology in Scotts Valley, CA. His job includes managing a group that is responsible for control-system design of actuator and spindle servos on 2.5- and 1.8-in. disk files. In his nine years with Seagate, he has helped to develop a host of disk-file products. Tremaine has BSEE and MSEE degrees from San Jose State University, San Jose, and an MBA from Golden Gate University, San Francisco. He is a registered professional engineer in California, and he is completing an engineer degree at Stanford University, Stanford, CA, this year. Tremaine is married and has two children.

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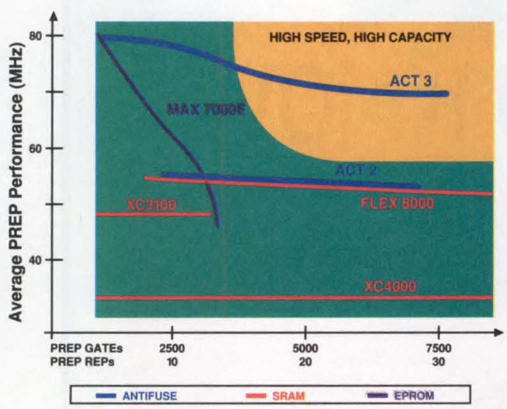

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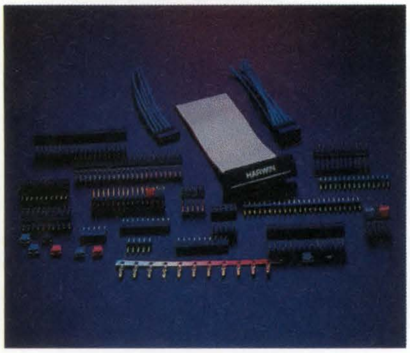

Harwin, Inc. offers a variety of solder, wire-wrap, DIL and SIL sockets. Along with reeled and loose pc board sub miniature sockets, headers, PLCC and PGA sockets. These high reliability sockets are designed to meet severe environmental conditions of high shock, vibration, bump, etc. – ideal choice for those applications where space is limited. Harwin, Inc. (812) 285-0055 FAX (812) 285-0056.

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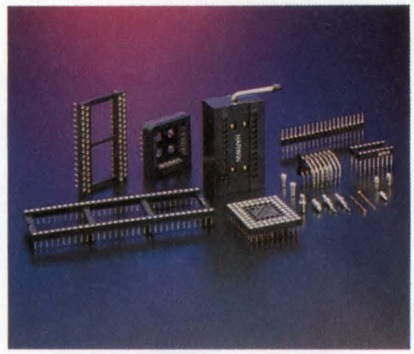
CIRCLE NO. 214

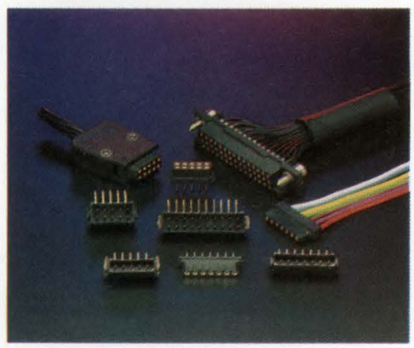
Pin Headers and Shunts on 2MM Centers



Pin headers are available from Harwin, Inc., in single and double row, 2 to 32 position lengths in both vertical and horizontal styles. A "small footprint" horizontal style is available for use where PCB space is at a premium. All versions are stocked in both gold and tin finishes. The 2mm shunts are designed with a low initial point of contact to eliminate the possibility of intermittent contact. The body is end stackable with tapered entry for easy pin header insertion. The contacts offer low insertion force, high retention and are open top for test probe access. Both gold and tin finishes are available. Harwin, Inc. (812) 285-0055 FAX (812) 285-0056.

CIRCLE NO. 225

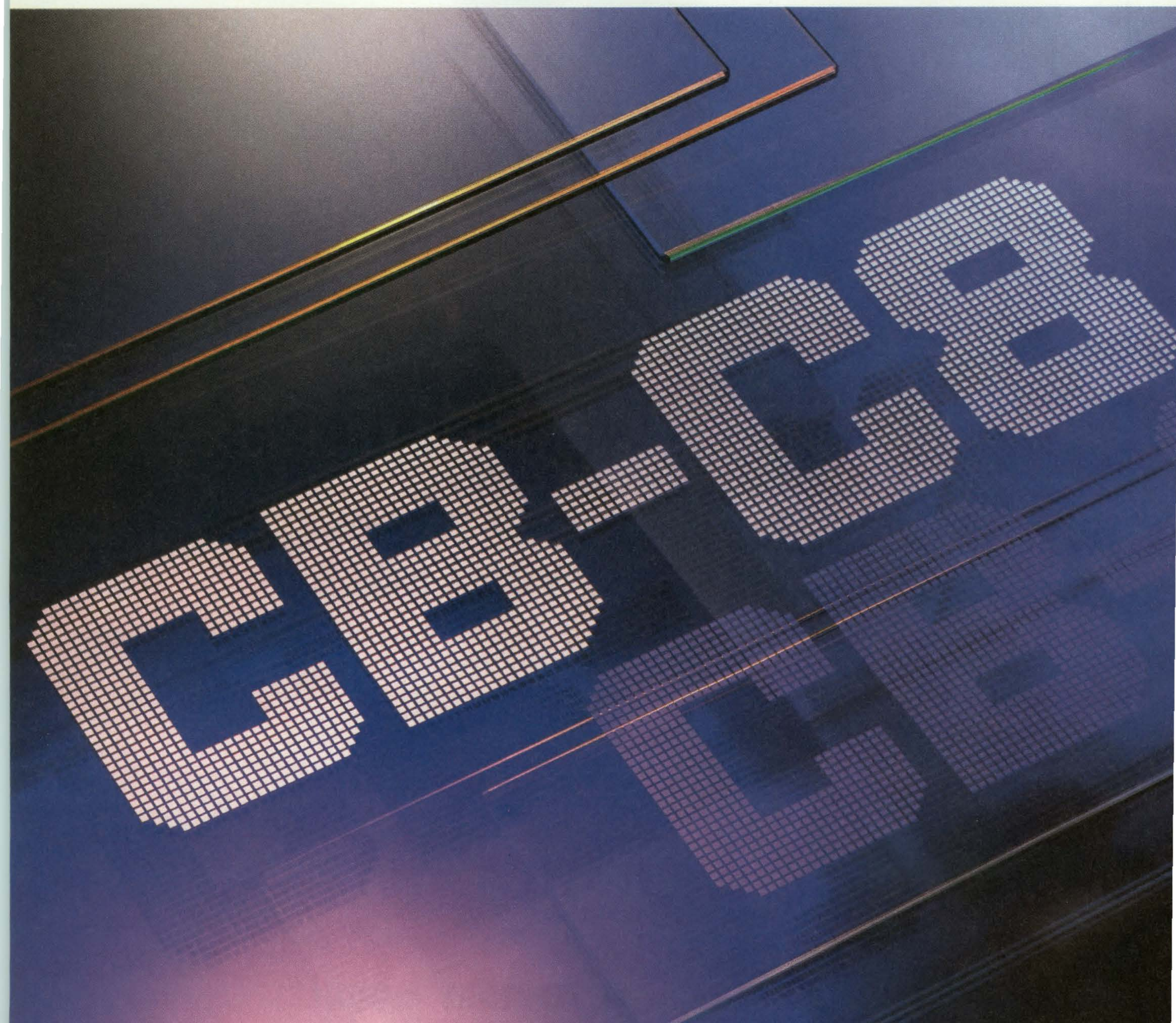
2mm High Density Connectors Available in 3 Row Versions



Harwin, Inc. announces the availability of a 3 row version of its popular connectors on 2mm centers. These "Datamate" connectors are designed for use in applications such as mobile communications,data processing, medical and military equipment where miniaturization and absolute contactintegrity is required. The high temperature moldings are produced in 27 to 63 contact versions and the range is doubled by the option of including two power contacts in each size. Additional features include polarization, shrouded contacts, selective plating, replaceable contacts, jackscrew options, small fooprint and low profile. Harwin, Inc. (812) 285-0055 FAX (812) 285-0056.

CIRCLE NO. 226

Systems on silicon enter



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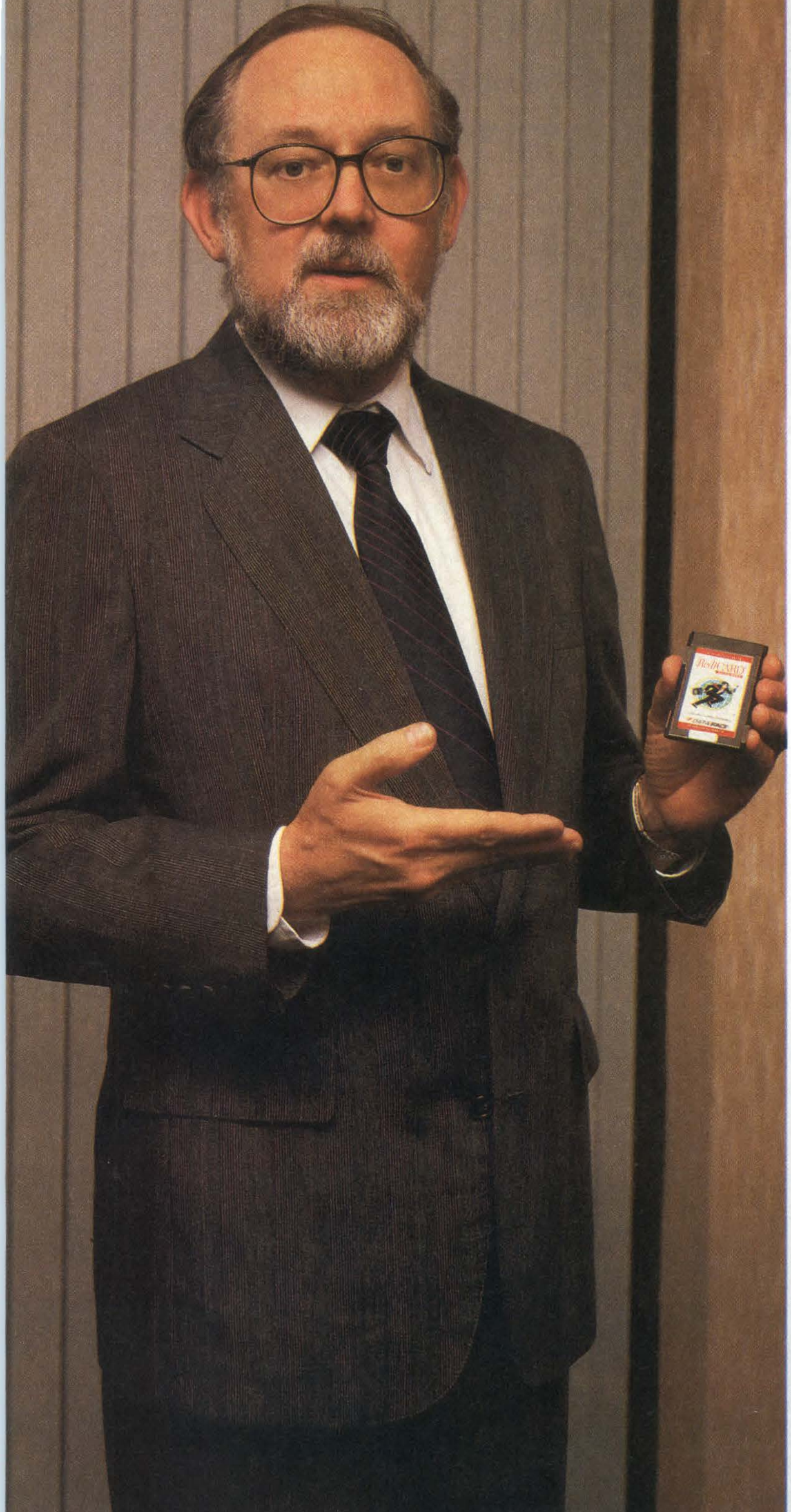

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CIRCLE NO. 188

A bevy of new workstations offers price/performance options

No fewer than four workstation makers have announced new models or new configurations of already-released models. The new offerings come from Hewlett-Packard, IBM, Sun, and Tatung. The basic packages range in price from under $5000 to over $30,000, with most in the $10,000 to $20,000 range.

IBM and HP have the more powerful workstations. IBM's RS/6000 3BT, with optional 1-Mbyte Level 2 cache, achieves a SPECfp92 rating of 205.3. Sun and Tatung, with similar units based on the microSPARC II, offer better prices. Tatung quotes a base price of $4570, but Sun's prices (around $10,000) include more hardware options.

Consult **Table 1** for more details, but bear in mind that the listings show ranges of specifications for several basic configurations. Other configurations and options are also available.—**Gary Legg**

New workstations offer powerful processing at ever lower prices. Shown here is Hewlett-Packard's HP 9000 Series 700 Model 715.

TABLE 1—WORKSTATIONS

Manufacturer	HP	IBM	Sun	Tatung
Models	HP 9000 Series 700	RS/6000 41T, 41W,	SPARCstation 5 715, 725	COMPstation II-385 3AT, 3BT
Processor	PA-RISC 7100LC Power2	80-MHz 601, microSPARC II	70-MHz, 85-MHz microSPARC II	85 MHz
SPECint92	66.6 to100.1	88.1 to 114.3	57 to 64	64
SPECfp92	96.5 to 137	98.7 to 205.3	47.3 to 54.6	54.6
Memory (Mbytes)	32	16 to 32	32	16
Maximum memory (Mbytes)	256 to 512	256 to 512	256	256
Cache (kbytes)	256	512 to 1024	24	NA
Disk (Mbytes)	525	540	535 to 1050	520
Color monitor	17 in.	17 in.	17 in.	14 in.
Price	$9995 to $19,005	$12,100 to $32,300	$9595 to $11,595	$4570

Hewlett-Packard Co, Palo Alto, CA. (800) 637-7740. **Circle No. 401**

International Business Machines Corp, Somers, NY. (800) 426-3333. **Circle No. 402**

Sun Microsystems Computer Corp, Mountain View, CA. (800) 872-4786. **Circle No. 403**

Tatung Science and Technology Inc, Milpitas, CA. (800) 659-5902. **Circle No. 404**

PC flash disk emulates hard disk. The PC Flash Disk, a half-size flash-memory card for the ISA or EISA bus, is essentially a hard disk without moving parts. The disk replaces the disk and controller and does not require cabling. An onboard expansion BIOS eliminates the need for special software. The board also allows for cold boots and provides full magnetic hard-disk emulation. It's available in capacities from 1 to 32 Mbytes. 1-Mbyte version, $180 (100). **M-Systems**, Fremont, CA. (510) 505-9081. **Circle No. 405**

SCSI adapter boosts I/O rate. By simultaneously processing up to 255 read or write requests, the ABP842 SCSI host adapter doubles the speed at which disk drives and other peripherals deliver data. Its high-speed memory stores all I/O requests from the operating system as opposed to most adapters, which, after receiving four requests, store additional requests in a "mailbox" and force the OS to wait. The VL-bus-based board comes with SCSI ribbon cable, installation software, and Corel SCSI Version 2 drivers and utilities. $379. **AdvanSys**, San Jose, CA. (408) 383-9400. **Circle No. 406**

RAID controller works with PC operating systems. The LDP Cache IV RAID 1 controller provides RAID Level 1 (mirroring) capabilities for PC-bus systems. It controls SCSI drives but appears as an IDE controller to the system, allowing use of standard OS drivers. The controller supports as much as 16 Mbytes of cache memory. It provides data-transfer rates of 5 Mbytes/sec, with bursts to 10 Mbytes/sec. $795 without cache memory. **Lomas Data Products Inc**, Marlboro, MA. (508) 460-0333. **Circle No. 407**

DSP board works on PCI bus. The Eagle-56, a DSP board based on Motorola's DSP56002, operates on the PCI local bus. A 40-MHz version offers 20 MIPS performance, and a 66-MHz version boosts performance to 33 MIPS. Each board has a high-speed parallel host interface and four banks of 64k×24-bit zero-wait-state SRAM. 40-MHz version, $2695; 66-MHz version, $3695. **Momentum Data Systems Inc**, Costa Mesa, CA. (714) 557-6884. **Circle No. 408**

PCI and VL graphics cards provide true color. The VideoBlitz II graphics accelerators, available for the PCI and the VL bus, display true (24-bit) color.

The PCI version, based on the Weitek P9100 accelerator chip, produces a 1280×1024 true-color display; the VL version makes an 800×600 24-bit display. Both versions have 2 Mbytes of VRAM; the PCI version is expandable to 4 Mbytes. PCI version, $589; VL version, $549. **Genoa Systems Corp,** San Jose, CA. (408) 432-9090, ext 262. **Circle No. 409**

PCI and VL graphics cards allow video playback. The Viper Pro graphics accelerators, available for the PCI and VL buses, allow 30-frames/sec video playback with the optional Video Power chip from Weitek. The graphics processor is Weitek's P9100, which provides 1280×1024 true-color (24-bit) displays. The boards are available with 4 Mbytes of VRAM or with 2 Mbytes, upgradable to 4 Mbytes. 2-Mbyte version, $479; 4-Mbyte version, $699. **Diamond Computer Systems Inc,** Sunnyvale, CA. (408) 736-2000. **Circle No. 410**

Computer cards embed PC architecture. Two new 16-bit single-board computers enable use of the PC architecture in embedded systems. The SAT-486SLC-33, based on a 33-MHz 486SLC processor, and the SAT-386SX-25, based on a 25-MHz 80386SX, are 4.5×7.1-in. boards that operate at temperatures from –40 to +85°C. The 486 version is also available with clock-doubled parts for clock speeds to 66 MHz. A 16-bit PC/104 connector allows expansion with additional functions. SAT-486SLC-25-1M (with 1 Mbyte of onboard parity-checked DRAM), $995; SAT-386SX-25-1M, $895. **WinSystems,** Arlington, TX. (817) 274-7553. **Circle No. 411**

Pentium and PCI work on passive backplane. The SB586 single-board CPU is based on the Pentium processor and contains a PCI local bus extension. It's available with a choice of two PCI-bus passive backplanes from the manufacturer. The board includes IDE and SCSI-2 controllers. CPU, $3525; backplanes, $379 to $529. **Industrial Computer Source,** San Diego, CA. (800) 523-2320. **Circle No. 412**

PCMCIA card adds enhanced parallel port. The SPP-100, a Type II PCMCIA card, is configurable either as a standard parallel port or as an enhanced parallel port (EPP), as defined by the IEEE 1284 specification. A DOS client driver, compatible with PCMCIA Card Services Specification 2.1, configures the card. A separate enabler program allows use without Card Services and Socket Services installed. A cable provides a D-25 connection. $195. **Quatech Inc,** Akron, OH. (216) 434-3154. **Circle No. 413**

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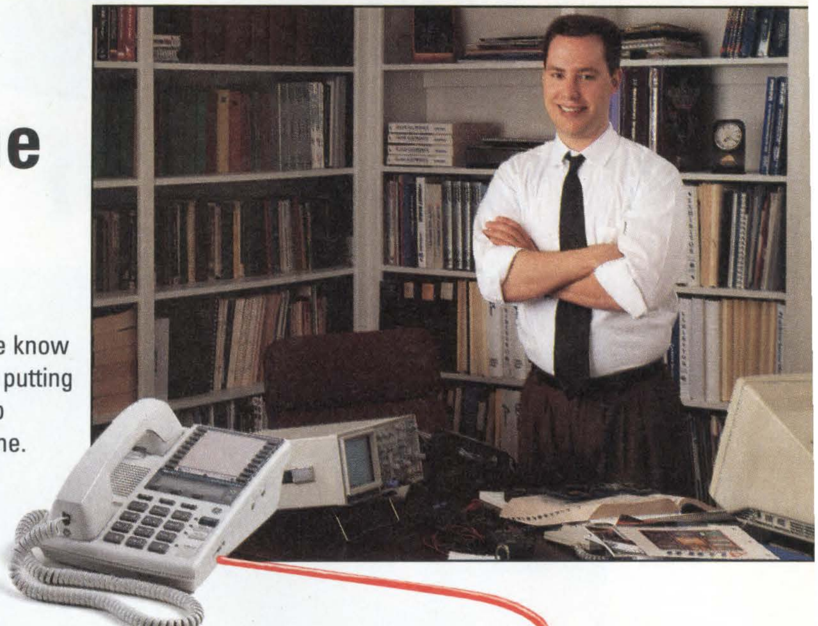

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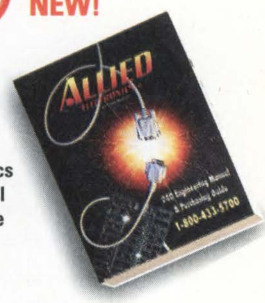

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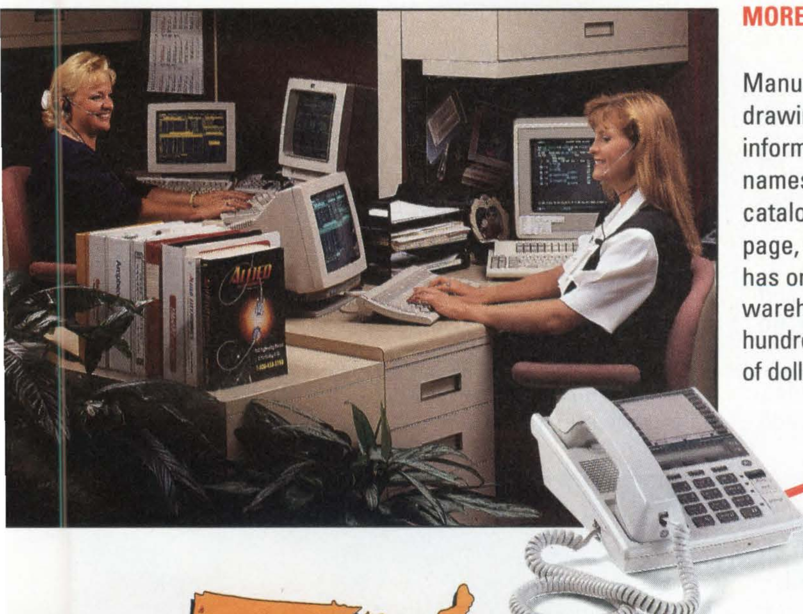

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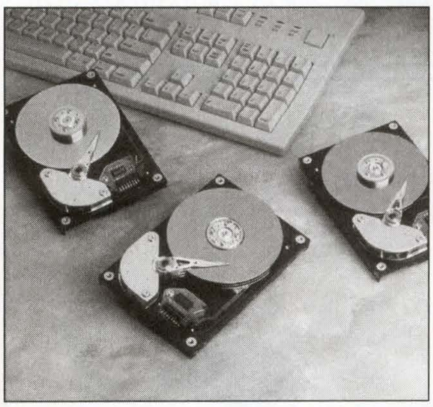
DRAM cards hold 2 to 32 Mbytes. The new Type I, 88-pin DRAM cards, each about the size of three credit cards stacked, are JEDEC/JEIDA compliant and hold 2, 4, or 8 Mbytes of data. Versions to be available later this year will hold 16 and 32 Mbytes. The cards are available with 16- and 18-bit memory, with and without parity, respectively. Memory-access time is 60 nsec. Prices range from $107 (2 Mbytes, no parity) to $370 (8 Mbytes with parity). **Motorola Inc,** Austin, TX. (512) 933-6700.
Circle No. 414

Computer board combines Pentium and PCI bus. The LBC4500 connects a Pentium processor with the PCI local bus in a single-board computer for a passive backplane. The card is designed for use with the manufacturer's LBP14 passive backplane, which provides four PCI slots and eight ISA slots. From $3295. **Diversified Technology,** Jackson, MS. (800) 443-2667.
Circle No. 415



Disk drives increase capacity and performance. Models 425, 850, and 1275 in the Filepro Advantage disk-drive family offer formatted capacities of 425, 850, and 1275 Mbytes, respectively. All models are available with either an Enhanced IDE or SCSI-2 interface. The drives support PIO Mode 4, the IDE specification for transferring data at 16.7 Mbytes/sec, and also DMA Modes 1 and 2, for transfer rates of 13.1 and 16.7 Mbytes/sec, respectively. Model 425, $255; Model 850, $399; Model 1275, $599. **Conner Peripherals Inc,** San Jose, CA. (408) 456-4500.
Circle No. 416

Computer board has 100-MHz 486. The Little Board/486 DX4 puts a 100-MHz 486 and other functions of a PC/AT motherboard into the profile of a 5.25-in. disk drive. With three or four expansion cards, the total space consumed equals a half-height drive. The board accepts PC/104 modules for onboard expansion. $1950 (100). **Ampro Computers Inc,** Sunnyvale, CA. (408) 522-2100.
Circle No. 417

PCI and VL cards combine graphics and video. The Imascan boards, available for the PCI and VL buses, combine with an attachable Chroma module to graphics acceleration, video frame grabbing, and video-in-a-window display. The boards use the Tseng ET4000/W32P graphics processor for 800× 600 displays of 24-bit color; a single frame buffer holds both graphics and video display data. Video input via the Chroma module can be RS-170, NTSC, PAL, or SECAM in 16- or 24-bit color or monochrome. Imascan with Chroma module, $1195. **Imagraph Corp,** Chelmsford, MA. (508) 256-4624.
Circle No. 418

ELECTRONIC DESIGN AUTOMATION

Software lets you simulate and test ATM network designs. ATM Modeler is a software protocol analyzer for testing circuit designs developed for asynchronous transfer mode (ATM) networks. Used with the company's Optium simulation environment, the tool provides a customizable test environment capable of simulating ATM networks with up to 4000 end systems and a variety of network traffic. $35,000. **Vantage Analysis Systems Inc,** Fremont, CA. (510) 659-0901.

Circle No. 500

Graphical system design tool provides tighter integration with simulators. Version 1.2 of DesignVision now has the ability to interact directly with VHDL and Verilog simulators from third parties. Not only can you describe behavioral models graphically, you can also set simulation breakpoints in the graphical diagram, display the current simulation state in the diagram, and step through simulation while displaying the simulation changes graphically. A debugging panel lets you step forward or backward through simulation time. The workstation-based software costs $10,000, but, until October 31, 1994, your company can purchase its first copy for $3000. **Vista Technologies Inc,** Schaumburg, IL. (780) 706-9300.

Circle No. 501

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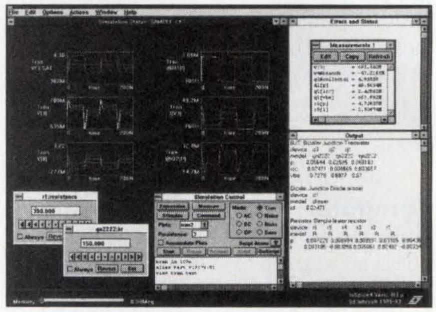
Spice simulator provides graphical results while the simulation is running. The ICAP/4 Virtual Circuit Design Lab lets you avoid the traditional batch-mode simulation of Spice simulators and see graphical waveforms as the simulation progresses. While the simulator is running, you can alter circuit values and observe the effects instantly. An interactive stimulus mode lets you sweep component or model parameters and compare the changing circuit performance. A cross-probing tool lets you see node voltages and device currents directly on the schematic. The software lets you use simulation breakpoints to stop simulation when a voltage, current, or computed device parameter satisfies a condition you set. Although the simulator directly accepts Spice netlists from all major schematic design tools, the included



SpiceNet schematic design tool can drive the entire simulation process, including graphical circuit editing, Spice netlist generation, simulation control, circuit measurement, and waveform display. ICAP/4 costs $2595 and runs under Windows, Windows NT, and on Macintosh systems. **Intusoft,** San Pedro, CA. (310) 833-0710.

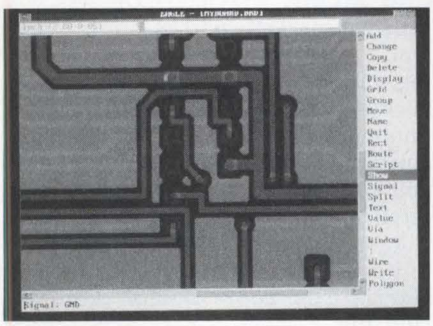
Circle No. 502

CIRCLE NO. 85

CIRCLE NO. 105

Timing-driven layout tool for ASICs improves performance and reduces die area. The ChipBench product from IBM provides a complete top-down, timing-driven, physical-design tool for ASICs. The company claims the tool reduces design-cycle time, improves performance through shorter wiring delays, and reduces chip area. The workstation-based tool starts at $246,000. **Altium Inc**, San Jose, CA. (408) 534-4140. **Circle No. 503**

Software tool lets you design and simulate communication systems using graphical blocks. The Advanced Communication Link Analysis and Design Environment (Acolade) lets you model communication systems by stringing together models for each system block such as channel, transmitter, receiver, encoder, and decoder. The tool includes a wide variety of models that may be interconnected to describe virtually any conceivable system topology. Acolade for PCs costs $8000; for Sun Sparc systems, the cost is $12,000. **Amber Technologies Inc**, Concord, MA. (508) 369-0515. **Circle No. 504**



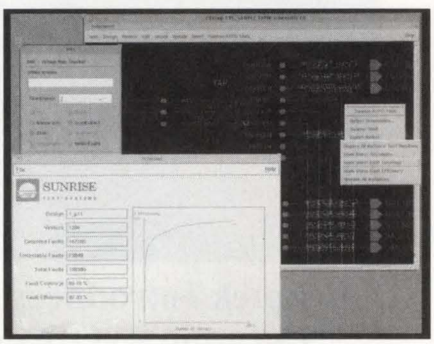
Schematic capture and pc-board layout software takes advantage of 32-bit system. Running on 386 or higher PCs under DOS, Eagle 3.0 runs in the 32-bit protected mode and is able to use the entire system RAM. The software includes schematic entry, a layout editor, and an autorouter. $1897. **CadSoft Computer Inc**, Delray Beach, FL. (407) 274-8355. **Circle No. 505**

Partition large designs into multiple FPGAs for rapid prototyping. The Concept Silicon partitioning software is aimed at the developers of real-time and DSP ASICs and systems. The software provides a complete set of graphical tools for mapping a design onto either the company's Paradigm RP configurable hardware architecture or custom prototype hardware. The Paradigm RP turnkey prototyping system handles designs with up to 250,000 gates and starts at $60,000. Concept Silicon costs $28,000. **Zycad Corp**, Fremont, CA. (510) 623-4400. **Circle No. 506**

Spice modeling tool for geometries below 0.5 μm. The Device Model Builder is a modeling and characterization tool to help you develop models and parameters for submicron designs. The software will be available in the third quarter and starts at $50,000. **Meta-Software Inc**, Campbell, CA. (408) 369-5400. **Circle No. 507**

Automatic place and route tool speeds physical layout of ICs. The PathFinder multilayer router features a window-routing architecture and a topology manager that lets you place and route complex ICs up to four times faster than previous tools from the company with density improvements of 20 to 30%. The tool uses global routing information to generate chip layout topologies early in the design cycle that will meet timing requirements and reduce layout iterations. PathFinder for gate and embedded arrays is available now, and versions for cell-based designs will be available in the fourth quarter. From $200,000. **Compass Design Automation,** San Jose, CA. (408) 433-4880. **Circle No. 508**

Signal-integrity tool includes new IBIS modeling specifications. The I/O Buffer Information Specification (IBIS) 1.1 includes capabilities for simulating open-drain and open-collector driver ICs. Because the models are tailored specifically for signal-integrity simulation, they offer Spice-level accuracy while simulating faster. LineSim Pro V3.2 includes the new IBIS features and costs $1295. **HyperLynx Inc,** Redmond, WA. (206) 869-2320. **Circle No. 509**



Automatic test-pattern-generation software offers test logic synthesis. The 2.0 version of TestGen offers improvements in full scan performance, IEEE 1149.1 JTAG support, and test logic synthesis. The tool can automatically select and implement the most effective test methodology for each portion of a complex circuit design in a single pass. The tool may insert full scan, partial scan, or use nonscan design for test techniques where scan cannot be inserted. TestGen 2.0 starts at $75,000; the test-synthesis option costs $25,000. **Sunrise Test Systems Inc,** Santa Clara, CA. (408) 980-7600. **Circle No. 510**

Create reprogrammable prototype for ASICs. The Logic Animator lets you create reprogrammable prototypes of ASICs containing as many as 50,000 gates. The software for creating the prototypes costs $60,000 and the FPGA-based reprogrammable hardware costs $30,000 per unit. Volume production is scheduled for the third quarter. **Quickturn Design Systems,** Mountain View, CA. (415) 967-3300. **Circle No. 511**

Device modeling and characterization tool adds submicron MOSFET model capability. The BSIM3 model was developed specifically for modeling submicron MOSFETs. The model accurately represents short-channel effects and can predict scaling effects on output characteristics in advance of your process capability. BSIM3 is part of the Success device modeling and characterization tool that interfaces to the company's analog simulator and to analog simulators from other companies. The complete Success system costs $25,000. **Anacad EES,** Milpitas, CA. (408) 954-0600. **Circle No. 512**

Design tool lets you explore a variety of tradeoffs in pc-board and MCMs. EDAnavigator lets you work concurrently with electrical, thermal, routability, partitioning, packaging, and component-placement issues to arrive at an optimum design with a minimum of iterations. The tool is available with a variety of modules that let you configure a system to suit your requirements. EDAnavigator runs on workstations and is priced from $10,500 to $45,000, depending on configuration. **Harris Electronic Design Automation Inc,** Fishers, NY. (716) 924-9303. **Circle No. 513**

SHORTS

VCS 2.1 now provides back annotation of delays and other functions, enabling the Verilog simulator to be used as a sign-off simulator. The simulator costs $40,000. **Chronologic Simulation,** (415) 965-3312. **Circle No. 514**

The Aida II automatic test-pattern-generation software now includes a partial scan test capability. $49,000. **Crosscheck Technology Inc,** (408) 432-9200. **Circle No. 515**

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CIRCLE NO. 153

5½-digit DVM attaches to PC's parallel port. Unlike classical handheld meters, the 1.41×3.75×6.3-in. Intelligent DVM includes no display; it uses your PC to present its readings. The $299.95 autoranging unit (1-range version: $239.95) offers an error of ±0.01% of full-scale-range (FSR) and a ±0.015% FSR/°C temperature coefficient. A $339.95 unit reduces errors by 40% and is 1/10 as sensitive to temperature. On the most sensitive range, the units resolve 100 nV; the least sensitive FSR is ±200V. A differential multiplexer scans eight inputs; there are two digital outputs. Conversion speed is 13 readings/sec. Windows-based software provides full control; it converts readings to engineering units and displays data as numbers or graphs. **Delta Quest,** San Jose, CA. (408) 997-8644.

Circle No. 420

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ISA bus DSO boards use sequential sampling to capture 300-MHz repetitive signals. The single-channel PCI-425 ($1695) and the 2-channel PCI-435 ($2695) have 50Ω inputs. Although they do not acquire single-shot transients, their bandwidth rivals that of many high-speed benchtop scopes. The BenchCom software that accompanies each unit lets you set up the boards and integrate them into your system. A $495 package called BenchTop lets you store and recall setups and waveforms. Delivery, 6 weeks ARO. **PC Instruments Inc,** Twinsburg, OH. (216) 963-0800.

Circle No. 421

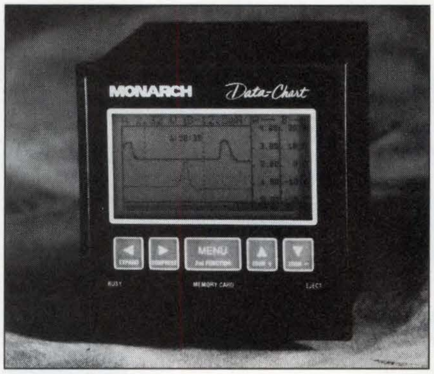
Software tool lets you program DSP applications in Visual Basic. WinSpox enables users of Visual Basic for Windows to control compute- or I/O-intensive operations with a minimum of programming effort. The package works with PCs equipped with fixed- or floating-point DSPs manufactured by TI and Analog Devices. WinSpox doesn't care whether the target resides on the PC motherboard or on an ISA bus add-in card; it does require that the target be running Spox V2.0, the vendor's DSP operating system. WinSpox includes a VBX (Visual Basic Extension) that permits interaction with the Windows Resource-Management Interface (RMI). $3000. **Spectron Microsystems,** Goleta, CA. (805) 968-5100.

Circle No. 422

ISA bus board captures analog signals at 60M samples/sec. The 30-MHz-bandwidth CompuScope 6012 resolves 12 bits. It can capture two channels simultaneously at 30M samples/sec, or one channel at 60M samples/sec. The board, which includes 512k samples of capture memory, can address 8M samples. Signal-to-noise

ratio is 62 dB at the maximum sampling rate. Real-time software calibration reduces the offset and gain temperature coefficients to 20 ppm/°C. Software drivers permit transferring data to a 486 PC's extended memory at 1.5M words/sec. $6995. (Upgrade from the vendor's CompuScope 1012: $2500.) **Gage Applied Sciences Inc**, Montreal PQ, Canada. (514) 337-6893.
Circle No. 423

Data-acquisition boards offer "hands-off" setup and calibration for under $1000. The $995 DT31-EZ and the $895 DT34-EZ, which lacks D/A outputs, take up to 330k 12-bit samples/sec. Except for address settings, the units are completely free of analog trims and digital jumper or switch settings. Data-transfer modes include 1- and 2-channel DMA, programmed I/O, and fast transfers (330k samples/sec on 486-based PCs) using the REPINSW (repeat instring word) instruction. A 512-point channel-gain memory lets you select different gains for each channel. You can connect 16 single-ended or eight differential signals, and you can select gains of 1, 2, 4, or 8 under software control. The inputs, which tolerate ±35V continuously with power on (±20V with power off), withstand electrostatic discharges of 1.5 kV. Each board includes eight TTL I/O lines and complies with FCC Class-A electromagnetic-interference standards. **Data Translation Inc**, Marlboro, MA. (508) 481-3700. **Circle No. 424**



Paperless recorder captures data for over 9½ years. The ¼-DIN-size, panel-mounted, line- or dc-powered Data-Chart has one or two channels. The unit can record as fast as 100 samples/sec or as slowly as 1 sample/10 min. It stores from 64k to 512k 8-bit samples in a nonvolatile PCMCIA card; an internal 16k-sample memory holds new data while you change cards. A back-lit 2.9×1.5-in. 160×80-pixel LCD presents the latest data or lets you look at previously acquired signals. You can equip the unit with several types of signal conditioning, including linearization and cold-junction compensation for three types of thermocouples. From $670. **Monarch Instrument**, Amherst, NH. (603) 883-3390. **Circle No. 425**

VMEbus plug-in triggers on anomalies and does 96-channel, 200-MHz timing analysis. The Timbat-PB plugs onto the vendor's VBT-325, a VMEbus analyzer that occupies a single VMEbus slot. The resulting product performs state and timing analysis, automatically detects timing violations, and creates a cycle-by-cycle screen display of bus addresses and data. The 200-MHz timing analyzer can trigger on any combination of 1, 0, and don't-care signals qualified by pattern duration. $5995. **VMEtro Inc**, Houston, TX. (713) 584-0728. **Circle No. 426**

TEST & MEASUREMENT

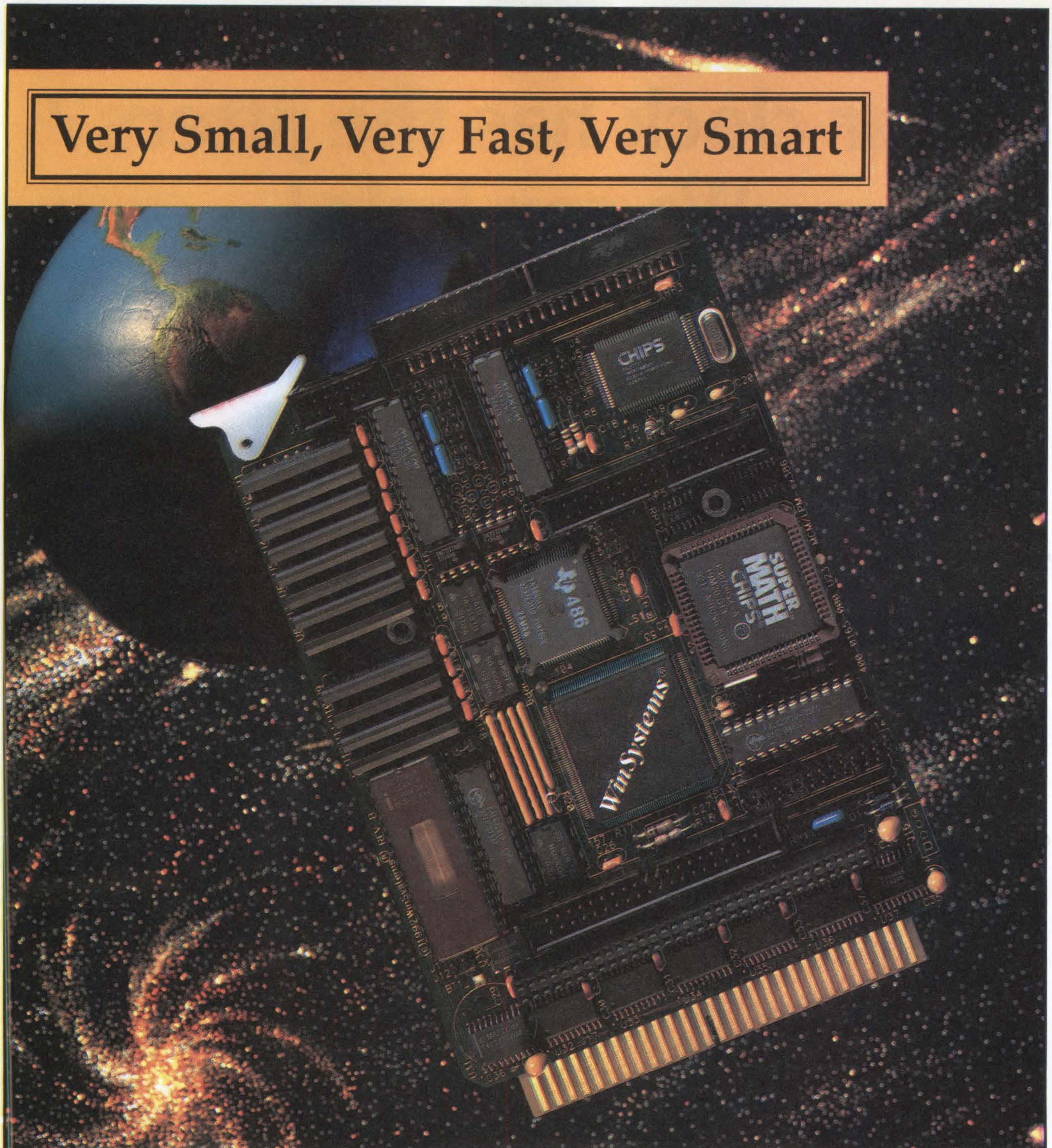
1M-sample/sec ISA bus ADC boards offer simultaneous sampling and a differential programmable-gain amplifier per channel. The Win-30PGSH (gains of 1, 2, 4, and 8) and the Win-30PGSL (gains of 1, 10, 100, and 1000) accept eight differential signals. Each channel has its own sample-hold circuit and differential-input programmable-gain amplifier. This configuration eliminates delays associated with settling of an amplifier shared by multiple channels. The 12-bit ADC converts a single input 750,000 times/sec, but its speed rises as it scans more channels. When it scans four or more channels, it makes a total of 1M conversions/sec. $2250. **United Electronic Industries,** Watertown, MA. (617) 924-1155. **Circle No. 427**

16-bit ISA bus data-acquisition board costs $995. The LDAS-16-AC takes 50,000 samples/sec and provides 16 TTL I/O lines. The board itself accepts 16 single-ended or eight differential inputs. An expansion multiplexer allows up to 256 analog inputs. C-language libraries cost $295. **Analogic Corp,** Peabody, MA. (508) 977-3000. **Circle No. 428**

Handheld device programmer also functions as ROM emulator. The $795, battery-powered Orbit 32 programs EPROMs to 8 Mbits, EEPROMs, and flash devices as well as some CMOS PROMs and serial EEPROMs. It accepts DIPs with up to 32 pins in rows whose center-to-center spacing ranges from 0.3 to 0.6 in. The unit, which operates in 8-, 16-, and 32-bit modes and also functions as a ROM emulator, has a user interface that is based on a splash-proof membrane keypad and a 4-line×20-character alphanumeric display. In many cases, the unit allows you to edit a device's contents while emulation is in process. **Stag Microsystems Inc,** Santa Clara, CA. (408) 988-1118. **Circle No. 429**

Units convert 8- and 16-bit SCSI bus from single-ended to differential and back and extend bus up to 56m. These SCSI bus converters and extenders let you mix single-ended and differential units on the bus. Operation is automatic and does not require programming. Versions are available for SCSI-1 and -2, and for SCSI-2 Fast and SCSI-2 Wide. Packaging options include open boards for OEM use and fully encased units with power supplies. Some configurations even include cables. Prices range from $300 to $1550. **Ancot Corp,** Menlo Park, CA. (415) 322-5322. **Circle No. 430**

2-channel frequency synthesizer covers 100 kHz to 310 MHz with 0.1-Hz resolution. The PTS 310 contains two independent synthesizers. Phase noise is –115 dBc/Hz at a 1-kHz offset from the carrier, spurious out-



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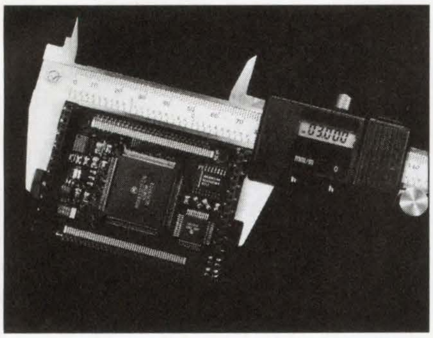
puts are below −70 dBc, frequency switching takes place in under 20 μsec, and output power is +13 dBm. Each channel has its own 50-pin parallel interface. A unit with an oven-controlled oscillator stable to ±10 parts/billion from 0 to 50 °C and 1 ppm/year costs $8225. **Programmed Test Sources Inc**, Littleton, MA. (508) 486-3008. **Circle No. 431**



1-oz, $495 data logger teams 68332 and PIC16C64 μPs. The 2×3×0.5-in. Tattletale Model 8 accepts eight analog inputs, which it digitizes to 12 bits at up to 100k samples/sec. It includes 256 kbytes to 1 Mbyte of RAM, 128 kbytes to 1 Mbyte of flash EEPROM, two RS-232C ports, a real-time clock, and 25 digital I/O lines. For data-intensive applications, you can add a PCMCIA adapter. Support includes C and Basic libraries, technical notes, documentation, tools, and sample programs. Two mezzanine prototyping boards let you connect signal conditioning, communications, I/O, and memory circuits. **Onset Computer Corp**, Pocasset, MA. (508) 563-9000. **Circle No. 432**

ISA bus boards expand digitizer's memory to 1 Gbyte, accept 200 Mbytes/sec. The MEM500 board stores 32, 64, 128, or 256 Mbytes. It makes 32- and 64-bit data transfers via an auxiliary bus at speeds to 200 Mbytes/sec. The board was designed for use with the vendor's DA500 500M-sample/sec 350-MHz digitizer—you can connect up to four MEM500s to a DA500—but it is also available separately. Power required is 5V at 2.4A max. $6950 to $34,900. **Signatec Inc**, Corona, CA. (909) 734-3001. **Circle No. 433**

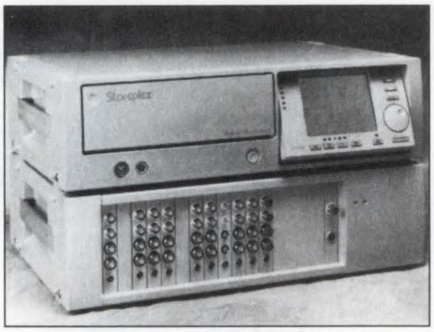
Add-in for 1-2-3 and Excel brings FFT capabilities to Windows spreadsheets. FFTtools V2.0 is a DLL that calculates mixed-radix FFTs. It preprocesses data sets to remove the mean, pad the data with zeros, truncate the data to speed calculations, or window the data with any of 17 taper functions. It also post-processes FFTs to center them at dc or make them single-sided, logarithmically compress their amplitude, scale them into physical units, compute power, or compute the phase of noisy data. $99. Users' guide, $25. Upgrade from FFTtools V1.0, $39 ($29 for registered users). **Integrated Scientific Resources**, Santa Monica, CA. (310) 453-6809. **Circle No. 434**

PCMCIA data-acquisition card captures eight channels at 25k samples/sec. The $299 PCM-DAS08 plugs into type II and III PCMCIA slots. Its 12-bit ADC converts at 25k, 12.5k, 6.25k, or 3.125k samples/sec. The standard input range is ±5V, but ranges of ±0.5V and ±0.05V are also available. The card has three CMOS digital outputs and two digital inputs. One of the inputs can act as a rising-edge trigger for the ADC. A $49 software package includes card and socket services, a uni-

versal data-acquisition library, and calibration routines. **Computer Boards Inc**, Mansfield, MA. (508) 261-1123.
Circle No. 435

Data-acquisition software graphs to 110k points/sec in real time. Snap-Master V3.0 can create real-time graphs of much of the data gathered by data-acquisition boards. Most competitive packages plot at speeds no faster than 15k points/sec, so they often must plot graphs from previously acquired data. Snap-Master achieves the 110k-point/sec speed using a 25/50-MHz 486DX2 PC with a graphics accelerator; plotting speed is 80k points/sec without the accelerator. New displays include dials, bar graphs, simulated LEDs, and digital meters. \$995 to \$2480. **HEM Data Corp**, Southfield, MI. (313) 559-5607. **Circle No. 436**

Units test PCMCIA sockets. PCCTest 350 series testers verify that PCMCIA sockets are working correctly. The µP-based units, which are PCMCIA cards themselves, verify all data, and address and control signals on sockets that comply with V2.x of the PCMCIA standard. An on-board ADC measures the supply voltages. The accompanying software works with socket controller ICs from Intel, Vadim, and Cirrus Logic. An optional RS-232C interface permits connection of a terminal for interactive debugging. \$495 to \$795. **Sycard Technology**, Sunnyvale, CA. (408) 247-0730. **Circle No. 437**



Portable cassette-tape instrumentation recorder acquires digital as well as analog data. The Storeplex Portable Instrumentation Recorder now accepts a digital record/replay module that acquires data from sensors that have digital outputs. You can now also replace the unit's 2-channel analog record/playback modules with 4-channel record-only modules, thus doubling the channel capacity. A single S-VHS cartridge can store 69 Gbytes. From \$35,000. **Racal Recorders Inc**, Irvine, CA. (714) 727-3444. **Circle No. 438**

2-channel, 8-pole active filter tunes from 0.03 Hz to 1 MHz. Both of the Model 3988's channels can operate as highpass or lowpass filters or voltage amplifiers with up to 70 dB of gain and a 7-MHz bandwidth. In the highpass mode, the maximum corner frequency is 300 kHz. Minimum high- and low-pass corner frequencies of 0.003 Hz are optional. You can pick Butterworth or Bessel characteristics with 48 dB/octave slope, and you can connect the two channels as one bandpass or band-reject filter. The inputs accept single-ended or differential signals at levels to ±10V. Prefilter gain adjusts in 10-dB steps; postfilter gain adjusts in 0.1-dB steps. \$2995. **Krohn-Hite Corp**, Avon, MA. (508) 580-1660. **Circle No. 439**

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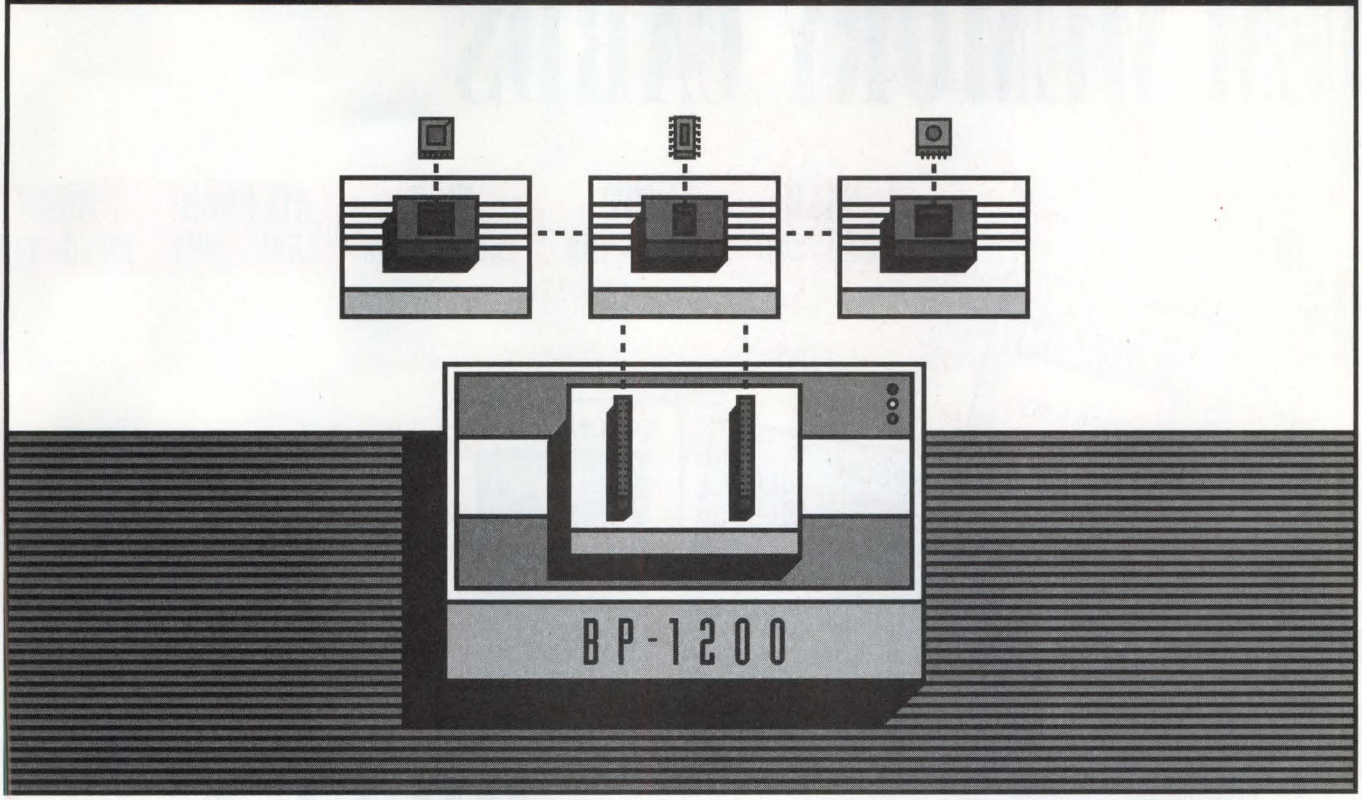
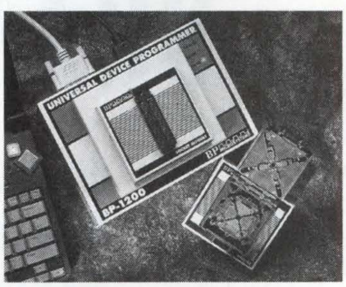


The BP-1200 universal device programmer leads the industry in devices supported, programming speed, ease of use and reliability. With prices starting at $2495, **free software updates**, and a three year limited warranty,* the BP-1200 is simply the best choice for those seeking the biggest bang for the buck!



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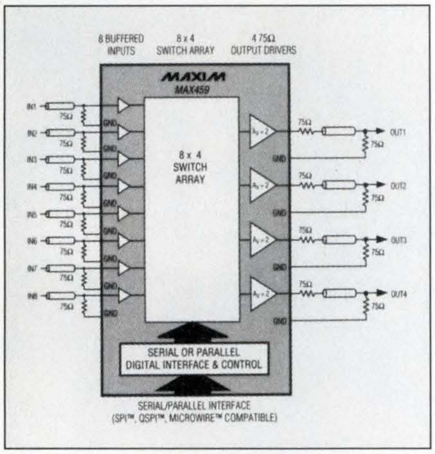
8-bit ADCs shut down power to 0.5 mW. The 20-MHz MP8786 and MP8776 typically dissipate 110 mW. Both converters include output-enable control logic to produce 3-state outputs that can directly interface with a bus or a μP. Pin-for-pin replacements of the company's MP8775 and MP8785, the 8776 ($5.28 (1000)) and 8786 ($5.42) come in 24- and 20-pin, packages, respectively. **Micro Power Systems**, Santa Clara, CA. (408) 727-5350. **Circle No. 440**



100-MHz crosspoint switches drive 75Ω cable. The MAX458/459 8×4 video crosspoint switches replace multiple switches, amplifiers, and logic. The 458 includes four digitally controlled, 100-MHz unity-gain-stable output buffers (gain of +1) and has a differential phase and gain error of 0.05° and 0.01%, respectively. The 459 includes four 90-MHz, 300V/μsec amplifiers with a fixed gain of +2 for directly driving 150Ω back-terminated cable without external feedback resistors. To parallel multiple switches, a digitally controlled disable mode turns off each output amplifier and puts each into a high impedance state. The devices come in 40-pin DIPs, and prices start at $24 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 441**

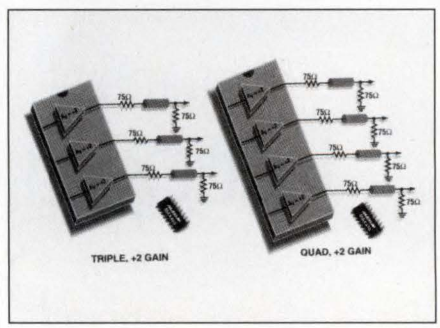
Genlock IC produces eight standard NTSC and PAL frequencies. The EL4584 generates a master clock that is phase-locked to an external horizontal sync reference. The IC includes eight preset frequencies; you can also use an external divider to generate nonstandard frequencies. When you use the IC with the company's EL4583 sync separator, the IC generates H-sync phase-locked clocks. The internal PLL includes a phase-frequency detector, which preempts locking to a harmonic, and a coast feature, which disables the loop without disturbing the VCO. An external varactor and LC-tuned circuit or crystal oscillator controls the VCO's frequency, which can go up to 35 MHz. In 16-pin DIPs and SOICs, the chip costs $4.71 (1000). **Élantec Inc**, Milpitas, CA. (408) 945-1323. **Circle No. 442**

Photosensor ADC has 20-bit resolution. The DDC101 current-input ADC directly connects to low-level sensors, such as photodiodes and other current-output devices. The IC uses a patented delta-modulation topology—slightly different from delta-sigma and integrating converters—that accurately digitizes the low-current levels. Using digital integration, oversampling, correlated double sampling, and digital filtering, the IC improves noise and linearity as input level decreases. With an input signal of 0.1% full-scale, the maximum linearity error is 0.0003% FSR. The conversion rate is 15 kHz. The ADC comes in 24-pin SOICs and 28-pin DIPs; prices start at $22.95 (1000). **Burr-Brown Corp**, Tucson, AZ. (800) 548-6132. **Circle No. 443**

Electronic circuit breaker integrates fast fault protection and control. The UCC3912 IC integrates a 0.15Ω power MOSFET and operates from 3 to 8V. Other features include digitally programmable current limit from 0 to 3A, a programmable on-time, and a programmable start delay. When disabled, the IC draws 1 μA. During extended faults, the IC automatically opens the circuit and resets it at a 3% duty cycle to limit power dissipation. Other than supply bypass, the IC requires only a single external capacitor for fault timing. $2.50 (1000). **Unitrode Integrated Circuits Corp**, Merrimack, NH. (603) 424-2410. **Circle No. 444**

Dual op amps top ±5V video specs. The HA5022 and HA5023 specify typical 0.07-dB gain flatness to 20 MHz, 0.03% and 0.03° respective differential gain and phase, and 0.8-mV input offset when running from a ±5V supply. These ICs are dual versions of the company's HA5020. The 5022 features a per-output enable/disable, which allows video multiplexing without a separate multiplexer. When configured for a gain of +1, the amplifiers provide a 125-MHz, 3-dB bandwidth, a 28-MHz full-power bandwidth, and a 350Vμsec slew rate. At gains of +2, the same specs are 95, MHz, 26 MHz, and 475V/μsec, respectively. A 16-pin DIP or SOIC HA5022 costs $3.30 (100). The 8-pin 5023 costs $3.20. **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7224. **Circle No. 445**

16-bit DAC integrates fast interface. The DAC712 comes with a precision ±10V temperature-compensated reference, a ±10V output amplifier, and a 16-bit port-bus interface. The digital interface has 60-nsec min write-pulse widths, is double buffered, and has a clear function that resets the analog output to bipolar zero. Double buffering permits simultaneous updating of several DACs. The output swings ±10V using ±12 to ±15V supplies. Maximum power dissipation is 600 mW. In 28-pin DIPs and wide SOICs, 13- and 14-bit linearity grades are available starting at $13 (100). **Burr-Brown Corp**, Tucson, AZ. (800) 548-6132. **Circle No. 446**



Triple and quad video buffers eliminate drive amplifiers. The MAX467 through 470 have closed-loop gains of +1 or +2 for driving 50 or 75Ω back-terminated coaxial cables with low differential gain and phase error of 0.01% and 0.03°, respectively. Specified for ±5V operation, the buffers guarantee an output drive of ±2.5V into a 150Ω load. The buffers also feature 100-MHz unity-gain bandwidths and 300Vμsec slew rates. Prices for the 16-pin DIPs and SOICs start at $3.70 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 447**

Video DACs feature true color and gamma correction. Each IC in the ADV15x series combines three 10-bit

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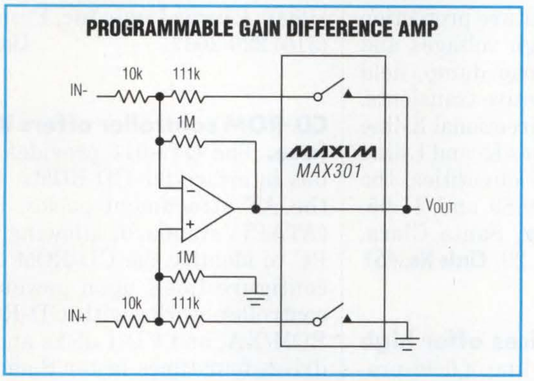

Maxim's new precision analog switches guarantee 3Ω on-resistance flatness and 2Ω channel matching. These ground-breaking specifications assure lower distortion, improved linearity and accuracy, and freedom from trimming for attenuators, tuned filters, and programmable-gain amplifiers. The circuit shown, for example, allows CMRR as low as 0.012% without trimming. All switches operate from single supplies of 10V to 30V, or dual supplies of ±4.5V to ±20V.

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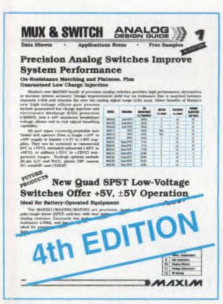
PART	FUNCTION	R_{ON} (Ω)	MATCH (Ω)	FLATNESS (Ω)	CHARGE INJECTION (PC)	V_{LOGIC}	*COST ($)
MAX301	dual SPST	30	2	3	15	✔	1.23
MAX303	dual SPST	30	2	3	15	✔	2.57
MAX305	dual SPST	30	2	3	15	✔	2.57
MAX317	SPST	30	N/A	3	10	✔	1.05
MAX318	SPST	30	N/A	3	10	✔	1.05
MAX319	SPST	30	2	3	10	✔	1.41
MAX333A	quad SPST	30	2	3	10	N/A	3.60
MAX351	quad SPST	30	2	3	10	✔	1.76
MAX352	quad SPST	30	2	3	10	✔	1.76
MAX353	quad SPST	30	2	3	10	✔	1.76
MAX361	quad SPST	85	2	9	10	✔	1.29
MAX362	quad SPST	85	2	9	10	✔	1.29
MAX364	quad SPST	85	2	9	10	N/A	1.14
MAX365	quad SPST	85	2	9	10	N/A	1.14



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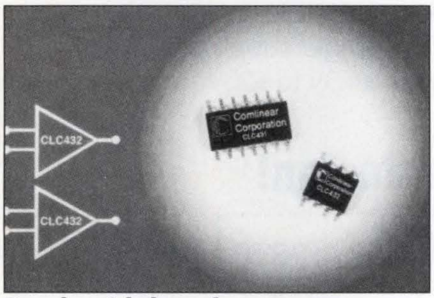
CIRCLE NO. 205

video DACs and associated color-palette RAM in one package. The DACs can deliver 24-bit true-color performance at rates up to 220 MHz. Four other family members operate at 170, 135, 110, and 85 MHz. The ADV7150 and 7152 feature three 8-bit control inputs that provide 256^3 addressable colors. Their companion, the pseudo-color 7151, displays images of equal resolution but with a choice of 256 colors/frame. The 7151's three 256×10-pixel color look-up table enables on-chip linearization, including gamma correction and monitor calibration. Prices range from $69 to $71 for the 85-MHz versions to $121 to $167 for the 220-MHz grades. **Analog Devices**, Wilmington, MA. (617) 937-1428. **Circle No. 448**



Dual wideband op amps save board space. The CLC431 and CLC432 current-feedback amplifiers feature typical dc-coupled small-signal bandwidths of 62 MHz at gains of +2 and typical slew rates of 2000V/μsec. The amplifiers operate from single 10 to 36V and dual ±5 to ±18V supplies. Typical supply current is 7.1 mA/channel (R_L=infinity). The dual amplifiers have closely matched dc and ac electrical characteristics, and channel isolation is 70 dB at 10 MHz. The 14-pin 431 ($2.99 (1000)) includes a disable feature that operates single-ended or differentially to accommodate a wide range of logic families. The 432 ($2.49 (1000)) comes in an 8-pin package. Both are available in DIPs and SOICs. **Comlinear Corp**, Fort Collins, CO. (303) 226-0500. **Circle No. 449**

Video preamps meet XGA-monitor requirements. The LM1207 and LM1208 video preamplifiers have bandwidths of 85 and 130 MHz, respectively. Both feature 0 to 4V-dc controls for interfacing with μCs, on-chip video blanking requiring only six external components, and dc restoration. The 1208 also features a 40-dB drive-control range. The outputs are stable, and output rise and fall times are symmetrical. The devices come in 28-pin DIPs, and prices begins at $2.20 (1000) and $2.50, respectively. **National Semiconductor**, Santa Clara, CA. (408) 721-5240. **Circle No. 450**

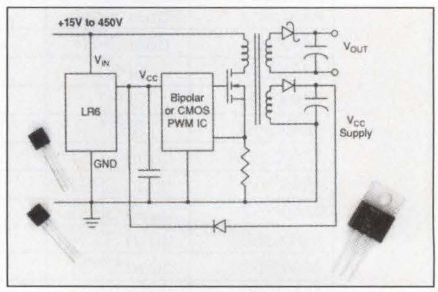
Small bus drivers meet auto standards. The Si9241EY and Si9243EY narrow-body SOICs meet the ISO9141 standard for communication between automotive computers and diagnostic equipment. The devices include short-circuit and overtemperature protection and can handle the high voltages and stresses imposed by load dump, field decay, and other automotive transients. The 9241 features a bidirectional K-line pinout. The 9243 provides K- and L-line pinouts. In large OEM quantities, the 9241 and 9243 cost $0.89 and $1.05, respectively. **Siliconix**, Santa Clara, CA. (800) 554-5565, ext 29. **Circle No. 451**

Interconnection devices offer high I/O densities. The IQ line of field-programmable interconnect devices (FPIDs) offers I/O densities from 96 to 320 ports. The devices operate as fast as 100 MHz and have pin-to-pin delays of 10 nsec. The heart of the devices' architecture is a nonblocking globally connected switch matrix, which allows flexible routing signals. You can program each I/O port as an input, an output, or a bidirectional port. The devices offer programmed switch-matrix connections and I/O port attributes that are configured with data stored in internal SRAM cells and registers. Prices range from $0.20 to $0.30/port (10,000). **I-Cube Inc**, Santa Clara, CA. (408) 986-1077. **Circle No. 452**

Serial memory interfaces with μP. The X84041 provides 4 kbits of EEPROM organized as 512 bytes. The 5V nonvolatile-memory device adapts serial-memory functions to a μP. The architecture incorporates write-, output-, and chip-enable signals, which exist on wide bus systems, eliminating the need for latches and I/O ports. The devices replace low-density byte-wide devices in applications with low package size and height. The device comes in 8-pin SOICs ($1.64) and DIPs ($1.45) (10,000). **Xicor Inc**, Milpitas, CA. (408) 432-8888. **Circle No. 453**

V.32bis chip sets have small form factor. The CL-MD1414UN and its PCMCIA version, CL-MD1414UNP, are data, fax, and voice modem chip sets that offer external controller code that supports international communication standards. By moving this code to external ROM, EPROM, RAM, or flash memory, you can design internationally compliant data, fax, and voice modems. A mixed-signal design makes it possible to integrate analog and digital functions on two CMOS chips. Standards supported include CCITT V.23, V.21, V.32, V.32bis, V.22, Bell 212A, and Bell 103 for data and CCITT V.17, V.29, V.27ter, and V.21 ch2 for fax. $50 (1000). **Cirrus Logic Inc**, Fremont, CA. (510) 226-2037. **Circle No. 454**

CD-ROM controller offers IDE interface. The OTI-011 provides an IDE-bus interface for CD-ROMs. It follows the AT attachment-packet interface (ATAPI) standard, allowing the host PC to identify the CD-ROM drive and configure itself upon power-up. The controller works with CD-ROM, CD-ROM/XA, and CD-I disks and handles drives four times faster than the standard CD-ROM speed. The device comes with ATAPI drivers and costs $8.95 (10,000). **Oak Technology Inc**, Sunnyvale, CA. (408) 737-0888. **Circle No. 455**



Start-up regulator runs off 15 to 450V-dc inputs. The LR645 3-terminal, high-input voltage regulator provides a fixed output of nominally 10V. Available in TO-92, TO-220, and surface-mount SOT-89 packages, the ICs can output 3 mA of continuous and 30 mA of peak current. Typical line regulation is 0.1 mV/V, and load regulation is 50 mV/mA. Supply current is typically 50 μA. A 100-nA typical off-state leakage current ensures low power dissipation when the IC is off. $0.21 (50,000). **Supertex Inc**, Sunnyvale, CA. (408) 744-0100. **Circle No. 456**

Digital video mixer handles 12-bit data. The HSP48212 accepts two 12-bit digital video signals and provides a weighted average proportioned according to a 12-bit mix ratio. The 13-bit output value is automatically rounded to

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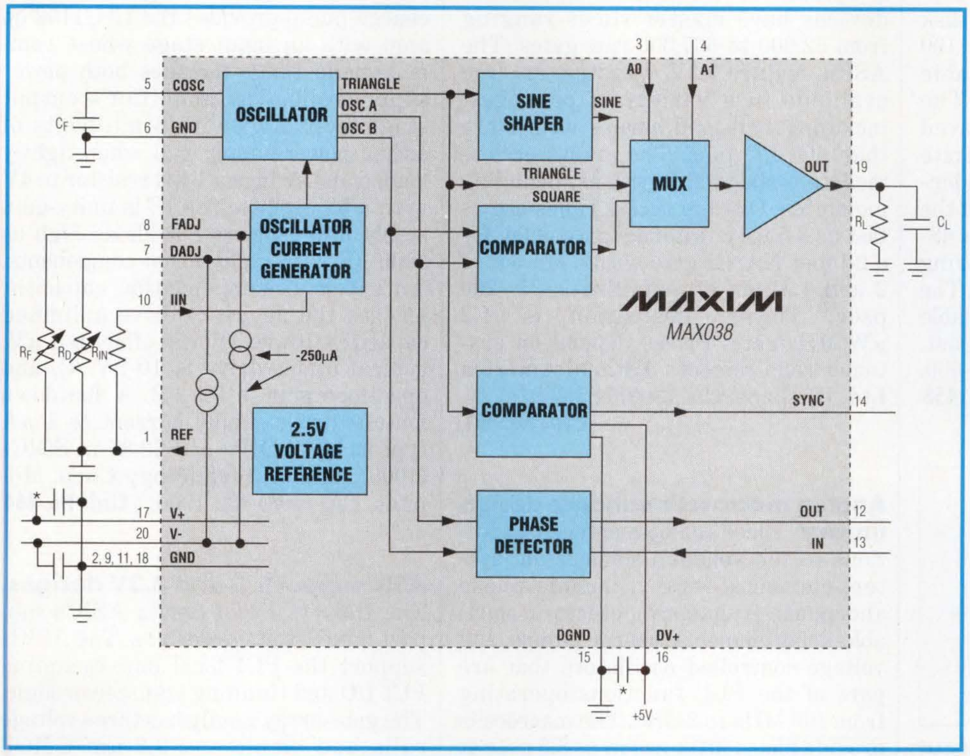

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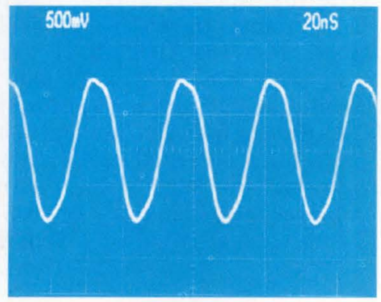

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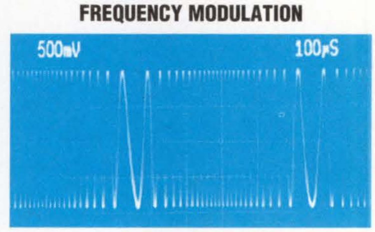

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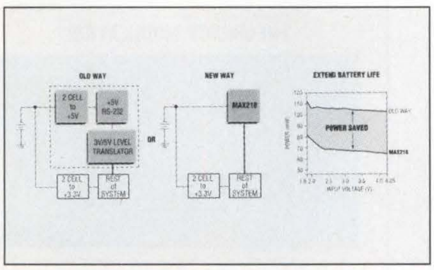
CIRCLE NO. 206

12, 10, or 8 bits to match system needs. The device accepts video at clock rates to 40 MHz and delays each input signal by as many as seven clock cycles to help synchronize video sources. It is available in 68-pin PLCC ($14.32 (1000)) or 64-pin PQFP ($18.46) packages. **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, x7200. **Circle No. 457**

Disk controllers include error correction. The AIC-8300 family of disk controllers handle data as fast as 100 Mbps and provide programmable error-correction coding (ECC). The ECC is a 297-bit, 3-way interleaved code that applies to data. A separate ECC protects the disk's data-field identifiers. Both the AIC-8370 IDE and the AIC-8320 SCSI devices include a 48-Mbyte/sec buffer interface for storing data flowing between host and disk. The parts cost $20 each; the 8370 is available now, and the 8329 is due in August. **Adaptec**, Milpitas, CA. (408) 945-8600. **Circle No. 458**



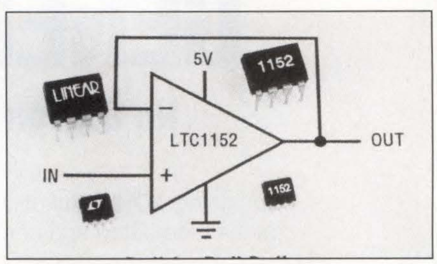
Two cells produce RS-232C output levels. The MAX218 dual transceiver operates from input voltages of 1.8 to 4.25V and maintains true RS-232C and EIA/TIA-562 voltage levels. The IC guarantees data rates up to 120 kbps. The two receivers remain active in 1-μA shutdown mode to monitor external devices that can wake up the IC when data needs to be transferred. The ICs come in 20-pin SSOPs, DIPs, and wide SOICs, and prices start at $2.10 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 459**

μC supervisor has programmable watchdog timer. The X25043 microcontroller (μC) supervisor combines 4 kbits of EEPROM with a complex reset controller and a watchdog timer with programmable intervals. The device has a high-speed serial peripheral interface and software protocol, which allows rapid access to data on a 3-wire bus. The reset controller generates a reset signal to the μC during power-up, power-down, and brown-out situations. The watchdog timer begins running once the reset signal is released. Two EEPROM bits of a configuration register, which selects one of four options, control the watchdog timer. 8-pin DIP, $1.50 (10,000). **Xicor Inc**, Milpitas, CA. (408) 432-8888. **Circle No. 460**

0.5-μm gate array has high gate count. The HG72G/E gate-array family operates faster than 100 MHz. The devices have master slices ranging from 52,000 to 667,000 raw gates. The ASICs feature 3.3V operation and are available in a variety of packages, including ball-grid arrays with more than 600 I/O pins. The arrays accommodate embedded functions, including memories. On-chip access times are as fast as 3.5 nsec. Internal gate delay for a 2-input NAND gate with a fan-out of 2 and 1.4 mm of metallization is 200 psec. Power dissipation is 1.2 μW/MHz/gate. Prices depend on customer requirements. **Hitachi America Ltd**, Brisbane, CA. (800) 285-1601. **Circle No. 461**

Analog macrocells enhance design library. These analog macrocells, additions to the vendor's semicustom system-elements library, include phase and phase-frequency detectors, variable-delay elements, charge pumps, and voltage-controlled oscillators that are part of the PLL functions operating from 100 MHz to 2 GHz. The macrocells provide phase jitter as low as 6.5 psec at 622 MHz. The library also includes DACs having 3-, 4-, 5-, 6-, and 8-bit resolutions at speeds as high as 500 MHz. An 8-bit video DAC with 4-nsec RAM macrocells offers 1- and 3-channel graphics. NRE charges, $40,000. **Synergy Semiconductor**, Santa Clara, CA. (408) 773-3643. **Circle No. 462**

0.7-μm ASICs feature low power. The TC170 series of ASICs are fabricated in a 0.7-μm process and come as gate arrays or standard cells. Typical gate delays are 270 psec; the devices operate from 5V. The arrays employ two layers of metallization and typically dissipate 4.4 μW/MHz/gate. Gate complexity ranges from 22,000 to 194,000 for the TC170G gate array and 5000 to 219,000 for the TC170C standard cell. The design libraries are compatible with the company's 3V T180/183 series. Volume pricing is $15 for a 45,000-gate product. **Toshiba America Electronic Components Inc**, Irvine, CA. (800) 879-4963. **Circle No. 463**



Zero-drift op amp swings rail to rail. An integrated high-frequency charge pump provides the LTC1152 op amp with an input stage whose common-mode range includes both power supply rails. The amplifier's output stage swings to within millivolts of either power-supply rail when lightly loaded and swings a 1-kΩ resistor to 4V with a 5V supply. The IC is unity-gain stable into capacitive loads as high as 2000 pF with no external components. An external compensation capacitor enables the device to drive unlimited capacitive loads. Typical offset is 1 μV, typical offset drive is 10 nV/°C, and open-loop gain is 130 dB. A shutdown feature drops supply current to 1 μA typ. $3.12 in DIPs and $3.37 in SOICs (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 464**

ASIC supports 5 and 3.3V designs. The Universal PCI Series ASICs support mixed-voltage designs. The ASICs support the PCI local bus, including PCI I/O and Gunning transceiver logic. The gate-array family has three voltage rails and employs a 0.6-μm CMOS process including as many as 223,000 gates. Other features include a 290-nsec propagation delay for a 2-input NAND gate, a 2.7-μW/MHz/gate power dissipation, a 2- or 3-layer metallization, and 160- to 304-pin plastic quad flat packaging. Special macros include PLL, clock-tree synthesis, and RAM and ROM. $6 to $60 (10,000). **NEC Electronics Inc**, Mountain View, CA. (800) 366-9782. **Circle No. 465**

ASIC family offers high-reliability plastic package. This ASIC family is available in plastic packaging that the vendor claims rivals ceramic packaging's reliability. The packaging suits avionics and military applications and enables ASICs to withstand 1000 temperature cycles over a –65° to +150°C temperature range. The temperature testing exceeds the reliability requirements of ceramic-packaged MIL-STD-883 products. $299; same device in ceramic, $399. **American Microsystems Inc**, Pocatello, ID. (208) 234-4690. **Circle No. 466**

POWER SOURCES

Lithium thionyl-chloride cells run for 15 years continuously outdoors. Eternacell lithium thionyl-chloride cells have an open-circuit voltage of 3.65V and capacities ranging from 0.9 to 30 Ahr. Cell sizes include 2/3A, 1/2AA, AA, C, D, and DD. The cells are hermetically sealed in stainless-steel cases and have a 15-year outdoor service life min. 2/3A, \$4.97; DD, \$17.95 (1000) **Power Conversion Inc**, Elmwood Park, NJ. (800) 452-1211.
Circle No. 364

PCMCIA power controller replaces forest of MOSFETs. The MIC2560 is a PCMCIA-slot power controller that manages the profusion of both main-supply and programming voltages. The controller's 16-pin surface-mount package fits between a PCMCIA controller and a PCMCIA socket, replacing 6 to 10 MOSFETs and associated glue logic. The device's outputs are short-circuit and overvoltage protected. \$2.96 (1000). **Micrel Semiconductor**, San Jose, CA. (408) 944-0800. **Circle No. 365**

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50W dc/dc converter suits telecomm applications. The HDB49-C-40 50W dc/dc converter has outputs of 5.6, 12, –12, and –5.2V. Outputs are adjustable by ±10%. The converter accepts input voltages ranging from 35 to 60V. Noise and ripple are 1% p-p. The unit is overvoltage, overload, and short-circuit protected. Operating temperature is 0 to 50°C with no derating. The unit complies with FCC or VDE EMI regulations and measures 6.60×3.94×1.95 in. \$99 (100). **Total Power International Inc**, Lowell, MA. (508) 453-7272. **Circle No. 366**

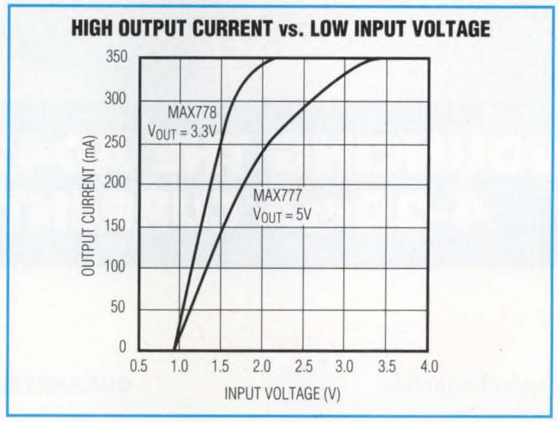
Supplies energize ultraminiature ultraviolet lamps. The 44 series and PS-5 series power supplies accept 5, 12, and 24V dc and measure 3×3.3×1.5 in. The supplies power Pen-Ray and CP series ultraviolet lamps. The lamps are low-pressure, cold-cathode, mercury gaseous-discharge lamps made of double-bore quartz whose lighted length ranges from 0.75 to 90 in. \$40 to \$240. **UVP Inc**, Upland, CA. (800) 452-6788, ext 210. **Circle No. 367**

High-density dc/dc converters output 5 or 3.3V. The PKU series of high-density dc/dc converters comprises a 5V, 150W model and a 3.3V, 100W model. The converters accept 36 to 72V dc and measure 2.19×4.79×0.66 in. Their calculated MBTF is 1.2 million

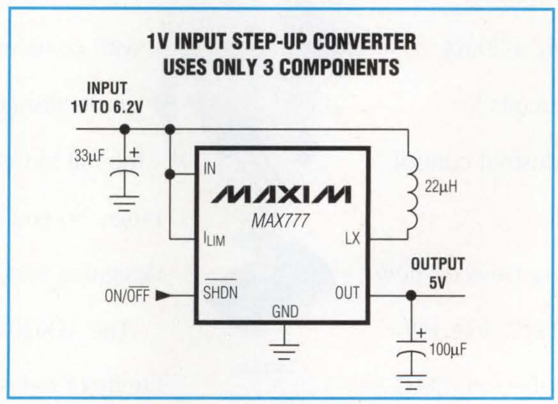
1-CELL (1.1V) INPUT STEP-UP GUARANTEES 5V, 30mA OUTPUT

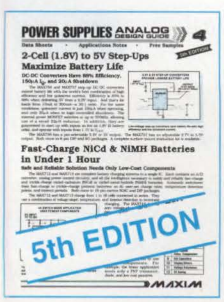
Internal Synchronous Rectifier Assures Complete 20µA Shutdown

The MAX777/MAX778/MAX779 step-up dc-dc converters deliver more power from a single battery cell (1.1V) than any other IC solution available. An internal active rectifier diode increases efficiency and provides true 20µA shutdown. Only 2 capacitors and a small 22µH inductor are needed, saving space and cost. Guaranteed start-up is 1V (10mA load). In shutdown, the internal switched rectifier opens the DC path from the input to the output, stopping current drain associated with conventional step-up converters. Also, the Active Rectifier™ allows these regulators to act as buck/boost converters, providing regulation for input voltages above and below the output voltage. Order the complete surface-mount evaluation kit (MAX778EVKIT-SO) to speed your design.



- **5V @ 30mA or 3.3V @ 60mA from 1.1V Inputs, Guaranteed**
- **Internal Synchronous Rectifier**
- **True 20µA Shutdown Supply Current**
- **3.3V or 5V Regulated Output from 1V to 6.2V Input**
- **8-Lead DIP or SOIC Package**
- **MAX777: 5V Output**
  MAX778: 3.3V/3V Output
  MAX779: Adjustable Output (2.7V to 6V)
- **Evaluation Kit Available**





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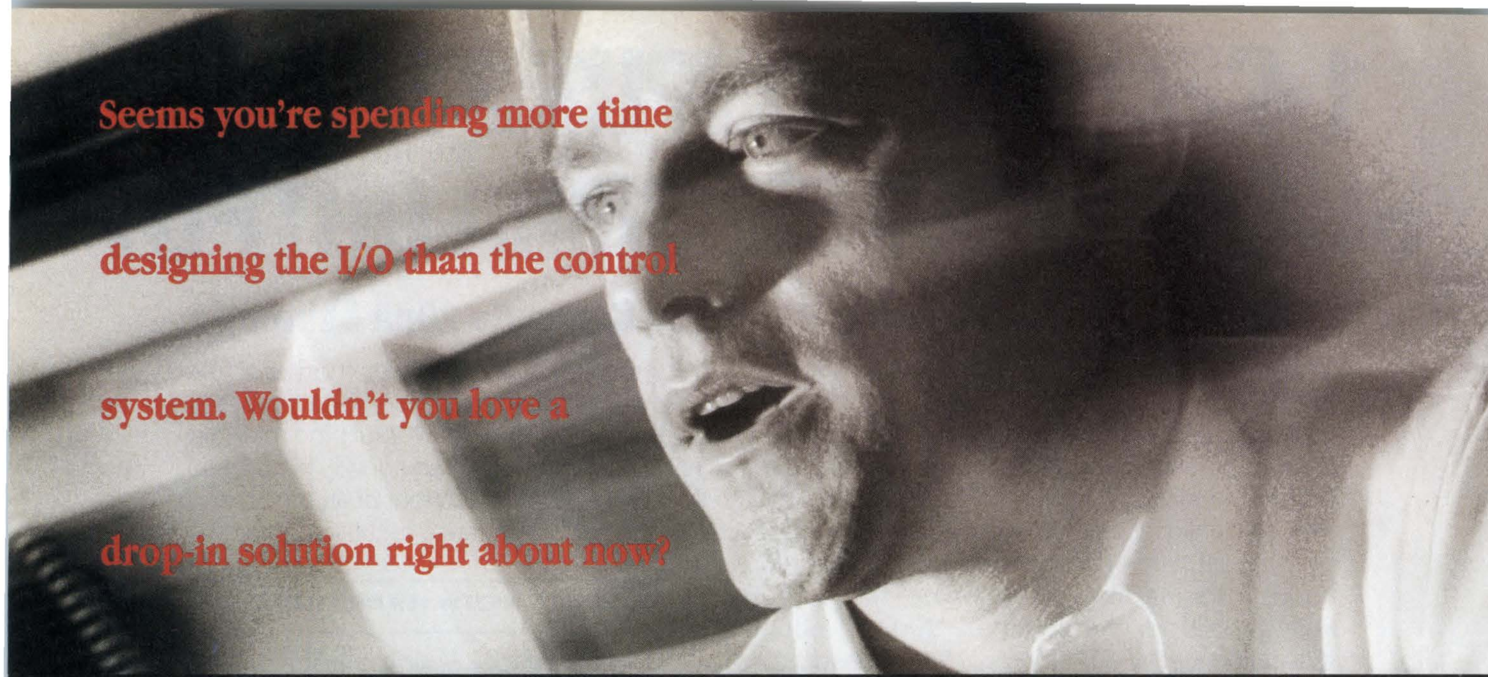


CIRCLE NO. 210

POWER SOURCES

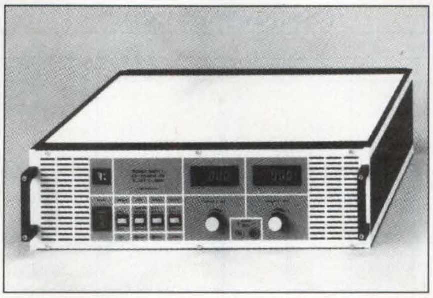
hours at 25°C ambient. Below 60°C, the converters require no heat sinks if airflow is 300 lfm. $145 (1000). **Ericsson Components Inc**, Richardson, TX. (214) 997-6561. **Circle No. 368**

Lithium primary batteries are thin enough to fit in PCMCIA cards. Powerdex lithium primary batteries furnish 3 or 6V outputs yet measure 0.7 mm thick. Units come in 6.6×9.4-, 4.6×7.4-, and 3×3.9-cm sizes. Capacities are 50 to 1400 mAhr. You can solder the batteries' coplanar side tabs directly to a pc board. **Gould Electronics Inc**, Eastlake, OH. (800) 722-7890. **Circle No. 369**

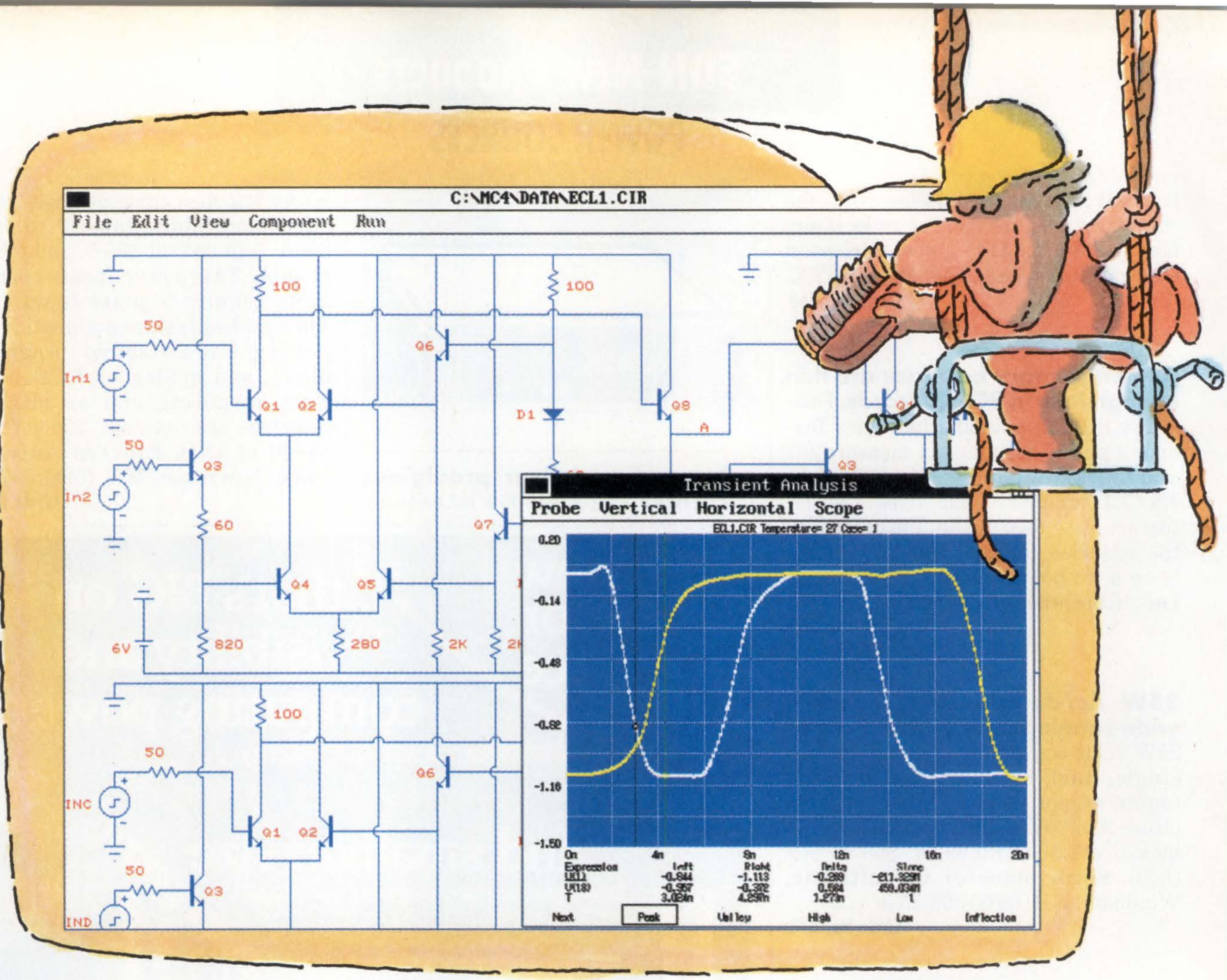
25W dc/dc converters accept wide-ranging inputs. The TA series 25W dc/dc converters is available with single, dual, or triple outputs. The inputs accept voltages ranging from either 9 to 36V or 20 to 72V. The units measure 2.50×3×0.83 in. $58 to $69 (500). **Semiconductor Circuits Inc**, Windham, NH. (603) 893-2330. **Circle No. 370**

Miniature 0.5 and 1W dc/dc converters target distributed applications. The PM600 series 0.5 and 1W dc/dc converters measure 1.25×0.8×0.4 in. and exhibit 50% efficiency. The converters operate from either 5 or 12V ±10%. The converters come with an internal input filter. $15 (OEM quantities). **Computer Products**, South Boston, MA. (617) 464-6656. **Circle No. 371**

Rechargeable-battery snap bollixes 9V primary batteries. A battery snap for 7.2 or 8.4V NiCd rechargeable batteries has a third contact that precludes users' connecting conventional 9V primary batteries. The third contact strikes a plate found only on rechargeable batteries. $0.40 (1000). **Memory Protection Devices Inc**, Farmingdale, NY. (516) 293-5891. **Circle No. 372**



Lab supplies deliver prodigious currents. The EA-9000 laboratory power supplies come in three voltage/current combinations: 0 to 18V at 300A, 0 to 36V at 180A, and 0 to 72V at 90A. The power-factor-corrected units require 3-phase input power. The supplies feature automatic remote sensing, 0.15% stability, programmability, and analog or LCD meters. Rack mounting and an IEEE-488 interface are optional. $3000 (2 kW); $8000 (6 kW). **Electro Automatic Corp**, Lawrence, MA. (508) 687-6411. **Circle No. 373**



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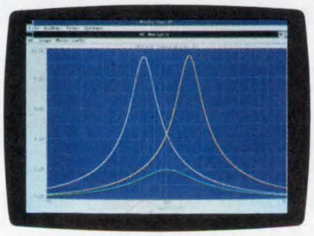

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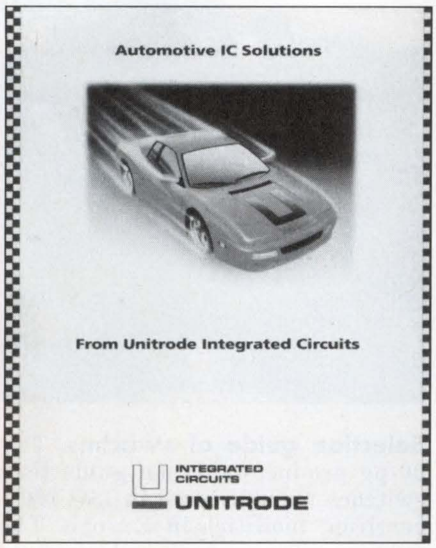
CIRCLE NO. 149

Catalog of Xilinx products. Digi-Key is the first catalog distributor to carry Xilinx products; this catalog covers the full range, including field-programmable gate arrays, erasable programmable-logic devices (EPLDs), serial configuration PROMs for FPGAs, and the Viewlogic base development system. **Digi-Key Corp**, Thief River Falls, MN. **Circle No. 516**



Brochure features ICs for automotive applications. This 12-pg brochure includes both text and diagrams pertaining to motor-control ICs, driver/special-function ICs, and power-management ICs. The brochure also highlights typical applications, including multiplex wiring, automatic suspension control, air-bag activation systems, and ignition control. **Unitrode Integrated Circuits Corp**, Merrimack, NH. **Circle No. 517**

Technical note covers DSO applications. *Digital Oscilloscope Applications in High Speed Electronics* explains how scope bandwidth and sample rate affect the measurement of both repetitive and single-shot signals. The publication also addresses problems making measurements in the presence of noise; cross-channel timing measurements; crosstalk; µP crashes; timing problems due to clock stew; metastability; probes; and using long memory to gain higher effective bandwidth. **LeCroy**, Chestnut Ridge, NY. **Circle No. 518**

Free configuration tool for data-acquisition systems. This free tool allows designers to reduce the complexity and time to configure a PC-based-data acquisition system for PC/XT/AT/EISA and Micro Channel-based computers, including laptops and notebooks. **National Instruments**, Austin, TX. **Circle No. 519**

Catalog details technical supplies. This illustrated buying guide provides information on electronic tools, test equipment, and technical supplies for assembling, testing, and repairing electronic products. The catalog also covers precision hand tools, test instruments, datacomm/telecomm equipment, tool kits, soldering/desoldering systems, lamps, magnifiers, and static-control products. **HMC**, Canton, MA. **Circle No. 520**

Guide to test-and-measurement instruments. This 96-pg guide contains information and specifications on a line of hand and stationary tachometers, frequency meters, running time meters, insulation testers, stroboscropes, controllers, and static eliminators. In addition, the catalog presents information on multimeters and test instruments. **Herman H Sticht Co**, Brooklyn, NY. **Circle No. 521**

Book teaches graphical programming language. *Cutting Your Test Development Time with HP VEE* provides a detailed tutorial on HP VEE, a graphical programming language. The book features numerous programming examples along with additional exercises for advanced users. $38. **Hewlett-Packard**, Palo Alto, CA. **Circle No. 522**

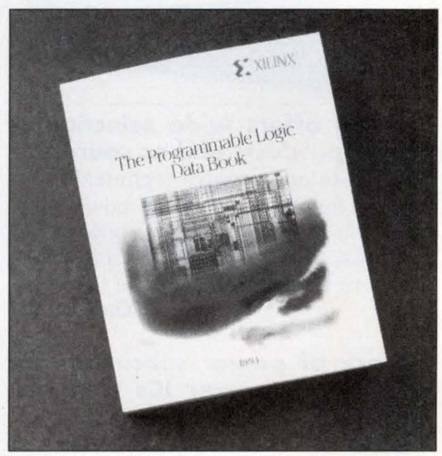
Catalog describes new electronic test-and-calibration instrumentation. This 98-pg catalog describes a line of signal sources, including waveform, function, and pulse generators; precision calibrators and multimeters; and RF signal/sweep generators. It also covers a line of high-performance VXI signal sources, options, and accessories. **Wavetek Corp**, San Diego, CA. **Circle No. 523**

Catalog describes line of pc-board pin headers and receptacles. A 50-pg catalog provides information on and product drawings for standard and custom interconnections for pc boards. **Specialty Electronics Inc**, Landrum, SC. **Circle No. 524**

Brochure highlights books and journals for instrumentation, measurement, and sensors. This catalog details a range of books, journals, and reference works for instrumentation, measurement, and sensors. Sample copies of journals mentioned in the brochure are available. **Institute of Physics Publishing Inc**, Philadelphia, PA. **Circle No. 525**

Guide for comm products, ASICs, and cache controllers. *The 1994 Vitesse Product Selection Guide* contains general information on all Vitesse standard products and ASICs. Products include 1-Gbps Fibre Channel-compatible data-communications devices, 2.5-GHz SONET-compatible ICs, and cache controllers for Pentium and P54C CPUs. **Vitesse Semiconductor Corp**, Camarillo, CA. **Circle No. 526**

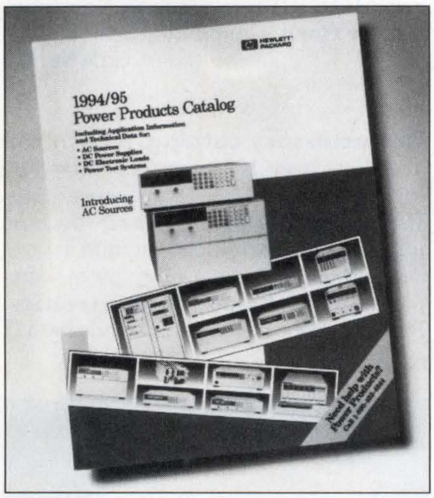
Test-accessory catalog. A 36-pg catalog lists over 100 products, including logic-analyzer test accessories, IEC1010-safe probes, and banana jacks. Other products include boxes, test strips, and laboratory power supplies. **ITT Pomona Electronics**, Pomona, CA. **Circle No. 527**



Data book for programmable-logic products. This 600-pg data book offers detailed information on field-programmable gate arrays, erasable programmable-logic devices, and serial PROMs. Electrical and timing parameters for all subfamilies are provided. The book offers 160 pgs on applications, ranging from general design hints to documented subsystem examples. Also included is *The Best of XCELL*, a collection of newsletters filled with hints for programmable-logic users. **Xilinx Inc**, San Jose, CA. **Circle No. 528**

Heat sinks for cooling μPs detailed. This 36-pg catalog covers a broad range of heat sinks, attachment methods, interface materials, and other thermal-management products. A heat sink/μP selector guide and an applications form are also included. **Aavid Engineering Inc**, Laconia, NH.
Circle No. 529

Data book on DSP products. This data book contains detailed technical information on a variety of DSP products, including video imaging products, enhanced speed grades of existing products, and data sheets of 41 DSP products. **Logic Devices Inc**, Sunnyvale, CA. **Circle No. 530**



Catalog offers wide selection of power products and ac sources. A 66-pg catalog provides technical information for ac sources, dc power supplies, dc electronic loads, power test systems, and solar-array simulators. **Hewlett-Packard,** Palo Alto, CA.
Circle No. 531

Library of power subcircuits for developing power ICs and systems. *Circuit Simulation of Switching Regulators Using HSpice* is a collection of papers and subcircuit models that allows you to convert power building blocks, such as switching regulators, pulse-width modulators, and inverters, to board or IC designs. The library comprises power subcircuits for simulating switching-regulator power systems in continuous- or discontinuous-conduction modes. All the library subcircuits come as HSpice files on a floppy disks or as standard Spice files. To download the files, call DOM Engineering Services at (512) 477-0756, *EDN* at (617) 558-4231, or the Intusoft BBS on Compuserve. The library and technical-reserach packet costs $50. **Meta-Software,** Campbell, CA.
Circle No. 532

RF/wireless handbook provides applications and design information. This 1100-pg handbook incorporates application information and design short cuts for engineers. The handbook highlights amplifiers, companders, IF systems, front-end systems, baseband processors, frequency synthesizers, and transmitters. **Philips Semiconductors,** Sunnyvale, CA.
Circle No. 533

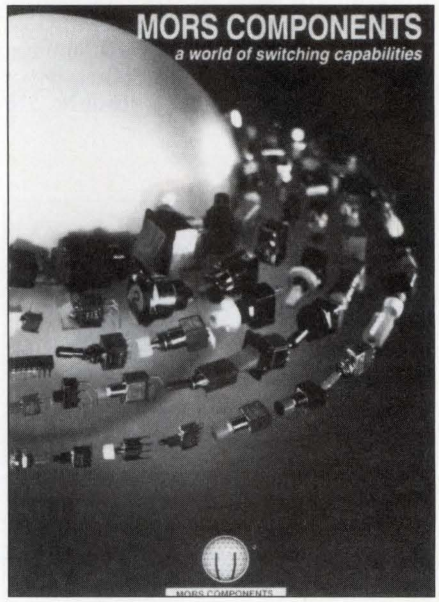
Catalog features discontinued semiconductor products. This 106-pg guide details the selection of devices available to be built to various screening levels and in various packages. **Rochester Electronics Inc,** Newburyport, MA. **Circle No. 534**

Catalog features optoelectronic products. This 88-pg short-form guide details optoelctronic products, including military high-reliability displays, optocouplers, LED lamps, infrared and fiber-optic emitters, and custom products. **Siemens Components Inc,** Cuptertino, CA. **Circle No. 535**

Application guide for low-temperature infrared sensors. This 16-pg guide is for users with little or no experience with low-temperature infrared sensors. Topics include infrared energy and how an infrared sensor works. The brochure also includes charts, graphs, and a list of applications. **Watlow Electric,** St Louis, MO. **Circle No. 536**

Literature on interconnection applications. This 8-pg brochure highlights interconnection technologies for improving pc-board building efficiency and reliability. It also describes additional interconnection products designed to meet electronic production needs. **Zierick Manufacturing Corp,** Mt Kisco, NY. **Circle No. 537**

Paper evaluates high-performance, VME-based embedded computer systems. *The SKYchannel Technical White Paper* reviews circuit-switched architectures, quick-ring architectures, and packet-bus architectures for communications on and between VME accelerator boards. **SKY Computers Inc,** Chelmsford, MA.
Circle No. 538



Selection guide of switches. This 50-pg product-selection guide lists switches manufactured in ISO 9002-certified facilities in Europe. The guide specifies washable and miniature toggle, rocker, and pushbutton switches and power toggle switches. In addition, the guide covers switch hardware and switch-sealing boots. **MORS/ASC,** Wakefield, MA. **Circle No. 539**

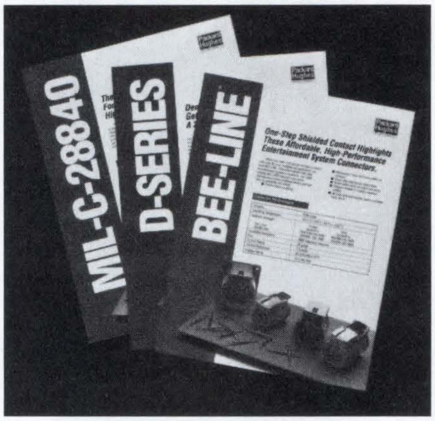
Guide highlights full-service testing. This 10-pg illustrated guide details the testing, procurement, and assembly of high-reliability electronic components. Four pages describe state-of-the-art testing services for discrete and high-complexity circuits. Two other pages cover the parts-management program, which combines procurement, testing, and just-in-time delivery of microcircuits and semiconductors. **Solid State Testing Inc,** Burlington, MA. **Circle No. 540**

Brochure provides application data for environmental test chambers. This 20-pg, color brochure details application, operational, and dimensional specifications for a line of environmental test chambers. The brochure also details controls, instrumentation, and chamber-design characteristics that help achieve specific environments. **Blue M Electric,** Blue Island, IL. **Circle No. 541**

Catalog describes 4-channel portable recorder. A 10-pg, 4-color brochure describes the Dash IV 4-channel field and lab recorder. The brochure contains specifications and a variety of full-size unretouched chart samples. **Astro-Med Inc**, West Warwick, RI. **Circle No. 542**

Handbook on distributed power architectures. This free comprehensive design guide covers the benefits of distributed power and details physical, electrical, and mechanical issues related to decentralized power architectures. It also describes component mechanical integrity and how each element in a distributed system affects reliability. **Ericsson Components AB**, Stockholm, Sweden. **Circle No. 543**

Brochure describing expandable, embedded PCs and modules. This 16-pg, 4-color catalog offers an overview of embedded-PC products, including single-board computers, PC/104 modules, and software tools. Also featured is a line of PC/104 modules, including analog-I/O, digital-I/O, VGA, and flat-panel controllers; communications; networking; solid-state-disk; and a Sound-Blaster-compatible audio card. **WinSystems Inc**, Arlington, TX. **Circle No. 544**



Connector data sheets. These data sheets describe three families of 20-gauge electrical connectors for high-performance and rugged field applications. The families include the Bee-Line connectors for airborne applications, the D-Series connectors for the most rugged environments, and the MIL-C-28840 connectors for shipboard applications. **Packard-Hughes Interconnect**, Irvine, CA. **Circle No. 545**

Brochure on electromagnetic shielding. *The Unseen Force* details a new diagnostic service that performs an on-site analysis of electromagnetic levels, provides an evaluation, and designs and installs a shielding solution. Free. **Lindgren R F Enclosures Inc**, Glendale Heights, IL. **Circle No. 546**

Brochure describes Visual Engineering Environment. This 12-pg, color brochure (Literature 5962-9239E) describes Hewlett-Packard's Visual Engineering Environment (VEE). The brochure focuses on VEE's graphical programming language, its benefits over traditional methods of generating code, and its impact on areas of automated test. Examples illustrate how VEE can be applied in jet-engine component testing, design verification for mobile phones, life testing for consumer appliances, and functional test for transponders. **Hewlett-Packard**, Palo Alto, CA. **Circle No. 547**

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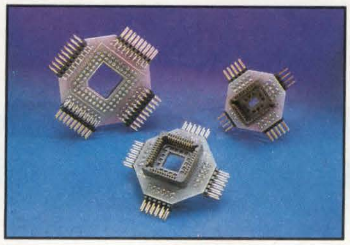

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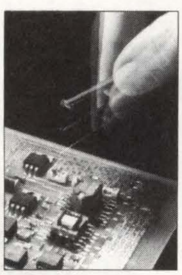

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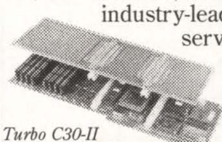

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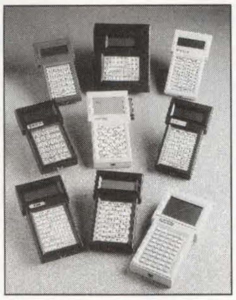

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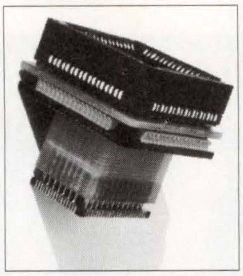

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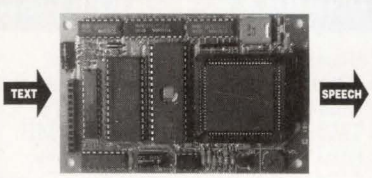

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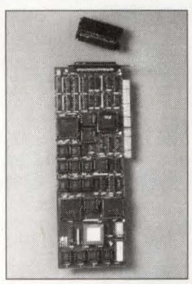

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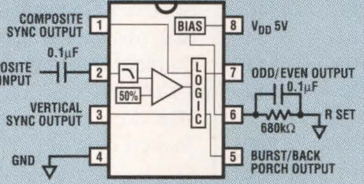

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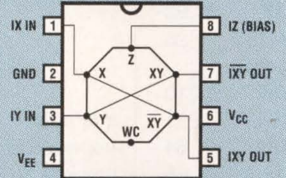

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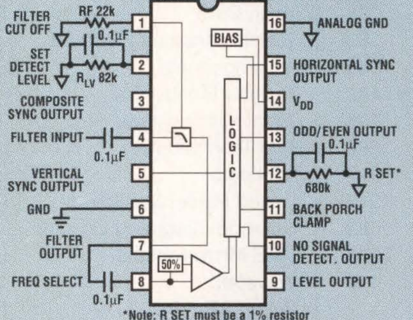

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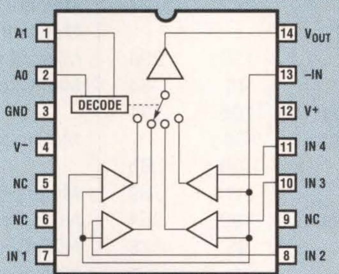

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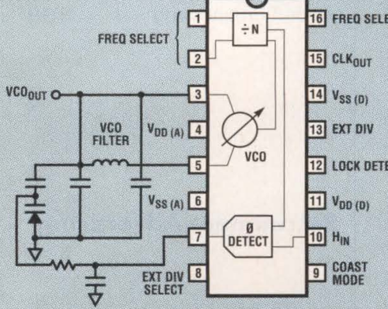

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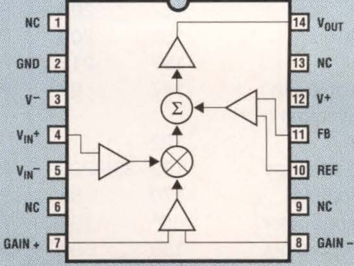

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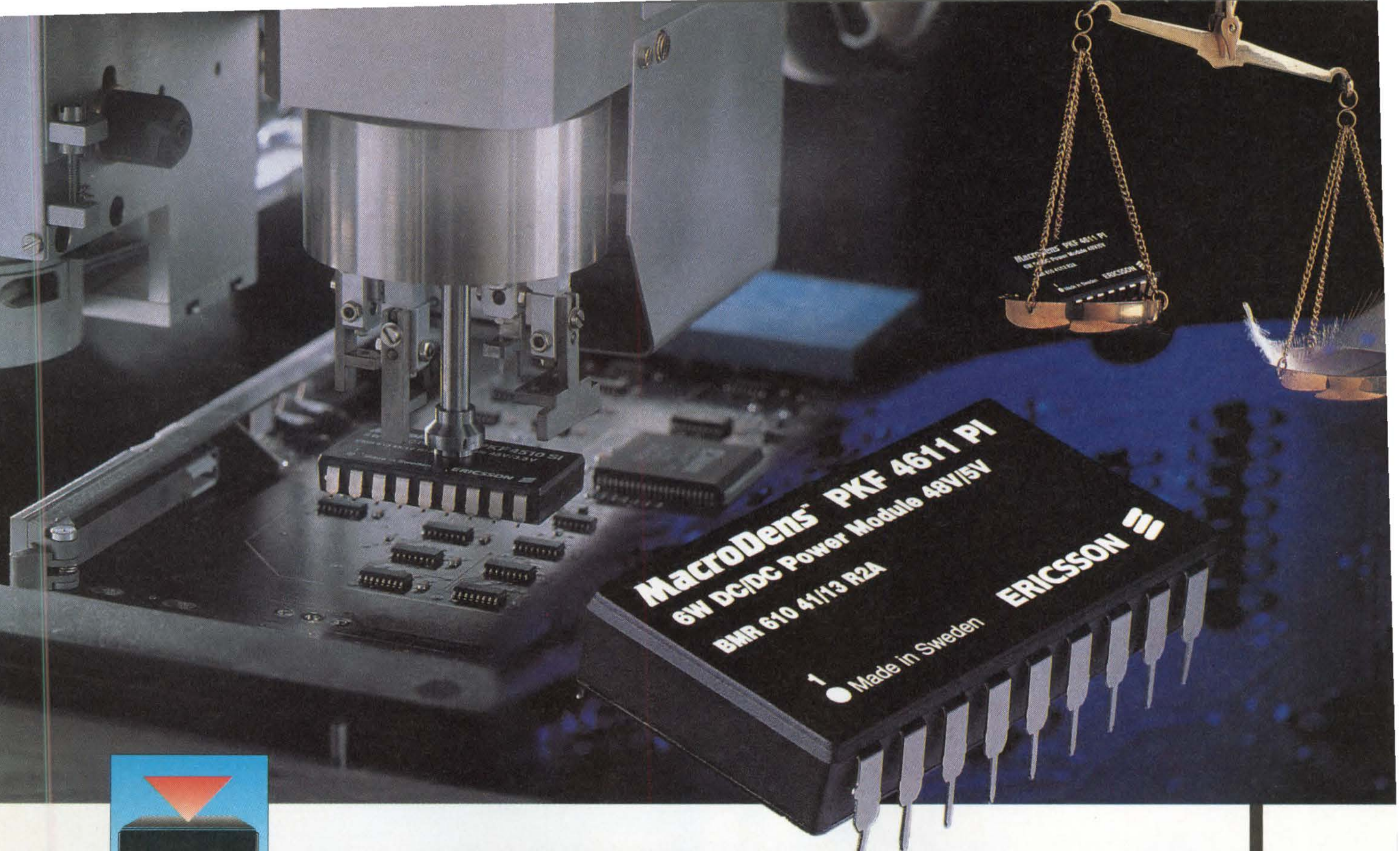

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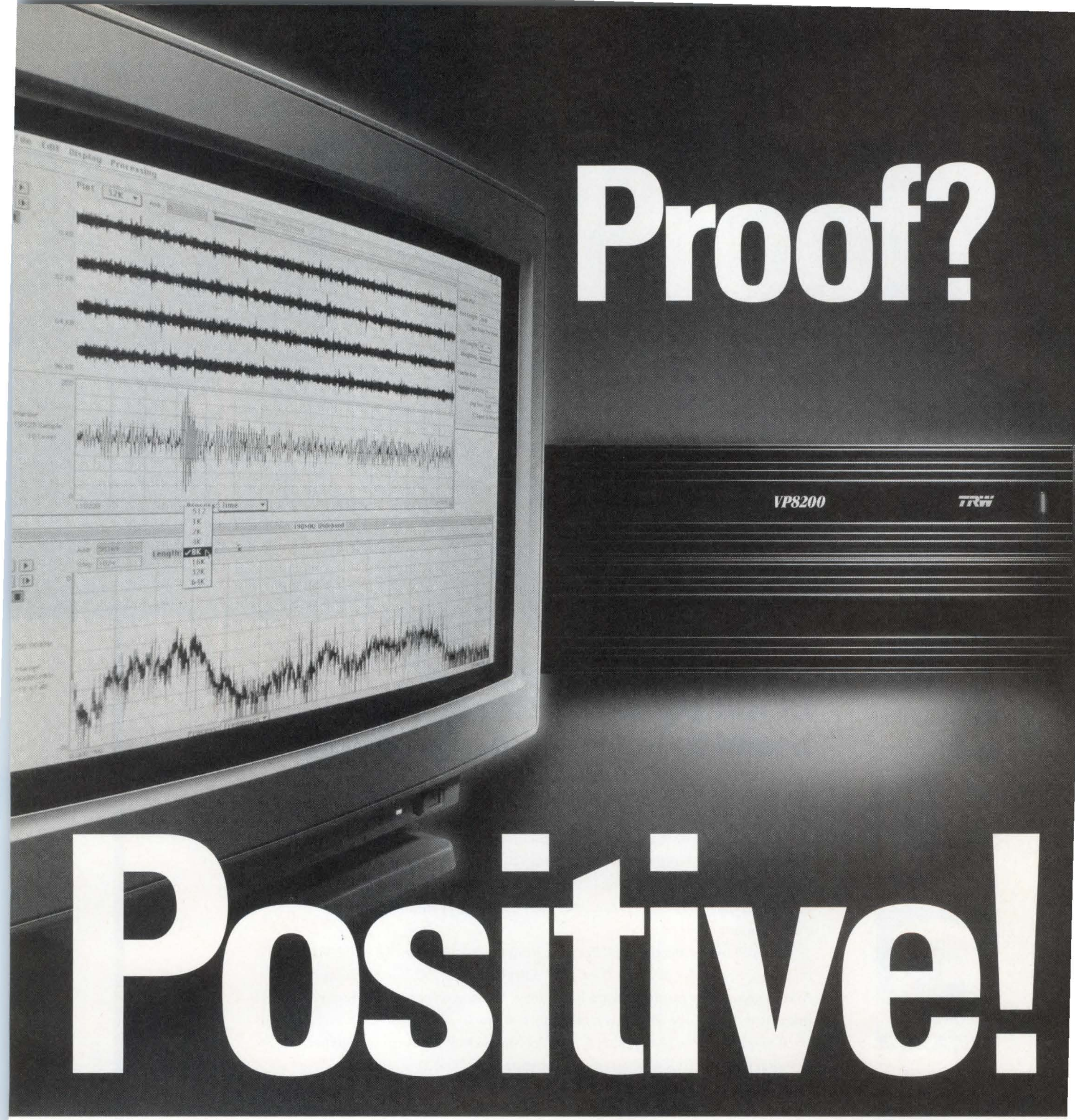

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DAC '94 and The Grateful Dead

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Just like there are sets of songs that get the Dead audience all rocking and sets that put everyone to sleep, there are DAC panels that have everyone talking and others that people walk out on. And, just like there are lightweight, occasional recreational drug users next to hard-core junkies in the Dead concert, there are occasional PC-based schematic-capture FPGA designers next to hard-core Unix-workstation-pumping, Ver-

ilog/Synthesis/ATPG, 200-MHz, 350k-gate GaAs ASIC designers at DAC. Both worlds employ "pushers" (salesmen) to provide the controlled substances (or controlled software) to the users for a hefty cut of the price.

Both subcultures wear special attire (tie-dyes or suits), trade bootleg material (concert tapes or EDA benchmarks), and converse in special words that have meaning only to members of that particular subculture ("electric Kool Aid," "ganja," "tripping" vs "ESDA," "PLI," and "regressions"). Just as there are unique personalities known in the Dead world (Timothy Leary, Bill Graham, Jack Kerouac, Tom Wolfe, Ken Kesey, and Hunter S Thompson), unique personalities also exist in the DAC world (Aart De Geus, Ron Collett, Bill Fuchs, Richard Goering, John Sanguinetti, and Joe Costello). But enough cultural anthropology, on with the awards!

WORST OVERALL SURPRISE AT DAC: An awful lot of attendees at DAC were caught off guard when the DAC exhibit hall closed a day early. Yes, technically it was buried in the schedule, but who reads schedules until the day of the event? (As a consequence, on Thursday, I found myself in a 2½-hour lunch/interrogation about industry trends with Ron Collett, a market researcher.) Also, DACnet had technical problems the first day that made it very difficult to log in and use. This meant many people were hard to contact because they blew off retrying the healthy DACnet on subsequent days. (A good DACnet note: they added telnet and ftp capability this year—great!)

MOST ANXIOUS EDA VENDOR(S): Virtually all of the non-Cadence- and non-ViewLogic-affiliated Verilog vendors were acting like debutantes at their first ball. Because Synopsys tipped its hand in the Verilog/VHDL wars in its failed bid for Chronologic, and Mentor is openly stating it needs a Verilog solution, the remaining independent Verilog vendors are terrified at

Every time an interesting exchange started, the moderator would actively step in and stop it.

the prospect of not being asked to dance.

WHAT EDA USERS THOUGHT WAS HOT: Because submicron and low-power design seems to be of interest to quite a few people these days, one of the hottest talked-about companies at DAC this year was Epic Design Technology. Its PathMill is an advanced static analysis tool, PowerMill is the leading dynamic power analysis tool, and TimeMill is the Spice-like accelerated analysis tool—all for submicron design.

The second hot topic was Chrysalis' Design Insight and Design Verifyer, two of the first commercial tools to take the formal verification approach to check for your design flaws. Because these products take a mathematical approach, Chrysalis claims that formal verification beats dynamic simulations by orders of magnitude in overnight regressions.

The third topic people were discussing was Synopsys' Behavioral Compiler, a tool that can take algorithmically written Verilog or VHDL and convert it to gates. Unlike regular synthesis that pretty much translates from the original structure in the source HDL, Behavioral Compiler literally juggles around things like registers, multiplexers, and adders to best fit the designer's scheduling goals.

The Redwood/Comdisco demo and the recent purchase of Redwood by Cadence were also on people's minds. (The big question is how many of the original Redwood R&D engineers are going to stick around?) Cadence's Verilog and VHDL co-simulation products were also hot. (Mix and match Verilog/VHDL source/libraries at will!)

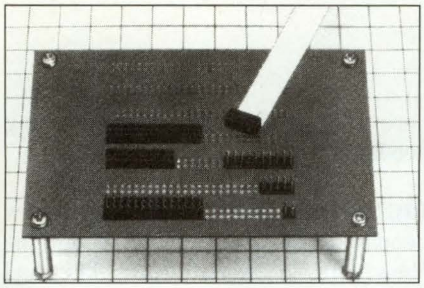
ArcSys is targeting Cadence in the place and route business, and Integrated Silicon Systems (ISS) also seems to be attacking Cadence on the mask-verification front (Dracula). Everyone goes after the big company.

BEST DAC PANEL: Tie between the EE Times/DEC/ViewLogic-sponsored DAC Forum and the DAC-sponsored Four CEO panel. What people liked about the DAC Forum was that they could "vote" electronically for what a particular panelist was saying at the moment, making it very audience interactive in a grand way. (Only users—no vendors—were given the handheld voting machines.) What the audience liked about the Four CEO Panel was a rare look at how these industry bigwigs see the world.

WORST DAC PANEL: The EE Times Benchmarking Summit. Lots of people on the panel and in the audience came prepared to discuss issues like the Actel Proposal, how Prep works, benchmarking clauses in nondisclosure agreements, and benchmarkers who blackmail EDA vendors. Instead, the moderator (a non-EDA-knowledgeable person) had everyone spend 2 hours partaking in a UN conflict-resolution exercise where we had to argue the opposing side's point of view. (Someone would say something and the moderator would then have everyone determine, "What should I write in the 'ASSUMPTION' column and in the 'WANTS' column on that statement?") Every time an interesting exchange started, the moderator would actively step in and stop it. As a result, all we could do was lightly touch some of the politics of benchmarking.

BEST AFTER-HOURS PARTY: Quickturn Emulation's Tuesday night bash. The company had a sit-down dinner after which the Temptations per-

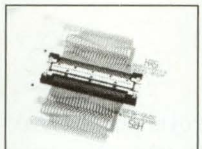
2mm PITCH CONNECTORS FOR STACKING



High densification in assembly is now possible with Hirose's A3C-A3D series of ultra compact 2mm pitch connectors for board-to-board stacking. When combining with other receptacles in the A3 family, a number of diverse lightweight applications are possible. Pin assortments on the receptacles are 2 through 20, plus 24, 26, 28, 32, and 50. Pin headers are available from 2 to 28. Ideal for HDD, FDD, VTR and mobile telephone production. When used board-to-board, the spacing between boards can be either 6mm or 5.1mm. For information, contact **Hirose Electric (U.S.A.), Inc.** 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 or FAX (805) 522-3217. For instant fax catalog information: 1-800-879-8071. Ask for number 5006.

CIRCLE NO. 70

High Density Board-to-Board Connector Proves Ideal for Downsizing PC's.

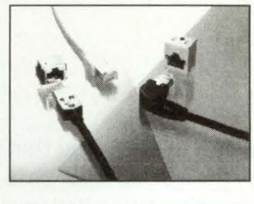


Developed for downsizing personal computers and workstations, Hirose is providing its 3200 series of high-density interface connectors (board-to-board) with 0.8mm contact spacing and 152 positions. The new 3200 series connector offers two rows of contacts with 0.8mm contact pitch. Its low profile is only 5.5mm from the PCB with a reliable two point contact pin; each pin is protected by an insulator wall against deformation caused by severe handling, such as twisting.

For further information, contact **Hirose Electric (U.S.A.), Inc.,** 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 or FAX (805) 522-3217. For catalog information by fax: 1-800-879-8071, ask for # 8004.

CIRCLE NO. 72

Hirose Shielded Modular Connectors



Hirose Electric has announced the TM11 Series of shielded modular connectors for computers, office automation equipment, and telecom. The TM11 series offers the only connectors specifically designed and compatible with industry standards to provide RFI/EMI shielding and protect against ESD discharge. The low profile TM11 has eight signal lines and a grounded shield. 6-8 positions currently available.

For further information, contact the sales department, **Hirose Electric (U.S.A.), Inc.,** 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 or FAX (805) 522-3217. For instant fax catalog information: 1-800-879-8071, ask for # 3002.

CIRCLE NO. 73

Great Designs Are A Snap With Hirose Circular Connectors!

The uncomplicated design of the HR10A Snap-Lok™ circular connector series assures rugged dependability and enables rapid, error-free mating and unmating—even under the most adverse situations.

Three shell sizes are available (7mm, 10mm and 13mm) with insert arrangements from 4 to 20 contacts; in-line receptacle jacks are also available with crimp or solder contacts.

The handsome, high-tech design and sturdy construction of Snap-Lok™ connectors ensure engineering integrity. That's why so many leading manufacturers worldwide insist on only Hirose HR10A series connectors.

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From the birth of the SMT revolution, Hirose engineers have been a step ahead of the pack. They have been applying their creativity and experience to develop and manufacture what OEM's need for cutting-edge, miniature, SMT designs.

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CIRCLE NO. 74

formed. Although it had appeared that ViewLogic was going to win this award with a ferry ride to a sit-down dinner on Harbor Island and comedian (everyone was schmoozing like crazy to get tickets before this event), the comedian turned out to be a flop in many people's opinion. (He was more caustic than funny: Attendees were stuck laughing nervously to be polite.) It was rumored that LSI gave 100 of its "most favored customers" a regatta in San Diego bay with six people per sailboat. It sounded like fun, but was too limited a party to qualify for an award.

BEST USE OF DAC TERRAIN FOR A PARTY: Synopsys' wild night at the zoo. The moment you got off the bus, there was a table full of beers with helpers saying "Take two! The tour's 45 minutes," as they shooed you onto the double-decker open-air tour bus to go around the zoo. (Harvey Jones, Synopsys' chairman, who was sitting two seats behind me, commented on how excited I was when we saw the sheep exhibits.) Stumbling off the bus, we got more beer and great predinner munchies at a party where we could pet six different animals. Then we had a choice of a swordfish or chicken dinner in an open-air Gilligan's Island setting. Afterwards, all 300 of us were given Irish coffee as we walked to the firedrummer's performance. (In contrast, Collett reports that Cadence also had a dinner at the San Diego Zoo for about 65 people with no tour and three petting animals brought in after dinner. Mentor did something of similar ilk and size at the San Diego Aquarium.)

BEST RARE DAC FREEBIE: Summit Design's denim jackets. They were well made with a small, tasteful "Summit" patch on the left shoulder. Total number given away: 175 (120 went to its Pacific Rim distributor, 25 on the showroom floor, and 30 for schmoozers).

BEST COMMON DAC FREEBIE: The Official DAC gym bag. It's sturdy, useful and has a tasteful royal purple, teal, and black color scheme. (One user wondered if IBM was "in" on the bag's color scheme because all the IBM shirts matched it *exactly*.) Runners Up: a tie between the ViewLogic soccer ball and the Epic Design Technology sports radio. (ViewLogic consciously chooses a high-quality freebie that's a pain to carry back on the plane so everyone can see you carrying it in the airport. They did it last year with the baseball bat and this year with the soccer ball. The message I get with this type of freebie is "we're hard to work with.") The Epic Design Technology sports radio is great (batteries included!) but *nowhere* near the quality of a Sony.

It took five years to get fully debugged Verilog libraries from ASIC vendors—why should Vital be different?

MOST UNEXPECTED DAC FREEBIE: Quad Design's hammers. (Racal-Redac and Analogy gave out tape measures. Are their marketing managers a little confused about what the hardware-design industry is?) Runner Up: Aptyx's coconuts. Huh?

MOST CONTENT-FREE VENDOR PRESENTATION: Synopsys' talk on submicron design. I'm told it was 40 minutes and only two things were said: design is headed toward the submicron level, and there's going to be more transistors on chips in the future. A close second was Cadence's re-engineering talk where the company spent 20 minutes vaguely discussing customer successes and stating that, "Cadence is here to help with your re-engineering needs."

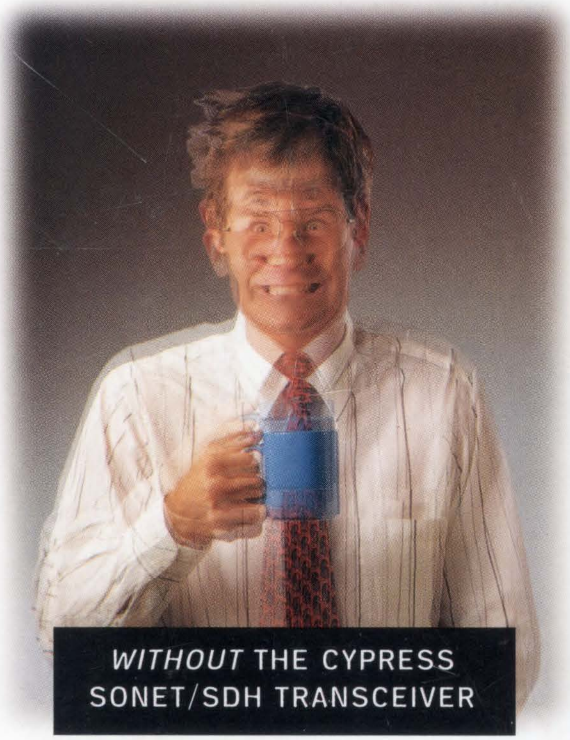
BIGGEST VENDOR LIE: Quite a few people told me about going through the ViewLogic Soccer Ball Quest. They had to sit through a "VHDL is better than Verilog" talk by a ViewLogic salesman. The salesman confidently said that "Vital is just around the corner! VHDL handles concurrent processes better!" These statements surprised the experienced simulation users because they've always described Verilog as "just like C but with wires, registers, and constructs to handle concurrent processes." Plus, it took five years to get fully debugged Verilog libraries from ASIC vendors—why should Vital be different? Ready for a discussion on these topics, they asked the salesman to explain his reasoning. The salesman replied, "Well, that's what I've been told."

WHAT DO YOU MEAN "WHAT'S NEW?": A long-time customer asked people in the Mentor booth: "What do you have new this year?" They were unable to answer with anything other than a simple design manager tool.

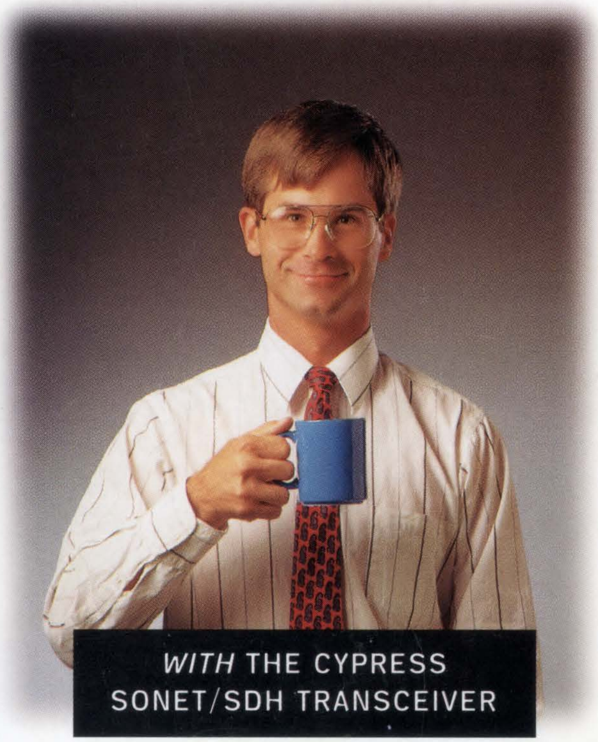
MOST PERSONALLY GRATIFYING DAC PANEL: The HDL Summit. Ron Collett moderated six panelists ranging from Verilog bigots to people using both to VHDL bigots. As usual, Collett tried to conclude the panel with his spin that VHDL was where everyone was going, etc. Just to annoy him, I pointed out how, years ago, a researcher at Dataquest had made a now-embarrassing prediction that VHDL users would outnumber Verilog in early '92—a prediction that turned out to be greatly exaggerated. That Dataquest researcher was Ron Collett.

John Cooley, an EDA consumer advocate and founder of the outlaw E-mail Synopsys Users Group (ESNUG), lives on the Holliston Poor Farm in Massachusetts. He raises sheep and is an EDA- and ASIC-design instructor and project-in-crisis consultant. He can be reached at "jcooley @world.std.com" or at (508) 429-4357.

DELICIOUS ATM, WITHOUT THE JITTERS.

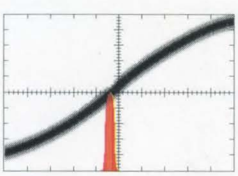


WITHOUT THE CYPRESS SONET/SDH TRANSCEIVER



WITH THE CYPRESS SONET/SDH TRANSCEIVER

Here's a wake-up call for anyone designing-in ATM functionality: the CY7B951 SST™ (SONET Serial Transceiver) clock recovery chip from Cypress. With its miniscule jitter of just 10 ps, the SST is as close as you can get to guaranteed flawless performance in your ATM environment.



Industry's Lowest Jitter

In fact, it is the only solution to support both major ATM application frequencies (51.8 OC-1 and 155.52 MHz OC-3.)

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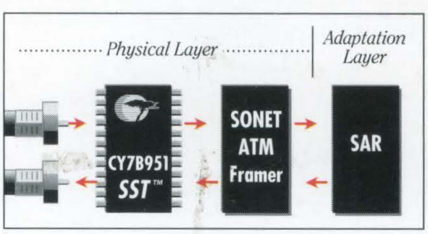

By using advanced BiCMOS technology, the SST consumes a miserly 50 mA, for power savings of up to 50% over competitive devices. And its loop-back testing capabilities enable in-system diagnostics.

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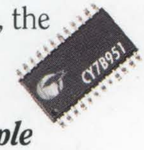

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