EDN®

A CAHNERS PUBLICATION

August 20, 1992

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

VOTE FOR EDN's INNOVATION FINALISTS PG 39

Special Report:

Ruggedized, off-the-shelf computers gear up for military use

pg 118

SPECIAL ISSUE

Military Technology

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Multirate filters alter sampling rates even after you've captured the data pg 129

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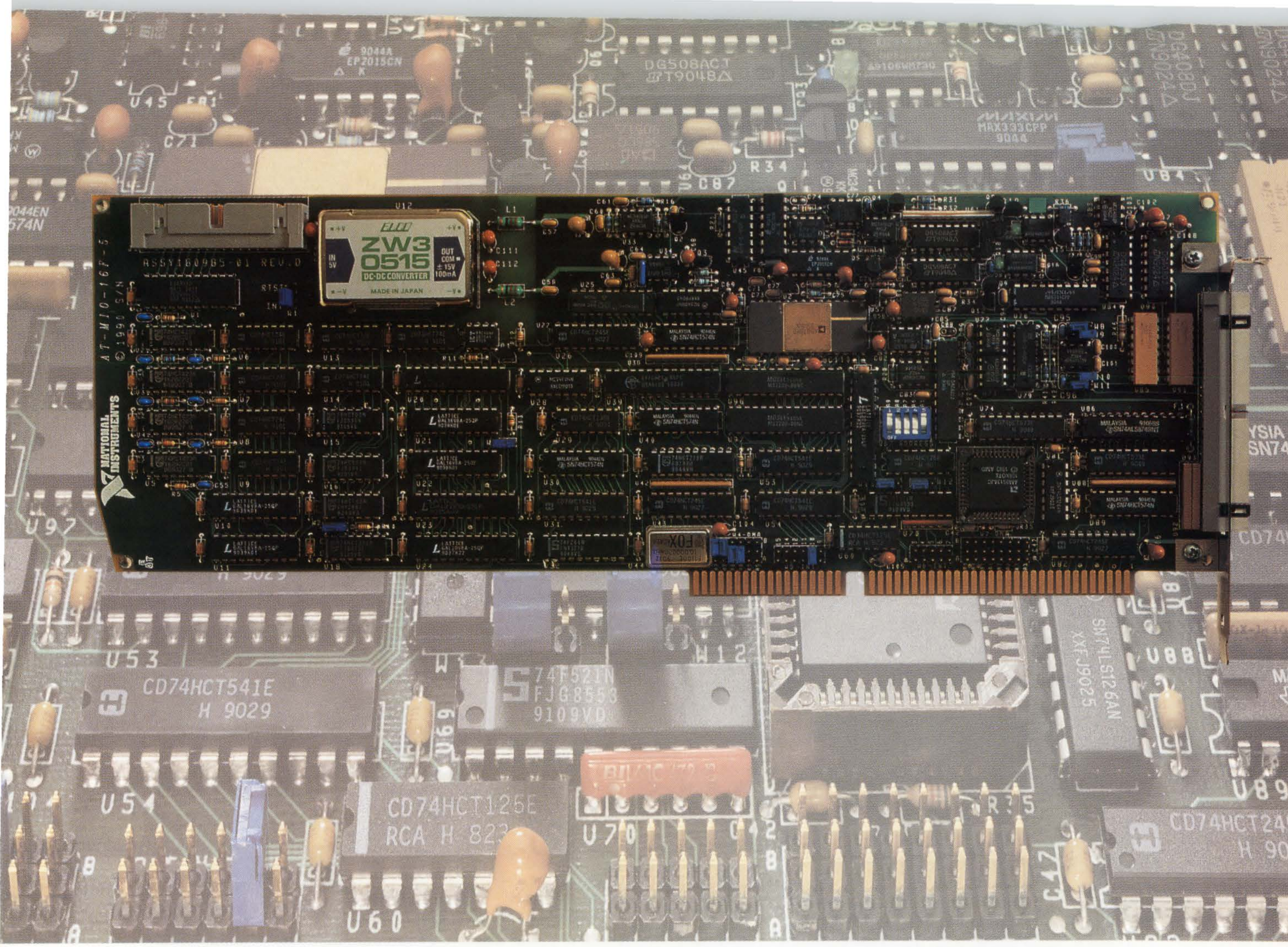

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CIRCLE NO. 119

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Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
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Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) $14.95 ZYSW-2-50DR (SMA) 59.95		

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F141 REV. D

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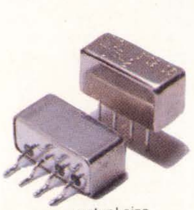

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SPECIFICATIONS

Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB) $\overline{X}$	■ Conv. Loss (dB) δ	Isol. L-R (dB)	Price,$ Ea. 10 qty
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9..95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.
■ $\overline{X}$ = Average conversion loss at upper end of midband ($f_U/2$)
δ = Sigma or standard deviation

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CIRCLE NO. 4

F 145 REV. F

EDN
MAGAZINE EDITION

August 20, 1992 VOLUME 37, NUMBER 17

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

On the cover: Commercial, off-the-shelf (COTS) ruggedized computers offer computer manufacturers and the government the chance to benefit from military belt tightening. Because COTS do not have to meet full military specs, everyone involved saves time and money. (Photo courtesy Mercury Computer Systems Inc; concept by Jim Caron; photography by David Petty Photography; model tanks by Chicago Model International) . . . . **PAGE 118**

MILITARY TECHNOLOGY SPECIAL ISSUE

Vote for Innovation, Win a Calculator

Your votes will determine the winners in EDN's Innovations and Innovator of the Year competition. Use the bound-in ballot to make your choices. **39**

SPECIAL REPORT

Ruggedized computers

Firms that develop and produce ruggedized computers have obtained new customers among prime contractors who no longer have to create computers that meet full military specifications.
—J D Mosley, Technical Editor **118**

DESIGN FEATURE

Multirate filters alter sampling rates after you've captured the data

You've digitized an analog signal, but the sampling rate is too high—or too low—for your system. Multirate filters can't supply missing information, but they can alter the effective sampling rate after you've acquired the data.*—John Allen Mitchell, Comdisco Systems* **129**

TECHNOLOGY UPDATE

Board-level protective devices provide insurance against electronic disaster

By augmenting primary system protection with some secondary protection at the pc-board level, you can greatly enhance the reliability of your system.*—Tom Ormond, Senior Technical Editor* **75**

Continued on page 7

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- Extended Operating Temperature
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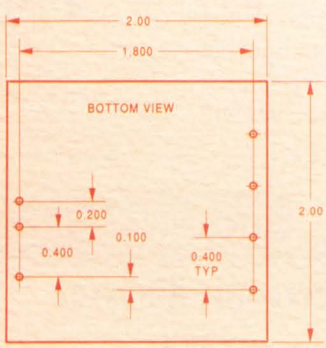
- TTL-compatible ON/OFF control
- Metal Case Shielding
- Single V_{OUT}: 2.1, 3.3, 5, 12, 15V
- Dual V_{OUT}: ±5, ±9, ±12, ±15V
- Triple V_{OUT}: 5, ±12V and 5, ±15V



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DC/DC Converters Single/Dual/Triple 25 *New* Models

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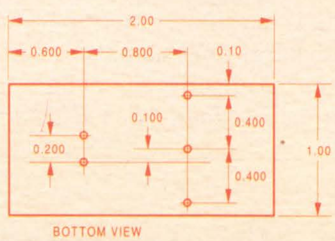
- Metal Case Shielding
- World's *ONLY* Wide Range 5V_{IN}
- Extended Operating Temperature
- Single V_{OUT}: 3.3, 5, 12, 15V
- Dual V_{OUT}: ±5, ±12, ±15V
- Triple V_{OUT}: 5, ±12V and 5, ±15V



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DC/DC Converters Single/Dual Output 15 *New* Models

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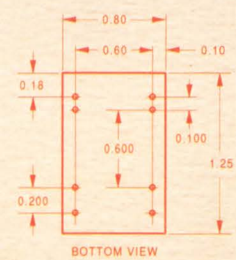
- V_{OUT}: 5, 12, 15, ±12, ±15



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CIRCLE NO. 5

EDN
MAGAZINE EDITION

August 20, 1992

Continued from page 5

TECHNOLOGY UPDATES

In-circuit programming instruments infiltrate commercial applications — 91

Soldering-in EPROMs and EEPROMs simplifies manufacture and enhances reliability but complicates programming. Commercial in-circuit programming instruments overcome these complications. *—Brian Kerridge, Technical Editor*

Portable data carriers: Small, rugged memories put data where it's needed — 99

Cleverly packaged memory devices put data in places where a computer can't go. Some even contain an RF transponder for wireless access.*—Gary Legg, Senior Technical Editor*

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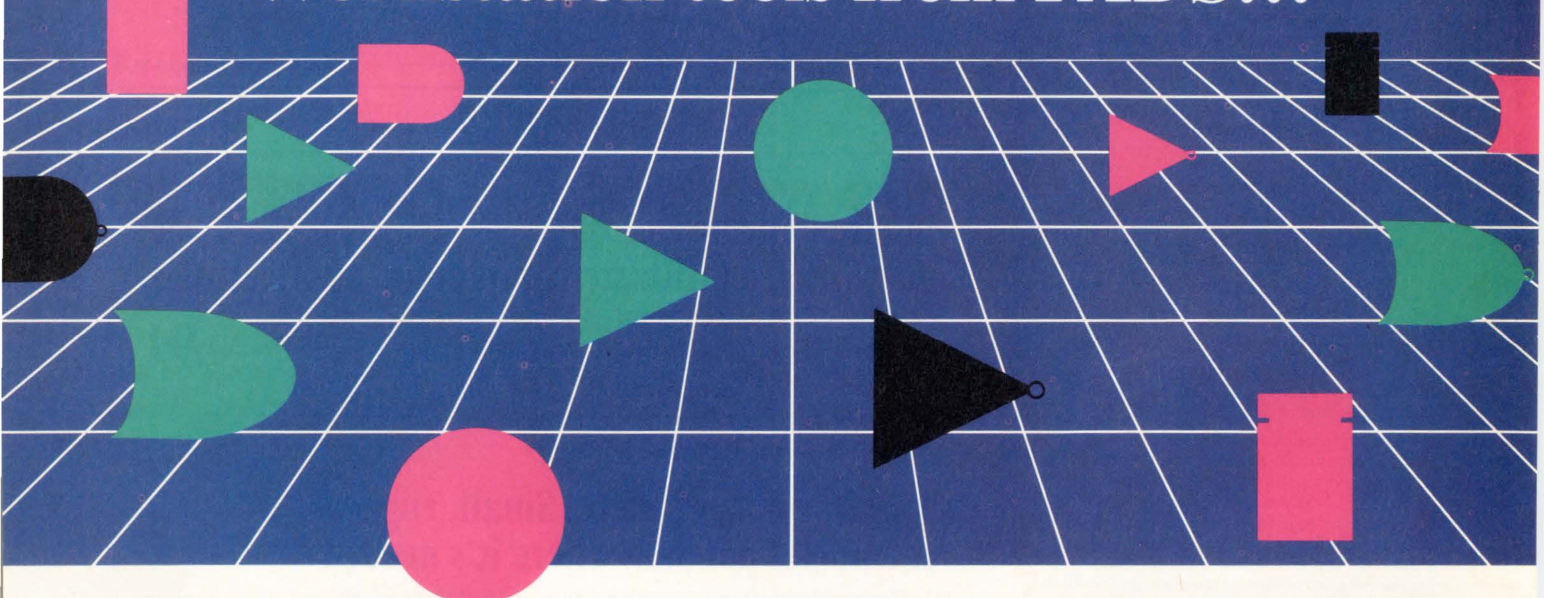
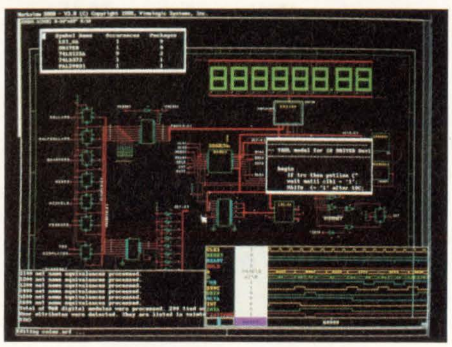
FINALLY, One Company offers you the Power *and the ease*... with integrated Workstation tools from PADS...





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- ▲ Multiple windows for probing simulation results
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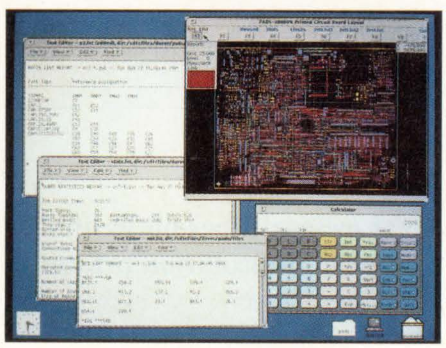

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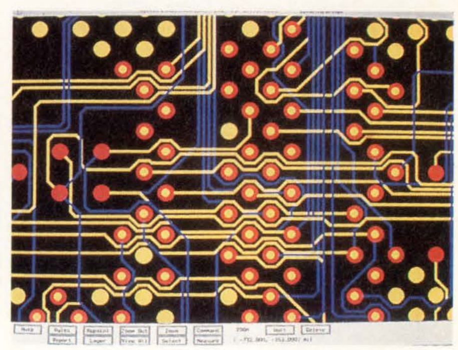

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CIRCLE NO. 20

INSIDE EDN

A summary and analysis of articles in this issue

In this election year, we're asking you to vote twice—once in November and once now.

When you turn to pg 39, you'll read descriptions of the finalists in **EDN's annual Innovation and Innovator of the Year Competiton.** You'll also find a ballot with a list of this year's finalists. Vote for your favorite products and people on the postage-paid ballot and return it by September 14. This year, you can even fax the ballot by using an 800 number. By the way, every person who votes will be eligible to win an HP calculator. See the details on the back of the ballot.

EDN was inundated with candidates in our annual Innovation crusade. "Entries were way up this year and that made the judging especially difficult," says Executive Editor Steve Leibson. "In fact, we had to use a piece of software called Best Choice 3 from Sterling Castle Software to do the judging. It allowed us to judge entries two at a time instead of 30 all at once. All of the judges were pleased with the results." After making the final determinations, the judges (EDN's home-office technical editors) wrote up the descriptions you'll see in our special Innovation section.

We've done our work—now it's up to you. Tell your peers what you think of their efforts by marking your ballots.

Now to the issue you're holding in your hands—our annual Military Technology Special Issue. The Special Report on **ruggedized computers** was assigned to Technical Editor J D Mosley, who investigated what's been happening in that area since the purse strings have been tightened on military spending. She says that although government spending is down overall for military purchases, electronics is not an area that's feeling the pinch. "The government is trying to work smarter and more efficiently, and that means more electronics and less human intervention," says Mosley.

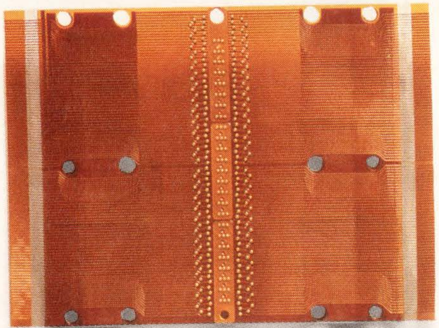
More and more, contractors are evaluating off-the-shelf ruggedized computers instead of demanding top-of-the-line customized units. But just how much ruggedization does a manufacturer need to build into its computer to grab a good share of the available purchasing dollars? Mosley says everyone is still feeling their way along, but she believes that the military is providing a good opportunity for the off-the-shelf computer industry to pick up some much-needed business.

Military electronics in general needs a high level of protection against transients to satisfy use in harsh environments. Customarily, protection has been afforded on the system level. That's just not enough, says Senior Technical Editor Tom Ormond. He sees the need for **board-level protection devices,** especially when you take into consideration that many high-speed components use submicron fabrication technologies. These components are inherently more prone to damage caused by surges.

Continuing with our military theme is an article by Technical Editor Brian Kerridge on **in-circuit programming.** Traditionally boosted by the aerospace and military sectors, in-circuit programming is beginning to break through to the commercial side because of the problems in handling small-package devices in manufacture. Kerridge covers the issues and the instruments.

Not all of the articles in this issue are defense-related. For example, read Senior Technical Editor Gary Legg's report on **portable data carriers.** Not only does he touch all the bases, but he throws in a few unusual applications--just for the fun of it.

Joan Morrow Lynch
Managing Editor

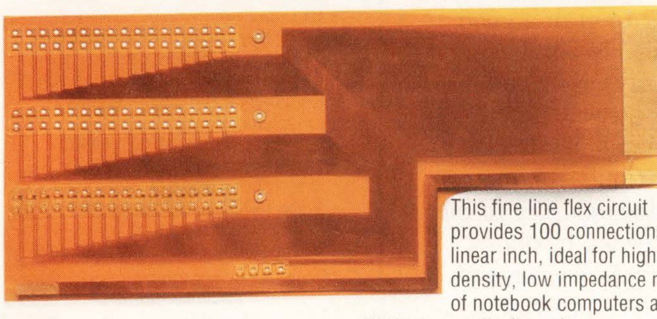


RSC#60

Systems using fast clock rates—as in telecommunications—need the controlled signal impedance of our mother-daughterboard interconnect.

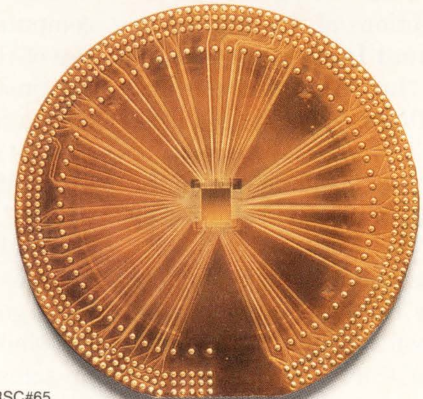
RSC#61

Our design-for-manufacture process benefits multilayer rigid-flex circuits that require the electrical integrity and high reliability critical for applications like infrared imaging and target acquisition systems.



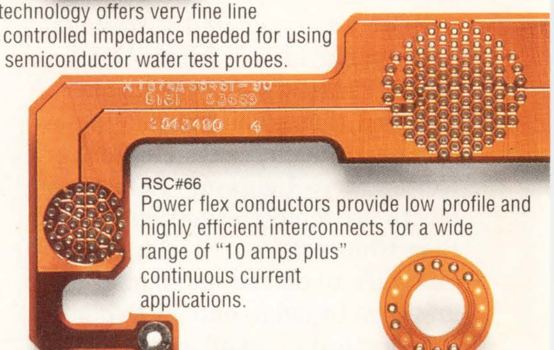
RSC#64

This fine line flex circuit provides 100 connections per linear inch, ideal for high density, low impedance needs of notebook computers and medical monitors.



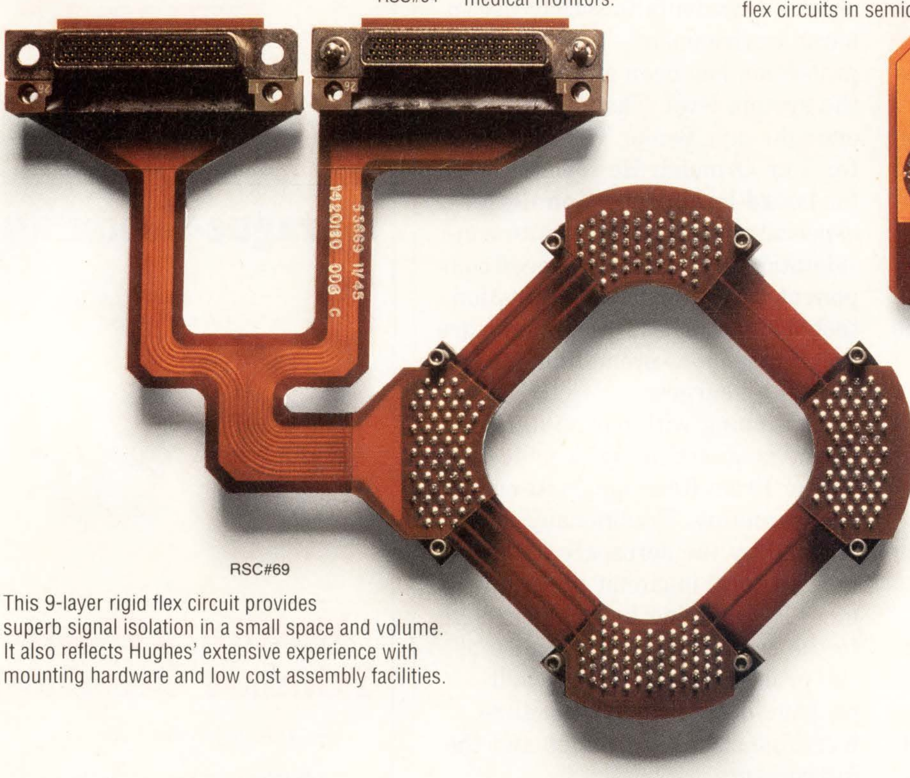
RSC#65

Our Gold Dot technology offers very fine line densities with controlled impedance needed for using flex circuits in semiconductor wafer test probes.



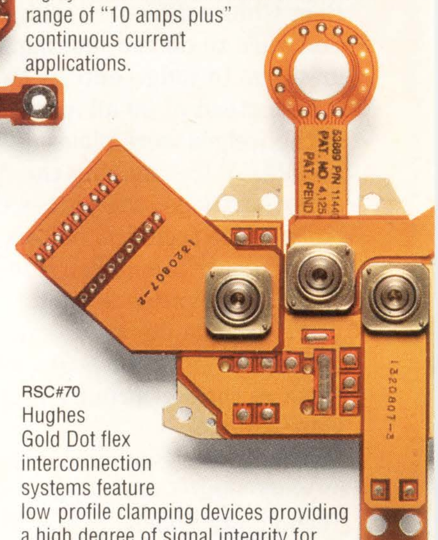
RSC#66

Power flex conductors provide low profile and highly efficient interconnects for a wide range of "10 amps plus" continuous current applications.



RSC#69

This 9-layer rigid flex circuit provides superb signal isolation in a small space and volume. It also reflects Hughes' extensive experience with mounting hardware and low cost assembly facilities.



RSC#70

Hughes Gold Dot flex interconnection systems feature low profile clamping devices providing a high degree of signal integrity for ultrasound equipment and high speed memory devices.

AS YOU CAN SEE, WE'RE

No other flex circuit company can do as much for you as Hughes Interconnect Systems. For a

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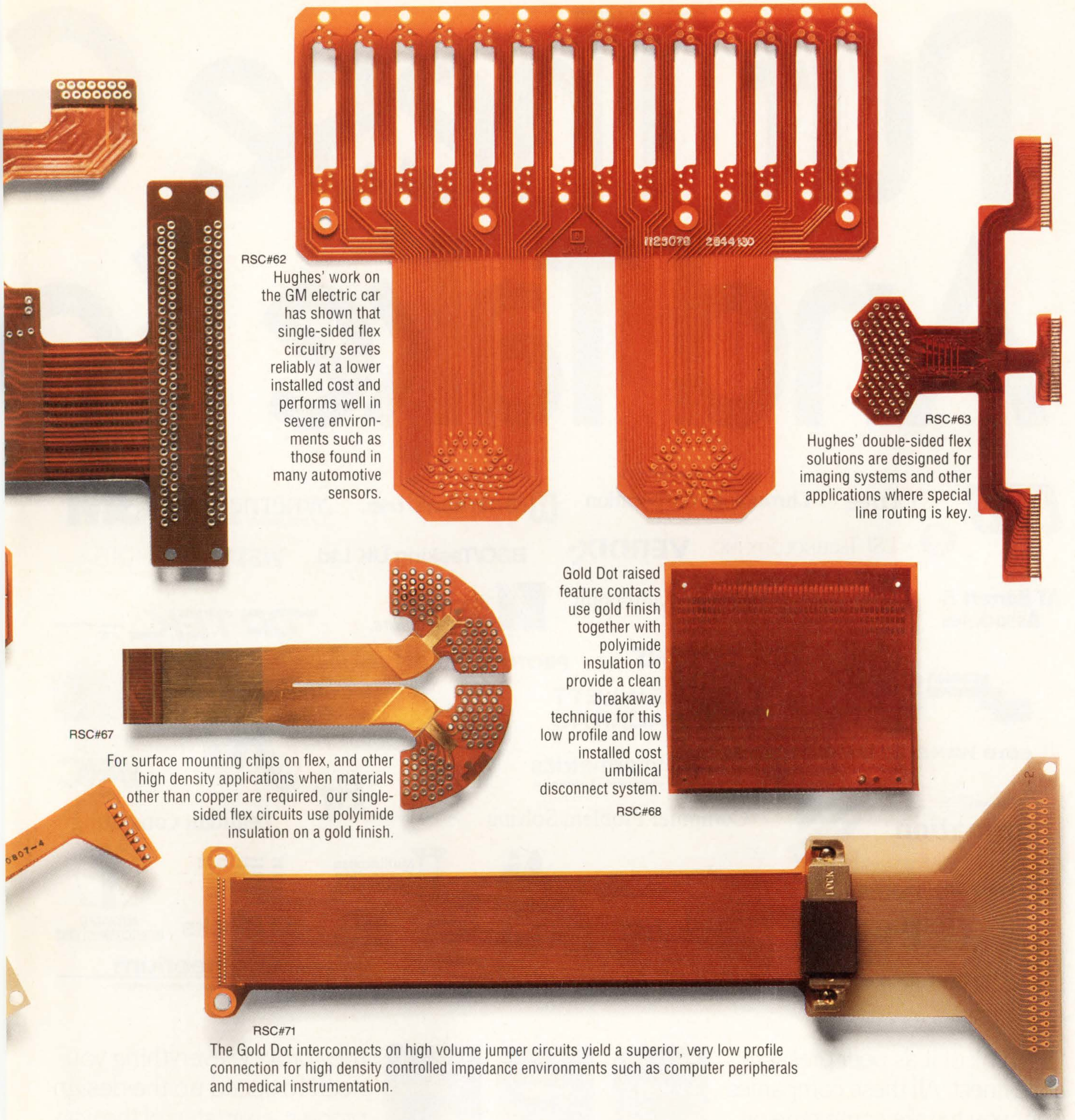

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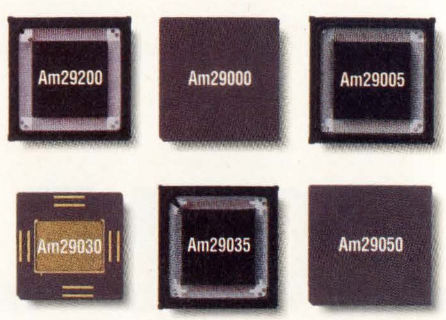
Think of it as peer pressure at its finest. All these companies want you to take some time off: Time off your design cycle, and your time to market. They're the Fusion29K℠ Partners, and their support helps make the 29K™ Family of embedded RISC processors so fast and easy to use.



The 29K Family includes parts for every conceivable application–from the brand new low cost, easy-to-use Am29200™ to the top-of-the-line Am29050™ with on-chip floating point coprocessor.

Fusion29K Partners include over 100 reputable companies with more than 200 different support products. Together, they provide everything you need to speed up the design process, every step of the way. From evaluation, to system and hardware design, software development, hardware and software integration, system debug—all the way to production.

The Fusion29K Partners have a whole arsenal of time and labor saving devices. You'll find emulators, simu-

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lators, CASE and CAE tools, C compilers, machine and source level debuggers, logic analyzers, and manufacturing support of all kinds. All of the highest quality and performance standards.

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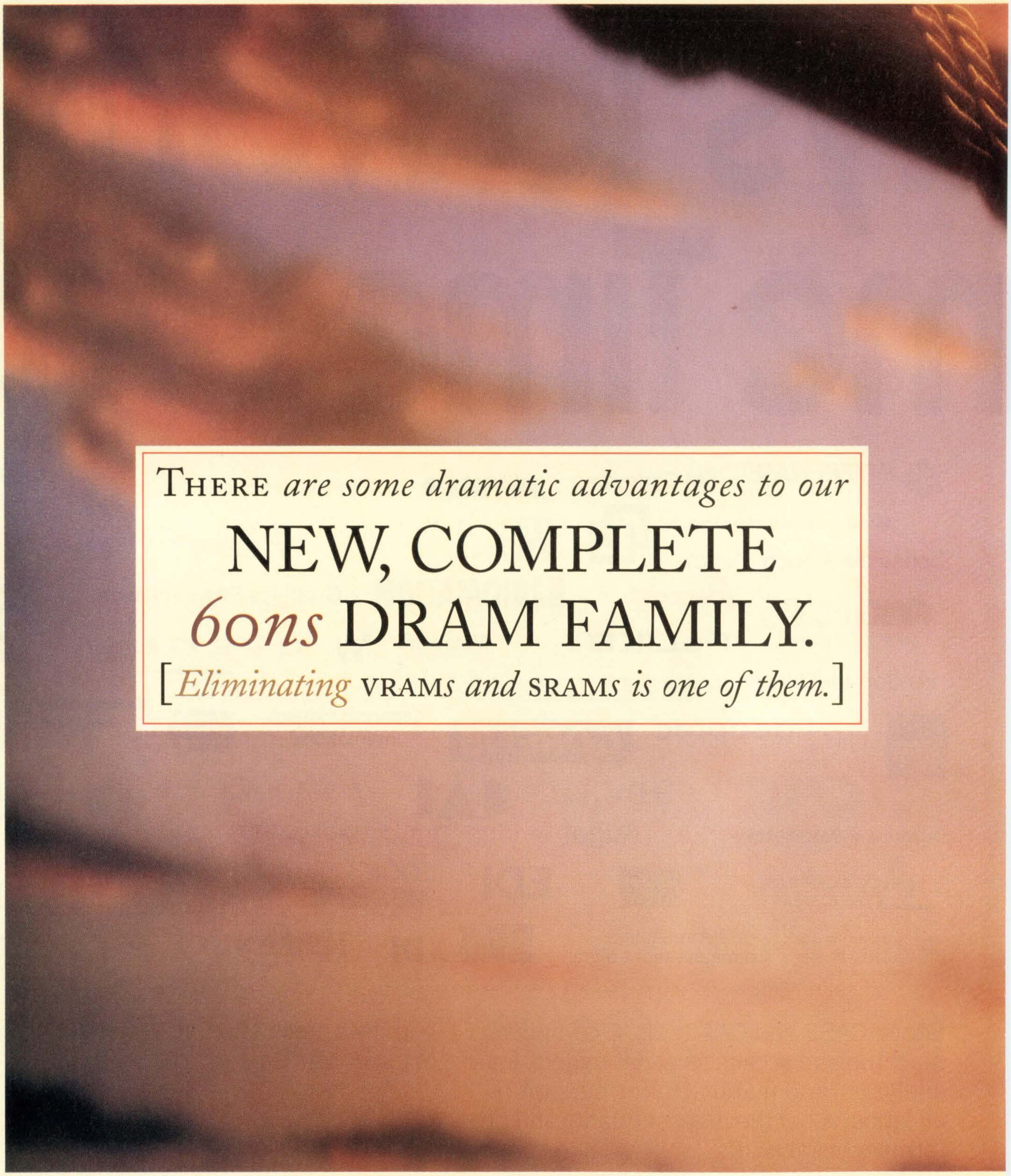
For more information on the 29K Family of embedded RISC processors and Fusion29K support, call AMD today: **1-800-292-9263 Ext. 3.**

With this much support, you may be able to take some time off for yourself.

Advanced Micro Devices

CIRCLE NO. 24

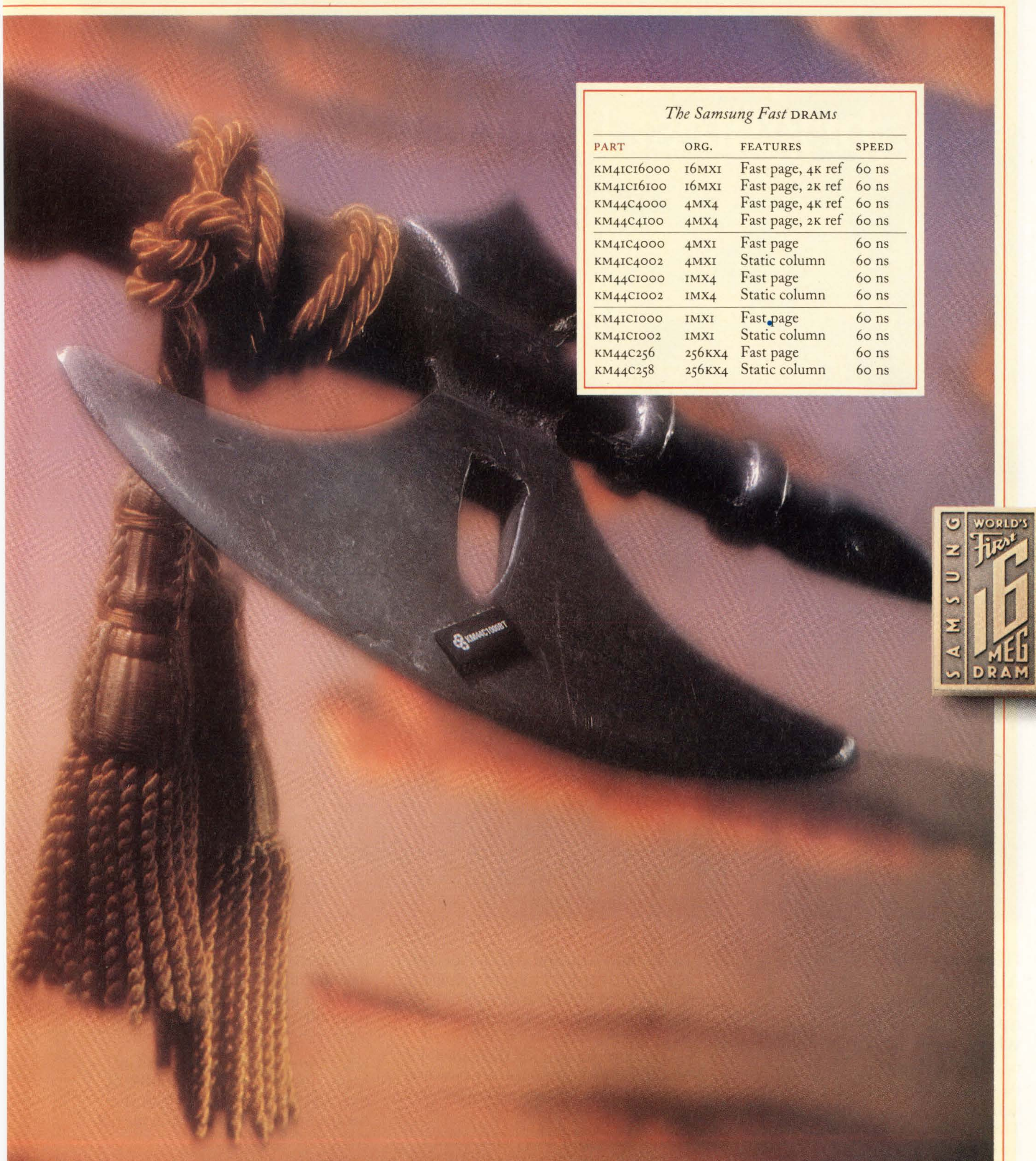


At Samsung, we're not content to have brought the world its first 16-meg DRAM.

We're extending the gains we've made in this important segment of technology, by introducing a complete family of DRAMs at the highest speeds in use—60 nanoseconds.

These are speeds that will let designers of many 386 systems eliminate SRAM cache altogether. And for many high-end graphics OEMs, it will be possible to eliminate VRAMs.

Of course, one result of those things will be that you'll be able to lower the axe, so to speak, on unwanted costs.



The Samsung Fast DRAMs

PART	ORG.	FEATURES	SPEED
KM41C16000	16MX1	Fast page, 4K ref	60 ns
KM41C16100	16MX1	Fast page, 2K ref	60 ns
KM44C4000	4MX4	Fast page, 4K ref	60 ns
KM44C4100	4MX4	Fast page, 2K ref	60 ns
KM41C4000	4MX1	Fast page	60 ns
KM41C4002	4MX1	Static column	60 ns
KM44C1000	1MX4	Fast page	60 ns
KM44C1002	1MX4	Static column	60 ns
KM41C1000	1MX1	Fast page	60 ns
KM41C1002	1MX1	Static column	60 ns
KM44C256	256KX4	Fast page	60 ns
KM44C258	256KX4	Static column	60 ns

But the advantages don't end there. Reduced parts count will mean greater reliability, lower power consumption, and reduced assembly costs.

We offer the fast DRAM in 1Mb, 4Mb, and even 16Mb densities. Which not only puts us on the cutting edge. But will do the same for you.

For more information, please call 1-800-446-2760 or 1-408-954-7229 today. Or write to DRAM Marketing, Samsung Semiconductor Inc., 3655 No. First St., San Jose, CA 95135.

SAMSUNG

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CIRCLE NO. 25

EDITED BY SUSAN ROSE

Finite element program for electronic applications

MSC/EMAS version 2 from MacNeal-Schwendler Corp is a set of tools for dealing with problems in EMI and crosstalk, antennas, electrical apparatus, and RF and microwave equipment. The software applies the finite-element analysis method to problems in each application area.

For EMI/crosstalk, the software determines electromagnetic interference, coupling, and shielding effects at frequencies from dc to RF. The electrical-apparatus section of the tool computes electrical and electromechanical parameters for transformers, actuators, motors, and nondestructive evaluation tools, and electric-field devices such as switch gear and insulators. The antenna section of the software calculates S parameters, far-field radiation patterns, current densities, and other parameters of interest to antenna designers. The RF/microwave part of the tool gives a complete picture of field behavior. The sofware runs on 11 different supercomputers, mainframes, and workstations, including models from Cray, HP, IBM, Sun, and DEC. You lease this software at a rate that reflects the hardware you are using. For example, base products for workstations described above start at $300 per month. The MacNeal-Schwendler Corp, Los Angeles, CA, (213) 258-9111.

Top-down meets bottom-up in ASIC and IC design

At this year's Design Automation Conference, Silvar-Lisco announced a 3-year, OEM agreement with High Level Design (HLD) Systems to integrate Silvar-Lisco's place-and-route software with Cadence Design Systems' tools. The resulting product, a floorplanner from HLD Systems called Design Planner II, lets you use Silvar-Lisco's place-and-route products, SC (structured custom), and Gards (gate array) from Cadence Design Framework I and II. The layout tools provide 3-level metal placement and routing for mixed-macro and standard-cell designs without the difficulty of using an encapsulated tool or incurring the costs of performing software integration. Available now, the floorplanner costs $25,000 for the SC family and $35,000 for the Gards family. Both families run on the HP700 and Sun SPARCstation. Cadence Design Systems, San Jose, CA, (408) 943-1234. HLD Systems, Santa Clara, CA, (408) 982-2550. Silvar-Lisco, Sunnyvale, CA, (408) 991-6000.

Simulator models large, critical battery arrays

Testing high-capacity dc-power management systems that use large battery arrays is not an easy task. You can, however, substitute batteries with Loral Command and Control Systems' C03050 battery simulator. The system simulates battery power and backup systems such as those used in space vehicles, satellite battery systems, hospitals, and large telephone switching systems.

The simulator eliminates the need for large chemical batteries during test. Testing is easier because batteries don't have to be recharged and tests don't have to be rerun due to failed batteries. The simulator is computer controlled with an optional IEEE-488 link. You can load battery performance/life curves to define simulation for the target batteries. Users can set simulation speed (for rapid charge and discharge cycling), state of charge, and battery voltages. You can also set and simulate battery temperature and pressure.

The simulator has a capacity of up to 200 Ahr, 97A continuous discharge, 15-kW maximum discharge power, 148V dc discharge voltage, and 155V dc charging voltage. The device requires 208V ac, 3-phase at 70A (3-wire and ground). The simulator is available now and costs $199,000. Loral Command and Control Systems, Colorado Springs, CO, (719) 594-1944, contact Robert Golightly.

Video conference will explore virtual reality

On September 30, the IEEE will broadcast a video conference to explore the use of virtual reality and other computer aids as educational tools. "Emerging Technologies: Will Your Company Be Ready?" deals with three main topics: computer aids for product design, computer aids for manufacturing control, and virtual reality for planning, training, and education in the workplace. Dr Leo Young, 1980 president of the IEEE, now with the Office of the Deputy Director for Research and Engineering in the Department of Defense, will lead the video conference. The conference will be broadcast from noon to 3:00 PM EDT. For information on registration and viewing sites, contact Judy Brady, IEEE Marketing Dept, Piscataway, NJ, (908) 562-3991, FAX (908) 981-8062.

Functions enhance DSP library

Although developing DSP applications often involves writing many lines

Software combines neural networks and fuzzy logic

Traditionally, neural networks and fuzzy logic have been treated as two distinctly different technologies. Now National Semiconductor is combining the two technologies for embedded control applications. The company is developing software that uses two steps: using neural networks to define rules and using fuzzy logic to run the rules in real time.

Using the software, neural networks generalize the rules from a set of learned prototypes. The fuzzy-logic system then uses the resultant rules, variables, and variable membership functions to solve a control problem. The fuzzy-logic application takes control inputs and uses the multiple rules to derive a series of control outputs. The fuzzy-logic application runs as an Assembly Language program in a microcontroller. Neural networks are made up of sets of multilevel nodes, each linked to inputs or the previous-level nodes by variably weighted interconnects. The network can learn and store multiple rules, which are produced by an input set of values. The company is using neural networks to learn "correct" rules for fuzzy-logic applications.

The company is developing a neural-network-based, software-development package that generates fuzzy-logic applications. The development software will run on PCs, and the fuzzy-logic applications generated will run on the company's microcontrollers, such as the 4-bit COP4, 8-bit COP8, and the 16-bit HPC/HPC+. The first products are expected in 1993. National Semiconductor, Santa Clara, CA, (408) 721-5000.

---

of assembly-language or C code, you can also use ready-to-run libraries of functions. Star Semiconductor's cell library now includes 140 DSP functions that you can combine with other functions or "cells" to produce stand-alone DSP software. New functions include filters, signal detectors, I/O operations, math operations, and others. For example, new signal-conditioning blocks provide both A-law and μ-law compression and expansion blocks. You'll use the functions with the company's Sproclab development system to produce operating software for the Sproc-1400 DSP chip. However, you can also use the development system to code and test complex DSP algorithms on the Sproclab before moving to other families of DSP chips for your final product. Instead of having you write code and link modules, the Sproclab lets you connect the block diagrams of the various DSP functions, after which it produces code and loads it into a Sproc-1400 chip for testing. The Sproclab development system costs $8950. Star Semiconductor Corp, Warren, NJ, (908) 647-9400, FAX (908) 647-4755.

EE BBS goes on line

Gerald S Harrison's EE Public Domain Library is now available to qualified engineers, for a $45 yearly download fee, from his electronic bulletin board (BBS) at (516) 681-1612. Harrison has been collecting electronic-engineering public-domain programs for 10 years from a variety of sources. The collection fills 32 IBM PC disks. His BBS has free facilities other than the library. Harrison has been distributing the disks for a $10 media fee from his residence at 36 Irene Lane E, Plainview, NY 11803.

Scholarship promotes the future of electronics

Winners of the 1992 IEEE, Region 6 scholarship will be honored at presentation during the Wescon Electronics Show and Convention in Anahiem, CA, November 17 to 19. The winners will be chosen from high-school students from the class of 1993 who attend school in Alaska, Arizona, California, Hawaii, Idaho, Montana, Nevada, New Mexico, Oregon, Utah, and Washington state, and who plan to major in electronics or associated fields at 4-year colleges (in any state). The IEEE, Region 6, will award two scholarships, one for $5000 and one for $3000, for the best essays describing the importance of electronics technology and the future of electronics in the United States. For more information about the scholarship and awards ceremony, contact Natalie Perlin, ECM Marketing Services, Los Angeles, CA, (213) 772-2965.

Port real-time operating system to custom hardware

Developers of real-time embedded systems can now use the Vxworks real-time operating system from Wind River Systems on custom hardware provided the target system uses one of the compatible μP families. The Board Support Package Porting Kit lets you use any hardware that incorporates Motorola 680x0 and 683xx, SPARC, Mips R3000, Intel 80960, Gmicro 100, 200, 300, or the Fujitsu SPARClite family of μPs. The Vxworks base port kit is $995 and a Vxworks development-system license fee is $22,500. Target licenses depend on volume and start at $600 for a single license. Wind River Systems, Alameda, CA, (415) 748-4100.


Maggie White
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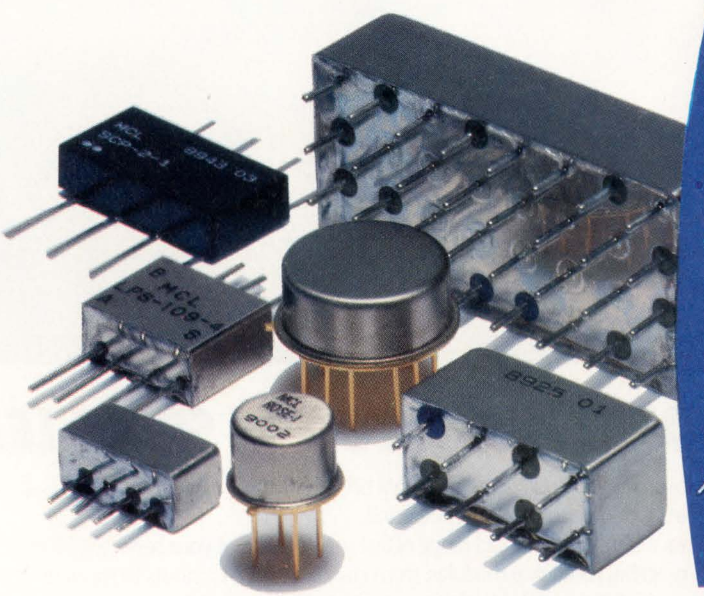

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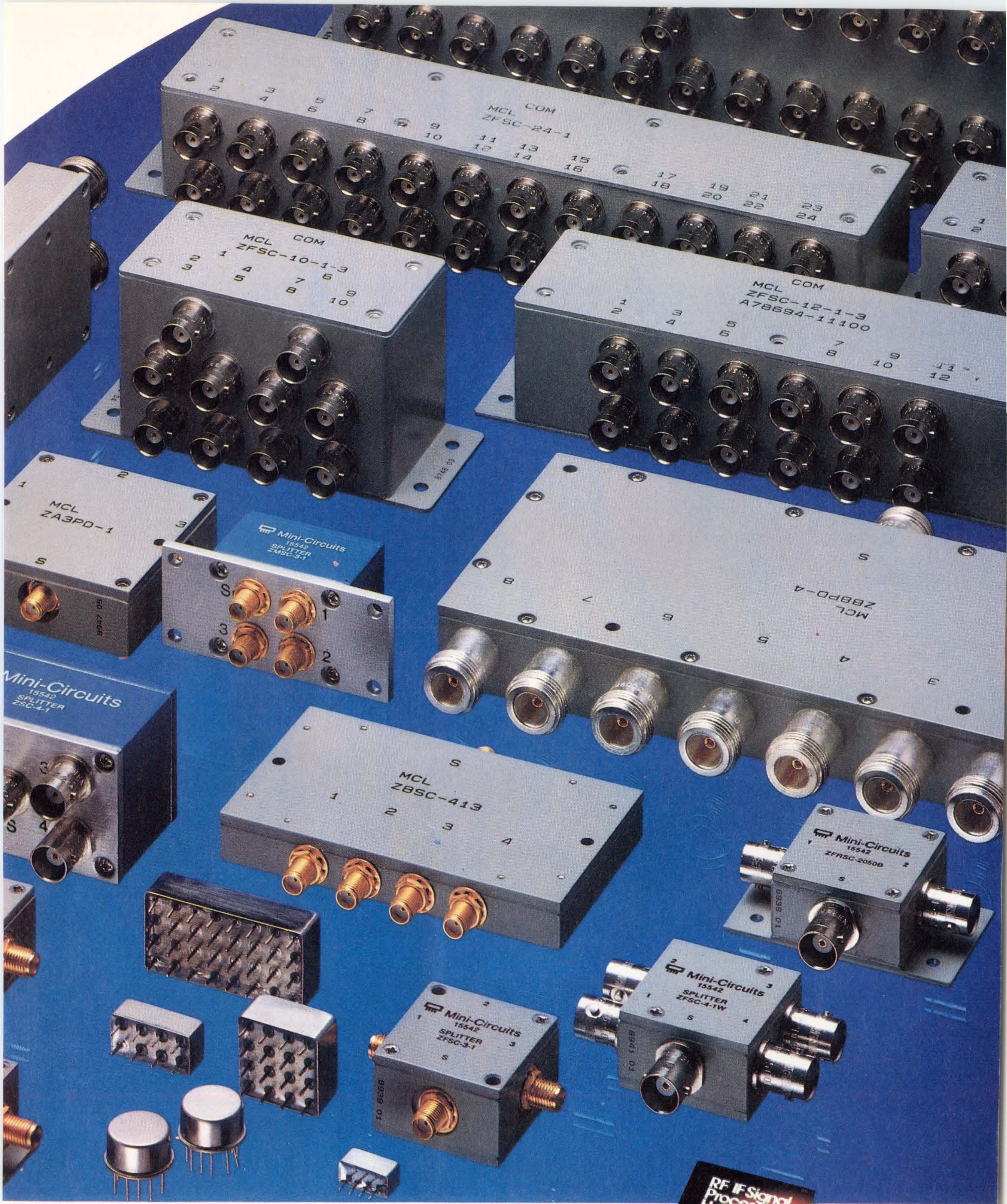
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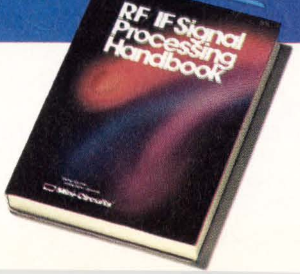
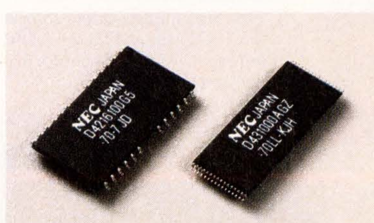

RF IF Signal
Processing
Handbook

NEC offers the industry's broadest line of thin-package memories.

Super-high-density surface mounting is an innovative design strategy that allows you to reduce system size while boosting performance. The new package technology is especially helpful for compact products including notebook PCs, workstations, and IC cards. To help you implement small, lightweight designs, NEC offers the industry's broadest variety of TSOP memories.

DRAM	1M	1M x 1	60/70/80ns
		256K x 4	60/70/80
	4M	4M x 1	60/70/80
		1M x 4	60/70/80
		512K x 8	70/80
		512K x 9	70/80
		256K x 16	70/80
		256K x 18	70/80
	16M	16M x 1	60/70/80
		4M x 4	60/70/80
VRAM	2M	256K x 8	70/80
SRAM	256K	32K x 8	55/70/85/100
	1M	128K x 8	70/85/100
	4M	512K x 8	55/70/85/100
Fast SRAM	1M	64K x 16	15/20
		64K x 18	15/20

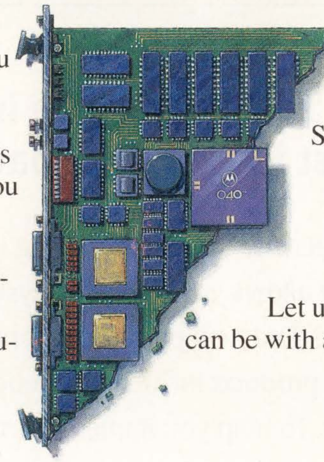
As the leader in memory technology, NEC is committed to meeting your needs for advanced TSOP devices. For more information, contact NEC today.



From the leader in memory technology

NEC

Why Settle for ½ an '040 Board?



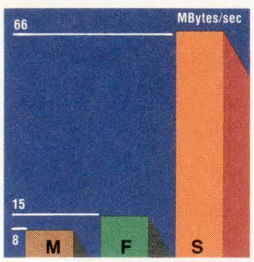
You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

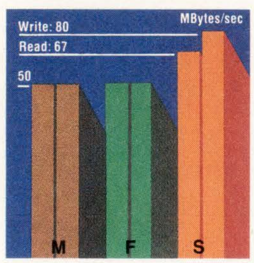
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



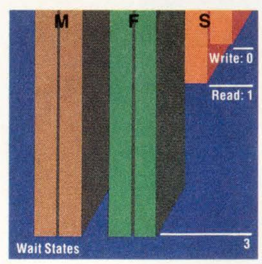
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



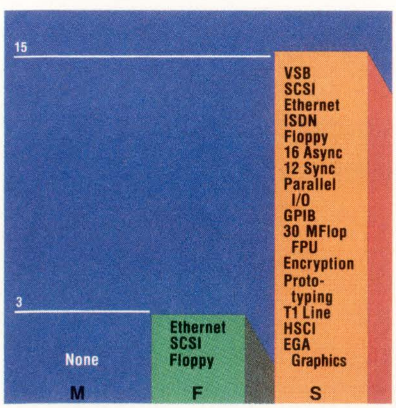
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



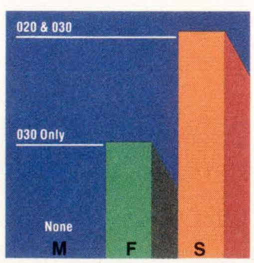
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



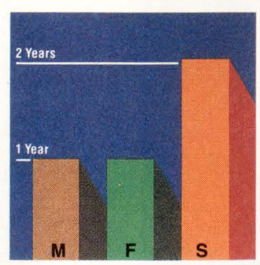
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



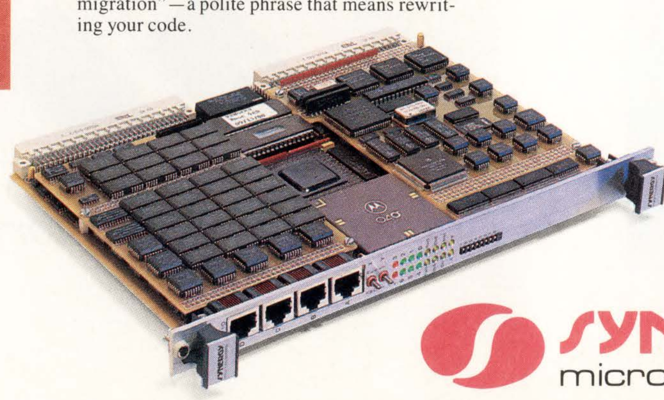
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 **(619) 753-2191** FAX: 619-753-0903

CIRCLE NO. 30

Reader calls attention to patent

In Richard Quinnell's article about 2-Mbit VRAMs (video RAMs) (EDN, March 16, 1992, pg 37), I was particularly interested in the discussion of the use of the "stop-column" feature that allows a tiled organization of memory pages to increase graphics drawing speed.

Metheus Corporation holds US patent 4,546,451 and foreign patents relating to the organization of pages of page-mode memory devices into tiles to allow more effective use of page-mode operation in graphics display memories.

It is unfortunate that this information was not available to Quinnell when he wrote the article. It might be appropriate to call our patent to the attention of your readers so that they can determine if their particular application of the new VRAM technology will require licensing of our technology.

Bob Bruce
Vice President, Technology
Metheus Corp
Beaverton, OR

(Ed Note: The example I gave in the article is related to the Metheus Corp patent.)

How to prevent viruses from entering your software

Charles Small, (in his article, "Shareware and freeware are a phone call away" (EDN, March 2, 1992, pg 49), should be aware that many companies such as mine absolutely forbid (on pain of instant dismissal) importation of any "unauthorized" software for fear of viruses. We're not just lazy or selfish.

Dennis Block, Manager
AT&T
Bedminster, NJ

(Ed note: If Dennis Block is afraid of viruses, he can get a clean copy of a shareware program from the original author or a reputable shareware dealer. Even if he cannot import software past his company's defenses, he can still share software he has developed with others.)

Editorial reinforces back-to-basics viewpoint

Three cheers for the editorial, "Don't blame the kids" (EDN, April 23, 1992, pg 41). Jon Titus is right on target. I can only add that we must also return to the basics, and I mean the very basics—reading, writing, and 'rithmetic—not to mention values; that is, right and wrong. More money can't fix it.

Teachers belong to one of the few professions not being judged on the product they produce. American students' performance continues to decline—and with it the future of this country.

Jim Hargraves
Paramax Systems Corp
Paoli, PA

Address correction

Following is the correct address and phone number for Northern Telecom Inc (EDN, March 2, 1992, pg 62):
Northern Telecom Inc
105 Laurentian Blvd
St Laurent, Quebec H4N 2M3,
Canada
(514) 744-8755
Contact: Demetri Elias.

Omission

In the Special Report on 8- and 16-bit microcontrollers (EDN, June 18, 1992, pg 96), Toshiba America Electronic Components Inc (TAEC) was mentioned in the text and tables, but left out of the Manufacturers' List. The address, phone number, and fax number are
9775 Toledo Way
Irvine, CA 92718
Phone (714) 455-2000
FAX (714) 859-3963

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(actual size)

AMD Introduces The World's First 386 Microprocessor With 3-Volt Technology.

Two standard dry-cell batteries. There's really nothing special about them. Aside from the fact that they can run a powerful, portable 386 computer for a full eight hours. Provided, of course, that portable is built around a low-voltage Am386™ microprocessor.

The 25MHz DXLV and the 25MHz SXLV are available in PQFP packaging.

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For more information on the low-voltage Am386 microprocessors call AMD today at **1-800-222-9323**. You'll never look at dry-cell batteries the same way again.

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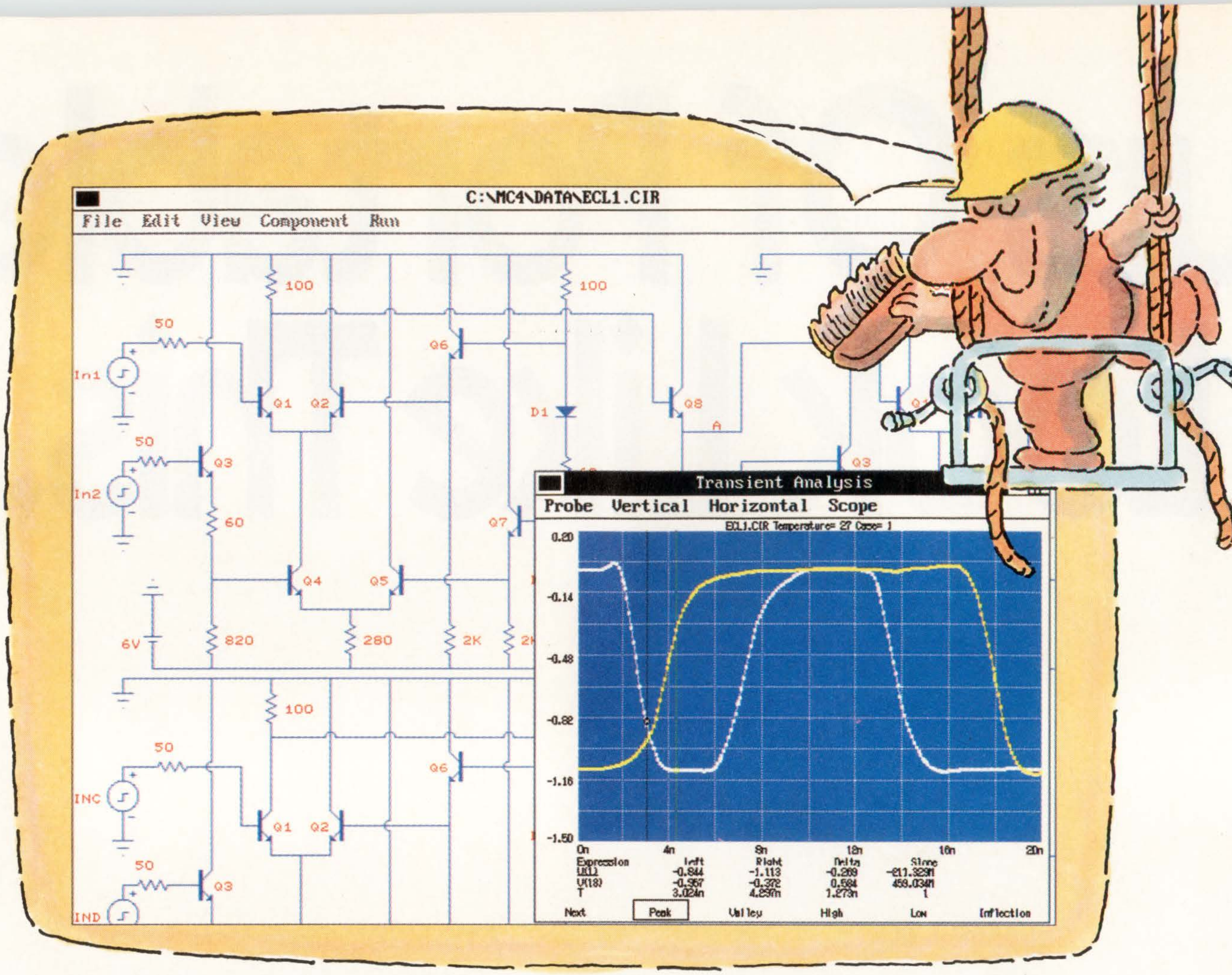
CIRCLE NO. 32



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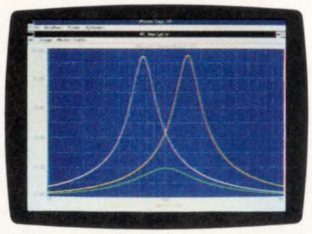

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Now sample MICRO-CAP IV power. It comes, for example, from SPICE 2G.6 models plus extensions. Comprehensive analog behavioral modeling capabilities. A massive model library. Instant feedback plotting from real-time waveform displays. Direct schematic waveform probing. Support for both Super and Extended VGA.

And the best is still less. At $2495, MICRO-CAP outperforms comparable PC-based analog simulators — even those $5000+ packages — with power to spare. Further, it's available for Macintosh as well as for IBM PCs. Write or call for a brochure and demo disk. And experience firsthand added SPICE and higher speed — on larger circuits.

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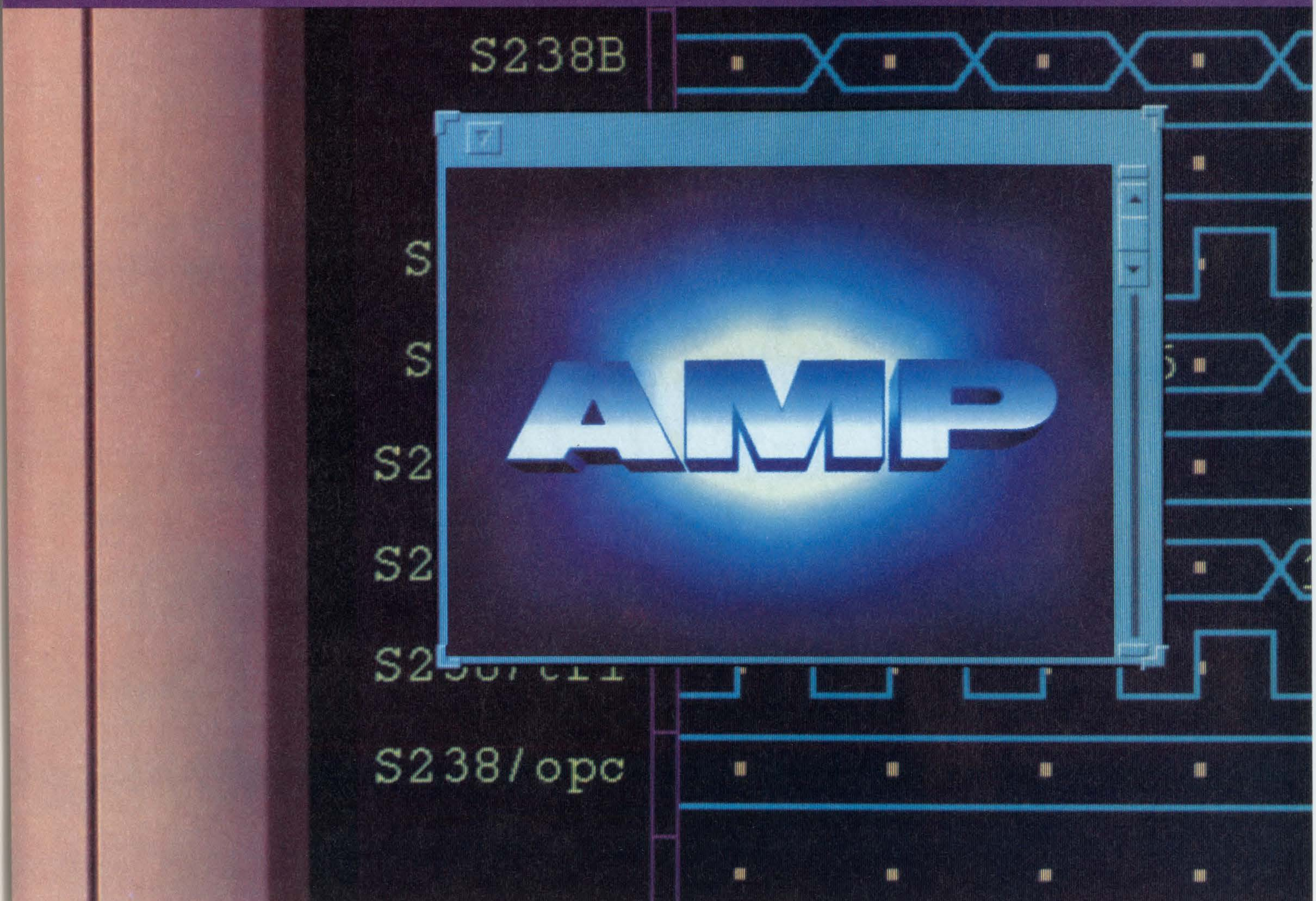
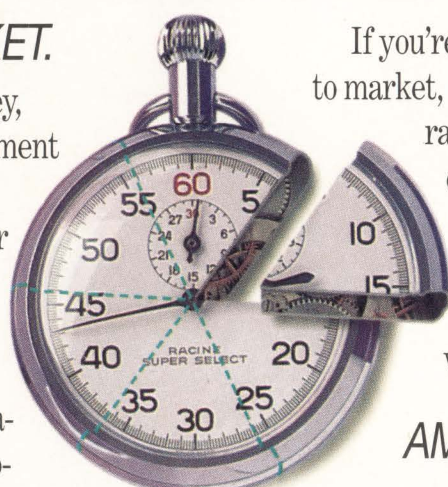
CIRCLE NO. 33

HOW MANY AMPS DOES IT TAKE TO POWER YOUR PRODUCT DEVELOPMENT?

ONLY ONE.



FROM IDEA TO MARKET.



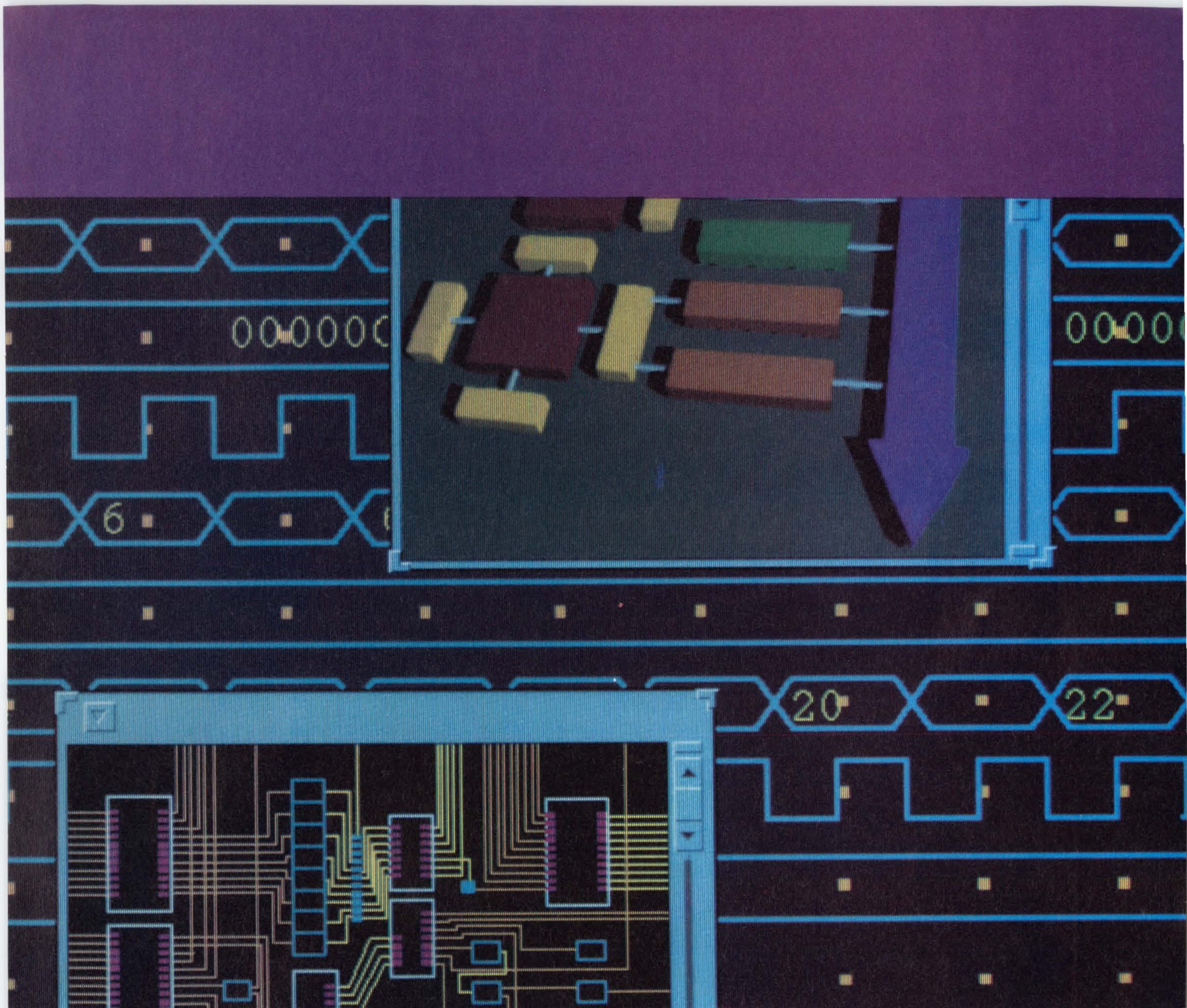
The resources you need for that journey, especially with today's tight development schedules, can tax even the largest companies. AMP can help make your trip to market easier, and faster.

Our capabilities today go far beyond connectors . They include interconnect design, analysis, simulation and validation, systems development, and packaging design. And unequalled production experience in everything from 'metal-and-plastic' to heavy machinery, precision optics to SMT boards to complete plug-and-play systems.

If you're concerned with reducing time to market, dealing with higher clock rates, coping with shrinking envelopes, and generally keeping pace with fast-changing technologies and design methodologies, look into what AMP has to offer, today.

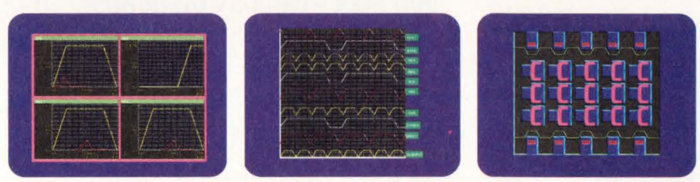
AMP DESIGN SERVICES: EDA TO THE MAX.

One of the toughest jobs you face is analyzing and proving your initial design, and performing board placement and routing. We'll take you from



schematic or logic diagram all the way to a valid software first article.

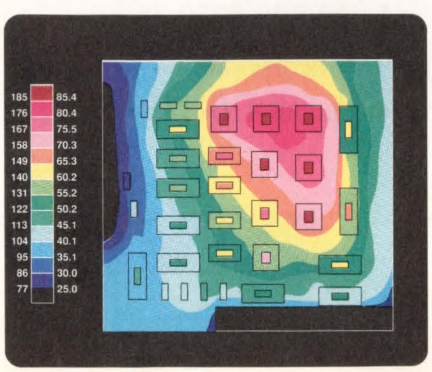
Our comprehensive EDA toolset includes current, state-of-the-art software programs, and our own interconnect and device models–developed specifically for critical aspects of current design such as net simulation, timing verification,



Characterized device and connector models are used in waveform analysis, timing verification, and board design.

analog transient noise effects, system impedance, and transmission line layout rules.

Talk to AMP early in your design cycle, and we'll put you on board faster–with flexible service offerings that range from help with specific problems to complete project management. Tap us for the years of experience we've put into engineering under critical electrical, mechanical, power, thermal,

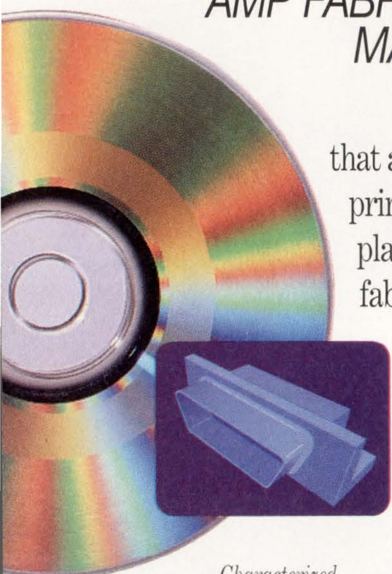


Placement optimization uses thermal analysis, along with electrical, power, and manufacturing considerations.

(Courtesy of BETAsoft, Dynamic Soft Analysis Inc., Pittsburgh, P.A.)

and manufacturing constraints. And shave a lot of time-to-market and development cost off your project.

AMP FABRICATION SERVICES: MAKING IT REAL.



Major elements of your job that add up to major time include printed circuit boards, backplanes, card cage design and fabrication, and systems packaging. Our help here can put you ahead of the crowd and let you spend that time on your real business.

Characterized models speed simulation; 2D and 3D CAD files simplify board layout and package design. (Models available on CD-ROM.)

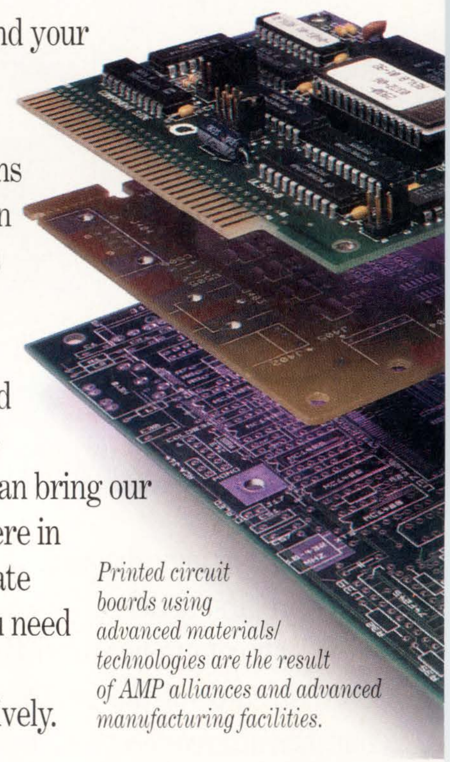
Packaging is a crucial element of systems performance, and our modelling, simulation, power and thermal analyses, and noise budget balancing are crucial for packaging success. When you're ready, our manufacturing experience – from clean room to global shop floor – can pay off at any level you choose: board, subsystem, or finished product.

Look to AMP for the help you need to meet tight production schedules and narrow market windows, and the resources you want to move into next-generation technologies. Our knowledge base in fast boards, high-speed cable assemblies, surface mount technology, and related subjects can simplify the transition to faster logic and smaller form factors.

Complete system architectures include packaging systems, power supplies, and I/O. Developed and manufactured to your requirements.

Custom high-performance cable assemblies represent value-added capabilities in advanced design technologies.

THE BIG PICTURE: FROM CONCEPT TO PRODUCTION.



Your program, and your problems, are unique. Your program is yours alone, but your problems don't have to be. We can help in any of the areas we've listed here.

Or let us put it all together for you, and move you from start to finish. Our specialists can bring our services to you anywhere in the world, and coordinate the AMP resources you need to bring your idea into production. Cost-effectively. And on time.

Printed circuit boards using advanced materials/ technologies are the result of AMP alliances and advanced manufacturing facilities.

For more information, call our Product Information Center at 1-800-522-6752 (fax 717-986-7575). AMP Incorporated, Harrisburg, PA 17105-3608. In Canada call 416-475-6222.

THIS IS AMP TODAY.

AMP

CIRCLE NO. 34

Vote for Innovation

The time has come to vote in EDN's Third Annual Innovation and Innovator competition. You'll find a complete list of the finalists and a ballot in the special Innovation Supplement that accompanies this regular issue of EDN. The finalists our editors have chosen represent the most innovative products and people among the applications submitted to us for judging. To us, a product is innovative when

- It offers significantly higher levels of performance than were previously possible.
- It solves a continuing problem much more effectively than its predecessors.
- It exhibits a marked degree of "cleverness" that differentiates it from earlier products.
- It embodies new technology that advances the state of the art or uses older technology in a unique and innovative manner.

Such products might not have an immediate, widespread, or obvious use. Some innovative products take time to catch on and fire the imagination of designers.

Our editors also look for innovative people and design teams. They seek people who did innovative work during the past year and people who work in innovative ways. Perhaps a group of workers broke through management barriers to increase their efficiency and creativity. Or, an engineer could have made a significant breakthrough in designing a product or part of a product.

Now that you know what we look for, take a few minutes to read our Innovation Supplement and vote for your choices. We'll announce the winners at Wescon '92 in Anaheim, CA. You'll also hear about the winners in EDN's magazine and news editions.

As you review the finalists, you may be disappointed that none of your company's products or people are among them. Even though a great deal of work goes into each application, we can select only a few finalists in each category. On the other hand, your company may have never entered this year's competition. If you want to be sure to receive a nomination packet for the 1993 Innovation and Innovator awards, drop me a note and I'll make sure we send you one. If you know someone else in your company who should get the information, let me know and I'll make sure we send it to them, too. Our awards program is international, and we seek and receive entries from companies worldwide.

For information on the 1993 awards program, circle number 801 on the Information Retrieval Service form in this issue, reach me via fax, or send your request to EDN Innovation Awards, EDN Magazine, 275 Washington St, Newton, MA 02158 USA.

Jon Titus
Editor

Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

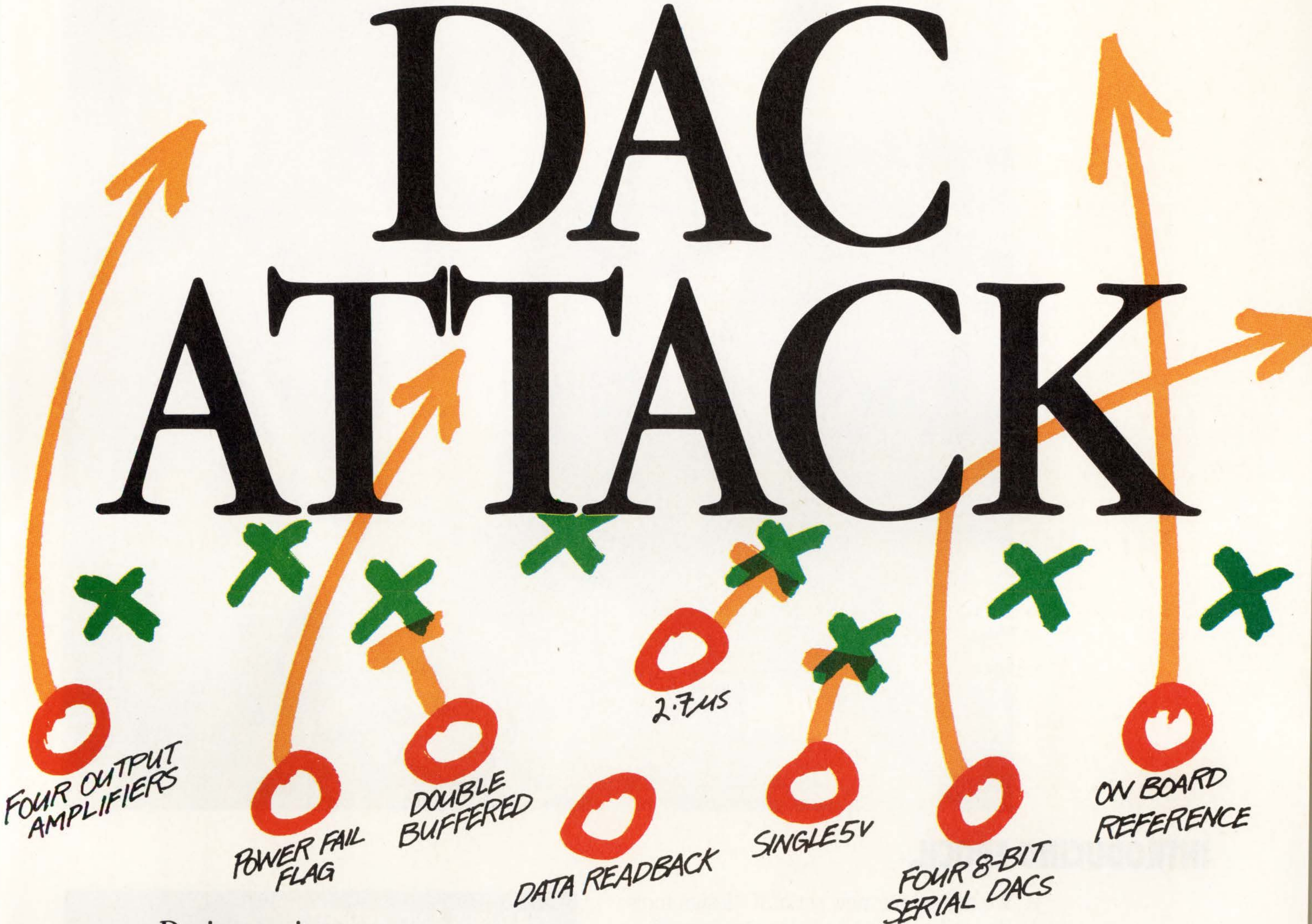
American Society of
Business Press Editors Award
1988, 1983, 1981

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8,N,1; on 9600-bps modems, try (617) 558-4580, 4582, or 4398.

CIRCLE NO. 35

National Semiconductor

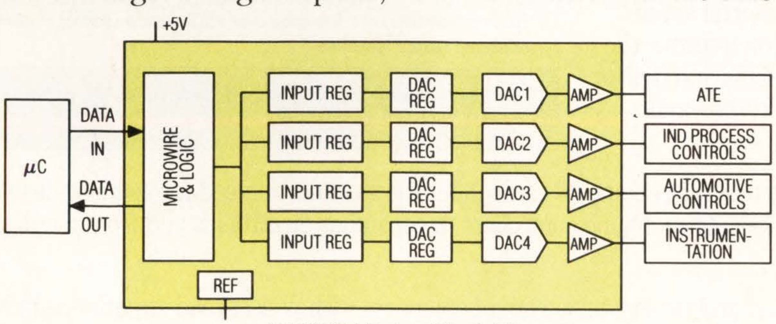
DAC ATTACK



Design a winner with our new quad 8-bit serial DAC.

With National's DAC0854, you'll tackle your next design with the advantages of higher speed, higher integration and on-chip diagnostic capabilities.

That's the lineup that puts excess wiring, wasted board space, and rising test costs on the defensive. With the DAC0854, more efficient designs are part of every game plan.



DAC0854 System Block Diagram

Play to win.

To get that competitive edge, call us for a free sample at 1-800-NAT-SEMI, ext. DAC. Or, fax: 1-800-888-5113.

National Semiconductor

NORTH AMERICA: P.O. Box 7643, Mt. Prospect, IL 60056-7643 (Tel: 1 800 628 7364, ext. DAC; Fax: 1 800 888 5113); **EUROPE**: Industriestraße 10, D-8080 Fürstenfeldbruck, Germany (Tel: 49 8141 103 0; Fax: 49 8141 103 515); **HONG KONG**: 15th Floor, Straight Block, Ocean Center, 5 Canton Rd., Tsimshatsui, Hong Kong (Tel: 852 737 1654; Fax: 852 736 9921); **JAPAN**: Sanseido Building 5F, 4-15-3, Nishi-shinjuku, Shinjuku-ku, Tokyo, Japan 160 (Tel: 81 3 3299 7001; Fax: 81 3 3299 7000).

EDN

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

INNOVATION™

VOTE FOR INNOVATION WINNERS

VOTE FOR INNOVATION, WIN A CALCULATOR

This year, you can vote for EDN's Innovator and Innovations of the Year awards and enter a chance to win a Hewlett-Packard 48S scientific calculator at the same time. You can see a photo of the calculator on the ballot.

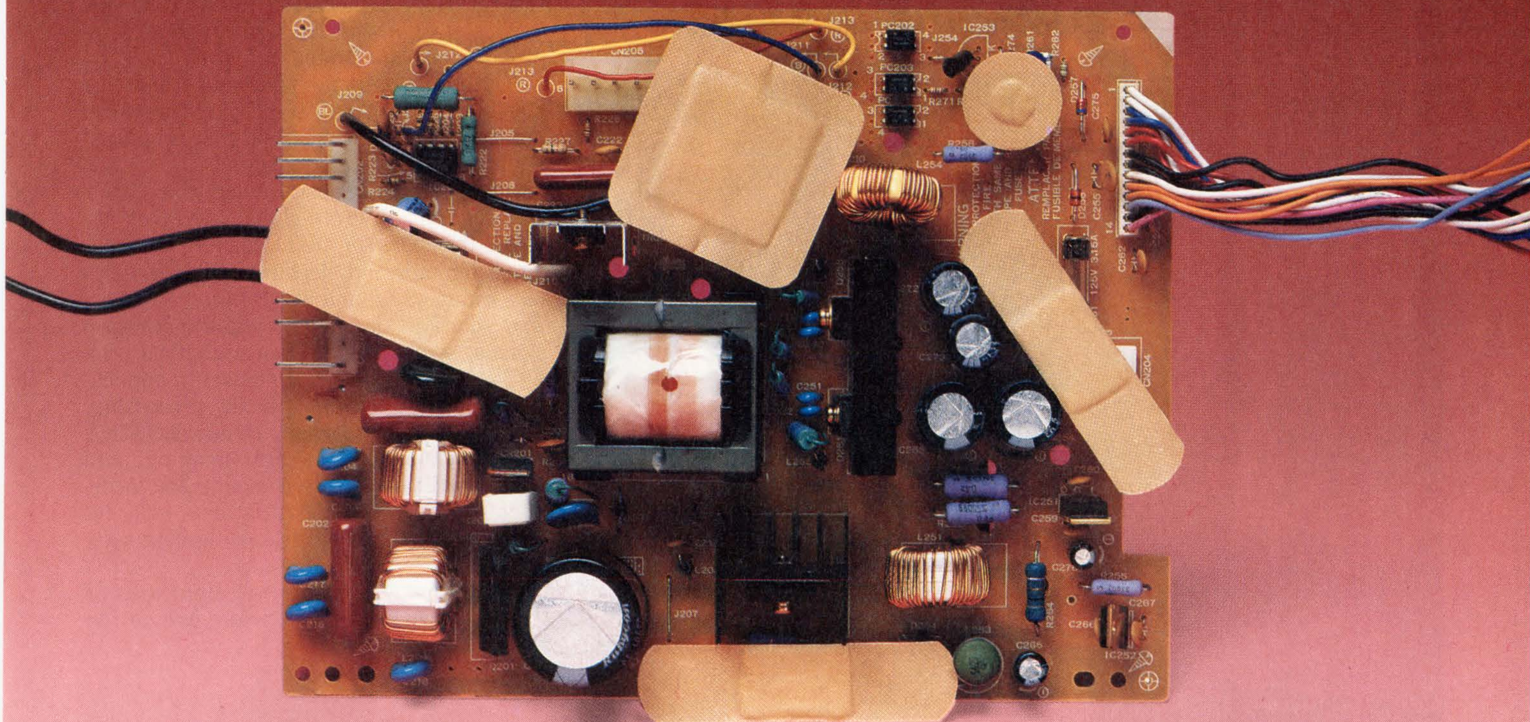
On the following pages, you'll find brief descriptions of the finalists in various award-program categories. EDN's editors selected these finalists from nearly 100 nominations in the 1992 Innovation and Innovator of the Year awards competition.

Carefully consider these finalists and mark your votes on the postage-paid ballot that appears at the end of this special-awards supplement. This year, EDN has one new category—μPs—in addition to the categories of previous years: ICs and semiconductors; test and measurement; CAE/CAD; computers and peripherals; components, hardware, and interconnect; software; power sources; and the Innovator of the Year. Please mark one vote in each category and mail the ballot before September 10.

After an independent accounting firm tallies the votes, EDN will announce the winners at a black-tie awards banquet to be held this November at Wescon/92 in Anaheim, CA. We'll also print a special section in our November 26 issue naming the winners.

Five ballots will also be drawn at random; the people who sent in these ballots will win the HP 48S scientific calculator. These innovative calculators pack 2100 functions, a graphics display with plotting capabilities, a serial port for communications with PCs, and an infrared printer link. They go beyond mere number crunching by performing symbolic math and dimensional analysis. So go ahead, vote for innovation!

No Band-Aids.® 500kHz Switcher.



Fast, Clean, Thrifty.

The LT1241 family of pulse width modulators from Linear Technology enable 500kHz operation of off-line switching regulators–with only 50ns of current sense propagation delay. The LT1241/2/3/4/5 are pin-compatible with 3842 type parts and contain all the circuitry necessary for off-line switchers: temperature compensated reference, high gain error amplifier, fast current sensing comparator with blanking, and high current totem pole output stage.

Each of these parts has improved speed and lower quiescent current (8mA typical) than 3842 type devices. Start up current has been reduced to 170μA typical. Cross conduction current spikes in the totem pole output stage have been eliminated–making 500kHz operation practical. To make the LT1241 family easier to use, we've added true blanking to the current sense comparator which virtually eliminates the filter and allows the current sense loop to operate with minimum delays.

The LT1241 family eliminates "Band-Aids" in power supply design. Parts are available in 8-pin SO packages or 8-pin DIP. Pricing in 1000-up quantities starts at $1.96. For details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035/408-432-1900. For literature only call **800-637-5545**.

LT1241 FEATURES

- **50ns I Sense Delay**
- **No Shoot-Thru**
- **500kHz Operation**
- **Wide Controllable Pulse Width at 100kHz**
- **Low Start Up Current**
- **Built-in Blanking**
- **Low Power**
- **High Speed 3823 Equivalent**
- **Pin Compatible 3842 Equivalent**
- **8-Pin SO Pkg**
- **Cheap**

LINEAR TECHNOLOGY

TOUGH PRODUCTS
FOR TOUGH APPLICATIONS.

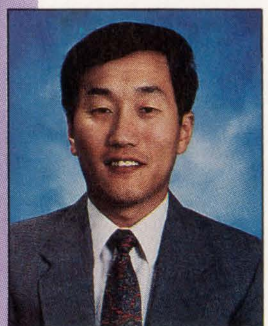
ISO 9000
COMPLIANT

Band-Aid is a registered trademark of Johnson & Johnson Co.

CIRCLE NO. 38

Dr Dapang Chen and Shie Qian

Although spectrograms (joint time-frequency analyses or JTFAs) have existed for many years, the conventional method of calculating them, using the short-



time Fourier transform (STFT), suffers from a number of problems. DSP Software Manager Dr Dapang Chen (left) and DSP Engineer Shie Qian developed a new spectrogram technique using the Gabor transform. The new technique runs faster and thus allows real-time spectrogram analysis in more situations.

STFTs are slow, so you cannot use them for most real-time applications. The Gabor spectrogram computes six times faster than the STFT. Furthermore, STFT analysis applies a window to the signal, and no compromise window shape can produce good resolution in both the time and frequency domains. In contrast, the Gabor transform employs a Gaussian function that is optimal for both time and frequency.

Chen and Qian also solved the Gabor transform for discrete signals (the discrete Gabor transform or DGT), making the technique far more applicable to digitized signals commonly found in μP-based systems. The solution also covers infinite-duration signals, so the DGT is more practical than FFTs for analyzing real signals in applications such as speech and image processing, synthesized music, sonar, radar, acoustics, vibration analysis, medical imaging, and power monitoring. The company has incorporated the Gabor transform into its Labview graphical programming language.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

National Instruments
Austin, TX
(512) 794-0100

Analog Devices' ADXL50 Design Team

The Analog Devices ADXL50 design team took a new and unproven manufacturing process called surface micromachining and combined it with mixed-signal electronics to create a low-cost, monolithic silicon acceleration sensor. The team that accomplished this feat includes design, process, and production staff members.

The company decided to bring surface micromachining from the university lab onto the production floor because the technology promised the ability to combine sculpted silicon microstructures with active circuitry. The champion who guided the project to completion was company veteran Dr Richard Payne (center if photo), director of the company's Automotive and Sensor Products Group. Payne is an IEEE fellow.

The team's lead circuit designer, Steve Sherman (left), designed several analog products for the company before attacking the acceleration sensor. He designed the AD645 FET-input, low-noise op amp; the AD526 programmable-gain op amp with a μP interface; and the AD538 simultaneous analog multiplier, divider, and exponentiator. His sensor-circuit design for the ADXL50 can resolve capacitance changes of a mere 30 aF ($30 \times 10_{18}$ F). Robert Tsang, an Analog Devices Fellow, developed the fabrication process that combines surface micromachined features and BiCMOS circuitry.

The ADXL50 sensor measures accelerations to ±50g with 8% accuracy over a temperature range of −55 to +125°C. It has a programmable output bandwidth ranging from dc to 1 kHz and operates on power-supply voltages of 5 to 24V. The device costs $5 in automotive OEM quantities.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

Analog Devices Inc
Norwood, MA
(617) 461-3557

SIGNAL PROCESSING. GRIZZLY?

Designing a signal processing system can be a bear of a problem—immense, mean, and unforgiving. Engineers grappling with conventional analog or digital technologies face risk and unpredictability at every turn, with no guarantee of success. Designers invest months of development time in a brutal design process that's as lengthy as it is frustrating. Productivity and time to market are devoured in the struggle!

SPROC Technology Tames The Task

At the core of STAR Semiconductor's unique signal processing solution is the SPROC™ chip, the first-ever programmable signal processor using the "Sketch and Realize"™ design approach. With a single SPROC chip and a SPROClab development system, signal processing becomes a tame task.

Why wrestle with circuit breadboards crawling with sensitive analog components? Or agonize over line after line of assembly code? One SPROC chip integrates the functionality of hundreds of analog and passive components to cut system costs. And SPROClab employs system-level graphical programming so you can capture designs as signal flow block diagrams. You gain all the benefits of a digital solution—***without writing software!***

Stop laboring with trial-and-error debug methods, cumbersome logic analyzers, or software simulators to debug a design! Engineers using SPROC technology download designs ***directly*** onto actual silicon and interactively debug systems as they execute in ***real time!*** Using the SPROC chip's unique built-in probe feature, you can easily modify design specifications to tune system performance during execution.

With SPROC technology, engineers focus on designing to create better products in less time.

If you can't bear to see your productivity mauled by the problems of signal processing design, call STAR Semiconductor at **908/647-9400.** We'll send you a brochure and demo disk telling how to tame your next signal processing project.

STAR Semiconductor Corporation
25 Independence Boulevard, Warren, NJ 07059
Telephone: (908) 647-9400 FAX: (908) 647-4755

SPROC Users Slash Development Time

APPLICATION	PREVIOUS TECHNOLOGY	PREVIOUS DEV. CYCLE	SPROC DEV. CYCLE	$ SAVINGS (1st YEAR)
Secure FSK modem	analog	6 months	**3 weeks**	**$50,000†**
Adaptive noise canceler	DSP	6 months	**1 week**	**$57,500***
Power supply controller	analog	6 months	**1 day**	**$60,000***
Closed-loop vibration controller	analog	3 months	**2 weeks**	**$240,000†**

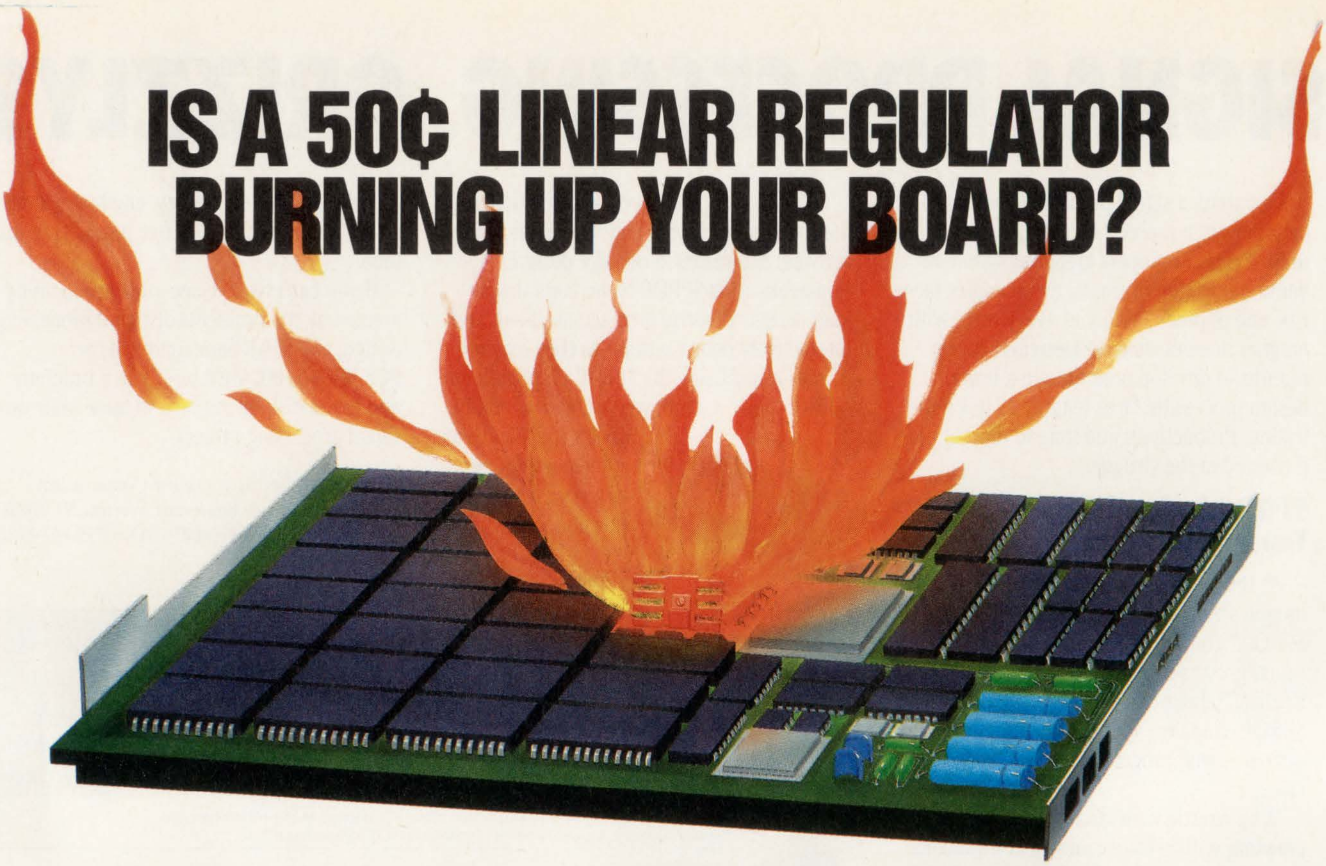
†Total system savings including project overhead, engineering resource, and system hardware costs.
*Estimated savings in engineering resource based on cost of $10,000 per man month.

STAR SEMICONDUCTOR

The Signal Processing Company

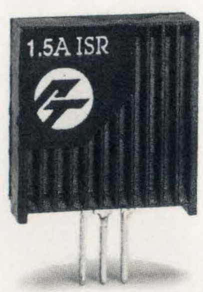
CIRCLE NO. 39

IS A 50¢ LINEAR REGULATOR BURNING UP YOUR BOARD?



PLAY IT COOL WITH OUR 1.5 AMP INTEGRATED SWITCHING REGULATOR

Do you have a board with a 3-terminal linear regulator that's generating more heat than an irate customer? Are you locked into a tight compact design that leaves no extra space for a larger heatsink? Fortunately, you can now play it cool with an innovative product from Power Trends—a 1.5 Amp Integrated Switching Regulator (ISR) that needs no heatsink.



Power Trends' 1.5 Amp ISR is pin-compatible with existing 3-terminal "78 and 79 Series" linear regulators, fits into the same space, and is just as easy to use. With 85% efficiency, our ISR provides a cool replacement alternative for a hot linear regulator. Of course it costs more, but it could save you thousands.

Specifications include: laser-trimmed output voltages from 3.3 to 15 volts, calculated MTBF of over 1,000,000 hours, 0.2% line and 0.4% load regulation, and power densities of 25 to 100 watts per cubic inch.

So if you have a heat/space/reliability problem now, or just want to make sure you don't have one in the future—check out Power Trends' super-efficient ISR. Call or write for more information, and ask about samples.

POWER TRENDS

Power Trends, Inc. 1101 North Raddant Road, Batavia, IL 60510 • (708) 406-0900 • FAX (708) 406-0901

CIRCLE NO. 40

Dr Terry J Scheffer and Benjamin Clifton

While other companies are spending millions of dollars to develop fast, high-contrast LCDs using active-matrix circuitry, Principal Scientist Terry J Scheffer (right) and Senior Design Engineer Benjamin Clifton created a technique, which they call active addressing, that produces the desired results using far less costly passive LCDs. They discovered that by changing the way the LCD panel excites the liquid-crystal material, they could achieve video display speeds and contrast ratios of 40:1 using easily manufactured, inexpensive LCD panels.

The key to this development was recognizing that the apparent incompatibility between fast response and high contrast in conventional passive LCDs could be overcome through unconventional driving techniques. Conventional passive LCDs drive one pixel row at a time. Consequently, fast-response, low-viscosity liquid-crystal material can relax during the relatively long periods between voltage pulses. This relaxation results in low contrast. Active addressing increases the row-excitation rate from the usual 16 Hz to several kHz by exciting several rows simultaneously. Consequently, the low-viscosity liquid-crystal material never has time to relax, and contrast ratios stay high.

The active-addressing technique employs a mathematical algorithm to calculate appropriate row-excitation sequences and voltages. This technique can excite as many as half of the LCD's rows simultaneously. The active-addressing control circuitry calculates the appropriate drive voltages. Active addressing increases the complexity of LCD-driver ICs, but it eliminates the complex manufacturing process required for fabricating active-matrix panels. Although not yet in production, prototype active-addressing LCDs achieve 50-msec response times with 40:1 contrast ratios.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

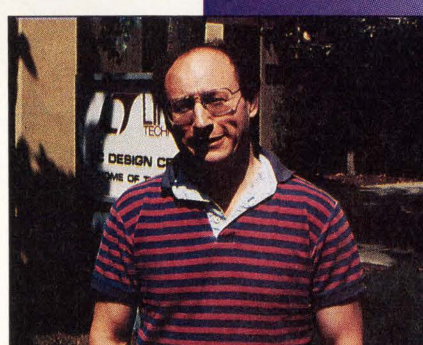
In Focus Systems Inc
Tualatin, OR
(503) 692-4968

Jim Williams

Jim Williams' forte is explaining and popularizing the application of linear-IC technology; the vehicles for his work are application notes, books, and contributed articles in trade journals, including EDN. A recent example is the "Jim Williams papers" on high-speed amplifier techniques. Jim is a staff scientist at Linear Technology. Last year, Linear Tech published a more comprehensive version of the high-speed amplifier series as a 132-page application note.

You might not think that explaining and popularizing a technology involves innovation, but Bob Dobkin, Linear Tech's vice president of engineering, convincingly argues otherwise. In nominating Williams, Dobkin writes, "The innovation in this process lies in identifying problems a customer will face and then finding and sharing the solutions." Without Jim's advocacy to the design community—and that of a dedicated cadre of applications professionals throughout the industry—many promising technologies would languish as laboratory curiosities.

Jim championed the notion that, to be successful, a manufacturer must offer its customers the solutions it has discovered to the problems the customers will face in using the manufacturer's products. Williams says that customers confront three classes of problems: cost constraints, technical difficulties, and design freedoms. When vendors offer advice, they must keep that context always in mind. To solve problems, Jim says, "you have to stick yourself in your customer's shoes."



Linear Technology Corp
Milpitas, CA
Phone (408) 432-1900

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

INNOVATORS

Jeff Robinson

Frustration forced Jeff Robinson to break the Von Neumann bottleneck for DSP μPs. For years he watched as engineers attacked signal-processing problems using imprecise analog circuits and DSP systems that were forever too slow. In October 1991, 15 months after he acquired the first round of venture capital to start his company, Robinson and his development team produced the Sproc-1000 DSP μP and the Sproclab Development System.

At the Sproc-1000's core is a central memory architecture that accommodates as many as four processors on one IC. Each processor operates from the same software on the same data in round-robin fashion. The net effect is to multiply the basic processor's speed by the number of processors on the chip. Therefore, you can write a DSP program and then buy the appropriate number of processors to produce the desired throughput.

The Sproclab Development System allows you to create DSP programs by drawing block diagrams, a method Robinson calls "sketch and realize." The resulting programs separate the signal-processing tasks, which they assign to the Sproc-1000 μP, from the logical operations, which they assign to a companion μP. Thus, the Sproc-1000 and the Sproclab Development System take significant steps toward easing design engineers' frustrations by putting easily scalable processing horsepower and simple DSP programming within their grasp.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

Star Semiconductor Corp
Warren, NJ
(908) 647-9400

INTEGRATED CIRCUITS AND SEMICONDUCTORS

ispLSI 1032 PLD

The ispLSI 1032 is a programmable logic device (PLD) that features in-system programming. The reprogrammable device has 6000 gates and uses the company's 0.8μm E^2CMOS process. Because you can program these devices using TTL-compatible logic, you can reconfigure the PLDs without removing the devices from the circuit board. A 5-wire interface provides "on-the-fly" programming.

The chip contains 192 registers, 64 universal I/O cells, 8 dedicated input ports, 4 dedicated clock-input ports, and a global routing pool (GRP). The GRP interconnects all of the elements in the PLD. The basic logic unit in the device is the generic logic block (GLB). There are 32 GLBs, each with 18 inputs and 4 outputs.

The four internal sections of the GLB consist of an AND array, product-term sharing array, reconfigurable registers, and control functions. The AND array consists of 20 product terms, which can produce the logical sum of any of the GLB inputs. You can configure the outputs as combinatorial or registered. All outputs feed into the GRP for connection to the inputs of any GLB on the device.

The device's 64 universal I/O cells connect directly to an I/O pin. You can program each cell to be a combinatorial, registered, or latched input. You can also program the cells to be outputs or bidirectional I/O ports having 3-state interfaces. All I/O signal levels are TTL-compatible. The PLD operates as fast as 80 MHz and has a propagation delay (t_{pd}) of 15 nsec.

The chip runs on the company's pDS development system software. The pDS software runs on a DOS-compatible 386 or 486 computer running Microsoft Windows. You can implement multiple hardware configurations on the same board and upgrade the board in the field via a modem link. An isp engineering kit lets you debug programs using a DOS-compatible computer. A chip in an 84-pin plastic leaded chip carrier costs \$121.25 (100), the pDS software costs \$995, and the isp engineering kit costs \$395.

To vote for this entry as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

Lattice Semiconductor Corp
Hillsboro, OR
(503) 681-0118

The High Performance of Two Chips from the Lowest Cost Product!

You can't beat Harris Semiconductor's HI5812 for price/performance. It's the lowest cost, 12-bit sampling analog-to-digital converter available today. And with significantly lower power consumption than the competition, it's even more cost effective.

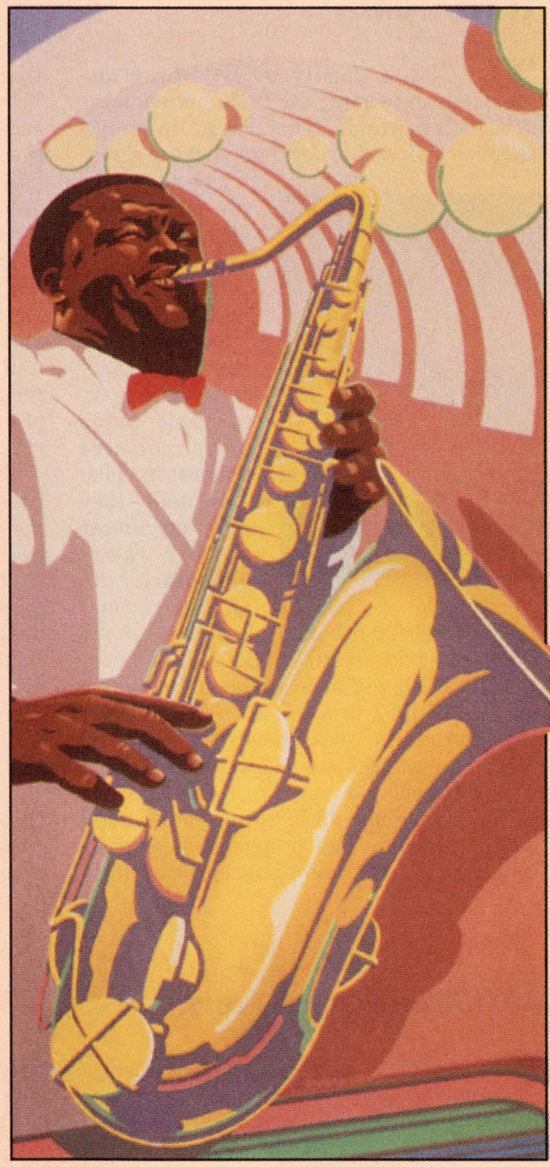
The HI5812 is ideal for numerous applications having input frequencies of up to 30 KHz. It's fast. The throughput rate is 60 kilosamples-per-second. Conversion time is as low as 15 microseconds with a single 5 volt supply.

With track and hold built in, it's the equivalent of two chips needed for other manufacturers' solutions. And you can rely on the HI5812 to meet your design requirements. No missing codes over the full industrial temperature range. User-selectable outputs feature full, high-speed CMOS, three-state bus driver capability. It typically draws just 1.9 mA.

HI5812 12-Bit Sampling A/D Converter

HI5812JIP	24-Lead PDIP	(N)
HI5812KIP	24-Lead PDIP	(N)
HI5812JIJ	24-Lead CERDIP	(N)
HI5812KIJ	24-Lead CERDIP	(N)
HI5812JIB	24-Lead SOIC	(W)
HI5812KIB	24-Lead SOIC	(W)

N = Narrow W = Wide



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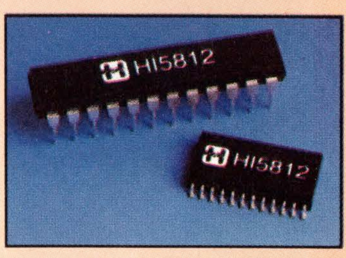

REACH THE HIGHS AND LOWS

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HARRIS
SEMICONDUCTOR

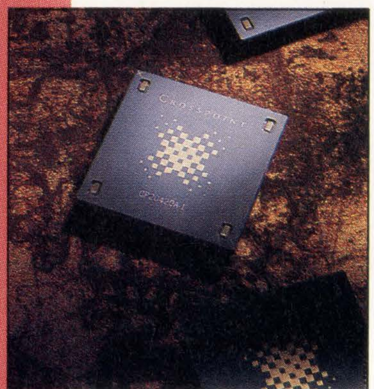
CIRCLE NO. 41

INNOVATION

INTEGRATED CIRCUITS AND SEMICONDUCTORS

CP20K FPGAs

The CP20K family of field-programmable gate arrays (FPGAs) provide the best of two worlds. The arrays' design resembles a mask-programmed gate array, which allows the use of industry-standard ASIC design tools, yet is field programmable. FPGAs have a gate-array-like structure with rows of basic gates and register transistor cells. Essentially they offer an almost sea-of-gates granularity in an FPGA form.



The CP20420 has 4.2k gates in a 155-pin PGA (pin-grid array). A 12k-gate version, the CP21200, will be available in the fourth quarter of 1992 in a 223-pin PGA. The arrays can attain clock speeds as fast as 40 MHz for a counter and 52 MHz for a flip-flop with a fanout of 3.

The arrays use an 0.8-μm, 2-level metal CMOS process. The programmable interconnection is a metal-to-polysilicon antifuse that fits into a via between the two levels. The antifuse has an off-resistance of 1 GΩ and an on-resistance of 100Ω. Each connection has a capacitance of 0.65 fF per antifuse. Each chip also has five power and ground planes that have four decoupling capacitors.

The arrays also feature RAM logic tiles (RLTs) to implement RAM and sequential logic. The mixture of gates and RLTs provides a dual-granularity structure. In addition, the chips have a JTAG interface for program and test. Variable output drives of 4, 8, and 12 mA are similar to gate arrays.

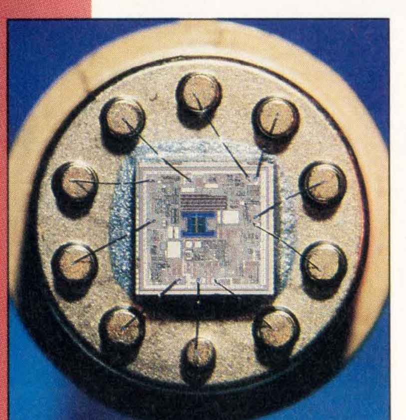
Taking advantage of the similarity between the FPGA and standard gate arrays, the company integrated the array libraries and tools with the workstation CAE tools from Mentor Graphics, Viewlogic, Synopsys, and Cadence. Therefore, gate-array designers can use the FPGA without changing design tools. The CP20420 costs $203.96 (1000); design kits for Mentor 8.0, Synopsys, Viewlogic, and Cadence workstations cost $3950 to $4950 per license.

To vote for this entry as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

Crosspoint Solutions Inc
Santa Clara, CA
(408) 988-1584

ADXL50 Acceleration Sensor

The ADXL50 acceleration sensor combines a surface-micromachined capacitive sensor with on-chip signal-conditioning and self-test circuitry. The sensor can gauge collisions, judge inertial positioning, and monitor active systems. Its primary application is automotive air-bag systems.



Surface micromachining is a process for making silicon structures that can move. Multiple thin films—as well as layers of silicon and silicon oxide—are deposited and etched to produce movable parts with dimensions of 1 to 2 μm. This process lets electronic circuitry and micromachined structures reside on the same chip.

The ADXL50 measures acceleration in a single plane of sensitivity over the ±50g range to an accuracy of 5%. Unlike accelerometers that monitor the resistance changes of stressed piezoresistors to detect acceleration, the ADXL50 measures changes in capacitance and is therefore insensitive to temperature changes.

The signal-conditioning circuitry provides excitation signals for the sensor and amplifies the analog output signal. The ADXL50 comes in a 10-lead TO-100 can and costs $23 (100). The sensor is also available in other package styles, and it costs $5 in automotive OEM quantities.

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

Analog Devices Inc
Automotive and Sensor Products Group
Norwood, MA
(617) 461-3557

The Flexibility of NV RAM With the Security of ROM in One Chip

You'd hate for your system to forget critical data, like programs and setup information. On the other hand, it's very appealing to be able to read and write data quickly. The DS1645 Partitionable Nonvolatile SRAM gives you the best of both worlds with sixteen separate blocks of memory that can each be configured with the characteristics of either ROM or RAM. And you can change those designations at any time — RAM to ROM or vice versa.

Save Space and $$

With program *and* data memory stored in one chip, a single DS1645 can take the place of multiple existing memories, including ROM, EEPROM, FLASH, and SRAM. In a world where printed circuit board real estate does not come cheap, you can save precious space.

Add, Change, or Eliminate Write Protection

Through easy-to-produce software — 24 read cycles to be exact — you can write-protect any or all blocks of memory. And you can alter that write protection at any time through this software. No additional hardware is needed.

Data Stays When Power Goes

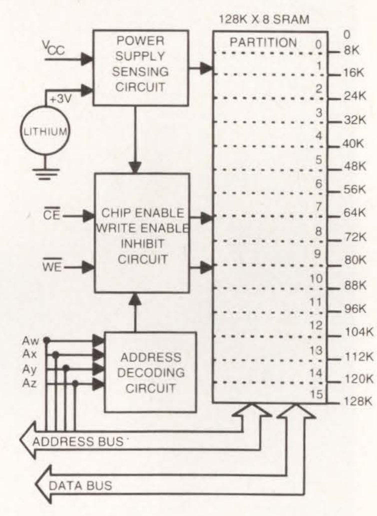
Dallas Semiconductor has been refining the technology of lithium-backed memories for eight years. Like its other nonvolatile RAMs, the DS1645 safeguards data when the power goes out of specification and retains information for over 10 years in the absence of external power.

Prevent Data Corruption

The DS1645 takes a further step towards preventing data corruption by looking beyond voltages, at irregularities in the microprocessor's operation. In sections defined as ROM, a highly structured sequence of operations — one that would never occur normally — is required to overwrite the memory. Through this mechanism, the DS1645 ensures that an out-of-control microprocessor does not destroy data.

A Fast Write

Write cycle times are the same as read cycle times: 70 nanoseconds. Further, there are no limitations on the number of write cycles (unlike EEPROM and FLASH), making the DS1645 ideal for real-time data logging. The DS1645 can do a specific byte write, so you don't have to re-write the entire page every time you need to make an update.



How Much Memory Do You Need?

The DS1645 has one megabit of memory that can be divided into 16 8K x 8 blocks. We also offer 256K and 4-megabit Partitionable SRAMs.

For more information on our complete family of nonvolatile SRAMs, give us a call.

DALLAS SEMICONDUCTOR

The leader in NV SRAMs

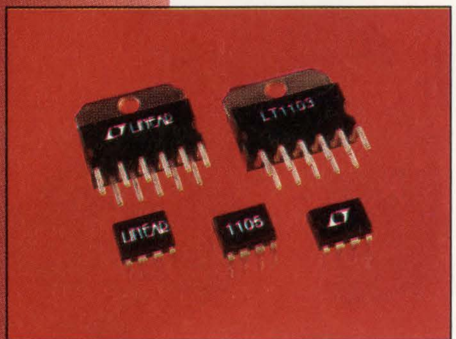
CIRCLE NO. 42

4401 South Beltwood Parkway, Dallas, Texas 75244-3292 Telephone: 214-450-0448 FAX: 214-450-0470

INTEGRATED CIRCUITS AND SEMICONDUCTORS

LT1105 Switching Regulator

The LT1105 switching regulator simplifies off-line switching-power-supply design by eliminating the need for an optocoupler, reference, and error amplifier. The regulator supplies a 15V regulated dc output for driving the totem-pole output stage gate of an external FET and provides ±1% line and load regulation.



Using flyback voltage signals available from a power transformer, the LT1105 operates from universal ac line voltages. On-chip circuitry eliminates or minimizes error sources such as primary leakage inductance spikes, parasitic impedances, and nonlinear transformer behavior.

The regulator eliminates flyback-voltage leakage inductance spikes by creating a blanking period that prevents the spike from entering the measurement circuit. It eliminates skin effects via a sampling scheme triggered by the signal that turns the switch back on.

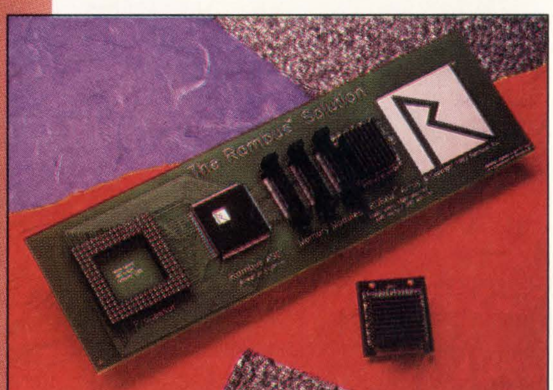
The LT1105 provides an additional level of correction by adjusting the internal reference level upward as the primary current increases. You set the amount of increase by using an external resistor. The regulator costs $4.25 (100).

To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

Linear Technology Corp
Milpitas, CA
(408) 432-1900

Rambus DRAM Technology

The Rambus technology is a revolutionary approach to transferring data between a master and a high-speed RAM that operates at 500 Mbytes/sec. It consists of a 16-line Rambus channel that interconnects Rambus dynamic RAMs (RDRAMs) and a dedicated master, such as a µP or a peripheral. An RDRAM consists of a standard page-mode CMOS DRAM and an on-chip slave Rambus interface. Dedicated µPs and peripherals have a master Rambus interface to control the Rambus channel.



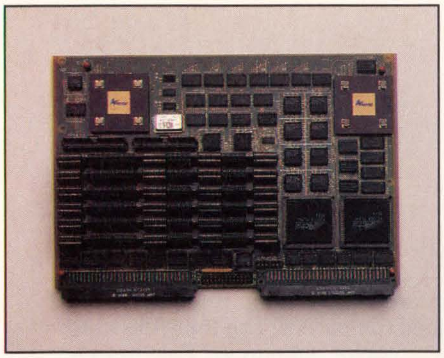
The 16-line Rambus channel consists of nine data, two control, two clock, one ground, one supply, and one voltage reference (VREF) line. The Rambus channel is 10 cm long and has a master on one end and resistive transmission-line terminators on the other. RDRAM packages can be evenly distributed at 100-mil intervals along the line. The two clock lines connect at the master end of the Rambus channel.

The clock signal, which operates at 250 MHz, is synchronous with the data lines and transfers data on both clock edges. Data from the master to the RDRAMs propagates at full voltage and transfers to the RDRAM slave interface on the clock transitions. Data from the RDRAMs must transfer in both directions on the bus. The terminators absorb the data traveling down the receiving end of the line. Half-voltage data levels on the master end reflect to the full-voltage data levels before the master samples the data.

The full-voltage level on the Rambus channel is 600 mV and nominally swings between 2.5V and 1.9V. You can adjust the threshold voltage (VREF) to 2.2V by using external resistors. Currently, the 4-Mbit generation of RDRAMs has a 512k × 9-bit organization. RDRAMs sell at a 25% premium over the price of an ordinary DRAM.

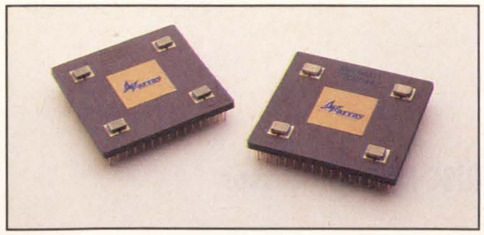
To vote for this entrant as IC and Semiconductor Product of the Year, mark the appropriate box on the ballot.

Rambus Inc
Mountain View, CA
(415) 903-3800



400 MOPS FOR 6U VMEbus SYSTEMS

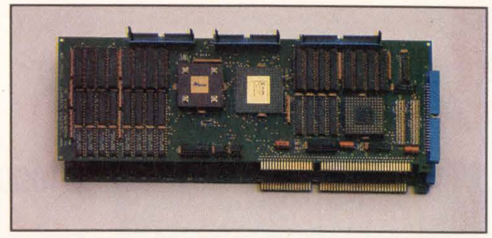
This 6U VMEbus board performs 400 million operations per second and is optimized for frequency domain processing such as FFTs and finite impulse response (FIR) filters using fast convolution. The FDaP features a private 32-bit, 20 MHz high-speed data I/O bus and extensive double buffering for continuous processing of real-time data. An additional 32-bit complex output provides phase/magnitude data. The a66540 is available in 25 MHz and 40 MHz versions. A single 40 MHz version can execute a 1K point FFT in 132.7 µs and a 64K point FFT in 13.1 ms. These times are nearly halved for real input. Multiple FDaPs can be cascaded to achieve almost linear improvement in FFT performance. Plug 400 MOPs into your system by calling **array** Microsystems' Hotline: 719-540-7999.



THE DaSP/PaC CHIPSET:

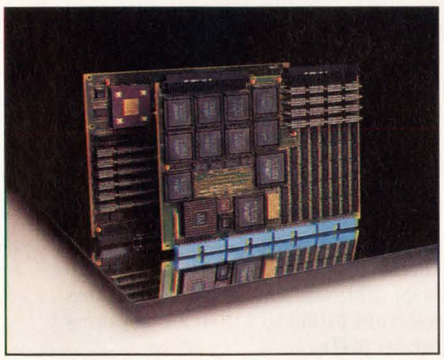
The heart of the world's fastest DSP product family

The Digital array Signal Processor (DaSP) executes 16 high-level instructions, including FFT butterflies, windowing, complex multiplies, and general-purpose functions. The Programmable array Controller (PaC) manages the entire system, including address generation for the DaSP and memory, and I/O up to 80 MHz. Using a single chipset, for example, a 1024 point FFT requires only 12 instructions and can execute in only 131 µsec; a complex FIR filter, using 28 instructions, processes at a 2.3 MHz rate. For even higher performance, you can cascade the chipset. Both utilize a 144-pin PGA format and are available in 30 and 40 MHz versions. To receive complete technical information, call **array** Microsystems' Hotline: 719-540-7999.



PC-FDaP PERFORMS 250 MOPS!

The a66550 Frequency Domain array Processor (FDaP) brings high performance FFT processing to any PC-AT compatible computer. The two board set will fit into two full size PC-AT slots, operate on the 16 bit PC-AT (ISA) bus, and allow real or complex input from either the high speed connectors on the back panel or from the PC-AT bus. The FDaP accommodates an optional complex I-and-Q to magnitude-and-phase converter for post-FFT processing. Available in two memory configurations, the a66550 handles complex FFTs up to 32K points and real FFTs up to 64K points. The a66550 can compute a 1024 point complex FFT in just 210 µs. For complete technical information, call **array** Microsystems' Hotline: 719-540-7999.



CORNERTURN PROVIDES QUANTUM LEAP IN 2D IMAGE PROCESSING PERFORMANCE

The a66545 Cornerturn™ board, used in conjunction with the a66540 FDaP board for real-time two-dimensional image processing, is the first capable of processing an entire 256 x 256 pixel frame of image data in 15.2 milliseconds. This equates to a continuous, real time rate of 65 frames per second. For 512 x 512 images, the board set transforms images in 71 milliseconds, or 14 frames per second. Designed for medical imaging, radar, sonar, machine vision, and other real-time 2D image processing applications, the board set features performance of 400 MOPS at a clock rate of up to 40 MHz. The Cornerturn accepts 32-bit complex I/O data through 10 MHz double-buffered external I/O connectors or through the VMEbus and stores it in one of four on-board frame store memory buffers. For technical assistance, call **array** Microsystems' Hotline: 719-540-7999.

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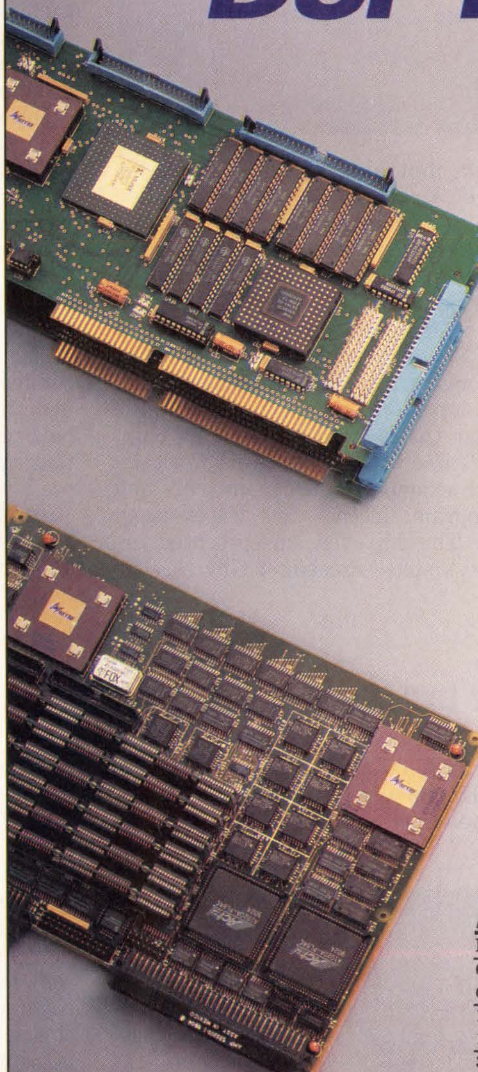
DSP Built For Speed



PC-AT DSP

1K FFT/126µs

DSP engine for the 16-bit PC-AT Industry Standard Architecture (ISA) bus

Performance Benchmarks

FFT size	a66550/32K @25MHz
64 Real	7.2 µs
64 Complex	10.9 µs
1024 Real	125.9 µs
1024 Complex	209.9 µs
32K Real	5.90 ms
32K Complex	10.49 ms
64K Real	15.73 ms
64K Complex	N/A

VME DSP

1K FFT/79.6µs

DSP engine for industry-standard VMEbus

Performance Benchmarks

FFT size	a66540A @40MHz	a66540A Cascade Sys.
64 Real	5.1 µs	2.9 µs
64 Complex	5.0 µs	3.7 µs
1024 Real	79.6 µs	29.6 µs
1024 Complex	132.7 µs	59.1 µs
32K Real	3.69 ms	0.91 ms
32K Complex	6.56 ms	1.82 ms
64K Real	7.37 ms	1.82 ms
64K Complex	13.11 ms	3.64 ms

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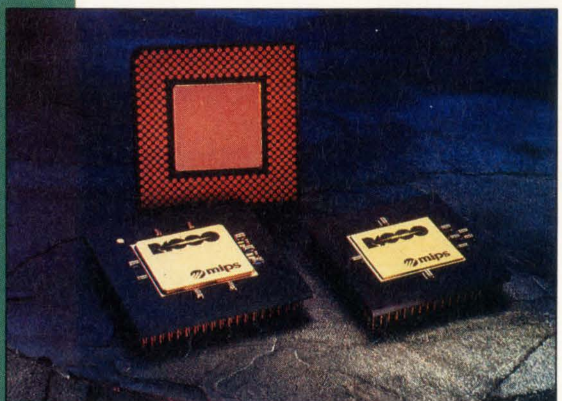
INNOVATION

MICROPROCESSORS

R4000 RISC Microprocessor

Mips Computer Systems Inc
Sunnyvale, CA
(408) 720-1700

The Mips R4000 is a third-generation reduced-instruction-set computer (RISC) μP that serves as the core for general-purpose computers and for



embedded control systems. The 64-bit chip—the first 64-bit μP—supplies execution units for both floating-point and integer math operations. In addition, the basic R4000 architecture supplies a memory-management unit (MMU), 8 kbytes of primary-instruction cache memory, 8 kbytes of primary-data cache memory, and primary and secondary cache-memory controllers.

Although the R4000 is a 64-bit μP chip, it is compatible with earlier Mips 32-bit devices. For example, you can mix 32- and 64-bit programs in the same R4000-based computer. The chip's flat, unsegmented virtual-address space exceeds 4 Gbytes. The R4000 μP comes in three versions. The R4000PC's primary cache memory is meant for use in low-cost desktop computers and in embedded computers. The R4000SC uses secondary cache memory. For multiprocessing systems, the R4000MC lets you add a secondary cache as well as extra R4000MC chips. The MC version uses cache-coherency mechanisms that are needed to synchronize multiple processors.

The Mips chips use superpipelining so that the chip can issue two instructions on each clock cycle. Clock cycles are divided into subcycles internally, and an instruction is issued on each subcycle. The processor can issue and execute back-to-back arithmetic-and-logic unit (ALU) instructions and load-and-store instructions without restriction.

Internal clock circuits let you program the rise and fall times of transmit clock (TCLK) and receive clock (RCLK) signals so that you can match the clocks' characteristics to those of your external loaded transmission lines. You can program the TCLK and RCLK signals to be either one half or one third of the processor's master clock frequency.

The R4000 chip is available from six semiconductor suppliers worldwide. In quantities of 500, the three configurations have prices from $1050 to $1610 for versions that run at 50 MHz.

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

Intel486 DX2 Microprocessor

Intel Corp
Santa Clara, CA
(408) 765-8080

The Intel486 DX2 microprocessor runs at 50 MHz but uses a 25-MHz CPU bus. Thus, the chip can boost system performance without requiring you to design an entire system for high-speed operation.

Like its Intel486 DX predecessor, the Intel486 DX2 comprises an integer unit, a floating-point unit, and an 8-kbyte cache. An on-chip PLL circuit uses the external system clock as an input and produces a faster internal clock. A 3-layer metal process lets the core CPU run at 50 MHz, which is twice the speed of the CPU bus.

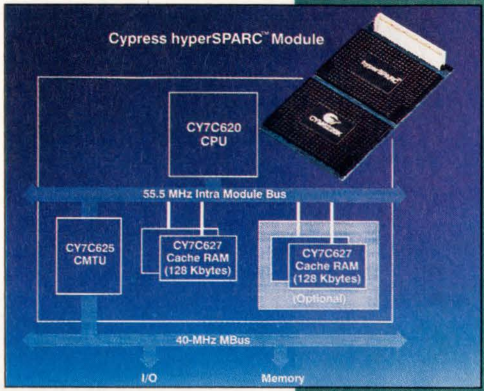
The processor's integer performance is 40.5 MIPS (V1.1 Dhrystones); its overall SPECmark rating is 19.2 (SPEC '89). The device uses a system-management mode for overseeing system power consumption as well as for implementing suspend-and-resume operation. DOS and Unix are among the operating systems ported to the processor. The device comes in a 168-lead pin-grid array and costs $517 (1000).

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

HyperSPARC Processor

The HyperSPARC processor provides a superscalar, superpipelined SPARC processor in a selection of four modules. The modules let you select either one or two processors and either 128 kbytes or 256 kbytes of cache memory. The modules operate on the Mbus architecture, which allows designers to upgrade the processor without having to redesign the computer system. Because designers are looking for low power consumption, low cost, and high operating speeds, Cypress uses a 0.65 μm process to produce the chips. The company uses the same process to manufacture static RAMs (SRAMs). The HyperSPARC chips use 3.3V logic levels for communicating with each other on the module. All off-module signals are standard 5V logic levels.

Instead of putting all of the SPARC architecture on a single chip, Cypress provides a central-processing unit (CPU) chip, a cache and memory-management/tag unit (CMTU) and a cache data unit (CDU). Each CPU chip—there can be one or two on each module—supplies an 8-kbyte two-way set-associative instruction cache. The 128- or 256-kbyte unified cache on the module acts as a primary cache for data, and as a secondary cache for instructions. The modules operate at a clock rate of 66.7 MHz, but later versions should operate at up to 100 MHz. All of the Mbus operations occur at 40 MHz.



At the 66.7-MHz operating frequency, the company claims performance of 70 SPECmarks (Spec '89) and 55 SPECint (Spec '92). Prices start at $3500 each for sample quantities of the single-processor CYM6221 module.

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

Cypress Semiconductor Corp
Ross Technology Div
San Jose, CA
(408) 943-2653

Sproc-1000 DSP Chip

The Sproc-1000 represents a major departure from the architecture and programming methods used with other DSP chips. The chip consists of a central memory unit shared by as many as four 24-bit fixed-point processors. The Sproc processor incorporates all processor units, interprocessor communication circuits, and memory required to develop DSP applications.

Unlike other DSP architectures, which base real-time operations on allocating processing power as interrupts occur, this processor time division multiplexes its central memory to provide concurrency between various processors. The patented memory multiplexing scheme simplifies the programming and coordination of multiple processors that together run a single application. Input and output data-flow managers handle switching between concurrent tasks. These managers communicate with the processors and other on-chip elements through a 12-bit address and 24-bit data bus, and with off-chip I/O devices through a serial port. Off-chip parallel I/O ports are available, too. The price for the 4-GSP member of the Sproc-1000 family is $70 (1000).

The key to the Sproc architecture is the software-development system that you use to compile your application. You enter your design graphically at the block-diagram level. Block diagrams can incorporate both analog and digital elements that reside in the software's cell library. The software tools include a signal-flow editor, a cell library, custom filter-design software, and loading and debugging programs. The software runs on MS-DOS-based computers. Designing your application and programming a Sproc chip requires four steps: creating a signal-flow diagram, compiling and linking the program, downloading your program to the chip, and testing and debugging.

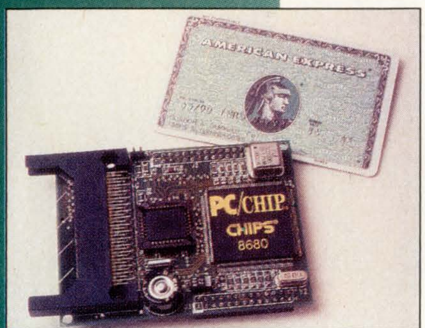
To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

Star Semiconductor Corp
Warren, NJ
(908) 647-9400

INNOVATION

MICROPROCESSORS

8680 PC/Chip



The 8680 PC/Chip from Chips & Technologies supplies the heart of a personal computer on an integrated circuit. Its CPU is compatible with 8086-μP instructions. The chip provides a mode of operation called Superstate, which lets you trap any I/O-port or interrupt call so you can actively monitor and control I/O activities. This type of feature is vital for portable and low-power applications. The attendant Superstate table, registers, and operating circuits are all unseen by software during normal operation. The CPU transfers to the Superstate upon I/O-port operations, normal interrupts, activity on four interrupt pins on the IC, or an internal timer interrupt.

You do not have to act on all of the transferred operations. The Superstate processor lets you identify the actions that you want trapped. In general, the Superstate portion of the chip lets you avoid entanglements with the PC's BIOS and its operating-system complexities. The Superstate frees you from having to monitor I/O-port activity and I/O-port access counts, and from having to wake up any sleeping portions of the system to check for activity.

The Superstate is almost invisible during normal operation of the chip, and the Superstate characteristics cannot be modified by any software that accesses I/O ports, interrupts, memory, or any other system facility. You enter and set up the Superstate's operating mode at power-up or when you reset the chip. Because the Superstate mode is transparent during normal operation, you can use existing operating systems and BIOS routines in your computer system.

In portable or low-power applications, you'd use the Superstate to help you manage power, shutting down peripherals that haven't been used for a given time. Once the computer enters its Superstate, you can enable or disable other events that would cause Superstate actions.

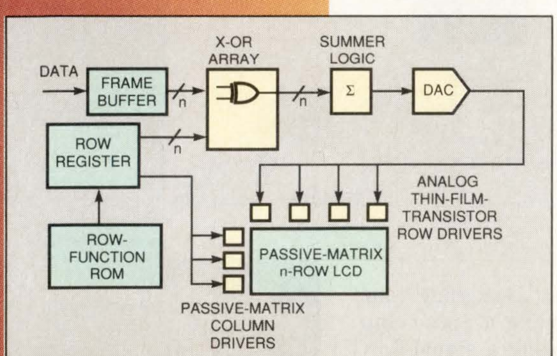
In addition to being compatible with an 8086 μP chip, the chip operates essentially as a personal computer. The 8680 PC/Chip provides all of the necessary PC system logic, a CGA-compatible display controller, and a serial port. The color-graphics-array (CGA) controller operates with either flat-panel or CRT-based displays. You can connect the chip to standard 8-bit I/O devices and ICs. The chip costs $35 (10,000) and comes in a 160-pin quad flatpack.

To vote for this entrant as Microprocessor Product of the Year, mark the appropriate box on the ballot.

Chips & Technologies Inc
San Jose, CA
(408) 434-0600

COMPUTERS AND PERIPHERALS

Active Addressing Technology for LCDs



Active addressing lets passive-matrix LCDs display high-contrast moving images for low production costs. Most experts once believed that only active-matrix LCDs could achieve high-contrast, full-motion images. However, active-matrix displays have a hefty price tag because they use a thin-film transistor for every addressable dot on the screen.

Traditionally, passive-matrix LCDs use electronics that address the display one row at a time. When you use fast (low-viscosity) liquid-crystal material to achieve full-motion video, the optical response of one row significantly decays while the electronics addresses the other rows. The result is low contrast.

Using active addressing, a standard passive-matrix LCD can strobe multiple rows simultaneously and maintain precise voltages at each pixel. The control circuitry sequences through the display's rows using an algorithm, which can cause the circuitry to activate half of the rows simultaneously.

The control circuitry uses the algorithm to calculate the column voltages and uses active-matrix-display analog driver ICs to apply the voltages to each row pattern. The circuitry then calculates the next row pattern and applies new voltages to the columns.

Because active addressing increases the pulse rate to the liquid-crystal material from 16 Hz to well over 1 kHz, the crystal's optical response doesn't have time to decay. Prototypes of passive-matrix LCDs that use active addressing have achieved contrast ratios of 40:1 while reaching switching speeds of 50 msec, which is sufficient to display full-motion video.

To vote for this entrant as Computers and Peripherals Product of the Year, mark the appropriate box on the ballot.

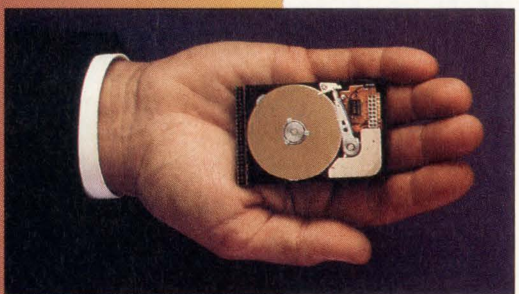
In Focus Systems Inc
Tualatin, OR
(503) 692-4968

INNOVATION

COMPUTERS AND PERIPHERALS

Stingray 1842 1.8-in. Disk Drive

The Stingray 1842 1.8-in. disk drive holds 40 Mbytes and can withstand 300g nonoperating shocks. The dual-platter drive is approximately half the size of a single-platter 2.5-in. drive. With the electronics mounted to the head-disk assembly, the drive measures 76.85×50.8×15 mm and weighs 3.2 oz.



The drive's many features let it meet the rugged requirements of mobile computing. For example, in most drives, the heads drag along the disk surface when the spindle motor stops. Repeated head takeoffs and landings result in friction-induced damage to the head-disk-assembly interface and can cause long-term reliability problems. In contrast, the Stingray 1842 uses a ramp loading and unloading mechanism to prevent the heads from touching the media.

Because the heads don't slap the disk during power-down, the drive can resist a 300g nonoperating shock. During power-down and inactivity periods, the spindle motor's back EMF ensures that the heads are securely loaded and locked on the ramp structure. During power-up, a microprocessor determines when the spindle motor is up to speed before reading the servo bursts and calibrating the heads to read and write data.

The dynamic ramp-loading mechanism lets the drive spin down to sleep mode as many as 1 million times. The drive consumes 15 mW in sleep mode and can recover from this mode in approximately 1.5 sec. Because the heads do not drag on the media, spin-ups and spin-downs are faster and consume less power than those of conventional drives.

Other specifications include an 18-msec access time, 0.8A start-up current, 3571-rpm spindle speed, interface transfer rate of 4.0 Mbytes/sec, media transfer rate as fast as 1.9 Mbytes/sec, −40 to +70°C operation; and a 100,000-hour MTBF. The drive costs $285 ($1000 per month OEM).

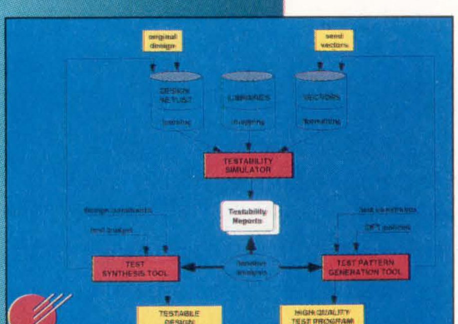
To vote for this entrant as Computer and Peripherals Product of the Year, mark the appropriate box on the ballot.

Intégral Peripherals Inc
Boulder, CO
(303) 449-8009

CAE/CAD

TestGen Sequential ATPG Software

TestGen is automatic test pattern generation (ATPG) software that creates manufacturing test programs for digital sequential integrated circuits. It consists of a sequential vector generator, a high-speed software fault simulator, a suite of test-synthesis and testability-analysis tools, and a dynamic vector compactor. The software works at the gate level and uses nine proprietary circuit-analysis techniques. It requires only netlist input.



TestGen works with all types of digital integrated circuits from single-clock, fully synchronous circuits to multiple, internally generated, gated clocks in highly asynchronous circuits. It uses a single-fault model: stuck-at-1 and stuck-at-0. The product works with circuits using built-in self-test (BIST), JTAG, and other test methodologies.

The software also identifies and grades difficult-to-test areas on the target circuit prior to vector generation. After the designer selects the percentage of partial scan to use in the current vector generation session, the TestGen selectively includes flip-flops in the scan chain. Before vector generation, it recommends where to add more test structures to the circuit to make it more testable. It also compacts test vectors, thereby reducing test program size by 50 to 300%.

For forward-time processing, the software uses the targeted D frontier technique, which greatly increases the number of mandatory assignments by limiting the D frontier to one target D element. This reduces the overspecification of state variables that can result when using other algorithms. In reverse-time processing, TestGen uses the state knowledge of previously generated vectors for state justification, avoiding the memory overhead of a state-transition diagram.

For faults aborted during the standard test-generation phase, the software uses knowledge that it gained about fault propagation from the fault simulator. A single-process floating license costs $95,000.

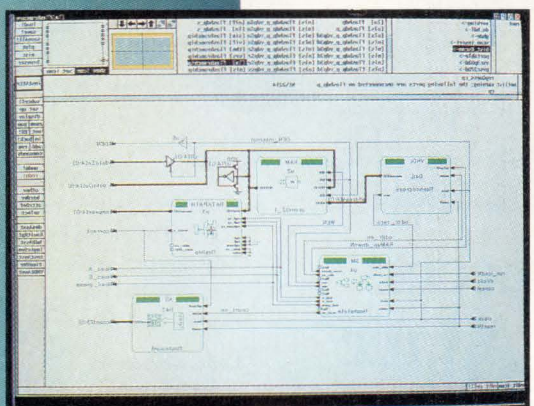
To vote for this entrant as CAE/CAD Product of the Year, mark the appropriate box on the ballot.

Sunrise Test Systems Inc
Sunnyvale, CA
(408) 739-4000

ASIC Navigator

Compass Design Automation
San Jose, CA
(408) 434-4880

Although many ASIC development systems shackle you to one design method, the ASIC Navigator lets you use several graphics- and text-based design techniques to create just one ASIC or systems of ASICs using a top-down approach. This product covers the entire design cycle by providing tools for design specification, verification, partitioning, synthesis, and floorplanning.



Graphic design entry styles that the ASIC Navigator uses include schematics, state-machine diagrams, tables, and data-path diagrams. You can also enter text descriptions of blocks using either VHDL (VHSIC Hardware Description Language) or the Verilog hardware description language. A graphic block diagram ties all of the individually specified blocks together.

The product synthesizes a VHDL model from a system specification using any or all of the above entry methods. This model then becomes the focus of your verification efforts. You verify through simulation. The ASIC Navigator's simulator can handle a mix of behavioral and structural VHDL descriptions, so you can start simulations before your detailed design specification is complete. The product's partitioner divides your design into physically realizable portions and lets you play "what if?" games with your design to find an optimal system configuration.

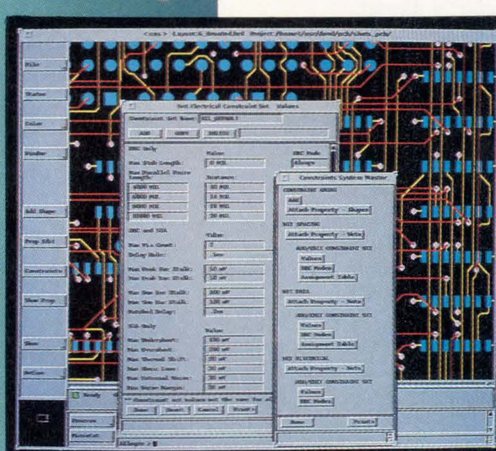
A Test Assistant module accepts high-level descriptions of your test strategies so that the logic synthesizer can create the appropriate test circuitry. A timing verifier tells you what effect the additional test circuitry will have on your design. The logic synthesizer uses a variety of synthesis and logic compilers to create logic from your design specifications. The individual synthesis tools include modules for synthesizing control circuits, random logic, data-paths, multipliers, memories, and test circuitry. The synthesizer can also handle three-state logic, I/O pads, and balanced clock trees. Prices start at $95,000 per seat.

To vote for this entrant as CAE/CAD Product of the Year, mark the appropriate box on the ballot.

Allegro Correct-By-Design Software

Cadence Design Systems Inc
Chelmsford, MA
(508) 256-2300

Allegro Correct-By-Design (CBD) software lets you create physical designs for pc boards, hybrid circuits, and multichip modules. Because the package integrates place-and-route tools with front-end design-analysis tools, it short-circuits the design-analyze-redesign loop.

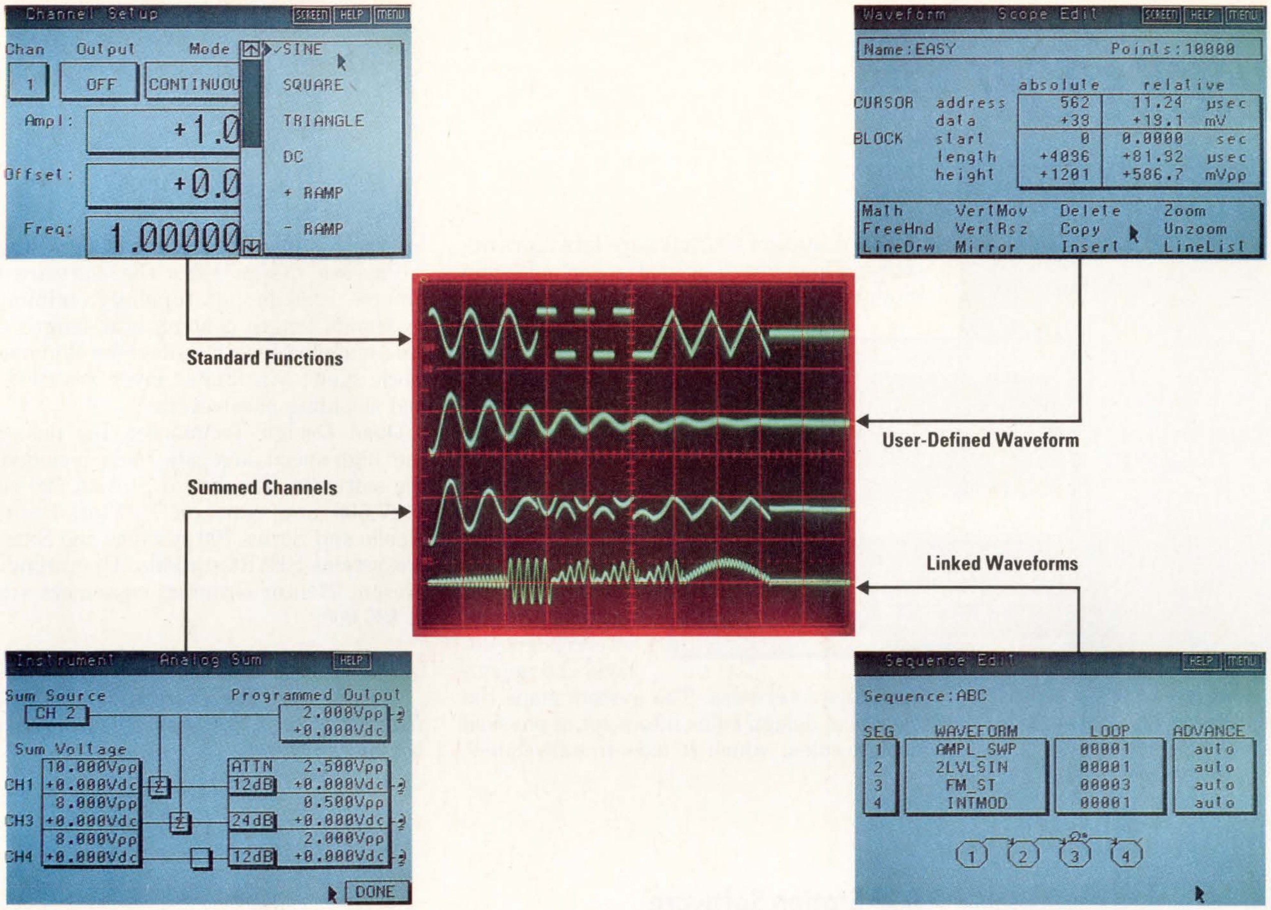


Using Allegro CBD, you can assign system constraints early in the design process. You specify rules by part, net, group, page, and other classifications. Defined component placement, critical timing paths, and etch width are among rules the software can enforce. The software applies these rules across multiple packaging technologies.

Central to the software is a constraints editor that lets you establish electrical, physical, and thermal limits. A design-rule checker ensures that the software adheres to the limits you set during interactive and automatic board-layout sessions. The system can defer or ignore constraints via an overriding configuration-management control module.

The software is available for Hewlett-Packard PA-RISC-based computers, as well as for workstations from Sun Microsystems, Digital Equipment Corp, and IBM. Prices range from $12,500 to $60,000, depending on the configuration.

To vote for this entrant as CAE/CAD Product of the Year, mark the appropriate box on the ballot.



Just A Sample Of What The First 50 MHz Four-Channel Arb Can Do.

You're looking at the most versatile Arbitrary Waveform Generator you can buy. Speed, resolution and a choice of 1 to 4 synthesized channels mean that Wavetek's new Model 295 can take the place of multiple instruments in a wide variety of applications.

Model 295 is easy to use, too. For example, a handy mouse lets you quickly create waveforms on an oscilloscope. You can use the convenient front panel keyboard to enter math expressions or recall stored waveforms. A sophisticated graphic interface provides windows-like pull-down menus with easy-to-follow steps to make waveform creation and editing easier than ever before.

Waveforms created remotely can be loaded into the Model 295 via GPIB. An optional 3.5" disk drive allows unlimited waveform storage. Waveform looping and linking, along with inter-channel triggering, summing, and phase control, give you still more flexibility.

Each channel can operate like a separate Arb with 50 MHz sampling frequency, exceptional 2 ppm accuracy, and 12 bit vertical resolution. In addition, channels can be synchronized.

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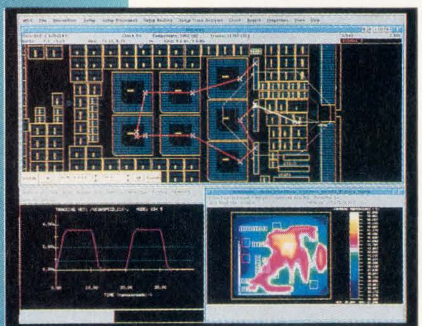
WAVETEK

Circle #6 For Literature Circle #7 For Demo

Board Station 500 software lets users design high-speed pc boards and multichip modules. The software combines timing-constraint-driven place-and-route algorithms and high-speed design-analysis tools.



The system lets designers specify a set of electrical rules covering topology constraints, interconnect delays, and impedance characteristics. The system maps the electrical design rules into a set of physical design rules, which it uses in subsequent interactive place-and-route design stages.

Physical design rules the software can enforce include net topology, minimum/maximum length control, stub-length control, matched-length control for eliminating clock skew, via limits, layer restrictions, and shielding parameters.

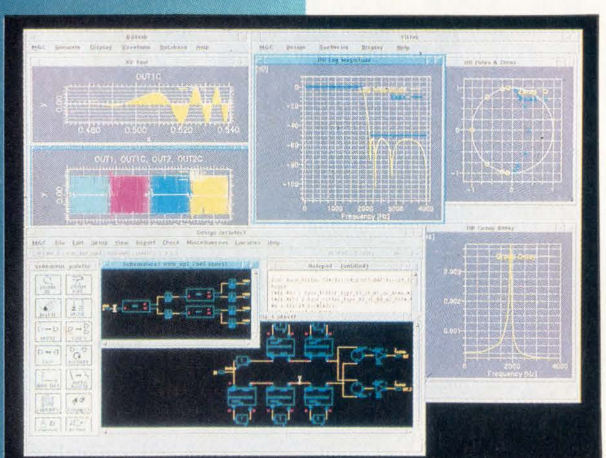
Quad Design Technology Inc designed the high-speed analysis tools included in the software. The Board Station 500 costs $127,500 and runs on Hewlett-Packard Apollo and Series 700 systems and Sun Microsystems SPARCstations. Upgrading for present Mentor Graphics customers starts at $30,000.

To vote for this entrant as CAE/CAD Product of the Year, mark the appropriate box on the ballot.

Mentor Graphics Corp
PCB Division
San Jose, CA
(408) 436-1500

DSP Station Software

The DSP Station software performs top-down design of DSP systems from high-level specifications through simulation and optimization from multiple physical implementations.



The software provides analysis tools that address the needs of the DSP designer, such as noise and stability analysis, area vs bandwidth tradeoffs, and frequency-domain sensitivity analysis.

DSP Station also helps you plan development and production times for your proposed DSP system and analyze cost/performance ratios. For fast implementation, you can use the software to generate assembly code for a commercial DSP chip. For quick prototype development, you can synthesize a design for a gate array or an FPGA. For the best cost/performance ratio, you can use high-level synthesis to create designs for standard cell module generators. DSP Station lets you use a common input format to drive all the implementation paths.

The software also helps you analyze hardware/software tradeoffs, as well as analog/digital partitioning, from the early phases of design. It also lets you compare various system architectures.

The package includes three forms of synthesis: filter designs, assembly language code for programmable DSPs, and DSP architectures for custom integrated circuits.

The filter design synthesis uses arithmetic optimization techniques in addition to the normal filter approximation routines. Assembly language synthesis uses optimizing techniques to map all your DSP functions onto the particular architecture of the target programmable processor. Silicon synthesis utilizes either bit-serial or bit-parallel modules configured in an optimal design based on scheduling for each signal processing task.

The product, which starts at $33,000, represents a cooperative development effort of a university research lab (Interuniversity Microelectronics Center), an industrial customer (Philips), and a commercial CAE vendor (Mentor Graphics Corp).

To vote for this entrant as CAE/CAD Product of the Year, mark the appropriate box on the ballot.

Mentor Graphics Corp
San Jose, CA
(503) 685-7000
European Development Center
Leuven, Belgium
(32) 16-203063

Minimum Daily Requirement

Compact TOKIN Surface Mount Devices
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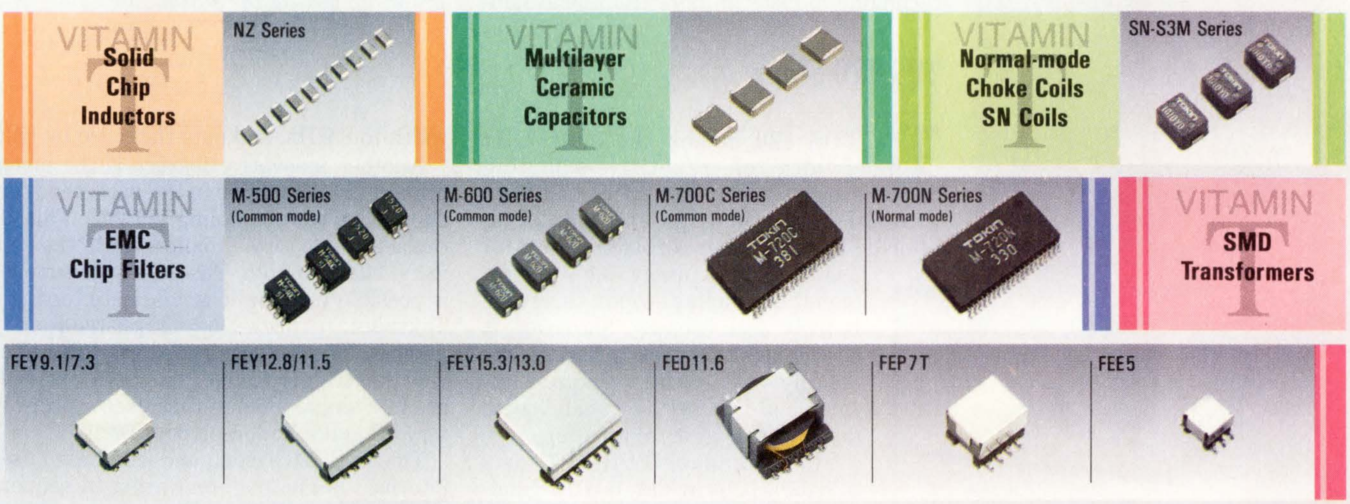

TOKIN

Tokin Corporation

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Phone: 367-9157 Fax: 739-5950
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Phone: 2237076 Fax: 2236093, 2278772

Tokin Europe GmbH

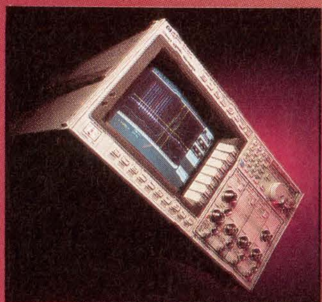
Knorrstr. 142, 8000 München 45, Germany
Phone: 089-311 10 66 Fax: 089-311 35 84

CIRCLE NO. 43

INNOVATION

TEST AND MEASUREMENT

HP 54720A Real-Time-Sampling DSO



Hewlett-Packard Co
Colorado Springs, CO
(800) 452-4844

For capturing single-shot transients, the HP 54720A is, at 4G 8-bit samples/sec on two channels simultaneously, currently the fastest sampling, highest-bandwidth digital scope available as a standard product. Where the waveforms are repetitive, however, sequential-sampling scopes offer greater bandwidth. (The 54720A's bandwidth is 1.1 GHz for single-shot phenomena and 1.5 GHz for repetitive waveforms.) The modular scope has a high-resolution color display, a numeric keypad, and a 3½-in. disk drive. The instrument costs more than $55,000 with probes. You can also configure the scope with four channels that each take 2 Gsamples/sec.

The heart of the scope's acquisition system is a hybrid-circuit module built around a sampler (a proprietary bipolar IC) and four 0.5-Gsample/sec flash ADCs (implemented on proprietary bipolar ICs that each contain two ADCs). The four ADCs take interleaved samples to form a 2-Gsample/sec converter. When you configure the unit with two 4-Gsample/sec plug-ins, pairs of these hybrid modules act in concert to achieve the 4-Gsample/sec acquisition rate on both channels simultaneously. Hence, each 4-Gsample/sec channel contains eight 0.5-Gsample/sec ADCs.

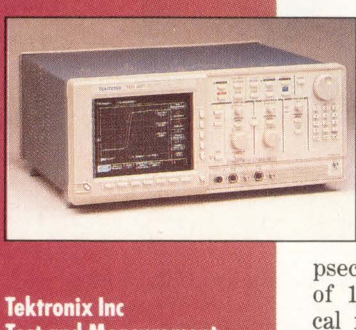
The sampler uses a sample-and-filter technique in place of more traditional sample-and-hold or track-and-hold circuits. In the sampler, the charge held on the sampling gate bleeds off at a precise rate, halving the required postamplifier bandwidth and permitting the use of an amplifier with only moderately high input impedance. The lowpass filters that follow the postamplifier use thick-film inductors and capacitors printed onto the hybrid substrate. The system exhibits noise of 250 μV rms; with its ¼ sampling-rate finite-impulse-response filters enabled, it exhibits a resolution of 6.2 effective bits with a 1-GHz signal and 7.5 bits with a 1-MHz signal.

Obtaining all of the performance this sampling technology is capable of requires extremely precise triggering. A dual-slope trigger interpolator produces a time-interval measurement resolution of 1 psec and provides timing accuracy of ±(30 psec + 0.007%) when averaging 16 measurements in the equivalent-time sampling mode. The rms jitter is 6 psec ±0.005% of the delay setting.

The scope also features memory depths to 32 ksamples, a display-update rate of 170 waveforms/sec, and 19 automatic measurements with user-definable parameters.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

TDS 820 Scope



Tektronix Inc
Test and Measurement Group
Beaverton, OR
(800) 426-2200;
(503) 627-7111

The TDS 820 makes the multi-GHz bandwidth of repetitive-sampling digital scopes, which heretofore had been available only in high-end products, affordable to a much broader group of users. Unlike many high-end sequential-sampling scopes, this scope is truly user friendly. Moreover, it overcomes a frustrating shortcoming of earlier sequential-sampling DSOs—their inability to display pretrigger information.

The 2-channel TDS 820 costs $19,100. It provides 6-GHz bandwidth, 0.4-psec timing resolution, 3-psec rms jitter, a maximum record length of 15,000 samples/channel, 14-bit vertical resolution, and typical input noise of 600 μV (waveform averaging cuts the effective noise by factors as great as 100). Moreover, by holding the bandwidth to a "mere" 6 GHz, the designers incorporated a signal delay line in each channel that stores 1.5 nsec of pretrigger data and allows internal triggering. Deleting the delay lines saves $450, increases the bandwidth to 8 GHz, and cuts the noise by half.

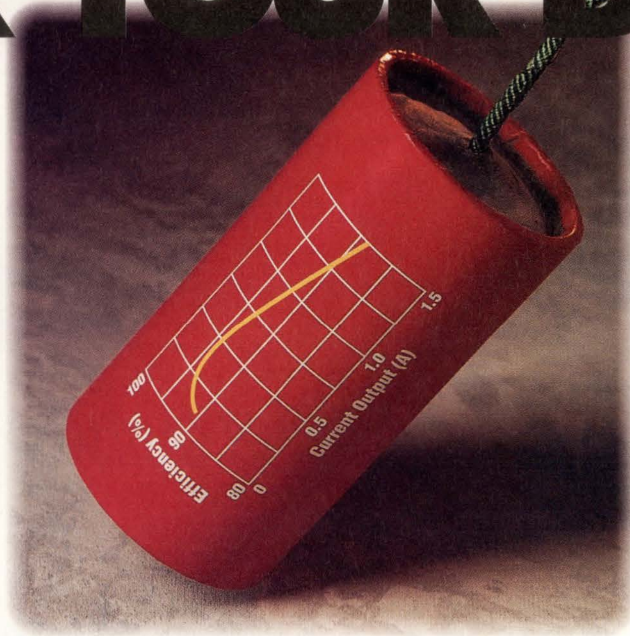
Another innovative feature is the monolithic charge amplifier in the patented traveling-wave-gate sampling system. This IC replaces the hybrid circuit used in the vendor's 11800 family. The IC's performance is possible because it is fabricated using a Tektronix-proprietary high-frequency process. The two compensated delay lines and the trigger pickoff for both channels are in a single module that uses a proprietary IC and a Teflon pc board.

The TDS 820's menu and icon-based user interface is another innovation in sequential-sampling DSOs. The scope's high-resolution monochrome CRT displays a 16-level gray scale. The scope can present the display in the form of dots or vectors, and you can select infinite or 250-msec-to-10-sec variable persistence. Cursor measurements and 24 automatic measurements with variable thresholds further enhance the unit's usefulness.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

What do designers of notebook computers and other battery-powered systems get with Siliconix' new power conversion chip set?

MORE BANG FOR YOUR BUCK.



That means higher power conversion efficiency, smaller system size, both 3.3-V and 5-V compatibility and longer battery life. DC/DC conversion at 94% measured efficiency.

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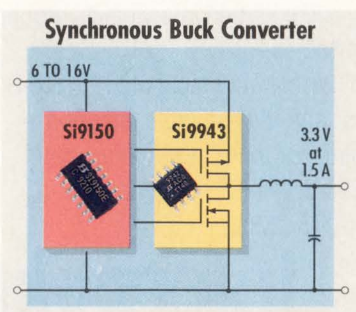

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Siliconix

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Fax: (408) 727-5414, Attn. Mailstop 43-970

INNOVATION

TEST AND MEASUREMENT

90-Series Scopemeters

In packages that measure 2.4×5.1×10.2-in. and weigh 4 lb (with batteries), the 90-series Scopemeters provide all the measurement functions many engineers need. The units act as 2-channel digital storage os cilloscopes (DSOs) with 50 MHz repetitive-signal band-width and 4-digit multimeters (DMMs). The 97, which has an electroluminescent back-lit display, also includes a sine/square-wave generator. Prices range from $1195 to $1795.

Although these instruments are not the first small scopes with LCDs, they are the first with such displays to offer so many features. The features include a 3000-count DMM. The DMM, which resolves >4000 counts without overloading, shares its input leads with the scope's channel A. Scopes that make cursor measurements also provide numeric readouts, but few of them can indicate such quantities as an ac waveform's rms value; these units can. Moreover, few scopes include a calibrator—as these units do—to ensure 3⅔-digit accuracy of their cursor measurements.

Most DSOs of even moderate bandwidth are ac powered and fan cooled. These units use so little power that, not only can they be convection cooled, they are sealed against moisture (they aren't waterproof, however). Furthermore, the units' low power consumption lets them run for four hours before their NiCd cells need recharging. If you don't have access to ac for battery charging, you can replace the NiCd cells with C-size alkaline cells.

Inputs that are isolated from the chassis are commonplace in high-quality digital meters, but you won't find such inputs on most scopes. As a result, measuring waveforms in the presence of high common-mode voltages subjects operators to the possibility of a lethal shock. To provide protection in such applications, the Scopemeters' inputs withstand 600V rms with respect to the case. Using the model 97's RS-232C port to, say, send a waveform to a recorder, doesn't defeat the isolation; the port is optically isolated. The serial-interface cable includes an optical-to-electrical converter powered from the receiving device's RS-232C port.

The most novel technology embodied in the units relates to their measuring capabilities. An 8-bit ADC digitizes the signals for both the waveform and numeric displays at a rate of 25 Msamples/sec. The numeric display uses digital-signal-processing (DSP) techniques implemented in a proprietary IC (one of two in each instrument) to convert the ADC's 8-bit output to a resolution equivalent to approximately 13 bits. DSP techniques also extract the rms values of ac waveforms. On the 95 and 97, you can also obtain readouts in dB and watts.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

John Fluke Mfg Co Inc
Everett, WA
Philips Test and Measurement
Eindhoven, The Netherlands
(800) 443-5853;
(206) 356-5500

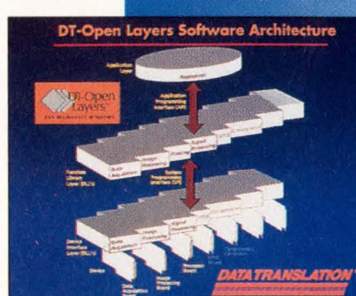
SOFTWARE

DT-Open Layers Software Standard

DT-Open Layers, a proposed software standard for Windows-based data-acquisition and image-analysis applications, offers the possibility of changing your system's hardware configuration without altering your application software. The standard ensures that different hardware devices will perform specific application operations—such as sampling an input voltage or capturing an image—identically, even when those devices require different instructions to perform the operations.

Application programs' hardware independence results from the standard's two main components—a set of application-programming interfaces (APIs) and a system-programming interface (SPI). The APIs are standard interfaces between application programs and function libraries; the SPI is a standard link between function libraries and device-driver software. DT-Open Layers requires use of function libraries and driver software implemented with Windows' dynamic-link libraries (DLLs).

The APIs in DT-Open Layers define generic entry points, parameters, and structures for existing and foreseeable image-processing and data-acquisition functions. The SPI takes advantage of Windows' installable-driver concept; using Windows-compatible message-passing routines, it allows functions and application programs to query and determine the types and abilities of hardware devices, thus taking advantage of hardware features that might otherwise be implemented in software.



The DT-Open Layers standard is available to anyone at no charge.

To vote for this entrant as Software Product of the Year, mark the appropriate box on the ballot.

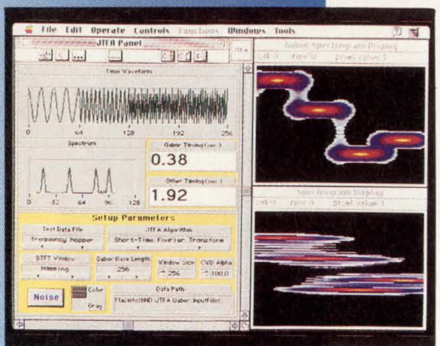
Data Translation Inc
Marlboro, MA
(508) 481-3700

INNOVATION

SOFTWARE

Gabor Spectrogram

The Gabor Spectrogram represents a signal's power spectra in the joint time-frequency plane. The spectrogram gives up to twice the resolution of an equivalent short-time Fourier transform (STFT) and runs six times faster due to its greater computational efficiency. National Instruments announced this algorithm at the March 1992 International Conference on Acoustics, Speech, and Signal Processing and includes it in the $1995 Labview for Macintosh and $1495 Labwindows for DOS Analysis Libraries.



The company developed this spectrogram by first applying its own "orthogonal-like" Discrete Gabor Transform (DGT) to a signal, followed by the pseudo Wigner-Ville Distribution (PWVD). The DGT and the PWVD have been known for decades but have seen limited practical use because they are difficult to implement. The company's "orthogonal-like" DGT resolves difficulties with the DGT in the selection of basis functions and auxiliary window functions. In addition, combining the DGT with the PWVD removes some of the PWVD's liabilities.

The DGT decomposes a signal into a linear combination of time-shifted and frequency-modulated Gaussian basis functions. Gaussian basis functions require fewer spectral coefficients than does the STFT, which makes it easier for your computer to perform a DGT. The PWVD also gives better joint time-frequency resolution than the STFT. But the PWVD suffers from mathematical artifacts that lack physical interpretation, such as cross-term interference and negative terms. By using the DGT with the PWVD, the spectrogram separates the artifacts from the useful terms. The spectrogram also allows precalculating the PWVDs of the basis functions and storing them in a lookup table, making computation faster than the equivalent STFT.

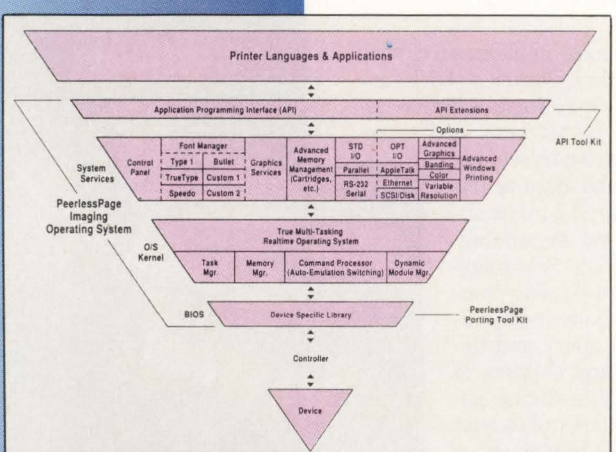
You use the spectrogram for analyzing time-varying signals where simultaneous time-frequency results are necessary. Applications include speech processing and recognition, image processing, synthetic music, seismic exploration, sonar, radar, acoustics, vibration analysis, medical imaging, data compression, and computerized vision.

To vote for this entrant as Software Product of the Year, mark the appropriate box on the ballot.

National Instruments
Austin, TX
(512) 794-0100

Peerless Imaging Operating Environment

The Peerlesspage imaging operating environment simplifies the development of printing and imaging application programs and makes those programs virtually hardware independent. Software services provided by Peerlesspage for printing and imaging products are somewhat analogous to the services that MS-DOS provides for PCs. Designers making use of those services can shorten product-development times.



The heart of Peerlesspage is a real-time multitasking operating system designed specifically for printing, imaging, and graphics applications. Extensions include printer emulations, page-description languages, font management, and control-panel management. Printer languages available with the environment include PCL 4 and 5, Postscript level II, HPGL, IBM Proprinter, and Diablo 630. Font support includes Postscript, Truetype, and Bitstream. A software banding algorithm reduces memory requirements for high-resolution printing—1200 × 600-dpi images require only 2 Mbytes, compared with 10 Mbytes for printers without the software.

Products that can use Peerlesspage include standard page printers, stand-alone network printers, publishing systems, scanning and image-capture systems, multifunction peripherals (printer, scanner, and fax), and graphics-display subsystems. Versions of the environment are available for Intel i960, AMD 29000, and Mips R3000 μPs. Price is negotiable with each OEM contract; use of the product typically adds $5 to the end-user price of a printer.

To vote for this entrant as Software Product of the Year, mark the appropriate box on the ballot.

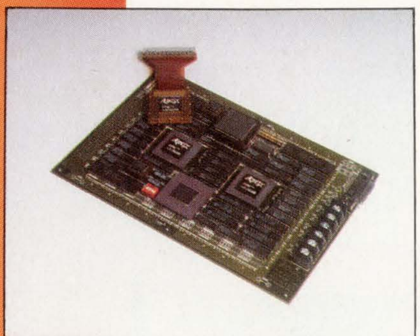
Peerless Systems Corp
Redondo Beach, CA
(310) 536-0908

INNOVATION

COMPONENTS, HARDWARE, AND INTERCONNECTS

AX1024 Programmable Interconnect Device

The AX1024 field-programmable interconnect components can create a resistive circuit path between any two of 940 inputs and outputs. Each device has a RAM-based programming scheme that enables you to reprogram device connections on the fly.



A programmed connection uses a pass transistor to electrically join two of the I/O pins. Once activated, the pass transistor stays on, making the bandwidth of the AX1024 interconnect independent of the transistor's switching speed. Signals sent through the interconnect device must stay between 0 and 5V, but they do not have to conform to any logic levels; they can even be analog signals.

The interconnect device is available in two versions. In addition to its 940 interconnect pins, the $2938 AX1024D provides 64 diagnostic pins on an attached flex cable. The device package features spring-loaded connecting pins and is intended for prototype troubleshooting.

The $1105 AX1024R has no diagnostic pins. This unit is housed in a more conventional surface-mountable pin-grid array. Both of these devices connect to a pc board using a 32×32-pad array spaced on 40-mil centers.

You need software to make these programmable devices useful. The development software currently available runs on SPARCstations and costs $15,000. The company plans to announce PC software shortly. Two prototyping boards are available that will help you use the AX1024 devices.

Aptix Corp
San Jose, CA
(408) 428-6200

To vote for this entrant as Component, Hardware, and Interconnect Product of the Year, mark the appropriate box on the ballot.

Active Eurocard Connector

The Active Eurocard Connector is a pc-board-to-backplane connection system that lets you mount a daughter card having active circuits on the connector. The right-angle connector attaches to the pc board via 126 solder-tail pins on 0.1-in. centerline spacings. The VMEbus- and Multibus II-compatible connector mates with all standard Type C Eurocard DIN backplane connectors having 96 pins on three rows.

By incorporating active devices on the connector, you can shorten the signal path from an IC to the backplane. The shorter distance can improve signal integrity and reduce the bus-loading effects caused by distributed capacitance and inductance. The active connector also frees up board space for other components, which is helpful for dense board designs.

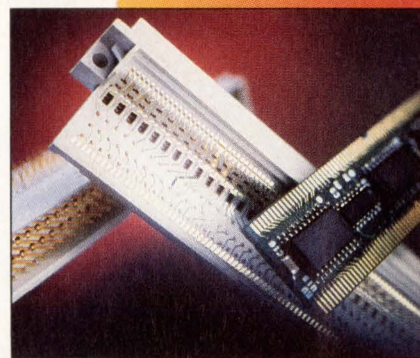
The connector has a liquid-crystal-polymer housing that can withstand infrared and vapor-phase soldering processes. The connector's two metal-on-elastomer strips fit into housing grooves to connect the daughter card to the connector. A module-retaining bracket fits over the daughter card and onto the connector. The card can hold customer-supplied ICs or devices the company supplies. The connector's phosphor-bronze contacts have a minimum of 30 μin. of gold plating.

Tests show that the active connector improves upon standard Eurocard DIN connectors. For example, the Active Eurocard Connector exhibits 6 pF of capacitance and 21 nH of inductance compared with 13 pF and 45 nH for a standard Eurocard connector that has a through-hole VMEbus-board design. The active connector also minimizes crosstalk and impedance variations. For 2-nsec rise times and seven lines switching simultaneously, a standard connector exhibits twice as much crosstalk as the active connector. The impedance deviation measures 10% less for the active connector. $14 to $15, excluding active devices (OEM).

To vote for this entrant as Component, Hardware, and Interconnect Product of the Year, mark the appropriate box on the ballot.

INNOVATION

COMPONENTS, HARDWARE, AND INTERCONNECTS



AMP Inc
Technology and Strategic Products Group
Harrisburg, PA
(717) 564-0100

COMPONENTS, HARDWARE, AND INTERCONNECTS

Flexible Universal PLCC ZIF Test Socket

Aries Electronics Inc
Frenchtown, NJ
(908) 996-6841

Devices in plastic leaded chip carriers (PLCCs) can be difficult to test or program because there are at least seven PLCC package types. Instead of fussing with different sockets, you can use the Universal PLCC ZIF Test Socket from Aires Electronics. This zero-insertion-force (ZIF) socket quickly adapts itself to 20-, 28-, 32-, 44-, 52-, 68-, and 84-pin PLCC packages.

As you rotate the handle on the top half of the socket, four jaws open or close in unison to adapt the socket to a specific package. Releasing the handle lets the spring-loaded jaws firmly hold the corners of the chip in the "dead-bug" position (pins pointing up). As you close the clamshell case, the top latches to the bottom to hold the chip firmly for testing or programming. As the socket's name implies, no force is necessary to seat the chip in the socket, although some force is needed to latch the top and bottom parts of the socket assembly.

Closing the socket and latching the top half in place establishes the contacts between the socket's contact springs and the PLCC's leads. The contact springs are actually long fingers that extend into the center of the socket in a pattern resembling the letter X. This arrangement lets the socket accept a large family of PLCC devices without rearranging contacts or using adapter boards. Thus, the same set of metal fingers makes a positive contact with the leads on any of the PLCC packages noted above. The chip-holding mechanism provides inserts that adapt the socket to 32-pin rectangular PLCCs.

The socket suits products that require you to frequently change PLCCs; for example, test equipment, device programmers, and burn-in systems. You can also use the socket in applications that may require different types of PLCCs during development and prototyping. Cost is $200 per socket.

To vote for this entry as Component, Hardware, and Interconnect Product of the Year, mark the appropriate box on the ballot.

INNOVATION

POWER SOURCES

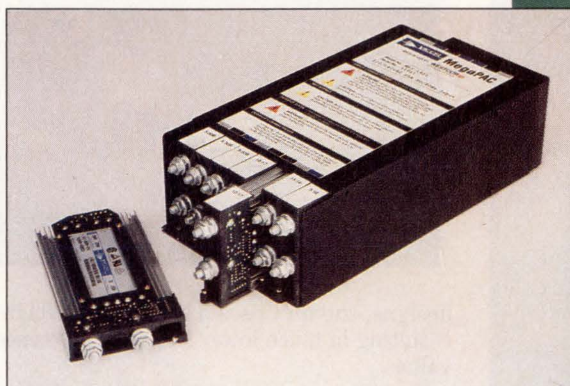
Megapac Power Supply

The Megapac is a field-configurable, off-line switching power supply. The unit consists of a bulk line-to-dc supply and any of one to eight slide-in modular assemblies. Each module contains a dc/dc converter that can generate as much as 200W at 2 to 95V.

Users can readily customize the Megapac by inserting converter modules of different voltages or power levels. To do so, you remove a single screw, slide the existing module out, and then insert a new module. You can parallel the modules with bus bars to provide high-current arrays of as much as 240A per power supply.

All Megapac outputs feature remote sense, overvoltage protection, and current limit. Line regulation (from high line to low line) equals ±0.1% and load regulation (no load to full load) measures ±1%. Efficiency figures range from 80 to 85%, depending on the output voltage, and set-point accuracy equals 1%. The units meet VDE 0871 and FCC 20780 class A requirements for conducted EMI.

A fully configured Megapac converter is housed in a fan-cooled package measuring 11.8×6×3.4 in. The supply is available in commercial and industrial versions with operating ranges of 0 to 65°C and −20 to +65°C, respectively. Prices range from $885 to $1685.



To vote for this entry as Power Source Product of the Year, mark the appropriate box on the ballot.

Westcor Corp
Los Gatos, CA
(408) 395-7050

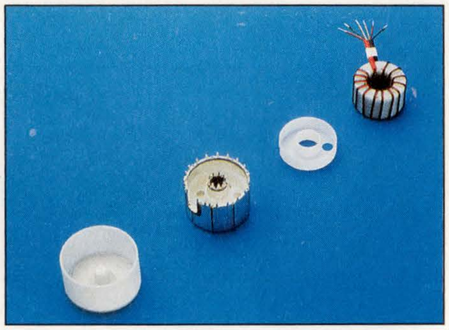
INNOVATION

POWER SOURCES

Philips Industrial Activities SA
1301 Wavre, Belgium
10-438211

3D-PCB Transformer

The 3D-PCB transformer facilitates the design of the magnetics section in high-frequency switching power supplies. Rather than rely on traditional core



designs, the unit uses a segmented design, resulting in much lower leakage inductance values.

Transformer construction uses a ferrite core in the form of a torus with a center hole. The primary winding is wound directly around the core. The secondary winding is made up of a number of electrically conductive segments. These segments, which are formed somewhat like U-shaped plates, feature mounting pins that you solder to a pc board. The transformer is not fully assembled until the secondary segments have been soldered to the board.

All segments are metallized portions of the outer surface of a cap made from an electrical insulating material, such as plastic. The design integrates one plastic cap for the earth shield, the secondary insulation provided by the plastic cap itself, and several turns of secondary windings.

You can connect the secondary turns in series, in parallel, or in series-parallel combinations via connections on the pc board. Thus, you can tailor the transformer to provide output-voltage and current values to satisfy many user-specific applications. The 3D-PCB transformer is currently being used in a line of 300W supplies. Because the unit is a custom design, prices depend on user requirements.

To vote for this entrant as Power Source Product of the Year, mark the appropriate box on the ballot.

BOARD-LEVEL PROTECTIVE DEVICES

Units provide extra insurance against electronic disaster

TOM ORMOND, Senior Technical Editor

You can never have too much protection. By augmenting primary system protection with some secondary protection at the pc-board level, you can greatly enhance the reliability of your system.

Surges (or transients), be they current or voltage in nature, are a fact of life in any system or electrical interconnection. As a result, proper design techniques must include protective devices.

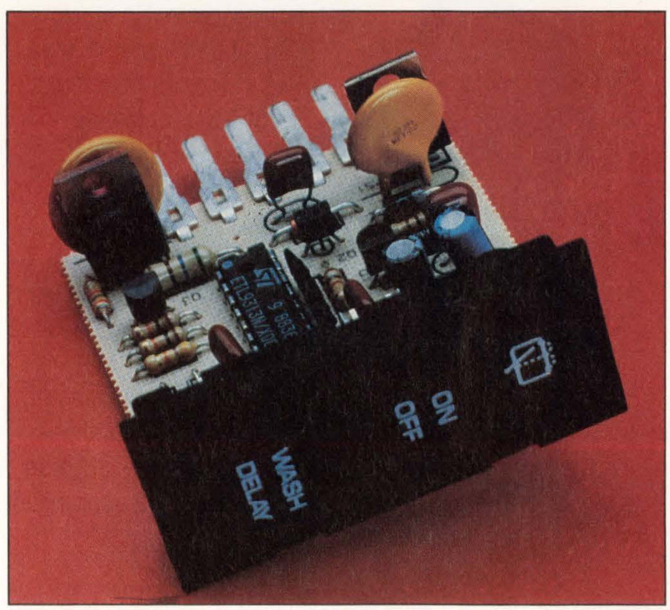
You should not treat transient protection as an afterthought in the system design cycle. In a system with no transient suppression, the weakest device will absorb most of the transient energy and probably fail. If you replace this device with one having higher ratings, then the next weakest device in the system will assume the role of providing transient protection by failing when hit with a burst of transient energy.

A number of factors can cause damage to electronic circuitry—ESD, lightning strikes, inductive surges coupling across traces, ac line surges, and short circuits. Historically, protection has been a system-level consideration. Shielded enclosures took care of ESD problems. Signal lines were guarded as they entered the enclosure, power supplies protected against line surges, and fuses should have handled short-circuit conditions.

There was a time when primary protection schemes were able to handle the task at hand because system operating speeds weren't so fast and pc boards were lightly populated. Therefore, protection problems weren't too tough. Today, system-level-only protection schemes are really not adequate—there's a definite need for secondary board-level circuit protection. Boards containing surface-mount components tend to be rather heavily populated, making them expensive to fabricate. Damage to a single component can become a very expensive proposition.

Military electronics is another area where board-level protection is paramount. Military gear must function in very harsh environments rife with damage-causing factors, like shock and vibration. Portability—a fact of life with much military electronics gear—also increases the chances for ESD problems.

An additional factor that increases the need for board-level protection schemes is that today many high-speed, high-functionality components use submicron



A problem with a load motor can cause transistor drives for rear wash-wipe systems to overheat. Polyswitch devices from Raychem provide resettable protection for the transistors so intermittent faults won't cause permanent damage.

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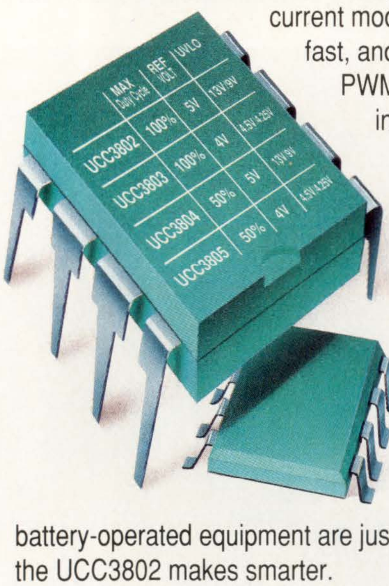

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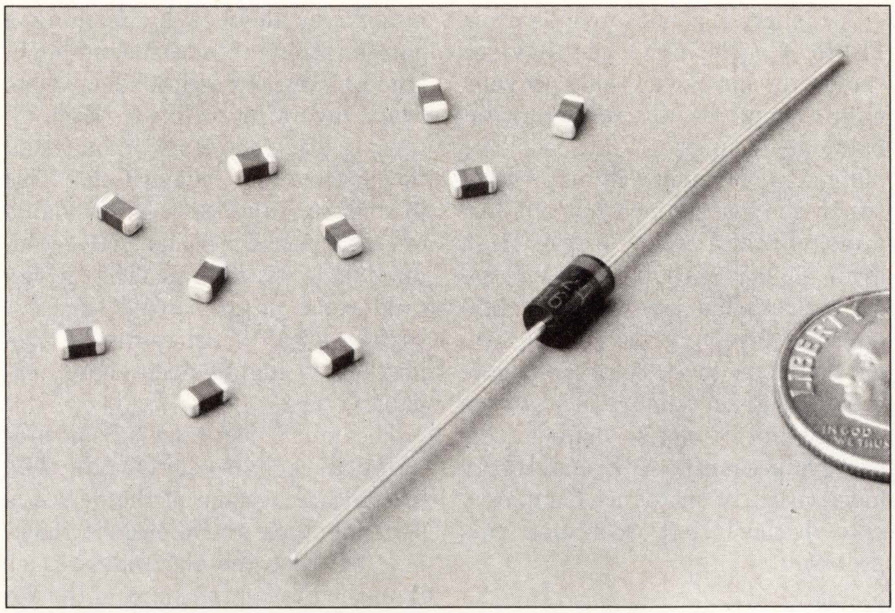
BOARD-LEVEL PROTECTIVE DEVICES

fabrication technologies. As a result, these components are inherently more susceptible to damage caused by electrical stresses. In addition, increased chip-trace-density combines with the high speed to increase inductive-coupling problems.

A number of board-mountable, transient-suppression devices are available today, the most common of which are varistors and sidacs (bilateral trigger devices) for overvoltage protection and thermistors and relay-based devices for overcurrent protection.

You can find two types of varistors: silicon and metal oxide. Silicon TVSs (transient voltage suppressors) are available from Motorola and General Semiconductor Industries (**Table 1**). The silicon TVS is characterized by a fast response time (subnanosecond) and a high surge-handling capability. The silicon TVS has V-I characteristics that are similar to those of other silicon pn-junction devices.

Unlike most diodes, however, silicon TVSs are built with large area junctions. They have a low dynamic impedance in the avalanche mode, which provides the low clamping voltages necessary for protection of semiconductor-based electronics. On the plus side, silicon TVSs are small, have no practical wear-out limitation, and feature a broad voltage spectrum. From a negative standpoint, the silicon TVSs have high capacitance values and a relatively low 1-shot current capability.



Compatible with automated assembly equipment, ML Series TVS devices from Harris are rated for peak current levels ranging to 2000A. They feature a multilayer construction that distributes heat evenly throughout the device to minimize peak temperatures.

The second TVS type available is the metal oxide varistor (MOV), which derives its electrical behavior from the semiconducting properties of zinc oxide (ZnO). Philips, World Products, and MCG Electronics make MOVs. The companies produce them by blending fine particles of ZnO, various other metal oxides, and a binder into a powder. This powder is then compacted into a disk shape and sintered until cured.

Many MOVs physically resemble ceramic disk capacitors, but some devices are available in tubular packages. Electrically, MOV material can produce nonlinear semiconductive action that is inherently bidirectional. MOVs can clamp high surge voltages, withstand high-surge current and energy, respond rapidly, and have reliably provided ac power protection over the years. On the negative side, MOVs have high capacitance, they are not rated for continuous power, they are somewhat bulky, and you must current-derate them when handling multiple pulses.

As the numbers in **Table 1** illustrate, today's TVS devices have a lot to offer. Given the clamping voltage and surge-current handling capabilities listed, the devices will handle a spectrum of applications. Response times are all in the nanosecond range and operating ranges are more than sufficient for both commercial and military applications.

Table 1—Representative transient-voltage-suppressor (TVS) parameters

Manufacturer	Model	Type	Clamping voltage (V)	Surge current (A)	Response time (sec)	Operating range (°C)	Price
General Semiconductor	SMC Series	Silicon	5 to 170	200	1×10^{-9}	−55 to +150	From $0.52 (5000)
MCG Electronics	DP-10, -20, -30, -33, -35	Silicon	±11 to ±260	120	1×10^{-9}	−55 to +85	From $58
Motorola	MR2535L	Silicon	24 to 32	110	1×10^{-6}	−65 to +175	$3 (1000)
Philips Components	2322-592, 2322-593	MOV	14 to 615	100 to 1200	20×10^{-9}	−55 to +80	From $0.15 (1000)
World Products	Super S	MOV	205 to 1100	9000	15×10^{-9}	−55 to +85	$0.07 to $0.30 (10,000)

BOARD-LEVEL PROTECTIVE DEVICES

Although it's not obvious from **Table 1's** listings, the devices shown do have one thing in common—they are all single grain-boundary (junction) devices. The number of boundary interfaces between conducting electrodes determines breakdown voltage. High grain counts satisfy high-voltage applications but low-voltage breakdowns need low grain counts. Single-boundary processing can handle the high grain requirements quite readily, but it's not as viable for the low grain counts. AVX and Harris have recently introduced suppression devices that overcome this problem.

Improving performance

The multilayer TVS devices in the ML Series (Harris Corp) and Transguard Series (AVX Corp) are compact, surface-mountable chips that are voltage dependent, nonlinear, and bidirectional. They have an electrical behavior similar to that of back-to-back diodes—they are fully symmetrical, offering protection in both forward and reverse directions.

The manufacturer constructs the multilayer devices by forming a combination of alternating electrode plates and semiconductive ceramic layers into a block. Each alternate electrode layer is connected to opposite end terminations. This formation enhances the available cross-sectional area for active conduction of transients. The design produces a large increase in active surface area, which results in proportionally higher peak energy capability.

The multilayer construction provides a second advantage. The breakdown voltage of the device is dependent on the dielectric thickness between the electrodes rather than the overall thickness of the device. Vendors can offer a variety of breakdown voltage ratings simply by varying the dielectric thickness.

The Transguard units from AVX have a current capability of 150 to 300A. They have a response time of 1 nsec max and they are available in a variety of surface-mount packages—0805, 1206, 1210, and axial-lead. These low-voltage devices have a circuit-operation capability ranging to 60 working volts. Clamping voltage figures range from 15.5 to 30V and transient energy figures cover a 0.3 to 1.2J spectrum. Transguard suppressor prices start at $0.45 (1000).

The V18MLA Series multilayer TVSs from Harris are aimed at automotive applications. The units are rated for peak currents ranging to 2000A. The devices are specified for voltage ranging to 18V and they have a jump-start overvoltage capability of 24.5V.

V18MLA suppressors are available in 1206-, 1210-, 1812-, and 2220-size packages. Units in the series will accommodate the complete range of automotive transient conditions, from worst-case alternator load dumps to secondary effects such as ignition system transients and ESD. Prices start at $0.46 (1000).

Meet the new kid on the block

Another type of unit on the market offering some pretty impressive performance is the sidac. The sidac is a bilateral trigger device designed for high-energy applications where other trigger devices are unable to function without the aid of

For more information . . .

For more information on the board-level protection products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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FAX (814) 834-1556
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Myrtle Beach, SC 29577
(803) 448-9411
FAX (803) 448-1943
Circle No. 701

General Semiconductor
2001 W Tenth Pl
Tempe, AZ 85281
(602) 731-3221
FAX (602) 966-6396
Circle No. 701

Harris Corp
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Somerville, NJ 08876
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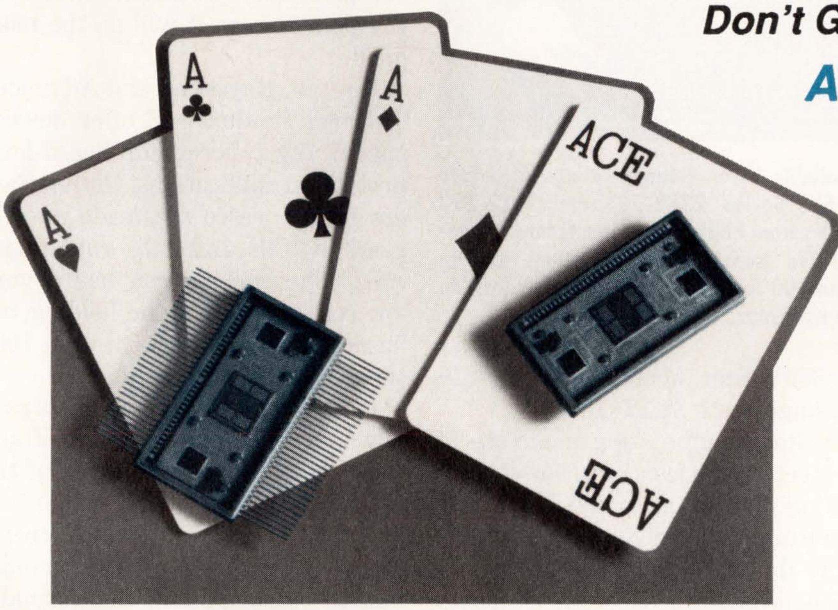

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For additional information and product literature, call Mike Glass at (516) 567-5600 extension 7545.❑

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BOARD-LEVEL PROTECTIVE DEVICES

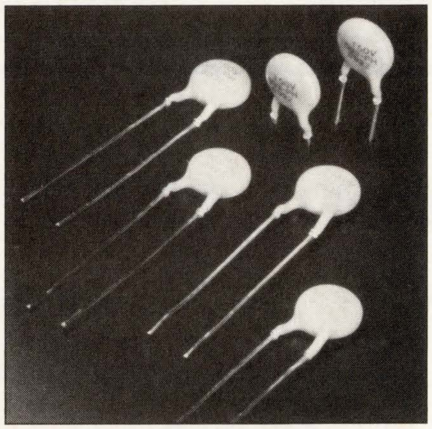
additional power-boosting components. Being a bilateral device, the sidac will switch from a blocking state to a conducting state when the applied voltage of either polarity exceeds the break over voltage. As in other trigger devices, the sidac switches through a negative resistance region to the low-voltage on-state and the unit will remain on until the main terminal current is interrupted or drops below the holding current rating.

In operation, the sidac normally connects between the high side of the circuit being protected and ground. As long as the monitored voltage remains below the specified value, the sidac presents a high off-state impedance. If the monitored voltage exceeds the specified clamping-voltage level, the sidac starts clamping in 1 nsec or less.

Sidacs are as fast as other currently used protection devices, and they can respond without a voltage overshoot. The sidac offers a lower impedance than a zener diode during conduction and it can handle higher currents.

Motorola and Teccor Electronics both offer sidac devices. Motorola offers two families of devices. MKP9V units—\$0.74 to \$1.80 (1000)—have an on-state current rating of 0.9A rms and break over voltages ranging from 120 to 270V. Dynamic holding-current requirements equal only 100 mA. Units in the MK1V Series—\$1.04 to \$3.15 (500)—feature an on-state rms current rating of 1A and are available with break-over-voltage levels of 115, 125, and 135V. Dynamic holding current for these devices is also equal to 100 mA.

The P Series line of sidacs from Teccor Electronics features more than 30 units covering a break-over-voltage range of 60 to 660V. Surge-current ratings of 150 to 500A are available. Clamping speed is specified at 1 nsec and holding-current values range from 150 to 750 mA.



Available with voltage ratings of 14 to 615V, Series 2322-592 and 2322-593 MOVs from Philips Components have nonrepetitive transient-current ratings ranging from 100 to 1200A and will respond within 20 nsec max.

A 380V unit housed in a TO-220 package costs \$2.32 (100).

Voltage suppression is one use of protective devices, another is providing protection against high temperatures caused by excessive current flow. The task of protecting pc boards from excessive currents is gaining in importance as the boards continue to decrease in size while component packing densities increase. Solid-state devices and pc-board traces are particularly susceptible to current-related damage. A number of devices are available that provide the needed protection, but some of these options are devices originally intended for primary protection at the system level. Such devices may not be the best solution for providing secondary protection at the board level.

Secondary (board-level) protection differs from primary (system-level) protection in several ways. First, pc boards are basically dc powered, so you can tailor protection devices for dc. Inrush current, which can cause nuisance tripping problems, is not a major concern at the board level.

Energy let-through is a critical parameter with board-level protection devices because of component and trace sensitivity. Energy let-through is directly related to the trip speed of the protective device. Finally, the task of resetting or replacing protection devices must not dominate system design. A remote or auto-reset capability lets designers place the protection device at the point where it will do the most good.

Inresco, Raychem, and Advanced Thermal Products all offer devices specifically tailored for board-level protection applications. Circuit Savers from Inresco are made up of a reed switch and two concentric coils. The sensing coil has a very low resistance, and the holding coil has a resistance that is at least 1000 times that of the sensing coil.

In normal operation, the current flows through the sensing coil and the normally closed contacts of the reed switch to the load. When the current exceeds the trip current, the sensing coil generates enough flux to start opening the normally closed lead; this action switches the holding coil into the circuit to immediately protect the load. The flux generated by the holding coil finally completes the transfer of the contacts to the normally open position and shunts power completely around the load. When the current level falls to 25% of rated current, the circuit saver will automatically reset itself.

Current ratings for the circuit savers range from 50 mA to 1A, and voltage figures span from 5 to 30V. Trip time for a 1A unit equals 40 μsec for a 400% overload and let-through energy measures 0.0009 A^2sec. Prices range from \$1.52 to \$3.27 (1000).

Raychem and Advanced Thermal Products both offer positive temperature coefficient thermistors for board-level protection service. Polyswitch devices from Raychem perform their protective duties by rapidly increasing their resistance

BOARD-LEVEL PROTECTIVE DEVICES

in response to excessive currents. When the current flowing through the polyswitch is within its maximum rating, the unit's base resistance is very low. If the current rises above the rated value, polyswitch resistance rises abruptly and decreases the current level until a thermal-equilibrium state is achieved.

Depending on the polyswitch in question and the amount of current flow, the trip time can be as short as 0.1 sec. Once power is removed from the protected circuit, the polyswitch device's resistance begins to drop towards the normal base value. This in essence resets the device so that normal operation can begin once the fault is corrected and the power is reapplied.

Raychem currently offers six families of leaded polyswitches encompassing more than 80 individual devices. In addition, surface-mount polyswitch protectors are available with ratings ranging from 300 mA at 60V to 1.5A at 30V. The surface-mount units are housed in packages ranging in size from 0.3×0.21 to 0.34×0.26 in. Prices range from $0.25 to $1.

Advanced Thermal Products' line of overcurrent protective devices use ceramic thermistors as the temperature-monitoring element. The line includes devices with maximum voltage ratings of 15, 50, 132, 265, and 400V. Minimum must-switch current ratings (value at which the unit must switch into the high resistance state) range from 0.1 to 2.31A. Switching speeds of 100 μsec are available. Prices, depending on quantity and device size, range from $0.20 to $0.80. EDN

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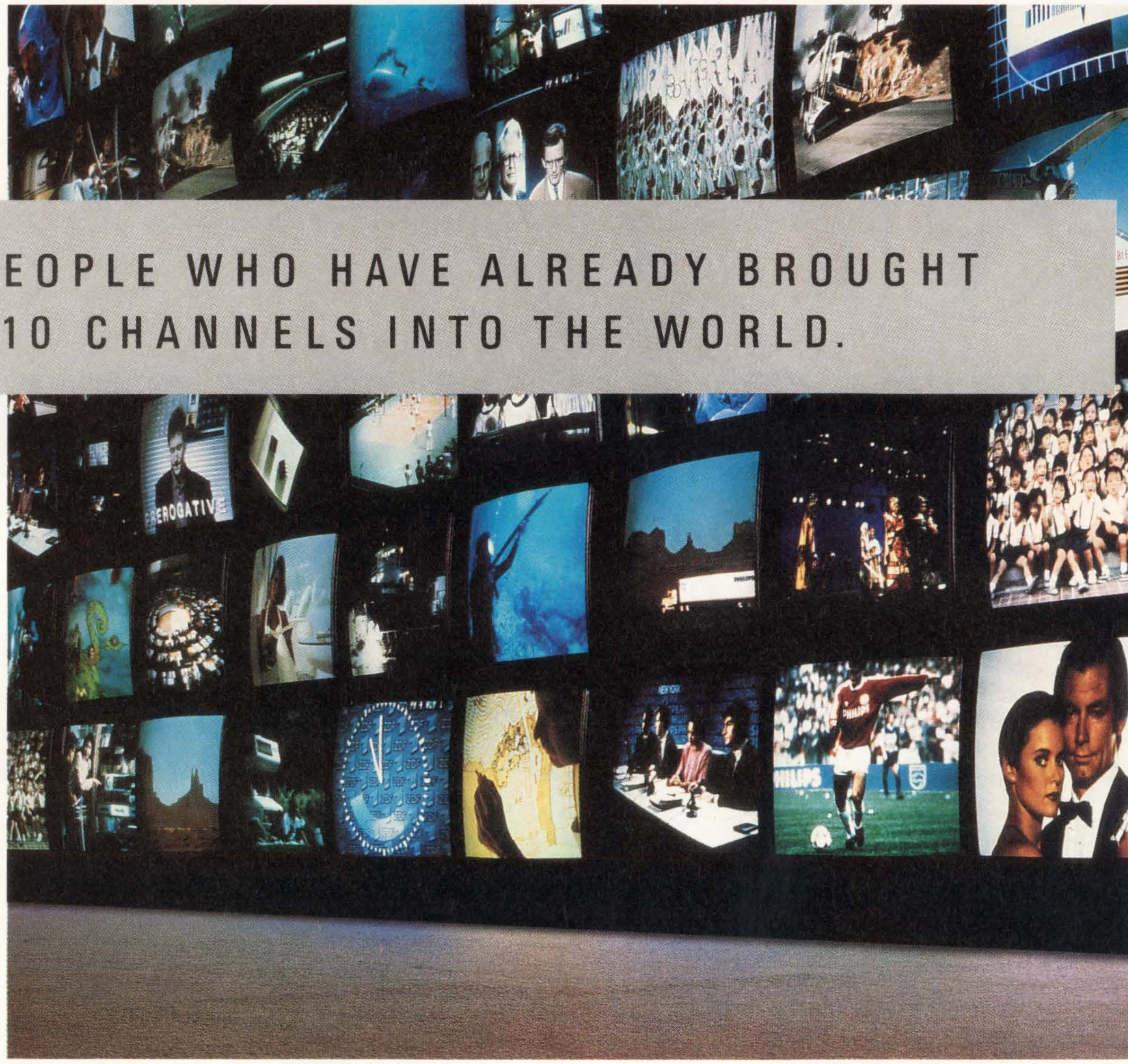

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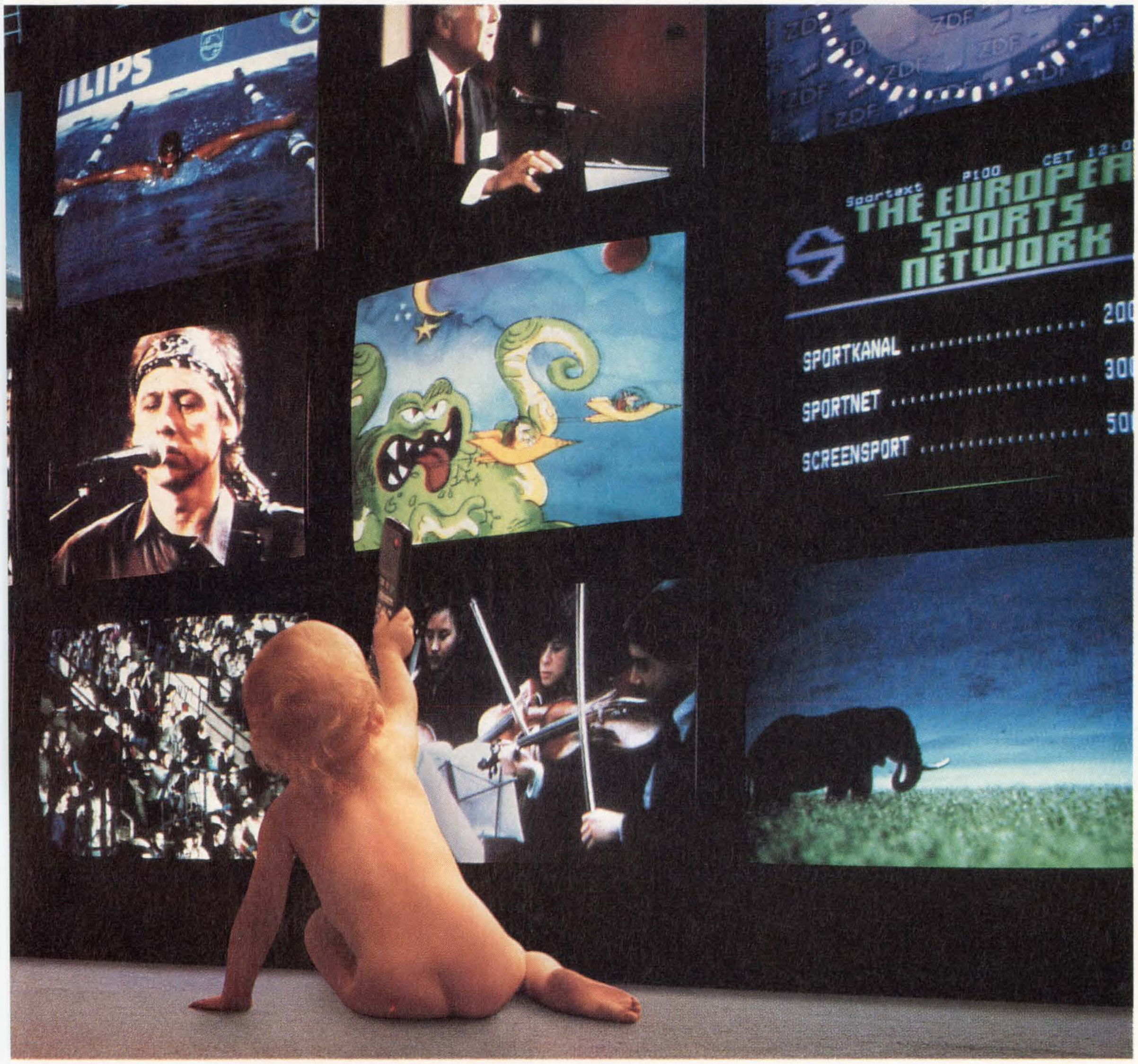

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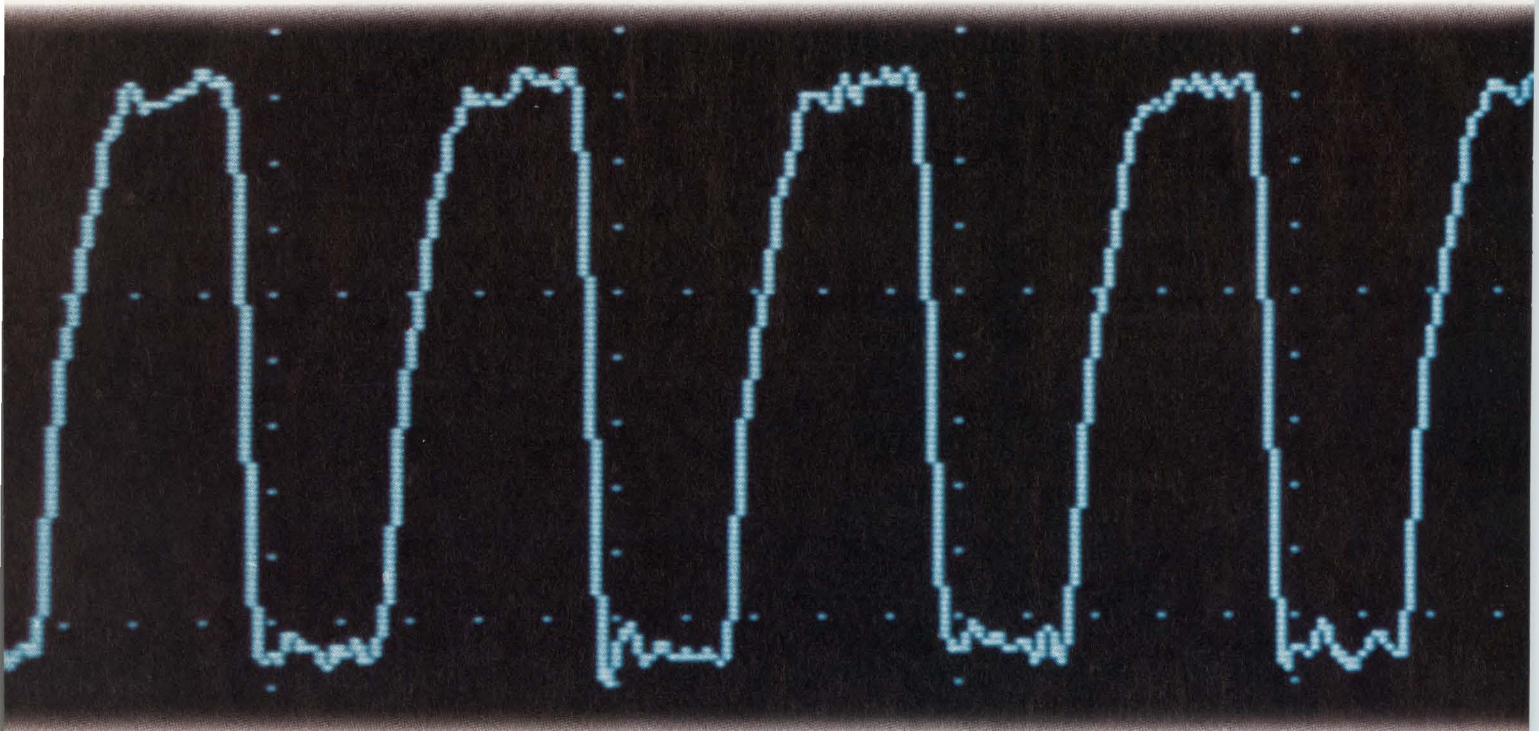
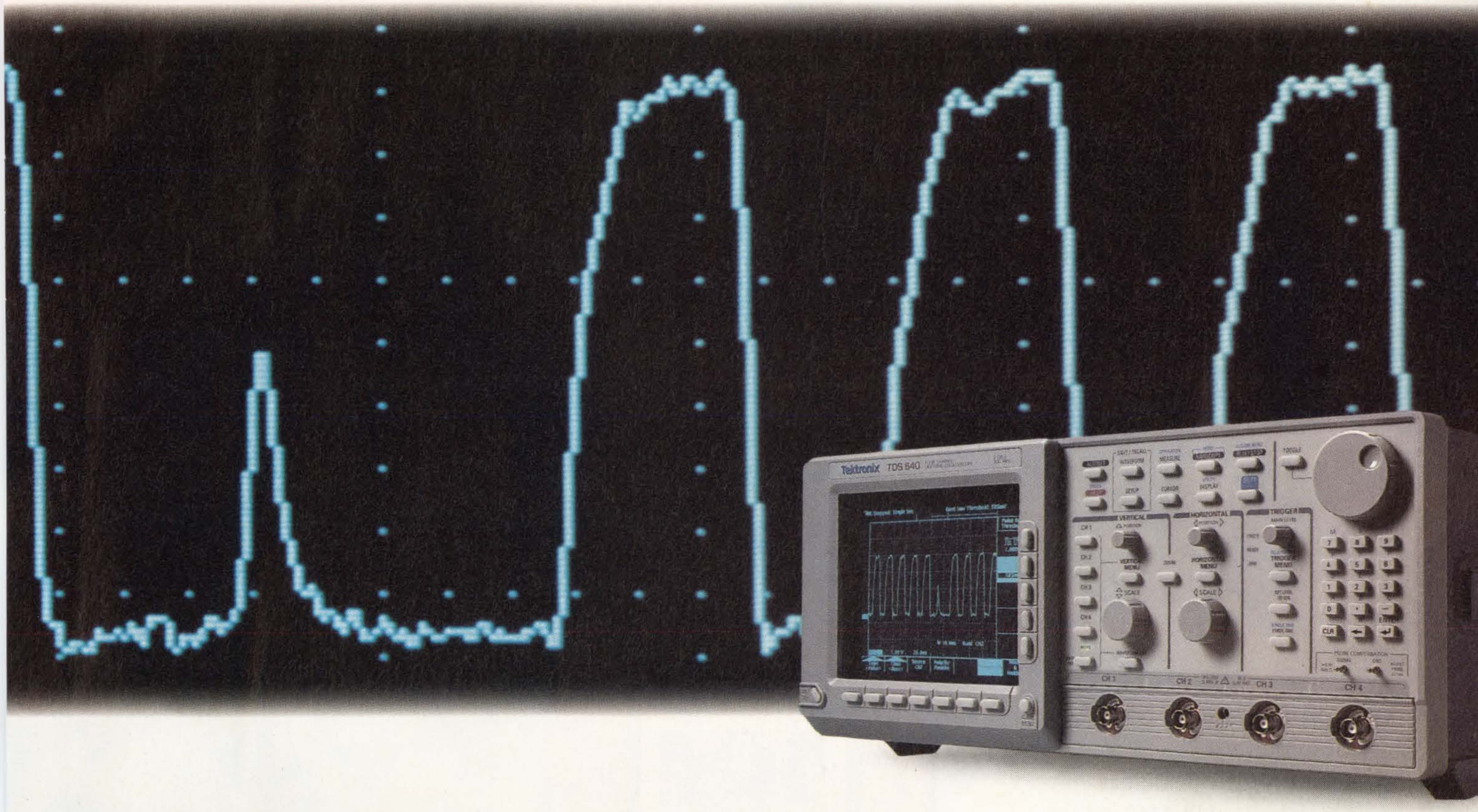


THE LITTLE RUNT.



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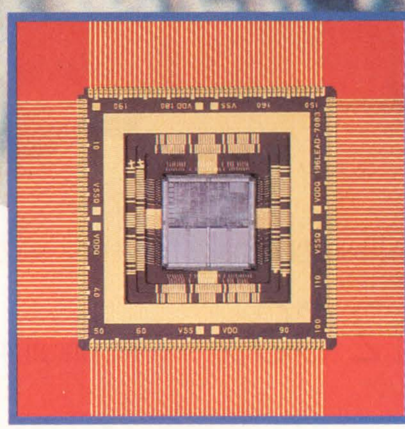

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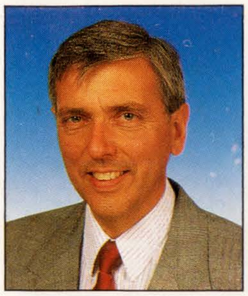
In-circuit programming instruments infiltrate commercial applications

BRIAN KERRIDGE, Technical Editor



Soldering-in EPROMs and EEPROMs simplifies manufacture and enhances reliability but complicates programming. Commercial in-circuit programming instruments overcome these complications, but require customization and a lot of forethought.

A few commercial in-circuit programming (ICP) instruments answer the growing need to program EPROMs and PLDs *after* pc-board assembly. In contrast with early forms of ICP, which were virtually device-specific, today's ICP instruments offer comprehensive and user-oriented facilities similar to those you expect to find in conventional chip-level programmers. **Table 1** presents an overview of these ICP instruments and their principal characteristics. Prices range from $3500 for a bench model suitable for programming a single target assembly to $25,000 for a ruggedized portable version that programs multiple assemblies.

ICP remains principally aerospace and military driven because these organizations mandate that all components must be soldered-in to satisfy reliability and ruggedizing requirements. However, ICP is showing signs of migrating to the commercial sector, particularly as designers turn to surface-mount and thin-small-outline-package (TSOP) programmable devices for medical and telecomm products. In commercial applications, the motivation to employ ICP includes reliability as well, but also results from acute difficulties in handling small-package parts in manufacture. **Refs 1** and 2 cover the pros and cons of ICP in more detail.

When you're selecting an ICP instrument, you should be just as concerned with selecting a vendor to support you as with the specifications of the programmer itself. ICP still involves a degree of customization and, although most users believe they can handle the work themselves, vendors' experience shows that ICP newcomers still need their support. In fact, many seasoned ICP users continue to rely totally upon their vendor for customizing each new design.

Several ICP instruments have developed from vendors' existing conventional programmer designs. The main difference is that dedicated edge-connector sockets on the ICP instruments replace the usual EPROM zero-insertion-force (ZIF) sockets. The dedicated edge connectors provide many more contacts, which ICP needs for it to take control of all the hardware on your target assembly.

Hardware adapters, either open pc boards or enclosed units, mate with connectors along the right-hand side of Elan Digital Systems' ICP-5 portable benchtop programmer. The ICP-5 provides ZIF sockets to accept source data from programmed devices as an alternative to downloaded files.

In principle, ICP is simply a matter of carrying signals, similar to those used for conventional chip-level programming, to similar memory parts permanently soldered onto a pc board. In practice, the problem is channeling those signals around other devices on the same pc board without compromising the programming signals or damaging the other unsuspecting nonprogrammable parts.

To make ICP work, you need more than just the ICP instrument. You need a hardware adapter to link your target assembly to the programmer, and a software configuration file to take control of all hardware and programming of your assembly. In addition, to enable this level of control, it's likely you'll have to build extra hardware into your target assembly, or, at the very least, run additional traces on your pc board. The **box** "Guidelines for designing-in ICP" answers questions on what you need to do to prepare a design for ICP.

Even accepting that you can install the necessary features on

Table 1—Representative in-circuit programmers

Vendor	Model	Type	Number of address lines	Number of data lines	Number of TTL control lines	Max number of target assemblies accepted[2,3]	Vpp[1] Number of lines	Vpp[1] Rating per line
Data I/O	Boardsite 4100	Benchtop	32	32	24	4	2	0 to 25V, 2A
	Boardsite 4400	Benchtop	32	32	24	32	2	0 to 25V, 2A
	Boardsite 5100	Ruggedized portable	32	32	24	8	2	0 to 25V, 2A
Elan Digital Systems	5-ICP	Benchtop portable	23	16	16	2	3	0 to 25V, 0.8A
	5-ICP/ UMI	Benchtop portable	23	32	16	4	3	0 to 25V, 0.8A
Logical Devices	Unipro-ICP	Benchtop	20	16	40	8	4	0 to 27V, 2A
Oliver Advanced Engineering	Omni	Benchtop	64	64	64	8	4	±38V, 10A
Stag Programmers	ICP 9000-1	Benchtop	64	32	8	4	4	0 to 25V, 1A
	ICP 9000-2	Benchtop	64	32	8	4	4	0 to 25V, 1A
	ICP 9500	Benchtop	128	64	16	8	8	0 to 25V, 1A
Sunrise Electronics	T-2000	Benchtop	24	16	8	1	1	0 to 30V, 3A
	T-4000	Benchtop	24	16	24	64	3	0 to 30V, 3A
	T-5000	Benchtop portable	24	16	24	64	3	0 to 30V, 3A
	T-6000	Ruggedized portable	24	16	8	8	1	0 to 30V, 3A
	T-8000	Benchtop	24	16	24	64	3	0 to 30V, 5A

Notes: 1. V_{PP} =programming supply, V_{CC} =power supply.
2. Limitation depends on bus allocation per target assembly, V_{CC} current rating, or size constraint. (It can be faster overall to program and verify fewer target assemblies simultaneously).
3. Assumes isolation between target assemblies.
4. Internal 68000 processor running OS-9.

your target assembly, other questions arise on how to proceed. The **box** "Common questions from ICP first-timers" supplies some of the answers.

The most important ICP advice is to think about the consequences of ICP well before you intend to apply it to your design. ICP instrument vendors echo this point over and over, but still it seems some designers ignore the message. The difficulties and costs of back-tracking on an existing design to build-in ICP multiply excruciatingly over the relative ease of designing-in beforehand. Even on a simple target assembly with only memory parts, you need to run multiple traces to some pins, and you generally need to thicken-up traces along principal supply lines. So at the very least, you need a new pc-board issue. If you simply cannot change a pc-board layout, Logical Devices offers the option of using a bed-of-nails connection system with their programmers, but this is not a preferred route.

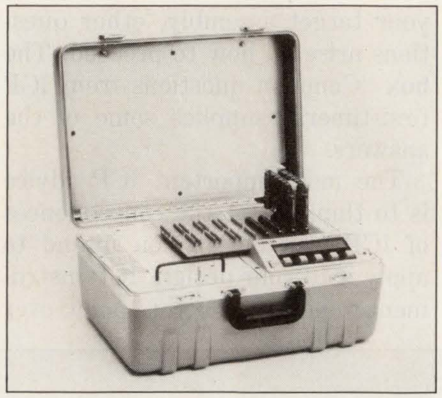
As part of their ICP applications-

V_{CC}[1]		Control			Interfaces					
Number of lines	Rating per line	External PC	Internal PC	Local panel keys	RS-232C	Parallel	SCSI	IEEE-488	Base price	Comments
2	0 to 7V, 6A	✓			✓	✓			$14,000	
2	0 to 7V, 6A	✓			✓	✓			$20,000	
2	0 to 7V, 6A		✓	✓	✓	✓			$20,000	1-Mbyte RAM expandable to 8 Mbytes; options: 25-MHz 386 CPU, 3.5-in. floppy drive, water-tight case, UV-eraser mounted in lid
2	0 to 8V, 2.4A			✓	✓	✓			$8975	Two master ZIF sockets to source data from 24-, 28-, 32-, or 40-pin devices
3	0 to 8V, 2.4A			✓	✓	✓			$9995	Two master ZIF sockets to source data from 24-, 28-, 32-, or 40-pin devices
4	0 to 27V, 5A			✓	✓				$8000	Bed-of-nails adapter
4	±38V, 10A	✓		✓	✓	✓		option	$14,995	ESD damage screening, parametric testing
1	0 to 7V, 8A		✓[1]	✓	✓	✓			$13,000	5.25-in. floppy drive, ARINC compatible, 3-year software upgrade
1	0 to 7V, 8A		✓[1]	✓	✓	✓	✓	✓	$16,000	5.25- and 3.5-in. floppy drives, 40-Mbyte hard disk, ARINC compatible, 3-year software upgrade
2	0 to 7V, 8A		✓[1]	✓	✓	✓	✓	✓	$21,000	5.25- and 3.5-in. floppy drives, 40-Mbyte hard disk, ARINC compatible, 3-year software upgrade
2	0 to 7V, 1.5A	✓							$3495	
3	0 to 7V, 7.5A	✓							$13,950	
3	0 to 7V, 7.5A		✓						$19,950	3.5-in. floppy drive, 120-Mbyte hard disk
2	0 to 7V, 7A		✓		option	option			$19,950	3.5-in. floppy drive
3	0 to 7V, 10A	✓			✓	option	✓	option	$45,000	5.25- or 3.5-in. floppy drive, 20-Mbyte hard disk

IN-CIRCUIT PROGRAMMERS

support service, Data I/O, Elan, and Stag issue a questionnaire covering design details of your target assembly. Stag's version contains six pages of questions the company likes to have answered before designing your software-configuration file and hardware adapter. In addition, all vendors like to receive copies of your target assembly's schematics before proceeding. The extent of this detail is a good indicator of how much forethought you must apply before embarking on ICP. Depending on the complexity of your target assembly, you should expect to pay from $2500 for a vendor to provide a configuration file and hardware adapter.

Although vendors provide a turnkey ICP service, it's still possible to go it alone. A major part of the work consists of developing a software configuration file to drive your assembly. Vendors include a software utility with an ICP instrument to perform this task. You create a source file by entering mostly text information about your target assembly. A compiler feature reformats the file to machine code in preparation for driving your assembly. The ease with which you can operate these tools is clearly an important factor. Data I/O offers you a taste of its software by issuing a PC demo disk (**Ref 3**) that takes you through the data-entry procedure.



Data I/O's 5100 ruggedized portable model suits in-field ICP applications. You can control the instrument using five "soft" keys and an LCD, or by plugging in an external PC monitor and keyboard. The unit includes a removable 44-Mbyte hard-disk cartridge for updating and security.

Guidelines for designing-in ICP

Before you can use ICP, you need to build some basic but essential features into your pc-board assembly. If your pc board already has an I/O connector with unused pins, the chances are that this connector will be a suitable access point for ICP. If not, then you will have to design-in a dedicated ICP connector.

The list of recommendations below refers mainly to designs using UV-erasable, one-time-programmable, or flash EPROMs.

- Run separate traces from EPROM pins V_{cc} (5V supply) and V_{pp} (programming supply) to the ICP connector. V_{pp} is at 5V for read/verify mode, but may be up to 25V for programming.
- Build enough copper into the V_{pp} and V_{cc} traces to handle currents as high as 50 mA required during programming. A good ground plane is also essential to minimize voltage overshoot—device vendors often specify voltages more strictly for programming than for reading.
- Decouple both V_{cc} and V_{pp} close to EPROMs using 0.01- to 0.1-μF ceramic capacitors.
- Ideally, separate V_{cc} from the pc board's main 5V supply. Most EPROMs require V_{cc} at 6V or more during programming (eg, Intel's "Quick-pulse" algorithm specifies 6.25V). This voltage exceeds the maximum V_{cc} level of standard LS/HC logic, which can be as low as 5.25V. Even if you do separate V_{cc} and apply 6V, EPROM data outputs will then switch up to 6V. So check the likelihood of damage to other devices on the data bus.
- Flash EPROMs require 5V on V_{cc} for programming or erasing, so V_{cc} separation is unnecessary.
- Run all data and address bus lines from EPROMs to the ICP connector. Also, run EPROM control pins CE (chip enable), OE (output enable), and PGM (program) to the ICP connector.
- If your EPROMs output via a data-bus buffer, you will need to install a bidirectional version to allow for programming as well as read/verify mode. ICP requires control of the DIR (direction) line of this buffer. Normally, you can control DIR by connecting it to OE on the EPROM.
- Don't indiscriminately mix EPROMs of the same generic type in your design. Some nominally equivalent parts require different programming algorithms (eg, 27C020s from AMD (Sunnyvale, CA) and Texas Instruments (Dallas, TX) use Flashrite and Snap algorithms, respectively).
- When you intend to use ICP with EPLDs' or μPs' on-chip programmable memory, it's likely you'll need to add 3-state buffers to isolate memory from the remainder of the circuit in the programming mode. At this stage, it's best to seek advice from ICP specialists.

Acknowledgment

Thanks go to Philip Townley, ICP applications engineer at Elan Digital Systems for helping with these design guidelines.

ICP is not necessarily a programming panacea. For plenty of applications, EPROMs in sockets and a \$1000 PROM programmer remains a more sensible arrangement. Often, pc boards are not readily removable from an instrument or system; for example, when the system in not based on a backplane construction. In this case, replacing a few socketed chips is vastly easier and faster than wrestling-out a whole pc board. Although quality engineers generally despise general-purpose IC sockets, they can't complain if you use high-quality sockets.

If you're using ICP, and your target assembly uses UV-erasable EPROMs, you'll need to get an outsize UV eraser to take whole pc-

Common questions from ICP first-timers

Newcomers to ICP tend to raise certain questions. These questions—and their answers—are as follows:

Are the following pc-board assembly and design characteristics compatible with ICP?

	Compatible	Incompatible
Contains memory only	*	
Contains μPs	*	
Contains address decoders	*	
Contains other TTL and VLSI parts	*	
Uses multiplexed address/data	*	
Uses dedicated socket for ICP	*	
Includes multiple edge connectors	*	
No access to EPROM V_{PP} pin		*
EPROM OE pin tied low		*

What if I can't raise an EPROM V_{cc} pin above 5V or can't apply a programming pulse to the correct pin?

Then you can't use a memory-IC vendor-approved programming algorithm. Alternative general algorithms can do the job, but your choice will depend on the specific memory device and pc-board layout.

How easy is it for my manufacturing and customer-service operators to use ICP?

You can operate most ICP instruments locally using a few basic keys and a simple LCD, just as you would a conventional programmer. Remote operation is also possible if you link the programmer to a PC or a VAX mainframe.

How can I configure an ICP instrument for a specific target assembly?

You need an assembly-configuration software file, and a custom-built hardware adapter to connect your target assembly to the programmer.

You develop a source file for the assembly configuration using an editor utility program, which runs on a PC or on the programmer itself. The same program compiles your source file to machine code for directly controlling and programming your target assembly.

Each time you operate ICP, you download the appropriate assembly-configuration file from an internal hard- or floppy-disk, or from a host computer via RS-232C.

How long does it take to develop an assembly-configuration file?

Depending on assembly complexity, it can take a few minutes or a few hours. Once you've entered the source file, compiling the file takes seconds or minutes depending on which programmer you use.

Programmer vendors offer a service to produce configuration files for you.

Can I gang-program assemblies?

Yes. But be sure to look for a programmer that isolates the connectors for each target assembly to prevent one failed assembly affecting the others. The following is a typical gang-programming arrangement:

Typical number of target assemblies

	Target-assembly data-bus width			
	8 bits	16 bits	32 bits	64 bits
General-purpose programmer	4	2	1	0
Top-end programmer	8	4	2	1

How long will it take to program?

The time varies according to which programmer you use, which algorithm you use, and the parameters of your target assembly. As an example, using an Intel Quick-pulse algorithm, and assuming one device per eight bits, the following times could apply:

Typical programming time in seconds
(including empty and verify check)

	Target-assembly data-bus width			
	8 bits	16 bits	32 bits	64 bits
One assembly	10.7	10.7	11.1	12.3
Two assemblies	15.1	15.1	15.5	Not available
Eight assemblies	29.1	60.4	62.0	Not available

Acknowledgment

Thanks go to Richard Hough, ICP specialist at Stag Programmers, for helping with the information in this box.

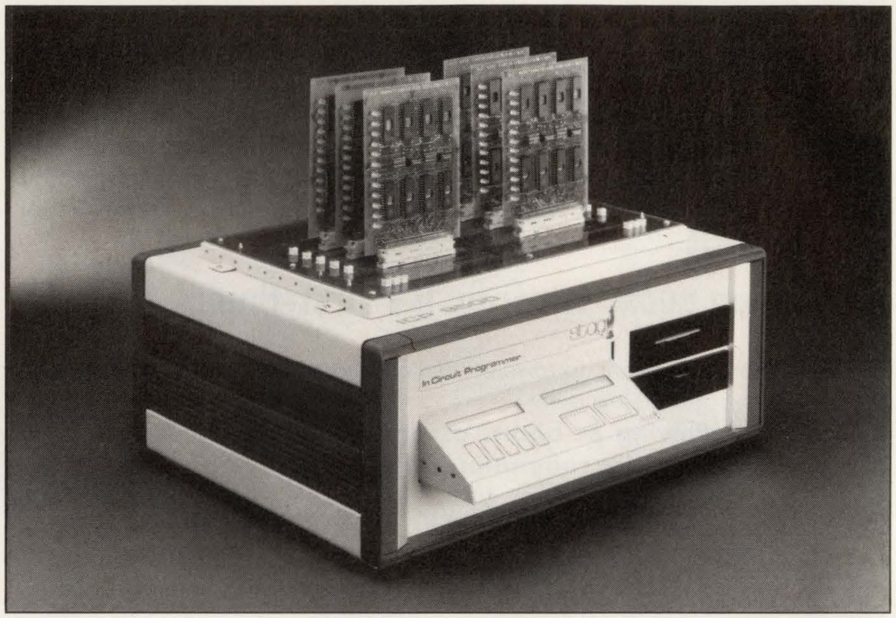
board assemblies. If your pc board is particularly large, and you can erase only one assembly at a time, the 20 minutes or so it takes creates a process bottleneck. Added to this inconvenience, you should anticipate spending as much as $10,000 for an eraser, rather than closer to $500 for a chip-size eraser.

Prefer approved algorithms

One of the headaches of the programming business, of conventional or ICP, is staying abreast of changes to programming algorithms. According to Mike Radovich, product manager with Data I/O, a programming algorithm for any device may change four to seven times over a typical 5-year life of the device. The primary reason for algorithm changes is process changes by the manufacturer.

Radovich adds that even where an algorithm is stable for a principal part, don't necessarily expect the algorithm for its recognized second-source equivalent to be identical. Simply having the same part made in a different foundry can mean you need to use a different programming algorithm. Knowing which algorithm you should be using at any time is where programmer vendors can help you out. Generally, vendors include a 1-year free software-upgrade service with the sale of a programmer. Thereafter, the service becomes chargeable at around $1500 per annum.

Where possible, programmer vendors strive to use the same programming algorithms for ICP as for discrete-chip programming. In most cases, if you adopt your programmer vendor's advice when laying out your pc board, then there's no problem in using a standard programming algorithm.



You can program as many as eight target assemblies simultaneously, and maintain isolation between assemblies, using Stag Programmers' ICP 9500. With an external terminal, you can use the internal 68000-based processing system to develop target assembly-configuration files. In your manufacturing plant, you have complete control of ICP using an integral keyboard and LCD.

For more information . . .

For more information on the programming products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

Data I/O Corp
10525 Willows Rd NE
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Redmond, WA 98073
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FAX (206) 882-1043
Circle No. 710
In UK:
Data I/O Ltd
660 Eskdale Rd, Winnersh
Wokingham RG11 5TS, UK
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Elan Digital Systems
2162 N Main St
Walnut Creek, CA 94596
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In UK:
Elan Digital Systems Ltd
Elan House, Little Park Farm Rd
Segensworth W
Fareham PO15 5SJ, UK
489-579799
FAX 489-577516
Circle No. 713

Logical Devices Inc
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Fort Lauderdale, FL 33309
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FAX (305) 974-8531
Circle No. 714

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In cases where it's not possible to install some of the recommended features, it becomes necessary to consider special ICP algorithms. As an example, if you can't run separate lines to V_{cc} pins, or you can't isolate all superfluous logic hanging on the data bus, then you won't be able to apply the 6V or greater that some standard programming algorithms specify. In this case, you'll have to use a special low-voltage algorithm (5V on V_{cc}), which consequently extends programming time.

Programmer vendors prefer not to employ special algorithms, although their experience proves such algorithms to be entirely reliable. Such algorithms are officially nonpreferred because, at present, no memory-IC vendor offers approved algorithms with V_{cc} set to 5V. Memory-IC vendors offer a service for approving alternative programming algorithms, but the level of service varies widely between vendors and depends on how significant you are as a customer.

If you use a nonapproved algorithm and subsequently discover programming errors, it's difficult to know who to blame except yourself. This potential predicament reinforces the valuable advice to build-in rather than back-in to ICP. EDN

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1. Clark, Barry M, "Improve reliability by rigging pc boards for in-circuit programming," *EDN*, April 9, 1992, pg 135.

2. Data I/O Corp, "Introduction to in-circuit programming."

3. Data I/O Corp, "Boardsite in-circuit programming system," demo disk.

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PORTABLE DATA CARRIERS

Small, rugged memories put data where it's needed

GARY LEGG, Senior Technical Editor

Cleverly packaged memory devices put data in places where a computer can't go. Some even contain an RF transponder for wireless access.

Portable data carriers—nonvolatile-memory devices that perform useful functions away from a computer, rather than inside one—are becoming much easier to use. They're small, they're rugged, and they come in handy shapes: everything from keys and tags to buttons and matchstick-sized cylinders (**Table 1**). Some even transfer data without wires.

Many data carriers now contain an RF transponder, which eliminates the need for electrical contact. With a reader/writer device—either a stationary or a hand-held unit—you can access the data in an RF data carrier from as far away as a meter or more.

Another type of carrier has a simple electrical interface that transfers data at the touch of a single-wire probe. Other carriers, notably key- and tag-shaped ones, plug into special receptacles.

The central feature of portable data carriers is, of course, portability. The smallest and most rugged of carriers can slip on a key ring, stick to an employee badge, or even be implanted under the skin of an animal. The devices are useful not only for transporting data, but, in many cases, for acquiring data. Memory cards (**Ref 1**) are larger data carriers that tend to find use with computers and instruments; smart cards (**Ref 2**) serve applications where a card shape isn't a detriment and where ruggedness isn't a primary requirement.

One of the fastest growing applications for portable data carriers is radio-frequency identification (RFID). An RF data carrier attaches to practically anything and contains identifying data that is readable (and often writeable) without physical contact. Most transponders in RF data carriers operate in the range of 125 to 135 kHz.

Coin-shaped data carriers from Dallas Semiconductor use only two electrical contacts to transfer data to and from their battery-backed SRAM. In the application shown here, an adhesive-backed data carrier is attached to an employee badge. Each carrier contains a readable, but unalterable, serial number that provides identification for access control.

Seeing great potential for RFID, Texas Instruments last year entered the market with a small, 64-bit, read-only RF memory device. The company now has a read/write version and expects to have products with greater memory capacity by the end of the year. Current devices are available in the form of a glass cylinder 4×30 mm (**Fig 1**).

To access data in a TI device, a reader unit or a reader/writer unit first sends a 50-msec, 134-kHz RF power burst via

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Abbott Electronics, Inc., 2727 S. La Cienega Blvd., Los Angeles, CA 90034-2643 • Telephone 310/ 202-8820 • Fax 310/ 836-1027 an antenna. The power burst charges a capacitor in the data carrier; the capacitor, in turn, provides power for a return data transmission. After a return transmission, the power capacitor discharges and the RF transponder resets.

Data communication takes about 20 msec, and a complete read cycle lasts about 120 msec. Write cycles take longer. All communication occurs via frequency-shift key (FSK) transmissions, with frequency transitions between 134.2 and 122.2 kHz.

Maximum read and write distances depend on several factors: the type of reader (stationary or handheld), type and size of antenna (gate or ferrite rod), transponder orientation with the antenna, and communication regulations of the country where the equipment is in use. Read distances can be as great as 2m; write distances are slightly less.

A new kind of memory will be making its debut in RFID products later this year. Racom Systems (Boulder, CO) is completing development of an RF device that contains ferroelectric RAM. Ferroelectric RAM (FRAM) is dual-mode memory that can operate either as nonvolatile RAM or as dynamic RAM (DRAM) that becomes nonvolatile on power-down. Ramtron Corp (Sydney, Australia and Colorado Springs, CO) developed FRAMs.

Memory keys from Datakey contain from 1 to 512 kbits of memory. Versions are available with serial or parallel access and with read/write or one-time-programmable memory.

According to Charlie Cushing, Racom's executive vice president and chief operating officer, a read/write FRAM will cost about the same as read-only devices using other technologies. Or, compared with other RF read/write devices, a FRAM will offer more memory capacity for a comparable price. Cushing expects that a 256-bit device will sell for $4 to $5 in quantities of 1000. By comparison, a 64-bit read/write device from TI costs $8 to $11.

The two companies' products are dissimilar in several respects, however. Racom's device will be available in packages similar to credit cards (but slightly thicker) and in glass cylinders. The cylinders will be 2 mm in diameter and 11 or 12 mm long—much smaller than the TI devices. However, read and write

Table 1—A sampling of small portable data carriers

Device type and characteristics	Memory configuration			Price (1000)	Manufacturer
	Type	Capacity (bits)	Access		
RF memory tag Memory and RF transponder in glass cylinder 30x4 mm in diameter. Operates on power received from an external transmitter and stored in an internal capacitor. Frequency of data transmissions is 134 kHz. Maximum read distance ranges from about 20 cm to about 2m. Write distance is slightly less.	Mask ROM[1]	64	Serial	$6 to $8	**Texas Instruments Inc** 24 Forest St, MS 20-27 Attleboro, MA 02703 (508) 699-3174 FAX (508) 699-3647 **Circle No. 719**
	Read/Write[2]	64	Serial	$8.40 to $11.20	
Touch memory button Factory-written, unique serial number and (usually) battery-backed static RAM in a stainless steel can. Simple 2-contact form allows data transfer at the touch of a probe. Stick-on and snap-in versions available. Some versions offer password protection.	Laser-written serial number	48	Serial	$1.59	**Dallas Semiconductor** 4401 S Beltwood Pkwy Dallas, TX 75244 (214) 450-0448 FAX (214) 450-0470 **Circle No. 720**
	Static RAM plus 48-bit serial number	1 to 4k +48	Serial	$3.50 to $6.81	
Memory key or token Static-resistant plastic molded around memory in the shape of a key or a tag. From 16 to 28 electrical contacts in key shaft, 16 in token. Insert-and-turn operation (key) or plug-in operation (token).	EEPROM	1 to 4k	Serial	$3.50 to $12	**Datakey Inc** 407 W Travelers Trail Burnsville, MN 55337 (800) 328-8828, (612) 890-6850 FAX (612) 890-2726 **Circle No. 721**
	EEPROM	64 to 256k	Parallel	$28 to $100	
	EPROM[3]	256 to 512k	Parallel	$15 to $19	
	Fuse link	26	Serial	$1.25	

Notes:
1. Each device is factory programmed with a unique ID number. Programming method not identified.
2. Manufacturer would not disclose memory type, citing competitive reasons.
3. Because memory chip is encapsulated without an erase window, the device is one-time programmable.

PORTABLE DATA CARRIERS

distances will also be much less—25 to 30 cm for a card and about half that for a cylinder.

Read distances can be as great as 15m with a new product from Dallas Semiconductor. (Under some conditions imposed by communications regulatory agencies, such as the FCC, the distance may be less.) The DS2569 touch/proximity chip is a variation of the company's Touch Memory line, which made its debut a year ago.

For read operations, the device receives RF transmissions at 132 kHz; it generates control signals for an external transmitter that responds at a frequency near 300 MHz. Writing to memory requires electrical contact. The device has 512 bits of battery-backed static RAM (SRAM) (216 of which are available for user applications) and 96 bits of ROM that is programmable during manufacture.

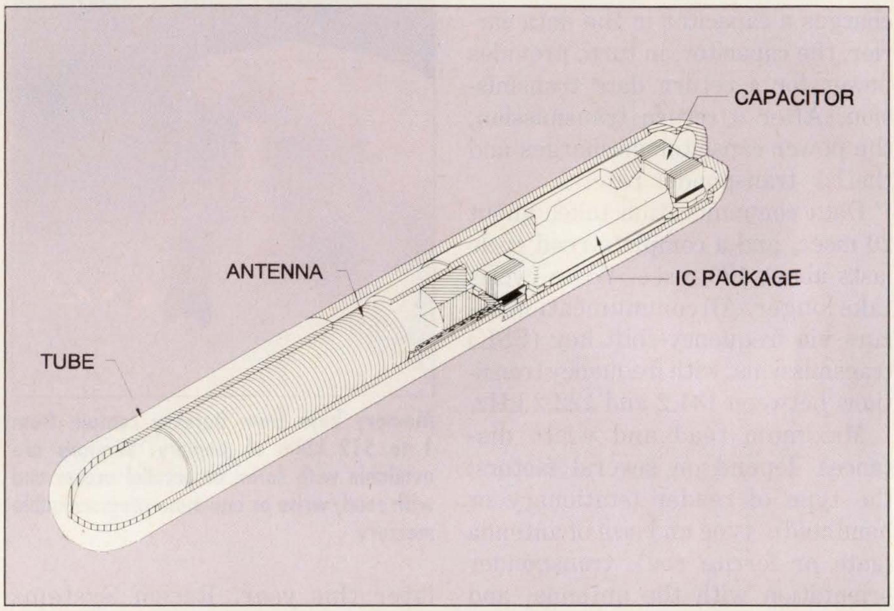


Fig 1—RF memory tags from Texas Instruments operate on power obtained by rectifying a 50-msec, 134-kHz power pulse received from an external transmitter. Stored in a capacitor, the power lets the tag reply with a transmission of its stored data.

An easy touch

Applications that don't require RF devices' "proximity" operation can use cheaper data carriers that rely on electrical contact for all data transfers. Touch Memory products are the easiest of this type to use; they implement a single-wire communication scheme that makes data transfer quick and virtually foolproof. The button-shaped, stainless steel can that holds each memory module has just two contacts—ground, which is on the can's base and sides, and data, which is on the can's lid. Internal circuitry guards against data corruption that might result from faulty or momentary contact (**Fig 2**).

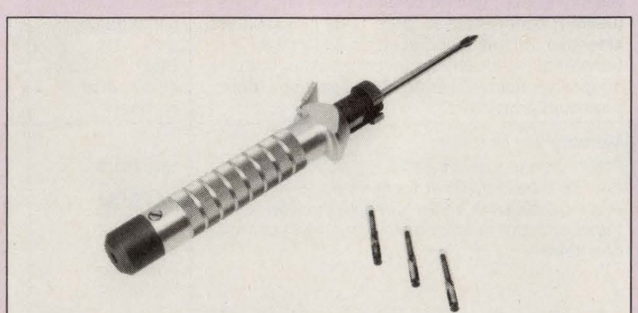
Touch Memory data carriers contain as much as 4096 bits of battery-backed SRAM; the lithium batteries that power the devices are good for ten years. The devices are available in adhesive-backed, stick-on versions or with snap-in receptacles. One receptacle is designed for use on a key chain.

Key-chain data carriers are also available with hefty memory capacities. Datakey, for example, sells memory keys with as much as 256 kbits of EEPROM or 512 kbits of

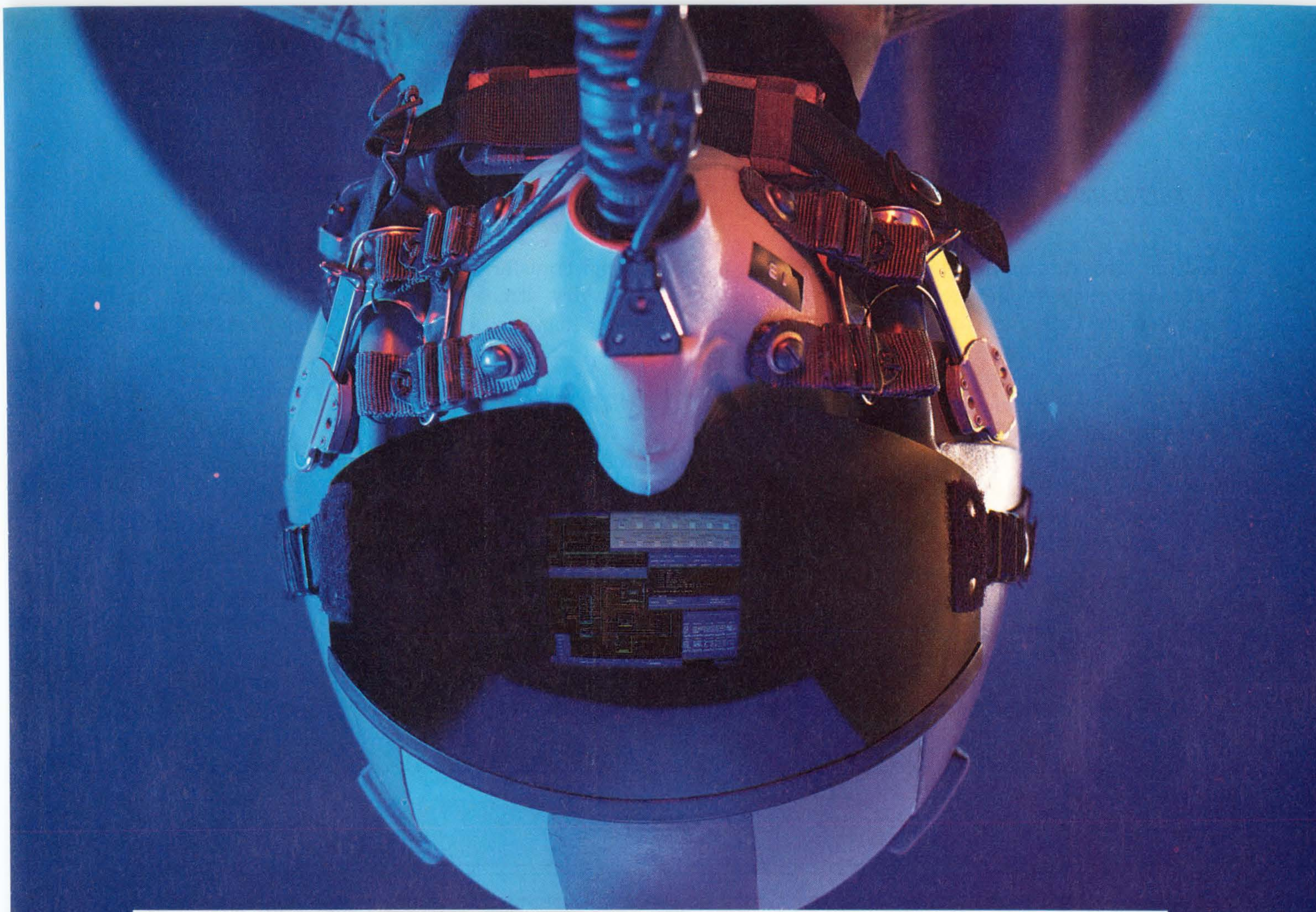
Memory tag bytes dog

Throughout Canada and in some US and European locations, memory devices are going to the dogs—literally. Animals unlucky enough to live in one of a few select cities are subject to having their metal ID tags augmented by electronic ones implanted in the neck.

The electronic tags, packaged in tiny, glass cylinders, are injected under the skin. Data stored in a tag identifies not only the animal, but the animal's owner and address. Each tag contains an RF transponder that can transmit the data to a reader device, so animal-control officers simply "scan" stray dogs to determine where they belong.



A pain in the neck is what dogs probably think of RF dog tags. The identification devices are injected under the skin of the neck.



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PORTABLE DATA CARRIERS

one-time programmable memory. Necessarily, these devices have much higher transfer rates than smaller-capacity data carriers. They're available in versions with either serial or parallel access.

Because the Datakey devices contain standard memory ICs, they work just like ICs on a circuit board. In fact, each key consists of a tiny circuit board that brings out a flatpack IC's electrical connections to the key shaft. The assembly is surrounded, except for these contacts, with molded static-resistant plastic.

Static resistance is important for key chain use, according to Datakey applications engineer Steve Serber. A person can carry and transfer a charge of 15 kV in a dry atmosphere, Serber says, yet many data carriers don't provide nearly that much protection. Except for low-cost, light-duty products, all of Da-

Trash-can memory redefines GIGO

You'd think it would have started in Silicon Valley, but computer-aided trash collection is a European invention. In France and Germany, some trash containers now contain nonvolatile memory devices that dump their contents to computers on garbage trucks.

When a garbage truck lifts and empties a container, it also weighs the container and reads a unique number stored in the container's memory device. The number identifies the container's owner, allowing billing according to the amount of garbage produced.

In Paris, trash containers use Touch Memory data carriers from Dallas Semiconductor. Texas Instruments' RF data carriers find use in German trash containers.

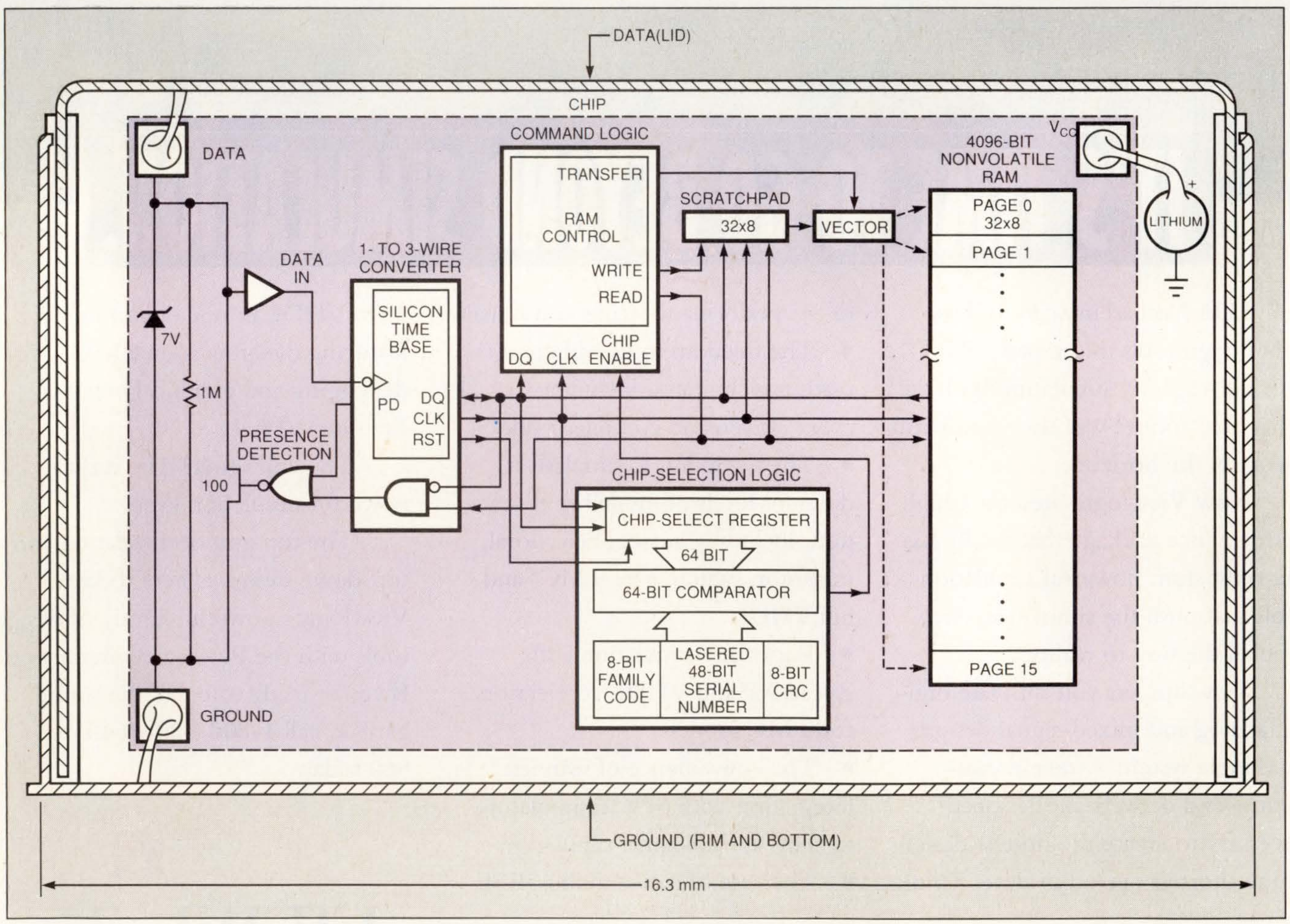

Fig 2—Dallas Semiconductor's Touch Memory data carriers contain features that help ensure data security and integrity. An unalterable, unique 48-bit serial number provides positive device identification, and some carriers also provide for a user password. Use of cyclic-redundancy-check code and scratchpad memory guard against data corruption even if electrical contact with a data carrier is faulty.

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PORTABLE DATA CARRIERS

takey's keys do; the cheaper versions protect to 10 kV.

To experiment with data-carrier applications, you can use development kits from the devices' manufacturers. Dallas Semiconductor, for example, sells a Touch Memory starter kit for $75. The kit includes assorted Touch Memory devices, a serial-port adapter, PC software, and assorted hardware. Datakey offers a different kit for each of its different types of carriers, with prices ranging from $250 to $350. TI's $1700 kit includes a stationary read/write RF unit (with antenna) and an assortment of read-only and read/write RF transponders. EDN

References

1. Small, Charles H, "Small memories take on wider applications," *EDN*, June 20, 1991, pg 67.
2. Legg, Gary, "Smart cards gear up for belated success," *EDN*, October 24, 1991, pg 51.

Article Interest Quotient
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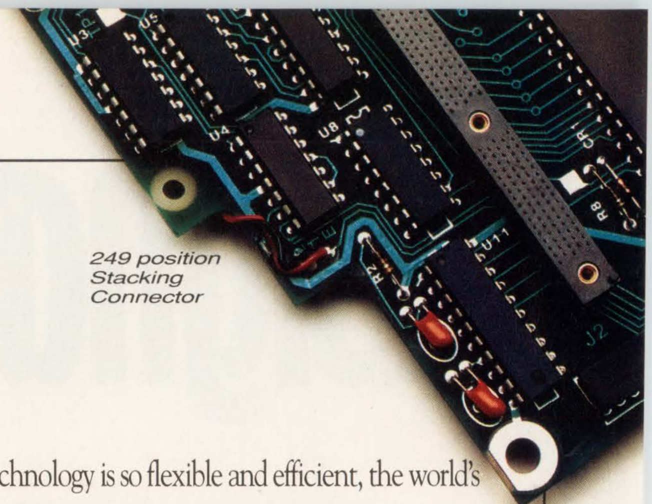
What's Coming Up In EDN

The September 3 issue of EDN Magazine will show you how to bring IC layout in-house so you can shorten design cycles and time-to-market. For Futurebus+ fans, Technical Editor John Gallant reports that a Futurebus+ standard seems right around the corner. Also, keep a lookout for some new Design Ideas.

1,156 position
LGA Socket



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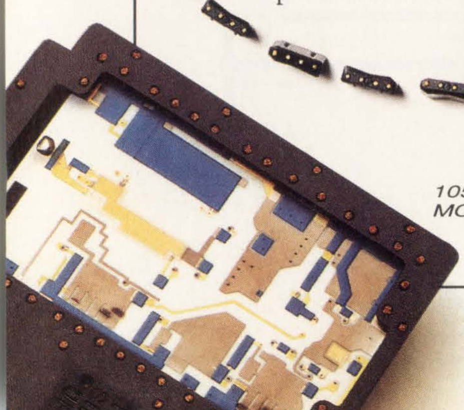

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CIRCLE NO. 80

Low-cost fiber-optic link achieves 1.5-Gbps data rate

The FTM- and FRM-8500 optical transmitter and receiver modules have changed the economics of implementing fiber-optic data links. These devices use low-cost optical components and a proprietary method for modulating laser diodes to transmit data at 1.5 Gbps over inexpensive multimode fiber.

The laser diodes the modules use as the optical source are the same ones found in compact-disc players and have an MTTF (mean time to failure) of 200,000 hours. The modules connect to standard 50/125- and 62/125-μm multimode fiber. The units are robust enough to tolerate a link having multiple connectors and a mix of fiber types. Data-transfer rates range from 100 Mbps to 1.5 Gbps over distances as great as 500m. The bit-error rate is $<10^{-12}$ with a link-loss budget of 10 dB.

The data link comprises three parts: the FTM-8500 transmitter module, the FRM-8500 receiver module, and the FLC-1000 link-controller IC. Both modules directly convert between electrical and optical signals, so you can use either encoded or NRZ data formats. The controller IC monitors the status of the transmitter and receiver modules. It provides signal compensation such as receiver gain control and transmitter bias voltages.

The link controller also provides a system-test interface that lets you monitor the data link's status and performance without using special optical test equipment. For example, the controller can measure optical power levels, report link failures, automatically shutdown optical transmission when you remove a connector, and monitor reliability factors such as drive currents, bias voltages, and transmitter temperature.

Both modules use 5 and 12V supplies and draw 300 mA at 5V and 40 mA at 12V. They measure 0.685×0.870×2.725 in. and have pin connectors that you can socket or solder to a pc board. The controller is available in a 28-pin DIP or SOIC package.

The transmitter module costs $310, the receiver module costs $300, and the controller IC costs $60, all in small qty. An evaluation board is also available.

—**Richard A Quinnell**

Finisar Corp, 3515 Edison Way, Menlo Park, CA 94025. Phone (415) 364-2722. FAX (415) 364-3041. Contact Jerry Rawls.

Circle No. 730

These fiber-optic transmitter and receiver modules use low-cost multimode optical components to send data at 1.5 Gbps over fibers as long as 500m.

Printer delivers 600-dpi resolution

Calcomp has built a 600 × 600-dpi laser printer, the CCL 600, around a 16-MHz Intel i960KB RISC μP and 82961KD print coprocessor pair. This printer is the first to deliver 600-dpi resolution for both A- and B-size sheets and sells for $4495. Current high-resolution, B-size printers cost more than $10,000.

Designed for monochrome, high-density printing, the CCL 600 prints the first page in less than 20 sec. Subsequent pages print faster, printing an 11 × 17-in., B-size page at a rate of 4 pages/minute; A-size pages print at 8 pages/minute. Operation is faster if you use a 300-dpi-resolution printer.

The processor combination provides print banding, which processes and prints pages as bands or subsets of the page. Banding minimizes the amount of memory needed for high-resolution printing. The CCL 600 needs only 2 Mbytes of dynamic memory for B-size printing. Memory expands to 42 Mbytes. Banding also speeds up printing—only a small portion of a page is done at a time.

The CCL 600 easily interfaces to standard computers (such as the IBM PC, and Apple Macintosh), workstations, and servers. Standard I/O interfaces include RS-232C, Centronics parallel, and Appletalk. A SCSI disk interface can also be added. The printer can be networked and can run multiple page-description-language (PDL) emulations. It emulates Postscript (Microsoft Trueimage), HP PCL5, and HP-GL/2 PDLs.

Calcomp CCL 600 laser printer

- Monochrome laser printer
- Prints A-, B-size sheets
- 600 × 600 or 300 × 300 dpi
- 35 resident fonts
- 4 pages/minute, B-size; 8 pages/minute, A-size
- 2000/1000 pages/month, duty cycle
- i960KB/82961KD CPU, coprocessor
- 2-Mbyte memory (expands to 42 Mbytes)
- 42 lbs, 14.9 × 18 × 22.4 in.
- $4995

For a fast design turnaround, Calcomp used the Peerless page-imaging operating system to provide a multitasking operation, PDL interpretation, I/O control, and to drive the Intel 82961KD print coprocessor.

See the Editors' Choice for a description of a coprocessor pair used in the CCL 600 printer.—**Ray Weiss**

Calcomp, Computer Graphics Group, 2411 W La Palma Ave, Anaheim, CA 92801. Phone (800) 932-1212; (714) 821-2000.

Circle No. 731

The Calcomp CCL 600 laser printer is built on the Intel printer-processor combination. It handles B-size paper with up to 600 × 1200-dpi resolutions.

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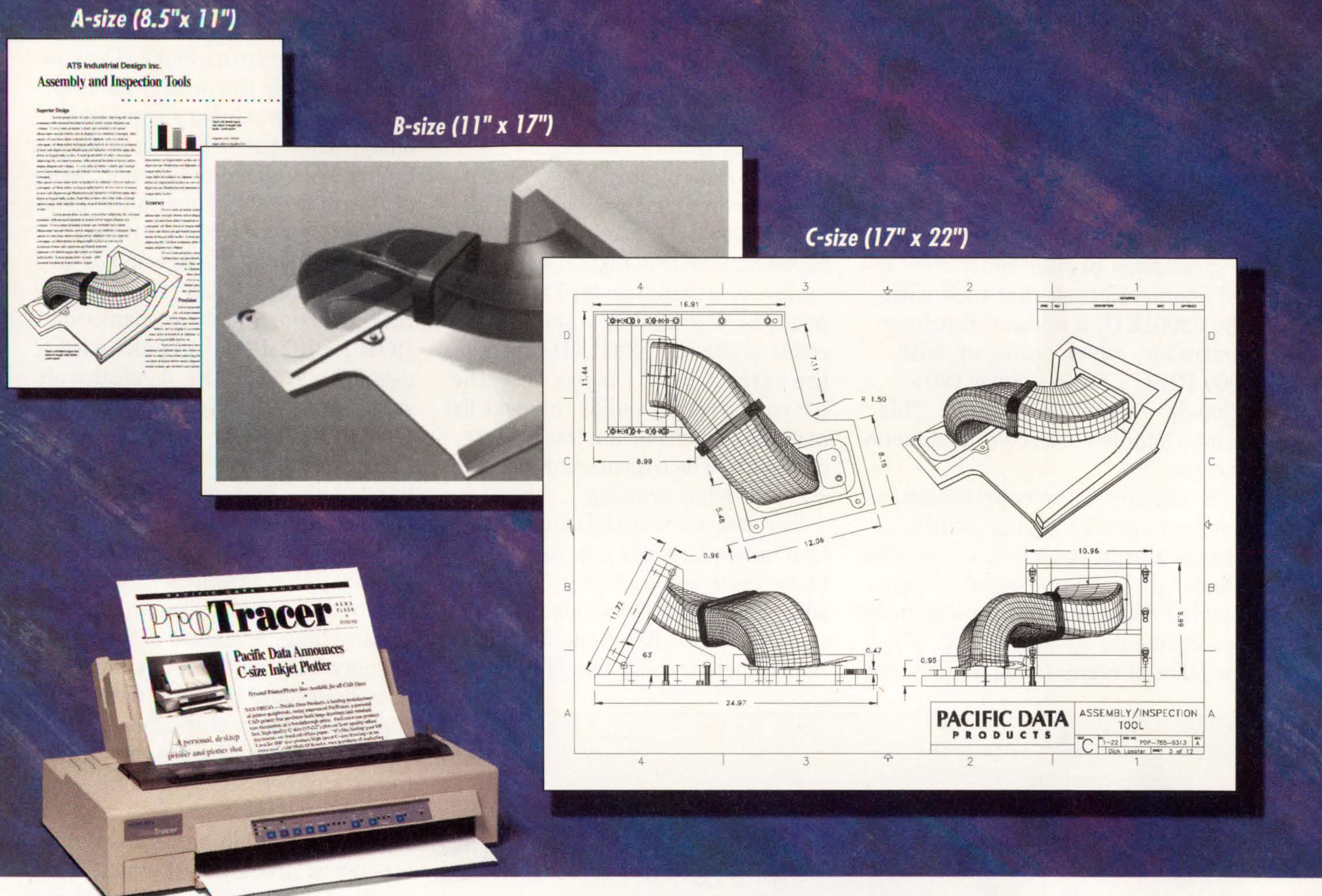

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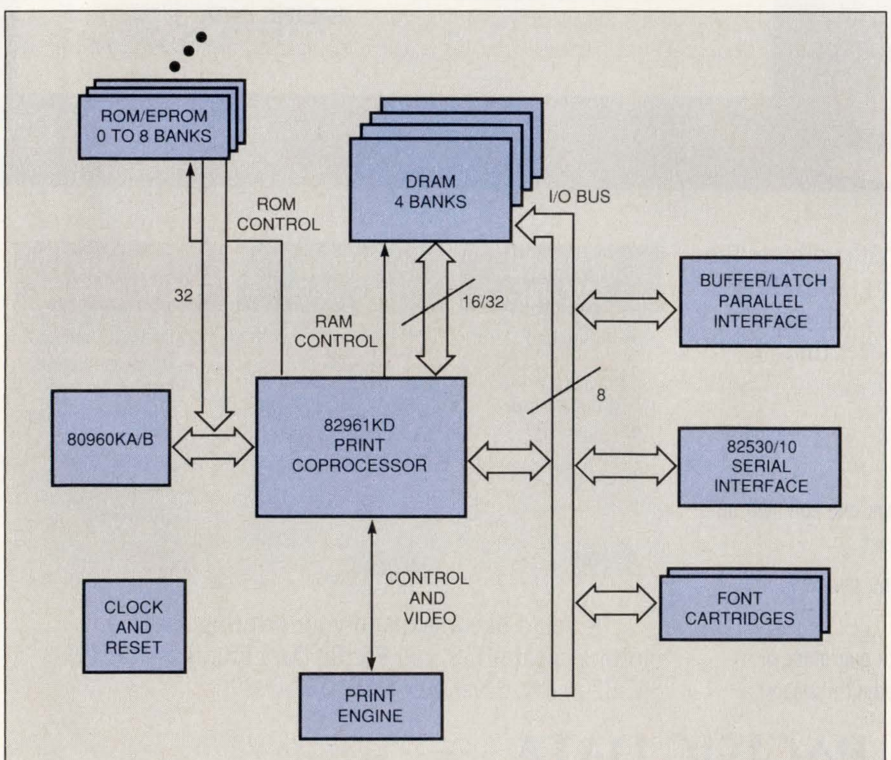
Intel laser-printer i960/coprocessor combination ups performance, cuts logic

Designing laser-printer controllers is a tough task, combining embedded μPs, staged data processing, and I/O control. One way to minimize glue logic, speed throughput, and simplify printing is to supplement the printer μP with a specialized printer controller. Intel engineers took that tack with the 82961KD, a dedicated printer controller, which teams up with i960 RISC μPs to deliver 600 × 1200-dpi-resolution printing. This combo handles both color and monochrome.

To cut costs, the coprocessor implements print banding, which breaks a print page into sections (or bands) that are processed sequentially. Print banding drops memory requirements by as much as 80% for 600-dpi resolutions, as only one completed band is held in dynamic memory rather than the full page. Banding was pioneered by HP's Laserjet printers running PCLs (printer-control languages), but it hasn't been a commercial success with Postscript-based printers. The 80960/82961KD combination opens up low-cost banding for Postscript printers. Processing is sped up because while the 82961KD processes the current band Display List, the μP concurrently builds the next list instead of waiting for the page to complete. The coprocessor also handles full-page printing.

The i960xx/82961KD combination also minimizes control logic. More than just a printer coprocessor, the 82961KD includes two memory controllers: one for dynamic memory and one for read-only μP program memory. The controllers enable the printer μP to access program memory simultaneously, while the printer coprocessor builds print lines in dynamic memory or moves them out to the printer. The controllers work directly with four banks of page-mode or static-column DRAM (eight with a RAS decoder), and two banks of ROM/EPROM (eight banks with a decoder). At 20 MHz, typical wait states are 2,0,1,0 for 100 nsec, interleaved EPROM memory, and 2,1,1,1 for 70-nsec DRAM. An I/O bus handles font cartridges and serial/parallel interfaces.



Combining Intel's i960 RISC μP with the 82961KD printer coprocessor delivers high resolution and fast printing. The coprocessor does printline graphics processing and acts as a memory and an I/O controller.

The coprocessor relieves the printer μP of graphics processing; it converts the high-level printer display languages into a compact Display List that combines print data limits and pointers with actual coprocessor operators. For execution, the Display List is then passed to the coprocessor by setting a special address register. This address register is double buffered: While one list is processed the next list can be set up. Display List processing completion triggers an interrupt, notifying the printer μP.

The 82961KD is a second-generation coprocessor. The first generation, the 82961KA (introduced in 1991) provides memory, I/O, and printer interfaces; however, it lacked the -KD's graphics-processing capabilities. With the -KA, graphics processing (processing the Display List with fonts) has to be done in the i960 μP. Whereas, the -KD has a Graphics Execution unit with 3-operand bitblt, line-drawing, and fill functions that appear in the coprocessor Display List.

The Graphics Execution Unit sports a simple, powerful 25-operation instruction set. Initialization operations set bit mapping and

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processing parameters; bitblt operators move, process, and logically combine memory bitmaps (including halftone bitmaps). Scanline operations enable programmers to compress font and special images into lines of compressed bit images. Bitmap addresses do not have to be on word or byte boundaries. Control instructions are simple: Jump to a graphic order (operation) in the Display List and STOP, which halts Display List processing.

Graphics processing speeds up with the 82961KD. For example, on a 20-MHz 80960SA CPU, a 2-operand bitblt operation processes 32 bits × 32 scan lines in 165 μsec; it takes only 34 μsec on a 20-MHz 80960SA/82961KD combination.

Scanline tables are a compact mechanism for replicating and filling polygon objects in memory. An object scanline table holds a set of drawing vectors or bounds for building the graphic object. Scanlines use RLL (run-length-limited) compression to reduce memory, storing 64- or 4096-pixel run-lengths into 16 or 32 bits of memory, respectively. Scanlines are represented in the Display List by a destination bitmap address and the Scanline table address. Scanlines save memory because the bitmap image is compressed into a table in memory, rather than being part of a Display List. Halftone tables supplement scanline tables for halftoning objects.

The Peerless Group, a printer-technology company, designed the 82961KD. Peerless also sells the PeerlessPage Imaging Environment for the printer-chip combination, which includes a printer-oriented, multitasking operating system and a full set of printer services, including font and memory management, control-panel interfaces, and advanced graphics. It handles a number of printer-description languages (PDLs), including HP's PCL- and Postscript-compatible interpreters. The software is available separately. The software core starts at 60 to 100 kbytes, without fonts and extras. Pricing is OEM based, with royalties running as low as $5 per unit, including software tools.

The 82961KD's printer partner is the Intel i960, a family of 32-bit RISC μPs. The family's low end includes the i960SA/SB, running at 10 and 16 MHz with 512 bytes of instruction cache, and a multiplexed external bus (32 bits address and 16 bits data). The -SB includes an 80-bit floating-point unit. Next is the KA/KB, running at 16, 20, and 25 MHz, with a full 32-bit external bus. Topping the family is the i960CA, a superscalar RISC unit running up to 33 MHz with an 8-, 16-, or 32-bit data bus.—**Ray Weiss**

The Peerless Group, 2629 Manhattan Beach Blvd, Redondo Beach, CA 90278. Phone (310) 536-0908. **Circle No. 732**

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CIRCLE NO. 85

RUGGEDIZED COMPUTERS

US military budget cuts may spell financial disaster for weapons manufacturers. But firms that develop and produce ruggedized computers have obtained new customers among prime contractors who no longer have to create computers that meet full military specifications.

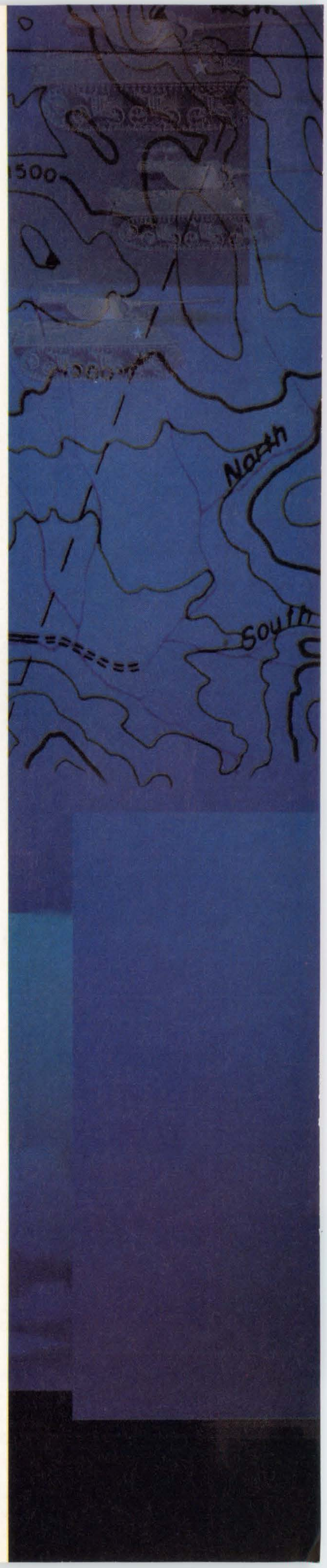
JD MOSLEY, Technical Editor

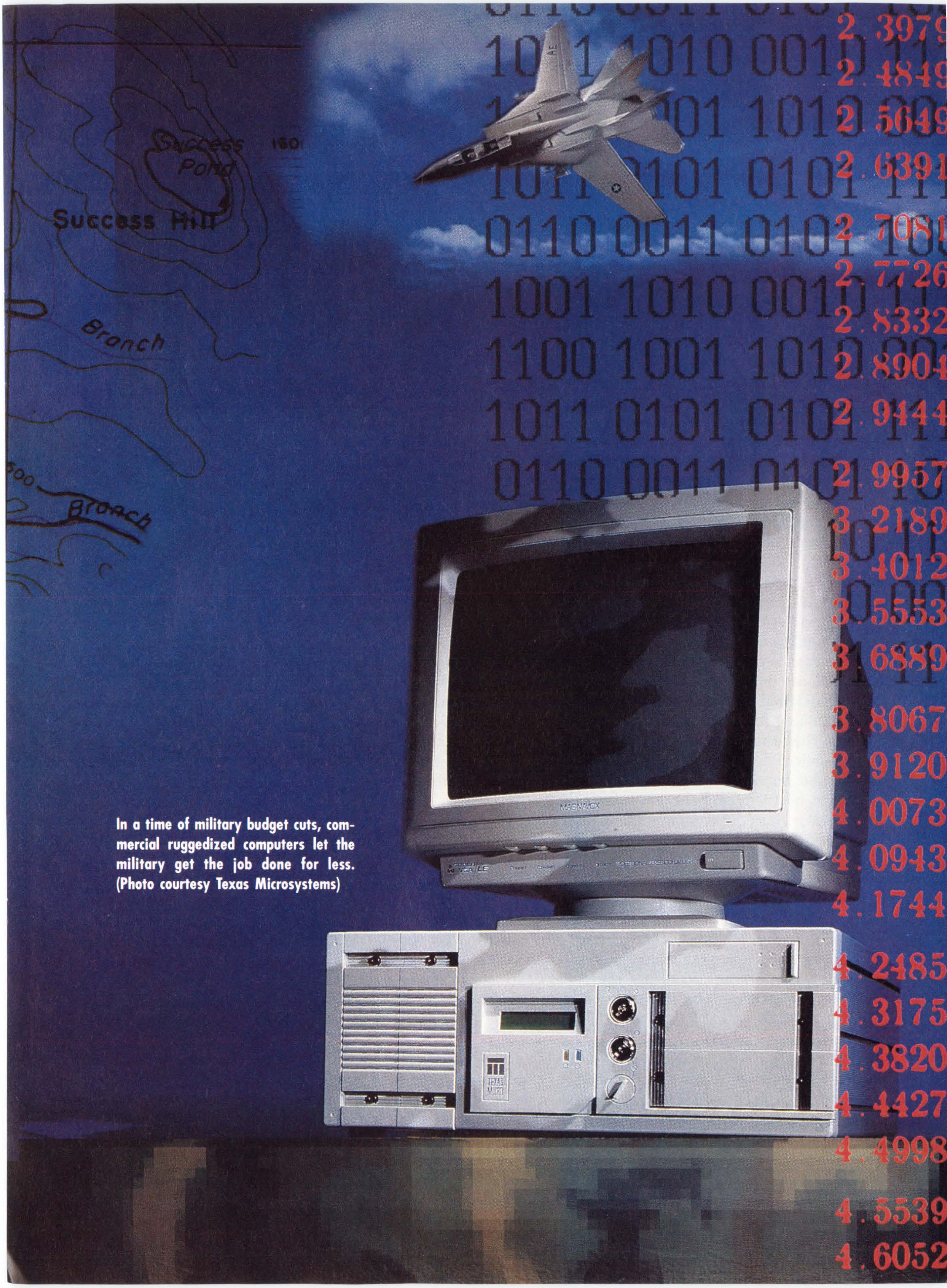
Although the end of the Cold War has terminated many military programs, the electronics industry may actually benefit from the belt tightening and cost scrutiny resulting from military budget cuts. For example, as the US armed forces seek ways to operate more efficiently, an increasing number of contracts are specifying commercial, off-the-shelf (COTS) ruggedized computers instead of custom-built units that meet full military specifications. However, the tricky part involves figuring out just how rugged a computer must be to meet the needs of each military project.

By letting contractors purchase COTS computers, the US government predicts savings of at least 50%. Ed Marcato, Director of Marketing at Mercury Computer Systems, says that where a MIL-spec version might cost five times as much as an ordinary PC, a COTS computer would probably cost about two times as much.

However, the savings is not merely monetary. Purchasing a commercially available computer reduces the time it takes the prime contractor to fulfill contractual obligations. Thus, the cutting-edge technology incorporated into the design at the specification stage still represents the latest engineering developments when the computer reaches its final destination in the field.

The contract won by Texas Microsystems to produce a handheld unit, referred to as the Soldier's Computer, illustrates the time and monetary savings. Scott Hovey, Texas Microsystems' portable products project manager, says, "the challenge is to get on the leading





In a time of military budget cuts, commercial ruggedized computers let the military get the job done for less. (Photo courtesy Texas Microsystems)

edge of technology without being on the *bleeding* edge." Therefore, the company plans to implement currently available pen-computing and voice-recognition techniques and to avoid such undeveloped concepts as virtual reality.

Trouble in paradise

Despite the increased latitude now available to computer designers, COTS has also created confusion and frustration. The lack of established precedent for designing less-than-bomb-proof computers that still withstand harsh military treatment has resulted in some contracts that call for COTS computers, but specify modifications that negate any potential savings of time or money. The problem is that no one is certain exactly how much ruggedization is necessary to meet each contract's specifications.

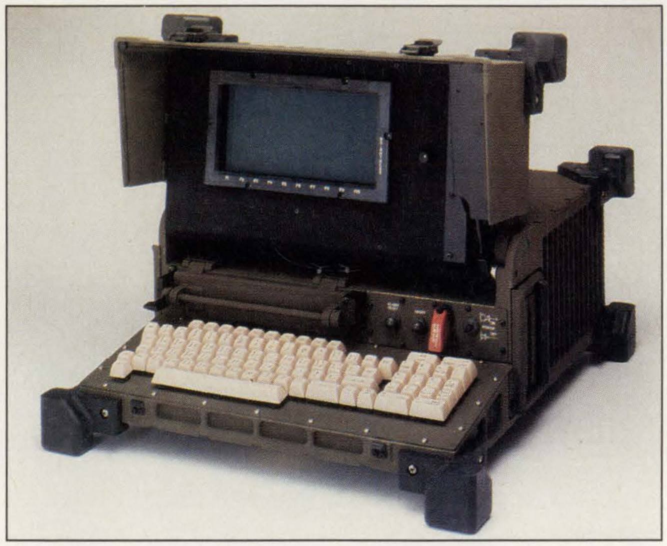
Yet, the government's directive is clear: Stop reinventing the wheel for each project. Current military budgets only allow for adaptation costs, not development costs. As Rex Zerger, Vice President of Sales and Marketing at Texas Microsystems, points out, the majority of contracts involve equipment that doesn't need to withstand battlefield conditions, and budget requirements will eventually drive the specifications into accordance with that reality and stabilize the stipulations placed on ruggedized equipment.

Ruggedization involves taking a commercial product and expanding its environmental performance without altering the schematic. Manufacturers add stiffeners and tie-downs to prevent boards from flexing under impact and house the boards in enclosures that can withstand hostile treatment and surroundings. As Allen Zubatkin, Vice President of Manufacturing at Mercury Computer Systems, notes, innovative packaging plays an important role when ruggedizing products for military applications.

Avionics in particular has stringent space and weight requirements, so contractors must provide maximum processing power in minimal configurations. By adapting commercial products to military needs, contractors not only maximize the processing power per centimeter, they also maximize the processing power per dollar spent.

Furthermore, the government has established standards for ruggedization, such as MIL-810C. Extensive testing to meet those standards and verified data from those tests must be available for government inspection during procurement. When selecting a vendor for ruggedized computers, it is important to ensure that the company has a solid understanding of the rules and regulations, as well as the supporting data for proof of compliance.

Consider, for example, the AN/UGC-144 communication terminal from Group Technologies. Its 8086 terminal processor has its own 40-Mbyte hard-disk drive and uses MS-DOS. The communication μP is an 80386 CPU that provides multitasking, event-driven services. Despite these fairly commonplace features, this terminal meets MIL-STD-810 for operation in rain, sand, dirt, and fungus. Drop testing involved 26 cycles of letting the unit fall 48 in. Its TEMPEST certification indicates that no electronic signals that would be detected by surveillance equipment will escape from the unit. This means even the keyboard's keystrokes have to be shielded from snoopers. Lightning protection and nuclear survivability round out the list of highlights. Yet the unit is available for as little as $16,000 (100).



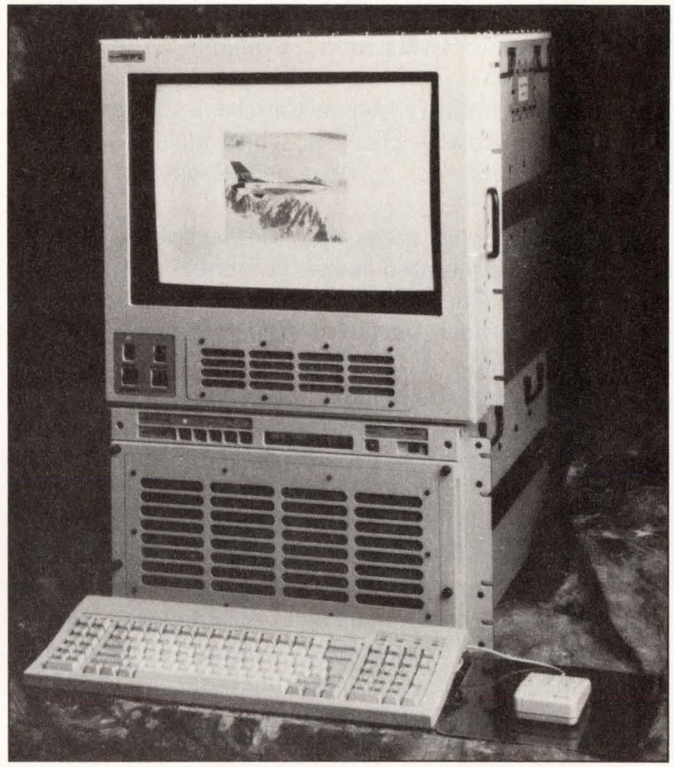
The AN/UGC-144 communication terminal from Group Technologies is available off the shelf and costs about half the price of a full MIL-spec computer.

John Rogert, marketing manager for Group Technologies, says that the toughest military ruggedization requirements for computers involve temperature. Freezing temperatures cause the lubricants in hard-disk drives to freeze. LCDs experience problems at both ends of the thermometer. Yet, even the relaxed military requirements for ruggedization may specify an operating-temperature range from freezing to 120°F. Storage and transit temperatures vary even more, from −40°F to +160°F. To compensate for such extreme temperatures in a box that has to be impervious to sand, water, and dirt, Group Technologies arranges components for maximum heat dissipation, coats the boards to seal out humidity, and then uses the aluminum enclosure itself as a heat-sink for conductive cooling.

Fault tolerance is another critical factor that frequently appears in military-bid requests. Although not every computer the military uses will wind up on a battlefield, each of these computers must operate reliably for battlefield conditions. Texas Microsystems has a line of fault-tolerant PCs that use the company's fault-tolerant system architecture.

The hardware's design maximizes system availability, data integrity, and data recovery for DOS-based applications. The series of fault-tolerant computers couple selective-component redundancy with diagnostic, regulatory, and recovery systems. The enhanced BIOS comprises a set of programs that coordinate data transfer and control instructions between the CPU, various peripherals and the computer's custom diagnostic coprocessors. The BIOS functions as a multitasking operating system, performing one layer below DOS to asynchronously control the interaction among the processors and peripherals.

To protect the most vulnerable hardware subsystems, the firm adds a redundant power supply, battery backup, and hard-disk drives. You can configure disk caching for either write-through or write-back operation. And to prevent a CPU crash from corrupting data on the computer's hard disk, the company uses a set of algorithms referred to as data-change auditing. This software lets you return the hard-disk data to a consistent point predating the hardware failure. A front-panel LCD provides system status and warning messages.

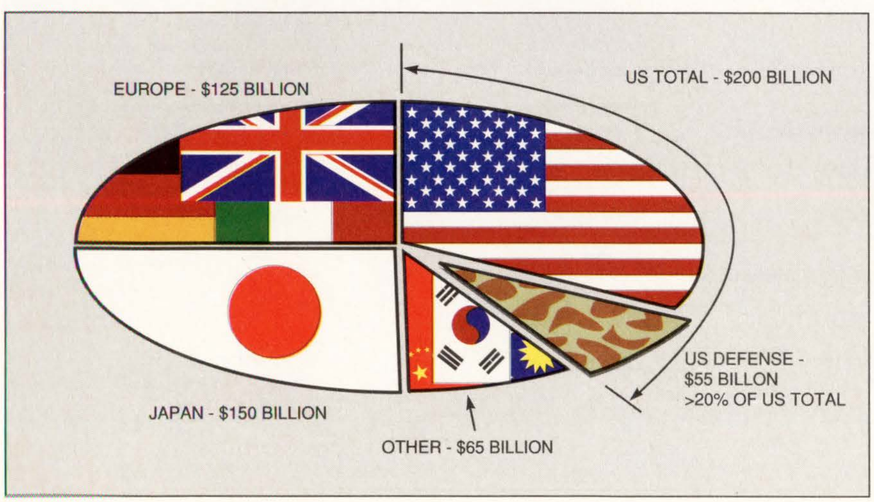


The ruggedized and TEMPEST-compliant SPARCstation from Codar Technology meets both the military's and Sun Microsystems' specifications.

Minimize maintenance, maximize reliability

Even the components of rugged computers can vary from those found in commercial units. Besides the obvious need to use military versions of every IC on board, you may need unique components to meet some of the military's rigorous needs. Simtek Corp (Colorado Springs, CO) is a manufacturer of nonvolatile static RAMs (SRAMs). David Bowers, the firm's vice president of sales and marketing, observes that when avionics and weapons incorporate embedded processors, requirements for maximum system reliability often clash with limited available space.

Consider, for example, computer systems for wire-guided torpedoes. The torpedoes receive instructions and power via an umbilical wire attached to the deployment vehicle. At some point, the wire breaks and the torpedo's computer must reboot as a self-powered device with full knowledge of the weapon's trajectory and direction. Using batteries to keep the computer's memory intact introduces yet another level of mainte-



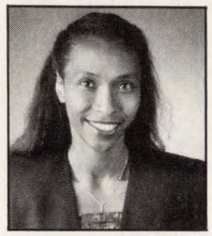
US defense electronics represent approximately 10% of the worldwide market. Despite the dropping defense budget, military electronics should maintain a steady dollar volume. (Statistics courtesy United Technologies Microelectronics Center)

nance and vulnerability. In addition, Bowers says that battery-backed SRAMs aren't available as MIL-STD devices and that core-memories are expensive and heavy. Thus, military contractors have embraced his company's nonvolatile SRAMs, which meet MIL-STD-883 requirements for environmental operation from −55°C to +125°C.

However, Bowers notes that the decline in military spending has prompted many IC vendors to drop or simply not develop military versions of their chips. If this trend continues, system designers for military contractors will have an increasingly difficult time ruggedizing units to government specs.

In addition, Hovey says that a lack of components from US companies is prompting contractors to use off-shore devices when prototyping ruggedized units. A prime example involves the shortage of American-made displays for rugged computers. At this point, Hovey has encountered no restrictions on the use of Japanese parts for the contracts his company has obtained. However, he notes that several US companies have shifted their manufacturing sites overseas to avoid the higher duties imposed upon imported components, such as color LCD panels. The duty on fully assembled computers is a fraction of the duty cost for imported parts. These computer manufacturers, unable to obtain US-built panels, are left little choice but to shut down US assembly plants due to this bureaucratic bungle that originally intended to aid US manufacturers of LCD panels.

So although the relaxation of military requirements for computer systems was an attempt by the government to reduce both procurement time and costs, the process is still evolving. As both the contractors and the government go through the growing pains of working flexibility into procurement, the end result promises to provide benefits for everyone—including the taxpayer. EDN



Author's Biography

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Acknowledgment

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Manufacturers of ruggedized computers

For more information on ruggedized computers such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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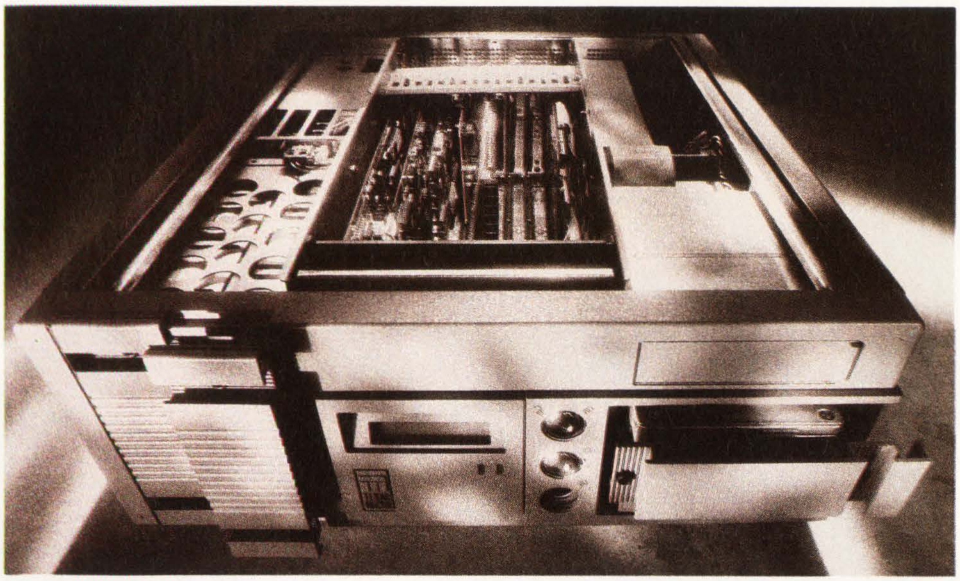

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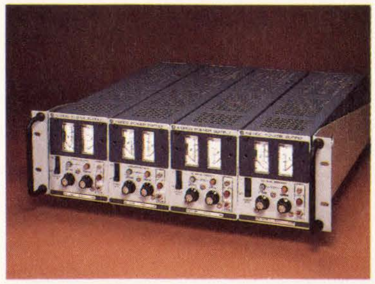

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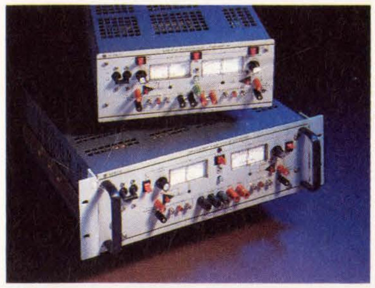

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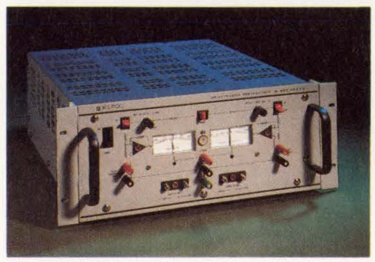

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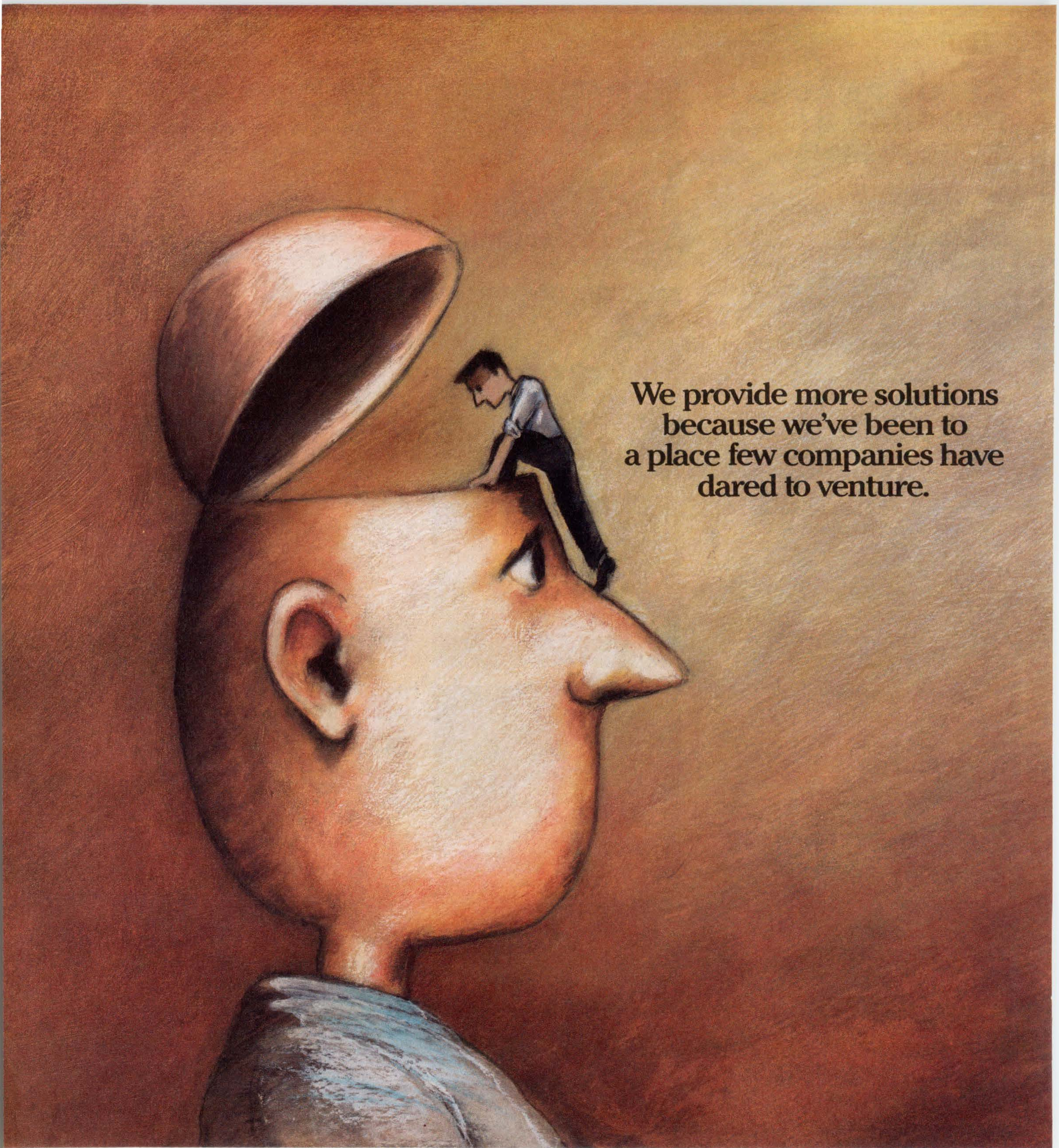
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John Allen Mitchell, Comdisco Systems

You've digitized an analog signal, but the sampling rate is too high—or too low—for your system. Multirate filters can't supply missing information, but they can alter the effective sampling rate after you've acquired the data. With graphical development tools, designing such filters isn't difficult.

Recent advances in DSP ICs and development software have made digital-signal-processing techniques more attractive than ever. Digital filters are particularly appealing because they offer stability, predictability, and ease of control that are difficult, if not impossible, to achieve using analog techniques. However, the very proliferation of DSP systems brings with it the need for accurate communication at different data rates. Transferring music from a CD to digital audio tape (DAT), for example, means having to switch from the 44.1-kHz sampling rate of CDs to the 48-kHz rate used by DAT recorders. This example is typical of multirate systems, which shift the effective sampling rate of discrete-time signals up and down. Usually, these shifts occur in multirate filters. Using the techniques explored here, you can design efficient multirate filters for any DSP application.

In a typical DSP system, an analog signal first passes through a lowpass antialiasing filter that removes unwanted components. The system then samples the signal and converts it to a digital format. The digitized signal next proceeds to the heart of the system, the digital signal processor, which performs the numerical manipulations. The DSP algorithm—a program employing binary addition, subtraction, multiplication, and other numerical processes—dictates the exact nature of the manipulations. For example, when the DSP μP performs the filtering, it would numerically convolve the digitized signal with a set of filter coefficients that define the filter's response. After processing, the system converts the digital signal back to an analog format and smooths it with a lowpass reconstruction filter.

DSP design tools generally fall into two classes: those that use a data-driven computational model and those that use a time-driven model. This article explores the time-driven style because of its simplicity and suitability for multirate filter design.

In the time-driven style of control, a master clock runs at the highest signal frequency in the DSP system. The clock is incremented in discrete steps, or iterations, at the inverse of the sampling frequency. Each block in the design performs its particular function once every iteration unless a special "hold" input is high. In that case, the block is disabled. A disabled block ignores data arriving at its input; data at the block's output remains unchanged. (The behavior is much like that of synchronous digital circuits.) By selectively enabling and disabling function blocks, you can create different kinds of multirate filters.

The following discussion presents three multirate filter designs. All of them change an input sample rate by strategically enabling and disabling the hold inputs of function blocks. Note that you can consider a block to be enabled if its hold input is not connected; that is, the block behaves as if its hold input were pulled to zero.

These designs are synchronous—all the sampling rates are rational multiples of each other. You can realize asynchronous systems in a similar way, but their implementation is beyond the scope of this article.

Without multirate filtering, the only way to shift from one sampling rate to another is to convert the digital signal to a continuous analog waveform and then resample the analog waveform at the new rate. Though straightforward, such an inelegant solution carries with it analog-type problems, such as instability and noise—to say nothing of expense. Obviously, a better solution is to manipulate the sample rate entirely in the digital domain without any intermediate analog processing.

There are a number of multirate filter methods that work almost equally well, although all involve various tradeoffs that the designer must be evaluate. These tradeoffs include algorithmic complexity, digital-signal-processor loading, and system memory requirements.

First classical method

Increasing a signal's sampling rate by some integer factor L is called interpolation. Decreasing the sampling rate by an integer factor K is called decimation. By combining these two operations you can change the sampling rate of a given signal by any rational factor. You can express this factor as the ratio L/K, where L represents the ratio of the number of a data set's real and interpolated samples to its real samples and K

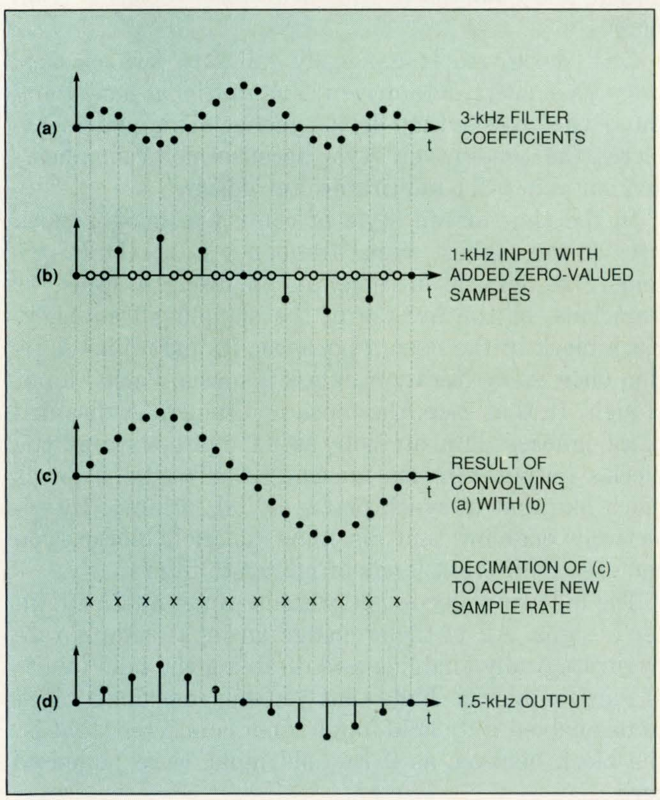


Fig 1—Interpolation and decimation change a signal's sample rate.

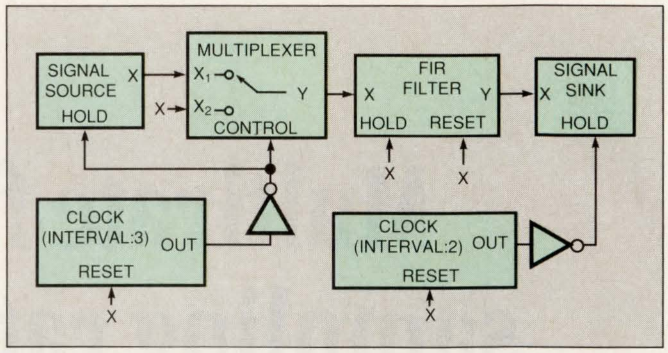


Fig 2—This simple approach to multirate sampling is not very efficient because a large fraction of the terms computed are eventually multiplied by zero.

represents the ratio of samples retained to the set's total number of samples after interpolation.

Consider the following up-sampling example. Suppose an A/D converter samples a signal at 1 kHz, but for the sake of further digital signal processing, you must increase the sampling rate to 1.5 kHz. The ratio L/K would be 1.5/1; its simplest fractional equivalent is 3/2. This ratio tells you to first interpolate the signal by 3 and then decimate it by 2. The process involves inserting $3-1$, or 2, samples between each pair of input samples and then discarding $2-1$, or 1, sample out of every 2—that is, every other sample—to achieve the new rate.

Fig 1 illustrates this process. First, increase the sampling rate by zero padding—adding zero-valued samples between each pair of input samples. This operation raises the effective sampling frequency to 3 kHz. Shifting to the final 1.5-kHz rate is a simple matter of halving the 3-kHz value by discarding every other sample. However, discarding every other sample at this stage would eliminate half of the original samples. The effect is the same as sampling the signal at a rate lower than twice the highest frequency component, an operation that violates the Nyquist criterion. The reconstituted signal would consequently suffer from aliasing.

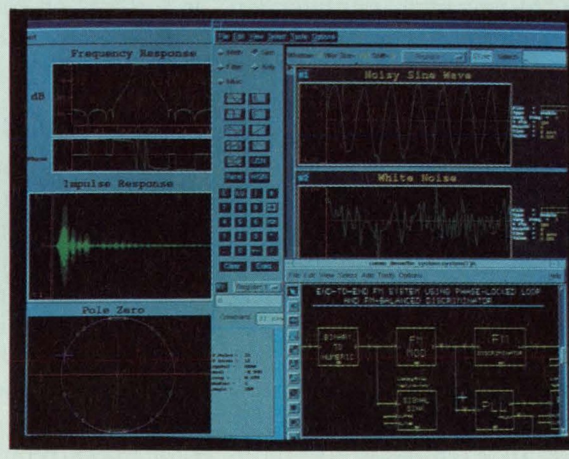
You can avoid this problem by inserting an interpolating filter between the zero-padding and decimation stages. (The filter coefficients are at the top of the diagram.) The filter assigns approximate values to the zero-padded samples in much the same way that an integrator smooths a spiky analog signal. Once the waveform is properly interpolated, you can safely discard samples to achieve the new down-sampled rate.

The signal-flow diagram in **Fig 2** represents what is probably the simplest means of achieving sample-rate conversion using decimation and interpolation. The symbology is similar to that used in the DSP Framework from Comdisco Systems (see **box**, "Automating multirate-filter design"). To achieve a system sample rate of 3 kHz (the least common multiple of 1 kHz and 1.5 kHz), the clock's interval is set at 3 so that its output goes high one time out of three. When inverted, the output goes high two out of three times. Consequently, the source block fires only on every third sample.

The input for this design originates at the signal-source block. This block represents a file containing the original data. In practice, the source might be a block of memory, the digital portion of an A/D converter, or some other supply that you can enable. The output of the source block goes to a multiplexer. The multiplexer's other input is left unconnected and is

Automating multirate-filter design

In the multirate systems discussed in this article, the output is precise, stable, and predictable because mathematical functions, as opposed to physical circuit properties, dictate the waveform manipulation. This predictability is the beauty of DSP.



The DSP framework allows graphical DSP design and analysis and can automatically generate programs, netlists, and VHDL specs.

But DSP does have an uglier side; to process waveforms under software control, you must have software. Traditionally, programming DSP µPs has involved hand coding—a task so complex and laborious that many designers avoid it out of shear intimidation, clinging, instead, to older, less elegant approaches. This situation needn't exist. With today's graphics-based DSP-software development tools, you can design, test, and even implement sophisticated DSP systems without writing (in the usual sense) a single character of code.

Graphics-based DSP software tools let you design DSP systems as if you were building them from discrete components. You need not even be aware that software is what determines the system characteristics. You create designs by drawing on a workstation screen and connecting blocks (icons) to form signal-flow diagrams. These diagrams take the place of DSP-algorithm programs expressed as text. The diagrams incorporate the mathematics for filters, multipliers, channels, and similar functions. The computer handles the arcane formulas that were once the province of mathematicians. You can concentrate on your design rather than on programming details.

Traditionally, engineers have been forced to hand-craft complex models to simulate various DSP designs and compare tradeoffs among them. This process is time consuming and error prone and tends to inhibit the number of iterations a designer is willing to try. Comdisco Systems' graphical DSP Framework lets users design, analyze, and even automatically implement any DSP system, including those discussed in this article.

The DSP Framework lets you create signal-flow diagrams by connecting DSP function blocks. The blocks have a hold input that disables the function for as long as a nonzero value is present. When a block is disabled, it ignores any input and does not update its output. Therefore, you can control a signal's sample rate by selectively enabling and disabling the function blocks that process the signal.

Because the polyphase filter allows efficient execution but is difficult to design from scratch, Comdisco Systems now includes a custom polyphase-filter block as part of its DSP Framework library. To use the block, you enter the interpolation rate, the decimation rate, and the name of the file containing the FIR-Filter coefficients. The software automatically creates the necessary number of subfilters, apportions the coefficients among them, and generates the input and output clocks.

Thus, with just a few commands, users can automatically create polyphase filters of any complexity. Issuing a few more commands automatically generates code to program the design into a fixed- or floating-point DSP processor. The DSP Framework can also automatically partition a design for execution on multiple processors and can generate VHDL code to synthesize an ASIC or an FPGA.

therefore interpreted as zero. Because the multiplexer's control input is connected to the same clock as the source block's hold input, the multiplexer selects the output from the source block whenever the source block fires; it otherwise selects a zero. The multiplexer therefore outputs a signal having a 3-kHz sample rate; two out of every three samples have a value of zero.

The output of the multiplexer goes to an interpolating filter of the finite-impulse-response (FIR) variety. The filter rejects spectral components that would lead to aliasing and interpolates the proper magnitudes for the zero-padded samples. Generally, you select the passband of this filter to be symmetrical about $\frac{1}{4}f_S$, where f_S represents the new sampling rate. You determine the filter's cutoff frequency (f_C) by halving the smaller of the two sampling frequencies and selecting a value just under that value. Because 1 kHz is the smaller of this system's two sampling frequencies, the filter's f_C should fall just below 500 Hz—say, at 400 Hz or so. This choice ensures that the filter will attenuate alias components close to the 1-kHz sampling frequency.

The last stage in the system is the signal sink. This block represents a file that receives the interpolated digital signal from the filter. In a real multirate-filter system, the signal sink could be a block of memory, the digital section of a DAC, or some other stage that you can enable. A clock whose interval is 2 switches the signal sink on and off at every other sample, thereby decimating the 3-kHz digital signal to 1.5 kHz.

Although this multirate system is straightforward and requires a minimum of hardware, it is inefficient in several ways: One is that the filter computes all of the outputs when only every second output is required. Another is that it multiplies outputs by 0 two out of three times. Thus, this implementation wastes processor cycles computing unneeded outputs and performing unnecessary multiplications. It wastes memory too because the filter's tapped delay line must store unnecessary data. These drawbacks can prove burdensome in systems where memory is tight and execution time is at a premium. One way to tackle these shortcomings is to focus on conserving CPU time and not give too much thought to conserving memory. Doing so yields the next approach to multirate filtering.

Second classical method

Fig 3 shows a multirate-filter design that doesn't compute outputs it doesn't need. This design is about twice as fast as the previous one. Note that the input stage, which comprises a clocked signal source and a 2-input multiplexer, is the same as before. The difference lies in the FIR-filter section, which the diagram breaks down into its three constituents. These are a tapped delay line, a dot-product stage, and a source of filter constants. Understanding how the overall design works requires a slightly more detailed look at the filter constituents.

Fig 4 illustrates the workings of the three FIR-filter sections. The tapped delay line consists of a series of cascaded delay elements, the number of which depends on the filter order. (For simplicity, the number of stages in this illustration is just four.) Data moves sequentially down the delay line. After going through

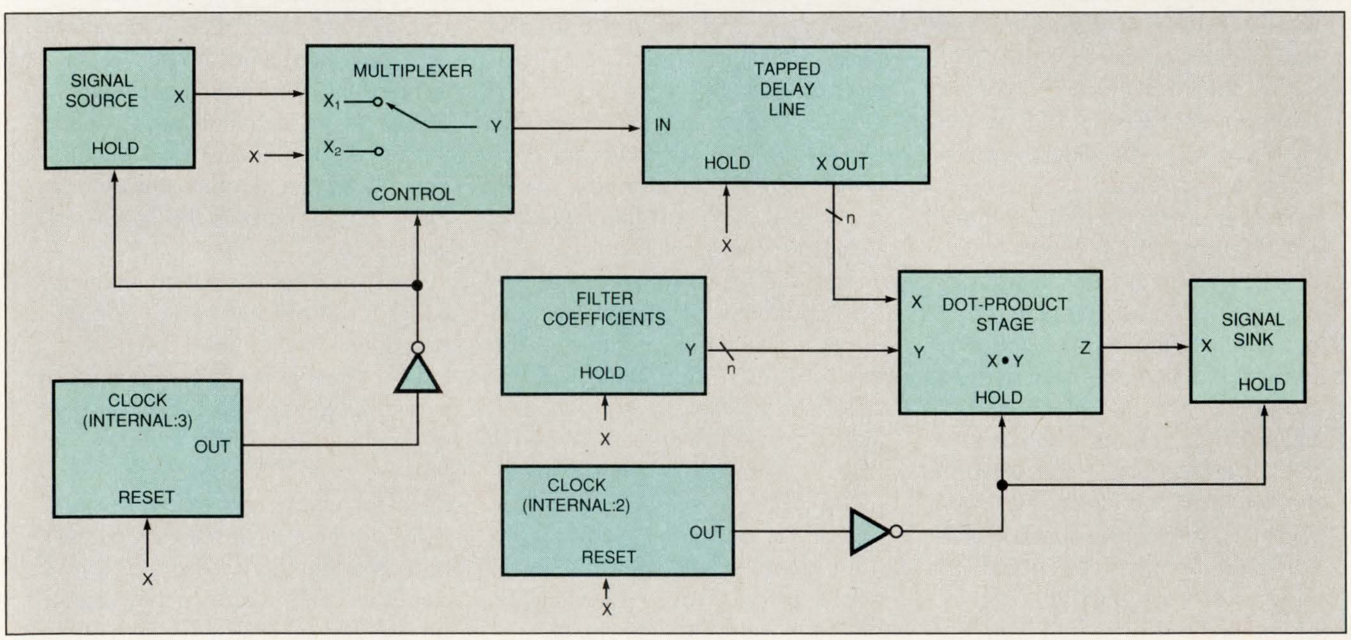


Fig 3—This more efficient approach enables the dot-product stages only when you need their outputs.

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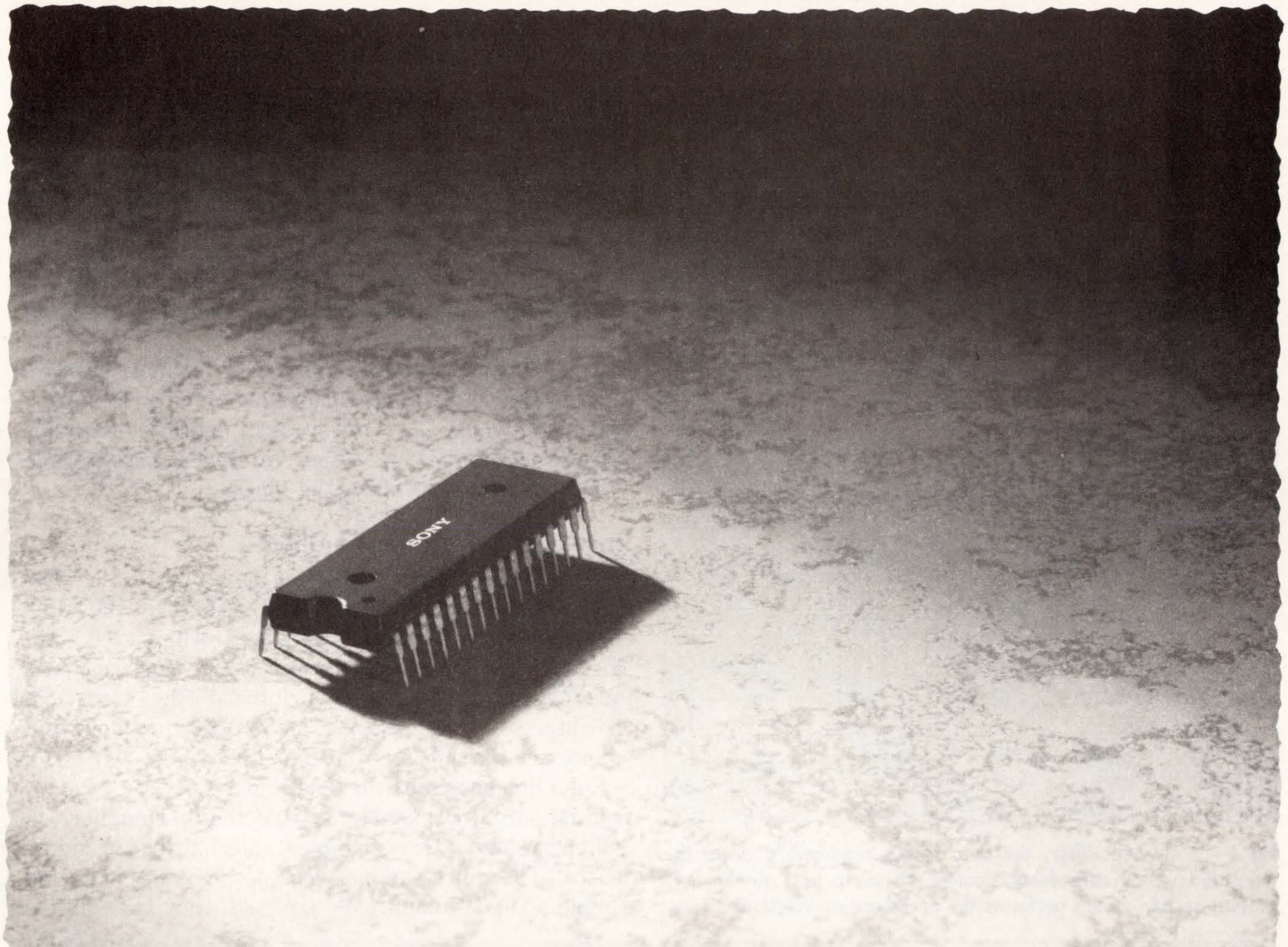

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each delay element, the data goes to the dot-product section, which performs the necessary convolution.

The dot-product section multiplies the input samples by a set of filter coefficients, b_0 to b_n. These coefficients, which define the filter's impulse response, are stored in the filter-constants block. The output of the dot-product stage is therefore a sum-of-products, the value of which is a linear function of present and previous input values. The process is akin to what happens in an analog lowpass filter integrating a continuous function. By enabling the dot-product stage only when it is needed, you can both modify the sampling rate and save on execution time.

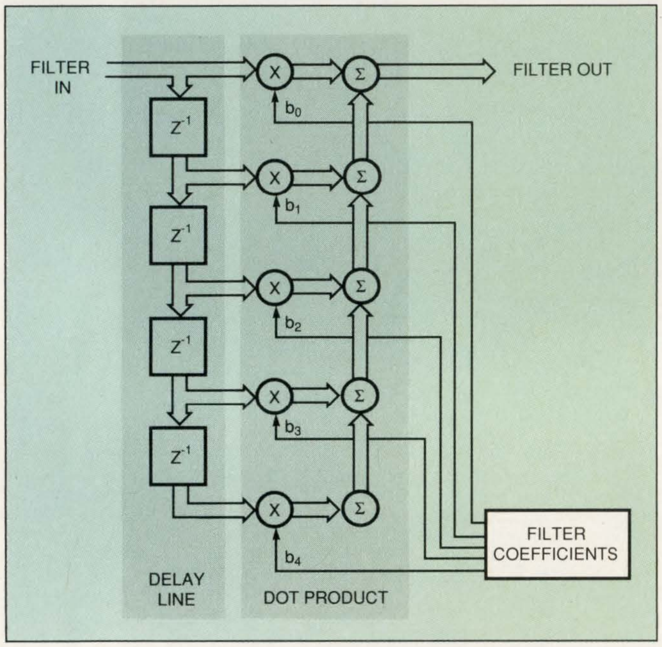

Fig 4—In this FIR filter, the data moves sequentially down the delay line. After each delay element, the data goes to the dot-product section, which performs the necessary convolution.

Now go back to **Fig 3,** where the FIR filter appears in a simpler, high-level format. Note how blocks substitute for the delay-line, dot-product, and filter-constant sections, and how single lines represent the multiple lines that actually connect the blocks.

Unneeded operations go on hold

The tapped delay line sends its data to the dot-product stage, which multiplies the data by the filter coefficients before sending outputs to the signal sink. The dot-product stage performs the X∘Y operation only for every second multiply. During the other intervals, the interval-2 clock places the multiply on hold and suppresses the output from the signal sink.

Fig 5 demonstrates the relationship between the input and output clocks. Notice that the up-sample clock is high two out of three samples, thus halting the signal source. The down-sample clock is high every second sample. (The two sinusoids look as if they have differ-

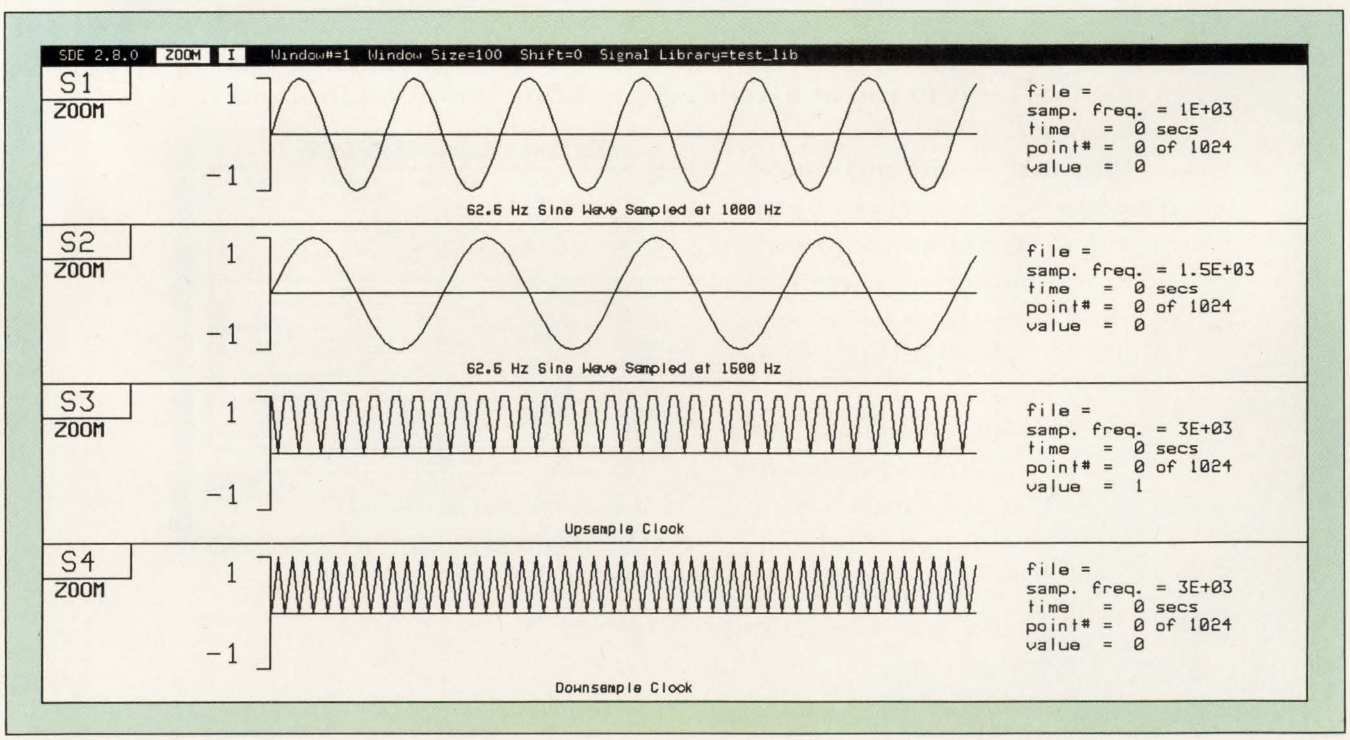

Fig 5—This display shows an input signal sampled at 1 kHz (S1), the output signal sampled at 1.5 kHz (S2), the up-sampled clock signal (S3), and the down-sampled clock signal (S4).

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ent frequencies because both use the same scale but have different sample rates. You can easily verify, however, that the sinusoids do have the same frequency.)

Because calculating multiplicative convolutions and convolutional sums is so processor intensive, this multirate implementation saves time by performing those operations only when they are necessary. However, the system is still inefficient because two of every three inputs to the tapped delay line are zero. Although not computing outputs that are destined to be ignored saves time, multiplying by zero wastes time too. The next implementation avoids this difficulty by exploiting the structure of the FIR filter.

In contrast to the previous "brute force" designs, the following multirate implementation wastes no time adding zero-valued samples that end up being discarded or multiplied by zero. This technique is accordingly more efficient, although its operation is certainly less intuitive.

The previous designs used a single filter, which took combined input samples and zero-valued samples, performed calculations on them using a set of internal filter coefficients, and produced an output with a new sample rate. The next approach splits the filter into several subfilters, each of which takes a subset of the overall filter coefficients, performs the necessary calculations, and outputs the result at a specified time. The outputs from the various subfilters then combine sequentially into a single output. Because each subfilter performs its calculations at a particular time or phase, this implementation is called the polyphase technique.

Fig 6 shows the basic operation of a polyphase filter. Note how different its action is from that of the previ-

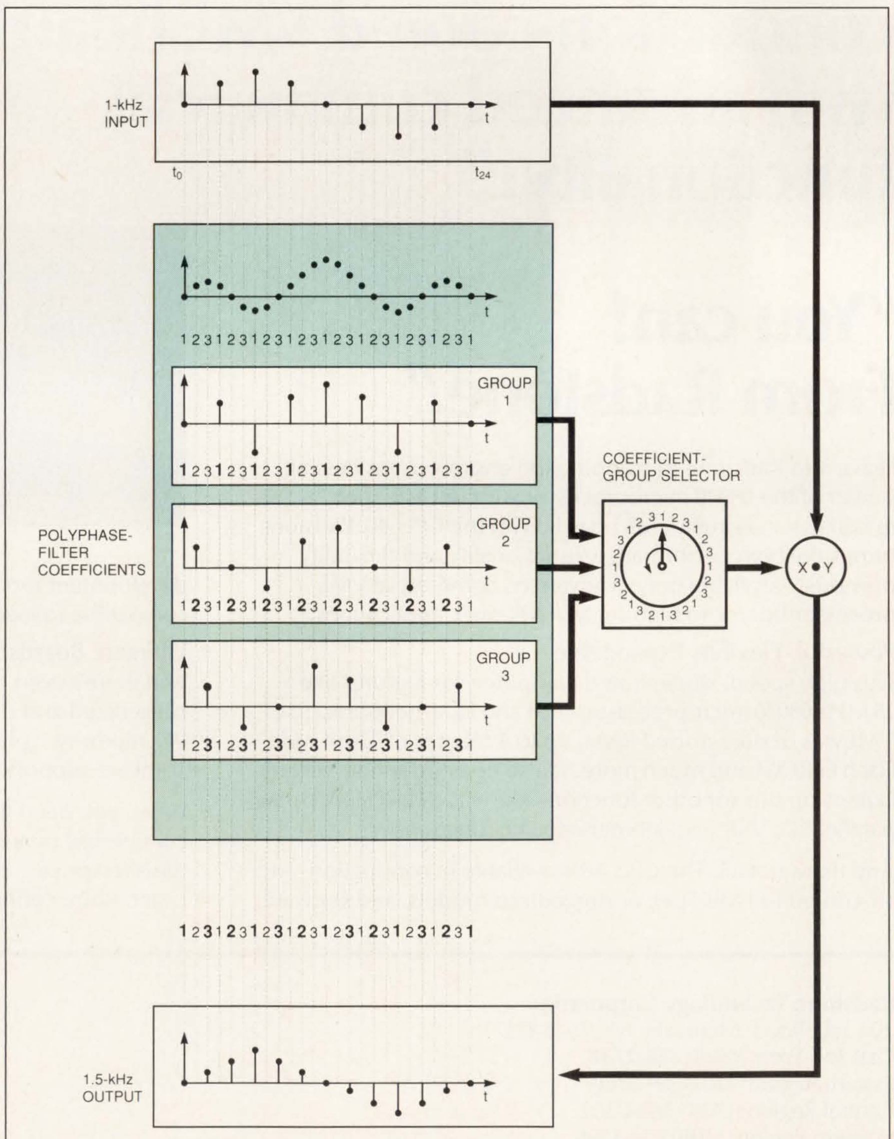

Fig 6—The polyphase filter achieves its efficiency by interpolating the proper sample magnitudes at the same time it assigns positions. No decimation takes place.

ous examples. The designs that used interpolation and decimation first assigned positions to the samples by zero padding. They then interpolated to assign the proper magnitudes to the zero-valued samples before decimating them. The polyphase filter achieves its efficiency by interpolating the proper sample magnitudes at the same time it assigns positions. No decimation takes place.

Once again, the f_C of the filter is the least common multiple of the input and output frequencies (in this case, 3 kHz). The filter coefficients are divided into three groups. Now follow the action of the filter as it increases the sampling rate of the 1-kHz input to 1.5 kHz. You'll note that at t_0, the first input sample is convolved with the first filter coefficient in group 1. The result appears at the output. At the next instant, the corresponding filter coefficient in group 2 would go unused because no output is destined for that time. Therefore, the filter ignores that coefficient and jumps to group 3 because the corresponding coefficient there will determine an output. As with t_1, no output is destined for time t_4, so no convolution takes place. The filter jumps to the next coefficient that will cause an output. This coefficient comes from group 2. In a like manner, the next coefficient to result in an output will come from group 1.

As you can see by following what happens at each instant, t_n, the filter selects a coefficient from group 1, then from group 3, then from group 2, and repeats the process. The coefficient-group selector commutates this sequence. (In an actual polyphase filter, a clock controls coefficient selection.)

Polyphase filter uses three subfilters

The high-level system block diagram for the polyphase filter appears in **Fig 7**. Note the three subfilters and the 3-phase clock, which enables each filter at the proper time. The overall sample rate is equal to the input or output sample rate, whichever is larger. In this case, the output frequency of 1.5 kHz determines the overall sample rate, which is also the speed at which the signal sink is clocked. However, the signal source (input), though clocked at 1.5 kHz, needs to run at 1 kHz. The data-read clock, which holds the signal-source block for one out of every three samples, accomplishes the adjustment. The source block therefore outputs at 1 kHz.

The subfilters are sequentially enabled by a 3-phase

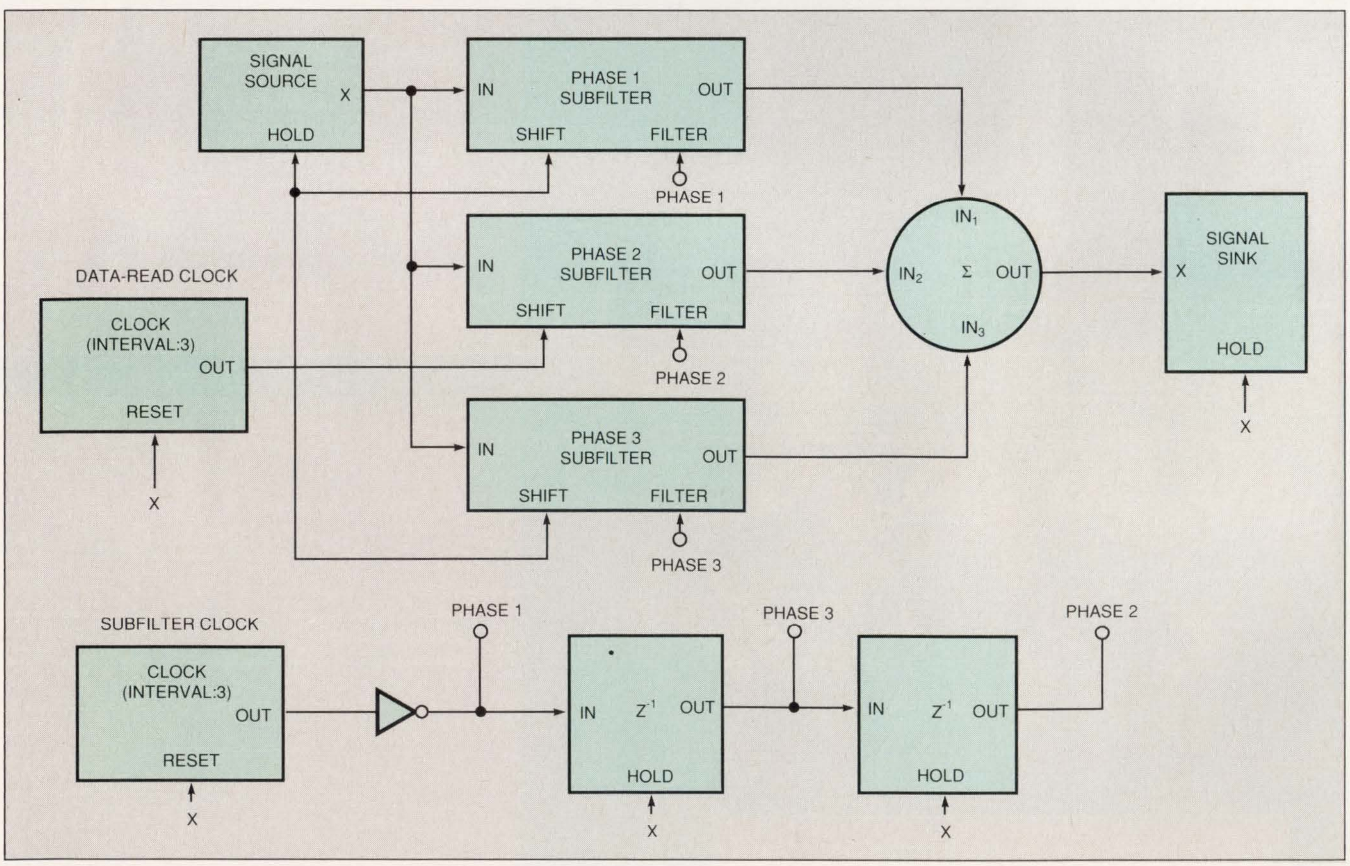

Fig 7—In this high-level system block diagram for the polyphase filter, note the three subfilters; note also the 3-phase clock, which enables each filter at the proper time. The overall sample rate is equal to the input or output sample rate, whichever is larger.

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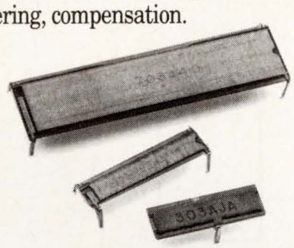

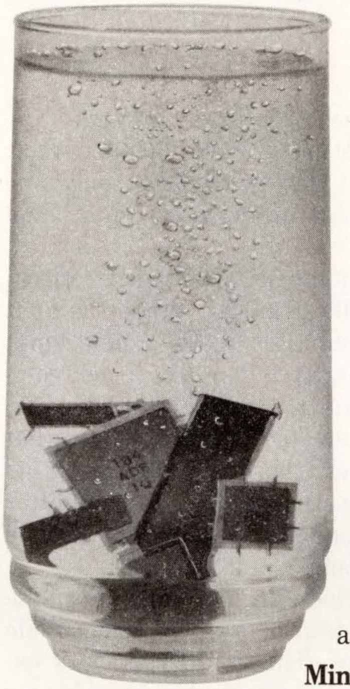

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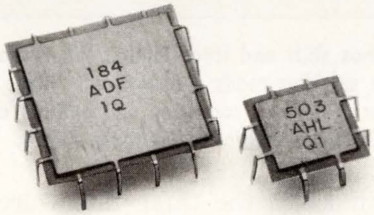

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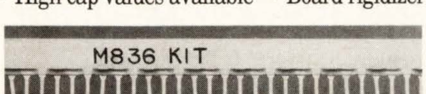

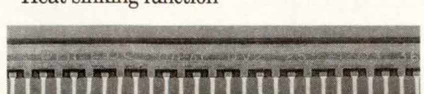

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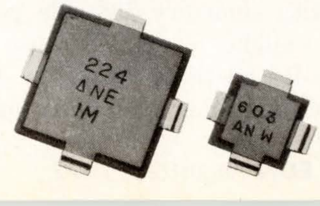

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clock—a tapped delay line with three outputs. The outputs are skewed so that only one is low (active) at any time. Accordingly, at any given time, only one subfilter will compute a dot product, output it, and have it selected at the adder.

Fig 8 shows the components of each subfilter block. Each block has shift and filter inputs. When the shift input is low (zero), the subfilter reads a new input sample. When the filter input is low, the block computes and outputs a dot product. Otherwise the subfilter multiplexer selects a zero to be output. (Note that for demonstration purposes, the **Fig 6** example used only one dot-product stage. In actuality, each subfilter performs its own dot-product calculation, as **Fig 8** shows. The result is the same.)

The 3-phase subfilter clock ensures that only one subfilter outputs sample data at a given time, while the other two output zeros. The use of this clock explains why **Fig 7** conveniently substitutes an adder for the multiplexer normally used to commutate the three subfilter outputs into a single output.

Because of their relative efficiency, polyphase filters are better for multirate filtering than simpler implementations. They do, however, take significantly longer to design. This statement is especially true when the difference between the original and interpolated sampling rates is great because a polyphase filter would require many subfilters and subcoefficients. Keep in mind the following when planning polyphase systems of the type presented here:

- The simulation clock (master clock) should match either the input or the output sample rate, whichever is higher.
- The sampling frequency you assume when designing the filter will be the least common multiple of the two sample rates.
- When the sample-rate change is expressed as a ratio L/K, L represents the number of subfilters needed, and K represents the factor by which you will be decreasing the sampling rate. If L>K, hold L−K out of L inputs. If K<L, hold K−L out of K outputs. (K will be 1 in cases of pure interpolation, and L will be 1 in cases of pure decimation.)

Although the two classical multirate filter designs yield equally accurate results, the polyphase implementation saves the most CPU time. Polyphase filters are undeniably more complex than ones that use traditional zero-padding methods, but polyphase filters' complexity shouldn't dissuade you from experimenting. You might, for instance, use only one tapped delay line for all three subfilters. Because splitting up the subfilters takes more glue logic, you might arrive at an implementation in which the three filters are not really separate. The filter selects only one coefficient at a time, so you might use a single filter along with an addressing scheme that assigns coefficients as needed. EDN

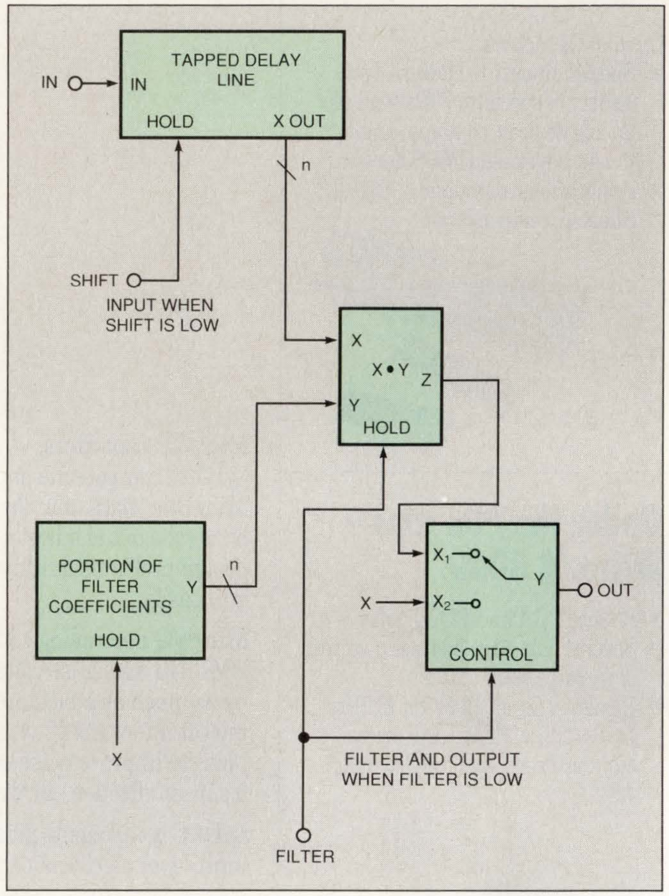

Fig 8—Each subfilter block has shift and filter inputs. When the shift input is low (zero), the subfilter reads a new input sample. When the filter input is low, the block computes and outputs a dot product. Otherwise, the subfilter multiplexer outputs a zero.

Author's biography

John Allen Mitchell is a technical marketing engineer with Comdisco Systems in Foster City, CA, where he has worked for three and a half years. His responsibilities include writing of application notes, articles, and marketing literature. He holds a BS in electronic engineering technology from California Polytechnic State University. John's hobbies include creating electronic music (he has a recording studio in his home), writing poetry, and painting. His paintings have been exhibited in two galleries.

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

Spice models low-bias op amps correctly

Bonnie C Baker, Burr-Brown Corp, Tucson, AZ

Having correct values for input-bias currents of low-bias operational amplifiers is critical, especially when you model transimpedance circuits. Yet Spice macromodels for operational amplifiers do not always model dc parameters correctly. This Design Idea presents an example of a technique you can use to correct the Spice model of any low-bias op amp.

In the Spice macromodel in **Fig 1**, the input bias current of the OPA627 should equal twice the IS of the P-channel JFET model JX, or 1.0 pA. However, a Spice simulation will predict that the gate current from J1 and J2 is 10 to 20 pA, depending on the common-mode voltage of the input stage and the magnitude of the supply voltages. The way the model simulates the drain-to-gate and source-to-gate nodes of the input FETs generates this additional current.

The culprit causing the additional current is the Spice default value, GMIN. In this case, 1/GMIN is the impedance between the drain-and-gate and the source-and-gate. This impedance keeps the gate node of each FET from floating. The default value for GMIN is 1×10^{-12}S.

For example, if $V_{DG}=14V$, $V_{GS}=1.6V$, and $IS=500\times10^{-15}A$, the op amp's simulated bias current will register greater than the expected 1.0 pA. The simulated bias is

$I_{BIAS}=IS\times2+I_{GS}+I_{DG}$,
$I_{BIAS}=IS\times2+V_{GS}\times GMIN+V_{DG}\times GMIN$,
$I_{BIAS}=0.5\times10^{-12}A\times2+1.6V\times1\times 10^{-12}+14V\times1\times10^{-12}$,
$I_{BIAS}=16.6$ pA.

The solution is to add two voltage-controlled current sources (G11 and G21) to each gate of the differential pair of the operational amplifier (**Fig 1**). Adding G11 to the gate node of J1 and G21 to the gate node of J2 results in the following calculations (assume the voltage across G11 is 15V):

$I_{BIAS}=IS\times2+I_{GS}+I_{DG}-I_{G11}$,
$I_{BIAS}=IS\times2+V_{GS}\times GMIN+V_{DG}\times GMIN - V_{G11}\times GMIN-I_{G11}$,
$I_{BIAS}=0.5\times10^{-12}A\times2+1.6\times10^{-12}A+14\times10^{-12}A-15\times10^{-12} A-(1.6\times10^{-12}A+14\times10^{-12}A-15\times10^{-12}A)$,
$I_{BIAS}=1.0$ pA,

where the V_{G11} term in the second equation accounts for the current through the resistor from a JFET's gate to ground (not shown in **figure**) that is part of

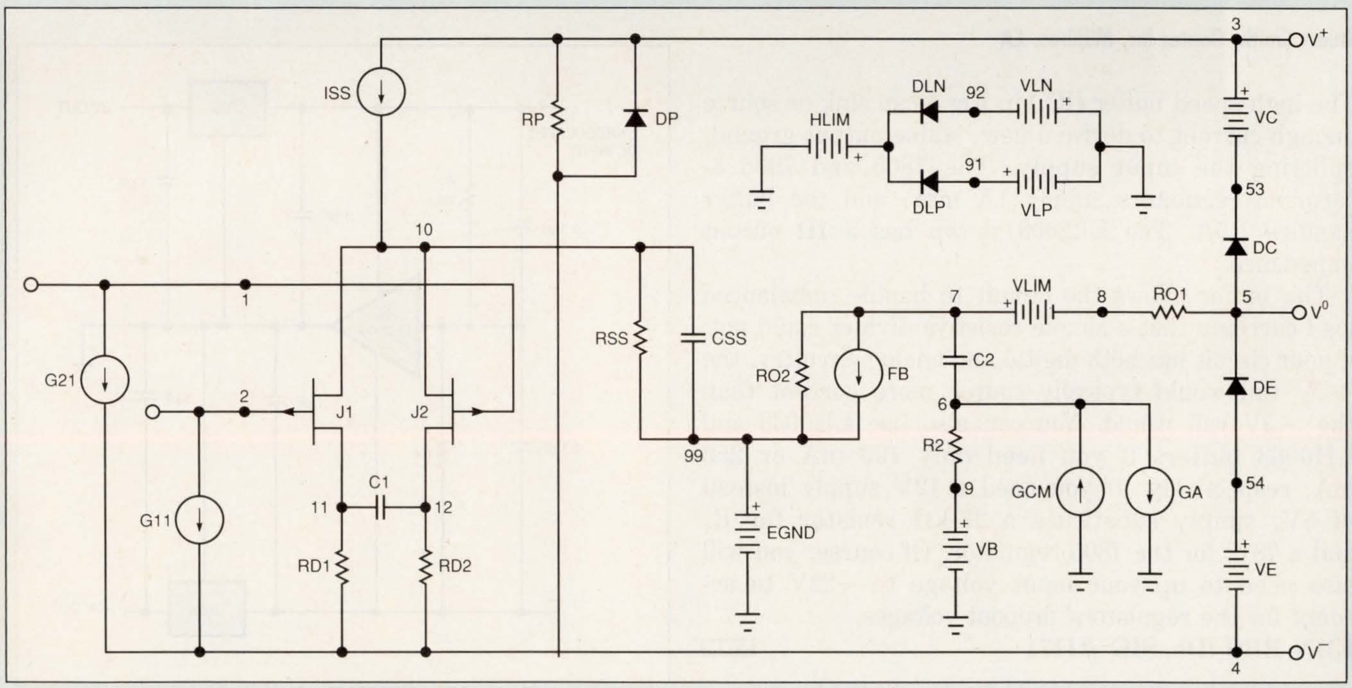

Fig 1—Adding a pair of voltage-controlled current sources, G11 and G21, to this Spice macromodel of a JFET-input op amp cancels side effects of the JFETs' models to yield accurate simulations of input-bias currents.

the current source's Spice model. Also note that the current (I_{G11}) in the second equation expands to three terms in the third equation because G11 has three control voltages (see **listing**).

Another solution to this problem is possible. You could change GMIN to a smaller value, such as 1×10^{-13}. Changing GMIN to 1×10^{-13} will give an input-bias current of 1.156 pA. This approach may seem to be the most logical. However, changing this parameter can cause convergence problems elsewhere in the model and will not give an accurate simulation.

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Listing 1—Low-bias op-amp macromodel

```
* CONNECTIONS:   NON-INVERTING INPUT
*                | INVERTING INPUT
*                | | POSITIVE POWER SUPPLY
*                | | | NEGATIVE POWER SUPPLY
*                | | | | OUTPUT
*                | | | | |
.SUBCKT OPA627   1 2 3 4 5
C1   11 12 3.182E-12
C2    6  7 23.00E-12
CSS  10 99 40.45E-12
DC    5 53 DX
DE   54  5 DX
DLP  90 91 DX
DLN  92 90 DX
DP    4  3 DX
EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
FB    7 99 POLY(5) VB VC VE VLP VLN 0 419.4E6 -40E6 40E6 40E6 -40E6
GA    6  0 11 12 2.432E-3
GCM   0  6 10 99 3.779E-9
ISS   3 10 DC 1.840E-3
HLIM 90  0 VLIM 1K
*
* Input JFETs for the OPA627
*
J1   11  2 10 JX
J2   12  1 10 JX
*
* Input bias current correction circuitry
*
G11 2 4 POLY(3) (10,2) (11,2) (4,2) 0 1E-12 1E-12 1E-12
G22 1 4 POLY(3) (12,1) (10,1) (4,1) 0 1E-12 1E-12 1E-12
*
R2    6  9 100.0E3
RD1   4 11 419.4
RD2   4 12 419.4
RO1   8  5 54
RO2   7 99 1
RP    3  4 4.286E3
RSS  10 99 108.7E3
VB    9  0 DC 0
VC    3 53 DC 2.700
VE   54  4 DC 2.700
VLIM  7  8 DC 0
VLP  91  0 DC 55
VLN   0 92 DC 55
.MODEL DX D(IS=800.0E-18)
*
* Model for the input JFETs, J1 and J2
*
.MODEL JX PJF(IS=500.0E-15 BETA=1.545E-3 VTO=-1)
*
.ENDS
```

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Buffer splits power supply

Stuart Smith, Elantec Inc, Milpitas, CA

The high-speed buffer (IC_1) in **Fig 1** can sink or source enough current to derive a new, stable output ground, splitting the input supply. The 7805 and 7905 3-terminal regulators supply 1A max, and the buffer handles 1.5A. The EL2008 shown has a 1Ω output impedance.

The buffer allows the circuit to handle unbalanced load currents that a simple resistive divider could not; if your circuit has both digital and analog circuitry, the +5V rail would typically source more current than the −5V rail would. You can also use LH0033 and LH0063 buffers if you need only 100 mA or 250 mA, respectively. If you need a 12V supply instead of 5V, simply substitute a 22-kΩ resistor for R_1 and a 7812 for the 7805 regulator. Of course, you will also need to up your input voltage to ~22V to account for the regulators' dropout voltages.

EDN BBS /DI_SIG #1171 EDN

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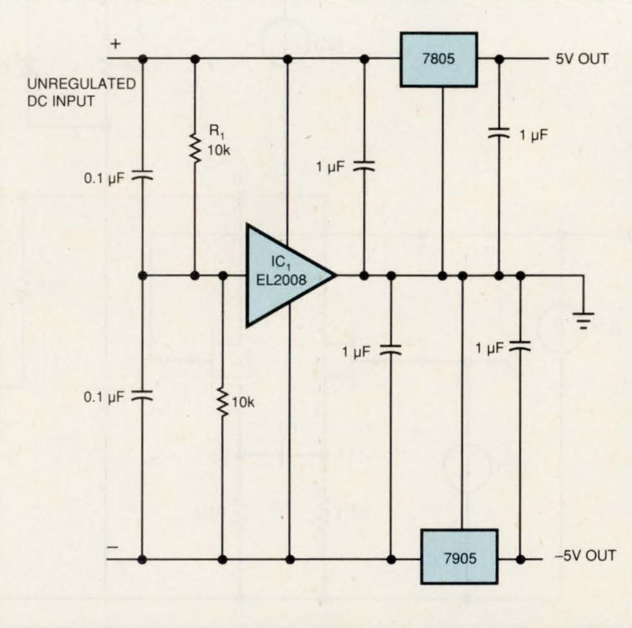

Fig 1—The high-speed buffer splits the input supply by sinking or sourcing enough current to compensate for unbalanced loads.

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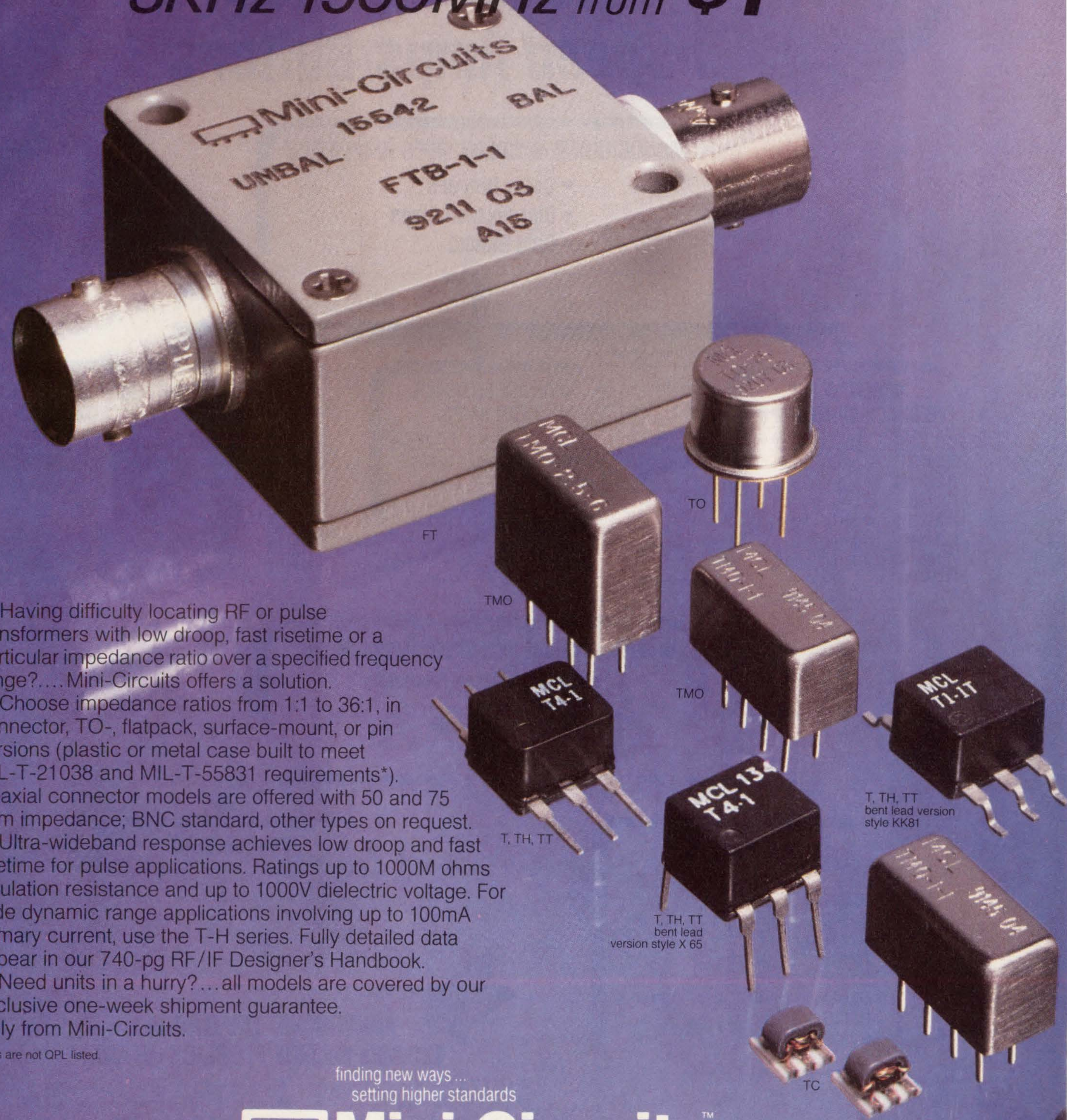

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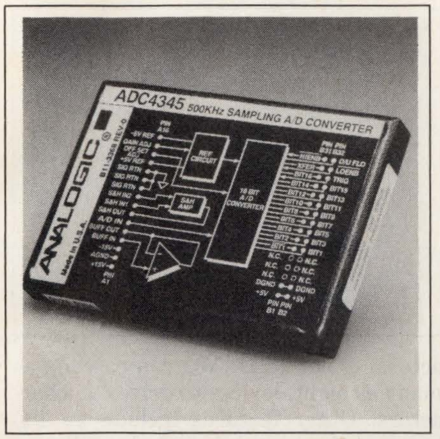
Integrated Circuits



Integrated S/H and A/D converter. The ADC4345 unit integrates a S/H circuit and a 16-bit A/D converter in a 2.5×3.5×0.44-in. module. It can digitize 250-kHz signals, using a 500-kHz sampling rate. Step response is 800 nsec, and the noise specification is 50-μV rms maximum. S/N ratio from dc to 100 kHz is 95 dB, and the peak distortion at 100 kHz is −99 dB. $460 (100). **Analogic Corp,** Data Conversion Products Group, 360 Audubon Rd, Wakefield, MA 01880. Phone (508) 977-3000. FAX (617) 245-1274. **Circle No. 391**

Light-sensor array. The TSL214 integrates a 64×1-pixel charge-mode array, 64-bit shift register, clock generator, S/H circuit, and analog buffer in a single 14-pin clear-plastic DIP. You only have to supply an external clock between 10 kHz and 500 kHz and a control signal to initiate an integration period. Each pixel measures 120×70 μm, and they are spaced 125 μm center to center. $6.80 (1000); evaluation kit, $125. **Texas Instruments Inc,** Semiconductor Group, Box 809066, Dallas, TX 75380. Phone in US and Canada, (800) 336-5236, ext 3990; (214) 995-6611, ext 3990. **Circle No. 392**

PCM transmission chips. The MV1403 family combines frame synchronization, time-slot 16 signaling functions, HDB3 (high-density bipolar) encoding and decoding, and cyclic-redundancy-check circuits on a single chip to transmit PCM signals according to CCITT recommendations. The series features several dual-function devices: the MV1442 device that has an HDB3 encoder/decoder and provides clock regeneration for 2.048-Mbps transmission; the MV1443 time-slot zero transmitter/receiver; the MV1444 transmitter and HDB3 encoder; and the MV1445 receiver and HDB3 decoder. $10.74 to $13.50 (1000). **GEC Plessey Semiconductors,** 1500 Green Hills Rd, Scotts Valley, CA 95067. Phone (408) 438-2900. **Circle No. 393**

Fast SRAMs. The HM6708SH 256-kbyte static RAMs have a 65,536×4-bit organization. The 5V devices feature access times of 10 and 12 nsec. The 0.8-μm devices have TTL-compatible inputs and outputs, and are suitable as secondary cache RAMs for i486, 68040, or R4000 μPs operating at 40 or 50 MHz. The devices come in a 24-pin SOJ package and draw 140 mA operating and 40 mA in standby. The 10-nsec version, $29; 12-nsec version, $23 (1000). **Hitachi America Ltd,** Semiconductor & IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (800) 448-2244; (415) 589-8300. FAX (415) 583-4207. **Circle No. 394**

Floppy-disk controllers. The FDC37C651 and FDC37C652 controllers contain the company's 765B CMOS floppy-disk controller core, a digital data separator, two 16450-compatible UARTs, a bidirectional parallel port, multiple power-down circuitry, an IDE port, and on-chip, 24-mA ISA bus drivers. You can software-select the options for the FDC37C651 chip through configuration registers. The FDC37C652 chip has game-port select logic to integrate an on-chip game port. FDC37C651, \$6.35; FDC37C652, \$5.39 (10,000). **Standard Microsystems Corp,** Component Products Div, 80 Arkay Dr, Hauppauge, NY 11788. Phone (516) 435-6000. **Circle No. 395**

LCD driver IC. The e1350 LCD driver IC operates on supply voltages as low as 3V and typically draws 95 μA. It communicates with most 4-, 8-, and 16-bit μPs to drive 128 segments (16 characters) on an LCD. You can cascade as many as eight devices to drive 128 characters. Other features include an I²C bus interface, an integrated oscillator, display-memory switching, and automatic increment loading. The 40-pin DIP, less than \$3 (OEM qty). **Siliconix Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054. (408) 988-8000. **Circle No. 396**

0.8-μm CMOS gate arrays. The TGC1000 and TGC1000LV series consists of 12 arrays ranging from 16k to 455k gates. The TGC1000 arrays operate from 5V, and the TGC1000LV arrays consume 0.8 μW/MHz/gate, operating from 2.7 to 3.6V. The low-voltage arrays have fail-safe input buffers that let you mix 3 and 5V logic. A library contains macros for internal and IEEE-1149.1 scan testing. NRE charges, from \$20,000. **Texas Instruments Inc,** Semiconductor Group (SC-92053), Box 809066, Dallas, TX 75380. Phone (214) 995-6611, ext 3990. **Circle No. 397**

Analog ASIC. The VRSA-Tile RPA-160 analog array consists of 16 tiles in a 4×4 grid pattern. Each tile contains 24 npn and 18 pnp transistors; two Shottky diodes; two programmable MOS capacitors; and 13 programmable thin-film resistors. Macrocells consist of op amps, comparators, multiplexers, analog multipliers, and analog buffers operating as fast as 200 MHz. NRE costs for turnkey designs, \$50,000 to \$75,000. **Raytheon Co,** Semiconductor Div, Box 7016, Mountain View, CA 94039. Phone (415) 968-9211. **Circle No. 398**

One-time-programmable memory. The Am27V010 1-Mbit one-time-programmable memory device operates from 3.3V ±0.3V; it has an access time as short as 200 nsec. Maximum power consumption in standby mode is 90 μW. When you access the device at a 5-MHz rate, the power consumption is 54 mW. The chip comes in a 32-pin plastic leaded

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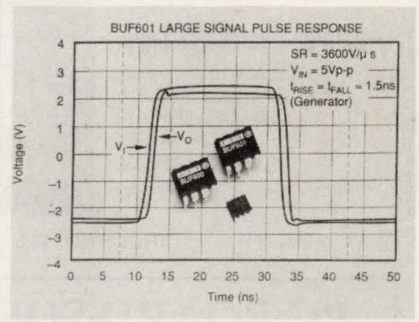
chip carrier, a DIP, or thin SO package. The 200-nsec version, $13.20 (100). **Advanced Micro Devices Inc,** Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400. **Circle No. 399**

ISA bus controller. The VL82C380 ISA bus controller works with 386DX-based systems. It contains an on-chip cache having a look-aside, write-back architecture. The controller maintains coherency during DMA or master-mode transfer cycles, eliminating flushes and invalidations. It can also access 64 Mbytes of external RAM. $20 (OEM qty). **VLSI Technology Inc,** 8375 South River Pkwy, Tempe, AZ 85284. Phone (602) 752-8574. **Circle No. 400**



High-slew-rate buffer amplifiers. The BUF600 and BUF601 monolithic, open-loop, unity-gain buffer amplifiers have a symmetrical slew rate of 3600V/μsec. An automatic quiescent-current control circuit produces a 320-MHz bandwidth at a quiescent current of 3 mA for the BUF600 and 6 mA for the BUF601. The devices have 1.5-nsec rise and fall times, −62-dB total harmonic distortion, and operate from −40 to +85°C. BUF600, from $5.68; BUF601, from $5.83 (100). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. **Circle No. 401**

Motor-control chips. The TDA5340/5341 disk-drive motors drive full-wave brushless DC motors without requiring commutation sensors. They have a voice-coil motor driver, start-up circuitry, and an automatic park procedure. The TDA5341 chip includes a frequency-locked loop to control motor speeds as fast as 6000 rpm. Maximum spindle-drive current is 1.6A. A sleep-mode function draws 200 μA. TDA5340, $7.80; TDA5341, $8.75 (1000). **Signetics Co,** Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000. **Circle No. 402**

Components & Power Supplies

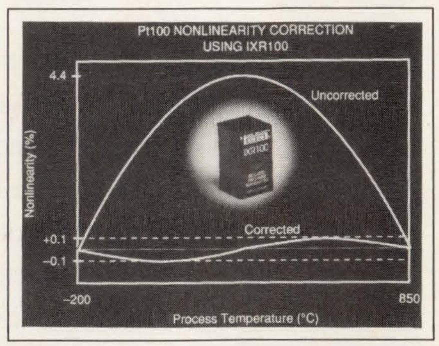
Rotation sensors. TLE Series sensors operate over a −40 to +150°C range and feature reverse polarity and overvoltage protection. The 4921U and 4922U have dynamic mode operation for speed detection and timing applications. The 4971U, 4973U, and 4974U units feature static operation for zero-rotation speed sensing. The 4973U has a 2-lead connection for applications requiring long wire runs; the 4974U offers symmetrical output for applications requiring a 50% duty cycle. \$2.54 to \$2.85 (1000). **Siemens Components Inc,** Integrated Circuit Div, 2191 Laurelwood Rd, Santa Ana, CA 95054. Phone (408) 980-4598. **Circle No. 351**

LCD module. The G2446 module has a 240×64 dot-matrix format and features a built-in controller and dc/dc con-

verter. It incorporates edge lighting. Contrast equals 6:1, and brightness measures 60 cd/m^2. The module's power requirements are 5V at 12 mA; an inverter for the edge lighting requires 5V at 700 mA. Operating range spans 0 to 50°C. \$143 (100). Delivery, stock to eight weeks ARO. **Seiko Instruments USA Inc,** 2990 Lomita Blvd, Torrance, CA 90505. Phone (310) 517-7829. FAX (310) 517-7792. **Circle No. 352**

Thyristors. The C712 is a 2000V, 1000A, 53-mm inverter-grade thyristor. The C770 is a 2000V, 2100A device. Both units feature an interdigitated gate pattern that optimizes the turn-on area for high di/dt capability. C712, \$250; C770, \$550 (1 to 99). **Powerex Inc,** Hillis St, Youngwood, PA 15697. Phone (412) 925-4422. **Circle No. 353**

Two-wire transmitter. The self-powered, IXR100 2-wire transmitter excites and linearizes signals from RTDs and can condition thermocouples while supplying power on a single 4- to 20-mA wire pair. It provides as much as 1500V rms galvanic isolation for industrial sig-



nals in noisy environments. The unit provides matched current sources for sensor excitation. It operates from supply voltages of 36 to 11.6V. From \$49 (100). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. **Circle No. 354**

Elastomeric interconnector. The GN is a strip connector with conductors spaced on 0.1-mm centers. The connector can carry 200 mA/mm^2 with a 0.6-mm-wide electrode. The units come in lengths of 2 to 5 mm and in widths of 2 to 4 mm. $1 per linear inch. **Shin-Etsu Polymer America Inc,** 34135 Seventh St, Union City, CA 94587. Phone (510) 475-9000. **Circle No. 355**

Keypad switches. These switches are available in three versions—12- and 16-position units and a 12-position model with LCD. All units employ conductive rubber switching and are constructed from plastic that has a UL 94V-0 rating. The two circuit codes are decimal and matrix. The 12-position model, $16 (500). **Augat Inc,** Box 779, Attleboro, MA 02703. Phone (508) 222-2202. FAX (508) 222-0693. **Circle No. 360**

Panel switch. The Touch-Tell switch combines a programmable LCD module, tricolor backlighting, driver, and a momentary-action pushbutton switch in a single housing. The display provides a full-screen graphics capability and has 864 pixels in a 24×36 matrix. The spst internal switch is rated for 12V dc at 50 mA and it has a 10^6-cycle lifetime. $49.25. **Cherry Electrical Products,** 3600 Sunset Ave, Waukegan, IL 60087. Phone (708) 360-3483. **Circle No. 356**

DC/DC converters. PKE Series converters are designed for 48 and 60V systems. The line consists of five single-, dual-, and triple-output models. Input-to-output isolation equals 1500V dc and efficiencies range from 80 to 85%. The outputs are short-circuit proof, and the input incorporates a transient suppressor. Dual-output module, $98; triple-output module, $105 (250). **Ericsson Components Inc,** 403 International Pkwy, Richardson, TX 75081. Phone (214) 997-6561. **Circle No. 357**

DC/DC converters. K Triple Series 55W converters feature two separate power sections. Each section operates antiphase to the other to reduce ripple current stress. Efficiencies range as high as 90%. Isolation equals 1544V dc. The units operate over a −25 to +80°C range. $150.50 (100). **Calex Mfg Co Inc,** 2401 Stanwell Dr, Concord, CA 94520. Phone (800) 542-3355; (510) 687-4411. FAX (510) 687-3333. **Circle No. 358**

Indicator lights. Series 5700 indicators feature incandescent and LED illumination in a variety of colors including a red-green bicolor LED. Versions are available for operation with voltages of 5 to 28V, and nominal lamp life equals 25,000 hours. Operating range spans −20 to +75°C. From $0.90 (1000). **C&K Components Inc,** 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400. **Circle No. 359**

VME 4-channel DSP board. The MMI-420 6U VME board contains four 27-MHz 56001 DSP chips. The board encodes 16-bit audio signals at sampling rates of 48 kHz for DAT (digital audio tape) and 44.1 kHz for CD. Each chip has a 16k×24-bit static RAM, 16k×24-bit data memory, and 16-kbyte boot EPROM. The DSP chips and the VMEbus have access to a multiport 4-Mbyte RAM. A variety of daughter boards can access one or more DSP chips. $3225. **Vigra Inc,** 4901 Morena Blvd, Bldg 502, San Diego, CA 92117. Phone (619) 483-1197. FAX (619) 483-7531. **Circle No. 380**

Leather-covered laptop computer. The Notepad 386SX, a leather-covered laptop computer, runs at 20 MHz, is 1.5 in. thick, and fits in a leather portfolio carrying case. The computer comes with DOS 5.0, 2 Mbytes of RAM (expandable to 4 Mbytes), 3.5-in. floppy-disk drive, and options for a 40-, 60-, or 80-Mbyte internal hard-disk drive. A fax/modem, PS/2 mouse, serial and parallel ports and a 4.4-Ahr rechargeable NiCd battery are standard. With 40-Mbyte hard-disk drive, $2995. **Lighthorse Technologies Inc,** 4105 Tolowa St, San Diego, CA 92117. Phone (619) 270-7399. FAX (619) 483-1196. **Circle No. 381**

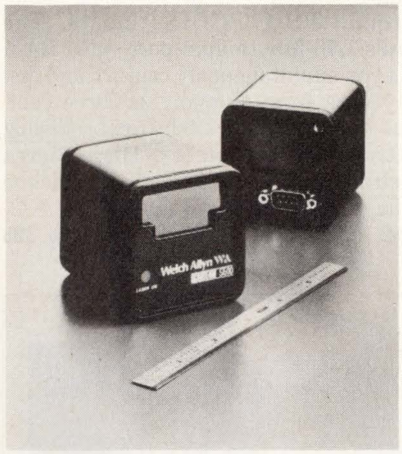
15-in. high-resolution color monitor. The ECM 1560 is compatible with VGA, Super VGA, XGA, IBM's 8514A, and Mac II standards. Digital memory sizing lets you preprogram preferred frequencies. The flat square tube has a maximum resolution of 1024×768 pixels. The Vari-Scan monitor features a 40-MHz bandwidth, 9-pin-analog and 5-BNC-analog input ports, a 0.28-mm dot pitch and a 50- to 100-Hz vertical scan rate. Approximately $1395. **Electrohome,** 809 Wellington St N, Kitchener, ON N2G 4J6, Canada. Phone (519) 744-7111. FAX (519) 749-3131. **Circle No. 382**

SCSI-2 solid-state drive. With a 68020 32-bit microprocessor and a dedicated 40-MHz SCSI-2 processor, the Silicon-Disk Pro achieves an access time of 0.02 msec and a transfer rate of 10 Mbytes/sec. The solid-state drive automatically formats when installed in an IBM, DEC, Sun, DG, SGI, HP, and other SCSI-based systems. Capacity ranges from 8 to 512 Mbytes. $3995 to $58,995. **Atto Technology Inc,** Baird Research Park, 1576 Sweet Home Rd, Amherst, NY 14228. Phone (716) 688-4259. FAX (716) 636-3630. **Circle No. 383**

VGA to video-scan converter. Simulscan converts RGB video-graphics-array (VGA) output to composite RS-170 and S-video formats. The external unit lets you display computer-screen images on a TV or record them on a VCR. The unit converts 640 × 480 VGA pixels into video-formatted signals having 24-bit resolution to display 16 million colors. To install the unit, you unplug the VGA monitor, plug the existing unit into the VGA card, and plug the VGA monitor and TV into the converter. $495. **IEV International Inc,** Visual Information Processing, 3030 S Main St, Suite 300, Salt Lake City, UT 84115. Phone (800) 438-6161; (810) 466-9093. FAX (801) 466-5921.

Circle No. 384

PCMCIA 2.0 industrial interface. The ZT 8921 STD-32 Bus module provides two card slots for memory cards adhering to the PCMCIA (Personal Computer Memory Card International Association) standard. The module also has a 16-kbyte PROM socket for BIOS extensions and comes with Microsoft's Flash File System Version 2.0 device drivers. $485. **Ziatech Corp,** 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. FAX (805) 541-5088. **Circle No. 385**

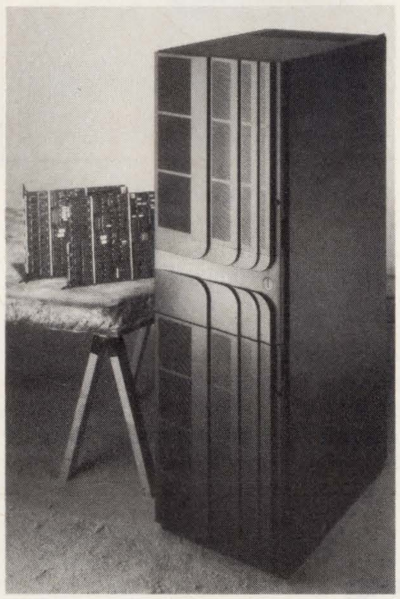


Bar-code scanner and decoder. Scanteam 5600, a fixed-mount, moving-beam, laser-diode-based bar-code scanner, features a compact design for limited mounting spaces; the unit's noncontact scanning suits scanning on curved and irregular surfaces. The scanner measures 2.3 × 2.3 × 2.7 in. You can attach as many as three scanners to the Scanteam 7300 programmable decoder board, which provides a host-computer interface. Scanteam 5600 and 7300, $1195 and $430, respectively. **Welch Allyn Inc,** Data Collection Div, 4619 Jordan Rd, Skaneateles Falls, NY 13153. Phone (315) 685-8945. FAX (315) 685-3172. **Circle No. 386**

Short-range modem. Model 1080 short-range modem communicates synchronously or asynchronously over an RS-232C link. The modem communicates half- or full-duplex over a distance of 13 miles at data rates from 1.2 to 19.2 kbps. You can initiate local analog-loopback or remote digital-loopback test via the front panel switch or the RS-232C link. You can also set the RTS-to-CTS delay to 7 or 53 msec. $295. **Patton Electronics Co,** 7958 Cessna Ave, Gaithersburg, MD 20879. Phone (301) 975-1000. FAX (301) 869-9293.

Circle No. 387

SBus frame grabber. A single-slot SBus frame grabber, Data Cell S2200, provides real-time 24-bit color image capture and display. The card accepts composite video/S-Video (NTSC/PAL), analog RGB/YUV, or multiple monochrome (RS-170/CCIR) inputs. The card's 1.75-Mbyte dual-port video RAM lets you simultaneously capture and display data from as many as three cameras in real-time. $5499; Itex or Visilog software also available. **High Sierra Technologies Inc,** 749 Kelly Dr, Incline Village, NV 89450. Phone (702) 832-0792. FAX (702) 832-0778. **Circle No. 388**



Unix-network server. The NS 5500 Netserver, configured for eight Ethernets, can process more than 2250 I/O operations/sec. A multiprocessor architecture separates network file- and disk-management functions and allocates them to specialized processors. Three storage processors control 30 SCSI channels and 81 Gbytes of disk storage. $124,900; with redundant power supply, $149,000. **Auspex Systems Inc,** 2952 Bunker Hill Lane, Santa Clara, CA 95054. Phone (408) 492-0900. FAX (408) 492-0909. **Circle No. 389**

Color text terminal. TR-170 terminals contain a firmware driver that allows them to run Software Link's PC-MOS operating system. Twenty-five TR-170 terminals can share a single DOS-compatible computer. The terminals run VGA text mode and feature a 14-in. nonglare CRT. A multipage feature stores eight application-session pages, allowing you to hot-key between sessions. $895. **Relisys,** 320 S Milpitas Blvd, Milpitas, CA 95035. Phone (408) 945-9000. FAX (408) 945-0587. **Circle No. 390**

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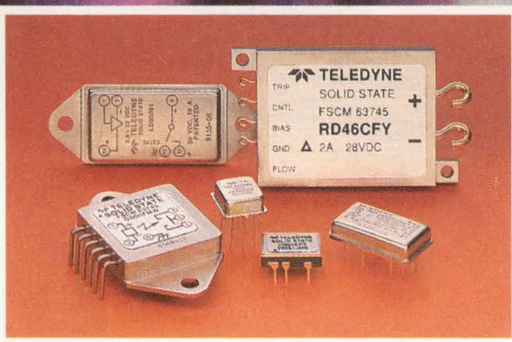

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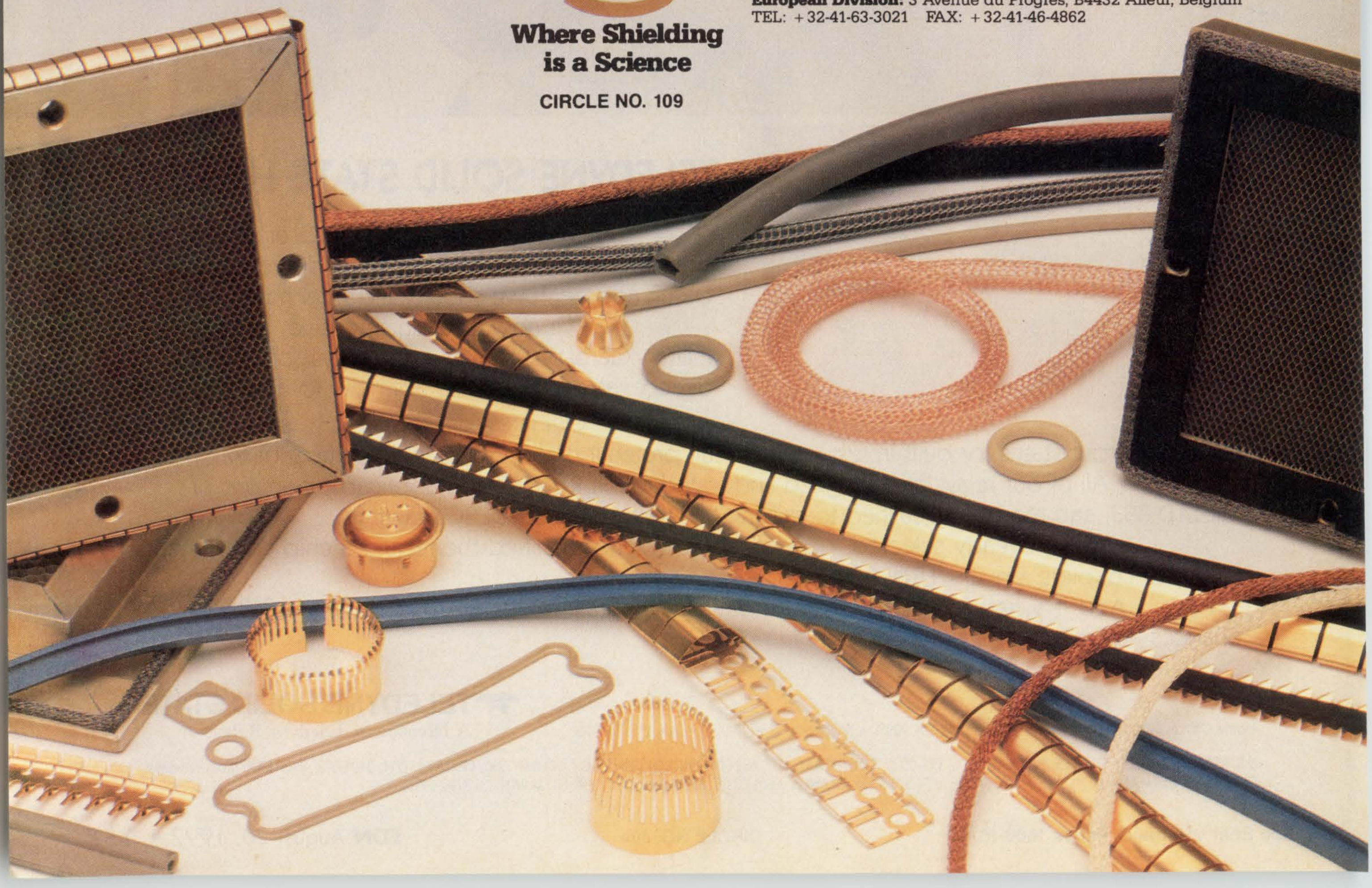


Test & Measurement Instruments

3½-digit DMM for less than $30. The DM2 weighs 7 oz and is the size of a deck of cards. It measures dc current with 0.1-μA resolution on its most sensitive range and checks diodes. Other functions include measuring dc volts to 1 kV, ac volts to 500V, resistance to 2 MΩ, and dc current to 200 mA. Accuracy is 0.8%. A fuse protects the current ranges. The meter comes with a manual, test leads, and a spare fuse. $27.95. **Beckman Industrial Corp,** 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 495-3200. FAX (619) 268-0172. TLX 249031. **Circle No. 363**

Data-acquisition-and-control system. The SI-100, which mounts in a 19-in. EIA rack, is programmable via an RS-232C port. It transmits all of its data via an RS-422 interface at any rate from 0 to 6 MHz. The unit accepts from 1 to 16 modules. Analog-input modules have eight channels. You can vary each channel's gain over a range of 0.8 to 100 and its offset to ±2.5V. The A/D converter takes a maximum of 500 ksamples/sec (total for all channels) and produces data with a selectable resolution of 8 to 12 bits. You can vary the sampling rate of any one channel from 0.12 to 62.5 ksamples/sec. As you vary the sampling rate, you also vary an antialiasing filter's cut-off frequency. For each channel, you can select a filter that has flat, Bessel, or elliptic response. Analog output modules have eight channels, each with a 12-bit multiplying DAC. Digital I/O modules have 24 channels each. From $7200; channels cost $400 to $1100, depending on how many you order. **Sheldon Instruments,** Box 877, Orem, UT 84509. Phone (801) 376-7861. FAX (801) 374-8022. **Circle No. 362**

60-MHz analog-digital oscilloscope. The 2212 operates as a DSO with two channels, 8-bit resolution, 4 kbytes/channel of memory, and a 20-Msample/sec acquisition rate. For viewing signals faster than 10 MHz, it converts at the touch of a button to an analog scope. The unit provides automatic setup; setup storage; cursor measurements of voltage, time, and frequency; an X-Y display mode; and a parallel printer interface. $2495; IEEE-488 and RS-232C options, $300. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 361**

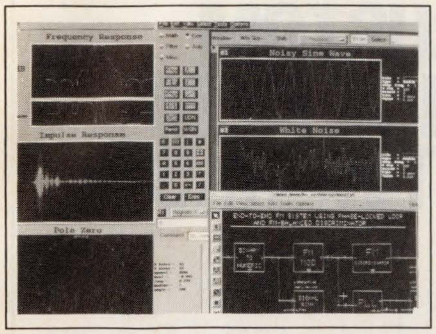
4-channel, 50-MHz arbitrary-waveform generator. The Model 295, which uses direct digital synthesis, provides frequencies accurate to 2 ppm. Channels can operate independently, or you can lock their frequency and phase to the master channel. For example, this capability lets the generator accurately synthesize 3-phase voltages. Nonvolatile memory stores 10 standard waveforms; 30 more waveforms are furnished on a 3½-in. disk. You can create waveforms by entering mathematical expressions, or by drawing with a mouse. Each channel's memory is 32k points (128k optional). Operating modes include continuous, triggered, burst, gate, and sweep. The unit can add waveforms and can produce amplitude- and suppressed-carrier-modulated waveforms. $5995 (one channel) to $18,410 (four channels with all options). Delivery, 4 to 6 weeks ARO. **Wavetek Corp,** 9045 Balboa Ave, San Diego, CA 92123. Phone (619) 279-2200. **Circle No. 364**

Harmonic analyzer. The TCI 5-19 measures harmonic distortion in 60-Hz power-distribution systems. (A 50-Hz version is also available.) The handheld, battery-powered, μP-based unit, which is supplied with voltage probes and a 1000A clamp-on current transformer, displays five functions of the first 19 harmonics on a graphical LCD screen. The unit works with voltages to 1 kV. $1895; thermal recorder for waveforms, $400. **Trans-Coil Inc,** 7878 N 86th St, Milwaukee, WI 53224. Phone (800) 824-8282; (414) 357-4480. FAX (414) 357-4484. **Circle No. 365**

Handheld 2-channel, audio frequency analyzer. The 3569A functions as a sound-level meter, a real-time sound-intensity meter, an octave analyzer, a ⅓-octave analyzer, a 2-channel FFT analyzer with a 20-kHz frequency span, and a reverberation-time analyzer that computes reverberation times in octave and ⅓-octave bands. The unit accepts inputs directly from microphones; it can store calibration factors for 15 microphones. With a $250 utility package, it can transfer data to the vendor's Model 95 palmtop PC, which can store the data on RAM-disk cards. $13,000; FFT- and reverberation-time analysis require the installation of $2000 options. Delivery, 8 weeks ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 366**

Debug support for Microtec C compiler on 68K and Z180. The debugger that is integrated with the 68000 UEM in-circuit emulator now includes source-level-debugging support for Microtec Research's C compiler on the 68000 and Z180 μPs. This integrated package also supports compilers from several other vendors. $5500. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. FAX (410) 381-3253. **Circle No. 367**

PC-based test tools for boundary-scan pc boards. Asset 1.2, which runs on 80386-and i486-based PCs, allows quick design verification and debugging of pc boards that incorporate a boundary-scan interface conforming to IEEE-1149.1. The software supports a scan-path selector and linker, and it permits importing device- and board-level vectors in the TSSI format. Test system, $7495; diagnostic system, $13,495; scan-function library, $2495; boundary-scan demonstration module, $695; general demonstration module, $995. **Texas Instruments Inc,** Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 3990; outside the US, (214) 995-6611, ext 3990. **Circle No. 368**



DSP design system. Additions to the DSP Framework version 3.0 include the Signal Calculator, the Hardware Design System option, the Simulation Toolset, and the Filter Design System. Base price for Sun-4, DECstation, and HP/Apollo workstations, $25,000. **Comdisco Systems Inc,** 919 E Hillsdale Blvd, Foster City, CA 94404. Phone (415) 574-5800. FAX (415) 358-3601. **Circle No. 369**

Autosketch for Windows. You can use the Autosketch illustration tool for technical illustration, architectural drafting, engineering drawings, flowcharts, and information graphics. The program comes with more than 2000 predrawn symbols and stores files in a DXF format. Autosketch for Windows 3.0 or higher, $299; update, $75. **Autodesk Retail Products,** 11911 North Creek Pkwy S, Bothell, WA 98011. Phone in US and Canada, (800) 228-3601; (206) 487-2233. FAX (206) 483-6969. **Circle No. 370**

Fax management under Unix. Replix Unix-based fax-management software allows you to send, receive, route, view, and manage faxes from your desktop computer. It runs with Sun-3, SPARC, IBM AIX RS/6000, HP 700, SCO Unix, ISC Unix, and Samsung i860 workstations. Base price, $2395. **Samsung Software America,** 1 Corporate Dr, Andover, MA 01810. Phone (508) 685-7200. FAX (508) 685-4940. **Circle No. 371**

Programming tools for board tester. The Test Xpress set of PC Unix-based software tools speed programming for test of pc boards on the GR228X tester. The set consists of three tools. ATG Xpress is a test-program development environment; Wave-Link, a waveform editor, takes simulation vectors from a design simulator, reformats them and produces in-circuit programs for the tester; and FS-ATG generates test programs for PAL devices, PLDs, and PGAs, accounting for device types, package styles, and board-level constraints. ATG Xpress, $12,500; Wave-Link, $15,000; FS-ATG, $4600. **GenRad Inc,** 300 Baker Ave, Concord, MA 01742. Phone (508) 369-4400, ext 2970. **Circle No. 372**

CAD/CAM developers' kit. Release 11 of the CAD/CAM Developers Kit/DXF is a library of C functions that reads and writes Release 11 DXF files with a few lines of C language code. The kit runs with the following compilers: Microsoft C 5.1 and 6.0; Borland Turbo C 2.0 and C++; Metaware C 386 1.6; and Watcom C 386 8.0, 8.5, and 9.0. Personal edition for in-house use only, $599; professional edition including royalty-free distribution rights, $1199. **Building Block Software,** 371 Moody St, Waltham, MA 02154. Phone (617) 899-4350. **Circle No. 373**

Modeling and simulation for packaging designs. Aztec System models and simulates advanced electronic-packaging designs. The system provides accurate prediction of pulse shape, delay, and crosstalk. Magnetic properties of the interconnections are accounted for in calculating frequency-dependent inductance and skin-effect resistance matrices. From $35,000; individual modules, from $10,000. **Arizona Packaging Software Inc,** 1840 E River Rd, Suite 100, Tucson, AZ 85718. Phone (602) 577-8886. FAX (602) 577-0687. **Circle No. 374**

Signal-analysis software. The Xmath signal-analysis module (SAM) provides a library of signal-processing and communications-analysis functions for Xmath. Using Xmath's object-oriented architecture helps to speed up analysis. Signals are represented by objects called parameter-dependent matrices. For SPARCstation or DECstation, from $6000. **Integrated Systems Inc,** 3260 Jay St, Santa Clara, CA 95054. Phone (408) 980-1500. FAX (408) 980-0400. **Circle No. 375**

Unix software-engineering package. Treesoft 2.1 applies a tree structure to the development and maintenance of application and real-time software written under one or more programming languages. The package provides project modeling; generation of makefiles; graphical viewpaths; configuration management; testing of unit, integration, and regression; reusability; problem-report management; profiling; project communications; and report generation. Software for Sun-3 and Sun-4 workstations, $8500. **+1 Software Engineering,** 2510-G Las Posas Rd, Suite 438, Camarillo, CA 93011. Phone (805) 389-1778. **Circle No. 376**

Cost model for ASICs. Using the ASIC Standard Cost Model to calculate the manufacturing cost and estimate the fair market value for an ASIC device allows you to make design/cost trade-offs. The program calculates costs for CMOS gate-array, standard-cell, and full-custom designs. For PC or Macintosh computers, $1995. **Valence Associates,** Box 14932, Fremont, CA 94539. Phone/FAX (510) 651-5453. **Circle No. 377**

PC telecom software. Crosstalk Communicator 2.1 enables PC users to communicate with other personal computers, bulletin-board and on-line services, and minicomputers. This revision includes a split-screen "chat" utility and an archive-file content viewer. $99; upgrade, $20. **Digital Communications Associates Inc,** 1000 Alderman Dr, Alpharetta, GA 30201. Phone (800) 348-3221; (404) 442-4521. FAX (404) 442-4364. **Circle No. 378**

Test-loaded pc boards. The 9400-401 CAD-MAP program uses CAD system ASCII output to reduce test-preparation time after fixturing. It converts the CAD database into a set of test files that are ready to debug with the company's 9420 manufacturing-defects analyzer. The program also provides test-fixture build specifications from the CAD database. $2495. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. **Circle No. 379**

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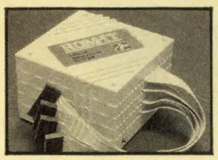

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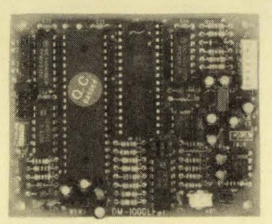

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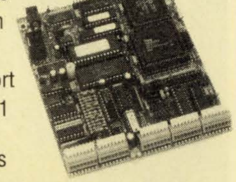

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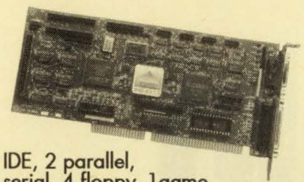

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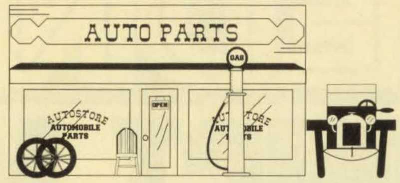

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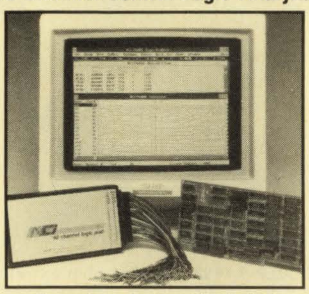

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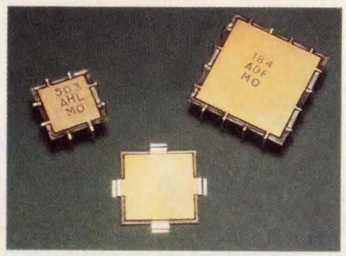

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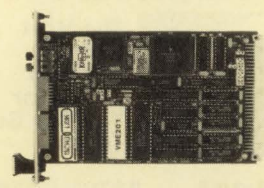

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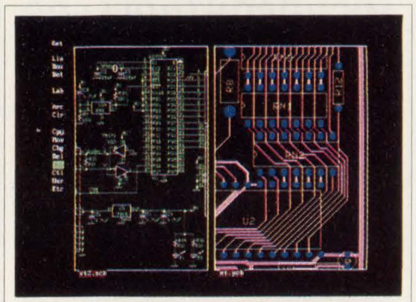

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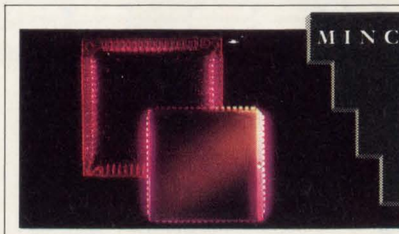

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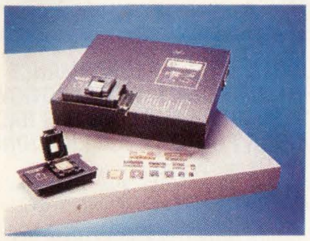

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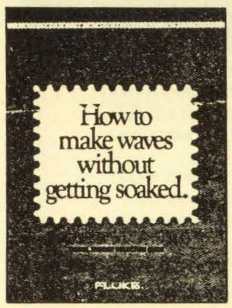

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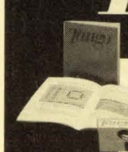

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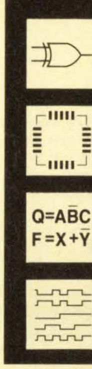

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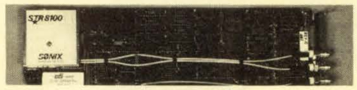

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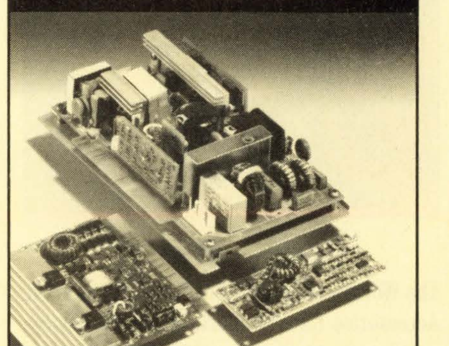

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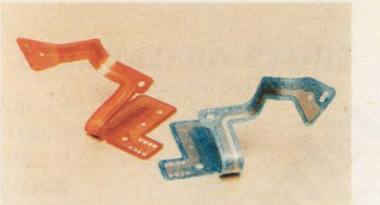

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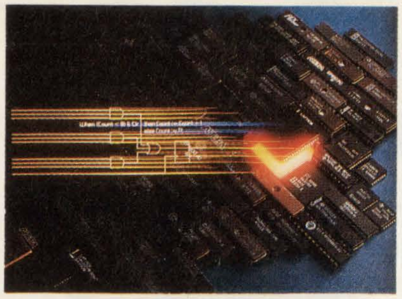

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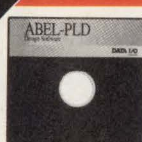

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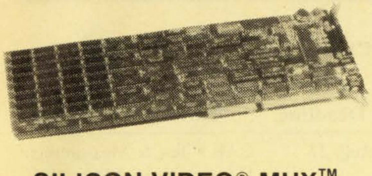

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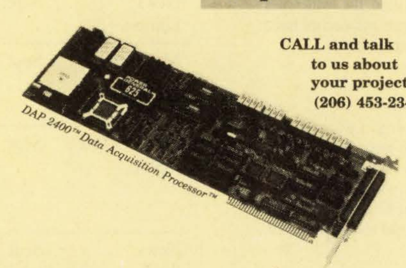

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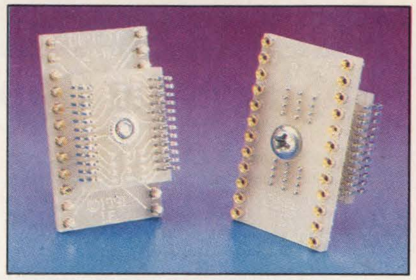

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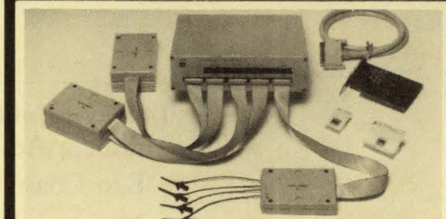

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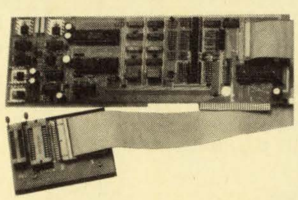

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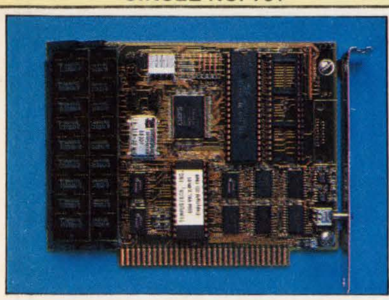

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SOFTWARE ISSUE	Sept. 17	Aug. 27	SOFTWARE ENGINEERING SPECIAL ISSUE (To be polybagged with the Sept. 17th Magazine Edition issue)
News Edition	Sept. 24	Sept. 10	Automotive Electronics Sensors • Computers & Peripherals • Regional Profile: Oregon, Washington
Magazine Edition	Oct. 1	Sept. 10	TEST & MEASUREMENT SPECIAL ISSUE • European Technology Update • Data Acquisition Software • Superconductors • How to Design it Right the 1st Time Series—Part I PLD/FPGA Directory
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We are currently seeking an experienced technical professional to coordinate and supervise a staff of 10-12 Engineers in the design of hardware and software to support transit and railroad innovations. You'll provide technical direction for developing digital/analog hardware and real-time control software, interfacing with customers, consultants and management, as well as oversee group budgeting. We require a creative, results-oriented BS/MSEE with a strong record (7+ years) of technical and supervisory experience, able to bring personal leadership and technical supervision together to achieve dynamic results.

GRS offers excellent compensation, including relocation assistance, strong benefits and outstanding growth potential. ***Please send or fax your resume to: Human Resources Dept. 2, General Railway Signal Corporation, P.O. Box 20600, Rochester, NY 14602-0600; fax (716) 783-2099.***

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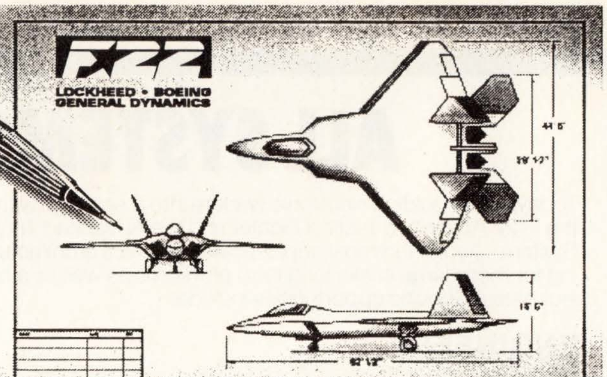

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Consider your options. Plot your strategy. Make your move. Your next decision could put you among a select group of engineers assigned to the F-22 Advanced Tactical Fighter. General Dynamics Fort Worth Division is working on engineering and manufacturing development of the F-22 Advanced Tactical Fighter as part of a three-company team with Lockheed and Boeing. The Air Force plans to procure the F-22 to replace the current F-15 Eagle air superiority fighter. The F-22 production phase will begin in 1996 and extend to the year 2014. Your next move could put this project within your reach.

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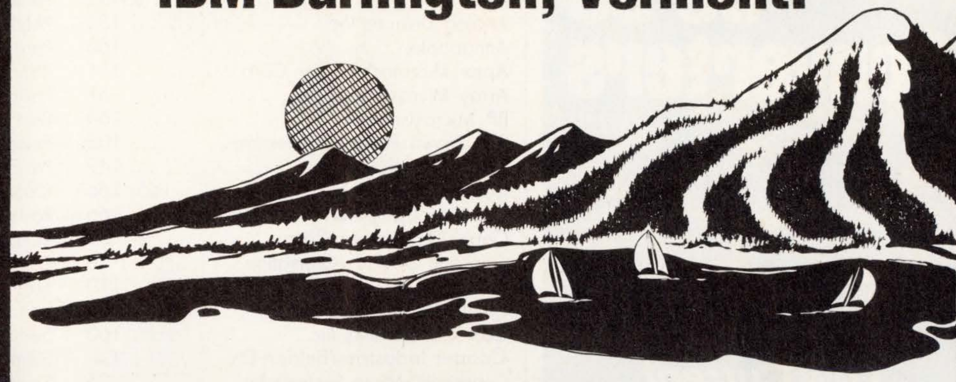

One of the world's most advanced semiconductor operations is what you'll find at IBM's major development and manufacturing facility in Burlington, where continued business growth is matched by a superb living environment. We now have outstanding career opportunities for engineers with the specialized computer skills to make significant impact on RISC microprocessor development.

Logic Design

Responsible for definition, logic design and verification of high performance RISC microprocessors. To qualify, you must possess a BSEE or higher, with an emphasis on Computer Engineering, and be capable of carrying logic design through to physical chip design stage. Minimum of 3 years in logic/chip, CMOS and VLSI design required. RISC experience is key. Background in microprocessor and multiprocessor design desirable.

Circuit Design

Will design CMOS circuitry for RISC-based microprocessor functions. Includes custom SRAM cache design, complex logic dataflow circuitry, random logic, IO, clocking and other circuitry in custom microprocessor layouts. Requires BSEE or higher with emphasis on Computer Engineering or Circuit Design. Ability to design complex CMOS or Bi CMOS circuits and perform circuit analysis and verification is essential, along with minimum of 3 years circuit design experience in industry. CMOS, VLSI, digital circuit design is a prerequisite.

Physical Design

Responsible for CMOS VLSI chip physical design of RISC microprocessor in advanced CMOS technology. Includes using state-of-the-art CAD tools to perform chip layout, wiring and chip timing analysis. A BSEE or higher, with emphasis on Computer Engineering or Circuit Design, is essential, along with at least 3 years of physical design experience in industry. RISC and CMOS, VLSI design experience (chip layout/wiring) necessary. Background in microprocessor design desirable.

Located between Lake Champlain and Vermont's Green Mountains, Burlington offers year round recreation and open space. Unspoiled beauty, affordable housing and a sense of community come together here. This is life at its most enjoyable; technology at its best.

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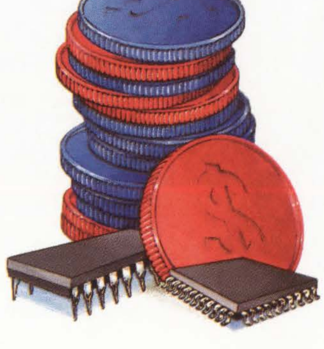
Every company experiences finger pointing when a design doesn't work.

Your circuit designers claim the models are not accurate. The model developers claim the process shifted since the time they began work on the models. The process engineers claim the model developers aren't tracking the process.



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