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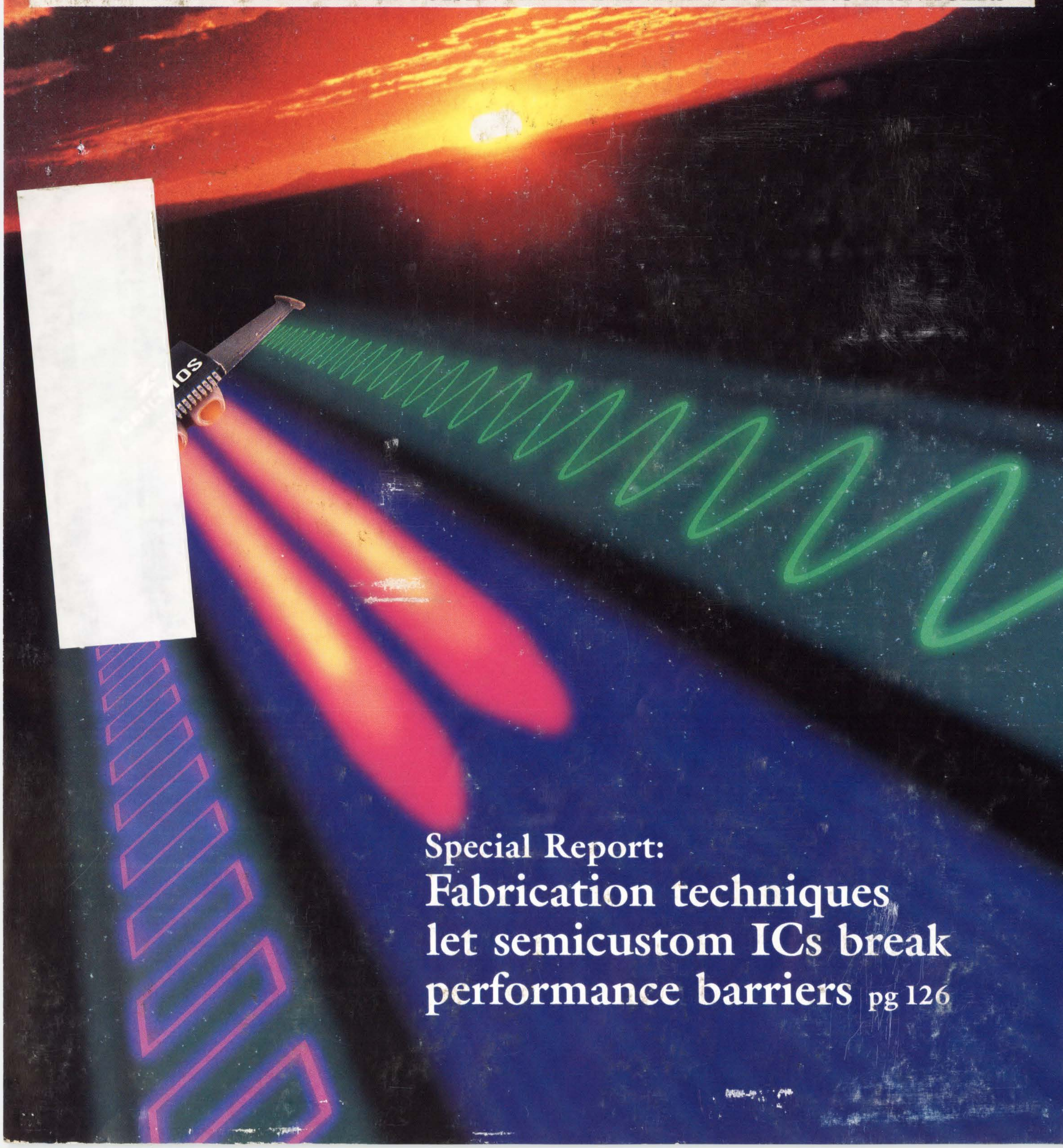
EDN®

ASIC SPECIAL ISSUE

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Special Report:

Fabrication techniques let semicustom ICs break performance barriers pg 126

Our Model 91 will make your pulse race and help you function better.

Introducing the latest member of the 90 Series family: Model 91 Synthesized Pulse Function Generator. It delivers functions and pulses to 20 MHz with five digit frequency accuracy. Out the rear it has pulses to 50 MHz and a 100 MHz clock output. Choose ECL, CMOS or TTL levels, or set your own.

The functions and pulses can be swept or modulated, and there is even GPIB programmability. Plus an external frequency input that lets you use the Model 91 as a frequency counter.

With all these capabilities, Model 91 redefines the concept of an all-purpose benchtop instrument.

About all it doesn't do is generate arbitrary waveforms, but there's the Wavetek Model 95 Synthesized Arbitrary Function Generator for that.

Of course if you want even greater pulse generation capability, our four-channel Model 869 is among the most accurate pulse generators in the world.

For more information about our multi-purpose function generators, high performance pulse generators, or test development and arbitrary waveform software, call Wavetek at 1-800-874-4835.

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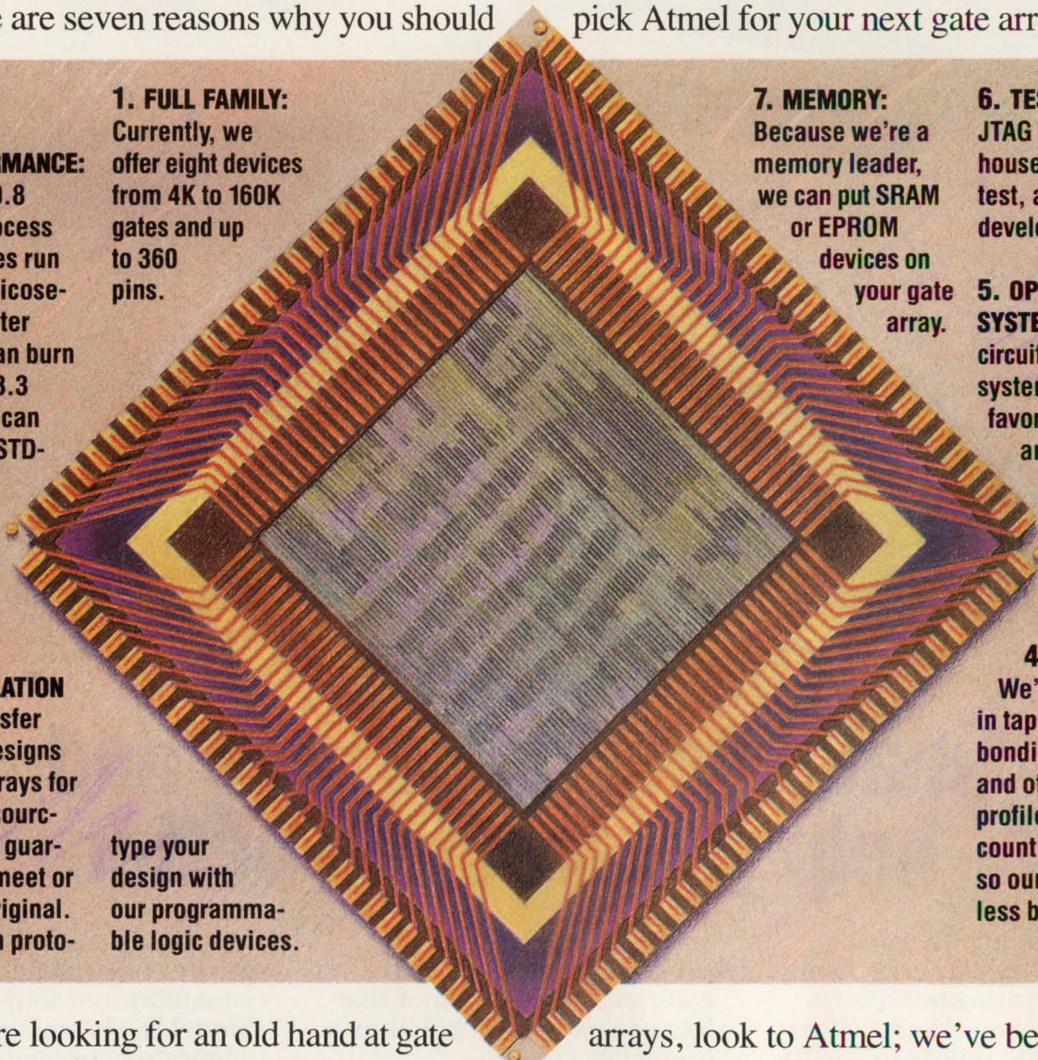
ATMEL GATE ARRAYS OPEN TO THE PUBLIC

Atmel engineers have been successfully making gate arrays for some of the world's biggest computer makers for more than a decade. That's some 650 different personalizations. Now we are offering our latest generation to the public.

Here are seven reasons why you should pick Atmel for your next gate array.



1. FULL FAMILY: Currently, we offer eight devices from 4K to 160K gates and up to 360 pins.

2. PERFORMANCE: We use a 0.8 micron process so our gates run fast (260 picosecond inverter delays), can burn less fuel (3.3 Volts) and can meet MIL-STD-883C.

3. TRANSLATION EASE: Transfer existing designs into our arrays for alternate sourcing. Atmel guarantees to meet or beat the original. Or, you can prototype your design with our programmable logic devices.

4. PACKAGES: We're a leader in tape automated bonding (TAB) and other low-profile, high-pin-count packages, so our arrays use less board room.

5. OPEN DESIGN SYSTEM: We make circuits, not design systems. Use your favorite hardware and software.

6. TEST PROOF: JTAG eases in-house system test, and cuts test development time.

7. MEMORY: Because we're a memory leader, we can put SRAM or EPROM devices on your gate array.

So, if you're looking for an old hand at gate arrays, look to Atmel; we've been making great arrays for almost as long as they've been around. Call, write or FAX us to get our latest gate array literature.

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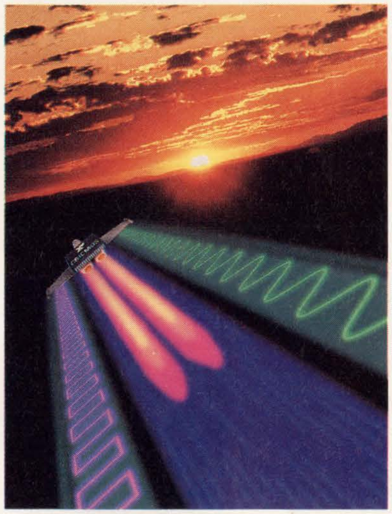
CIRCLE NO. 34

EDN Magazine Edition

Volume 36, Number 18

September 2, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Manufacturers of semicustom circuits are implementing processing technologies that yield faster operating speeds, wider bandwidths, and greater circuit densities. With their capabilities and ease of implementation, today's semicustom ICs soar to a new level in your high-performance applications. See our Special Report on pg 126. (Photo courtesy Exar; concept, Ilhan Refioglu; art direction, Yashi Okita; photography, Tom Skrivan)*

ASIC SPECIAL ISSUE

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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FLUKE AND PHILIPS – THE GLOBAL ALLIANCE IN TEST & MEASUREMENT

FLUKE® PHILIPS PHILIPS

70 SERIES II

8 New Meters. 8 Old-Fashioned Values.

Introducing Fluke's 70 Series II, next-generation multimeters that meet the increasing demands of your job and your budget.

Consider. At the top of the line, the new Fluke 79 and 29 deliver more high-performance features – capacitance, frequency, a fast 63-segment bar graph, Lo-Ohms range, Smoothing™, faster ranges – than DMMs costing much more.

At the entry level, the new model 70, Fluke's lowest-priced DMM ever, delivers unparalleled Fluke quality at a price comparable to "disposable" meters.

And in between are all the models that have made the 70 Series the most popular DMM family in the world – updated, refined and delivering even more value than ever.

"BASICS" REDEFINED

No matter which 70 Series II you choose, you get simple, one-handed operation. High resolution. And built-in, go anywhere reliability.

Automatic Touch Hold® – standard on every model – locks the reading on the display and signals you with a beep, automatically updating for each new measurement without a reset. Leaving you free to concentrate on your work, not on your meter.

YOUR BEST CHOICE

Best of all, every 70 Series II is a Fluke, backed by a worldwide service network and an industry-leading 3 year warranty.

So the next time you're in the market for a new meter, ask for the one that guarantees old-fashioned value. Fluke 70 Series II. For more information call **1-800-6789-LIT**. Or call 1-800-44-FLUKE, ext 33 for the name of your nearest Fluke distributor.

Fluke 79 Series II & 29 Series II
$185*
4000 Count Digital Display (9999 in Hz & ⊣⊢)
63 segment Analog Bar Graph
0.3% Basic DC Voltage Accuracy
Automatic Touch Hold®
Diode Test, Audible Continuity Beeper
Autoranging, Manual Ranging
Holster with Flex Stand™
Frequency Counter to over 20 kHz
Capacitance 10 pF to 9999µF
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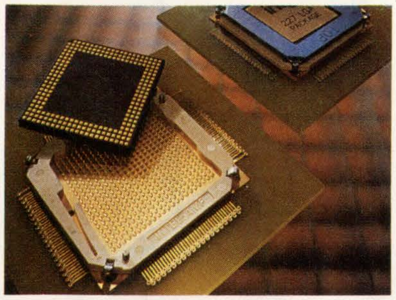
79/77/75/73/70 for measurements to 4800 V-A.
29/23/21 for higher energy measurements.
*Fluke 70 Series II suggested U.S. list prices range from $69 to $185.

FLUKE®

CIRCLE NO. 35



***A variety of housings for ICs** are making them easier to place in any design. Higher pin counts, increased packing densities, and the use of surface-mount technology make specialized IC packages viable options to the standard DIP (pg 63).*

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

Express Request

TECHNOLOGY UPDATES

EDITORS' CHOICES

PRODUCT UPDATE

Continued on page 9

Cahners Publishing Company, A Division of Reed Publishing USA □ Specialized Business Magazines for Building & Construction □ Research □ Technology □ Electronics □ Computing □ Printing □ Publishing □ Health Care □ Foodservice □ Packaging □ Environmental Engineering □ Manufacturing □ Entertainment □ Media □ Home Furnishings □ Interior Design □ and Lodging. Specialized Consumer Magazines for Child Care □ Boating □ and Wedding Planning.

Continued from page 7

DESIGN IDEAS

EDITORIAL

These days, you need to spend just about the same amounts for hardware and software development. If you don't, it will cost you.

NEW PRODUCTS

PROFESSIONAL ISSUES

At the next technical conference, don't just sit there.—*Jay Fraser, Associate Editor*

DEPARTMENTS

EDN BBS Update

EDN continues to upgrade the Bulletin Board System (BBS) to make it easier for you to access the information you need, when you need it. The BBS ((617) 558-4241) now has a 220M-byte drive, courtesy of Quantum. The expanded disk space accommodates more than 80 new public-domain and shareware postings. And four modems mean you don't have to wait to get on line. In the Design Ideas section, we've increased the software coverage. We also recently launched new Special Interest Groups for FPGAs, DSPs, and PLDs. Stay tuned for our 9600-baud and MNP-5 error-correcting modems, which are in the works.

And Speed Were
rd Combination.

AMD Presents The MACH™ Family Of High Speed, High Density PLDs.

Nothing can squash an elegant, high density design faster than a slow, unpredictable and expensive PLD. That's why we've developed the MACH PLD family—for both density, and speed.

The MACH family gives you everything you need in a PLD on state-of-the-art CMOS: Densities up to 128 macrocells or 3600 equivalent gates. Clock speeds up to 66.7 MHz. And absolutely predictable, worst-case delays as low as 12ns per 16 product term macrocell.

And they work for peanuts. The MACH family can bring your costs down as low as a penny per gate—up to 40% less than other high density PLDs.

Model Number	Equiv. Gates	Macro Cells	Max. Delay	System Speed	I/O Pins	Hard-Wired Option
MACH 110	900	32	12ns	66.7 MHz	44	MASC 110
MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120*	1200	48	15ns	50 MHz	68	MASC 120
MACH 220*	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230*	3600	128	15ns	50 MHz	84	MASC 230

*Available Q4 1991.

With the MACH family you'll get to market faster, too. Because it's supported by most popular design tools: Including ABEL,™ CUPL,™ LOG/iC,™ MINC, OrCad,® and AMD's own PALASM® software. There's also hardware and software support from over 20 additional FusionPLD partners.

Every MACH part migrates easily to a pin-compatible hard-wired MASC™ counterpart—for high volume orders with no redesign, no NRE, no performance glitches, no problems.

So don't horse around with slow, unpredictable, high density PLDs—start designing with the MACH family from AMD. Call **1-800-222-9323** for more information.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088

CIRCLE NO. 37

How Orbit's Fores
Out of IC Deve

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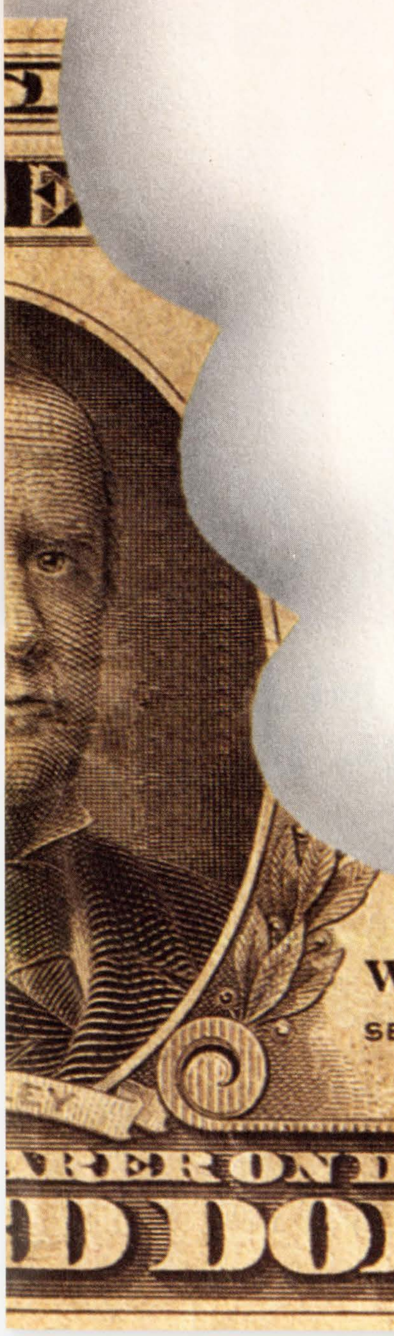
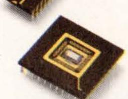


Foresight Makes Silicon Affordable.

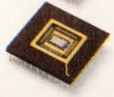
Lower your ASIC development costs with Foresight, the multi-project wafer service with guaranteed quick turnaround.

Foresight is Available:

In 36 different CMOS Processes



With feature sizes down to 1.2 microns



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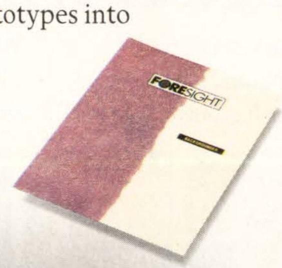
Take the Bite Out of Mixed Signal IC Design.

Partition your analog/digital ASICs—and separately design and verify critical segments through fabrication—with Tiny Chips. You'll dramatically reduce NRE costs and move confidently and quickly from prototypes into production.



Ready. Set. Fab.

Foresight runs start every two weeks, so you can meet even the tightest deadlines—whatever your design rules.

Foresight Run Schedule: 1991		
Apr 10, 24	May 8, 22	Jun 5, 19
Jul 3, 17, 31	Aug 14, 28	Sep 11, 25
Oct 9, 23	Nov 6, 20	Dec 4, 18

Save Time and Money.

Call Orbit Semiconductor for the information you need to get started. Contact Technical Marketing, Orbit Semiconductor, 1230 Bordeaux Dr., Sunnyvale, CA 94089. Or call (408) 744-1800 or (800) 331-4617. In CA (800) 647-0222. Fax (408) 747-1263.

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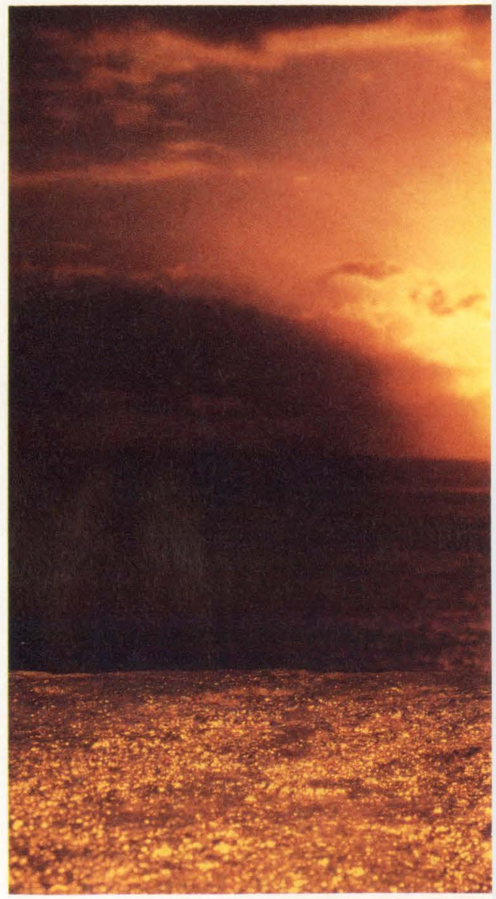
CIRCLE NO. 38

What others promise, we guarantee.

CIRCLE NO. 39

You have to build a to build just

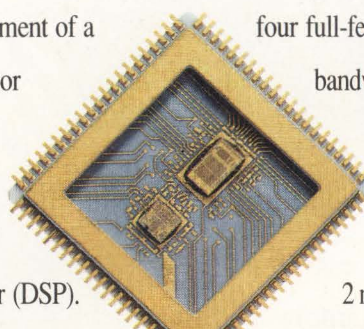


The new Tek TDS Series

More than a million Tektronix oscilloscopes have all been leading up to this: the most powerful, versatile, and intuitive instruments ever developed for the mainstream of test and measurement.

The new TDS 500 Series is the culmination of everything Tek has learned in the design, manufacture and use of digitizing oscilloscopes. It's an achievement made possible only by the unique integration of acquisition functions and combinational trigger logic onto a single board.

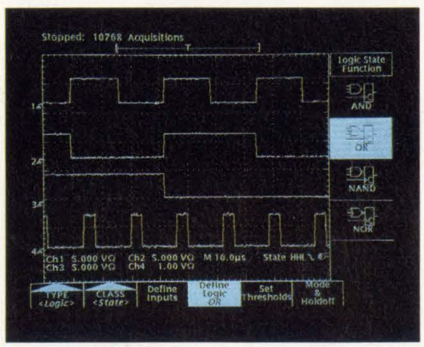
Only by the development of a milestone multiprocessor architecture.



Only by the addition of Tek's TriStar™ Digital Signal Processor (DSP).

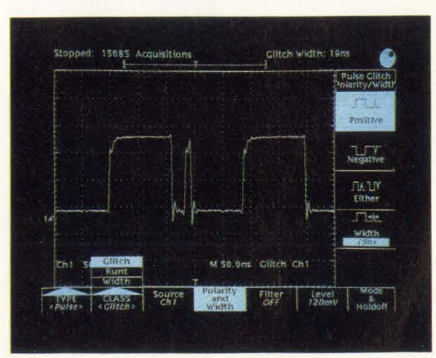
Only by Tek's capacity for taking the hard work out of high performance.

The TDS Series performs, *live*, updates and measurements that inhibit most other digitizing scopes. Its real-

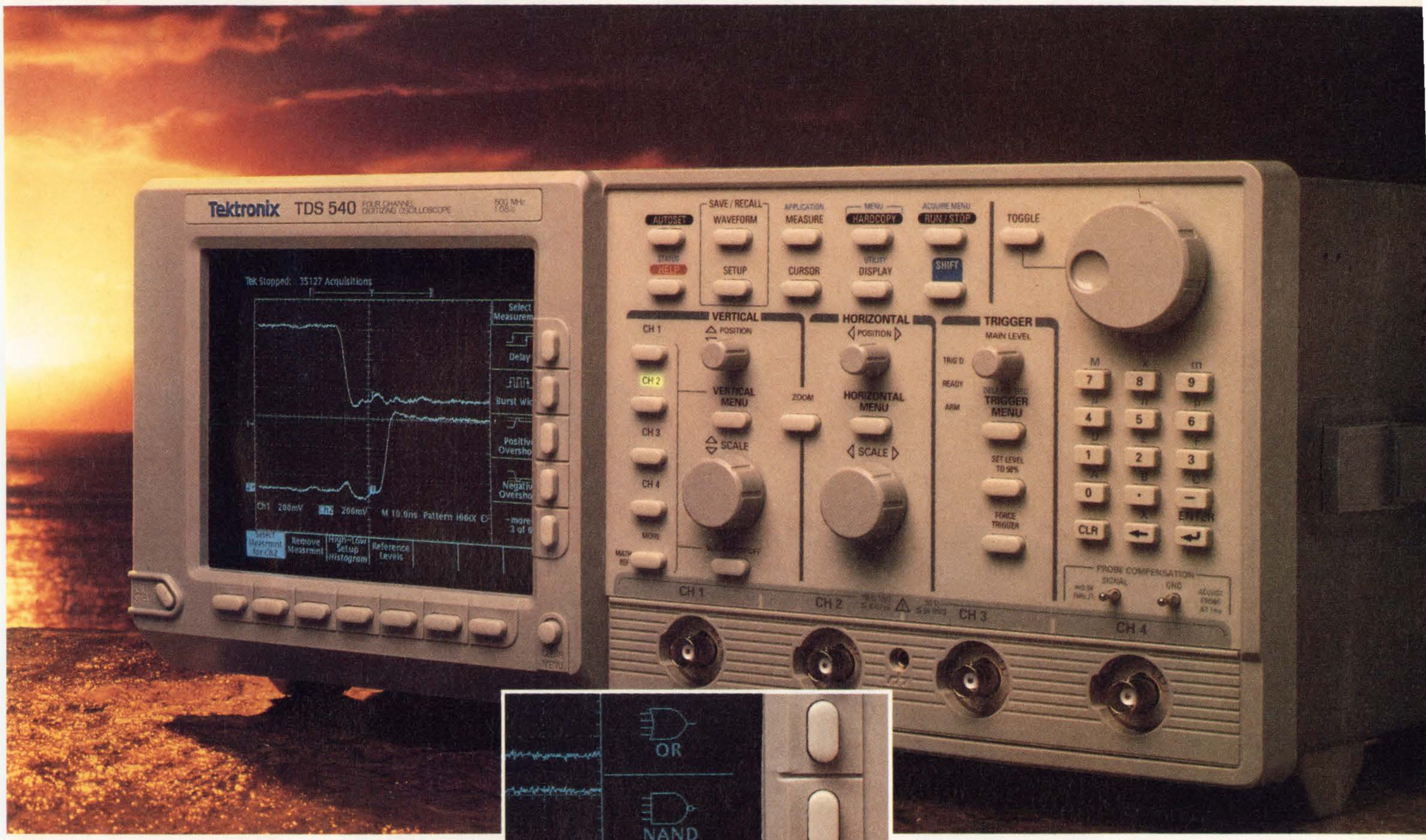


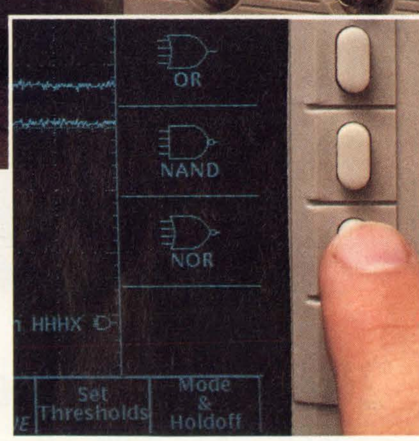
time DSP lets you perform single-shot averaging and extend resolution to 12 bits. The TDS Series arms you with up to four full-featured channels. 500 MHz bandwidth. Up to 1 GS/s sampling and 4 ns peak detect. Up to 50K record lengths. Time interval, 2 ns glitch, runt, pattern and state triggers. With acquisition sensitivity and fast overdrive recovery bringing greater waveform detail within your grasp.

And if you think oscilloscopes aren't as easy to use and comprehend as they



million oscilloscopes one like this.





could be, you owe yourself a demo of the TDS. Its simplified front panel, VGA-quality display resolution, on-line help text, innovative icons that instantly differentiate menu functions — all add up to a scope that makes the user's manual more a formality than a necessity.

The TDS Series signals the start of a new generation of friendlier, more powerful instruments from the world's leading supplier of digitizing and analog oscilloscopes. To get a first-hand feel for why performance like this only comes along about once in a million scopes, contact your Tek sales engineer or call **1-800-426-2200.**

One company measures up.

Tektronix
COMMITTED TO EXCELLENCE

CIRCLE NO. 41

55A-186067

NEWS BREAKS

EDITED BY SUSAN ROSE

PROGRAMMABLE IC TESTER IS EASY TO USE AND AFFORDABLE

Maxtec International Corp's $4750 Pro-Line PL-5010 stand-alone IC tester is easy to program and does not require previous testing experience. The μP-based unit contains a resident device library that encompasses tests for more than 90% of all existing 14- to 28-pin ICs. The software can automatically identify a device under test (DUT) by comparing its parameters with stored library responses. An optional program also lets you test custom or nonstandard chips. The tester can perform a loop test that continues to test the device until a failure occurs. For in-circuit testing, a learning function stores the test responses from a board that you know functions properly so that you can use the correct responses to test other boards. The tester displays its results and pin-specific diagnostics on a 2-line, 20-character vacuum-fluorescent display. Front panel LEDs indicate the operation mode and the type of DUT. You can also interface the tester to a PC via an RS-232C port. Maxtec International Corp, Chicago, IL, (312) 889-1448.—JD Mosley

LOW-POWER, 1.8-IN. HARD-DISK DRIVE HOLDS 21.4M BYTES

The 1.8-in. Model 1820 hard-disk drive from Intégral Peripherals takes rotating memory into unexplored territory. Designed to be run from batteries, the 21.4M-byte drive features a 15-mW sleep mode, and can wake up in 1.5 sec. A head-loading ramp keeps the read/write heads off of the storage medium when the drive is turned off or asleep. This feature boosts the number of start/stop cycles that the drive can endure to 1,000,000. When it's not asleep, the drive has an average seek time of 20 msec and a track-to-track seek time of 8 msec. The drive's head-disk assembly and controller card are separate so that you can fit the device into tight spots. The two components measure $0.394 \times 2.01 \times 2.76$ in. and $0.276 \times 2.01 \times 3.03$ in., respectively. You can piggyback the controller onto the head-disk assembly to create a 1-piece unit. Engineering samples of the drive cost $485. Intégral Peripherals, Boulder, CO, (303) 449-8009, FAX (303) 449-8089.—Steven H Leibson

THERMAL IMAGER PROVIDES MCM THERMAL PROFILES

The enhanced version of Compix Inc's 6000 thermal-imaging system lets you get high-resolution pictures of the temperature at every point in operating hybrid circuits and multichip modules (MCMs). The enhancement is a fixed-focus lens that increases the imager's resolution by reducing its field of view to 0.4×0.5 in. You can operate the imager with or without the lens. The basic system, which costs $18,500, has variable focus and a minimum field of $3\frac{1}{2} \times 5$ in. So configured, it is suited to profiling pc-board temperatures. The system is $28,500 with the lens; the company is offering upgrades. Compix Inc, Tigard, OR, (800) 926-6749, (503) 639-8496.—Dan Strassberg

DIGITAL DELAY GENERATOR FOR VXIBUS

The 9001 digital delay generator from Cal-AV Labs lets you generate delays from 0 to 99 nsec with 1-nsec resolution and <50-psec jitter. The board supports trigger rates up to 15 MHz. Output pulsewidth follows input for pulse-train delays. The delay generator has four channels in a C-size module for $2700. A 6-channel version (9002) is also available in a D-size module for $3900. Cal-AV Labs, Campbell, CA, (408) 371-0666, FAX (408) 371-0672, contact Ken Hirschberg.—Doug Conner

NEWS BREAKS

Z8-BASED MICROCONTROLLER INCLUDES ON-CHIP DSP

The Z86C94 microcontroller from Zilog combines a 16-bit DSP with a 24-MHz, 8-bit Z8 µP. The DSP section operates as a slave processor, executing code from on-chip RAM and handling functions such as a 16×16-bit multiply-and-accumulate in a single clock cycle. The chip also includes 8-bit A/D and D/A converters, three counter/timers, 16 I/O lines, a UART, and a 40-kHz pulse-width modulator.

The chip offers a flexible interface between the CPU and outside memory. You can wire the chip to operate with either multiplexed or demultiplexed address and data lines, addressing as much as 64k bytes of external memory. If you choose multiplexed operation, you free up eight signal lines that are usable as additional I/O pins.

The company has a real-time emulator, a software assembler, and evaluation boards to help you develop applications for the device. In addition, it supplies core software for servo applications, the inspiration for the part. The $15 (1000) chip comes in 84-pin plastic leaded chip carriers or 80-pin plastic quad flat packs. Zilog Inc, Campbell, CA, (408) 370-8000, FAX (408)370-8056.—Richard A Quinnell

AWARD HONORS EXCELLENCE IN ELECTRONICS PACKAGING

Electronic Packaging and Production Magazine (EP&P) and NEPCON (National Electronic Packaging Conference) are cosponsoring the first annual Milton S Kiver Excellence In Electronics Packaging And Production Award in February, 1992. The award honors significant achievement in developing equipment and materials to advance state-of-the-art electronics-packaging design and production. The seven categories to receive awards are computer-aided-technology packaging hardware, interconnection, and components; electromechanical devices; printed-circuit chemicals and materials; pc-board assembly equipment and accessories; production test and inspection; hybrid materials; and fabrication equipment. The award will be presented at NEPCON West, February 25 to 27 at the Anaheim Convention Center, Anaheim, CA.

All entries for the awards will be screened by the editorial staff of EP&P and the NEPCON advisory board in September. A panel of electronics-industry experts will do the final judging. All entry forms must be submitted by September 16, 1991. EP&P, 1350 E Touhy Ave, Des Plaines, IL 60018, (708) 635-8800.—Susan Rose

SERIAL BUS LINKS I/O ACCESSORIES ON THE DESKTOP

Digital Equipment Corp and Signetics' Access serial bus links as many as 14 I/O accessories through a single interface to a desktop computer or workstation. The bus lets you connect keyboards, mice, trackballs, handheld scanners, and other accessories in a daisy-chain along a 4-wire cable as long as 26 feet. You can unplug and plug-in accessories along the chain without rebooting your system. You can also add compatible accessories to your system without loading additional device drivers. The bus allows the host computer to read configuration data from the accessory so that it can customize the drivers already installed.

The two companies defined the bus as an open specification, letting both computer and accessory vendors easily adopt it. The specification includes software protocols for various accessory types, generic device drivers, and electrical standards. The protocols work in conjunction with the Phillips I^2C bus. Both companies are offering development kits containing bus specifications and a tutorial. In addition, DEC is incorporating the bus in its next-generation X-terminals. Signetics, Sunnyvale, CA, (408) 991-3505, contact Shlomo Waser. Digital Equipment Corp, Littleton, MA, (800) 678-6736.—Richard A Quinnell

DIGITAL VIDEO ENCODER HANDLES MULTIPLE STANDARDS

The SAA7199 digital video encoder from Signetics accepts digitized video or graphics data and generates analog signals in NTSC or PAL standard video formats. Incoming signals may be digitized NTSC, PAL, or SECAM video; 24-bit red-green-blue graphics; VGA graphics; or one of four other video formats. The IC can accept timing signals from the graphics system supplying data, provide timing signals to the graphics system, or derive its timing by locking onto an incoming video signal. The video-lock capability lets you superimpose graphics data onto any video source. The parts cost $47 (100). Signetics, Sunnyvale, CA, (408) 991-2000.—Richard A Quinnell

CMOS FLASH ADCs CUT BANDWIDTH VS POWER COMPROMISES

Micro Networks' MN5906 6-bit and MN5902 8-bit flash ADCs provide input bandwidths and sampling rates that rival those of power-hungry ECL converters. The MN5906 features no-missing-codes sampling rates of 40 to 50 MHz, depending on the grade. Running at these sampling rates, this converter dissipates just 200 mW from one 5V supply. The large-signal input bandwidth of the MN5906 is 100 MHz—four times the Nyquist rate—and is an important factor in undersampling applications such as synchronous demodulation and digital radio. The 8-bit ADC consumes 400 mW max from a 5V supply, and guarantees no-missing-codes performance at a 20-MHs sampling rate. This ADC's large-signal input bandwidth is 50 MHz, or five times Nyquist.

One important aspect of these converters' high bandwidths is that they produce no sparkle (spurious) codes at these fast-slewing frequencies, even in the presence of over-range analog inputs. Sparkle codes arising from fast-slewing or over-driven inputs have traditionally been a shortcoming of flash ADCs. You can stack the two converters to obtain an extra bit of resolution, and both are available in pipeline or transparent timing modes. The devices are sampling now; volume production will begin in the fourth quarter of 1991. Prices for samples of the 6- and 8-bit devices are $25 and $42, respectively. Micro Networks, Worcester, MA, (508) 852-5400, FAX (508) 853-8296.—Anne Watson Swager

MONOLITHIC 5-TAP DELAY LINE HAS PROGRAMMABLE RANGE

Brooktree Corp's Bt630 5-tap delay-line IC features a 50-MHz bandwidth and a variable delay range that you can set from 25 to 400 nsec. The IC typically dissipates 50 mW of power, a substantial advantage compared with the 300-mW power dissipation typical of hybrid circuits. You can use the delay-line IC in applications that require input pulse widths as narrow as 15 nsec. The IC offers an output-delay accuracy spec of the greater of ±5% of delay setting or ±2 nsec. The accuracy spec applies to both the leading and trailing edge of a signal pulse. You can buy samples of the $11.10 (100) IC now. Brooktree Corp, San Diego, CA, (800) 452-7580, (619) 843-3642, FAX (619) 452-1249.—Maury Wright

ANALOG-DESIGN COURSE EASES FRUSTRATION

The 3-day, $995 Structured Analog Design course, sponsored by Ardem Associates, helps you learn how to let algebra work for, instead of against, you. The course will teach you how to use the formal methods you already know with much less work. The course will especially help you get maximum benefits from CAD programs. Dr R D Middlebrook of the California Institute of Technology teaches the course, which is offered both publicly and in-house. Upcoming dates are September 16 to 18 in Boston, MA and November 20 to 22 in Los Angeles, CA. Ardem Associates, (714) 592-0317, FAX (714) 592-0698.—Susan Rose

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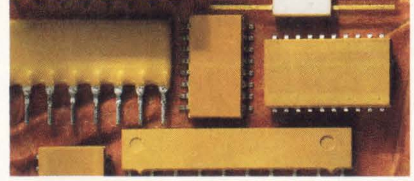

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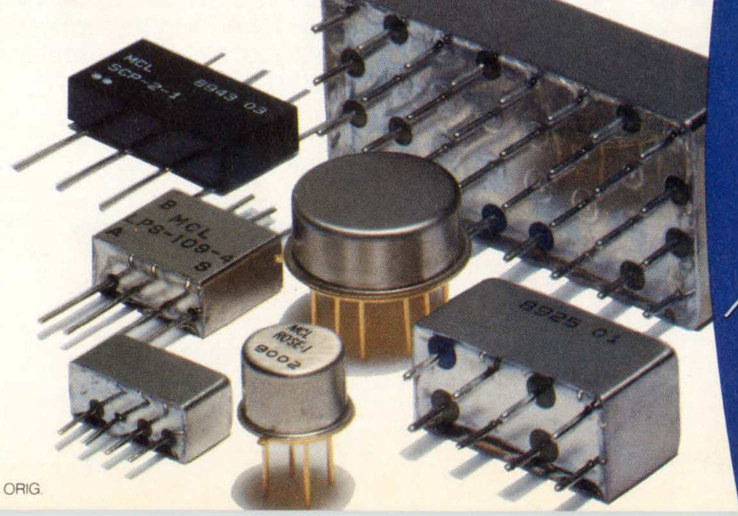
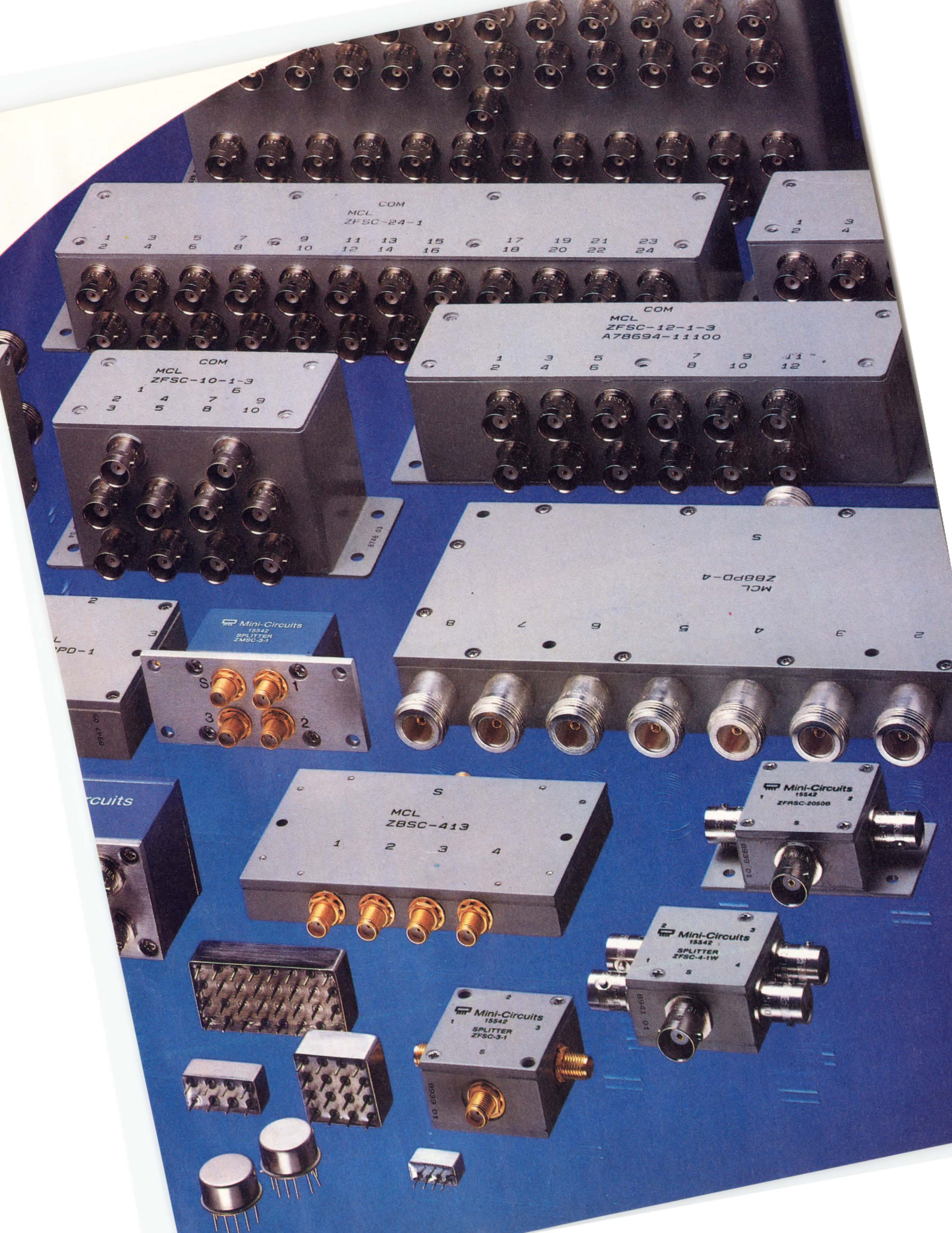


F134-1 REV. ORIG.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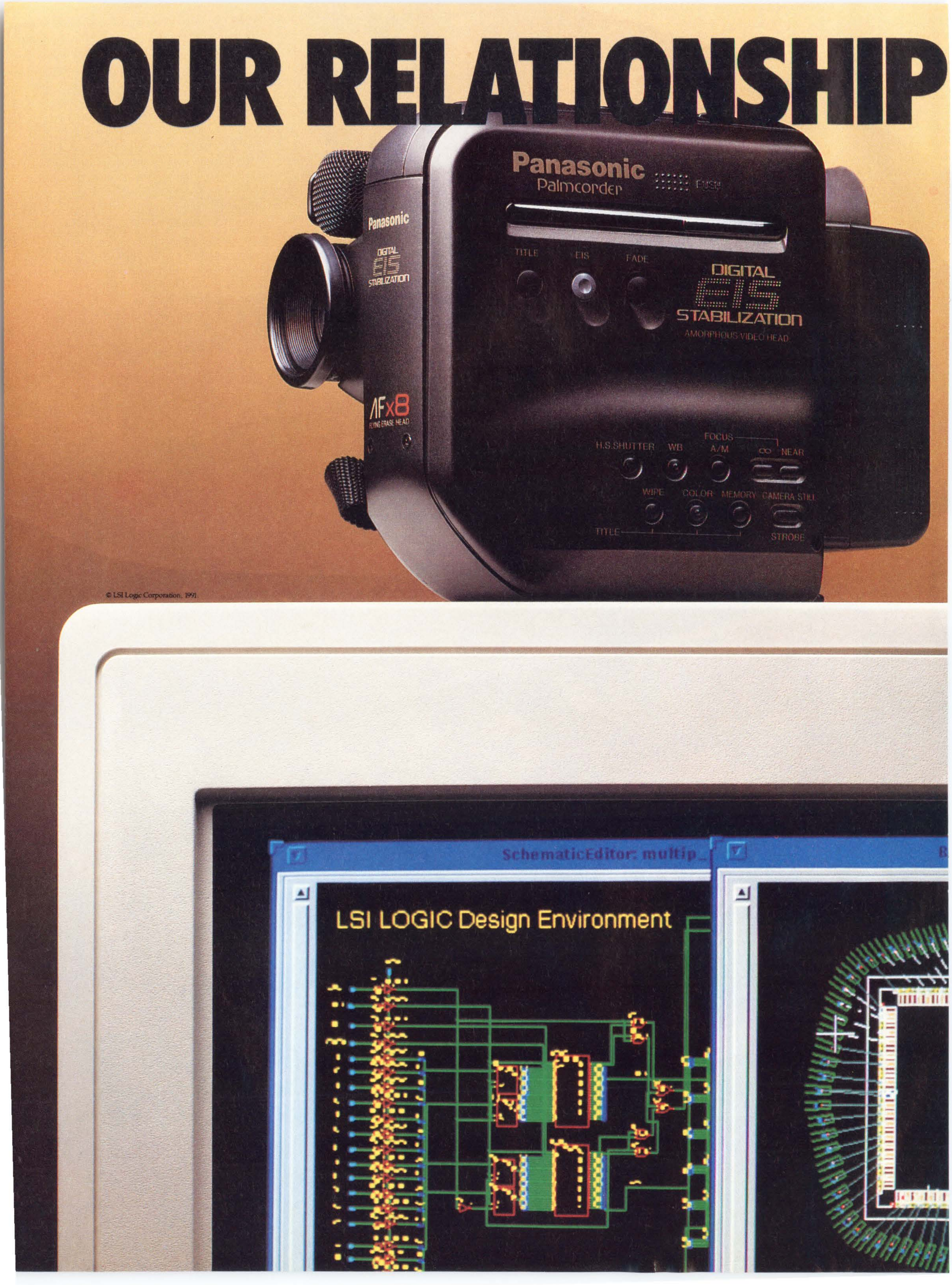
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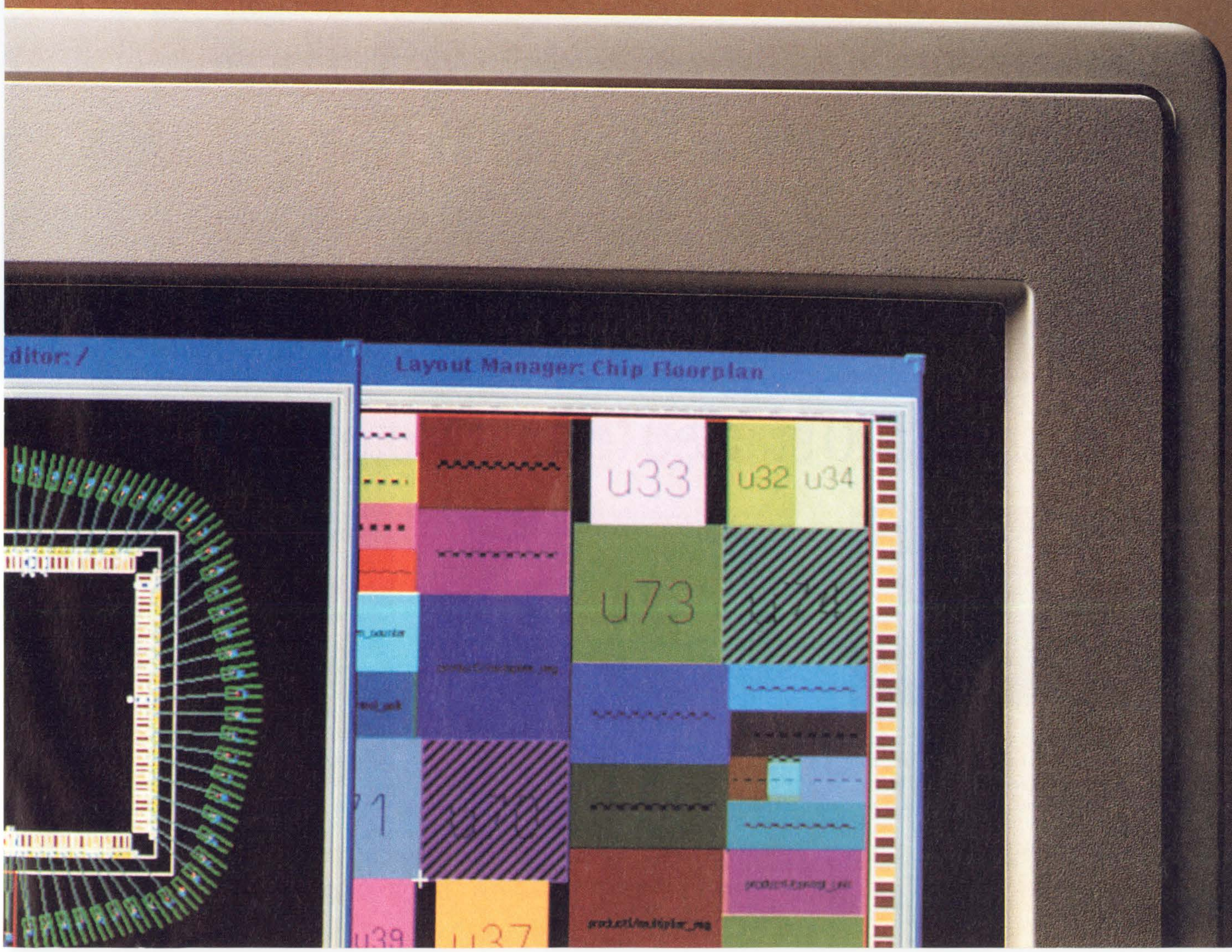

Layout Manager: Chip Floorplan
u33
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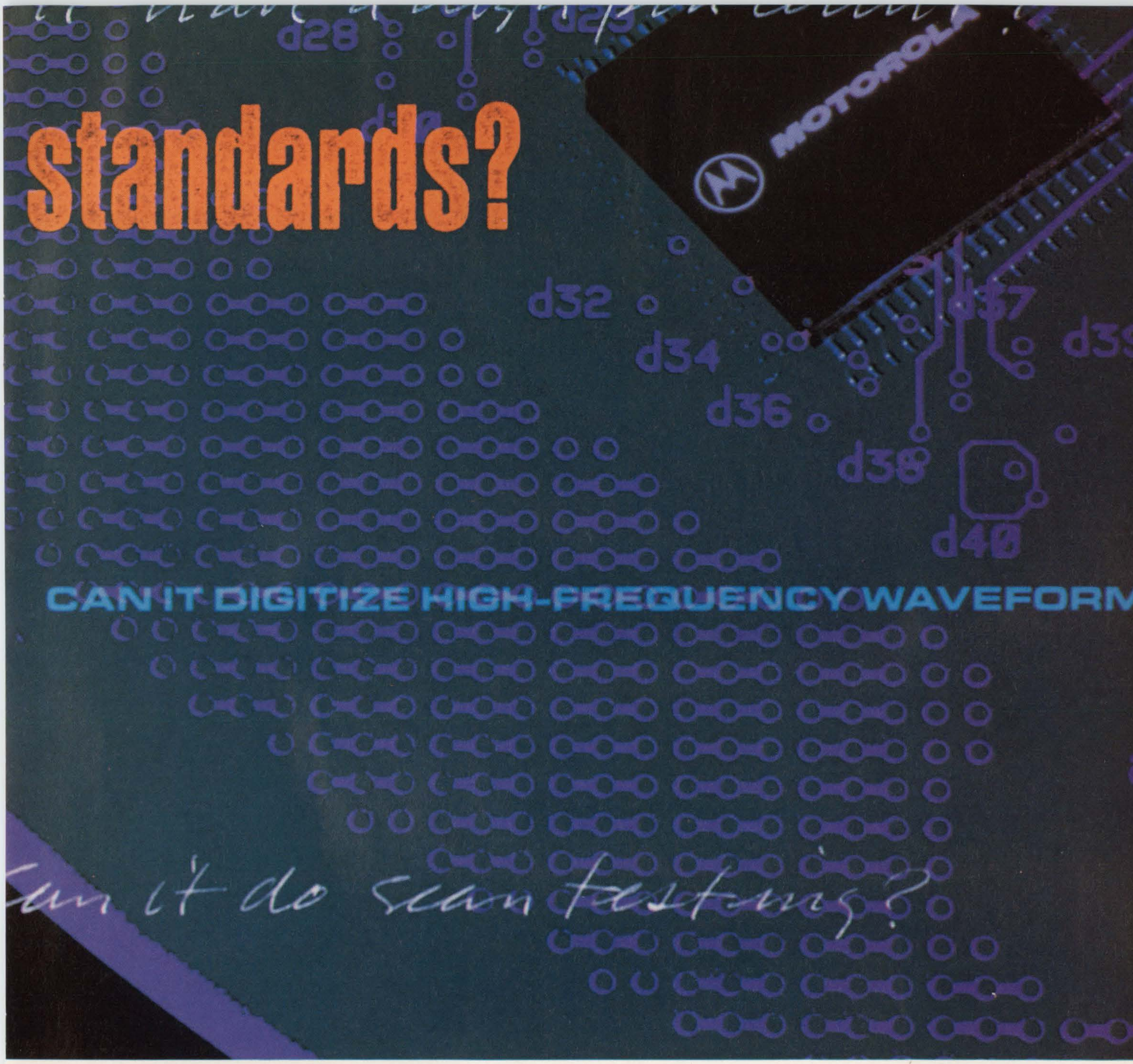

signal technology, Teradyne had to pass a few tests.

With the A500, Motorola had the ability to digitize waveforms at 20 MHz, plus the high pin count necessary to guarantee that their ISDN U-Interface worked the way it was supposed to.

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Operations Manager

To Motorola, delivering Six Sigma quality is not just a promise. It's a way of doing business. And it's a test that must be passed by suppliers as well.

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CIRCLE NO. 47

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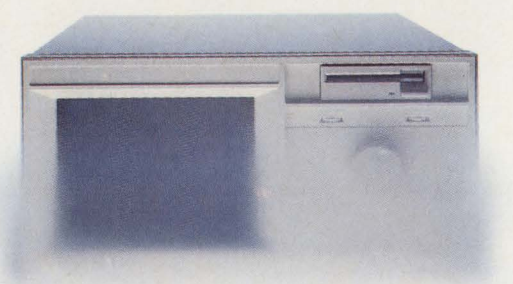

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SIGNALS & NOISE

Views on salespeople and engineers

As an engineer with professional experience in sales, I read with dismay the anonymous letter, "Engineers' salaries should be 'professional,' " (EDN, March 14, 1991, pg 26). It is pointless and inaccurate to describe salespeople (not, please, sales*men*) as people who "goofed off through college years (and landed *his* job because of *his* personality)." The stereotypical loud salesperson wearing a cheap suit is only as accurate as the stereotypical nerdy engineer wearing a pocket protector; both are demeaning generalizations born of bigotry and ignorance.

Over the last 20 years, the engineering community has changed the way the world lives. Engineers have created power over life (been to a hospital recently?) and death (witness the technical destruction wrought in Kuwait and Iraq). Yet engineers have few heroes outside their own narrow circle, and collectively we go largely unrecognized. Perhaps, in part, this is because we refuse to tout our brilliant success in the former case and own up to our deep responsibilities in the latter. Perhaps we aren't treated professionally because we do not act professionally—slandering the trade of others is hardly a professional way to act.

Ian Bruce
Analog Devices
Norwood, MA

More on experimentation for budding scientists et al

Your editorial "Where are the experimenters" (EDN, February 4, 1991, pg 29) prompts me to sit down and write in support of your position on the importance of youthful experimentation for budding scientists and engineers. Although I lived in the Midwest as a youth (St Louis, to be exact) and did not have a "Canal Street," (that place sounds like Heaven to me!), I do know how important Radio Shack, Allied Radio, and Olive Electronics were in helping me to develop an interest in, and understanding of, the principles behind what I practice today. You very eloquently and succinctly put across a very important point.

You could go a little further and ask another very important question. "Where are the 90s' versions of such books as *The Boys First (Second, Third) Book(s) of Radio & Electronics?*" In reading those books I got my first push to go out and buy the parts and kits that got my blood boiling to know and do more. Those books can still be found in libraries, but they have to compete with other recreation media that are a lot more attractive. Maybe the engineering profession could work on packaging fundamental engineering information in some equally attractive format.

Michael Cerulo,
BSEE, MSEE, PE
Staff Engineer
General Electric Co
Cincinnati, OH

Of engineers, actors, unions, and royalties

An anonymous writer in Signals & Noise (EDN, March 14, 1991, pg 26) asks, "Actors and singers get royalties from their work for years after—why shouldn't engineers?"

It shouldn't be imagined that performing artists receive royalties because their employers are kindly, warm-hearted, benevolent corporations. It likely has more to do with the fact that they have strong unions that have historically been willing and able to endure long and rather nasty strikes. Despite this, there are a number of cases of well-known performers who were cheated out of their royalties, or at least had to go through lengthy legal battles to obtain them.

On the other hand, engineers earn an average salary 15 to 20 times that of the average performing artist.

SIGNALS & NOISE

Also, if we pay royalties to engineers, should we also pay royalties to civil engineers when we drive on a bridge, to architects when we live in a house, to chemists when we use synthetics, or to chefs when we use a recipe? Something makes me suspect that in a system like this, it would be the lawyers who would end up with most of the royalties.

The main argument against royalties for engineers, however, is that as the writer states, it would "attract good engineers by rewarding them." Although this is true, it is irrelevant unless there is a scarcity of engineers. The writer's idea of "rewarding with a generous salary" people who work hard obtaining an education is not suited to the free labor market, where incomes depend only on supply and demand. (It could be implemented under a Communist system, though.) When there is an oversupply of engineers, good ones can be attracted by a simple salary.

Michael Robinson
San Jose, CA

Engineers' salaries in a different class

In response to Jon Titus's editorial, "Smart weapons, smart lessons" (EDN, March 14, 1991, pg 35), salaries of professionals such as doctors, lawyers, or sales people are one thing, and those of engineers are an entirely different thing. It all boils down to supply and demand. The problem is, too much of anything is likely to be "cheap."

Unless admissions to engineering colleges are controlled, and severely restricted or limited, as is the case with medicine, we are going to continue to sing the same song over and over again. Our services are readily available. This is a fact of life; we take it or leave it.

B P Shah, PE
Professor of Engineering
University of the District of Columbia
Washington, DC

Reader objects to automatic phone answering

In response to "Automated phone systems are here to stay" (EDN, March 28, 1991, pg 29), Sanford Morganstein obviously wants to promote automated telephone answering. However, I agree with Jon Titus in his editorial, "That's not my job" (EDN, Jan 3, 1991, pg 35).

Our "old-fashioned" system (according to Sanford Morganstein) does have Rohm's Phonemail, and it's surprising the number of hangups we get when someone gets the computer voice rather than a human voice. Competition being what it is today, can we afford to offend those parochial callers who want to speak with thinking listeners?

Personally, I'm offended when I get entangled with these automated answering systems as I'm spending my money on long distance. Why should I waste my money running through a complicated series of button pushing to leave a message?

Ed Oxner
Staff Engineer
Siliconix Inc
Santa Clara, CA

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps (or less) modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200/2400, 8,N,1 in shorthand.

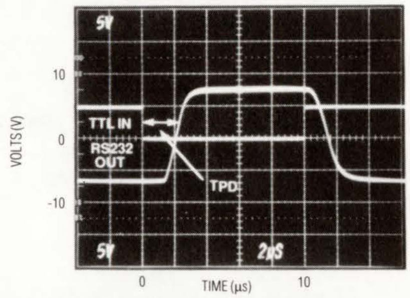
EDN

MAXIM
DESIGN NEWS
Analog Design Insights from Maxim Integrated Products No. 22

Analog Solutions For Tough Design Problems

New +5V RS-232 Transceiver Doubles Speed of Existing +5V RS-232 Devices!

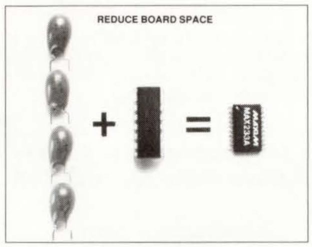
MAX232A PROPAGATION DELAY



The **MAX232A** +5V dual RS-232 transceiver is guaranteed to operate at data rates up to 116kb/s, while driving real loads – 2500pF and 3kΩ. And, the MAX232A uses space-saving 0.1µF caps.

(CIRCLE 1)

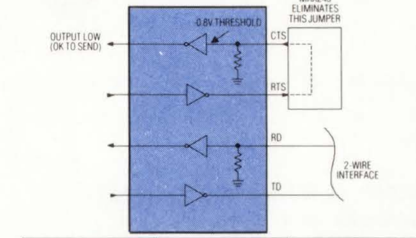
+5V-Powered, Dual RS-232 Transceiver Needs No External Components



The **MAX233A** dual RS-232 transceiver saves board space by integrating all charge-pump capacitors needed for +5V operation within a 20-pin DIP or SO package. Guaranteed data rates up to 116kb/s.

(CIRCLE 2)

RS-232 Transceiver Simplifies Cabling



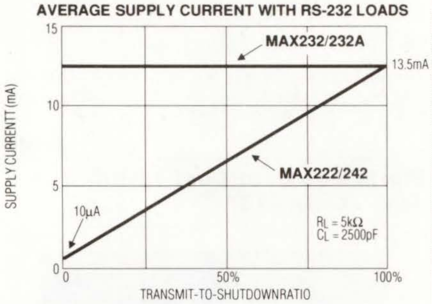
RECEIVER INPUT	R1 OUTPUT	R2 OUTPUT
≤ -3V	HIGH	HIGH
OPEN	HIGH	LOW
≥ +3V	LOW	LOW

The **MAX243** switches between 2-wire and 4-wire interfaces without interrupting communications, and requires no cable change or extra jumpers. This device operates with 0.1µF capacitors, and is guaranteed for data rates up to 116kb/s.

(CIRCLE 3)

RS-232 Dual Transceiver Saves 67mW of Power in Shutdown Mode

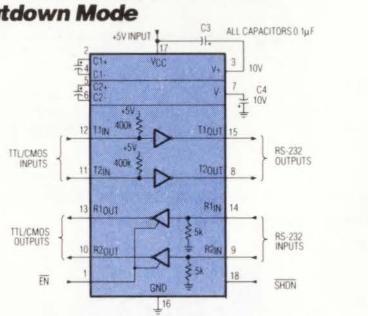
AVERAGE SUPPLY CURRENT WITH RS-232 LOADS



The **MAX222** dual transceiver is guaranteed for data rates up to 116kb/s and operates with space-saving 0.1µF capacitors. It saves up to 67mW of power by reducing supply current from 13.5mA during normal operation to only 10µA in shutdown mode.

(CIRCLE 4)

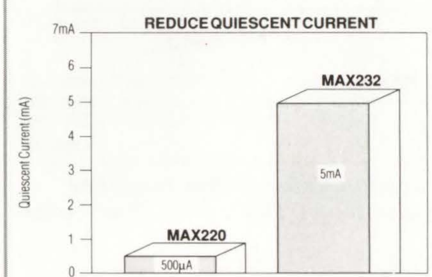
Power-Saving RS-232 Dual Transceiver Stays Active in Shutdown Mode



The **MAX242** dual transceiver is guaranteed for data rates up to 116kb/s and saves space with 0.1µF external capacitors. It features a shutdown mode that saves up to 67mW of power. And, the MAX242 receivers remain active in the shutdown mode. Separate three-state output controls allow bused configurations.

(CIRCLE 5)

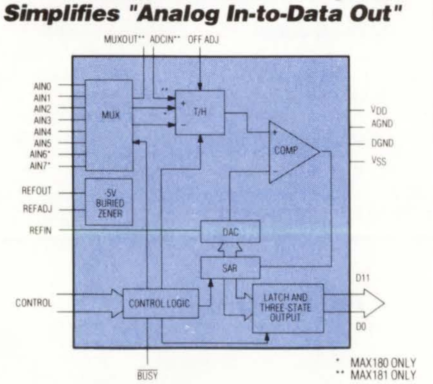
RS-232 Transceivers at 1/10th the Power!



The **MAX220** dual +5V transceiver is designed specifically for low-power operation. Quiescent operating supply current is a mere 500µA unloaded. And, the MAX220 is guaranteed to operate at data rates up to 20kb/s.

(CIRCLE 6)

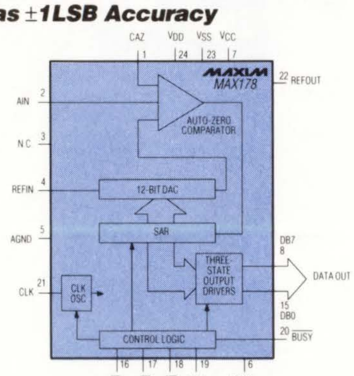
Self-Contained 8-Ch 12-Bit System Simplifies "Analog In-to-Data Out"



The **MAX180/181** have a progammable mux 7.5µs conversion times, 6MHz full-power bandwidth track/holds, and a 25ppm/°C low voltage reference.

(CIRCLE 7)

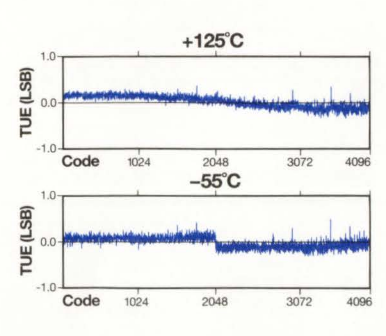
Calibrated 12-Bit ADC with T/H Has ±1LSB Accuracy



The **MAX178** 60µs ADC is calibrated for ±1LSB total unadjusted error, providing true 12-bit performance over the full military temperature range.

(CIRCLE 8)

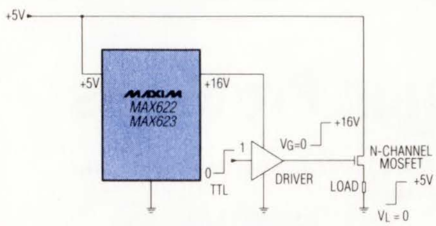
4-Channel ADC with T/H Maintains ±1LSB Accuracy



With no gain, offset, or linearity adjustments, the total error for a **MAX182** stays below ±1LSB from -55°C to +125°C for all codes. Pin-compatible upgrade for AD7582.

(CIRCLE 9)

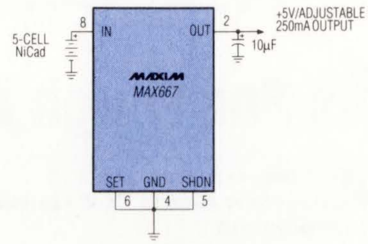
Regulated Charge Pumps Generate High-Side Voltages and Eliminate Expensive FETs



The **MAX622/623** high-side, charge-pump converters provide the supply voltage required to drive low-cost, N-Channel MOSFET switches in high-current applications.

(CIRCLE 10)

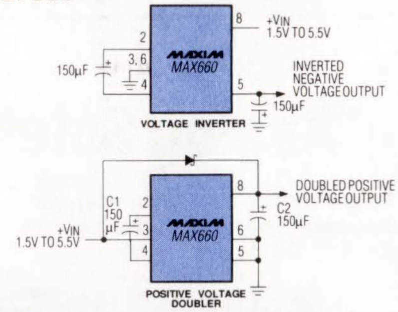
5V Linear Voltage Regulator Has 150mV Dropout at 200mA



The **MAX667** is the only CMOS linear voltage regulator that has both low dropout and ultra-low, 20µA, no-load quiescent current. Ideal for battery-powered applications.

(CIRCLE 11)

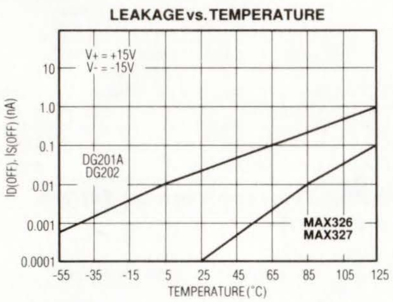
100mA-Output, Monolithic Voltage Converter Upgrades ICL7660



The **MAX660** charge-pump voltage inverter converts a +1.5V to +5.5V input to a -1.5V to -5.5V output. It is a pin-compatible, high-current ICL7660 upgrade. 100mA is supplied with only a 0.65V voltage drop. Efficiency exceeds 90% for most applications.

(CIRCLE 12)

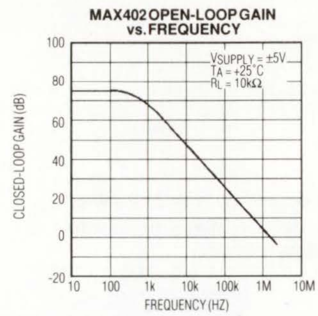
Switches Reduce Leakage Currents to 10pA max



The **MAX326/327** quad, SPST, CMOS analog switches have low 10pA max leakage and operate from single or dual supplies. Upgrade to DG201A/202 and DG211/212.

(CIRCLE 13)

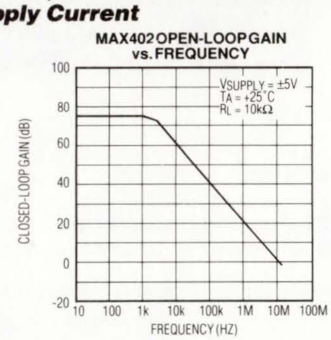
2MHz Micropower Op Amp — 7V/µs Slew Rate from <75µA



No other op amp matches the new **MAX402**'s combination of high speed and micropower operation. It has a 2MHz unity-gain bandwidth and draws only 75µA max supply current.

(CIRCLE 14)

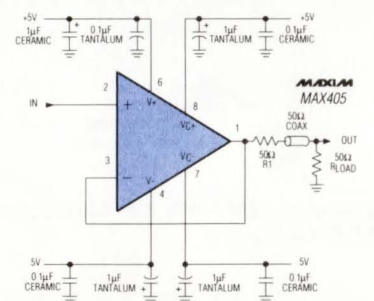
10MHz Micropower Op Amp Slews at 40V/µs – From Less Than 375µA Supply Current



The **MAX403** is unity gain stable and uses 1/10th the supply current of an OP37. Ideal for low-power signal processing and remote sensors.

(CIRCLE 15)

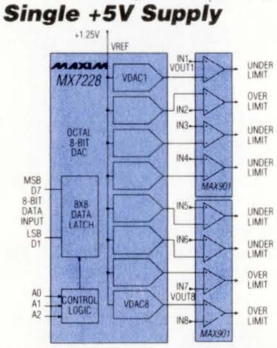
Precision Video Buffer Amplifier Guarantees 0.99V/V Gain Over Temp



The **MAX405** combines 180MHz bandwidth, 650V/µs slew rate, and 0.01° diff phase and 0.03% diff gain from ±5V supplies. Available in small 8-pin DIP or SO packages.

(CIRCLE 16)

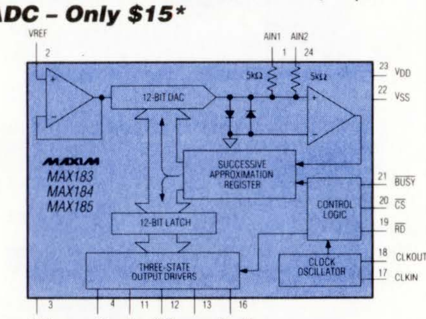
8ns, 18mW Comparators Operate from Single +5V Supply



The **MAX900** series of single/dual/quad comparators offer 8ns response time and draw only 3.6mA per comparator from a +5V supply. Unlike other high-speed comparators, the common mode voltage range extends below ground for single +5V applications.

(CIRCLE 17)

World's Lowest Cost 12-Bit, 3µs ADC – Only $15*



The **MAX183/184/185** BiCMOS, high-speed, 12-bit ADCs have low code-edge noise and low 90mW power consumption. These devices, with wide input range (+15V, +10V or ±5V) and versatile power-supply operation (+5V and -12V to -15V), are ideal for PC data-acquisition cards.

*FOB USA 1000pc.

(CIRCLE 18)

★ DATA SHEETS ★

MAX232A	(Circle 1)	MAX178	(Circle 8)	MAX403	(Circle 15)
MAX233A	(Circle 2)	MAX182	(Circle 9)	MAX405	(Circle 16)
MAX243	(Circle 3)	MAX622/623	(Circle 10)	MAX900/1/2/3	(Circle 17)
MAX222	(Circle 4)	MAX667	(Circle 11)	MAX183/	(Circle 18)
MAX242	(Circle 5)	MAX660	(Circle 12)	MAX184/185	
MAX220	(Circle 6)	MAX326/327	(Circle 13)		
MAX180/181	(Circle 7)	MAX402	(Circle14)		

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PACIFIC MICROELECTRONICS, PTY. LTD., (Rep., Australia): Ph: 61-2-481-0065 Fax: 61-2-484-4460.
FUJITSU MIKROELEKTRONIK GmbH (Dreieich-Buchschlag, Germany): Ph: 06103-6900 Fax: 06103-690122.

CIRCLE NO. 52

News Flash

SPORTS	SCIENCE AND TECHNOLOGY
The 90 Nanosecond Workout An Exhaustive Look At High Tech Training Equipment PAGE 2B	Virtual Reality Close But No Cigar PAGE 8

Silicon Valley C

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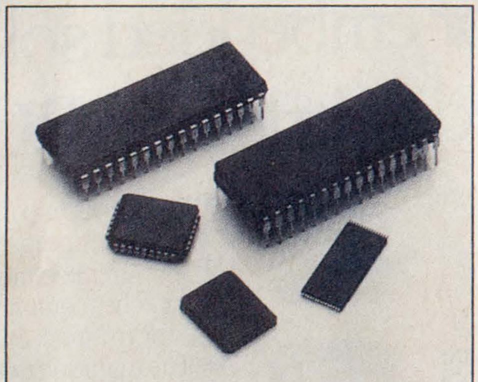

How Fast Is A Flash?
A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

AMD Ships 2 PLCC Flash

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash — hence the name.

Standard, But With A Little More Flash

AMD's Flash memory famil effectively etches in silicon the de-fact standard for this burgeoning technolog that is compatible with Intel's initia Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Meeting

Vice Pr At L

From AMD.

FOOD

Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants

PAGE 7F

zette

MORNING EDITION

ASHES!

Megabit, 90ns,

Memories

The AMD Flash family offers designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1 Mbit and 2 Mbit capacities. TSOP packages will be available in the second half of this year. (LCC not currently available in 2 Mbit.)

AMD's 2 Mbit Flash memories come complete with embedded program and erase algorithms on board. These automatic algorithms speed up the design process and considerably shorten time to market. Previously, engineers were required to develop tedious and time-consuming algorithms to implement in-system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other tasks while these operations are in progress. AMD plans to include embedded algorithms in a future release of its 1 Mbit part.

The Ultra-Violet Blues

Flash technology is particularly suited to applications requiring reprogramming in place, because these devices can be reprogrammed in seconds, and within the system.

To update the code on a UV EPROM, the part must first be removed from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components, costly service calls, and headaches.

Flash memories, on the other hand, can be bulk erased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, over phone lines, or even ISDN

(continued)

ident To Speak

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the *de facto* industry standard.

Our standards, however, are a bit higher. And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323.** And start making some headlines of your own.

Advanced Micro Devices

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CIRCLE NO. 53

Oki's Advanced ASIC Tools Reduce Your Risk.

As an ASIC designer for high-performance systems, you know the sinking feeling of working for weeks on a high-density design—only to have it crash. You know the risks involved in designing with tools that offer no assurances—Will path delays meet spec? Will routed signals violate timing? Will power problems cause unexpected voltage drops?

Oki's advanced tools provide the lift you need to dive comfortably into the highest levels of ASIC design:

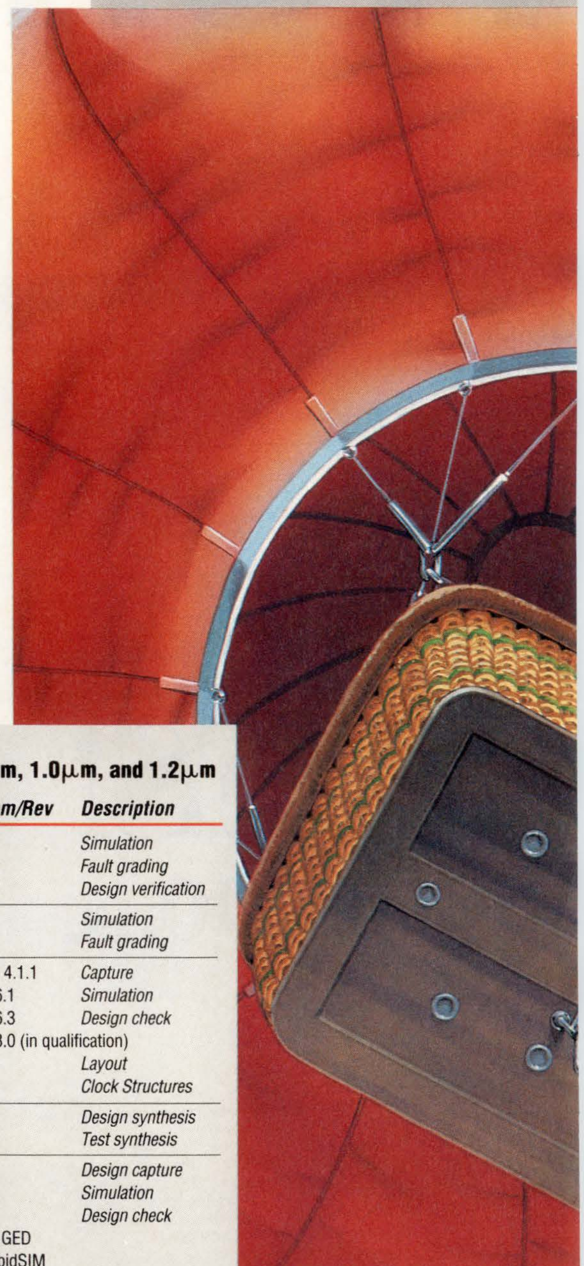
Timing-driven layout - enables control of critical net and path delays, better ensuring a design-to-silicon match.

Clock tree structures - automatically route logic signals where you want them and when you want them, optimizing clock distribution.

Power calculator - locates and corrects power distribution and dissipation problems, increasing overall system reliability.

Coupled with our 0.8μm leading-edge sea-of-gate technology and our high-level support—such as Verilog, Synopsys, and IKOS—these Oki software tools not only optimize ASIC performance but also optimize design time.

So go ahead and take the plunge. Call 1-800-OKI-6388, Dept. 050, for Oki's ASIC capabilities brochure. See how risk-free ASIC design can be.



Oki ASIC Design Tool Support for 0.8μm, 1.0μm, and 1.2μm

Vendor	*Platform*	*Operating System/Rev*	*Description*
Cadence	Sun/SPARC Solbourne	Sun OS 4.1.1 Verilog 1.5C	*Simulation* *Fault grading* *Design verification*
IKOS		4.0 up	*Simulation* *Fault grading*
Mentor Graphics	HP/Apollo DNx Series	DNIX 5.03, Sun OS 4.1.1 Digital application 6.1 Digital application 6.3	*Capture* *Simulation* *Design check*
	HP9000	Digital application 8.0 (in qualification)	
	Sun/SPARC Solbourne	Parade	*Layout* *Clock Structures*
Synopsys	Sun/SPARC Interface to Mentor, Valid, Viewlogic	Sun OS 4.1.1	*Design synthesis* *Test synthesis*
Valid	Sun/SPARC Sun-3	Sun OS 4.1.1 GED, ValidSIM, RapidSIM	*Design capture* *Simulation* *Design check*
	DECstation 3100 IBM RS6000	ULTRIX, ValidSIM, GED GED, ValidSIM, RapidSIM	
Viewlogic	Sun/SPARC	Sun OS 4.1.1 Workview 4.0	*Design capture* *Simulation*
	PC386	DOS 3.3, Workview 4.0	

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WHEN YOU PLUNGE INTO ASIC DESIGN, YOU WANT SUPPORT TOOLS THAT WORK.

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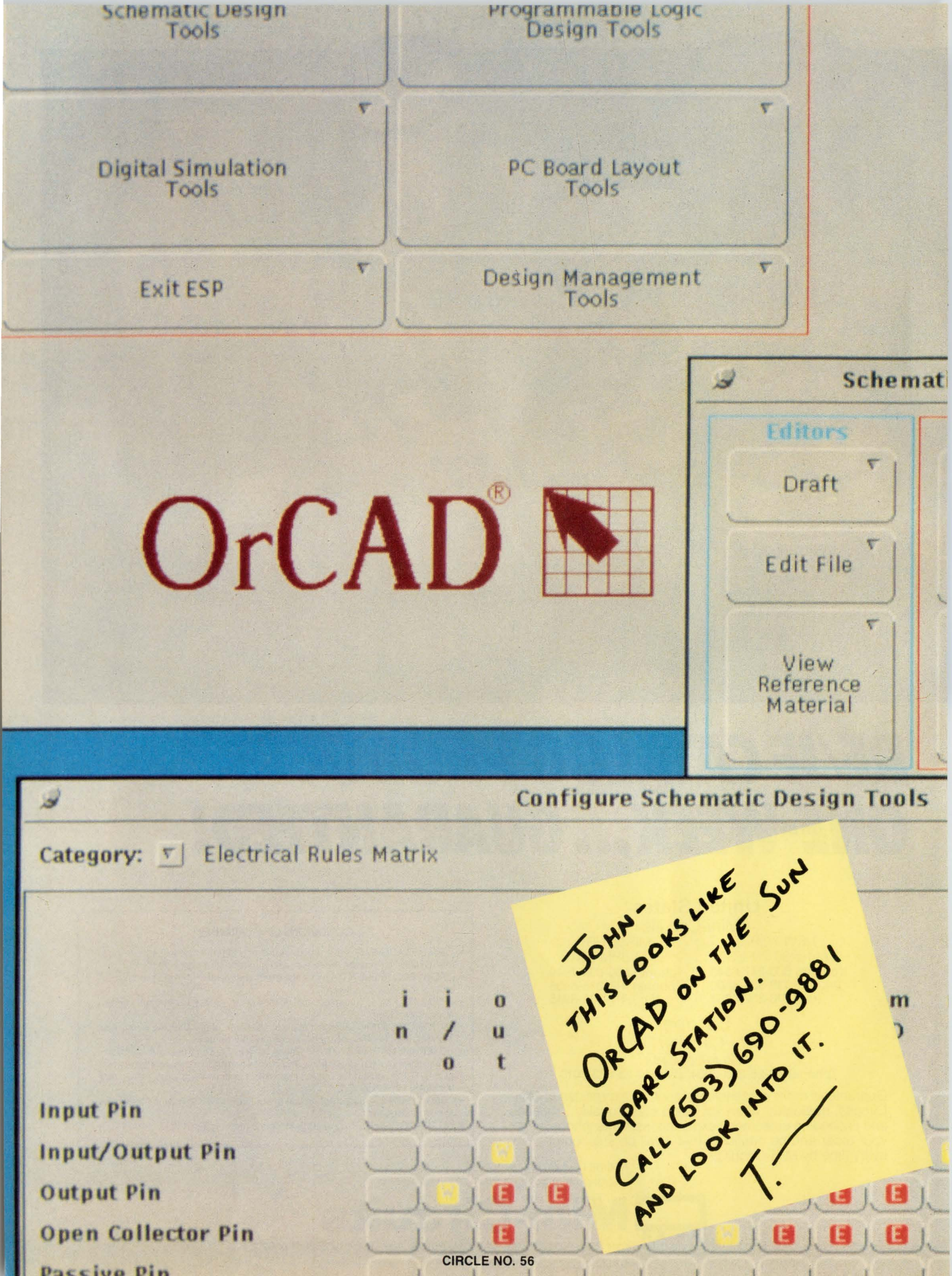
CIRCLE NO. 54


Schematic Design Tools
Programmable Logic Design Tools
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Edit File
View Reference Material
Configure Schematic Design Tools
Category: Electrical Rules Matrix
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Input/Output Pin
Output Pin
Open Collector Pin
Passive Pin
JOHN-
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ORCAD ON THE SUN
SPARC STATION.
CALL (503) 690-9881
AND LOOK INTO IT.
T.

CIRCLE NO. 56

ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Are LEDs going out of style?

I have been searching for a replacement for an LED that was discontinued by Fujitsu. It is the model FED073K1WA. The 10-mW device has a 730-nm peak wavelength, a 10° half angle, and a spectral half width of 25 nm.
Alex H Clark
Leeds & Northrup
North Wales, PA

We called Fujitsu (Santa Clara, CA), and the company has indeed discontinued this LED. Phone calls also revealed that Rohm (Irvine, CA), Philips Components (Riviera Beach, FL), and Harris Semiconductor (Melbourne, FL) not only do not make such a part but also are phasing out their LED product lines.

Siemens (Cupertino, CA) still manufacturers LEDs but does not offer the part you describe, which the company characterized as "oddball." If any readers know of a source of these LEDs, please contact Ask EDN.

Need more information about power pulser

We are developing an inexpensive medical ultrasound instrument and need a power pulser. The output of the pulser should be a 1- to 2-μsec square wave. The pulse-repetition frequency should be between 3600 and 7200 pulses/sec. The output of the pulser should be variable between 60 and 400V. Can you help us?
Jonathan Keroes, MD
President
Cardioscope
San Francisco, CA

You really haven't given us enough to go on. You haven't said whether you want to buy an instrument-level pulser to use in developing your product or OEM modules—one of which you can put in each unit you ship.

You describe the unit as a power pulser, but you haven't stated the unit's peak output power or the impedance of the load. You say the pulse amplitude is 60 to 400V, but voltage is not power. If you're looking for an OEM device, you need to say how you propose to adjust the output voltage and frequency. Should the unit use externally mounted potentiometers or should it accept binary numbers that represent the pulse amplitude and frequency? In addition, you haven't indicated what kind of power source the unit should use or whether you prefer a pulser that uses an ac or a dc supply.

If you need a pulser that you can supply in quantity as part of a medical instrument, consider hiring a consulting engineer to design one for you. A search through the Electronic Engineers Master Catalog failed to reveal any companies that make modular pulsers for OEM applications.

Additional source of high-temperature components

In reference to your response concerning high-temperature components in the June 20, 1991, issue of Ask EDN, Linear Technology Corp still offers a line of 200°C components. These parts are the LT1001XH precision op amp; LT1007XH low-noise, high-speed precision op amp; LM101AXH uncompensated general-purpose op amp; LM118XH high-slew-rate op amp; LM129XH 6.9V precision voltage reference; LM111XH general-purpose comparator; and LM119XH high-speed dual comparator.

In addition, there are other devices from Linear Technology that have a good history of operation at 200°C (and higher) even though they are not specified at that temperature. Any design engineer seeking more data about 200°C operation of our components should contact the marketing department or their local field-applications engineer.
Alan Rich
Field Applications Engineer
Linear Technology Corp
1630 McCarthy Blvd
Milpitas, CA 95035
(408) 432-1900
FAX (408) 434-0507

One out of two isn't bad

In answer to the second-source problem from Margaret Motamed of Xerox in the June 6, 1991, Ask EDN, the only apparent manufacturer of the 92C32 is indeed Western Digital. Standard Microsystems makes a device with the same basic part number, the COM92C32, but it is not the same part at all. Even the package is different.

However, the NEC μPB9201C floppy-disk interface—seemingly a bipolar part—has a MOS version available from Intel (408) 765-8080, the μPB9201C. At least the pinouts are identical. The Center for Military Replacement Parts is in the business of assisting the military services and their suppliers in finding obsolete and otherwise difficult-to-find components.
Bob McIntyre, Institute for Technology Development
Advanced Microelectronics Div
Center for Military Replacement Parts
1 Research Blvd
Starkville, MS 39759
(601) 325-2240
FAX (601) 325-8144

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241; leave a letter in the ask_edn Special Interest Group.

CALENDAR

Comex '91: Mobile Communications Exhibition & Conference, London, England. Jim Williams, Marketing, Frametrack Ltd, Keswick House, 207 Anerley Rd, London SE20 8ER, UK. (81) 778-3343. FAX (81) 778-8402. September 10 to 12.

Buscon '91 East, Washington, DC. CMC, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500. FAX (203) 857-4075. September 10 to 13.

Government, Industry, and University Neural Network Applications Workshop, Huntsville, AL. US Army Research Office, SLCRO-AO-A, Box 12211, Research Triangle Park, NC 27709. (919) 549-4341. FAX (919) 549-4310. September 11 to 12.

Midcon '91, Rosemont, IL. Midcon/91, 8110 Airport Blvd, Los Angeles, CA 90045. (800) 877-2668; (213) 772-2965. FAX (213) 641-5117. TLX 181350. September 11 to 13.

International Electronics Manufacturing Technology Symposium, San Francisco, CA. Paul Wesling, 12250 Saraglen Dr, Saratoga, CA 95070. (408) 725-6472. September 16 to 18.

High Performance VLSI Packaging Seminar, Atlanta, GA. Pat Fruscello, ICE Corp, 15022 N 75th St, Scottsdale, AZ 85260. (602) 998-9780. FAX (602) 948-1925. September 17.

Transmission and Distribution Conference & Exposition, Dallas, TX. IEEE/PES Registration, 2368 Eastman Ave, Suite 11, Ventura, CA 93003. (805) 654-0171. September 22 to 27.

Electronics Design Show, Birmingham, W Midlands, UK. MGB Exhibitions Ltd, Marlowe House, 109 Station Rd, Sidcup, Kent DA15

7ET, UK. (81) 302-8585. FAX (81) 302-7205. TLX 918389. September 24 to 25.

Electrical Overstress/Electrostatic Discharge Symposium, Las Vegas, NV. EOS/ESD Association, Box 913, Rome, NY 13440. (315) 339-6726. FAX (315) 339-6793. September 24 to 26.

Failure Mode and Effect Analysis (seminar), Boston, MA. Quality Alert Institute, 1475 S Colorado Blvd, Suite 206, Denver, CO 80222. (800) 221-2114; (212) 353-4420. FAX (800) 473-8348. September 27.

Information Security 91, Vienna, Austria. Diebold GesmbH, Graf Starhemberg-Gasse 25, A-1040, Wien (Vienna), Austria. (504) 13000. FAX (504) 1309. September 30 to October 1.

Electronic Imaging East, Boston, MA. Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; (617) 232-3976. FAX (617) 232-0854. September 30 to October 3.

IEEE-Holm Conference on Electrical Contacts, Chicago, IL. IEEE, Holm Conference Registrar, Box 1331, Piscataway, NJ 08855. (201) 562-3863. FAX (201) 562-1571. October 6 to 9.

Telecom '91: World Telecommunications Exhibition, Geneva, Switzerland. International Telecommunication Union, Place des Nations, CH-1211 Genève 20, Switzerland. (22) 730-5236. (22) 733-7256. October 7 to 15.

Symposium on High Density Integration in Communications and Computer Systems, Waltham, MA. Harry Lockwood, GTE Laboratories Inc, 40 Sylvan Rd, Waltham, MA 02254. (617) 466-2786. FAX (617) 890-9320. October 17 to 18.

HOW ENGINEERING SEES OUR NEW 32-BIT INTEGRATED PROCESSOR.

Actually, a bullet doesn't do it justice. But you get the picture. Motorola's new 68330 integrated microprocessor is fast.

And well it should be. After all, it gets its firepower from a 68020-based core processor that's optimized to run on a 16-bit data bus. So you get 32-bit microprocessor performance with the economy of a 16-bit memory system.

68000 MICROPROCESSOR FAMILIES					
68000 CPUs Architectural Integration	000	020	030	040	
68EC000 EMBEDDED Performance/Cost	EC000	EC020	EC030	EC040	
68300 INTEGRATED Functional Integration	302	330	331	332	340

Motorola's 68000 families let you choose the performance and integration that's right for your application.

As the simplest and lowest priced member of the 68300 family, the '330 is an ideal companion to your favorite peripheral circuits. Even if you've already combined them into an ASIC or custom circuit.

What's more, the 68330's Systems Integration Module comes already loaded with system glue logic. Saving you the trouble of designing in functions like clock

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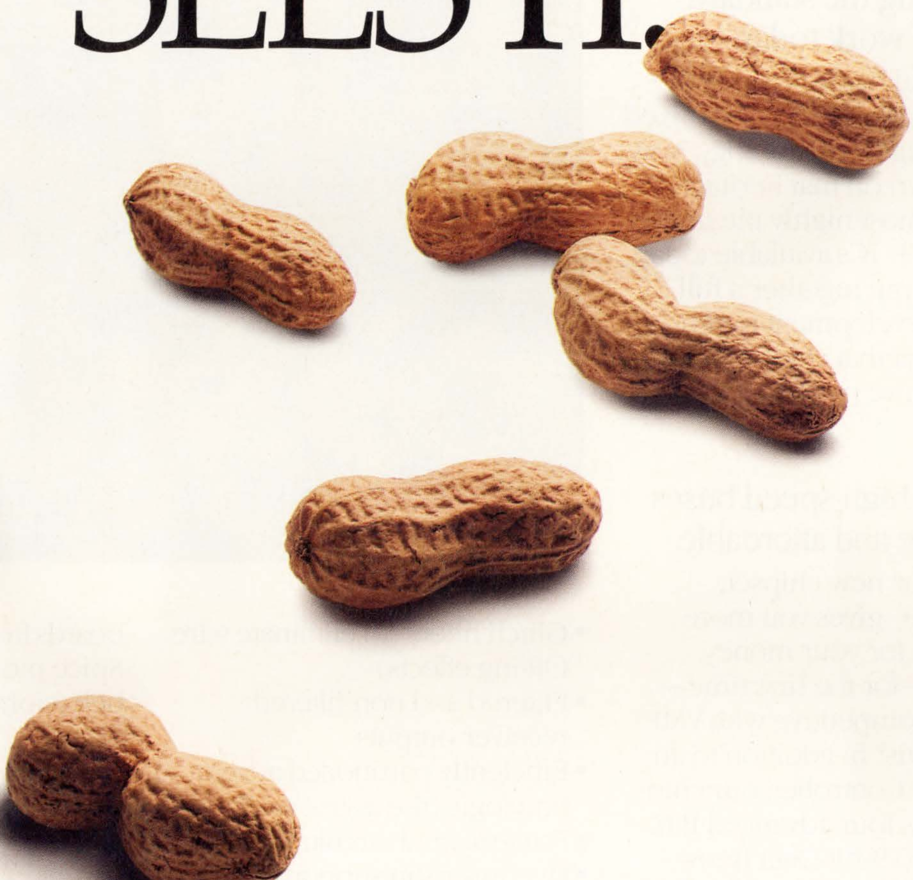
HOW PURCHASING SEES IT.



generation, chip selects and interrupt control.

And, since the '330 is fully binary software compatible with all members of the 68000 and 68300 families, it provides a seamless migration path, reams of reusable code, popular operating systems and familiar development tools.

All of which can save you a lot of trouble, while lowering overall system costs and raising your accountants' morale.

So if you're looking for 32-bit performance at a 16-bit system price, call 1-800-845-MOTO. Ask for a free 68330 product sample,* and discover a high-caliber value.

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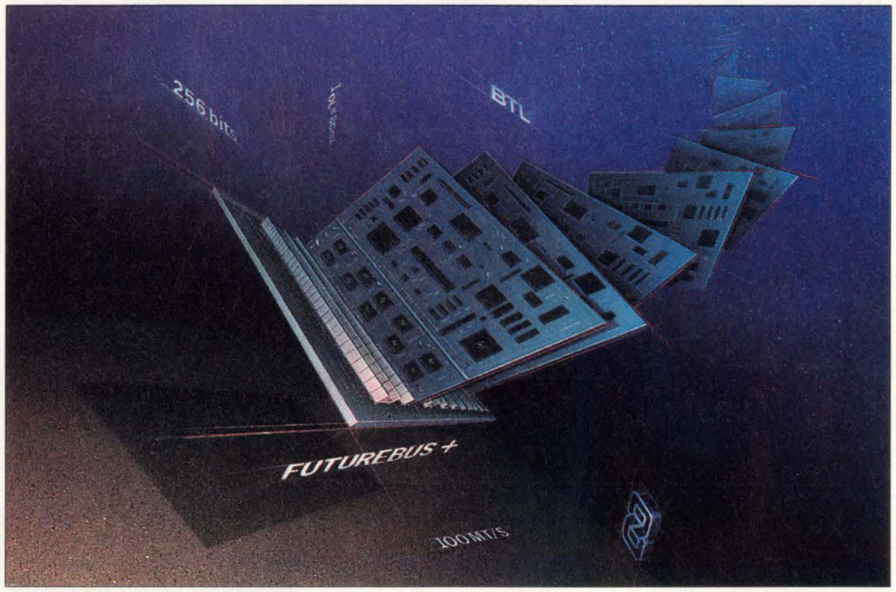
Come see us at BUSCON East BOOTH #404

Futurebus+. Now you can start your design without waiting for the future.



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National has long been the industry leader in BTL and mixed analog + digital technology. Now we've drawn on that heritage to make the most highly integrated Futurebus + ICs available today. We've also put together a full range of development tools to help you put that chipset to work. And the entire package is available now.

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Between them, they offer you a variety of features designed to break the throughput bottleneck in high-performance computer systems:

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- Efficiently partitioned arbitration logic (the fastest available)
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Start with our Designer's Handbook, with a slave-memory-board application note, product data sheets, and application notes on BTL design technology. Other tools include wire-wrap boards from Mupac and Hybricon, Spice models, and Verilog® behavioral models.

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EDITORIAL

It's only software

Not too long ago, we reached an important milestone; the value of software in electronic products outstripped the value of the hardware. Because software is intangible, it's difficult to pin down an exact value for "software content," but software's importance grows daily. Unfortunately, many companies and managers treat software as if it were a poor relation. It becomes easy to say, "It's only a few lines of code. What could go wrong?"

If you need an example of software gone awry, just think back a few months to when several large US telephone networks were badly clogged with phone calls. In some areas, it was impossible to make or receive a call. It turns out that three or four lines of code were changed in a switching system built by DSC Communications (Plano, TX), but the code wasn't thoroughly tested before it was used. As is often the case, minor changes don't always get simulated and tested the way they should. In this case, those untried lines of code disrupted telephone systems in Washington, DC, Los Angeles, and elsewhere.

Many managers don't understand the value of software. After all, you can't touch software, and you can't easily determine its value the way you can the value of integrated circuits, displays, metal cases, and power supplies. Also, managers don't understand what it costs to produce good software. When it comes to a hardware project, engineers need specific tools if they are going to do their jobs. Typical hardware projects require oscilloscopes, computers, simulators, workstations, logic analyzers. But what of software projects; what do they need? Often the managers' answers are, "Buy them a C compiler and a couple of PCs, and let them get to work."

Software projects require more than just a compiler and personal computers (PCs). You have to think of the software part of a project as needing almost the same expenditures as the hardware part. Software engineers need workstations, a network, top-notch operating systems, debugging and testing tools, and computer-aided software engineering (CASE) packages. Yes, they need compilers, too. Throw in program libraries, project-management software, trips to software conferences, and short training courses, and you get an idea of what a software project can cost.

When you start your next product-development plan, be sure to set aside a reasonable budget for software development. Today, reasonable can easily mean half the cost of the project. Just because you can't touch the software and manipulate it the way you can hardware, you must still give software its due. If you neglect software, it has a habit of catching up with you. If you're still a nonbeliever, just ask the people at DSC Communications about the importance of good software.

Jon Titus
Editor

Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

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First, we're delivering 040 VME single board computers today. In quantity. So you can get started while the rest of the world waits for a delivery date from other suppliers.

Second, our new CPU-40 board is setting performance standards nobody else can touch. Like 30,000 dhrystones sustained at 25 MHz.* And DMA transfers at a screaming 50 Mbytes per second sustained (3 microseconds on the VMEbus).

So it might just be the last 040 board you'll ever need.

That's because we've fully optimized the on-board architecture. Thanks to our 281-pin gate array, DMA operations can be handled between on-board RAM, the VMEbus and on-board I/O devices. Or through our FLXi interface to other I/O drivers.

All of which means the CPU is free over 75% of the time to run your application.

Developing new applications is also a snap. Choose from the broadest range of third-party software in the business, including VMEPROM,™ pSOS+,™ VRTX32,™ OS-9,™ VxWorks,™ UNIFLEX,™ MTOS™ and UNIX® 5.4.

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CPU-40 PERFORMANCE CHARACTERISTICS

Data from	CPU	CPU	CPU	CPU	VMEbus	SCSI*	Floppy Disk*	Ethernet*	Shared RAM*	VMEbus*
Transfer to	Shared RAM	EPROM	Serial I/O Timers	SCSI, Ethernet Controller, Floppy Disk	Shared RAM	Shared RAM	Buffer RAM	Dual-port RAM	VMEbus	VMEbus
Transfer Speed	53.7 MB/sec	16 MB/sec	2 MB/sec	2 MB/sec	5 MB/sec	4 MB/sec	500 KBit/sec	10 MBit/sec	15 MB/sec	15 MB/sec
Local 68040 CPU Operation	100%	100%	100%	100%	70%	80%	100%	100%	75%	100%

**DMA x FPS*

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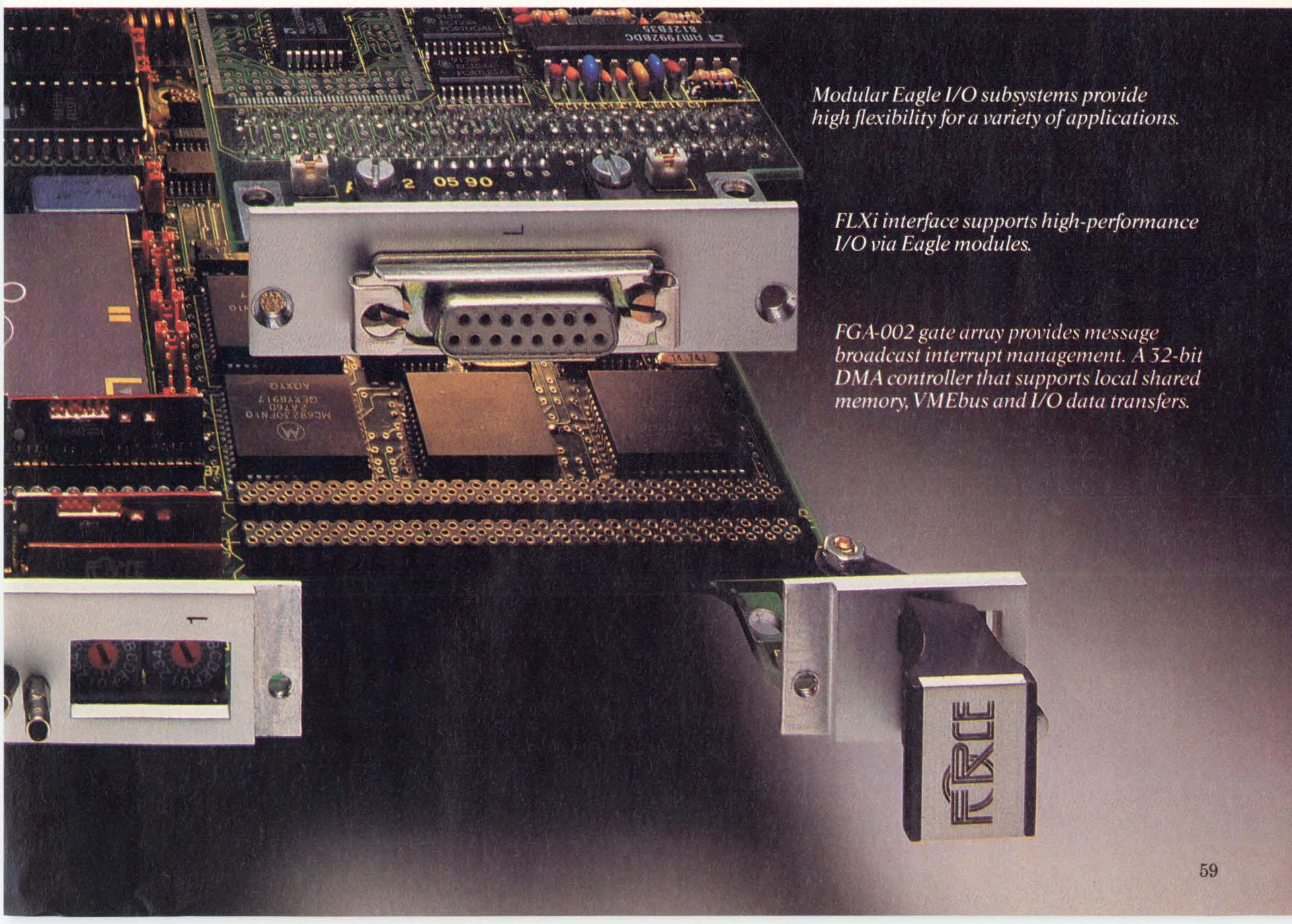
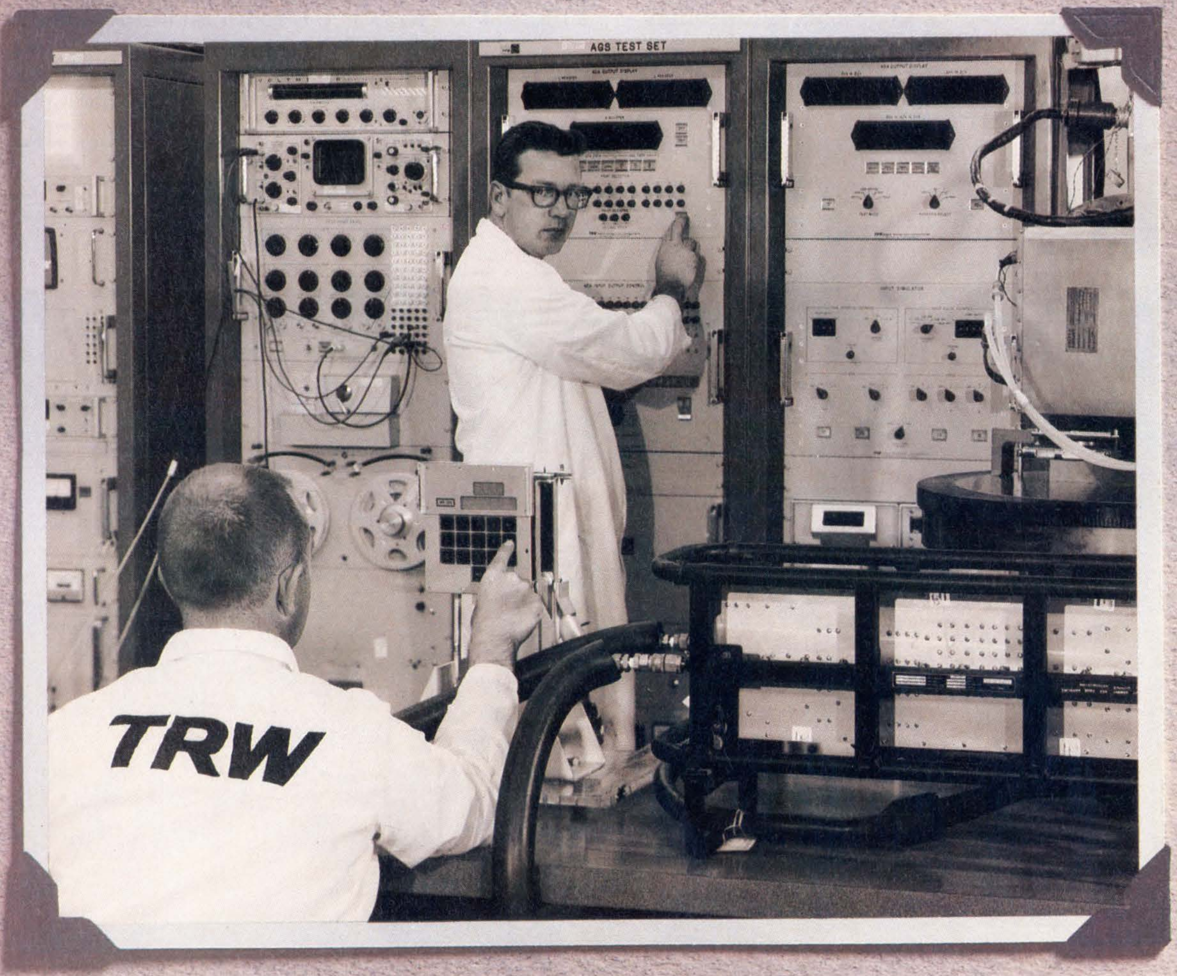
CIRCLE NO. 63



WE DESIGNED THE BEST A/D CONVERTER IN NO TIME AT ALL. BUT THEN, WE HAD A 30-YEAR HEAD START.



8-bit resolution. 40 Msps. Two-step architecture and CMOS technology that reduces power dissipation to less than 180mW.

All with a significant cost advantage. And all from a single +5 Volt power supply.

That is the TMC1175, developed in only months by TRW LSI Products Inc. But then, that's what you can expect from the industry leader in high-performance A/D converters.

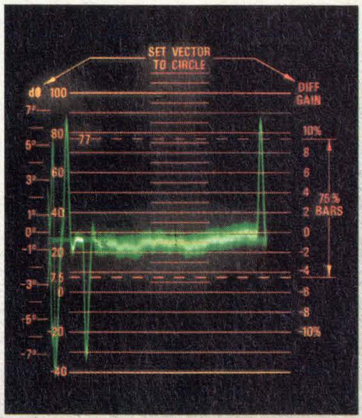
Our years of setting standards have given us the ability to respond quickly to changing needs in the industry, continually improving our line of products in terms of performance and cost. The same dedication to perfection that earned us an Emmy award in 1989 for video technology.

With the TMC1175, video driving amplifiers can be eliminated. The Track-and-Hold circuit is built-in; so is the voltage reference. All digital inputs and three-state outputs are TTL-compatible. And all performance specifications are guaranteed over the -20°C to 75°C temperature range.

All of which makes the TMC1175 excellent for Digital Television designs. Video Digitizing. Image Scanners. Multimedia. And low cost, high speed Data Conversion. It can even be used in PC video board designs.

The TMC1175 is available in 24-pin plastic skinny DIP, 28-lead PLCC and 24-lead plastic SOIC (small outline) suitable for surface mount applications.

And of course, TRW LSI backs you with all the support you need. With field and in-house application engineers. Application notes. And a full line VLSI Data Book.



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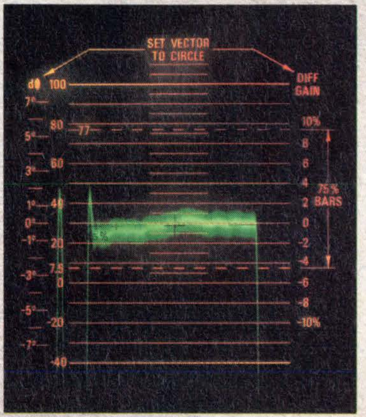

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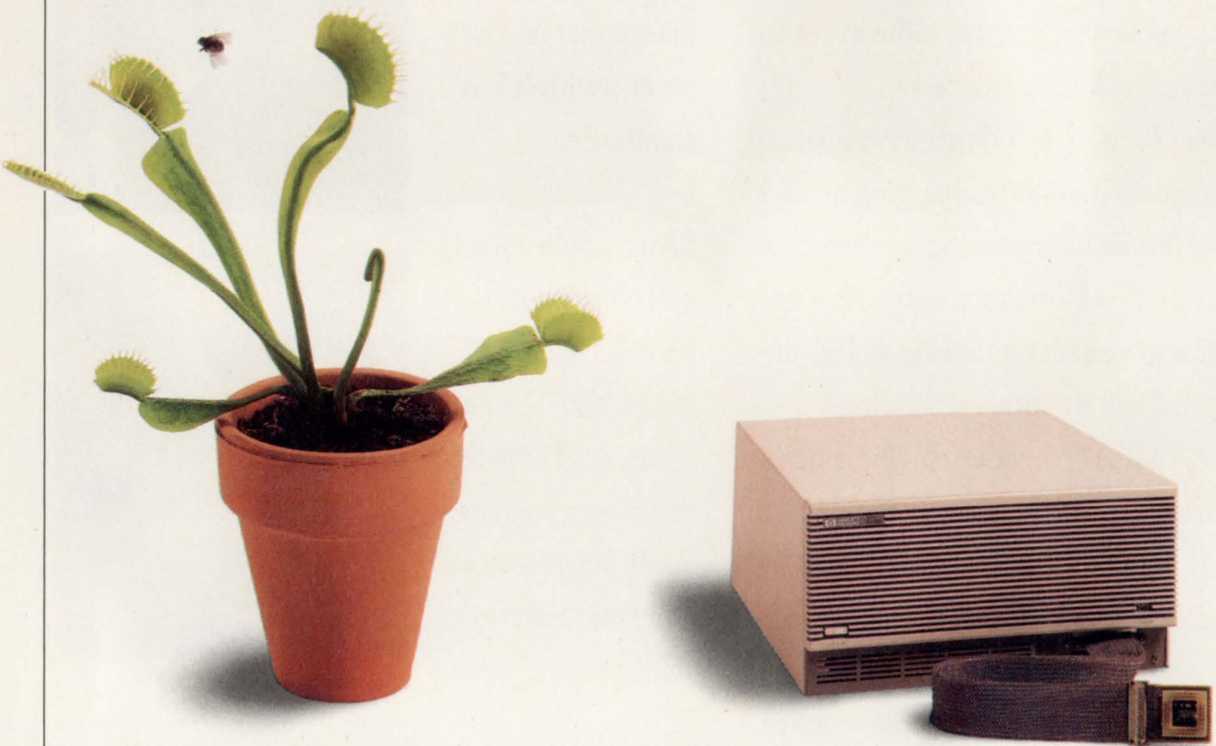

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SPECIALIZED IC PACKAGES

A variety of housings satisfies diverse needs

When you look at IC packages today, you'll notice a number of choices besides the ubiquitous DIP. Three trends are the driving force behind the introduction of these packages—higher pinout requirements, increased packing density, and surface-mount technology.

Tom Ormond, *Senior Editor*

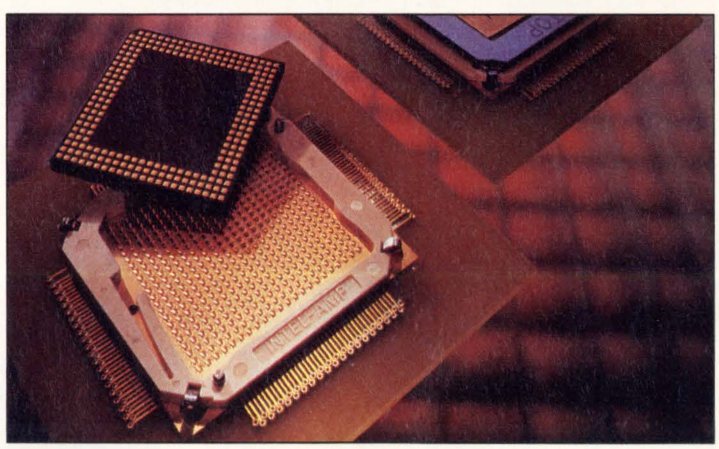
None of today's variety of IC packages can boast of the dominance once enjoyed by the DIP. Rather, these different packages address specific needs in a given area of design. The PGA (pin-grid array) is the package of choice in the through-hole area for high-pin-count ASICs, gate arrays, and μPs. In the surface-mount area, three packages are vying for dominance—the LCCC (leadless ceramic chip carrier), the PLCC (plastic leaded chip carrier), and the PQFP (plastic quad flat pack). During the surface-mount revolution, standard pin pitches for these surface-mount packages moved steadily from 100 to 25 mils.

As viable as today's standard packages are, they don't necessarily satisfy the needs of all applications. For example, package size may be too large for the design in question. These size considerations can involve both package height and mounting area. Then there's the problem of insufficient I/O on standard packages. In some cases, the I/O density may not suffice. There are also noise considerations. Fortunately, some IC vendors offer devices in configurations that can handle very stringent system-design constraints, such as packaging density.

Seeq Technology has introduced a low-profile, 28-pin PGA package, which is designed specifically for avionics and military EEPROM applications ranging in density from 16 to 256k bits. The package design is consistent with other PGAs, and Seeq is submitting the package outline for standardization to JEDEC's publication 95 and future incorporation into DESC specification 38510.

The hermetically sealed, alumina-ceramic PGA has a gold-plated lead finish that complies with MIL-38510. The unit has a solder-sealed gold lid, which is preferred in high-vibration and mechanical-shock environments. The package dimensions are 0.55×0.65 in.—a surface-area requirement that is about 40% of that for an equivalent-pin-count DIP, significantly improving packing densities in memory-intensive applications. When mounted, the package typically stands 0.141 in. above the board, including a clearance standoff of 0.05 in.

Quality Semiconductor has carried the



Featuring a mounted profile of 0.2 in., *the AMPflat socket assembly from AMP accommodates land-grid-array devices with as many as 484 contact positions. The assemblies feature positive contact wipe and are available with either gold or tin-lead-over-nickel plating.*

Specialized IC packages

high packing-density concept even further by shrinking the size and pinout spacing of its small-outline package for fast CMOS TTL (FCT)-compatible logic devices. Designed for 20- and 24-pin surface-mount devices, the quarter-size outline package (QSOP) employs a dense 25-mil pin spacing and a half-width, 150-mil body to increase the board density of FCT logic by 400%, when compared with conventional SOIC packages.

With QSOPs, FCT functions can save 75% more space than traditional SOIC-packaging methods. This space saving makes the device particularly suitable for laptop and notebook computers. Another key advantage for designers is that the QSOP uses shorter package bonding wires. This feature reduces the ground-bounce problems associated with FCT logic devices by 30% over SOICs. In addition, QSOP improves overall board performance by shortening circuit-board traces.

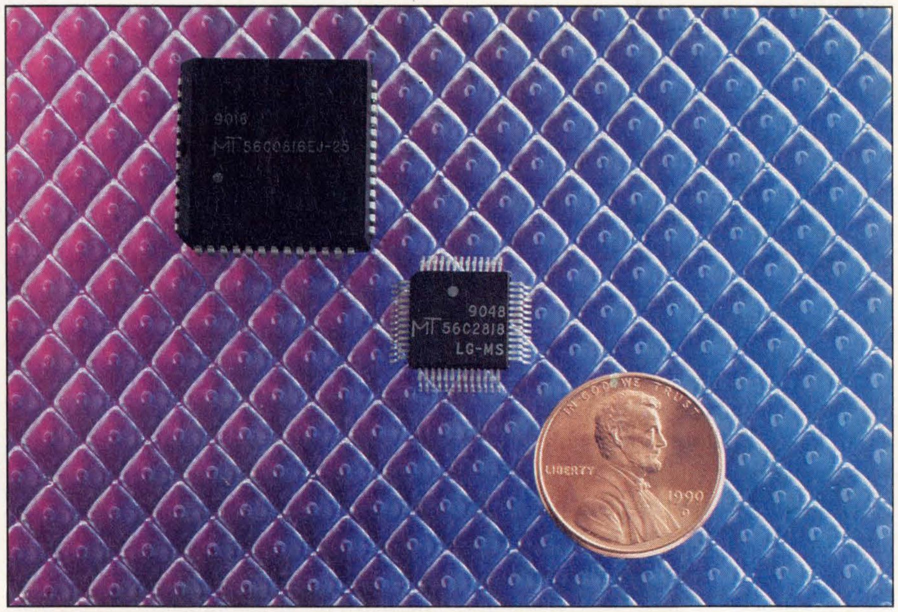
The 25-mil spacing used in the QSOP is an accepted industry standard for high density surface-mount packaging. The package outline dimensions are identical to the industry standard 14-pin SOIC packages. As a result, QSOP requires no new tooling and presents no new assembly and test challenges to system manufacturers.

Talk about I/O density

Packing density and board real estate are not the only system-design constraints; you must also address I/O-density problems. For example, Mitsubishi offers a tape-automated bonding, quad flat pack (TAB QFP) for its 0.8-μm CMOS gate arrays—devices designed for systems running at frequencies ranging to 100 MHz. Alternate packages, such as ceramic pin-grid arrays and PQFPs, use wire-bonding technology. Although these packages can achieve pin counts into the mid-300 range, tape-automated bonding is necessary beyond that pin count.

TAB QFPs have a very fine lead pitch and a small footprint (**Fig 1**). The TAB process bonds a silicon device to prefabricated copper leads on sprocketed plastic that resembles camera film. The tape in a TAB QFP is a roll of polyimide film with holes punched to hold the die. A copper layer is laminated onto the film, then etched and plated to produce the lead frame. Chips prepared specifically for TAB QFPs have bumps on their bond pads. In a step called inner-lead bonding, the leads on the lead frame are attached to the bumps, which are then encapsulated in resin.

The TAB QFP offers an outer lead pitch of 0.25 mm, letting you place 576 pins on a 40 × 40-mm package. The flexibility of the leads lets you mount the package on a pc board with either side of the package facing up. The inner lead pitch (the distance between the leads con-



In a memory application, *pc-board space is often at a premium. Micron Technology's line of cache-data static RAMs come in a 10-mm plastic quad flat pack—a unit that's 30% smaller than a comparable plastic leaded chip carrier.*

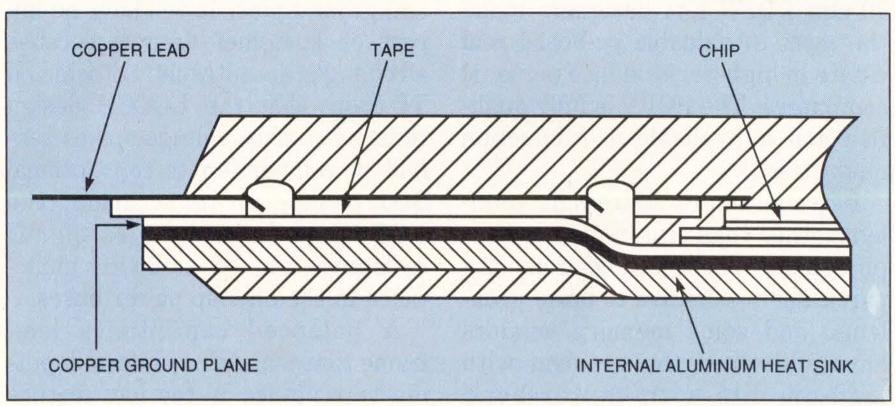


Fig 1—By utilizing an internal heat sink, *the tape-automated-bonding package from Mitsubishi has a standard dissipation rating of 3W. You can increase dissipation to 22W by using an external heat sink and mounting the package upside down on the pc board.*

necting the lead frame to the chip) is less than 90 μm. The thermal coefficients of the die, tape, and molding resin are balanced to minimize mechanical stress on the chip and prevent the package from warping.

The TAB QFP is designed to provide lower thermal resistance than standard plastic packages. The internal aluminum heat sink quickly spreads heat from the die to the periphery of the package. The heat sink is not covered by the plastic used to encapsulate the chip. This lets you mount the package directly to the copper layer on the pc board to dissipate as much as 3W of power. To increase dissipation to 22W, simply mount the package upside down on the board and attach an external aluminum heat sink to the exposed internal heat-sink surface.

***Designed for memory-intensive applications** where real estate needs are a prime concern, Seeq Technology's 280-pin, pin-grid-array package measures 0.55 × 0.65 in.—about 40% of the surface area needs of equivalent-pin-count DIPs.*

How small is small?

Micron Technology now offers its family of cache-data static RAMs (SRAMs) in a 10-mm, 52-pin PQFP. The footprint of the new package is 40% smaller than a 52-pin PLCC—the current industry-standard package for cache data RAMs. In fact, Micron believes that its 10-mm PQFP, which has overall dimensions of 14.3 mm, is the smallest memory package in the industry.

A line of SRAM devices in the 10-mm PQFP lets designers make the most of valuable pc-board real estate in high-performance personal computers. The PQFP is fully qualified and is available in production quantities.

IC vendors are addressing problems other than size in memory applications. These applications are particularly sensitive to noise problems, and some memory vendors have addressed the problem with lead-on-chip-with-center-bond (LOCCB), small-outline J-lead (SOJ) plastic packages.

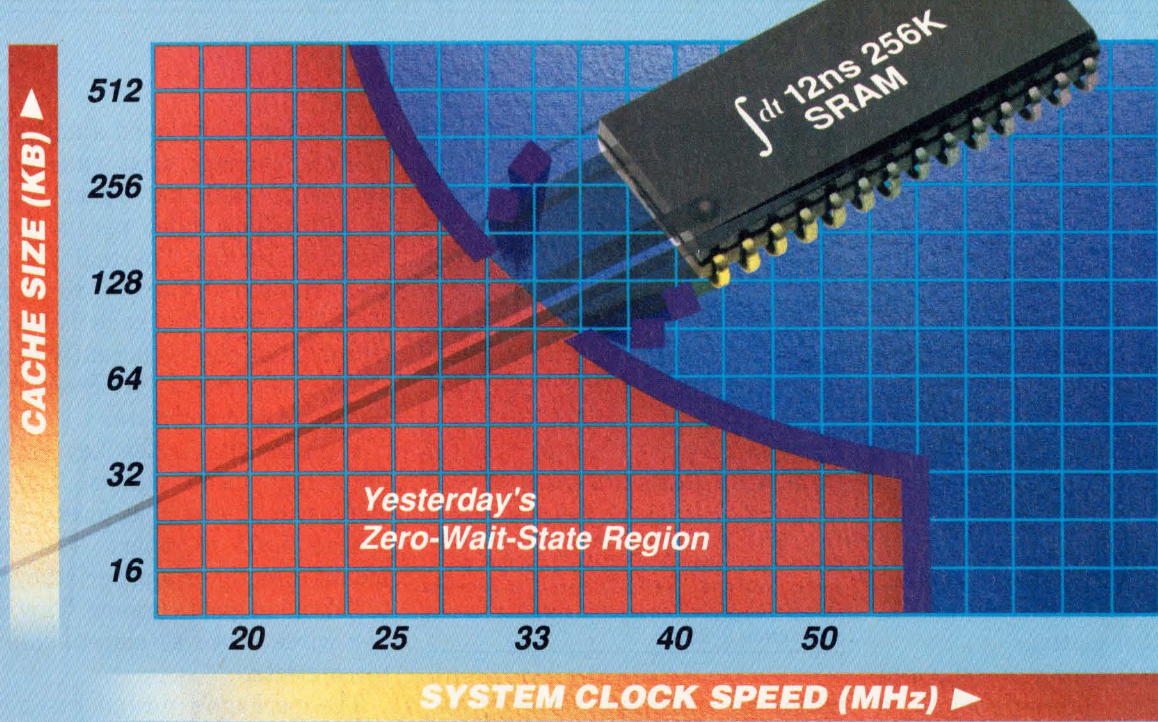
For example, Texas Instruments (TI) and Hitachi Ltd have worked together to develop an LOCCB package for 16M-bit dynamic RAMs (DRAMs). The innovative 24- or 28-pin housing increases the amount of silicon available within a standard package, minimizes on-chip noise, and improves the uniformity of the electrical characteristics of the package leads.

The package will house chips as large as 330 × 660 mils and conforms to JEDEC standards of 400 × 750 mils. The package has dual power and ground pins. It will have no impact on customer designs because all changes are internal. Hitachi and TI claim that the LOCCB design reduces on-chip voltage spikes tenfold in comparison to conventional SOJ packages. In addition, the LOCCB package features 20-mΩ resistance and 10- to 20-nH inductance in the on-chip power buses.

A balanced capacitance lead frame that maintains uniform input-pin capacitance is the key feature of the LOCCB design. All internal leads are equidistant from one another. A passive Y-lead in the middle of the lead frame and on either side minimizes differences in pin-to-pin capacitance. Two metal bus lines, integral to the lead frame structure, run in parallel above the length of the chip. One bus line links the dual ground pins located at the ends of the package, and the other bus line links the corner dual power pins on the other side of the chip. The arrangement thus provides multiple bonds between the bus lines and the circuit. Thanks to the dual pin arrangement, maximum values of voltage drop, resistance, electrical noise, and inductance equal 0.2 V, 10 mΩ, 0.02 V, and 6 nH, respectively. The LOCCB package minimizes the size of on-chip power buses; the package's lead frame routes power above the chip's surface.

Chip designs from both TI and Hitachi have bond pads for contacting the lead frame located in the chip's center, rather than around its periphery. Centering the bond pads reduces thermal and mechanical stress on the chip and voltage drops

Smash the Cache Barrier



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Integrated Device Technology

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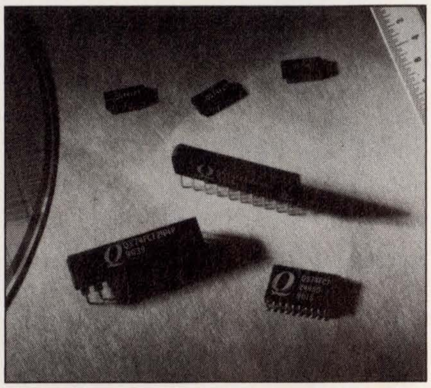
Specialized IC packages

associated with long traces on the chip itself.

The AMPflat land-grid array (LGA) socket assembly from AMP accommodates LGA packages with as many as 484 positions. It is configured on a 0.05-in. centerline grid and offers a mounted profile of 0.2 in. The keystone of the assembly is a contact array that is only 0.009-in. high when fully compressed, features 10-psec max delay, and has a per-contact thermal resistance of 200°C/W. The unit features positive contact wipe, a replaceable contact array, and a choice of gold or tin-lead-over-nickel platings.

The socket assembly is composed of a heat-clamp pressure plate, a chip-carrier nest to hold the LGA, a contact array, and an insulator-spacer. These components are sandwiched between a cover plate and a base plate. The insulator thickness is selected to match the thickness of the pc board for a given assembly. In this manner, the resultant stack thickness of the assembly yields the required normal forces under compression. You can install or remove the clamping top plate using an ordinary screwdriver. Both top and bottom plates are made of stainless steel. The bottom plate insulator is assembled with adhesive on its top and bottom surfaces so that the bottom plate is permanently attached to the pc board after initial installation.



***In addition to reducing ground bounce** by 40%, QSOP packages from Quality Semiconductor increase fast CMOS TTL-logic packaging density by 400%. The package presents no assembly challenges and requires no new production tooling.*

The multichip module seems to be the package of the future. As evidence of the capability achievable with these modules, consider the following development: IBM engineers have developed a multichip-module package that can handle electronic traffic moving at a speed of 280 million miles per hour. An evolution of the Thermal Conduction Module (TCM), invented in 1980, the 5-in.^{2} package holds 121 silicon chips and is currently in production as part of IBM's System/390 Series large computers.

High density is the key to handling high-speed signals. The 121 chips within the new package are spaced 0.375 in. apart. The chips mount directly on a proprietary material called glass ceramic. Tiny copper wires serve as chip-to-chip interconnects.

The package's design resembles a multilayered club sandwich. The chips are bonded directly to a 63-layer slice of glass ceramic. The 0.001-in.-thick copper wires link the chips together. The wiring also threads through two million holes in the ceramic layers. The dense wiring is equivalent to approximately 140 ft of copper wire per in.^{2} of package. The copper interconnects within the new package replace the molybdenum wiring

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used in earlier TCMs, improving electrical conduction. And the glass ceramic that replaces the old alumina-ceramic base in the TCM improves electrical-signal speed.

The IBM engineers had to solve one difficult problem in developing the materials for the package: Because the ceramic must be sintered (or fired) with the copper wires in place, the designers had to develop a ceramic that would harden before copper melts. The new glass-ceramic crystallizes at 1742°F, just 203° below the melting point of copper. The computer-chip package sets a number of performance records.

Because the glass ceramic has a low dielectric constant, signal transmission speed increases by 25% when compared with the older TCM. The chip-packing density also reduces signal travel time. The package conducts heat away from the chips twice as fast as the older package. Finally, the glass ceramic has a thermal coefficient of expansion that perfectly matches that of the silicon chips. As the chips heat and expand during computer operation, the glass ceramic will expand at the same rate, ensuring the integrity of circuit technology used in the package.

A look into the future offers no clear picture of any significant new packaging concepts. There's little doubt, however, that packaging concepts will continue to appear. For the near term, new packages will most likely be finer-pitch variations of today's most popular packages. EDN

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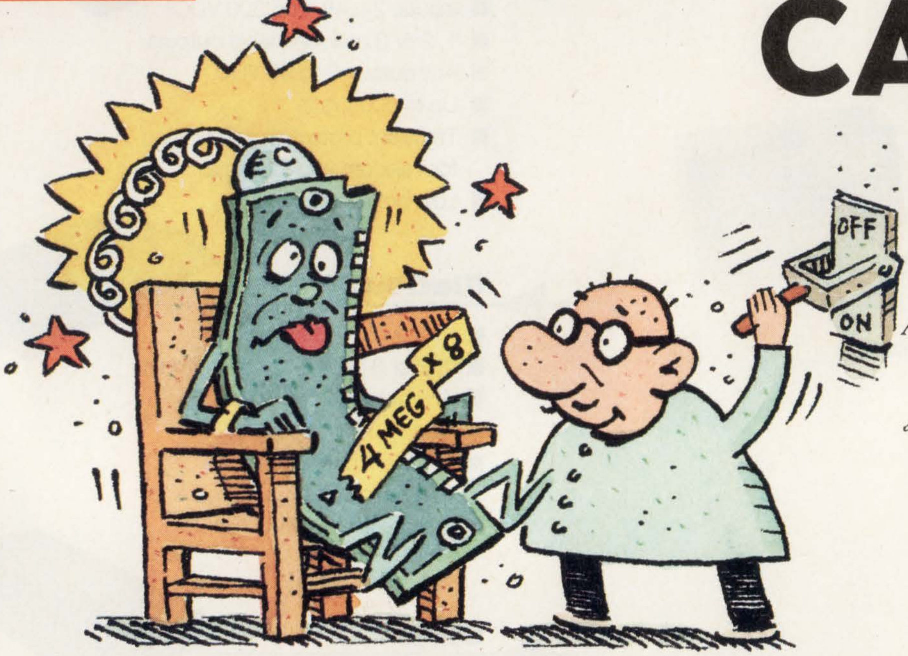

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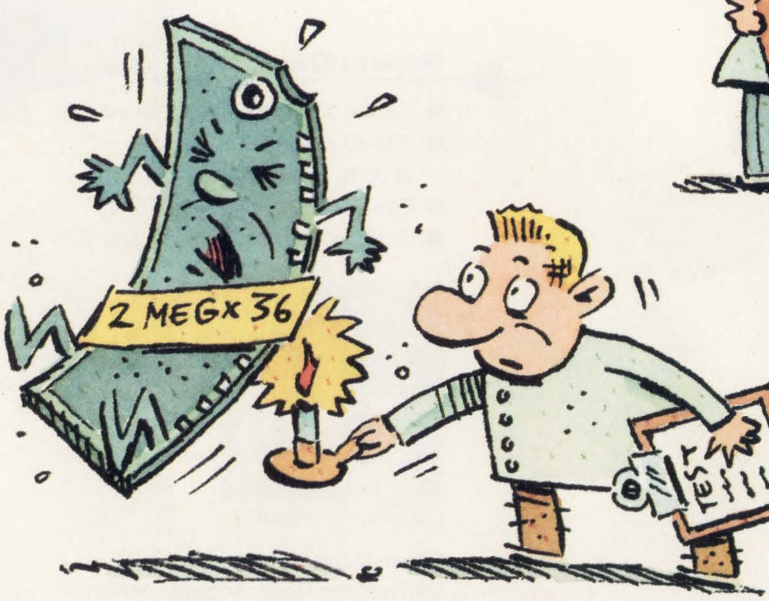

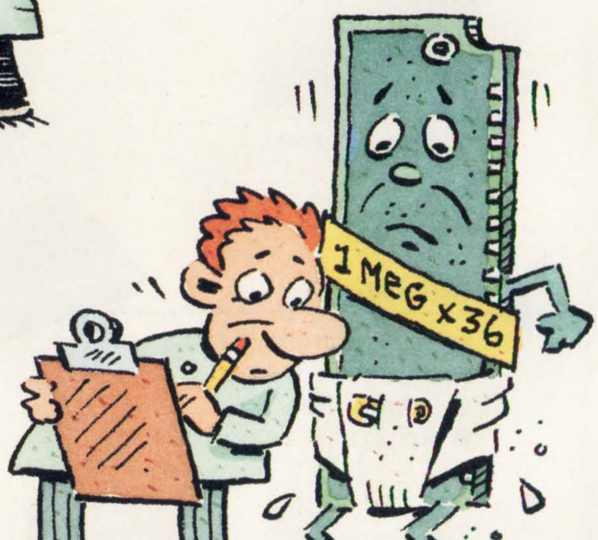

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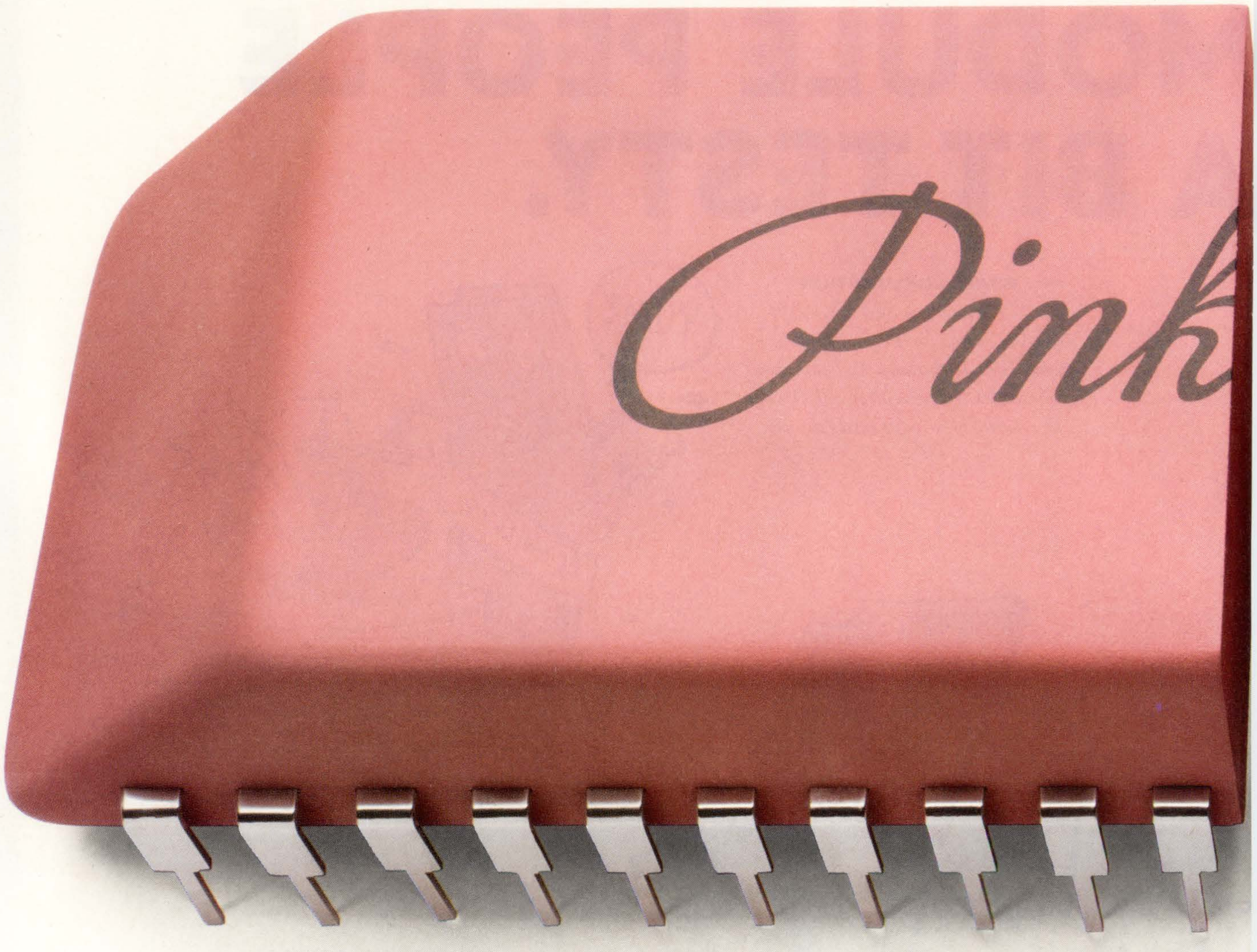

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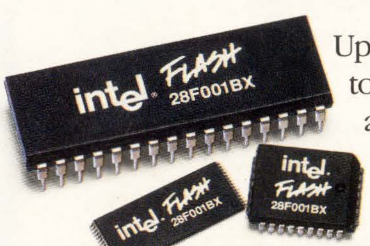

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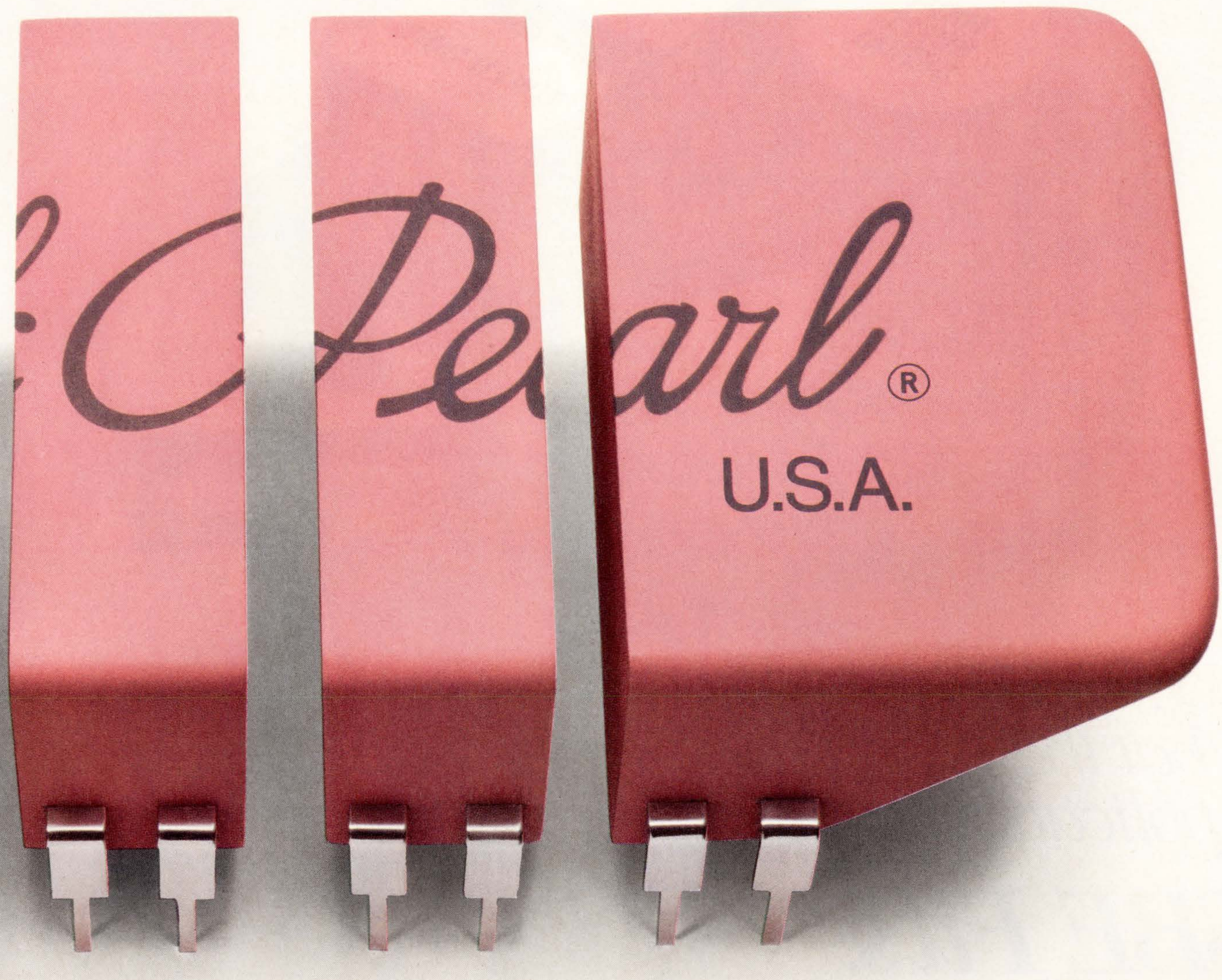

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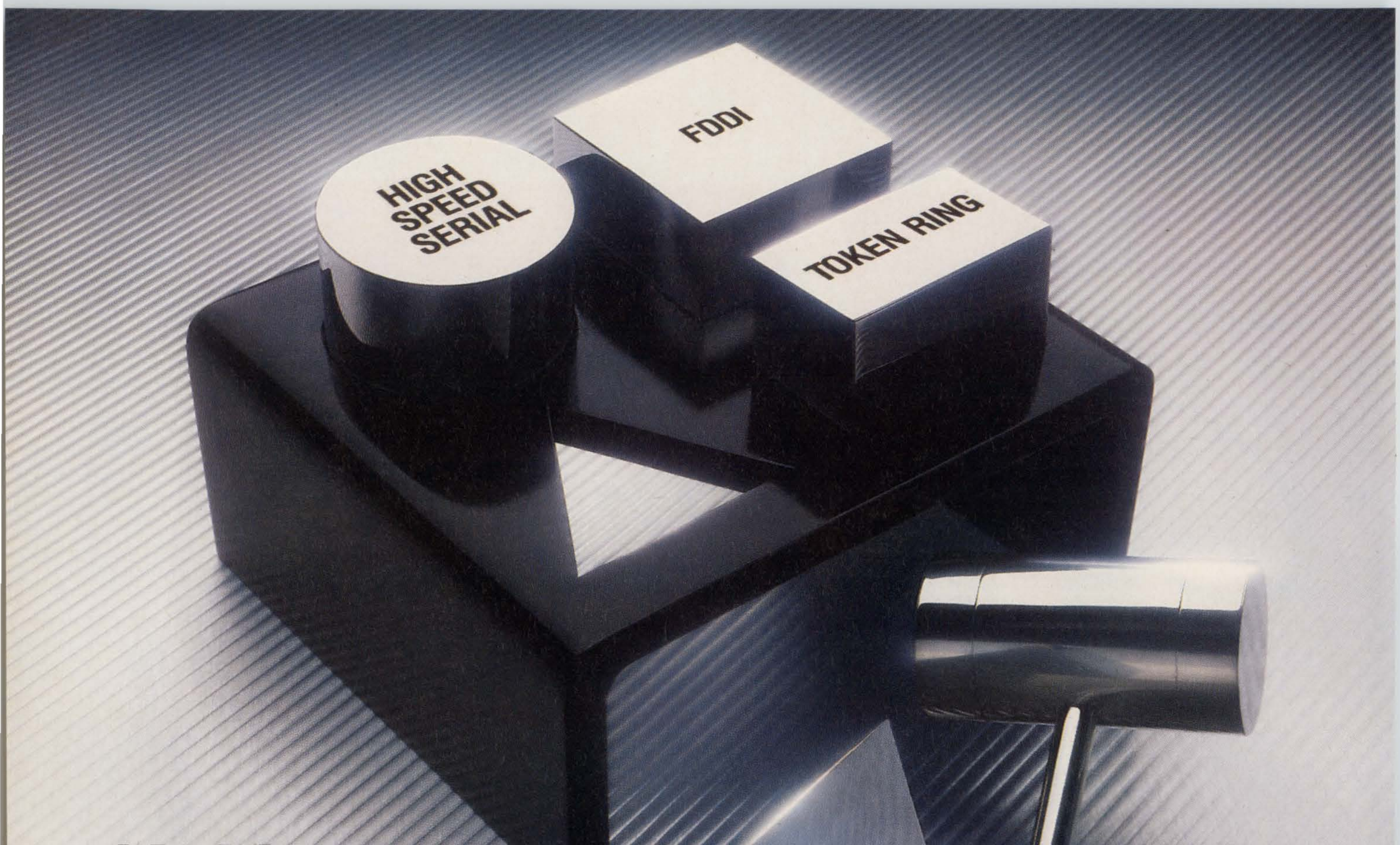
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OVERSAMPLING DATA CONVERSION

Technique bolsters dc-to-audio converters

Their low cost, high resolution, and high linearity make oversampling converters attractive candidates for converting low-frequency and audio-range signals. To make sure they suit your application, take the time to understand their filter characteristics.

Anne Watson Swager, Regional Editor

Contrary to what you might have heard, oversampling data converters won't displace converters with traditional architectures in all applications. However, the ADCs and DACs currently available are particularly adept at two tasks: converting high-quality voiceband and audio analog and digital signals, and converting low-frequency analog signals with high resolution.

For audio applications, oversampling converters exhibit extremely low noise and distortion when converting small signals. For low-frequency applications, oversampling ADCs offer high resolution at low cost. And, unlike integrating and V/F converters, they don't require any external components. Both sets of converters benefit from the oversampling technique's inherent filtering. Unfortunately, this filtering causes one major drawback: The converters can require from hundreds of microseconds to hundreds of milliseconds to complete a conversion.

Fig 1 compares the response of a conventional sampling ADC to two 16-bit

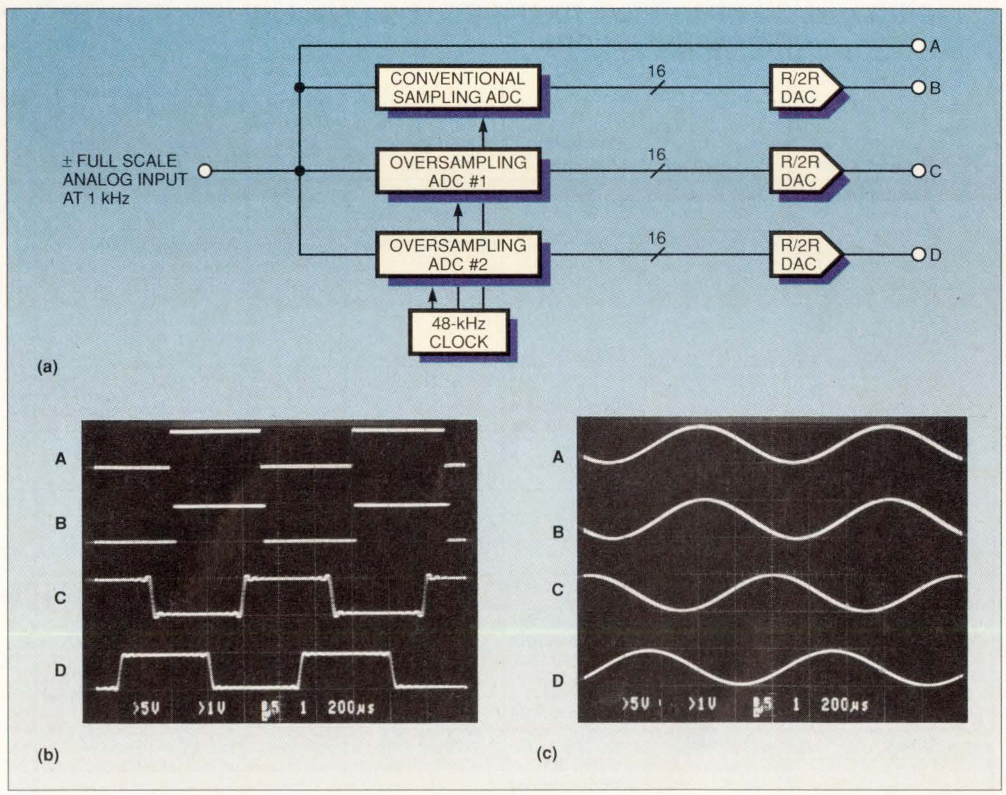

Fig 1—Oversampling ADCs can't easily multiplex *between two inputs because of the time required for an entire conversion. Compared with a conventional sampling ADC* ***(a)****, two different oversampling converters exhibit two different delayed responses to step* ***(b)*** *and sine-wave inputs* ***(c)****. The horizontal scale for these two photos is 200 µsec/div and the vertical scale was normalized so that one division equals ± full scale. (Photos courtesy Analog Devices)*

audio-range oversampling ADCs, all operating at 48k samples/sec. While the conventional converter's delay to a step input is around 20 μsec (**Fig 1b**, trace B), the step and sinusoidal responses (**Fig 1b** and **1c**, traces C and D) of two different oversampling converters exhibit delay times of 400 to 750 μsec. The delays of **Table 1**'s low-frequency converters can be as high as 400 msec.

This delay limits the converters' ability to multiplex their inputs and also can destabilize feedback control loops. Certain converters minimize this delay, as Crystal Semiconductor's new generation of dc converters has done, but oversampling converters operate more effectively on continuous streams of data than they do converting single events.

The inherent filtering defines the converters as continuous-time devices. Oversampling converters are essentially huge filters with analog (or digital) inputs and digital (or analog) outputs. If filtering is an advantage for your application, these converters are a potentially good choice. If filtering is a disadvantage—either because of the delay it causes or because you want to be able to change certain filter characteristics drastically—these converters are a bad choice: You can't take the filter out of an oversampling data converter.

Applying the name *oversampling* to these converters is somewhat imprecise. Oversampling is just one aspect of this conversion technique, which Crystal Semiconductor calls "delta-sigma," Analog Devices and Motorola call "sigma-delta," and Philips calls "bit-stream." Generally, you can use any data converter to oversample just by raising the sampling rate above the Nyquist rate. However, in this article, "oversampling" refers to a technique that combines oversampling, noise-shaping, and digital filtering (see **box**, "Oversampling converters in five languages").

An oversampling converter is the epitome of a mixed-signal device, using about 10% of circuit space for analog functions and 90% for digital ones. A number of the converters listed in **Tables 1** and **2** separate the two functions and accomplish conversions using one analog and one digital device. In some cases, especially if you want to build high-dynamic-range DACs, manufacturers advocate using a building-block approach.

Table 1—Representative oversampling ADCs for low-frequency and high-dynamic-range applications

Manufacturer	Part number	Resolution (bits)	Differential linearity (max)	Integral linearity (max) (%)	Filter characteristics: 3-dB cutoff (Hz)	Filter characteristics: Settling time (msec)	Modulator sampling rate (Hz)	Output rate (Hz)	Input range (V)	Power supply (V)
Analog Devices	AD7701/03	16/20	±0.5 LSB no missing codes	±0.0015	0.1 to 10	120	16k	4k	0 to 2.5, or ±2.5	±5
	AD7710/11/12/13	8.5 to 21	no missing codes	±0.0015	2.62 to 262	400 to 4	20k (varies with gain)	10 to 1000	0 to 2.5, or ±2.5	5 to 10, or ±5
	AD79024	20 (90 to 115 dB dynamic range)	NS	±0.003	9.375 to 300	160 to 5	4M	1k	±2.5	±5
Crystal Semiconductor	CS5501/03	16/20	±0.5 LSB no missing codes	±0.0015	0.1 to 10	125	16k	4k	0 to 2.5, or ±2.5	±5
	CS5505/07 CS5506/08	16 20	±0.5 LSB no missing codes to 18 bits	±0.003	17	50	16.384k	20	0 to 2.5, or ±2.5	5 or ±5
	CS5322 and 23	24 (120 to 130 dB dynamic range)	NS	NS	25.7 to 412	16 to 0.125	23 to 375	62.5 to 1000	±10	±5
	CS5324	NS (120 dB dynamic range)	NS	NS	0 to 500	NA (see comments)	256k	32k	±10	±5 •
Sipex	SP4620	20 (110 dB dynamic range)	±0.25 LSB	±0.012	950	32	512k	2k	±2.5	±5

Notes:
NS=not specified
NA=not applicable

According to Craig Aine, an applications engineer with Philips/ Signetics, separating the analog and digital portions of an oversampling converter reduces crosstalk, thereby improving the system's overall performance. Both Sony and Philips produce 1-bit DACs, which when combined with digital filters produce DACs with an overall resolution anywhere from 16 to 20 bits. Philips' TDA1547, when teamed with the noise-shaping block inside the SAA7350 and a separate digital filter, features a typical dynamic range of 108 dB and a nonlinearity of 0.2 dB, with inputs from −60 to −120 dB.

At the other end of the circuit-complexity spectrum, manufacturers are integrating these converters into even larger devices, such as codecs, echo-canceling modems, and DSP system chips. Both Motorola's DSP56156 ($105 (100)) and Analog Devices ADSP-21msp50 ($93 (100)) integrate oversampling codecs with 16-bit DSP μPs.

Give pros and cons their due

When manufacturers first began marketing these converters a few years ago, the front pages of the data sheets listed an impressive set of advantages:

- No S/H amplifier required
- Digital instead of analog filtering
- No laser trimming or factory calibration required
- Inherent linearity
- Nonexistent or lowered antialiasing requirements.

The first two of these claims are easy to substantiate, but the rest require further explanation. No S/H amplifier is required because of the high oversampling and averaging nature of the technique. A particular ADC's output results not from one sample taken at one instant in time, but from a large number of samples taken over a period of time. Also, digital filters do have redeeming characteristics when compared with analog filters—linear-phase digital filters are easier to design than comparable analog filters. Digital filters don't rely on precise component matching.

The advantage of no factory trimming or calibration doesn't apply to all oversampling converters. However, these converters contain far fewer precision analog components and don't require strings of matched resistors or capacitors. In some cases, dc converters include autocalibration circuits. However, these circuits are completely independent of the oversampling architecture itself. And ADCs designed to perform in the audio range may require trimming if you want to achieve accurate offset and gain specs at data rates higher than those of the dc converters.

Power dissipation (mW max)	Package	Price (100)	Comments
40	20-pin DIP or SOIC	$15/$18	Filter specs based on a nominal clock of 4.096 MHz. Both parts are second sources for the CS5501/03.
40	24-pin double-wide DIP or SOIC	$15/$16/$14/$17	Family of signal-conditioning ADCs with programmable-gain front ends for sampling various types of transducer outputs. Nominal clock rate is 10 MHz. Filter cutoff and gain settings determine overall resolution, output rate, and filter settling time. 7713 draws only 5.5 mW.
50	28-pin DIP, 44-pin quad flat pack	$52	Designed primarily for biomedical and other high-dynamic-range applications.
40	20-pin DIP or SOIC	$18.20/$27.70	Filter specs based on nominal clock of 4.096 MHz.
4.5	20- and 24-pin DIPs and SOICs	$15.70 $18 $11.20 $13.50	CS5507/08 have single-channel differential inputs. CS5505/06 have four pseudo-differential inputs. Converters will either continuously convert, or only sample on demand.
100	2-chip set, 28-pin LCC	$269.70	Five cutoff frequencies selectable over the specified range. Suits seismic and high-dynamic-range applications.
180	28-pin LCC	$217	User must add two stages of external filtering. High-dynamic-range applications. Nominal clock rate is 1.024 MHz.
290	28-pin double-wide DIP	$295	Nominal clock rate is 1.024 MHz. Designed for biomedical-instrumentation, seismic, and other high-dynamic-range applications.

1-bit DAC has ideal linearity

The linearity advantage stems from the fact that most oversampling converters perform a 1-bit D/A conversion in the feedback of the analog-modulator block. This 1-bit converter switches between only two reference points. As Dave Welland, a designer of oversampling converters at Analog Devices, explains it, the modulator picks two points and the filter draws a straight line between them. Thus, 1-bit DACs exhibit ideal integral linearity. If the remainder of the converter's design is perfect, the overall integral linearity of a 1-bit architecture will be close to ideal.

Although the majority of oversampling converters are based on 1-bit architectures, multibit samplers, such as the Sipex's SP4620, also exist. You can't make the same case for inherent integral linearity for multibit systems as you can for monobit systems. A multibit DAC just doesn't have the ideal integral linearity that a 1-bit DAC does. The integral nonlinearity of the SP4620, ±0.012 at full scale, is higher than that of the other converters in **Table 1**. This higher number is due to the device's performance at high signal levels: The S/N-plus-distortion performance tapers off between 84 and 90 dB for low-frequency signals greater than −20 dB. However, according to Eric Blom, the converter's designer, this device's linearity is very close to that of a 1-bit architecture at lower signal levels.

Oversampling converters' differential nonlinearity and monotonicity are more closely related to the noise shaping and filtering (averaging) functions than with the resolution of the modulator feedback. Thus, all of these converters, whether mono-or multibit, feature differential nonlinearity better than ±0.5 LSB. The SP4620's maximum differential nonlinearity is ±0.25 LSB. Manufacturers arrive at these numbers by using statistical measures, such as histograms, rather than the more traditional measurements normally performed on successive-approximation converters.

Be careful not to confuse multibit architectures with something called the MASH architecture. MASH refers to multistage noise shaping, not to multibit feedback. This architecture is most common in audio converters produced by companies such as Matsushita and Sanyo for use in their own audio products.

The modulator portion of the converter isn't the only element of the converter that can affect linearity. Every digital filter in these converters has an accumulator. If the word length of the device's accumulator isn't long enough to handle overflow bits, the filter will truncate the result. This truncation can cause missing codes.

Don't ignore aliasing

The final advantage, and one of the most misunderstood features of these converters, is the reduced or nonexistent antialiasing-filter requirements of oversampling ADCs. Although it's true that the internal digital filter will remove a certain band of unwanted frequencies—the filters' job is to get rid of out-of-band quantization noise—it's also true that oversampling converters are *not* completely free from aliasing problems.

In general, the digital filter does nothing to remove the input spectrum that repeats at integer multiples of the internal sampling rate. For example, those converters with a 10-Hz passband sampled at a 16-kHz rate, will pass to their outputs and not attenuate any components of the input signal near 16, 32, and 48 kHz. In some cases, the converter will also alias input frequencies greater than one half the output word rate.

Unfortunately, because each of these converters' digital filter is different, it's impossible to generalize what type of external filtering will be required with each converter for every application. In some cases, no filter will be necessary. In others, a simple RC filter will provide the necessary attenuation.

The oversampling nature of these converters can also relax input ADC filtering requirements. As the sampling rate increases, the repeated input spectrums spread out more in frequency, and you can use a filter with an even more gradual rolloff to attenuate any unwanted components.

Front-end filtering not only prevents aliasing but also prevents noise spikes riding on the input signal from saturating the analog modulator and digital filter. An input capacitor to ground also prevents those converters with switched-capacitor inputs from kicking spikes back to the driving circuitry.

Concentrate on the filter

Thus, these converters don't let you completely forget about the effects of aliasing, and they even have a few disadvantages of their own:

- Antialiasing filter considerations are still required
- Filter delay disrupts multiplexing
- Filter relay disrupts loop stability.

Note that the word "filter" is common to all the entries in this list. Besides being familiar with an oversampling converter's architecture, understanding the filtering inherent to the conversion technique is the key to properly selecting and applying one of these converters. The oversampling ADCs in **Fig 1** have the same speed, resolution, and bandwidth, but the differences in their filters caused very different delays.

Every filter inside every oversampling converter is unique, and is not necessarily a brick-wall lowpass filter. The converters accomplish the filtering in multiple stages, each of which can have different characteristics. For example, some converters combine comb filters, which have a sin(x)/x response, with a more conventional lowpass filter. The notches of the comb filters in the CS5505 and AD771x families of low-frequency converters (**Fig 2**) help to reject 50- and 60-Hz line frequencies. The CS5505 filter's notch at 60 Hz provides a minimum attenuation of 58 dB over line fluctuations of 1%.

Evaluating the filter characteris-

Oversampling converters in five languages

After working with traditional converters, it's probably difficult to place faith in a device that contains a 1-bit or low-resolution DAC. However, oversampling converters are close relatives of some familiar devices, such as dual-slope integrating converters and V/F converters, all of which use charge-balancing techniques. **Fig A** describes the conversion in five levels, from block diagram to s- and z-domain equations.

Oversampling-conversion techniques rely heavily on one basic fact of all data converters: the conversion process itself introduces inherent error—the quantization noise. The oversampling technique capitalizes on quantization noise. In fact, it intentionally produces a gross amount of the noise, shapes it, and then uses huge filters to dispose of it. ADCs and DACs perform the same basic steps, but in reverse.

For example, the two-step A/D conversion consists of an analog modulator/noise shaper front end and a digital filter (**Fig A**). Two crucial actions take place in the modulator block: oversampling and noise shaping. The combination of a large data rate compared with the bandwidth of the signal and the integrating architecture of the modulator produce noise that increases with frequency. As the s-domain equations and frequency-domain plots show, the modulator block essentially lowpass filters the signal and highpass filters the noise.

The digital-filter block also has two roles: to remove the high-frequency noise produced in the modulator, and to decimate the oversampled bit stream down to the converter's specified output rate.

This simplistic presentation belies the complexity of both the modulator and digital filter. Most real converters contain 2nd-order or higher-order modulators. Instead of the more common 1-bit feedback DAC in the modulator, some converters use multibit feedback. The modulator order, the number of feedback bits, and the oversampling rate all determine the converter's achievable S/N ratio. Unfortunately, converters with higher-order loops can be unstable and susceptible to overloads, so their designs usually include circuitry to sense overload-induced instability.

Just as no two modulators are alike, no two digital filters are alike. These converters usually perform the filtering in many stages: those stages can be FIR (finite impulse response), IIR (infinite impulse response) filters, or both. The overall filter characteristics determine the delay, passband, and stopband levels, as well as antialiasing requirements.

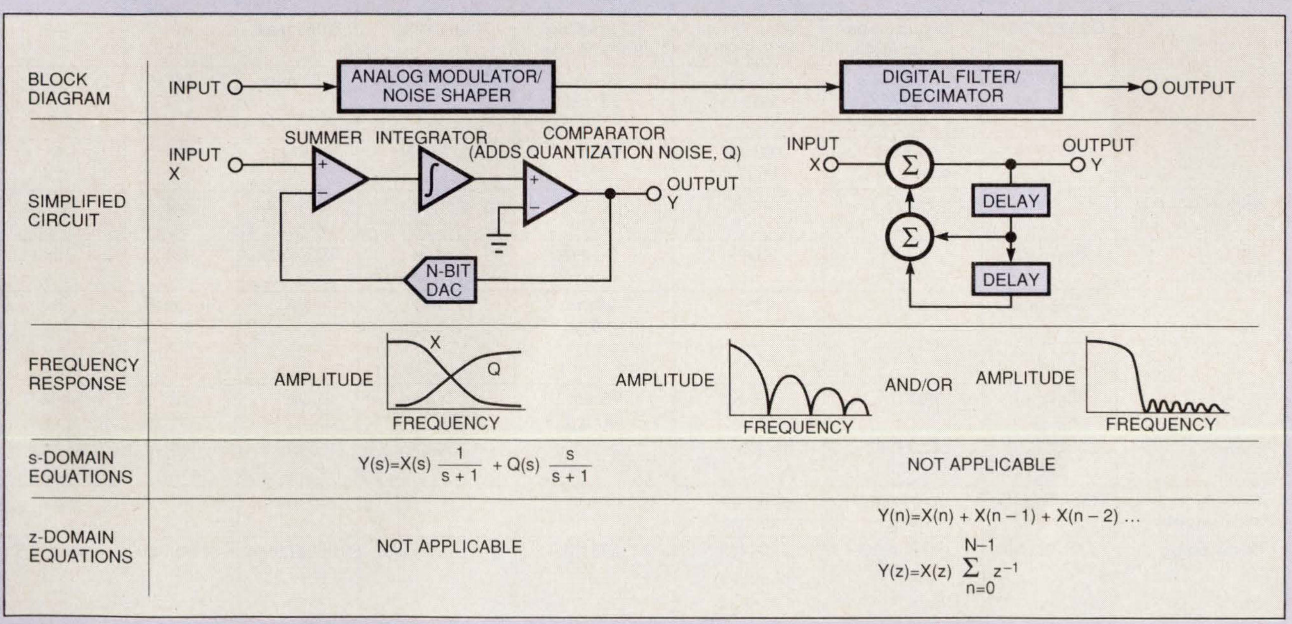

Fig A—Oversampling data conversion requires *two basic steps: analog modulation and digital filtering. You can describe these functions using simplified circuit diagrams, frequency-response plots, and s- and z-domain equations.*

tics of a particular oversampling converter is the most important part of data sheet scrutiny. Most of **Table 2**'s audio converters have filter bandwidths approximately equal to one half the input or output rate. However, the same is not necessarily true for the low-frequency ADCs in **Table 1**. It's particularly important to realize that either the quoted output data rate or modulator sampling rate divided by two is *not* necessarily equivalent to the device's input-signal bandwidth, as it would be in a traditional converter. There are separate specifications for the filter's 3-dB bandwidth, the modulator's sampling rate, and the output rate.

For example, the CS5501/3 and AD5501/3 data sheets quote the filter cutoff as the clock frequency divided by 409,600. Using the recommended clock rate of 4.096 MHz, the maximum bandwidth of the device is 10 Hz. If you based your assumption of these devices' bandwidths on a Nyquist treatment of the maximum output rate of the device, which is 4 kHz, you would erroneously think that the bandwidth is 2 kHz, not the actual value of 10 Hz. In one low-frequency case, the SP4620, the 3-dB bandwidth of the filter happens to be close to half of the device's 2-kHz output rate. However, this Nyquist-type relationship between the filter cutoff and output rate is rare.

The filters' cutoff points scale with the master clock frequency that you provide, but in many cases the converter's designer has optimized the device's performance for a particular frequency. Although most of these converters were primarily designed to operate over a limited range of clock frequencies—

Table 2—Representative oversampling converters for audio and voiceband applications

Manufacturer	Part number	Description	Dynamic range (dB)	S/N ratio + distortion (THD+noise) (dB)	Passband frequency (−3-dB corner)	Passband ripple (dB)	Maximum input rate/ output rate (kHz)	Power supply
Analog Devices	AD1879	18-bit stereo ADC	103 typ	98 typ	21.7 kHz	0.001 typ	55	±5
	AD28msp01	16-bit modem front end	NS	80 typ	200 Hz to 4.8 kHz	0.1 max	9.6	5
Crystal Semiconductor	CS4328	18-bit stereo DAC	95 typ 93 min	94 typ 92 min	0 to 23.5	0.001 max	48	±5
	CS5317	16-bit voiceband ADC	84 typ 78 min	THD only=80 typ 72 min	5	NS	20	±5
	CS5326/7/8/9	16- and 18-bit stereo ADCs	95 to 97 typ 92 to 94 min	92 to 94 typ 90 to 92 min	21.6 to 23.5	0.001 max	50	±5
	CS5336/8/9	16-bit stereo ADCs	95 typ 92 min	92 typ 90 min	0 to 22/0 to 24	0.01 max	50	±5
	CS5349	16-bit stereo ADC	90 typ 88 min	85 min 87 typ	0 to 24 kHz	0.01 max	50	5
Motorola	DSP56ADC16	16-bit ADC	96 typ	90 typ	0 to 45.5 kHz	0.001 max	100	5
Philips/ Signetics	SAA7323	16-bit stereo DAC	93 min	−90 max −95 typ	14.5 to 21.8 kHz	0.035 max	48	5
	SAA7350	1-bit DAC	98 typ	−93 max −96 typ	NA	NA	16 to 53	5
	TDA1547	1-bit DAC	108 typ	96 min 101 typ	NA	NA	NA	±5
Sony	CXD2552Q	1-bit DAC	NS	96 min (SNR only)	NA	NA	NS	5
Texas Instruments	TMS320AD50	Voiceband codec	80 min 84 typ	62 min	20	0.5 max	40	5
UltraAnalog	ADC20048	20-bit ADC	108 typ	−96 typ	21.5 or 23.5 kHz	0.00087 max	44.1 or 48	±15 and 5

Notes:
NS=not specified
NA=not applicable

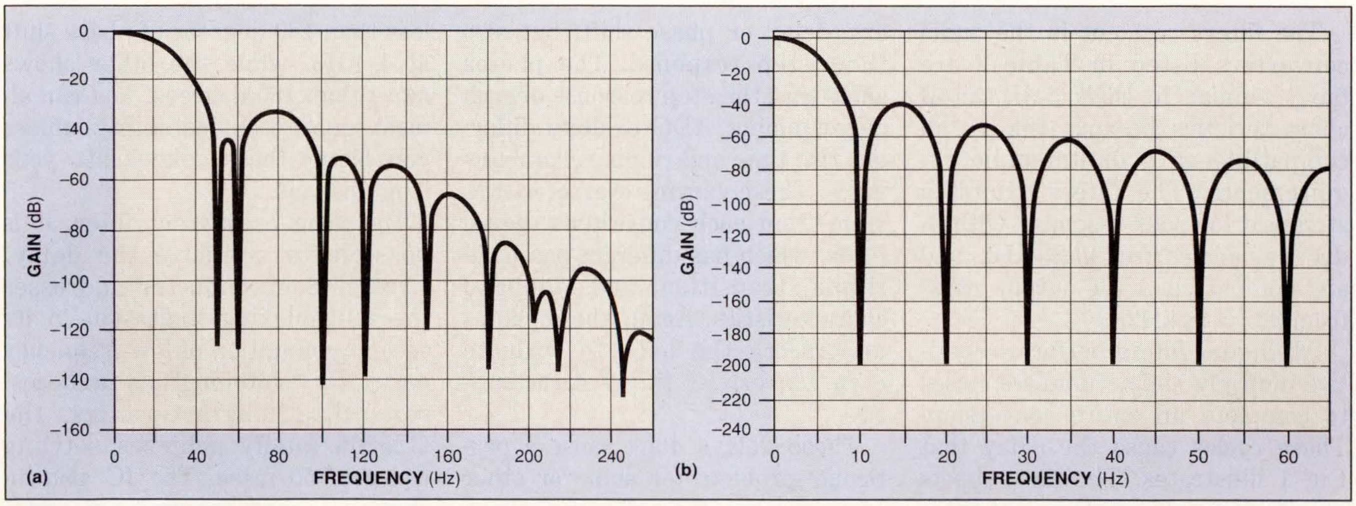

Fig 2—No two oversampling converters' filters are alike. Both Crystal Semiconductor's CS5505 (a) and Analog Devices' AD7710 (b) ADCs use comb filters, but each has slightly different notch characteristics.

Power dissipation (mW)	Package	Price (100)	Comments
900 typ	28-pin DIP	$42	Includes stable voltage reference and two 1-bit, fifth-order modulators.
500 typ	24-pin DIP or SOIC	$21.45	Specialized for echo-canceling. Also operates at other standard modem rates.
600 typ	28-pin DIP or SOIC	$37	Serial port supports four different interface modes.
300 max	18-pin DIP or 20-pin SOIC	$29.40	Intended for applications such as modems, sonar, and voice-recognition systems. Includes on-chip phase-lock loop.
450 typ	28-pin double-wide DIP	$70.56/$80.90/ $84.70/$97	The CS5326/8 have filters with CD requirements.
400 typ	28-pin double-wide DIP 28-pin SOIC	$56.40	Same modulator in CS5326 family, but different digital filter. CS5336 has 22-kHz cutoff, 8/9 have 24-kHz cutoff.
425 max	28-pin double-wide DIP	$56.40	Includes 2V reference.
400 max	20-pin DIP	$19.80	Specifications listed for 16-bit output. 12-bit output is also obtainable at a 400-kHz rate.
300 typ	44-pin quad flat pack	$16.51	Lower performance version, the SAA7322, is also available.
375 typ	44-pin quad flat pack	$26	Requires either front-end DSP μP or digital filter to achieve specs listed. External clock typically equals 256 or 384X sampling frequency, which is typically 44.1 kHz, but can range from 16 to 53 kHz.
800 typ	32-pin shrink DIP	$17.50	Performance specs achieved by using a separate digital filter and SAA7350 noise shaper's output.
400 max	44-pin quad flat pack	$7.50	S/N ratio listed requires an accompanying digital filter, such as the CXD1144BP ($36).
45 typ	25-pin LCC	$10	Device is also available as a megacell module in the company's DSP cell library.
2800 typ	2×3-in. module plus 48-pin DIP	$164	Multibit architecture in the analog front end.

an attribute common to almost all oversampling converters, and particularly true of audio converters—many devices in **Table 1** let you program the filter characteristics. As the filter cutoff changes, so does the filter's settling time and the converter's resolution.

For example, the AD771x family of signal-conditioning ADCs lets you program the filter cutoff from 2.62 to 262 Hz via a 12-bit control register. Data-sheet tables relate the internal $(\sin(x)/x)^3$ filters' first notch to the 3-dB frequency and the final resolution. This converter family also contains programmable-gain amplifiers, so that another table relates the above characteristics to your chosen gain. At the maximum master-clock frequency of 10 MHz, the minimum cutoff frequency is 2.62 Hz, and the maximum programmable cutoff frequency is 262 Hz. The effective resolution of the device—measured as the magnitude of the output rms noise to a full-scale input—varies between 21 and 8 bits as you change these cutoff points. The resolution is highest at the lowest cutoff frequency, and lowest at the highest cutoff frequency.

Oversampling data conversion

The filters resident in the audio converters listed in **Table 2** are fairly similar in their 3-dB cutoff characteristics because they're all compatible with digital-audio requirements. The filters exhibit a standard lowpass response with 3-dB frequencies around 20 kHz, and are compatible with output rates from 32 to 48 kHz.

All digital filters perform repetitive multiply and accumulate cycles to complete an entire conversion. These cycles cause the delay that **Fig 1** illustrates. The data sheets specify the delay in terms of filter settling time. For these converters, the filter settling time is more of a last-output-change to present-output-change number, or simply the inverse of the output data rate.

Fig 1's photos make a strong point, not only about the converters' delay or phase shift, but also their step response. The photos show that the step response of each oversampling ADC exhibits different rise time and ringing characteristics. These varying characteristics stem from each converter's digital filter, which has different passband ripple, transition, and stopband characteristics. Again, these photos underscore the need to evaluate each converter's filter characteristics.

These delays don't cause a particular problem for audio or other systems that typically work from continuous streams of data. However, they do cause substantial phase shifts at relatively low frequencies and can cause major problems in feedback control systems. In **Fig 1**'s examples, one converter's sine-wave response shows slightly less than 180 degrees of phase shift at 1 kHz, while the other shows more than 180 degrees. You can almost guarantee instability unless you factor these delays into your loop analysis.

By using a different filter, it is possible to minimize the delay. Crystal Semiconductor addresses the multiplexing limitation in its second generation of low-frequency parts. By "softening" its predecessor's filter characteristics, the CS5505 family achieves settling times of 50 msec. The IC also includes a convert-control pin and a data-ready flag similar to a successive-approximation converter. The device also includes a 4-channel multiplexer.

Converter vendors also argue that the commercial availability of ADCs in the $10 to $20 range challenges the traditional data-acquisition design approach. If you use one ADC per channel, the multiplexing problem doesn't exist.

For more information . . .

For more information on the oversampling converters discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Idle tones exist

Although the multiplexing issue is an important system consideration, oversampling converters exhibit other subtle effects that can influence your system's performance. Low-frequency noise, known as spurious or idle tones, is a potential problem unique to the oversampling-converter architecture. Like any other electronic component, the behavior of oversampling converters isn't ideal. The converters produce a large amount of quantization noise that ideally has no relationship to the input signal. In reality, however, the nature of the input can have an affect on the performance of the converter's analog modulator.

For example, an input signal whose dc level lies very close to the transition point of the modulator's sampler creates a very small-error feedback voltage. The modulator

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has to integrate many of these small errors to change states. A very low-frequency signal results that persists through the digital filter to the output.

This signal manifests itself as a low-frequency tone in the passband. The converter's designer can reduce the production of unwanted tones by designing higher-order modulators, but higher-order modulators extract their own design penalties because of instability. Multibit architectures generally have lower tonal effects than do single-bit architectures.

Unfortunately, there isn't an easy way to evaluate the existence or level of these tones from the data sheet. Depending on their level, these idle tones may not be a problem for your application. Also, you may be able to shift your dc operating point away from the transition region.

Once aware of their drawbacks, you can decide whether oversampling converters will benefit your dc-to-audio converter requirements. However, don't expect the designers of these converters to forever be content with just dc and audio frequencies. According to Randy Skinner, a marketing manager at Burr-Brown, which will soon offer audio DACs based on this technique, "everything that can be invented using oversampling technology, hasn't been invented yet," and oversampling converters will invariably work with wider bandwidths in the future. EDN

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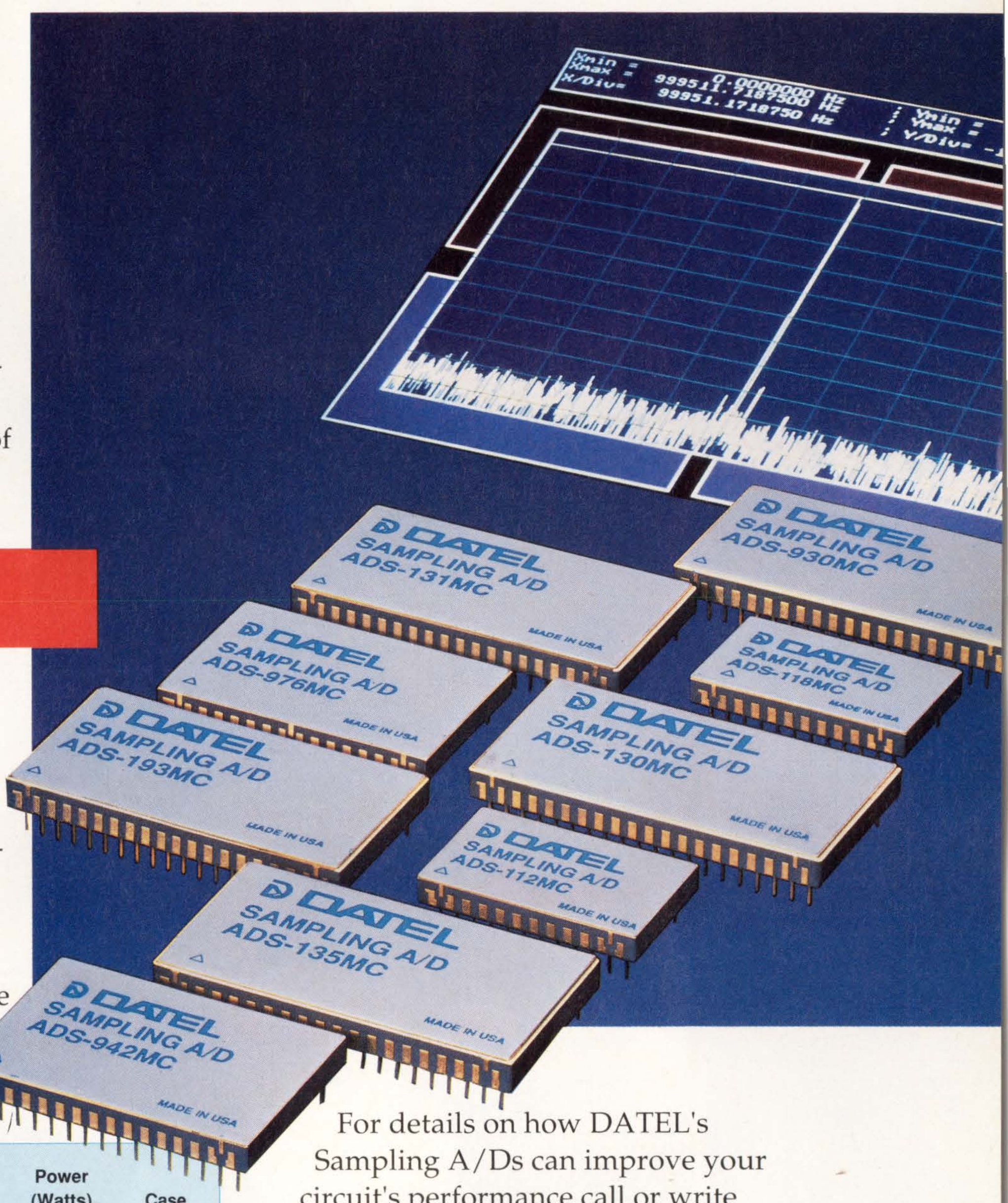

Model	Bits	Throughput (MHz)	Linearity (LSB)	Power (Watts)	Case
ADS-111	12	0.500	±1/2	1.3	24-PIN
ADS-193	12	1.0	±1/2	1.3	40-PIN
ADS-112	12	1.0	±1/2	1.3	24-PIN
ADS-117	12	2.0	±3/4	1.4	24-PIN
ADS-132	12	2.0	±1/2	2.9	32-PIN
ADS-118	12	5.0	±1/2	2.3	24-PIN
ADS-131	12	5.0	±3/4	3.6	40-PIN
ADS-130	12	10.0	±3/4	3.8	40-PIN
ADS-924	14	0.300	±1	1.3	24-PIN
ADS-928	14	0.500	±1/2	2.9	32-PIN
ADS-941	14	1.0	±3/4	3.1	32-PIN
ADS-942	14	2.0	±3/4	3.2	32-PIN
ADS-944	14	5.0	±1	3.4	32-PIN
ADS-976	16	0.200	±2	1.8	32-PIN
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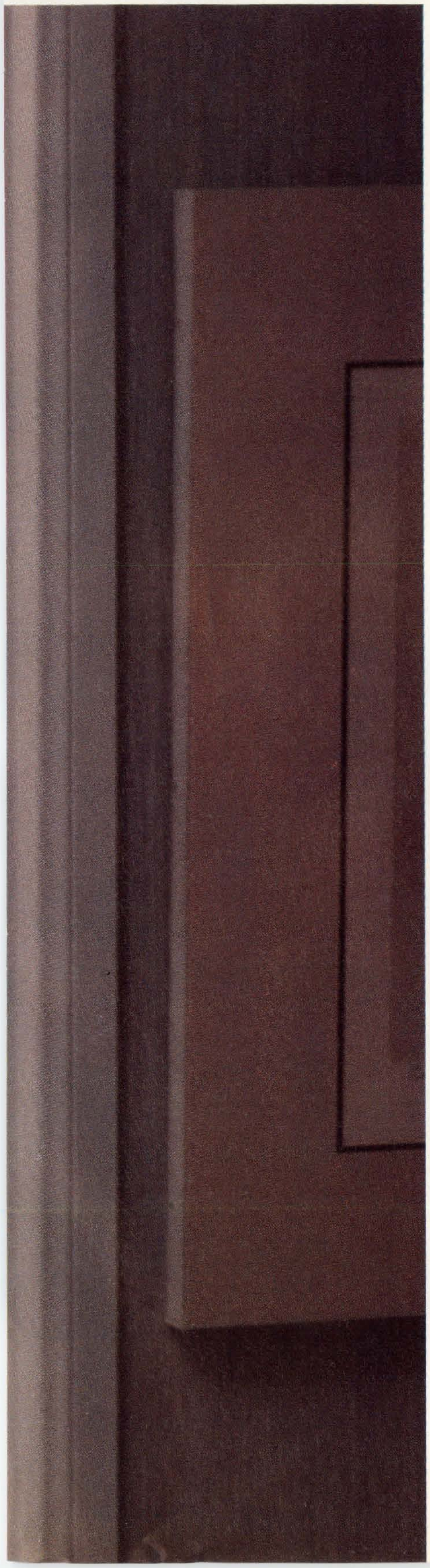

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TEXAS INSTRUMENTS

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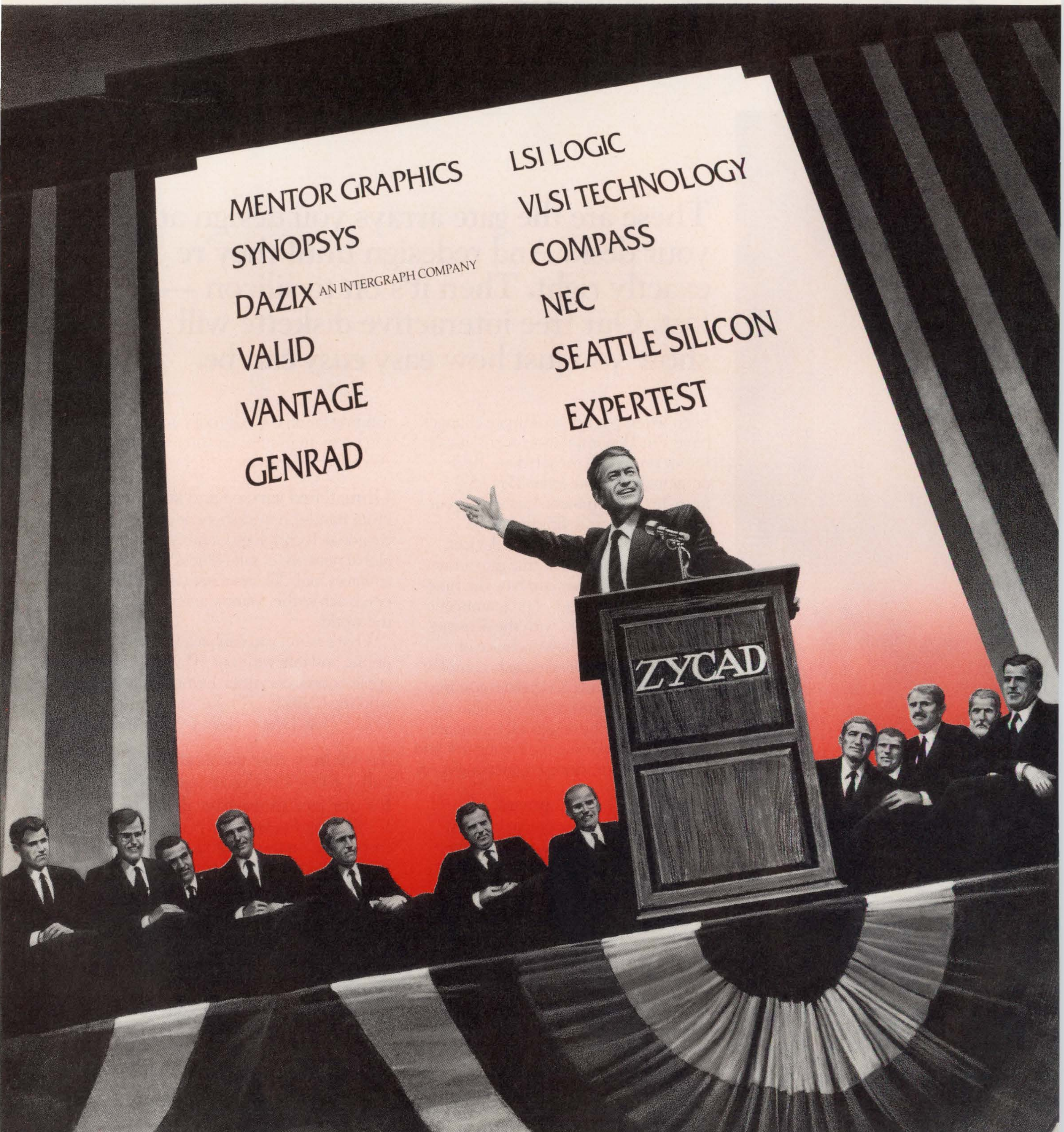

And Who's Leading It?

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CAE STANDARDS

Framework teams strive to build standards

The CAD Framework Initiative has begun to polish the tarnished image of committee-based standards development. With a new structure in place, they aim to accelerate achieving a framework standard.

Michael C Markowitz,
Associate Editor

The CAD Framework Initiative's (CFI) goal is the "development of worldwide industry standards for electronic design automation tools and their supporting framework environments that will remove barriers to integration." As CFI demonstrated at the recent Design Automation Conference, they have made great strides toward delivering on this goal. And a recently announced decision to restructure the CFI aims to accelerate the delivery.

Many definitions of a framework exist. One definition calls a framework a software infrastructure that provides a common operating environment for CAE tools. Perhaps a broader and better conceptual definition equates a framework to a collection of software services and utilities that operate on a CAE database. You should recognize, however, that while this discussion focuses on the work of the CAD Framework Initiative, frameworks can have a much broader scope. Frameworks can encompass CASE, mechanical CAE, and data and tools residing anywhere in an organization.

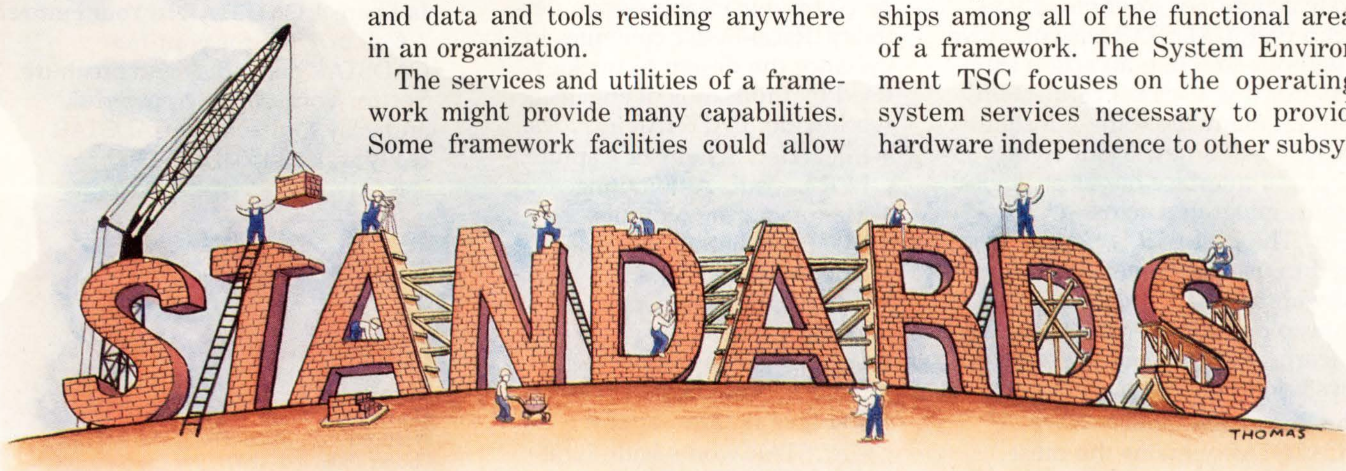
The services and utilities of a framework might provide many capabilities. Some framework facilities could allow you to launch, manage, and use diverse collections of tools and provide a means of both static and dynamic intertool communications. Other services could create, organize, and manage enormous amounts of design data. Still other framework tools could provide a means of managing the design process itself by enforcing company-defined sequences and methods.

Many of these features go well beyond the users' initial, and perhaps naive, demand for compatibility of their design tools. Superficially, compatibility appears to be a problem of user interface and intertool communication. Fortunately, CFI recognized much of the depth and breadth of the problems inherent in frameworks from the outset and built its volunteer organization to address seven critical areas via technical subcommittees (TSCs).

TSCs make problems manageable

According to CFI documents, the Architecture TSC is responsible for the interdependencies and interrelationships among all of the functional areas of a framework. The System Environment TSC focuses on the operating-system services necessary to provide hardware independence to other subsys-

Rod Thomas



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tems within the framework. The Design Data Management TSC's purview is to address the mechanisms for storing, accessing, and versioning design data. Defining the specification for that part of the framework that organizes the activities necessary to create and complete a design is the Design Methodology Management TSC. The Design Representation TSC concentrates it efforts on the conceptual data models that describe the various elements of the design. Ensuring the definition of the mechanisms for efficient sharing of design information between tools is the Intertool Communications TSC. Finally, the User Interface TSC covers that portion of the system that manages all interactions with the designer or other user.

One initial shortcoming of CFI was its failure to address the problem caused by the burgeoning variety of libraries. Bill Johnson, Director of CAE for Sun Microsystems, sees the separate but related libraries that his organization must maintain, for such diverse tasks as synthesis, simulation, and purchasing, as his biggest headache. The CFI added an eighth TSC in February to address issues related to the digital representation and distribution of electrical components such as models and libraries. Recognizing the enormous efforts required to support, drive, and chair a TSC, CFI created the chairman's post for the Component Information Representation TSC as a full-time position.

These eight subcommittees contributed to the DAC '91 Integration Project. This project highlighted the progress made on draft standards in tool encapsulation, data representation, and intertool communication. CFI wrote the draft standards with an eye toward both the Integration Project and the organization's planned November 1991 release of the CFI 1.0 framework specification.

Listing 1–Tool abstraction specification for Blossom timing analyzer

```
(cfitool  1 "SONY blstv" 1
    (tool    "SONY"
        (versionlist "1.0")
        "/usr/sony/bin/blstv_script"
        (description "SONY BLOSSOM"))
    (arguments
        (arg_string cell_library_i
            (get_input cell_library_i)
            (label "cell_library:")
            (default /usr/sony/dacLib/demo/clb/demo"))
        (arg_string cell_library
            (concat "-1 " (value cell_library_i)))
        (arg_boolean line_editing
            (iftrue "-e")
            (iffalse "-ne")
            (label "Line_Editing")))
   (data
        (datadef cell_library_data
            (direction input)
            (argref cell_library_i)))
    (structure
        (commandargs
            (value cell_library)
            (value line_editing))
        (env "host" "sun")))
```

To perform tool encapsulation, the Design Methodology Management TSC defined a tool abstraction specification (TAS) that tells the framework what information is necessary to launch a particular tool as well as what to do with any code the tool returns after launching. This specification is unique for every tool and could contain such information as the tool's name, version number, location on the host system, tool parameters, argument declarations and definitions, data declarations, command-line syntax definitions, and result-code declarations that aid in determining a tool's termination state.

Listing 1 is a simple TAS for Sony Corporation's Blossom static-timing-analysis tool. The advantage of the specification is that each tool would have a single TAS, which vendors could package with their tools, so you could truly plug-and-play into CFI-compliant frameworks.

Despite the appeal that the TAS offers, you must recognize that it only provides "loose integration." While the specification provides tool-launch facilities, it doesn't yet address more complex issues such as tool dependencies and design-data management capabilities. The CFI will concentrate on these needs next.

To emphasize the preliminary nature of the encapsulation shown at DAC, Laurence Brevard, Chairman of the Design Representation TSC and author of the CFI '91 Integration Project description, suggests "cockpit" as a more accurate and descriptive term than framework for the type of encapsulation that the TAS achieves. (In addition to calling the framework a cockpit, CFI classed all netlist-generating tools as "producers," all netlist-using tools as "consumers," and facilities that store design information as "DR (Design Representation) Servers.")

Design representation was deemed important for its promise to eliminate the data translators often needed to move data between tools. Progress in design representation started when its TSC extended the information model for electrical connectivity developed for last year's demonstration at DAC. The new model offers the netlist connectivity information that helped define the programming interface operations the TSC would have to provide. The draft programming interface allows read, create, and modification of design data in three levels of hierarchy: a top cell, composed of intermediate cells, which are ultimately built from primitives. Last year, the TSC implemented the ability to create and use nets. This year's draft specification makes both nets and ports able to use bundles.

According to Laurence Brevard, the nomenclature was often a big-

CFI's membership

The CAD Framework Initiative's member roll currently numbers 44 companies. Although these companies fit into three general categories—hardware vendors, software vendors, and end users—the companies may have several internal organizations participating in the discussions representing their various interests.

This list is far from comprehensive. A number of nonmember vendors currently take the politically expedient position that they are closely following CFI's progress and evaluating their membership roles. Their reasons for not currently belonging to the organization run the gamut. Although President and CEO of OrCAD, John Durbetaki, promises his company will ultimately join CFI, he doesn't see OrCAD as the pioneer in this case.

One problem common to smaller companies is the commitment of engineers and dollars to the effort. Tony Wainwright, president and CEO of IC-layout and verification-tool vendor Silvar-Lisco, plans on increasing his company's level of involvement once CFI reaches a point where the company's involvement might pay off. Similarly, John Willey, VP of marketing at Vantage Analysis Systems, thinks his company has to pick its battles. Vantage is carefully following CFI's progress but currently feels that the members will work toward the best possible solution, and Vantage has little that it can add.

Bryce Baker, CAE Manager at Gould AMI expressed another concern. His company hadn't joined CFI out of concern for the political infighting that he expected would occur. Such politicking does occur—two oft-mentioned examples include the discussion over the user interface (Motif versus Open Look) and the extension language (Lisp-based Scheme versus something C-based). In spite of this action though, Baker is impressed by CFI's progress and is re-evaluating his company's decision.

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ger hurdle for the TSC than you might expect. The subcommittee chose the term bundle because the term "bus" came with too much baggage and wasn't broad enough—the committee defined "bus" as a uniform indexed array of signals. In contrast, in VHDL (VHSIC Hardware Description Language) contexts, a bus is one signal with multiple drivers. A "composite signal" is the term often used in VHDL to refer to a uniform indexed array. The TSC defined "bundle" as a group of signals that can be either indexed or individually named.

The Intertool Communications TSC defined a programming interface for creating, sending, and receiving messages to allow tools and services to communicate with and potentially control each other. The interface uses a multicast message system that offers two types of messages. In both types, neither the sender nor the receiver knows of each other; the receiver's "address" and the message's "content" determine delivery. The first message type is a *notification message*, which is generally of interest to many tools. Notification messages simply announce a change of state. In contrast, a *request message* is captured by only one tool and causes an action to occur.

At the Design Automation Conference, CFI demonstrated all of these specifications integrated into several software tools from member companies. These tools were then run on several networked, heterogeneous workstations. CFI also announced a new membership structure that includes four levels of membership. This restructuring was necessary, according to CFI President Andy Graham, because of concern that CFI didn't have the resources and infrastructure to finish the task of establishing the framework standard.

The restructuring will allow CFI to accomplish several tasks. The organization will hire several full-time staff members to supplement and accelerate the volunteer committees; organize a prototyping project to test standards proposals; create conformance tests for adopted standards; and establish or contract for laboratory facilities.

After determining its needs, CFI created a Sponsor class of membership, which charges $125,000 to each of ten Sponsor members. Currently, six vendors—Cadence Design Systems, Digital Equipment Corp, Hewlett-Packard, IBM, Mentor Graphics, and Sun Microsystems—have contributed. According to Tony Zingale, Director of Marketing for Cadence Design Systems, the reason for contributing is simple: "We want CFI to succeed."

In return for the $125,000, each sponsor can assign people to the labs, where they can see and learn of integration problems and issues first hand. The fee also prepays any conformance-testing software that CFI develops. The least tangible benefit—but the one most emphasized by the sponsors—is the promise that the market will grow when the framework standards are adopted. CFI's Graham likens the sponsor membership dues to ordering a full dinner versus ordering your meal a la carte. However, the money doesn't buy increased influence with the committees.

According to Hewlett-Packard's Group Market Segment Manager for EDA, Dick Lubinski, many of the smaller CAE players have expressed concern that the sponsor members will have greater weight in railroading their favorite standards through the committees. Bill Johnson, Director of CAE at Sun Microsystems and CFI Board Member, says that the smaller players needn't worry. The board recognized that smaller companies would have greater difficulty coming up with large membership fees and wanted to ensure their continued

For more information . . .

For more information on the CAD Framework Initiative, circle the appropriate number on the Information Retrieval Service card or use EDN's Express Request service. When you contact CFI directly, please let them know you read about them in EDN.

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FAX (512) 338-3853
Andy Graham
Circle No. 700

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input. As a result, the Sponsor membership was created essentially as a means for the larger, more established CAE vendors to subsidize the smaller players.

One of the larger CAE vendors, Valid, isn't currently a sponsor. According to Senior Product Marketing Manager Larry Rice, the company might be seen as selfish, but it believes its customers would rather see it invest in implementation of the standard rather than the development of it. The company values its membership, feels it has much to contribute as a corporate member ($10,000), and thinks it spends significantly more than the $125,000 already—via the people it sends to meetings.

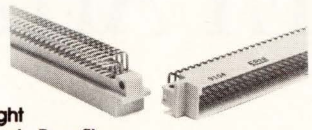
Other large vendors—among them Racal-Redac and Siemens-Nixdorf—are evaluating Sponsor membership. Julia Miller, Manager of US Framework Activities for Siemens-Nixdorf, said the company was evaluating sponsorship and whether sponsoring CFI would jeopardize the funding her company receives from JESSI (Joint European Submicron Silicon Initiative) and the European Community.

Although appearances are often deceiving, all of the CFI sponsors spoke with one mind in regard to their investment as being a means for expediting the standard's development. As CFI rushes to deliver its 1.0 specification, it will be interesting to see how quickly the vendors incorporate the specification into their tools. EDN

Reference

1. Brevard, Laurence, *The CFI '91 Integration Project*, CAD Framework Initiative Inc, 1991.

Article Interest Quotient
(Circle One)
High 509 Medium 510 Low 511



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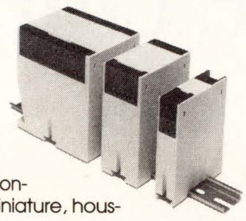

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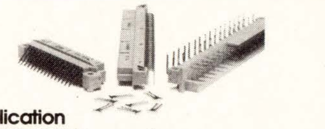

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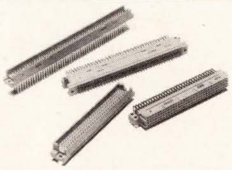

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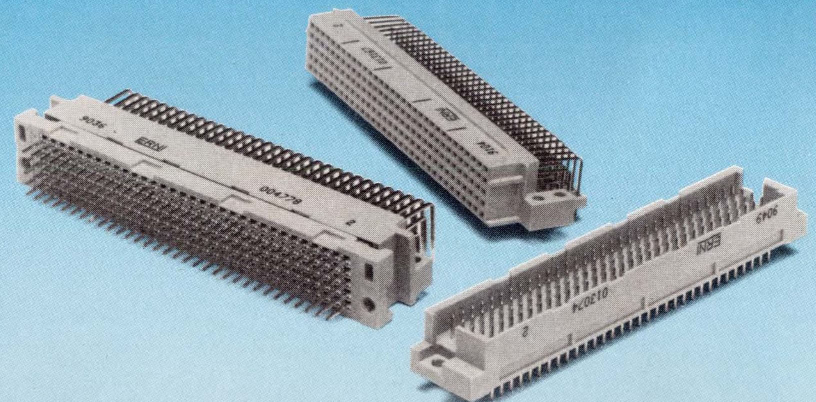

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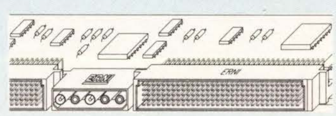

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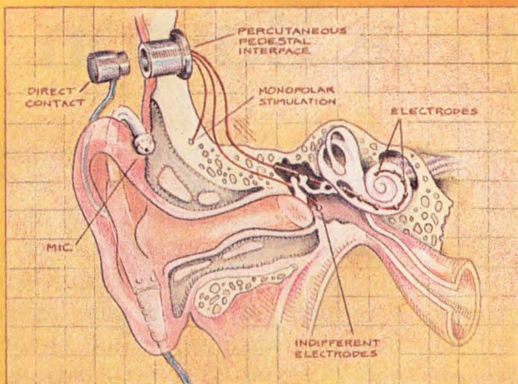

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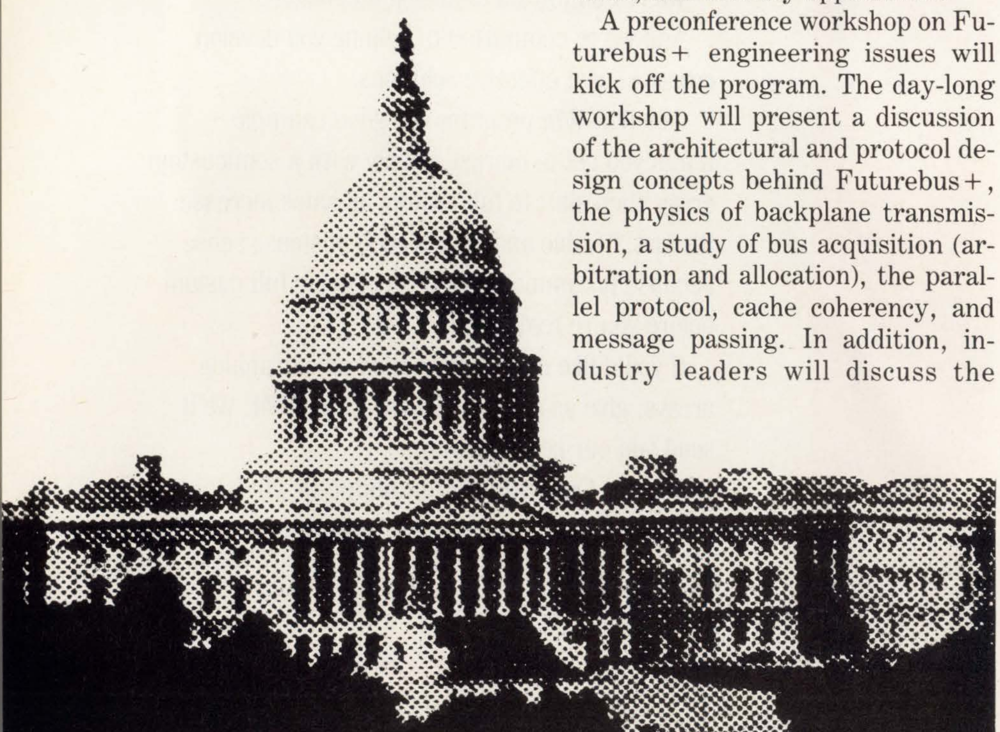
Keep pace with bus technology at Buscon

Julie Anne Schofield,
Associate Editor

Buscon East moves to Washington, DC, this year and will once again afford attendees the opportunity to discuss and evaluate new products, observe hands-on demonstrations, and keep pace with the electronics industry. The show will be held Tuesday, September 10 through Friday, September 13 at the Omni-Shoreham Hotel.

Two exhibit floors will showcase the latest products and technology from more than 150 vendors. Included in the variety of products presented will be bus boards of all architectures, systems software, card cages, connectors, communications software, graphics software, chips, and a host of other products for commercial, scientific, government, and military applications.

A preconference workshop on Futurebus+ engineering issues will kick off the program. The day-long workshop will present a discussion of the architectural and protocol design concepts behind Futurebus+, the physics of backplane transmission, a study of bus acquisition (arbitration and allocation), the parallel protocol, cache coherency, and message passing. In addition, industry leaders will discuss the emerging profiles and related specifications and their impact on Futurebus+. Because of the highly technical nature of this session, attendees should have engineering knowledge of bus transfer mechanisms, transmission-line theory, and TTL and BTL (bipolar-transistor logic).



The following three days offer a series of full- and half-day sessions, nearly half of which are new for 1991. Topics will include the Sbus, peripheral interfaces, advanced networking, real-time software, Futurebus+ management perspectives, the VMEbus, Futurebus+ silicon issues, and Multibus II. *Defense Electronics* magazine is coordinating a session on military applications.

The Sbus business

The morning part of Wednesday's Sbus session aims to provide card and system developers with a thorough understanding of the technical issues in areas such as hardware design, DMA control, firmware, programming environments, and device drivers. Also included in this session is an overview of Sbus business opportunities. The afternoon session addresses the basics, tools, and actual practice of using Forth in the Sbus environment.

Thursday's full-day session on real-time systems software is divided into two parts: a software-management/design-tool seminar in the morning and an in-depth technical view of critical issues, such as the differences between real-time kernels and Unix, in the afternoon.

Two other bus sessions are the

Buscon/91 East program schedule

	Tuesday, September 10	Wednesday, September 11	Thursday, September 12	Friday, September 13
8:30 am to 4:30 pm	**Session 101** Futurebus+: Engineering considerations	**Session 201** Sbus	**Session 301** Real-time systems software	**Session 401*** Military applications
8:30 am to 12 pm		**Session 202** Peripheral interfaces—SCSI-2 and beyond	**Session 302** Futurebus+: Management perspective **Session 303** VMEbus	
1 pm to 4:30 pm		**Session 203** Advanced networking	**Session 304** Futurebus+: Silicon issues **Session 305** Multibus II	

*Session ends at 2:30 pm.

VMEbus session Thursday morning and the Multibus II session Thursday afternoon. The VMEbus session will provide attendees with an update on the VME specifications as well as details on how the VMEbus has been expanded to 64 bits. Attendees of the Multibus II session will hear about the bus's expanding role in the open-systems market. They will also learn about backplane advances, hot-board insertion, communications technology, connectivity, military versions, and RISC-processor support.

Don't miss the bash

Rounding out the program will be the presentation of the Buscon Product of the Year award at the Buscon Bash, Thursday, September 12, from 5:30 to 7 pm. The winner will be the vendor who has contributed the most substantial technical innovation to the industry over the past year. EDN Editor Jon Titus will be among the judges.

Several registration options are available. Passport #1 costs $695 and entitles you to attend the Futurebus+ preconference workshop, one full-day session each day of the conference, the exhibition halls, and the Buscon Bash. You'll also receive a copy of the official conference proceedings. Passport #2 costs $545 and entitles you to all the privileges of Passport #1 except admission to the preconference workshop September 10.

Tickets for the preconference Futurebus+ workshop cost $255. Full-day sessions cost $245 each; half-day sessions cost $145 each. Seminar registrants receive free admission to the exhibition. Registering for the exhibition at the conference will cost $10. Exhibit-hall hours are 10 am to 5 pm on Wednesday, September 11 and Thursday, September 12, and 10 am to 4 pm on Friday, September 13.

To obtain more information on Buscon/91 East, contact Buscon/91 East, CMC, 200 Connecticut Ave, Norwalk, CT 06856; phone (203) 852-0500; FAX (203) 857-4075. To register for seminars or sessions, phone (800) 243-3238. EDN

Article Interest Quotient
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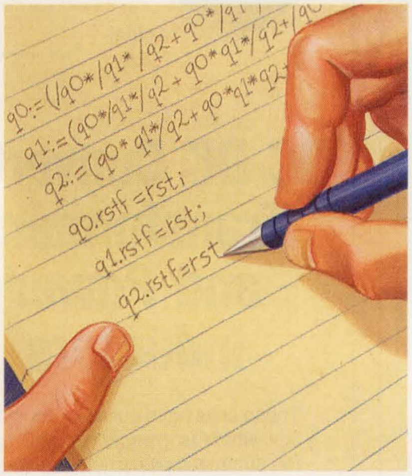
High 512 Medium 513 Low 514

You Design Actel FP
You Do A PLD. But Th



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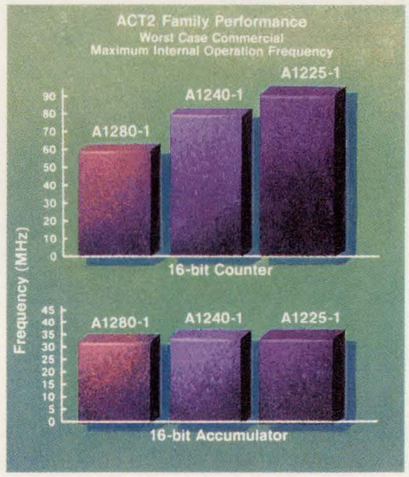
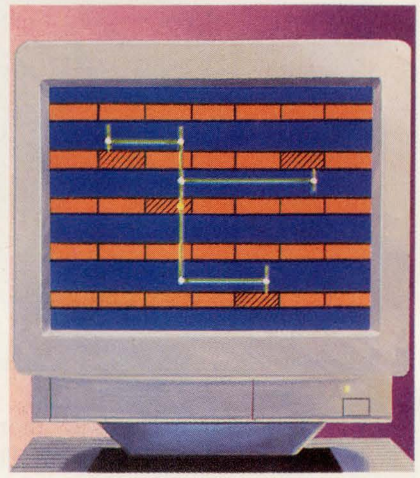


Fast. Fast. Fast.

Our FPGAs are real speed demons. Whatever application you may be working on, our parts will give you the kind of performance you're looking for.



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Coupled with your PLD tools, Actel's Action Logic™ System (ALS) software lets you create your own FPGAs—using a 386 PC or workstation—right at your own desk. With Auto Place and Route that's proven in thousands of applications.

Announcing A Simple Way To Get From PLDs to FPGAs.

If you're a PLD designer with an interest in fast, flexible FPGAs, but you think you don't have time to learn new design techniques, we'd like to change your mind.

Actel's ALES™ 1 program translates the output of PLD tools like CUPL™ and LOG/iC™ into logic optimized for our ACT™ devices. Entire FPGA designs can be developed with PGA Designer.™ ABEL™ 4.0 includes optimization for Actel devices. You don't have to give up your existing PLD design tools or Boolean equations.

Actel devices offer everything you want in an FPGA. Like high I/O and flip-flop counts. And 100% automatic place and route gets you to market fast.

Once your FPGA is designed, our Action Logic™ System (ALS) converts the captured design into a completed device in minutes. To give you true, high-density, desktop-configurable, channeled gate arrays.

Other FPGA manufacturers fall short on design verification. Our exclusive ActionProbe™ diagnostic tools, give you 100% observability of internal logic signals. So you don't have to give up testability for convenience.

It's never been easier to make your innovative designs a reality. We offer you a complete family of powerful FPGAs, like the A1010 and A1020, available in 44, 68 and 84 pin PLCC versions and implementing up to 273 flip-flops or up to 546

GAs The Same Way
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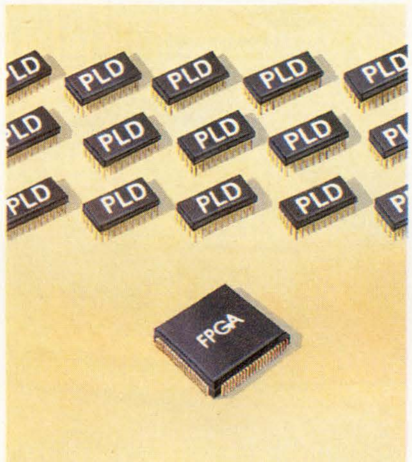
Designing with Actel FPGAs gives you more freedom than you ever imagined. More gates. More flip-flops. More I/O. In fact, our new A1280 is the largest FPGA in the world.



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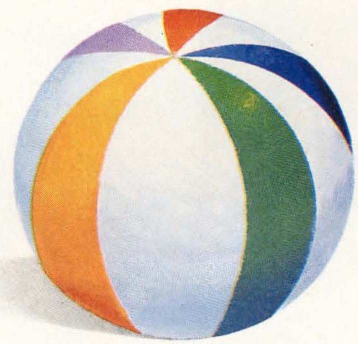
Actel FPGAs give you far more gates per square inch. As much as ten times as many as the densest PLDs. That can save a lot of real estate.



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Designing Actel FPGAs is so simple that you'll have more time to do the things that made you want to become an engineer in the first place. Or just relaxing. You've earned it.

latches. And the first member of our ACT 2 family, the powerful A1280. With 8,000 gates, up to 998 flip-flops, and 140 I/O pins, it's the highest capacity FPGA today. And our A1240-1 is the fastest. In the A1240-1, 16-bit counters run at 75 MHz, 16-bit accumulators at 33 MHz. Enough capacity and speed to handle almost any application.

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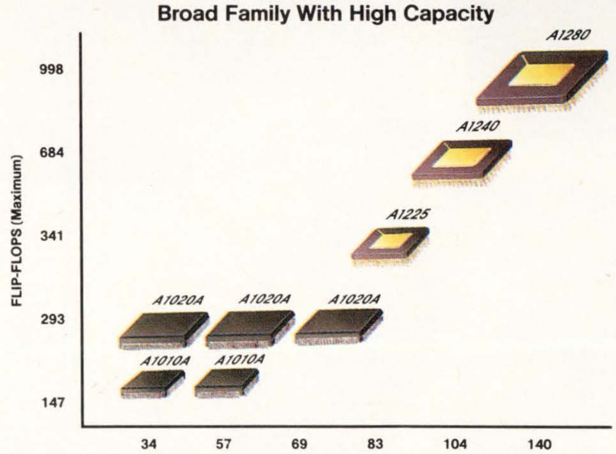
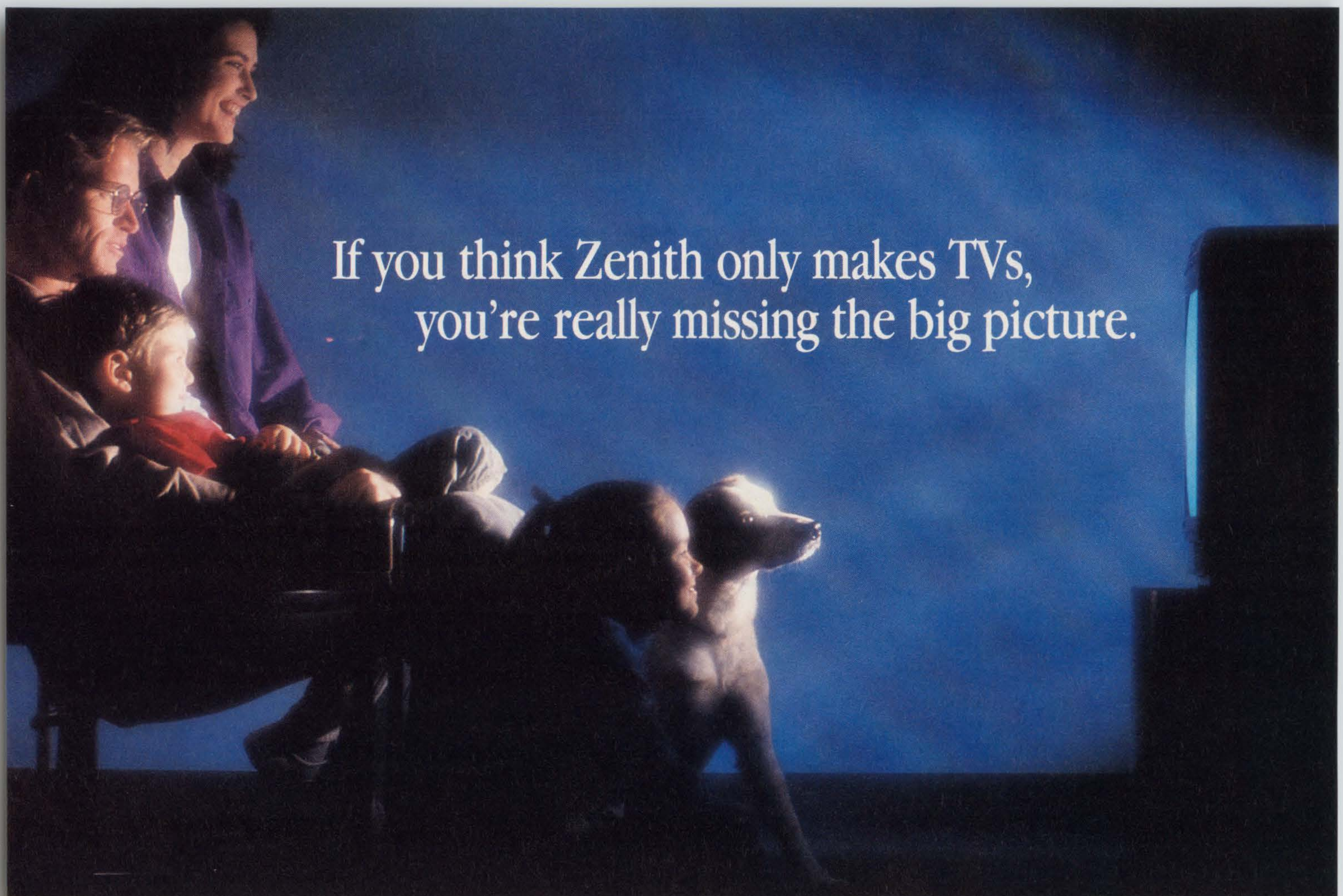


Actel

Risk-Free Logic Integration

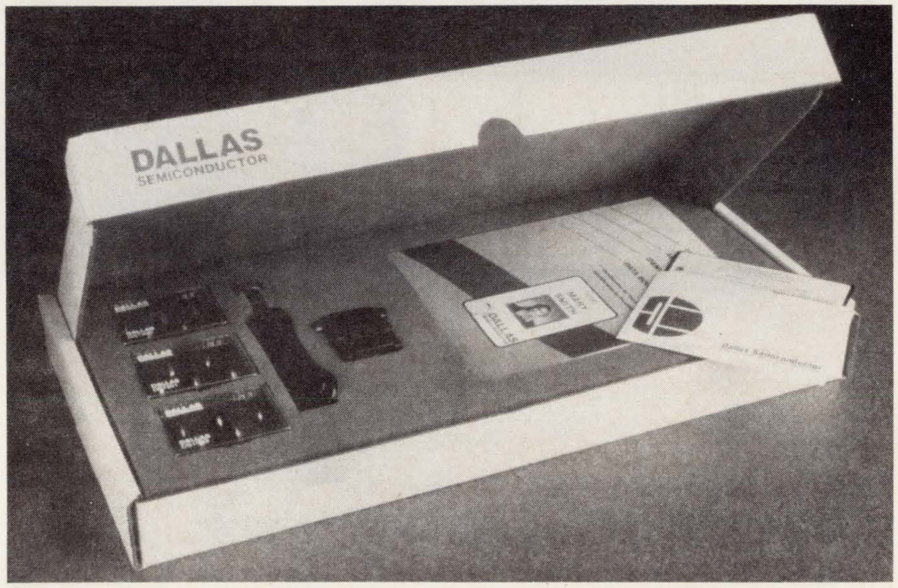
CIRCLE NO. 93


If you think Zenith only makes TVs,
you're really missing the big picture.

Sticky memory chips let you read and write bits for a wireless database

The DS199x Touch Memory family comprises battery-backed data carriers housed in coin-shaped steel containers that have adhesive backing. These data carriers provide a practical way to attach nonvolatile memory chips to objects other than pc boards. The adhesive fastens these chips on items such as equipment, badges, and corridor walls. Because you can read and alter the data contained in these ICs without hard-wiring them to a computer, you can use them to create a wireless database that isn't limited by distance, degradation, or RF interference.

The ability to update and alter their data instantly makes these chips superior to bar codes and expands upon the applications previously served by such ink-on-paper technology. For example, these ICs can hold as much as 100 times more information than a bar code and can transfer that data at an error-free rate of 16.6k bps. And, unlike bar codes, these silicon-based data carriers can communicate directly with other chips in your information system, without the power consumption and expense of supplemental optical equipment.



***Have fun discovering applications for these sticky nonvolatile RAMs** by ordering a $75 DS9092K Touch Starter Kit. This kit includes both DS1990 and DS1991 touch-memory ICs, a DS9092 Touch Probe for reading and writing the ICs, a DS9097 serial-port adapter, and demonstration software.*

The memory IC is enclosed in a 16-mm-diameter, stainless-steel can, which has a sealed lid that serves as the electrical-contact point for a probe. The probe leads to a spare I/O pin in your system's µP or microcontroller. Communications between the CPU and the memory occur directly through the lid of the chip's coin-shaped enclosure.

The chip's steel housing also provides protection from corrosive or rugged environments. Applications include tracking manufacturing processes, storing calibration settings, recording quality-control data, controlling access to equipment or buildings, managing assets, and verifying test procedures.

To communicate, the chip's circuitry multiplexes address, data, and control lines onto a single bond pad that extends to the lid of the can. The rim and bottom of the can provide a ground pad for the chip. Therefore, data transfers occur exactly as they would through a normal copper wire, without any need for magnetic or optical conversions.

When contacted by a probe, the memory IC emits a wake-up signal that will arouse the probe out of a standby, low-power state. The chip then sends signals indicating its family code, a unique serial number, and a Cyclic Redundancy Check (CRC) code. The CRC code validates the serial number and qualifies the electrical connection.

The chip calculates such a CRC code for each page of data it receives. The chip then appends the calculated CRC to the incoming data packet, thereby providing a way of validating that data when the probe subsequently reads it.

A second data-verification technique prevents the memory contents from being corrupted in a case when, during a write cycle, an incomplete connection occurs between a probe and the chip. The

EDN EDITORS' CHOICE

chip first writes incoming data into a temporary scratchpad memory for verification. Once verified, the chip copies the data into its main memory, even if the probe has lost contact with the chip.

This chip family is also useful in applications where security is a factor. Because you must enter a 64-bit password before they will begin to transfer data, these chips deny access to their contents to any unauthorized person.

You can select from an assortment of memory chips, including the $1.58 (1000) DS1990-R3 48-bit serial-number ROM chip; the $3.38 (1000) DS1993S-F5 4k-bit read/write IC; and the $3.71 (1000) 1152-bit, password-protected chip. You can also purchase a panel-mountable probe for $5 or a handheld version for $7. For $75, you can buy a DS9092K starter kit that includes a variety of adhesive ICs, a probe, a serial-port adapter, and demonstration software.—***JD Mosley***

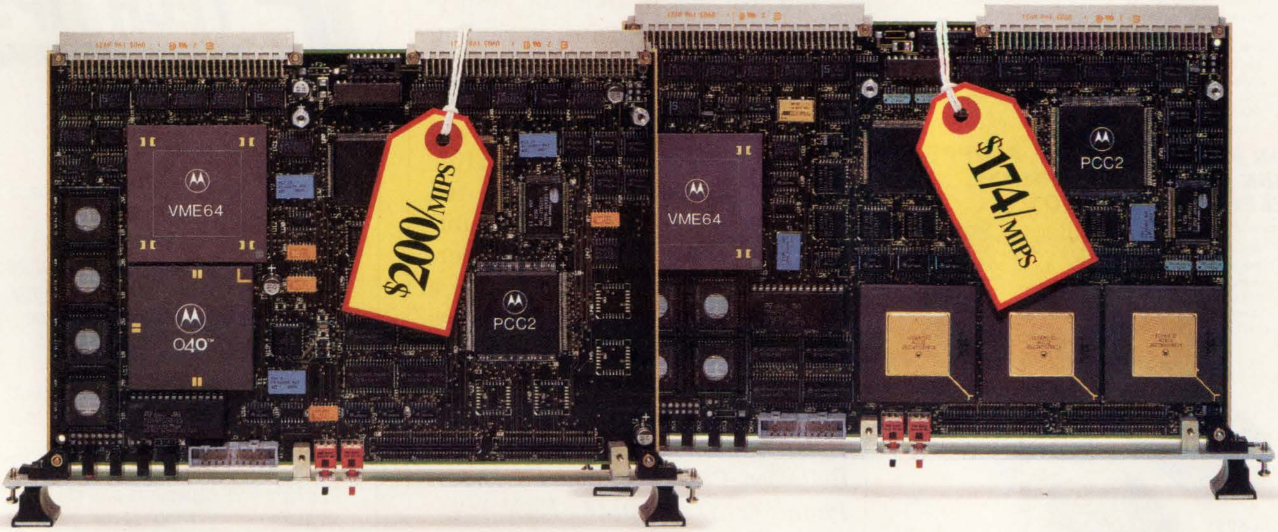
Dallas Semiconductor, 4401 S Beltwood Pkwy, Dallas, TX 75244. Phone (214) 450-0448. FAX (214) 450-0470.

Circle No. 733

ASK EDN

Got a design problem that's driving you nuts? That's what Ask EDN is for. If one of us can't figure it out, we'll find someone who can. Write to us at Ask EDN, 275 Washington St, Newton, MA 02158 or send a fax to (617) 558-4470. Or put something on MCI at EDNBOS.

The competition will call us ruthless. You can call us at 1-800-234-4VME.



It's enough to make other VME board builders call us names. Or call it quits. A new 23 MIPS VME single board computer based on the 88100 RISC microprocessor. Or a new 20 MIPS VME board based on the 68040 CISC microprocessor.

Both are built by Motorola and offered at $3,995 each. That's just $174/MIPS for the RISC board, which compares nicely with the $1,000/MIPS you've been asked to pay for somebody else's board. And it's just $200/MIPS for the CISC board.

The MVME187 (RISC) and MVME167 (CISC) boards employ VME D64 architecture. And both come with four 32-bit timers.

Malcolm Baldrige National Quality Award

For a free color brochure, call the 800 number above. And see why the competition undoubtedly wishes we'd call the whole thing off.

MOTOROLA
Computer Group

Handheld, battery-powered units combine 50-MHz bandwidth DSO with DMM

With displays that occupy about one-third of their area, *the 90-series Scopemeters look a bit unconventional. The combination of a 50-MHz, 2-channel DSO, a full-function DMM, and a function generator in a handheld, battery-powered instrument is even more unconventional.*

Some engineers and technicians, including those in research and development, will probably find that the diminutive model 93, 95, and 97 Scopemeters provide all the measurement functions they need. The units act as 2-channel digital-storage oscilloscopes (DSOs)—having a 50-MHz repetitive-signal bandwidth—as well as 4-digit multimeters (DMMs). The model 97 also includes a sine-/square-wave generator.

Each battery-powered unit weighs 4 lbs (with batteries installed) and measures 2.4×5.1×10.2 in. One of the scope's useful features is a 3000-count DMM that resolves more than 4000 counts without overloading and shares its input leads with the scope's channel A.

Scopes that make cursor-controlled measurements (something that the models 95 and 97 also do) might seem to perform a function similar to a DMM's, but most cursor-controlled measurement functions differ in capability from these units' numeric displays. For example, few scopes with cursor-controlled measurements can indicate an ac waveform's rms value. The numeric displays for these units can. Moreover, these scopes include a calibrator to ensure $3\frac{2}{3}$-digit accuracy of their cursor measurements.

The units' user interface appears intuitive and straightforward. (An inscrutable user interface was the Achilles' heel of a small LCD scope introduced about four years ago by another firm.)

The instruments employ soft keys along the bottom of their screens. Legends appear on the screen just above the keys. When a key selects a function that necessitates further choices, a pop-up menu appears. You negotiate this menu with a pair of arrow keys and make your choice with an enter key. In this way, you are never buried in nested menus, unsure of how to get out of your predicament. Because the 240×240-pixel screen has limited ability to display tiny pictures, the menus use words, not icons. Although the units don't include a conventional range selector or a numeric keypad, the menu scheme and the autoranging function work well.

Other enhancements abound to help users. For example, users often need to position the instrument six feet or more from their eyes. In such circumstances, seeing the display can present problems. For such situations, you can widen the trace to three pixels. Service personnel often need to affix a scope or meter to a door or partition so that they have both hands free for positioning the probes. These units have articulated tilt stands that hook over the top of doors and partitions. In such precarious locations, damage is a real possibility. To prevent damage, a 4-mm-thick transparent polycarbonate shield protects the display.

Most DSOs of even moderate bandwidth are ac powered and fan cooled. These units use so little power that they can be convection cooled, and they can be sealed against moisture. Though they aren't waterproof, you can actually drop one into a bucket of water


Killer Specs.
Panther® SCSI
Stalking system performance is your goal. That's why Maxtor's 1.2GB SCSI Panther was designed to perform a data seek in just 13ms. No other drive in its class features such lightning speed.
Panther's hunting prowess of 2ms track-to-track seek time stands out compared to Seagate's Wren 7 seek time of 2.5ms. And Panther outruns the competition with a 30Mb/sec. internal transfer rate.
Experience counts. Panther uses the reliable head disk assembly used in the Maxtor XT-8000, which boasts more than 300,000 units in the field. Panther shreds the competition with the widest range of available controllers, an MTBF of 150,000 hours, Novell certification and a highly competitive price.
Call about the full line of Panther drives that range from 1.2GB to more than 1.7GB capacity. If you're stalking performance, check out Panther's killer specs.
Call your nearest Authorized Maxtor Distributor.

1GB-plus Disk Drive Comparison Criteria	Maxtor Panther P0-12S	Seagate Wren 7
Capacity (unformatted)	1.2GB	1.2GB
Seek Time	13ms	15ms
Track-to-Track	2ms	2.5ms
Internal Transfer	17.4 to 29.7Mb/s	15-23Mb/s
Maximum Seek	26ms	34ms

We Drive Harder.
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Novell Labs Tested & Approved
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CIRCLE NO. 99

without causing it permanent damage—provided you retrieve it quickly. Moreover, the units' low power consumption allows them to run for four hours before the NiCd battery requires recharging. If you don't have access to ac for battery charging, you can replace the NiCd battery with four C-size alkaline cells.

Inputs that are isolated from the chassis are commonplace in high-quality digital meters, but you won't find such inputs on most scopes. As a result, measuring high-voltage waveforms (for example, the drop across a current-sensing shunt in series with the high-side line connection of an integral-horsepower motor) could subject operators to a lethal shock. In such applications, the units' DMM heritage saves the day—and possibly your life. The inputs withstand 600V rms with respect to the chassis.

For example, using the model 97's RS-232C port to send a waveform to a recorder doesn't defeat the isolation; the port is optically isolated. The serial-interface cable includes an optical-to-electrical converter powered from the receiving device's RS-232C port.

The measuring capabilities embody the most novel technology in the units. An 8-bit ADC digitizes the signals for both the waveform and numeric displays at a rate of 25M samples/sec. The numeric display uses DSP techniques implemented in a proprietary IC (one of two in each instrument) to convert the ADC's 8-bit output to a resolution equivalent to approximately 13 bits. DSP techniques also extract the rms values of ac waveforms. In addition, on the models 95 and 97, you can obtain readouts in decibels and watts. All models indicate continuity, resistance, and frequency.

The data that produce the numeric readouts also produce the waveform display. At high sweep speeds, the units use random-repetitive sampling, which lets you take advantage of the 50-MHz analog bandwidth and allows you to view pre- and post-trigger events. All models have a display memory that stores a record whose width is more than twice that of the screen. In models 95 and 97, a zoom mode lets you easily fill the screen with displays of selected phenomena that normally occupy a small fraction of the screen width. The fast sampling lets the units capture single-shot transients whose bandwidth is more than 1 MHz. Moreover, at all sweep speeds, models 95 and 97 alert you to glitches as short as 40 nsec.

Model 93 sells for $1195. Model 95, which adds 1-mV scope sensitivity, glitch capture, cursor measurements, waveform averaging, and storage for eight waveforms, lists for $1495. The top-of-the-line 97 sells for $1795. Besides offering all of the 95's features, it performs waveform math and can store and recall 10 front-panel setups. It also provides a sine-/square-wave generator, a serial port, and electroluminescent backlighting for the display.

All units come with a long list of accessories, including a carrying case, batteries, a battery charger, test leads, high-voltage probes, and a protective yellow-rubber holster.—***Dan Strassberg***

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (206) 347-6100. FAX (206) 356-5116. TLX 185102.

Circle No. 731

Philips Test and Measurement. Building TQIII-4, 5600 MD Eindhoven, The Netherlands. Phone local office.

Circle No. 732

Automated mixed-signal-design tools tackle test travails

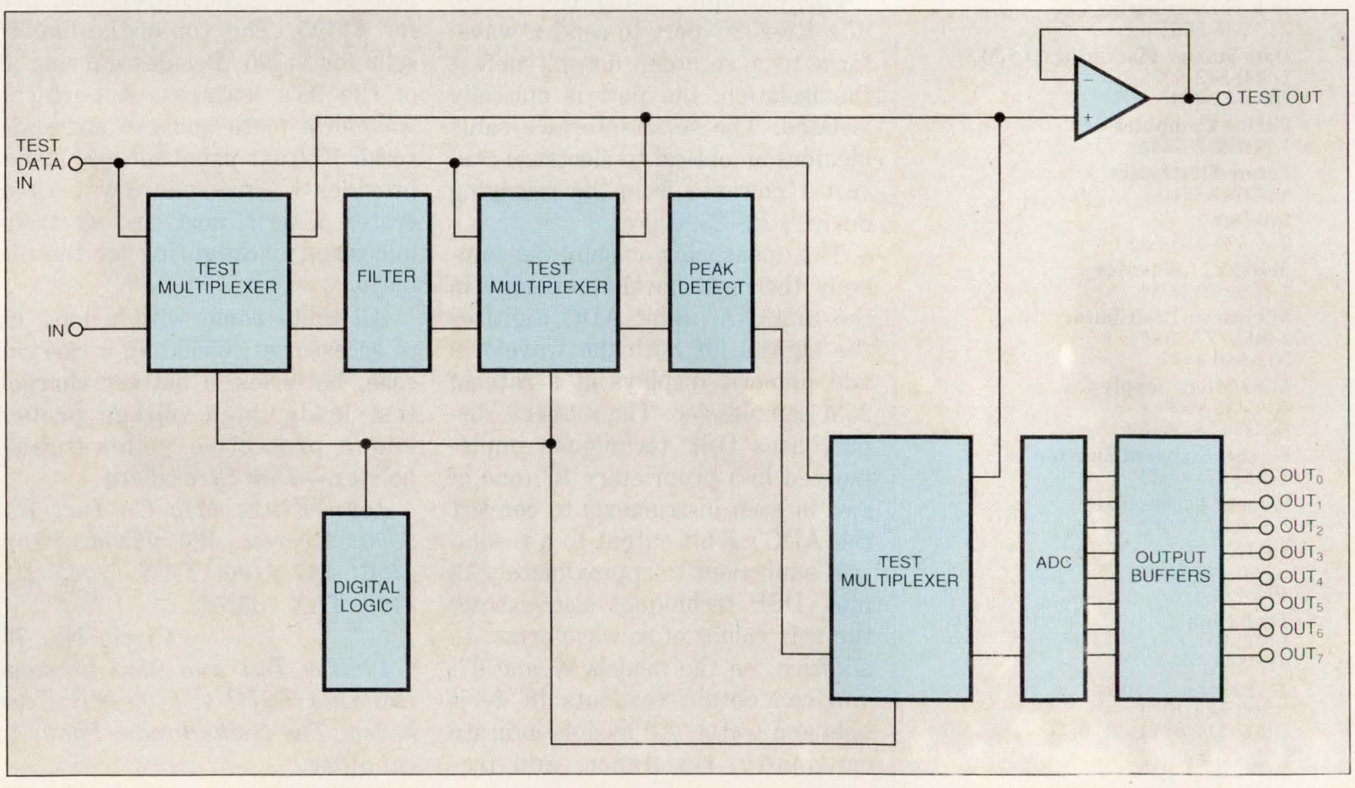
MSDS is a suite of software tools that automates and simplifies mixed-signal ASIC designs. More often than not, mixed-signal design uses quasicustom methods that require tweaking performance of existing cells and handcrafting models and test programs. Test development, in particular, is an especially tricky problem.

Analog-circuit testability is addressed via multiplexer cells coupled to each of the analog building blocks. These multiplexer cells allow something akin to analog scan. Each of these blocks, modeled and characterized for accurate simulation, is automatically inserted into your design—you can remove any of them by request. The software that provides this capability, MSTest, is available on site at the vendor's facility.

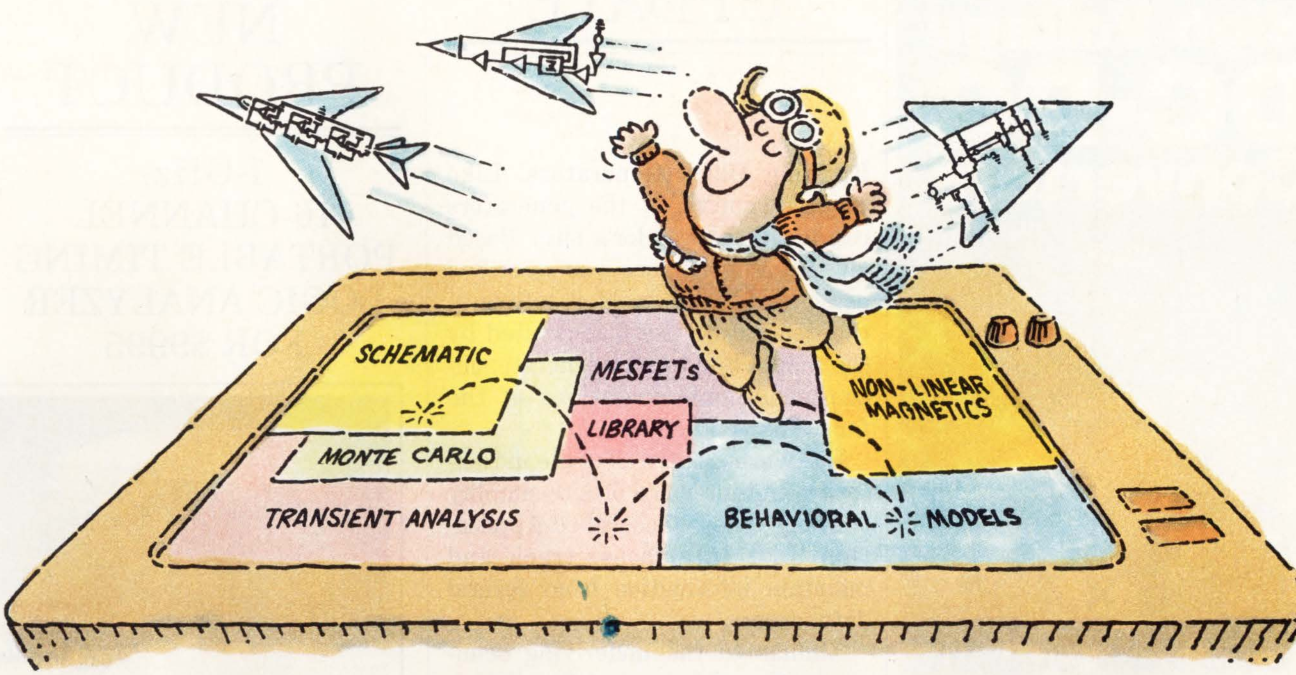
The software you'll actually receive includes several components. The Analog Model Builder uses a data-sheet paradigm. You enter your performance requirements alongside data sheet columns that define absolute limits; if your specifications impose restrictions on other parameters, these restrictions are immediately reflected in the data sheet. The model builder is essentially a compiler that adjusts model parameters for 17 analog functions—such as filters, DACs, ADCs, comparators, references, and regulators—based on your specifications. For existing cells, the software creates a behavioral model that you can simulate and a schematic symbol for design capture. Specifications for custom cells generate files, which the vendor then uses to create the behavioral model, symbol, and implementation.

The Design Critiquer compares your design against a set of rules constructed to highlight potential design flaws, such as design errors or implementation problems. Among the problems the software can flag are power-supply busing problems, schematic construction errors, and insufficient drive and improper sense levels.

Another component of the tool suite is the Parameterized Analog



By inserting test multiplexers, which in this case act as analog switches, *the mixed-signal design solution (MSDS) ensures that functional blocks are controllable and observable, thereby allowing MSTest to generate a thorough test program.*



THE NEW MICRO-CAP III.™ SO YOU CAN TEST-FLY EVEN MORE MODELS.

It wasn't easy. But we did it. Made the long-time best-selling IBM® PC-based interactive CAE tool even better.

Take modeling power. We've significantly expanded math expression capabilities to permit comprehensive analog behavioral modeling. And, beyond Gummel Poon BJT and Level 3 MOS, you're now ready for nonlinear magnetics modeling. Even MESFET modeling.

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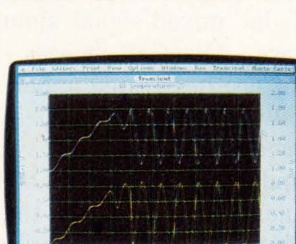
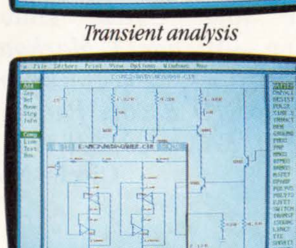
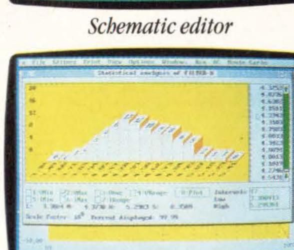


Transient analysis



Schematic editor



Monte Carlo analysis

And don't forget MICRO-CAP III's extended routine list—from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

Cost? Still only $1495. Evaluation versions still only $150. Brochure and demo disk still free for the asking. Call or write for yours today. And see how easily you can get ideas up and flying.

spectrum

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UPDATE

Building Block Generators. Like the test software, the generators reside at the vendor's site. Based on the performance you specified using the model-builder software, the generators use files created by the model builders to generate silicon-level implementations of the functions you need.

Software creates all of the initialization and interface files to simplify training. These files, called Application Tool Interfaces, track and maintain information from several databases.

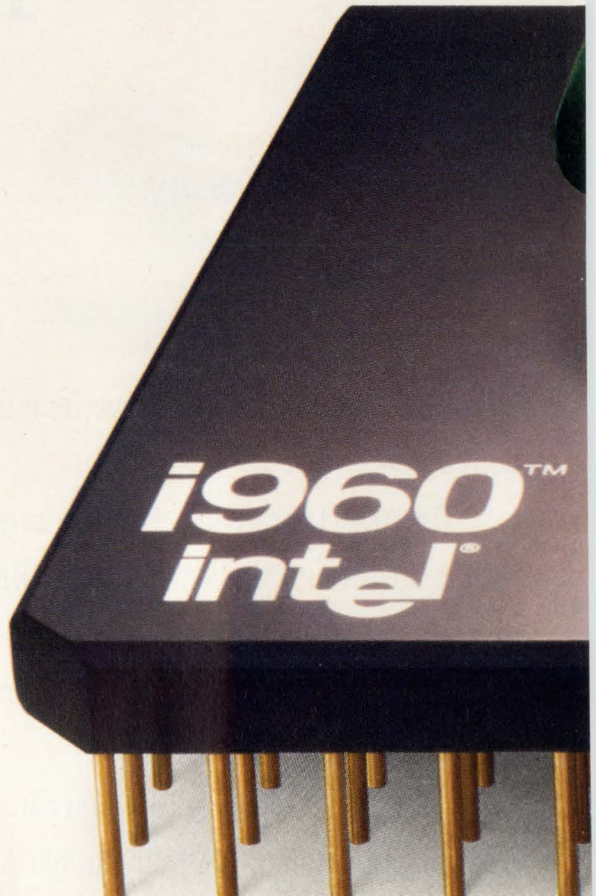
Similar to the underlying semiconductor process—a 1.5μ digital, 3.5μ analog double metal, double polysilicon process—the software handles mixed-signal design over a 12V operating range (−6 to +6V or 0 to 12V).

Beyond the company's proprietary software, the MSDS suite includes Mentor Graphics' NETed schematic-capture software and Saber/Cadat mixed-signal simulation software. All of the pieces of the tool kit are integrated under an X-Window-compliant graphical user interface. The software is available now and is priced from $75,000. The cost includes training for the company's own software as well as for Saber and Cadat simulator training.—***Michael C Markowitz***

Gould AMI, 2300 Buckskin Rd, Pocatello, ID 83201. Phone (208) 233-4690. FAX (208) 234-6795.

Circle No. 730

Move into the right 32-bit architecture and you'll be comfortable there for a long, long time.



Since nobody really relishes the thought of moving, you want to find an architecture you can stay with. And with the most complete line of 32-bit embedded processors, the Intel i960™ family is the perfect place to call home.

It's not only the most complete line, it's also the most complete solution. For starters, you get compatibility across the entire i960 line. So whatever direction you want to move within the family, the move is easy.

And with a price/performance path from under $20 all the way up to 100 MIPS, you'll have plenty of room to grow.

Obviously, a complete solution would be incomplete without a comprehensive set of development tools and support. Which is why we put together the Solutions960 Collection. Over 100 hardware and software products from debuggers to printer controller boards to help

High-frequency semicustom ICs

The plain-vanilla semicustom array is no longer adequate for many of today's applications. Manufacturers of semicustom circuits are turning to advanced processing technologies and improved architectures to provide faster speeds, wider bandwidths, and greater functionality.

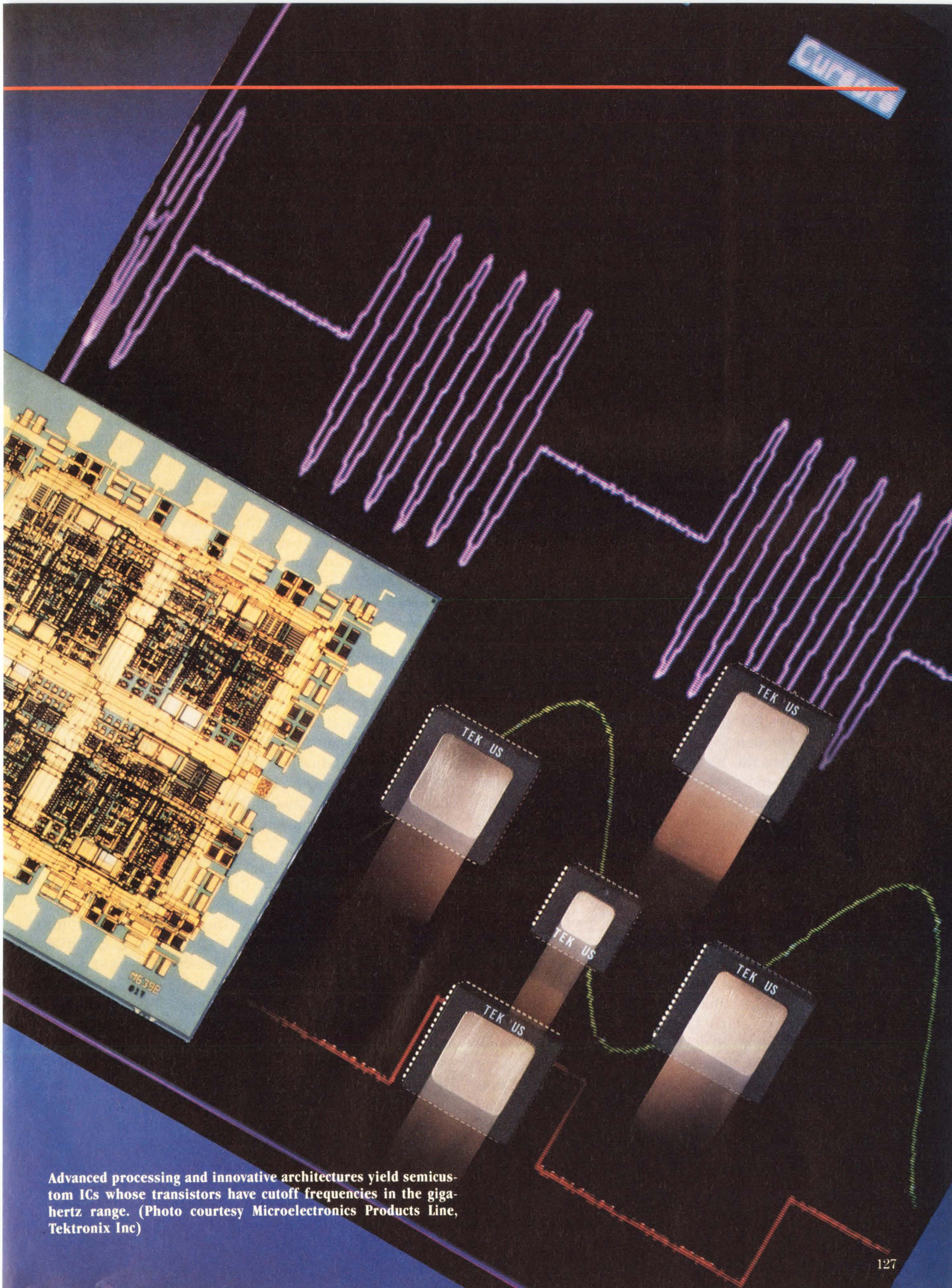
Dave Pryce, Associate Editor

Component-level bipolar arrays of limited performance will serve many ordinary needs indefinitely, but the trend in today's semicustom ICs is to higher performance and easier implementation of the final circuit. To achieve these goals, many suppliers have developed processing technologies that yield faster operating speeds, wider analog bandwidths, and greater circuit density. To ease design and layout, most of these higher-performance chips have a tile structure and a library of macrocells that replicate functional building blocks.

First- and second-generation linear bipolar arrays contained various quantities of low-performance npn transistors having gain-bandwidth products (f_Ts) of about 300 MHz and even-lower-performance lateral pnp transistors having f_Ts as low as 5 MHz. An f_T of 300 MHz may not seem that low, but if you have to use such transistors to design an amplifier with a 20-dB gain and a 50-MHz bandwidth, you probably won't succeed. The gain-bandwidth plot of **Fig 1** shows why.

Measured on the 6-dB/octave slope of a transistor's current-gain vs frequency curve, the gain-bandwidth product of a transistor is a constant. That is, as the bandwidth increases from a low-frequency value (f_0) to the cutoff frequency (f_T), the gain drops at the rate of 6 dB/octave, or 20 dB/decade. As **Fig 1** illustrates, for a transistor that has a low-frequency gain of 100 (40 dB) and a cutoff frequency of 300 MHz, the bandwidth for 20 dB of gain is only 30 MHz. If, as suggested earlier, you really needed a 50-MHz bandwidth, then you'd have to settle for a gain of approximately 15.5 dB.

Such gain-bandwidth plots clearly illustrate why transistors having f_Ts in the gigahertz range are so important to obtaining high-frequency performance in amplifier circuits. If, in the previous example, the transistor had a cutoff frequency of 3 GHz, it would have a gain of about 35.5 dB at a bandwidth of 50 MHz. Conversely, for a gain of 20 dB, the bandwidth would be about 300 MHz. Although plots of a transistor's current gain vs frequency don't tell the complete story of a circuit's high-frequency performance, they are indicative of the circuit's intrinsic capability.



Advanced processing and innovative architectures yield semicustom ICs whose transistors have cutoff frequencies in the gigahertz range. (Photo courtesy Microelectronics Products Line, Tektronix Inc)

The gain-bandwidth product, f_T, of the individual transistors is instrumental in determining the high-frequency performance of a semicustom circuit.

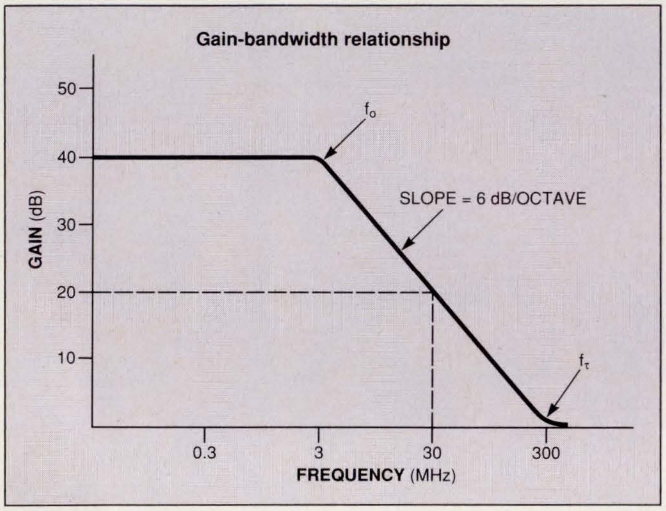


Fig 1—This gain-bandwidth plot shows why the f_T of a transistor is critical. As the bandwidth increases from the low-frequency value (f_o) to the cutoff frequency (f_T), the gain drops at the rate of 6 dB/octave. For a transistor that has an f_T of 300 MHz, the bandwidth for 20 dB of gain is only 30 MHz. If the transistor had an f_T of 3 GHz, the bandwidth for 20 dB of gain would be 300 MHz.

Creating transistors that have cutoff frequencies in the gigahertz range requires special processing. At its elemental level, such processing is sometimes only a carefully controlled shallow-base diffusion, which enhances high-frequency performance. Cherry Semiconductor Corp uses this technique to fabricate its Genesis 3300 and 5200 semicustom arrays. These arrays feature 1-GHz npn transistors, which can extend circuit performance considerably beyond that obtainable with ordinary 300-MHz transistors. Unfortunately, the pnp transistors in these arrays are 5-MHz devices, which negates the possibility of constructing high-frequency complementary circuits.

Despite the lack of high-frequency pnp transistors to complement the npn devices, the 3300 and 5200 arrays are quite versatile. Both have a tile-based layout that incorporates four transistor geometries together with diffused and ion-implanted resistors. The smaller of the two chips, the 114×74-mil 3300, is sized for use in a 0.150-in. SOIC package. The 181×140-mil 5200 chip features 25 general-purpose macrocells, a voltage-reference cell, and fuse links for active trimming. All told, the 5200 has 386 transistors and 1030 resistors; however, 152 of the transistors are either lateral or substrate pnp types, which impose inherent limitations.

Lateral and substrate pnp transistors are common in many semicustom arrays—not just those from Cherry Semiconductor—and you should be aware of their limitations. First, these transistors have a limited frequency response, which thwarts the construction of complementary high-frequency circuits. In addition, the current gain of a lateral pnp transistor generally falls off rapidly above 50 μA, which limits its use to biasing and current-mirror circuits. Although the substrate pnp transistor is a vertical device whose performance is somewhat superior to that of a lateral device, its collector is connected to ground, which is the substrate. This connection limits the substrate pnp to use as an emitter follower.

Fabricating semicustom ICs that include npn transistors having f_Ts of about 1 GHz is relatively easy, but it is quite another matter to incorporate pnp transistors with similar performance on the same chip. The job gets even tougher when the vendor wants to extend the transistors' response to 3 or 4 GHz or add digital circuitry that also operates at high speeds. Manufacturers of semicustom ICs are getting the job done by using advanced processing techniques and innovative architectures.

Vertical pnp transistors need isolation

To provide complementary npn/pnp transistors, for example, a semicustom array has to have some form of isolation for the vertical pnp transistors. Manufacturers typically use either collector-diffusion isolation or dielectric isolation for this purpose. To increase the frequency response of either npn or pnp transistors, the chip's structure must minimize both the device size and any parasitic capacitances. For digital circuitry, nonsaturating logic such as ECL has the advantage of high speed but at the expense of high operating currents. To keep current drain at reasonable levels, some manufacturers use high-speed CMOS for both analog and digital functions. In an effort to combine the best of both worlds, Exar Corp uses a BiCMOS technology that combines high-density CMOS and programmable EEPROM with high-speed complementary bipolar transistors. Another company, Tektronix, uses highly specialized bipolar processing to obtain very-high-frequency capability.

Tektronix uses a fabrication technology it calls Super High Pi (SHPi) to alleviate some of the problems designers of high-speed analog circuitry face. SHPi is a recessed-oxide isolation process that substantially reduces parasitic (collector-to-substrate) capacitance and uses smaller device profiles for high chip densities. Junction isolation typically uses 80% of the collector area of a transistor to accommodate the lateral diffusion and depletion area of the p+ isolation. Recessed-oxide

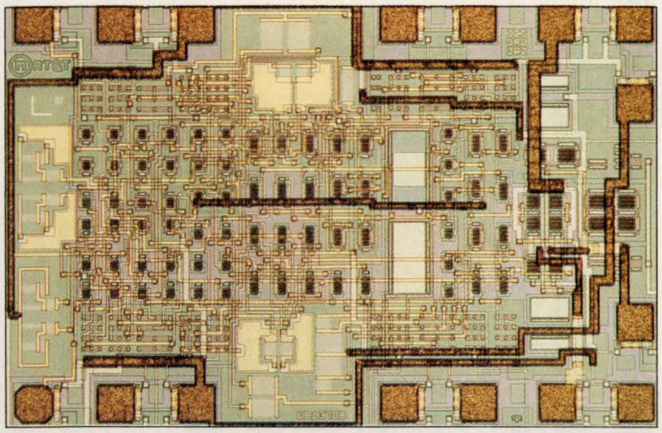


Fig 2—This high-speed comparator was implemented using the ALA210 tile array from AT&T Microelectronics. The array has complementary npn and pnp transistors that have peak cutoff frequencies of 4.5 and 3.75 GHz, respectively.

isolation replaces the p+ isolation with a smaller area nearer the active base region. This arrangement eliminates the inactive collector region and reduces the size of the device.

The Quickchip 6 family of tile arrays uses this fabrication technology and features npn transistors that have an f_T of 8.5 GHz and lateral pnp transistors that have an unusually high f_T of 80 MHz. The array's p-channel JFETs work at frequencies as high as 600 MHz. The largest of the three arrays, the QC 6-120, contains 12 tiles and provides the designer with 500 npn transistors, 300 pnp transistors, 144 JFETs, and more than 4000 implanted resistors. The chip also has 96 Schottky diodes and 96 large npn transistors on its perimeter. For versatility in external connections, the array has 54 bonding pads.

Design tools for the tile-array family include a Quicktile design guide, libraries of Spice and TekSpice device models, and the QuickIC software package. The device models have process-state data that let the models effectively simulate circuit performance over the range of process variations. The software package features tools for graphic schematic capture (netlist generation), netlist-guided layout, schematic-to-layout verification, design-rule checking, and parasitic-capacitance calculation.

Close matching is desirable

Although several companies offer semicustom arrays that have complementary npn and pnp transistors, a substantial difference often exists between the cutoff frequencies of the respective transistors, particularly at frequencies higher than 2 GHz. AT&T Microelectronics probably comes the closest to providing a true match at these high frequencies. The company's ALA-200 series UHF linear arrays are fabricated in a process AT&T calls CBIC (complementary bipolar integrated circuit) and feature transistors that have a peak f_T of 4.5 GHz for npn devices and 3.75 GHz for pnp devices. These peak values, which apply for a collector current of 3 mA, reduce to typical values of 3.5 and 2.7 GHz, respectively, at a collector current of 1 mA. These figures represent an approximate 80% match between npn and pnp transistors—unusually good performance for such high-frequency devices.

The ALA201 contains six tiles (five standard tiles and one power tile) and has 68 npn and 43 pnp transistors, 480 resistors, and 21 capacitors. The ALA202 contains 12 tiles (nine standard, two power, and one input) and has 136 npn and 86 pnp transistors, 960 resistors, and 38 capacitors. The ALA210 is a small array that has symmetrically located components optimized for the design of a single, high-performance circuit. **Fig 2** shows this IC implementing a high-speed comparator. The ALA210 has 38 npn and 36 pnp transistors, 160 resistors, and 6 capacitors. The array also has three areas set aside for optional thin-film resistors.

Typical applications for these arrays include 300-MHz op amps, buffers and video drivers that operate at frequencies as high as 700 MHz, 2-nsec comparators, pin electronics with a 2000V/μsec slew rate, VHF and UHF amplifiers, analog multiplexers, and 200M-bps optical data-link transceivers.

Dielectric isolation works well

Another company that offers complementary bipolar arrays is Harris Semiconductor. Its HTA2000 analog tile array features dielectric isolation, which eliminates substrate parasitics and allows the use of vertical pnp transistors for true complementary npn/pnp structures. The f_Ts of the npn and pnp devices are closely matched at 1.2 GHz and 1.0 GHz, respectively. The HTA2000 has 10 tiles of 60 transistors each plus areas for capacitors and NiCr resistors. A library of 24 analog cells includes op amps, buffers, comparators, S/H circuits, voltage references, and differential video circuits. A device library includes p-channel JFETs, buried zener diodes, NiCr resistors, and MOS capacitors. You can simulate the analog cells either at the circuit level or with company-developed macromodels, which can run 40 times faster than circuit-level analysis. End users can custom design their own cells using components available on the array.

BiCMOS technology has the greatest potential for combining high-performance analog and digital functions.

For design support, the HTA2000 uses Fastrack. This tool won the EDN Innovation of the Year award in 1990 and is the basis of the Cadence Analog Artist, which runs on Sun workstations. Fastrack provides a menu-driven interface for design capture, circuit and macromodel simulation, and yield prediction. The system also includes an interactive graphical simulator and analysis tools, such as Monte Carlo techniques, to evaluate performance and cost tradeoffs.

The HTA2000 tile array lets you implement designs requiring as many as 10 op-amp equivalents. For designs that require more than 10 op-amp equivalents, users have the option of switching to a cell-based implementation, which uses the tile-array functions as standard cells. The designer can add other functions created with the full-custom, transistor-level design tools and can achieve op amps that work at frequencies as high as 70 MHz.

Sipex Corp also offers complementary bipolar tile arrays. Its SP2101, SP2104, and SP2107 arrays contain 4, 12, and 20 tiles, respectively. Each tile has 16 small npn and 16 small pnp transistors with respective f_Ts of 1000 and 600 MHz. Each array also has various quantities of medium- and large-size npn and pnp transistors with f_Ts in the 500- to 800-MHz range as well as diodes and capacitors. The arrays provide space for stable thin-film NiCr or SiCr resistors, which the company laser trims to user-defined requirements. The arrays feature dielectric isolation and are available in 20 and 35V processes. Although the f_T match between the small npn and pnp transistors in these arrays is not that close, it's good enough for many complementary circuits.

A library of macrocells includes op amps, video amplifiers, S/H amplifiers, comparators, multipliers, references, and logic cells. Most of the macrocells require one or two tiles. The largest array, the 20-tile SP2107, has 780 transistors and 54 I/O pads. The company's 1991 Analog Array Data Book summarizes the features of each array and includes schematics and performance specifications for more than 25 macrocells. Each array is personalized by defining four mask layers: the thin-film resistor layer, the two aluminum layers, and the via layer for connecting the two aluminum layers.

Design services provide often-needed aid

Sipex is typical of most semicustom vendors that offer a range of design services. For the customer who wants to take full control of a design and layout, the company offers a design manual, P-Spice models, and GDSII layout templates that run on industry-standard hardware platforms. Alternatively, the company can share the design and layout tasks with the customer or provide full turnkey design services. Integration services include design consultation, layout verification, mask manufacture, and the fabrication and testing of 25 prototypes.

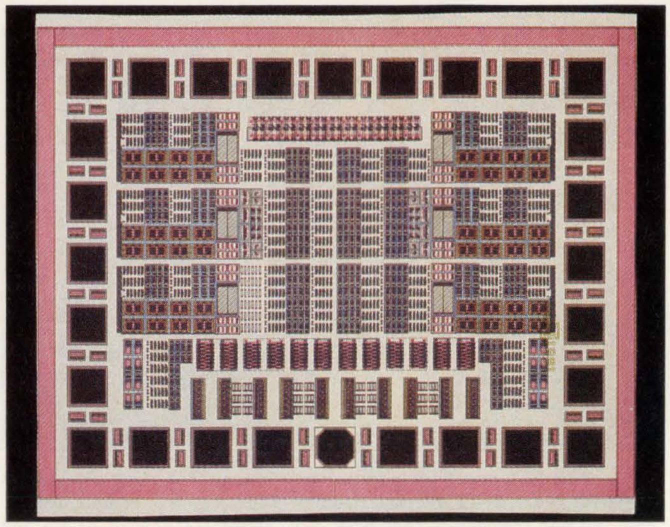


Fig 3—This BiCMOS tile array from Micro Linear combines 4-GHz bipolar analog technology with dense 1.5-μm CMOS digital technology. This FC3510 array has approximately 600 active components and more than 2.5 MΩ of resistance.

The semicustom arrays discussed thus far are primarily analog chips. Configuring the individual transistors or tiles on these arrays into logic gates or flip-flops is possible, but such arrays do not lend themselves to digital functions. If you anticipate the need for both analog and digital capabilities on the same chip, you'll want to look at other arrays such as those from Micro Linear, GEC Plessey Semiconductor, and Exar.

The FC3510 BiCMOS tile array from Micro Linear combines 4-GHz bipolar analog technology with a 1.5-μm CMOS digital technology. The array consists of different types of mini tiles. Each tile is a collection of specific components such as npn, pnp, NMOS, and PMOS transistors; poly resistors; MOS capacitors; and gates. The FC3510 contains approximately 600 active components and more than 2.5 MΩ of resistance **(Fig 3)**. Using the array, a designer can realize as many as 12 analog functional blocks and 22 CMOS gates.

The FC3510 is the type of chip that could prove suitable for handling data-receiver functions that require a moderate amount of low-power digital circuitry along with low-noise, precision analog circuits. For example, data quantizers for FDDI applications work at 280M-bps data rates. The FC3510's combination of 4-GHz bipolar devices and dense, high-speed CMOS logic seems attractive for such applications.

When GEC Plessey Semiconductor acquired Ferranti, it also acquired several series of arrays that include both analog and digital capabilities. The MFE macrochip, for example, has 48 linear cells and 80 digital gates. Each linear cell contains four small npn transistors, two "monistors" for use as either npn or lateral pnp transistors, and two resistor cells. Each resistor cell contains one 8-kΩ, eight 2-kΩ, and four 500Ω resistors. The array also has 16 medium npn transistors, 68 large npn transistors, and 16 nitride capacitors (7.5 pF max). All the npn transistors have an f_T of 3 GHz typ; that of the lateral pnp transistors is 30 MHz typ. The MFE chip won't provide complementary circuits and has a limited digital content, but its high-frequency capability is noteworthy.

For applications requiring a high digital content, you can look at Plessey's ULA-DF and -DT series of macrocell-based mixed analog/digital bipolar arrays. The DF series can run at system speeds as fast as 100 MHz. The f_T of the npn transistors in the analog cells is 1.1 GHz. You can configure the matrix cells for digital functions as five different gate types with effective delays as low as 1 nsec and as flip-flops with speeds as fast as 1.5 nsec. The DF series comprises six arrays having 32 to 82 analog cells and 224 to 1216 matrix cells. Each analog cell contains 24 transistors and 19 resistors. Each matrix cell is equivalent to two 2-input gates and consists of eight transistors and two resistors.

The DT series is similar to the DF series but can handle system speeds as fast as 200 MHz. The series comprises seven arrays having 26 to 120 analog cells and 252 to 3762 matrix cells. Each analog cell contains 43 transistors and 52 resistors. The f_T of the npn transistors in the analog cells is 6 GHz. Structurally, the matrix cells are the same as those of the DF series, but gate delays less than 0.5 nsec are possible.

As with many standard off-the-shelf devices, the trend in custom and semicustom circuits is not only to high-frequency capabilities, but to technologies that provide the best compromise for combined analog/digital circuits. The technology that appears to offer the best compromise is BiCMOS. Although the basic technology has been around for a decade or more, only in the past few years have manufacturers started to implement BiCMOS capabilities in their products—largely in response to the demand for mixed-signal circuitry.

BiCMOS versatility answers the call

Exar Corp, a long-time supplier of semicustom arrays, has developed a process it calls E^2CBiCMOS. Implemented with an extensive library of standard cells, the process allows system-level design of custom and semicustom circuits that combine analog, digital, and programmable-memory functions. The process even lets you implement a switched-capacitor filter. An 18V process yields 1.5-GHz npn transistors and 0.7-GHz isolated, vertical pnp transistors. A 5V process yields 4-GHz npn and 1.5-GHz vertical pnp transis-

Manufacturers of high-frequency semicustom ICs

For more information on semicustom ICs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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tors. These arrays suit mixed-signal applications that require complementary npn/pnp transistors for high-frequency bipolar circuitry and high-density, high-speed CMOS or EEPROM.

A partial cross-section of the array illustrates the E^2CBiCMOS process by showing the diffusion of a vertical pnp transistor and an EEPROM cell (**Fig 4**). The vertical pnp device is isolated from the other devices by an n+ sinker, n+ buried layer diffusion rings on the sidewalls, and an n− buried layer at the bottom. The EEPROM has a tunnel implant and a thin tunnel oxide, where the tunneling of electrons to the floating gate occurs. **Fig 4** does not show the npn transistor, lateral pnp transistor, NMOS and PMOS devices, or base resistors.

The N1600 1.6-μm and N2000 2.0-μm cell libraries implement the E^2CBiMOS process. These functionally identical libraries contain more than 100 cells, including analog cells, complementary bipolar cells, digital cells, memory macrocells of EEPROM, bias generators, bandgap references, and I/O-pad cells. Configurable in a nearly limitless number of ways, these cells—along with the process options—let designers select from a variety of circuit functions to satisfy their applications. These applications can range from low-voltage, low-power hearing aids to mixed-signal read/write channels for hard-disk drives to telecommunications and high-speed instrumentation.

Other companies that offer versatile cell-based, high-frequency semicustom ICs are National Semiconductor and Sierra Semiconductor. National Semiconductor has its Clasic (Customizable Linear Application Specific Integrated Circuits) library of standard cells. The company's LFast bipolar process creates npn transistors that have an f_T of 2.5 GHz; pnp devices are approximately 40 MHz. The high-density capability of this process lets designers create circuits containing more than 100 equivalent op amps as well as digital-logic circuitry. The op amps have bandwidths as high as 25 MHz, and logic cells have gate delays of 1.5 nsec and toggle frequencies as high as 140 MHz.

Sierra Semiconductor's SCDS (Sierra Custom Design System) library has nearly 700 cells and is implemented in a 1.5-μm CMOS technology. In addition to standard digital cells, the library includes ADCs, DACs, buffers, op amps, multiplexers, microcontroller cores, arithmetic functions, oscillators, PLLs, comparators, and EEPROMs. The library's digital cells operate as fast as 70 MHz and feature toggle rates as fast as 120 MHz. The PLLs operate as fast as 100 MHz, and the analog cells operate as fast as 65 MHz. Also available are 50- to 100-MHz video DACs and 10-nsec comparators. Sierra's Montage software system lets system engineers design and simulate complex mixed-mode circuits at their own desks using integrated CAE design tools and a Unix-based workstation.

The semicustom devices described here offer a variety of choices for users who need a proprietary circuit

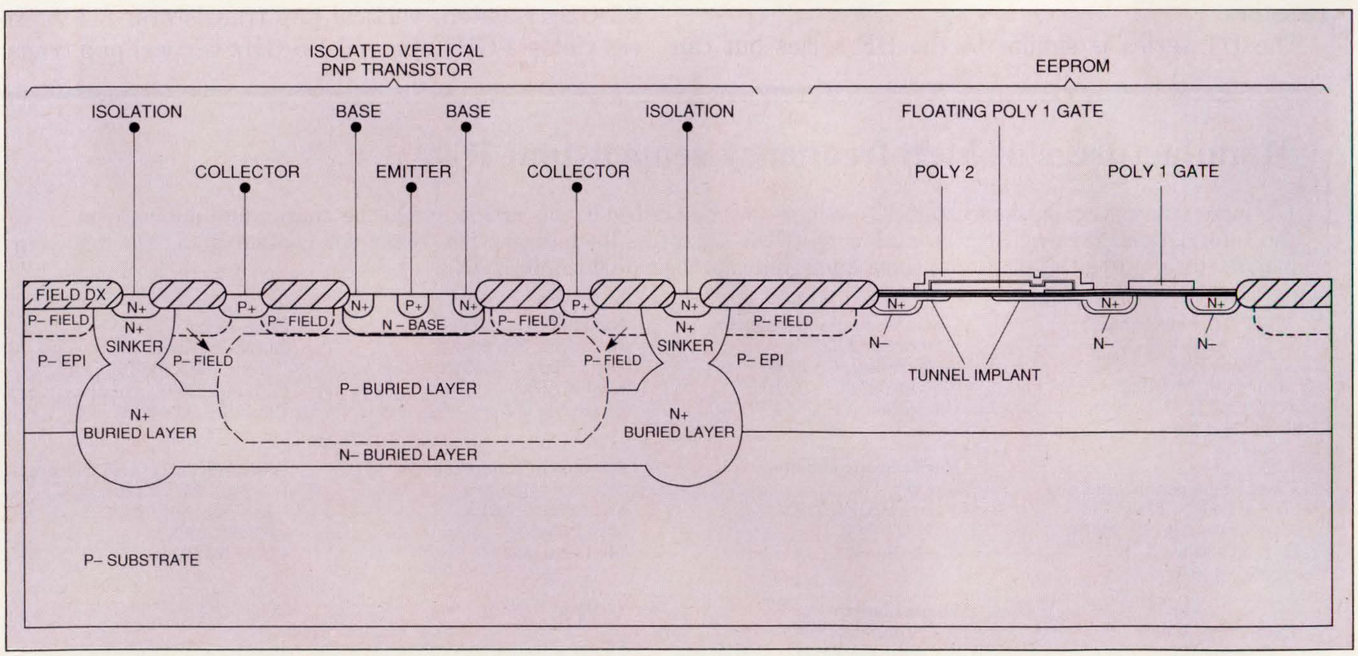

Fig 4—A partial cross-section of an array made in Exar Corp's E^2CBiCMOS process illustrates the diffusion of a vertical pnp transistor and an EEPROM cell. The pnp transistor is isolated from other devices on the chip by an n+ sinker and n+ buried-layer diffusion rings on the sidewalls.

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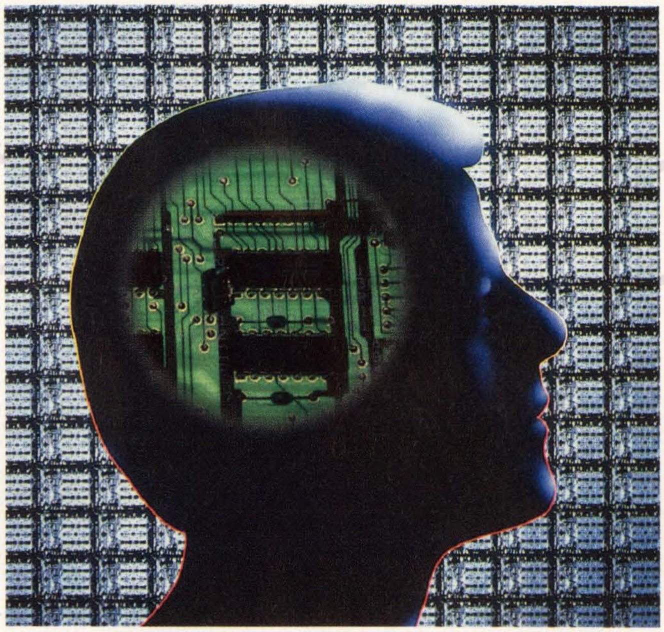

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When a system exceeds restrictions, designers are often forced to trade efficiency for acceptable EMC performance—with undesirable results. As a finished design is modified to accommodate necessary remedial shielding measures, weight and volume inevitably increase, and overall efficiency drops.

Planned EMC controls and testing during the design phase, on the other hand, not only help you maintain the integrity of the original design, but allow modifications in favor of greater system efficiency. In computer design, for example, EMC considerations such as selecting lower clock frequency, maintaining the smallest possible circuit layout areas, utilizing multi-layer boards, and minimizing the use of multiple shielding all contribute to optimum design efficiency.

The three EMC design techniques.

Achieving EMC is largely a function of three control techniques: Suppression, Isolation, and Desensitization. Through a combination of these methods, undesirable signals (EMI/RFI) are suppressed at their origin...generating circuits are isolated...and susceptible circuits are desensitized. When applied from the beginning, these techniques help you create fully integrated designs that offer both optimum performance and the best possible production economies.

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dedicated to a specific task. Granted, semicustom circuits do carry some excess baggage in the form of NRE charges, but when a standard part won't do the job, you may need to consider either a full custom or a semicustom circuit. The NRE charges for a full-custom circuit are always higher—usually much higher—than those for a semicustom circuit and thus require large-volume production runs to justify the charges.

Because of this high start-up cost, many users elect the semicustom approach, in which NRE charges can be as low as $5000 for simple bipolar or CMOS circuits of small size. In such cases, amortizing these charges is easy, even with modest quantities. But don't be misled. NRE charges for some large and complicated semicustom circuits can approach $100,000. In such cases, you may want to consider a full-custom circuit that can optimize chip size and reduce the piece-part cost.

Because of the wide range of NRE charges and unit pricing, this article does not mention typical costs for these high-frequency semicustom ICs. There is no such thing as typical. You need to know the exact chip that will satisfy your needs, and this selection often requires careful evaluation. The package type also affects price. A ceramic package is obviously more expensive than a plastic one. If your final circuit dissipates more than a few hundred milliwatts, you'll probably need an even more expensive package with substantial heat-sinking capabilities. Other factors affecting the final cost of a semicustom IC are the operating temperature range and performance or reliability screening. You'll want to explore all of these factors before making a final decision. EDN

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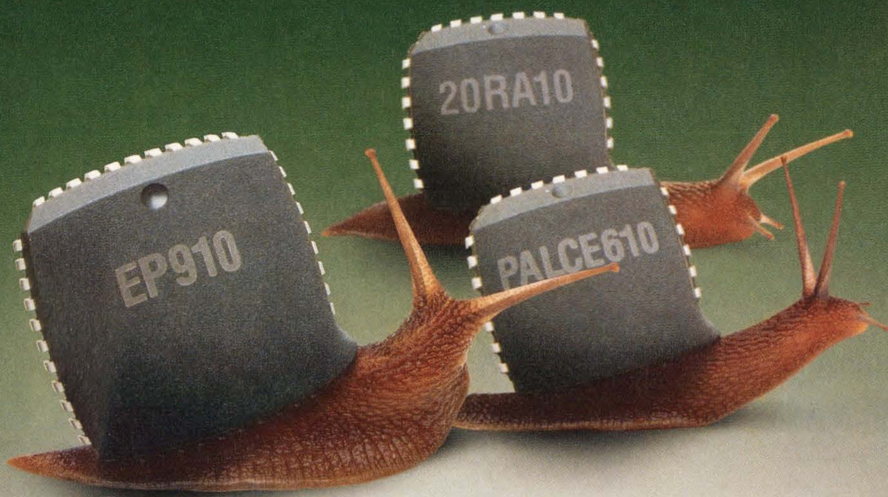
A question for designers who aren't yet using high-performance μPLDs.



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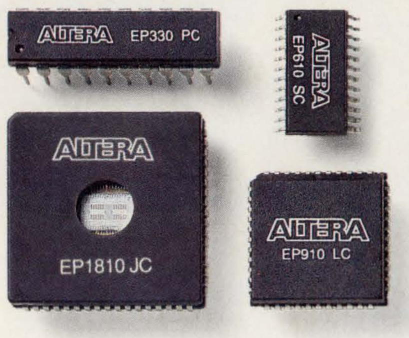

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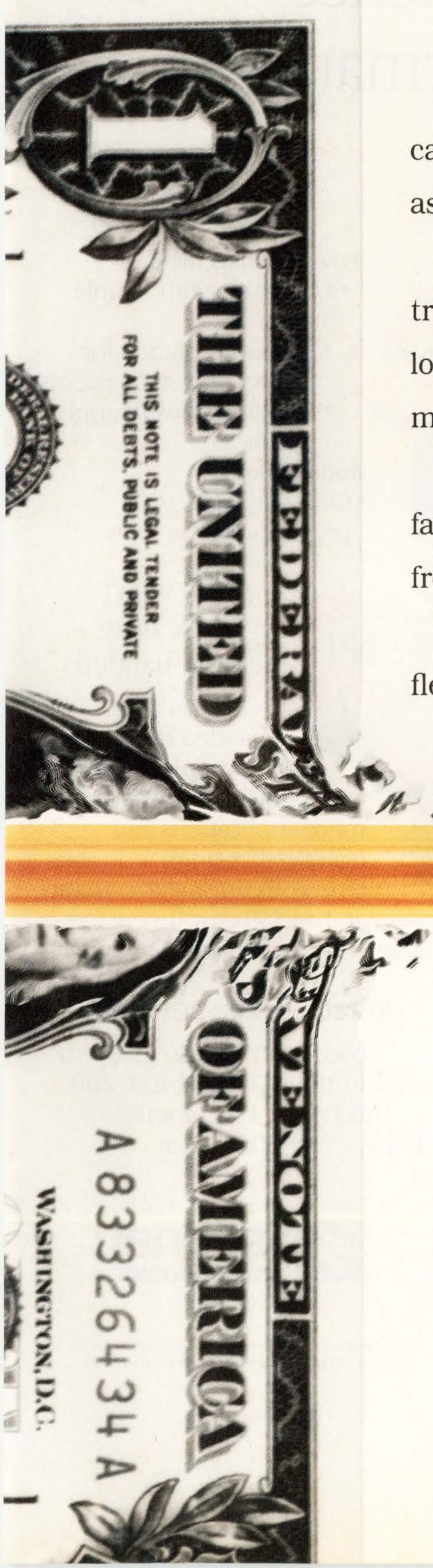

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Don't get skewed on your next ASIC design

Clock skew is a problem that hides from your analysis tools until after you place and route your ASIC. If you don't consider its effects and plan an effective strategy to combat it, skew can cripple your design.

Eric Ryherd, *Consultant, Vautomation Inc*

You can minimize clock skew in large ASICs by considering its effects early in the design. Ignoring clock skew can cause costly layout iterations and significant schedule delays. Any ASIC design with more than 200 clock loads or 10,000 gates is likely to suffer clock skew. Understanding where clock skew comes from will prepare you to avoid it during the design. Although you can minimize clock skew in many ways, you are wise to consider the pros and cons of each.

The hardest part of designing to avoid skew is skew's insidious nature. Prelayout logic simulations calculate signal delays based on statistical rules. These rules usually assume an even distribution of the cells when calculating delays. **Fig 1a** shows the simulator's view of the clock distribution in the prelayout simulations. The delay calculator computes the average delays for the clock with a given number of loads and a given die size. Because all of the delays are the same, there is no clock skew.

After completing the ASIC layout, you can back-annotate the delays caused by different wire lengths into the design. Post-layout delays for each branch of the clock differ because of the different amount of wire that each clock buffer must drive. **Fig 1b** shows a schematic representation of the actual post-layout clock distribution. Since flip-flop E is very close to the clock-driver pin, its total clock delay is very short. Flip-flop A, on the other hand, is in the far corner of the die and its delay is exceedingly large. If the D input of flip-flop A comes directly from the Q output of flip-flop E, then the design may have clock skew problems.

This example emphasizes that clock skew is usually a problem when the output of one flip-flop feeds the input of another flip-flop without any intervening logic. Before you back-annotate the layout effects into your simulation, the simulator assumes the clock to both flip-flops is identical. Therefore, flip-flop A follows flip-flop E by one clock cycle (**Fig 2a**). After back-annotating the layout parasitics, the simulation shows the clock at flip-flop E arrives earlier than at flip-flop A (**Fig 2b**). If flip-flop E's output changes quickly enough, the transition will violate flip-flop A's hold time and flip-flop A's state will become unknown. Hold-time violations

Pre-layout simulations won't reflect clock skew because the simulation assumes statistical, balanced delays.

are usually most severe in best-case-delay simulations where the clock-to-Q delay of flip-flop E is very short.

Often, flip-flops from widely separated blocks feed subsequent flip-flops in the scan chain. This technique almost guarantees significant clock skew between these nodes. You can use level-sensitive-design techniques due to their inherent insensitivity to clock skew.

In high-speed designs, clock skew can cause setup-time violations in the worst-case timing. For critical paths, you must add the worst-case clock skew to the total path delay. To properly account for skew, you must either ensure that the start and destination flip-flops are on the same clock branch or cut a few more nanoseconds out of the critical path. Whatever you do, don't forget to add the clock-skew margin to your critical paths. Most static-timing analyzers don't factor in the possible skew; you may have to add it in yourself.

A sharp rise time on the clock signal will eliminate potential simulation errors. Most digital simulators do not model slow rise or fall times accurately. Keeping the rise time short minimizes the error.

Minimizing the rise time also reduces skew caused by threshold differences on the clock pin of different types of flip-flops. Depending on how your ASIC vendor builds each flip-flop cell, the switching threshold can vary. For example, one type of flip-flop might have a switching threshold of 2V where another has a threshold of 2.8V. A 1V/nsec rise time on the clock would result in an 0.8-nsec clock skew between these two flip-flops before you consider skew induced by clock distribution.

Most ASIC vendors recommend distributing the clock using a balanced tree. This method uses a high-drive cell to drive typically eight clock loads. These eight loads could be clock drivers, each of which drive

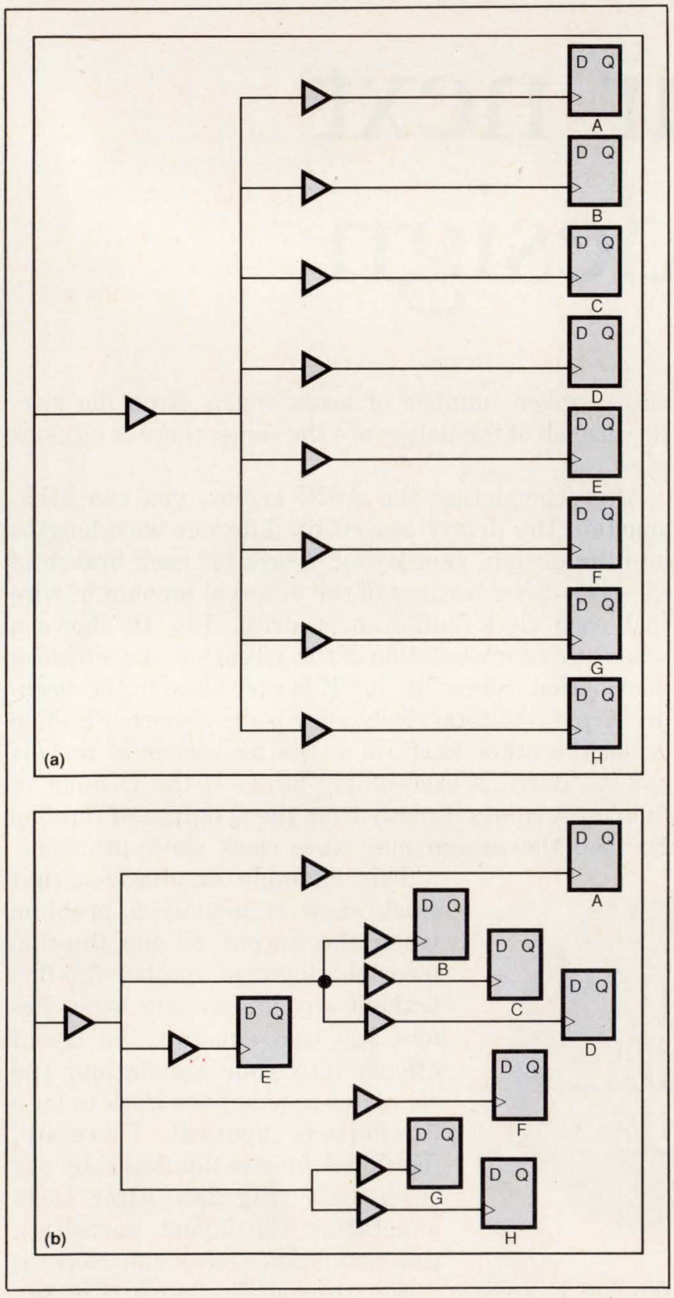


Fig 1—Prelayout simulation (a) assumes even *and balanced clock distribution, even though such symmetry is unlikely to hold after layout (**b**).*

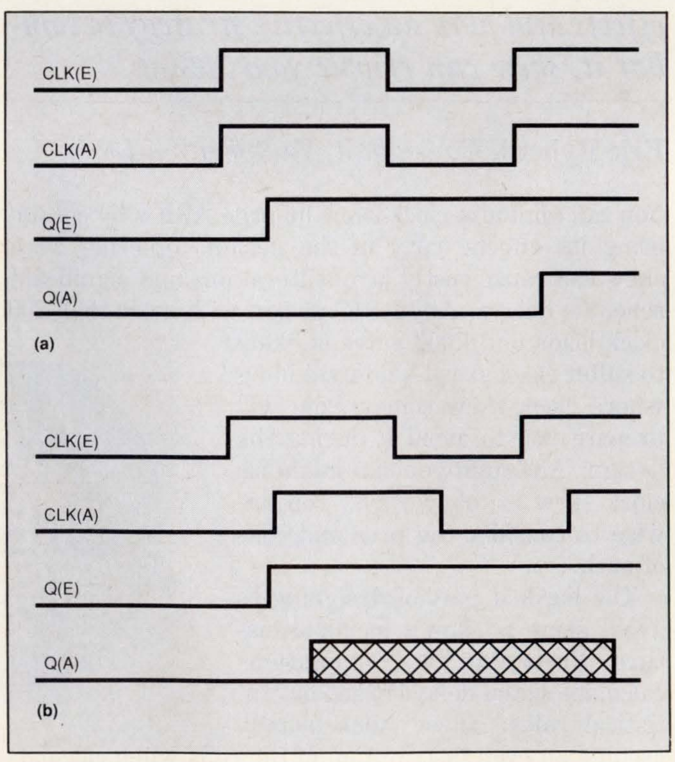


Fig 2—In an ideal world, *consecutive flip-flops driven by the same clock will serially shift data (**a**). However, skew may disrupt this ideal vision (**b**).*

Avoiding chip-to-chip clock skew

Clock-skew is a tough problem on an ASIC, but the problem gets worse for boards and systems. Fortunately, the number of clock loads is relatively small on a board. Usually, you can minimize the problems of board-layout skew with careful placement and routing of the clock line.

You must also use proper termination on most clock lines. Terminating TTL or CMOS signals is an art. Experiment with series, parallel, and even active termination using fast diodes to get the cleanest clock signals possible.

You also need to consider board delays. Think about the clock running against the grain of your logic. For example, your clock trace for a set of pipeline registers should run up the pipe, against the flow of data running down it. This technique biases the race between clock and data toward the clock by clocking more significant bits before less significant bits.

You must also compensate for the delay characteristics of the different devices. You must eliminate the skew at the input to the ASIC's internal flip-flop, in addition to its external clock pin. Where one chip on your board might be a best-case chip, another may be a worst-case chip. If the best-case chip directly feeds the worst-case chip, signals may violate hold-time requirements of the worst-case chip. CMOS ASICs typically have a large difference between best- and worse-case delay characteristics.

The switching thresholds of different devices are much worse on a board than they are on an ASIC. The CMOS input of an ASIC may not switch until 2.3V, where a TTL device may switch at 1.8V. Therefore, a clean, sharp rise time is a must on the clock signal. Using Spice or a transmission-line simulator can help you design a clean clock signal. Finally, don't forget to add the ASIC's internal skew to the total clock skew.

Obviously these sources of skew present a formidable design task. Fortunately, several simple schemes can keep your headaches to a minimum. All techniques require implementation at early stages in the design.

- Specify similar clock delays on all chips in the system. If one ASIC has a clock delay of 5 nsec and another of 8 nsec, your design immediately suffers from 3 nsec of skew. Specify the minimum possible clock delay that all chips can attain.
- Minimize the clock-delay time. You can calculate best-case and worst-case delay times by multiplying the typical delay time by a factor. A typical best-case factor is 0.5, where a typical worst-case factor is 2. If the typical delay is 6 nsec, then the skew between best- and worst-case is 9 nsec. However, if the clock delay is only 3 nsec, then the best-to-worst skew is only 4.5 nsec. Keeping the clock delay time as short as possible minimizes the difference between best-case and worst-case chips.
- Inputs should have hold times as close to zero as possible. Buffering inputs with the same delay as the clock lets you make the hold time zero. This hold time eliminates the differential between best- and worst-case since zero multiplied by anything is still zero. Unfortunately, knowing how much delay you need to add to balance the clock delay is difficult to predict before the layout is finished. You may need to manually place and route these signals.
- Minimize output delays. You can minimize these delays by driving outputs directly from flip-flops to minimize the best- to worst-case delay differences.
- If possible, use level-sensitive design. Design clock-generation circuits carefully to ensure proper pulse widths and to maintain edge-to-edge relationships. Maintaining sufficient pulse widths becomes difficult in high-speed designs. Also, level-sensitive design requires that you terminate and balance two clocks instead of just one.
- Use a phase-locked loop (PLL) to regenerate the clock. The PLL can eliminate much of the skew problem. PLL circuits can nearly eliminate the total clock delay and the difference between best and worst case.

Following these suggestions won't necessarily eliminate your clock-skew problems. At best, these techniques can only lessen skew. If you have a large design with many ASICs from several different vendors, you must be prepared to handle the inevitable clock skew and remain flexible enough to allow some last minute adjustments. If you have extra I/O, providing several extra outputs with various amounts of delay is often useful.

Logic optimization programs wreak havoc with much of the balancing logic you may add to your clock-distribution circuits.

another eight loads giving a clock fan-out of 64. These 64 drivers could be yet another set of drivers to drive 512 loads. This tree extends until all clock loads are driven. The trick in using this technique is that you must ensure that each of these branches has the same delay or is balanced. To balance the tree, you must often add artificial clock loads to some branches to balance the tree.

Another popular clock-distribution technique uses a high-drive I/O cell to drive a carefully laid-out clock network. In this case, an 8- or 12-mA driver drives a wide metal clock trunk. Exiting from this trunk are several smaller tributaries, which feed the clock loads.

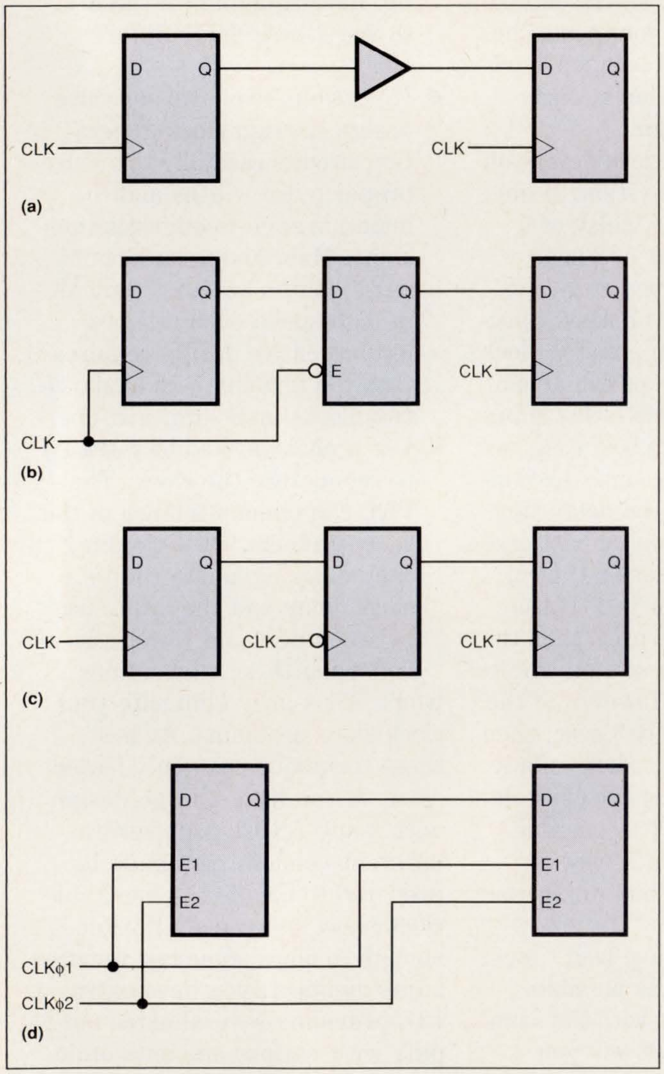


Fig 3—You can use several techniques to reduce clock skew: *You can insert delay elements (**a**), negative-level-triggered latches (**b**), negative-edge-triggered flip-flops (**c**), and 2-phased level-sensitive flip-flops (**d**).*

Although this technique often results in lower overall clock delay and skew, you generally can't control which flip-flops appear on the same clock branch because the layout software, not you, places the flip-flops. Any one branch of the clock network typically has near zero clock skew, although skew between branches may be significant.

You can significantly speed up the design of a large ASIC by using logic synthesis. Unfortunately, synthesis may place the flip-flops from functional blocks of the design on different clock branches without regard to skew. You may need to manually correct synthesized clock-distribution schemes. As a result, logic synthesis can cause you to lose some of synthesis' productivity gains in the need to correct for clock skew at the back end of the design. Optimizing logic with an automatic tool is almost guaranteed to remove any "fixes" you may have inserted to avoid clock skew. Optimizers love to remove unnecessary-logic gates—including those crucial for proper clock-skew control.

The simplest solution to clock skew uses a buffer as a delay element (**Fig 3a**). You need to add enough delay to compensate for the worst-case clock skew. Because inverters only use half a gate and one routing channel, two or four inverters are generally sufficient and inexpensive. Unfortunately, because the placement software will likely place all of the inverters in adjacent slots, the post-layout delay will likely be less than you anticipated. Thus, you may want to add a bit more than the minimum required delay. Hopefully your ASIC vendor can provide you with some accurate guidelines for predicting the actual delay of your inverter chain. Be especially careful of signals that have several destinations to ensure that you are not adding delay to a critical path. Add the inverters only to those paths that have a flip-flop output connected to a flip-flop input.

A negative-level-gated latch holds the current value of the flip-flop halfway through the next clock cycle. This method works well if you can ensure that the latch is on the same clock branch as the flip-flop (**Fig 3b**). If the flip-flop and latch are on different branches, the latch suffers the same clock-skew problems as the rest of the chip. The penalty for using this method is that the latch adds another load onto your clock, usually the last thing you want to do. Also, holding the data halfway through the next clock cycle precludes using this technique for speed-sensitive signals.

Adding a negative-edge-triggered flip-flop is similar to adding a negative-level-gated latch, without the same clock-branch restriction on the flip-flop. Note in

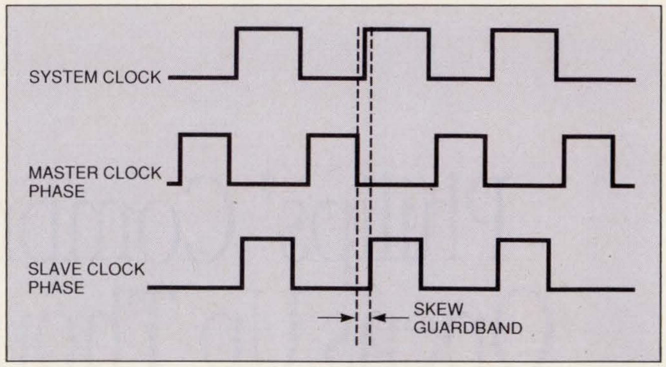


Fig 4—When you generate a dual-phase, nonoverlapping clock pulse, *the skew guardband—dead time between pulses—must be subtracted from your total cycle time.*

Fig 3c that the clock for the positive-edge- and negative-edge-triggered flip-flops are not on the same branch as in **Fig 3b.** The drawback to this technique is the number of gates the design needs. Buffering an entire 32-bit register with this method doubles the gate count for the register.

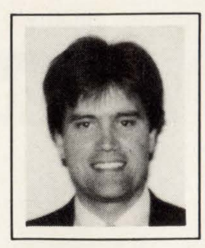
Another skew-reduction method uses level-sensitive design (LSD) techniques (**Fig 3d**). Two nonoverlapping pulses clock the master and slave portion of the flip-flop. Unfortunately, most ASIC design libraries don't contain models for level-sensitive design. In addition, most static-timing analyzers assume single-phase clock-designs and rising-edge-triggered flip-flops. If your ASIC vendor does not have the cells you need for level-sensitive design, you will have to build them from lower level cells.

Also, using nonoverlapping clocks eliminates some of your cycle time. **Fig 4** illustrates the tradeoff between lost cycle time and clock-skew guardband. LSD requires that you use accurate clock-generation circuitry. Spice simulations of the clock-generation circuits are critical in high-speed designs. Without performing Spice simulations to verify your designs, you may find the pulse width of the 2-phase clocks can narrow to near zero after process, voltage, and temperature variations are considered.

You may also have to balance two clock trees instead of just one. Generally, LSD works well for scan-test rings where the clock cycle time is relatively slow and the skew guardband can be fairly large. EDN

Author's biography

Eric Ryherd is an independent ASIC-design consultant for Vautomation Inc. He is an IEEE member who earned his BSCSE from Rensselaer Polytechnic Institute, (Troy, NY).



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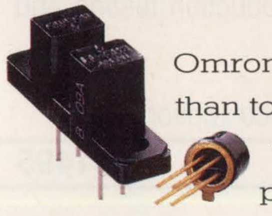

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Logic-synthesis tools take the tedium out of logic design

Logic-synthesis tools automate tedious tasks while freeing your time for the creative side of design. And ASIC designers are finding that these tools suit many applications. But you'll have to follow some guidelines to use the tools effectively.

Joseph P Paradise, *Paradise Technical Services*

Logic synthesis automates some of the tiresome, manual tasks designers have performed in the past. It also allows designers to combine different design methods in one project. Synthesis and optimization can free designers for creative tasks, can ensure an error-free realization, and can ultimately shorten design cycles.

You initiate logic synthesis by formulating a design description. You can enter your designs in formats ranging from low-level netlists to high-level behavioral descriptions. The logic synthesizer returns a compiled output in the form of a netlist optimized according to your constraints and options. It can then perform further analysis and iteration to produce a final description that you can pass to other CAE tools.

The flow chart in **Fig 1** provides a general description of how logic synthesis works. In the first step, a system's concept undergoes architectural planning and partitioning before being reduced to tangible modules. That is, you develop connectivity, data flow, and hierarchy as the design specification takes form. Eventually, you identify specific functions as candidates for synthesis.

Your choice of language description for these functions will strongly influence the final results of the synthesis. A design formulated on behavior, rather than on gate connections, will provide more latitude for the synthesis tool. Designers who favor detailed schematic diagrams and laboratory breadboards may have a difficult time or be unwilling to make the transition from detailed descriptions to behavioral descriptions. However, those who do not switch can still instruct their synthesis tool to minimize their designs' areas or delays; they just won't be able to exercise all of the other features that synthesis tools offer.

Options abound once you decide to use a high-level-language design description. Hardware description languages (HDLs) such as VHDL or Verilog are possible choices. Additional formats include Boolean expressions, truth tables, input-output waveforms, and finite-state-machine descriptions. Module characteristics and coding complexity often decide which option you will choose. However, you may find that the complete design comprises individual modules having different types of descriptions. Mixing formats is perfectly acceptable and allows the most suitable format to accompany each design block, or module, within a larger hierarchy.

Logic synthesis promises to minimize the detailed tasks that designers face in reducing concepts to working circuits.

At the synthesis and optimization stage in the flow chart, you can set constraints to guide your design's translation to the gate level. For specific applications, you can constrain the synthesizer to a library subset (for example, gate primitives having four or fewer inputs). Constraint parameters for area, delay, pin loading, and testability provide control over optimization. A logic library supplies the information the tools need to map the design specification to actual gates.

During compilation, the tools' routines perform several functions: they collapse your hierarchical design into a single-level design, translate abstract models to target-library components, monitor critical paths with an internal timing analyzer, and evaluate cost-function constraints to make optimization tradeoffs. Timing analysis and cost-function optimization are two tasks designers are glad to relinquish to logic synthesis. The final result of compilation is an output netlist tailored to your specifications.

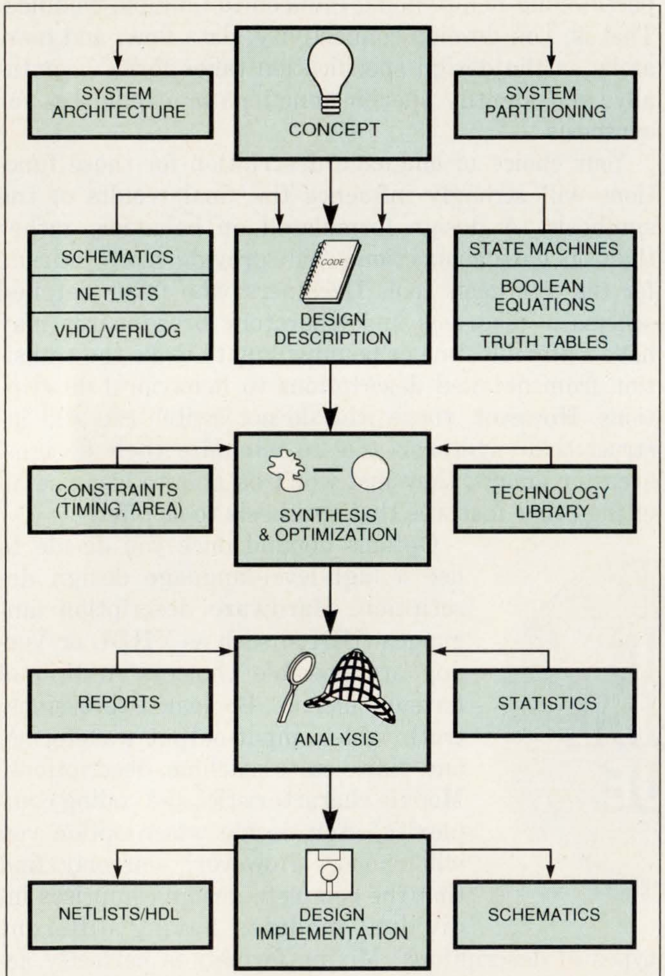

Fig 1—This flow chart diagrams the *steps you must take to design an ASIC, using logic synthesis.*

A variety of report and translation options aid the next phase: netlist analysis. For example, the synthesizer can produce schematics that provide gate-level information about the synthesized design in graphical form. It can also produce tabulated and sorted internal node lists, area/delay values, and compiler statistics that yield additional details. You can edit the synthesized schematic manually on a workstation or integrate the netlist with other design modules. You can then submit the processed netlist to a silicon foundry for implementation.

Compiling an actual design will translate the flow chart's theory into practice. This tutorial, using the PC version of ISS's Instant Logic package, explains the task of reducing a conceptual design to a final gate-level description. **Fig 1**'s flow chart again serves as a guideline for executing this step-by-step procedure.

Begin by using a schematic-capture package, such as the PC version of OrCAD from OrCAD Systems

```
Name      Priority;


/*********************************************************/
               Priority Interrupt Encoder
*/



/** Inputs and Outputs  **/

pin [2..8] = ![IREQ1..7];
pin[15,21,22] = ![IPL0..2];



/**  Declarations and Intermediate Variable Definitions  **/

LEVEL7INT =  IREQ7.dq;
LEVEL6INT = !IREQ7.dq &  IREQ6.dq;
LEVEL5INT = !IREQ7.dq & !IREQ6.dq &  IREQ5.dq;
LEVEL4INT = !IREQ7.dq & !IREQ6.dq & !IREQ5.dq &  IREQ4.dq;
LEVEL3INT = !IREQ7.dq & !IREQ6.dq & !IREQ5.dq & !IREQ4.dq &  IREQ3.dq;
LEVEL2INT = !IREQ7.dq & !IREQ6.dq & !IREQ5.dq & !IREQ4.dq & !IREQ3.dq &  IREQ2.dq;
LEVEL1INT = !IREQ7.dq & !IREQ6.dq & !IREQ5.dq & !IREQ4.dq & !IREQ3.dq & !IREQ2.dq &  IREQ1.dq;



/**  Logic Conditionals  **/

Condition (
        if LEVEL7INTout [IPL2,IPL1,IPL0];
        if LEVEL6INTout [IPL2,IPL1     ];
        if LEVEL5INTout [IPL2,     IPL0];
        if LEVEL4INTout [IPL2          ];
        if LEVEL3INTout [     IPL1,IPL0];
        if LEVEL2INTout [     IPL1     ];
        if LEVEL1INTout [          IPL0];
)
```

Fig 2—For this design example, *an engineer began with this existing PLD-design file. The logic-synthesis tool accepts such files as input and generates both documentation and a netlist for an ASIC foundry.*

Table 1—Optimization examples

Circuit number	Circuit type	Input pins	Output pins	Optimization mode	Area (equiv gates)	Critical path delay (nsec)	386-33 (CPU-sec)
CKT1	Arithmetic	5	3	Area	34	4.3	6
				Delay	43	4.2	7
CKT2	Arithmetic	7	10	Area	99	14.4	10
				Delay	123	8.7	12
CKT3	Arithmetic	5	1	Area	13	10.8	8
				Delay	16	7.3	9
CKT4	Arithmetic	8	4	Area	169	18.2	65
				Delay	213	10.3	76
CKT5	FSM Description	29	22	Area	330	10.9	46
				Delay	330	10.9	48
CKT6	Customer design	91	78	Area	2488	26.4	450
				Delay	3490	17.9	478
CKT7	Netlist translation	33	25	Area	593	51.9	26
				Delay	773	30.6	29
Tutorial	Priority encoder	11	4	Area	14	3.9	17
				Delay	19	2.4	18

(Hillsboro, OR), to build a top-down block diagram for a complete design. Imagine that one of the blocks defines a function having no gate-level equivalent in the logic-device library: a priority interrupt encoder for a CPU. Luckily, the encoder was implemented in a PLD some time back on another board-level product. Researching the company files reveals a Logical Devices (Fort Lauderdale, FL) CUPL-language description for the PLD.

Design description

The original CUPL file then becomes the complete design description for this particular module in the hierarchy. As **Fig 2** shows, the CUPL code is essentially a set of Boolean-logic equations, originally used to map the design to the PLD's AND/OR topology. The engineer updates the OrCAD schematic block for the encoder to match the corresponding pin names as coded in the CUPL file. The engineer also specifies a file name that OrCAD will eventually use to attach the detailed gate-level description as a hierarchical block. That way, the detailed description will be available, one layer down, in an OrCAD schematic.

To port the CUPL design to the synthesis tool, CUPL software can translate the proprietary CUPL format into a standard Berkeley PLA equivalent—a truth-table format. Most PLD tools can perform similar translations, and many logic-synthesis tools accept this format without editing. Using the logic-synthesis tool, the designer next specifies an ASIC vendor's library and selects area and delay parameters for optimization. The logic-synthesis software then creates application-specific files from the device library, language descriptions, and specified configuration and optimization parameters.

Engineers sometimes compile designs twice, optimizing for minimal area in one run and minimal delay in the other. They can do this when the design doesn't have strict, predetermined delay or area requirements or when the design is small and will compile quickly. **Table 1** shows the results of such dual-compilation runs for a variety of circuits, including this article's circuit, "Tutorial." Comparing the area vs delay data for the encoder module shows that the significantly reduced propagation time produced by delay optimization is the best choice for this design. Selecting the delay-optimized netlist from the two netlists produced completes the analysis phase.

Before compilation, a designer can direct the logic-synthesis tool to create an OrCAD-compatible netlist database. A netlist database, or "netlist," is the set of files a software tool needs to determine the connectivity of a design. Because the designer bound the netlist file to the block symbol during the top-down design, the logic synthesizer's output netlist is automatically attached to the initial OrCAD block diagram. **Fig 3** shows the final schematic in OrCAD's graphical format.

The designer could have begun with high-level equations, truth tables, finite-state machine descriptions, or even existing netlists and used this same logic-synthesis software for other modules in the high-level block diagram. All such descriptions would produce gate-count estimates to determine if the partitioning approach were practical.

Applications abound

Using logic synthesis and optimization extends well beyond the simple illustrations in this article. This section provides additional application ideas.

A design formulated on behavior, rather than on gate connections, will provide more latitude for the synthesis tool.

You can use logic synthesis to convert existing ROM, PLD, or FPGA implementations to a gate array or standard cell. Because many synthesis tools support equation and truth-table formats, they can interface to popular CUPL, Boolean, OrCAD, PLD, or ABEL languages. Even ROMs may benefit from logic-synthesis conversion, resulting in less silicon in the case of sparse ROM arrays.

An engineer may have a complete netlist and require a schematic for documentation. This requirement may be important if the engineer or ASIC vendor has not documented last-minute changes to the netlist. Once the synthesizer translates the netlist, the synthesizer can produce a gate-level schematic of the final circuit as well as workstation-compatible files.

Logic-synthesis tools can help you and the foundry accommodate different clocking schemes. At the chip level, whereas designers may use one clocking scheme, ASIC foundries may take a different approach to handling system-clock distribution. For example, gate arrays and FPGAs may use large, lumped buffers in the I/O section to drive extremely long, high-capacitance nets. Some gate arrays use tapered-width metal traces to balance the loading to individual modules. You may create your design using gate arrays or FPGAs, but your foundry may use only standard cells. Using a standard cell may require distributed clocking along with signal rebuffering and locating balanced loads throughout the chip core. You or the foundry can use a logic-synthesis tool to automatically convert from one scheme to another. In this case, the tool can create a distributed clock tree, ensuring minimum edge skew by automatically balancing clock loading and delays.

You can use the synthesis tool to convert an existing schematic into another form. You may add or change vendor libraries, convert from gate array to standard cell, or upgrade to a new technology.

Finally, some logic-synthesis tools offer options that feature automatic test-program generation (ATPG) and testability logic. Inserting testability logic such as scan test or JTAG logic automatically during synthesis frees you to concentrate on the design without making manual compromises for testability considerations.

Guidelines and limitations: user caveats

Logic synthesis can be effective, and its predictable results can instill confidence in its users. Here are some guidelines that will help you achieve consistent satisfaction with these tools:

Synthesis is not a panacea for every design. Your expectations should be realistic.

- Logic synthesis is most effective when you achieve some expertise with the tool. You are always in control; the tools aid but don't replace the designer.
- Prudent use of available options and features will enhance the final design.
- Even with proper use, a synthesis tool will not readily accept every design. For example, not every design will be smaller after optimization. Understand these limitations, thoroughly read the

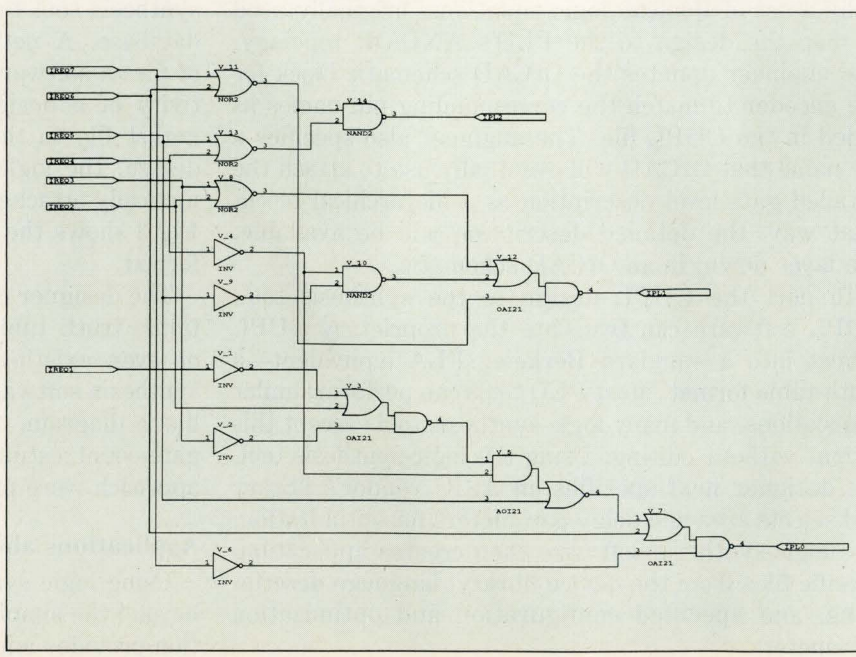

***Fig 3—From a PLD-design file, the logic-synthesis** tool produced an output file that OrCAD displays as a gate-level schematic.*

manuals, and talk to application-support people before plunging in. "Knob-twirlers" who do not systematically master their logic-synthesis tool will waste precious resources.

Tool efficiency depends highly on design description.

- A detailed description may overly constrain the synthesis tool, whereas a very abstract design definition will probably yield disappointing results. In fact, synthesis tools are only beginning to support true behavioral descriptions.
- Most synthesizers use subsets of VHDL or Cadence Design Systems's (Lowell, MA) Verilog. These tools have constructs to instantiate a specific library component when the language will not allow the synthesizer to create one. Be sure to learn the details of programming in an HDL format. But be forewarned: mastering a language such as IEEE 1076 VHDL will take a significant amount of your time.

Partitioning and structure choices greatly affect results.

- Synthesis is still a CPU-intensive procedure with finite limits. Synthesis tools work better on smaller partitions, especially logic groups separated by

How to differentiate among synthesis tools

Commercial logic synthesis has its roots in tools that generate PLD fuse maps from sum-of-products equations. At logic synthesis' most general level, the logic-synthesis tools rely on logic-library parameters to synthesize gate-array and standard-cell ASICs.

Several companies make synthesis tools. Synopsys' Design Compiler (Mountain View, CA), Racal-Redac's Silcsyn (Westford, MA), Mentor Graphics' Design Consultant (Beaverton, OR), Viewlogic's VHDL Designer (Marlboro, MA), and ISS' Instant Logic (Research Triangle Park, NC) are representative suppliers. LSI Logic (Milpitas, CA) and VLSI Technology (San Jose, CA) are two ASIC foundries that have their own software, LES and ASIC Synthesizer, respectively.

Given that the software ranges in price from less than $1000 to more than $100,000, you should ask if cost reflects value. To start with, each company offers synthesis and optimization compilers in some form. As cost—but not necessarily quality—increases, so do the nearly endless variety of features and options. Expect your time as well as money investment to grow with complex packages. Rather than detail each vendor's product, here are categories of features to look for:

Computers and user interfaces

Some packages interface to a wide variety of machines and have outputs targeted to a plethora of supported schematic- and netlist-database formats. Sophisticated graphics, mouse-driven pull-down menus, command script languages, schematic view options, and support for the X-Window System graphical environment are noteworthy features to look for.

Input source-language formats

The prevailing trend is to support the two major industry-standard HDL languages, IEEE 1076 VHDL and Verilog. Some vendors support additional proprietary HDL formats, particularly those workstation vendors who have already established a high-level format for simulation support.

A long list of compiler parameters are available. Some examples include: area limits; maximum and minimum propagation delay; maximum and minimum rise and fall delay; setup, hold, and clock-edge checking; operating condition variations in temperature, voltage, and process; maximum driving pin transition time; and maximum pin fanout.

Vendor library support

Some synthesis tools feature a long list of vendor-endorsed ASIC libraries. All the packages allow you to create new libraries from vendors' spec sheets. However, the official libraries offer accuracy and support that become important when the vendor receives your design for fabrication.

Options and extensions

Optional features for some software include timing verification, automatic test-program generation, and test synthesis.

Horsepower

Design size and logic-synthesizer speed depend on the computer that the logic synthesizer runs on. But efficient algorithms and cost functions used during compilation can coax more performance from a computer.

Engineers can justify the modest time investment needed to learn and employ logic synthesis as their designs' sizes increase.

function. You should separate blocks of random combinational logic from more structured circuitry. Regular, replicated structures, such as data-path, arithmetic, and counter logic are not likely to synthesize efficiently. A function such as a simple binary decoder will reduce quickly with manual techniques, but may take some effort to describe to a synthesis tool. In these cases, you should simply generate a conventional schematic or netlist, or use a parameterized compiler from a major ASIC vendor.

- Some synthesis packages can selectively compile a design, allowing for manual intervention.
- Control logic, glue logic, and well-defined state machines are good synthesis candidates. (Irregular logic structures may be a mere fraction of a highly integrated design, but they can consume a disproportionate share of a designer's time. Therefore, the quibble that a synthesis tool should handle only this little chunk of a design is not valid.) They also become difficult to maintain and document as the design "band-aids" grow. Apply discipline; use an HDL or alternate high-level format. The result will be a more streamlined, quickly implemented, and error-free design.
- When optimizing existing netlists, be especially careful with partition size. Very small modules are ineffective, whereas very large modules overtax the computer. Attempt to work within a guideline range of 300 to 3000 logic gates.

Area and delay optimization are not always independent functions.

- Area optimization will sometimes result in the best delay specifications too. You cannot always move along the mythical area-delay tradeoff curve. In reality, a reduced area implies a reduced gate count, hence, a reduced source of delay.

Back-annotated netlists perform differently.

- What happens after the handoff to the ASIC foundry? The ASIC gate-array or standard-cell foundry will usually autoroute your design. You will have little control over how they autoroute an individual net. Actual delays of longer runs, especially, will probably deviate from your logic-synthesis tools' pre-routing estimates. You should anticipate and leave leeway for the inevitable differences in pre- and post-autorouting delays as you optimize your design. When using the logic-synthesis tool to optimize a design that has critical paths, you should maintain a close interface with the foundry to avoid having to autoroute the design more than once.

You may lose traceability to your original design.

- A random-logic netlist can reduce to an optimized output and a modified schematic. But don't expect specific nodes and signal names to be intact—the synthesis tool may "collapse" them, or factor them out. A higher-level description provides an alternate reference for engineers who depend on schematic diagrams for ultimate verification.

Don't pay for what you don't need.

- Most of the full-featured synthesis tools are expensive. Be sure to understand what each base package provides and what options you will need to complete a project.

High-level design may not be a natural style.

- Many engineers design visually, decomposing a function into specific library elements in the comfort of a schematic-capture environment. For these designers, synthesis tools will work best as optimizers, reducing random-logic gate count.
- Synthesis offers much more for those who can think in abstract, textual terms. These designers should try to conceptualize the design's structure or behavior and let the tool work through the translation and mapping details. This method will become inevitable as designs grow beyond human ability to create at the primitive (transistor, gate, or small-module) level. As an added advantage, structural or behavioral formats transport easily to different vendors' high-level languages and synthesis packages.
- Even after engineers are convinced that synthesis represents the wave of the future, the most difficult task becomes allocating time. You will have to expend significant effort to learn and adapt to new methods. Absorbing the detailed information in a logic-synthesis manual or design course takes time. Even after making this investment, the results achieved strongly correlate with an engineer's synthesis experience. A single pass or first design seldom produces ideal results. An engineer may face his biggest test *after* convincing management to purchase expensive software to improve productivity. If an engineer has not moved very far along the learning curve, he may have to explain to this same management that the initial use of the tool will delay the project's schedule.

The mechanics of performing logic synthesis are rela-

tively straightforward, so you won't have difficulty justifying the modest time investment needed to learn and employ this technique. As the size of designs increases, the time it takes to learn and use other logic-design techniques grows disproportionately, whereas logic synthesis' learning and design time increases more gradually in relation to gate count. Furthermore, logic synthesis can efficiently reduce a large, raw design by 20 to 30%, whereas manual methods are inefficient for large designs. **EDN**

Author's biography

Joseph L Paradise started his own consulting firm, specializing in technical writing, presentations, and training, one year ago. Previously, he spent 20 years in the IC industry in design-engineering and management positions, all involving semicustom IC design or CAD support. He obtained a BSEE from the New Jersey Institute of Technology (Newark, NJ) and a masters in electrical engineering from Stevens Institute of Technology (Hoboken, NJ). He is a member of the Society for Technical Communications. In his spare time, he enjoys woodworking and camping.

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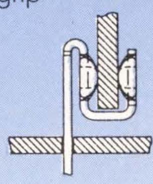
TAKE SOLDER PASTE AND DIPPING OUT OF CIRCUITS ASSEMBLY

...and improve product reliability

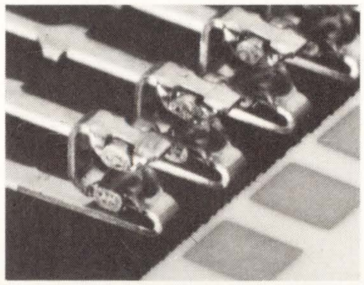
NAS solder and flux bearing edge clips are applied with a method that is simple, quick and exceptionally consistent. Solder paste, solder and flux dipping, and board clean-up — all steps in the circuits assembly process that yield high rates of rejects — are eliminated.

Preforms on edge clip terminals contain precisely the right amounts of the proper solder and flux for each application, and the exclusive NAS "Claw" grip holds each preform. This unique grip design provides direct contact between solder and conductor pads, a beneficial wiping action as clips are attached and positive control of solder flow. A single reflow operation for top and bottom preforms — using any method that raises temperatures to reflow levels — produces perfect solder joints every time.

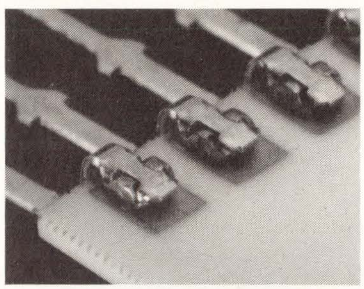


When you use NAS solder and flux bearing edge clips, expensive rework becomes virtually a thing of the past.

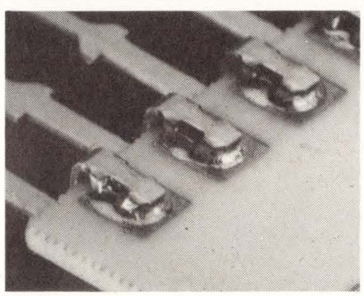
The simple, efficient method of applying NAS solder and flux bearing edge clips:



Direct contact between solder preforms and conductor pads produces a beneficial wiping action as clips are attached, either manually or with a lead attachment machine.



Interference fit holds clips firmly in position for reflow. Top and bottom preforms are reflowed in one operation using any method that raises temperatures to reflow levels.



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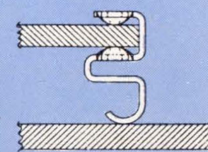

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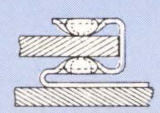

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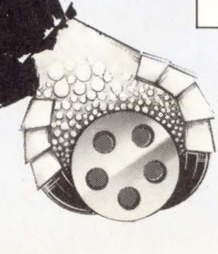

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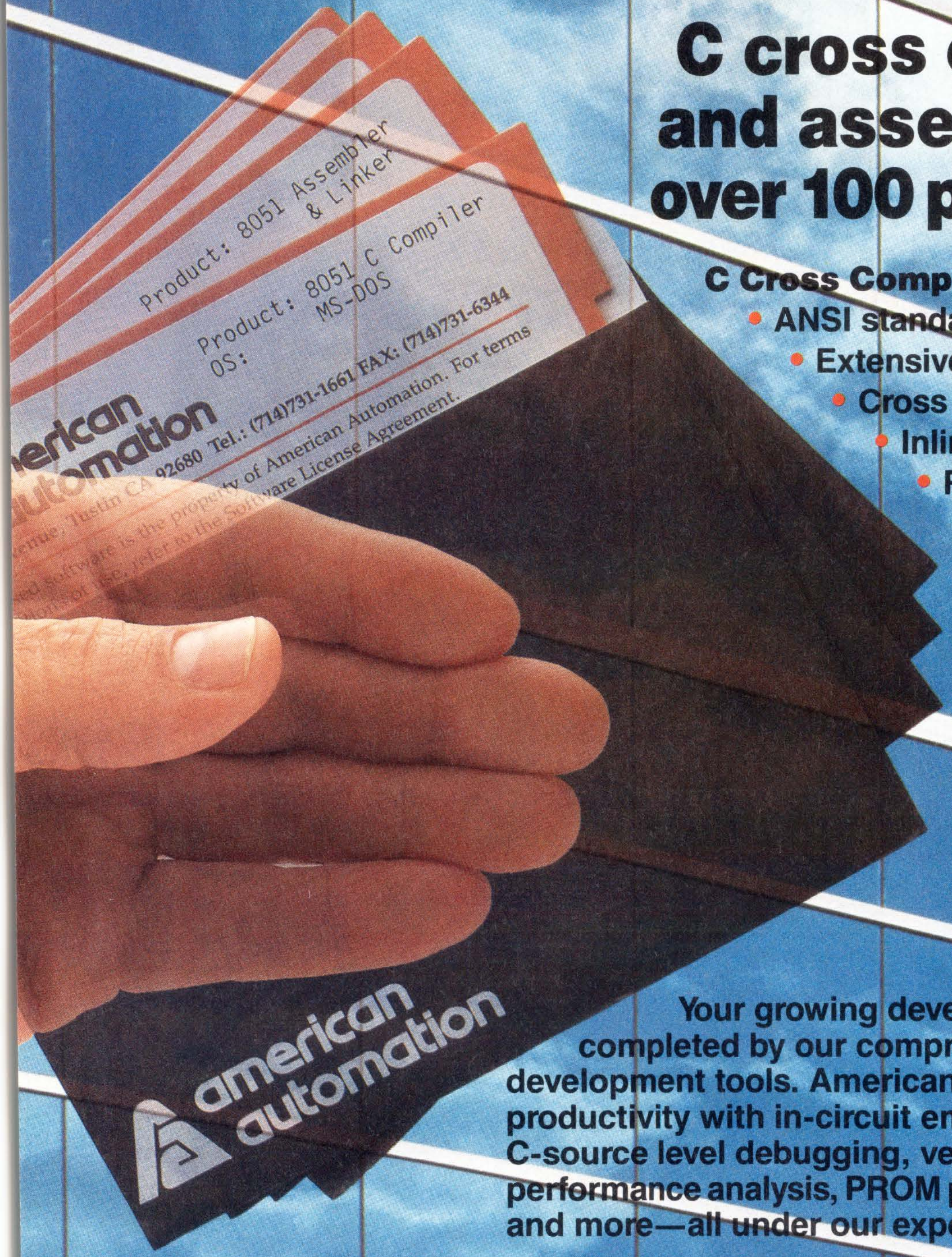

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DESIGN NOTES

No Design Switiching Regulator
5V Buck-Boost (Positive to Negative) Regulator – Design Note 49

Ron Vinsant

Introduction

This simple, no design regulator, operates with an input between 4.5V DC and 40V DC. It provides a –5V output at a maximum output current of 1A to 3A depending on input voltage.

This converter is based on the Linear Technology LT1074 switching regulator IC. This device needs only a few external parts to make up a complete regulator including thermal protection and current limit. This design uses off-the-shelf parts for low cost and easy availability of components. Specifications for the circuit are in Table 1.

Circuit Description

Figure 1 shows the schematic of the circuit. For the purpose of this explanation assume that the output is at a constant –5V DC and that the input voltage is greater than +4.5V DC.

At intervals of $\approx$10µs (100kHz) the control portion of the LT1074 turns on the switch transistor between the V_{IN} and V_{SW} pins impressing a voltage across the inductor, L1. This causes current to build up in the inductor.

The control circuit determines when to turn off the switch during the 10µs interval to keep the output voltage at –5V DC. When the switch transistor turns off, the magnetic field in the inductor collapses and the polarity of the voltage across the inductor changes to try and maintain the current in the inductor. This current in the inductor is now directed (due to the change in voltage polarity across the inductor) by the diode, D1, to the load. The current will flow from the inductor until the switch turns on again, (continuous operation) or until the inductor runs out of energy (discontinuous operation).

C2 is a low ESR type electrolytic capacitor that is used in conjunction with L1 as the output filter. C5 and L2 form a post filter that reduces output ripple further.

Referring back to Figure 1, the divider circuit of R1, R2, R3 and R4 is used to set the output voltage of the supply against an internal voltage reference of 2.21V DC.

R3, R4, C3 and C4 make up the frequency compensation network used to stabilize the feedback loop.

Conclusion

This Design Note demonstrates a fully characterized positive to negative converter circuit that is both simple and low cost. This design can be taken and reliably used in a production environment without the need for any custom magnetics. A P.C. board layout and FAB drawing are available from Linear Technology.

Table 1. Performance Summary (Operating Temperature Range 0°C to 50°C)

Input Voltage Range			+4.5V to +40.0V DC
Output	Output Voltage (±0.15V DC)		–5.00V DC
	Max Output Current At V_{IN} = 4.5V DC		1.0A DC
	Max Output Current At V_{IN} = 40.0V DC		3.5A DC
	Typical Output Ripple at I_{OUT} = 2.5A DC @ Switching Frequency	With Optional Filter (L2 & C5) Without Optional Filter (L2 & C5)	50mVp-p 300mVp-p
	Load Regulation V_{IN} = 4.5V DC	At I_{OUT} = 0.1A DC to 1.0A DC	0.6%
	Line Regulation I_{LOAD} = 1A	At V_{IN} = 4.5V DC to 40.0V DC	0.2%

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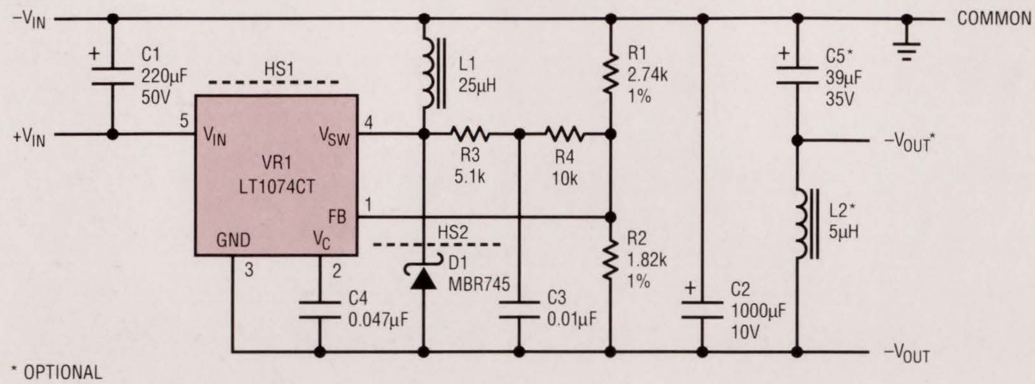

$$-V_{OUT} = 2.21\left[1 + \frac{R1 \,||\, (R3 + R4)}{R2}\right]$$

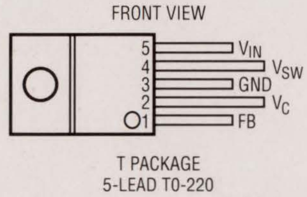

Figure 1. Package and Schematic Diagrams

Table 2. Parts List

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR
PCB	1	003A	PCB FAB, Buck-Boost Converter	LTC
D1	1	MBR745	Diode, Schottky, 7A, 45V	Motorola
HS2	1	6038B-TT	Heatsink	Thermalloy
VR1	1	LT1074CT	Switching Regulator, 100kHz	LTC
HS1	1	7020B-MT	Heatsink	Thermalloy
C1	1	UPL1H221MPH	Cap, Alum Elect, Low ESR, 220µF, 50V	Nichicon
C2	1	LXF10VB272M12X30LL	Cap, Alum Elect, Low ESR, 1000µF, 10V	United Chemicon
C3	1	CK06BX103K	Cap, Ceramic, 0.01µF, 100V	AVX
C4	1	CK05BX473K	Cap, Ceramic, 0.047µF, 100V	AVX
C5	1	UPL1V390MAH	Cap, Alum Elect, Low ESR, 39µF, 35V	Nichicon
L1	1	CTX 25-5-52	Inductor, 25µH, 5A	Coiltronics
L2	1	CTX5-5-FR	Inductor, 5µH, 5A	Coiltronics
R1	1	MF 1/8W 2.74kΩ	RES, MF, 1/8W, 1%, 2.74kΩ	
R2	1	MF 1/8W 1.82kΩ	RES, MF, 1/8W, 1%, 1.82kΩ	
R3	1	CF 1/4W 5.1kΩ	RES, CF, 1/4W, 5%, 5.1kΩ	
R4	1	CF 1/4W 10kΩ	RES, CF, 1/4W, 5%, 10kΩ	

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EDITED BY CHARLES H SMALL

DSP system comprises only five major chips

Vladimir Bochev
Bulgarian Academy of Sciences, Sofia, Bulgaria

If you go beyond Texas Instruments' TMS320C2x application notes, you can make a digital-signal-processing system from the DSP μP, four memory chips, and a handful of PAL devices. **Fig 1** is a sketch of such a system. The host-interface and wait-state circuits are left for you to handle. This design will never need upgrading because it accommodates the DSP μP's maximum allowed memory in minimal area.

The key to the design's compactness is the Micron MT5C1008 128k×8-bit static RAMs. These RAMs provide, in one package, the separate data and program memory that the architecture of DSP μPs demand. The circuit decodes the program-select line ($\overline{PS}$) to determine which port of the dual-port RAMs to access.

The design uses Cypress CY7C132 2k×8-bit dual-port static RAMs as global memory when the DSP μP asserts its $\overline{BR}$ pin. This pin is under your software's control. The system communicates with the outside world via its global memory.

The address and data buffers in **Fig 1** enable a host to set up and control the DSP system. The OR-gate circuit below the main diagram in **Fig 1** is an alternative way to disable the system's memory when the global memory is operating.

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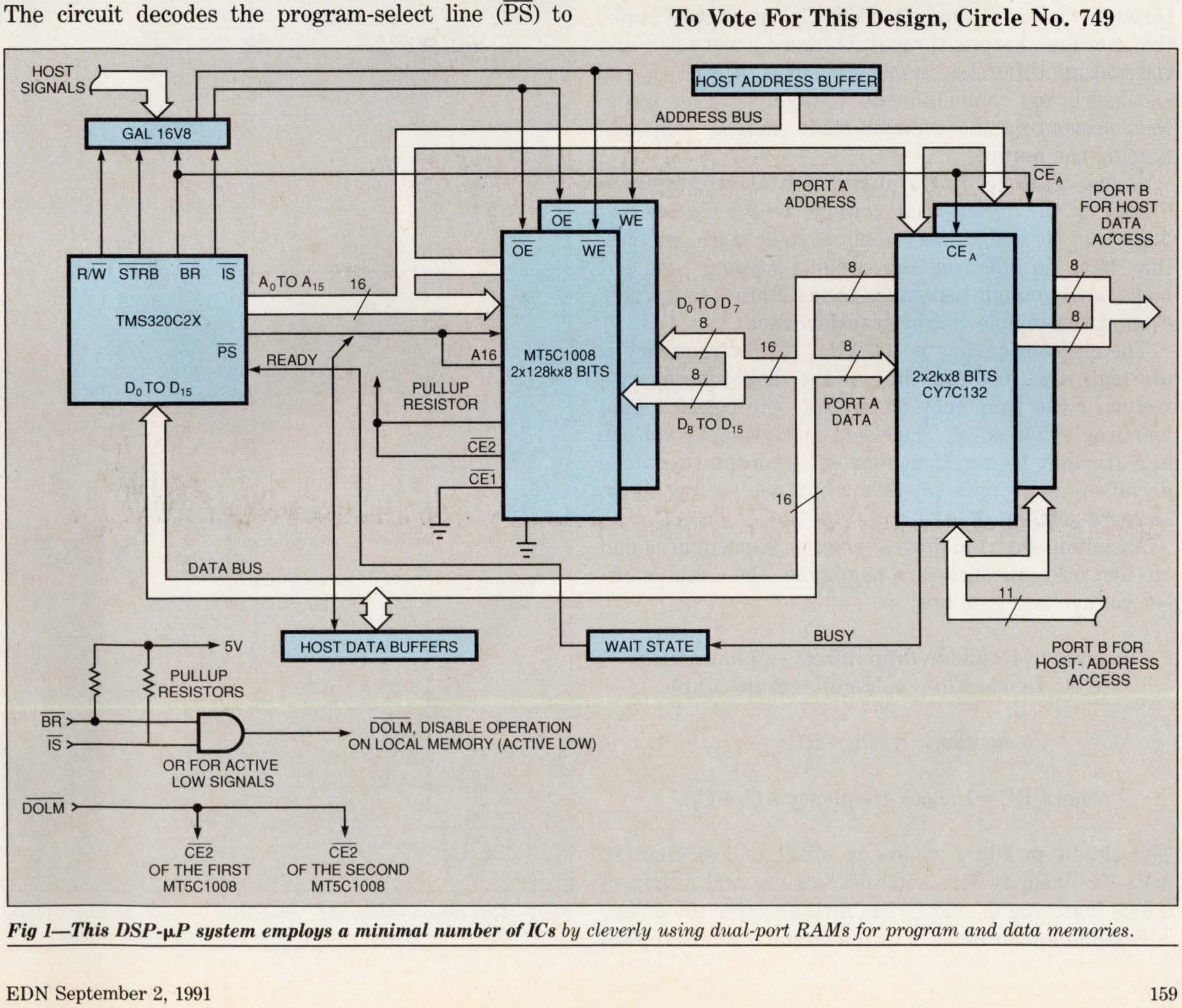

***Fig 1—This DSP-μP system employs a minimal number of ICs** by cleverly using dual-port RAMs for program and data memories.*

Capacitive coupling tames high voltage

Henry Yiu
Perkin Elmer, Pomona, CA

The differential amplifier in **Fig 1** uses charge balancing to bring differential voltages imposed on high common-mode voltages down into a range that the amplifier's IC can handle. This scheme avoids the costly precision resistors and horde of components that other designs require.

When the clock is low, C_1 charges through diodes D_1 and D_2 into C_3. Simultaneously, C_2 charges through diodes D_3 and D_4 into C_4. The voltages across C_3 and C_4 do not change much because C_3 and C_4 are so much larger than C_1 and C_2.

When the clock is high, C_1 discharges through diodes D_5 and D_6 from C_4. Simultaneously, C_2 discharges through diodes D_7 and D_8 from C_3. At steady state, the average charges through C_1 and C_2 are zero, and the voltage difference across C_3 and C_4 is V_{IN}. C_3 and C_4 absorb any common-mode voltage, however large, thus preventing the common-mode voltage from disturbing the output.

A low-leakage JFET instrumentation amplifier measures the differential voltage across C_3 and C_4. Note that R_1 and R_2 serve only to keep a proper bias; they have no effect on the circuit's settling time but must have enough resistance to maintain a unity gain even at reasonable charge-transfer rates.

The clock frequency is 100 kHz. If this frequency is too high, the recovery time of the diodes becomes a factor; if the frequency is too low, the circuit's gain will drop below unity. The clock's peak-to-peak voltage is a fraction higher than four diode drops to reduce dc offset and ripple injection, but not so low as to increase settling time.

Assuming that the diodes' junction capacitances and on- and off-resistances are negligible, the circuit's offset voltage and gain are

$$\text{dc offset} = 4 \times (\text{diode-drop offset}) + (\%\ \text{mismatch}\ C_1\text{-}C_2) \times (\text{clock p-p voltage}) \times (\text{diode drop})$$

$$\text{dc gain} = R_1/(R_1 + RC),$$

$$\text{where } RC = 1/(\text{clock frequency} \times C_1 + C_2).$$

The circuit in **Fig 1** yields an offset of less than 20 mV, 1% linearity for ±500-mV inputs, and a gain of 0.995. Matching C_1 and C_2 can further lower the offset.

Possible enhancements to the circuit include replacing D_2, D_4, D_6, and D_8 with analog switches to reduce the offset that the diodes cause and putting zener diodes in series with the other diodes to raise the instrumentation amplifier's input voltage above two diode drops. **EDN BBS /DI_SIG #1013** EDN

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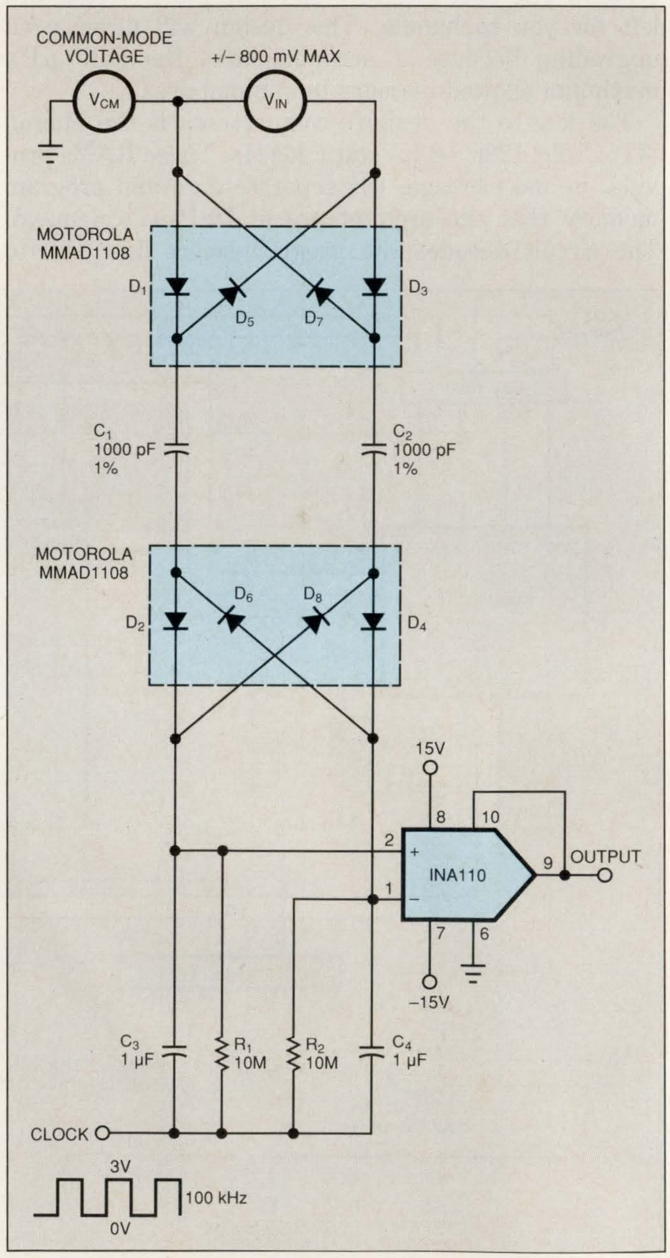

*Fig 1—**This charge-balancing, capacitive voltage divider** isolates a tiny differential voltage from a large common-mode voltage.*

Active filter discriminates FM

K Radhakrishna Rao and Ajoy Raman
Indian Institute of Technology, Tamil Nadu, India

Because the Burr-Brown UAF41 universal filter provides four second-order outputs, you can use it as the basis for a wideband, linear discriminator for sinusoidal signals. Using the values **Fig 1** specifies, the circuit develops a ±10V output corresponding to a ±15% frequency deviation from a 10.5-kHz center frequency. The circuit's accuracy is 1%, and the circuit handles 1 to 5V inputs without loss of accuracy.

IC_1 in **Fig 1** develops V_{O1} (bandpass), V_{O2} (lowpass), V_{O3} (highpass), and V_{O4} (notch). If you set the filter's gain at unity and symbolize the filter's pole Q as Q_O and its center frequency as ω_O, the magnitude of the filter's transfer function is

$$|V_{O4}/V_{O1}| = Q_O((\omega_O/\omega) - (\omega/\omega_O)).$$

Setting $\omega = \omega_O + \Delta\omega$ simplifies the transfer function—as a first approximation—to

$$|V_{O4}/V_{O1}| = -2Q_O\Delta\omega/\omega_O.$$

In this form, the transfer function resembles that of an FM discriminator. Note that such an FM discrimi-

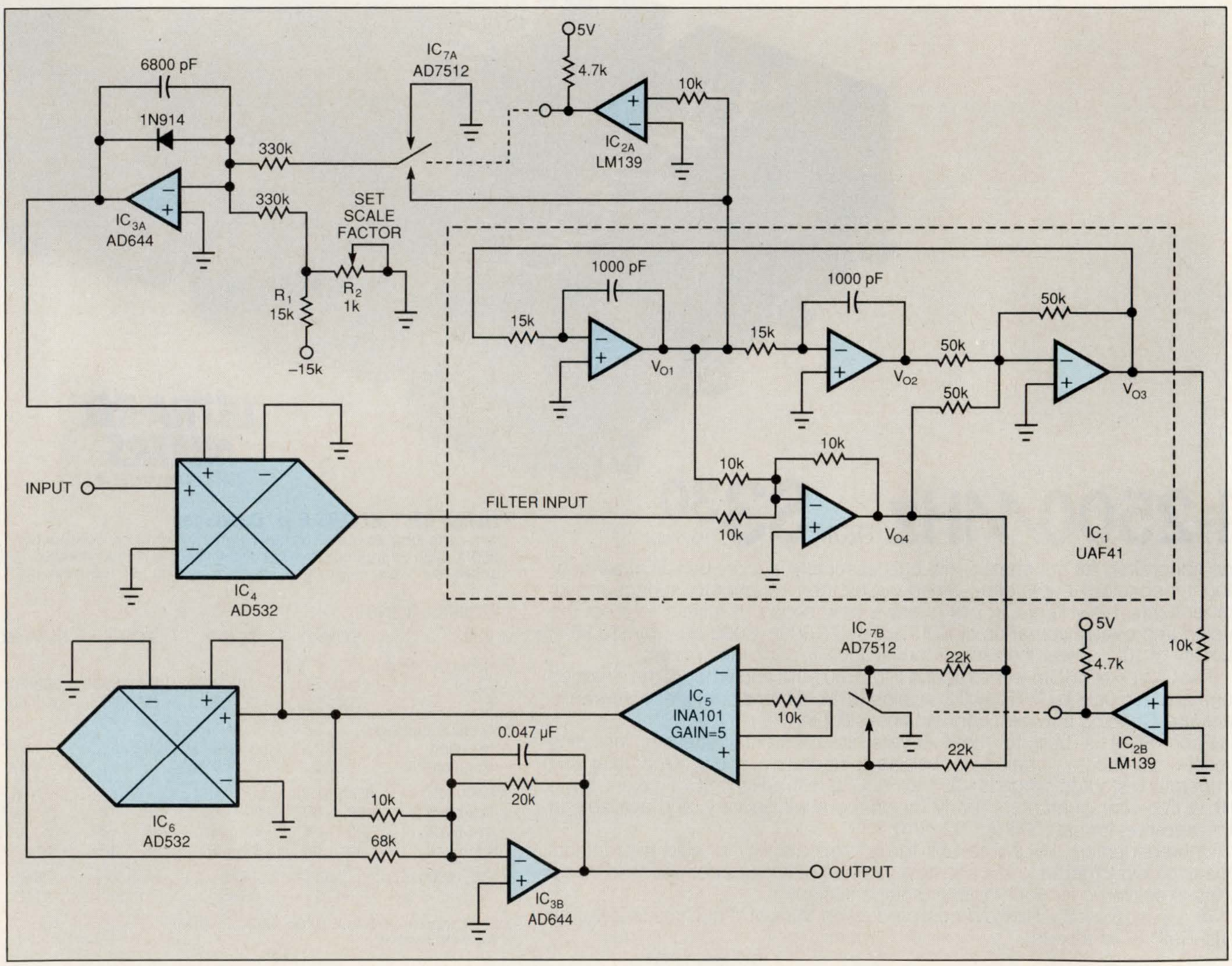

Fig 1—Illustrating a classic exercise in analog computation, *the universal filter, instrumentation amplifier, multipliers, and other components form a wideband FM discriminator.*

nator has two desirable properties: Its sensitivity is independent of its center frequency, and the output's magnitude does not depend on the input's magnitude.

In **Fig 1,** multiplier IC_4 controls the amplitude-control loop around IC_1. This loop keeps the magnitude of the bandpass output, V_{O1}, constant. Comparator IC_{2A} and analog switch IC_{7A} half-wave rectify V_{O1}. Integrator IC_{3A} compares the average value of V_{O1} to the reference voltage from divider R_1-R_2, thus developing a control voltage for multiplier IC_4.

The phase relationship between the notch output, V_{O4}, and the highpass output, V_{O3}, provides the key to obtaining the magnitude of V_{O4}. The notch output is either in phase with V_{O3} or out of phase with V_{O3}. Note that comparator IC_{2B} and analog switch IC_{7B} synchronously rectify V_{O4} by switching the inputs of instrumentation amplifier IC_5.

To obtain accuracy better than 0.1% for ±15% deviation, you must reintroduce the second-order term, $(\Delta\omega/\omega)^2/2$. Multiplier IC_6 squares the circuit's output, and IC_{3B} adds the properly scaled second-order term to the first-order term to produce an accurate output.

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Modified RTD bridge eliminates errors

R Jayapal
Bharat Heavy Electricals Ltd, Tamil Nadu, India

Fig 1 shows an improved method of measuring temperature with a resistive temperature detector (RTD). This scheme works especially well for self-heated RTDs used in flow meters. In such applications, relatively large excitation currents flow through the detectors. Such large current flows render conventional bridge schemes, which must have closely matched currents in both arms of the bridge, ineffective and subject to error.

The circuit in **Fig 1** eschews a bridge. Instead, the measuring and reference detectors are connected in series. The circuit's differential-output voltage is a function of resistance only. Because the detectors are in series, current-mismatch errors cannot arise.

A standard IC723 voltage-regulator circuit supplies the excitation current.

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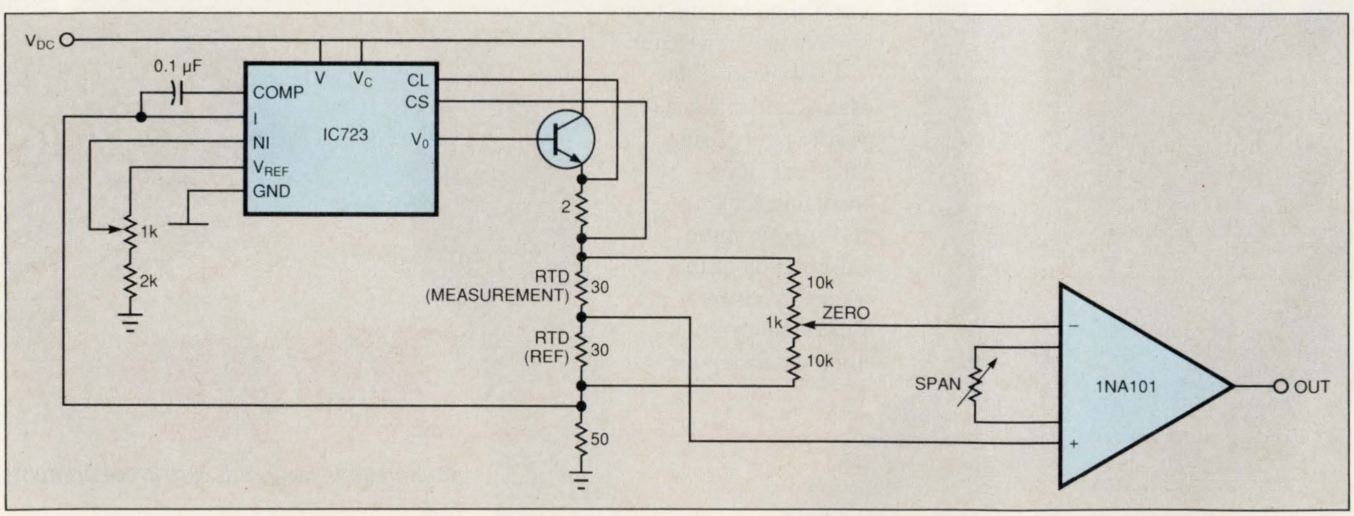
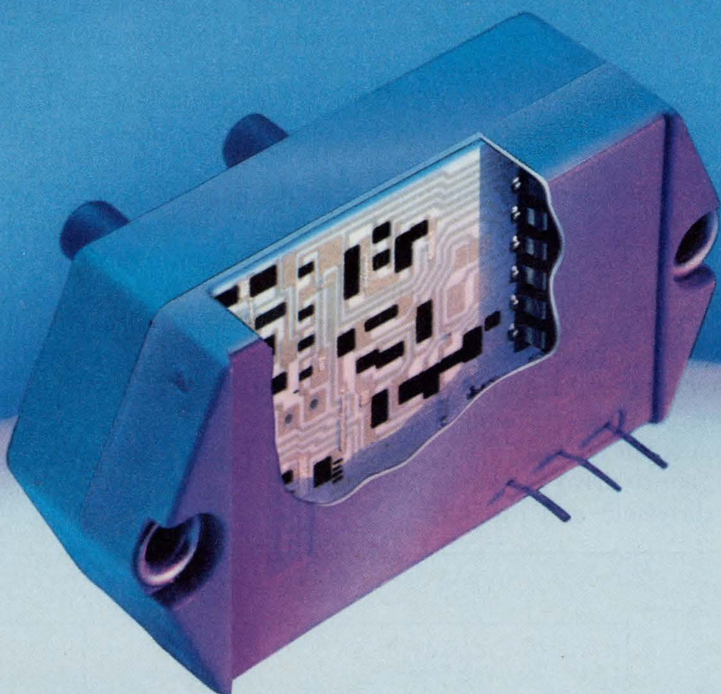


***Fig 1—Exciting both a reference and a measuring RTD** with the same current avoids current-imbalance errors.*

HAWKER SIDDELEY

Advanced Pressure Sensors



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142SC series .. 0 to 1psi up to 0 to 150psi

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CIRCLE NO. 121

1244 Reamwood Avenue ■ Sunnyvale, CA 94089 ■ Tel: (408) 744-1500 ■ Fax: (408) 734-0407

Battery powers isolated pulser

John A Haase
Colorado State University, Fort Collins, CO

The pulse generator in **Fig 1** produces a 5 or 10V, constant-amplitude, isolated output into a 50Ω load. The signal presented to the generator's trigger input can vary over more than a 30:1 range. The minimum triggering pulse is 600 mV for 800 nsec. The circuit can run for one year on two 9V batteries; its low current drain makes it superior to isolation circuits that use optoisolators.

The input triggers the pulse circuit via a common 1:1 pulse transformer. Such transformers support only microsecond step functions, ignoring training edges. Hence, the pulse's duration is not critical.

Transistor Q_2 provides gain to drive the anode gate of thyristor CR_1 below threshold and discharge C_1 through the load. This action results in a fast rise-time pulse output. The negative potential on C_1 at Q_6's emitter determines the voltage level of the output pulse. Switch S_1 selects a 5 or 10V pulse. To ensure maximum output, keep the input-pulse repetition rate below 20 Hz. If you push test switch S_2, the LED will flash every time the pulse generator fires.

Transistor pairs Q_1-Q_2 and Q_3-Q_4 form conventional current limiters rather than constituting voltage-biasing elements. This configuration makes Q_2 a high-impedance, low-drain amplifier. Q_1 and Q_2 are compatible high-beta, low-I_C transistors.

EDN BBS /DI_SIG #1010

To Vote For This Design, Circle No. 748

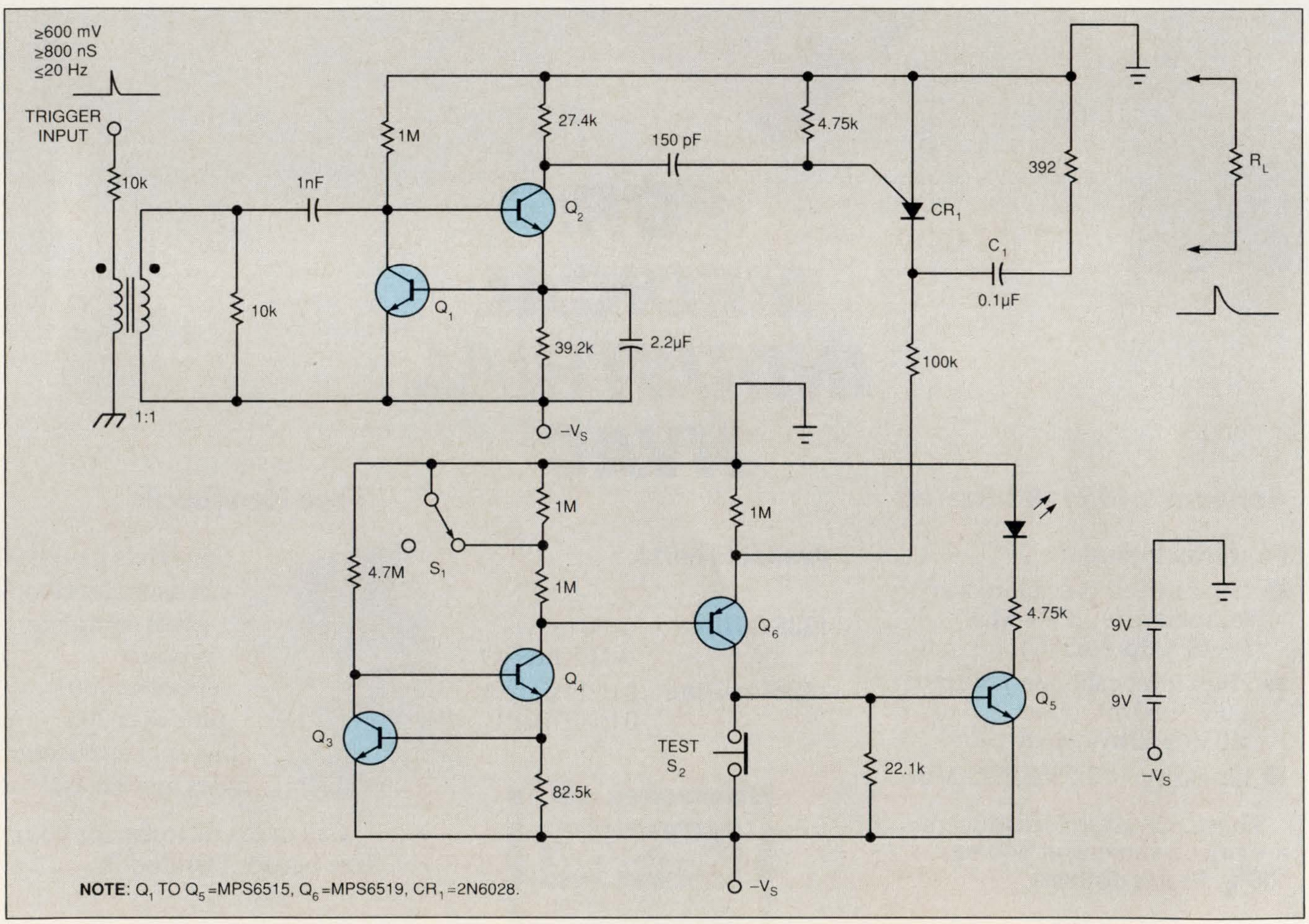
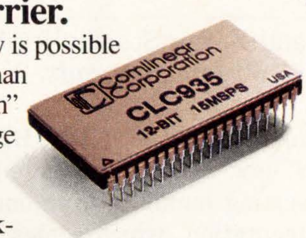


*Fig 1—**This isolated, low-drain pulse generator** will operate for a year from two 9V batteries.*

Because you're thinking fast...

Off-the-chart performance in a new 12-bit, 15MSPS A/D converter.

This one breaks the 74dB barrier.

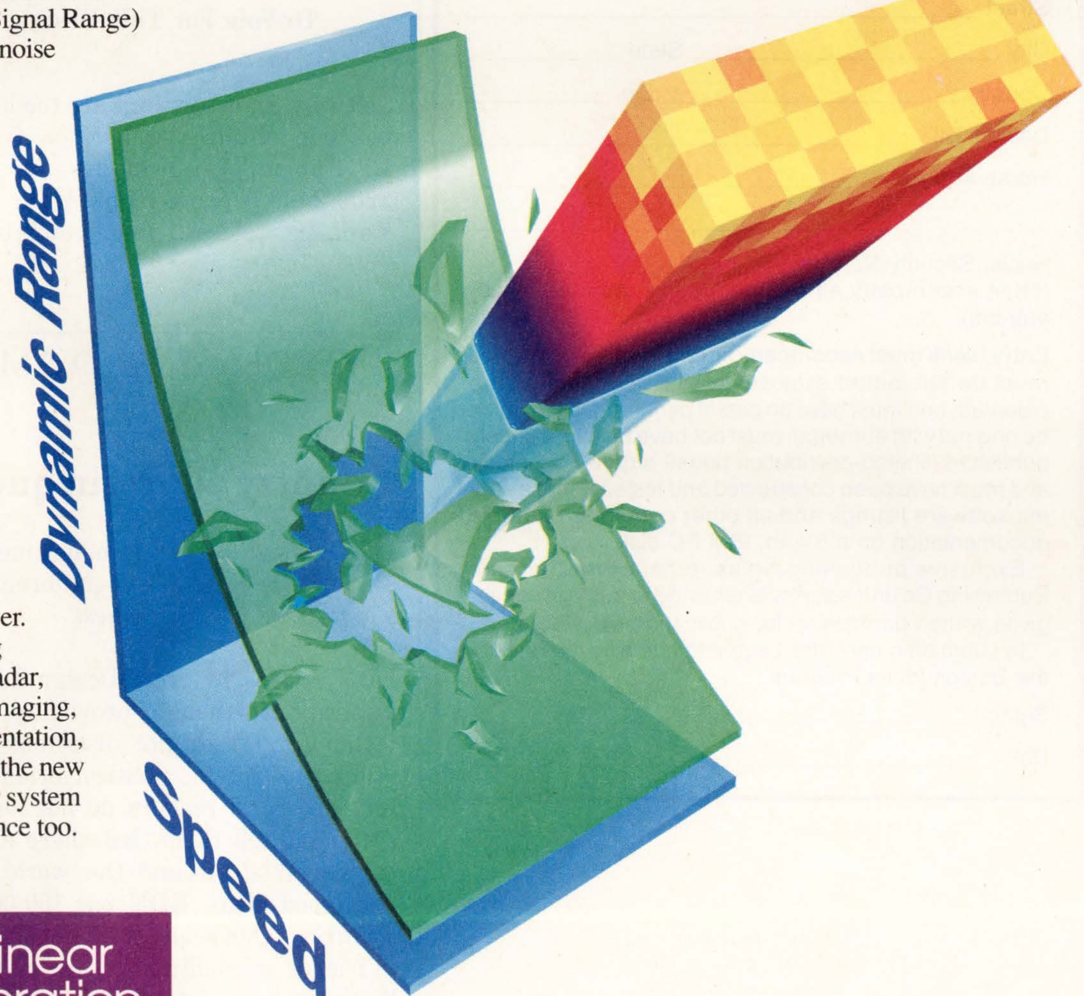


Yes, it really is possible to get more than 74dB of "clean" dynamic range from a 12-bit converter... without breaking the laws of physics.

The secret is in the track-and-hold design. And that's where the CLC935 excels. So you get a 12-bit, 15MSPS converter that has a 75dB SFSR (Spurious Free Signal Range) at 7.5MHz, a signal-to-noise ratio of 67dB out to Nyquist, 0.35 LSB differential non-linearity, and a 135MHz small-signal bandwidth. Now that's a true performance breakthrough in an A/D.

Before now, the only way you could get this performance was with large, expensive board designs. Now, it's available in a 40-pin DIP that takes less than 2.3 square inches of board space. And only 5.2W of power.

So if you're bumping against A/D limits in radar, infrared and medical imaging, ultrasound, or instrumentation, call for details. Maybe the new CLC935 can give your system off-the-chart performance too.



CIRCLE NO. 122

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SOFTWARE SHORTS

New algorithm converts number bases

Dušan Mudrić and Zoran Stojsavljevic
Institute Mihajlo Pupin, Belgrade, Yugoslavia

Extensive documentation in **EDN BBS /DI_SIG #1015** details a new algorithm, called the prefix method, for converting numbers from one base to another. The documentation, which comes with its own nifty, ready-to-run scientific word processor, also contains an example of the algorithm implemented in 8051 single-chip μP assembly language. **EDN**

To Vote For This Design, Circle No. 751

Software Shorts listings are too long to reproduce here; you can obtain the listings from the EDN BBS's DI Special Interest Group (617-558-4241, 300/1200/2400,8,N,1—from Main Menu, enter (s)ig, <s/di_sig>, rk*nnn*, where *nnn* is the number referenced).

FEEDBACK AND AMPLIFICATION

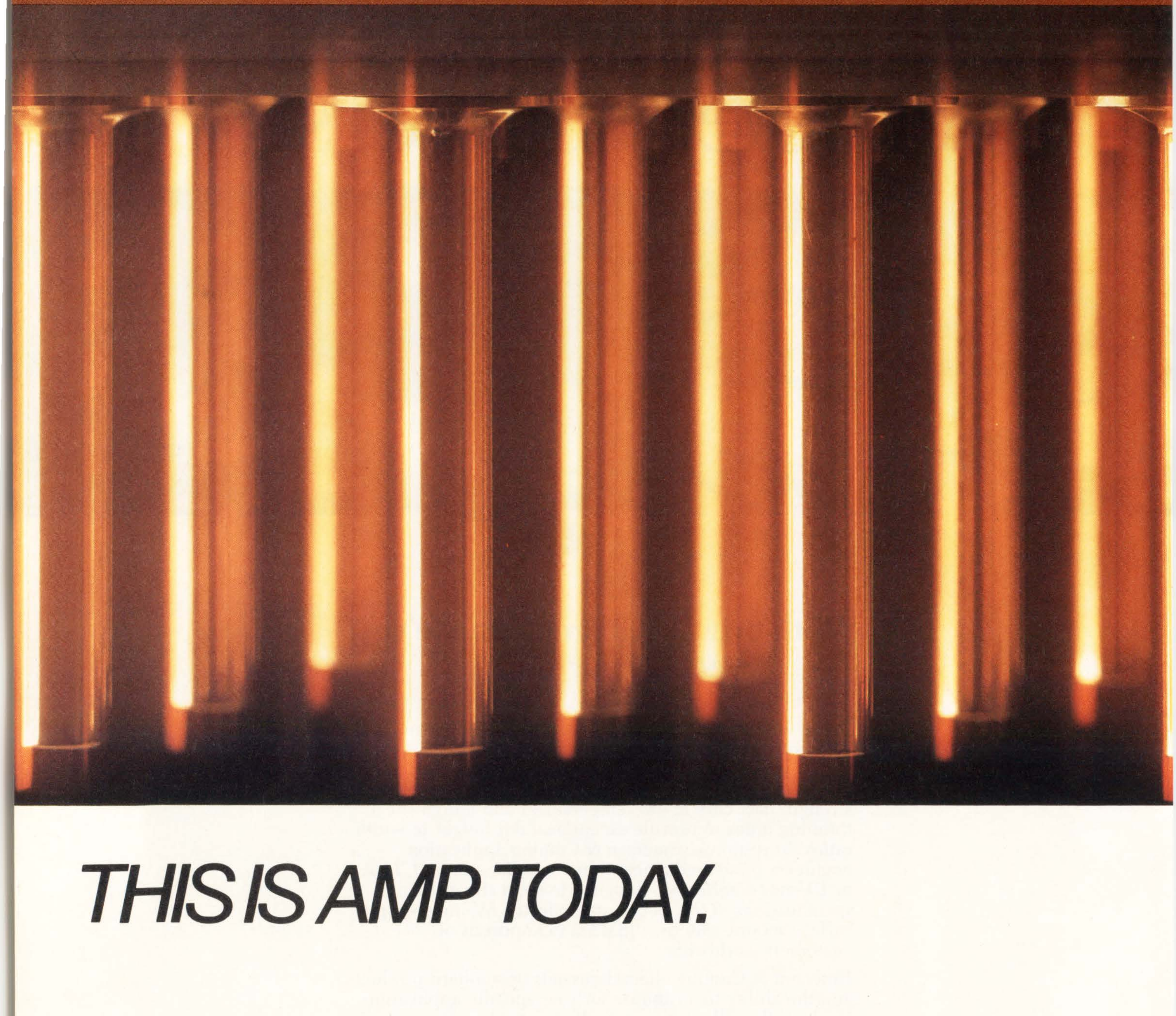
Country of origin questioned

If EDN is an American magazine, why do you publish so many Design Ideas from foreigners?
Name Withheld by Request

EDN strives to print Design Ideas that are useful, inspirational, thought-provoking, educational, and entertaining. We do not discriminate based on gender, country of origin, political orientation, age, race, or religion. EDN readers do not need the Design Ideas section to tell them that there are plenty of brilliant engineers, all around the world, who are brimming with good ideas. EDN has 150,000 readers in several countries. Our readers obviously pass their copies on to friends in countries where EDN is not distributed. We hear from five to ten of these readers, on the average, every day. So if you would like to see more US Design Ideas, then you and your US buddies should send in more good entries.
Charles H Small and Anne Watson Swager
Design Ideas Editors

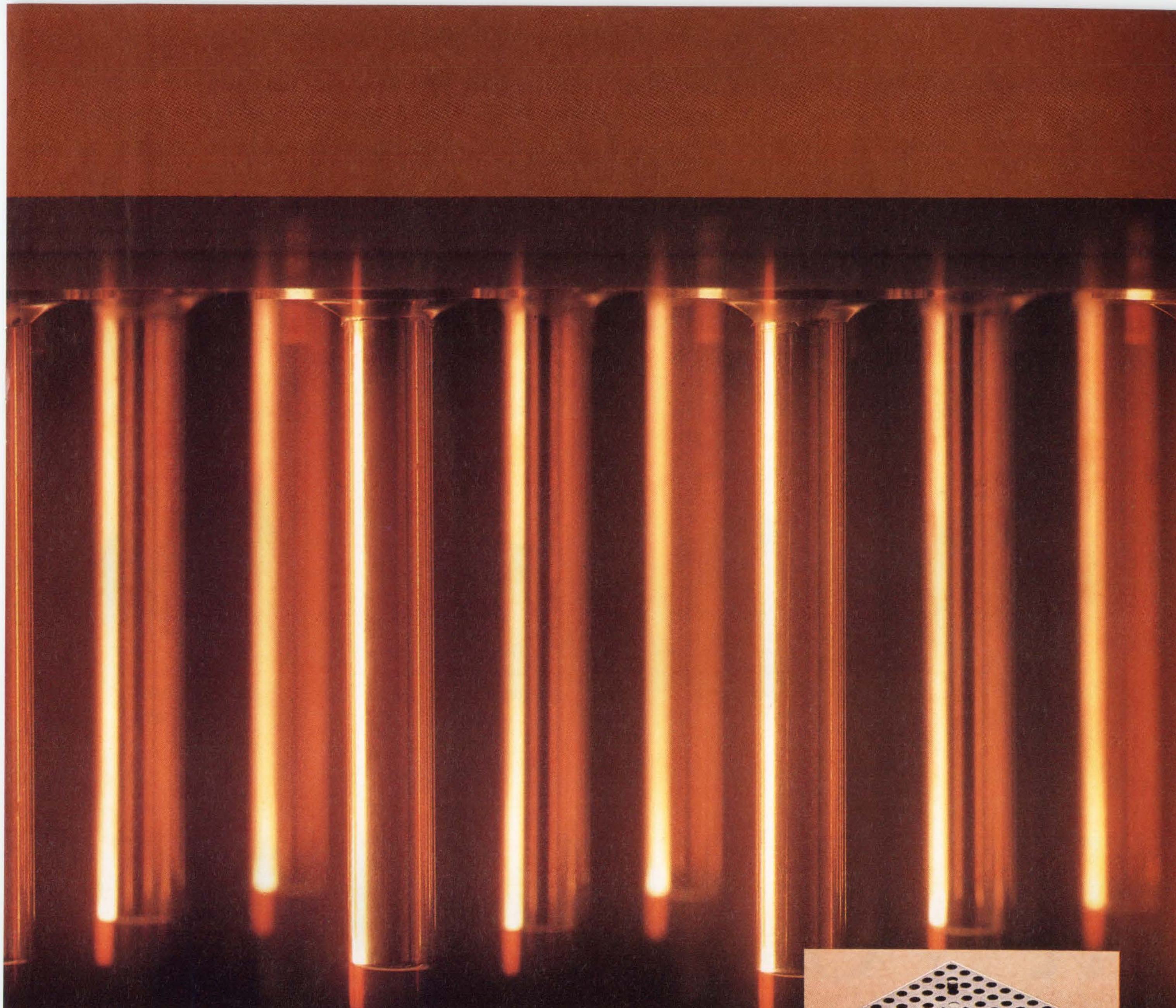
EDN

Helping production cope with the pressures of high pincount packages.



THIS IS AMP TODAY.

*J. B. Cullinane, "A User's Evaluation of Pin Grid Array Sockets", *Connection Technology*, June 1990.

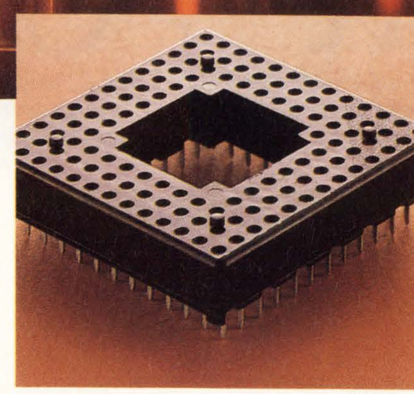


As PGA pincounts go up, so do the insertion/withdrawal forces required to socket them. When counts reach about 121, conventional socket contacts put your total insertion force in the 28 to 50 pound range—hardly conducive to efficient manufacturing.

Not so with AMP LIF PGA sockets. We use a dual-beam contact, and we stagger contact row heights to reduce insertion force requirements dramatically. For the same 121-pin package, our socket design requires an average 13.1 pounds insertion force*, 50-75% lower than conventional sockets. This can make a significant difference in everything from operator fatigue and device stress to board integrity and ease of field service.

And our exclusive design provides excellent normal contact force as well—the contacts utilize a long beam geometry, providing ample deflection with no compromise between normal force and insertion/extraction force.

Sizes: 10x10 to 25x25, with quick turnaround on special patterns. For more information, call the AMP Product Information Center at 1-800-522-6752 (fax 717-561-6110). In Canada call 416-475-6222. AMP Incorporated, Harrisburg, PA 17105-3608.



Dual-beam contact LIF PGA

AMP

CIRCLE NO. 124

is for Bandwidths from DC to video.

means Counts up to 200,000 with the HI-7159.

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is for Just call 1-800-4-HARRIS, ext. 1405, for more information.

stands for Knowledge that our application support people provide.

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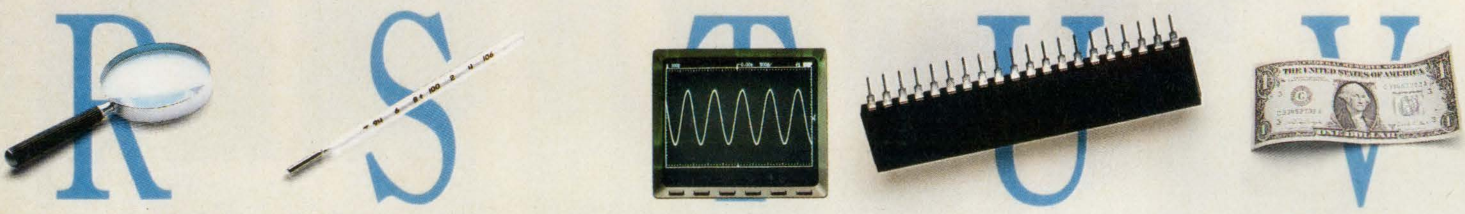


is for Resolutions from 4 bits to 18.

means Stability over temperature, a guaranteed Harris design criterion.

is for Test instrumentation. The perfect place to put our A-to-D and D-to-A converters to the test.

is for Unique like our HI-7153. It's an 8-channel MUX, a track-and-hold amp, and a 10-bit ADC in one.

is for the Value we give you through superior price/performance.

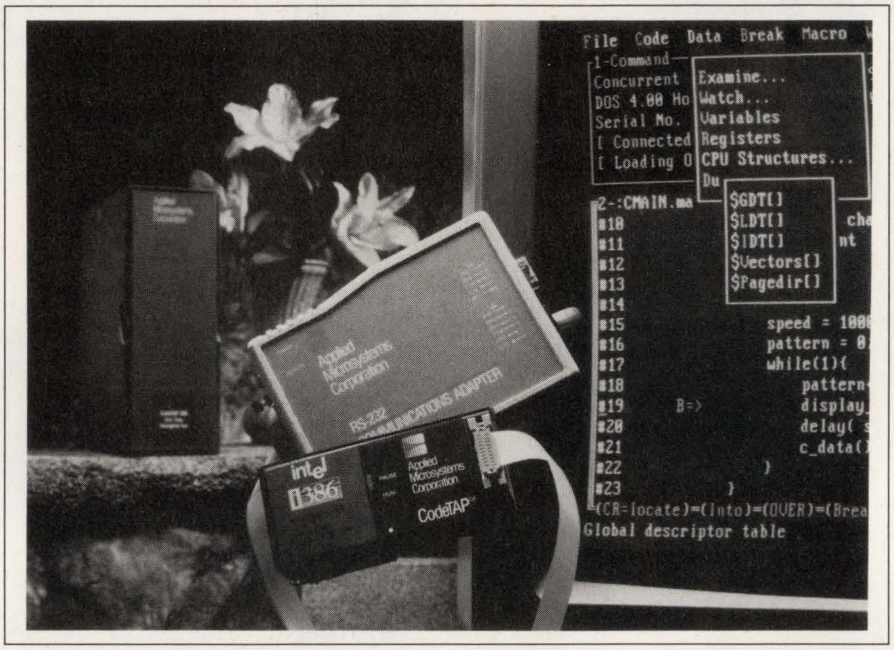
Harris covers A to D

For everything you need in data conversion, there are only six little letters to remember. H•A•R•R•I•S.

No wonder. Because Harris is the leader in high-precision and high-speed data acquisition, with the industry's broadest line of A-to-D and D-to-A converters. Plus all the

Development Tool For i386SX

- *Monitors and controls target without using its memory*
- *Includes target probe, RS-232C adapter, and debugger*



The Codetap 386 SX tool develops embedded systems based on the i386SX μP. The product demonstrates many of the capabilities of an in-circuit emulator but it costs much less. Without modifying your code in any way or using any target memory or I/O resources, the tool allows you to monitor and control the execution of a program running at the processor's full clock speed in your target system. The tool supports the μP's protected and real modes. The hardware consists of a target probe and an RS-232C adapter. The software includes a windowed source-level debugger called Validate/SoftscopeIII and Pharlap's assembler/linker/locator. From $5995.

Applied Microsystems Inc, Box 97002, Redmond, WA 98073. Phone (206) 882-2000. **Circle No. 358**

Arbitrary Waveform And Function Generator

- *Has 20-MHz sample clock*
- *Generates 16 standard waveforms mathematically*

The 2202A generator recreates waveforms that you define it and mathematically synthesizes 16 functions, including sine, square, triangular, ramp, and sin(x)/x waves. The generator's sample clock runs from 0.1 Hz to 20 MHz. A 12-bit DAC converts stored or computed data to waveforms. A step attenuator provides open-circuit output ranges of 100 mV, 1V, and 10V; separate gain-vernier and output-offset DACs maintain full resolution at low amplitudes and with output offset. The waveform memory stores 32k samples, but the computed waveforms use none of this memory. A sequence-generator option lets you link and loop on segments to define very long waveforms. You can create and edit waveforms using only a general-purpose scope and a mouse. $2495; sequence option, $895.

Pragmatic Instruments Inc, 7313 Carroll Rd, San Diego, CA 92121. Phone (619) 271-6770. FAX (619) 271-9567. **Circle No. 359**

IEEE-488 Bus Extender

- *Increases allowable bus length to 300m*
- *Transfers 900k bytes/sec*

The GPIB-130 IEEE-488 bus extender is about the size of a cigarette pack and uses 5V dc power. The units work in pairs to extend the bus beyond its normal 20m maximum length; the extenders permit 300m-long buses. In buffered mode, the extenders transfer data at 900k bytes/sec over cables of any length. In the unbuffered mode (handshake accompanies each byte), the maximum rate decreases as you increase the cable length. The transfer rate is 140k bytes/sec at 300m. The devices support two parallel-polling modes. The immediate mode returns a valid response in the required time if the cable length is 100m or less. The stored mode returns the prior response and requires that your program issue two poll commands. $995.

National Instruments Inc, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. TLX 756737. **Circle No. 360**

M and DM SERIES
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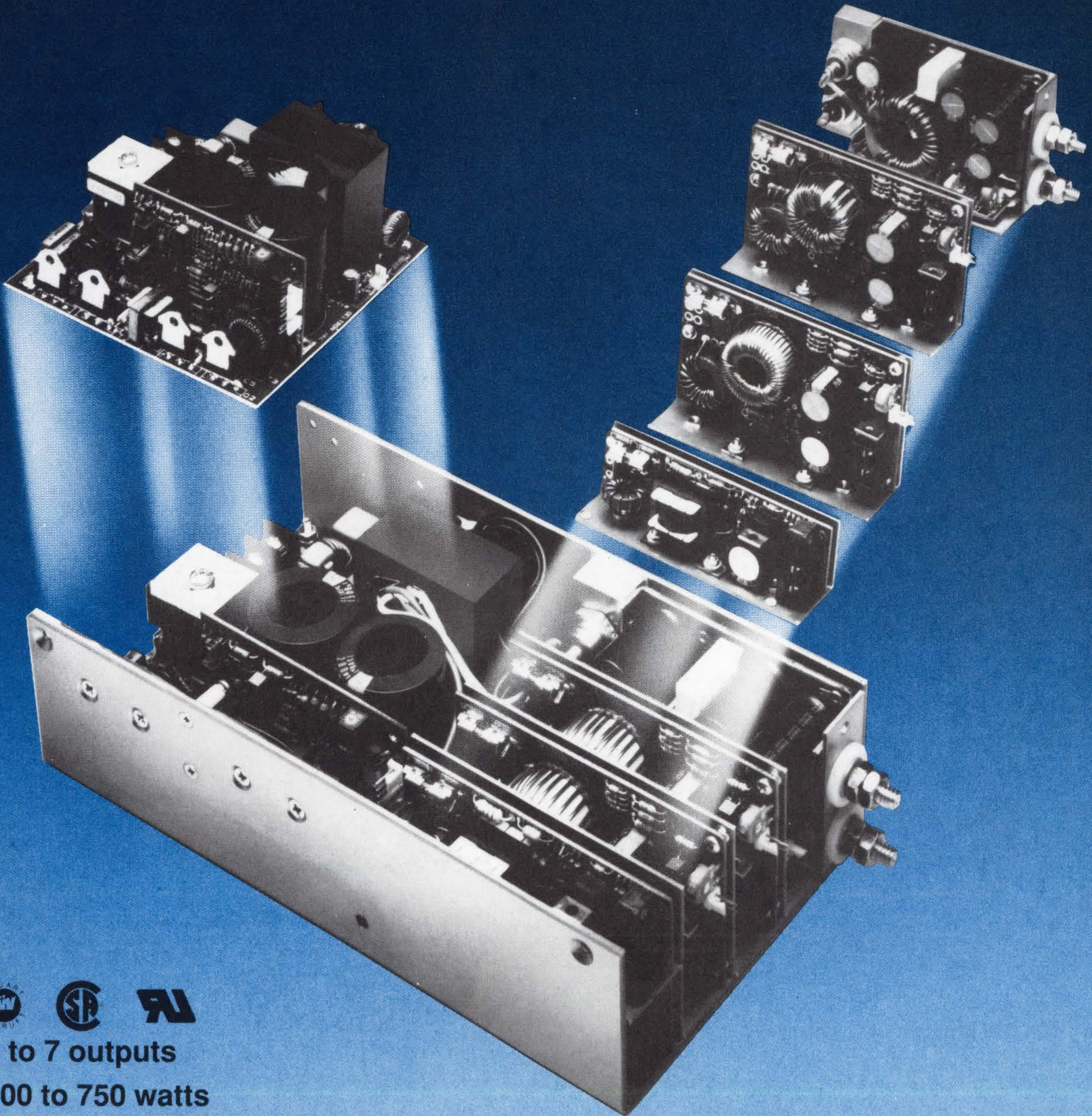

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- 400 to 750 watts
- 2 weeks delivery
- No engineering charge
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POWER PRODUCTS

M-102 2/91

M/DM SERIES SELECTION CHARTS

Input Module Power Codes	
A	400W
B	500W
C	600W
D	750W

Output Module Types	
J	1/2 Height
K	Full Height
L	Double Full
R	Small Main
M	Main
N	Super Main

M Type Main Module Ratings		
Power Rating	Current Multiplier	
	Single	Multiple
400W	0.8	0.6
500W	1.0	0.8
600W	1.2	1.0
750W	N/A	1.2

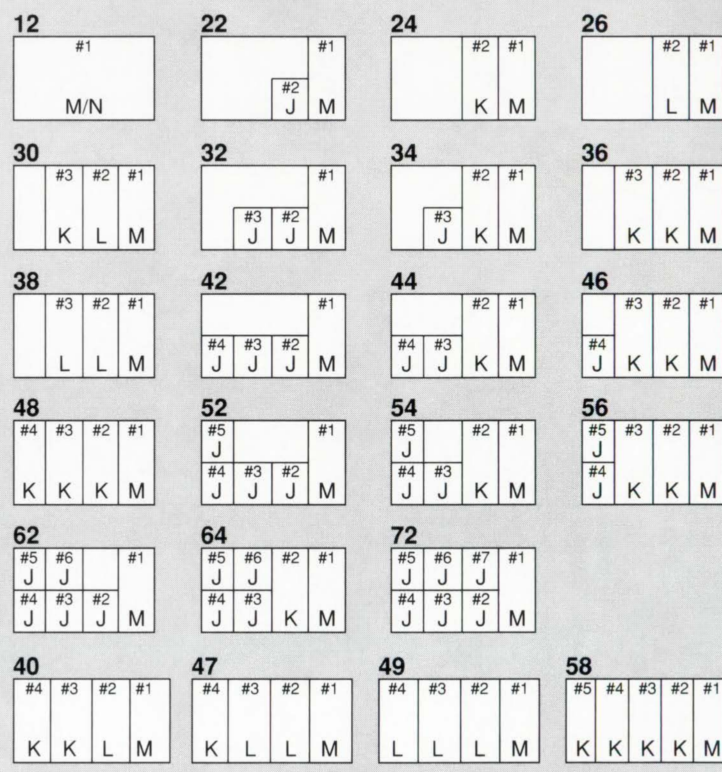
Options	
Option Code	Function
01	Power Fail Monitor
02	Auto Ranger
04	Pilot Bias
08	Active Surge Limit
16	Redundant
32	Cover
64	Fan Cover

Options 02, 04, 08 mutually exclusive.

Output Modules							
Output		Type					
Code	Volts	J Amps	K Amps	L Amps	R Amps	M Amps	N Amps
0	2	10	20	30	40	100	150
1	3.3	10	20	30	40	100	150
2	5	10	20	30	40	100	150
3	12	6	12	24	17	42	62
4	15	5	10	20	13	33	50
5	18	4	8	16	11	28	42
6	24	3	6	12	9	21	31
7	28	2.5	5	10	7	18	27
8	36	2	4	8	6	14	21
9	48	1.5	3	6	4	10	16
A	2.2	10	20	30	40	100	150
B	2.4	10	20	30	40	100	150
C	2.7	10	20	30	40	100	150
D	3	10	20	30	40	100	150
E	3.6	10	20	30	40	100	150
F	4	10	20	30	40	100	150
G	4.5	10	20	30	40	100	150
H	5.7	10	20	30	36	90	135
J	6.3	10	20	30	32	80	120
K	7	9	18	30	28	70	105
L	8	8	16	30	25	62	93
M	9	8	15	30	22	56	84
N	10	7	14	30	20	50	75
P	11	7	13	27	18	45	68
Q	13.5	6	11	22	15	37	56
R	17	5	9	18	12	30	45
S	19	4	8	16	11	26	39
T	21	4	7	14	10	24	36
U	23	4	7	13	9	22	33
V	26	3	6	12	8	19	29
W	29	3	5	10	7	17	26
X	32	2	5	9	6	16	24
Y	40	2	4	8	5	13	20
Z	44	2	4	7	5	12	18

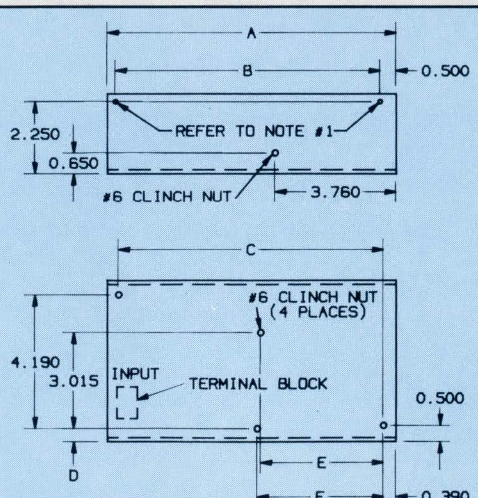
For multiple output modules of a given type, voltages are arranged in ascending order by magnitude in the same sense as the output number sequence. Shaded ratings are stock, others available on special order.

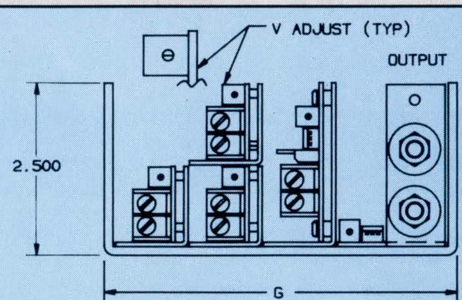
Output Configurations
Output #1 can be Type K, L, R, M. For singles, M or N only.



The boxes above are diagramatic representations of the power supplies as viewed from the output end. The two digit numbers above the boxes are the configuration codes. Configurations 40,47, 49 and 58 – Power Code D, Case 3. Configurations 26, 30 and 38 – Power Codes C and D, Case 2. Remaining configurations – Power Codes A, B, C and D, Cases 1 and 2.

M/DM SERIES DIMENSIONS





(1) With cover (#6-32), W/O cover (.150 dia.)
(2) W/fan cover unit height (4.100)
(3) Terminal Blocks (#6-32)
(4) Studs (1/4-20)

	Case 1	Case 2	Case 3
	400/500 W	600/750 W	600/750 W
A	9.000	9.630	9.630
B	8.25	8.880	8.880
C	8.260	8.890	8.890
D	.410	.425	1.725
E	3.820	4.450	4.450
F	3.930	4.560	4.560
G	5.050	5.200	6.500

DESCRIPTION

Moduflex switchers form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. These subunits and assembly hardware are pre-approved by safety agencies so that certifications can automatically apply to custom models. Additional advantages include first piece delivery within two weeks and the elimination of engineering costs for qualified "OEM" requirements using stock modules.

The M and DM Series offers the highest power density available in the industry, delivering 6 watts per cubic inch at an ambient temperature of 50°C. The design features "State of the Art" topology, a meticulous thermal structure and the use of high efficiency circuits and components to attain the desired power density.

The modular system concept reduces manufacturing to simple submodules, capable of high volume production with a superior quality level.

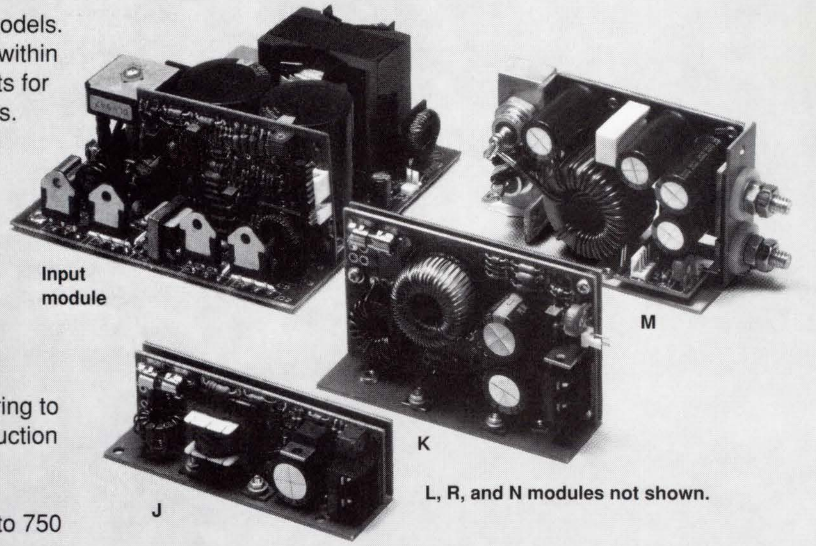
M Series are available in power ratings from 400 to 750 watts with only a slight size increase. This power versatility permits system expansion without the need for extra power supply space. DM Series available in power ratings of 400 or 600 watts.

FEATURES

- TUV, UL, CSA.
- 6 watts per cubic inch.
- 400-750 watts output.
- 120 kilohertz MOSFET design.
- Current mode control.
- All outputs:
  - *Adjustable*
  - *Fully regulated*
  - *Floating*
  - *Overload and short circuit proof*
  - *Overvoltage protected*
- Standard features include:
  - *System inhibit*
  - *Load proportional DC fan output*
- Options include:
  - *Auto ranger for continuous input operation*
  - *Power fail monitor*
  - *Independent pilot bias*
  - *Cover*
  - *Fan cover*
  - *Active surge limit*
  - *Redundant operation*

MODEL SELECTION

Input modules are available in ratings of 400, 500, 600, and 750 watts with corresponding code letters A through D. See Power Codes chart opposite.



L, R, and N modules not shown.

Output modules are available in six types J, K, L, R, M and N in nominal power outputs of 75, 150, 300, 200, 500 and 750 watts respectively. Type M or main output modules are variable power rated depending upon the power level of the input module. This is reflected in the rating table opposite which shows the corresponding multiplier applicable to the output current ratings of the M module as a function of the power rating of the input module. For example, a 750 watt multiple will have its M type module configured to produce 600 watts of output. The ratings of output modules are given in the table of output types. Ratings in shaded areas are stocked for fast delivery.

HOW TO ORDER

To form the proper model number defining a custom requirement, select the letter M to designate the series, then choose the desired configuration of output modules and list the configuration code. Insert the power code letter for the power level and follow with the output code numbers or letters for each specific output. Enter a dash and from the option table insert the sum of the option codes. Add a suffix letter K, L or R to designate the substitution of one of these module types for the type normally specified for output #1. See example below. For DC input add a prefix D to the model number.

MODUFLEX 500W QUAD SWITCHER

D M 44 B 2 3 3 6 - YY X

- D — DC Input
- M — Series
- 44 — Configuration
- B — Power Code
- 2 — Output #1 Code
- 3 — Output #2 Code
- 3 — Output #3 Code
- 6 — Output #4 Code
- YY — Sum of Option Codes
- X — Output #1 Variant

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz. Strappable.
40-60 VDC for DM Series.

INPUT SURGE
Less than 68 Amps peak from cold start.

HOLDUP TIME
20 milliseconds from loss of nominal AC power.
3 milliseconds for DM Series.

OUTPUTS
See model selection table.

ADJUSTABILITY
±5% trim adjustment.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries.

REMOTE SENSING
On all outputs except type J modules.

RIPPLE & NOISE
1% or 100mV pk-pk, 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS cooling air directed over the units for full rating. Two test locations on chassis rated for max. temperature of 90°C.

TEMPERATURE COEFFICIENT
±0.02%/°C.

EFFICIENCY
80% typical.

SAFETY
Units meet UL 1950, CSA 22.2 No. 220, CSA bulletin 1402C, IEC 950, VDE 0804, VDE 0806, VDE 0805 (proposed). Certifications in process.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC 60Hz. input. Not applicable to DM Series.

EMISSIONS
Units meet FCC 20780 Part 15 Class A and VDE 0871/6.78 Class A for conducted emissions. Compliance with Class B limits by use of additional external filter. DM Series also meet Bellcore TR-TSY-000515.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%.
R, M and N modules – 200 microseconds.
J, K, and L modules – 500 microseconds.

UNDERVOLTAGE
Protects against damage for undervoltage operation.

OVERVOLTAGE PROTECTION
Standard on all outputs.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Auxiliaries have additional backup fuse protection.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

SOFT START
Units have soft start feature to protect critical components.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided.

SHOCK
MIL-STD 810-D Method 516.3, Procedure III.

VIBRATION
MIL-STD 810-D Method 514.3, Category 1, Procedure I.

MECHANICAL
400 W/500 W – 2.5" H x 5.05" W x 9.00" L. Case 1.
600 W/750 W – 2.5" H x 5.20" W x 9.63" L. Case 2.
600 W/750 W – 2.5" H x 6.5" W x 9.63" L. Case 3.

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME compatible power fail signal providing 4 milliseconds warning before main output drops by 5% after an input failure.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not applicable to DM Series.

PILOT BIAS
Optional circuit provides SELV output of 5 volts at 75 milliamps independent of the main power converter. Output isolation compliant to safety specifications referenced above.

ACTIVE SURGE LIMIT
Limits input surge to less than 18 Amps, and provides rapid reset.

COVER
Optional flat cover recommended when customer supplied fan cooling is directed through the length of the unit.

FAN COVER
Optional cover with brushless DC fan which provides the required air flow for full rating of Moduflex power supplies.

REDUNDANT
This option is specified when two or more like M units are to be used in an N + 1 redundant hookup using external isolating diodes. Cable assemblies are provided that interconnect the remote sensing leads and the single redundant wire which provides current sharing. This option not available for M units containing J modules.

POWER FACTOR CORRECTION
Refer to Bulletin FM-101 for M Series units with 0.99 power factor and harmonic currents compliant to IEC 555-2.

Deltron inc.
290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215/699-9261 • FAX: 215/699-2310

Int'l. Units: Delaire • Sallynoggin Road, Dun Laoghaire, Co. Dublin, Ireland. Tel: (01) 851411 Prefixes – from U.K. – (0001)–Int'l. + 353–(1) Telex: 30442DEL EI
Delinc • Padre Mier y Dr. Mina, Reynosa, Tamps., Mexico 08866. Tel.: (892) 38723 Prefix – from USA – (01152) FAX (892) 38776

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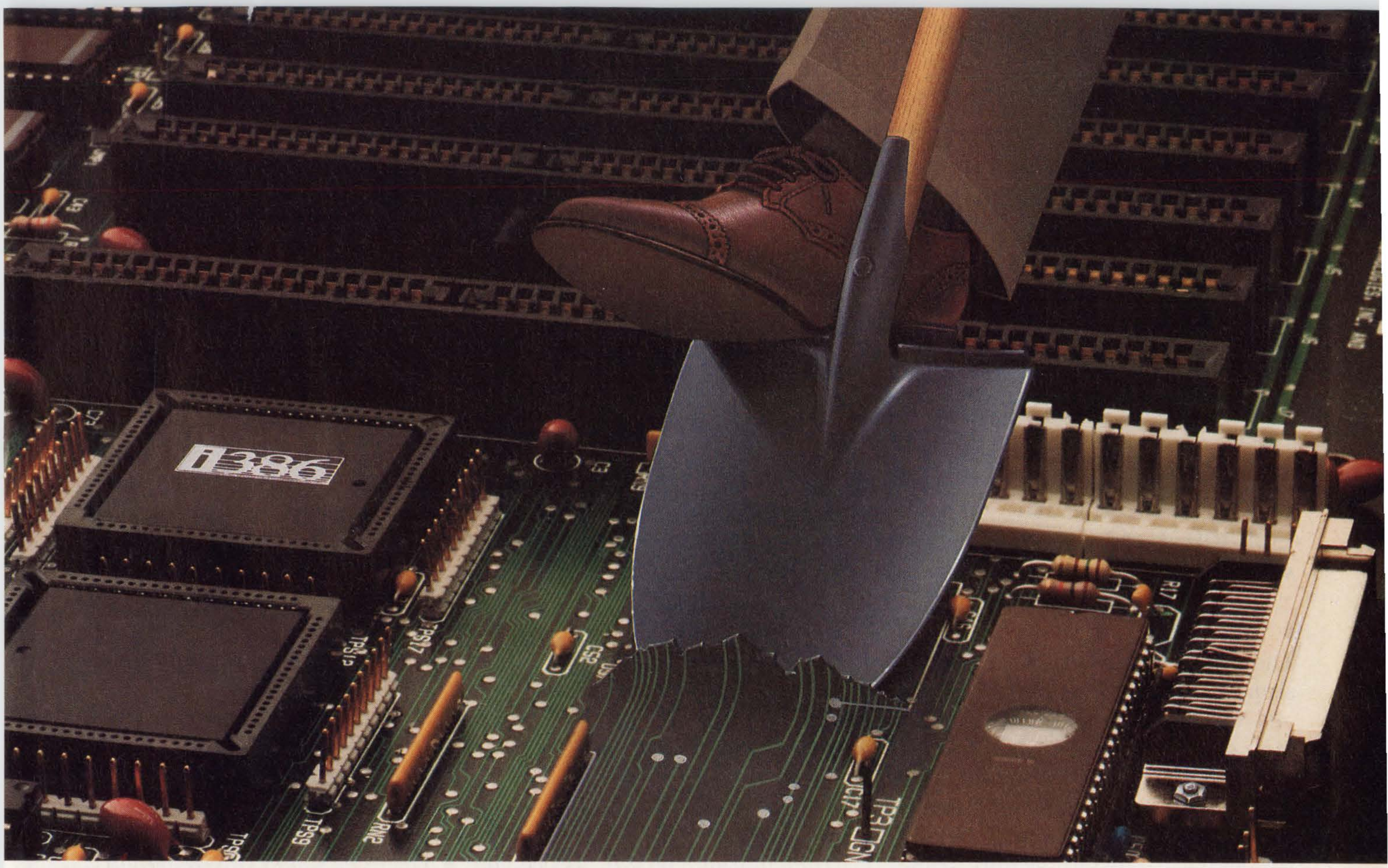

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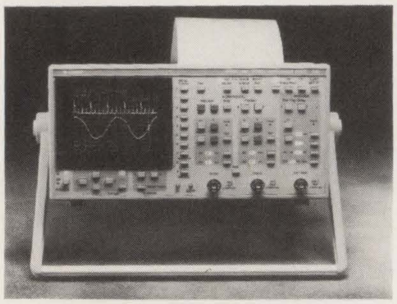
So step on it. And call us at **1-800-227-1817, ext. 52** today. We think you're going to really dig it.

adaptec

When you're serious about SCSI.

CIRCLE NO. 126



100-MHz-Bandwidth Portable DSO

- *Weighs 14.3 lbs and measures 5.3×15.3×10.9 in.*
- *Takes 200M samples/sec*

The 465 portable 2-channel oscilloscope measures 5.3×15.3×10.9 in. and weighs 14.3 lbs. It offers 100-MHz bandwidth and captures transients at 200M samples/sec simultaneously on both channels. Some scopes that have an equal repetitive-signal bandwidth acquire transient data much more slowly and therefore have a much lower single-shot bandwidth. Resolution is nominally 8 bits. Display memory is 512 bytes/channel. Nonvolatile memories store setups and waveforms. An optional integral 4-color pen plotter provides permanent records of anything the screen can display. \$3490; plotter, \$500.

Gould Inc, 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7263. FAX (216) 328-7400. **Circle No. 361**

Digital-Test Module For VXIbus

- *Provides 48 TTL inputs and 48 TTL outputs*
- *Allows you to create 576-channel systems*

The 6451 digital test module is a C-size VXIbus (VME extensions for instrumentation) plug-in device; it provides 48 bidirectional TTL I/O channels that operate to 20 MHz. You can configure the I/O channels to provide 48 stimuli and to monitor 48 responses. You can also use groups of channels exclusively for inputs or outputs. You can synchronize several modules to create systems with as many as 576 channels. Timing skew between channels in one module is ±5 nsec. Between channels in synchronized modules, skew is ±7.5 nsec. \$14,995. Delivery, 16 weeks ARO.

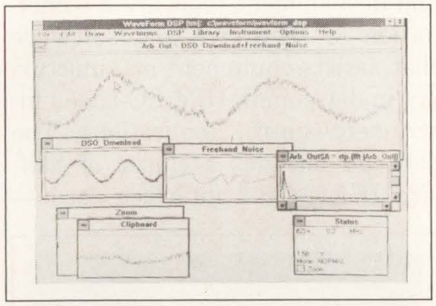
Racal-Dana Instruments Inc, 4 Goodyear St, Irvine, CA 92718. Phone (800) 722-3262. FAX (714) 859-2505. **Circle No. 362**

Arbitrary Waveform Software

- *Lets you capture, create, and edit waveforms*
- *Operates under MS-Windows 3.0*

Waveform DSP is an IBM PC-based

software tool kit that lets you capture, create, edit, and analyze waveforms, and then upload them to an arbitrary waveform generator. The software runs under MS-Windows 3.0. You can create waveforms by expressing them as equa-



tions, drawing them, downloading them from a digital oscilloscope, or calling them from a library. You can view and modify the waveforms in either the time or frequency domains. If you change a waveform in the frequency domain, the software will, on command, convert it to its time-domain equivalent. Cubic-spline curve fitting lets you define complete waveforms by specifying their values at a few discrete points. $895. Delivery, four to six weeks ARO.

Wavetek San Diego Inc, Box 85265, San Diego, CA 92138. Phone (800) 874-4835; (619) 279-2200.

Circle No. 363

TTL And CMOS IC Tester

- *Includes library of 600 14- and 28-pin TTL and CMOS ICs*
- *Diagnostic messages appear on 2-line display*

Model PL 5010 tests TTL and CMOS digital ICs whether the devices are connected in a circuit or not. You can operate and program the instrument in a stand-alone mode. The tester stores a library that lists descriptions of more than

600 ICs—90% of the most commonly used 14- and 28-pin devices. The instrument vendor updates the library as IC vendors introduce new parts. Optional PC-based software lets you develop programs for custom ICs. The tester sports a 2-line × 20-character vacuum-fluorescent display on which appear operator prompts and explanations of why devices failed. A loop feature tests parts for extended periods to find intermittent failures. The

tester can automatically identify the type of device you have connected. $4500.

Maxtec International Corp, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448.

Circle No. 364

Arbitrary Waveform Generator For ISA-16 Bus

- *Has two channels; each converts at 50M points/sec*
- *Has 0.01%-resolution, 0.001%-error frequency synthesizer*

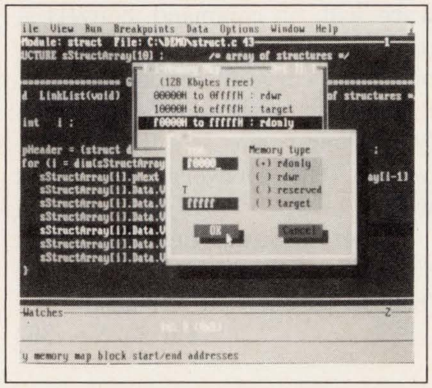
The AWG502 plug-in device for the 16-bit ISA bus contains a 2-channel arbitrary-waveform generator with 64k words of waveform memory/channel. It uses 12-bit DACs to convert stored data into waveforms and has additional 12-bit DACs for offset and 8-bit DACs to adjust the output amplitude. Full-scale output is ±8V into an open circuit. The maximum data rate is 50M points/sec per channel. A synthesizer lets you set the output frequency in 0.01% steps, each accurate to 0.001%. Under software control, you can select among ten 3- to 5-pole transitional filters with cutoff frequencies from 10 kHz to 40 MHz. Multiple-segment looping lets you create very long waveforms. $3500.

Signatec Inc, 357 N Sheridan St, Suite 119, Corona, CA 91270. Phone (714) 734-3001. FAX (714) 734-4356. **Circle No. 365**

80C186/80C188 Emulator

- *Permits real-time emulation at 16 MHz*
- *Hosted by IBM PC/ATs*

The Zaxpak 2000 is an IBM PC/AT-hosted, in-circuit emulator for the 80C186 and 80C188 μPs operating at clock speeds to 16 MHz. The emulator, which communicates with its host via a parallel interface and supports the 80C187 coprocessor, has an 8k-frame trace buffer and 256k bytes of emulation memory (expandable to 1M byte). The Paradigm Debug/ERX source-level debugging interface is a customized version of Borland's Turbo Debugger that supports hardware breakpoints, real-time trace, and peripheral-register views. It works with C, C++, and PL/M-86 compilers from Borland, Intel, and Microsoft. Zaxpak 2000, $14,785; with symbolic-debug software only, $12,990.



Zax Corp, 2572 White Rd, Irvine, CA 92714. Phone (800) 421-0982; in CA, (800) 233-9817; (714) 474-1170. **Circle No. 366**

VXIbus-Based Board Tester

- *Operates to 100 MHz*
- *Allows integration of IEEE-488 instruments*

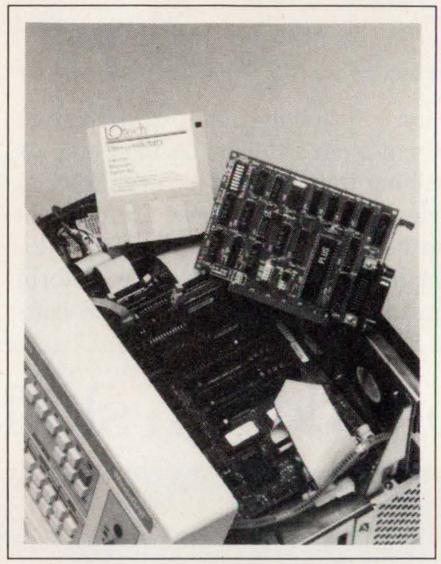
The HP 307x pc-board test systems are based on the VXIbus (VME extensions for instrumentation). The system is a combinational tester—it performs both functional and in-circuit testing. Using an external VXI chassis, the system can test at 100 MHz; that is, it can apply patterns to a unit under test and compare the unit's responses with the desired ones at this rate. The test head lets you construct fixtures with a minimum of custom work. The system accommodates four VXI backplanes and can use additional ones that you mount externally. It also lets you connect and mount IEEE-488 instruments. From $221,500. Available, November 1991.

Hewlett-Packard Co, 19319 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 367**

IEEE-488.2 Interfaces And Development Tools

- *Libraries of functions link to C programs*
- *Hardware options for 8- and 16-bit ISA buses*

The Personal488/OEM-P interfaces and development tools are a combination of hardware and software that assists equipment manufacturers in developing IBM PC-based instrument-control applications. The package includes a choice of half-size IEEE-488.2 interface cards—



one for the 8-bit ISA bus and one for the 16-bit version of the bus. In addition, there are libraries of IEEE-488.2 functions that you can link to programs you write in Microsoft C. The hardware and software handle both DMA and interrupt-driven I/O transfers. The DMA transfer rate is 1M byte/sec, the maximum speed of the IEEE-488 bus. An addition to the software provides drivers that control RS-232C-based instruments. Package with 8-bit board, $795; package with 16-bit board, $895; RS-232C drivers, $100; 8-bit board, $195; 16-bit board, $295 (100).

IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. TWX 650-282-0864.

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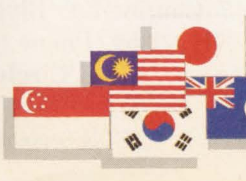

Asia/Pacific Sales Headquarters
35th Floor, Shun Tak Centre
200 Cannaught Road
Central Hong Kong
011-85-2-859-6044

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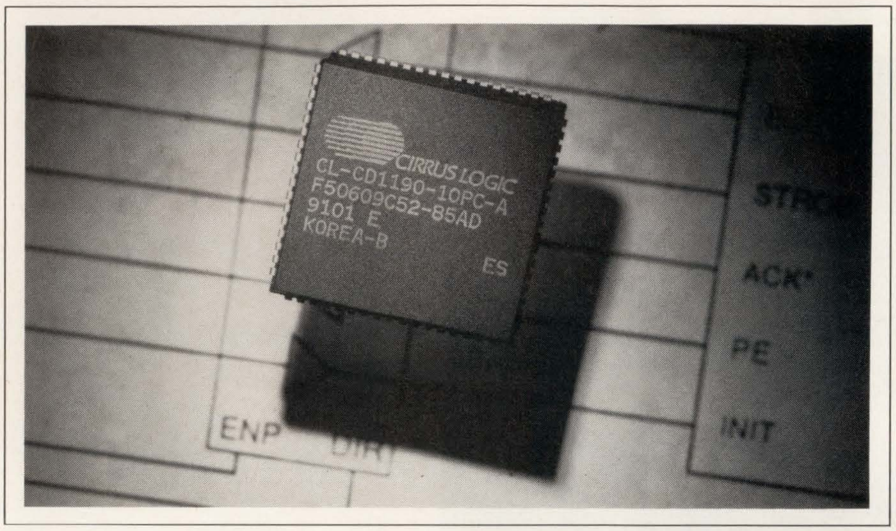


Printer/Scanner Interface Controller

- *Used in PC-to-printer channel*
- *Transfers data at rates to 250k-bytes/sec*

Compared with the current standard, the CL-CD1190 printer/scanner interface controller more than doubles the data-transfer rates of PCs and workstations to printers. The controller provides an industry-standard parallel data-transfer channel that can handle data rates to 250k bytes/sec for Centronics-and Dataproducts-compatible printers and scanners. Compared to the typical byte-at-a-time interface, the 128-byte FIFO buffer offered by the controller effectively eliminates the need for the CPU of the host computer to manipulate "handshake" bits or control the data transfer. In a typical 80386-based PC, the controller reduces CPU loading from 80 to 8%, according to the vendor. CL-CD1190 in a 68-pin plastic leaded chip carrier, $21.50 (10,000/year).

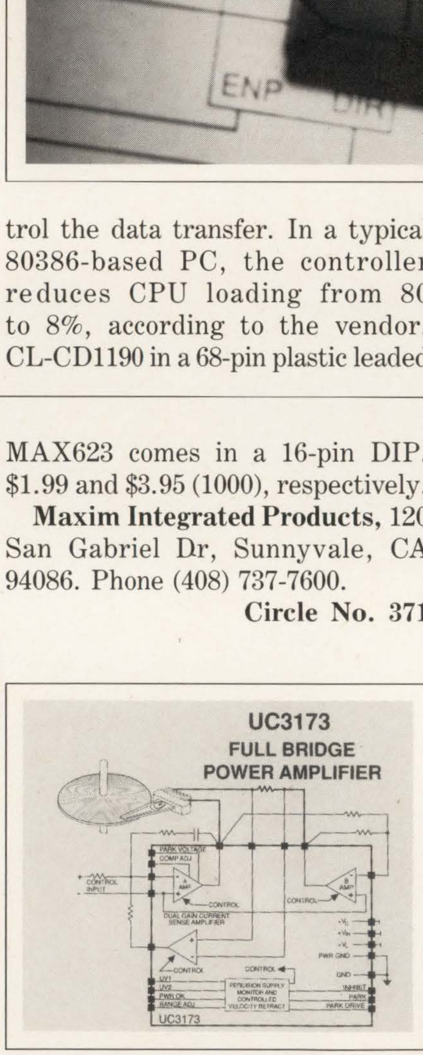
Cirrus Logic, 1463 Centre Pointe Dr, Milpitas, CA 95035. Phone (408) 945-8300. FAX (408) 263-5682. TLX 171918. **Circle No. 370**

High-Side Power Supplies

- *Boost V_{in} by 11V*
- *Drive n-channel MOSFETs*

The MAX622 and MAX623 are regulated charge-pump converters that provide the required voltage to circuits that drive n-channel MOSFETS in high- and low-side switching applications. The converters generate a regulated output that is 11V greater than the input supply. This regulated output provides the higher gate voltage required by low-cost n-channel MOSFET switches and eliminates the need for more expensive p-channel MOSFETs or pnp transistors. A logic-level, power-ready output indicates when the high-side voltage reaches the proper level. The MAX622 requires three low-cost external capacitors; the MAX 623 has these capacitors built in. Both devices operate over an input-supply range of 3.5 to 16.5V and have a typical quiescent current of 70 µA. The MAX622 comes in 8-pin DIP and small-outline packages; the MAX623 comes in a 16-pin DIP. $1.99 and $3.95 (1000), respectively.

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. **Circle No. 371**

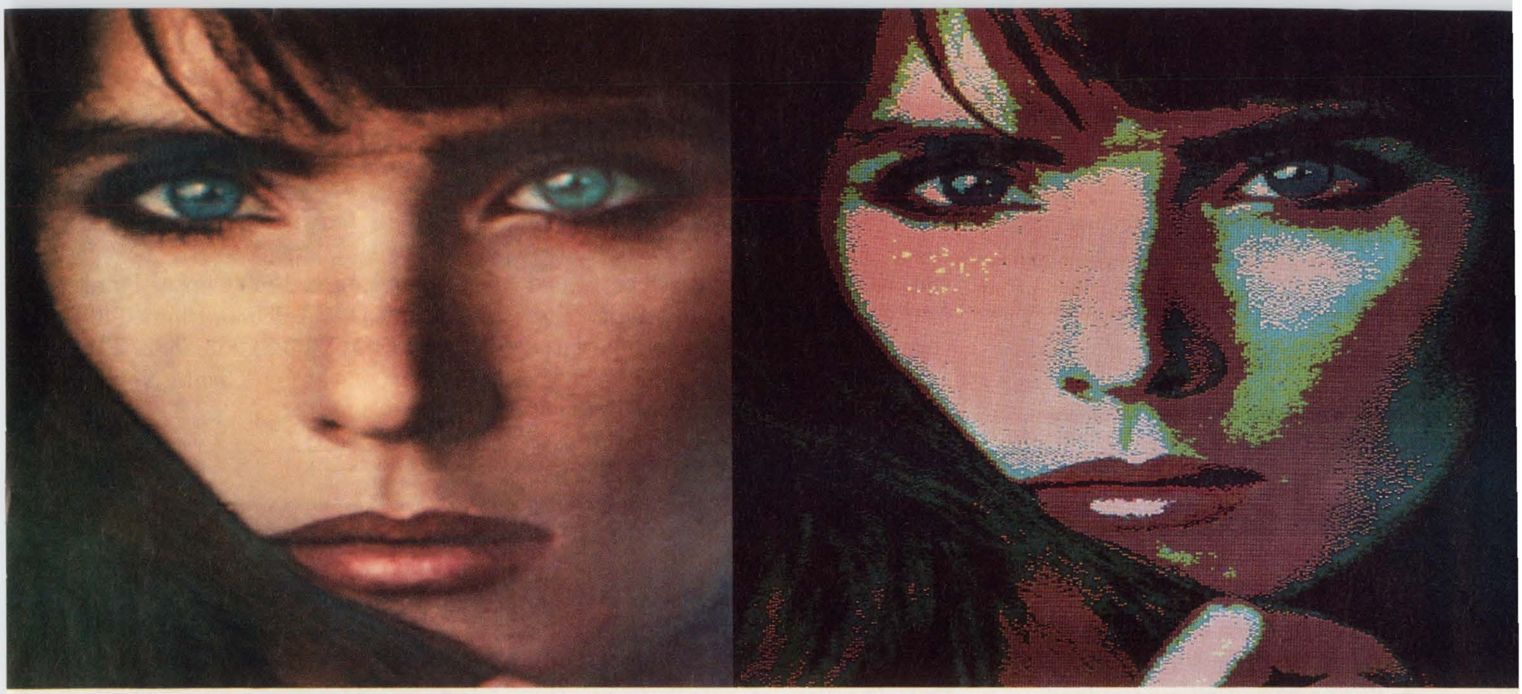


Voice-Coil Driver

- *Provides multiple functions*
- *Includes a full-bridge amplifier*

Designed for head-positioning servo applications in hard-disk drives, the UC3173 integrates several functions. A current-sense amplifier monitors load current. A voltage comparator can monitor two independent supply voltages and activate the built-in head-parking function when either voltage is below a minimum value. The park function, which can work with operating voltages as low as 1.2V, also allows the application of a programmable retract voltage to limit the maximum head velocity. A separate low-side-drive pin permits insertion of a series impedance to control the maximum retract current. The full-bridge power stage is rated for a continuous output of 0.45A and features a low saturation voltage to ensure full drive at low supply voltages. The output stages also feature current-limiting and thermal-shutdown protection. The device operates from either a 5V or a 12V supply. UC3173 in a 24-pin SOIC, $3.55; in a 28-pin plastic leaded chip carrier, $3.80 (1000).

Unitrode Integrated Circuits Corp, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410. **Circle No. 372**



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With Cirrus Logic LCD VGA controllers, your answer is yes. Which is why we're the leading supplier of display controller chips in the laptop and notebook market.

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Our monochrome solutions give you displays that *PC Magazine* called "the stars of our VGA color-mapping tests"* with up to 64 shades of gray. And with a lower dot clock rate, your power consumption is lower than other solutions for longer battery operation.

Cirrus Logic LCD controllers are fully compatible with the popular PC video standards and will work with LCD, plasma, or electroluminescent displays.

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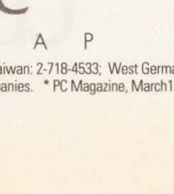
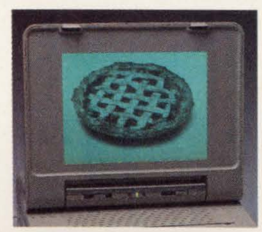
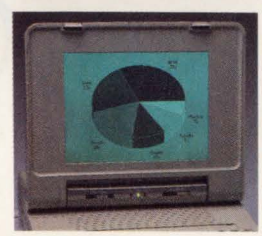
Design a more competitive product. One that looks better — and makes you look better. That lasts longer on a battery. Use the display solutions from a proven technology leader in laptop and motherboard VGA: LCD controller chips from Cirrus Logic.

Get the picture. Get more information on LCD controllers.
Call 1-800-952-6300, ask for dept. LL24



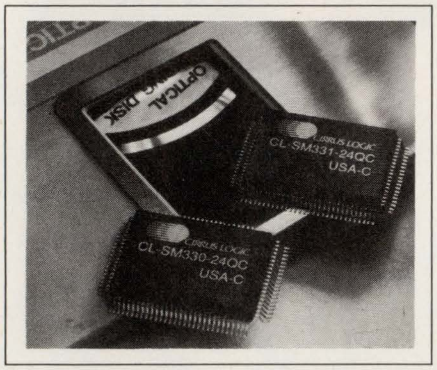




Cirrus Logic monochrome LCD controllers will also make everything from realistic scanned images to business charts look tastier.

CIRRUS LOGIC

C L O S I N G T H E G A P

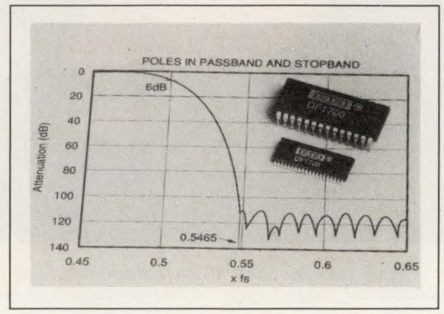


Dual-Chip Controller For Optical Disk Drives

- *Suits $3^1/_2$- and $5^1/_4$-in. drives*
- *Supports industry standards*

The CL-SM330/331 2-chip set is designed for embedded controller applications in magneto-optical disk drives. The CL-SM330ENDEC/ECC chip and the CL-SM331 SCSI disk controller support established industry standards for $3^1/_2$- and $5^1/_4$-in. drives. These standards include ANSI and ISO formats using the Continuous Composite Servo (CCS) standard for rewritable, partial ROM, and Write Once, Read Many (WORM) applications. The chip set can operate in both initiator and target modes and complies with the SCSI-2 standard, which allows bus data transfer rates to 3M bytes/sec (asynchronous) and 5M bytes/sec (synchronous), and disk NRZ data-transfer rates to 24 MHz. The SM330 implements logic for the encoder/decoder (ENDEC), formatter, and error detection and correction functions. This chip, which controls the flow of data between the controller and the disk read/write head, also performs on-the-fly hardware error correction in conjunction with the SM331. The SM331 controls the flow of data between the host and the SM330, providing a SCSI link between the system bus and the optical drive. The CL-SM330 and CL-SM331 come in 100-lead quad flat packs. \$85 per set (sample qty).

Cirrus Logic, 1463 Centre Pointe Dr, Milpitas, CA 95035. Phone (408) 945-8300. FAX (408) 263-5682. TLX 171918. **Circle No. 373**



Dual-Channel Digital Audio Filter

- *Provides 8× oversampling*
- *Accepts 16-bit input data*

The DF1700 is a dual-channel CMOS digital filter that can provide 8× oversampling to audio DACs.

The filter accepts 16-bit input data and is user-selectable for 16-, 18-, or 20-bit output data. The output of the first FIR filter is oversampled 2× by the second FIR filter. This 4× oversampled data is again oversampled 2× by the third FIR filter, further separating the desired analog signal and the sampling frequency. The 8× oversampling lets the designer use a low-cost, low-order analog filter at the output of the DAC without concerns about fold-over noise. The DF700 is compatible with the company's PCM1700, PCM67 or a pair of PCM63 digital-audio D/A converters. The filter is also compatible with 8× oversampling DACs from other manufacturers. Other specifications include a passband ripple of less than 0.00005 dB and stopband attenuation greater than 110 dB. DF700, in a 28-pin DIP or a 40-pin SOIC, from $14.90 (100).

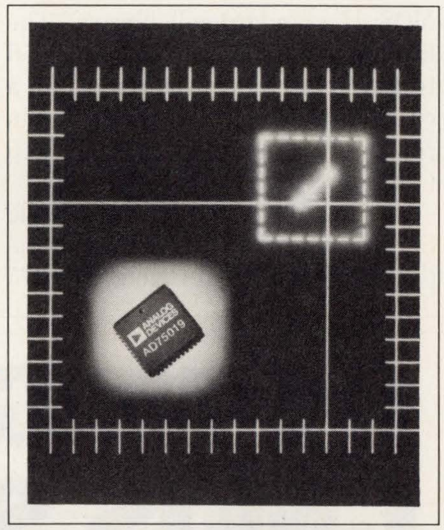
Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111.

Circle No. 374

Crosspoint-Switch Array

- *Contains 256 switches*
- *Handles analog signals to 26V p-p*

Containing 256 switches, the AD75019 connects any of 16 analog inputs to any of 16 outputs. In addition to being the industry's largest analog-switch array, the AD75019 can handle analog signals as large as 26V p-p, compared with only 12V p-p for other arrays, according to the vendor. The control interface features a TTL/CMOS-compatible 3-wire serial port and internal latches, which store the desired switch setup. Each switch has a typical on-resistance of 200Ω. The



crosspoint array can operate from ±5V or ±12V supplies or from a single supply or asymmetrical bipolar supplies. A serial output lets you cascade multiple devices. The array, which is a Linear System Macro (LSM) that you can customize, is cells from the company's Bi-

CIRCLE NO. 131

MOS II standard-cell library. The library offers the flexibility needed to adapt the basic architecture to a custom circuit. AD75019 in a 44-pin plastic leaded chip carrier, $15 (100).

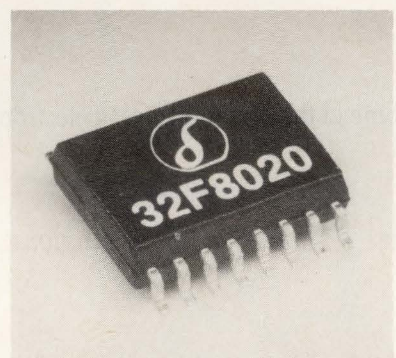
Analog Devices, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. **Circle No. 375**

10-Bit A/D Converters

- *Offer 20- and 40-MHz versions*
- *Include track-and-hold circuit*

Designed for high-sampling-rate applications, the 20-MHz SPT7810 and the 40-MHz SPT7814 10-bit A/D converters incorporate a track-and-hold circuit and a proprietary conversion technique, achieving their performance and eliminating the need for external components. Power consumption is 1.3W, a fraction of what is required for full-parallel or flash converters—according to the company. The monolithic devices feature an input capacitance of less than 5 pF and a S/N ratio of 57 dB at 1 MHz. Inputs and outputs for both devices are ECL compatible. The output-data format is straight binary. An over-range output signal indicates overflow conditions. Both devices operate from 5V and −5.2V supplies and accommodate an input range of ±2V. The SPT7810 and SPT7814 come in 28-pin ceramic DIPs. $79 and $109 (100), respectively.

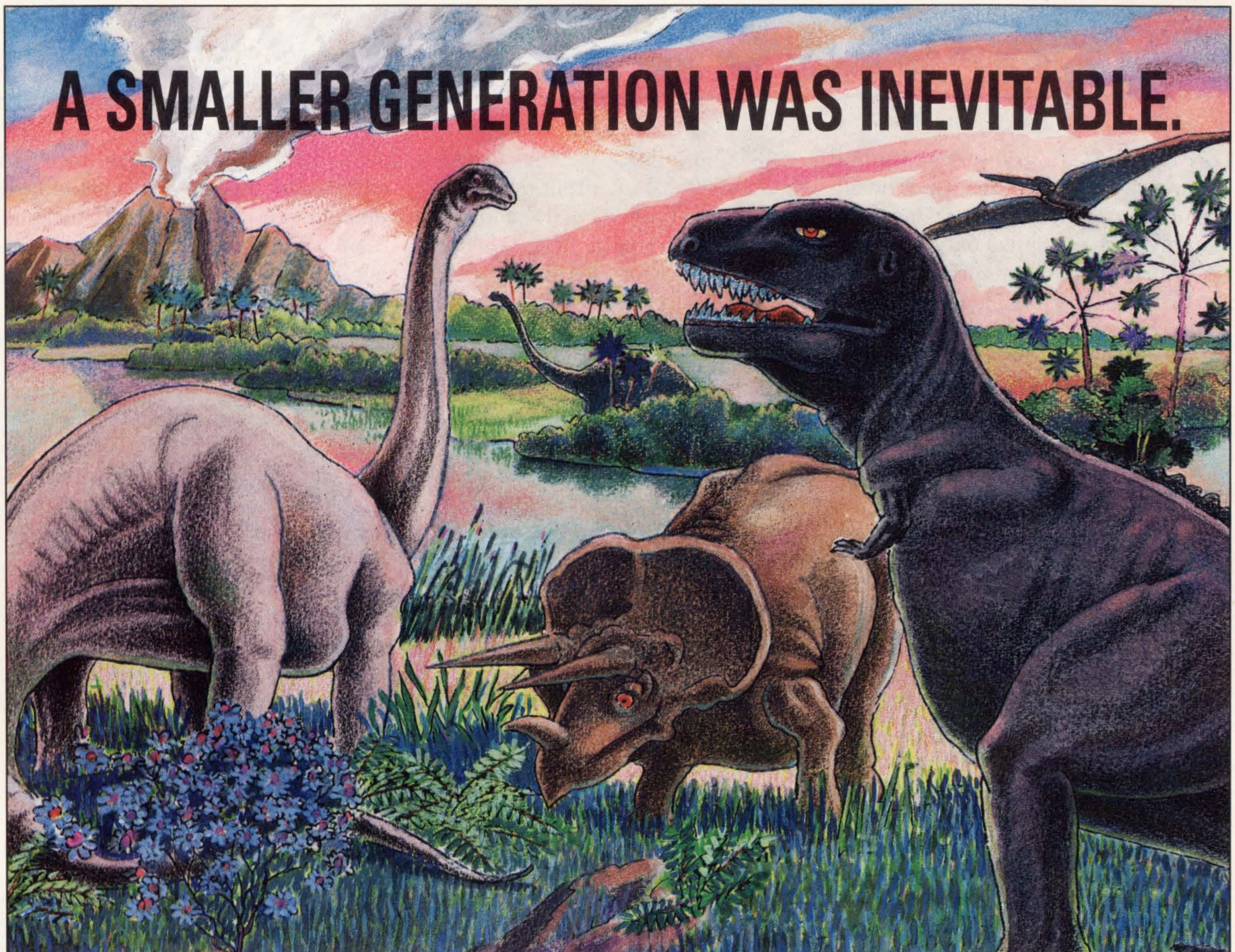
Signal Processing Technologies, 1510 Quail Lake Loop, Colorado Springs, CO 80906. Phone (719) 540-3999. FAX (719) 540-3970. **Circle No. 376**

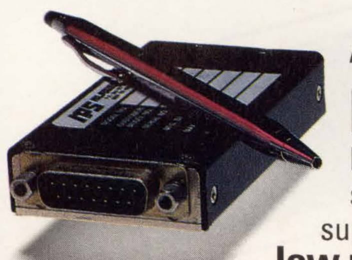


Lowpass Filter For 1.5- To 8-MHz Range

- *Includes pulse-slimming equalization*
- *For constant-density recording*

The SSI 32F8020, which operates over a frequency range of 1.5 to 8 MHz, features programmable pulse-slimming equalization that provides 0 to 9 dB of high-frequency boost for constant-density recording applications. The chip combines an electronically controlled 7-pole, low-pass filter with a single-pole, single-zero differentiator. Both outputs feature delay matching, which





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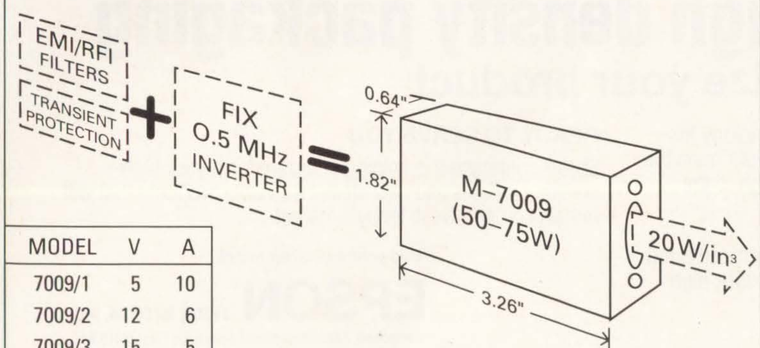
- Environmental conditions: MIL-STD-810C
- DC output: floating
- Line/load regulation: ±1%
- Ripple & noise: 30 mVp-p, typical
- Protections: current limiting, OVP
- Efficiency: 75%-82%
- EMI/RFI: MIL-STD 461/2
- Components: Hi-Rel industrial grade



MODEL	V	A
7009/1	5	10
7009/2	12	6
7009/3	15	5

MPS MILPOWER SOURCE, INC.

Call us for more information: Tel: 603-267-8865 FAX: 603-267-7258 Belknap Industrial Park, Rte. 106, Belmont NH 03220 USA

is unaffected by programmed equalization or bandwidth. The filter chip operates from a single 5V supply and consumes only 175 mW. A 5-mW idle mode provides long battery life in portable applications. The 32F8020, in 16-pin DIP and surface-mount packages, $5 (OEM).

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (800) 624-8999, ext 151; (714) 731-7110. FAX (714) 669-8814.

Circle No. 377

Current-Feedback Op Amp

- *High-speed performance*
- *Enhanced dc accuracy*

The LT1223 current-feedback amplifier uses thin-film resistors and wafer-level trims to obtain improved dc accuracy. Offset voltage is a maximum of 3 mV and input-bias current is 3 μA. The amplifier, which operates from ±4.5V to ±18V supplies, provides a minimum of 50 mA of output drive. Slew rate (1000V/μsec) and bandwidth (100 MHz) remain fairly constant over a range of closed-loop gains. Important in video applications, the differential gain and phase are 0.02% and 0.12°C, respectively, when operating with a gain of 2 and driving a 75Ω cable. The LT1223 is available in 8-pin plastic or ceramic DIPs and 8-pin small-outline packages. From $2.85 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; (408) 432-1900. **Circle No. 378**

Static RAM Modules

- *Have 2M-bit density*
- *Organized as 64k×32 and 256k×8 bits*

The MCM3264 and MCM8256 2M-bit static RAM (SRAM) modules come in a zig-zag in-line package (ZIP) and meet JEDEC-standard pinouts. The 3264 (64k×32-bit) and 8256 (256k×8-bit) modules are available in 15- and 20-nsec versions. The 3264 contains eight 64k×4-bit SRAMs and features a general output enable and a 1-byte enable for each of the four bytes. The 8256 contains eight 256k×1-bit SRAMs. Each nibble of the byte is accessed through a separate chip enable on the module. Both modules operate from a single 5V supply, have 3-state outputs, and are TTL compatible. The MCM3264 is packaged in a 64-lead ZIP; the MCM8256 comes in a 60-lead ZIP. For either module, 20-nsec versions, $195; 15-nsec versions, $275 (100).

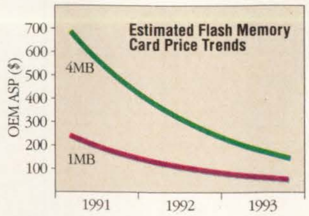
Motorola, MOS Memory Products Div, Box 6000, Austin, TX 78762. Phone (512) 928-7726.

Circle No. 379

CIRCLE NO. 135

Actual Size.

With this simple card trick.



systems—from PCs to fax machines to bar-code readers.

The secret of the card's magic is Intel's ETOX™II Flash technology—combining RAM, ROM and mass storage capabilities onto a solid-state, energy-efficient medium. A technology so successful that volume continues to rise and prices continue to drop.

Want to know more about the secrets of this amazing technology? Then call (800) 548-4725 today and ask for Literature Packet #C8A01. And start performing your own disappearing tricks.

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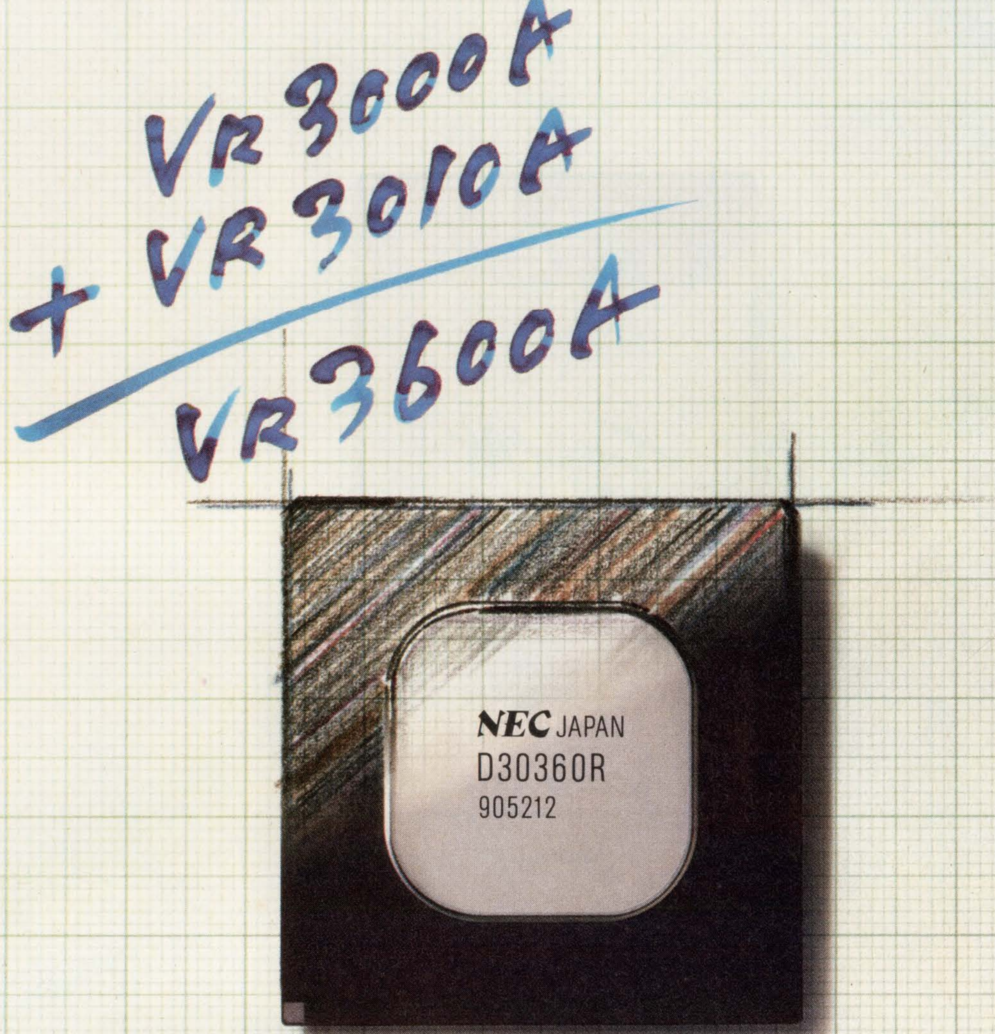

VR3000A
+ VR3010A
VR3600A
NEC JAPAN
D30360R
905212

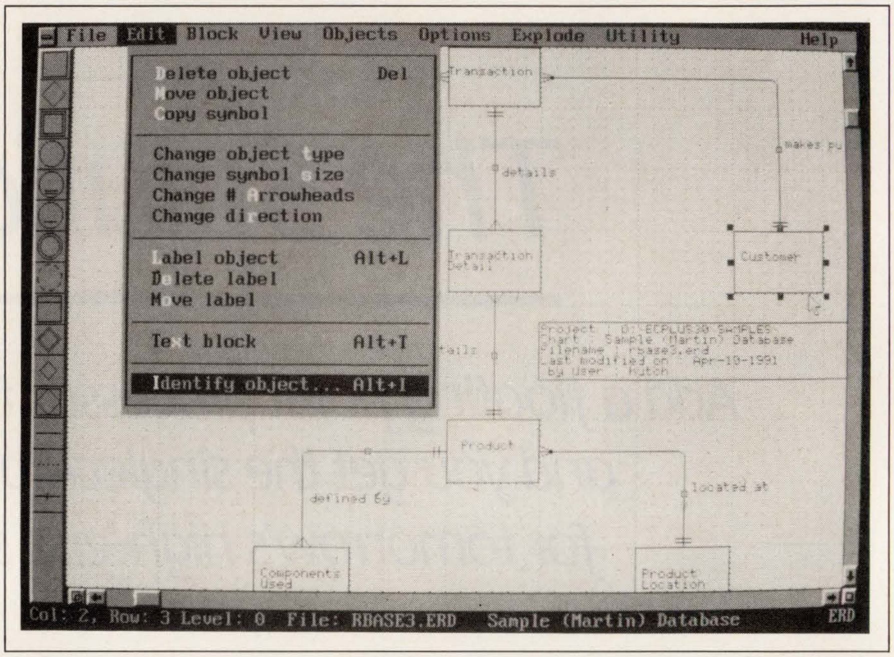
CIRCLE NO. 137

CAE & SOFTWARE DEVELOPMENT TOOLS

Front-End CASE Tool

- *Has low-cost core CASE functions*
- *For IBM PC/ATs, PS/2s, and compatibles*

Easycase Plus 3.0 is an upgrade of the supplier's front-end CASE tool. It allows use of data-flow diagrams (DFDs), transformation schema (real-time extensions to DFDs), state-transition diagrams, entity-relationship diagrams, data-model diagrams, and structure charts. It supports methodologies that include Yourdon/DeMarco, Gane and Sarson, SSADM, Ward-Mellor, Yourdon-Constantine, Chen, Martin, and Bachman. The product's Windows-like interface includes pull-down menus, pop-up dialog boxes, icons, scroll bars, hot keys, shortcut keys, and object dragging. Another version, Easycase Professional 3.0, includes an analysis-manager module that performs chart and data-dictionary consistency checking and verification against specific layout and methodology rules. Use of either version requires EGA or VGA graphics and a Microsoft (or compatible) mouse. $495; professional version, $649.



Evergreen CASE Tools Inc, 16650 NE 79th St, Suite 200, Redmond, WA 98052. Phone (206) 881-5149. FAX (206) 883-7676. **Circle No. 351**

Neural-Network Software

- *Artificial neurons recognize patterns in data*
- *Simulates Intel neural-network chip*

Dynamind 2.0 uses artificial neurons, modeled loosely on biological neurons of the human nervous system, to recognize patterns and trends in data. The software "learns" from experience; once trained, it finds patterns and associations in data that statistical or expert-system analysis can miss. It can read data from many popular spreadsheets. Developed jointly with Intel, the software simulates Intel's 80170NX ETANN (electronically trainable analog neural network) chip. It runs on any 80286-, 80386-, or 80486-based computer with a minimum of 640k bytes of memory. It requires DOS 3.0 or higher and EGA or VGA graphics. A mouse and a math coprocessor are optional. $79.

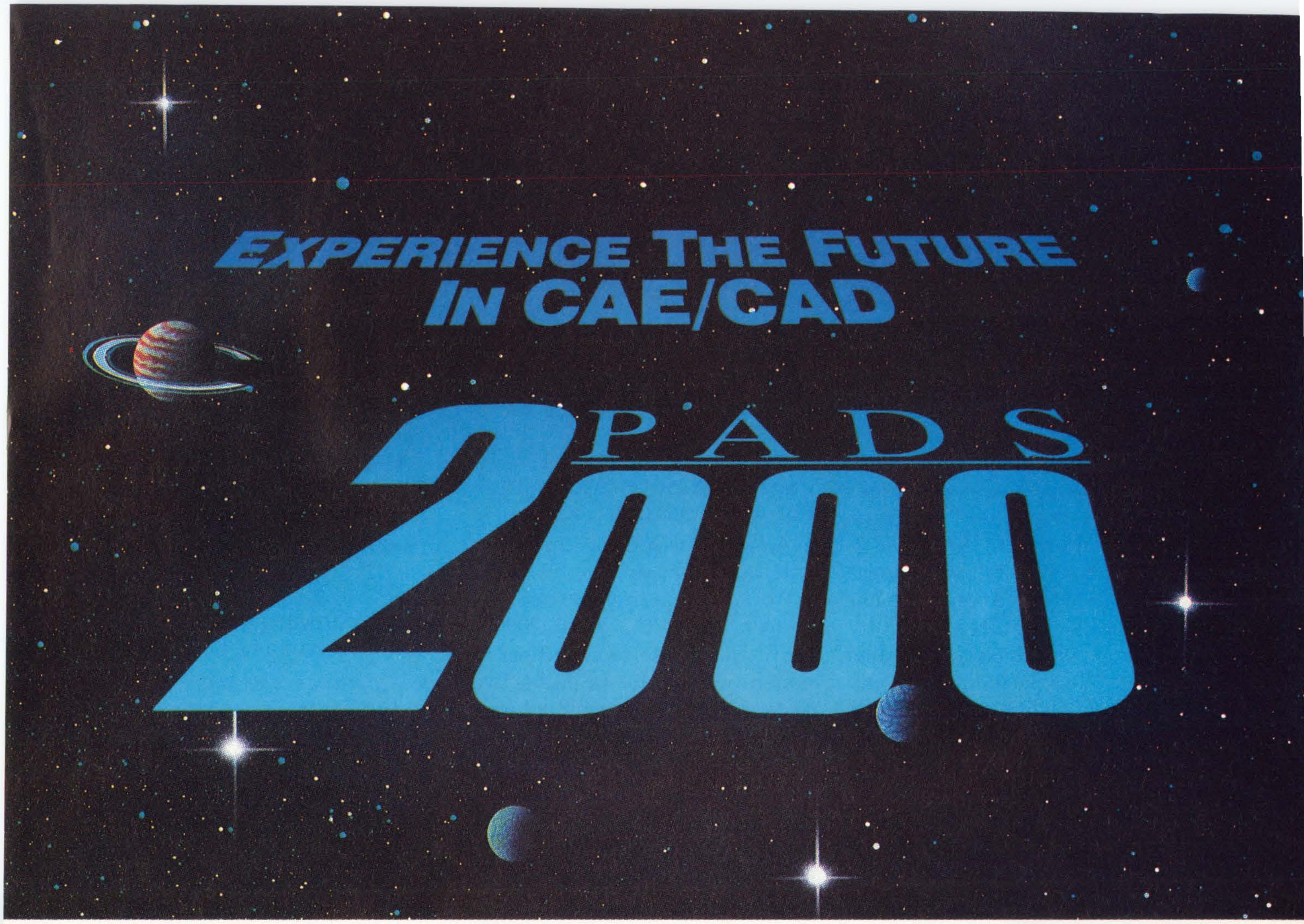
Neurodynamx Inc, Box 323, Boulder, CO 80306. Phone (303) 442-3539. **Circle No. 352**

ASIC Diagnostic Software

- *Permits observations at cell level*
- *Reduces E-beam searches*

CX-Probe, a workstation-based diagnostic software package, uses its developer's patented on-chip test structures to enable ASIC manufacturers to automatically isolate and identify functional failures in ASIC devices. It can run independently, or it can take advantage of fault-coverage test patterns generated by CX-Test, the developer's software for fault simulation and automatic test-pattern generation. A test-point matrix functions as an on-chip grid of sense probes; the software, a workstation, and automatic test equipment (ATE) constitute an automatic logic analyzer. The software uses the output of ATE to diagnose failures in ASIC devices caused by manufacturing defects, computer-aided design errors, and macrocell library errors. The software's diagnostic capabilities reduce the need to back trace from end test results; consequently, it reduces the need for time-consuming E-beam searches for defects. The package runs on Sun 4, SPARCstation 1, or SPARCstation 2 workstations; it works with ATE that includes Advantest 3320, Ando 8034 and 9035, Schlumberger Sentry 50, and Credence ASIX-2. License fee, $125,000 per copy.

Crosscheck Technology Inc, 2833 Junction Ave, Suite 100, San Jose, CA 95134. Phone (408) 432-9200. **Circle No. 353**

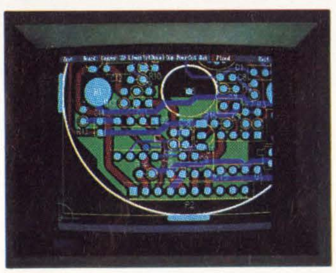


PADS 2000 is a Personal Computer based Printed Circuit board design system with many advanced features capable of outperforming most Workstation-based CAD systems—*at a fraction of the cost.*

As the most productive PC based board CAD system available today, PADS-2000 can handle even the most complex designs including: double sided surface mount boards, mixed technology boards, high speed designs and layouts exceeding 2000 IC's.

PADS-2000 design functionality includes:

- Over 11,000 parts/32,000 connections
- 1 micron Resolution
- True T-Routing capability
- Intelligent Copper Pour feature leaving isolated tracks and pads
- 0.1° parts/pads rotation
- Extensive Macro capability
- Digital, Analog and Critical Circuit autorouters



- On-line and Batch Design Rule Checking
- Instant track/segment length measurement
- Complete Forward/Backward ECO capability
- Uses 32 bit/386 native code for increased speed and functionality
- Easy-to-learn and Easy-to-use

Call today for a demonstration at your local authorized CAD Software Dealer.

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(800) 255-7814

CAD
Software, Inc.
119 Russell Street
Littleton, MA 01460

CIRCLE NO. 138

X-Windows Math Analysis

- *Provides interactive math analysis*
- *Tailored for engineering use*

Xmath, a mathematical-analysis software package for X-Windows, provides fast computation on X-Windows systems. It features a spreadsheet-style editor for matrices; point-and-click graphics annotation; on-line hypertext help; and a built-in source-level debugger window for script-based programming. The interactive Xmath plotting environment, built around the OSF/Motif user interface, has Macintosh-like features. It automatically generates plots from data or computations, including 2-D scatter plots, 3-D surface plots, multiple X and Y plots, and multiple-curve strip charts. With the point-and-click interface, you can interactively annotate or alter the plots. The software incorporates application-specific engineering objects that include vectors, matrices, polynomials, and lists. Single-user license, $2495; existing users of Matrix can upgrade at no charge.

Integrated Systems Inc, 3260 Jay St, Santa Clara, CA 95054. Phone (408) 980-1500. FAX (408) 980-0400. **Circle No. 354**

PC-Based Software For PC-Board Design

- *Allows arched or beveled miters at route corners*
- *Works interactively or manually*

Version 3.0 of the PADS-2000 pc-board design software offers designers who prefer to interactively route a board the capability to automatically insert an arched or beveled miter at each route corner. Seven different mitering radii are available. Users also can manually route with arc segments, inserting or deleting segments at corners; the software checks for proper spacing. The software also permits editing of copper-pour "islands," and it automatically deletes islands smaller than a given size. Additional features include pad-stack modification on individual components, drill-hole checking, and improved blind/buried via support. $6995.

CAD Software Inc, 119 Russell St, Littleton, MA 01460. Phone (800) 255-7814; (508) 489-8929. FAX (508) 486-8217. **Circle No. 355**

Electromagnetic Simulation For Microwave Circuits

- *Simulates microwave ICs*
- *Has greatly increased speed and simulation complexity*

The approach used by version 3.0 of EMSim, software for the electromagnetic simulation of linear, multiport MMIC (microwave monolithic

IC) and MIC (microwave hybrid IC) components, surpasses other methods' speed and simulation complexity by as much as an order of magnitude. The product has applications in the design and analysis of high-frequency communications circuits. These applications include amplifiers, filters, and signal-distribution networks—where interelement coupling and circuit-compaction effects degrade circuit response and cannot be analyzed by simulators that use popular equivalent-circuit technology. The software uses an algorithm based on a method-of-moments electromagnetic formulation. Analysis times for a complex MMIC circuit with 20 to 30 MMIC elements are typically less than an hour on a Sun SPARCstation. An interactive graphical interface permits input of planar microwave circuits; GDS-II mask files can be imported directly. Versions for Sun 4 and SPARCstations are available now. Later this year, versions for HP/Apollo series 3000 and 4000, HP Series 300 and 400, and IBM RS/6000 will be available. From $19,500.

EEsof Inc, 5601 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (818) 991-7530. FAX (818) 991-7109. **Circle No. 356**

Background-Mode Debugging System

- *Works in background mode for Motorola 68331/332 and 68340*
- *Needs no target resources and costs less than an emulator*

The EST Series 300 debugging system operates through the background mode on the 68331, 68332, and 68340 microcontrollers, thus making use of debugging services built into the chips' microcode. The system provides the hardware and logic to enable background mode for debugging and to disable it for real-time execution. According to the product's supplier, the system does not require stable ROM, RAM, interrupt vectors, and RS-232 communications as a ROM monitor does. Rather, like an in-circuit emulator, the system needs no target resources. Low-level background-mode commands allow downloading, booting, and halting an application; single stepping or multiple stepping through instructions; simple or conditional breakpoints on RAM or ROM code and data; and execution trace. A version of the Intermetrics XDB 5.0 debugger is available for symbolic source-level debugging in C. $2450; with XDB and tool kit, $5950.

Embedded Support Tools Corp, 10 Elmwood St, Canton, MA 02021. Phone (617) 828-5588. FAX (617) 821-2268. **Circle No. 357**

The next generation of IDC Interconnection:

Same performance, one-half the size.

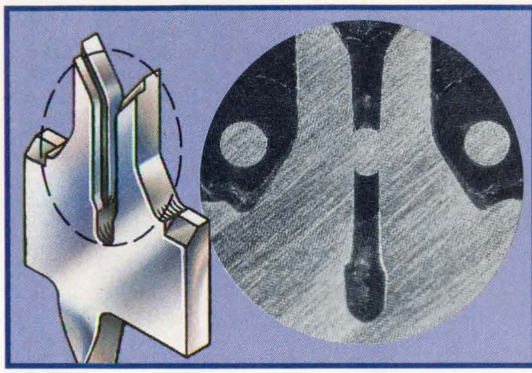
System 311 is the next generation of reliable high performance IDC mass termination systems from Thomas & Betts, a pioneer in the development of IDC.

A natural evolution, the new System 311 combines the finest capabilities of our proven Ansley® IDC System, downsized and precision engineered to terminate .025 pitch cable.

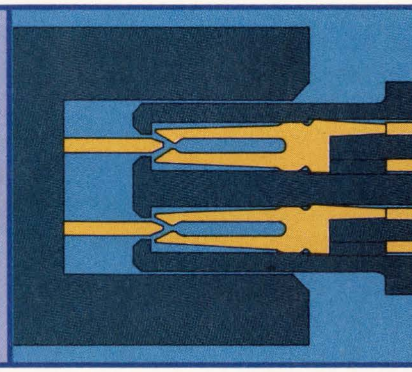
Performance-oriented features make System 311 the new standard in IDC fine pitch systems – a beryllium copper contact with a dual mating beam that provides greater than 100 grams normal force (150 KPSI Hertz Stress), a unique "coined-slot" IDC contact joint, one piece housing design,

• ***NORTH AMERICA*** **– Canada:** 708-357-0404; **Mexico:** Naucalpan, 905-393-85-10 • ***PACIFIC*** **– Australia:** Wyong North, NSW, 61-43-53-2300; **Hong Kong:** Kowloon, 852-739-1286; **Japan:** Tokyo, 81-3-3791-6411; **Singapore:** 65-747-0244; **Taiwan:** Taipei, 886-2-713-0509

TION



Contact-to-Conductor Relationship – Thomas & Betts' "coined-slot" contacts are designed to position the terminated conductors within a specified region for maximum conductivity and reliability.



Precision Lead-In Design – assures that repeated connect/disconnect functions are consistently smooth and without pin damage.

Our Own Vertical Eject Design – saves board real estate and ensures positive locking and easy disengagement of header from mating socket without stress to cable, contacts, or solder joints.

and high performance materials are combined to ensure excellent system integrity and maximum reliability.

System 311 incorporates these customer-requested features into a compact interconnect system with board space savings of up to 50%.

From cable to connectors to application tooling, System 311 is designed to meet or exceed the most stringent customer requirements for fine pitch IDC mass termination.

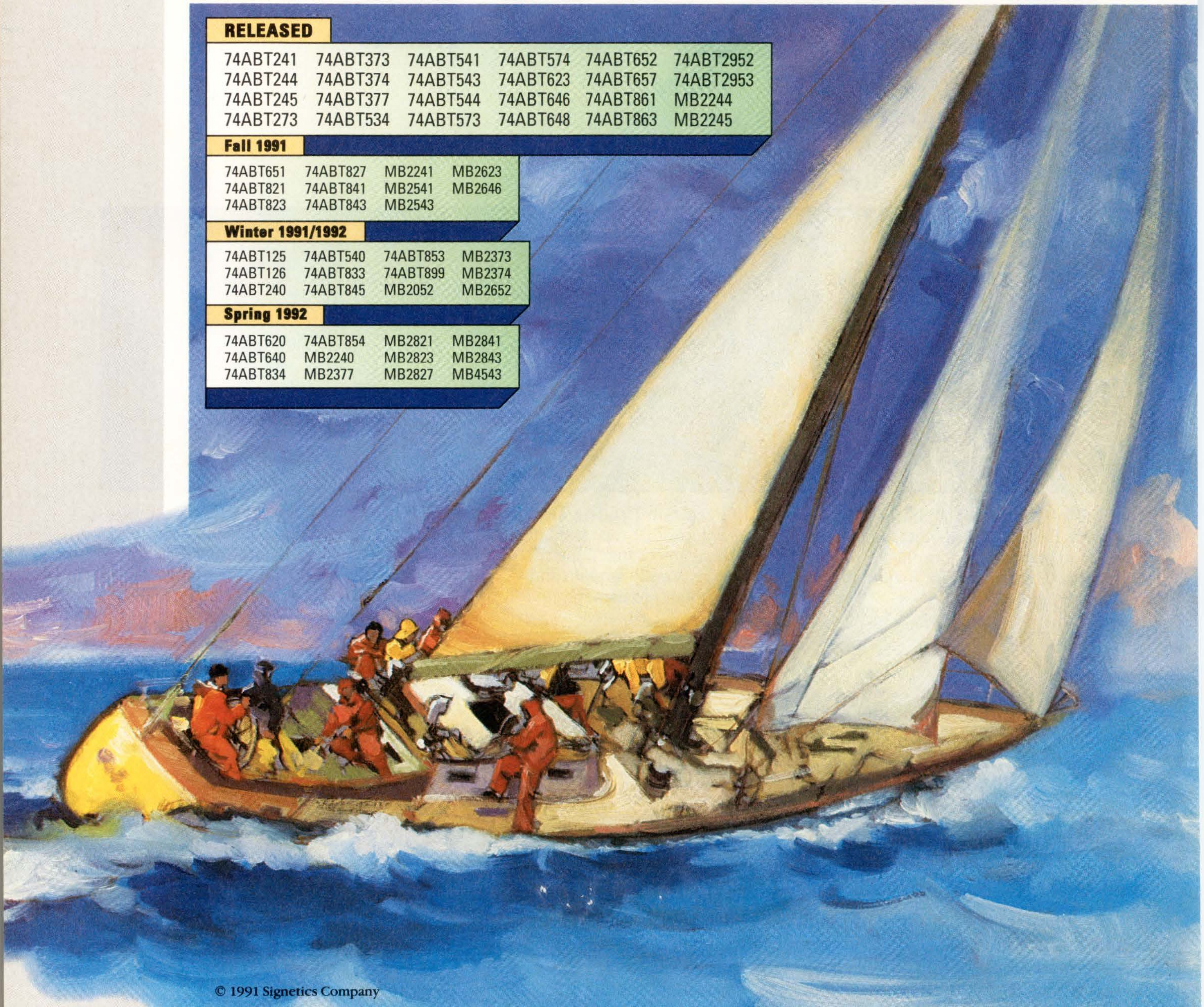
For complete information or help with a specific application, call or fax: Thomas & Betts Corporation, Electronics Division, 200 Executive Center Drive, Greenville, S.C., Phone: 803-676-2900, Fax: 803-676-2991.

For the new System 311 Catalog call 800-344-4744.

Thomas&Betts

• ***EUROPE* – England:** Marlow, 44-6284-6055; **France:** Rungis Cedex, 33-1-4687-2385; **Germany:** Egelsbach, 49-6103-4040; **Italy:** Milano, 39-2-6120451; **Luxembourg:** Foetz, 35-255-0002; **Spain:** Barcelona, 34-3-3002252; **Sweden:** Upplands Vasby, 46-760-88110

Signetics ABT. Advanced BiCMOS in performance



RELEASED					
74ABT241	74ABT373	74ABT541	74ABT574	74ABT652	74ABT2952
74ABT244	74ABT374	74ABT543	74ABT623	74ABT657	74ABT2953
74ABT245	74ABT377	74ABT544	74ABT646	74ABT861	MB2244
74ABT273	74ABT534	74ABT573	74ABT648	74ABT863	MB2245

Fall 1991			
74ABT651	74ABT827	MB2241	MB2623
74ABT821	74ABT841	MB2541	MB2646
74ABT823	74ABT843	MB2543	

Winter 1991/1992			
74ABT125	74ABT540	74ABT853	MB2373
74ABT126	74ABT833	74ABT899	MB2374
74ABT240	74ABT845	MB2052	MB2652

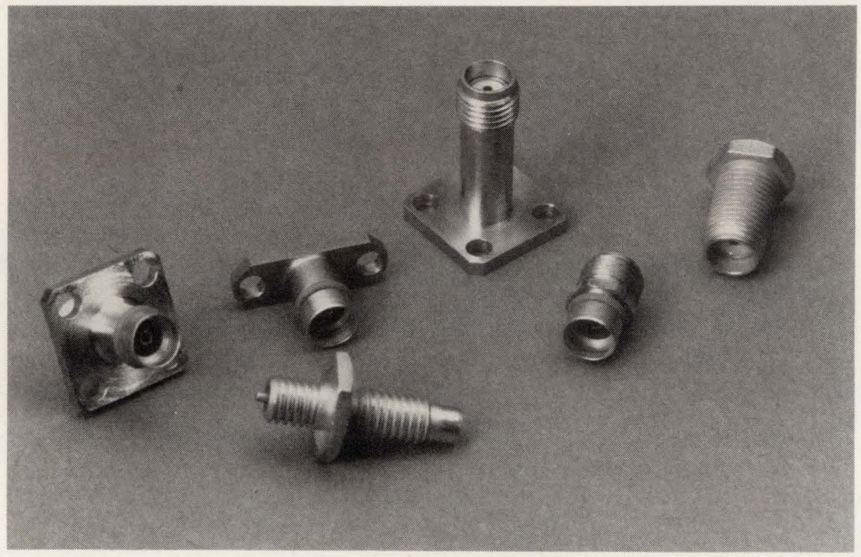
Spring 1992			
74ABT620	74ABT854	MB2821	MB2841
74ABT640	MB2240	MB2823	MB2843
74ABT834	MB2377	MB2827	MB4543

Philips Semiconductors

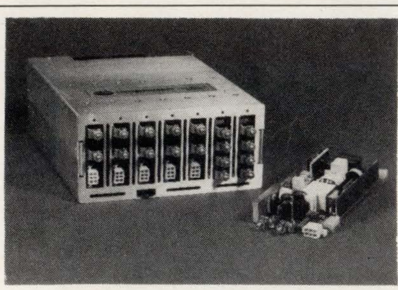
RF Launchers

- *Available in hermetic and nonhermetic versions*
- *Stack on 0.2-in. centers*

Designed for matched impedance lines, these RF launchers come in SMA, SMC, 3.5-mm blindmate, and 2.8-mm blindmate styles. Hermetic and nonhermetic units are available in various mounting versions. The devices stack on 0.2-in. centerlines. Termination end choices include round-pin, flat-tab, slotted round-pin, nail-head, or female contact. The hermetic launchers incorporate a fused glass-to-metal coaxial seal, which is either within the connector or comes as a loose piece brazed or soldered into the module. The units are available with square, rectangular, or round flanges. Cable dielectric can be exposed at varying lengths beyond the panel mounting end. \$3 to \$7 (1000). Delivery, 6 to 10 weeks ARO.



AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752.
Circle No. 380



Switching Power Supplies

- *Have as many as 14 outputs*
- *Develop 800W output*

Unimod multiple-output switching power supplies can provide as many as 14 outputs in virtually any combination of 16 single- and multiple-output modules. Housed in a fan-cooled 3.8×8×11-in. case, the supplies provide an output of 400 to 800W. Available output levels range from 2 to 48V. The supplies have an autorange input, which accepts 115 or 230V ac. Supply output levels have a ±10% adjustment range. Single output supplies can be paralleled for higher current applications. The units feature n+1 redundancy capability. Efficiency figures range to 85%, and MTBF equals 100,000 hours. Overload and overvoltage protection is standard. \$650 to \$1130. Delivery, two to eight weeks ARO.

Unipower Corp, 2981 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-2442. FAX (305) 971-1837. **Circle No. 381**

Mil-Spec Relay

- *Qualified [illegible] MS-24149-D1*
- *Has a [illegible] contact rating*

The FC-200 dpdt general-purpose relay is qualified to MS-24149-DI and AFCL M6106 for applications involving high inductive loads. The device has a contact rating of 10A at 28V dc and 115/220V ac. The relay is hermetically sealed and features a balanced armature design. Operating time for either ac or dc loads equals 20 msec; release time equals 20 msec for dc loads and 50 msec for ac loads. Measuring 2.6×2.5×1.6 in., the relay operates over a −70 to +125°C range. It can withstand 25g shock for 11 msec; vibration sine rating measures 10g from 10 to 1500 Hz. Insulation resistance equals $10^8\Omega$. Suppression circuitry is available for dc units. \$160. Delivery, eight weeks ARO.

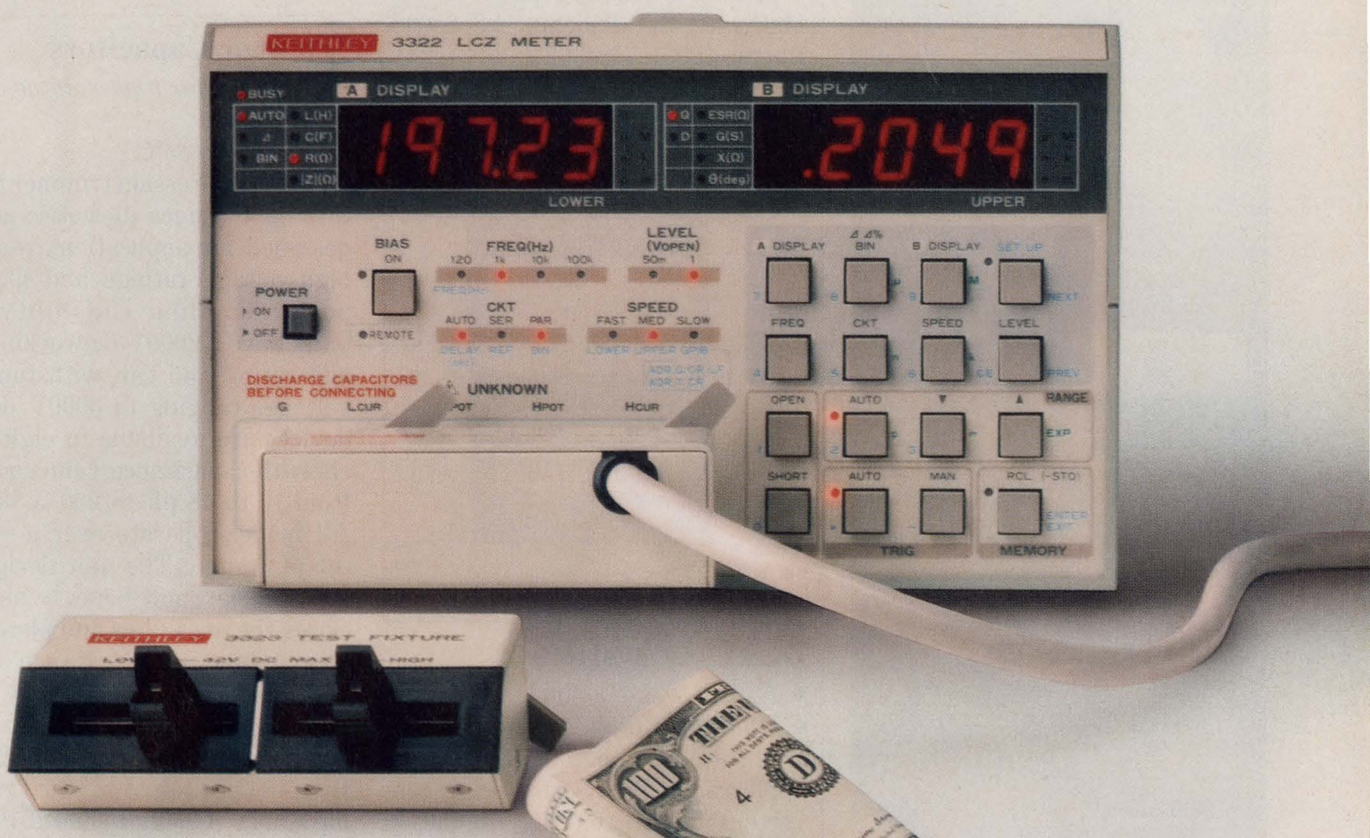
Struthers-Dunn/Hi-G Co Inc, Lambs Rd, Pitman, NJ 08071. Phone (609) 589-7500. FAX (609) 589-2619. **Circle No. 382**

Pressure Sensor

- *Is fully signal conditioned*
- *Available as a basic element*

The MPX5050 fully signal-conditioned pressure sensor integrates the sensing element, offset calibration, temperature-compensation circuitry, and signal amplification on a monolithic silicon chip. The unit is well suited for μP-based systems that use A/D converter inputs because the sensor output scale is calibrated from 0.5 to 4.5V. The device is temperature compensated for a

Two new ways for you to make sensitive LCZ measurements. Even if you're sensitive about price.



Keithley has found a way to fit accuracy and value into the same LCZ meter. In fact, we've found a *couple* of ways.

Introducing the affordable Keithley LCZ meters: a benchtop Model 3321 and a multifeatured Model 3322. Both deliver 0.1% basic accuracy, 4-1/2-digit resolution, automatic setting of function and equivalent circuits, multiple test frequencies, and more. The 3322 adds binning and deviation capabilities, plus other value features.

Now, make reliable measurements with ease. Obtain more accurate test results. And, have some money left in the budget – maybe for some Keithley test fixtures?

Looking for a meter to make sensitive AC measurements? Talk to a manufacturer that's also sensitive about price. Call Keithley Instruments at 1-800-552-1115.

KEITHLEY INSTRUMENTS

CIRCLE NO. 140

0 to 85°C range. The unit uses a silicon shear stress strain gauge for differential pressure measurements of 0 to 7.5 psi. The units are available in a basic element package as well as in single-and dual-ported versions. Customized outputs are also available. \$45 (100).

Motorola Inc, MD Z201, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (800) 752-3621; (602) 244-4556. FAX (602) 244-5738.

Circle No. 383

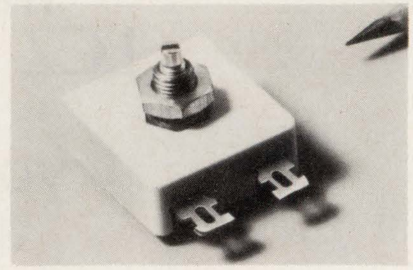
DC/DC Converters

- *Feature 0.001% ripple*
- *Offer adjustable output*

Well suited for photomultiplier tube applications, PC Series dc/dc converters feature 0.004% regulation and 0.001% output ripple. Remote voltage programming and remote voltage monitoring are standard. Positive or negative output voltages (fully adjustable) of 1500, 2000, or 2500V are available. Input voltage requirement equals 15V ±5%. The fully encapsulated converters operate over a −10 to +60°C range and have a 1-ppm/°C temperature coefficient. Internal voltage control, current monitor, and reverse-polarity protection are offered as standard features. Other output levels are available on special order. \$85 (OEM qty).

Emco High Voltage Co, 11126 Ridge Rd, Sutter Creek, CA 95685. Phone (209) 223-3626. FAX (209) 223-2779.

Circle No. 384



Trimmer Capacitors

- *Designed for high-voltage applications*
- *Operate to 85°C*

Type 9 compression trimmer capacitors have a mica dielectric and are designed for applications requiring high-voltage ratings and high RF power-handling capability. The units have a 2000V dc working voltage rating and can withstand test voltages ranging to 3000V dc. The devices are available in eight models with capacitance values ranging from 10 to 48 pF to 250 to 480 pF. All models operate over a −35 to +85°C range. The unit design features a ceramic base, which encloses the mica films and plates. Device insulation resistance equals $10^{11}\Omega$ min. From \$3.49 (100). Delivery, 10 weeks ARO.

Sprague-Goodman Electronics Inc, 134 Fulton Ave, Garden City Park, NY 11040. Phone (516) 746-1385. FAX (516) 746-1396.

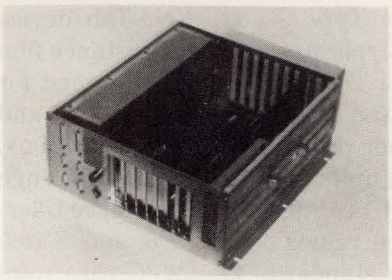
Circle No. 385

Magnetic Components

- *Meet MIL specs*
- *Are surface mountable*

Series 600xx power inductors and transformers are surface-mountable devices that meet MIL-T-27/356 specifications. The devices are designed to be compatible with automatic insertion equipment and can be supplied as filter inductors, ripple suppressors, common-mode chokes, isolation transformers, step-up transformers, or step-down transformers. The devices operate over a 0.1- to 300-MHz range. Inductance values range from 100 mH to 10H. The components accommodate temperatures of −55 to +125°C with only a 2% change in inductance. Other specifications include 30°C max temperature rise, and 30% max inductance drop while handling rated current. $7 to $9 (1000).

Vanguard Electronics Co Inc, 1480 W 178th St, Gardena, CA 90248. Phone (213) 323-4100. FAX (213) 329-8427. **Circle No. 386**

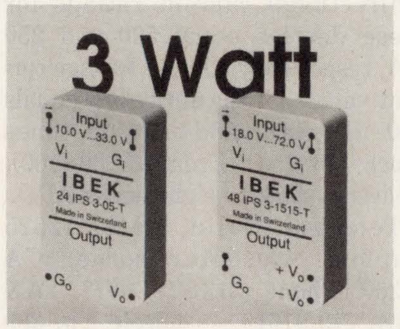


Transportable Chassis

- *Designed for industrial applications*
- *Accommodates two drives*

Designed for industrial applications, the QPC5304 chassis has a small 6.5×14.25×16-in. footprint for easy conveyance. The unit comes with a 6-slot backplane; it can accommodate two 3½-in. disk drives; and it's designed for 286, 386, and 486 single-slot computers. The standard chassis comes with a 200W power supply as well as two 3½-in. dc fans, which combine to generate an 80-cfm air flow. The filtered, air-cooling system is designed to exclude dust and dirt while keeping the enclosure close to ambient temperature. The enclosure side plates are made of extruded aluminum with heavy steel plates in front and rear. The rear plate has provision for a standard AT-compatible DIN connector. Space is also provided for two 25-pin D connectors and four 9-pin D connectors. $925.

Qualogy Inc, 109 Bonaventura Dr, San Jose, CA 95134. Phone (408) 434-5200. **Circle No. 387**



DC/DC Converters

- *Feature a 3-kV isolation*
- *Available in single- and dual-output versions*

IPW3 dc/dc converters develop a 3W output and feature 3000V p-p input-to-output isolation. The converters are available with input ranges of 10 to 33 or 18 to 72V. Single- and dual-output versions provide 5, 12, or 15V. Operating efficiencies range to 80% and full-power operating range equals either −25 to +71 or −40 to +85°C. The pc-board-mountable converters are housed in an industry-standard, 24-pin DIP. The devices include an input filter and provide short-circuit protection as a standard feature. $60 to $70 (100).

Melcher Inc, 200 Butterfield Dr, Ashland, MA 01721. Phone (800) 828-9712; (508) 881-4715. FAX (508) 881-5082. **Circle No. 388**

Solid-State Relays

- *Screened to MIL-R-28750*
- *Switch 2A*

FB Series solid-state relays are available with W- or Y-level screening of MIL-R-28750. The FB00CDW and FB00CDY switch dc and bidirectional loads of 2A and 1A, respectively (both have a 0.1Ω on-resistance and an 80V load rating). Bidirectional and dc switching ratings for FB00FCW and FB00FCY models equal 0.5A and 1A, respectively (both have a 180V load rating). FB00KBW and FB00KBY models are rated for 350V and have an on-resistance of 1.8Ω. The dc and bidirectional current ratings for these devices equal 500 and 250 mA, respectively. Output leakage current values for the entire line equals 200 nA max, and turn-on times reach 150 μsec. From $64.35 (100). Delivery, stock to eight weeks ARO.

Teledyne Solid State, 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077. FAX (213) 779-9161. **Circle No. 389**

DC/DC Converters

- *Designed for military applications*
- *Have a 45W/in.³ density*

The RY2805-75 and RY2805-50 Series military dc/dc converters switch at 1 MHz and provide full power output at 95°C. They accept 28V inputs and output 5V at 15 and 10A, respectively. Power density equals 45 W/in.³ for the 75W version and 30 W/in.³ for 50W units. The converters include an EMI filter. Under MIL-STD-461C, the converters meet CS02, CS06, and the narrowband emissions of CE03 when used with two external capacitors and an external inductor. Output and input overvoltage protection, short-circuit current limit, thermal shutdown, input transient protection, and soft start are standard features. From $1900.

Raytheon Co, 465 Center St, Quincy, MA 02169. Phone (617) 479-5300. **Circle No. 390**

High-Density Supplies

- *Output 3500W*
- *Have a 7.6 W/in.³ power density*

M Series switching power supplies develop a 3500W output from a package measuring 5×8×11.5 in.—a power density of 7.6 W/in³. Internal current-mode control provides $n+1$ capability for as many as eight supplies. Standard features include overvoltage protection, overcurrent protection, overtemperature protection, power-fail flag, power-good flag, redundant bidirectional error signals, remote margining, and bidirectional synchronization signals. The supplies operate from inputs of 208 to 230V ac or 220 to 350V dc. $2495.

OPT Industries Inc, 300 Red School Lane, Phillipsburg, NJ 08865. Phone (908) 454-2600. FAX (908) 454-3742. **Circle No. 391**

Power Resistors

- *Feature values as low as 0.1Ω*
- *Rated for 20W*

The Type MP821 Kool-Tab device incorporates a power resistance film in a TO-220 package. Designed for power supply, motor control, and other power-switching applications, the units feature a resistance range of 0.1 to 9.99Ω, and resistance tolerance values of ±1, ±5, and ±10% are standard. At a 25°C case temperature, the resistors have a 20W power rating. Single-screw mounting simplifies attachment to a heat sink. MP821 0.1Ω, 5% device, $1.95 (5000). Delivery, six weeks ARO.

Caddock Electronics Inc, 17271 N Umpqua Hwy, Roseburg, OR 97470. Phone (503) 496-0700. FAX (503) 496-0408. **Circle No. 392**

DC/DC Converters

- *Have four isolated converters in a single package*
- *Deliver 750 mW/output*

HPR2xx Series dc/dc converters have four totally isolated converters housed in a SIP measuring 0.35×2.22×0.41 in. Each of the four outputs delivers 750 mW of unregulated power to dual loads. The converters accept inputs of 5, 12, 15, or 24V and output ±5.2, ±12, and ±15V. Internal input and output filtering is standard. The units operate at 295 kHz and have efficiency figures ranging to 84%. Operating range spans −25 to +85°C. $16.89 (1000).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. **Circle No. 393**

"You think ITC might make me a better designer, Tracy?"

Tracy: "For sure, Mark. I was there last year. It's really a great conference, with lots of good papers. Maybe we could both go this year?"

Mark: *"But ITC's a test conference. See, right there -* ***International Test Conference.****"*

"But lots of designers go to ITC. Their program has some of the best design papers I've seen anywhere. They really should call it International Test and Design Conference."

"Come on, Tracy! You're putting me on!"

"No, really. You know we have to design testable, reliable designs quickly - designs that go into production fast and bug free. Well, ITC really covers test full-cycle. Look at this program - **design/test integration, design for testability, BIST, boundary scan, fault simulation.** It's all there, and more."

"So, we should go to ITC to find out what's happening in design?"

"Not everything, of course. But test is the hottest thing in design. And ITC's been covering design/test integration for years. And nearly half of ITC attendees work in design."

"What do they have besides technical papers?"

"There are about 120 papers. But there are also 18 tutorials, panel sessions, exhibits, professional meetings and user group meetings. And ITC's reception and other social events give you lots of chances to get to know people - to make contacts. The problem, really, is to take it all in."

"O.K. I'm convinced. Where is it and when?"

"That's another plus - it's in Nashville, at the Opryland Hotel. We can catch some great live country music, and in late October the weather's terrific. The dates are October 26 - 30, 1991."

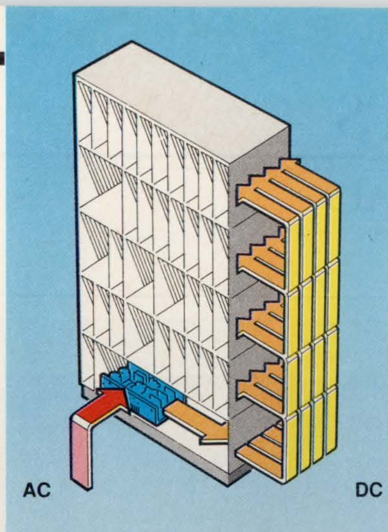
"So what do we do next?"

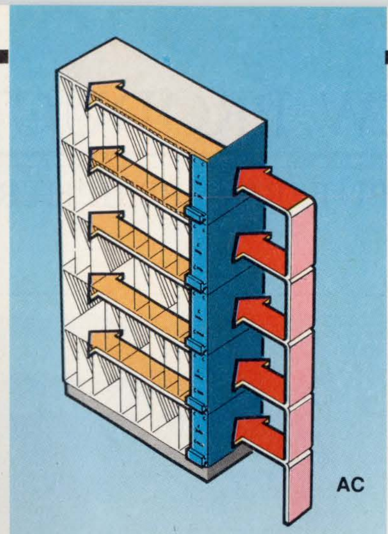
"ITC will send us a program and registration information. Just call **ITC at 814 941-4666.**"

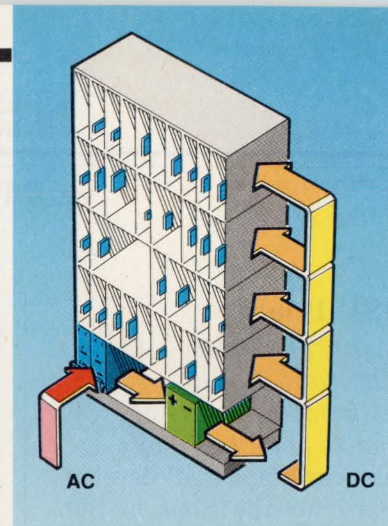
IEEE COMPUTER SOCIETY

IEEE THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

CIRCLE NO. 144







The Power in Telecommunications

It's your choice!

However you decide to power your electronic equipment, Ericsson can provide a choice of proven power supply solutions to meet your needs.

For example, the PLY series of 150 to 400 Watt open frame switchers can supply quadruple and adjustable DC outputs from an AC input to power a whole rack of electronic equipment.

A more distributed approach is offered by the PLB series of Eurocard AC/DC switchers. Depending upon the requirements, these 60 to 100 Watt units can power one or more shelves of equipment with the added security and fault tolerance which distributed power brings.

But perhaps decentralised on-card DC/DC converters offer the ultimate distributed power system. This can be powered by an AC/DC switcher in parallel with an optional battery back-up. Ericsson's renowned on-card DC/DC converters, PKA, PKC and PI, range from 0.3 to 40 Watts with up to three outputs and will provide a highly reliable and fault tolerant system.

Whichever you choose, you can be confident that their reliability and performance will be unsurpassed.

For full technical information on all of these products simply call us, or fax us the coupon.

Please send me your latest information **EDN 9/2/91**

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Company

Job Title

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France	**Ericsson Components Europe,** Guyancourt Tel:(01) 30 64 85 00 Fax:(01) 30 64 11 46
Germany	**Ericsson Components Europe GmbH,** Neu-Isenburg Tel:(06102) 200 50 Fax:(06102) 20 05 33
Great Britain	**Ericsson Components Europe,** Coventry Tel:(0203) 553 647 Fax:(0203) 225 830
Hong Kong	**Ericsson Components AB East Asia,** Wanchai Tel:575 6640 Fax:834 5369
Italy	**Ericsson Components Europe,** Milano Tel:(02) 3320 0635 Fax:(02) 3320 0641
Norway	**Ericsson Components A/S,** Oslo Tel:(02) 650 190 Fax:(02) 644 138
United States	**Ericsson Components Inc,** Richardson, TX Tel:(214) 997 6561 Fax:(214) 680 1059

ERICSSON

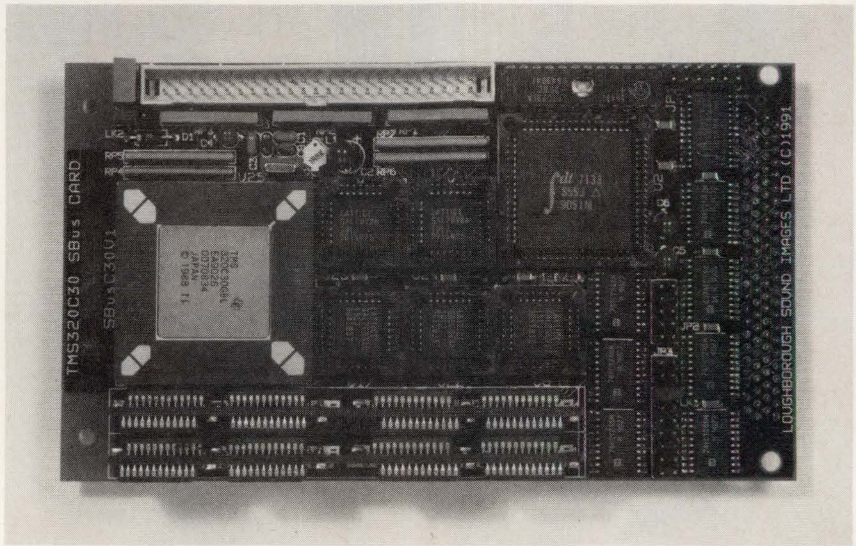
CIRCLE NO. 146

NEW PRODUCTS

COMPUTERS & PERIPHERALS

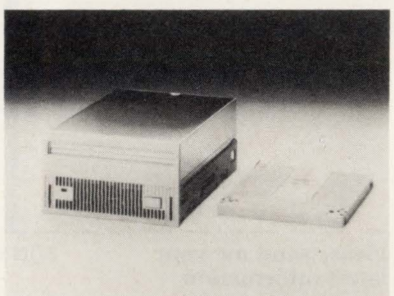
Sbus DSP Board

- *Employs a TI 33-MHz TMS320C30 DSP chip*
- *Has 128k × 32-bits of RAM expandable to 512k × 32 bits*



The Sbus board is a DSP development board for the Sbus in Sun SPARCstations. The board uses TI's 33-MHz TMS320C30 DSP chip and 128k × 32 bits of zero-wait-state RAM. You can expand the RAM to 512k × 32 bits. You can also add a daughter card, which has dual 16-bit ADCs and DACs. Two different daughter cards containing either a 200-kHz I/O module or a delta-sigma I/O module are available. The board also contains the company's 16-bit DSP-Link expansion bus for high-speed communication with other Sbus boards. The board operates as an Sbus slave, and it has a 2k × 32-bit dual-port static RAM for communicating with the SPARC-station. $4595. Board with TI's assembler and linker, TI's C compiler, and Spox operating system, $9595. Available, third quarter of 1991.

Spectrum Signal Processing Inc, Suite 301-3700 Gilmore Way, Burnaby, BC V5G 4M1, Canada. Phone (604) 438-7266. FAX (604) 438-3046. **Circle No. 403**



Rewritable Magneto-Optical-Disk Drive

- *Runs at 3600 rpm and transfers data at 1M byte/sec*
- *Stores 650M bytes and has 37-msec average access time*

The RO-5031 magneto-optical-disk drive conforms to the ISO standard for rewritable operation. The 5¼-in.-disk drive stores 650M bytes and rotates as fast as 3600 rpm. The drive can switch between 3600 and 1800 rpm speeds to permit compatibility with most ISO media. The high rotational speed permits a sustained read-transfer rate of 1M byte/sec and a write-transfer rate of 500k bytes/sec. A single-step seek method and a split-head optical system enables an average access time of 37 msec. An embedded SCSI controller is compatible with SCSI-1 and SCSI-2 communications. The drive has a 256k byte, dual-port data buffer, and it has an MTBF of 30,000 hours. $4000.

Ricoh Corp, 5150 El Camino Real, Suite C-20, Los Altos, CA 94022. Phone (415) 962-0443. FAX (415) 962-0441. **Circle No. 404**

Fast SCSI Host Adapter

- *Transfers 32-bit data on the EISA bus*
- *Bus mastering lets a SCSI device transfer data to RAM*

The EISA SCSI Master host adapter lets an EISA bus computer communicate with as many as seven fast SCSI devices. Operating as the bus master, the board permits a SCSI peripheral to communicate with the system memory without CPU intervention. The board transfers 32-bit data at 33M bytes/sec in block-transfer mode. All SCSI-1, Fast SCSI, and SCSI-2 peripherals can be attached to the board. Software drivers for DOS, OS/2, and Netware operating systems are available. Drivers resident in SCO Unix, SCO Xenix, and ISC Unix operating systems directly support the board. Adapter, software, cable, and documentation, $695.

Adaptec Inc, 691 S Milpitas Blvd, Milpitas, CA 95035. Phone (408) 945-8600. **Circle No. 405**

Enhanced VGA Card

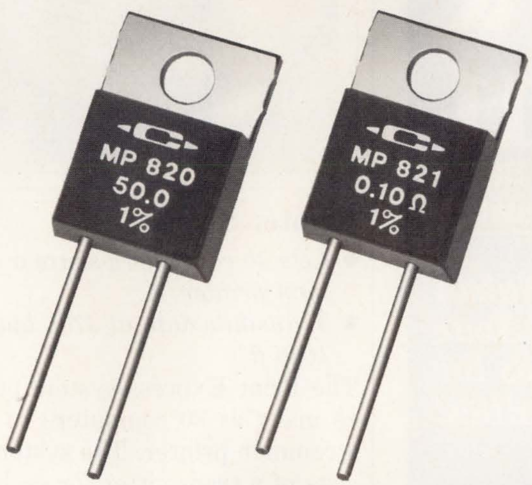
- *Displays 1024 × 768 pixels at 24 bits/pixel*
- *Has 3M bytes of RAM and supports 16.7M colors*

The Trucolor 1024AT 16-bit ISA

CADDOCK
ELECTRONICS, INCORPORATED

More *New* Power Resistors

New Low Resistance to 0.10Ω
Non-Inductive Designs
TO-220 Power Packages



Kool-Tab® Power Film Resistor
20 Watts at 25°C Case Temperature

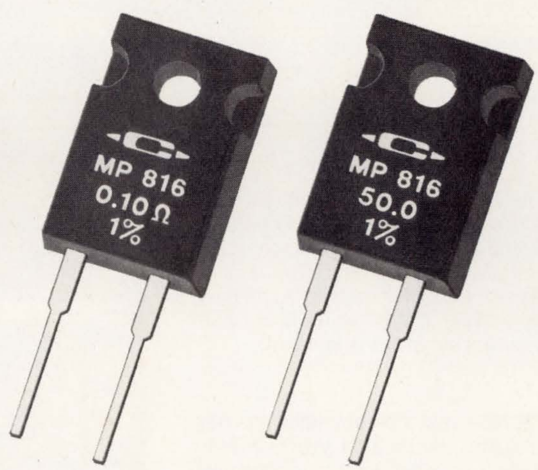
- **Metal Mounting Tab**
- **Resistance Range of 0.10 ohm to 10K**
- **Tolerance ±1%, ±2%, ±5% or ±10%**

CIRCLE NO. 147

Kool-Pak™ Power Film Resistor
16 Watts at 25°C Case Temperature

- ***Lower Cost***
- **Thermally Conductive Molded Package**
- **Resistance Range of 0.10 ohm to 10K**
- **Tolerance ±1%, ±2%, ±5% or ±10%**

CIRCLE NO. 148



More high performance resistor products from

CADDOCK
ELECTRONICS, INCORPORATED

Call or write for your copy of the Kool-Tab® and Kool-Pak™ data sheets.

Applications Engineering
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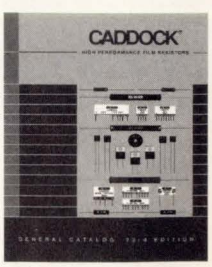
17271 North Umpqua Hwy.
Roseburg, Oregon 97470
Phone: (503) 496-0700
Fax: (503) 496-0408

Sales Office - USA and Canada
Caddock Electronics, Inc.
1717 Chicago Avenue
Riverside, California 92507
Phone: (714) 788-1700
Fax: (714) 369-1151

The 23rd Edition of the Caddock General Catalog includes specifications on over 200 models of high performance resistor products.



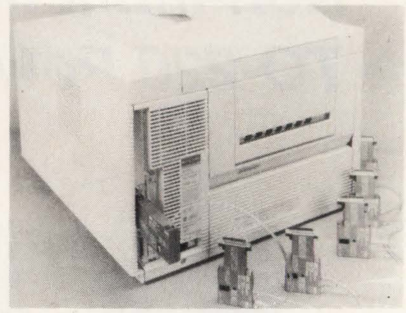
CIRCLE NO. 149

L-141.071

board for enhanced VGA graphics displays six resolution modes ranging from 320×200 pixels to 1024×768 pixels. Because the board produces 24 bits/pixel, it can display more than 16.7M colors. The board drives all fixed and multisynchronous VGA monitors having either interlaced or noninterlaced scan rates. The standard configuration has 1.5M bytes of video RAM, and an option provides 3M bytes of video RAM. The board has analog red, green, and blue outputs along with standard VGA synchronization signals on a VGA-compatible connector. It uses five ASICs, 20 ICs, 24 memory chips, and 24 components to minimize cost. Board with 3M bytes of RAM, $1499.

Ventek Corp, 31336 Via Colinas, Suite 102, Westlake Village, CA 91362. Phone (818) 991-3868. FAX (818) 991-4097.

Circle No. 406



Printer Sharer

- *Lets 30 computers share a common printer*
- *Transmits data at 370k bps over 4000 ft*

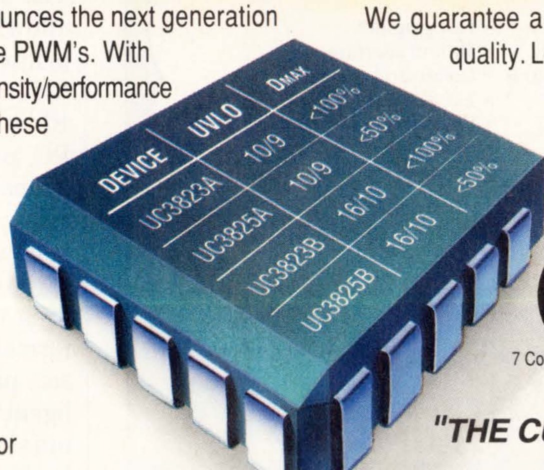
The Print Express system permits as many as 30 computers to share a common printer. The system consists of a transmitter for each computer and a receiver for the printer. Both the transmitters and the receiver plug directly into parallel ports on the respective devices. Each plug-in unit has an RJ12 connector, which permits data transmission over twisted-pair cables. The system transfers data at 370k bps over a maximum distance of 4000 ft. You can arrange the topology of the network in a star, bus, or mixed configuration. When a computer issues a print command, the network queues the command and prints the job in the sequence it is received. A starting kit, consisting of a transmitter and receiver, connectors, cables, and power supply, $149; additional transmitters, $59.

IMC Data Manager, 1360 Bordeaux Dr, Sunnyvale, CA 94089. Phone (800) 537-5999; (408) 744-9004. FAX (408) 744-0572.

Circle No. 407

All It Takes Is The *Right* Power

Unitrode Integrated Circuits announces the next generation of industry standard current mode PWM's. With increased demands on higher density/performance power supply designs, consider these features of the **UC3823A** and **UC3825A** family:



- Adjustable blanking of leading edge current noise
- Trimmed oscillator discharge for accurate frequency and dead time control
- Latched over current comparator
- Full cycle restart after fault
- Outputs active during UVLO
- Optional UVLO thresholds
- MHz+ performance

We guarantee a continued commitment to uncompromised quality. Look to Unitrode Integrated Circuits to provide unique solutions for your design needs. For more information on the **UC3823A** and **UC3825A** family, contact your Unitrode Representative or call:

(603)424-2410

7 Continental Boulevard, Merrimack, NH 03054 FAX (603) 424-3460

"THE CURRENT MODE PWM LEADER"

INTEGRATED CIRCUITS

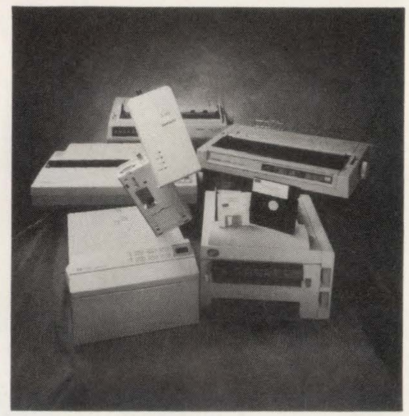
UNITRODE

CCITT V.32bis Modem

- *Connects SNA, X.25, and ISDN networks*
- *X.25 PAD supports four simultaneous sessions on the network*

The Ultra 144 modem conforms to the 14.4k-bps data-transmission rate defined by the CCITT V.32bis standard. Data transfers run at a 38.4k-bps rate defined by the CCITT V.42bis standard. The modem lets mainframes, workstations, and IBM PCs communicate as well as SNA, X.25, and ISDN networks. You receive the maximum 50% throughput improvement over 9600-bps synchronous communications. The modem's X.25 packet assembler and disassembler (PAD) supports four simultaneous sessions on a packet-switching network. The company's Autosync provides synchronous communications, and the modem supports the CCITT V.25bis standard for synchronous autodialing. It's also backward compliant with V.32, V.22bis, V.23, V.22, and V.21 specifications. $1199.

Hayes Microcomputer Products Inc, Box 105203, Atlanta, GA 30348. Phone (404) 840-9200. FAX (404) 441-1238. **Circle No. 408**



Printer Emulator

- *Lets you use boldface type, italics, and font size*
- *Emulates IBM 3287, 3262, 3268, or 4224 printers*

The Mainprint CG stand-alone unit allows a personal-computer (PC) printer to emulate an IBM 3287, 3262, 3268, or 4224 system printer. It's compatible with more than 400 PC printers. The unit has a Hex Transparency feature that lets you take advantage of the printer's boldface type, italics, and font size. A host parameter feature configures the emulator to print certain formats such as a specific character set, paper size, and pitch. An intelligent printer-sharing feature permits the printer to be used for both PC and mainframe applications. The emulator automatically switches between mainframe and PC print jobs. The unit lets IBM

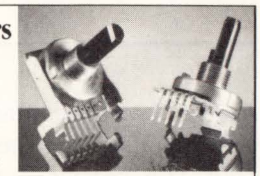
Vertical Mount Fixed Resistors

Series RSS Vertical Mount Metal Oxide Fixed Resistors feature self-standing, snap-in terminals, and they exhibit an excellent high frequency response and low inductance, making them suitable for PC board mounting in power supplies, switching regulators, monitors, printers, and color TVs.

Model RSS3FB is rated at 3W with a resistance range of 1Ω to 100KΩ. Model RSS5FB is rated at 5W with a resistance range of 1Ω to 2.4KΩ. Both are available in 15mm and 25mm heights. Free samples are available, contact Noble at 708/364-6038.

CIRCLE NO. 155

2-, 4-Bit and 5-Bit Rotary Encoders



Noble SDB161 2-, 4- and 5-bit encoders are compact (21mm ø) with a low profile (under 10mm height). Built with a sturdy diecast and steel construction, these encoders offer long life and reliability.

SDB161 encoders are for relative (2-bit) and absolute (4-bit, 5-bit) reference applications. 2-bit switches offer 36 detented positions; 4-bit switches offer 12 or 16 detented positions; 5-bit switches offer 24 or 32 detented positions. All encoders feature continuous rotation. The 2-bit is available in gray code; the 4-and 5-bit versions offer either binary or gray code. Custom designs can be accommodated. For free samples, contact Noble at 708/364-6038.

CIRCLE NO. 156

BIG IDEA

(If you didn't see the 3mm trimmer potentiometer, look again!)

When it comes to quality execution of electronic componentry, Noble crosses all the Ts and dots every I.

Our surface mount trimmer potentiometer (TMC3K) continues our commitment to space saving design, bringing state-of-the-art performance to a new dimension:

3.0mm x 3.65mm x 1.5mm

Easily adjusted, TMC3K incorporates a metal glaze element for outstanding stability; it is designed for reflow soldering, can be adhesive-mounted to circuit boards, and is available on 8mm tape for automated assembly. Operating temperature range is − 30°C to + 125°C.

The Noble 3mm potentiometer is perfect for hand held equipment, disk drives, bar code devices, and other consumer and business electronic products. For a free sample and more information on why it makes sense for you, call or write Noble today.

NOBLE

5450 Meadowbrook Industrial Court
Rolling Meadows, IL 60008
Phone: (708) 364-6038 FAX: (708) 364-6045

CIRCLE NO. 159

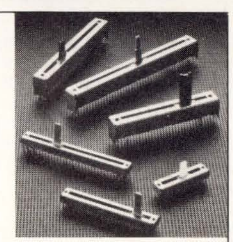
4mm Surface Mount Trimmers

TMC4K "chip" trimmers feature a ceramic substrate, a metal glaze element, and an insulated knob for easy adjustment. The TMC4K can withstand operating temperatures of -30℃ to +125℃ and is rated at 0.2 watts of power at 20V. Its standard resistance range is 200Ω to 1MΩ. Outside dimensions are 3.8mm wide x 4.5mm long (2.1mm height).

Available on tape and reel. Can be held to a circuit board by an adhesive for reflow soldering. Call Noble at 708/364-6038 for a free sample.

CIRCLE NO. 157

Slide Potentiometers



The VJ Series High and Low Profile Slide Potentiometers are lightweight, durable, and provide smooth operation. They function as volume, balance, brightness/contrast, temperature, lighting and graphic equalizer controls.

The Low Profile Series (with single or dual elements) features a slide travel of 15, 20, 30, 45, or 60mm. The High Profile Series is available in 30, 45, 60, 80 or 100mm travel.

Custom designs can be accommodated. Contact Noble at 708/364-6038 for a free sample.

CIRCLE NO. 158

3270 software communicate with an ASCII printer in the same manner that the software communicates with an IBM system printer. $995.

Avatar Corp, 65 South St, Hopkinton, MA 01748. Phone in Canada, (800) 235-2370; in US (800) 282-3270; (508) 435-3000. FAX (508) 435-2470. **Circle No. 409**

EISA Bus Computer

- *Has a 50-MHz 486 μP and a 256k-byte second-level cache*
- *Has 8M bytes of RAM and seven EISA slots*

The Deskpro 486/50L EISA bus computer uses an Intel 50-MHz 80486 μP. The standard model comes with a 256k-byte second-level cache, 8M bytes of RAM expandable to 104M bytes, advanced VGA graphics for displaying 256 colors having 640×480-pixel resolution, and seven EISA expansion slots. The desktop unit can store 2G bytes internally and more than 20G bytes externally. Software security features include power-on password, keyboard password, and network server mode. Both the 510M-and 340M-byte hard-disk drive have an access time of 12 msec. A 120M-byte hard-disk drive has a <19-msec access time. Backup options include a 1.3G- and a 2G-byte digital audio-tape drive. Model 120, $11,299; Model 340, $12,999; Model 510, $13,999.

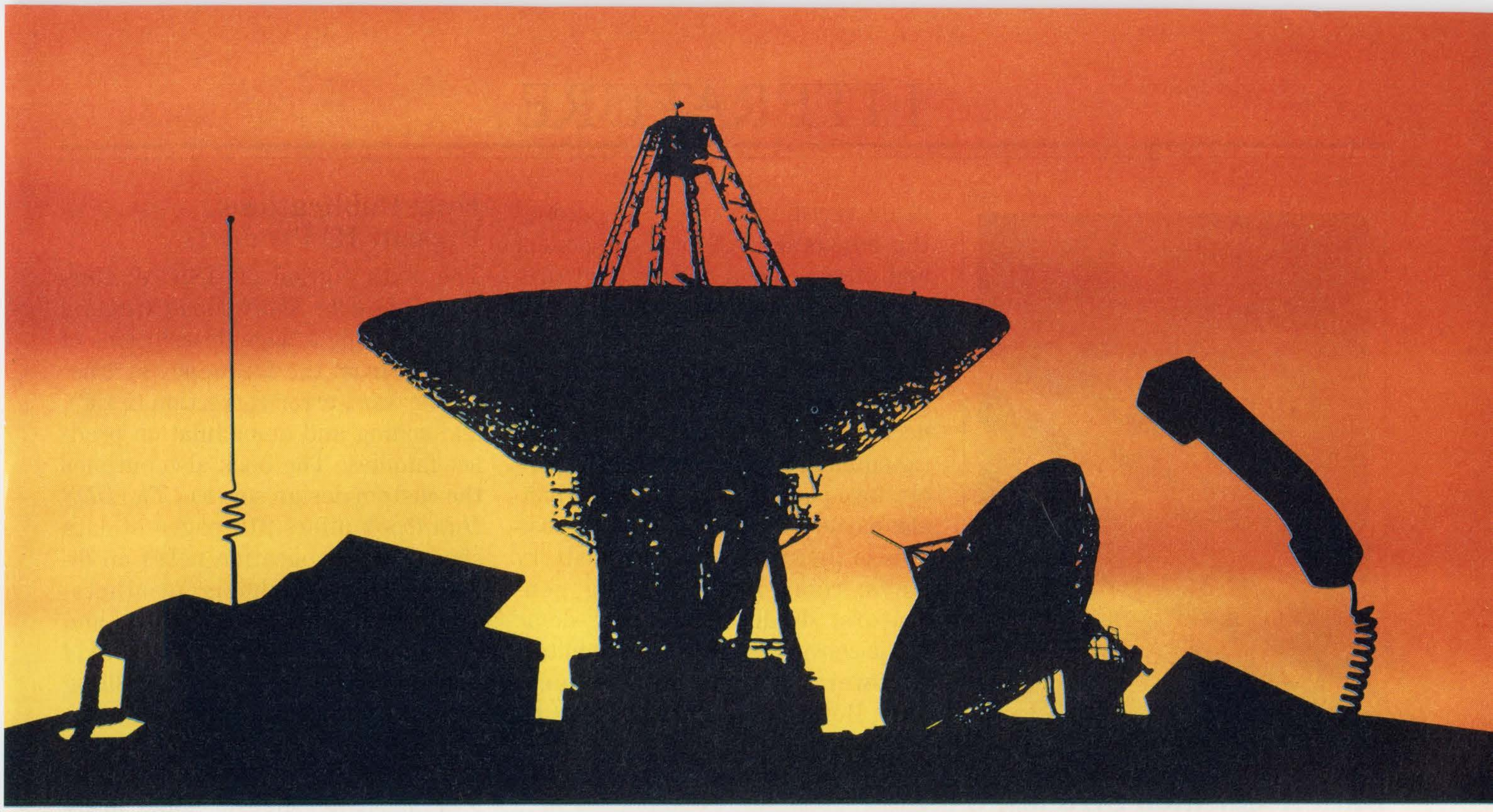
Compaq Computer Corp, Box 692000, Houston, TX 77269. Phone (713) 370-0670. **Circle No. 410**

Ruggedized Computer

- *Trades-off high cost for moderate ruggedness*
- *Has a 25-MHz 80386 μP and a 64k-byte cache*

The Model 302i is a ruggedized computer for industrial and laboratory environments. The computer's design is a tradeoff between expensive MIL-standard designs and inexpensive office-desktop designs. The computer has a 19-in. rack-mount chassis, a positive-pressure fan having filtered air flow, vibration mounts for the hard-disk drive, and a locking bar for the add-in cards. You can remove the computer's tray-mounted mother board using a single tool. The computer features a 25-MHz 80386 μP, a 64k-byte cache, eight ISA bus expansion slots, a 230W power supply, as much as 40M bytes of RAM, two serial ports, and one parallel port. Model with 4M bytes of RAM, a 52M-byte IDE hard-disk drive, and a 3½-in. 1.44M-byte floppy-disk drive, $3995.

Intel Corp, #AP-69, Box 7641, Mount Prospect, IL 60056. Phone (800) 548-4725. **Circle No. 411**



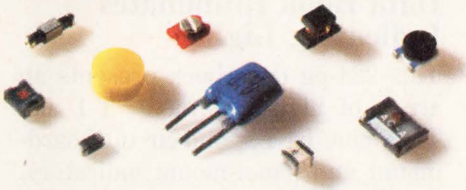
Murata Erie. We don't make faxes, cellular phones or satellite systems. But we make things better for those who do.

Whatever the telecom product, when you seriously consider your options in passive components, you'll see we can make a difference.

But how to compare? Well, specs are a start. But the fact is, specs often seem surprisingly similar–much like physical appearances.

There's always individual component cost, a comparison we at Murata Erie heartily encourage. But if you stop there, you could overlook some other very important distinctions.

Think first about product-line breadth. And the measurable advantages that can accompany acquiring most or all your passives from a single source. Then think about Murata Erie's product line, offering virtually



any type passive your product requires.

Now consider supplier capacity. Look at our multiple plants in North America and overseas. And ask yourself what other company could routinely ship, for example, 3.5 billion ceramic capacitors per month. Or match our network of local distributors–people ready to respond not only with product but with technical expertise as well.

Finally, try to find a company with more experience. You might begin by asking who pioneered, and continues to pioneer, electro-ceramic technology, the core of numerous electronic sub-technologies ranging from dielectrics to piezoelectrics.

All that done, we think you'll find choosing the right passive component line a simpler task. Getting started is even easier. Write or call us today. We'll show you how, for telecom OEMs, we're making things a lot better. And how we'll do the same for you.

muRata ERiE®

MURATA ERIE NORTH AMERICA

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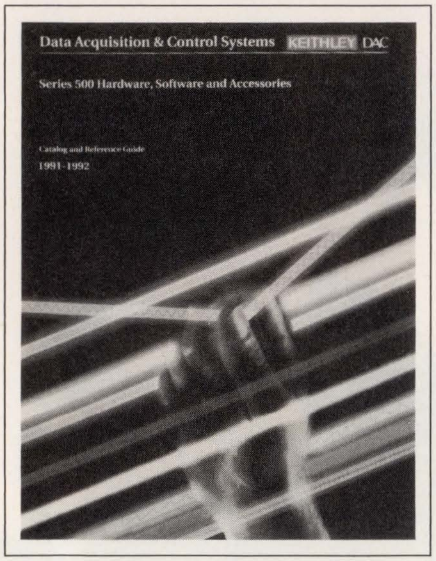


Publication Describes Data-Acquisition Systems

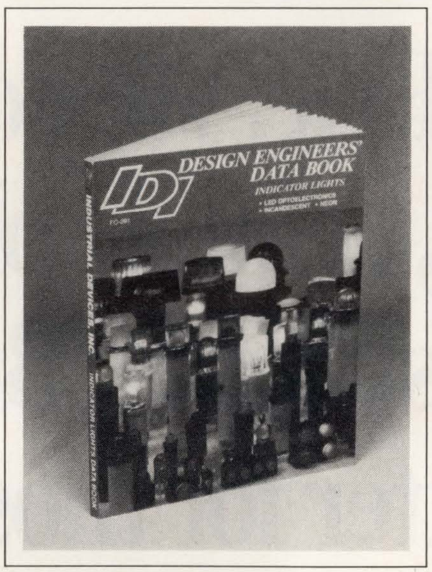
This 64-pg catalog highlights data-acquisition systems, software, and applications. It incorporates measurement and control systems, entry-level acquisition systems, and portable monitoring systems. Describing a spectrum of software that's compatible with the vendor's DAC hardware, it includes languages, menu- and window-driven data-acquisition packages, and process-monitoring and control software. Specifications for the complete Series 500 Measurement and Control Systems include the 10-slot high-speed mainframe; the portable 10-slot system; the IEEE-compatible 10-slot system, the small system with A/D, D/A, digital I/O, and triggering; IEEE-488 programmable small system/data logger with D/A, A/D, digital I/O, and triggering; and more than 30 different plug-in modules for measurement, signal conditioning, and control.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. **Circle No. 394**

Switch-Mode Rectifier Series

This 23-pg short-form catalog presents electrical specifications, operating characteristics, and design benefits of the Twinpack switch-mode rectifier systems. It outlines the advantages of each component and offers charts and product photos. Describing Twinpack modular power systems, the publication includes the PS/19; system status/control panels; low-voltage disconnect panels; miniload centers; digital-equalize panels; fuse-alarm panels; fuse panels; circuit-breaker panels; battery-disconnect panels; positive or negative-bus bars; battery trays; relay racks; ringing generators; dc/dc converters; dc/ac static converters; and a μP monitor.

Power Conversion Products Inc, Box 380, Crystal Lake, IL 60014. **Circle No. 395**



Data Book Illuminates Indicating Lights

This 224-pg data book presents an array of high-brightness, T-1 and T-1¾ blue LEDs, and circuit-board-mount and panel-mount indicators. Other products include flat-nosed LEDs, dual-quad multicolor LED assemblies, incandescent indicators, neon glow lamps, and oil-tight indicators. The publication provides specifications, illustrations, and a complete cross-reference of competitive products.

Industrial Devices Inc, 260 Railroad Ave, Hackensack, NJ 07601. **Circle No. 396**

Four Publications Present IC Products

The sixth edition of *ASIC & Custom Products Short Form Catalog* provides single-page descriptions of devices from the frequency-synthesis, forward-error-correction (FEC), and coding and demodulation product families. The book also outlines the custom design service. *The DDS Handbook* offers 216 pages of data sheets and application notes on direct-digital-synthesis products, from ASICs through board- and chassis-level products. *The Spread Spectrum Handbook* is a 189-pg compilation of data sheets and application products. *The Forward Error Correction Handbook* covers FEC encoding and decoding in its 56 pages of data sheets.

Stanford Telecom, ASIC & Custom Products Div, 2421 Mission College Blvd, Santa Clara, CA 95056. **Circle No. 397**

AT/Micro Channel Codas For Waveform Analysis

These five application notes show how you can use IBM PC/AT and Micro Channel Architecture Codas and advanced Codas packages to perform waveform analysis. AN-7, *Applications in Medical Research,* outlines how AT/Micro Channel Architecture Codas and advanced Codas have been applied in medical research. AN-8, *A Closer Look at the Peak Capture Algorithm,* shows how the manufacturer provides a computer-based solution to automatic detection of peak, valley, mean, and period information on periodic waveforms. AN-9, *A Closer Look at Waveform Integration,* demonstrates how you can apply the package's rectification and integration functions to waveforms, such as aortic blood flow, to measure blood volume and other physiological parameters. AN-10, *Measuring High Voltage Signals with AT/MCA Codas,* explains how researchers can use a voltage di-

C&C Computers and Communications

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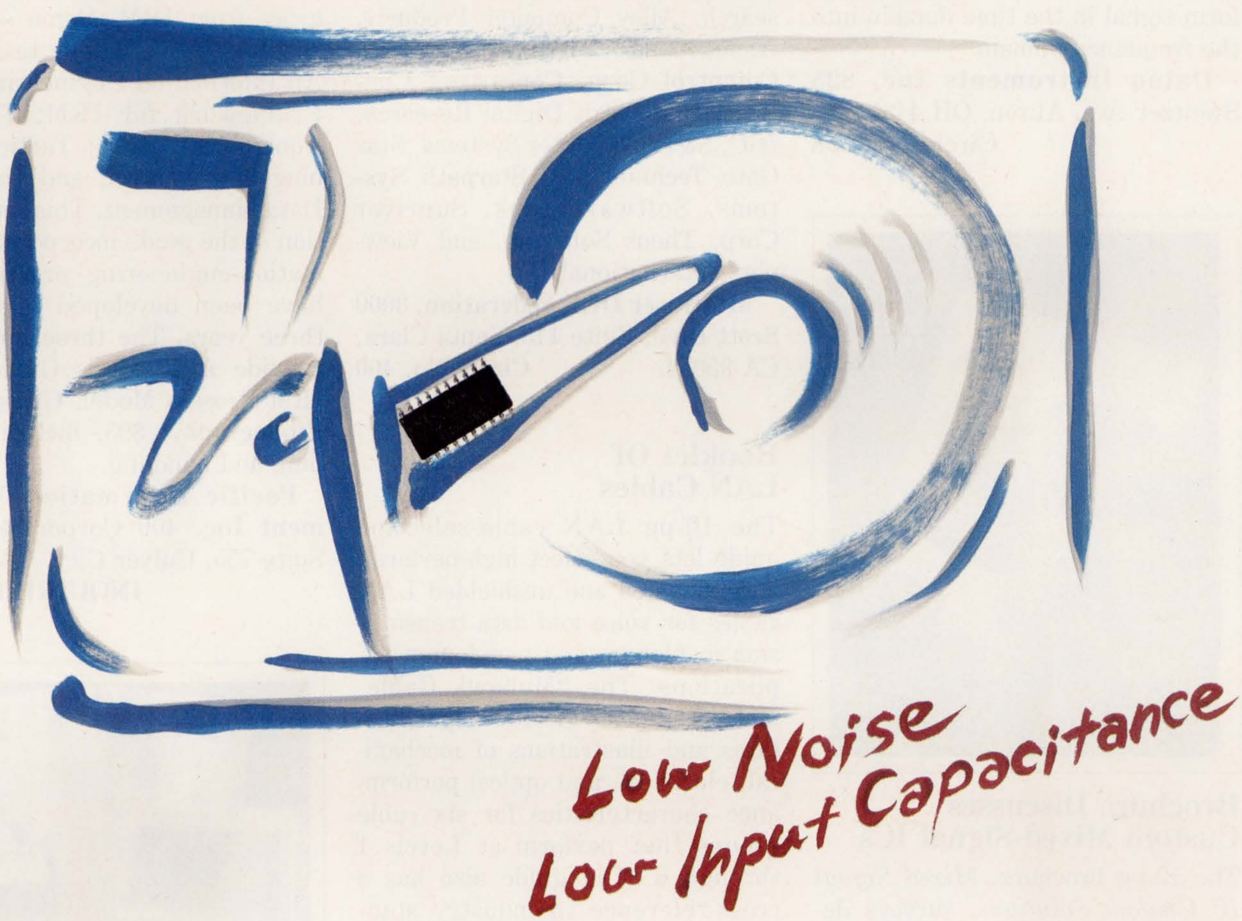

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vider circuit and shunt resistors to measure voltage signals >±5V. AN-11, *Waveform Analysis Using the Fourier Transform,* shows how you can use the AT/Micro Channel Architecture Codas package's Fourier-transform algorithm to mathematically convert any waveform signal in the time domain into the frequency domain.

Dataq Instruments Inc, 825 Sweitzer Ave, Akron, OH 44311.
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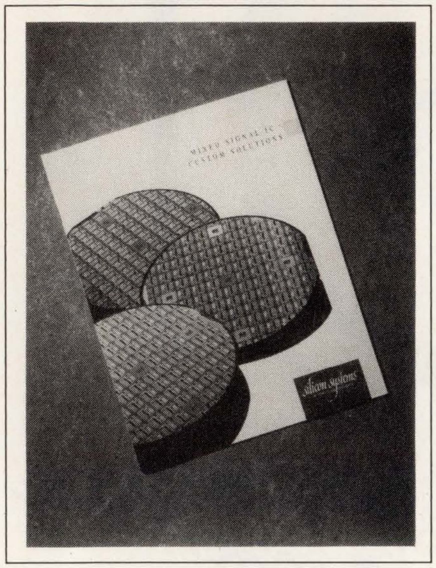

Brochure Discusses Custom Mixed-Signal ICs

The 12-pg brochure, *Mixed Signal IC Custom Solutions,* surveys design approach, computer-aided tools, process technologies, fabrication capability, and assembly operation. Easy-to-read charts compare and contrast design approaches and processes. A flow chart shows how the step-by-step approach allows satisfactory custom solutions.

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680.
Circle No. 399

Directory Provides Plethora Of Information

The Multiuser DOS Directory is a comprehensive guide to text- and graphics-based DOS work-group solutions for computer users, resellers, system integrators, and information systems managers. It presents multiuser DOS software environments, multiport serial boards, and multiuser graphics-display adapters. The directory describes products from Advanced Micro Research, Alloy Computer Products, Arnet Corp, Bluebird Systems, Comptrol Corp, Concurrent Controls, Digiboard, Digital Research, IGC, S&H Computer Systems, Star Gate Technologies, Starpath Systems, Software Link, Sunriver Corp, Theos Software, and Viewport International.

Multiuser DOS Federation, 3000 Scott Blvd, Suite 115, Santa Clara, CA 95054. **Circle No. 400**

Booklet Of LAN Cables

The 10-pg LAN cable-selection guide lets you select high-performance shielded and unshielded LAN cables for voice and data transmission in plenum and nonplenum applications. The "Mohawk Cablemate Planner" includes specifications and illustrations of mechanical, electrical, and optical performance characteristics for six cable groups that perform at Levels 1 through 6. The guide also has a cross-reference to industry standards for Levels 1 through 6.

Mohawk Wire And Cable Corp, 9 Mohawk Dr, Leominster, MA 01453. **Circle No. 401**

Guide To Information-Engineering Management

The Information Engineering Management Guide explains how to make a smooth transition from the information-research-management (IRM) philosophy of traditional data processing to the information-engineering approach. The guide provides a function-oriented "road map," showing how to introduce information engineering to an enterprise. It shows how you can augment current management practices; how to smoothly introduce information engineering into the current environment; and how to gradually increase the use of information engineering and control the pace of the enterprise's transition away from IRM. Some of the 16 chapters in the 280-pg text include An Information Engineering-Based Framework for IRM; The IRM Control Structure; Tactical Planning and Control; and Integrated Data Management. This second edition of the guide incorporates information-engineering practices that have been developed in the past three years. The three appendixes provide A Reader's Guide to the IRM Process Model, Glossary, and Bibliography. $95, including shipping and handling.

Pacific Information Management Inc, 400 Corporate Pointe, Suite 755, Culver City, CA 90230.
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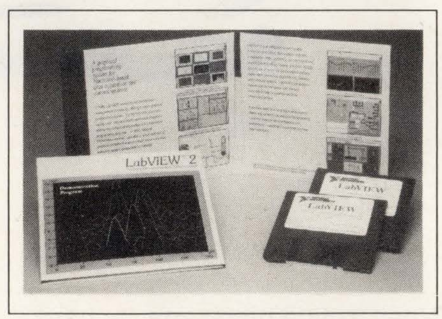
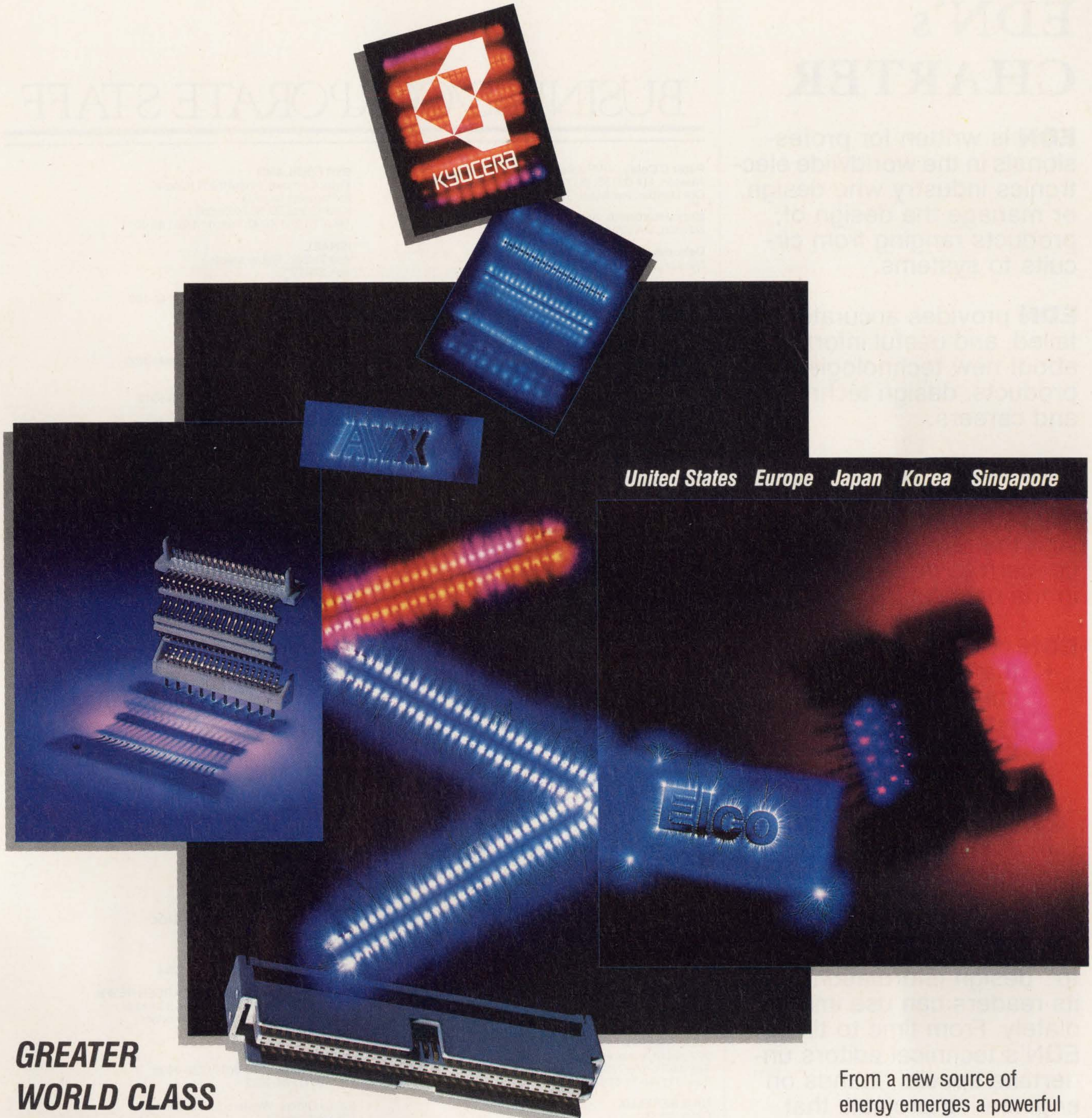


Instrumentation-Software Demo Package

This demonstration package for a Macintosh computer with at least 2M bytes of RAM, 2M bytes of hard-disk space, and a 13-in. monitor provides a "guided tour" of the Labview 2 instrumentation software package. It explains how the software works, shows how to build a virtual instrument (VI), and looks at a completed VI and its components.

National Instruments Corp, 6504 Bridge Point Pkwy, Austin, TX 78730. **Circle No. 402**



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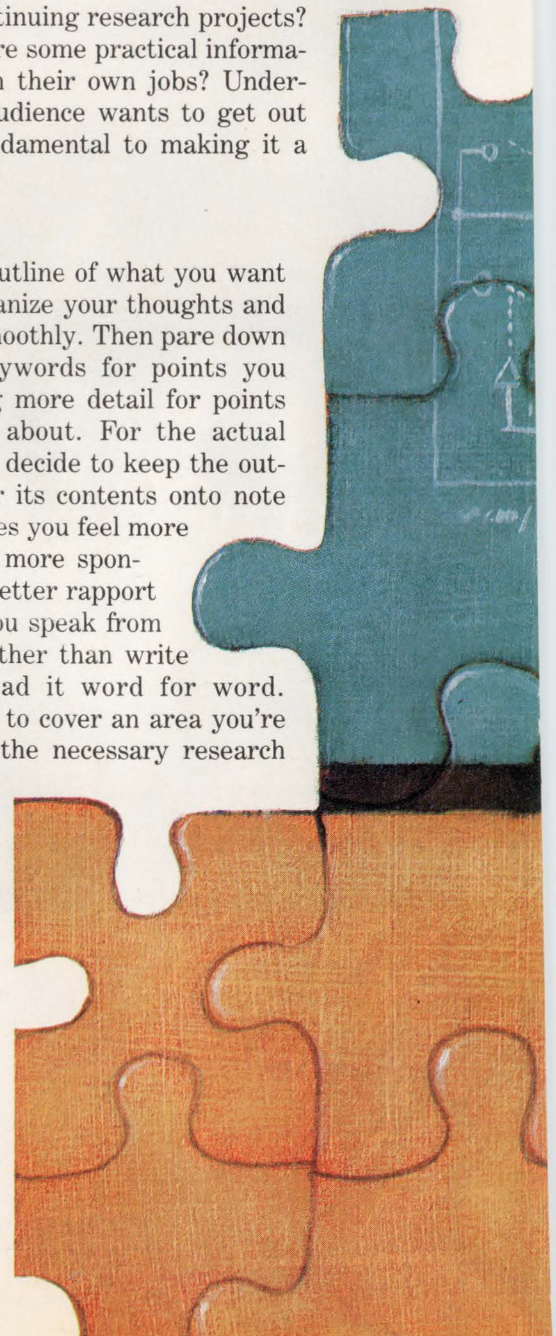
CIRCLE NO. 161

At the next technical conference, don't just sit there

Here's how to put the pieces together to run a successful conference session

Jay Fraser, Associate Editor



Dave Cutler

You see a notice on the bulletin board about a technical conference and decide you want to go. Your manager gives you permission, but then he throws you a curve ball: why just attend the conference when you can present a paper at it?

To humor him, you write a report about the project you're working on and submit it to the sponsoring organization. They like it so much that they want you to chair one of the sessions. Your boss thinks that's just wonderful because it will mean more prestige for the company. But you've never arranged or run a conference session in your life... What are you going to do?

What you're going to do is accept the offer to chair the session, prepare carefully, and make it a success.

Analyzing your audience

Before you deal with your own presentation, the people on the panel, or the facilities you have at your disposal, you have to consider your audience.

Who are you going to be speaking to? Will they be specialists in your field or a general audience? Will they be educators, managers, or engineers who have hands-on jobs?

Your audience should determine how you present your material. For example, if they're specialists, you can assume a basic level of knowledge and use some technical terms without bothering to define them. If they're not familiar with your specialty, you may have to explain the background of your subject first and define specialized terms as you go along.

It's very important to understand why people are coming to your session. Do they want to hear about new inventions? Do they want to stay up to date on continuing research projects? Do they want to acquire some practical information they can apply in their own jobs? Understanding what your audience wants to get out of your session is fundamental to making it a success.

Preparing yourself

Develop a detailed outline of what you want to say to help you organize your thoughts and make your talk flow smoothly. Then pare down the outline, using keywords for points you know well and leaving more detail for points you're less confident about. For the actual presentation, you may decide to keep the outline format or transfer its contents onto note cards—whichever makes you feel more comfortable. You'll be more spontaneous and create a better rapport with the audience if you speak from an outline or notes rather than write out a speech and read it word for word.

If your talk is going to cover an area you're not familiar with, do the necessary research to become knowledgeable about it. Audiences catch on very quickly when a speaker is uncertain of his subject.

If you're addressing a general audience, be sure to define the technical terms you use, and even if you are speaking to a group of experts in your field, avoid


CUTLER

jargon. You may think what you are saying is clear, but some specialized words have different meanings in different regions and countries—and even in different companies.

After you've completed the outline, rehearse your speech. That means delivering it out loud. It's best to give the speech to an audience, such as a few of your friends or coworkers, who can offer helpful criticism. If you can't round up an audience, you can speak into a tape recorder and analyze your own performance.

If you're going to use slides or transparencies with your talk, show them to your test audience. Remember to keep your slides and transparencies simple and bold. The information on them should be easy to assimilate and should be legible to people in the rear of the room where you'll be speaking.

Entire books have been written about public speaking, and space doesn't allow for a discussion of all the nuances involved, but keep the following points in mind:

- Make and maintain eye contact with your audience. Don't bury your head in your notes and mumble, and don't stare at the ceiling. Move your eyes to different sections of the audience as you speak. Try to make everyone in the audience think you're talking to him or her personally.
- Be aware of how the audience is reacting to you and respond to them accordingly. If they're whispering among themselves, they could be bored. Pick up the pace of your talk, ask the audience a question, or make a joke. If you see blank looks on their faces, they may not understand what you're talking about. Clarify what you've already said. If they're fidgeting in their seats, the session may have gone on too long. Call for a coffee break.
- Don't deliver your speech in a monotone. Vary the pace and volume of your voice. Use humor—if you're good at it—and use anecdotes to illustrate your points. The audience will respond better to you if you include some personal experiences in your talk than if you speak exclusively about abstract concepts.

Understanding what your audience wants is fundamental to success

- Use visual aids if they're appropriate. After you organize your speech, see where they would be most helpful. Don't start with some flashy visual aids and try to build your talk around them. Also, try not to overdo them. Don't use a 15-minute videotape where two or three transparencies projected on a screen would do. Visual aids are supposed to help convey your ideas, not draw attention to themselves and divert the audience from what you're trying to say.

Preparing the other speakers

If you're lucky, you may be allowed to select the other people who will make up your panel. However, it's much more likely that the sponsoring organization will choose the other speakers. When you receive their names, call them up and introduce yourself. Go over the basic information about the conference—where and when it will be held, when your session will start, what the topics will be, how long each speaker will have, and how long they will have to answer questions from the audience.

Ask each person on your panel for an outline of his or her presentation—including graphics— and set a deadline for receiving them. Relay panel members' visual-aid-equipment needs to the conference organizers. Use the outlines to familiarize yourself with the topics and write your introductions. Checking the outlines also enables you to make sure your speakers are covering their subjects thoroughly and not repeating each other.

The same rules about delivering a speech apply to all of the panelists. Give them some guidance if they need it. Also, ask them for suggestions about how to run the conference session. They may have more experience than you do.

Finalizing the details

When you arrive at the conference center or hotel, take a look at the room where your session will be held. Test the sound system and make sure all the necessary equipment is there for the visual aids you and your speakers are going to use. Also make sure there are spare bulbs and fuses on hand.

When you talk to the conference organizers, ask them to keep outside interruptions to a minimum during your panel's presentation. Arrange to have a person take telephone calls and messages for people attending your session.

As soon as you can, get together with the other people on your panel. Go over your plans once more and show them the introductory material you've written. They may have corrections or additions to their degrees, titles, or work experience. Don't take anything for granted. Be certain that before they leave, everyone knows the time and the place of the session.

Some conference centers make rooms available for rehearsals. Take advantage of them. Having your panelists give their speeches in advance will help you smooth out

any rough transitions and make sure you're staying within the allotted time.

When it's time to begin, begin on time. It's unprofessional to start late, and a delay will only irritate the audience. Your opening remarks should kindle the listeners' interest and set the tone for what's to follow. Explain why the session will be important to them. Tell them about the information they will receive and the practical knowledge they will gain.

Your opening remarks should also include an acknowledgment of the sponsoring organization and its chairman or president. If time will be set aside for questions after the speakers are done, mention that too.

It's not a good idea to pass out printed material at the beginning of the session. The members of the audience will thumb through it or start to read it and not pay attention to what the speakers are saying. Paper shuffling is another distraction you can easily eliminate.

After you introduce your panelists, listen to them as they speak. Make sure they don't run over their time limits or drift off their subjects. Also, think up a question to ask each one. Sometimes audience members may be reluctant to ask anything at first. A question from you could break the ice.

When the question and answer period is over, make your closing remarks. You should briefly summarize what has been said and thank the speakers and the audience. You might also explain to the audience where they can get more information on the topics that were discussed. Try to end on time. Your audience will appreciate your consideration for their other commitments.

Following up

After your conference session is over, you should evaluate it. You never know, if you successfully chair one session, you'll probably find yourself on the podium again sometime. Analyze your own performance as a speaker and as a leader. Ask yourself what went well, what didn't, and how you could have improved the meeting.

Of course, you may not be the most objective judge of how you handled the session. If possible, sit down with the other panelists and ask them to critique it.

Don't forget the people the session was held for—the audience. If you have the time, mingle with them after the meeting. Answer their questions and ask them what they liked or didn't like about the presentation.

You could also ask the audience to fill out a questionnaire. It should be brief and have space on it where they can write their personal opinions. You can have names and addresses optional, that way you'll probably get more response. And let the audience take the questionnaire home, if they like, and mail it to you later.

Planning and running a conference session takes some effort. It also involves skills you might not use on your job every day, such as public speaking and organizing people. But when the session goes well and the audience leaves with new knowledge and ideas, it can be a very satisfying experience. EDN

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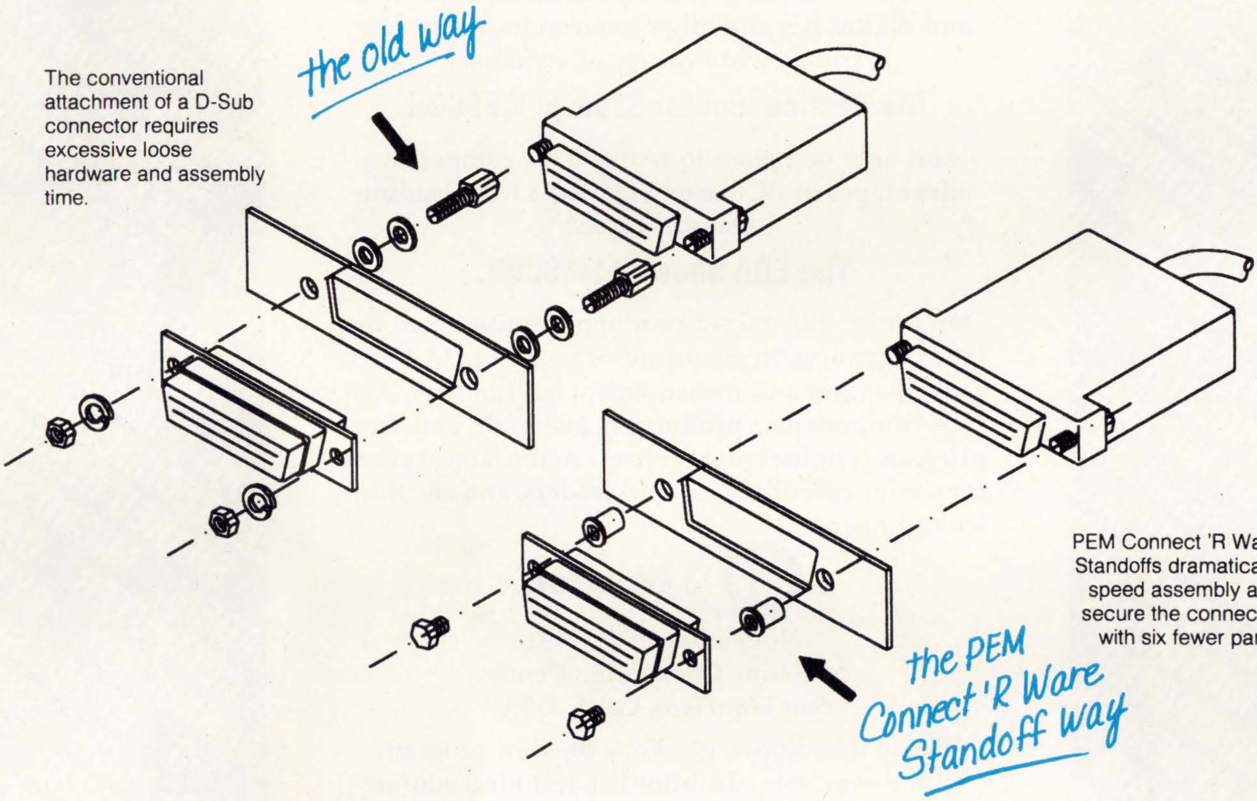

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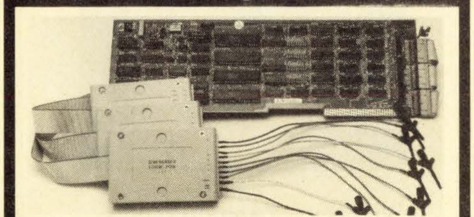

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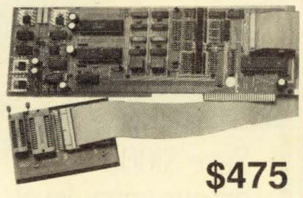

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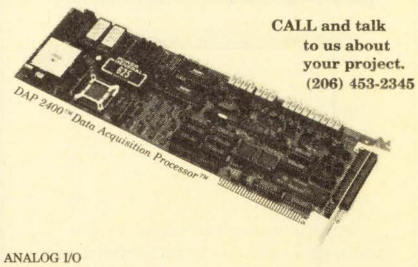

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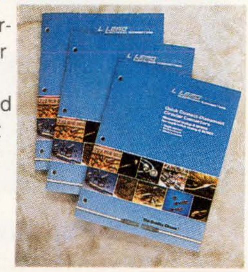

LEMO's new circular connector catalog highlights expanded shell and insert designs. Insert configurations are available in single, multi or mixed designs including signal, coaxial, triaxial, high voltage, fiber optic and fluidic/pneumatic. Shell styles are available in standard chrome plated brass, anodized aluminum or stainless steel.

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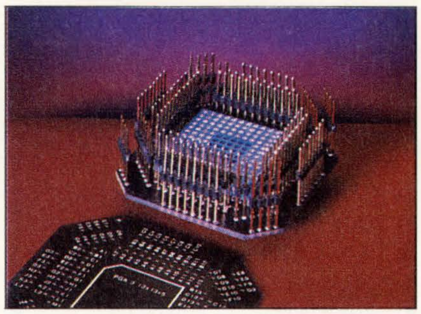

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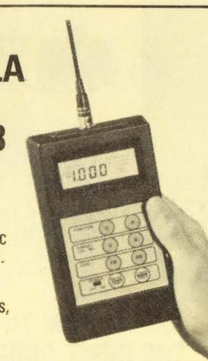

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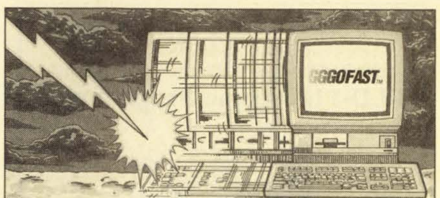

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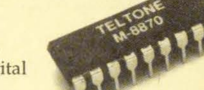

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1991 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	Oct. 1	Sept. 5	Computers & Peripherals/Networks, DSP Chip Directory • ICs & Semiconductors/ Memory Technology, Instrumentation
News Edition	Oct. 3	Sept. 13	ICs & Semiconductors, Multimedia**
Magazine Edition	Oct. 10	Sept. 19	Test & Measurement Special Issue, Oscilloscopes, VXI Board Directory • CAE/ASICs, Sensors & Transducers •
News Edition	Oct. 17	Sept. 27	ATE/Board & IC Testing, Artificial Intelligence**, Regional Profile: New Mexico & Arizona**
Magazine Edition	Oct. 24	Oct. 3	Telecommunications ICs, Graphics & Video Circuits, Computers & Peripherals, Software, Wescon Preview Issue
Magazine Edition	Nov. 7	Oct. 17	High Performance DSPs • CAE/ASICs, Computers & Peripherals/Communications, Software, Wescon Show Issue
News Edition	Nov. 14	Oct. 25	Telecommunications**, Wescon Show Issue
Magazine Edition	Nov. 21	Oct. 31	18th Annual Microprocessor Directory • Test & Measurement, CAE/ASICs, ICs & Semiconductors

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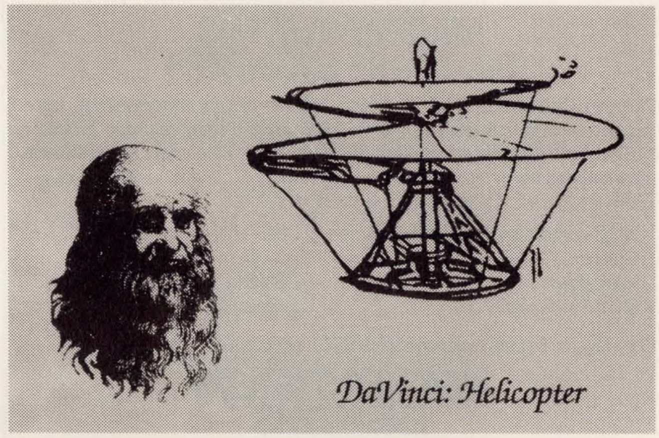

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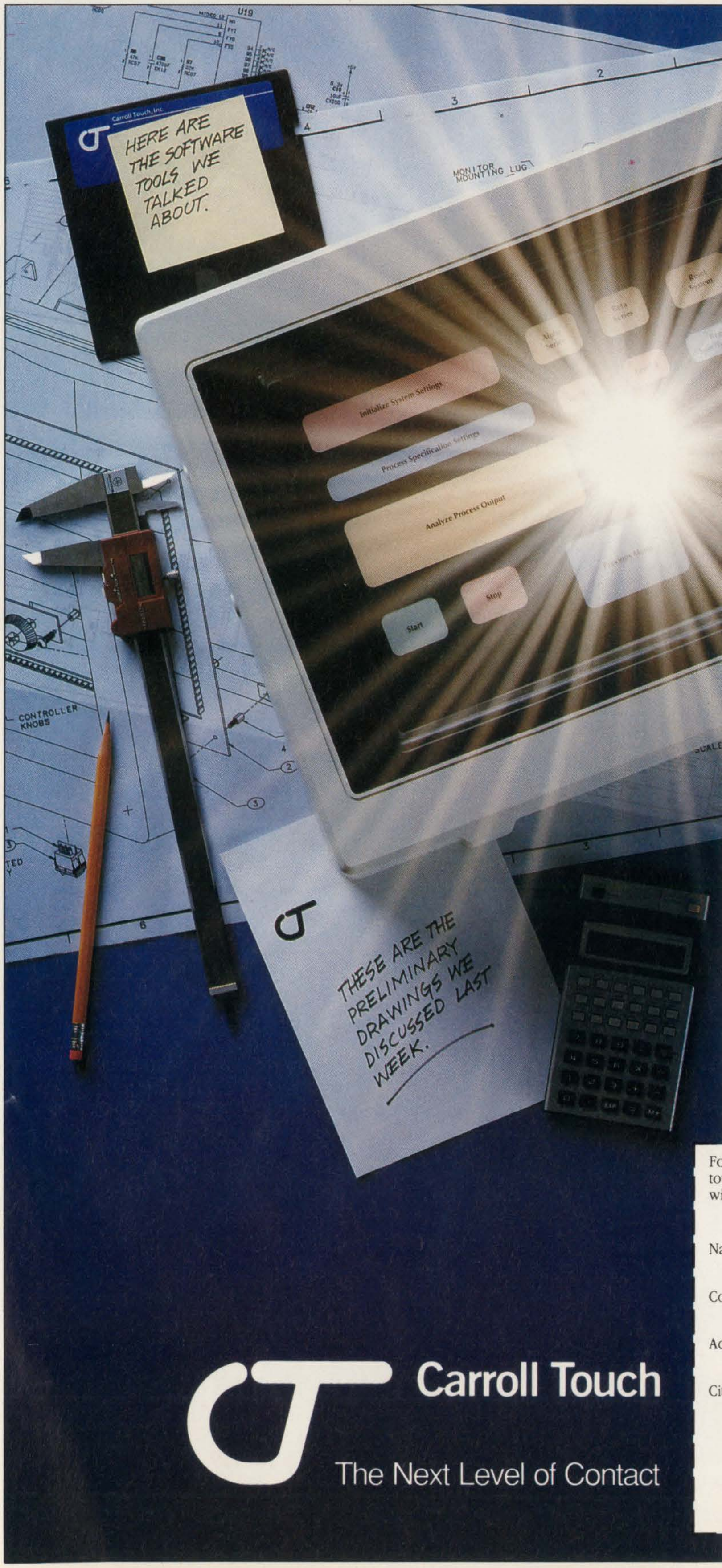

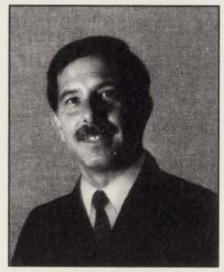

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