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MARCH 1, 1991

EDN®

SPECIAL ISSUE: Communications Technology

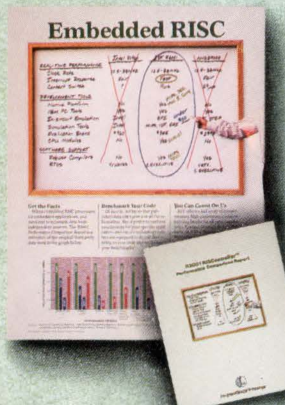
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report: ISDN links product-development parties concurrently

pg 80

Count On IDT

The R3001 RISController™: The Embedded Processing Solution



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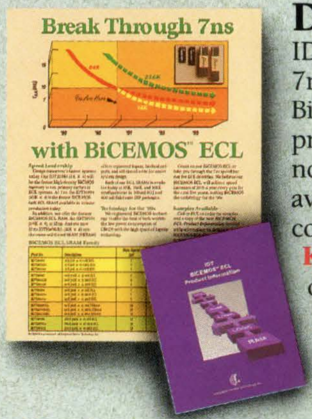

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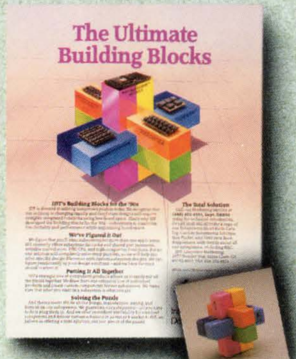

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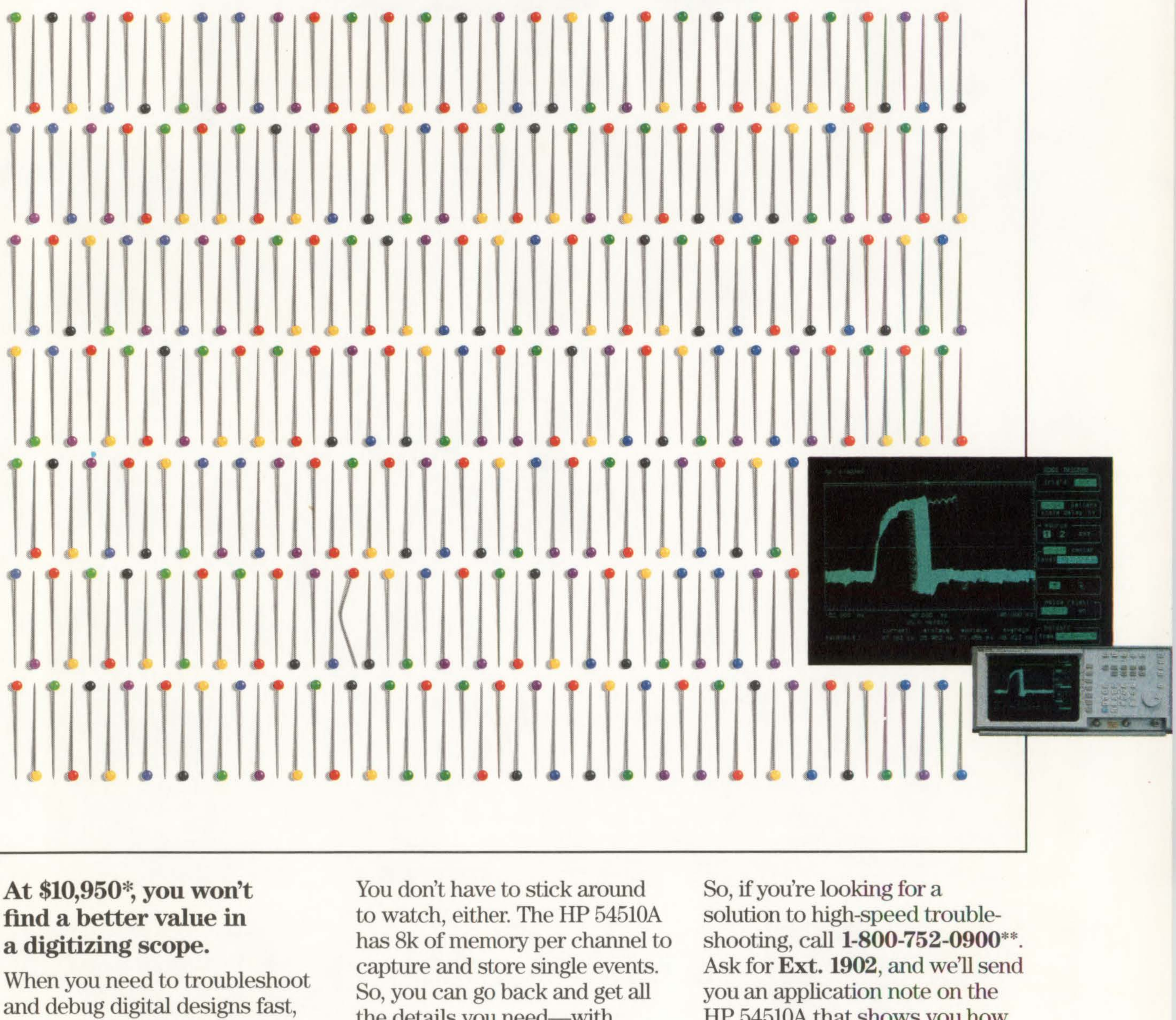

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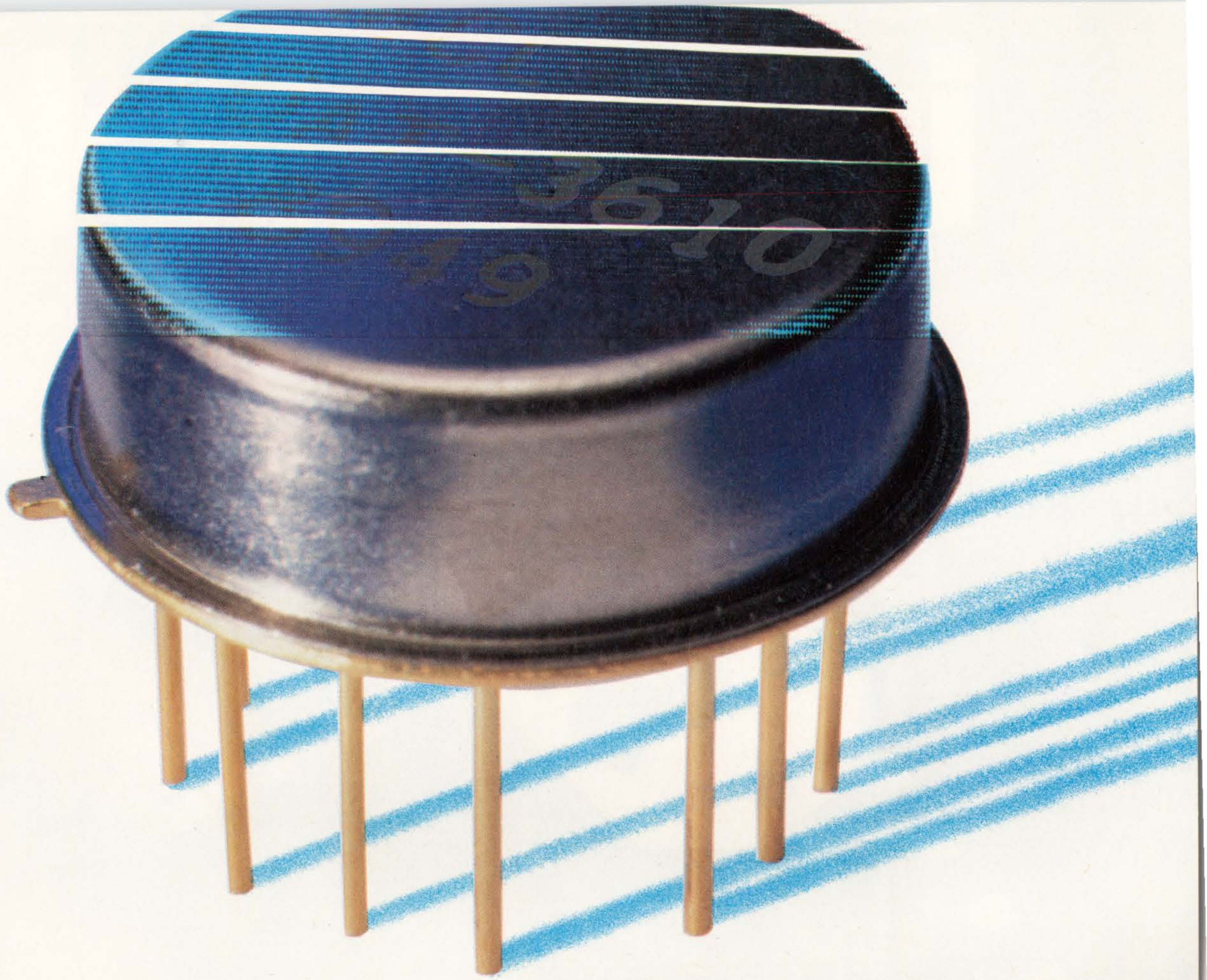

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1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
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1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ		1.4	
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Rise/Fall time, typ (nsec)		3.0	

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Volume 36, Number 5

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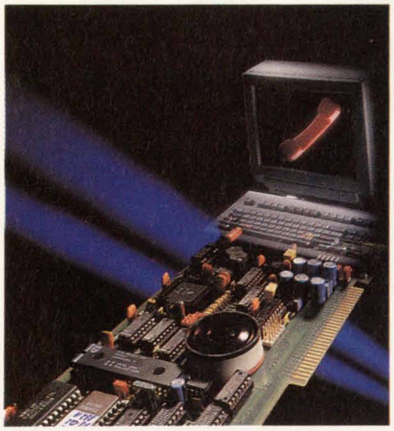
March 1, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Using existing telephone lines, the ISDN (Integrated Services Digital Network) lets marketing, design, test, and manufacturing teams merge their efforts simultaneously. See the Special Report on pg 80. (Photo courtesy Philips Components)*

SPECIAL ISSUE: COMMUNICATIONS TECHNOLOGY

Continued on page 7

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Continued from page 5

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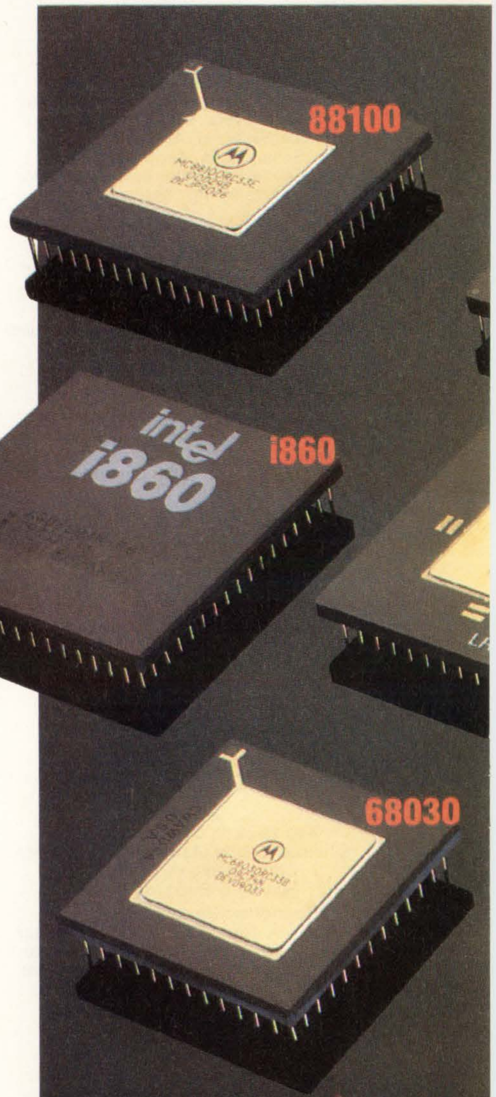

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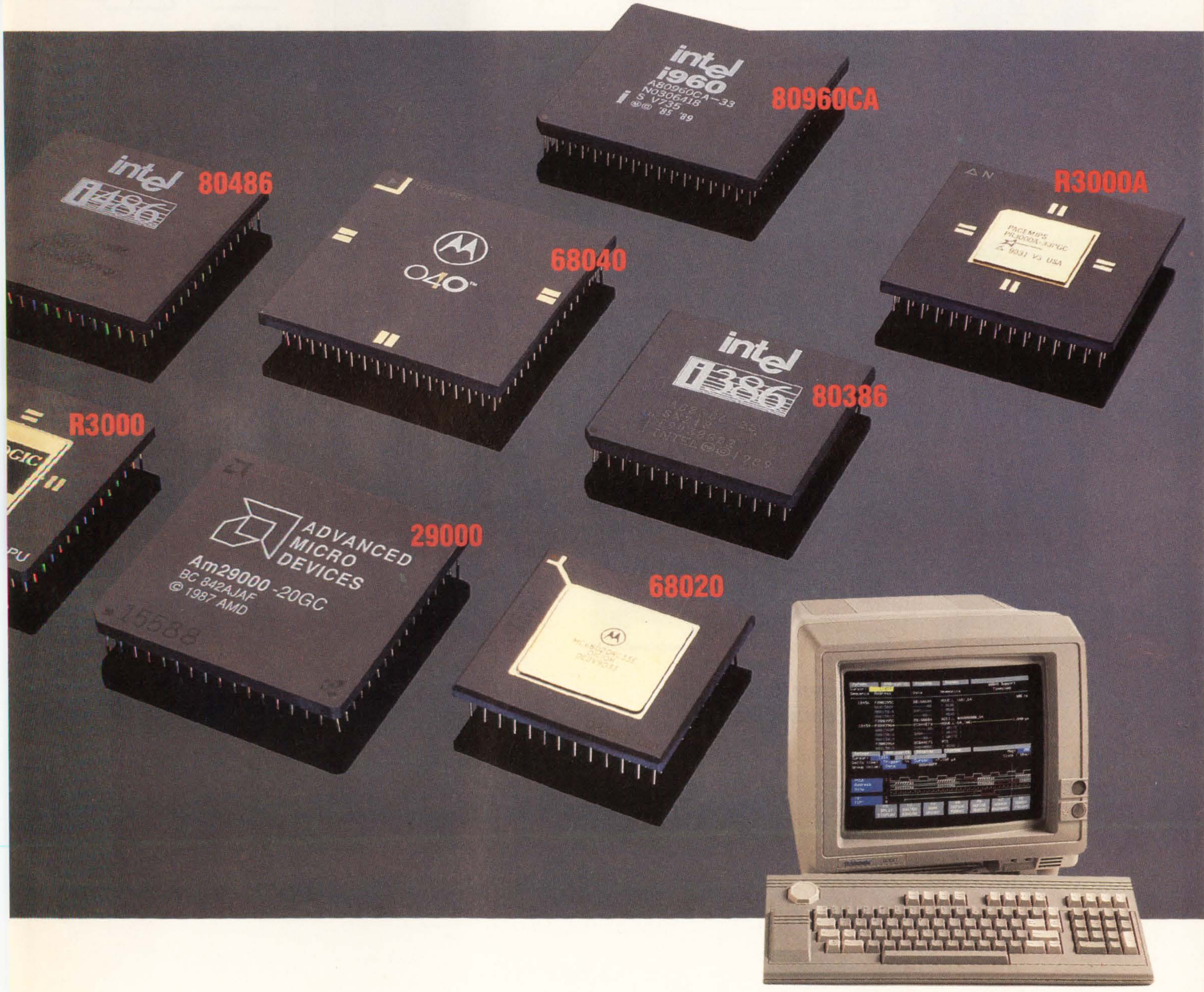

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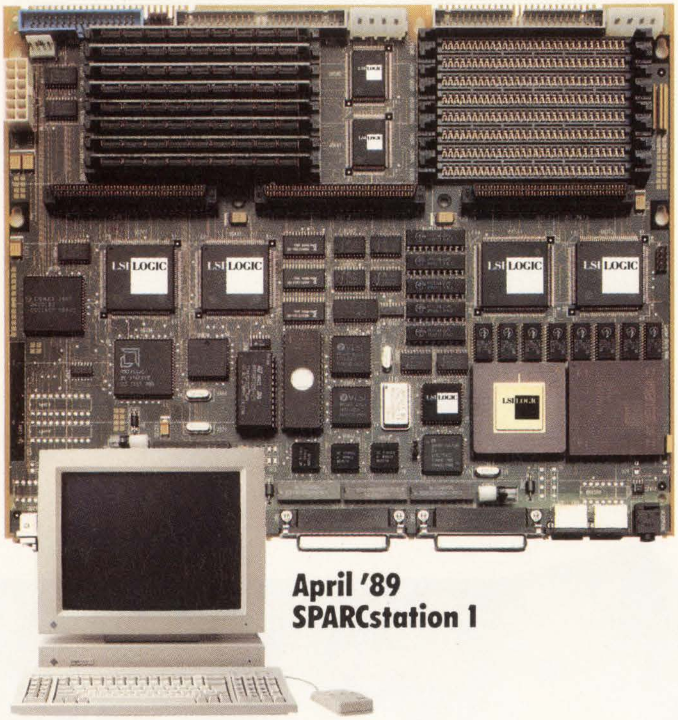
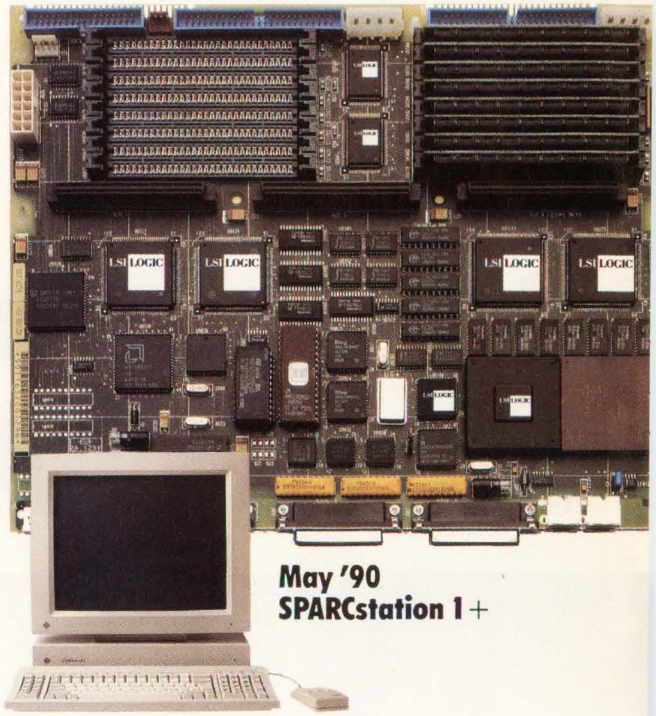
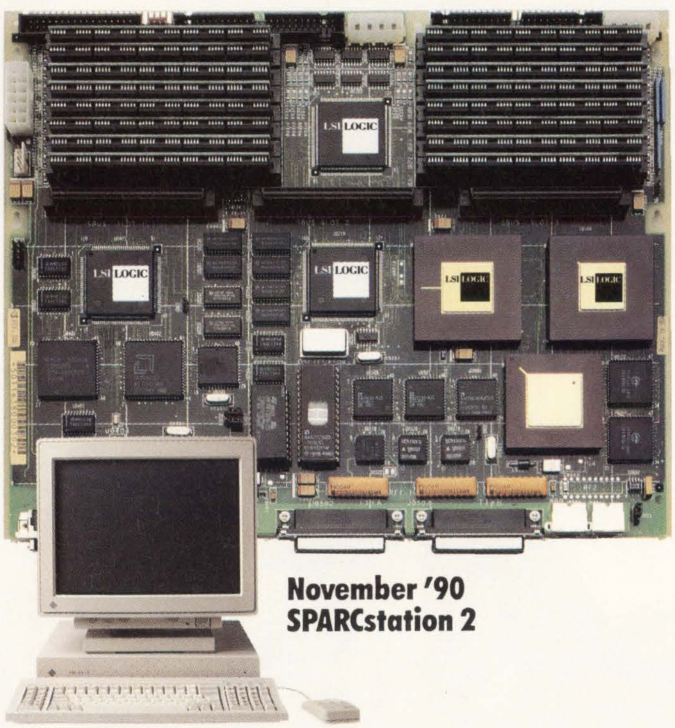


April '89
SPARCstation 1



May '90
SPARCstation 1+



November '90
SPARCstation 2

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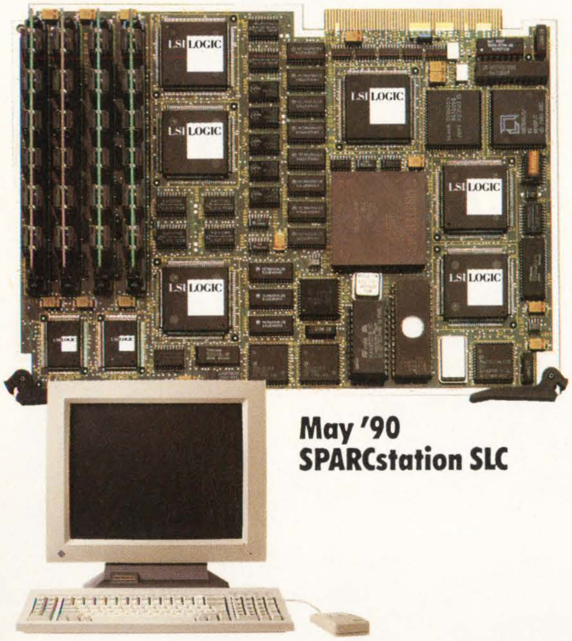

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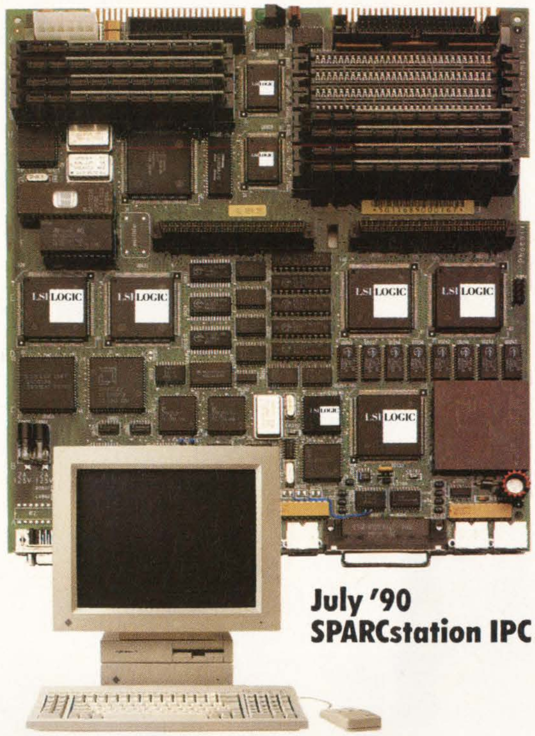
SPARCstation SLC



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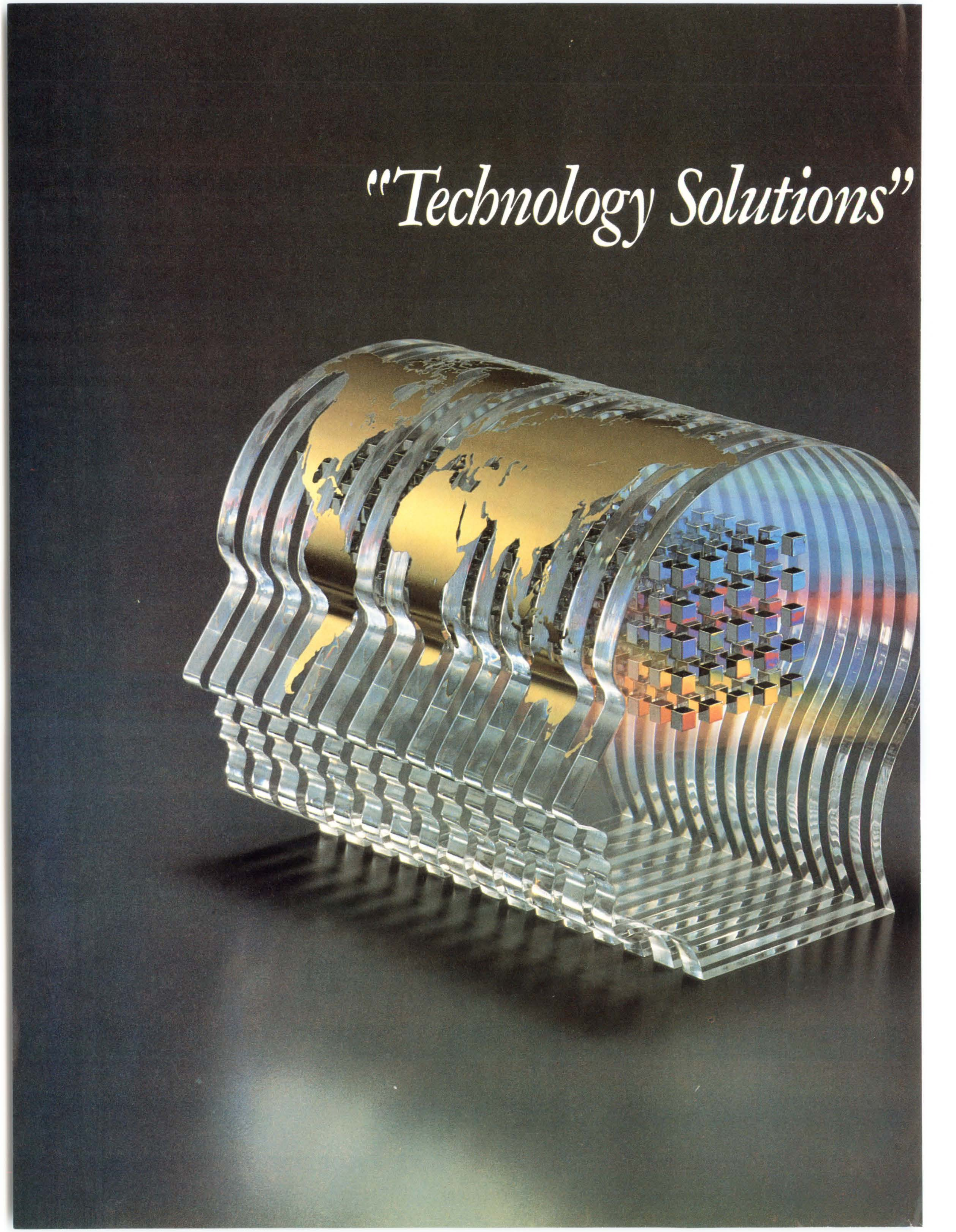
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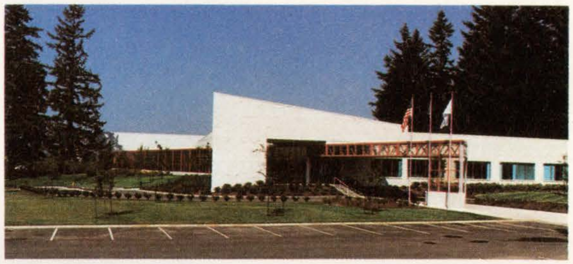

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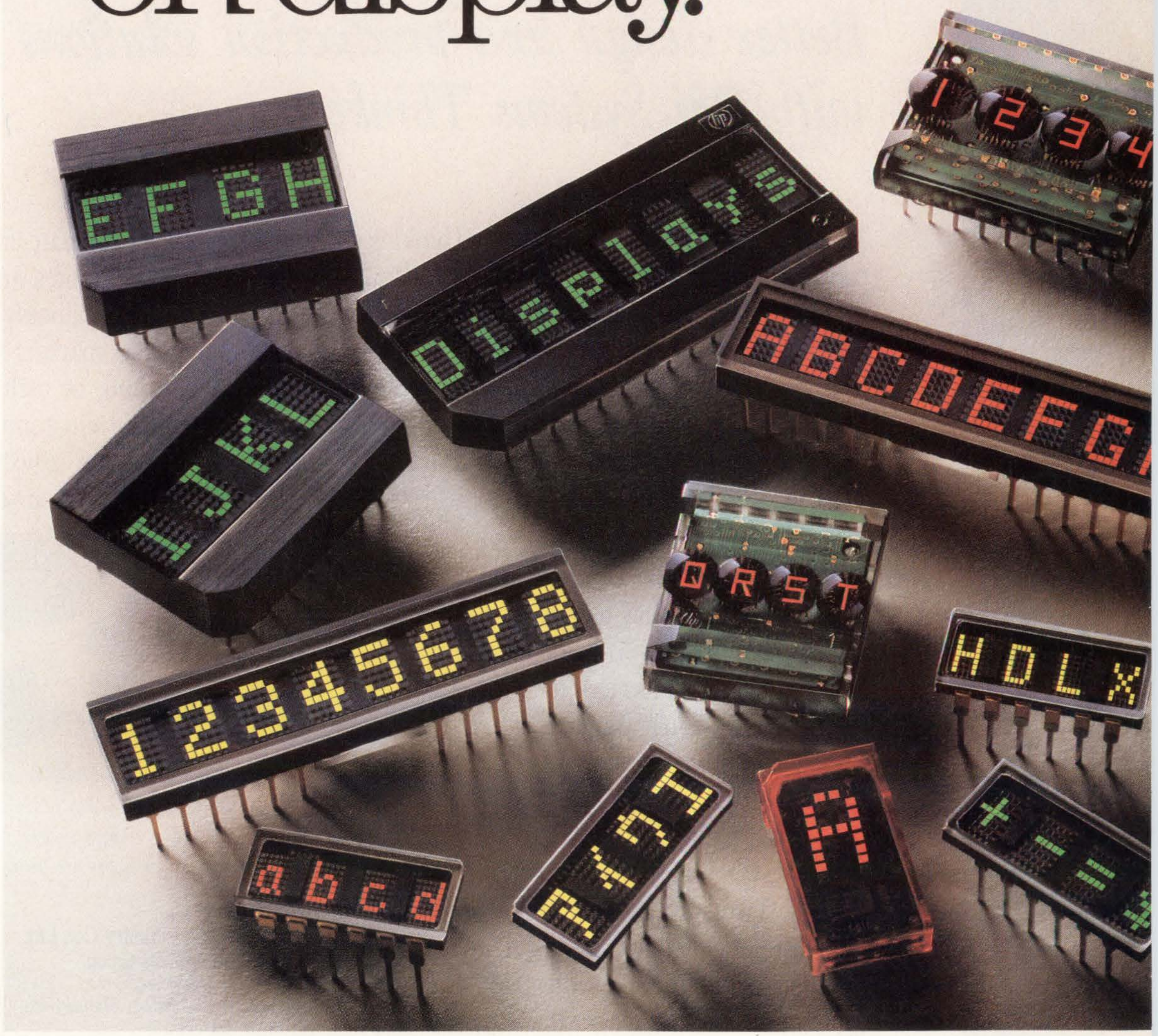

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EDITED BY SUSAN ROSE

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Dataq Instruments' Codas version 5.3 is a computer-based oscillograph for real-time data acquisition and analysis that combines IBM PC/AT hardware and MCA software. The oscillograph can acquire, display, and store waveform data at rates reaching 50,000 samples/sec over as many as 16 channels. The package lets you select from three real-time display modes, a variety of frequency-domain analysis tools, and a built-in statistics program. It also performs automatic date and time stamping, on-the-fly control of all recording functions, X-Y waveform plotting, and channel-by-channel scaling and calibration in any linear unit of measure. You can customize the $2790 system by linking it to C-language programs. Dataq Instruments Inc, Akron, OH, (800) 553-9006, FAX (216) 434-5551.—J D Mosley

REPEATER IC HANDLES TWISTED-PAIR ETHERNET

National Semiconductor's DP83950 repeater interface controller (RIC) for Ethernet hub applications has 13 ports. One port is Attachment Unit Interface (AUI) compatible; the other 12 have integrated 10Base-T transceivers. You can cascade devices to form a hub that contains as many as 832 ports and behaves as a single logical device.

The IC has internal counters and registers that collect network performance statistics, such as time between packets, collision occurrence, and phase-lock errors. It also provides status display signals that let you drive as many as 60 LEDs to indicate the status of each port visually. The IC includes an encoder/decoder and PLL clock-recovery circuits, an elasticity buffer for regenerating preamble codes, and a μP interface. The $145 (100) IC is available in sample quantities. National Semiconductor Corp, Santa Clara, CA, (408) 721-7020, FAX (408) 732-9742.
—Richard A Quinnell

DEVELOPMENT BOARD INCORPORATES FERROELECTRIC MEMORY

After five years of development, you can finally get your hands on nonvolatile memory based on ferroelectric materials from Ramtron Corp. However, you cannot buy the memory chips themselves. Instead, these devices are installed on the company's $4995 FEDS-1 evaluation and development board. This board plugs into an IBM PC/AT bus slot and couples 16 FMx 1208 ferroelectric RAM chips to an Intel 8097 microcontroller. Each chip contains 512 bytes of 250-nsec, nonmultiplexed, ferroelectric-based dynamic RAM (DRAM). The board can operate this memory in two modes: In the dynamic mode, the ferroelectric RAMs operate like DRAMs with unlimited read/write capabilities. In nonvolatile mode, the memory chips will store data for more than one year without power and can endure more than 10^6 power cycles.

The onboard 8097 μC and the host PC have access to the ferroelectric memory. The package includes development software that runs on the host PC and a monitor program that runs on the onboard 8097 μC. The board is a demonstration vehicle for the company's initial ferroelectric parts; the company plans to offer higher-capacity parts later this year. Ramtron Corp, Colorado Springs, CO, (719) 481-7000, FAX (719) 481-9170.—Steven H Leibson

PRECISION OP AMPS FIT IN DIGITAL BITS

Max425 and Max426 CMOS op amps from Maxim Integrated Products use internal nulling for low drift. First, a nulling cycle shorts the op amps' input and determines a correction factor for zeroing the input stages. On-chip control logic stores the correction factor, which remains applied to the input stages via 8- and 16-bit DACs. You can program the 50-msec nulling cycle at power-up, once per minute, or on command. The second nulling technique uses a 300-Hz commutating input stage to minimize the effect of the op amp's input offset voltage (V_{IO}) and 1/f noise. Key maximum specifications are 5-μV V_{IO}, 0.05-μV/°C V_{IO} TC, and 200-pA input bias current. V_{IO} noise in a 0.1- to 10-Hz bandwidth is typically 0.25 μV p-p. Both op amps have 140-dB-min open-loop voltage gain, and a common-mode and power-supply rejection-ratio of 120 dB min. Internal compensation yields gain bandwidths of 350 kHz and 15 MHz for the Max425 and Max426, respectively. Price is $9.50 (100). Maxim Integrated Products, Sunnyvale, CA, (408) 737-7600, FAX (408) 737-7194.
—Brian Kerridge

SCIENTISTS MASS PRODUCE SEMICONDUCTOR LASERS

Scientists at IBM's Zurich Research Laboratory have fabricated between 5000 and 20,000 lasers on a 2-in. wafer by using 1/5000th-in.-deep trenches etched into a semiconductor wafer. In addition to being useful for reading compact discs, printing copy in laser printers, and transmitting information along fiber-optic networks, these lasers might be integrated onto optoelectronic chips that carry data using both light and current. Once etched into the wafer, the lasers are coated with a semireflective material that improves reliability. IBM Research Div, Yorktown Heights, NY, (914) 945-2885, FAX (914) 945-1263.—Michael C Markowitz

ASIC CHIP SET INTEGRATES TOUCH-INPUT TECHNOLOGY

CT ASIC is a 3-chip set of mixed-mode ICs from Carroll Touch. The chip set includes one ASIC, a masked 80C52, and an EEPROM that stores your touch system's parameters. This chip set uses 40% less pc-board space than an equivalent circuit made from discrete components. The chips' phototransistor conditioning circuits handle complex signal-processing functions, such as calibration, gain storage, and ambient-light level tracking. The chip set starts at $2000, which includes 10 hours of engineering consultation and support. You must negotiate a royalty fee and a per-program fee for the schematic. Carroll Touch, Round Rock, TX, (512) 244-3500, FAX (512) 244-7040.—J D Mosley

KIT LOWERS MULTIPROCESSOR DEVELOPMENT COST

The Transputer Education Kit from Computer System Architects includes a PC-based expansion card (which incorporates one Inmos T400 Transputer), a large collection of development software, and 1500 pages of documentation. The $236 kit eliminates one of the many factors impeding multiprocessor system development—the cost of development hardware and software. (Note: You must add 1 to 4M bytes of RAM chips to the board.) The expansion card incorporates five high-speed serial ports for connecting additional processor boards to create a multiprocessor system. Additional processor boards without software, documentation, or memory cost $150. The development software package includes Occam and C cross-compilers; a cross-assembler; a source-level debugger; and example, demonstration, and diagnostic programs. Computer System Architects, Provo, UT, (801) 374-2300, FAX (801) 374-2306.—Steven H Leibson

EMBEDDED CONTROL BOTTLENECKS ARE NOW JUST A FLEETING MEMORY.

New 512K CMOS PROMs optimize performance.

As embedded control microprocessors shift into high gear, you need memory solutions that won't jam up system performance.

With access times as low as 20 ns, our 512K PROMs with fast column access let your microprocessor read right from PROM. For applications from communications and networking to peripherals and avionics, these high-performance, high-density, low-power, CMOS PROMs move embedded control performance into the fast lane.

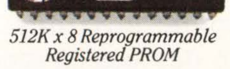
Choose the CY7C285 or CY7C289 for a 64-byte page and WAIT signal that eliminates invalid data. Address latches in the CY7C289 give you the speed you need to support high-speed RISC or CISC microprocessors. Pick the CY7C286 for the highest overall performance available at 50 ns. The CY7C287 offers registered outputs and synchronous operation.

You get higher performance than bipolar PROMs, but the power savings of CMOS.

512K x 8 Reprogrammable Fast Column Access PROM, 20 ns

512K x 8 Reprogrammable PROM

512K x 8 Reprogrammable Registered PROM



512K x 8 Reprogrammable Fast Column Access PROM

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Reduce your board parts count with the CY7C289, featuring an ALE option for synchronous address registers or asynchronous address latches.

Eliminate SRAMs in program store applications. Slim 300-mil packages and on-board registers help you save even more space.

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NEWS BREAKS

COMPLETE DATA-ACQUISITION SYSTEM ON ONE BOARD

The DAP 800 from Microstar Laboratories is an IBM PC/XT and PC/AT data-acquisition board with an 80C188 processor and 256k bytes of buffer memory. The board accepts eight 12-bit analog inputs and provides two 12-bit analog outputs. A programmable gain amplifier offers gains of 1, 10, 100, and 1000. For digital signals, the board has 8-bit input and output ports. The sample rate is 60,000 samples/sec max.

The board comes with software for real-time multitasking data-acquisition and control. The software performs more than 100 standard data-acquisition and -processing functions from closed-loop process control to spectral analysis with fast Fourier transforms. You can also download custom commands from a host computer. Because the board logs and processes data internally, it doesn't slow down the host computer while operating, which frees the host for other activities. The board is $1195. A higher-speed version of the board (100,000 samples/sec) is $1295. A stand-alone version, the DAP 801, which requires a single 5V supply, is $1395. Microstar Laboratories, Redmond, WA, (206) 881-4286, FAX (206) 881-5494.—Doug Conner

SPICE SIMULATOR MODELS SWITCH-MODE POWER SUPPLIES

The PSpice circuit-analysis program, version 4.05, from Microsim Corp makes simulating switch-mode power supplies easier. A cycle-by-cycle simulation of switch-mode supplies is difficult for Spice-based simulators and usually lengthens simulation times. However, this program's behavioral modeling and mixed analog/digital simulation features, which are separately priced options, let you use PWM macro models that simulate the controller section in the digital domain. Other new features include .SAVEBIAS, .LOADBIAS, and .WATCH statements. You can also specify the voltage between two nodes using the .NODESET and .IC statements. Prices for the package start at $950. A power-supply-simulation package costs $3950. Microsim Corp, Irvine, CA, (800) 245-3022, FAX (714) 455-0554.—Anne Watson Swager

VTC VMEBUS CONTROLLERS STILL AVAILABLE

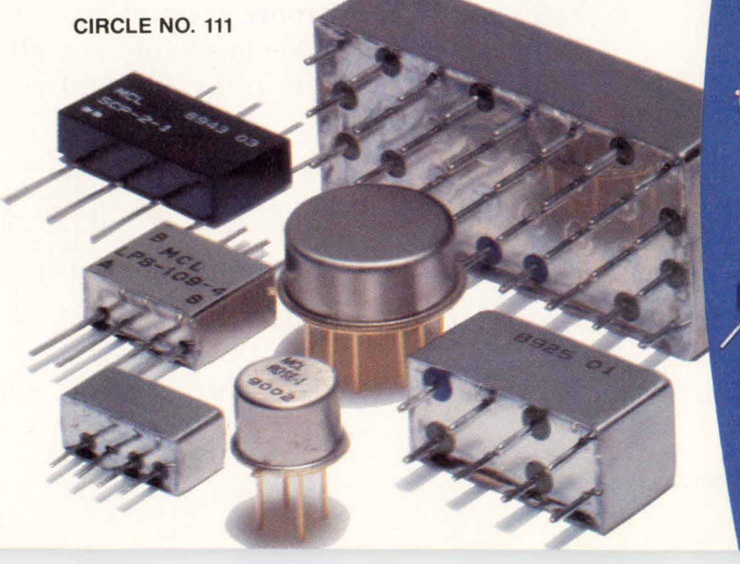
The VIC068 and VAC068 interface and control ICs for the VMEbus, developed by Control Data Corp's VTC facility, are still available. Cypress Semiconductor, the facility's new owner, will operate the plant as a wholly-owned subsidiary, Cypress Minnesota Inc.

The two ICs provide interface and address control for central processors and peripherals connecting to the VME bus. The VAC068 provides address transceivers, address decoding, DMA, and block-level transfer circuitry. The VIC068 handles arbitration, interrupts, and data transfers. Both devices connect directly to CPUs in the 680X0 family, but are usable with other CPUs. In 144-pin plastic pin-grid arrays, the parts cost $126 (100) for the VIC068 and $159 for the VAC068. Cypress Semiconductor, San Jose, CA, (408) 943-2600, FAX (408) 943-2796.—Richard A Quinnell

CAE VENDOR STRENGTHENS HDL OFFERINGS

Viewlogic Systems has enhanced their VHDL (VHSIC hardware description language) software tools with logic synthesis from personal-computer clone vendor Arche Technologies. The software is already integrated into Viewlogic's tools and includes VHDL synthesis, retargeting software, and a technology-library compiler. Viewlogic Systems, Marlboro, MA, (508) 480-0881, FAX (508) 480-0882. Arche Technologies, Fremont, CA, (415) 623-8100, FAX (415) 683-6754.—Michael C Markowitz

Mini-Circuits



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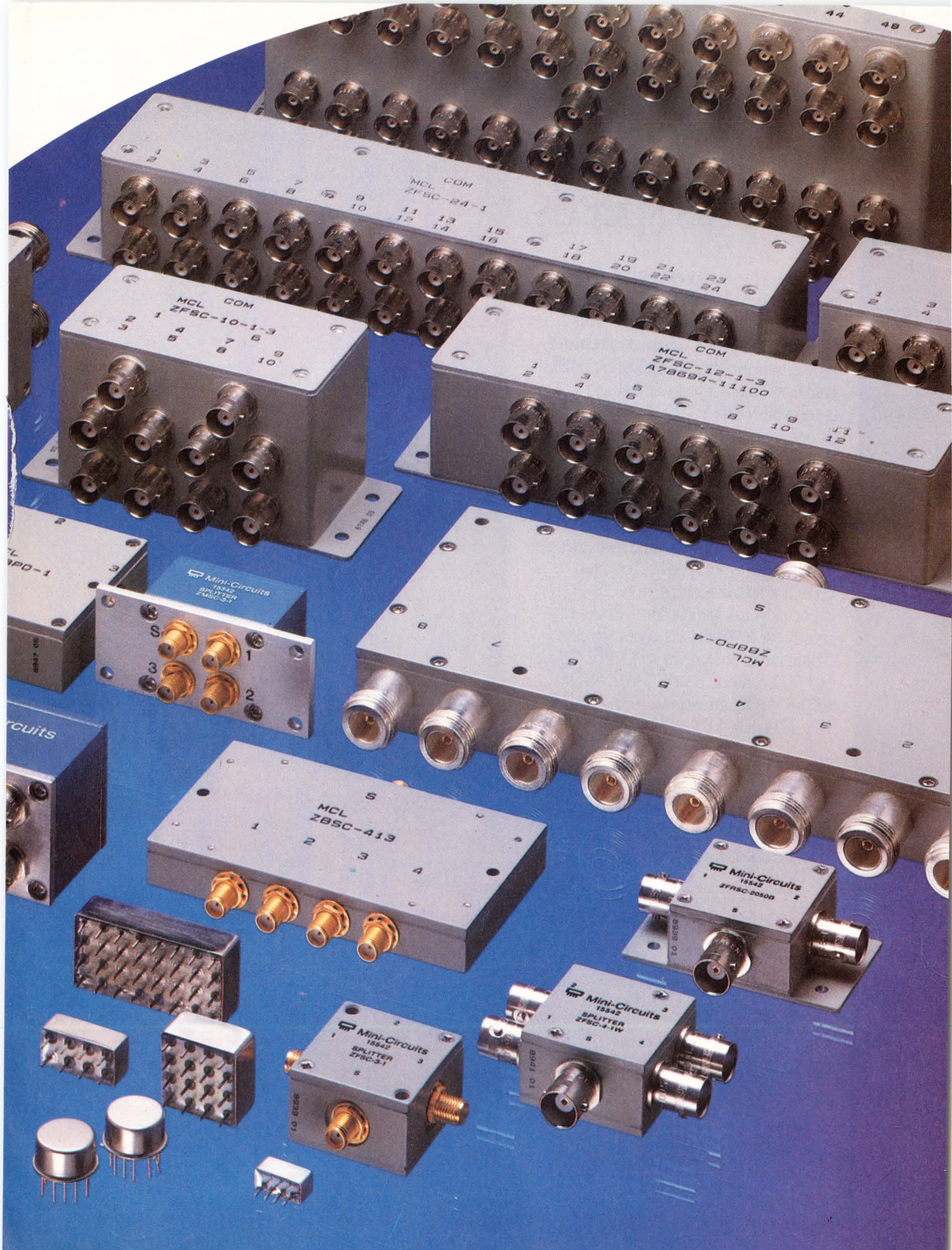
MCL COM
ZFSC-24-1
MCL COM
ZFSC-10-1-3
MCL COM
ZFSC-12-1-3
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15542
SPLITTER
ZMSC-3-1
MCL
ZBPD-4
MCL
ZBSC-413
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15542
ZFRSC-2050B
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SPLITTER
ZFSC-4-1W
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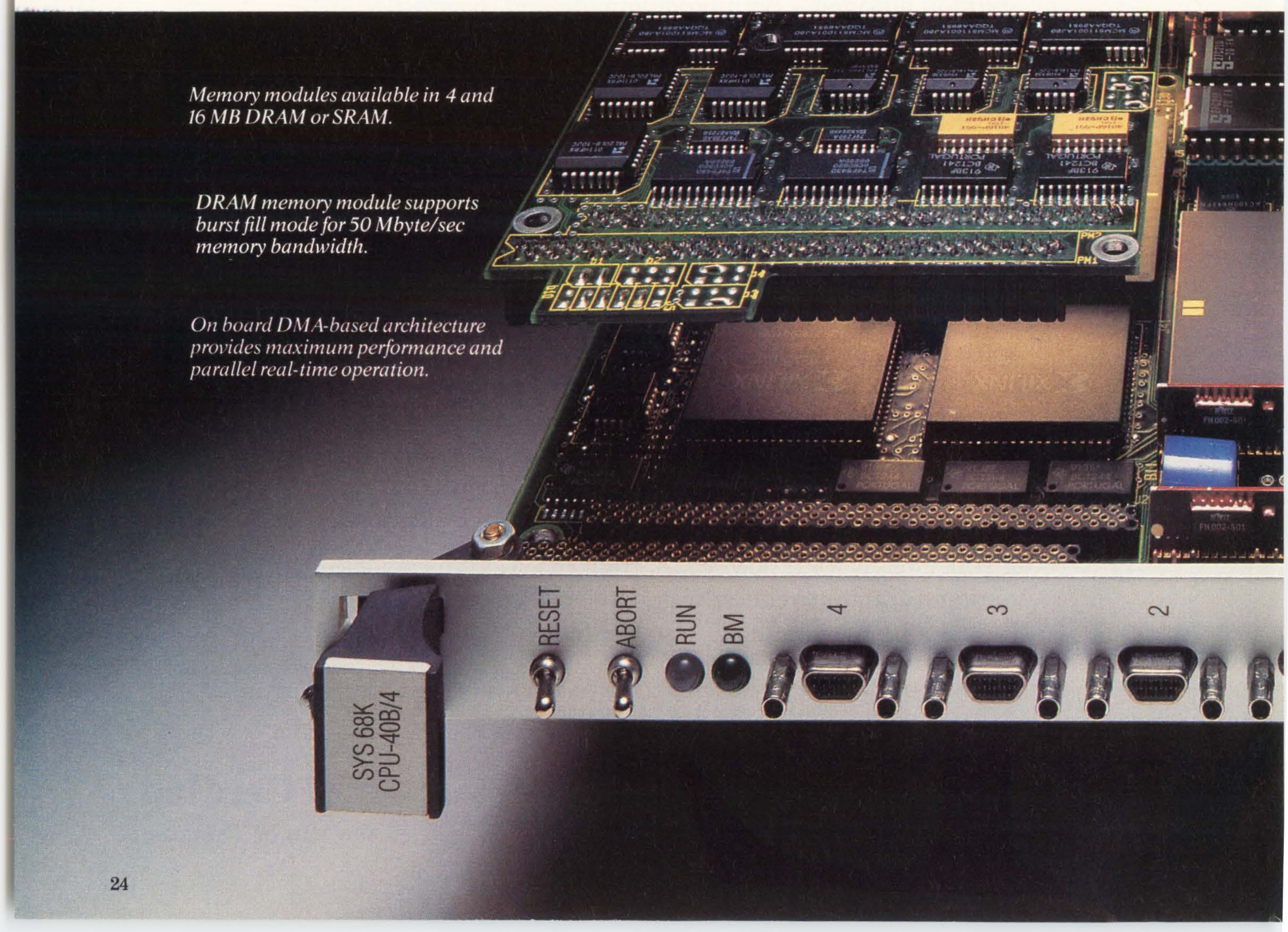
15542
SPLITTER
ZFSC-3-1

WHY THE FIRST 040 VME MIGHT AS WELL BE THE LAST.



Memory modules available in 4 and 16 MB DRAM or SRAM.

DRAM memory module supports burst fill mode for 50 Mbyte/sec memory bandwidth.

On board DMA-based architecture provides maximum performance and parallel real-time operation.

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Of course, we provide comprehensive support with the industry's best-rated documentation,** complete systems integration support and technical assistance.

CPU-40 PERFORMANCE CHARACTERISTICS

Data from	CPU	CPU	CPU	CPU	VMEbus	SCSI*	Floppy Disk*	Ethernet*	Shared RAM*	VMEbus*
Transfer to	Shared RAM	EPROM	Serial I/O Timers	SCSI, Ethernet Controller, Floppy Disk	Shared RAM	Shared RAM	Buffer RAM	Dual-port RAM	VMEbus	VMEbus
Transfer Speed	53.7 MB/sec	16 MB/sec	2 MB/sec	2 MB/sec	5 MB/sec	4 MB/sec	500 KBit/sec	10 MBit/sec	15 MB/sec	15 MB/sec
Local 68040 CPU Operation	100%	100%	100%	100%	70%	80%	100%	100%	75%	100%

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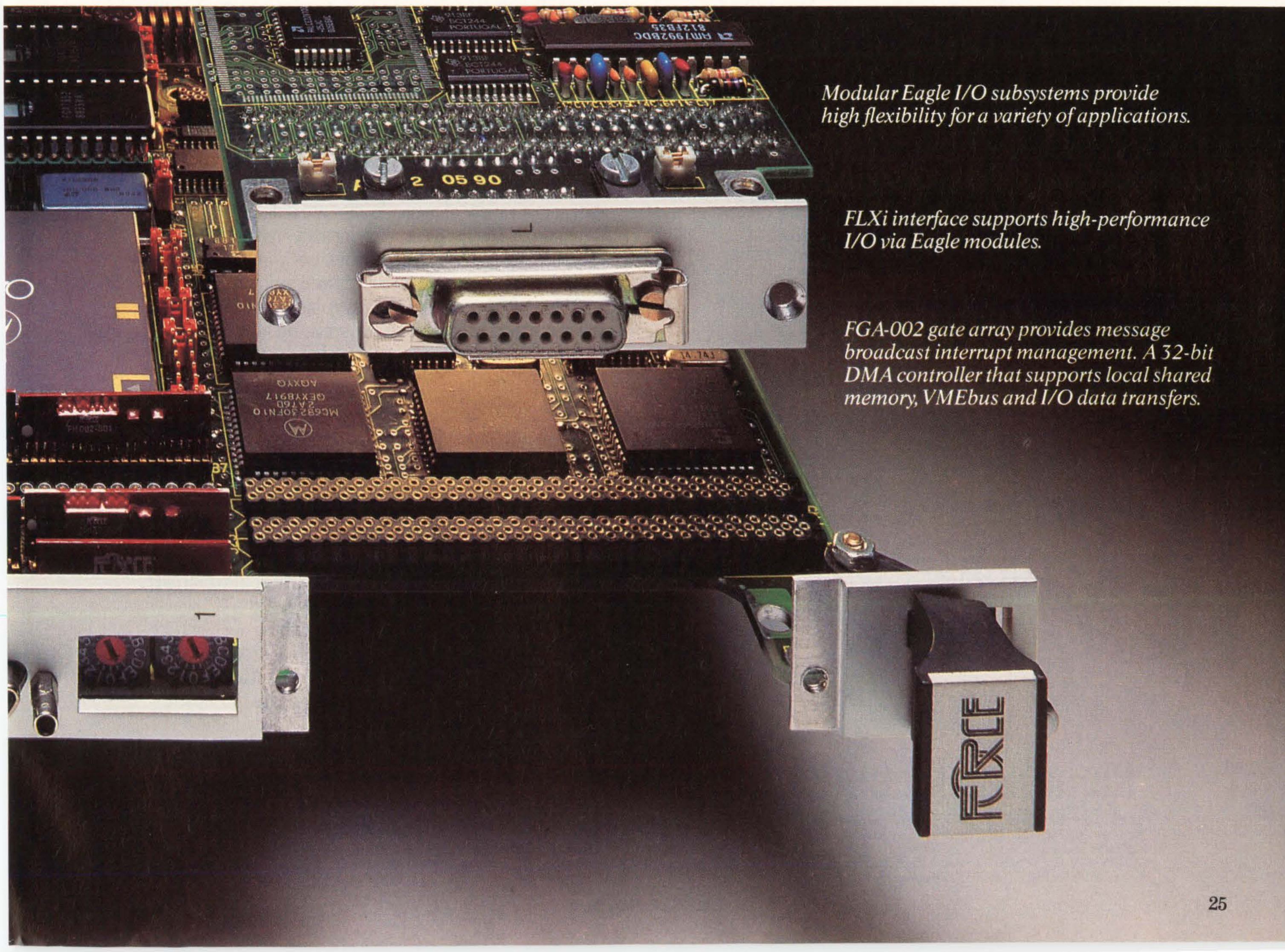
*Actual dhrystone results may vary depending on compiler used. **Computer Design News, March 12, 1990.

CIRCLE NO. 92



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FLXi interface supports high-performance I/O via Eagle modules.

FGA-002 gate array provides message broadcast interrupt management. A 32-bit DMA controller that supports local shared memory, VMEbus and I/O data transfers.

Z I L O G

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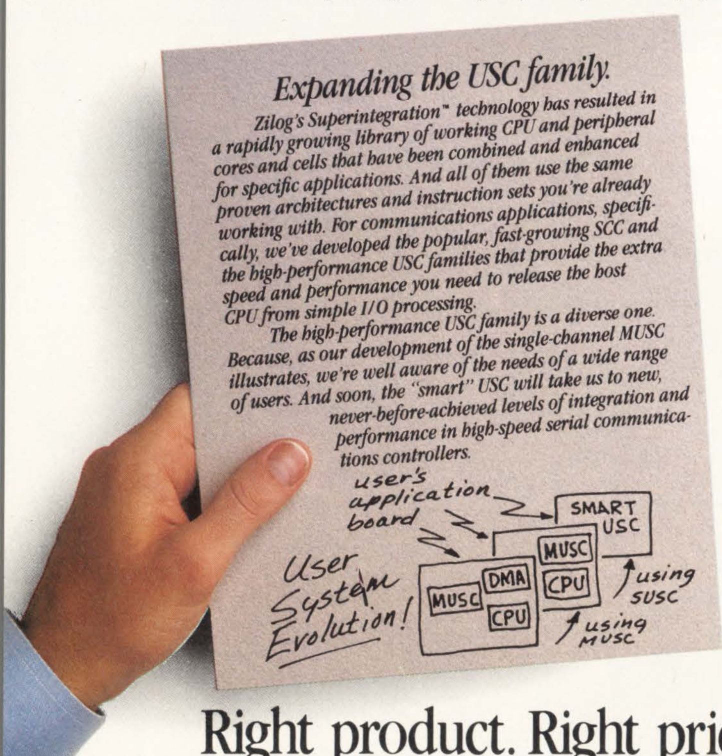
The MUSC's 10 Mbit/sec data transfer rate makes it the fastest single-channel general purpose controller available. CMOS and Superintegration™ give you higher throughput, while helping reduce the CPU workload. And the 32-byte FIFO transmit-and-receive buffers help reduce CPU overhead. So does the fact that the MUSC integrates two time slot assignment cells—one for receive and one for transmit. So data is automatically inserted into programmed time slots, reducing CPU overhead and external logic even more. And all of that frees up more CPU power for the system. The final touch is a separate 8-bit parallel I/O port, ideal for status or displays, that adds flexibility in local control or data presentation.



All the flexibility you need.

The MUSC's multiprotocol design lets you adapt your system to a variety of networks. But not only do you get 10 protocols, you get 8 encoding formats—including asynchronous, bit and byte synchronous, isochronous, Ethernet, and MIL-STD 1553B. And the Open Systems Interconnect (OSI) model features Time Slot Assignment that allows transmission of time multiplexed Synchronous Data Link Control (SDLC) protocol to the ISDN link level.

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Of course, the MUSC comes to you off the shelf, with Zilog's proven quality and reliability. And you have the advantage of CMOS and Superintegration. But you also have the MUSC's unique built-in bus-oriented testability, which allows access to nodes and registers for testing program functionality in real time. And, since dedicated pointer registers provide a window to serial flow during on-line testing, you can test transmission reliability of the controller during system operation.

To find out more about the MUSC or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

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CIRCLE NO. 93

SIGNALS & NOISE

The B-2 is not just an airplane

Regarding the editorial by Jon Titus (EDN, November 22, 1990, pg 31), enough already. The B-2 is not just an airplane; it's a system. It has not just one manufacturer, but many. All share in a piece of the pie. No one, except those who have access to all characteristics and capabilities of the plane, can even come close to making a judgment about the worth of the program. At worst, it's no more than a public-works program.

Nor can anyone, except those with program clearance, even begin to judge the stealth abilities of the plane. It takes complete system knowledge.

As for the SR-71, when has the military ever given up something without getting something in return? Sure, the Black Bird is valuable, but is it as valuable as what has replaced it? I wonder what that replacement is. I bet, if it is a plane, it's pilotless. No Gary Powers to worry about; I'll also bet it can be destroyed—completely—no pieces big enough to compromise its secrecy would be acceptable. Perhaps we'll be commenting about its mothball status 20 years from now.

Defense, no matter how costly, is the only thing our government is obligated to provide. Anything else, like HDTV, is a free ride.

L Alan Kudravy
Hawthorne, CA

What's the correct word?

In the second sentence of the second paragraph of the editorial (EDN, December 6, 1990, pg 51), did Jon Titus mean 'enormousness' rather than 'enormity?'

Bill Woodward
Westinghouse Savannah River Co

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps or less modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200/2400, 8N1 in shorthand.

EDN

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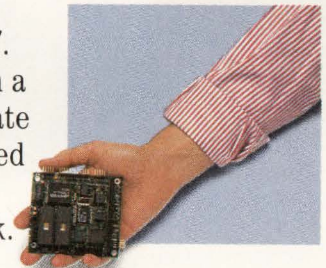

Our CoreModule™ family packs ready-made full PC- or AT-compatible intelligence into 3.6″ x 3.8″ x 0.6″. Just plug one into your circuit board — like plugging in a chip — to easily interface to your own logic. They operate over 0 to 70°C, and include a CMOS CPU, RAM, extended BIOS, Solid State Disk, serial and parallel I/O ports, keyboard and speaker interfaces, and a real-time clock.

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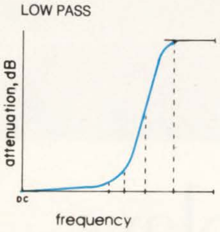
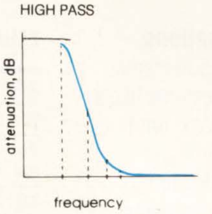


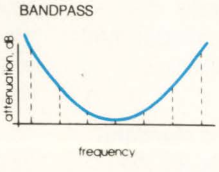
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz



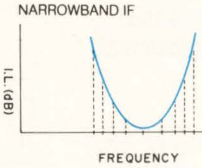
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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Budapest, Hungary

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Bolycore Enterprises USA
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We tracked down three sources of such transmitters

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PC-based layout packages not plentiful

As director of technical services, it is my responsibility to keep my company's CAD capabilities current and adjust them to meet a changing technology. We currently have a CAD system consisting of three Applicon color workstations utilizing a PDP11/34 processing facility with a 216k-byte memory and a Cal-comp 965 pen plotter.

It is a company goal to retreat from the central CPU approach and place a personal computer at each design station. The reasoning was due in part to the inflexibility of a CPU-driven system and the reliance on one piece of equipment. Also, the current business picture does not allow for the purchase of a workstation. I have investigated one software package, Cadisys, which runs on an IBM 386/486, and found it to have limited autorouting capabilities. I have reached a dead end in trying to locate other PC-based layout packages for hybrids. Your assistance in this search would be greatly appreciated.
Len Giambald
ILC Data Device Corp
Bohemia, NY

Mike Markowitz found the quasi-definitive word on PC-based hybrid software packages: According to Jim Hill of Layout Concepts (Boca Raton, FL, (407) 241-2823), Cadisys Corp's (San Jose, CA, (408) 441-8800) Cadisys is currently the best—and only—PC-based hybrid layout package. Layout Concepts has written a PC-based hybrid batch router, but the software needs another company to integrate it with tools that provide placement, support, and a user interface.

Don Davis of Accel Technologies, (San Diego, CA, (619) 554-1000) claims you can get away with using pc-board software from Accel, CAD Software (Littleton, MA, (508) 486-8929), and Orcad Systems Corp (Hillsboro, OR, (503) 640-9488) for mixed A/D hybrid designs. Unfortunately, Davis thinks that for ceramic substrates, you'll have to use a workstation.

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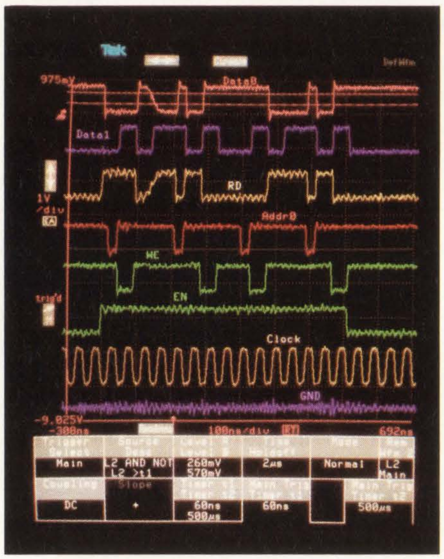

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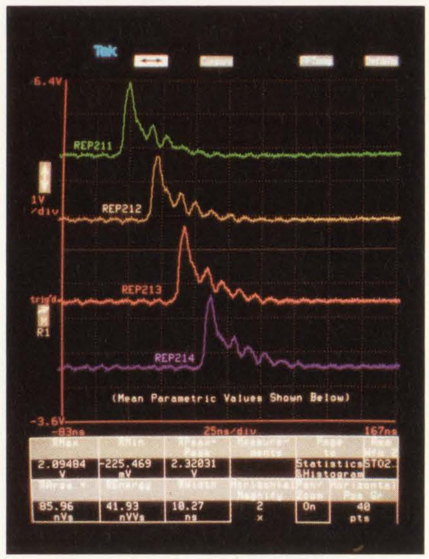

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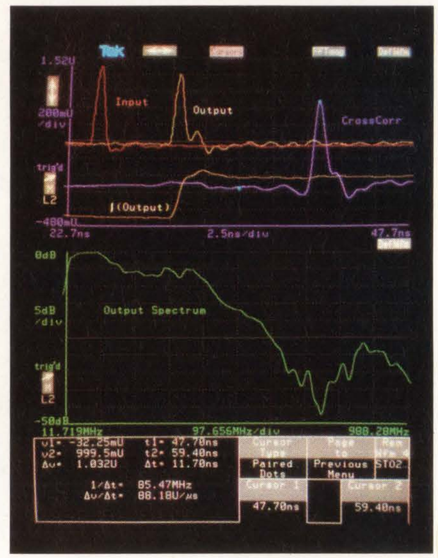

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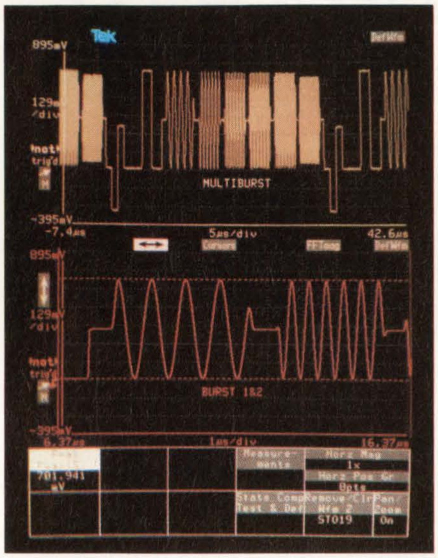

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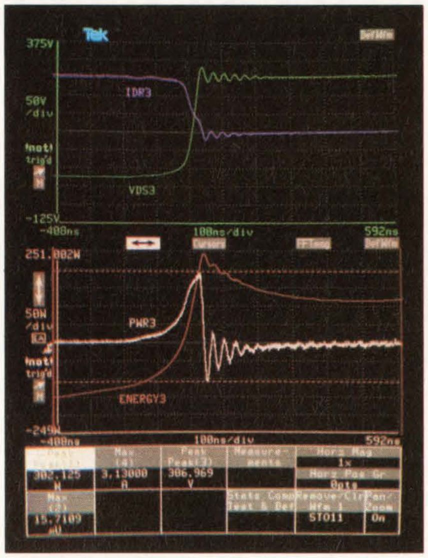

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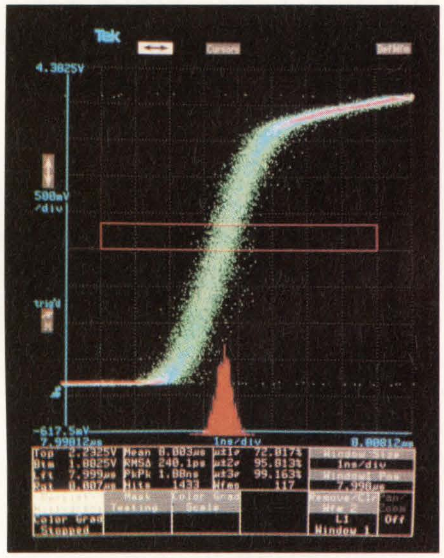

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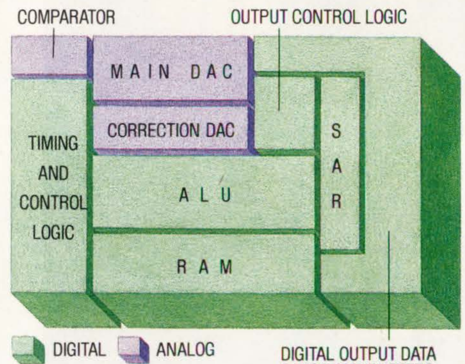

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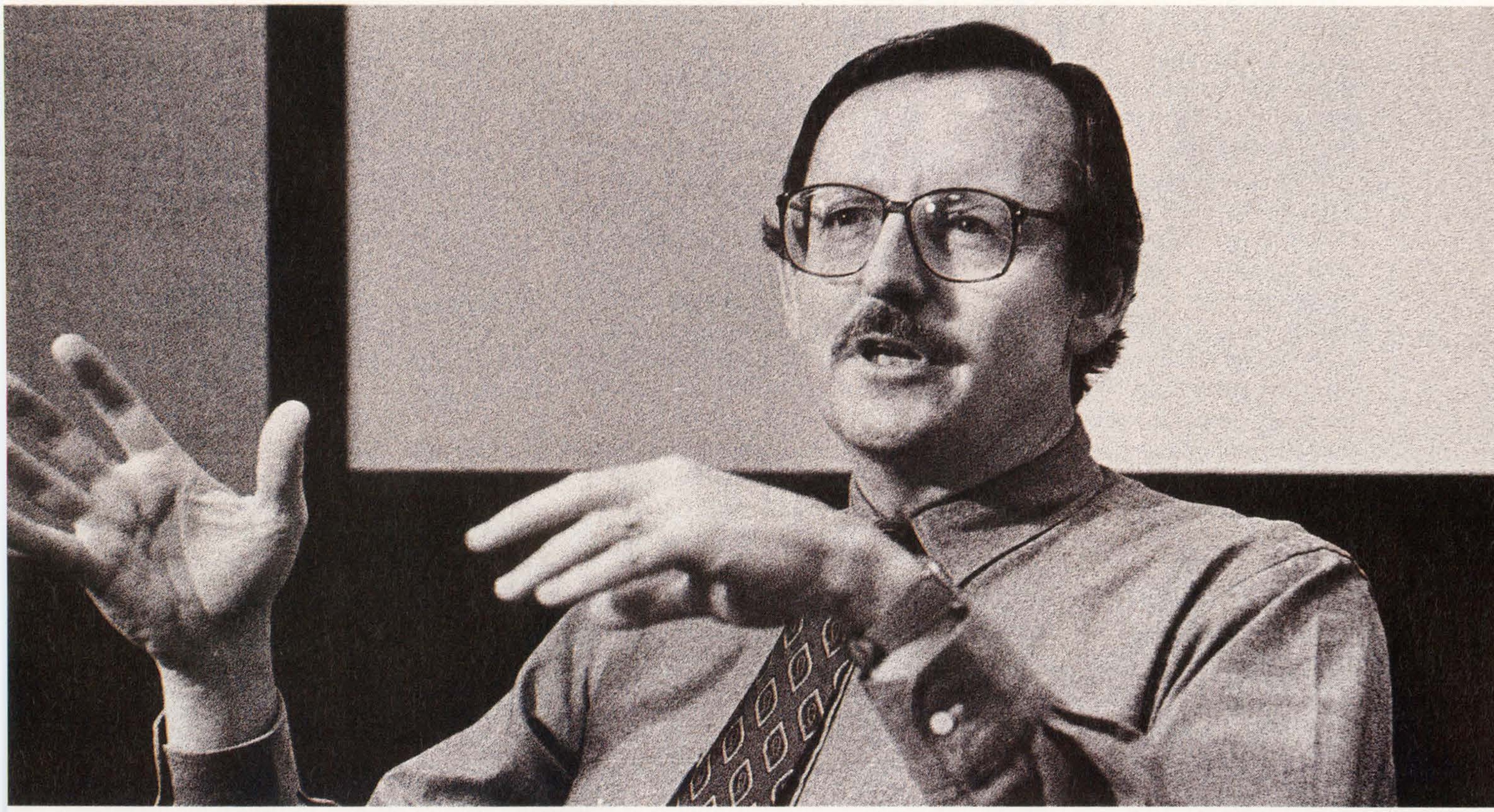

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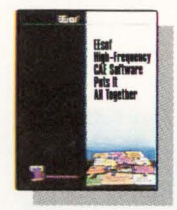

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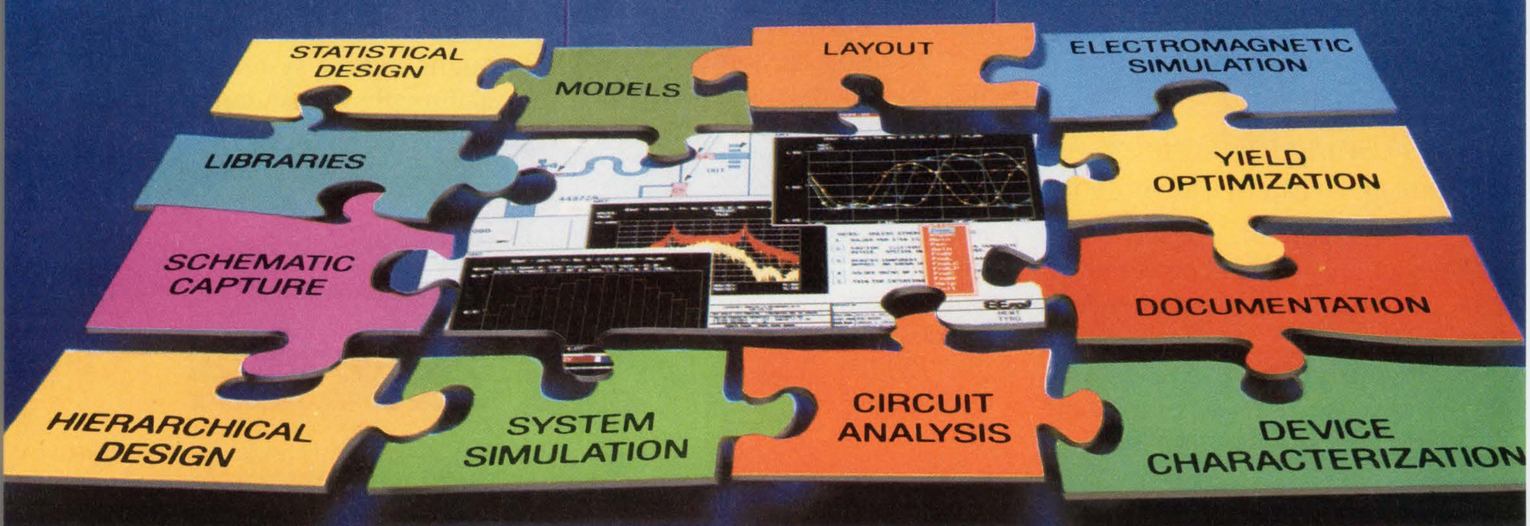
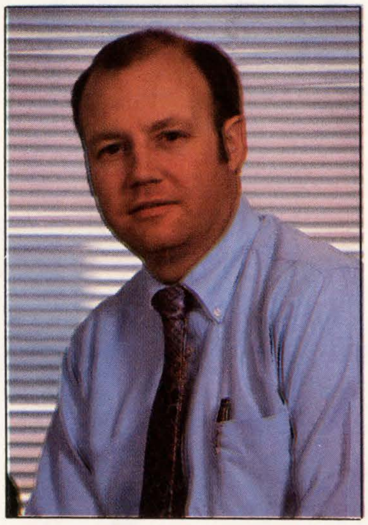


CIRCLE NO. 46

Look for recession opportunities



Without a doubt, the US and many of its trading partners are in a recession. Although the economic times look dim, opportunities still exist for those who are willing to pursue them. Over the last few years, I've come up with some observations that can help you identify present technical opportunities. Keep in mind that these points apply mainly to areas in which technical change is rapid.

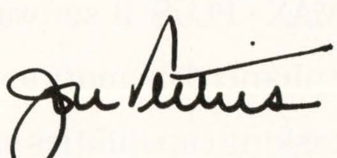
1. Technology spreads downward. Put another way, technology destroys centralization. Several examples come to mind—the telephone, the photocopier, and the personal computer. When the telephone became popular, few people could imagine its rapid spread through businesses because there just wouldn't be enough people to act as central-office operators. Today's pushbutton phone lets me control a global communication network. The communication technology—and the control of the phone network—spread downward from large central offices to individual users. Similar stories exist for the copier and the PC. Many centralized technologies are ripe for "fragmentation."

2. Innovative people bootleg technology. Take a look at the technology that people sneak into a company or organization to help them on the job. When personal computers became available, many people bought their own and put them in their offices. People will go to great lengths to get products that help them do a better job—even if those products aren't sanctioned or are forbidden by "management." Locating bootlegged products can lead to opportunities and to plans for new products.

3. Late adopters often surpass early adopters. Although this sounds contradictory, it's true. Many of the newcomers to the semiconductor industry are the ones who are willing to learn from the mistakes of the early adopters and adapt their businesses to new conditions. If you need confirmation of this, simply try to recall the names of three of the earliest transistor manufacturers. Although we hear about shorter times to market and narrower market windows, it can pay to let someone else go first. You don't always have to create something brand new.

4. People buy tools, not technology. It's easy to forget that most people don't care what kind of microprocessor is in their personal computer. Likewise, customers don't buy a fax machine because of the type of modem circuits it uses. Keep your eye on solving the customers' problems and keep the technology secondary. Sure, the technology is important, but it's a means to an end. Don't fall in love with it.

5. Technology bottlenecks are opportunities. One of today's biggest bottlenecks is software development. We're still at the craftsman level—everyone develops their own software, and software is recreated endlessly. Computer-aided software engineering (CASE) and object-oriented programming may yet prove to be helpful, but the software world still awaits a breakthrough akin to the development of mass-produced integrated circuits. Taking the hardware analogy further, software is still at the level of point-to-point wiring. Identify bottlenecks and find innovative solutions to remove them.



Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
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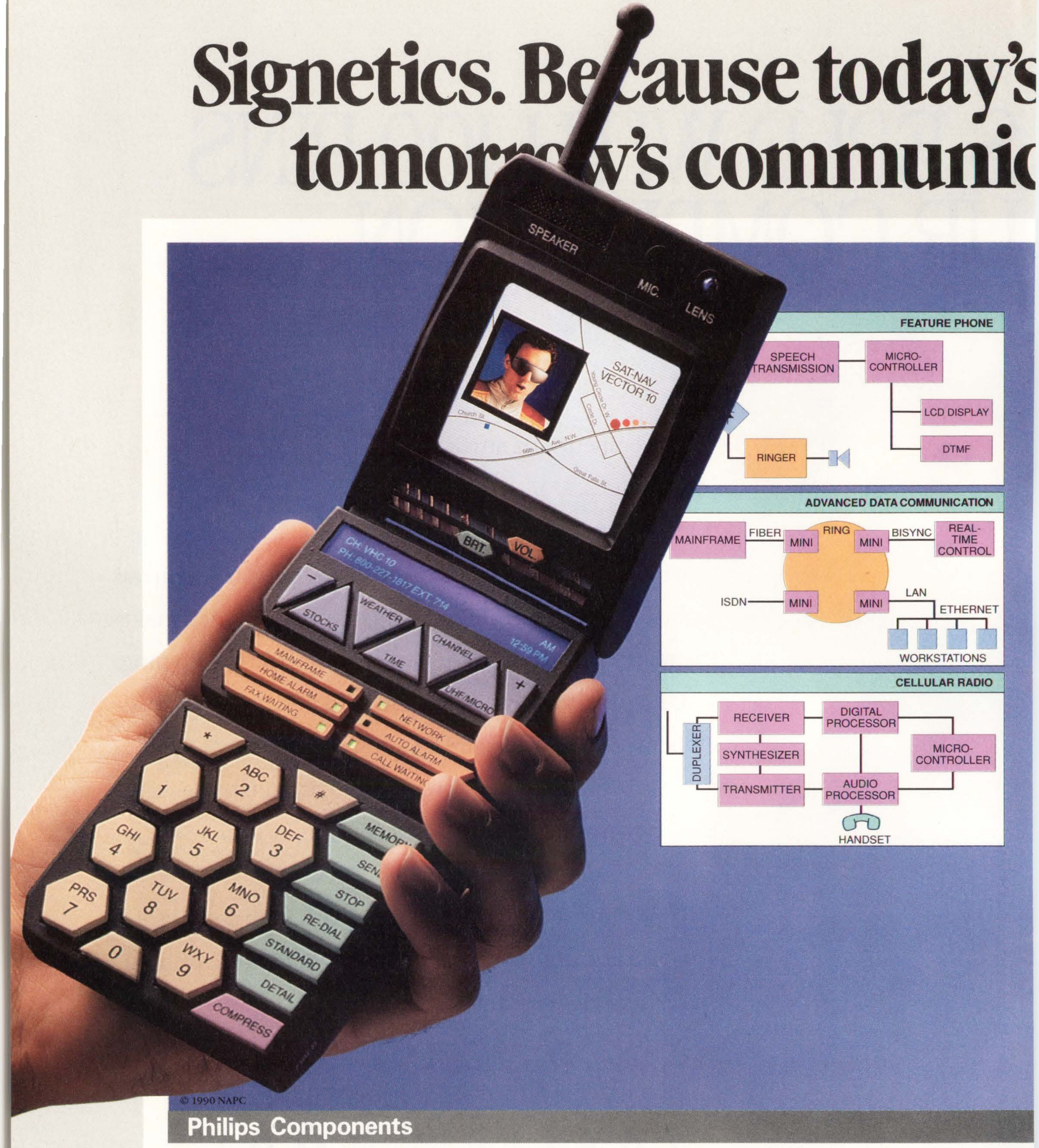
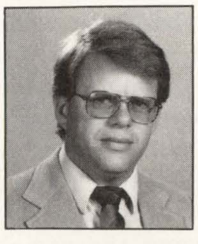
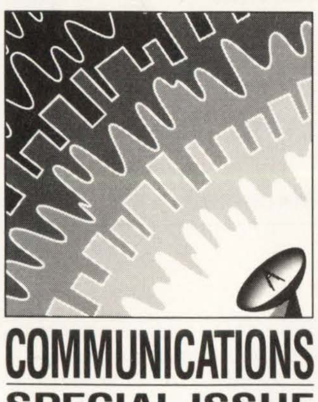


CAE tools help cure transmission-line woes



When pc-board traces act like transmission lines, all manner of problems can arise. CAE tools can help forestall those problems before you build your board.

Richard A Quinnell,
Regional Editor



Increasing logic speeds are forcing digital designers to consider transmission-line effects in printed-circuit boards. Yet most digital designers working with CMOS and TTL circuitry have little experience in recognizing and dealing with such effects. Fortunately, a variety of CAE tools can help to predict and correct transmission-line effects at all stages of pc-board design.

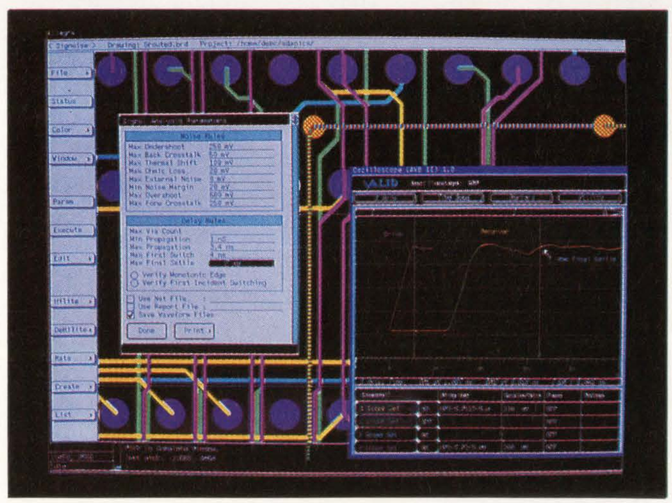
Transmission-line effects manifest in your circuit in many ways. They show up as delays that prevent clock and data signals from meeting IC setup and hold requirements. They also cause ringing signals, which can cross logic thresholds several times, thus wreaking havoc on counters and other edge-sensitive circuits. Ringing signals can swing beyond the rail voltages, possibly damaging components. Crosstalk noise can also be a manifestation of transmission-line effects.

ECL designers have long faced these problems and have developed a robust set of design rules to handle them. Unfortunately, well-established rules for high-speed CMOS and TTL design do not exist. There are guidelines, but those guidelines are broad rules of thumb (see **box**, "Do I need transmission-line tools?").

Such rules of thumb leave considerable room for error and are not adequate for many designs. If the rule you follow is too loose, you may produce a marginal design. A conservative rule becomes a tyranny if you follow it blindly—for example, placing line terminations where they aren't really needed. The resulting pc board will be much more expensive than necessary. In either case, rules of thumb give only crude estimates of critical parameters such as timing delays.

Broad as they are, rules of thumb do provide adequate guidance if your circuit's timing is not critical and if board cost is not a design constraint. If the timing has little margin, or if cost is an issue, however, you'll want stricter guidance as you calculate the expected behavior of every potential transmission line in your circuit. In such circumstances, transmission-line CAE tools really prove their worth.

You can use transmission-line CAE



Catching transmission-line problems before they happen *is the job of transmission-line screening tools such as Valid Logic Systems' Signal Delay Analyzer. Working within the Allegro pc-board design tool, the analyzer finds and highlights problem traces.*

tools at three stages in pc-board design: before beginning board layout, following component placement, and after routing. Not every tool is suitable for use at each stage, however. **Table 1** shows a representative selection of transmission-line CAE tools.

The tools fall into two categories: analysis and screening tools (**Ref 1**). The analysis tools analyze individual signal traces and let you study the circuit's behavior in detail using simulated waveforms. The screening tools check an entire circuit board in one pass but only give waveforms for selected traces. These tools produce tabular results for the remaining traces, flagging the ones that fail to meet noise margins. You can also use screening tools to analyze individual circuits.

A good use of analysis tools is to help establish design rules before you begin your pc-board layout. Use the tools to calculate the behavior of representative circuits. From these test cases, you can develop design rules specifically for your board. The rules you'll want to establish include maximum trace and stub lengths, minimum trace separation, maximum length of parallel runs with critical circuits, and line-termination type and value. You can also use the test-case information to select parameters such as trace width, substrate type and thickness, and the number and placement of ground planes.

Screening tools let you check for transmission-line effects once you know what your circuit will tolerate. For example, a placement screening tool yields an estimate of trace delays given your component placement. These estimates use a network's Manhattan distances—the shortest possible routes between nodes if the traces were to follow an X-Y grid. Screening tools that have this capability include Shared Resources' Crystal Placement and Quad Design Technology's PDQ.

The placement-based delay estimates will help you catch timing problems caused by long traces before investing time in a complete board routing. By feeding the estimated trace delays back into a logic simulator, you can determine whether the design possesses a fatal timing flaw.

If your timing simulator and the placement screening tool share the same database, you will save time and effort in arriving at a final layout. For example, a tool such as Valid Logic's Sigdelay, which is part of the company's Allegro pc-board CAD tool, lets you modify the board layout and quickly check the results using the same software. This interactive capability lets you quickly achieve a working design.

Don't stop short

The accuracy of these delay estimates peaks at ±20%. If your timing margins can absorb this error, you may be tempted to stop the analysis at this point. After all, you can usually add fixes for noise and

Do I need transmission-line tools?

When you're not sure that your designs require transmission-line analysis, estimate the number of transmission lines your design has. If a large number of your traces are transmission lines, your design will likely benefit from CAE analysis tools.

One rule of thumb for identifying potential transmission lines is that an unterminated trace will act as a transmission line if the time it takes a signal to propagate down the trace and back is more than ½ the signal's rise time. More conservative versions of the rule cut that ratio to ¼ or ⅕ (**Ref 2**).

Fig A translates these timing rules into suggested trace lengths for a given rise time. The graphs are for a propagation time of 2 nsec/ft, a typical value. You can use the chart to see if your circuits fall into the problem zone. If they do, you'll need to treat them as transmission lines to evade trouble.

Rules of thumb are only guidelines, however, and may be too loose or too tight. **Fig B** shows simulated waveforms for traces designed with the ½ and ⅕

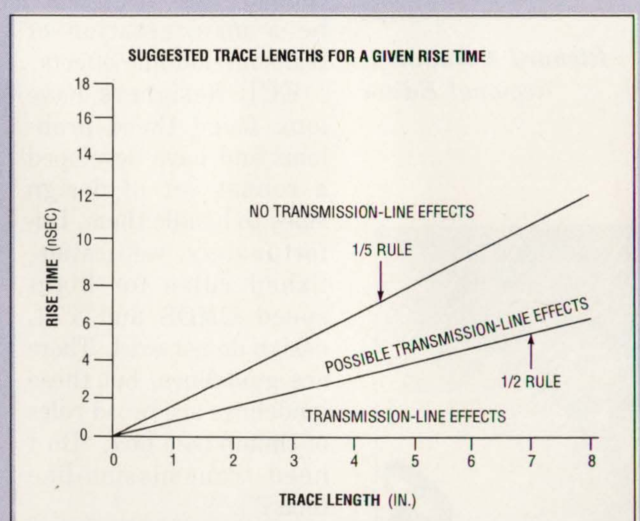
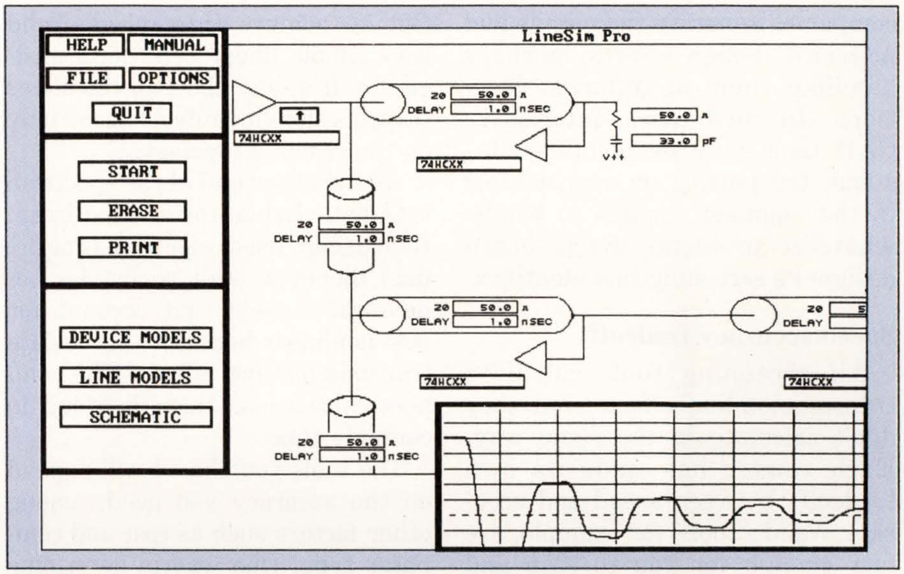


Fig A—Rules of thumb help you determine *if a trace might act like a transmission line. The graph translates the ½ and ⅕ timing rules into suggested trace lengths for a given rise time. The graphs assume a propagation time of 2 nsec/ft, a typical value.*

ringing problems after the board is fabricated. Only timing problems would have required you to do extensive redesign.

However, today's short design cycles may not allow you the luxury of chasing down noise and ringing problems. To minimize debug time, check your board's design for such transmission-line effects before building it. Use screening tools to check your board for crosstalk and ringing that violate the limits you set on each network. In addition, screening tools provide more accurate trace-delay information than placement-screening-only tools do. Several tools, such as Swiftlogic's Swiftline and Valid's Signal Noise Analysis tools, also check for signal overshoot and undershoot.



Analysis tools let you test single circuits *and calculate the results in detail. Tools such as Hyperlynx's Linesim Pro also simulate waveforms.*

Here again, having the transmission-line CAE tool and your pc-board CAD system share the same database can be an advantage. For example, Valid's Sigdelay and Signal Noise Analysis tools will highlight the failed traces directly on the pc-board plot and let you correct the problem interactively. The Swiftlogic tools bring the same capability to Mentor Graphics' CAE tools. The ability to design interactively is more than a convenience. Moving traces on a fully routed board can create new problems as fast as it cures old ones. Repeatedly iterating the design in batch mode can be quite tedious.

But such tight integration is advantageous only if you have access to the pc-board database. Some

rules. In this example, the traces are microstrips 6 in. long, 10 mils wide, and 20 mils above a ground plane. The ½ rule yields signals of marginal quality; the ⅕ rule yields extremely high-quality signals. Neither rule is the best choice for this board: The ½ rule might produce a marginal design, and the ⅕ rule would result in a board much more expensive than necessary.

These two rules, then, define a region of ambiguity. Outside the region you can be fairly certain that your trace either requires termination or doesn't. Within the region, the traces may or may not need termination; you can't tell without further analysis. If a significant number of your board's traces fall in the ambiguous region, a transmission-line CAE tool becomes almost a necessity.

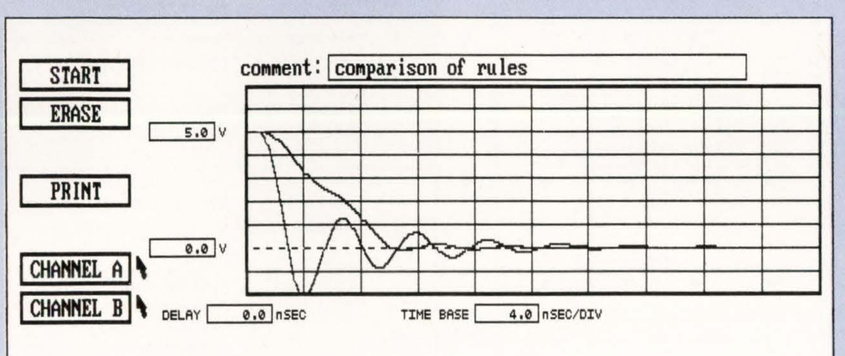


Fig B—Simulated waveforms *for traces designed with the ½ and ⅕ rules can be generated with the Hyperlynx Linesim tool. In this example, the traces are microstrips 6 in. long, 10 mils wide, and 20 mils above a ground plane. The ½ rule gives marginal results; the ⅕ rule is too restrictive.*

companies separate the circuit and pc-board design efforts, perhaps handling them at different locations. In such cases, interactive CAD tools may be pointless. Instead, try putting an analysis tool in the engineer's hands to handle whatever problems the pc-board designer's screening tool identifies.

Speed/accuracy tradeoffs

All screening tools calculate transmission-line effects, but they don't calculate in the same way. Each vendor has made its own tradeoffs between speed and accuracy. Valid's tools, for example, are fast enough for you to scan and modify your board interactively. But to achieve this speed, Valid uses simple linear behavioral models for ICs, and the tool calculates transmission-line effects based only on the circuit's topology.

At the other end of the spectrum is Quantic Laboratories' Boardscan. Boardscan uses electromagnetic-field theory as well as complex behavioral models that account for ICs' nonlinear behavior to calculate transmission-line effects. The complex calculations take their toll in compute time.

The tools you choose will depend on the accuracy you need, among other factors such as cost and computer type. One way to determine the accuracy you require is to test the tools using some of your existing pc-board designs. Then, check the results against the actual boards.

If you want to avoid transmission-line problems without using analysis tools, consider using one of the transmission-line-rule-driven pc-board autorouters. Valid's Allegro, Cadence's Amadeus Prance, and Shared Resources' Crystal pc-board design systems let you constrain their autorouters. You can use these tools to limit trace and stub lengths, match trace lengths, and control the connection ordering when routing. These features help control ringing and signal skew and ensure that signal transmitters and

Table 1—Representative transmission-line analysis tools

Company	Product name	Tool type	Features: Post-placement screening	Trace delay	Settling delay	Multiple-threshold-crossing detection	Over-shoot/under-shoot	Cross-talk analysis	Other features	Platforms	Price
Design Analysis Consultants	Timing Margin Analyzer	Analyzer		•	•				Worst-case timing analysis	IBM PC	$350
Hyperlynx	Linesim	Analyzer		•	•	•	•			80286-, 80386-, and 80496-based PCs	$495
	Linesim Pro	Analyzer		•	•	•	•			80386- and 80486-based PCs	$995
Quad Design Technology Inc	Preroute Delay Quantifier (PDQ)	Screening	•	•						Daisix, HP/Apollo, Sun, Valid, Viewlogic workstations	$11,000 for all
	Transmission-line Checker (TLC)	Screening		•	•	•			Also analyzes cables		
	Crosstalk Toolkit (XTK)	Screening						•	Also analyzes cables		
Quantic Laboratories Inc	Boardscan	Screening	•	•	•	•	•		Behavioral models	Unix workstation	$15,000
	Greenfield	Analyzer		•	•	•	•	•	Electromagnetic-field analysis	Unix workstation	$35,000
Shared Resources Inc	Crystal Placement Tool Set	Screening	•	•					Includes crystal pc-board design system	HP/Apollo, Sun workstations	$40,000
Swiftlogic Inc	SwiftLine	Screening	•	•	•	•	•		Includes package models	HP/Apollo, Sun workstations	$17,500 for both
	SwiftNoise	Screening						•			
Valid Logic Systems	Sigdelay	Screening	•	•	•	•			Lossy-line modeling	DECStation, VAXStation, Sun, IBM R6000 workstations	From $12,500
	Signal Noise Analysis	Screening					•	•			

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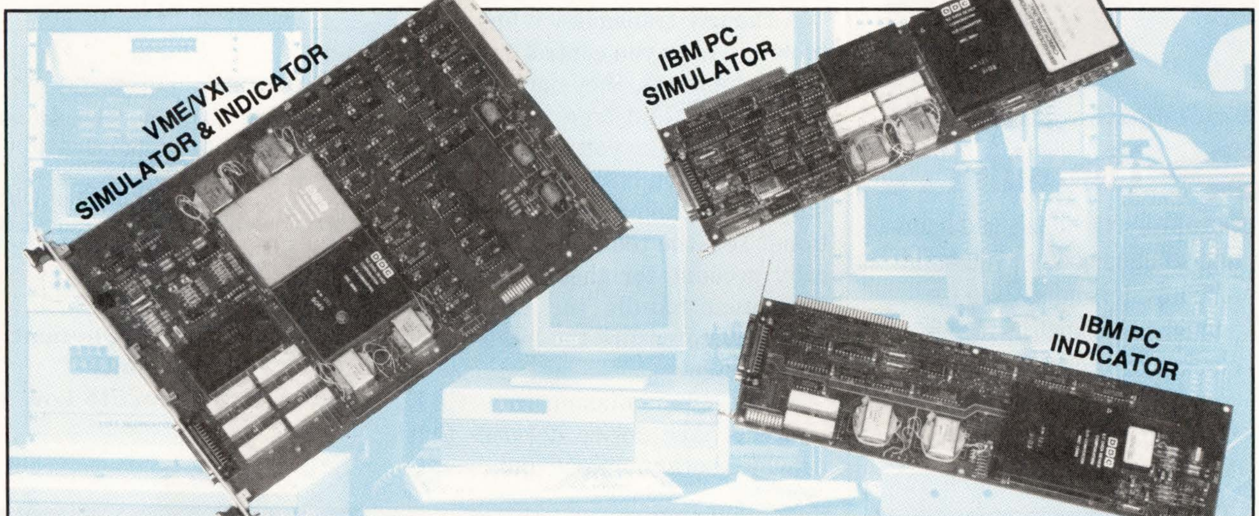

The IAC-37001 Simulator and Indicator provides independent channels for Synchro/Resolver-to-Digital and Digital-to-Synchro/Resolver conversion on the same VXI card. These instrument-grade converters operate independently with separate references and are mounted on a "C" size card conforming to VXI register-based specifications.

The S/D section allows selection of 20 or 16 bit mode, with accuracy to 18 arc seconds in either Synchro or Resolver mode. Signal inputs are transformer isolated, with programmable levels of 11.8, 26, or 90 volts L-L, and a frequency from 360 to 10KHz.

The D/S section of the IAC-37001 may be programmed for Synchro or Resolver output with an accuracy up to 20 arc seconds. A new feature is dynamic rotation, producing a constant clockwise rotation.

Applications include production testing, quality control inspection, and laboratory instrumentation. ❑

Sales Contact Circ. #35 Literature Circ. #36

The SIM-36010 Simulator is a full size IBM PC® based card containing a single-channel, wideband, high-accuracy instrumentation-grade Synchro/Resolver Simulator.

It accepts either a 36 or 115 Vrms reference signal and outputs a Synchro or Resolver signal at 11.8, 26, or 90 Vrms L-L with a drive capability of 1.5 VA. It includes a programmable dynamic rotation feature that provides a constant output rate, clockwise or counterclockwise, from 0.07 degrees per second to over 30 revolutions per second.

The SIM-36010 is a versatile Synchro/Resolver instrument for production testing, quality control inspections, and laboratory instrumentation. It is ideal for use on a stand-alone simulator in an engineering department or as part of PC based Automatic Test Equipment (ATE).

Demonstration software, which shows the SIM-36010 capability is available with the card. ❑

Sales Contact Circ. #37 Literature Circ. #38

The API-36005 Indicator is a full size IBM PC® based card containing a single-channel, wideband, high-accuracy, instrumentation-grade Synchro/Resolver Angle Position Indicator (API).

It accepts a reference signal of 26 or 115 Vrms, along with Synchro/Resolver signals of 11.8, 26, or 90 volts L-L, and converts these signals into 16 or 20 bits of binary angular information. Input signals are isolated over 360 to 5000Hz. It contains a built-in single-angle self-test feature for confidence testing. It is faster than conventional IEEE bus test systems.

It is ideal for use as a stand-alone Angle Position Indicator in the engineering lab or as part of PC based Automatic Test Equipment (ATE).

The API-36005 comes with an operating and maintenance manual, and demonstration software.

For additional information, contact Bill Cullum, 1-800-DDC-1772 ext. 389. ❑

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terminators are at the ends of networks.

The boards a rule-driven autorouter designs will be correct by construction, in theory. But the design will only be as good as its design rules. You still have to tell the autorouter what rules to use.

Although transmission-line CAE tools can help you control transmission-line effects, they don't guarantee a problem-free production board. The ICs you purchase and the boards you build will inevitably vary from their nominal specifications. Yet, the tools don't automatically account for those variations. You must handle the variations manually to ensure the integrity of your design.

Many transmission-line CAE tools do have device libraries that provide both nominal and worst-case models. No tool provides Monte-Carlo simulation using those models, however, nor do any handle variations in trace thickness or width. It's up to you to scan your design repeatedly to test for all relevant combinations of device and board variations. EDN

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1. Conner, Margery, "Simulators for high-speed board design spot trouble," *EDN*, December 21, 1989, pg 152.
2. Royle, David, "Rules tell whether interconnections act like transmission lines," *EDN*, June 28, 1988, pg 131.

Article Interest Quotient
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For more information . . .

For more information on the transmission-line products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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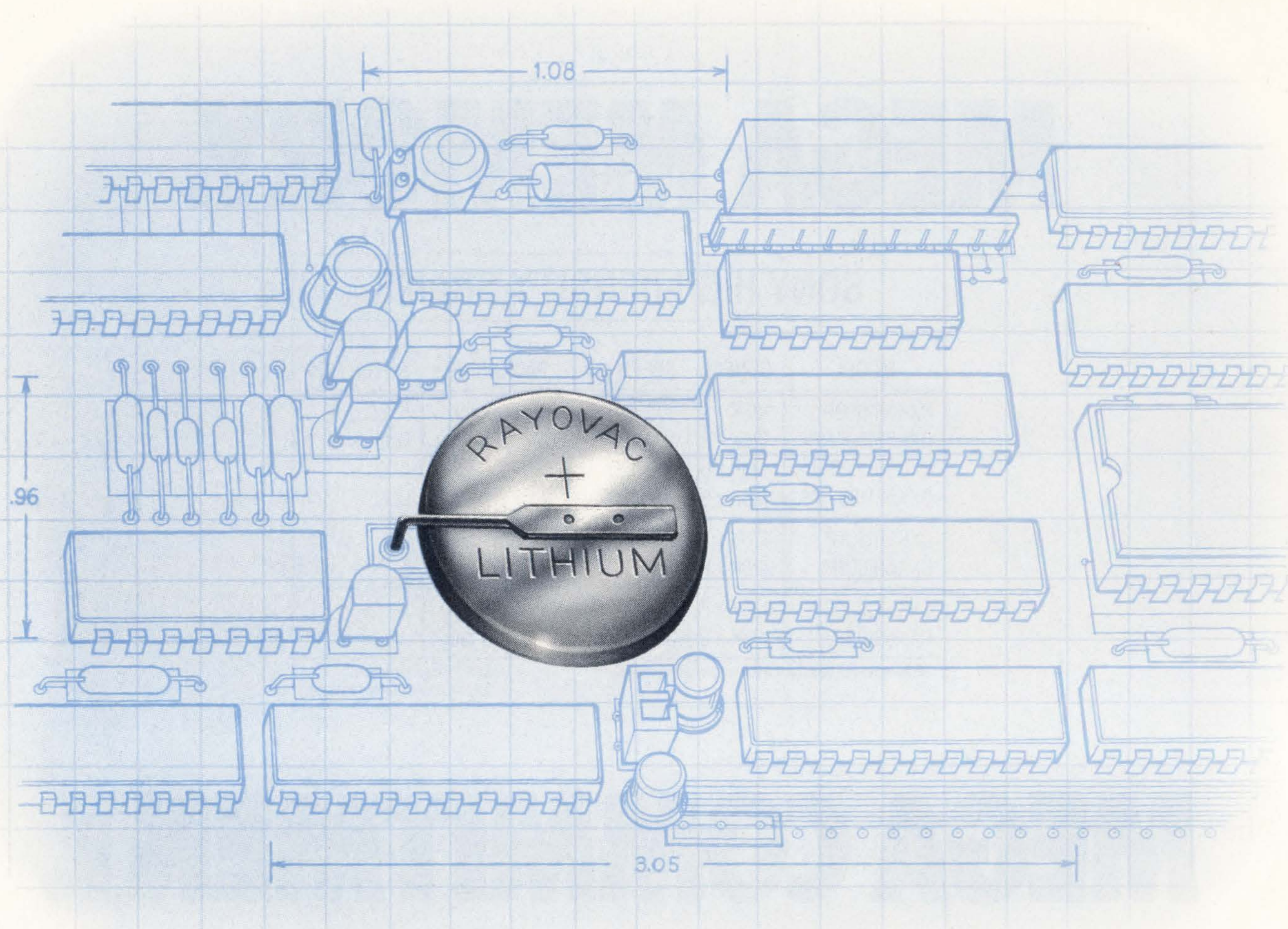

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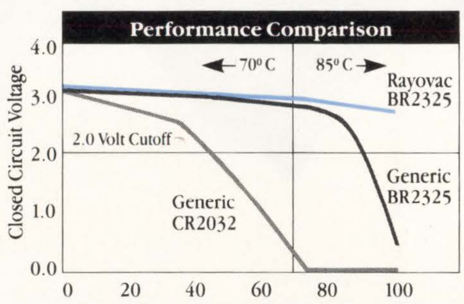

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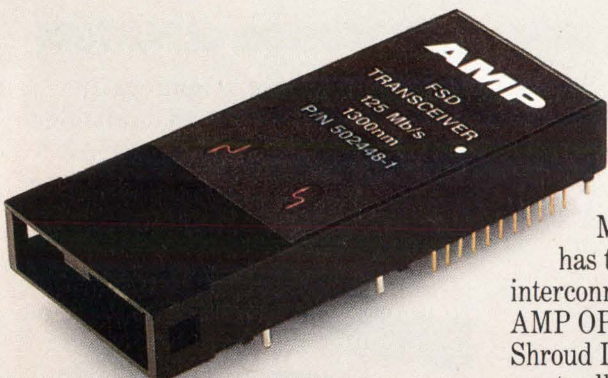

Good news for networks!

The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document.

More good news! AMP has the complete fiber optic interconnection system—the AMP OPTIMATE Fixed Shroud Duplex System—that meets all FDDI PMD requirements. And includes all the physical components you need to make your fiber optic network a reality.

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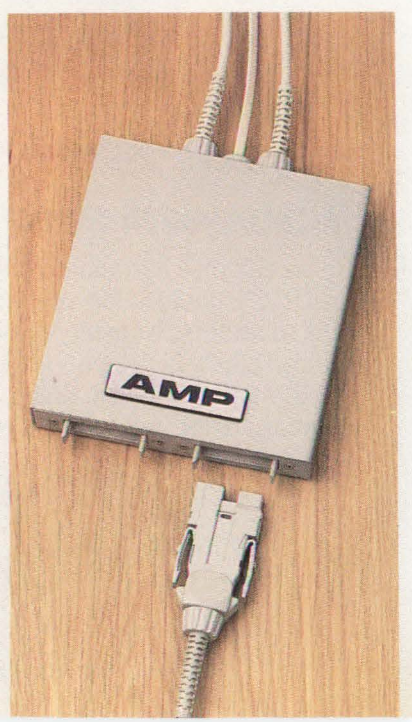

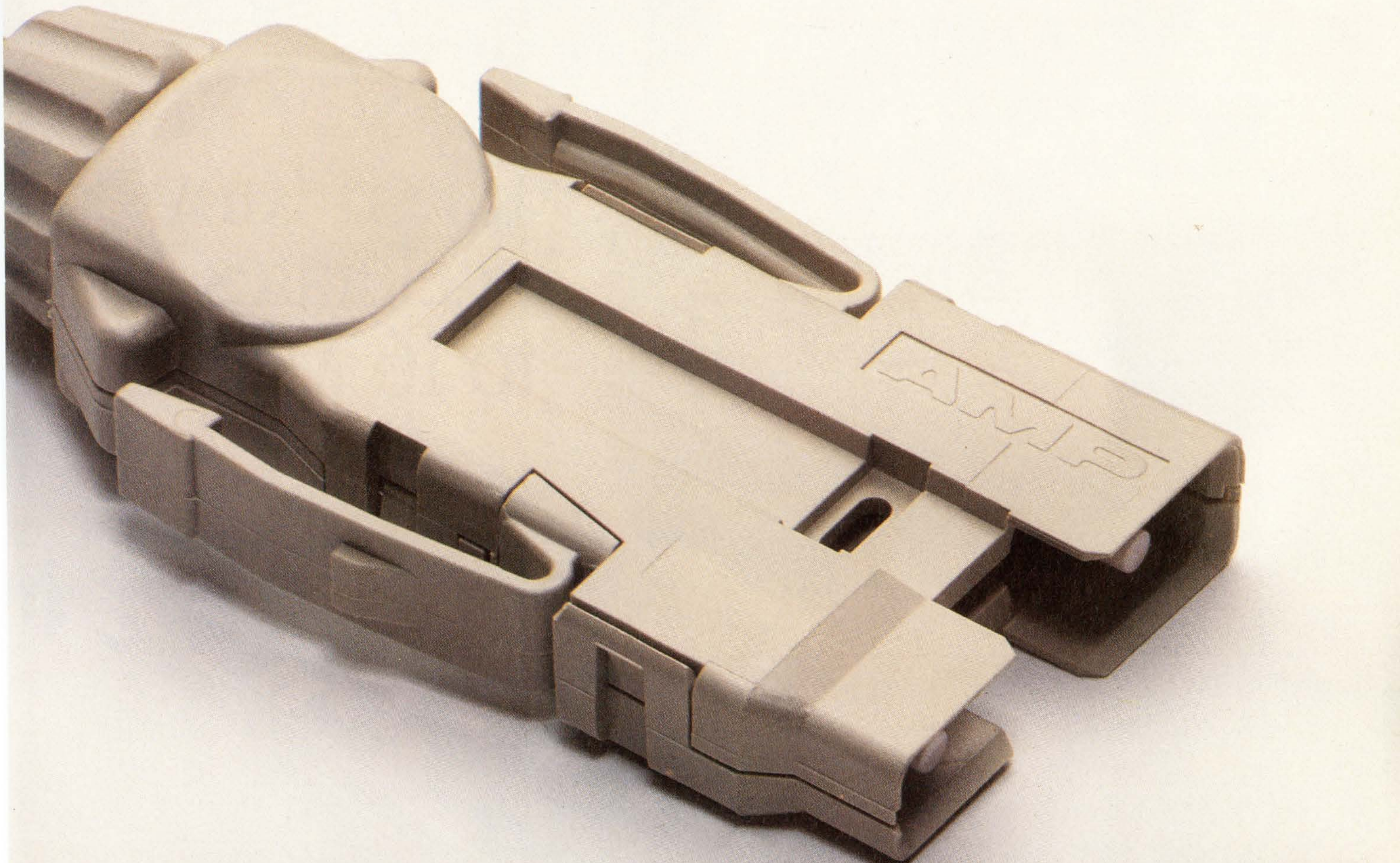

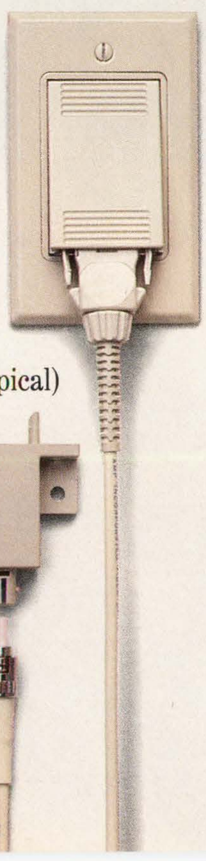

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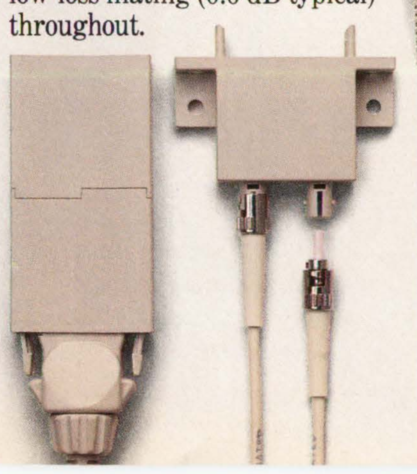

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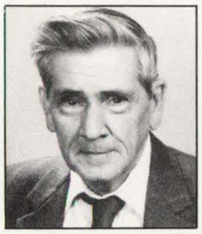


Transceiver modules are key factors in fiber-optic data links and can implement communications in both local- and wide-area networks.

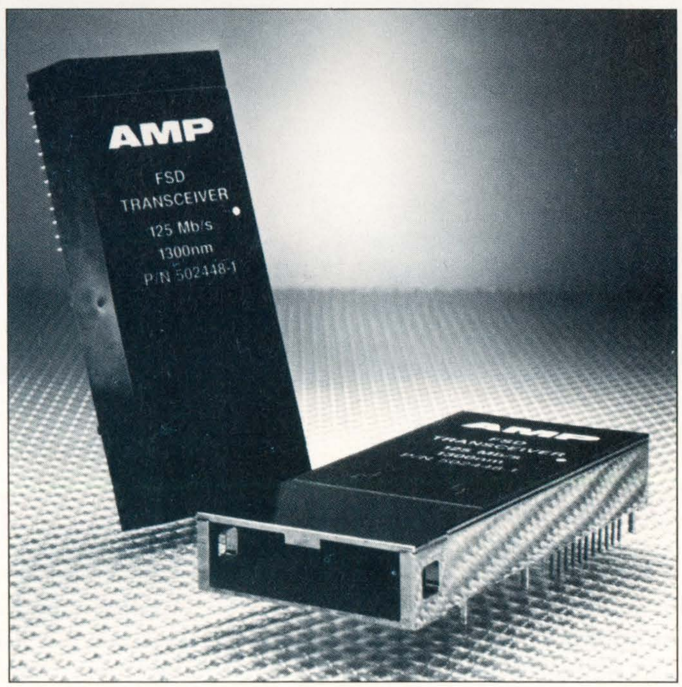
Dave Pryce,
Associate Editor

Advances in fiber-optic components and the implementation of new standards are having a dramatic effect on both short- and long-haul telecommunications. Rather than using a traditional copper-based system with its inherent bandwidth limitations and EMI/RFI problems, an increasing number of communications networks are implemented with fiber-optic cables. Local-area networks (LANs) based on the Fiber Distributed Data Interface (FDDI) are making their presence felt, and the emerging Synchronous Optical Network (SONET) standard will likely play a major role in long-distance applications. (For a description of these standards, see **box,** "Fiber-optic-network standards," pg 64.)

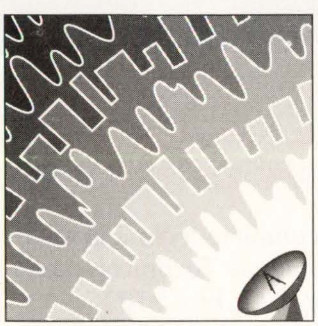
Of critical importance to the implementation of these state-of-the-art networks are the transmitter and receiver modules, which interface with the fiber-optic link. Many of these modules take the duplex form of a transceiver, which combines the functions of both the transmitter and receiver.

Typical of these transceivers are the multisourced FDDI modules available from such companies as AT&T, Hewlett-Packard, AMP, and Siemens. These modules have similar circuitry and feature a similar package that mounts on a printed-circuit board.

In the Hewlett-Packard version of the FDDI transceiver **(Fig 1)**, the transmitter section consists of a 1300-nm InGaAsP LED and a single custom bipolar LED-driver IC. The driver circuit provides temperature compensation to regulate the optical output power. The receiver section of the FDDI module consists of a 1300-nm InGaAs PIN (positive intrinsic negative) photodiode and two custom bipolar ICs. The preamplifier IC mounts in the optical subassembly with the PIN detector to maximize receiver sensitivity. The quantizer IC provides the final pulse shaping for both the logic output and the signal-detect



This pin-compatible multisourced FDDI transceiver *from AMP is similar to those available from Hewlett-Packard, AT&T, and Siemens.*



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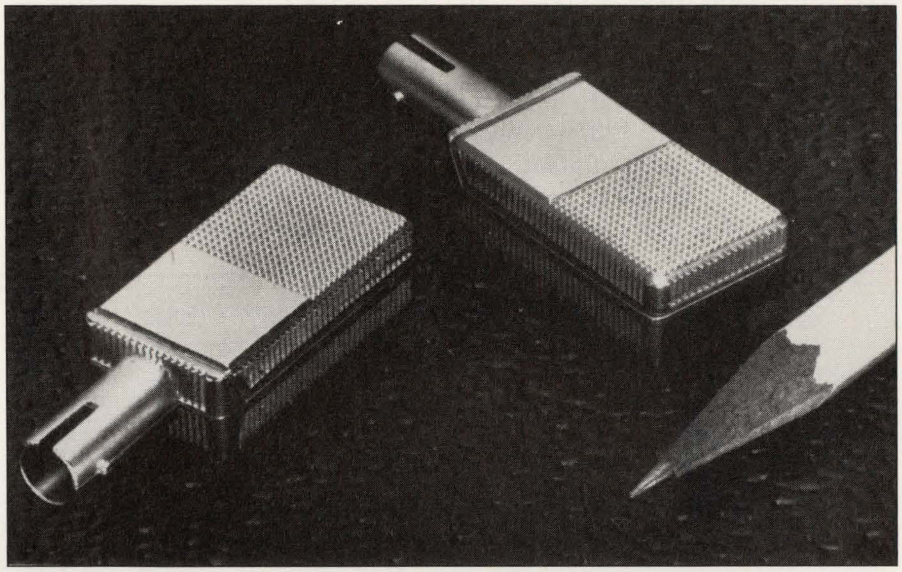
function. The data input to the transmitter and the data and signal-detect logic outputs of the receiver are differential, 100K ECL-compatible circuitry referenced to a 5V power supply.

Regardless of any minor circuit variations between FDDI transceiver modules from different vendors, all work in the same manner and provide essentially identical performance. Moreover, all come in a similar-size package with identical pin arrangements in the form of two rows of 11 pins each for pc-board connection. The module also has a built-in MIC (media interface connector) receptacle for connection to the fiber-optic link. Hewlett-Packard sells its HFBR-5125 version of these multisourced transceiver modules for $550 (1 to 9).

Hewlett-Packard also offers individual transmitter (HFBR-1125) and receiver (HFBR-2125) modules for $270 and $330, respectively. These FDDI-compatible modules come in a smaller 20-pin package with an ST simplex connector originally developed by AT&T. This combination is handy for designs, such as equipment that uses optical bypass switches, that can't use the duplex MIC connector.



FDDI modules are also available in simplex form. *These transmitter and receiver modules from Hewlett-Packard are individual, 20-pin devices with an ST-style fiber-optic connector.*

FDDI-compatible products and applications have been expanding at an accelerated pace, but the same has not been true for the still-emerging SONET standard. Nevertheless, authorities such as Mark Melliar-Smith, chief operating officer of the lightwave unit of AT&T Microelectronics, remain convinced that the networks of the future will likely be SONET networks. This conviction is a sound one. By standardizing transmission-line rates and specifying common rules of operation, SONET enables equipment from different vendors to function seamlessly across network boundaries.

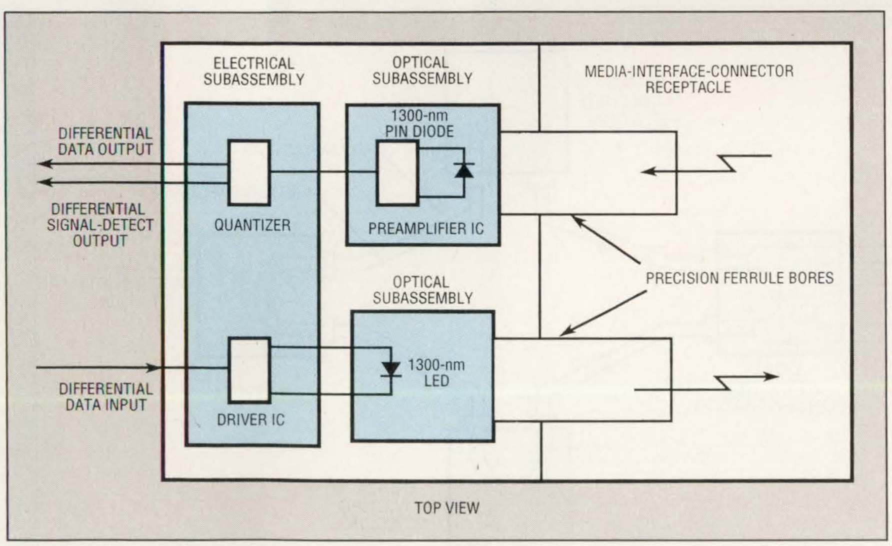


Fig 1—Multisourced FDDI transceivers all work in the same manner. *In Hewlett-Packard's version, the transmitter section uses a 1300-nm InGaAsP LED and custom driver IC. The receiver section uses a 1300-nm InGaAs PIN photodiode and two custom ICs. Regardless of the manufacturer, these FDDI modules come in similar-sized packages with identical pin connections.*

AT&T, among others, is backing up its conviction in SONET's future with products that are available now. At the Conference on Optical Fiber Communications recently held in San Francisco, AT&T introduced several SONET-compatible modules as part of its Astrotec series. Among these modules are the 1227 transmitter and 1310 receiver, which the company sells as a pair for $900 to $1100 (1000).

The 1227 transmitter consists of an InGaAsP 1300-nm Fabry-Perot laser diode, a low-power CMOS IC, and an InGaAs PIN photodetector as a backface monitor. These devices are contained in a hermetically sealed 20-pin package for pc-board mounting. Although uncooled, the transmitter meets all

Fiber-optic transceivers

SONET specifications over the −40 to +85°C range. The transmitter operates from a single 5V supply and can serve intraoffice links as long as 15 km. The 1227 operates at line rates of 51M, 155M, and 622M bps. At the latter rate, the transmitter can carry the equivalent of 8064 2-way voice telephone connections.

The 1310 receiver consists of an InGaAs PIN photodetector, a GaAs preamplifier, and a silicon bipolar comparator circuit. Like its companion transmitter, the receiver operates over the −40 to +85°C range. You can optimize the performance of the receiver for any data rate from 20M to 650M bps. In addition, the receiver is SONET compatible at 51.84M and 155.52M-bps data rates for intraoffice distances as long as 40 km. The device requires −5.2 and 5V supplies.

Fiber-optic-network standards

Networks with bit rates greater than 50M bps are handled by ANSI (American National Standards Institute). The two principal ANSI standards for use with fiber-optic networks are FDDI and SONET.

The ANSI Fiber Distributed Data Interface (FDDI) uses counter-rotating dual rings **(Fig A)**. The topology is essentially compatible with the IEEE-802.5 token-ring standard, but is slightly altered to accommodate high data rates. FDDI improves on the 802.5 standard by allowing the ring to pass the token to the next station for immediate access after transmitting the information packet. As a result, more than one packet of information can circulate at a time. The conventional 802.5 standard requires that the token return to the originating station before the next token is passed.

FDDI networks operate at 100M bps. They have a 2-km maximum cable length between nodes (stations), a 100-km maximum ring circumference, and a maximum of 500 nodes. The total length of the network can be 200 km. In contrast, Ethernet networks have a 0.5-km maximum cable length between nodes and a maximum length of only 2.8 km. Although the actual data rate for FDDI is 100M bps, the 4-bit/5-bit encoding scheme requires a 125M-baud transmission rate. The FDDI standard also specifies a 1300-nm LED for the photoemitter and a 1300-nm PIN diode for the photodetector. FDDI networks use multimode fiber cable with a core/cladding diameter of 62.5/125 μm.

Conceptually, a large-scale implementation of FDDI **(Fig B)** can support front-end, back-end, and backbone networks. The front-end network operates through a wiring concentrator to link equipment such as engineering workstations. The back-end network supports communications between mainframe computers or minicomputers and their associated storage devices. The backbone network uses gate-

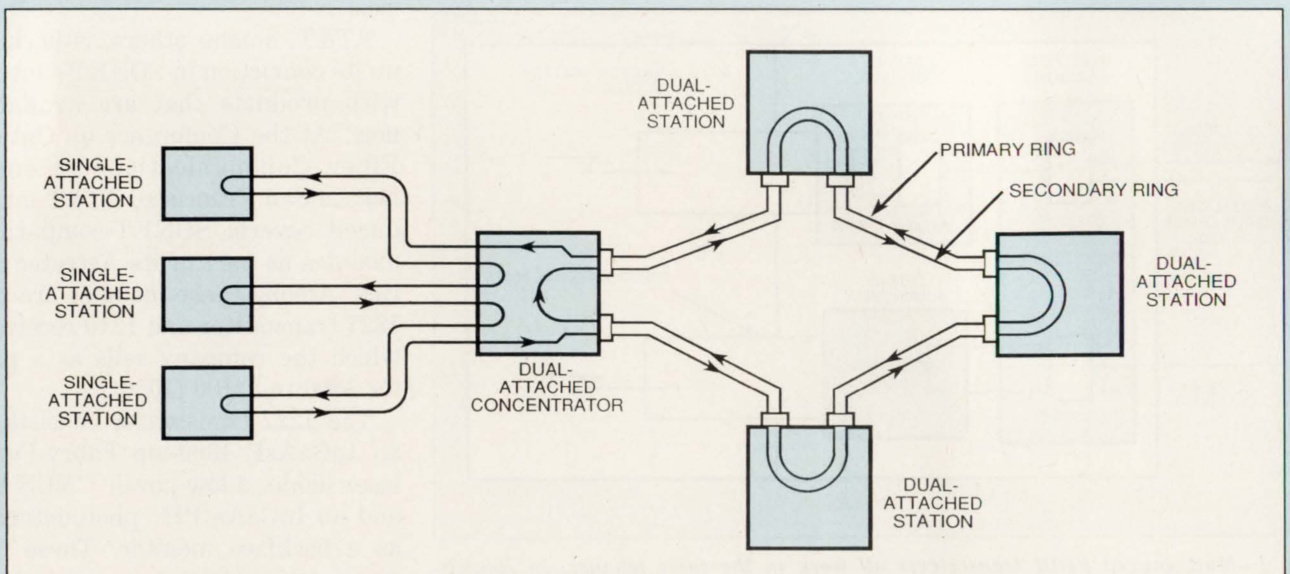


***Fig A—The Fiber Distributed Data Interface (FDDI)** uses counter-rotating dual rings, which allows more than one packet of information to circulate at a time.*

The implementation of FDDI-based systems is probably the most prevalent and the development of SONET-based systems the most dynamic among fiber-optic-transceiver applications, but many other applications exist for the devices.

Perhaps one of the least known, but most noteworthy examples is the use of fiber-optic transmitters and receivers in CATV systems. These systems use seemingly countless numbers of amplifiers to transmit and receive wide-band signals over 75Ω coaxial cable. By replacing the coaxial cable with fiber, CATV companies can greatly reduce the number of amplifiers in the typical system while reducing noise levels and expanding the bandwidth. Indeed, many suppliers of CATV equipment believe that future systems must use fiber if channel capacities are to grow beyond

ways to tie together various types of lower-speed LANs such as Ethernet, token-bus, and token-ring to form larger wide-area networks.

The ANSI Synchronous Optical Network (SONET) is not, by original intent, a local-area network. The standard was created to standardize transmission-line rates and architectures for long-haul fiber-optic systems. By specifying common rules of operation, SONET enables diverse vendor equipment to function seamlessly across network boundaries while transporting high-volume digitized voice, image, or data communications. SONET specifies a 1300-nm data link using either LEDs or lasers, depending on the distance and line rate. The standard encompasses line rates of 51.84M to 2488.32M bps and assigns specific line rates for each optical-carrier (OC) level. Examples include

Optical-carrier level	Line rate (M bps)
OC-1	51.840
OC-3	155.520
OC-9	466.560
OC-12	622.080
OC-18	933.120
OC-24	1244.160
OC-36	1866.240
OC-48	2488.320

Although SONET's primary application is in long-haul transmission over the switched telephone network, the standard may also prove useful for local loops. For example, SONET-compatible products are available that function well in single-mode FDDI applications as well as other single-mode private networks needing high capacity or lengths of 2 to 40 km.

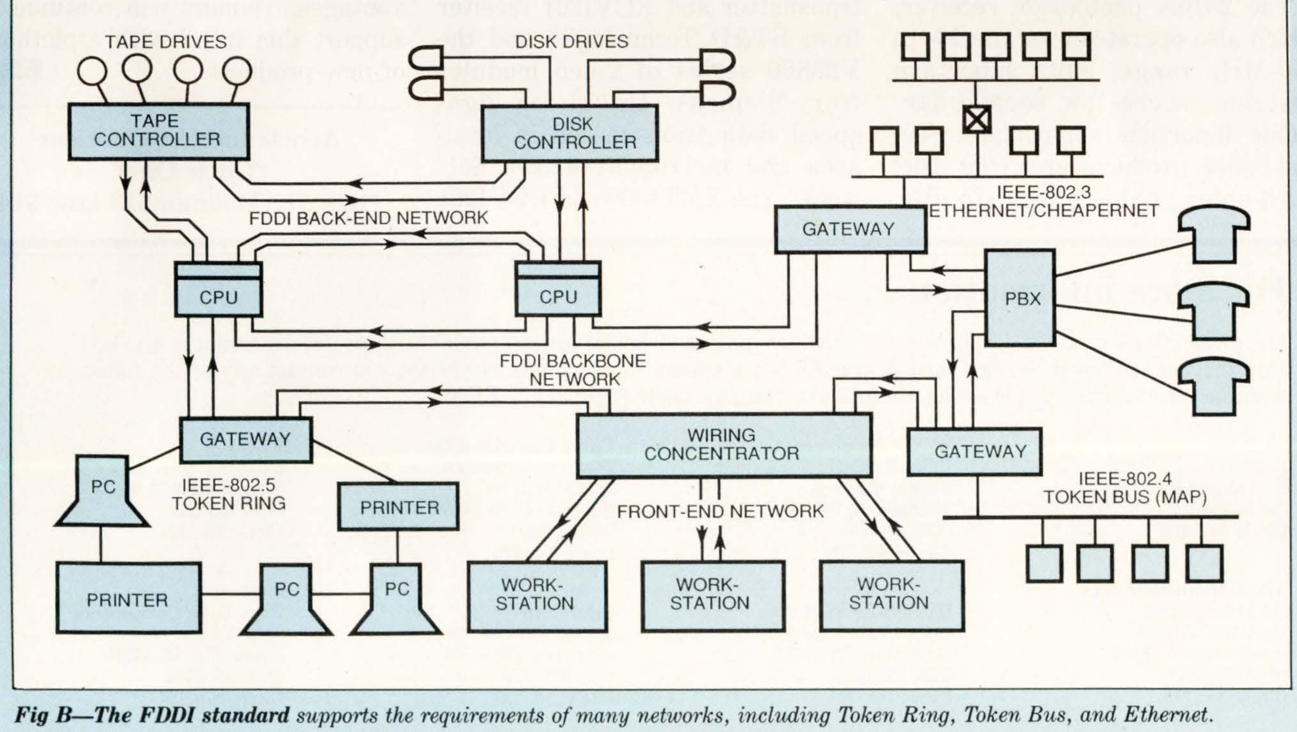


Fig B—The FDDI standard *supports the requirements of many networks, including Token Ring, Token Bus, and Ethernet.*

today's 550-MHz, 80-channel limit.

One of the companies addressing this need is Ortel Corp, which offers transmitter and receiver modules for CATV systems. Although expensive—single-quantity prices are $10,530 for the 1610A transmitter and $2295 for the 2610A receiver—these modules can be cost effective in certain sections of a CATV system. For example, the trunk network that moves signals from the head end to distant neighborhoods typically extends 15 to 20 miles. Spanning this distance using coaxial cable requires 30 to 50 amplifiers. A single laser-based transmitter can easily power a fiber-optic cable for a distance of 10 to 15 miles.

Ortel's 1610A CATV transmitter uses a distributed-feedback laser integrated with an optical isolator. The low-noise laser, which emits light at 1310 nm, suits 10- to 550-MHz AM CATV links for fiber-backbone and super-trunk applications. The optical output power is greater than 4 mW into single-mode 9/125-μm fiber cable.

The 2610A photodiode receiver, which also operates over the 10- to 550-MHz range, suits suboctave systems where low second-harmonic distortion is important. Second-order products are −60 dBc; third-order products are −75 dBc. The module, which has a gain 7 dB higher than that of an unmatched photodiode, uses a broadband RF output circuit to maximize delivered power. Like the transmitter, the receiver uses single-mode 9/125-μm cable.

Other applications

In addition to the fiber-optic modules suitable for FDDI, SONET, and CATV systems, a variety of general-purpose types are available for point-to-point and data-bus applications. Typical of these are the TX5000S010 transmitter and RX5237S010 receiver ($297/pair) from Litton Poly-Scientific. These modules operate at NRZ data rates of 1M to 25M bps and can serve a wide range of commercial and military applications. The modules have ECL-compatible inputs and require a single 5V supply. Both the transmitter and receiver come in 24-pin hermetically sealed packages that you can mount on a pc board.

Other examples of fiber-optic modules include the XMT1300 transmitter and RCV1201 receiver from BT&D Technologies and the V23800 series of video modules from Siemens. Useful for high-speed data transmission in local-area and metropolitan-area networks, the XMT1300 and RCV1201 modules are capable of data speeds as fast as 1.2G bps at distances of 10 km. Both the transmitter and receiver utilize GaAs integrated circuits to achieve this performance. The modules come in 28-pin, 1.5×1.0×0.25-in. hermetically sealed packages. The transmitter and receiver cost $860 and $1000 (1000), respectively.

The V23800-S1 and V23804-E1 video modules from Siemens suit security and surveillance applications. Using FM transmission, the 1300-nm devices can handle 7-MHz single-channel operation. The modules can transmit video signals over distances greater than 4 miles without a repeater. The 45×22×9-mm, 16-pin package lets you place as many as four modules on a single VMEbus board. In OEM quantities, the modules cost $260 each.

Although fiber-optic cables are not likely to completely replace the ubiquitous twisted pairs of copper wire and coaxial cable, an increasing number of applications are turning to fiber for its performance advantages. Vendors will continue to support this trend with a plethora of new products. EDN

Article Interest Quotient
(Circle One)
High 512 Medium 513 Low 514

For more information . . .

For more information on the transceiver modules discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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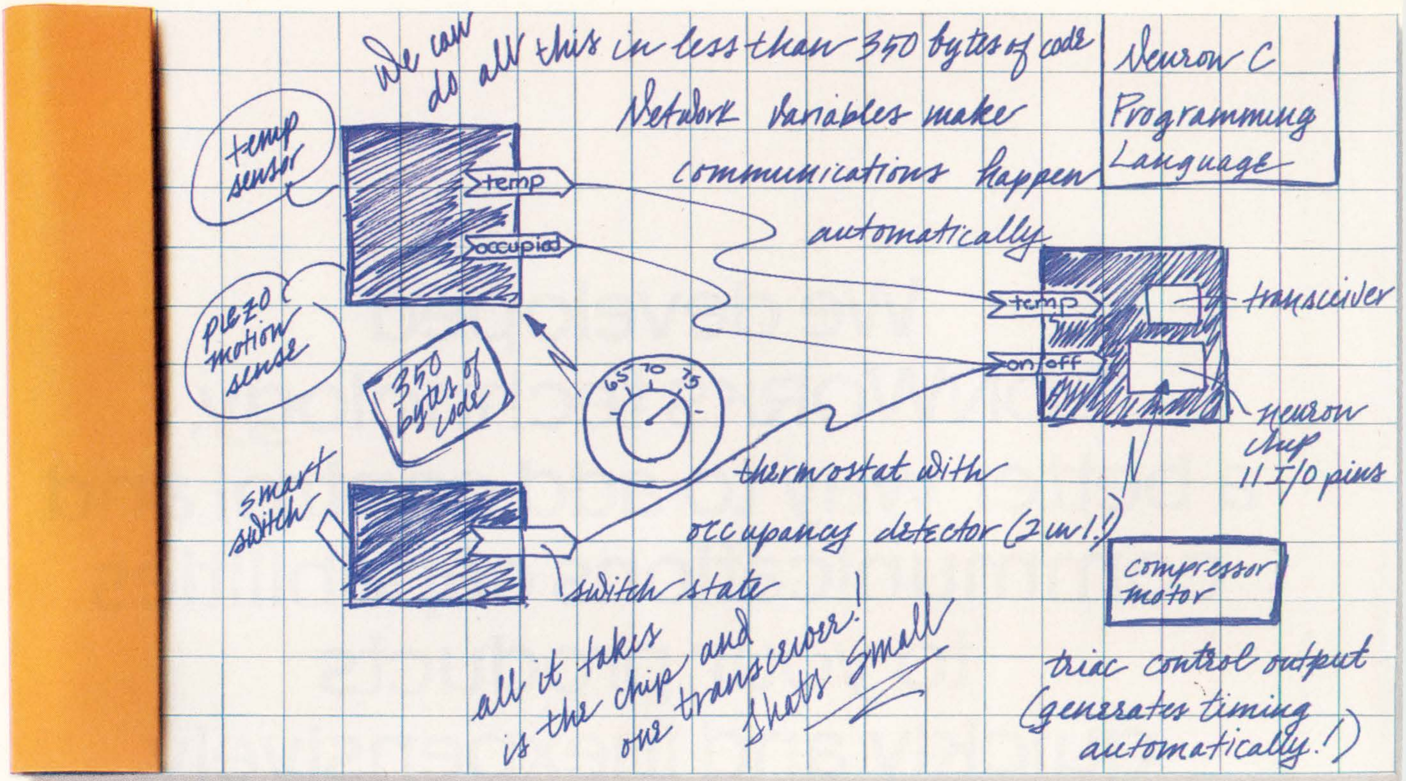
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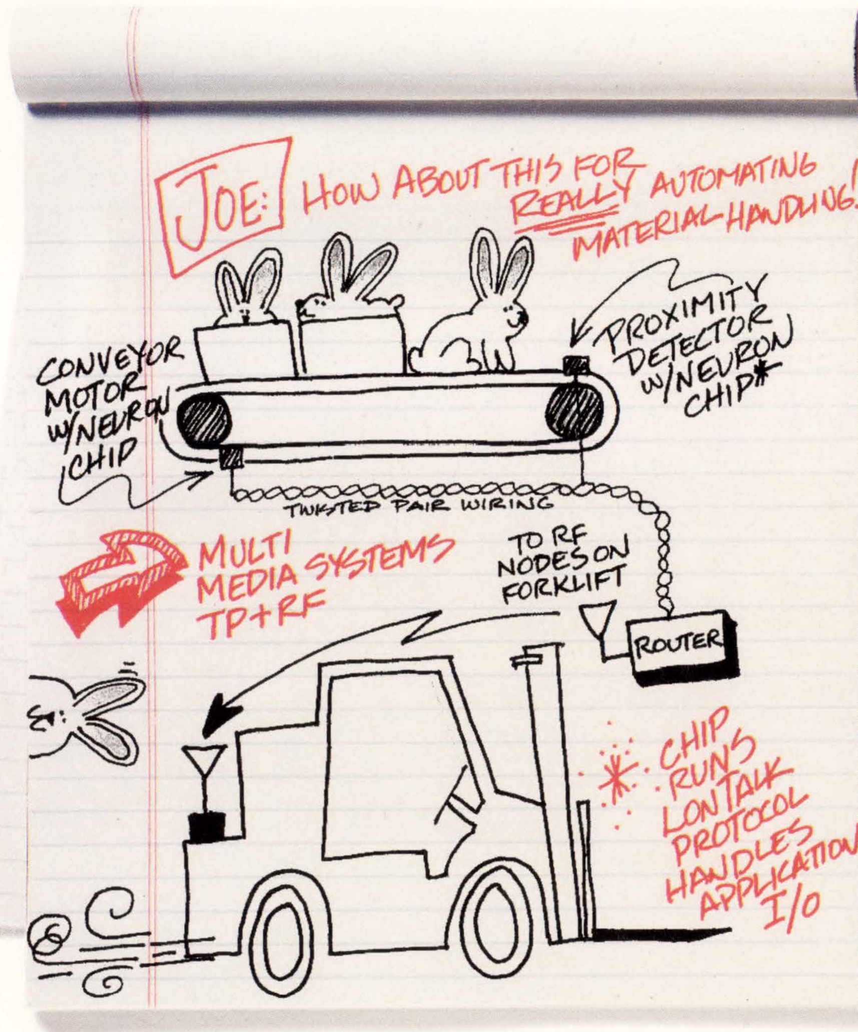
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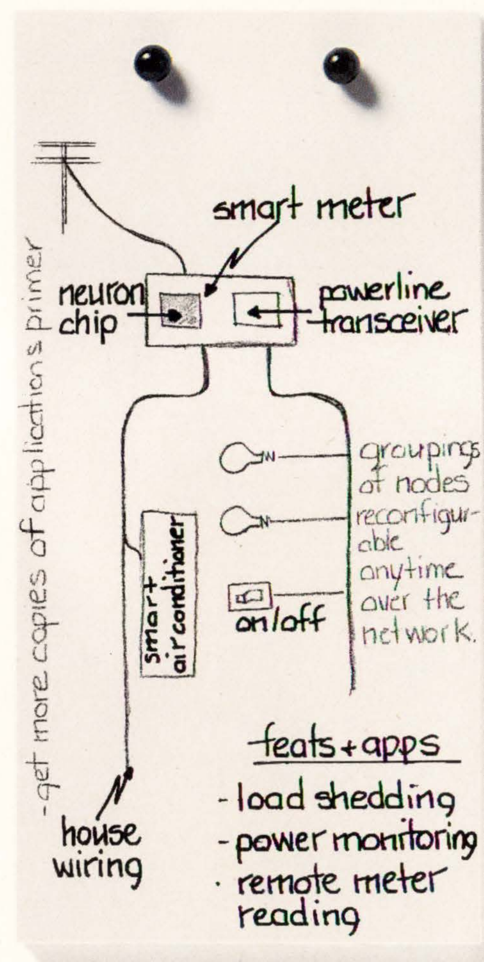
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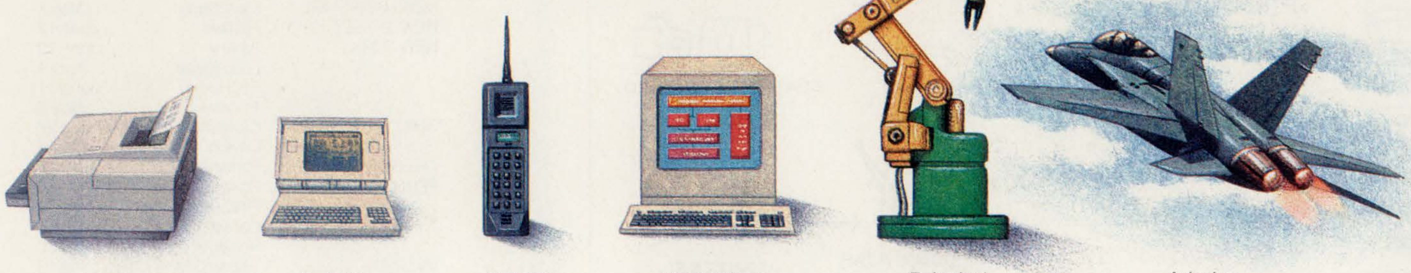

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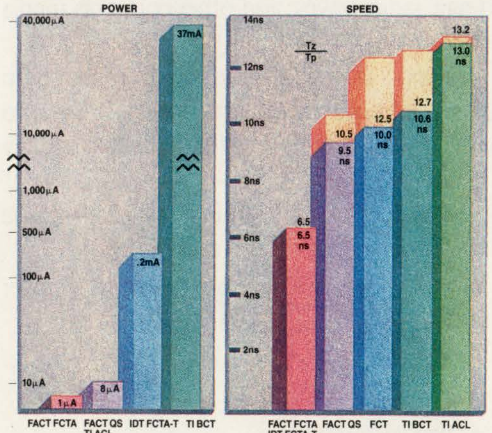

Databook worst case (commercial temp.) Prop delays = '374
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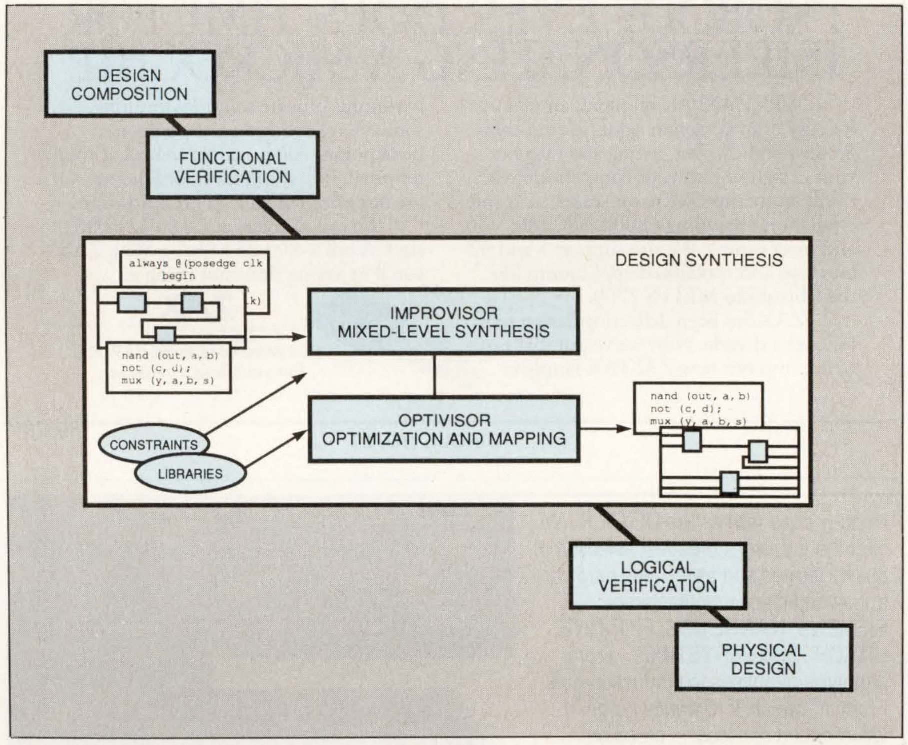
*From a 1990 study conducted by Washington Labs Inc., a subsidiary of Violette Engineering Corporation.

Logic-synthesis software shares simulation model libraries



By sharing a single model library with simulation and layout tools, *the Improvisor and Optivisor logic-synthesis software can closely integrate the design flow.*

The Improvisor and Optivisor are logic-synthesis tools that begin their existence using the Verilog HDL (Hardware Description Language). Unlike synthesis tools that accept VHDL (VHSIC Hardware Description Language) input, these tools can synthesize any construct allowed by the HDL.

Although the IEEE has sanctioned VHDL as an industry-standard HDL (IEEE-1076-1987), VHDL has a few shortcomings. The Improvisor and Optivisor synthesis tools address the major chinks in the VHDL armor.

First, Verilog-HDL ASIC libraries are currently more prevalent than VHDL ASIC libraries. The synthesis tools allow you to use the same library to drive both the synthesis and the simulation of your design. Rather than simulating to verify the approximate delay paths provided by the synthesis models, the delay from the synthesis tools will be the delay from the simulator. As a result, the tools perform some static-timing analyses. Consistent model libraries also allow you to use the Veritime and Verifault timing- and fault-analysis tools.

VHDL's second weakness is that, as a simulation language, it cannot synthesize some of its constructs. This shortcoming can cause problems for designers who don't limit their use of VHDL in designs that are to be synthesized. The synthesis tools, however, can synthesize the entire Verilog HDL.

Like the synthesis tools from Synopsys (Mountain View, CA), these tools divide the conversion of HDLs into logic as two operations. First, the Improvisor lets you perform architectural tradeoffs using RTL-level behavioral models. Then the Optivisor allows you to optimize the design for your particular performance or area needs.

The synthesis tools are integrated within the company's IC-and systems-design tool suites. In fact, where many simulation tools can extract delay information introduced by a circuit's physical layout, the Improvisor goes one better. Because the synthesis tools use the same library as the simulation tools, the synthesis software accepts delays added by the layout.

Back-annotated physical delays allow you to find, modify, and resynthesize paths whose performance falls out of specification as a result of layout effects. You can minimize the effect and time penalty of resynthesis by defining the section of code you want to synthesize. Also, going back to the HDL source code maintains data consistency and the integrity of your design.

To optimize your logic, the software uses two algorithms. A fast algorithm optimizes the circuit, using algebraic rules that treat the circuit as a polynomial equation. This algorithm temporarily replaces variables that it can't understand, such as inverted signals, with variables that it can understand. The second, more thorough algorithm optimizes the logic, using Boolean algebra rules where concepts such as inverted signals make sense.

You can choose the algorithm that applies to your circuit. However, because the second algorithm is more CPU intensive, it may be more appropriate for arithmetic circuit functions. Conversely, the vendor claims the first algorithm works better on control and random logic.

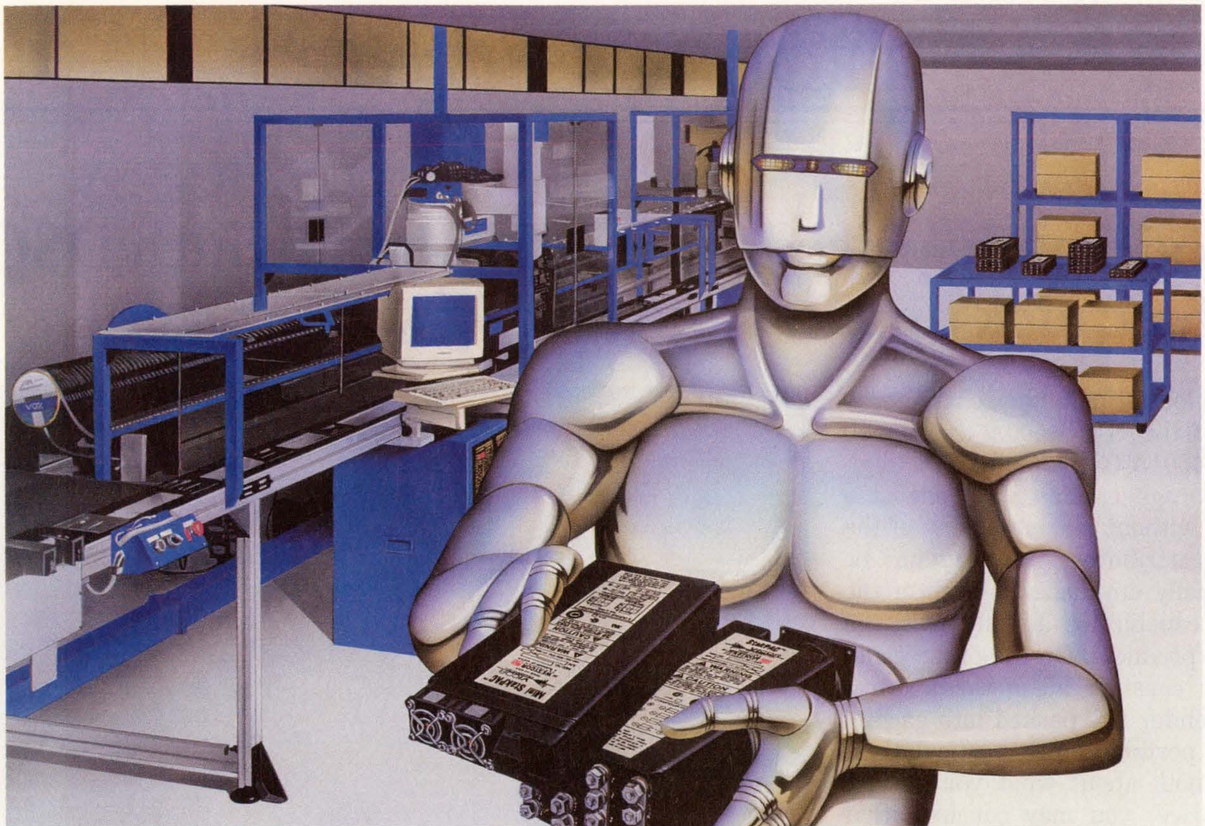
Both software packages run on Unix workstations from DEC, Sun, and HP/Apollo. The logic-synthesizing Improvisor costs $15,000. The cost of the optimization tool, the Optivisor, depends on your hardware configuration. The software's price starts at $35,000 and requires at least one copy of the Improvisor. A subsequent release of the software will accept a subset of VHDL.—***Michael C Markowitz***

Cadence Design Systems Inc, 555 River Oaks Pkwy, San Jose, CA, 95134. Phone (408) 943-1234. FAX (408) 943-0513.

Circle No. 731

WHAT'S COMING IN EDN

EDN Magazine's March 28, 1991 issue will be accompanied by a special supplement on software engineering. That issue begins with a guide to embedded DOS. Also, see our staff-written report on object-oriented programming and other useful software-related stories.



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SP1-1603	12 @ 100				
SP1-1604	15 @ 80				
SP1-1605	24 @ 50				
SP1-1606	28 @ 42				
SP1-1607	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8
Seven Output					
SP7-1801	5 @ 60	12 @ 16	12 @ 16	24 @ 8	24 @ 8
	#6	#7			
	5.2 @ 28	2 @ 30			

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*Standard models supply 1100 watts; high-powered version 1200 watts. Please contact the factory.

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ST1-1402	5 @ 120				
ST1-1301	12 @ 50				
ST1-1302	15 @ 40				
ST1-1303	24 @ 25				
ST1-1304	28 @ 21				
ST1-1305	48 @ 13				
Dual Output					
ST2-1401	2 @ 60	5 @ 60			
ST2-1402	5 @ 60	5 @ 60			
ST2-1403	5 @ 60	12 @ 33			
ST2-1404	12 @ 33	12 @ 33			
ST2-1405	15 @ 26	15 @ 26			
Triple Output					
ST3-1401	5 @ 60	12 @ 16	12 @ 16		
ST3-1402	5 @ 60	15 @ 13	15 @ 13		
ST3-1501	5 @ 90	12 @ 8	12 @ 8		
Quad Output					
ST4-1401	5 @ 30	12 @ 16	12 @ 16	5 @ 30	
ST4-1402	5 @ 30	15 @ 13	15 @ 13	5 @ 30	
ST4-1403	5 @ 30	12 @ 16	12 @ 16	24 @ 8	
ST4-1501	5 @ 30	15 @ 13	15 @ 13	24 @ 8	
ST4-1502	5 @ 60	12 @ 16	12 @ 8	5 @ 15	
ST4-1503	5 @ 60	15 @ 13	15 @ 7	5 @ 15	
ST4-1504	5 @ 60	12 @ 16	12 @ 8	24 @ 4	
ST4-1505	5 @ 60	15 @ 13	15 @ 7	24 @ 4	
Five Output					
ST5-1501	5 @ 30	12 @ 16	12 @ 16	5 @ 15	24 @ 4
ST5-1502	5 @ 30	15 @ 13	15 @ 13	5 @ 15	24 @ 4

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CIRCLE NO. 60

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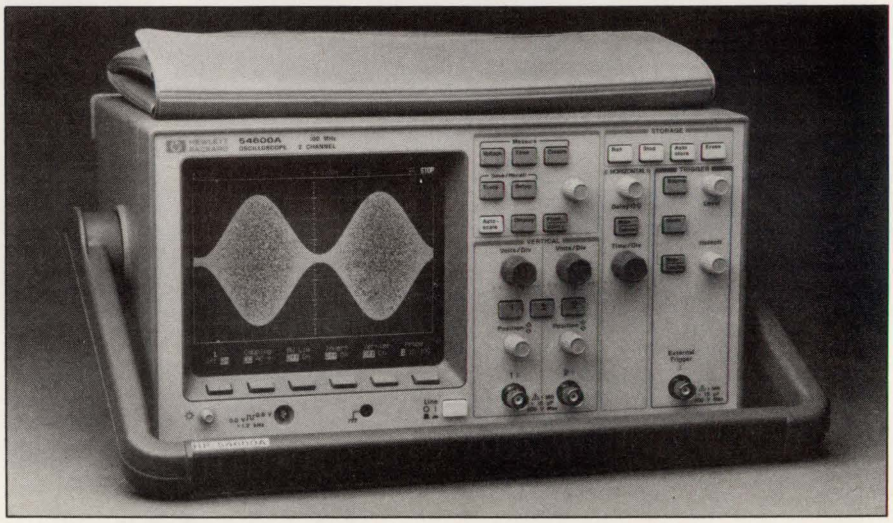

***"Analog feel" in a digital scope** involves more than just familiar controls. The HP 54600A and 54601A DSOs offer users a speedy display-update rate. In addition, an autostore mode provides infinite persistence in combination with a superimposed bright display of the last waveform captured.*

If you look at individual characteristics of the HP 54600A (2-channel) and 54601A (4-channel) DSOs (digital storage oscilloscopes) one at a time, without looking at any of the other attributes, you may not be especially enthusiastic; each of the DSO capabilities already exists in other products. On the other hand, if you consider all of the features the vendor has packed into each of these portable units, particularly if you think about what you get for the price, you may conclude that these oscilloscopes are indeed revolutionary.

You would be hard-pressed to disprove the assertion that no scope makes the power of digital technology more accessible. In this case, accessibility refers to affordability as well as ease of use. The 2-channel unit costs $3000, and the 4-channel unit costs $3500. Moreover, the controls have the familiar "feel" of analog-scope controls.

Although the use of analog-style controls—separate knobs for such functions as gain, position, and sweep speed—is hardly new in DSOs, these scopes are the vendor's first to incorporate the feature. (The vendor notes that it has no intention of abandoning the menu-driven interface that characterizes its DSOs. The new products, however, will appeal to a wider audience—one for which the analog feel is more appropriate.)

Unlike the majority of comparable units, these units accompany the analog controls with a fast display-update rate. No perceptible lag appears when you observe the output of a circuit under test and manually adjust the parameters of that circuit. With the exception of a few scopes that incorporate high-speed DSP μPs (such scopes have much higher prices than those of the new units), nearly all DSOs exhibit a noticeable lag in display updates. DSO vendors don't like to talk about this lag; understandably, their demonstrations don't make it obvious.

The 100-MHz analog bandwidth of the new scopes represents a "magic number." Despite the continuing increase in circuit clock rates, many users still regard 100 MHz as marking the boundary between low- and high-performance scopes. In these units, the bandwidth is usable when you view repetitive waveforms. In addition to their bandwidth, the scopes' maximum vertical sensitivity of 2 mV/div and 8-bit resolution contribute to their broad applicability.

The A/D-conversion rate is 20M samples/sec. Unlike scopes from this vendor that are optimized for capturing single-shot events, these units incorporate no reconstruction filters. Therefore, to obtain repeatable results with nonrepetitive waveforms, you should take 10 samples of each signal cycle. Observing this caveat limits the scopes to displaying single-shot events whose frequency is less than about 2 MHz.

When a DSO designer endows a product with an analog feel, the product need not sacrifice the conveniences users have come to expect of digital scopes. In these units, conveniences include cursor measurements of voltage and time and 12 automatic measurement modes. With an optional parallel, RS-232C or IEEE-488 interface and a graphics-capable printer, you can obtain hard-copy output. Internal memories can store 16 setups, and you can also use the RS-232C and IEEE-488 interfaces to control the scopes.—***Dan Strassberg***

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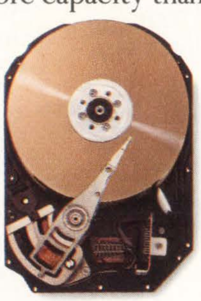

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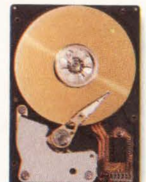

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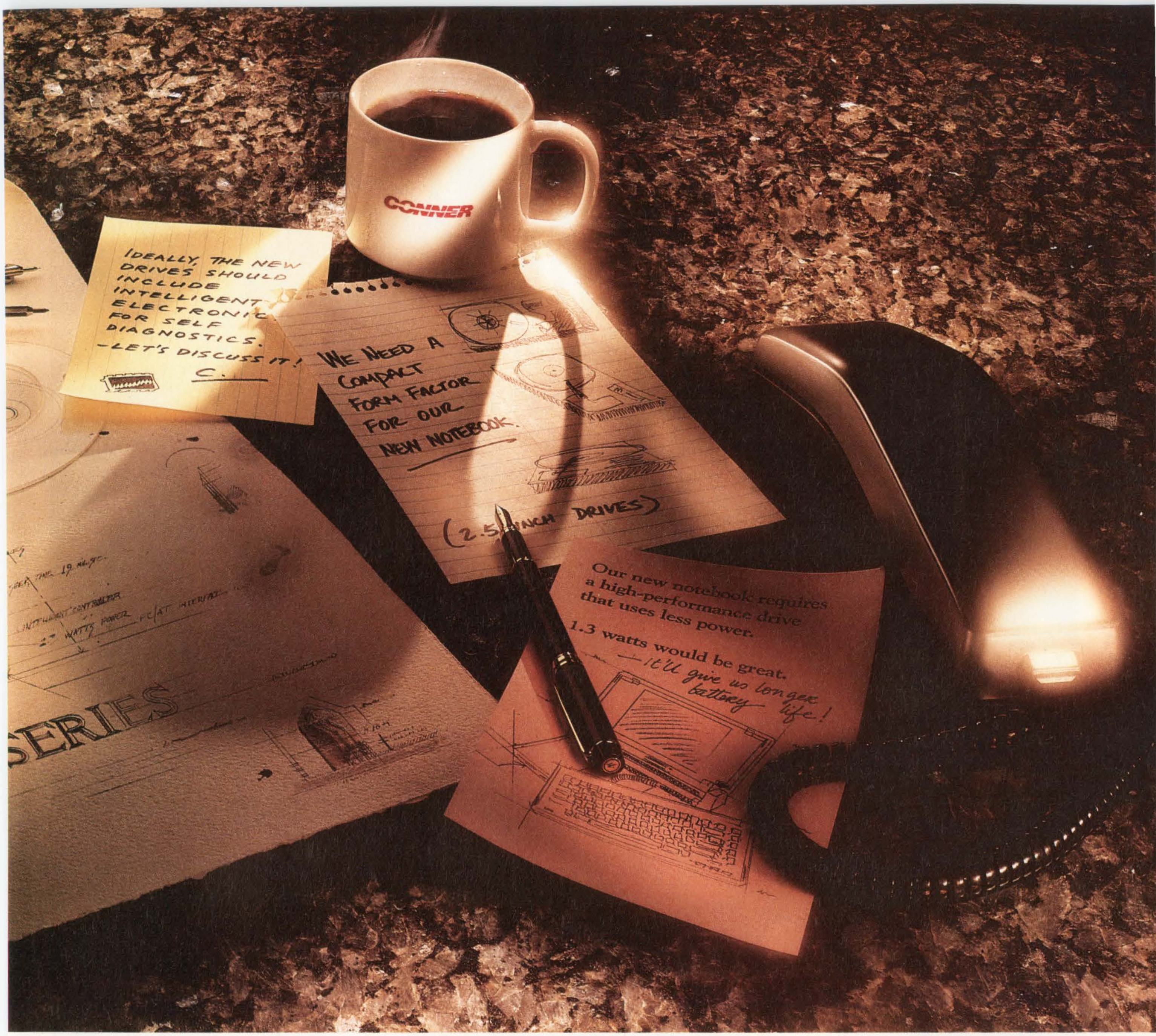

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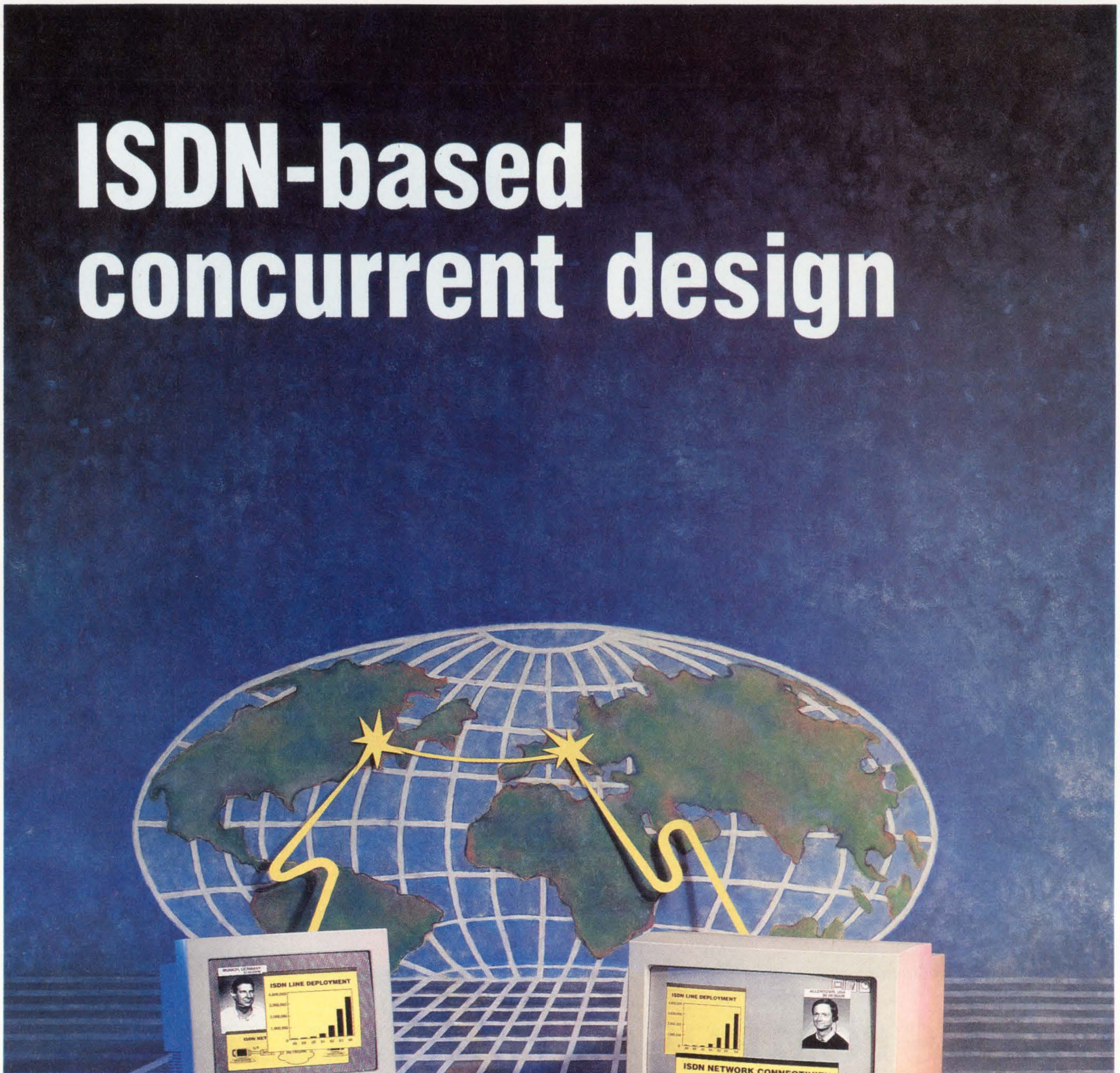
ISDN-based concurrent design



ISDN will let you hold desktop conferences with colleagues all over the globe. (Photo courtesy AT&T Microelectronics; Dave W Morrow, photographer; A Taryn Troiani, art director; Judy A Bullard, assistant artist)

Michael C Markowitz, Associate Editor

High-bandwidth, all-digital telephone lines will let you develop products using simultaneous inputs from everyone with an interest in the product's success.

The Integrated Services Digital Network (ISDN) can merge diverse product-development functions into a single operation. Recent standards-bodies decisions have finally stabilized ISDN, so vendors are beginning to develop applications that will fuse product definition, specification, and design. Don't hold your breath waiting for these new products, though; upgrading and installing all the switching equipment necessary to empower ISDN will take a few years.

ISDN applications fall into three categories: desktop conferencing, networking, and supplementary services. All are possible because of ISDN's inherent advantage over discrete networks: the existing telephone network of approximately 375 million miles of copper cable. The cable provides a universal local-, municipal-, and wide-area network that connects anyone or any machine with access to a telephone line.

Briefly (and with a minimum of acronyms—see **box,** "ISDN acronyms and terms," pg 84), the heart and soul of the Integrated Services Digital Network is a bidirectional, 192k-bps digital communications path. This path comprises two 64k-bps channels (B channels) for voice or data, one 16k-bps channel (D channel) for network signaling and control, and 48k bps of channel overhead for framing and error detection.

Phone interface stays the same

Under ISDN, ordinary phone calls have the same look and feel as they did before. But ISDN's internal workings differ significantly from those of the phone network you're using now. Consider how you place a call using a 2B+D ISDN line. When you dial a number, information such as your number, the number you've dialed, and call-setup data all flow on the D channel to a central-office switch. The switch routes the call through the local or long-distance carrier to the call destination's central office and, ultimately, to the number dialed.

The destination terminal reacts to the call by returning an acknowledgment over the D channel. Your receipt of the acknowledgment completes the connection and lets you send voice or data over one of the B channels. The second B channel gives you a range of options. You could carry on a conversation on one B channel while exchanging data on the other B channel. Alternately, you could send information on the second B channel to a second destination. You can use the D channel to send messages or data to yet another destination. Now, apply this convenience to your design responsibilities.

Sequential product design begins when marketers create a specification. They then turn this spec over to the designers. Design engineers design to meet the spec before throwing the project over the wall to the test and manufacturing people. The inefficiencies of this sequential method have forced companies to consider multidiscipline project teams that include marketing, design, test, and manufacturing personnel. Merging all of a product's development into a single operation is called concurrent engineering and is much easier when all personnel are on one campus.

Multisite concurrent engineering becomes possible by integrating design, marketing, manufacturing, reliability, and management functions via a dial-up, universal network. ISDN extends concurrent en-

COMMUNICATIONS
SPECIAL ISSUE

ISDN can connect any person, computer, or machine that has access to a phone line to any other person, computer, or machine with similar access.

gineering to include both customers and suppliers. Including the customer and supplier in the design from the beginning offers substantial benefits: You ensure a buyer for the product you're creating, and you'll know that the components you need will be available.

Request, send, and analyze data in one call

Contrast a voice and data party line with using a facsimile machine. A simple fax transaction currently requires three separate phone calls—the first to request the fax, the second to send it, and the third to discuss it. Using ISDN lets you complete the same transaction with one call. While you and your associate converse on one B channel, you can send your data across the second 64k-bps B channel, which is more than six times as fast as 9600-baud fax machines.

To lower costs, future fax machines could use either the high-speed B channel or the slower-speed D channel. Most users could send facsimile transmissions on the 16k-bps D channel using fax machines connected to their computer networks. The speed and image quality would be comparable to the transmissions of existing fax machines. The costs, however, will be lower because the D channel sends packet-switched data, for which you pay by the packet rather than for connect time. Engineering users who need better quality and faster throughput than D channel transmissions offer could attach next-generation fax machines to a B channel to transmit at either 64k or 56k bps.

But sending a fax is hardly concurrent engineering. Desktop conferencing *is* concurrent engineering. An ISDN 2B + D line lets two people in remote locations converse and share a workstation session via access to each other's local-area network. You and a colleague could discuss and write a project specification using a word-processor program, enter financial projections into a spreadsheet, draw a schematic, or run and evaluate a circuit simulation.

One workstation controls the application; the other acts as a dumb terminal. Control of the application passes between the two users via a message on the D channel. The desktop conference would demand only that each workstation have an internal ISDN terminal adapter. Expanding the conference to include multiple

An ISDN acronym workout

No article about ISDN would be complete without a quick tour of the network. And no tour of ISDN would be complete without using at least 10 acronyms:

The CCITT (Consultative Committee on International Telegraph and Telephone) standard defines several reference points within ISDN **(Fig A)**. Starting at the CO (central office) switch, the V interface connects the ET (exchange termination) to the LT (line termination). The V interface, ET, and LT all exist within the CO.

A 2-wire link called the U interface runs from the central-office switch to the subscriber's premises. Inside the premises, the 2-wire link becomes a 4-wire link at the NT1 (network termination 1) box. The 4-wire link allows extension phones; the 2-wire link doesn't.

If the box connects to company-owned or -leased private switchboards, it uses the T interface and terminates at an NT2 (network termination 2) box. Otherwise, the box uses the S interface to connect to the TE1 (terminal equipment 1). You can also connect non-ISDN equipment to the network by inserting a TA (terminal adapter) between the TE2 (non-ISDN equipment) and the S interface.

The S interface, unlike the other interfaces, allows point-to-multipoint operation in addition to point-to-point operation, but does not let you cascade ISDN terminals. As a result, the network permits additional extensions only from the T interface at the NT2 box.

Many of the capabilities that ISDN provides are available today via leased 24-channel, 1.544M-bps lines (T1). However, these lines are dedicated and inflexible, and you pay for them whether you use them or not. In contrast, ISDN offers on-demand, dial-up access for any two ISDN-ready sites. And because ISDN is a switched rather than a dedicated service, ISDN can route around failed network components.

participants would require adding control software. This ISDN conference would minimize or eliminate throw-it-over-the-wall sequential design flow by putting project team members a phone call away.

ISDN is a network

In addition to desktop conferencing through workstations connected directly to ISDN, you can also use ISDN to connect to existing local- and wide-area networks. These gateway applications let you connect to any remote homogeneous or heterogeneous networks via the telephone network.

Using an RS-232C cable between a Macintosh Appletalk network and an ISDN terminal adapter, you can use ISDN as a gateway into Appletalk. An ISDN-Ethernet bridge allows access into Ethernet networks. ISDN also enables gateways between token-ring networks.

Some of the supplementary features of ISDN also facilitate concurrent engineering. Engineering organizations can use these features to provide better service to their customers and tighter integration to their field representatives. These features include automatic number identification, automatic call back, messaging, electronic directories, call waiting, and call forwarding.

Because your number is sent out with the call-setup data, equipment at the destination can decode the source address and reference it to data stored in a computer memory. Based on the results of the comparison, an internal network at the destination can identify the calling party and route the call to a specific application, shipping, marketing, or design source. In addition, the person who fields the call can have all appropriate information on his or her workstation terminal before picking up the handset.

In fact, a mail-order firm had this capability in an ISDN trial a few years ago. The firm thought answering the phone with the customer's name would improve both service and customers' impressions. The company learned otherwise. Customers became highly suspicious, confused, or disoriented when they were greeted by name before they even had a chance to say hello.

Although the initial results of this trial were disappointing, consider the time savings for both callers and callees. Suppose, for example, your personal computer goes down or you need to order more memory to run a CAE application in Windows 3.0. You call your friendly out-of-the-neighborhood mail-order company, but all the attendants are busy. Do you postpone everything else while you hold the line? If the mail-order company has the appropriate ISDN services, you're

Text continued on pg 86

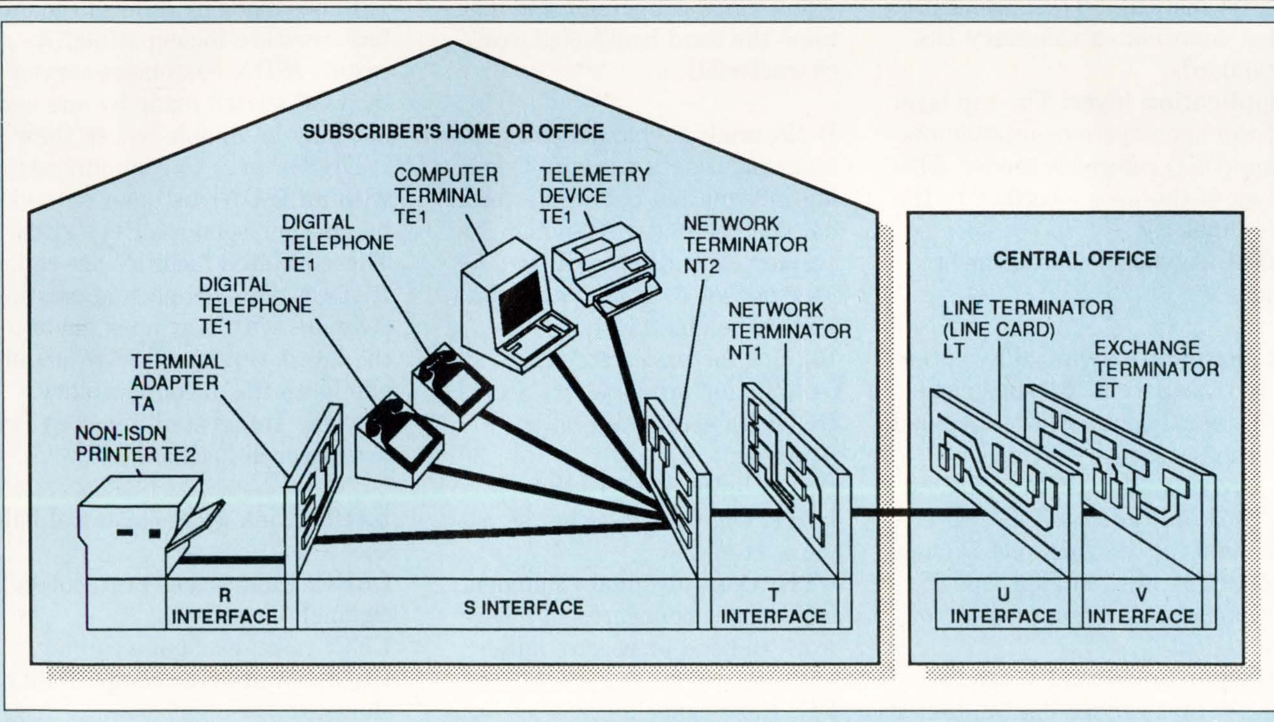


Fig A—Understanding all the interfaces and equipment *that you can connect to ISDN is easier if you visualize the network.*

ISDN acronyms and terms

Historians credit former US President Franklin Delano Roosevelt and the New Deal with creating an avalanche of acronyms to lift America out of the Great Depression. Roosevelt and the New Dealers have nothing on ISDN.

You won't need an immersion language course to use the features that the Integrated Services Digital Network provides. However, you'll need more than just a quick read through the following list to understand the technobabble spouted by the ISDN intelligentsia, who seem to create an acronym for any combination of words they use more than once. (ISDN elite might want to test themselves by seeing how many of the 68 acronyms they can define.)

ADPCM: Adaptive differential pulse-code modulation.
AMI: Alternate Mark Inversion. A trilevel coding scheme for transmitting data.
ANI: Automatic number identification.
ANSI: American National Standards Institute. The organization that coordinates voluntary US standards.
Application layer: The top layer of the open-systems-interconnection (OSI) reference model. This layer is the user interface to the terminal.
ATM: Asynchronous transfer mode.

B channel: A switchable, optionally transparent, 64k-bps channel; two B channels are included in the basic-rate service.
Basic rate: An ISDN access rate of 192k bps allocated as two B channels of 64k bps, one D channel of 16k bps, and 48k bps of overhead for framing and error detection.
BISDN: Broadband ISDN. An ISDN that carries digital data at rates of 1.544-MHz or higher by putting the data into fixed-length packets.
BRA: Basic-rate access.
BRI: Basic-rate-access interface.
BRITE: Basic-rate-interface T extension.

CCITT: Consultative Committee on International Telegraphy and Telephony. The international standards body responsible for ISDN.
CCS: Common-channel signaling. See also SS#7.
Circuit switching: Establishing a dedicated path between two devices via switching nodes.
CO: Central office.
Codec: Coder-decoder. A device that translates analog data into digital bit streams and vice versa.
Common carrier: In the US, generally long-distance telecommunications companies.
CPE: Customer-premises equipment.
CRC: Cyclic redundancy check.
CSD: Circuit-switched data.
CSDN: Circuit-switched digital network.
CSU: Channel service unit. Provides signal conversion and maintains the local loop's electrical characteristics.

D channel: A channel whose primary purpose is to convey signaling information between a terminal and the network switch. Its surplus capacity can be used for user packet data and other data such as telemetry. It operates at 16k bps for basic-rate access and 64k bps for primary-rate access.
DCE: Data communications equipment.
DSL: Digital subscriber loop.
DSS1: Digital subscriber signaling system 1.
DTE: Data-terminal equipment. Equipment connected to a network to send or receive data.

EC: Echo canceling.
ET: Exchange termination.

FDM: Frequency-division multiplexing. Multiple-source data transmission over a line using different transmission frequencies for each source's data.
4B3T line code: 4 binary bits are converted into 3 ternary bits for transmission across the U interface.
Frame: Transmitted bits that define, either through timing protocols in synchronous transmission or sequence in asynchronous transmission, a transport element.

Gateway: A connection between multiple networks.

HDLC: High-level datalink control. A protocol for bit-oriented, frame-delimited data communications.

IDN: Integrated Digital Network.
ISDN: Integrated Services Digital Network. Supports digitized voice, data, text, and image transmission.
ISDN islands: Central-office switches made by different manufacturers are incompatible. As a result, ISDN customers served by a CO switch made by one vendor may be unable to use their ISDN features to communicate with an ISDN customer served by another vendor's CO switch. These isolated facilities are called ISDN islands. Replacing existing switches with new ones made to the latest version of SS#7 should eliminate this incompatibility.
ISPBX: Integrated-Services Private-Branch Exchange.

LAPB: Link-access-protocol balanced.
LAPD: Link-access-protocol on D channel.
LEC: Local-exchange carrier.
LLC: Lower-layer compatibility element.
LT: Line termination. A line card

that terminates the subscriber loop at the PBX or central office.

NCTL: Network channel-terminating equipment.
NT1: Network termination 1. A box that physically and electromagnetically terminates the 2-wire U-interface transmission line and converts the line into the 4-wire S or T interface.
NT2: Network termination 2. A box that switches and concentrates subscriber's lines at the S interface.

OSI reference model: Defines a 7-layer architecture of communications functions that contains the application, presentation, session, transport, network, data-link, and physical layers.

PABX or PBX: Private (automatic) branch exchange. Essentially an automatic private switchboard linked to the central office via a trunk line.
Packet switching: Transmission by breaking up messages into smaller packets and independently sending them to their destination, where they are reassembled to recreate the message.
PCM: Pulse-code modulation. Regularly sampling an analog signal and converting the sample to a binary number.
PCTA: Personal-computer terminal adapter. Allows the personal computer to act as an ISDN terminal.
PDN: Public data network.
PID: Protocol identifier.
POTS: Plain, old-fashioned telephone service.
PRA: Primary-rate access.
Primary rate: An ISDN access rate of either 1.544M bps—23 B channels and one 64k-bps D channel, which is the North American and Japanese standard—or 2.048M bps—30 B channels and one D channel, which is the European standard.
PRI: Primary-rate access interface.
PSDN: Public-switched data network.
PSPDN: Public-switched packet data network.
PSTN: Public-switched telephone network.

R interface: Connects TA to non-ISDN TE2 equipment, often through an RS-232C port.
RBOC: Regional Bell operating company.

S interface: A reference point at the customer premises to which you can connect either an ISDN terminal (TE1) or a terminal adapter (TA); for example, the interface through which a digital telephone could connect to a PABX. This interface accommodates point-to-point and point-to-multipoint operation.
SAPI: Service access point identifier.
SDLC: Synchronous data-link control. A bit-oriented data communications protocol that IBM developed.
SLIC: Subscriber's line interface circuit.
SMDI: Simplified message desk interface.
SNA: Systems network architecture. A network architecture for IBM computer products.
SONET: Synchronous optical network. A standard for optical network elements.
SS#7: Signaling system 7. A family of standards that define message-transfer protocols, error and overload recovery, and call-related services.
STDM: Statistical time-division multiplexing. Allocates bandwidth based on the amount of data being sent by assembling data packets.

T1: The US's basic 24-channel, 1.544M-bps pulse-code-modulation system.
T1D1: The subcommittee (D1) of the T1 committee of the American National Standards Institute responsible for ISDN.
TA: Technical advisory.
TA: Terminal adapter. Connects non-ISDN terminals (TE2) to the digital network via the S interface. The interface between the TA and the TE2 is the R interface.
TCM: Time-compression multiplexing.
TDM: Time-division multiplexing. Using time divisions to combine many signals into a higher-bandwidth signal.
TE: Terminal equipment. A TE1 or a TA and a TE2.
2B1Q line code: 2 binary bits are converted into 1 quaternary bit for transmission across the U interface.
TE1: Terminal equipment type 1. Standard ISDN terminal equipment that you can connect to the S or T interface.
TE2: Non-ISDN terminal. Connects to ISDN via a terminal adapter.
TEI: Terminal endpoint identifier.
T interface: Electrically identical to the S interface, the T interface has a different protocol than the S interface to link NT2 boxes to the NT1 box.
TR: Technical requirements.

U interface: A twisted-pair subscriber loop that provides basic-rate access to the NT1 reference point from ISDN. Supports only point-to-point operation.
V interface: At the central office, the interface between the line termination and the exchange termination.

VAN: Value-added network.

X.25: CCITT standard that defines the interface between packet-type equipment and the phone system.

treated to a personalized message that promises the company will call you back when an attendant is available.

The order takers at mail-order companies would spend less time on the phone with each customer because order entry would be limited to the order itself; the customer's name, address, phone number, and account history would appear on the attendant's workstation as the attendant answers the phone. Similarly, when the order taker returns your call, all your account information would already be on the workstation before you answer.

Line busy? Leave a message

To improve the security of their local-area networks, many companies without ISDN use automatic call back to prevent unauthorized access. ISDN extends this application by enabling your internal communications system to monitor your phone. If you are unavailable for a call—either because you're away from your desk or on another call—the system reads the incoming call data. The system then looks up the phone number in an on-line database and stores the pertinent information in a call-back file. Your phone system also sends a message to your terminal notifying you of a message.

When you query the system, it displays the phone number stored during the initial call. The system can also display other relevant information, such as the caller's name, account, and clearance level. In addition, the system could call back the originating number. Automatic call back ensures that companies don't accidentally ignore customers' orders, requests, and comments; suppliers' inventory questions; test engineers' test-program development questions; or product managers' feature-analysis suggestions.

ISDN also gives users the ability to leave voice messages. Like the voice-mail systems in vogue today, ISDN could give users their own message-service box. The network could function as an executive assistant by letting you record a message for the network to deliver to one or more people. You could even schedule the message for delivery at a specific date or time.

Manufacturers of ISDN ICs

For more information on ISDN ICs, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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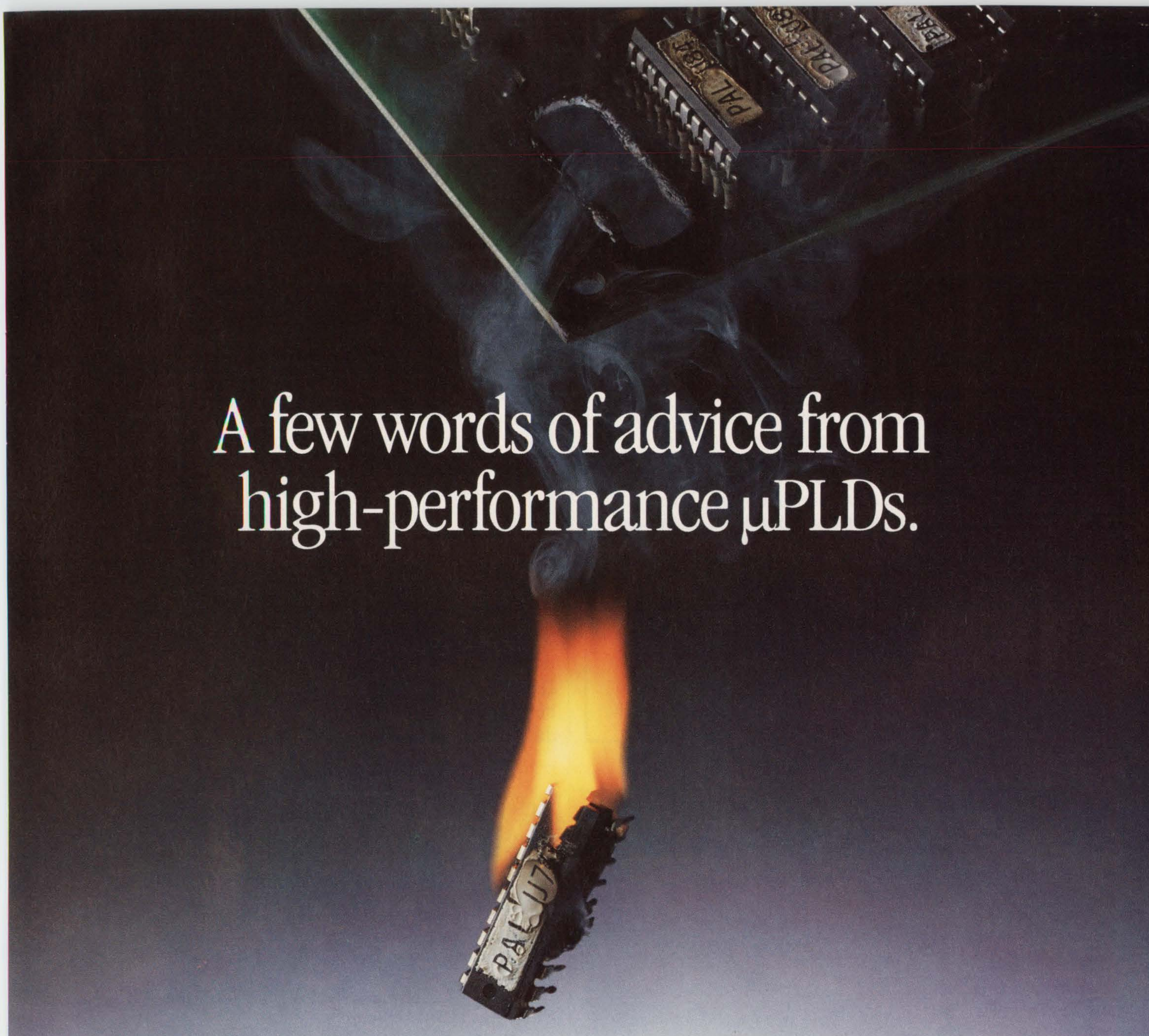

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ISDN-based concurrent design

A feature of ISDN not possible with a nonintegrated voice and data communications network is electronic directory service. To find a phone number and other, nonprivate information about a subscriber, you could query an electronic-directory database. After you receive the response from the database, you could place the call. The distinction from today's system is that rather than manually dialing the number, you hit the Enter key on your telecommunications terminal—much as you would place a call from a communications program. The directory, too, enhances concurrent engineering by putting you closer to the networks of data and people most likely to help your product design.

Most of the capabilities that ISDN offers aren't new. Many, in fact, are available today. What ISDN promises is lower cost and greater convenience than current phone systems. Today you must use multiple phone lines to perform multiple functions. In the future, ISDN will use one phone line to make your workstation both a computation engine and an integrated voice and data transporter. EDN

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Note: For more information on **Refs 1** and **3**, see the Book Reviews on page 181.

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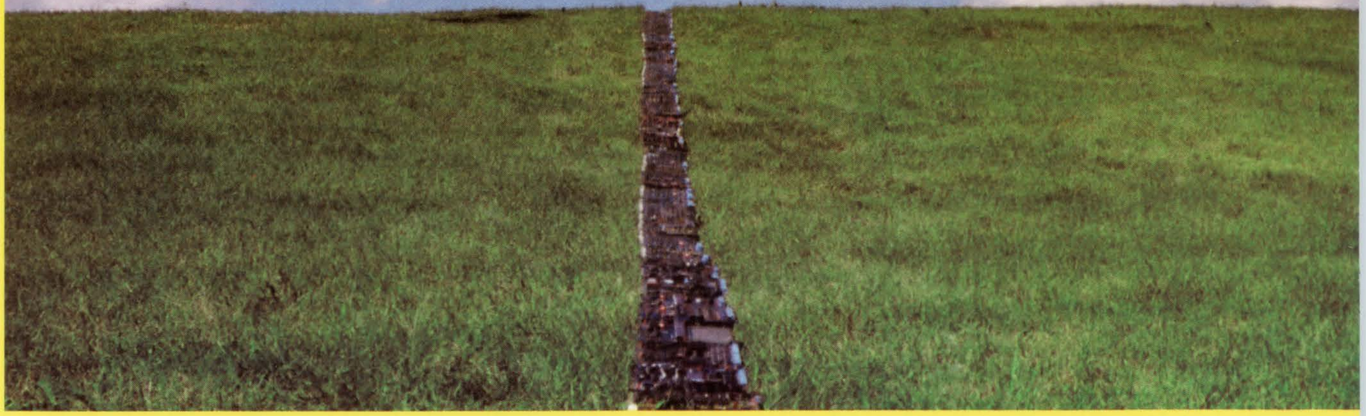

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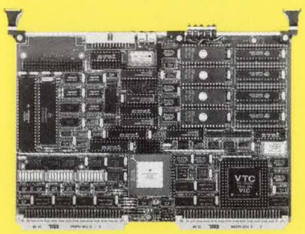

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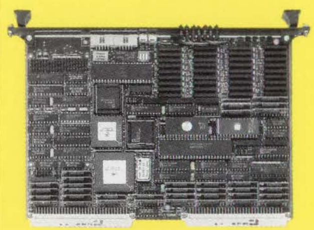

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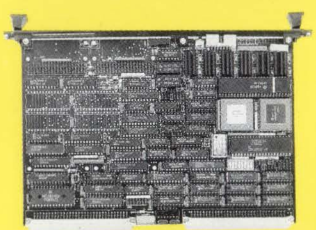

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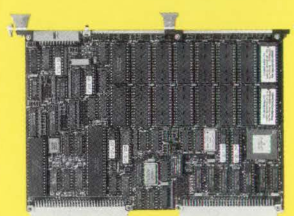

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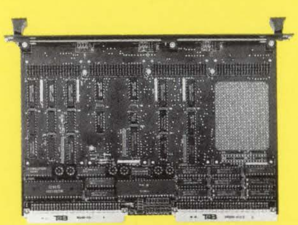

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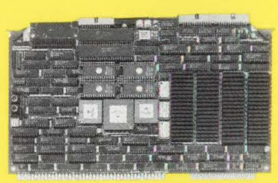

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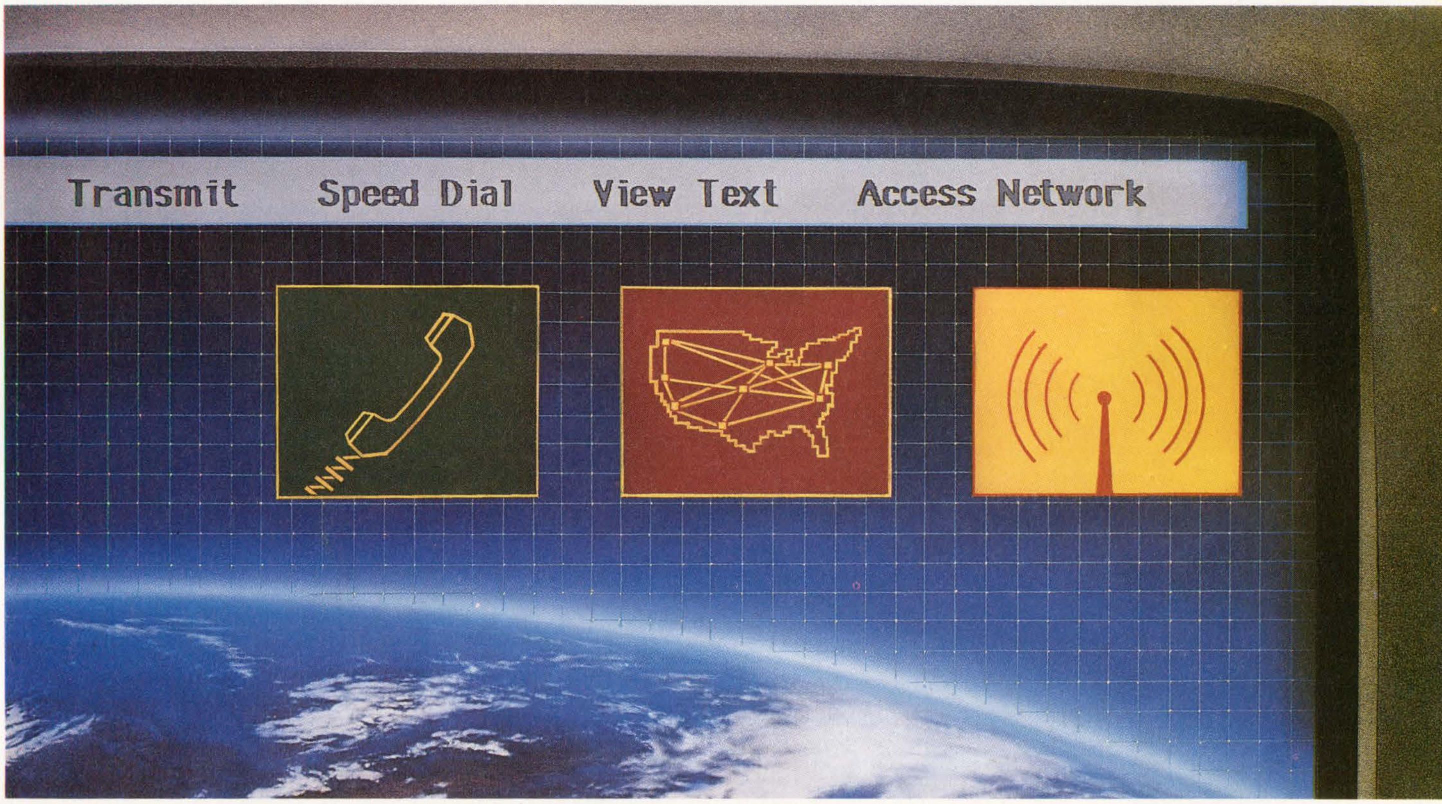

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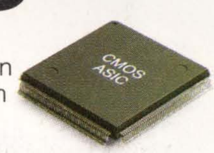

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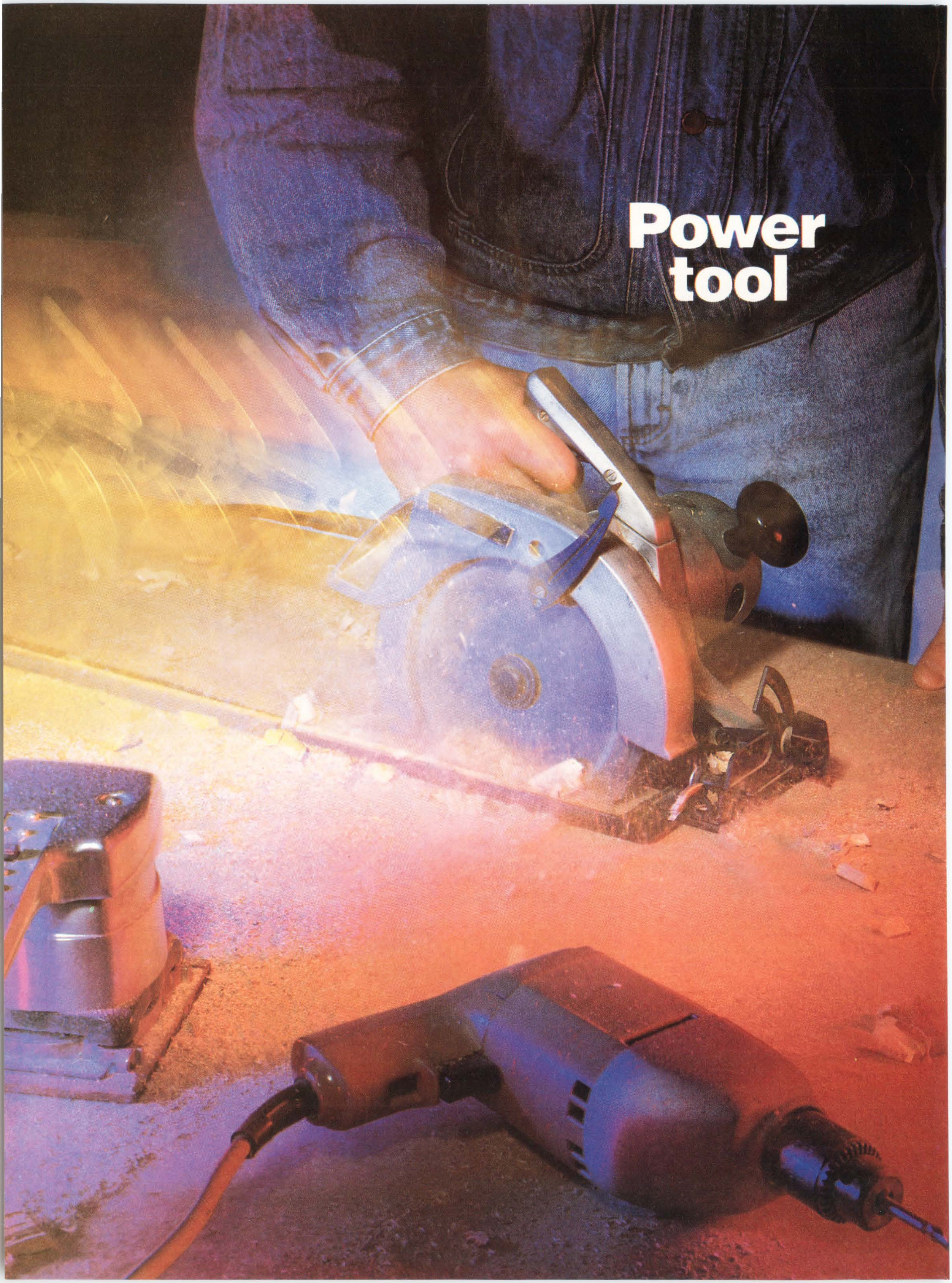
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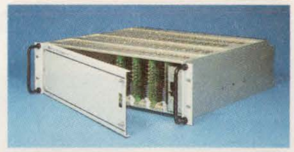

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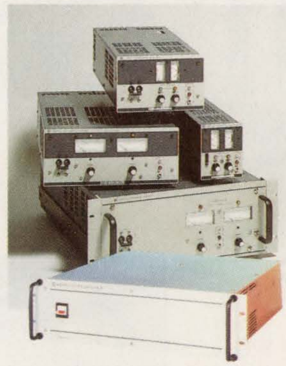

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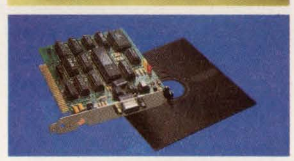

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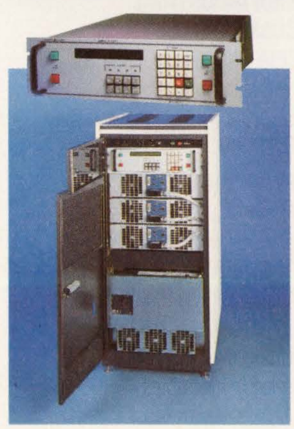

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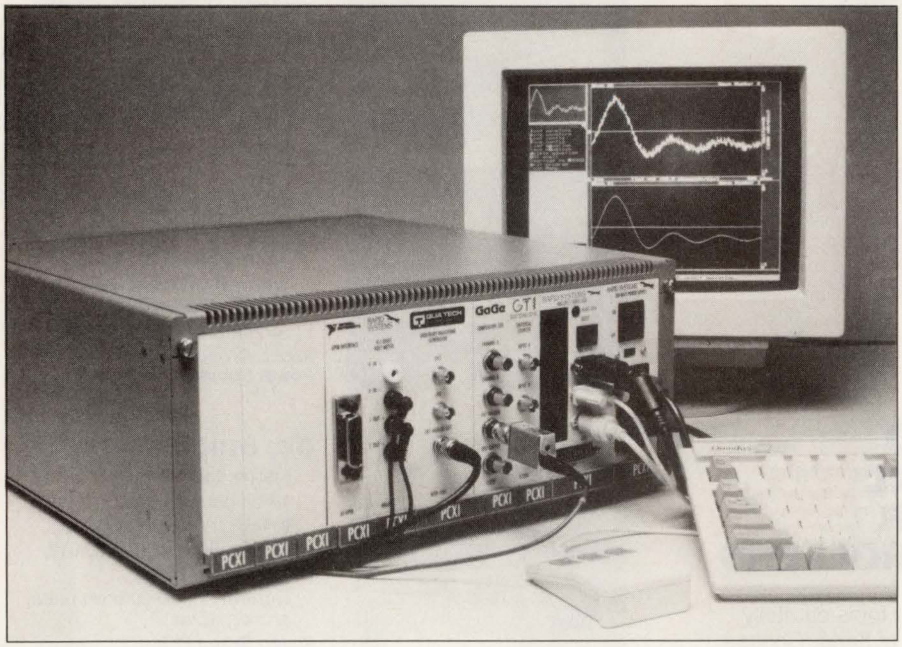

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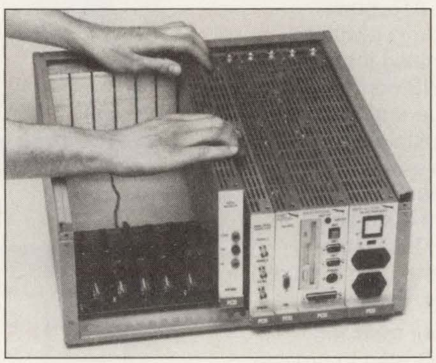

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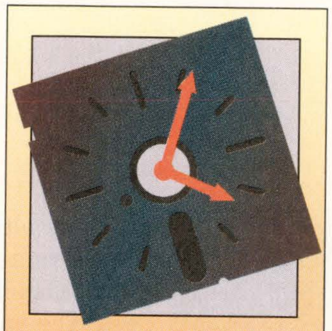

Task coordination: specific methods, general principles

Earlier parts of this series described several types of task coordination. This final installment classifies the various methods, diagrams the relationships among them, and provides guidelines for choosing methods that suit your requirements.

David L Ripps, *Industrial Programming Inc*

Task coordination is a fundamental and essential part of a real-time application. In principle, each task is an independent program that is capable of running asynchronously with respect to all other tasks. In practice, tasks are highly interrelated; they work in unison. Specifically, most tasks act upon the same body of current data. Some tasks bring fresh data into the body, others transform the data, and finally, some output a product or response based on the data. In every case, tasks feed data to each other, with producers and consumers coordinating to be sure that transformations are performed with consistent values.

The last few parts of this series described several different types of coordination that have evolved over many years and hundreds of applications. People have discovered that there is no one universal method that solves all coordination problems easily and efficiently. But they have also discovered that just a small set of basic techniques and methods does suffice for the vast majority of real-time applications.

In essence, coordination is the blocking of a task until some specified condition is met. Often, the condition is a function of information that is produced by one or more tasks and maintained by the operating system. But this need not be the case. With "pause/cancel-pause," for example, coordination is achieved without any transfer or permanent storage of information.

The specific methods of coordination described in previous parts differ significantly in both the nature of the unblocking condition and the type of information involved. These internal differences, in turn, lead to corresponding differences in the user-level characteristics and capabilities of the methods. As a result, the

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> In principle, tasks are independent programs that can run asynchronously with other tasks. In practice, tasks are highly interrelated.

application designer can usually choose a scheme that is exactly right at each point for which coordination is needed.

Nevertheless, to make a proper choice of coordination scheme, the designer must understand what the underlying differences are and how they appear at the task level. This final part attempts to classify the various methods and to diagram the relationships among them. This is an expanded version of a classification scheme originally published in 1983 (**Ref 1**).

Many alternate diagrams could be drawn, each of which represents a valid classification. The goal is to find a classification that will guide in the selection process. The end product is essentially a decision tree: If you need this characteristic, choose this branch.

Single-sided vs double-sided coordination

The first division (**Fig 1**) separates those methods in which only one partner can be held for coordination from those in which both partners are coordinating with each other. Single-sided methods are totally asymmetric: One task issues a wait for a certain condition to be true, another task sets the condition that ends the wait. However, the second task itself cannot be blocked while setting the condition. Furthermore, with most single-sided coordination methods, it is possible that no task waits since the end-wait condition may already have been set before the wait request is

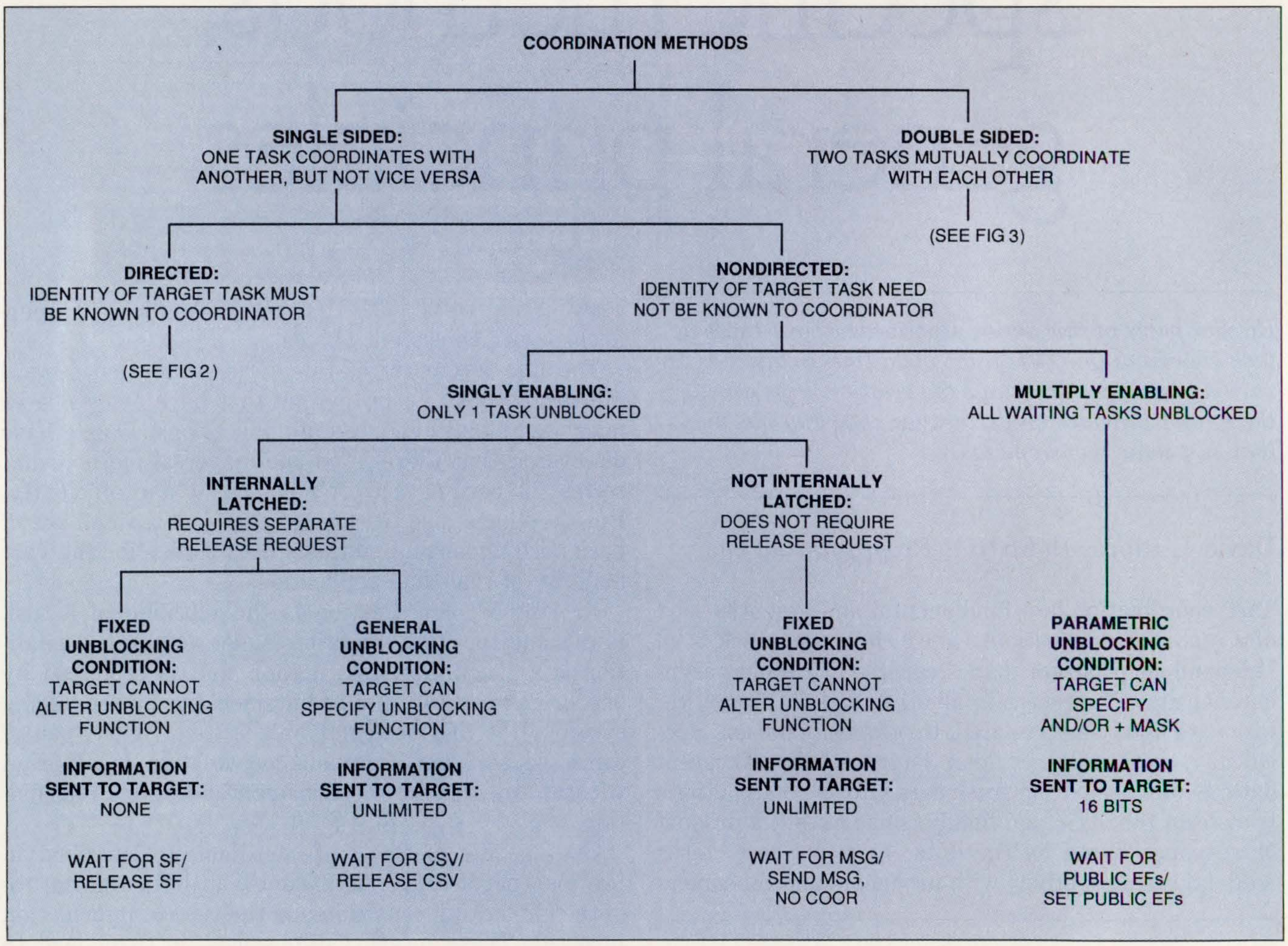

Fig 1—Task-coordination methods can be either single sided or double sided. Single-sided methods are asymmetric: One task issues a wait for a certain condition, and another task sets the condition. With double-sided methods, there is mutual coordination: Either task can wait for the other.

issued. Event flags always provide single-sided coordination.

Coordination can also be double sided to provide a greater degree of symmetry between the partners. With double-sided methods there is a mutual coordination between both partners; either partner can wait for the other. Specifically, the first task to issue a coordination request always waits for the second task to issue a matching request. One task always waits; there is no sense in presetting the end-wait condition. The pair "send-message-to-mailbox-with-wait-for-transfer/receive-message-from-mailbox-with-wait-for-transfer" produces this type of synchronization. However, unless both requests include the optional "with-wait-for-transfer," coordination via a mailbox will not be double sided.

Single-sided coordination

For lack of better terms, the partners in single-sided, task-to-task coordination will be referred to as the coordinator (**C**) and target (**T**), respectively. The target issues the wait; the coordinator sets the end-wait condition to continue the target.

Referring again to **Fig 1**, the next division separates those single-sided methods for which the identity of the target task must be specifically known to the coordinator and those for which such knowledge is not necessary. Consider, for example, the coordination that can be produced by the services *pause* and *canpau* (cancel-pause).

Task **T** pauses (for a given maximum time interval, or "forever").

```
pause (200+MS);
```

When task **C** wants **T** to continue, it cancels that pause.

```
canpau (tskTid);
```

The cancel-pause is always directed at a specific task. Thus, the identity of the target inherently must be known. Furthermore, only that one target task is unblocked, and no message or other information is transmitted from **C** to **T**. (Strictly speaking, when the pause is for limited duration (rather than with **NOEND**), one bit of auxiliary information is sent: Did the pause end because the time elapsed or was it canceled early for coordination?)

The term "directed" refers to those coordination methods for which the identity of the target task inherently must be known to the coordinator. In contrast, coordination based on event flags or messages is "nondirected." The task that supplies the unblocking information need never know the identity of the target task or tasks, if any.

Use directed methods whenever you need direct control over one specific task. Use nondirected methods whenever the coordination is not with any given task, but with any that may be interested or with the next task that has requested coordination. Among the nondirected schemes, public event flags provide broadcast, that is, coordination with any task that may be interested; message exchanges maintain multiple-server queues for coordination with the next available task.

In this discussion, the separation is based on inherent or necessary knowledge. In any given application, there could be only one task waiting for a particular public event flag or at a particular message exchange. Thus, there could be *a priori* knowledge of the coordination target even with public event flags or message exchanges. But this knowledge is not necessary to coordinate via public event flags or messages. With "pause/cancel-pause," target identity is an absolute necessity.

Nondirected methods

At the next lower level in the diagram, nondirected methods can be split further into those that never unblock more than one task upon a change in coordination data and those that unblock all waiting tasks that meet some function of the data. The first class is called singly enabling, the second multiply enabling. Public event flags are multiply enabling. Multiply enabling methods are used mainly for the broadcast of binary coordination data.

Singly enabling coordination methods can be subdivided even further into those that are internally latched by the operating system and those that are not. With latched methods, there is an internal busy/free flag (the latch) that is maintained by the operating system as part of the coordination data. A target task (**TskA**) makes a request to wait until a certain facility (such as a semaphore) is free. When **TskA** is permitted to proceed, the OS sets the flag busy. While the flag is set, the OS will not permit any other target task (**TskB**) to proceed. **TskA** must issue a specific release request to unlatch the facility to permit **TskB** to continue. (In this special case, each task is first the target and then the coordinator for the next target.)

Latched coordination methods provide mutual exclusion, that is, one-task-at-a-time access. Examples are semaphores (SFs) and controlled shared variables (CSVs). The major difference between these methods is the amount of auxiliary information that is associated with the coordination mechanism and the flexibility of

Most tasks act upon the same data. Some tasks add fresh data, others transform the data, and some create a product or response based on data.

the unblocking condition. (The auxiliary information isn't transmitted directly from the coordinator to the target in the same sense that a mailbox message is transmitted. The auxiliary information is associated with the coordination mechanism as a whole, not with any single act of coordination. Thus, the CSVs that the target receives may have been set by several tasks, or by one task at several different times.) SFs work only with the busy/free latch, the identity of the current owner of the latch, and the wait queue; this is all the unblocking function can depend upon. In contrast, CSVs permit complete freedom to maintain any amount of auxiliary information and to use that information in any arbitrary way via the unblocking function.

A message exchange is not inherently latched and hence does not necessarily lead to mutual exclusion. If there are 10 messages available at the exchange, then 10 tasks will be permitted to proceed. Dijkstra's **P/V** coordination works the same way.

Of course, a designer can force a message exchange to be effectively latched by permitting only one message to be posted. The message becomes an external (task-level) latch. Whichever task has been given the message at a given moment has also been granted permission to continue.

Directed methods

Now turn your attention to single-sided, directed methods (**Fig 2**). In selecting among these schemes, it is important to decide if the end-wait condition supplied by the coordinator should be stored or transient. Transient means that the end-wait information is lost if the target is not already blocked. The coordination provided by "pause/cancel-pause" is transient. So is "pause-for-signal/send-signal." (With this mechanism, for pure coordination without "side effects," the response of the target should be to ignore the signal.)

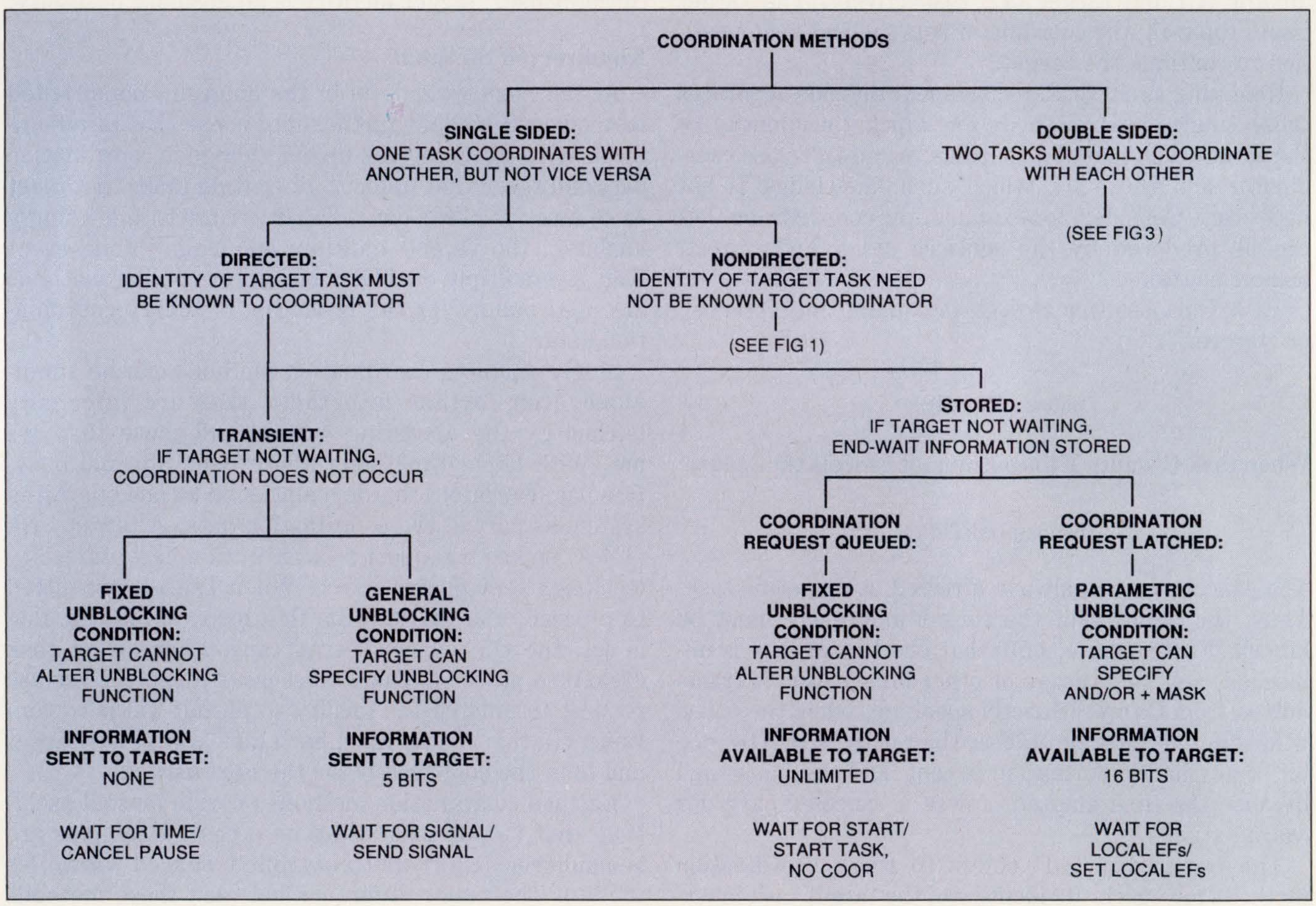

Fig 2—Single-sided task-coordination methods can be either directed—when the coordinating task knows the identity of the target task—or nondirected.

Of the two, "pause/cancel-pause" requires less internal overhead and thus is recommended if no auxiliary data needs to be sent to the target. Since the target task is told which of the 32 signals ended the pause, "pause-for-signal/send-signal" inherently transmits five bits of auxiliary data. Nevertheless, the OS does not retain those five bits after coordination is achieved. If the target doesn't save the information, it is lost.

Use local event flags if you need directed coordination with storage of the unblocking data. Up to 16 bits of data are available per task. However, although the target receives a snapshot of the 16 event-flag bits, they are not strictly information transmitted from the coordinator to the target; other tasks may have set (or reset) some of the bits. Even more important, although the unblocking data is stored, it is held in a single variable (the current value of the local event flags); there is no sense of queuing. Thus, if more than one task attempts to start a given target by setting the same local event flag (or flags), there will be only one continuation.

"Wait-for-start/start-task-without-coordination" is another single-sided method that is directed to a specific task. In this special case, the target is Dormant while it waits. Without stretching the definition too much, interpret Dormant as wait-for-start.

"Wait-for-start/start-task-without-coordination" differs from the local event flags by queuing the requests and thus guaranteeing that each separate act of coordination (ie, start request) will eventually be serviced. Because of the runtime argument, the coordinator can send an unlimited amount of information to the target.

Attributes of task-to-task coordination methods

Method	1	2	3	4	5	6	7
pause (=wait for time)/ cancel pause	SS	DI	SE	NL	FC	TR	none
wait for signal/ send signal	SS	DI	SE	NL	FC	TR	signal number
wait for local EFG/ set local EFG	SS	DI	SE	NL	PC	ST	group value
wait for start/ start task without coordination	SS	DI	SE	IL	FC	ST	runtime argument
wait for semaphore/ release semaphore	SS	ND	SE	IL	FC	ST	none
wait for CSV/ release CSV	SS	ND	SE	IL	GC	ST	variables
send msg with wait/ receive msg without wait or recv msg with wait/ send message without wait	SS	ND	SE	NL	FC	ST	message
wait for public EFG/ set public EFG	SS	ND	ME	NL	PC	ST	group value
wait for start/ start task with wait	DS	DI	SE	IL	PC	ST	runtime argument
send msg with wait/ receive msg with wait	DS	ND	SE	NL	FC	ST	message

Notes:
Column 1: SS = single sided, DS = double sided
Column 2: DI = directed, ND = nondirected
Column 3: SE = singly enabling, ME = multiply enabling
Column 4: IL = internally latched, NL = not internally latched
Column 5: FC = fixed unblocking condition (uc), PC = parametric uc, GC = general uc
Column 6: ST = unblocking condition stored, TR = unblocking condition transient
Column 7: Amount of information transferred

Double-sided coordination

Next, focus your attention on double-sided coordination. The terms target and coordinator that were introduced for single-sided coordination must be redefined if they are to be applied to the partners of double-sided methods. Since in double-sided coordination either partner can wait, the target cannot be defined as the task that issues the wait request. However, double-sided methods always involve at least one transfer of information. The coordinator for double-sided methods is that task that supplies the information and the target is that task that receives the information (at the first transfer if there are two).

Double-sided methods can be subdivided into those that have a unidirectional transfer of information at the coordination point and those that have a bidirectional exchange of information upon coordination (**Fig 3**). When the coordination is achieved via a mailbox (with wait on both the send and receive), there is first a mutual and symmetric synchronization: The first task to arrive waits for the second. Once both tasks have reached the coordination point, the content of one message is transferred from the sender to the receiver. That ends the coordination partnership; both tasks then continue.

In contrast, with the pair "wait-for-start/start-task-with-wait-for-termination," there are two transfers of information, one into the target and another into the coordinator. The target is the task being started. It is either already at the coordination point by being Dormant (waiting for start) or arrives there by issuing a termination request (which is equivalent to wait for restart). The coordinator issues the start request with wait for termination. If the target is not Dormant, the coordinator waits until the target terminates and thus becomes available for restart. In either case, there is an initial mutual synchronization of the two partners. Next, the runtime argument is transferred from the coordinator to the target, and the target continues (restarts at its entry point). However, the coordinator does not continue. It takes a second event, the termination of the target, to continue the coordinator. At that second event, there is another transfer of information, this time a transfer of the return argument from the target back to the coordinator. You can characterize this type of coordination as stimulus/response. The simple Ada rendezvous is also of this type.

The two double-sided coordination methods that

Although no one method will solve all task-coordination problems easily and efficiently, a small set of basic methods can suffice.

have evolved happen to have another significant difference: Start task is directed, mailboxes are not. In choosing between these two methods, this difference can be decisive, especially if there are many transactions to perform by any of several equivalent tasks. If mailboxes are chosen, the parameters of the transaction can be queued as a message. When one of the equivalent consumer tasks becomes available, it seeks the next message from the mailbox. Thus, with the work queue maintained via a nondirected mailbox, there can never be both an available transaction and an available consumer task. In contrast, when the transaction parameters are sent to a specific consumer via a start-task runtime argument, you have no simple way to distribute the work equitably. You could have some consumers idle (Dormant) while others have a long queue of restart requests. To help balance the scales, start task has the advantage of bidirectional transfer of information, whereas the mailbox has only a unidirectional transfer.

In some cases, you have to decide whether it is more important to have automatic load leveling (which favors mailbox coordination) or more important to be able to coordinate with the completion of the transaction (which favors start-task). When both features are required, it is necessary to combine two different methods of coordination. For example, a mailbox can be used to receive the transaction parameters. Included with the parameters is the identity of the task that produced the transaction. After depositing the parameters at the mailbox, the producer issues a wait for one of its local event flags. A consumer task receives the parameters, completes the transaction, and then sets the local event flag to continue the producer. Thus, you have achieved nondirected, double-sided coordination with two coordination points, but at the expense of extra service calls.

The concept of coordination, as expounded here, requires that each partner task issue a service call to indicate its desire to participate in the coordination. Consider a task that receives coordination information. It performs a willful act (the invocation of a service call) to activate the transfer of information. Since the receiving task selects the point within its code at which the information is to be received, this type of transfer is synchronous. Information transfer during coordination must be synchronous.

Of course, it is possible to send information to a task even when that task is not calling for it. Signals provide that type of asynchronous transfer whenever the re-

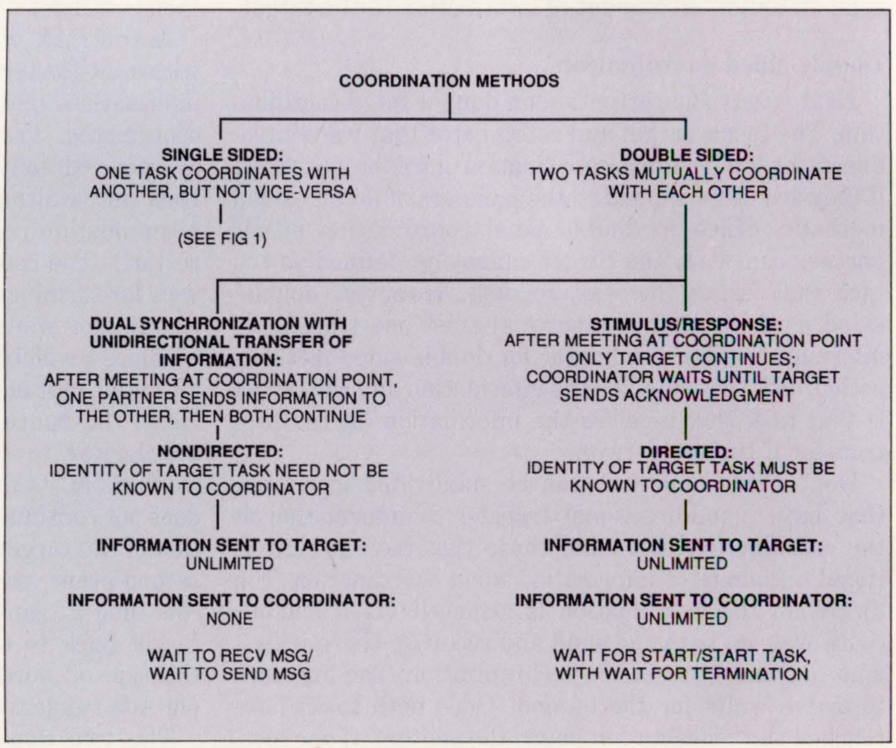

Fig3—Double-sided task coordination can involve either a unidirectional or a bidirectional transfer of information.

ceiving task has not issued a wait-for-signal. In this case, the sending task is imposing information on the receiver, not coordinating with it.

Equivalence of coordination methods

Are the methods diagrammed in **Fig 1** a fundamental set of coordination primitives, or can the coordination they provide be achieved by an even smaller set? You should consider three issues: (1) the extent to which the attributes of one class of methods can be simulated by restricting or limiting the use of another class, (2) the degree to which the unblocking function used in one method can be simulated using different methods, and (3) the efficiency, clarity, and vulnerability of such simulations.

Altering attributes by restricted use

As you have already seen, nondirected coordination can always be reduced to a corresponding directed method by permitting only one task to be the target. Thus, if only one task ever waits at a given message exchange, any task sending a message to that exchange is, in effect, sending it to that specific task. However, this restriction is imposed by the application designer; it is not enforced by the OS.

Similarly, the mutual exclusion that results from internal latching can be achieved with message exchange, by providing external latching. Suppose a given exchange is primed initially with a single message. That message may be taken from the exchange and put back, but no other message is allowed to be posted. In this case, the message becomes the latch; the exchange functions as a (binary) semaphore.

Generally, singly enabling coordination becomes multiply enabling when each task immediately releases the facility to any other task that may be waiting. For example, suppose you need a big event-flag group, say one that is 128 flags long. You could use controlled shared variables to create the group and submit the address of correspondingly big AND and OR unblocking functions in the *waicsv* requests. Then, all you have to do is always follow the *waicsv* calls by *rlscsv* to make the big event-flag group multiply enabling.

Thus, you see that the inherent attributes of certain coordination methods can be simulated by imposing task-level restrictions on the use of more general (and hence slower) methods. It remains to be seen whether the unblocking functions themselves can be simulated.

Synthesizing unblocking functions with CSVs

With a sufficiently general primitive, such as controlled shared variables, it is easy to synthesize the deblocking function of a wide range of other coordination methods. Making a priority-enqueued message exchange illustrates this point.

First, define a message structure, *msg*, that has a header (used to queue and control the message) and some text (shown as a nominal single character).

```
struct msg
   {
     /*common header*/
       struct msg   *nxt;     /*pointer to next message, if any*/
       short int    pty;      /*message priority*/
       short int    len;      /*text length, if needed*/
     /*content*/
       char         text;
   };

#define msgptr struct msg* /*pointer to this type of message*/
```

If all messages are of known fixed length, *len* could be omitted; if the queue is first in, first out, *pty* could be omitted.

At the task level, the message exchange would be a group of controlled shared variables that contain a pointer to the first message and a pointer to the last message in the queue. Both are 0 when the exchange is empty.

```
struct mx
   {
     msgptr first;          /*pointer to first message*/
     msgptr last;           /*pointer to last message*/
   };

#define mxlen     sizeof(struct mx)     /*size of exchange*/
#define mxid      struct mx*            /*identifier of exchange*/
```

Synthesize four basic functions:

```
mxid   create_x ();      /*create (empty) message exchange*/
int    send_x ();        /*send to message exchange*/
int    receive_x ();     /*receive from msg exchange*/
int    delete_x ();      /*delete message exchange*/
```

Create entails just a direct call of *crcsv*.

```
mxid create_x (key)          /*create (empty) message exchange*/
  long int key;              /*key of message exchange*/
    {
    return ((mxid) crcsv (key, (long) mxlen));
    }
```

For example,

```
#define MEX1 0x4D455831

mxid mex1;                     /*id of message exchange*/

mex1 = create_x (MEX1);        /*create message exchange*/
```

The delete follows a similar pattern.

The procedure to add a new message first waits for exclusive access to the exchange variables, inserts the new message, and then releases access. For efficiency, two special cases are recognized. The first is an empty exchange. In this trivial case, both exchange pointers

An application designer can usually choose a task-coordination scheme that is exactly right at each point for which coordination is needed.

are set to the new message. In the second special case—an incoming message with 0 priority—the message is immediately placed at the end of the queue. In the general case, the program must traverse the message queue.

```
send_x (xid, smsg)                    /*send to message exchange*/
  mxid  xid;                          /*id of message exchange*/
  msgptr smsg;                        /*ptr to message*/
   {
    int        result;                /*result of OS service call*/
    msgptr     prev;                  /*ptr to previous messages*/
    msgptr     next;                  /*ptr to next messages*/
    short int  npty;                  /*priority of new message*/

  /*wait for exclusive access*/

    if ((result = usecsv (xid, WAIFIN)) != NOERR)
      return (result);                /*failure*/

  /*add new message to priority chain*/

    if (xid->first == 0)
      { /*exchange is empty*/
        xid->first = xid->last = smsg; /*new msg is only msg*/
        smsg->next = 0;               /*new msg is end of chain*/
      }

    if (smsg->pty == 0)
      { /*0 priority: place new msg directly at end*/
        next = xid->last;             /*get current last*/
        next->nxt = smsg;             /*chain new msg to last*/
        xid->last = smsg;             /*new msg is last msg*/
        smsg->next = 0;               /*new msg is end of chain*/
      }
    else
      { /*find proper place based on priority*/
        npty = smsg->pty;             /*get priority of new message*/
        prev = xid->first;            /*get current first on chain*/
        if (npty > prev->pty)
          { /*new message is to be first*/
            xid->first = smsg;        /*new msg becomes first msg*/
            smsg->next = prev;        /*connect msg to chain*/
          }
        else
          {
            while (((next = prev->nxt) != 0) && (next->pty > = npty))
              prev = next;            /*continue down chain*/
            prev->nxt = smsg;         /*connect msg to chain*/
            if ((smsg->nxt = next) == 0)
              xid->last = smsg;       /*new msg is new last msg*/
          }
      }

 /*release access*/
   return (rlscsv (xid));
  }
```

Typical use would be

```
  struct msg msg1;                    /*test message*/
    ...

    send_x (mex1, &msg1);             /*send messages to exchange*/
```

The receive procedure waits for the exchange to be nonempty and then dequeues the first message.

```
int not_emp ();     /*unblocking function*/

int receive_x (xid, dmsg, dur)        /*receive from msg exchange*/
  mxid  xid;                          /*id of message exchange*/
  msgptr *dmsg;                       /*ptr to message buffer*/
  long int dur;                       /*max wait time*/
   {
    int  result;                      /*result of OS service call*/
    msgptr prev;                      /*ptr to previous messages*/
    msgptr next;                      /*ptr to next messages*/

  /*wait until there is a message*/

    if ((result = waicsv (xid, not_emp, dur)) != NOERR)
      return (result);                /*time or failure*/

    *dmsg = xid->first;               /*deliver current first on chain*/
    if ((xid->first = (*dmsg)->nxt) == 0)

        xid->last = 0;                /*exchange now empty*/

  /*release access*/
    return (rlscsv (xid));
   }

int not_emp (xid)
  mxid  xid;    /*id of message exchange*/
   {
    if (xid->first == 0)
      return (1);                     /*not empty: unblock*/
    else
      return (0);                     /*empty: keep waiting*/
   }
```

A sample receive call is

```
  msgptr buf;   /*buffer for addr of test messages*/
    ...

  result = receive_x (mex1, &buf, 1+SEC); /*receive msgs from exchange*/
  printf ("Receive: result = %x, text = %c\n", result, buf->text);
```

By similar techniques the task-level programmer can fabricate a message exchange with whatever priority or nonpriority queuing algorithm is desired. The problem is efficiency. Every task waiting for a message has the same *not_emp* calculation performed every time the exchange is released. Say there are four tasks waiting for a message at an empty exchange. A message is added. As a result, the same *not_emp* calculation is performed four times: once (successfully) upon release after the message is added, and then three times (unsuccessfully) after the first task takes the message and releases the exchange.

However, you know by the inherent nature of an exchange queue that *not_emp* must succeed for the first task and must fail for all remaining ones. Thus, you could build this knowledge into the specific send and receive request functions of an OS-level exchange and completely avoid the overhead of *not_emp*. But, for a task-level exchange, you cannot do this. The generality of the CSV primitive requires that you compute

> You can have a simple OS with just a few coordination primitives, but the application suffers as a result.

the unblocking function each time, since in principle, the result could be to block or unblock.

In addition, every message transfer with a task-level exchange requires four OS services: two to get the controlled shared variables and two to release them. An equivalent OS-level exchange uses only half that many calls and thus has only half that many context switches. As always, the penalty for generality is loss of efficiency. In real-time applications, the loss of efficiency is often disastrous to overall system performance.

Synthesizing unblocking functions with mailboxes

Only the MTOS-UX operating system provides controlled shared variables. With most other real-time operating systems, the mailbox is the only general primitive with which all coordination is to be done. Can various unblocking functions be formed from just mailboxes?

A technique for simulating semaphores with mailboxes has already been described. Beyond that, the road becomes long and treacherous. To take one example, simulate the AND unblocking function of an event-flag group using only mailboxes. To make it even simpler, forgo the maximum wait limit; waits can be forever.

Define a public variable to house the value of the group

```
extern short int   values;          /*value of simulated EFG*/
```

and control access to that variable through a mailbox (MB1) that acts as a semaphore. MB1 is primed with a dummy initial message. A trivial implementation of *waiefg* would then be

```
short int curval;                        /*local copy of EFG*/
short int mask;                          /*AND mask for EFG*/
long int access;                         /*zero-length message for access to EFG*/
long int stabuf;                         /*status of service call*/

access = 0;                              /*make length of access message 0*/

do
  {
    rcvmbx (MB1,&access,&stabuf,WAIFIN);        /*gain access to EFG*/
    curval = values;                            /*capture value*/
    sndmbx (MB1,&access,0L,&stabuf,CTUNOC); /*release access*/
  }
while ((curval & mask) != mask);
```

This method fails as soon as no task can use the group. At that point, the access message remains in the mailbox causing the **do** loop to be repeated constantly.

To avoid such repetition, after one unsuccessful test do not repeat the loop until some task has used and released the group. For this, you need a second mailbox. MB2 receives a dummy "group was released" message and is initially empty. The simulated *waiefg* now becomes

```
rcvmbx (MB1,&access,&stabuf,WAIFIN);            /*gain access to EFG*/
curval = values;                                /*capture value*/
sndmbx (MB1,&access,0L,&stabuf,CTUNOC);         /*release access*/

if ((curval & mask) != mask)
  { /*condition not immediately satisfied: wait for change*/
    do
      {
        rcvmbx (MB2,&access,&stabuf,WAIFIN);        /*wait for change*/
        sndmbx (MB2,&access,0L,&stabuf,CTUNOC); /*release change msg*/

        rcvmbx (MB1,&access,&stabuf,WAIFIN);        /*gain access to EFG*/
        curval = values;                            /*capture value*/
        sndmbx (MB1,&access,0L,&stabuf,CTUNOC); /*release access*/
      }
    while ((curval & mask) != mask);
  }
```

The function to set some of the bits (corresponding to *srsefg*) is

```
rcvmbx (MB1,&access,&stabuf,WAIFIN);            /*gain access to EFG*/
values &= onbits;                               /*set some bits*/
sndmbx (MB1,&access,0L,&stabuf,CTUNOC);         /*release access*/

sndmbx (MB2,&access,0L,&stabuf,CTUNOC);         /*indicate change*/
rcvmbx (MB2,&access,&stabuf,WAIFIN);            /*cancel change*/
```

While this is a proper simulation of an event flag, it is terribly slow. The work performed by a single *srsefg* requires four separate calls in the mailbox simulation. Since most of the processing time of any service call is in the context switch and similar fixed overhead, the time required to do *sndmbx* or *rcvmbx* is about equal to that required for *srsefg*. Thus, the simulation of *srsefg* runs about four times slower. The simulation of *waiefg* is even worse. When *waiefg* is fabricated at the task level, it takes four mailbox calls per waiting task to do the unblocking calculations. This costs four context switches per task. When the same unblocking calculations are performed within the OS as part of *srsefg*, there are no additional context switches, no matter how many tasks are waiting for the event flags.

A mailbox simulation of an event flag is also subject to a serious side effect. After a task (**C**) changes the flag values, all waiting tasks must be continued via **MB2** so that they can perform their coordination condition tests. While these tests are going on, **C** is blocked waiting for the access message to be passed from task to task. It is not until the last task has seen the change

A classification guide for selecting task-control processes takes the form of a decision tree: If you need this characteristic, choose this branch.

and returned the message to **MB2** that **C** can continue. But if even one of the tasks that must see the change message is relatively low in priority, it can take indefinitely long for that message to work its way back to **C**. Thus, with a simulated event-flag group, a high-priority task can become blocked for reasons unrelated to it and beyond its control. However, when the OS does the unblocking, the calculations are performed directly and immediately so that there cannot be any uncontrolled delays.

High overhead and undesirable side effects are typical whenever one attempts to simulate a specific coordination method at the task level using general coordination primitives. To answer the question posed earlier, yes, you can have a simple OS with just a few coordination primitives, but the application suffers as a result.

To sum up, coordination is the blocking of one or more tasks until some specified condition is met. Over the years, various methods of coordination have evolved to solve the specific kinds of problems that arise in real-time applications. These methods are fundamentally different in their attributes and effects. For example, some methods require that the identity of the coordination partner be specifically known, while others work with total anonymity. Another basic difference is in the amount of auxiliary information transmitted during the act of coordination or associated with the coordination scheme.

This final part of the real-time programming series has analyzed and classified the major coordination schemes to help guide your selection of the most appropriate technique, based on desired coordination properties and communication requirements. The classification rests upon the following dichotomies:

- single sided vs double sided—Double-sided schemes are symmetrical; whichever task gets to the coordination point first waits for the other. Thus, two tasks are mutually coordinating with each other. In contrast, single-sided schemes are asymmetrical. One task coordinates with another, but not vice versa. The roles of the coordinator and target tasks are always distinct.
- directed vs nondirected—In directed methods the identity of the target task must be specifically known to the coordinator. In nondirected methods, the identity of the target is hidden.
- singly enabling vs multiply enabling—Singly enabling procedures permit only one task at a time to proceed when more than one is waiting for coordination. Multiply enabling procedures release all tasks that satisfy the coordination condition.
- transient vs stored—With a stored mechanism, the OS retains the coordination information until it is needed. With a transient mechanism, if the target is not waiting for coordination, the continue-task information is lost.
- unidirectional vs bidirectional—When coordination is accompanied by an exchange of information, the flow of that information can be in one or two directions.

In some cases, the properties of one coordination method can be constructed from another (often more general) scheme. For example, a nondirected mecha-

Companion disk offer

All of the C examples in this series, plus applications of your own, can be run on a PC with a set of demonstration disks available from Industrial Programming Inc. The disks contain a full version of MTOS-UX for an IBM PC/AT or compatible. An application program is edited, compiled, linked, and loaded under MS-DOS. The MTOS-UX then takes over the hardware to execute the program in real time. At any time, you can enter an ctl/dlt command from the console to return control to MS-DOS.

The demonstrator requires an AT with a least 512k bytes of RAM and a hard disk with 2M bytes available for MTOS libraries and scratch storage. Program preparation requires the Microsoft C compiler/linker, version 5.0 or later. Microsoft tools are not included with the MTOS-UX demonstrator.

The demonstration version has all of the features and facilities of standard MTOS-UX. Hownever, there is a limit of six of each type (six tasks, six mailboxes, six semaphores, and so forth). The disk set costs $25; unlimited versions are also available. For more details, call IPI at (800) 365-6867 or (516) 938-6600, or write to 100 Jericho Quadrangle, Jericho, NY 11753.

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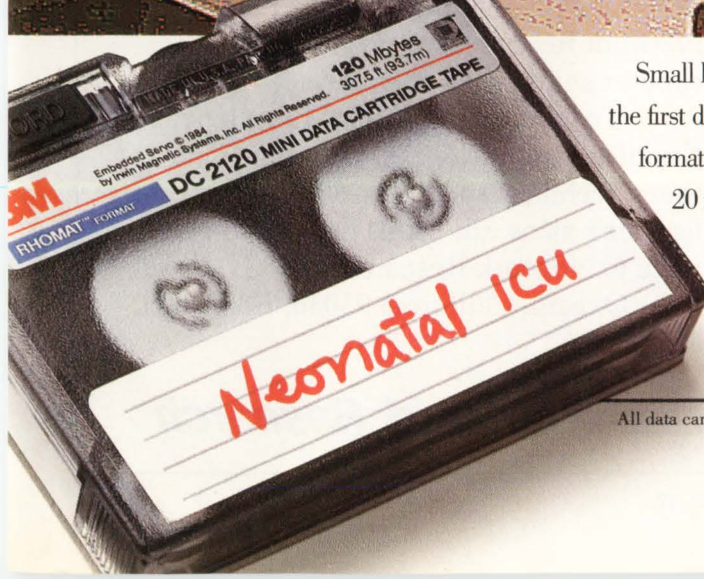

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nism reduces to a directed one if (by the design of the application) only one task is ever allowed to be the waiting target. Furthermore, controlled shared variables are sufficiently general to enable the task-level programmer to build almost all the other coordination mechanisms. Nevertheless, such task-level constructions are very inefficient compared with OS-level services. EDN

Reference

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		0.022 – 0.47	11.0V
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Spice simulations use controlled sources to model NTSC signals

You can use Spice-variety circuit-simulation software to model NTSC video signals. You can then use these models to design and test video circuits.

Anthony M Radice, *General Instrument Corp*

As simulation tools become less expensive and more readily available to design engineers, simulating a design accurately before production release becomes more practical. Because the computer can do a spread of analyses while you work on something else (or even go home for the evening), being able to accurately describe a variety of conditions and operational models for a circuit is to your benefit. You could improve the accuracy of video-circuit models if you could simulate a video input signal. This article details how to use Spice to build models of NTSC video signals from a set of controlled sources.

The methods presented here were tested with MicroSim Corp's (Laguna Hills, CA) PSpice circuit-simulation software. With minor modification, the technique should work with any software that simulates independent and controlled voltage and current sources. The general procedure is to build several common video signals in a piece-wise, linear fashion. These signals are the modulated-ramp, multiburst, and composite test signals, and are typically used on the bench to do circuit testing. Thus, simulation results and actual tested results should match well. For background information on PSpice, see **Refs 1** and **2**; for methods of testing video signals, see **Ref 3**; and for details on video-signal composition, see **Ref 4**.

To build simulated video signals, start by establishing some ground rules and setting up a template for a variety of signals. These chores are not difficult because video is very repetitive. You can make the following assumptions:

- Vertical sync will not be a factor at this time in this discussion.
- The horizontal interval is 63.56 μsec. All timing signals are rounded to the nearest 0.01 μsec, and all add up to the 63.56-μsec period. The total cumulative rounding error, about 4 nsec, works out to an error of about 5.7°/line.
- All references to time are relative to the beginning of the "front porch" of the video signal. The front-porch interval is the first of the six video signal intervals and is 1.4 μsec long.
- In the signal descriptions, volts will represent IRE levels, so the simulated output voltage will be 1.4V p-p. If 1V p-p is required, use a final scaling multiplier of 0.7143. An IRE (Institute of Radio Engineers) unit is a measurement unit used for video signals. It represents 1% of the voltage difference between blanking (where the visible spot is gone, or "blanked," and defined as 0 IRE) and peak = white level (defined as 100 IRE). The horizontal pulse of NTSC video signals, as well as other timing pulses, extend to a point 40 IRE below blanking, making the video signal 140 IRE p-p.

To build simulated video signals, start by establishing some ground rules and setting up a template for a variety of signals.

Table 1—Parameters for PSpice PULSE command

Symbol	Parameter	Default	Typical value
<v1>	Initial voltage	None	0V
<v2>	Pulsed (t0) voltage	None	1V
<td>	Initial delay	0	*
<tr>	Rise time	TSTEP	0.2 μsec
<tf>	Fall time	TSTEP	0.2 μsec
<pw>	Pulse width	TSTEP	*
<pr>	Cycle period	TSTEP	63.56 μsec

*Varies with selected waveform.

These simulations describe only the time response (.TRAN) of the circuit. You should undertake other analyses, such as .AC, .DC, and .NOISE, separately.

Before starting the waveform simulations, review the PULSE independent-voltage-source PSpice command. This command, whose parameters are given in **Table 1**, has the form:

```
V<name> <(+)node> <(-)node> PULSE(<v1>
+ <v2> <td> <tr> <tf> <pw> <pr>)
```

Each parameter is a separate entity. For example, the rise and fall times are not part of the pulse width. Thus, you can have a very long rise or fall time and a very short pulse width. The PULSE command builds up the gating signals necessary to turn various parts of the video signal on and off. **Ref 1** gives detailed information about this command. **Table 1** uses typical values to build a template for this command; you can change these values to suit a particular application.

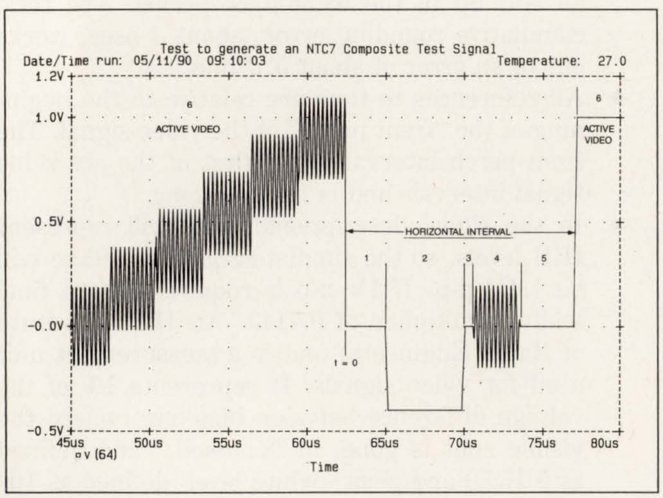

Fig 1—A video line has six distinct periods. *The bulk of the line consists of active video information; the rest contains the front porch, the horizontal-sync pulse, the breezeway, the color burst, and the back porch.*

First, build up the horizontal interval and then use it as a template to build the test signals. Each video line comprises six distinct periods **(Fig 1)** totaling 63.56 μsec. The horizontal interval consists of periods 1 through 5 in **Table 2** and **Fig 1**. Active video occurs during period 6.

Using the information in **Table 2**, you can specify the horizontal interval as the sum of an independent pulsed voltage source and a controlled voltage source. The controlled source is a sine-wave generator for color burst. This generator is gated, or multiplied, by a pulse that enables it at the correct interval. **Fig 2** shows the progression of this process. **Fig 2a** is the HSync pulse. **Fig 2b** is the gating pulse for the color-burst signal, followed by the 3.58-MHz sine-wave generator **(Fig 2c)**. **Fig 2d** is **Fig 2a** plus the product of **Fig 2b** and **Fig 2c**.

The first Spice statement builds the negative-going horizontal = sync pulse. (Nodes are represented as <nnn>.)

```
V_HSync <+1> <-1> PULSE(0 -0.4 1.4u 0.2u
+ 0.2u 4.7u 63.56u)
```

The output of this pulse is zero for the front-porch interval (1.4 μsec). The pulse has 0.2-μsec rise and fall times, a full amplitude of −0.4V (−40 IRE), and a width of 4.7 μsec. The period of this pulse is 63.56 μsec.

To build the color-burst signal, start with a sine-wave generator that has a peak value of 0.2V and, thus, a peak-to-peak amplitude of 40 IRE:

```
V_CB <+2> <-2> SIN(0 0.2 3579545 0 0 0)
```

The generator's signal has a 0V offset, a 0.2V peak amplitude signal at 3.579545 MHz, and no delay, damp-

Table 2—Video-signal intervals

Interval	Length (μsec)	Transition time (μsec)
Front porch	1.4	0.2
Horizontal-sync pulse	4.7	0.2
Breezeway	0.5	0.2 (envelope)
Color burst	2.6	0.2 (envelope)
Back porch	1.4	0.2
Video information	51.76	0.2

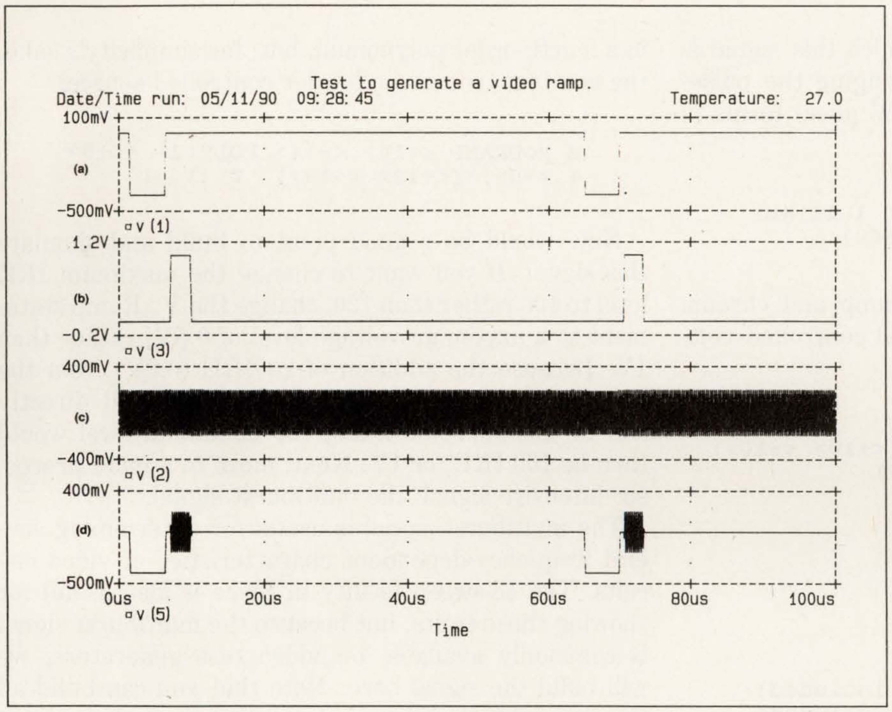

Fig 2—Summing and gating various sources simulates the horizontal interval. *The horizontal-sync pulse* ***(a)****, summed with the product of the color-burst gating pulse* ***(b)*** *and the 3.58-MHz sine wave* ***(c)****, produces the composite horizontal-interval signal in* ***d****.*

ing, or phase offset. The following pulse will gate this generator:

```
V_CB_Gate <+3> <-3> PULSE(0 1.0 7.0u
+ 0.2u 0.2u 2.6u 63.56u)
```

This pulse has a delay of 7 μsec after the start of the front-porch interval, a 2.6-μsec burst width, a ±20-IRE amplitude centered on 0 IRE, and a period of 63.56 μsec. Now, multiply V_CB and V_CB_Gate, which produces a gated, controlled voltage source, E_CB:

```
E_CB <+4> <-4>  POLY(2)  (<+2> <-2>)
+ (<+3> <-3>)  0  0  0  0  1
```

Note that the terms following a second-order polynomial in Spice are the following "p" coefficients: p0 is the offset, p1 is the V1 term, p2 is the V2 term, p3 is the $V1^2$ term, and p4 is the $V1 \times V2$ term. Because V2 (V_CB_Gate) is zero over all but the color-burst interval, this term effectively gates the color burst. This gating is the key aspect of all the signals you will build. Finally, add the terms E_CB and V_HSync to obtain another controlled source, E_HI:

```
E_HI <+5> <-5> POLY(2) (<+1> <-1>) (<+4>
+ <-4>)  0  1  1
```

This expression shows that the summation of nodes ±1 through ±4 generates the horizontal interval. At this point, writing the previous terms into a simulation file and running it would be useful. Once successful, you're ready to move to the next step. Use this horizontal-interval template to build the first of the full video signals: the modulated ramp.

The characteristic of the modulated ramp is a 40-IRE p-p chroma signal superimposed on a 0- to 100-IRE luminance ramp (**Fig 3**). This signal is useful for determining differential phase (change of phase relative to burst as a function of signal amplitude) and differential gain (change of gain as a function of signal amplitude). You can adjust the level of the envelope of the chroma so that it does or does not exceed the 0-IRE level, the 100-IRE level, or both. Start with a signal that has a minimum envelope value of −20 IRE and a maximum envelope value of 120 IRE. Start with a specific chroma generator and its "switch":

```
V_CHROMA <+10> <-10> SIN(0 0.2 3579545
+ 0 0 76)
V_CHR_SW <+11> <-11> PULSE(0 1 11.4u
+ 0.2u 0.2u 51.76u 63.56u)
```

These terms generate a chroma signal 76° ahead of the V_CB generator, which has a phase of 0°. The signal is 40 IRE p-p and centered on the 0-IRE refer-

First, build the horizontal interval and then use it as a template to build the test signals.

ence. Now, generate the ramp to which this signal is added. Generate the ramp by rearranging the pulse-width (0.2 μsec) and rise-time (51.756 μsec) terms in the pulse specification:

```
V_RAMP <+12> <-12> PULSE(0 1 11.4u
+ 51.76u  0.2u  0.2u  63.56u)
```

You can now sum together the ramp and chroma signals using a third-order-polynomial controlled voltage source:

```
E_VID1 <+13> <-13> POLY(3) (<+10> <-10>)
+ (<+11> <-11>) (<+12> <-12>)
+ 0 0 0 1 0 1

p0 - Offset
p1 - V_CHROMA
p2 - V_CHR_SW
p3 - V_RAMP
p4 - V_CHROMA^2
p5 - V_CHROMA * V_CHR_SW
p6 - V_CHROMA * V_RAMP (not included)
p7 - V_CHR_SW^2        (not included)
p8 - V_CHR_SW * V_RAMP (not included)
```

As the terms of the polynomial increase, the coefficients can rapidly become difficult to visualize. Writing down the terms can help. The final step in building a modulated ramp is to sum this video signal with the horizontal interval. You could perform this summation in a fourth-order polynomial, but, for simplicity's sake, the last term is a second-order controlled source:

```
E_MODRAMP <+14> <-14> POLY(2) (<+5>
+ <-5>) (<+13> <-13>)  0  1  1
```

Now would be a good point to build and simulate this signal. If you want to change the maximum IRE level to 100 rather than 120, change the V_Ramp statement to a maximum voltage level of 0.8V, rather than 1V. Because the addition of 20 IRE (0.2V) from the maximum level of the chroma source would directly add to this 0.8V (80 IRE), the maximum level would then be 100 IRE, or 1V. Next, move to a more processor-intensive signal: the multiburst signal.

The multiburst signal is useful for determining several frequency-dependent characteristics of video circuits. The ac-sweep facility in Spice is also useful for showing these traits, but because the multiburst signal is commonly available on video test generators, we will build the signal here. Note that you can build all these simulated signals into subcircuits and then use the subcircuits in a library of analysis tools.

In the video portion, a multiburst signal consists of a white bar (100 IRE) and several bursts of frequencies: 500 kHz and 1, 2, 3, 3.579545, and 4.2 MHz. These frequencies are centered on 50 IRE and are 50 IRE p-p in amplitude (**Fig 4**). Sometimes these bursts are part of another test signal, such as the NTSC combina-

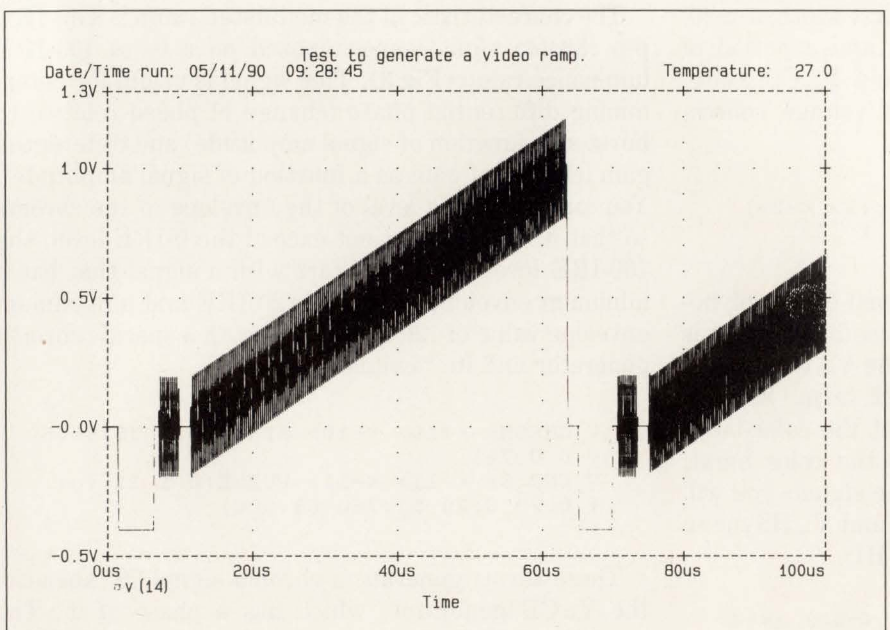

Fig 3—The modulated ramp is useful for determining differential phase and gain. *The signal is a 40-IRE p-p chroma signal superimposed on a 0- to 100-IRE luminance ramp. By manipulating the coefficients in the Spice listings, you can change chroma offset, ramp levels, and other parameters.*

tion test signal (**Ref 4**). But for this application, the bursts will take up the entire horizontal line.

Build the white bar by generating a pulse of 100 IRE, then dropping it to 50 IRE (by adding a −50-IRE term) to form the center of the bursts. Considering just this portion of the signal, you can generate

```
V_WB  <+20> <-20> PULSE(0  1   11.4u
+ 0.2u 0.2u 51.76u 63.56u)
V_DRP <+21> <-21> PULSE(0 -0.5 15.4u
+ 0.2u 0.2u 47.76u 63.56u)
E_LUM <+22> <-22> POLY(2)  (<+20> <-20>)
+ (<+21> <-21>) 0  1  1
```

V_WB strongly resembles V_CHR_SW in the simulation of the modulated ramp. This term is useful for gating the entire video portion of the line. Now, generate the six frequency terms of the signal. They are all similar.

```
* 500-kHz Signal, 6-usec width, envelope
* +0.2 usec each end.
V_FR1        <+23> <-23>   SIN(0 0.25
+ 500000 0 0 0)
V_FR1_SW   <+24> <-24> PULSE(0 1 18.0u
+ 0.2u 0.2u 6.0u 63.56u)

* 1-MHz Signal
V_FR2        <+25> <-25>   SIN(0 0.25 1MEG
+ 0 0 0)
V_FR2_SW   <+26> <-26> PULSE(0 1 25.0u
+ 0.2u 0.2u 6.0u 63.56u)

* 2-MHz Signal
V_FR3        <+27> <-27>   SIN(0 0.25 2MEG
+ 0 0 0)
V_FR3_SW   <+28> <-28> PULSE(0 1 32.0u
+ 0.2u 0.2u 6.0u 63.56u)

* 3-MHz Signal
V_FR4        <+29> <-29>   SIN(0 0.25 3MEG
+ 0 0 0)
V_FR4_SW   <+30> <-30> PULSE(0 1 39.0u
+ 0.2u 0.2u 6.0u 63.56u)

* The "Magic Number", 3579545 Hz, zero
* reference phase.
V_FR5        <+31> <-31>   SIN(0 0.25
+ 3579545 0 0 0)
V_FR5_SW   <+32> <-32> PULSE(0 1 46.0u
+ 0.2u 0.2u 6.0u 63.56u)

* 4.2-MHz Signal
V_FR6        <+33> <-33>   SIN(0 0.25
+ 4.2MEG 0 0 0)
V_FR6_SW   <+34> <-34> PULSE(0 1 53.0u
+ 0.2u 0.2u 6.0u 63.56u)
```

You must gate each of the above frequency components, in its respective set, by the appropriate pulse. These terms are as follows:

```
E_F1 <+35> <-35> POLY(2) (<+23> <-23>)
+ (<+24> <-24>) 0 0 0 0 1
E_F2 <+36> <-36> POLY(2) (<+25> <-25>)
+ (<+26> <-26>) 0 0 0 0 1
E_F3 <+37> <-37> POLY(2) (<+27> <-27>)
+ (<+28> <-28>) 0 0 0 0 1
E_F4 <+38> <-38> POLY(2) (<+29> <-29>)
+ (<+30> <-30>) 0 0 0 0 1
E_F5 <+39> <-39> POLY(2) (<+31> <-31>)
+ (<+32> <-32>) 0 0 0 0 1
E_F6 <+40> <-40> POLY(2) (<+33> <-33>)
+ (<+34> <-34>) 0 0 0 0 1
```

Finally, sum the individual terms. Use an eighth-order polynomial because you are strictly taking a SUM. Not dropping any nodes is crucial, as Spice would deliver bizarre results.

```
E_MBRST <+41> <-41>  POLY(8)
+ (<+ 5> <- 5>) (<+22> <-22>) (<+35>
+ <-35>)  (<+36> <-36>) (<+37> <-37>)
+ (<+38> <-38>) (<+39> <-39>) (<+40>
+ <-40>)  0  1  1  1  1  1  1  1  1
```

As before, now is a good time to build this signal and simulate it. Variations on the signal include varying the phase of the individual components or the width of individual frequency components. Because of the rounding of the time periods, the phase of an individual

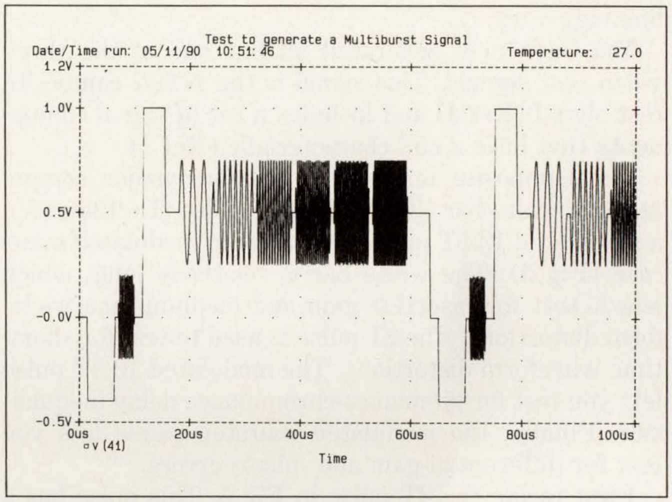

Fig 4—A multiburst signal contains bursts of six different frequencies. *The Spice simulation of this signal uses an eighth-order polynomial to sum the individual frequency terms. You can modify these expressions to reflect different phases and burst widths of the individual frequency components.*

You can specify the horizontal interval as the sum of an independent pulsed voltage source and a controlled voltage source.

burst relative to the color burst in a given horizontal line may vary.

You have now generated all but one of the three video test signals. This signal is the NTC7 composite test signal **(Ref 4)** and includes a set of signal components that have a $\sin^2$ characteristic **(Ref 2)**.

The composite test signal has four major components: a white bar (100 IRE), a 2T pulse (T = 125 nsec), a modulated 12.5T pulse, and a 6-step modulated staircase **(Fig 5)**. The white bar is relatively long, which lets it test for insertion gain and medium-time waveform distortions. The 2T pulse is used to test for short-time waveform distortions. The modulated 12.5T pulse lets you test for luminance-chrominance delay inequalities. Finally, the modulated-stairstep signal lets you test for differential-gain and -phase errors.

First tackle the 2T pulse in **Fig 5**. This pulse has a $\sin^2$ characteristic and a pulse width equal to two periods of the 3.58-MHz chroma subcarrier. Therefore, take the output of a generator with a frequency of $(3.58 \div 4)$ MHz **(Fig 6a)** and square it through a controlled-source polynomial. This squaring doubles the frequency to $(3.58 \div 2)$ MHz and puts the voltage characteristics at the correct levels, which are between 0 and 1V **(Fig 6b)**. Phase the generator properly to get the 0-IRE intercepts to match the gating generator and your desired location. First, generate the frequency and square the output.

```
V_2TGEN   <+50> <-50>    SIN(0 1 894886
+ 0 0 0)   ; To Be Modified **
E_2TGN    <+51> <-51>   POLY(1)  (<+50>
+ <-50>)   0 0 1
```

This pulse should be centered on 35.4 μsec. (All numbers for location and pulse widths are from the NTC7 television report in **Ref** 4.) The pulse, from zero crossing to zero crossing, is $1/(894{,}886 \times 2) = 0.559$-μsec wide. Because of the short length of this pulse, you must make an exception to the accuracy assumption. The gating pulse and its associated multiplication statement are, therefore,

```
V_2TGAT <+52> <-52> PULSE(0 1 35.1255u
+ 0.001u 0.001u 0.559u 63.56u)
E_2TGTE <+53> <-53>   POLY(2)  (<+51>
+ <-51>) (<+52> (-52>)   0 0 0 0 1
```

You calculate the delay of the gating pulse (35.1205 μsec) from the desired center location (35.4 μsec) minus half of the 2T pulse width (0.559 μsec). The 0.001-μsec

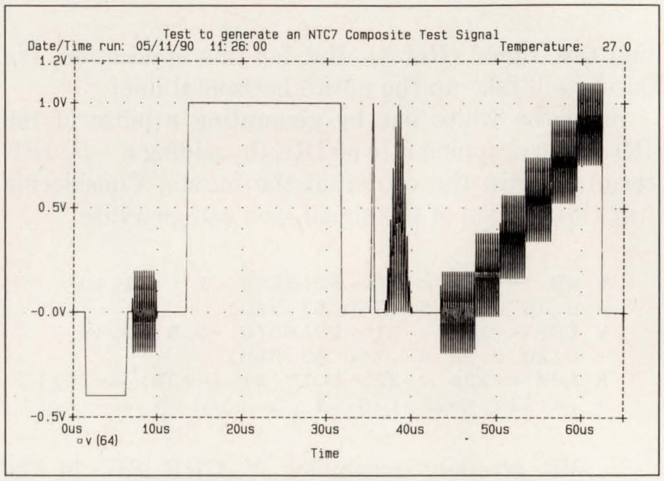

Fig 5—Multiple video-system testing opportunities are inherent *in the NTC7 composite test signal. The white bar is useful for testing insertion gain and medium-time waveform distortions; the 2T pulse lets you test short-time waveform distortions; the 12.5T pulse lets you test for luminance-chrominance delay disparities; and the modulated staircase provides a handy test for differential-phase and -gain errors.*

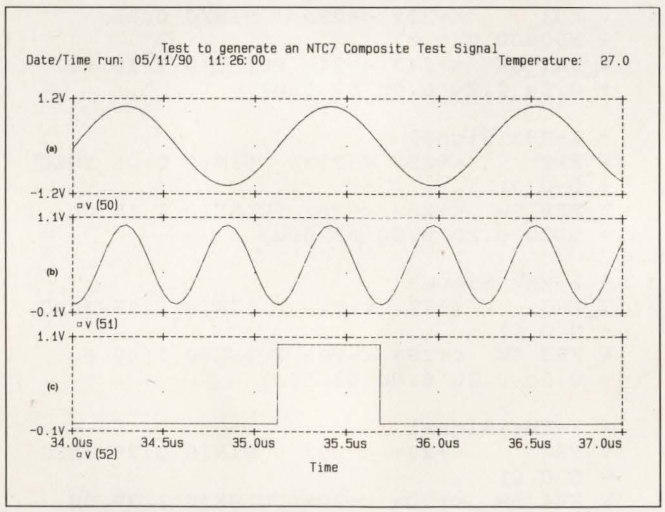

Fig 6—To generate the 2T and 12.5T signals, *square the output of an 895-kHz generator **(a)** to produce the 1.79-MHz waveform at the correct voltage levels in **b**. Several Spice manipulations are necessary to calculate correct delays and phasing to form the envelope of the output **(c)**.*

rise and fall times and the 0.559-μsec pulse width must total the zero intercepts of the 2T pulse because the rise and fall times and the pulse width are independent time periods. During the rise and fall times, the output product will not be zero because the gating signal has a value during the transitions. This transitional value helps form the envelope of the output **(Fig 6c)**.

Now, you can calculate the phase of the 2T generator

Table 3—Chroma staircase characteristics

Burst	Amplitude (p–p)	Centered	Time (μsec)	Start (μsec)
1	40 IRE*	0 IRE	4	43.4
2	40 IRE	18 IRE	3	47.4
3	40 IRE	36 IRE	3	50.4
4	40 IRE	54 IRE	3	53.4
5	40 IRE	72 IRE	3	56.4
6	40 IRE	90 IRE	3	59.4

*IRE stands for Institute of Radio Engineers. One IRE unit represents 1% of the voltage difference between blanking, which is 0 IRE, and peak white level, which is 100 IRE.

to "arrange" a zero crossing at exactly 35.1255 μsec into the simulation. While performing this calculation, keep in mind that the $\sin^2$ wave comes from a signal at half the frequency. You want to center either the 90° or the 270° peak at 35.4 μsec. Because one period of the V_2TGEN signal is 1.117 μsec, the timing works out to 31.678 cycles to get from start at 0° phase to 35.4 μsec into the signal. Subtracting the 31 cycles and converting to degrees (0.678×360°), you can see that the generator's phase would be 244° if it started at reference 0°. The generator's phase should be 270°, so start the generator at reference 26°. The V_2TGEN statement is thus

```
V_2TGEN  <+50> <-50>   SIN(0 1 894886
+ 0 0 203)
```

Put the 12.5T pulse aside for now and assemble the easy part of the line so you can experiment. The composite test signal has a white bar 18-μsec long that starts at 13.4 μsec and then drops to 0 IRE prior to the 2T pulse. After the 2T pulse, the signal drops to 0 IRE for the 12.5T pulse. The 12.5T pulse is centered at 38.4 μsec. After this pulse, the composite signal drops to 0 IRE until 43.4 μsec into the waveform. At this point comes the modulated-staircase signal, which you can regard as six bursts of chroma with the characteristics **Table 3** shows.

The phase of this staircase signal does not change relative to each step and to the color-burst signal. You can build the signal from a chroma source and a series of pulses for the "steps." First, build the white bar, which resembles V_WB of the multiburst signal, only shorter.

```
V_WB2 <+55> <-55>  PULSE(0 1 13.4u 0.2u
+ 0.2u 18.0u 63.56u)
```

Now, assemble the staircase for the chroma. Because the first chroma burst is centered on 0 IRE, the first step of the staircase is 0. Thus, skip the first step and proceed to the remaining five. Each step adds 0.18V (18 IRE) to the base level of the chroma. Note that the chroma switches on at 43.4 μsec and the first "riser" on the staircase switches on at 47.4 μsec.

```
V_SC1 <+56> <-56>  PULSE(0  0.18  47.4u
+ 0.01u  0.01u  15.0u  63.56u)
V_SC2 <+57> <-57>  PULSE(0  0.18  50.4u
+ 0.01u  0.01u  12.0u  63.56u)
V_SC3 <+58> <-58>  PULSE(0  0.18  53.4u
+ 0.01u  0.01u   9.0u  63.56u)
V_SC4 <+59> <-59>  PULSE(0  0.18  56.4u
+ 0.01u  0.01u   6.0u  63.56u)
V_SC5 <+60> <-60>  PULSE(0  0.18  59.4u
+ 0.01u  0.01u   3.0u  63.56u)
```

Because the phase should be 0° and V_CB is already the correct amplitude, you can take the chroma itself directly from V_CB. You now need to generate the correct gating pulse and gate the chroma.

```
V_CB_STC <+61> <-61>  PULSE(0  1  43.4u
+ 0.01u  0.01u  19.0u  63.56u) E_CBSTC
+ <+62> <-62>  POLY(2) (<+2> <-2>)
+ (<+61> <-61>) 0 0 0 0 1
```

You can now assemble the composite signal short of the 12.5T pulse. You can accomplish this task with one statement. Again, be very careful with node numbers.

```
E_COMP <+64> <-64>  POLY(9)
+ (<+ 5> <- 5>)  (<+55> <-55>)  (<+50>
+ <-50>) (<+62> <-62>)  (<+56> <-56>)
+ (<+57> <-57>) (<+58> <-58>)
+ (<+59> <-59>) (<+60> <-60>)
+ 0 1 1 1 1 1 1 1 1 1
```

The above statement is in the order horizontal interval, white bar, 2T pulse, space, and the chroma and staircase signal. Now would be a good time to assemble and simulate the above statements.

The last step in building the composite test signal is adding the 12.5T modulated pulse to the chroma signal. Build this pulse by generating an envelope of the 12.5T $\sin^2$ characteristic, the modulation pulse, and the gating pulse. Then, multiply them together. You build the 12.5T pulse in much the same way as the 2T pulse. First, generate a sine wave at 3.58÷25 MHz, then square it to get a frequency of 3.58÷12.5 MHz

Each video line comprises six distinct periods totaling 63.56 μsec. The horizontal interval consists of periods 1 through 5; active video occurs during period 6.

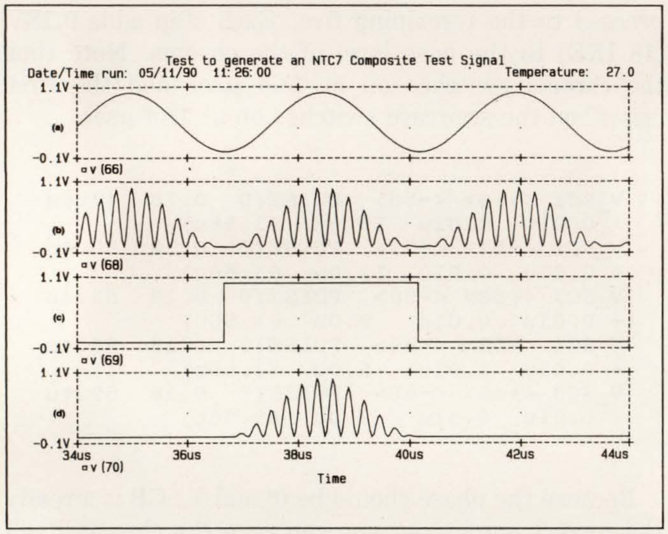

Fig 7—The last step in simulating an NTC7 composite test signal *is adding the 12.5T modulated pulse to the chroma signal. Squaring a 3.58-MHz ÷ 25 signal in* ***a*** *produces the 286.4-kHz waveform in* ***a****. Modulation produces the signal in* ***b****, and gating this signal with* ***c*** *yields the composite waveform* ***(d)****.*

(Fig 7a). The statements for these operations are

```
V_12TGEN   <+65> <-65>   SIN(0 1 143182
+ 0 0 0)   ; To Be Modified **
E_12TGN    <+66> <-66>  POLY(1) (<+65>
+ <-65>)    0 0 1
```

Now, generate the modulation as a 100-IRE p-p chroma signal centered on 50 IRE, and multiply the envelope by the modulating signal **(Fig 7b)**.

```
V_12TCHR <+67> <-67>  SIN(0.5 0.5
+ 3579545 0 0 0) E_12TEM  <+68> <-68>
+ POLY(2) (<+66> <-66>) (<+67> <-67>)
+ 0 0 0 0 1
```

The zero-crossing period of this signal is 3.492 μsec. This signal should be centered at 38.4 μsec. You can generate the gating pulse for the 12.5T signal **(Fig7c)**:

```
V_12TGAT  <+69> <-69>  PULSE(0 1 36.654u
+ 0.001u 0.001u 3.49u 63.56u)
```

Now, multiply the gating pulse by the product of the envelope and modulation **(Fig 7d)** and adjust the phase of the envelope to make the intercepts of the envelope symmetrical at the 0-IRE level. The gating product is

```
E_12TPRD  <+70> <-70>  POLY(2) (<+68>
+ <-68>) (<+69> <-69>) 0 0 0 0 1
```

The zero-crossing point must occur at 36.654 μsec, so the phase of V_12TGEN must be

$$\text{MOD}\left[\frac{36.654\times10^{-6}}{\left(\dfrac{1}{143{,}182}\right)}\right]\times360°=89°.$$

The modified simulation statement is

```
V_12TGEN  <+65> <-65>  SIN(0 1 143182
+ 0 0  89 )
```

Finally, change the summation statement to a tenth-order polynomial and add the E_12TPRD term:

```
E_COMP <+64> <-64>  POLY( 10 )
+ (<+ 5> <- 5>) (<+55> <-55>) (<+50>
+ <-50>) (<+70> <-70>)+ (<+62> <-62>
+ (<+56> <-56>)  (<+57> <-57>)  (<+58>
+ <-58>) (<+59> <-59>)  (<+60> <-60>)
+ 0 1 1 1 1 1 1 1 1 1  1
```

Note the three separate changes in this equation with respect to the earlier E_COMP equation, which had no 12.5T signal:

- Change the POLY term in the first line from a 9 to a 10
- Add nodes ±70 in the second line
- Add a tenth 1 in the last line.

Fig 8 gives the Spice listing for the simulation of the NTC7 composite test signal. Note that both the 2T and the 12.5T pulses rely on low-frequency generators as sources. The phase relationship of these generators, relative to the respective pulse location, changes from line to line. Thus, the first simulation of these pulses is correct in time, but the next line is not. You could build up a longer simulation file to correct this problem. This more extensive simulation file would set up the various phase relationships between burst and the respective pulses; a final gating pulse train would enable the correct lines as outputs at the appropriate times. Such a subcircuit would be from two to four times the size of this model.

Text continued on pg 128.

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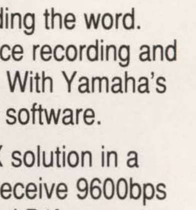

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CIRCLE NO. 76

```
Test to generate an NTC7 composite test signal
*
* Major point of this test signal is to develop the Sin² characteristics
*  of the 2T and 12.5T pulses.
*

* Horizontal Sync Tip
V_HSync     1  0  PULSE(0 -0.4 1.4u 0.2u 0.2u 4.7u 63.56u)  ; Make HSync

* Color Burst
V_CB        2  0    SIN(0 0.2 3579545 0 0 0)              ; Burst Amplitude 40
V_CB_Gate   3  0  PULSE(0 1 7.0u 0.2u 0.2u 2.6u 63.56u) ; When turn ON
E_CB        4  0    POLY(2) (2 0) (3 0) 0 0 0 0 1          ; X

* Horizontal Interval
E_HI        5  0    POLY(2) (1 0) (4 0) 0 1 1              ; Sum

* Active Video - White Bar
V_WB2      55  0  PULSE(0  1  13.4u 0.2u 0.2u 18.0u 63.56u)

* Active Video - 2T Pulse
V_2TGEN    50  0    SIN(0 1 894886 0 0 203)
E_2TGN     51  0    POLY(1) (50  0) 0 0 1
V_2TGAT    52  0  PULSE(0 1 35.1255u 0.001u 0.001u 0.557u 63.56u)
E_2TGTE    53  0    POLY(2) (51  0)  (52  0)  0 0 0 0 1

* Active Video - Staircase
V_SC1      56  0  PULSE(0  0.18  47.4u  0.01u  0.01u  15.0u  63.56u)
V_SC2      57  0  PULSE(0  0.18  50.4u  0.01u  0.01u  12.0u  63.56u)
V_SC3      58  0  PULSE(0  0.18  53.4u  0.01u  0.01u   9.0u  63.56u)
V_SC4      59  0  PULSE(0  0.18  56.4u  0.01u  0.01u   6.0u  63.56u)
V_SC5      60  0  PULSE(0  0.18  59.4u  0.01u  0.01u   3.0u  63.56u)

* Active Video - Chroma
V_CB_STC   61  0  PULSE(0  1  43.4u  0.01u  0.01u  19.0u  63.56u)
E_CBSTC    62  0    POLY(2) (2  0) (61  0) 0 0 0 0 1

E_COMP     64  0    POLY(9)
+    ( 5  0)  (55  0)  (53  0)
+    (62  0)  (56  0)  (57  0)  (58  0)
+    (59  0)  (60  0)
+ 0 1 1 1 1 1 1 1 1 1

R0     1  0 1MEG
R1     2  0 1MEG
R2     3  0 1MEG
R3     4  0 1MEG
R4     5  0 1MEG
R5    50  0 1MEG
R6    51  0 1MEG
R7    52  0 1MEG
R8    53  0 1MEG
R8A   55  0 1MEG
R9    56  0 1MEG
R10   57  0 1MEG
R11   58  0 1MEG
R12   59  0 1MEG
R13   60  0 1MEG
R14   61  0 1MEG
R15   62  0 1MEG
R16   64  0 1MEG

.OPTIONS ITL5=0 RELTOL=0.01 ACCT
.TRAN 35nS 100uS
.PROBE
.END
```

Fig 8—This routine lets you simulate the complex NTC7 composite test signal. *The main complication in generating this signal is the careful attention you must devote to timing considerations. Once simulated, this signal lets you test a multitude of performance parameters in video systems.*

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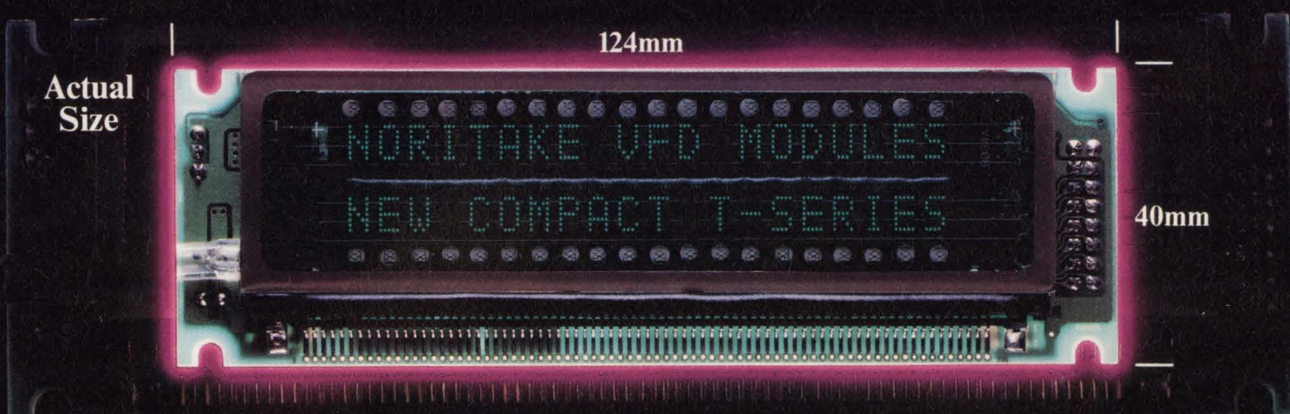

Part No.	No. of Characters	Character Size (WxH)mm	Tpy. Icc (mA)
CU165SCPB-T20A*	1X16	3.05X 5.05	TBD
CU205SCPB-T20A*	1X20	3.30X 5.00	TBD
CU209SCPB-T20A	1X20	4.45X 8.80	300
CU406SCPB-T20A	1X40	3.00X 5.00	350
CU20025SCPB-T20A	2X20	2.60X 5.00	320
CU200211SCPB-T60A	2X20	6.40X11.20	1200
CU40026SCPB-T20A	2X40	3.30X 5.10	700
CU20045SCPB-T23A	4X20	3.00X 5.00	400
CU20049SCPB-T20A	4X20	6.40X 9.10	1100

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CIRCLE NO. 86

You can use the modulated-ramp signal for determining differential phase and gain.

Fig 9 shows the equivalent circuit the routine in **Fig 8** produces. As you can see, the circuit uses 15 pulse and sine-wave generators, as well as two squaring circuits and a large collection of signal summers and multipliers. The 1-MΩ resistors are tokens, essentially open circuits, inserted because Spice will not work without generator and load impedances. Configuring such a circuit without the aid of Spice would be frightening to contemplate.

If your simulation of this last test signal is complete, you have all the tools necessary to build video test signals. Every test signal is a composite of luminance and chrominance information. All you have to do is provide the timing; superposition takes care of the rest. You should also now understand this technique well enough to tackle other complex waveforms. PAL and proposed HDTV signals are easy to simulate if you take the time to sit down and disassemble them into pulses, levels, and frequencies.

The computational load of these simulations is much greater than that of a simple transient or ac analysis of a circuit. Completing these simulations takes a correspondingly longer time. The signals described here were run on both a standard IBM PC/XT and a Compaq 386/25. The numbers in **Table 4** are those for a Compaq 386/25. A VAX 780 would have comparable numbers, and a 4.77-MHz IBM PC/XT with a coprocessor would take approximately 18 times longer. At the completion

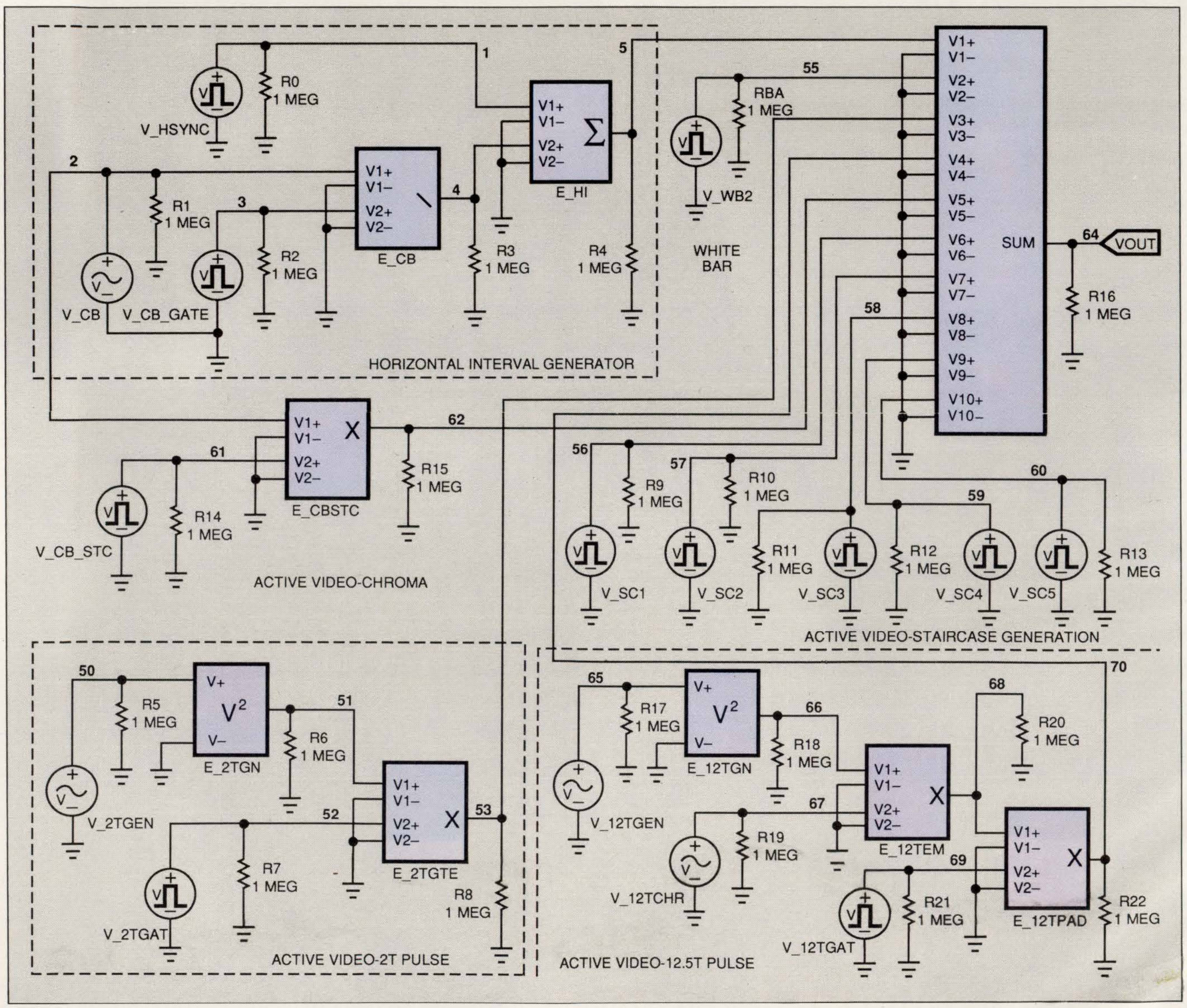

***Fig 9—You need a plethora of generators, squarers, summers, and multipliers** to generate the NTC7 test signal. This equivalent circuit, which is useful for testing all essential video parameters in a video-circuit model, corresponds to the PSpice listing in **Fig 8**.*

Decisions, Decisions, Decisions...

The pressure is always on. You've got to figure out how to get to market faster and more cost-efficiently. You've got to reduce the after-sales service costs that dilute profitability. Plus, you've got to increase your share-of-market and maintain revenues that will keep your management and the stockholders happy.

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Table 4—Signal-execution loads

Signal	Time to run	Extra nodes
Modulated ramp	1 min, 16 sec	10
Multiburst	3 min, 20 sec	27
NTC7 composite	2 min, 57 sec	24

of all computations, the PSpice .OPTIONS statement is set to

ITL5 = 0 ; Allow an unlimited number of iterations.
RELTOL = 0.01 ; This cuts down on computation time,
; but does not seriously degrade accuracy.

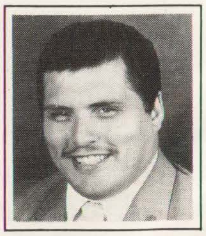
Set up the PSpice .TRAN statement for an analysis length that's appropriate for your application. All the timing simulations performed here were executed to an analysis length of 100 μsec. The PSpice .PROBE facility generated the plot files.

If you intend to do repeated simulations of video signals, try using the .SUBCKT facility in Spice to build up a repertoire of these signals. This utility lets you keep the circuits in a library and call them up when you need them. EDN

References

1. PSpice Manual, MicroSim Corp, 23175 La Cadena Dr, Laguna Hills, CA 92653.
2. Tuinenga, Paul W, *SPICE: A Guide to Circuit Simulation & Analysis Using PSpice*, Prentice Hall, Englewood Cliffs, NJ, 1988.
3. "Television Operational Measurements: Video and RF for NTSC Systems," TEK Television publication AX-3323-2, Tektronix Inc, Box 500, Beaverton, OR 97077.
4. "Video Facility Testing Technical Performance Objectives," NTC7 Report, Public Broadcasting Service, Engineering Services, 475 L'Enfant Plaza SW, Washington, DC 20024.

Author's biography



Anthony Radice is a senior digital design engineer in General Instrument's (Hatboro, PA) Broadband Communications Group, where he's worked for eight years. He's responsible for the design and development of digital audio and video transmission systems. He holds a BSEE from Drexel University. Tony is a volunteer fireman and enjoys personal computing as a hobby.

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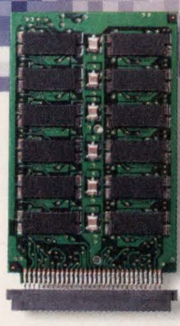

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	16MB	✔	✔		✔	✔
EEPROM	8KB - 192KB	✔	✔		✔	✔
FLASH EEPROM*	512KB - 2MB	✔	✔		✔	✔
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CIRCLE NO. 77

Amplifier scheme lowers drift and noise

Jim Williams
Linear Technology Corp, Milpitas, CA

Fig 1's circuit combines a low-noise op amp, IC_1, with a chopper-based carrier-modulation scheme to achieve a low-noise, low-drift dc amplifier whose performance exceeds any currently available monolithic amplifier. The amplifier's offset is less than 1 μV, and its drift is less than 0.05 μV/°C. The circuit in **Fig 1** has noise within a 10-Hz bandwidth less than 40 nV. The amplifier's bias current, which is set by the bipolar input of IC_1, is about 25 nA. These specifications suit the demands of transducer signal-conditioning circuits.

The 74C04 inverters (IC_3 to IC_6) form a simple 2-phase square-wave clock running at about 350 Hz. The complementary oscillator signals (ϕ_1 and ϕ_2) provide drive to S_1 and S_2, respectively, causing a chopped version of the input to appear at IC_1's input. IC_1 amplifies this ac signal. S_3 and S_4 synchronously demodulate IC_1's square-wave output. Because S_3 and S_4 switch synchronously with S_1 and S_2, the circuit presents proper amplitude and polarity information to IC_2, the dc output amplifier. This output stage integrates the square wave to provide a dc voltage output. R_1 and R_2 divide down the output and feed it back to the input chopper where the divided output serves as a zero signal reference. The ratio of R_1 and R_2 sets the gain, in this case to 1000. Because a 1-μF capacitor ac-couples IC_1 to the output stage, IC_1's dc offset and drift don't affect overall circuit offset, resulting in the overall amplifier's low offset and drift.

When using this amplifier, it's important to realize that IC_1's bias current flowing through the input-source impedance causes additional noise. In general, to maintain low-noise performance, the source resistance should be below 500Ω. Fortunately, the resistances of transducers such as strain-gauge bridges, RTDs, and magnetic detectors are well below this figure.
(EDN BBS /DI_SIG #936) **EDN**

To Vote For This Design, Circle No. 746

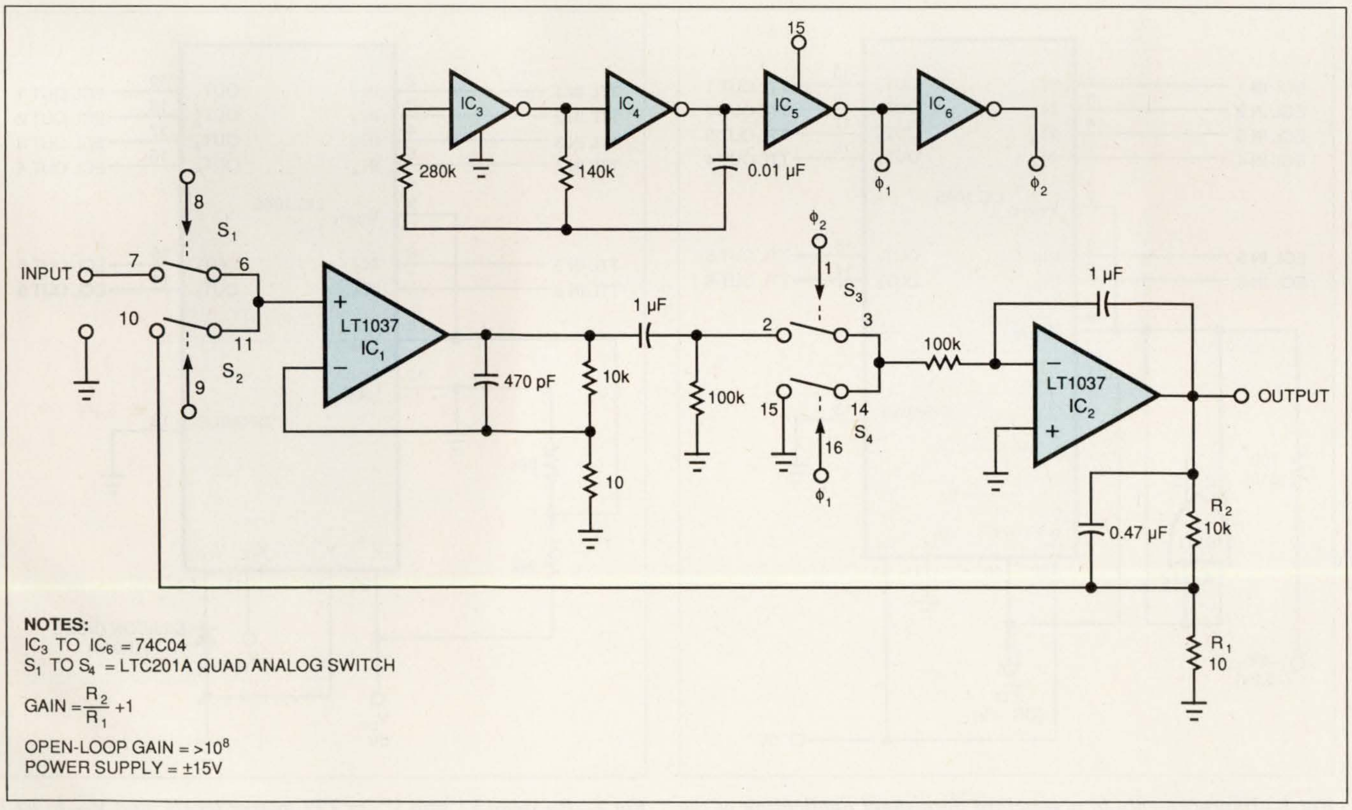


***Fig 1—By synchronously modulating the input** and ac-coupling a low-noise op amp to a dc amplifier, this circuit achieves noise and drift specs of 1 μV and 0.05 μV/°C, respectively.*

IC converts from TTL to ECL and back

Rolf R Safferthal
Independent Consultant, Dreieich, Germany

The circuits in **Fig 1** and **Fig 2** convert as many as six signals per chip either from ECL to TTL or from TTL to ECL using the same IC. The IC holds six translators and typically consumes less than 8 mW per ECL-TTL converter. It consumes 4 mW when converting from TTL to ECL. These power levels are 10 to 20 times less than the popular 10124 and 10125 translators. The tradeoff for lowering the power is speed—the propagation delay is 60 nsec for ECL-TTL translation and 100 nsec for TTL to ECL.

The data sheet for the LTC-1045 IC shows a typical application for ECL-to-TTL conversion. You can reduce the power consumption of this circuit by another 30% by reducing the $-5.2V$ supply to $-2V$. Also, you can improve upon the reference-voltage generation. V_{TRIP1} is the reference input for inputs 1 through 4, and V_{TRIP2} is for inputs 5 and 6. A simple resistor divider works well with a clean ECL supply. However, if the reference input picks up too much noise, you can easily replace the resistor divider by an unused, inverting 10101 ECL gate with direct feedback (**Fig 1**). The output of such a configuration delivers a stable reference voltage and exactly tracks the ECL trip point with voltage and temperature. To attain the highest possible speed and a hysteresis of approximately 20 mV, the I_{SET} pin should connect directly to V^-.

You can also use this IC as a TTL-to-ECL converter (**Fig 2**). The device has four power-supply connection pins. Two of them, V^+ and V^-, power the internal circuit. The minimum voltage difference between these pins has to be 4.5V, and the input voltage must stay within these rails. For a TTL-to-ECL converter, V_{CC} normally equals 5V. Because the incoming voltage swing is relatively large with TTL, the easiest way for building up the reference voltage is with a resistor divider.

The other two power-supply connections, V_{OH} and V_{OL}, power the output-driver stage. The minimum voltage difference between these pins has to be 3V, and the values determine the output levels, swinging

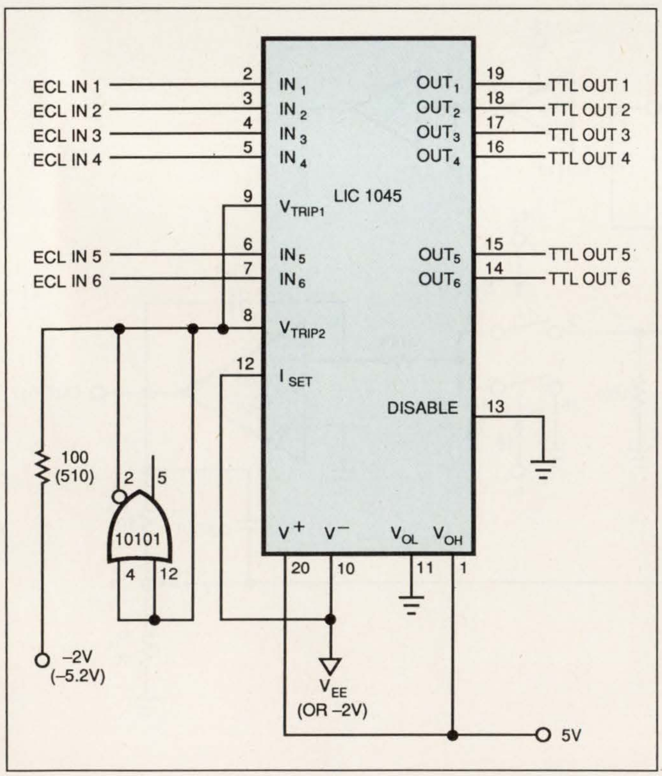


Fig 1—Improvements to a standard data-sheet application of the IC's ECL-to-TTL converter include lowering the supply voltage to −2V and using an ECL gate to generate the reference voltage.

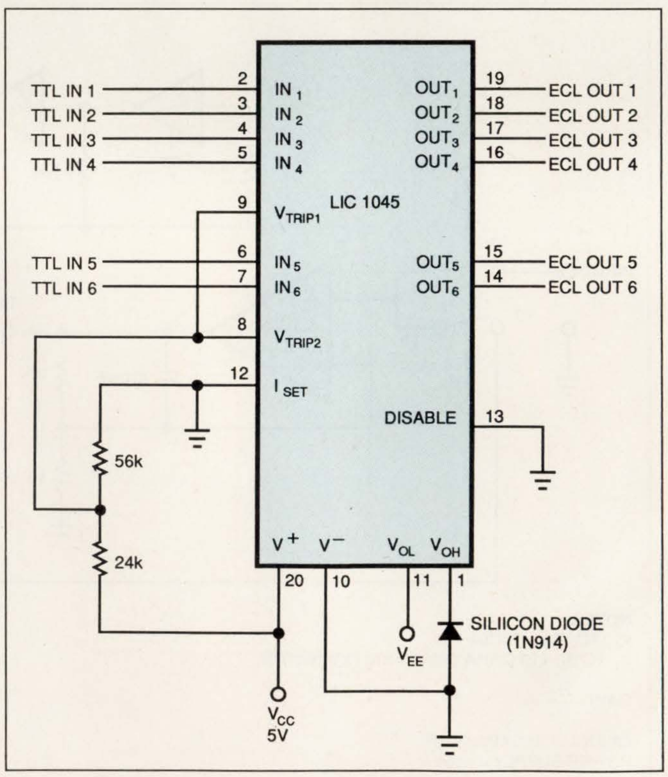
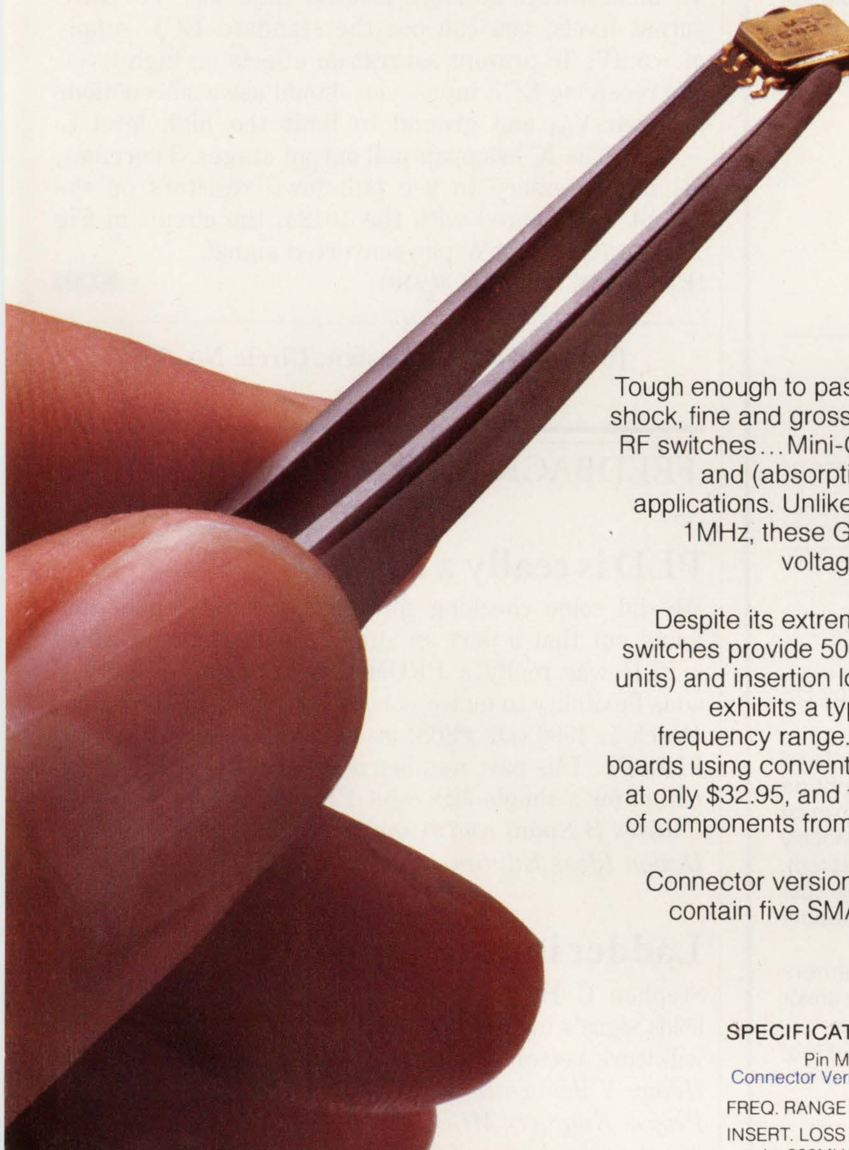


*Fig 2—By tying V^+ and V^- to TTL power levels, and V_{OL} to ECL levels, you can reverse the circuit in **Fig 1** and create a TTL-to-ECL converter.*



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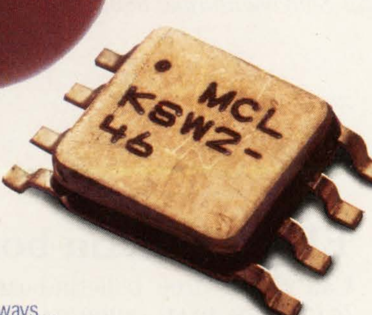

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nearly from rail to rail under moderate loads. The selection of these voltage levels does have some constraints. V^+ must always be more positive than V_{OH}. For ECL output levels, you can use the standard ECL supply of −5.2V. To prevent saturation effects on high levels at a receiving ECL input, you should use a silicon diode between V_{OH} and ground to limit the high level to −0.7V. The IC has push-pull output stages. Therefore, it's not necessary to use pull-down resistors on the outputs. Compared with the 10124, the circuit in **Fig 2** saves 10 to 30 mW per converted signal.
(EDN BBS /DI_SIG #940) EDN

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FEEDBACK AND AMPLIFICATION

PLD is really a PROM

We did some checking for an interested reader and found out that a part an author (and company) called a PLD was really a PROM. The Design Idea "PLD adds flexibility to motor controller" on pg 177 of EDN's March 1, 1990 (DI #808) issue contains a part labeled PLE5P8. This part number is an obsolete MMI designation for a simple 32×8-bit PROM.

Charles H Small and Anne Watson Swager
Design Ideas Editors

Ladder improves design

Stephen C Hageman's Design Idea, "Peak detector holds signals indefinitely" (EDN, May 24, 1990, pg 173), will work better if you use an R/2R ladder network.

Heiner V Schlichting
Project Engineer MBB
342 Schrobenhause 8898, Germany

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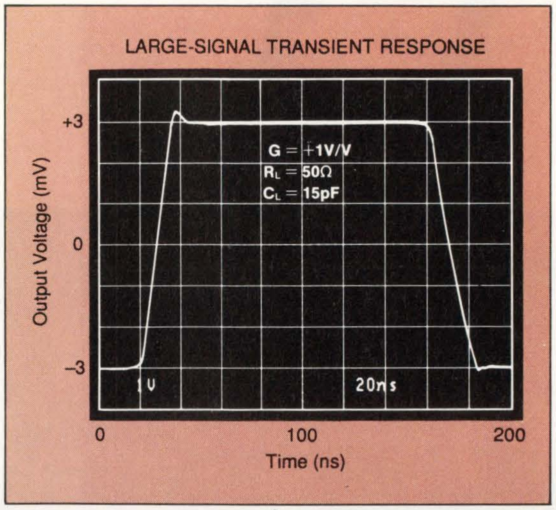

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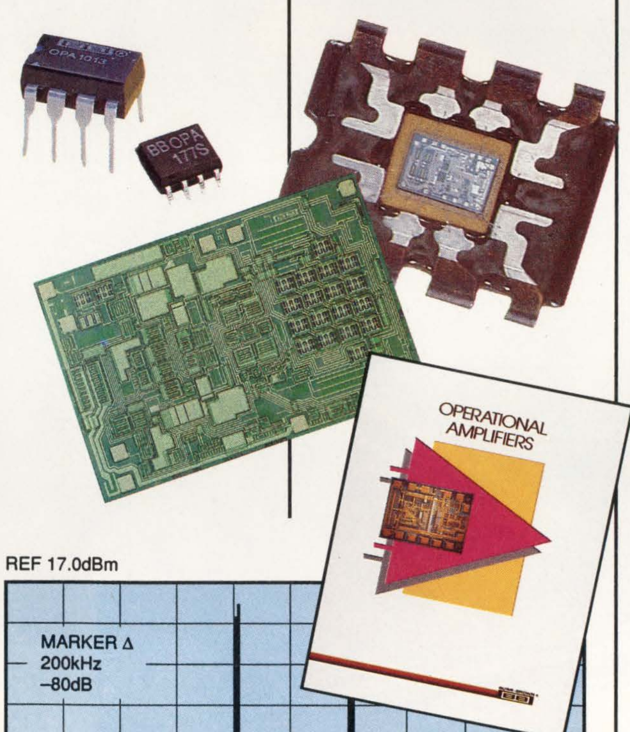

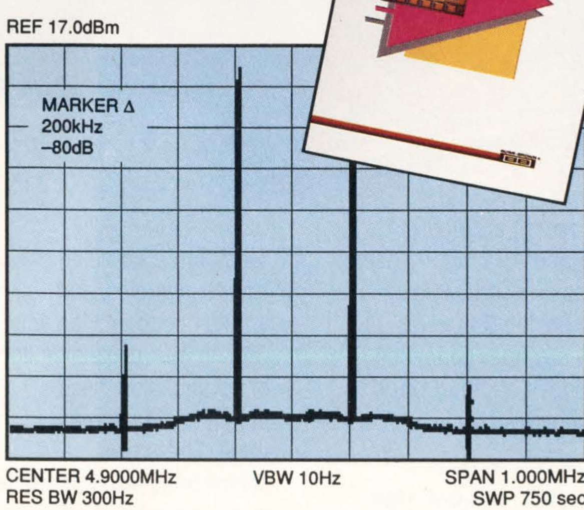

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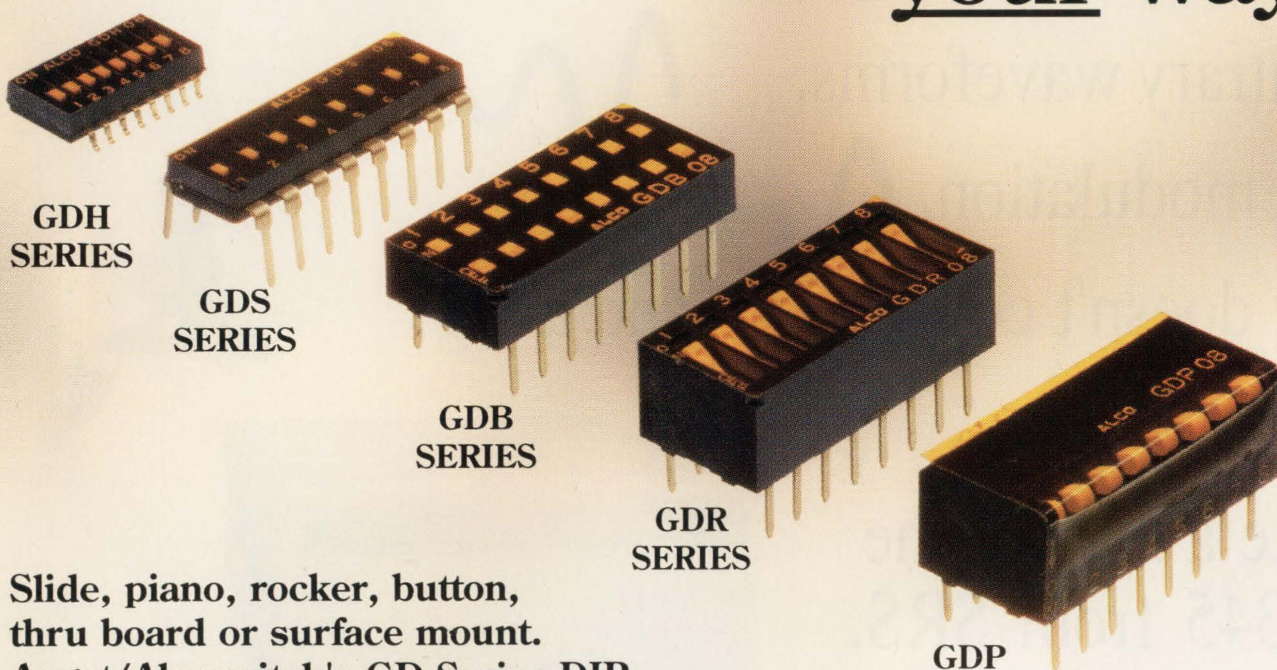

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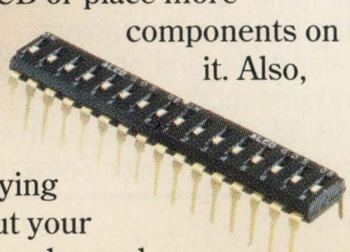

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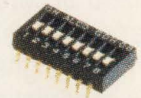

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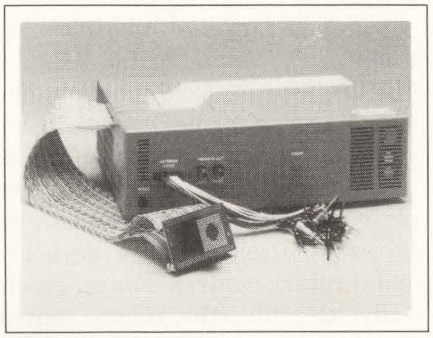
CIRCLE NO. 81

TEST & MEASUREMENT INSTRUMENTS

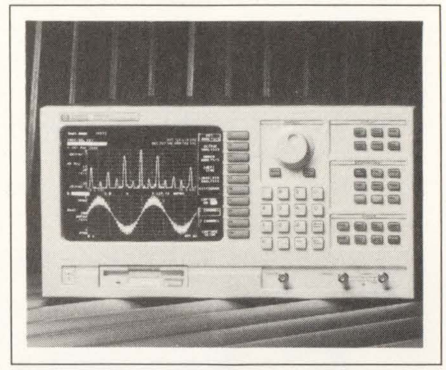


68302 In-Circuit Emulators

- *Have two 4k × 72-bit trace buffers*
- *256k-byte emulation memory expands to 2M bytes*

The HMI-200-68302 supports all features of the 68302 μP. The HMI-200-68000 with the HMI-240-68302 adapter also supports the 68302 but has some limitations. However, this emulator and adapter also work with the 68000, 68008, and 68010. Both emulators permit real-time emulation, provide four complex break and trigger points, and offer a pair of 4k × 72-bit trace buffers. Emulation memory is 256k bytes expandable to 1M or 2M bytes. The Sourcegate debugger works with C, Pascal, Ada, and PL/M compilers from more than a dozen sources. A performance-analysis option is also available. HMI-200-68302, $8995; HMI-200-68000 with HMI-240-68302, $8495; Sourcegate for MS-DOS, $1500; Sourcegate for Sun and Apollo workstations, $3000; performance-analysis option, $2495.

Huntsville Microsystems Inc, Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. FAX (205) 882-6701. **Circle No. 351**



FFT-Based Spectrum/ Network Analyzer

- *Makes swept-sine measurements*
- *Automates tests using programs written in Basic*

The 35665A FFT-based instrument performs spectrum analysis to 102.4 kHz and network analysis to 51.2 kHz. Among the unit's capabilities are swept-sine measurements and curve fitting. The analyzer's capture memory can store as many as 6.4M bytes. Frequency resolution is 400 lines. A 1.44M-byte floppy-disk drive stores instrument states, data, and programs. You can program the unit in the vendor's Instrument Basic language. In the fast-average mode, the analyzer makes 30 sets of measurements/sec; with its display enabled, it updates its display to faster than 10 times/sec. From $12,500. Delivery, 12 weeks ARO.

Hewlett-Packard Co, 19319 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 352

Synthesized Function Generator

- *Generates sine, square, triangular, and ramp waveforms*
- *Operates from dc to 1.6 MHz*

The 2003 synthesized function generator produces sine, square, triangular, and ramp waveforms from dc to 1.6 MHz. The unit, which displays messages on a 2-line LCD, receives commands from a keyboard and a rotary control. For an essentially long life, the rotary control is a position encoder, rather than a potentiometer. An optional RS-485 interface allows remote control. You can place several generators on a single serial loop and assign each generator a unique address. Output is 20V p-p into an open circuit and 10V p-p into 50Ω. $500.

Global Specialties, 70 Fulton Terrace, New Haven, CT 06512. Phone (800) 527-1028; in CT, (203) 624-3103. FAX (203) 468-0060.

Circle No. 353

V20H/V30H In-Circuit Emulator

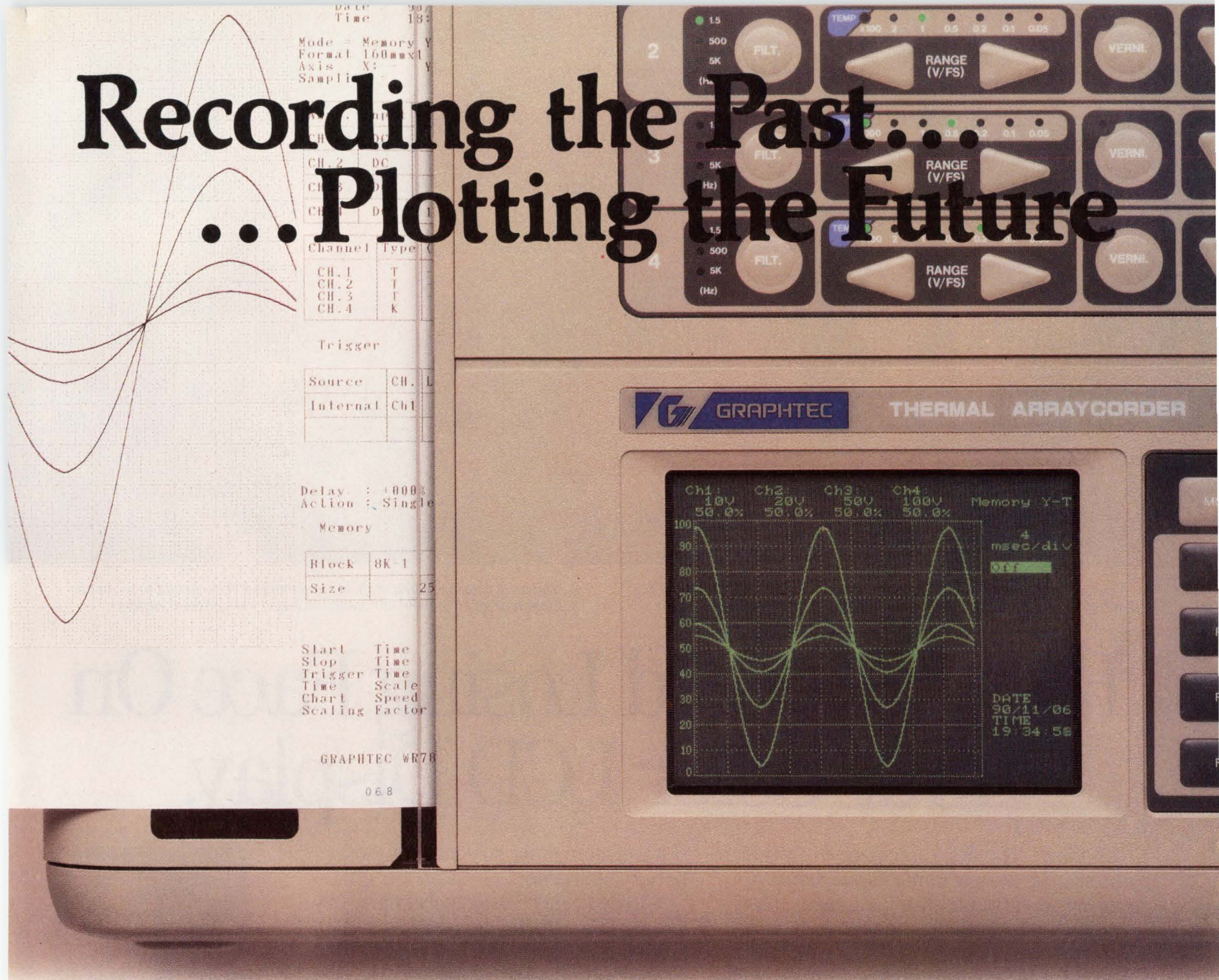
- *Has 131,072 hardware breakpoints*
- *Displays trace data in C or PL/M formats*

The V20H/V30H Icealyzer is an in-circuit emulator for the NEC V20H and V30H μPs. It includes 131,072 hardware breakpoints that you can set on any condition or machine-cycle type—including data accesses. The included source-level debugger shows trace data in C, PL/M, or assembly language. A real-time performance analyzer identifies time-critical routines for optimization. The performance analyzer captures every instruction to ensure acquisition of infrequently accessed routines—for example, those that service interrupts. $7295.

Softaid Inc, 8930 Route 108, Columbia, MD 21045. Phone (800) 433-8812; in MD, (301) 964-8455. FAX (301) 596-1852.

Circle No. 354

Recording the Past...
...Plotting the Future



Our reputation precedes us! From 5 subsidiaries and 35 distributors in more than 40 countries worldwide, thousands of customers purchased more in 1989 than ever before. And they were able to choose new products from an ever-expanding array of plotters, penless plotters, digitizers, recorders and supplies.

The Graphtec reputation is one of building products that work well and last a long time. We earned that reputation the hard way, by delivering over 40 years of the best innovation, support, and after-sales service in the industry.

You really can see the difference in Graphtec products. Our new WR7800 Thermal Arraycorder not only has a 14-bit A/D converter for better waveform accuracy, it also includes an easy-to-read 320×256 dot electroluminescent screen for monitoring real-time or stored data. Other notable features include 32Kb and 256Kb memory cards, 3 built-in thermocouple inputs, an RS-232C interface (GPIB optional), and a jog dial for easy operability.

We invite you to go see a Graphtec WR7800 and experience these enhanced features firsthand.

WR7800

GRAPHTEC

GRAPHTEC CORPORATION 503-10 Shinano-cho, Totsuka-ku, Yokohama 244, Japan Tel: (045) 825-6250 Fax: (045) 825-6396

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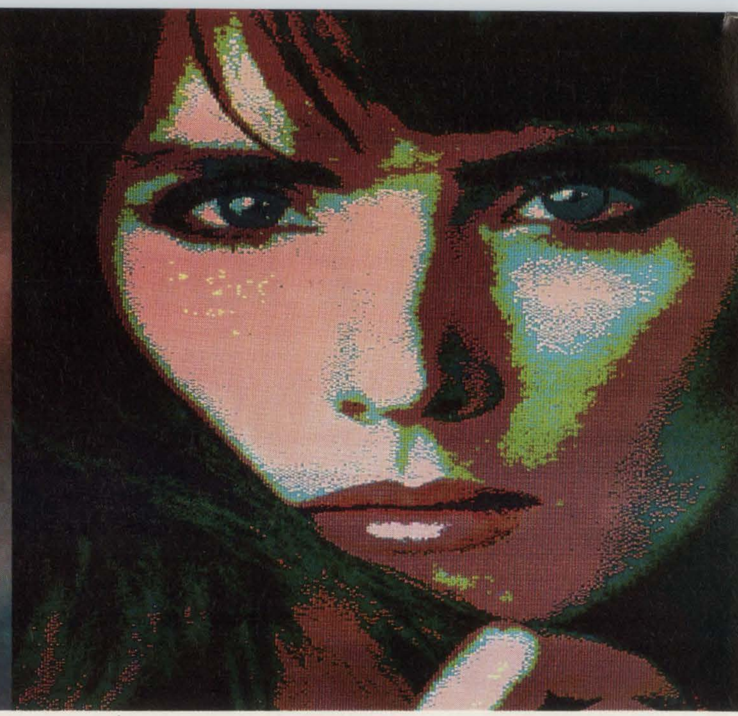
Europe: Graphtec Europe GmbH Tel:(040)511-5059 Fax:(040)511-9155 **United Kingdom: Graphtec (UK) Ltd.** Tel:(0270)625-115 Fax:(0270)626-733

Picture your flat panel display using Cirrus Logic controller chips. They actually add colors to your display capabilities for more realistic shading.



The same panel looks flat without our enhanced VGA capabilities. And it will lose face faster without our optimized power management system.

How To Avoid Losing Face On Your Color LCD Display.

Face it. The first thing everybody notices about your newest laptop is the display quality. Is it bright? Are the images clear and well modeled? Are the colors vivid?

With Cirrus Logic LCD VGA controllers, your answer is yes. Which is why we're the leading supplier of display controller chips in the laptop and notebook market.

For life-like 3-dimensional imaging, Cirrus Logic color LCD controllers offer technology leadership for your color products. With direct support for the latest active-matrix color LCD panels. Our controller chips do more than support your panel's color capabilities — they enhance it with full VGA color support and a fuller color palette. To give you color so good it competes with CRT quality.

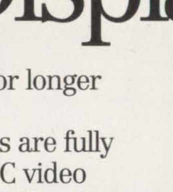
Our monochrome solutions give you displays that *PC Magazine* called "the stars of our VGA color-mapping tests"* with up to 64 shades of gray. And with a lower dot clock rate, your power consumption is lower than other solutions for longer battery operation.

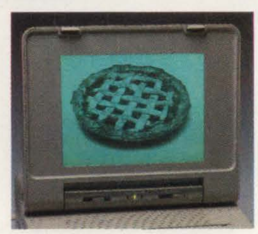
Cirrus Logic LCD controllers are fully compatible with the popular PC video standards and will work with LCD, plasma, or electroluminescent displays.

Simplify your design job. A higher level of integration gives you all this in the smallest form factor available. We also supply software and hardware design notes and full design support. You get the results you want quickly and easily.

Design a more competitive product. One that looks better — and makes you look better. That lasts longer on a battery. Use the display solutions from a proven technology leader in laptop and motherboard VGA: LCD controller chips from Cirrus Logic.

Get the picture. Get more information on LCD controllers. *Call 1-800-952-6300, ask for dept. LL24*





Cirrus Logic monochrome LCD controllers will also make everything from realistic scanned images to business charts look tastier.

CIRRUS LOGIC

C L O S I N G T H E G A P

INTEGRATED CIRCUITS

Dual-Port RAMs

- *Have 9-bit width*
- *Access times as low as 25 nsec*

The first two members of this family of dual-port RAMs have configurations of 1k×9 bits (IDT70101, IDT7010, IDT70105) and 2k×9 bits (IDT70121, IDT7012, IDT7015). Speed ratings range from 25 to 55 nsec. The ×9 configuration of these devices allows designers to use the extra bit as a parity bit for error detection. In addition, the devices are true dual-port memories that include on-board arbitration logic—an arrangement that allows simultaneous access of data from both ports by multiple processors, without risk of data corruption. Another advantage is that the 25-nsec devices allow zero wait-state operation. The devices come in 48-pin DIP and LCCs, and sidebrazed 52-pin LCC and plastic leaded chip carriers. IDT70105-25P, $21.65 (100).

Integrated Device Technology Inc, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 988-3029. **Circle No. 355**

Low-Voltage Compandor

- *Operates from 2.1 to 7V*
- *Provides 40 dB of control*

The MC33110 compandor IC contains two variable-gain circuits. One circuit is configured as an expander, and the other is configured as either a compressor or expander. Each circuit has a full-wave rectifier to provide average-value information to a variable gain cell located in either the input stage or the feedback path. A stable bandgap reference provides the necessary precision voltages and currents. Operating from a supply voltage of 2.1 to 7.0V, the compandor can compress an 80-dB dynamic range to 40 dB and re-expand it to 80 dB. The reference unity-gain level is 100 mV rms. 14-pin DIP or 14-pin SO package, $0.82 (10,000).

Motorola Inc, EL340, 2100 E Elliot Rd, Tempe, AZ 85284. Phone (602) 897-3615. **Circle No. 356**

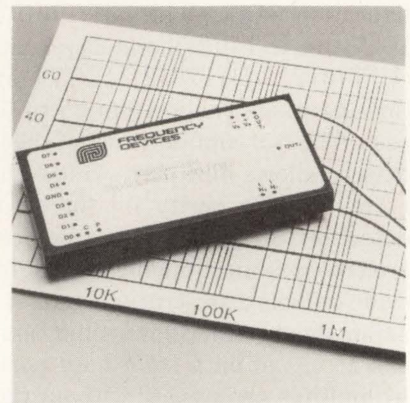
Video Crosspoint Array

- *Has eight inputs and four outputs*
- *Bandwidth is 300 MHz*

According to the vendor, the DG884 is the first monolithic crosspoint array to offer a 300-MHz bandwidth in an 8×4 configuration. A digitally selectable switching matrix is able to route any of the array's eight inputs to any of its four outputs. The use of DMOS switches connected in a T arrangement is instrumental in providing the −3-dB bandwidth of 300 MHz, and adjacent-input crosstalk of −85 dB at 5 MHz. The array also features an $r_{DS(on)}$ resistance of 45Ω (typ) and an off-state input capacitance of 8 pF max. Extensive TTL-compatible control and two sets of on-chip latches simplify interfacing to a microprocessor data bus. The on-chip data latches also provide a readback feature to interrogate any of the switches' existing status in a network. The DG884 in a 44-pin plastic leaded chip carrier or ceramic LCC, from $24 (1000).

Siliconix, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (800) 554-5565, ext 1900.

Circle No. 357



Programmable-Gain Amplifiers

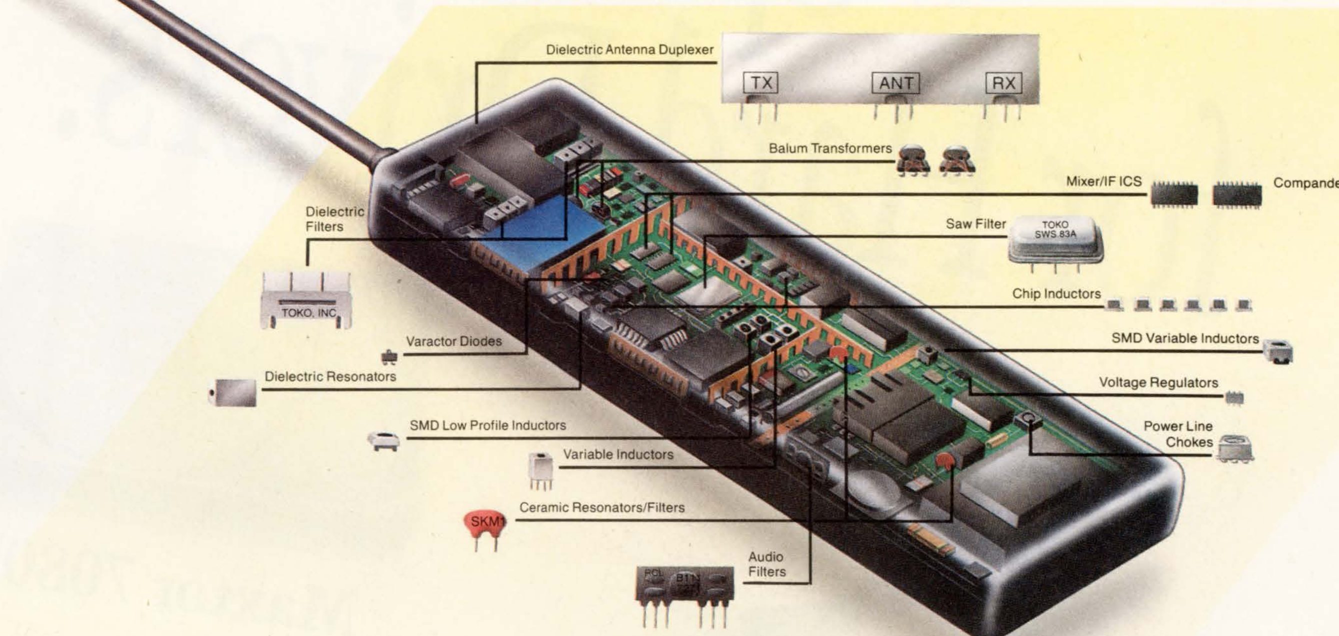
- *Have 100-kHz bandwidth*
- *Three models available*

Featuring a full-power bandwidth of 100 kHz, 830PGA programmable-gain amplifiers have a rated output of ±10V at ±10 mA. The amplifiers are available in gain ranges of 0 to 20 dB in 0.5-dB steps, 0 to 40 dB in 1.0-dB steps, and 0 to 60 dB in 2.0-dB steps. Gain selection is achieved by an 8-bit data word, a latch-strobe bit, and a transition-polarity bit, all of which are CMOS compatible. The amplifiers have a CMRR of 80 dB typ at 1 kHz and 60 dB min from 10 Hz to 100 kHz. THD is 0.003% at 1 kHz and 0.02% at 90 kHz. Gain matching between individual amplifiers is 0.04 dB, and phase matching is 0.5°. Other specifications include an input impedance of 1 MΩ shunted by 47 pF, an input noise of 20 μV over the 100-kHz bandwidth, and an output impedance of less than 1Ω. The amplifiers operate from a ±15V supply. $70 (100).

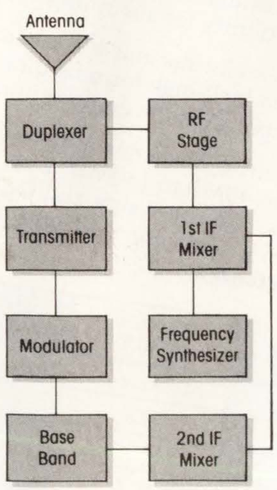
Frequency Devices Inc, 25 Locust St, Haverhill, MA 01832. Phone (508) 374-0761. FAX (508) 521-1839.

Circle No. 358

The Undercover Story On RF Performance.



For RF Components with the Quality and Performance Difference, the Name to Know Is Toko.



Look inside leading personal communications products, and you'll find more of Toko. From dielectric antenna duplexers to power line chokes, Toko can offer an application-specific RF solution for every stage of your design.

Our selection of RF components is the most comprehensive in the industry and includes: surface mount, fixed, variable, and molded inductors; LC, SAW, ceramic, helical and dielectric filters; Balun transformers; and communication-specific ICs.

All are designed to work together and feature low loss for exceptional performance. Tuneable or fixed construction magnetics, ceramics, hybrids, and ICs...all are available from one source: Toko.

Toko is also the world's largest manufacturer of coils and filters and one of the most vertically integrated. Our quality and reliability are unequalled; an enviable industry-low failure rate has resulted in numerous top supplier preferred classifications.

Whatever your RF/IF application–personal communications, satellite communications, computer, automotive convenience systems, or video–the name to know is Toko.

Discover the quality and performance difference Toko products can make in your RF/IF application. For more information, write Toko today, attention: RF/IF Engineering, or call the Toko location nearest you: Midwest, (708) 297-0070; East, (203) 748-6871; Southeast, (205) 772-8904; West, (408) 432-8281.

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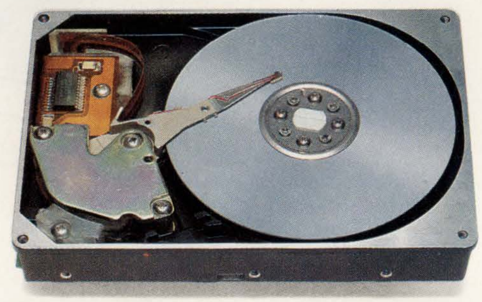
CIRCLE NO. 96

Specs for Hard Drivers.



Maxtor 7080

Simplicity of design makes Maxtor's Cheyenne Series inch-high 80MB 7080 disk drive the most reliable in its class. Compare Maxtor's four-head, two-platter design to Seagate's six-head, three-platter design. Fewer moving parts make Maxtor's drives inherently more dependable.

Power consumption is a very low 2.8 watts, making it one of the lowest in the 80MB class. The 7080 is also Novell Labs certified, and is available with either SCSI or AT interface, giving you flexibility for a winning system.

Exceptionally fast 17ms seek time and 32K cache buffer in the new generation inch-high form factor give Maxtor faster data throughput than the competition.

Call and ask about our entire Cheyenne family of disk drives with capacities from 40MB to 130MB. Don't fall for the off-the-wall claims. Give us a shot and we'll prove Maxtor specs can't be matched. **Call your nearest Authorized Maxtor Distributor.**

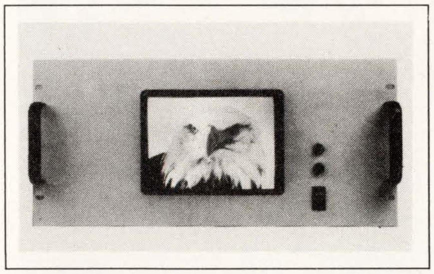
3.5-inch Disk Drive Spec.	**Maxtor 7080A**	Seagate 1102A
Seek Time	**17 Msec.**	19 Msec.
Standard Buffer Size	**32K**	8K
Form Factor	**3.5" x 1"**	3.5" x 1.6"
Heads-Disks	**4/2**	6/3
Avg. Power Consumption	**2.8 watts**	9 watts

We Drive Harder.

Maxtor®

NEW PRODUCTS

COMPUTERS & PERIPHERALS



Rack-Mount VGA Monitor

- *Has a 10-in. screen with a 0.28-mm dot pitch*
- *Has 8.75×15.3-in. enclosure*

The RMM-213 rack-mount, 10-in. color monitor comes in an 8.75×15.3-in. enclosure and is VGA compatible. It operates with computers that have an RGB analog video output and a TTL synchronization output. Its input-signal connector is a 15-pin D-shell. The CRT has a 0.28-mm dot pitch, and a short-persistence phosphor produces sharp pictures. The monitor produces 640×480-, 640×400-, and 640×350-pixel images. A tinted Lexan protective panel covers the screen. Front-panel controls include power on/off, brightness, and contrast. An internal switching power supply operates from 110V ac having 50- or 60-Hz line frequencies. The unit has a horizontal scan rate of 31.5 kHz ±400 Hz and a vertical scan rate of 60 or 70 Hz. $1095.

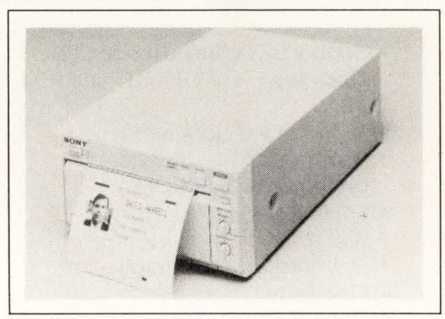
Recortec Inc, 1290 Lawrence Station Rd, Sunnyvale, CA 94089. Phone (800) 729-7654; in CA, (408) 734-3443. FAX (408) 734-1240. **Circle No. 362**

NTDS Interface Adapter

- *Contains single LLS channel for VMEbus*
- *Multichannel DMA controller permits full-duplex operation*

The Model 10042601 VMEbus board provides a low-level-serial (LLS) Type-E interface for a Navy Tactical Defense System (NTDS). An MC68000 μP lets you write application software to integrate or emulate NTDS devices. The board's features include a 32k-word dual-port static RAM buffer, a 4-channel DMA controller, a 16-bit VMEbus data path, 24-bit VMEbus addressing, and programmable interrupt levels and vectors. The DMA controller permits full-duplex operation for the LLS channel. Software-controlled Abort and Interrupt features simplify LLS transaction protocols. An EPROM provides the device driver, which supplies buffer transfers, interrupt control, asynchronous data transactions, data and command detection, and configuration commands. The device driver also lets you use high-level languages, such as C, Fortran, or Ada, to control operations. $4975.

Get Engineering Corp, 9350 Bond Ave, El Cajon, CA 92021. Phone (619) 443-8295. FAX (619) 443-8613. **Circle No. 363**



Video Printers

- *Include one color and two b/w models*
- *Produces peel-off adhesive-backed prints*

The UP-910 b/w printer, one of three video-printer models, produces prints as large as 6×8 in. It produces 128 levels of gray and a maximum resolution of 750×508 dots. It takes 25 sec to produce a print, and it operates on EIA or CCIR b/w video standards. The UP-610 b/w sticker printer produces 2⅛×3½-in. prints. The unit produces peel-off, adhesive-backed prints. A typical application is the labeling of parts with a video photo; this application augments barcoding methods that are used to identify and control inventory. The UP-3000 color printer produces 500-line resolution prints. It produces 256 colors from a palette of more than 16 million colors/pixel. A wide-scan mode produces prints as large as $4^{3}/_{8} \times 3^{1}/_{4}$ in. UP-610, $2000; UP-910, $2150; UP-3000, $3895.

Sony Security Systems, 3 Paragon Dr, Montvale, NJ 07645. Phone (201) 358-4954. FAX (201) 358-4927.

Circle No. 364

SCSI Supervisor

- *Lets you remove devices while system is operating*
- *Runs 17 diagnostic tests on individual drives*

The SSM6 SCSI Manager equips a SCSI-drive enclosure with a variety of supervisory functions. It lets you remove a SCSI disk, tape, or optical drive while the host system is operating, or "hot." The unit maintains the integrity of the SCSI bus so that removal or installation of a device in an active system doesn't affect ongoing operations. Because the unit can essentially isolate an attached device, it can also perform the following functions: change SCSI ID numbers; copy data from one device to another; compare contents in different devices; power individual devices up and down; format drives; run as many as 17 diagnostic tests on individual drives; and reset the SCSI bus. You can operate the unit from a front-panel keyboard and LCD or from a system terminal. A terminal connects to the unit via a serial port. The SSM6 adds approximately $1500 to the price of a drive enclosure (OEM qty).

Sigma Information Systems, 3401 E La Palma Ave, Anaheim, CA 92806. Phone (714) 630-6553.

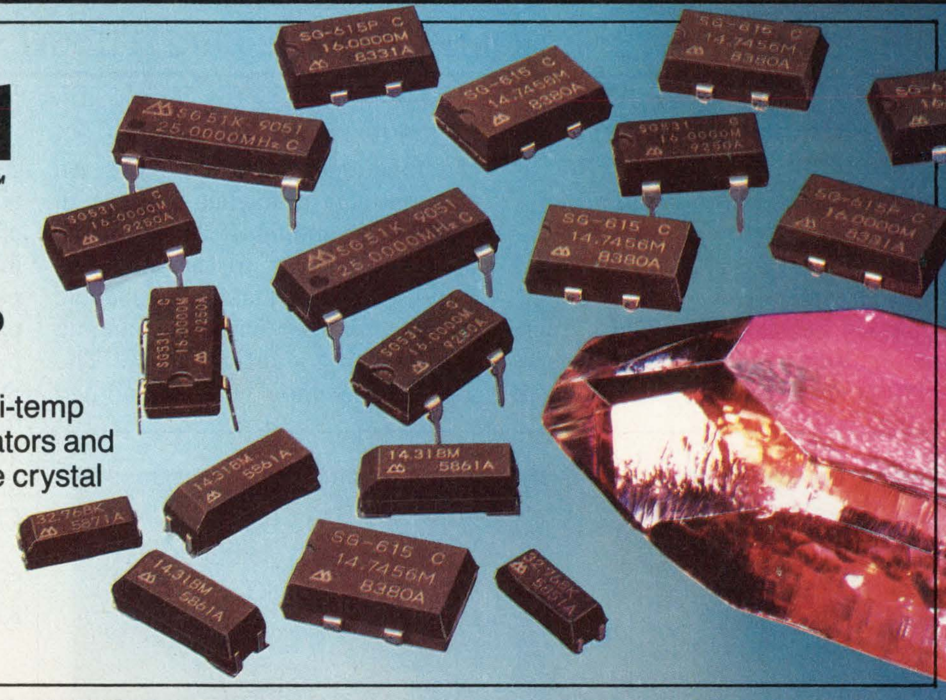
Circle No. 365

EPSON

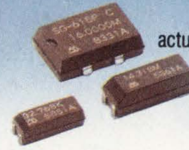
THE CRYSTALMASTER™

leads new crystal oscillator technologies into the 90's with...

the most cost effective hi-temp SMD crystals and oscillators and low cost plastic thru-hole crystal oscillators.



EPSON SURFACE MOUNT CRYSTALS AND OSCILLATORS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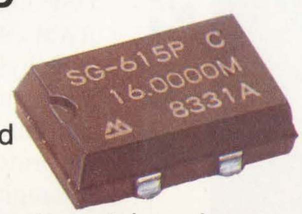


Epson has pioneered the first truly heat resistant crystal for use in its surface mount crystals and crystal oscillators. Capable of withstanding 260°C for 20 seconds...far above the demands of standard IR and vapor phase reflow processing systems...these labor-saving high-temp SMD crystals have become the accepted standard for surface mount crystal and oscillator components.

MODEL SG-615 OSCILLATOR

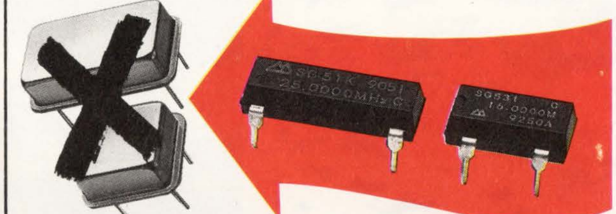
Frequency:	1.5 to 66.7 MHz
Symmetry:	45/55 (TYP)
Rise/Fall Time:	5 nsec (TYP)
Tristate:	Available
Compatible Technology:	CMOS and TTL
Op. Temp. Range:	−40°C to 85°C

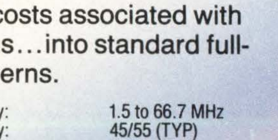
MODEL MA 505/506 CRYSTAL
Frequency: 4.00 to 66.7 MHz

MODEL MC-405 CRYSTAL
Frequency: 32.768 KHz

EPSON® EPSON AMERICA, INC.
Component Sales Department Telephone: 213/787-6300

EPSON THRU-HOLE OSCILLATORS
REPLACE METAL CAN OSCILLATORS

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Epson has introduced the first plastic low cost, high performance auto-insertable thru-hole crystal oscillator. Its unique hermetically sealed crystal, embedded in a plastic package, gives the same EMI protection and higher performance than metal can oscillators...at a much lower cost. And, the auto-insertion feature reduces manufacturing costs associated with hand inserting metal cans...into standard full-size or half-size hole patterns.

MODEL SG-51/SG-531 OSCILLATOR

Frequency:	1.5 to 66.7 MHz
Symmetry:	45/55 (TYP)
Rise/Fall Time:	5 nsec (TYP)
Tristate:	Available
Compatible Technology:	CMOS and TTL

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CIRCLE NO. 98

Rack-Mount Industrial Computer

- *Uses 80386 and optional 80486 module*
- *Has FCC Class A, UL, and CSA approval*

The Selectable Performance rack-mount industrial computer is compatible with the IBM PC/AT. It has a 25-MHz 80386 μP and supports the functions of an 80486 μP. An optional plug-in module contains an 80486 μP running at 25, 33, or 50 MHz. According to the manufacturer, you can install the module in five minutes without changing the existing configuration. The computer comes with a modified Award BIOS that runs the 386 or 486 CPU without modifications. Its features include 1M to 16M bytes of 32-bit memory, support for a numeric coprocessor, two RS-232C ports, one 8-bit and seven 16-bit expansion slots, a parallel-printer port, and a game port. A 16-bit SCSI controller permits data-transfer rates as fast as 10M bytes/sec. The computer meets the requirements for FCC Class A, UL, and CSA approval. $6995.

VGS, 12165 Branford St, Unit Q, Sun Valley, CA 91604. Phone (818) 834-2852. FAX (818) 834-2854.

Circle No. 366

Dual-Port DSP Board

- *Uses 33-MHz TMS320C30 chip for the ISA bus*
- *Provides 512k bytes of static RAM and two RS-232C ports*

The C30 DSP board for the ISA bus uses a 33-MHz TMS320C30 DSP chip and 512k bytes of static RAM (SRAM) that's expandable to 768k bytes. It also has two RS-232C ports, a DSP-Link parallel-expansion interface, and a reserved area for prototyping additional circuitry. A daughter board uses 64k byte dynamic RAMs (DRAMs) to expand the memory to the DSP chip's address capability of 16M words. Bank interleaving achieves one- to three-wait-state access times. Another daughter board contains as much as 1.28M bytes of SRAM with zero-wait-state access time. The memory is divided into five banks of 64k × 32 bits each. C30, $3795; development package with TI's assembler-linker, TI's C compiler, and Spox operating system, $5995; 256k-byte SRAM daughter board, $595; 1M-word DRAM daughter board, $2495.

Spectrum Signal Processing Inc, 3700 Gilmore Way, Suite 301, Burnaby, BC Canada V5G 4M1. Phone (800) 663-8986; in BC, (604) 438-7266. FAX (604) 438-3046.

Circle No. 367

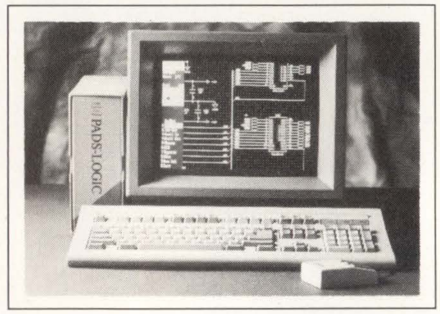
CAE & SOFTWARE DEVELOPMENT TOOLS

Ada Editor And Tool Set For X-Window System

- *Syntax-directed editor assists Ada programming*
- *Direct access to text of Language Reference Manual*

Release 3.0 of the Keyone syntax-directed editor and design tool set runs under the X-Window system and assists in the design, development, and documentation phases of Ada software projects. The editor displays Ada language control structures; access to the text of an integrated Language Reference Manual (LRM) is possible at any time during an editing session. Language templates assist the user in selecting language constructs, and the editor's syntax analysis reduces the number of errors encountered during later compilation. The new release is available under the X-Window system on Hewlett-Packard, Sun, IBM RISC, and DEC workstations, and on IBM PS/2 computers. On Sun workstations, it is also available under Sunview and Openlook. From $900 for PC systems to $18,000 for large DEC VAX networked systems.

Ada Technology Group Inc, 1900 L St NW, Suite 500, Washington, DC 20036. Phone (202) 296-1321. **Circle No. 376**



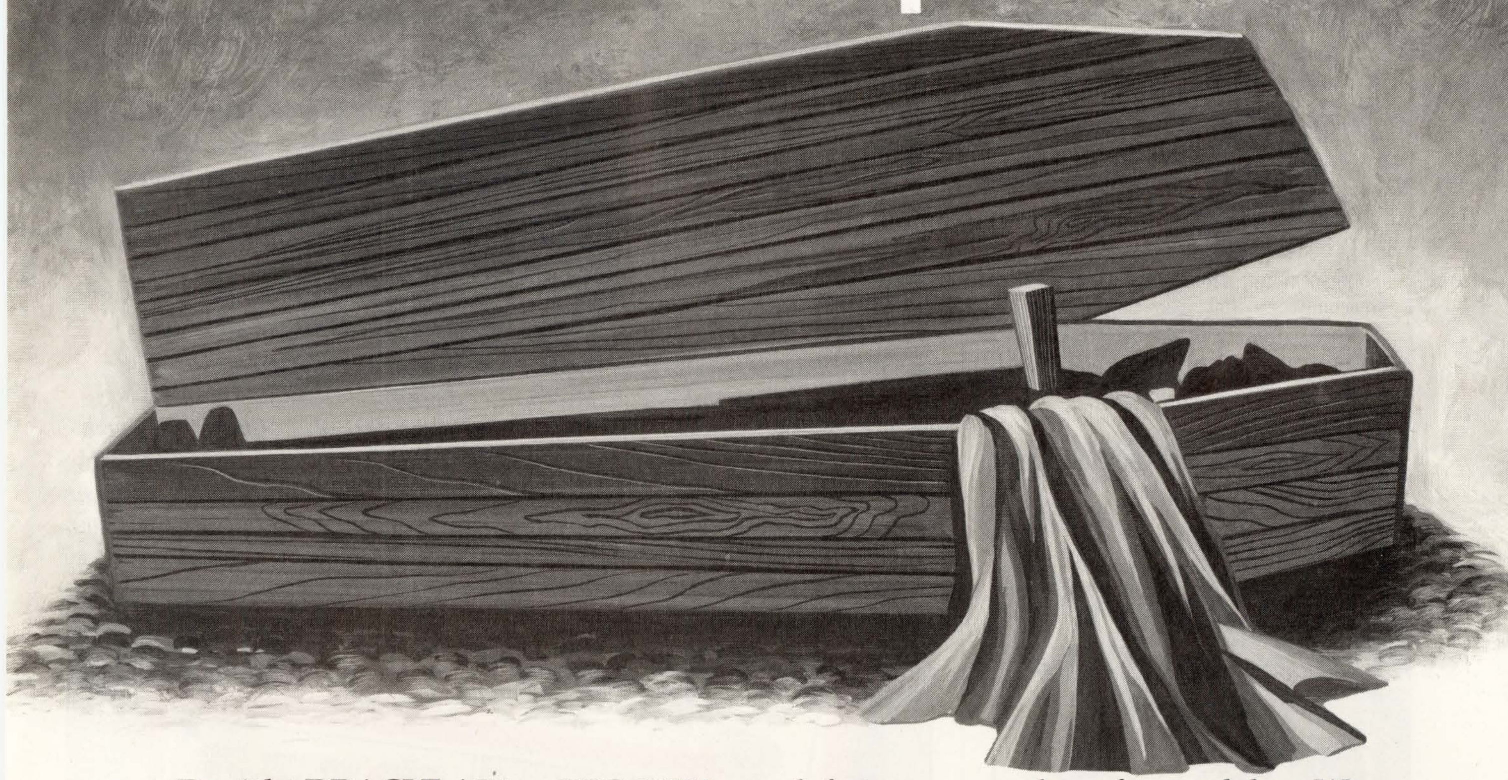
Schematic-Capture Software

- *Runs on PCs*
- *Provides quick access to design information*

Version 2.0 of Pads-Logic schematic-capture software has the advantage of a multisheet database; it holds all design information in memory and it provides the quick response time of a single-sheet database. Enhancements in the new version include library browsing of graphical symbols and parts, a new graphics driver for additional graphics cards (including Metheus and Elsa cards), interfaces to laser printers and Post Script devices, and improved transfer of data to Pspice and Aldec's Susie Simulator. $450.

CAD Software Inc, 119 Russell St, Suite 6, Littleton, MA 01460. Phone (508) 486-9521. FAX (508) 486-8217. **Circle No. 377**

ISS. We've driven a stake through the DRC vampire



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Modeling Software For Mixed-Mode Designs

- *Works with OrCAD/SDT III schematic capture*
- *Allows designing functions in block-diagram form*

OOTM (Object-Oriented Transcendental Modeling) uses Orspice and OrCAD/SDT III to enhance the behavioral-modeling option available with Pspice. You can use it to graphically describe blocks of circuitry; you define block functions and link those definitions to icons. Using the OrCAD netlist, Orspice then matches each icon with the representative circuit netlist to generate a complete simulation file automatically. You can then evaluate your block diagram with the behavioral modeling option in MicroSim's Pspice simulation software by using "Probe" to display or print any voltage or current waveform. After completing your conceptual design, you can substitute actual subcircuits for the conceptual blocks one at a time. The software runs on IBM PCs and compatible computers with floating-point processors. From $2785 for a minimum DOS-only package (OrCAD/SDT III, Pspice/Probe with behavioral-modeling option, Orspice with Basic and OOTMs) to $5540 for OS/2 and DOS/16M versions.

NW Silicon Specialists Inc, 2700 NW 185th Ave, Suite 1200, Portland, OR 97229. Phone (503) 645-8297. **Circle No. 378**

Linker/Compressor For DOS Program Files

- *Shrinks .EXE files as much as 50%*
- *Runs fast and saves disk space*

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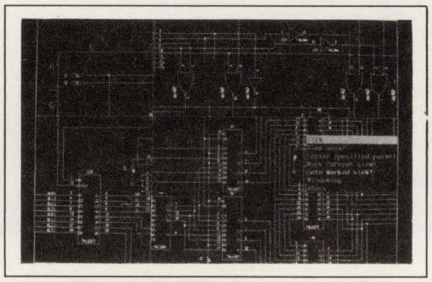
saves as much as 50% of file space. According to the supplier, it runs at least four times faster than Microsoft's Link. Each compressed .EXE file produced by the program contains an embedded decompression routine that requires less than 1k byte of extra memory. When you run the .EXE file, the decompression routine takes control and expands the compressed program back to its original form. Package for new buyers, $250; users' upgrade, $29.95.

SLR Systems, 1622 N Main St, Butler, PA 16001. Phone (412) 282-0864. FAX (412) 282-7965.

Circle No. 379



Schematic Design

- *Front-end schematic-design tools for ASICs, and PLDs*
- *Costs less than $1000*

Capfast, a schematic-design and interface package for Sun workstations, has a hierarchical multipage schematic editor, an on-line electrical rules checker, an interactive simulation grapher, a parts library, an intelligent packager, a symbol-creation editor, and interfaces for Spice, Hilo, Susie, Actel, Xilinx, and popular pc-board design packages. The Sun version is compatible with a PC version, so users can transfer schematics between the two types of computers without modifying their designs. The Sun version runs on all Sun models, color and monochrome, and comes with a year of free support. The package features ASCII file formats and open databases, allowing designers to integrate Capfast tools with their own applications and those of other vendors. It allows designers to create complex schematics for pc-board, PLD, and ASIC designs. Options include EDIF 2 0 0 translators, which allow the translation of complete schematics to workstations from Mentor Graphics, Cadence, and Valid. Other options allow translation to and from the Computervision CADDstation and the Intergraph EDA system. $995.

Phase Three Logic Inc, 1600 NW 167th Pl, Beaverton, OR 97006. Phone (503) 645-0313.

Circle No. 380

Development-Tool Package

- *Allows programming in C for DSP*
- *Provides workstation functions on IBM PC*

A new release of the Intertools software-development package helps embedded-systems designers develop applications for Motorola's DSP96002 on an IBM PC. It includes an optimizing C cross-compiler, a Motorola-compatible macro assembler, utility programs (run-time library routines, formatter, linking-locator, ROM processor, global symbol mapper, symbol list utility and librarian) and XDB, a source-level cross-debugger. This version offers the convenience of programming in C as well as taking advantage of the 96002's unique architecture. The C cross-compiler features optimization techniques that include instruction scheduling and coalescing, lifetime analysis, and C loop construct analysis. The package also provides hand-coding of critical routines through in-line assembler routines or through the use of the Motorola-compatible assembler. Compiler, $1350; assembler, $1100; debugger, $2000.

Intermetrics Microsystems Software Inc, 733 Concord Ave, Cambridge, MA 02138. Phone (800) 356-3594; in MA, (617) 661-0072. FAX (617) 828-2843. **Circle No. 381**

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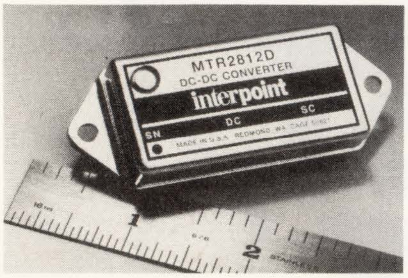

DC/DC Converters

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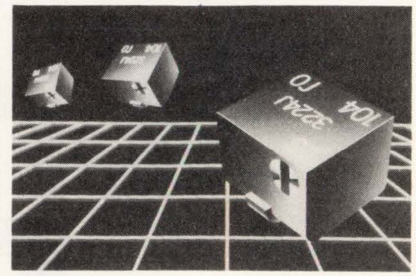
Interpoint Corp, Box 97005, Redmond, WA 98073. Phone (206) 882-3100. FAX (206) 882-1990.

Circle No. 372

Multiturn Trimmers

- *Have a 200-cycle rotational life*
- *Resistance values range to 2 MΩ*

Model 3224 trimmers are 4-mm 11-turn trimmers that are sealed for compatibility with all surface-



mount placement, soldering, and cleaning processes. The units have a rotational life of 200 cycles and are available with resistance values ranging from 10Ω to 2 MΩ. Contact resistance variation equals 1%, temperature coefficient measures 100 ppm/°C, and resistance tolerance equals 10%. Constructed of high-temperature plastic material, the units can be wave or reflow soldered. Also, they will survive cleaning systems that rely on aqueous or semiaqueous high-pressure wash and solvent techniques. The trimmers feature a smooth-top surface and a flush side-adjustment screw. The trimmers are supplied on 12-mm-wide tape; the 7-in. reel has 500 pieces, and the 13-in. reel houses 3000 units. $1.98 (1000). Delivery, eight weeks ARO.

Bourns Inc, 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5071. TLX 676423.

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SIP Sockets

- *Feature solderless termination*
- *Stackable side-to-side*

These SIP sockets feature compliant pins, which permit solderless termination of components to backplanes and pc boards. The socket contacts feature posts that accommodate the standard plated-through-hole tolerance of 0.040 in. The units have a 0.213-in.-high profile and are constructed of high-temperature-tolerant plastic. They feature a 0.025- to 0.03-in. standoff that facilitates board cleaning. The units are available with 6, 8, 10, or 12 positions and are end-to-end and side-to-side stackable. The units are compatible with robotic placement systems. $0.05 to $0.08/contact position.

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752.

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Subminiature Connectors

- *Offer 78-position capacity*
- *Available in plug and receptacle versions*

These high-density D subminiature connectors are available in board- and cable-mount versions. The board-mount units are available in 15-, 26-, 44-, and 62-position receptacles and 78-position plug and receptacle designs. The cable mount line includes a 15-position receptacle, a 62-pin plug, and 78-pin plug and receptacle designs. All units feature 30-μin. gold plating on the contact area. All female contacts are protected by a closed-funnel entry design, which eliminates stubbing during mating. Board-mount units include a lock feature that reduces connector-assembly time. The connectors have a metal front shell and are available with female screw locks or threaded inserts. The connectors come in 15- to 78-position board-mount receptacles. $1.41 to $6.40 (10,000). Delivery, six to eight weeks ARO.

ITT Cannon, Components Div, 1851 Deere Ave, Santa Ana, CA 92705. Phone (714) 261-5300.

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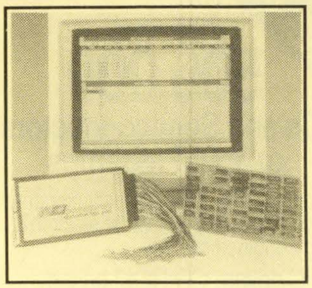

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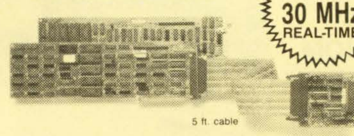

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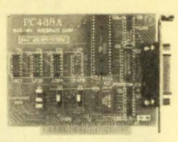

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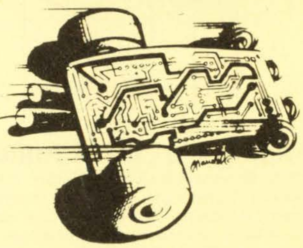

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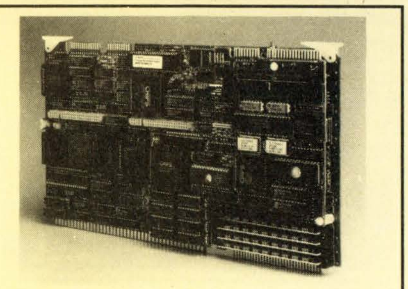

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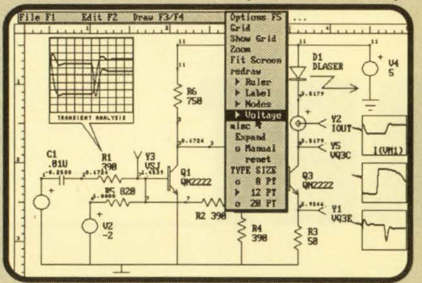

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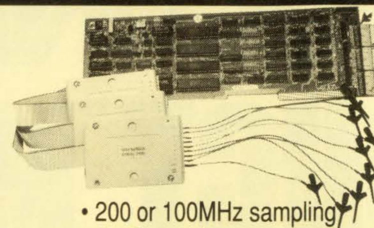

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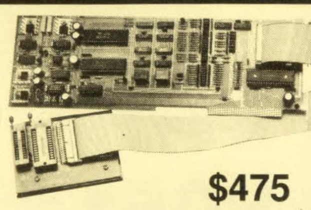

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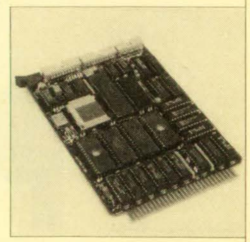

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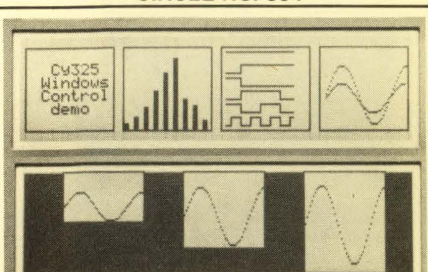

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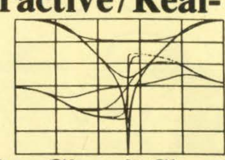

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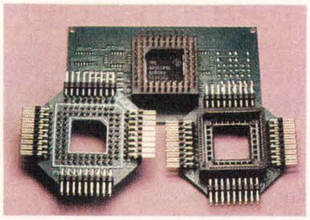

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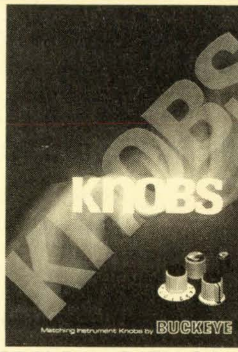

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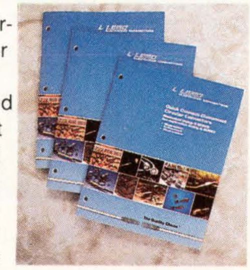

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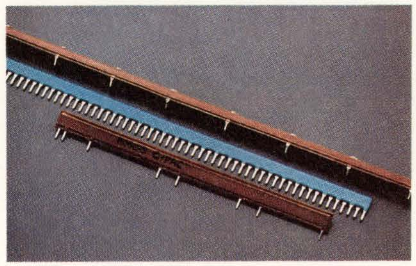

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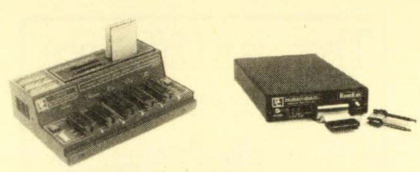

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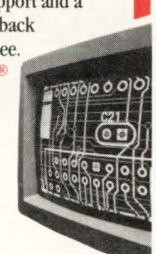

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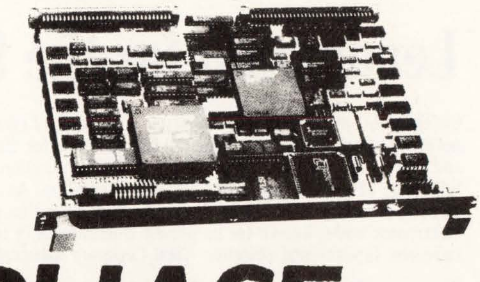

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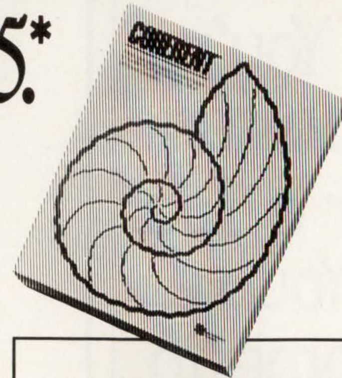

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*Byte Execl benchmark, 1000 iterations on 20 MHZ 386.
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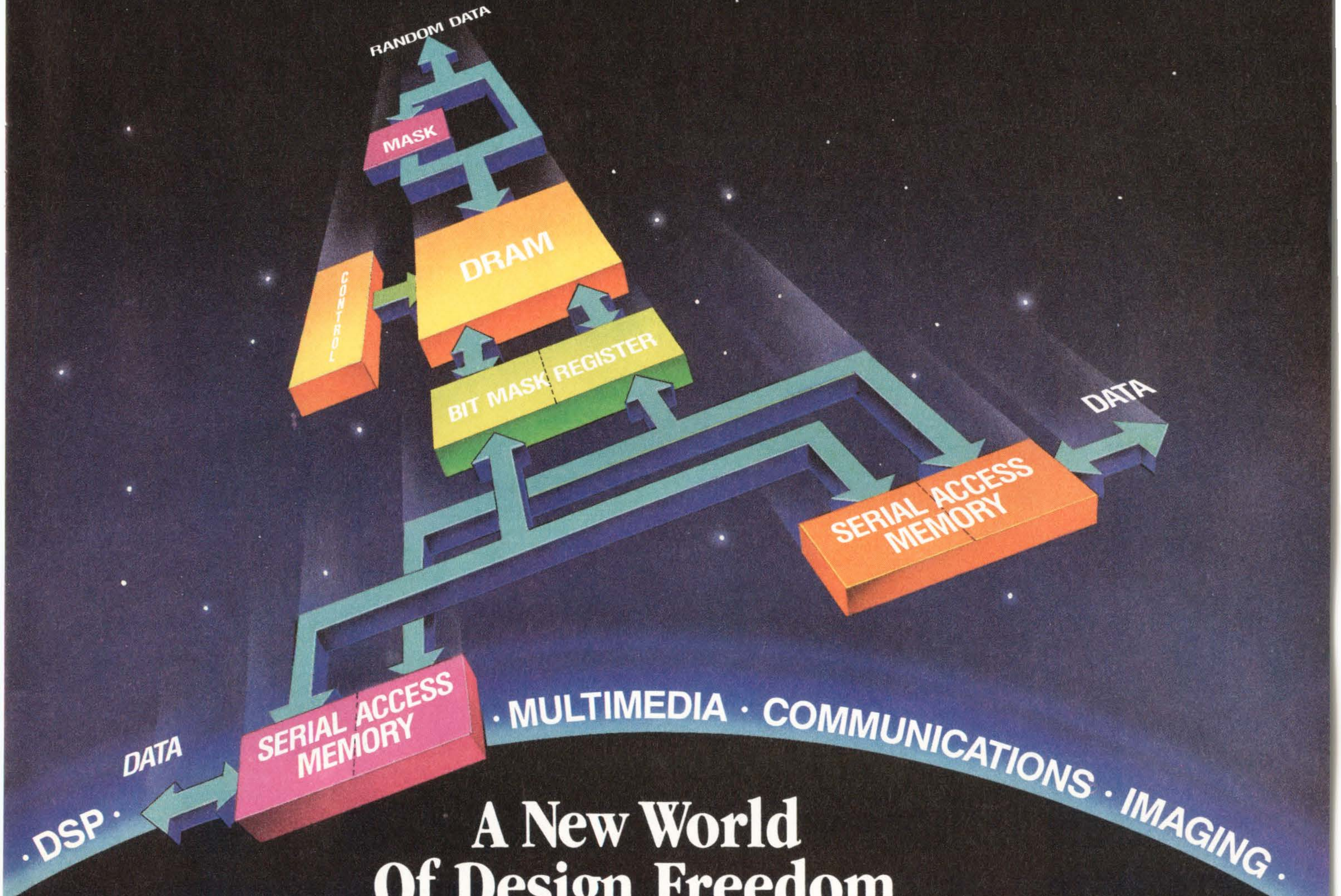

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*Provides SAM stop address input **Call for military availability

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BOOK REVIEW

ISDN from A to Z

The ISDN Sourcebook. 607 pgs; $225. Information Gatekeepers Inc, Boston, MA, 1990.

The Basics Book of ISDN. 48 pgs; Free. Codex Corp, Mansfield, MA, 1990.

ISDN Design: A Practical Approach, by Steve Hardwick. 152 pgs; $34.95. Academic Press, San Diego, CA, 1989.

The ISDN Sourcebook contains plenty of information for both ISDN aficionados and neophytes. Starting from an explanation of what the Integrated Services Digital Network is, the 607-page soft-cover book progresses through a brief description of the international, US governmental, and US nongovernmental organizations involved in specifying or implementing ISDN.

The guide contains a bibliography covering ISDN literature from 1982 to 1988. Also included in the bibliography are references to Bellcore publications; a listing of company, professional-society, and trade-journal special issues on ISDN; and a directory of publications that focus on ISDN.

Another chapter provides insight into the current worldwide status of ISDN. Two chapters enumerate the US companies that implement ISDN and provide a list of mostly US suppliers of ISDN equipment, software, and services. The book also contains a section devoted to ISDN applications. A telecommunications calendar lists events from 1990 to 1998. Not surprisingly, the calendar is heavily weighted toward the present and lists no events for 1995 to 1997. The final 23-pg chapter is a somewhat self-serving description of the numerous ISDN publications of the book's publisher, Information Gatekeepers.

The book concludes with 17 appendices, which include information ranging from a description of US and foreign tariffs and services to user-forum and study-group recommendations. Unfortunately, many of the pages in the appendix are photocopies and, occasionally, are of too poor quality to be of much use.

One item missing from *The ISDN Sourcebook* is a comprehensive glossary. Although short, partial glossaries are included in some of the appendices, the book doesn't contain a thorough dictionary of terms. Otherwise, the publication is a useful, detailed guide to most anything you'd ever want to know about the Integrated Services Digital Network.

The Basics Book of ISDN, which the Codex Corp publishes and distributes free of charge, is a short, light approach to ISDN. The short book—or long pamphlet—explains how you can assess your communications needs and how ISDN might fit into your plans. With the exception of one chapter that discusses ISDN products and equipment, you can even read the text without an ISDN glossary.

Although ISDN texts tend toward the incomprehensible, some clear, understandable design books do exist. One such text is *ISDN Design: A Practical Approach*, by Steve Hardwick. The book is tailored for managers who evaluate the ISDN marketplace. It starts with a mostly acronym-free introduction to ISDN and progresses to cover standards, ISDN terminals, exchanges, and software. With the current emphasis on design for testability, the chapter on testing ISDN systems is timely. The conclusion looks at a company's decision to build ISDN products. This source comes up short, though, in its optimism for the ISDN marketplace. Although ISDN has been the technology of the future for several years now, the book ignores the arguments for and against ISDN's ultimate success.

—Michael C Markowitz

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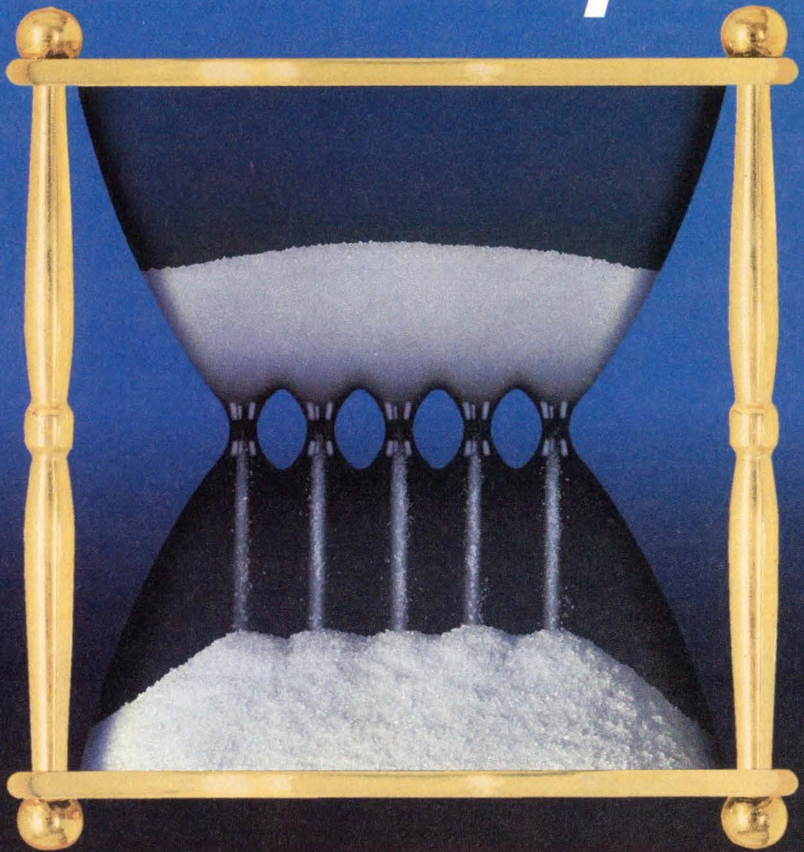

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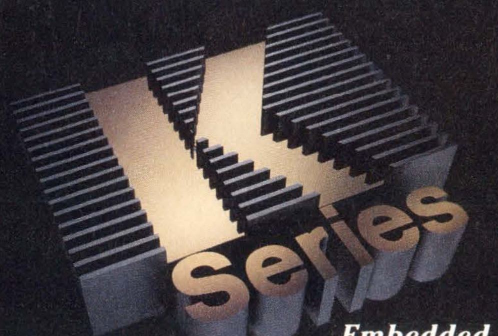

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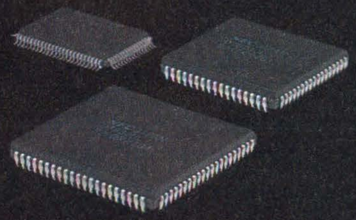

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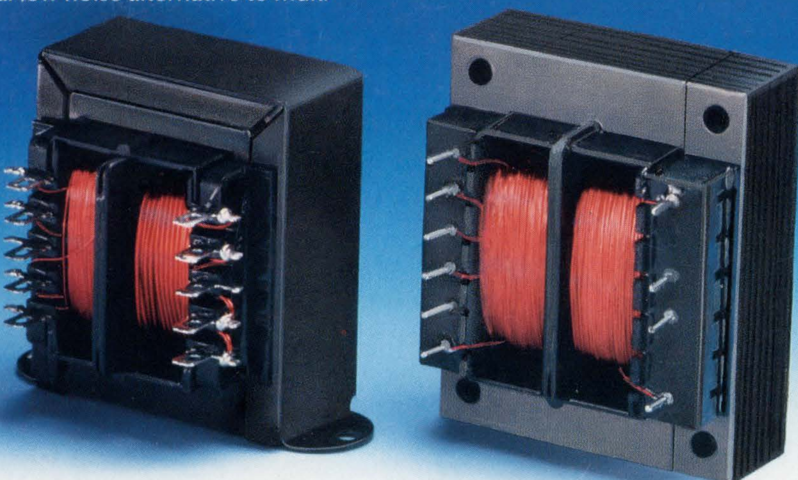
ONE-4-ALL™ TRANSFORMERS FEATURE HIGH ISOLATION FOR TRIPLE OUTPUT REGULATED POWER SUPPLIES IN MICROPROCESSOR APPLICATIONS.

Once again, Signal "The American Original" comes through with a complete line of 50/60 Hz transformers for triple-output regulated supplies. These new **"one-4-all"™** transformers feature the same dual high-temperature bobbin construction and insulating shroud originally developed for the company's very successful International Series. Because they have high isolation and reduced interwinding capacitance characteristics, and require no electrostatic shield, the transformers are an ideal low noise alternative to multi-output switchers. They satisfy UL 506 requirements, and CSA safety and performance standards.

Offered in PC and chassis mount versions, the **"one-4-all"** has dual complementary outputs (± 15 VDC and ± 12 VDC) and additional isolated single output for +5 VDC with in-circuit performance specs.

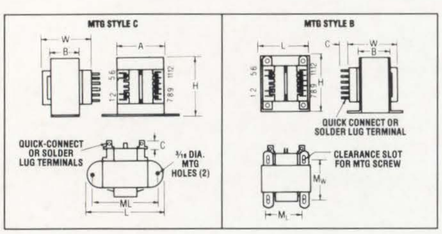
Signal transformers are available through Signal's **PRONTO** 24-Hour Off-the-Shelf shipment program. For additional technical data, contact Signal Transformer, 500 Bayview Avenue, Inwood, N.Y. 11696.

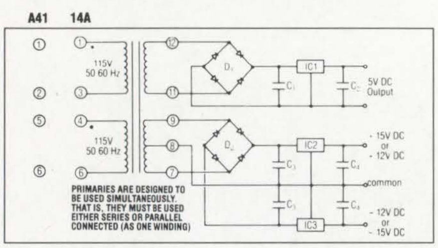
BUY DIRECT
(516) 239-5777
Fax: (516) 239-7208.

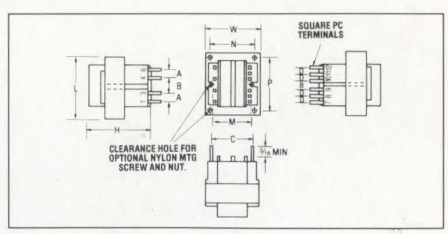


PART NUMBER PRIMARY 50/60 Hz	DC OUTPUT		VA	PRICE
115/230V	Regulator 1	Regulator 2		
A41-25-512	5V @ 1.25A	± 12V @ 150MA	25	16.25
A41-25-515	5V @ 1.25A	± 15V @ 130MA	25	16.25
A41-43-512	5V @ 2A	± 12V @ 300MA	43	20.75
A41-43-515	5V @ 2A	± 15V @ 250MA	43	20.25
A41-80-512	5V @ 3.5A	± 12V @ 600MA	80	28.50
A41-80-515	5V @ 3.5A	± 15V @ 500MA	80	28.50

PART NUMBER PRIMARY 50/60 Hz	DC OUTPUT		VA	PRICE
115/230V	Regulator 1	Regulator 2		
14A-20-512	5V @ 750MA	± 12V @ 200MA	20	15.00
14A-20-515	5V @ 750MA	± 15V @ 175MA	20	15.00
14A-30-512	5V @ 1.25A	± 12V @ 250MA	30	17.75
14A-30-515	5V @ 1.25A	± 15V @ 200MA	30	17.25
14A-56-512	5V @ 3A	± 12V @ 300MA	56	21.00
14A-56-515	5V @ 3A	± 15V @ 250MA	56	21.00







Dimensions								Mtg.	Mtg.		Mtg.	
VA	L	W	H	A	B	C	Terminals	Style	ML	MW	Screw	Lbs.
25	2 13/16	1 7/8	2 5/16	2	1 1/8	5/16	3/16 (.187)	C	2 3/8	–	#6	1.25
43	3 1/8	2 1/16	2 11/16	2 1/4	1 1/8	5/16	3/16 (.187)	C	2 13/16	–	#6	1.6
80	2 1/2	2 3/8	3	–	1 3/8	5/16	3/16 (.187)	B	2	2 3/16	#6	2.8

Dimensions								Pin	Mtg.			Mtg. Screw		
VA	L	W	H	A	B	C	D	Dimensions	M	N	P	Size	Quantity	Lbs.
20.0	2 1/4	1 7/8	1 5/8	.400	.400	1.460	.200	0.038SQ	1 1/2	–	–	#4	2	0.90
30.0	2 5/8	2 3/16	1 9/16	.550	.275	1.680	.275	0.045SQ	–	1 3/4	2 3/16	#6	4	1.15
56.0	3	2 1/2	1 13/16	.600	.300	1.900	.300	0.045SQ	–	2	2 1/2	#6	4	1.70

signal TRANSFORMER

The American Original.™

CIRCLE NO. 44