A CAHNERS PUBLICATION

MAY 26, 1988

# EDN®

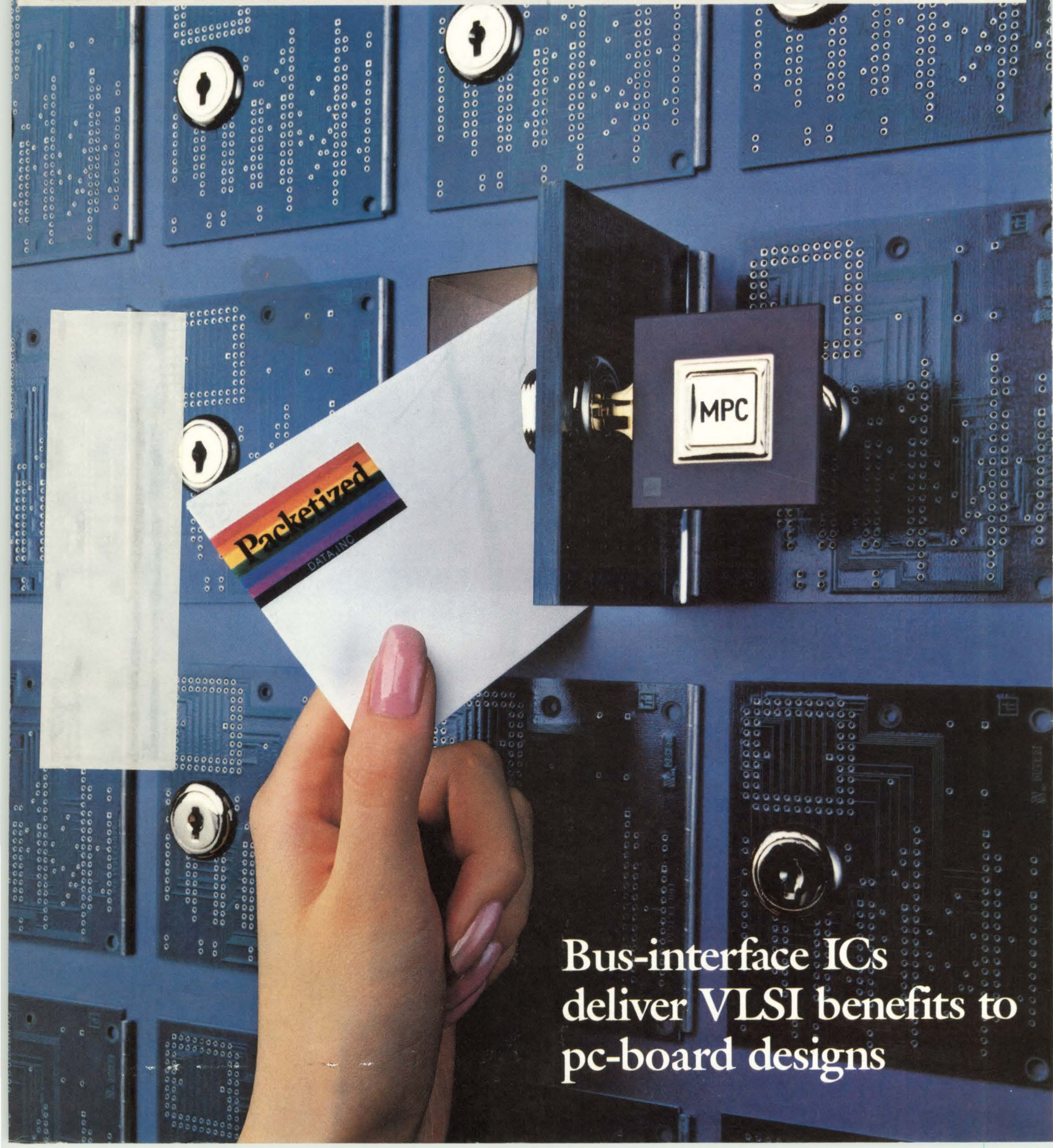
Designer's Guide to state machines—Part 1

Designer's Guide to noise analysis—Part 2

Software function libraries

Uniting ultrasonics and microelectronics

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS




## Bus-interface ICs deliver VLSI benefits to pc-board designs

# Devices' 29K. platform.



**CIRCLE NO 175**

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## *absorptive... reflective*


### dc to 4.6 GHz *from* $32.95 (1-24)

Tough enough to pass stringent MIL-STD-883 tests, useable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

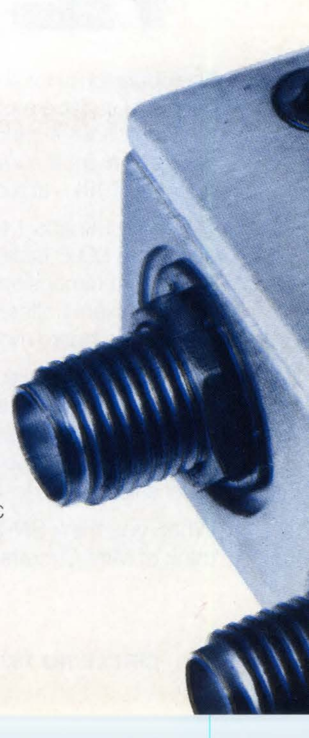
Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

***Switch fast... to Mini-Circuits' GaAs switches.***

SPECIFICATIONS

| Pin Model | **KSW-2-46** | | **KSWA-2-46** | |
|---|---|---|---|---|
| Connector Version | **ZFSW-2-46** | | **ZFSWA-2-46** | |
| FREQ. RANGE | dc-4.6 GHz | | dc-4.6 GHz | |
| INSERT. LOSS (db) | typ | max | typ | max |
| dc-200MHz | 0.9 | 1.1 | 0.8 | 1.1 |
| 200-1000MHz | 1.0 | 1.3 | 0.9 | 1.3 |
| 1-4.6GHz | 1.3 | 1.7 | 1.5 | 2.6 |
| ISOLATION (dB) | typ | min | typ | min |
| dc-200MHz | 60 | 50 | 60 | 50 |
| 200-1000MHz | 45 | 40 | 50 | 40 |
| 1-4.6GHz | 30 | 23 | 30 | 25 |
| VSWR (typ) ON | 1.3:1 | | 1.3 | |
| OFF | — | | 1.4 | |
| SW. SPEED (nsec) rise or fall time | 2(typ) | | 3(typ) | |
| MAX RF INPUT (bBm) | | | | |
| up to 500MHz | +17 | | +17 | |
| above 500MHz | +27 | | +27 | |
| CONTROL VOLT. | **-5V** on, OV off | | **-5V** on, OV off | |
| OPER/STOR TEMP. | -55° to +125°C | | -55° to +125°C | |
| **PRICE** (1-24) | **$32.95** **$72.95** | | **$48.95** **$88.95** | |



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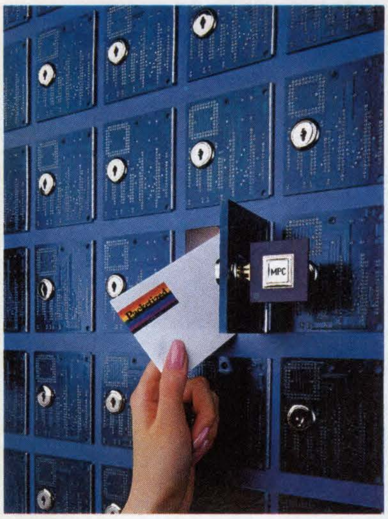
**CIRCLE NO 184**

Volume 33, Number 11

# EDN

May 26, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



***On the cover:** Bus-interface chips open up pc-board real estate, allowing you to incorporate extra features and functions. See pg 122. (Photo courtesy Intel Corp)*

## DESIGN FEATURES



*Continued on page 7*

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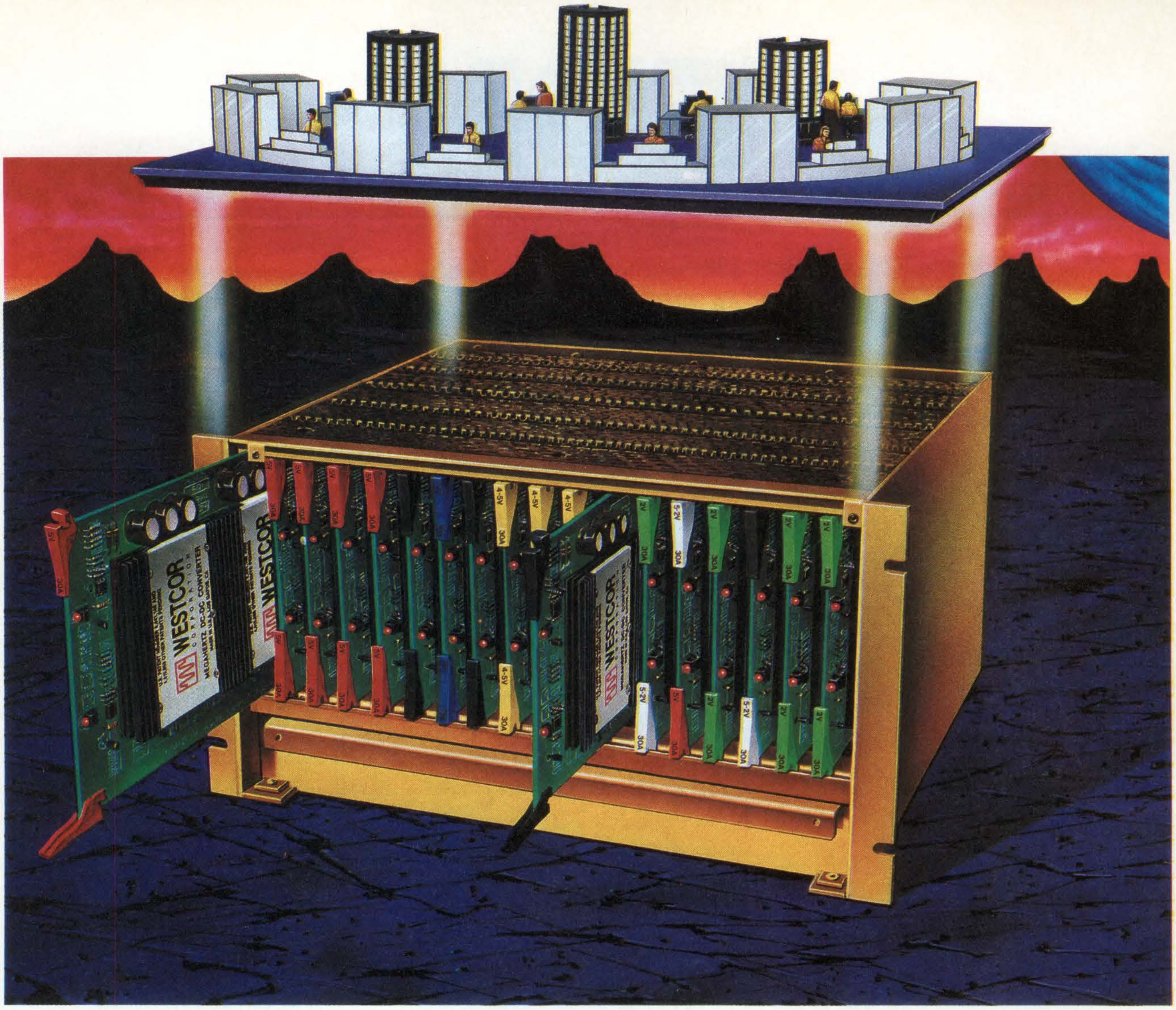


# A NEW WORLD OF HIGH POWER FLEXIBILITY

Westcor's PowerCage™ and PowerCards™ comprise a modular power supply system of galactic power (7200 watts max.), flexibility (36 outputs max.) and efficiency (80% typ.). More like an expandable computer mainframe in design and concept than a standard high power supply, the PowerCage offers space-age alternatives to users of outdated 5x8x11 inch box switchers.

Measuring 19x10.5x11.25 inches deep the PowerCage fits into a standard NEMA rack and powers 18 slots for single or dual output PowerCards or dummy cards. PowerCage backplanes provide connections for easy configuration by the user.

Low profile (.8″) PowerCards supply single outputs from 2 to 75 VDC at up to 400 watts (outputs from 2 to 5 VDC limited to 60 amperes). Dual output cards source two isolated outputs each at half of the above ratings. Single output cards can be paralleled with current sharing to provide kilowatts via simple backplane configuration.

The nucleus of each PowerCage system is Westcor's patented 1 MHz, high power density, high reliability converter. Consider these benefits and features: 208 VAC 3 phase input; remote/local sense on all outputs; TTL power good signal and status LED's; designed to meet UL, CSA and VDE safety requirements; TTL inhibit; over-temperature, over-current, over-voltage protection; "hot" card insertion; full power at 50°C.

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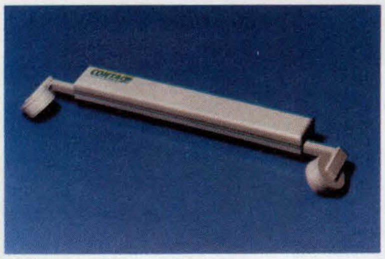
CIRCLE NO 182

*Continued from page 5*





***Ultrasonic ranging systems** suit applications that require the sensing of relatively large objects over great distances (pg 61).*

## TECHNOLOGY UPDATE



## PRODUCT UPDATE



## DESIGN IDEAS



*Continued on page 9*

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

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*Continued from page 7*

EDN

May 26, 1988



## EDITORIAL 

Some electronic companies take the sue-the-bastards attitude. Unfortunately, it seems to be spreading.

## NEW PRODUCTS



## PROFESSIONAL ISSUES 

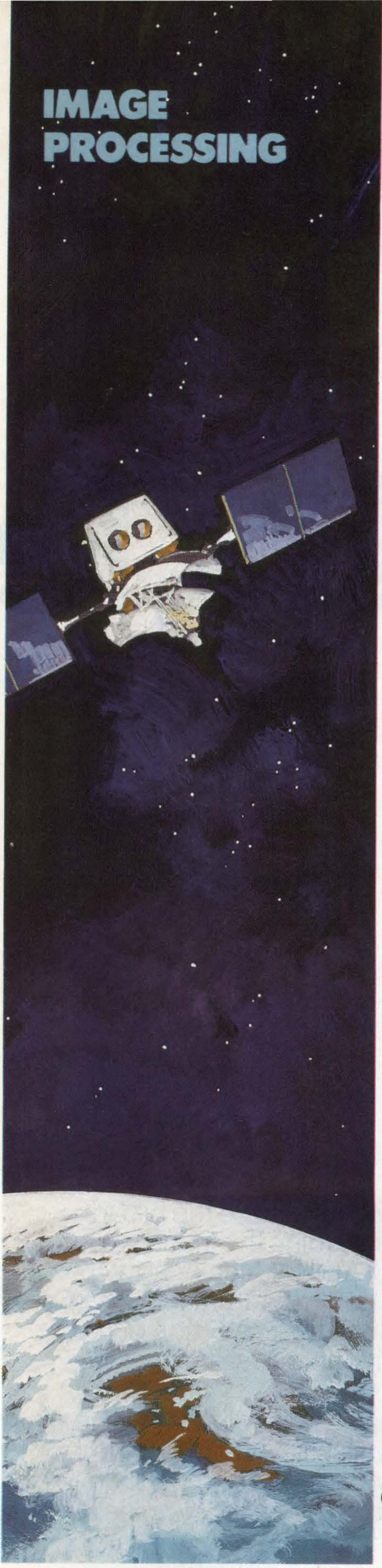
Differential equations and Shakespeare: Melding engineering studies and liberal arts.—*Deborah Asbrand, Associate Editor*

## LOOKING AHEAD 

Worldwide GaAs IC market expands at robust pace. . .Continuous industries falter in MAP plans.

## DEPARTMENTS


# SIGNALLING A NEW ERA




IN DSP.

# THE IMS A100 CASCADEABLE SIGNAL PROCESSOR

Using pulse compression to improve range resolution, a modern radar system compares signals transmitted to and reflected from a target.

A typical system may use a pattern 512 samples long, collected at a data rate of 2.5 MHz.

This requires more than a billion multiplications a second!

Yet the INMOS A100 Cascadeable Signal Processor enables a pulse compressor with this capability to fit a circuit board half the size of a typical PC card and dissipates less than 30 Watts.

A combination of performance, low power dissipation and reduced board area that means significant reductions in systems costs. Equally impressive results are found in applications such as beamforming, filtering and image processing.

Whatever DSP area you are in the INMOS IMS A100 processor is the only serious contender.

The following features show why the IMS A100 signals a whole new era in DSP. If you would like more information, clip the coupon today.

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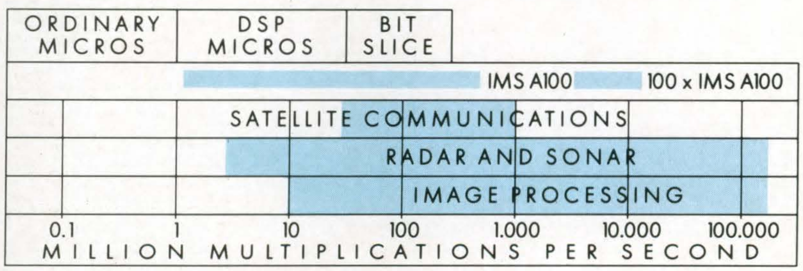
- Block floating point support
- Complex number support
- Easy to control from most ordinary and DSP microprocessors
- Data throughput to 10 MHz
- Power dissipation 1.5 Watts
- Fully static CMOS implementation
- 84 pin Ceramic PGA and Cerquad Packages
- MIL-STD-883C processing available

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Software Planning Manager

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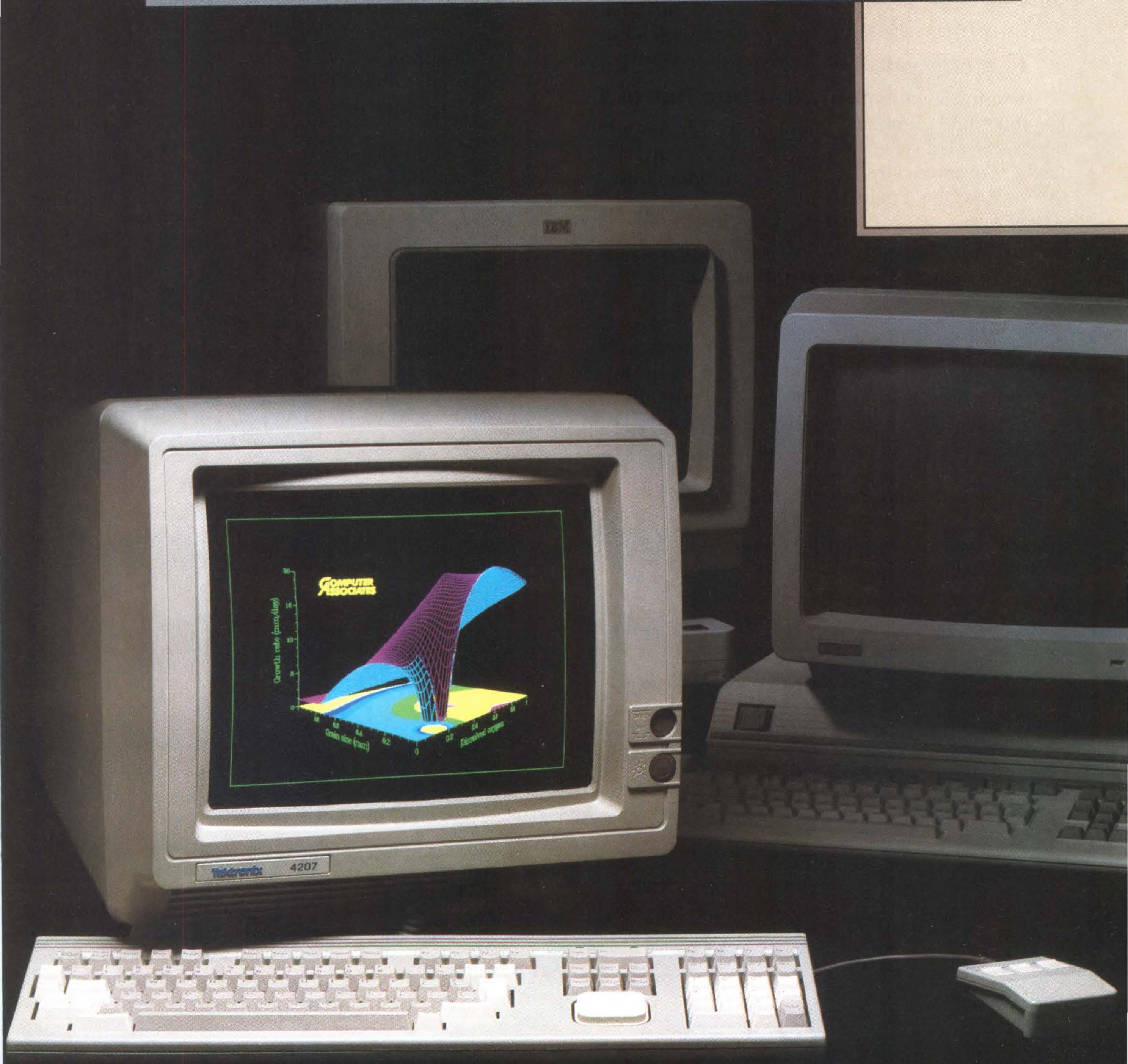
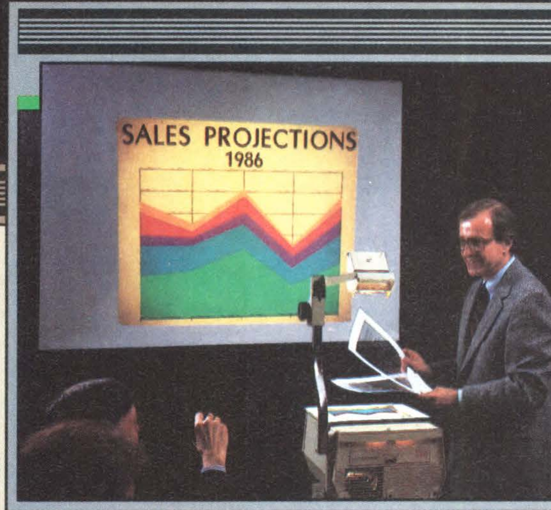
**CIRCLE NO 178**

## TEK 4200 SERIES TERMINALS

# WHY TEK BUILDS A BETTER GRAPHICS TERMINAL FOR IBM AND DEC THAN IBM AND DEC.



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Only the 4200 Series delivers interactive true zoom and pan with the other superb graphic and alphanumeric features made famous by Tektronix.

**Tek Software and peripheral compatibility is without equal in the graphics industry.** The 4200 Series is supported by more than 175 world-class software vendors offering a full range of solutions for MIS, manufacturing and engineering.

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4200 Series are immediately available from authorized distributors or by contacting your local Tektronix representative. For information: **call 1-800-225-5434.** In Oregon, 1-235-7202.

**Comparison of Graphics Terminals**

| | TEK | DEC | IBM |
|---|---|---|---|
| DEC Host Compatible | Yes | Yes | No |
| IBM Host Compatible | Yes | No | Yes |
| Multiple Active Sessions | Yes | Yes | No |
| Tek 4010-4100 Command Set | Yes | No | No |
| Segments | Yes | No | No |
| True Zoom and Pan | Yes | No | No |
| IBM GDDM (Graphical Data Display Manager) Support | Yes | No | Yes |
| Graphics Addressability of 4096 × 4096 | Yes | No | No |
| VT200 Alphanumerics | Yes | Yes | No |
| Background Hardcopy | Yes | No | No |
| Separate Graphics and Alphanumeric Regions | Yes | No | Yes |

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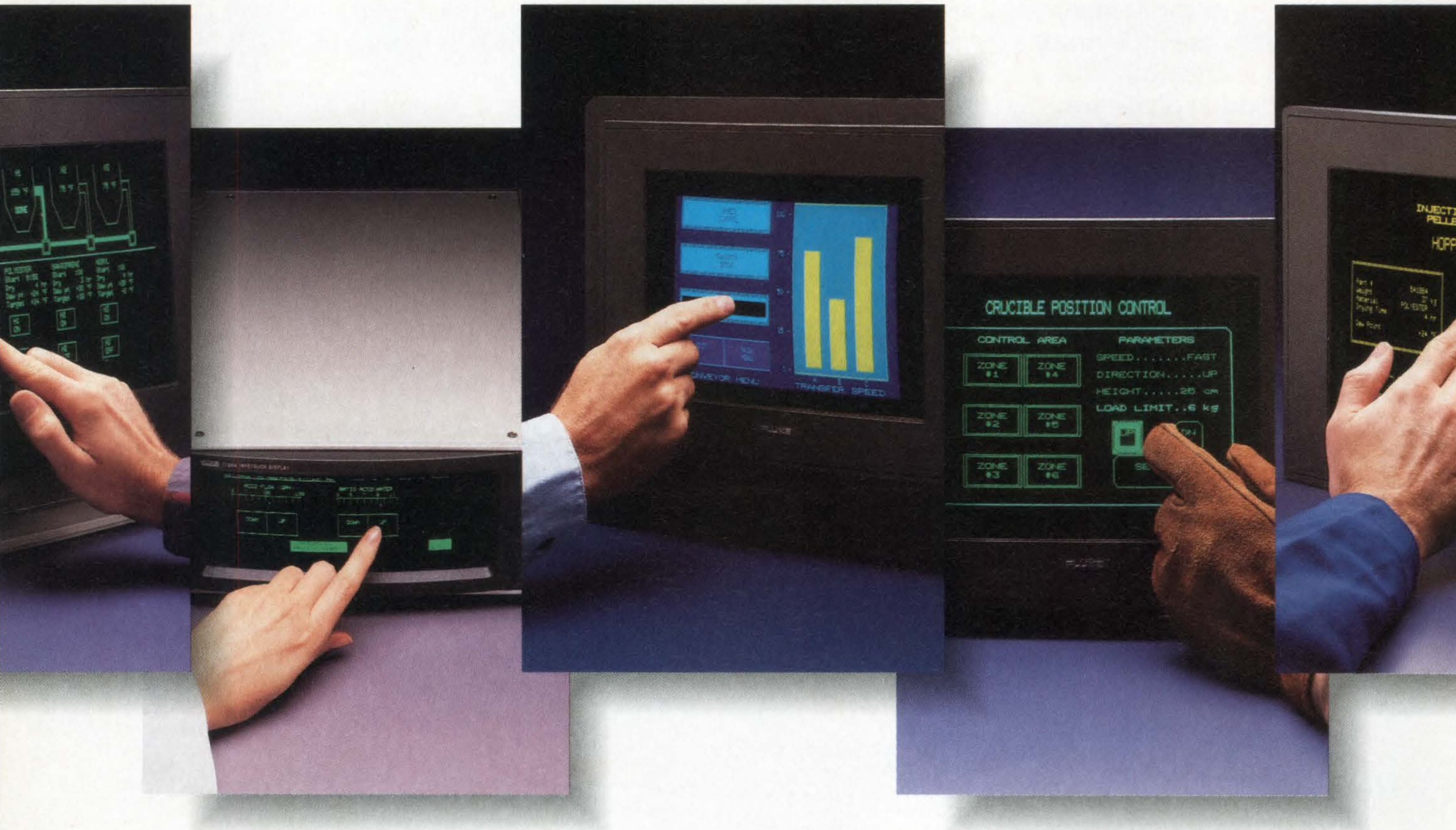


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# NEWS BREAKS

EDITED BY JOANNE CLAY

## FIVE COMPANIES PARTICIPATE IN ARCNET DEMONSTRATION

Visitors to the Control Expo '88 show in Chicago, IL (June 7 to 9, 1988) will be able to witness a practical demonstration of the Arcnet network's ability to interface a range of dissimilar hardware and software systems. Five companies—Contemporary Control Systems Inc (Downers Grove, IL, (312) 963-7070), Comendec Ltd (Birmingham, UK, TLX 33435), Matrix Corp (Raleigh, NC, (919) 833-2000), Xycom Inc (Saline, MI, (313) 429-4971), and Ziatech Corp (San Luis Obispo, CA, (805) 541-0488)—will link their equipment via an Arcnet network. The networked equipment will include STD Bus systems running MS-DOS and VME Bus systems running MS-DOS and OS9/68k, all of which will operate as process controllers. In response to requests from these process controllers, a VAX/VMS computer will download data to them over the network.—Peter Harold

## CMOS ARITHMETIC LOGIC UNIT OPERATES IN 26 NSEC

If you're designing pipeline signal-processing circuitry, you may want to consider the L4C381 arithmetic logic unit (ALU) from Logic Devices (Sunnyvale, CA, (408) 720-8630). This device offers 10 arithmetic and logical functions on two 16-bit inputs. The ALU offers add, subtract, negate, and accumulate functions, which it completes within 26 nsec. Both the inputs and the output have 16-bit registers that can be used or individually bypassed. You can cascade the devices for calculations that use more than 16 bits. The ALU comes in a 68-pin, plastic leaded chip carrier (PLCC). The 26-nsec version costs $24 (1000).—Richard A Quinnell

## PATENT GRANTED FOR SERIAL/PARALLEL ONBOARD TEST TECHNIQUE

The US Patent Office has granted a patent (number 4,720,672) to Logical Solutions Technology Inc (Campbell, CA, (408) 374-3650, TLX 172867) for its serial/parallel testability system. The company claims that this test technique, which it offers in the form of testability chips and technology licenses, adds only 1% to the amount of circuitry on a pc board. Contributing to this low overhead figure is the fact that the company's testability chips can replace more-conventional shift registers, multiplexers, and decoders while adding testability to the board.—Steven H Leibson

## CONFIGURABLE μC FAMILY INCLUDES EMULATOR

You can customize the TMS370 family of 8-bit μCs from Texas Instruments (Dallas, TX, (800) 232-3200, ext 700) by choosing the peripherals you want on chip. The company will initially offer six standard components that meet most customers' needs. Because of the family's modularity, you can configure an emulator to emulate any of the possible combinations of standard components that can be placed on chip. The list of components, which is expected to grow, includes EEPROM, ROM, RAM, serial I/O ports, timers, and 8-bit A/D converters. The price of the μCs ranges from $3 to $10 in production quantities.—David Shear

## GRAPHICS CHIP COMBINES FUNCTIONS OF TWO EARLIER PARTS

Because it combines the functions of two earlier parts, the HD63487 Memory Interface and Video Attribute Controller (MIVAC) from Hitachi America (San Jose, CA, (408) 435-8300) may help you shrink your graphics-system design. The MIVAC has a 33-MHz pixel rate and a 1M-byte memory space. You can program it for a variety of display modes, such as a monochrome, 640×480-pixel mode or a color, 16-bit, 640×400-pixel mode. The device comes in a 68-pin PLCC and costs $25 (5000); it will be available in production quantities in the third quarter of 1988.—Richard A Quinnell

# NEWS BREAKS

## HALF-HEIGHT, 5¼-IN. DRIVE STORES 71M BYTES

Model 3085 is a half-height, 5¼-in., hard-disk drive from Miniscribe (Longmont, CO, (303) 651-6000) that stores 71.3M bytes and features a 22-msec average access time. A rotary voice-coil actuator and a closed-loop servopositioning feature give the drive its fast access time and 1100-tpi track density. The drive incorporates a standard ST412 disk-drive interface and costs less than $700 (1000).—Steven H Leibson

## LOGIC SYNTHESIS AND TTL LIBRARY FOR PGAs

You can now use standard TTL functions to design a programmable gate array (PGA) without paying a gate penalty. Xilinx (San Jose, CA, (408) 559-7778) offers automated-design-implementation software with a library of 40 TTL functions. This supplement to the Xact development system allows you to design a combination of TTL functions and PLDs, then strips out unused logic to conserve gate usage. The $1500 software package also converts schematic net lists and PLD equations to a PGA net list and provides automatic placement and routing. The TTL library is priced separately at $500.—Richard A Quinnell

## PLOTTERS GUARD DATA AGAINST ELECTRONIC EAVESDROPPERS

If your designs must remain secret, consider using the Tempest Draftmaster I and II E-size plotters from Hewlett-Packard Co (Palo Alto, CA, phone local office). The plotters meet Tempest NACSIM 5100A electronic-security standards and are listed on the US Government's preferred-products list. The single-sheet HP 7595A-T and roll-fed HP 7596A-T Tempest Draftmaster plotters are essentially electromagnetically hardened versions of the company's 7585B and 7586B plotters. They cost $14,900 and $16,900, respectively.—Steven H Leibson

## DIGITAL SAMPLING OSCILLOSCOPE OFFERS 2-GHz BANDWIDTH

The PM3340 2-GHz sequential-sampling digital oscilloscope from Philips (Eindhoven, The Netherlands, TLX 35000; in the US: John Fluke Mfg Co Inc, Everett, WA, (206) 347-6100) gives you 10-bit resolution and a 512-point record length. This oscilloscope has all the measurement features normally found on a digital storage oscilloscope; for example, it has voltage and time cursors, automatic measurements, and waveform math. The PM3340 also has some useful but less-common features. An "eye pattern" display mode allows you to examine digital communication signals. The voltage-histogram display mode shows the distribution of amplitude probabilities over a selected time interval. The scope's fast Fourier transform (FFT) function lets you examine signals in the frequency domain. The PM3340 includes both IEEE-488 and RS-232C interfaces and costs $16,000.—Doug Conner

## 1.5-μm ANALOG-CELL FAMILY COEXISTS WITH DIGITAL CIRCUITS

NCR Microelectronics Div (Fort Collins, CO, (800) 334-5454) will add a family of analog cells to its VS1500 1.5-μm CMOS ASIC-cell library in July. These analog functions include an op amp, a comparator, a bandgap voltage reference, two analog switches, an ECL input buffer, matched resistor blocks, and analog input and output pads. The company has already added these analog cells to its VS2000 2-μm cell library. Earlier this year, the company introduced a family of high-speed digital cells to the VS1500 library; the family includes 48-mA output drivers, Schmitt-trigger input buffers, and flip-flops that can attain 140-MHz toggle rates.—Steven H Leibson

## PHONE-SET IC FEATURES DYNAMIC AUDIO GAIN LIMITING

In addition to performing all the speech and line-interface functions required in telephone sets, the TEA1064 IC from Philips Components Div (Eindhoven, The Netherlands, TLX 51573) features dynamic gain limiting in its microphone channel. As a result, the audio signal transmitted to the telephone line remains relatively free of distortion, irrespective of the loudness of the phone user's voice. You can use it with dynamic, magnetic, piezoelectric, or electret microphones, and it provides a single-ended or differential drive for a variety of earpieces. It can operate from phone-line voltages as low as 1.7V, and it includes a 3-mA supply output for peripheral circuits such as dialers, microcontrollers, and displays. The device meets the performance requirements of all the major PTTs (post, telephone, and telecommunications authorities) in Europe, the USA, and the Far East. The IC is available in a 20-pin DIP or surface-mounting mini-pack; it costs around gld 3 in high volume.—Peter Harold

## VISIBLE-LIGHT LASER DIODE EMITS 3 mW AT 680 NM

Targeting the replacement of bulky HeNe gas lasers, the NDL3200 semiconductor laser from NEC Corp (Tokyo, Japan) and its US affiliate, NEC Electronics Inc (Mountain View, CA), emits more than 3 mW of visible energy with a 680-nm wavelength at room temperature. The laser will sell for $500 in the US. Unlike the larger gas lasers, this device is packaged in a petite, 9-mm can. It consumes far less power than a gas laser does: It runs on 100 mA at 2.2V. The company claims that the 680-nm light is 1000 times more visible to the human eye than competing 780-nm semiconductor lasers. The firm also asserts that the shorter wavelength will allow optical-disk manufacturers to achieve smaller spot sizes; let printer, facsimile, and copier vendors increase product speeds; and permit fiber-optic sensors to achieve greater sensitivities.—Steven H Leibson

## ANALOG / DIGITAL ASIC MERGES STANDARD CELLS AND ARRAYS

The Expert Array from Mietec (Oudenaarde, Belgium, TLX 85739) allows you to subdivide a mixed analog/digital ASIC into sections that are implemented with standard cells and sections that are implemented with mask-programmable arrays of analog components and logic gates. Both the standard-cell and the array sections are integrated on the same silicon die with the company's 40V SBIMOS technology. You can use the technique to produce standard-function parts that you can modify for different applications—for example, telephone ICs that you can adapt to different international standards. Alternatively, you can use the technique to accelerate the prototyping phase of a custom design by implementing well-defined circuitry with standard cells, and using arrays to implement any circuitry that may require redesign. The initial nonrecurring engineering (NRE) charges for the Expert Array are similar to those for normal standard-cell designs.—Peter Harold

## AMERICAN FIRM LICENSES EUROPEAN VERSION OF MULTIBUS I

Micro Industries (Westerville, OH) has licensed the Advanced Multibus System (AMS) line of boards from Siemens AG (Munich, West Germany) for manufacture and distribution in the US. The AMS boards support Intel's Multibus I electrical specification but do not use that standard's card format or connector system. The double-Eurocard-size AMS boards use DIN pin-and-socket connectors instead of the edge connectors employed by Multibus I cards. US prices for AMS cards range from $500 for digital I/O boards to $7500 for an 80386-based CPU card.—Steven H Leibson

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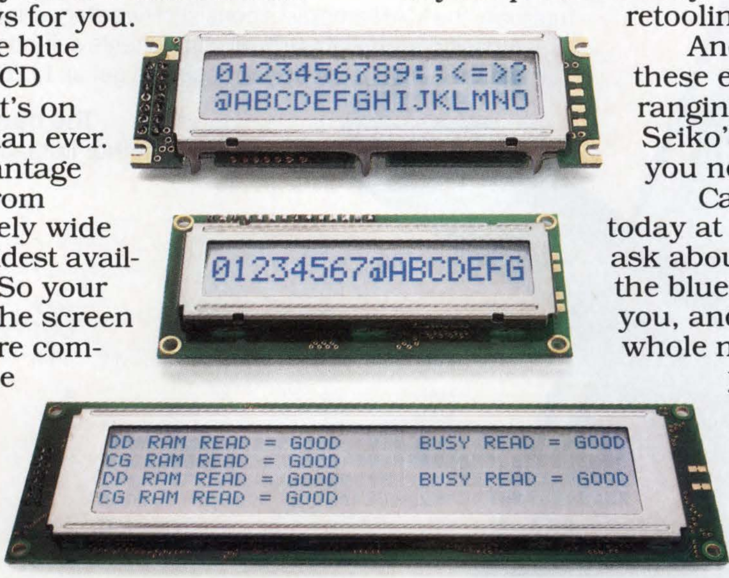


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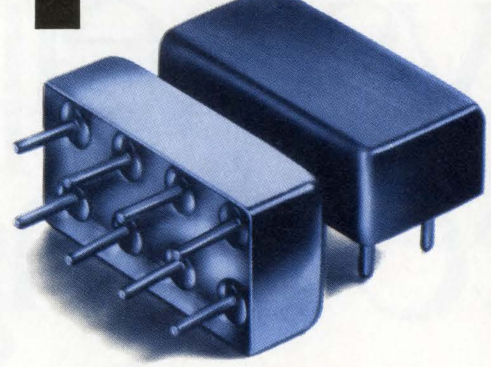

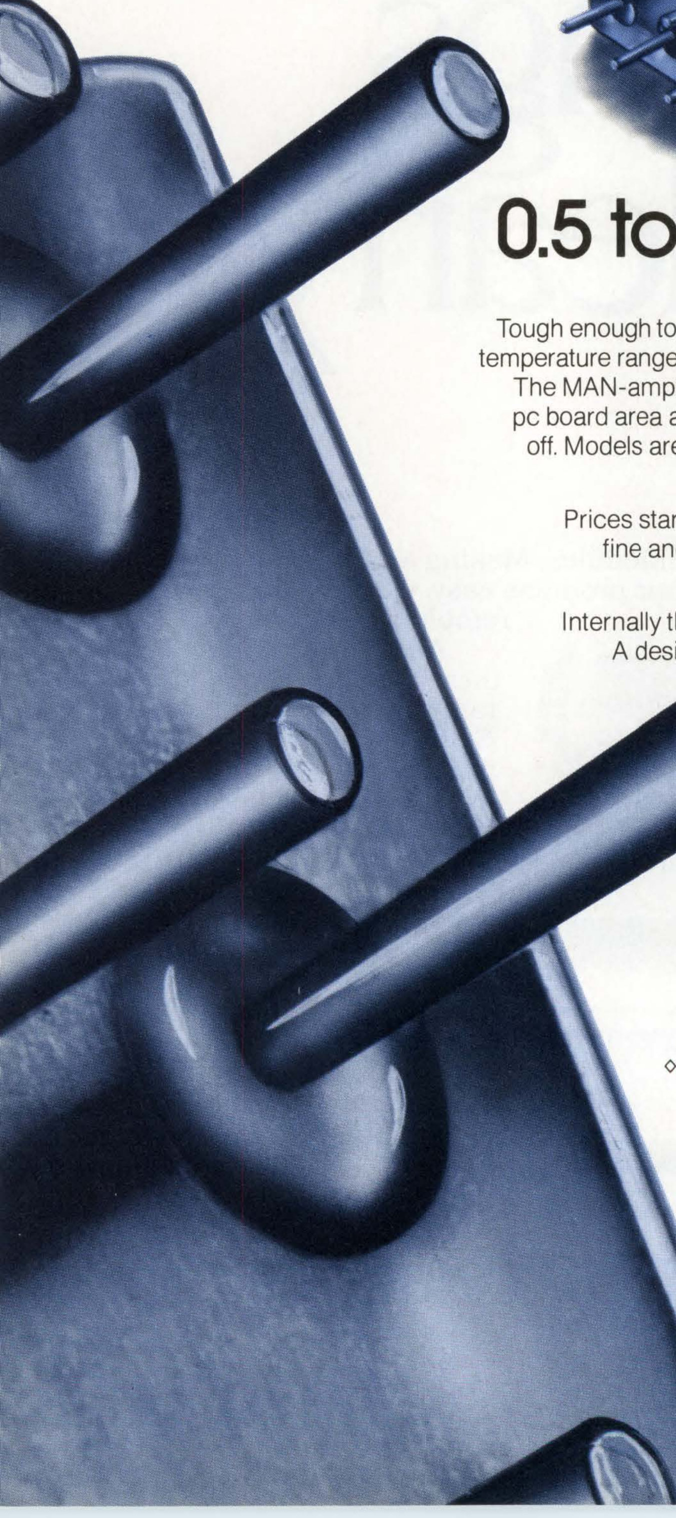

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|---|---|---|---|---|---|---|---|
| MAN-1 | 0.5-500 | 28 | 1.0 | 8 | 4.5 | 60 | 13.95 |
| MAN-2 | 0.5-1000 | 19 | 1.5 | 7 | 6.0 | 85 | 15.95 |
| MAN-1LN | 0.5-500 | 28 | 1.0 | 8 | 2.8 | 60 | 15.95 |
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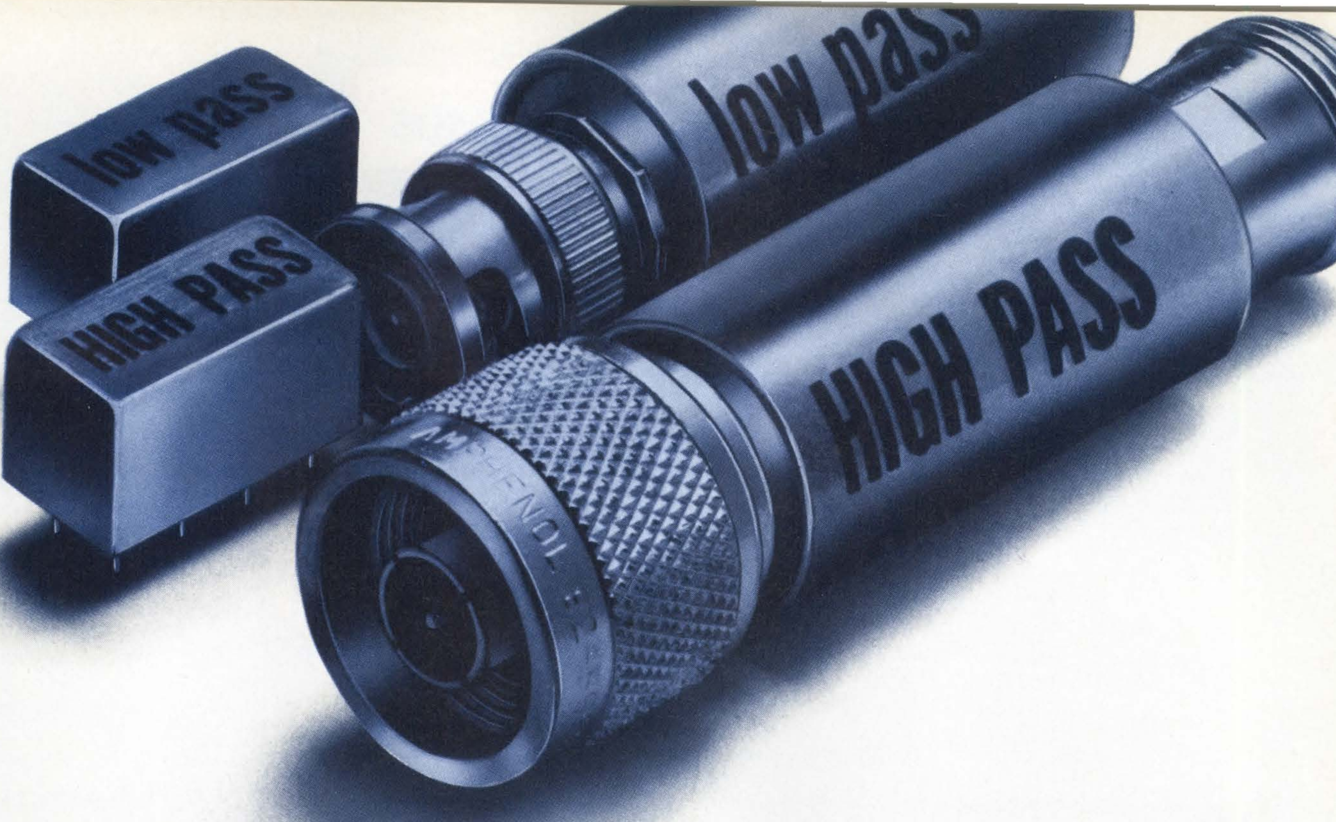
**CIRCLE NO 160**

C118 REV. B

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| LOW PASS Model *LP- | 10.7 | 21.4 | 30 | 50 | 70 | 100 | 150 | 200 | 300 | 450 | 550 | 600 | 750 | 850 | 1000 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min. Pass Band (MHz) DC to | 10.7 | 22 | 32 | 48 | 60 | 98 | 140 | 190 | 270 | 400 | 520 | 580 | 700 | 780 | 900 |
| Max, 20dB Stop Frequency (MHz) | 19 | 32 | 47 | 70 | 90 | 147 | 210 | 290 | 410 | 580 | 750 | 840 | 1000 | 1100 | 1340 |

Prices (ea.): P $9.95 (6-49), B $24.95 (1-49), N $27.95 (1-49), S $26.95 (1-49)

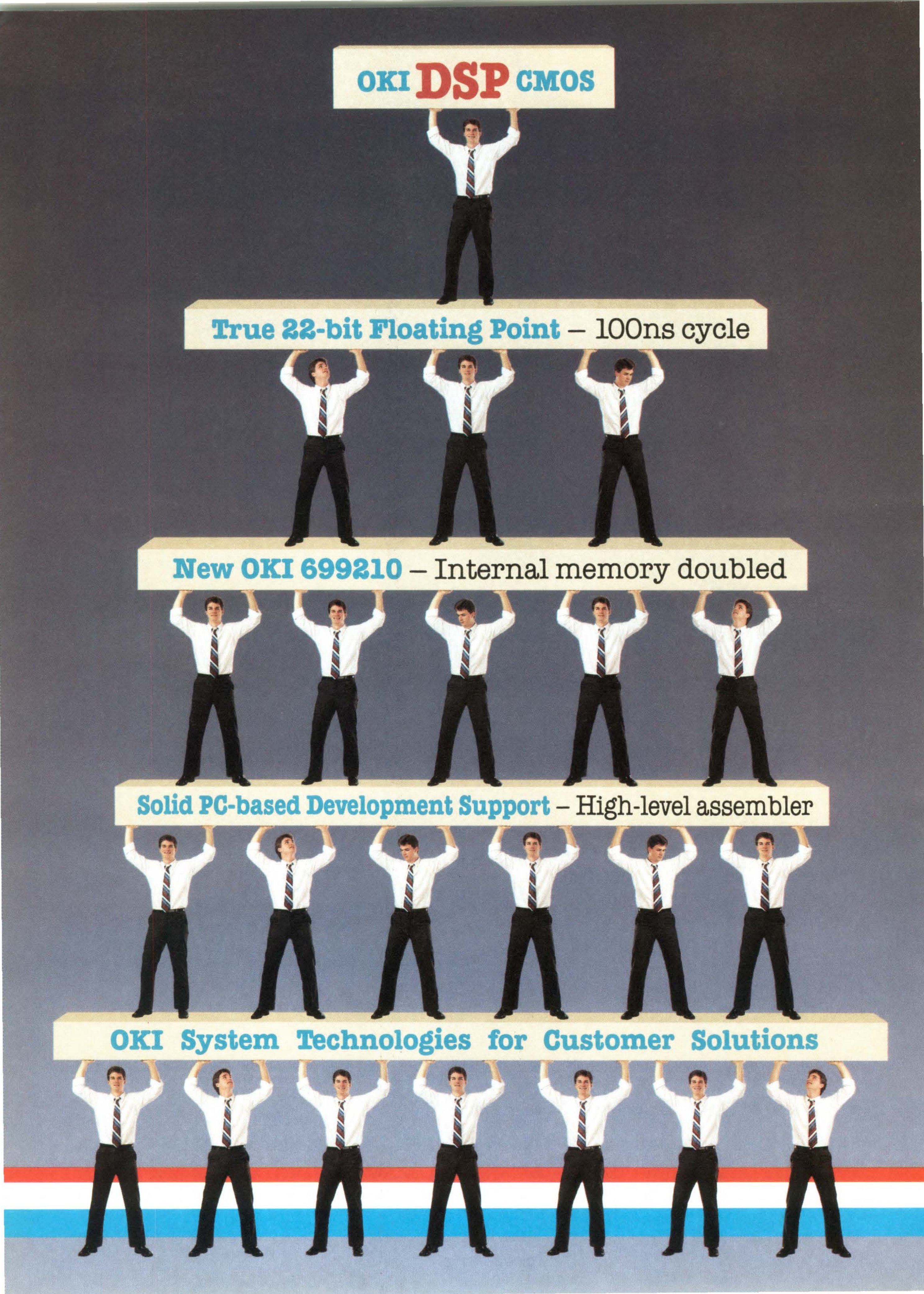
| HIGH PASS Model *HP- | 50 | 100 | 150 | 200 | 250 | 300 | 400 | 500 | 600 | 700 | 800 | 900 | 1000 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pass Band (MHz) start, max. | 41 | 90 | 133 | 185 | 225 | 290 | 395 | 500 | 600 | 700 | 780 | 910 | 1000 |
| Pass Band (MHz) end, min. | 200 | 400 | 600 | 800 | 1200 | 1200 | 1600 | 1600 | 1600 | 1800 | 2000 | 2100 | 2200 |
| Min. 20dB Stop Frequency (MHz) | 26 | 55 | 95 | 116 | 150 | 190 | 290 | 365 | 460 | 520 | 570 | 660 | 720 |

Prices (ea.): P $12.95 (6-49), B $27.95 (1-49), N $30.95 (1-49), S $29.95 (1-49)

*Prefix P for pins, B for BNC, N for Type N, S for SMA    *example:* **PLP-10.7**

C105 REV.D

**CIRCLE NO 161**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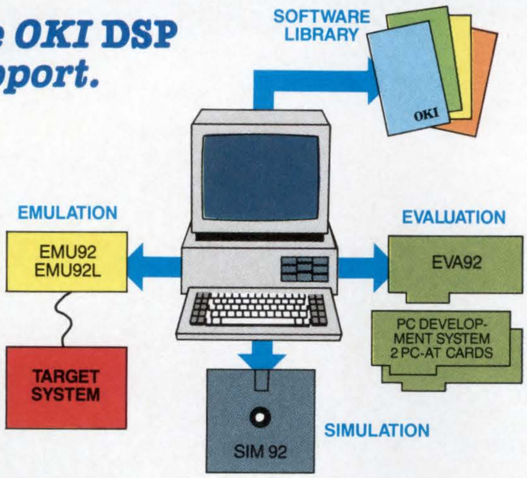


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CIRCLE NO 157

## Current-feedback amp has limitations

I agree with David Nelson's comments (in Signals & Noise, February 4, 1988, pg 34) about the use of the term "transimpedance amplifier." The circuit used in Analog Design's AD9610 should correctly be called a "current feedback" configuration.

I would like to make a few observations about the gain-bandwidth-independence property of the current-feedback configuration. I can specifically remember using a Class A all-npn amplifier of this type in 1960 as a video amplifier in the first TV studio camera to use transistors. The complementary configuration now being presented by Comlinear, Analog Devices, Elantec, and other companies represents a Class A-B version capable of operating in an op-amp configuration. However, its so-called gain-bandwidth independence is achieved only at the expense of limiting unity-gain bandwidth by the value of the series resistor in the feedback path. The need to use low values of feedback elements to obtain wide bandwidths also represents a severe limitation when low-power or inverting-mode operation is required.

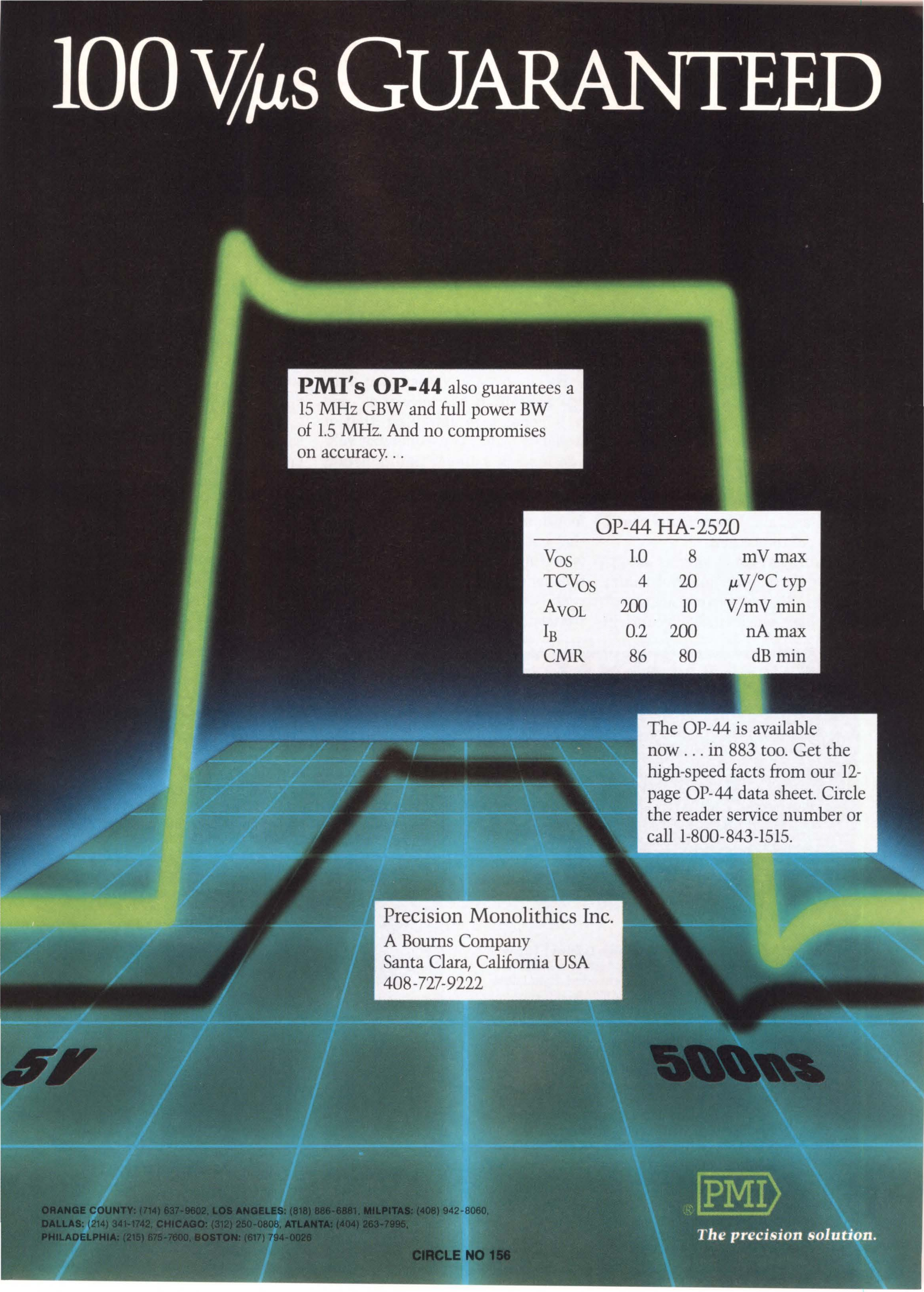

"BY THE WAY, DID YOU EVER GET RID OF THE PULSATING ORANGE AND FUCHSIA STRIPES IN YOUR COMPUTER?"

I have devised a solution to the above limitations in the form of a complementary quad input configuration that allows for gain-bandwidth optimization while also maintaining true op-amp high-voltage impedance and differential-input capability (the patent application is pending). I would be pleased to discuss these ideas with anyone who is interested in obtaining wide-bandwidth, wide-dynamic-range amplifiers using complementary bipolar processes.

*Derek Bray*
*Director, Design Services*
*Analog Design Tools Inc*
*Sunnyvale, CA*

## A fair hearing for transconductance

I have some comments on Keats Pullen's recent letter (Signals & Noise, March 17, 1988, pg 34). I



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CIRCLE NO 156

helped Tarlton Fleming review Keats Pullen's original submission to Design Ideas, and I think EDN is being fairer than fair.

Keats criticizes electronics engineers in general, and EDN's editors in particular, for not being properly appreciative of transconductance, or $g_m$, and of how important it is in the circuit-design process. On the contrary, many of us engineers appreciate that $g_m$ is a very essential phenomenon. And we take it for granted. Specifically, most bipolar transistors have a $g_m$ that's so close to theoretical that you *can* take it for granted: $g_m = 39 \cdot i$ (and the corollary: current is an exponential function of $V_{be}$). Yet Keats Pullen wants me to measure the $g_m$ on every transistor I use, and I have found that I don't have to do that.

Keats says that as long as beta is greater than some nominal value, such as 20, "it's unimportant." Keats may work with circuits in which any beta over 20 is perfectly adequate, but I work with many circuits in which a minimum beta of 100 or 300 or 700 is essential. And I work on other designs in which a maximum limit for beta is enforced. In other cases, the betas must be matched very carefully. I don't think it's proper for Keats to essay to tell everybody that measuring or specifying beta for their transistors is wrong. He can't tell everybody how to do their jobs.

He's correct in saying that voltage gain often has linearities, and he's correct in implying that it would be foolish to assume that voltage gain is a linear and constant function for all sizes of signal. But I don't know any engineer who's so foolish as to refuse to acknowledge that gain can vary or distort. Keats is setting up a straw man when he tells us not to trust voltage gain.

On the other hand, using *only transistors* (bipolar or FET), I have designed current amplifiers that have excellent linear and stable gain over wide ranges of current. Apparently Keats Pullen thinks I'm imagining things when I rely on the excellent linearity and constancy of the gain of modern planar transistors?

Furthermore, Keats tells us that the $g_m$ of tubes and FETs *is* (q/kT) times the device's operating current, for small currents. Unfortunately, that is a case of gross oversimplification. For some devices, it's approximately true, but for others, $g_m$ per unit of current is never more than a small fraction of (q/kT), depending on device physics, geometries, etc. And apparently Keats has a fixation on "inherently exponential nonlinearities," but conveniently ignores the fact that FETs and tubes are most often operated in their square-law regions. Doctrinaire opinions must be rejected whenever they are wrong.



   

Keats has argued that measuring the $g_m$ and its deviation from theoretical is very important for the design of low-distortion circuits. In some fields (RF or microwave amplifiers?) he is correct, but in other areas, the use of feedback makes the need to compute the distortion an obsolescent art. Modern operational amplifiers and other feedback amplifiers can now provide low-distortion gain, which, only 20 years ago, did require strenuous and rigorous low-distortion circuit design. It's also true that modern circuit-analysis simulators such as Spice can provide rather accurate treatment of the linear and nonlinear parts of $g_m$ and of other circuit elements, so it's not always necessary for the engineer to give any particular thought to that part of the analysis. (I agree with Jim Williams; I believe it's wrong to do low-distortion circuit design without thinking about it, and I myself refuse to do so, but it is *possible* to do so . . . .)

I have no objection to the use of $g_m$ as a tool that's useful in design. But I do object to being told that other tools are not useful.

Incidentally, as I recall the original Design Idea submission by Keats Pullen, he stood on his soapbox and proclaimed that you really must measure the $g_m$ of the devices, but he never showed any advantages or useful design tricks that would make your circuit design easy and neat after you had measured $g_m$. So, if he could show us an example of a useful circuit in which his $g_m$ analysis made for new and improved insights, I'd have no objection to seeing it published. But as it is, he just seems to be hollering, "Look, everybody's out of step with Johnny. . . ."

*Robert A Pease*
*Electronics engineer*
*National Semiconductor*
*San Francisco, CA*

### YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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| Max. Points/Second | 1000 GS/s | 100 GS/s |
| Vertical Resolution | 11 bits | 9 bits |
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| Fully Programmable | Yes | Yes |

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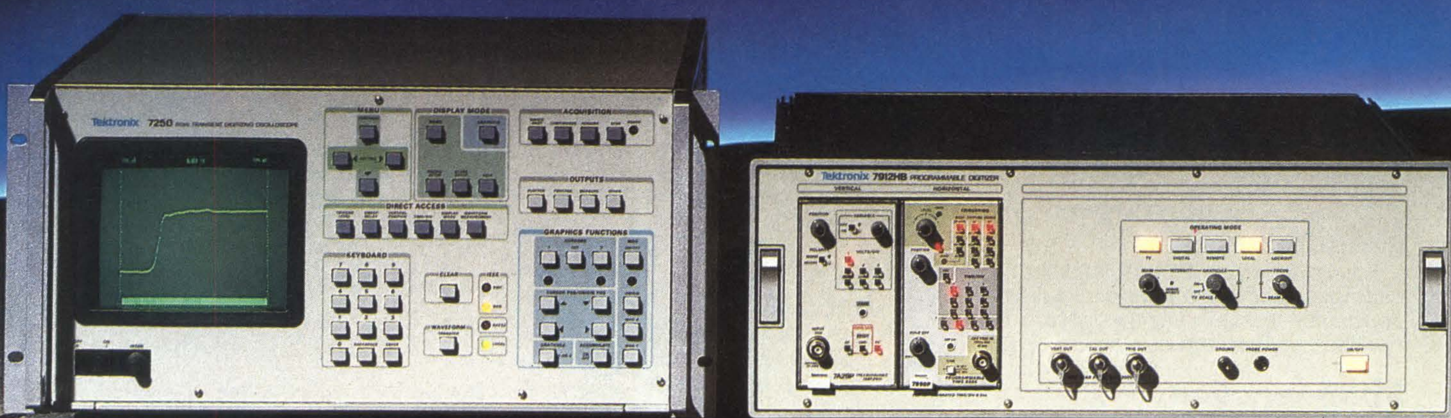


CIRCLE NO 154

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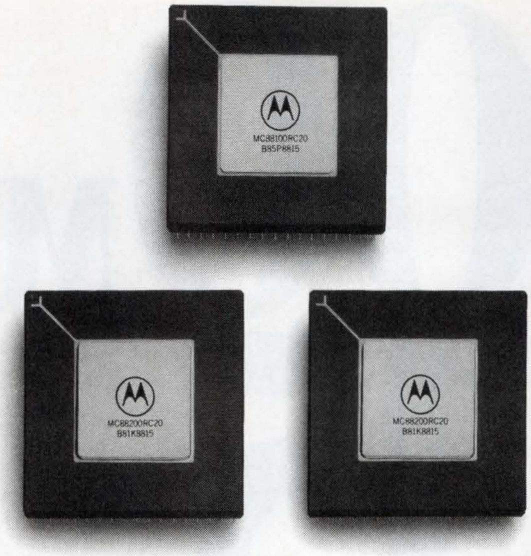


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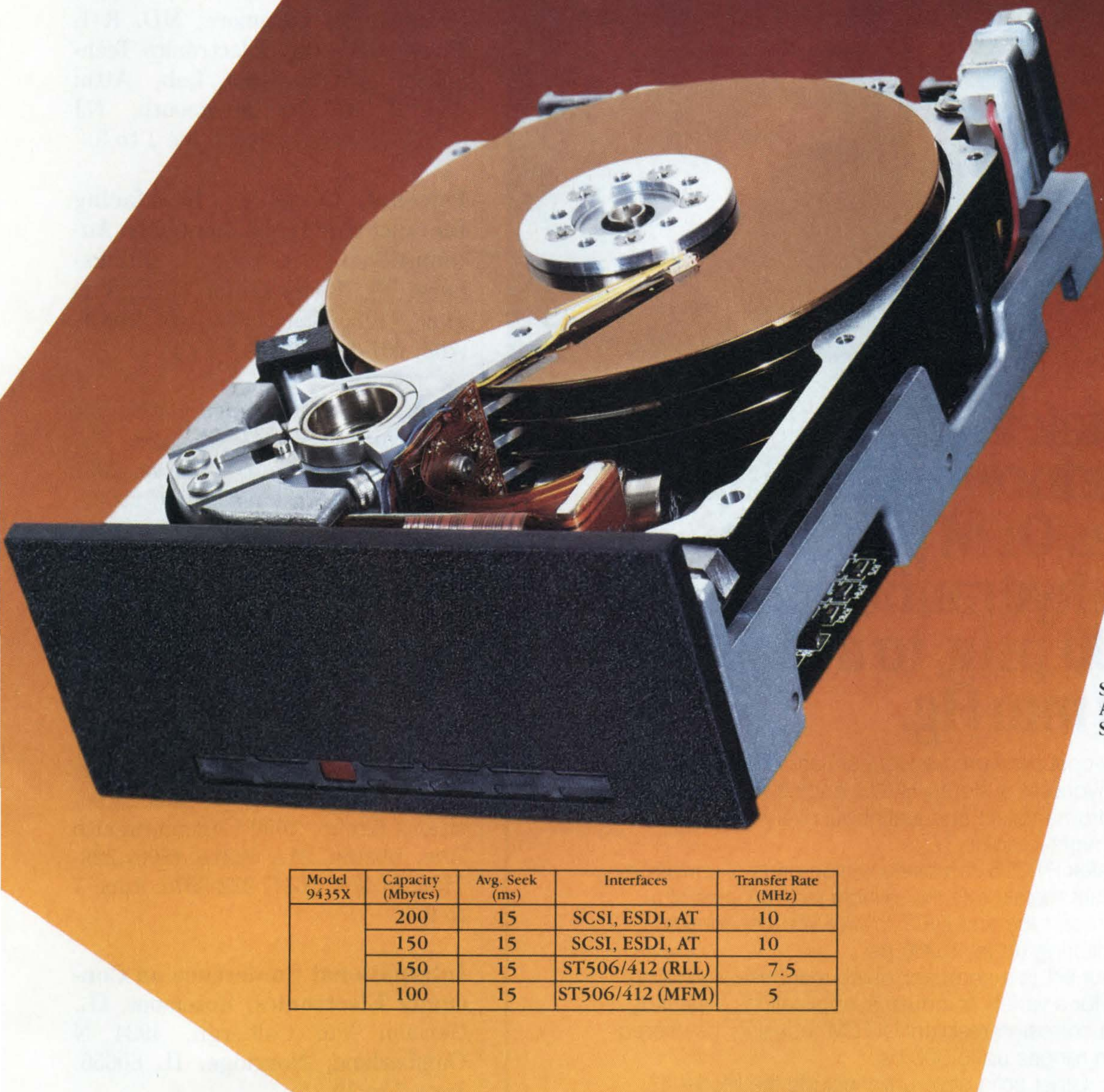


SHOWN
ACTUAL
SIZE

| Model 9435X | Capacity (Mbytes) | Avg. Seek (ms) | Interfaces | Transfer Rate (MHz) |
|---|---|---|---|---|
| | 200 | 15 | SCSI, ESDI, AT | 10 |
| | 150 | 15 | SCSI, ESDI, AT | 10 |
| | 150 | 15 | ST506/412 (RLL) | 7.5 |
| | 100 | 15 | ST506/412 (MFM) | 5 |

# CALENDAR

**Troubleshooting Microprocessor-Based Equipment and Digital Devices** (seminar), Dallas, TX. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. May 31 to June 3.

**42nd Annual Frequency Control Symposium,** Baltimore, MD. R L Filler, US Army Electronics Technology and Devices Lab, Attn: SLCET-EQ, Ft Monmouth, NJ 07703. (201) 544-2467. June 1 to 3.

**Personal Computer Interfacing for Scientific Instrumentation Automation** (short course), Blacksburg, VA. Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. (703) 961-4848. June 2 to 4.

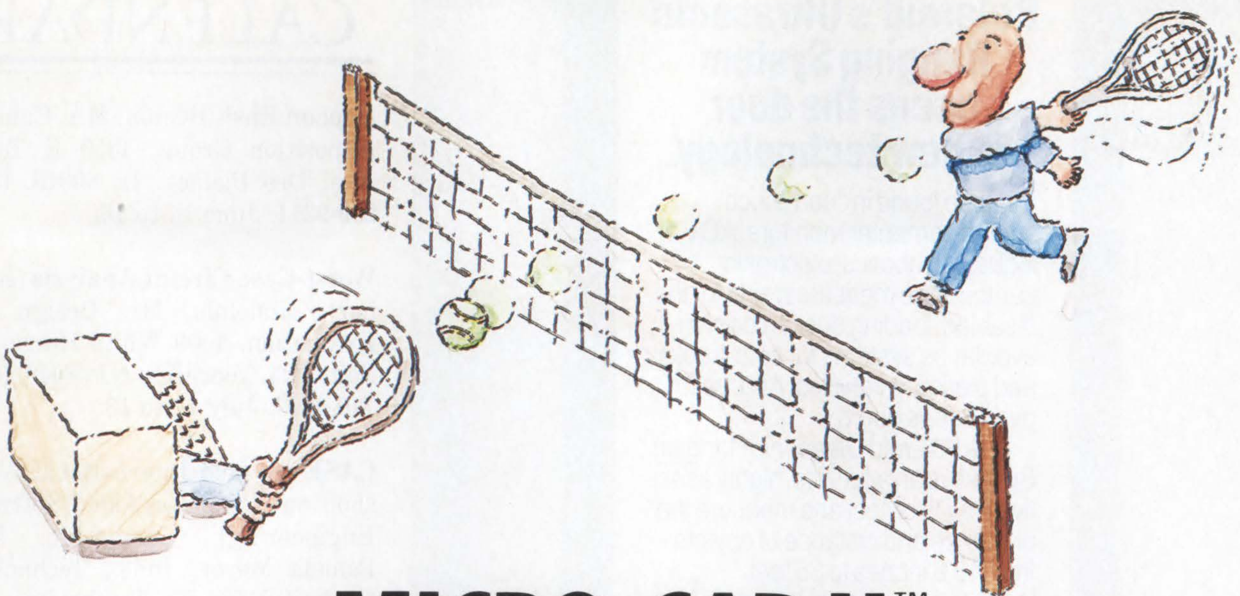
**International Summer Consumer Electronics Show,** Chicago, IL. Consumer Electronics Shows, 2001 Eye St NW, Washington, DC 20006. (202) 457-8700. June 4 to 7.

**FiberTour 88,** Boston, MA. Joan Barry, Xpos, Box 8872, Salem, MA 01971. (617) 744-9767. Conference cosponsored by Lightwave magazine. June 7 to 8.

**ATE & Instrumentation Conference East,** Boston, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. June 7 to 9.

**International Conference on Consumer Electronics,** Rosemont, IL. Geriann Van Calbergh, 4924 N Cumberland, Norridge, IL 60656. June 7 to 10.

**25th Design Automation Conference,** Anaheim, CA. MP Associates, 7366 Old Mill Trail, Suite 101, Boulder, CO 80301. (303) 530-4333. June 12 to 15.



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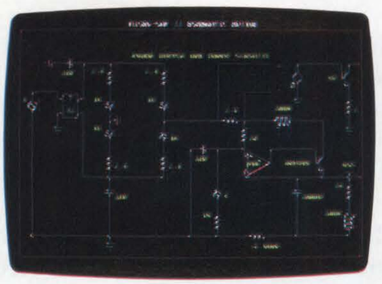

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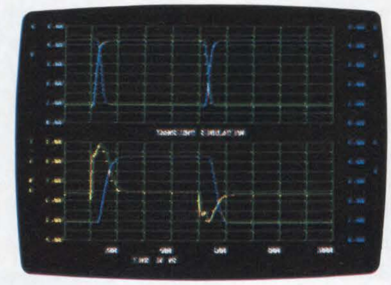

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**Nepcon East,** Boston, MA. Cahners Exposition Group, 1350 E Touhy Ave, Des Plaines, IL 60018. (312) 299-9311. June 14 to 16.

**Worst-Case Circuit Analysis** (seminar), Honolulu, HI. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. July 11 to 13.

**CASE '88** (2nd International Workshop on Computer-Aided Software Engineering), Cambridge, MA. Pamela Meyer, Index Technology Corp, 1 Main St, Cambridge, MA 02142. (617) 494-8200, ext 1988. July 12 to 15.

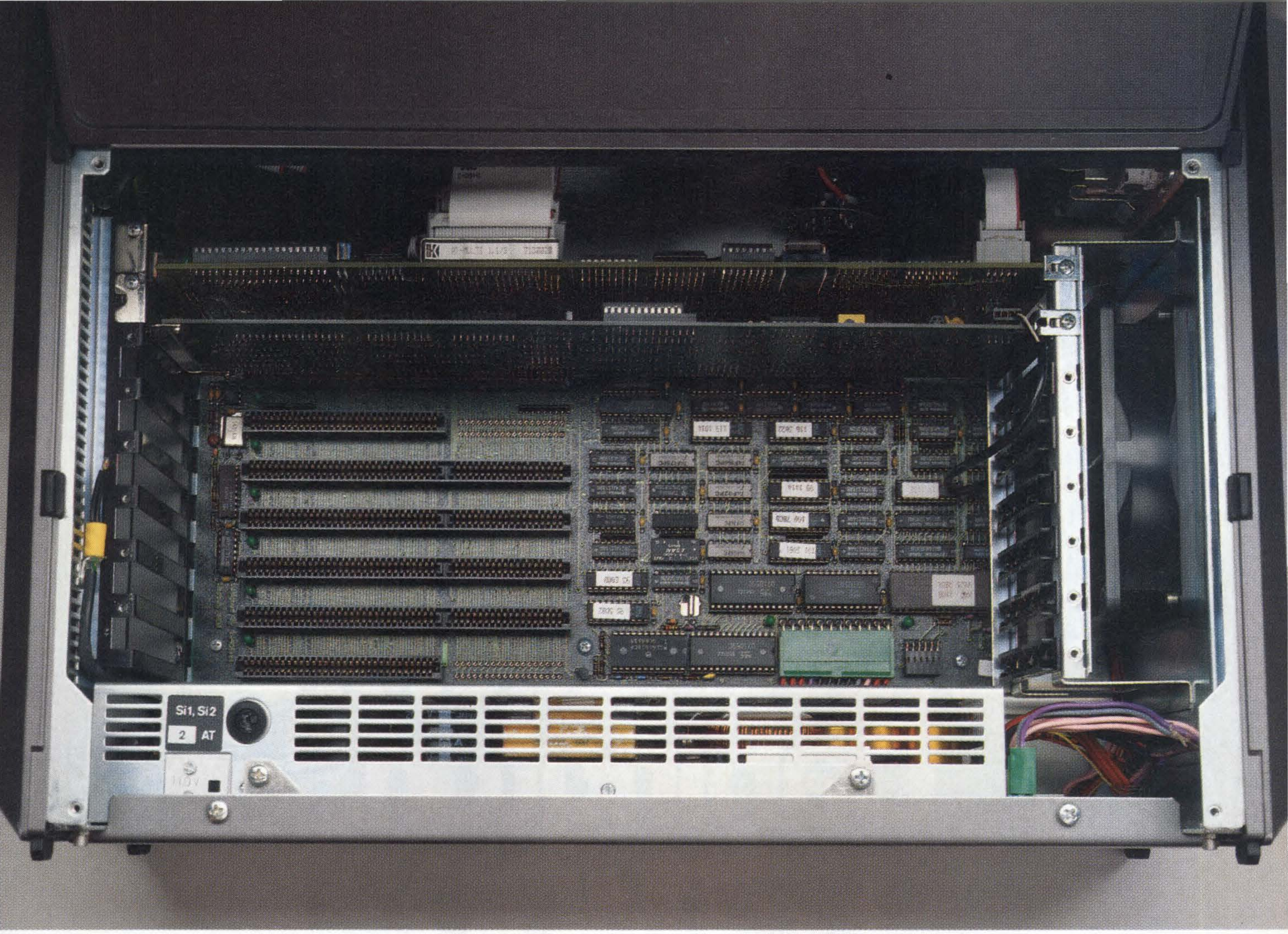
**Siggraph,** Atlanta, GA. Barbara Voss, Robert P Kenworthy Inc, 866 United Nations Plaza, Suite 424, New York, NY 10017. (212) 752-0911. August 1 to 5.

**Midcon,** Dallas, TX. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (800) 421-6816; in CA, (213) 772-2965. August 30 to September 1.

**Surface Mount '88,** Marlborough, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. August 30 to September 1.

**Modern Electronic Packaging** (seminar), Santa Clara, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. September 7 to 9.

**12th International Fiber Optic Communications and Local Area Networks Exposition,** Atlanta, GA. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (800) 323-1088; in MA, (617) 232-3111. September 12 to 16.

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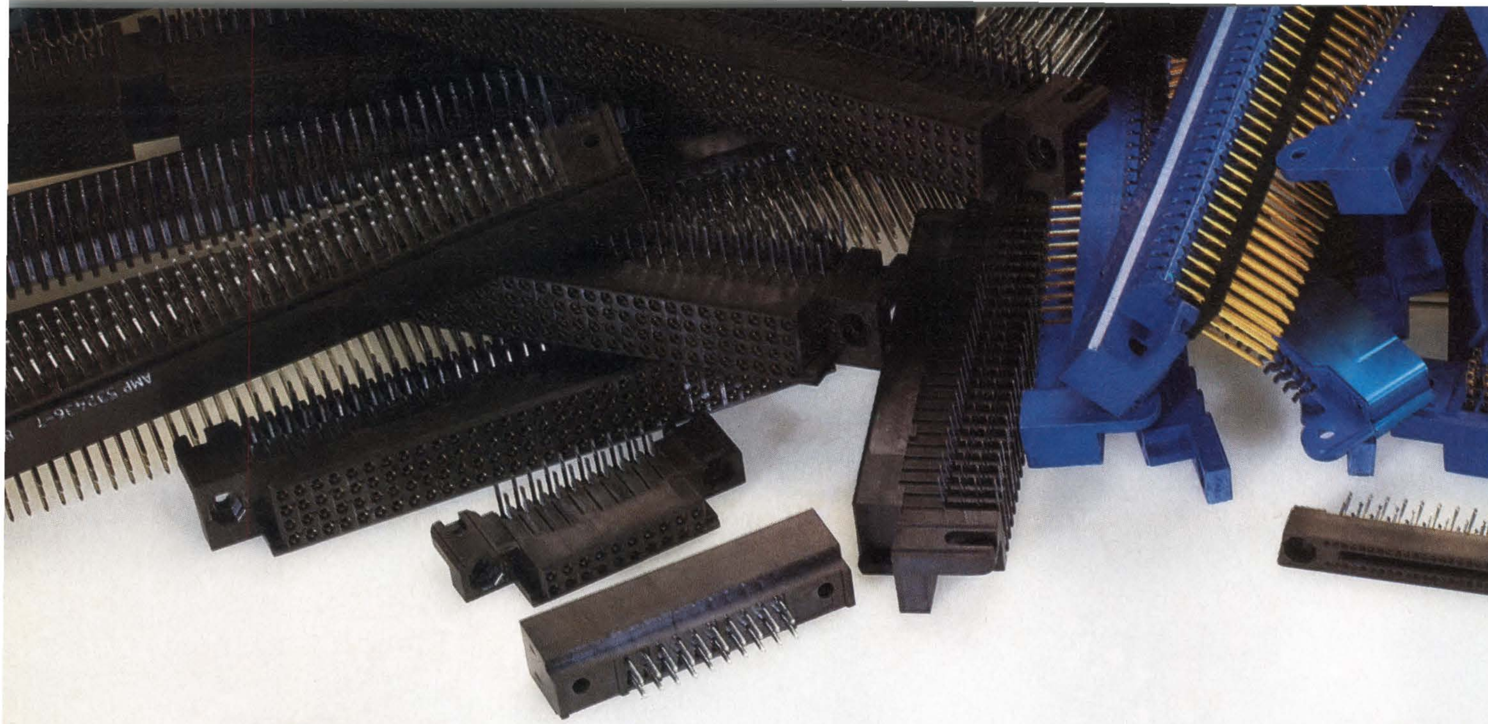

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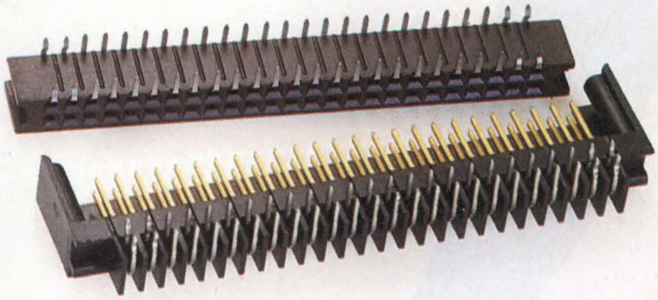

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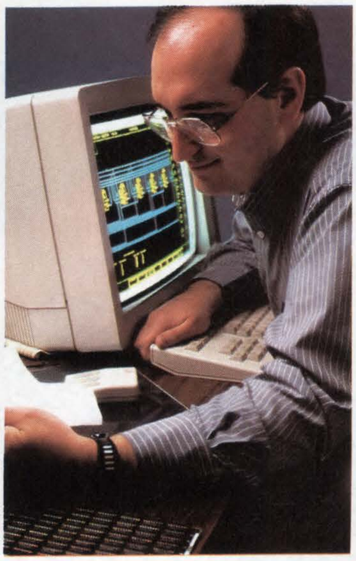
**CIRCLE NO 134**

# EDITORIAL

## An industry named Sue



Lawsuits seem to be taking up more and more time in the electronics industry. Perhaps the most widely publicized suit in recent days is the copyright-infringement suit being brought against NEC by Intel. Intel claims that NEC incorporated Intel's copyrighted 8086 microcode in NEC's V Series μPs. NEC counters that it did not appropriate the 8086 microcode, but that even if it had, it wouldn't be in violation of copyright—Intel's copyright was already forfeit, NEC claims, because Intel had built several million 8086-family μPs without prominently displaying a copyright symbol.

Meanwhile, Zilog—which acquired the rights to build NEC's V Series μPs—is also suing NEC, because the NEC-Intel suit raises questions about the future value of V Series chips. Because of their uncertain future, the V Series chips appeal to fewer designers, claims Zilog. NEC is countersuing Zilog for infringing on a host of unrelated patents. But wait: NEC has also brought up an old legal issue, that of Zilog's copyright on the letter Z.

Legal actions involve prices as well as copyrights. For example, shortly after the current US-Japan semiconductor trade agreement went into effect, the supply of dynamic RAMs (DRAMs) dried up and prices skyrocketed. Today, the prices originally agreed upon would look very good, but you won't find any DRAM chips on the market for those amounts. However, says Atari, a contract is a contract. The company is currently suing Micron Technology because Micron won't deliver DRAMs at an agreed-upon price that's lower than the DRAMs' current market value.

On the software front, Apple is suing both Microsoft and Hewlett-Packard for reproducing Apple's copyrighted Macintosh user interface in windowing products for IBM PCs and compatible computers. Apple filed a similar suit some time ago against Digital Research but settled the suit out of court. Along somewhat different lines, Hewlett-Packard and a host of other vendors of Unix-based workstations may take AT&T and Sun Microsystems to court over the future existence of Unix as an open standard.

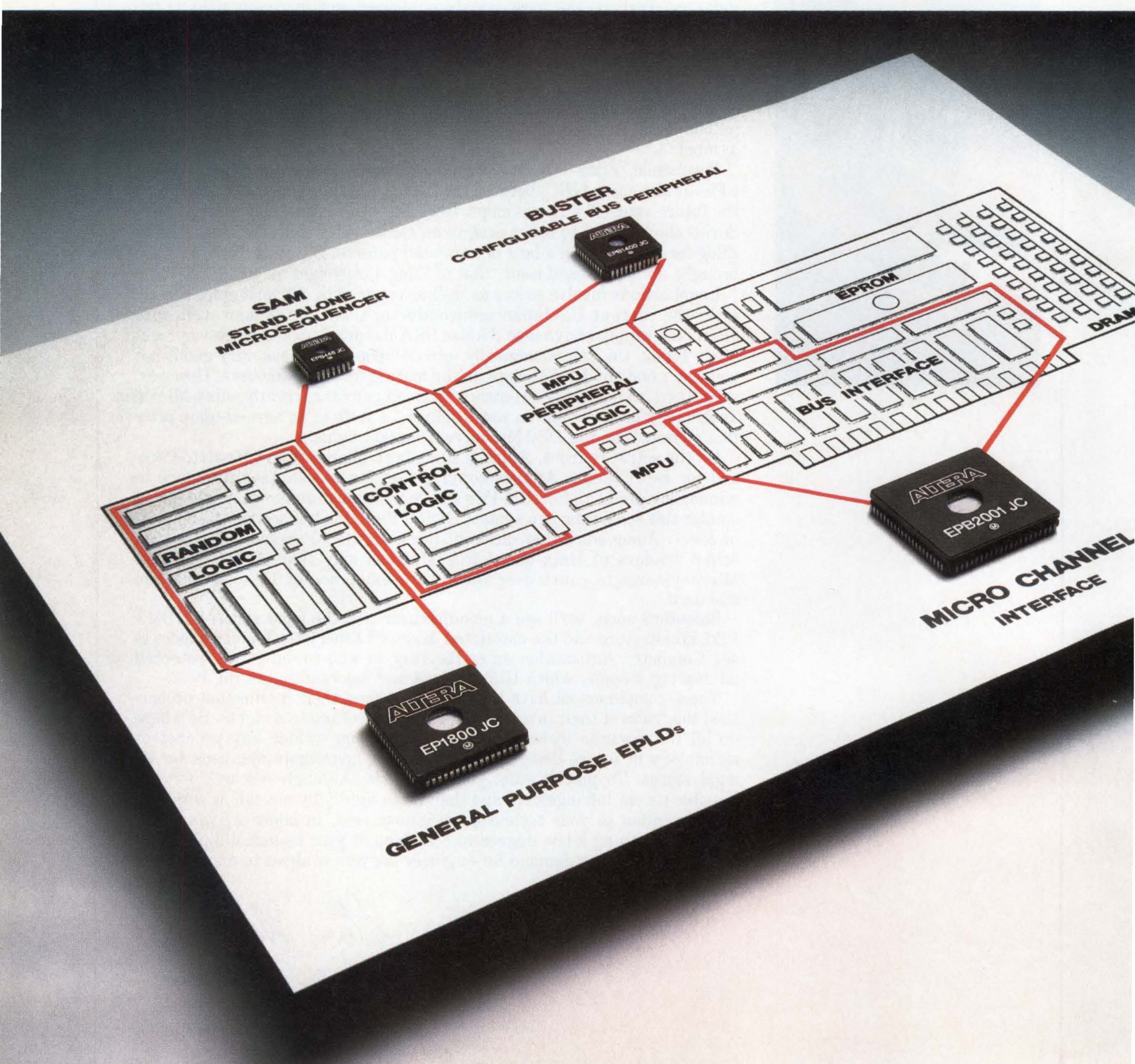
Sometime soon, we'll see a manufacturer test the legal status of IBM's PS/2 architecture and the associated Micro Channel bus. You can expect to see Computer Automation enter the fray as well to defend its patented addressing scheme, which IBM licensed and incorporated in the PS/2.

These companies all have the right to defend their intellectual properties, the fruits of their investments, and their contractual rights. So where do all the lawsuits leave you? Well, before you include any product or technology in future designs, you must now investigate and consider its legal status. To play it safe, you should do thorough research for any possible patent infringement and then tread lightly by not calling unnecessary attention to your technological innovations. In addition, you might consider pursuing a law degree to complement your technical diploma. It looks as though the demand for engineer/lawyers is about to explode.

Steven H. Leibson

**Steven H Leibson**
**Regional Editor**

# After 4 years of we're announcing



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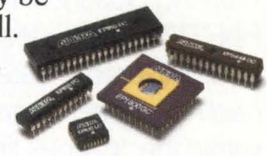

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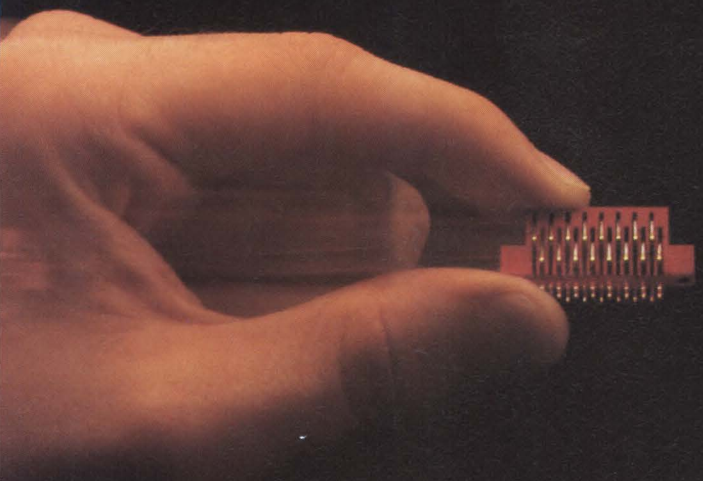

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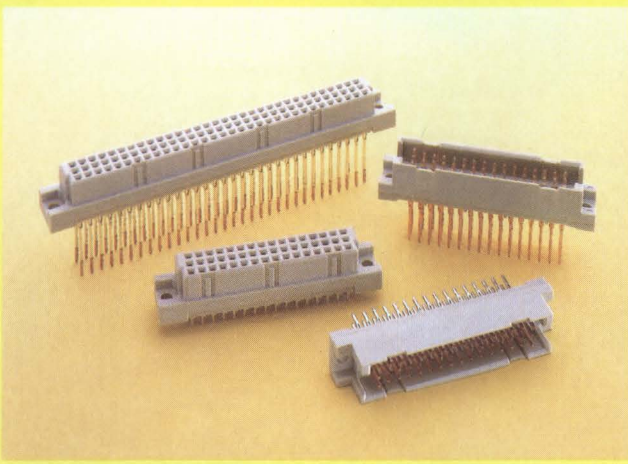

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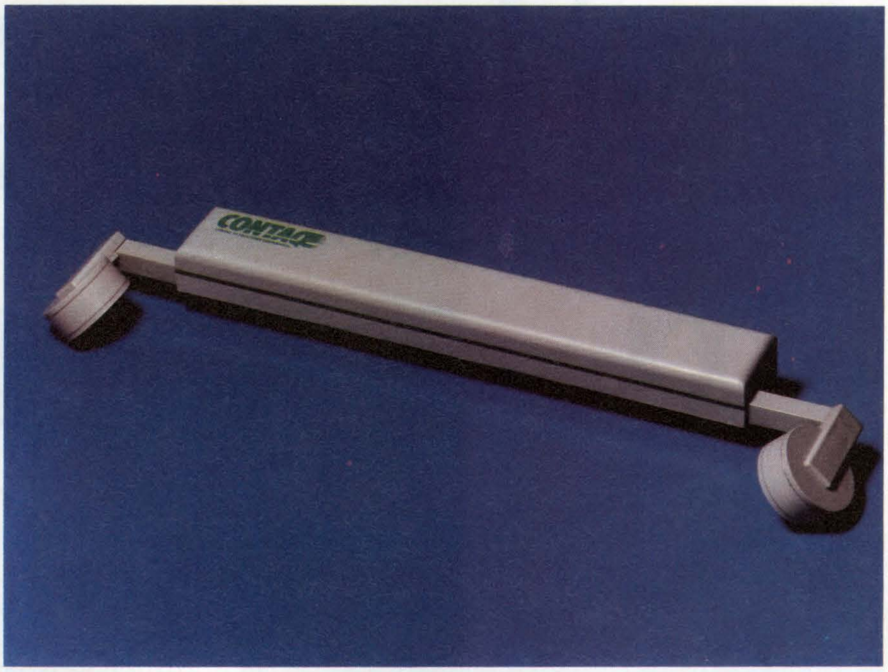
# Uniting ultrasonics and microelectronics reaps a cost-effective ranging system

John Gallant, *Associate Editor*

Proximity detection and position measurement are no longer "contact sports": Techniques that remotely sense the presence of an object are replacing mechanical devices, such as feelers, rollers, and floats, which make direct contact with the object to be detected. One of these technologies is ultrasound. If you have an application that requires the sensing of relatively large objects (anywhere from a few inches in diameter to a few feet) over great distances (as much as 50 ft), you may want to consider an ultrasonic ranging system.




***The $695 PointScreen, an ultrasonic input device** from Contac Technologies Corp, attaches to the front of a computer display. When you point your finger within an inch of the screen, two electrostatic transducers report your finger position to the terminal.*

Ultrasonics involves transmitting a burst of ultrasonic waves (greater than 20 kHz) and listening for an echo return from an object. The formula for determining the distance from the transmitter to the object is

$$D = V \times t/2,$$

where D equals the distance to the object in feet, V equals the speed of sound in feet/sec (1125 feet/sec in air at 22°C), and t equals the time elapsed between the transmitted pulse and the return echo in seconds. In effect, an ultrasonic-ranging system acts like a pulsed-radar system using ultrasonic waves, therefore allowing you to employ many radar signal-processing techniques, such as chirping, range windowing, and time-sensitivity control, to aid in ranging.

Even though this article concentrates on ultrasonic devices operating in air, it is also possible to transmit ultrasonic waves through liquid media. Fish finders use this technology, for example, as well as medical electronics, which transmits ultrasonic waves into the body. In fact, ultrasonic liquid-level detectors can operate in one of two ways: ultrasonic waves traveling in air and an echo reflecting from the surface of the liquid to a receiver in the air, or ultrasonic waves traveling in the liquid and a reflecting echo to a submerged receiver when the surface level is detected.

### The transducer comes first

An ultrasonic-echo ranging system consists of a transducer and an electronic module. One popular transducer on the market is an electrostatic device available from Polaroid Corp. It is composed of a very thin, Kapton foil that transforms electrical energy into sound waves and, conversely, sound waves into electrical energy. The foil, which has a conductive (gold) coating on its front side, is stretched over a metallic (aluminum) backplate. The backplate has a series of concentric grooves over which the foil is suspended.

The foil and the backplate represent an electrical capacitor. When charged, the foil experiences an electrostatic force. An ac voltage at a given frequency (nominally between 40 and 100 kHz) forces the foil to move at the same frequency and emit sound waves. A returning echo signal produces an electrical voltage. A perforated front cover mechanically protects the foil with only a small sacrifice in signal strength.

The company specifies the minimum transmit sensitivity as follows: 110 dB above a 20-μPa (micro Pascals) sound pressure level at a distance of 1m from the transducer, with an applied 150V dc bias signal and a 300V ac, 50-kHz signal. The

# Who drives Power Mosfets faster, at lower power, for less?

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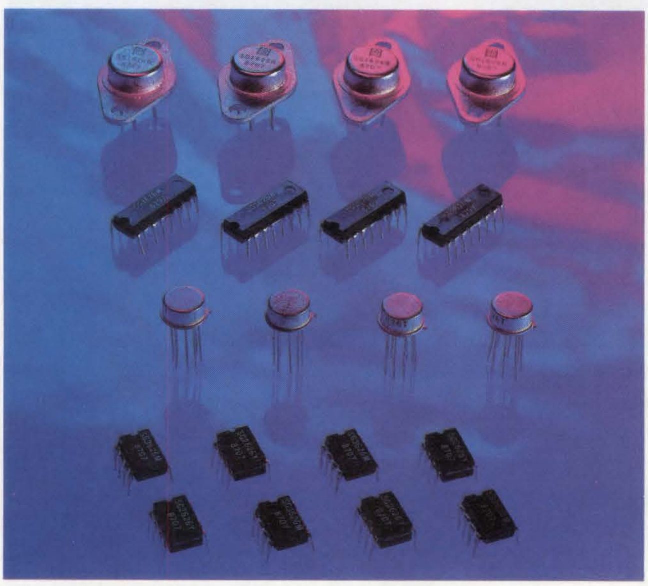

Silicon General's new line of dual high speed drivers do the job of driving power MOSFETS better than anything else on the market today.

Against 3 out of 4 competitors, the new SG1626/ SG3626 operates 1.5 to 3 times faster.

Versus the long time industry standard, the SG1626/SG3626 dissipates only half the power at similar switching times.

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**Ideal for switching power supplies and motor control.**

The SG1626/SG3626 is a dual inverting driver ideally suited to drive power MOSFETs and other applications calling for the conversion of digital input signals to high speed outputs to drive large capacitive loads. A non-inverting version, the SG1625/3625, is also available.

These devices use high voltage schottky logic to convert TTL signals to high speed outputs up to 18 volts. Totem pole outputs have 3.0 amperes peak current capability so they can drive 2500 picofarad loads in less than 40 nanoseconds.

**Pin for pin compatible.**

The SG1626 is pin for pin compatible with National's DS0026, Motorola's MMH0026, Teledyne's TSC426 and Intersil's ICL7667.

**Call us for samples and data.**

Several packages are available including 8 pin plastic, cerdip, ceramic, TO-99, TO-66 and 16 pin batwing. Best temperature range is -55° C to 125° C. Other parts operate from -25° C to 85° C and 0° C to 70° C.

To arrange shipment of sample quantities and/or receive full technical information, please address Silicon General, Inc., Semiconductor Group, 11861 Western Avenue, Garden Grove, California 92641. Telephone (714) 898-8121. TWX: 910-596-1804. FAX (714) 893-2570.

SILICON GENERAL

minimum receive sensitivity with an applied 150V dc bias is −42 dB below 1V/Pa at 1m.

Polaroid has three versions of the electrostatic transducer for sale. In minimum-quantity orders of 10, an instrument-grade unit (cold-roll-steel housing) costs $15, an environmental-grade unit (aluminum housing) costs $17, and a reduced-size unit (7000 Model) costs $14.50. Prices drop considerably for large-quantity orders. For example, the 7000 Model transducer costs $2 in quantities of 500,000 to 1,000,000.

**Piezoelectric wonders**

Although the electrostatic transducer appears to be the most popular, the phenomenon of piezoelectricity provides another viable means for developing ultrasonic transducers. These types of transducers use the piezoelectric properties of synthetic polycrystalline ceramics such as barium titanate and lead zirconate titanate. A polarization process aligns the molecular dipoles of the ceramics in one direction (the poling axis). Applying an electrical field along the axis produces a mechanical deformation. Compressing or stretching forces produce a voltage.

Because piezoelectric ceramic—piezoceramic—transducers have to achieve sufficient amplitude before they can function as ultrasonic transmitters and receivers, they are generally connected as benders. One such bender configuration cements together two discs or rectangular strips of ceramic of opposite polarization (**Fig 1**). When you apply a voltage, one piece contracts while the other expands. Although the actual deformation is small, the displacement of the entire assembly is relatively large. Essentially, the bender behaves like a heated bimetal strip.

Piezoceramic transducers offer advantages in severe operating environments because, thanks to their configuration, they can be packaged in hermetically sealed cases. They generally exhibit a sharp resonant peak at the frequency of operation, however. The bandwidths of these devices can be less than 1 kHz. Tuning techniques can broaden the frequency-response characteristics to tens of kHz, but a sacrifice in sensitivity will result.

Blatek uses various bender techniques to produce its 8000 Series of piezoceramic transducers, which have standard frequencies of 25, 40, 100, and 200 kHz. A 40-kHz version of the 8010 transducer, for example, achieves a transmit sensitivity of 25.0 dB referenced to 1 μbar/V measured at a distance of 1m from the transmitter; the receive sensitivity is −60.0 dB relative to 1V/μbar at a distance of 1m. The untuned 6-dB bandwidth is specified at 400 Hz. The aluminum housing of the 200-mW 8000 Series measures 1 in. in diameter and 13/16 in. in depth (including mounting pins). Each family member sells for $10.95.

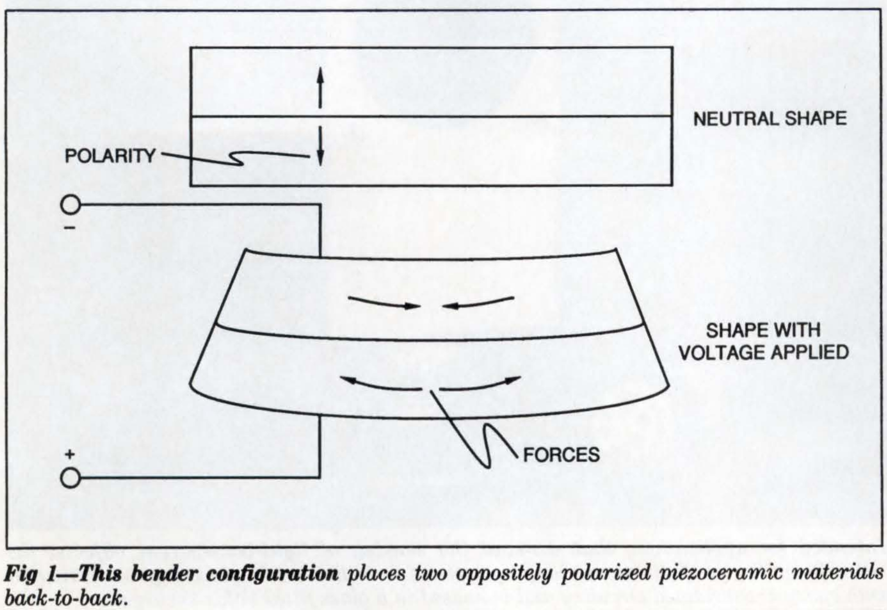



*Fig 1—**This bender configuration** places two oppositely polarized piezoceramic materials back-to-back.*

**Side lobes can cause trouble**

All ultrasonic transducers have a power-radiation pattern similar to that of an electromagnetic antenna. This pattern exhibits a main beam with side lobes for both transmit and receive modes. The Polaroid transducer, for instance, has a nominal 10° beamwidth (3 dB) at 50 kHz with the first side lobe nominally 28 dB below the main-beam peak response. If the receiver sensitivity is set below the side-lobe level, the ranging system can erroneously detect an ultrasonic echo off the main axis. With the Polaroid device, you have to ensure that the receiver sensitivity is below any echoes returning from the side lobe.

Massa Products Corp manufactures a number of piezoceramic transducers that virtually eliminate side lobes. Two products, Models E-152 and E-188, generate a broad-beam and a narrow-beam pattern, respectively.

Model E-152 comes in two versions and uses proprietary technology to generate a 75° beam at 40 kHz and a 60° beam at 75 kHz without side-lobe patterns. The manufacturer specifies the transmit sensitivity as 10 dB relative to 1 μbar/volt at 1 ft from the transducer (untuned). The untuned bandwidth is 1 kHz. The 40-kHz product has a receive sensitivity of −57 dB relative to 1V/μbar (untuned); the 75-kHz model has a receive sensitivity of −62 dB relative to the same reference.

Model E-188 also comes in two versions. Operating at 215 and 220 kHz, respectively, each version generates a 10° beam. Both specify a transmit sensitivity of 20 dB above 1 μbar/V measured 1 ft from the transducer and a receive sensitivity of −77 dB relative to 1V/μbar measured from the same distance.

The Model E-152 transducer measures 0.437 in. in diameter×0.397 in. in depth, and Model E-188 measures 0.510 in. in diameter×0.580 in. in depth. All models cost $66 (the minimum order is $100).

Although the transducer is an essential ingredient of an ultrasonic ranging system, it represents only one-half of the design. An electronic module is still required to drive the transducer and detect echo returns. You can accomplish this at the chip level or purchase ranging modules with the electronics optimized for a particular transducer.

Texas Instruments' offering is a 2-chip set intended to interface to a 50-kHz, 300V ac transducer. The TL852 Sonar Ranging Receiver has a digitally programmable gain; the TL851 Range Control Chip measures distances from 6 in. to 35 ft and has an internal oscillator that supplies a 50-kHz signal to the transducer. Essentially, the TL852 is an op amp with a gain control block. You can change the overall gain in steps dependent on the transmit time, permitting the selective detection of objects as a function of range.

You can also opt for TI's SN28827 Sonar Ranging Module, which incorporates the TL851 and the TL852 chip set on a 2.21×1.89-in. pc board. The board requires no additional circuitry to interface to a 300V ac electrostatic transducer. When coupled to the transducer, the module transmits 16 cycles of ultrasonic waves at 49.4 kHz. An external blanking input selectively excludes echoes in a multiple-echo environment. The module sells for $13.80 (100). The individual 100-piece price for the TL851 and the TL852 is $2.16.

If you want, Polaroid offers a starter kit that you can use to evaluate its ultrasonic transducer for distance measurements. The $165 kit contains an instrument-grade transducer, a modified ranging board, a demonstration board that drives the ranging board and displays distances in 0.1-ft increments on a 3-digit LED display, two Polapulse 6V batteries, a battery holder, and two manuals.

A number of manufacturers offer ultrasonic-ranging systems with the transducer and electronics packaged in a single enclosure. The Agastat line of sensing systems from Electro Corp, for instance, combines the transmitter and the

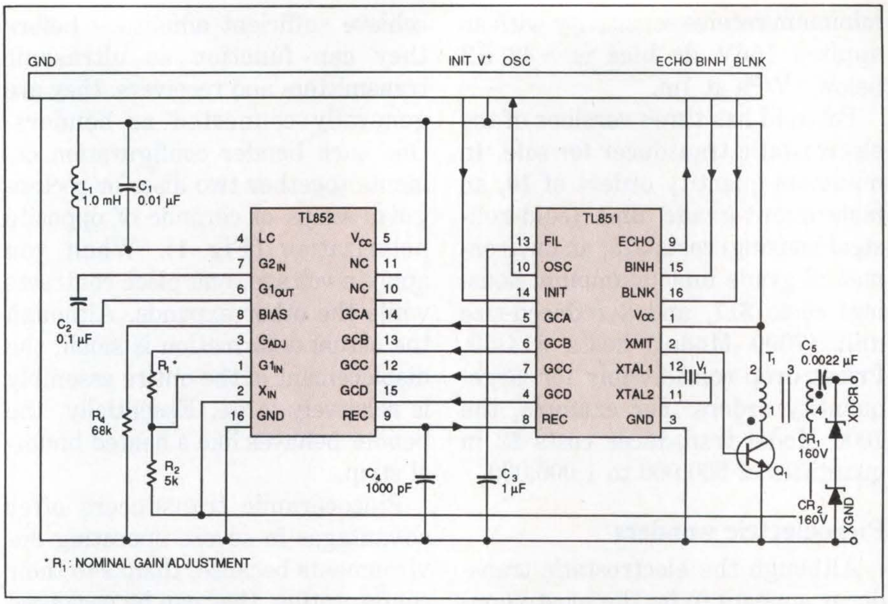
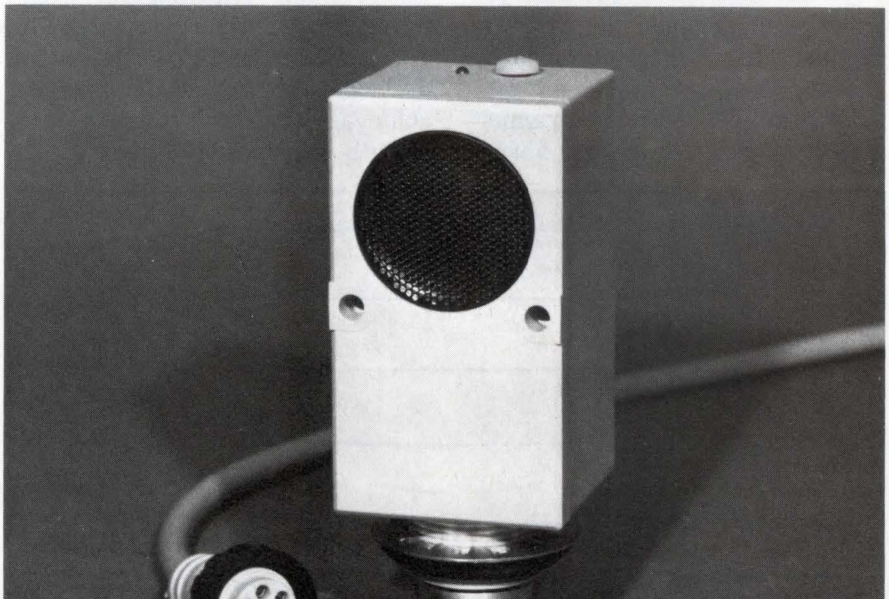



***Fig 2—When interfacing with a 50-kHz, 300V electrostatic transducer,*** *the SN28827 Sonar Ranging Module from Texas Instruments transmits 16 cycles of ultrasonic waves at 49.4 kHz.*



***Intended for applications that demand the sensing of light-transparent objects,*** *the Ultra-Beam Series of ultrasonic ranging systems from Banner Engineering is constructed with epoxy-encapsulated circuitry and is housed in a glass-filled Valox enclosure.*

receiver in one unit. The PLE version uses the Polaroid transducer and senses objects within the range of 4 in. to 21 ft. The unit is available with either an analog output that spans a 4- to 20-mA current range or a switched output that gives a normally open (NO) or normally closed (NC) output when it detects an echo. A µprocessor (the COPS400) selects three overlapping ranges; you select the desired range by inserting a key into the module.

The PCU version uses a Massa Products' piezoceramic transducer and senses objects within the range of 4 to 30 in. The PCU units are designed for hostile environments that preclude the use of electrostatic transducers. Analog units come with either 4- to 20-mA or 0 to 5V outputs, and switched-output units (NO or NC) provide either npn or pnp output switches. On the analog models, you can adjust the minimum range point and the span by means of multiturn potentiometers. A PLE analog version costs $320, and a switched-output version costs $270. A PCU analog version costs $240; a switched-output version costs $210.

Although primarily a manufacturer of photoelectric products, Banner Engineering Corp is aware of the suitability of ultrasonic ranging in certain applications and is now offering a series of such systems. The Ultra-Beam Series is intended to solve the problem of proximity detection for ranges that fall beyond the limits of photoelectrics and for applications that require sensing of light-transparent objects.

The series uses the Polaroid transducer operating at 50 kHz and senses objects within a range of 20 in. to 20 ft. For reliable detection, objects must present at least one square foot of surface area for each 10 ft of range between the sensor and the object.

## Misuse of ultrasound can cause headaches

As with most distance-measuring technologies, ultrasound displays advantages in certain applications and disadvantages in others. One advantage, regardless of application, is its ability to sense virtually any material, whether solid or liquid. An echo results whenever an ultrasonic beam encounters a medium with a different acoustic impedance than the medium in which it is traveling. Independent of color, the reflecting medium can be transparent, translucent, or opaque. Typical applications that are well-suited to ultrasonic detection are shown in **Fig A.**

Electro-optical waves travel at the speed of light. To economically use electro-optics, therefore, the transducer must rely on intensity measurements, which have limited range and are subject to air contamination such as dust and fog. Ultrasound, in contrast, propagates at the speed of sound (1125 feet/sec at 22°C in air). Thus, with the aid of inexpensive electronics, you can detect echoes from objects a few inches away to as far away as 50 feet.

The decrease in intensity of ultrasonic waves in the direction of propagation is principally a combination of two effects. One effect is the inverse square law in which the intensity drops 6 dB when the distance to an object doubles. The other is due to the absorption of sound in air, which varies somewhat with humidity and dust content, but most importantly with frequency. For example, the absorption at 40 kHz is approximately 0.08 dB/ft, whereas the absorption at 150 kHz is about 2 dB/ft.

Ultrasound is not problem free, however. The principle environmental consideration is the temperature-dependent velocity of sound in air. The velocity varies according to the equation:

$$V_{AIR}=1087\sqrt{(273+T°C)/273}\ \text{feet/sec},$$

where T°C equals the temperature in degrees Centigrade.

This variation produces a 7% measurement error when the system is operating over a temperature range of 0 to 40°C without temperature compensation. Feasible compensation schemes include temperature measuring and positioning a reference object a known distance from the object. For example, Electro Corp (Sarasota, FL) sells a $15 temperature-compensation reference target that attaches to the company's PLE ultrasonic modules. Because the reference target is a fixed distance (6.56 in.) from the transducer, the time elapsed between a transmit pulse and the detected echo calibrates the velocity of sound at a particular temperature. The module ignores the echo from the reference target when making range measurements from an object.

### Windy environment can prove troublesome

Air turbulence can also cause problems in ultrasonic ranging. Air currents and layers of different densities cause refraction of the sound wave, which can be a significant source of error when sensing hot objects or detecting targets in windy environments.

Humidity and air pressure are other minor considerations. For a change in relative humidity of 20%, humidity effects a propagation delay of 0.07%. Although normal atmospheric air-pressure changes have no substantial effect on measurement

The Ultra-Beam 925 is a switched-output model with spdt C-type relay outputs. The Ultra-Beam 923 provides two analog outputs with adjustable positive or negative slopes. You can adjust the range limits for the 0 to 10V dc and 0- to 20-mA outputs with potentiometers. Both units come in NEMA-1, -2, and -12 housings with a red LED indicator that lights up when the unit detects an object. The Ultra-Beam 925 costs $150; the 923 costs $10 more.

The 942 Series of ultrasonic distance sensors from Micro Switch includes a model that provides two independent switched outputs (NO or NC). The states change when a target moves through two set points, independently adjustable in 0.04-in. steps. In addition, the unit provides two analog outputs with 0 to 10V dc and 4- to 20-mA ranges. A 215-kHz piezoceramic transducer generates a 10°beam that covers a range of 5.9 to 59 in.

A $1603 integral version, which has the electronics and transducer enclosed in an aluminum housing, has the capability of manually rotating the sensor 360°. A $1627 remote version, which has the transducer remotely wired to the housing through a 39.4-in. cable, has a beam-concentrator accessory that narrows the beam width to 4° for sensing objects within a range of 2 to 79 in. The beam-concentrator accessory costs $45.

Ultrasonic-ranging systems are also available as computer-board products and with RS-232C interfaces for communicating with a computer or a terminal. Contac Technologies Corp manufactures one distance-measuring plug-in board for the IBM PC bus (the UDM-PC) and one for the STD Bus (the UDM-STD).

The boards interface with the Po-

accuracy, you can't use ultrasonic techniques in high or low air-pressure chambers. Sound cannot travel in a vacuum.

Sound pollution is one other possible source of error in an ultrasonic-ranging system. You should take care that external noise sources do not generate ultrasonic harmonics that the receiver will detect.

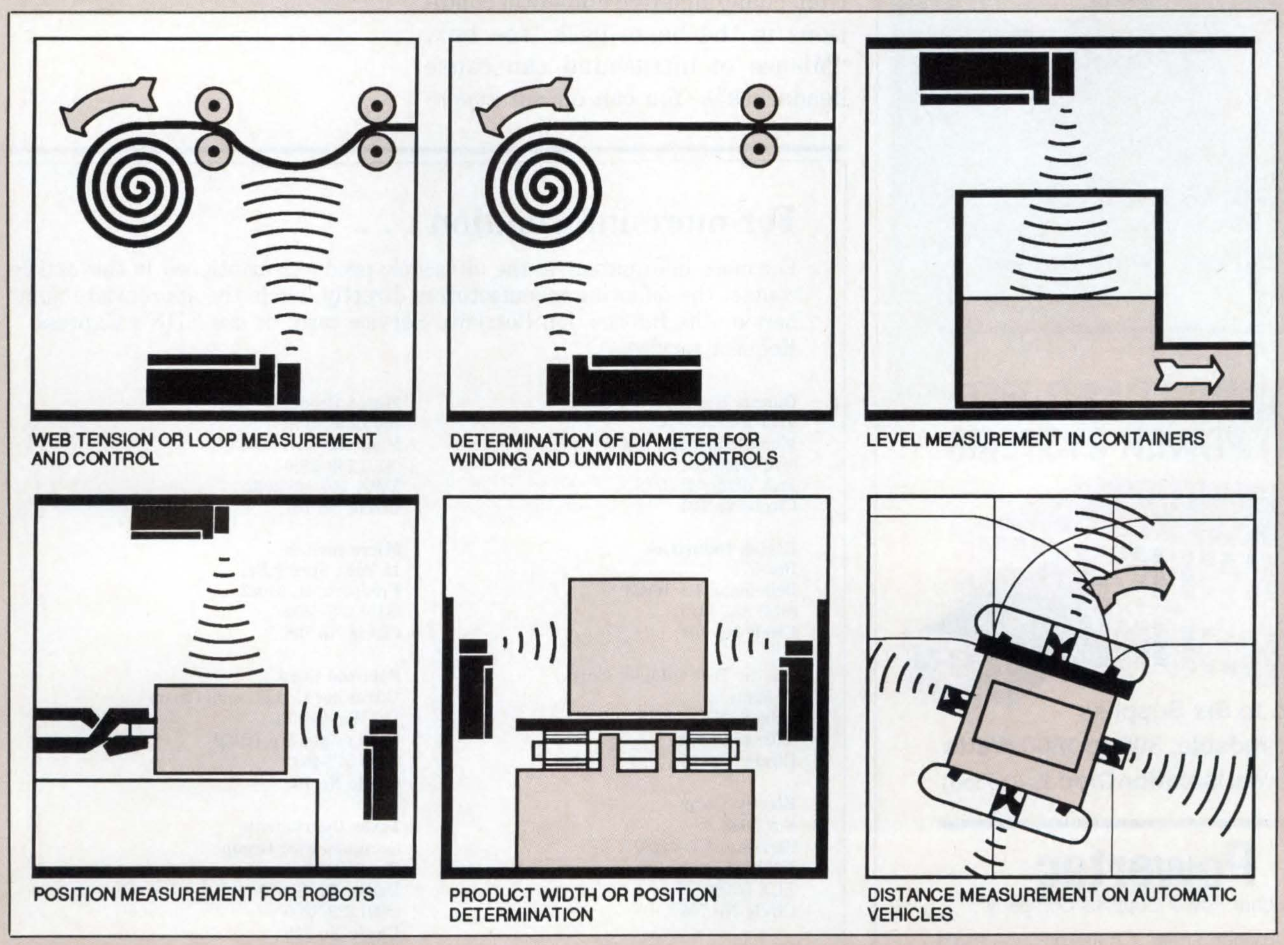



***Fig A—Ultrasonic ranging is well-suited*** *to a number of applications (courtesy Micro Switch, a Honeywell Div).*

laroid transducer and provide range detection from 6 in. to 35 ft with a resolution of 0.05 in. and an accuracy of ±1%. The IBM PC product comes with I/O driver software and demonstration programs on a floppy disk. The STD bus product can either operate in a stand-alone mode or respond to jumper-selectable interrupts. A $369 multiplexer board is available for interfacing as many as seven ultrasonic transducers to the UDM-PC and -STD boards. The two boards sell for $436 and $369, respectively.

A similar computer product, the UDM-RMU, can interface two ultrasonic transducers to an RS-232C port communicating at 9600 baud. The $495 remote unit gets its power from a wall-mounted power supply and measures 6.5×3.5×1.38 in.

Although ultrasonic techniques are well matched to certain measurement applications, they suffer from changing environmental conditions in the beam path (see **box**, "Misuse of ultrasound can cause headaches"). You can obtain *expensive* ultrasonic ranging systems that include elaborate environmental-compensation techniques, but these types of systems are not within the focus of this article. Therefore, you may have to resort to some imaginative signal processing. Fortunately, you can solve many of these problems, or lessen their effect, by using μprocessor techniques and look-up tables for temperature, atmospheric pressure, and humidity-compensation data. **EDN**

**Article Interest Quotient**
**(Circle One)**
**High 518 Medium 519 Low 520**

## For more information . . .

For more information on the ultrasonic products mentioned in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

**Banner Engineering Corp**
9714 10th Ave N
Minneapolis, MN 55441
(612) 544-3164
FAX (612) 544-3213
**Circle No 703**

**Blatek Industries**
Box 574
Bellefonte, PA 16823
(814) 355-4910
**Circle No 704**

**Contac Technologies Corp**
15 Main St
Bristol, VT 05443
(802) 453-3332
**Circle No 705**

**Electro Corp**
Box 3049
Sarasota, FL 34230
(813) 355-8411
TLX 52683
**Circle No 706**

**Massa Products Corp**
280 Lincoln St
Hingham, MA 02043
(617) 749-4800
TWX 710-348-6932
**Circle No 707**

**Micro Switch**
11 West Spring St
Freeport, IL 61032
(815) 235-6600
**Circle No 708**

**Polaroid Corp**
Ultrasonic Components Group
119 Windsor St
Cambridge, MA 02139
(617) 577-4681
**Circle No 709**

**Texas Instruments**
Semiconductor Group
Box 809066
Dallas, TX 75380
(800) 232-3200
**Circle No 710**

# DRAMs, SRAMs, EEPROMs, CMOS Logic, Flash Converters, SOT-23s, Linear, MOSFETs:

Samsung sets the pace.

# Samsung. Setting the pace.

Samsung is a leading semiconductor company with worldwide resources. In process, design and manufacturing, we're setting the pace for the industry.

To date, Samsung has invested more than $600 million in the development of new products. By 1989, this will have grown to one billion dollars. Such commitment will place Samsung among the top ten producers in the world by the beginning of the next decade.

Samsung is a leader in the manufacture of products utilizing state-of-the-art CMOS processes. Our 6-inch wafer fabrication lines in Korea are some of the most advanced in existence, as is our Class I wafer fab facility in San Jose, the heart of Silicon Valley. Not only are we able to produce such leading edge products as DRAMs, SRAMs, CMOS Programmable Logic and Advanced CMOS Logic, but we produce them in high volume at low cost.

Samsung maintains advanced R&D facilities in Kiheung and Bucheon, Korea and in San Jose, California. At each of these facilities we have not only created our own advanced designs for current products, but we are at work now on our 4-megabit DRAM and our 1-megabit SRAM designs.

As you read on, one thing will be clear: Samsung is committed to designing, developing and delivering sophisticated products.

Products that set the pace.

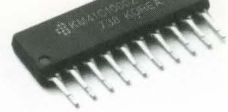

*Samsung's sophisticated manufacturing facility at Bucheon employs internally-developed Advanced CMOS and Bipolar processes.*

*Samsung's high-volume manufacturing facility at Kiheung has one of the world's most advanced 6-inch wafer fabrication lines.*

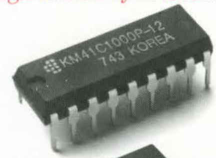
*Samsung's World Headquarters in Seoul is the center of a global organization comprised of 26 companies which operate worldwide.*

*Samsung's U.S. Headquarters in San Jose includes Engineering, Marketing, Sales and Administration and also boasts state-of-the-art R&D and Class 1 manufacturing wafer fabrication.*

# Samsung's new 1Mb DRAMs set today's fast memory pace.



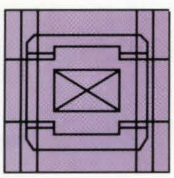
*In the 1Mb DRAM, Samsung's pacesetting CMOS technology provides superior immunity to electrostatic discharge, lower soft error rates and high immunity to latchup.*



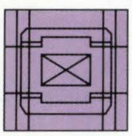
The KM41C100X and KM44C25X series of one-megabit DRAMs in CMOS technology are our latest high-density memory offerings. Fabricated using Samsung's internally developed CMOS technology, they feature line widths as fine as 1 $\mu$m.

This leading technology enables us to offer a device with very low power consumption and high-speed access times. Our pace setting DRAMs are designed for computing applications from mainframes and minis to high performance graphics stations and work stations, as well as for instruments and telecommunications products.

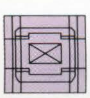
*Samsung technology has evolved from 2.5 micron to sub-micron in just four years.*



**1984-64K**
117$\mu^2$ cell size
2.5$\mu$m geometry



**1985-256K**
62.5$\mu^2$ cell size
1.6$\mu$m geometry



**1987-1Mb**
27$\mu^2$ cell size
1.0$\mu$m geometry

**1988-4Mb**
10.25$\mu^2$ cell size
0.8$\mu$m geometry

Our 1Mb DRAMs are manufactured in production volumes at our 6-inch wafer fabrication facility, considered to be one of the most advanced of its kind, using very high-resolution steppers and state-of-the-art etching and implantation equipment. Samsung is adding DRAM wafer capacity with a new 6-inch facility which will be equipped to manufacture our 4Mb DRAM.

Samsung 1Mb DRAMs are available in a wide variety of options and organizations. We offer a choice of 256K x 4 or 1M x 1 organizations with features like Fast Page, Nibble and Static Column modes. With the addition of the 1Mb to the 64K and 256K, Samsung's dynamic RAMs cover the entire range of densities and organizations.

All are available in plastic DIP, ZIP, and SOJ or PLCC industry standard packages.

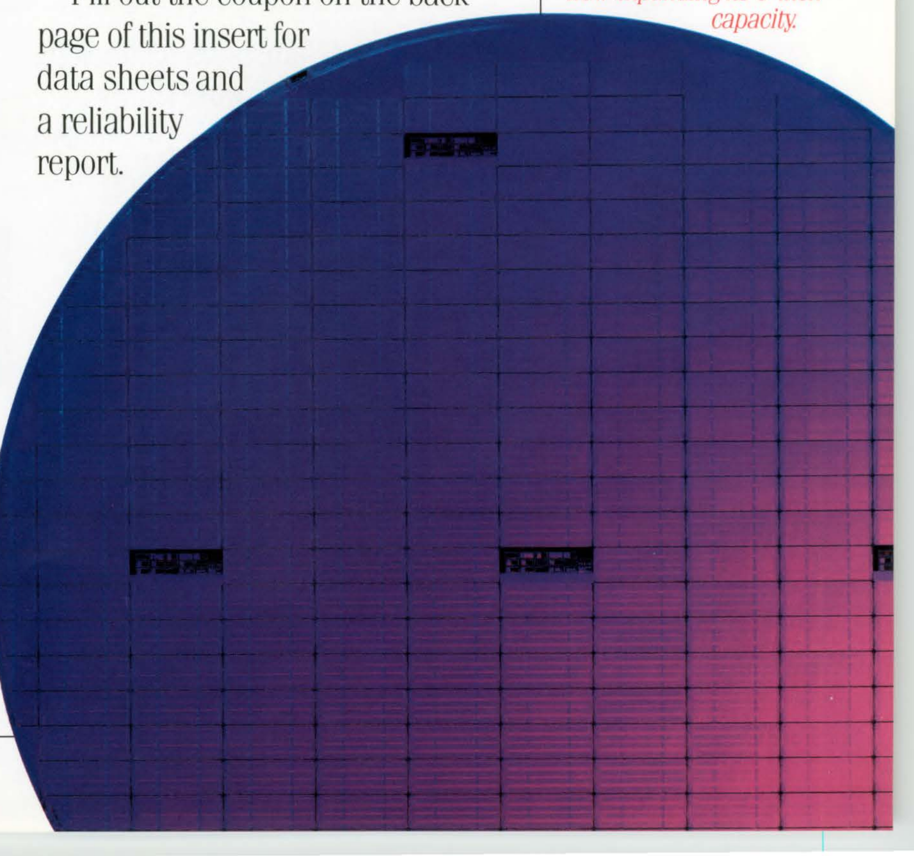
Our packaging technology is not limited to components. Samsung SIP and SIMM memory modules for the 256K and 1Mb DRAMs offer a cost effective method of utilizing surface mount technology to increase board density.

| Part Type | Organ. | Features | Speeds | Packages | Avail. |
|---|---|---|---|---|---|
| KM41C1000 | 1M x 1 | Fast Page mode | 100,120 | DIP, ZIP, SOJ | Now |
| KM41C1001 | 1M x 1 | Nibble mode | 100,120 | DIP, ZIP, SOJ | 2Q '88* |
| KM41C1002 | 1M x 1 | Static Column mode | 100,120 | DIP, ZIP, SOJ | 2Q '88* |
| KM44C256 | 256K x 4 | Fast Page mode | 100,120 | DIP, ZIP, SOJ | 2Q '88 |
| KM44C258 | 256K x 4 | Static Column mode | 100,120 | DIP, ZIP, SOJ | 2Q '88 |
| KM41256 | 256K x 1 | Page mode | 120,150 | DIP, ZIP, PLCC | Now |
| KM41257 | 256 x 1 | Nibble mode | 120,150 | DIP, ZIP, PLCC | Now |
| KM41464 | 64K x 4 | Page mode | 120,150 | DIP, ZIP, PLCC | Now |
| KM4164 | 64K x 1 | Page mode | 120,150 | DIP | Now |
| KMM48/9256 | 256K x 8/9 | Page or Nibble modes | 120,150 | SIP module | Now |
| KMM58/9256 | 256K x 8/9 | Page or Nibble modes | 120,150 | SIMM module | Now |
| KMM48/91000 | 1M x 8/9 | Fast Page mode | 100,120 | SIP module | 2Q '88 |
| KMM58/91000 | 1M x 8/9 | Fast Page mode | 100,120 | SIMM module | 2Q '88 |

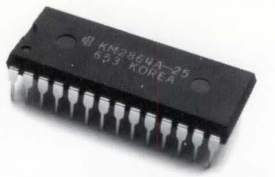
*Samples available now.

Fill out the coupon on the back page of this insert for data sheets and a reliability report.

*Samsung's 6-inch wafer fabrication facility in Kiheung is one of the most advanced in the world, boasting a Class 10 level clean room. Samsung is now expanding its 6-inch capacity.*



Circle No. 167




*Advanced Samsung 16K and 64K EEPROMs are now available in production quantities.*

# Samsung EEPROMs also outpace industry standards.

Samsung's 64K and 16K EEPROMs meet or surpass all industry standards for performance, reliability and quality. They have standard endurance ratings of 10,000 erase/write cycles and data retention ratings of 10 years.

And our "H" version 64Ks offer a quick 2 millisecond per byte write time, reducing write time by a factor of 5.

| Part Type | Organi-zation | Speed | Features | Tech-nology | Pinout | Avail-ability |
|---|---|---|---|---|---|---|
| KM2816AP | 2K x 8 | 250,300,350 | 10ms (max) write time | NMOS | 24 pin | Now |
| KM2817AP | 2K x 8 | 250,300,350 | Ready/Busy, 10ms (max) write time | NMOS | 28 pin | Now |
| KM2864AP | 8K x 8 | 250,300,350 | Data Polling, 10ms (max) write time | NMOS | 28 pin | Now |
| KM2865AP | 8K x 8 | 250,300,350 | Data Polling, Ready/Busy, 10ms (max) write time | NMOS | 28 pin | Now |
| KM2864AHP | 8K x 8 | 250,300,350 | Data Polling, 2ms (max) write time | NMOS | 28 pin | Now |
| KM2865AHP | 8K x 8 | 250,300,350 | Data Polling, Ready/Busy, 2ms (max) write time | NMOS | 28 pin | Now |
| KM28C64P | 8K x 8 | 150,200,250 | Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time | CMOS | 28 pin | May '88* |
| KM28C65P | 8K x 8 | 150,200,250 | Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time | CMOS | 28 pin | May '88* |

*Samples available now.

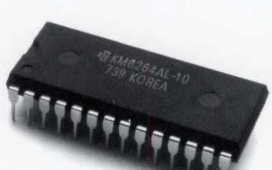
Our new 64K KM28C64 series (available 2nd quarter 1988) is fabricated with our pacesetting floating gate CMOS processing. It features low power dissipation of 100$\mu$A standby and access times of 150ns, 200ns and 250ns. These advanced 8K x 8 EEPROMs also feature a 32-byte page mode to slash write times to 150 microseconds per byte and a 5-millisecond write cycle. This allows the entire 64K memory to be written in only 1.3 seconds.

Samsung's EEPROMs excel in such rugged applications as communications, instrumentation, robotics and industrial control. All our EEPROMs meet JEDEC pinout standards.

Fill out the coupon on the back page of this insert for samples, a data sheet, and reliability report.

Circle No. 168


*Samsung's 256K (32K x 8) KM62256 SRAMs are available with access times of 100ns, 120ns and 150ns, all in low-power versions with standby current of only 4$\mu$A (typical).*




*Samsung SRAMs are fabricated using 1.2 $\mu$m CMOS technology. In 1988, we are ramping up 256K and 64K SRAM production.*

# The fast pace continues with Samsung low power SRAMs.

The pace of Samsung's technology development in static RAMs is as strong as it is for all our memory products. With the introduction of the KM62256 (32K x 8) SRAM Family, we now offer a wide low power CMOS SRAM line, including our KM6264A industry standard 64K SRAMs.

The KM62256 256K SRAM is fabricated using our internally developed 1.2 $\mu$m CMOS technology which meets both high speed and low power requirements. We offer 80ns 64K SRAMs and 100ns 256K SRAMs in high volume. They're ideal for process control, medical instruments, and hand held devices.

Samsung is ramping up production of both the 256K and 64K CMOS SRAMs. Our complete line is available now in industry standard packages and pinouts.

| Part Type | KM62256L | KM6264AL |
|---|---|---|
| Organization | 32K x 8 | 8K x 8 |
| Speeds | 100, 120, 150ns | 80, 100, 120ns |
| Package | 28 DIP | 28 DIP |
| Max Current (standby) | 100$\mu$A | 100$\mu$A |
| Availability | Now | Now |

Fill out the coupon on the back page of this insert for a data sheet and reliability report.

Circle No. 169

# Samsung Advanced AHCT CMOS Logic Family keeps pace with the fastest 16- and 32-bit microprocessors.



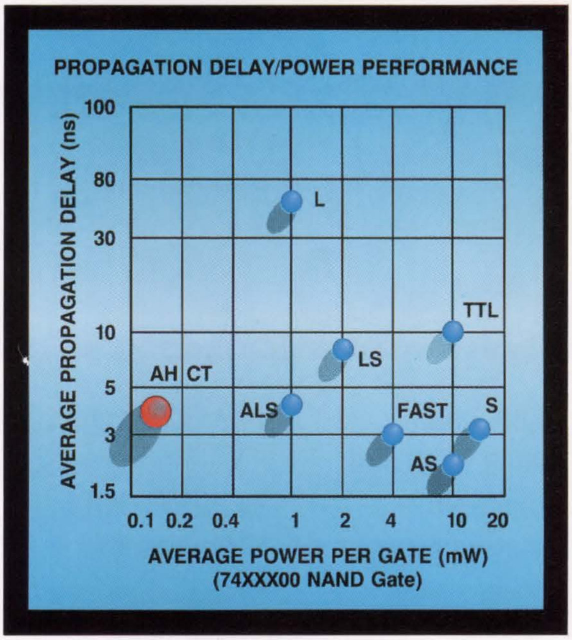
*Samsung's Advanced CMOS Logic is available in both DIP and SOIC packages.*

Available now in production quantities, our Advanced AHCT CMOS Logic Family meets the demands of your 16- and 32-bit designs for high speed, high drive and low power.

Samsung has 111 of the most popular standard logic functions available off the shelf now, with samples free for the asking. By mid-year, we will add another 50 part types to the list. This means you can design our part into your product and move into production now with no waiting.

For power reduction in your existing designs, AHCT offers pin-for-pin, part-for-part replacement for ALS and FAST.™ It fits right in and reduces power tenfold. Yet our AHCT doesn't have a premium price. It costs the same as ALS.

Fill out the coupon on the back page of this insert for free samples and a data book.




Circle No. 170

**KS74AHCT PARTS LIST**

**Gates and Inverters**

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| 00 | 20 |
| 01 | 21 |
| 02 | 22 |
| 03 | 27 |
| 04 | 30 |
| 05 | 32 |
| 08 | 51 |
| 09 | 58 |
| 10 | 86 |
| 11 | 132 |
| 12 | 133 |
| 14 | 266 |

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|---|---|
| 125 | 367 |
| 126 | 368 |
| 210 | 465* |
| 240 | 466* |
| 241 | 467* |
| 244 | 468* |
| 365 | 540 |
| 366 | 541 |

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|---|---|
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| 74 | 534 |
| 76 | 564 |
| 78 | 574 |
| 107 | 670 |
| 109 | 794* |
| 112 | 821* |
| 173 | 822* |
| 174 | 823* |
| 175 | 824* |
| 273 | 825* |
| 374 | 826* |
| 377 | |

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|---|---|
| 75* | 793* |
| 77* | 841* |
| 259 | 842* |
| 373 | 843* |
| 533 | 844* |
| 563 | 845* |
| 573 | 846* |

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| | | |
|---|---|---|
| 242* | 643 | 652* |
| 243* | 645 | 658* |
| 245 | 646 | 659* |
| 640 | 648 | 664* |
| | 651* | 665* |

**Counters**

| | | |
|---|---|---|
| 160 | 190 | 590* |
| 161 | 191 | 591* |
| 162 | 192 | 592* |
| 163 | 193 | 593* |
| 168 | 390* | |
| 169 | 393 | |

**Decoders/Encoders**

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|---|---|---|
| 42 | 148* | 238 |
| 138 | 154 | 239 |
| 139 | 155 | |

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|---|---|---|
| 121* | 123* | 423* |

**Logic Level Converters**

| | |
|---|---|
| 4049 | 4050* |

**Multiplexers**

| | |
|---|---|
| 151 | 253 |
| 153 | 257 |
| 157 | 258 |
| 158 | 352 |
| 251 | 353 |

**Shift Registers**

| | |
|---|---|
| 164 | 299 |
| 165 | 595 |
| 166 | 596 |
| 194 | 597 |
| 195 | |

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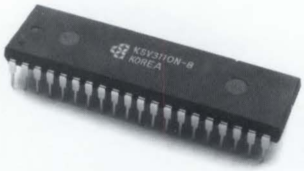
|---|---|
| 181* | 522* |
| 182* | 679 |
| 183 | 680 |
| 280 | 682 |
| 518* | 684* |
| 519 | 686* |
| 520* | 688 |
| 521 | 689* |

*Part types available in 2Q '88. All other part types available now.

*FAST is a trademark of Fairchild Semiconductor, Inc.*



*KSV3110 Combo A/D-D/A Flash Converter*

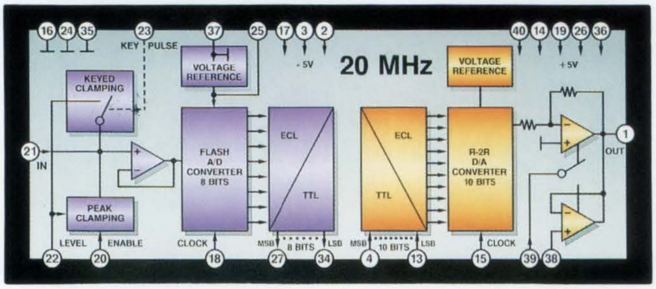
*KSV3208 A/D Flash Converter*

# Samsung's KSV3110 combo A/D-D/A and KSV3208 A/D set the pace in flash converters.

The pacesetting technology of our single-chip KSV3110 A/D-D/A data converter provides independent 8-bit A/D converter functions and 10-bit R-2R D/A converter functions over an operating range of DC to 20MHz.

With the ease of design you get with the KSV3110's two chips in one, you'll save both money and real estate, leaving room and resources to add other features. And having fewer parts cuts down power drain and boosts system reliability.

The KSV3110 gives TTL-compatible input/output, 1% absolute non-linearity and selectable peak level input or keyed clamping.




The impressive linear characteristics of the KSV3110 are shared by our new KSV3208 A/D flash converter. It provides the same features for applications that don't require D/A conversion.

Samsung also offers the support chips to ease the integration of the KSV3110 into video applications. For example:

- KA2606 Sync Separate IC
- KA2153 Chrominance Signal Processor for NTSC systems
- KA2154 Video Chroma Deflection System for NTSC and PAL systems

Fill out the coupon on the back page of this insert for samples and a Flash Converter IC Data Book.

Circle No. 171

| Part Type | Resolution A/D | Resolution D/A | Linearity A/D | Linearity D/A | Conversion Speed | Industry Part |
|---|---|---|---|---|---|---|
| KSV3110N-10 | 8 bits | 10 bits | ± ½ LSB | ± ½ LSB | 20 MSPS | |
| KSV3110N-9 | 8 bits | 10 bits | ± ½ LSB | ± 1 LSB | 20 MSPS | |
| KSV3110N-8 | 8 bits | 10 bits | ± ½ LSB | ± 2 LSB | 20 MSPS | |
| KSV3110N-7 | 8 bits | 10 bits | ± ½ LSB | ± 4 LSB | 20 MSPS | |
| KSV3100AN-8 | 8 bits | 10 bits | ± ½ LSB | ± 2 LSB | 20 MSPS | UVC3101 |
| KSV3100AN-7 | 8 bits | 10 bits | ± ½ LSB | ± 4 LSB | 20 MSPS | UVC3101 |
| KSV3208N | 8 bits | | ± ½ LSB | | 20 MSPS | |
| KAD0820ACN | 8 bits | | ± ½ LSB | | 1.5 μsec | ADC0820BCN |
| KAD0820BCN | 8 bits | | ± 1 LSB | | 1.5 μsec | ADC0820CCN |
| KAD0808IN | 8 bits | | ± ½ LSB | | 100 μsec | ADC0808CCN |
| KAD0809IN | 8 bits | | ± 1 LSB | | 100 μsec | ADC0809CCN |
| KDA0800CN | | 8 bits | | ± ½ LSB | *100 nsec | DAC0800LCN |
| KDA0801CN | | 8 bits | | ± 1 LSB | *100 nsec | DAC0801LCN |
| KDA0802CN | | 8 bits | | ± ¼ LSB | *100 nsec | DAC0802LCN |
| KDA0806CN | | 8 bits | | ± 2 LSB | *150 nsec | DAC0806LCN |
| KDA0807CN | | 8 bits | | ± 1 LSB | *150 nsec | DAC0807LCN |
| KDA0808CN | | 8 bits | | ± ½ LSB | *150 nsec | DAC0808LCN |
| KS7126CN | 3½ digit | | ± ½ LSB | | 333 msec | TSC7126 |
| KS25C02 | CMOS 8-bit successive approx. register | | | | | DM2502 |
| KS25C03 | CMOS 8-bit successive approx. register | | | | | DM2503 |
| KS25C04 | CMOS 12-bit successive approx. register | | | | | DM2504 |

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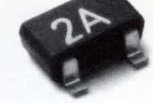

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**SOT-23 PART TYPES**

| | | |
|---|---|---|
| MMBR5179 | MMBT5087 | MMBTA55 |
| MMBT2222A | MMBT5088 | MMBTA56 |
| MMBT2484 | MMBT5401 | MMBTA63 |
| MMBT2907A | MMBT5550 | MMBTA64 |
| MMBT3904 | MMBT6428 | MMBTA70 |
| MMBT3906 | MMBTA05 | MMBTA92 |
| MMBT4123 | MMBTA06 | MMBTA93 |
| MMBT4124 | MMBTA13 | MMBTH10 |
| MMBT4125 | MMBTA14 | MMBTH17 |
| MMBT4126 | MMBTA20 | MMBTH24 |
| MMBT4401 | MMBTA42 | BCX70G |
| MMBT4403 | MMBTA43 | BCX71G |

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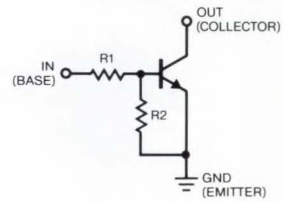
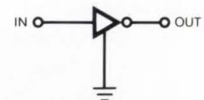
Internal Circuit




Function

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MC1458CN*
MC4558CN*
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KS273 (TLC273)

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KA2418N—Tone ringer with bridge diode
KA2412FN—Speech network
KA2413N—DTMF
KS5808N—DTMF
KS5805AN/BN—Pulse dialer
KS5819N—Pulse/DTMF (22 DIP)
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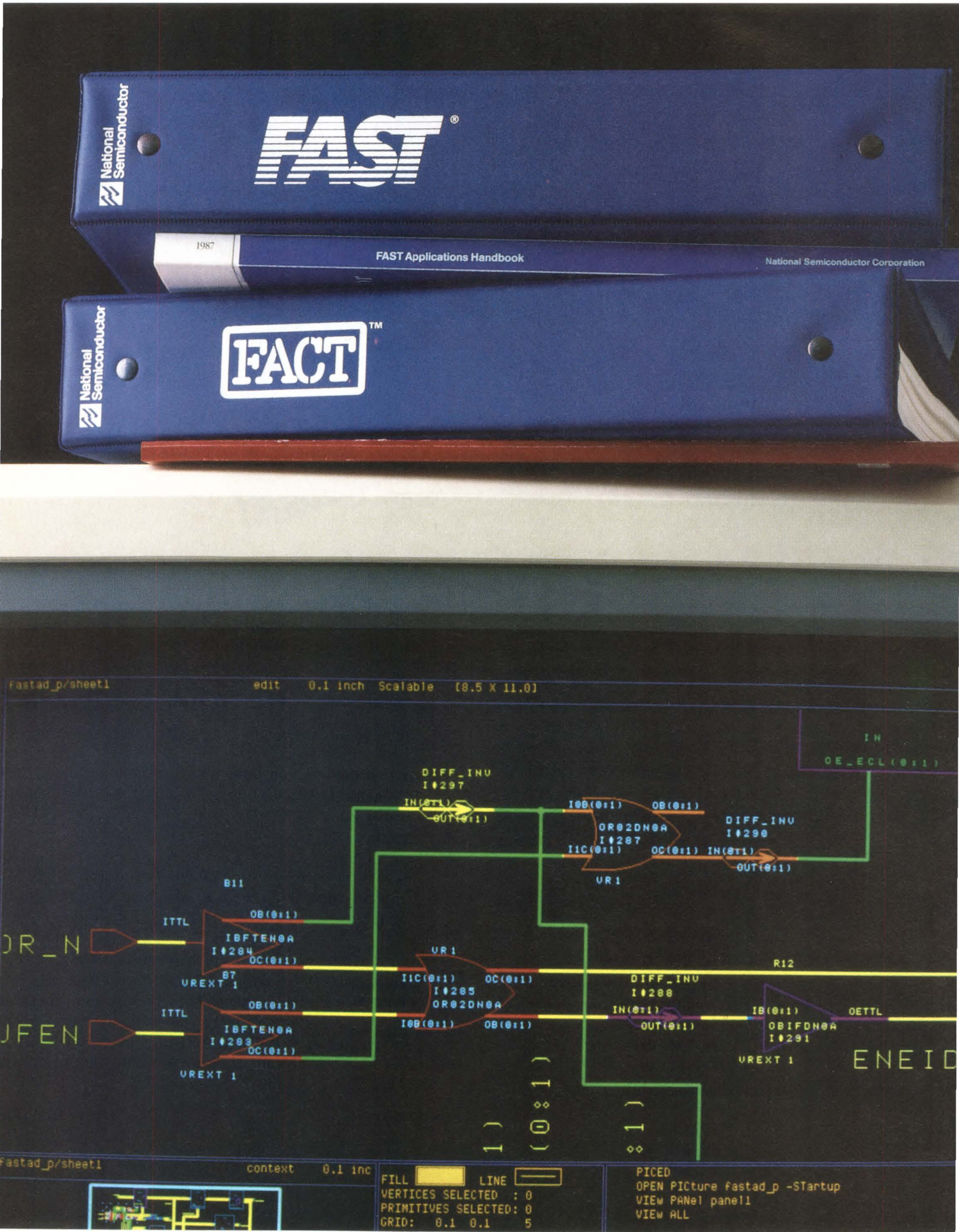
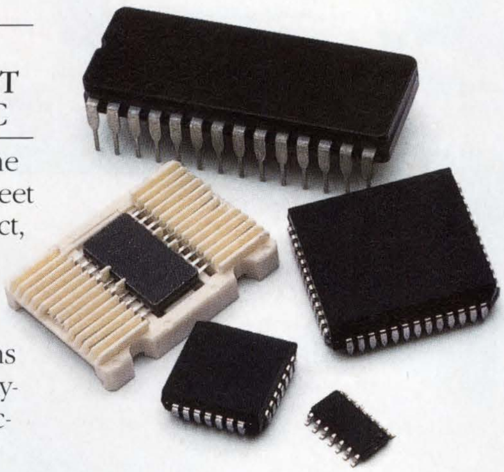


# The logic in choosing National.



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- an integrated PC to VAX solution in November 1985
- a PC as an intelligent graphics terminal for CAE in February 1986
- a complete Sun Workstation-based CAE solution in October 1986

In 1986, CASE also announced major marketing agreements with Digital Equipment Corporation and Sun Microsystems for the joint promotion of the Vanguard CAE Design System on the VAXstation and Sun-3 series of high performance engineering workstations.

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**CASE TECHNOLOGY**

**CIRCLE NO 123**

# Function libraries can expedite the development of application programs

Chris Terry, *Associate Editor*

Portability, connectivity, and productivity. These three concepts are tossed about so freely today that they are in danger of losing their significance. But if you're designing applications software for the microcomputer market, you need to achieve a certain level of success in all three areas—and that's where function libraries can play a very useful part.

You need portability because your customers may be using anything from a 1982 clunker running MS-DOS 1.1 to a lightning-fast 80386 machine running PC-DOS 3.3 or even OS/2. You need connectivity because users who travel don't want to waste time exiting from your application to bring up Crosstalk or Relay Gold. They want to be able to dial up the office computer from within their applications programs, send their data, and get right back to generating or analyzing more data. Finally, you need productivity to get your software to the market before someone else does—and that means not reinventing the wheel, however graceful and elegant your version of the wheel might be.

It's likely that one of the many available libraries of C, Pascal, or Basic functions can help you meet all three of the goals for the development of successful applications programs. Most of the libraries provide a wide range of both general and special functions at prices that range from $50 to $500. If you're writing for the IBM PC or PS/2 families and compatibles, you'll find that almost every library contains routines for screen handling, pop-up menus, and windows. Some libraries offer completely independent windowing functions; others have an interface to the Microsoft Windows package, with plans for interfacing to the OS/2 Presentation Manager when that is released.

Typical of these general libraries is the C-Worthy Interface Library (Solution Systems), which costs $195 for object code only and $495 for object code with forms interface and library source code. You can order this library to work with the C compilers from Microsoft, Borland International (Scotts Valley, CA), or Lattice (Lombard, IL). It contains more than 350 C functions and 75 functions written in assembly language. The library also has menu functions; 62 DOS interface functions (including file-handling, directory, and time and date conversions); system and context-sensitive help functions; screen-handling and windowing functions; and a form-interface library for database applications.

The interface library is useful if you have overseas customers, because all the messages are isolated in separate files so that you can, if you wish, translate them into foreign languages. The package does not, however, have any communications functions.

> **You don't have to write validation routines for a data-entry system. Instead you can use pretested date, numerical, and value-range validation routines.**

Two of the most comprehensive library collections are those from Greenleaf Software and Essential Software. Both of these collections do offer communications libraries that are available separately, but, for the sake of consistency, it's probably best to use them in conjunction with the general functions.

Greenleaf Functions, version 3.10, is the set's general library and contains 297 C functions that cover all DOS and BIOS capabilities, string handling, serial ports, graphics, printers, random numbers, clock/calendar handling and time and date conversions, and system interfacing (including interrupt handling). Another library, named Datawindows, provides all the C functions you need for a complete data-entry system. Object code for the general library costs $185; for Datawindows, it costs $225; source code is extra, but you can order various money-saving combinations of these libraries with or without source code.

The Greenleaf Comm library ($185) contains about 120 routines that are completely compatible with those of both the general library and Datawindows and ensure that, when the user terminates an application, an orderly exit to the operating system is guaranteed. If your system contains a multiport expansion board from Digiboard Inc (St

# 0 to 60 in 5 seconds


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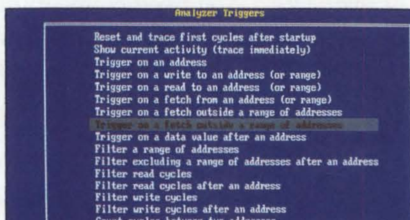


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Louis Park, MN), you can open and close as many as eight serial ports and define all port parameters.

**Controlling modems**

Status functions let you determine the status of the line, of the modem, of the buffer, and of other important flags and semaphores; you can also customize some of these routines so that the system ignores certain types of errors. In addition, timing and timer functions are included. A comprehensive set of modem-control functions lets you control all the operations of Hayes-compatible intelligent modems.

**Protocol sequences available**

You don't have to construct protocol sequences from these basic building blocks; the communications library includes block- and file-level protocol sequences that you can call in order to transfer files in either direction using XON/XOFF or hardware RTS/CTS flow control, or the XMODEM protocol, which is the widely used public-domain protocol originated by Ward Christensen for user-group bulletin boards.

It's a pity that the Greenleaf Comm library supports only the XMODEM checksum error-detection scheme. This scheme detects only 99.2% of transmission errors, whereas the later CRC scheme detects 99.997% and it's not much more complex. Most public-domain communications programs and many commercial programs that implement XMODEM use CRC as the primary mode, and fall back to checksum mode only if the computer at the other end of the line can't provide the CRC mode.

The Essential Software collection of C functions offers some capabilities that other collections do not. The C Utility Library ($185) has system, screen-handling, and graphics routines that differ little from those of the other collections; it also contains functions that initialize the COM: ports to the desired word format and data rate, and that let you transfer asynchronous characters to and from either port.

**Advanced graphics applications**

Essential Graphics sells for $299 and has all the functions that you need for advanced graphics applications; it supports a wide variety of displays and hard-copy devices. One distinctive library in this group is ResidenC, a tool kit for the development of TSR (terminate and stay resident) programs. Another library, Screenstar, lets you design easy-to-use screens and menus and validate all keyboard input according to the requirements of individual fields (eg numerical, character, date, phone number). ResidenC and Screenstar each cost $99.

The Essential Communications library contains functions that let you communicate, at speeds as fast as 9600 bps, with any asynchronous RS-232C device via the PC's COM: ports. In addition to functions for setup and for setting the port parameters, this library has services for keyboards, screens, low-level interrupts, and timers. In addition, a complete set of functions for controlling Hayes-compatible intelligent modems is included; flow-control functions allow you to use hardware RTS/CTS handshaking or XON/XOFF flow control; and a set of higher level functions implements the XMODEM protocol with CRC error detection. You can buy this library for $185. A supplementary debugger, named Breakout, is unique to this collection. It allows you to turn your PC into a data-line monitor that detects most setup and transmission errors (such as speed mismatch or incorrect RS-232C cable connections) and that also scans the XMODEM protocol interactively. The debugger costs $125.

The Entelekon collection is large, and, although it doesn't include any communications functions, it's comprehensive enough for most purposes. The C Function Library contains more than 500 C functions divided into 12 groups: 18 system-status and -control functions; 70 string functions, 24 cursor-control functions; 47 keyboard-control and data-entry management functions; 28 time-related functions; 30 general utility functions such as numerical format-conversion routines; 86 video-control functions; 15 graphics functions; 6 linked-list operations for linking, unlinking, and finding records in doubly linked lists; 88 printer-control functions; and 18 functions for constructing menus and validating keyboard input. The $159.95 price includes all source code.

**Windowing power**

The C Power Windows library provides functions for constructing as many windows as you like (only the size of available memory sets a limit). When purchased alone, it costs $159.95. You can obtain the C Functions Library and Power Windows, together with a library of Superfonts for C, on 20 diskettes, for $199.95.

A third library in this collection is the B-Tree Library and ISAM (Indexed Sequential Access Method)

> If you need communications capability, look for a library that has modem-handling functions both for bare-bones modems and Hayes-compatible modems.

driver, which lets you construct a B-tree database manager with as many as 16.7 million records per file and the same number of keys. The functions include facilities for constructing indexes and finding keys by Boolean selection.

According to the vendor, the functions in these libraries complement, rather than duplicate, the functions found in libraries supplied with the Borland and Microsoft C compilers. Furthermore, a few complex, multipurpose functions, which you can call by means of macros, considerably reduce the size of the code that you finally incorporate into your application programs.

**A low-priced C alternative**

A comprehensive but reasonably priced collection of C functions comes from Zortech. All of the libraries are intended for use with Borland's Turbo C or Microsoft's Quick C. The company also supplies a C compiler, and a $295 C video tutorial on ten 1-hour tapes. Hotkey is a tool kit for TSR programs; Supertext is a text editor that is compatible with Wordstar; Proscreen lets you draw data-entry screens to suit your application and then generates the C source code to implement them. Windows lets you design any number of windows into your application. Finally, Games furnishes the source code for various games, including chess and backgammon. Each of these libraries costs $49.95, including source code.

The cream of the collection is Comms, which also costs $49.95 and contains not only a full set of modem-control functions for Hayes-compatible intelligent modems, but also various functions that emulate VT52, VT100, and ANSI terminals. You can use as many as eight serial ports. The basic functions support data rates as fast as 38.4k bps, but successful use of rates higher than 9600 bps depends on the efficiency of other parts of your applications program.

The character flow-control functions include hardware RTS/CTS and DTR/DSR handshaking, and XON/XOFF flow control. For block-mode transfers, you can choose the Kermit or XMODEM protocols. The XMODEM functions use CRC as the error-detection scheme, and automatically revert to checksum mode if the remote station does not support CRC. The distribution disk includes two demonstration programs.

The 121-page paperback manual for Comms presents a useful introduction to serial communications, and clear descriptions of each of the functions. Technically, it is well organized, comprehensive, and easy to use. However the manual is marred by a large number of typographical and grammatical errors, which tend to stop you cold and make you read a sentence again to be sure you understand it.

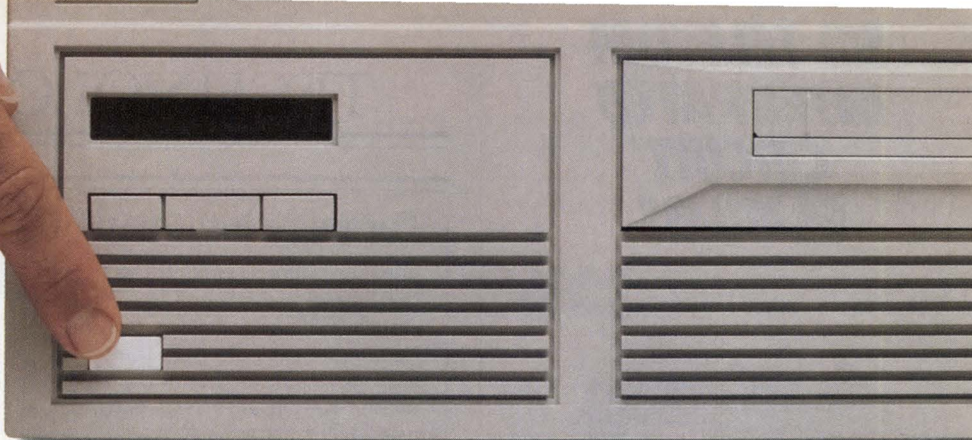
**You can sometimes mix-and-match functions from different libraries, but more often you're better off writing the few functions you lack.**

Libraries similar to the ones written in C are also available for Pascal programmers. Blaise Computing offers Power Tools Plus for $129. A set of general-purpose functions are designed to complement and enhance the libraries supplied with Borland's Turbo Pascal; Turbo C Tools, at the same price, is a similar set of tools for Borland's Turbo C or Microsoft's Quick C. Versions that work with Microsoft's C 5.0 and Pascal compilers are also available for $175 each.

C Asynch Manager and Pascal Asynch Manager furnish functions at several levels. At level 0 are the most basic hardware-control functions such as port initialization, interrupt services, and data transfers between the circular buffers and the ports. These functions are all written in assembly language. Using the functions at level 1, you can set port parameters, write characters to the output queue or read characters from the input queue, establish XON/XOFF flow control, and perform other relatively rudimentary operations. Level 2 contains the more complex operations involved in controlling Hayes-compatible intelligent modems and transferring files in block mode. Special functions allow you to implement the XMODEM protocol (with CRC error detection). C Asynch Manager and Pascal Asynch Manager cost $175 each.

**Few choices in Basic**

Not many general and specialized libraries are available for Basic, perhaps because Pascal and C are overtaking Basic in popularity for commercial application programs. One very good collection, however, is sold by Hammerly for $99. It's called ProBas, and it works with all versions of Microsoft's QuickBasic and Business Basic compilers, as well as IBM's BasCom compiler. The general ProBas library lets you use virtual screens and has a complete set of I/O routines written in assembly language and optimized for speed. This library also includes more than 200 high-level functions for screen control, file and string handling, data compression and expansion, and many other features. It has numerous low-level functions for serial-port initialization and



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## For more information

For more information on the function libraries discussed in this article, contact the following manufacturers directly, or circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

**Blaise Computing Inc**
2560 9th St, Suite 316
Berkeley, CA 94710
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**Circle No 711**

**Entelekon**
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Houston, TX 77024
(713) 468-4412
**Circle No 712**

**Essential Software Inc**
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S Orange, NJ 07079
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**Circle No 713**

**Greenleaf Software Inc**
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**Circle No 715**

**Solution Systems**
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**Circle No 716**

**Zortech Inc**
366 Massachusetts Ave
Arlington, MA 02174
(617) 646-6703
**Circle No 717**

character I/O, including checksum and CRC computations for error detection.

The Tele Comm Toolkit ($75) from the same collection contains high-level functions for the control of intelligent modems, for terminal emulation (VT52, VT100, and ANSI), and for file transfer using XMODEM protocol with both CRC and checksum error-detection modes. This library is unique in having the YMODEM protocol as well; although similar to XMODEM, it works at data rates from 300 to 38,400 bps (its predecessor causes problems at rates greater than 1200 bps).

### Know your library

Function libraries are well worth exploring. To maintain consistency, you should probably pick one that matches your compiler. And keep in mind that some libraries suit some applications areas better than others do. Then get to know your library really well. If you later find that you need functions that aren't in your library, you may be able to find them in a different collection. But you need to be careful: It's not always easy to assess if and how functions from different collections can work smoothly together. Unless you're a very skilled programmer and know both your language and your library inside out, mixing functions from different collections may give you more trouble than writing the missing functions yourself. **EDN**

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|---|---|---|---|---|---|---|---|---|
| MARKETS SERVED | SSI DEVICE NUMBER | 103 0-300 BPS | 212A 1200 BPS | V.21 0-300 BPS | V.22 600/ 1200 BPS | V.22 bis 1200/ 2400 BPS | V.23 0-1200 BPS | PRODUCT FEATURES |
| **UNIVERSAL APPLICATIONS** Stand-Alone or Integral Modem Designs | 73K212 | | | | | | | High performance single-chip modems with easy-to-use cost-effective features. |
| | 73K221 | | | | | | | |
| | 73K222 | | | | | | | |
| | 73K224 | | | | | | | |
| **LOW POWER APPLICATIONS** • Lap Tops • Portable Terminals • Line Powered Modems • Battery-Powered Units | 73K212L | | | | | | | High performance single-chip modems providing low-power operation from a single + 5 volt supply. |
| | 73K221L | | | | | | | |
| | 73K222L | | | | | | | |
| | 73K224L | | | | | | | |
| **DEDICATED INTEGRAL APPLICATIONS** • Bus-Oriented Systems • Credit Verification • Automatic Teller Machines • Pay Telephones • Diagnostic Equipment | 73K212U | | | | | | | Enhanced single-chip modems with a fully integrated 16C450 UART function, and added circuitry to simplify integral designs. |
| | 73K221U | | | | | | | |
| | 73K222U | | | | | | | |
| **EUROPEAN DATA COM APPLICATIONS** Multi-standard modems requiring videotex compatibility | 73K322* | | | | | | | Single-chip modems add V.23 and special features to standard operating modes; available in + 12 volt or + 5 volt versions. |
| | 73K322L* | | | | | | | |
| | 73K324* | | | | | | | |
| | 73K324L* | | | | | | | |

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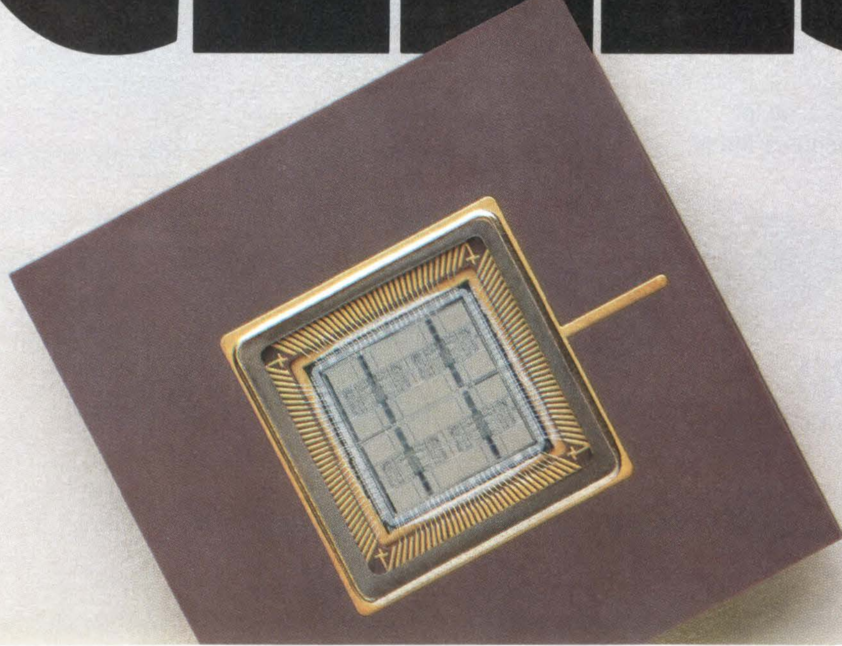

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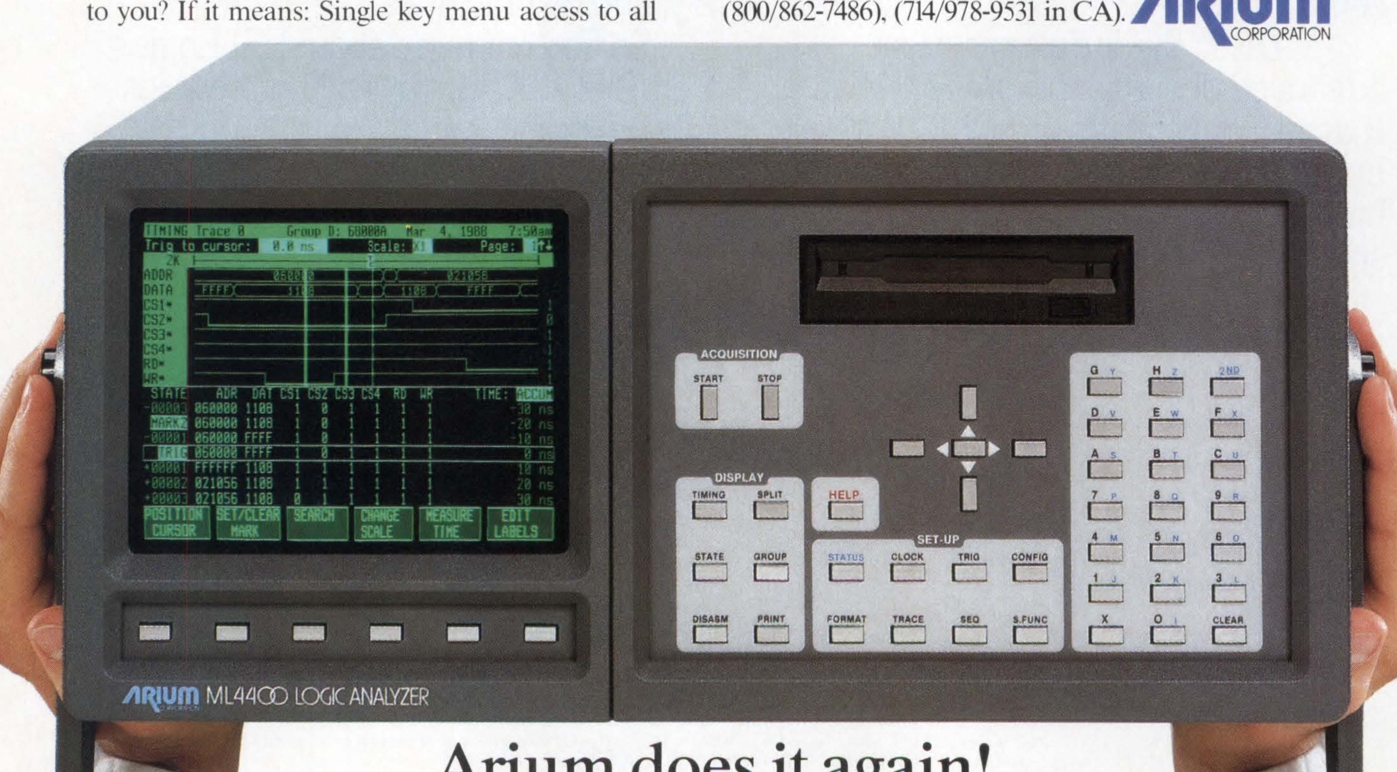
For more data on the new ML4400, as well as on our family of Arium 8/16/32-bit logic analyzers at prices as low as $2495, contact ARIUM CORPORATION, 1931 Wright Circle, Anaheim, CA 92806-6052. Telephone 800/TO-ARIUM (800/862-7486), (714/978-9531 in CA).

ARIUM CORPORATION




## Arium does it again!

CIRCLE NO 120

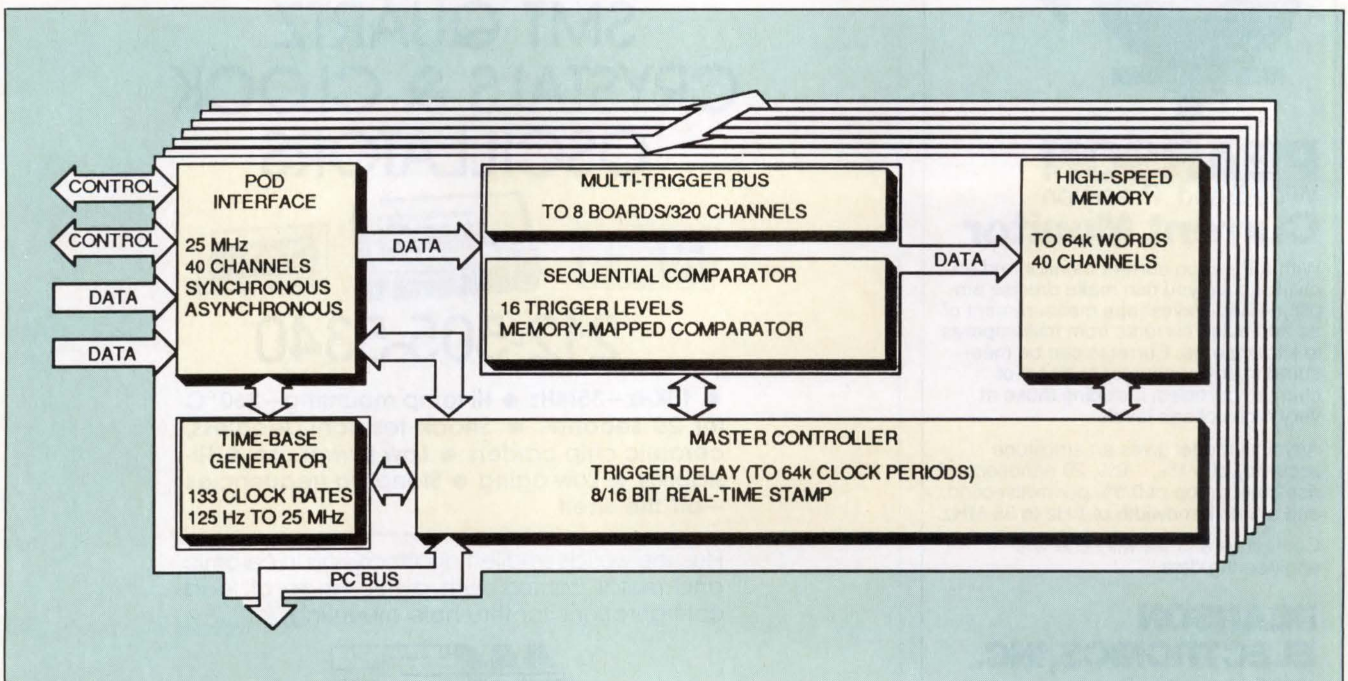
# Logic analyzer samples at 1 GHz and handles 320 channels with 64k-word memory

You can no longer regard logic analyzers that plug into the IBM PC Bus merely as tools for the debugging of 8-bit systems with modest clock speeds. With pricing that begins at $2995, the model 40, 80, and 320 logic analysis systems provide a combination of features heretofore associated with more expensive stand-alone instruments. Ranging from a 40-channel system with a 4k-word ROM to a 320-channel system with a 64k-word memory, the family's logic analysis systems perform 125-MHz timing analysis, incorporate a 16-level sequential-triggering scheme, and accept an optional pod that permits 1-GHz equivalent-time sampling of repetitive patterns.

Systems that have 160 or fewer channels include personal computers and are roughly the size of sewing machines. They incorporate backlit LCDs or, optionally, electroluminescent displays. The 40-channel system's computer is IBM PC/XT compatible and based on a 10-MHz 8088 μP; the PCs that come with the larger systems are IBM PC/AT compatible and employ 10-MHz 80286 μPs. You can configure custom systems by mounting logic analysis boards in PC- or PC/AT-compatible chassis. The vendor offers the logic analyzers with pattern generators, comparators, and test-development software as a low-cost automatic test system for complex devices and circuit boards.

To prevent future obsolescence, both the timebase generator and the comparators that trigger the analyzers are housed on submodules that plug into the PC Bus-mounted logic analysis boards. If your system includes multiple analyzer boards, a private trigger bus that runs across the tops of the boards synchronizes their operation. The inability to synchronize such multiple-board configurations was a shortcoming of some earlier PC-based logic analyzers.

You can operate these logic analyzers as state analyzers synchronously with a SUT (system under test) clock running at 25 MHz max, clocking from the logical combination of three external rising edges and two falling edges. You can also operate the logic analyzers asynchronously as timing analyzers; when the analyzer is running in the asynchronous mode, you can set its internal clock to run at 133 rates from 125 Hz to 25 MHz. Channel multiplexing enables the analyzers to operate to 125 MHz but reduces the number of channels to ⅕ that

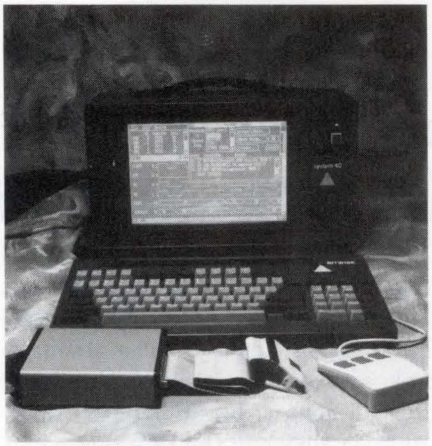



***The block diagram of this logic-analyzer*** *family reveals the private trigger bus that synchronizes multiple boards and the plug-in submodularity of the time-base generator and comparator.*

available at 25 MHz. However, multiplexing increases by 5× the amount of samples the logic analyzer's memory can store: for example, a system with 64k words of memory can store 320k samples at 125 MHz.

Instead of using single-word comparators, the logic analyzers base their triggering on truth tables stored in RAM. You can set them to trigger on the logical AND of five 8-bit comparison bytes. Thus, triggering can occur on individual addresses, rather than on an entire address range, which may contain addresses of no interest.

A 16-level trigger sequencer uses eight qualifier inputs from the pod. You can use the sequencer to trigger any logic-analyzer module in the system or to trigger an external instrument, such as a digital storage oscilloscope. The analysis systems also permit triggering to occur as late as the Nth ($N \leq 256$) occurrence of an event. When not using qualifiers, you can employ the trigger delay in regard to 64k states.



***A small portable case** houses everything but the pod in systems that have 160 or fewer channels. An equivalent-time-sampling pod acquires data on repetitive patterns at 1 GHz.*

A Multi-Trace feature lets you track down intermittent faults without running the risk of missing the problem you are trying to isolate. You can partition the memory to collect as many as 256 sets of data in a single trace, which permits you to collect different data without having to stop and then restart tracing.

You can substitute an internally generated time stamp for either eight or 16 channels of data. To track down multilevel trigger sequences, you can insert the trigger level into the time-stamp data stream. You can also measure frequencies and time events with reloadable 8-bit counters (there is one counter for each trigger level) and link counters to create delays as long as $2^{40}$ events.

System with 80 channels and 64k-word memory, \$15,000. 1-GHz, equivalent-time sampling pod for 40 channels, \$1800. ***—Dan Strassberg***

*BitWise Designs Inc, 297 River St, Suite 501, Troy, NY 12180. Phone (800) 367-5906; in NY, (518) 274-0755. TWX 710-110-1708.*

**Circle No 699**



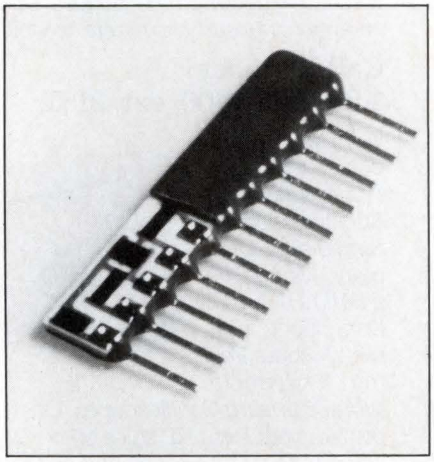
  

# PC-based resistor-network CAD handles a variety of package types

The Resicalc CAD program for the IBM PC and compatible computers not only allows you to design semicustom resistor networks, it provides guide-price information and dial-up access to quotations, delivery information, and order-placement facilities. Because the program incorporates the company's resistor-network design rules, it can immediately apprise you as to whether or not your design is manufacturable. If your initial design violates these design rules, you can conduct "what-if" experiments to decide on a suitable design compromise.

The program allows you to design single-in-line-packaged networks or design networks packaged in surface-mounting leadless carriers with leadouts suitable for either through-hole or surface mounting. You specify the number of pins (4 to 13), the lead pitch (0.05 or 0.1 in.), the maximum height of the network, and the number of resistors that the network must contain; the program then calculates the network's length for you. You can also specify an unpassivated network, a network passivated with an epoxy or plastic coating, and whether the networks should be delivered on tape, in sticks, or packaged in boxes.

To specify the electrical parameters of the resistor network, you enter each resistor's absolute value, absolute tolerance, tolerance relative to another specified resistor, absolute temperature coefficient, temperature coefficient relative to another specified resistor, and maximum power dissipation. The absolute resistor tolerance can be as good as 0.5%, the relative tolerance as good as 0.1%, the absolute temperature coefficient as low as 50 ppm/°C, and the relative temperature coefficient as low as 20 ppm/°C. The ability to specify relative tolerances and relative temperature coefficients makes the CAD package suitable for the design of temperature-tracking resistive dividers. Its help windows permit you to obtain the range of possible values for each parameter.



***The Resicalc CAD package lets you design*** *through-hole, surface-mount, or leadless-carrier resistor networks on an IBM PC or compatible, and allows you to access the vendor's mainframe to place an order or to obtain price and delivery information.*

The specification of the resistor network's internal interconnect pattern constitutes the final stage of the design process. After you've specified an input and output leadout for each resistor, the CAD package draws a schematic diagram of the network on the PC's monitor. It then proceeds to check your design parameters against the company's design rules to determine if the design is manufacturable. Your design will fail this test if, for example, it requires more substrate area than is available in the package you've specified. If your initial design proves unmanufacturable, you can iterate the design until it complies both with your requirements and the company's resistor-network design rules. (The design editor in the Resicalc version evaluated for this article could have been more sophisticated, but was nonetheless useable.)

After you've designed your resistor network, Resicalc can provide you with a guide price; if your PC is equipped with a modem, Resicalc lets you obtain actual price and delivery information by using a toll-free number to phone the company's computer. You can also use this phone link with the company's computer to place an order for prototype or production quantities of the resistor network. Alternatively, Resicalc can print out a completed order form for you, or can transfer your order and design file to a floppy disk for mailing to the company.

The company supplies the Resicalc CAD package free-of-charge on an IBM PC-compatible floppy disk. ***—Peter Harold***

*Ericsson, Business Area Components, Box 98, 56300 Granna, Sweden. Phone 46-39011020.*

**Circle No 701**

*Ericsson Components, 3255 Scott Blvd, Suite 4D, Santa Clara, CA 95054. Phone (408) 988-3603.*

**Circle No 702**

# Modular logic analyzer offers expansion and ease of use

The Model 1230 modular logic analyzer consists of a basic unit to which you add plug-in boards to provide extra channels and other features as needed.

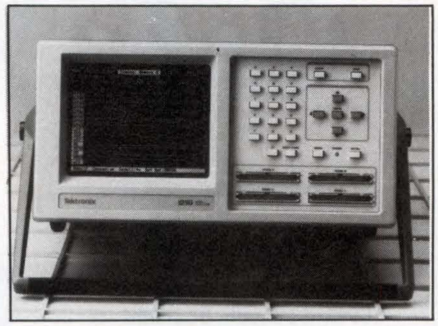
Using all 16 of the basic unit's data-acquisition channels and an internal or external clock, you can perform data capture at 25 MHz max. Using the internal clock and eight or four channels, you can capture data at a maximum of 50 or 100 MHz, respectively. Glitch capture is available on eight of the channels.

You can increase the analyzer's capacity to 64 channels by adding three expansion boards, each of which duplicates the basic unit's data-capturing capability and features its own timebase.

The analyzer stores data in any of four nonvolatile, 2047-bit/channel-deep memories. You can compare memories for display and view highlighted differences, or you can use memory comparison in trigger conditions. The system visually presents the data in memory as a timing diagram, a state display, or, if an optional probe is employed, as a disassembly of μP code.

The basic unit, as well as each expansion board, comes with a programmable threshold probe. This probe allows you to select from preset threshold values for TTL, ECL, and CMOS, or to program a threshold in 100-mV increments from −9 to +9V. Among the options you can obtain for the unit are TTL-only probes and disassembly probes for various 8- and 16-bit μPs.

The unit offers 14 levels of triggering, with three IF-THEN-ELSE conditions available on each level. You can assign names to as many as 24 data values, then use these names as data in the triggering setup, making it easy to read and understand. Nonvolatile memory provides a place to store as many as eight setup conditions.



***This analyzer's basic unit features 16 channels that provide sampling rates to 100 MHz,** but expansion boards permit the addition of as many as 64 channels with four timebases.*

The unit is easy to use. Each menu screen presents prompts, reminding you which buttons to employ in making selections. Pressing the Notes key elicits a detailed explanation of the current menu selection. If you obtain the international-notes option, the unit will present these explanations in French, German, Spanish, or Dutch.

The basic unit comes with an RS-170 video output of the display screen. You can add a parallel printer port to produce hard copies of the display or to list the contents of the memory on a graphics printer.

You can also add an RS-232 or GPIB interface, permitting a host controller to block transfer data and setups and to emulate keystrokes for remote control of the unit.

Basic unit, $2795; each channel-expansion board, $1200; other options, from $200; μP probes, from $600. Delivery, for some options, 8 to 10 weeks ARO.

**—Richard A Quinnell**

*Tektronix, Box 12132, Portland, OR 97212. Phone (800) 245-2036; in OR, (503) 627-7111. TLX 151754.*

**Circle No 698**

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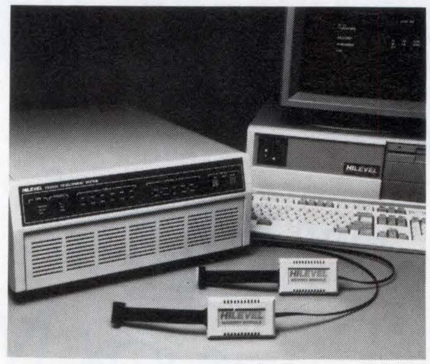
# Microcode system puts control store in pod

The DS5000 microcode development system has its control-store ROM-emulation RAM (writable control store) in its target-system interface pods. The emulation memory of earlier microcode development systems resides in the chassis of these development systems. The longer connecting cables needed for the earlier architecture cause a significant propagation delay. The DS5000 exhibits 15- to 150-nsec access times, depending on the memory pod selected, for the system under development.

The DS5000's chassis has 16 card slots that will accept either memory-pod interface cards or logic-analysis cards. Thus, the system can either emulate a 512-bit-wide control-store ROM or perform 256-channel logic analysis—or provide some intermediate mix of the two functions. Each memory-pod interface card and logic-analysis card has its own independent clock.

The system's memory depth ranges from 1k- to 64k-words, depending on the configuration. Its 8- to 512-bit microcode word is addressable in 8-bit increments. It emulates ROMs, PROMs, and static RAMs—both registered and non-registered. Each emulated memory device can have as many as three chip-select inputs. The system is therefore more suitable for microprogrammed μPs and ASICs that use conventional, byte-wide ROMs than for bit-slice μPs, which need more flexible control stores.

Each logic-analyzer card features 16-level state-machine triggering with four word-recognizers per level. The cards can operate independently to monitor multiple asynchronous processes while one card —typically the one monitoring the fastest process—serves as a synchronizing time stamp for the rest. The logic-analyzer cards perform software-performance analysis as well as state and timing analysis. The maximum timing resolution is 15 nsec. The memory pods provide only a TTL-level interface, but the logic-analysis cards handle ECL levels as well as TTL levels.



***The DS5000 microcode development system*** *has its ROM-emulation writeable control store in its target-system interface pods, thus minimizing propagation delays caused by interconnecting cables.*

The unit requires a computer for control. Software is available for the IBM PC/AT and DEC VAX, Sun, or Apollo workstations. The cost of typical systems ranges from $10,000 to $20,000, depending on the configuration. You can expect delivery six weeks ARO.—***Charles H Small***

*HiLevel Technology Inc, 31 Technology Dr, Irvine, CA 92718. Phone (800) 445-3835; in CA, (714) 727-2100. TLX 655316.*

**Circle No 697**

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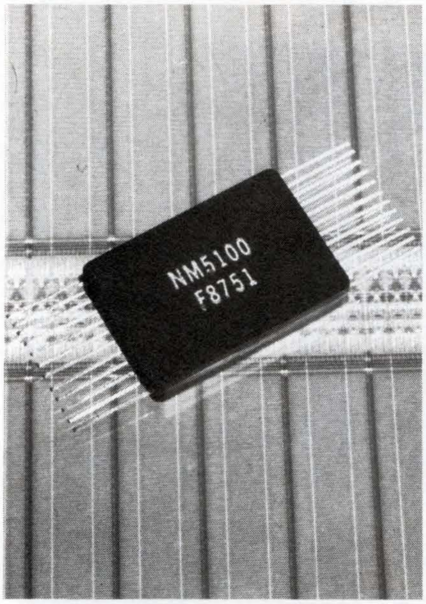
CIRCLE NO 138

# BiCMOS chips expand memory applications of static RAMs

By combining the speed of ECL and the circuit density of CMOS, BiCMOS static RAMs have surpassed the performance of many bipolar and CMOS equivalents. As a result, BiCMOS chips with ECL I/O promise to supplant a growing number of existing memory devices in cache- and main-memory applications. (Three such BiCMOS devices were presented at the International Solid-State Circuits Conference in February.)




***Targeting workstation and large-computer** applications, the model NM5100 BiCMOS, 256k-bit static RAM achieves access times as low as 15 nsec.*

National Semiconductor's model NM5100 will be offered with access times of 15 and 18 nsec. You can buy sample quantities of the 18-nsec version now, and production quantities should be available in September; the 15-nsec version is scheduled for the first quarter of 1989. The device has 262,144-bit storage locations configured as two matrices of 16 blocks each; each block has 64 columns and 128 rows. By selecting only 64 cells at a time, the chip minimizes row-line delay and dc power consumption.

The NM5100's $-5V\pm10\%$ supply voltage allows an interface with 10K and 100K ECL. The chip draws 180 mA of quiescent current (0.9W dc power dissipation), and its input terminals meet the 2-kV ESD rating of MIL-STD-883.

The company proposes a new figure of merit for high-speed memories. By forming a product of two existing figures of merit—speed-power product and cost per bit—you obtain speed-power-cost per bit (in nanoseconds - milliwatts - cents/bit), allowing you to consider all the major tradeoffs when comparing memory ICs. This mode of comparison places the NM5100 ahead of most CMOS, bipolar, and GaAs memory devices.

The 1-μm BiCMOS III process used to fabricate the NM5100 includes systems in the manufacturing line for monitoring device reliability during production. These systems define the process margins by correlating various device and process parameters with yield and burn-in data. By combining this data with statistical process-control techniques, production engineers can detect process-parameter drifts early enough to correct and stabilize them.

The NM5100 chip measures 213×386 mils. The packages include a 24-pin, 365×535-mil ceramic flat-pack with a 30-mil lead pitch, and a 24-pin, 400-mil-wide ceramic DIP. 18-nsec version, $96; 15-nsec version, $125 (100).—***Tarlton Fleming***

*National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 749-7421. TLX 346353.*

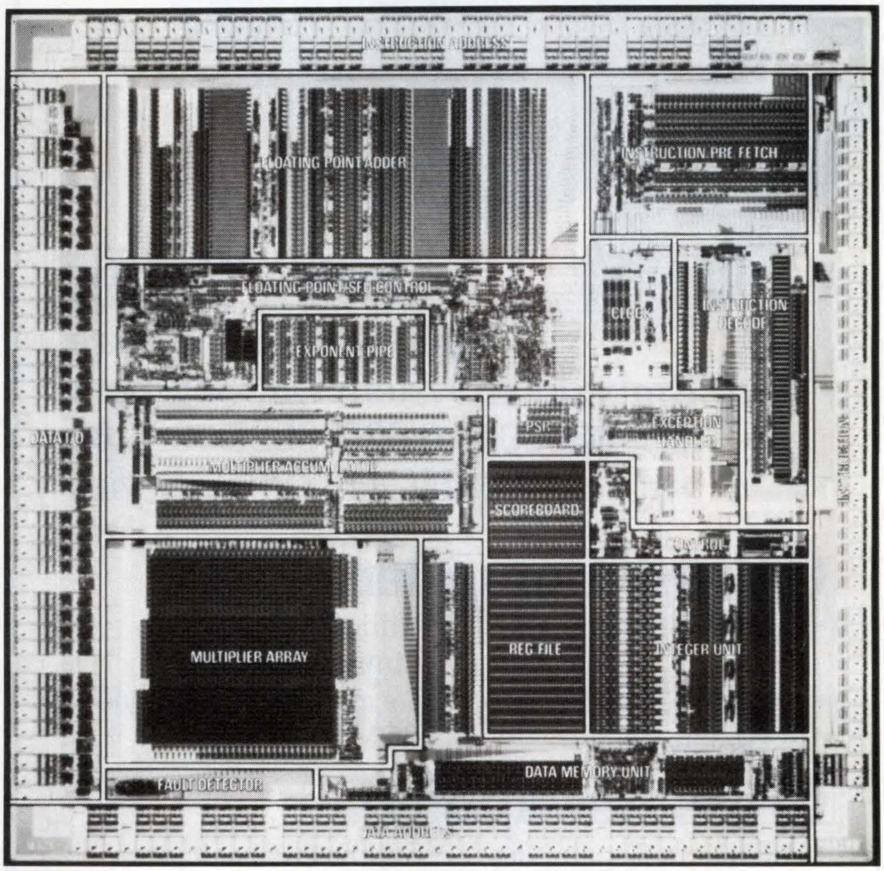
**Circle No 700**

# RISC chip set has CPU, floating-point and integer math, cache, and MMU

The Motorola 88000 chip set takes advantage of the silicon-saving RISC architecture to integrate all the major CPU-board functional blocks. The 88100 CPU includes multiple pipelined execution units, and integer and floating-point math processors. The 88200 CMMU (cache memory management unit) features an MMU (memory management unit), a cache controller, and a 16k-byte cache.

Based on a Harvard-type architecture, the 88100 implements separate instruction and data paths. The 88100's minimum configuration connects to two 88200 CMMUs, one for data and one for instructions, whereas the 88000 chip set's minimum configuration provides both 17 MIPS and 34,000 Drhystones (the MIPS spec is normalized to VAX MIPS). Using the 88000 chip set in multiprocessor designs further boosts performance specs.

These processors provide such high performance levels because the RISC architecture's characteristics require less silicon to implement than do the CISC architecture's. Therefore, designers can add to chips such features as pipelining, multiple execution units, and combined MMU and cache controllers. This integration eliminates chip-to-chip delays and lets operations occur concurrently, resulting in a faster CPU.




***Multiple execution units and register scoreboarding*** *allow the RISC-based 88100 CPU to launch an instruction every clock cycle.*

Consider, for example, the 88200 CMMU chip, which includes both an MMU and a cache. The IC concurrently performs the MMU address-translation task and effects the access to on-chip cache memory. This concurrency results in zero-wait-state access on cache hits, despite the fact that the cache is physically mapped to ensure cache coherency. Designs employing a separate, physically mapped cache and an MMU usually have to implement virtual caches to achieve zero-wait-state operation.

The 88200 includes a 16k-byte, 4-way-set-associative cache; increasing the number of associative sets in a cache improves the hit rate more than does merely increasing the cache's size. The cache controller employs a "least recently used" algorithm to replace cached data. You can connect as many as four 88200s to the 88100's instruction pipeline, and four more 88200s to the data pipeline. The controller also monitors all memory-bus operations to automatically maintain cache coherency when multiple CMMUs are used.

The 88100 CPU includes separate pipelines for instructions and data. The chip includes 32 general-purpose registers and uses register "scoreboarding" techniques to accommodate the concurrent execution and manipulation of multiple instructions. All the integer, logical, bit-field, and branch operations execute in one clock cycle. The concurrency achieved by the pipelines and register scoreboard allows the chip to launch an instruction every cycle.

The initial version of the chip features a 20-MHz clock. Motorola plans to speed up the chip and may build the device with ECL technology in the future. At the 20-MHz processor clock speed, the buses between the CPU and CMMU chips operate at 160M bytes/sec, and the cache to main memory bus operates at 64M bytes/sec.

The 88000 chip set is suitable for use in tightly coupled multiprocessor systems. You can interface as many as four 88000 chip sets to one block of main memory and have the four processors execute a single copy of the operating system. The 88200 CMMU units include hardware to maintain cache coherency in such multiprocessing environments.

Motorola's Microprocessor Products Group plans to make the chips available in PGA (pin grid array) packages in the third quarter at a cost of $375 for the 88100 and $480 for the 88200 (100). In addition, Motorola's Microcomputer Div plans to offer the chips on an 8.5×3.4-in. hybrid module that will accommodate as many as four 81000 and eight 82000 chips in a multiprocessor configuration. A single-processor module, the HM88K-1P32, with one CMMU for instructions and one CMMU for data, will be offered at a cost of $1400 (100) in the third quarter.

For development support, the company currently offers in limited quantity a system with an 88100 chip but a discrete MMU/cache. In the third quarter, it will offer a system that includes the full chip set. Both systems incorporate the AT&T Unix 5.3 operating system and assembler; a linker; and C and Fortran software packages. For software development, you can also purchase prerelease versions of an assembler, linker, and simulator that execute on 68000-based systems. —***Maury Wright***

*Motorola Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 440-2839.*

**Circle No 695**

*Motorola Microcomputer Div, 2900 S Diablo Way, Tempe, AZ 85282. Phone (602) 438-3500.*

**Circle No 696**

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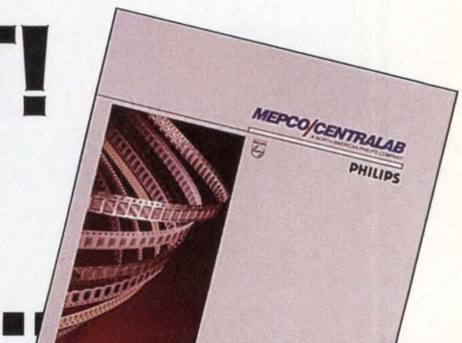


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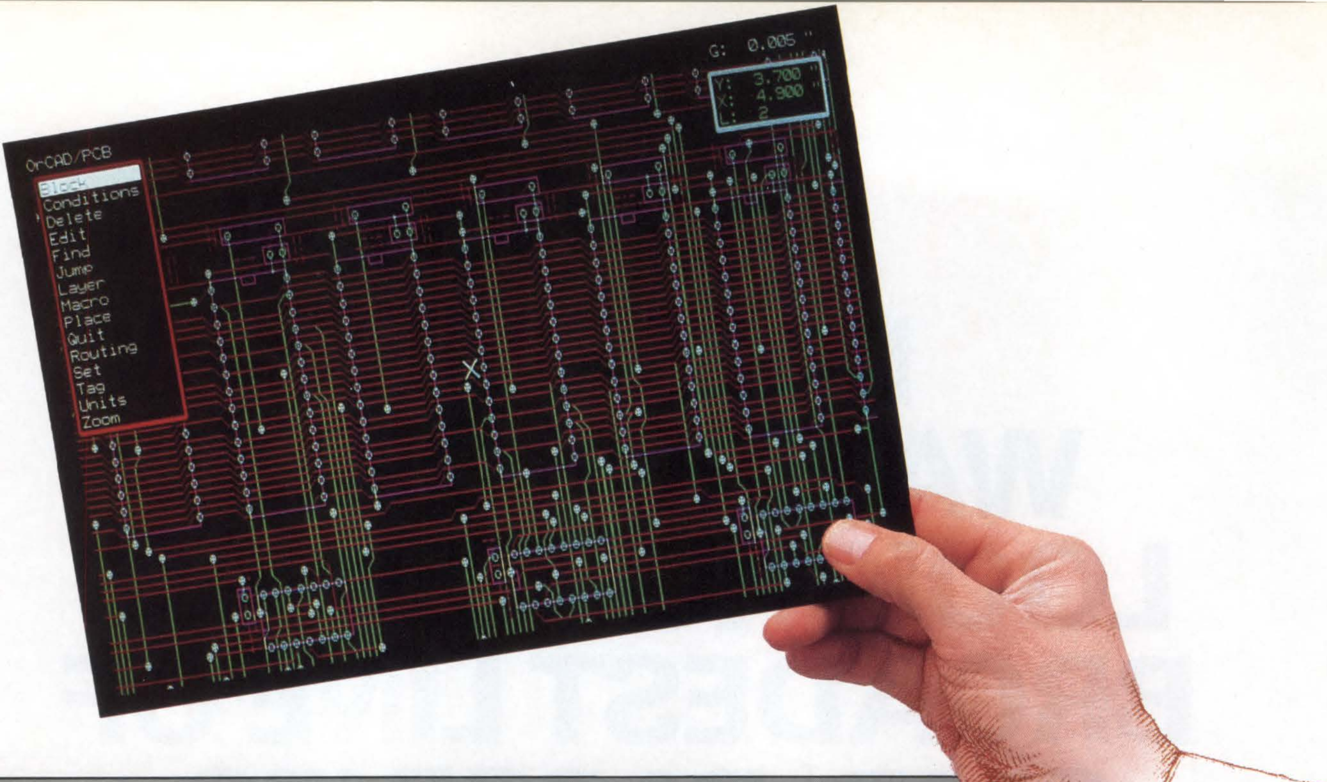


# PCB LAYOUT ON YOUR PC. FOR ONLY $1495. OrCAD PCB COMES TO LIFE.

With nearly 10,000 systems already in use, electrical engineers like the no-nonsense capability of OrCAD/SDT schematic capture. Well, now there's even more to like. Introducing OrCAD/PCB. A fast, easy-to-use PCB layout package that runs on your PC. And costs only $1,495.

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- Selectable track and via widths from 0.001″ to 0.255″.
- Square, rectangular, round, elliptical, and SMD pads.
- Grid bases of 100, 50, 25, 10 and 5 mils. Or, go off grid to 1 mil.
- Support for digital and analog components and surface-mount devices.
- Ratsnest and force vector placement.
- Definition of board edge, forbidden zones, and copper zones.

### GIVE OUR DEMO DISK A SPIN.

If you need affordable, no-nonsense PCB layout, call for a free OrCAD/PCB demo disk. Not an OrCAD user? Call for the SDT demo disk while you're at it (OrCAD/SDT costs only $495). Then, watch your PCB layouts take shape.

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# Mix-and-match logic-analyzer modules fit acquisition needs

The ML4400, a modular logic analyzer, is based on a mainframe that can take as many as four capture modules. Each capture module time-stamps the acquired data, thus allowing you to display this data from each of the modules simultaneously on a split screen. All data, both synchronous and asynchronous, is lined up on the screen in time for easy viewing. You can use cross-triggering to trigger the modules together, or you can use each module as a separate logic analyzer.

For example, a single ML4400 can be configured to analyze two 68020 μPs, 20 channels at 100 MHz, and 4 channels at 400 MHz. You can cross-trigger all of these modules, and with time-stamping, you can display data captured from any module with that from another module.

The standard capture module acquires 20 channels containing 8192 samples at 100 MHz asynchronous and 40 channels containing 4096 samples at 50 MHz synchronous. The ability to acquire data at 50 MHz synchronously should keep up with available μPs for some time. It is necessary to use synchronous acquisition when analyzing μPs in order to gather data when it is stable.

The logic pods available for the standard capture module are the standard 100-MHz pod and the 80-channel, 25-MHz expansion pod. The expansion pod multiplexes the input to allow 80-channel acquisition for the standard 100-MHz pod with a maximum rate of 25 MHz.

The μP pods interface with the standard capture module. Pods for the 8086, 68000/68010, 68020, 8085/8031/8035, 6800/6802/6808, 6809/6809E, 6502, NSC800, and Z80 are available. All of the μP pods include

***The keypad, soft keys, menus, and on-line help screens*** *make this logic analyzer easy to use. The keypad tilts up to allow easy access to the logic-pod input connectors without giving up front panel space.*

the ability to disassemble the captured data. Also, if you have pods that work with the ML4100, you can get an adapter for the ML4400.

The high-speed capture module acquires 4 channels at 400 MHz with a sample depth of 32k samples. It can also be used to capture 8 channels with 16k samples at 200 MHz or 16 channels with 8k samples at 100 MHz. The high-speed capture module can also support transitional timing.

Two logic pods are available for the high-speed module—the 400- and the 200-MHz pods. The 400-MHz pod has 16 channels so you need only one of these pods for as many as four high-speed capture modules. You can use the 200-MHz pod for more than one application—for example, using 8 channels at 200 MHz, the 200-MHz pod provides glitch-capture circuitry, or it can acquire 16 channels at 100 MHz synchronous.

You control the ML4400 from a front panel keypad and soft keys under the 7-in. display or with a standard IBM PC-style keyboard. The system is set up via menus and has on-line help screens. When the logic analyzer is turned on, it de-faults to a mode that allows simple types of acquisition for inexperienced users.

The pods connect to the front of the ML4400 where you can access the connectors by lifting the tilt-up front panel. This arrangement provides easy access to the cables on the front of the instrument and avoids wasting front-panel space.

The mainframe comes standard with serial and parallel printer interfaces, trigger outputs, a color-video interface for the IBM EGA, CGA, and compatibles, an IBM PC-style keyboard interface, eight nonvolatile setups, and a ROM emulator interface without the probe. An optional 3½-in. floppy-disk drive is available for data storage.

A starter system is available that includes the mainframe, a standard capture module, and a 40-channel logic pod for $4995. The mainframe costs $2895, the standard capture module is $1795, the high-speed capture module is $1995, the 200- or the 400-MHz pod costs $1995, and the µP pods range from $500 to $1690. You can expect delivery in four to six weeks ARO.—***David Shear***

*Arium Corp, 1931 Wright Circle, Anaheim, CA 92806. Phone (800) 862-7486; in CA, (714) 978-9531.*

**Circle No 694**

LOOK WHAT ELEVEN YEARS, 2 MILLION CPUs, AND 16 THOUSAND BOARD AND SYSTEM BUILDERS ARE DOING TO THE WORLD'S FIRST OPEN STANDARD BUS...

# ...THEY'RE MAKING IT STRONGER, POWERFUL, AND MORE POPULAR

## MULTIBUS I: TODAY'S MOST POPULAR, BEST SUPPORTED AND EASIEST TO IMPLEMENT OEM BUS.

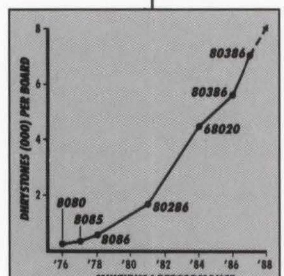
Back in 1976 when Intel introduced Multibus I, it was 8-bits wide and supported the only major microprocessor then in existence, the 8080.

The world loved the open bus concept and jumped on the Multibus bandwagon. Quickly, Multibus I gained a level of acceptance that remains unequaled today.

*1976: The debut of Multibus I. Few would have dared to predict the impact it would have on the world.*


*1986: The world's most powerful 32-bit microprocessor, the 80386, is introduced on Multibus I before any other bus.*

And, while Multibus I has remained true to its foundation as a solid, dependable standard, it has undergone a carefully controlled evolution that has produced a thoroughly modern architecture. One capable of supporting the newest 32-bit microprocessors, as well as the first Multibus board ever built, *in the same system!*

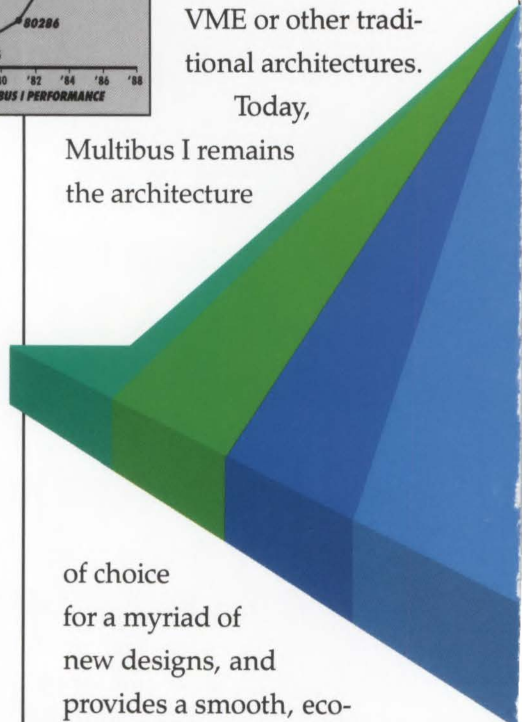



This unmatched compatibility, coupled with the ability to absorb new technology, has made Multibus I today's most popular, most versatile, best supported and easiest to implement OEM bus architecture.

## FOUNDATION OF THE MULTIBUS FAMILY.

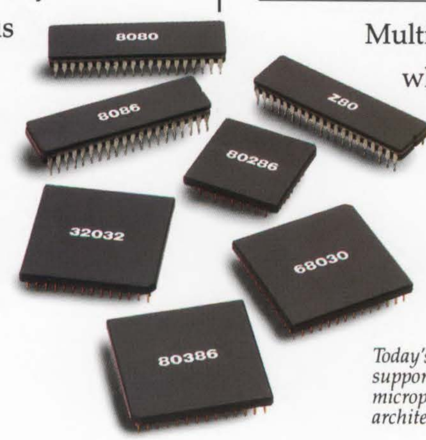
In 1982, Intel introduced Multibus II, a totally new *advanced* bus architecture designed not to replace Multibus I, but to open up entire new classes of applications impossible with Multibus I, VME or other traditional architectures.

Today, Multibus I remains the architecture of choice for a myriad of new designs, and provides a smooth, economical upgrade path for existing applications.



## KEEPING PACE WITH TECHNOLOGY, WITHOUT COMPROMISING COMPATIBILITY.

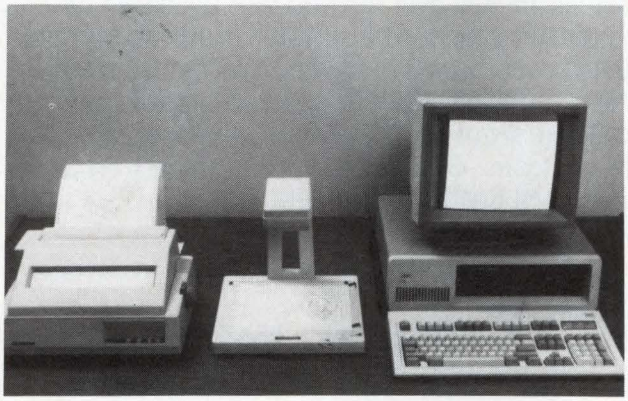
Multibus I has done what no other architecture




*Today's Multibus I supports every major microprocessor architecture.*

# READERS' CHOICE

Of all the new products covered in EDN's **March 3, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, refer to the indicated pages in our **March 3, 1988,** issue, or use EDN's Express Request service.



## ◀ IMAGE SCANNER

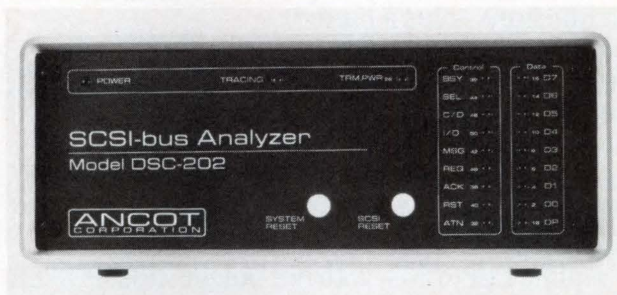
The N-205 image scanner provides user-selectable resolution to 200 dots/in. and employs an image sensor that performs overhead scanning of documents (pg 190).

**Chinon America Inc.**
**Circle No 604**

## PC AUTOROUTER

PADS-SuperRouter is a 3-stage pc-board routing package that runs on 80286- or 80386-based computers (pg 208).

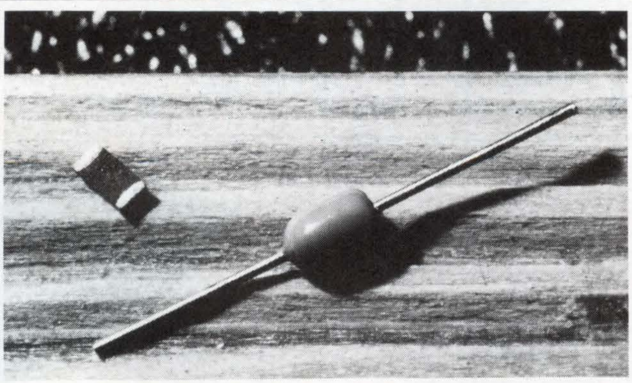
**CAD Software Inc.**
**Circle No 606**




## ▲ SCSI-BUS TESTER

The DSC-202 SCSI-bus analyzer/emulator can trace activity on the SCSI bus without affecting bus operation; it can record 32,000 56-bit-wide events and display them in several formats (pg 201).

**Ancot Corp.**
**Circle No 605**



## ▲ MULTILAYER VARISTORS

The MLV multilayer varistors can protect sensitive I/O signal lines from voltage spikes caused by ESD, lightning, nuclear-electromagnetic pulse, or other transient phenomena (pg 95).

**AVX Corp.**
**Circle No 601**

## AUDIO AMP

The TDA7350 audio power amplifier can operate as a 12W/12W stereo amplifier or as a 24W bridge amplifier (pg 182).

**SGS-Thomson Microelectronics (Italy).**
**Circle No 602**
**SGS-Thomson Microelectronics (USA).**
**Circle No 603**

# Launch your design with an 8K × 8 SRAM that uses ZEROPOWER.™

Launch your design with ZEROPOWER—the static RAMs that keep data afloat in any non-volatile memory application.

SGS-THOMSON Microelectronics backs you with a whole ZEROPOWER UL recognized family, and each member has a built-in lithium battery that maintains complete data retention, even in the event of system power loss.

All ZEROPOWER RAMs use full CMOS process technology to ensure low current drain. Plus, each device combines analog power fail detect and switching circuitry.

The big news is SGS-THOMSON's MK48Z08. The MK48Z08 has an 8K × 8 architecture—plus a battery cell life of over 11 years at 70°C. Four configurations are offered for maximum design flexibility. Each conforms to JEDEC 28-pin DIP packaging to allow direct replacement of conventional 8K × 8 SRAMs, 2764 EPROMs or 8K × 8 EEPROMs.

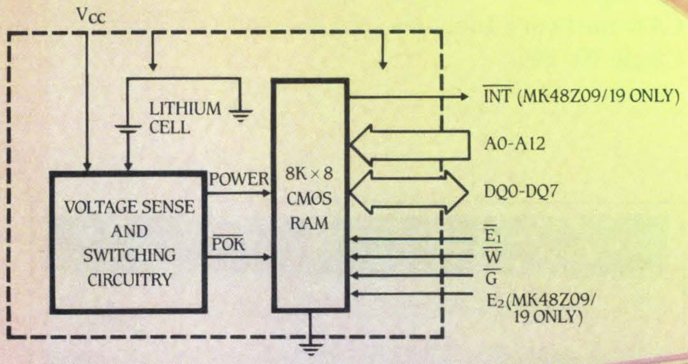
Unlike EEPROMs, with our unique ZEROPOWER memories, there's no limit to the number of write cycles you can perform. Plus, the combination of fast read and write cycles and no additional circuitry requirements makes the chip a breeze to interface with your microprocessor.

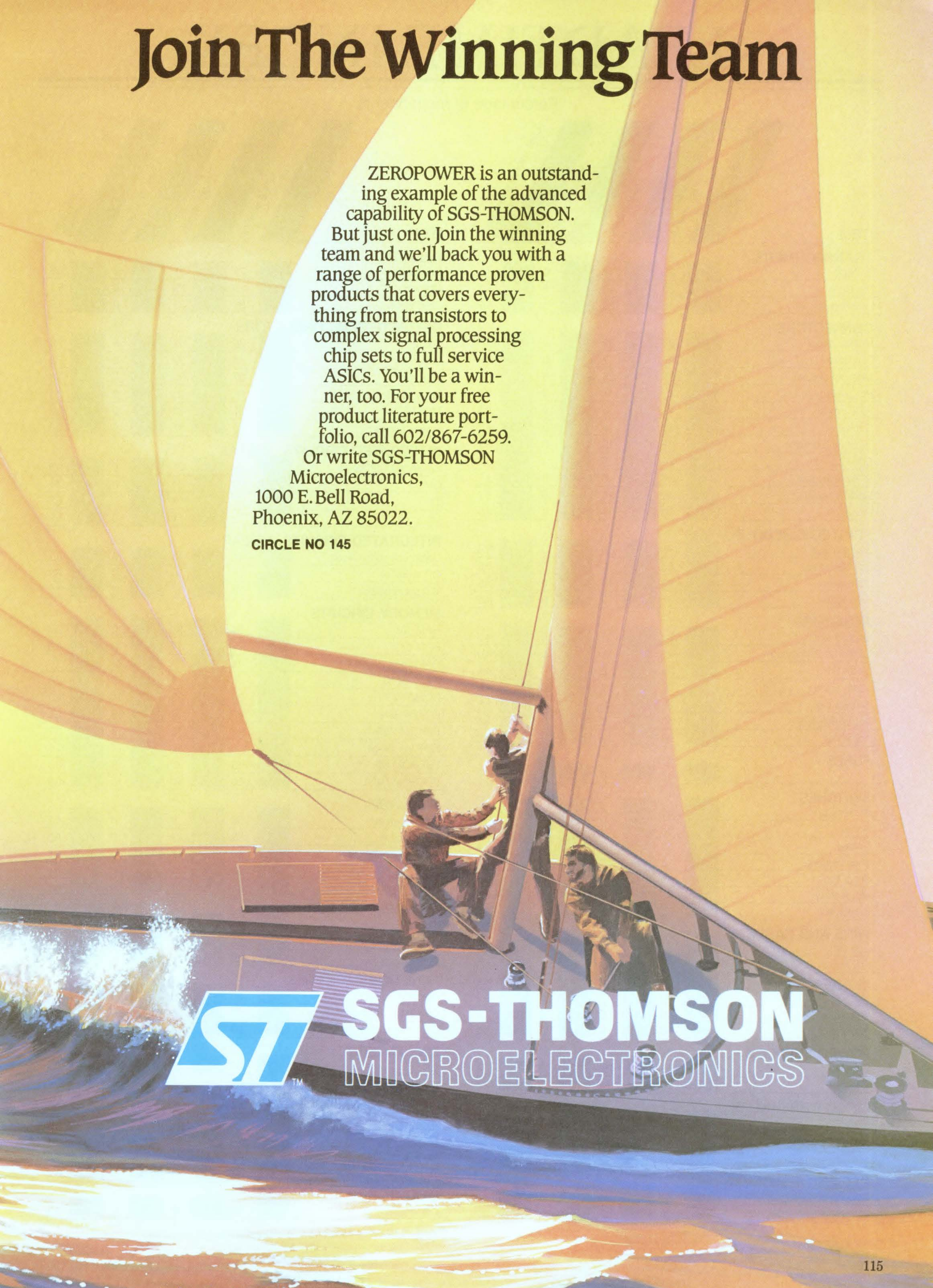
Don't worry about reliability, either. Our 16K and 64K ZEROPOWER devices (even higher densities are just over the horizon) are based on the industry's most sophisticated assembly technology and over 5 years of proven battery experience.

For convincing reliability documentation and a complete set of application notes, contact the winning team—SGS-THOMSON Microelectronics, 1000 E. Bell Road, Phoenix, AZ 85022. 602/867-6259.

| DEVICE | TEMP RANGE | WRITE PROTECT VOLT. | BATTERY LIFE OVER TEMP | U.L. RECOG | SPEED | KEY FEATURES |
|---|---|---|---|---|---|---|
| MK48Z02 | 0-70 C | 4.75V | 11 yrs. | Yes | 120-250ns | 2K × 8 SRAM unltd. write cycles |
| MK48Z12 | 0-70 C | 4.5V | 11 yrs. | Yes | 120-250ns | 2K × 8 SRAM unltd. write cycles |
| MKI48Z02 | -40-85 C | 4.75V | 6 yrs. | Yes | 120-250ns | 2K × 8 SRAM indust. temp. range |
| MK148Z12 | -40-85 C | 4.5V | 6 yrs. | Yes | 120-250ns | 2K × 8 SRAM indust. temp. range |
| MK48T02 | 0-70 C | 4.75V | 11 yrs.* | Yes | 120-250ns | 2K × 8 SRAM w/realtime clock |
| MK48T12 | 0-70 C | 4.5V | 11 yrs.* | Yes | 120-250ns | 2K × 8 SRAM w/realtime clock |
| MK48Z08/09 | 0-70 C | 4.75V | 11 yrs. | Yes | 150-250ns | 8K × 8 SRAM w/additional CE and power fault flag (– 09) |
| MK48Z18/19 | 0-70 C | 4.5V | 11 yrs. | Yes | 150-250ns | 8K × 8 SRAM w/additional CE and power fault flag (– 19) |

*3.3 yrs. minimum clock operating in battery backed mode.

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# LEADTIME INDEX

Percentage of respondents

| ITEM | Off the shelf | 1-5 weeks | 6-10 weeks | 11-20 weeks | 21-30 weeks | Over 30 weeks | Average (weeks) | Last month's average (weeks) |
|---|---|---|---|---|---|---|---|---|
| **TRANSFORMERS** | | | | | | | | |
| Toroidal | 0 | 25 | 50 | 13 | 12 | 0 | 9.7 | 7.3 |
| Pot-Core | 0 | 20 | 40 | 40 | 0 | 0 | 10.0 | 7.8 |
| Laminate (power) | 10 | 30 | 20 | 30 | 10 | 0 | 9.6 | 8.3 |
| **CONNECTORS** | | | | | | | | |
| Military panel | 0 | 22 | 45 | 22 | 11 | 0 | 10.4 | 10.8 |
| Flat/Cable | 13 | 47 | 33 | 7 | 0 | 0 | 4.7 | 5.6 |
| Multi-pin circular | 0 | 25 | 33 | 25 | 17 | 0 | 11.6 | 9.4 |
| PC (2-piece) | 8 | 25 | 50 | 17 | 0 | 0 | 7.2 | 7.4 |
| RF/Coaxial | 13 | 47 | 27 | 13 | 0 | 0 | 5.2 | 5.3 |
| Socket | 12 | 63 | 19 | 6 | 0 | 0 | 3.7 | 4.7 |
| Terminal blocks | 19 | 31 | 37 | 13 | 0 | 0 | 5.7 | 5.4 |
| Edge card | 12 | 29 | 53 | 6 | 0 | 0 | 5.8 | 5.7 |
| D-Subminiature | 13 | 50 | 31 | 6 | 0 | 0 | 4.4 | 5.1 |
| Rack & panel | 10 | 40 | 30 | 20 | 0 | 0 | 3.2 | 6.4 |
| Power | 20 | 30 | 40 | 10 | 0 | 0 | 5.4 | 5.5 |
| **PRINTED CIRCUIT BOARDS** | | | | | | | | |
| Single-sided | 0 | 71 | 29 | 0 | 0 | 0 | 3.7 | 5.4 |
| Double-sided | 0 | 25 | 75 | 0 | 0 | 0 | 6.5 | 5.8 |
| Multi-layer | 0 | 20 | 67 | 13 | 0 | 0 | 7.8 | 7.5 |
| Prototype | 6 | 81 | 13 | 0 | 0 | 0 | 2.7 | 4.3 |
| **RESISTORS** | | | | | | | | |
| Carbon film | 47 | 32 | 16 | 5 | 0 | 0 | 2.7 | 4.2 |
| Carbon composition | 42 | 21 | 26 | 11 | 0 | 0 | 4.3 | 4.0 |
| Metal film | 30 | 25 | 45 | 0 | 0 | 0 | 4.1 | 4.4 |
| Metal oxide | 18 | 55 | 18 | 9 | 0 | 0 | 4.0 | 4.6 |
| Wirewound | 11 | 39 | 28 | 22 | 0 | 0 | 6.5 | 8.8 |
| Potentiometers | 5 | 53 | 32 | 10 | 0 | 0 | 5.2 | 6.1 |
| Networks | 19 | 38 | 24 | 19 | 0 | 0 | 5.7 | 6.3 |
| **FUSES** | 39 | 33 | 28 | 0 | 0 | 0 | 2.9 | 4.4 |
| **SWITCHES** | | | | | | | | |
| Pushbutton | 10 | 50 | 35 | 5 | 0 | 0 | 4.6 | 5.8 |
| Rotary | 0 | 33 | 47 | 20 | 0 | 0 | 7.6 | 6.1 |
| Rocker | 0 | 55 | 36 | 9 | 0 | 0 | 5.4 | 5.4 |
| Thumbwheel | 0 | 33 | 25 | 42 | 0 | 0 | 9.4 | 7.7 |
| Snap action | 0 | 46 | 36 | 18 | 0 | 0 | 6.7 | 6.5 |
| Momentary | 0 | 58 | 25 | 17 | 0 | 0 | 5.9 | 6.3 |
| Dual in-line | 0 | 55 | 27 | 18 | 0 | 0 | 6.1 | 6.6 |
| **WIRE AND CABLE** | | | | | | | | |
| Coaxial | 15 | 54 | 31 | 0 | 0 | 0 | 3.6 | 4.2 |
| Flat ribbon | 12 | 65 | 23 | 0 | 0 | 0 | 3.1 | 5.5 |
| Multiconductor | 13 | 47 | 40 | 0 | 0 | 0 | 4.1 | 4.6 |
| Hookup | 35 | 40 | 25 | 0 | 0 | 0 | 2.8 | 3.2 |
| Wire wrap | 31 | 46 | 23 | 0 | 0 | 0 | 2.8 | 4.2 |
| Power cords | 18 | 65 | 12 | 5 | 0 | 0 | 3.1 | 5.9 |
| **POWER SUPPLIES** | | | | | | | | |
| Switcher | 7 | 43 | 21 | 22 | 7 | 0 | 7.9 | 7.4 |
| Linear | 0 | 29 | 50 | 14 | 7 | 0 | 8.6 | 7.7 |
| **CIRCUIT BREAKERS** | 20 | 27 | 13 | 33 | 7 | 0 | 8.7 | 8.0 |
| **HEAT SINKS** | 7 | 53 | 27 | 13 | 0 | 0 | 5.3 | 5.1 |
| **RELAYS** | | | | | | | | |
| General purpose | 12 | 47 | 18 | 23 | 0 | 0 | 6.1 | 6.1 |
| PC board | 6 | 28 | 33 | 33 | 0 | 0 | 8.5 | 7.2 |

| ITEM | Off the shelf | 1-5 weeks | 6-10 weeks | 11-20 weeks | 21-30 weeks | Over 30 weeks | Average (weeks) | Last month's average (weeks) |
|---|---|---|---|---|---|---|---|---|
| **RELAYS** | | | | | | | | |
| Dry reed | 0 | 23 | 31 | 31 | 15 | 0 | 11.8 | 8.6 |
| Mercury | 0 | 25 | 38 | 25 | 12 | 0 | 10.7 | 9.1 |
| Solid state | 0 | 25 | 33 | 33 | 9 | 0 | 10.8 | 8.9 |
| **DISCRETE SEMICONDUCTORS** | | | | | | | | |
| Diode | 23 | 36 | 18 | 14 | 4 | 5 | 7.0 | 7.0 |
| Zener | 5 | 44 | 17 | 22 | 6 | 6 | 9.2 | 7.3 |
| Thyristor | 7 | 27 | 33 | 33 | 0 | 0 | 8.5 | 8.8 |
| Small signal transistor | 13 | 37 | 31 | 13 | 6 | 0 | 6.9 | 7.4 |
| MOSFET | 0 | 37 | 36 | 27 | 0 | 0 | 7.9 | 10.2 |
| Power, bipolar | 0 | 45 | 18 | 37 | 0 | 0 | 8.3 | 9.3 |
| **INTEGRATED CIRCUITS, DIGITAL** | | | | | | | | |
| Advanced CMOS | 7 | 20 | 40 | 27 | 6 | 0 | 9.5 | 9.6 |
| CMOS | 6 | 29 | 41 | 24 | 0 | 0 | 7.7 | 7.1 |
| TTL | 23 | 15 | 54 | 8 | 0 | 0 | 5.9 | 6.5 |
| LS | 21 | 22 | 43 | 14 | 0 | 0 | 6.1 | 5.9 |
| **INTEGRATED CIRCUITS, LINEAR** | | | | | | | | |
| Communication/Circuit | 10 | 40 | 40 | 10 | 0 | 0 | 5.6 | 8.7 |
| OP amplifier | 20 | 27 | 33 | 20 | 0 | 0 | 6.4 | 6.3 |
| Voltage regulator | 16 | 28 | 39 | 17 | 0 | 0 | 6.4 | 7.2 |
| **MEMORY CIRCUITS** | | | | | | | | |
| RAM 16k | 11 | 34 | 22 | 33 | 0 | 0 | 7.7 | 9.7 |
| RAM 64k | 8 | 25 | 25 | 34 | 0 | 8 | 10.4 | 8.8 |
| RAM 256k | 7 | 14 | 36 | 0 | 14 | 29 | 15.8 | 10.0 |
| RAM 1M-bit | 0 | 13 | 37 | 0 | 25 | 25 | 17.5 | 12.5 |
| ROM/PROM | 0 | 34 | 33 | 22 | 0 | 11 | 10.3 | 11.0 |
| EPROM 64k | 0 | 25 | 42 | 25 | 0 | 8 | 10.3 | 9.5 |
| EPROM 256k | 0 | 42 | 25 | 25 | 0 | 8 | 9.3 | 9.3 |
| EPROM 1M-bit | 0 | 0 | 33 | 17 | 33 | 17 | 19.4 | 11.6 |
| EEPROM 16k | 0 | 13 | 37 | 37 | 0 | 13 | 13.2 | 10.6 |
| EEPROM 64k | 0 | 20 | 40 | 30 | 0 | 10 | 11.5 | 10.9 |
| **DISPLAYS** | | | | | | | | |
| Panel meters | 9 | 36 | 46 | 9 | 0 | 0 | 5.8 | 6.7 |
| Fluorescent | 0 | 33 | 45 | 22 | 0 | 0 | 7.8 | 8.5 |
| Incandescent | 0 | 66 | 17 | 17 | 0 | 0 | 5.4 | 6.5 |
| LED | 10 | 53 | 21 | 16 | 0 | 0 | 5.3 | 8.1 |
| Liquid crystal | 15 | 15 | 39 | 31 | 0 | 0 | 8.4 | 10.5 |
| **MICROPROCESSOR ICs** | | | | | | | | |
| 8-bit | 0 | 34 | 58 | 8 | 0 | 0 | 6.6 | 7.6 |
| 16-bit | 0 | 12 | 88 | 0 | 0 | 0 | 7.3 | 9.3 |
| 32-bit | 0 | 0 | 78 | 22 | 0 | 0 | 9.8 | 7.6 |
| **FUNCTION PACKAGES** | | | | | | | | |
| Amplifier | 0 | 22 | 45 | 33 | 0 | 0 | 9.3 | 6.4 |
| Converter, analog to digital | 8 | 17 | 42 | 25 | 8 | 0 | 9.8 | 8.6 |
| Converter, digital to analog | 10 | 20 | 30 | 40 | 0 | 0 | 9.2 | 9.2 |
| **LINE FILTERS** | 17 | 33 | 33 | 17 | 0 | 0 | 6.0 | 9.4 |
| **CAPACITORS** | | | | | | | | |
| Ceramic monolithic | 6 | 55 | 33 | 6 | 0 | 0 | 4.7 | 5.8 |
| Ceramic disc | 12 | 47 | 24 | 17 | 0 | 0 | 5.8 | 5.1 |
| Film | 0 | 57 | 29 | 14 | 0 | 0 | 5.7 | 4.8 |
| Aluminum electrolytic | 5 | 47 | 27 | 21 | 0 | 0 | 6.5 | 4.8 |
| Tantalum | 0 | 47 | 29 | 24 | 0 | 0 | 7.1 | 6.2 |
| **INDUCTORS** | 0 | 42 | 42 | 16 | 0 | 0 | 6.8 | 9.3 |

Source: *Electronics Purchasing* magazine's survey of buyers

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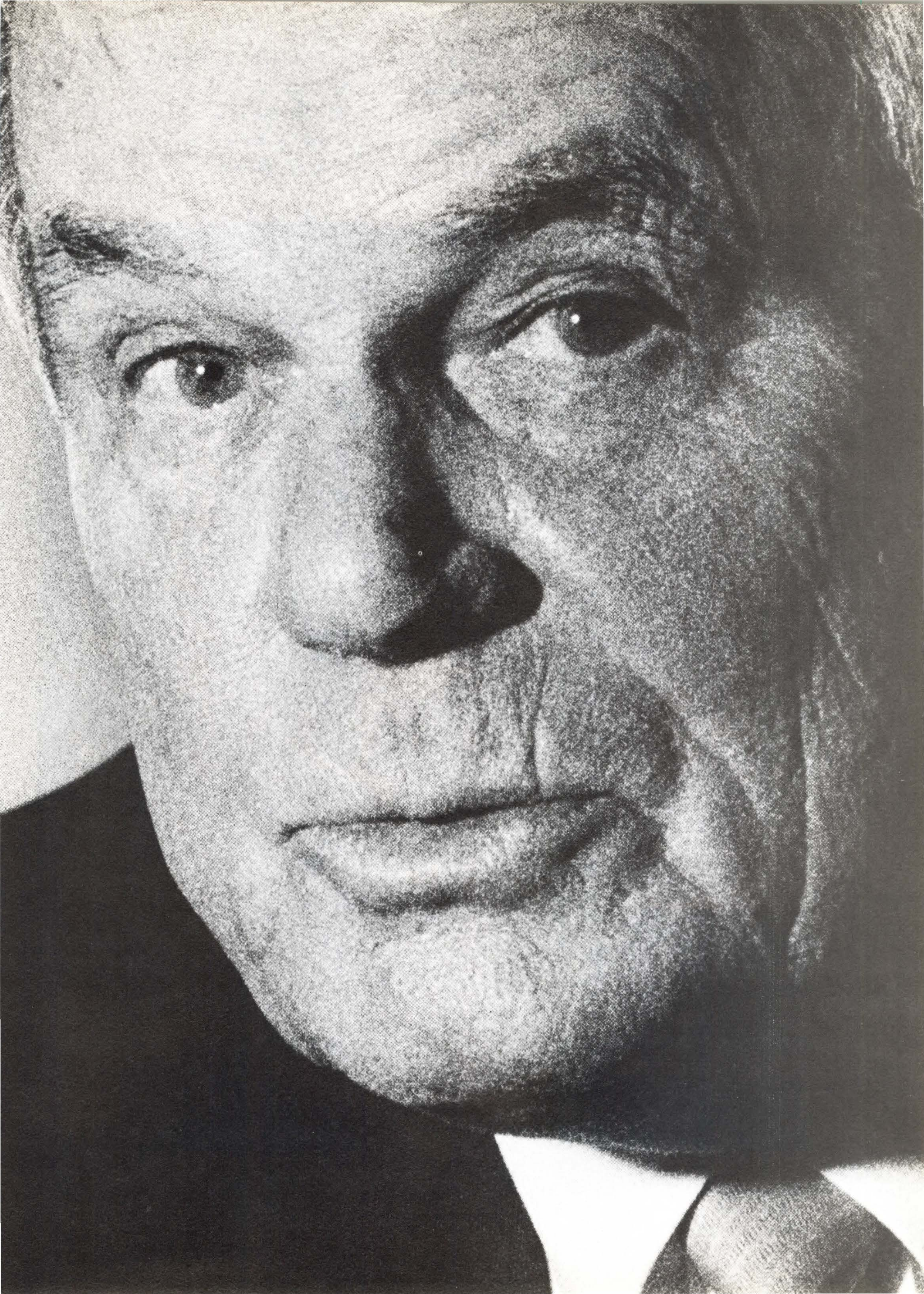
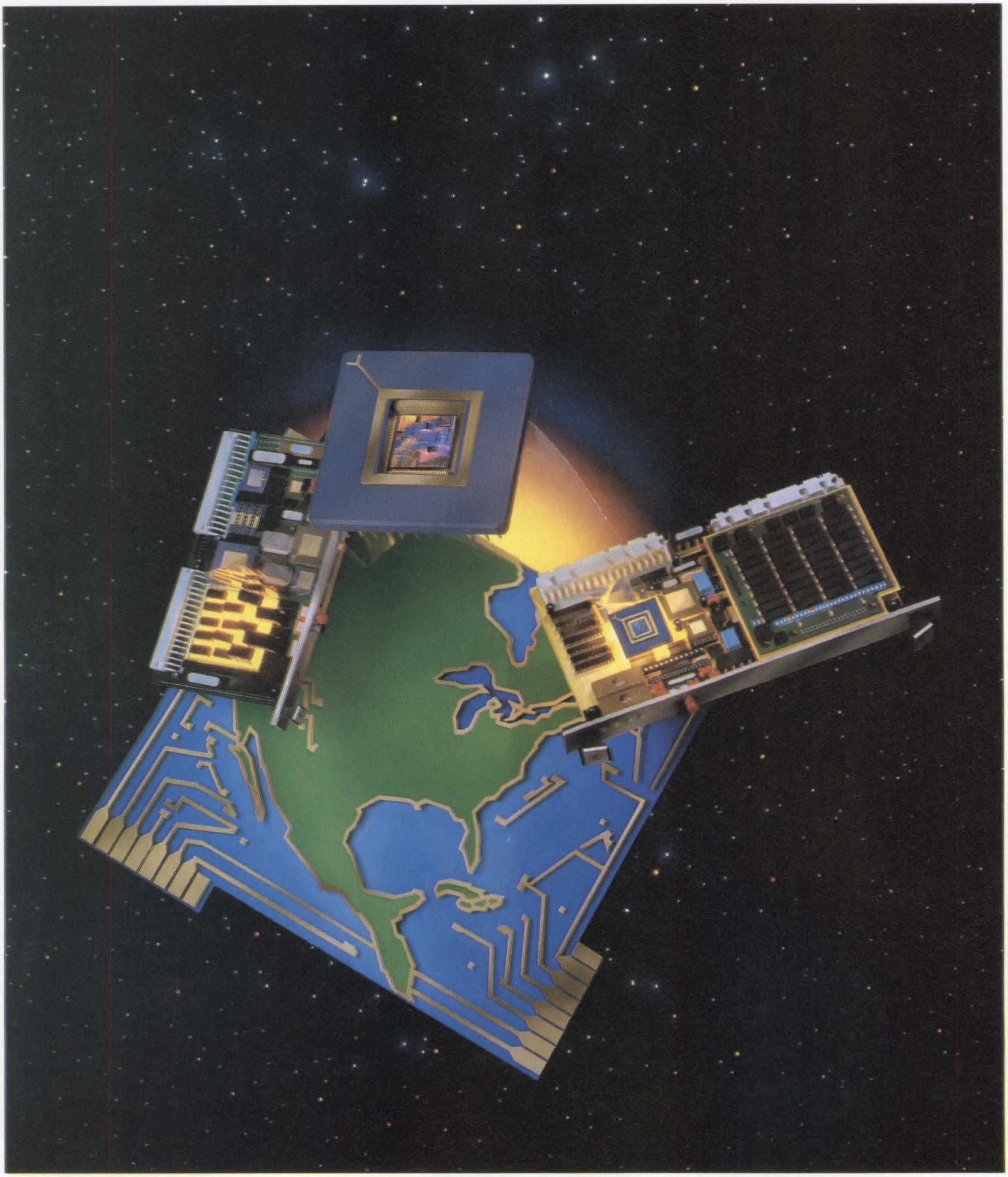


Commercially available VLSI ICs enable designers to pack more functions onto pc boards compatible with standard 32-bit multimaster buses. In Multibus II and VME Bus applications, bus-interface ICs can replace anywhere from a dozen to several dozen discrete and programmable-logic chips.



***Designers of Multibus II and VME Bus boards*** *will encounter a world of difference when they design with VLSI bus-interface ICs. (Photo courtesy Motorola Microcomputer Div)*

Special Report

# Bus-interface ICs

Maury Wright, *Regional Editor*

Now, years after the development of the bus specs themselves, VLSI chips for commercial 32-bit multimaster bus interfaces are readily available and economically feasible. Application-specific VME Bus- and Multibus II-interface ICs offer pc-board designers the same advantages as other VLSI chips: lower parts count, lower power consumption, and lower cost. Moreover, because of the extra pc-board real estate that an interface chip affords, you can add features and functions—even though the size of the board is fixed.

Without bus-interface ICs, designers of Multibus II or VME Bus boards must dedicate a substantial amount of pc-board real estate to bus-interface circuitry. Interfaces implemented with discrete ICs or PLAs can take up 20 to 30% of the real estate available. In contrast to the simple interfaces of older 8- and 16-bit buses such as the STD Bus and Multibus I, the 32-bit multimaster buses, with their interrupt-structure, arbitration-scheme, and burst-data-transfer features, result in the added interface complexity.

Thirty-two-bit multimaster buses are necessary to harness the power of 32-bit μPs, custom processors, and RISC μPs in open systems. The architecture of these high-performance systems has generated the system-on-a-board distributed-intelligence concept. Most boards of this type include a local μP and memory, and communicate with other boards by transferring commands and blocks of data across the bus.

The trend toward distributed intelligence increases the need to place more functions on a single board, and therefore bus-interface ICs will play an important role in the design of new boards. DEC, for instance, employed a custom VLSI interface chip on every board intended for its 32-bit BI bus. In fact, DEC developed and produced the chip before beginning to use the BI bus. You can also expect interface chips to be very important in designing boards compatible with IBM's Micro Channel bus. The Micro Channel bus's small board size and power limitations make VLSI interfaces mandatory for most add-in-card applications (see **box**, "ICs mate cards to Micro Channel size/power specs").

The system-on-a-board concept is useful in the creation of multiprocessor systems, but it is also commonly used to partition a typical single-CPU system into functional blocks. Disk or communication boards, for example, can function as a system just as a CPU board can. And, you can design disk and communication boards as bus masters.

Bus-interface ICs for VME Bus or Multibus II designs greatly simplify the task of designing a system on a board. And, you can use the saved real estate to add value to your product. In some cases, the different features of the chips themselves may sway you to choose a particular bus. For example, several VME Bus chips are available that implement an interface appropriate for any kind of board; although a simple A/D-converter board may not need to incorporate a system on a board, it may reside in a powerful system. Or, you may find that you want the inherent message-passing function of the Multibus II Message-Passing Coproces-

Boards designed without VLSI bus-interface chips sacrifice 20 to 30% of their available real estate to the PLAs and discrete logic implementing the interface.

sor (MPC) chip to provide a standard platform on which to build your system.

Briefly, consider the two bus architectures. The VME Bus is based on the shared-memory concept. During a bus cycle, a bus master addresses memory or I/O space on another board. To communicate, one board writes command and status information into a mailbox on another board. Boards can perform block transfers of data across the bus.

Although Multibus II can operate as a shared-memory bus, the Multibus II spec defines a message-passing scheme. The message-passing protocol provides a

## ICs mate cards to Micro Channel size/power specs

Although IBM developed the Micro Channel bus for use in its personal computers, the 32-bit multimaster bus has features comparable to the commercially available multimaster buses discussed in the accompanying article. The bus supports burst data transfers, arbitration, direct DMA operation between bus masters, and automatic system configuration. And, because of its size and power specs, you may find bus-interface ICs even more helpful in Micro Channel board design than in VME Bus and Multibus II board design.

Micro Channel-compatible cards have only about 33 in.$^2$ (3×11½ in.) of available pc-board real estate. Furthermore, each board in a Micro Channel system can only draw 1.4A. You can design full-featured cards that meet the spec, however, by employing VLSI interface ICs.

Chips and Technologies Inc offers four single-chip interfaces for Micro Channel boards—notwithstanding that the company may be better known for its personal-computer mother-board chip sets. Each of the four chips is packaged in a 68-pin PLCC, and each consumes less than 100 mA.

The 82C611 and 82C612 cost \$7.80 and \$10 (10,000), respectively, and connect directly to the Micro Channel bus. You only need external bus drivers for the data lines. The chips fit applications for general-purpose Micro Channel cards, and include the POS (programmable option select) registers for storing board-configuration information. The chips also include decoders for low-order address bits, and control circuits that can drive external circuits during Micro Channel board-identification operations. In addition, the 82C612 has circuitry that handles DMA handshake and arbitration functions.

The company's 82C574 and 82C575 single-chip interfaces target simple applications such as serial-port cards and modems and cost \$5.60 and \$6.40 (10,000), respectively. These ICs also include the POS registers. They perform I/O and address decoding and require virtually no support chips in most designs. The 82C574 includes one block of sixteen 8-bit general-purpose I/O ports, and the 82C575 includes two such blocks.

Altera Corp also offers a single-chip Micro Channel interface. The EPB2001 connects directly to the bus and only requires bus drivers for the data bus. The 84-pin IC is priced at under \$12 (10,000) and consumes less than 200 mA. Along with the interface circuitry, the IC includes a block of programmable logic and EPROM. Users can program the Micro Channel identification in the EPROM. The programmable logic allows the customization of POS-configuration and address-decoding functions.

### Two-chip set includes DMA

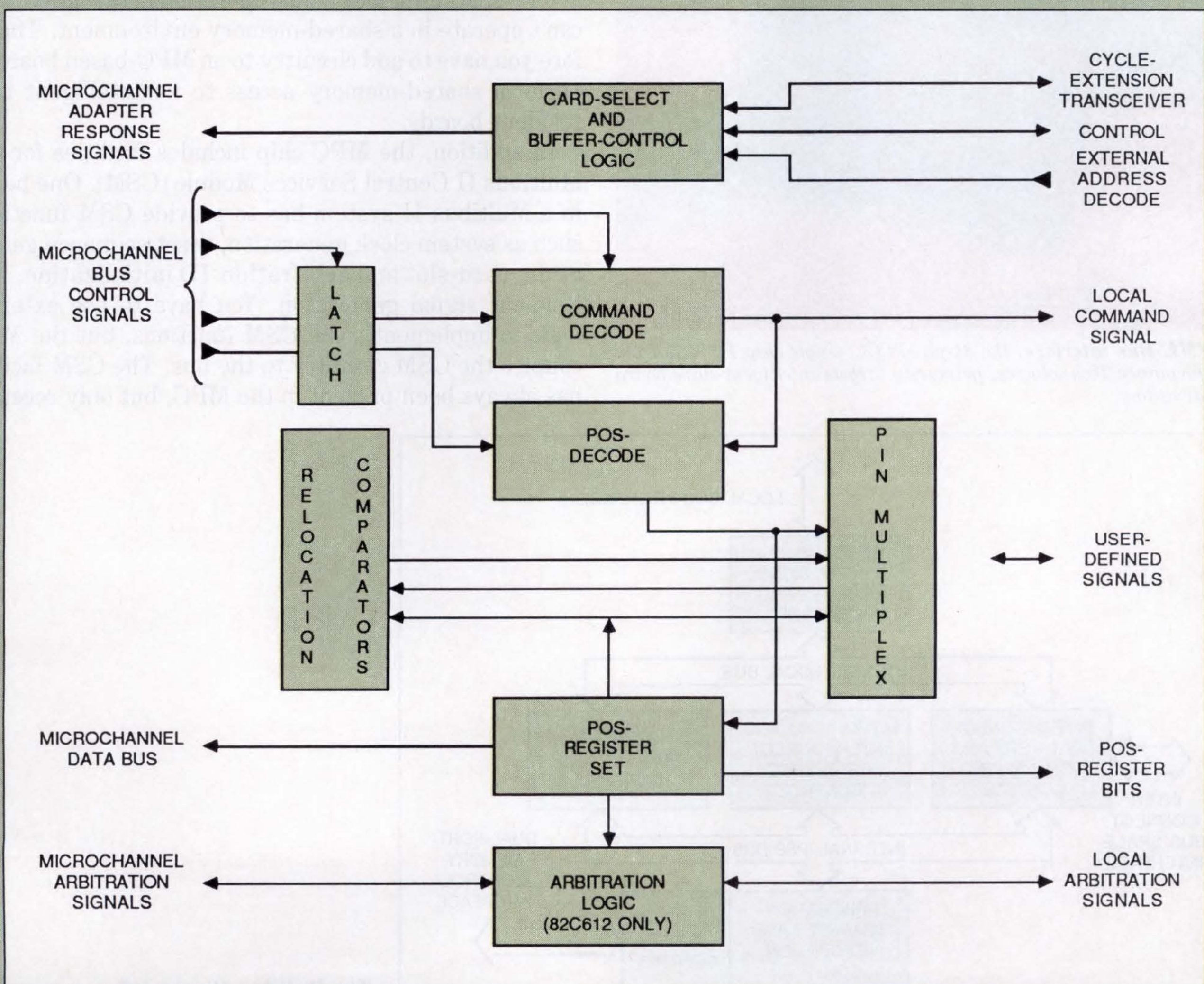
By combining the EPB2001 with the EPB2002 DMA arbitration chip, you can also use the chip in applications such as disk controllers that require DMA capabilities. The DMA chip costs less than \$5 (10,000), and the 28-pin IC draws less than 200 mA.

PLX Technology Corp has taken a different approach to bus-interface chips. The company designed a PLD equipped with high-current bus drivers, and it offers the chip programmed in a Micro Channel interface configuration. The 24-pin MCA 1200 performs bus-request and local-arbitration protocols. The \$26 chip does not include all the features of the VLSI devices discussed above, but with the PLD approach you can customize the standard configuration to fit your application.

Finally, for designers of memory boards, Edsun Laboratories Inc offers a 2-chip set for implementing 512k- to 8M-byte Micro Channel boards. The EL2010 chip set costs \$35 (1000) and includes POS registers, selectable standard way for all boards to pass commands, status information, and data. Interrupts are contained in message packets and are handled by software. In fact, Multibus II has no hardware interrupt lines. You can implement a message-passing protocol in a VME Bus system, but no specification for doing so exists.

To implement message passing for Multibus II, you must have a bus-interface IC. The lack of availability of an MPC chip has actually hampered the bus's acceptance. Intel introduced Multibus II and the concept of message passing at the same time, and the company planned the MPC chip from the onset. Most designers

identification codes, and decoding for one parallel and two serial ports. The company also offers the $2500 Designware package, which includes a sample memory board, artwork and other manufacturing information, an on-board BIOS, and EMS (enhanced memory specification) 4.0 software drivers.

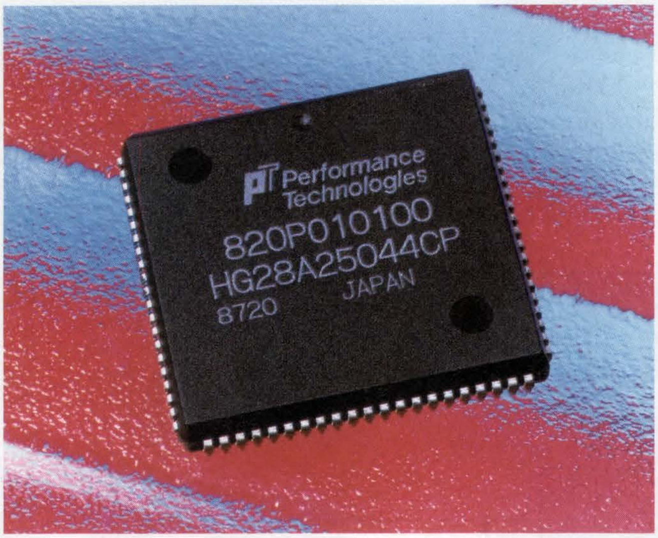



***Integrating the Micro Channel bus interface into a single chip*** *allows manufacturers to design multifunction boards within the bus's 33-in.² size and 1.4A power constraints. Chips and Technologies includes POS registers and decoders on its 82C611/612 ICs, which come in 68-pin PLCCs and draw less than 100 mA.*

## The delay in availability of the Message-Passing Coprocessor chip hurt the popularity of Multibus II.

interested in Multibus II were also attracted by the message-passing concept, but the chip has only been available during the past year. In fact, when NCR implemented Multibus II in its Tower family of computers, it had to develop a proprietary VLSI Multibus II-interface chip set. (NCR's Microelectronics Div in Colorado, CO, may someday put the 2-chip set on the market.)

You can now purchase the MPC chip from both Intel and VLSI Technology. VLSI Technology has always acted as a foundry and a source for the IC, but recently Intel has also started to produce the IC. VLSI Technology sells the part for $175 (1000), yet expects the chip to drop to the $100 range before the end of the year; Intel prices its chip at less than $100 (1000). VLSI Technology also plans to offer a version of the MPC that complies with MIL-STD-883B. The military version will be available at the end of the second quarter and initially will cost about $1000 in single quantities.

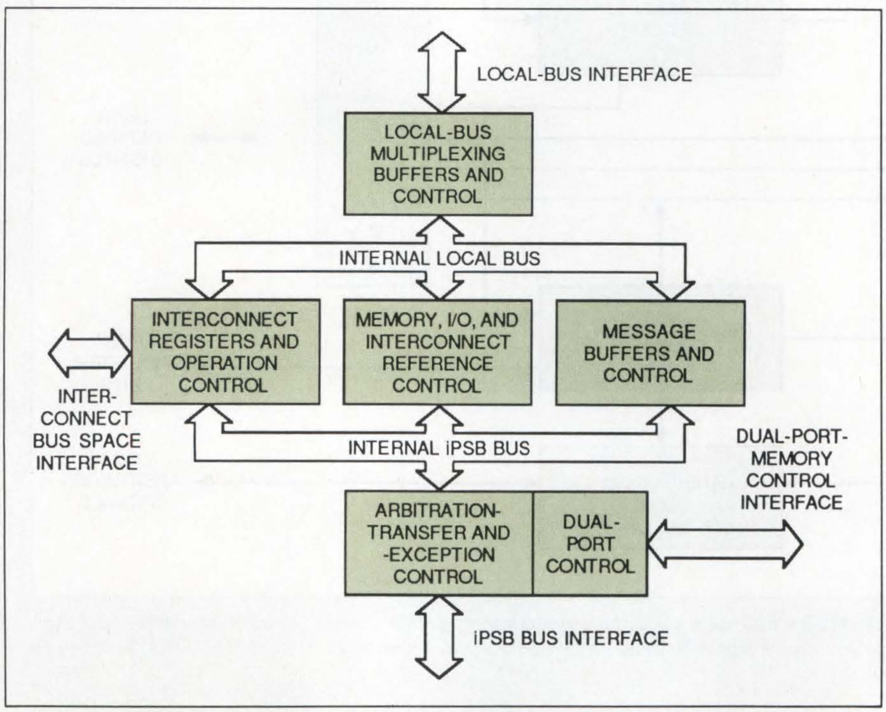



***A VME Bus interface,*** *the 84-pin PLCC single-chip PT-VSI from Performance Technologies, primarily targets intelligent-slave-board applications.*

### Interface provides μP independence

The MPC provides a processor-independent interface to Multibus II, but you must use external bus drivers to physically connect to the bus. Although Multibus II allows shared-memory bus operations, the MPC chip can't operate in a shared-memory environment. Therefore you have to add circuitry to an MPC-based board to perform shared-memory access to nonintelligent bus-resident boards.

In addition, the MPC chip includes facilities for the Multibus II Central Services Module (CSM). One board in a Multibus II system has to provide CSM functions such as system clock generation, reset-sequence generation, card-slot and arbitration-ID initialization, and time-out signal generation. You have to use external logic to implement some CSM functions, but the MPC couples the CSM circuitry to the bus. The CSM facility has always been present in the MPC, but only recently




***The Multibus II spec defines a message-passing protocol,*** *and the MPC chip, available from Intel and VLSI Technology, implements the protocol along with the bus-interface circuitry.*

## VME Bus manufacturers address compatibility issues

Recently, reports have surfaced in the trade press regarding the incompatibility of VME Bus boards from different vendors. Manufacturers of VME Bus boards claim that compatibility problems have been minor, and the worldwide volume of VME Bus board sales may belie the fact that customers have really found incompatibilities. But, with new systems operating faster, and as more board designers implement VME Bus features to reduce latencies, you should ensure that the boards you buy or design meet the VME Bus spec. Indeed, compatibility issues have spawned at least two new business ventures.

### Early designs violated spec

Most manufacturers of VME Bus boards admit that early board designs may have violated the spec. According to VME Bus specialist Shlomo Pri-Tal of Motorola, however, spec violations rarely occur now. Pri-Tal believes incompatibility primarily shows up at a logically higher design layer than the VME Bus spec defines. For example, some VME Bus boards support software message passing, though the spec does not define a message-passing protocol.

Motorola has started a software standardization effort for VME Bus systems. The company proposes standardizing the way software drivers and operating-system kernels interface to VME Bus hardware. The idea received a generally warm reception from VME Bus vendors and customers at the recent Buscon trade show in Anaheim.

Two start-up companies have involved themselves in testing the compatibility of VME Bus boards and systems. One of these, Ultraview Corp, offers the $1995 VBAT (VME Bus anomaly trigger) VME Bus board that monitors 94 VME Bus signals and detects 27 classes of timing violations. You simply install the VBAT in your system, and the board continuously monitors violations by any board in the system.

### Test for spec compliance

The board is suitable for use in either development or strictly test applications. It indicates violations via LEDs on the VME Bus front panel; to detect the source of these violations, you can use the VBAT in combination with a logic analyzer.

Joel Libove, Ultraview president, claims that the VBAT board has detected some violation in 80% of the VME Bus systems he has tested. A single board can cause a violation in a system. Libove admits that many violations often have no effect on system operation. For example, he has found many boards that don't hold data stable for the entire data strobe, and other boards that generate a glitch in the bus-busy signal.

But Libove has also found more serious violations. For example, the VME Bus spec defines an overlapped arbitration capability: A board can begin arbitration during the last phase of the previous bus cycle and therefore reduce bus latency. Most boards today don't implement overlapped arbitration, however. And Libove points out that many boards don't respond to overlapped arbitration correctly, and could cause a failure in a system with boards that do implement this feature.

VMElaboratories has experienced similar spec violations, according to VP of operations Joel Witt. Witt claims that boards often violate the VME Bus address-pipelining feature. Address pipelining allows a bus master to broadcast a new address on the bus before the previous data transfer is complete. Again, many boards don't presently implement this feature, but boards that don't handle address pipelining correctly can cause system failures. Witt points out that more and more boards will implement features that can possibly improve system performance.

### You can get a certificate

VMElaboratories is the other start-up that offers testing services to manufacturers of VME Bus boards. The company provides certification that a board meets the VME Bus spec. When the company detects violations, it gives the board manufacturer directions on revising the board to meet the spec. The certification includes examination of the board design to ensure that specs such as trace length from connector to bus driver are met, and the boards go through full functional testing. The certification process costs $3500 to $4000 for simple memory boards and can range to $7000 or more for high-end CPU boards.

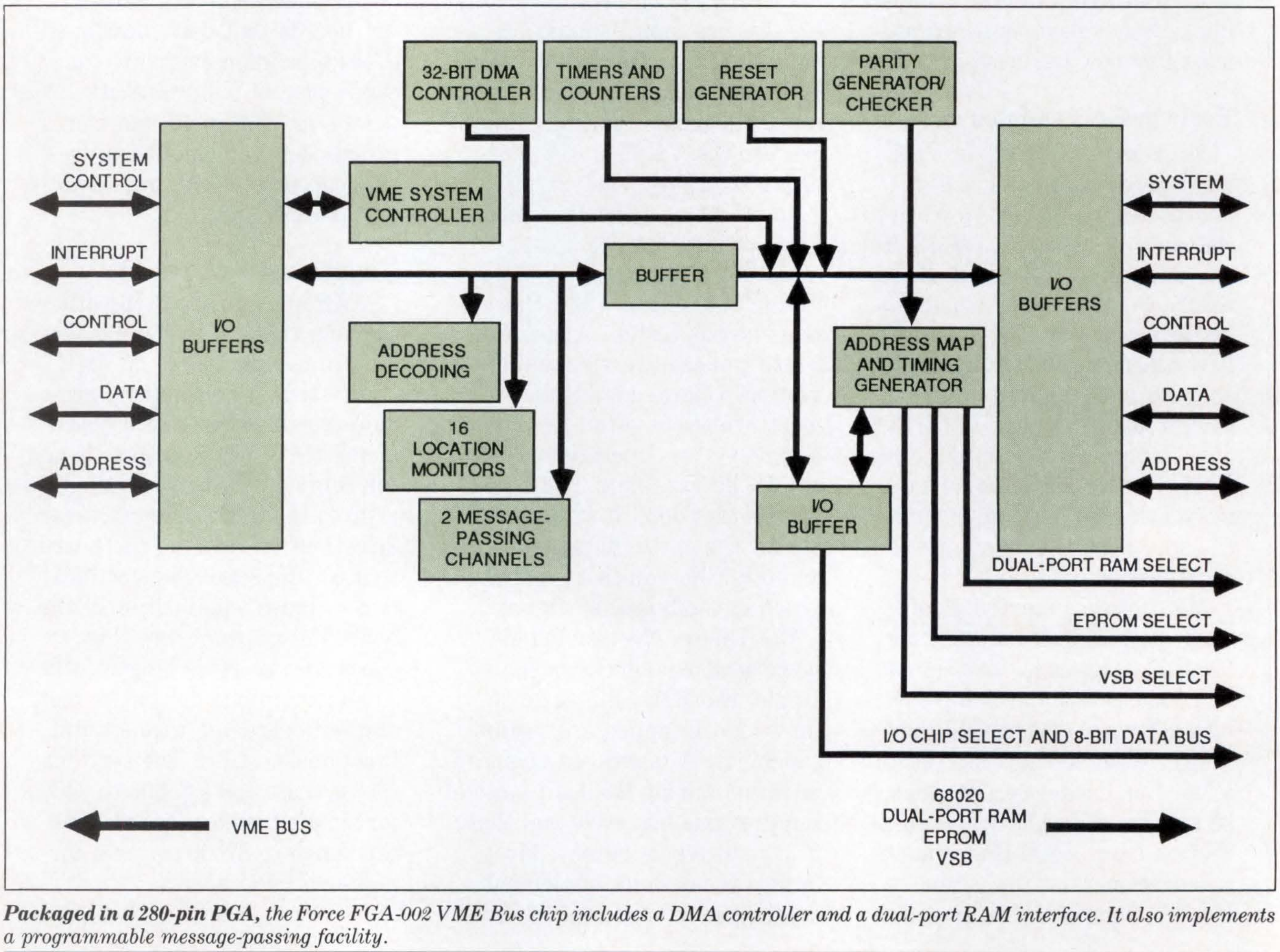
ICs that implement the VME Bus interface invariably have been designed for use with 68000 family μPs.

have Intel and VLSI Technology provided a description of its operation and certified that the CSM facility is operational.

Having but a single choice of an interface IC for Multibus II actually presents designers with some advantages. Every board vendor implements a nearly identical interface, and therefore all boards plug together and work together. The message-passing protocol is well-defined and fully operational. MPC-based boards can sustain a 32M-byte/sec data-transfer rate; Multibus II specs a maximum 40M-byte/sec rate.

When you consider VME Bus ICs, you confront the exact opposite situation. A lot of companies are involved in developing VME Bus interface chips. Although, at the time of this writing few, if any, board manufacturers have purchased VME Bus interface chips, there will be a number of chips from which to choose by the time this article is printed. Several board manufacturers have made use of bus-interface ICs developed in house, and at least five board manufacturers who have done so are now offering the ICs for sale. Several more board vendors are in the process of developing similar ICs. And the VITA (VME Bus International Trade Association) Technical Consortium —a group of VME Bus board manufacturers that funded the design of an interface chip—expects the first chips to be out by the end of the second quarter.

Most of the currently available VME Bus boards employ an interface made of PLAs and discrete logic. Because the VME Bus spec does not include a message-passing protocol, you don't have to use an interface chip, but VME Bus boards benefit from their use as much as Multibus II boards. Moreover, the use of such chips will most likely provide some amount of commonality among the interfaces of different boards. Incompatibility hasn't been a widespread problem for VME




***Packaged in a 280-pin PGA,*** *the Force FGA-002 VME Bus chip includes a DMA controller and a dual-port RAM interface. It also implements a programmable message-passing facility.*

Manufacturers of VME Bus interface chips disagree on whether high-current bus drivers should be on or off chip.

Bus users, but some such instances have surfaced (see **box,** "VME Bus manufacturers address compatibility issues").

**VME Bus suits wide-ranging applications**

The number of available and planned VME Bus chips is an indication of the flexibility possible when implementing the interface. You can build relatively low-cost systems with half-sized VME Bus boards for factory automation, and you can also find VME Bus boards in high-performance computers and workstations. Because the spec does not tie a designer to a specific protocol such as message passing, you can tailor the interface on a board for a specific application.

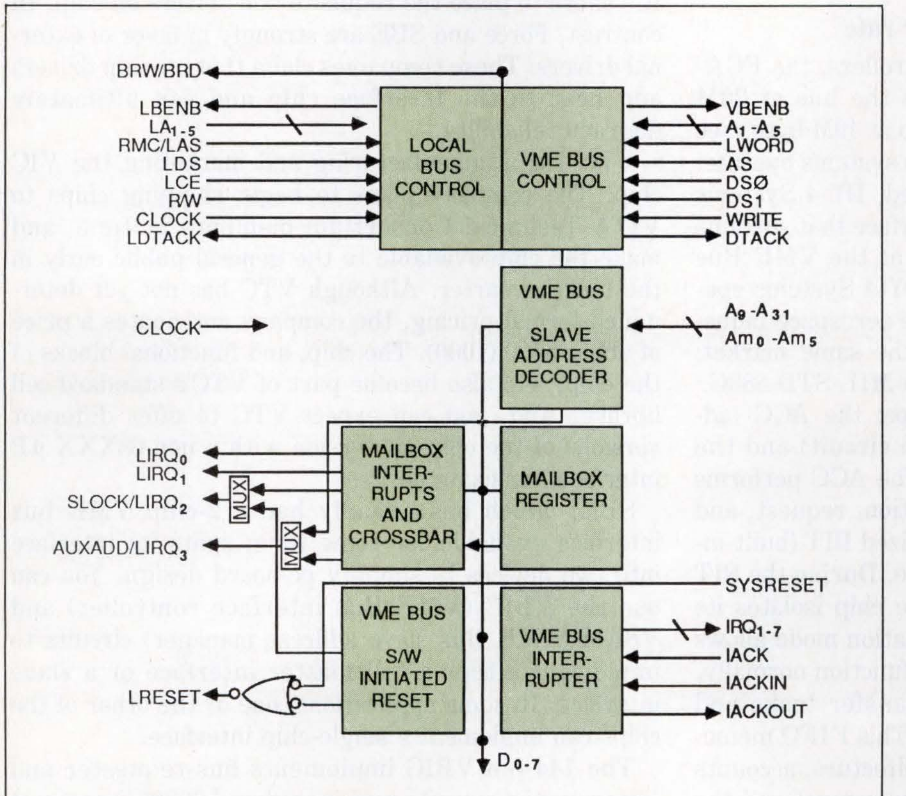
You will find few common architectures among the various VME Bus chips except that all of the chips work most effectively with the 68XXX family µPs. For now, using a different µP will force you to use a substantial amount of glue logic. Otherwise, the ICs have overlapping features, but no two manufacturers have chosen to implement the same feature set.

Force Computers chooses to implement a 2-channel message-passing capability in its FGA-002 interface chip. You can program the protocol that the chip uses to pass messages, but a board based on the chip can still operate in a shared-memory environment. The chip also includes 16 location monitors, an on-chip 32-bit DMA controller, and a dual-port RAM interface. It can implement either the VME Bus master or slave interface.

The FGA-002 is packaged in a 280-pin PGA and probably includes more overall features than the other chips available. The chip does not include a bus interrupter, however, and only includes a single-level arbiter. Some applications demand the ability to nest more levels of arbitration, or to use different schemes such as round-robin arbitration.

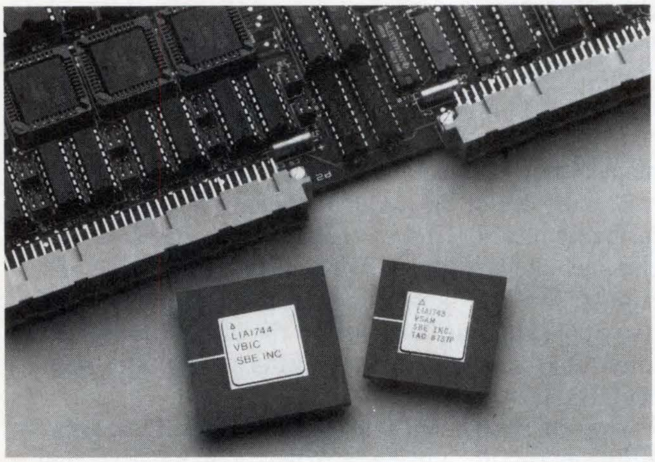
The Force IC also carries a hefty price tag. In addition to the purchase price, you have to pay a \$40,000 1-time licensing fee. The fee entitles you to a development board that includes 1 chip, a manual, 90 days of support, and 3 days of training for 3 people. The IC sells for \$690 in single quantities or \$390 in 1000-piece quantities and will be available in August.

Electronic Modular Systems Inc (EMS) has also announced plans to ship an interface chip in the third quarter. Like the chip from Force, the 208-pin-PGA




***A bus-interrupter circuit and 16 dual-ported read/write mailboxes*** *match Performance Technologies' PT-VSI interface chip to peripheral-control applications.*

## Manufacturers of VME Bus interface chips disagree on whether high-current bus drivers should be on or off chip.



*By partitioning its interface into two ICs, SBE offers designers of VME Bus boards a choice of a single-chip interface for slave applications or a 2-chip, slot-1 master implementation.*

EMS chip will include a 32-bit DMA controller, but will also contain a combination static-RAM/dynamic-RAM controller. Other features include a multimode arbiter and a bus interrupter. The company estimates that the chip will cost $300 to $400.

**Chips sustain 40M-byte/sec transfer rate**

Thanks to their on-chip DMA controllers, the FGA-002 can send bursts of data across the bus at 30M bytes/sec, and the EMS chip can do so at 40M bytes/sec—faster than most present VME Bus systems operate. For applications requiring more speed, DY-4 Systems has developed a 2-chip VME Bus interface that sustains memory-to-memory data transfers at the VME Bus theoretical limit of 40M bytes/sec. DY-4 Systems specializes in boards and systems for the aerospace industry and designed the chip set for the same market; versions will be available qualified to MIL-STD-883C.

The interface consists of two chips: the ACC (advanced system architecture control circuit) and the DARF (data address register file). The ACC performs typical functions such as bus arbitration, request, and control. The chip also offers a specialized BIT (built-in-test) function and a bus-isolation mode. During the BIT procedure, and upon any failure, the chip isolates its host board from the system. The isolation mode allows the rest of the system to continue to function normally.

The DARF chip handles data-transfer tasks and includes an 8×70-bit FIFO memory. This FIFO memory, along with a write-optimized architecture, accounts for the fast transfer rate. DY-4 Systems developed the ACC and DARF chips for use on its own boards, and is currently only offering the chip set for sale to its board and system customers. You can expect the chips to be available to the public in the third quarter, however; prices will vary from $250 to $400 per set.

**Chip targeted for universal applications**

Unlike Force Computers and DY-4 Systems, Motorola has taken the approach of building a general-purpose chip to fit the widest variety of master and slave applications. The company recently began selling its MVME6000 interface chip for $175, and is also considering licensing a third-party semiconductor house to sell the chip.

The MVME6000 includes four location monitors, a bus interrupter, multiple arbitration modes, and a system clock driver. The 6000-gate chip is packaged in a 132-pin PGA and is fabricated with a bipolar process, which supports on-chip drivers. The device includes drivers for the bus-control signals and for the lower eight data and address bits.

Of all the bus-interface ICs available, Motorola's MVME6000 and VITA's VME Bus Interface Chip (VIC) exhibit the most similarity. The designers of both ICs chose to place the requisite bus drivers on chip. In contrast, Force and SBE are strongly in favor of external drivers. These companies claim that on-chip drivers add heat to the interface chip and can ultimately degrade reliability.

VTC Inc is manufacturing and marketing the VIC chip. The company plans to begin shipping chips to VITA Technical Consortium members in June, and make the chip available to the general public early in the fourth quarter. Although VTC has not yet determined formal pricing, the company anticipates a price of about $100 (1000). The chip, and functional blocks of the chip, will also become part of VTC's standard-cell library. And, you can expect VTC to offer different versions of the chip—a version with a non-68XXX μP interface, for example.

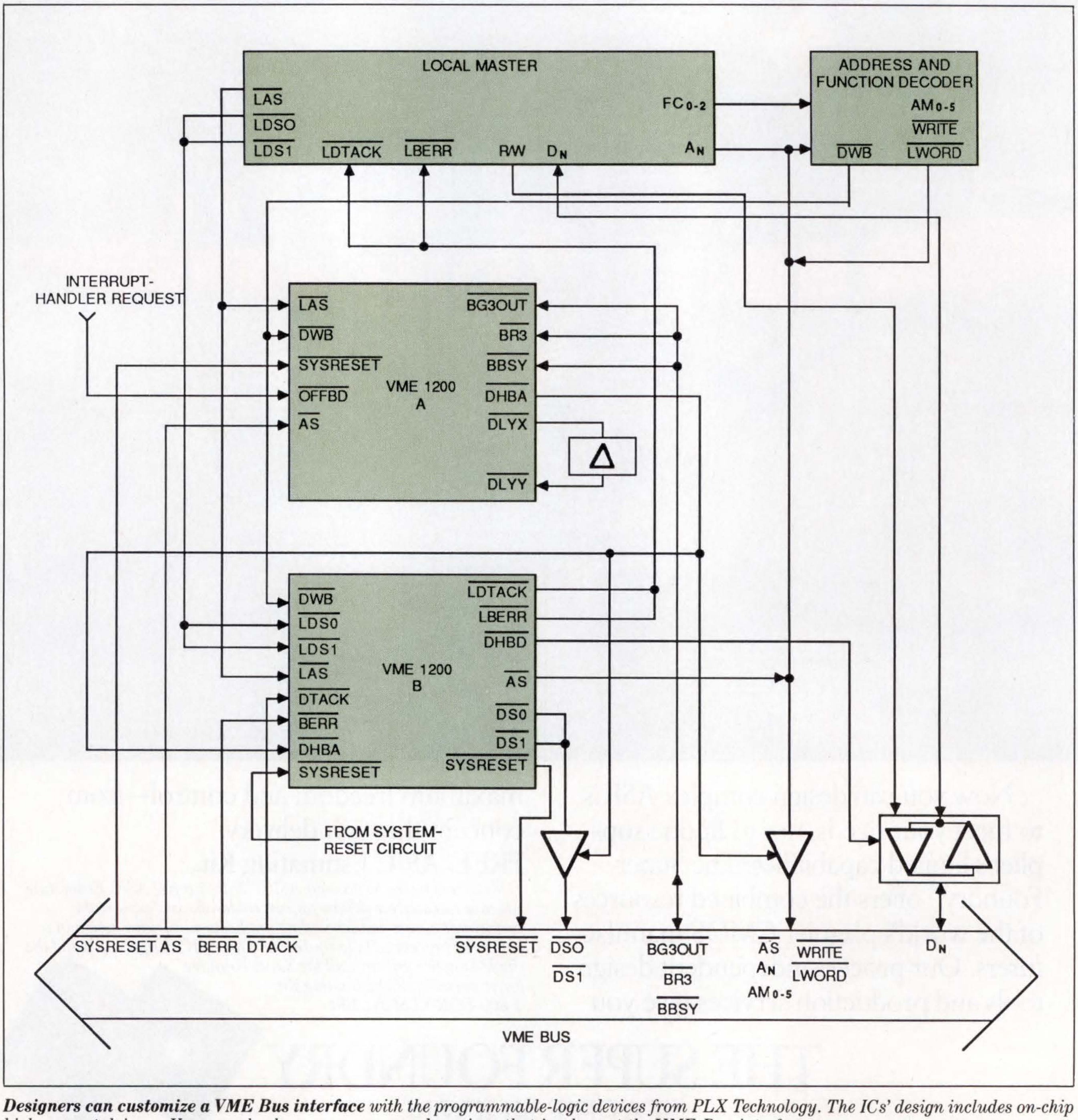
SBE, which has actually had a 2-chip VME bus interface available for some time, splits its interface into two devices to simplify pc-board design. You can use the VBIC (VME Bus interface controller) and VSAM (VME Bus slave address manager) circuits to implement either a full master interface or a slave interface. In some applications, one or the other of the chips can implement a single-chip interface.

The 144-pin VBIC implements bus-requester and -interrupter circuits and includes a 68000 interrupt controller. The 120-pin VSAM decodes bus addresses

Multibus II's local bus, the Multibus II iLBX, essentially implements nothing more than a data and address extension of the local μP's bus.

and includes the location monitor, status register, and mailbox register. The set costs \$175 (1000), but it should drop to \$125 by year's end. To obtain the ICs, you also have to make a \$1395 1-time developer-kit purchase that includes chips, manuals, documentation, and unlimited telephone support. Later this year SBE plans to introduce a second version of the VSAM chip that will be self-configuring and therefore usable as a slave interface on boards with no μP.

Two other companies have introduced chips targeted




***Designers can customize a VME Bus interface** with the programmable-logic devices from PLX Technology. The ICs' design includes on-chip high-current drivers. You can also buy preprogrammed versions that implement the VME Bus interface.*

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The VME subsystem bus includes arbitration capabilities and is suitable for hosting graphics and I/O processors.

strictly for intelligent-slave applications such as I/O controller boards. Performance Technologies introduced its PT-VSI chip last fall and has sold a number of evaluation units. The 84-pin PLCC consumes only ½W and costs $75 (100). The chip provides address-decoding functions, a bus-interrupter circuit, and 16 dual-ported read/write mailboxes. The chip can also interface with as many as four local μPs for multiprocessor applications.

Ciprico's Pipeline System Interface (PSI), enclosed in an 84-pin PLCC, includes VME Bus slave logic for control-register decoding, an interrupt generator, and the bus interface; it's up to you to add external arbitration capabilities. Actually, you can use the PSI chip on any board compatible with a bus based on the shared-memory architecture. The IC includes a pipeline to ready the next data-transfer address while a data transfer is in progress. Ciprico only plans to offer the IC in quantities of 5000 or more, and has priced the chip at less than $50 in such quantities.

### Programmable devices include bus drivers

In some cases, you may prefer to implement simple master or slave interfaces with some type of programmable logic. To that end, PLX Technology has developed a programmable-logic device with high-current outputs just for such applications. The VME 1200, for example, includes two chips that perform as a bus master. Selling for $52, the set includes a single-level arbiter and a bus requester. For slave applications, PLX offers the single-chip VME 2000 for $26. This interface supports address pipelining and block-move data transfers.

PLX will also support your efforts to customize one or more programmable devices for your application. You can start with a preprogrammed device such as the VME 2000, and modify the programming codes to meet your needs. PLX also offers a device for the Micro Channel bus (see **box,** "ICs mate cards to Micro Channel size/power specs"). The VSB 1200 and VSB 2000 are intended for master and slave VSB (VME Subsystem Bus) implementations; each of these cost $26.

The VME Bus industry has accepted the VSB as the standard local bus for the VME Bus. You can employ the VSB to expand the functionality of a VME Bus board and maintain the system-on-a-board concept. Motorola offers a full VSB master/slave chip, the MVSB2400, for $175. The chip includes master-mode control logic, a master and slave block-transfer control module, the VSB requester, the VSB arbiter, a time-

## Manufacturers of bus-interface ICs

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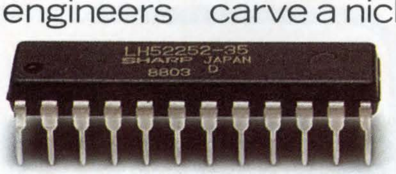


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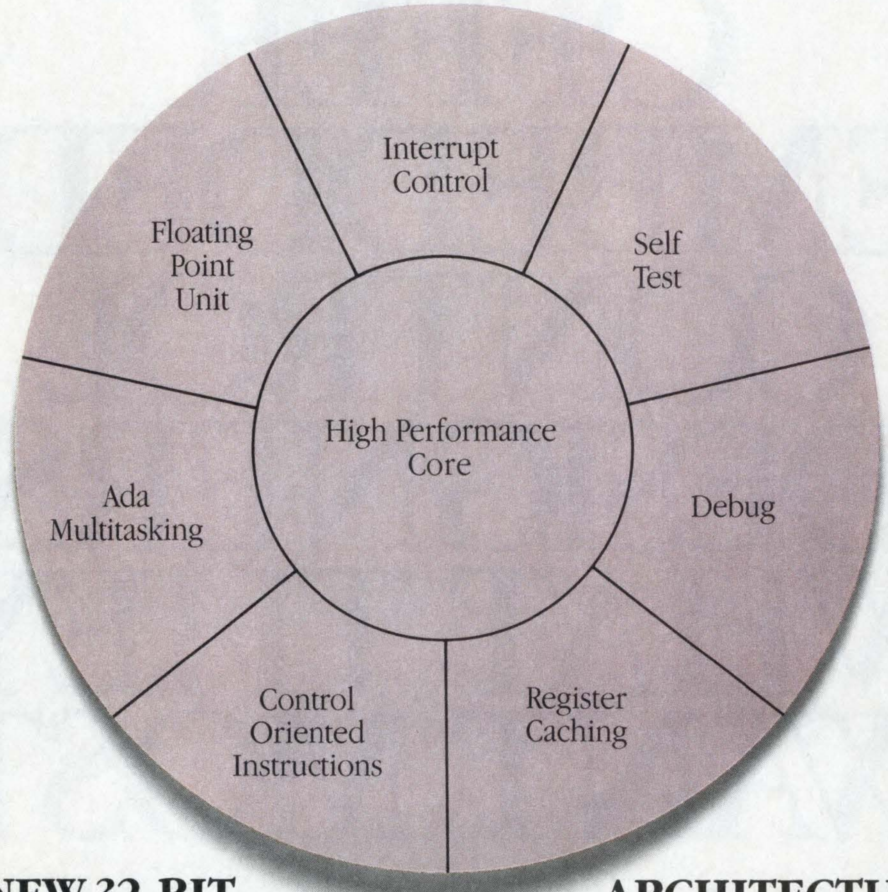


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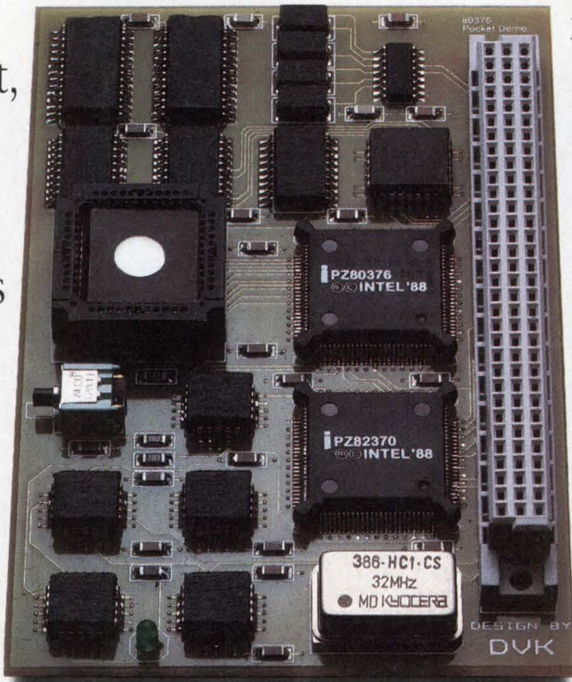


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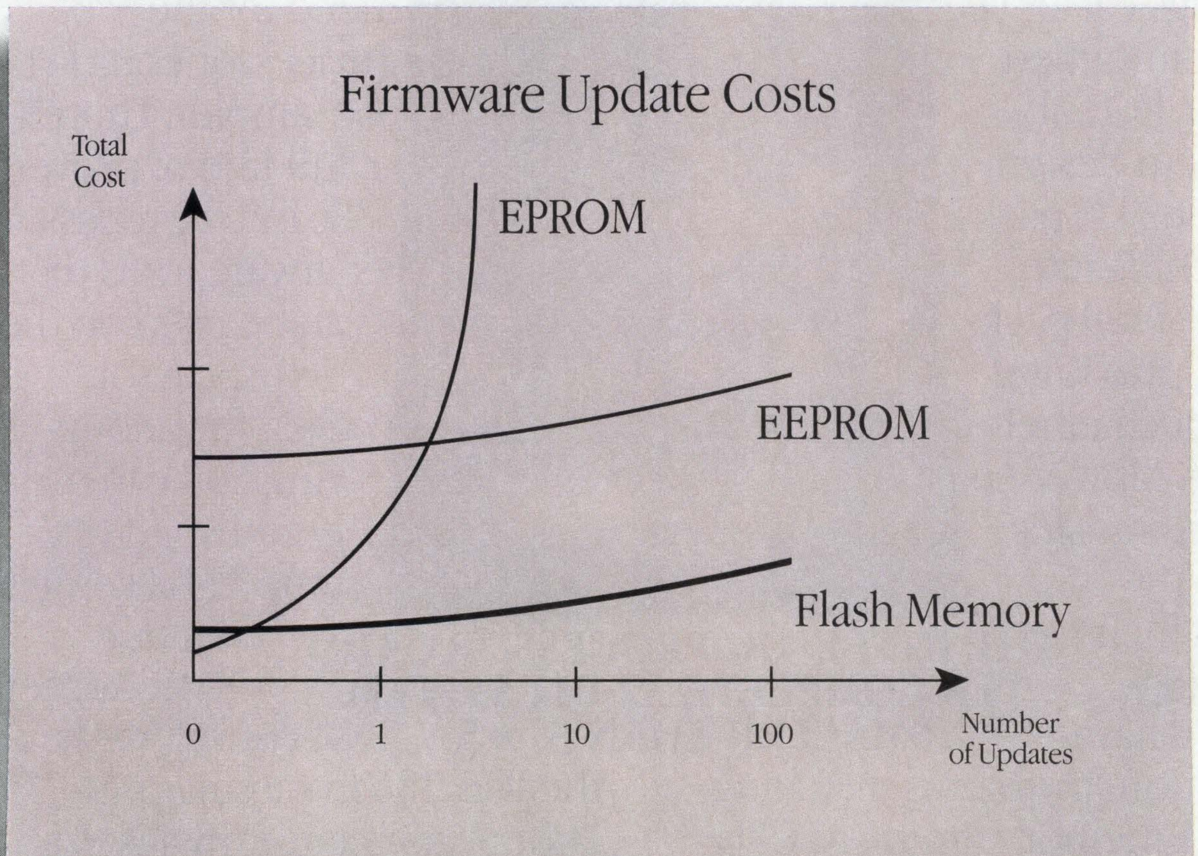


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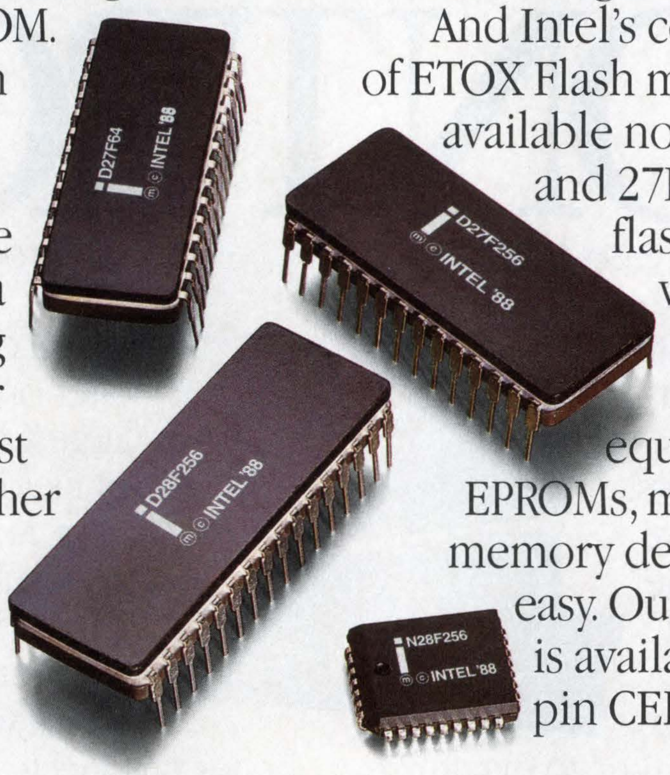


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|---|---|---|
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# Clever techniques improve thermocouple measurements

*Thermocouple (TC) measurements require linear-circuit proficiency. To ensure accurate results, you should understand the need to compensate for parasitic junctions, the importance of certain characteristics of the op amps and associated components, and the ways to otherwise condition and linearize the TC's low-level output signals.*

Jim Williams, *Linear Technology Corp*

Thermocouples are inexpensive, but achieving reasonable accuracy—say ±0.5°C—requires careful signal conditioning and cold-junction compensation. Although thermocouples don't require any external excitation, and their small size and low output impedance produces wideband, low-noise output signals, their nonlinear, millivolt-level outputs degrade measurement sensitivity.

A TC senses ambient temperature by producing, across the junction, a small voltage proportional to temperature. To measure that voltage, you must connect the TC wires to an amplifier or voltmeter, creating two unwanted parasitic junctions that produce error voltages in series with the desired signal (**Fig 1**). These parasitic junctions must have the same temperature. To interpret the TC voltage as an absolute-temperature signal, you must either maintain these parasitic junctions at a known temperature or compensate for their effect electronically. The TC, in effect, measures temperature at its "hot" junction with respect to temperature at the two parasitic junctions—historically called the "cold junction."

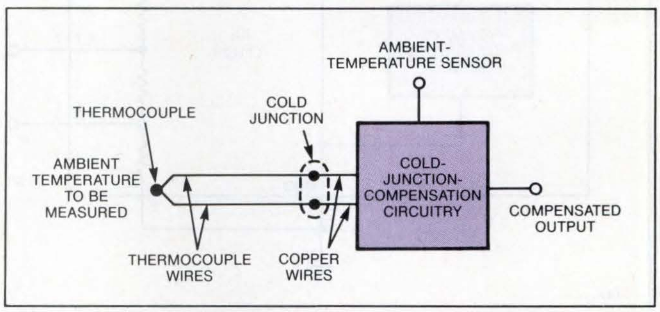



***Fig 1—For accurate thermocouple measurements,*** *the thermocouple's cold junction and the compensation circuit's temperature sensor must be isothermal.*

## Cold junctions generate spurious voltage

The term "cold junction" derives from the practice of maintaining the parasitic junctions at 0°C by immersing them in a mixture of ice and water. Although very accurate, this approach is impractical for most applications. As another option, you can simulate the ice bath by servo-controlling a Peltier cooler, but again this approach is too complex and bulky for most applications.

*Thermocouples are by far the most widespread contact-type temperature transducers in use today.*

A better technique **(Fig 2a)** employs an electronic-compensation circuit, which tracks the cold-junction temperature instead of maintaining the junction at a constant temperature. The circuit offers the same result as an ice bath, but is simpler to implement. It produces 0V at 0°C, and its slope of output voltage vs temperature is the same as that of the thermocouple, over the expected range of cold-junction temperatures. For proper operation, the compensator's temperature sensor must be isothermal with the cold junction.

The cold-junction compensator, $IC_1$, measures the cold-junction's ambient temperature and generates output voltages that are scaled for use with E-, J-, K-, R-, S-, and T-type thermocouples. Low supply current in

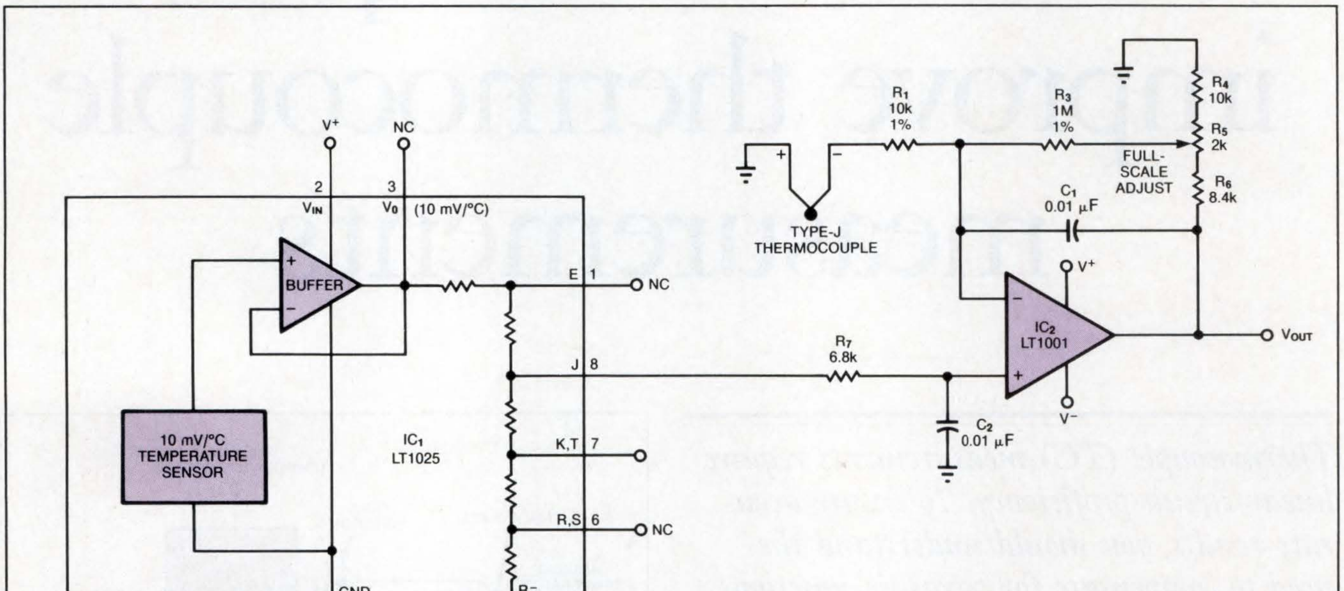



***Fig 2—Each of these circuits combines the thermocouple's output** with the electronic cold-junction compensation of $IC_1$. Circuit **a** subtracts these voltages; circuit **b** arranges the voltages in a series-opposed fashion and amplifies the difference.*

$IC_1$ minimizes the self-heating that would otherwise degrade isothermal operation with the cold junction; low power consumption also supports battery operation. The chip's ±0.5% accuracy is compatible with the overall accuracy achievable in a thermocouple-based system.

### Subzero temperature swings $V_{OUT}$ negative

The op amp in **Fig 2a** amplifies the difference between the thermocouple voltage and the cold-junction-compensation voltage from $IC_1$. $C_1$ and $C_2$ provide filtering, and potentiometer $R_5$ trims the signal gain. $R_6$ has a typical value; another value may better accommodate the desired trim range. Reducing $R_6$ and increasing $R_5$, for example, will provide higher gain with lower trim resolution. **Fig 2b** shows a similar circuit, for a type-K thermocouple, which combines the TC and compensation voltages in series-opposed fashion. The optional pulldown resistor ($R_4$) allows $V_{OUT}$ to swing negative, thereby representing sub-0°C temperatures.

Low bias current in $IC_2$ is important to avoid offset errors due to the op amp's input filter ($R_7$, $C_2$) and the output impedance of $IC_1$. Type-J, -K, -E, and -T thermocouples, which have Seebeck coefficients of 40 to 60 μV/°C, require high-grade precision bipolar amplifiers such as **Fig 2b**'s LTKA001. (This device provides 30-μV offset voltage, 1.5-μV/°C drift, and 1-nA input bias current.)

Particularly critical applications call for a chopper-stabilized amplifier such as **Fig 2b**'s LTC1052 (5-μV offset, 0.05-μV/°C drift, 30-pA input bias current, and $30\times10^6$ open-loop gain). This amplifier is appropriate for use with type-R and -S thermocouples (whose Seebeck coefficients range from 6 to 15 μV/°C), especially if the application covers a large swing in ambient temperature or does not allow offset adjustments.

Another source of error in thermocouple amplifiers is inadequate open-loop gain. An amplifier for type-K thermocouples, for instance, which produces 100 mV/°C, must have a closed-loop gain of 2500. In this application, an ordinary op amp that specs a minimum open-loop gain of $50\times10^3$ would produce a $(2500/50{,}000)\times100=5\%$ gain error! Although normally you would calibrate the closed-loop gain by trimming, temperature drift in the open-loop gain can still degrade the output accuracy. The minimum recommended open-loop gain for use with type-E, -J, -K, and -T thermocouples is 250,000. This value is also adequate for use with type-R and -S thermocouples, if the amplifier's output produces 10 mV/°C or less.

### Eschew kovar package leads

Regardless of the type of op amp that you choose, a dual-in-line package is preferable to a TO-5 metal can, especially if the op amp's supply current exceeds 500 μA. The TO-5's kovar leads introduce thermocouple effects that can generate ac and dc offsets in the presence of external air motion or thermal gradients in the package.

You should also be aware of considerations related to, but external to the thermocouple amplifier itself. These include overvoltage protection, common-mode voltage, and noise. Protection is necessary because thermocouple wires often pick up static voltages or make contact with high voltage that can damage the amplifier circuit.

The $R_{LIMIT}$ resistor in **Fig 3a,** for instance, attenuates

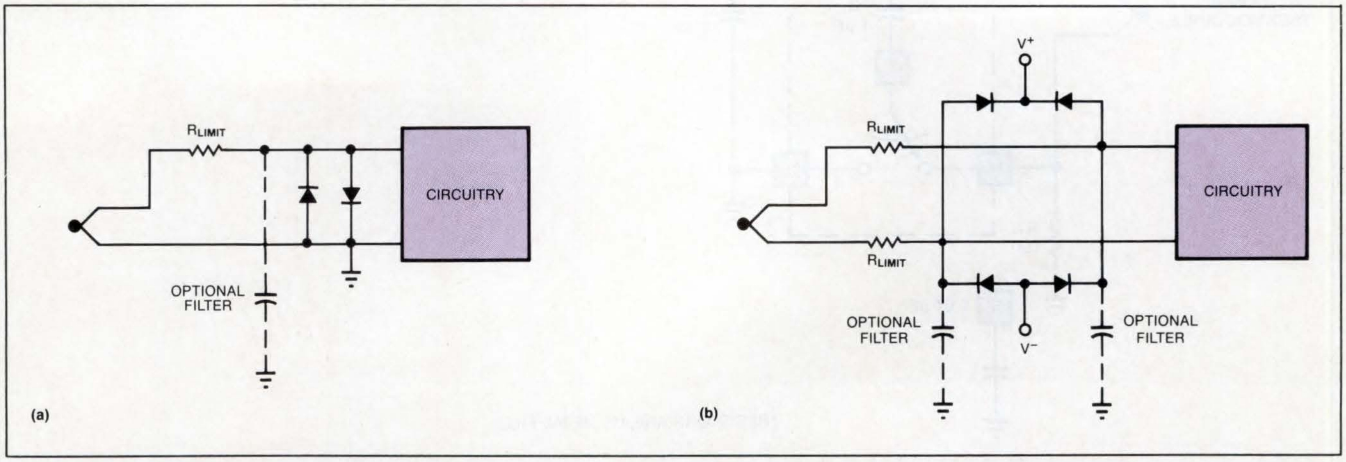



***Fig 3—The resistors you see here protect the circuits*** *from overvoltage on the thermocouple lines. The optional capacitors provide signal filtering for grounded or battery-operated systems **(a)**, or for systems **(b)** subject to open ground connections or open thermocouple lines.*

*Electronic cold-junction compensation tracks the junction temperature instead of maintaining the junction at a constant temperature.*

fault voltages. And, by adding a capacitor (shown as dashed lines), you can obtain signal filtering as well. **Fig 3b**'s circuit shows balanced protection for a differential input. Again, connecting the optional capacitors provides lowpass signal filtering in addition to overvoltage protection. The diodes are effective in clamping the signal path to the supply voltages, but you must evaluate the effect of diode-leakage currents, especially if the limit resistors have high values. Similarly, bias currents flowing into the amplifier circuitry through high-value limit resistors can generate measurement errors. In some cases you must compromise accuracy to meet a system's requirements for voltage protection and noise rejection.

The amplifier circuit of **Fig 4** combines filtering with full differential sensing of the thermocouple voltage. If all signals remain within the supply-voltage range of the switched-capacitor building block ($IC_1$), the circuit provides 120 dB of common-mode rejection. (If the signals exceed this range, the circuit may require protection networks as discussed with regard to **Fig 3**.) Switch action within $IC_1$ transfers charge from the external "flying capacitor" $C_1$ to the external output capacitor, $C_2$. You can vary this rate of transfer, and hence the overall bandwidth, by controlling the chip's commutating frequency. Resistor $R_1$ provides a bias-current path for $IC_1$'s floating inputs, and the pulldown resistor (shown as dotted lines) enables subzero-temperature readings.

Protection networks and differential operation may not suffice in thermocouple applications that have high levels of noise and common-mode voltage. Industrial

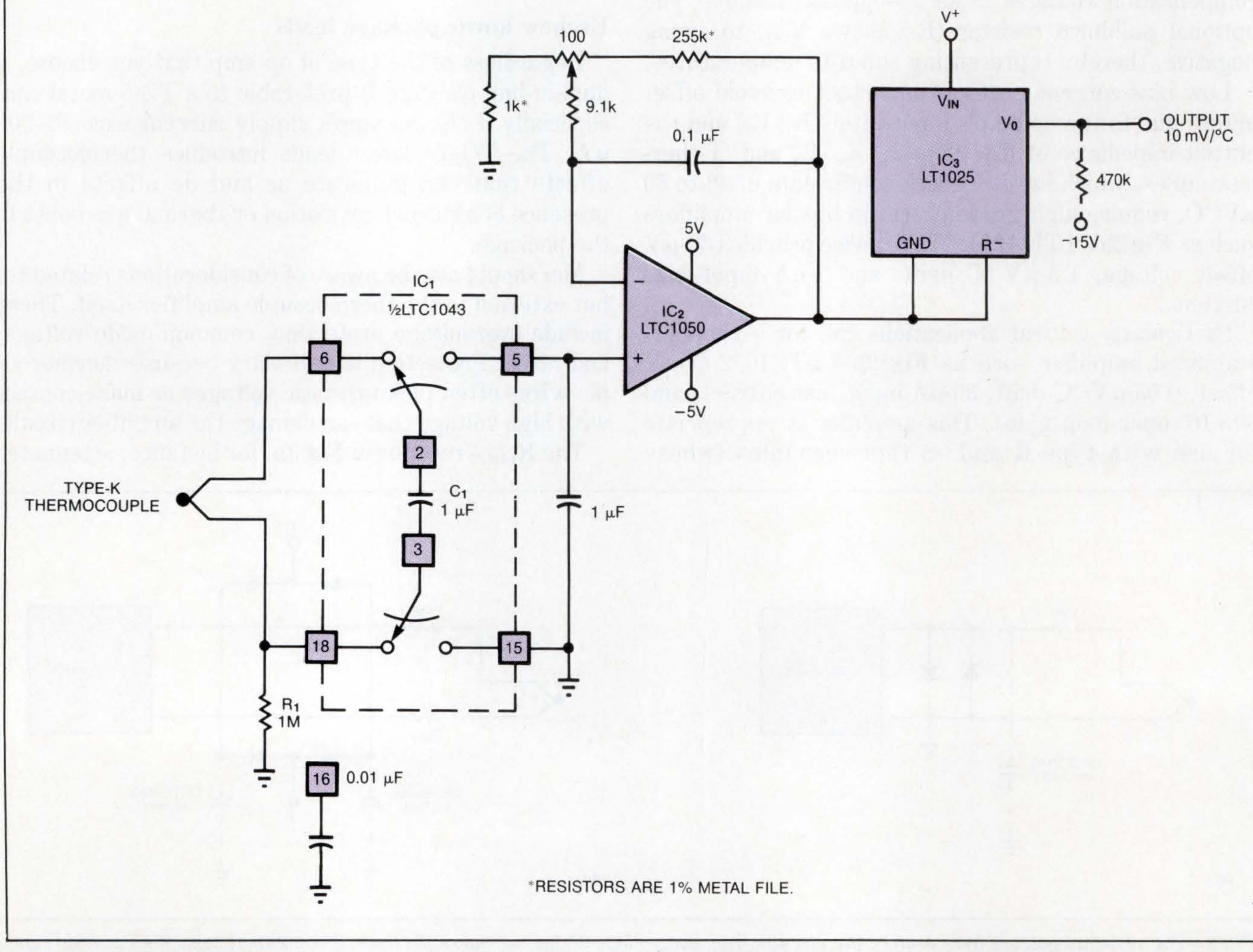
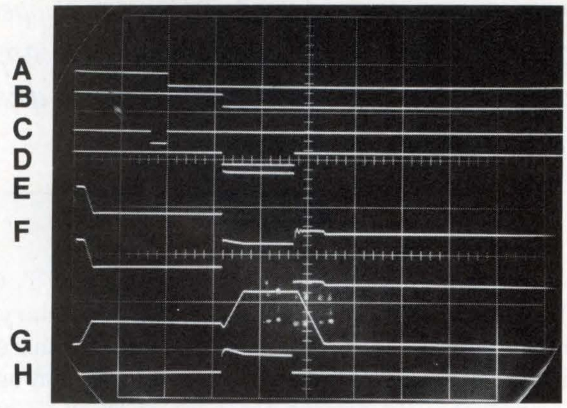



***Fig 4—This differential-input thermocouple amplifier*** *implements "flying capacitor" isolation with a switched-capacitor circuit ($IC_1$).*




| TRACE | VERTICAL | HORIZONTAL |
|---|---|---|
| A | 50V/DIV | 50 μSEC/DIV |
| B | 50V/DIV | 50 μSEC/DIV |
| C | 50V/DIV | 50 μSEC/DIV |
| D | 50V/DIV | 50 μSEC/DIV |
| E | 10V/DIV | 50 μSEC/DIV |
| F | 10V/DIV | 50 μSEC/DIV |
| G | 10V/DIV | 50 μSEC/DIV |
| H | 50 mA/DIV | 50 μSEC/DIV |

***Fig 6—These waveforms depict selected signals from Fig 5's circuit.*** *The negative-pulse level in trace E, for example, represents the desired thermocouple temperature.*

environments, for example, can generate ground-potential differences of 100V or more. For these conditions, you must galvanically isolate the thermocouple and its signal-conditioning circuitry from ground. The circuit requires a fully isolated power source and an isolated signal-transmission path that is referred to ground at the output. Careful design allows a single path to transfer both the floating power and the isolated signals. What's more, thermocouples allow you to trade bandwidth for dc accuracy.

**One transformer isolates signal and power**

The isolated signal conditioner of **Fig 5** provides ±0.25% accuracy in the presence of 175V common-mode voltages. A single transformer, $T_1$, transmits the isolated power and data. First of all, take note of the oscillator circuit consisting of inverter $IC_{1A}$ and associated components, which generates the clock signal shown in **Fig 6,** trace A. Inverters $IC_{1B}$, $IC_{1C}$, and associated components stretch the positive pulses in this signal (trace B), and apply them to the 2.2-kΩ resistor, $R_1$. The pulse amplitudes are stable because the inverters obtain a stable supply voltage from the (approximate) 10.7V regulator consisting of $IC_2$ and $IC_3$.

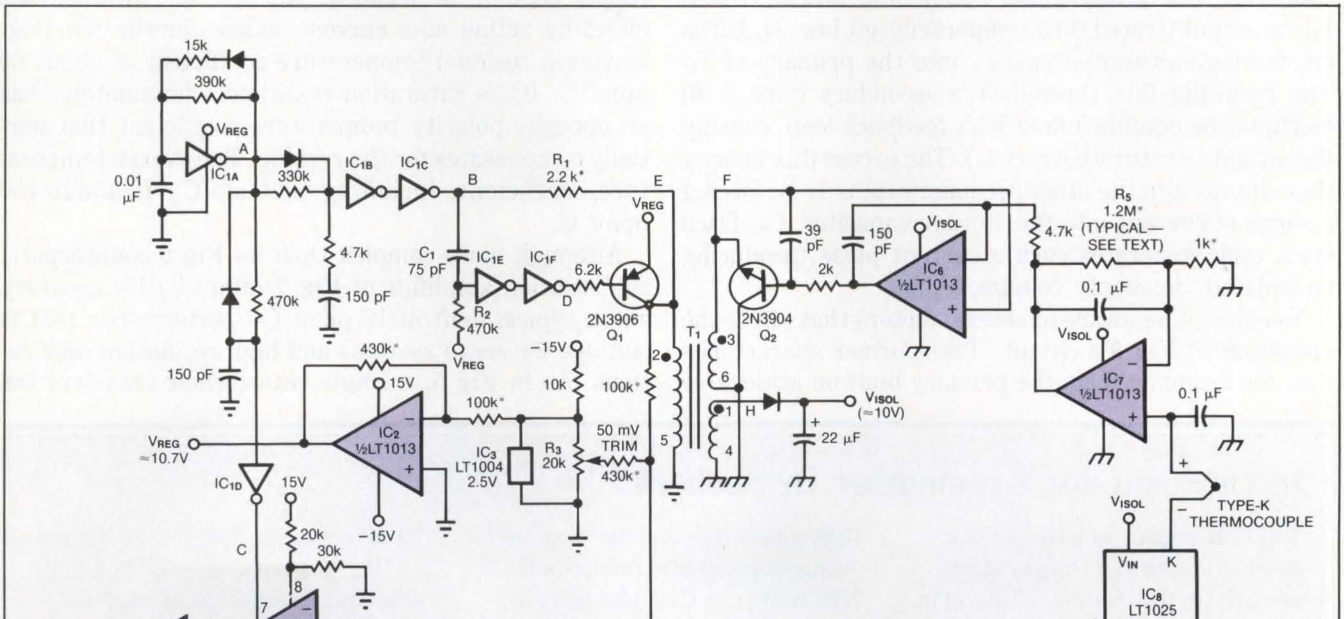



***Fig 5—Transformer $T_1$ provides 175V isolation*** *for the power and signals of this thermocouple-signal conditioner. Accuracy is ±0.25%.*

*Protection networks and differential operation may not suffice in thermocouple applications that have high levels of noise and common-mode voltage.*

Current pulses in $R_1$ drive the primary of $T_1$ (trace E), producing voltage pulses in the secondary (the emitter of $Q_2$, trace F). Op amp $IC_6$ compares this signal with the conditioned thermocouple voltage that op amp $IC_7$ produces. By driving the base of $Q_2$, $IC_6$'s output (trace G) forces the transformer's secondary voltage (pin 3) to clamp at the level of $IC_7$'s output. The clamping action is active for low output voltages because $Q_2$ operates in the inverted mode.

$T_1$'s primary voltage clamps in response to a clamp on the secondary voltage. After $IC_6$'s output settles, the stable, clamped primary voltage represents the thermocouple's output signal. Meanwhile, a delayed clock signal (trace C) from inverter $IC_{1D}$ controls the sample/hold amplifier, $IC_4$, causing that device to sample the $T_1$ primary voltage. $IC_4$ returns to the hold mode when the clock waveform (trace A) goes low. Potentiometer $R_3$ adjusts the sample/hold signal's offset, and potentiometer $R_4$ adjusts the gain.

When $IC_{1C}$'s output (trace B) makes a high-to-low transition, the differentiator action of $C_1$ and $R_2$ causes $IC_{1F}$'s output (trace D) to temporarily go low. $Q_1$ turns on, forcing substantial energy into the primary of $T_1$. The resulting flux through $T_1$'s secondary (pins 3, 6) disrupts the equilibrium of $IC_6$'s feedback loop, causing the output to saturate (trace G). The excess flux energy then dumps into the other secondary (pins 1, 4), forcing a surge of current into the storage capacitor, $C_3$. Each clock cycle generates such a current pulse, producing an isolated, dc supply voltage, $V_{ISOL}$.

You should be aware of several factors that affect the operation of **Fig 5**'s circuit. Transformer characteristics, for example, form the primary limit on achievable accuracy. The clamping scheme relies on avoiding saturation of the transformer's core. The clamp interval must be short, and $T_1$'s primary current during this interval should remain extremely low with respect to the core-saturation value. The power-refresh pulse occurs immediately after the data transfer rather than before, to allow a pause for the transformer's core to recover from saturation. The low clock frequency (350 Hz) ensures adequate time intervals for this purpose; the resulting low bandwidth is not of consequence in most thermocouple applications.

To trim the circuit's gain, select $R_5$ ($IC_7$'s feedback resistor) according to the desired maximum temperature and the thermocouple type. You should set $IC_7$'s output to 50 mV before adjusting the offset trim ($R_3$); the circuit cannot read $IC_7$ outputs below 20 mV because of saturation in $Q_2$. The drift of the output voltage vs temperature depends on constant-magnitude current pulses into the primary winding of $T_1$, which in turn depends on the temperature coefficient of the copper used in the winding. $R_1$, however, swamps this effect by acting as a current source for the winding, leaving a residual temperature coefficient of about 60 ppm/°C. $IC_{1C}$'s saturation resistance, fortunately, has an opposite-polarity temperature coefficient that partially compensates for the residue. The overall temperature coefficient, including that of $IC_3$, is about 100 ppm/°C.

Although more complex than its **Fig 5** counterpart, the isolation amplifier of **Fig 7** offers 0.01% accuracy and a typical drift of 10 ppm/°C—performance that is suitable for servo systems and high-resolution applications. As in **Fig 5,** a single transformer transfers the

## In case you don't remember Dr Seebeck

Thermocouples are by far the most widespread temperature sensors in use today. Their principle of operation, however, dates back to 1822, when an Estonian physician discovered the thermocouple effect by accident. While studying the effects of heat on galvanic connections, Thomas Seebeck joined a piece of copper to a piece of bismuth, forming a loop. He then noted that a nearby compass was indicating a magnetic disturbance. Not realizing that electric current was flowing, Seebeck labeled the effect "thermomagnetism."

He went on to experiment with different combinations of metals and eventually published the results of his work **(Ref 1).** Further investigations, of course, have established that "thermomagnetism," now known as the "Seebeck effect," is a reliable and repeatable electrical phenomenon.

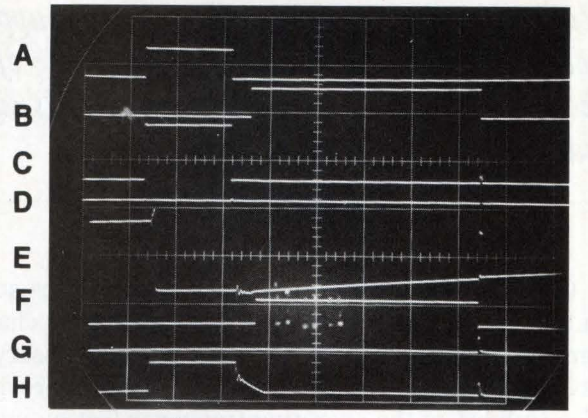
### Reference

1. Seebeck, Thomas, *Magnetische polarisation der metalle und erze durch temperatur-differenz*, Abhaandlungen der Preussischen Akademic der Wissenschaften, 1823, pg 265-373.

isolated data and power. The thermocouple voltage, however, undergoes pulse-width modulation before coupling across the transformer. The circuit then demodulates this signal back to dc.

Again, inverter $IC_{1A}$ generates the clock waveform (**Fig 8**, trace A). This waveform's high-to-low transition sets flip-flop $IC_2$ (trace B), after a small delay introduced by inverters $IC_{1B}$, $IC_{1C}$, and associated components. The clock signal, buffered by inverters $IC_{1D}$ and $IC_{1E}$, also drives the primary of $T_1$ (trace C). As a result, the $T_1$ secondary receives energy and delivers it to the storage capacitor, $C_1$, creating $V_{ISOL}$, the isolated supply voltage for that side of the circuit.

Besides generating $V_{ISOL}$, pulses in the $T_1$ secondary clock the pulse-width modulator, a closed-loop circuit that includes $IC_{4B}$, $IC_{6B}$, $IC_{7A}$, and $IC_{7B}$. Op amp $IC_8$ amplifies the thermocouple signal and applies it to the noninverting input of $IC_{6B}$, which in turn servo-biases comparator $IC_{7A}$. Each time that $IC_{7B}$ allows $C_2$ (trace E) to receive charge via resistor $R_1$, $IC_{7A}$ produces a pulse whose duration is proportional to the thermocouple voltage. After inversion by $IC_{2A}$, these pulses also drive the $R_2/C_3$ integrator, which delivers a dc voltage to the inverting input of $IC_{6B}$. $C_6$ provides compensation for the feedback loop.




| TRACE | VERTICAL | HORIZONTAL |
|---|---|---|
| A | 20V/DIV | 50 μSEC/DIV |
| B | 20V/DIV | 50 μSEC/DIV |
| C | 10V/DIV | 50 μSEC/DIV |
| D | 20V/DIV | 50 μSEC/DIV |
| E | 2V/DIV | 50 μSEC/DIV |
| F | 10V/DIV | 50 μSEC/DIV |
| G | 10V/DIV | 50 μSEC/DIV |
| H | 20V/DIV | 50 μSEC/DIV |

*Fig 8—The positive pulse width in trace B of the Fig 7 circuit corresponds to the thermocouple's temperature.*

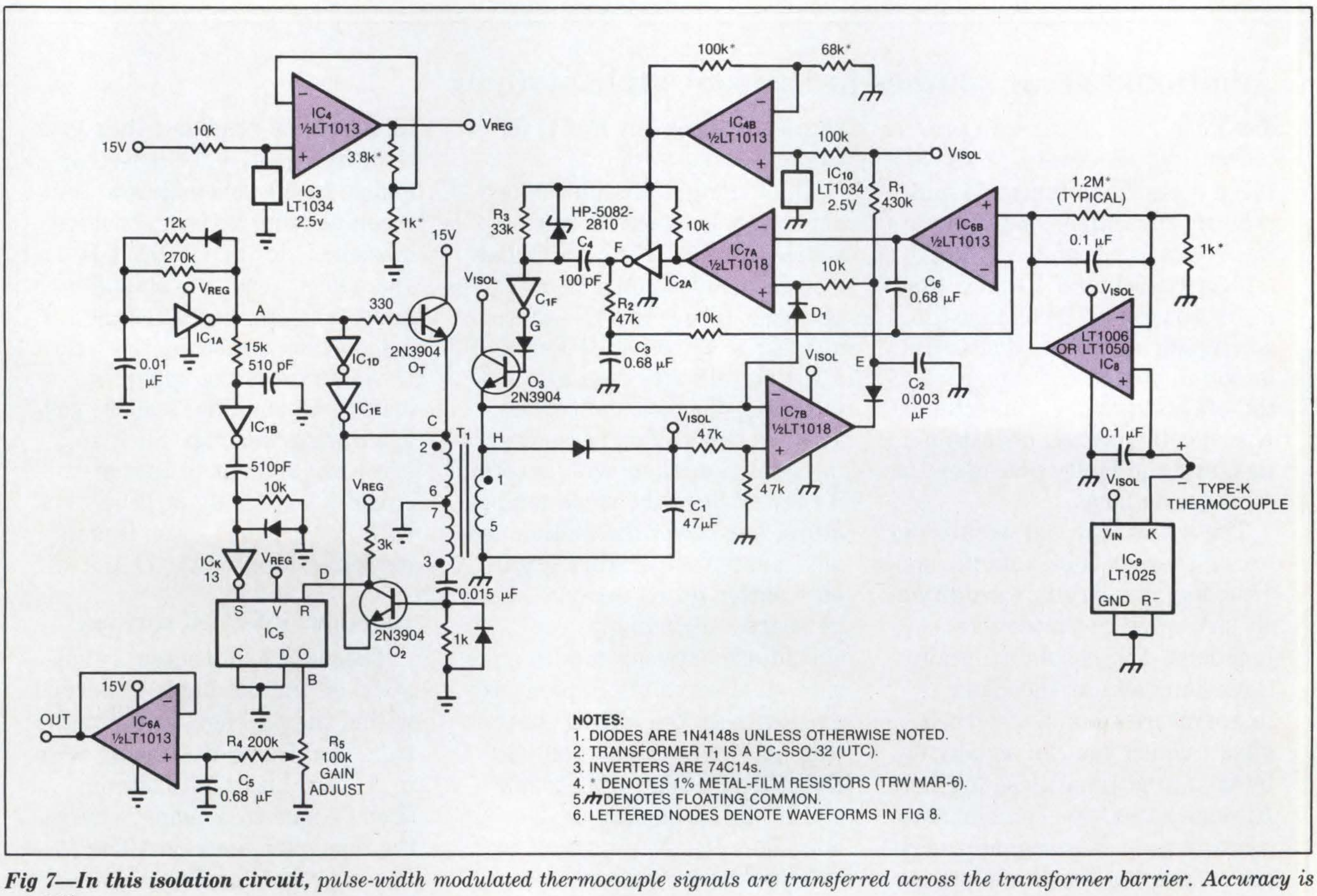



*Fig 7—In this isolation circuit, pulse-width modulated thermocouple signals are transferred across the transformer barrier. Accuracy is ±0.01%.*

*Variations in ambient temperature, supply voltage, and clock frequency have little effect on the PWM isolation amplifier's signal output.*

Circuit accuracy demands stable pulse widths at the output of $IC_{2A}$. $IC_{2A}$'s low-loss, MOS switching characteristics contribute to the precise timing necessary, as does the stabilized supply voltage that $IC_{4B}$ provides. The stability of the operating frequency (set by inverter $IC_{1A}$) has little effect on the pulse widths because this frequency is common to the primary-side demodulation scheme.

Demodulation proceeds as follows: $C_4$ and $R_3$ differentiate the negative-going edge of $IC_{2A}$'s output, causing $IC_{1F}$ to deliver a pulse (trace G) to the base of $Q_3$. In response, $Q_3$ delivers a fast spike to $T_1$'s secondary (trace H). (Diode $D_1$ at $IC_{7A}$'s noninverting input breaks a regenerative loop that could cause oscillation.) $T_1$'s primary section between pins 7 and 3 receives the spike, which then drives the base of $Q_2$. $Q_2$ behaves as a clocked demodulator, pulling its collector low (trace D) only when its base is high and its emitter is low—when $T_1$ is transferring data rather than power.

The collector spike from $Q_2$ resets flip-flop $IC_5$. Like $IC_{2A}$, this flip-flop is an MOS device powered by a stable supply (obtained from $IC_4$), and clocked by the same frequency as the pulse-width modulator. As a result, the flip-flop's Q output signal has a dc-average value that depends primarily on the desired thermocouple signal at $IC_8$'s output. Variations in the ambient temperature, supply voltage, and clock frequency have little effect.

**Delay translates to offset error**

Filter components $R_4$ and $C_5$ extract the signal's dc value; $R_5$ permits adjustment of the overall gain. The voltage follower, $IC_{6A}$, produces the circuit's output. Because this scheme depends on the accurate timing of edge signals at the flip-flop, you must account for the small delay in discharging $C_2$ (trace E) to avoid a small offset error. The delay in $IC_5$'s S (set) line compensates for this error by setting the rising edge of trace B coincident with that of trace F. Trace B's falling edge requires no such compensation because wideband cir-

## Additional error sources in thermocouple systems

You must exercise care in processing the low-level signals that thermocouples produce. In general, thermocouple *system* accuracies greater than 0.5°C are difficult to achieve. Besides the major sources of error that the accompanying article discusses in detail, you should be aware of the effects that the connection wires, cold-junction uncertainties, and the faulty placement of sensors can have.

The wires that you use to connect a thermocouple and its conditioning circuitry form additional, unwanted thermocouple junctions. You should maintain these junctions at the same temperature to minimize their effect, which you can usually do by mounting them close togther. In some cases, you can eliminate a junction by selecting appropriate connecting wires and other accessories; consult **Ref 1**, for example.

The joining of dissimilar metals always produces a thermocouple junction. Such dissimilar metals include the leads of IC packages (kovar in TO-5 cans; alloy 42 or copper in DIPs), and a variety of other metals found in plating finishes and solders. The net effect of all these thermocouple junctions will be zero if they all have the same temperature, but power dissipation usually causes temperature gradients within an IC package or a pc board. Accordingly, you should use extreme care to ensure an absence of temperature gradients, in the vicinity of the thermocouple terminations, in the cold-junction compensator, and in the thermocouple amplifier.

If you can't eliminate a given temperature gradient, then position the sensitive leads isothermally. In the schematics in the accompanying article, sensitive leads include the LT1025's $R^-$ and output pins, the amplifier-input pins, and leads for the gain-setting resistors. One effect to watch for is the apparent drift in an amplifier's offset voltage during warmup. Such an error can amount to tens of microvolts, especially in TO-5 cans with kovar leads—even if drift measures zero for the chip itself.

**Junctions infest IC package**

The culprit, of course, is mismatched thermocouple materials within the package, in the path from lead frame to bonding wire to IC metallization to silicon. (Lead frame to bonding wire is the dominant junction.) The effect is proportional to power dis-

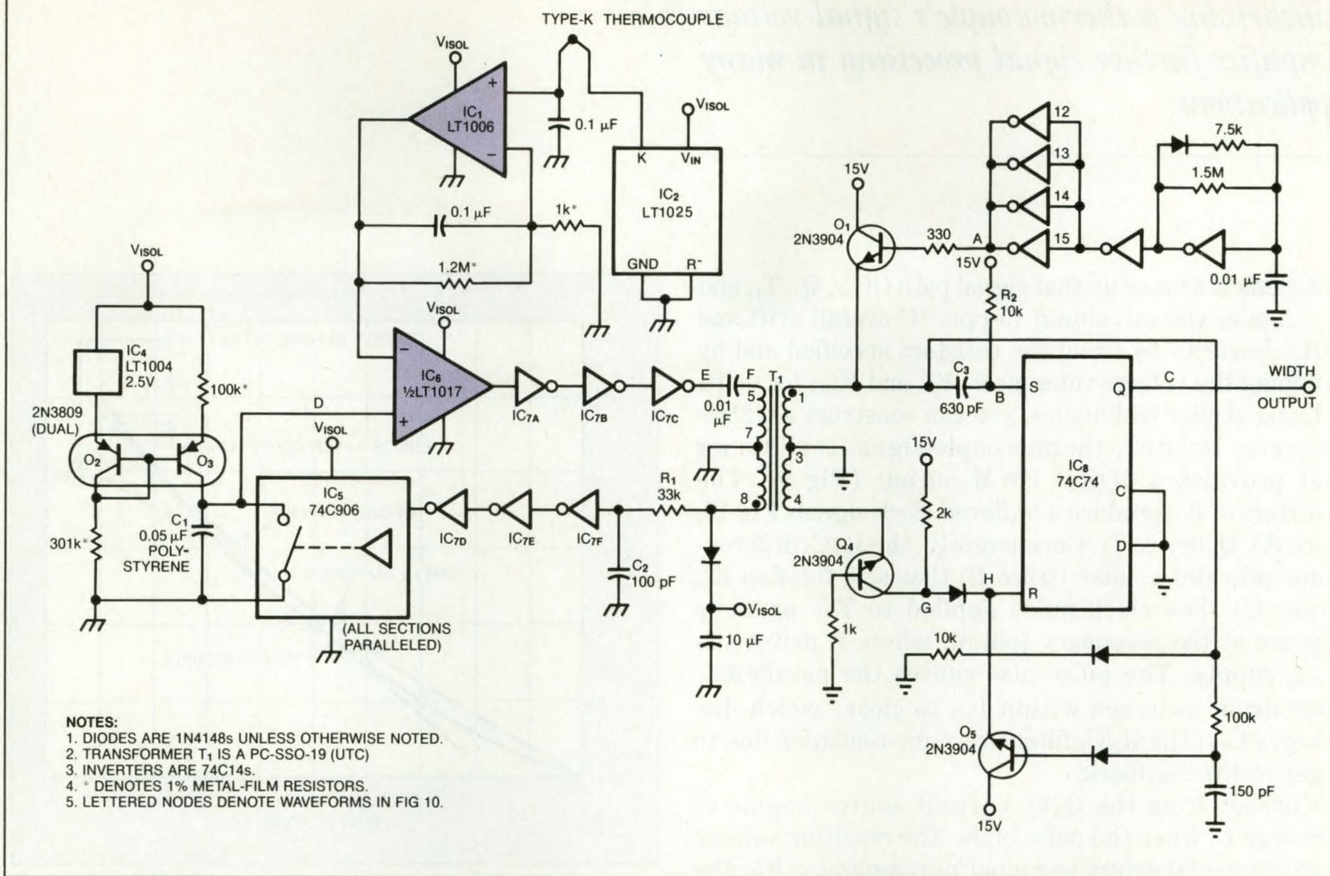



***Fig 9—This thermocouple amplifier** provides signal conditioning, isolation, and a pulse-width modulated output.*

sipation, and you can minimize it by choosing ICs that draw low supply current, by operating them at low supply voltages, and by avoiding TO-5 cans. You can accommodate the remaining drift by specifying a 5-minute warmup before calibrating the system or measuring its performance.

The thermocouple's cold junction is another significant source of error. A true cold junction (ice-bath reference) will contribute error according to slight deviations from the desired temperature, but an active-compensator IC makes errors in the process of sensing and tracking the ambient temperature. You must take measures to ensure accurate tracking by maintaining the cold junction and the IC at the same temperature. These measures include the use of high-thermal-capacity blocks and thermal shrouds.

Because a thermocouple measures its own temperature, the placement of the thermocouple can also be a source of error. In fluid systems, for instance, eddy currents or the effects of laminar flow around the thermocouple can cause remarkably large errors. Even a simple surface measurement can be inaccurate because of poor thermal conductivity between the surface and the sensor.

Silicone thermal grease can ease this problem, and you should mate as much of the sensor surface as possible to the measured surface. (Ideally, the thermocouple should lodge tightly in a hole drilled in the surface.)

Keep in mind that thermocouple leads act as heat pipes that provide direct thermal paths to the sensor. This isn't a problem if the surface has a large thermal capacity, but other situations may require some thought. For example, you might thermally mate the lead wires to the surface. Also, coiling the wires within the ambient temperature of interest will minimize their heat-pipe effects. You should be skeptical of results, even for applications that are apparently simple. Experiment with several sensor positions and mounting options, and if the results agree you are probably on the right track.

## Reference

1. *Omega temperature measurement handbook*, Omega Engineering, Stamford, Connecticut, 1987.

*Linearizing a thermocouple's signal voltage simplifies further signal processing in many applications.*

cuit elements make up that signal path ($IC_{1F}$, $Q_3$, $T_1$, and $Q_2$). Again, you can obtain 10-ppm/°C overall drift and 0.01% linearity by using the resistors specified and by matching the voltage references, $IC_3$ and $IC_{10}$, for drift.

Using similar techniques, you can construct a 0.25%-accurate, isolated, thermocouple-signal conditioner that provides a digital PWM output **(Fig 9)**. The inverters of $IC_3$ produce a buffered clock signal **(Fig 10,** trace A). $Q_1$ drives $T_1$. Concurrently, the $R_2/C_3$ differentiator provides a spike (trace B) that sets flip-flop $IC_8$ (trace C). The clock pulse applied to $T_1$'s primary appears at the secondary (pin 8), where it drives the $V_{ISOL}$ supply. The pulse also causes the paralleled, open-drain switches within $IC_5$ to close, which discharges $C_1$. (The $R_1/C_2$ filter prevents oscillation due to regenerative feedback.)

Current from the $Q_2/Q_3$ current source begins to recharge $C_1$ when the pulse ends. The resulting voltage ramp (trace D) drives one input of comparator $IC_5$; the signal related to the thermocouple voltage drives the other input. The comparator switches high when these voltages reach equality, causing a pulse to ripple down the $IC_{7A}$, $IC_{7B}$, $IC_{7C}$ inverter chain (trace E) and drive $T_1$'s secondary. (Three inverters serve to sharpen the signal's low-to-high transitions.) As a result, $T_1$'s primary produces a negative spike (pin 4) that biases $Q_4$, causing its collector to go low (trace G).

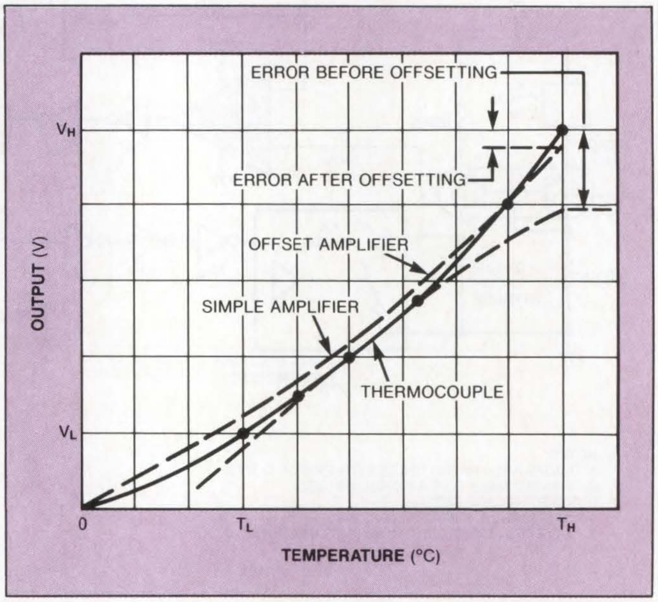
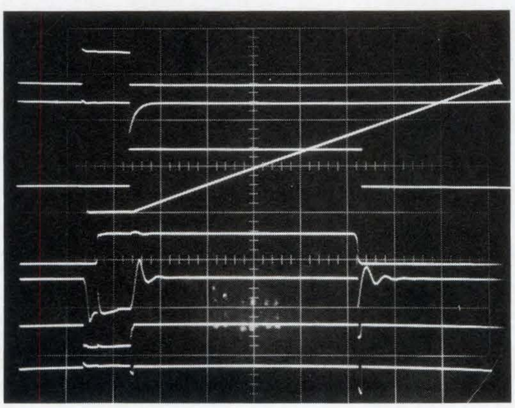



***Fig 11—By introducing an offset voltage and shifting the gain of a simple amplifier,*** *you obtain an output that more closely matches the thermocouple characteristic.*




| TRACE | VERTICAL | HORIZONTAL |
|---|---|---|
| A | 20V/DIV | 50 μSEC/DIV |
| B | 20V/DIV | 50 μSEC/DIV |
| C | 20V/DIV | 50 μSEC/DIV |
| D | 0.05V/DIV | 50 μSEC/DIV |
| E | 20V/DIV | 50 μSEC/DIV |
| F | 20V/DIV | 50 μSEC/DIV |
| G | 50V/DIV | 50 μSEC/DIV |
| H | 20V/DIV | 50 μSEC/DIV |

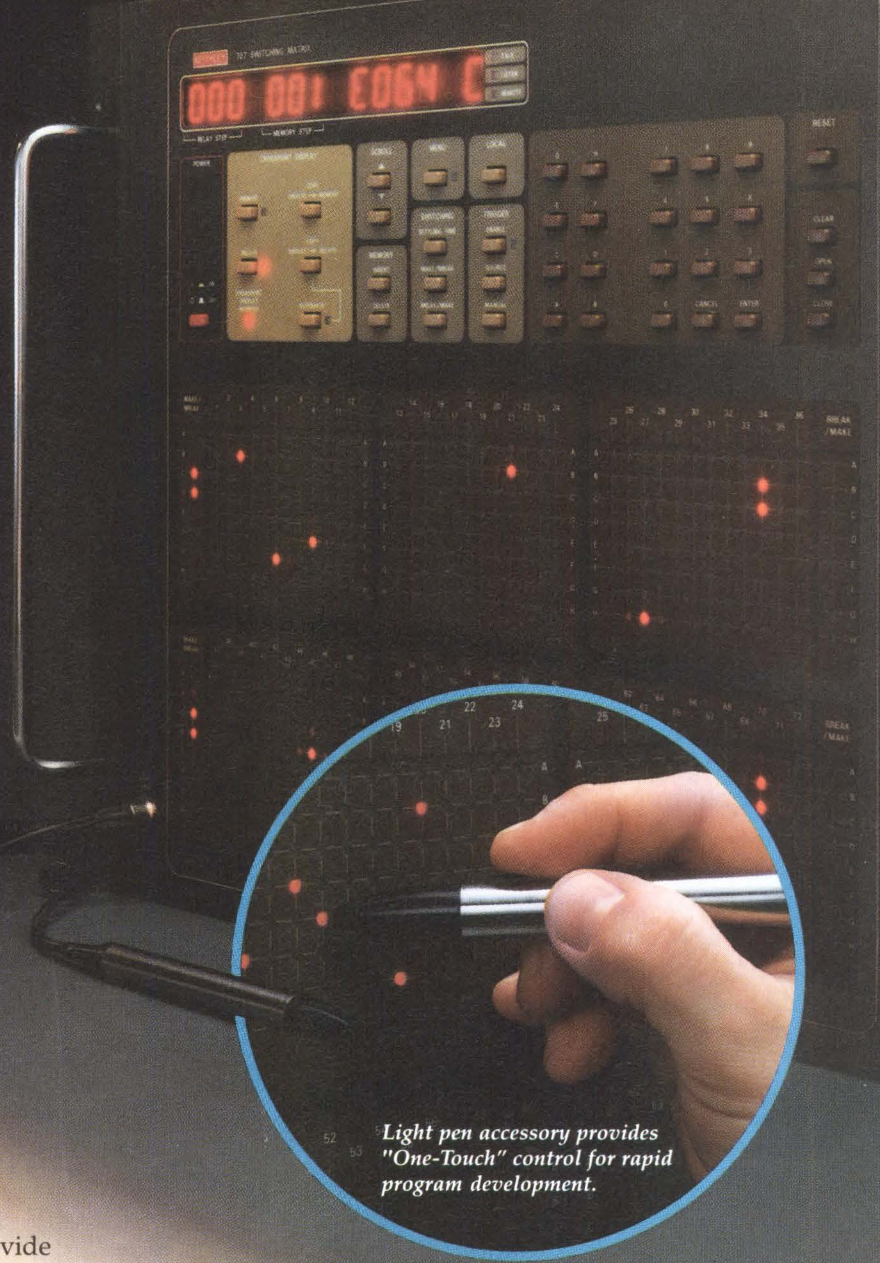
***Fig 10—Of particular interest in these waveforms of the Fig 9 circuit*** *is the pulse-width-modulated output (trace C).*

Transistors $Q_4$ and $Q_5$ form a clocked, synchronous demodulator that pulls $IC_8$'s R (reset) pin low only when the clock signal (the emitter of $Q_1$) is low; this condition occurs during data transfer but not during power transfer. The demodulated output (trace H) contains a single negative spike that resets the flip-flop. Because this spike is synchronous with the high-to-low transition of trace E, $IC_8$'s output-pulse duration (trace C) is proportional to the thermocouple temperature.

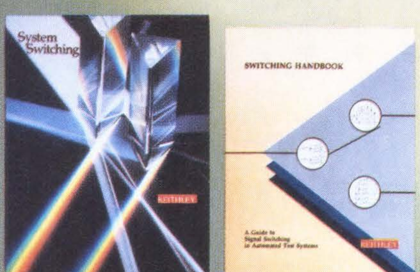
### Four techniques linearize TC signal

Because a thermocouple's response to temperature is nonlinear, its signal-conditioning circuit produces a nonlinear signal. By linearizing this signal, however, you can simplify further signal processing in many applications. Offset addition, breakpoints, analog computation, and digital correction are four techniques useful for this purpose.

Offset-addition schemes rely on biasing the nonlinear "bow" with a constant term. The resulting output voltage is high at the low end and low at the high end, but errors between these two extremes are reduced **(Fig 11)**: The compromise reduces overall error. This approach is suitable for applications in which nonlinearity is either slight over a wide range or great over a narrow range.



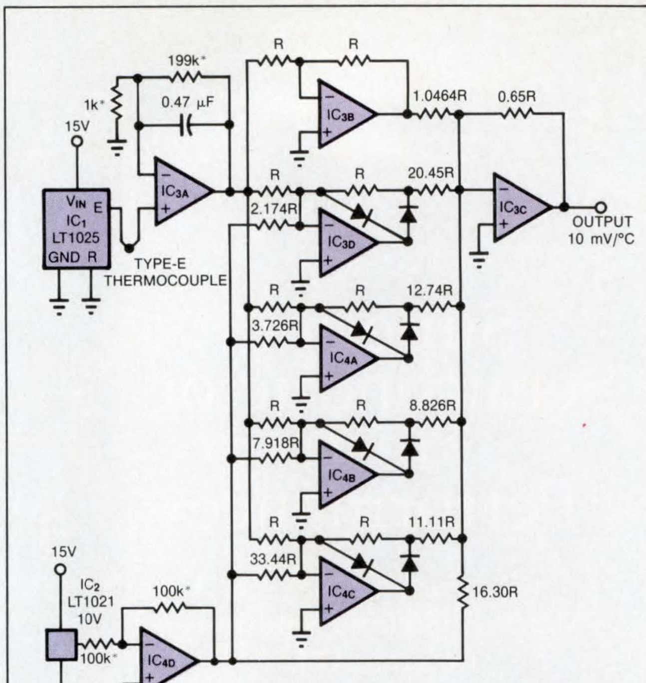




System Switching
SWITCHING HANDBOOK

Type-S thermocouples are relatively nonlinear—they generate 6 μV/°C at 25°C and 11 μV/°C at 1000°C. **Fig 12** shows an offset-addition linearizing circuit for such a thermocouple. This circuit is similar to that of **Fig 2b,** except for the offset term derived from $IC_2$ and applied through $R_4$. $IC_3$ is a chopper-stabilized op amp, useful for minimizing drift. Circuit accuracy is ±3°C for the range of 800 to 1200°C. To calibrate the circuit, set $V_T$=0.0000V and trim $R_5$ so that $V_{OUT}$=1.669V. Then, set $V_T$=9.585V (T=1000°C) and trim $R_2$ so that $V_{OUT}$=9.998V.

The **Fig 13** circuit is an adaptation of a configuration **(Ref 1)** that uses breakpoints to change circuit gain as the input signal varies. This method requires that you scale the input and feedback resistors associated with amplifiers $IC_{4A\text{-}4D}$, $IC_{3B}$, and $IC_{3D}$. Current summation at $IC_{3C}$'s inverting input produces an output voltage that is linear with the thermocouple temperature. Different-value input resistors cause each of the amplifiers, $IC_{3D}$, $IC_{4A}$, $IC_{4B}$, and $IC_{4C}$, to begin contributing current at a




NOTES:
1. OP AMPS ARE 2XLT1014s (QUAD).
2. R=10k; OTHER VALUES ARE TARGET VALUES.
3. DIODES ARE 1N4148s.
4. * DENOTES 0.1% METAL-FILM RESISTORS.

***Fig 13—The thermocouple's output is linearized*** *thanks to the introduction of discrete breakpoints (amplifiers $IC_{3D}$, $IC_{4A}$, $IC_{4B}$, and $IC_{4C}$), which become active at different signal levels.*

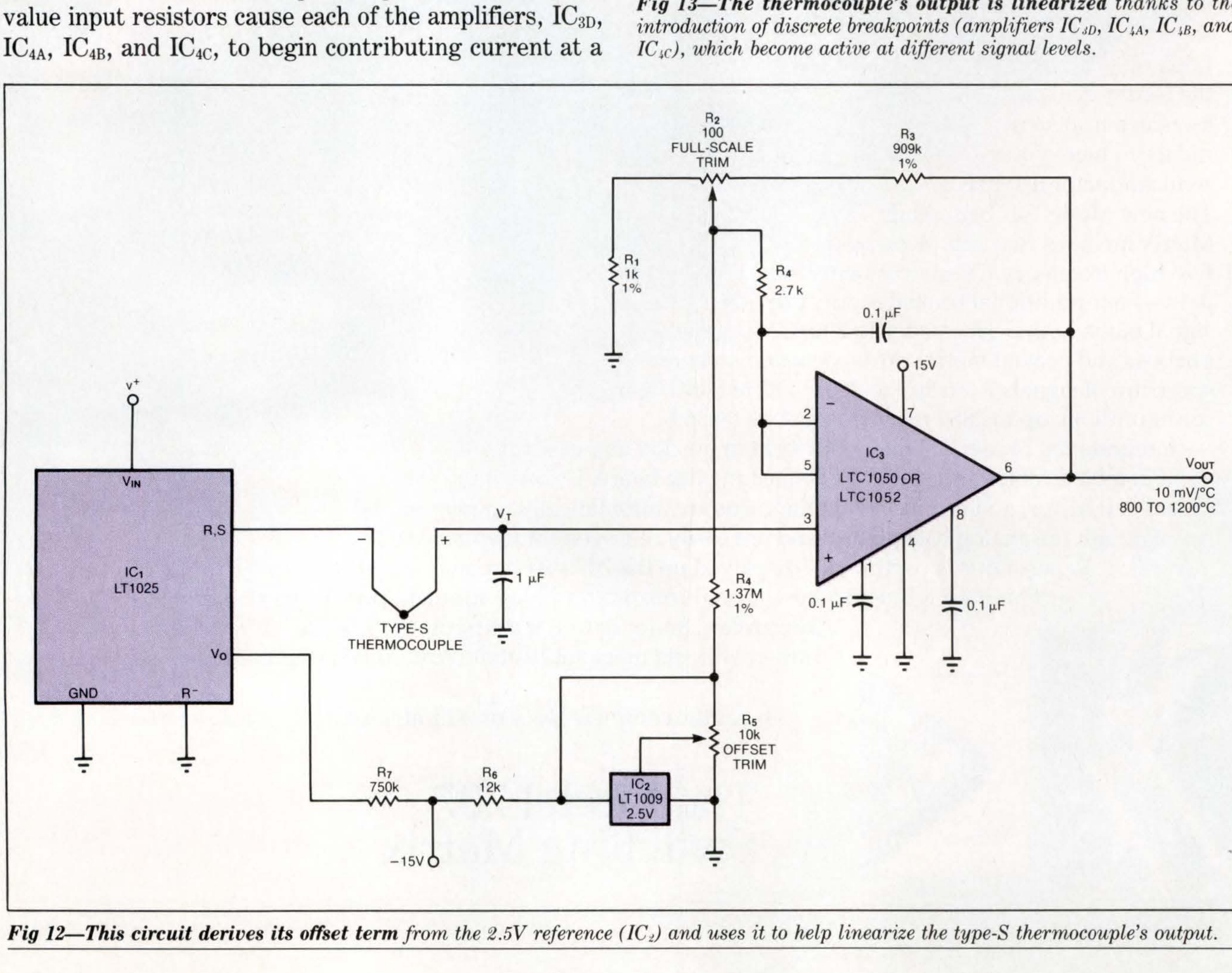



***Fig 12—This circuit derives its offset term*** *from the 2.5V reference ($IC_2$) and uses it to help linearize the type-S thermocouple's output.*

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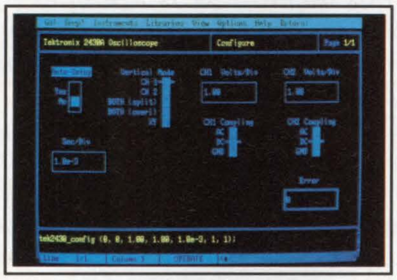

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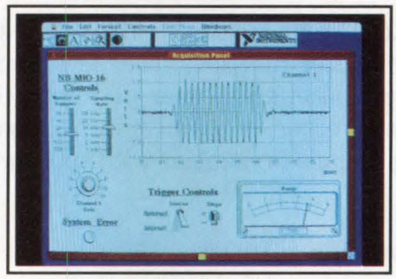

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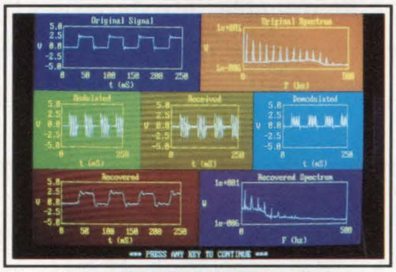

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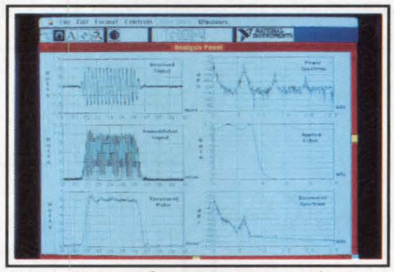

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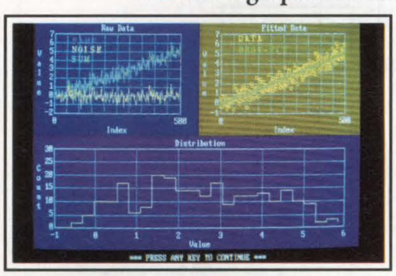

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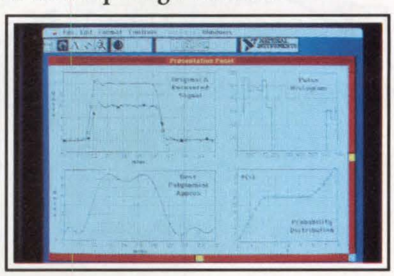

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*Because they eliminate calibration trimming, digital techniques have become a popular method for linearizing thermocouple signals.*

different level of input signal, and the switching diodes produce a piecewise-linear response from each amplifier. For the range of 0 to 650°C, typical circuit accuracy is ±1%.

**Fig 14**'s circuit (**Ref 1**) replaces the breakpoints with continuous analog-computer functions, uses fewer amplifiers and resistors, and offers similar performance. The multifunction converter, $IC_4$, linearizes the response by combining a single breakpoint with appropriate scaling.

**Implement breakpoints in software**

Digital techniques have become popular for linearizing thermocouple signals because they eliminate calibration trimming. For instance, the **Fig 15** circuit—which Guy M Hoover of Linear Technology Corp developed—feeds a digitized thermocouple voltage to a μP that implements a large number of breakpoints in software. To use the circuit, you simply load the software and apply power; the μP then linearizes the digitized thermocouple signal and stores the result. *(Ed Note: The listing that provides all the necessary code for this application is available by sending a self-addressed, stamped envelope ($0.39 postage) to Software Listings Editor, EDN, 275 Washington St, Newton, MA 02158).*

$IC_4$ is a 10-bit A/D converter that gives 0.5°C resolution over the 0 to 500°C range. $IC_2$ amplifies and filters the thermocouple signal; $IC_1$ provides cold-junction compensation; and $IC_3$ provides an accurate reference voltage. (To maintain accuracy, the reference requires a minimum 6.5V supply; the A/D converter monitors this voltage via the $R_1$-$R_2$ divider.) The 1024-step resolution that $IC_4$ provides (24 more than the required 1000) ensures 0.5°C of temperature resolution, even for the nonlinear thermocouple characteristic. Linear interpolation between temperature-data points spaced 30°C apart, for example, introduces less than 0.1°C of error.

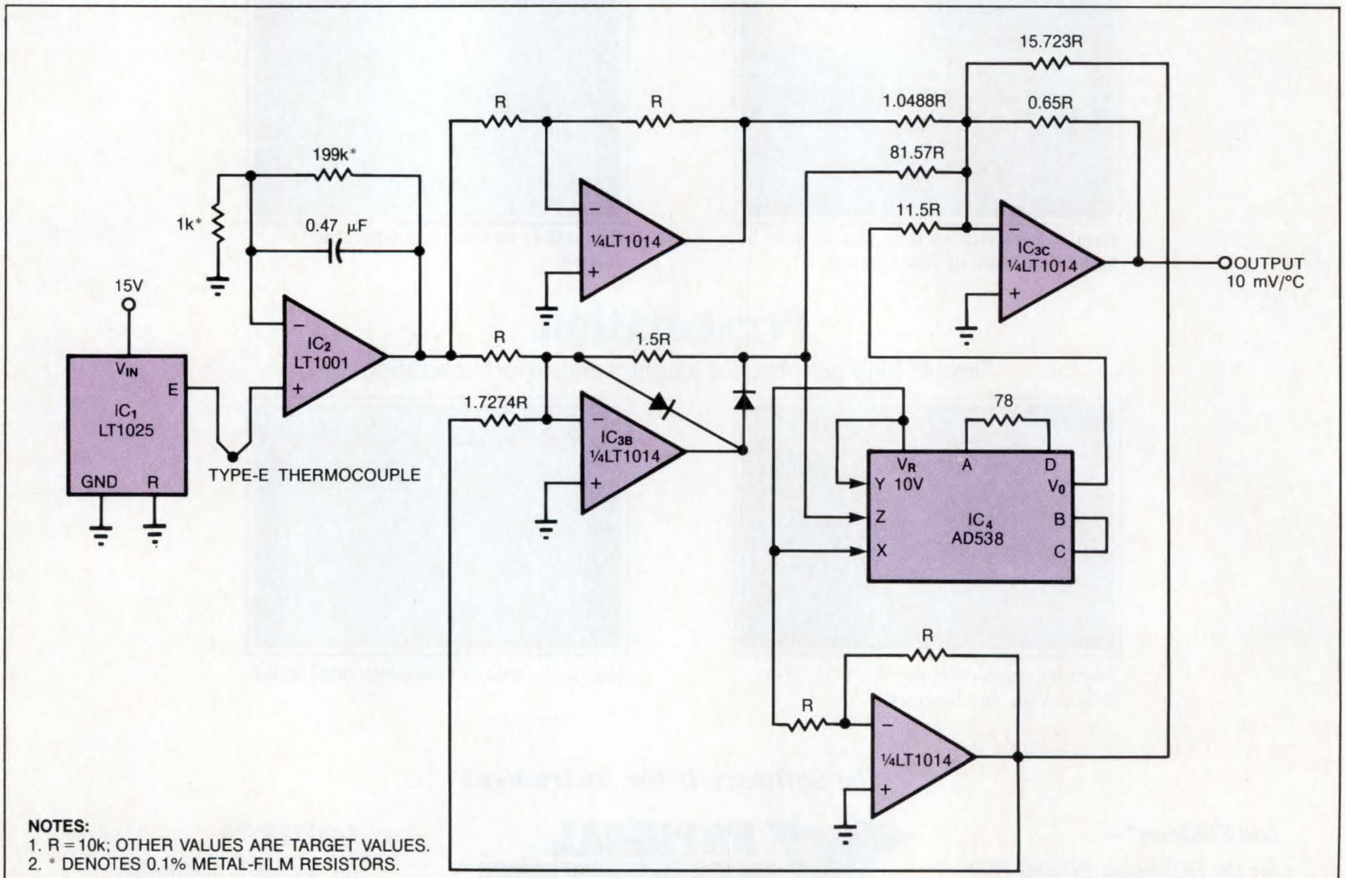
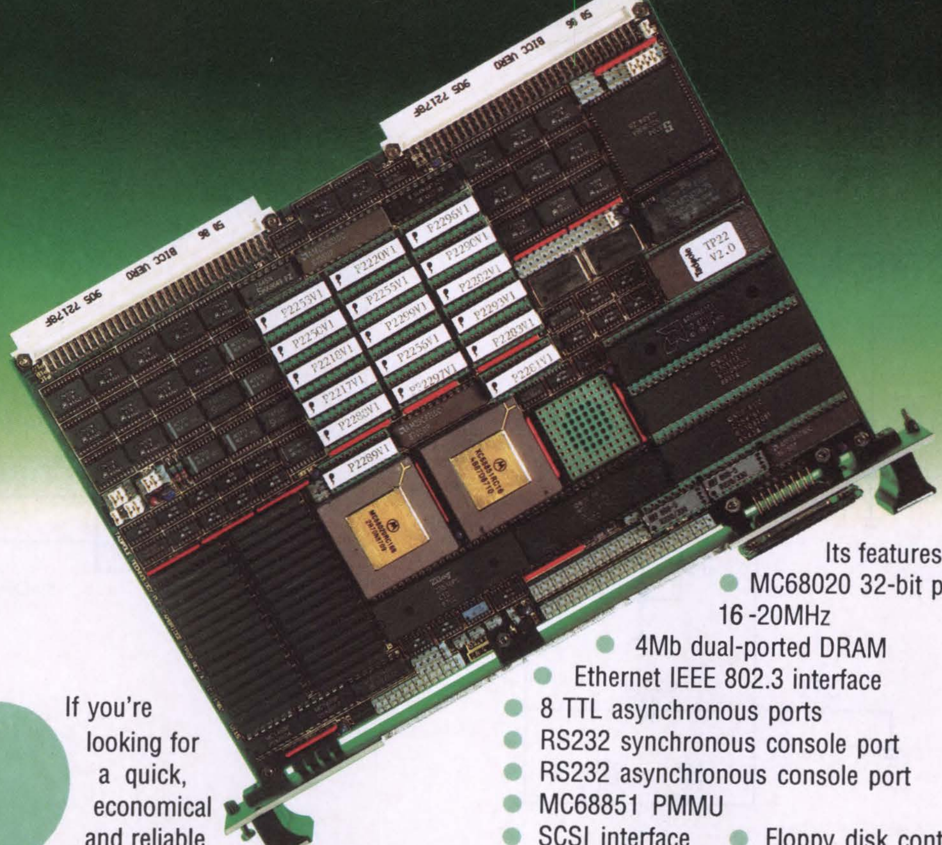



***Fig 14—Offering performance comparable to that of Fig 13,*** *this linearizing circuit uses analog-computer functions in place of breakpoints.*

# One board not five.



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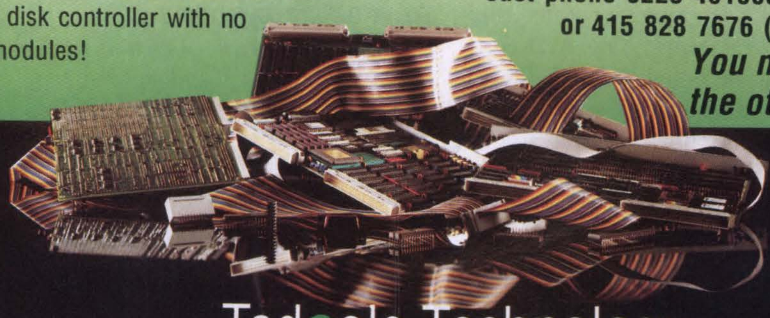

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**CIRCLE NO 108**

*Eddy currents and the effects of laminar flow around a thermocouple can cause remarkably large measurement errors.*

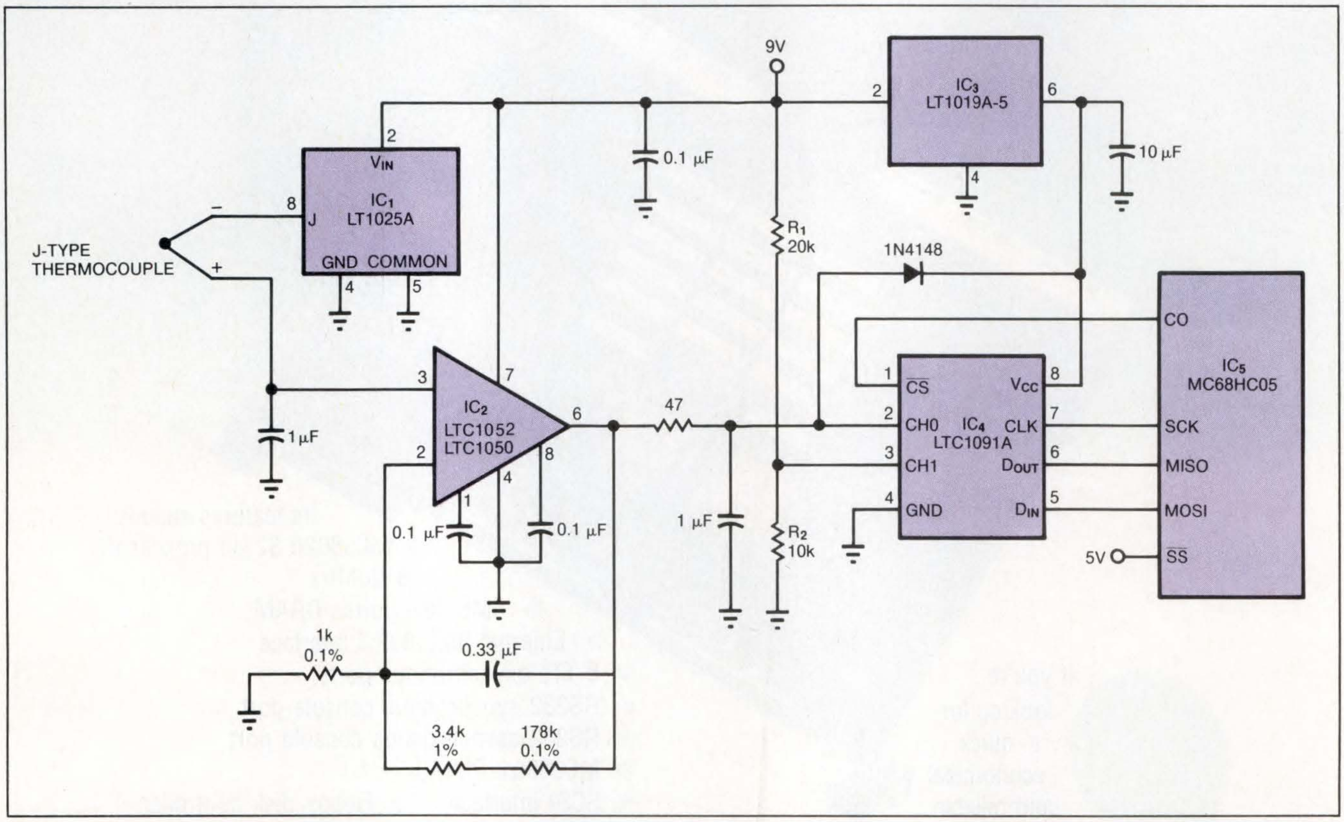


***Fig 15—By introducing a microcomputer ($IC_5$) to implement breakpoints in software,*** *this thermocouple-linearizing circuit eliminates calibration trimming. The software listing is available from EDN; see text for details.*

The cold-junction compensator, $IC_1$, dominates the offset-error budget by contributing errors as high as 0.5°C. ($IC_4$'s 5-µV offset contributes no more than 0.1°C.) The gain error is 0.75°C max, due primarily to the use of gain resistors with 0.1% tolerance values. $IC_3$'s output-voltage tolerance and $IC_4$'s gain error also contribute to the overall gain error; you can reduce this figure by trimming $IC_3$'s gain resistors. The A/D converter maintains a linearity error below 0.15°C. Typically, these errors combine to produce an overall value of 0.5°C or less, exclusive of the thermocouple itself. Additional wire-connection errors of 0.5 to 1.0°C are not uncommon in practice, but with care you can keep these errors below 0.5°C. **EDN**

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3. *Practical temperature measurements*, application note #290, Hewlett-Packard Co, Palo Alto, CA, 1983.

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5. *Manual on the use of thermocouples in temperature measurement*, ASTM special publication #470A, American Society for Testing of Materials, Philadelphia, PA, 1974.

## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.*

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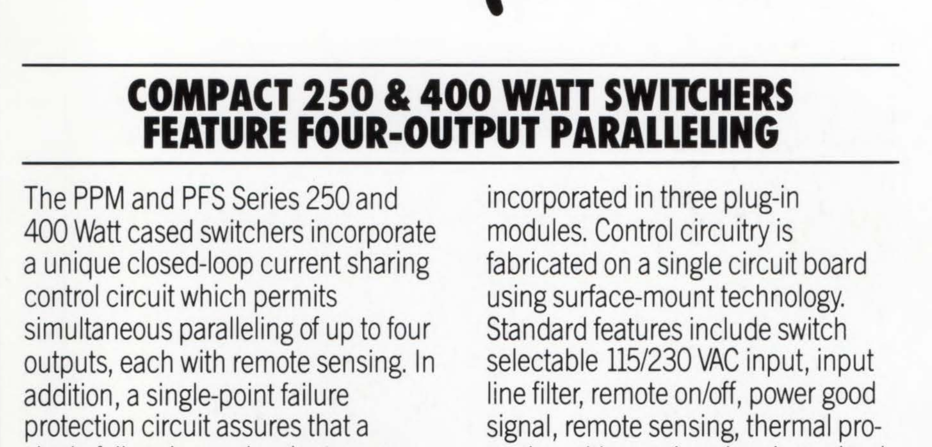

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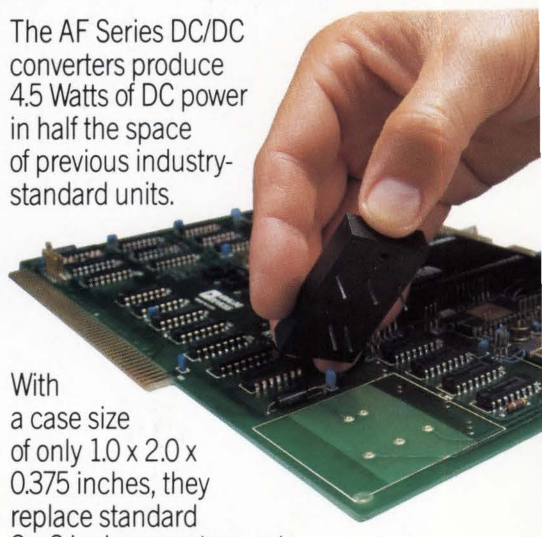


With a case size of only 1.0 x 2.0 x 0.375 inches, they replace standard 2 x 2 inch converters, yet have the same pinouts.

This series is fabricated with surface-mounted components on a miniature thick-film substrate to achieve 6 watts per cubic inch power density and efficiencies up to 66%. Available in single (+5, +12 or +15V) and dual (±12V or ±15V) outputs, the input voltage can be either +5 or +12VDC

Other key specifications include ±1.0% line regulation, 0.5% load regulation, and 40mV p-p ripple and noise. These converters are ideal for board-mounted applications in computers, I/O boards, telecommunications, process control and scientific instruments. The AF Series is on distributor shelves now.

From Computer Products/ Stevens-Arnold

**Circle No. 2**



**Your Partner in Power**

## UNIVERSAL INPUT SWITCHERS OPERATE FROM 85 TO 264 VAC

Operate from any line voltage from 85 to 264 VAC without changing jumper wires or switches. Computer Products/Boschert's new NFS40, NFS50 and NFS110 Universal Input Series open frame switchers eliminate worldwide


line voltage selection problems and offer system design flexibility.

On the low end, the NFS40 series of single and multiple output 40 watt switchers measures a tiny 5" x 3" x 1.2". These switchers provide more than 2.2 watts/cubic inch, and will fit into very small spaces.

The NFS50-7608 50 watt switcher directly replaces the industry standard 6.3" x 3.9" 40 watt unit. No need to mechanically redesign. Just drop it in and enjoy the benefits of universal input, plus 10 additional watts for any system extras.


For small to medium systems, check out the NFS110 series 110 watt switchers. The +12V output will deliver up to 9 amps to start disk drives. The small 7.0" x 4.25" x 1.8" size delivers more than 2.0 watts per cubic inch.

All of these switchers will operate reliably with no load on the output, making them ideal for expansion systems. Also, each output is fully regulated. NFS40 and NFS110 evaluation units are now available. NFS50 is in distribution.

From Computer Products/Boschert
***Circle No. 3***

## POPULAR DC/DC CONVERTERS HAVE NEW LOW PRICES

Design in high performance and reliable operation at new low prices. The ES, EA and H series have filled a lot of PC boards to date but never so economically. Prices have been reduced by 10% for the ES series and 15% for the H and EA series. Also, the H and EA series are available in new 1.0 x 2.0 x 0.38 inch non-conductive packages. Check the table below and send for the latest data on our top performers. Or better yet, call your distributor for these low cost solutions.

| Series | Output Power | Output Type | Input Voltage | Output |
|---|---|---|---|---|
| H | 1 Watt | Single | 5, 24, 48V | ±5V @ 200mA |
| EA | 1.8 Watts | Dual | 5V | ±12 or ±15V @ 60mA |
| ES | 15 Watts | Triple | 12, 24, 48V | +5V & ±12V<br>+5V & ±15V<br>or<br>±5V & +12V |

From Computer Products/Stevens-Arnold
***Circle No. 4***

## TAKING THE RISK OUT OF CUSTOM OPEN FRAME SWITCHERS

Computer Products/Boschert can take the risk out of custom switcher development. You get a predictable, highly reliable switcher, based on our well-known standard circuits.

Here's why:

**Field-Proven Building Blocks**. The quickest, least expensive way to build a custom switcher is using existing circuits. Computer Products/Boschert has hundreds of building blocks, field proven over our 15 year history. We understand their use and limitations. Your custom design is predictable, economical and virtually risk-free.

**Appropriate Topology**. Using the wrong topology is either costly or unreliable. Since we understand and build virtually every type of switcher, there is no need to squeeze your custom needs into our favorite topology. You get the correct topology for your power requirement.

**Experience**. Your supply is built by a company exclusively dedicated to switchers for 15 years. Our ability to integrate electrical, mechanical and thermal designs is exceptional. Our new medium power designs deliver more than 2 watts/cubic inch. The result is a highly compact switcher that meets or exceeds your system requirements.

**Safety Approval**. UL and CSA usually take no more than eight weeks. Full VDE certification usually takes only 12 to 16 weeks after your final prototype approval. TUV approval is also available.

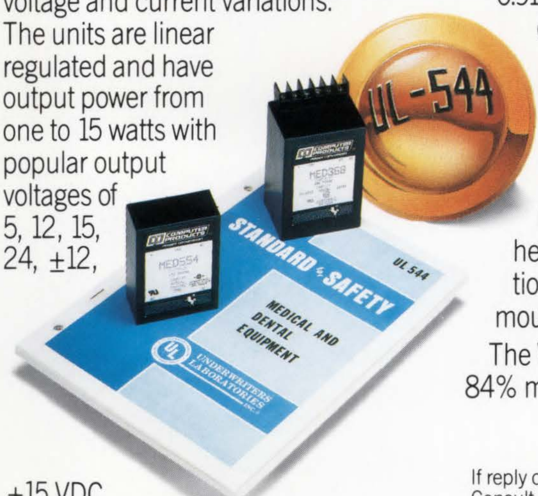
**Manufacturability**. Every supply we make is designed with manufacturability in mind. We use a common parts base, with well characterized components that meet our conservative stress derating guidelines. Check for further information on custom switchers.

From Computer Products/Boschert
***Circle No. 5***

## LINEAR POWER MODULES MEET UL544 MEDICAL REQUIREMENTS

For UL544 approval you can rely on Computer Products/Power Products new MED 300/500 Series of AC/DC encapsulated power modules. They meet or exceed the stringent UL544 requirements for medical equipment. These supplies are recommended for use in non-patient contact medical, dental and laboratory applications where high isolation and low leakage are critical.

The MED 300/500 series is provided in single, dual and triple output models offering 63 different output voltage and current variations. The units are linear regulated and have output power from one to 15 watts with popular output voltages of 5, 12, 15, 24, ±12,




±15 VDC, plus others available. Standard protection features such as overtemperature, overload and short circuit protection are included.

The power modules incorporate a split-bobbin wound transformer which provides high isolation between primary and secondary with low coupling capacitance. This results in 2500 VAC isolation voltage and less than 10uA leakage current.

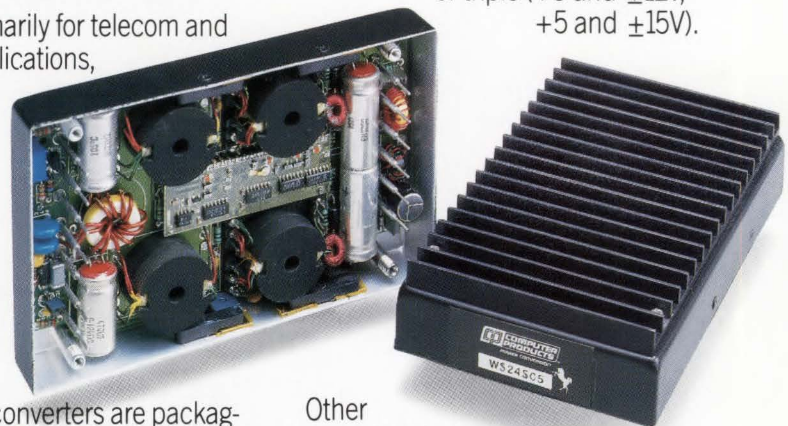
The units are available in either printed circuit mountable or chassis mountable packages. In addition to UL544 approval the series is CSA certified.

From Computer Products/ Power Products ***Circle No. 6***

## 100 WATT DC/DC CONVERTERS HAVE LOW PROFILES, HIGH EFFICIENCIES

Designed primarily for telecom and computer applications, the new WS Series from Computer Products/ Stevens-Arnold offers 100 watts with single, dual, and triple outputs. The converters are packaged in a low profile case (3.5 x 5.5 x 0.91 inches) producing a power density of 5.7 watts per cubic inch. Available in chassis mount with screw terminations or printed circuit board mounting. The PCB mount version is supplied with a heat sink (adds 0.35 inches to height) which allow for conventional cooling with *no* special mounting required.

The WS Series has an efficiency of 84% minimum and a 2:1 input range of either 18 to 36 VDC or 36 to 72 VDC Output ranges supplied are single (+5, +12 or +15V), dual (+5 and +12V), or triple (+5 and ±12V, +5 and ±15V).




Other important features include 500 VDC isolation, input surge protection, reverse voltage protection and remote on/off control with idle currents down to 10mA.

Key Specifications:

- Line Regulation ...... ±0.5% max.
- Load Regulation .. 2.0% (to no load)
- Ripple and Noise .. 100mV p-p max.

This series is available through distribution.

From Computer Products/Stevens-Arnold ***Circle No. 7***

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Designer's Guide to noise analysis—Part 2

# Spreadsheet helps you evaluate system noise

*An ordinary electronic spreadsheet can help you evaluate and correct noise problems in an electronic system. Part 1 of this 2-part article described techniques for analyzing the noise contributions of a system's individual elements. This article, part 2, shows how you can use a spreadsheet program to evaluate the system's overall performance as you modify the individual elements.*

Peter Fazekas, *ILC Data Device Corp*

To optimize the noise performance of an electronic system, you need to determine the noise contributions of each of the elements of the system and then replace or modify the sections you identify as troublesome. An ordinary electronic spreadsheet can be an invaluable aid in analyzing and modifying a system's noise performance.

Your first task in setting up a system for noise analysis is to draw a block diagram of the system. This diagram should include all of the major functional blocks (such as transducers, amplifiers, and filters), and any individual components that might contribute to the overall noise level of the system. You then assign a table of attributes to each functional block and individual element. At the very least, the table should contain the following information:

- The equivalent input noise voltage and/or noise current of the block
- The input and output impedance of the block, if applicable
- The power-supply rejection ratio (PSRR) of the block, if applicable
- For filter blocks, the noise equivalent bandwidth (NEBW) of the filter's corner frequencies (upper and lower).

With the above information, you can calculate the effective rms noise (at the system's output) that's caused by each source. First, you determine the effective NEBW filter corner frequency from the input of each block to the system's output. Next, you find the equivalent output-noise spectral density caused by each source (to calculate it, you multiply the input-noise spectral density by the signal gain from the source to the output). Finally, you calculate the total rms noise level by multiplying the output-noise spectral density by the square root of the effective NEBW that you've calculated for each block. Later, you'll enter all of the calculated values in the above sections in your electronic spreadsheet.

**Fig 1** is a block diagram of a typical system (a data-acquisition system, in this case) that's suitable for noise analysis with a spreadsheet. Before you can make the optimum tradeoffs between noise and other parameters, you must thoroughly understand your circuit's functions. The A/D converter you choose should be

*To analyze noise in a system, you first set up a block diagram that includes all of the functional elements that contribute to the total noise level.*

transparent to the system—in other words, the speed and resolution of the converter should be high enough to reproduce the signals accurately. The sample system in **Fig 1** uses the ADC-00300 converter (from ILC Data Device Corp); the part has a conversion-rate capability of 2 MHz and a resolution of 12 bits, which more than meet the system's requirements.

The signal amplifier you choose for such a circuit must be able to amplify the signal without adding any observable noise of its own, and without causing distortion because of its limited bandwidth.

The bandpass filter is the system's frequency-shaping network; it determines the dominant corner frequencies of the noise bandwidth. The preamplifier is normally the major noise-determining component in the system. Ideally, the preamplifier noise would be lower than that of the transducer; if you can't make it so, you should do your best to reduce the preamplifier's noise contribution by optimizing its gain and its signal-to-noise ratio.

### Using the spreadsheet in noise calculations

A spreadsheet is helpful in calculating system noise, because when you change any of the parameters of the individual circuit elements, the spreadsheet can immediately show you the effects of those changes on the overall system noise. To use a spreadsheet most efficiently for noise analysis, you should begin by entering the characteristic values of the system as variables, and then direct all subsequent references to these values back to the appropriate data cell. Thus, you need to change a value only once instead of each time you use it in the calculation.

**Tables 1** through **6** represent an electronic spreadsheet. **Table 1** tabulates the data describing the characteristics of the individual sections of the system. **Table 2** is a sytematic evaluation of the NEBW of each section of the circuit. You calculate the NEBW in two parts: the low-frequency corner ($f_L$) and the high-frequency corner ($f_H$). It's convenient to start at the section closest to the output (the signal amplifier in this case), and work toward the input (the transducer).

If two first-order filters have −3-dB corner frequencies of $f_a$ and $f_b$, then the NEBW corner frequency is $f_{a'}=\Pi/2f_a$ if the filter is a lowpass type, and $f_{a'}=2/\Pi f_a$ if the filter is a highpass type. Also, the equivalent NEBW corner frequency of the two combined filters is $f_L=f_D/(1-(1/(1+R)))$ for a highpass filter, and $f_H=f_D\cdot(1-(1/(1+R)))$ for a lowpass filter. In these equations, R is the ratio of the larger corner frequency

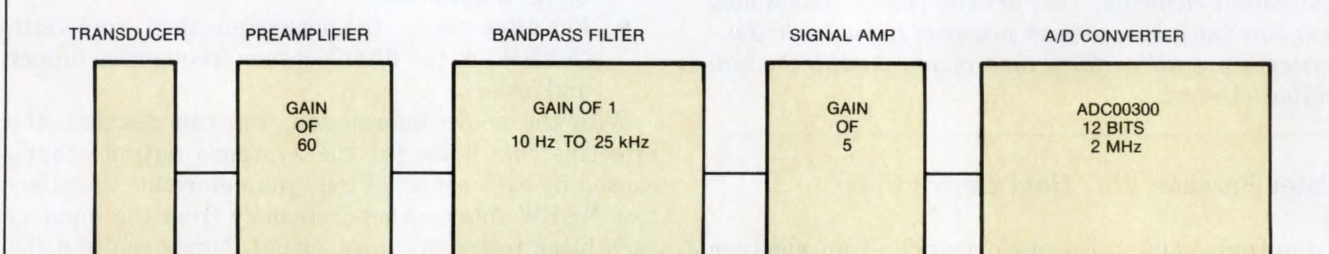


***Fig 1—Systematic noise analysis is helpful** in designs such as this typical data-acquisition system. By using an electronic spreadsheet to evaluate the effect of design changes on the system's noise characteristics, you can easily modify the system to achieve optimum noise performance.*

divided by the smaller one, and $f_D$ is the dominant NEBW corner frequency (the one closest to the center of the signal passband). The individual elements of **Table 2** are defined as follows:

- *Self corner frequency* is the NEBW of the particular stage you're evaluating
- *NEBW to output* is the combined NEBW of all stages following the stage under evaluation
- *Dominant pole* is the value of $f_D$
- *Correction factor* is the value $1/(1-(1/(1+R)))$ for the lowpass filter and $1-(1/(1+R))$ for the highpass filter
- *Combined corner* is the value of $f_L$ and $f_H$
- *Total NEBW* is $f_H-f_L$.

**Table 3** calculates the amount of noise contributed by the individual sources. The parameters are defined as follows:

- *Noise input* is the self-noise at the input to the stage under evaluation. This value comes directly from **Table 1.**
- *Total NEBW* is the combined NEBW of the section under consideration and all subsequent sections in the system, as evaluated in **Table 1.**
- *Noise gain* is the gain of all the stages between the noise source and the output of the system.
- *RMS noise* is noise input×noise gain×$(\text{NEBW})^{0.5}$.

**Table 4** compares the total noise and signal levels of the system. Most of the elements in this table are

## TABLE 1—SPREADSHEET VALUES

| | | | | |
|---|---|---|---|---|
| **TRANSDUCER** | | | | |
| INPUT NOISE | $1.28^{-8}$ | V/RT Hz | | |
| OUTPUT IMPEDANCE | 10000 | OHMS | | |
| CORNER FREQ | 45000 | −3 dB HI | 70685.83 | NEBW HI |
| | 3 | −3 dB LO | 1.91 | NEBW LO |
| MAX SIGNAL | $5.00^{-3}$ | V | | |
| **PREAMPLIFIER** | | | | |
| INPUT NOISE | $1.50^{-8}$ | V/RT Hz | | |
| | $9.00^{-12}$ | A/RT Hz | | |
| PSRR | 316.23 | RATIO | 50 | dB |
| CORNER FREQ | 50 | −3 dB HI | 78.54 | NEBW HI |
| STAGE GAIN | 60 | RATIO | 35.56 | dB |
| CORNER FREQ | 10000000 | −3 dB HI | $1.57^{7}$ | NEBW HI |
| | $1.00^{-3}$ | −3 dB LO | $6.37^{-4}$ | NEBW LO |
| **BANDPASS FILTER** | | | | |
| INPUT NOISE | $5.00^{-8}$ | V/RT Hz | | |
| PSRR | 1778.28 | RATIO | 65 | dB |
| CORNER FREQ | 200 | −3 dB HI | 314.16 | NEBW HI |
| STAGE GAIN | 1 | RATIO | 0 | dB |
| CORNER FREQ | 25000 | −3 dB HI | 39269.91 | NEBW HI |
| | 10 | −3 dB LO | 6.37 | NEBW LO |
| **SIGNAL AMPLIFIER** | | | | |
| INPUT NOISE | $5.00^{-8}$ | V/RT Hz | | |
| PSRR | 1000 | RATIO | 60 | dB |
| CORNER FREQ | 500 | −3 dB HI | 785.40 | NEBW HI |
| STAGE GAIN | 5 | RATIO | 13.98 | dB |
| CORNER FREQ | 100000 | −3 dB HI | 157079.63 | NEBW HI |
| | 2 | −3 dB LO | 1.27 | NEBW LO |
| **POWER SUPPLY** | | | | |
| INPUT NOISE | $1.00^{-5}$ | V/RT Hz | | |
| CORNER FREQ | 1591.55 | −3 dB HI | 2500 | NEBW HI |
| | $1.00^{-3}$ | −3 dB LO | $6.37^{-4}$ | NEBW LO |
| **A/D CONVERTER** | | | | |
| MAX SIGNAL INPUT | 1.50 | V | | |
| RESOLUTION | 12 | BITS | | |
| LEVEL OF 1 LSB | $3.66^{-4}$ | V | | |
| SAMPLE RATE | 60000 | PER SEC | | |
| QUANTIZATION NOISE | $1.06^{-4}$ | V | | |
| CORNER FREQ | 30000 | −3 dB HI | 47123.89 | NEBW HI |

**NOTE:**
RT Hz=$\sqrt{\text{Hz}}$

*A spreadsheet is a useful tool for analyzing the effects of changes in the noise contribution of individual elements on the performance of the whole system.*

self-explanatory. The measures of system performance are the S/N ratio and the noise figure. The S/N ratio is the peak signal divided by the total noise. The noise figure is the S/N ratio at the output divided by the S/N ratio at the input (it's also defined as the total noise divided by the source noise).

In an optimum design, the noise generated by the input device is the limiting factor in the system's S/N ratio—all other sources contribute lesser amounts of noise, so they don't degrade the overall noise performance. The design shown in **Fig 1** is not an optimum one. In it, the preamplifier's noise voltage and noise current, as well as the power-supply noise through the preamplifier, are the same as or higher than the self-noise of the transducer. As a result of these noise contributions, the S/N ratio of the system is far from optimum.

The input noise voltage of the preamplifier is a

## TABLE 2—NEBW CALCULATIONS

| | | | | |
|---|---|---|---|---|
| **SIGNAL AMP** | | | | |
| SELF CORNER FREQ | 1.27 | NEBW LO | 157079.63 | NEBW HI |
| NEBW TO OUTPUT | $1.00^{-5}$ | NEBW LO | $1.00^{10}$ | NEBW HI |
| DOMINANT POLE | 1.27 | LO FREQ | 157079.63 | HI FREQ |
| CORRECTION FACTOR | 1.00 | LO FREQ | 1.00 | HI FREQ |
| COMBINED CORNER | 1.27 | LO FREQ | 157077.17 | HI FREQ |
| TOTAL NEBW | 157075.89 | Hz | | |
| **BANDPASS FILTER** | | | | |
| SELF CORNER FREQ | 6.37 | NEBW LO | 39269.91 | NEBW HI |
| NEBW TO OUTPUT | 1.27 | NEBW LO | 157077.17 | NEBW HI |
| DOMINANT POLE | 6.37 | LO FREQ | 39269.91 | HI FREQ |
| CORRECTION FACTOR | 1.20 | LO FREQ | 0.80 | HI FREQ |
| COMBINED CORNER | 7.64 | LO FREQ | 31415.83 | HI FREQ |
| TOTAL NEBW | 31408.19 | Hz | | |
| **PREAMPLIFIER** | | | | |
| SELF CORNER FREQ | $6.37^{-4}$ | NEBW LO | $1.57^{7}$ | NEBW HI |
| NEBW TO OUTPUT | 7.64 | NEBW LO | 31415.83 | NEBW HI |
| DOMINANT POLE | 7.64 | LO FREQ | 31415.83 | HI FREQ |
| CORRECTION FACTOR | 1.00 | LO FREQ | 1.00 | HI FREQ |
| COMBINED CORNER | 7.64 | LO FREQ | 31353.12 | HI FREQ |
| TOTAL NEBW | 31345.48 | Hz | | |
| **TRANSDUCER** | | | | |
| SELF CORNER FREQ | 1.91 | NEBW LO | 70685.83 | NEBW HI |
| NEBW TO OUTPUT | 7.64 | NEBW LO | 31353.12 | NEBW HI |
| DOMINANT POLE | 7.64 | LO FREQ | 31353.12 | HI FREQ |
| CORRECTION FACTOR | 1.25 | LO FREQ | 0.69 | HI FREQ |
| COMBINED CORNER | 9.55 | LO FREQ | 21719.37 | HI FREQ |
| TOTAL NEBW | 21709.82 | Hz | | |
| **POWER SUPPLY—SIGNAL AMP** | | | | |
| SELF CORNER FREQ | $6.37^{-4}$ | NEBW LO | 2500 | NEBW HI |
| NEBW TO OUTPUT | 1.27 | NEBW LO | 157077.17 | NEBW HI |
| DOMINANT POLE | 1.27 | LO FREQ | 2500 | HI FREQ |
| CORRECTION FACTOR | 1.00 | LO FREQ | 0.98 | HI FREQ |
| COMBINED CORNER | 1.27 | LO FREQ | 2460.83 | HI FREQ |
| TOTAL NEBW | 2459.56 | Hz | | |
| **POWER SUPPLY—BANDPASS FILTER** | | | | |
| SELF CORNER FREQ | $6.37^{-4}$ | NEBW LO | 2500 | NEBW HI |
| NEBW TO OUTPUT | 7.64 | NEBW LO | 31415.83 | NEBW HI |
| DOMINANT POLE | 7.64 | LO FREQ | 2500 | HI FREQ |
| CORRECTION FACTOR | 1.00 | LO FREQ | 0.93 | HI FREQ |
| COMBINED CORNER | 7.64 | LO FREQ | 2315.72 | HI FREQ |
| TOTAL NEBW | 2308.08 | Hz | | |
| **POWER SUPPLY—PREAMP** | | | | |
| SELF CORNER FREQ | $6.37^{-4}$ | NEBW LO | 2500 | NEBW HI |
| NEBW TO OUTPUT | 7.64 | NEBW LO | 31353.12 | NEBW HI |
| DOMINANT POLE | 7.64 | LO FREQ | 2500 | HI FREQ |
| CORRECTION FACTOR | 1.00 | LO FREQ | 0.93 | HI FREQ |
| COMBINED CORNER | 7.64 | LO FREQ | 2315.38 | HI FREQ |
| TOTAL NEBW | 2307.74 | Hz | | |

## TABLE 3—CONTRIBUTION OF INDIVIDUAL SOURCES

| SECTION | INPUT NOISE (V/RT Hz) | NEBW (Hz) | NOISE GAIN | RMS NOISE (V) |
|---|---|---|---|---|
| TRANSDUCER | $1.28^{-8}$ | 21709.82 | 300 | $5.67^{-4}$ |
| PREAMPLIFIER | | | | |
| VOLTAGE | $1.50^{-8}$ | 31345.48 | 300 | $7.97^{-4}$ |
| CURRENT | $9.00^{-12}$ | 31345.48 | 3000000 | $4.78^{-3}$ |
| BANDPASS FILTER | $5.00^{-8}$ | 31408.19 | 5 | $4.43^{-5}$ |
| SIGNAL AMPLIFIER | $5.00^{-8}$ | 157075.89 | 5 | $9.91^{-5}$ |
| POWER SUPPLY | | | | |
| PREAMPLIFIER | $1.00^{-5}$ | 2307.74 | $9.49^{-1}$ | $4.56^{-4}$ |
| BANDPASS FILTER | $1.00^{-5}$ | 2308.08 | $2.81^{-3}$ | $1.35^{-6}$ |
| SIGNAL AMPLIFIER | $1.00^{-5}$ | 2459.56 | $5.00^{-3}$ | $2.48^{-6}$ |
| A/D CONVERTER | | | | $1.06^{-4}$ |

## TABLE 4—SYSTEM PERFORMANCE EVALUATION

| | |
|---|---|
| NOISE FROM TRANSDUCER (V) | $5.67^{-4}$ |
| NOISE FROM ELECTRONICS (V) | $4.87^{-3}$ |
| A/D QUANTIZATION NOISE (V) | $1.06^{-4}$ |
| TOTAL NOISE | $4.90^{-3}$ |
| 1 LSB OF A/D CONVERTER (V) | $3.66^{-4}$ |
| PEAK SIGNAL LEVEL (V) | 1.50 |
| SIGNAL-TO-NOISE RATIO (dB) | 49.71 |
| NOISE FIGURE (dB) | 18.74 |
| RATIO OF NOISE TO 1 LSB | 13.39 |

characteristic of the particular amplifier you select; you can improve the performance of the preamplifier only by selecting a device with lower input noise. For example, you can choose state-of-the-art op amps whose input noise voltage ($3^{-9}$V/$\sqrt{\text{Hz}}$) is 20% that of the device shown in **Fig 1.**

You can reduce the input noise current in two ways. First, you can replace the preamplifier with a device having superior characteristics. That way, you can easily improve the performance ($9^{-12}$A/$\sqrt{\text{Hz}}$) of the selected device by two orders of magnitude, but you may incur a large cost penalty. Second, you can select a transducer with a lower output impedance. The self-noise of the transducer will drop as a function of the square root of the resistance, and the noise-current gain will drop linearly with resistance, thus providing a net increase in the S/N ratio. You can also decrease the resistance by placing a transformer in front of the preamplifier.

The easiest way to reduce power-supply noise is to place a filter at the supply's output. If you use a filter with an $f_H$ of 10 Hz, for example, the overall noise bandwidth drops to 10 Hz−7.64 Hz, or 2.36 Hz. This amount of filtering may be neither necessary nor practical, however. If the system's space allocations limit the

## TABLE 5—CONTRIBUTION OF INDIVIDUAL SOURCES
(REVISED DATA)

| SECTION | INPUT NOISE (V/RT Hz) | NEBW (Hz) | NOISE GAIN | RMS NOISE (V) |
|---|---|---|---|---|
| TRANSDUCER | $1.28^{-8}$ | 21709.82 | 300 | $5.67^{-4}$ |
| PREAMPLIFIER | | | | |
| VOLTAGE | $3.00^{-9}$ | 31345.48 | 300 | $1.59^{-4}$ |
| CURRENT | $9.00^{-14}$ | 31345.48 | 3000000 | $4.78^{-5}$ |
| BANDPASS FILTER | $5.00^{-8}$ | 31408.19 | 5 | $4.43^{-5}$ |
| SIGNAL AMPLIFIER | $5.00^{-8}$ | 157075.89 | 5 | $9.91^{-5}$ |
| POWER SUPPLY | | | | |
| PREAMPLIFIER | $1.00^{-5}$ | 92.04 | $9.49^{-1}$ | $9.10^{-5}$ |
| BANDPASS FILTER | $1.00^{-5}$ | 92.04 | $2.81^{-3}$ | $2.70^{-7}$ |
| SIGNAL AMPLIFIER | $1.00^{-5}$ | 98.66 | $5.00^{-3}$ | $4.97^{-7}$ |
| A/D CONVERTER | | | | $1.06^{-4}$ |

*In an ideal system, the preamplifier (first stage) would largely determine the overall system noise.*

size of the filter, as they would in a hybrid microcircuit, you can gradually adjust the filter's corner frequency until it's just low enough to do the job. This adjustment is easy to do on a spreadsheet; you reduce the corner frequency (while watching the S/N ratio) until you note no further improvement.

**Tables** 5 and 6 show the revised data that results when you add the characteristics of an improved op amp and a band-limited power supply—preamplifier noise voltage=3 nV/$\sqrt{\text{Hz}}$, preamplifier noise current=$9^{-14}$ A/$\sqrt{\text{Hz}}$, and power-supply upper NEBW corner frequency=100 Hz—to **Table** 1. **Tables** 5 and 6 show the revised spreadsheet results for **Tables** 3 and 4.

### Evaluating the revisions

As evidenced by the magnitude of the individual sources, the major contributor to the overall system noise, both before and after modification, is the transducer. The 0.73-dB noise figure indicates that the electronics increases the noise level of the transducer by only 0.73 dB (8.8%). In most cases, you don't need to attempt further improvement, and you can consider the design completed.

**TABLE 6—SYSTEM PERFORMANCE EVALUATION (REVISED DATA)**

| | |
|---|---|
| NOISE FROM TRANSDUCER (V) | $5.67^{-4}$ |
| NOISE FROM ELECTRONICS (V) | $2.18^{-4}$ |
| A/D QUANTIZATION NOISE (V) | $1.06^{-4}$ |
| TOTAL NOISE | $6.17^{-4}$ |
| 1 LSB OF A/D CONVERTER (V) | $3.66^{-4}$ |
| PEAK SIGNAL LEVEL (V) | 1.50 |
| SIGNAL-TO-NOISE RATIO (dB) | 67.72 |
| NOISE FIGURE (dB) | 0.73 |
| RATIO OF NOISE TO 1 LSB | 1.68 |

The techniques described here provide a systematic method for comprehensive noise analysis. You can perform this analysis with relative ease and freedom from error-prone manual calculations. Keep in mind, however, that these methods are general approximations of the required solutions. They will suffice for most systems because noise, by nature, is a random variable whose amplitude is only an approximation. If you need a more exact value for the noise amplitude, you can use the integrals described in part 1 of this series ("A systematic approach facilitates noise analysis," EDN, May 12, 1988, pg 153) to obtain a more accurate result.

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## References

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## Author's biography

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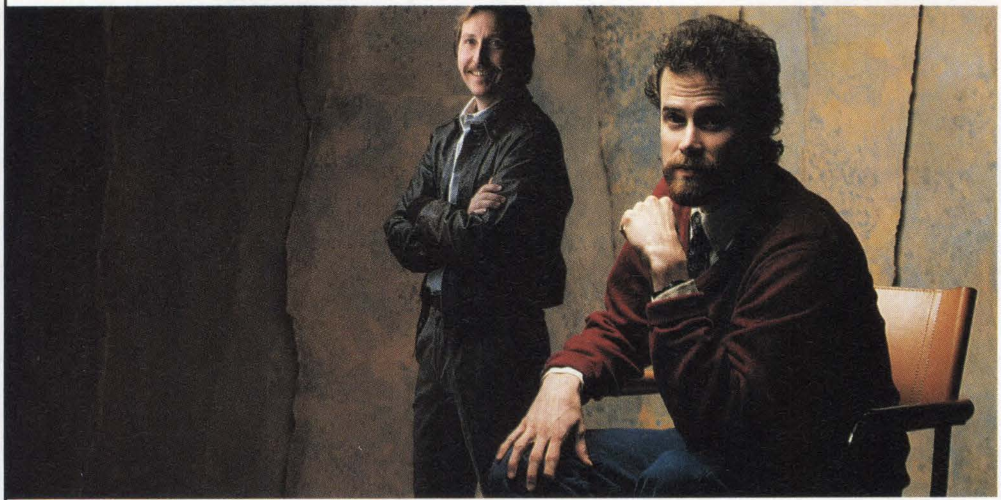

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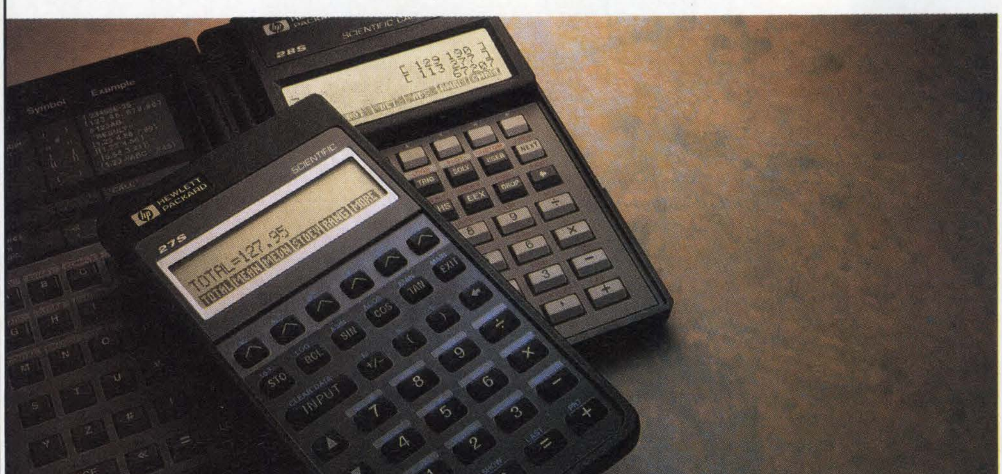

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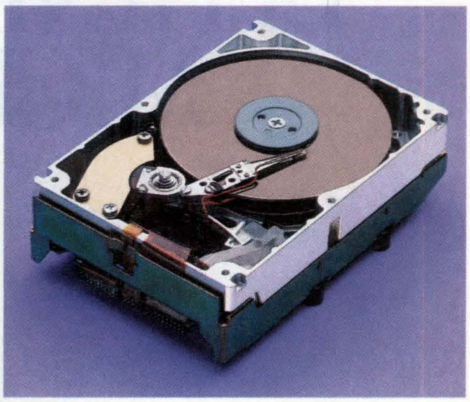

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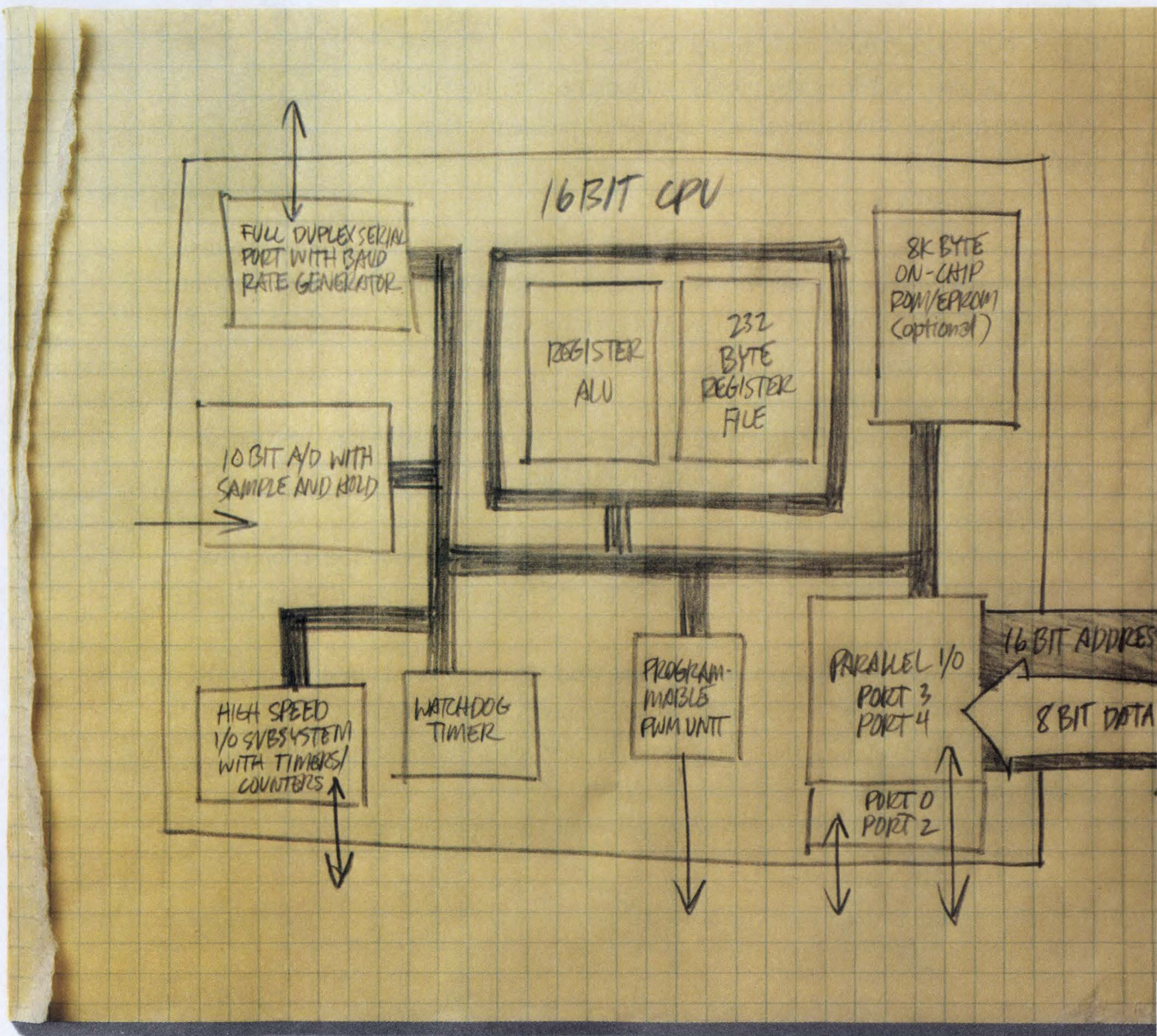


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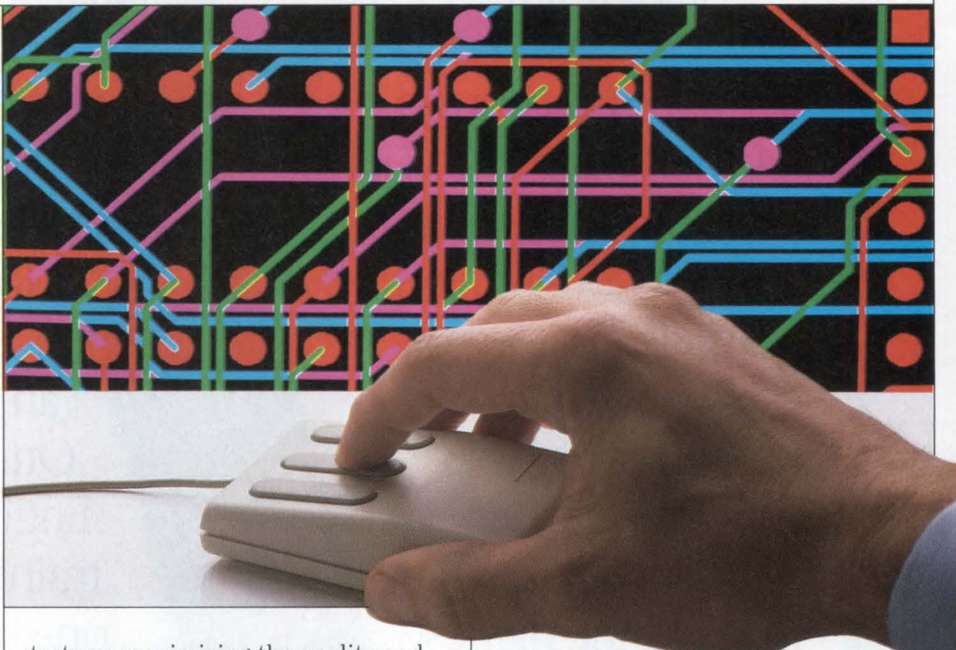

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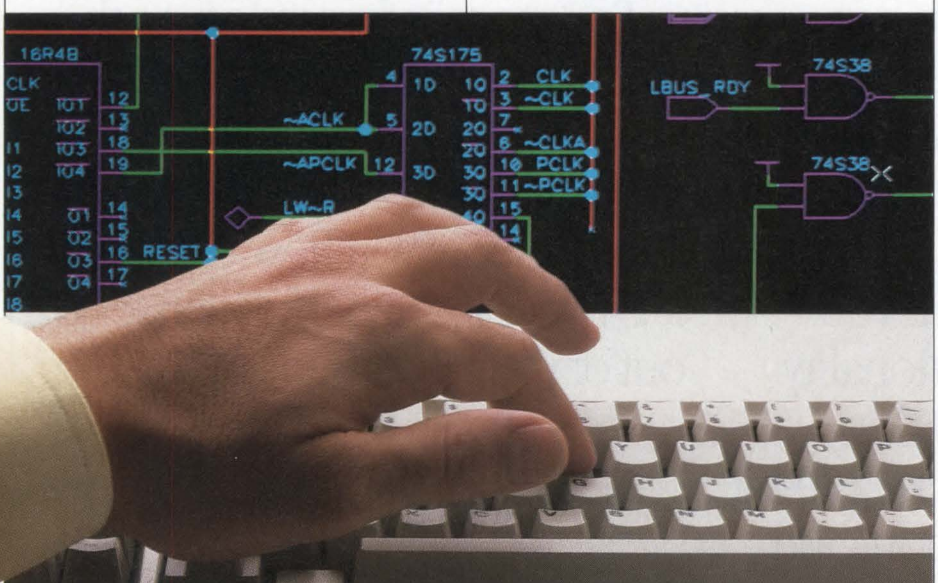


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# State machines solve control-sequence problems

*This article, part 1 of a 2-part series, provides a refresher in the basic theory of state machines and offers two detailed examples of synchronous-state-machine design with common PLDs. Part 2 will follow up with an example of a more difficult, asynchronous state machine and will give some background information on state-machine software packages. Part 2 will also detail a PLD having a novel architecture that suits large state machines.*

Stan Kopec, *Altera Corp*

The state-machine design method provides a structured, systematic approach to the task of designing stand-alone signal-generation or control circuitry for arbiters, bus controllers, encoder/decoders, sequencers, or special counters. You can implement state machines with a variety of logic building blocks, such as TTL SSI/MSI devices, programmable logic devices (PLDs), and ASICs. The user-configurable features of PLDs lend themselves to these control-logic tasks because such tasks often entail making design changes and correcting errors. With PLDs, you can easily and quickly modify your design as you discover errors or as design requirements change. Combining a state-machine game plan with a PLD implementation provides an effective means of solving some knotty control-logic design problems.

Nevertheless, approaching your first PLD state-machine design can be an intimidating prospect. Like mathematical proofs, state-machine design—the way it's presented in many textbooks—often has an air of unreality about it. A few concrete design tips that show how PLDs and state machines mesh, however, can turn the mystery into reliable, working logic.

You can obtain a wide variety of PLDs. Both bipolar and CMOS versions are available; EPROMs, EEPROMs, or fuse links provide the programmability. PLDs have a very regular structure. You can think of a PLD as a stack of identical slices. Each slice of a PLD, beginning with inputs, proceeding through an AND/OR array, and terminating in a possibly registered logic output, is a macrocell. Structurally, the architectures of common, established devices reduce to two basic forms: PLAs, which have a programmable-AND/programmable-OR array, and PALs, which have a programmable-AND/fixed-OR array (newer architectures employing NAND/NAND and NOR/NOR arrays are becoming available, but are not yet in common use).

Each category contains devices that provide either a logic array only (combinatorial PLD) or a logic array plus dedicated registers (registered PLD). A combinatorial PLD is useful only in asynchronous machine designs or for decoding outputs. A PLD with all outputs registered is useful only in synchronous designs. You can also obtain a third kind of PLD—one that allows you to program combinatorial or registered operation on a macrocell-by-macrocell basis **(Table 1)**.

*Combining a state-machine game plan with a PLD implementation provides an effective means of solving some knotty control-logic design problems.*

**TABLE 1—PLD FUNCTIONAL FEATURES AND STATE-MACHINE UTILITY**

| FEATURE | STATE-MACHINE VALUE |
|---|---|
| PROGRAMMABLE LOGIC ARRAY OUTPUT INVERSION | DeMORGAN'S INVERSION OF FUNCTIONS: REDUCE P-TERMS |
| PROGRAMMABLE REGISTERED/ COMBINATORIAL MACROCELLS | STATE VARIABLES/OUTPUT DECODING IN SINGLE DEVICE MACROCELL CASCADING IN SINGLE DEVICE |
| PROGRAMMABLE FLIP-FLOP TYPE | FLIP-FLOP SELECTION FOR MINIMUM P-TERM CONSUMPTION |
| PLA ARCHITECTURE | P-TERM DISTRIBUTION AS REQUIRED BY EQUATIONS |
| VARIABLE/PROGRAMMABLE P-TERM DISTRIBUTION | HIGH P-TERM MACROCELLS FOR COMPLEX EQUATIONS/P-TERM REALLOCATION BETWEEN MACROCELLS |
| POWER-ON RESET OF FLIP-FLOPS | STATE FLIP-FLOPS START IN KNOWN STATE (ZERO) ON POWER-UP |

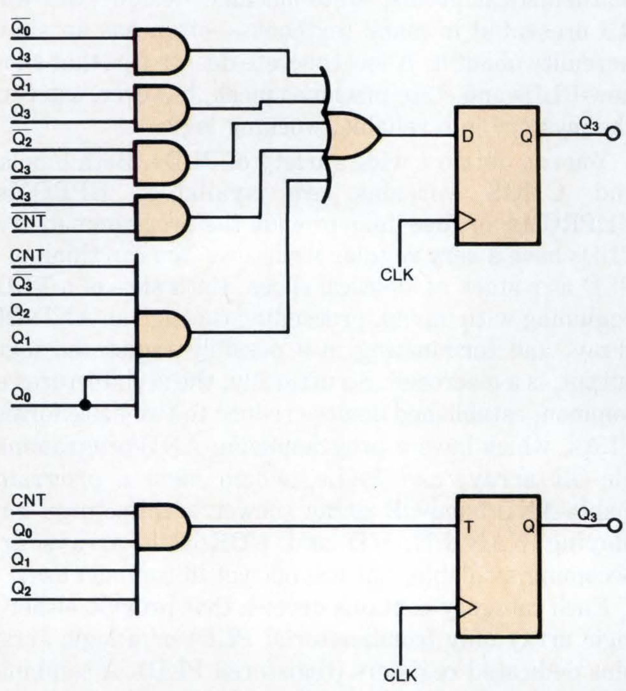



***Fig 1—To determine which flip-flop type is most efficient for an application** you have to analyze the state-transition logic of your state machine. For example, when implemented with D flip-flops (as shown), this 4-bit counter requires five p-terms for its MSB (or most significant state variable). If it's implemented with T flip-flops, it requires only one p-term.*

By using these chips, you can design state machines having either a synchronous or an asynchronous clocking mode.

### Flip-flops for different uses

When you design synchronous state machines, having different register or flip-flop types available on the same PLD can prove useful. Older PLDs offer you a single type of flip-flop, typically the D or SR type. Newer PLDs frequently provide you the option of a user-selectable flip-flop type. In practice, D flip-flops sometimes give you a more efficient synchronous-state-machine implementation; at other times T, SR, or JK flip-flops provide a more efficient synchronous-state-machine implementation. A 4-bit, binary up-counter, which is a basic state machine, provides an example of flip-flop usage.

The fundamental units of a PLA (programmable logic array) are its programmable AND structures. To logically AND logic signals is to take their logical product; therefore, these AND structures are called product terms, or p-terms. Determining which flip-flop type is most efficient for an application requires that you analyze the state-transition logic of your state machine. In a synchronous state machine implemented with D flip-flops, for example, the most significant bit (MSB)—or most significant state variable—of the 4-bit counter requires five p-terms; in a synchronous state machine implemented with T flip-flops, it requires only one p-term **(Fig 1).**

PLD p-terms implement the state-transition logic and output decoding for your state machine. The programmable-OR structure of a PLA allows you to allocate the p-terms where needed. You pay for this flexibility in performance and total p-term count. The PLA's added programmable logic stage can increase the chips' overall array delay over that of the fixed-OR stage of a PAL (programmable array logic). In terms of sheer capacity, typical PLAs provide 48 or fewer p-terms; typical PALs have from 64 to 480 p-terms, or more.

### PAL structure lacks flexibility

The PAL's drawback is that p-terms are assigned in a fixed way to its macrocells. Once you use up the p-terms, you must cascade macrocells (reducing efficiency and performance) or rework the design. To avoid this problem, some PLDs have variable p-term distribution, which varies the p-term count between macrocells. This approach tends to give the PLD a little more flexibility in fitting a given state-machine design. To get the best fit, however, you must consider p-term count and flip-flop type jointly.

Some PLDs also give you the option of inverting their logic-array outputs. This inversion can increase p-term packing by allowing you to use deMorgan's Theorem: $\overline{(A+B)}=\overline{A}\cdot\overline{B}$. Slightly extending this basic statement shows how you can use selective inversion to transform an expression having two p-terms (A+B) into an expression having a single p-term:

$$A + B = \overline{\overline{(A + B)}} = \overline{(\overline{A} \times \overline{B})}.$$

Similarly, you can trade off p-term count for input-variable count in more complex expressions. The p-term savings can sometimes be very dramatic.

### A synchronous DMA state machine: $M_1$

A DMA controller is a good example of a synchronous state-machine design. It's very similar to many state-machine designs you might encounter in a µP-based system. Thinking through the overall design and discussing implementation tradeoffs is a good way to get a feel for the design task.

The DMA controller actually consists of two linked synchronous state machines, as **Fig 2** shows. The master state machine ($M_1$) controls the overall type of transfer to be executed and decides what types of bus cycles to run. The slave state machine ($M_2$) actually runs the bus cycle, issuing control signals, etc, to execute the transfer. (**Ref 1** thoroughly covers the procedure of partitioning a state machine.)

Three loadable down-counters provide address and byte-counting functions. The byte-counting functions interact with the state machines. Four byte-wide data-holding registers permit the assembly of bytes into words, which increases transfer efficiency; they also perform the required byte swapping.

The data bus in this design is a 16-bit 8086 bus. The bus can support 8- and 16-bit peripherals. For efficiency, the memory is accessed only 16 bits at a time. All peripheral transfers start with a DMA request (DREQ)

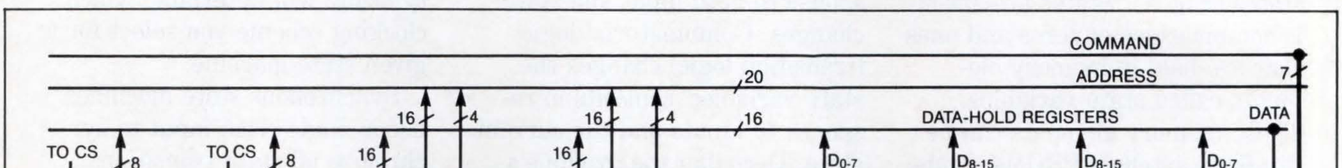



*Fig 2—**This DMA controller comprises two linked synchronous** state machines. The master state machine ($M_1$) controls the overall type of transfer to be executed and decides what types of bus cycles to run. The slave state machine ($M_2$) actually runs the bus cycles.*

*State-variable assignment is one area of state-machine design that is not very algorithmic.*

from the peripheral to trigger transfers of data. This sequence holds true whether the peripheral is the source or the destination of the data.

The DMA controller will have to contend with the following possible combinations of data sources and destinations:

| DATA SOURCE | DESTINATION |
|---|---|
| 16 MEM | 16 MEM |
| 16 MEM | 8 I/O |
| 16 MEM | 16 I/O |
| 16 I/O | 16 MEM |
| 8 I/O | 16 MEM |

The DMA controller will read or write two consecutive byte-wide bus transfers when an 8-bit peripheral is involved.

The sequence of events required to execute a transfer are as follows:

- 1. The μP loads the source and destination pointer register/counters, byte counter, and command register
- 2. The μP gives the STARTX signal to the DMA controller
- 3. $M_1$ requests the bus (REQBUS) from the μP (on DREQ if I/O is involved)
- 4. The μP grants the bus (GRANT) to $M_1$
- 5. $M_1$ initiates the bus cycle
- 6. $M_2$ runs the source/destination bus cycles requested
- 7. $M_1$ decrements the byte counter by 1 or 2

## State-machine basics

State machines are digital logic blocks with inputs, outputs, and states **(Fig A)**. States are specific combinations of zeros and ones that are held in memory elements called state variables. These memory elements can be flip-flops, latches, PROMs, counters, or other bistable structures. Some (asynchronous) state machines even employ state variables composed of feedback paths in otherwise combinatorial logic structures.

The memory in state machines allows them to follow your predefined sequence of states in response to both input and state changes. Combinatorial logic (transition logic) changes the state variables' contents in response to inputs and the current state. Decoding the machine's state and (optionally) its inputs generates the state machine's outputs.

### Synchronous or asynchronous

You can use either a synchronous clocked or an asynchronous unclocked mechanism for your state machine. Your application typically will determine which clocking scheme you select for a given state machine.

Synchronous state machines use a single clock input to synchronize all state transitions. Asynchronous machines can change state in response to any input change. Frequently, in distributed systems or on buses, a central clock is not available because of signal-timing skews or other reasons. Consider the RS-232C handshake, for example. The RS-232C interface has no defined clock signal, and its operation consists of a defined handshake between the data transmitter and the receiver via the DSR, DTR, CTS, and other signals. Transitions between states occur when the appropriate inputs are asserted.

In contrast to synchronous machines, in which both inputs *and* a clock edge must occur to effect a transition, in an asynchronous machine, any input

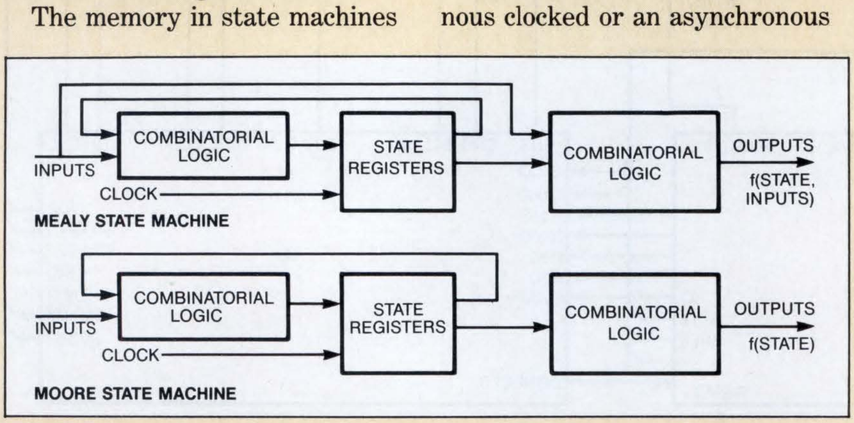



***Fig A—State machines are digital logic blocks*** *with inputs, outputs, and states. States are specific combinations of zeros and ones that are held in memory elements called state variables.*

- 8. Loop back to Step 5 until the byte counter equals zero (BC0)
- 9. $M_1$ releases the bus after the transfer is complete
- 10. $M_1$ asserts the XFERDONE line
- 11. Loop back to Step 1.

**Fig 3** shows the state-transition diagram of a state machine that implements $M_1$ with 13 states. For simplicity, the diagram does not show any holding (hold-state) transitions. (You can assume that each state has such a transition, whose equation is the complement of the logical OR of all transition terms that force a new state.) Neither is the state-transition diagram cluttered with all the possible paths back to the RESET state. However, just because the state-transition diagram shows no hold-state and reset transitions does not mean you can ignore these transitions when you write your state-variable excitation equations—you must include the equations in your PLD specification.

In a synchronous state machine, functions next to the transition arrows must be true on the rising edge of CLK in order for the state change to occur. Outputs for a given state are in the states' circle symbols (they're in typical Moore-machine notation; a Mealy machine would associate outputs with transition arrows, not states).

**List inputs and outputs**

The first step in designing the logic to implement the state machine is to list inputs and outputs. The state diagram shows that $M_1$ has nine inputs (exclusive of CLK) and 13 outputs. Because you have 13 states, you

glitch is unqualified and can cause problems. In such designs, you should use Schmitt-trigger buffers or filtering to condition the inputs for added safety.

In general, synchronous machines are easier for you to design and less error prone than asynchronous ones; the synchronous state machine's single clock source lets you more easily avoid spurious machine transitions. Asynchronous designs should be a last resort.

**Mealy and Moore machines**

The two basic classes of state machines are Mealy and Moore machines. Mealy machines have outputs that are combinatorial functions of the state and the inputs. Moore machines' outputs are functions only of the machine state. Moore outputs change only on state transitions; Mealy outputs can change directly in response to inputs. Mealy machines can give you more-efficient implementations (that is, implementations having fewer state variables) in those applications requiring many output combinations per state.

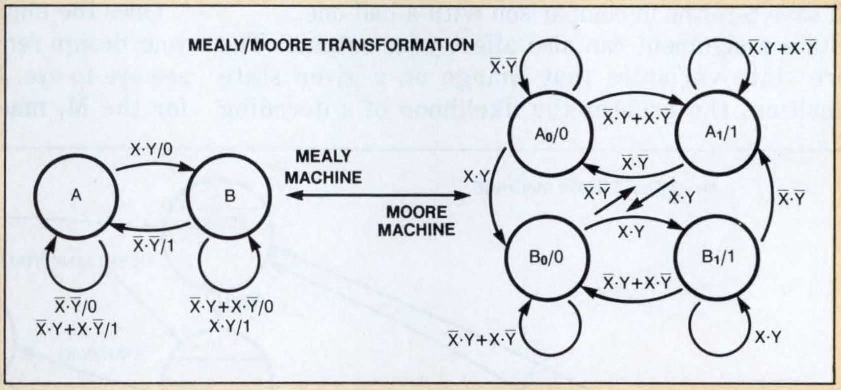



*Fig B—You can implement any state-machine specification as either a Mealy or a Moore machine. The Mealy version has two states (one state variable) and one output, which varies according to the input combination of X and Y. The equivalent Moore version has four states (two state variables) that generate the corresponding output function.*

**Fig B** shows two alternative implementations of the same state machine. The Mealy version has two states (one state variable) and one output, which varies according to the input combination of X and Y. The Moore version has four states (two state variables), which generate the corresponding output function.

The differences in the operation of these two implementations are externally undetectable. In fact, you can always transform your Mealy machine design into an equivalent Moore machine: For each Mealy-machine state transition that has a different output value (or values), you insert a new state in the Moore machine.

*Most designers use a trial-and-error method of state assignment to see if the target PLD has enough p-terms to satisfy the state machine's requirements.*

know that you can encode these states with four state variables (that is, four flip-flops: $2^4=16$). The outputs plus the state variables equal 17, so an initial estimate is that you'll need a PLD (or PLDs) with at least 17 macrocells and nine inputs.

The second step is to assign state-variable combinations to particular states. State-variable assignment is one of the areas of state-machine design that is not very algorithmic. Most designers use a trial-and-error method of assignment: they assign variables, generate flip-flop excitation equations for different types of flip-flops, and see if the target PLD has enough p-terms to satisfy the equations' requirements. Some PLD-software packages can automatically look for a PLD or group of PLDs that will hold your equations.

You'll have three unused states, because you need only 13 of the 16 possible state-variable combinations. You should strive to achieve an optimal state-variable assignment, because a good state-variable assignment will save p-terms in comparison with a bad one.

State assignment can also affect your outputs. The more state variables that change on a given state transition, the greater the likelihood of a decoding glitch. If your outputs will drive edge-sensitive logic directly, you may want to consider using a state assignment that's similar to a Gray code. This type of assignment allows only one variable to change at a time. By allowing only one variable to change at a time, you eliminate glitches.

After making the state assignment, you generate the state-transition equations. If you decide to use D flip-flops, the flip-flop excitation equations must cover all instances in which the flip-flop's output in the next state is a one. This coverage includes hold-state transitions as well as transitions between states. The equations for SR flip-flops, on the other hand, reflect only transitions between states and are frequently more compact. You can minimize the equations by using methods outlined in most basic logic-design texts (see **Ref 1 or 2**) or, with some practice, you can learn to minimize the equations for most designs by inspection. For complex designs, you may need state-machine-design software.

Once the minimization is done, you're ready to see if your design requirements and the PLDs you've chosen see eye to eye. **Fig 4** shows a typical state assignment for the $M_1$ machine. The figure contains excitation

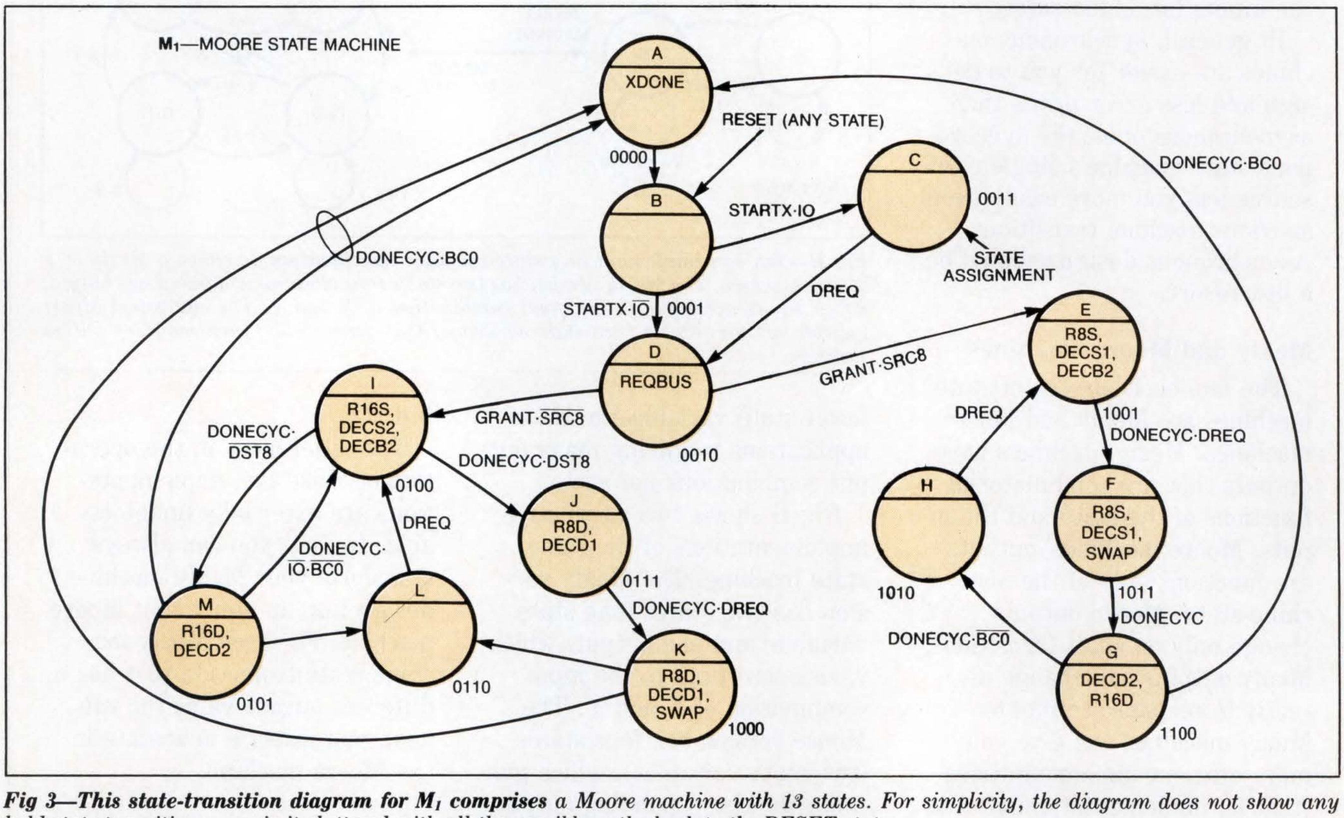



*Fig 3—This state-transition diagram for $M_1$ comprises a Moore machine with 13 states. For simplicity, the diagram does not show any hold-state transitions, nor is it cluttered with all the possible paths back to the RESET state.*

equations for both D-flip-flop and SR-flip-flop realizations. The p-term requirements for state variables of the D-flip-flop implementation are 11, 12, 9, and 6. The p-terms for the SR-flip-flop design are (set/reset) 4/6, 5/7, 2/3, and 2/3. So, in this instance, the availability of SR flip-flops in the target PLD is a plus. Output p-term decoding requirements are much more modest: A typical output consumes two p-terms.

Most PLDs don't directly satisfy the high p-term counts of the D-flip-flop implementation of $M_1$. Given the macrocells of most basic PLDs, only one equation of the D-flip-flop realization would fit within an 8-p-term macrocell. To increase the logic-term count, you'd have to cascade macrocells to build up an adequate number of terms. If you used traditional 20-pin PALs (or equivalents), you'd need three devices: a 16R4 for the registered/state-variable part of the job and two 16L8s for the combinatorial-output decoding and p-term expansion.

Higher-density PLDs such as the EP600/900 and

```
State  State Variables
        Q3 Q2 Q1 Q0
---------------------
A        0000
B        0001
C        0011
D        0010
E        1001
F        1011
G        1100
H        1010
I        0100
J        0111
K        1000
L        0110
M        0101
Unused   1101 1110 1111

M1 D Flip-Flop Excitation Equations:

D3 = (0111*DONECYC*DREQ + 1X00*DONECYC' + 0010*GRANT*SRC8 +
     10X1 + 1100*DONECYC*BC0' + 1010)*RESET'             (6 TERMS)

D2 = (1011*DONECYC + 1100*DONECYC' + 1100*BC0 + 0010*GRANT*SRC8' +
     0100 + 01X1*DONECYC' + 011X*DREQ' + 0101*IO*BC0'*DONECYC +
     1000*DONECYC*BC0')*RESET'                           (9 TERMS)

D1 = (0001*STARTX + 0010*GRANT' + 0011*DREQ' + 0100*DONECYC*DST8 +
     0111*DONECYC' + 0111*DREQ' + 0101*DONECYC*IO*BC0' +
     1X00*DONECYC*BC0' + 0110*DREQ' + 1001*DONECYC*DREQ +
     1011*DONECYC' + 1010*DREQ')*RESET'                  (12 TERMS)

D0 = 0000 + 0001*STARTX' + RESET + 0001*STARTX*IO + 0X11*DREQ' +
     0100*DONECYC + 0101*DONECYC' + 0111*DONECYC' +
     0010*GRANT*SRC8 + 1001 + 1011*DONECYC               (11 TERMS)

M1 SR Flip-Flop Excitation Equations:

S3 = 0111*DONECYC*DREQ + 0010*GRANT*SRC8                 (2 TERMS)
R3 = RESET + 1000*DONECYC*BC0' + 1100*DONECYC*BC0        (3 TERMS)

S2 = 0010*GRANT*SRC8' + 1011*DONECYC                     (2 TERMS)
R2 = RESET + 0111*DONECYC*DREQ + 1100*DONECYC            (3 TERMS)

S1 = 0001*STARTX + 1001*DONECYC*DREQ + 1X00*DONECYC*BC0' +
     0101*IO*BC0'*DONECYC + 0100*DONECYC*DST8            (5 TERMS)
R1 = RESET + 0001*STARTX*IO' + 0010*GRANT + 0111*DONECYC*DREQ +
     0110*DREQ + 1010*DREQ + 1011*DONECYC                (7 TERMS)

S0 = 0000 + 0010*GRANT*SRC8 + 1010*DREQ + 0100*DONECYC   (4 TERMS)
R0 = RESET + 0001*STARTX*IO' + 0011*DREQ + 1011*DONECYC +
     0101*DONECYC + 0111*DONECYC*DREQ                    (6 TERMS)
```

***Fig 4—This typical state assignment for $M_1$*** *also has excitation equations for both D-flip-flop and SR-flip-flop realizations. For $M_1$, the availability of SR flip-flops in the target PLD is a plus. The p-term decoding requirements of the output are modest: A typical output consumes only two p-terms.*

*The more state variables that change on a given state transition, the greater the likelihood of a decoding glitch.*

22V10 have higher macrocell and output counts. They can also mix and match combinatorial and registered functions. For example, two EP600s or 22V10s, or a single EP900 (24 macrocells/12 inputs), could potentially implement $M_1$. The EP1210s' and the 22V10s' variable p-term distribution can support $M_1$'s high p-term count. The EP600/900s also have programmable flip-flop types, so they allow an SR implementation; for $M_1$, SR flips-flops require the fewest p-terms.

Which devices you use to implement your state-machine design will depend on the device speed, component cost, board space, and personal preference. Low-density, bipolar PALs offer the highest speed; CMOS PLDs have higher densities and a more flexible architecture. A PLA's architecture can also implement the SR design of the $M_1$ machine effectively. The SR design requires 32 p-terms. Because popular PLAs such as the 82S105 supply 48 p-terms, they can contain this design. However, you must use external PLDs to decode the PLA's state variables, and the result is still a multichip design.

**A synchronous bus controller: $M_2$**

The $M_2$ machine implements the flow shown in **Fig 5.** $M_2$ requires a minimum of eight CLK edges to perform a bus transfer. The machine requires nine basic states, including IDLE. Each type of cycle (memory read, memory write, I/O read, and I/O write) requires $M_2$ to stimulate distinct output-control lines. This machine is therefore a good candidate for a Mealy design.

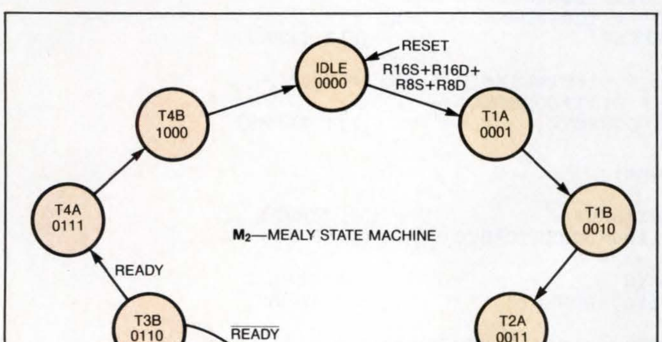



***Fig 5—From $M_2$'s state-transition diagram,** you can see that each type of cycle (memory read, memory write, I/O read, and I/O write) requires $M_2$ to stimulate distinct output-control lines. This machine is therefore a good candidate for a Mealy design. (The unlabeled transitions are unconditional.)*

The machine takes its primary inputs from $M_1$ for 8- and 16-bit source and destination commands—R8S, R16S, R8D, and R16D—along with SWAP. Additional inputs consist of an external ready line (READY), as well as the source and destination control lines for memory and I/O operations. The source and destination control lines come from the command register.

The machine generates two types of outputs. One type—$\overline{MEMRD}$, $\overline{MEMWR}$, $\overline{IORD}$, $\overline{IOWR}$, and $\overline{ALE}$—effects μP communication and bus control. The remaining lines decrement the appropriate address counters by either one or two, signal $M_1$ that transfer is complete (DONECYC), and enable address and data information on the computer's buses at the appropriate times.

$M_2$ has nine inputs and 14 outputs. You need four state variables to encode the nine states, leaving seven states unused. $M_2$ has very little internal branching in its control flow **(Fig 5).** This lack of branching is typical of many sequencer applications. The implementation of the machine resembles that of a modulo 9 counter, except that the READY input causes a wrinkle at states T3A and T3B: HOLSTATE if READY not active.

**Fig 6** shows both D and T flip-flop excitation equations for $M_2$. The D implementation in this case actually requires fewer p-terms than the T. This situation occurs partially because of the complexity of implementing the RESET terms with toggle equations.

One solution for the problem of implementing RESET is to take advantage of the separate flip-flop reset-input terms that many PLDs have. If you define the reset state as 0000, you can reduce the logic-term requirements.

Outputs consume between one and six p-terms; the four control lines ($\overline{IORD}$, $\overline{MEMWR}$, etc) consume four to six p-terms each. Because no function requires more than eight p-terms for the D-flip-flop design, these equations fit into an 8-p-term macrocell (which is common to many PLDs) with no cascading. In this case, the macrocell consumption is equal to outputs plus state variables, or a total of 18.

An alternative implementation of this machine as a Moore machine would require 33 states: eight clocks times four cycle types, plus IDLE. These states would require six state variables to encode them, plus the output decoding for the 14 outputs, increasing the total number of macrocells required to 20. $M_2$ shows the economy of a Mealy machine when the machine flow is constant, but the outputs vary depending on the inputs.

Predicting the performance of your synchronous state machine isn't difficult if you read the PLD's data

*Which devices you use to implement your state-machine design will depend on the device speed, component cost, board space, and personal preference.*

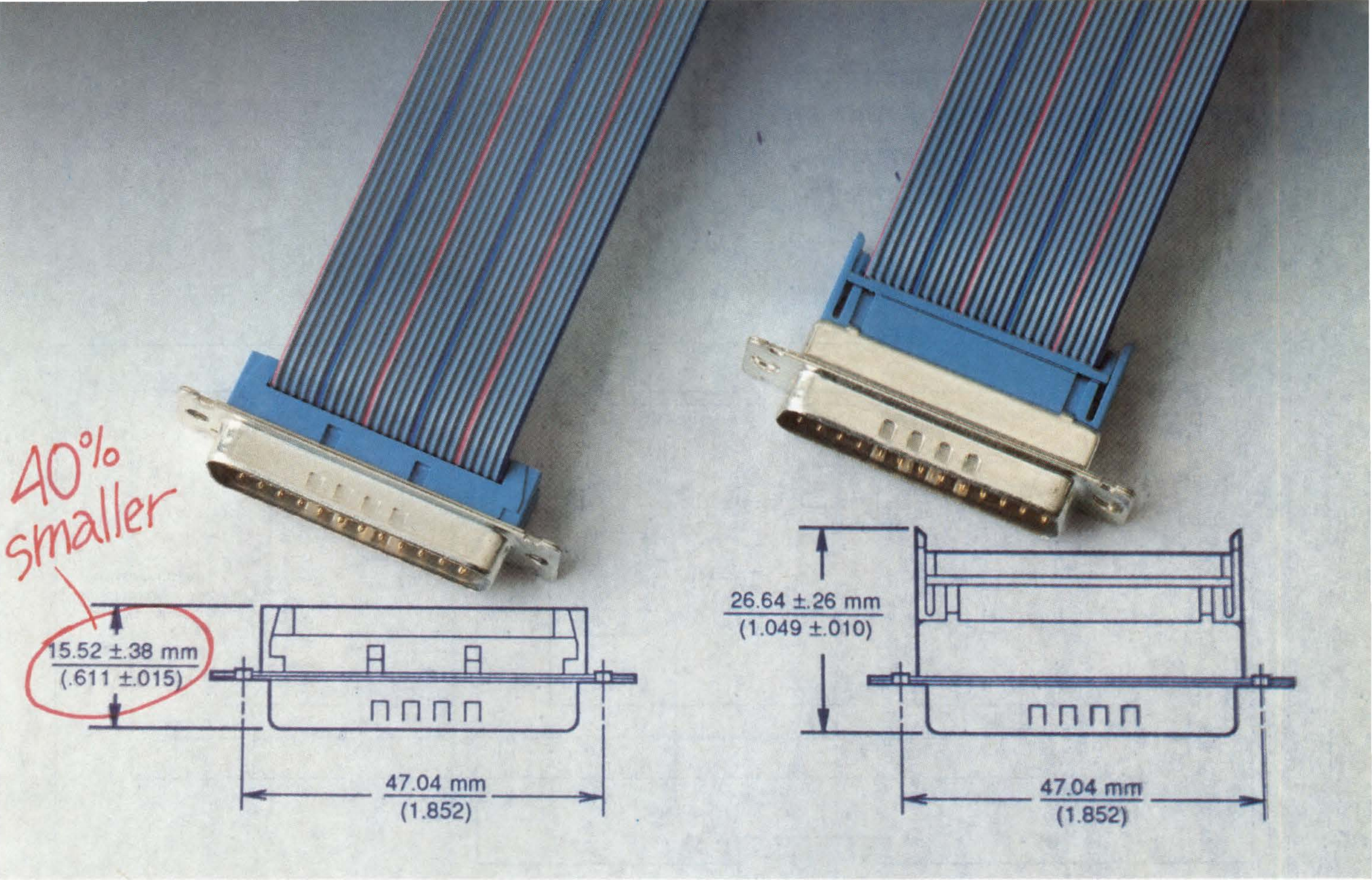
sheet carefully. Although PLD data sheets typically quote an $f_{MAX}$ number in megahertz, don't confuse this frequency with the potential operating frequency of your machine. The $f_{MAX}$ is typically an internal flip-flop toggle rate that benchmarks the absolute frequency. Your machine will be interacting with other circuitry, and you need to factor several additional specs into your calculations **(Fig 7)**.

The first critical number is clock-to-output delay (sometimes designated $T_{CO}$). Most PLDs also spec an input setup time to the clock ($T_{SETUP}$). $T_{SETUP}$ approximates the actual PLD logic array's input-output delay. The inverse of the sum of these two numbers is the fastest actual clock rate at which your state machine will probably be able to run. If the clock period is greater than this sum, you'll be able to take an output from your machine and feed it back into an input to affect the state transitions. Many designs include external logic in the PLD's output-input loop; you shouldn't ignore this logic, because its delays will lengthen the period.

These calculations hold true for a state machine in which each state variable is implemented in only a single macrocell. If you must cascade macrocells, you

```
State  State Variables
         Q3 Q2 Q1 Q0
---------------------
IDLE       0000
T1A        0001
T1B        0010
T2A        0011
T2B        0100
T3A        0101
T3B        0110
T4A        0111
T4B        1000
Unused     1001-1111

M2 D Flip-Flop Excitation Equations

D3 = 0111*RESET'                                    (2 TERMS)

D2 = (0011 + 010X + 0110)*RESET'                    (3 TERMS)

D1 = (0010 + 0X01 + 0110*READY)*RESET'              (3 TERMS)

D0 = (0000*R16S + 0000*R8S + 0000*R8D + 0000*R16D + 0010 +
     01X0)*RESET'                                   (6 TERMS)

M2 T Flip-Flop Excitation Equations:

T3 = 0111 + 1XXX*RESET                              (2 TERMS)

T2 = 0X11 + X1XX*RESET                              (2 TERMS)

T1 = 00X1 + 0111 + 0110*READY'+ XX1X*RESET          (4 TERMS)

T0 = 1XXX + X1XX + XX1X + XXX1 + 0000*R16S + 0000*R8S + 0000*R8D
      + 0000*R16D + XXX1*RESET                      (9 TERMS)

M2 Output Equations (Selected)

ENS = 0001*R16S + 0001*R8S                          (2 TERMS)

ENLL = R16D*(0011 + 01X0 + 0101) + R8D*SWAP'* (0011 + 01X0 +
       0101)                                        (6 TERMS)

LDL = 0110 * SWAP' * (R8S + R16S)                   (2 TERMS)

IORD' = (0011 + 010X + 0110) * SMIO'* (R16S + R8S)
                                                    (6 TERMS)

MEMWR' = (0101 + 0110) * DMIO * (R16D + R8D)        (4 TERMS)
```

***Fig 6—For $M_2$, the D-flip-flop implementation*** *in this case actually requires fewer p-terms than does the T-flip-flop implementation. This situation occurs partially because of the complexity of implementing the RESET terms with toggle equations.*

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*Predicting your synchronous state machine's performance is not difficult if you read your PLD's data sheet carefully.*

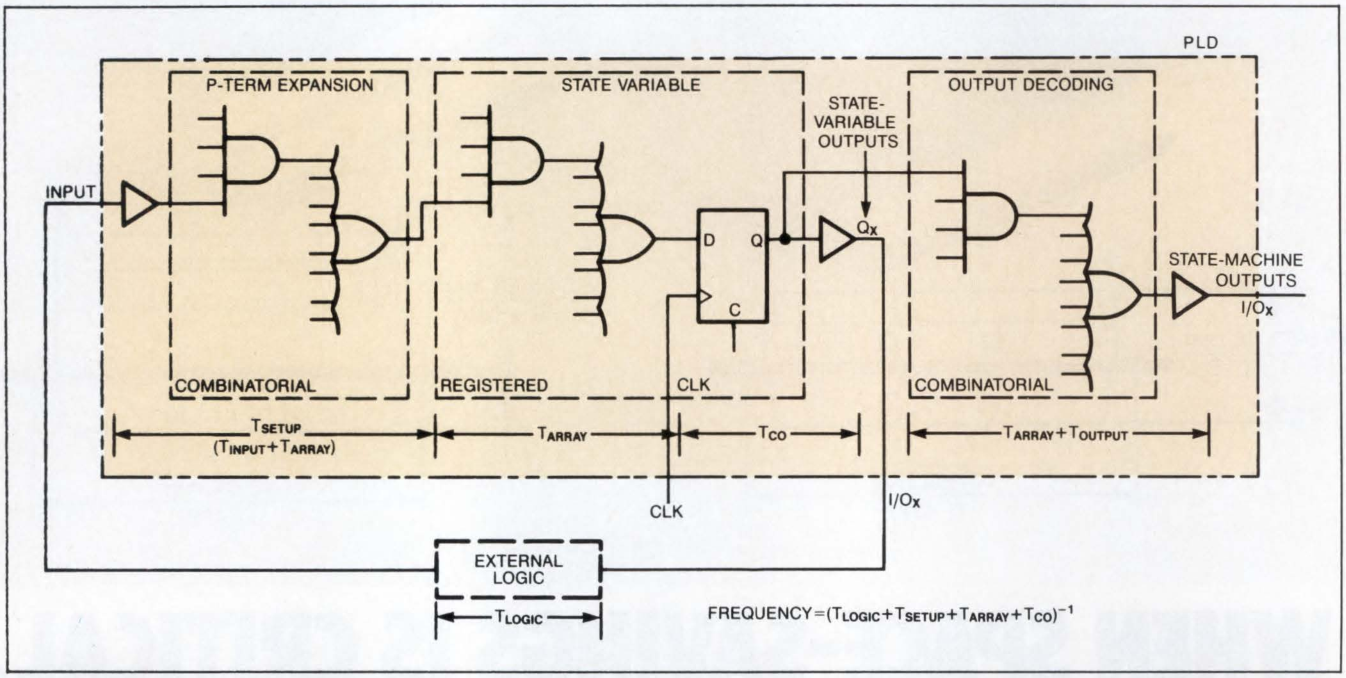


***Fig 7—Although PLD data sheets typically quote** an $f_{MAX}$ number in megahertz, don't confuse this frequency with the potential operating frequency of your machine. Your machine will interact with other circuitry, and you need to factor all the specs shown in this diagram into your calculations.*

must add an additional $T_{PD}$ (logic array) delay for each level of cascading. Depending on your application's requirements, this additional delay may or may not be a problem.

For example, when $T_{CO}$=15 nsec and $T_{PD}$=25 nsec, an added level could depress the operating rate from [1/(15 nsec+25 nsec)]=25 MHz, to [1/(15 nsec+25 nsec+25 nsec)]=16 MHz.

$T_{PD}$ also determines output-decoding time when you use separate PLDs for registered and combinatorial functions. This separation can prove to be a source of unacceptable clock-to-machine output skews. $T_{CO}+T_{PD}$ is the overall delay in this arrangement (15 nsec+25 nsec=40 nsec for a typical PLD). This delay limits such a multichip design to applications with 10-MHz or slower clocks.

If skews arising from the decoding's propagation delay do become excessive, you can modify the design to register the control outputs. This modification involves pipelining the control outputs. You clock each output flip-flop with the master machine's clock. The result is that the control lines are only one clock-to-output delay ($T_{CO}$) behind the clock. Unfortunately, pipelining can be very complex because of the look-ahead nature of output logic. Therefore, pipelining is best left as a last recourse. **EDN**

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## Author's biography

*Stanley Kopec is manager of product planning for programmble logic at Altera Corp in Santa Clara, CA. He has been with Altera for three years. Prior to joining Altera, Stan worked for Exel Microelectronics and was in charge of μP-peripheral development. He holds a BSEE from the State University of New York at Buffalo and an MSEE from the University of Illinois. In his spare time he enjoys racquetball, skiing, and reading.*

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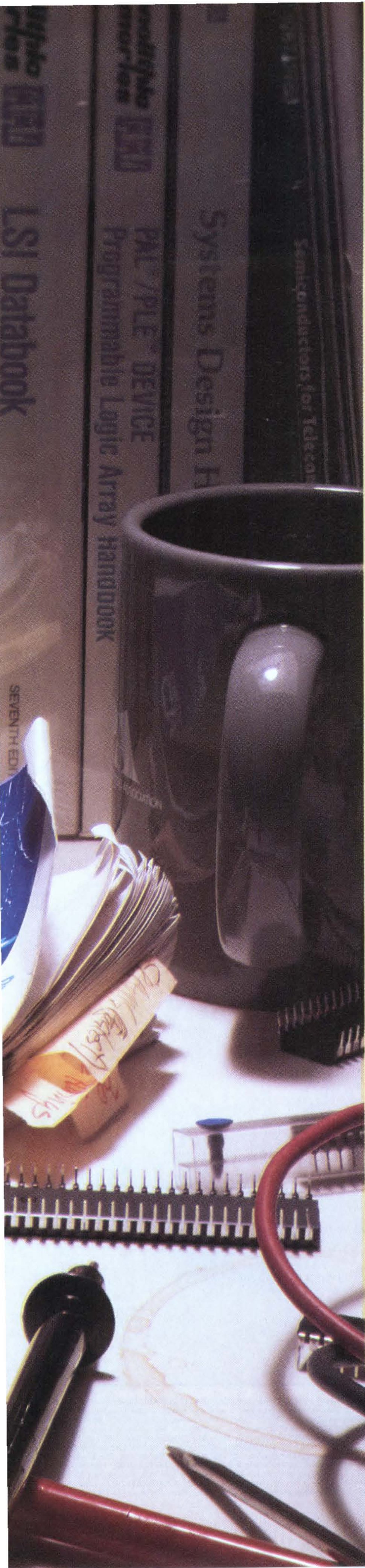


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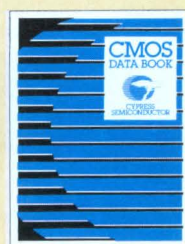


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| Max. Clock Freq. (typ)J/K F-F ($C_L$ = 15pF) | 150MHz | 60MHz | 45MHz | 2MHz |
| Quiescent Power Diss. (typ) (GATE) | 0.01$\mu$W | 0.01$\mu$W | 8mW | 0.01$\mu$W |
| Noise Margin $V_{IH(min)}/V_{IL(max)}$ | 3.5V/1.5V | 3.5V/1.5V | 2.0V/0.8V | 3.5V/1.5V |
| Output Current $I_{OH}I(min)/I_{OL}$ (min) | 24mA/24mA | 4mA/4mA | 0.4mA/4mA | 0.12mA/ 0.36mA |
| Op. Volt. Range | 2-6V | 2-6V | 4.75-5.25V | 3-18V |
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**Timing analysis complements simulation**

Note that timing analysis doesn't replace simulation. Simulation continues to provide a proven means of testing the function of a design by exercising and evaluating circuit logic (with a set of input patterns called test vectors). A thorough simulation can reveal a variety of errors, such as reversed polarities, missed clocking periods, or incorrect logic implementation.

Widely available simulators have simplified the generation of test vectors and made simulation a time- and cost-efficient method of uncovering certain circuit-behavior problems prior to test-program development or production.

Design verification using simulation has some significant limitations, however, particularly for VLSI circuit designs. Thorough simulation of large designs can require a prohibitive level of user input and system memory (200k bytes of test-vector input is not unusual for large circuits). And because simulation only exercises circuit functionality to the degree enabled by the input vectors, an incomplete set of input test vectors can severely limit the value of the results.

Simulation also fails to provide complete information about timing errors that occur because of the makeup of sequential systems. In such systems, signal propagation is not simultaneous—for example, many delays can influence the arrival time of signals at the several inputs of a single gate. Before you can safely finalize a design, you must solve timing problems caused by these delays—but simulation's pattern-dependent approach makes it impossible to detect all of them.

**Simulation can't locate critical paths**

For example, if a signal misses a given clock period, simulation might show an error, but it cannot report the path that introduced the critical delay. If the delay occurs under marginal conditions, simulation might not reveal the error at all, and the circuit could go to

*Undiscovered timing problems can pervade VLSI designs that simulators have pronounced error free.*

production with a flaw destined to make it fail under certain conditions. So, though simulation alone can detect some timing errors, it cannot fully analyze circuit timing.

These limitations of simulation, along with the steady increase in VLSI circuit sizes, have prompted many designers to include timing analysis as part of their overall verification scheme **(Fig 1).** Before you espouse timing analysis, however, you should understand what it can bring to your own design process.

Timing analyzers detect hazardous timing situations —and in very large designs, at least a few of these situations are likely to go undetected by simulation. In addition, timing analysis can help you identify long delay paths that affect the maximum speed of your design. Some timing analyzers report delay information only on selected paths, and some report delays on all the paths in a circuit. Either approach lets you speed up your design by finding the slowest propagation paths (called critical paths), pinpointing the troublesome delays, and allowing you to make necessary changes. For designers working with VLSI circuits, critical-path reporting is an effective alternative to guessing at the slowest paths in advance.

Timing analysis has its own inherent limitations, of course. For instance, static timing analysis cannot recognize or exercise circuit functionality, so it may report on logically impossible paths (although some tools allow you to specify and disable these paths), and it does not verify the logical correctness of the design. So timing analysis is an adjunct to—not a replacement for—simulation in ensuring proper logic function.

**Picking a timing analyzer is complex**

Once you accept the fact that timing analysis is essential to efficient VLSI design, you must address several questions:

- Is error detection enough, or do you need more detailed analysis of circuit timing (that is, information for optimizing circuit speed)?
- Will you need information about every path in certain circuits?
- How will you calculate delays through and between blocks when generating models?
- Does your average design-cycle time demand a timing analyzer that runs interactively, or will batch mode be acceptable?

You can obtain the answers to these questions only through an understanding of available approaches. In some cases, you can make definite value judgments; for example, static timing analysis is frequently preferable to dynamic timing analysis. In other instances, your choice of analysis tools will depend on the nature of the designs and technologies you routinely encounter. Delay calculation for boards consisting of standard TTL parts, for instance, is straightforward because logic delays are nearly independent of the logic implementation. In such cases, you can rely on libraries of basic gate delays in assembling a picture of system timing. But in VLSI MOS circuits, basic delay calculations are more complicated. When selecting a timing analyzer for MOS environments, you will therefore want to select a tool that provides carefully calibrated gate-level models —or, perhaps, one that can carry out analysis on the transistor level **(Ref 1).**

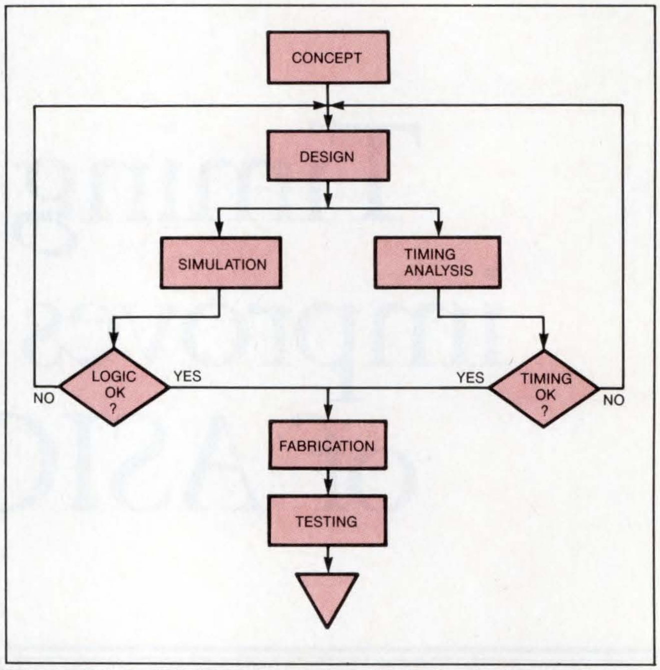
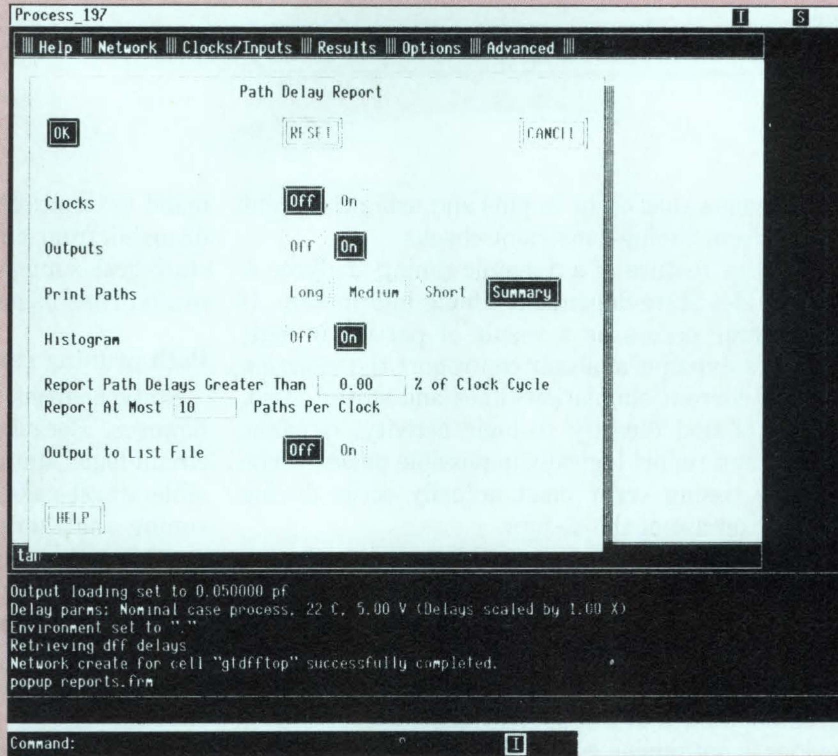



***Fig 1—When ASIC design*** *employs both simulation and timing analysis, the complementary approach to verification can result in significant cost and time savings.*

**Dynamic analysis finds state dependence**

At the heart of any timing-analysis method is the concept of the critical path—the slowest of all signal-propagation paths during a given cycle of circuit operation. Some timing analyzers require you to guess the critical path, exercise it with input vectors, and see if any errors occurred during that exercise. This technique is known as pattern-dependent, or dynamic, timing analysis, and it runs as an integrated extension to simulation. The dynamic approach detects errors by

# Timing analyzer is integral to ASIC compiler




***The user interface** for the Concorde timing analyzer lets you control major functions from a single menu.*

The Concorde timing analyzer from Seattle Silicon (Bellevue, WA) is an integral part of the Concorde ASIC Compiler, a combination of automated tools for ASIC design.

The compiler supplies logic synthesis and generation of simple cells and complex modules for specific semiconductor processes. It links to CAE gate-level simulators and provides a set of tools for placement and routing in complex VLSI circuits. The tools allow designers with limited IC design experience to use a CAE workstation to construct high-end ASIC designs.

### Match circuit size

The Concorde timing analyzer is exclusively a full-coverage static timing analyzer, but it is database compatible with simulators so that static analysis and simulation share the same models and delay calculations. Concorde's static approach and path-pruning capability make it fast and memory efficient (memory usage in the Concorde critical-path algorithm varies linearly with circuit size).

The static approach provides comprehensive path information on the gate and block levels and relieves you of the responsibility for creating test vectors. When coupled with traditional analysis tools, Concorde provides a practical, efficient methodology for performing path analyses and finding timing errors.

Concorde performs both critical-path and full-path enumeration; you may select either algorithm for any portion of a design. The critical-path delay computations include interconnect capacitance. A path-disable utility lets you temporarily disable illogical paths that may be listed during critical-path analysis.

As a companion to traditional logic-simulation tools, the Concorde timing analyzer allows you to detect many timing errors that simulation alone might miss: setup and hold errors, pulse-width constraint violations, warnings about glitches on gated clock lines, and long path errors. With Concorde, you can find and fix such problems while you can still do it economically. In addition to flagging errors, Concorde provides you with circuit-speed estimates that you can use to optimize overall performance.

Concorde can derive gate and interconnect models from the circuit geometry of the target process. The models are calibrated for accuracy and allow you to examine how process, temperature, and voltage variations affect timing. Concorde's modeling is integrated with the cell and module generators, so it automatically incorporates changes and generates new models based on the options you choose during design modification.

### Track down critical paths

The Concorde timing analyzer provides other features that are useful in the VLSI-development environment: full support and recognition of multiple clocks within circuits; full path disabling, including state assignment to primary inputs; a critical-path query mode that allows you to locate the critical path to a node, from a node, or between specified nodes; a histogram-output mode that graphically shows clustering of path delays relative to the driving clock signal; and timing analysis of asynchronous portions of the design, such as preset and clear circuitry.

*Simulation only exercises circuit functionality to the degree enabled by the input vectors.*

buffering events that occur in pins and using the event data to perform timing-constraint checks.

One positive feature of a dynamic timing analyzer is that it provides state-dependent timing information. If a timing error occurs as a result of particular logic conditions, a dynamic analyzer can report the violation in terms of current simulation times and states. Also, because it is tied directly to logic activity, dynamic analysis cannot report logically impossible paths—to be detected, a timing error must actually occur during functional exercise of the design.

However, several important problems can make dynamic timing analysis an unattractive alternative to static timing analysis for VLSI design. One disadvantage to pattern-dependent tools is that they fail to provide any comprehensive path information. One of the greatest values of timing analysis is the assistance it provides in optimizing circuit speed. But, particularly in VLSI circuits, such optimization depends on efficiently identifying paths prone to troublesome delays. Because dynamic timing analyzers do not take a path-oriented approach, they aren't always the best tools to assist with your optimization efforts.

Another related drawback of dynamic analyzers is the amount of time and user input they can require. Because dynamic timing analyzers perform timing checks only on those portions of a circuit they fully exercise with test vectors, dynamic analysis of large circuits usually demands multiple runs. In addition, dynamic analysis causes a slowdown in simulation time because it requires that the simulator (and/or models) continually evaluate relationships among signals arriving at components.

**Static timing analysis is path oriented**

These drawbacks can make dynamic timing analysis cumbersome for many design situations. But in nearly all cases, you can use path-oriented static timing analysis, which is based on an algorithm that sums component and interconnect delays either forward or backward along each path. This computation does away with dynamic timing analysis's pattern dependency. Because simulators calculate worst-case delays (those responsible for the slowest path in a circuit) directly from component and interconnect delays, static timing analyzers do not force you to guess at critical paths. The pattern-independent, path-oriented approach of static timing analyzers accurately identifies your critical paths for you.

Static timing analyzers also do away with the demand for multiple runs. Because the static approach is divorced from circuit functionality, you can obtain a statistical summary for all circuit paths without repeated runs using multiple input vectors.

**Path pruning can prevent false alarms**

Static analysis does have some limitations of its own, however. Because it traces paths without exercising circuit logic, static analysis can report a logically impossible worst-case path. For this reason, good static timing analyzers include some kind of path-pruning capability that allows you to disable illogical or impossible paths for subsequent iterations. Also, a static analyzer might not report all state-dependent timing errors because it can't always determine the state of a pin at any given time—it is only aware of potential transitions.

**Fig 2** illustrates some of the differences discussed above. Accurate dynamic analysis of this circuit requires full test vectors and accurate models of each of the five gates. Even with full user input, this approach provides no hard information about the delays along the various paths. However, it does report on dynamically detectable state-dependent timing errors. For instance, if the D and CLK signals arrive at the flip-flop simultaneously, dynamic timing analysis can detect and report the resultant setup violation, but it cannot identify the paths involved. Static timing analysis of the circuit in **Fig 2** can identify the setup violation, identify the slowest path to the D input, and identify the node-to-node delays along both the path to D and the path to CLK. Knowing the component delays within specific paths allows you to modify design elements to speed up

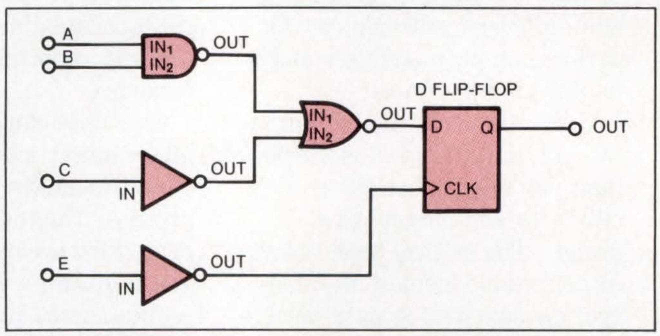



***Fig 2—A simple circuit** illustrates the differences between dynamic and static timing analysis. Dynamic timing analysis would report that a setup violation occurs if signals reach the flip-flop's D and CLK inputs at the same time. Static timing analysis would report the same violation but would also report the slowest path to D (A, B, or C to D) and also provide the delays between nodes on both the critical path to D and the path to CLK.*

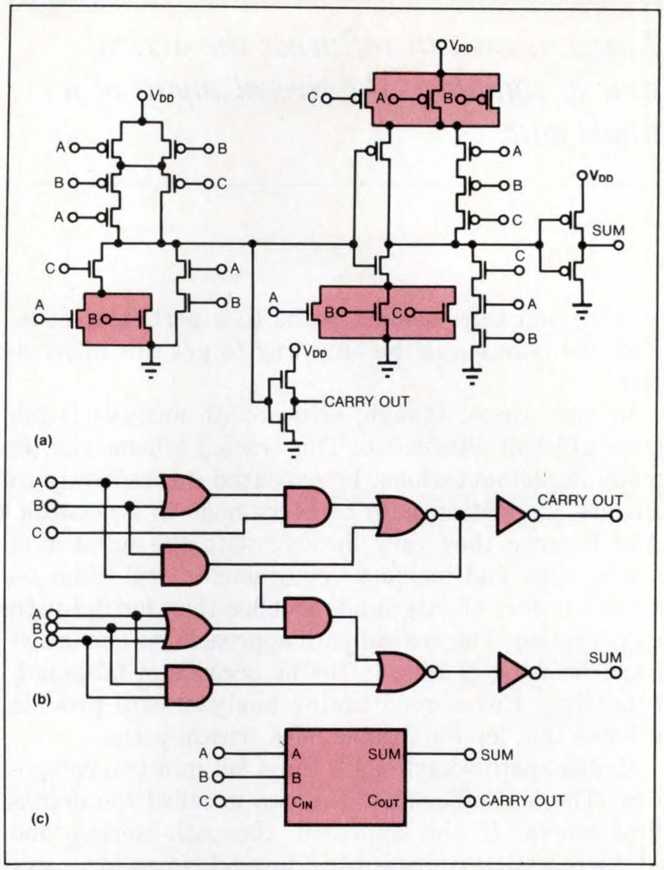



***Fig 3—Timing analysis may be conducted** on three different levels in any circuit: transistor-level **(a)**, gate-level **(b)**, and block-level **(c)**.*

a path. A static timing analyzer provides all this information quickly and automatically without requiring you to supply input vectors.

In addition to choosing between static and dynamic timing analysis, you must choose among several modeling levels when implementing timing analysis. **Fig 3** shows the circuit of **Fig 2** as it appears to a timing analyzer operating on each of three useful levels of analysis: transistor, gate, and block levels.

Analysis on the transistor level **(Fig 3a)** yields highly accurate timing information, but such thorough analysis can be slow. And if the circuit in question uses bidirectional transistors, you may need to devote additional time to manually providing directionality information. Without such input, the transistor-level timing analyzer may stall in endless loops caused by directional ambiguity.

When a transistor-level model is the only circuit model available, or when the need for high accuracy justifies the added input and CPU time, transistor-level analysis is the mode to choose. If you routinely generate full geometry in designing circuits, you might want to purchase an extractor to draw accurate transistor-level models directly from your design. In this case, transistor-level analysis is relatively efficient.

**Design and analyze at the same level**

Often, however, designers work on the gate level from the outset. In these cases, gate-level analysis **(Fig 3b)** is preferable. This approach relies on standard gate-level delay models rather than on transistor representations. Because each gate typically comprises four or five transistors, gate-level analysis is significantly faster than transistor-level analysis. But with some gate-level analyzers, in order to approach the accuracy of transistor-level analysis, you have to spend time calibrating delay models. Gate-level timing analysis eliminates the directionality problems common to the transistor-level approach.

Some timing analyzers permit analysis on an even higher level. The block-level approach **(Fig 3c)** fully analyzes pin-to-pin delays for any specified path. This approach is perhaps most useful in conjunction with gate-level analysis or in analysis of large functional blocks (such as RAMs and ROMs) that do not lend themselves to gate-level implementations. You might also use block-level analysis to accelerate your timing-analysis cycle or to describe the timing of a block not yet implemented.

A final consideration important to implementing a timing-analysis routine has to do with the way the timing analyzer traces through the net list. Here you have two primary choices: full path enumeration, which traces every path through a design, or critical-path analysis, which searches for and identifies only the fastest and slowest paths converging at a node. The latter method is sometimes called "block-oriented" analysis.

Full path enumeration provides comprehensive information about every path and delay in a circuit. You can run it forward from a specified input or backward from a chosen output. However, some problems make this approach impractical for many applications. In large designs, so many paths exist that full enumeration requires too much CPU time and memory—and these requirements increase exponentially with the number of nodes. Also, this approach is so thorough that it frequently reports superfluous information; many paths that might be identical from your viewpoint will be enumerated and flagged. For instance, if your design includes a 32×32-bit register file to which a bit may be written in any location, full enumeration would nonetheless report on all 1024 equivalent paths—although some timing analyzers do sort through and eliminate such redundancies **(Ref 2)**.

For these reasons, full enumeration is not always justifiable, though at times the comprehensive output it provides may prove worth the time and memory required. For instance, in the course of optimizing the speed of your design, it may help you to know the

*Many delays can influence the arrival time of signals at the several inputs of a single gate.*

second- and third-slowest paths to a particular node. Full enumeration is the only way to get this information.

In most cases, though, critical-path analysis is the more efficient alternative. This tracing scheme can, in many implementations, be executed interactively to analyze the critical path to every node in a network. And because they vary linearly with the number of nodes, time and memory requirements will often be several orders of magnitude smaller than for full-path enumeration. The critical-path approach has one drawback: masking of relevant paths because of false-path reporting. But a good timing analyzer will provide utilities that let you disable false critical paths.

Critical-path search algorithms fall into two categories. The less efficient of the two is called the depth-first search. In this approach, the path-exercise and -determination routine runs several times for every node with multiple fan-ins or fan-outs. For instance, signal A occurs before signal B in the circuit shown in **Fig 4.** A depth-first search of this circuit would process signal E once when A occurs and again when B occurs. It's not difficult to see that this repeated application of the delay-modeling routine is inefficient.

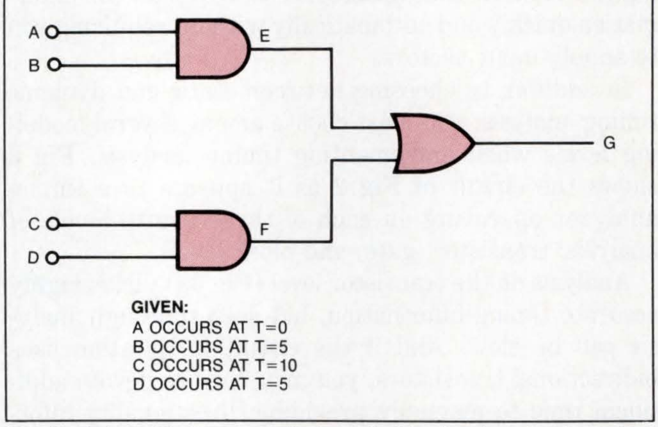



***Fig 4—A breadth-first search** through this circuit waits for both A and B to occur before processing signal E. A depth-first search processes signal E twice: once when A occurs, and again when B occurs.*

### Breadth-first searches wait for all inputs

The alternative is the breadth-first search, in which the analyzer's application of the delay-modeling routine waits for all inputs to arrive before processing a given block. A breadth-first search applied to the circuit in **Fig 4** would wait to process signal E until both A and B had arrived at the node.

So breadth-first searching is more efficient than depth-first. However, the depth-first search does make it easier to detect and prune feedback loops as you scan, because the loops appear when you first process a block; the breadth-first search requires that you wait until multiple signals arrive at a node. This aspect of choosing a tracing method is most important for circuits with many static latches, because a pure breadth-first approach will not effectively break loops with multiple entry and exit points **(Ref 2).**

To summarize, then, the following questions and considerations are relevant to the selection of a timing-analysis tool:

- Which method of timing analysis is best, dynamic timing analysis or static timing analysis?

When answering this question, you will want to consider the timing-error-detection capability of existing simulation tools, the availability of adequate structural and functional delay models, the time available for the timing-analysis cycle, and your need for state-dependent timing information and path information.

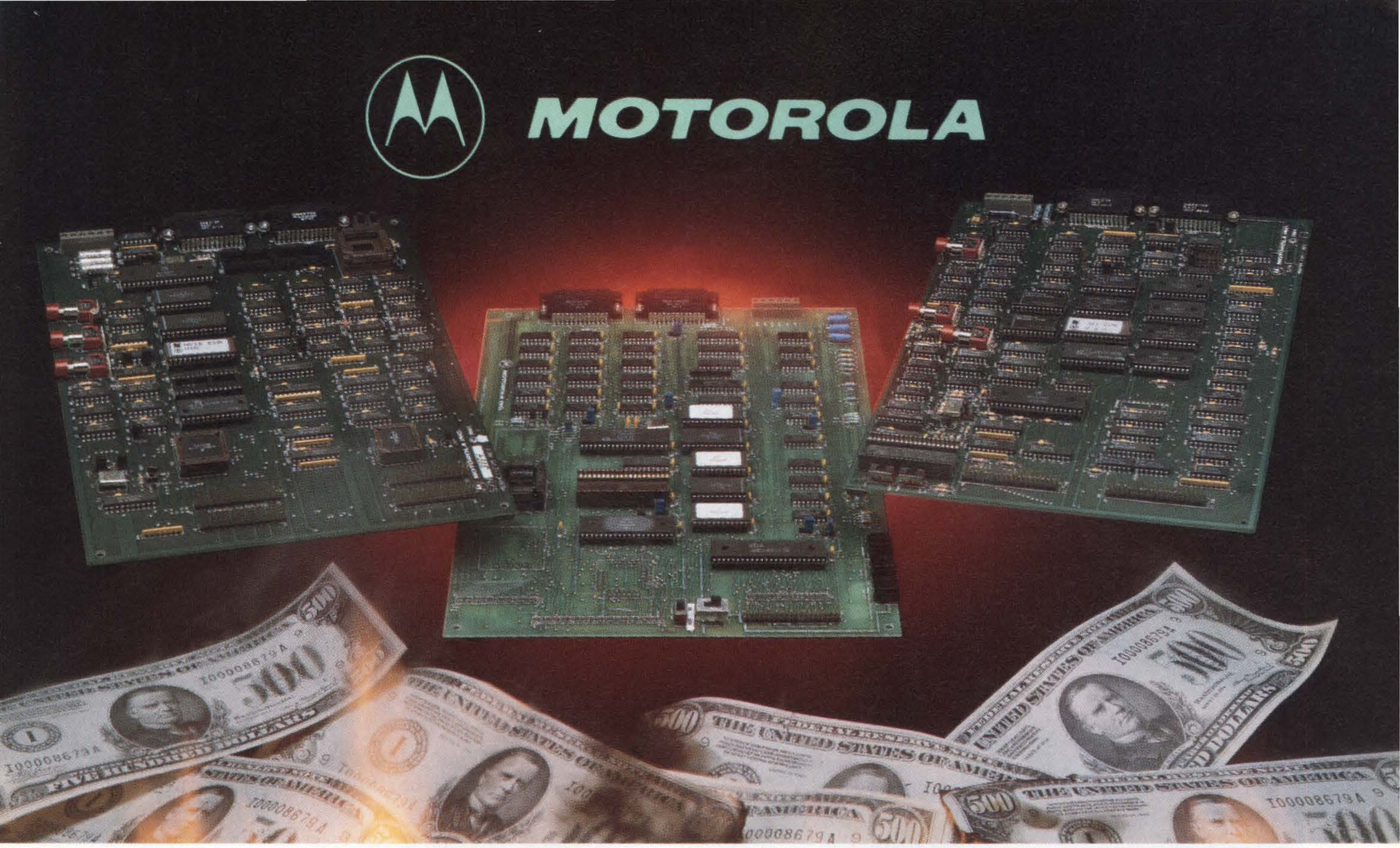
Your decision will depend primarily on your environment. Unless you routinely work with fairly simple circuit designs and have much time for modeling, input, and multiple runs, static timing analysis is usually preferable.

- What circuit levels will you routinely analyze—transistor-level, gate-level, or block-level?

Here, you must consider the time investment required for accurate transistor-level analysis, whether you need full chip analysis, and the availability of appropriate gate-delay models. Mixed-level automated analyzers provide the greatest flexibility. In general, gate-level analysis will probably prove most useful in the widest range of situations—particularly when well-calibrated gate-level models are available. The transistor- and block-level approaches offer particular advantages in certain environments: the former when an extractor or switch-level models are available, the latter when a top-down analysis is desirable.

- What tracing algorithms do the timing-analysis tools you're considering offer—path enumeration, critical-path analysis with a depth-first search routine, or critical-path analysis with breadth-first search routine?

Which algorithm is best for your application depends on the available time and memory, on whether you need information on every path, and on whether you need best/worst case information. The two methods of critical-path analysis provide good best- *and* worst-case information with reasonable run times. Although high-


MOTOROLA

ly time and CPU intensive, full-path enumeration proves useful when you require comprehensive information about paths and delays. (When you use critical-path methods, guard against the masking caused by false-path reporting.)

You needn't deal with all of these considerations before purchasing an automated timing-analysis tool. A good timing analyzer will provide the necessary operational features and modeling libraries so that you can address at least some of the questions and considerations on a design-by-design basis. **EDN**

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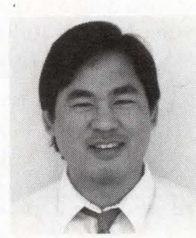
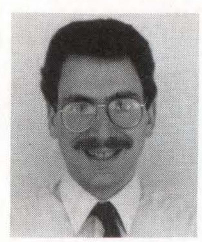
## Authors' biographies



*Dennis Hara is manager for module development/verification tools at Seattle Silicon Corp in Bellevue, WA. In this job, he oversees development of timing analyzers and simulation models. He is also responsible for compiler-development tools. He holds a BSEE from the University of Hawaii and an MS in Computer Science from the University of Washington. Before joining Seattle Silicon three years ago, he worked for Boeing Aerospace Co.*



*Jeffrey Stone is a senior software engineer responsible for software development at Seattle Silicon. He holds a BS in Engineering from the University of Illinois at Chicago. He joined Seattle Silicon four years ago; before that he worked at GTE Business Communications Systems in Northlake, IL.*

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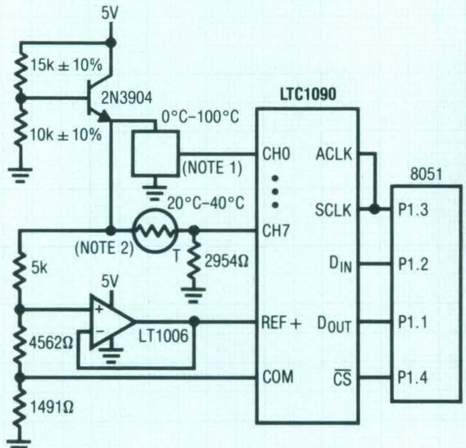


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**CIRCLE NO 69**

# DESIGN IDEAS

EDITED BY TARLTON FLEMING

## Circuit screens narrow pulse widths

Irwin Cohen
*Hewlett-Packard, Rockaway, NJ*

The **Fig 1** circuit passes a pulse from $V_{IN}$ (A) to $V_{OUT}$ (B) only if the pulse duration exceeds a minimum value, determined by R and C. The minimum values for positive and negative pulses ($t_P$, $t_N$) differ somewhat:

$$t_N = RC\ln\left(\frac{V_L}{5}\right)$$
$$t_P = RC\ln\left(\frac{5-V_H}{5}\right).$$

Based on the states of A and B, the dual 2- to 4-line decoder ($IC_1$) delivers control signals to the bases of $Q_1$ and $Q_2$. (The #1 decoder operates as a simple inverter; if necessary, you can substitute an inverter such as a ⅙74HC14.)

If A is low, for example, then B is high, $Q_1$ is cut off, and $Q_2$ is saturated. When the arrival of a positive pulse drives A high, $Q_2$ cuts off almost immediately, allowing C to charge through R. If A goes low before node X crosses $IC_2$'s switching threshold (meaning the pulse is too narrow), $Q_2$ turns on and discharges C—the circuit then waits for the next pulse. Otherwise, B goes low and $Q_1$ turns on, quickly pulling X to the level of A, and allowing the B output to emit an approximate replica of the pulse.

When A is high and B is low, a sequence similar to the above enables the circuit to screen negative-going pulses. In either case, the R value should conduct much less current than that in the collector of either transistor. Note that the Schmitt-trigger thresholds of $IC_2$ are not symmetrical with respect to 5V and ground, which results in different values for $t_N$ and $t_P$. You can, however, make these values equal by using an analog comparator to construct a symmetrical-threshold Schmitt trigger. Further, you can achieve independent control of $t_N$ and $t_P$ by introducing an analog switch to select the value for R. **EDN**

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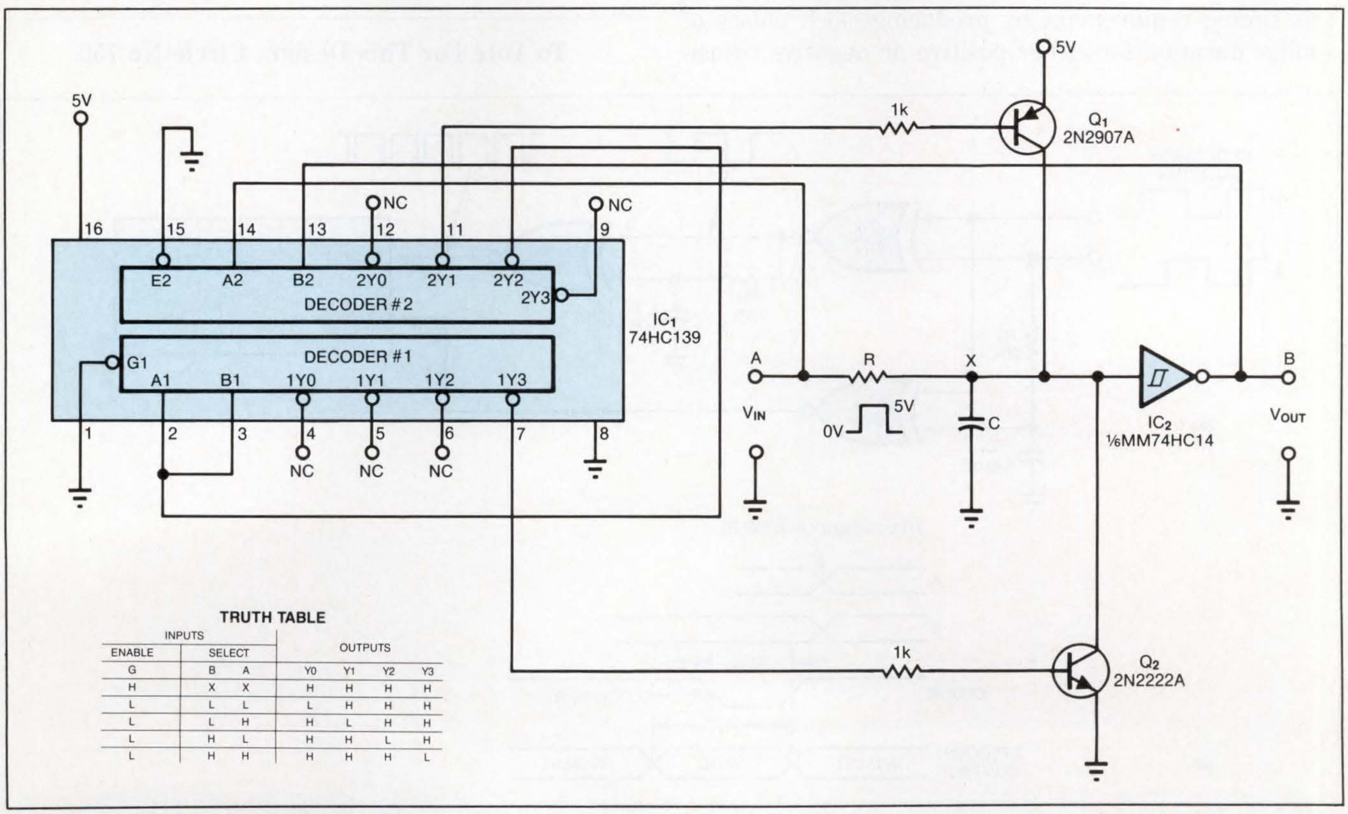


| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| ENABLE | SELECT | | | | | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
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*Fig 1—**This circuit monitors** the digital input $V_{IN}$, blocking any pulse interval (high or low) whose duration is less than the interval set by R and C.*

# Tachometer circuit reduces parts count

William McClelland
*Stahl Research, Port Chester, NY*

The tachometer circuit of **Fig 1** requires only one IC (besides the counter), yet it achieves the same resolution and eliminates backlash just as the 3-IC circuit of an earlier Design Idea did ("Improved tachometer eliminates backlash," March 31, 1987, pg 210).

A standard shaft encoder's A and B ports generate square waves with the same frequency as the shaft turns. The phase of A will lead or lag that of B by 90°, depending on the direction of rotation. To obtain maximum resolution, the tachometer circuit must count every change of state for the A and B signals. Each such change causes a change of state at $IC_{1A}$'s output, followed by a 1-μsec negative pulse at the output of $IC_{1C}$. These clock pulses' positive (trailing) edges cause the counter to count up or down according to the direction of shaft rotation.

You should set the $R_1C_1$ time constant such that it is approximately twice that of the $R_2C_2$ product, to ensure adequate setup and hold times for the up/down signal with respect to the positive clock edges. $IC_{1C}$ supports this timing requirement by producing clock pulses of similar duration for either positive or negative transitions from $IC_{1A}$.

The exclusive-NOR logic of $IC_{1B}$ generates the correct polarity of the up/down signal when necessary—at the positive clock edges—by combining the A value with the B value just prior to a transition of either A or B. $C_1$ provides memory by storing the B value voltage for about 2 μsec. (To understand this single-gate encoding, note that, because the phase relationship of B and A is + or −90°, adding −90° to B makes the phase difference 0 or −180°, depending on the direction of rotation. Therefore, an exclusive-NOR operation on A and a phase-shifted B produces a logic 1 when the inputs are in phase, or a logic 0 when they are 180° out of phase.)

If necessary, you can invert the up/down signal's polarity by swapping the A and B connections or by using a fourth X-NOR gate as a selectable inverter buffer. To invert the clock signal, substitute identical-pinout, X-OR gates (4070s) for the 4077 X-NOR gates. And if necessary to guarantee standard CMOS rise and fall times, you should buffer the A and B signals with Schmitt-trigger gates such as 74C914s. The maximum frequency for A or B is approximately $(4R_1C_1)^{-1}$. **EDN**

**To Vote For This Design, Circle No 750**

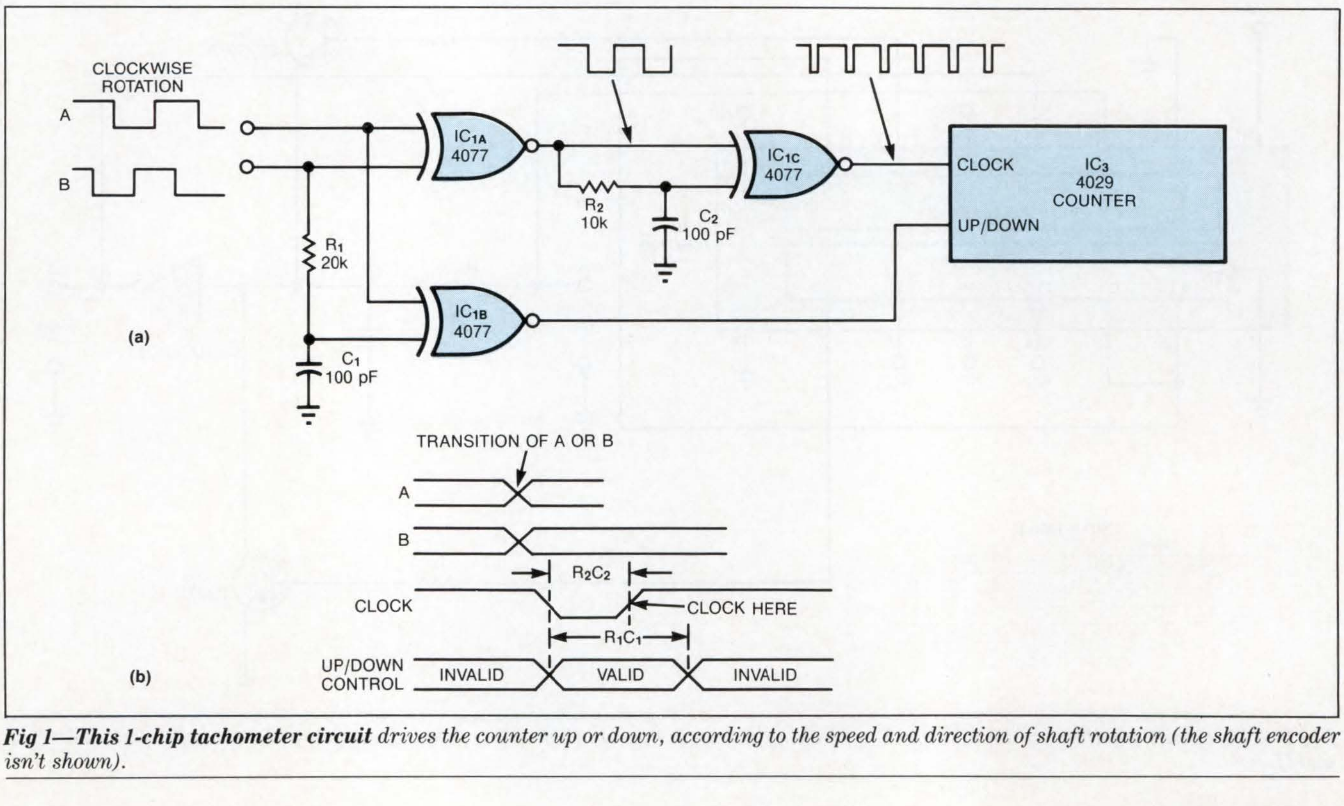


***Fig 1—This 1-chip tachometer circuit** drives the counter up or down, according to the speed and direction of shaft rotation (the shaft encoder isn't shown).*

# Circuit doubles digital frequency

John R French
*Singer Co, Wayne, NJ*

The circuit in **Fig 1** doubles the frequency of a digital signal by operating on both signal edges. Each transition causes the exclusive-OR gate, $IC_1$, to produce a pulse, which clocks flip-flop $IC_3$ after propagating through buffers $IC_{2C}$ and $IC_{2B}$. If you remove capacitor $C_1$, the circuit produces narrow output pulses. By including $C_1$, you can obtain a desired duty cycle for a given input frequency $f_{IN}$. The $C_1$ value for an approximate 50% duty cycle is

$$C_1=\frac{1}{2R_1f_{IN}}.$$

When $f_{IN}$=1 MHz, for example,

$$C_1=\frac{1}{2\times2400\times10^6}=208\text{ pF}.$$

Gate delays limit the maximum output frequency, $f_{LIMIT}$:

$$f_{LIMIT}=\frac{1}{tplh_{IC_1}+tplh_{IC_{2A}}+tplh_{IC_3}+tphl_{IC_1}}$$
$$=\frac{1}{(23+25+100+22)\times10^{-9}}$$
$$=5.8\text{ MHz.}$$

EDN

**To Vote For This Design, Circle No 747**

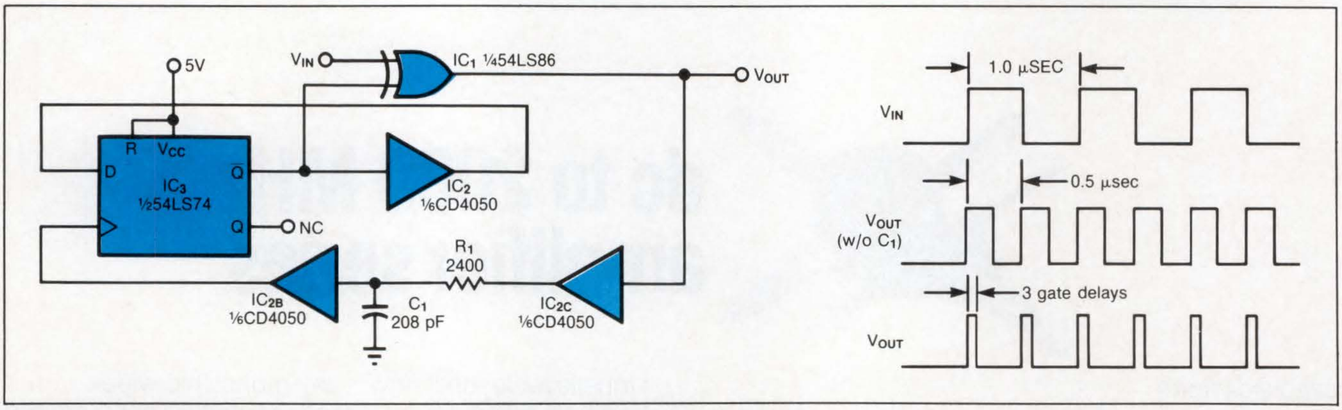


*Fig 1—**This circuit doubles** the frequency of $V_{IN}$ for inputs as high as 5.8 MHz.*

# Battery-backup circuit offers system reset

Terry Patterson
*Research and Productivity Council, Fredericton, New Brunswick, Canada*

On many microprocessor boards, during power-up a simple RC circuit maintains the reset state until the μP and the power supply have stabilized. When the μP powers down during a brownout, though, these circuits don't provide a reset pulse nor do they protect a battery-backed RAM system from spurious write operations. The **Fig 1** circuit does both.

Comparator $IC_{1A}$ senses the 5V supply voltage according to the threshold you set using $R_1$. A 4.75V threshold, for instance, causes the comparator's output to switch low at that level, discharging $C_1$. The capacitor remains discharged until the supply voltage rises above its upper threshold (4.84V in this case), then begins to recharge; 6 msec later, comparator $IC_{1B}$ pulls the reset line high, producing a minimum 6-msec reset pulse. $IC_{1B}$'s open-collector output allows the μP and

other devices to take control of the reset line as required. $IC_2$ provides a 2.5V reference for the comparator, and $S_1$ gives you manual-reset capability.

The circuit protects the static RAM by pulling its $\overline{CE}$ (chip enable) input high during low-voltage conditions, and by providing a minimum of 2V to the $V_{DD}$ terminal. The 3V lithium battery delivers current (1 μA typ) through a Schottky diode, $D_2$, resulting in the static RAM's $V_{DD}$ being only 0.1V below the system's $V_{CC}$. To reduce power consumption, you should ground the unused $IC_2$ inputs. **EDN**

**To Vote For This Design, Circle No 749**

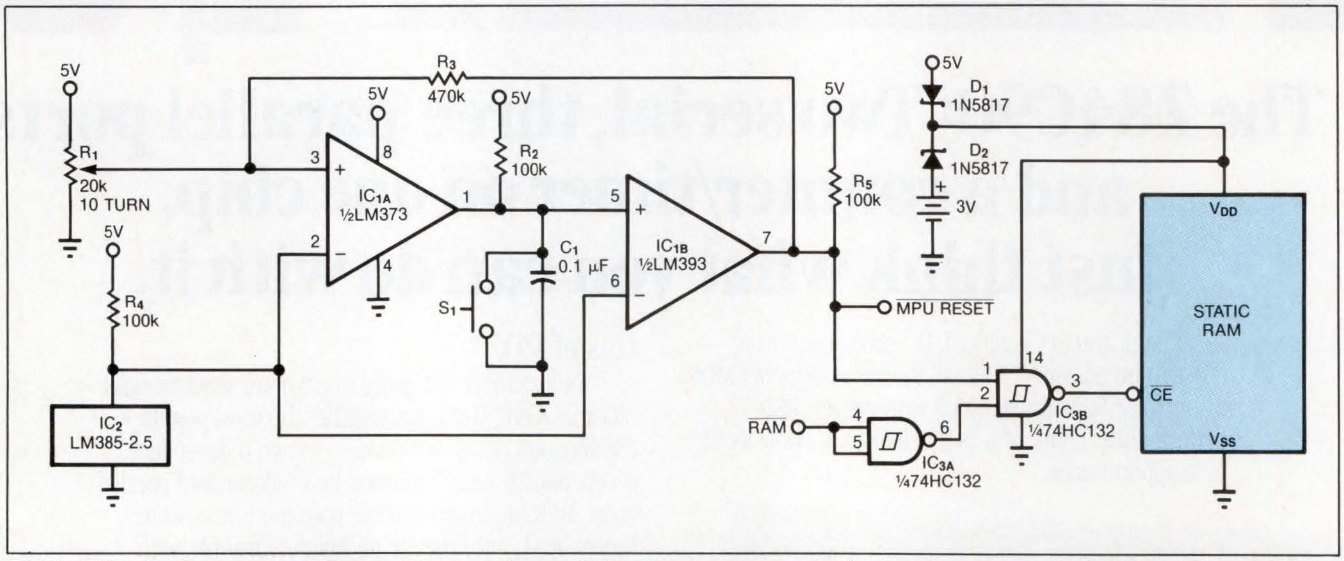


*Fig 1—**This circuit protects a μP system** by asserting a minimum 6-msec reset pulse during power turn-on or brownouts, by providing at least 2V to the static-RAM system, and by deselecting the static RAM to avoid spurious write operations.*

# Timer output has variable duty cycle

George Indorf
*Intronics Inc, Edwardsville, KS*

When configured as a free-running multivibrator, a 555 timer provides no more than a 50% duty cycle. By adding two transistors, however, you can obtain a variable, 5 to 95% duty cycle without changing the sum of the on and off times **(Fig 1)**. When $V_{OUT}$ goes low, $Q_1$ is on and $Q_2$ is off, disconnecting $V^+$ while the timing capacitor ($C_2$) discharges into pin 7 of the timer. When $V_{OUT}$ goes high, $Q_2$ reconnects $V^+$ for recharging $C_2$.

Adjusting the linear trimming potentiometer ($R_3$) to increase the charging resistance increases the on time, but decreases the off time by the same amount by decreasing the discharge resistance (the converse is also true). As a result, the sum of the on and off times remains constant. $R_2$ protects $Q_2$ and the timer against high charge/discharge currents. **EDN**

**To Vote For This Design, Circle No 748**

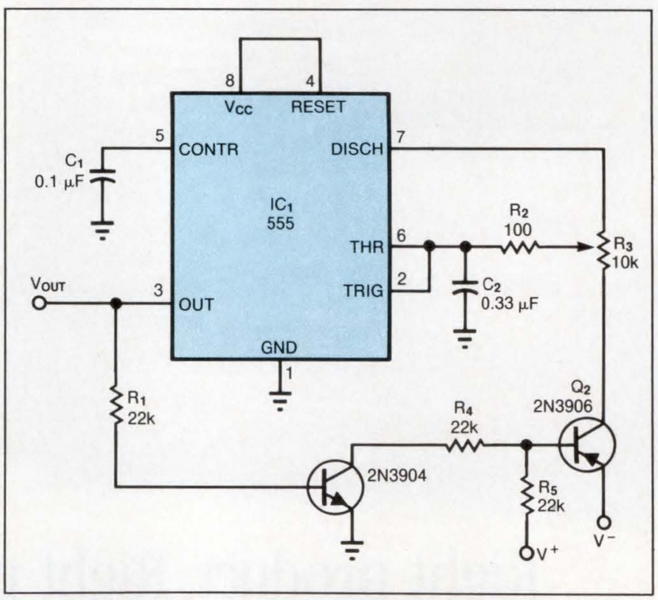


*Fig 1—**Adjusting this circuit's trimming potentiometer, $R_3$,** varies $V_{OUT}$ from 5 to 95% without affecting the $IC_1$'s time constant.*

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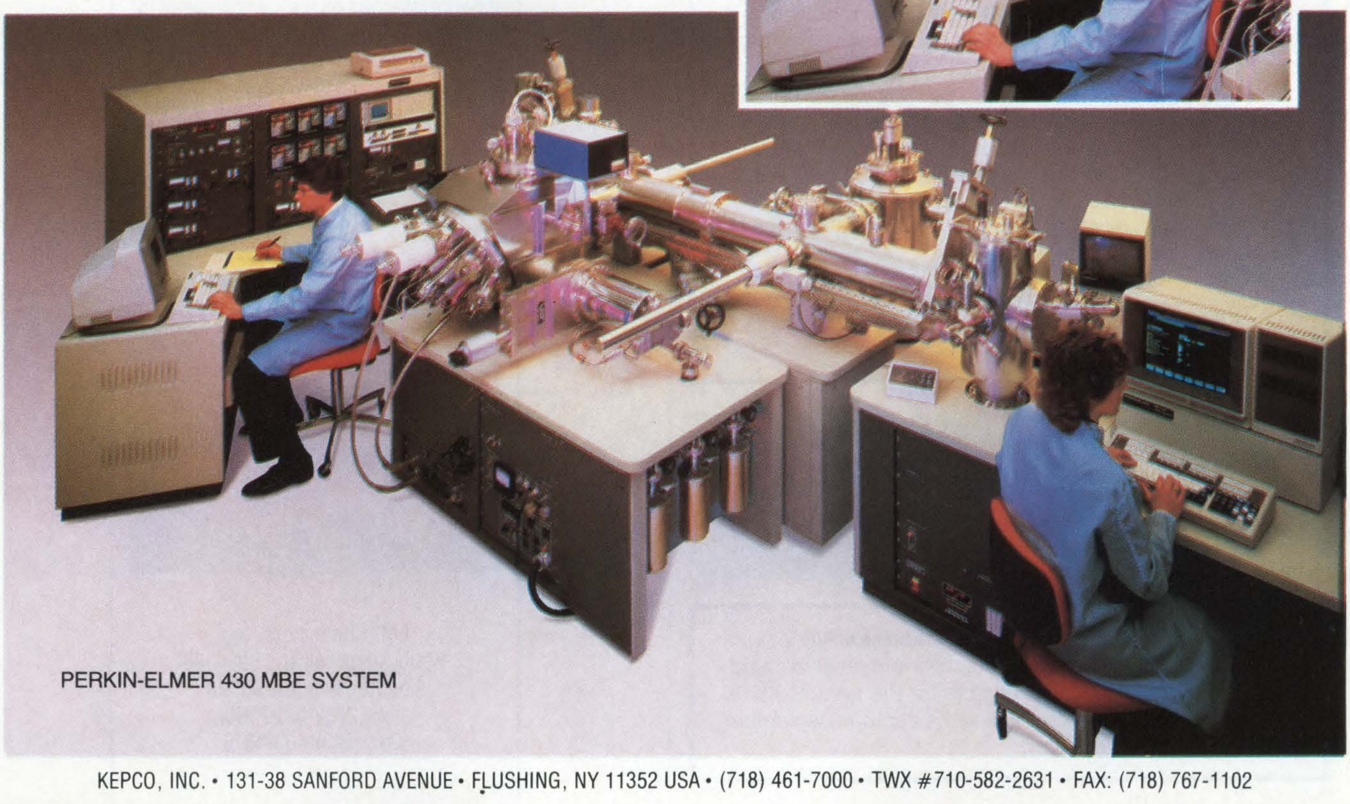

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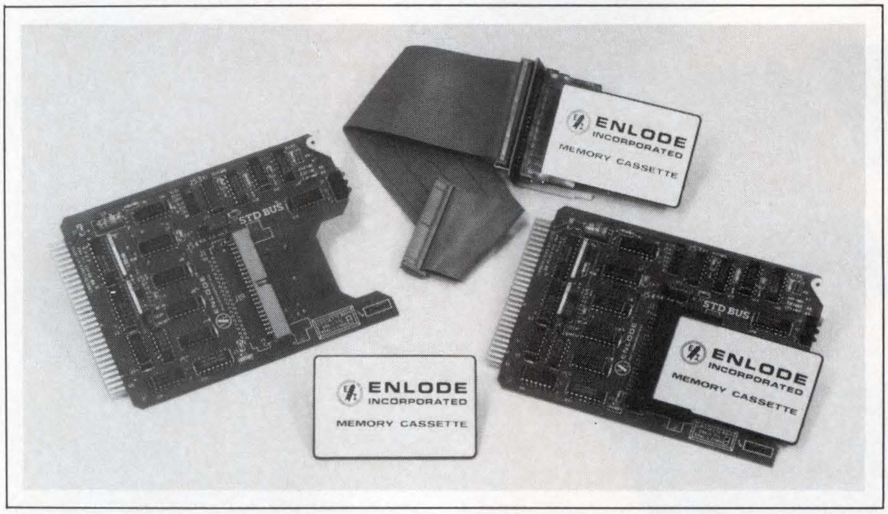
**San Jose, CA 95131-1002**

**CIRCLE NO 76**

## COMPUTERS & PERIPHERALS

### CASSETTE MEMORY

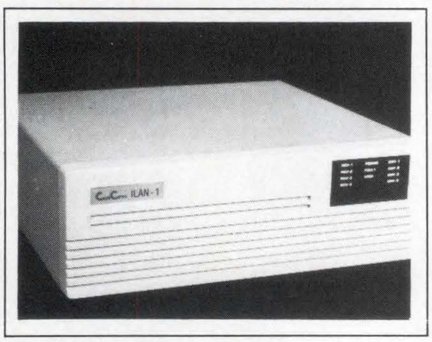
- *Uses a removable RAM cassette*
- *System asynchronously transfers data at 3M bytes/sec*




The 234/334C is a cassette memory system for the STD bus. It comes in two versions. Model 234-1 comes with a TTL bus card; model 334C-1 is the CMOS bus version. You can insert the credit-card size RAM into a socket mounted on the card. The system transfers data asynchronously to the cassette at rates of 3M bytes/sec. The card appears to the host processor as four sequential ports in the I/O map. The board has a counter which holds the current cassette address. Following each read/write from the host, the counter is incremented to the next data location in the cassette. The cassettes have CMOS static RAM, a write-protect switch, and a replaceable lithium battery which provides data retention for three years min. Cassettes have capacities of 64k, 128k, 256k, and 512k bytes. Board, $285. Prices vary for the cassettes according to capacity.

**Enlode Inc,** 1728 Kingsley Ave, Orange Park, FL 32073. Phone (800) 874-7729. TLX 466036.

**Circle No 365**




### LAN CONNECTOR

- *Serves as many as four Ethernet or Starlan networks*
- *System connects ISO, TCP/IP, DECnet, XNS, and TOP*

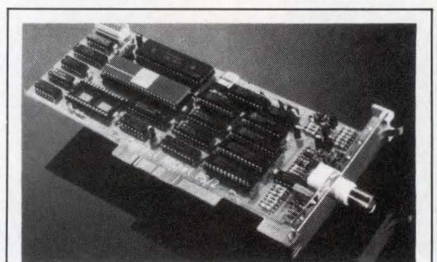
The ILAN-1 networking system can integrate multiple LANs in a single communication network. The basic node system chassis serves as many as four Ethernet or Starlan networks in any combination. Modular interface cards let you accommodate growing or changing network configurations. The system features protocol transparent connectivity allowing ISO, DECnet, TCP/IP, XNS, and TOP protocols to be mixed on any of the interconnected LANs. A plug and play feature automatically determines network-device locations and passes packets from one network to another when necessary. The nodes are cascadable to accommodate large networks and modular software defines the network configuration. Remote network-management software monitors network statistics and security. Prices range from $4575 to $10,850.

**CrossComm,** 133 E Main St, Marlborough, MA 01752. Phone (617) 481-4060.

**Circle No 366**

### NETWORK CARD

- *Allows IBM PS/2 model 50, 60, and 80 to operate under Netware*
- *Board uses the SMC-9026 controller chip*



Micronet is an ArcNet network card for the IBM PS/2 model 50, 60, and 80 computers. The single-slot short card operates under Novell's Netware network operating system. The card utilizes the SMC 9026 controller chip and a custom transceiver with a cable driver. It comes with a floppy disk containing automatic software setup routines for I/O address, interrupt, and memory addresses. It supports up to 7 different I/O port addresses, 7 memory buffer addresses, and 8 interrupt levels. The board connects to RG-62/U or other 93Ω cable through a BNC connector. A high speed cache-buffer arrangement increases the throughput speed. $398.

**C&C/Connect,** Box 280, Batavia, IL 60510. Phone (312) 879-7003.

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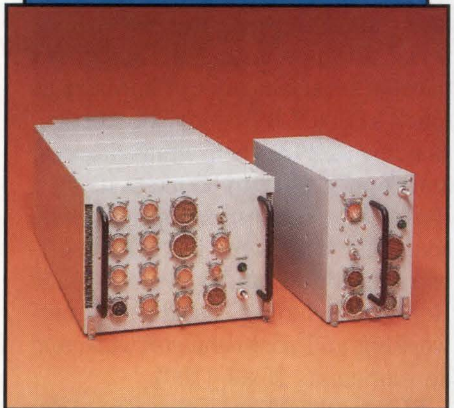

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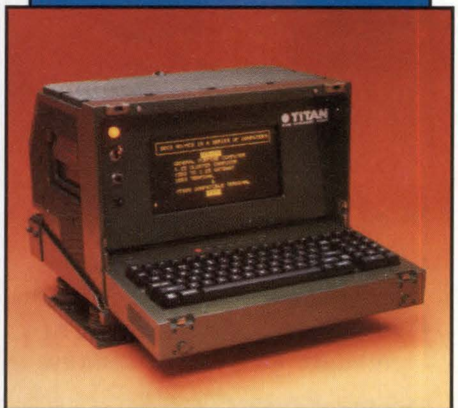

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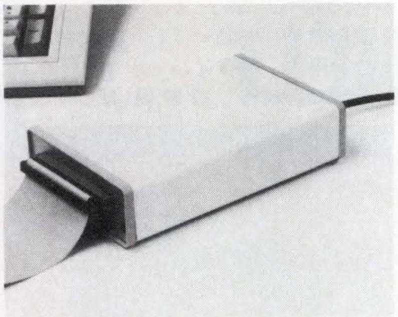


## SCSI EXTENDER

- *Uses coax or fiber optics to increase communication distance*
- *Fiber cable operates full SCSI standard for a 2-mile distance*

The Paraline SCSI bus extender extends the communication distance of the SCSI bus by a distance of more than 2 miles over a single fiber-optic cable or as far as 1000 ft with coaxial cables. An extender is required on each end of a cable run. The product is completely transparent in that the system operates as if connected by the SCSI standard. A Parahub model has one parallel port and four serial ports, which you can use as a node for branch networks. When connected, the system can transmit asynchronous data at 1.5M bytes/sec and synchronous data at 4.5M bytes/sec, which is compliant with the SCSI standard. Coax extender, $395; fiber-optics extender, $820; coax Parahub, $1195; fiber-optics Parahub (available in June), $2625.

**Paralan Group,** CDR Systems Inc, 7171 Ronson Rd, San Diego, CA 92111. Phone (619) 560-1272.

**Circle No 368**

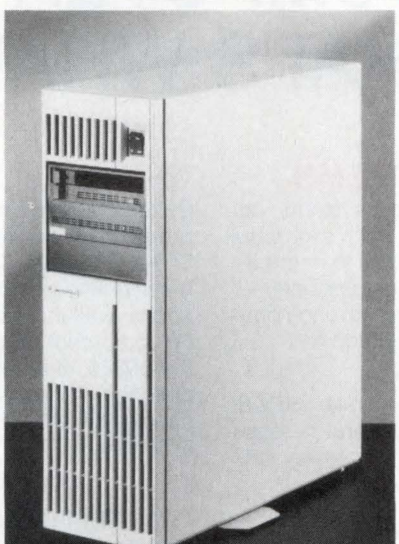
## CPU BOARD

- *Runs Unix and real-time applications*
- *Board uses a 25-MHz 68030 μP and 1M or 4M bytes of RAM*

The HK68/M130 is a single-board computer for Multibus I. The board features a 25-MHz 68030 CPU, 1 or 4M bytes of dynamic RAM with parity, as many as 2M bytes of EPROM, and a 4-channel 32-bit DMA. In addition, the board includes a SCSI interface, four RS-232C serial I/O ports, a 16-bit parallel port, and an 8-bit iSBX connector. It includes 128 bytes of non-volatile RAM, three 16-bit counter/timers, an iLBX memory-expansion port, mailbox interrupt support, and a full master/slave interface to Multibus I. The device's optional features include a 68881 or 68882 floating-point coprocessor and a time-of-day clock with battery back-up. The board runs under Unix System V.3, Ready System's VRTX Real-Time Executive, and Microware's operating systems. Board with 4M bytes of dynamic RAM, $4995.

**Heurikon Corp,** 3201 Latham Dr, Madison, WI 53713. Phone (608) 271-8700. TLX 469532.

**Circle No 369**



## UNIX SYSTEM

- *Operates at 4.5 MIPS using a 20 MHz 68030 μP*
- *VME Bus system supports 20 asynchronous devices*

Model 3300 is a member of the company's VME Delta Series of Unix-based computer systems. The system achieves 4.5 MIPS using a single-board computer with a 20 MHz 68030 μP. The system occupies a single slot in a six-slot VME Bus chassis; the five remaining slots are expansion slots. The board has 4M or 8M bytes of RAM, a 68882 floating-point coprocessor, a SCSI interface, an Ethernet interface, four serial I/O ports, and a Centronics parallel interface. It can support as much as 300M bytes of disk storage, as many as 20 asynchronous devices, and connectivity to 96 users using a DeltaLink controller option. The computer runs a broad base of software products under System V/68 Rel 3 including local-area networking and real-time software and development. $6995 (100).

**Motorola Microcomputer Div,** Marcom Dept-DW283, 2900 S Diablo Way, Tempe, AZ 85282. Phone (800) 556-1234.

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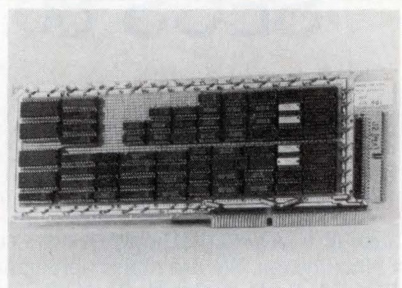


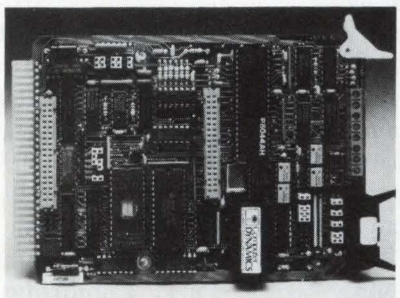
## INTERFACE BOARD

- *Emulates a Gould computer HSDII card for IBM PC/AT*
- *Onboard FIFO allows burst transfer rates of 6.6M bytes/sec*

The PCHSD IBM PC/AT board emulates the functions of a Gould HSDII (high-speed data interface). It provides a high-speed bidirectional link for transferring control, status, and data between the computer and devices that connect to a Gould HSDII. The board can also communicate with an HSDII in a Gould machine. It transfers 16-bit words to and from main PC memory, and 32-bit words to and from the external device. The board can reformat the words by byte swap and word swap. A high-speed FIFO buffer allows burst transfers at 6.6M bytes/sec between the PC and the external device. C subroutines supplied with the board provide the software for writing control, reading status, and reading and writing data. $4675. Delivery, 30 to 60 days ARO.

**Applied Data Sciences Inc,** Box 814209, Dallas TX 75381. Phone (214) 243-0113. TLX 247799.

**Circle No 371**



## BITBUS BOARD

- *Can operate in four modes*
- *As a gateway, it lets STD Bus processors talk to Bitbus*

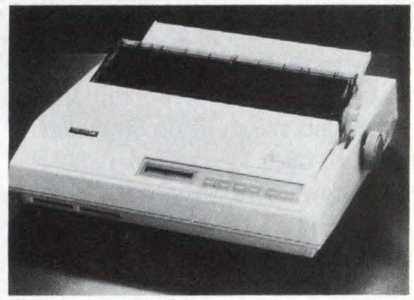
Using Intel's 8044 Bitbus Enhanced μP, the STD-BitBoss STD Bus board provides an interface to the Bitbus and sockets for as many as 64k bytes of EPROM and 40k bytes of RAM or EEPROM. It operates in four different modes. First, it can act as a gateway that allows STD Bus processors to communicate with the Bitbus. Second, it can act as a remote peripheral, responding to input and output commands. Third, programs can be burned into an EPROM on the board through the Bitbus, allowing flexible communications to the host or other nodes in the system. Fourth, it can act as a host CPU for the STD Bus. The board permits transmission at speeds as high as 62.5k bps for a distance of 13.2 km, and as high as 375k bps for a distance of 900m. $300 (OEM qty).

**Computer Dynamics Inc,** 105 S Main St, Greer, SC 29651. Phone (803) 877 8700.

**Circle No 372**

## PRINTER

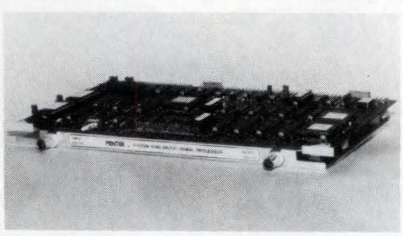
- *Color graphics with 360×360 dot/in. resolution*
- *Prints draft-quality material at a 216-cps rate*



The P321SLC 24-pin dot-matrix printer can produce color graphics at 360×360 dots/in. Besides black, it prints in orange, green, purple, yellow, cyan, magenta, and brown, using a special color ribbon that comes with the printer. The unit prints draft-quality output at 216 cps and letter-quality material at 72 cps. A 16-digit LCD front-panel display allows you to choose from a variety of print modes including font selection, pitch, printer emulation, and four preset printer configurations. The printer has a built-in tractor for fanfold paper, and a fanfold bypass allows you to print on cut-sheet paper without unloading the fanfold paper. The unit contains 32k bytes of resident memory for a print buffer or downloadable fonts. An additional 32k-byte memory card is available as an option. $949.

**Toshiba America Inc,** Information Systems Div, 9740 Irvine Blvd, Irvine, CA 92718. Phone (800) 457-7777.

**Circle No 373**



## DSP SYSTEM

- *Employs three TI TMS320C25 DSP chips for Multibus I*
- *Companion analog I/O board has 16-bit ADCs and DACs*

The System 4080 digital signal processor (DSP) board and a mating analog I/O board are integrated as a module for the Multibus I. The Model 4182 DSP board contains three TMS320C25 DSP chips arranged as a master and two slaves. The master processor runs at 20 MHz, and the two slave processors run at 40 MHz. The master processor has a 32k×16-bit static CMOS RAM, and each slave has an 8k×16-bit static CMOS RAM. The host has access to the board through a 1k×16-bit static dual-port RAM. The board contains two sockets for 8k-byte or 32k-byte EPROMs. The Model 4062 analog I/O board features 16-bit A/D and D/A converters, a 7th-order elliptic antialiasing input filter and an output filter. The conversion rates are programmable to 50 kHz. Model 4182, $5500; Model 4062, $1495.

**Pentek Inc,** 10 Volvo Dr, Rockleigh, NJ 07647. Phone (201) 767-7100.

**Circle No 374**

## MOTHER BOARD

- *Features 12-MHz 80286 for IBM PC/AT and compatibles*
- *1M byte of RAM and EGA graphics capability*

The SBC-286 IBM PC/AT-compatible mother board features a 12-MHz 80286 μP and 1M byte of RAM. It also includes a Western Digital WD37C65 floppy-disk controller that supports both 5¼- and 3½-in. floppy-disk drives, a SCSI interface, EGA graphics capability based on Chips & Technologies devices, a Centronix parallel printer port, and two RS-232C ports. Eight expansion slots provide for future upgrades to OS/2. The board measures 8½×13 in. and comes with a one-year warranty. Board with a custom diagnostic program, $875.

**Logos Computers,** 555 W Lambert Rd, Suite L, Brea, CA 92621. Phone (714) 255-8105.

**Circle No 375**

## SCSI BOARD

- *Operates in Multibus II systems*
- *Provides two independent SCSI bus interfaces*

The TP600 SCSI bus controller board for Multibus II systems features two independent synchronous/asynchronous SCSI bus interfaces, an onboard 68020 μP, and from 1M to 4M bytes of parity-checked dynamic RAM. Separate DMA controllers direct data transfers between the iPSB message-passing coprocessor (MPC) and onboard memory, as well as transfers to and from the SCSI buses. The DMA controller that transfers data between the MPC and onboard memory is configured as a 32-bit controller to maximize iPSB bus throughput. The DMA controller that transfers data to and from the SCSI bus interfaces has a 32-byte buffer that allows it to convert 8-bit SCSI bus data transfers into 32-bit memory transfers. A memory-protection scheme allows you to partition the onboard memory so that you can implement onboard executive programs or a multitasking operating system. You can use the board as a system master in multiprocessing systems or as an intelligent file-manager resource. £3423.

**Tadpole Technology plc,** Titan House, Castle Park, Cambridge CB3 0AY, UK. Phone (0223) 461000. TLX 818152.

**Circle No 376**

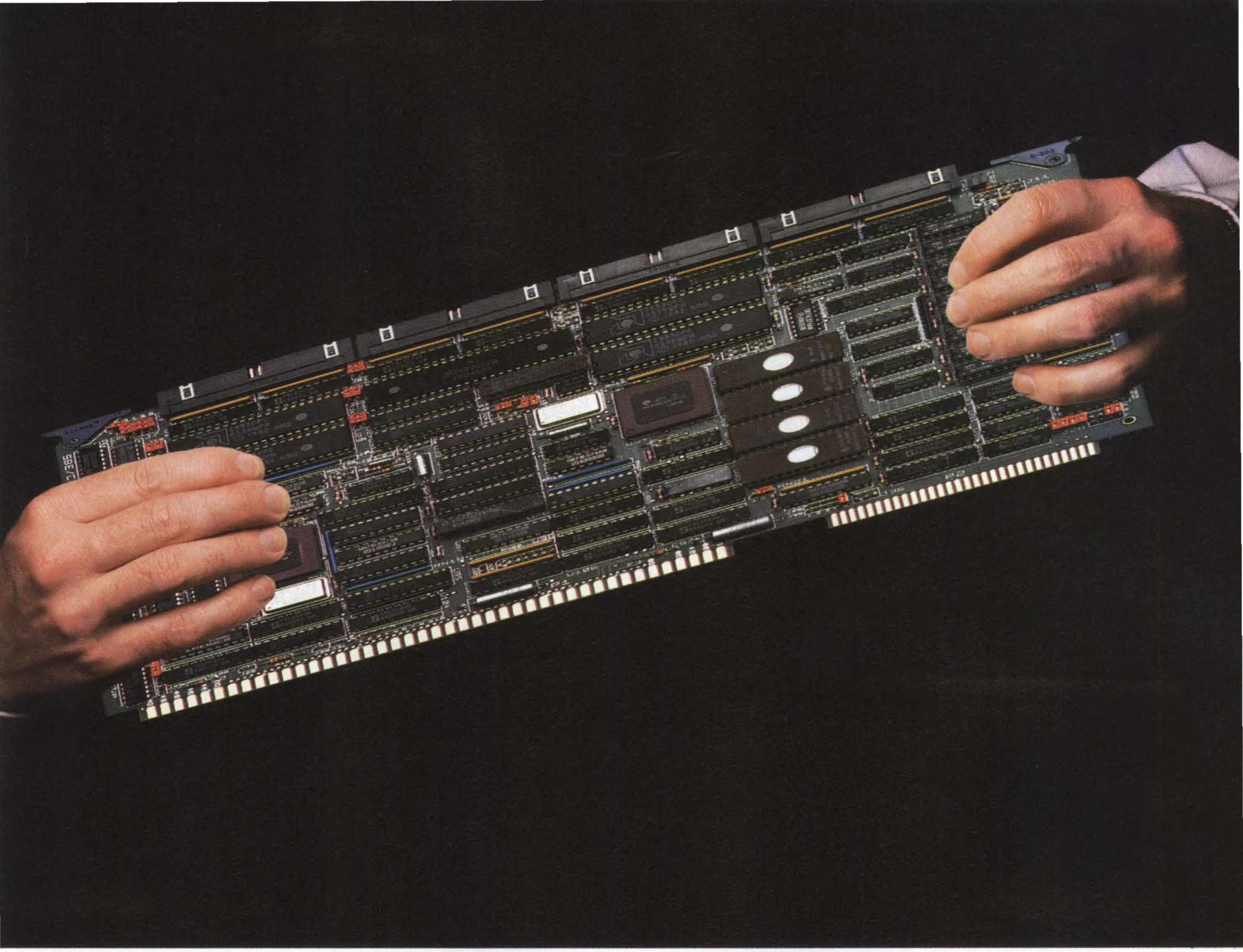
**Tadpole Technology Inc,** 6747 Sierra Ct, Suite K, Dublin, CA 94568. Phone (415) 828-7676.

**Circle No 377**

## INDUSTRIAL NETWORK

- *Provides low-cost networking for process control*
- *Allows point-to-point and broadcast data transfer*

Operating over low-cost 2-wire cabling, the Signatrans-ZM50 modular industrial-networking system allows you to transmit data and commands between as many as 256 network stations. It is suitable for data acquisition and process control, using a range of sensors and actuators. In its simplest mode, by setting DIP switches to allocate the same address to an input channel and an output channel, you can cause the network to automatically transfer data from the input to the output channel. You can set up as many as 128 of these I/O pairs, joining input and output channels anywhere in the network. By using a



handheld programming unit, you can program the system to perform point-to-multipoint transfers, so that the information on one input channel automatically appears at several output channels. As an alternative, you can add a communications processor station on the network, which, in addition to providing a gateway to other networks, provides terminal control of the network. Network topology can be either open ended or in ring configurations, and the network can be as long as 20 km. A typical station, with I/O modules to provide analog and digital I/O capabilities, costs approximately DM 2000.

**Funke & Huster GmbH,** Langemarckstrasse 28, 4300 Essen 1, West Germany. Phone (0201) 22091. TLX 857637.

**Circle No 378**



## 386 EMULATOR

- *Maps ROM contents into overlay memory at 20 MHz*
- *System consists of an in-circuit probe and chassis*

The HyperICE-386 real-time in-circuit emulator lets you develop systems based on Intel's 80386 μP. The system consists of an in-circuit probe and a universal chassis. You can map a system's ROM contents into the unit's 128k bytes of overlay memory in a real-time rate as high as 20 MHz. Only one wait state is necessary for systems operating from 20 to 25 MHz. Three 8000-gate gate arrays provide extensive trigger logic, which can stop the emulator at any point, down to the register level. Transparent tracing records all chip functions as it runs in real time. You can define any combination of address, data, status, and logic probe events as the criteria for a trace. Probes are also available for Motorola's 68000, 68008, and 68010 μPs. From $17,500.

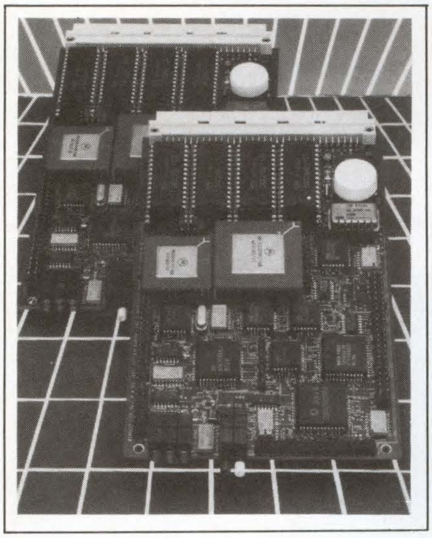
**Microcosm Inc,** 15275 SW Koll Parkway, Beaverton, OR 97006. Phone (503) 626-6100. TLX 759527.

**Circle No 379**

## COMPUTER BOARD

- *Runs a 68020 μP and 68881 math coprocessor*
- *Interfaces with the IIOC bus*

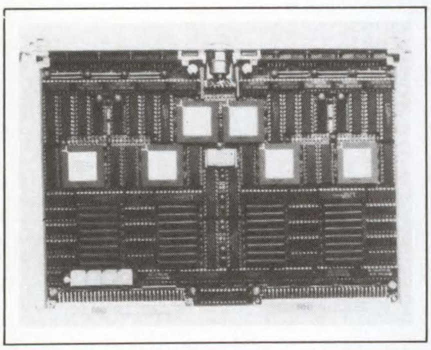
The 10632-E32 single-board computer for the IIOC (Intelligent I/O channel) bus is a low-cost I/O bus for VME Bus systems. By utilizing surface-mount components, the single-Eurocard board houses a 16.7-MHz 68020 μP and 68881 math coprocessor, 512k bytes of zero-wait-state static RAM, four 32-pin EPROM sockets, two serial I/O ports, a 68230 parallel I/O timer, a SASI/



SCSI-compatible I/O port, and a real-time clock/calendar. You can run Microware's OS-9/68020 operating system on the board. DM 2480.

**EKF Elektronik GmbH,** Weidekampstrasse 1A, 4700 Hamm 1, West Germany. Phone (02381) 12630. TLX 828621.

**Circle No 380**



## TRANSPUTER BOARD

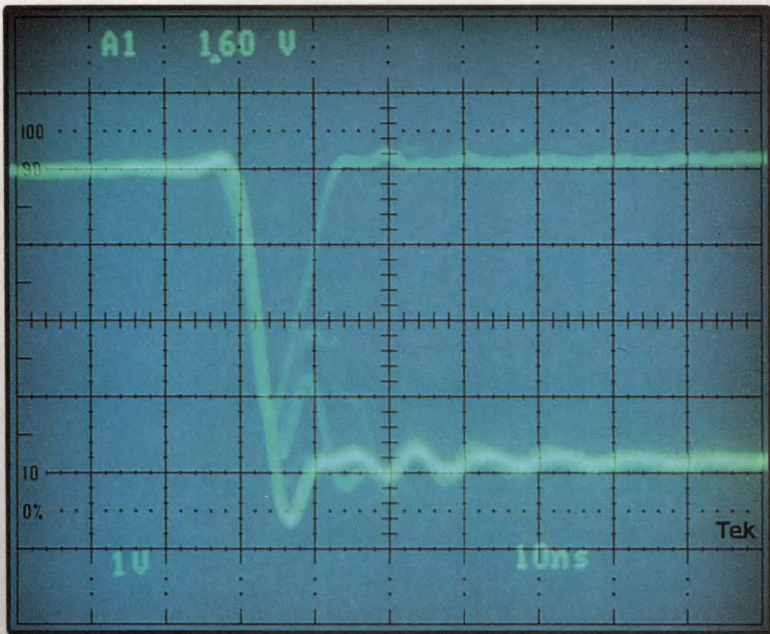
- *Contains 4 32-bit transputer nodes*
- *Board contains 1M byte of RAM for each of the four nodes*

The VMTM module is a double-height Eurocard for the VME Bus that contains 4 transputer processing nodes. Each node is built from a T800 or T414 transputer with 1M byte of local memory. This combination offers up to 40 MIPs and 6M flops of parallel-computing power. The nodes communicate via 16 link-channels at 20M bps each and are configurable under software control using a C004 link switch. You can access the nodes independently from the VME Bus. Four link adapters are address mapped to the VME Bus. You can combine any number of these boards within the VME system using plug connectors. The hardware is supported by Occam and compilers for C, Pascal and Fortran 77. Each board supports as many as four users in a multi-user environment. A Megatool development package is available for all OS-9 systems as well as for Sun workstations running Unix. $8375. Delivery, 4 to 6 weeks ARO.

**Parsytec GmbH,** Juelicher Strasse 338, D-5100 Aachen, Germany. Phone (241) 1822275.

**Circle No 381**

# SINGLE-SHOT PULSES TO 350 MHz



# VISIBLE! ONLY FROM TEK.

Now you can locate elusive glitches, pulses and infrequent events other scopes fail to show—using the 350 MHz Tek 2467 Transient Intensifying Oscilloscope.

faults in normal room light. You don't need a viewing hood. Being able to pinpoint problems this readily makes the critical difference in many troubleshooting situations.

In short, seeing is believing.

### 350 MHz Tek 2467.

The 2467's 4 cm/ns visual writing speed is *100 times faster* than that of any other portable instrument, thanks to Tek's patented microchannel plate CRT.

### What it displays, competitors don't even see.

The result: you see everything that happens in your circuit, whether it occurs once or repetitively. Including asynchronous noise, crosstalk, bus contention, marginal timing, metastability and even the one-in-a-million anomaly.

Because the 2467 specifies *visual* writing speed, not the *photographic* writing speed of other scopes, you can view all faults in normal room light.

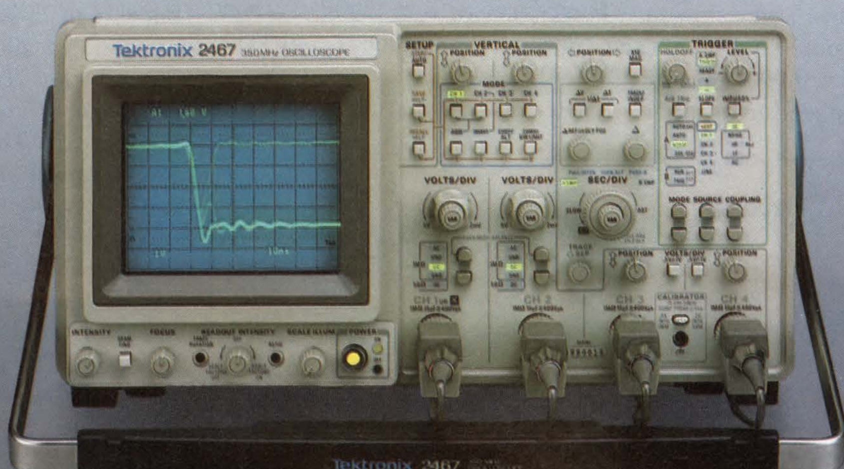
Four independent channels, 500 ps/sec sweep speeds, 1% timing accuracy and 2% vertical accuracy enhance the 2467's problem-solving power.

Built-in automation features help speed your troubleshooting even more and make this one of the easiest scopes to use. It sets up in seconds, for example, at the push of a button.

### A complete measurement package that sets up in seconds.

Ask your Tek representative for a 2467 demonstration—and see just what you've been missing. For additional information, return the reply card or call Tek direct:
**1-800-426-2200.**

### When the measurement counts, count on Tek.

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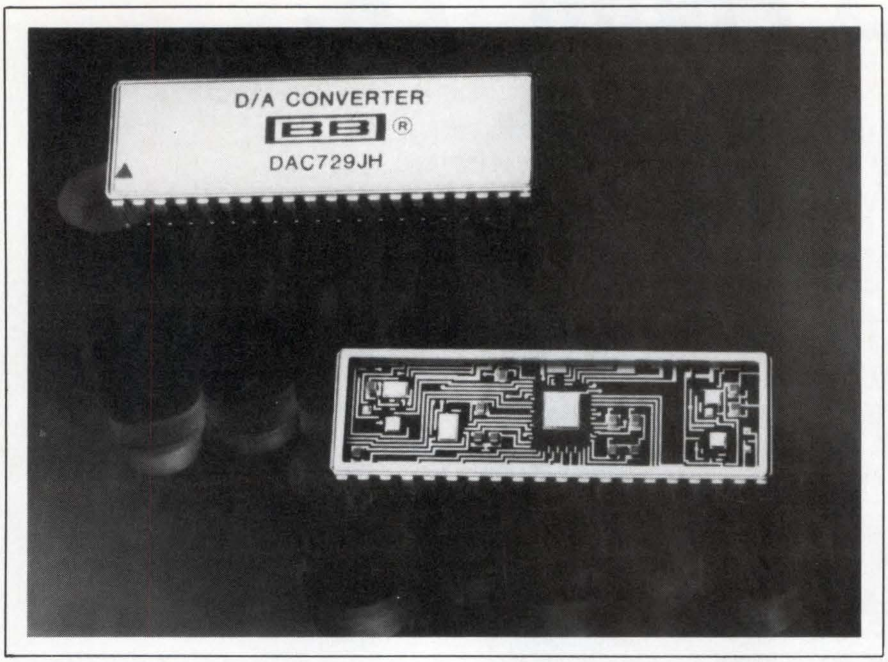
COMMITTED TO EXCELLENCE

**CIRCLE NO 63**

## INTEGRATED CIRCUITS




### 18-BIT DAC

- *Ultra-high resolution*
- *Fast-settling internal op amp*

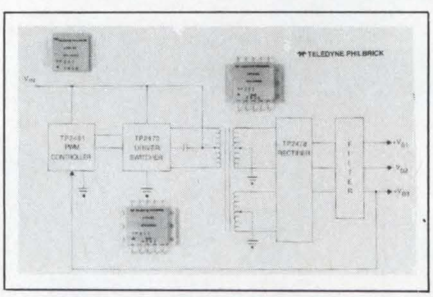
As supplied from the factory, the DAC729 features a guaranteed linearity of 16 bits and is user adjustable to 18-bit linearity. It includes a low-drift 10V reference and a low-drift, low-noise output amplifier. The device settles to ±0.00076% of full-scale range in 8 μsec for a full-scale voltage step, and in 300 nsec for a full-scale current step. The DAC729 is offered in two performance grades and has a specified 0 to 70°C temperature range. The voltage output ranges include ±2.5, ±5 and ±10V. In a 40-pin ceramic DIP, $141 (100).

**Burr-Brown,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

**Circle No 351**

### SMPS POWER HYBRIDS

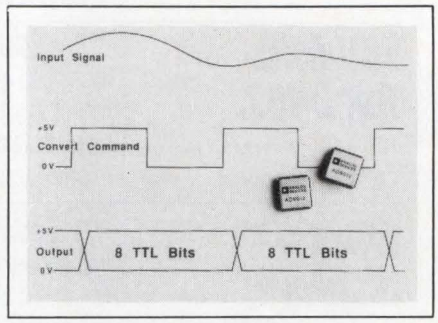
- *MIL-STD-883 3-chip set*
- *Operates to 500 MHz*



With the addition of a transformer, input and output filters, and two capacitors, the 2473, 2478, and 2491 hybrid ICs form a complete switch-mode power supply. The 2491 is a regulating pulse-width modulator that provides all the control functions for a dc/dc converter. Operating at 167 kHz as normally supplied, the factory can modify the 2491 to operate at any frequency from 50 to 500 kHz. The 2473 is a power driver/switcher that includes two 30A FET switches. Configured for a 100W converter, the 2473 is capable of 85% efficiency. The 2478 is a combination full-bridge/half-bridge Schottky rectifier that features a low forward-voltage drop of 0.9V at 20A, and a maximum rating of 40A. The hybrids are specified for operation from −55 to 125°C and meet the requirements of MIL-STD-883B/S. 2473, $443; 2478, $502; 2491, $292 (100).

**Teledyne Philbrick,** 40 Allied Dr, Dedham, MA 02026. Phone (617) 329-1600.

**Circle No 352**




### 8-BIT FLASH ADC

- *180-MHz bandwidth*
- *TTL compatible*

The AD9012 monolithic 8-bit flash A/D converter provides typical word rates of 100 MHz and has TTL-compatible digital outputs. It has a guaranteed minimum encoding rate of 75 MHz, and its 180-MHz bandwidth allows signal-sampling beyond the Nyquist rate without the need of an external track-and-hold circuit. The device features an input capacitance of only 16 pF, thereby reducing the demands on an input buffer. The S/N ratio is >46 dB, and the harmonic suppression is 54 dB from dc to 1.23 MHz. The linearity grades are ±½ LSB and ±¾ LSB. The power consumption is <1.2W. You can order the AD9012 in either a 28-pin DIP or a 28-pin ceramic LCC package. The device is available in both industrial and military temperature grades. From $70 (100).

**Analog Devices,** Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577.

**Circle No 353**

# Sweet 16! (MHz)
## Our new static CMOS 80C286!

## Low power is the icing on the cake.

Now you can have your cake and eat it too: a 16 MHz high-throughput microprocessor with low CMOS power consumption.

Complete compatibility with the NMOS 80286: same pinout, same advanced multitasking architecture, same instruction set, same software. But with 16 MHz performance and a 60% reduction in operating power.

Static CMOS design eliminates trade-offs required by NMOS microprocessors. You get top-end throughput (@ 10, 12.5, or 16 MHz) when you need it or you can stop our 80C286 and put your system into standby without fear of data loss or instruction execution errors. In either case, the Harris 80C286 has the lowest power requirement of any 80286.

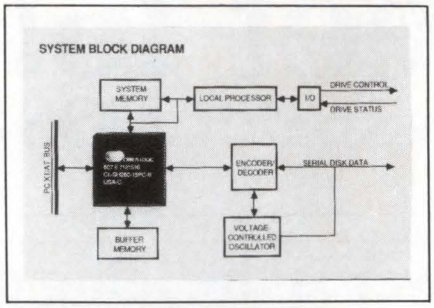
Designed with multitasking in mind, the 80C286 is an exceptional performer in real-time control, portable instrumentation and data acquisition applications. And, coupled with our 80C86, 80C88 and F.O.R.C.E.-based microprocessors for distributed processing, the 80C286 is a great host.

Upgrading your system performance is a piece of cake with our 80C286. Give us a call and join the party. In U.S. phone 1-800-4-HARRIS, Ext. 1286. In Canada, 1-800-344-2444, Ext. 1286.


IN MICROPROCESSORS, THE NAME IS
# HARRIS

Harris Semiconductor: Analog - CMOS Digital
Gallium Arsenide - Semicustom - Custom

HARRIS




## DISK CONTROLLER

- *Interfaces with bus for IBM PC/XT and PC/AT*
- *Integrates three functions*

The CL-SH260 hard-disk controller chip provides a real-time hardware and software interface for the IBM PC/XT, PC/AT, and compatible computers. The device integrates formatter, buffer-manager, and bus-controller functions on a CMOS chip. Designed for computers using an 80286 or 80386 µP, the SH260 can handle NRZ data rates to 24M bits/sec and supports a 1:1 sector interleave on the hard disk. The chip's bus interface includes automatic wait-state generation for compatibility with µPs running at speeds from 6 to 20 MHz. The SH260 is compatible with ST506, ST412, ST412HP, ESDI, and SMD disk interfaces. The chip is packaged in an 84-pin PLCC. $30 (5000).

**Cirrus Logic,** 1463 Centre Pointe Dr, Milpitas, CA 95035. Phone (408) 945-8300. TLX 171918.

**Circle No 354**

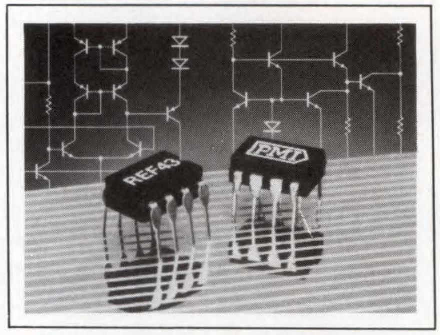
## 32-BIT RISC µP

- *25-MHz operating frequency*
- *4G-byte direct-address space*

Fabricated in standard-cell CMOS, the S-25 RISC (reduced-instruction-set computer) µP can sustain an average processing rate of 15 MIPS at a clock rate of 25 MHz. Using the chip's SPARC (Scalable Processor Architecture) design, it is possible to develop compatible products that increase in performance. The chip also provides a 4G-byte direct-address space and 256 pages of 4G-byte indirect-address space. The majority of S-25 instructions execute in a single cycle. Samples will be available in July, with production scheduled for September 1988. $325 (5000).

**Fujitsu Microelectronics,** 50 Rio Robles, San Jose, CA 95134. Phone (408) 922-9000.

**Circle No 355**




## LOW-POWER REFERENCE

- *2.5V output*
- *1.5-mV tolerance*

The REF-43 low-power precision reference provides a stable 2.5V output that is largely independent of variations in supply voltage, load conditions, and ambient temperature. The reference is suitable for use in 8-, 10- and 12-bit data-acquisition systems, including those operating from a single 5V rail. The REF-43 has an initial output tolerance of 1.5 mV and a thermal drift of <10 ppm/°C. Capable of delivering 10 mA of output current, the REF-43 requires only 450 µA of quiescent supply current. A variety of packages are available. REF-43GP, $3.75 (100).

**Precision Monolithics Inc,** Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222.

**Circle No 356**

## DUAL COMPARATOR

- *2.3-nsec propagation delay*
- *Low power dissipation*

The HCMP96870A ultra-high-speed dual comparator is an improved version of the industry-standard AM6687. The improvements include

# High-Rel ACL Reporting for Duty


## Advanced CMOS Logic is the newest reinforcement in the world's broadest High-Rel CMOS product line.

If you're designing tactical military systems, it's more logical than ever to come to GE Solid State for all your High-Rel logic needs. Because we've just introduced well over 50 ACL logic devices that give you the speed of FAST† plus all the benefits of CMOS. These devices, fully compliant to Mil-Std-883 Rev C, are available in both AC and ACT (TTL-compatible) versions.

## Call toll-free, 800-443-7364 ext. 23

In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

### Reporting for Duty

- Two Hex Inverter/Buffers*
- Three Quad 2-Inputs*
- Three Dual Flip-Flops
- Two 3- to 8- Line Decoder Demultiplexers*
- Two Quad 2-Inputs Multiplexers
- One 4-Bit Full Adder with Fast Carry
- Two 4-Bit Binary Counters
- Two Synch 4-Bit Binary Up-Down Counters
- Two Octal Buffer Line Driver 3-State*
- Two Octal BUS Transceiver 3-State*
- One Quad 2- to 4- Line Data Selector
- One 9-Bit Odd/Even Parity Generator/Checker
- Three Octal Buffer Line Driver 3-State (Inverting)*
- One Octal Transparent Latch 3-State
- One Octal D-Type Flip-Flop 3-State*
- One Octal Transparent Latch 3-State(Inverting)
- One Octal InvertingTransparent Latch 3-State

*Standard Military Drawings available

† FAST is a trademark of Fairchild Semiconductor Corp.

GE Solid State

**_GE/RCA/Intersil Semiconductors_**

Three great brands. One leading-edge company.

*Trademark of General Electric Company, U.S.A.

a shorter propagation delay of 2.3 nsec, faster rise and fall times of 1.2 nsec, reduced hysteresis, and higher input slew rates. The device also features a power dissipation of 250 mW, which is lower than that of competitive devices, according to the manufacturer. It's available in a 16-pin ceramic DIP and a 20-terminal LCC. The operating temperature range is −25 to +85°C. In a 16-pin DIP, $8.49 (100).

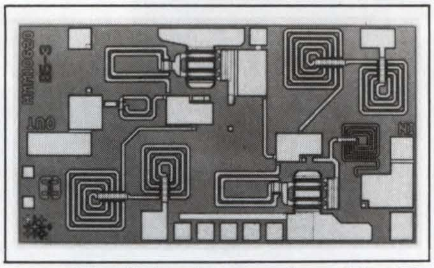
**Honeywell Inc,** 1150 E Cheyenne Mountain Blvd, Colorado Springs, CO 80906. Phone (719) 540-3900.

**Circle No 357**

## 2- TO 6-GHz MMIC

- *Small-signal gain of 11.5 dB*
- *Power output of 13 dBm*

Fabricated in GaAs, the HMM-10620 MMIC (monolithic microwave IC) operates over a frequency range of 2 to 6 GHz with a typical gain of



11.5 dB. Gain flatness is ±0.5 dB. The MMIC includes two GaAs FET gain stages that have negative feedback. At a supply voltage of 8.5V, the typical current drain is only 40 mA. Power output at 1-dB compression is 13 dBm (typ); the noise figure is 5.5 dB (typ). The HMM-10620 is directly cascadable; it does not require external dc-blocking at the RF output port. The chip uses a TiPlAu metallization system and is available screened to MIL-S standards. $50 (1000).

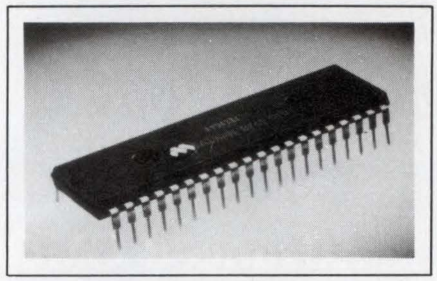
**Harris Microwave Semiconductor,** 1530 McCarthy Blvd, Milpitas, CA 95053. Phone (408) 433-2222.

**Circle No 358**

## LCD DRIVER

- *Handles 32 LCD segments*
- *2000V ESD protection*

Fabricated in CMOS, the AY0438I is a 32-segment liquid-crystal-display (LCD) driver that provides ESD (electrostatic discharge) protection to 2000V. The AY0438I can drive any parallel LCD, whether standard or custom. The driver accommodates 7-, 9-, 14-, or 16-segment characters as well as decimals and positive and negative symbols. To reduce the number of control lines to three, the device uses serial inputs. The AY0438I, which includes



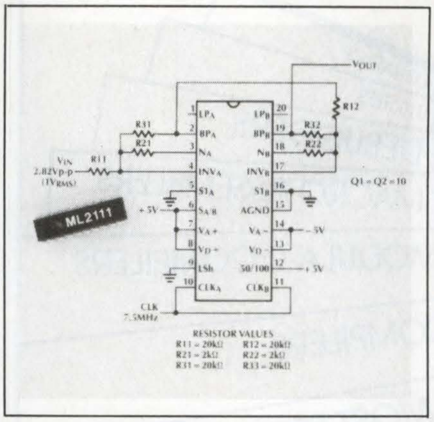
an on-chip oscillator, is compatible with CMOS, NMOS and TTL devices. $2.45 (5000).

**Microchip Technology Inc,** 2355 Chandler Blvd, Chandler, AZ 85224. Phone (602) 963-7373.

**Circle No 359**

## DUAL S/C FILTERS

- *30-kHz and 150-kHz capability*
- *All filter configurations*




The ML2110 and ML2111 switched-capacitor (S/C) filters work at frequencies to 30 kHz and 150 kHz, respectively. Both filters provide bandpass, lowpass, highpass, allpass, and notch outputs. The devices support all filter configurations, including Butterworth, Chebyshev, Bessel, and Cauer. Each unit includes two independent second-order filters on a single chip. You can use each of the independent filters as a first-order or second-order (quadratic) filter. With one ML2110 or ML2111, a user can realize two second-order filters or a single fourth-order filter. The devices differ from each other only in their maximum operating frequency and the product of Q and the center frequency. They operate from ±5V or ±2.5V (the latter voltage provides a reduced frequency capability). Packages include 20-pin DIP and 20-pin SOIC. In a 20-pin DIP, ML2110, $3.75 and ML2111, $6.75; in a 20-pin SOIC, ML2100, $3.85 and ML2111, $7.15 (100).

**Micro Linear Corp,** 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200.

**Circle No 360**

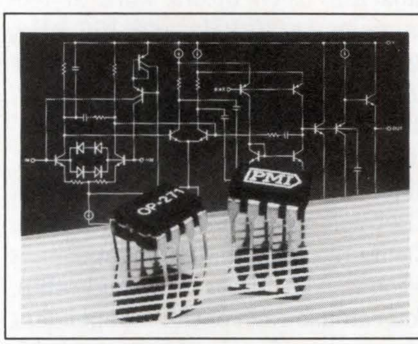
## PBX FILTER CHIP

- *Digital operation*
- *C-Message weighted*

Fully digital in its operation, the S3541 filter chip has a C-Message weighted filter for sounds in the 35-Hz to 4-kHz range, a 35-Hz highpass filter to remove low frequencies, and a 1-kHz notch filter for use within US telephone-system voice- and data-communications channels. It's designed for installation directly on a customer line to remove noise, for line-test instrumentation systems, or in PABX diagnostic sections to monitor line noise. According to the vendor, the chip offers several advantages over comparable analog products, such as freedom from temperature drift, an efficient serial interface, a compact parallel $\mu$P interface, and better accuracy. The device meets all specifications of Bell publication 41009 and IEEE Standard 743. In a 28-pin DIP, $17.95 (1000).

**Gould Inc,** Semiconductor Div, 3800 Homestead Rd, Santa Clara, CA 95051. Phone (408) 246-0330.

**Circle No 361**




## DUAL OP AMP

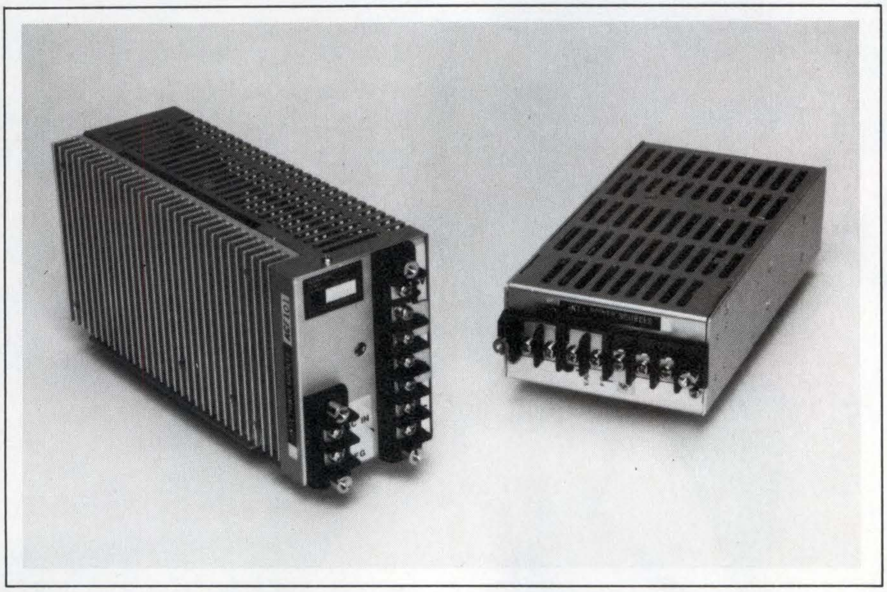
- *5-MHz gain-bandwidth product*
- *Low offset voltage*

The OP-271, a unity-gain-stable dual op amp, features a typical slew rate of 8.5V/$\mu$sec, a settling time to 0.01% of 2 $\mu$sec, and a gain-bandwidth product of 5 MHz. The input offset voltage is 75 $\mu$V typ and 200 $\mu$V max. The open-loop gain exceeds 400,000 and the input bias current of 20 nA minimizes the dc error caused by source resistance. The common-mode rejection is a minimum of 106 dB. Packaged in an 8-pin ceramic DIP, the device conforms to the industry-standard dual op amp pinout and is a pin-compatible upgrade for the TL072, TL082, LF412, and 1458/1558 dual op amps. Industrial grade, $4.50; military grade, $10.50 (100).

**Precision Monolithics Inc,** Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TLX 713719541.

**Circle No 362**

## COMPONENTS & POWER SUPPLIES



### DC/DC CONVERTERS

- *Have efficiency ranges to 90%*
- *Feature adjustable outputs*

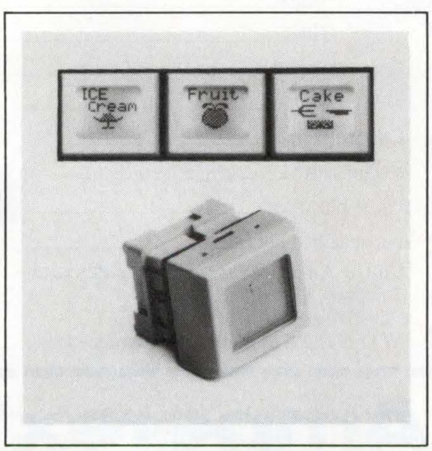
The chassis-mount DCE Series 100W and DCF Series 150W dc/dc converters feature efficiencies as high as 90%. Outputs of 5, 12, 15, and 24V are available from four nominal inputs of 12, 24, 48, and 110V. These convection cooled units are packaged in brushed aluminum cases and are specified for full rated load to 50°C. All models feature adjustable outputs (±10%), input filter, overvoltage protection, and short circuit protection. In addition, the DCF units include remote sense and disable as standard. DCE Series, $129 (OEM qty); DCF Series, $199. Delivery, six to eight weeks ARO.

**International Power Sources Inc,** 10 Cochituate St, Natick, MA 01760. Phone (617) 651-1818.

**Circle No 385**

### SWITCH MODULE

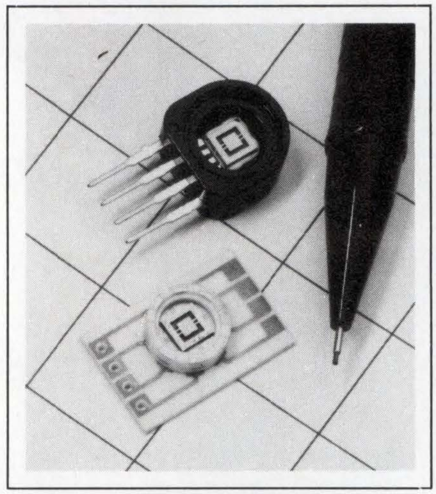
- *Features a 24×36-pixel display matrix*
- *Integrates an LCD and driver into spst switch keycap*




Designed to minimize the man/machine interface problem, this module integrates a low-power LCD, with LED backlighting, and a custom IC driver into the keycap of a spst, momentary-action switch. The super-twist LCD consists of 864 pixels in a 24×36 matrix which provides full screen graphics capability. You can also operate the unit as a 5×7 alphanumeric display and realize three lines of as many as six characters per line. The 0.875×0.75-in. module is designed for through-panel mounting and requires only 0.75 in. behind-the-panel space. It has a 0 to 40°C operating range, 1Ω max contact resistance, and a lifetime spec of one million operations. $40.72 (100).

**IEE Inc,** Component Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311.

**Circle No 386**



### ACCELEROMETER

- *Specified for 12V operation*
- *Has 200g measurement capability*

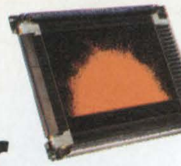
The SXL Series accelerometers employ a 0.16×0.16-in. sensor chip. A special cavity and boss structure are micromachined into each chip and four piezoresistive elements are ion-implanted into each chip to form a wheatstone bridge sensor. The three units in the series have measurement capabilities ranging to 10, 50, or 200g. While the devices are specified for operation at 12V dc, you can operate with any supply between 3 and 15V. Typical full scale outputs are 50 to 100 mV and accuracy is better than 0.1% of full-scale output (FSO). Cross-sensitivity is less than 1% FS output. Standard units are housed in a ceramic package. Other package options are available on request. $57

**Sensym Inc,** 1255 Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-1500.

**Circle No 387**

# ONCE YOU'VE SEEN FUJITSU'S AC PLASMA DISPLAY, YOU'LL TAKE A DIM VIEW OF ANYTHING ELSE.

**CIRCLE NO 93**



The only way our bright new 8050 display looks anything like the others is through a pair of sunglasses.

That's because the 8050 is without a doubt the brightest, most readable display in its class.

It's the first 10-inch, AC-memory, flat panel display to deliver 640 x 400 resolution with an extraordinary 44 foot-lamberts of brightness. Along with a contrast ratio of greater than 20:1. All in a package just over one inch thick.

In fact, the only thing more impressive than these numbers is looking at the display yourself. Then you'll really appreciate its exclusive solid black background. And the brightness and flicker-free clarity of text and graphics.

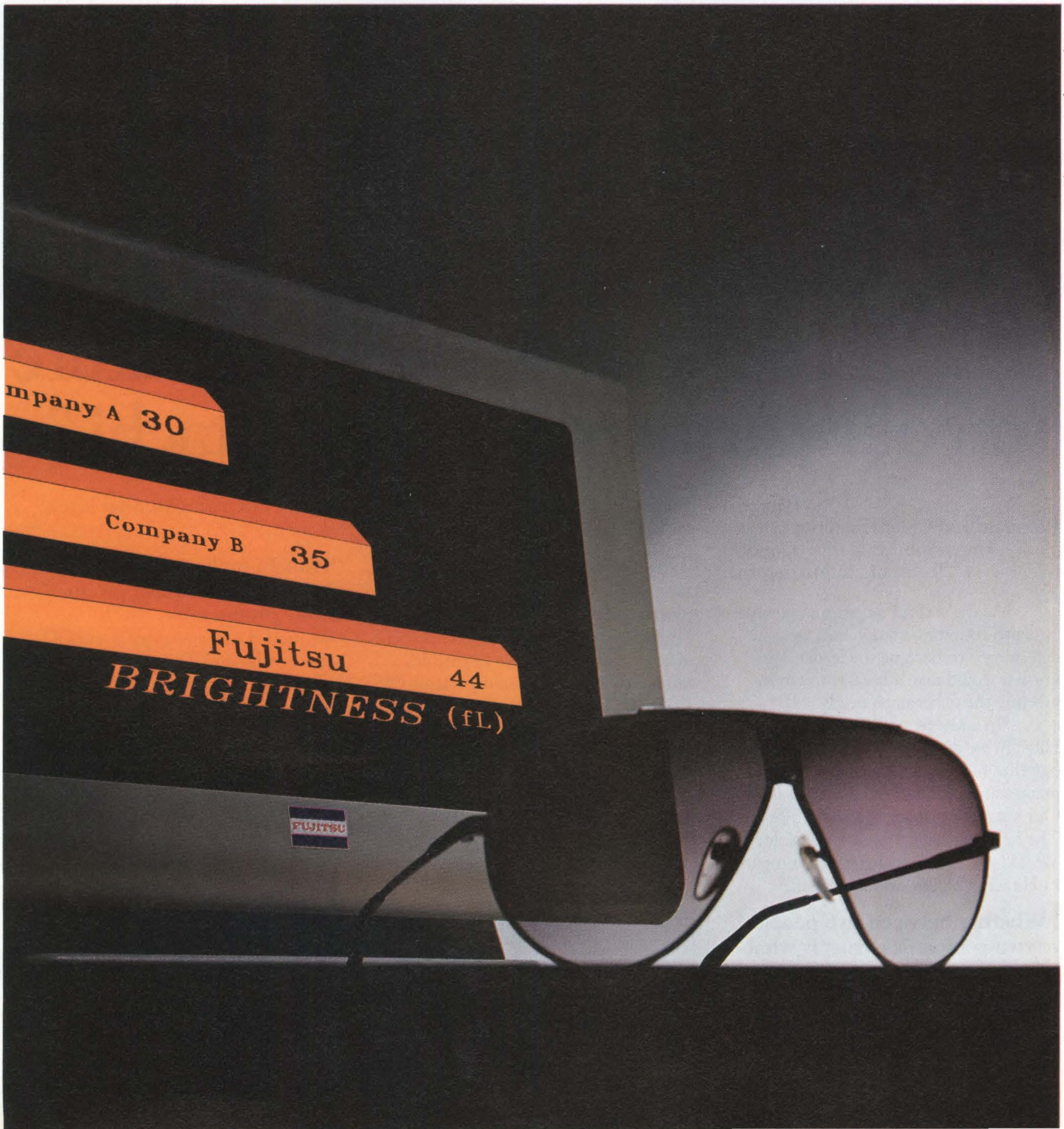
And what's truly amazing is that you'll get this remarkable performance under some of the worst possible conditions. Like bright sunlight. And viewing angles up to 120 degrees.

So if your application calls for the clearest images with maximum contrast, call us today at **1-800-556-1234, Ext. 238.** Inside California call, **1-800-441-2345, Ext. 238.** Or write Fujitsu Component of America, Inc., 3330 Scott Boulevard, Santa Clara, CA 95054-3197.

We'll brighten your day.

FUJITSU
**FUJITSU**
**COMPONENT OF AMERICA, INC.**





# "We bet our entire company's future on our partnership with Hitachi."

**—Jim Balkcom**
**President and Chief Executive Officer**
**Humminbird® Depth Sounders**
**Techsonic Industries, Inc.**

"As the second largest manufacturer of depth-sounding equipment, we were determined to become the leader. We knew it would take a breakthrough in meeting the fisherman's needs.

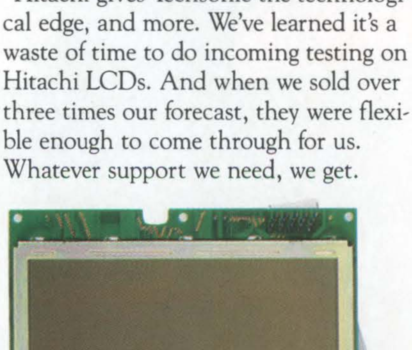
"In strategic partnership with Hitachi, we developed the LCD technology that redefined the depth-sounder market and ultimately quadrupled its size. Our share went from 20 to over 50%. The new technology was a big risk for us. We laid the whole future of our company in Hitachi's hands, and it paid off."

### "Whether between two people, or two companies, trust is what makes partnerships work."

"We've shared technologies, design concepts, marketing plans and other critically confidential information across both sides of the table. That's partnership. Trust makes it work . . . and continue to grow."

### "Hitachi defines quality the same way we do—meeting customers' needs."

"Hitachi gives Techsonic the technological edge, and more. We've learned it's a waste of time to do incoming testing on Hitachi LCDs. And when we sold over three times our forecast, they were flexible enough to come through for us. Whatever support we need, we get.



And the best part is, we never have to ask for it."

### "Hitachi makes it clear that their most important product is our product."

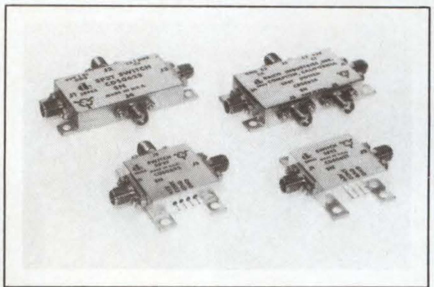
"We needed to team up with an LCD supplier who had the expertise, the capabilities, and the desire to work with us to develop the right solutions. Partnering with Hitachi made Humminbird No. 1, and we're sure it's going to keep us there."

To learn about how partnering with Hitachi can benefit your company, call Tom Klopcic or David Ross at (312) 843-1144. Or write to Hitachi America, Ltd., Electron Tube Division, 300 N. Martingale Road, Suite 600, Schaumburg, IL 60173.

**HITACHI®**

**Hitachi America, Ltd.**
**Electron Tube Division**

**CIRCLE NO 92**



## RF SWITCHES

- *Feature replaceable SMA connectors*
- *−55 to +155°C operating range*

Operating over 20 to 2000 MHz, CDS062X switches handle as much as 14 dBm of RF power over the full military range of −55 to +125°C. All of the switches feature standard replaceable SMA connectors. Each switch features integral TTL drivers, 50Ω terminations, and low power consumption—for example, 12 mA at 5V for the CDS0622. The typical isolation is more than 75 dB at frequencies as high as 1 GHz and 56 dB above 1 GHz. The insertion loss measures 0.9 dB below 1 GHz and 1.4 dB above 1 GHz. The switches are available with optional military screening. CDS0621 spst, $270; CDS0622 spdt, $336; CDS0623 sp3t, $336; CDS0624 sp4t, $372.

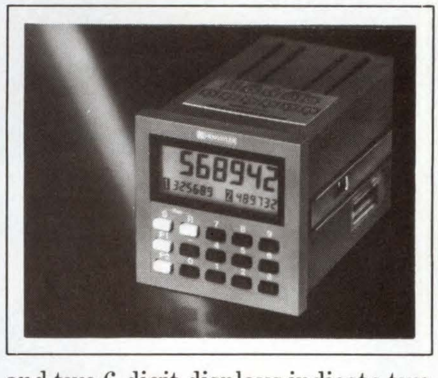
**Daico Industries Inc,** 2139 E Del Amo Blvd, Compton, CA 90220. Phone (213) 631-1143.

**Circle No 388**

## PANEL COUNTER

- *Provides a 7-digit count with two threshold levels*
- *Has several control outputs*

The Dino panel counter can perform a variety of simple control functions—for example, level or positional control—without additional circuitry. Its DIN-standard 72-mm-square front panel houses an LCD display and a control keyboard. A 7-digit display indicates the current count,



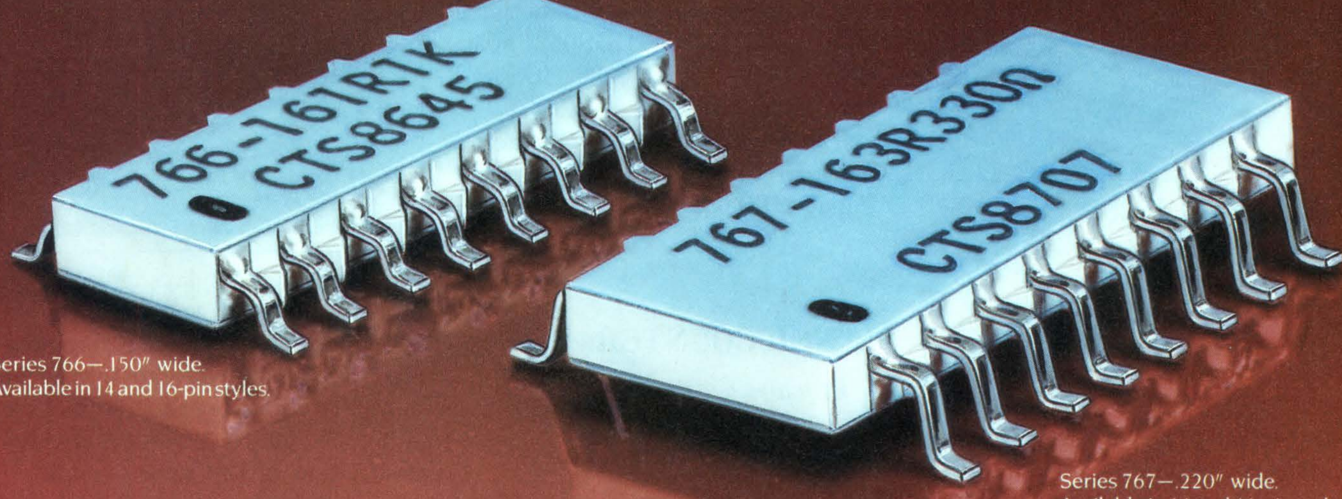

and two 6-digit displays indicate two preset counts that you can enter via the keyboard. To prevent unauthorized changes, you can totally or partially disable the keyboard. When the current count coincides with either of the preset counts, a corresponding control output is activated. The DIP-switch settings allow you to program these outputs into a bistable (above/below threshold) mode, or one of them into a monostable mode. Depending on the model, these outputs may be either changeover relay contacts or short-





**CIRCLE NO 48**

# CTS SOLID CERAMIC
# Surface Mount Resistor Networks



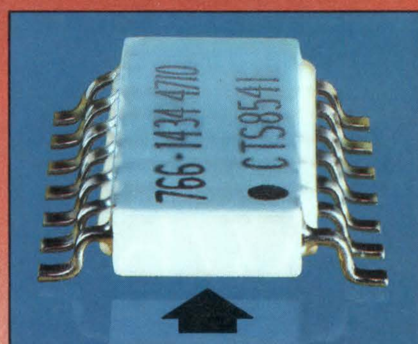

Series 766—.150″ wide.
Available in 14 and 16-pin styles.

Series 767—.220″ wide.
Available in 14 and 16-pin styles.

# Now in two sizes... .150″ and .220″ wide

## CONSIDER THESE CTS SOLID CERAMIC ADVANTAGES:

- Compatible with all SOIC processes
- Custom circuits readily available
- Maximum power dissipation
- Dimensional accuracy and stability
- Vapor phase or IR solderable
- Meets MIL-R-83401 environmental test requirements




Ample space is provided between body and board for fast thorough cleaning after soldering.

**These CTS Solid Ceramic Surface Mount Resistor Networks** are backed by the same resistor reliability that has set the industry standards for decades! Over 150,000 element *years* of continuous life testing confirms the reliability of each and every CTS network.

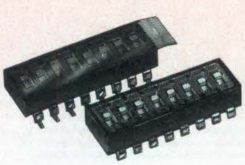

WRITE TODAY for new brochure entitled "CTS Surface Mount Resistor Networks." Contact: CTS Corporation, Berne Division, 406 Parr Road, Berne, IN 46711. Phone: (219) 589-8220. TWX: 810-323-1580.

**CIRCLE NO 102**

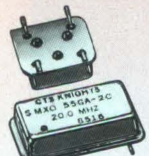
**Call TOLL FREE 1-800-982-0030**
for name and location of nearest CTS Sales Engineer

# CTS. MEANS RELIABILITY

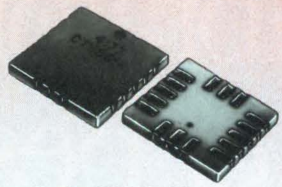
CTS CORPORATION • ELKHART, INDIANA



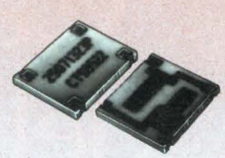
**Series 207—Surface mount,** process compatible AUTO-DIP™ Switches.
Phone: (805) 238-0427
**CIRCLE NO 103**



**Surface Mount Hybrid Clock Oscillators**
Fully hermetic resistance weld packages.
Phone: (815) 786-8411
**CIRCLE NO 104**



**Series 763 .350″ x .350″ Leadless**
Up to 20 pads. Meets LCC pad configurations.
Phone: (219) 589-8220
**CIRCLE NO 105**



**Series 762 User Trimmable**
Available in 8, 14, 16 or 18 solder pads.
Phone: (219) 589-8220
**CIRCLE NO 106**

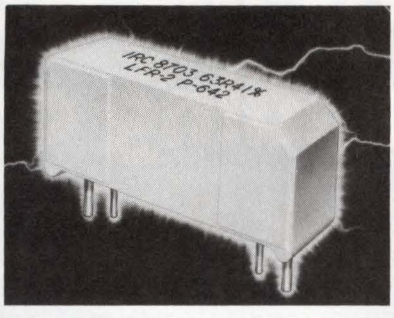
circuit-protected transistor outputs. An additional output is provided to indicate a zero count condition, and a direction output indicates the current direction of counting. Nonvolatile storage of the control output conditions during power failures is available as an option. You can configure the counter inputs for continuous up or down counting, for difference counting, or as a 1-, 2- or 4-phase phase discriminator. The input frequency limits are 5 kHz and 30 Hz for electronically and mechanically generated pulses, respectively. The device operates from a 10 to 30V dc supply, or from a 100 to 270V ac supply. DM 500.

**Hengstler GmbH,** Postfach 100, 7209 Aldingen 1, West Germany. Phone (07424) 891. TLX 760422.

**Circle No 389**

**Hecon Corp,** 15 Meridian Rd, Eatontown, NJ 07724. Phone (201) 542-9200. TLX 132457

**Circle No 390**




## THERMAL PROTECTORS

- *Meet FCC, EIA, UL and CSA requirements*
- *Rated for 2W at 25°C*

Units in the LFR-2 family of line-feed resistors provide board-level thermal protection for line cards and tip-and-ring circuits. The devices meet FCC, EIA, UL, and CSA saftey requirements and are available in two basic versions: precision-grade and commercial-grade. Resistance values span a 1 to 30 kΩ range, power rating equals 2W at 25°C, and operating range equals −40 to +85°C. Temperature coefficients are as low as 40 ppm/°C for the precision units and 300 ppm/°C for commercial grade devices. Resistance tolerance measures 1, 2, and 3% for precision units and 5 and 10% for the commercial devices. LFR-2 units come in a 4-pin SIP. $1.50 to $2.50 (5000).

**IRC Inc,** Box 1860, Boone, NC 28607. Phone (800) 255-4472; in NC, (704) 264-8861.

**Circle No 391**

## POWER MOSFET

- *Dissipates 125W*
- *Features a Kelvin pin to eliminate internal voltage drops*

The MTP40N06M power MOSFET is a current sense type device. It is rated for 40A, 60V and has a minimum on-resistance of only 40 mΩ. The device is housed in a 5-pin

# E-T-A® Circuit Breakers. Accepted by the world's most demanding critics.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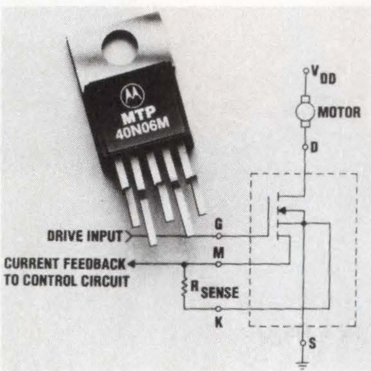
CIRCLE NO 91

TO-220 which is capable of dissipating 125W. The pinout includes the standard gate, drain, and source of the FET as well as a mirror and a Kelvin pin. You use the Kelvin pin to eliminate internal voltage drops which would cause erroneous sense voltage and an error in the current being sensed. This device mirrors the load current and reduces it by a factor of 900—the current mirror ratio—to reduce the power loss in the sense resistor by the same factor. \$2.80 (100). Delivery, four to 10 weeks ARO.



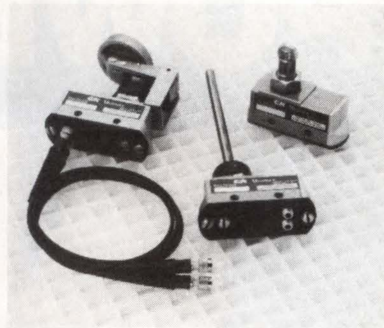

**Motorola Inc,** Semiconductor Products Sector, Box 52073, Phoenix, AZ 85072. Phone (602) 244-4911.

**Circle No 392**

## SWITCHES

- *Designed for hazardous environments*
- *Immune to EMI/RFI*

These metal-cased units contain a fiber-optic snap-action switch. The enclosure is designed to provide protection for indoor/outdoor use as defined by NEMA standards for type 4 enclosures. Two switch types are available. One works with 230 μm glass fiber to accommodate long distance applications. The second switch is compatible with 1000 μm plastic fiber for use in short distance applications. Both types operate over a −54 to +71°C range. The switches are immune to EMI/RFI and do not introduce any EMI/RFI into the environment. The enclosures are available with a variety of actuators—plain plunger, roller plunger, rod actuator, large knob, roller lever, and spring-loaded roller. \$40 to \$150. Delivery, six to eight weeks ARO.



**C&K/Unimax Inc,** Ives Rd, Wallingford, CT 06492. Phone (203) 269-8701.

**Circle No 393**

CONFIGURE-YOUR-OWN

## MIL SPEC • HIGH RELIABILITY

# POWER SUPPLIES


# A HIGHER LEVEL OF PERFORMANCE

### INTRODUCING EL 2000 SERIES

## Complete AC to DC and DC to DC multi output systems.

### MORE BENEFITS

**Save Space:** Completely protected AC-DC systems with rugged high density packaging to 8 watts/in$^3$.

**Less Heat:** Efficiencies to over 80% with next generation circuitry.

**Higher Reliability:** MTBF to 500,000 hours with conservative design criteria including NAVMAT guidelines.

### MORE CHOICES

- Up to 8 DC outputs to 500 watts.
- 1ø, 3ø and DC inputs.
- −55°C to +85°C operation.
- Mil-Std-704A-D, 1399 and 1275 input surge and spike protection.
- Meets many provisions of Mil-Std-810D, Mil-E-5400 and Mil-E-16400.

**Call or write for our new EL 2000 Catalog today!**

ARNOLD MAGNETICS

## ARNOLD MAGNETICS CORPORATION

4000 Via Pescador, Camarillo, California 93010-5049
Phone: (805) 484-4221 • TWX 910-343-6468 • FAX: (805) 484-4113


## DISPLAY

- *Operates over −30 to +85°C*
- *Available in pinned and pinless versions*

Model FE0203 is a 3½-digit liquid crystal display. In addition to the 0.5-in. digits, the display includes three decimal points, a low battery annunciator, a plus/minus sign, and a colon. The unit comes in transmissive, reflective, and transflective versions and is available with DIP connector pins or is pinless for use with elastomeric connectors. The displays measure 2×1.2 in. Its standard operating range equals −20 to +60°C, but is available with an extended operating range of −30 to +85°C. $7.98 (100).

**AND,** 770 Airport Blvd, Burlingame, CA 94010. Phone (415) 347-9916.

**Circle No 394**

## INDICATOR

- *Compatible with multiple sensors*
- *Has automatic resolution capability*

Model 500T, a digital temperature indicator, is compatible with type J, K, T, E, R, S, and B thermocouples and platinum RTDs with alpha of 0.00385 or 0.00392. A miniature rotary switch allows users to select the sensor type. The indicator features an automatic resolution capability. For measurements below 1000°, resolution equals 0.1°. From


1000° up, resolution automatically switches to 1°. Measurement capability ranges from −346 to +3325° in either F or C. The device provides a single-limit set point that can be set at any point within the indicator's range. The indicators also have a 0.5A relay for powering alarms. Measurement accuracy equals ±0.5°. $299.

**Beckman Industrial Corp,** 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 495-3236.

**Circle No 395**

WE CAN SHAPE YOUR FUTURE
MHS has a proven track record in the integration of very fast, low-power systems on silicon: SRAM, microcontrollers, ASIC, and telecom chips.
Because we built our 0.7/1.2 micron Super-CMOS wafer fab for volume and quality, it is fully qualified by the highest military & space authorities, and praised by some of the world's most demanding IC users.
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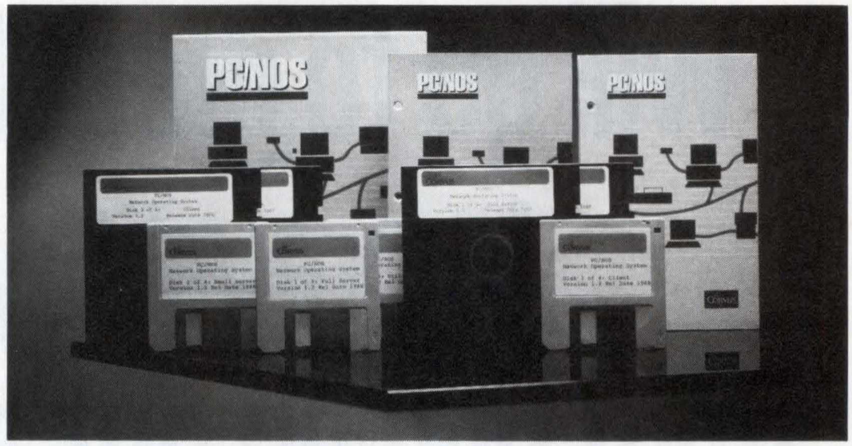
## CAE & SOFTWARE DEVELOPMENT TOOLS

### NETWORK OS

- *Works with a 4M-bit/sec, twisted-pair network*
- *Provides caching in LIM expanded memory*




Version 1.2 of the PC/NOS network operating system works with the vendor's Omninet/4 LAN, which provides a 4M-bit/sec data-transfer rate over a twisted pair of cable. The operating system provides distributed resource sharing, so you don't need a network file server; it also provides file and record locking under DOS 3.1 and later. The OS can use any expanded memory that conforms to version 3.2 or later of the LIM standard; you can specify the amount of expanded memory that the OS will use for caching, as well as the number of packets and open files. The OS employs standard DOS commands and, according to the vendor, is very easy to install and use. $695.

**Corvus Systems Inc,** 160 Great Oaks Blvd, San Jose, CA 95119. Phone (408) 281-4100. TLX 278976.

**Circle No 400**

### SOFTWARE

- *Demonstrates qualities and capabilities of neural networks*
- *Simulates paradigms for solutions to difficult problems*

The Awareness software package runs on IBM PCs and compatibles and consists of programs that demonstrate four neural-network paradigms. The generalization paradigm uses a generalized learning rule and demonstrates that a layered neural network can solve the exclusive-OR function, which perceptrons cannot do. The associative paradigm exhibits many of the computational capabilities of neural networks, such as preferential learning, fault tolerance, differentiation, and association. The optimization paradigm is an example of a neural network that can produce solutions to combinatorial optimization problems. The self-organization paradigm is an example of a nearest-neighbor classifier that behaves as an optimal signal processor in the presence of noise. The documentation contains introductory material on neural networks, together with the equations and references from the original papers that describe each paradigm. To run this software, you'll need an IBM PC or compatible that has a graphics card and at least 256k bytes of RAM. A math coprocessor is recommended but not essential. $250.

**Neural Systems Inc,** 2827 W 43rd Ave, Vancouver, BC V6N 3H9, Canada. Phone (604) 263-3667.

**Circle No 401**

### VME BUS FORTH

- *Lets you develop real-time Forth programs*
- *Provides math library and database facilities*

The PolyForth V4000 software development system is for use on VME Inc's V4000 VME Bus CPU board. The V4000 board is based on NCR's NC4016 µP, which executes high-level Forth code as its native instruction set. The NC4016 chip runs at 8 MHz; at this speed, according to the vendor, Forth programs execute 19 times faster than do compiled C programs running on a 10-MHz 80286. The software package includes complete source code, an optimizing compiler, clock/calendar management facilities, and utilities. You can create ROM-resident Forth programs as large as 64k bytes for embedded applications. At additional cost, you can obtain extensive libraries of mathematical and database-management routines. Software only, $2950; software and CPU board, $5745.

**Forth Inc,** 111 N Sepulveda Blvd, Manhattan Beach, CA 90266. Phone (213) 372-8493. TLX 275182.

**Circle No 402**

### FORTH FOR OS/2

- *Has segmented memory model*
- *Same file interface for paths and directories*

UR/Forth is a high-performance Forth programming environment for 80286- and 80386-based personal computers and runs in protected mode under Microsoft's OS/2 operating system. The package provides a segmented memory model and places code and data in one seg-


# PSpice

## The Standard for Analog Circuit Simulation Now Available on the Macintosh II

Since its introduction just over four years ago, MicroSim's PSpice has sold more copies than all other commercial Spice programs combined. In addition to running on the IBM PC family, including the new PS/2, the Compaq 386, the Sun 3 workstation and the VAX/VMS family, PSpice is now available on Apple's Macintosh II.

All these features which have made PSpice so popular are available:

- Standard parts libraries for diodes, bipolar transistors, power MOSFET's, opamps, voltage comparators, and transformer cores.
- GaAs MESFET devices.
- Non-linear transformer devices modeling saturation, hysteresis, and eddy current losses.
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs.

In addition, all these PSpice options are available on the Macintosh:

- Monte Carlo analysis to calculate the effect of parameter tolerances on circuit performance.
- The Probe "software oscilloscope", allowing interactive viewing of simulation results.
- The Parts parameter extraction program, allowing you to extract a device's model parameters from data sheet information.
- The Digital Files interface, allowing you to transfer data from your logic simulator to (or from) PSpice. The interface performs the necessary D to A or A to D conversions.

Each copy of PSpice comes with our extensive product support. Our technical staff has over 50 years of experience in CAD/CAE and our software is supported by the engineers who wrote it. With PSpice, expert assistance is only a phone call away.

Please call or write today for a free evaluation copy of PSpice. Find out for yourself why PSpice is the standard in analog circuit simulation.

MicroSim Corporation

23175 La Cadena Drive, Laguna Hills, CA 92653 U.S.A. • (714) 770-3022 (800) 826-8603 • Telex 265154 SPICE UR ment, headers in another segment, and the dictionary hash table in a third segment. It uses dynamic memory-allocation functions in a "well-behaved" manner, and provides a uniform file interface that supports paths, directories, and fixed disks. You can store Forth programs and data in normal OS/2 files and manipulate them with standard system commands and utilities. The package includes a table-driven screen editor that can handle as many as six files simultaneously; a table-driven 80286/87 assembler; and three libraries of software floating-point, 80287-assisted floating-point, and 80387-assisted floating-point routines. To run the package, you'll need a PC/AT, PS/2 Model 50 or higher, or compatible machine that has 2M bytes of RAM, a hard-disk drive, and a graphics adapter compatible with the IBM MDA, CGA, EGA, or VGA. $350.

**Laboratory Microsystems Inc,** Box 10430, Marina del Rey, CA 90295. Phone (213) 306-7412.

**Circle No 403**

## DATA ACQUISITION

- *Matches Helios-I hardware to IBM PCs and compatibles*
- *Lets you store and analyze data acquired by Helios-I*

Three data-analysis packages that run on IBM PCs and compatibles have been adapted to work with the vendor's Helios-I measurement-and-control system. The CIMPAC data-acquisition and instrument-control software package provides animated graphics for the display of data values, trends, and alarm conditions. The package is menu driven and lets you set up complex control and data-acquisition command sequences on the Helios-I; it features extensive on-line help and has facilities for intelligent event processing and for the automatic generation of reports. Labtech Notebook, from Laboratory Technologies Inc (Wilmington, MA), and the vendor's Helios Toolbox are packages that help you develop software for the Helios-I system and enhance the system's performance. CIMPAC, including a hardware PC interface, $3695; Labtech Notebook, $995; Helios Toolbox, $295.


**John Fluke Mfg Inc,** Box C9090, Everett, WA 98206. Phone (800) 443-5853; in WA, (206) 347-6100. TWX 910-445-2943.

**Circle No 404**

## ASIC DESIGN TOOL

- *Automatic generation of test vectors*
- *Synthesizes ASIC layout from a logical input*

Two major options have been added to the Genesil IC design system, version 7.0: Automatic Test Generation (ATG) and Logic Compiler. The ATG option uses proprietary algorithms to identify and optimize the test vectors needed to achieve target test coverage at the gate level. You can use it for sequential circuits, as well as for RAMs, ROMs, 3-state and precharge signals, and combinatorial circuits. By using seed vectors generated by Genesil logic simulations of the ASIC design, you can achieve fault coverage for difficult circuits in the same amount of time usually needed for

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much less complex ICs. A coverage analysis report tells you whether your design is inherently testable or whether you need to add testability blocks. The Logic Compiler option helps you to improve IC design performance and density by automatically performing functional, logical, and physical optimization. You can use this compiler for individual blocks, collections of blocks, or complete ASIC chips. It accepts input in the form of net lists generated by Genesil, and compresses the overall logic to reduce the number of gates required; it then compiles the optimized circuitry into standard cells. As options to Genesil, the prices are ATG, $39,500; Logic Compiler, $24,500.

**Silicon Compiler Systems Corp,** 2045 Hamilton Ave, San Jose, CA 95125. Phone (408) 371-2900.

**Circle No 405**

## UPGRADED PDL

- *Enables laser-printer output for DoD-STD-2167 documents*
- *Compresses files to reclaim unused disk space*

Version 2.1 of the Byron Ada program design language and document generator, which runs on VAX/VMS systems, has been recompiled to achieve a speed increase of approximately 50%. Byron now saves an intermediate form of the source code in a program library and lets you reclaim unused disk space by compressing the partition master file. This version of the program design language works with the LaTex text formatter, available from Kellerman & Smith (Portland, OR) or from the vendor, and it lets you generate tables and laser-printer output for the STLDD and SDDD documents required by DoD-STD-2167. $15,000 to $35,000, depending on host configuration.

**Intermetrics Inc,** 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-1840. TWX 710-320-7523.

**Circle No 406**

## C CROSS-COMPILER

- *Runs on HP Series 300 host under HP/UX*
- *Generates code for 68000 μP family*

OS-9/XCC is a C cross-compiler that runs on Hewlett-Packard Series 300 workstations under the HP/UX operating system (a version of Unix). It generates assembly-language code for target machines that are based on the Motorola 68000 family of μPs and run under the OS-9 operating system. The package provides extensive libraries based on the Berkeley 4.2 version of Unix, including standard I/O and math routines. It also includes the C Executive, a preprocessor, a 1-pass C compiler, optimizer utilities, a macroassembler, and a linker. It produces compact, position-independent, re-entrant code for the OS-9 target machine. Two versions are available: One is for 68000 targets and costs $3000; the other is for 68020 targets and costs $4500.

**Microware Systems Corp,** 1900 NW 114th St, Des Moines, IA 50322. Phone (515) 224-1929. TLX 910-520-2535.

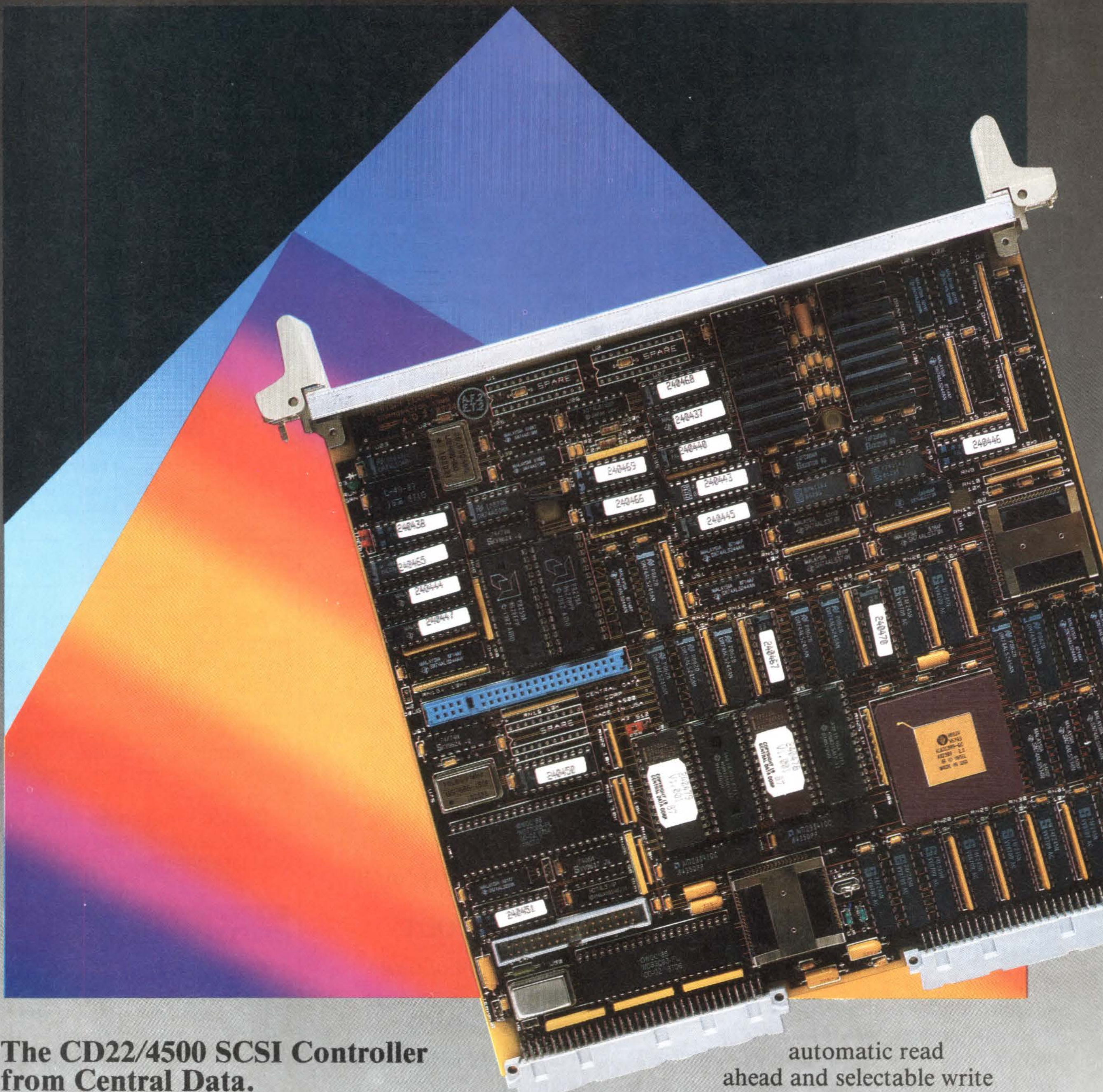
**Circle No 407**

## GATE-ARRAY LAYOUT

- *Automates the design of GaAs gate arrays*
- *Operates at the layout level*

The TQ3000 TurnChip ASIC layout module extends the automation of GaAs gate arrays from concept to fabrication. It supports designs that use the TriQuint (Beaverton, OR) TQ3000 chip, a GaAs array of 3000 equivalent gates that can operate at toggle rates as high as 1 GHz and that has 64 I/O pins that you can program to interface with ECL, TTL, and CMOS devices. The package forms part of the vendor's Gate-Array WorkSystem, a set of modular CAE software tools that TriQuint employs to enable you to perform both logic-design and layout functions on the same computer.

# Disk-Caching SCSI for Multibus* II.



## The CD22/4500 SCSI Controller from Central Data.

Central Data is committed to a leadership role in the Multibus II market. With special emphasis on SCSI support.

The CD22/4500 provides the ultimate Multibus II SCSI solution. It's fast, transferring data at the limits of the SCSI bus. And versatile, providing either direct SCSI commands or Intel compatible PCI commands.

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*Multibus is a trademark of Intel Corporation.

**CIRCLE NO 94**

The enhanced schematic net list provides all the information necessary for layout; you can interact with the net list to drive the layout process, and still retain control over device placement, priority nets, and critical signal timing. You only need to send minimal data to the foundry because it uses the same software; thus, the package not only shortens the development cycle by eliminating iterations between designer and foundry, but also improves the security of your design. $3000.

**Tektronix CAE Systems Div,** Box 4600, Beaverton, OR 97075. Phone (800) 835-9433; in OR, (503) 629-1152.

**Circle No 408**

## CROSS COMPILER

- *Runs on an IBM PC, PS/2, or compatible*
- *Compiles Forth source code to TMS34010 code*

The LMI Forth metacompiler runs on an IBM PC or PS/2 host or compatible and generates ROMable native code for Texas Instruments' TMS34010 graphics processor. The TMS34010 is a general-purpose CPU with machine-level instructions for both linear and XY-addressed line drawing, pixblt (pixel block transfer), region fills, clipping, and other graphics operations. The Forth metacompiler provides multipass, table-driven compilation; allows local labels and conditional compilation directives; and permits optional generation of "headerless code" to conserve memory in the target system. The package is compatible with the Forth-83 standard and lets you build applications in layers, using incremental compilations. You can create either ROMable or disk-based applications. To make programming easier, both the compiler and the cross-assembler accept byte addresses, automatically translating these into the bit addresses required by the TMS34010. The package includes a loader program that not only uploads a compiled image into the RAM on a TMS34010 development board, but provides communication between the development board and the host PC. You'll need a host that has at least 320k bytes of RAM and runs under DOS 2.0 or later; because the source files for the TMS34010 target system require 400k bytes of disk space, the vendor recommends a hard disk. $1000.

**Laboratory Microsystems Inc,** Box 10430, Marina del Rey, CA 90295. Phone (213) 306-7412.

**Circle No 409**

## ZOOM FOR AUTOCAD

- *Lets you set up, zoom, and pan with single-touch commands*
- *Eliminates drawing regenerations during zoom*

ZoomIt is a software add-on for Autodesk's (Sausalito, CA) AutoCAD version 2.5 or higher. It requires less than 10k bytes of memory and operates in conjunction with a tablet template that fits into transparent areas of the AutoCAD tablet template and the vendor's own tablet template, The Standard. ZoomIt lets you initiate standard zoom and pan operations by touching one point on the template rather than by using three or more keystrokes. The package eliminates Zoom All regenerations, second regenerations caused by changes in drawing extents, and accidental regenerations that may occur while performing normal AutoCAD zooms. In normal use, the program will probably save you a 30-sec regeneration every 10 minutes or so. $99.

**Palisades Research,** 869 Via de la Paz, Pacific Palisades, CA 90272. Phone (213) 459-7528.

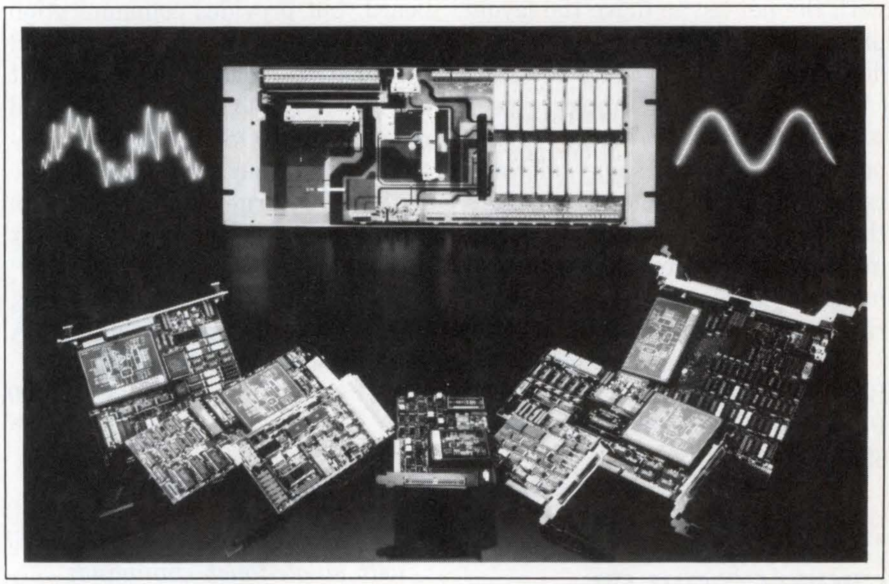
**Circle No 410**

# NEW PRODUCTS

## TEST & MEASUREMENT INSTRUMENTS

### SIGNAL CONDITIONERS

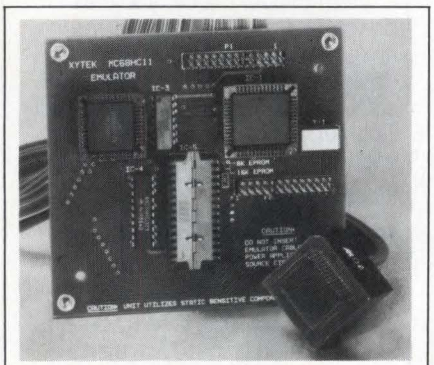
- *Allow analog and digital I/O*
- *Provide ohmic isolation to 1500V*



The DT760 signal-conditioning system consists of a back panel that accommodates 16 ohmically isolated, 1500V breakdown analog-input modules from the vendor's DT500 Series, which also includes a 9-pole, lowpass, Bessel antialiasing filter. The system provides 16 or 32 nonisolated digital I/O lines and a pair of D/A outputs. If you need isolated digital I/O capability, you can include it by tying in one of Opto-22 Corp's PB16A panels. If you must provide 4- to 20-mA current-loop outputs, you can substitute V/I converters for four of the input signal conditioners. The back panel incorporates screw terminals for connection to the monitored and controlled devices, and features connectors for cables to a data-acquisition board in the host computer system. Mounted next to each pair of screw terminals is a thermistor that provides cold-junction compensation when you use the terminal pair as a thermocouple input. $395; when equipped with serial Bitbus output, $550.

**Data Translation Inc,** 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700. TLX 951646.

**Circle No 415**




### 68HC11 EMULATOR

- *Interfaces to 52-pin PLCC socket via one cable*
- *Uses microcode in 8k- or 16k-byte CMOS EPROM*

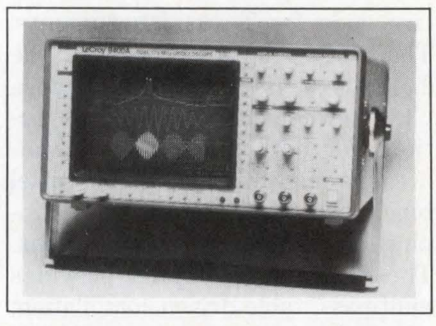
This 68HC11 emulator aids microcode development. It draws power from the 52-pin PLCC socket on your board—the socket that normally accommodates the μP. Instead of storing your microcode in the 68HC11's mask-programmed ROM, you store it in an 8k- or 16k-byte EPROM that you program off-line and insert into a ZIF (zero insertion force) socket on the emulator board. $497.

**Xytek Industries Inc,** 19431 W Davison, Detroit, MI 48223. Phone (313) 838-6961.

**Circle No 416**

### 175-MHz SCOPE

- *Stores 32k words/channel*
- *Offers 10-mV/div sensitivity*




The 9400A digital storage oscilloscope features a bandwidth of 175 MHz at 10 mV/div and a bandwidth of 225 MHz typ at 1V/div. The scope can store 32k points/channel (192k points max). After capturing a waveform, you can expand it horizontally by a factor of 100 and search for events that might not be apparent in a more compressed display. Whatever the scope's sweep speed, its deep memory allows it to sample at higher rates than can scopes with shallower memories. Such higher rates of sampling prevent aliasing problems caused by sampling rapidly changing signals too slowly. An optional IEEE-488 interface and an IBM PC or compatible computer running optional software provide the scope with signal-analysis and long-term data-storage capabilities. $9900. Delivery, six weeks ARO.

**Le Croy,** 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 425-2000. TWX 710-577-2832.

**Circle No 417**

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CIRCLE NO 88

## PROM PROGRAMMER

- *Programs 24-, 28-, and 32-pin devices in gangs and sets*
- *Handles eight 1M-bit EPROMs simultaneously*

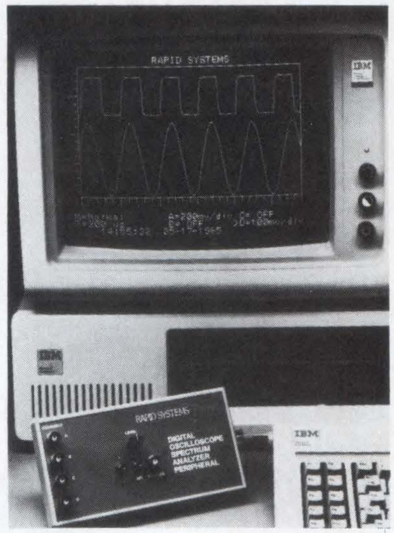
When used with the vendor's PP42 programmer, the 42M101 programs EPROMs and EEPROMs with capacities as large as 1M bit. It handles devices in 24-, 28-, and 32-pin packages and can program as many as eight devices simultaneously; when operating in the gang mode, it programs all devices identically, whereas when operating in the set mode, it programs each device differently. The programmer has two RS-232C ports. You can use either port to download information from a computer or from a development system. You can expand the programmer's RAM to hold 8M bits of data. The programmer recognizes Intelligent Identifier and Silicon Signature codes in the devices to be programmed and automatically configures the programming parameters accordingly. 42M101 module, $1095.

**Stag Microsystems Inc,** 1600 Wyatt Dr, Santa Clara, CA 95054. Phone (800) 227-8836; in CA, (408) 988-1118. TWX 910-339-9607.

**Circle No 418**

## DATA ACQUIRER

- *8-bit, 500-kHz ADC with 2k-point memory fits PC Bus*
- *Includes five software packages*



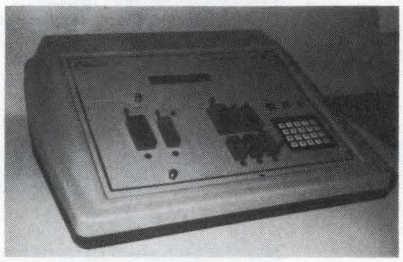
The R15 PC Bus 4-channel A/D converter features software-programmable 10-mV/div to 20V/div preamplification, 8-bit resolution, a 500-kHz conversion rate, and 2048-point data memory. It comes with software for data logging direct to

Text continued on pg 266

disk or to a plotter, for operation of the computer as a digital storage oscilloscope (DSO) or a spectrum analyzer, and for transferring data files to ILS, DaDisp, Lotus 1-2-3, and Ashton-Tate's dBase series. $995.

**Rapid Systems Inc,** 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

**Circle No 419**



## PROGRAMMER

- *Runs in stand-alone and computer-controlled modes*
- *Handles new device technologies via software updates*

According to the vendor, the University programmer can program virtually any programmable memory or logic device on the market. The programmer supports more than 700 device types from 29 manufacturers. As devices that incorporate new technologies appear, the vendor will offer software upgrades and "technology modules" to provide the modifications required for the programmer to program these devices. The programmer's internal buffer accommodates 32k bytes; you can specify a 64k- or 128k-byte buffer as an option. You can operate the unit in a stand-alone mode via its 20-key touchpad and its 20-character LCD display. You can also operate it from a remote terminal or computer via its RS-232C port. The device-drive signals are furnished by high-speed D/A converters under control of an 8085 μP. $3495.

**Advanced Programming Systems,** 35623 Chaplin Dr, Fremont, CA 94536. Phone (415) 796-0682.

**Circle No 420**

## VOLUME PROGRAMMER

- *Uses both 68000 and Z80 CPUs to speed programming*
- *Can handle 2M-bit devices with 24 to 40 pins*

The P16-IV is suitable for programming large quantities of EPROMs and EEPROMs in a production environment. It employs a Z80 μP and a 68000 μP to achieve its speed. It can program devices that have capacities as large as 2M bits and that come in 24- to 40-pin packages. Its adapters accommodate devices housed in flat packs and leadless chip carriers, plastic leaded chip carriers, pin grid arrays, and small outline integrated circuit packages. The programmer includes a 2M-bit buffer that accepts data from a master device, serial port, Centronics-compatible parallel port, or IEEE-488 port or keyboard. $4995 with either a 16-gang, 32-pin module or with an 8-gang, 40-pin module.

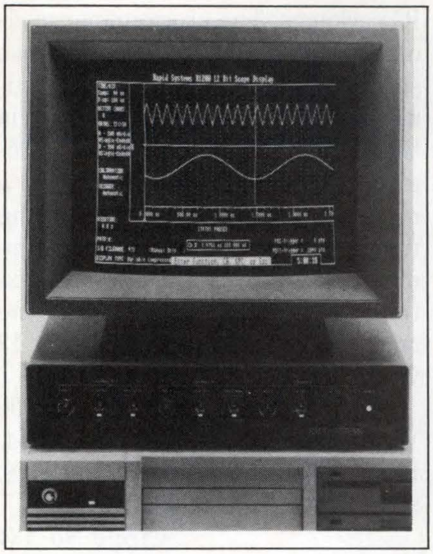
**Adams-Macdonald Enterprises Inc,** Promac Div, 800 Airport Rd, Monterey, CA 93940. Phone (408) 373-3607. TLX 882141.

**Circle No 421**

## PC-BASED DSO

- *Performs 12-bit sampling to 1 MHz*
- *Rejects noise with true differential inputs*

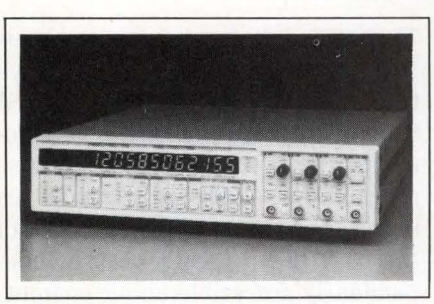
The R1200 allows your IBM PC or compatible computer to function as a 2-channel DSO (digital storage oscilloscope) with true differential inputs and a sampling rate you can vary from 1 Hz to 1 MHz. The



software lets you select sensitivities from 1 mV to 20V/div. Each channel has its own ADC and antialiasing filter. The trigger modes include pretrigger and posttrigger, internal and external trigger, and digital and analog trigger. The vertical zooming allows you to take advantage of the 12-bit amplitude resolution by expanding a portion of a displayed waveform for detailed analysis. An autosave feature can automatically store displayed waveforms on your hard disk. You can obtain real-time FFT spectrum analysis as an option. $2995.

**Rapid Systems Inc,** 433 N 34th St, Seattle, WA 98013. Phone (206) 547-8311. TLX 265017.

**Circle No 422**



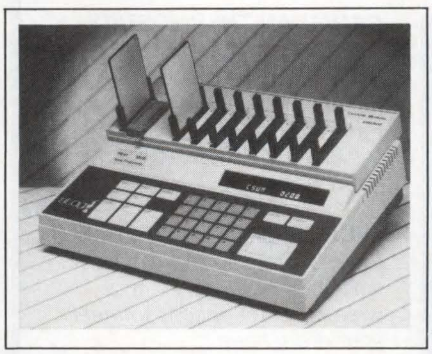
## INTERVAL COUNTER

- *Resolves single-shot intervals to 4 psec*
- *Measures frequency to 1.3 GHz*

The Model SR620 is a reciprocal interpolating time-interval counter that features 4-psec, single-shot time-interval resolution. The standard timebase ages 3 parts/billion/day. An optional, ovenized timebase ages at ⅙ of this rate. You can also supply your own 5- or 10-MHz timebase. When the unit makes a 1-sec measurement of frequency, its 16-digit LED display presents 11 digits of meaningful data. The instrument can measure frequency to 1.3 GHz as well as interval, period, phase, pulse width, risetime, and falltime. An X-Y driver lets you use your scope to display histograms and trends; you can obtain hard copies on a printer interfaced to the Centronics-compatible port or on a plotter that supports HPGL (Hewlett-Packard Graphics Language). In addition to RS-232C and IEEE-488 ports, the counter has analog outputs that enable strip-chart recorders to plot mean and deviation data. The unit's built-in functions include the calculation of 1-million-sample Allan variance. $3850.

**Stanford Research Systems Inc,** 1290 D Reamwood Ave, Sunnyvale, CA 94809. Phone (408) 744-9040. TLX 706891.

**Circle No 423**



## PROGRAMMER

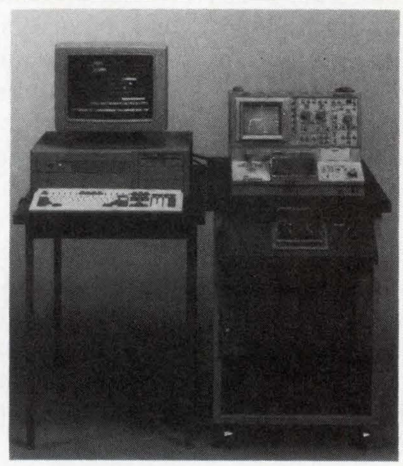
- *Gang programs credit-card-size memory modules*
- *Loads data from EPROM, host system, or smart card*

The 41M900 custom module for the vendor's PP41 programmer enables it to program credit-card-size "smart card" memory modules, which are easier for users to interchange than are more conventional

IC packages. The programmer module supports Seiko/Epson-format smart cards. The programmer module allows downloading of data via the PP41's RS-232C port. The programmer can also copy data from a master EPROM. You can use editing functions contained in the programmer's firmware to edit the data extensively before programming the smart cards. $1475. Delivery, 12 weeks ARO.

**Stag Microsystems Inc,** 1600 Wyatt Dr, Santa Clara, CA 95054. Phone (800) 227-8836; in CA, (408) 988-1118. TWX 910-339-9607.

**Circle No 424**



## FAILURE ANALYZER

- *Based on device curve tracer*
- *Tests 192-pin devices in less than five minutes*

The S3701 failure analysis system is based on the vendor's 370 curve tracer, PEP 301 computer, and TSI 8150 test-system interface. It automates the failure-analysis process and can test a 192-pin VLSI device in less than five minutes. Each pin of the DUT (device under test) is independently accessible under computer control. 140-channel system, $39,250; 192-channel system, $53,100. Delivery, eight to 12 weeks ARO.

**Tektronix Inc,** Box 1700, Beaverton, OR 97075. Phone (800) 835-9433. TLX 151754.

**Circle No 425**

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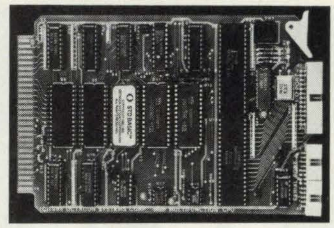
**NEW** **$195* STD BUS CONTROL COMPUTER**



Includes multitasking BASIC that runs faster than BASICA on an IBM/AT! Ideal for cost-sensitive applications requiring high performance and software integration. The 8410 CPU card includes an 8088 CPU, 2 serial ports, 5 counters, 9 interrupts, 32K RAM, and 16 TTL I/O lines that can also drive an opto module rack. All hardware and interrupts supported in BASIC. Program size up to 64K on card, 256K with chaining using an optional memory card. Autorun from RAM or EPROM. Use your IBM PC to develop and debug programs. FREE 1988 STD BUS CATALOG.

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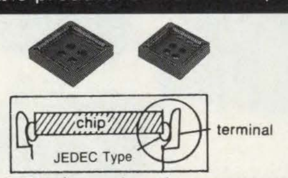


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**CIRCLE NO 328**

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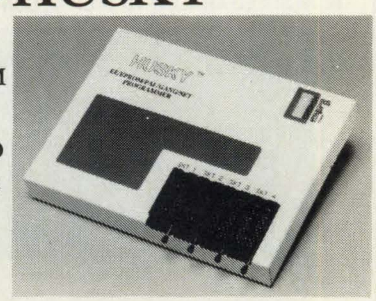

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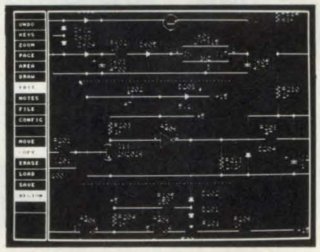

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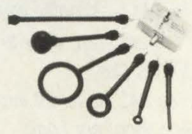

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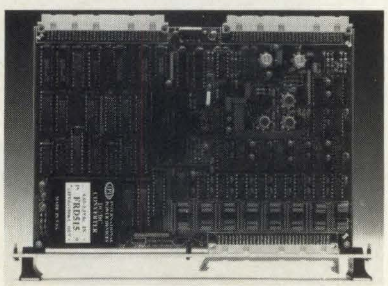

VMIC announces a high speed VMEbus, 12-bit analog-to-digital converter (VMIVME-3101) with 32 single-ended/16 differential front panel inputs. A wide variety of input filter options are available. The new product features built-in-test. Each front-panel input is monitored by an unbuffered self-test multiplexer. The self-test multiplexer provides a means of testing all inputs, and enables buffer amplifier offsets to be eliminated in software. The product is designed with a provision for simultaneous settling and conversion which gives A/D conversion throughputs to 200 kHz. The A/D converter conversion time is 3$\mu$s.

The price is $2,895.00 with all options.

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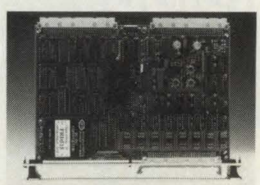

VMIC announces a VMEbus High Resolution Analog input board (VMIVME-3116) that features built-in-test and auto-calibration. The new product is designed with 32 single-ended/16 differential front panel inputs with a wide variety of input filter options. The Built-in-Test hardware features on-board precision voltages which may be read for fault detection and isolation. Each front-panel input is monitored by an unbuffered self-test multiplexer. The self-test multiplexer provides a means of testing all inputs, and enables buffer amplifier offsets to be eliminated in software. The ADC board features a resolution of 16 bits and a conversion time of less than 20 microseconds.

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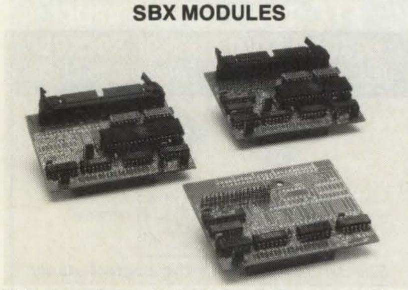

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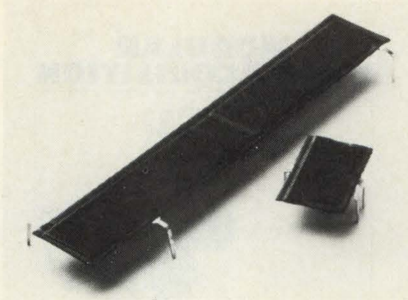

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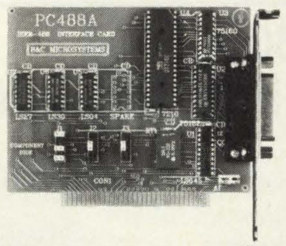

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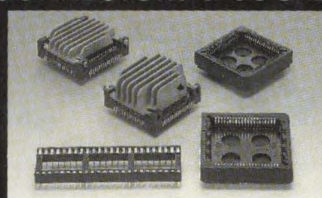

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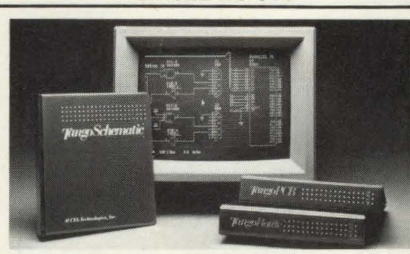

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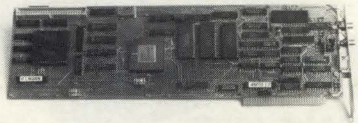

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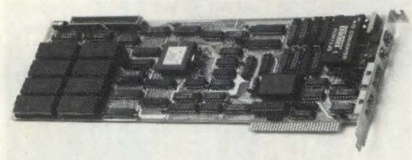

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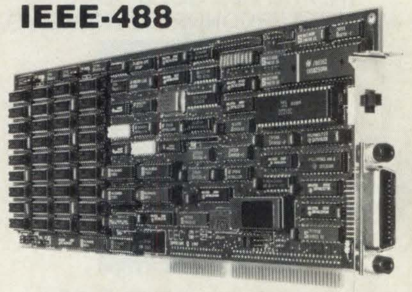

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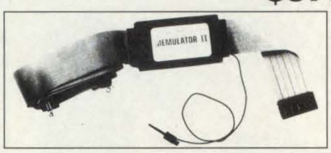


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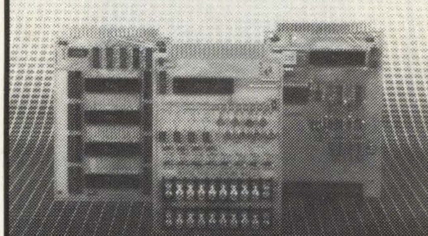

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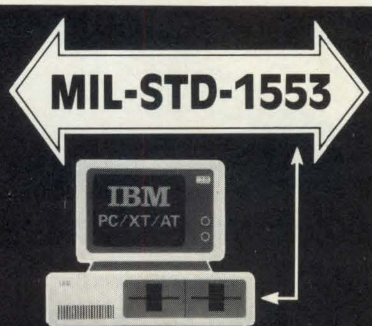


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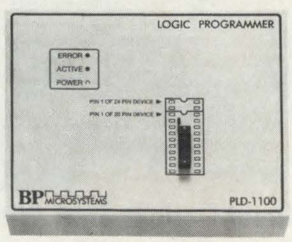


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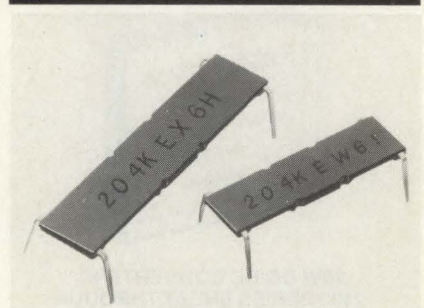

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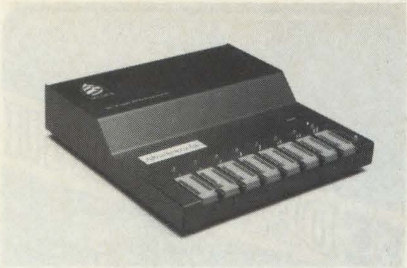

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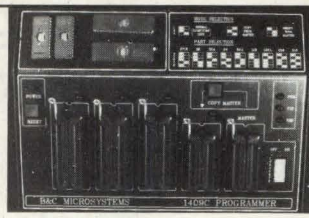

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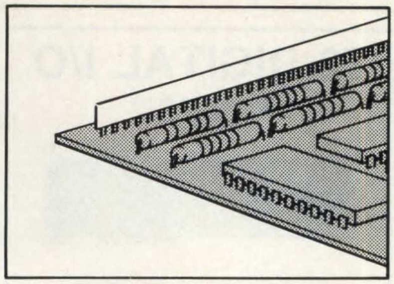

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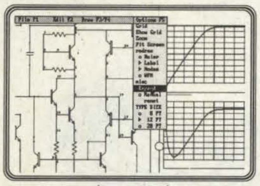

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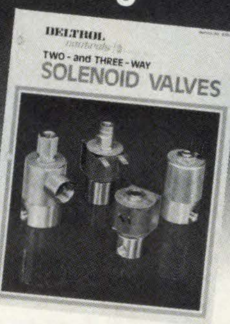


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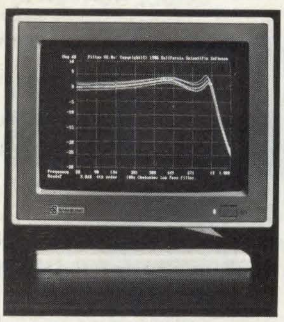

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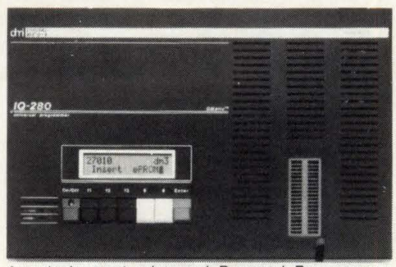


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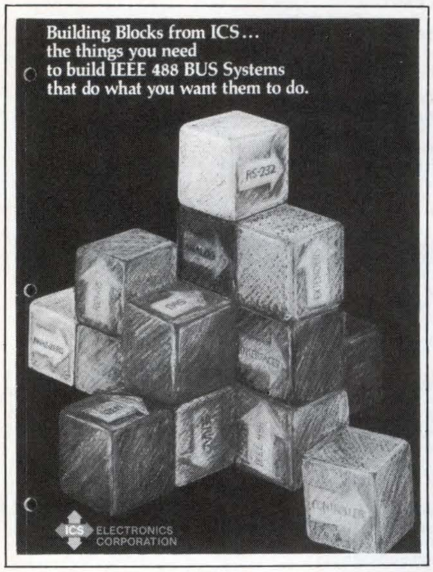


## Publication features IEEE-488 products

This 84-pg catalog surveys the vendor's IEEE-488 bus enhancement products, including interfaces, analyzers, extenders, and controllers. The product locator helps you find the eight main categories of IEEE-488 Bus products. A domestic price list, and a list of domestic sales representatives and international sales distributors are also provided.

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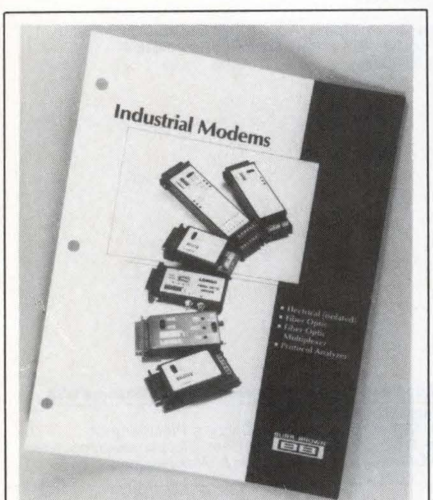


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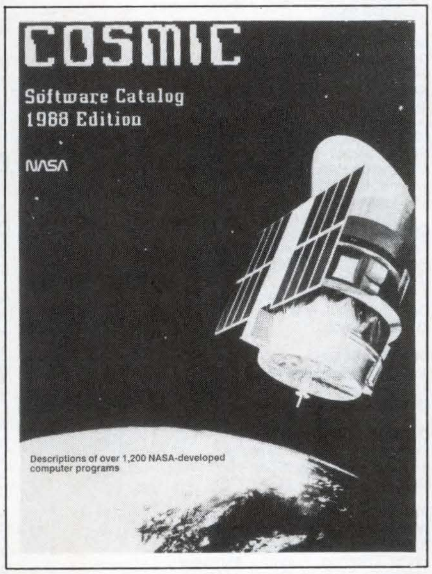


## Software developed under auspices of NASA

The 1988 Cosmic catalog describes 1219 computer software programs, as well as 50 newly added programs, that have been developed with the aid of NASA funding. The abstract for each program explains the program's capabilities, provides information to help you decide on applications, and lists the programming language, machine environment, size, and prices of the source code and supporting documentation. The publication also features keyword and author indexes, and subject classifications. Some of the program subjects include thermodynamics, structural mechanics, artificial intelligence, image-processing heat transfer, and circuit design. Printed edition, \$25; microfiche set, \$10; magnetic tape, \$50.

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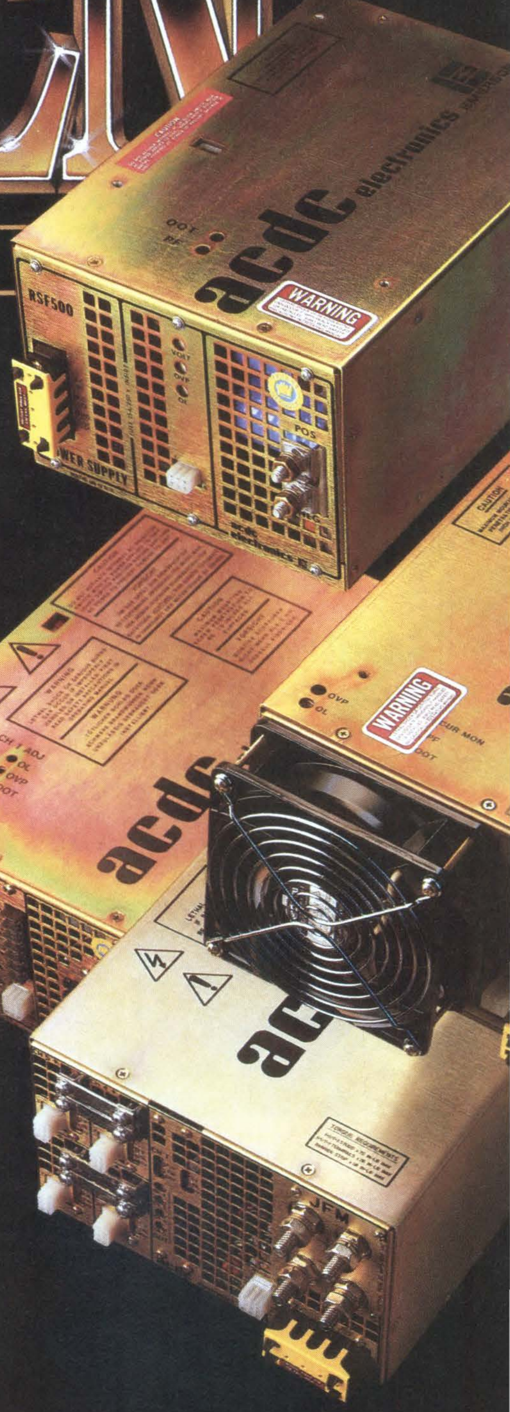


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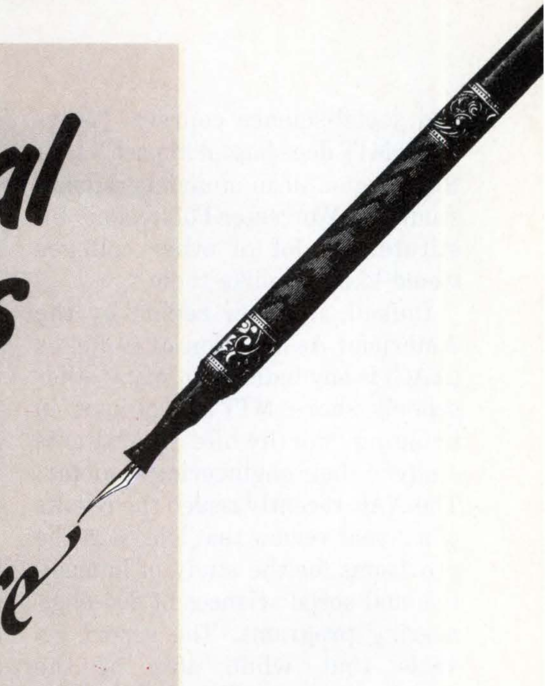

## Melding engineering studies and liberal arts

Deborah Asbrand
*Associate Editor*

As a project engineer for Hughes Aircraft Co, Bob Wilson enjoyed supervising the engineering students who took summer jobs with the company—with one exception. When the students presented a paper on their project and then made an oral presentation of their findings, what Wilson read and heard sometimes made him cringe.

"These senior-level students could neither write nor spell adequately," says Wilson. "They misunderstood what business or industry is all about and what industry is looking for in engineers."

Similar complaints about the writing and speaking skills of newly graduated engineers are filtering through electrical-engineering circles. Such remarks aren't new, but they are increasing in number. Some observers dismiss the criticisms as workplace renditions of "when-I-was-a-kid" stories and say that young engineers' unpolished writing and speaking skills are a function of the newcomers' youth. Others say, however, that the problem is genuine and fueled by the inability of engineering curricula to keep pace with the workplace changes that have occurred over the past two decades.

At many companies, engineers work more often than ever with sales and marketing staffs, and they need to be able to convey their ideas in clear terms to people who may have no technical background. Technical talent is as important as ever, but it's no longer enough.

The prime target for reform is the liberal-arts component of engineering programs. Although the Accreditation Board for Engineering and Technology requires students in accredited programs to take 12.5% of their classes in humanities and social sciences, engineering departments have generally soft-pedaled the requirements and given their students little direction or support. Students often fulfill the requirement by enrolling in a string of assorted 101-level courses.

In recent years, the movement to change this scenario has gathered steam. It's been buoyed by a renaissance of appreciation for the study of liberal arts and the notion that familiarity with the arts, humanities, and social sciences isn't just an academic exercise but an important tool that will serve young people in their intellectual development, regardless of degree program. Engineering educators held two separate meetings last fall to discuss, among other things, how colleges and universities can incorporate more meaningful liberal-arts studies into their engineering programs.

Another important harbinger of change was last year's decision by MIT, the nation's leading engineering institution, to step up its students' participation in humanities and social-science courses. "Anything MIT does has an impact," says Bill Grogan, dean of undergraduate studies at Worcester Polytechnic Institute. "A lot of other colleges would like to be like them."

Indeed, if a new report by the American Association of Colleges (AAC) is any indication, many other schools share MIT's problems in bringing worthwhile liberal-arts study to their engineering students. The AAC recently issued the results of a 2-year review that looked at the provisions for the study of humanities and social sciences of 204 engineering programs. The report reveals that while 45% of the engineering programs it examined did make advanced study in either the humanities or social sciences available to students, only 20% required it and 9% made it difficult or impossible for students to accomplish.

*Engineers say that their professional success hinges as much on their ability to work with other people as it does on their design of innovative products.*

**A people-oriented profession**

Given their expanded responsibilities, engineers say that their professional success hinges as much on their ability to work with other people as it does on their design of innovative products. "Our work is less engineering and more people-oriented," says Boeing test engineer Dale Ogle. Ogle counts among his most useful college courses the two philosophy classes he took. The knowledge he gained in those classrooms helps him "mainly in relating to others. We tend to think there's a right or a wrong to an issue, but there are always shades of gray."

Other engineers say that they've used their own initiative to acquire a diverse scholastic background. Although he's employed as a design engineer for a Melbourne, FL, maker of communications and computer equipment, Terry McCarty points to the dozen or so liberal-arts courses he took in the military as a crucial part of his undergraduate education. A richer education, he says, helps him examine a problem from several vantage points. "In engineering if you have just one way of looking at things, you miss a lot." In addition to his BSEE, McCarty holds an MBA. "Finding out how business people think was totally new to me," he says. "It was a whole new point of view."

Wilson says he began the groundwork for his future eight years ago, when he started taking speech and accounting courses at a college close to his Westminster, CA, home. "I knew I needed to know those things; I didn't look at it as an academic exercise," says Wilson. "This approach has allowed me to step off on my own." Last year, Wilson ended his 18-year career with Hughes to found Spectra Computer Services, a computer consulting company.

Corporate recruiters are looking for candidates who display similar well-roundedness. "Organizational boundaries have to be crossed frequently in order to get things done," says Hewlett-Packard corporate recruiting manager Barbara Waugh. "You really have to know how to present yourself, what you stand for, and what other people are saying. It doesn't work to have highly technical people who can't roll with the punches in volatile environments."

"When we interview people, we're trying to gain an understanding of their technical competence as well as what they're all about as people," says Russ Johnson, manager of strategic employment for Digital Equipment Corp (Maynard, MA). "We look at whether a person has a liberal-arts background and a broad skill set. All things being equal, we'll hire the engineer with the mixed skill set."

College placement officials are well aware that the most sought-after students on their campuses are those who exhibit a facility for engineering and communication. Exemplary writing and speaking skills "are the main things that corporate recruiters are looking for from our engineering students," says Kathleen Stanton, technical career advisor for the Career Planning and Placement Center at the University of California at Berkeley.

Turning out more of these highly prized graduates, though, isn't readily done. In fact, engineering education has sagged under heavy criticism on several counts in recent years. It's estimated that $2 billion to $4 billion is needed to replace and repair deteriorating laboratory equipment, and faculty shortages combined with large student enrollments have led to lopsided student-to-teacher ratios. Given the wide scope of problems they have to tackle, undergraduate engineering departments have preferred to table the issue of how and whether to improve liberal-arts study.

A 1986 report by the National Science Board minced no words in condemning the state of most engineering programs. It deemed lab instruction to be "uninspired, tedious, and dull," and called courses and curricula "out of date in content, unimaginative, poorly organized, and failing to reflect recent advances in the understanding of teaching and learning."

The most persuasive case for beefed up liberal-arts study, however, comes from observing several longstanding campus programs that attest to the harmonious coexistence of the humanities, social sciences, and engineering. The prestigious California Institute of

Technology, for example, requires its students to complete 150 units of study in math, science, and technology and nearly the same number—108—in liberal studies. Harvey Mudd College, part of the Claremont College system in southern California, was founded on the belief that engineering students should have to grapple with advanced studies in the humanities and social sciences.

> *A 1986 report called courses "out of date in content, unimaginative, poorly organized, and failing to reflect recent advances in the understanding of teaching and learning."*

The program at Worcester Polytechnic Institute (WPI) in Worcester, MA, is among the most ambitious efforts. It mixes a tough technical curricula with an equally strenuous program of liberal studies. Unlike many schools, WPI splits its humanities and social-science components into two distinct areas of study. In the humanities, students must pursue a direction of study that leads to some form of accomplishment. Those who choose to study music, for example, must cap their classwork with a performance before a critical audience.

Students must take an equally active role in the area of social science. "There was a feeling that students needed an experiential requirement here," says undergraduate dean Grogan, who, as a member of the electrical-engineering faculty, was on the committee that devised the new requirements in 1970. To complete the social-science requirement, he says, "a student has to solve a problem dealing with technology and society, or human values." To facilitate the advanced study, WPI operates project centers in Washington, DC; San Francisco; London; and Dublin. Students travel to a center and work on their projects for seven weeks. In total, nonengineering classes account for nearly 22% of WPI students' studies, nearly twice as many credit hours as the accreditation board requires.

By sponsoring rigorous liberal-arts studies and maintaining their high standings within the engineering community, these and other programs lay waste to the idea that the study of liberal arts somehow undermines technical achievement. The schools further disprove the contention that four-year engineering programs simply don't allow time for the study of such "nonessentials" as history, literature, or music.

MIT, for example, elected not to increase the number of courses that its students were required to take, but to bring cohesiveness to the existing requirements. To accomplish the objective, the school has narrowed from 150 to 100 the courses students may choose from. It has also required students to actively pursue some depth of study in a nonengineering field of their choice.

### Student opposition

MIT encountered student opposition to its plans in the form of a petition signed by 1500 of its undergraduate engineering students. Among some engineers-to-be, liberal arts remains a dirty word. "When you start talking to engineering students about taking classes in the humanities and social sciences, particularly on big campuses, you begin to pick up this cynical feeling that those classes are weak and not as interesting as tough engineering courses," says Tad Beckman, chairman of the department of humanities and social sciences at Harvey Mudd College.

Part of the problem is that many students subscribe to what Grogan calls a "zero sum" mentality—the belief that a facility for science and mathematics carries with it a natural weakness in another area. "Students go into engineering because someone in high school told them they were good at math," says Grogan. "The corollary is always that they're not good at something else. Our philosophy is, if you're good, you're good." Indeed, he adds, WPI's requirement that students not only pursue liberal studies but pursue a path that leads to accomplishment opens the eyes of many engineering students to their ability to succeed in nontechnical areas.

Behind students' distaste for liberal studies, though, lies widespread public misconception about what engineers do. John Lang, training and development manager for Analog Devices, says that when he addressed a group of high-school guidance counselors about careers in engineering, he stressed the need for students to write well and make polished presentations. "They were surprised at that because they thought engineers always had someone there to translate for them and so didn't need good communications skills," says Lang.

Certainly, the study of liberal arts is no panacea for improving engineering education. As the AAC report states, "Clearly, the influence of studying these fields can be overstated." Furthermore, while some engineering recruiters emphasize the need for students who have more diversified backgrounds, others say they're pleased with students' level of knowledge. Few, however, will dispute the value of training students to be people first, engineers second. **EDN**

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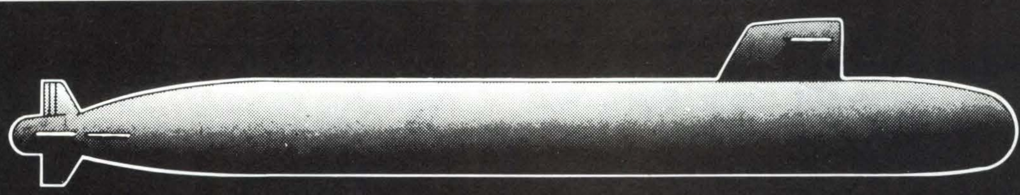

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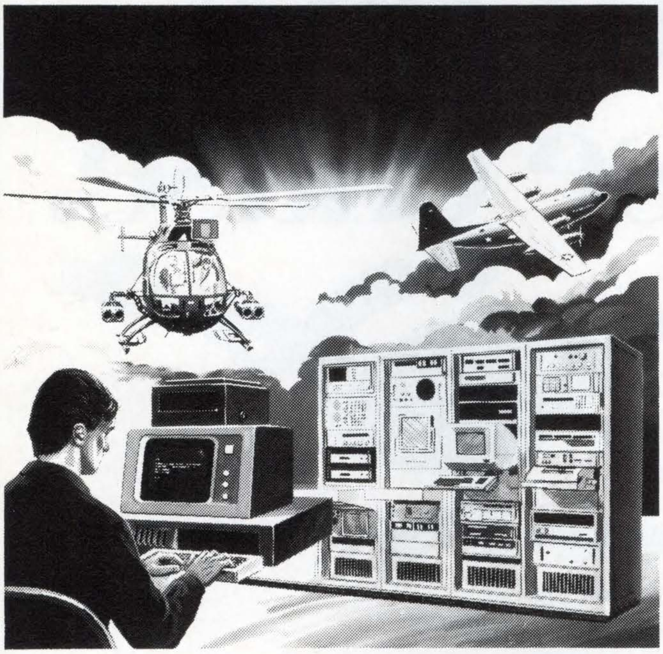

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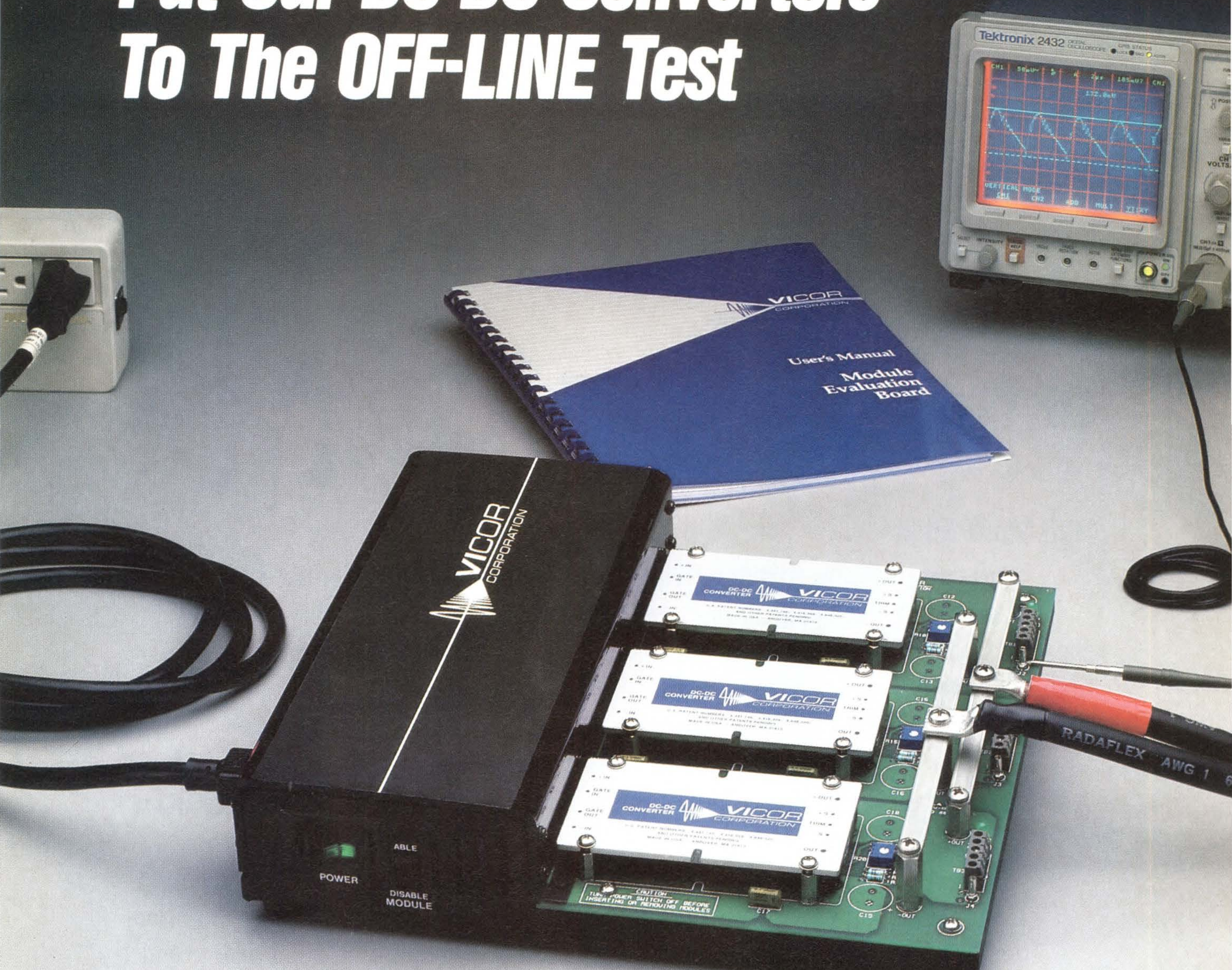


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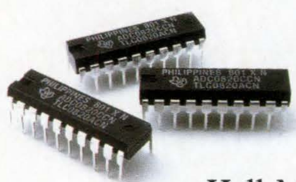

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CIRCLE NO 189

## Worldwide GaAs IC market expands at robust pace

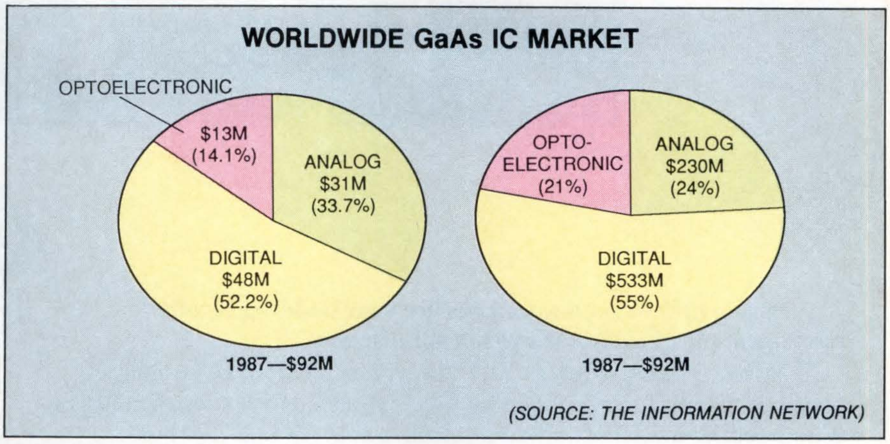
By 1992 the worldwide market for gallium arsenide ICs should reach \$962M, according to The Information Network, a market-research company based in San Francisco, CA. This forecast posits substantial growth for a market that grossed less than \$100M last year.

The US market will actually have the smallest—but still a quite healthy—growth rate of 50.7% through 1992. By comparison, Europe and Japan will enjoy compounded annual growth rates of 63.9% and 89.7%, respectively. Large demand in the communications and military sectors will stimulate growth in Europe; the communications and computer sectors will be the primary motivators in Japan.

The Information Network doesn't believe that Japan will necessarily dominate the worldwide market. The market researchers point out that Japan's vertically integrated structure dictates that almost all Japanese-produced GaAs ICs will remain in captive markets for the next few years. This high rate of internal absorption means that Japanese companies will not be free to sell these ICs abroad for some time. Consequently, Japan will test at home to achieve volume production, high yields, and low cost.

The GaAs industry in general has had to clear several hurdles, including processing methods, quality control, production yields, packaging, testing, and standards. The Information Network stresses, for example, that GaAs manufacturers must be successful at the LSI level in order to be cost effective. By offering increased logic density that results in a larger number of functions per chip, GaAs can offset the high cost of their devices, and at the LSI level, beat silicon in terms of price vs performance.

At present, a minimum of 50% of all applications for GaAs ICs goes for applications where only one additional GaAs chip substantially enhances the accuracy or bandwidth of the general system, which is generally defined by ECL devices. The need for compatibility with ECL ICs is therefore quite clear.




## Continuous industries falter in MAP plans

Developed in the early part of this decade, MAP (Manufacturing Automation Protocol) represents a concerted effort, initially on the part of General Motors, to establish a standard means of communication between computers and other manufacturing equipment in factories. A number of other major users of factory equipment and industrial LANs soon joined GM in the project. Skepticism has been growing, however, in the past year or two, because of the slow development of MAP products and the ebbing support of equipment vendors, according to Venture Development Corp (Natick, MA).

The overwhelming need for multivendor compatibility, particularly in industries that manufacture continuously (as opposed to those who produce in a batch or discrete way), has left only the very largest companies with the biggest facilities willing to test and adopt MAP standards and products. Most continuous manufacturers, VDC concludes, will wait for the widespread acceptance of products and for general industry support before committing themselves to the new technology. MAP thus faces a somewhat circular predicament.

The limited availability of MAP products biases companies against long-range purchasing plans that include MAP products. Continuous manufacturers, VDC found, tend to be quite conservative and will wait for strong vendor support before they commit to MAP technologies. Other manufacturers feel ill-equipped to adopt MAP standards, which they find too sophisticated and often a thing of the very distant future. Still others associate MAP with discrete manufacturing, partially because of GM's close ties to MAP development. Overall, however, most manufacturers concede the importance of communications standards for future automation development. Not only will standards ultimately solve the multivendor problem of incompatibility, but they will also streamline network design and reduce the costs of interfacing. The next few years will see a significant increase in the number of supervisory networks used in process plants, and hence this period may prove critical to the success of MAP standards and products.

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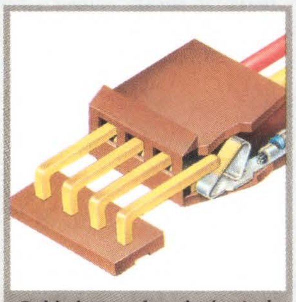

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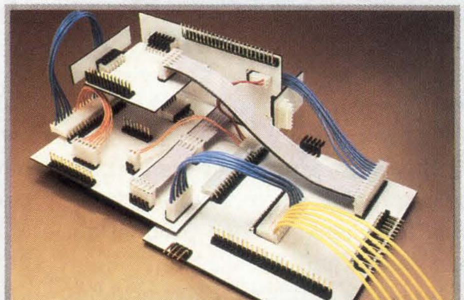

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