A CAHNERS PUBLICATION

MARCH 31, 1988

EDN®

Digitize analog signals using simple procedures

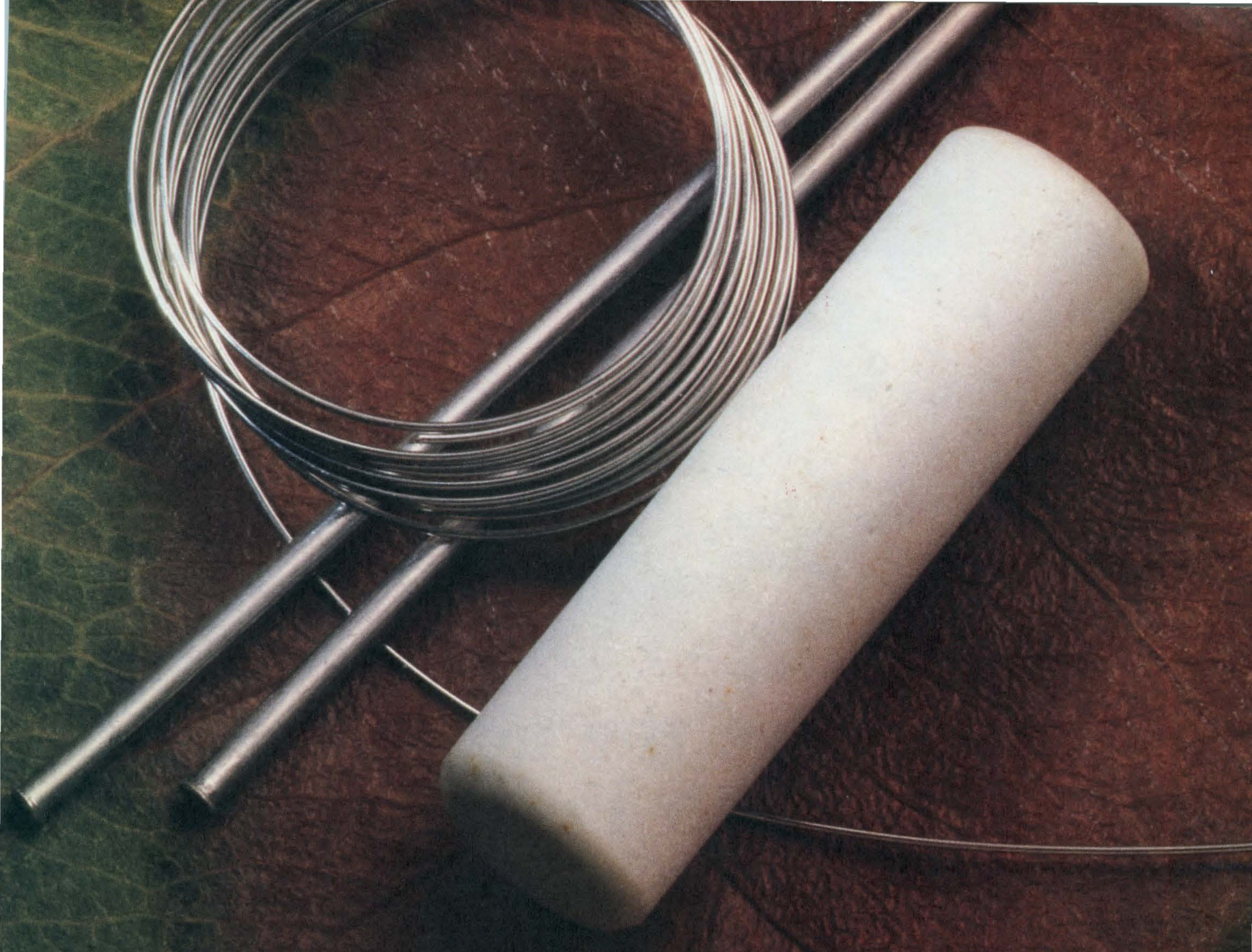
Motor modeling eases control-system design

Fiber-optic transmitter and receiver modules

Video RAMs

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Smart-power ICs expand application horizons



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dc to 3GHz

- less than 1dB insertion loss over entire passband
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- 5 section, 30dB per octave roll-off
- VSWR less than 1.7 (typ)
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- meets MIL-STD-202
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finding new ways...
setting higher standards

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LOW PASS Model *LP-	10.7	21.4	30	50	70	100	150	200	300	450	550	600	750	850	1000
Min. Pass Band (MHz) DC to	10.7	22	32	48	60	98	140	190	270	400	520	580	700	780	900
Max, 20dB Stop Frequency (MHz)	19	32	47	70	90	147	210	290	410	580	750	840	1000	1100	1340

Prices (ea.): P $9.95 (6-49), B $24.95 (1-49), N $27.95 (1-49), S $26.95 (1-49)

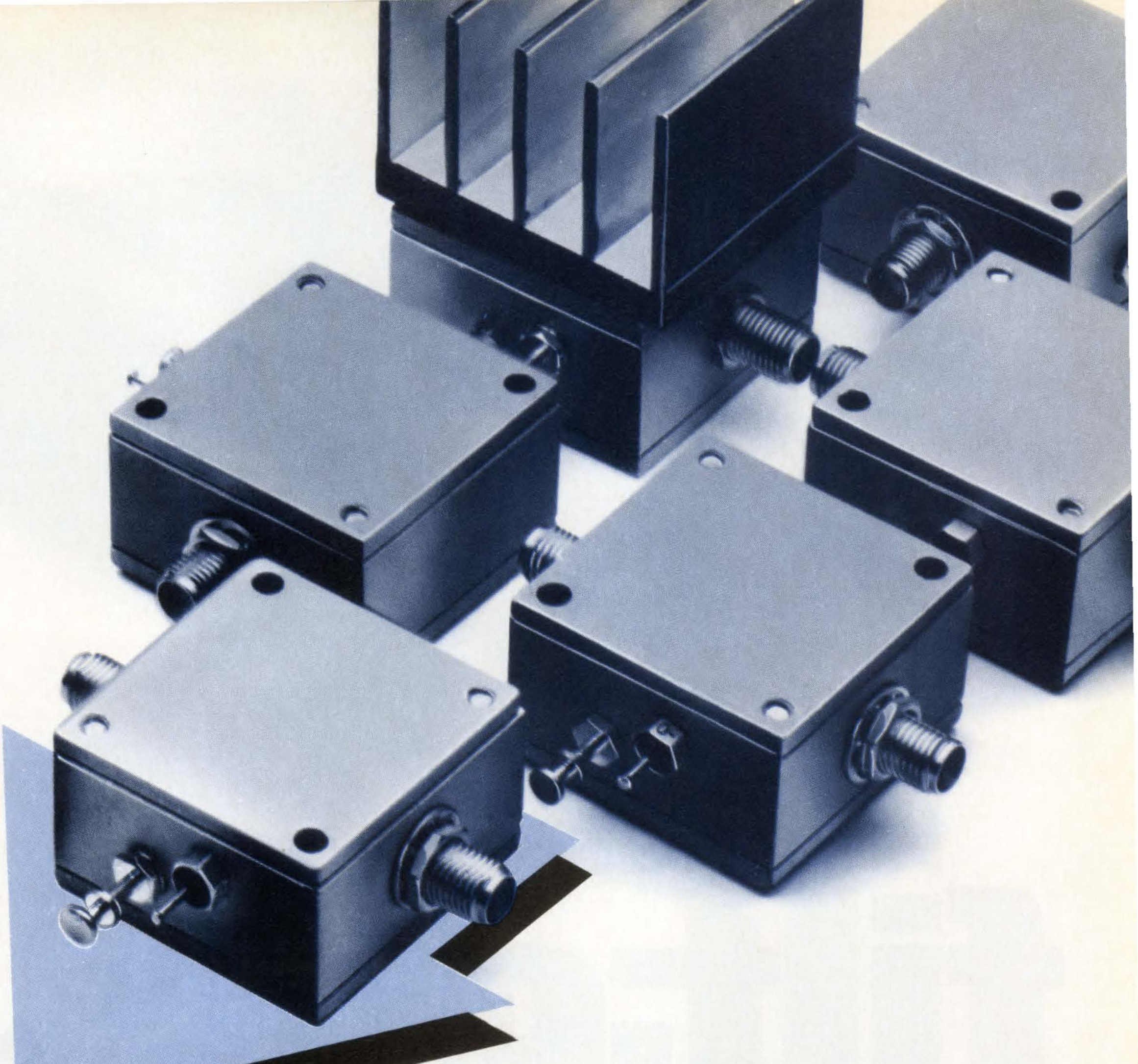
HIGH PASS Model *HP-		50	100	150	200	250	300	400	500	600	700	800	900	1000
Pass Band (MHz)	start, max.	41	90	133	185	225	290	395	500	600	700	780	910	1000
	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	150	190	290	365	460	520	570	660	720

Prices (ea.): P $12.95 (6-49), B $27.95 (1-49), N $30.95 (1-49), S $29.95 (1-49)

*Prefix P for pins, B for BNC, N for Type N, S for SMA   *example:* **PLP-10.7**

C105 REV.D

CIRCLE NO 199



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50KHz—2000MHz, Low Noise 100mW output Gain Controlled from **$69.95**

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One week delivery... one year guarantee.

SPECIFICATIONS

MODEL	FREQUENCY MHz	GAIN, dB (min.)	MAX. POWER OUTPUT dBm(typ)	NF dB(typ)	PRICE $ Ea.	Qty.
ZFL-500	0.05-500	20	+9	5.3	69.95	1-24
ZFL-500LN	0.1-500	24	+5	2.9	79.95	1-24
ZFL-750	0.2-750	18	+9	6.0	74.95	1-24
ZFL-1000	0.1-1000	17	+9	6.0	79.95	1-24
ZFL-1000G*	10-1000	17	+3	12.0	199.00	1-9
ZFL-1000H	10-1000	28	+20	5.0	219.00	1-9
ZFL-1000LN	0.1-1000	20	+3	2.9	89.95	1-24
ZFL-1000VH	10-1000	20	+25	4.5	229	1-9
ZFL-2000	10-2000	20	+17**	7.0	219.00	1-9

* 30dB gain control **+15dBm below 1000MHz

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CIRCLE NO 198

C101REV.D

Volume 33, Number 7

EDN

March 31, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: Recent introductions in the smart-power-IC area are giving designers alternatives to discrete solutions in many applications. See pg 112. (Photo courtesy Motorola)

DESIGN FEATURES

Continued on page 7

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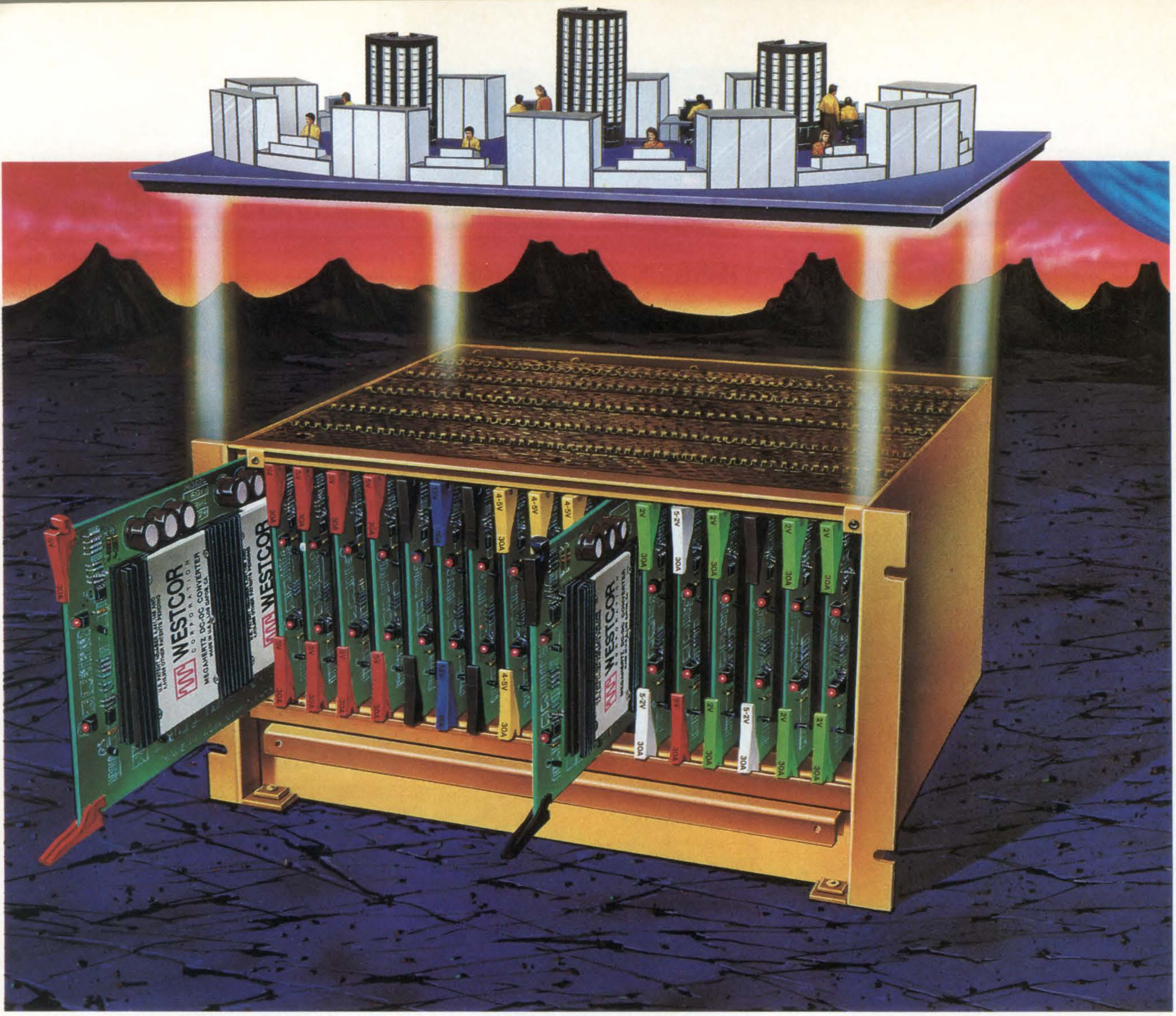


A NEW WORLD OF HIGH POWER FLEXIBILITY

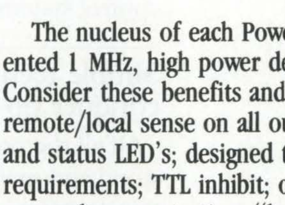
Westcor's PowerCage™ and PowerCards™ comprise a modular power supply system of galactic power (7200 watts max.), flexibility (36 outputs max.) and efficiency (80% typ.). More like an expandable computer mainframe in design and concept than a standard high power supply, the PowerCage offers space-age alternatives to users of outdated 5x8x11 inch box switchers.

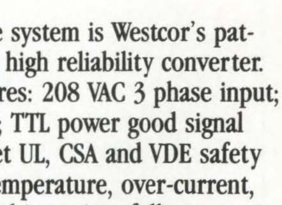
Measuring 19x10.5x11.25 inches deep the PowerCage fits into a standard NEMA rack and powers 18 slots for single or dual output PowerCards or dummy cards. PowerCage backplanes provide connections for easy configuration by the user.

Low profile (.8″) PowerCards supply single outputs from 2 to 75 VDC at up to 400 watts (outputs from 2 to 5 VDC limited to 60 amperes). Dual output cards source two isolated outputs each at half of the above ratings. Single output cards can be paralleled with current sharing to provide kilowatts via simple backplane configuration.

The nucleus of each PowerCage system is Westcor's patented 1 MHz, high power density, high reliability converter. Consider these benefits and features: 208 VAC 3 phase input; remote/local sense on all outputs; TTL power good signal and status LED's; designed to meet UL, CSA and VDE safety requirements; TTL inhibit; over-temperature, over-current, over-voltage protection; "hot" card insertion; full power at 50°C.

Future options include: DC input; IEEE-488 programmability; fault tolerant operation and battery backup. To discover a new world of high power flexibility, please contact us.





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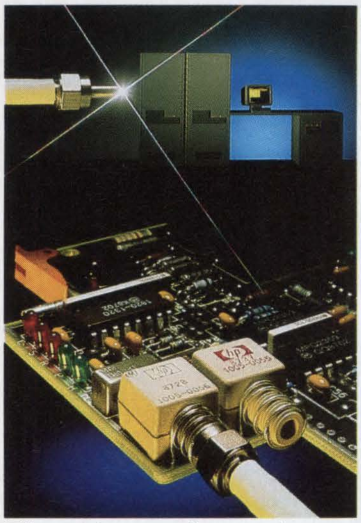

***Fiber-optic transmitters and receivers** accommodate a spectrum of data rates that extends from dc into the gigabit-per-second range (pg 57).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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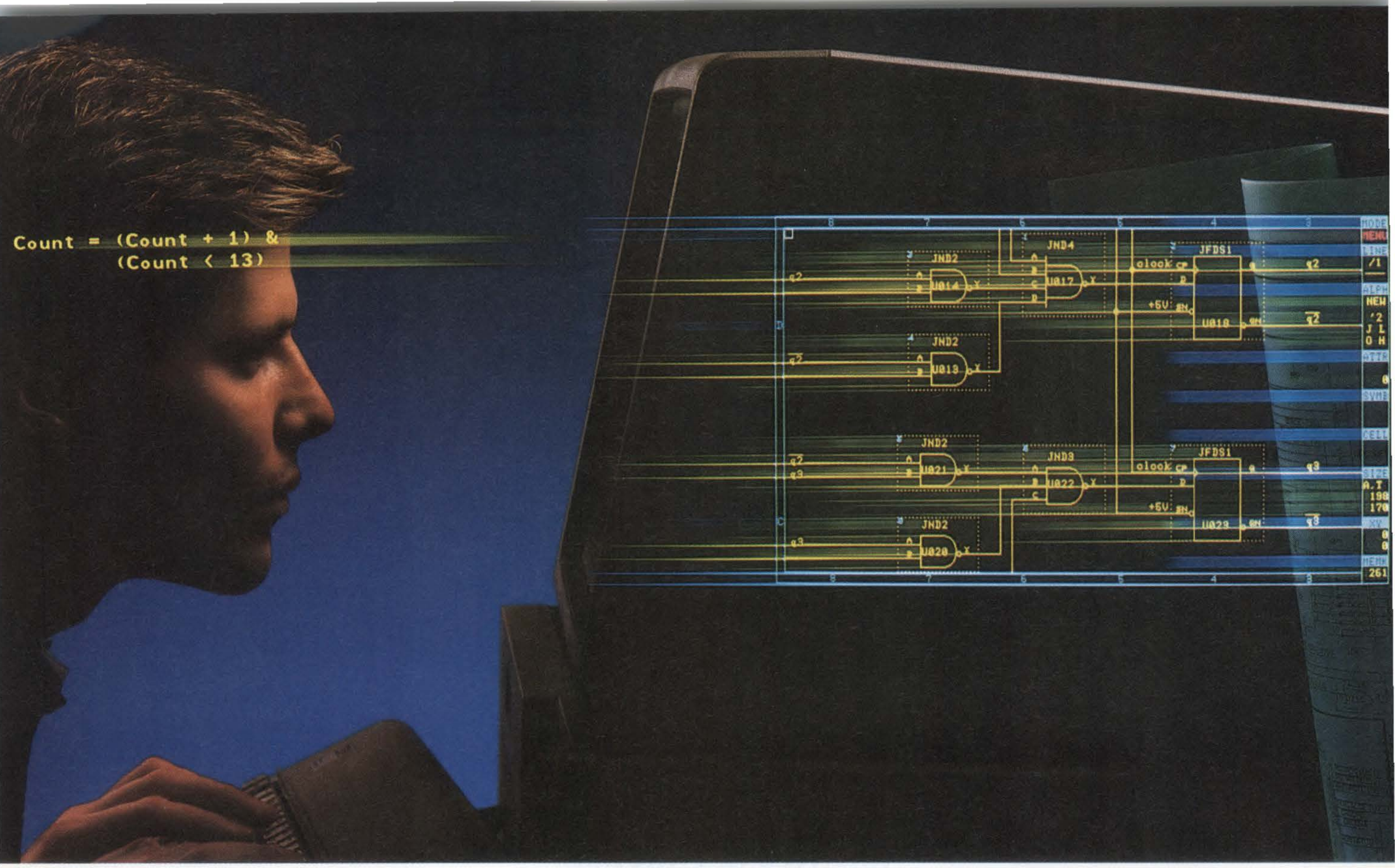

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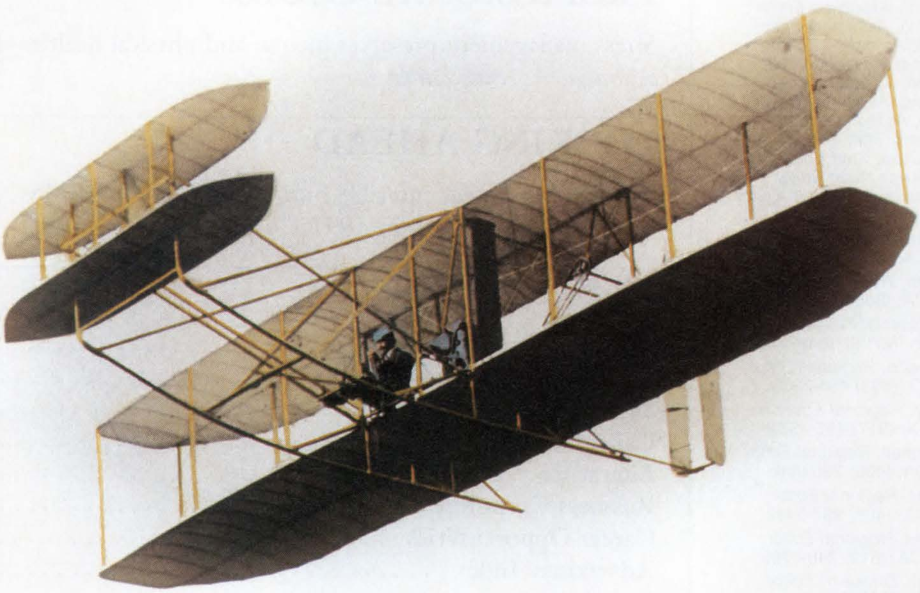
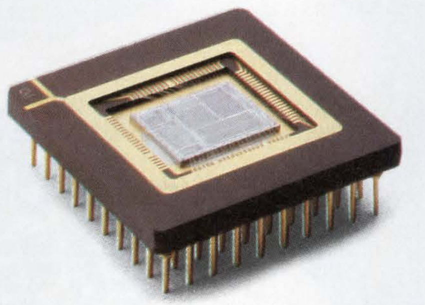


"IT'S GOT POSSIBILITIES, BUT IT'S JUST TOO POWERFUL FOR MY APPLICATION NEEDS."

DESIGN ENGINEER, 1988



Over the centuries, people have looked at the latest in technology with a bit of skepticism. The Transputer from INMOS is no exception.

When we first introduced the Transputer, designers were indeed intrigued. They were impressed with our T800—a 32-bit floating point microprocessor with an average speed of 10 MIPS and the ability to sustain 1.5 MFLOPS or 4.0 million single precision whetstones. "Incredible," designers said. "But it's more than we can use."

Not true. The fact is as a stand-alone processor, the T800 gives you benefits you can use every day. It runs programs even faster than Intel's combined 80386 and 80387 or Motorola's combined 68020 and 68881. Plus, it requires significantly less memory to hold compiled code.

And, by increasing the number of Transputers, you can increase system performance proportionally with no limit to the number of Transputers that can operate concurrently. Like linking seven T800's together to give you the processing power of a mighty Cray 1S supercomputer.

Or you could use ten IBM add-in cards from INMOS carrying ten T800's each, to enable your desktop PC to deliver 150 MFLOPS. That's like having the power of 150 11/780 VAX machines right at your fingertips.

So take another look at the Transputer. It's not just a dream for the future, it's a high-performance product for today. And it's a technology that is already taking off.

TRANSPUTER

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Like a beach in summer, Valid is drawing crowds of loyal Sun followers. And for good reason.

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What's more, our CAE/CAD solutions work on everything under the Sun, from their low-cost Sun-3/50 to the powerful, high-speed Sun-3/260. There are even brighter days ahead, because Valid will support future Sun products.

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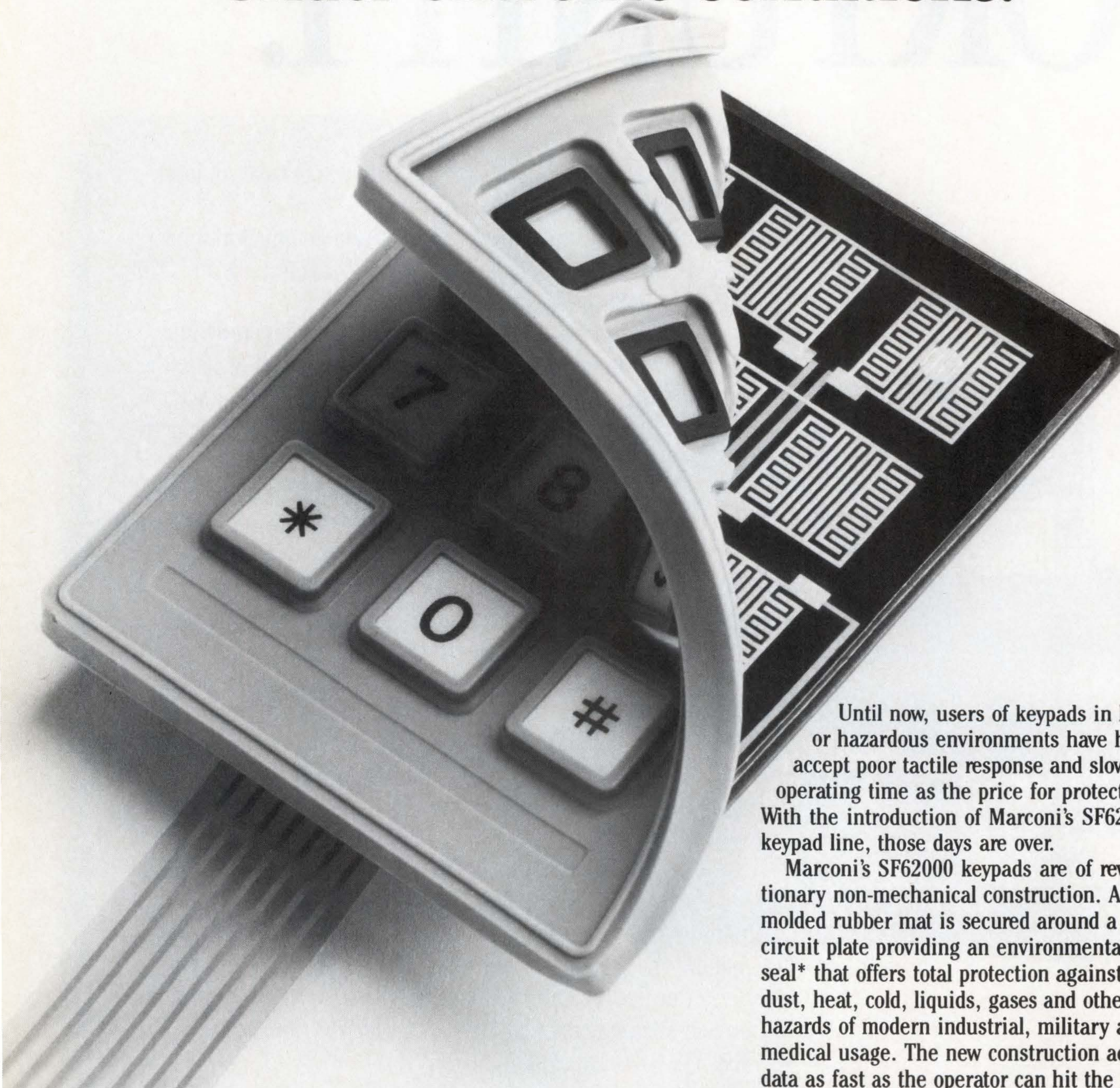
Marconi introduces the only keypad made to give extreme reliability. Under extreme conditions.



Until now, users of keypads in hostile or hazardous environments have had to accept poor tactile response and slower operating time as the price for protection. With the introduction of Marconi's SF62000 keypad line, those days are over.

Marconi's SF62000 keypads are of revolutionary non-mechanical construction. A molded rubber mat is secured around a rigid circuit plate providing an environmental seal* that offers total protection against dirt, dust, heat, cold, liquids, gases and other hazards of modern industrial, military and medical usage. The new construction accepts data as fast as the operator can hit the keys, with positive tactile "snap action" confirming contact even when the keys are not struck precisely.

The SF62000 line is available in 4, 12, 16 key and QWERTY formats in a variety of mat colors and keytop legends. For complete information, including the availability of samples, write or call today.

*Exceeds BS 5490 (Class IP67) requirements.

See Us At The EDS Show, April 26-28, Booth #631

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CIRCLE NO 192

Your next destination:

NEWS BREAKS

EDITED BY JOANNE CLAY

STANDARD-CELL LIBRARY SUPPORTS 2-GHz TOGGLE RATES

You can design LSI circuits requiring as many as 6000 equivalent gates and 2-GHz toggle rates by using TriQuint Semiconductor's (Beaverton, OR, (503) 641-4227) QLSI standard-cell library. Parts designed using the GaAs-based QLSI standard-cell library will support higher toggle rates and consume less power than do equivalent designs that use silicon-based ECL. A variety of I/O cells allows you to use this library to develop ICs that can interface directly to ECL, TTL, and CMOS logic families. The standard-cell library makes more efficient use of die area than gate arrays do. The efficient use of die area helps keep your production costs down. The nonrecurring engineering (NRE) cost for a QLSI standard-cell IC starts at $60,000, including design manuals and work-station software. Typical turnaround time from receipt of customer input to delivery of the packaged parts is 16 weeks.—Doug Conner

TAPE-DRIVE VENDORS DISCUSS DIGITAL AUDIO TAPE STANDARD

By invitation from Hewlett-Packard Co (Palo Alto, CA) and Sony Corp (Tokyo, Japan), 26 tape-drive manufacturers met on February 26, 1988, to review a proposed data-storage format for digital audio tape (DAT) that was jointly developed and presented by the two host companies. Although commercial audio DAT decks have yet to penetrate the US market because of high prices and piracy concerns, DAT cartridges promise to make an ideal, compact, low-cost data-storage medium. The HP/Sony format can store more than 1.3G bytes on a DAT cartridge costing only a few dollars, and it supports a data-transfer rate of 11M bytes/sec. Neither Sony nor HP has yet introduced products that employ the proposed storage format.—Steven H Leibson

TINY TELECOMM MODULE INTEGRATES T1/CEPT STANDARDS

The T1/CEPT Line Card from Dallas Semiconductor (Dallas, TX, (214) 450-0400) is a CMOS chip set that meets both the T1 (North American) and the CEPT (European) telecommunications standards. Mounted on a circuit board that's about the size of a stick of chewing gum, the four chips that make up the circuit include the DS2187 receive-line interface, DS2180A T1 transceiver or DS2181A CEPT transceiver, DS2175 elastic store, and DS2186 transmit-line interface. Because of the design of this modular board, only minor modifications are needed to convert your telecommunications equipment for access to either the T1 or the CEPT network—so telecommunications equipment built with the board can be offered on the international market.

In the event of a revision in either the T1 or the CEPT standard, the manufacturer can make the board meet the new requirements by replacing a single chip. Accordingly, you can concentrate on the design requirements of your equipment rather than preoccupying yourself with unstable telecommunication standards. You can buy the T1/CEPT Line Card for $98 (5000). The manufacturer also offers application notes and $100 designer kits for the chip set.—J D Mosley

C++ COMPILER RUNS ON IBM PCs AND COMPATIBLE COMPUTERS

Zortech (Arlington, MA) will start shipping its $99.95 C++ compiler for IBM PCs and compatible computers in April. Initially developed by AT&T Bell Laboratories, the C++ language is a superset of the C language that incorporates a new data type called "classes." Zortech claims that its compiler, which is compatible with the Codeview source debugger from Microsoft (Bellevue, WA), is the first true C++ compiler to be released for DOS-based machines.—Steven H Leibson

NEWS BREAKS

MID-SIZE LCD CONTROLLER EASES DISPLAY DEVELOPMENT

Cybernetic Microsystems (San Gregorio, CA, (415) 726-3000) has introduced a window-based controller for liquid-crystal displays (LCDs). The CY325 LCD Windows Controller provides a high-level interface between your μP or μC and a mid-size LCD module (240×64 pixels or smaller). The window capability lets you easily create sophisticated user interfaces. Once a window is created, you send data to the display; it appears only in the active window. The CY325 provides separately controlled graphics and text planes. Six softkeys interface directly to the controller, which tells the user when it detects a keystroke. It ignores further keystrokes until your software acknowledges the first keystroke. Communication with the controller can take place via a parallel or serial interface, or both. The CY325 is available in a 40-pin DIP and costs $20 (1000).
—David Shear

LOW-COST TMS320C25 DSP EMULATOR SPECS 40-MHz DEBUGGING

If you've been waiting for a low-cost in-circuit emulator for the TMS320C25 DSP chip, consider the $1995 320C25 ICE Pak from Memocom (Carrollton, TX, (214) 446-9906). This 3.5×5.6-in.[2] unit replaces the target DSP chip in systems under development and lets you perform real-time emulation and debugging at clock speeds reaching 40 MHz. For the basic price, the unit comes with 16k words of 35-nsec static RAM for zero-wait-state program memory; communication software; and a monitor/debug command set in firmware that includes a disassembler, set and clear break-point capability, single-step trace, display and modification of memory and I/O, and a command to copy external program ROM to the emulation space.

To obtain more program memory, you can buy a $2495 version of the ICE Pak that has 64k words of 35-nsec static RAM. Or, for $2995, you can purchase an upgraded version that includes 64k words of program memory and 512 words of memory for forward or reverse real-time trace. The emulator plugs into any host computer or terminal that has an RS-232C port, and it can communicate as fast as 19.2k baud.—J D Mosley

FLOATING-POINT CHIPS WILL EXPAND 56000 DSP FAMILY

By the end of 1988, Motorola (Phoenix, AZ) expects to have prototypes of two 32-bit floating-point chips that will eventually join the 24-bit DSP56001 DSP chip as part of the company's line of digital-signal-processing (DSP) chips. Already designated DSP96001 and DSP96002, the new chips will provide both single-precision and single-extended-precision math operations that are compatible with the IEEE-754 standard. The manufacturer claims that the ICs will be compatible with both object and source code for its DSP56001 chip. Motorola now offers software-development tools that will be directly compatible with floating-point chips—when the chips are available. The ICs will fill two roles: The DSP96001 will suit stand-alone DSP applications, and the DSP96002 will operate as an attached processor for 32-bit μPs.—Jon Titus

MODEM CHIP SUPPORTS PROCESS-CONTROL DATA PROTOCOL

The 20C12 modem IC from NCR Microelectronics Div (Fort Collins, CO, (303) 226-9500) implements the highway addressable remote transducer (HART) communications protocol recently introduced by Rosemount Inc (Eden Prairie, MN). The HART protocol is designed for process-control applications; it allows pressure, temperature, and flow transducers to communicate with control-room equipment over twisted-pair wires in either multidrop or point-to-point topology. Sample quantities of the 20C12, which operates at 1200 bps and uses the standard Bell 202 modem modulation technique and frequencies, will be available in April, and production quantities will cost $9.50 (1000).—Steven H Leibson

NEWS BREAKS: INTERNATIONAL

ASIC AGREEMENT PROVIDES E-BEAM PROTOTYPES AND VOLUME SOURCING

Philips Components Div (Eindhoven, The Netherlands, TLX 51573) and European Silicon Structures (ES2) (Bracknell, UK, TLX 847724) have signed an agreement that will provide their customers with a rapid prototyping service and a volume source for ASICs implemented in Philips' 1.5-μm double-layer-metal CMOS process. By the end of 1988, the same facilities will be available for designs that use Philips' 1.2-μm CMOS process. Under the agreement, ES2 will provide the prototyping and low-volume production facility by implementing the Philips process rules on the E-beam direct-write equipment installed at ES2's factory in Aix-en-Provence, France. Philips will then provide customers with volume sourcing from its wafer-fabrication plants in Europe, the USA, and the Far East. As part of the agreement, ES2's E-beam technology will also be made available to Philips.—Peter Harold

FIELD BUS PROVIDES LOW-COST INDUSTRIAL NETWORKING

The Signatrans-ZM50 low-cost industrial network from Funke & Huster GmbH (Essen, West Germany, TLX 857637) allows you to transfer data among I/O modules on a simple 2-wire field bus or on telephone lines. You can connect as many as 256 intelligent stations, each supporting several I/O modules, to the network. All of these stations have equal priority, and they can communicate over the network on a point-to-point or selective-broadcast basis. When the network is in its simplest operating mode, assigning the same address to any input channel and any output channel causes data to be transferred automatically, via the network, between these input and output channels. Alternatively, you can operate the network with a handheld programming unit or with a communications processor that provides control and data logging via a terminal, and also provides a gateway to other systems. A typical station, with modules that provide analog and digital I/O capabilities, costs around DM 2000.—Peter Harold

SYSTEM LETS YOU LOCATE UNDERGROUND NETWORKS EASILY

The Lora (localization by radio) Beacon developed by Établissements Jousse (Jouy le Potié, France, TLX 780183) is an inexpensive system for marking and locating underground networks. To use the system, you bury markers containing LCR-type passive resonant circuits at selected points on the network. A transmitter/receiver unit tuned to the circuits' resonant frequency can locate the markers. The system thus eliminates the need for searching large-scale structural drawings or for digging. The Lora Beacon, which was originally developed for use with agricultural irrigation and drainage systems, can be used with any kind of underground network. It can also mark boundaries underground.

The marker is a resonant circuit sealed inside a 15-cm (outer diameter), 0.6-mm-thick plastic ring. The unit's ultrasonic weld is watertight, and the passive circuit requires no energy source, so the unit will last indefinitely. The transmitter/receiver operates at 40 kHz and is enclosed in a cast-aluminum housing; it's powered by rechargeable dry batteries. The antenna is protected by a molded, fiberglass-reinforced polycarbonate sheath. The entire assembly weighs only 2.1 kg. The markers cost Fr 64 (around $11.50) (100); the transmitter/receiver is Fr 15,000 (approximately $2600). Delivery from Paris is additional.—Joanne Clay

How To Wring Workstation-Level PCB Designs Out Of Your PC.

P-CAD's new Master Designer turns an ordinary PC into a full-fledged PCB workstation.

When you need to wring every drop of performance out of your next PCB design, you need Master Designer™ software.

Master Designer provides all the horsepower you'd expect only from workstations priced from $50K up to as much as $200K.

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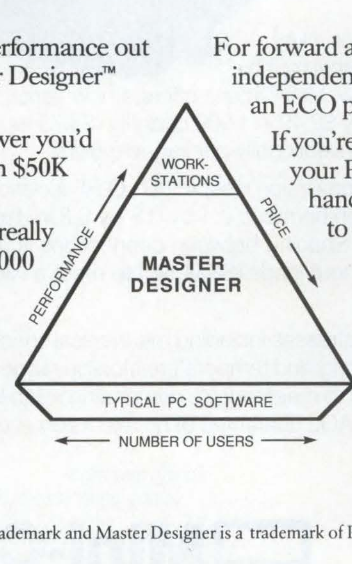
P-CAD's Master Designer routes multiple layers simultaneously cutting the number of vias and unrouted subnets in half.

So, you'll wring out cleaner designs and higher completion rates (up to 100%).



For forward annotation of logic changes and "history independent" back annotation, Master Designer also has an ECO processing option.

If you're interested in wringing every penny out of your PCB design station instead of wringing your hands, ring P-CAD. Let P-CAD show you how to turn a PC into a high-powered workstation.

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CIRCLE NO 189

SURFACE MOUNT MIXERS

$2.49 (1,000 qty)

The opportunity for automated, low-cost assembly is a key benefit of surface-mount technology, but is often wiped out by the high price of surface-mount components. Now, Mini-Circuits offers a new series of mixers to meet the pricing demands of SMT ... only $2.49 in 1,000 quantity ($3.75 ea. in quantity of 10) ... at a cost even lower than most conventionally-packaged mixers.

The SCM-1 spans 1 to 500MHz with only 6.0dB conversion loss, 45dB LO-RF isolation, and 40dB LO-IF isolation. Housed in a rugged, non-hermetic 0.4 by 0.8 by 0.3 in. high (maximum dimensions) plastic/ceramic package. Spacing between connections is 0.2 in. The mixer is offered with leads (SCM-IL) or without leads (SCM-INL) to meet a wide range of pc board mounting configurations.

Each SCM-1 is built to meet severe environmental stresses including mechanical shock/vibration as well as temperature shock. The operating and temperature storage range is −55°C to +100°C. Each SCM-1, designed and built to meet today's demanding reliability requirements, carries Mini-Circuits' exclusive 0.1% AQL guarantee of no rejects on every order shipped (up to 1,000 pieces).

When you think SMT for low-cost production, think of Mini-Circuits' low-cost SCM mixers.

SPECIFICATIONS (typical)	SCM-1L (with leads)	SCM-1NL (no leads)
FREQ. RANGE (MHz)		
LO, RF	1-500	
IF	DC-500	
CONVERSION LOSS (dB)		
Mid-Band (10-250MHz)	6.3	
Total Range (1-500)	7.5	
ISOLATION (dB)	(L-R)	(L-I)
Low-Band (1-10MHz)	60	45
Mid-Band (10-250MHz)	45	40
High-Band (250-500MHz)	40	35
PRICE	$2.49 (1,000 qty)	
	$3.75 (10-49)	

Units are shipped in anti-static plastic "tubes" or "sticks" for automatic insertion.

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setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
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CIRCLE NO 187

C115 REV. ORIG.

tough attenuators

one-piece design defies rough handling from $11.95 (1-49)

- Each unit undergoes high-impact shock test
- Unexcelled temperature stability, .002 dB/°C
- 2W max. input power (SMA is 0.5W)
- BNC, SMA, N and TNC models
- Immediate delivery, one-year guarantee
- **50 ohms, dB values,** 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 12, 15, 20, 30, and 40
- **75 ohms dB values,** 3, 6, 10, 15, 20 BNC only
- **Price** (1-49 qty.)
  CAT (BNC) $11.95 SAT (SMA) $14.95
  TAT (TNC) $12.95 NAT (N) $15.95

*Freq. (MHz)	Atten. Tol. (Typ.)	Atten. Change, (Typ.) over Freq. Range		VSWR (Max.)	
		DC-1000	1000-1500	DC-1000 MHz	1000-1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

*DC-1000 MHz (all 75 ohm or 30 dB models) DC-500 MHz (all 40 dB models)

Model Availability

SAT (SMA) CAT (BNC) NAT (N) TAT (TNC)

Model no. = a series suffix and dash number of attenuation.
Example: CAT-3 is CAT series, 3 dB attenuation.

Precision 50 ohm terminations only $6.95 (1-24)
DC to 2 GHz, 0.25W power rating, VSWR less than 1.1
BNC (model BTRM-50), TNC (model TTRM-50)
SMA (model STRM-50), N (model NTRM-50)

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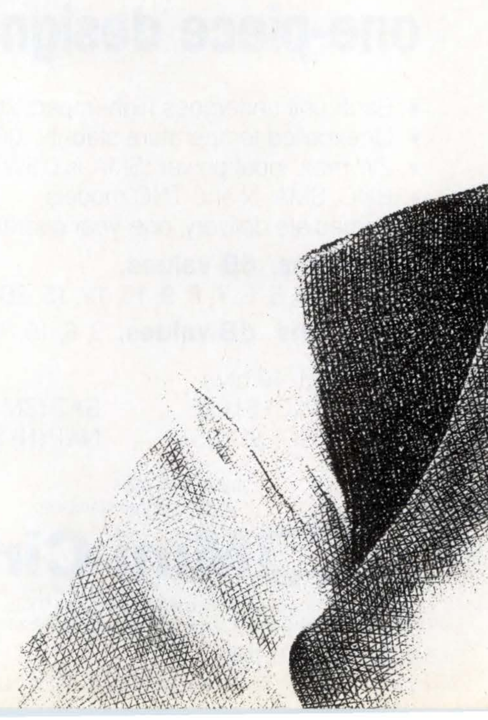
C 92 REV. C

"We don't plan to let VME rest on its laurels."

Shlomo Pri-Tal Manager, VME System Architecture and Technology



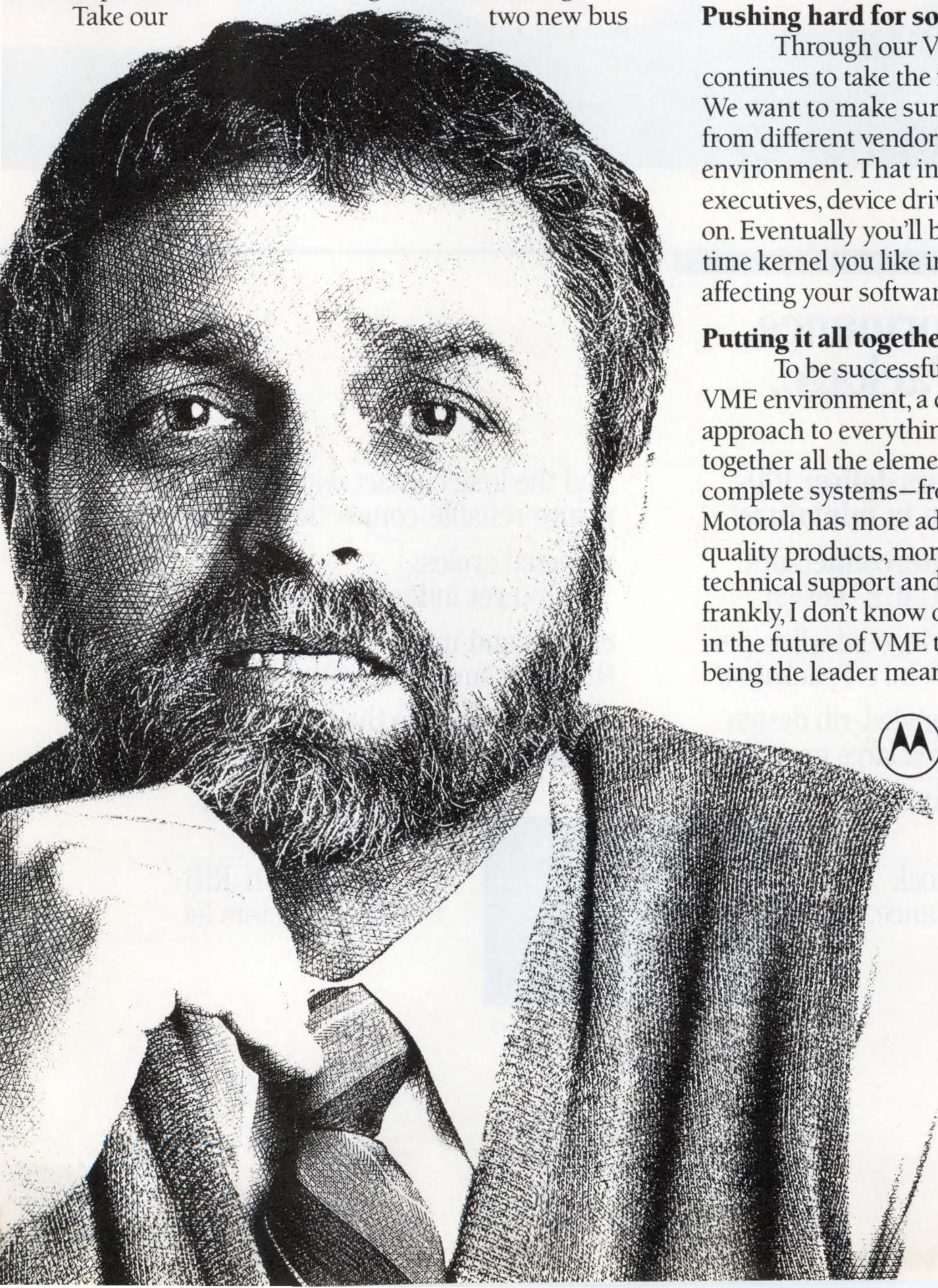
People think Motorola invented VME. Actually, a lot of companies had a hand in developing it. That's one of its main strengths: it's an *open architecture,* with no patents or copyrights to worry about.

Building open systems, to open markets.

In the long run, open systems benefit everyone. That's why we've always fought so hard for VME standardization through VITA, IEEE and IEC. Because standards create a very competitive market, where the OEM has literally thousands of VME choices—from Motorola and elsewhere.

Chipping away at interface standards.

These same standards have enabled Motorola to push bus hardware to higher levels of integration. Take our two new bus interface products, for example—the VME and VSB chips. They eliminate a major source of potential design errors for OEMs. So they can focus on *applications,* rather than bus interface problems.



Plugging in mainframe performance.

To maximize OEM product life cycles, you need a way to keep on plugging in new technologies, without obsoleting your current products. That's exactly what our 68000 family—within a VME architecture—does for you. Right now we have 020-based boards that are more powerful than the mainframes of 10 years ago. And 030 products that put the power of *today's* minicomputers on a desktop.

Pushing hard for software standards.

Through our VMEexec project, Motorola continues to take the initiative in standardization. We want to make sure VME software modules from different vendors work together in a common environment. That includes UNIX,® real-time executives, device drivers, network services, and so on. Eventually you'll be able to plug, say, any real-time kernel you like into a VME board—without affecting your software investment.

Putting it all together.

To be successful in today's more complex VME environment, a company has to take a systems approach to everything it does. That means putting together all the elements—chips, boards, software, complete systems—from a single reliable source. Motorola has more advanced technology, more high quality products, more software resources, more technical support and more VME experience. And frankly, I don't know of anyone who's investing more in the future of VME than Motorola. That's what being the leader means.

MOTOROLA

Microcomputer Division

Approaching our technology from your point of view.

CIRCLE NO 186

For reprints of this series,
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in California, 1-800-441-2345, Ext. 230.
Or write: Motorola Microcomputer Division,
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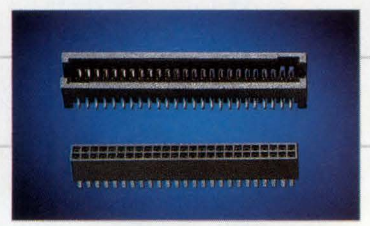
Big Performance. Little Package.

Rib-Cage connectors deliver 100-gram normal force in miniature/ microminiature interconnectors.

Du Pont's RIB-CAGE™ design lets you pack 0.100-in. centerline performance into 0.050-in. c/l packages.

Our patented angled-rib design creates a contact area large enough to produce a normal force of 100 grams, with remarkably high shock and vibration resistance.



Actual size of 50-position 0.050-in. (1.27-mm) vertical surface-mount RIB-CAGE card connector and mating male header.

And the long contact wipe helps assure reliable connections through repeated cycles.

You get inductance, capacitance and impedance values that are compatible with faster signal speeds (thanks to the 0.050 in. design), along with high current capacity and low circuit resistance.

In addition, RIB-CAGE connectors let

Comparison doesn't consider the long run

The editorial "Think big" by Jon Titus (EDN, December 24, 1987, pg 45) showed a lack of research. With regard to Apple's success story, it certainly started with Wozniak and Jobs. But Wozniak bailed out several years ago when Apple was becoming so big so rapidly, and Jobs was forced out a year or two later when it was obvious the direction he wanted to take the company in was contrary to its future success. It is very doubtful that the technical expertise of Wozniak or the entrepreneurship of Jobs could have come close to predicting (or "thinking big" enough about) the current state of Apple Computer. Sculley's skillful mid-course corrections are probably the chief reason the company is still on track toward greater success today.

The cheap shot taken at Tandy in this comparison of "thinking big" was completely unwarranted. While Apple's success story reads like a roller-coaster ride, Tandy's is one of executing a very well managed and thought-out long-range plan. Its consistent growth and introduction of new personal-computer products over the past 10 years earned it the front cover of *Byte*. Its current product line has such breadth and depth that it simply can't be denied that Tandy shares a leadership role in the personal-computer industry.

Michael Tierney
Vallejo, CA

(Ed Note: Mr Tierney missed the point of the editorial. The reference to Tandy and Apple was made to show the differences in their first computers, *not their continuing business.—Jon Titus)*

ATE vendor supports design for testability

I'm in hearty agreement with one point made by Jon Turino in his letter (EDN January 21, 1988, pg 32). I, too, believe that too many manufacturers still are not taking design for testability (DFT) seriously.

But in suggesting that my article "Cluster testing overcomes many testability problems" (EDN, October 15, 1987, pg 133) supports this disregard, Mr Turino has apparently missed the point of the article. The article addresses test engineers who have to live in the real world—which means they are still given boards with severe testability problems, and told to test them.

It's no good telling those engi-

neers that they might as well give up until DFT is fully realized. Nor does my discussion of available test solutions for here-and-now testability problems encourage a cavalier attitude towards DFT. Claiming that it does is a bit like saying that helping car-crash victims encourages reckless driving.

My colleagues at Teradyne and I strongly support DFT, and we pay it considerably more than "lip service." In fact, we're actively warning our customers that the day is fast approaching when boards without DFT will be untestable at any price. We're also urging customers to adopt well-thought-out DFT techniques such as scan-path and boundary-scan design; these techniques not only make a board observable and controllable, but also open the way to automating large portions of the test-development process.

Our confidence that scan design will gain rapid acceptance over the next few years, finally, is reflected by Teradyne's recent acquisition of Aida Corp. Aida's product line consists of design tools that specifically address scan and other DFT approaches.

May I also respond to Mr Turino's charge that articles like mine are evidence of some conspiracy on the part of automatic-test-equipment (ATE) vendors to foster a need for million-dollar-plus ATE? That price range is the domain of full-board functional testing, to which my article suggests an alternative: cluster testing. Cluster testing is usable in the context of a primarily in-circuit test approach, and it can typically be implemented with ATE hardware costing half as much as full-board functional-test equipment.

Steve Caplow
Teradyne Inc
Boston, MA

Correction

In the technology update "High-performance DMMs and calibrators bring standards-lab specs to the benchtop" (EDN, February 4, 1988, pg 57), the formula given on pg 62 is incorrect. Schlumberger specifies the long-term drift of its DMMs according to the formula:

$$(\text{ppm of reading})\cdot\sqrt{T},$$

where T is the time in years.

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

LOOK WHAT ELEVEN YEARS, 2 MILLION CPUs, AND 16 THOUSAND BOARD AND SYSTEM BUILDERS ARE DOING TO THE WORLD'S FIRST OPEN STANDARD BUS...

...THEY'RE MAKING IT STRONGER,
POWERFUL, AND MORE POPULAR

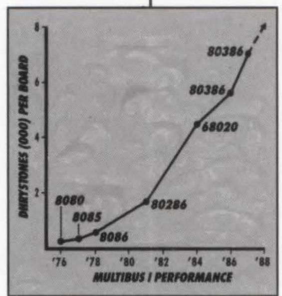
MULTIBUS I: TODAY'S MOST POPULAR, BEST SUPPORTED AND EASIEST TO IMPLEMENT OEM BUS.

Back in 1976 when Intel introduced Multibus I, it was 8-bits wide and supported the only major microprocessor then in existence, the 8080.

The world loved the open bus concept and jumped on the Multibus bandwagon. Quickly, Multibus I gained a level of acceptance that remains unequaled today.

1976: The debut of Multibus I. Few would have dared to predict the impact it would have on the world.

1986: The world's most powerful 32-bit microprocessor, the 80386, is introduced on Multibus I before any other bus.

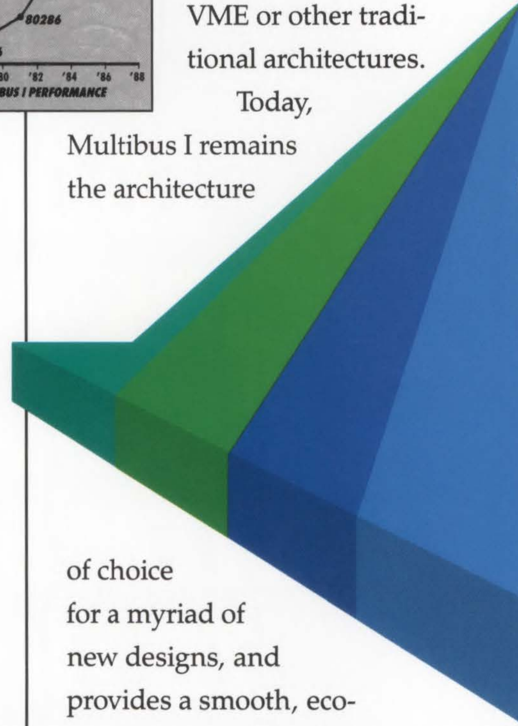


And, while Multibus I has remained true to its foundation as a solid, dependable standard, it has undergone a carefully controlled evolution that has produced a thoroughly modern architecture. One capable of supporting the newest 32-bit microprocessors, as well as the first Multibus board ever built, *in the same system!*

This unmatched compatibility, coupled with the ability to absorb new technology, has made Multibus I today's most popular, most versatile, best supported and easiest to implement OEM bus architecture.

FOUNDATION OF THE MULTIBUS FAMILY.

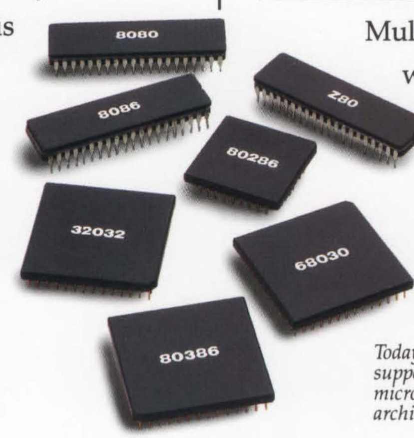
In 1982, Intel introduced Multibus II, a totally new *advanced* bus architecture designed not to replace Multibus I, but to open up entire new classes of applications impossible with Multibus I, VME or other traditional architectures.



Today, Multibus I remains the architecture of choice for a myriad of new designs, and provides a smooth, economical upgrade path for existing applications.

KEEPING PACE WITH TECHNOLOGY, WITHOUT COMPROMISING COMPATIBILITY.

Multibus I has done what no other architecture



Today's Multibus I supports every major microprocessor architecture.

WE'RE HERE FOR YOU!

The companies listed below would like you to know that Multibus I is alive and well and prospering. Multibus I offers the broadest product family. Plus scores of new products incorporating the very latest technology.

Whether you're developing new applications or upgrading existing ones, these industry leading companies offer a wide range of Multibus I products to give you the competitive edge. Today. And long into the future.

For your free Multibus I Data Book plus future new product announcements, just return the reader service card. Or for faster response, call the MMG or one of the participating companies listed below.

Discover the many *new* reasons Multibus I is today's most popular, most versatile, best supported and easiest to implement OEM bus.

Company	Address / Contact	CPUs	Digital I/O	Analog I/O	Special I/O	Periph Cont	Comm/Net	Graphics	Memory	Software	Packaging	Systems
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OMNIBYTE™	245 West Roosevelt Road West Chicago, IL 60185 Contact: Peter A. Czuchra (800) 638-5022 In IL: (312) 231-6880	•	•		•	•	•			•		•
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SBE, INC. MICROCOMPUTER BOARDS AND SYSTEMS	2400C Bisso Lane Concord, CA 94520 Contact: Sales Admin. (415) 680-7722 TWX 910-366-2116	•	•		•	•	•	•		•	•	•
ZERO Electronic Solutions UNIT OF ZERO CORPORATION	6790 Flanders Drive San Diego, CA 92121 Contact: Frank Hom (800) 854-7086 In CA: (800) 772-7086								•		•	
ZERO SCANBE UNIT OF ZERO CORPORATION	3445 Fletcher Avenue El Monte, CA 91731 Contact: Mike Burton (800) 227-0557 FAX (818) 444-3953										•	
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MUPAC®	10 Mupac Drive Brockton, MA 02401 Contact: Steve Cobb (617) 588-6110 FAX (617) 588-0498										•	

Use this convenient product reference guide to quickly locate the companies that offer the types of Multibus I products you need.

CIRCLE NO. 98

The Multibus Manufacturers Group, or MMG, is dedicated to the proposition that everyone benefits from strong, open standards. Membership is open to hardware and software manufacturers, application integrators, end users and even students.

To learn more about what the MMG can do for you, contact Dan Fink, MMG executive director.

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CIRCLE NO 150

DC TO 6 GHZ TRANSIENT EVENT CAPTURE. A WORLD WHERE TEK STANDS ALONE.

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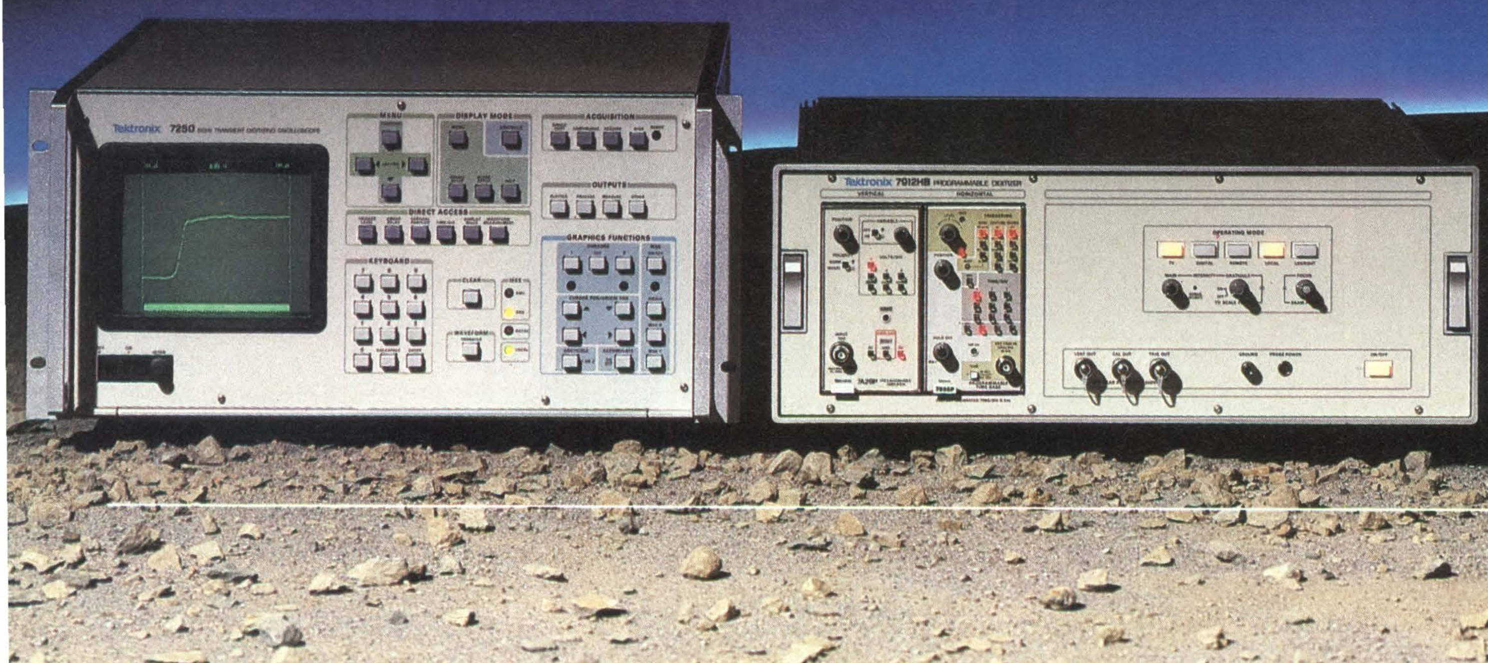
No other digitizing oscilloscope can automatically capture and record lightning-fast events whether single-shot or low-rep rate that more and more applications—from particle physics and lasers to semiconductor characterization—regularly encounter.

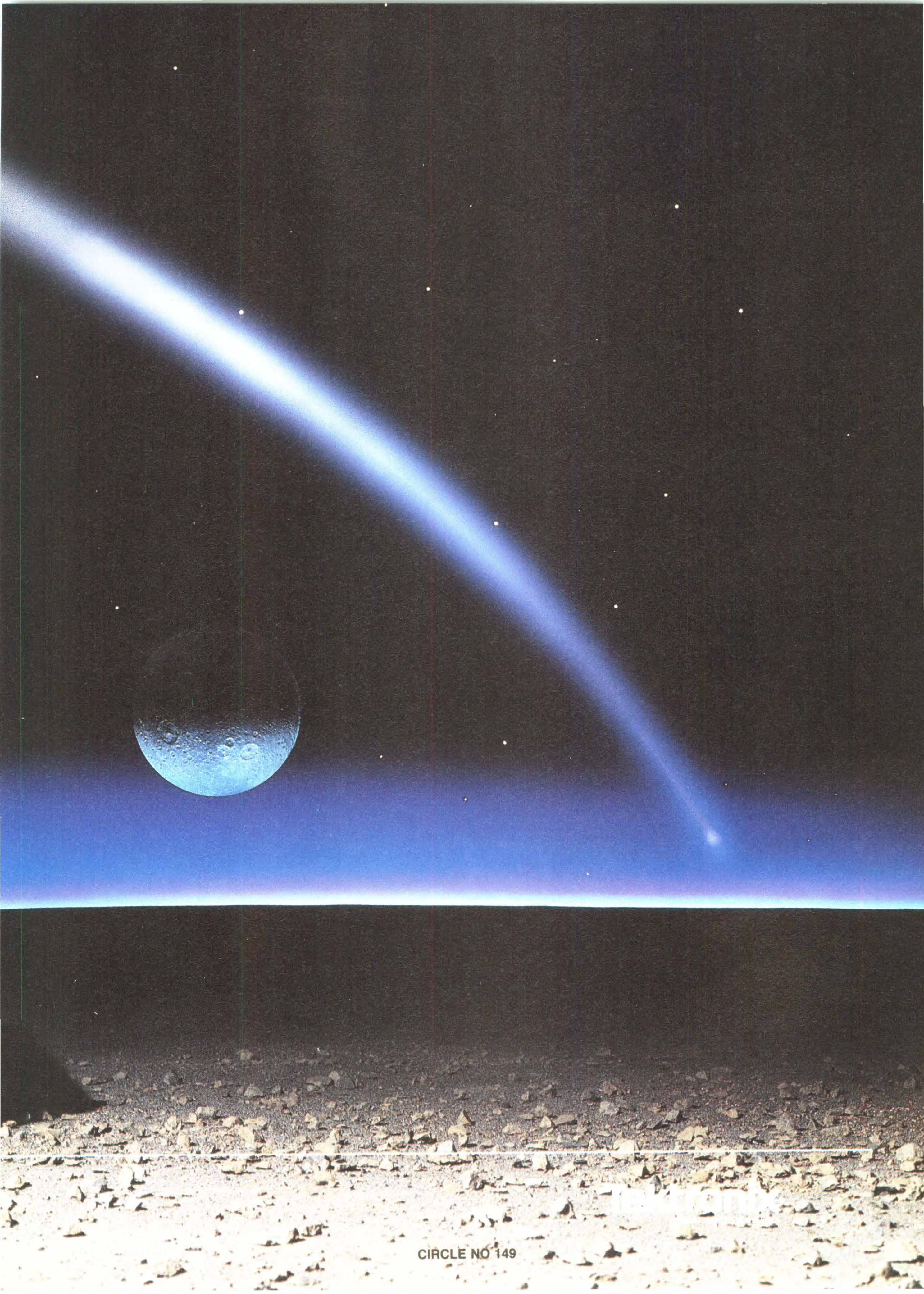
The 6 GHz Tek 7250 can capture transients of 50 ps rise time at 1 picosecond/point; with 11-bit vertical and 9-bit horizontal resolution. Menu-driven, with on-board measurements and integral monitor, it is easily the highest performance transient digitizing oscilloscope ever made.

The Tek 7912HB achieves 10 ps/point time resolution, allowing capture of events with transitions of less than 575 ps. In addition to its 750 MHz analog bandwidth, triggering capabilities and 10 waveform-per-second data transfer rate, the 7912HB offers the plug-in module flexibility of a Tek laboratory oscilloscope, such as the new 7A29P programmable amplifier.

Characteristics	7250	7912HB
Analog Bandwidth	6 GHz	750 MHz
Rise Time	50 ps	575 ps
Fastest Time/Point	1 ps/pt.	10 ps/pt.
Max. Points/Second	1000 GS/s	100 GS/s
Vertical Resolution	11 bits	9 bits
Input Signal Range Vertical	5V full scale, 10 divisions	80mVto 8V full scale, 8 div.
Input Sensitivity	500mV/div.	10mV/div. to 1V/div.
Fully Programmable	Yes	Yes

For more information on the world of Tek digitizing, call 1-800-835-9433. Or contact your Tek representative.




CIRCLE NO 149

CALENDAR

Digital Signal Microprocessor and Microcomputer Chips and Development Systems (seminar), Cambridge, MA. Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. April 4 to 6.

Worst-Case Circuit Analysis (seminar), Orlando, FL. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. April 4 to 6.

Microcircuit Interconnections and Assembly Methods (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 7.

Association for Information and Image Management (AIIM) Show, Chicago, IL. AIIM, Box 1059, Belmont, CA 94002. (301) 587-8202. April 11 to 14.

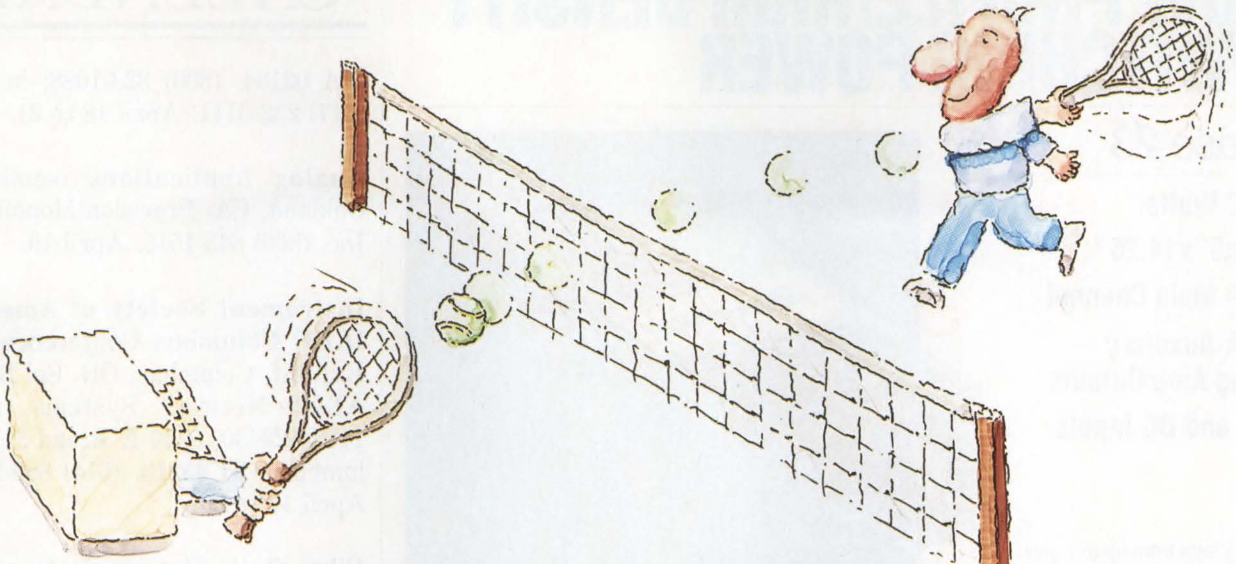
Electrostatic Discharge (ESD): Concern or Over-concern? (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 12.

Hybrid Microcircuit Technology (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 18.

American Power Conference, Chicago, IL. Robert Porter, Chicago Institute of Technology, Chicago, IL 60618. (312) 567-3202. April 18 to 20.

Worst-Case Circuit Analysis (seminar), San Diego, CA. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. April 18 to 20.

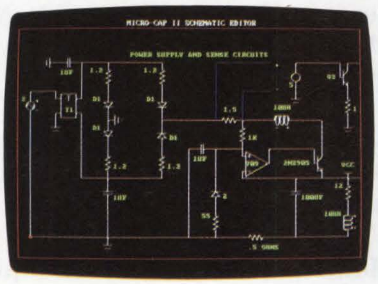
4th International Integrated Services Digital Networks Exposition, St Louis, MO. Information Gatekeepers, 214 Harvard Ave, Boston,



MICRO-CAP II.™
The CAE tool with fully interactive analog simulation for your PC.

Spectrum Software's MICRO-CAP II® is fast, powerful, and feature rich. This fully interactive, advanced electronic circuit analysis program helps engineers speed through analog problems right at their own PCs.

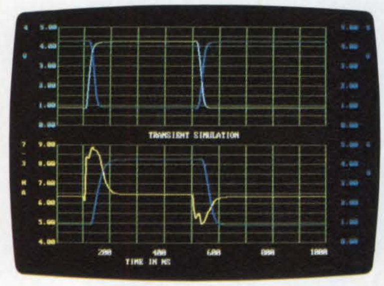
MICRO-CAP II, which is based on our original MICRO-CAP software, is a field-proven, second-generation program. But it's dramatically improved.



Schematic Editor

MICRO-CAP II has faster analysis routines. Better resolution and color. Larger libraries. All add up to a powerful, cost-effective CAE tool for your PC.

The program has a sophisticated integrated schematic editor with a pan capability. Just sketch and analyze. You can step component values, and run worst-case scenarios—all interactively. And a 500-type* library of standard parts is at your fingertips for added flexiblity.



Transient Analysis

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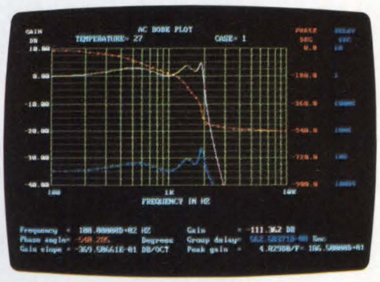

AC Analysis

spectrum

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CIRCLE NO 148

CALENDAR

MA 02134. (800) 323-1088; in MA, (617) 232-3111. April 18 to 21.

Analog Applications (seminar), Oakland, CA. Precision Monolithics Inc, (800) 843-1515. April 19.

Instrument Society of America/IEEE Columbus Conference and Exhibit, Columbus, OH. Sol Black, AT&T Network Systems, Dept 11CB123430, 6200 E Broad St, Columbus, OH 43213. (614) 860-5605. April 19 to 20.

Fiber Optic Communication Systems (short course), Washington, DC. Integrated Computer Systems, 5800 Hannum Ave, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. April 19 to 22.

IEEE Instrumentation/Measurement Technology Conference (IMtc/88), San Diego, CA. Bob Myers, IMtc, 1700 Westwood Blvd, Los Angeles, CA 90024. (213) 475-4571. April 19 to 22.

Troubleshooting Microprocessor-Based Equipment and Digital Devices (seminar), Milwaukee, WI. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. April 19 to 22.

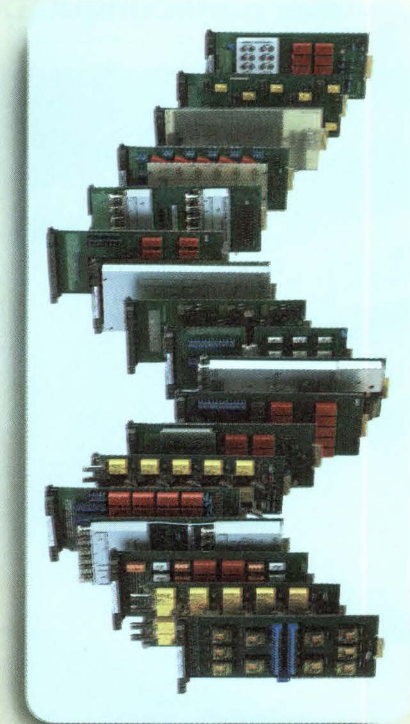
Modern Electronic Packaging (seminar), Raleigh, NC. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. April 20 to 22.

Analog Applications (seminar), Boston, MA. Precision Monolithics Inc, (800) 843-1515. April 21.

Modern Microwave Techniques (short course), Los Angeles, CA. UCLA Extension, 10995 Le Conte Ave, Los Angeles, CA 90024. (213) 825-3344. April 25 to 28.

KEITHLEY ON SWITCHING:

IT'S IN THE CARDS



Our line of 18 signal switching cards is the widest variety anywhere, so you can configure a system to match your signal types without sacrificing system performance.

SIGNAL INTEGRITY

To get the most from your test system, you must make sure your signals are switched without attenuation, distortion or alteration by the switching and interconnect. Since Keithley has more switching cards than anyone, you can be assured of signal integrity, no matter what the test. Choose from:

Matrix	Most flexible
Scan/Multiplex	1, 2, or 4 pole switching
Sensitivity	Currents to 40fA, voltages to 30nV
High Level	Currents to 5A, voltages to 1000V
Bandwidth	Frequencies to 500MHz
Temperature	Thermocouple cards with $<1\mu V$ offset and built-in reference
Special Applications	Hall effect, nanovolt switching, Kelvin switching, universal adapter

Each of these switching capabilities is referenced in our new Switching Handbook.

SYSTEM INTEGRATION

Keithley switches let you customize applications by mixing cards in two or 10-slot mainframes. For larger systems, you can connect up to five mainframes and program them at one IEEE-488 address.

Keithley switching further simplifies system integration with digital I/O, triggers in/out, relay setup memory, inspect mode for determining relay configuration, and more.

SYSTEM PERFORMANCE

Our products are designed for compatibility, and you'll find the proof in easier system integration and smoother performance. And in addition to switching, we also supply the full range of programmable measurement and source instrumentation for many test requirements. Plus, our Application Engineering Department is always available to help you select the right instruments and configure them for peak system performance.

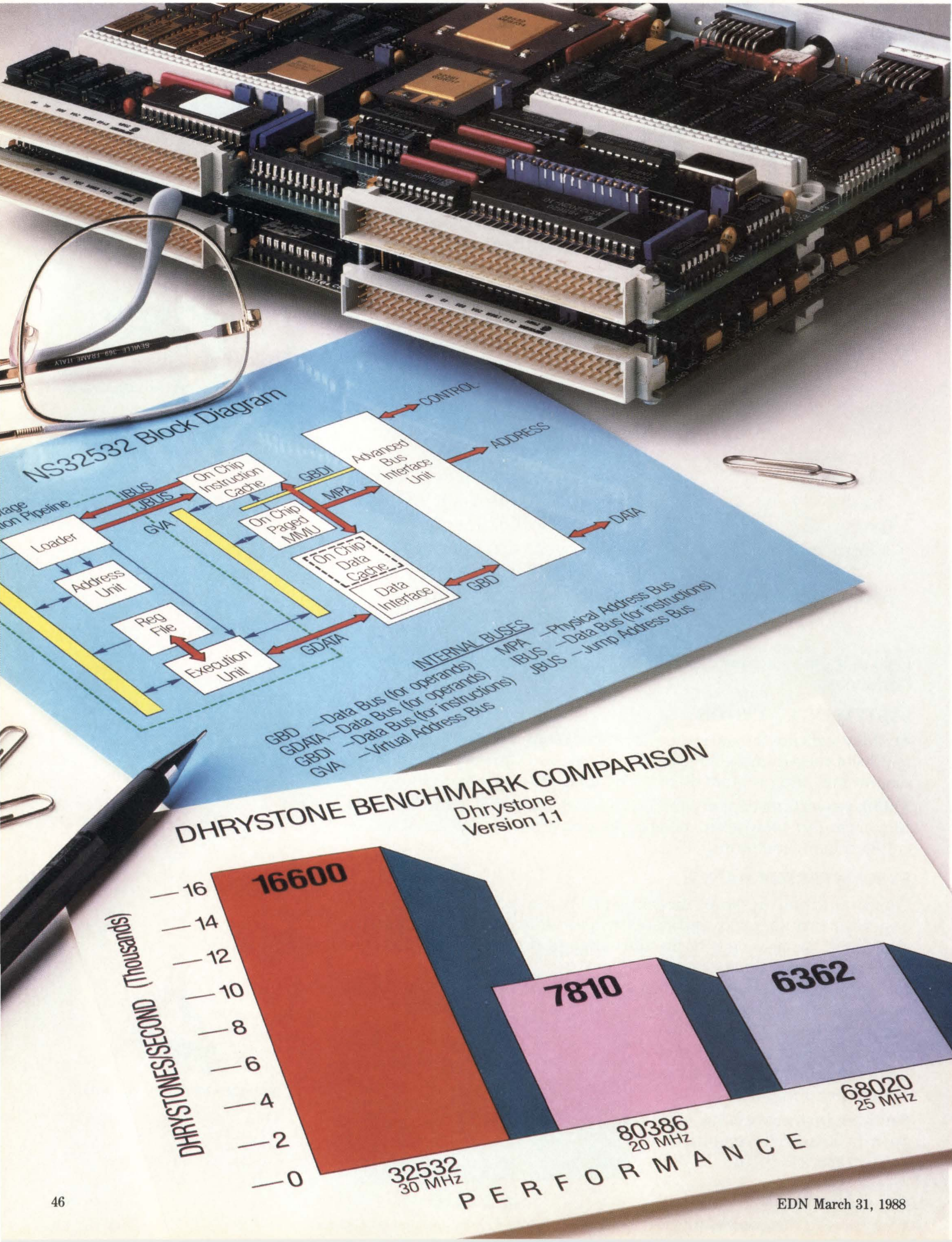
Keithley Instruments Inc., 28775 Aurora Road, Cleveland, Ohio, 44139. (216) 248-0400.

Call or write the Information Center for more on Programmable Switches, Sources, and Measurement instrumentation. Then find out how to receive your free copy of Keithley's new Switching Handbook with useful information and practical guidelines on getting maximum performance from your test system.

SOURCE • MEASURE • CONNECT

KEITHLEY

CIRCLE NO 147


NS32532 Block Diagram
CONTROL
ADDRESS
DATA
GBD
Advanced Bus Interface Unit
On Chip Instruction Cache
On Chip Paged MMU
On Chip Data Cache
Data Interface
Loader
Address Unit
Reg File
Execution Unit
IBUS
JBUS
GVA
GBDI
MPA
GDATA
Pipeline
INTERNAL BUSES
GBD —Data Bus (for operands)
GDATA—Data Bus (for operands)
GBDI —Data Bus (for instructions)
GVA —Virtual Address Bus
MPA —Physical Address Bus
IBUS —Data Bus (for instructions)
JBUS —Jump Address Bus
DHRYSTONE BENCHMARK COMPARISON
Dhrystone
Version 1.1
DHRYSTONES/SECOND (Thousands)
16
14
12
10
8
6
4
2
0
16600
7810
6362
32532
30 MHz
80386
20 MHz
68020
25 MHz
PERFORMANCE

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The NS32532: Real-world performance for real-world applications.

At National, we believe that a high-performance 32-bit microprocessor should be worked with, not around.

That's why the NS32532 offers you some of the highest performance specs in the industry.

Yet it's performance you can *use.* Because the NS32532 was created for real-world designers working on real-world systems to meet real-world needs.

PERFORMANCE YOU CAN COUNT ON

The NS32532 is capable of delivering 15 MIPS peak performance, 8-10 MIPS sustained, at 30 MHz.

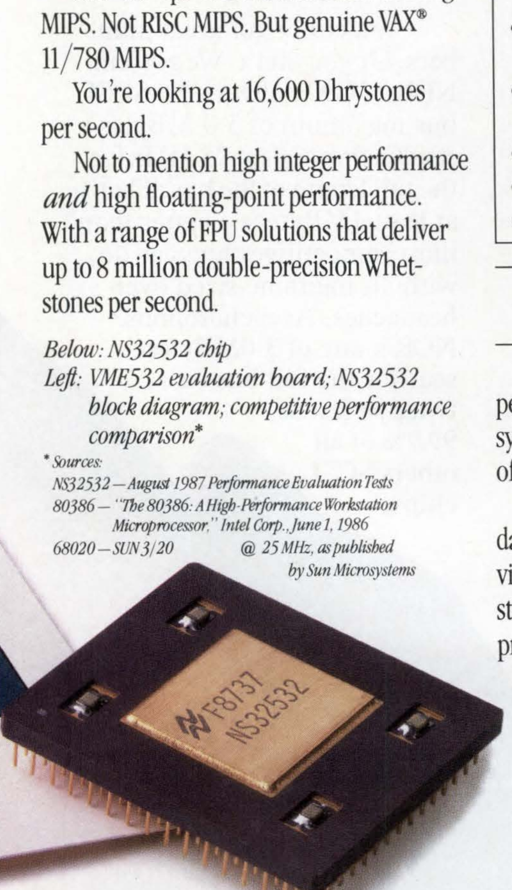
Not "no-ops" MIPS. Not benchmarking MIPS. Not RISC MIPS. But genuine VAX® 11/780 MIPS.

You're looking at 16,600 Dhrystones per second.

Not to mention high integer performance *and* high floating-point performance. With a range of FPU solutions that deliver up to 8 million double-precision Whetstones per second.

Below: NS32532 chip
*Left: VME532 evaluation board; NS32532 block diagram; competitive performance comparison**

* *Sources:*
NS32532 — August 1987 Performance Evaluation Tests
80386 — "The 80386: A High-Performance Workstation Microprocessor," Intel Corp., June 1, 1986
68020 — SUN 3/20 @ 25 MHz, as published by Sun Microsystems



The NS32532

- 8-10 MIPS sustained, 15 MIPS peak
- 20-, 25-, and 30-MHz devices
- On-chip 1,024-byte 2-way set associative physical data cache
- On-chip 512-byte direct mapped physical instruction cache
- Hardware cache invalidate for high-performance cache coherency
- On-chip demand-paged memory management including 64-entry fully associative Translation Lookaside Buffer
- 4-stage instruction pipeline including instruction prefetch and branch prediction
- 2-clock basic READ/WRITE cycle
- 1-clock burst-mode transfers
- Unique bit-manipulation and string-handling instructions
- Highly symmetrical and orthogonal instruction set producing compact code
- Extremely fast context switch (3.6 μs) and interrupt service (1.3 μs)
- Fabricated in M^2CMOS
- 370,000 transistor sites
- SAMPLES AVAILABLE NOW

SUPER-MINI PERFORMANCE ON A CHIP

The NS32532 achieves its superior performance because it integrates key systems functions on a single piece of silicon.

Only the NS32532 incorporates on-chip data and instruction caches, demand-paged virtual memory management, and a 4-stage instruction pipeline. With instruction prefetches and branch prediction. Plus a hardware cache invalidate mechanism that ensures cache coherency.

SCALABLE PERFORMANCE

The NS32532 is one of seven CPUs based on the same 32-bit architecture. With the same orthogonal, highly symmetrical instruction set.

Which means you can migrate your design throughout the entire performance range without having to re-engineer your software at any level. And you can build consistently competitive systems without resorting to some "more innovative" architecture that leaves you and your software investment in the lurch.

PERFORMANCE THAT'S READY FOR YOU TODAY

We've already begun sampling silicon. We've already ported UNIX® System V.3 and VRTX.® And we've already produced a board-level implementation — a fully integrated, fully populated, plug-and-go VME-compatible native environment... available now for evaluation. So are nearly 150 other members of the Series 32000® family, including coprocessors, peripherals, development tools and optimizing compilers.

To talk about putting our performance into practice in your application, call our Application Engineers toll free: **800/538-1866, ext. 532 or 800/672-1811, ext. 532** (within California).

National Semiconductor

CIRCLE NO 146

NCR keeps standards

Command	SCSI Bus Sequences	53C90	Competitor
Wait for Select and Receive	Selection to ID message	0.7µs	—µs
	ID message to 1st CDB	0.7µs	—µs
	1st CDB to Disconnect message	2.6µs	—µs
	6th CDB to Disconnect message	0.9µs	—µs
	Disconnect message to Bus Free	0.2µs	—µs
Reselect and Transfer	Reselection to ID message	4.2µs	—µs
	ID message to 1st Data Byte	0.6µs	—µs
	Data Transfer	—	—
	Last Data Byte to Status	0.2µs	—µs
	Status to Command Complete	0.9µs	—µs
	Command Complete to Bus Free	0.2µs	—µs
Total SCSI Bus Overhead Time		**11.2µs**	**372µs***

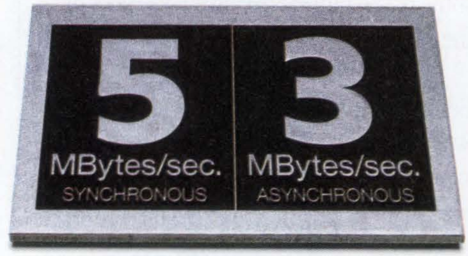
SCSI Bus Phase Overheads

Finally, a cure for SCSI overheadaches.

NCR's 53C90 is the only chip that can give you fast, fast, fast relief from overheadaches . . . and that includes the newest "A" and "6250" versions from the competition.

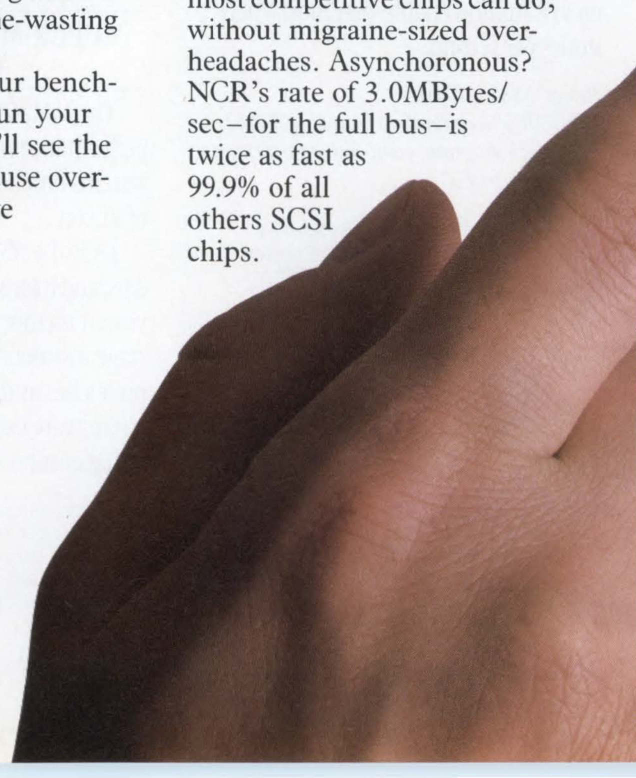
Using combination commands, dedicated sequential logic and dual-ranked registers for command pipelining, the 53C90 is magnitudes faster on and off the bus. Plus NCR implements complex bus sequencing in hardware, not time-wasting software.

Here's our benchmarks. But run your own and you'll see the other guys cause overheadaches, we cure them.



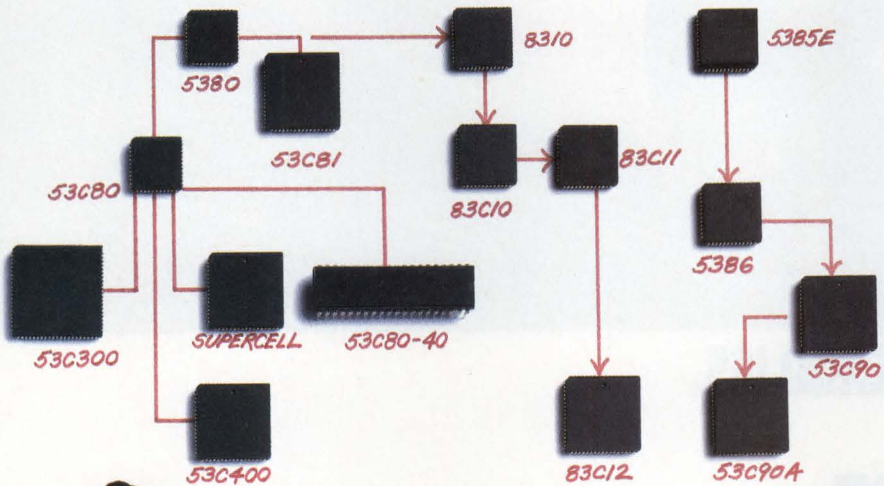
How our data transfer rates rate.

You either got great numbers. Or you don't. We got 'em. NCR 53C90 delivers the SCSI bus maximum of 5.0 MBytes/sec synchronous at 25 MHz for the full length of the bus. That's at least 1MByte/sec better than most competitive chips can do, without migraine-sized overheadaches. Asynchoronous? NCR's rate of 3.0MBytes/sec–for the full bus–is twice as fast as 99.9% of all others SCSI chips.



*Electronics Magazine August 20, 1987 Pg. 65

raising the for SCSI.



A big well-connected family.

Other suppliers can't show you much of a family tree compared to NCR. That's because NCR goes back to the "Mayflower" of SCSI controllers with the 5385 in 1982. The most recent offshoot of that original line is the high-performance 53C90A. Consistent with good family planning the software for the 53C90 is similar to our 5385 and 5386, so you can quickly convert to the 53C90. A single chip host bus adapter (53C400), integrated buffer controller (53C300) and an ASIC supercell fill out our product offering. And you can bet we'll be there when you need SCSI II.

How to get zap-resistance, latch-up protection and the blessings of the FCC.

For example, the NCR 5380 and 53C90 families give you ESD protection up to 10,000 volts on the SCSI bus. NCR also provides controlled fall times to reduce the undershoot that could cause other CMOS chips to latch-up. Controlled assertion rates also reduce generated RFI, an important factor in winning FCC approval for the final product.

It's time to raise your standards.

In SCSI, it's not so much if you implement the standard, but how. Because our chips have an edge over other chips from other manufacturers, they can help give you and your product an edge in the market. We've shipped more than 3-million 5385's and 5380's and production quantities of the 53C90. If you don't want to just settle for the standard, call NCR today.

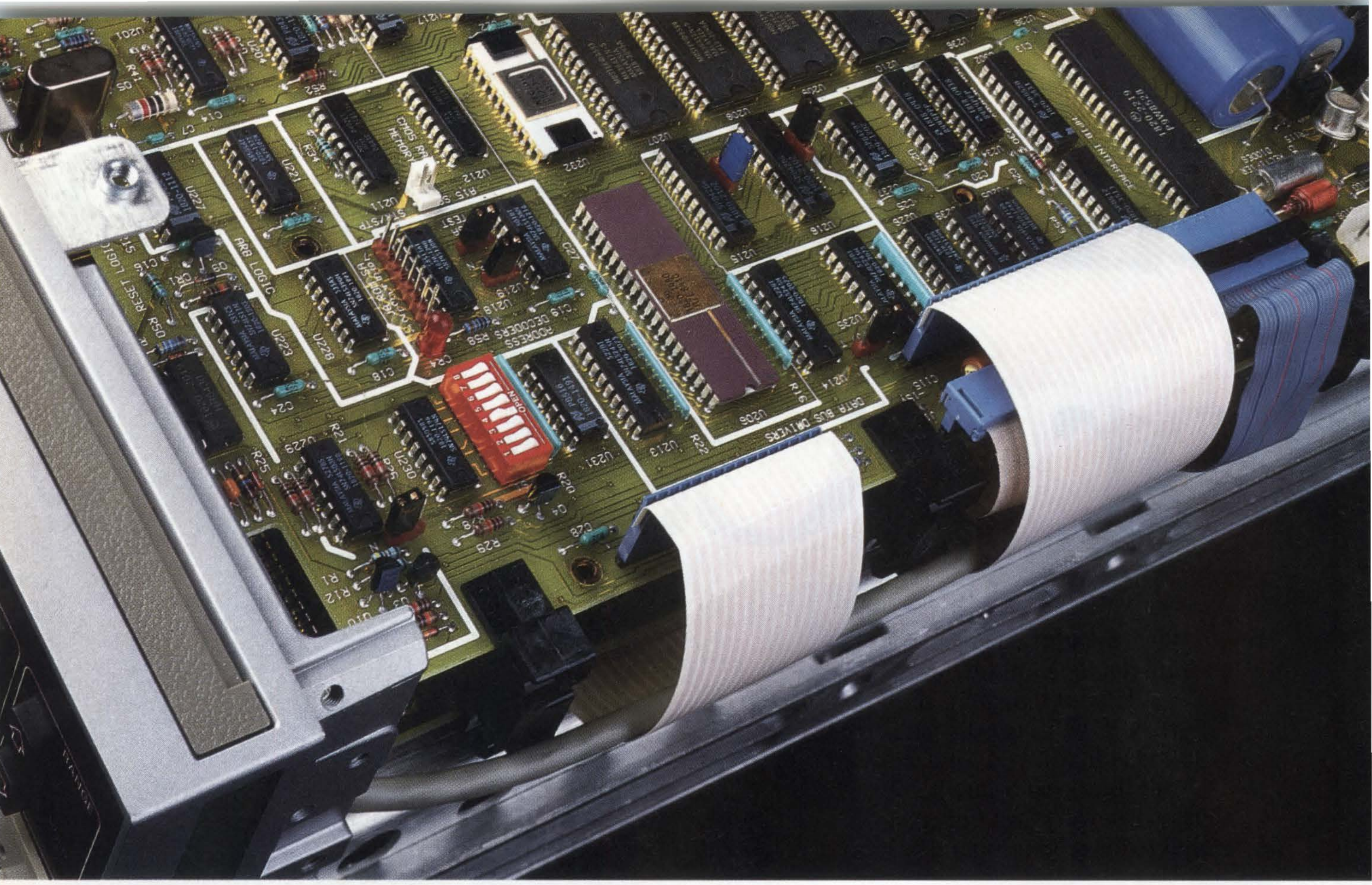
For documentation call our hot line 1-800-334-5454. Or write to, NCR Microelectronics, SCSI Products, 1635 Aeroplaza Drive, Colorado Springs, CO 80916.

For technical assistance, call 800-525-2252, Telex 452457.

NCR

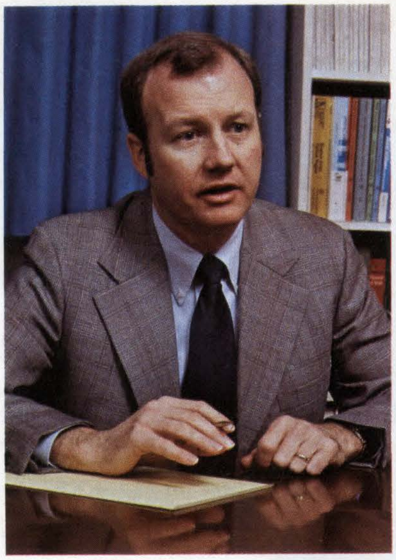
NCR Microelectronics Division

CIRCLE NO 145



EDITORIAL

Reading can be fun



Reading technical articles can be amusing if you learn how to read between the lines. In the spirit of April Fool's Day, here are comparisons of what authors say and what they actually mean:

WHAT THEY SAY:	WHAT THEY MEAN:
We can show that . . .	*Well, it's not at all clear to us, but we're shaming you into taking it for granted.*
It didn't operate as was predicted . . .	*It burst into flames.*
A high transient thermal effect . . .	*We burned our fingers on the 2N3055.*
After many experiments, we found a solution. . . .	*We fiddled with it for a long time and finally got it to work.*
A typical sample . . .	*The only time it did more or less what we wanted it to.*
We ran transient tests . . .	*The fuse blew every time we turned it on.*
As a first approximation . . .	*This value is flagrant guesswork.*
You can improve this method . . .	*Nothing we tried had a hope of working.*
Here are the fundamental engineering principles . . .	*We lifted this from another article.*
You can solve the equation numerically . . .	*We got eight answers that look vaguely right.*
It's interesting to compare . . .	*It isn't of the slightest interest, but it fills more space, we'll get paid more, and we can take a shot at Fred's article published in . . .*

EDITORIAL

However, you can't reach the theoretical maximum power output . . .	*You'll destroy all the output buffers if you adjust R_3 when the power is on.*
The gain figure is sub-optimal . . .	*It has no gain and the noise figure is 22 dB.*
We haven't optimized the amplifier's efficiency. . . .	*It's giving 2W out for 10W in and the output transistors are glowing red.*
Performance is extremely good.	*It worked for three hours and then died.*
We thank Joe Smith for his comments about our manuscript . . .	*Joe Smith completely rewrote the article at the last minute.*
The author's wish to thank Chris Hendrie for his comments about the manuscript . . .	*Chris gave us hell for using his dot-matrix printer so often.*
The authors want to thank Elizabeth Scott for her assistance.	*Ms Scott finally got the circuit to work.*

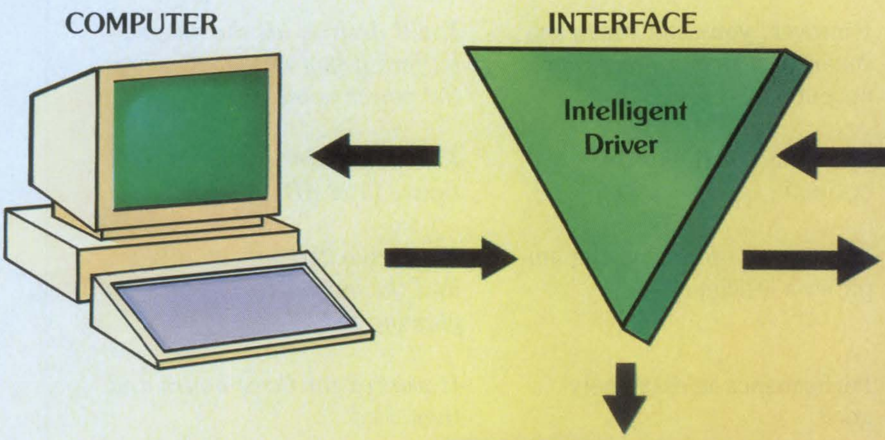
Well, I must confess a lack of originality. I've reproduced the comments above—with permission—from the December 1987 issue of *Radio Communication*, the journal of the Radio Society of Great Britain. The idea originated in *FM News*, the Central Scotland FM Group's newsletter.

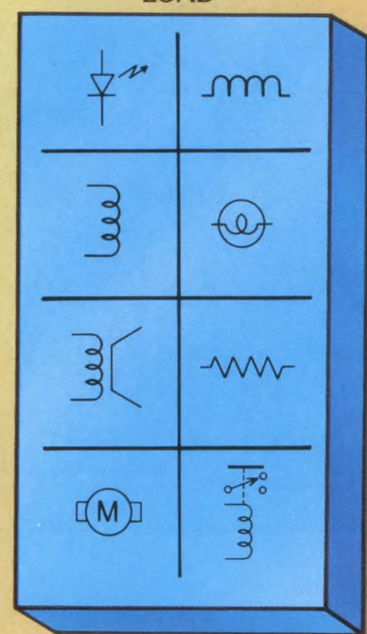
That's it until next year, when we look at press releases and ads . . .

Jon Titus

Jon Titus
Editor

Who Makes Power And Tough Enough For





POWER AMPLIFICATION

- From CPU small signals to power currents into the load
- Any input level accepted: TTL, CMOS, etc.
- Wide supply voltage range

LOAD CONTROL

- Load condition monitoring
- Resistive and highly inductive loads
- Dynamic stability with all loads

CPU FEEDBACK

- Output ON or OFF
- Alarm output
- Load conditions (open/short)

SAFETY FUNCTIONS

- No indeterminate states upon power on
- Current limitation
- Link disconnect
- Reset functions
- High noise immunity
- Thermal protection
- Overvoltage protection

SGS-THOMSON Microelectronics, of course.

In fact, engineers now have a full range of self protecting power devices capable of intelligently interfacing with computers.

No other industrial load driving solutions are simpler or more cost-effective. SGS-THOMSON integrates protection, diagnostic feedback and control functions on a single IC.

Short circuits, overloads, ground and load disconnection are no problem.

Meeting your demanding specs is no problem, either. SGS-THOMSON offers a full range of current ratings and configurations. Plus, you can choose from power packaging, mini-dip or surface mount ICs.

DEVICE	VCC max. (in V.)	I max. (in A.)
TDE1607	36	0.5
TDE1647	50	1.0
TDE1737	50	1.0
TDE1747	50	1.0
TDE1767	50	1.2
TDE1767A	60	1.2
TDE1787	50	1.2
TDE1787A	60	1.2
TDE1798	50	0.5
TDE3207	36	0.3
TDE3237	36	0.3
TDF1778	35	2.0
TDF1779A	35	2.0
UAF1780	35	2x2.5

SGS-THOMSON Microelectronics
1000 E. Bell Road, Phoenix, Arizona 85022

CIRCLE NO 134

Fiber-optic transmitters and receivers enhance data-link performance

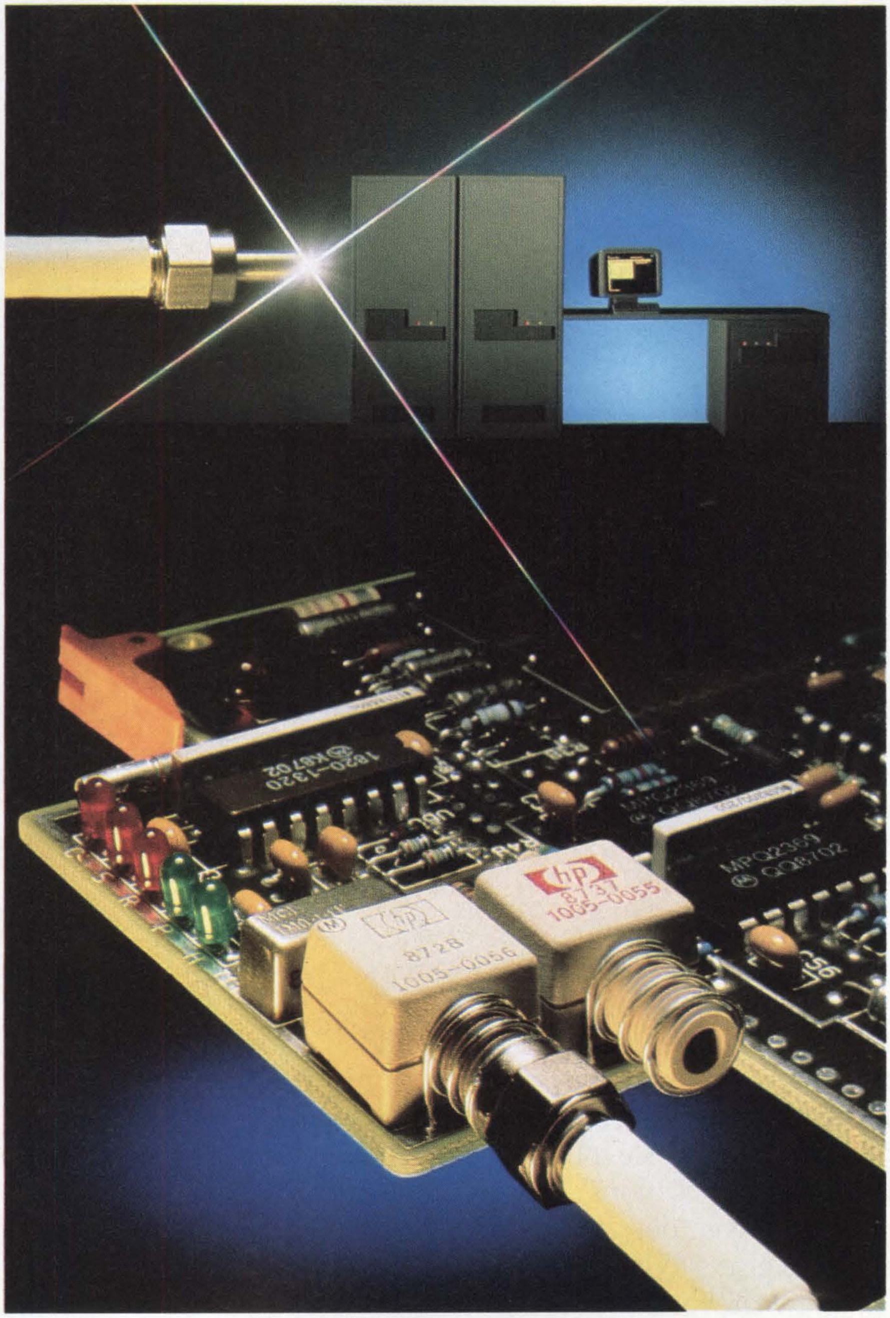
KEEPING AMERICA COMPETITIVE

Tom Ormond, *Senior Editor*

Off-the-shelf fiber-optic transmitter and receiver modules provide designers with a cost-effective way to significantly improve data-link transmission performance. Available in matched sets or as individual transmitters or receivers, these modules accommodate a spectrum of data rates that extends from dc into the gigabit-per-second range. They not only improve transmission bit error rates—BER figures of at least 10^{-9} are commonplace—but they also extend transmission-distance capabilities into the kilometer range and minimize EMI/RFI problems.

Moreover, these transmitter and receiver modules are user friendly—totally transparent in some cases. Whatever your application, you simply connect the fiber cable, apply appropriate power, and you're ready to transmit and receive data. And this user friendliness applies to short-distance computer-to-peripheral low-data-rate applications as well as long-distance, high-speed transmissions.

A look at some of the transmitter and receiver modules available today will best illustrate the design advantages they offer. The low end of the data-rate spectrum is an appropriate place to start.

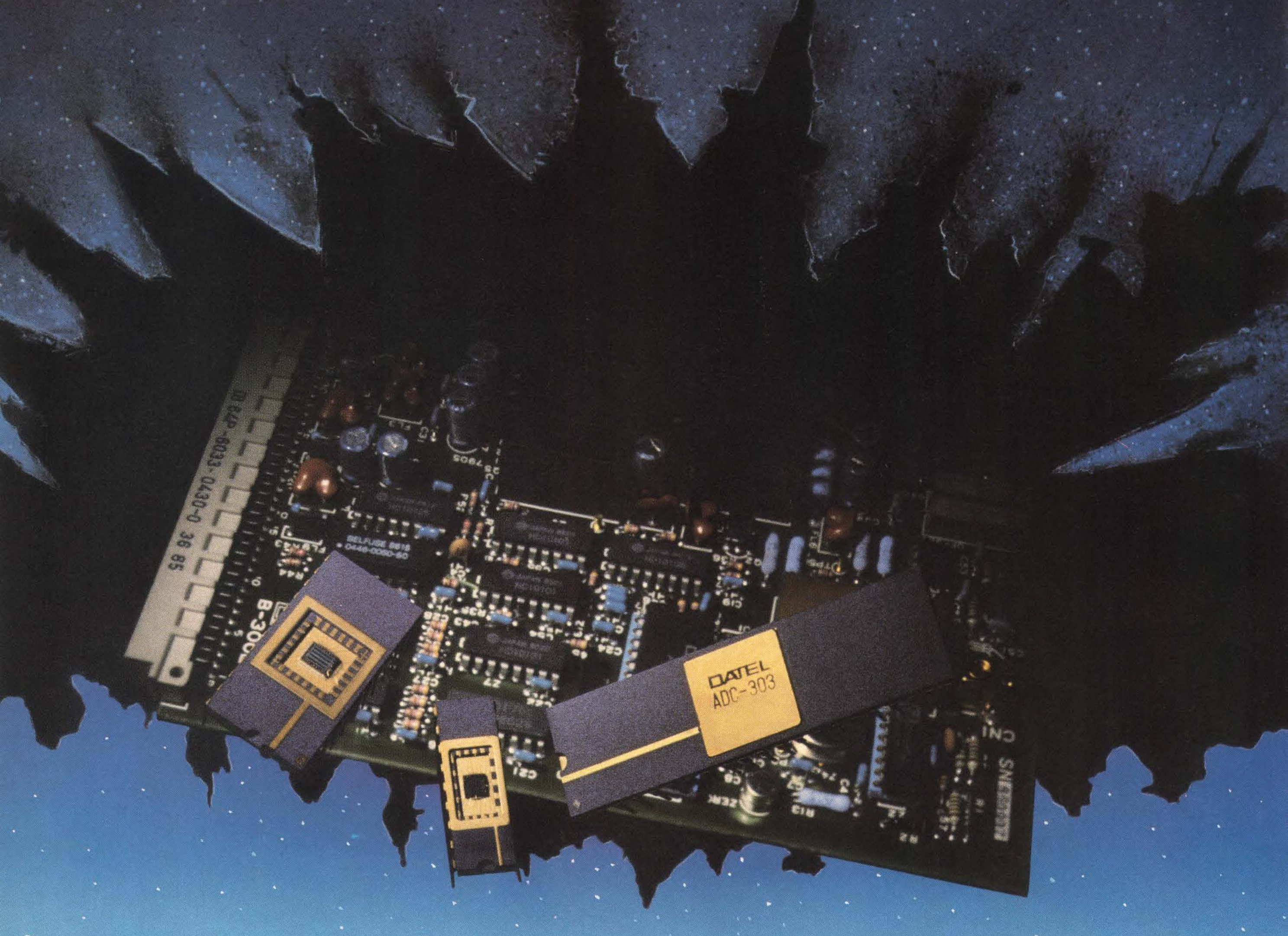


Capable of accommodating transmission distances of 3 km, *Hewlett-Packard's HFBR-24X6 receivers process data at 150M-bps rates and are available with either SMA- or ST-type connector ports.*

Handling computer interfaces

Eotec, Fibermux, Litton, and Thomas & Betts all offer products aimed at improving the computer-to-peripheral data-transfer interface. Eotec has developed a multiple-protocol Network Link transceiver, the 22-1004, which replaces conventional hard wire in RS-232C, RS-422, and TTL-format asynchronous data links and networks. The Network Link is also compatible with programmable controllers from Allen-Bradley, GE, Gould, Honeywell, Square D, and Westinghouse.

FLASH CONVERTERS



Break through to new performance levels

DATEL's broad range of Flash Converters provide you with tomorrows performance today! Performance features such as wide input bandwidths and low power consumption makes us the high reliability component supplier of choice for both commercial and military applications.

Speed up your designs with DATEL's Flash Converters today.

Call or write for information on all DATEL data conversion products. Call (617) 339-3000.

FLASH CONVERTERS			SAMPLING BOARDS	
MODEL	BITS OF RESOLUTION	CONVERSION RATE	SAMPLING RATE	MODEL
ADC-310	10	20 MHz	12 MHz	ADC-B310
ADC-300	8	20 MHz	16 MHz	ADC-B300
ADC-301		30 MHz	30 MHz	ADC-B301
ADC-302		50 MHz	50 MHz	ADC-B302
ADC-303		100 MHz	100 MHz	ADC-B303
ADC-304		20 MHz	20 MHz	ADC-B304
ADC-207	7	35 MHz	35 MHz	ADC-B207

DATEL

CIRCLE NO 133

LEADERS IN DATA CONVERSION TECHNOLOGY
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MIL-STD-1772
DATEL
Certified

The 22-1004 has master/slave switches that allow you to totally control the direction of optical and electrical signals in the network. In a data-link application, these switches allow you to select different formats at each end of the link without having to worry about any data conversion. An optional lockout feature permits multiple-point access from the terminal to the processor; an active terminal automatically locks out all other terminals until communication is complete.

The transceiver features a built-in repeater and provides 1200-ft transmission capability when using the company's industrial-grade fiber-optic cables (standard lengths start at 25 ft). The cost is $2390 per data link. Data rates (NRZ) range from dc to 1M baud, and the BER spec is 10^{-9}. The Network link operates over the range of 0 to 60°C. The 22-1004 is totally transparent so you can retrofit existing hard-wire systems without having to change any electrical connections.

The FX family of miniature modules from Fibermux ranges from a transparent DCE port extension to a 10M-bps high-speed asynchronous link. Each of the four products measures only 1.6×0.75×4.5 (or 5.5) inches.

The FX102 accommodates asynchronous 10M-bps data rates, includes a field-selectable DTE/DCE configuration switch, and offers a choice of RS-232C- or RS-422-type interfaces.

The FX111 is an asynchronous low-speed RS-232C data link that derives its operating power from the DTE host. It offers data rates to 19.2k bps and a maximum transmission-distance capability of 1 mile. Like the FX102, it includes a built-in DTE/DCE configuration switch.

The FX112 offers synchronous as well as asynchronous RS-232C communications at data rates to 38.4k bps. You can configure this link to provide an internal clock (with five different settings), to operate from an external clock signal, or to act as a slave. It also offers a choice of a standard 12-dB system gain or, optionally, 20 dB.

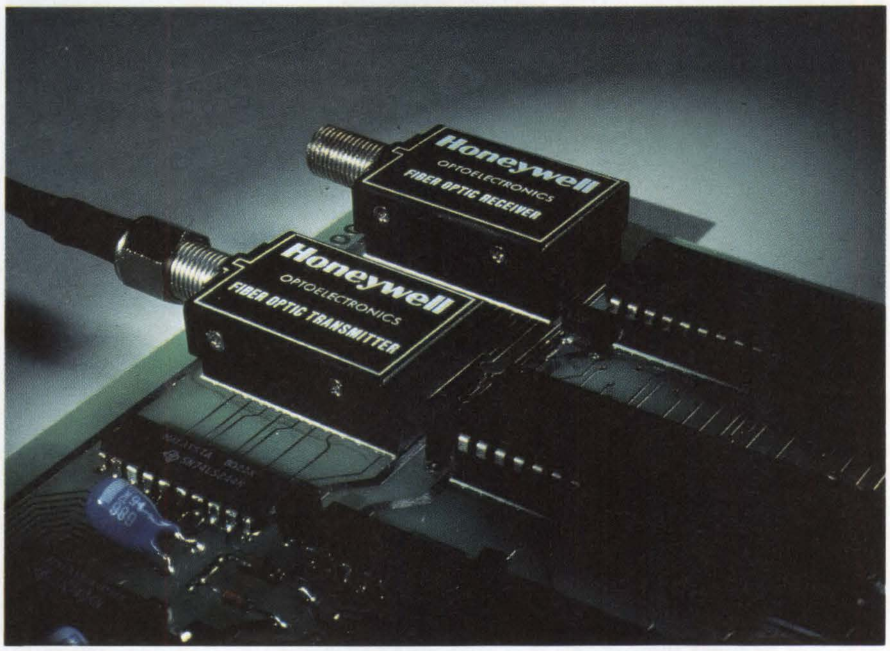
The FX113 completes the family. A true DCE port extender, it allows the DCE to supply both receive and transmit clocks. The FX113 supports synchronous RS-232C data rates to 38.4k bps, DCE clocking, and two full-duplex control lines.

All four links feature dBJUST, an automatic-gain-control system that automatically adjusts for short cable lengths. Each is also available in a card-only version, which includes four data sets per card (these configurations have a /Q-4 suffix). Prices vary from $150 (FX111) to $1350 (FX111/Q-4 with high-power optics).

Litton offers three RS-232C fiber-optic transceivers that provide full-duplex capability and extend the transmission distance of standard unrepeatered signals to more than 8 km. All units meet MIL-STD-202E requirements for shock and vibration, and they can interface with either DTE or DCE.

The EO3675 and EO3672 transceivers provide asynchronous transmissions at data rates to 200k bps, and the EO3671 provides asynchronous/synchronous transmissions at rates to 56k bps. All units specify a BER of 10^{-9}. Supply requirements are ±12V dc at 200 mA for the EO3672 and EO3675 and 12V dc at 120 mA for the EO3671. The operating range also varies: The EO3672 and EO3675 operate over 0 to 70°C; the EO3671 operates over 0 to 50°C.

The transmitters use a microlensed LED source that emits at a nominal wavelength of 840 nm. The typical optical output power varies with the fiber transmission media, ranging from 30 μW for 50-μm core fiber to 950 μW for 200-μm core fiber. The receivers have pin-diode detectors and feature sensitivities of −38 dBm (EO3672 and EO3675) and −45 dBm (EO3671). A 25-pin D subminiature connector provides the electrical interface; SMA-compatible connectors, which accommodate 50/125-, 62.5/125-, 85/125-, or 100/140-μm fiber, provide the optical interface. The EO3671 costs $999; the EO3672, $349; the EO3675, $399. All prices are quoted per set for quantities of 100.



Placing no restrictions on input data format, *Honeywell's HFM Series of low-profile transmitter and receiver modules handle dc to 25M-bps data rates and feature user-selectable power ratings.*

Thomas & Betts has just introduced an RS-232C-type fiber-optic data link, the 9481. Designed for computer, terminal, and printer applications, the link accommodates either plastic or glass duplex fiber cable and handles 19.2k-baud asynchronous data rates.

In addition to transferring data in either direction, the link supports six control/handshake lines over the same cable. It also eliminates RFI/EMI problems, extends transmission distances to 2 km with 140-µm core glass fiber (200m over plastic fiber), and derives its power either directly through the DB25 connector or via an external power supply.

The 9481 is available in both male and female and DTE and DCE configurations and is compatible with AT&T Technologies ST-type optical connectors. You can readily install the link on site without any modifications to existing RS-232C installations. The link operates over 0 to 70°C, specs a 10^{-9} BER, and requires ±12V. It is priced at $36 (OEM qty) for a plastic-fiber version or $54 for a glass-fiber unit.

As mentioned previously, today's fiber-optic transmitter and receiver modules are capable of doing more than just satisfying low-speed computer-to-peripheral link applications. Modules to handle faster data transmissions are readily available.

AMP's 5013XX Optimate line handles data rates ranging from 25M to 220M bps. The units operate in the 820- and 1300-nm wavelength range and offer either TTL or ECL compatibility. All of the modules feature a receptacle that mates with connectors that accommodate 125- to 250-µm fibers.

The transmitters employ an LED (either AlGaAs or InGaAsP) as the light source. Minimum peak-output power ratings vary with fiber-core size. For the TTL-compatible 25-MHz transmitter (501388), for example, this spec is −20 dBm for a 50-µm-core fiber with a 0.21 NA (numerical aperture) and −12 dBm for a 100-µm-core fiber with a 0.3 NA. For the same fibers, the output rating for the ECL-compatible 220-MHz transmitter (501344) is −16 to −23 dBm, respectively. Output spectral widths range from 50 to 100 nm and maximum rise and fall times (20 to 80% points) are 2 to 5 nsec.

The receivers employ either silicon or InGaAs pin diodes as the optical detector. BER specs are either 10^{-9} or 10^{-12}, and minimum input levels range from −30 to −37 dBm. The receivers operate at a 40 to 60% duty cycle and specify rise and fall times of 1 to 5 nsec max.

All of the units operate over 0 to 70°C. TTL-compatible transmitters require 5V supplies, whereas their receiver counterparts operate from ±5V. The ECL-compatible transmitters and receivers require −5.2V and +5/−5.2V, respectively. Prices for the Optimate line start at $200/pair.

Receiver extends capabilities

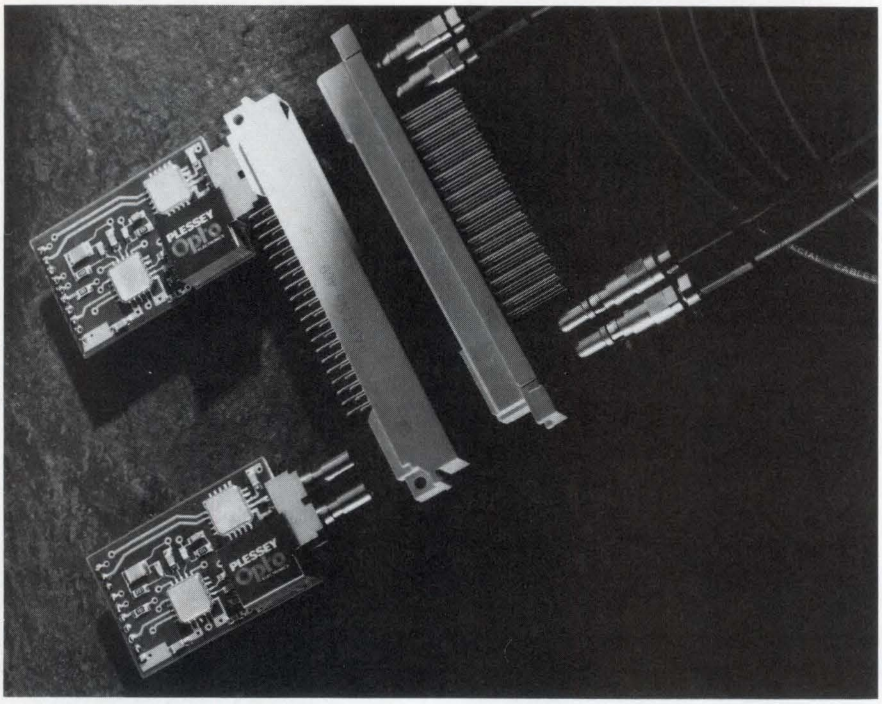
Hewlett-Packard's HFBR-24X6 receiver family extends the capabilities of the company's 820-nm component line to 150M bps. Designed for cost-sensitive digital applications, the receivers are well suited for analog/video service in applications involving workstation and security-transaction links.

The receivers contain a pin photodiode, an IC preamplifier, and a lens. Thanks to a dynamic range of 24 dB, the HFBR-24X6 units can accommodate a wide range of link distances—typically 1m to 3 km at 35M bps.

You have a choice of either SMA (-2406) or ST (-2416) connector ports. The receivers are fully compatible with the company's HFBR-14XX transmitters and are fully specified for use with 62.5/125-, 100/140-, and 50/125-µm multimode fiber. They cost $25 (1000).

Honeywell's HFM Series of data links consists of trilevel transmitters and receivers designed for point-to-point digital-data transmission. All of the modules are housed in metal packages, operate from 5V, and come with SMA or ADM (AMP Inc) optical connectors.

The line includes two transmitter modules, the HFM2010 and the



***Available in either through-hole or surface-mount** configurations, the Plessey P35-8858 is a 40M-bps transceiver that provides 600m transmission distance capability in LAN applications.*

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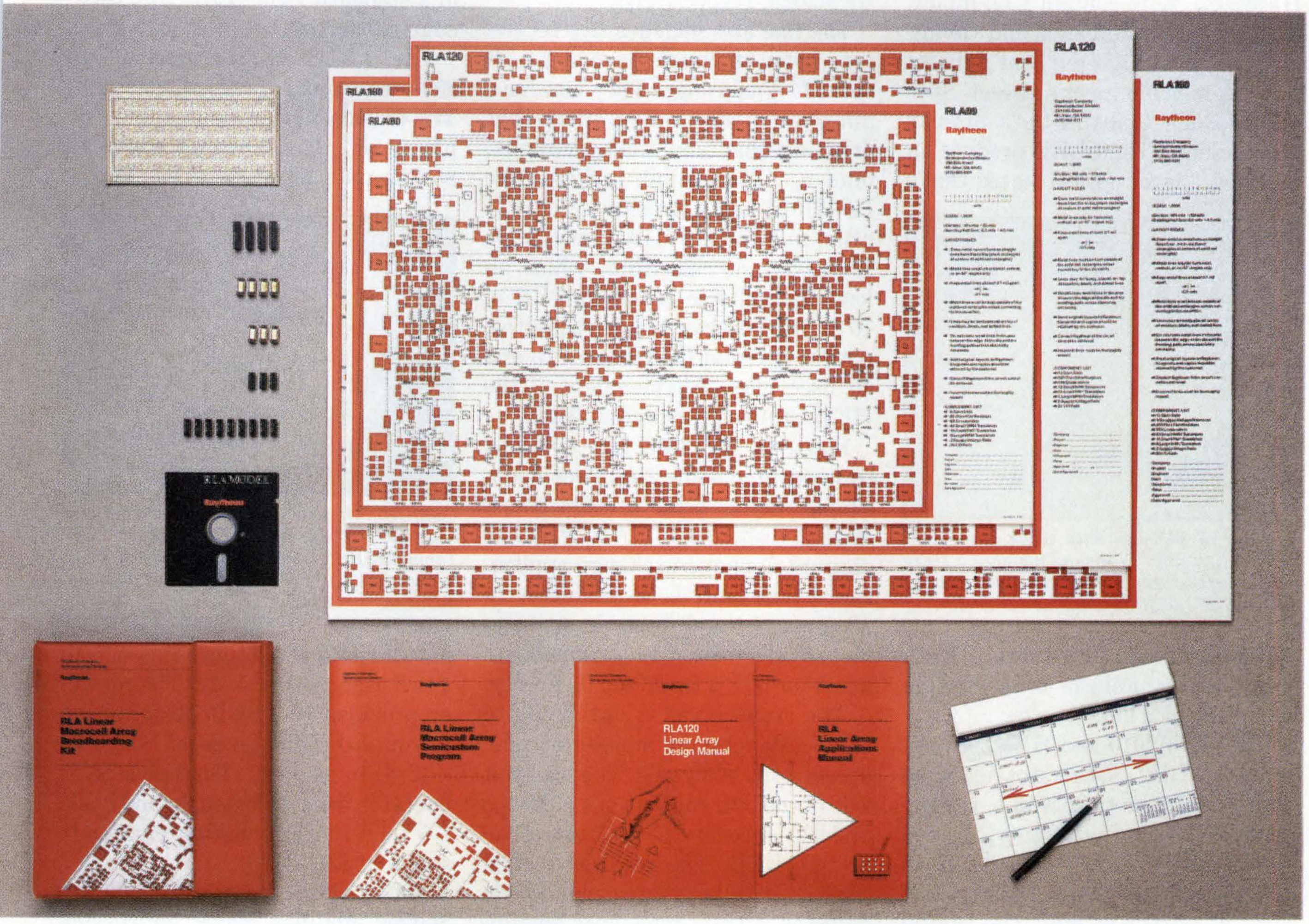

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[1]PSPICE is a trademark of MicroSim Corporation.
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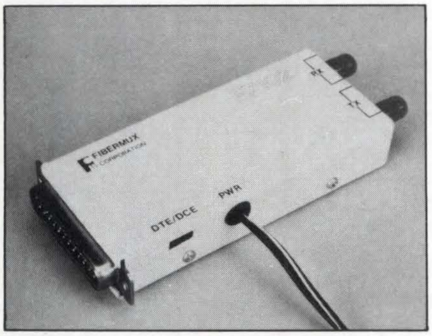
HFM2025. Both contain TTL inputs that drive encoder logic and timing circuits, plus high-current drivers for the manufacturer's Sweet Spot LED. Each transmitter's bipolar Masterslice IC and LED produce an encoded 3-level optical signal that's independent of data format. Both units are capable of transmission distances of 2 km.



Capable of 10M-bps data rates, *the FX102 optical link from Fibermux includes a DTE/DCE configuration switch and offers a choice of RS-232C- or RS-422-type interfaces.*

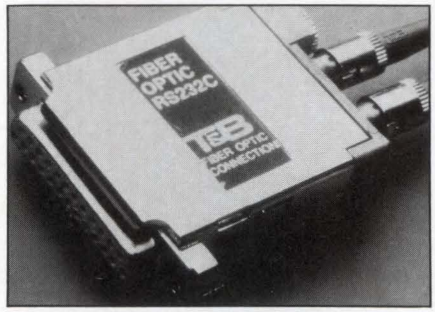
The HFM2010 and HFM2025 operate at NRZ data rates of dc to 10M bps and dc to 25M bps, respectively. Working with 100-μm core fiber, the HFM2010 outputs 10 to 100 μW min, and the HFM2025 outputs 10 to 50 μW min. The typical peak-output wavelength measures 820 nm, and the optical pulse widths are 50 and 20 nsec (HFM2010 and HFM2025, respectively).

The line also includes two receivers, both of which have a 24-dB optical-signal range. They also have pin photodiode preamplifiers that drive decoder and timing circuits, plus a TTL output buffer. The HFM1010 has a sensitivity of −31 dBm, and the HFM1025 specifies a sensitivity of −25 dBm, which allows the units to achieve a BER of 10^{-9}. The receivers have respective optical rise and fall times of 25 and 10 nsec max. All members of the HFM Series are priced at $120.

Plessey's P35-8858 is a 40M-bps transceiver module that provides a simple way to achieve 600m transmission distances in LAN, PBX, or digital-telephone-exchange applications. The unit is available with either a through-hole or surface-mount termination to accommodate a mother board for added flexibility.

The transceiver is optimized to handle Manchester biphase encode/decode type of signals. The transmit side of the unit consists of a 50M-bps biphase encoder IC that drives an 850-nm LED. The receiver section consists of a large-area photodiode detector, a transimpedance amplifier, and decoder ICs. The optical interface employs a pair of expanded-beam optical connectors housed in a standard DIN 41612-type card-edge connector.

The P35-8858 operates at an 850-nm nominal optical wavelength. The transmitter generates 28 to 60 μW (−15.5 to −12 dBm) through an 85/125-μm multimode fiber. Transmitter rise and fall times range from 4 to 8 nsec, respectively. The receiver provides 10^{-9} BER performance for optical input levels of −25.5 to −12 dBm at 25°C. The transceiver operates from a 5V supply and has a −5 to +70°C operating range. It starts at $350 (100).



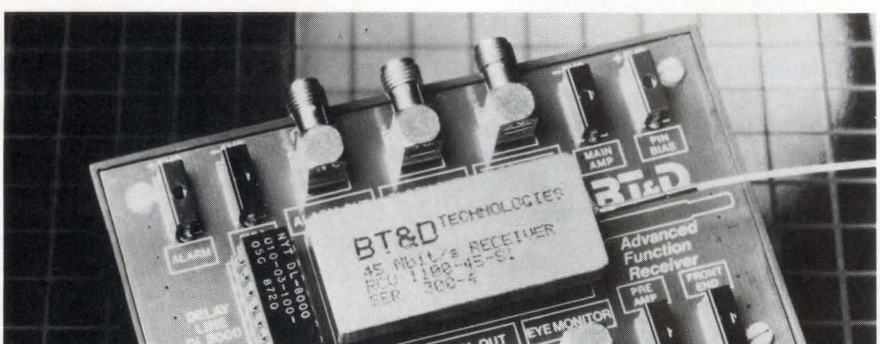
Compatibility with plastic or glass fiber *is a key feature of this RS-232C transceiver from Thomas & Betts. Available in a DTE or DCE configuration, the unit extends transmission distances to 2 km.*

All of these transmitter and receiver modules have impressive data-transfer rates, but AT&T and BT&D offer modules capable of handling much higher frequencies—1G bps, for example.

Speed is no problem

AT&T has recently introduced transmitter and receiver modules designed for high-speed digital applications. Both types of modules operate at 1.3-μm nominal optical wavelengths over single-mode fibers.

The Astrotec 1218-type transmitter incorporates a InGaAsP laser, a thermoelectric cooler, and an integral monitoring photodiode. In addition, it includes modulation circuitry and temperature and feedback controls. Standard features include a 50Ω input impedance, a data-transmission rate (with NRZ format) of 1G bps, and an average ouput power of −10 to 0



Operating in the 1200- to 1600-nm wavelength range, *BT&D's RCV 1000 receiver family includes units that accommodate data rates of 800M bps. Integrated electronics provides ECL-compatible complementary outputs.*

dBm. A number of options allows users to individually specify bit rate and output spectral width (200, 565, or 880M bps, and 5, 15, 20, or 50 nm, respectively).

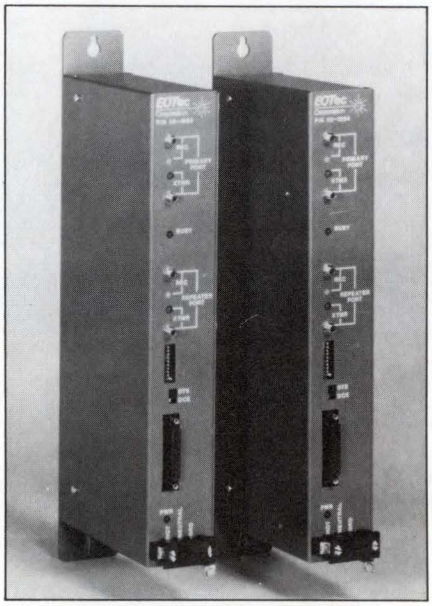
The transmitter is housed in a hermetically sealed 14-pin SIP. It operates over −65 to +85°C and requires a 5V supply. It sells for $2500 to $4500, depending on configuration and quantity.

The Astrotec 1306AA, a wide-bandwidth linear receiver, can operate at speeds to 1.7G bps. It incorporates a low-capacitance, hermetically sealed APD (avalanche photodiode) followed by a GaAs IC preamplifier. The preamplifier's transimpedance is adjustable to optimize sensitivity and bandwidth parameters.

The receiver's dynamic range spec is greater than 18 dB. At optimum sensitivity, the APD has a gain of 10. When operating at a 1.7G-bps data rate, the 1306AA's sensitivity for a 3×10^{-11} BER equals −32 dBm at 23°C. This sensitivity is measured at the receiver's connector.

The 1306AA is housed in an EMI-shielded, corrosion-resistant package that includes a 20-in. long single-mode fiber pigtail and an AT&T 2016A connector. The unit costs $2850 (100) and operates over 0 to 65°C.

BT&D Technologies' RCV receiver family includes devices that are either implemented totally in silicon or in a combination of silicon and GaAs to achieve optimal bit-rate choices and sensitivity. Suitable for single-mode or multimode applications in the 1.2- to 1.6-μm wavelength range, the units convert optical information into ECL-compatible signals.



Totally transparent to an existing electrical system, *Eotec's Network Link extends RS-232C and RS-422 station-to-station transmission distances to 12,000 feet.*

The family includes models that accommodate data rates spanning 50M to 800M bps. The basic receiver design features an InGaAs pin photodiode, a transimpedance-type preamplifier, and integrated electronics that provides ECL-compatible complementary outputs, partial clock extraction, and selected analog outputs for performance monitoring. Receiver sensitivities reach −10 dBm. The receivers operate over a −40 to +85°C range and are housed in 28-pin hermetically sealed metal DIPs. Their supply requirements are ±5V. Prices start at $350 (OEM qty). **EDN**

Article Interest Quotient
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For more information . . .

For more information on the fiber-optic transmitter and receiver modules described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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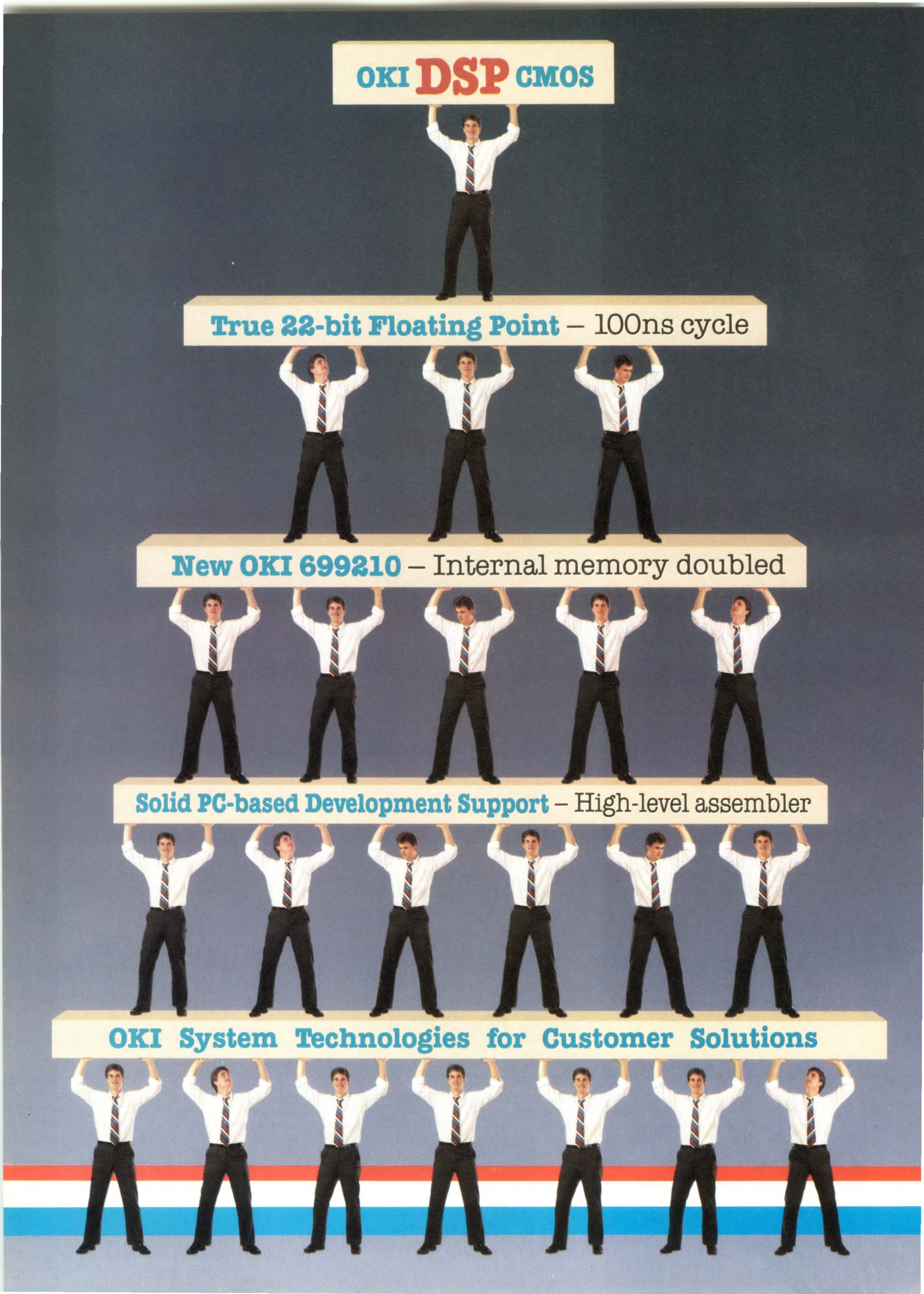
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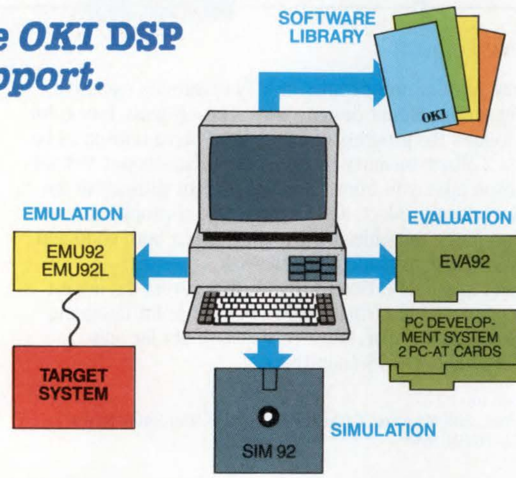

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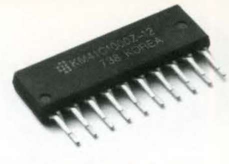

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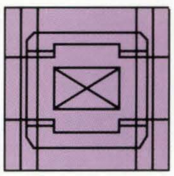
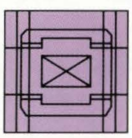


1984-64K
117μ² cell size
2.5μm geometry



1985-256K
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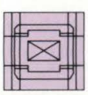
1.6μm geometry



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KM41C1001	1M x 1	Nibble mode	100,120	DIP, ZIP, SOJ	2Q '88*
KM41C1002	1M x 1	Static Column mode	100,120	DIP, ZIP, SOJ	2Q '88*
KM44C256	256K x 4	Fast Page mode	100,120	DIP, ZIP, SOJ	2Q '88
KM44C258	256K x 4	Static Column mode	100,120	DIP, ZIP, SOJ	2Q '88
KM41256	256K x 1	Page mode	120,150	DIP, ZIP, PLCC	Now
KM41257	256 x 1	Nibble mode	120,150	DIP, ZIP, PLCC	Now
KM41464	64K x 4	Page mode	120,150	DIP, ZIP, PLCC	Now
KM4164	64K x 1	Page mode	120,150	DIP	Now
KMM48/9256	256K x 8/9	Page or Nibble modes	120,150	SIP module	Now
KMM58/9256	256K x 8/9	Page or Nibble modes	120,150	SIMM module	Now
KMM48/91000	1M x 8/9	Fast Page mode	100,120	SIP module	2Q '88
KMM58/91000	1M x 8/9	Fast Page mode	100,120	SIMM module	2Q '88

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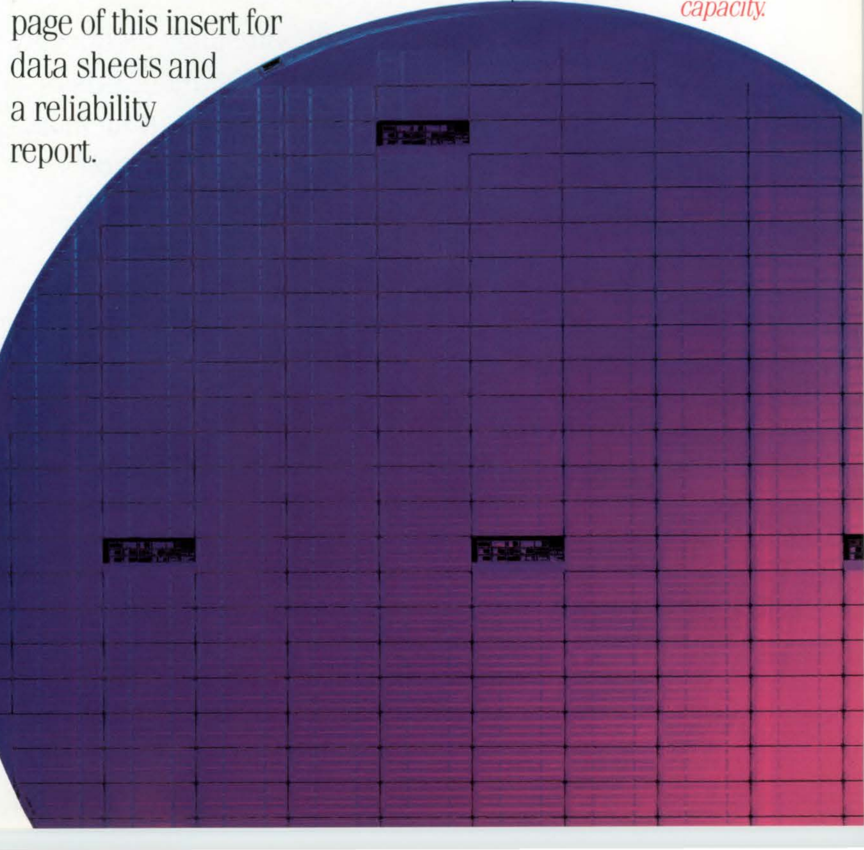

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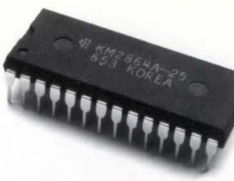


Advanced Samsung 16K and 64K EEPROMs are now available in production quantities.

Samsung EEPROMs also outpace industry standards.

Samsung's 64K and 16K EEPROMs meet or surpass all industry standards for performance, reliability and quality. They have standard endurance ratings of 10,000 erase/write cycles and data retention ratings of 10 years.

And our "H" version 64Ks offer a quick 2 millisecond per byte write time, reducing write time by a factor of 5.

Part Type	Organization	Speed	Features	Technology	Pinout	Availability
KM2816AP	2K x 8	250,300,350	10ms (max) write time	NMOS	24 pin	Now
KM2817AP	2K x 8	250,300,350	Ready/Busy, 10ms (max) write time	NMOS	28 pin	Now
KM2864AP	8K x 8	250,300,350	Data Polling, 10ms (max) write time	NMOS	28 pin	Now
KM2865AP	8K x 8	250,300,350	Data Polling, Ready/Busy, 10ms (max) write time	NMOS	28 pin	Now
KM2864AHP	8K x 8	250,300,350	Data Polling, 2ms (max) write time	NMOS	28 pin	Now
KM2865AHP	8K x 8	250,300,350	Data Polling, Ready/Busy, 2ms (max) write time	NMOS	28 pin	Now
KM28C64P	8K x 8	150,200,250	Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time	CMOS	28 pin	May '88*
KM28C65P	8K x 8	150,200,250	Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time	CMOS	28 pin	May '88*

*Samples available now.

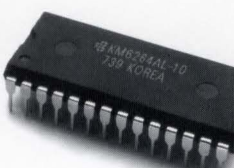
Our new 64K KM28C64 series (available 2nd quarter 1988) is fabricated with our pacesetting floating gate CMOS processing. It features low power dissipation of 100μA standby and access times of 150ns, 200ns and 250ns. These advanced 8K x 8 EEPROMs also feature a 32-byte page mode to slash write times to 150 microseconds per byte and a 5-millisecond write cycle. This allows the entire 64K memory to be written in only 1.3 seconds.

Samsung's EEPROMs excel in such rugged applications as communications, instrumentation, robotics and industrial control. All our EEPROMs meet JEDEC pinout standards.

Fill out the coupon on the back page of this insert for samples, a data sheet, and reliability report.

Circle No. 168

Samsung's 256K (32K x 8) KM62256 SRAMs are available with access times of 100ns, 120ns and 150ns, all in low-power versions with standby current of only 4μA (typical).



Samsung SRAMs are fabricated using 1.2 μm CMOS technology. In 1988, we are ramping up 256K and 64K SRAM production.

The fast pace continues with Samsung low power SRAMs.

The pace of Samsung's technology development in static RAMs is as strong as it is for all our memory products. With the introduction of the KM62256 (32K x 8) SRAM Family, we now offer a wide low power CMOS SRAM line, including our KM6264A industry standard 64K SRAMs.

The KM62256 256K SRAM is fabricated using our internally developed 1.2 μm CMOS technology which meets both high speed and low power requirements. We offer 80ns 64K SRAMs and 100ns 256K SRAMs in high volume. They're ideal for process control, medical instruments, and hand held devices.

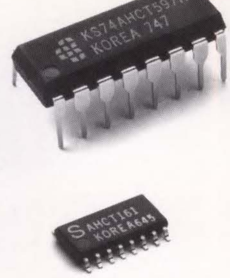
Samsung is ramping up production of both the 256K and 64K CMOS SRAMs. Our complete line is available now in industry standard packages and pinouts.

Part Type	KM62256L	KM6264AL
Organization	32K x 8	8K x 8
Speeds	100, 120, 150ns	80, 100, 120ns
Package	28 DIP	28 DIP
Max Current (standby)	100μA	100μA
Availability	Now	Now

Fill out the coupon on the back page of this insert for a data sheet and reliability report.

Circle No. 169

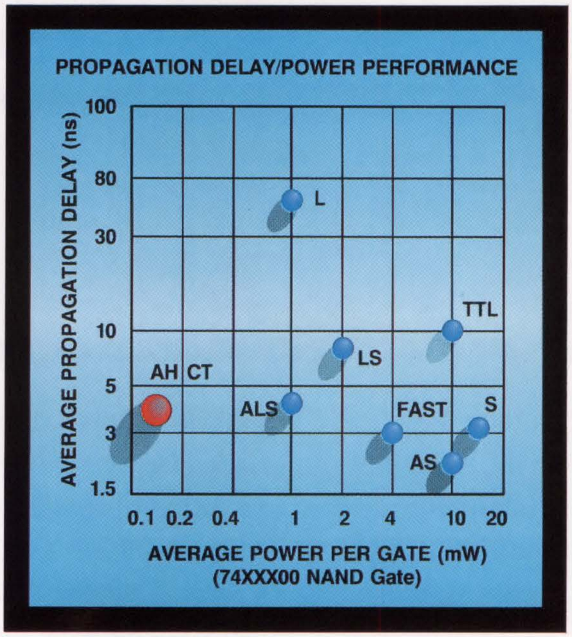
Samsung Advanced AHCT CMOS Logic Family keeps pace with the fastest 16- and 32-bit microprocessors.



Samsung's Advanced CMOS Logic is available in both DIP and SOIC packages.

Available now in production quantities, our Advanced AHCT CMOS Logic Family meets the demands of your 16- and 32-bit designs for high speed, high drive and low power.

Samsung has 111 of the most popular standard logic functions available off the shelf now, with samples free for the asking. By mid-year, we will add another 50 part types to the list. This means you can design our part into your product and move into production now with no waiting.



For power reduction in your existing designs, AHCT offers pin-for-pin, part-for-part replacement for ALS and FAST.™ It fits right in and reduces power tenfold. Yet our AHCT doesn't have a premium price. It costs the same as ALS.

Fill out the coupon on the back page of this insert for free samples and a data book.

Circle No. 170

KS74AHCT PARTS LIST

Gates and Inverters

00	20
01	21
02	22
03	27
04	30
05	32
08	51
09	58
10	86
11	132
12	133
14	266

Buffers & Line Drivers

125	367
126	368
210	465*
240	466*
241	467*
244	468*
365	540
366	541

Flip-Flops

73	399
74	534
76	564
78	574
107	670
109	794*
112	821*
173	822*
174	823*
175	824*
273	825*
374	826*
377	

Latches

75*	793*
77*	841*
259	842*
373	843*
533	844*
563	845*
573	846*

Transceivers/Registered Transceivers

242*	643	652*
243*	645	658*
245	646	659*
640	648	664*
	651*	665*

Counters

160	190	590*
161	191	591*
162	192	592*
163	193	593*
168	390*	
169	393	

Decoders/Encoders

42	148*	238
138	154	239
139	155	

Multivibrators

121*	123*	423*

Logic Level Converters

4049	4050*

Multiplexers

151	253
153	257
157	258
158	352
251	353

Shift Registers

164	299
165	595
166	596
194	597
195	

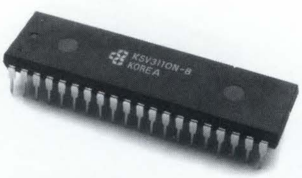
Arithmetic Circuits

181*	522*
182*	679
183	680
280	682
518*	684*
519	686*
520*	688
521	689*

*Part types available in 2Q '88. All other part types available now.

FAST is a trademark of Fairchild Semiconductor, Inc.

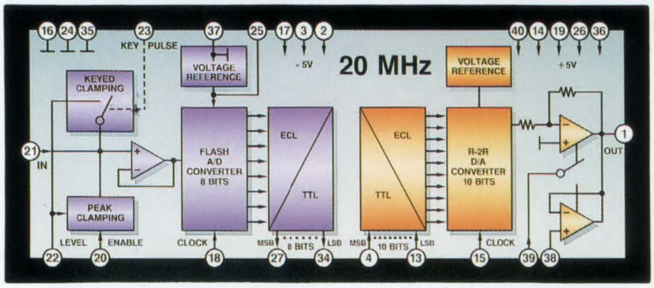
Samsung's KSV3110 combo A/D-D/A and KSV3208 A/D set the pace in flash converters.



KSV3110 Combo A/D-D/A Flash Converter

KSV3208 A/D Flash Converter

The pacesetting technology of our single-chip KSV3110 A/D-D/A data converter provides independent 8-bit A/D converter functions and 10-bit R-2R D/A converter functions over an operating range of DC to 20MHz.



With the ease of design you get with the KSV3110's two chips in one, you'll save both money and real estate, leaving room and resources to add other features. And having fewer parts cuts down power drain and boosts system reliability.

The KSV3110 gives TTL-compatible input/output, 1% absolute non-linearity and selectable peak level input or keyed clamping.

The impressive linear characteristics of the KSV3110 are shared by our new KSV3208 A/D flash converter. It provides the same features for applications that don't require D/A conversion.

Samsung also offers the support chips to ease the integration of the KSV3110 into video applications. For example:

- KA2606 Sync Separate IC
- KA2153 Chrominance Signal Processor for NTSC systems
- KA2154 Video Chroma Deflection System for NTSC and PAL systems

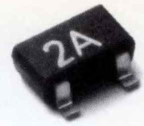
Fill out the coupon on the back page of this insert for samples and a Flash Converter IC Data Book.

Circle No. 171

Part Type	Resolution A/D	Resolution D/A	Linearity A/D	Linearity D/A	Conversion Speed	Industry Part
KSV3110N-10	8 bits	10 bits	± ½ LSB	± ½ LSB	20 MSPS	
KSV3110N-9	8 bits	10 bits	± ½ LSB	± 1 LSB	20 MSPS	
KSV3110N-8	8 bits	10 bits	± ½ LSB	± 2 LSB	20 MSPS	
KSV3110N-7	8 bits	10 bits	± ½ LSB	± 4 LSB	20 MSPS	
KSV3100AN-8	8 bits	10 bits	± ½ LSB	± 2 LSB	20 MSPS	UVC3101
KSV3100AN-7	8 bits	10 bits	± ½ LSB	± 4 LSB	20 MSPS	UVC3101
KSV3208N	8 bits		± ½ LSB		20 MSPS	
KAD0820ACN	8 bits		± ½ LSB		1.5 μsec	ADC0820BCN
KAD0820BCN	8 bits		± 1 LSB		1.5 μsec	ADC0820CCN
KAD0808IN	8 bits		± ½ LSB		100 μsec	ADC0808CCN
KAD0809IN	8 bits		± 1 LSB		100 μsec	ADC0809CCN
KDA0800CN		8 bits		± ½ LSB	*100 nsec	DAC0800LCN
KDA0801CN		8 bits		± 1 LSB	*100 nsec	DAC0801LCN
KDA0802CN		8 bits		± ¼ LSB	*100 nsec	DAC0802LCN
KDA0806CN		8 bits		± 2 LSB	*150 nsec	DAC0806LCN
KDA0807CN		8 bits		± 1 LSB	*150 nsec	DAC0807LCN
KDA0808CN		8 bits		± ½ LSB	*150 nsec	DAC0808LCN
KS7126CN	3½ digit		± ½ LSB		333 msec	TSC7126
KS25C02	CMOS 8-bit successive approx. register					DM2502
KS25C03	CMOS 8-bit successive approx. register					DM2503
KS25C04	CMOS 12-bit successive approx. register					DM2504

*Settling Time

Samsung's SOT-23s set the pace for surface mount technology.



Samsung has 100 types of SOT-23 available now.

Samsung has introduced 100 types of SOT-23s with an AOQL of 100 ppm or better—all with competitive pricing. They're ideal for both hybrid and surface mount applications. The entire line is in full production and available from stock. Samsung can deliver SOT-23s in the quantities you need when you need them.

SOT-23 PART TYPES

MMBR5179	MMBT5087	MMBTA55
MMBT2222A	MMBT5088	MMBTA56
MMBT2484	MMBT5401	MMBTA63
MMBT2907A	MMBT5550	MMBTA64
MMBT3904	MMBT6428	MMBTA70
MMBT3906	MMBTA05	MMBTA92
MMBT4123	MMBTA06	MMBTA93
MMBT4124	MMBTA13	MMBTH10
MMBT4125	MMBTA14	MMBTH17
MMBT4126	MMBTA20	MMBTH24
MMBT4401	MMBTA42	BCX70G
MMBT4403	MMBTA43	BCX71G

66 other types also available

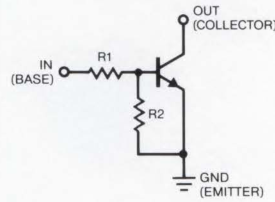
Samsung now has available a new family of digital transistors, the KSR1000 Series (NPN) and KSR2000 Series (PNP), with 40 part types in each family. They're especially useful for applications where logic circuits are being interfaced with electromechanical systems.

We also offer an extensive line of industry standard TO-92, TO-126, and TO-220 transistors, plus TIP-Series power transistors, small signal transistors, high speed high voltage switching power transistors, Darlington power transistors and 1500V TO-3P transistors.

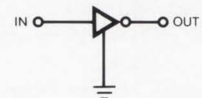
Fill out the coupon on the back page of this insert for samples and a copy of our new Transistor Data Book.

Circle No. 172

Internal Circuit



Function



Samsung's new KSR1000 and KSR2000 Series digital transistors are especially useful for applications where logic circuits are being interfaced with electromechanical systems.

Samsung sets a fast pace in delivering linear ICs.

The quality of Samsung linear ICs has gained them solid market acceptance. We now have over 250 industry-standard ICs available for immediate delivery. And Samsung has invested substantially to ensure that you get the latest technology, with high reliability in high volume at very low cost.

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Voltage Regulators
KA336Z-5 (LM336-5)
KA431CZ* (TL431)
KA431CN (TL431)
LM723CN
LM317T
MC78TXXCT
MC78XXCT
MC78XXACT
MC78LXXACZ
MC78MXXCT
MC79LXXACZ
MC79MXXCT
MC79XXCT
μA78S40CN
KA385Z-1.2 (LM385-1.2)

OP AMPS
KA301AN* (LM301A)
LM741CN*
MC1458CN*
MC4558CN*
LM358N*
LM358AN*
LM348N*
LM324N*
LM324AN*
MC3403N*
KS271 (TLC271)
KS272 (TLC272)
KS273 (TLC273)

Telecommunications ICs
KA2410N—Tone ringer
KA2411N—Tone ringer
KA2418N—Tone ringer with bridge diode
KA2412FN—Speech network
KA2413N—DTMF
KS5808N—DTMF
KS5805AN/BN—Pulse dialer
KS5819N—Pulse/DTMF (22 DIP)
KS5820N—Pulse/DTMF (18 DIP)
KT3040—CODEC filter
KT5116—CODEC
LM567N*—Tone decoder
LM567LN—Tone decoder Micropower

Timers
KS555N* (CMOS)
KS555HN* (CMOS)
KS556N* (CMOS)
NE555CN*
NE556CN*
NE558CN

Comparators
KA319N
KA710CN
LM311N*
LM393N/AN*
LM339N/AN*
KS374N (TLC374)
KA361N (LM361)

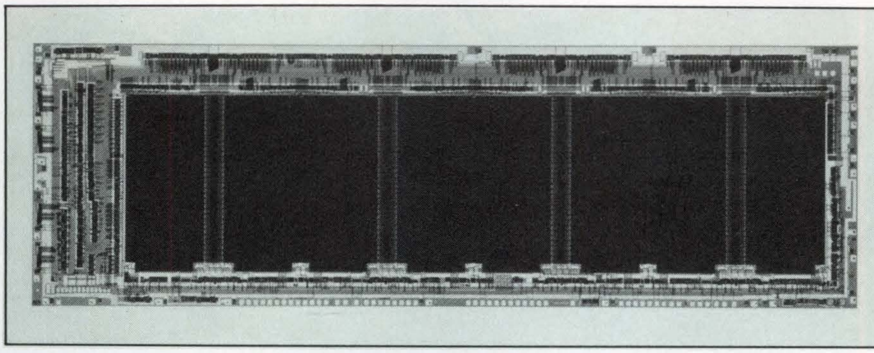
RS-232 Interface
MC1488N*—Driver
MC1489N/AN*—Receiver

*Also available in surface-mount package (SOIC).

Circle No. 173

1M-bit video RAMs offer speed for high-resolution graphics displays

Margery S Conner,
Regional Editor



***Art A—The TC524257 1M-bit video RAM** supports such features as flash write, split-register transfer, and raster ops. The TC524256 is a stripped-down version of the TC524257. Both products are from Toshiba.*

Deciding what type of RAM to use for your graphics-display memory used to be simple: A low-resolution graphics system, with its correspondingly low bandwidth and price, dictated that you use low-cost dynamic RAMs, while a high-resolution, higher-cost system could justify choosing the more-expensive dual-ported video RAMs. Today, however, demand for high-resolution displays is increasing even in the low-cost personal-computer market. To obtain 1024×1000-pixel resolution and 8 bits of color for your high-resolution display, you'll need to use a video RAM. Fortunately, added features and a lower cost per bit make the most recently developed 1M-bit video RAMs increasingly practical to use.

Although 64k- and 256k-bit video RAMs have been available for a few years, their steep price and limited capabilities have kept them from gaining widespread use. The 1M-bit RAMs that will become available this year, however, may rapidly change that situation.

First, although video-RAM prices have historically been well over three times the price of dynamic RAMs, you can expect the newly introduced 1M-bit video RAMs to shrink that price difference. For example, Mitsubishi estimates that the initial price for its M5M442256 will be about three times that of a dynamic RAM, or about $60. But within a year the company expects to see the price fall to $40 to $45. Texas Instruments estimates that the price of a 1M-bit video RAM will drop to less than twice that of a dynamic RAM, making the video RAMs competitive for use in personal-computer displays as well as higher-resolution graphics terminals.

US regulates RAM prices

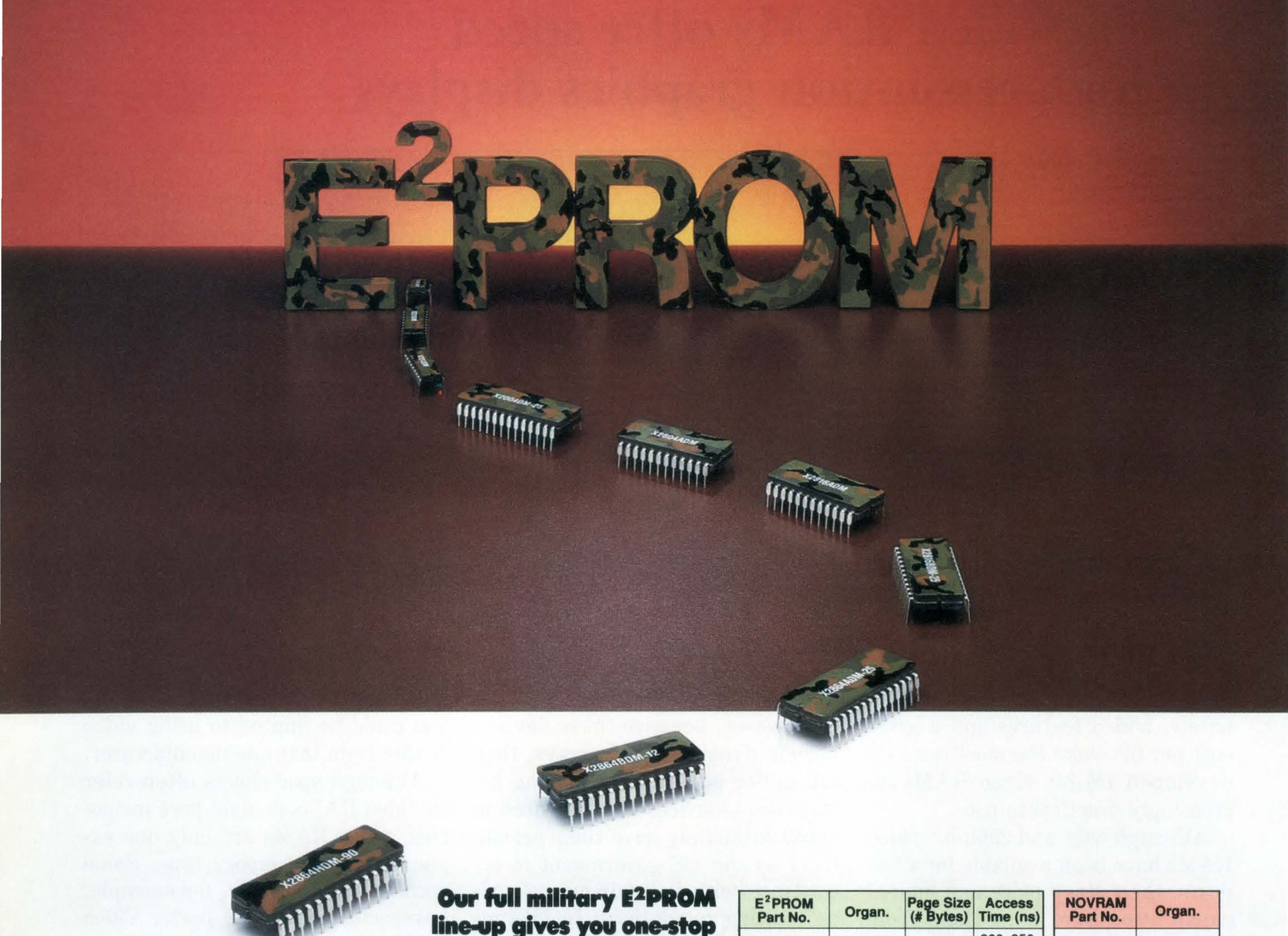
However, because these devices include dynamic-RAM arrays, they fall under government pricing restrictions—devices manufactured in Japan ultimately have their pricing fixed by the US government in accordance with its "fair-market-value" pricing regulations. Incidentally, Texas Instruments' device is manufactured in Japan, as is Mitsubishi's. Samsung's is manufactured in Korea, however, and the fair-market-value pricing regulations don't control the prices of parts manufactured in Korea. At present, Toshiba is the only video-RAM manufacturer that will quote a firm price for its video RAM (the TC524256/7). The company has been shipping parts since November.

Second, these RAMs all support a variety of graphics-intensive features. (**Table 1** lists some of the most significant features for the 1M-bit video RAMs that will be available this year.) Matching your application needs to the correct video-RAM features is the best way to determine the right device for your application. But be wary of basing your design on a video RAM that has sophisticated but unique features. In the future, as JEDEC standards for video RAMs emerge, you could be limited to using video RAMs from that one manufacturer.

Although spec sheets often refer to video RAMs as dual-port memories, video RAMs are only one example of that memory type. Some cache-memory RAMs, for example, have multiple parallel ports. Video RAMs, however, have one bidirectional parallel port, and at least one serial port, which is often, but not always, bidirectional **(Fig 1)**. A video RAM incorporates a dynamic-RAM memory array that feeds a serial shift register, which is also called a serial-access memory, or SAM. This architecture allows a processor to load the dynamic RAM at the same time that the serial shift register feeds the video display.

If, instead of video RAMs, you were to use standard dynamic RAMs for video memory, you'd have to trade off either display quality (because of restricted access to the video memory by the CRT) or drawing speed (because of restricted access by the CPU).

XICOR RAISES MILITARY DESIGNS TO A HIGHER LEVEL.

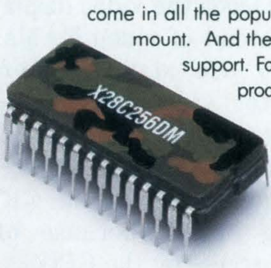


Our full military E²PROM line-up gives you one-stop shopping convenience.

Now you can promote your memory-intensive military designs to a higher level of functionality. With Xicor's complete line of military E²PROMs, NOVRAMs and E² potentiometers.

They raise system performance and power economies to a new level. And unlike most memories, Xicor E² devices can be remotely reprogrammed in the field, via telephone link. In the case of our E² potentiometers, they can automatically tune themselves while in service--kind of like an "electronic screwdriver." Plus our high density E²PROM memories are loaded with features like Page Mode, $\overline{\text{DATA}}$ Polling, Toggle Bit and Software Data Protection.

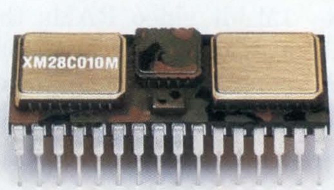
Volume-manufactured in JEDEC-approved pin-outs, Xicor E² devices come in all the popular packaging configurations, including surface mount. And they're backed by Xicor's on-site technical design support. For more details on JAN, DESC Drawing and 883C products, call (408) 432-8888 today, or write: Xicor, Inc., 851 Buckeye Court, Milpitas, CA 95035.



E²PROM Part No.	Organ.	Page Size (# Bytes)	Access Time (ns)
X2804AM	512 x 8	N/A	300, 350, 450
X2816AM	2048 x 8	N/A	300, 350, 450
X2816BM	2048 x 8	16	250, 300
X2864AM	8192 x 8	16	250, 300, 350, 450
X2864BM	8192 x 8	32	120, 150, 180
X2864HM	8192 x 8	32	90
X28256M	32768 x 8	64	250, 300, 350
X28C256M	32768 x 8	64	250, 300, 350
XM28C010M	131072 x 8	64	250, 300

NOVRAM Part No.	Organ.
X2210M	64 x 4
X2212M	256 x 4
X2004M	512 x 8
Serial I/O Part No.	**Organ.**
NOVRAM X2444M	16 x 16
E²PROM X2404M	512 x 8
E²PROM X24C16M	2048 x 8
E²POT™ Part No.	**Max. Resis.**
X9103M	10K Ω
X9503M	50K Ω
X9104M	100K Ω

E²POT™ digitally controlled potentiometer is a trademark of Xicor, Inc.



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MAKES IT MEMORABLE

CIRCLE NO 166

Video RAMs can have any or all of several optional features, such as write-per-bit, flash-write, split-register transfer, and raster ops (for definitions of these and other video-RAM terms, see **box,** "A video-RAM glossary," see pg 84). Generally, however, the manufacturers will probably divide into two camps: those that take an approach similar to Texas Instruments', and those that use one like Toshiba's. Texas Instruments' TMS44C251 video RAM doesn't perform raster ops, for instance, so it requires a graphics processor that can assume more control over the video data. The company expects customers to use the TMS44C251 video RAM with its TMS34010 graphics processor. Toshiba's TC524257 video RAM, on the other hand, has no allegiance to any particular processor architecture: It does perform raster ops. (The TC524256, however, doesn't perform raster ops; it's a stripped-down version of the TC524257.) Most of the Japanese manufacturers seem to be producing chips that provide a subset of the Toshiba chip's capabilities.

All of the 1M-bit video RAMs support some form of a write-per-bit feature. This feature is useful in accelerating vector draws: It allows you to access individual bits of a pixel that are not located contiguously in memory. A standard write-per-bit implementation requires you to reload the write mask for each $\overline{RAS}$ cycle. Unfortunately, a write-per-bit feature can't be implemented in page-mode operation unless the same write mask is used for each page-mode cycle: The mask is loaded during the falling edge of $\overline{RAS}$ and can't be changed until the next $\overline{RAS}$ cycle. (Page-mode addressing means that the $\overline{RAS}$ signal is latched, while the $\overline{CAS}$ signal changes.)

You'll also encounter a problem with the write-per-bit feature if your graphics processor has a multi-

TABLE 1—1M-BIT VIDEO RAMs

MANUFACTURER AND MODEL	RAM-ARRAY ACCESS TIME (nSEC)	SERIAL-PORT CYCLE TIME (nSEC)	RASTER OPS	BLOCK WRITE	FLASH WRITE	PERSISTENT WRITE PER BIT	SPLIT-REGISTER TRANSFER	PACKAGE (28 PINS)	AVAILABILITY (SAMPLES)	PRICE	COMMENTS
FUJITSU											
81C4251	100 OR 120	30 OR 40					•	DIP, ZIP	JUNE 1988	2×N* (SAMPLES)	
81C4252	100 OR 120	30 OR 40	•	•	•		•	DIP, ZIP	AUG 1988		
HITACHI											
HM534251	100, 120, OR 150	30, 40, OR 50	•		•			SOJ, ZIP	JUNE 1988	$40	128k×8-BIT VERSION WILL BE AVAILABLE IN THE 3RD QTR OF 1988
MITSUBISHI											
M5M442256	80, 100, OR 120	30, 35, OR 40			•		•	ZIP, SOJ	2ND QTR 1988	3×N*; WILL DROP TO 2×N	
NEC											
MPD42274	100 OR 120	30 OR 40			•			ZIP, DIP, SOJ	JULY 1988	$65 (SAMPLES)	
UPD42273	100 OR 200	30 OR 40						ZIP, DIP, SOJ	JULY 1988	$65 (SAMPLES)	
OKI SEMI-CONDUCTOR											
MSM514251	100 OR 120	30 OR 40						DIP, ZIP	MAY 1988	3×N*; WILL DROP TO 2×N	STATIC COLUMN ACCESS
MSM514252	100 OR 120	30 OR 40						DIP, ZIP	MAY 1988		FAST PAGE
SAMSUNG											
KM42C4256	100 OR 120	25 OR 35						DIP, ZIP, SOJ	DEC 1988	1.5×N*	
KM42C4257	100 OR 120	25 OR 35		•	•		•	DIP, ZIP, SOJ	APRIL 1989	2.0×N*	
TEXAS INSTRUMENTS											
TMS44C251	100, 120, OR 150	30, 33 OR 40		•		•	•	SOJ	NOW	3×N* (SAMPLES); 1.7×N* (PROD QTY)	
TOSHIBA											
TC524256	100 OR 120	30 OR 40	•	•				ZIP, SOJ	NOW	$74.25 (1000)	128k×8-BIT VERSION AVAILABLE IN THE 2ND QTR OF 1988
TC524257	100 OR 120	30 OR 40	•	•	•		•	DIP, ZIP, SOJ	NOW	$79.65 (1000)	

*N = THE PRICE OF A 1M-BIT DRAM, WHICH IS CURRENTLY ABOUT $20. FOR VIDEO RAMs MANUFACTURED IN JAPAN, THESE PRICES ARE SET ACCORDING TO US GOVERNMENT FAIR-MARKET-VALUE REGULATIONS.

plexed address and data bus: Mask data information can collide with the $\overline{\text{RAS}}$ address. Texas Instruments' graphics processor uses a multiplexed address and data bus: Its TMS44C251 video RAM circumvents the transient write mask by incorporating a "persistent write mask," a write mask that doesn't need to be rewritten.

Perhaps the most controversial of the video-RAM options is "flash write"—the ability to clear an entire row of video memory in a single memory cycle. You'll find this capability useful for rapidly manipulating entire rows in a plane—changing a background color, for example. However, keep in mind that there are tradeoffs associated with using flash write. For instance, it appears that the proposed JEDEC standard for video RAMs will allow manufacturers to incorporate either flash write or persistent write in their video RAMS, but not both. Therefore, the manufacturers that implement flash write in their video RAMs do so at the expense of the persistent write mask.

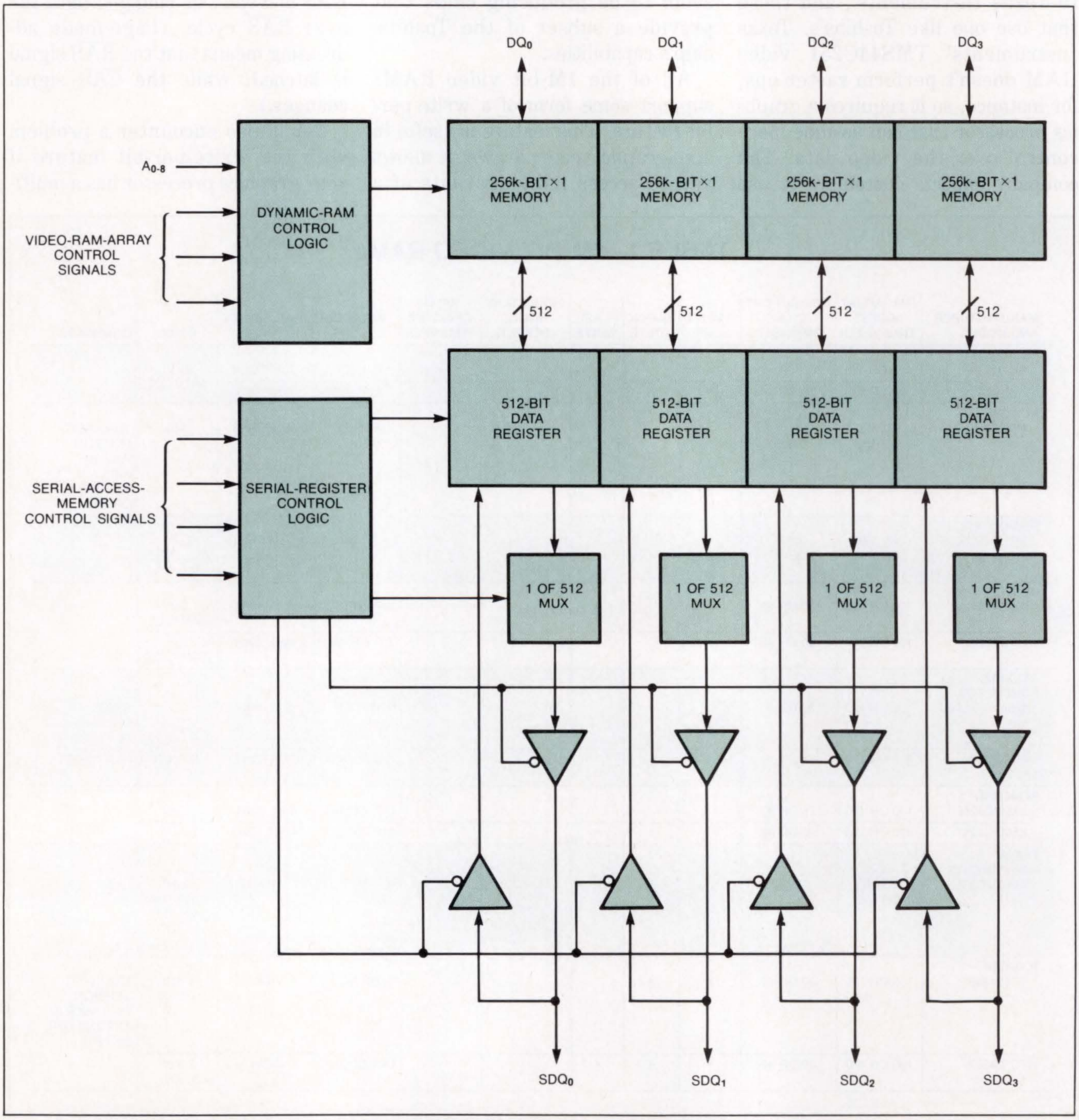

Fig 1—A video RAM contains a dynamic RAM memory array *that feeds a serial shift register. This architecture allows a processor to load the parallel array at the same time that the video hardware is being fed by the serial shift register.*

45ns

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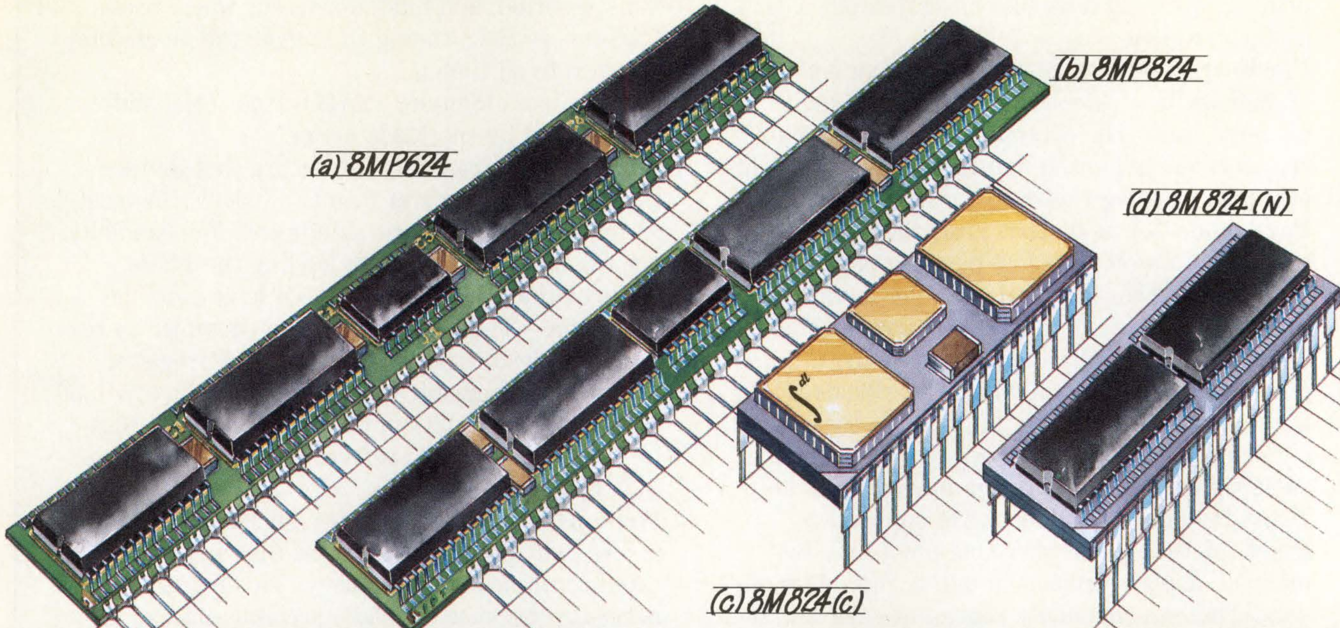

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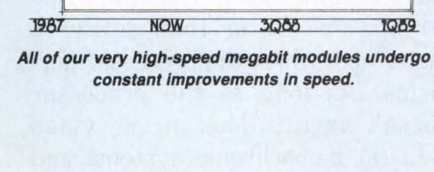

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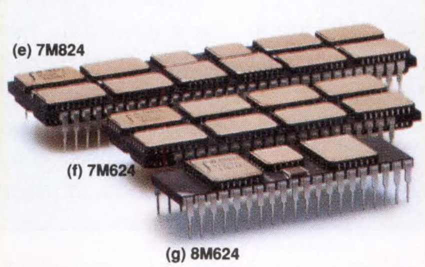

(a)	64Kx16	8MP624
(b)	128Kx8	8MP824 SIP
(c)	128Kx8	8M824(C) monolithic pinout
(d)	128Kx8	8M824(N) monolithic pinout w/SOICs
(e)	128Kx8	7M824 memory subsystem
(f)	64Kx16	7M624
(g)	64Kx16	8M624

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CIRCLE NO 165

A video-RAM glossary

BitBlt—A raster op.

Bit-mapped memory—A video memory organized so that each bit is associated with a pixel. In a color system, in which multiple bits represent a pixel, a pixel will have one bit associated with each color plane.

Flash write—The ability to change an entire row of memory in a video RAM array in a single memory cycle. The contents of an on-chip data register determine the nature of the change—for example, clearing the row or changing its color.

Page mode—A mode that gives the CPU fast access to data on the same memory page. Rather than strobing the row and then the column address, the row stays constant while the column adresses change. Virtually all video RAMs support fast page mode, in which the signals retain their relative characteristics, but are asserted at a much higher rate. (Fast page mode is not the same thing as enhanced page mode, which only Texas Instruments' video RAM supports.)

Pixel (picture element)—One point on a bit-mapped display comprising one or more bits of data. The bits commonly represent color and intensity.

Raster op—The transfer of a block of memory to another section of memory, while also performing a Boolean function on the source and destination data. One of the most common applications of raster ops is window creation. A raster op is also called a bit-block transfer, or BitBlt.

Refresh methods—Video RAMs support three types of refresh schemes for their dynamic-RAM arrays: RAS-only refresh cycles; write cycles on the 512 address combinations of A_{0-8} during an 8-msec period; and hidden refresh, which uses CAS-before-RAS timing to trigger the on-chip internal refresh timing.

Serial-access memory (SAM)—the serial shift register fed by the RAM array.

Split-register transfer—A feature that divides the serial shift register into two halves: the least significant and the most significant. You can shift out the MSBs while you're loading the LSBs. Without the split register, you'd have only one cycle time—30 nsec, for example—in which to reload the serial register. With the split register, you have the register cycle time multiplied by half of the number of bits in the register. For a 1024-bit serial register, therefore, this time would be 512×30 nsec=15 μsec.

Write-per-bit—The write-per-bit feature lets you access individual bits of a pixel that are not located contiguously in memory. This feature is necessary because bit-plane architecture can locate each bit of a pixel on different planes in different parts of memory, which makes altering an individual pixel more complex than altering an individual word. The write-per-bit feature speeds the process by allowing you to mask the bits in a word that are not associated with the pixel in question, so that you can get at the appropriate bit on each plane.

In addition, flash write is not much use in a windowing environment because it requires that the entire row be rewritten, thus preventing you from doing a fast fill or clear operation within a screen. Further, the trend in video memory is for more off-screen memory to be implemented with video RAM: Flash write can destroy off-screen memory because you can't mask locations from a transfer. You can simulate flash writes by using register-to-memory transfer cycles.

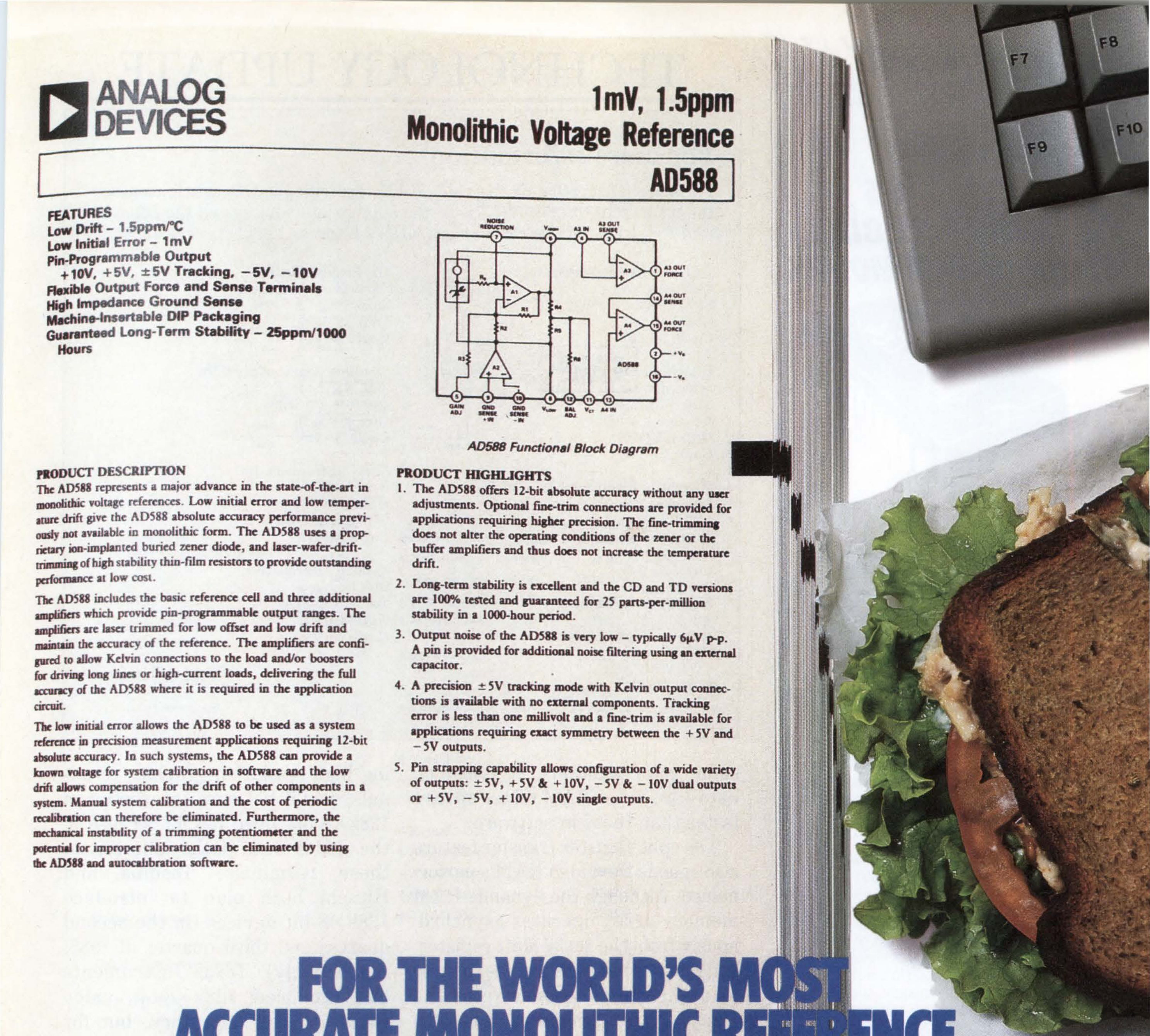
Unlike flash writes, which change the contents of entire lines of display memory, you can use block fills to color in bounded areas. (Many graphics applications consist mainly of colored shapes.) Without block fills, the processor must access memory one address at a time and change the data or color that's associated with each pixel. Because the same data will appear on the data bus of the same RAMs for several cycles, block fills can speed this boundary-filling process by broadcasting the color data to several memory locations within a single cycle.

Video RAMs that support block fills have on-chip logic that can write a given 4-bit data pattern to any combination of four adjacent memory addresses, allowing the CPU to write as many as 16 bits to the RAM in a single memory cycle.

Although block write is useful in area fills, you can also use it for clearing the screen. For example, clearing all 512 lines of display memory with flash write takes 102 μsec; using block write in page mode and with register-to-memory transfers takes 110 μsec. If speed is not critical, you can use a block write alone, at 4 msec.

On-chip raster ops

The Toshiba, Fujitsu, and Hitachi video RAMs support on-chip raster ops. To evaluate the importance of this feature, you'll need to examine your system needs and processor capabilities carefully. The advantage of incorporating raster ops in a video RAM is speed: Hardware raster ops are faster than software raster ops, which the processor performs. As long as the processor doesn't have to look at the video data (in monochrome systems and



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AD588 Functional Block Diagram

PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 and autocalibration software.

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Long-term stability is excellent and the CD and TD versions are 100% tested and guaranteed for 25 parts-per-million stability in a 1000-hour period.
3. Output noise of the AD588 is very low – typically 6μV p-p. A pin is provided for additional noise filtering using an external capacitor.
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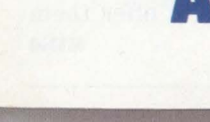

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For the most accurate reference on the AD588, call Applications Engineering at (617) 935-5565, Ext. 2628 or 2629. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

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Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 559-2037; Colorado: (303) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 251-9550; Austria: (222) 885504; Belgium: (3) 237 1672; Denmark: (2) 845800; France: (1) 4687-34-11; Holland: (1620) 81500; Israel: (052) 28995; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050

CIRCLE NO 178

For more information . . .

For more information on the video RAMs described in this article, contact the manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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some color systems, it doesn't), hardware video-RAM raster ops are faster than those in software.

The split-register transfer feature also speeds the video RAM's performance. Although the dynamic-RAM memory array operates asynchronously from the serial shift register, you must either synchronize them to load the shift register from the array, or use a scheme such as split-register transfer.

Speedy performance

Split-register transfer consists of dividing the register in two, giving you a least significant half and a most significant half. You can shift out the most significant bits while you're loading the least significant bits. Rather than trying to fit those operations into a tight timing window (one memory cycle), the processor only has to have the second half filled by the time the first half shifts out.

Initially, all 1M-bit video RAMs will be configured as 256k×4 bits. This size nicely supports video memories for PC and workstation displays. However, if you're designing high-resolution graphics terminals, you'll be more interested in 128k×8-bit video RAMs because of the wider data paths inherent in these terminals. Toshiba and Hitachi both plan to introduce 128k×8-bit devices (in the second quarter and third quarter of 1988, respectively). Texas Instruments has produced 128k×8-bit video RAMs in the laboratory, but for now has decided not to offer them commercially. **EDN**

References

1. Pinkham, Ray, "One megabit video RAM technology and applications," *TI Technical Journal*, March-April, 1987, pg 14.
2. Conner, Margery S, "Graphics engines," *EDN*, March 4, 1987, pg 112.

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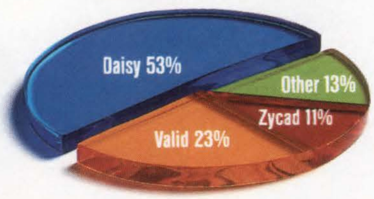

Simulation accelerator market share. Source: Prime Data, 1985 and 1986 unit shipments.

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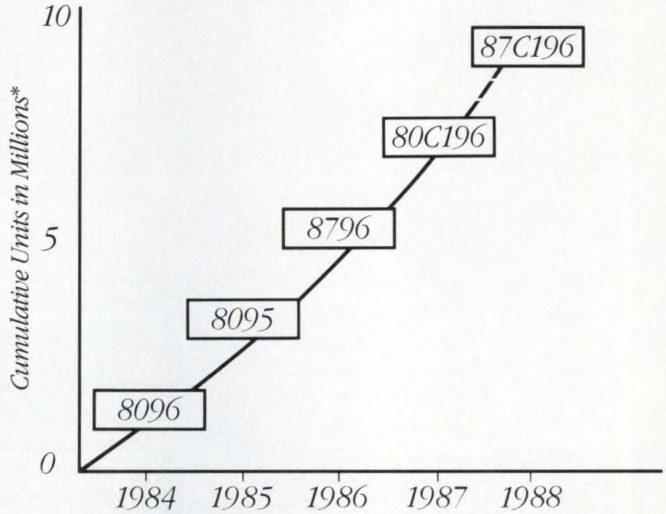

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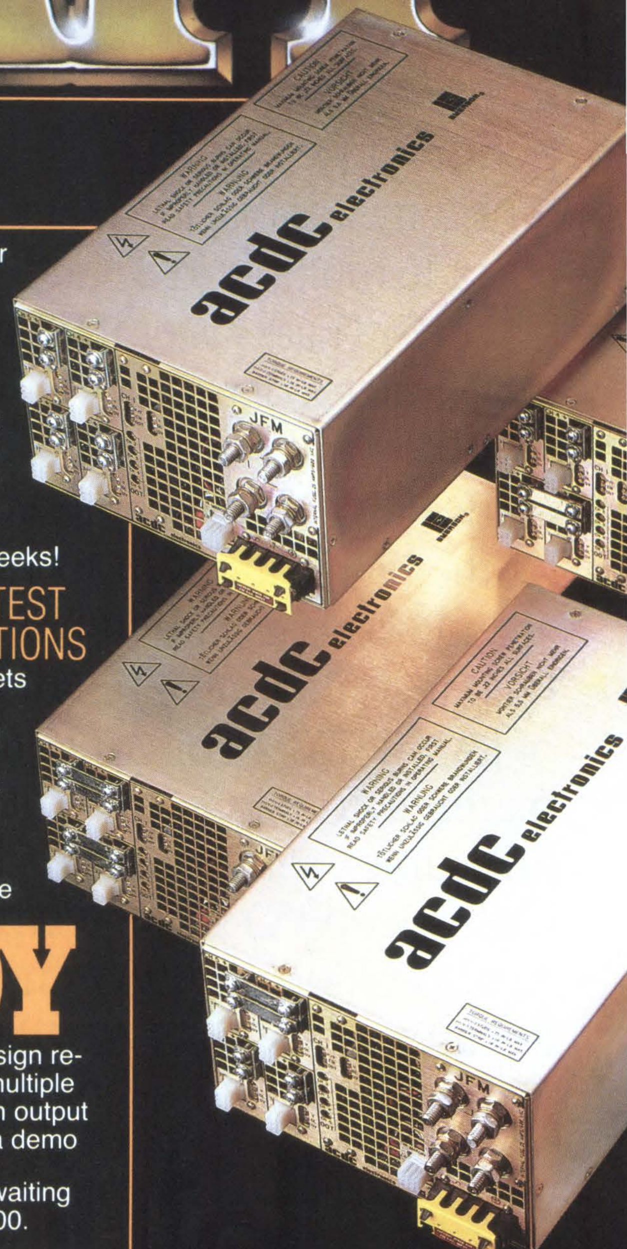

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5V/200A	TABLE B	TABLE B	TABLE B	TABLE B

TABLE A AUX's	TABLE B AUX's
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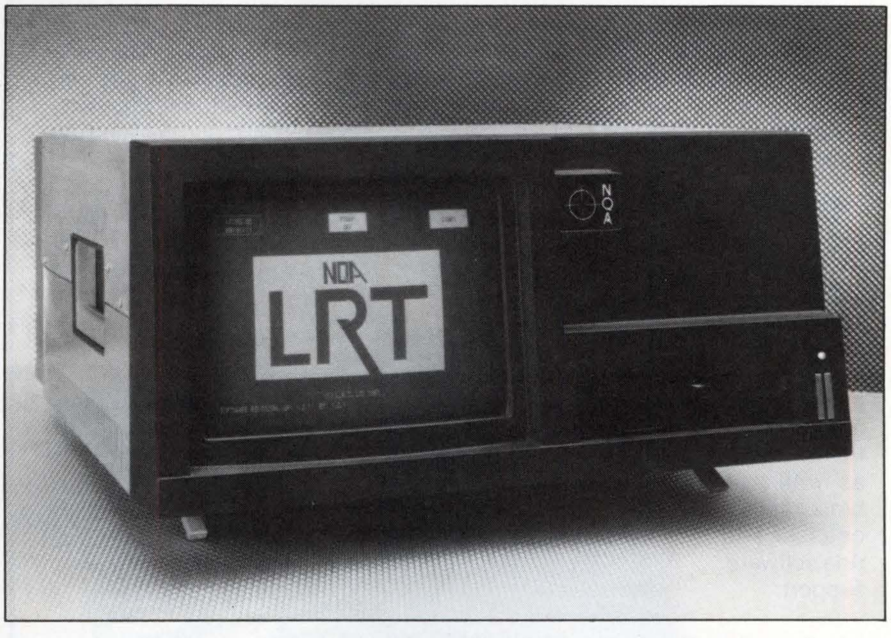
LAN analyzer diagnoses Ethernet faults before they cause system failures

Because the OSI (Open Systems Interconnection) layer-4 protocols used in IEEE-802.3 (Ethernet) LANs automatically retransmit packets that contain errors, users don't usually notice gradual degradation of network performance until it causes the network to crash. However, by using the NQA network quality analyzer to monitor your network, you can pinpoint and repair network flaws before the network becomes inoperative. The analyzer examines both the physical (layer 1) and data-link (layer 2) characteristics of the LAN. Unlike other physical-layer testers, it can also perform TDR (time domain reflectometer) tests to locate major cable and transceiver defects while the LAN remains in service.



By simultaneously performing in-service cable tests and protocol analysis, *the NQA network quality analyzer pinpoints Ethernet faults in particular network nodes. The analyzer can also perform in-service TDR tests to locate cable faults.*

Without disturbing normal traffic on the LAN, the analyzer measures five coaxial-cable signal parameters for each transmitted Ethernet packet—that is, jitter, dc component, ac component, fall time, and bit rate. By examining the framing information for each packet to determine the source of each packet, the analyzer can correlate these cable measurements with particular network nodes. In addition, the instrument measures the network bias (the voltage on the cable caused by the transceivers' bias currents). Measurements are displayed graphically on the instrument's 9-in. CRT, along with the appropriate limit values that are specified in the IEEE-802.3 standard. Because these measurements are a good indicator of the network's state of health, periodic testing of the LAN with the analyzer allows you to predict when a network failure is likely to occur.

A special cable implant unit that you can position anywhere in the network allows you to perform TDR measurements. To perform in-service TDR tests, the analyzer drives the Ethernet cable with a bias voltage that causes all network nodes to back off from the network for approximately 0.1 sec. During this time, the analyzer drives a series of pulses to the cable and examines the reflections that occur at discontinuities in the cable's impedance. The results from a large number of pulses are digitally processed to establish the location and magnitude of each reflection. By examining the trace you can identify a variety of cable faults, including short or open circuits and improperly installed transceivers.

The positional accuracy in determining the locations at which reflections occur is ±1.2m (excluding variations in the coaxial cable's propagation velocity), and the range of the TDR measurement is greater than 500m on both sides of the implant unit. If you have a map of your network, you can annotate the distance axis of the screen display with network node identifiers. Also, because the reflectometer trace is digitized, you can zoom in on a small portion of the trace, store it on disk, or compare it with previously acquired traces.

The analyzer's layer-2 protocol-analysis functions allow you to build up a source/destination matrix of network activity, to monitor individual station characteristics, or to obtain general network statistics—for example, bandwidth utilization, packet density, and collision rate. Although the analyzer examines the layer-2 protocol to determine a packet's source address, destination address, and its cyclical redundancy check, the packet's data isn't decoded. As a result, use of the analyzer by service engineers won't constitute a breach of network security. If you do want to examine the data, optional protocol decoding and analysis software is available for the unit.

Because the NQA detects degradation of LAN performance before the network crashes, it can use the LAN under test to communicate with other equipment. For example, you could control and interrogate the analyzer from an Ethernet terminal or host computer. To provide distributed network monitoring—for example, on either side of a bridge between two networks—a special measurement pod that the company is developing will contain only the front-end-measurement capabilities of the NQA analyzer. You'll be able to upload the pod's test results via the network into a central NQA analyzer to evaluate them or log them on disk. The company also intends to provide an ISDN (Integrated Services Digital Network) interface to link the units together.

To simplify the operation, you drive the NQA analyzer via its touch-sensitive screen and soft-key menus. The standard unit has a 360k-byte floppy disk on which you can store recorded information or test programs. You can optionally install a 40M- or 100M-byte hard disk. Operating with a time resolution of 5 minutes, the analyzer's internal RAM can record over 24 hours of data, the floppy disk can record for over 30 days, and the hard disk can record for over a year. A Centronics printer port and graphics command set allow you to download screens to a printer. The NQA analyzer costs approximately $25,000.—***Peter Harold***

Logic Replacement Technology Ltd, Arkwright Rd, Reading, Berks RG2 0LU, UK. Phone (0734) 311055. TLX 847395.

Circle No 659

Single-chip, 64-bit floating-point processor offers 32-word register file

The WTL 3364 floating-point processor integrates on one chip a 64-bit floating-point multiplier, a 64-bit floating-point ALU, a divide/square-root unit, and a 32-word×64-bit register file with six ports. This chip can execute as many as 20M flops, and its architecture gives you much of the flexibility you get with multichip-set, floating-point processors; it also helps you save money and board space.

The 3364 provides single-cycle throughput on all multiplier and ALU operations. In addition, the on-chip register file lets you operate the multiplier and ALU simultaneously, even when using independent operands. To understand how this works, you need to understand how the register file is configured.

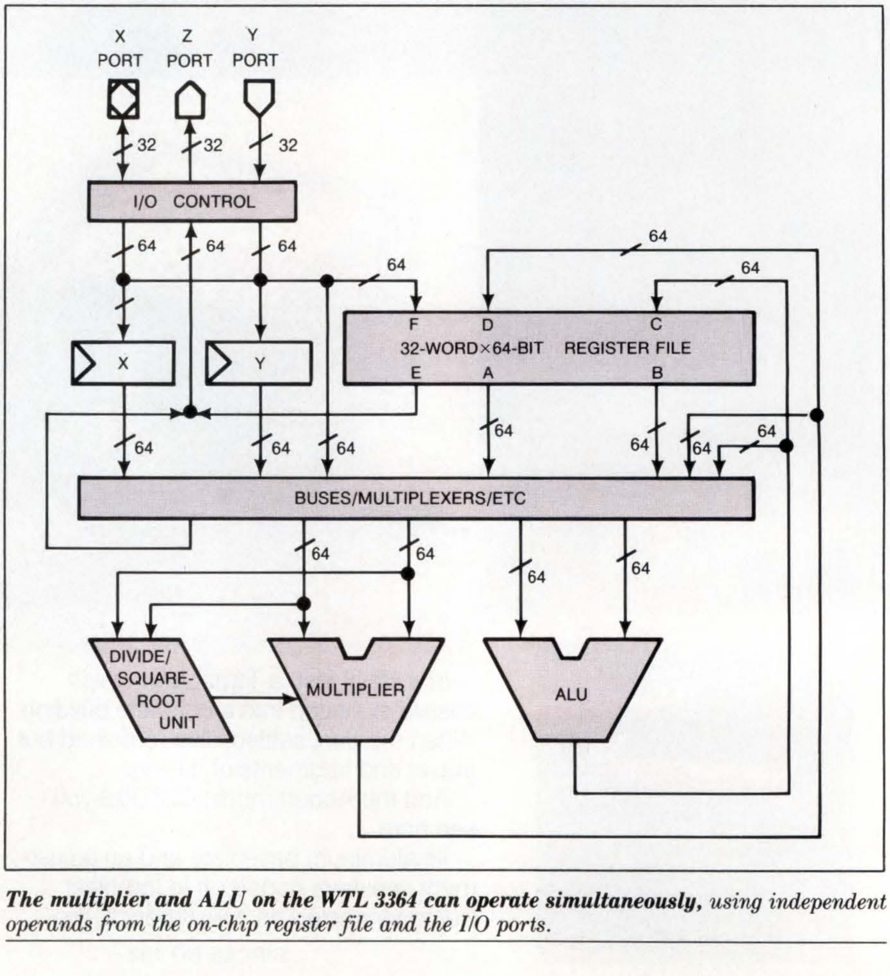
The register file has three read ports and three write ports. You can use two of the read ports to supply two of the four operands required for simultaneous and independent use of the ALU and multiplier. The other two operands can come from the external X and Y input ports. You can write results from the ALU and multiplier to the register file simultaneously, using two of the write ports. The third write port allows you to load the register file with external data, and the third read port allows you to store data from the register file externally.

The register file also supports bypassing on loads, on stores, and in register-to-register operations. This bypassing function saves you one cycle of latency in each case. For example, bypassing on loads means that you can load data into the register file and use it as an operand on the same cycle. Bypassing on register-to-register operations means that you can write the result of an arithmetic operation into the register file and use this same result as an operand of an immediately following operation—all in the same clock cycle.

The processor has three 32-bit I/O ports configured as one input port, one output port, and one bidirectional port. You can also use these three ports as a single 64-bit bidirectional port. All three ports can be single or double pumped. Single-pump mode allows you to transfer one 32-bit data word/clock cycle on each port, and double-pump mode allows you to transfer two 32-bit data words/clock cycle on each port.

The on-chip divide/square-root unit can operate in parallel with the multiplier and ALU. During the first clock cycle of the divide/square-root operation, no other operations can take place. However, once the divide/square-root operation begins executing, the multiplier and ALU perform functions in parallel. For example, during 29 of the 30 clock cycles required for the double-precision IEEE square-root operation, which is one of the more time-consuming operations, the multiplier and ALU can also be executing operations in parallel.

The device conforms completely to the IEEE standard for binary floating-point operations. This



The multiplier and ALU on the WTL 3364 can operate simultaneously, *using independent operands from the on-chip register file and the I/O ports.*

standard gives you IEEE representation of floating-point numbers and IEEE exception handling.

Microcoding is a time-consuming task with any floating-point processor, and the WTL 3364 is no exception. This chip does, however, have features that help simplify your microprograming task.

First, the 6-port on-chip register file allows you to use a register-based programming model rather than a bus-based model. Register-based programming models are usually simpler and easier to program.

Second, both the source of the operands and destination of the results are specified in the same instruction. The chip automatically delays destination addressing to match the latency of the operation, so you don't have to keep track of the time when a result becomes available.

Third, all operations except divide and square root have a register-to-register latency of two cycles (in the 2-cycle latency mode). Whether you use the multiplier or the ALU with floating-point or integer operations, the results all have the same latency; thus, you have one less variable to keep track of when you're microprogramming.

For computer and cost-sensitive applications where high I/O bandwidth is of secondary importance, you can use the WTL 3164. This chip is functionally identical to the WTL 3364 except that the 3164 has one 32-bit bidirectional I/O port and comes in a 144-pin PGA package.

The WTL 3364 is mounted in a 168-pin pin-grid array. Samples of the 100-nsec version of the WTL 3364 and the WTL 3164 are now available; volume deliveries are scheduled for July. The WTL 3364 costs $909; the WTL 3164 is priced at $829.—***Doug Conner***

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Circle No 663

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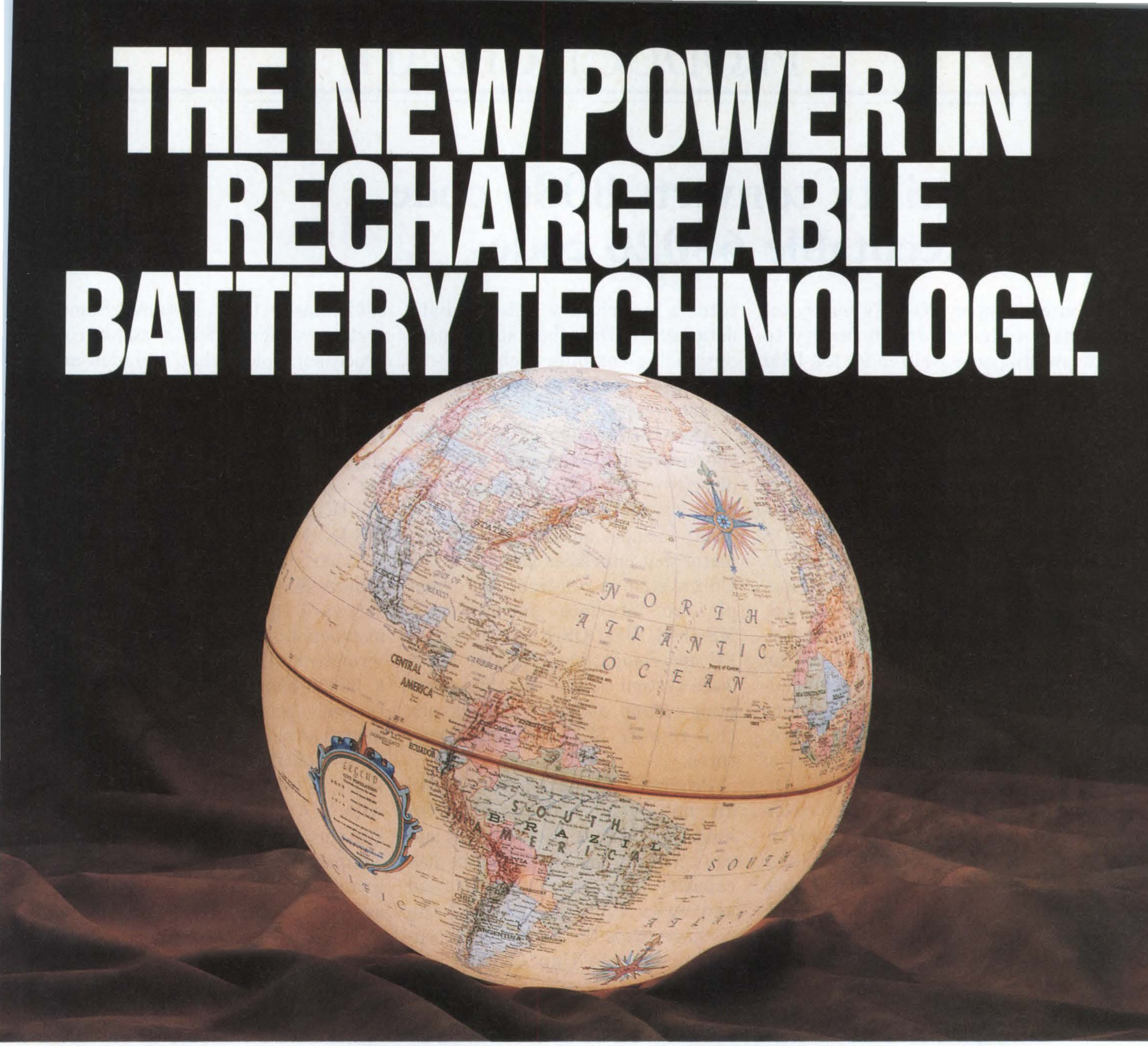

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CIRCLE NO 161

Unix utility converts 8086 code into executable 68020 code

You can employ XDOS's binary-to-binary-code-conversion facility to allow programs written for the IBM PC and compatible computers to execute on Unix-based systems. This Unix utility program for 68020-based systems includes a binary compiler that performs the code conversion and an environment emulator that emulates the MS-DOS operating-system environment. It permits the end user to simultaneously execute multiple, converted, PC programs in Unix windows.

System designers and OEMs can use XDOS as a bridge between multiuser, multitasking Unix systems and personal-computer software. The utility addresses the needs of end users in scientific-, CAE/CAD-, and business-computing environments, who require the performance potential of Unix-based systems but who must also use such widely employed IBM PC application software packages as WordPerfect and Lotus 1-2-3.

XDOS converts MS-DOS programs without modifying them. The utility performs a 2-stage conversion. First, the binary compiler performs an instruction-decode and flow-analysis operation and generates a proprietary, intermediate data format. Then the compiler uses optimizing-compiler techniques to generate executable code for the target system.

After the compiler has performed the conversion, the end user can directly execute the program on the Unix system, because the XDOS utility includes an environment emulator that interfaces the code to the Unix system at run-time. For example, an interface library maps MS-DOS, MS-DOS BIOS, and IBM PC and compatible-computer hardware system calls to the Unix operating system, and also manages calls that require MS-DOS data structures.

Programs converted with XDOS are not affected by the MS-DOS limit on 32M-byte disk volumes and can therefore use the full Unix disk capacity. The programs can read and write Unix files because the package maps the MS-DOS file environment into Unix. XDOS also provides a Unix utility that reads MS-DOS files.

The XDOS utility provides an alternative to the two principal means currently offered by system vendors for adding MS-DOS compatibility to 68020-based Unix systems. Some system vendors offer an add-in coprocessor board that includes an Intel 8086-family μP. Adding a coprocessor, however, limits you to executing MS-DOS programs in a single-tasking mode. Furthermore, the coprocessor requires a copy of MS-DOS, in addition to Unix, to run MS-DOS software.

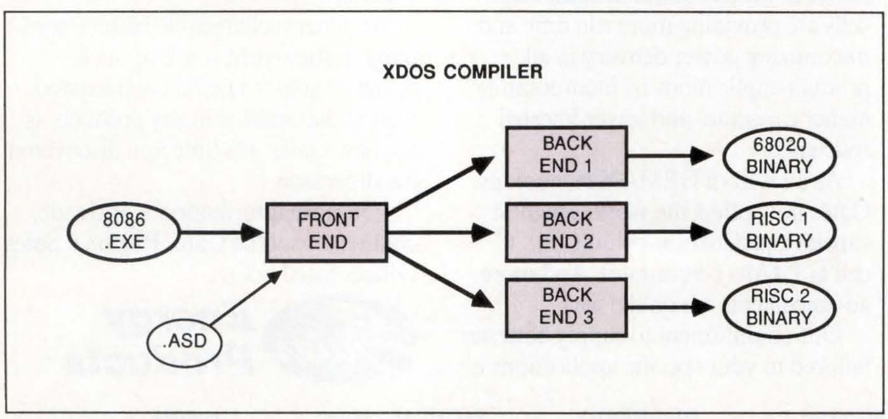
Other system vendors attempt to achieve MS-DOS compatibility with software that simulates the 8086 instruction set and the MS-DOS environment. Using such software on a 68020-based system, however, typically provides only the performance level of an IBM PC, PC/XT, or compatible computer. In contrast, when programs converted with XDOS execute on 68020 target systems their performance level is comparable to that of source programs executing on 80386-based systems.

The company has certified XDOS for use with most popular MS-DOS business software. The software is currently available for 68020-based systems. OEMs can license the software on a royalty basis. The suggested end-user pricing ranges from $425 to $2000, depending on the number of users the Unix system supports.

The company also plans to offer XDOS for systems with non-68020 processors, such as RISC-based Unix systems. To implement XDOS on other processors, the software designer must write a front end to the XDOS compiler that generates the processor's proprietary intermediate code.—***Maury Wright***

Hunter Systems, 444 Castro St, Mountain View, CA 94041. Phone (415) 965-2400.

Circle No 662



***The 2-stage binary compiler** used in XDOS will allow the software to be ported to many processor environments. Each port to a new processor requires the software designer to develop a front end that performs flow analysis and generates intermediate code.*

Floating-point, array-processor boards add computation power to PCs

Based on AT&T's DSP32 floating-point DSP chip, DSP32-PC add-in boards accelerate general-purpose math applications on the IBM PC, PC/AT, and compatible computers. The family of floating-point array processors includes an 8M-flop, IBM PC half-card version and a 25M-flop, full-card IBM PC, PC/AT version. The PC version performs a 1024-point complex FFT in 14 msec, an FIR filter at 250 nsec/tap, and a 3×3 matrix multiplication in 7 μsec; the PC, PC/AT version performs a 1024-point complex FFT in 3.25 msec, an FIR filter at 80 nsec/tap, and a 3×3 matrix multiplication in 2.2 μsec.

If you develop computation-intensive applications, such as signal processing, graphics, image processing, scientific computing, CAE, CAD, and CAM, the DSP32-PC floating-point array processor will let you employ your PC to host your software. The board's analog and digital interfaces also suit it to practical applications, such as process control and speech analysis. For example, the DSP32-PC's modular phone connector lets you record and store speech on a hard disk for analysis and playback, and its 8-bit codec, which provides D/A and A/D conversion, also features lowpass and bandpass filtering for processing speech signals.

You can purchase software-development-support tools for the DSP32-PC separately or as a complete development system comprising the array-processor board, an assembler, a window-based emulator, demonstration programs, and a library of optimized assembly-language applications.

The library contains 57 commonly used math routines and a number of signal-processing, image-processing, and graphics routines. Among these are routines for real and complex FFTs, FIR filters, and Hamming window functions, as well as a graphics routine that converts 16-bit color pixels to 5-bit, gray-scale values, and an image-processing routine that performs a histogram equalization algorithm for gray-scale images.

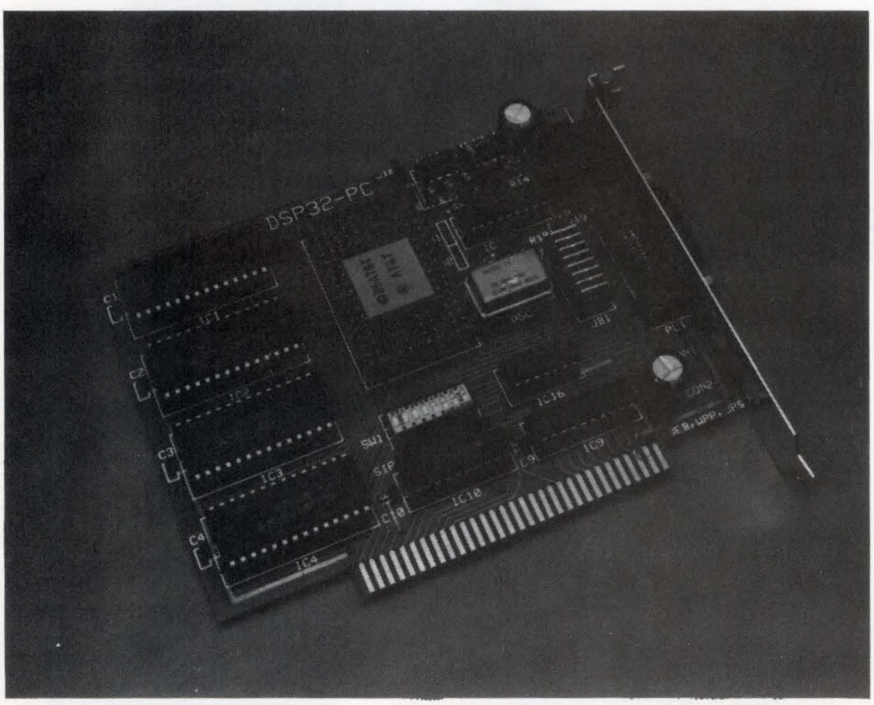
The vendor plans to ship a C compiler for the array-processor board by June. The compiler will let you code the bulk of your applications in C and speed-critical portions of your core algorithms in assembler language. The compiler will come with a math library.

The 25M-flop IBM PC, PC/AT version, based on the 80-nsec CNOS DSP32C IC, will include as much as 256k-bytes of static RAM. The vendor will begin shipping the board when quantities of the IC are available, by the beginning of the fourth quarter.

The 8M-flop, IBM PC version of the DSP32-PC, based on the 250-nsec NMOS version of the DSP32 IC, is available now and costs $695. It includes 32k bytes of zero-wait-state static RAM; you can obtain it with 128k-bytes of static RAM for an additional $50. The DSP32-PC's C compiler will cost $1500. The development system—the array-processor board, assembler, window-based emulator, demonstration programs, and applications library—costs $995. —***Maury Wright***

Communications Automation & Control, 2348 Eden Lane, Bethlehem, PA 18018. Phone (215) 865-9706.

Circle No 661



The 8M-flop array processor *for IBM PCs and compatible computers lets software developers use their PCs to host computation- intensive applications, such as graphics, image processing, and speech analysis.*

IEEE-488 interface for Mac transfers 800k bytes/sec

The MacSCSI 488 interface, which provides transparent data translation for as many as 14 IEEE-488 instruments and peripherals, plugs into the Small Computer Systems Interface (SCSI) port of your Mac Plus, Mac SE, or Mac II computer to facilitate data transfers at 600k bytes/sec for the Mac Plus and Mac SE, and at 800k bytes/sec for the Mac II. Because the modem-sized MacSCSI 488 is a stand-alone unit, it conserves your Mac's expansion slots and doesn't require disassembly of your computer for installation.

The unit achieves its data-transfer speeds by acting as a pipeline between the host computer and your SCSI instrument, translating protocols via the MacSCSI 488's internal μC during transmission. Other SCSI controllers for the Macintosh computer translate instrumentation data into Forth, thus adding an interpretation step before conversion.

The MacSCSI 488 will not interfere with operation of any external hard-disk drives controlled via your Macintosh's SCSI port. The unit comes with software device drivers that let you program it in many popular languages such as Microsoft BASIC 3.0, Turbo Pascal, Lightspeed C, VIP, and Hypercard.

You can write IEEE programs for the MacSCSI 488 using high-level Hewlett- Packard-style commands, such as ENTER, OUTPUT, CLEAR, and SPOLL (serial poll). The use of such high-level commands makes programs for the MacSCSI 488 shorter and more readable than programs that rely entirely on low-level, bus-transaction commands. But, if you prefer, you can instead program the unit with low-level commands such as UNT (untalk), UNL (unlisten), and MLA (my listen address).

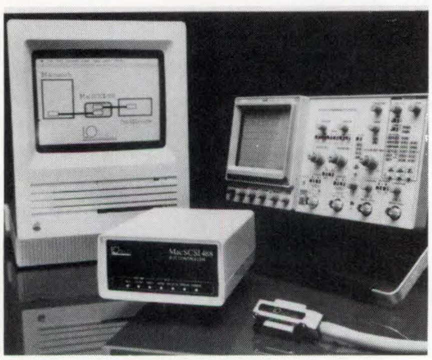
The unit includes a memory resident desk-accessory program that makes IEEE programming a utility of your Macintosh's software system. The desk-accessory software lets you acquire and save data from an IEEE-488 instrument while you running an application program on your host computer. For example, the program will let you set up an experiment and acquire data from an oscilloscope or DMM, and then paste that data into a spreadsheet program.

The MacSCSI 488 sells for $795, including language drivers and desk-accessory software.

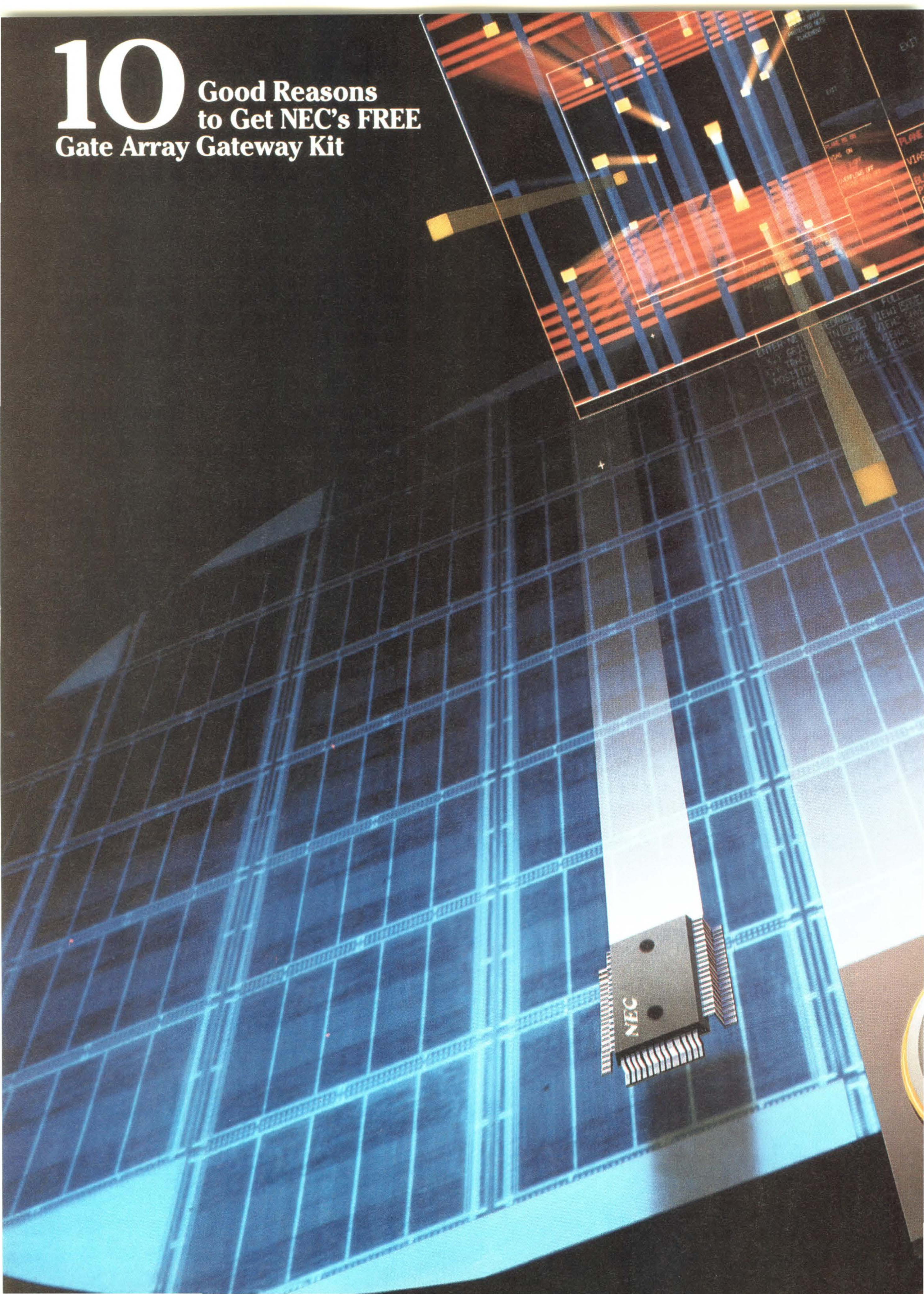
—*J D Mosley*

IOtech Inc, 23400 Aurora Rd, Cleveland, OH 44146. Phone (216) 439-4091. TWX 650-282-0864.

Circle No 660



Providing IEEE-488 control *for the various Macintosh computers at communication speeds ranging from 600k to 800k bytes/sec, the modem-sized MacSCSI-488 interface lets you connect as many as 14 instruments to your computer.*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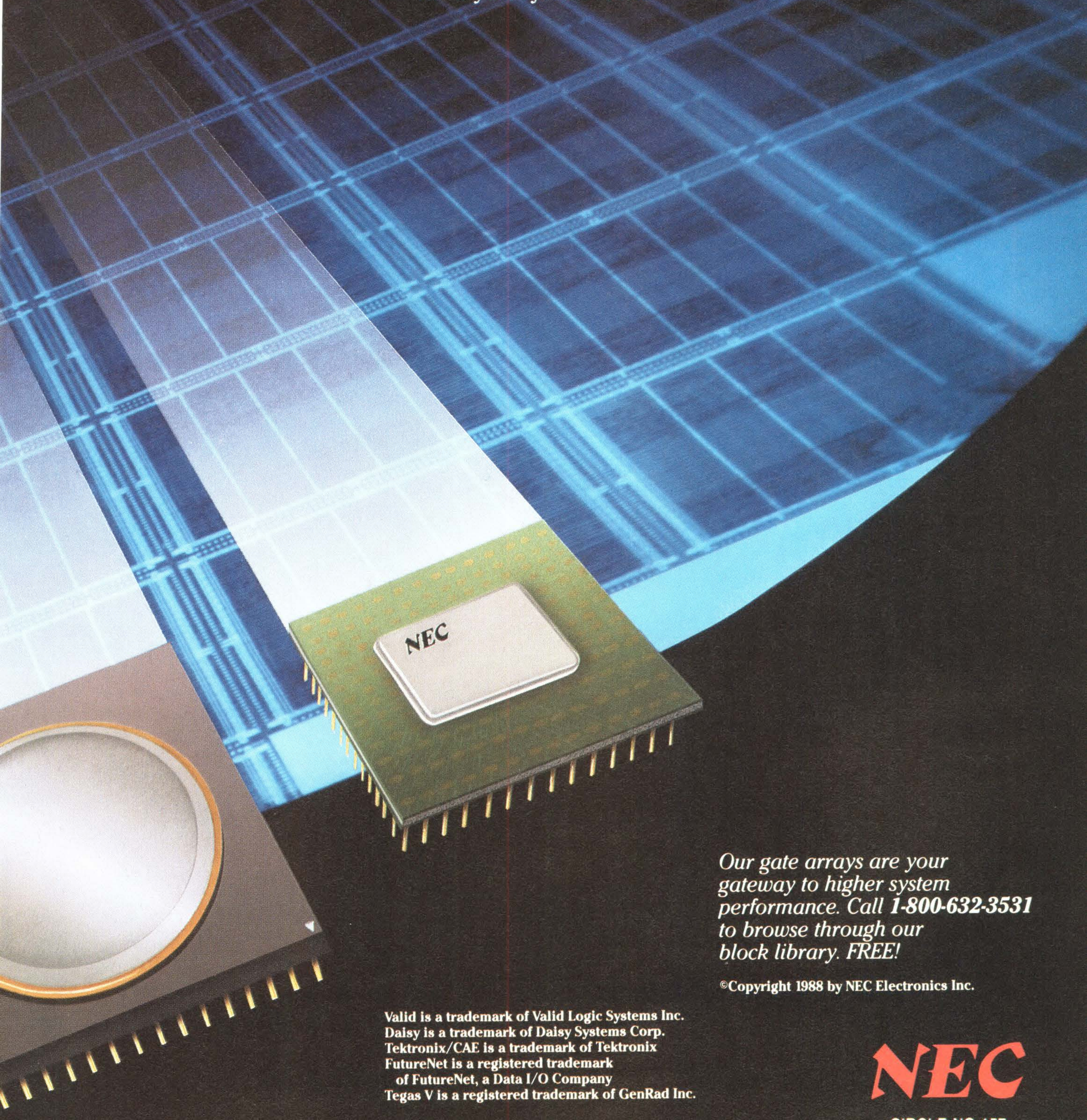
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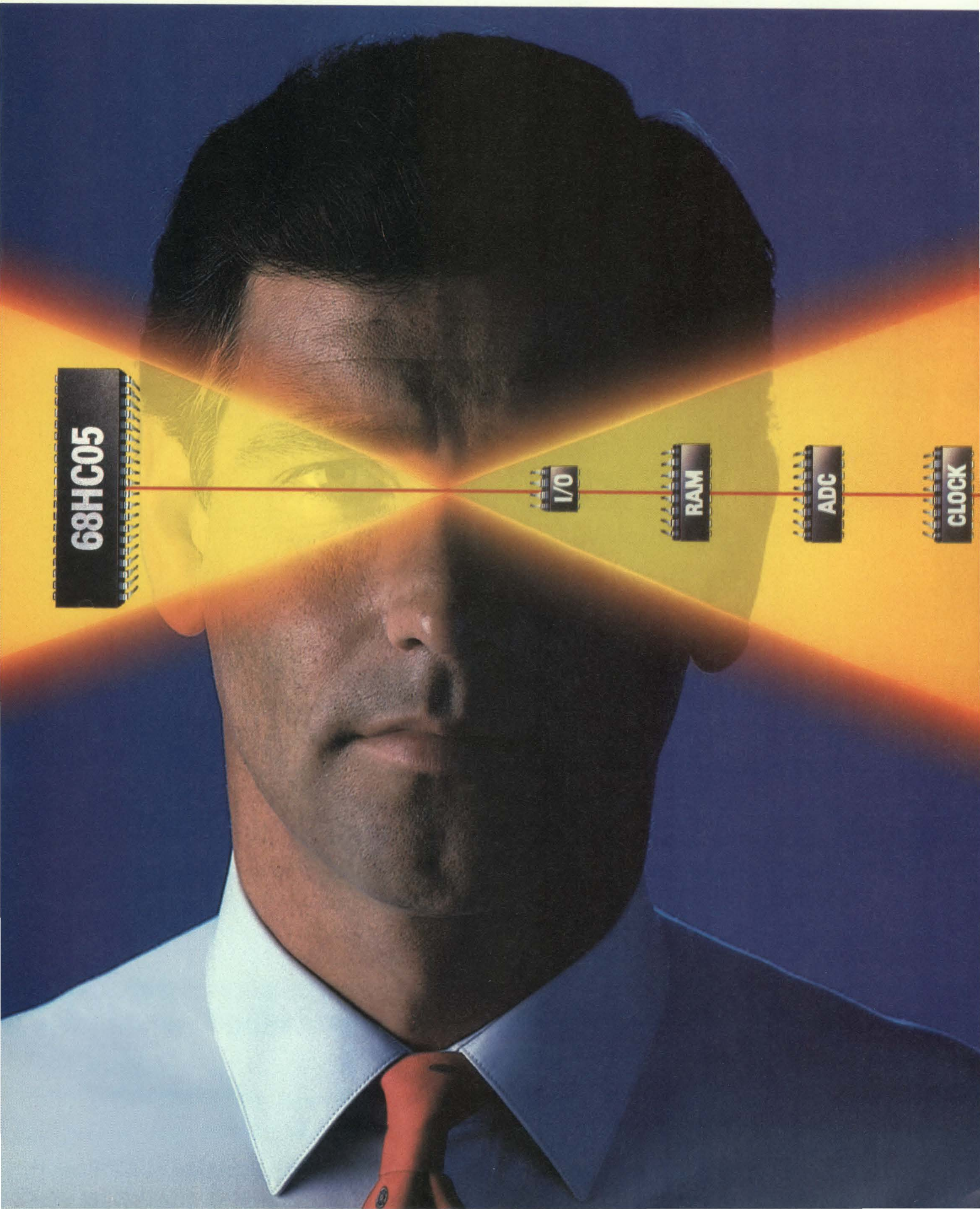

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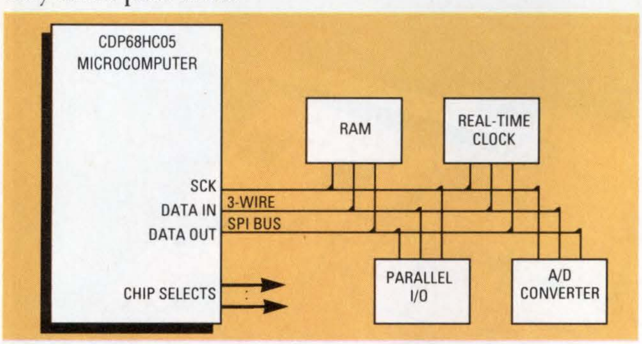

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The real beauty of the SPI is that it eliminates limitations imposed by microcomputers.

For example, you can easily extend the amount of I/O or memory with SPI RAMs, I/O chips or shift registers. And the modular SPI bus gives you the ability to expand without losing lots of PC-board space. Reduced package sizes and minimized interconnect wiring lead to reduced board size.

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On-Chip User ROM (bytes)	4160	7744	2176	2176
Bidirectional I/O Lines	24	24	28	16
Unidirectional I/O Lines	7 inputs	7 inputs	3 inputs	3 inputs
Timer size (bits)	16	16	16	16
Prescaler size (bits)	*	*	*	*
External timer oscillator	no	no	yes	yes
Serial peripheral interface	yes	yes	yes	no
Serial communications interface	yes	yes	no	no

*prescaler fixed as ÷4

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If you need another reason to choose our 6805 family, here it is: they're so easy to prototype with our Piggyback! We have the 68EM05C4 and 68EM05D2 Emulators, custom 40-pin packages that contain the C4/C8 or D2 micros with a Piggyback EPROM socket.

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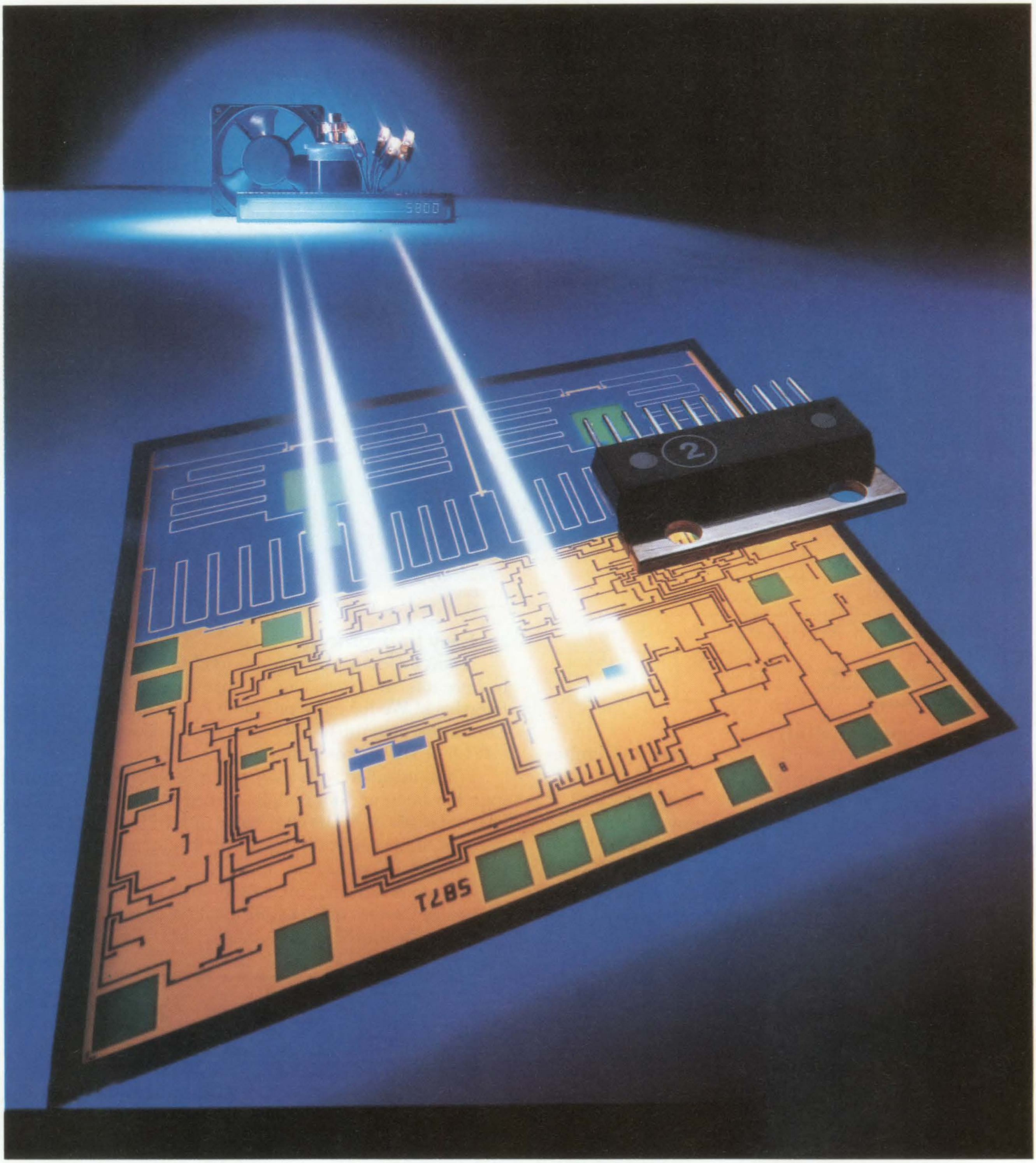
Although largely hidden in custom applications in the past, smart-power ICs are now becoming available as standard products that satisfy a variety of applications, and semicustom ICs suit designs where custom versions are cost prohibitive. Whether semicustom or standard, available devices depend greatly on the IC process technology.



***Today's smart-power ICs** find extensive use in a variety of motor-control applications. (Photo courtesy Sprague Semiconductor)*

KEEPING AMERICA COMPETITIVE

Smart-power ICs

Dave Pryce, *Associate Editor*

Smart-power ICs are not yet a major factor in replacing the various combinations of logic and power needed by a multitude of applications that currently use discrete power devices and monolithic ICs. However, the trend is definitely in the upward direction. The growing availability of monolithic smart-power ICs is making the devices increasingly attractive as alternatives to discrete solutions. In order to make intelligent decisions about these intelligent ICs, you should be aware of the recent product introductions by several manufacturers that are investing heavily in the smart-power niche. First, though, it might be useful to survey some growth figures that characterize the smart-power market.

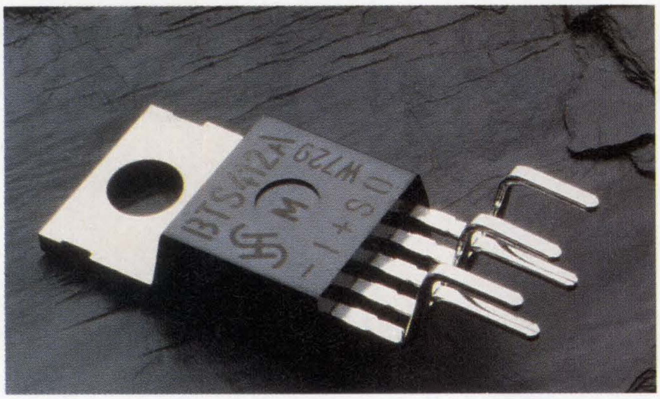
Electronic Trend Publications (Saratoga, CA) in a report, "Smart-Power Markets and Applications," estimates that smart-power ICs will represent only 9% of the total available market in 1988, growing to 33% by 1995. The most significant projection, however, is the switch from custom to standard products. ETP estimates that custom devices will decline from 70% of all smart-power ICs in 1988 to 25% in 1995, while standard products will increase in use from 13% to 60%. Semicustom power devices will constitute 17% of smart-power in 1988 and 15% in 1995.

The significance of these figures is that manufacturers of equipment produced in relatively low volume can now begin to avail themselves of the benefits of smart-power technology through the use of standard parts. Custom parts are often inexpensive on a piece-part basis, but manufacturers must have large-volume production runs in order to amortize the engineering charges, which are typically in the range of $50,000 to $100,000. Semicustom ICs will continue to play a limited role for unique circuit requirements in which production volumes are moderate. The lower engineering charges for semicustom circuits (typically in the range of $10,000 to $20,000) do not have as great an impact on unit costs as do those for full-custom circuits. For many manufacturers, however, the increasing availability of a wide range of cost-effective standard parts will be the key to unlocking the door to the use of smart-power ICs.

Cost effectiveness depends on technology

Cost effectiveness is very much dependent on the IC vendor's available technology. As one marketing manager for a major semiconductor firm put it, "No one needs a $4 solution to a $1.50 problem." The truth of such statements seems obvious, but it's often overlooked in the attempt to combine several discrete functions that use different processing technologies into a single integrated circuit. Although hybrid ICs generally represent a more expensive approach than monolithic designs, the merging of processing technology is not a major problem with hybrids—it is a relatively simple

Forecasts indicate that custom versions of smart-power ICs will decline in use from 70 to 25% between 1988 and 1995, while standard products increase 13 to 60%.



This 5-lead TO-220 package is the carrier of choice *for a large number of smart-power ICs, including the Siemens BTS412A. The package's metal tab provides a substantial amount of heat-sinking capability, particularly when the tab is attached to additional pc-board copper.*

matter to combine individual bipolar, CMOS, and DMOS chips on the same hybrid substrate.

The fabrication of diverse technologies into a single monolithic IC, however, is not a trivial matter. Merged-technology chips require complex layout and processing techniques that are difficult to master. In many cases, the number of mask layers alone is a deterrent to economical fabrication. The monolithic-IC manufacturers that successfully manage the complex tasks of merged technology—at high production yields—will be the winners, whether the final product is a custom, semicustom, or standard off-the-shelf device.

An example of the leading-edge technology required in the fabrication of smart-power chips is the Multipower-BCD (Bipolar-CMOS-DMOS) process **(Fig 1)** that SGS-Thomson Microelectronics uses for many monolithic chips. Multipower BCD allows the integration of CMOS, vertical DMOS, lateral DMOS, and bipolar npn and pnp transistors on the same chip. Most smart-power technologies require a drain contact at the bottom of the die (substrate) in the fabrication of vertical DMOS devices. This requirement means you can have only one power device (or several having common drains) on each chip. This type of construction also limits the output DMOS device to low-side switching where the load is between the device and the supply voltage, and the drain of the DMOS device is connected to ground. Other technologies allow the integration of lateral DMOS devices, which you can use as high-side switches or drivers, but these transistors are not usually power devices.

The BCD technology used by SGS-Thomson is different. It allows the integration of multiple, isolated, vertical DMOS power transistors that you can use for any output-stage configuration **(Fig 2),** including low side, high side, half bridge and full bridge. Motorola Semiconductor's SmartMOS processing technology offers similar capabilities for providing vertical and lateral power devices. Other manufacturers use different approaches to combine bipolar or CMOS logic with bipolar or DMOS output stages. All have their place, depending on the final smart-power application.

No less important than processing technology, packaging techniques are also playing a major role in obtaining maximum performance from smart-power chips. To dissipate the heat generated by the chips, manufacturers commonly use DIPs whose copper lead frames have the four center pins tied together for heat sinking the chip to the pc board. For high-power appli-

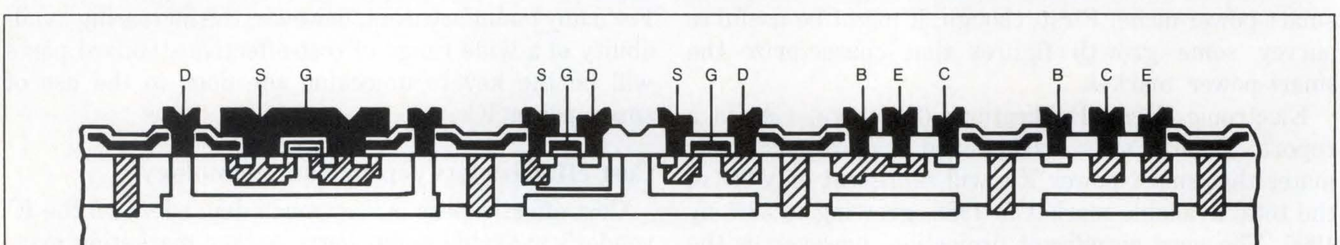


Fig 1—Merged-technology chips require complex processing. *Multipower-BCD technology from SGS-Thomson combines bipolar linear, CMOS, and DMOS power devices on the same monolithic chip. The bipolar and CMOS devices are rated at 20V; the DMOS devices at 60V.*

cations, 5-lead TO-220 and metal-tabbed, 15-lead Multiwatt packages provide greater power-dissipation capabilities. Hybrid circuits, of course, come in a variety of package styles and shapes designed to satisfy particular needs. On-going efforts in package development will likely provide further innovative solutions to the problem of heat removal.

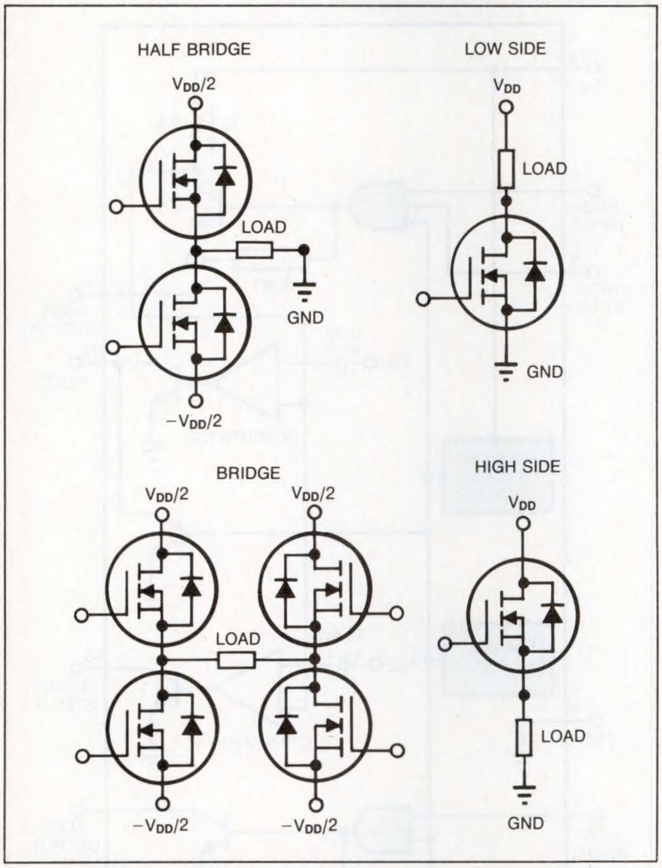


Fig 2—Versatile processing technologies, *such as Multipower BCD from SGS-Thomson and SmartMOS from Motorola, allow the integration of any output-stage configuration: low-side, high-side, half-bridge, and full-bridge topologies.*

What is smart power?

The term "smart power" is something of a misnomer —it has become a marketing catchword, and its meaning is subject to different interpretations. Some IC manufacturers label their power drivers as smart-power ICs simply because the devices have latched inputs. Some manufacturers of monolithic ICs say that you should not include hybrids in the smart-power category. And, of course, you could argue indefinitely about how much intelligence and power it takes to qualify a device for the smart-power category.

This editor's personal definition includes both monolithic and hybrid ICs, a *significant* amount of intelligence, and a power-output capability of at least 1W. The device's power output can be any combination of voltage and current whose product equals 1W; the device need not have amperes of output-current capability. Moreover, the device's intelligence must be internal to the device, rather than external. For example, a device that protects itself against short circuits, overloads, high temperatures, and excessive dissipation is certainly "smart."

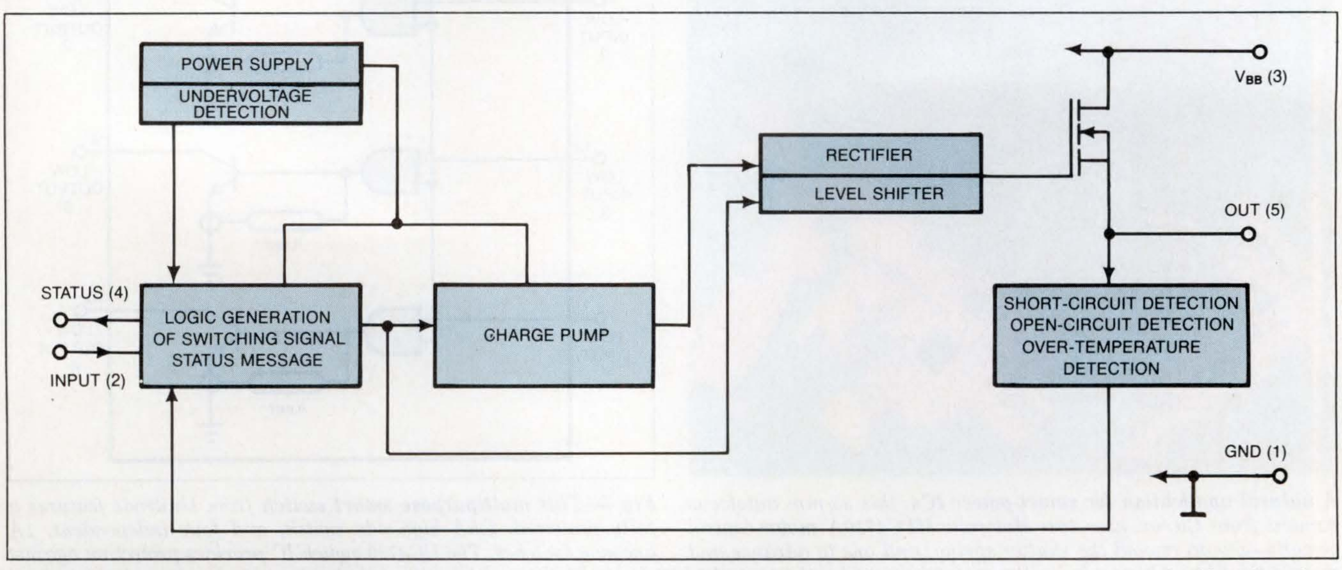


Fig 3—This power switch has a significant amount of intelligence. *The BTS-412A high-side switch from Siemens protects itself against short circuits, overloads, undervoltage, and excessive junction temperatures.*

The term smart power has become a marketing buzzword. It's defined here as any circuit that has significant intelligence and a power capability of at least 1W.

One example of a device that fits this internal-smartness category is the BTS-412A from Siemens **(Fig 3),** an intelligent monolithic power switch in a 5-lead TO-220 package. Fabricated in a process Siemens calls Smart SipMOS, the device has a high-side switching capability that meets the ground-return requirements of automotive applications. The BTS-412A has a current rating of 12A and works in a voltage range between 7 and 35V; you can use it in both 12 and 24V applications. The output power switch is connected as a source follower; its gate voltage is kept about 6V higher than the positive supply voltage by means of an internal charge pump. The gate resistance determines the switching speed of the device. Internal logic circuitry uses low-voltage CMOS; the charge-pump circuitry uses high-voltage CMOS.

The hallmark of the BTS-412A is its many protective features. In the event of a short circuit, the current switches off after approximately 40 μsec. In the event of an overload condition, the temperature sensor switches the device off when its junction temperature exceeds 150°C; in the case of an undervoltage condition, the device shuts off immediately. An additional protective function is the action of a 10V zener diode at the output, which aids in de-energizing inductive loads at switch-off. The device includes a status pin that provides fault information to logic- or microprocessor-based systems. Unlike ICs made by some other processing technologies, Smart SipMOS does not use

A natural application for smart-power ICs, *this 35-mm autofocus camera from Canon uses two Motorola MPC1710A motor-control circuits—one to rewind the shutter spring, and one to advance and rewind the film. All circuits in the camera are under the control of Motorola's MC68HC11 microprocessor.*

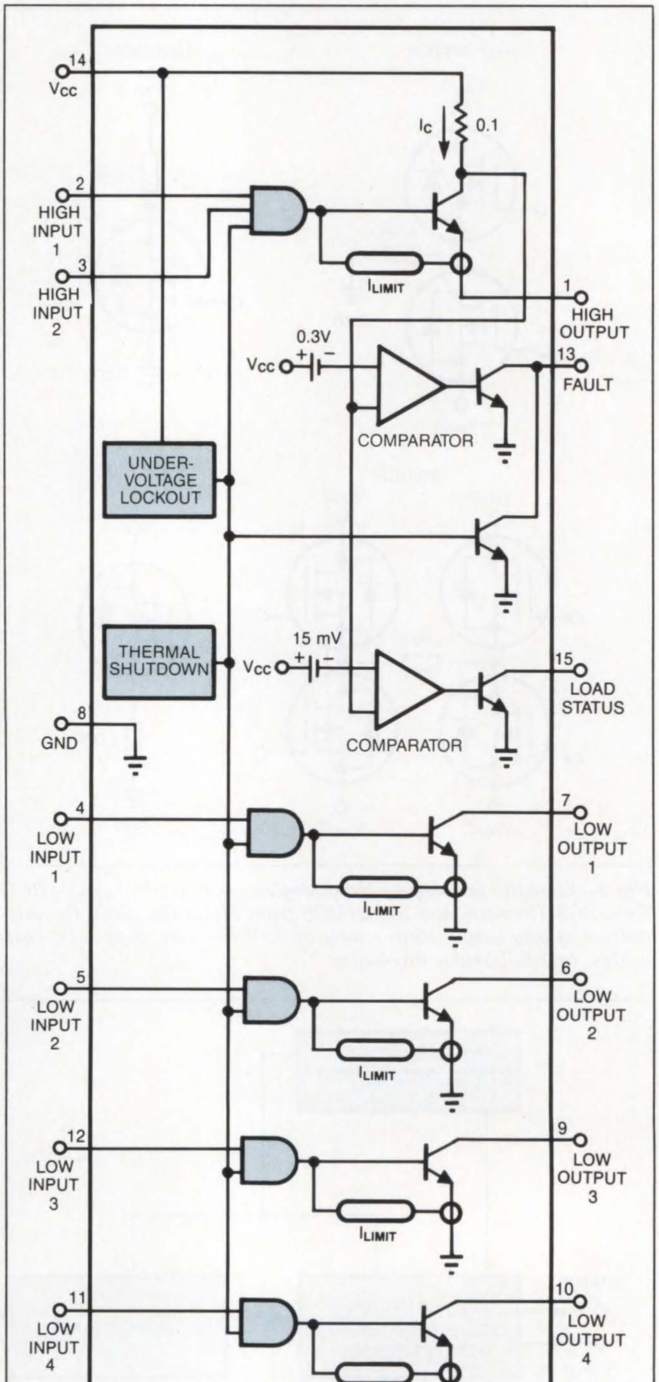
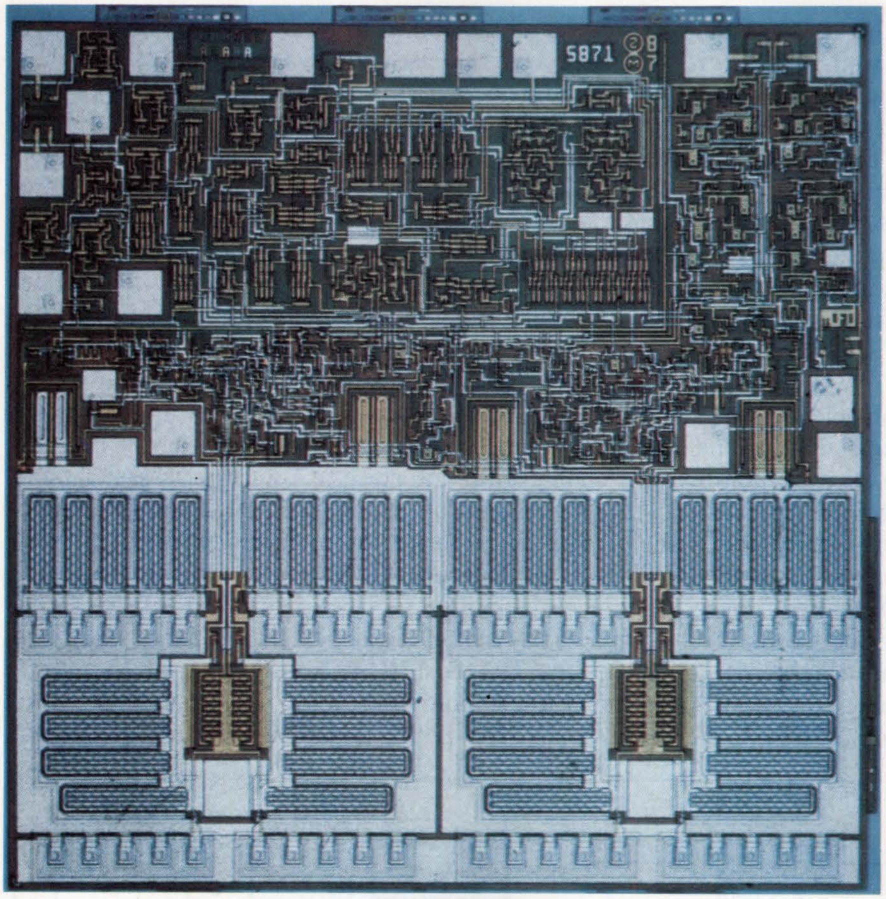


Fig 4—This multipurpose smart switch *from Unitrode features a fully protected, 4.5A high-side switch, and four independent, 1A low-side switches. The UC3720 switch IC provides protection against short circuits and has thermal-shutdown and undervoltage lockout functions.*



***This intelligent translator/driver chip** from Sprague Semiconductor uses the company's BiMOS II process. The top half of the UC5871 contains the chip's CMOS logic, control, and protective circuitry. The bottom half contains the bipolar power circuitry, including a dual full-bridge output stage.*

complex junction isolation—only the simple epitaxial base material of a normal SipMOS transistor. The BTS-412A costs $6.25 (1000).

Very similar to the BTS-412A is the MPC1510 Smart-MOS high-side switch from Motorola. Like the Siemens device, the MPC1510 has a current rating of 12A and comes in a 5-lead, TO-220-style package. Although the MPC1510 is designed to operate at voltages lower than 18V, it can withstand 40V for a maximum of 250 msec, as occurs with a clamped load-dump in automotive ignition systems. The MPC1510's protection features include short-circuit current limiting, thermal shutdown, inductive-load clamping, and a diagnostic status pin. The input of the device accepts commands from CMOS or TTL logic or directly from the output of a microprocessor. The MPC1510 costs $5.48 (100).

A third example of high-side drivers is National's LM1951, which also comes in a 5-lead, TO-220 package. Fabricated in a deep-base-pnp bipolar process, the LM1951 operates over a range of 4.5 to 26V and has a current rating of 1A. Like the 12A-rated BTS-412A and MPC1510, the LM1951 has an impressive array of protection features. These features include short-circuit protection, overvoltage shutdown, thermal shutdown, reverse-voltage protection, and a negative-output-voltage clamp. Suitable for high-speed switching to 50 kHz, the LM1951 has a TTL/CMOS-compatible input and an error-flag pin. The device also features a very low quiescent current of 10 μA. A lower-cost version, the LM1921, has a higher quiescent current of 1.5 mA and does not have a diagnostic flag. The LM1951 costs $1.95; the LM1921 is $1.25 (1000).

A multipurpose smart switch is available from Unitrode Integrated Circuits. The UC3720 **(Fig 4)** contains a fully protected 4.5A high-side switch and four independent 1A low-side switches. The bipolar IC, which operates in the range of 8 to 40V, is encapsulated in a 15-lead Multiwatt package and has a power-dissipation capability of 25W at a case temperature of 75°C. The UC3720 has an over- and undercurrent fault-indication pin and a load-status pin. Its protection features include undervoltage lockout, instantaneous current limit, hiccup-mode current limit, and thermal shutdown. The UC3720 costs $6.20 (100).

The future cost effectiveness of smart-power ICs will depend greatly on processing technology and packaging innovations.

High-side power switches like the BTS-412A, MPC1510, and LM1951/LM1921 are well suited for driving inductive loads such as solenoids and small incandescent lamps that use a common ground. Automotive applications, in particular, offer a wide range of uses for these devices, which have the potential for functioning well in multiplexed systems. In addition to using high-side drivers, automotive applications also use various types of motor-control ICs for power-seat, power-window, and windshield-wiper functions.

Intelligent motor-control ICs

Another major market for motor-control circuits is computer peripherals. Disk drives, tape drives, and printers consume millions of 2-phase stepper-motor circuits and 3-phase brushless dc-motor circuits. Although many of these applications use custom ICs designed for special requirements, a number of standard products are also available **(Ref 1)**. Many of these standard products are capable of delivering a considerable amount of power, and some are quite smart.

One example of a motor-control circuit that fits the smart-power category is the L6217 from SGS-Thomson. The device is fabricated in an advanced, high-density bipolar process that uses integrated-injection logic (I^2L) for the digital portions of the chip. Although not promoted as a smart-power device, the L6217 contains a considerable amount of intelligence and can deliver several watts of power to its load. Operating from a motor-supply voltage from 8 to 16V, the L6217 **(Fig 5)** drives both phases of a bipolar stepper motor (400 mA max/phase). The IC provides pulse-width-modulation (PWM) control of the phase current. Dual 6-bit D/A converters program the output current of each phase for use in either full-step, half-step, or microstep applications. The latched inputs to the D/A converters and the phase inputs that select the direction of current flow minimize the interface to a microprocessor.

The power section of the L6217 is a dual H-bridge driver that has internal clamp diodes for current recirculation. To maintain the degree of accuracy required for microstepping, the circuit internally senses and compares the motor current to the outputs of the D/A converters. External RC networks program the internal monostable multivibrators to set the motor-current decay time. The L6217 is supplied in a 44-pin PLCC

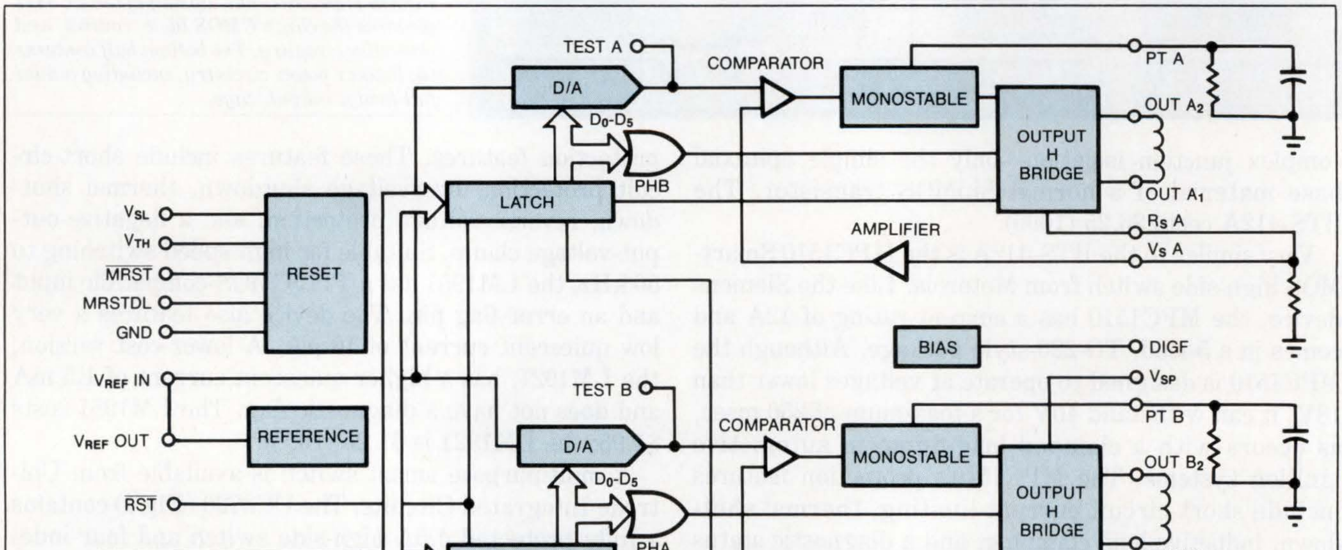


Fig 5—Fabricated in a high-density bipolar process, *the L6217 from SGS-Thomson drives both phases of a bipolar stepper motor to 400 mA/phase. Latched inputs and dual 6-bit D/A converters provide the intelligence for driving motors in full-step, half-step, and microstep applications.*

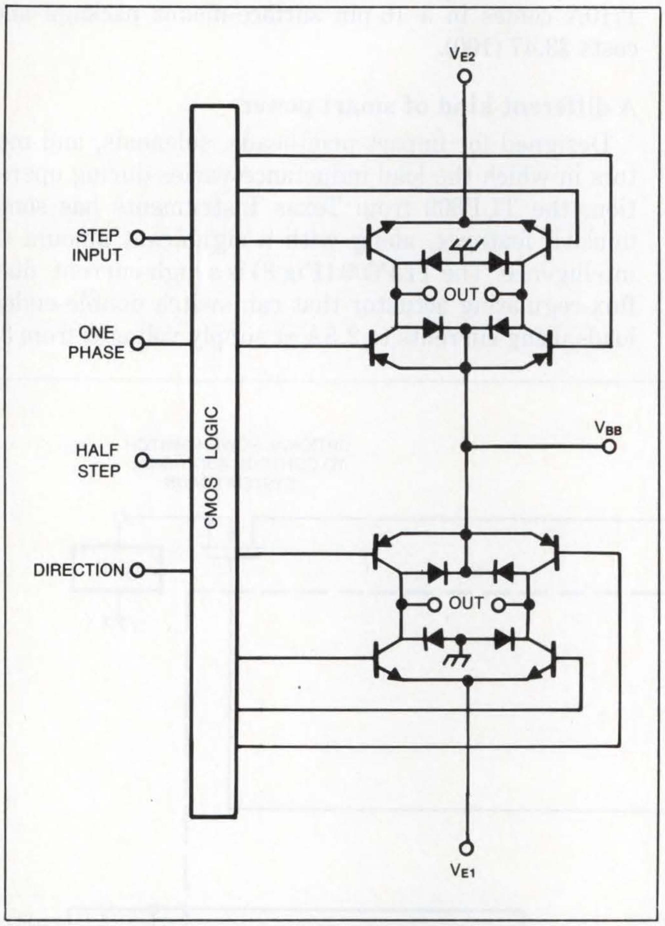
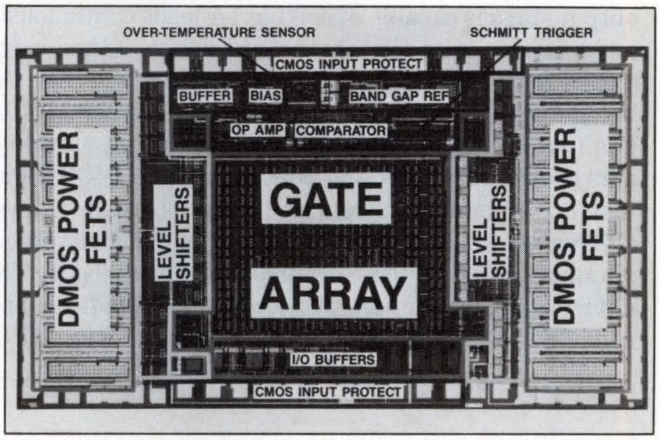


Fig 6—This driver/translator uses BiMOS technology. The UCN-5871 from Sprague exploits the company's BiMOS II processing to combine low-power CMOS logic with high-voltage bipolar output stages. The device has an output rating of 45V, 1A and has three stepper-motor drive formats; it also features protection against inductive transients and has a thermal-shutdown capability.



Fabricated in CMOS/DMOS, this MPD8020 semicustom smart-power array from Micrel contains a multitude of active and passive devices. Included are 16 100V, 200-mA vertical DMOS FETs, 16 115V CMOS level shifters, 200 CMOS gates, 12 TTL/CMOS-compatible I/O buffers, and a variety of configurable analog circuits.

that has 11 of the 44 pins reserved for heat sinking the device. The L6217 costs $4.77 (1000).

Another example of a smart motor-control circuit that interfaces microprocessors to bipolar stepper motors comes from Sprague Semiconductor. Using BiMOS II technology, the UCN5871 **(Fig 6)** combines low-power CMOS logic with two high-current, high-voltage bipolar output stages. The device provides PWM control for 2-phase bipolar stepper motors. The H-bridge output stages operate from a motor-supply voltage of 10 to 45V and have a continuous-current rating of 1A/phase. The UCN5871 translator/driver can control a maximum of 90W of power in a 2-phase circuit.

The CMOS logic section of the UCN5871 provides the sequencing logic, the direction control, the source-enable control, and a power-on reset function. Three stepper-motor drive formats (wave drive, two phase, and half step) are externally available. The logic inputs are compatible with CMOS, PMOS, and NMOS circuits. TTL or LSTTL may require the use of pullup resistors to ensure an input-logic high state.

The high-current bipolar bridges of the UCN5871 include both ground-clamp diodes and flyback diodes for protection against inductive transients. Thermal-protection circuitry disables the outputs if the chip temperature exceeds safe operating limits. Two versions of the device are available. The UCN5871B comes in a 22-pin plastic DIP that has a copper lead frame and heat-sinkable tabs. The UCN5871EB is supplied in a 44-lead PLCC for surface-mount applications. Device costs are $3.36 and $3.66 (1000), respectively.

Not all motor-control circuits go into automotive and computer-peripheral applications. The Canon EOS series of 35-mm autofocus cameras, for example, uses two Motorola MPC1710A motor-control ICs—one to rewind the shutter spring and the other to advance and rewind the film. Fabricated in a BiMOS version of Motorola's SmartMOS technology, the MPC1710A incorporates isolated CMOS, bipolar npn transistors, and a lateral DMOS output stage. Motorola chose this particular process for its efficiency at breakdown voltages below 25V, low on-resistance, simple processing, and overall cost effectiveness. In the Canon camera application, the MPC1710A works with Motorola's MC68HC11 8-bit microprocessor and the SFX10, a custom power FET.

The MPC1710A **(Fig 7)** is for use in low-voltage, battery-operated motors. The device operates from motor-supply voltages from 2 to 6V; its H-bridge

Although expected to decline in use, hybrid circuits will continue to play an important role in high-power applications.

output stage is capable of driving 1A loads continuously and 3A loads peak. The low on-resistance of the bridge varies from 0.21 to 0.41Ω, depending on whether the bridge is sinking or sourcing current. The MPC1710A has four control modes—forward, reverse, standby, and brake—all under the control of the CMOS logic, which commands the output stage through a level shifter. A separate pin is available for driving an optional power switch to control additional loads. The device includes an undervoltage lockout feature and consumes 1-mA max quiescent current. The MPC-1710A comes in a 16-pin surface-mount package and costs $3.47 (100).

A different kind of smart power

Designed for impact printheads, solenoids, and motors in which the load inductance varies during operation, the TLP609 from Texas Instruments has some unusual features, along with a significant amount of intelligence. The TLP609 (**Fig 8**) is a high-current, dual flux-regulating actuator that can switch double-ended loads using currents to 2.5A at supply voltages from 30

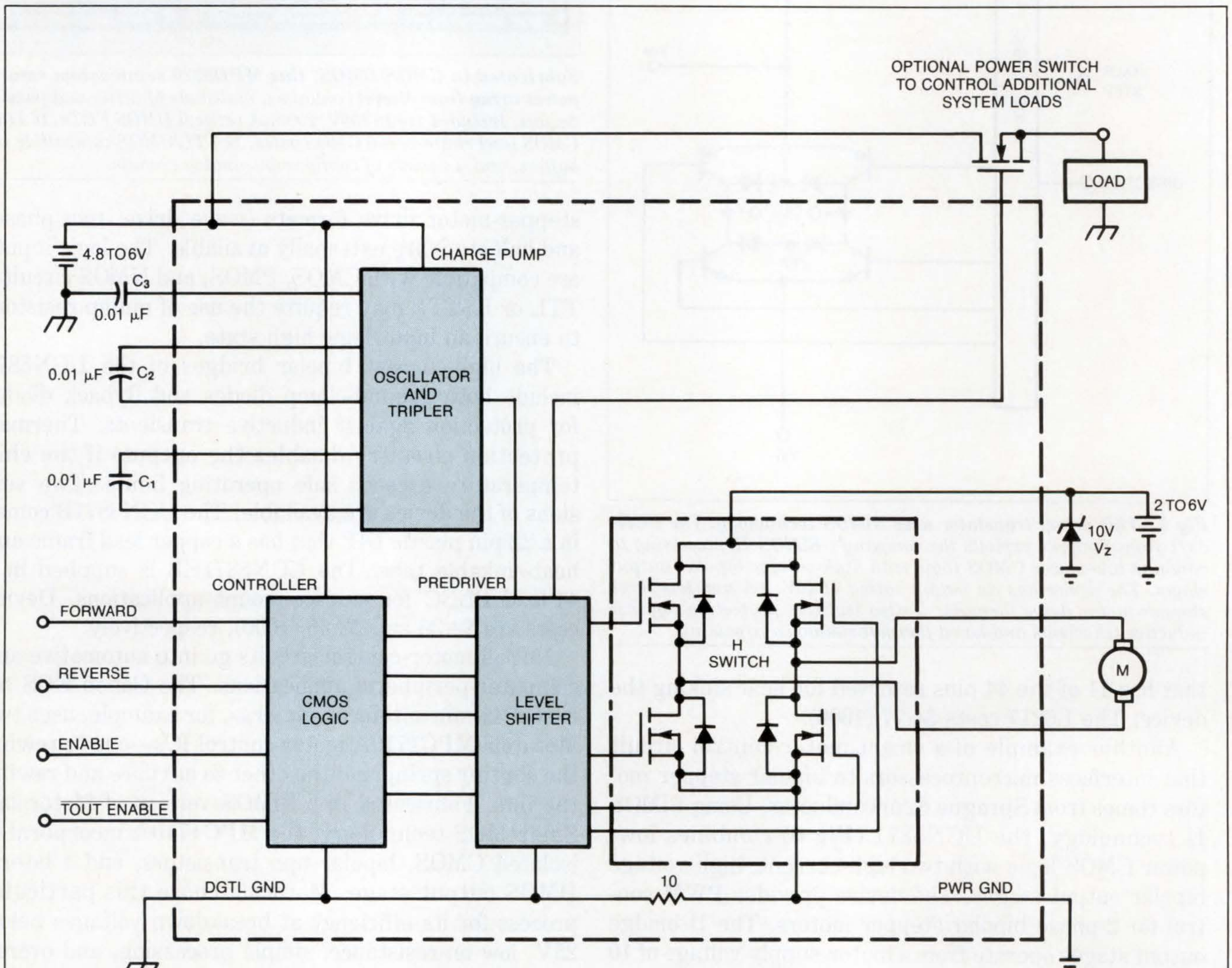


***Fig 7—Fabricated by a processing technology called SmartMOS,** the MPC1710A motor-control circuit from Motorola operates at a motor-supply voltage from 2 to 6V and can drive 1A loads continuously. The device, which is used in the Canon EOS 35-mm camera, combines isolated CMOS, bipolar npn transistors, and a lateral DMOS output stage.*

Smart-power ICs come in all forms—custom, semicustom, and standard products—including monolithic and hybrid versions.

to 60V. The device performs the function of flux regulation for two independent channels under the control of standard TTL or CMOS input signals. Flux is proportional to the integral of the inductive-load voltage, which is a function of the total amount of current in the load and its magnetic field. Under flux regulation, the load current will vary to compensate for core saturation, temperature changes, and other variations of load inductance during operation.

Each channel of the device has a separate sink and source output for driving each end of the inductive load. Internal feedback circuitry, consisting of an integrator and a voltage comparator, provides flux regulation via chop-mode operation of the source output. The integrator provides current to the capacitor terminal proportional to the differential voltage between the sink and source output of each channel. The voltage at the capacitor terminal, referred to ground, is proportional to the integral of the source-to-sink load voltage. The comparator hysteresis controls the charge and discharge voltage excursions at the capacitor terminal, thus controlling the on and off time of the source-output chopper.

The TLP609 also has a number of protective features, including thermal shutdown, short-circuit protection for the sink outputs, internal ESD protection, low-voltage sensing, and sink-output clamp diodes for inductive-transient suppression. You must use external, high-speed clamp diodes for the source outputs. The device comes in a single-in-line power package that has a metal tab for heat-sinking purposes. The TLP609 costs $5.49 (100).

Semicustom also plays a role

Although custom circuits dominate smart-power applications today, and standard products are expected to dominate in the future, a stable, smaller niche exists for semicustom devices. Many manufacturers whose pro-

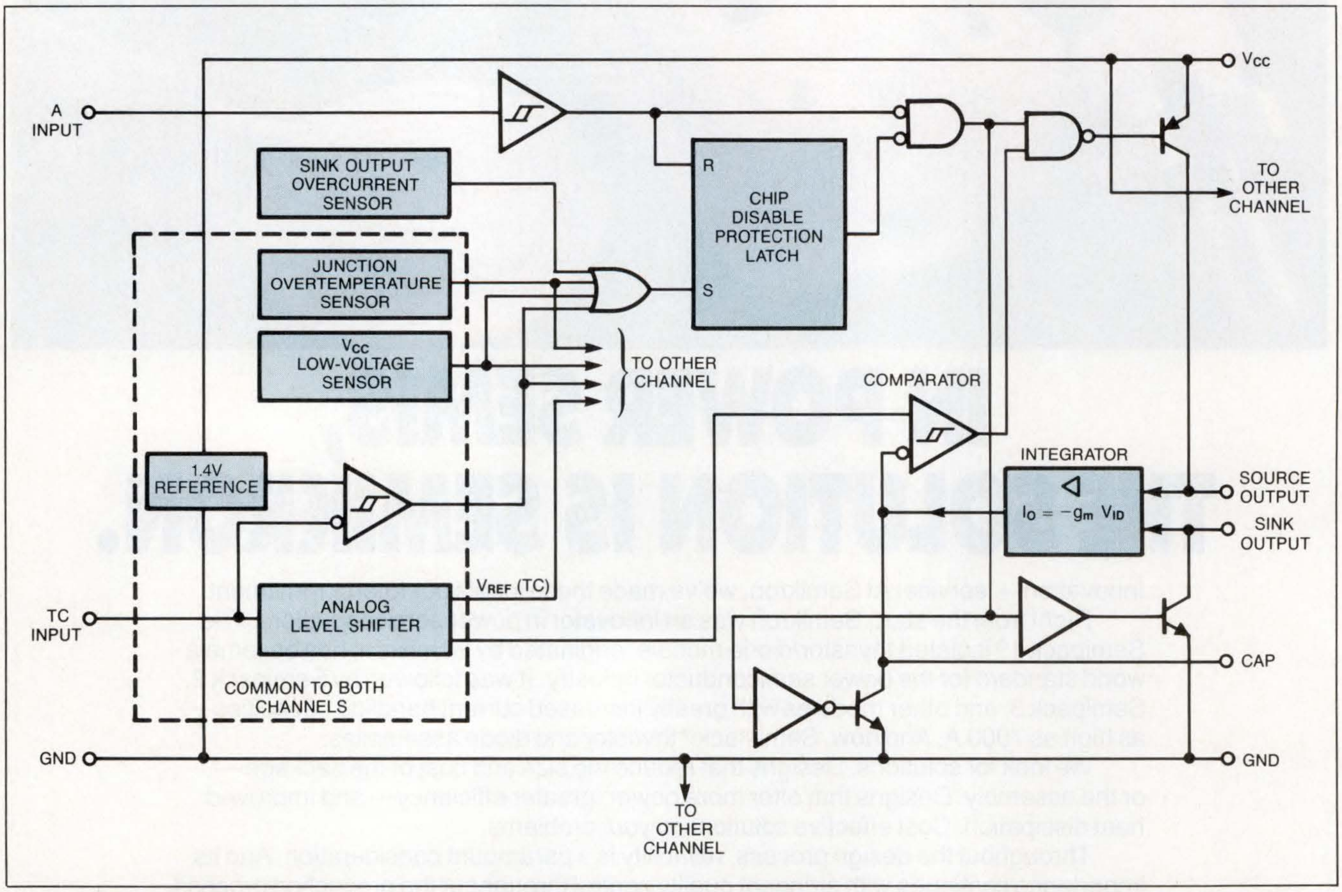


__Fig 8—A dual flux-regulating circuit,__ the TLP609 from Texas Instruments drives impact printheads, solenoids, and motors in which the load inductance varies during operation. Protective features in the device include thermal shutdown, short-circuit protection for the sink outputs, internal ESD protection, and low-voltage sensing.

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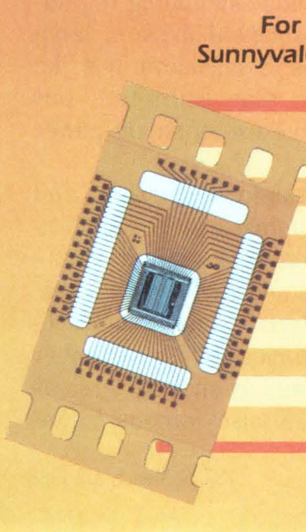

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Smart-power circuits are currently finding their greatest use in automotive and computer-peripheral applications.

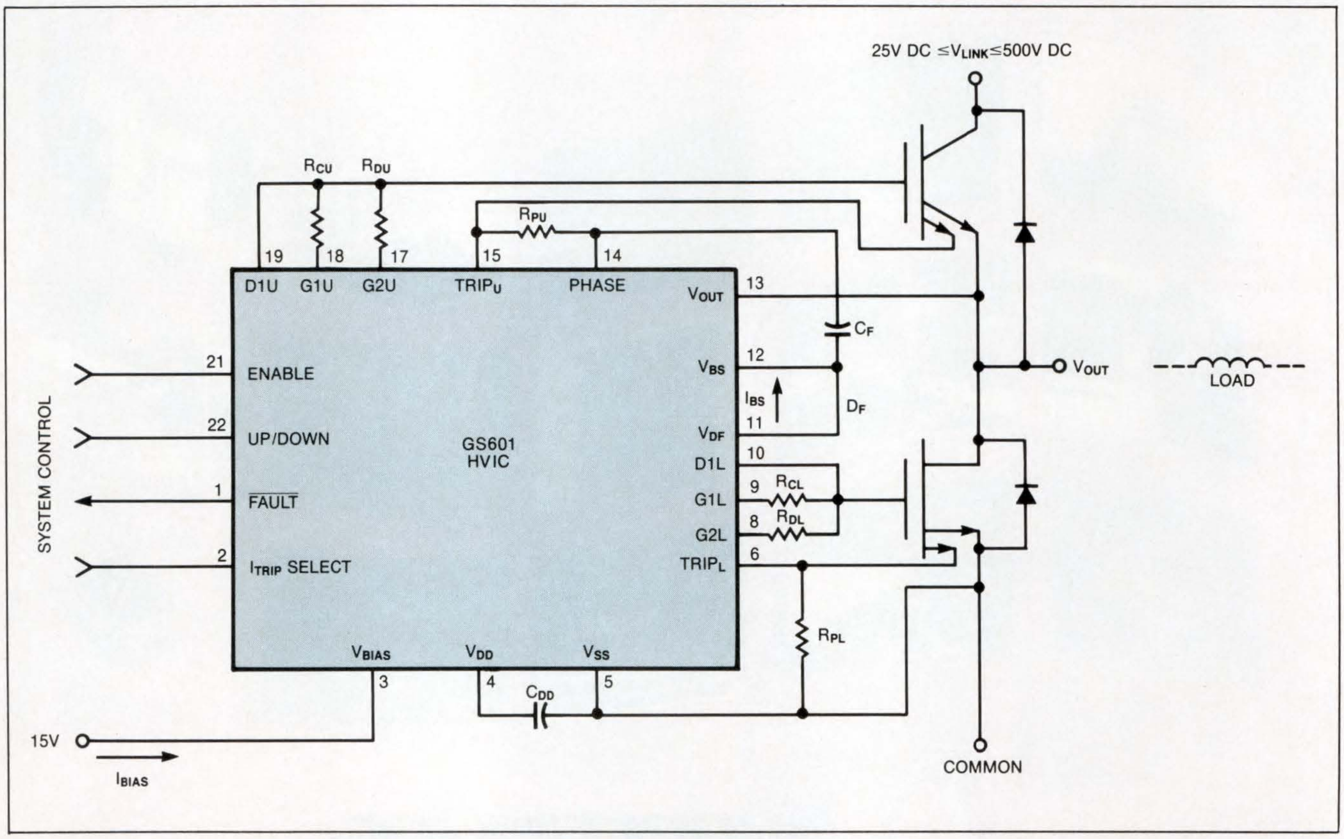

Fig 9—A monolithic power IC from a major supplier of smart-power hybrids, *General Electric's GS601 is a digitally controlled device for use as a PWM driver of high-voltage MOSFETs. The driver has a maximum rating of 500V at its high-voltage pins and can supply a peak current of 0.5A to the external power devices. The GS601 includes a number of protection features.*

duction volumes can't justify the cost of a custom-circuit development, and who can't find a standard product that suits their needs, are turning to semicustom circuits. One example of the direction that smart-power semicustom circuits are taking is the MPD8020 array from Micrel.

Fabricated in CMOS/DMOS, the MPD8020 smart-power array contains a wide range of active devices that may well satisfy the needs of many designers who have been looking for a solution to problems that demand smart-power ICs. The available devices in the MPD-8020 include 16 fully floating 100V, 200-mA vertical DMOS FETs, 16 CMOS level shifters rated at 115V, 200 uncommitted CMOS gates, 12 TTL/CMOS-compatible I/O buffers, a unity-gain analog-output buffer, three configurable op-amp/comparator/Schmitt-trigger cells, a bandgap reference, and an overtemperature sensor.

A single 5 to 15V supply powers the logic and analog circuitry. The high-voltage sections operate at voltages as high as 100V. The chip can derive the 15V analog/digital supply from one 24, 28, or 100V supply. For rail-to-rail switching in push-pull and H-bridge applications, you can also use an internal voltage pump to drive the high-side gates of the DMOS FETs at a level 15V higher than the 100V supply voltage. To assist the designer, Micrel makes separate kit parts available in 40-pin DIPs for analog ($20) and digital ($15) SSI/MSI functions. Applications for this semicustom smart-power circuit are numerous; they include switching regulators, motor control, relay and solenoid drivers, lamp drivers, and automotive switches. Semicustom ICs like the MPD8020 are expected to play a limited, but nonetheless important, role in the use of smart-power devices.

Although monolithic ICs (standard, custom, and semicustom) are expected to dominate future applications, hybrid ICs and modules dominate present ones—particularly where high-voltage and high-power capabilities are required. General Electric, one of the earliest suppliers of smart-power hybrids, offers a number of standard hybrid modules as well as custom versions for specialized requirements. GE also intends to an-

Automotive applications employ a common ground return, which requires the use of high-side drivers that operate between the positive supply and the load.

Manufacturers of smart-power ICs

For more information on smart-power ICs, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

GE Integrated Power Systems Dept
Box 13049
Research Triangle Park, NC 27709
(800) 243-7364;
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Micrel Inc
1235 Midas Way
Sunnyvale, CA 94086
(408) 245-2500
TWX 910-379-0007
Circle No 651

Motorola Inc
Technical Information Center
Box 52073
Phoenix, AZ 85074
(512) 928-6705
Circle No 652

National Semiconductor
2900 Semiconductor Dr
Santa Clara, CA 95052
(408) 721-5000
TWX 910-339-9240
Circle No 653

SGS-Thomson Microelectronics Inc
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nounce monolithic versions of smart-power circuits in the immediate future. One precursor to such products may be the GS601, a high-voltage, half-bridge driver.

The GS601 (**Fig 9**) is a digitally controlled power IC for use as a PWM driver of n-channel MOSFETs or IGBTs (insulated-gate bipolar transistors) in line-rectified, totem-pole applications to 240V ac. For those unfamiliar with the device, an IGBT (or sometimes IGT) has the minimal drive requirements of a MOS gate and the superior current-density capabilities of a bipolar transistor. The IGBT is also capable of blocking high voltages without the penalty of the high forward-voltage-drop characteristic (accruing from high on-resistance) of MOSFET devices.

The GS601 has a maximum rating of 500V dc for its high-voltage pins and can supply a peak drive current of 0.5A to the external power devices. The IC interfaces with both standard and current-sensing n-channel power-MOSFET/IGBT devices. In addition to latch-immune CMOS logic, the device includes overcurrent protection, a lockout feature to prevent simultaneous conduction of the output stage, and an undervoltage lockout function to ensure proper start-up. Apart from the output stage, the GS601 operates from a single, low-current 15V bias supply. The GS601 is packaged in a 22-pin DIP and costs $11.84 (100).

Although custom-monolithic and hybrid ICs account for the majority of present-day shipments of smart-power circuits, this situation is expected to change over the course of the next few years. In many instances, custom products will become standard products when the need for a particular device becomes common. In other cases, a common need already exists that will prompt the introduction of a standard product. As processing technology and packaging techniques continue to develop, IC vendors are expected to introduce an increasing number of smart-power ICs as standard products, primarily in monolithic form. Although all forms of smart-power circuits will continue to coexist, the direction is clear. **EDN**

Reference

1. Pryce, Dave, "Motor-control ICs extend performance levels of stepper and brushless dc motors," *EDN*, November 26, 1987, pg 61.

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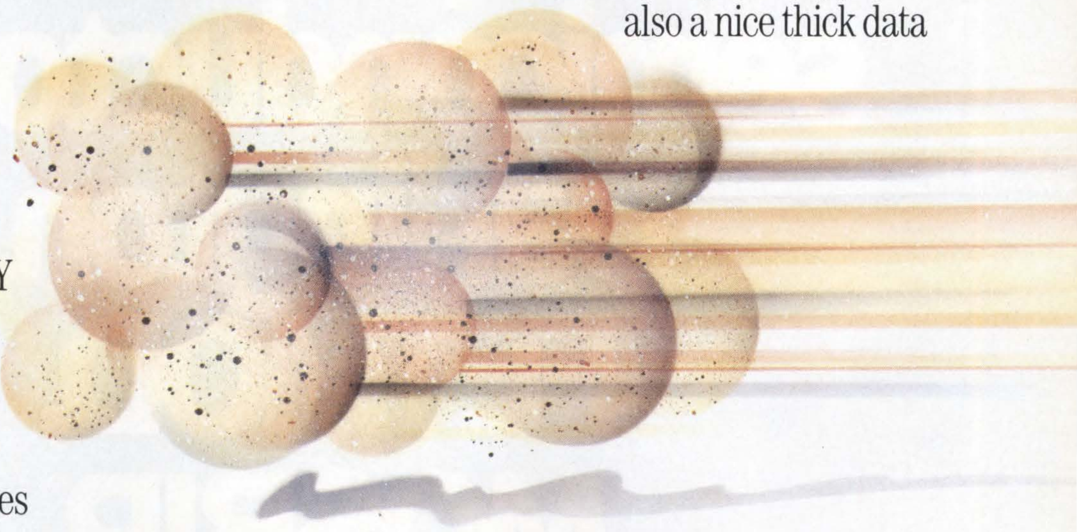

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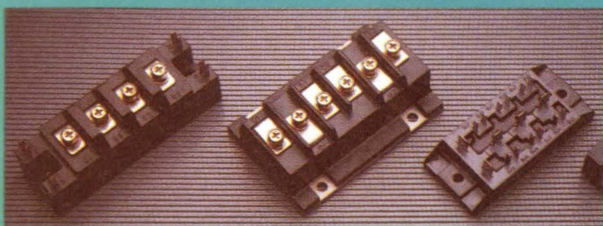

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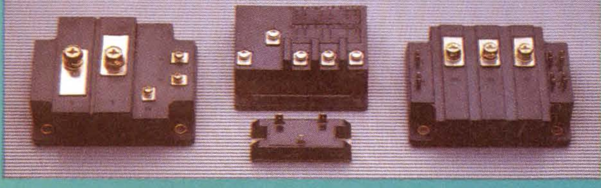

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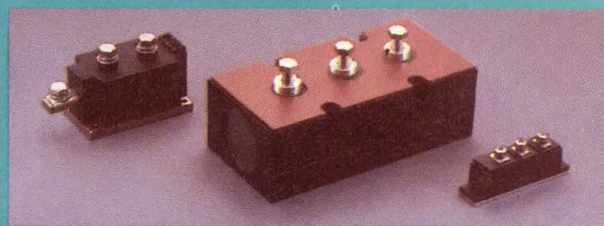

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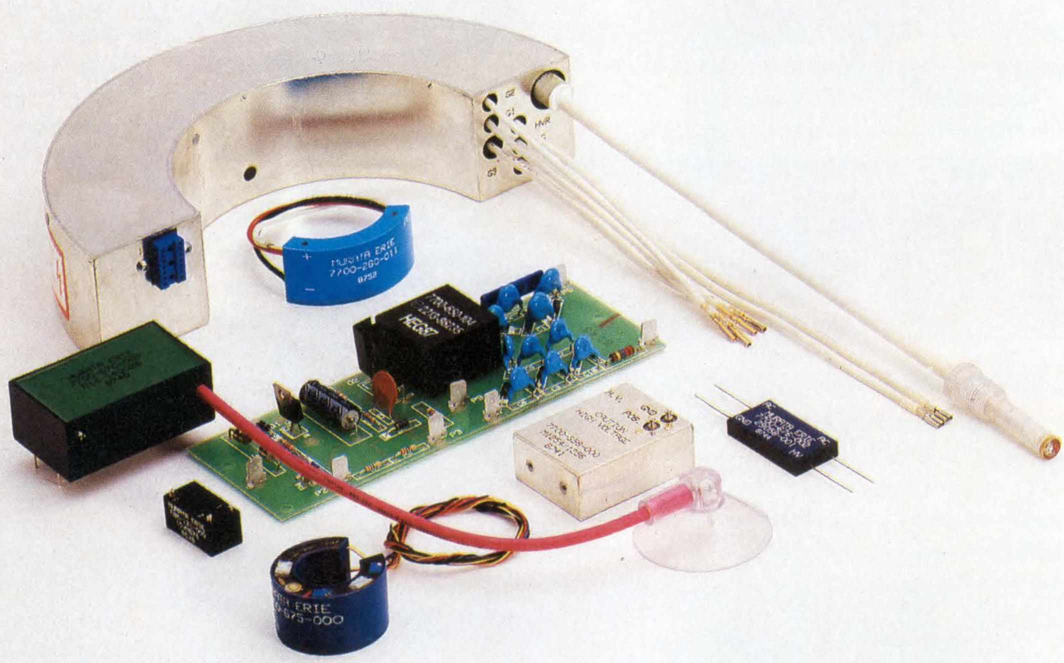

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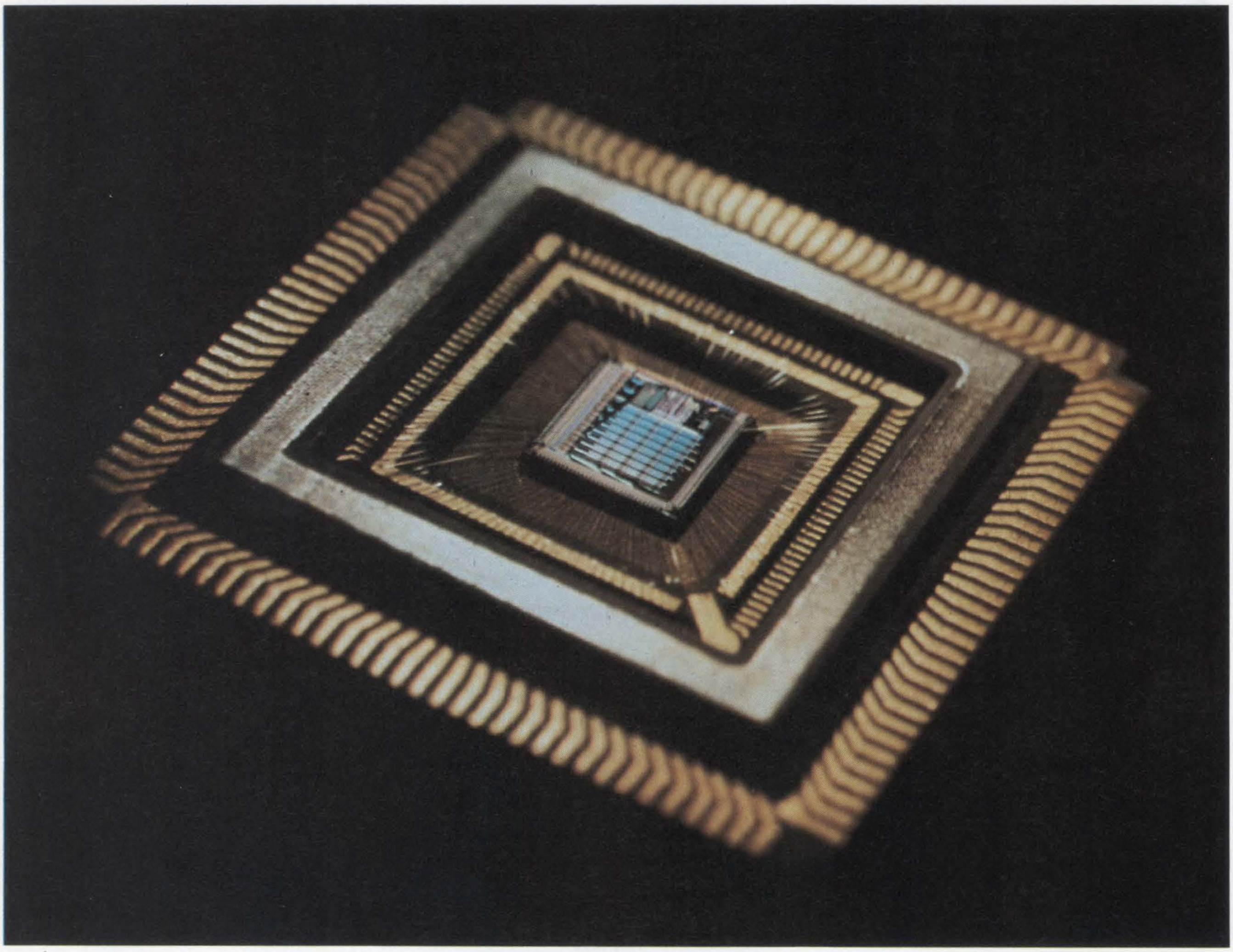

VHSIC devices, *such as this matrix switch from TRW Inc, are among the first ICs to incorporate standard testability circuits.*

PART THREE
DECADE '90
The future of system design

Design for testability creates better products at lower cost

Chips, boards, and systems of the 1990s will be far more sophisticated than those of today. Engineers who adopt a design-for-test (DFT) philosophy will create easily testable, more-reliable products that cost less to manufacture and operate. Without DFT methods, the cost of testers, fixtures, and test programs will soar.

Steven H Leibson, *Regional Editor*

Many design engineers' and managers' attitudes about product testability seem to have frozen during an earlier era in electronics, when a technician could troubleshoot almost any problem in 20 minutes with a scope and a little savvy. For products designed without a design-for-testability (DFT) philosophy, today's most advanced in-circuit ATE testers can do no more than automate the time-honored tradition of sticking a test probe into a failing test node to find the problem. But as electronic systems grow in complexity, this approach grows less and less effective and increasingly costly.

Today's electronic systems are already making test probing impractical because surface-mount technology, VLSI, and other advanced electronic-packaging schemes hide thousands of circuit nodes from the probe tip. The majority of systems built in the 1990s will certainly present even more difficulty in testing. As electronic-device technology and system design advance, therefore, the traditional attitude toward testing is becoming more and more unrealistic.

In the past, many design engineers ruled out design for testability because they thought it would cost too much, take up too much space, and delay their projects. Project managers pressed by schedule and cost constraints still encourage these attitudes because, for the most part, testing provides feedback about manufacturing quality—information that's important to the manufacturing department but not necessarily to the design lab.

Today, as they have in the past, many design engineers use every available transistor for speed, capacity, or other performance features, leaving no room for testability circuitry. The designs they create, therefore, are often difficult or impossible to test. In the 1990s, however, successful designs will allocate some circuitry for testability, which leads to better product quality and a shorter development cycle.

Testing provides quality feedback

Testing and DFT methodologies are initially useful to validate a design once it's actually built, but they serve best to provide valuable feedback on the manufacturing process once a product reaches production. "There's no sense in building a product that you can't test and can't build reliably," says Paul Gifford, manager of central systems engineering at Sequent Computers (Beaverton, OR). Sequent plans to incorporate scan design in its third-generation, multiprocessor computer systems to ensure that the products will be manufactured correctly. Gifford believes that the benefits of the DFT approach far outweigh the extra effort required to design testability into the computers. Further, he says, the performance penalty (if any) for adding DFT is only 5 to 6%.

Ignorance of DFT methods and the perception that testability is of secondary importance are the last major obstacles that a company must overcome before it can adopt a DFT orientation. When you consider a product's entire life cycle—including manufacturing, testing, and field service—you find that DFT methods actually save time and money in comparison with the traditional approach of "tossing it over the wall and letting the test engineer handle it."

Today's unknown testing costs

Sadly, many companies don't know what product testing really costs them. Ask a test manager what it costs to test a product and you'll often get a figure derived from the total number of products tested divided by the cost of the entire test operation. That figure gives you an average test cost for all the products run through the testing department, but it doesn't paint a very accurate picture of the true cost for any particular product. In addition, such an estimate of test-department costs generally doesn't include field-maintenance and repair costs.

Logical Solutions Technology Inc (a Campbell, CA, testability consulting firm) estimates that the average electronics manufacturer spends between 35 and 45% of a product's total cost on testing parts, subsystems, and final assemblies. The company says that its customers have saved, on the average, about $1.5 million per year by following its DFT recommendations. Note that these figures represent savings for systems built at today's complexities, not for the more complex systems that will be built in the 1990s. Test experts predict that test problems will be much worse for very complex systems unless design engineers add testable-design and DFT methods to their lexicon.

At the 1987 Government Microcircuit Applications Conference (held in Orlando, FL), Mitre Corp (Bedford, MA) reported on a study it performed for the Electronic Systems Div of the US Air Force to determine the impact built-in test (BIT) circuitry would have on equipment maintenance. The study indicated that BIT would improve both instantaneous and steady-state equipment availability, and that it would improve mission reliability by identifying weak modules before a critical failure occurred. From a field-service viewpoint, BIT reduces the occurrences of "cannot duplicate" (CND) and "retest OK" (RTOK) situations, because BIT circuitry pinpoints failing components.

Intermittent failures cease to be difficult to find and repair in systems that have BIT, because the BIT circuitry can store the identity of the faulty module. In addition, the incorporation of BIT circuitry reduces the mean time to repair (MTTR) by eliminating fruitless CND and RTOK maintenance actions; the BIT circuits immediately indicate the problem source, eliminating the troubleshooting phase of repair.

Mitre's report indicates that a BIT design with a 90% chance of isolating a problem incurs 10 to 30% extra design time during a product's development cycle. However, such incremental development costs add very little to the product's overall life-cycle costs **(Fig 1a)**. Considering the time and money required to develop and debug tests and test fixtures, as well as to perform field maintenance and repair, DFT methods ultimately save your company both time and money. According to the Mitre report, although the system-design phase of product development represents only about 15% of the product's total life-cycle cost, it has a 70% impact on that product's operation and support costs **(Fig 1b)**.

Testability also translates into product quality during production, because it lets you ship fewer products with undiscovered faults. In the field, products that are designed to be testable can be repaired more quickly, resulting in less down time for the customer. Though Mitre's report specifically applies to military systems, which have longer development and life cycles, the report's conclusions have equal validity for commercial product development, even if the numbers aren't exactly the same.

Three keys to testability

Because of the overwhelming evidence that DFT is simply part of a good overall design strategy, many companies are actively developing DFT methods. Though these methods differ, they all focus on the three keys to testability: partitioning (to break complex systems into testable blocks), control (to allow a test to stimulate testable blocks), and visibility (to extract the system's response to the test stimuli).

DFT methods take several approaches, which include divide-and-conquer, several types of serial scanning, and built-in self-test (BIST) or built-in test (BIT) (see **box,** "DFT methods focus on scan-path testing.") Each of these methods recognizes that you can no longer test increasingly complex systems simply by increasing the number of test probes on an ATE tester. Such an approach has grown prohibitively expensive as system complexities soar. Instead, the current DFT methods focus on adding test circuitry to the product. This extra circuitry allows less-complex test equipment to perform simpler tests with better fault coverage.

A divide-and-conquer test scheme works well in systems that can be divided into easily testable blocks or in blocks that have existing tests. For example, RAM and ROM blocks are relatively simple to test, yet they consume large portions of a system's transistor budget, so testing them is worthwhile. Today's test methods can verify the operation of these structures quite easily when they're isolated from the rest of a system.

In a paper presented at the 1987 Custom Integrated Circuits Conference, National Semiconductor (Sunnyvale, CA) discussed techniques for isolating blocks of circuitry embedded in an IC. If such a block is based on an existing standard part, such as the 82C50 asynchronous communications element in National's paper, you can use an existing test to verify that block's operation by employing data multiplexers to bring the block's input and output signals to the chip's leads.

National Semiconductor's paper also compares parallel and serial methods of accessing such isolated blocks. Parallel-access methods allow faster testing, but require more points of contact between the tester and the system. Serial-access methods are slower, but don't require as many test points. Because serial test methods require fewer test probes and less-expensive test equipment, engineers are adopting such techniques more and more frequently.

When engineers at NCR's Microelectronics Div (Fort Collins, CO) developed the PLM (Prolog machine) microprocessor in conjunction with the Computer Science Div of the University of California at Berkeley, they knew that the complexity of the chip would make testing difficult unless they included some on-chip test circuitry. Designed to act as a coprocessor in an engineering workstation, the PLM implements a tagged architecture and five hardware stacks to support the Prolog language environment. The resulting IC, representing a system with a complexity of about 45,000 gates, incorporates eleven 32-bit data buses, sixty-four

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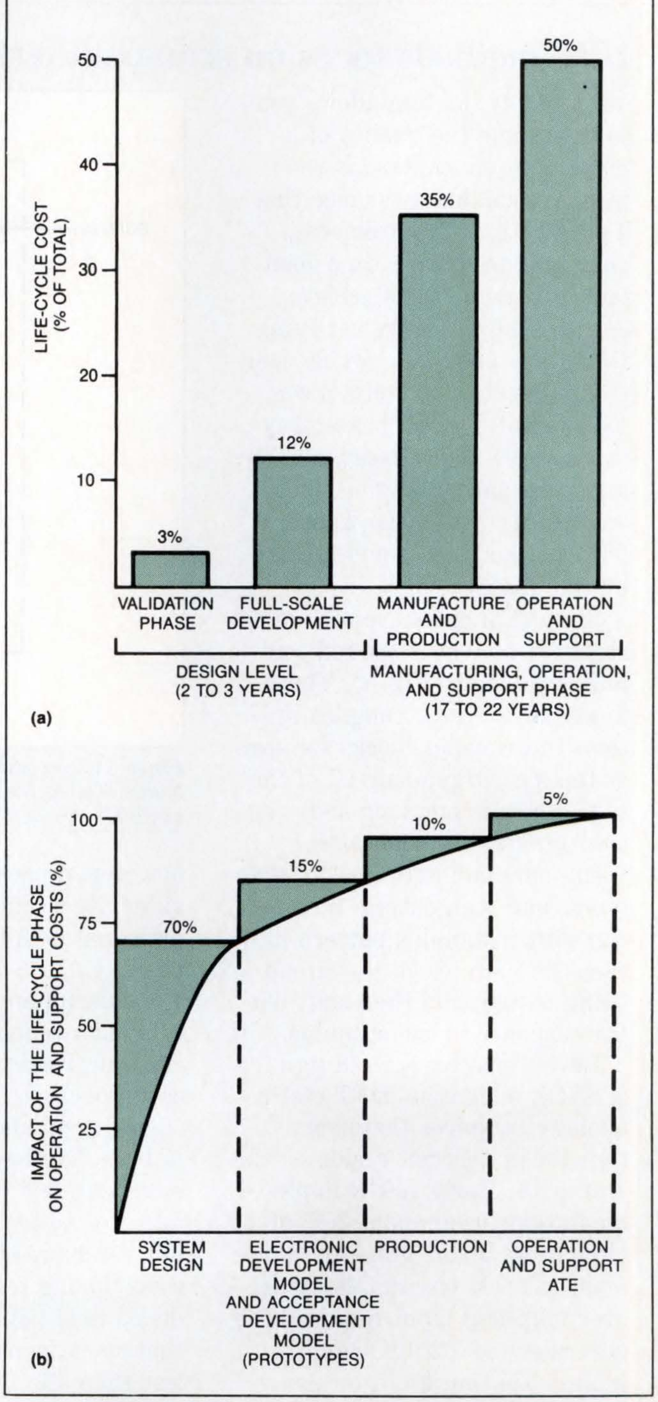

Fig 1—Although DFT methods add to the cost of a product's development phase, *the production, operation, and support phases represent the largest portion of the product's total life-cycle cost* ***(a).*** *And although the system-design phase of product development represents only about 15% of the total product-life-cycle cost, it has a 70% impact on that product's operation and support costs* ***(b).***

DFT methods focus on scan-path testing

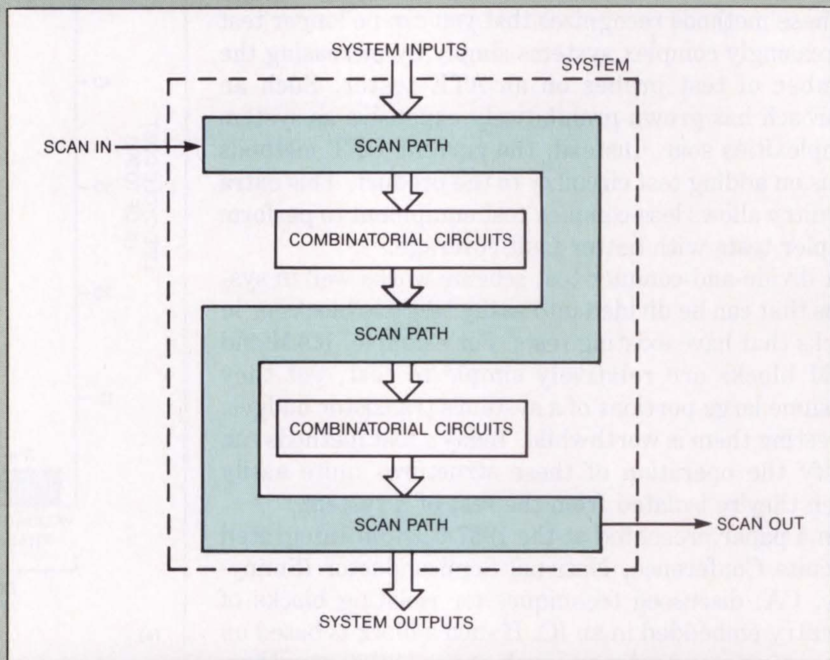

***Fig A—A scan path divides the combinatorial portions of a system** into easily testable blocks. The blocks are surrounded by a scan path composed of all of the sequential circuits in the system, which are connected to form one or more long shift registers.*

Very simply, testing allows you to determine the quality of a manufactured system. If you want reasonable assurance that a product is without defects, your test must have very good fault coverage. Tests achieve complete coverage by verifying that every node in a circuit operates properly. For today's complex circuits, which have many inaccessible nodes because of integration and packaging, most engineers turn to scan-based DFT methods to provide the required observability.

Scan techniques use a circuit's registers as fences around combinatorial logic **(Fig A)**. These fences divide even complex systems into smaller blocks for easier testing. Organizing all of the registers into one long shift register creates the scan path. Using only two data lines, a scan input, and scan output, a tester can shift a stimulus pattern into the scan path, clock the circuit being tested, and then shift out the response to the stimulus.

Level-sensitive scan design (LSSD), a rigorous DFT methodology, requires that every register in a circuit reside on the scan path. Early LSSD implementations used about 25% of a circuit's available gates to implement the test circuits, because every flip-flop input required the equivalent of a 2-input multiplexer. That multiplexer also added an extra delay to the circuitry, slowing the system's maximum speed.

Recent test-circuit designs, however, do not inflict such penalties. According to Fred Bulow, president of Aida Corp (Santa Clara, CA), "Scan-path testing is a wonderful approach if you have to build a reliable product and are concerned with development costs, because test-development costs are nil and fault coverage is 100%." Bulow claims that scan-path test circuits add about 5 to 15% to the cost of a raw IC, but you more than recover those costs during testing and from reduced field failures. He adds that speed penalties amount to less than 5%.

As a concrete example of scan-path costs, consider the gate arrays from Integrated Logic Systems Inc's (ILSI, Colorado Springs, CO). The firm adds scan-path logic to its gate arrays by incorporating five extra transistors in each of the arrays' sequential cells. This test circuitry consumes a mere 0.4% of the total silicon die area and uses about 4.5% of the total interconnection on the circuit to link the sequential cells into a scan path. The scan path has a negligible effect on the gate array's maximum clock speed.

Though the costs of ILSI's test logic are low, the scheme provides tremendous benefits. For a 1438-gate design, ILSI's automatic test generator (ATG) created a set of test vectors in 13 minutes that provides 99.3% fault coverage. To produce a test

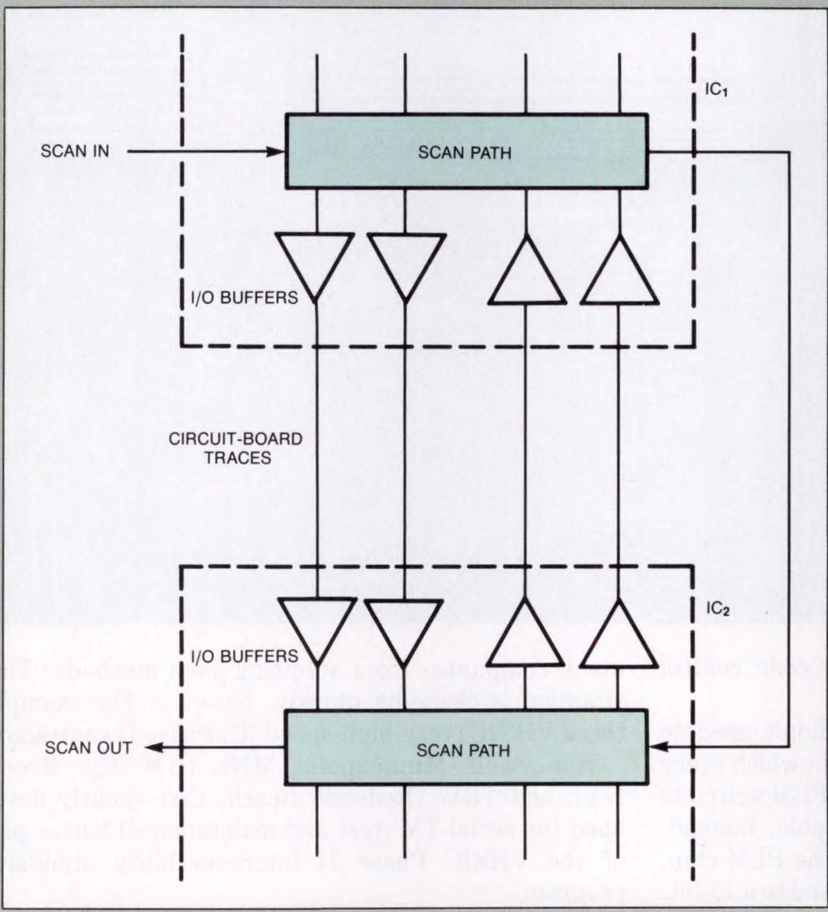

***Fig B—The boundary-scan method lets you test all of the I/O buffers** and associated circuit-board traces by using serial test techniques.*

for the same design without testability circuits, a fault-grading program required almost 14 hours and provided only 85% fault coverage. Further, for a 2456-gate design, the ATG required 14 minutes to create a test with 99.88% fault coverage; for the same circuit without scan-path logic, the fault-grading program required a little more than 57 hours to create a test that yielded 59% fault coverage.

You can also use a form of scan-path testing called "boundary scan" to check interconnections between ICs. If each IC has a scannable register attached to its input and output buffers, the registers create a scan path surrounding the buffers and the pc-board traces (**Fig B**). An ATG can create a test with 100% fault coverage for this simple topology in a very short time. In addition, if the boundary scan registers are part of the IC's level-sensitive scan path, you can use those boundary-scan registers to test the IC's internal circuitry as well. JTAG's latest testability-bus proposal encompasses both boundary-scan and IC-testing capabilities.

Even if you merely add a scan path to your design, you'll still need a tester to check the circuitry. By adding a little more logic to the scan path, you can build the entire tester into your system. Such built-in self-test (BIST) and built-in test (BIT) circuits allow a system to verify its own operation on an ongoing basis.

Engineers designing BIST circuits usually employ a linear-feedback shift-register configuration (a procedure that's also called "signature analysis") and a pseudorandom test-pattern generator. These items both reduce the number of stimulus and response vectors stored in the self-test circuitry, and decrease the amount of time required for the test. Thus, to add BIST capability to a circuit that has scan logic, you require only the test-pattern generator and the signature-analysis feedback registers.

BIST also allows you to test an IC at full speed, a situation that is becoming less and less feasible on testers as clock speeds climb beyond 100 MHz. Because BIST circuits use the same types of transistors that the chip's other circuits use, the tests can easily run at the maximum possible clock rate.

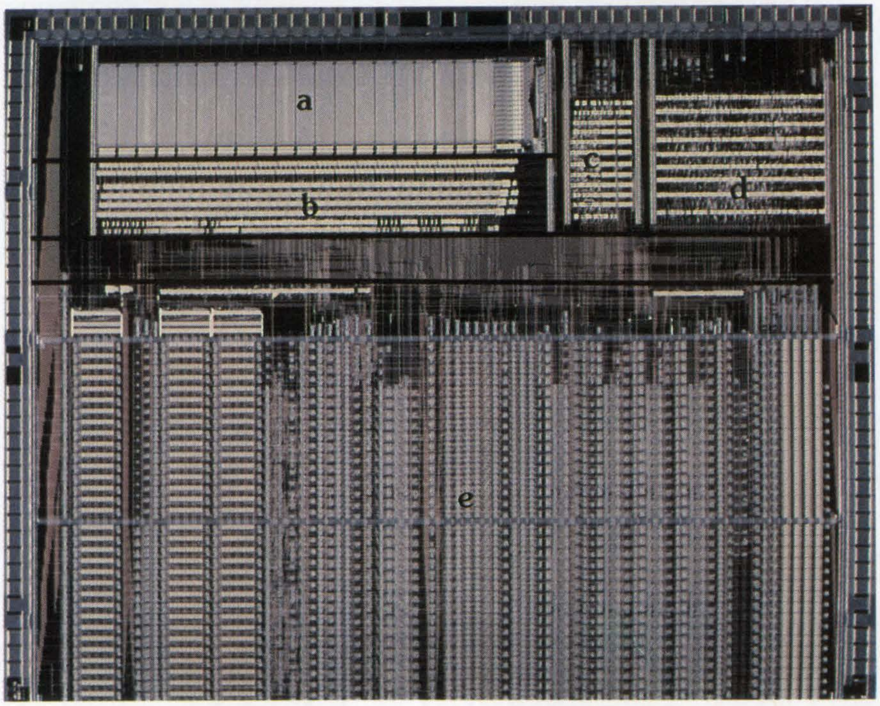

*Fig 2—The PLM (Prolog Machine) μP developed jointly by NCR and the University of California at Berkeley incorporates two serial scan paths and extra microcode to aid in testing the chip. Engineers can completely test the microcode ROM **(a)** with the first scan path **(b)**. The second scan path **(c)** reads a 16-bit status register that provides a gross indication of the operability of the chip's data path **(e)**. Microcode test instructions perform a more detailed check of the data-path's integrity and of the operation of the microsequence controller **(d)**.*

32-bit registers, and an 80,000-bit microcode control store **(Fig 2)**.

NCR's engineers decided that they didn't need to create a fully scannable design (a design in which every flip-flop is in the scan chain), because the PLM's circuits are already very observable and controllable. Instead, they designed two serial scan paths for the PLM chip, providing test access to the control store and to a 16-bit, data-path status register. Using these scan paths, test engineers can completely check the integrity of the microcode ROM and obtain a gross indication of the data path's operability. The scan paths add less than 5% to the chip's total area, but they allow a tester to check 70 to 80% of the μP's circuitry.

In addition, NCR's engineers incorporated extra microinstructions in the PLM's control store to facilitate detailed testing of the chip's data path. The company uses these microinstructions to check the IC's operation during manufacture. Self-test programs running on the PLM in a system can use them as well to monitor the chip's function while the system is operating.

So far, test standards have been lacking

Although companies such as NCR are already employing serial test methods to build complex systems, the lack of serial test-bus standards has prevented many companies from adopting such methods. That situation is changing quickly, however. For example, three VHSIC (very-high-speed IC) Phase II contractors —Honeywell (Minneapolis, MN), IBM (Rye Brook, NY), and TRW (Redondo Beach, CA)—jointly developed the serial TM (test and maintenance) bus as part of the VHSIC Phase II interoperability standards program.

The TM bus consists of four unidirectional lines, including a 6.25-MHz clock, a control line, and two data lines. A master test and maintenance controller uses the synchronous, backplane-level TM bus to check the status of as many as 32 modules in a system, sending data and control bits out on one unidirectional data line and receiving module status back on the second data line. In addition, Honeywell and IBM created an ETM (element test and maintenance) bus to allow an embedded test and maintenance processor to monitor as many as 32 individual devices within a module.

Other serial test standards are starting to appear as well. In 1985, Philips (Eindhoven, the Netherlands) started a test-bus study group that eventually became known as JTAG (the joint test action group), an ad hoc committee with representatives from European and US companies. JTAG hopes to create one serial test standard that IC vendors, board manufacturers, and systems

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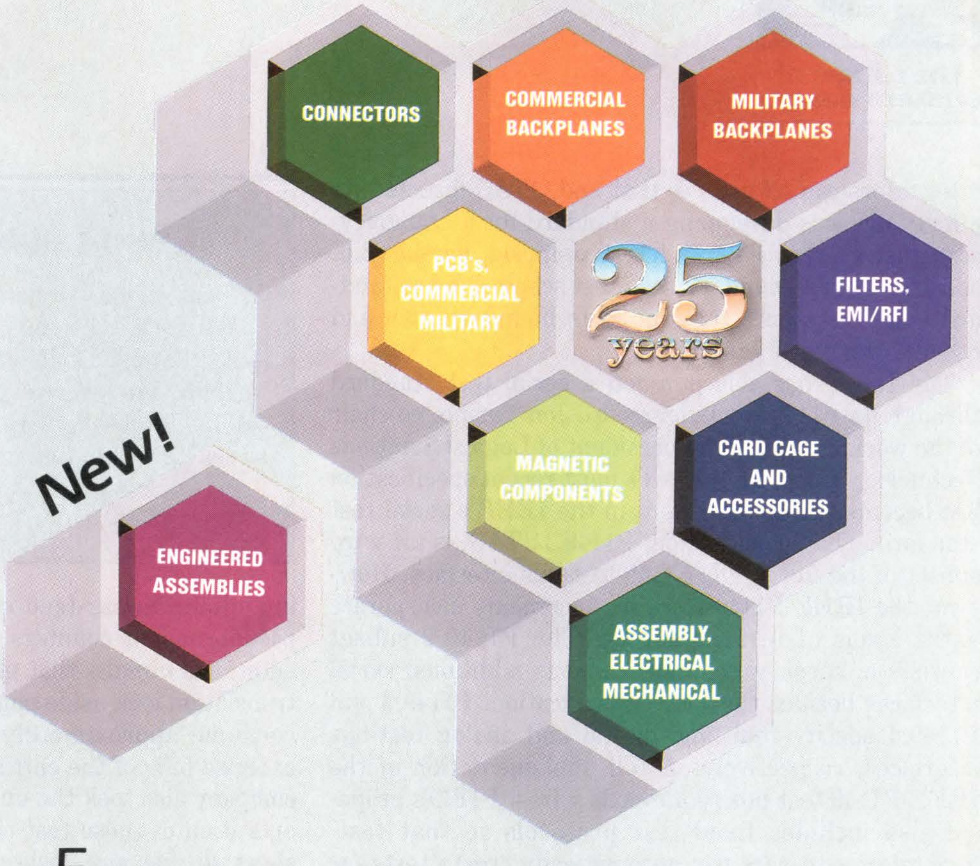

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integrators can all use. To that end, JTAG directed its efforts towards developing a standard for a boundary-scan test system. JTAG's latest proposal, version 2.0, specifies both a boundary-scan test scheme and a standard test-access port that supports boundary-scan and other serial test methods.

The IEEE has also pursued a serial test standard through its P1149 working group. Jon Turino, co-chair of the working group and president of Logical Solutions Technology Corp, says JTAG's most recent specification has become the first element in the IEEE's serial test standard. That specification, P1149.1/JTAG, is a 4-wire subset of the full IEEE P1149 test-bus interface. However, the IEEE P1149 working documents incorporate extra levels of test capability. The P1149.2 subset consists of seven wires and supports additional serial interfaces besides the JTAG specification. P1149.3 and P1149.4 specify real-time digital and analog test-bus interfaces, respectively. A full implementation of the IEEE P1149 test bus requires 25 wires. P1149's proposal also includes fixed test protocols so that test-generation software can automatically create tests for boards and systems that incorporate scan circuitry.

Standard ICs lack test ports

Standards such as the JTAG and IEEE proposals promise to make DFT methods far more popular with engineers who develop systems based on ASICs, because engineers can include testability circuits in an ASIC definition without having to invent a DFT scheme. However, designers who design systems with standard ICs still face a major obstacle: Chip vendors have not taken a leadership position in offering testable parts.

One reason for this omission, of course, has been the lack of a standard test bus. But another reason, say IC vendors, is that customers have not requested testability features. Without market demand, the chip makers had little reason to add testability features to standard ICs. As standard semiconductor products grow in complexity, however, the same pressures that encourage engineers to use DFT methods for ASICs are forcing the IC vendors to add a variety of testability circuits to their standard parts. Such test circuits make the job of testing the individual ICs much faster and easier. System designers can then employ these on-chip test circuits for board- and system-level tests as well.

For example, Intel (Santa Clara, CA) added substantial testability circuitry to its 80386 µP. The circuitry included linear-feedback shift registers and pseudorandom counters for built-in self-testing, plus additional circuits that give the µP direct access to its translation look-aside paging buffer. These test circuits consume approximately 2% of the total silicon, but exercise 52% of the chip's 285,000 transistor sites. The company also took the unusual step of documenting the operation of those test circuits in the processor's data sheet so that any designer developing an 80386-based system could make use of the test circuits with a power-up, self-test software routine. Intel claims that several companies designing 80386-based systems are taking advantage of the µP's on-chip testability features.

Standard-test-bus information

If you would like more information about the JTAG testability bus, contact Rod Tulloss, the chair for JTAG's North-American working group: You can reach him at AT&T, (609) 639-6116. To obtain more information about the IEEE's P1149 testability-bus efforts, contact Jon Turino at Logical Systems Technology Inc, (408) 374-3650.

Convincing management is tough

Pat Gelsinger, the Intel engineer who spearheaded the drive to add testability circuits to the 80386, says he had a hard time convincing the Intel's management to allocate silicon for those circuits. However, the DFT methodology made a great contribution to the 80386 project: It let Intel both obtain a fully functional device quickly and test production parts quickly. These facts produced a fundamental change in the company's attitude towards DFT methods. You can expect to see more testability circuits in future Intel products, says Gelsinger.

Another chip vendor, Texas Instruments (Dallas, TX), incorporated a complete serial scan path in its TMS320C30 DSP processor. A 4-wire serial test port emerges from the chip's package on four dedicated test pins. The DSP processor contains about 700,000 transistors. It will be available in the third quarter and will be one of the company's first ICs to incorporate testability circuits. Test circuitry uses about 10% of the chip. Although Texas Instruments perceived only a small

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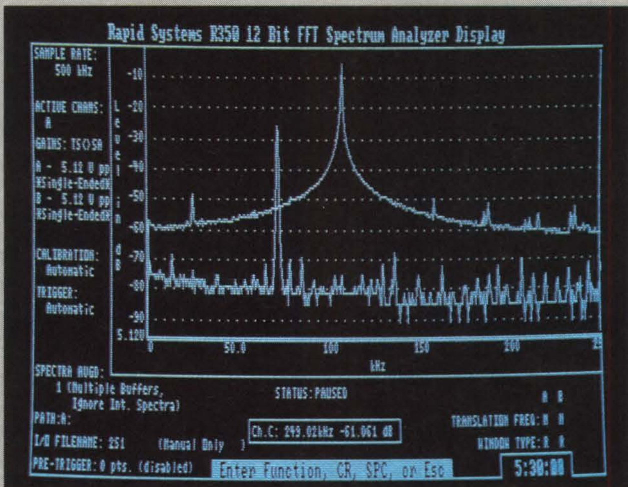
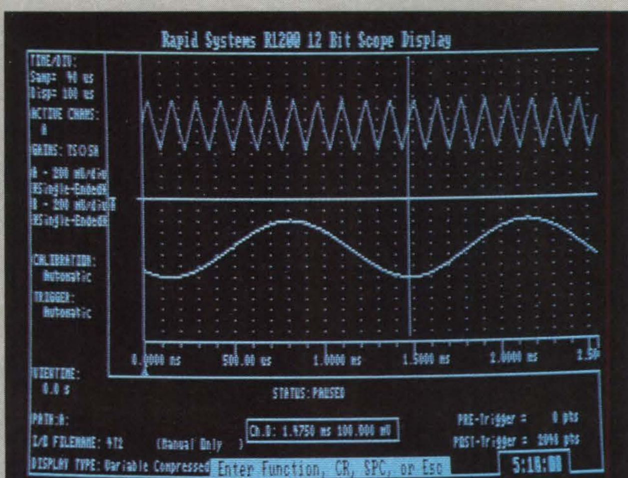


The R350 is a PC-based 12-bit, 2-channel, 500 KHz, real-time, FFT spectrum analyzer. Sample 2 channels simultaneously. 32K data buffers. Autosave spectrums to hard or floppy disk. Two modes of spectrum averaging. Fully differential inputs. Linear or log amplitude scaling. Amplitude and frequency cursor. Display spectrums 5 to 10 times a second. Print, store, retrieve and overlay spectrums. 500 KHz anti-aliasing filters on each channel, 80db of dynamic range.



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amount of customer interest in testability, the company decided that increasingly complex designs such as the TMS320C30 required a DFT approach—just to help the company test the device during production. Now the company simply considers DFT methodology a part of good overall design practice.

Scan-path design will help the company's engineers fabricate the DSP processor and develop future versions of the part. "The TMS320C30 has a very modular architecture, and we can test each module independently to isolate fabrication problems," says Ray Simar, chief architect and program manager for the processor. In addition, when Texas Instruments broadens the TMS320C30 family, it will do so simply by adding new modules to the existing architecture. "That module will not be considered complete until it has the 4-wire test interface and test vectors," Simar says. The scan path provides an added benefit: It makes software development much easier by allowing an in-circuit emulator to read the μP's complete internal state through the scan path.

Companies attempting complex designs—such as Sequent, Intel, and Texas Instruments—already embrace DFT methods, because these methods allow them to build better-quality products at lower cost. More companies will follow their lead in the 1990s. Considering the benefits that DFT affords, and the fact that standards for DFT are imminent, the way is clear for you to adopt DFT methodologies now. **EDN**

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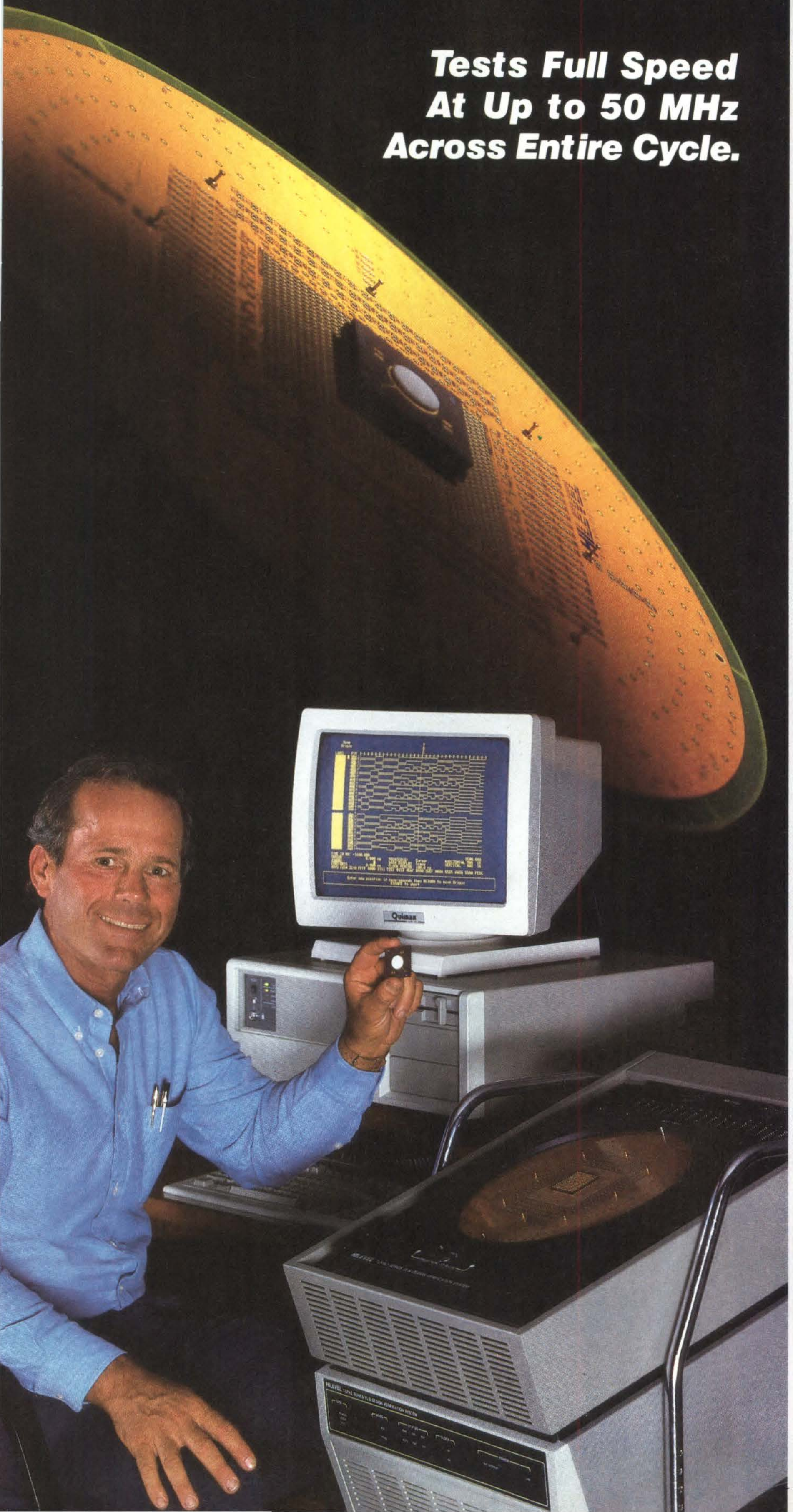

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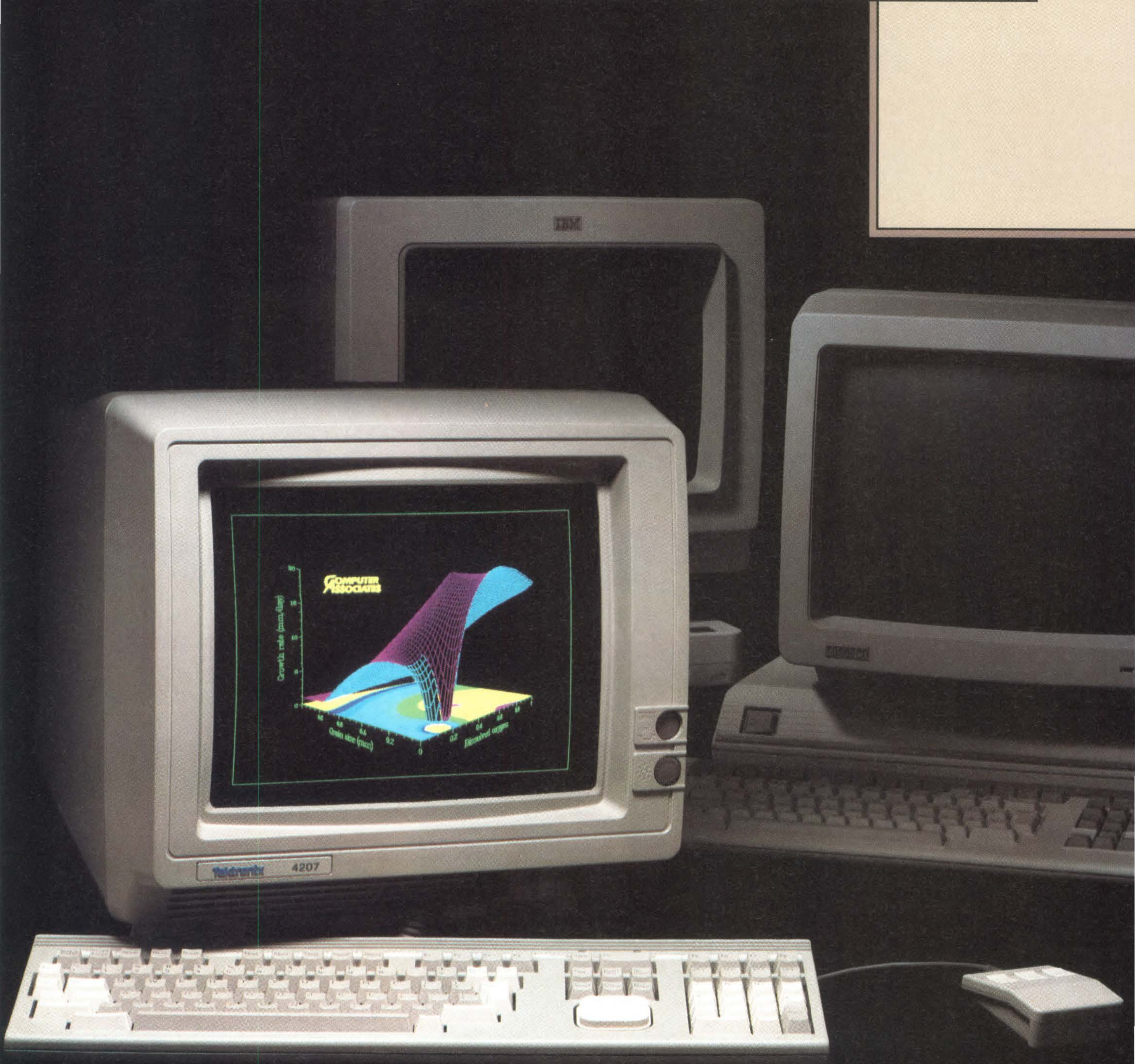

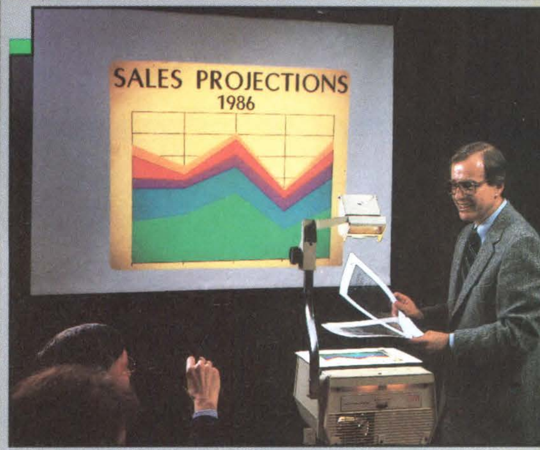

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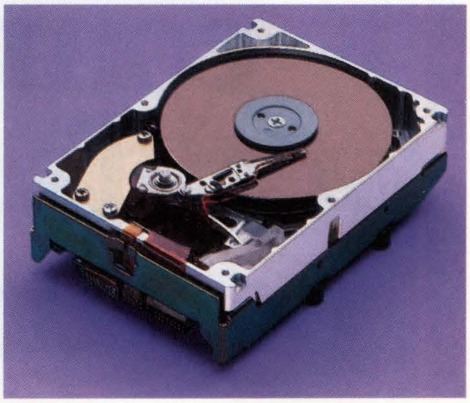

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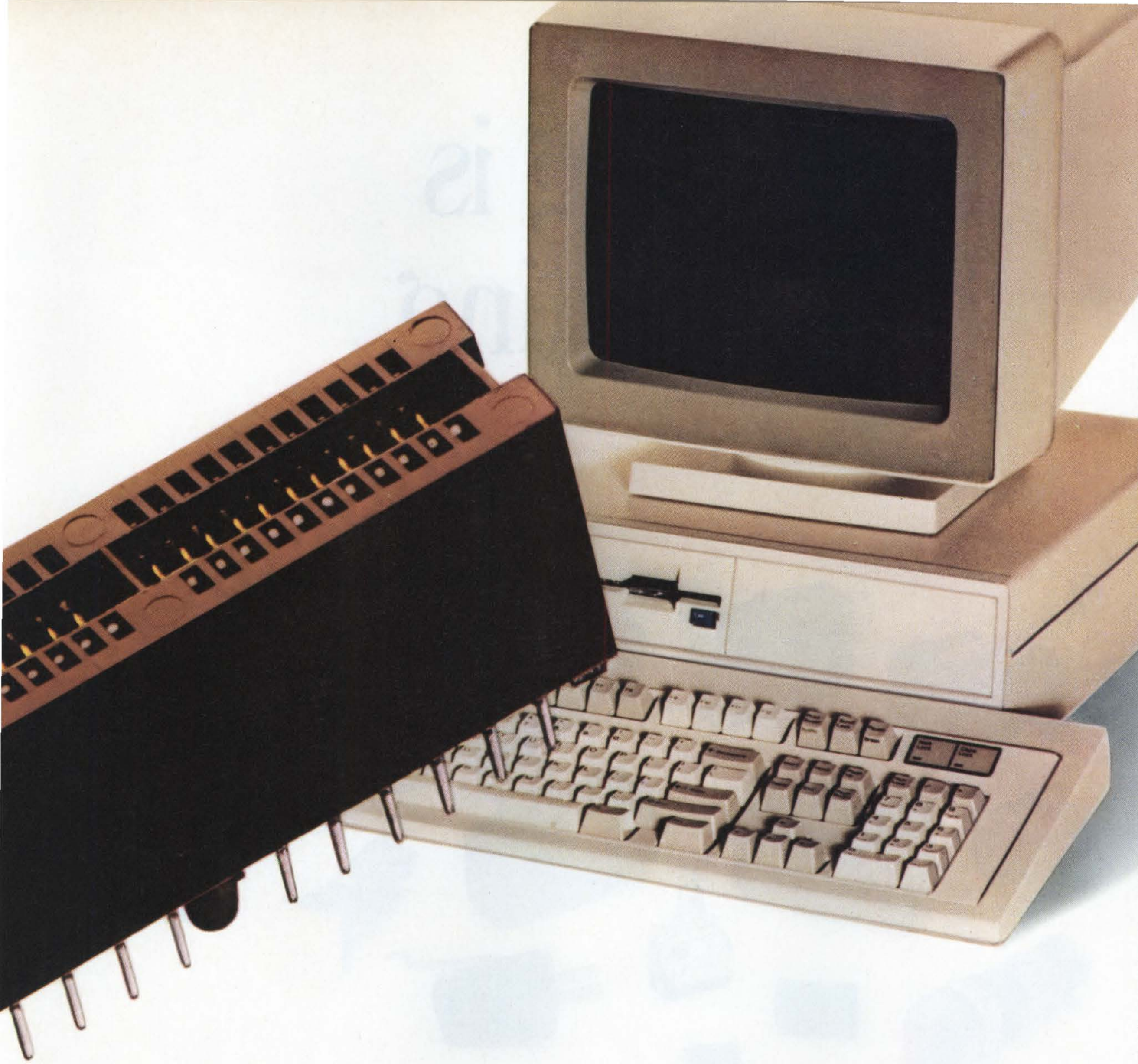

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Digitize analog functions using simple procedures

A digital implementation of a traditionally analog function yields both technical and economic advantages. If you've had trouble converting analog functions to a form that a μP can handle, you'll be glad to learn of some simple procedures for converting from the frequency domain to the time domain.

George Ellis, *Industrial Drives*

As μPs become smaller, less expensive, and more powerful, more and more designers are using them to implement signal-processing functions that once were considered exclusively analog in nature. Digital implementations of filters, integrators, compensators, and similar functions yield greater flexibility, lower temperature drift, and much smaller unit-to-unit variation than their analog counterparts, which use op amps. Further, digital versions may also be cheaper, particularly if they are part of a system that already contains many digital components.

Even expert analog designers sometimes find it difficult to change the analog versions' frequency-domain parameters to the time-domain parameters needed by the corresponding digital versions. It's not that difficult, however, if you divide the task into three major stages:

1. Design the function you want in the frequency domain.
2. Convert the parameters from the frequency domain to the sample-data domain.
3. Convert the parameters from the sample-data domain to the time domain.

First design in the frequency domain

Analog designers generally are familiar with the basic principles of frequency-domain design—the use of root-locus and Bode plots, for example. These principles are based on the Laplace operator s, which is sometimes written as "jω." The normal practice is to write the transfer functions as H(s). To implement an integration expression, you would replace instances of 1/s with integrators consisting of op amps and capacitors, and you would use resistors for scaling.

When you want to convert an analog function to the time domain for digital implementation, however, a few restrictions apply. First, you must write the function as a ratio of zeros to poles; and second, the poles and zeros must appear either as real and single elements or as complex conjugate pairs. Because many analog functions inherently impose these restrictions, you'll find that most frequency-domain functions are already in this form.

A familiar example is a single-pole lowpass filter, for which the frequency-domain expression is

$$H(s)=2\pi f/(s+2\pi f),$$

Designing a digital implementation of a traditionally analog function is easier if you first transform the function from the frequency to the sampled-data domain.

where f is the break frequency. If you set the break at 100 Hz, the filter's expression becomes

$$H(s)=628.3/(s+628.3).$$

The second stage is to convert the frequency-domain (s-plane) expression to an equivalent sample-data (z-plane) expression. The difference between the two planes is that s-plane functions are based on integrations, and z-plane functions are based on time delays. It's convenient to use the z-plane expressions as an intermediate step because they are much closer to the operations of a digital system than are the s-plane expressions, and thus are easier to convert to the final time-domain expressions for which you can write a program.

For each s-plane function, an equivalent z-plane function exists; refer to **Table 1** for an abbreviated list of s-plane functions and their z-plane counterparts. Before you can convert the s-plane functions to the z plane, however, you must first select the sample time (cycle time), T, of the system. The value of T is somewhat arbitrary, but as a general guideline, select a value of T such that the sample frequency is at least 10 times the system bandwidth.

The 100-Hz lowpass filter mentioned in step 1 serves as a good example of how to use **Table 1.** Beginning with the first stage,

$$H(s)=628.3/(s+628.3).$$

If you select a 1-kHz sample rate, then T=0.001; replacing this value in entry 3 of **Table 1** yields

$$H(z)=z(1-e^{-0.6283})/(z-e^{-0.6283})$$
$$=0.4665z/(z-0.5335).$$

If the function is very complex, you can break down the full s-plane function into two or more simpler subfunctions, each of which is represented by one of the s-plane functions in **Table 1.** The final z-plane function is therefore the product of all the z-plane counterparts of the s-plane subfunctions.

In **Table 1,** the term T, although defined as the sample time of the system, also implies a relationship to dc gain (an integrator is a good example: Doubling the sample rate doubles the final count). The inclusion of gain terms is advantageous because it eliminates the need to adjust the overall gain of your filter at the end of the design process. You'll find that many z-transform tables do not include dc-gain terms, and therefore they differ from **Table 1.** However, you can use any set of transform tables to obtain subfunctions of a complex s-plane function, provided that you use them correctly and take into account any additional steps (such as gain adjustment) that they may require.

Once you've converted your function to the sample-

TABLE 1—S-PLANE/Z-PLANE COUNTERPARTS

ENTRY NO	S-PLANE EXPRESSION		Z-PLANE COUNTERPART
1	INTEGRATOR: $1/s$	⟷	$Tz/(z-1)$
2	DIFFERENTIATOR: s	⟷	$(z-1)/Tz$
3	REAL POLE: $a/s+a$	⟷	$z(1-e^{-aT})/(z-e^{-aT})$
4	REAL ZERO: $(s+a)/a$	⟷	$(z-e^{-aT})/(z(1-e^{-aT}))$
5	COMPLEX POLES: $\dfrac{\omega^2}{s^2+2\alpha\omega s+\omega^2}$	⟷	$\dfrac{z^2(1-2\times e^{-\alpha\omega T}\times\cos(\sqrt{1-\alpha^2}\times\omega T)+e^{-2\alpha\omega T})}{z^2-2\times z\times e^{-\alpha\omega T}\cos(\sqrt{1-\alpha^2}\times\omega T)+e^{-2\alpha\omega T}}$
6	COMPLEX ZEROS: $\dfrac{s^2+2\alpha\omega s+\omega^2}{\omega^2}$	⟷	$\dfrac{z^2-2\times z\times e^{-\alpha\omega T}\cos(\sqrt{1-\alpha^2}\times\omega T)+e^{-2\alpha\omega T}}{z^2(1-2\times e^{-\alpha\omega T}\cos(\sqrt{1-\alpha^2}\times\omega T)+e^{-2\alpha\omega T})}$

WHERE a=1/TIME CONSTANT OF POLE
α=DAMPING RATE
e=EXPONENT
T=SAMPLE TIME
ω=NATURAL FREQUENCY ($2\pi f$)

data (z-plane) domain, you can then move on to the final design stage of the digital implementation, converting from the sample-data domain to the time domain. In order to do so, it's important that you understand that, because data is normally updated once every cycle, the variables in the system are only "snapshots." Consequently, data is represented either as new or as delayed by some integer number of samples.

Normally you add a subscript to a function to indicate, in shorthand form, the number of delay cycles. For example, f_k indicates the most recent value of f(t) (that is, in the current cycle). The expression f_{k-1} indicates the value of f(t) delayed by one sample period (that is, the value of f(t) during the previous cycle).

One of the basic properties of the z plane is that dividing a value by z yields the value you'd obtain after a delay of one sample time. Thus, the goal of this stage is to rewrite the z-plane function, replacing each z with a delay. You can accomplish the conversion to the time domain by performing the following steps:

1. Write the transfer function in the z plane as a function of output to input.

2. Multiply out the equation so that no "z"s appear in any denominator.

3. Divide the terms in the equation by the highest power of z that appears in the equation.

4. Replace the z-plane functions with functions that represent a delay of one sample period for each negative power of z. For example, replace $z^{-2}\times out(z)$ with out_{k-2}.

5. Move the undelayed output term to the left side of the equation and move all other terms to the right side.

Use the steps to implement a lowpass filter

Felicitously, the 100-Hz lowpass filter is simple enough to provide a complete demonstration of the entire digital-implementation process:

- stage 1 (write the s-plane function):

$$H(s)=2\pi f/(s+2\pi f)=628.3/(s+628.3)$$

- stage 2 (convert to z-plane function):

$$H(z)=0.4665z/(z-0.5335)$$

- stage 3 (convert to time domain):

step 1: $OUT(z)/IN(z)=0.4665z/(z-0.5335)$
step 2: $OUT(z)\times(z-0.5335)=IN(z)\times 0.4665z$
step 3: $OUT(z)-0.5335\times OUT(z)/z=0.4665\times IN(z)$
step 4: $OUT_k-0.5335\times OUT_{k-1}=0.4665\times IN_k$
step 5: $OUT_k=0.5335\times OUT_{k-1}+0.4665\times IN_k$.

You can now write a Basic program that simulates the function of a lowpass filter with the characteristics specified in step 5. The program **(Listing 1)** simulates the action of driving the filter with a 25-Hz sine wave and displays the filter's first 200 outputs. When you run the program, you'll see that the output is attenuated by 3% of the input and that it lags the input by a delay of 1

LISTING 1—SIMULATION OF LOWPASS FILTER

```
1 REM  100-HZ SINGLE-POLE LOWPASS FILTER WITH INPUT OF 25 HZ.

4 REM  OUT0 AND IN0 ARE THE MOST RECENT VALUES OF

6 REM  OUT AND IN.

8 REM  OUT1 IS OUT DELAYED BY ONE SAMPLE TIME.

10 TIME=0
20 T=0.001
30 OUT1=0
40 PRINT "  TIME      INPUT      OUTPUT"
50 FOR K=1 TO 200
60     TIME=TIME+T
70     IN0=SIN(6.283*25*TIME)
80     OUT1=OUT0
90     OUT0=(0.4665*IN0) + (0.5335*OUT1)
100    PRINT USING " #.###  ####.###  ####.###",TIME,IN0,OUT0
110 NEXT K
120 END
```

Each s-plane function has a z-plane counterpart. You can use these functions by breaking down complex functions into separate subfunctions.

to 2 msec, corresponding to phase angles between 10° and 20°. A lowpass filter driven at 25% of its break frequency (as this one is) should theoretically provide 3% attenuation and 14° of lag—which correlates well with the experimental result.

You can apply steps to complex functions

You can apply the step-by-step design procedure to transfer functions much more complicated than the lowpass filter in the previous example. For instance, consider an integrator with lead compensation. Assume that the lead zero is set to 10 Hz, the pole is set to 40 Hz, and the dc gain is 0.25. The integrator is to have a gain of 100 at 1 rad/sec, and the sample time is 0.001 sec. Applying the 3-stage design procedure to the integrator yields the results of **Fig 1**.

From these results, you can write a Basic program that simulates the operation of the filter when it receives a 20-Hz input **(Listing 2)**. From the definition of H(s), the gain of the transfer function is −8 dB at 20 Hz, and the output lags the input by 53.1°. When you run the program, you'll find that if you eliminate (by

STAGE 1:

$$H(s)=\frac{s+62.83}{s+251.3}\times\frac{100}{s}$$

$$=\frac{s+62.83}{62.83}\times\frac{251.3}{s+251.3}\times\frac{62.83}{251.3}\times\frac{100}{s}$$

STAGE 2:

$$H(z)=\frac{z-0.9391}{0.0609z}\times\frac{0.2222z}{z-0.7778}\times 0.25\times\frac{100\times 0.001z}{z-1}$$

$$=0.09122\times\frac{(z-0.9391)z}{(z-0.7778)(z-1)}$$

STAGE 3:

STEP 1: $\frac{OUT(z)}{IN(z)}=0.09122\times\frac{(z-0.9391)z}{(z-0.7778)(z-1)}$

STEP 2: $OUT(z)\times(z^2-1.778z+0.7778)=0.09122\times IN(z)\times(z^2-0.9391z)$

STEP 3: $OUT(z)\times(1-1.778/z+0.7778/z^2)=0.09122\times IN(z)\times(1-0.9391/z)$

STEP 4: $OUT_k{}^{1}1.7778\times OUT_{k-1}+0.7778\times OUT_{k-2}=0.09122\times IN_k-0.08567\times IN_{k-1}$

STEP 5: $OUT_k=1.778\times OUT_{k-1}-0.7778\times OUT_{k-2}+0.09122+IN_k-0.08567\times IN_{k-1}$

Fig 1—For just about any frequency-domain function you want to digitize, *this simple 3-stage design procedure will work. In the first stage, you write the function in its s-plane form. In the second stage, you transform the expression to the sample-data (z-plane) domain. The third stage transforms the expression to the time-domain form that you can implement digitally. The example presented here is a digital implementation of a lead-compensated integrator.*

LISTING 2—SIMULATION OF LEAD-COMPENSATED INTEGRATOR

```
10 REM  LEAD-COMPENSATED INTEGRATOR WITH AN INPUT AT 20 HZ.

20 REM  OUT0 AND IN0 ARE THE MOST RECENT SAMPLES OF OUT AND IN.

40 REM  OUT1 AND IN1 ARE OUT AND IN DELAYED BY ONE SAMPLE TIME.

60 REM  OUT2 IS OUT DELAYED BY TWO SAMPLE TIMES.

80  DEFDOUBLE I,O,T
90  DEFINT K
100 TIME=0.0
110 T=0.001
130 IN1=0.0
140 OUT1=0.0
150 OUT2=0.0
160 PRINT "  TIME       INPUT       OUTPUT"
170 FOR K=1 TO 200
180     TIME=TIME+T
190     OUT2=OUT1
200     OUT1=OUT0
210     IN1=IN0
220     IN0=SIN(6.283*20*TIME)
230     OUT0=(1.778*OUT1)-(0.7778*OUT2)+(0.09122*IN0)-(0.08567*IN1)
240     PRINT USING " #.###  ####.###  ####.###",TIME,IN0,OUT0
250 NEXT K
260 END
```

When designing digital filters, you must limit the input signal frequency to avoid the aliasing phenomenon.

subtraction) the dc portion of the gain, the output is 40% of the input (an attenutation of about 8 dB), and the output lags the input by 7 msec (equivalent to approximately 50° at 20 Hz). These results correlate well with the s-plane design characteristics.

Limit the input frequency to avoid aliasing

When designing digital filters, you must take care to avoid aliasing effects. Aliasing is the name of a phenomenon that causes input frequencies greater than half the sampling frequency to appear in the output transformed into frequencies less than half the sampling rate. **Fig 2** shows the effects of aliasing on a system with a sample rate of 100 Hz. You'll see that all input frequencies greater than 50 Hz (which is half the sampling rate) appear in the output as frequencies between 0 and 50 Hz.

For integral harmonics of the sampling rate, the apparent frequency is 0. All other frequencies are transformed to the difference between f (the input frequency) and xn, where n is the sampling rate and x is an integer representing the nearest integral harmonic of the sampling rate. Thus, in **Fig 2,** an input frequency of 230 Hz appears as an apparent output frequency of $230-(2\times100)=30$ Hz; an input of 270 Hz would appear as $(3\times100)-270=30$ Hz. Aliasing continues indefinitely as you raise the input frequency.

Thus, to avoid spurious output signals, you must limit the maximum input frequency to a value that is no greater than half the sampling rate of the system. You can achieve this limit by raising the sampling frequency so that aliasing will not begin until a frequency occurs that is higher than that of any expected signal; this is the preferred (and least expensive) method. If it is impractical (or otherwise undesirable) to raise the sampling rate, you can insert an analog lowpass filter in the signal path before the digitizing circuitry.

Procedure suits many applications

The 3-stage design procedure presented here is suitable for a wide variety of s-plane functions, including notch filters and PID compensators in servo systems. Not only does it produce more accurate break frequencies than some other popular methods (for example, the bilinear transformation or the w-plane transform), it is also a good deal more straightforward. You can depend on the procedure to produce accurate digital implementations of traditionally analog filters, with minimal complications.

However, in certain circumstances, stage 3 does not always produce the optimum result with respect to arithmetic noise, to which integrators are very sensitive. You may, therefore, find it desirable to separate an integrator from other functions and design it for minimum noise.

Likewise, for higher-order functions, you may wish to break up the frequency-domain functions into parallel (not cascaded) subfunctions and implement each part separately, using the 3-stage design procedure for each subfunction. And finally, if you find that the computing time imposes an undue delay between the instant at which the data is sampled and the instant at which the corresponding output value becomes available, you may want to rewrite the equations in a manner that allows the processor to perform much of the background computation before the data cycle begins. **EDN**

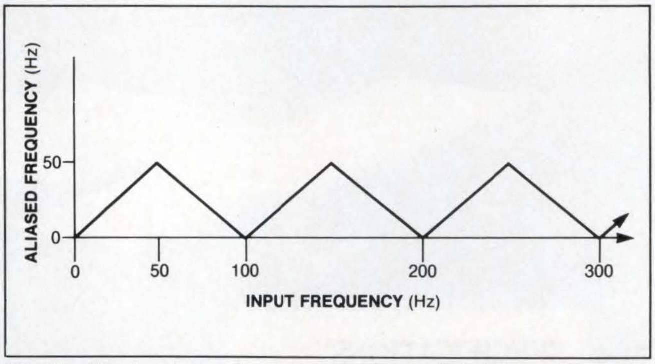
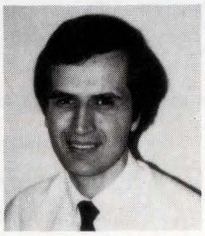


Fig 2—Aliasing is a phenomenon of sampled-data systems *and results in spurious output signals. Input frequencies that are greater than half the sampling rate appear in the output as frequencies between 0 and half the sampling rate. To avoid aliasing effects, you must place an upper limit on the input signal frequency.*

Author's biography



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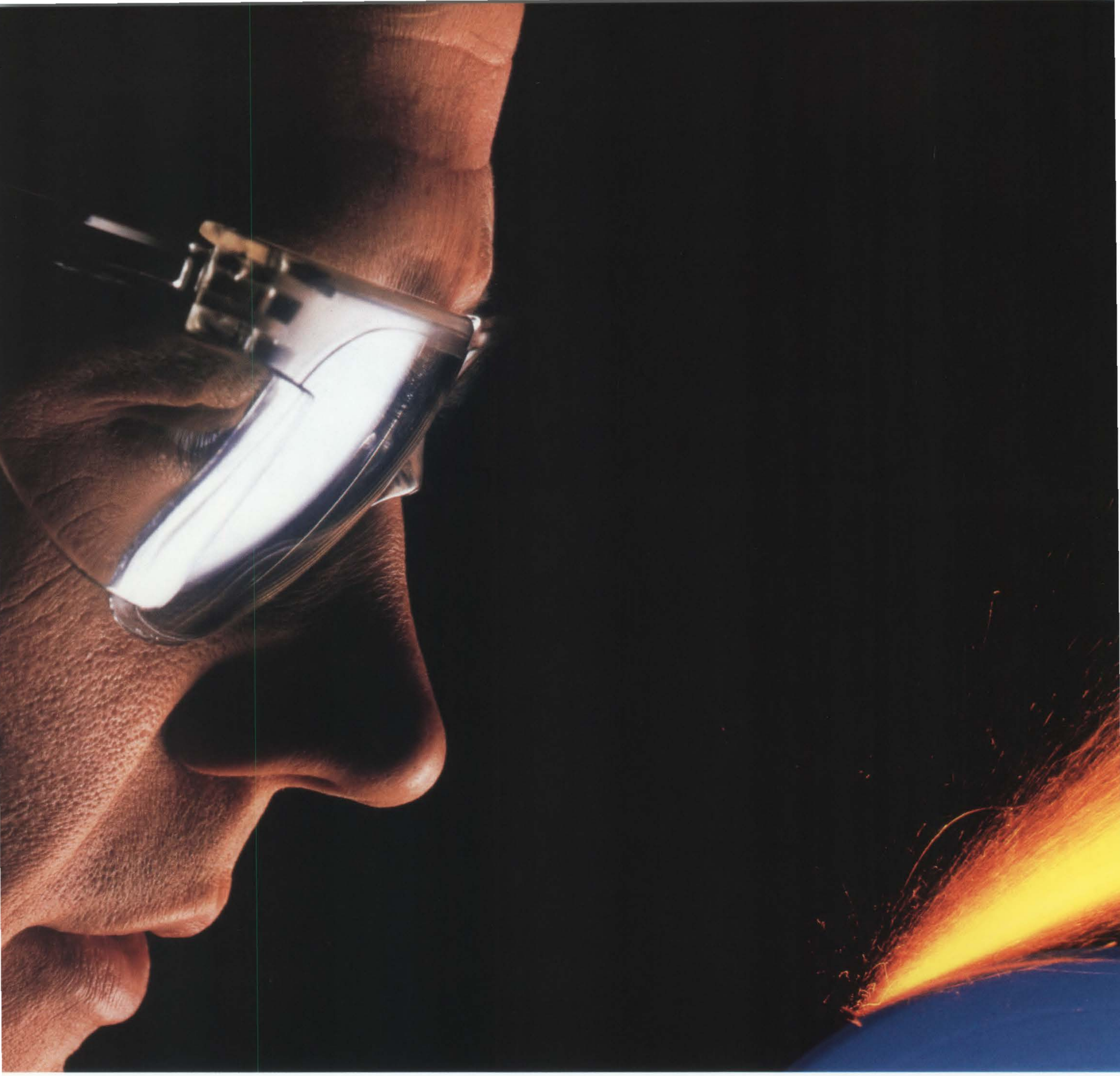

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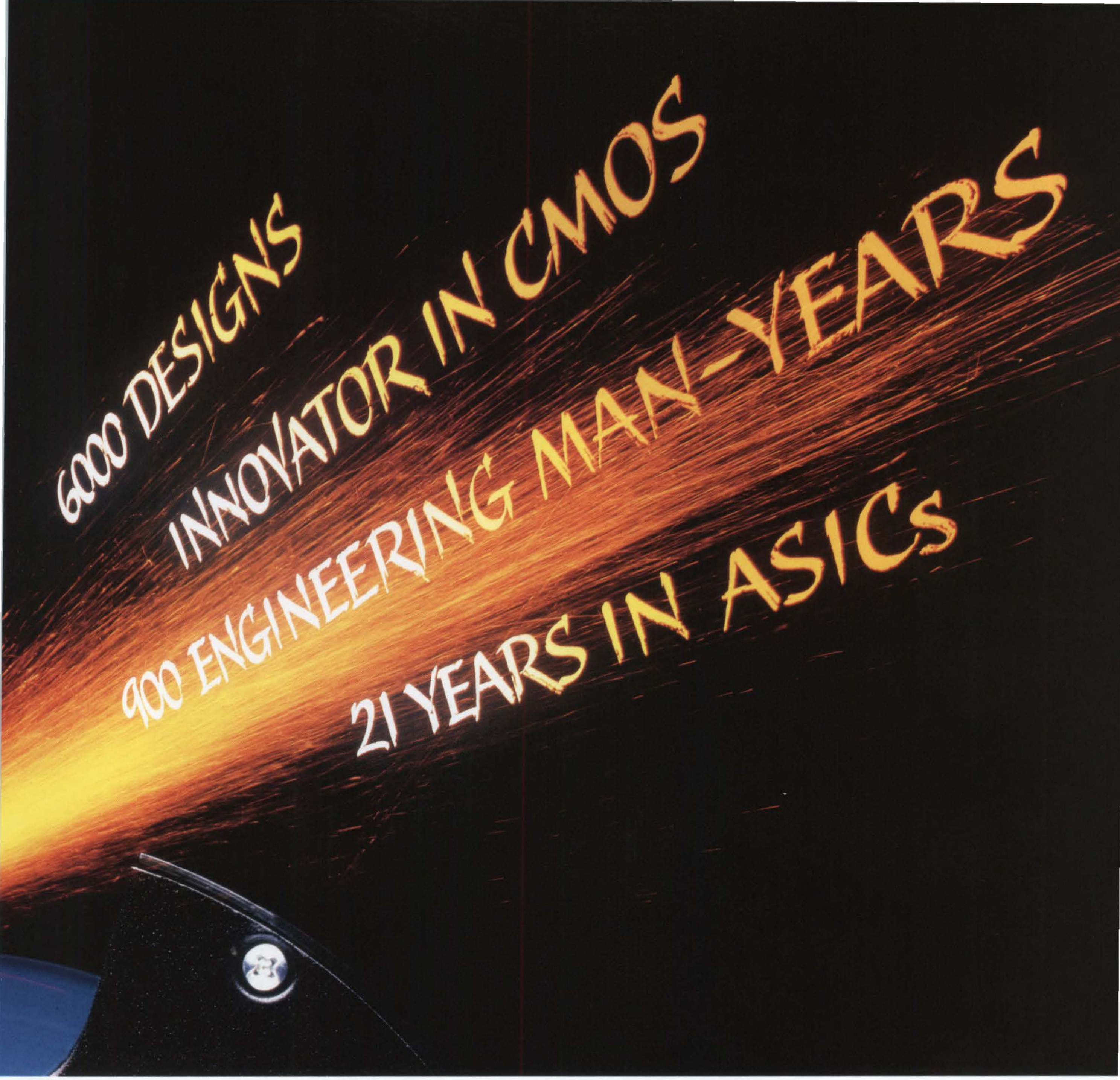
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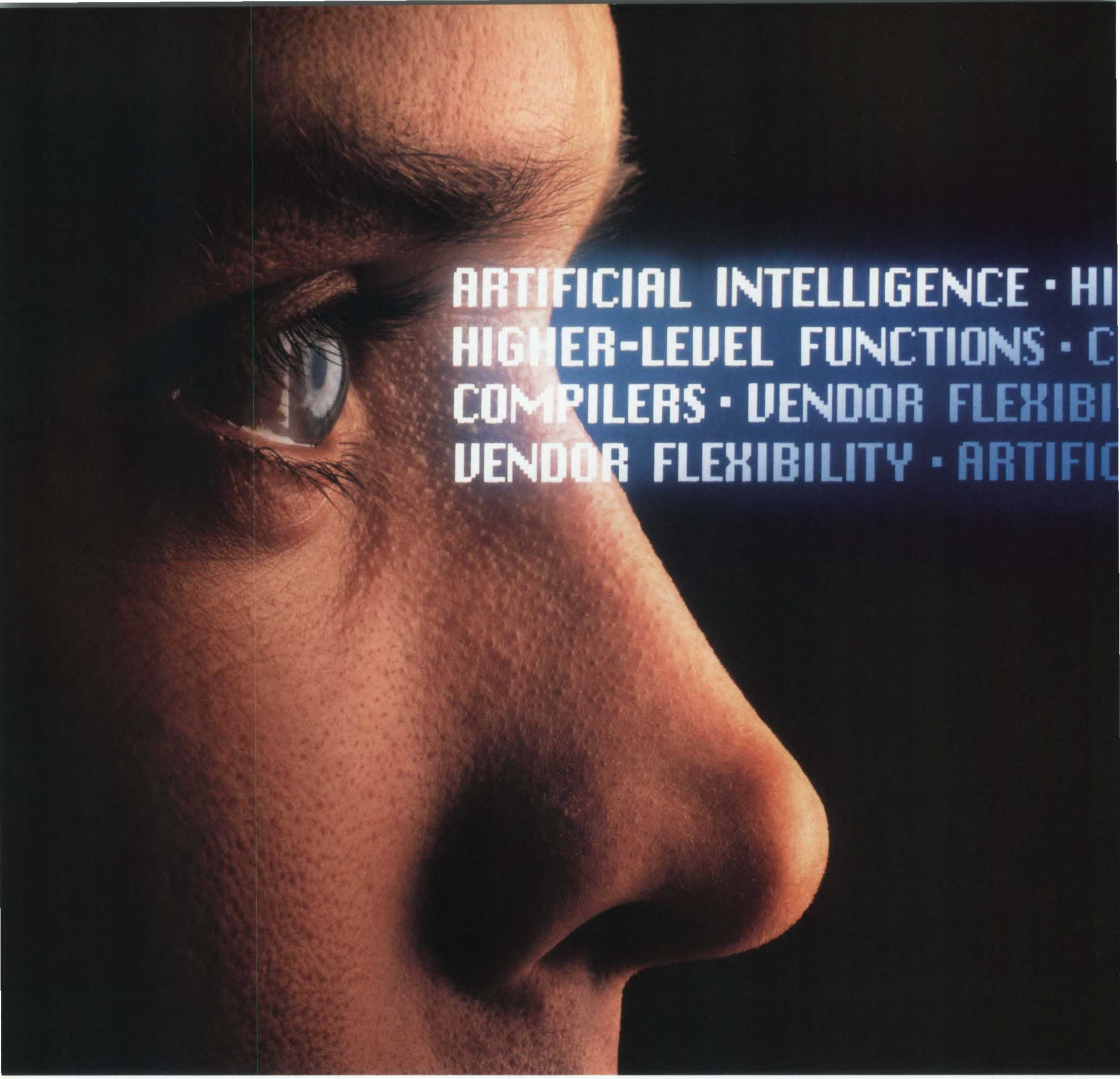

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Motor modeling simplifies design of control systems

Electric motors are electromechanical systems, but you can model them as purely electrical networks of familiar components. These models enable you to accurately predict the performance of feedback control systems that use motors.

Claudio de Sa e Silva, *Unitrode Corp*

An electric motor is a device that transforms electric power into mechanical power. In the case of permanent magnet (PM) electric motors, this power transformation works in both directions. Therefore, the electrical impedance depends on the mechanical load, and similarly, the mechanical behavior of the motor depends on conditions at the electrical end.

Because of the motor's dual nature, you can represent it, along with its mechanical load, as a set of familiar electrical components, such as capacitors and resistors. Constructing such models improves your understanding of motors and allows you to accurately predict the response of feedback control systems that use them.

Before getting started, it is important to understand the system of measurement units used in the analysis.

The metric system has undergone a number of changes in its history, but the latest version is called SI (Systeme International d'Unites). This system has become popular in most of the industrialized world, largely because it is coherent—that is, the product or quotient of two or more units is the unit of the resulting quantity. Certain simplifications result from using SI metric units.

The SI system uses Newtons (N) to measure force and meters (m) to measure distance. Consequently, the units of torque are Nm (**Table 1**). If a motor shaft rotates at an angular velocity of ω_M radians per second, with torque T_M, the mechanical power output will be equal to the product of T_M and ω_M, and the units will be watts if T_M is in Nm.

In the SI system, K_T equals K_V

Motor manufacturers usually specify a torque constant (K_T) and a voltage constant (K_V) for their motors. These constants have different values when the torque and speed are measured in English units, but their numerical values are equal when you use SI units. This fact becomes obvious when you consider that the total mechanical power must equal the converted electrical power:

$$V_A I_A = T_M \omega_M \text{ (watts)} \quad (1)$$

$$V_A/\omega_M = T_M/I_A = K_{TV}, \quad (2)$$

where V_A is the internally generated armature voltage, *Because of the motor's dual nature, you can represent it along with its mechanical load as a set of familiar electrical components.*

or back electromotive force (EMF), *not* the voltage you apply to the motor, and I_A is the armature current. T_M is the total torque developed. (See **Fig 1** for definition of motor terms.)

A motor is a transformer

If you do the same thing with the familiar electrical transformer, you get the turns ratio:

$$V_1I_1=V_2I_2 \text{ (watts)} \quad (3)$$

$$V_1/V_2=I_2/I_1=N_1/N_2. \quad (4)$$

Thus, the nondimensional turns ratio N_1/N_2 is analogous to the dimensional torque (or voltage) constant K_{TV}. Furthermore, **Eqs 2** and **4** give a clear hint that the angular velocity (ω_M) is analogous to voltage, while the torque (T_M) is analogous to current.

The units of K_{TV} may be either Nm/A or V/(rad/sec). Thus, specifying both K_T and K_V for a motor is like measuring and specifying both the voltage ratio and the current ratio of a transformer.

There is a clear analogy between K_{TV} and a transformer's turns ratio; angular velocity and voltage; and torque and current. Because the motor behaves as a transformer, you might expect to find the square of K_{TV} involved in something analogous to impedance transformation.

Suppose you apply a constant current I_A to the armature of a motor whose load is its own moment of inertia J_M (Nm sec^2). Neglecting mechanical losses,

TABLE 1—UNITS CONVERSION

THESE UNITS	{ X → = ; = ← ÷ }	SI UNITS	DIMENSION
OZ	2.78×10^{-1}	N	MLT^{-2}
LB	4.448	N	MLT^{-2}
IN.	2.54×10^{-2}	m	L
FT	3.048×10^{-1}	m	L
GF	9.807×10^{-3}	N	MLT^{-2}
G CM^2	10^{-7}	Nm SEC^2	ML^2
FT LB SEC^2	1.356	Nm SEC^2	ML^2
OZ IN SEC^2	7.063×10^{-3}	Nm SEC^2	ML^2
FT LB	1.356	Nm	ML^2T^{-2}
OZ IN	7.063×10^{-3}	Nm	ML^2T^{-2}

NOTE: THE DIMENSIONS ARE M (MASS), L (LENGTH), AND T (TIME). THE GRAM (G) IS A UNIT OF MASS, AND THE GRAM-FORCE (GF) IS A UNIT OF FORCE. THE POUND (LB) AND THE OUNCE (OZ) ARE INCLUDED AS UNITS OF FORCE ONLY.

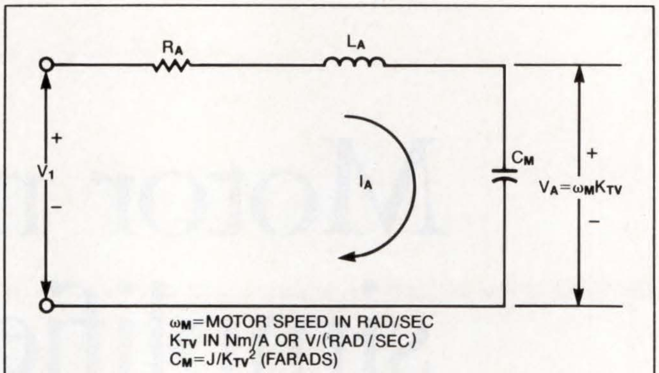


Fig 1—This series RLC circuit *is an excellent model of a dc motor loaded with an essentially inertial load. Here, J is the total moment of inertia, including the motor's J_M.*

according to Newton's law for rotating objects,

$$T_M=J_M\alpha_M,$$

where α_M is the angular acceleration $d\omega_M/dt$.

Since, from **Eq 2**, $T_M=I_AK_{TV}$,

$$I_AK_{TV}=J_Md\omega_M/dt.$$

Also from **Eq 2**,

$$\omega_M=V_A/K_{TV}$$

so that

$$I_A=(J_M/K_{TV}^2)\times(dV_A/dt). \quad (5)$$

Eq 5 has a familiar form; the quantity J_M/K_{TV}^2 is analogous to a capacitor. It follows that the motor "reflects" a moment of inertia J_M back to the electrical primary as a capacitor of J_M/K_{TV}^2 farads.

A neat way to check this result is to equate the energy stored kinetically in J_M with the electrical energy stored in a capacitor C_M:

$$\tfrac{1}{2}C_MV_A^2=\tfrac{1}{2}J_M\omega_M^2$$
$$C_M=J_M(\omega_M/V_A)^2.$$

Since $\omega_M/V_A=1/K_{TV}$,

$$C_M=J_M/K_{TV}^2 \text{ (farads)}. \quad (6)$$

Similarly, a torsional spring with spring constant K_S (Nm/rad) is reflected as an inductance of K_{TV}^2/K_S henries. And a viscous damping component B (Nm sec/rad) appears as a resistor of K_{TV}^2/B ohms.

Once you can represent the mechanical load by means of electrical elements, you can draw an equivalent circuit of the motor and its mechanical load. The armature has a finite resistance R_A and an inductance L_A, through which the torque-generating current I_A must flow. You have to include these components; they are too large to ignore. You can represent an inertially loaded motor as shown in **Fig 2**, where the moment of inertia, J, is the sum of the load's J_L and the rotor's J_M.

It turns out that, in practice, the moment of inertia that the motor must work against or with (depending on how you look at it) is by far the most important component of the mechanical load. A frictional component also exists, but because it is largely independent of speed, you would represent it electrically as a constant current source, which could not affect the dynamic behavior of the motor. And, since you rarely find a torsional spring load, it makes sense to only concentrate on the inertial aspect of the problem.

Measuring the components isn't difficult

The measurement of R_A and L_A is not difficult. A good ohmmeter will get you R_A, and you can measure the electrical time constant τ_E to calculate L_A:

$$L_A=\tau_E R_A.$$

Just make sure that the rotor remains stationary during these measurements.

To determine the value of the capacitor, C_M, you need to measure the shaft speed. If you are measuring the speed of a brushless dc motor, you can use the signal from one of the Hall effect devices as a tachometer. If the Hall frequency is f_H, and the number of rotor poles is P, the angular velocity ω_M is

$$\omega_M=4\pi f_H/P \text{ (rad/sec)}.$$

With motors of other types, you will need a strobe light or some other means (for example, a tachometer) to measure speed.

Measure the mechanical time constant

A good way to measure C_M is through a measurement of the mechanical time constant τ_M. Measure τ_M by driving the motor with a constant voltage and measuring the time it takes to accelerate from zero speed to 63% of the highest speed achievable at the voltage used. To set a safe limit on the starting current during the measurement of τ_M, apply a low voltage, or add a resistor in series with the motor, or both. The setup is shown in **Fig 2**. Note that the armature resistance R_A is already known. You can add resistors R_B, if needed, to limit the armature current I_A to a value that is safe for both driver and motor.

The first step in measuring τ_M is to apply an armature voltage, which, as mentioned before, will probably be lower than the motor's normal armature voltage. Let the motor run freely and measure W_{MAX} and I_{MAX}, and use these values to calculate the armature voltage V_{MAX}:

$$V_{MAX}=V_{CC}-V_{SAT}-I_{MAX}(R_A+R_B).$$

Here V_{CC} is the supply voltage, V_{SAT} is the saturation voltage of the driving circuit, and I_{MAX} is the current drawn by the unloaded motor at maximum speed. Thus, you can calculate the voltage constant K_{TV}:

$$K_{TV}=V_{MAX}/\omega_{MAX} \text{ (V/(rad/sec))}.$$

Probably the best way to measure the frequency of a PM motor's Hall pulses is with an oscilloscope. Set the oscilloscope time scale so that you can easily read the pulse frequency corresponding to an angular velocity of 63% of ω_{MAX}, so that

$$\omega_M=0.63\omega_{MAX}.$$

By holding and releasing the motor shaft, take several readings of the time τ_M required to accelerate from zero

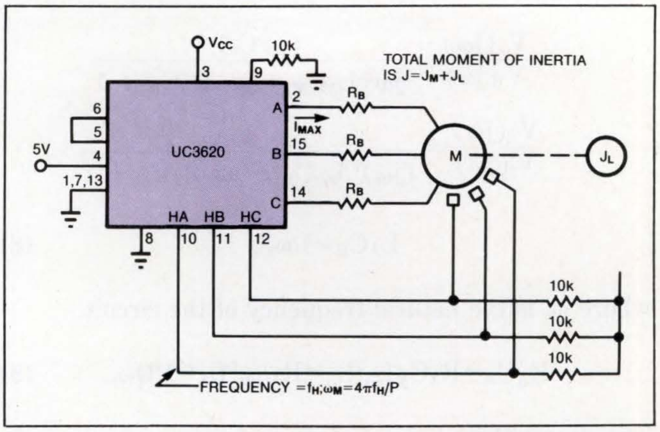


*Fig 2—**You can use this setup** to measure $C_M=J/K_{TV}$ of a 3-phase brushless dc motor with inertial load, J_L. The motor voltage, $V_M=V_{CC}-V_{SAT}$, where V_{SAT} is the output saturation voltage.*

The motor "reflects" a moment of inertia, J_M, back to the electrical primary as a capacitor of J_M/K_{TV}^2 farads.

to ω_M. Take these readings "on the fly," as the motor accelerates toward the maximum speed ω_{MAX}. Having obtained a good value of τ_M, you can now calculate

$$C_M=\tau_M/(R_A+R_B) \text{ (farads)}.$$

This completes the RLC equivalent circuit. If the value of J_M is also required, you can calculate it:

$$J_M=C_M K_{TV}^2.$$

In the circuit of **Fig 1**, V_1 is the voltage applied to the motor leads, and V_A is the actual armature voltage, or back EMF. This latter voltage is equal to $\omega_M K_{TV}^2$. To derive an expression relating the speed to the applied voltage, you can write

$$\omega_M/V_1=(1/K_{TV})(V_A/V_1) \text{ ((rad/sec)/V)} \quad \textbf{(7)}$$

If V_1 is a constant voltage, the speed ω_M will also be constant. That the speed is constant is clear from the circuit of **Fig 1**, as well as from a knowledge of motors. If, however, V_1 varies sinusoidally at some frequency, f, the speed ω_M will vary similarly, but the amplitude and phase will depend on the frequency f. This fact is very important if you plan to include the motor in a feedback loop, because the motor's contribution to the overall loop gain and phase shift is an important factor in determining stability. The motor's transfer function—that is, **Eq 7** expressed as a function of frequency—gives a precise description of how the amplitude and phase behave at different frequencies. To express the transfer function, use the variable $j\omega$, where $j=(-1)^{1/2}$ and $\omega=2\pi f$.

$$\frac{V_A(j\omega)}{V_1(j\omega)}=\frac{(j\omega C_m)^{-1}}{j\omega^2 L_A C_M + j\omega R_A C_M + 1}$$

$$\frac{V_A(j\omega)}{V_1(j\omega)}=\frac{1}{(j\omega)^2 L_A C_M + j\omega R_A C_M + 1}$$

$$L_A C_M=1/\omega_n^2, \quad \textbf{(8)}$$

where ω_n is the natural frequency of the circuit.

$$R_A C_M=R_A C_M L_A/L_A=R_A/\omega_n^2 L_A=1/Q\omega_n. \quad \textbf{(9)}$$

The circuit Q is

$$Q=\omega_n L_A/R_A.$$

Therefore,

$$\frac{V_A(j\omega)}{V_1(j\omega)}=\frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2+\frac{j\omega}{Q\omega_n}+1}$$

Furthermore, using **Eq 7**,

$$\frac{\omega_M(j\omega)}{V_1(j\omega)}=\left(\frac{1}{K_{TV}}\right)\cdot\frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2+\frac{j\omega}{Q\omega_n}+1}. \quad \textbf{(10)}$$

Because you have determined the values of K_{TV}, ω_n, and Q, you can calculate the magnitude and phase angle of **Eq 10** for various values of $j\omega$. For a given $\omega=\omega_1$, you can evaluate **Eq 10** to obtain a complex number A_1+jB_1 whose angle is

$$e_1=\tan^{-1}(B_1/A_1)$$

and whose magnitude you can express in decibels as follows:

$$M_1=20\log_{10}(A_1^2+B_1^2)^{1/2}.$$

A plot of these quantities, using a logarithmic frequency scale, is called a Bode plot. It can be a handy tool in understanding how the device will affect the final loop performance.

A small 3-phase brushless dc motor is used in a hard-disk Winchester drive. The motor's characteristics, measured as above, are

- $K_{TV}=0.015$ Nm/A or V/(rad/sec)
- $R_A=2.5\Omega$
- $L_A=0.002$H
- $J=0.001$ Nm $\sec^2$.

The J value was measured with three magnetic disks mounted, and it represents the actual value required for the application. Using **Eq 6**,

$$C_M=J/K_{TV}^2=0.001/(0.015)^2=4.44\text{f}.$$

The 4.44 farads may seem like an unusually large value for a capacitor, but it simply reflects the large amount of kinetic energy that the included inertia can store. From **Eq 8**,

$$\omega_n=\frac{1}{\sqrt{L_A C_M}}=\frac{1}{\sqrt{0.002\times 4.44}}$$

$$= 10.61 \text{ rad/sec}$$

From **Eq 9**,

$$Q=\omega_n L_A/R_A=10.61\times0.002/2.5=0.0085.$$

(The quality factor Q has no units).
The motor transfer function, given in **Eq 10**, is

$$\frac{\omega_M(j\omega)}{V_1(j\omega)}=\frac{66.67}{\left(\frac{j\omega}{10.61}\right)^2+\frac{j\omega}{0.09}+1}\ \text{(rad/sec)/V.} \tag{11}$$

A calculator that is preprogrammed to operate with complex numbers (for example, the HP 28C or 15C) makes the evaluation of this equation an easy task. With the 28C, you can set up a user routine called Bode, as follows:

<<DEG DUP ABS LOG 20 X SWAP ARG>>

This routine will convert a complex number $x+jy$ into $20\log(x^2+y^2)^{1/2}$ at level 2, and arc tan (y/x) at level 1. **Table 2** shows several such computations of **Eq 11.**

At ω_0, the transfer function evaluates as 66.67 (rad/sec)/V. As ω increases from zero, the gain decreases as shown in the gain column of **Table 2**. A Bode plot shows the gain relative to the initial, or dc, gain. Therefore, subtract $20\log_{10}(66.67)=36.4$ dB from each gain value in **Table 2** and plot the result. In effect, you are plotting only the function

$$G(j\omega)=\frac{1}{\left(\frac{j\omega}{10.61}\right)^2+\frac{j\omega}{0.09}+1}. \tag{12}$$

Compare **Eq 12** with **Eq 11. Fig 3** shows the results.

Note that to about 100 rad/sec (15.9 Hz), the phase lag barely exceeds 90°. The first pole occurs at ω=0.09 rad/sec, at which point the phase lag is 45°. The second pole, widely separated from the first in this case, occurs at a frequency in excess of 1000 rad/sec, as you can see from the further bend in the phase curve. The gain, which was drooping at a rate of −20 dB/decade below 100 rad/sec, now begins to bend toward a steeper droop of −40 dB/decade after the second pole is reached. At very high frequencies, the phase lag will reach 180°.

Used in a speed-control feedback loop, this motor will perform well, provided that you take its gain and phase behavior into account. You can account for gain and phase by incorporating the motor transfer function into the overall loop equation, which will also include other components. By performing this analysis, you will not only improve your understanding of a particular motor's behavior, but you will also better understand the differences between motors. **EDN**

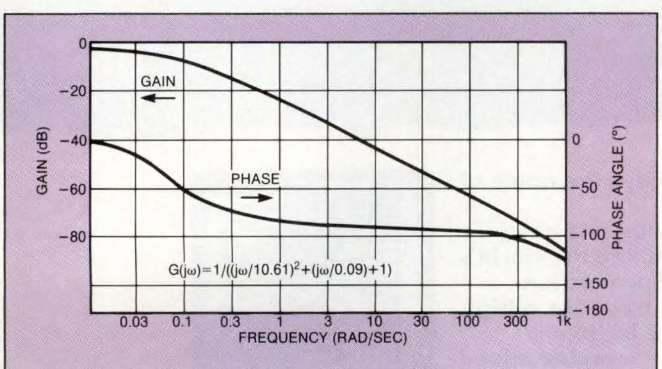
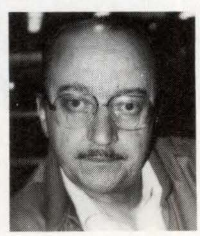


Fig 3—The Bode plot of the motor described by Eq 11 displays the effect of two widely separated poles.

TABLE 2—CALCULATED VALUES OF EQ II

ω (RAD/SEC)	$\omega_M(j\omega)/V_1(j\omega)$	GAIN (dB)	PHASE (°)
0.01	65.9−j 7.32	36.4	−6.3
0.03	60−j 20	36.0	−18.4
0.1	29.8−j 33.2	33.0	−48.0
0.3	5.5−j 18.4	25.7	−73.3
1.0	0.53−j 5.95	15.5	−84.9
3.0	0.06−j 2.00	6.0	−88.4
10.0	0−j 0.60	−4.4	−89.9
30.0	$-4.2\times10^{-3}-j\,0.20$	−14.0	−91.2
100	$-4.7\times10^{-3}-j\,0.06$	−24.5	−94.5
300	$-4.5\times10^{-3}-j\,0.02$	−34.2	−103.5
1000	$-2.9\times10^{-3}-j\,3.7\times10^{-3}$	−46.6	−128.6
3000	$-7.1\times10^{-3}-j\,3\times10^{-4}$	−62.3	−157.4

Author's biography



Claudio de Sa e Silva is an applications engineer at Unitrode Corp in Manchester, NH. Before joining Unitrode in 1984, he was a project engineer with Allen Bradley Co. Claudio received his BSEE from Columbia University and holds one patent. He has designed UHF receivers, phase-locked loops, and many dc-motor drives. He enjoys books and music in his spare time, and a good laugh at any time.

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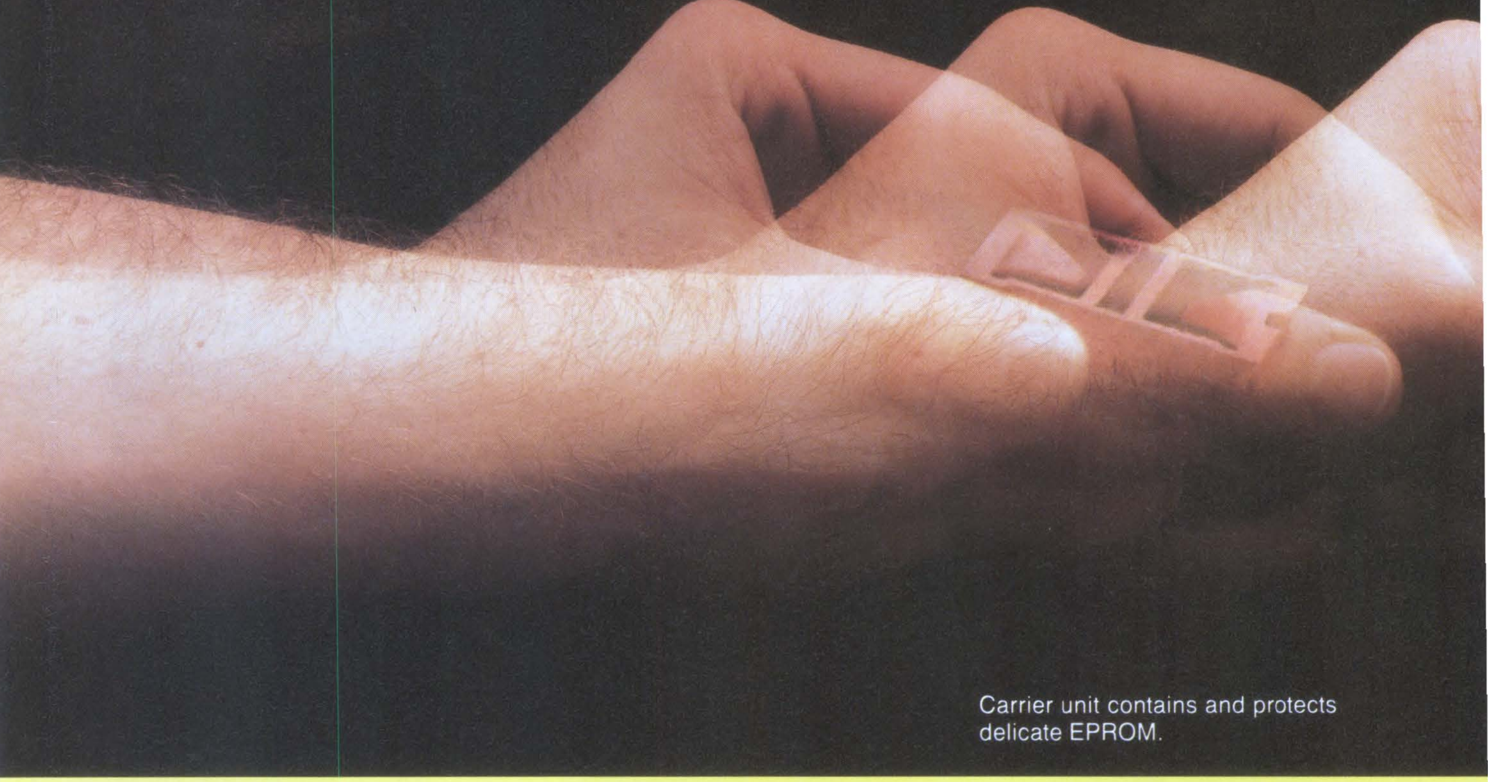

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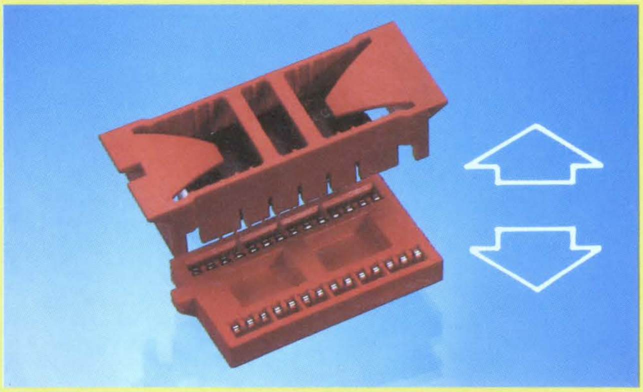

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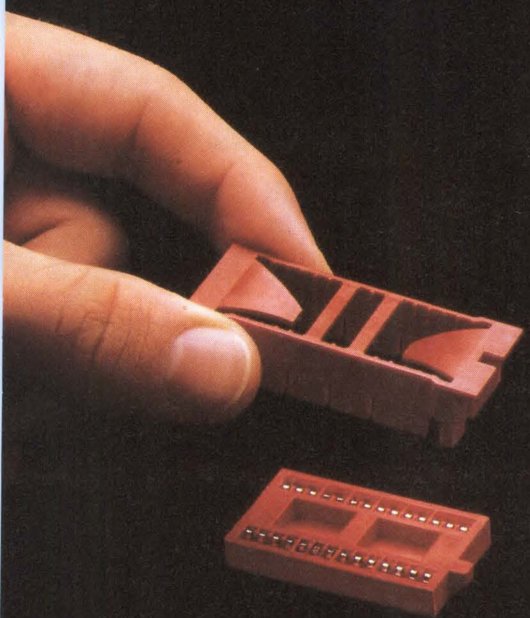

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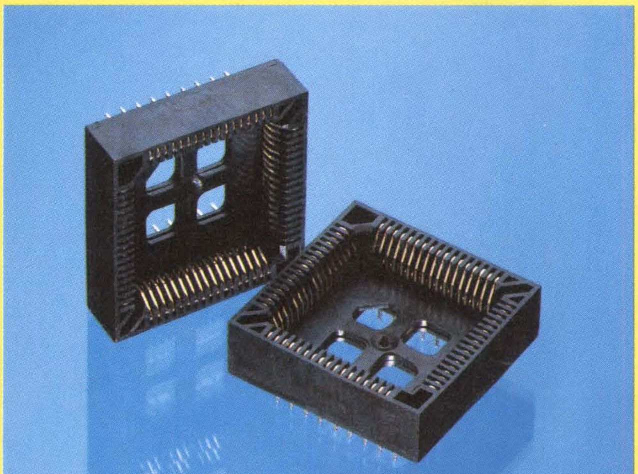

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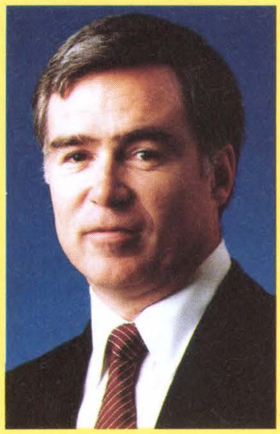

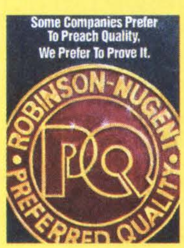

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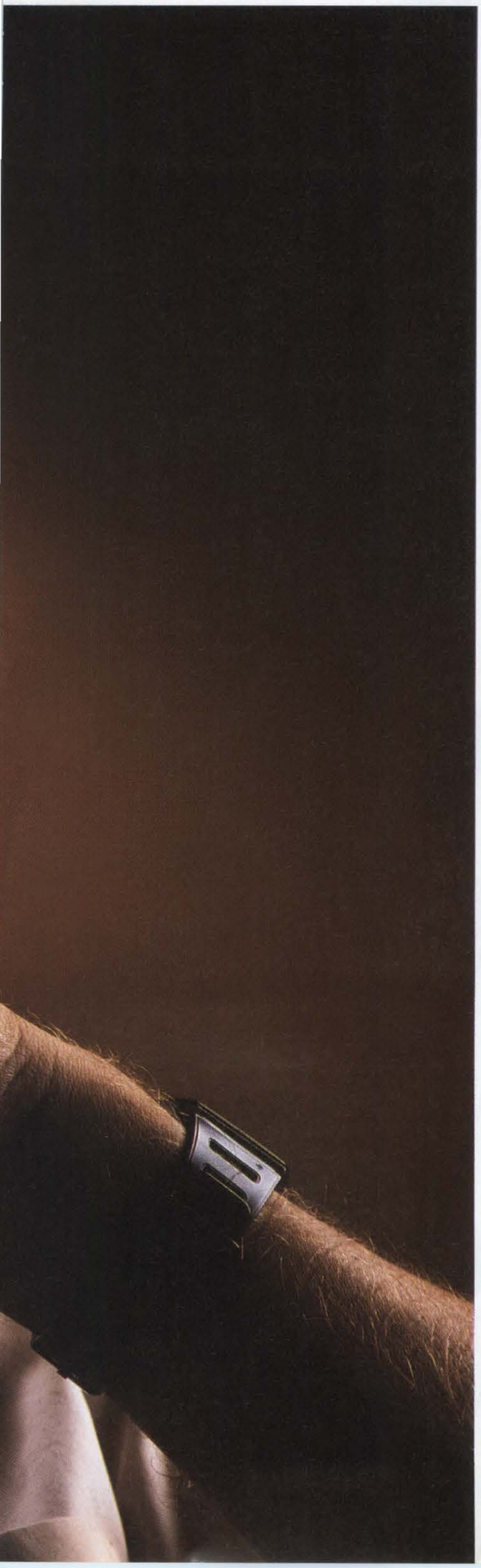

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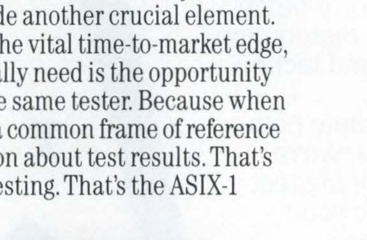

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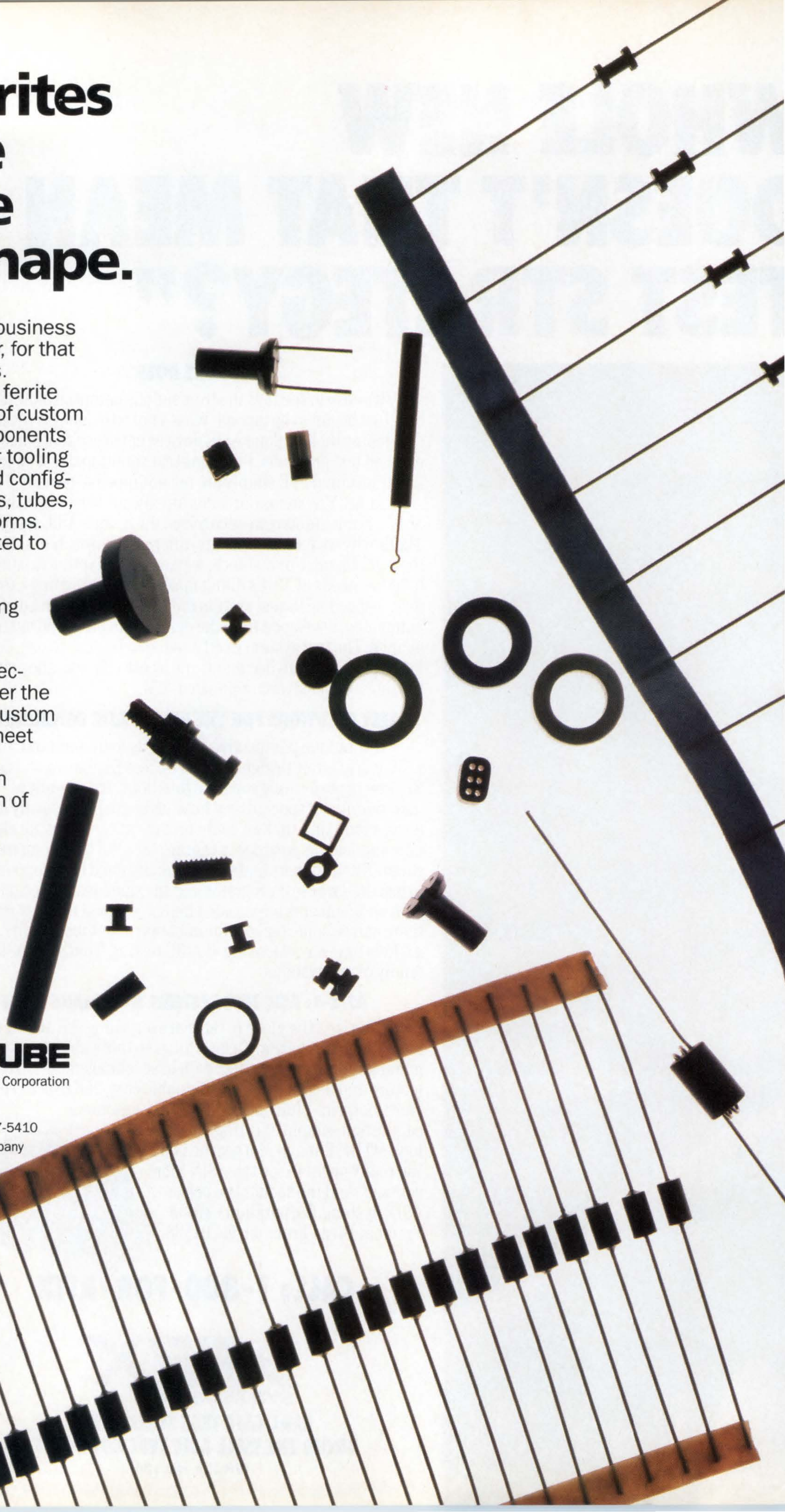

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Simple techniques help you conquer op-amp instability

Of all the problems that plague the op-amp user, the least understood and most vexing is an op amp's tendency to oscillate under certain conditions. The greater the op amp's bandwidth, the more acute the problem. Fortunately, you can use some simple techniques to quell these spurious oscillations.

Barry L Siegel, *Elantec Inc*

Operational amplifiers oscillate for many reasons. Both your application circuitry and the internal circuitry of the op amp can contribute to instability. The classical reason for instability is that your circuit's loop gain is greater than one (0 dB) when the phase shift through the amplifier varies from its low-frequency value by 180°. But other, less-well-understood factors also influence an op amp's stability. Understanding these factors will allow you to avoid oscillations in your op-amp designs.

For example, another cause of op-amp instability is power-supply inductance. A good rule of thumb is that the higher the amplifier's bandwidth, the more sensitive the op amp is to power-supply inductance. The circuit of **Fig 1** illustrates the point. As the amplifier drives its load, the load current generates a voltage across the supply-lead inductance, L_1. This voltage is essentially in phase with the input signal. Any stray capacitance between the V^+ terminal and the amplifier's input will cause oscillation.

Furthermore, the feedback need not be to the input. Stray capacitance between the V^+ node and an internal

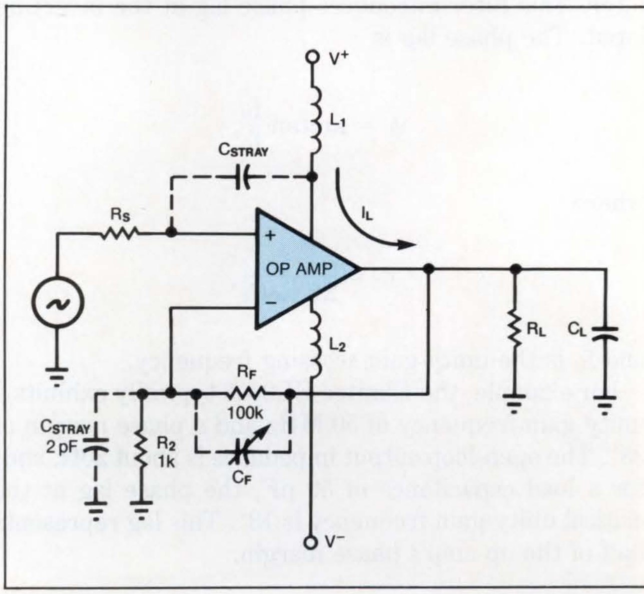

***Fig 1—Load current drawn through power-supply** lead inductance, L_1, generates a voltage. Stray capacitance can couple this voltage into the op amp's positive input and cause instability. Also, stray capacitance at the inverting input can form a lowpass filter. C_F cancels the filtering action.*

The higher its bandwidth, the more sensitive an op amp is to power-supply inductance.

node in the amplifier—the second stage, for example—can cause unstable performance.

The solution for this problem is to decouple the power-supply leads with capacitors. But, even so, problems still exist. Capacitors can become quite inductive at certain frequencies. An axial-lead CK05 ceramic capacitor can exhibit 10 nH at frequencies above 10 MHz, and it tends to resonate at 50 MHz. To avoid this problem, use chip capacitors that have minimal lead inductance. For example, AVX Corp's MLC Series surface-mount capacitors exhibit less than 1.5 nH of series inductance.

Obviously, not all applications lend themselves to surface-mount components. The alternative decoupling scheme in **Fig 2** can reduce the ringing on both the power-supply rail and the output, thereby minimizing the chance for oscillation. Because large capacitors can resonate with small parallel capacitors, you need the small series resistors, R_Q, to minimize the Q of the circuit.

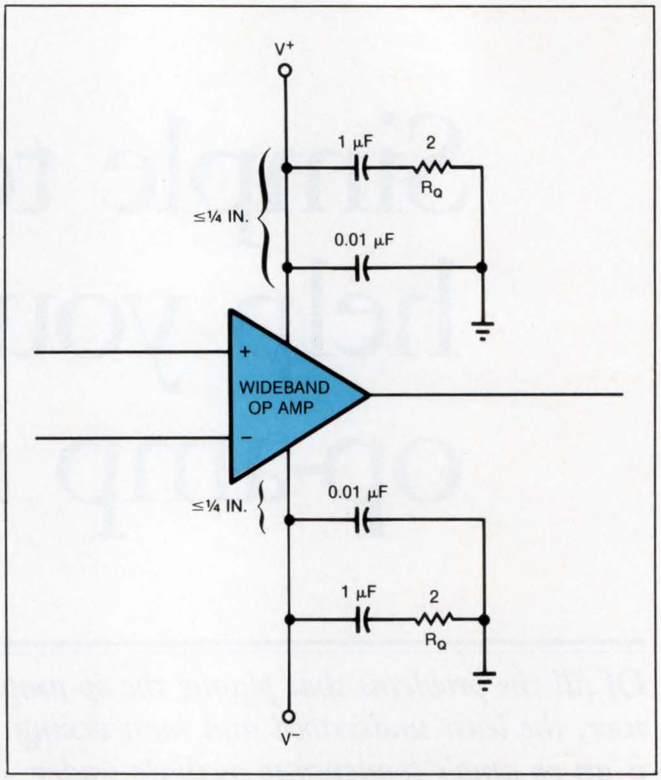

***Fig 2—If you can't employ surface-mount chip capacitors** in your design, you can use this power-supply decoupling scheme with conventional axial-lead components. Because large capacitors can resonate with small parallel capacitors, you need the small series resistors (R_Q) to minimize the Q of the circuit.*

Load capacitance degrades margin

A third oscillation gremlin arises from load capacitance. Degradation in phase margin can induce oscillation. In this instance, the operational amplifier in **Fig 1** exhibits an (open loop) output impedance (R_O), which, coupled with the load capacitance (C_L), forms a lowpass filter. This filter introduces phase lag at the inverting input. The phase lag is

$$\phi = \arctan \frac{f_U}{f_C},$$

where

$$f_C = \frac{1}{2\pi R_O C_L},$$

and f_U is the unity-gain crossing frequency.

For example, the Elantec EL2006 typically exhibits a unity-gain frequency of 50 MHz and a phase margin of 35°. The open-loop output impedance is about 20Ω, and, for a load capacitance of 50 pF, the phase lag at the critical unity-gain frequency is 18°. This lag represents half of the op amp's phase margin.

Emitter followers misbehave

External circuit elements are not the only reason for op-amp instability: The output stage of the op amp can have inherent problems. Most IC op amps use compound emitter followers for their output stages. Emitter followers tend to oscillate into a capacitive load. **Fig 3a** illustrates the hybrid-pi model of an emitter follower. **Fig 3b** is the equivalent circuit modeled from the emitter's perspective.

$$R_1 = \frac{1}{g_M} + \frac{r_{bb'} + R_S}{h_{FE}},$$
$$R_2 = r_{bb'} + R_S,$$
$$L_1 = \frac{C_\pi r_\pi (r_{bb'} + R_S)}{h_{FE}} = \frac{r_{bb'} + R_S}{2\pi f_T}. \quad (1)$$

The appearance of the inductor, L_1, might at first be puzzling. You can interpret L_1 as accounting for the transistor's h_{FE} rolloff of −6 dB per octave. As its h_{FE} decreases, the output impedance of the emitter follower increases. This behavior is, after all, that of an inductor.

Given that the output impedance of an emitter follower can appear to be inductive, and given that the load is

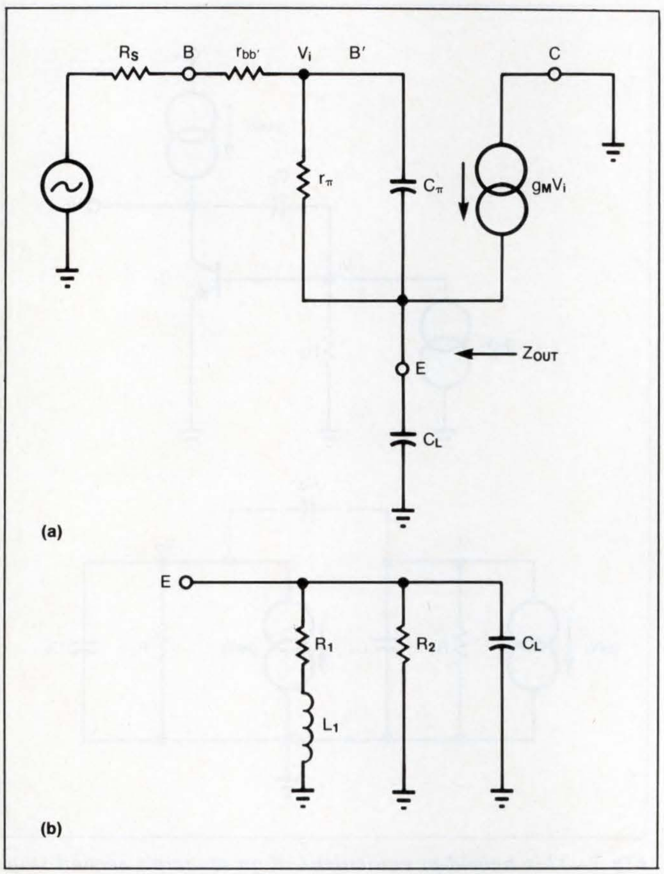

***Fig 3—Op-amp emitter followers tend to oscillate into** capacitive loads. **Fig 3a** illustrates the hybrid-pi model of an emitter follower; **Fig 3b** is the equivalent circuit modeled from the emitter's perspective. L_l accounts for the transistor's h_{FE} rolloff.*

capacitive, a tuned parallel-resonant circuit is possible; consequently, the follower can oscillate. For example, the EL2006 uses transistors whose nominal f_T is 400 MHz, and the emitter-follower stage sees a cumulative source resistance (including $r_{BB'}$) of about 15Ω. **Eq 1** predicts a value for L_l of about 6 nH (plus 10 nH for lead and wire-bond inductance). The resonant frequency is

$$f = \frac{1}{2\pi\sqrt{(L_l + L_{STRAY})\,(C_L)}}.$$

A 50-pF load yields oscillation in the neighborhood of 180 MHz.

Input capacitance can induce phase shift

Further, consider the effects of capacitance at the op amp's input. In conjunction with the feedback network, it can form a lowpass filter and induce phase shift (**Fig 1**). C_{STRAY} at the op amp's inverting input comprises the input capacitance of the device in parallel with any stray capacitance on the board. The phase lag and corner frequency are

$$\phi = \arctan\frac{f_U}{f_C}, \qquad (2)$$

where

$$f_C = \frac{1}{2\pi\, R_{EQUIV}\, C_{STRAY}}, \qquad (3)$$
$$R_{EQUIV} = R_F \parallel R_2.$$

For **Fig 1**'s circuit and the EL2006's unity-gain frequency, the erosion in phase margin consumes virtually all of the device's 32° of margin. Therefore, for wideband op amps, you must keep R_{EQUIV} (**Eq 3**) relatively low. Specifically, for the EL2006, the R_{EQUIV} must be below 1 kΩ. Alternatively, you can place a small capacitor in parallel with R_F. The capacitor's value is

$$C = \frac{(R_2)\,(C_{STRAY})}{R_F}.$$

In the real world, this formula predicts a value that overcompensates the loop. An empirical approach employs the old TV repairman's trick of using a "gimmick." A gimmick is two lengths of wire (22 or 24 AWG works nicely) cut to about 6 in. and loosely twisted together. The gimmick forms a very small, low-inductance capacitor. You first solder the gimmick in parallel with R_F (C_F in **Fig 1**) and monitor an oscilloscope for optimum pulse response while incrementally trimming the gimmick. Once you obtain the optimum response, you carefully unsolder the gimmick and measure its value on a capacitance bridge. One word of caution: The required capacitance may change slightly between your breadboard and the final pc board.

Pole-splitting compensation

No matter how carefully you apply an op amp, you could run afoul of problems arising from the op amp's internal circuitry. One potential problem area is the common technique of pole-splitting compensation. Op-amp designers incorporate pole-splitting compensation for a number of reasons. One obvious reason is that alternate compensation schemes usually require large capacitors, and capacitors take up a lot of space on the IC. However, the primary reason is that, in general, pole-splitting compensation is one of the best ways to

External circuit elements are not the only reason for op-amp instability—an op amp's output stage can have inherent problems.

compensate for (and preserve the slew rate of) an op amp with multiple poles in its transfer characteristic.

Pole-splitting compensation allows IC designers to take advantage of the Miller effect. Because of the voltage gain of the second stage, a small capacitor achieves unity-gain stability and preserves the op amp's slew rate. Unfortunately, the technique is fraught with danger, particularly when applied in wideband amplifiers.

On the surface, pole splitting is simplicity itself. **Fig 4** shows the equivalent circuit of an op amp having a differential-input stage with modest voltage gain, a second stage with large voltage gain, and an output stage designed to furnish current gain to drive the load. In **Fig 4,** the second and third stage are combined and the differential-input stage is replaced by an equivalent voltage-controlled current source. Furthermore, the second stage is an integrator by virtue of capacitor C_C. The model's unity-gain crossover frequency is

$$V_{OUT}(s) = \frac{(g_M)\,(V_{IN}(s))}{sC_C}, \qquad (4)$$

$$f_U = \frac{g_M}{(2\pi)\,(C_C)}$$

where g_M is the amp's transconductance and C_C is the value of the integrating capacitor.

Eq 4 can predict the unity-gain frequency for most amplifiers that use split-pole compensation. Occasionally the equation needs to be modified to suit a given circuit topology.

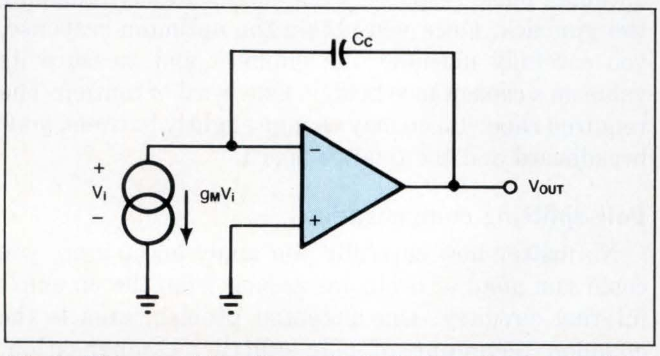

***Fig 4—This circuit is the equivalent of an op amp** having a differential-input stage with modest voltage gain, a second stage with large voltage gain, and an output stage designed to furnish current gain to drive the load. The second and third stage are combined, and the differential-input stage is replaced by an equivalent voltage-controlled current source. The second stage is the heart of the pole-splitting technique, because it's an integrator by virtue of capacitor C_C.*

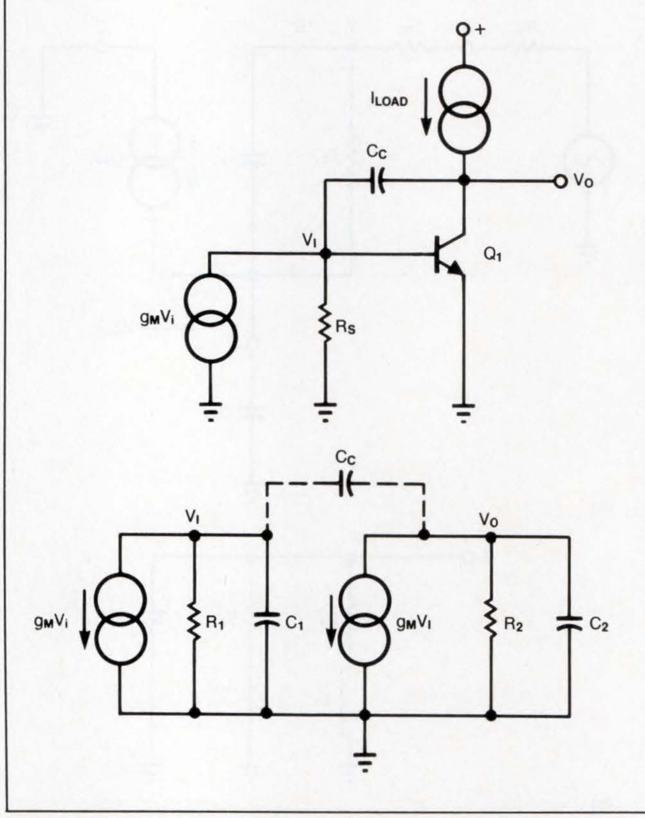

***Fig 5—This hybrid-pi equivalent of an op-amp's second** stage graphically illustrates why the stage has two poles: One arises from the input's RC elements, and one arises from the output's RC elements.*

Eq 4 predicts that **Fig 4**'s circuit will be a well-behaved, trouble-free amplifier with a response of 20 dB per decade. But the amplifier will be well behaved only if the second stage acts as an integrator. To understand how this compensation scheme can fail, you need to delve into the details of a typical circuit used in the second stage of the op amp. **Fig 5** depicts such a circuit and its hybrid-pi equivalent. You can see from the diagram that the second stage has two poles: P_1 is the result of input resistances and capacitances and P_2 is the result of output resistances and capacitances. The poles are:

$$P_1 = \frac{1}{R_1C_1},\ P_2 = \frac{1}{R_2C_2},$$

where

$$R_1 = R_S \parallel R_\pi,\ R_2 = R_{OUT},\ C_1 = C_\pi,$$
$$\text{and } C_2 = C_{OUT}.$$

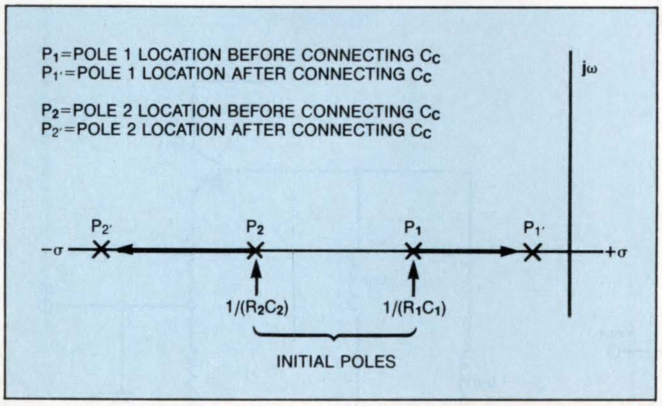

***Fig 6—The pole-splitting technique** derives its name from the effect that connecting a compensation capacitor (C_C) has on the two poles of **Fig 5**. The capacitor moves the dominant pole toward the origin while simultaneously moving the other pole further away. The net effect of the split is to disable the nondominant pole, leaving only a single pole in effect.*

Analysis of **Fig 5**, including the effects of C_C, yields the equations

$$P_1 = \frac{1}{R_1(C_1 + C_C) + R_2(C_2 + C_C) = g_M R_1 R_2 C_C} \quad \textbf{(5)}$$

$$= \frac{1}{g_M R_1 R_2 C_C}$$

and

$$P_2 = \frac{(g_M)\,(C_C)}{C_1C_2 + C_C(C_1 + C_2)}. \quad \textbf{(6)}$$

Examining **Eqs 5** and **6** gives you an insight into the circuit's behavior. First, observe that as either g_M or C_C increases, the input pole, P_1, moves in toward the origin. Second, the nondominant pole, P_2, moves away from the origin as a function of g_M and C_C **(Fig 6)**. In other words, the poles split apart. P_2's influence moves above the maximum frequency range of the op amp, leaving P_1 behind to create, in effect, an amplifier with a single dominant pole. The stage becomes an integrator, because the secondary pole has been pushed to a very high frequency (or "broadbanded"), where its phase shift is irrelevant.

Inevitably, however, there are other poles in the gain path that the simple model of **Fig 5** doesn't account for. Splitting out the nondominant pole enables these additional poles, and they contribute to phase shift through the stage—hence the op amp's instability. In short, the stage is no longer a simple integrator.

Fig 7 illustrates a typical op-amp gain stage. It's a simplification of both the 741's first stage and the second stage of the ELH0032. Note that two signal paths to the output exist: a direct path through Q_4, and an indirect path through Q_3 and the current-mirror transistors Q_{16} and Q_{10}. The indirect path introduces a delay, and its voltage gain is about half that of the direct path. These factors introduce additional poles.

Output stage becomes inductive too

Finally, instability can arise from problems in the output stage. The circuit shown in **Fig 8** employs typical Class AB biasing of the output stage's emitter followers, and is, in fact, the ELH0032's circuit. It is commonly referred to as a "2ϕ maker" **(Eq 6)**. Assuming that 1 mA flows through R_5 and R_6, the emitter current of Q_7 will be about 4 mA. In effect, the circuit forces a voltage equal to $1.9\times V_{BE}$ across the base-emitter junctions of Q_{11} and Q_{12}, setting their emitter currents at about 1.3 mA. From a dc point of view, this circuit acts like a battery that's connected from the base of Q_{11} to the base of Q_{12}.

The ELH0032's output impedance (R_O) at dc is about

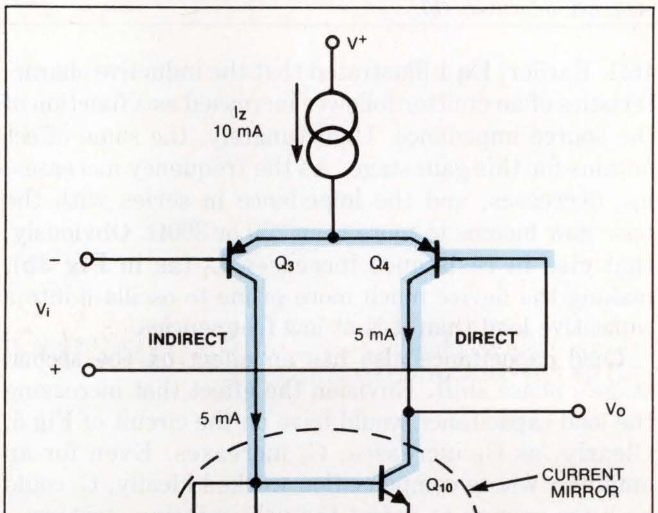

***Fig 7—This typical op-amp gain stage has two signal** paths to the output: a direct path through Q_4; and an indirect path through Q_3 and current-mirror transistors Q_{16} and Q_{10}. The indirect path introduces a delay, and its voltage gain is about half that of the direct path. These factors introduce additional poles that corrupt the pole-splitting scheme.*

Because an emitter follower's output impedance can be inductive, and its load is capacitive, the follower can oscillate.

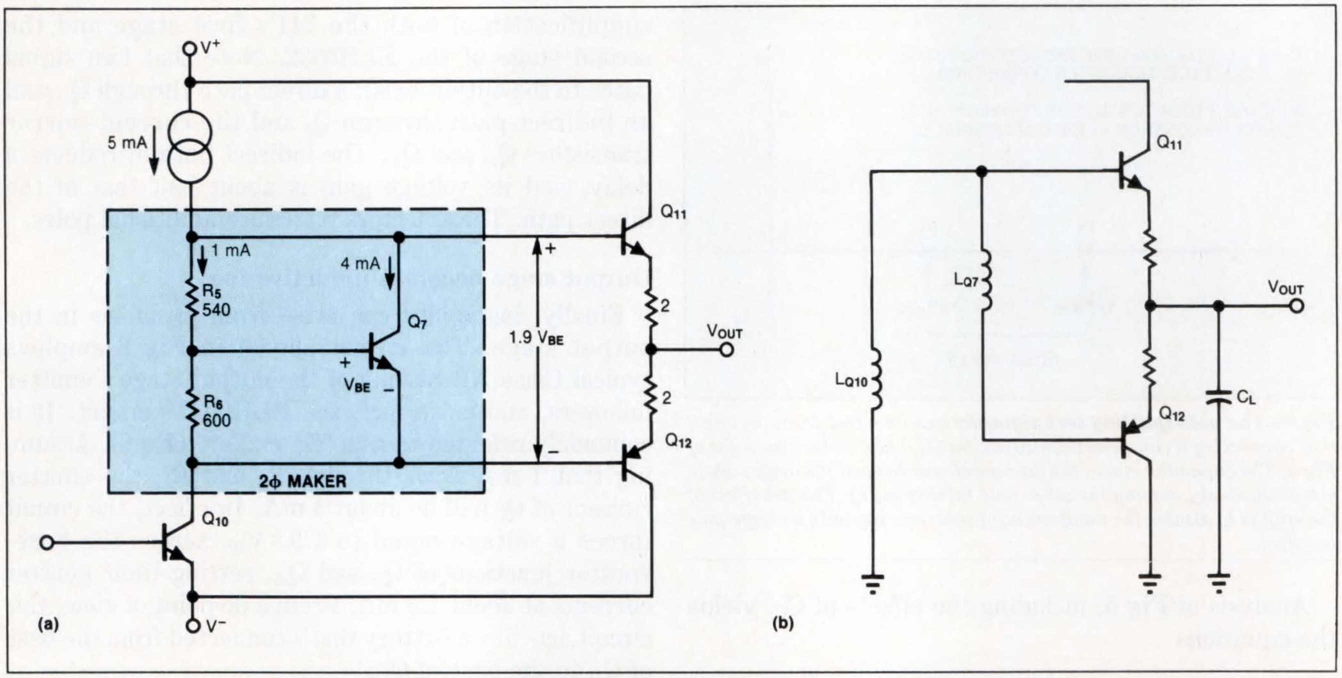

***Fig 8—The impedance of the biasing network (a)** (called a "2φ maker") for output transistors in an op amp's gain stage can cause the stage's output impedance to vary from 16Ω at dc to 200 or 300Ω at high frequencies. Increasing the compensation capacitor, C_C, makes the output stage act inductively **(b)**.*

16Ω. Earlier, **Eq 1** illustrated that the inductive characteristics of an emitter follower increased as a function of the source impedance. Unfortunately, the same effect obtains for this gain stage. As the frequency increases, h_{FE} decreases, and the impedance in series with the base now blooms to more than 200 or 300Ω. Obviously, that rise in resistance increases L_1 (as in **Fig 3b**), making the device much more prone to oscillate into a capacitive load than it is at low frequencies.

Load capacitance also has an effect on the second stage's phase shift. Envision the effect that increasing the load capacitance would have on the circuit of **Fig 5**. Clearly, as C_L increases, C_2 increases. Even for an amplifier whose compensation worked ideally, C_2 could be large enough to defeat the pole-splitting strategy.

For example, if you split

$$\frac{1}{R_2C_2}$$

out to the vicinity of f_U, the additional phase shift that would occur could make the amplifier unstable. What makes this output-capacitance problem particularly troublesome is that the amplifier depends on the output stage to isolate the load from the second stage. This isolation scheme is certainly effective at dc, where the full h_{FE} of the emitter followers comes into play. But at higher frequencies, when the isolation is most critical, the output stage doesn't help. As a consequence, C_L is essentially transferred to the second stage directly, increasing C_2 **(Fig 5)**, and jeopardizing the ability of C_C to broadband the second stage.

Finally, in the simple model of **Fig 5**, the major effect of making C_C larger is simply a corresponding decrease in f_U. In practice, the requirements for unity-gain stability dictate both a minimum and a maximum value for C_C; a real-world designer can't increase C_C infinitely. To understand these limits intuitively, imagine that C_C of **Fig 5** increases to an arbitrarily large value. At a given frequency, C_C shorts out transistor Q_1, and the stage becomes noninverting. That condition is positive feedback, which is obviously not what your circuit needs.

A very complex oscillation can result when the compensation capacitor is made arbitrarily large and it interacts with the output-stage biasing. Referring to **Fig 8a**, as C_C increases, Q_{10}'s collector-base junction becomes a short as in the case above. At a given high frequency, Q_{10} can be modeled as an inductor, as shown in **Fig 3b**. Furthermore, the class-AB bias network also behaves like an inductor. The equivalent circuit of **Fig 8b** is the net result. The emitter follower's penchant for

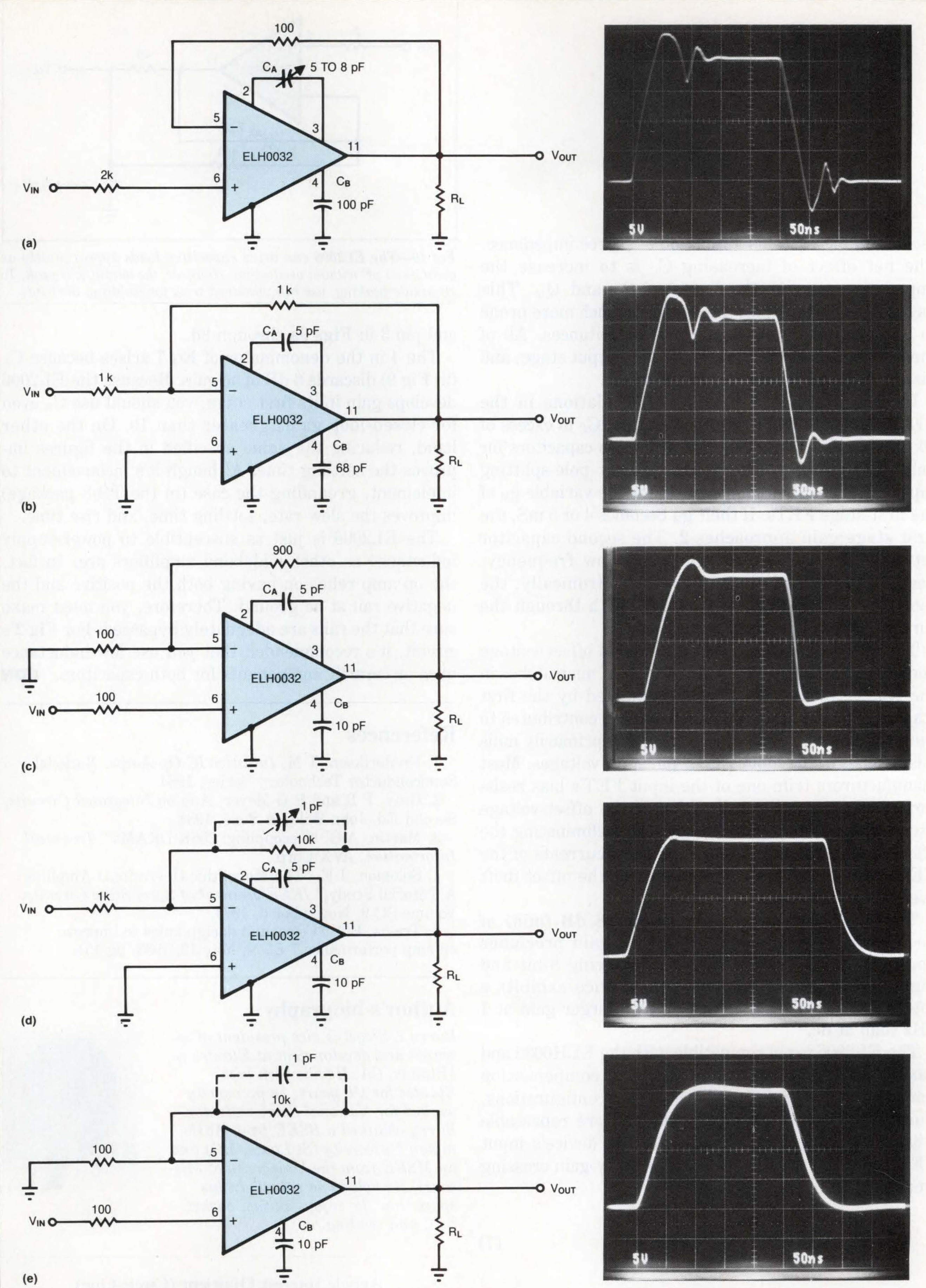

***Fig 9—These compensation schemes will produce** stable amplifiers under all normal operating conditions.*

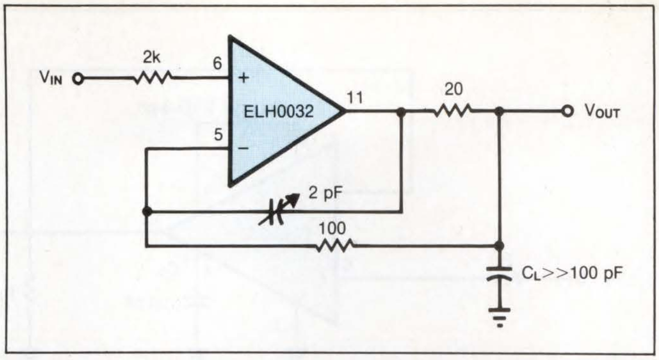

Fig 10—The EL2006 can drive capacitive loads approximately as great as 25 pF without oscillating. However, the output will peak. To eliminate peaking, use this standard trick for isolating the load.

oscillation increases as a function of source impedance. The net effect of increasing C_C is to increase the impedance seen at the bases of Q_{11} and Q_{12}. This increase, in turn, makes the amplifier much more prone to oscillate—even into small load capacitances. All of these effects result in gyration of the output stage, and bizarre oscillations are the consequence.

In the case of the ELH0032, oscillations in the 200-MHz region will result for values of C_C in excess of 20 pF. Further, the device requires two capacitors for unity-gain stability. One is the familiar pole-splitting capacitor. The other compensates for the variable g_M of the first-stage FETs. If their g_M becomes 4 or 5 mS, the first stage gain approaches 2. The second capacitor jettisons the gain at an arbitrarily low frequency, keeping the device unity-gain stable. Ironically, the same capacitor enables the indirect path through the current mirror discussed earlier.

The ELH0032 doesn't exhibit minimal offset voltage and offset-voltage drift partly because of mismatches in the second stage that are not attenuated by the first stage. Also, the devices' laser trimming contributes to the offset-voltage drift. Laser trimming primarily nulls mismatches in the input FETs' pinch-off voltages. Most manufacturers trim one of the input FET's bias resistors, depending on the direction of the offset-voltage skew. This trimming does a fine job of eliminating the offset, but it also mismatches the drain currents of the FETs, which action, in turn, increases the offset drift over temperature.

The ELH0032 develops a feeble 48 dB (min) of open-loop gain. Obviously, this low gain precludes applying the device in systems requiring 8-bit and higher accuracy. In addition, the device exhibits a thermal tail that manifests itself as a larger gain at 1 kHz than at dc.

The EL2006 is pin compatible with the ELH0032 and has an open-loop gain of 86 dB. The compensation schemes recommended for various gain configurations, shown in **Fig 9**, work every time and are repeatable within the variations of the g_M of the device's input FETs. You can predict the device's unity-gain crossing frequency from the equation

$$f_U = \frac{g_M}{4\pi(C_A + 1\text{ pF})}, \qquad (7)$$

where g_M is the transconductance of the input JFETs (4 mS) and C_A is the capacitor connected between pin 2 and pin 3 in **Figs 9a** through **9d.**

The 4 in the denominator of **Eq 7** arises because C_B (in **Fig 9**) discards 6 dB of ac gain. Because the EL2006 develops gain in its first stage, you should use C_B even for closed-loop gains greater than 10. On the other hand, reducing the value specified in the figures improves the settling time. Although it's inconvenient to implement, grounding the case (in the TO-8 package) improves the slew rate, settling time, and rise time.

The EL2006 is just as susceptible to power-supply inductance as other wideband amplifiers are. In fact, the op amp relies on having both the positive and the negative rail at ac ground. Therefore, you must make sure that the rails are adequately bypassed. For **Fig 2's** circuit, it's recommended that you use low-inductance mica or ceramic components for both capacitors. **EDN**

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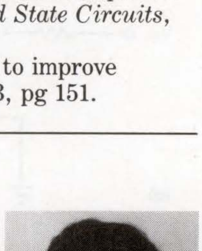
Author's biography



Barry L Siegel is vice president of research and development at Elantec in Milpitas, CA. He has been with Elantec for 4½ years; he previously worked for National Semiconductor. Barry obtained a BSEE from Washington University (St Louis, MO) and an MSEE from the University of Missouri. He holds one patent. In his spare time, he enjoys skiing, basketball, and reading.

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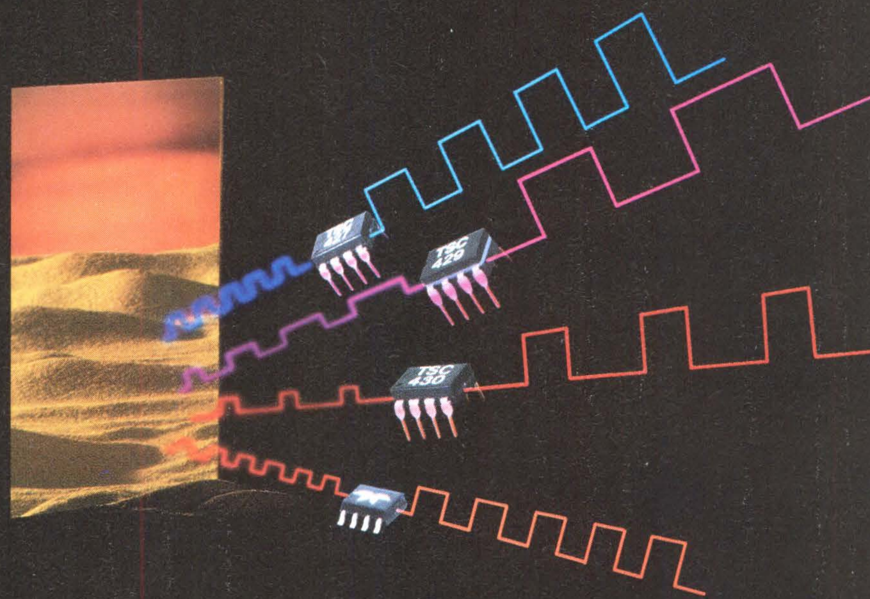

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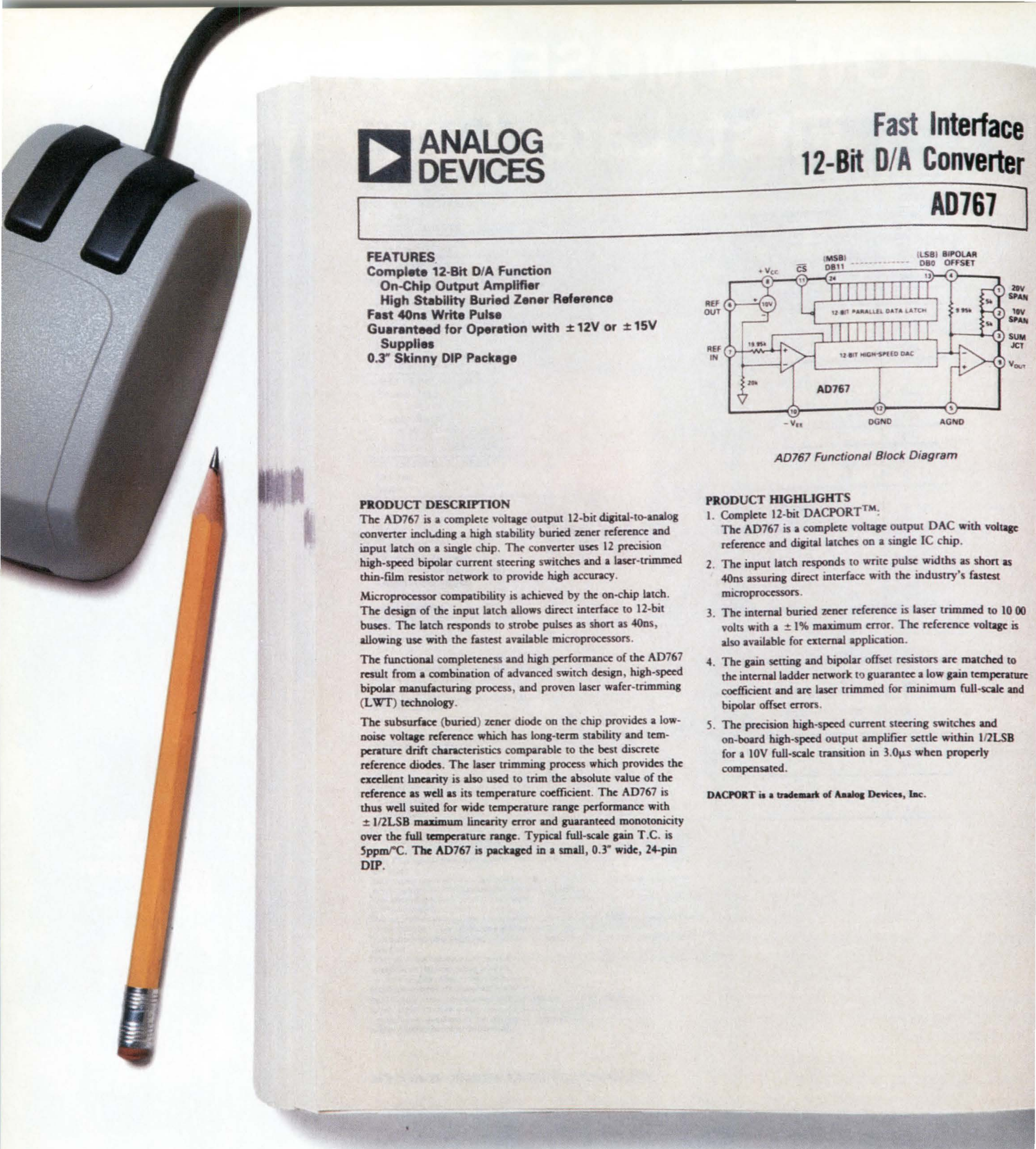

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AD767 Functional Block Diagram

PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried zener reference and input latch on a single chip. The converter uses 12 precision high-speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high-speed bipolar manufacturing process, and proven laser wafer-trimming (LWT) technology.

The subsurface (buried) zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ± 1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5ppm/°C. The AD767 is packaged in a small, 0.3" wide, 24-pin DIP.

PRODUCT HIGHLIGHTS

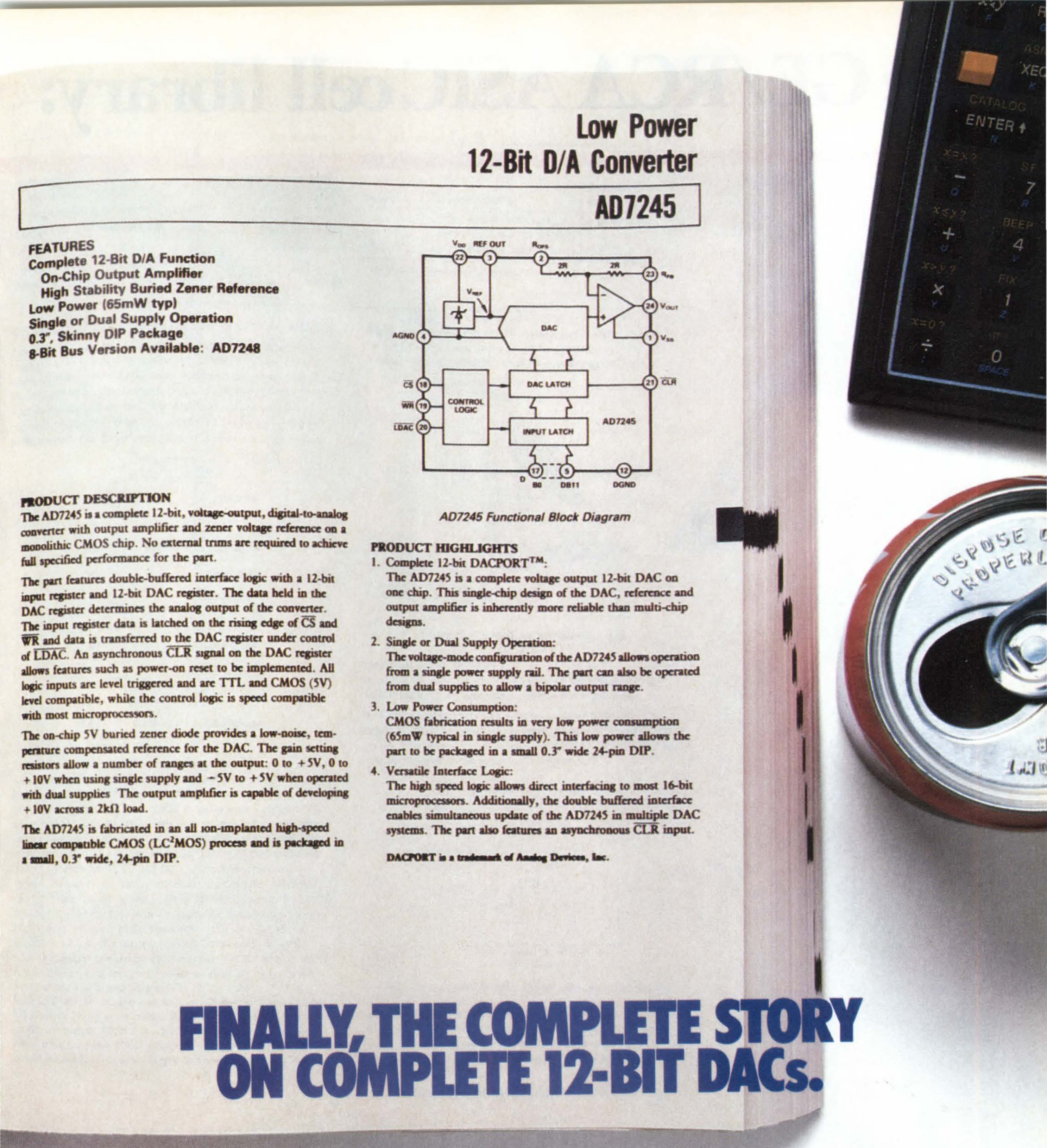
1. Complete 12-bit DACPORT™:
   The AD767 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The input latch responds to write pulse widths as short as 40ns assuring direct interface with the industry's fastest microprocessors.
3. The internal buried zener reference is laser trimmed to 10.00 volts with a ± 1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full-scale and bipolar offset errors.
5. The precision high-speed current steering switches and on-board high-speed output amplifier settle within 1/2LSB for a 10V full-scale transition in 3.0μs when properly compensated.

DACPORT is a trademark of Analog Devices, Inc.

Bringing complete 12-bit DAC functionality and performance to your designs no longer requires having to deal with all the problems associated with external components. Instead, it simply requires specifying our new AD767 or AD7245.

Both the AD767 and AD7245 feature an on-chip stable buried Zener reference, output amplifier and microprocessor interface logic. And these complete functions come packed into skinny 0.3" DIPs. All this means you no longer have to deal with error budgets, product characterizations, or space constraints related to external components.

If digital interface speed is what you're after, the AD767 responds to pulse widths as short as 40ns, allowing it to be used with today's fastest processors. On the other hand, if low power dissipation is critical to your application, the LC²MOS AD7245 consumes only 65mW. There's also


Low Power
12-Bit D/A Converter
AD7245
FEATURES
Complete 12-Bit D/A Function
On-Chip Output Amplifier
High Stability Buried Zener Reference
Low Power (65mW typ)
Single or Dual Supply Operation
0.3", Skinny DIP Package
8-Bit Bus Version Available: AD7248
VDD REF OUT ROFS
2R 2R
VREF
DAC
AGND
VOUT
VSS
CS
WR
LDAC
CONTROL LOGIC
DAC LATCH
INPUT LATCH
CLR
AD7245
DB0 DB11 DGND
AD7245 Functional Block Diagram
PRODUCT DESCRIPTION
The AD7245 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.
The part features double-buffered interface logic with a 12-bit input register and 12-bit DAC register. The data held in the DAC register determines the analog output of the converter. The input register data is latched on the rising edge of CS and WR and data is transferred to the DAC register under control of LDAC. An asynchronous CLR signal on the DAC register allows features such as power-on reset to be implemented. All logic inputs are level triggered and are TTL and CMOS (5V) level compatible, while the control logic is speed compatible with most microprocessors.
The on-chip 5V buried zener diode provides a low-noise, temperature compensated reference for the DAC. The gain setting resistors allow a number of ranges at the output: 0 to +5V, 0 to +10V when using single supply and −5V to +5V when operated with dual supplies. The output amplifier is capable of developing +10V across a 2kΩ load.
The AD7245 is fabricated in an all ion-implanted high-speed linear compatible CMOS (LC²MOS) process and is packaged in a small, 0.3" wide, 24-pin DIP.
PRODUCT HIGHLIGHTS
1. Complete 12-bit DACPORT™:
The AD7245 is a complete voltage output 12-bit DAC on one chip. This single-chip design of the DAC, reference and output amplifier is inherently more reliable than multi-chip designs.
2. Single or Dual Supply Operation:
The voltage-mode configuration of the AD7245 allows operation from a single power supply rail. The part can also be operated from dual supplies to allow a bipolar output range.
3. Low Power Consumption:
CMOS fabrication results in very low power consumption (65mW typical in single supply). This low power allows the part to be packaged in a small 0.3" wide 24-pin DIP.
4. Versatile Interface Logic:
The high speed logic allows direct interfacing to most 16-bit microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7245 in multiple DAC systems. The part also features an asynchronous CLR input.
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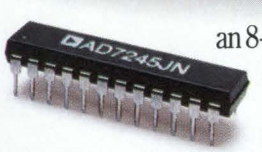
AD7245JN

The GE/RCA ASIC cell library:

EDITED BY TARLTON FLEMING

Serial-data system uses 4-wire distribution

James C Smith
NASA, Greenbelt, MD

A common 4-wire communications bus lets you send 12-bit serial data to any one of 16 (or fewer) receiving stations **(Fig 1)**. Each 16-bit data packet consists of a 4-bit address followed by the 12-bit data word. All stations receive the data packet, but only the selected station generates a strobe that updates that station's data latch.

You must provide the Data, Clock, and Sync signals as shown in the timing diagram. Timing for the Sync signal is critical—to avoid generating false address strobes as previous data shifts through the address decoder IC_3, the Sync signal must go low just before the data packet begins. Then, proper strobe generation requires that it go high at the mid-point of the last (sixteenth) clock pulse.

Data shifts through the serial shift registers IC_1 and IC_2 on the Clock signal's leading edge. The coincidence of the Clock, Sync, and Address-Select signals allows the NAND gate, IC_8, to generate a data strobe for latches IC_5-IC_7. Note that IC_4 and the thumbwheel switch, S_1, let you change the station address; in a simpler, dedicated system, you would connect the desired IC_3 output directly to IC_8. Remote stations may require the optional optoisolators, Q_1-Q_3. EDN

To Vote For This Design, Circle No 747

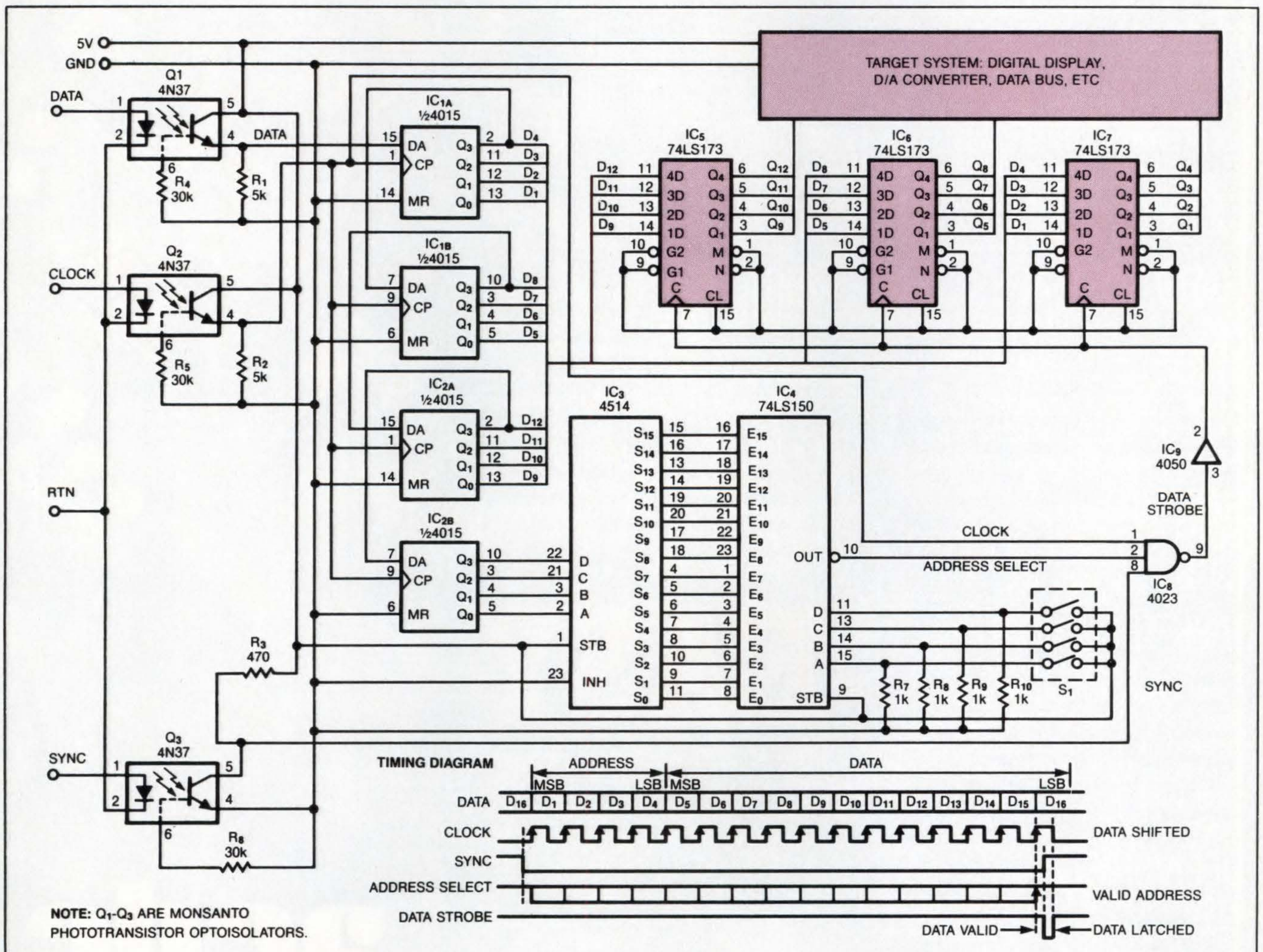

***Fig 1—This circuit receives a 16-bit serial data word,** decodes the 4-bit address and, if appropriate, stores the subsequent 12-bit data word in latches IC_5-IC_7.*

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60	+5V/5.0A	+12V/2.5A	−12V/0.5A		RBT 61	PCB
70	+5V/6.0A	+12V/2.5A	−12V/0.7A	−5V/0.7A	RBQ 71	PCB
135	+5V/15A	+12V/4.0A	−12V/0.7A	−5V/0.7A	RBQ 131	L BRACKET
135	+5V/15A	+15V/3.2A	−15V/0.7A	−5V/0.7A	RBQ 132	
135	+5V/15A	+12V/3.0A	−12V/0.7A	+24V/1.5A	RBQ 133	
135	+5V/15A	+15V/2.4A	−15V/0.7A	+24V/1.5A	RBQ 134	
175	+5V/20A	+12 or 15V/4A	−12 or 15V/3A	−5V/1.0A	RBQ 171	U CHANNEL
175	+5V/20A	+12 or 15V/4A	−12 or 15V/3A	+24V/1.5A	RBQ 173	
220	+5V/25A	+12 or 15V/4A	−12 or 15V/3A	−5V/1.5A	RBQ 221	U CHANNEL
220	+5V/25A	+12 or 15V/4A	−12 or 15V/3A	+24V/3.0A	RBQ 223	

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CIRCLE NO 124

Power-fail circuit gives prompt response

Neal E Pritchard
Emerson Electric Co, Oceanside, CA

Adding power-fail circuitry to a flyback-converter power supply presents a problem. A flyback converter's control circuit is usually located in the input section and referenced to the ac line **(Fig 1a)**. Any circuitry you want to add there must have proper spacing from the chassis and the output section and must include some form of isolation for safety reasons. The additional cost and complexity of this approach is contrary to the intent of using a flyback converter in the first place.

To eliminate the isolation requirement, you can locate the power-fail circuit in the output section, perhaps in the form of an undervoltage detector for E_O. Unfortunately, in this configuration, the output capacitor's storage effect delays the alarm by approximately

$$\frac{dE_O}{dt} = \frac{I}{C_1}.$$

To provide an alarm signal 1 msec before an E_O drop of 0.1V, for example, requires a C_1 value of 10k µF per ampere of load current (I). Such a large capacitance is impractical for most power-supply designs, and therefore the circuit must somehow detect ac-line loss before E_O begins to drop.

Referring to **Fig 1b**, you can see that the voltage E_S reflects the V_{IN} that occurs while the transistor is conducting:

$$E_S = -V_{IN}\left(\frac{N_S}{N_P}\right).$$

You can detect a loss of power by monitoring E_S as shown in **Fig 2**. By rectifying and filtering E_S, the D_1/C_1 network produces a negative voltage proportional to V_{IN}. IC_{1A} compares a fraction of this voltage with a fixed voltage established by the 2.5V shunt regulator IC_2. D_2 and C_2 then delay the low-to-high transitions that IC_{1A} produces, which ensures that the power-fail signal (V_{OUT}) remains low during power-up. The IC_{1B} comparator's open-collector output then goes high when C_2 charges to 2.5V. (A larger-valued C_2 increases the delay, but too large a value will cause a noisy signal transition.)

The power supply's storage time depends on its circuit design, the ac-line voltage, and the load current, but the warning time (defined as the time interval between the power-loss alarm and a 5% drop in E_O) depends primarily on C_1. Reducing the value of C_1 increases the warning time, but the upper limit must be less than the storage time. **Fig 2** provides an approximate 5-msec warning time and a 10-msec turn-on delay when operating with a typical 5V flyback converter.

EDN

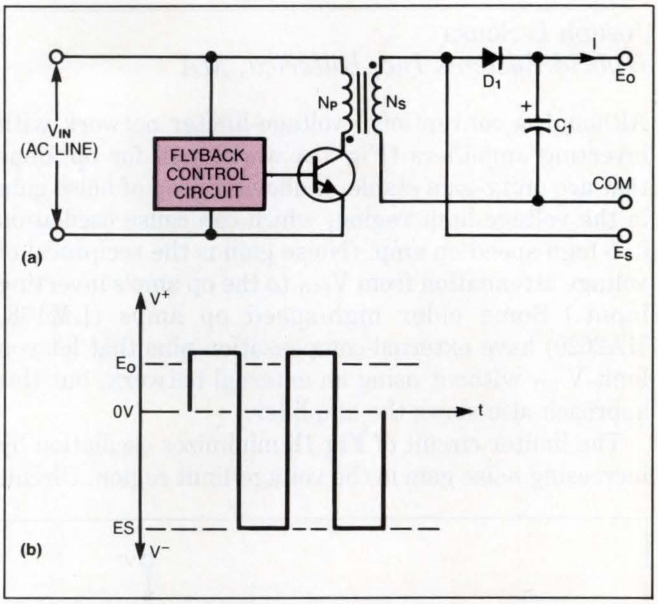


***Fig 1—This typical flyback converter (a)** produces positive pulses which, after filtering, produce the output voltage E_O. The normally unused negative pulses **(b)** are proportional to V_{IN}.*

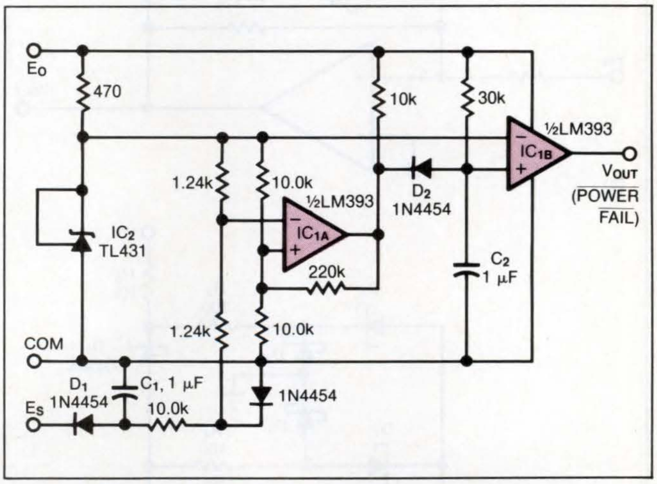


***Fig 2—When connected to the Fig 1 power supply,** this circuit senses a loss of V_{IN} by monitoring the voltage E_S. (A loss of power causes V_{OUT} to go low.)*

To Vote For This Design, Circle No 750

Voltage limiter restrains fast op amps

Joseph L Sousa
Hybrid Systems Inc, Billerica, MA

Although a conventional voltage-limiter network with inverting amplifiers **(Fig 1a)** works well for op amps that are unity-gain stable, it allows a drop of noise gain in the voltage-limit region, which can cause oscillation in a high-speed op amp. (Noise gain is the reciprocal of voltage attenuation from V_{OUT} to the op amp's inverting input.) Some older high-speed op amps (LM108, HA2620) have external-compensation pins that let you limit V_{OUT} without using an external network, but this approach also slows the amplifier.

The limiter circuit of **Fig 1b** minimizes oscillation by increasing noise gain in the voltage-limit region. Circuit operation is fast because the op amp does not require slew-rate-limiting compensation capacitors, nor does it require a resistor from the summing junction to ground, which would permanently increase noise gain. (Note that most fast op amps will oscillate if the noise gain is too low; they are most stable (by design) for high values of noise gain.)

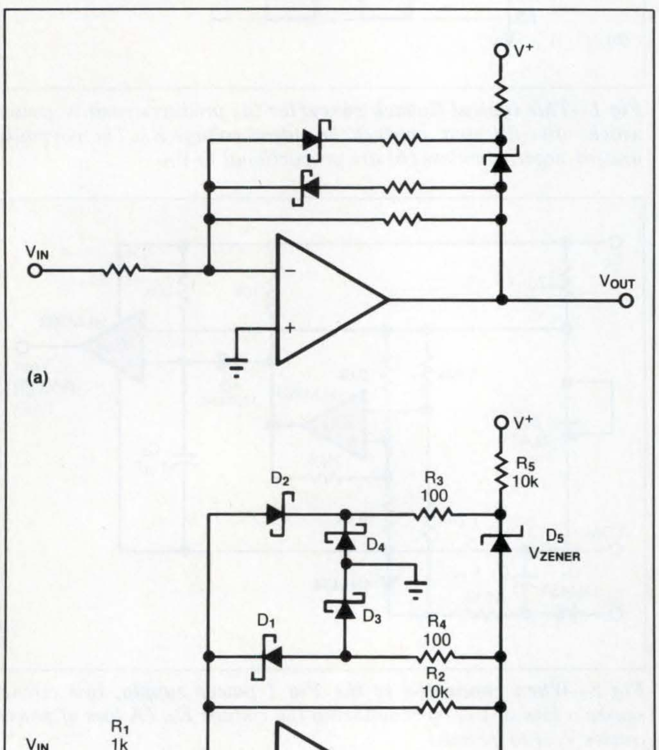


Fig 1—The conventional network for limiting the output-voltage swing of an op amp (a) can allow oscillation in a high-speed op amp. The circuit of b provides almost oscillation-free limiting for fast op amps by maintaining high noise gain in the voltage-limit regions.

The voltage dividers, R_3/D_4 and R_4/D_3, help produce an increasing noise gain in the voltage-limit regions. Diode D_3 begins to turn on, for instance, if V_{OUT} exceeds the positive limit (0.4V). The resulting current in D_3 curbs oscillation by decreasing the diode's dynamic resistance, which increases noise gain for the amplifier. (Overdriving the amplifier will result in higher diode current, producing even higher noise gain in the limit region.) Diode D_4 produces a similar clamping effect by turning on as V_{OUT} approaches the negative limit ($-0.4V-V_{ZENER}$). Well-matched diodes produce similar voltages and currents, allowing their dynamic resistances to track one another. When choosing values for R_3 and R_4, be sure to account for the op amp's output impedance in series with each resistor (30Ω for an HA2539, for example).

The **Fig 1b** circuit's lowest noise gain occurs in the valley region **(Fig 2)**, where the R_3/D_4 and R_4/D_3 dividers have not yet counteracted the noise-gain-reduction effects of diodes D_2 and D_1. Low-level oscillation (less than 0.5V p-p) may occur in the valley region (-40 mV$>V_{IN}>-0.5$V), but the high noise gain on either side of the valley marks the boundary of the amplitude of such oscillations.

You can eliminate oscillation by raising the floor of

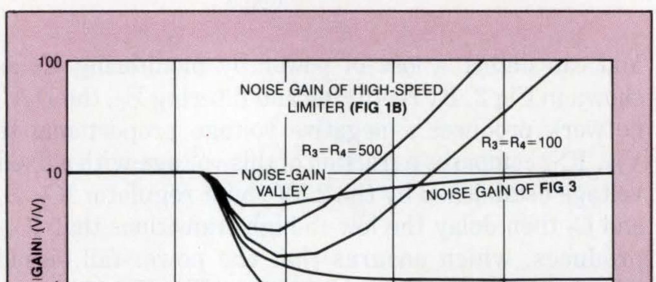
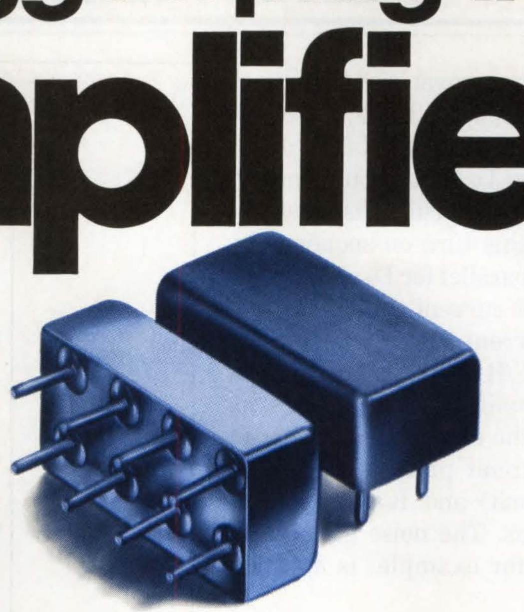


Fig 2—The higher noise gain of the high-speed-limiter circuit of Fig 1b accounts for its better stability. This circuit can oscillate only for the narrow range of V_{IN} corresponding to the noise-gain valley.

rugged plug-in amplifiers



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MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95

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CIRCLE NO 125

C118 REV. B

the noise-gain valley in one of two ways: Either increase the values of R_3 and R_4 or, as shown in **Fig 3,** return D_3 and D_4 to low-level bias voltages instead of to ground. These connections cause D_3 and D_4 to turn on before D_1 and D_2, which alters the noise-gain curve as shown in **Fig 2.** (You can also achieve this turn-on sequence by substituting several diodes in parallel for D_3 and for D_4.)

Resistors R_5 and R_6 limit the current through D_3 and D_4 and indirectly limit the current through D_1 and D_2. The values of the ratios of R_3/R_5 and R_4/R_6, however, should not be less than the amplifier's rated noise gain. Because these resistors limit the diode impedance of D_3 or D_4 at high current, the circuit produces a voltage transfer of R_4/R_1 (positive limit) and R_3/R_1 (negative limit) in the hard-limit regions. The noise gain in the negative-hard-limit region, for example, is approximately

$$\frac{V_{OUT}}{V_{INV}}=\frac{R_4+R_{D3}+R_6}{R_{D3}+R_6},$$

where V_{INV} is the amplifier's inverting-input voltage (R_{D3} is the dynamic resistance of D_3.) A more-complicated expression describes noise gain below the hard-limit region (as shown by the curves of **Fig 2**):

$$\frac{V_{OUT}}{V_{INV}}=\left[\frac{R_1\|(R_{D1}+(R_{D3}+R_6)\|R_4)}{R_2+R_1\|(R_{D1}+(R_{D3}+R_6)\|R_4}+\frac{(R_{D3}+R_6)\|(R_{D1}+R_1\|R_2)}{R_4+(R_{D3}+R_6)\|(R_{D1}+R_1\|R_2)}\left(\frac{R_1\|R_2}{R_{D1}+R_1\|R_2}\right)\right]^{-1}.$$

The dominant pole of some high-speed amplifiers (HA2539 and HA2540) is sensitive to the source impedance you apply at the amplifier inputs. For these, you should add series input resistors according to directions in the data sheet.

The Schottky diodes recommended for this circuit exhibit about 1 pF of capacitance when reverse biased. You may need to cancel this capacitance by connecting approximately 1 pF between the amplifier's summing junction and ground. (1N914 diodes are satisfactory in some applications, but they exhibit about 5 pF when reverse biased.) **EDN**

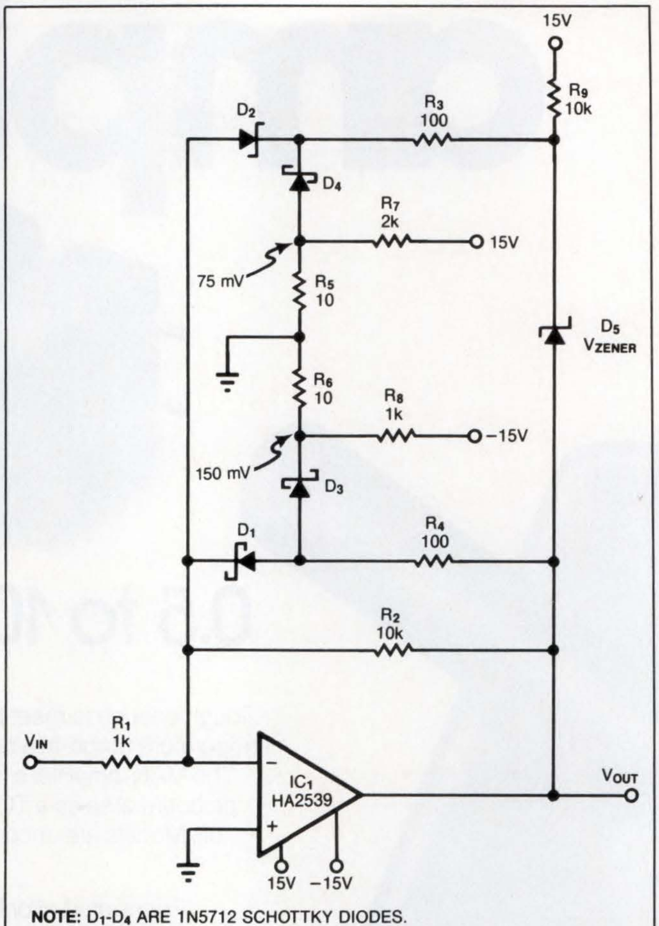

Fig 3—By connecting D_3 and D_4 to small bias voltages instead of to ground, you can eliminate oscillation in the noise-gain valley by raising the valley's floor.

To Vote For This Design, Circle No 746

Adapt a 68020 emulator to the 68030 μP

Mike Ruhland
University of Chicago, Chicago, IL

The **Fig 1** adapter circuit lets you use a 68020 in-circuit emulator (ICE) for developing a target system based on the 68030 μP. You eliminate the cost of a new ICE, of course, and the retrofit will not damage or modify your existing 68020 ICE. Simply plug the adapter board's 68030 header into the 68030 socket, and plug the 68020 emulator into the adapter's 68020 socket.

Logic on the adapter board supports the 68030's synchronous bus interface, which uses $\overline{\text{STERM}}$ instead

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Speed	10-25 MHz	8-12.5 MHz	10 MHz
Memory Support	16 Mb Physical Paged	1 Mb Physical Segmented	16 Mb Physical 8 or 128 Segments
16-bit Registers	12 General	8 General	15 Dedicated
Instruction Pre-fetch	256-Byte Assoc. Cache; Burst Mode	6-Byte Queue	None
Multiprocessor Support	Local or Global	Local only	Local only
Wait Logic	Programmable	Programmable	Hardwire
DMA	4 Channels, 6.6 Mb/s @ 10 MHz	2 Channels 2 Mb/s @ 8 MHz	2 Channels, 3.2 Mb/s @ 10 MHz
Counter/Timers	3 16-bit	3 16-bit	2 16-bit
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CIRCLE NO 129

of $\overline{DSACKX}$ as the machine-cycle termination signal. NAND gates sample the target system's $\overline{STERM}$ signal on the CLK signal's rising edge, and flip-flop IC_{1A} latches the result. The IC_1 flip-flops provide stable control signals to the PAL, IC_7, and the data buffers, IC_2-IC_5.

These buffers latch data as the 68030 μP would, during synchronous read operations. The emulator runs 68020 cycles, however, so the buffers must hold their data until $\overline{DSACKX}$ informs the emulator that it can issue the latch strobe. (The target system sees a synchronous cycle of n clock pulses, while the emulator sees an asynchronous cycle of $n+$ clock pulses.) Other control signals to the buffers provide external-bus arbitration, indicate data direction for read and write operations, and command the high-impedance state between bus cycles.

The PAL handles bus arbitration and controls the address and data strobes. As a result, the target system sees the strobes negate as though an actual

TABLE 1—PAL EQUATIONS

```
PAL16R4                                          PLD DESIGN SPEC
UX                                               1988
020 TO 030 TARGET DAUGHTER BOARD. ASYNCH AND SYNCH SUPPORT.
UNIVERSITY OF CHICAGO, CHICAGO, IL
CLK      NC       NC       /BGACK    /BG      RWN     /DS      /AS      /SYNC    GND
GND      NC       /RW      /DOE      NC       /HIZ    NC       /30AS    /30DS    VCC

RW=RWN                                   ;invert for data buffers
DOE:=/BGACK* AS                          ;enable/disable buffers rising CLK after AS
HIZ:=BGACK                               ;strobe tristate control bus arbitration, rising CLK
        +/AS*BG                          ;if BG, tristate at end of bus cycle, rising CLK
IF (/HIZ) 30 DS=DS*/SYNC                 ;68030 data strobe with synchronous control
IF (/HIZ) 30AS=AS*/SYNC                  ;68030 addr strobe with synchronous control

DESCRIPTION: /RW generator, data buffer control and strobe generation.
```

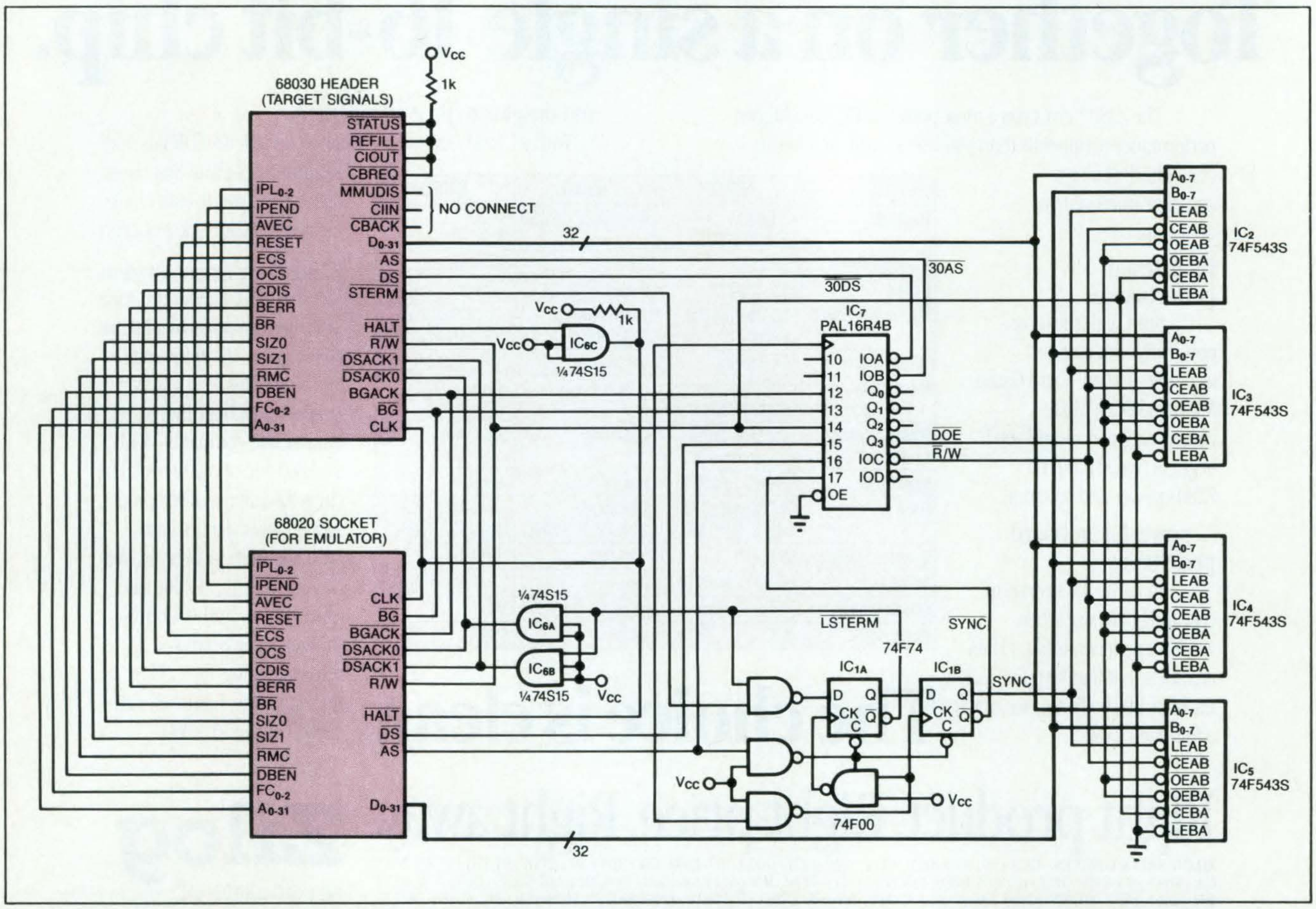

Fig 1—This circuit constitutes an adapter board that lets you develop a 68030 μP system by using a 68020 in-circuit emulator.

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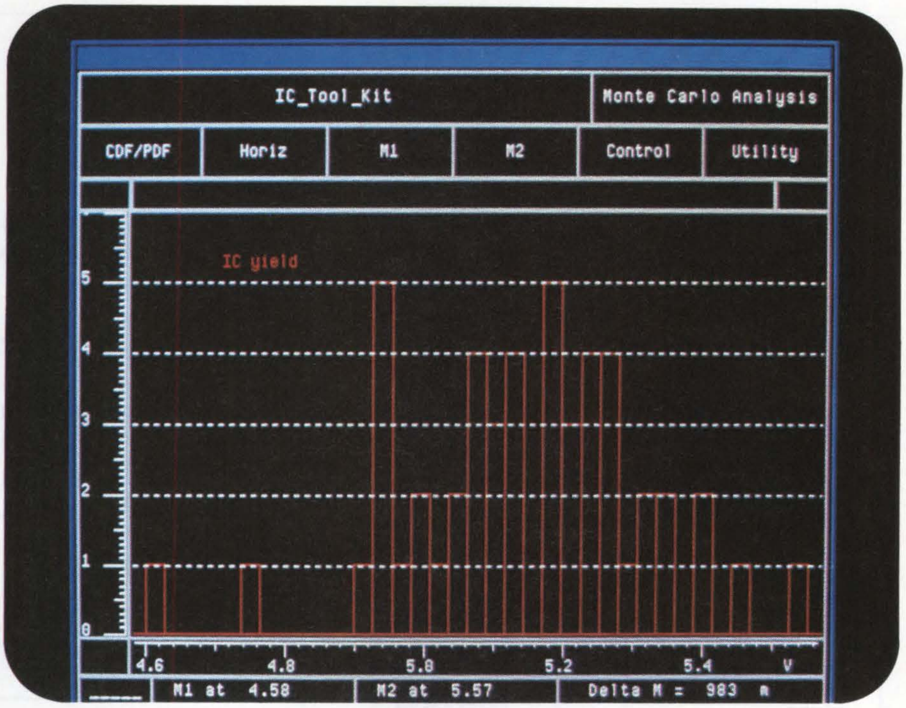

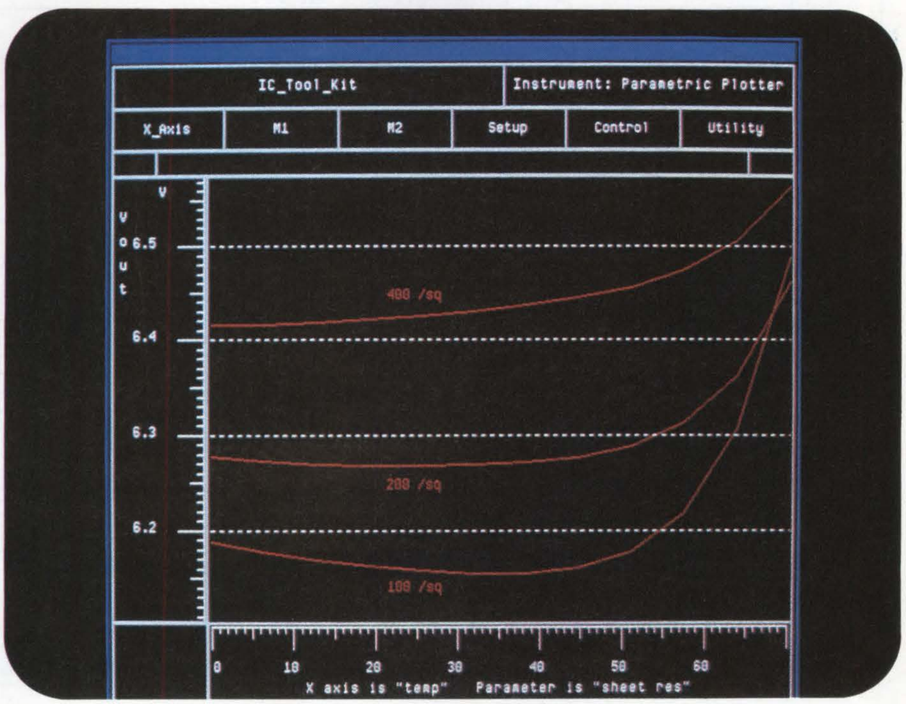

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CIRCLE NO 126

68030 were running its synchronous bus cycle. The emulator, meanwhile, has not completed its asynchronous cycle and therefore continues to assert its strobe signals for another clock cycle. **Table 1** lists the PAL equations. A 15-nsec or faster PAL allows 68030 emulation at clock frequencies exceeding 16 MHz.

Unlike an actual 68030 μP, the adapter board does not provide a data cache or a burst-mode transfer. It does not support $\overline{\text{STATUS}}$, $\overline{\text{REFILL}}$, $\overline{\text{CIOUT}}$, or $\overline{\text{CBREQ}}$ signals (these always appear high to the target system), nor does it support the $\overline{\text{MMUDIS}}$, $\overline{\text{CBACK}}$, or $\overline{\text{CIIN}}$ input signals—these may assume any state without affecting the board's operation.

The target system should provide open-collector drivers for the $\overline{\text{DSACKX}}$ lines. If it doesn't, you can alter the circuit so that IC_{6A} and IC_{6B} buffer the target's $\overline{\text{DSACKX}}$ lines (as well as $\overline{\text{LSTERM}}$) before passing them to the emulator. **EDN**

To Vote For This Design, Circle No 748

PLD generates sequence for PROMs

V Lakshminarayanan
Sneha Corp, Bangalore, India

Fig 1's circuit uses an inexpensive PLD (IC_1) to control the programming of various Signetics PROMs and other pin-compatible devices. The circuit generates the signals required for programming sequential memory locations, and it also generates a control signal (TVCC) for switching the V_{CC} supply, a chip-enable signal (TCE), and a signal (CO) that drives the PROM's output

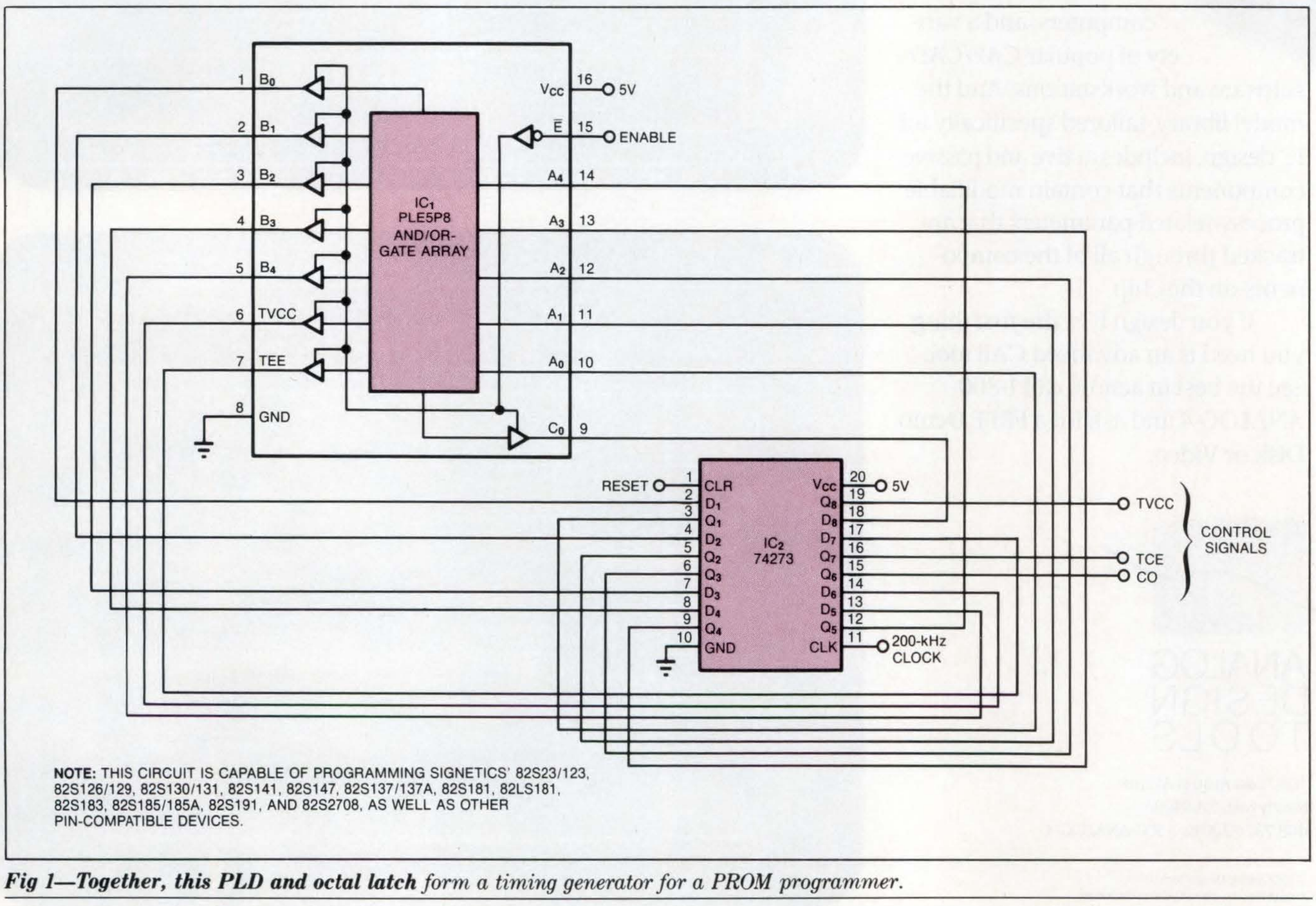

***Fig 1—Together, this PLD and octal latch** form a timing generator for a PROM programmer.*

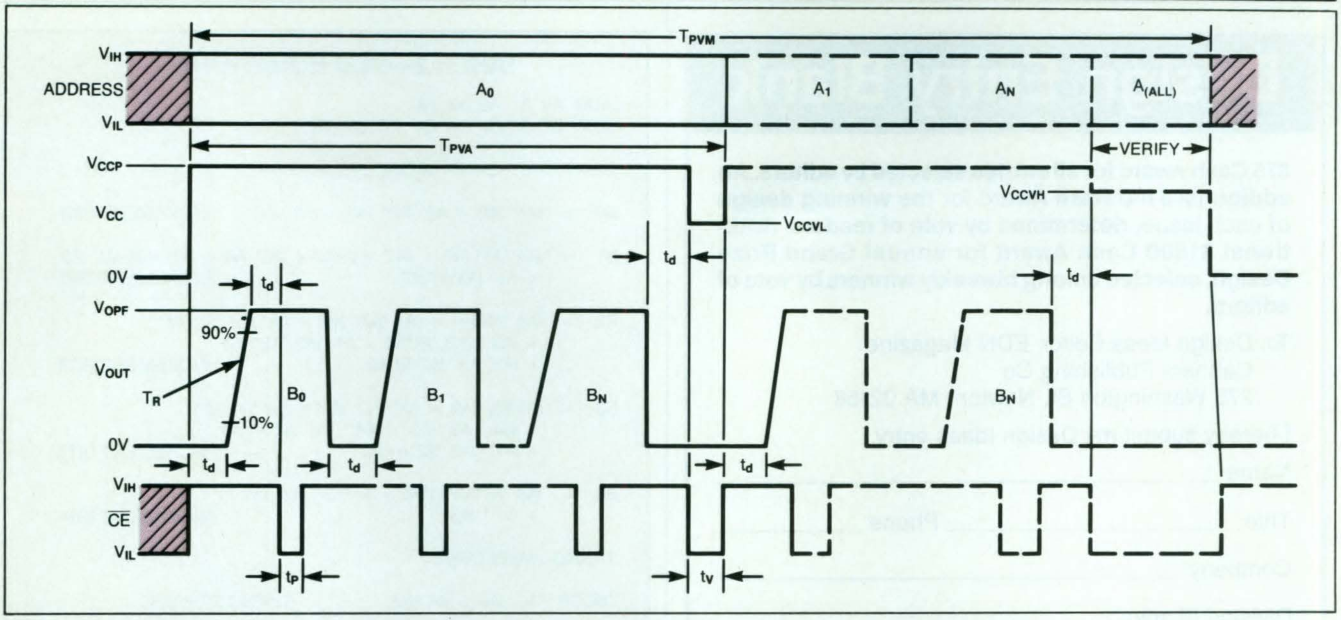

*Fig 2—**These waveforms are the product** of the programming sequences produced by the circuit of **Fig 1**.*

TABLE 1—TRUTH TABLE

TIMING GENERATOR FOR PROM PROGRAMMING

A4 A3 A2 A1 A0 B4 B3 B2 B1 B0 TVCCP TCE CO

;STATE ;AAAAA	NEXT STATE BBBBB	TIMING WAVEFORMS TVCCP	TCE	CO	;##	;COMMENTS
LLLLL	LLLLH	H	H	L	;01	;TAKE VCC TO VCCP ;AND CE TO VIH
LLLLH	LLLHL	H	H	H	;02	;AFTER TD DELAY
						;APPLY VOPF TO OUTPUT TO BE PROGRAMMED
LLLHL	LLLHH	H	L	H	;03	;AFTER TD DELAY TAKE
						;CE TO VIL FOR A PERIOD TP
LLLHH	LLHLL	H	L	H	;04	;
LLHLL	LLHLH	H	L	H	;05	;
LLHLH	LLHHL	H	L	H	;06	;
LLHHL	LLHHH	H	L	H	;07	;
LLHHH	LHLLL	H	L	H	;08	;
LHLLL	LHLLH	H	L	H	;09	;
LHLLH	LHLHL	H	L	H	;10	;
LHLHL	LHLHH	H	L	H	;11	;
LHLHH	LHHLL	H	L	H	;12	;
LHHLL	LHHLH	H	L	H	;13	;
LHHLH	LHHHL	H	L	H	;14	;
LHHHL	LHHHH	H	L	H	;15	;
LHHHH	HLLLL	H	L	H	;16	;
HLLLL	HLLLH	H	L	H	;17	;
HLLLH	HLLHL	H	L	H	;18	;
HLLHL	HLLHH	H	L	H	;19	;
HLLHH	HLHLL	H	L	H	;20	;
HLHLL	HLHLH	H	L	H	;21	;
HLHLH	HLHHL	H	L	H	;22	;
HLHHL	HLHHH	H	H	H	;23	;AFTER A PERIOD TP ;RETURN CE TO VIH
HLHHH	HHLLL	H	H	L	;24	;AFTER A DELAY OF TD
						;REMOVE VOPF FROM THE PROGRAMMED OUTPUT
HHLLL	HHLLH	L	L	L	;25	;TAKE VCC TO VCCL & ;CE TO VIL
HHLLH	HHLHL	L	L	L	;26	;LOOP HERE UNTIL ;RESET

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ISSUE WINNER

The winning Design Idea for the January 7, 1988, issue is entitled "Circuit vocalizes dialed phone numbers," submitted by V Lakshminarayanan of Sneha Corp (Bangalore, India).

TABLE 2—PLD EQUATIONS

```
.ADD  A0 A1 A2 A3 A4
.DAT  B0 B1 B2 B3 B4 TVCCP TCE CO

;NEXT STATE GENERATOR

B0  =  /A4* /A0 + A4* /A3* /A0 + /A1* /A0      ;INCREMENT LSB

B1  =  /A4* A1* /A0 + /A4* /A1* A0 + /A1* A0 + A4* /A3* /A1* A0
       + A4* /A3*A1*/A0                        ;INCREMENT BIT1

B2  =  /A4 *A2*/A1 + /A4 *A2* /A0 + A4* /A3 *A2* /A1
       + /A3 * /A2 *A1*A0 + A4 */A3 *A2* /A0
       + /A4 *A3 */A2*A1*A0                    ;INCREMENT BIT2

B3  =  /A4*A3 */A2 + A3* /A2 */A1 + /A4 *A3 */A1
       + /A4 * A3 */A0 + /A4 * /A3 *A2*A1*A0
       + A4 * /A3 *A2*A1*A0                    ;INCREMENT BIT3

B4  =  /A4 *A3*A2*A1*A0 + A4*A3* /A2* /A1
       + A4 * /A3                              ;INCREMENT BIT4

;TIMING WAVEFORMS

TVCCP  =  /A4 + A4 */A3              ;TIMING FOR VCC

TCE    =  /A4 */A3 */A2* /A1 + A4 * /A3 *A2*A1     ;TIMING FOR CE

CO     =  /A4 * /A1 * A0 + /A4 *A2 + /A4* A3
          + /A4 */A3 * A1 + A4 * /A3 */A0 + A4 */A3 */A2
          + A4 * /A3 * /A1           ;TIMING FOR OUTPUTS
```

pins to the voltage levels that the manufacturer has specified.

Applying a 200-kHz clock signal to the octal D-type flip-flop, IC_2, produces a 5-μsec pulse-sequence delay (t_D), a 100-μsec programming interval for TCE (t_P), and a 120-μsec interval for applying V_{CC} during programming (t_{VCCP}). **Fig 2**'s waveforms are those specified by Signetics. Karnaugh maps enable the derivation of the PLD equations of **Table 2** from the truth table of **Table 1**.

EDN

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UES1301 - UES1303	SPD605 - SPD630	50 - 300	6	40
UES1001 - UES1003	SHF1102 - SHF1106	200 - 600	1	35
DO-4 AND DO-5				
UES704HR - UES706HR	SDR600 - SDR606	50 - 600	15	45
1N5812 - 1N5816	1N5812 - 1N5816 (QPL)	50 - 150	20	35
UES804HR - UES806HR	SDR804HR - SDR806HR	400 - 1000	50	60
UES801 - UES803	SDR803 - SDR807	50 - 250	100	60
1N6304 - 1N6306	1N6304 - 1N6306	50 - 150	70	50
Schottky Rectifiers*				
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	SPD0801 - SPD1001	60 - 100	1	1
USD245HR	SPD5823 - SPD5825	20 - 40	5	1
Centertaps—Positive, Negative, and Doublers				
UES2604HR - UES2606HR	SHA2604 - SHA2606	200 - 400	30	35
681-1 thru 681-6	SDA180A - SDA180G	50 - 1000	15	5μs
689-1 thru 689-6	SDA280A - SDA280G	50 - 1000	15	150
Single Phase Bridges				
673-1 thru 673-85	SDA276A - SDA276L	50 - 3000	1.5	5μs
676-1 thru 676-12	SDA356BF - SDA356NF	100 - 1200	1	30
680-1 thru 680-6	SDA304A - SDA304G	50 - 1000	10	5μs
684-1 thru 684-6	SDA267A - SDA267G	50 - 1000	10	150
679-1 thru 679-6	SDA130A - SDA130G	50 - 1000	25	5μs
802-1 thru 802-4	SDA18A - SDA18G	200 - 800	35	50
Three Phase Bridges				
700-1 thru 700-6	SDA294A - SDA294L	50 - 3000	.5-2	5μs
696-1 thru 696-6	SDA35AUF - SDA35FUF	100 - 600	14	70
678-1 thru 678-6	SDA167A - SDA167G	50 - 1000	25	5μs

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CIRCLE NO 127

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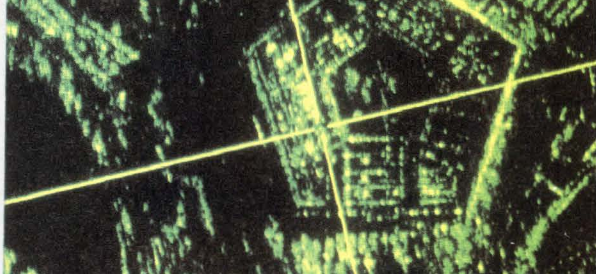

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March 21 to April 22 (Northeastern Edition)

DATE	TIME	SITE
3/21 Monday	9:00-11:00 AM	GENERAL ELECTRIC COMPANY Chestnut St., Phildelphia, PA
3/21 Monday	12:30-2:30 PM	UNISYS CORPORATION 70 E. Swedesford Rd., Paoli, PA
3/21 Monday	3:00-4:30 PM	UNISYS CORPORATION 2476 Swedesford Rd., Paoli, PA
3/22 Tuesday	9:00-11:00 AM	UNISYS CORPORATION Township Line & Union Meeting, Blue Bell, PA
3/22 Tuesday	11:30-1:00 AM-PM	KULICKE & SOFFA INDUSTRIES, INC. 2101 Blair Mill Road, Willow Grove, PA
3/22 Tuesday	2:00-4:00 PM	LEEDS & NORTHRUP Sumneytown Pike, North Wales, PA
3/23 Wednesday	8:30-11:00 AM	RCA CORPORATION Delaware & Market St., Camden, NJ
3/23 Wednesday	11:30-1:30 AM-PM	RCA CORPORATION Marne Hwy., Moorestown, NJ
3/23 Wednesday	3:00-4:30 PM	DAVID SARNOFF RESEARCH CENTER 201 Washington Road, Princeton, NJ
3/24 Thursday	8:30-11:00 AM	LOCKHEED ELECTRONICS U.S. Hwy. 22, Plainfield, NJ
3/24 Thursday	12:30-2:30 PM	ITT DEFENSE COMMUNICATIONS 492 River Road, Nutley, NJ
3/24 Thursday	3:00-4:30 PM	ITT AVIONICS 390 Washington Ave., Nutley, NJ
3/25 Friday	8:30-11:00 AM	AT&T BELL LABS 600 Mountain Ave., Murray Hill, NJ
3/25 Friday	12:30-2:00 PM	AT&T BELL LABS 260 Cherry Hill Rd., Parisppany, NJ
3/25 Friday	2:30-4:00 PM	AT&T BELL LABS Whippany Road, Whippany, NJ
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3/28 Monday	11:30-1:30 AM-PM	SINGER CO., KEARFOTT DIVISION 1150 McBride Ave., Little Falls, NJ
3/28 Monday	2:30-4:30 PM	ALLIED BENDIX CORPORATION Route 46, Teterboro, NJ
3/29 Tuesday	8:30-10:30 AM	EATON CORPORATION, AIL 45 Oser Ave., Hauppauge, NY
3/29 Tuesday	11:00-1:30 AM-PM	EATON CORPORATION, AIL Walt Whitman Rd., Melville, NY
3/29 Tuesday	2:00-4:00 PM	FAIRCHILD WESTON CORPORATION 300 Robbins Lane, Syosset, NY
3/30 Wednesday	8:30-11:00 AM	HAZELTINE CORPORATION Cuba Hill Road, Greenlawn, NY
3/30 Wednesday	11:30-1:00 PM	NORDEN SYSTEMS 75 Maxess Rd., Melville, NY
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3/31 Thursday	10:45-12:30 AM-PM	UNISYS CORPORATION Marcus Ave., Great Neck, NY
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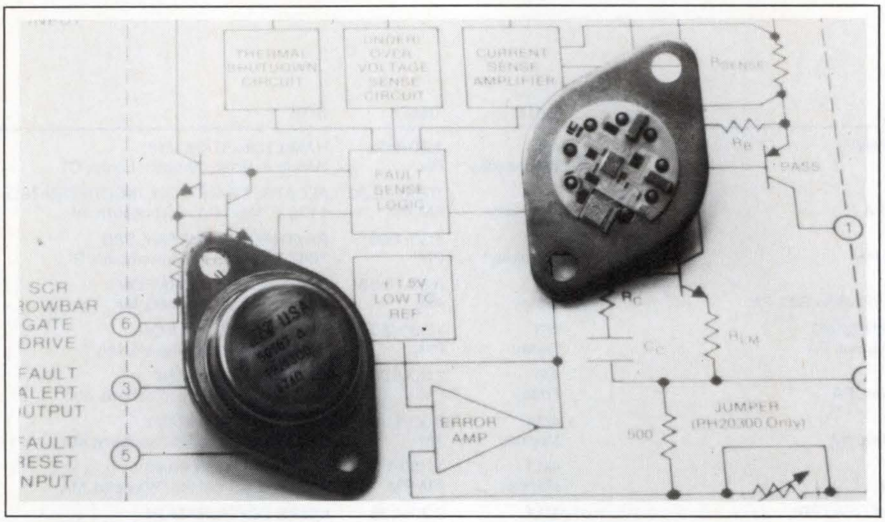

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Micro Networks, 324 Clark St, Worcester, MA 01606. Phone (617) 852-5400.

Circle No 351

CMOS DSP CHIP

- *Lower-speed version of original 20-MHz type*
- *Lower current than NMOS types*

The TMS320C10NL-14, a 14-MHz version of the CMOS TMS320C10NL 20-MHz device is pin for pin and object code compatible. It executes 3.5 MIPS and performs a 16×16-bit multiplication in 280 nsec. The CMOS device has a typical supply current of 25 mA, compared with 180 mA for the NMOS TMS32010NL-14. The device comes in a 40-pin DIP. \$9 (1000).

Texas Instruments, Semiconductor Group (SC-784), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 352

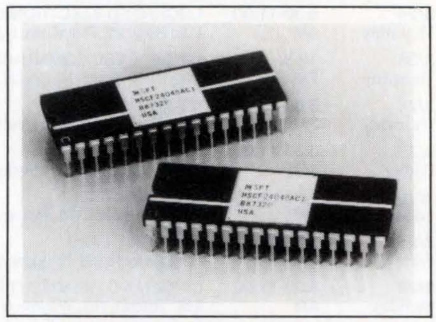
RISC PROCESSOR

- *Operates in either RISC or MIL-STD-1750A mode*
- *Low-power 1.5 μm CMOS fabrication*

The UT1750AR reduced-instruction-set computer (RISC) is a μP that also supports MIL-STD-1750A 32-bit floating-point operations and 48-bit extended-precision floating-point operations on chip. It has a full 64k-word address space and is expandable to 2M words with the optional UT1750 memory-management unit. The UT1750AR has built-in μP bus arbitration and DMA support; it also contains a 9600-baud UART for MIL-STD-1750AR console mode. In the RISC mode, the device operates at 6 MIPS of throughput, using a 12-MHz clock; in the MIL-STD-1750' mode, it operates at 0.7 MIPS, using the digital-avionics-instruction set. The UT1750AR is TTL compatible and is available in either a 144-pin pin-grid array or a 132-lead flatpack. \$650.

United Technologies Microelectronics Center, Military Standard Products Dept, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907. Phone (800) 645-8862; in CO, (303) 594-8259.

Circle No 353



PROGRAMMABLE FILTER

- *Programmable, 7th-order lowpass active filter*
- *Implements RC and SC filters on same chip*

Designed primarily for instrumentation and data-acquisition systems, the HSCF24040 implements both RC (resistor-capacitor) and SC (switched-capacitor) filters on the same chip. It provides high-precision antialiasing protection prior to A/D conversion. Device specifications guarantee full 12-bit performance with respect to noise, distortion, and antialiasing protection. A differential architecture for the SC filter provides an 85-dB dynamic range, and the RC/SC filter provides a >76-dB stopband attenuation. The SYNC and CNVRT control signals, combined with a programmable reduction in the sample rate, eliminate the need for an external S/H function prior to A/D conversion in many applications. The HSCF24040 operates from a ±5V supply and dissipates 150 mW. $26.90 (100).

Honeywell Inc SPT, 1150 E Cheyenne Mountain Blvd, Colorado Springs, CO 80905. Phone (719) 540-1000.

Circle No 354

QUAD OP AMP

- *Low offset voltage*
- *Independent operation*

The HA-5134 quad op amp features a maximum offset voltage of 100 µV. Unlike most quad devices (that share a common bias network), the four op-amp units (on a single chip) are completely independent in their operation. This independent functioning can boost the device's channel-separation performance to 120 dB. The slew rate is 1V/µsec, the unity-gain bandwidth is 4 MHz, and the minimum gain is 1500V/mV. The op amp comes in a 14-pin ceramic DIP. HA1-5134-2, $16.20; HA1-5134-5, $9.45 (100).

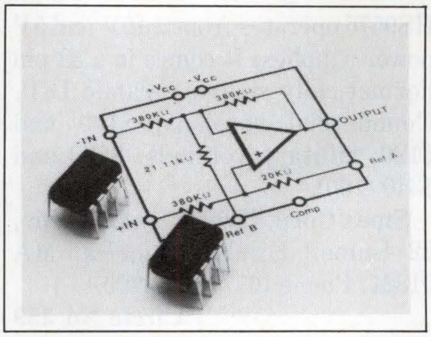
Harris Corporation, Semiconductor Sector, Box 883, Melbourne, FL 32901. Phone (305) 724-7800.

Circle No 355

DIFFERENTIAL AMP

- *±200V common-mode range*
- *74-dB common-mode rejection*

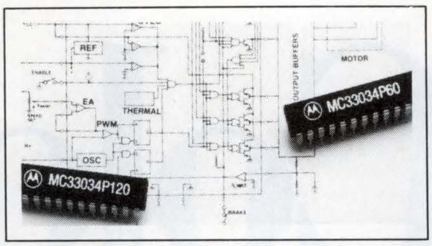
According to the vendor, the INA117P differential amplifier offers you a safe, economical approach to conditioning low-level signals in the presence of high voltages. It has a differential input range of ±10V



and a common-mode input-voltage range of ±200V. You can use the amplifier in ac or dc power-line monitoring, test equipment, and industrial-control and data-acquisition equipment not requiring total galvanic isolation. The device contains a premium-grade op amp and a precision resistor network on a single chip. It has a unity gain with a maximum error of 0.05% and a settling time of 6.5 µsec. $4.20 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 356



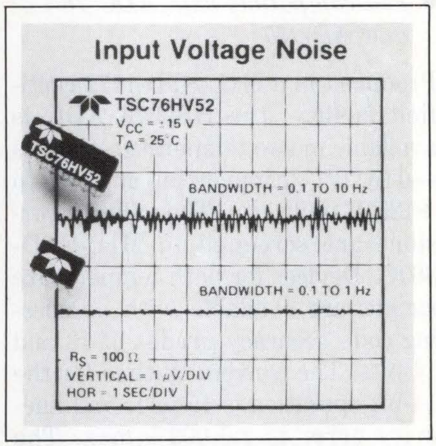
MOTOR CONTROLLER

- *For open-loop, 3- or 4-phase motor-control systems*
- *Two versions to satisfy different sensor phasing*

The MC33034 is an integrated brushless dc motor controller. It has a rotor position decoder for commutation sequencing, a temperature-compensated voltage reference that can supply power to Hall-effect sensors, a programmable sawtooth oscillator, three open-collector top drivers, and three high-current totem-pole drivers that can drive power MOSFETs. Its safety features include cycle-by-cycle current limiting, undervoltage lockout, internal thermal shutdown, and a fault output that you can interface to a microprocessor. It controls motors in major appliances, in blowers and pumps, in automotive fans and windshield washers, and in industrial machinery. $4.90 (100).

Motorola Inc, Technical Information Center, Box 52073, Phoenix, AZ 85072. Phone (602) 897-3840.

Circle No 357



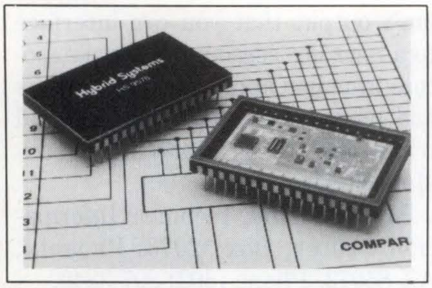
LOW-NOISE OP AMP

- *Chopper stabilized*
- *Single- or dual-supply operation*

The TSC76HV52 op amp is pin compatible with the low-voltage TSC-7652 and extends power-supply operation to ±15V. Single- or dual-supply operation is possible. The device's output-voltage swing is typically >±13V into a 2k-Ω load. The open-loop gain is 120 dB min with a 10k-Ω load. Optimized for low noise and low power, the op amp's noise is 0.2 [mu]V p-p for a 1-Hz bandwidth, and the supply current is 1 mA at ±15V. The offset-voltage drift is 0.3 µV/°C. The device extends the input common-mode voltage to the negative supply rail, permitting single-supply operation. The common-mode rejection is a 120 dB min. The device is available in 8- or 14-pin cerDIPs. From $4.85 (100).

Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (415) 968-9241. TWX 910-379-6494.

Circle No 358



16-BIT ADC

- *Converts in 15 μsec*
- *Pin-compatible with ADC-76 and AD-376*

Produced in a MIL-STD-1772 certified facility, the HS9576 ADC is available in two temperature ranges —0 to 70°C (commercial) and −55 to +125°C (military). The military versions are screened to MIL-STD-883C. Devices for both temperature ranges are available with no-missing-code accuracy grades of 13 and 14 bits. The conversion time for the 14-bit operation is 15 μsec and linearity error is ±0.003% max. The HS9576 operates from ±15V and 5V power supplies. It comes in a 32-pin hermetically sealed ceramic DIP. Commercial versions, $109 and $120; military versions, $299 and $340 (100).

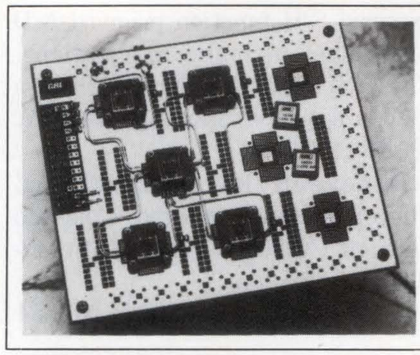
Sipex Corp, Hybrid Systems Div, 22 Linnell Circle, Billerica, MA 01821. Phone (617) 667-8700.

Circle No 359

GaAs LOGIC ICs

- *1.3-GHz expandable 4-bit adder*
- *1.4-GHz carry look-ahead generator*

The 10G100 is a 1.3-GHz, 1200-psec delay, expandable 4-bit adder. The companion 10G101 is a 1.4-GHz, 675-psec delay, carry look-ahead generator. The carry look-ahead IC expands the adder's capability of handling 16-bit-wide additions; multiple 10G100s and 10G101s can implement fast adders of any larger



word size. The GaAs chip set can process a 16-bit addition in 2.06 nsec compared with the 7.6 nsec required for 100K ECL circuits. The vendor also claims that you can realize a 30% improvement in speed by using the 10G101 separately to replace ECL look-ahead circuits in existing adder designs. The 10G100 and 10G101 are part of a series targeted for DSP subsystems such as BCD adders and subtractors, ALUs, digital filters, and FFT processors. The 10G100 and 10G101 operate over the 0 to 85°C temperature range and are available in 40-pin leaded or leadless chip carriers. 10G100, \$59.50; 10G101, \$55 (100).

GigaBit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91320. Phone (805) 499-0610. TLX 6711358.

Circle No 360

DRIVER IC

- *Incorporates three low-saturation-voltage drivers*
- *Protection against output desaturation*

The TDF1783SP driver IC contains three independent drivers that feature an output-saturation voltage of 0.35V at 1.5A. Their supply voltage range is 6 to 32V. By adding a sense resistor to each output you can program the output current limit. Internal logic for each driver detects desaturation of the output stage and automatically turns off the driver after a programmable delay period if desaturation occurs. In addition, the device has thermal-overload protection, which turns off all three drivers if the IC temperature rises excessively. \$4.50 (1000).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 361

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 362

TRANS-Z AMPLIFIER

- *280-MHz bandwidth*
- *Settles to 1% in 7 nsec*

The AD9611 transimpedance amplifier features a 280-MHz bandwidth and an offset voltage of ±0.5 mV; its dynamic performance is indepen-

dent of gain. It settles to 1% and 0.1% in 7 and 13 nsec, respectively; the rise and fall times are 1.3 nsec and 1.5 nsec. Designed for high-speed signal-processing applications that require high gain and wide bandwidth, the amplifier can drive ±4V into a 50Ω load; this capability allows the device to serve as an input buffer amplifier for high-speed, flash A/D converters. The device also suppresses voltage spikes that may damage flash ADCs. A proprietary feature of the device is constant power dissipation with load variations. This attribute, combined with a typical 720-mW power dissipation, lets the amplifier operate in ambient temperatures to 110°C without heat sinking. It operates from ±5V supplies and is available in industrial and military temperature grades. From $84 (100).

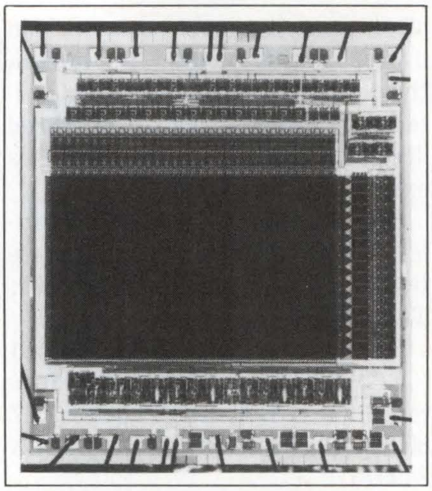
Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TWX 710-394-6577.

Circle No 363

CACHE-TAG RAMs

- *4096-word×4-bit organization*
- *15-nsec access time*

The SSL4180 and SSL4181 functionally equivalent circuits feature a fast flash-clear function and word-width expansion. The 4180 has a totem-pole output; the 4181 has an open-drain output. Both devices are TTL compatible, have 4096-word×4-bit organization and include an on-chip



comparator to generate a hit-or-miss output. The devices are packaged in 22-pin DIPs. Four speed ratings are available: 15-nsec version, $53; 20-nsec version, $32.30; 25-nsec version, $24.60; 35-nsec version, $17.50 (1000).

Saratoga Semiconductor, 10500 Ridgeview Ct, Cupertino, CA 95014. Phone (408) 973-0945.

Circle No 364

STATIC RAMs

- *4k-bit ECL devices fabricated in a bipolar/CMOS process*
- *Feature 8- and 10-nsec access times*

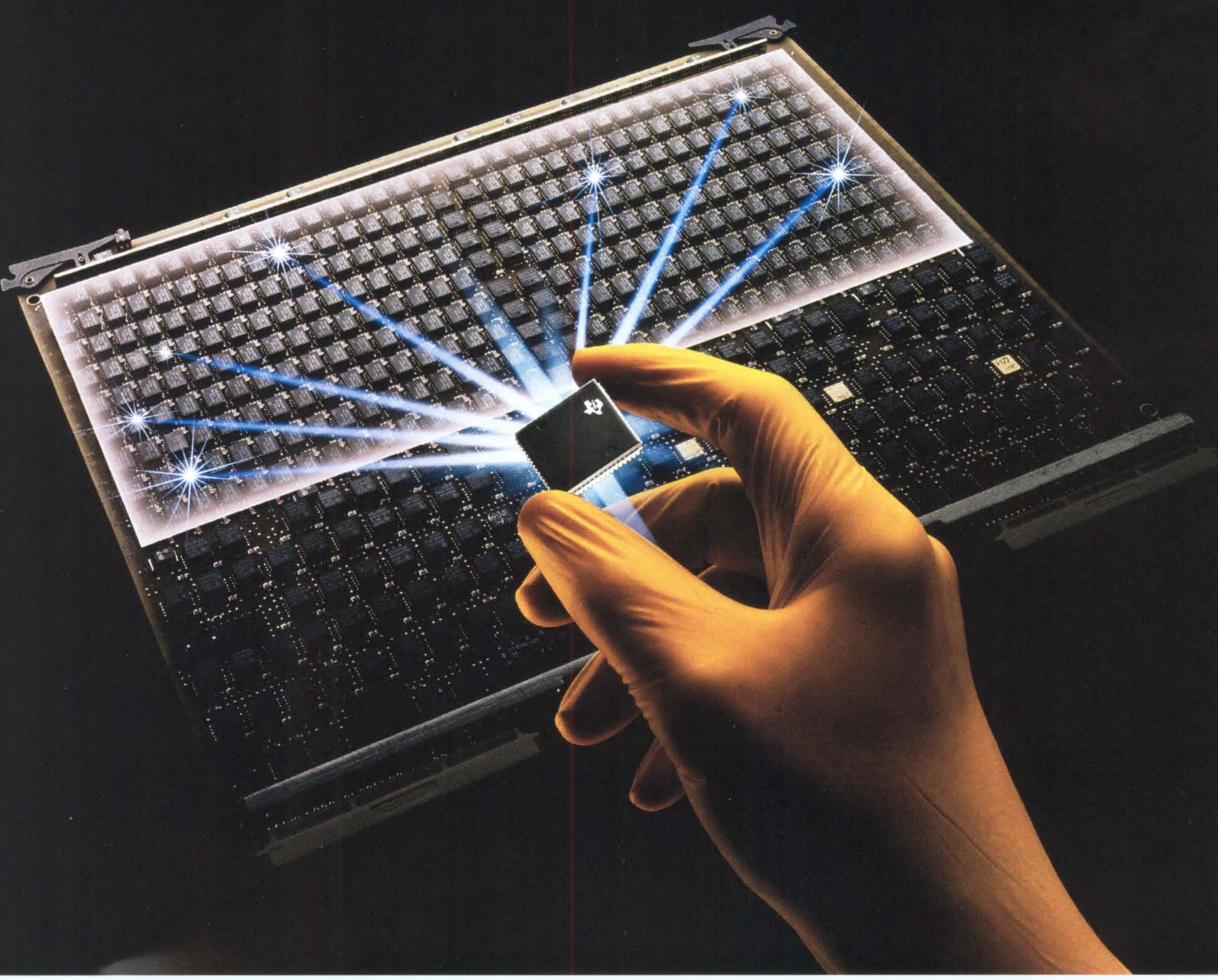
The SSM10470 (10K ECL) and 100470 (100K ECL) provide 10-nsec access times, and the 10474 (10K ECL) and 100474 (100K ECL) offer 8- or 10-nsec access times. These short access times suit the static RAMs for use in high-speed computers, graphics workstations, ATE, and high-speed logic analyzers. The 10470 and 100470 offer 4k×1-bit organization and come in 18-pin DIPS; the 10474 and 100474 feature 1k×4-bit organization and come in 24-pin DIPs. The devices are fabricated in a technology that integrates bipolar and CMOS elements in a monolithic chip. From $16.43 to $21.43 (100).

Saratoga Semiconductor, 10500 Ridgeview Ct, Cupertino, CA 95014. Phone (408) 973-0945.

Circle No 365

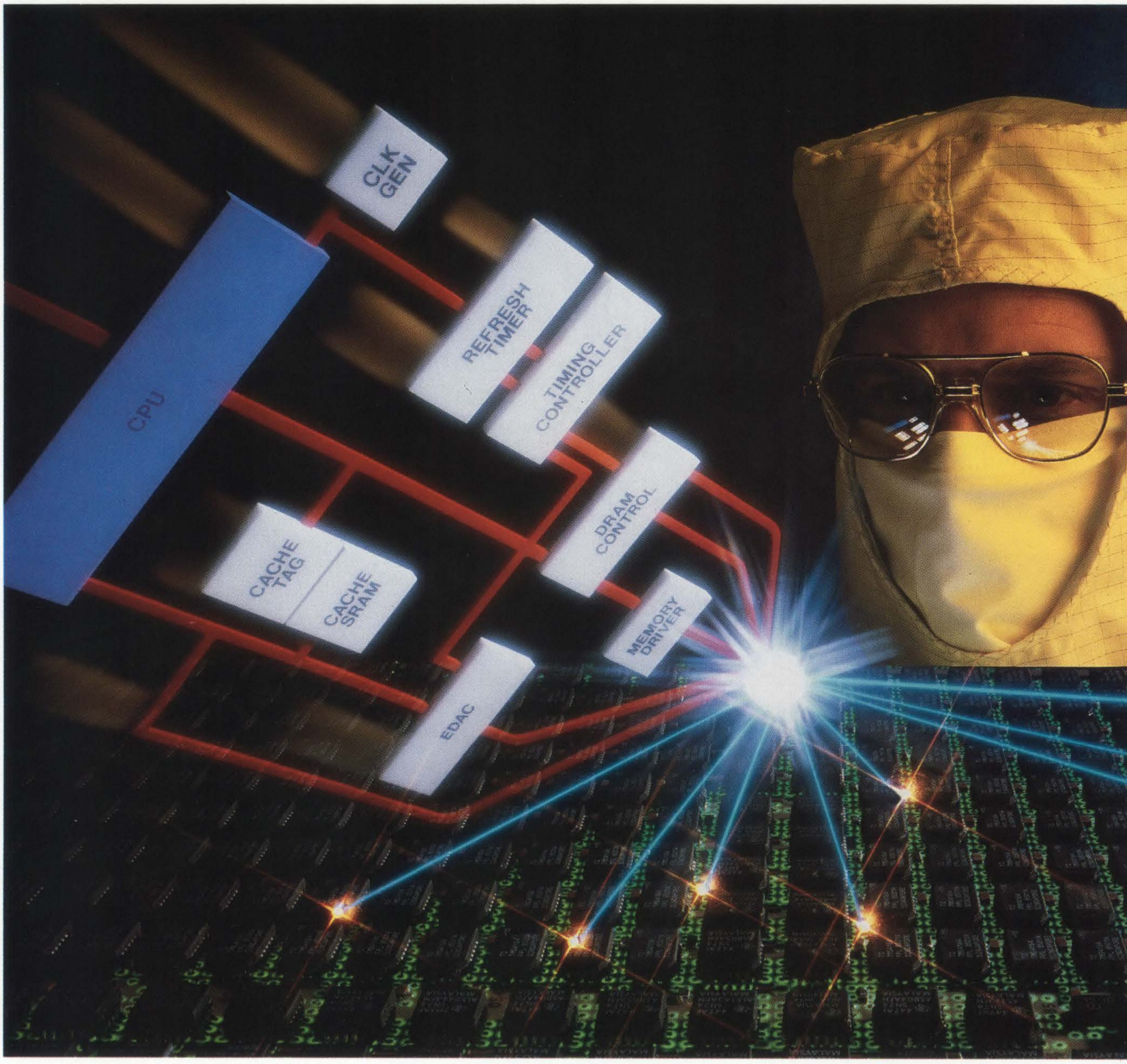
TEXAS INSTRUMENTS REPORTS ON MEMORY MANAGEMENT

IN THE ERA OF MegaChip™ TECHNOLOGIES



Memory management in the Era of MegaChip Technologies:

Memory-management ICs from you bring memory arrays up to



Memory systems are a prime area for significant improvements in overall system throughput. Read how TI's memory-management ICs can get you in and out of memory faster no matter which processor you choose.

You can now solve a problem whose solution has eluded design engineers for years: How to catch memory speeds up to CPU speeds. The solution lies with TI's advanced memory-management circuits, and you can use them with whichever processor best suits your application.

Texas Instruments can help processor speeds.

A universal architecture enables these TI devices to work with — and enhance — virtually any high-speed microprocessor or bus structure, even custom engines.

In addition, your component count is cut because these are single-chip VLSI circuits. Your design time and effort are shorter and easier because of TI's comprehensive Memory Management Design Kit *(see page 4)*.

TI addresses your major memory-design concerns

To immediately improve memory-access time, use both main and cache memories, as shown in the block diagram. This approach can produce up to a 3X increase in system performance.

Frequently accessed data and instructions are stored in a few high-speed static random-access memories and "tagged" by a TI industry-standard cache controller (SN74ACT2151/4). These 2K×8 CMOS controllers are the fastest available and can support deep cache architectures of 16K or even 32K.

This scheme is cost-effective because slower, less expensive dynamic random-access memories (DRAMs) can be used for main memory.

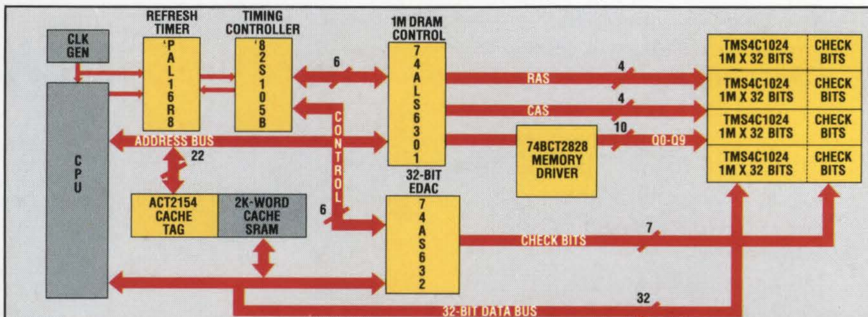
When you must assure system integrity, use of an error-detection-and-correction (EDAC) circuit can improve system reliability 500-fold. Since this approach is necessary with memory arrays larger than half a million bits, TI offers its leadership 32-bit EDAC.

The SN74AS632 detects dual-bit errors and detects and corrects single-bit errors while avoiding processor wait states. And at 25 ns for error detection, it meets your high-performance needs.

Interfacing between processor and main memory gets tougher as speeds increase. But TI has the SN74ALS6301 DRAM timing controller. It can handle any DRAM up to 1 Mbit and incorporates only the essential functions on chip to improve flexibility and speed and to allow for custom timing routines. This controller supports nibble- and page-mode access and scrubbing-mode refresh to increase memory output.

TI's MegaChip Technologies

Our emphasis on volume manufacturing of high-density circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies. They are the means by which we can help you and your company get to market faster with better, more competitive products.



High-speed memories can be designed with less effort and implemented more cost-effectively by using TI's family of universal memory-management ICs. These devices, all of which are contained in TI's Memory Management Design Kit, will work with and enhance almost any high-speed processor.

Soon to come: An ASIC (application-specific integrated circuit) solution.

Reducing over/undershoot is accomplished by TI's 2000 Series buffers and drivers — 25-ohm series-damping resistors on the output prevent false reads at DRAM input. For example, the SN74BCT2828 driver can reduce undershoot by 40% compared to traditional approaches. TI's 2000 Series has a high-drive current suitable for VME and MULTIBUS® II bus structures.

You can use any or all of TI's memory-management ICs to obtain the superior performance that marks a market winner. And there's no design rule that says your memory-management chips and your CPU have to come from the same supplier.

▶ *Turn page for more information.*

The tools you need to design a high-performance memory-management system are between these covers:

At \$149, the value of TI's Design Kit far outweighs its cost. In one compact file, we've included just about everything you'll need to bring your memory array up to speed. Everything, that is, except your imagination in creating your own unique product differentiators. Here's what you get:

- All necessary high-performance ICs, including
  - —SN74ACT2154 2K×8 Cache Address Comparator
  - —SN74AS632 32-bit EDAC
  - —SN74ALS6301 16K to 1 Mbit DRAM Controller
  - —SN74BCT2828 10-bit Buffer/Driver with series-damping resistor
  - —TIBPAL16R8-10 and TIB82S105B High-speed Programmable-logic Devices for user-defined timing control
  - —TMS4464 256K DRAM
- *Memory Management Applications Handbook* containing applications reports and briefs that supply valuable insights into memory-management system design.
- Data sheets on TI circuits designed for efficient memory management.
- Memory-management-product software graphic-symbol libraries and supporting documentation for use with Futurenet™ or Mentor Graphics™ CAE systems.

For more information on TI's Memory Management Design Kit, call 1-800-232-3200, ext. 3203, or contact your nearest TI field sales office or authorized distributor.

Texas Instruments Incorporated SDVØ63ED8ØØC
P.O. Box 809066
Dallas, Texas 75380-9066

YES, please send me more details on TI's universal memory-management ICs.

NAME ______________________________

TITLE ______________________________

COMPANY ______________________________

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AREA CODE ______ TELEPHONE ______________ EXT. ______

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Mentor Graphics is a trademark of Mentor Graphics Corporation.
®MULTIBUS is a registered trademark of Intel Corporation.

27-4510A

TEXAS INSTRUMENTS

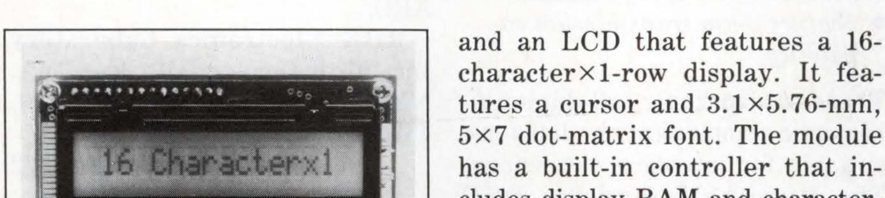
POWER SUPPLIES

- *Feature 90,000-hour MTBF*
- *Offer 80W of continuous output power*

The four SP1-80 Series 80W switching power supplies feature single-ended forward converter topologies and operate at a 45-kHz switching frequency to achieve a 90,000-hour MTBF. The various models offer 5, 12, 15, and 24V dc outputs. The supplies have a 70% min efficiency and feature circuitry that provides indefinite protection against short circuits on the output and that automatically recovers upon removal of the short. The line and load regulation spec at 0.1 and 0.5%, respectively. The devices' supply outputs are adjustable over a ±10% range. Their hold-up time equals 16 msec and their output ripple measures 1%. All models feature soft-start capability and power-good indicators. Optional features include a VDE-compatible B-input filter, a power-failure monitor, and a metal enclosure. $139. Delivery, stock to eight weeks ARO.

Power General, Box 189, Canton, MA 02021. Phone (617) 828-6216. TWX 710-348-0200.

Circle No 366



LCD MODULE

- *Offers back lighting*
- *Controller includes display RAM, character-generator ROM*

The AND673JO includes an LED that provides yellow backlighting and an LCD that features a 16-character×1-row display. It features a cursor and 3.1×5.76-mm, 5×7 dot-matrix font. The module has a built-in controller that includes display RAM and character-generator ROM. The module's dimensions are 80×36×16 mm. The supply voltage requirements are 5V for the LCD and 4V (at 125 mA max) for the LED back light. $25 (100).

AND Corp, 770 Airport Blvd, Burlingame, CA 94010. Phone (415) 347-9916.

Circle No 367

LED ARRAYS

- *Save assembly time*
- *Come in green, red, or yellow*

Featuring a tab on the bottom of their housings to improve positioning and alignment, these T-1 LED arrays are suited to right-angle mounting on pc boards. You can obtain them in blocks of 1, 2, 4, 8, and 16 to save assembly time. The LEDs come in red, green, or yellow, and they feature tinned terminals to improve the reliability of soldered contacts. No hardware is required to mount the assemblies. The units are compatible with automatic insertion and cleaning processes. From $0.50.

Elma Electronic Inc, 41440 Christy St, Fremont, CA 94538. Phone (415) 656-3400.

Circle No 368

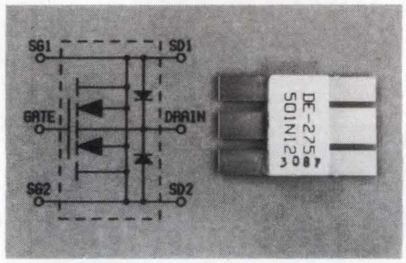
HEAT SENSOR

- *Reacts to heat from the human body*
- *Features a buffered digital output*

The IR1000 digital sensor module outputs a logic signal when a person moves into its field of view. A reference input allows you to adjust sensitivity and vary the sensing range. The module operates in daylight and responds to changes in infrared radiation in the range of 8 to 14 μm. To provide noise immunity, the module rejects signal fluctuations outside the range of 01. to 10 Hz. The digital output can drive either TTL- or CMOS-type devices. The output is buffered and provides ±150 mA. The module also provides an analog representation of the received infrared radiation for measurement applications. $25 (100).

Infrared Inc, Box 47, Parlin, NJ 08859. Phone (201) 721-7160.

Circle No 369



MOSFETs

- *Surface-mountable devices*
- *Switching speed specs at 1 nsec*

The DE-275 Series power MOSFETs have switching speeds of 1 nsec and average power ratings of 1 to 5 kW at pulse recurrence rates in excess of 10 MHz. The line includes P- and N-channel devices with 100 and 200V drain to source breakdown-voltage ratings and N-channel units with 500, 800, and 1000V ratings. The devices use a ceramic substrate with a thermal coefficient close to that of silicon, so the die are somewhat protected from uneven expansion and contraction. The thermal impedance from junction to heat sink equals 0.4°C/W. All DE Series devices are surface mountable. From $135.

Directed Energy, 344 E Foothills Parkway, Fort Collins, CO 80626. Phone (303) 226-6138.

Circle No 370

OPTICAL LINKS

- *Meet Tempest specifications*
- *Feature 2-km transmission capability*

These transparent, full-duplex fiber-optic communications links are suitable for interface extensions. The Micro1110T furnishes DCE (data communications equipment) compatibility at the terminal or CPU end of the link; the Micro1120T provides DTE (data terminal equipment) compatibility at the modem end. Both modules meet Tempest specifications and feature SMA-compatible connectors. The link transmission capability ranges to 2 km at data rates of 76.8k bps in synchronous or asynchronous mode. The data, receive/transmit clock, and control signals simultaneously pass through the link from DTE to DCE. The modules fully support the standard interface control-signals associated with the RS-232C and MIL-STD-188C standards. $385 per end.

Versitron Inc, 6310 Chillum Pl NW, Washington, DC 20011. Phone (202) 722-8600.

Circle No 371

IF AMPLIFIERS

- *Feature 70 dB typ IF gains*
- *Handle rugged military environments*

Models ICE2104 and ICEVT2104 linear IF amplifiers have a 4-MHz bandwidth centered at 21 MHz. The ICE unit has a single IF output, whereas the ICEVT provides IF and video outputs. Both amplifiers have 50Ω-input and -output impedances, and noise figures of 4 dB max. The ICE model features typical IF gains of 70 dB; the ICEVT typically generates IF and video I/O gains of 80 dB. Both amplifiers are suitable for rugged military environments. They weigh 3 oz and come in machined aluminum 3.53×1.5×9.48-in. packages. Each amplifier draws approximately 100 mA at 12V dc. ICE2104, $795; ICEVT2104, $935. Delivery, 90 days ARO.

RHG Electronics Laboratory Inc, 161 E Industry Ct, Deer Park, NY 11729. Phone (516) 242-1100. TWX 510-227-6083.

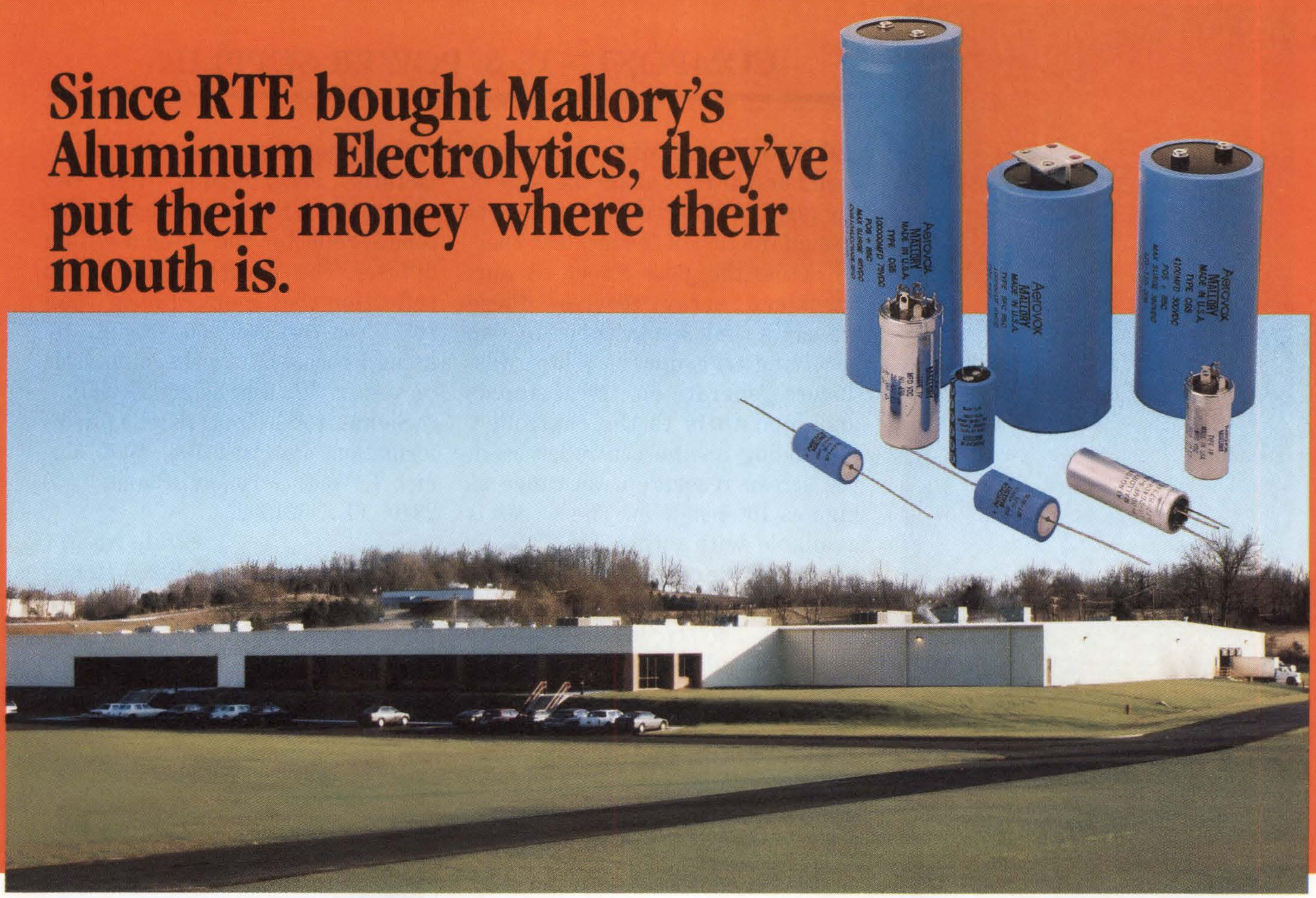
Circle No 372

TOUCHSCREEN

- *100 point/in. resolution*
- *Comes with controller and menu-driven software*

The pressure-sensitive IntelliTouch Trace screen uses two small transducers to send very short bursts of acoustic waves along the horizontal

Since RTE bought Mallory's Aluminum Electrolytics, they've put their money where their mouth is.

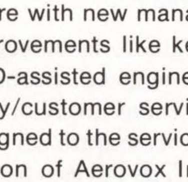


Announcing the latest, largest investment in this dynamic product line: our new Aerovox M plant – over 50% bigger & just across the street!

When RTE bought Mallory's aluminum electrolytic capacitor line last year, priority #1 was to retain the quality and respect this fine product line already enjoyed by retaining the same facility and skilled work force. However, they immediately began building for a bigger future with new management appointments plus major improvements like key equipment upgrades, in-house CAD-assisted engineering, and a computerized order entry/customer service system. Also, field sales was assigned to the service-driven rep and distributor organization of Aerovox Inc., another RTE company and a world-leader in AC capacitors.

But for the ambitious future RTE envisioned for this vital product line, we needed more room — fast! Available land across the street from the original Mallory plant allowed us to build — then move — without losing production or a single skilled worker!

Our new plant has been shipping product for over two months, with improvements in yields and quality already evident. So now our big news is about completing another giant step on our way to becoming #1 in aluminum electrolytics. For your next cap requirement, call your Aerovox rep or us, and see for yourself what a difference a full commitment to excellence can make in a product line that was outstanding to begin with!



Send for a set of technical bulletins today.

Now we're Aerovox MALLORY*

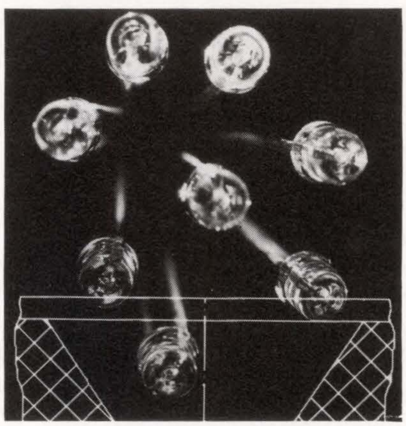
Glasgow, Kentucky 42141
(502) 651-8301 • FAX 502-651-9312

CIRCLE NO 183

and vertical edges of the screen. As each burst travels along the edge of the glass, a reflective array diverts a small fraction of the incident energy across the glass screen. A mirror-image array receives these wavelets and sends them to two receiving transducers. The transducers generate electrical signals and send them to the controller. Depending on the controller used, the screen resolution can range as high as 100 points/in. The screen is available with either RS-232C or bus controllers as well as menu-driven, general-purpose application software. The screen is available in 5- to 19-in. displays. For a screen with a cable and a controller, from $400 (OEM qty).

Elographics Inc, 105 Randolph Rd, Oak Ridge, TN 37830. Phone (615) 482-4100. TLX 350348.

Circle No 373



LED

- *Emits the majority of its light output laterally*
- *Suitable for wide-area illumination of displays*

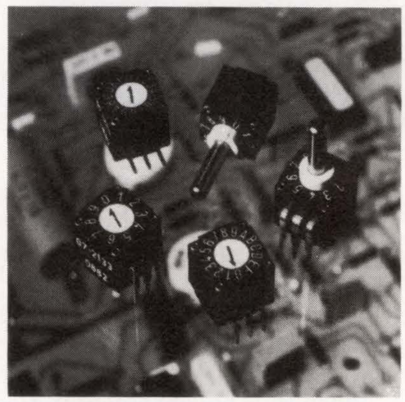
Suitable for the illumination of large-area displays, Argus 3-mm LEDs have a special lens that emits only 20% of the LED's light output in a forward direction—the remaining light output is emitted laterally. The LEDs are available in red, yellow, or green. under the model numbers LS-K380, LY-K380, and LG-K380 respectively. For optimal 2-dimensional lighting, the manufacturer recommends that you mount the LED in the center of a conical reflector and cover it with a diffuser. The reflector should have a reflection coefficient of more than 90%. You can get good results by using Procan-B7375 thermoplastic polyester. $0.15 to $0.20 (25,000).

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 374

Siemens, Opto Div, 19000 Homestead Rd, Cupertino, CA 95014. Phone (408) 257-7910. TWX 910-338-0022.

Circle No 375



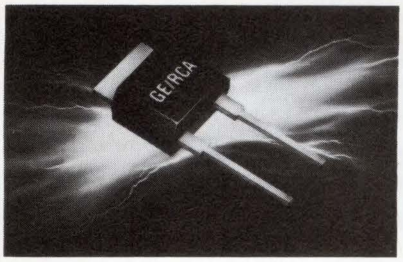
DIP SWITCHES

- *10,000-cycle switching life*
- *Available in shorting and nonshorting versions*

Available with BCD, hexadecimal, and Gray-coded outputs, Series 07 DIP switches come in shorting/nonshorting, horizontal-/vertical-mount versions. The devices feature either screwdriver or shaft-type actuation options, and they are hermetically sealed and washable. The contacts can switch 0.2A at 50V max. The switches have a lifetime of 10,000 switching cycles, and the operating range specs at −40 to +85°C. From $3.50 (100).

Elma Electronic Inc, 41440 Christy St, Fremont, CA 94538. Phone (415) 656-3400.

Circle No 376



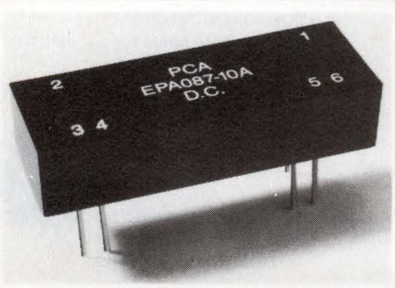
SUPPRESSOR

- *Handles 300A surge currents*
- *−40 to +85°C operating range*

The SGT23B13 transient surge protector can handle 300A peak surge currents. It features two monolithic compound structures—each consists of a thyristor whose gate contains a special diffused section that acts as a zener diode. The sections are connected in antiparallel to provide bidirectional protection in a single 2-lead, modified TO-202 package. In the forward-blocking mode, the SGT23B13's high-impedance, low-leakage off-state condition minimizes loading of the telecommunications line. Its operating range spans −40 to +85°C. $1.24 (1000).

GE Solid State, Route 202, Somerville, NJ 08876. Phone (201) 685-6456.

INQUIRE DIRECT



DELAY LINES

- *Feature 2- to 112-nsec delays*
- *20-nsec maximum rise times*

The EPA087 Series screwdriver-adjustable delay lines cover a 2- to 112-nsec delay range and are available with 50, 75, or 100Ω characteristic impedance. The eight delay ranges for each impedance level measure from 2 to 12 through 12 to 112 nsec. The output rise times (from the 10 to 80% points) vary with the variable delay range and spec at 2.5 nsec for a 2- to 12-nsec delay line to 20 nsec for the 12- to 112-nsec units. For a 100Ω, 2- to 12-nsec line, $20 (1000). Delivery, stock to six weeks ARO.

PCA Electronics Inc, 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761.

Circle No 378

DRIVER/CONTROLLER

- *Accommodates 600M-bps data rates*
- *Slow start/stop circuitry for laser protection*

The LDC 600 laser driver/controller can drive and control compatible laser diodes at 600M bps. It maintains preset optical power while providing a current source for regulating a thermoelectric cooler/heater. The 1.5×2-in. module readily mounts on standard pc boards. The unit features bandgap referenced current sources that allow it to maintain all parameters over the full operating range. This feature simplifies the system-design process by eliminating variations in forward current, drive level, and automatic laser-power control. Slow start/stop circuitry guards laser systems from damage that can occur when power is suddenly turned on or off. The module features 50Ω differential ECL inputs. $349.

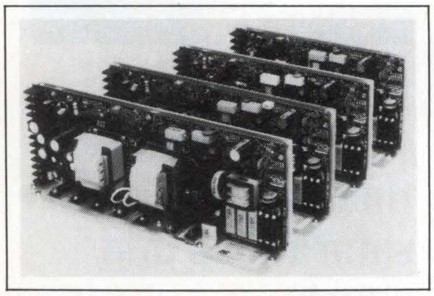
Tektronix Inc, Electro-Optic Components Group, Box 500, Beaverton, OR 97077. Phone (503) 627-4220.

Circle No 379

POWER SUPPLIES

- *Provide four outputs*
- *Feature international input capability*

The four SQM Series quad-output, open-frame switching power supplies provide outputs of 150 to



350W. The 5V main outputs have current ratings of 20 to 50A; auxiliary outputs of 5, 12, 15, and 24V have current ratings of 16A max. The supplies' standard features include international input capability, built-in line filtering, overload and overvoltage protection, and remote-sense and overtemperature-shutdown capability. Options include RFI/EMI covers, power-failure-detection circuitry, and power-valid signals. $239 to $379.

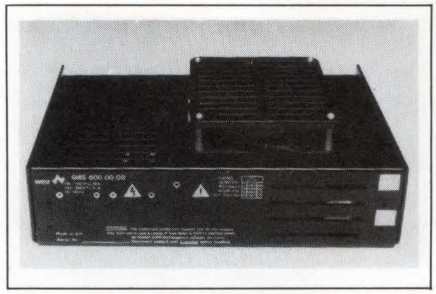
Switching Systems International, Box 1599, Placentia, CA 92670. Phone (714) 996-0909.

Circle No 380

SWITCH-MODE SUPPLIES

- *Provide 600W of output power at 12, 15, 24, or 50V*
- *Can be paralleled for greater output power*

The SMS600 series of single-output fan-cooled switch-mode power supplies provide output power of 600W and are available with nominal output voltages of 12, 15, 24, or 50V. The 12 and 15V outputs are covered by a single model, which features a potentiometer for output selection. The 24 and 50V versions have a potentiometer, which gives you approximately ±10% control over the output voltage. The line regulation is specified at less than 0.25% for a ±15% change in the input voltage, and the load regulation is better than 0.5% for a 10 to 100% load change. The power supplies have an 80% efficiency at normal operating loads. The supplies' standard features include remote output sens-



ing, and signals that indicate that the device is fully operational and that warn of power or output-fan failure. The output is protected against overcurrent and overvoltage conditions. The supplies meet major safety and RFI standards. £275 (100).

Weir Electronics Ltd, Durban Rd, Bognor Regis, Sussex PO22 9RW, UK. Phone (0243) 865991. TLX 86543.

Circle No 381

Weir Inc, 418 3rd St, Annapolis, MD 21403. Phone (301) 268-0122. TWX 510-600-7370.

Circle No 382

COMPUTERS & PERIPHERALS

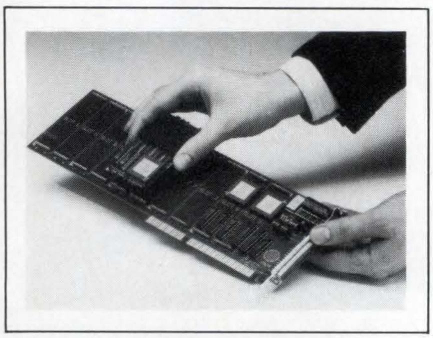
MONITOR SYSTEM

- *Uses phone lines to warn of possible facility damage*
- *Dials as many as four phone numbers*

The Model 1100 Sensaphone system is a monitoring system for remote or unattended facilities. A proprietary voice synthesizer delivers a warning message in English over phone lines if a condition exists that will damage the facility. In the event of an alert condition, the system will dial as many as four phone numbers in sequence. All built-in sensor functions are selectable and programmable and can sense electrical power, temperature, and sound from a smoke or fire alarm. The device has four digital alert channels. Its µP can simultaneously monitor as many as seven conditions. The system includes a call-in status-report feature with a programmable listening time. $300.

Phonetics Inc, 101 State Rd, Media, PA 19063. Phone (215) 565-8520.

Circle No 383



TRANSPUTER BOARD

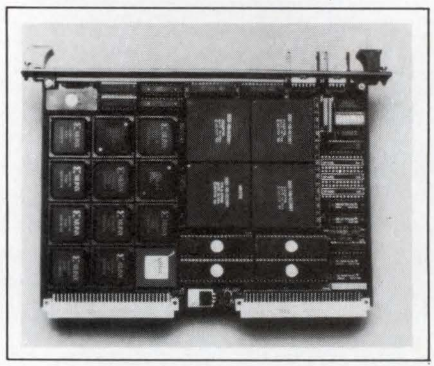
- *Modules for the IBM PC, PC/XT, and PC/AT*
- *Seven daughter boards and two mother boards*

The TRAM Transputer-modules family consists of seven daughter boards and two mother boards for the IBM PC, PC/XT, PC/AT, and compatible computers. The mother-and-daughter-board concept permits rapid prototyping and evaluation of multi-Transputer systems. The mother board contains rows of socket pins that accommodate daughter boards of varying sizes, and it features a digital switch on a chip, letting you "softwire" networks of Transputers into various configurations. Physically, the interface comprises a 16-pin dual-in-line socket with a 3.5-in. pitch. The smallest daughter board measures 1.05×3.5 in. and contains a Transputer with 32k bytes of static RAM. The largest board contains a Transputer and 1M byte of static RAM. IBM PC mother board, $1226; Eurocard mother board, $1750; daughter boards, $584 to $7471.

Inmos Corp, Box 16000, Colorado Springs, CO 80935. Phone (303) 630-4300.

Circle No 384

ADDRESS GENERATOR



- *Uses a custom, 80M-flop CPU to calculate IEEE 32-bit addresses*
- *Scales images and rectifies spatial distortions*

The AddGen MK 11 address-generator board performs image warping to spatially transform points of an image to a target space. The board calculates the address of the points in the target image for the particular space transformation used. It determines the course and subpixel locations and the magnification factors of the target pixel. It evaluates third-order polynomials at a 10-MHz rate for first- and second-order equations. The rate equals 5 MHz for third-order equations. The board can also perform depth-perspective transformations. It uses an 80M-flop CPU to calculate the IEEE 32-bit, floating-point addresses. You can scale images and rectify spatial distortions in an interactive manner. $6000. Delivery, 60 days ARO.

Datacube Inc, 4 Dearborn Rd, Peabody, MA 01960. Phone (617) 535-6644. **Circle No 385**


BELDEN PROTECTS YOUR FIBER OPTIC SYSTEM THROUGH THE HARSHEST ENVIRONMENTS
Belden® Multipurpose Computer Fiber Optic Cable
Belden® General Purpose LAN Fiber Optic Cable
Belden® Heavy-Duty Direct Burial Fiber Optic Cable
Belden® Plenum Breakout Fiber Optic Cable
Belden® BitLite® Military Fiber Optic Cable
Belden® Telecommunications Fiber Optic Cable
Rain, snow, dust, heat—new applications continuously test the limits of fiber optic performance. Without cables engineered specifically for your application, you may not realize the durability and high-volume information transfer you expected from your fiber optic system.
Extensive experience in LAN, video, telecommunications, data communications, instrumentation, process control, government and military applications allows Belden to anticipate and conquer your worst-case operating environments.
In addition to a wide range of standard products, Belden can manufacture the single-mode, armored, hybrid and high-fiber-count cables you need. Breakout configurations are available for easy termination and fast installation. Belden fiber optic cables are available in single piece standard put ups of 500, 1000, 3280 and 6560 feet. Custom lengths are also available.
Custom design, fast price and delivery information are as close as your local Belden Regional Sales office, while our nationwide distribution network can provide value-added services as well as cable selection and system design assistance.
When performance is critical—come heat or high water—contact Belden. We'll protect your fiber optic system through the harshest environments. Belden Wire and Cable, P.O. Box 1980, Richmond, Indiana 47375.
1-800-BELDEN-4
There is no equal.™
Copyright © 1987 Cooper Industries, Inc.
See us in EEM
COOPER INDUSTRIES
BELDEN
CIRCLE NO 181

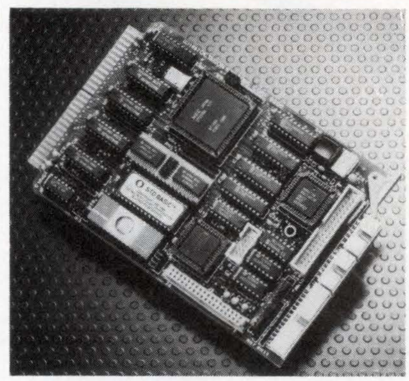
FACSIMILE

- *Telephone and facsimile machine speed-dials 32 numbers*
- *Transmits a business letter in 17 sec*

The FaxPhone 20 is a combination telephone and facsimile machine. It can speed-dial as many as 32 numbers (16 facsimile and 16 telephone) at the touch of a key. It's compatible with the following classes of facsimiles: G3, G2, and 6-minute FM units. It has a 5-pg automatic document feeder and can transmit a page at rates of 17 sec in G3 mode, 3 minutes in G2 mode, and 6 minutes in FM mode. Its document widths range from 5⅞ to 8½ in. A 20-digit, 2-line LCD provides step-by-step prompts and status messages. The unit records and prints out all facsimile use in periodic activity reports, so you always have a complete record of all transmissions and receptions. Its modem speeds range from 2400 to 9600 bps and have automatic fallback. $1995.

Canon USA Inc, 1 Canon Plaza, Lake Success, NY 11042. Phone (516) 488-6700.

Circle No 386



SYSTEM CARD

- *Has CPU, memory, and disk controller*
- *Includes multitasking operating system*

The 9500 board for the STD Bus combines many control and communications functions on one board. It features an 8-MHz, V25 CPU, which is code compatible with an 8088; two RS-232C ports; alphanumeric display and matrix keyboard ports; 24 digital I/O lines; a floppy-disk controller for two disks; an EEPROM programmer; 128k bytes of static RAM; an SBX expansion connector; and interrupt capability from 12 sources. Space for as much as 384k bytes of RAM or ROM is available. The card is all CMOS, but can drive CMOS and TTL peripheral cards. A multitasking operating system called STD Basic III is an interactive compiler with a universal set of industrial Basic commands that can manipulate hardware on the card or on other peripheral STD Bus cards. You can program STD Basic like Basic for the IBM PC; 37 of its 160 commands are tailored for the industrial environment. $695.

Octagon System Corp, 6510 W 91st Ave, Westminster, CO 80030. Phone (303) 426-8540.

Circle No 387

VOICE SYSTEM

- *Synthesis unit can recognize 200 words*
- *An 80C88 μP manages as much as 1M byte of RAM*

The Portable Voice Data Logger (PVDL) is a self-contained battery-powered, data-entry device. It consists of a Telxon Portable Computer (PTC) along with the company's voice-recognition and -synthesis unit. It uses CMOS surface-mount components to minimize size and power requirements. An 80C88 μP manages as much as 1M byte of static RAM. The device features a 64k-byte operating system, as much as 256k bytes of EPROM for applications, a real-time clock, multiple interrupts both vectored and polled, a 21-character×16-line display, an alphanumeric keypad, a modem, and a wand or a laser bar-code scanner. The voice-recognition and -synthesis subsystem is based on an SC-02/SSI-263A speech-synthesis IC, having unlimited text-to-speech synthesis capabilities. In addition, the susbsystem can recognize 200 words. The handheld unit withstands shock and vibration, EMI, and RFI. $3000.

The Voice Connection, 17835 Skypark Circle, Suite C, Irvine, CA 92714. Phone (714) 261-2366.

Circle No 388

BUS STIMULATOR

- *Allows you to generate VME Bus interrupts and bus requests*
- *Stimulates legal or spurious bus conditions*

The CVMEBS1 bus stimulus module allows you to excercise VME Bus-interrupt and bus-arbitration functions by generating bus signals that are not easily generated by other means. You can also use it to control generation of the VME Bus ACFAIL, SYSRESET, and SYSFAIL signals. By operating pushbuttons on the module's front panel, you can generate a VME Bus interrupt on any one of the VME Bus's seven interrupt levels or generate a bus request on any one of the four bus-request lines. For interrupts, you can also set the eight LSBs of the STATUS/ID that the module places on the bus during the interrupt-acknowledge cycle. During this interrupt-acknowledge cycle, the board simulates a ROAK (release on acknowledge) interrupter. When you activate a bus request, the selected bus-request signal remains active until the board receives a bus grant at the appropriate level —at which point the module asserts BBSY and negates the bus request. In addition to stimulating legal interrupt and bus-request cycles, you can also generate spurious interrupts or bus requests to test the system's response to ghost conditions. When you generate SYSFAIL, SYSRESET, or ACFAIL signals in normal mode, they are automatically cross coupled to simulate normal VME Bus operation. When the module is operating in its "spurious" mode, you can generate these signals individually. $2000.

Concise Technology, 227a Aylesbury Rd, Bierton, Aylesbury, Buckinghamshire HP22 5DS, UK. Phone (0296) 81483. TLX 975646.

Circle No 389

GRAPHICS PROCESSOR

- *Provides Multibus-II systems with 1024×800-pixel displays*
- *Incorporates two 82786 graphics processors*

The FAB210 is a color-display coprocessor card for Multibus-II systems. It includes an onboard 80286 CPU with 32k bytes of onboard RAM and 256k bytes of EPROM, and two 82786 graphics processors that access as much as 4M bytes of onboard video RAM. In noninterlaced mode, the unit can display images at a maximum resolution of

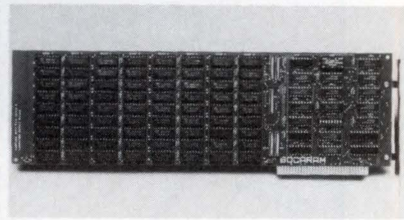
1024×800 pixels. The 8-bit pixels allow you to display 256 monochrome gray scales, or 256 colors from a palette of 16M colors via the onboard color look-up table. The 4M bytes of onboard video RAM can store as many as four separate full-resolution images, and you can transfer video information to the video RAM either via the Multibus-II iPSB bus or via the board's iLBX-II bus interface. The board displays video-camera images and can overlay these images with graphics information. The video output takes place via 75Ω RGB analog outputs and two TTL video outputs. From Fr Fr 36,000.

Centralp Automatismes, 16 rue Gabriel Peri, 92120 Montrouge, France. Phone (1) 42533617. TLX 632380.

Circle No 390

MEMORY BOARD

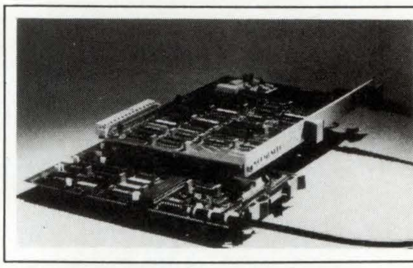
- *Provides 2M bytes of EMS 4.0 memory*
- *Parity-checked RAM uses 150-nsec, 256k-bit RAM chips*



The BocaRAM/30 memory board for the IBM PS/2 Models 25 and 30 or compatible computers comes with 0k, 256k, 1M, or 2M bytes of RAM. Its software drivers support the Lotus/Intel/Microsoft (LIM) expanded memory specification (EMS) version 4.0. The software includes a print spooler, an installation program, and diagnostics. The LIM version 4.0 expanded memory is compatible with all LIM/EMS version 3.2 memory software. The priority-checked memory is composed of 150-nsec, 256k-bit RAM chips. The board measures 13.25×4.2 in. and requires 5V at 1A typ. 0k-byte version, $175; 256k-byte version, $225; 1M-byte version, $345; 2M-byte version, $545.

Boca Research Inc, 6401 Congress Ave, Boca Raton, FL 33487. Phone (305) 997-6627. TLX 990135.

Circle No 391



LAN BOARD

- *Utilizes the SMC 9026 VLSI controller for connection to ArcNet*
- *Provides 2k bytes of dual-ported RAM*

The V-ARCO2 LAN interface board allows integrators to connect with ArcNet LANs. The board is built around the SMC 9026 VLSI controller and functions as an intelligent slave in a VME Bus system. It implements the J1 interface of the VME specification Rec C1. The interrupt level, interrupt vector, and base-address addressing range are jumper selectable. The board has 2k bytes of dual-ported RAM, which provide four 512-byte packet buffers. The board uses industry-standard ArcNet cable transceivers. The unit connects to the network cable either by a BNC connector on its front panel or via a coaxial lead to a connector on its chassis. $1590.

Comendec Ltd, C&C Marketing, Box 280, Batavia, IL 60510. Phone (312) 879-7003.

Circle No 392

SCHEMATIC CAPTURE

- *Lets you design pc boards and PLDs*
- *Library includes more than 2000 standard parts*

CapFast CF1000 is an entry-level schematic-design software package that runs on the IBM PC, PC/AT, PS/2, and compatibles. The package includes a schematic editor, a symbol editor, a symbol library, netlist extractors, a parts-list program, and a plotting utility. The symbol library contains more than 2000 standard parts in IEEE and ANSI formats. You can create an unlimited number of hierarchy levels and perform multipage schematic editing at any level. Other features include flexible property editing, automatic checking of the electrical design rules, split-screen capability, dynamic panning, and keyboard macros. To run the package, your computer must have an IBM EGA or a compatible display board. $395.

Phase Three Logic Inc, Box 985, Hillsboro, OR 97123. Phone (503) 640-2422. **Circle No 412**

DATA ANALYSIS

- *Lets you acquire, manipulate, and plot data*
- *Allows plotting of 10 dependent variables simultaneously*

KaleidaGraph is a data-analysis program for the Macintosh PC. You can acquire data from a spreadsheet program such as Excel or from a host computer with the aid of a communications program. The data-manipulation functions include statistical functions, least square regression, and linear/normal probability functions. You can save your plots as KaleidaGraph, Pict, or MacPaint documents, or direct the output to a laser printer. A built-in calculator provides the ability to execute programs with as many as 1000 steps, has 100 memory registers, and provides standard scientific-calculator functions. $179.

Peripherals Computers & Supplies Inc, 2457 Perkiomen Ave, Reading, PA 19606. Phone (215) 779-0522. **Circle No 413**

COMPONENT LIBRARY

- *Includes symbols for PC/AT chip sets*
- *Works with P-CAD CAE system*

LIB-2 is a component library that contains symbols and part characteristics for the PC/AT chip sets from Chips & Technologies, Inc (Milpitas, CA). You can use the library with the vendor's P-CAD CAE system. The library and CAE system help you design and lay out PC/AT-compatible products. $450.

Personal CAD Systems Inc, 1290 Parkmoor Ave, San Jose, CA 95126. Phone (800) 523-5207; in CA, (800) 628-8748. TLX 3717199

Circle No 414

COMPARATOR

- *Compares outputs of digital simulation runs*
- *Reports all differences between runs*

SimCompare can compare the outputs of any simulators, regardless of the host machines on which the simulations were run. You can ask the program to report on all differences between the runs, and you can also specify the parameters that interest you and request a report only, for example, on glitches longer than 100 nsec, or on transitions that violate the setup-time rules for the receiving device. You can also specify reporting limits that will help you evaluate best- and worst-case simulation results. The program is particularly useful for comparing your own simulation of an ASIC with the simulation run by the foundry that manufactures the device. The program runs on Apollo computers. $8000.

Logic Automation Inc, 19500 NW Gibbs Dr, Beaverton, OR 97006. Phone (503) 690-6900.

Circle No 415

REAL-TIME ADA

- *Lets you develop real-time software for embedded computers*
- *Provides real-time, multitasking, run-time kernels*

The RTAda Runtime System consists of several integrated modules that achieve the functionality, high performance, and predictable response necessary for real-time embedded applications. The kernel, ARTX, provides the Ada tasking model; system facilities such as queues, event flags, semaphores, and mailboxes; and explicit tasking-control mechanisms. The cross-development tools include validated Ada self-hosted and crosscompilers, a source-level debugger, a global optimizer, language tools, and downloading tools. Depending on host machine and target, from $4000 to $70,000.

Ready Systems, 449 Sherman Ave, Palo Alto, CA 94306. Phone (415) 326-2950.

Circle No 393

FAX PACKAGE

- *Lets IBM PCs send and receive fax messages*
- *Has an optical-character-recognition option*

The PC-Fax package allows you to use an IBM PC/XT, PC/AT, or a compatible computer to send fax messages to, or receive them from, an International Group III fax machine. Alternatively, you can use it to send telex messages or electronic mail. The package can transmit or receive any word-processing document, desk-top-publishing image, or paint-box-system image. You can generate input from the PC's memory or keyboard, from an optional digitizer tablet, or from a hard-copy scanner or fax machine. The fax software can capture and transmit drawings generated by CAD packages. When operating in the normal mode, the package provides 202×98-pixel resolution; when operating in the fine mode, it provides 204×196-pixel resolution. The basic software operates in accordance with International Group III CCITT fax standards, and you can upgrade it to Group IV. The transmission software includes a directory of fax numbers, as well as automatic dialing and redialing facilities. You can program the software to transmit messages during "cheap-rate" periods and to poll other fax or communications systems to determine if there are any fax messages programmed for transmission to your PC's number. The PC can receive fax messages while you're using it for other tasks. The software automatically saves incoming fax messages to disk, and it informs you of their receipt by audio and video prompts. You can then recall messages to the PC's screen and zoom in on them to examine details, or you can output them to a printer or plotter. PC-Fax package, including telephone-line interface hardware, £750; optical-character-recognition package, £295.

Softech Professional Systems Ltd, 9 Tonbridge Chambers, Pembury Rd, Tonbridge, Kent TN9 2HZ, UK. Phone (0732) 362688.

Circle No 394

80386 DEBUGGER

- *Provides real-time breakpoints in software*
- *Can work with CodeView and Symdeb debuggers*

Soft-ICE is a software-based debugging tool for program development under PC-DOS or MS-DOS. It takes full advantage of the 80386 architecture and provides a range of capabilities more commonly associated with hardware debuggers. The debugging tool runs entirely in extended memory, so that the target program has the full 640k bytes of main memory available to it. The debugger allows you to set real-time, hardware-level breakpoints for trigger by I/O port accesses, by interrupts, by reads or writes to specific memory locations or address ranges, or by conditions arising from the target program's execution. The debugging tool traps invalid operation codes and general protection violations that occur during the debugging of the target program. It runs in 80386 protected mode, so a runaway program can't overwrite it. To run the debugger, you need an IBM PS/2 Model 80, an 80386-based IBM PC/AT or compatible machine, or a computer with an 80386 coprocessor card, and your system must possess a Hercules monochrome-display adapter or IBM MDA; an IBM CGA, EGA, or VGA board; or a compatible. $386.

Nu-Mega Technologies, Box 7607, Nashua, NH 03060. Phone (603) 888-2386.

Circle No 395

C CROSSCOMPILER

- *Provides all Kernighan and Ritchie features of the language*
- *Compiles to assembly language for the DSP56000 family*

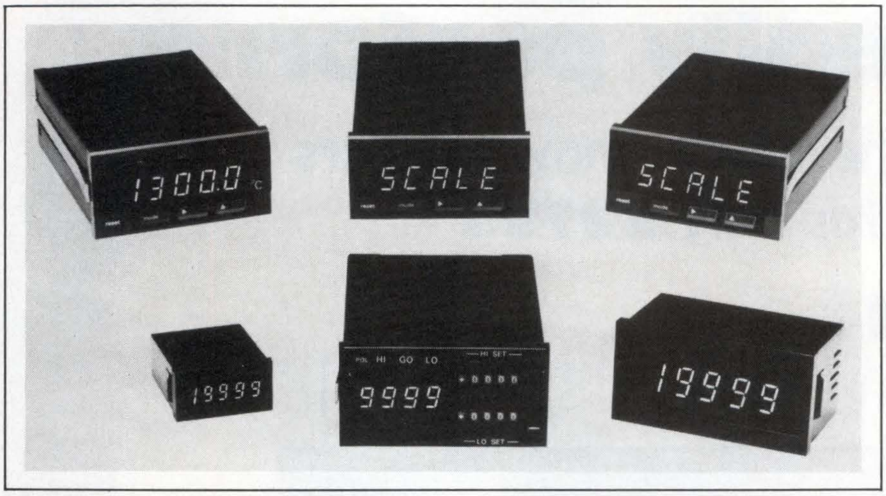
The DSP56KCC is a C crosscompiler that runs on IBM PCs and compatibles, Sun workstations, and VAX/VMS or VAX/Unix machines. The vendor will offer a Macintosh II version soon. The compiler generates assembly-language code for the vendor's DSP56000 family of digital signal processors; you can assemble and link the assembly-language code with the vendor's DSP56000CLAS cross-development tools. The preprocessor performs macro expansion, conditional compilation, and file inclusion. An incremental-compilation feature lets you optimize time-critical sections of your DSP code. MS-DOS version, $709; Unix and VMS versions, $4709.

Motorola Inc, Technical Info Center, Box 52073, Phoenix, AZ 85072. Phone (512) 440-2030.

Circle No 396

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS



DIGITAL PANEL METERS

- *34 models measure and control many variables*
- *Most models fit ⅛ DIN enclosures*

A+ Series digital panel meters comprise 34 models. Most of the meters come in ⅛ DIN cases, though the vendor will provide the meters uncased for OEM applications. The series includes 3½- and 4½-digit ac and dc voltage and current meters with scalable inputs; meter relays; process, temperature, and BCD monitors; a 6-digit counter; and several microprocessor-based instruments. $50 to $900.

Triplett Corp, 1 Triplett Dr, Bluffton, OH 45817. Phone (419) 358-5015.

Circle No 397

SIGNAL GENERATOR

- *Covers 10 kHz to 1 GHz*
- *Provides 13-dBm output*

The 2022C signal generator covers a frequency range of 10 kHz to 1 GHz and provides a 13-dBm output level. The unit includes both an internal modulation source and an external frequency-modulation input. You can use the internal source and the external input simultaneously to achieve composite modulation waveforms. When operating below 100 MHz, the unit specs a 10-Hz frequency resolution; when operating at or above 100 MHz, it has 100-Hz resolution. A standard IEEE-488 interface facilitates calibration. $4989. Delivery, four to six weeks ARO.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401. Phone (201) 934-9050.

Circle No 398

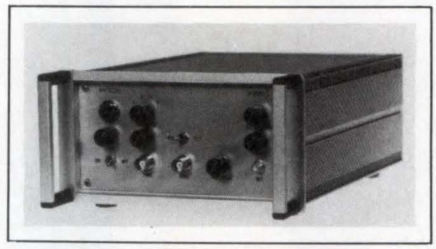
SYNTHESIZER

- *Provides output frequency resolution of 1 μHz*
- *Holds spurious outputs below −100 dBc*

When you supply a 5- or 10-MHz input to the 3031B reference-frequency synthesizer, it produces an output whose frequency differs from that of the input by a programmable amount of ±4 kHz max. If you use a 5-MHz input, you can control the frequency offset with a resolution of 1 μHz; if you use a 10-MHz input, the resolution equals 2 μHz. With a 100-Hz offset, phase noise is −145 dBc. The device features spurious outputs of −100 dBc. You can specify IEEE-488, BCD-TTL, front-panel, or analog-voltage frequency control. $14,950. Delivery, 12 weeks ARO.

Pentek Inc, 10 Volvo Dr, Rockleigh, NJ 07647. Phone (201) 767-7100.

Circle No 399



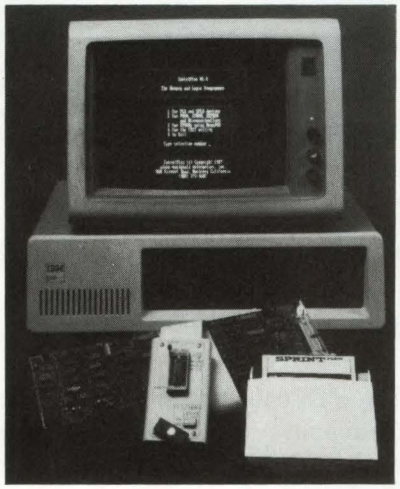
PULSE GENERATOR

- *Produces pulses at rates from 25 to 250 MHz*
- *Holds rise and fall times to 100 psec*

The Model AVNN-1-C pulse generator produces output pulses at repetition rates from 25 to 250 MHz, with a duty factor that you can vary from 30 to 70%. The rise time is 100 psec. Using single-turn controls, you can set the peak-to-peak output amplitude as high as 5V and add an optional, internally generated dc offset. This combination of capabilities enables the unit to drive ECL circuits. The generator provides a sync output for scope triggering; furthermore, you can trigger the generator's output by supplying a 0.3V rms sine wave or a 50% duty-factor square wave. Optionally, you can have the vendor equip the instrument so that you can program the output level, pulse width, and dc offset by applying dc voltages. The unit is housed in a 4×8×12-in. enclosure and operates from 110 or 220V, 50- or 60-Hz power. $2493 to $2973. Delivery, 60 days ARO.

Avtech Electrosystems Ltd, Box 5120 Station F, Ottawa, Ontario, Canada K2C 3H4. Phone (613) 226-5772. TLX 0534591.

Circle No 400



PROGRAMMER

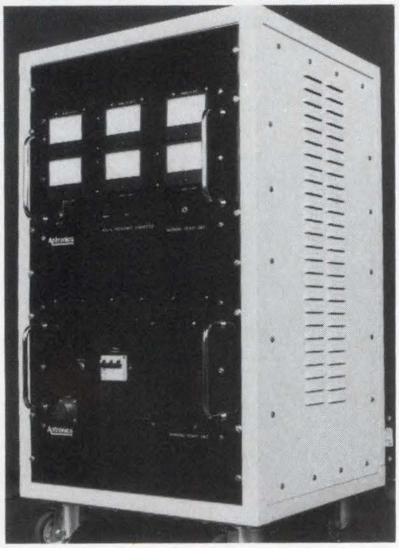
- *Consists of PC bus board and programming pod*
- *Includes PLDASM assembler and programming software*

The Sprint Plus programming system consists of a PC bus card, a 28-pin programming pod, the PLDASM logic assembler, and programming software. These items allow you to turn logic equations (and unprogrammed CMOS, NMOS, or bipolar PLDs) into programmed devices. In addition to logic devices, the product can handle EPROMs, EEPROMs, and bipolar PROMs. Because the unit resides in the host, it does not usurp a serial port, nor does it require you to download code into the programmer. As the company adds new devices to the unit's library, it will provide updates of the software on floppy disk, but no hardware or firmware modifications are scheduled. The programmer handles PLD data as standard

JEDEC files, and PROM data as standard binary or hex files. Before programming a device, the programmer verifies that it is blank; after programming, it verifies the contents. In addition, if a PLD's JEDEC file includes test vectors, the programmer applies them. $1795.

Promac, 800 Airport Rd, Monterey, CA 93940. Phone (408) 373-3607. TLX 882141.

Circle No 401



FREQUENCY CONVERTER

- *Provides a 3-phase, 400-Hz output*
- *Has optional remote-control facilities*

The MPC-643/682 static frequency converter provides a 400-Hz, 3-phase output with a line-to-line voltage of 160 to 200V. It requires a 50-Hz, 380 to 415V supply. The converter has overload, overtemperature, and output short-circuit protection. It also has remote voltage sensing and a soft-start facility. Its options include variable output-voltage control (via a front-panel or remote potentiometer) over the 160 to 200V range, as well as an 8-bit parallel or IEEE-488 interface for digital control of the output voltage. You can also have meters fitted to monitor each output phase. The converter mounts in a standard 19-in. rack and has an 18U-high front panel. From £8200.

Antronics Ltd, Book House, Glebelands Centre, Vincents Lane, Dorking, Surrey RH4 3HW, UK. Phone (0306) 883600. TLX 888941.

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IEEE-488 CONTROLLERS

- *Incorporate coprocessor with HP Basic 5.0 in ROM*
- *Include 8086- or 80286-based PCs*

The HP PC 305 and 308 are turnkey instrument-control systems based on the vendor's Vectra family of MS-DOS-based personal computers. They incorporate a Basic language coprocessor, a plug-in card that includes—in addition to an IEEE-488 interface—a 68000 coprocessor with 512k bytes of RAM separate from the Vectras' system RAM, and ROMs containing the HP Basic 5.0 language. HP Basic is an advanced dialect that supports structured programming constructs and includes a rich set of instrument-control instructions. The coprocessor can utilize system RAM as a RAM-disk. Once you have acquired data from IEEE-488-based instruments connected to the coprocessor card, you can analyze it on the same system with any of the commercially available data-analysis packages that run under MS-DOS on the 8086 or 80286 μP. $3895 to $6695, depending on type of display and whether the system includes a hard disk.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

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- *Provide two independent synthesized frequencies*
- *Reference both outputs to one frequency standard*

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Programmed Test Sources Inc, Box 517, Littleton, MA 01460. Phone (617) 486-3008.

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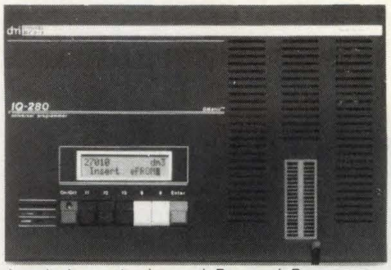

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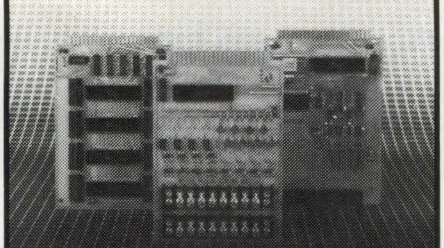

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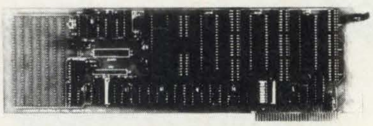

UNIVERSAL I/O

This board has nine 8 bit parallel I/O ports (8255's) and 16 analog inputs. Each analog input has a 0-5 volt range, 8 bit resolution 20 Meg. input impedance. Conversion time is 200 us per channel. This board also has interrupt-timer circuitry, prototyping area. A dip switch is used to select the I/O address (32 are used). The ports interface via 16 pin ribbon cables. This board uses a full size slot. Order Part number 83-064A at $229.95 from

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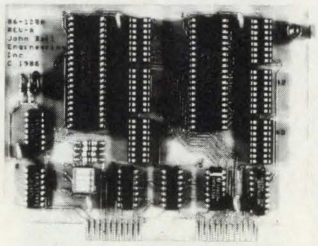

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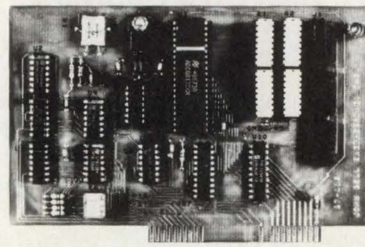

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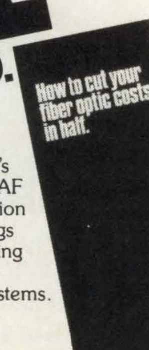

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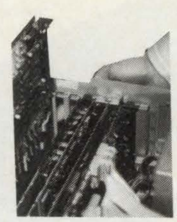

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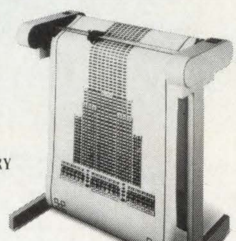

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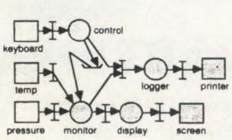

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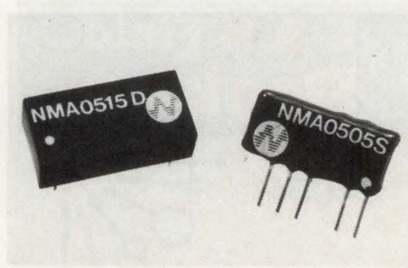

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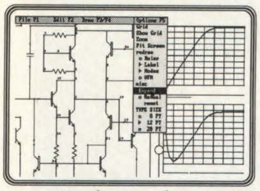

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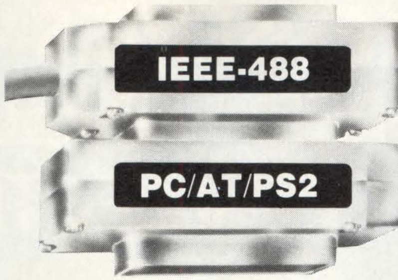

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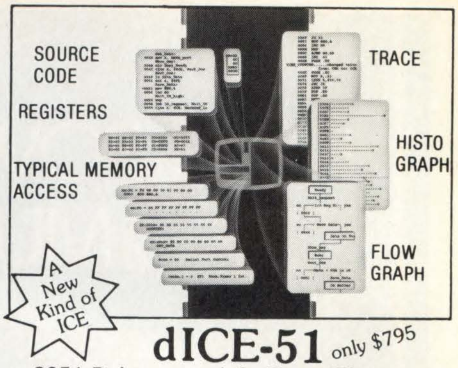

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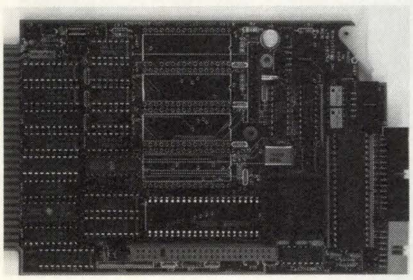

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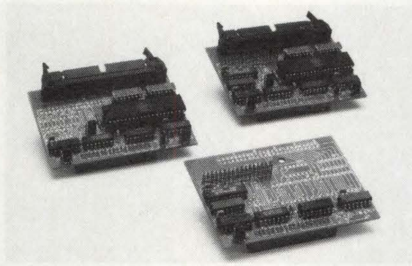

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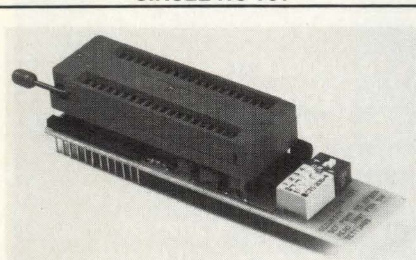

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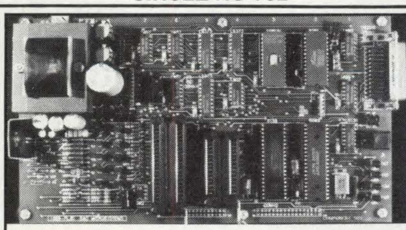

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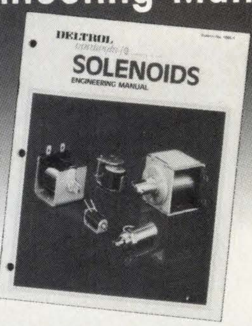

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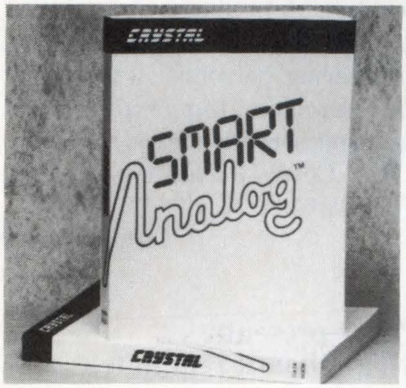

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If you use Spice (simulation program with integrated circuit emphasis), or are thinking of using it, this series can provide you with useful information. *Selecting Hardware for Math-Intensive Programs (Version 87.3)* includes evaluations of 80386-based accelerator boards, 80386-based personal computers, and a comparison of the 80287 and 80387 math coprocessors. It costs $30. *A User's Guide to Spice* allows you to compare the various versions of Spice before buying a circuit-simulation program and costs $40. *A Spice Tutorial* can make circuit design easier. The 100-pg document contains explanations, examples, and problems that illustrate the commands and circuit elements of Berkeley Spice; this manual also costs $40. Finally, *Spice Modeling Notes* shows you how to develop circuit element models using standard laboratory equipment. The price of this 140-pg publication is $55.

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The DPM-10 application note helps clarify your questions about several common terms and problem areas, such as isolated and nonisolated signal source inputs, common-mode voltages, and safety precautions for wiring primary line power to any device. The note provides wiring diagrams and standard formulas for component selection in voltage dividers, attenuators, and shunt circuits. It also guides you in the measurement of high- and low-level voltages, as well as the measurement of signals from resistance bridges, solid-state temperature sensors, and similar devices.

Acculex, 440 Myles Standish Blvd, Taunton, MA 02780.

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Software products for musicians

The vendor's *Musician's Music Software Catalog* contains a comprehensive overview of music software products and musical-instrument digital interfaces (MIDI). It helps you make the best choice for your needs when selecting music hardware and software computer products.

Digital Arts & Technologies, Dept CPR, Box 11, Milford, CT 06460.

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Data for measuring temperature

Designed to facilitate engineering calculations on personal computers, this 5¼-in. floppy disk contains temperature - measurement - handbook data. It highlights the computation of resistance vs temperature tables for resistance temperature detectors (RTDs) and millivolts vs temperature for a variety of thermocouples. It also generates wire tables for metals such as copper, aluminum, platinum, and constantan. Further, it describes specifications for the vendor's line of industrial RTDs and thermocouples and tells you how to determine parts numbers for probes; accessories; and heating, ventilation, and air conditioning products. Available at no cost to system designers and engineering personnel who specify and purchase temperature-measurement sensors and accessories.

RdF Corp, 23 Elm Ave, Hudson, NH 03051.

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Paper presents wiring-board laminates

The reprint of a paper *Printed Wiring Board Laminates for Multiplane Applications,* reproduced from the International SAMPE (Society for the Advancement of Material and Process Engineering) Electronics Conference Series, discusses a bendable laminate for printed wiring boards. It describes the material Bend/flex, a nonwoven fiber-reinforced epoxy, which can be postformed after printing, etching, and populating with components. The document details the material's physical and electrical properties and sums up preliminary results for surface-mount components and plated-through holes.

Rogers Corp, 1 Technology Dr, Rogers, CT 06263.

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Applications for dual-channel analyzers

The 32-pg booklet *A World of Applications* deals with 12 applications where you can use a dual-channel analyzer to identify and help you solve engineering problems. In the area of acoustics, it focuses on sound-intensity measurements and architectural acoustics. The section on electroacoustics reviews transducer measurements and sound-reinforcement systems. It also provides an analysis of servo systems and materials. Finally, it outlines how dual-channel analyzers can assist you in college courses.

Bruel & Kjaer Instruments Inc, 185 Forest St, Marlborough, MA 01752.

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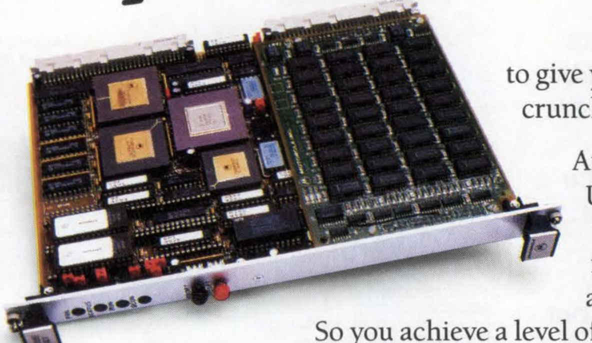

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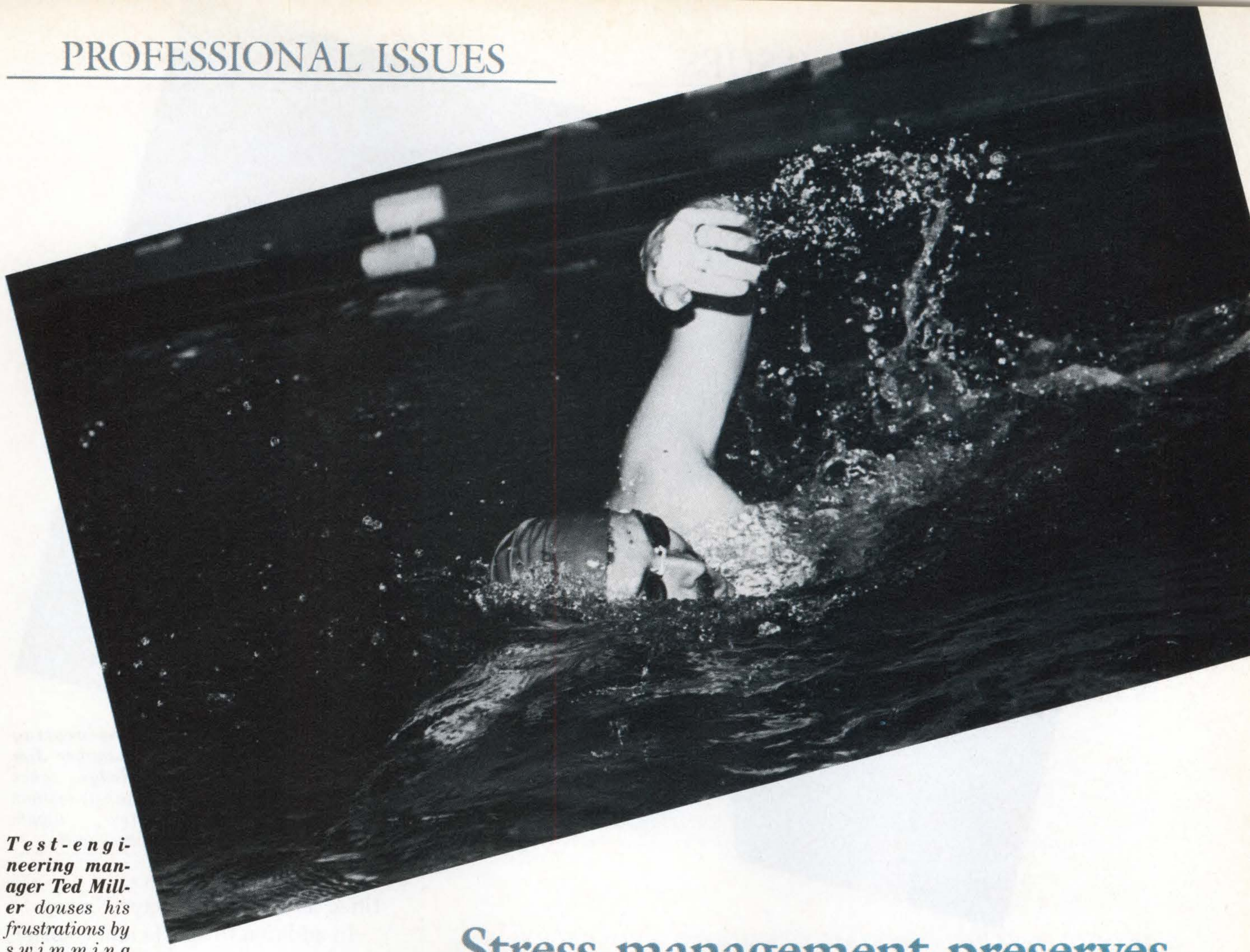


***Test-engineering manager Ted Miller** douses his frustrations by swimming laps several times each week.*

Stress management preserves mental and physical health

Deborah Asbrand,
Associate Editor

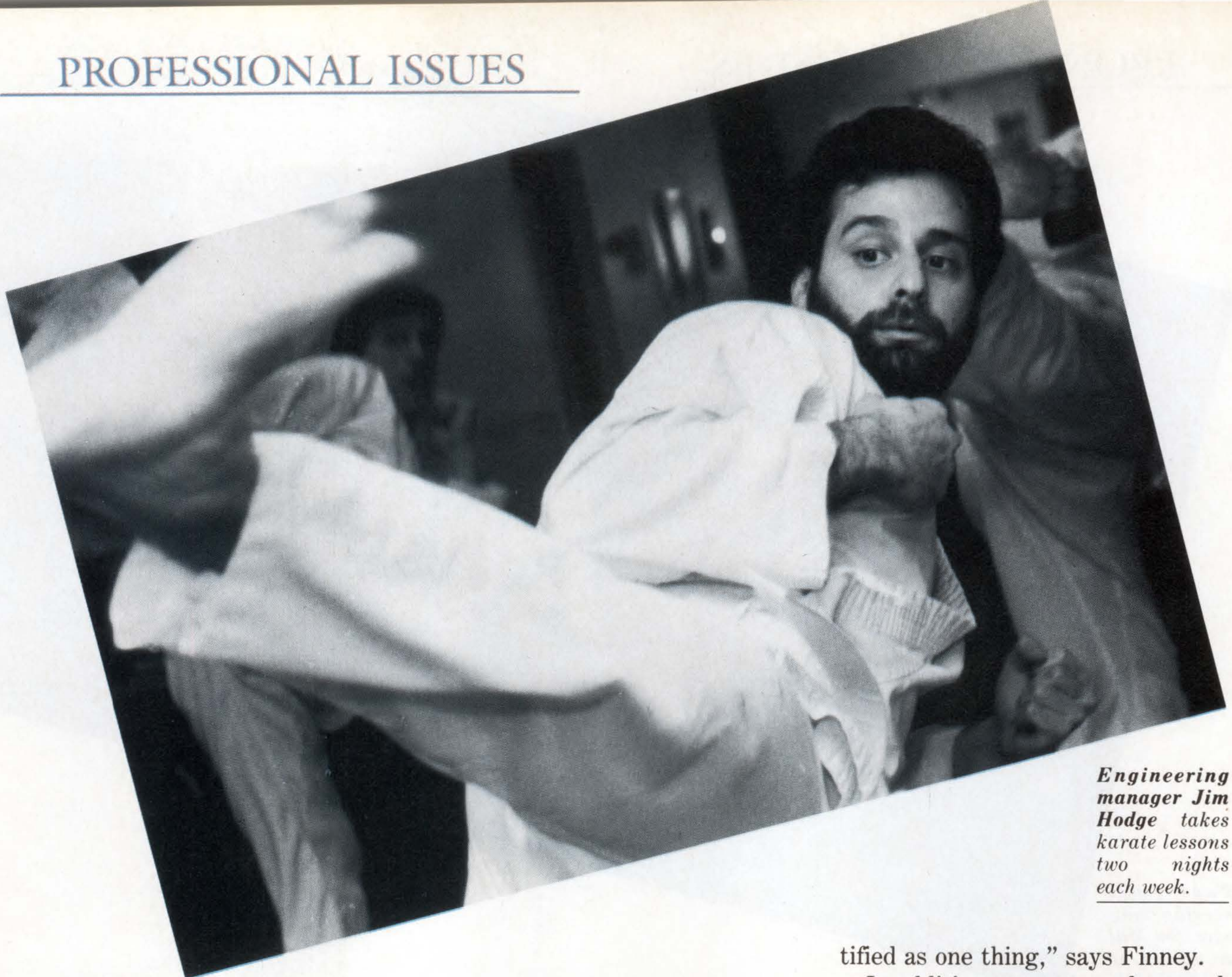
It happens all too often. A company sets ambitious timetables for project completion. Parts arrive weeks or months late. Managers insert last-minute design changes. To conclude a project on deadline, frantic engineers work extra hours, most of them unpaid.

Physical problems, such as throbbing temples and aching backs, usually result from the emotional pressures in the workplace. Employees describe themselves as "stressed out" and "maxed out." When the going gets really tough, they're "stressed to the max." "It's like being in a frying pan," says Ted Miller, a test-engineering manager for Teradyne (Boston, MA). "You feel like you're sizzling."

But while people under stress usually share a deep frustration and a long list of physical aches, the causes of those ailments vary from person to person. The same experience that reduces one person to a heap of frazzled nerves leaves another person cool and ready for more. "Look at the people on a roller coaster," says Paul Rosch, director of the American Institute of Stress (Yonkers, NY). "At the back you see the people holding on tight who can't wait to get off. In the front seats are the wild-eyed thrill seekers with their arms up in the air."

Just as stress defies definition, at least from a scientific point of view, so does a cure for it. Antidotes for stress are highly individualized. Some work out their frustrations best through physical exertion; others prefer the quieting, tranquil processes of meditation, yoga, or biofeedback. But in addition to finding quick relief, people need to develop a long-term plan for reducing stress. Knowing how to deal with tension can benefit a person's career as well as his or her health: "The secure, peaceful person is much more successful than the person who looks stressed," says Jean Hollands, a Mountain View, CA, consultant and author of the book, *The Silicon Syndrome—How to Survive a High-Tech Relationship.*"

Engineers aren't the only ones who are feeling the heat. In fact, the at-wits-end feeling, once expressed only by those willing to risk being labeled weak or incompetent, is being voiced loudly in all industry sectors. Employees are reporting more stress-related illnesses, and



Engineering manager Jim Hodge *takes karate lessons two nights each week.*

that's costing companies more money in lost work time and medical costs. Employees are also filing suits against employers whom they believe have caused inordinate amounts of stress at the workplace.

To protect themselves, more companies are trying to help their employees. They're developing stress-management strategies that teach workers how to handle on-the-job tensions as well as the personal problems that they carry into the workplace. Implementing such programs can be a difficult step to take. Although stress has shed much of its image as a taboo subject, many businesses have mixed feelings about admitting that their employees are under stress. As a result, some prefer euphemistic names for stress management. "Companies like it couched in different terms—motivational training, relaxation training, or conflict resolution," says Hollands.

Nevertheless, the number of employee-assistance programs (EAPs) has shot up 25% in five years. EAPs recognize stress as a full-fledged health hazard, and the best programs offer preventive measures in the form of physical-fitness programs and company-sponsored counseling for workers with financial, legal, psychological, or family problems.

At Hughes Ground Support Systems in Fullerton, CA, 13,000 employees can participate in outdoor recreational facilities and an intramural sports league, and they can consult two full-time counselors. Most employees who visit the counselors' offices have problems with alcohol or drug abuse and marital and family problems, says Mary Lou Finney, assistant manager of employee counseling and a counselor at the Fullerton facility for six years. Usually, individuals have a combination of problems that they need help with. "It's rare for someone to come in with a problem that's easily identified as one thing," says Finney.

In addition to sports and counseling, a monthly seminar on diffusing job stress is among the most popular on-site courses the company sponsors. The 40 employees who fill each session watch a 22-minute videotape narrated by the company's physician and then practice such stress-reducing techniques as stretching, fist clenching, abdominal breathing, and progressive muscle relaxation (see **box,** "Stress reduction for the desk-bound").

Busting loose

Whether it occurs in the form of a brief, imaginary excursion to a balmy South Sea island or through a strenuous game of basketball, some method of escape from stress is critical to an individual's physical and mental health. Indeed, the illnesses that result from unchecked stress read like a litany of human suffering: Hypertension, headaches, backaches, stomach disorders, skin rashes, and infertility are all at times attributable to tension.

Engineers respond to daily pressures in a number of ways. Ted Miller douses his frustrations by swimming in a pool that's a short walk from Teradyne. "I really pound the water and swim away my frustrations," says Miller, age 29. On the days that he doesn't swim, he runs five miles. He's also played basketball in the company's intramural league. The high-energy hollering in the games reflects much more than the participants enthusiasm, he says.

Jim Hodge, 32, a senior principal member of the technical staff at Concurrent Computer Corp (Tinton Falls, NJ), keeps his frustrations under control by taking karate classes two nights a week. He also maintains a careful diet and takes vitamins. Photographs of peaceful mountain scenes hang on his office walls. When he arrives at work each day, he switches on a small cassette deck beneath his desk that emits the soothing strains of Handel or Mozart.

On the hectic days when he works through lunch, Hodge reserves at least five minutes for some relaxing activity—taking a short walk or just leaning back in his chair and unwinding. The leisure action can take any form as long as it's unrelated to work. "It's definitely not looking at logic diagrams," he says.

The root of most problems

The most trying encounters in any engineering department, however, generally have nothing to do with sloppy diagrams or late parts. The source of greatest conflict is working with people. Indeed, mastering the social and political landscape of a company can require as much effort as solving differential equations.

Design engineer Nancy Stevens, 42, says that only about half of her work at her Carlsbad, CA, employer requires use of her engineering know-how. The rest, she says, taps talents she honed raising two children before she went into engineering 10 years ago. "At least 50% of what I do is organizational and requires me to focus my skills. Most of that I learned from being a housewife."

In fact, engineers who lack Stevens's organizational and diplomatic skills are at a distinct disadvantage in the workplace. "The nontechnical aspects of a company—the social and political issues—are really half the battle," says James Rago, a San Francisco consultant. A 1984 survey of 249 Canadian engineers found that organizational factors caused the greatest stress to the engineers. Among the engineers surveyed, those working as first-level supervisors—the middle managers—reported the most tension.

The most effective way to manage stress, experts say, is through cognitive restructuring. The lay-term translation? Instead of trying to change the people and events around you, focus your energies on altering the way you respond to them. "Stress isn't going to go away, so people need to improve their way of handling stress through their listening and communications skills," says John Kennedy, director of the San Jose, CA, office of Human Affairs International, which oper-

Stress reduction for the desk-bound

Two exercises that you can perform at your desk trigger the body's parasympathetic nervous system, lowering blood pressure and slowing the heart beat. These physical reactions can temporarily relax you.

Fist-clenching. Make a fist and squeeze it tightly for a count of three. Then outstretch your fingers and palm for another count of three. Repeat several times.

Abdominal breathing. Forget all those times you walk around trying to hold your stomach in. Instead, take a deep breath and extend your abdominal muscles as you inhale. Slowly exhale and feel your body relax. Abdominal breathing, as opposed to breathing only through your chest, relaxes your entire body.

Books to read for more information

Role Stress—How to handle everyday tension, by Stuart Palmer. Prentice-Hall Inc, Englewood Cliffs, NJ, 1981.

Stress Management—A comprehensive guide to wellness, by Edward Charlesworth and Ronald Nathan. Atheneum, New York, 1984.

The Joy of Stress, by Peter Hanson, MD. Andrews, McPeel & Parker, Kansas City, MO, 1985.

The Relaxed Body Book (a companion book to the PBS series "Bodywatch"), by the editors of *American Health* magazine. Doubleday & Co, Garden City, NY, 1986.

Calm Down—A guide to stress and tension control, by F J McGuigan. Prentice-Hall Inc, Englewood Cliffs, NJ, 1981.

Total Relaxation—The complete program for overcoming stress, tension, worry and fatigue, by Frederick Lenz, MD. The Bobbs-Merrill Co Inc, Indianapolis/NY, 1980.

ates employee-assistance programs on a contractual basis.

Long-term payoffs

Engineers who've taken the time to develop their business acumen say the benefits have been well worth their efforts. Miller recently capped three and a half years of night school with a master's degree in business administration from Boston University. The courses he took in organizational behavior have improved his ability to manage a project smoothly, he says. "When you come across engineering problems, you have the training to solve them. But when there are problems on your team, and you don't have the tools to solve them, you get very frustrated."

While working at a "panic pace" on a 16-month project, Hodge realized that his success in the position required a finesse that he didn't have in working with people. "I knew I needed some pointers," he says. He read books on management, self-esteem, and motivation. He also put to use his 30-minute commute listening to cassette tapes on the same subjects.

The same experience that reduces one person to a heap of frazzled nerves leaves another person cool and ready for more.

The result of his self-education, Hodge says, is a better understanding of how he can help the engineers on his projects work together. His sharpened management skills also make him a more reliable engineer. "When I was younger, I was more prone to get into trouble with people. I sometimes felt I had to blame someone else for my problems." Now, he says, he's aware of his own strengths and limitations.

Most engineers have little trouble developing "people skills." Once they are convinced of the need to develop such skills, they already possess the problem-solving muscle needed to acquire new skills, says Richard Mayer, manager of human resources for the Battelle Pacific Northwest Laboratory in Richland, WA. "Engineers get into problem solving," he says. "They want to make things better." And a little education goes a long way toward reducing the emotional frustrations in engineering. **EDN**

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May 26	May 5	CAE, Software, Sensors/Transducers	
June 9	May 19	CAE, Analog ICs, Test & Measurement	Closing: May 29 Mailing: June 16
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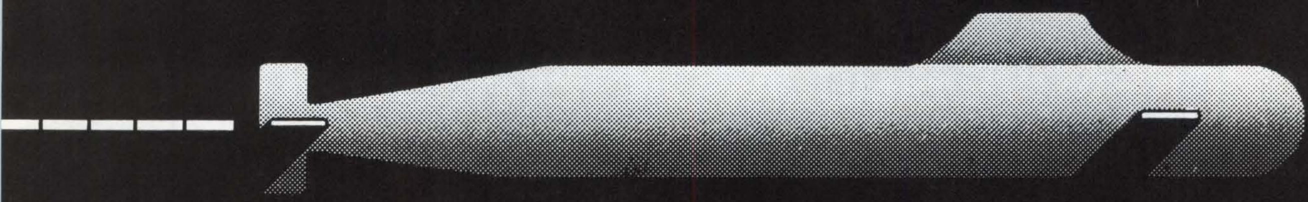

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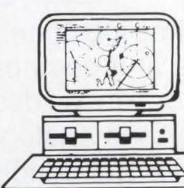
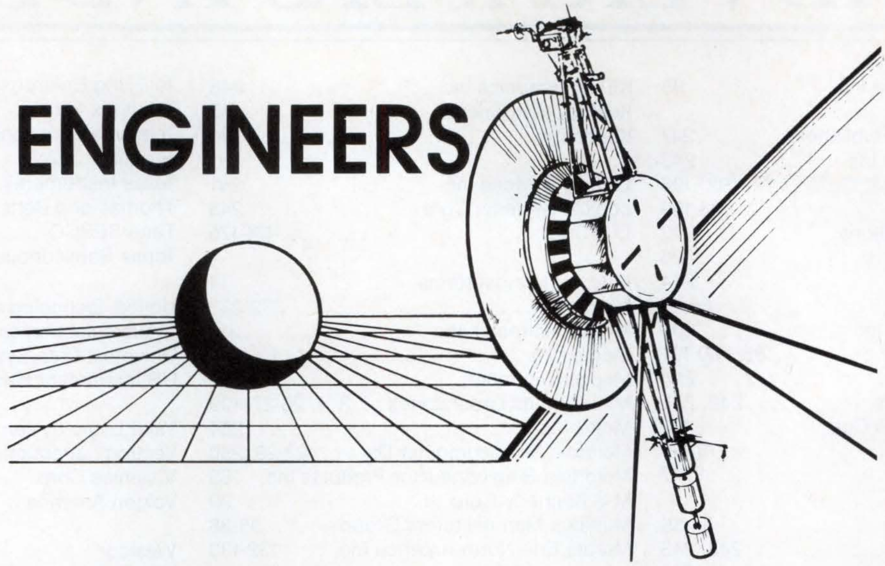


LORAL
Information Display Systems

ENGINEERS



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EDITED BY CYNTHIA B RETTIG

Expert systems will enter US business market via DBMSs

Expert systems may well make their first major mark in the US business market through database management systems (DBMSs), according to the *Intelligent Systems Analyst*, a publication of Richmond Research (New York, NY). Although databases constitute a primary computer application, they are unwieldy and often difficult for end users to master. Thus, the size of databases inherently invites the use of expert systems. Expert systems are most useful in situations where data abounds—and where it sometimes overwhelms conventional database management.

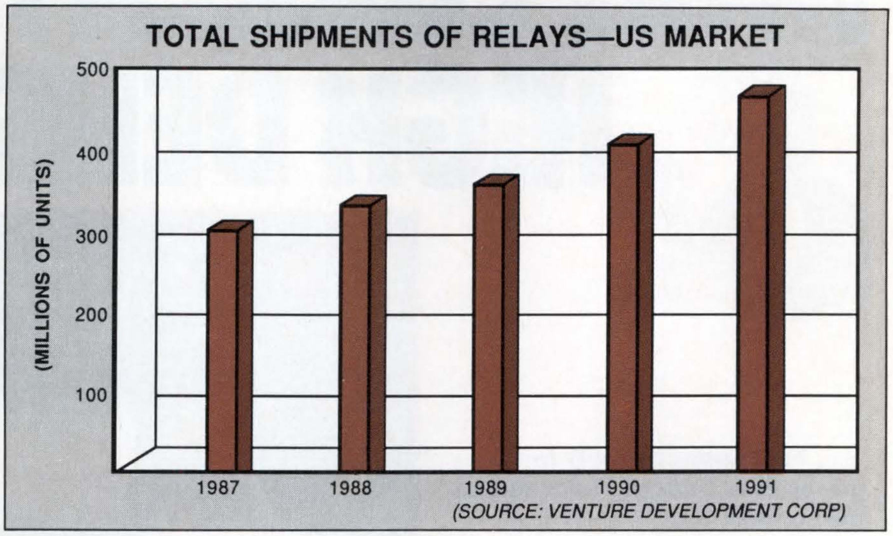
Recently, an increasing number of companies have become concerned with connectivity, integration, and embedded expert systems. Whereas some companies are moving into these areas by purchasing companies that develop expert tools, some software vendors have set up their own R&D teams to develop expert systems in house. Other companies have been entering alliances and joint ventures to meet the challenge of integrating expert systems into database management.

Richmond Research concludes that because IBM, whose mainframes store more than 80% of all existing database files, has put integrated SQL (Structured Query Language) into its new line of desktop computers, the mating of expert systems with DBMSs in the near future seems inevitable. In the personal-computer area, expert systems developed as shells with no outside reference are becoming obsolete as systems that facilitate access to specific databases begin to appear.

Several types of software could result from this trend in AI (artificial intelligence) applications. The implementation of intelligent interfaces is one. In this case, natural-language front ends that use adaptive interface approaches and aid the user in fathoming uncertain requests could play a significant role in improving database management. Intelligent back ends also present opportunities. Such software would analyze information stored in databases and discern patterns that, in turn, could also improve basic management techniques.

Another option involves reality checking—that is, solving the problems that occur when people enter inaccurate data. Expert systems could check for inconsistencies and maintain the integrity of database systems by indicating when totally illogical information or numbers are entered. An even more far-reaching application is the use of expert systems to facilitate the retrieval of information from among incompatible databases. The use of AI in this manner could hasten advances in interconnectivity.

The application of AI to database system management has just begun—and has begun slowly at that. But software developers may uncover great opportunities by considering how AI can fit into their products. And, conversely, database users should begin figuring out how intelligent databases could influence their businesses.



Relay market to gross $1.5B by 1991

The US market for relays should enjoy a steady 9% annual growth rate over the next few years. The estimated value of the 1987 market is $1 billion; by 1991, its value should reach $1.5 billion, according to Venture Development Corp of Natick, MA. A recent study conducted by the market research firm shows that 10 vendors account for 50% of the total relays shipped and that a majority of these companies derive 50 to 100% of their relay revenues from military customers.

In alphabetical order, the ten principal vendors are Aromat, Clare Division of General Instrument, Deutsch, Genicom, Hi-G/Nytronics, Leach, Omron, Siemens/Potter and Brumfield, Struthers-Dunn, and Teledyne Relays. Makers of military relays generally produce miniature, sealed, electromechanical relays of the TO-5 or crystal can type. Such relays resist high levels of shock and vibration and are very reliable in harsh environments. But they are also quite sophisticated and highly specialized, which is why so few companies have elected to compete in this large segment of the US relay market.

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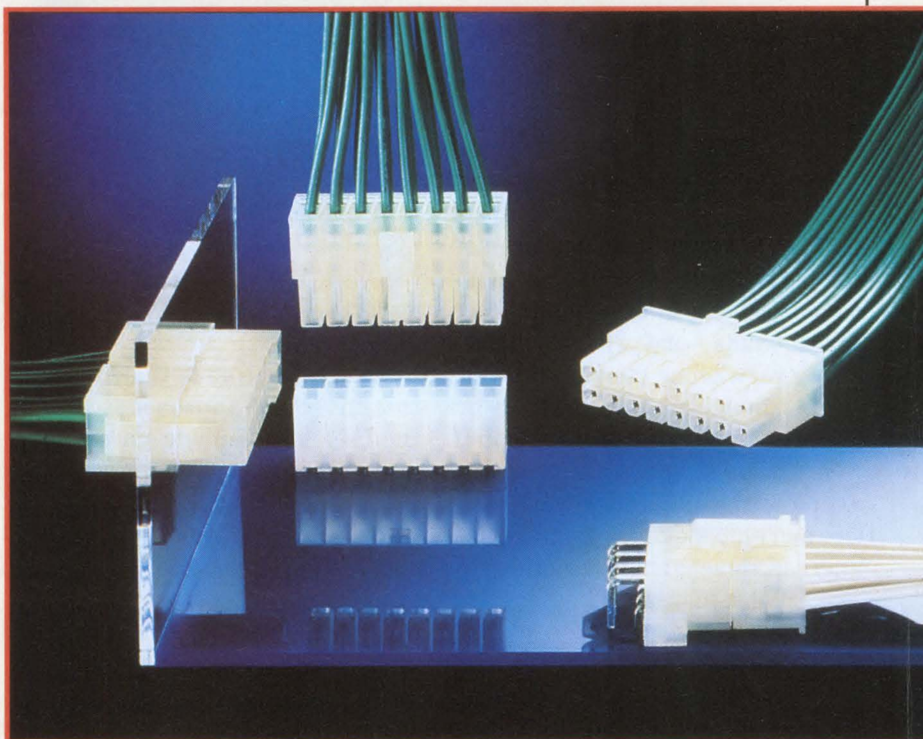

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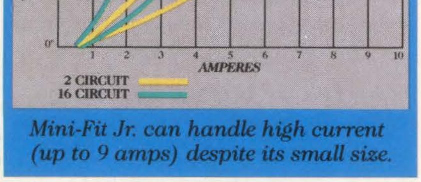

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