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APRIL 30, 1987

EDN

SPECIAL ISSUE:
Communications technology

Token-ring controller

Transformer SLICs

LAN analyzers

ASIC packages

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

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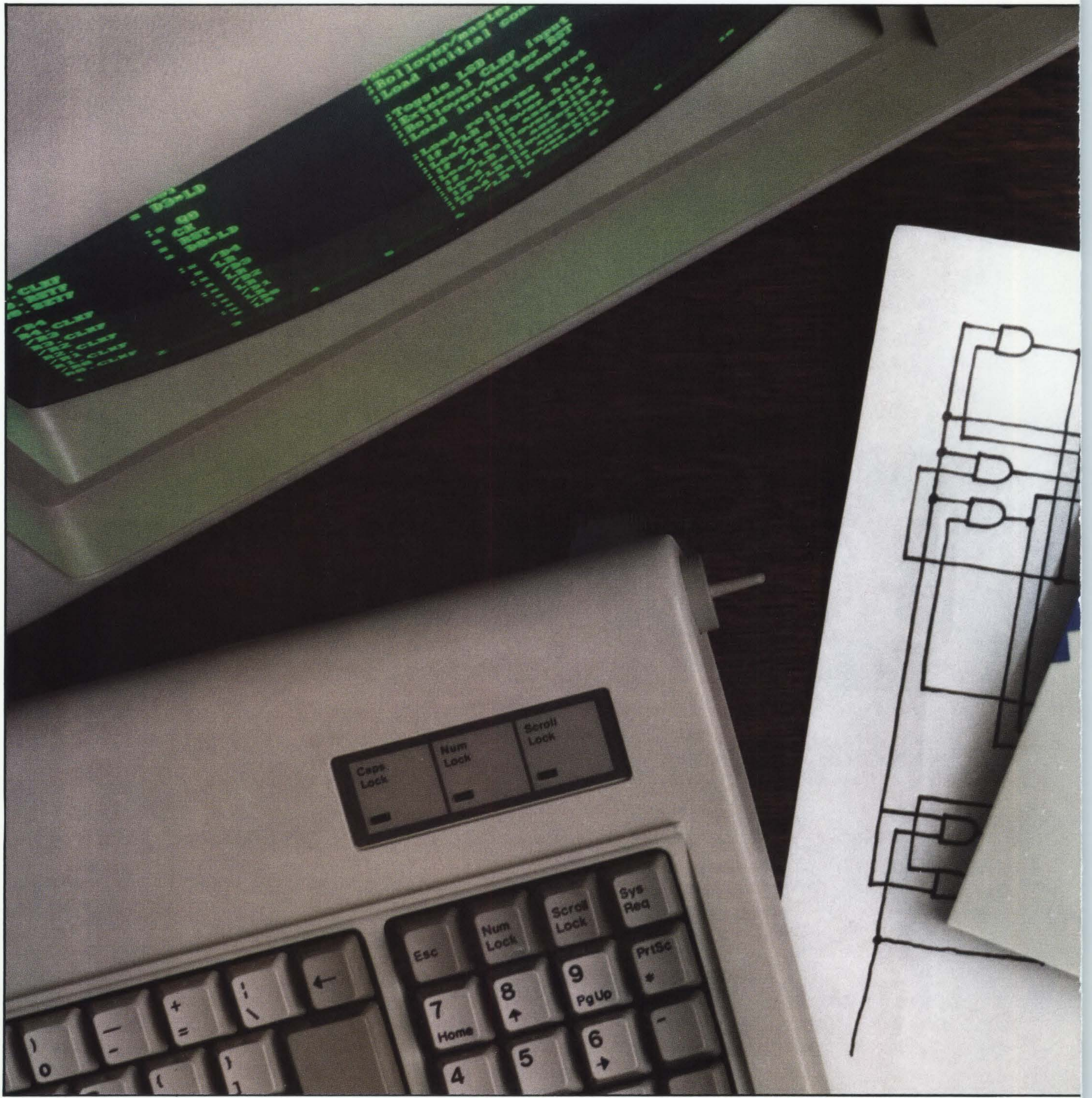


Save your system.

Standards Update

EMISSIONS CRACKDOWN— INSIDE THE FCC

It began in August, 1985, with a one million dollar seizure at Seequa Computer, followed with a crackdown on microcomputer manufacturers (March, 1986). Then in April, the FCC swept through Comdex, levying more than $250,000 in fines. The ominous nature of these actions by the FCC to enforce its computer emissions standards has left the industry wondering "What's next?" According to the leading laboratory in the field, Dash, Straus & Goodhue, Inc., of Boxborough, Massachusetts, it will be a move by the FCC to use its own Laurel, Maryland, laboratory to test mass marketed PCs to see who's non-compliant. The full range of FCC penalties, fines, seizures and arrests, could follow. In addition, the FCC has begun checking Customs files to see if the required FCC "740" form has been included. Failure by importers to file can result in a host of Customs related penalties in addition to the FCC's.

Help is on the way, however, from Dash, Straus & Goodhue (617 263-2662), the Northeast's largest testing, research and development firm dedicated to EMI, telecom and safety compliance. Customers can call DSG and receive, over the phone, a commitment to have a device tested, modified (if necessary), retested and verified within a guaranteed time for a guaranteed rate. DSG is an NBS accredited laboratory for emissions and telecommunications testing.

Circle Reader Service No. 2 for Dash, Straus & Goodhue.

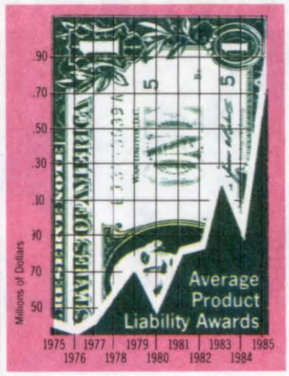
IS DDS THE NEXT TARGET FOR THE FCC?

Since it issued its Third Report and Order, Docket 81-216, in November of last year, the FCC has required nearly all manufacturers of Digital Data Systems to register their designs with the FCC. This includes Channel Service Units (CSU), Network Channel Terminating Equipment (NCTE), and nearly any device that interfaces with T1 or subrate lines. Also included are devices that encode *analog* signals, even though they interface through NCTE or CSU. Some manufacturers have been slow to comply, and their competitors have filed charges. The FCC has responded, issuing forfeitures to three manufacturers based on a complaint by Verilink.

Registering equipment for DDS connection is tricky. One lab proficient in the field is Dash, Straus & Goodhue, Inc., of Boxborough, Massachusetts. As an extra plus, the firm is one of the few labs also approved by the Canadian Department of Communications and can arrange for approvals in Canada as well.

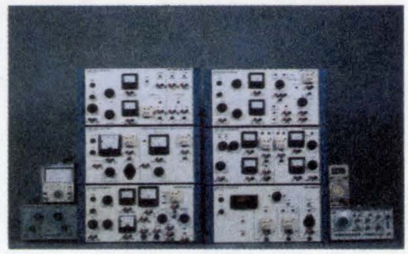
PRODUCT SAFETY— REFORM GAINS BUT LISTING IS BEST

Efforts to reform product liability laws have made slow gains in Congress. The liability Tort Reform Bill S.2760 has passed the Senate Commerce Committee 10 to 7. Basically, it encourages settlement by requiring manufacturers to make a reasonable offer in settlement prior to trial. If not accepted, the injured party's claim for pain suffering is limited to $250,000. But progress and reform is slow and sure to run into opposition in the House. The best bet to hedge



against lawsuits may be UL® listing and CSA® certification. While not a complete defense, failure to meet standards could leave a manufacturer with practically no defense in cases of shock or fire hazards. These and other worldwide safety approvals can now be obtained through one company, Dash, Straus & Goodhue, Inc. DSG can design, test, and coordinate submittals of products for UL, CSA, and West German approvals, often handling them simultaneously. Final tests carried out by these organizations are coordinated through DSG.

NEW INSTRUMENTS SPEED COMPLIANCE



An integrated workstation designed for the complete evaluation of telephones, modems, PBXs etc. for compliance with FCC Part 68, DOC CS-03 and EIA standards is now available from Compliance Design Inc. (617 264-4668). The Workstation makes setting up Part 68 laboratories practical for those manufacturers who wish to avoid heavy independent laboratory testing fees. The Workstation has become especially popular for manufacturers since they now have to meet the FCC's requirement of a six-month recheck on all equipment previously registered.

To ensure EMI compliance, CDI also makes available the famous Roberts Antenna.® The antenna is known for its near lossless receive characteristics and is identical to those used by the FCC for 25 years. Now an industry standard, the company guarantees that any reasonable site can meet the FCC's critical site attenuation requirements of OST-55 by using these antennas. In fact, as part of a package, CDI's engineers will test any customer's site and file it with the FCC, a prerequisite to using it for EMI testing. The antenna was designed by Willmar Roberts, former Assistant Chief Engineer of the FCC's laboratory in Laurel, Maryland. It is available exclusively from Compliance Design.

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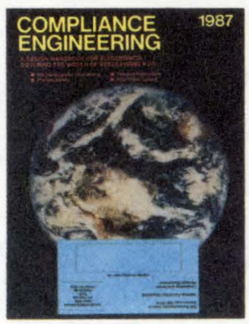
THE BEST *IS* AVAILABLE—FOR FREE!



The industry's standard handbook on EMI, ESD, telecom and safety, Compliance Engineering 1987 covers specifications and methods of engineering for Safety, EMI, ESD, and Telecom compliance. With the need to comply with these specifications universally recognized, engineers have sought out, but been unable to find, authoritative sources for issues related to designing for compliance. Now in Compliance Engineering, separate sections covering EMI, safety, telecom and ESD give a step-by-step approach to control and compliance. The 1985–86 edition drew rave reviews from its readers. You can receive the 1987 issue (available in January, 1987) free of charge just by circling the Reader Service Number below.

For *COMPLIANCE ENGINEERING 1987*, circle Reader Service No. 80.

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Min. Pass Band (MHz) DC to	10.7	48	60	98	140	190	270	400	520	580	700	780	900
Max. 20dB Stop Frequency (MHz)	19	70	90	147	210	290	410	580	750	840	1000	1100	1340

Prices (ea.): P $9.95 (6-49), B $24.95 (1-49), N $27.95 (1-49), S $26.95 (1-49)

HIGH PASS **Model** *HP-		**50**	**100**	**150**	**200**	**300**	**400**	**500**	**600**	**700**	**800**	**900**	**1000**
Pass Band (MHz)	start, max.	41	90	133	185	290	395	500	600	700	780	910	1000
	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	190	290	365	460	520	570	660	720

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*Prefix P for pins, B for BNC, N for Type N, S for SMA *example:* **PLP-10.7**

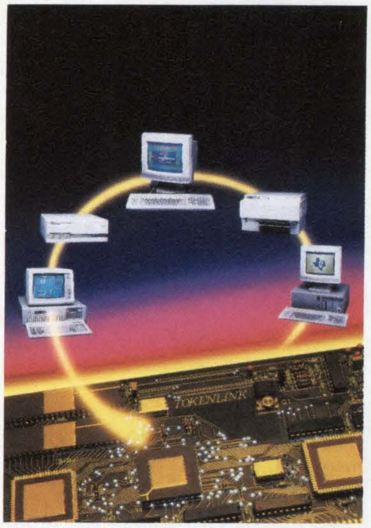
C105 REV. B

Volume 32, Number 9

EDN

April 30, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Encoder and protocol ICs are not the only chips you need to implement a local-area network: Transceiver ICs provide the link to complete an IEEE LAN. See pg 130. (Cover concept and design by Mary Ann Toperzer and David Neal; photography by Joseph Savant; photo courtesy Texas Instruments)*

DESIGN FEATURES

Continued on page 7

VBPA ABP

EDN®(ISSN 0012-7515) is published 38 times a year by Cahners Publishing Co, a Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158. William M Platt, President; Terrence M McDermott, Executive Vice President; Jerry D Neth, Vice President of Publishing Operations; J J Walsh, Financial Vice President/Magazine Division; Thomas J Dellamaria, Vice President Production & Manufacturing; Frank Sibley, Group Vice President. Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer; Robert L Krakoff, Executive Vice President. Circulation records maintained at Cahners Publishing Co, 270 St Paul St, Denver, CO 80206. Second class postage paid at Denver, CO 80202 and additional mailing offices. Postmaster: Send address changes to EDN®, 270 St Paul St, Denver, CO 80206.

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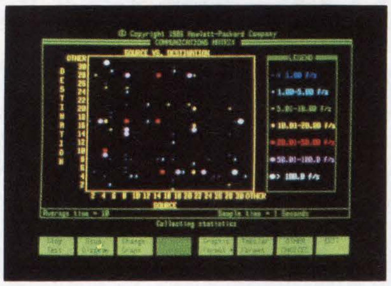

***You can use a LAN physical tester** or protocol analyzer for measuring the performance of a new network-protocol software release, resuscitating a crashed network, or tuning a LAN for peak performance (pg 59).*

Continued on page 9

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EDITORIAL 51

A new consortium has a chance to revitalize US manufacturing if government stays out of the way.

NEW PRODUCTS

PROFESSIONAL ISSUES 285

Widespread practice of unpaid overtime levies burden on salaried engineers.—*Deborah Asbrand, Associate Editor*

LOOKING AHEAD 305

Market for linear-proximity, displacement sensors to grow. . . "Moderate" growth forecast for semiconductors in 1987.

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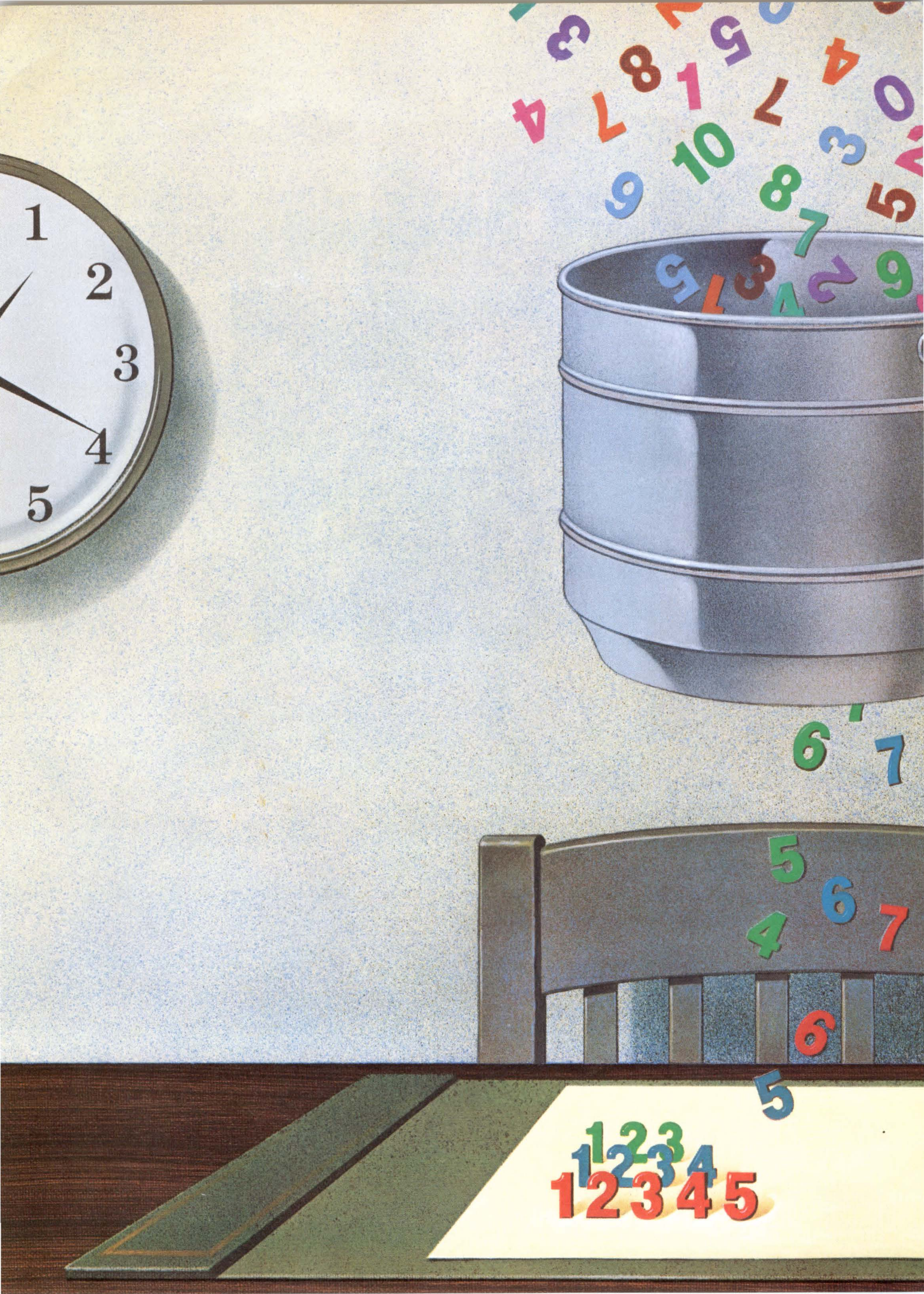

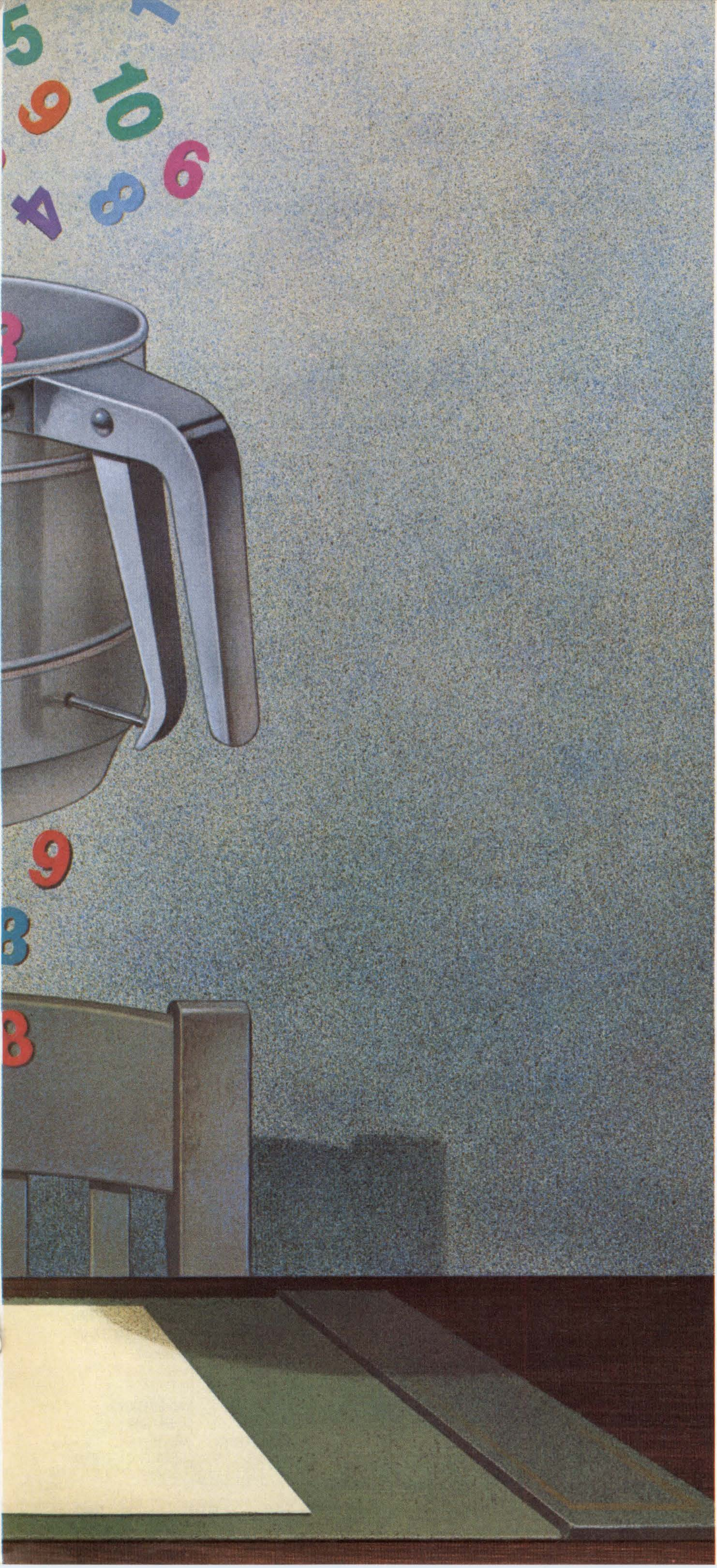

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MB81C75 -25, -35 16Kx4 (w/$\overline{OE}$)
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MB81C79 -45, -55 8Kx9
MB81C78A -35, -45 8Kx8
MB81C78 -45, -55 8Kx8
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MB8464 -15L/LL 8Kx8
MB8464A -10L/LL 8Kx8
MB8464A -12L/LL 8Kx8
MB8464A -15L/LL 8Kx8
MB8464A -80L/LL 8Kx8
MB8464A -10W, -15W 8Kx8
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MB8167 -35, -45 16Kx1
MB8167 -45W, -55W 16Kx1
MB81C67 -35, -45 16Kx1
MB81C69A -25, -30, -35, -45 4Kx4
MB81C68A -25, -30, -35, -45 4Kx4
MB8168 -55, -70 4Kx4
MB81C68 -45W, -55W 4Kx4
MB81C68 -55, -70 4Kx4
MB8422 -90, -120 2Kx8
MB8421 -90, -120 2Kx8
MB8417A -12, -12L 2Kx8
MB8417A -15, -15L 2Kx8
MB8417 -20, -20L 2Kx8
MB8416A -12L, -15L 2Kx8
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MB8416 -25W 2Kx8
MB8128 -10, -15 2Kx8
MB85402 -25 16Kx16

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MBM100490 -25 64Kx1
MBM10490 -15, -25 64Kx1
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MBM100470 -10, -15 4Kx1
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MBM100474A -10, -15 1Kx4
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MBM10474A -5, -7 1Kx4
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MBM10415AH 1Kx1

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MBM7226RA -20, -25 512x8
MBM7226RS -20, -25 512x8
MB7123E/H -35, -45 512x8
MB7124E/H -35, -45 512x8
MB7115E/H -35, -45 512x4
MB7116E/H -35, -45 512x4
MB7117E/H -35, -45 256x8
MB7118E/H -35, -45 256x8
MB7113E/H -35, -45 256x4
MB7114E/H -35, -45 256x4
MB7113L LOW-PWR 256x4
MB7114L LOW-PWR 256x4
MB7212RA -20 32x8
MB7212RS -20 32x8
MB7111E/H -25, -35 32x8
MB7112E/H -25, -35 32x8
MB7111L LOW-PWR 32x8
MB7112L LOW-PWR 32x8
MB7143E/H -55, -65 8Kx8
MB7144E/H -55, -65 8Kx8
MB7144Y -45 8Kx8
MB7242RA -20 4Kx8
MB7242RS -20 4Kx8
MB7141E/H -55, -65 4Kx8
MB7142E/H -55, -65 4Kx8
MB7142E/W -55, -65 4Kx8
MB7151E/H -45, -55 4Kx4
MB7152E/H -45, -55 4Kx4
MB7152Y -35 4Kx4
MB7133E/H -45, -55 4Kx4
MB7134E/H/Y -35, -45, -55 4Kx4
MB7238RA -20 2Kx8
MB7238RS -20 2Kx8
MB7137E/H -45, -55 2Kx8
MB7137E/H/SK -45 2Kx8 (Skinny DIP)
MB7138E/H -45, -55 2Kx8
MB7138E/H/SK -45 2Kx8
MB7138Y/SK -35 2Kx8
MB7138E/W -55 2Kx8
MB7127E/H -45, -55 2Kx4
MB7128E/H/Y -35, -45, -55 2Kx4
MB7128E/W -55 2Kx4
MB7232RA -20, -25 1Kx8
MB7232RS -20, -25 1Kx8,
MB7131E/H -45, -55 1Kx8
MB7131E/H/SK 1Kx8
MB7132E/H/Y -35 1Kx8
MB7132E/H/Y/SK 1Kx8
MB7121E/H -35, -45 1Kx4
MB7122E/H/Y -30 1Kx4

DRAMS

MB85227 -10, -12 256Kx9
MB85226 -10, -12 256Kx9
MB85225 -10, -12 256Kx8
MB85224 -10, -12 256Kx8
MB85214 -12, -15 256Kx8
MB85213 -12, -15 256Kx8
MB85211 -12, -15 512Kx4
MB85210 -12, -15 512Kx4
MB85206 -10, -12 256Kx4
MB85205 -10, -12 256Kx4
MB85204 -10, -12 256Kx4
MB85203 -10, -12 256Kx4
MB81C4257 -10, -12, -15 256Kx4
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MB81C4258 -10, -12, -15 256Kx4
MB81C4259 -10, -12, -15 256Kx4
MB81C1000 -10, -12, -15 1Mx1
MB81C1001 -10, -12, -15 1Mx1
MB81C1002 -10, -12, -15 1Mx1
MB81C1003 -10, -12, -15 1Mx1
MB85208 -10, -12 1Mx1
MB85201 -10, -12 1Mx1
MB81C258 -10, -12, -15 256Kx1
MB85108A -10, -12 256Kx1
MB85103A -12, -15 64Kx8
MB85101A -10, -12 64Kx4
MB81C466 -10, -12, -15 64Kx4
MB81464 -10, -12, -15 64Kx4
MB81461 -12, -15 64Kx4
MB8266A -10, -12, -15 64Kx1
MB8265A -10, -12, -15 64Kx1
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MB27C256H -10, -12 32Kx8
MB83256 -25 32Kx8
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MBM27C64 -25X, -30X/W 32Kx8
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MBM27C256A -20W, -25W 32Kx8
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MBM27256 -20X, -25X, -30X 32Kx8
MBM27C128 -20, -25 16Kx8
MBM27128 -20, -25, -30 16Kx8
MBM27128 -25X/W, -30X/W 16Kx8
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DMA CONTROLLER (CMOS)

MB89251A
SERIAL DATA TRANSMITTER (CMOS)

MB89254
PROGRAMMABLE INTERVAL TIMER (CMOS)

MB89255A
PARALLEL DATA INPUT/OUTPUT UNIT (CMOS)

MBL8284A
CLOCK GENERATOR & DRIVER

MB89284A
CLOCK GENERATOR & DRIVER (CMOS)

MBL8283
BIPOLAR OCTAL LATCH

MB89283
BIPOLAR OCTAL LATCH (CMOS)

MBL8282
BIPOLAR OCTAL LATCH

MB89282
BIPOLAR OCTAL LATCH (CMOS)

MBL8259A/-2
PROG. INTERRUPT CONTR.

MBL89259A/-2
PROG. INTERRUPT CONTR. (CMOS)

MB88308/9
CMOS OUTPUT EXPANDER

MB88306/7
CMOS OUTPUT EXPANDER

MB88304/5
NMOS 4/8-BIT I/O EXPANDER

MB4107
DATA SEPARATOR

MB1412AC
LS-TTL ERROR CHECKING/CORRECTION CIRCUIT (ECC)

MB1426
16-BIT ECC

SPECIAL CONTROLLERS (ASIC)

MB8877A
FLOPPY DISK CONTROLLER

MB8876A
FLOPPY DISK FORMATTER

MB89322
CRT CONTROLLER (6845 COMPATIBLE) (CMOS)

MB89321
CRT CONTROLLER (6845 COMPATIBLE) (CMOS)

MB89311
FLOPPY DISK CONTROLLER

MB88303P
TELEVISION DISPLAY CONTROLLER

TELECOM

MB87006
PLL

MB87004
DTMF/PULSE DIALER

MB87003
DTMF/PULSE DIALER

MB87001
SYNTHESIZER SYSTEM BLOCK

MB6024
CODEC

MB6022
CODEC

MB6021
CODEC

MB501/L
TWO MODULUS PRESCALER

MB503/504/506
TWO MODULUS PRESCALER

LINEAR

MB3712
POWER AMP

MB3713
POWER AMP

MB3722
POWER AMP

MB3714A
POWER AMP

MB3737
POWER AMP

MB3730
12W BTL AUDIO AMP

MB3731
18W BTL AUDIO AMP

MB3752
VOLTAGE REGULATOR

MB3759
PULSE WIDTH MODULATION (PWM) CONTROL

MB3760
PWM CONTROL CIRCUIT

DSP (DIGITAL SIGNAL PROCESSORS)

MB8764CR
-001 88-PIN PGA

MB8764CV
-001 84-PIN LCC

MB8764PR
-001 88-PIN PLASTIC PGA

MB87064P
42-PIN PLASTIC DIP

MB87064C
42-PIN CERAMIC DIP

MB87069C
64-PIN CERAMIC PGA

SCSI

MB87030
SYNCHRONOUS S.P.C.

MB89351
ASYNCHRONOUS S.P.C.

CONVERTERS

MB40547
-7/-8 8-BIT UH SPEED A/D

MB40576
6-BIT UH SPEED VIDEO A/D

MB40748
-8/-9 10-BIT UH SPEED D/A

MB40776
6-BIT UH SPEED D/A

MB40778
8-BIT HIGH SPEED D/A

MB40788
10-BIT UH SPEED D/A

MB88301A
6-BIT PWM NMOS D/A

MB4052
4 CHANNEL 8-BIT A/D

MB4053/63
6 CHANNEL 8-BIT A/D SUBSYSTEM

MB4072
8-BIT HIGH SPEED MULTIPLYING D/A

ETHERNET

MB8795
ETHERNET CONTROLLER

MB87012
802.3/ETHERNET CONTROLLER

MB502
MANCHESTER ENCODER/DECODER

CMOS GATE ARRAYS

UH SERIES:

C20000UH
20,160 GATES

UM SERIES:

C15006UM
15,120 GATES
+ 6K RAM

C10012UM
10,080 GATES
+ 12K RAM

UHB SERIES:

C12000UHB
12,734 GATES

C8700UHB
8,768 GATES

C6000UHB
6,000 GATES

C4100UHB
4,174 GATES

C3000UHB
3,066 GATES

C2200UHB
2,220 GATES

C1700UHB
1,724 GATES

C1200UHB
1,233 GATES

C830UHB
830 GATES

C530UHB
530 GATES

C330UHB
336 GATES

AV SERIES:

C8000AV
8,000 GATES

C6600AV
6,664 GATES

C5000AV
5,022 GATES

C3900AV
3,900 GATES

C2600AV
2,640 GATES

AVB SERIES:

C2000AVB
2,052 GATES

C1600AVB
1,674 GATES

C1200AVB
1,245 GATES

C850AVB
852 GATES

C540AVB
549 GATES

C350AVB
357 GATES

C4002AVM
4,087 GATES
+2K RAM

C2301AVM
2,375 GATES
+ 1K RAM

C1502AVM
1,564 GATES
+ 2K RAM

CMOS STANDARD CELLS

AV SERIES:
1.8μ 2-LAYER METAL

16K RAM, 64K ROM, PLAs, REGISTERS

SPECIAL LSI FUNCTIONS

>13K GATES 2 INPUT GATE EQUIVALENT

<1.4ns TYPICAL
<2.2ns WORST CASE

AU SERIES:
1.3μ DUAL-WELL, 2 AND 3 LAYER METAL

32K RAM, 128K ROM, PLAs, REGISTERS, MULTIPLIERS, ALU

STANDARD LSI EQUIVALENT FUNCTIONS

>40K GATES 2 INPUT GATE EQUIVALENT

<0.8ns TYPICAL
<1.3ns WORST CASE

BIPOLAR LSTTL GATE ARRAYS

EQUIVALENT GATES (2 INPUT GATES)

B240
360 GATES

B350
540 GATES

B350B
528 GATES

B600
924 GATES

B700B
1,080 GATES

B1100
1,680 GATES

B2000
3,162 GATES

BIPOLAR ECL GATE ARRAYS

EQUIVALENT GATES (2 INPUT GATES)

ET750
1,136 GATES

ET1500
2,192 GATES

ET3000
4,344 GATES

ET4500
6,280 GATES

ET2009
2,640 GATES
+ 9K RAM

ET3004
3,960 GATES
+ 4K RAM

PACKAGING

PLASTIC PIN GRID ARRAYS

FLAT PACK GULL WINGS

256-PIN CERAMIC GRID ARRAYS

SMALL OUTLINE J LEADS (SOJ)

PLASTIC ZIG-ZAG IN-LINE (ZIP)

SHRINK DIPs

SKINNY DIPs

SMALL OUTLINE DIPs

SINGLE IN-LINE PACKAGE (SIP)

SINGLE IN-LINE MODULES

PLASTIC GRID ARRAYS (PGA)

CERAMIC GRID ARRAYS (PGA)

PLASTIC LCCs

CERAMIC LCCs

PLASTIC FLAT PACK

CERAMIC FLAT PACK

FLAT PACKS w/ HEAT SINKS

SMALL OUTLINE DIP

CIRCLE NO 91

For spaceborne telescopes as well as commercial satellites, some of the extremely sensitive components and assemblies are shipped and stored in specially designed Hardigg containers. So, before they travel the vacuum of space, they travel with us.

PROVEN PERFORMANCE

These components needed to be safely contained in an extremely dry environment that could withstand shock up to 30g's. Not only did we meet the challenge, but provided a container that went well beyond the requirements. Just like we have with so many other difficult containerization problems for the commercial marketplace over the last twenty years.

Another example is a container we designed for a very delicate medical diagnostic component to a CAT Scan system. The units are stored and shipped all across the U.S., India, Africa, and Europe. We designed a container that not only protected the crystal elements from mechanical shock but also provided protection from damaging thermal shock as well.

CIRCLE NO 102

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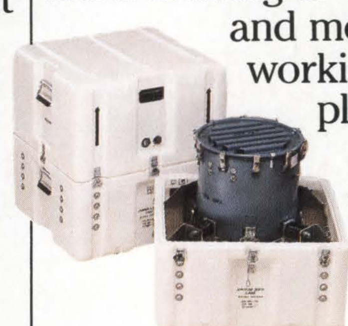
The reason we can provide answers to so many difficult containerization problems rests on our skillful, knowledgeable Applications Engineering staff, and our complete manufacturing capabilities. Our engineers are shock-mitigation and environmental engineering specialists that live and breathe containerization. And our facilities enable us to provide high or low volume quantities, while controlling every aspect of the manufacturing process; from mold making to tooling, and metal working to plastic fabrication.



So, before you send your next product on a journey to outer or inner space, call the container company that's a proven traveller-Hardigg.

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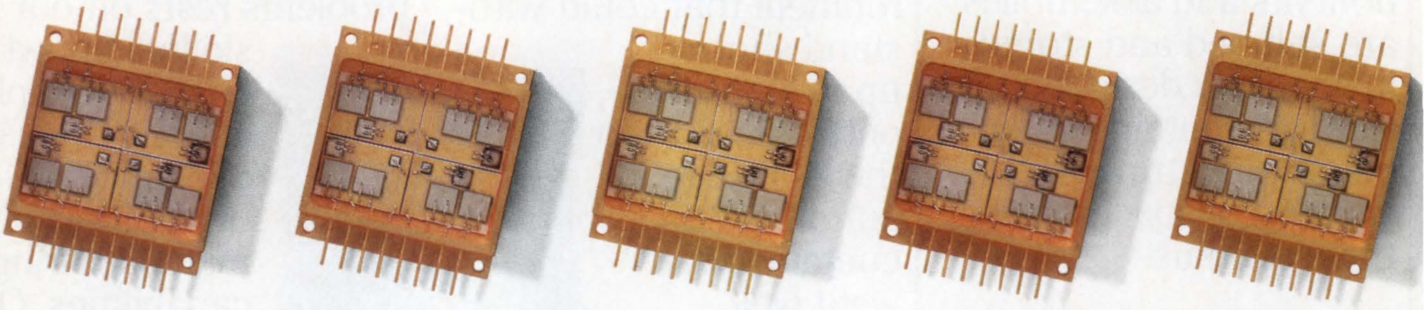

NEWS BREAKS

EDITED BY JOAN MORROW

22-BIT ADC OFFERS 0.5-PPM/°C FULL-SCALE STABILITY

Thaler Corp's (Tucson, AZ) 22-bit, dual-slope integrating A/D converter, the ADC100, comes in a 1×2-in., 40-pin ceramic DIP and operates over 0 to 70°C. It requires 5V and ±15V power supplies. The converter offers a full-scale stability of 0.5 ppm/°C max—which the company claims is 20 times better than the closest equivalent product. A floating current source, Vishay precision resistors, and calibration by an onboard μP reduce the total nonlinearity error to 3 ppm max. If you wish, you can autozero the linearity and the offset stability (0.1 ppm/°C max; 0.1 ppm/month max). With each converter ordered, Thaler provides the only additional parts needed for operation—a 25-MHz crystal and an integration capacitor. The ADC100 costs $300 to $500, depending on grade.—Tarlton Fleming

REPEATERS STRETCH MULTIPLEXED TERMINALS THREE MILES FROM HOST

Users of the HPS distributed communication subsystem family of multiplexers can now spread clusters of RS-232C terminals over cable distances as long as three miles. The Spur (Systech Pluriaxial Unplug Repeater) products include repeaters that connect with a mixture of coaxial and fiber-optic cables. Members of Systech Corp's (San Diego, CA, (619) 453-8970) HPS-5580 Spur family, which cost $610 to $2205 (100), provide flexibility in connecting cluster controllers to the LAN-based HPS multiplexer scheme. Each cluster controller interfaces to eight or 16 terminals via standard serial cables. Theoretically, the Spurs can connect 254 clusters, but host-adapter firmware currently supports 128 terminals.—Maury Wright

2400-BPS MODEM CHIP SET USES STANDARD COMPONENTS

Telebit Corp (Cupertino, CA, (408) 996-8000) is making available the license to build a 2400-bps modem with a 3-chip set based on readily available components. The design is based on the 320CM10 DSP chip, the 80C51 microcontroller, and the 6950B analog front end. These devices are supplied with mask-programmed code written by Telebit to perform all of the functions needed to implement a 2400-bps modem. You can purchase the microcode and design for a 1-time fee, or you can purchase the 3-chip set from the semiconductor manufacturers with the Telebit masks for less than $30 including royalty (25,000). A half-card, PC-based evaluation board will be available in May for $600.—David Shear

SOFTWARE DEVELOPMENT TOOLS SUIT REAL-TIME DSP APPLICATIONS

If your application needs to run complex DSP and image-processing algorithms at speeds reaching 8 MIPS, consider using EuclidTools from Datacube Inc (Peabody, MA, (617) 535-6644). This $2000 set of software development tools is designed for use with your VME Bus-compatible, Euclid host-controlled programmable coprocessor. EuclidTools includes a C compiler, an assembler, a linker, and an interactive debugger. You also get libraries for math, signal, and image processing. Run-time support routines handle interrupt processing and hardware management. Device drivers for Unix 4.2 and Microware OS-9 operating systems come with the package, as does test, diagnostic, and demo code.—J D Mosley

TOOL KIT SUPPORTS GRAPHICS FOR NEW IBM PCs' PROTECT MODE

The Graphics Development Toolkit (GDT) 3.0 gives programmers direct access to the IBM Operating System/2 protect mode for graphics software development. It was developed for IBM by Graphics Software Systems (Beaverton, OR, (503) 641-2200). You'll be able to buy it directly from GSS for $495 this summer when IBM releases the Operating System/2's developer's tool kit.

Device-independent graphics interfaces have been available for previous IBM PC versions, but they did not gain widespread acceptance because software developers usually preferred to write their own hardware-dependent drivers and avoid the 5 to 10% speed penalty of the software interfaces. However, IBM's inclusion of their proprietary graphics coprocessor in the Personal System/2 8514/A intelligent high-resolution display adapter, as well as the move by add-in graphics-board manufacturers to base their new boards on graphics engines from TI, Intel, and Hitachi, can give graphics hardware the horsepower necessary to handle a device-independent software interface's overhead.—Margery S Conner

ALLIANCE WEDS LINEAR-DESIGN COMPANY TO WAFER-FAB GIANT

Texas Instruments (Dallas, TX) and Linear Technology Corp (Milpitas, CA) have jointly announced a strategic alliance that provides alternate sourcing for analog parts designed by Linear Technology. The 5-year agreement gives TI alternate-source rights to as many as 60 existing and future device designs from LTC's catalog of op amps, comparators, voltage references, data converters, switch-mode power converters, filters, and interface circuits. Five-year-old LTC, a haven for some of the US's most prominent linear-IC design engineers, gains access to TI's wafer-fab, assembly, and test facilities, and it gains a valuable second source for its parts.—Steven H Leibson

TAPE CONTROLLER PROVIDES MESSAGE-PASSING SUPPORT

The Tapemaster 2000 from Ciprico (Plymouth, MN, (612) 559-2034) provides intelligent control of tape operations. This Multibus II board controls as many as eight formatted start/stop or streaming Pertec-compatible ½-in. tape drives at burst transfer rates of 32M bytes/sec and tape transfer rates reaching 1.5M bytes/sec. Featuring an onboard message-passing coprocessor and a 512k-byte tape-data buffer, the Tapemaster 2000 asynchronously processes tape requests from the host system without handshake timing restrictions. This $2495 controller also optimizes tape motion to minimize tape-repositioning cycles.—J D Mosley

CASCADABLE FIFOs BOAST 64-WORD CAPACITY AND 30-MHz SPEED

Consuming no more than 170 mA of power, three 64-word bipolar FIFO memories from Texas Instruments (Dallas, TX, (800) 232-3200) process data at rates as high as 30 MHz. When cascaded, the SN74ALS234, SN74ALS235, and SN74ALS236 can efficiently buffer long data streams between asynchronous subsystems operating at different speeds. The 'ALS234 and 'ALS236 sport 4-bit-wide organizations, input- and output-ready flags, and 30-MHz operating frequencies. The 5-bit-wide 'ALS235 specs a 25-MHz maximum frequency and offers flags to indicate input-ready, output-ready, half-full, almost-full, and almost-empty conditions. Each device sells for $13.72 (1000).—J D Mosley

Now there's a 96MB drive with something extra:

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If you're putting together multiuser or other high-end systems, Seagate has the manufacturing experience to deliver dependable, high-capacity 5¼″ drives—whether you need 10 or 10,000.

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Each drive is built with the same skill and reliability that have made Seagate the world's leading supplier of 5¼″ hard disc drives. People who demand performance have bought more than 5 million of our drives for small computer applications.

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Seagate

CIRCLE NO 146

125-MHz PULSE GENERATOR OFFERS 1-nSEC RISE TIME

The $3385 PM5785 pulse generator from Philips I&E Div (Eindhoven, The Netherlands, TLX 35000; in the US, (201) 529-3800) has a repetition rate between 1 Hz and 125 MHz and features user-selectable rise times of 1, 1.5, or 2 nsec. In addition to controlling the pulse-repetition rate, duration, and delay, you can use external triggering and gating inputs to synchronize the generator to an external clock or to generate synchronized pulse bursts. You can also externally control the pulse duration. A burst-mode option allows front-panel selection of bursts with 1 and 9999 pulses. The device offers four output-level ranges between 0.2 and 5V; output impedance backmatching absorbs more than 95% of signal reflections from mismatched loads.
—Peter Harold

SINGLE-BOARD COMPUTER SUITS LOW-COST OS-9 DEVELOPMENT SYSTEMS

The CC97 single-board computer from Compcontrol (Eindhoven, The Netherlands, TLX 51603; in the US, (408) 356-3817) requires only the addition of SCSI-compatible disk drives to provide a complete OS-9 operating-system environment on the VME Bus. The board runs a 10- or 16-MHz 68000/68010 μP, which is provided with 128k bytes of zero-wait-state static RAM, 2M bytes of dual port RAM, and space for as much as 256k bytes of EPROM. Battery backup is optionally available for 64k bytes of the static RAM. The board also includes a SCSI bus interface with DMA capability, four serial I/O channels (two of which have DMA capability), a real-time clock, a VME Bus interrupt requester and handler, and VME Bus system controller functions. The CC97 has an end-user price of approximately $3000.—Peter Harold

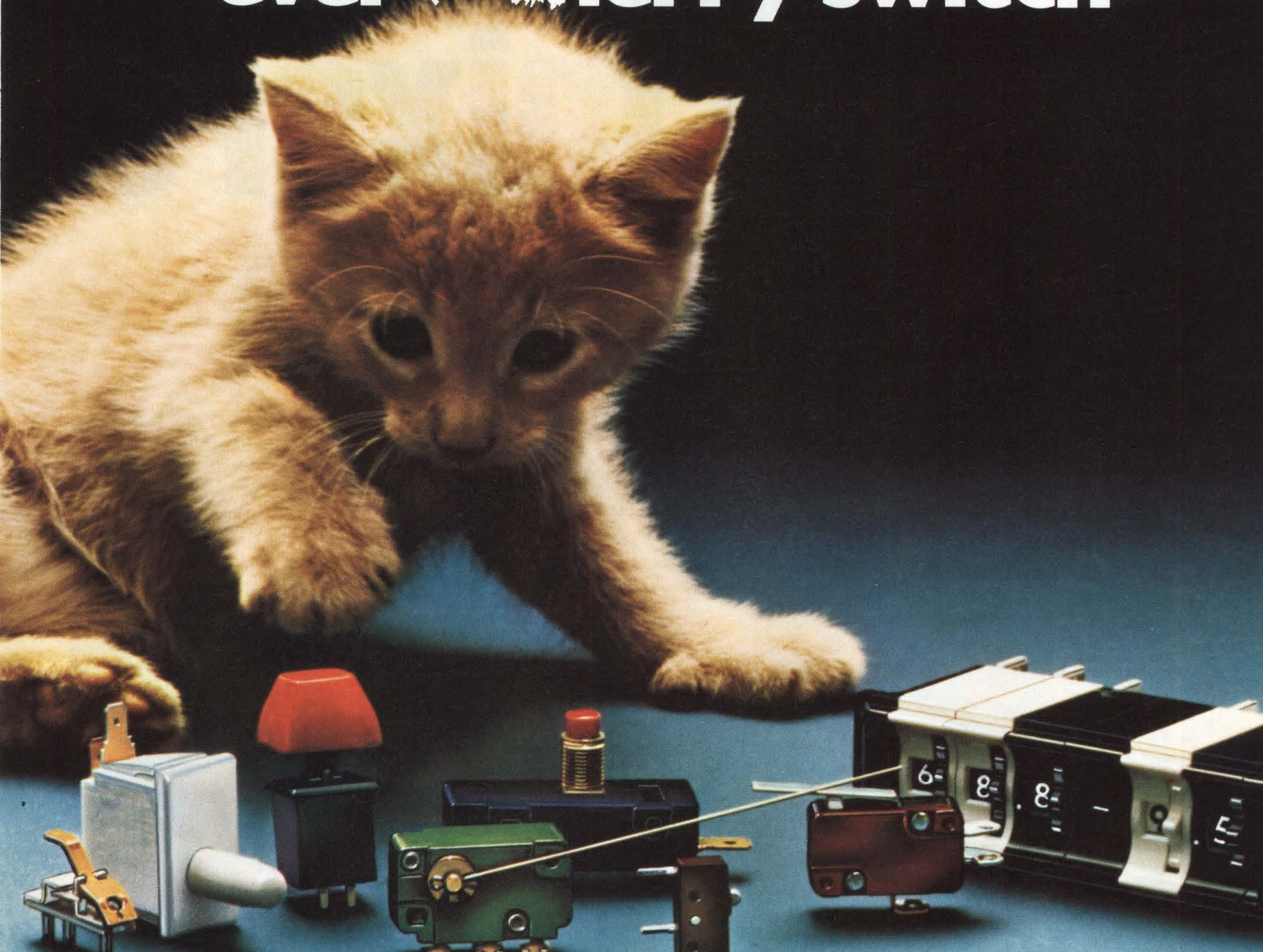
ADD-IN BOARD INTERFACES IBM PC TO DATA NETWORKS

The SICC-PC add-in card for IBM PC, PC/XT, and compatible computers allows you to access the German Federal Mail Service's Datex-P network or similar networks operating in other European countries. Manufactured by Stollmann GmbH (Hamburg, West Germany, Teletex (17) 403226), the card provides an X.25 standard communications interface; a software packet assembler/disassembler, which supports CCITT X.28, X.29, and X.3 recommendations; and 3270 terminal emulation. The Z80A μP-based board, which costs approximately DM 2950, is available with as much as 48k bytes of onboard parity-checked dynamic RAM. Physical communications interfaces include the X.21 and V.24; as an option, you can purchase an interface to plug the card into the IBM PC/AT bus.—Peter Harold

PEN RECORDERS FEATURE DIGITAL READOUT AND TRACE ANNOTATION

The SE110 and SE111 flat-bed pen recorders from BBC-Goerz/Metrawatt (Nuremburg, West Germany, TLX 623729; in the US, (303) 469-5231) are line/battery-powered, portable pen recorders that feature integral 3½-digit LCD readouts. Measuring 306×231×76 mm and weighing approximately 2.2 kg, the recorders write over a width of 100 mm on single-sheet or roll paper. Paper speeds range from 1 cm/hour to 60 cm/minute, and you can annotate the trace with instrument set-up information. Priced at 1650 DM, the SE110 has 18 dc measurement ranges between 1 mV and 500V full scale. The 1850 DM SE111 has 11 ac/dc voltage ranges between 0.15 and 300V full scale and 11 ac/dc current ranges between 0.6 and 1500 mA full scale. Separate probes increase the measurement range of the SE111 to 750V and 6A.—Peter Harold

There's a little tiger in every Cherry switch



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You see, we can control the quality of our switches because we fabricate most of our own parts (moldings, stampings, springs, printed circuits, etc.). And we can keep the price down because we're loaded with automatic equipment to handle high volume.

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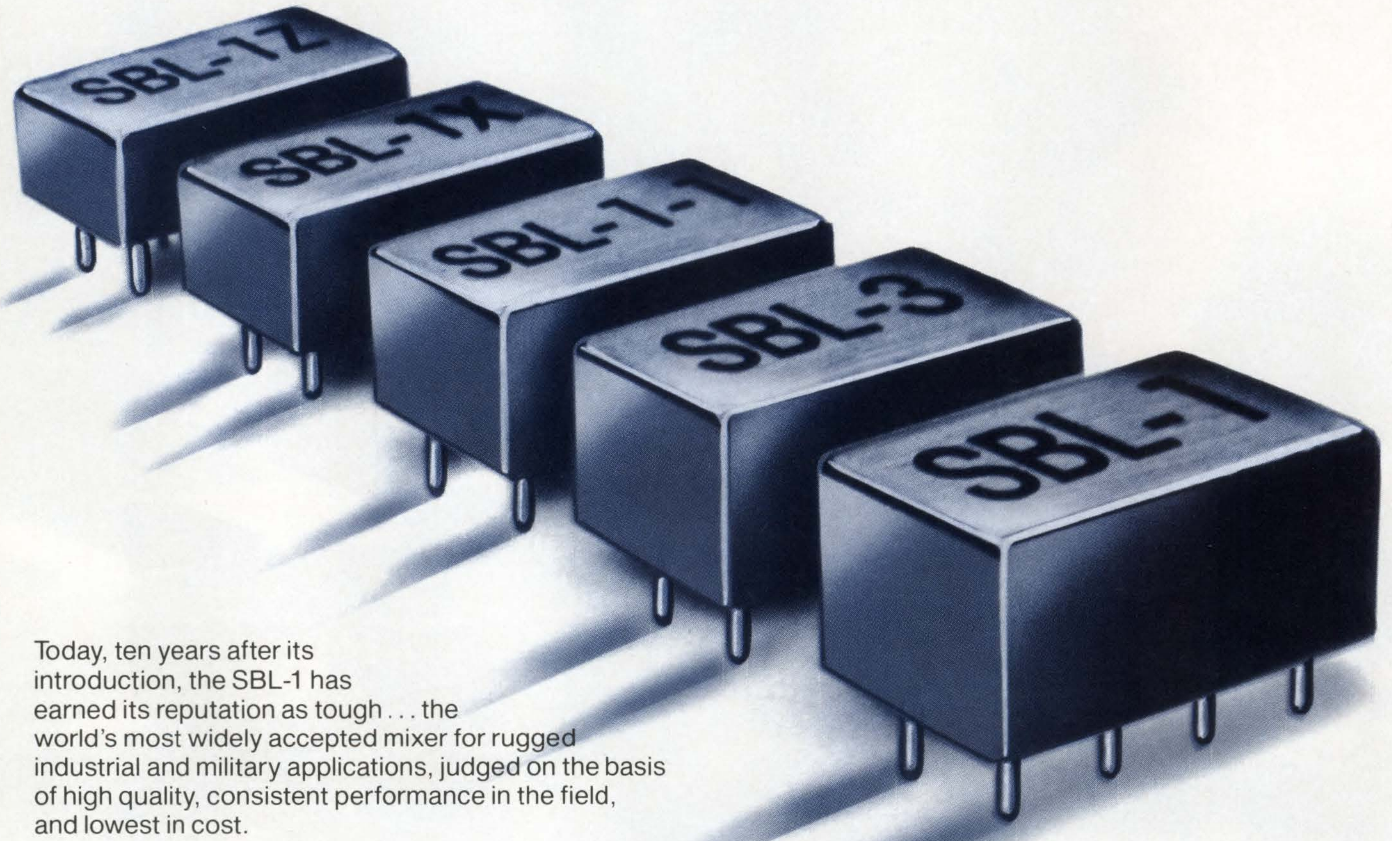
CIRCLE NO 79

more tough mixers



Today, ten years after its introduction, the SBL-1 has earned its reputation as tough . . . the world's most widely accepted mixer for rugged industrial and military applications, judged on the basis of high quality, consistent performance in the field, and lowest in cost.

And the winning formula is not a secret.

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The SBL-1 does have one drawback however. It only covers 1 to 500 MHz. That's why we've expanded the product family with additional models to cover 25 KHz to 1000 MHz. The new units are assembled with the same production and test expertise as the SBL-1; that's why we can offer 0.1% AQL on all SBL models . . . no rejects, not a single one, on every order shipped. So don't compromise your design or settle for a poor imitation. Specify Mini-Circuits SBL Mixers.

For full specifications call or write for latest RF/IF Signal Processing Handbook or refer to EEM, Gold Book, or Microwaves Directory.

SBL SPECIFICATIONS (typ.)

Model	Freq. (MHz)	Conv. Loss	Isolation,dB L-R	Isolation,dB L-I	Price (10-49)
SBL-1	1-500	5.5	45	40	**$4.50**
* SBL-1X	10-1000	6.0	40	40	**$5.95**
SBL-1Z	10-1000	6.5	35	25	**$6.95**
SBL-1-1	0.1-400	5.5	35	40	**$6.50**
SBL-3	0.25-200	5.5	45	40	**$7.50**

* If not DC coupled.

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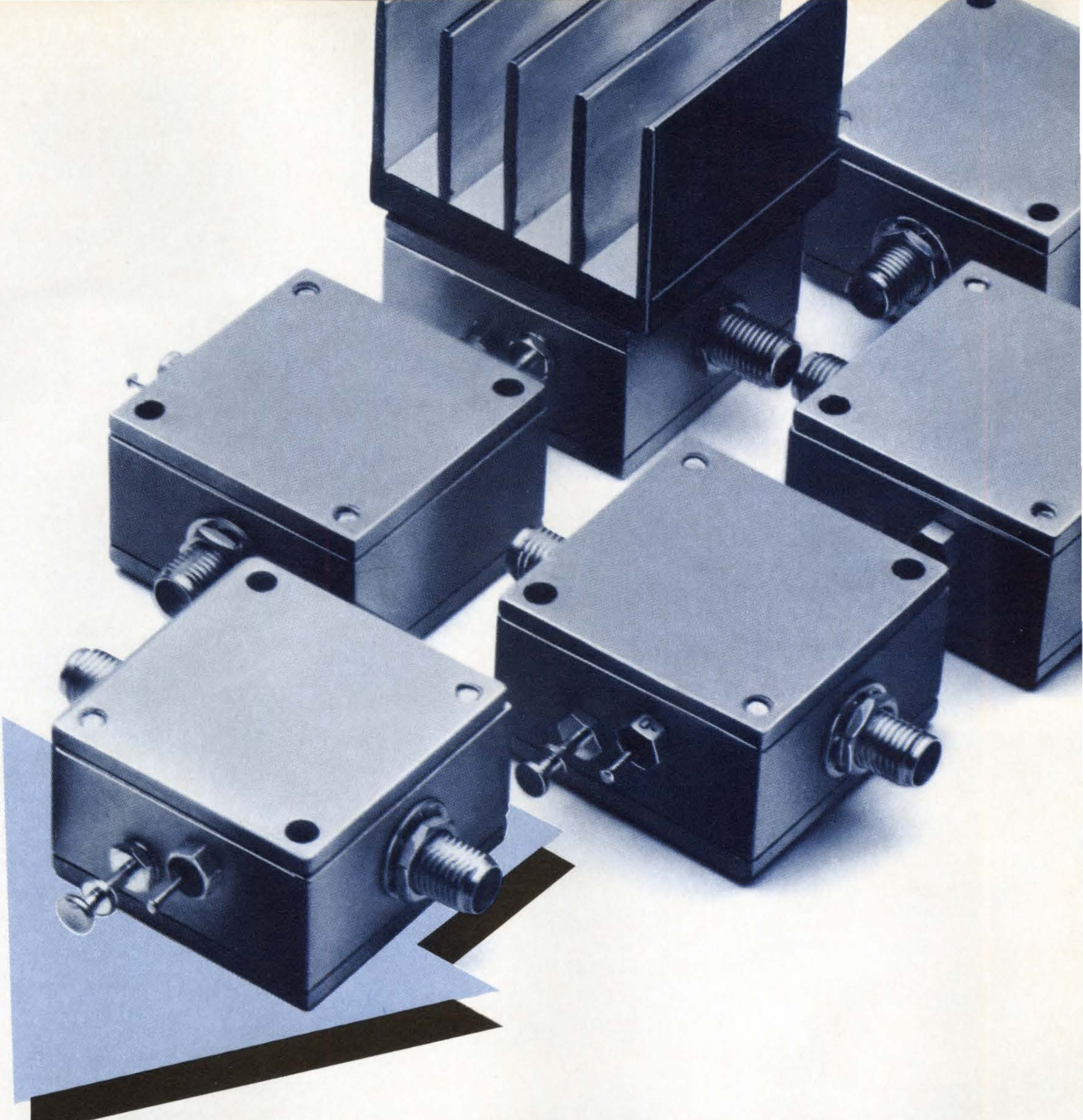
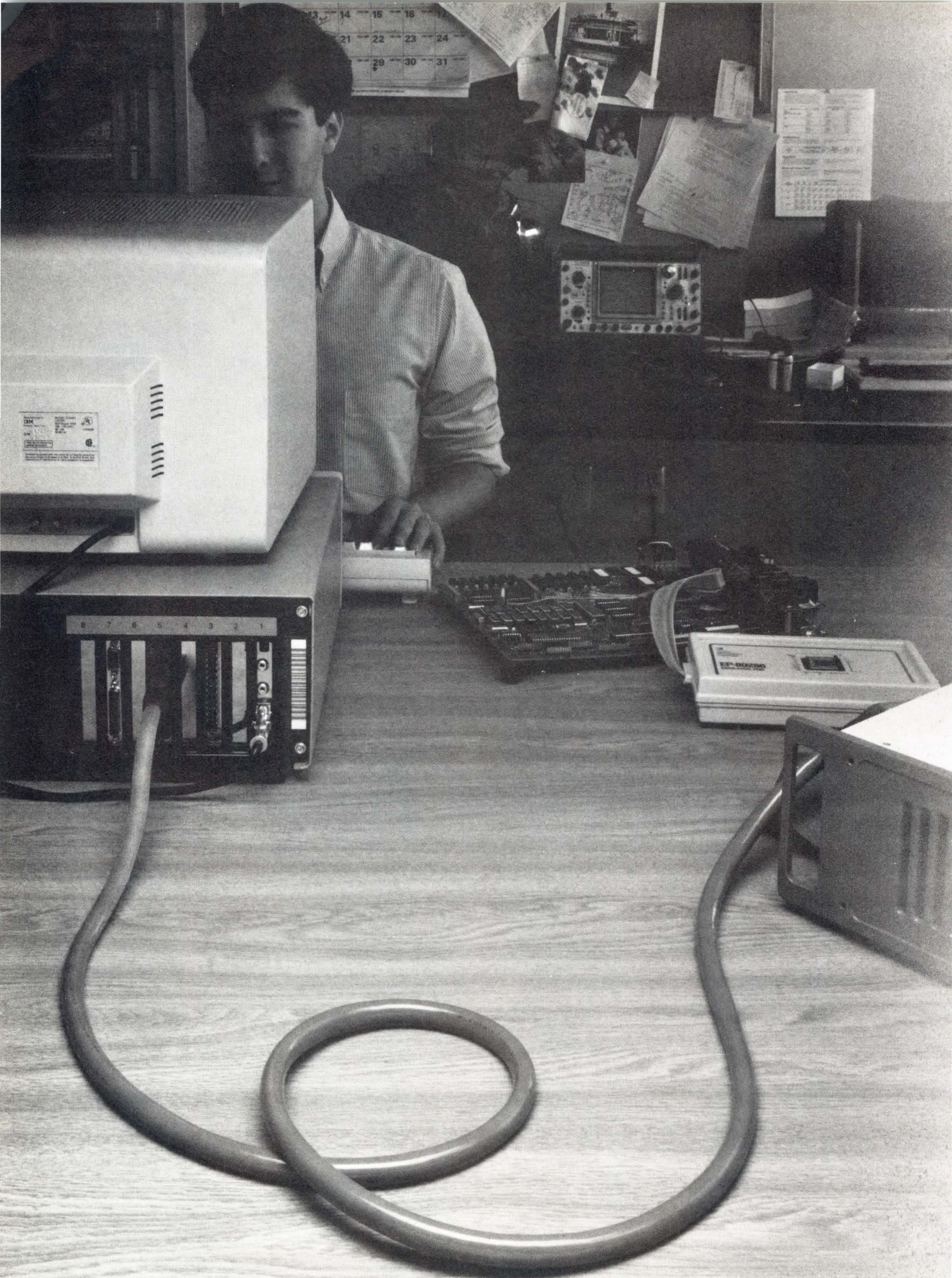
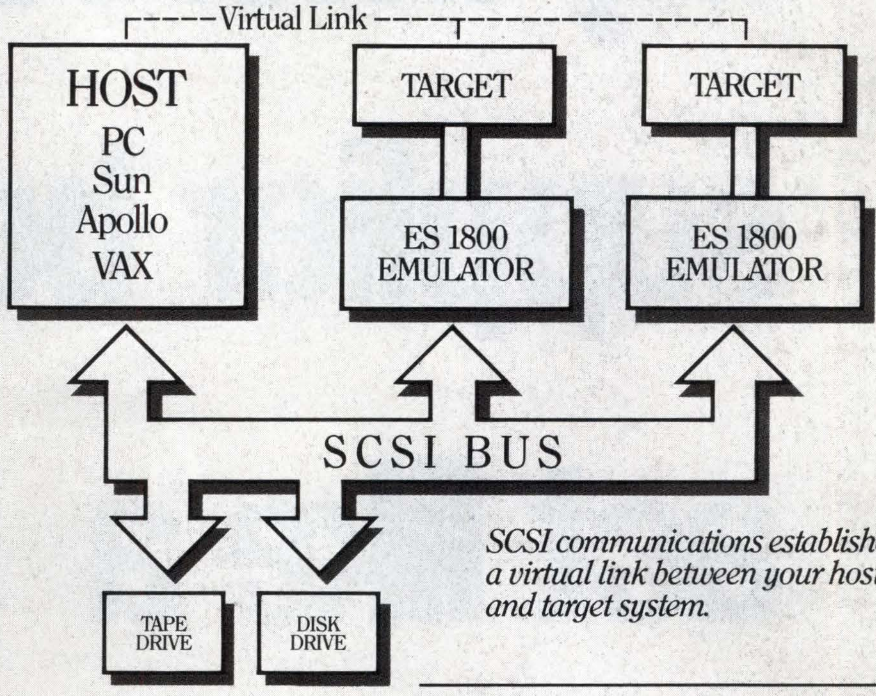
C104 REV. ORIG.



CIRCLE NO 123



Data shouldn't take 30 minutes to travel two and a half feet.



SCSI communications establishes a virtual link between your host and target system.

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HOSTS	OPERATING SYSTEMS	TARGETS	LANGUAGES	TOOLS
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MicroVAX	ULTRIX	8048 family	Pascal	Linkers
UNIX® workstations · Apollo · Sun · IBM AT	UNIX	8080, 8085, 8086/88, 80186/188 and 80286	FORTRAN	Locaters
MS-DOS workstations · PC · PC XT · PC AT · Compatibles	XENIX	68HC11, 6800/2/8, 6809/9E, 68000/8/10 and 68020	PL/M	Compilers
	MS-DOS	Z80, MK3880/4 and Z8001/2/3	Assembler	Symbolic debuggers
		NSC-800	Jovial	Source level debuggers
				Emulators

A stand-alone or host-control system of fully integrated debug tools built on high performance emulation.

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SIGNALS & NOISE

Generalizations about ICEs were in error

Dear Editor:

Certain statements made in the article "μP simulators let you debug software on an IBM PC" (EDN, December 11, 1986, pg 196) are sufficiently misleading to confuse an uninformed reader. For example, the article stated that "PC-based simulators generally offer more sophisticated software-debugging features than do expensive in-circuit emulators" and " . . . ICEs are optimized for hardware debugging, not software debugging. Microprocessor simulators are much better for software debugging . . . ."

Further, the article stated that " . . . a simulator lets you easily set up and modify I/O conditions to test your software. Because ICEs are hardware tools, their I/O conditions are more difficult to modify." The article also claimed that "before you can test code with an ICE, you have to load your code into ROM and into a real system."

Having spent several years in the emulator and software businesses, I would like to point out the following: First, the simulators discussed in the article do not offer features incremental to those available on today's in-circuit emulators.

Further, ICEs are a system-integration tool. They are optimized for both hardware and software. PC-based debuggers that work in conjunction with in-circuit emulation provide real-time code execution and the ability to handle asynchronous events (interrupts and exceptions) that are typical in embedded system design. No simulator can provide these functions.

Sophisticated emulators are perfectly capable of mimicking I/O transactions in the absence of target hardware. And since the earliest days of in-circuit emulation, overlay memory has completely obviated the need for target-system hardware during development. It is totally incorrect to say that "you'd have to load your code into ROM."

Sincerely yours,
Steve Dearden
Applied Microsystems Corp
Redmond, WA

(*Ed Note: The simulators discussed in the article provide engineers with a key feature—an operational software-development facility independent of the target hardware. You can use the simulators to test every possible path through your software, and you can also test all I/O conditions. Further, the top-of-the-line simulators include trapping and breakpoint capabilities that are superior to those of other tools such as in-circuit emulators (ICEs).*)

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CIRCLE NO 53

The article was not meant to imply that simulators are replacements for ICEs. Although you don't have to use both an ICE and a simulator for every design, you can use the two tools together effectively for complex designs. You can test and debug your software with the simulator, but testing in real time with real-time I/O requires that you test the target hardware. An ICE is the most effective tool for such testing.

Finally, some of the article's generalizations about ICEs were indeed in error. In fact, very few ICEs require that you program a PROM before testing your code. Many ICEs provide some facility for testing code with no target hardware, and some ICE vendors also provide high-level-language debugging capabilities.)

"IT'S NOT ONE OF OUR BETTER DESIGNS, BOB, BUT I FEEL CONFIDENT YOU PEOPLE IN SALES WILL BE ABLE TO FIND SOMEONE STUPID ENOUGH TO BUY IT."

Moral criteria for engineering work

Dear Editor:

Regarding the "engineers' social consciousness" dialogue in your magazine: After some 25 years in our profession, I must be mellowing, because I can see that such a dialogue in a technical publication can be useful. However, it is a waste of our time to read more repetition of the superficial and politically motivated opinions that appear in the mass media. Let us see contributions that offer specific (not vague) technical and/or professional insight.

The assumption that working on military programs indicates a lack of "social consciousness" is not logical. Most of the engineers I know who work on such programs have considerable social consciousness. They have resolved that their work is in society's best interest. Obviously, there are those in our society who disagree, for their own political and social reasons. There is no reason to assume that the social consciousness

of those who oppose military programs is superior to that of those who work on such projects.

If we must question the social consciousness of engineers, let us establish moral criteria. Is it not illogical to compare the morality of a defensive system to that of crematoria or germ warfare? Let us also establish moral criteria for nonmilitary engineering work. Let us resolve the question: Is it the technology or the application that must be judged?

Finally, if we are to establish moral criteria for engineers' social consciousness, let us test them against those of members of other professions, such as editors, managers, politicians, etc.

Please continue the dialogue. Please help us find facts and resolve these issues with logic.

Sincerely yours,
Thomas L Poppelbaum
Clinton, NY

WORM disks can protect design files

Dear Editor:

The article "Optical-disk drives target standard 5½-in. sites" (EDN, December 25, 1986, pg 42) ignored a potentially lucrative market for optical disks. We currently spend a great deal of time and money developing software that will counteract the write capability of magnetic media. The data that depicts drawings and other "released" data must be protected from accidental or intentional changes. The average file sizes range from 20k bytes for CADAM files to 138k bytes for Computervision files and 1.5M bytes for CATIA files. These files must be readily accessible for use by downstream functions. New versions must be generated from copies of released files. Write-once/read many (WORM) optical disks are ideal for this application.

Sincerely yours,
Bill Holmes
Data Systems Div
General Dynamics
San Diego, CA

Sorry, wrong number

EDN's January 22 News Breaks (pg 19) contained an incorrect phone number for Viking Connectors. The correct number is (818) 341-4330.

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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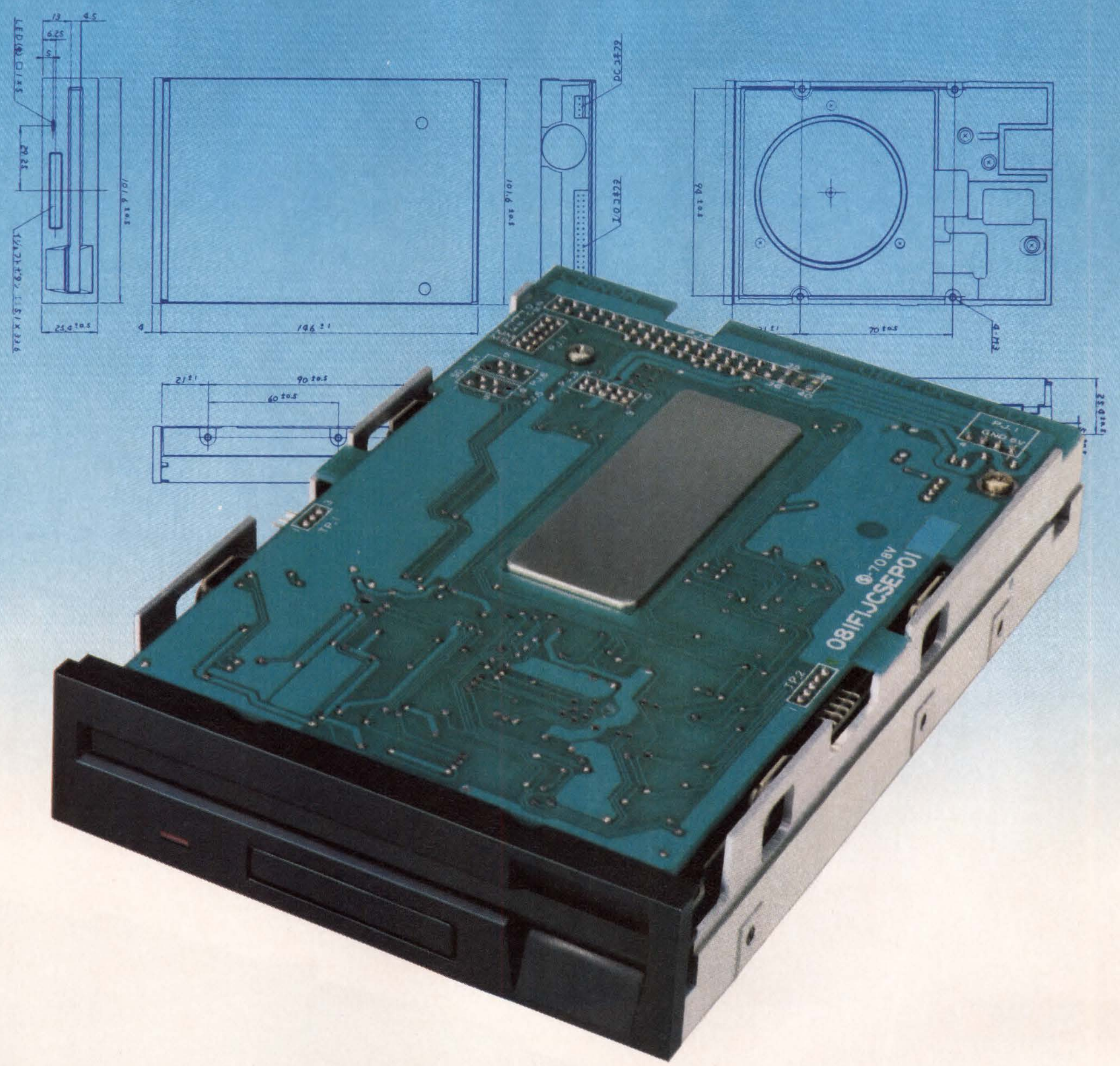

Chinon floppy disk drives are renowned in Japan for outstanding technical excellence and an extremely high level of overall quality. That kind of reputation doesn't come easy in a land where OEM's have some of the toughest standards in the world.

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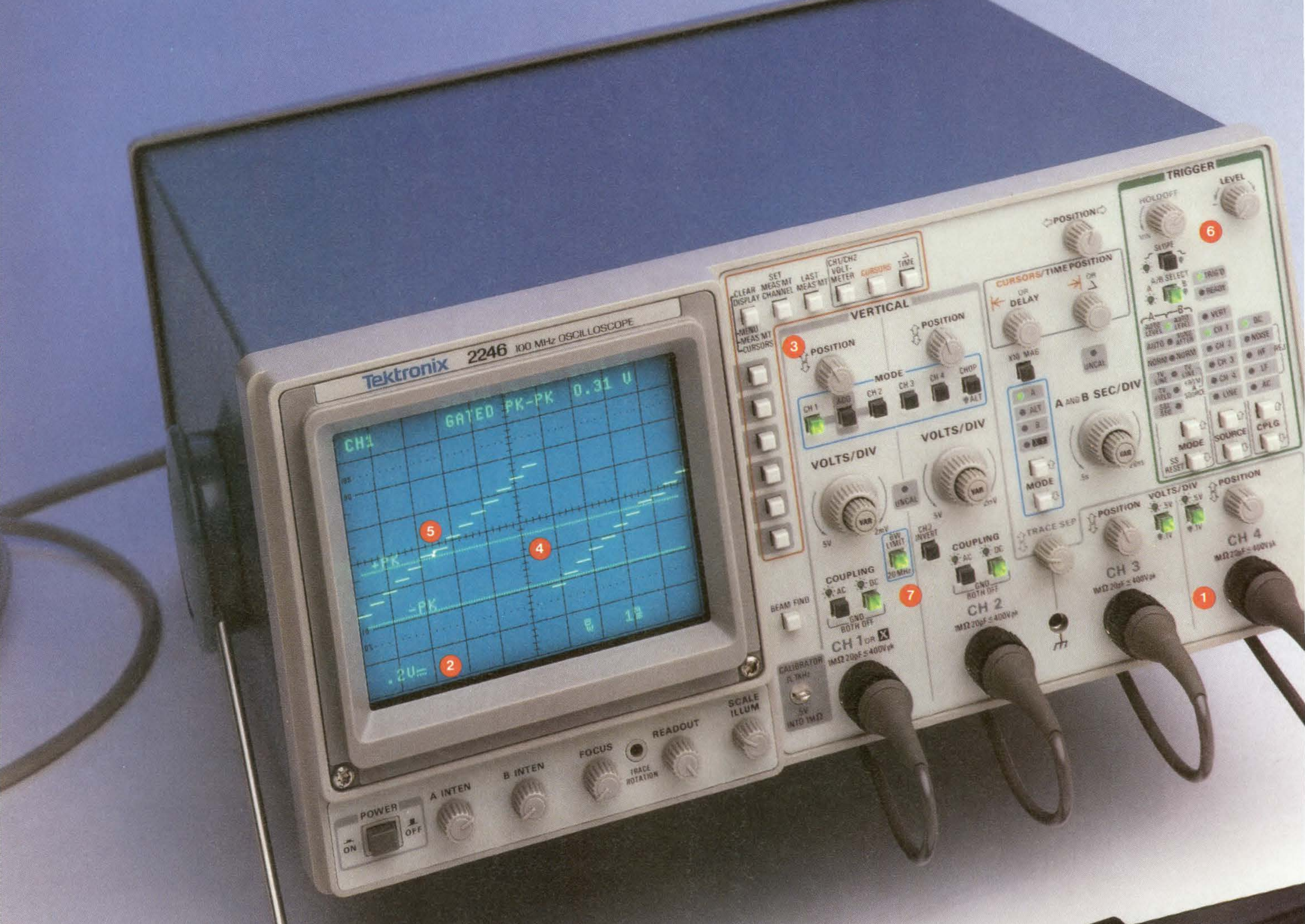
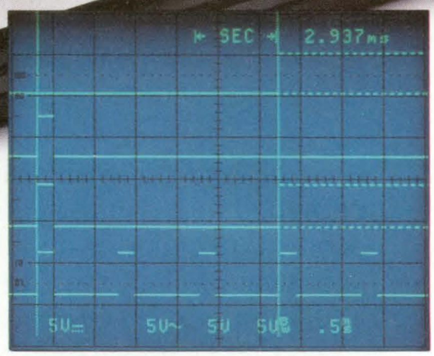
PICTURED IS CHINON F-354L: 5V, ONE-INCH, 1MB SLIM-LINE MODEL.

New GPS Series: with SmartCursors™

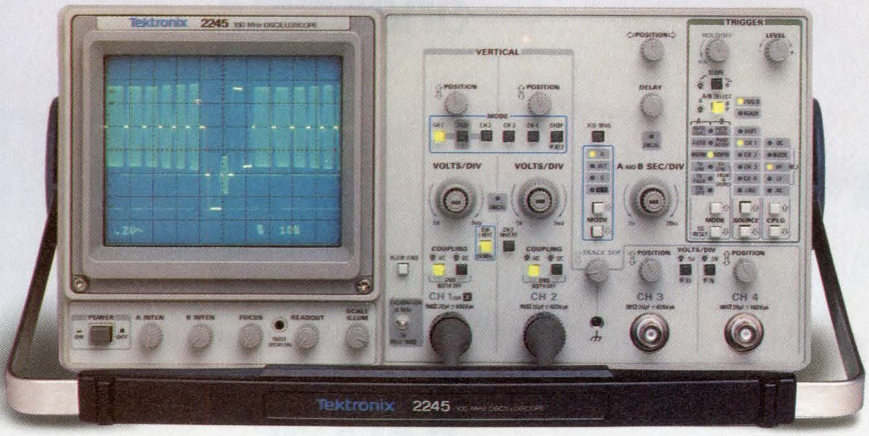


1 Four channels with 100 MHz bandwidth. 2 CRT readout of scale factors and measurement results. 3 Menu functions controlled by the top row of push buttons. 4 SmartCursors™ track ± peak or peak-to-peak voltage measurements. 5 Gated voltage mode makes it possible to itensify a portion of a waveform and make voltage measurements on that segment only. 6 Versatile triggering lets you trigger the main or delayed sweep on any of the four channels. 7 Backlit control buttons verify that a function is active.



The 2246 provides direct time readout information when seconds is selected in cursor mode. You also have 1/seconds in Hz and phase capability.

Tek sets the pace and push-button ease.



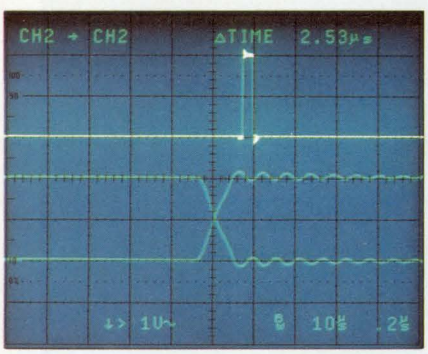
Work faster, smarter, with two new general purpose scopes from Tek. The four-channel, 100 MHz 2246 and 2245 set the new, fast pace for measurements made daily at the bench or in the field. They're easy to use and afford, by design. And backed by Tek's three-year warranty that includes the CRT.

On top: the 2246 with exclusive integrated push-button measurements. Your measurements are accessed through easy, pop-up menus and implemented at the touch of a button. Measure ± peak volts, peak-to-peak, dc volts and gated volts with new hands-off convenience and on-screen readout of values.

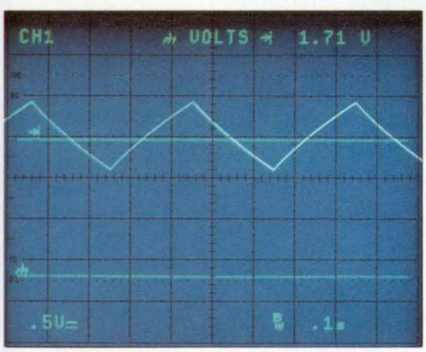
SmartCursors™ track voltmeter measurements in the 2246 and visually indicate where ground and trigger levels are located. Or use cursors in the manual mode for immediate, effortless measurement of waveform parameters like voltage, time, frequency, and phase.

Both scopes build on performance you haven't seen at the bandwidth or prices. Lab grade features include sweep speeds to 2 ns/div. Vertical sensitivity of 2 mV/div at full bandwidth for low-level signal capture. Plus trigger sensitivity to 0.25 div at 50 MHz, to 0.5 div at 150 MHz.

Features	2246	2245
Bandwidth	100 MHz	100 MHz
No. of Channels	4	4
Scale Factor Readout	Yes	Yes
SmartCursors™	Yes	No
Volts Cursors	Yes	No
Time Cursors	Yes	No
Voltmeter	Yes	No
Vertical Sensitivity	2 mV/div	2 mV/div
Max. Sweep Speed	2 ns/div	2 ns/div
Accuracy: Vert/Hor	2%/2%	2%/2%
Trigger Modes	Auto Level, Auto, Norm, TV Field, TV Line, Single Sweep	
Trigger Level Readout	Yes	No
Weight	16.5 lb/7.5 kg	16.5 lb/7.5 kg
Warranty	3-year on parts and labor including the CRT	
Price	$2400	$1875



Conventional ΔTime measurement is also available from the menu in the 2246 for increased timing accuracy. Shown above: a ΔTime measurement of pulse width.



The 2246 also makes it possible to measure either ΔVolts or absolute volts from ground.

Best of all, high performance comes with unmatched convenience. You can see it and feel it—in the responsive controls and simple front-panel design, in extensive on-screen scale factor readouts, and in simplified trigger operation that includes Tek's Auto Level mode for automatic triggering on any signal. Start to finish, the GPS Series saves steps and simplifies tasks.

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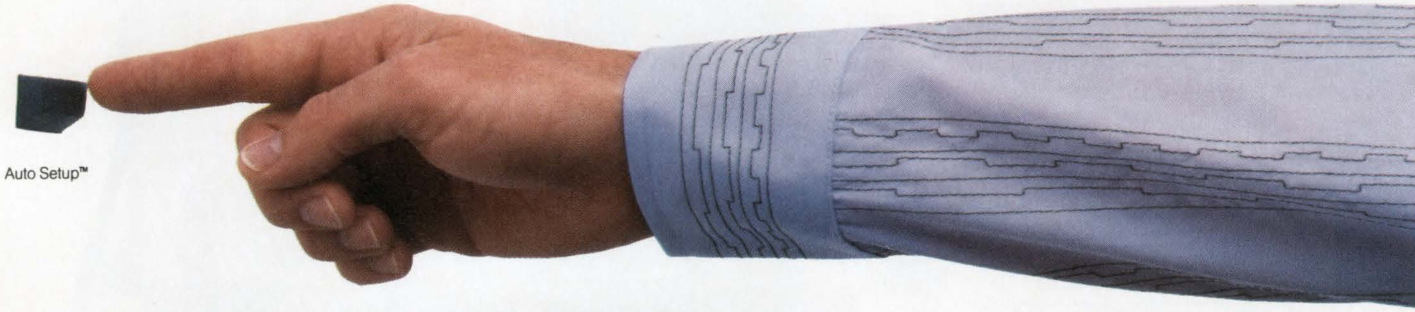
CIRCLE NO 155

The easiest setup in logic analysis?



You just put your finger on it.

Gould introduces Auto Setup™: from zero to 200 MHz in 26 seconds.

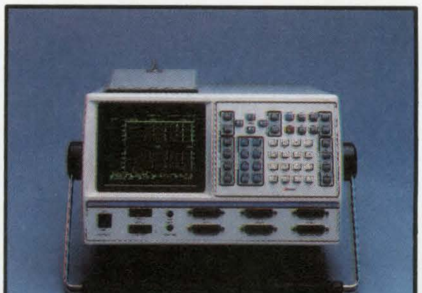
Gould already makes the industry's most powerful logic analyzer—the K450. Now, we make the easiest to use—the K450 with Auto Setup.™

Press a key, wait less than 30 seconds and, voila, you're ready to go.

What does Auto Setup™ do for you? Everything but connect the probes.

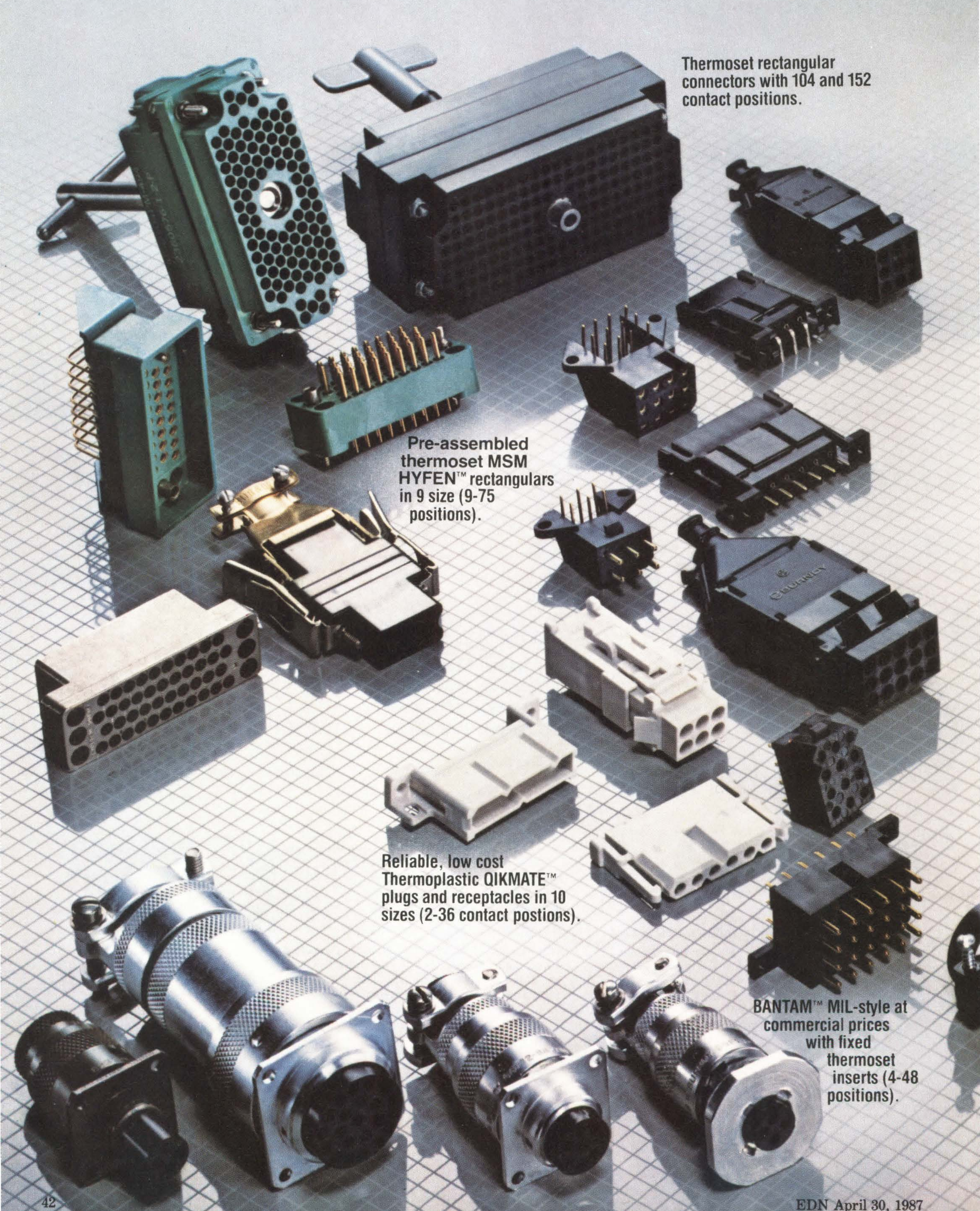
It checks probes for activity, sets the threshold, chooses the appropriate clock speed and arranges the channels on the screen, so that you can see exactly what you captured... instantly.

All high speed channels (24 at 200 MHz, 48 at 100 MHz) give you resolution to 5 ns. Sixteen interactive levels of Trace Control™ recognize and record the exact state/timing event you want. No other analyzer offers better triggering.



Gould K450. The industry's most sophisticated analyzer is now the easiest to use.

The one interconnect system



you never outgrow! TrimTrio™

Single contact system satisfies over 100,000 interconnect variations.

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Closed barrel Machined Contacts for both crimp and wire-wrap power applications up to 13 amps. **Open barrel Precision Formed** contacts for power and signal applications. **Sub-miniature Coax** (one-piece or 2-piece) for coaxial cable, shielded conductors and twisted pairs. These three basic types (with variations for different conductors, contact platings and termination options) make up the TRIM-TRIO contact system. All can be intermixed in any of scores of Burndy connector housings designed around this contact system.

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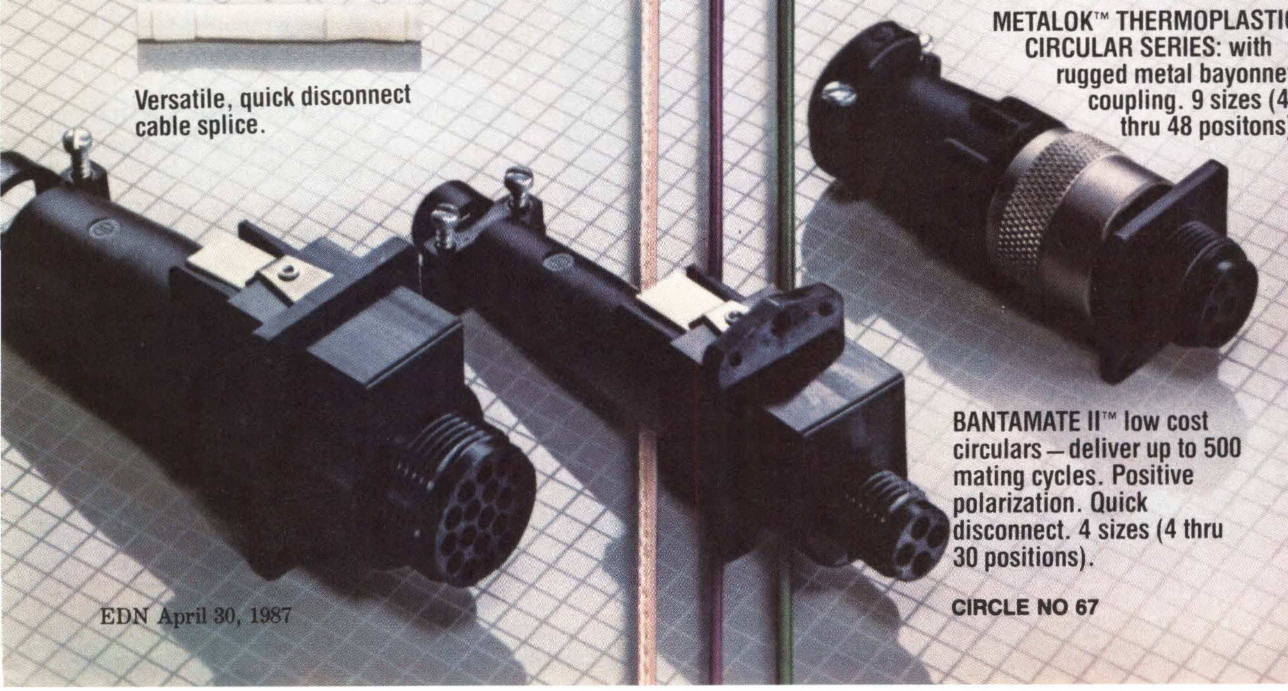

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CIRCLE NO 67

CALENDAR

Hands-on Programming in C, Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. May 12 to 15.

First Annual Disk Drive Components Review, Sunnyvale, CA. Technology Review Manager, Peripheral Research Corp, (805) 963-8081 or (805) 494-4413. May 12.

Opportunities in Flat-Panel Displays, Boston, MA. Ronnie Sarkar, Arthur D Little Inc, 15 Acorn Park, Cambridge, MA 02140. (617) 864-5770, ext 2377. May 18.

EMC Expo, San Diego, CA. EMC Expo, Box D, Gainesville, VA 22065. (703) 347-0030. May 19 to 21.

Satellite Communications (short course), Sunnyvale, CA. Continuing Education Institute, 21250 Califa St, Woodland Hills, CA 91367. (818) 710-1142. May 19 to 21.

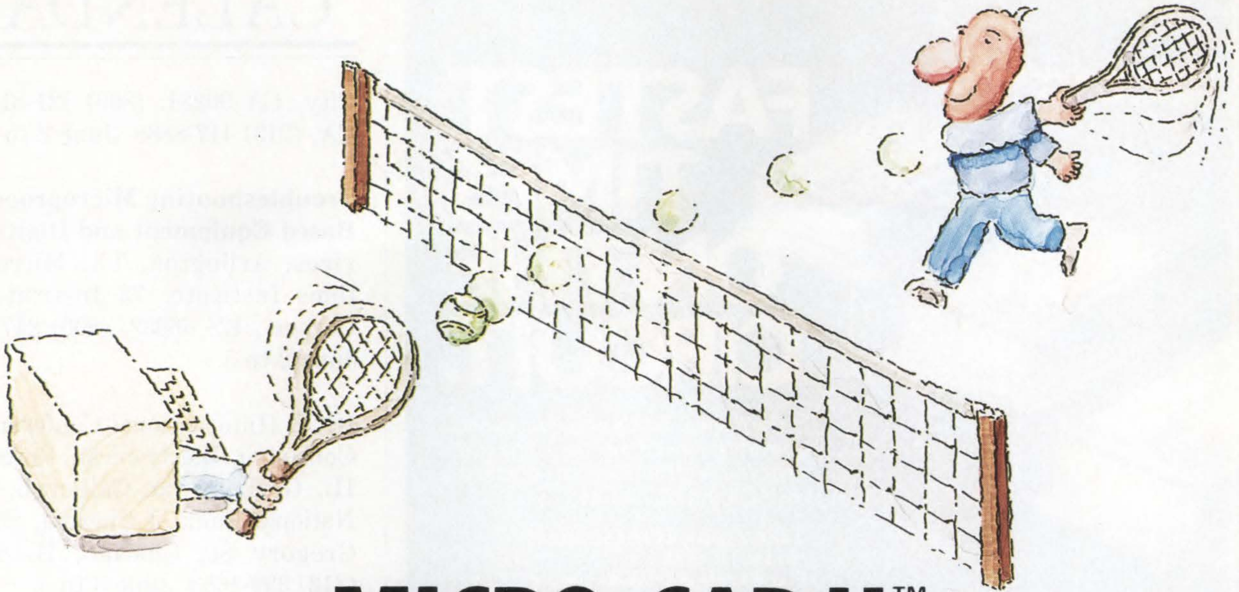
41st Annual Frequency Control Symposium, Philadelphia, PA. Synergistic Management, Box 826, Belmar, NJ 07719. (201) 280-0410. May 27 to 29.

International Workshop on Computer-Aided Software Engineering, Cambridge, MA. Index Technology Corp, 101 Main St, Cambridge, MA 02142. (617) 491-2100, ext 8000. May 27 to 29.

Personal Computer Interfacing for Scientific Instrument Automation, Blacksburg, VA. Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. (703) 961-4848. May 28 to 30.

Comdex/Spring, Atlanta, GA. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. June 1 to 4.

Hands-on Programming in C, Washington, DC. Integrated Computer Systems, Box 3614, Culver



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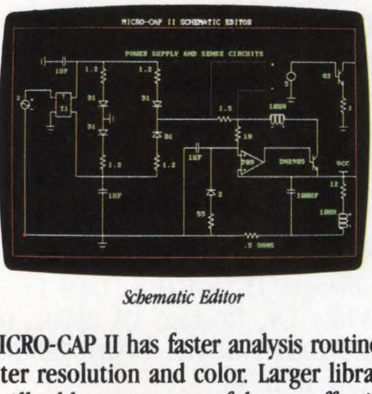

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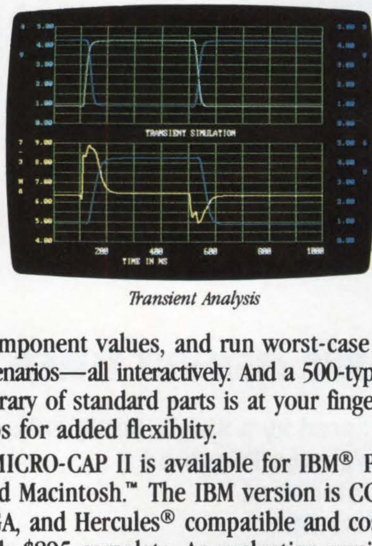

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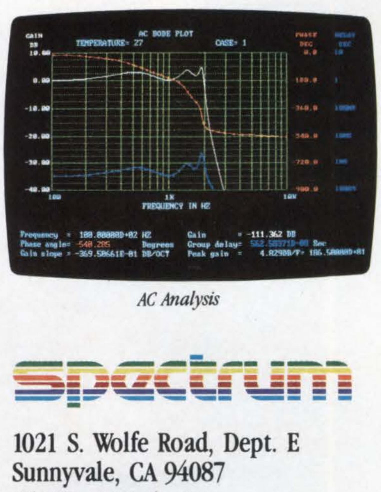

AC Analysis

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CIRCLE NO 143

City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. June 2 to 5.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Arlington, TX. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239. June 2 to 5.

ICCE (International Conference on Consumer Electronics), Rosemont, IL. Geriann Van Calbergh, First National Bank of Chicago, 8528 W Gregory St, Chicago, IL 60656. (312) 399-1653. June 3 to 5.

ISHM Europe (European Microelectronics Conference and Exhibition), Bournemouth, UK. Concorde Services, 10 Wendell Rd, London W12 9RT UK. 01 743 3106. June 3 to 5.

IEEE MTT-S International Microwave Symposium, Las Vegas, NV. Steven March, Symposium Steering Committee Chairman, Maury Microwave Corp, 8610 Helms Ave, Cucamonga, CA 91730. (714) 987-4715. June 9 to 11.

University /Government /Industry Microelectronics Symposium, Rochester, NY. Lynn Fuller, Rochester Institute of Technology, 1 Lomb Memorial Dr, Rochester, NY 14623. (716) 475-2035. June 9 to 11.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239. June 9 to 12.

National Computer Conference, Chicago, IL. AFIPS, 1899 Preston White Dr, Reston, VA 22091. (800) 622-1987; in VA, (703) 620-8955. June 15 to 18.

ISDN, Atlanta, GA. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (617) 232-3111. June 15 to 19.


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Fluorinert Liquids, used as a direct contact heat transfer medium, offer a range of physical properties that make them particularly suitable for electronic uses. They are non-polar and exhibit no solvent action. They are colorless, low in toxicity, non-flammable and offer exceptionally high dielectric strength plus thermal and chemical stability. Most important, they have almost no chemical reactivity and they evaporate without leaving a residue on parts.

Buy the numbers

Our FC™ numbers — FC-40, FC-70, FC-77, etc. — are used to identify Fluorinert Liquids that offer certain physical characteristics to meet specific application needs. These FC numbers are solely 3M designations for various fluorochemical products.

Fluorinert Liquids are being used cost-effectively in cooling, high reliability testing and vapor phase soldering operations. When you are interested in applying these versatile liquids in your own production, 3M can provide an abundance of technical information and support.

Technical assistance: the main benefit of Fluoronics Resources

3M offers prompt assistance to help you solve many production and testing problems. We provide comprehensive technical recommendations for specific fluids. We consult with you on the proper application equipment and help you evaluate production methods and results. Our service bulletins bring you up to date on the most recent advances in vapor phase soldering and high reliability testing. Ask us about 3M's audiovisual materials and on-site application training seminars.

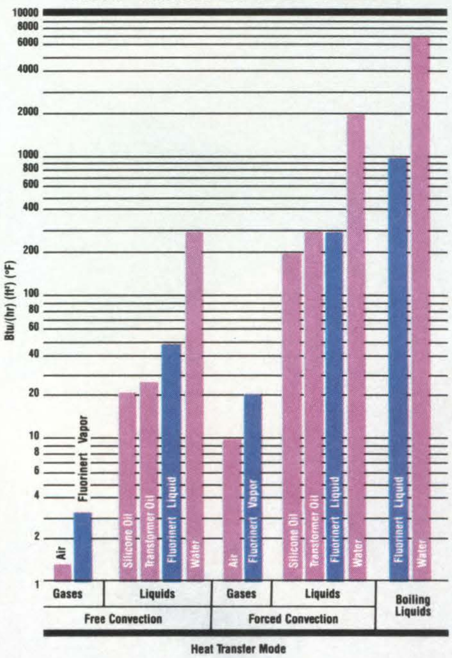
Discover Fluorinert™ Liquids' heat transfer capability

What are your needs? A precise degree of temperature control? Fast, uniform heat transfer? High dielectric strength? Fluorinert Liquids offer the broad range of physical characteristics required in most applications.

Fluorinert Liquids are an effective direct contact heat transfer medium whether used in a liquid or vapor state. Their unique properties enable you to use them in contact with sensitive components and substrates.

Major differences between the various products in the Fluorinert Liquids family can be seen in their boiling points. These can range from 56°C to 253°C. Should you need products with intermediate boiling temperatures, the 3M staff will work with you to fashion a product especially for your needs. It's an example of how 3M's Fluoronics Resources provide you with "customized" service to solve special problems.

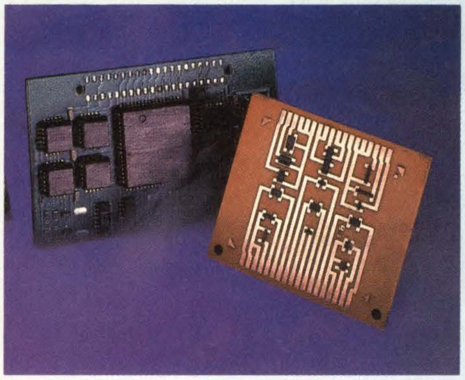
COMPARATIVE HEAT TRANSFER COEFFICIENTS



Fluorinert™ Liquids achieve accurate high reliability testing

It's a small world you work in. Where time ticks in nanoseconds and dimension is measured in Angstrom units. And as circuitry becomes more complex, a greater demand is placed on testing capability — not only in speed, but in higher reliability and accuracy.

Fluorinert Liquids meet those requirements by providing a controlled temperature environment and a high degree of electrical protection. They offer maximum compatibility between



the heat transfer medium and the device under test. Fluorinert Liquids reduce testing costs by reducing testing time substantially. They do this by rapidly reaching test temperature and providing precise and uniform temperature control. You'll minimize the number of faulty units by detecting defects before they become rejects.

These liquids provide cost-effective tests such as gross leak, thermal shock, liquid burn-in, ceramic crack detection, electrical environmental, temperature calibration and failure analysis/short detection.

Fluorinert Liquids are specified in the MIL-STD's for thermal shock and gross leak testing.

THERMAL SHOCK TEST CONDITIONS

Military Standard 883-1011			Military Approved Fluorinert Liquids	
Test Condition	Hot Test Step 1	Cold Test Step 2	Hot Test Step 1	Cold Test Step 2
A	100°C	−0°C	Water , FC-40	Water , FC-40, FC-77
B	125°C	−55°C	FC-40, FC-70, FC-5311	FC-77
C	150°C	−65°C	FC-40, FC-70, FC-5311	FC-77
D	200°C	−65°C	FC-70, FC-5311	FC-77
E	150°C	−195°C	FC-40, FC-70, FC-5311	Liq. N_2
F	200°C	−195°C	FC-70, FC-5311	Liq. N_2

GROSS LEAK TEST CONDITIONS

Military Standards	Military Approved Fluorinert Liquids		
	Indicator Fluids	Detector Fluids	Absorption Fluids
MIL-STD 883-1014	FC-40, FC-43	FC-72, FC-84	Do not apply
MIL-STD 750-1071	FC-40, FC-43	FC-72, FC-84	FC-43, FC-75, FC-77
MIL-STD 202-112	FC-40, FC-43	FC-72, FC-84	Do not apply

Discover higher yields in vapor phase soldering

Fluorinert Liquids have been the industry's fluid of choice since the vapor phase reflow soldering (VPS) process was introduced in 1975. There are a number of good reasons for this universal acceptance. VPS with Fluorinert Liquids produces highly reliable solder joints. The system reduces reject rates, increases production, and lowers production costs. With Fluorinert Liquids, you can be assured that your products will never be exposed to a temperature higher than the selected liquid's boiling point. (See above)

You'll avoid those problems usually associated with other systems — shadowing, uneven heating, and overheating. The liquids are non-flammable. Their low surface tension helps them evaporate quickly from the work pieces without leaving a residue.

VPS with Fluorinert Liquids is especially suited for boards with high mass or complex geometries. The liquid vapors completely surround the assembly and penetrate remote recesses to heat all surfaces evenly. The vapors are 15 to 20 times heavier than air so they can be contained easily within the work area. The system offers an oxygen-free, non-corrosive environment to minimize rejects from oxidation contamination.

Some typical applications using Fluorinert Liquids in VPS include surface mounted leaded or leadless components, through-hole leads and wire-wrap pins, lead frame attachment, reflow of electroplated solder or tin and miscellaneous metal joining.

VPS SELECTION GUIDE

Fluorinert Liquid	Boiling Point	Typical Solders
FC-43	174°C/345°F	70 Sn/18 Pb/12 In 100 In 58 Sn/42 In 58 Bi/42 Sn
FC-70, FC-5311 FC-5312	215°C/419°F	63 Sn/37 Pb 60 Sn/40 Pb 62 Sn/36 Pb/2 Ag
FC-71	253°C/487°F	100 Sn 95 Sn/5 Ag 60 Pb/40 Sn

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Thermal Conductivity Btu/(hr) (ft^2) (°F/ft)	0.037	0.033	0.008
Specific Heat Btu/(lb.) (°F)	0.25	0.28	0.23
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Coefficient of Thermal Expansion ft^3/(ft^3) (°F)	0.0008	0.0009	0.0015

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EDITORIAL

Hands off, Uncle Sam

If you think the US government does a good job of managing projects, consider two of Uncle Sam's recent ventures: tax simplification and arms sales to Iran. After such snafus, it seems wise to keep the government's involvement in most affairs to a minimum. However, industries and trade associations such as the Semiconductor Industry Association (SIA) continue to petition for government aid. The SIA's members want Congress to provide funds for the Semiconductor Manufacturing Technology Institute (Sematech). The institute's goal is to help US semiconductor companies compete with foreign manufacturing technology.

Facing similar competitive pressures from overseas manufacturers, 10 US companies founded the Microelectronics and Computer Technology Corp (MCC) in 1982. MCC now embraces 17 members, each of which contributes to the group's cooperative research into emerging technologies. The group receives no government money. Although MCC's research has yet to produce major new products, the corporation continues to attract new members. Sematech should follow a similar course, drawing its funds and expertise from member companies. The semiconductor industry cannot rely on government grants alone to fund manufacturing research and development.

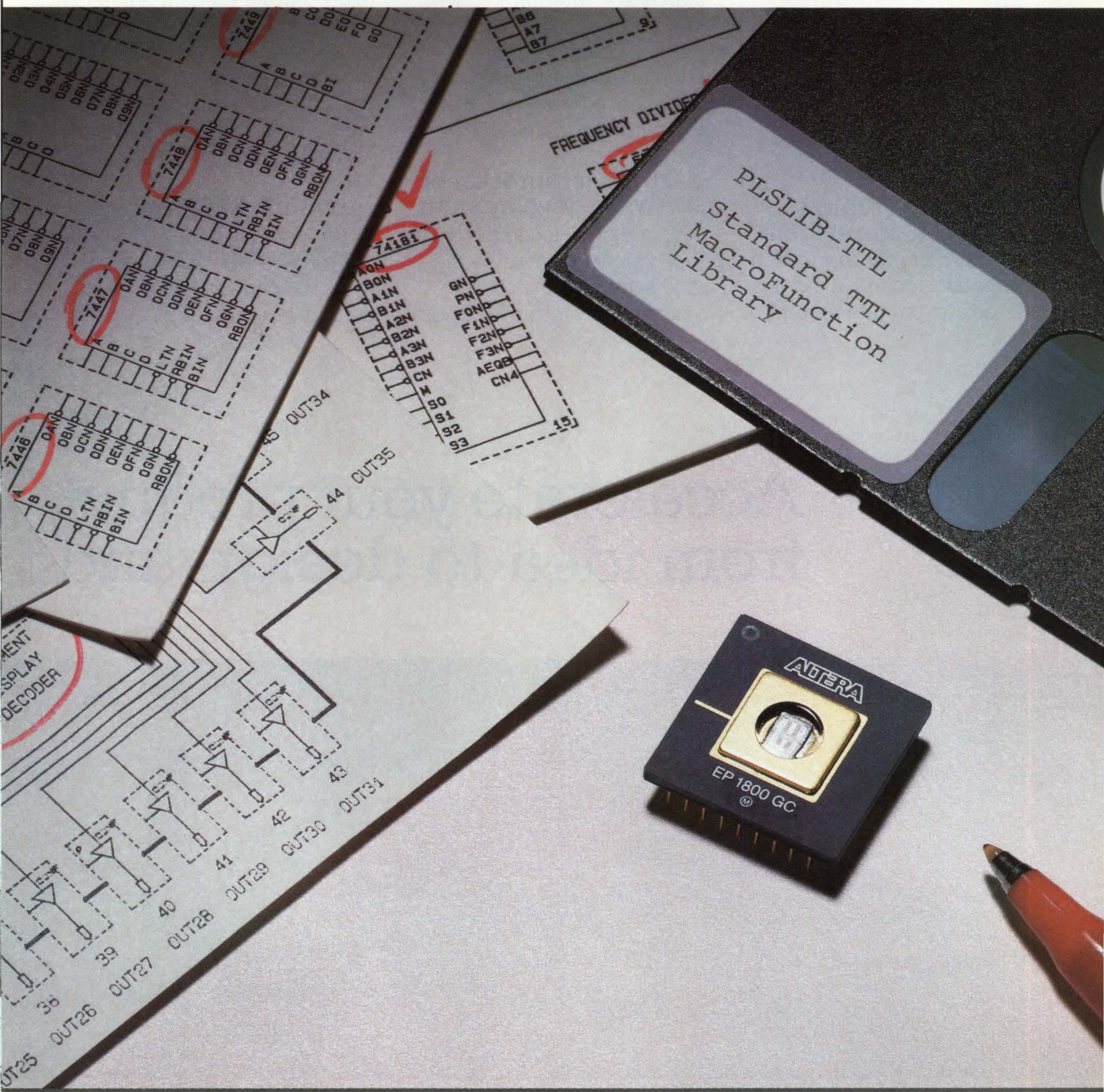
Surprisingly, the Department of Defense agrees. Its Defense Science Board recommends that a private-industry consortium tackle the development of 64M-bit memory chips. Member companies would contribute $250 million in start-up money, and the DoD would contract for $200 million worth of research each year.

So far, though, Sematech's role is undecided. For example, Intel's executives argue that Sematech should manufacture and sell chips on the open market. Executives at IBM, however, want an organization that develops manufacturing technology to be licensed for use by all member companies.

The Sematech consortium sounds like a good idea. Once it decides where it is going, it can make a major contribution to developing new semiconductor-manufacturing technologies. The US government, however, has a poor record of bringing its ventures to profitable conclusions. The government's handouts are tempting, but let's keep Sematech in private hands.

Jon Titus
Editor

Terms.



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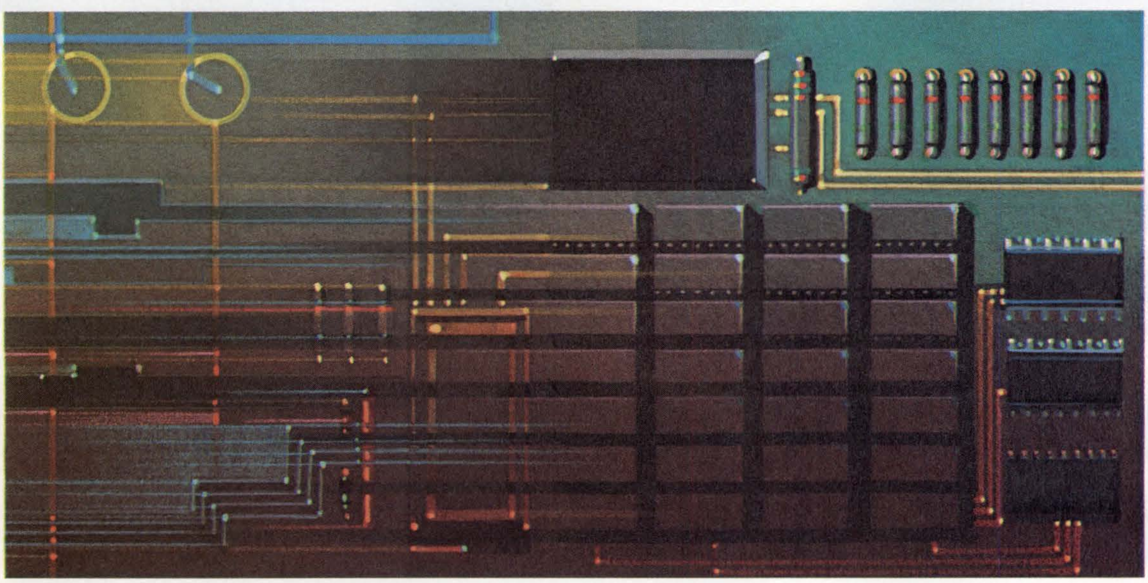

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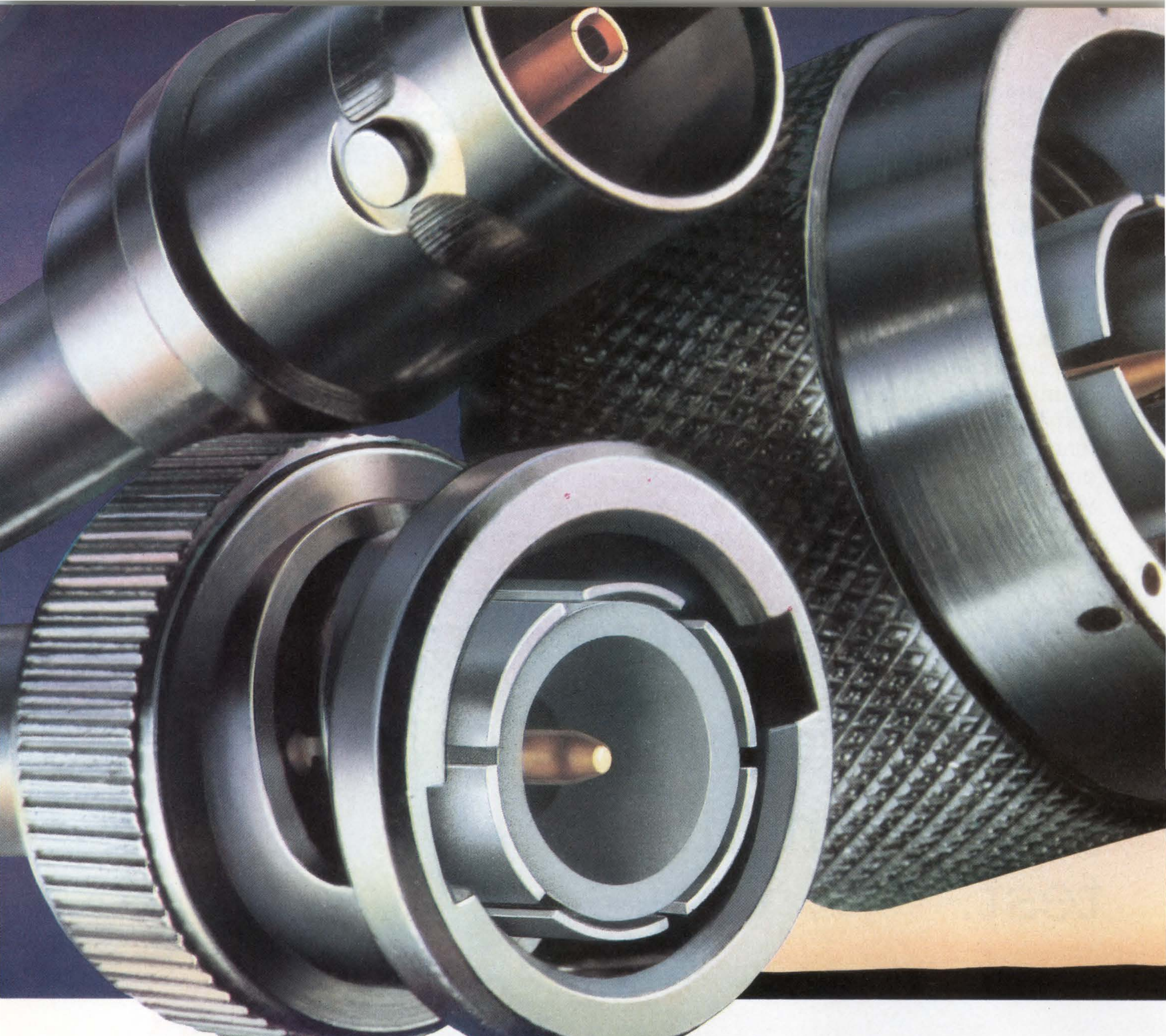

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AMP Interconnecting ideas

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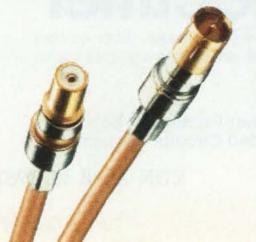

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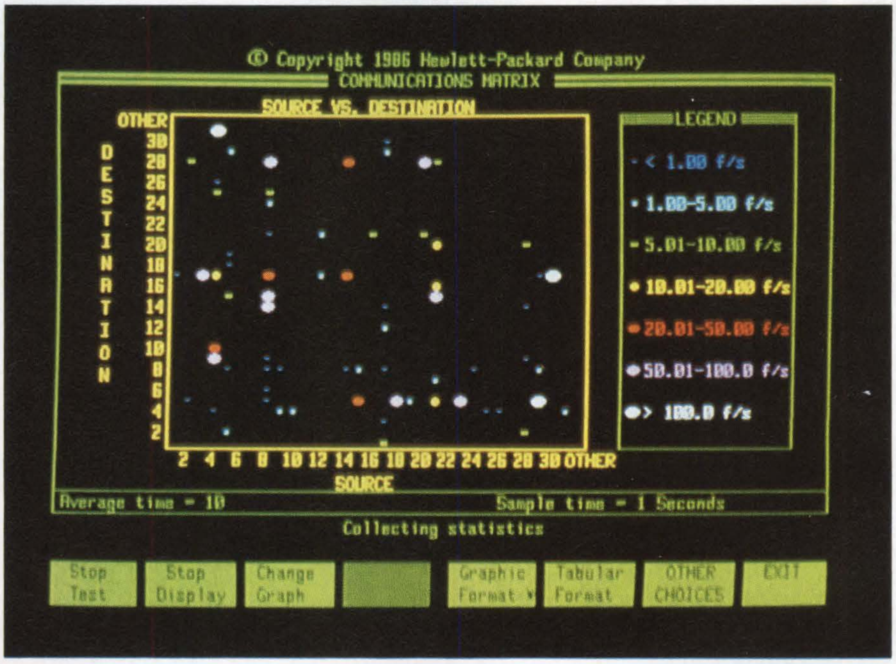
CIRCLE NO 107

IEEE 802.3 LAN testers and analyzers pinpoint network and equipment flaws

Steven H Leibson,
Regional Editor



***You can monitor communications among 31 nodes** with this communications display by using the optional LAN-performance software package on the Hewlett-Packard 4971S protocol analyzer.*

Troubleshooting an Ethernet local-area network can be a complex problem; sometimes magic seems to be the only solution. But instead of reaching for beads and rattles or a book of incantations the next time you have to troubleshoot a LAN, consider using equipment specifically designed for testing networks. Whether you're measuring the performance of a new network-protocol software release, testing your product's LAN interface, persuading products from different manufacturers to talk to each other over the net, resuscitating a crashed network, or just tuning a LAN for peak performance, you'll find that a LAN physical tester or protocol analyzer can make your job much easier.

Ethernet LANs are complex, comprising seven layers in what is generally called the OSI (open system interconnection) model developed by the International Organization for Standardization (ISO). In addition to the seven layers it explicitly describes, the model implies another layer (layer 0), the transmission medium **(Fig 1)**. Ethernet LANs usually implement layer 0 with a double-shielded coaxial cable.

Each network layer represents one or more physical components built from software, hardware, or a combination of both software and hardware. Any of these components can fail or be improperly designed. In addition, networks can include dozens or hundreds of nodes, each incorporating this complex, layered structure. Locating a network problem in all of this complexity is like looking for a needle in a haystack.

Xerox developed the Ethernet LAN more than a decade ago, and the IEEE published its Ethernet-based 802.3 standard in 1985. (In this article, the word "Ethernet" refers to both the Xerox LAN and the IEEE 802.3 LANs.) Ethernet LANs use a bus-contention protocol called the CSMA/CD (carrier sense, multiple access with collision detection), and they have a bus network topology. Although LANs using this technology have been operational for more than 10 years, instrument vendors started offering equipment for Ethernet LAN troubleshooting only within the last few years.

Strictly speaking, Ethernet and IEEE 802.3 define layer 1 and the media-access control (MAC) sublayer of layer 2. Within layer 1, a media-access unit (MAU, also called a transceiver) couples data-terminal equipment (DTE) to the transmission medium. The MAC sublayer defines the bit sequence (called a MAC frame or packet) used to transmit information over the LAN **(Fig 2)**.

The instruments for locating Ethernet LAN problems fall into two categories: physical testers and protocol analyzers. The physical testers, which cost less than protocol analyzers, test only the network protocol layers specified by IEEE 802.3 (layer 1 and the MAC sublayer) by checking individual LAN hardware components (cables and transceivers) for correct operation and certifying that these components are properly interconnected. Protocol analyzers perform some tests on the lower protocol layers but excel at studying communications in the upper layers.

The transceivers that are com-

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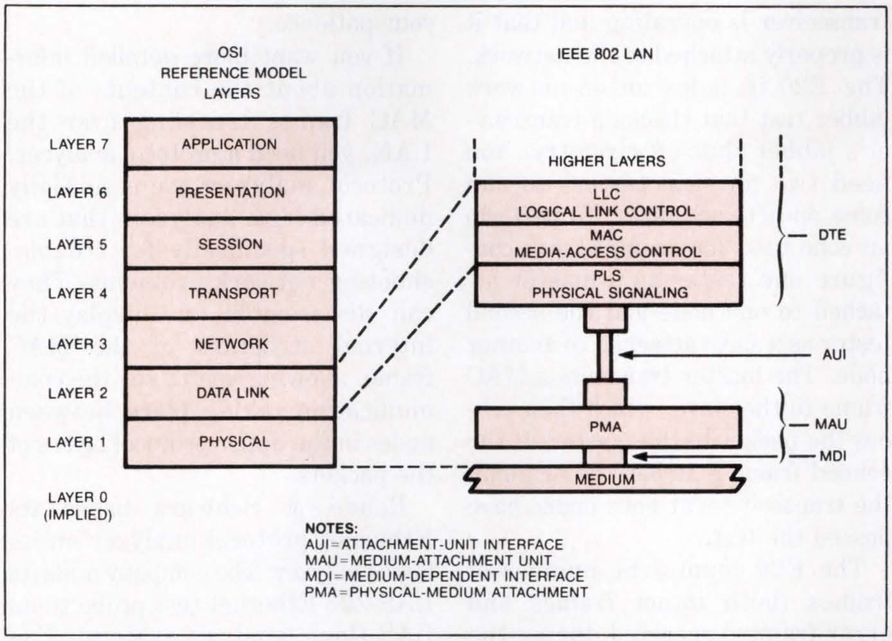


Fig 1—ISO's open system interconnection *(OSI) model specifies seven layers, but the IEEE 802.3 standard and Ethernet define only layer 1 and the media-access control (MAC) sublayer of layer 2. The LAN's transmission medium represents an implied layer 0.*

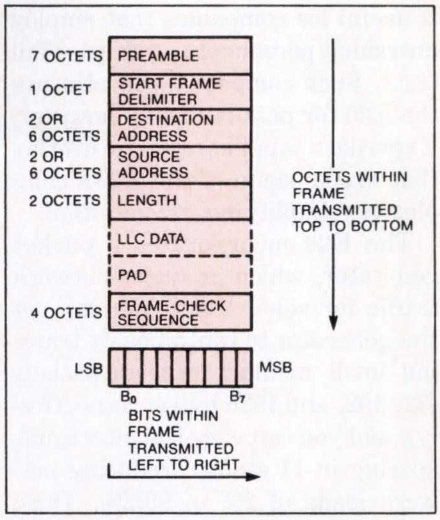


Fig 2—The MAC frame defined in the IEEE 802.3 standard *comprises seven fields. All the protocols above the MAC sublayer reside within the MAC frame's data field. The 802.3 standard refers to 8-bit octets, commonly called bytes. Short frames use pads within the data field to attain the standard's 64-octet minimum legal size.*

monly used for implementing Ethernet LANs couple to the double-shielded coaxial cable through a side-entry connection called a vampire or stinger tap and employ baseband signaling. However, some vendors offer broadband and fiber-optic transceivers and transmission media. For LAN testing purposes, the key feature common to Ethernet transceivers employing any transmission medium is the attachment-unit interface (AUI), which is physically embodied in a standard, 15-pin D connector. This interface and the associated AUI cable provide entry points into the LAN for testing.

When you're testing a product's network interface for correct operation, you need to ensure that the AUI cables and transceivers you use in the tests are functioning properly. Experdata's E20 and Cabletron's LAN MD both certify AUI cables and transceivers (see **Table 1**). These testers also verify that the transceivers are properly mated to the transmission medium. The E20's built-in time-domain reflectometer (TDR) allows you to locate short and open circuits on the network's coaxial cable.

Although Cabletron's LAN MD and Experdata's E20 testers appear to be physically similar, the instruments' features and operation differ. Both testers employ numeric LED displays; however, the LAN MD uses the numeric indicator to show test-status codes, and the E20 displays numeric information that includes the number of frames transmitted, collisions detected, and frames received with errors. Because it gives you this numeric data, the E20 lets you obtain quantitative as well as qualitative test results. The LAN MD gives you predefined status codes instead of quantitative test results.

The LAN MD's simpler operation

TABLE 1—PHYSICAL-LAYER TESTERS

	TESTS								
	TRANSCEIVER TESTS								
	OFF-NET	ON-NET	JABBER	ECHO TEST	COLLISION TEST	BERR TEST	TDR	TRANSMITTER LEVELS AND COLLISION THRESHOLDS	ROUND-TRIP DELAY TEST
CABLETRON LAN MD ($4000)	YES	YES	NO	YES	YES	NO	NO	YES	NO
EXPERDATA E20 ($4500)	YES	YES	YES	YES	YES	YES	YES	$185 OPTION	YES

NOTES:
1. THE E20 PROVIDES FOR TRAFFIC MEASUREMENT AND HAS A TRAFFIC GENERATOR; THE LAN MD DOES NOT.
2. BOTH INSTRUMENTS PROVIDE DROP CABLE.
3. THE LAN MD'S ECHO TEST REQUIRES TWO TESTERS.
4. THE E20'S ECHO, COLLISION, LINE-QUALITY, AND ROUND-TRIP DELAY TESTS REQUIRE TWO TESTERS.

is useful for companies that employ untrained personnel to run pass/fail tests. Such companies can also use the E20 for pass/fail tests, however: Experdata supplies a plastic overlay that masks some of the E20's complexity, simplifying its operation.

The E20 incorporates a packet generator, which produces network traffic for some tests. You can set the generator to continuously transmit small, medium, or large packets (72, 192, and 1526 bytes, respectively), and you can vary the interframe spacing in 11 steps, producing network loads of 2% to 99.2%. Thus, the generator can simulate network growth (more active nodes and more network traffic), allowing you to see how the devices on the LAN would respond to this extra traffic.

Both testers check transceivers for proper transmission and reception on and off the network. Off-network tests check a transceiver's basic components: the transmitter, receiver, and collision detector. One advantage the LAN MD enjoys over the E20 in testing transceivers is the ability to measure a transmitter's output-voltage levels and collision-detection thresholds by means of an off-network test. For the E20, this feature costs an extra $185.

On-network tests prove that the transceiver is operating and that it is properly attached to the network. The E20 includes an on-network jabber test that checks a transceiver's jabber shut-off circuitry. You need two physical testers to run some on-network tests. To perform an echo test, for example, you configure one tester as a master attached to one node and the second tester as a slave attached to another node. The master transmits a MAC frame to the slave, which then echoes the packet to the master. If the echoed frame matches the original, the transceivers at both nodes have passed the test.

The E20 counts the number of frames (both intact frames and error frames) received during the echo test and displays this information, yielding bit-error-rate information. Experdata suggests that this test is especially helpful in finding insidious shorts—for example, the kind that occurs when one strand of the coaxial cable's shield braid touches the transceiver's stinger contact intermittently, depending on cable flexure, vibration, or temperature. Unless you use a tester like the E20, finding such a short, which masquerades as an intermittent hardware or software problem in a DTE, can really test your patience.

If you want more detailed information about the contents of the MAC frames traveling over the LAN, you need a protocol analyzer. Protocol analyzers are essentially dedicated logic analyzers that are designed specifically for troubleshooting network problems. They can disassemble and display the internal structure of the MAC frame, allowing you to see the communication taking place between nodes in the upper protocol layers of the packets.

Rohde & Schwarz bases its Ethernet protocol analyzer on its logic analyzer: The company adds its LAS-Z23 Ethernet test probe to its LAS (logic analysis system). The test probe (which is available separately and costs DM 9080) incorporates shift registers that link a network transceiver's receiver and transmitter sections to several of the logic analyzer's data-capture and word-generator channels, respectively. You can measure interframe timing and network loading by using the system's event-timing analysis features, and you can create traffic with its logic generator.

The Ethernet disassembler supplied with the LAS-Z23 probe allows you to set filters and triggers

Although they look similar and perform similar tests, these LAN testers, *the E20 from Experdata (above) and the LAN MD from Cabletron (left), present their results differently. The Experdata tester presents numeric results; the Cabletron unit gives status codes.*

CIRCLE NO 138

so that the analyzer can selectively capture packets and present the captured information in fields resembling the MAC-frame format. Packet-filtering criteria based on preamble, source, destination, type, data, and frame-check-sequence (FCS) fields within the packet determine what information the analyzer keeps in its memory. The analyzer can also catch "runt" packets, frames shorter than 64 bytes.

To fit more frames into the analyzer's memory, you can choose to retain only portions of the captured packets. For example, if you are interested only in the number of packets exchanged between two nodes, you would set the analyzer to save only the address fields from the packets and discard the other infor-

The $49 LAN analyzer

If you need to analyze LAN performance for networks based on IBM PCs, you might want to try the $49 Smart LPT (LAN performance tester) from Innovative Software (Lenexa, KS). The software tests many different kinds of network hardware (not just Ethernet or IEEE 802.3 networks) from various manufacturers and includes drivers for LANs that use Novell's Advanced Netware and IBM's Netbios.

The test software employs a unique stimulus for evaluating LAN performance: It directs file requests to a word processor, spreadsheet, and database manager contained within a demonstration version of the company's network-compatible, integrated applications software, Smart. You install Smart, which comes with Smart LPT, on the network's file server. You can use this product to compare the performance of LAN hardware products from various manufacturers and to measure the effect of having different numbers of active users on a network.

The product allows you to specify the nodes' activity level for each simulation test. Plotting routines built into the software provide reports of the test performance, thus helping you to justify the purchase of one vendor's network over another's or to fine-tune the network-interface parameters in a file server for a given number of users.

TABLE 2—ETHERNET AND IEEE 802.3 PROTOCOL ANALYZERS

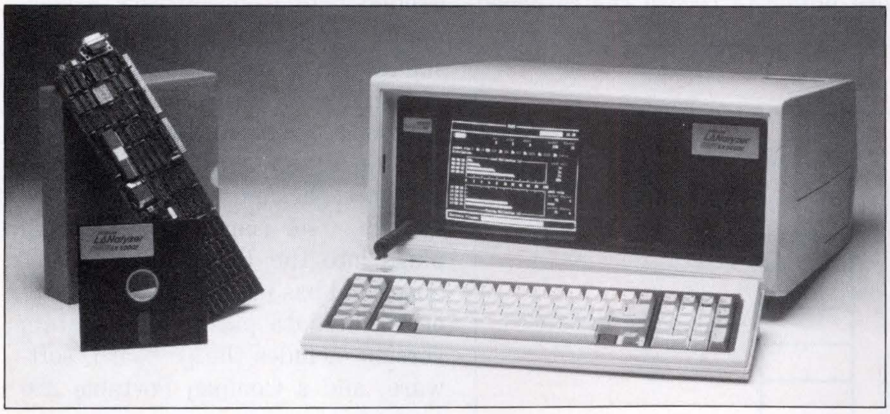
MANUFACTURER	MODEL	CAPTURE BUFFER (BYTES)	FILTER CHANNELS	GENERATOR CHANNELS	FILTER PROTOCOLS SUPPLIED	USER-DEFINED PROTOCOLS
COMMUNICATION MACHINERY CORP	DRN-1700 LANSCAN	192k	1	1	TCP/IP XNS ISO	NO
EXCELAN	EX5000E LANALYZER	700k	8	6	TCP/IP XNS ISO DECNET	YES
	EX5000EP LANALYZER	700k	8	6	TCP/IP XNS ISO DECNET	YES
HEWLETT-PACKARD	HP4971S	1M	16	16	TCP/IP XNS DECNET	YES
NETWORK GENERAL	SNIFFER	256k	1	1	TCP/IP XNS ISO SMB CORE NFS	YES
ROHDE & SCHWARZ	LAS 07	7k	12	1	NONE	NO

NOTES:
1. THE HP4971S COSTS $18,541. YOU MUST ADD $1390 TO $4450 FOR A DUAL FLOPPY-DISK DRIVE OR A HARD-DISK/FLOPPY-DISK PERIPHERAL AND $1495 FOR A VIDEO INTERFACE, MONOCHROME VIDEO DISPLAY AND KEYBOARD OR $2150 FOR A VIDEO INTERFACE, COLOR VIDEO DISPLAY, AND KEYBOARD.
2. YOU CAN ADD ANALYSIS CAPABILITY FOR IBM TOKEN-RING LANs TO THE SNIFFER FOR AN EXTRA $5000.

mation contained in the frame.

The LAS protocol analyzer can also simulate a LAN, so you can perform tests on a DTE without a network. The analyzer's probe simulates a network transceiver and communicates directly with the DTE. You can create stimulus/response programs by using the CP/M-86 operating system and Basic programming language supplied with the analyzer. This configuration gives you a tightly controlled system for conducting tests on unproven DTE hardware and software without wreaking havoc on an operational LAN.

Hewlett-Packard's 4971S protocol analyzer reveals its heritage through its keystroke-programming language, which is similar to those incorporated in the company's logic analyzers. The keystroke-programming language allows you to configure the analyzer's 16 filters, which accept address fields, type fields, and as many as 46 bytes within the packet's data field as capture criteria. You can program each filter to look for errors such as bad FCS fields, misaligned frames, and runt frames, and you can specify frame length as a filter parameter.



Available as a pc board and as a system, *the Excelan EX5000 LAN protocol analyzer provides eight capture filters and six packet generators. The system versions include a Compaq Portable 286 computer as the host machine.*

NO OF SYMBOLIC NAMES	CONTINUOUS LOG TO DISK	TIME-STAMP RESOLUTION	TDR	PRICE	COMMENTS
75	NA	NA	YES	$8500	ALSO AVAILABLE FROM SPIDER SYSTEMS (EDINBURGH, UK)
100 PER FILE	YES	10 μSEC	YES	$9500	PC BOARD PLUGS INTO PC OR PC/AT BUS; FREE DEMO DISK AVAILABLE
100 PER FILE	YES	10 μSEC	YES	$19,500	FREE DEMO DISK AVAILABLE
1000	YES	32 μSEC	NO	$21,426 TO $25,141[1]	
>100	NO	1 mSEC	NO	$19,000[2]	FREE DEMO DISK AVAILABLE
12	NO	100 nSEC	NO	DM 52400	

KEY:
TCP/IP=TRANSMISSION CONTROL PROTOCOL/INTERNET PROTOCOL
ISO=INTERNATIONAL ORGANIZATION FOR STANDARDIZATION'S OPEN SYSTEM INTERCONNECTION
XNS=XEROX NETWORK SERVICES
CORE=NOVELL CORE PROTOCOL
SMB=SYSTEM MESSAGE BLOCK (FOR IBM PC NETBIOS SYSTEMS)
NFS=SUN MICROSYSTEMS' NETWORK FILE SYSTEM
NA=NOT APPLICABLE

The 4971S filters are capable of more than simple byte matching within the MAC frame. Various standards define some of the layers above the MAC sublayer, creating subfields inside the MAC frame's data field. Hewlett-Packard supplies several predefined protocol definitions (listed in **Table 2**) that allow you to work with packets at the protocol level instead of the byte level. If the files supplied by the company don't cover your application, you can define your own protocols.

The $2000 18212A LAN-performance analysis software allows the 4971S to display a histogram showing the network's usage of selected node addresses plus the total network usage as a percentage of available bandwidth. You can select the communications matrix display that plots traffic among 31 user-selected node addresses. For systems with monochrome displays, the matrix indicates increasing traffic between nodes by using varying dot intensities; for systems equipped with color monitors, it uses different colors.

The 4971S contains 16 packet-generating channels, which can each send packets ranging from 5 to 2026 bytes (including the FCS) onto the network. Note that these limits exceed those specified by the IEEE 802.3 standard, so you can inject oversized and undersized frames into the network and use the analyzer to observe the effects on other network equipment. You can also use one of these generator channels to create a constant, background traffic level on the LAN by using a channel's packet-size and inter-frame-spacing control settings.

Generators as software probes

Packet generators can do more than merely create traffic on the network: You can also use them to test software performance in a developing product. Suppose you are building a product similar to the DTE shown in **Fig 3,** and you have modularized your network-interface software to resemble the layers of the ISO model. If you install a switchable, loopback protocol in each software layer, you can use the protocol analyzer's packet generator to successively activate each loopback while using the analyzer's capture buffer to record the returned frames. The analyzer time-stamps each echoed packet, allowing you to determine the response time or pass-through delay of each software layer.

Simultaneously, you can employ other packet generators within the analyzer to check your software's response to illegal packets, examine the effect of varying levels of background traffic on software performance, and test the response to simultaneous requests from multiple (simulated) nodes.

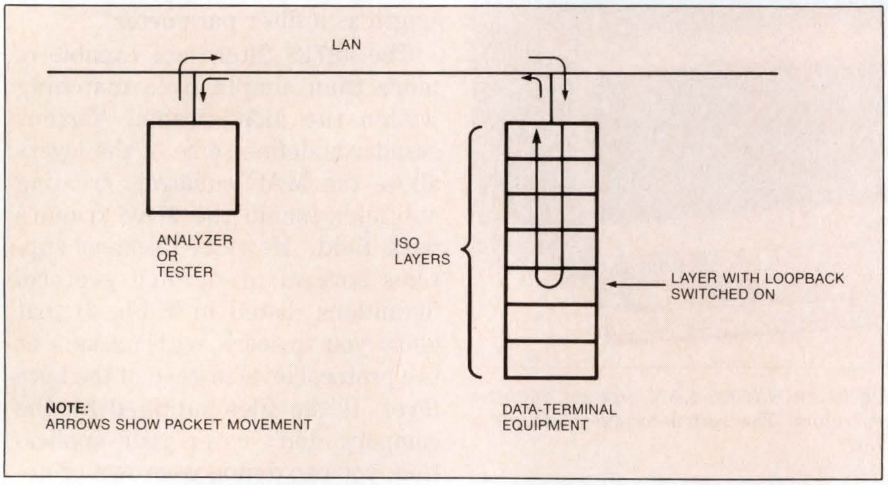


Fig 3—By using the loopback code in a DTE's software, *as well as a packet generator, capture buffer, and time stamp on each received packet, a LAN protocol analyzer can sequentially exercise each protocol layer and determine the pass-through delay it exhibits.*

Excelan offers its Lanalyzer protocol analyzer as a pc board and software package or as a complete system. The Lanalyzer pc board plugs into the IBM PC or PC/AT buses and has jumper settings for 8- or 16-bit data paths. The system version includes the pc board, software, and a Compaq Portable 286 computer.

The Lanalyzer includes eight filters and six packet generators. Each filter accepts multiple criteria for source and destination addresses, type-field value, and byte values within the packet's data field. The generators can transmit illegal packets containing FCS and preamble errors, send packets with inadequate interframe separation, and create collisions with frames transmitted by other network nodes.

Because of the Lanalyzer's complexity, Excelan offers a free demo disk that allows you to experiment with the product's user interface. The demo disk runs on an IBM PC or compatible computer and serves as an extended, interactive data sheet. If you are in the market for a LAN protocol analyzer, it's a good idea to spend an hour running the demo: It will give you a deeper understanding of the Lanalyzer in particular and of LAN protocol analysis in general. **EDN**

For more information . . .

For more information on the LAN testers and analyzers discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Cabletron Systems
Box 6257
Rochester, NH 03867
(603) 332-9400
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Circle No 710

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(805) 963-9471
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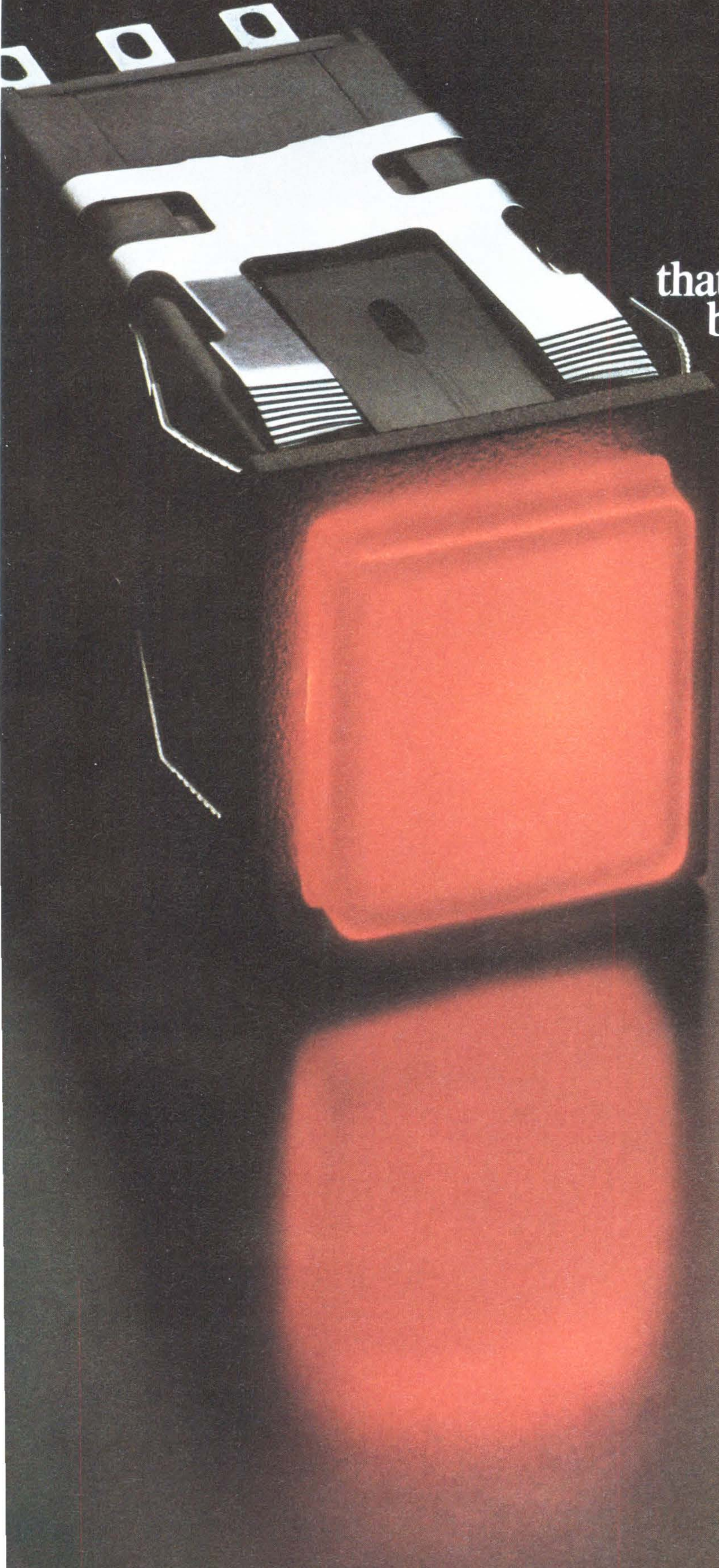

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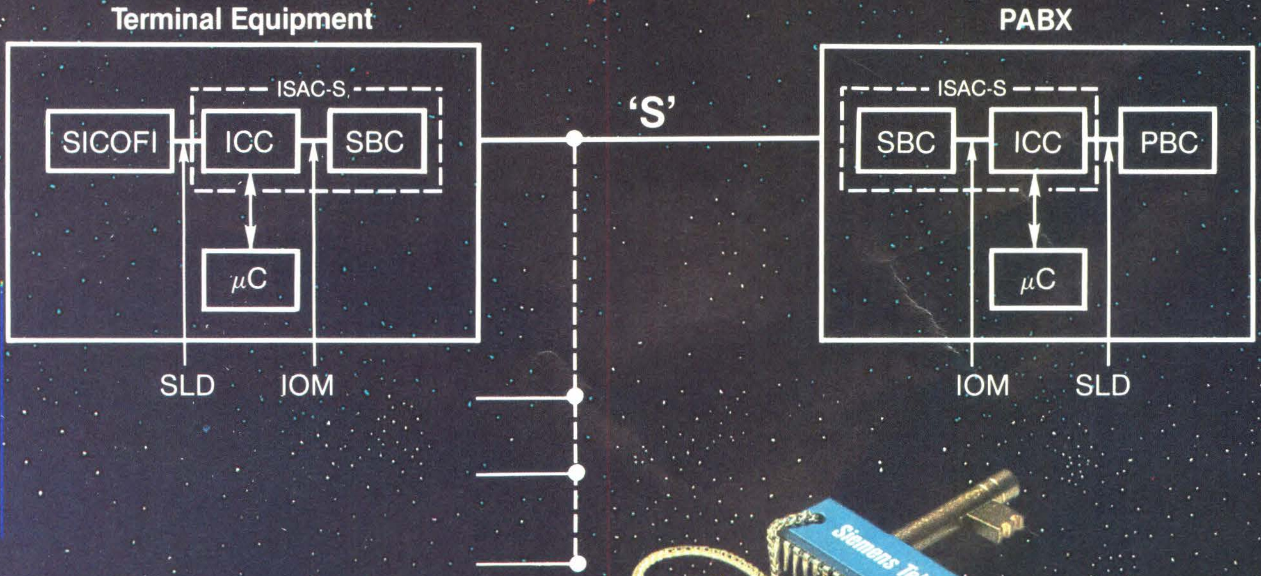

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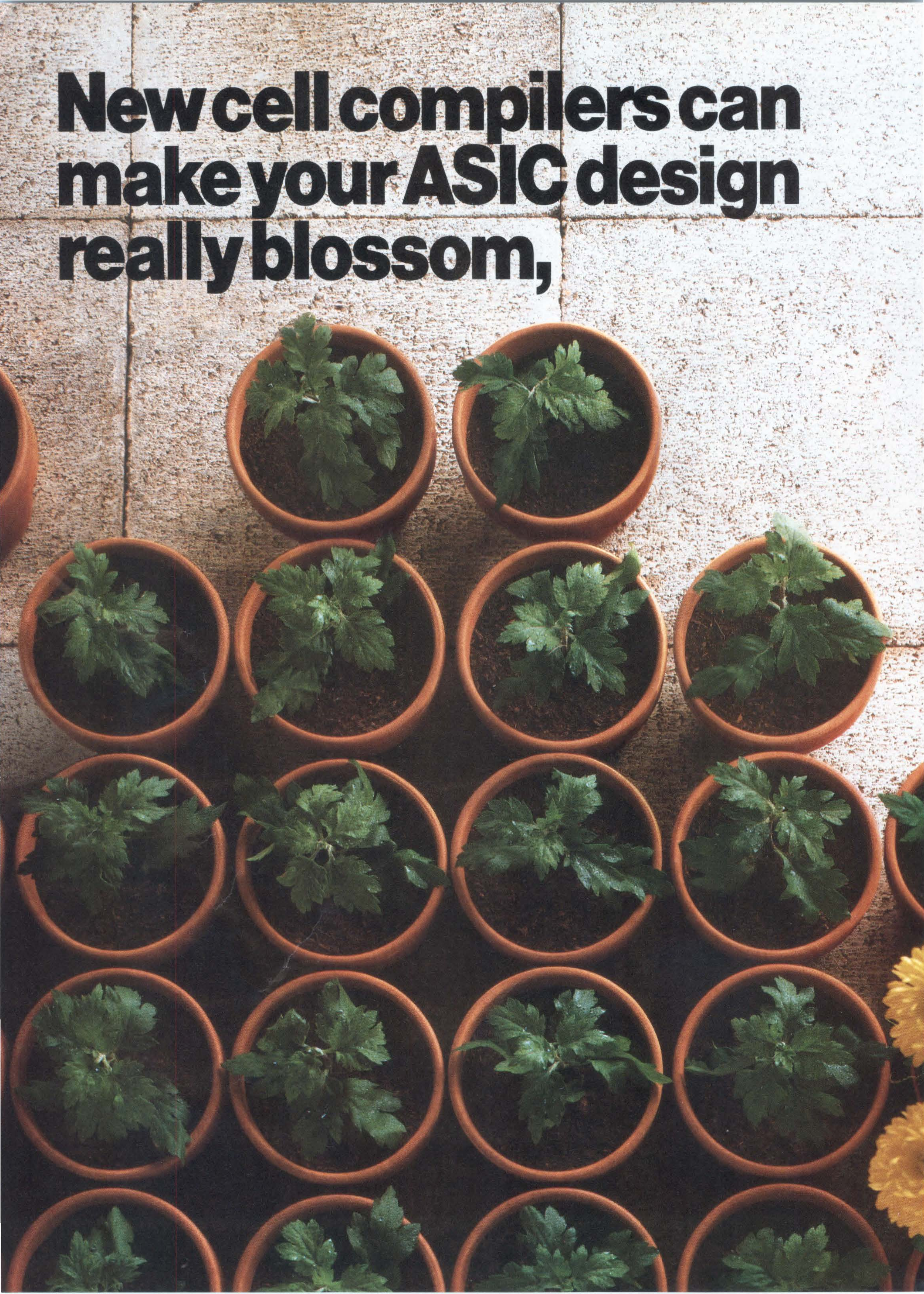
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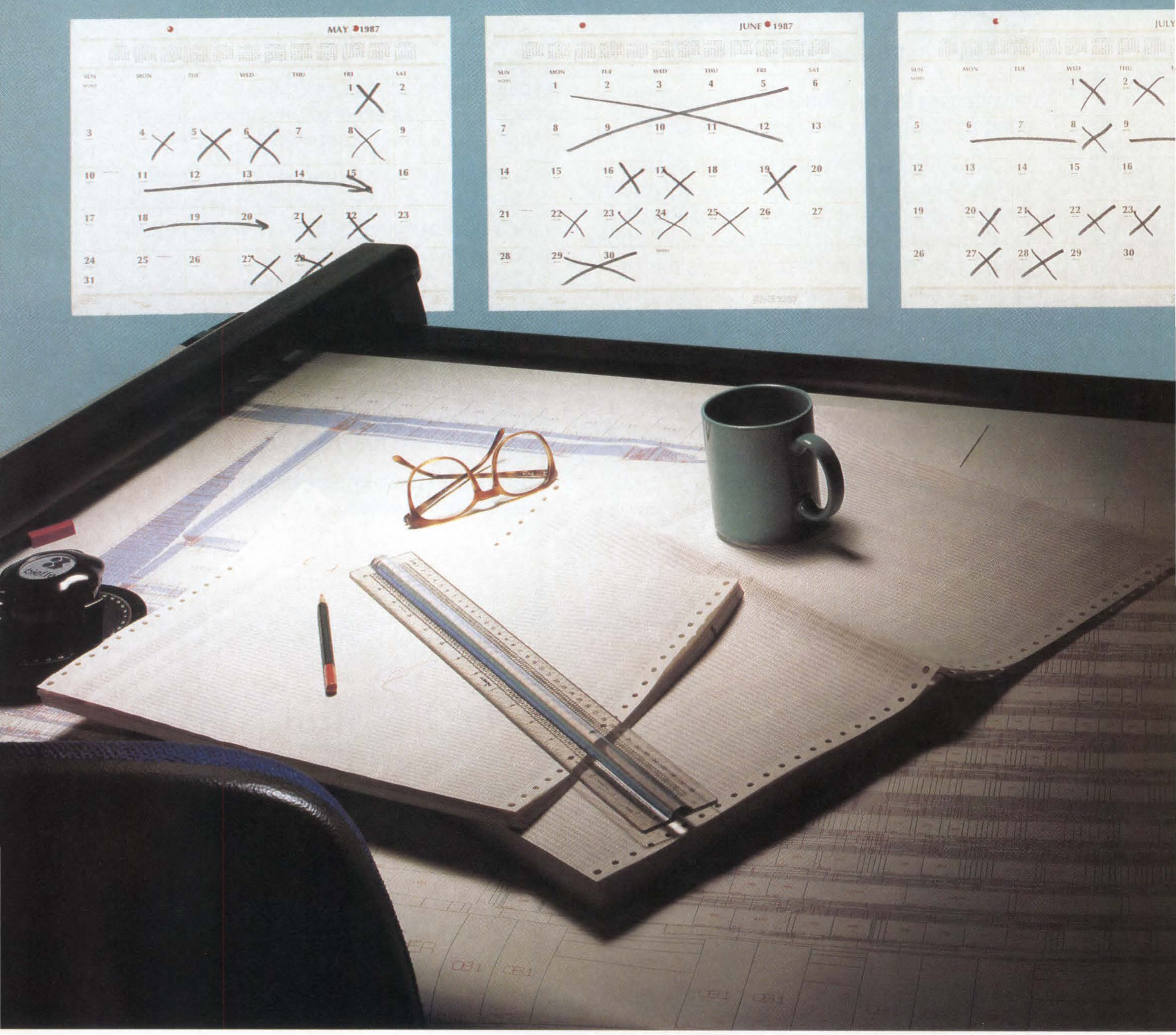

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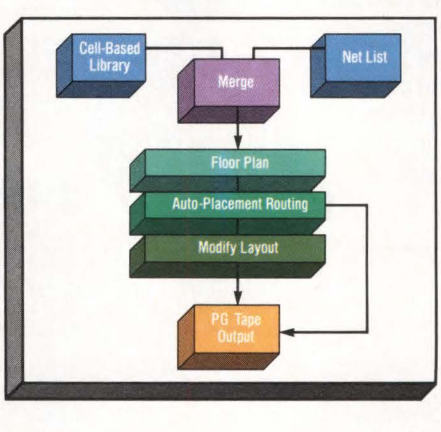

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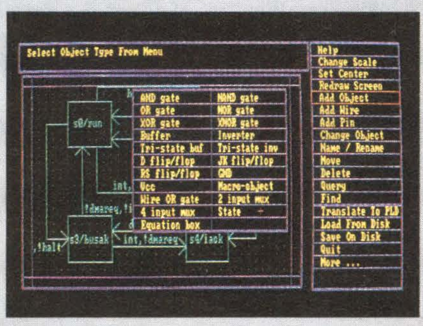

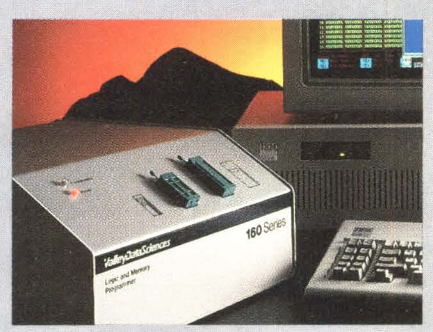

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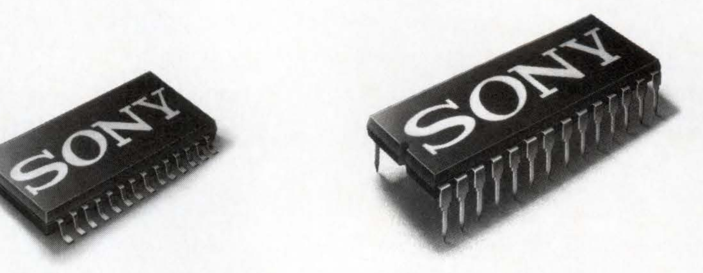
PART NUMBER	ORGANIZATION	SPEED (ns)	PACKAGE
CXK5814P—35L/45L/55L	2K x 8	35/45/55	300 mil DIP
CXK5816PN—10L/12L	2K x 8	100/120	600 mil DIP
CXK5816M—10L/12L	2K x 8	100/120	SOP*
CXK5416P—35L/45L/55L	4K x 4	35/45/55	300 mil DIP
CXK5864AP—70L/10L	8K x 8	70/100	600 mil DIP
CXK5864AM—70L/10L	8K x 8	70/100	SOP*
CXK5864PN—12L/15L	8K x 8	120/150	600 mil DIP
CXK5864M—12L/15L	8K x 8	120/150	SOP*
CXK5464P—45L/55L/70L	16K x 4	45/55/70	300 mil DIP

*Small Outline Package



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PART NUMBER	PROCESS	SPEED (ns)	PACKAGE	DATA RETENTION CURRENT (MAX)	DATA RETENTION CONDITION
CXK58256P—10L/12L	MIX MOS	100/120	600 mil DIP	50 μA	0 to 70°C
CXK58256MF—10L/12L	MIX MOS	100/120	SOP	50 μA	0 to 70°C
CXK58256P—10LL/12LL	MIX MOS	100/120	600 mil DIP	10 μA	0 to 70°C
CXK58255P—45/55/70	FULL CMOS	45/55/70	600 mil DIP	5 μA	−30 to 85°C
CXK58255P—45L/55L/70L	FULL CMOS	45/55/70	600 mil DIP	2.5 μA	−30 to 85°C

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Cost, device speed, size, and reliability determine the best package for an ASIC

Eva Freeman, *Associate Editor*

When you order an application-specific IC (ASIC) from a foundry, the foundry does everything but specify the design and select the chip package. Yet the latter is no idle task; choosing the best ASIC package requires some research on your part. The familiar, widely used plastic dual in-line package (DIP), for example—a package you might once have chosen without giving the matter much thought—slows signal transmission, requires considerable pc-board area, decreases reliability, and can even cost more than other ASIC packages.

The deficiencies of DIPs have led ASIC vendors to offer other packages: leaded and leadless chip carriers, pin-grid arrays (PGAs), small-outline packages, and flat packs. All foundries offer essentially the same set of packages. Choosing an ASIC foundry and selecting an ASIC package are, therefore, separate tasks.

Pin-grid arrays provide more leads *than any other package. VLSI Technology offers 84- to 149-pin packages in its plastic PGA product line; the company's ceramic PGAs are available in 68- to 224-pin versions.*

The package, not the vendor

ASICs are custom products, so foundries calculate the price of each ASIC order, including the packages, individually. Shopping for a vendor that delivers quality ASICs for a low price can hold down expenses, but the package you choose affects the total cost of an ASIC more than your choice of foundry.

The price of a particular package type varies little from foundry to foundry, but prices for different types of package cover a wide range. For example, a leadless ceramic chip carrier costs about eight times as much as a plastic leaded chip carrier (PLCC). Furthermore, you can often avoid using an expensive ASIC package simply by approaching the design of your chip with greater care and partitioning it into sections that will fit into distinct packages (see **box,** "Partition your design to reduce packaging costs").

Before you jump into a detailed evaluation of your ASIC and its packaging requirements, however, take a careful look once again at the plastic DIP. If you can use one, you should. Plastic DIPs are inexpensive (1¢ to 3¢ per lead), easy to insert into pc boards, and easy to solder. The 0.1-in. spacing between leads in a DIP leaves plenty of room for interconnections on a pc board.

Yet despite the convenience and low cost, plastic DIPs don't work in every application. You can't use a plastic DIP if you need high reliability, fast heat dissipation, a surface-mount design, a small package, or a low package profile.

When it comes to conserving pc-board surface area, small-outline packages are a good choice. These packages have an 0.05-in. pin spacing, a pitch that's half that of standard DIPs. Small-outline packages that have eight to 16 pins are 0.16 in. wide; small-outline packages with as many as 28 pins are 0.3 in. wide. DIPs are usually twice as wide as small-outline packages with the same number of pins.

You can use small-outline packages in surface-mount applications. The packages have gull-wing leads, which extend out from a package. The short leads of the small-outline package make it one of the most rugged packages.

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Small-outline packages can help you shrink the size of a pc board, but only if your chips have modest I/O requirements. The packages are available only in 8- to 28-pin versions. And for the many ASIC designs that require more than 40 pins, DIPs aren't the best solution, either. For a given increase in the number of pins, a DIP increases in size by an even greater percentage; a DIP with more than 40 pins is thus a very large package. A 48-pin DIP has a width of 0.6 in., so the package requires a board area of 1.4 in². The width of a 64-pin DIP is 0.9 in., which gives the package an area close to 3 in². As **Fig 1** shows, other packages require much less board area than large DIPs.

Besides using too much pc-board area, large DIPs have long internal interconnections. These intercon-

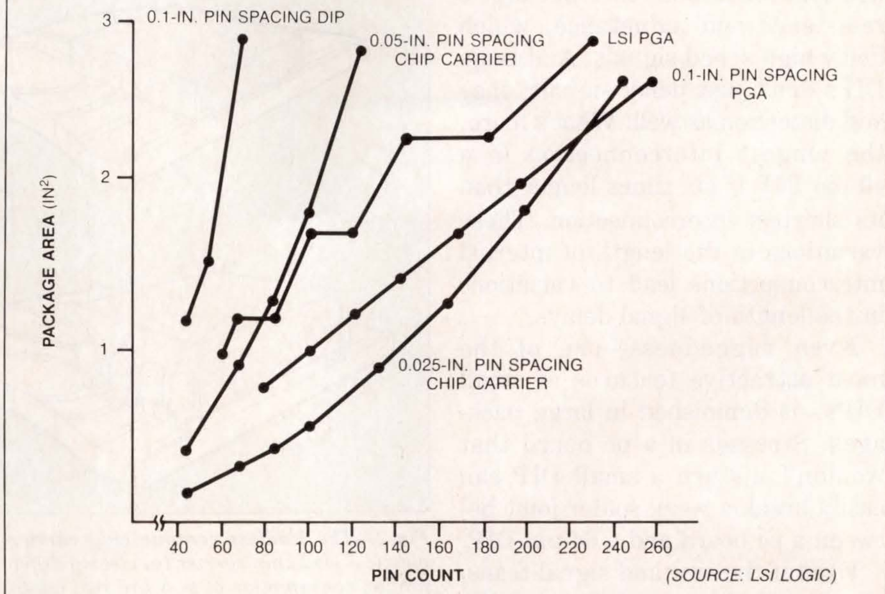


Fig 1—The size of a pc board depends largely *on the size of the chip packages. If you switch from a 64-pin DIP to a 68-pin leaded chip carrier, for example, you can reduce the size of your package by two-thirds.*

Partition your design to reduce packaging costs

When it comes time to package your ASIC design, don't be hamstrung by the idea that more packages mean higher cost. A 100-lead, plastic PGA, for example, costs more than two 68-pin PLCCs. Consequently, if you can partition your design to fit into two chip carriers, you'll spend less on packaging than if you use one PGA.

By partitioning a design that requires ceramic packaging, you can cut package costs considerably. Instead of placing the entire circuit into a ceramic package, look for sections that can function in a plastic package. If you move part of your design into a plastic package, you can choose a smaller, and therefore less expensive, ceramic package for the rest of the design.

To partition a design effectively, you must analyze all costs. A recent study of a 2300-gate, 125-pin gate array **(Ref 1)** showed that a single-package approach cost 2.3 times as much as a 2-package system. Partitioning the design reduced both the silicon costs and the package costs.

Don't take partitioning too far

You can, of course, partition a design beyond the point of utility. The use of three packages for the 2300-gate array resulted in a 14% cost increase over the 2-package approach. The 3-package configuration used less expensive packages and less expensive silicon dies than the 2-package implementation, but the sheer number of packages in the 3-package design outweighed the benefit of the smaller size of those packages.

To partition an ASIC circuit, you can use the same techniques that you use to partition a PLD circuit. For example, FutureNet's (Chatsworth, CA) Semicustom Development System software can divide a circuit into several PLDs or into several gate arrays **(Ref 2).** Using this logic-partitioning package, you can implement your design in various ways and find the most cost-effective solution.

An analysis of design costs is incomplete unless you assess the whole effect of partitioning a circuit. When you partition a chip, you increase the part count, which increases assembly costs. You also increase the amount of space you need on the pc board. The change in design may disrupt critical timing paths. Even so, if you can partition a large design, you can cut your ASIC costs in half.

References

1. Johnson, Dean P, and Jim Lipman, "IC packaging: An introduction for the VLSI designer," *VLSI Systems Design*, June 1986, pg 108.

2. Shear, David, "Tools help you retain the advantages of using breadboards in gate-array design," *EDN*, March 18, 1987, pg 81.

nections increase the package's resistance and inductance, which delay high-speed signals. And large DIPs don't just delay signals; they add distortion as well. What's more, the longest interconnection in a 40-pin DIP is six times longer than its shortest interconnection. These variations in the length of internal interconnections lead to variations in the length of signal delays.

Even ruggedness—one of the most attractive features of small DIPs—is diminished in large packages. Stresses in a pc board that wouldn't disturb a small DIP can easily break a weak solder joint between a pc board and a 64-pin DIP.

Even if the size and signal-transmission problems of large DIPs don't deter you, you still can't use a DIP for very large ASICs. The largest DIP that you can buy from an ASIC vendor is a 64-pin package.

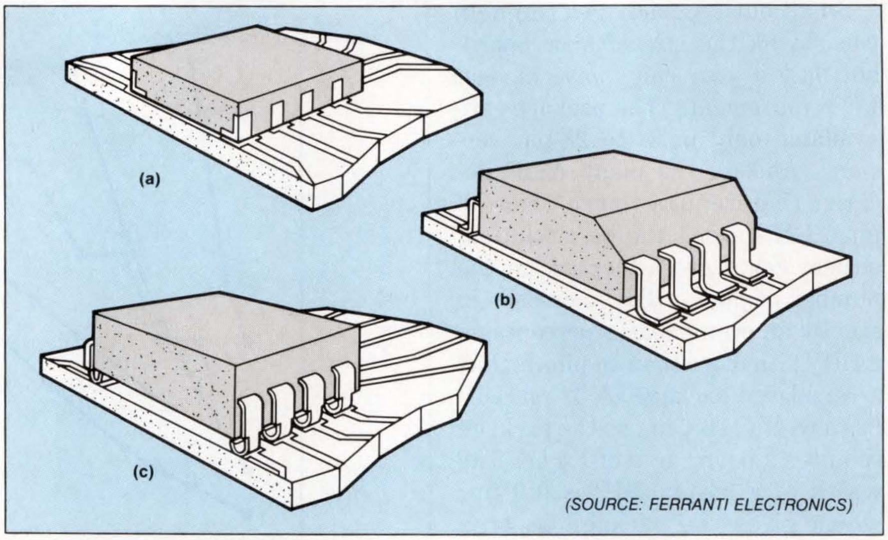


Fig 2—The leadless ceramic chip carrier (a), *small-outline gull-wing package* ***(b),*** *and plastic J-lead chip carrier* ***(c)*** *clearly differ in the degree to which they emphasize pc-board profile, consumption of pc-board real estate, and the ease with which you can inspect solder connections.*

Into chip-carrier range

Like most ASIC vendors, VLSI Technology (San Jose, CA) recommends that you use DIPs only for designs that have 40 or fewer pins. If your design requires 44 to 84 pins, the company advises that you use a chip carrier.

A chip carrier has conductors that extend from the die cavity to the periphery of the package. All chip carriers are surface-mount components. Chip carriers can be leaded or leadless.

In a leadless chip carrier, the conductors extend from the silicon die just to the edges of the package. The absence of long leads reduces the capacitance of the package, but also prevents you from inspecting solder connections to a pc board.

Because they lack metal leads, leadless chip carriers form a rigid connection with the pc board. Any incompatibility between the thermal-expansion coefficient of a package and the pc board that the package is mounted on can cause the package to separate from the board.

You can mount only the smallest size of leadless ceramic chip carrier on a conventional epoxy pc board. For larger leadless ceramic chip carriers, you must use a ceramic pc board. ASIC foundries don't offer plastic leadless chip carriers; no pc-board substrate matches the thermal-expansion characteristics of a plastic package.

The springiness of its metal leads gives a leaded chip carrier more compliance than a leadless chip carrier. Leaded chip carriers have leads shaped like the letter J, with the leads tucking under the package.

The J leads of leaded chip carriers and the gull-wing leads on small-outline packages have their respective advantages. On the one hand, J leads consume less board area than gull-wing leads. On the other hand, you can inspect solder connections on a gull-wing package easily, while the solder joints on a J-lead chip carrier are difficult to see. (**Fig 2**'s diagrams compare the appearance of leadless, J-lead, and gull-wing packages.)

Because J leads can flex with a pc board, you can mount a J-lead package on any type of pc board, including epoxy, ceramic, and polyimide pc boards. You can also mount these packages in sockets.

ASIC foundries offer leaded chip carriers both in ceramic and in plastic form. Each of these materials has its particular advantages (see **box,** "Ceramics vs plastics: Not an automatic choice").

A leaded chip carrier's leads don't need to be long, because the package needs to make contact only with the surface of the board. DIPs, which you must mount through a pc board, have longer leads than those of a leaded chip carrier. The latter's leads therefore add less capacitance than the pins of a DIP. A 48-pin DIP, for example, specs a capacitance of 2 pF; the capacitance of a 48-pin leaded chip carrier is 0.25 pF. Similarly, the capacitances of 64-pin DIPs and leaded chip carriers are 4 and 0.3 pF, respectively **(Ref 1).**

Leaded chip carriers don't solve every packaging problem. To solder a leaded chip carrier to a pc board, for example, you must ensure that the J leads are coplanar. If the leads aren't coplanar, the short leads won't contact the board.

Unlike leaded chip carriers, flat packs always form good contacts to pc boards. The leads in a flat pack extend straight out from the package, so you can make sure that all leads contact the pc board. Furthermore, you can see and repair any

Ceramics vs plastics: Not an automatic choice

Ceramic packages typically cost five to ten times as much as comparable plastic packages. You should therefore select plastic packages whenever possible (although many applications require the ceramic alternative). When it comes to encapsulating your prototypes, however, ceramic packages actually cost less than plastic ones, principally because it's easier to deliver small lots of parts encased in them.

For prototypes, the expense of the package is less important than fast turnaround time. An ASIC foundry can mount a prototype in a ceramic package manually and deliver it within a couple hours of your order. If you order a plastic package for your prototype, the foundry must set up an assembly line and then run the prototype through it—a procedure that can take several weeks. You should therefore choose ceramic packages for your prototypes even if you use plastic packages for your production models.

Ceramic packages are more reliable than plastic packages. VLSI Technology's package-engineering manager, Dean Johnson, notes that, although reliability is always important, it's less critical for production devices than for prototypes; you're checking the latter for design flaws, not production-type defects. "If you aren't sure that you have designed your prototype correctly," says Johnson, "you shouldn't have to worry about problems with the molding compound or molding temperature. The leads in ceramic packages also improve device reliability. Ceramic packages have gold-plated leads; plastic packages have tin- or solder-plated pins."

Ceramics satisfy reliability specs

Once you approve your prototype and start your production runs, you may switch to a plastic package. Even for production quantities, though, many applications require ceramic cases. Two characteristics of ceramics are superior to plastics: heat dissipation and chemical stability. The faster heat dissipation of ceramics enhances the reliability of ceramic ASIC packages. The chemical stability lets you use ceramics in contamination-sensitive applications.

Military contracts usually require ceramic packages. The government requires not only that ASICs operate in the −55 to +125°C temperature range, but also that they tolerate multiple cycles of temperature. Naturally, a package that specs a low thermal resistance can survive temperature cycles better than one that has a high thermal resistance.

TABLE A—TYPICAL THERMAL RESISTANCES

PACKAGE TYPE	θ_{JC} (°C/W)	θ_{JA} STILL AIR (°C/W)	θ_{JA} 300 FT/MIN (°C/W)
16-LEAD DIP–CERAMIC	28	95	
–PLASTIC		150	
24-LEAD DIP–CERAMIC	16	45 TO 60	30 TO 40
–PLASTIC	50	110 TO 130	
40-LEAD DIP–CERAMIC		45 TO 50	25 TO 30
–PLASTIC	45	110 TO 125	
68-LEAD CHIP CARRIER	5	50	35
WITH HEAT SINK			10 TO 20
68-LEAD CHIP CARRIER –CERAMIC			
IN SOCKET		40	30
WITH HEAT SINK/SOCKET		25 TO 30	10 TO 25
68-LEAD CHIP CARRIER –PLASTIC			
IN SOCKET		45	
SURFACE MOUNT		43	
PIN GRID (CAVITY UP)			
CERAMIC 64 TO 100 PINS (10×10 GRID)		30 TO 35	20 TO 23
PLASTIC		30 TO 35	20 TO 25

NOTE: DIE SIZE IS 200 MIL² UNLESS LIMITED BY CAVITY SIZE.

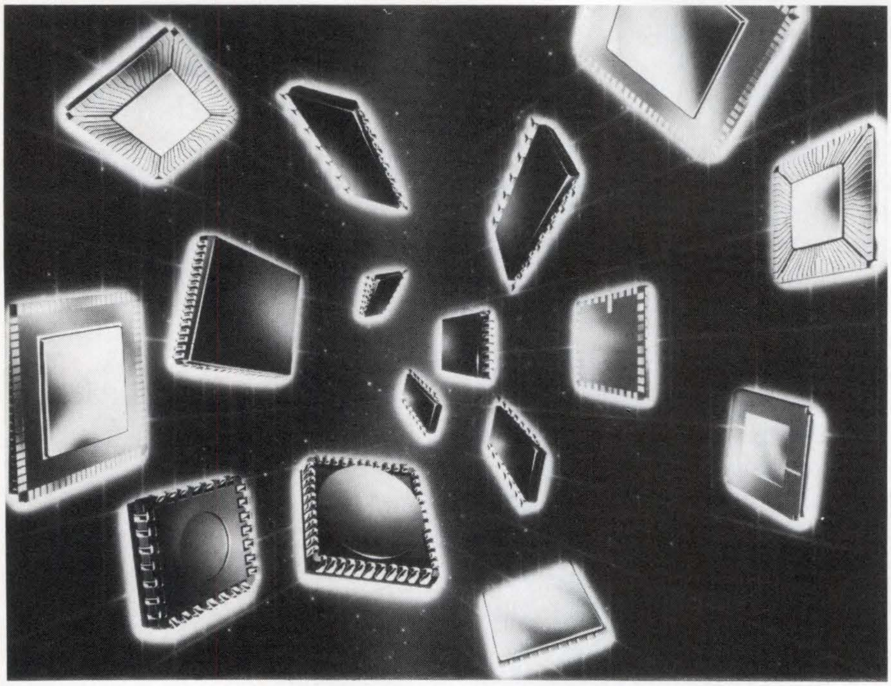
LSI Logic has taken measurements that show, for a 24-pin DIP, that the thermal resistance between the encapsulated device and its plastic case is 50°C/W **(Table A).** For a ceramic DIP, the thermal resistance is 16°C/W—an improvement in thermal resistance by more than a factor of three.

Chemical stability for many environments

The figures for the thermal resistance between an encapsulated IC and still air aren't quite as impressive as the figures for device-case thermal resistance. Still, the thermal resistance between a device inside a plastic DIP and still air is twice that of a ceramic DIP in the same environment.

Most nonmilitary ASIC applications don't have such stringent thermal specifications. But the chemical stability of ceramics is vital for systems that can't tolerate contaminants. Indeed, chemical stability is the reason why Gary Kelson, chief technical officer of Silicon Systems (Tustin, CA), recommends ceramics to many of his customers.

"We have customers who build hard-disk drives," he says. "Plastic packages emit organic vapors and shed flakes. Any residue is fatal to the operation of a hard-disk drive. Fortunately, ceramic packages are stable enough even for hard-disk drives."



***The constellation of packages for surface-mount ASICs** includes leaded and leadless chip carriers, flat packs, and small-outline packages. Most ASIC vendors offer all of these packages. (Photo courtesy Ferranti Electronics)*

broken connections. You must handle the leads with care, however; they break easily.

Flat packs are ideal for low-profile pc boards. They spec a 2-mm thickness, which makes them the thinnest of all chip packages. Yet even though they're so thin, they aren't the most compact way you can package an ASIC. For products that must fit into very small areas, you should use chip-on-board technology and forgo the package entirely.

The chip-on-board approach eliminates all problems traceable to the size and cost of packages because it eliminates the package itself. This approach is the least expensive packaging alternative. Instead of mounting your ASICs in packages, you simply use bare chips. To build a chip-on-board circuit, you bond ASICs to the metal traces on a pc board. You then cover the chips with epoxy, which holds the chip in place.

You can't replace an IC or repair a contact in a chip-on-board circuit, because you can't remove the epoxy. As a consequence, most chip-on-board circuits are in inexpensive consumer products, which contain throwaway pc boards. Typical of the applications of chip-on-board technology are watches and calculators.

The chip-on-board approach is not really viable unless you have an automated pc-board assembly system. Robots can attach a chip to a pc board with the consistency you'll need to ensure a high yield of parts with good contacts. You'll often find that the cost savings of chip-on-board circuits offset the expense of automated assembly.

PGAs for high pin count

You can't choose your packaging technology if your ASIC's pin count reaches three digits; you must use PGAs. The highest pin count for a chip carrier, for example, is 84 pins. Other package types provide even lower maximum pin counts. A 68- or 84-pin PGA costs about twice as much as a chip carrier with the same pin count, but if your design requires more than 84 pins, and you can't feasibly partition it, you must bear the added cost.

A PGA's pin count has essentially no limit. These packages contain tiny pc boards and one chip. Unlike all other packages, which have leads along their perimeters, a PGA has leads in rows under itself. Standard PGAs have as many as 224 leads. Custom PGAs can have close to 1000 pins. You can choose either plastic or ceramic PGAs. The ceramic versions cost about three times as much as plastic ones.

Right now, you can't mount a PGA on the surface of a pc board. The leads are long pins, which you must mount in holes in the pc board. Conceivably, however, by bending a PGA's pin, you can turn the pin into a J lead. Chip vendors are currently developing a J-lead PGA, which would mount on a pc-board surface. You may expect to see such packages by the end of the year.

Along with surface-mount PGAs, semiconductor manufacturers are developing inexpensive chip-bonding techniques and packages for high-speed devices. No new package will be as ubiquitous as the DIP, but the choice of packages should become broad enough to let you meet all system requirements. **EDN**

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1. Booth, Willard, *VLSI-Era IC Packaging*, Electronic Trend Publications, Saratoga, CA 1987. $1500.

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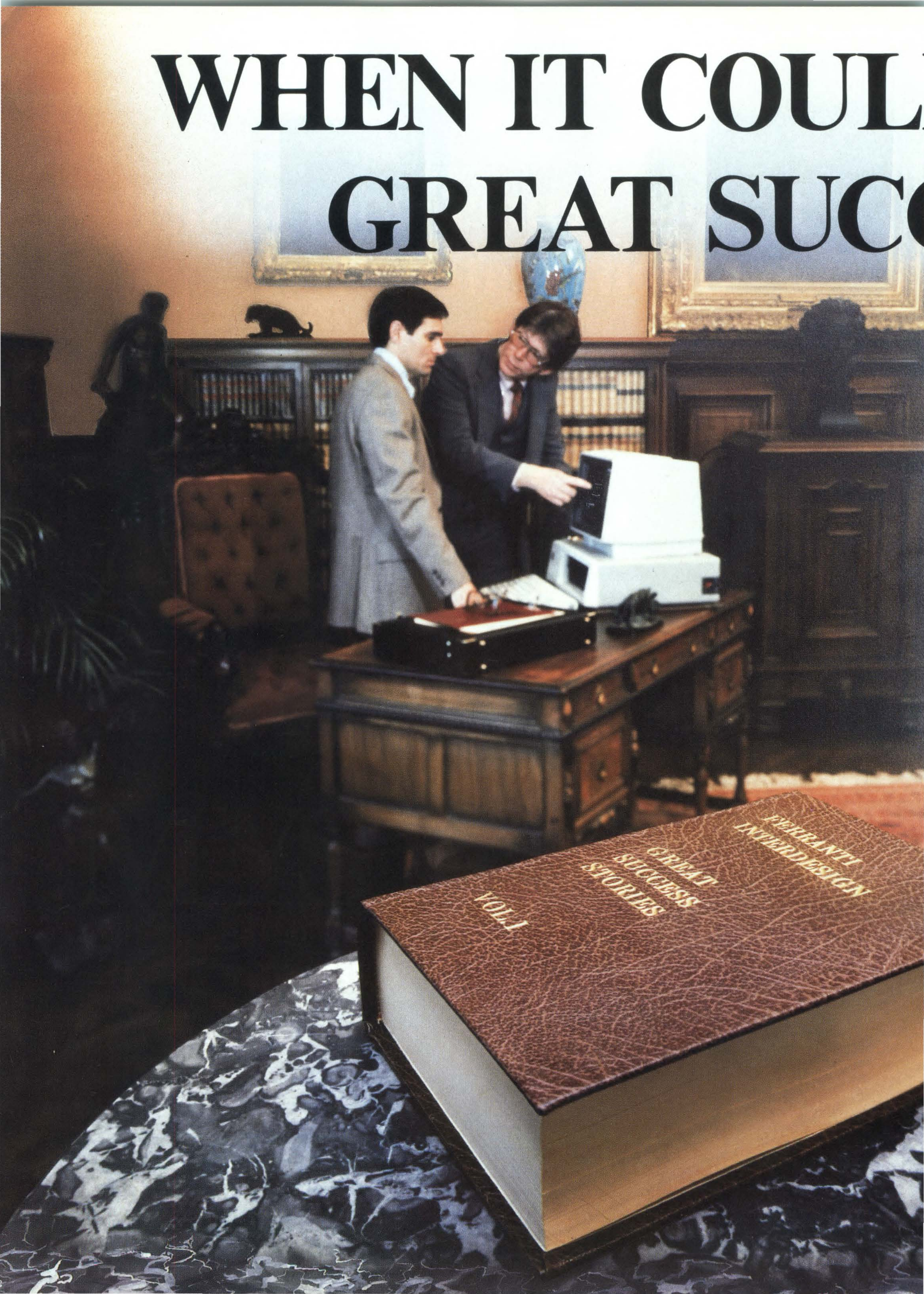
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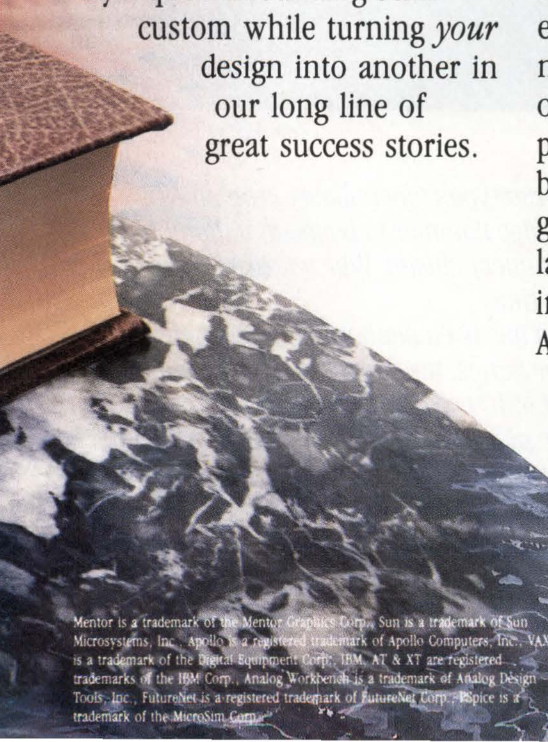

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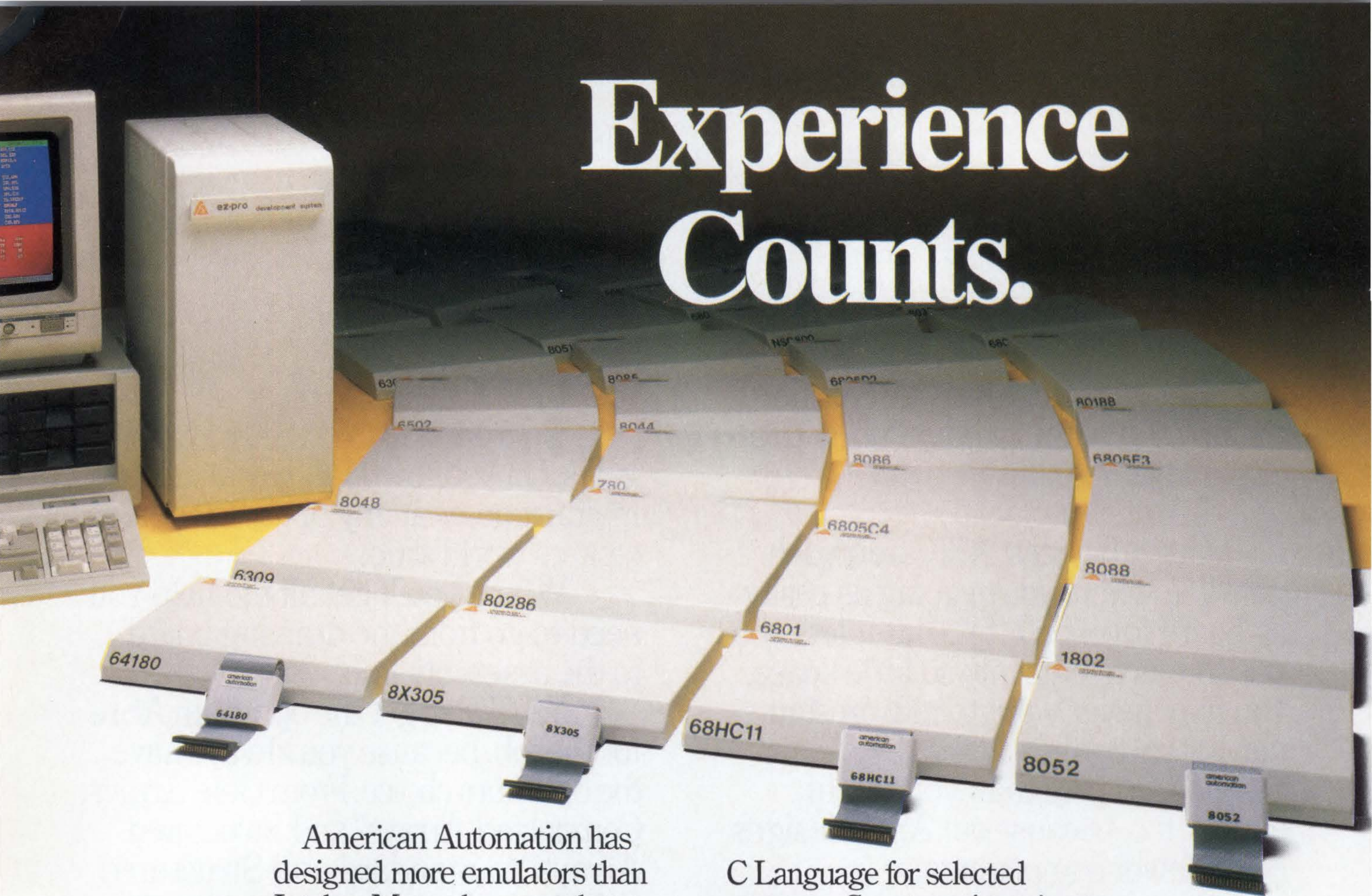

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CIRCLE NO 62

Ubiquitous conductive-rubber switches adapt to fit your application and budget

Margery S Conner,
Regional Editor

Versatile and inexpensive, conductive-rubber switches are one of the most commonly used switch types: Their applications range from VCR control panels to military electronics. To specify the switch you need, you'll have to determine four parameters: tactile response, stroke length, contact resistance, and actuation force.

This rubber-dome keyboard, from *Planar Products Div of IEE, uses hard-plastic key-caps to approximate the look and feel of a traditional typewriter keyboard.*

Two kinds of conductive-rubber switches are available: all-conducting and rubber-domed. The rubber-domed types are sold as part of an integrated custom keypad or keyboard, whereas the all-conducting types are sold as individual switches, which you then configure to your particular application.

Solution for a tight fit

Each all-conducting switch consists of an individual unit resembling a tiny hockey puck; the contact point protrudes from the bottom **(Fig 1).** All-conducting switches have the virtue of fitting in very small spaces such as car-radio control panels. Some, for instance, take up less than ⅛ in². Unfortunately, because the entire switch (including the bending area) consists of stress-sensitive carbon-impregnated silicone, its life expectancy is much shorter than a rubber-domed switch —only about 100,000 cycles.

A rubber-domed switch has a life expectancy of typically 25M cycles. It consists of a dome molded into an elastomer such as silicone; on the inside of the dome is a small pad of carbon-impregnated rubber with a typical resistance of 150Ω **(Fig 2a).** The contacts for the switch are separate interlaced traces on the keypad's pc board. The molded-rubber keypad fits over the pc board; when you depress the dome it collapses, shorting the conducting rubber pad between the two contact traces. Note that keypads made of rubber-domed switches are inherently sealed; you can spill a cup of coffee on one with no ill effects. The silicone operates with no degradation over a range of −40 to +120°C.

Rubber-domed switches have some drawbacks, however. The contact is momentary, so you have to supply any needed latching circuitry. Further, because of their 150Ω contact resistance, these switches can't handle much power.

Selecting a dome shape

A typical rubber-domed switch will probably cost about $0.07 apiece. This figure covers only the cost of the conductive elastomer and varies tremendously according to different specifications such as the switch's size and shape, the geometry of the dome walls, and the number of colors in the switch keypad. You'll also have to add the price of the pc board and the plastic housing.

If you decide that a rubber-domed conductive switch best suits the requirements of your application, you'll need to generate a drawing of the individual switch dome as well as the overall keypad layout. The dome shape determines the switch's tactile response and actuation force.

To ascertain which dome shape has the tactile response that you need, refer to the force-vs-stroke curves in **Fig 3.** The curves for the cone and bell shapes show a single bump, which indicates two very different types of click. Because of the cone's steeper sides, the collapse is abrupt, giving a sharp click response. The bell's more rounded

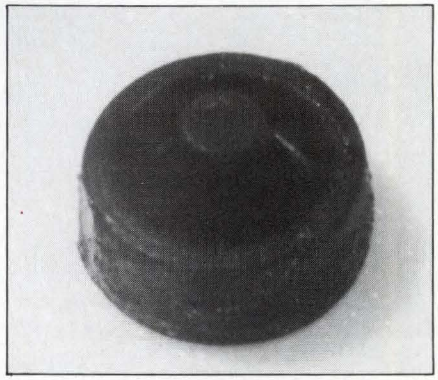

Fig 1—This all-conducting switch *from Digitran measures about ³⁄₁₆ of an inch in diameter. The switch fits nose down over the center contact just visible in the lower left-hand corner; a switch plate and keycap hold it in place. The switch's long nose keeps the outer wall of the switch from touching the contact encircling the center contact unless you depress the switch.*

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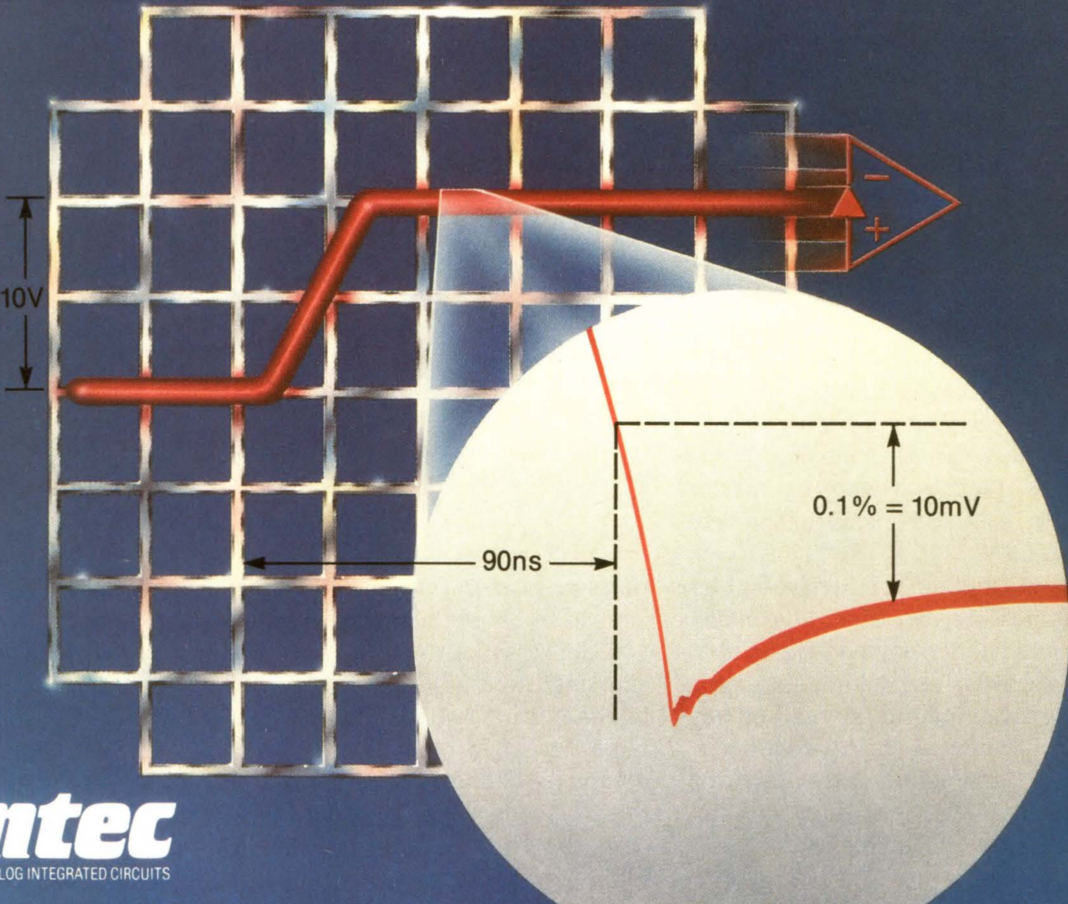

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sides impart a softer click response.

The secondary bumps on the double-cone and double-bell shapes indicate that these are keys with overtravel. Keys of this type have the spongier feel of the popular IBM typewriter keyboard. They do, however, require a separate keycap of hard plastic **(Fig 2b)**. The dome has a flattened top surrounded by a thin ring of rubber. This ring supports the conducting rubber pad as if it were on a tiny trampoline; after you depress the plastic keycap, you can continue to press the switch past the contact point until the ring bottoms out on the board. Overtravel also increases the reliability of a switch's actuation-force contact because you can continue to push past the initial point of contact.

Keycaps have advantages other than overtravel: You can customize a switchpad by substituting caps with application-specific legends, or you can dress one up with metallic keycaps. Remember that you have to add the price of the keycap (about $0.03 each in quantities of 50,000) to the total keypad price.

A key's stroke is the distance that a key travels before bottoming out on the underlying pc board, and it varies with the switch application. A typewriter keyboard stroke will range from 0.125 to 0.150 in.; a telephone-type keypad will range from 0.060 to 0.080 in.; and a calculator-type keypad will range from 0.030 to 0.040 in.

Some advice to follow

Harry Stern, vice president of engineering for Conductive Rubber Technologies, cautions against using an all-rubber switch in a long-stroke keyboard and recommends that you use keycaps if your application requires a long stroke. A long-stroke all-rubber key's top will tend to wobble as it slides down the key plate.

If you need a switch with a high degree of click, you may need to replace the carbon-filled conducting pad on the rubber dome with a snap dome—a metal disk that mounts over the contacts. When you depress the rubber dome, you snap the metal disk down to make momentary contact. A disadvantage is that the metal disk is abrasive to the pc-board contacts.

If you require a switch with very low contact resistance, you can specify a silver-filled pad in place of the carbon-filled one; the silver-filled pad has a resistance of about 1Ω. Be aware that the price of a switch with a silver-filled pad is about $0.16—or approximately twice that of one with a carbon-filled pad.

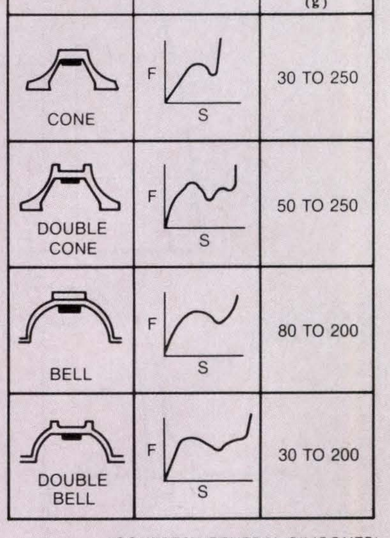
You must judge your need for high actuation force and sharp tactile feel vs a switch's life expectancy: A higher actuation force and a sharp tactile response result in a shorter switch life. In many military applications, the ability to withstand heavy environmental forces is a prerequisite. The steeper sides of cone-shaped domes support higher actuation forces as well as sharper tactile feel. However, their sides must flex more, which leads to a decrease in switch life. An average bell-shaped switch has a life of about 25M cycles; stiffer sides decrease the life by about 10%.

EPDM permits longer life

Substituting ethylene-prophylene diene methylene (mercifully shortened to EPDM) for the silicone elastomer can increase switch life to over 50M cycles without sacrificing any specs. EPDM is much more difficult for manufacturers to work with, however: They can't hold the molding process to a close tolerance. As a result, you can't use EPDM for switches with keycap sizes of less than 0.0625 in^2.

In addition, an EPDM switch's actuation force doesn't remain constant over time. Moreover, if you want backlighting, you can't use

RUBBER-DOMED SWITCH SHAPES



DOME SHAPE	ACTUATION FORCE vs STROKE	TYPICAL FORCE RANGE (g)
CONE	F / S	30 TO 250
DOUBLE CONE	F / S	50 TO 250
BELL	F / S	80 TO 200
DOUBLE BELL	F / S	30 TO 200

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Fig 3—A cone-shaped-dome switch's tactile response *is a sharper click than that of a bell-shaped switch. You can see the sharper tactile response in the force-vs-stroke curve. The steeper the slope of the curve after the contact point, the sharper the click. The steeper-sided cone-shaped domes sustain greater actuation forces.*

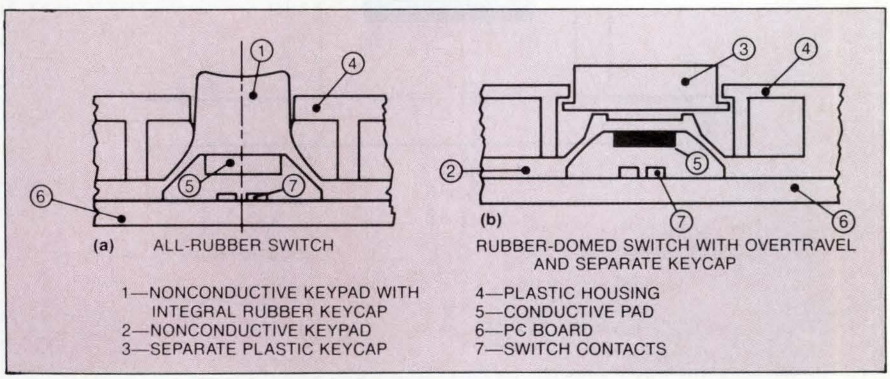

Fig 2—The most common form of conductive-rubber switch *is the rubber-domed type, which consists of a molded elastomer keypad, a plastic keypad housing, and a pc board. Usually you'll find it cheaper to meld the keycap with the keypad **(a)**, but if you need switch overtravel you'll have to use a separate plastic keycap **(b)**.*

EPDM because it's opaque. Before using this synthetic rubber, you should make sure that you really need the longer switch life.

IEE, on the other hand, has increased the life of its FTMK (full-travel military keyboard) switch by applying silicone in an unconventional way. Each keystation (**Fig 4**) in the keyboard is a separate mechanical unit, but, just like in a molded-keypad sheet, the silicone provides both the spring action and the conductive path between the two switch contacts. FTMK switches have a life expectancy that exceeds 50M cycles. Actually, IEE chose to stop the test at 50M cycles; the switch could very well last a lot longer. A 60-keystation MIL-STD-1280 (class 1, type 1) keyboard costs \$1200 (100).

Once you've decided on all four parameters needed to design the switch tooling and compiled a drawing, it's time to contact a molded-rubber manufacturer. Your prototype tooling will probably be a single-cavity mold. Marketing manager for General Silicones, Homer Bastug, estimates that a single-cavity mold (including 25 prototype pieces) for a 12-key telephone dome-type keypad will cost between \$1800 and \$2000.

Tooling for a 6-cavity mold will run between \$2500 and \$3000; the keypads themselves cost about an extra \$0.35 (50,000). Don't forget that dome-type keypads require plastic keycaps at an additional charge. All-rubber keypads will have a higher price both in tooling (\$2300 to \$2500 for the single-cavity mold, \$4000 to \$4500 for the 6-cavity mold) and in production quantities (\$0.65 to \$0.70 each), but you won't have to pay for separate keycaps and assembly costs.

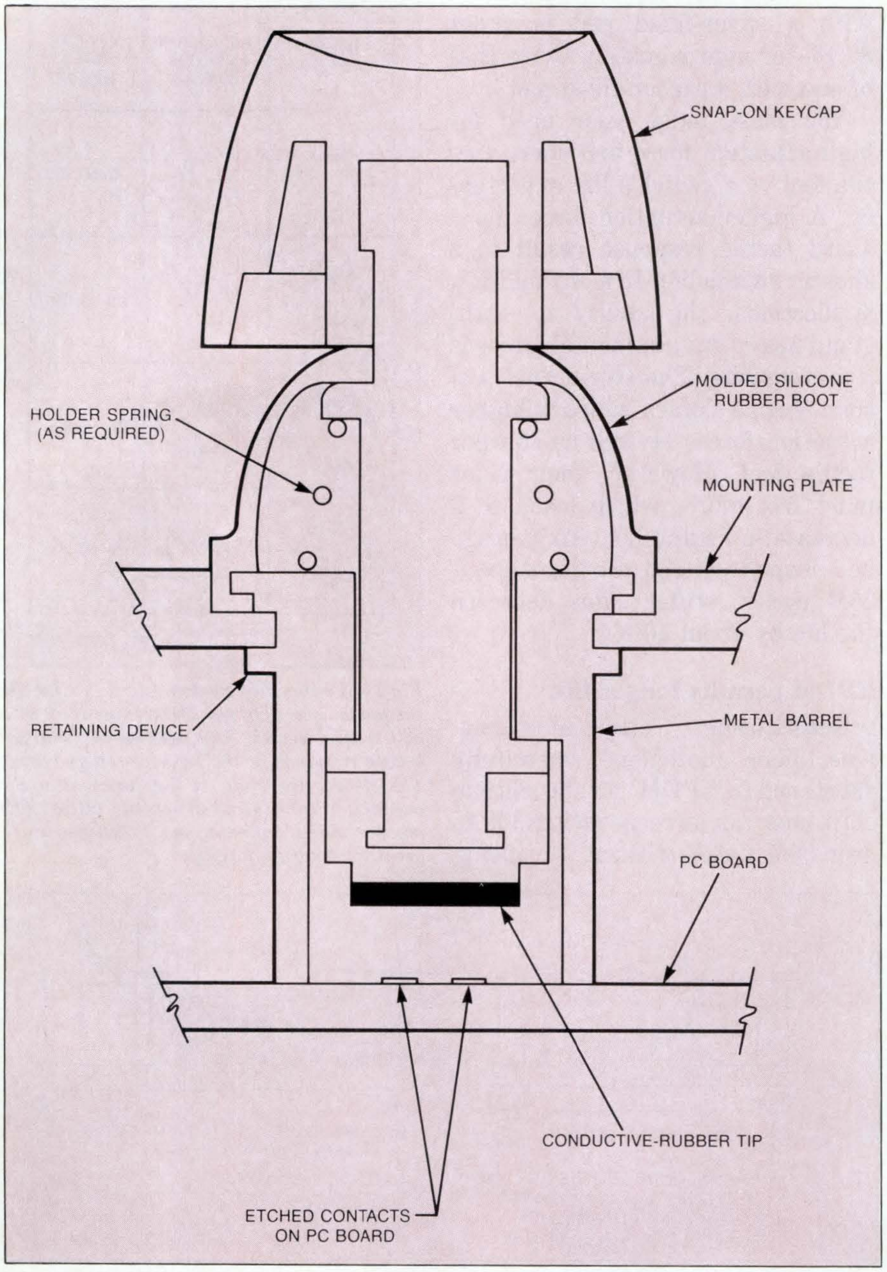

***Fig 4—The FTMK switch is a modular single keystation** that supports actuation forces as low as 90g. Its molded silicone rubber boot/spring can withstand submersion in three feet of liquid; the metal barrel provides EMI/RFI and Tempest shielding. (Courtesy Planar Products Div, IEE)*

Recommendations for prototype

Bastug suggests that you check the quality of the prototype tooling by holding the first-article keypad up to the light: Look for an even lighting of the domed-switch sides. Any dark spots indicate irregularities in the mold. Similarly, look for a smooth, even surface on the flat rubber surrounding the switches. And check that the air bleed paths are in-line and even. Finally, verify that the actuation force meets the specifications: A quality mold should be able to hold its switch force to ±10% of the spec. Aside from the obvious plus that quality tooling forms a quality rubber part, higher quality tooling lasts longer.

You have a choice of dealing with the molded-rubber manufacturer yourself or going through a distributor. Moxness Products and EECO have their manufacturing facilities in the US. Conductive Rubber Technologies, IEE, and Digitran each work with a number of molding companies and are also able to supply complete switch assemblies. Kokoku and Shin-etsu are US sales

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Dave Cray, director of engineering at Moxness Products, believes that keeping the manufacturing facilities in this country has allowed Moxness to be more responsive to any unforeseen tooling design changes. He concedes that Taiwanese manufacturing plants can offer lower prices, but he argues that these are offset by the communications barrier. In addition, he notes that some military contracts stipulate all components be US made.

Another option is to deal directly with the overseas manufacturer. The majority of conductive-rubber switch molding houses are in Taiwan; you can get a list of them from United Pacific International Inc, publishers of the magazine *Taiwan Electronics Industry Components* (Box 81-417, Taipei, Taiwan, ROC, TLX 28784 UNIPAINC).

Be aware, however, that if you opt for direct correspondence with a foreign company, you must know exactly what you need in tooling design; the foreign manufacturer will not be able to offer guidance. Further, even if you have complete switch drawings and specifications, you'll find it hard to communicate about quality concerns, and the language barrier will inevitably cause misunderstandings. The first time you design with conductive-rubber switches, you should consider going through a manufacturer with a sales office or broker in the US. **EDN**

Conductive-rubber switches serve as transducers

Although you may choose to design with conductive-rubber switches because of their usefulness as on/off actuators, you can easily adapt them to applications requiring speed- and direction-sensing transducers.

To configure such a switch as a speed-sensing transducer, Harry Stern, vice-president of engineering for Conductive Rubber Technologies, suggests using a bell-shaped switch and molding a conducting ring close to the base of the dome. You'll need two sets of contact traces on the pc board; the first set will be shorted together by the conducting pad at the dome's top; the second will be shorted by the ring at the dome's base. Timing circuitry derives the switch's depression speed by measuring the time that elapses between the two contacts.

To use conductive-rubber switches as direction sensors, mold a pivot point into the bottom of a broad, flat switch top. For example, in the simplest case of a left/right or up/down sensor, the switch will have two conductive-rubber pads with corresponding contacts on the pc board. Depending on the side you press on, the switch will make contact with the pc-board traces on that side. You can expand this design to include a multiple number of contacts and pads to achieve a crude joystick.

In addition, a rubber-domed switch can also function as a pressure transducer if you mold the conducting pad into a convex instead of a flat surface. This configuration requires that one broad contact trace encircle the other. As you press harder on the switch, more of the pad makes contact with the outer surface and contact resistance decreases. You can create a transducer that discerns discrete levels of pressure by ringing the initial contact trace with concentric partial circles connected to separate traces.

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For more information . . .

For more information on the conductive-rubber switches discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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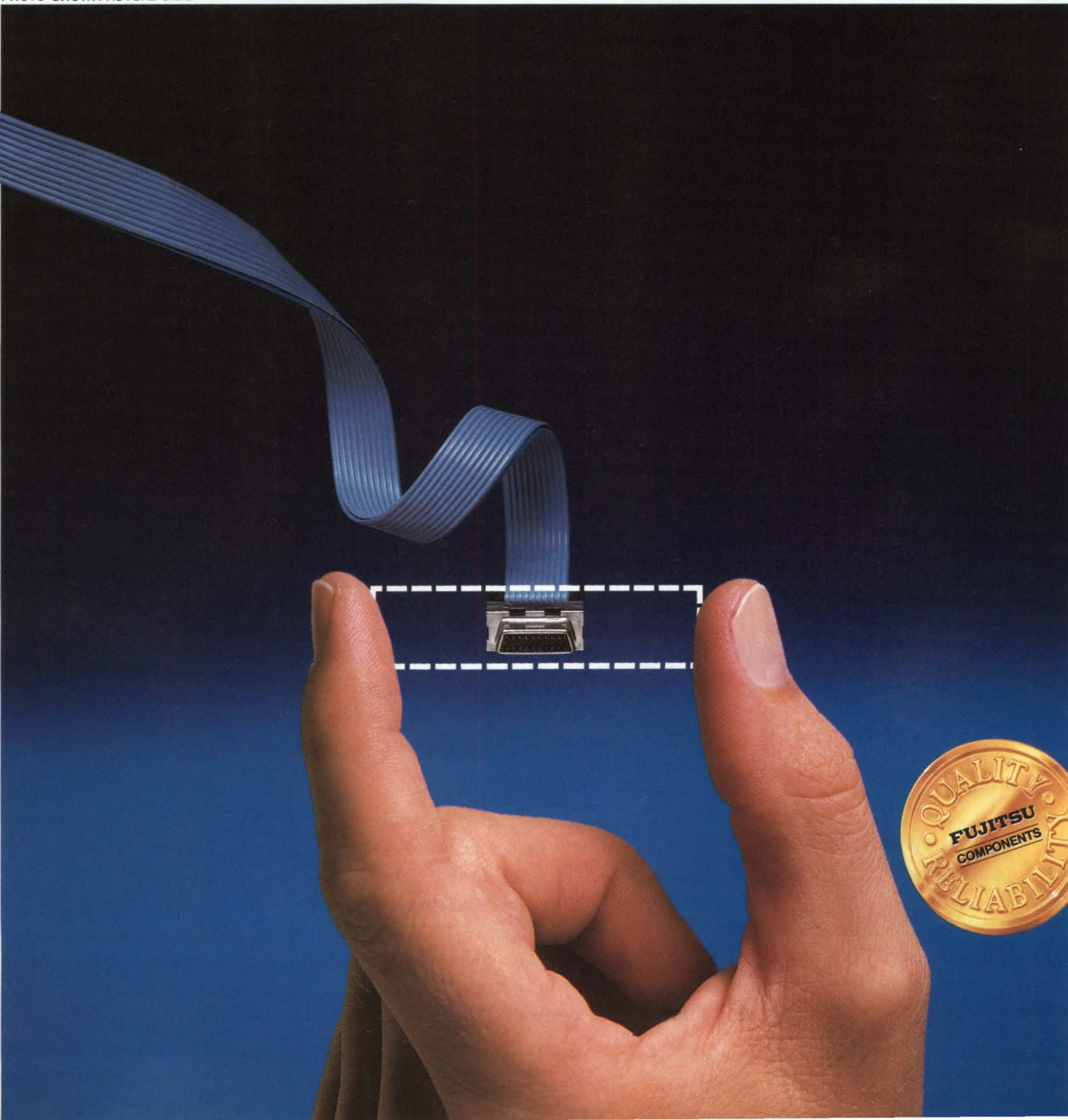

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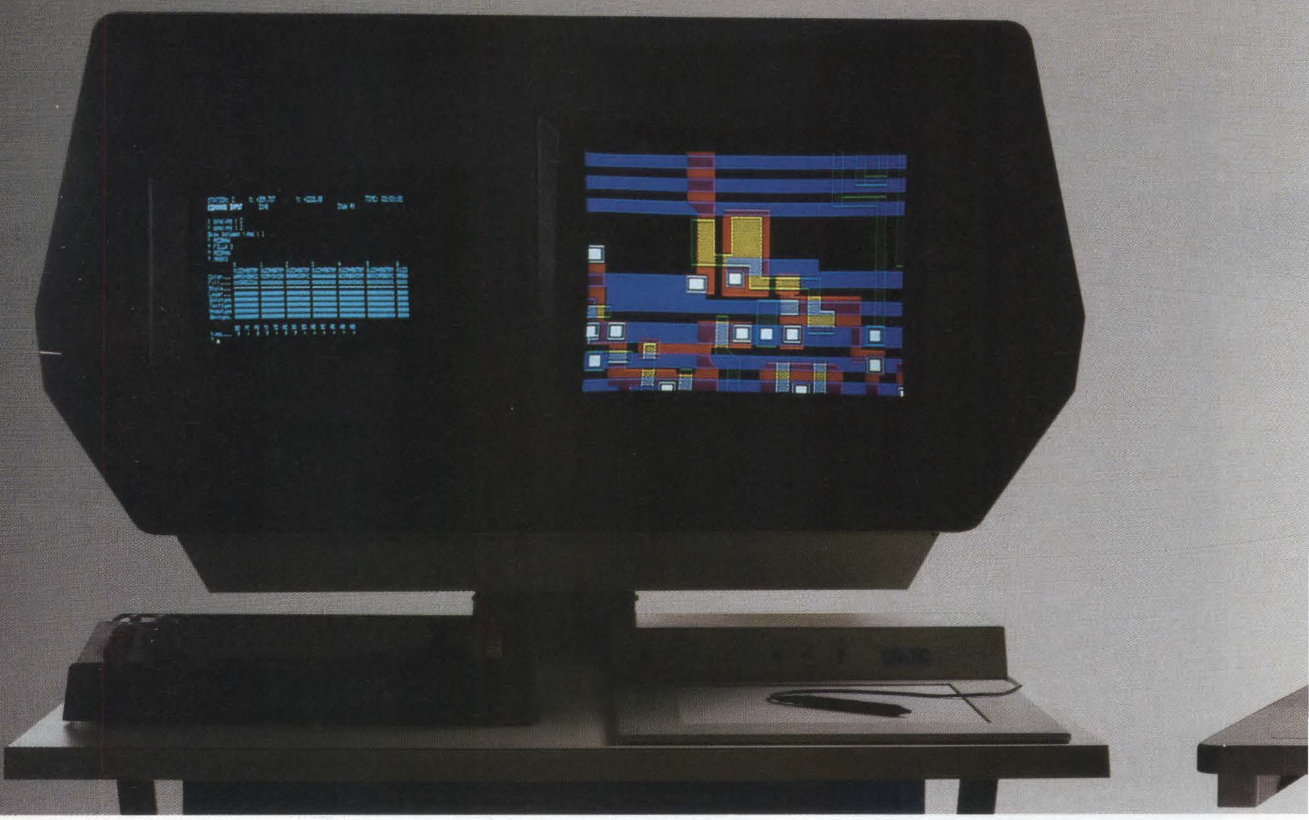

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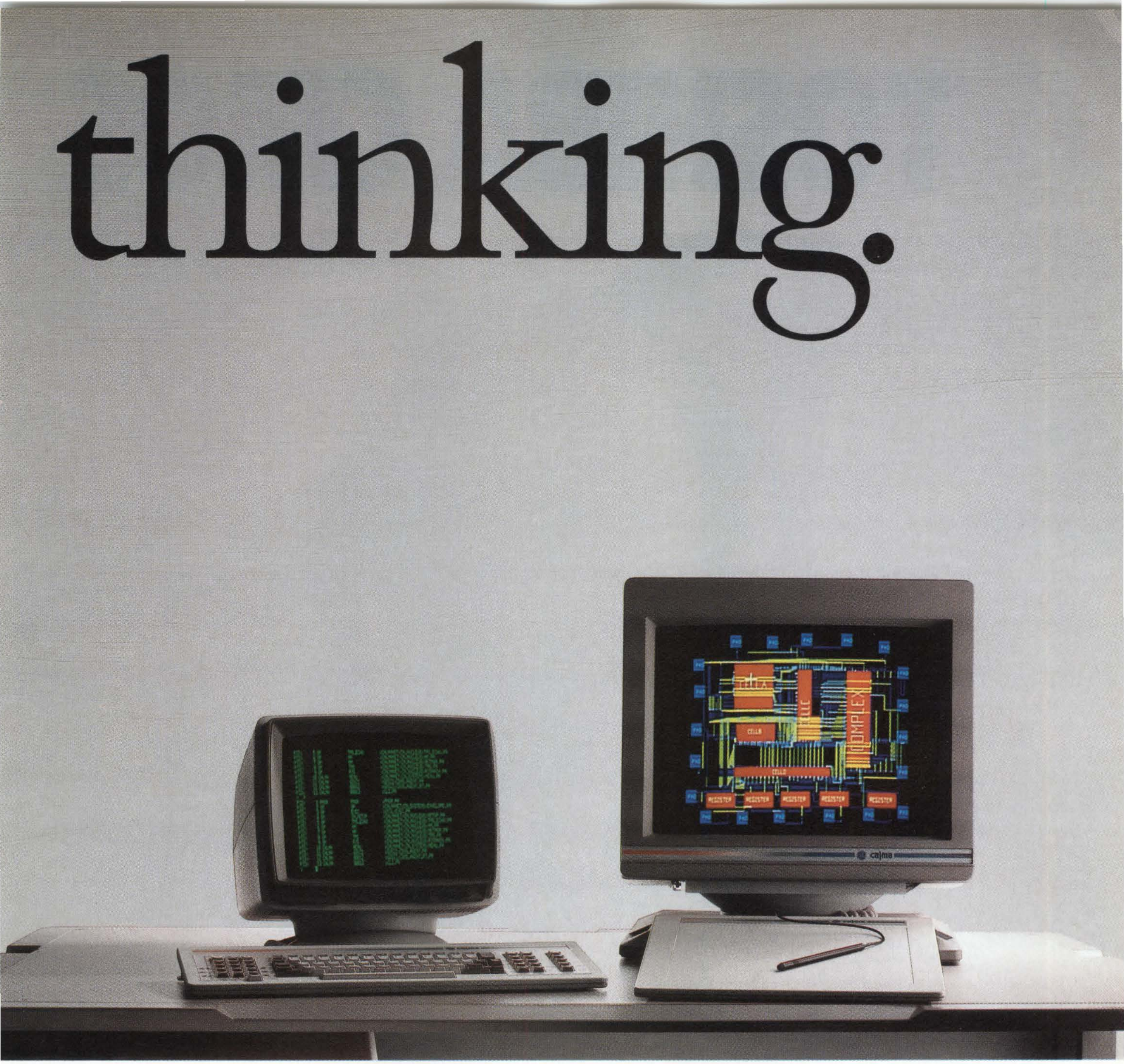

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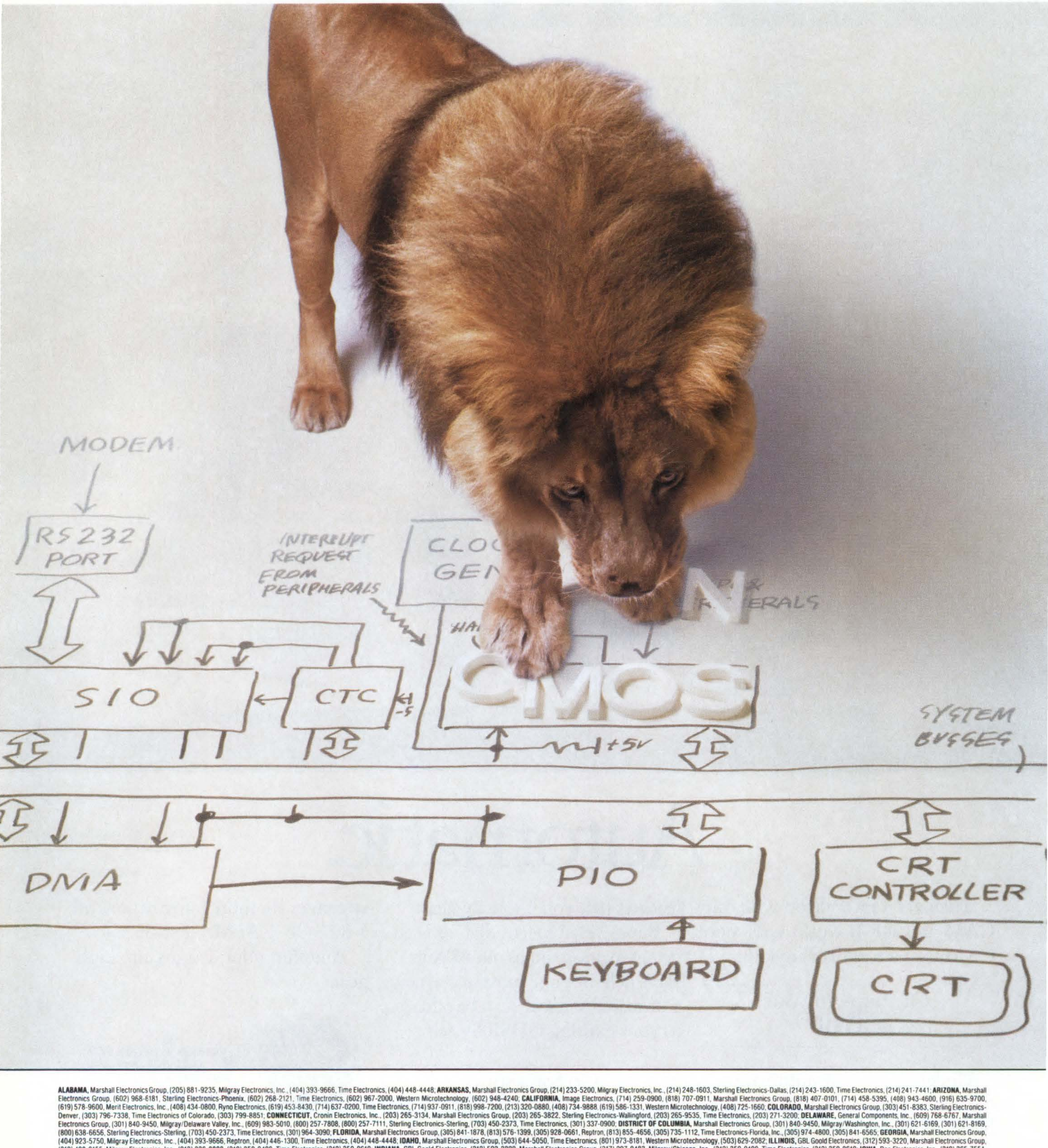


DSP chips provide building blocks for real-time signal processing

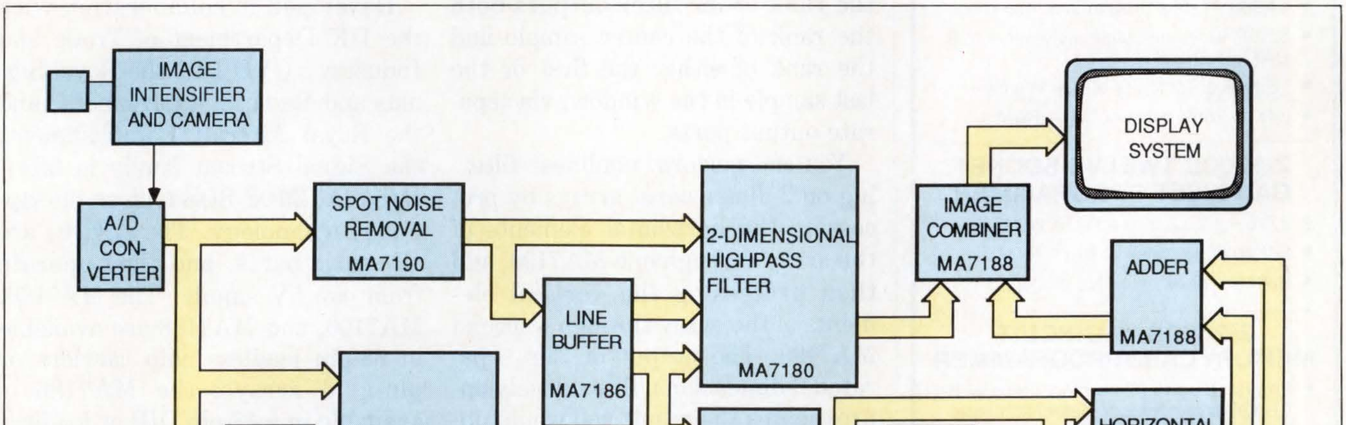
The MA7100 Signal Stream DSP chips handle 10-bit data at throughput rates as high as 20M samples/sec, allowing you to build DSP systems with a dynamic range of 60 dB and a bandwidth of 10 MHz. This level of performance makes the devices suitable for use in applications such as real-time video- and radar-image processing.

The family includes both algorithm-specific DSP ICs for linear and nonlinear filtering, and support ICs that allow you to combine devices to produce more complex DSP functions. The algorithm-specific DSP ICs comprise the MA7180 1- or 2-dimensional convolver and the MA7190 rank-order filter. The support devices include the MA7188 cascade ALU and the MA7186 video line buffer.

The MA7180 convolver performs a 2-dimensional convolution (sum of coefficient/data product pairs) on a 3×3 array of 10-bit data values with 8-bit coefficients, producing a 22-bit result. If you wish, you can round the result to 16 bits. The convolver allows you, for example, to perform lowpass noise filtering or edge detection on a video image by using a 3×3 array of pixel intensities extracted from the video image.

By adding one or more MA7186 video line buffers, you can perform 2-dimensional convolutions in real time, while a video image is being scanned. Each MA7186 can store two 64-, 128-, 256-, or 512-pixel scan lines or one 1024-pixel scan line. The MA7186 delays each line so that the corresponding 10-bit pixels are synchronized with those in the current scan line, making up the 3×3 array of pixel values. To process larger arrays, you can cascade video line buffers and convolvers and use MA7188 cascade ALUs to accumulate intermediate results.

By driving the MA7180's three 10-bit input ports with the same data, you can configure the convolver to perform a 9-stage, 1-dimensional convolution. To perform an alternative method of 2-dimensional filtering, you can add video



This DSP image-enhancement system operates in real time, *while an image is being scanned. The upper signal pathway removes spot noise introduced by the image intensifier and enhances the contrast of the image. The lower pathway eliminates background information and highlights the edges of the image.*

line buffers and cascade ALUs, cascading these 1-dimensional convolvers so that they process 2-dimensional arrays of data (for example, a 9×9 array of image pixels).

To implement functions that require nonlinear filters—functions such as spot-noise removal or background-level estimation—you can use the MA7190 rank-order filter. This device examines a moving window of 10-bit data values and reports the data value that occupies a specified rank within this window of values. The number of samples in the window (the filter length) and the rank of the data value selected for output is programmable, so you can implement various nonlinear filter functions, such as minimum, maximum, or median filters.

Alternatively, you can instruct the rank-order filter to give you the rank of particular samples in relation to the other samples contained within the window. In this mode, the rank-order filter outputs both the rank of the center sample and the rank of either the first or the last sample in the window, via separate output ports.

You can perform nonlinear filtering on 2-dimensional arrays by processing the horizontal elements of the array through one MA7190, and then processing the vertical elements of the array through a second MA7190. The output of this separated 2-dimensional filter closely approximates the result you would obtain by evaluating the rank of all the elements in the 2-dimensional array simultaneously.

A separated 2-dimensional filter requires the temporary storage of a section of the array between the horizontal and vertical rank-order filters. You can use MA7186 video line buffers to implement this store. The address generators in these buffers allow you to write rows and read columns (or write columns and read rows) of 10-bit data, simplifying the interface between the two filters. A second store, operating in the write-column/read-row mode, serves to reconstruct the output of the vertical rank-order filter, yielding a conventionally scanned video image.

The MA7188 ALU provides the arithmetic and logic functions you need when you cascade multiple MA7180 convolvers or MA7190 rank-order filters to implement more complex DSP algorithms. The ALU provides for the addition, subtraction, exclusive-ORing, or ANDing of two 16-bit input values. It can also evaluate the input's absolute value and choose between the maximum and minimum input value. An integral 16-bit-wide data-delay line (you can program the delay to between 0 and 32 clock cycles) allows you to resynchronize two data streams that have acquired different latency times in other parts of the DSP system. Alternatively, you can use the delay line to deliberately introduce latency between data samples.

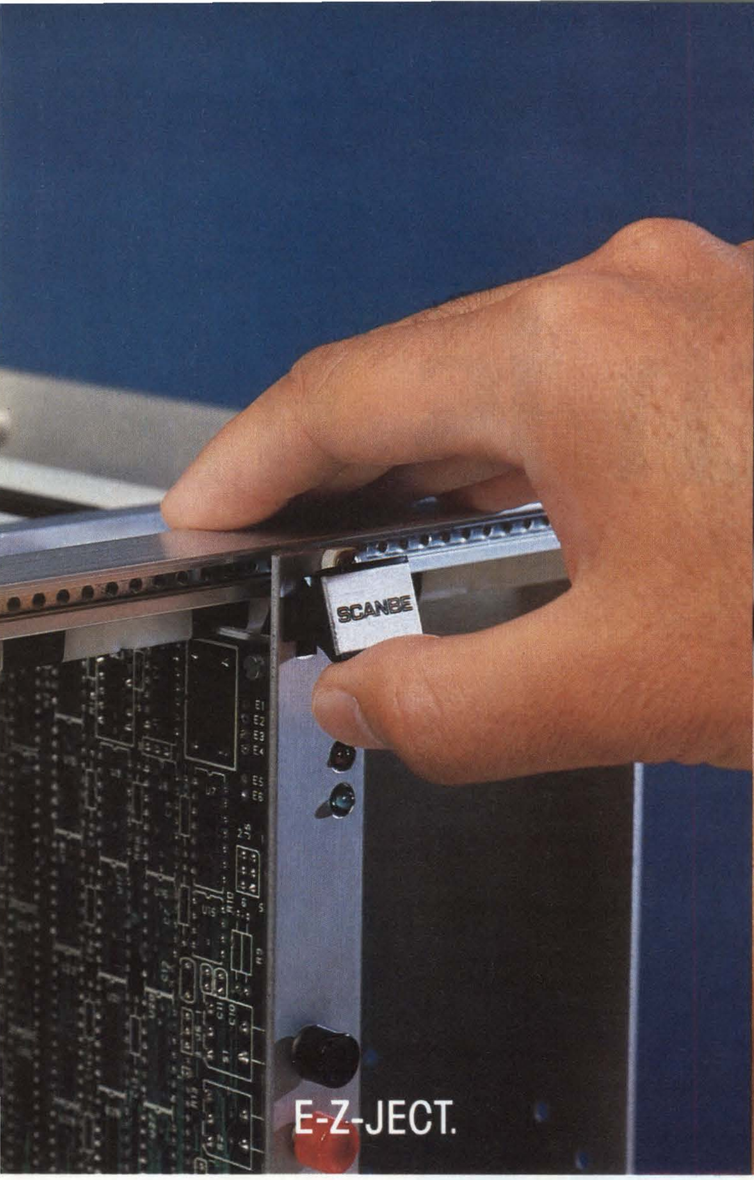
Developed in collaboration with the UK Department of Trade and Industry's CVD Div, the Royal Signals and Radar Establishment, and the Royal Aircraft Establishment, the Signal Stream family is fabricated in CMOS SOS (silicon-on-sapphire) technology. The devices are all static parts, and they operate from one 5V supply. The MA7180, MA7190, and MA7188 are available in 68-pin leadless chip carriers or pin-grid arrays; the MA7186 is available in a 48-pin DIP or leadless chip carrier. Pricing for the parts is approximately £200 for the MA7180, £150 for the MA7190, £50 for the MA7188, and £40 (1000) for the MA7186.—***Peter Harold***

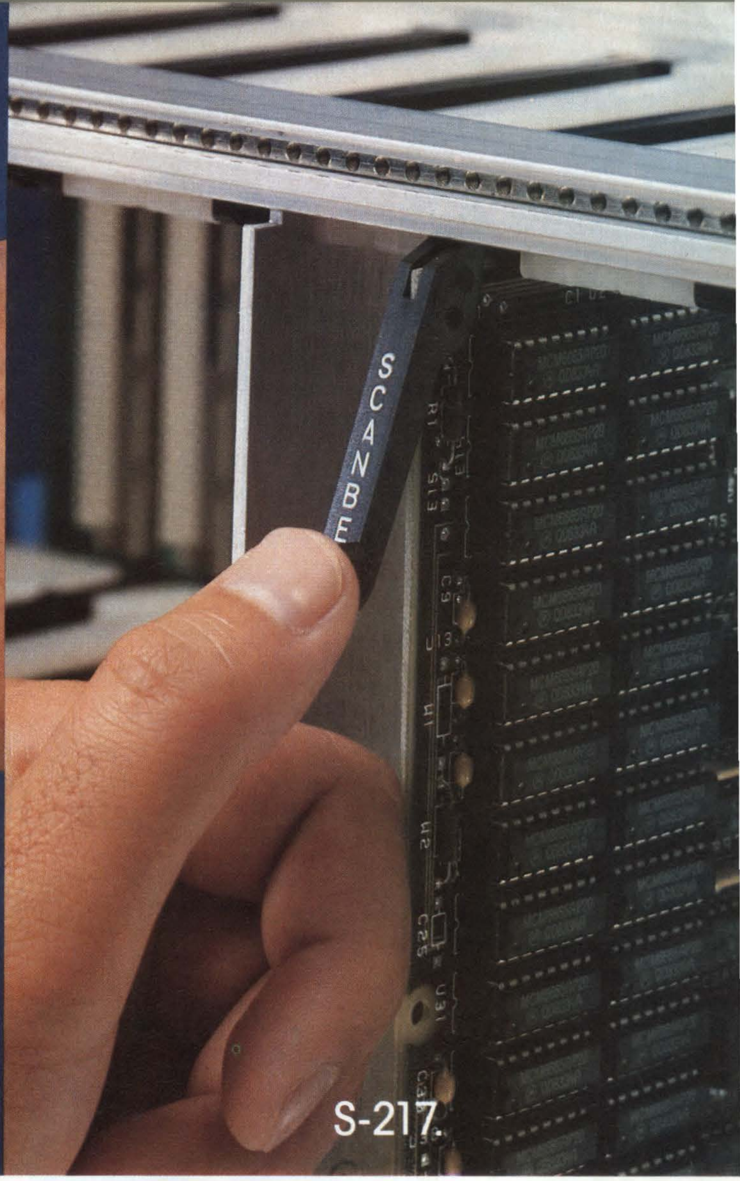
Marconi Electronic Devices Ltd, IC Div, Doddington Rd, Lincoln LN6 3LF, UK. Phone (0522) 688121. TLX 56380.

Circle No 725

Marconi Electronic Devices Inc, 45 Davids Dr, Hauppauge, NY 11788. Phone (516) 231-7710.

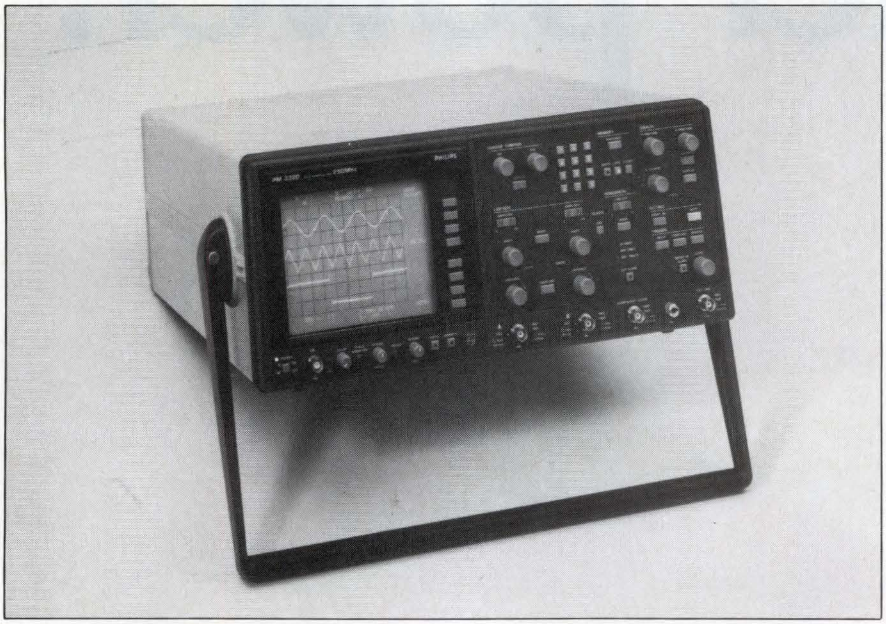
Circle No 726


SCANBE
E-Z-JECT.


SCANBE
S-217.

brighter power?

Digital storage oscilloscope captures 250M samples/sec, has 10-bit resolution



By positioning the on-screen cursors *around part of an oscilloscope trace, you can retrigger the instrument to recapture an area of particular interest with greater timebase resolution.*

The PM3320 digital storage oscilloscope (DSO) provides an equivalent analog bandwidth of 200 MHz for repetitive waveforms; in single-shot mode, it captures a minimum of 512 input samples at 4-nsec intervals. The instrument digitizes input signals to an accuracy of 10 bits. For single-channel operation, its memory depth is 4096 samples; for dual-channel operation, it is 2048 samples/channel.

You can set the scope to capture pre- or post-trigger traces, and you can capture glitches as short as 3 nsec even with the slowest timebase setting. Measurement functions include rise-time and peak-to-peak value determination, rms- or mean-value calculations, and the introduction of dc offsets as high as 300V.

The 10×12-cm CRT display includes an 8×10-cm graticuled trace area with annotation above and below the trace area, which indicates instrument settings relevant to the displayed traces. This annotated data is part of the information that the DSO transfers to a digital plotter for hard-copy recording of captured traces.

Annotations appear on the right-hand side of the display for the eight soft keys, which select secondary instrument functions. By adopting a soft-key approach to these secondary functions, the oscilloscope's front panel remains relatively uncluttered by dedicated function controls; horizontal timebase control, for example, requires two pushbuttons: one for selecting a timebase range, and one for choosing a repetitive, single-shot, or roll-mode display.

The scope also has an autoset feature, which provides rapid trace location by automatically selecting appropriate timebase and vertical-deflection sensitivities. You can store as many as 77 (optionally as many as 250) front-panel setups in nonvolatile memory and recall them either individually or in sequence.

Two on-screen cursors allow you to make measurements of captured traces. Moreover, you can use these cursors to define a portion of the captured waveform that you wish to view in more detail. The appropriate timebase and trigger delays are automatic so that the DSO can retrigger and capture this portion of the waveform with greater timebase resolution.

Optional IEEE-488 and RS-232C interfaces allow you to add remote programming and downloading of captured trace information. In addition, the interfaces enable you to display operator prompts or other information on the CRT. The interface card provides the instrument with a real-time clock also. The PM3320 is priced at $9900; delivery, eight weeks ARO.—***Peter Harold***

Philips, Industrial and Electroacoustic Systems Div, Box 218, 5600 MD Eindhoven, The Netherlands. Phone (040) 788620. TLX 35000.

Circle No 729

Philips Test & Measuring Instruments Inc, 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800. TWX 710-988-5348.

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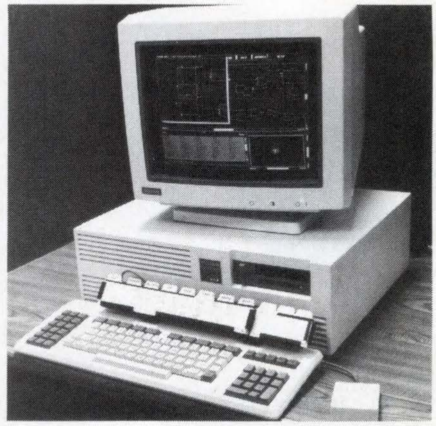
CIRCLE NO 140

Family of silicon compilers aids system and chip design

To lower the cost of silicon-compiler software, the general-purpose Genesil program is now available as five individual special-purpose packages: MacroCompiler, LogicDesigner, ChipBuilder, Mentor Series, and Server. Each package targets the requirements of a different type of IC designer. For example, ChipBuilder assists IC-layout specialists, whereas LogicDesigner helps engineers who want to have a third party lay out their chips.



Once you've entered and simulated *a design on a Mentor Graphics' workstation, you can use the Mentor Series package from Silicon Compiler Systems Corp (formerly Silicon Compilers Inc) to implement the design as a custom IC.*

MacroCompiler compiles cell blocks, but it can't combine the blocks into a complete IC layout. It compiles cell blocks such as RAMs, ROMs, data paths, random logic, PLAs, and multipliers. The package generates a geometric database and a logic-simulation model of each block.

LogicDesigner doesn't lay out complete ICs either, but it calculates device speed and die size in addition to compiling blocks. To estimate the characteristics of a completed IC, the program creates a layout in generic 3-, 2-, and 1.25-μm processes. Once you're satisfied with a design's speed and size, you can transmit a LogicDesigner file to the company's Prototype Tapeout Service, which optimizes the layout and places orders for prototypes from a foundry.

You don't have to transmit files to the Prototype Tape Service, however. You can lay out the chips yourself. The ChipBuilder package combines cell blocks into a complete IC layout and optimizes chip speed and size. It includes floor-planning, routing, and process-specific software.

The fourth package, the Mentor Series, provides both block-compilation and custom-IC layout tools. The package runs on Mentor Graphics' (Beaverton, OR) CAE systems and uses that company's schematic-entry and logic-simulation software to generate cell blocks.

The Mentor Graphics software runs on Apollo (Chelmsford, MA) workstations, but silicon compilation requires the memory and speed of a VAX. By using the Server package, you can enter a design on an Apollo workstation and run compilation and analysis programs on a VAX. This package gives every node on an Apollo-based network access to silicon compilation.

MacroCompiler sells for $75,000, and LogicDesigner costs $79,500. The Mentor Series is priced at $159,500; each Server package costs $450. The price of ChipBuilder depends on the host computer. For a MicroVAX II, for example, it costs $119,000; for a VAX 8650, it costs $295,000.—***Eva Freeman***

Silicon Compiler Systems Corp, 2045 Hamilton Ave, San Jose, CA 95125. Phone (408) 371-2900.

Circle No 728

SCSI development tools fill lab, field, or factory roles

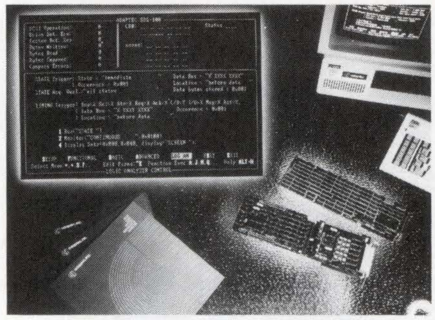
The SDS family of products can aid you in designing and developing SCSI-based host-adapter and peripheral-controller applications. These IBM PC-based products also suit factory- and field-test tasks. The product family includes the SDS-2 SCSI development and test system, the SDS-100 SCSI test system, and the SDS-210 SCSI logic analyzer.

The SDS-2 combines initiator- and target-emulation capabilities, allowing you to test and debug both host-adapter and peripheral-controller SCSI designs. You can connect the personal computer that runs the SDS-2 software to a SCSI host via an RS-232C link, so you can control the entire test environment from the PC.

The SDS-2 system includes two different software packages with different user interfaces. One software package allows you to select test functions from a menu. The other package provides a C programming language that you can use to develop hands-off comprehensive and repetitive tests. The SDS-2 also offers a library for use with both packages; the library includes more than 250 test functions that can be used to construct test sequences.

For dedicated test operations, you can use the SDS-100 test system. It includes a board and a software package that provides more than 50 preprogrammed SCSI test functions. The software accesses the SCSI bus through a special-purpose test adapter. The SDS-100 can also execute SCSI test routines that you've developed on the SDS-2.

With either the SDS-2 or the SDS-100 you can purchase the SDS-210 SCSI logic analyzer. The logic analyzer monitors and interprets SCSI-bus activity. Unlike μP logic analyzers that sample data at given intervals, the SCSI logic analyzer samples the bus on an event-driven basis. The analyzer employs a 10-MHz internal reference clock, and it acquires data by means of user-selectable criteria. It displays its analysis results in a variety of nonbinary, high-level formats.



The SDS-2 development system and SDS-210 logic analyzer *support the design and development of host-adapter and peripheral-controller SCSI implementations.*

The SDS-2 package includes an IBM PC/XT computer, a SCSI test and development board, and software. The complete package costs $19,500; you can buy the development system without the computer for approximately $16,000. At $5500, the SDS-100 add-in board and software fits factory- and field-test roles. You can add the SDS-210 logic analyzer to either system for $3750 if you purchase it with the SDS-2 or SDS-100, or $4500 if you purchase it later as an upgrade.

—Maury Wright

Adaptec Inc, 580 Cottonwood Dr, Milpitas, CA, 95035. Phone (408) 432-8600.

Circle No 727

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The K222L makes possible a variety of new applications. It is ideal for low-power, low-voltage modems; battery-powered, portable modems; power-sensitive laptop PC's; and telephone-line-powered modems—or any application where space and power is at a premium.

Best of all: the K222L is part of the K-Series family, so all existing 1200 bps modems designed with the Silicon Systems K212L or K221L can be easily upgraded by plugging the K222L into the same socket. And in the future—all modems designed with the K222L can be further upgraded to 2400 bps operation with the Silicon Systems K224L.

For more information on the K222L, or the other K-Series modem IC's, contact: **Silicon Systems,** 14351 Myford Road, Tustin, California 92680, phone: (714) 731-7110, Ext. 575.

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Circle 74 for Product Information

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*Available 2nd quarter 1987

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16Kx4 25ns 70/20mA
CY7C164
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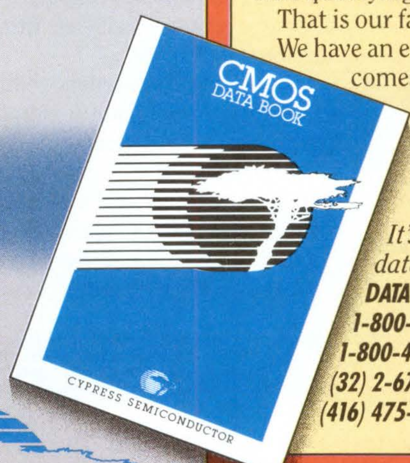
CY7C166
16Kx4 25ns 70/20mA
CY7C187
64Kx1 25ns 70/20mA



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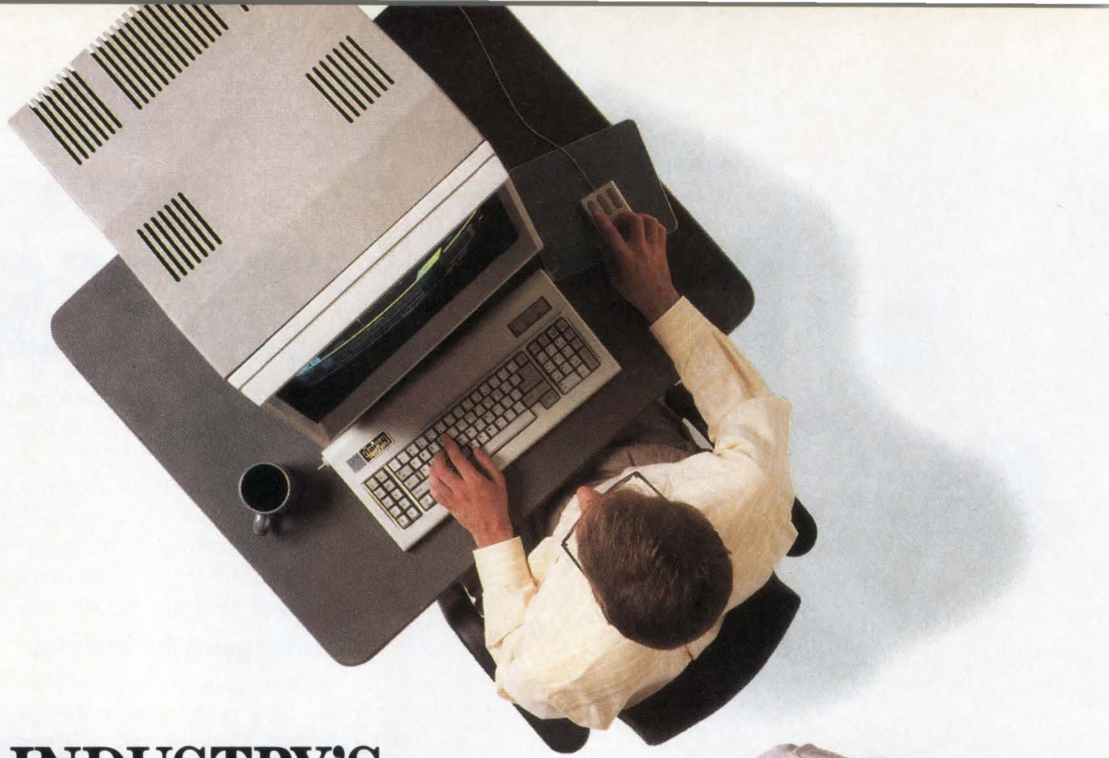

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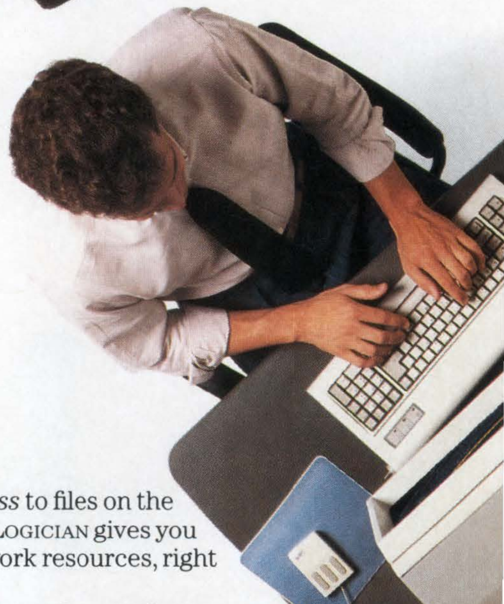

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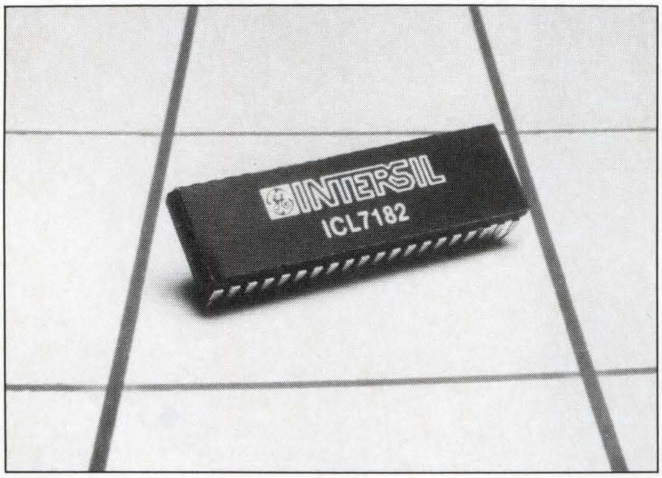
READERS' CHOICE

Of all the new products covered in EDN's **February 19, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **February 19, 1987,** issue.

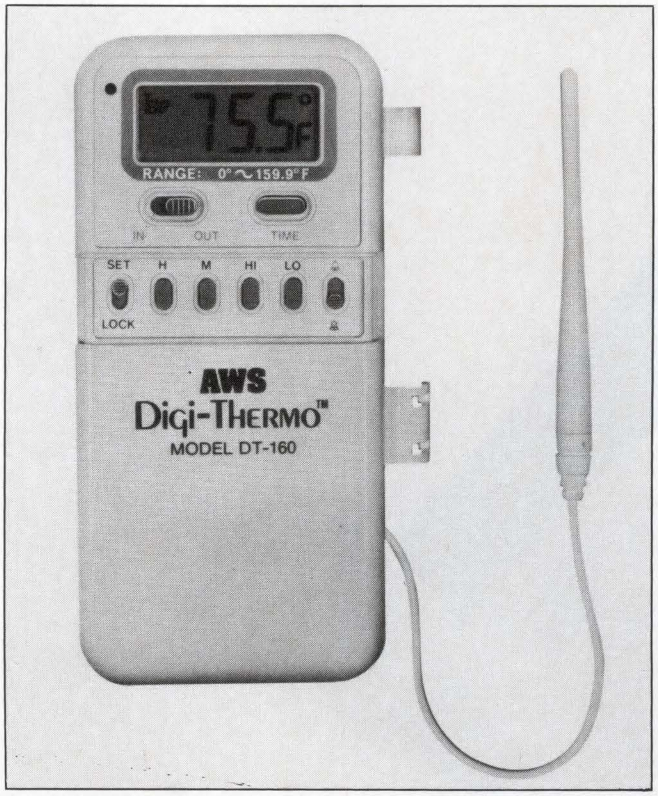


▲ BAR-GRAPH ADC

Model ICL7182 is an A/D converter that not only directly drives a multiplexed LCD but also requires only three external components to drive a 101-segment bar graph (pg 245).
GE/Intersil.
Circle No 603

MODULA-2 COMPILER

This Modula-2 compiler runs on any 8086/88-based machine under IBM PC-DOS or generic MS-DOS (pg 257).
Farbware.
Circle No 604



▲ DIGITAL THERMOMETER

The DT-160 pocket-sized digital thermometer measures 0 to 159.8°F. A temperature sensor mounted on the front panel allows you to display a room or probe temperature (pg 274).
A W Sperry Instruments Inc.
Circle No 605

▲ SCANNER

The Image Scanner Option Kit for Epson's EX-800, EX-1000, and LQ-2500 dot-matrix printers works with IBM PCs and compatibles equipped with EGA, CGA, or Hercules display adapters (pg 235).
Epson America.
Circle No 602

BURN-IN SOCKET

Simple and quick loading of plastic leaded chip carriers (PLCCs) is a key feature of these 68-pin burn-in sockets (pg 211).
3M.
Circle No 601

OPEN A NEW LINE OF COMMUNICATION.

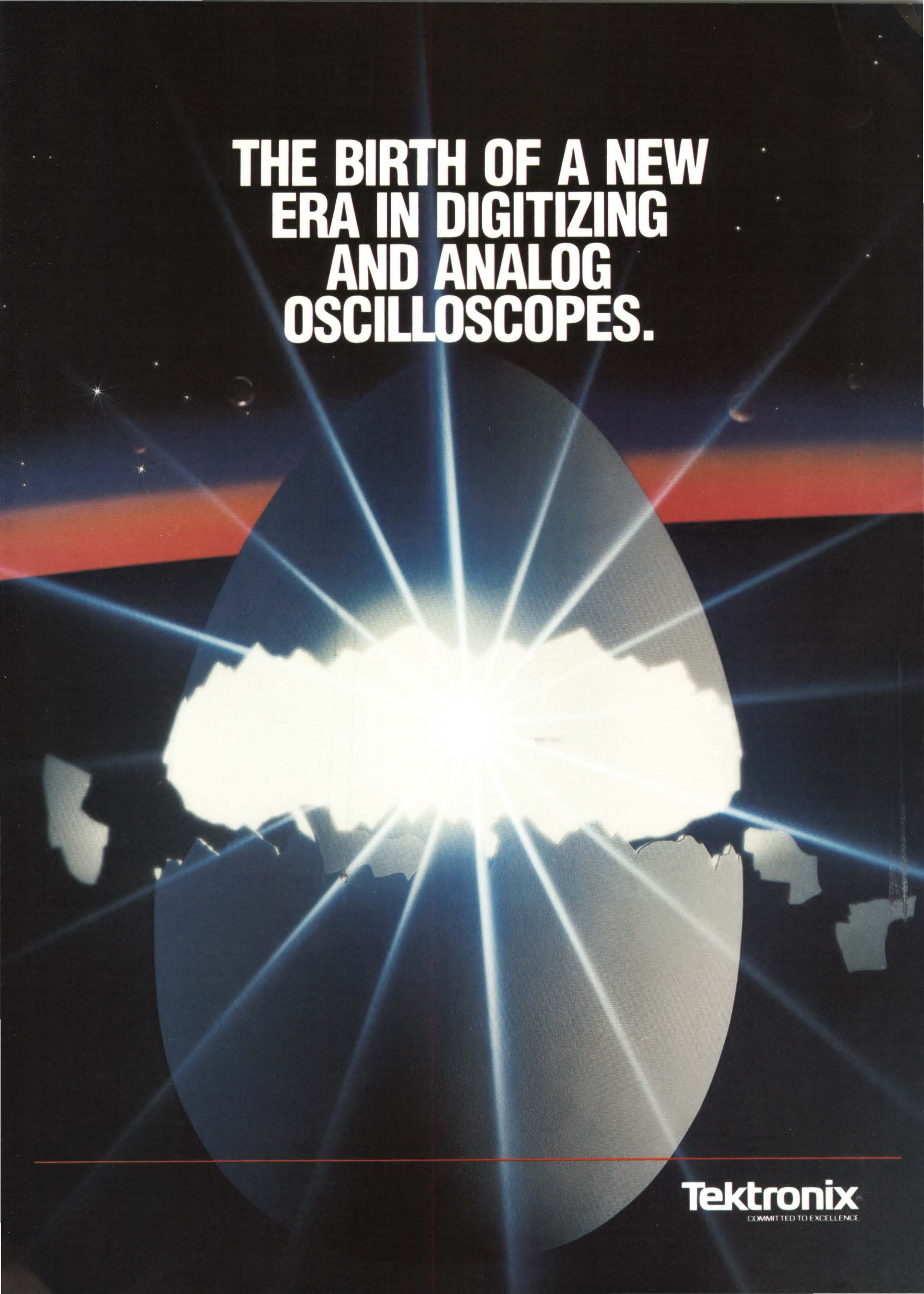
LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	6	19	56	13	6	0	8.6	11.0
Pot-Core	11	22	34	22	11	0	9.6	10.2
Laminate (power)	7	20	60	6	7	0	8.1	9.3
CONNECTORS								
Military panel	0	25	38	25	12	0	10.8	13.7
Flat/Cable	25	25	25	25	0	0	6.6	5.1
Multipin circular	22	11	45	22	0	0	7.3	13.1
PC	15	31	39	15	0	0	6.4	6.2
RF/Coaxial	11	34	22	33	0	0	7.9	6.6
Socket	40	27	20	13	0	0	4.5	5.4
Terminal blocks	28	39	28	5	0	0	4.3	5.9
Edge card	15	39	31	15	0	0	6.0	6.3
Subminiature	22	34	22	22	0	0	6.0	5.7
Rack & panel	10	50	30	10	0	0	5.5	7.6
Power	22	34	33	11	0	0	5.4	7.6
PRINTED CIRCUIT BOARDS								
Single-sided	0	60	27	13	0	0	6.0	5.6
Double-sided	0	45	50	5	0	0	6.1	6.4
Multilayer	0	7	79	14	0	0	8.7	8.0
Prototype	0	71	23	6	0	0	4.9	4.8
RESISTORS								
Carbon film	42	16	26	16	0	0	5.0	2.5
Carbon composition	34	33	11	22	0	0	5.3	4.6
Metal film	29	24	24	23	0	0	6.2	4.0
Metal oxide	20	50	10	20	0	0	5.4	3.6
Wirewound	25	19	31	25	0	0	6.9	5.3
Potentiometers	20	16	48	16	0	0	6.8	5.9
Networks	17	16	39	28	0	0	7.9	6.1
FUSES	39	33	17	11	0	0	4.1	4.8
SWITCHES								
Pushbutton	31	19	38	12	0	0	5.5	7.5
Rotary	17	25	33	25	0	0	7.3	7.5
Rocker	31	31	31	7	0	0	4.6	7.2
Thumbwheel	34	11	33	22	0	0	6.4	10.5
Snap action	34	22	33	11	0	0	5.1	8.7
Momentary	27	9	37	27	0	0	7.4	8.7
Dual in-line	11	22	56	11	0	0	6.8	9.2
WIRE AND CABLE								
Coaxial	23	38	31	8	0	0	4.8	3.1
Flat ribbon	38	19	31	12	0	0	5.0	3.3
Multiconductor	29	28	36	7	0	0	4.8	3.8
Hookup	55	35	10	0	0	0	1.9	1.6
Wire wrap	45	33	22	0	0	0	2.8	2.1
Power cords	21	37	42	0	0	0	4.5	4.3
Other	25	0	75	0	0	0	6.0	4.9
POWER SUPPLIES								
Switching	14	7	50	22	7	0	9.4	9.8
Linear	18	18	37	18	9	0	8.6	6.2
CIRCUIT BREAKERS	20	40	27	13	0	0	5.4	7.4
HEAT SINKS	17	25	50	8	0	0	6.0	5.4

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	39	22	22	11	6	0	5.6	5.5
PC board	13	20	40	27	0	0	7.9	8.0
Dry reed	12	38	12	38	0	0	7.9	5.7
Mercury	12	0	63	12	13	0	10.1	7.7
Solid state	13	33	27	20	7	0	7.9	5.6
DISCRETE SEMICONDUCTORS								
Diode	25	25	30	20	0	0	6.3	4.3
Zener	24	29	18	29	0	0	6.9	6.3
Thyristor	0	40	30	30	0	0	8.3	5.4
Small signal transistor	13	27	33	27	0	0	7.6	7.0
FET, MOS	0	56	22	22	0	0	6.9	7.6
Power, bipolar	15	31	39	15	0	0	6.4	8.1
INTEGRATED CIRCUITS, DIGITAL								
CMOS	11	34	33	22	0	0	7.1	8.2
TTL	13	34	40	13	0	0	6.3	5.5
LS	7	33	47	13	0	0	6.8	5.9
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	22	11	34	33	0	0	8.2	9.4
OP amplifier	6	31	44	19	0	0	7.3	8.5
Voltage regulator	8	39	38	15	0	0	6.6	6.7
MEMORY CIRCUITS								
RAM 16k	31	15	23	31	0	0	7.1	5.5
RAM 64k	33	17	33	17	0	0	5.8	5.2
RAM 256k	20	10	40	30	0	0	8.2	6.9
ROM/PROM	27	9	46	18	0	0	6.7	5.9
EPROM	25	38	12	25	0	0	6.0	7.0
EEPROM	11	22	34	33	0	0	8.5	7.3
DISPLAYS								
Panel meters	11	11	56	22	0	0	8.2	5.7
Fluorescent	0	0	57	43	0	0	11.2	8.4
Incandescent	0	25	50	25	0	0	8.6	7.4
LED	12	31	44	13	0	0	6.4	6.3
Liquid crystal	0	25	37	38	0	0	9.6	8.2
MICROPROCESSOR ICs								
8-bit	7	36	29	28	0	0	7.8	7.4
16-bit	11	11	56	22	0	0	8.2	7.4
FUNCTION PACKAGES								
Amplifier	11	11	22	45	11	0	11.8	9.1
Converter, analog to digital	10	20	60	10	0	0	7.0	8.0
Converter, digital to analog	11	22	45	22	0	0	7.7	8.6
LINE FILTERS	12	13	50	25	0	0	8.3	7.0
CAPACITORS								
Ceramic	32	26	32	10	0	0	4.9	6.4
Ceramic monolithic	25	38	31	6	0	0	4.6	8.1
Ceramic disc	15	54	31	0	0	0	4.7	7.5
Film	23	23	54	0	0	0	5.0	8.1
Electrolytic	28	28	33	11	0	0	5.2	6.6
Tantalum	6	44	38	12	0	0	6.3	6.8
INDUCTORS	8	31	38	23	0	0	7.6	8.5

Source: *Electronics Purchasing* magazine's survey of buyers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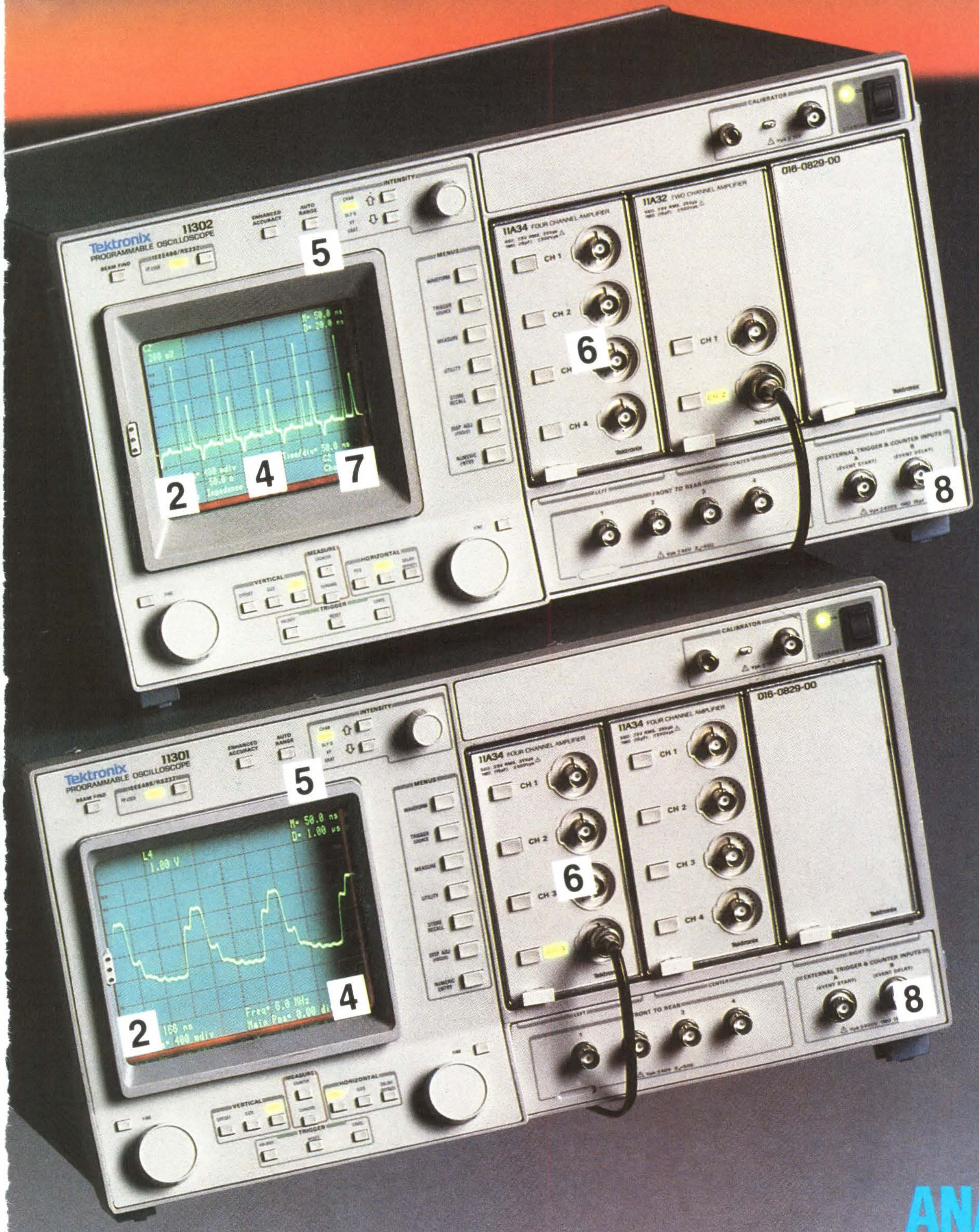
Vert. Sensitivity[4]	1 mV/div	1mV/div	Vert. Sensitivity[4]	1 mV/div	1 mV/div
Vert. Resolution	10-14 bits[3]	10-14 bits[3]			
Automatic Measurements	Min, Max, Mid, Mean, RMS, Peak-Peak, Rise, Fall, Width, Delay1, Cross, Period, Frequency, Main→ Window Trigger, YT Area, YT Energy, Cursors		Automatic Measurements	Peak-Peak, Min, Max, Mid, Frequency, Period, Width, Duty Cycle	
Timebase Accuracy	100 ps + .002% of the measured interval		Built-in counter/ timer	500 MHz 6 Function 10 digits	500 MHz 6 Function 10 digits

[1]Up to 8 traces may be displayed at once from any of up to 12 input channels.
[2]Absolute DC accuracy with full scale offset or Vc.
[3]14-bit resolution obtained using signal averaging.
[4]Except with 11A71 which has 10mV/div

Demonstrations are now in progress throughout North America. To get in touch with the future of measurement, contact your local Tek sales engineer or call Tektronix at 1-800-547-1512.



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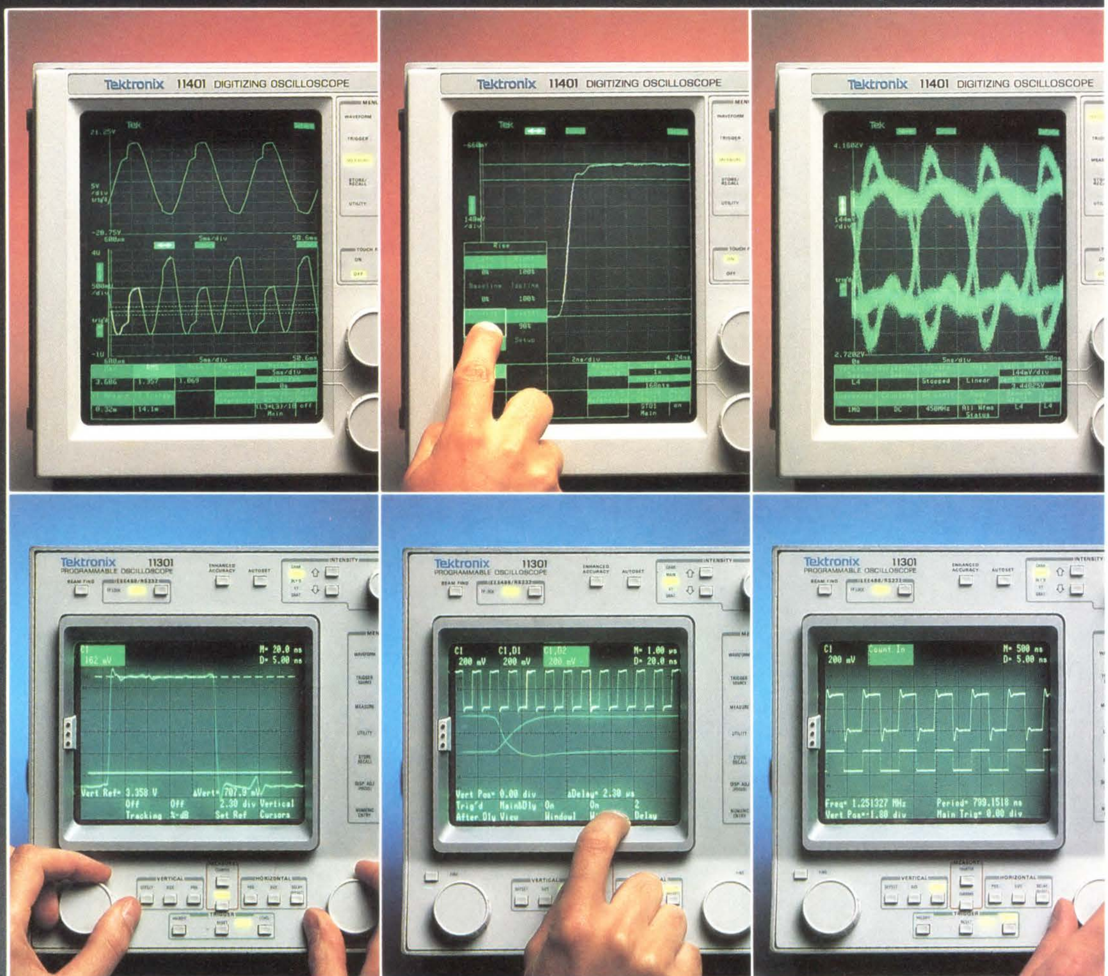
11401/11402 Digitizing Oscilloscopes

One example of innumerable waveform processing capabilities: square a voltage waveform and divide by a load resistance — (L3*L3)/10 — to make a power measurement.

Customize automatic measurements to meet your needs. Touching any measurement result, for example, causes annotation to appear showing exactly where the measurement is being taken.

Point Accumulate Mode keeps all digitized points in display memory to help you handle complex displays such as eye diagrams, measure worst case jitter, or catch low rep-rate glitches.



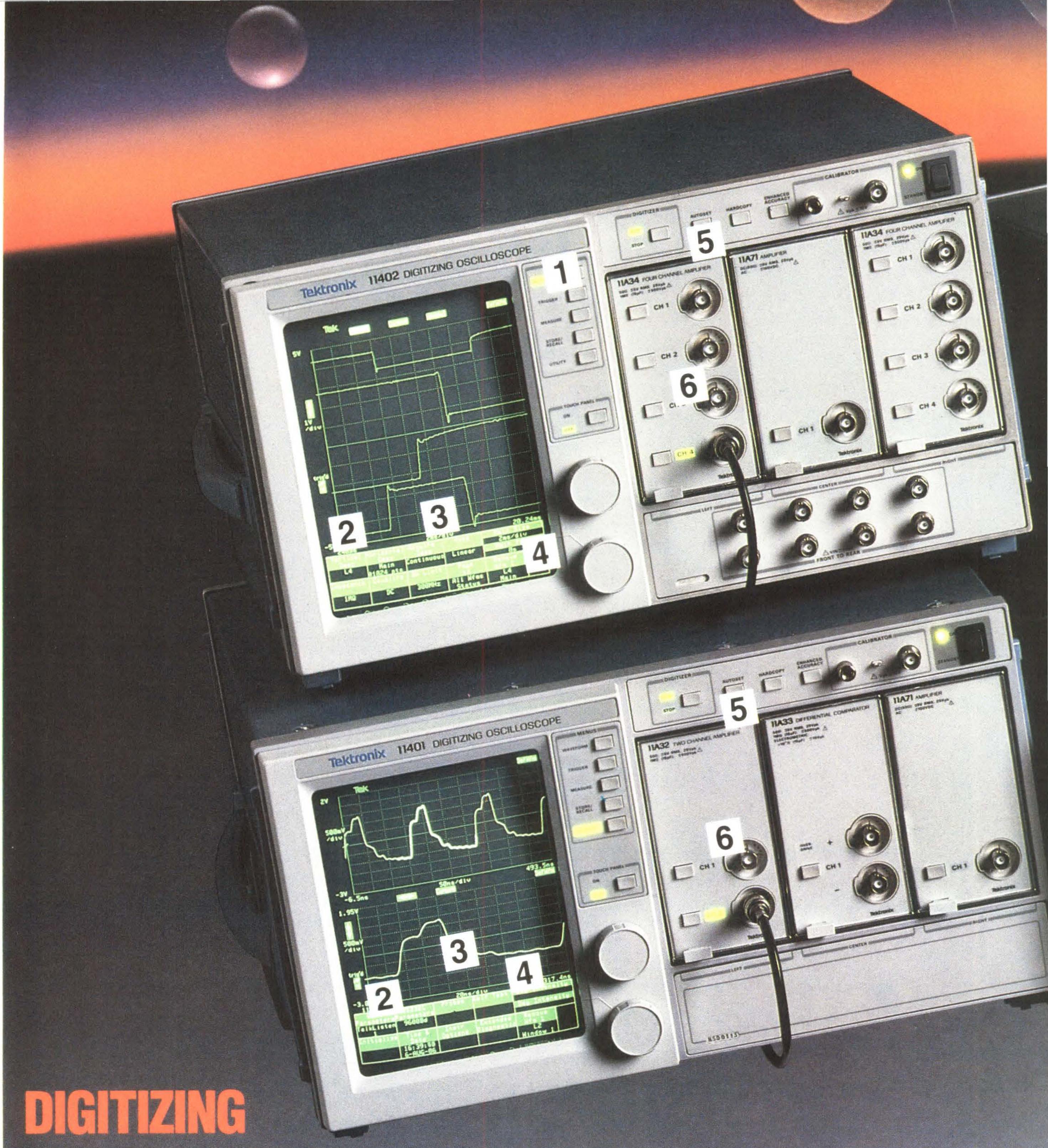
11301/11302 Analog Oscilloscopes

Call up cursors to help you make high-accuracy measurements, displayed in decibels, percent, degrees, volts or seconds.

Dual delayed sweeps allow expansion of the main sweep for close examination and accurate measurement of waveform parameters such as risetime and falltime.

Integrated 500 MHz universal counter/timer includes a unique counter-view feature that lets you see exactly what the counter/timer is triggering on.

CIRCLE NO 40



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1 **1 GHz.** The 11402 Digitizing Oscilloscope features a full 1 GHz bandwidth right at the probe tip—with no sacrifice in vertical resolution—to help you make the most demanding voltage and timing measurements.

2 **UP TO 8 TRACES.** High-resolution screen lets you display up to eight waveforms simultaneously, with an update nearly as fast as an analog scope. No scopes ever let you see so much at once.

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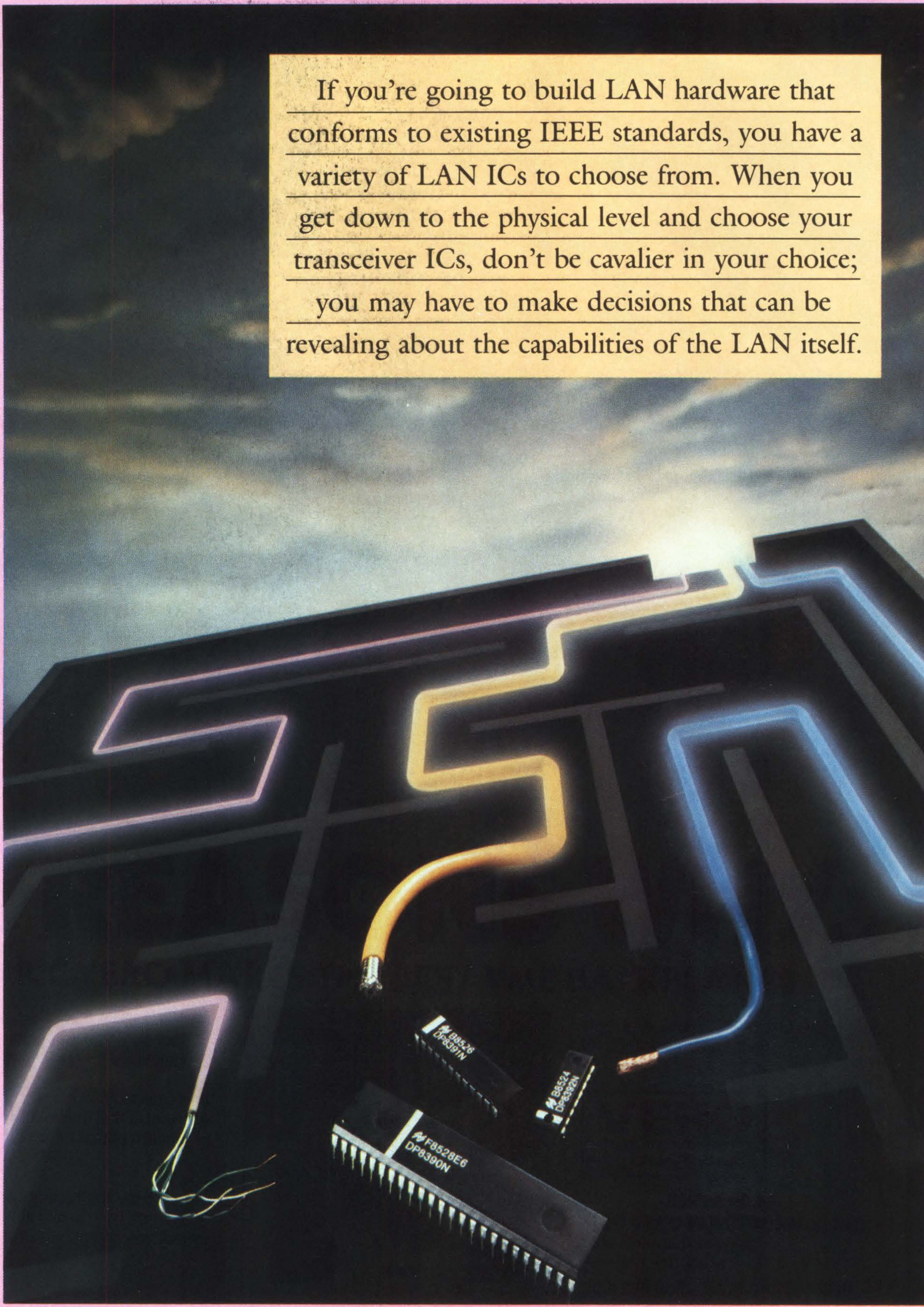
If you're going to build LAN hardware that conforms to existing IEEE standards, you have a variety of LAN ICs to choose from. When you get down to the physical level and choose your transceiver ICs, don't be cavalier in your choice; you may have to make decisions that can be revealing about the capabilities of the LAN itself.



Effective LAN designs begin with IC families that support the physical level; *these families, which include controllers and transceivers, can point the way through the bewildering maze of LAN architectures. (Photo courtesy National Semiconductor)*

Special Report

LAN ICs for IEEE-802 networks

Jim Wiegand, *Associate Editor*

The 7-layer Open Systems Interconnect (OSI) model for local-area networks (LANs), promulgated by the International Standards Organization, purports to specify all levels of the connection between the computer and the physical medium, from the topmost, application layer (layer 7) down to the physical layer (layer 1). You'll find that the physical layer is the best represented level of the network, with respect to available products, but the least discussed aspect of LANs. When you're selecting the ICs for your network hardware, however, you must pay as much attention to your choice of ICs for that physical level—the transceivers—as you do to the controller and encoder ICs. And when you're exploring the physical layer, you'll discover differences between the existing IEEE-802 architectures that are not often broached in the otherwise ample trade-press coverage of LANs.

In the US, the IEEE-802 LAN standards are becoming an increasingly popular realization of the OSI model (see **Ref 1**). **Table 1** (see page 133) lists the existing families of IEEE-802 LAN ICs, including transceivers. Transceivers provide the functions necessary to transfer data to and from a LAN's physical communications medium; you can't directly drive a coaxial cable, for example, with a protocol-controller chip. Transceivers are analog devices that provide buffering, filtering, level translation, and, in some cases, collision detection and clock generation. They form part of the network node, along with the controller and encoder circuitry. Your choice of transceiver is determined by such factors as speed, signaling requirements, the type of transmission medium, and ancillary LAN functions.

You may distinguish the variety of IEEE-802 LAN architectures from one another by the method used to access the transmission medium. Networks conforming to the IEEE 802.3 standard—Ethernet, Thinnet (Cheapernet), and StarLAN—employ the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access scheme. Transceivers for Ethernet and Thinnet are listed in **Table 1;** you can use RS-422 drivers as StarLAN transceivers.

IEEE-802.4 specifies a token-passing-bus access method (token bus, for short). The Manufacturing Automation Protocol (MAP) promulgated by General Motors is the leading contender for LANs using this approach. IEEE-802.5 specifies a token-passing-ring access method (token ring, for short), and IBM's implementation of this scheme appears to be taking over as the de facto standard for this architecture.

A LAN's access method does not entirely dictate the type of medium, and consequently the type of transceiver, you must use for the first network layer. For example, existing CSMA/CD LANs that adhere to the 802.3 recommendations em-

Your choice of transceiver is determined by such factors as speed, signaling requirements, and ancillary LAN functions.

ploy a variety of coaxial and twisted-pair cabling schemes.

Ethernet is an 802.3-type LAN that uses 0.4-in. coaxial cable as its transmission medium. It's a baseband network that operates at a speed of 10M bps and is configured in a bus topology. Most transceivers for Ethernet systems provide three basic functions: collision detection, antijabber, and line driving. If you select a transceiver that's lacking one or more of these functions, you'll have to ensure that some other part of the system provides the functions in question.

In a bus-based CSMA/CD system such as Ethernet, each station (the user equipment and its associated network-node circuitry) attached to the network is responsible for monitoring the bus for collisions between two or more attempts to access the network. If the transceiver detects a collision, the transmitting stations jam the network long enough for other stations connected to the bus to recognize that a collision has occurred. The stations then wait for a pseudorandom period of time before attempting to retransmit.

Transceivers use a level detector to perform the collision-detection function. The level detector compares the transmitted signal with the signal on the bus. If the two signals are identical, then a proper transmission is under way. If a collision has occurred, the signal on the bus will be the sum of the colliding signals and will therefore trip the level detector. The transceiver will then relay this information back to the LAN controller.

Keep your terminal equipment honest

Transceivers provide antijabber protection through use of a watchdog timer, which ensures that the LAN station doesn't gain control of the bus, lose track of the program it's running (as a result of any of a variety of causes), and then tie up the bus indefinitely. The transceiver will disable itself if it finds that it has transmitted for a period of time that exceeds the jabber time period.

The Ethernet specification requires that data be Manchester-encoded for transmission. Some transceivers will accept both Manchester-encoded signals and NRZ signals. If you give such a transceiver NRZ signals, it will perform the Manchester encoding for you. Other transceivers accept only encoded signals.

Because collision detection is carried out by means of a level detector, you must configure the transmitter portion of your Ethernet transceiver as a current-source output, in order to allow for the superposition of colliding signals. You must be careful to load the bus as little as possible, to avoid reflections on the bus and to minimize attenuation. Good analog design practices, such as limiting the length of pc-board traces, will ensure that your transceiver interface doesn't overload the Ethernet bus.

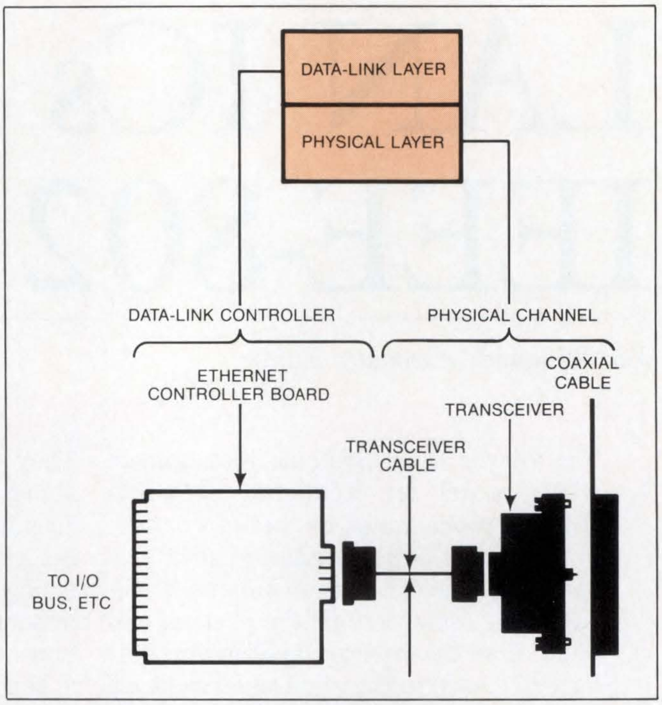


***Fig 1—The Ethernet specification requires** that you provide a separate, isolated transceiver module as the interface between the Ethernet controller and the Ethernet coaxial cable.*

The receive portion of the tranceiver must filter the incoming signal from the transmission medium to eliminate noise and avoid the acquisition of false signals. The receiver will recover and separate the clock and data information from the bus. Manchester-encoded data consists of, first, the inverted signal, and then the noninverted signal, packed into one bit time. This type of encoding ensures that there is one transition per bit time, thereby incorporating a clock signal into the data stream. After recovery and separation, the transceiver sends the data and clock to the controller.

Configure transceiver in separate module

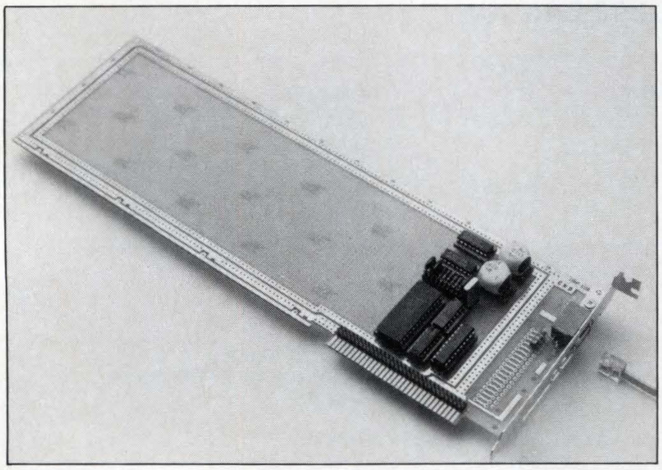
In the case of an Ethernet system, you build your transceiver in a separate module and isolate it from the Ethernet station **(Fig 1)**. You can use pulse transformers or optoisolators to isolate collision, receive, and transmit signals. You can accomplish the requisite power isolation for the transceiver module through the use of a dc/dc converter. On the other side, you connect the transceiver to the Ethernet coaxial cable via an

TABLE 1—IEEE-802 LAN ICs

MANUFACTURER	PART	FUNCTION	IEEE APPLICATION	PRICE (100)*	COMMENTS
ADVANCED MICRO DEVICES	7996	TRANSCEIVER	802.3	$23.90	10BASE5 (ETHERNET); 10BASE2 (THINNET); INCLUDES COLLISION DETECTION
	7990	CONTROLLER	802.3	$54.95	10BASE5; 10BASE2
	7992B	SERIAL INTERFACE ADAPTER	802.3	$19.15	10BASE5; 10BASE2; INCLUDES MANCHESTER ENCODING
EXAR	XRT82515	TRANSCEIVER	802.3	$15 TO $20 (SAMPLES)	1BASE5 (STARLAN)
	XRT82C516	ENCODER	802.3	$15 TO $20 (SAMPLES)	1BASE5
INTEL	82586	COPROCESSOR	802.3	$45 (CERAMIC DIP) $25.50 (PLASTIC DIP)	DEFAULTS TO 802.3; PROGRAMMABLE FOR OTHER FORMATS
	82501	ENCODER	802.3	$25	
	82588	CONTROLLER	802.3	$27.50 (CERAMIC DIP) $31.50 (PLCC)	1BASE5
MOTOROLA	MC68184	BROADBAND INTERFACE CONTROLLER	802.4	$35 (SAMPLES)	BACKBONE NETWORK
	MC68824	TOKEN-PASSING BUS CONTROLLER	802.4	$76	BROADBAND OR CARRIERBAND
NATIONAL SEMICONDUCTOR	DP8390	NETWORK INTERFACE CONTROLLER	802.3	$85 FOR 3-CHIP SET	MEDIA-ACCESS-CONTROL LAYER
	DP8391	SERIAL NETWORK INTERFACE	802.3		
	DP8392	COAXIAL TRANSCEIVER	802.3		INCLUDES COLLISION SENSING
SEEQ TECHNOLOGY	8003	DATA-LINK CONTROLLER	802.3	$48.85	
	8023	MANCHESTER-CODE CONVERTER	802.3	$44.95	
SIGNETICS	NE5080	FSK MODEM TRANSMITTER	802.4	$10	CARRIERBAND
	NE5081	FSK MODEM RECEIVER	802.4	$10	CARRIERBAND
TEXAS INSTRUMENTS	TMS38030	SYSTEM INTERFACE	802.5	$115 FOR ENTIRE CHIP SET	HOST INTERFACE
	TMS38010	16-BIT COMMUNICATION CPU	802.5		
	TMS38020	PROTOCOL HANDLER	802.5		MANCHESTER ENCODING AND CODE VIOLATION
	TMS38C51	RING INTERFACE CONTROLLER	802.5		INCLUDES WRITE-FAULT DETECTION
	TMS38052	RING INTERFACE TRANSCEIVER	802.5		DRIVERS, PHASE DETECTOR, FREQUENCY DETECTOR
THOMSON-MOSTEK	MK68590	CONTROLLER	802.3	$45	10BASE5
	MK68591	SERIAL INTERFACE ADAPTER	802.3	$17	10BASE5 (NMOS)
	MK68592	SERIAL INTERFACE ADAPTER	802.3	$12.50	10BASE5 (BIPOLAR)
	MK5030	CONTROLLER	802.3	$52 (2nd QTR '87)	1BASE5
	MK5032	CONTROLLER	802.3	$45 (3rd QTR '87)	ALL
	MK5033	MANCHESTER ENCODER	802.3	$14 (2nd QTR '87)	
	MK5034	MANCHESTER ENCODER	802.3	$15 (2nd QTR '87)	WITH INTEGRATED TRANSCEIVERS
	MK5035	MANCHESTER ENCODER	802.3	$13 (2nd QTR '87)	1BASE5
	MK5036	MANCHESTER ENCODER	802.3	$14 (2nd QTR '87)	SAME AS MK5035 WITH INTEGRATED TRANSCEIVERS
WESTERN DIGITAL	WD83C503	CONTROLLER	802.3	$15.50 (DIP)	STARLAN MINIHUB CONTROLLER
	WD83C510	CONTROLLER	802.3	$35	INCLUDES COLLISION DETECTION

*UNLESS OTHERWISE SPECIFIED.

A LAN's access method does not dictate the type of transceiver required for the LAN.



The simplicity of connection to the StarLAN network *is evident in this IBM PC StarLAN card, which incorporates Intel's 82588 controller. Note the pulse transformers at the top of the card; these devices provide the requisite isolation of collision, receive, and transmit signals.*

isolation diode (by contrast, a Thinnet system allows you to connect the transceiver directly to the coaxial cable).

Another CSMA/CD-based LAN, StarLAN, eases the requirements placed upon transceivers, both through its lower data rate—1M bps—and through its star topology. The latter unloads the collision-detection responsibility from the individual stations and places it with a hub controller. Chips like the Thomson-Mostek MK5030 hub controller perform this function. The hub controller accepts transmissions from stations on the network and retransmits them on all outgoing wire pairs. It detects collisions and transmits a collision-presence signal to the connected stations.

Medium raises new problems

Although the topology and the lower data rate of StarLAN ease some aspects of transceiver design, the transmission medium—unshielded twisted-pair wire—raises its own problems. The IEEE-802.3 standard allows transmitted signals to be ideal binary signals; that is, the rise and fall times associated with the signals may be effectively close to zero. Although textbook representations of these signals may be aesthetically pleasing, when the transceiver operates with these high-speed transitions, it supplies power to the higher-order harmonics of the basic signal. Increased power in these higher-order harmonics leads to problems with crosstalk and EMI. To minimize these unwanted features, you must limit the signals' rise and fall rates to the lowest rate your system will allow. The degree to which you can do so will depend upon the amount of jitter that stations in the LAN produce, and the specified error budget for your receiver.

If, for example, cumulative errors around your LAN create ±50 nsec of jitter at each transition, and you limit rise and fall times to 20 nsec, then the effective

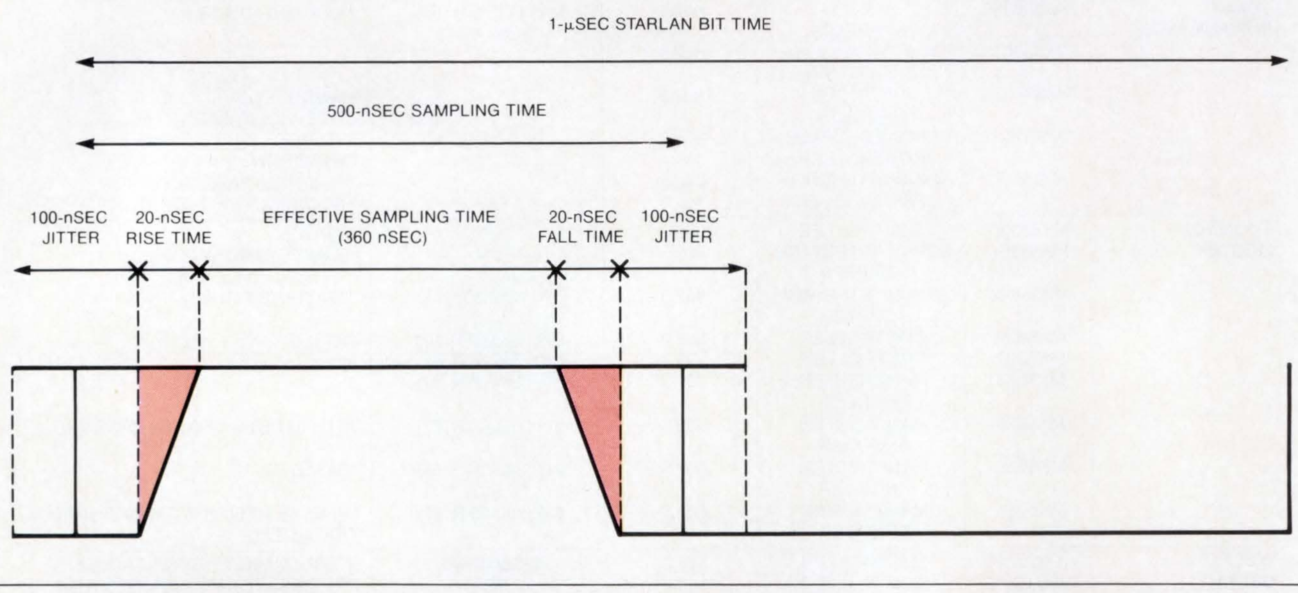


Fig 2—The effect of jitter and rise and fall times *on the effective sampling time available to LAN receivers is considerable. In this example, the effective sampling time is reduced by 28%. The 1-μsec bit time is consistent with a 1M-bps LAN, such as StarLAN.*

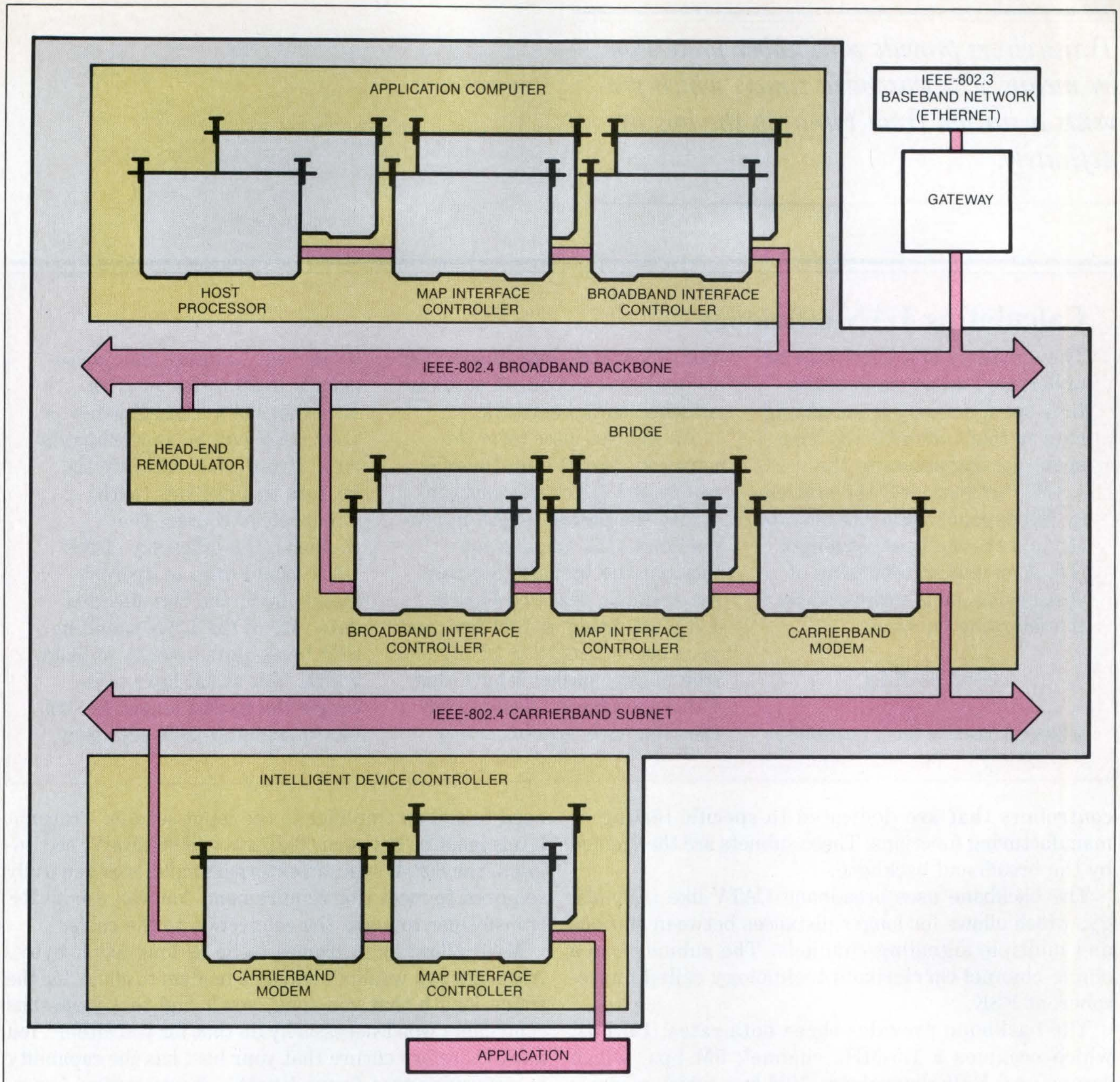


Fig 3—The hierarchical structure of MAP *specifies a broadband backbone network that can contain carrierband subnets dedicated to specific testing or manufacturing functions.*

sampling time available to your receivers for each bit falls from 500 nsec to 360 nsec (**Fig 2**). Furthermore, the receiver must sample the data at approximately 5 MHz. If you increase the rise and fall times, you'll have to increase the sample rate.

The CSMA/CD approach has two major disadvantages: Access is probabilistic—no station is guaranteed access to the bus upon each attempt—and the bus becomes less efficient under heavy load conditions. In real-time applications, probabilistic access is unacceptable. A station on the factory floor needs to have guaranteed access to the LAN if vital process-control information is to be transmitted in a timely fashion.

The principal effect of heavy loading is that, as more stations vie for the bus, the number of collisions, and the proportionate time spent dealing with collisions, increases. Network efficiency decreases in proportion. And you must not fall into the trap of thinking that you can just increase the bit rate of the LAN to make up for increased collision time (see **box,** "Calculating LAN efficiency").

A different approach to LANs—one that overcomes the difficulties associated with a probabilistic approach to LAN access and is therefore more suitable for real-time applications—is the token-bus approach. The MAP network, the leading example of this type of LAN, follows the IEEE-802.4 token-bus specification for the data-link and physical layers (layers 2 and 1). The MAP LAN architecture is a hierarchical structure that consists of a broadband backbone network linking "carrierband subnets" (**Fig 3**). The carrierband subnets provide low-cost networks to localized groups of

Transceivers provide antijabber protection by means of a watchdog timer, which prevents a station from tying up the bus indefinitely.

Calculating LAN efficiency

The efficiency of a LAN may be understood as the ratio of the time spent actually transmitting data to that time plus the time spent gaining access to the LAN. Furthermore, the efficiency (E) depends upon the bit rate (R) and the data-packet length (L). A simplified rendering of these relations is expressed by the following equation:

$$E=(1+RA/L)^{-1},$$

where A stands for a parameter that, for a given bus length, varies with the number of stations attached to the network.

As you can infer from the equation, to maintain the efficiency of a LAN, you must increase the packet length in proportion to the amount you increase the bit rate. Suppose, for example, that you have a LAN operating at 10M bps, and your packet length is 12,144 bits (the longest packet length that Ethernet allows). Assume further that A is approximately 9×10^{-5} sec (a figure that corresponds to 20 nodes on a 1m Ethernet bus). The efficiency of your LAN will be approximately 90%. If you could increase the bit rate to 100M bps (with Ethernet, of course, you couldn't), the efficiency of the LAN would drop to approximately 60%, and the effective data rate of the LAN would be 60M bps—quite a waste of bandwidth. You would have to increase the packet length to 120k bits to maintain 90% efficiency.

controllers that are dedicated to specific testing or manufacturing functions. These subnets are then joined by the broadband backbone.

The backbone uses broadband CATV-like technology, which allows for longer distances between stations and multiple signaling channels. The subnets use a single-channel carrierband technology called phase-coherent FSK.

The backbone provides three data rates: 1M bps, which occupies a 1.5-MHz channel; 5M bps, which occupies a 6-MHz channel; and 10M bps, which occupies a 12-MHz channel. The carrierband subnets provide data rates of 5M or 10M bps at signaling frequencies of 5 and 10 MHz or 10 and 20 MHz, respectively.

Your MAP transceivers are RF modems

RF modems are the transceivers for MAP systems. Carrierband and broadband modem ICs connect to the MAP cable on one side and to the token-bus controller on the other. The modem IC modulates data from a serial interface and transmits this signal onto the network cable. It also receives signals from the network, demodulates the information, and passes it on to the token-bus controller. Your modem IC should also include an antijabber function and loop-back tests.

At the cable interface, the IEEE 802.4 spec requires a minimum receiver sensitivity of 10 dBmV for both 5M- and 10M-bps data. If the receiver section of your modem chip meets these requirements, you may connect it directly to the coaxial cable; otherwise, you will need to add an amplifier to the input section. Transmit levels must be between 63 dBmV and 66 dBmV, according to the 802.4. spec; an external amplifier is generally required to meet this requirement. You can use an RF transformer to make the connection to the cable.

MAP allows data frames to be as long as 8k bytes. Although you wouldn't expect a modem to check for the frame length that you send, you'll find that token-bus controllers won't necessarily do that for you either. You must therefore ensure that your host has the capability to determine that frame lengths, frame-control bytes, the destination address, and the source address are correct as sent.

As with any design that uses high-frequency signals, you must be extremely careful with the layout of your modem card. All RF-carrying leads must be as short as possible, and a pc board with a good ground plane, both top and bottom, is recommended. The RF sections of your modem card may require separate EMI shielding as well.

Another access method that skirts the difficulties associated with CSMA/CD, and does so without the use of RF modems, is the token-ring approach delineated by IEEE 802.5. In a ring topology, all transmissions are point to point, which means that you can match the termination impedance of the medium very tightly, eliminating most reflections. In addition, each node is a regenerative repeater, thus easing timing constraints. Another advantage is the ease with which you can integrate fiber optics into the ring topology (the lack of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In the case of an Ethernet system, you build your transceiver in a separate module and isolate it from the Ethernet station.

Manufacturers of IEEE-802 LAN ICs

For more information on IEEE-802 LAN ICs, contact the following manufacturers directly or circle the appropriate number on the Information Retrieval Service card.

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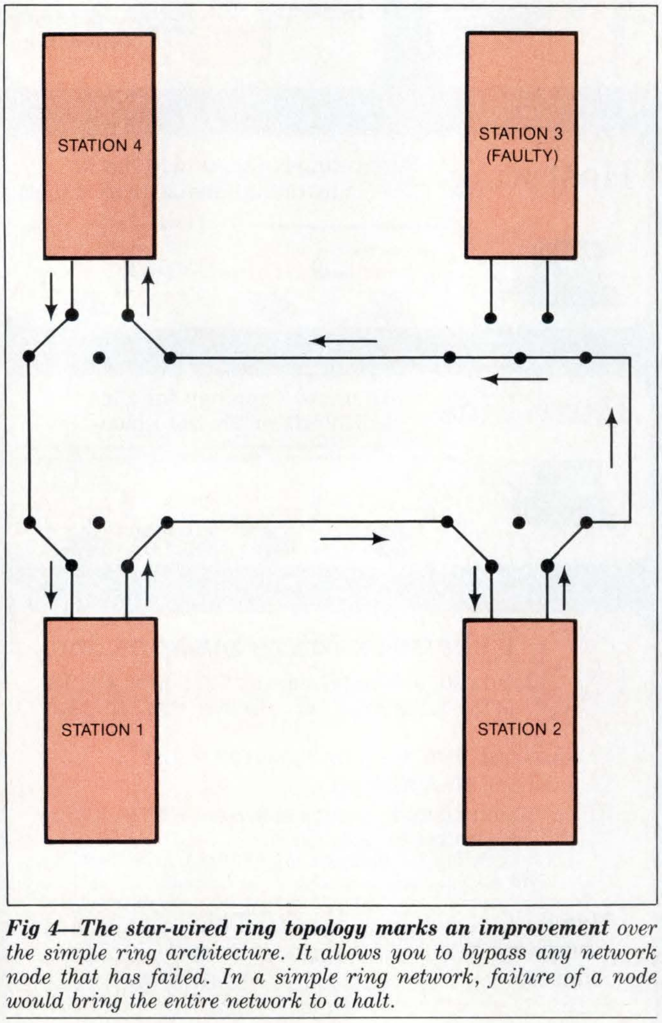

Fig 4—The star-wired ring topology marks an improvement *over the simple ring architecture. It allows you to bypass any network node that has failed. In a simple ring network, failure of a node would bring the entire network to a halt.*

low-cost taps precludes the use of fiber optics in a bus topology).

The ring configuration has one major reliability concern: What do you do when a node fails? In a simple ring configuration, a single node failure can bring down the entire network. In a variant of the basic ring, known as the star-wired ring **(Fig 4)**, the offending station is simply switched out of the network, and operation of the network continues unimpaired.

The token-ring protocol prescribes differential Manchester encoding for the ring-signaling format. This coding scheme always injects a signal transition at the center of a bit time; a zero bit has a transition at the beginning of a bit time, while a one does not. Besides incorporating clock information in the data stream, this format assures an average signal level of 0V dc. This signal level, in turn, prevents saturation of the transformer that couples the transceiver to the ring.

In the token-bus network, the transceiver must transform a TTL-level, Manchester-encoded signal into a differential current that's compatible with a twisted-pair transmission line with a characteristic impedance of 150Ω. (The IEEE-802.5 standard specifies twisted-pair wire as the transmission medium.) The receiver section provides functions for equalization, signal shaping, and retiming of the received signal.

You can see the importance of the retiming function from the fact that any adapter on the ring may be designated as the active monitor. The active monitor provides the master clock for the ring. As a packet travels around the ring, phase delays in the repeating stations can accumulate. When the packet returns to

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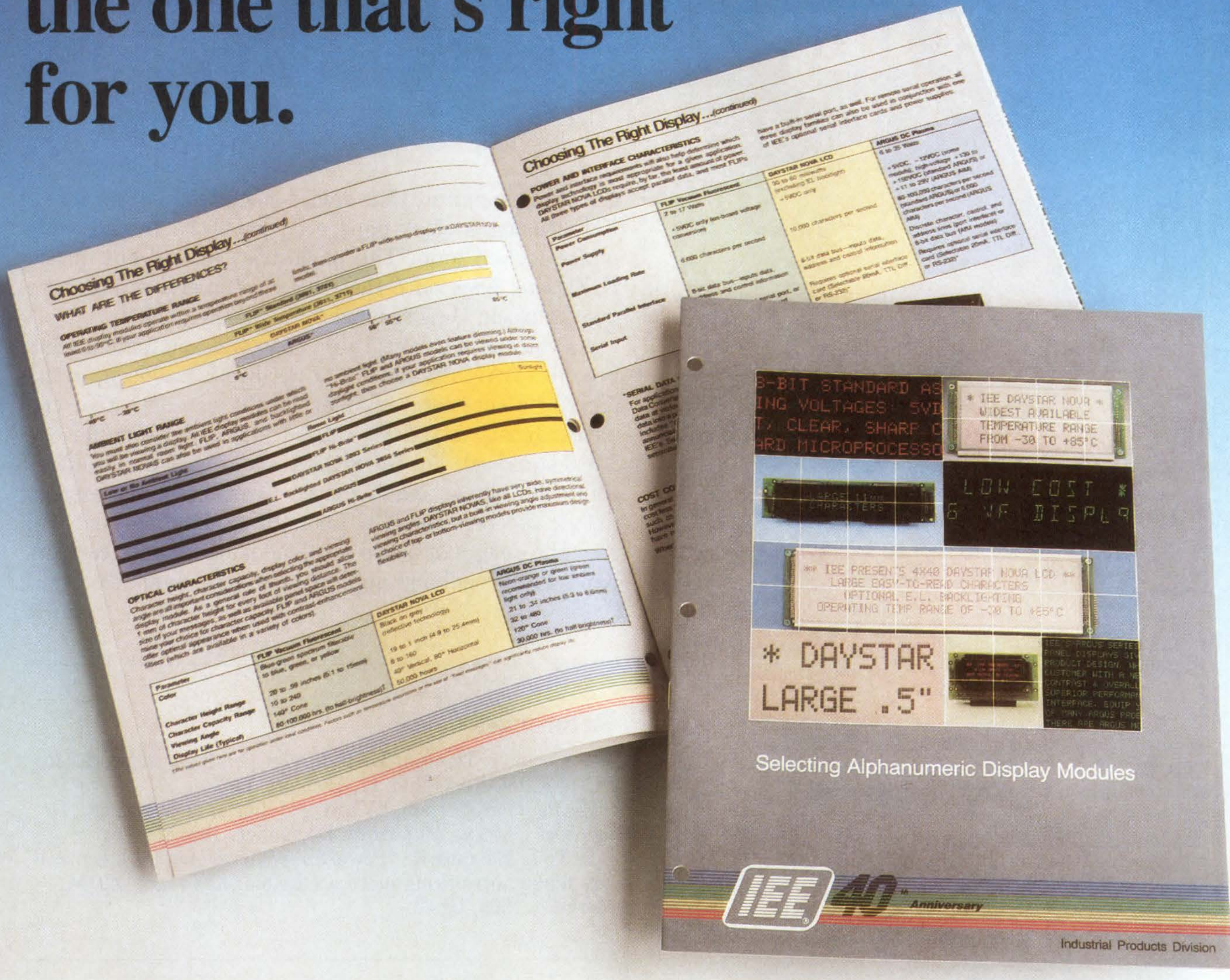

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For Immediate Application, Circle no 33. For Reference Material, Circle no 72 the active monitor, that device clocks the packet into a FIFO using a clock generated from the transceiver's phase-locked loop. The packet is clocked out of the FIFO and back onto the ring via the active monitor's master clock, thus resynchronizing the packet.

As you can see from **Table 1,** only Texas Instruments provides LAN ICs for the IEEE-802.5 standard, in the form of a complete chip set. You'll also note that the vast majority of today's LAN ICs are designed for the 802.3 standard. For the 802.4 standard, Motorola offers controller chips, and Signetics provides modem transmitter and receiver ICs. Look for modem ICs that will ease the design of board-level modems for both carrierband and broadband applications to be available soon.

EDN

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2. Coleman, Vernon, "VLSI and digital networking," *Integrated Circuits Magazine*, December, 1984, pg 36.
3. Teja, Edward R, "Powerful local-area-network controllers make networking more accessible than ever," *EDN*, March 3, 1983, pg 61.

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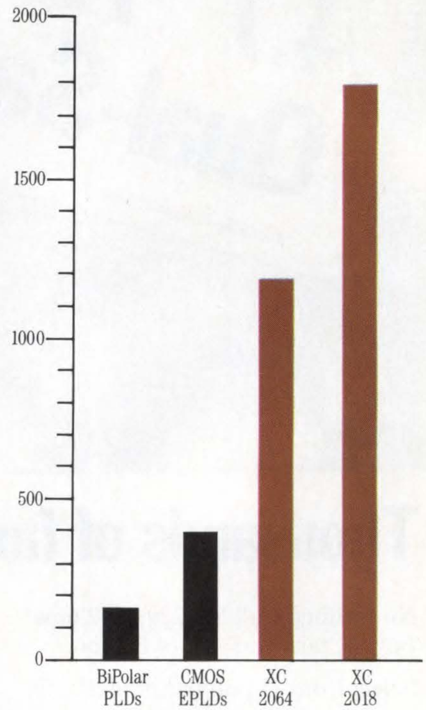

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Speed	250 ns, 300 ns, 350 ns	250 ns, 300 ns, 350 ns	200 ns, 250 ns, 300 ns	200 ns, 250 ns, 300 ns	200 ns, 250 ns, 300 ns	200 ns, 250 ns, 300 ns
Endurance	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles
End of Write Scheme		RDY/$\overline{\text{BSY}}$	$\overline{\text{Data}}$ Polling	$\overline{\text{Data}}$ Polling	RDY/$\overline{\text{BSY}}$, $\overline{\text{Data}}$ Polling	RDY/$\overline{\text{BSY}}$, $\overline{\text{Data}}$ Polling
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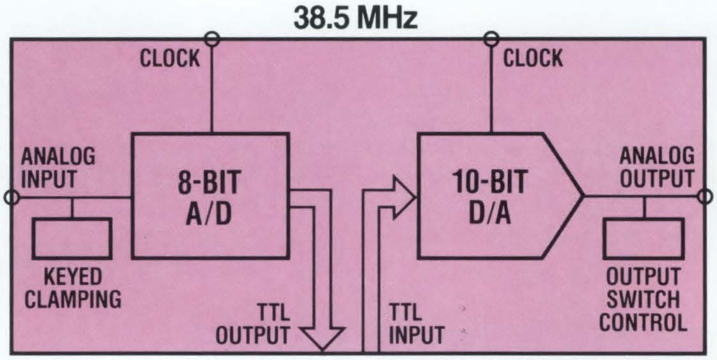

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Magnetic compensation gives new life to transformer-based SLICs

The transformerless monolithic SLICs that are becoming available are not yet proving to be cost-effective. A family of magnetic-compensation circuits offers an interim solution that can help reduce the size and cost of the transformer in a magnetic SLIC while preserving all of the advantages of a transformer-based design.

Chris Stacey, *National Semiconductor Corp*

Although IC designers have successfully implemented voice-processing and switching functions on digital subscriber-line and trunk cards in VLSI, the subscriber-line interface circuit (SLIC) continues to present a challenge. Current monolithic SLICs are expensive and somewhat inflexible devices because of their large die sizes and the demands of high-voltage processing. Acceptable solutions for the comparatively simple requirements that PABX lines impose upon SLICs have appeared, but central-office and trunk lines have more demanding specifications in a number of critical areas.

One problem that has proved troublesome for SLICs—and in particular monolithic SLICs—is that of maintaining good longitudinal balance when there is current induced into the subscriber's twisted-pair wiring by adjacent power cables, which may be comparable to the dc loop current. Other problems attend the reliability of the ring-tripping circuitry and of the device itself under overvoltage conditions. It's still the case, then, that a magnetics-based SLIC offers the most cost-effective and reliable solution for many phone-line applications.

Use of the TP3200 family of magnetic-compensation circuits, also known as SLIC-MCs **(Fig 1)**, can help you trim both the size and the cost of the transformer in your SLIC design while retaining all of the transformer's advantages. The SLIC-MC cancels the dc flux set up by the loop current in the transformer core by forcing a proportional current in the opposite direction through a cancellation winding. When this task is accomplished with a high degree of accuracy, the net dc magnetizing flux can be reduced to zero, and this result in turn allows you to wind the transformer on a small pot core without an air gap. (For a discussion of the magnetic-compensation principle, see **box,** "How SLICs employ magnetic compensation.")

In the TP3200 circuits, a differential amplifier and a network of 200-kΩ resistors, which form a bridge across the external loop current feed resistors, sense the loop current. The sense bridge employs on-chip precision Si-chrome resistors to ensure at least 60 dB of longitudinal balance. Si-chrome, a thin-film technique in which resistors are deposited over the thermal oxide of the device prior to passivation, is far superior to diffused or

A magnetics-based SLIC still offers the most cost-effective and reliable solution for many applications, including line, trunk, and special service interfaces.

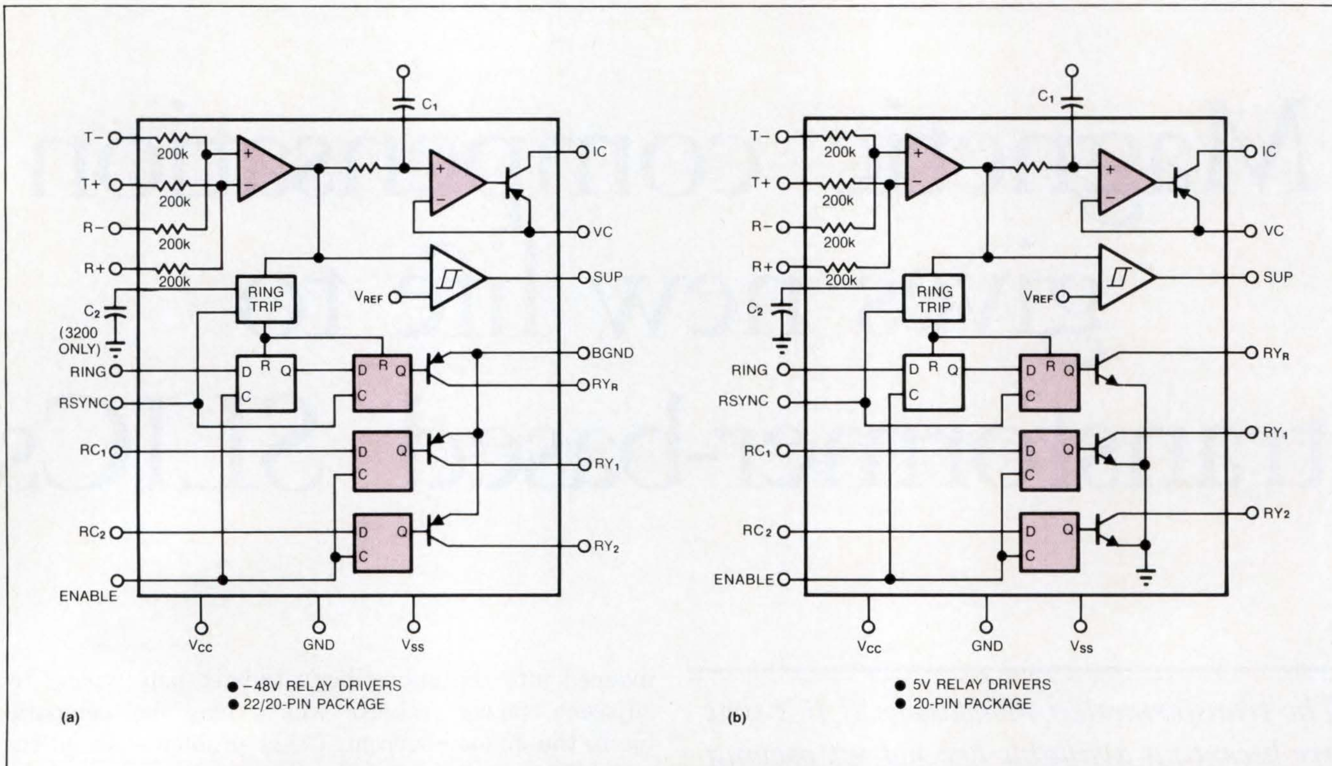

Fig 1—These magnetic-compensation circuits, *the TP3200/3202* ***(a)*** *and the TP3204* ***(b)*** *include a differential amplifier for sensing the magnitude of the loop current and a current source to drive the cancellation winding. The ICs also include three latched relay drivers—two general-purpose devices and one designed specifically as the ringing relay.*

polysilicon resistors with respect to matching tolerance and to breakdown voltage. Completing the flux-canceling part of the circuit is a high-compliance current source, which drives the cancellation winding. A single external resistor sets the gain of the cancellation path, providing you with full flexibility in designing the transformer to optimize the ratio of the number of turns on the cancellation winding to the number of primary turns. Ratios as high as 5:1 are practical.

Also in the device is a comparator that compares the loop current with an internal voltage reference to provide hook-switch detection via a supervision (SUP) output. In the presence of dial pulses, the comparator will provide a rectangular-wave replication at the SUP output.

Because the feed resistors and the transformer buffer the TP3200 itself from the line, the device is not directly subject to severe overvoltage conditions. In fact, the device needs only +5 and −5V power supplies, and it's fabricated with a standard 70V bipolar process that requires no expensive dielectric isolation. These factors help keep design and fabrication costs low.

Along with the magnetic-compensation circuit, TP3200 Series devices also include three relay drivers each (the transistors associated with pins RY_R, RY_1, and RY_2), and each driver has a latched output. A common Enable input strobes the latches, thereby allowing you to multiplex the latched inputs of a number of SLIC-MCs without resorting to I/O expanders or decoders. Two of the relay drivers are general-purpose outputs, suitable for a test relay and a battery-reversal relay (pins RY_1 and RY_2; see **Fig 2** for an example). The third driver is designed specifically for the ringing relay (pin RY_R). Following this latch is a flip-flop clocked by a Ring Sync input pulse, ensuring that the ring relay only makes and breaks coincidentally with a zero-crossing of the ringing voltage. This zero-crossing operation prevents arcing, which would wear down the relay contacts. The TP3200 and TP3202 have pnp drivers for use with −48V relays. The TP3204 employs npn drivers for use with +5V relays.

The SLIC-MC offers a choice of two methods for tripping the ringing signal upon answer—a fully automatic method, and a µP-assisted procedure. Ring-tripping requires that the circuit reliably distinguish between the 16- to 20-Hz ringing current in the loop and the direct current drawn as soon as the receiving telephone goes off-hook. Factors such as the number and type of ringers connected to the line (for example, bell or electronic ringers), the cable length and impedance, and the cable leakage all combine to produce considerable variations in the waveform of the ringing current. A reliable ring-tripping circuit must not be fooled into falsely tripping before the phone goes off-hook, nor must it fail to trip when it does go off-hook (the latter event produces a deafening sound level in the receiver).

In the automatic method of ring-tripping, the SLIC-

How SLICs employ magnetic compensation

One of the few limitations of the humble transformer is the degradation of performance that results from direct current passing through any one of its windings. The constant magnetic flux set up in the core introduces an offset in the B-H characteristic, thereby limiting the degree of alternating flux the core can handle before reaching saturation. Once the core is saturated, ac signals become distorted.

Conventional dc feed circuits in a subscriber-line interface are designed to provide at least 20 mA of current on a long loop, rising to about 100 mA on a very short loop. This current is normally fed through a split transformer winding **(Fig A).** To carry these high dc levels without saturation, the transformer core usually employs magnetic-alloy laminates. You may also use ferrite cores, but these cores require a large air gap between the core pieces, thus reducing the inductance per turn. In any case, a primary inductance in the 1.5 to 2.5H range is necessary to meet return loss and frequency-response specifications in a typical 900Ω circuit, thus making the final transformer size larger than is desirable. What is needed is a method that will enable the transformer to be wound on a small pot core without an air gap.

Fortunately, a simple technique—magnetic compensation—cancels the dc component of the magnetic flux set up by the loop current. The following equation determines the core's flux density:

$$B = I \times N \times \mu / A$$

where N is the number of turns, μ stands for permeability, and A represents the effective core area.

Consequently, for any given core where μ/A is a constant, you can cancel the flux by forcing a current with an equal ampere-turns product through an auxiliary winding in a direction opposite to that of the loop current.

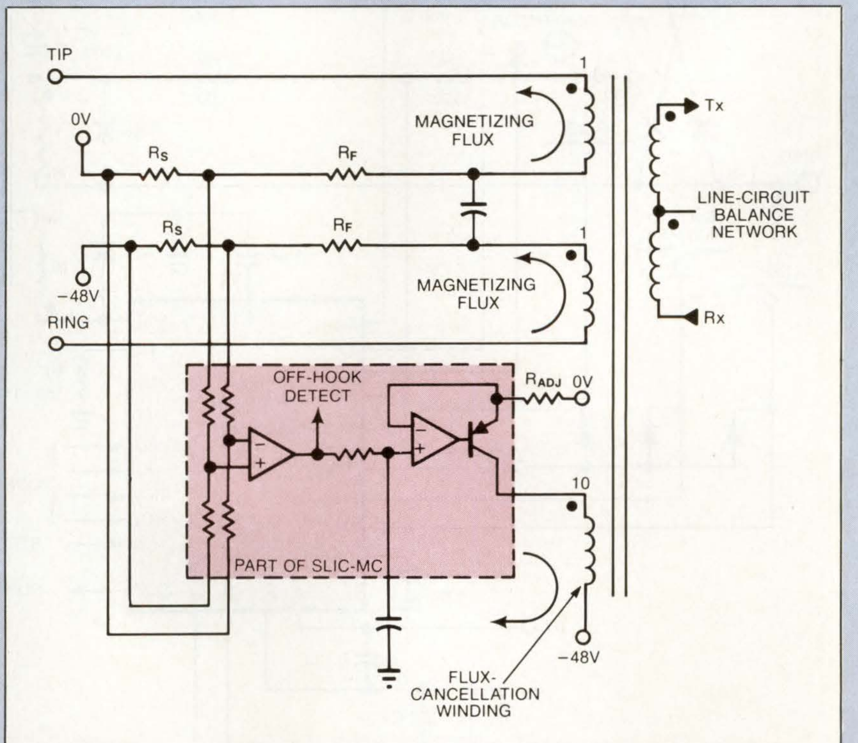

Fig A—Magnetic-compensation circuitry measures the loop current *by sensing the voltage across two matched battery-feed resistors (R_S). Circuitry in the SLIC-MC amplifies this voltage and uses it to drive a flux-cancellation winding. With proper selection of R_{ADJ} and transformer-winding ratios, the current in the cancellation winding exactly cancels the flux produced by the dc component in the loop current.*

A magnetics-based SLIC cancels the dc flux set up by the loop current in the transformer core by forcing a proportional current in the opposite direction.

MCs use only one small, loose-tolerance capacitor (C_2) rather than a sharp lowpass filter, which would require several cumbersome off-chip capacitors. During ringing, on each positive half-cycle of the sensed line signal a fixed current charges C_2. The current then discharges during the negative half-cycle. At the end of each ring cycle, a strobed comparator (not shown) checks to see if there is any residual voltage charge on C_2. If the loop current contains no dc component, the positive and negative half-cycles are approximately equal in duration; consequently, C_2 has no residual voltage at the end of the cycle, and the ring relay stays set. As soon as a direct loop current exceeding about 14 mA is drawn during ringing, the sensed ringing current signal becomes offset, resulting in a residual voltage on C_2 at the end of the full ring cycle. This sensed residual voltage automatically resets both latches and the ringing relay on the next Ring Sync input pulse.

The other ring-tripping method takes advantage of a line-card μP to sense the state of the supervision (SUP) output during ringing. This signal is essentially a rectangular wave that, by careful choice of internal voltage thresholds, is designed to have a duty cycle greater than 50% (logic-one duration) during on-hook

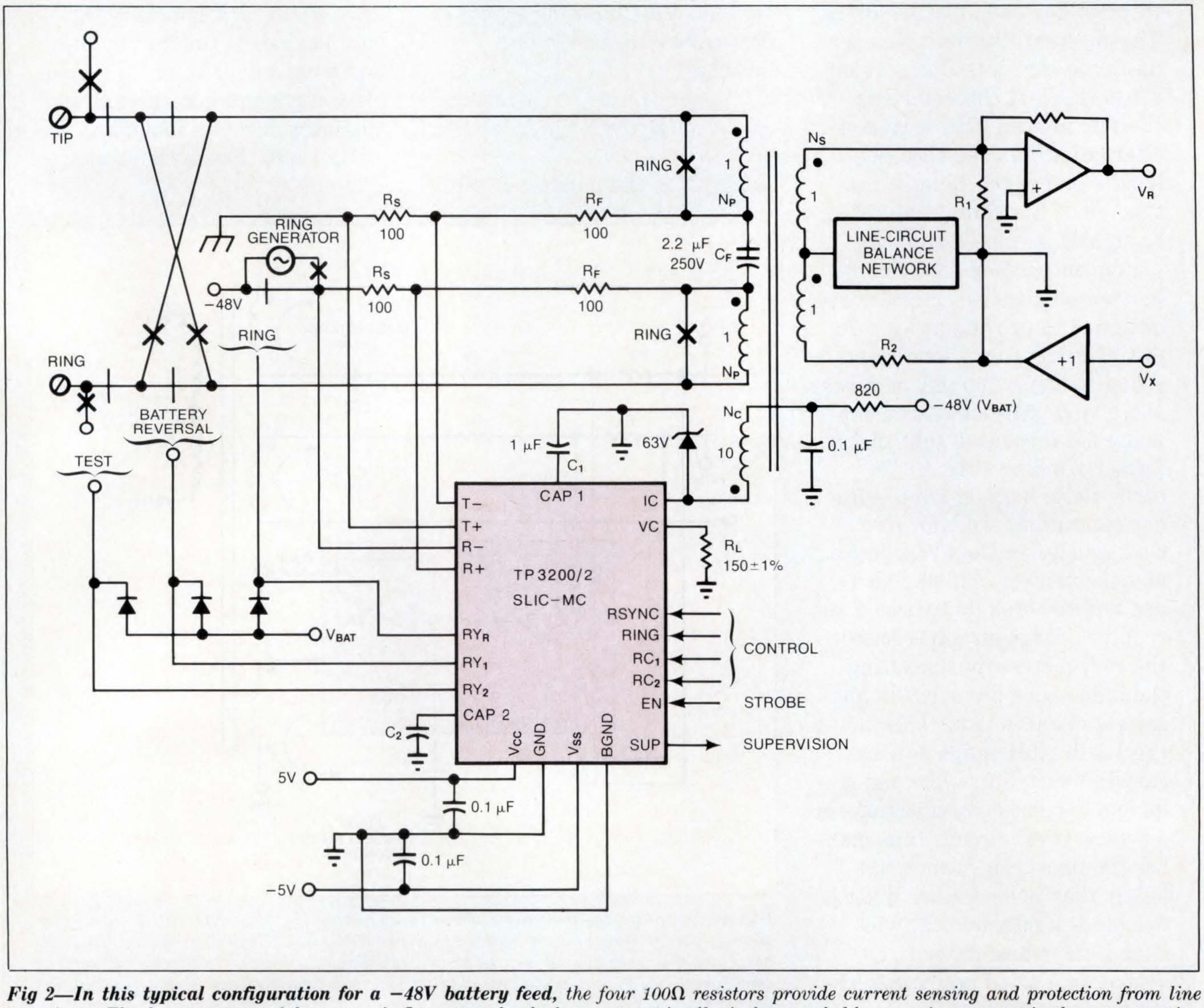

Fig 2—In this typical configuration for a −48V battery feed, the four 100Ω resistors provide current sensing and protection from line transients. The dc component of the magnetic flux set up by the loop current is effectively canceled by opposing current in the compensation winding.

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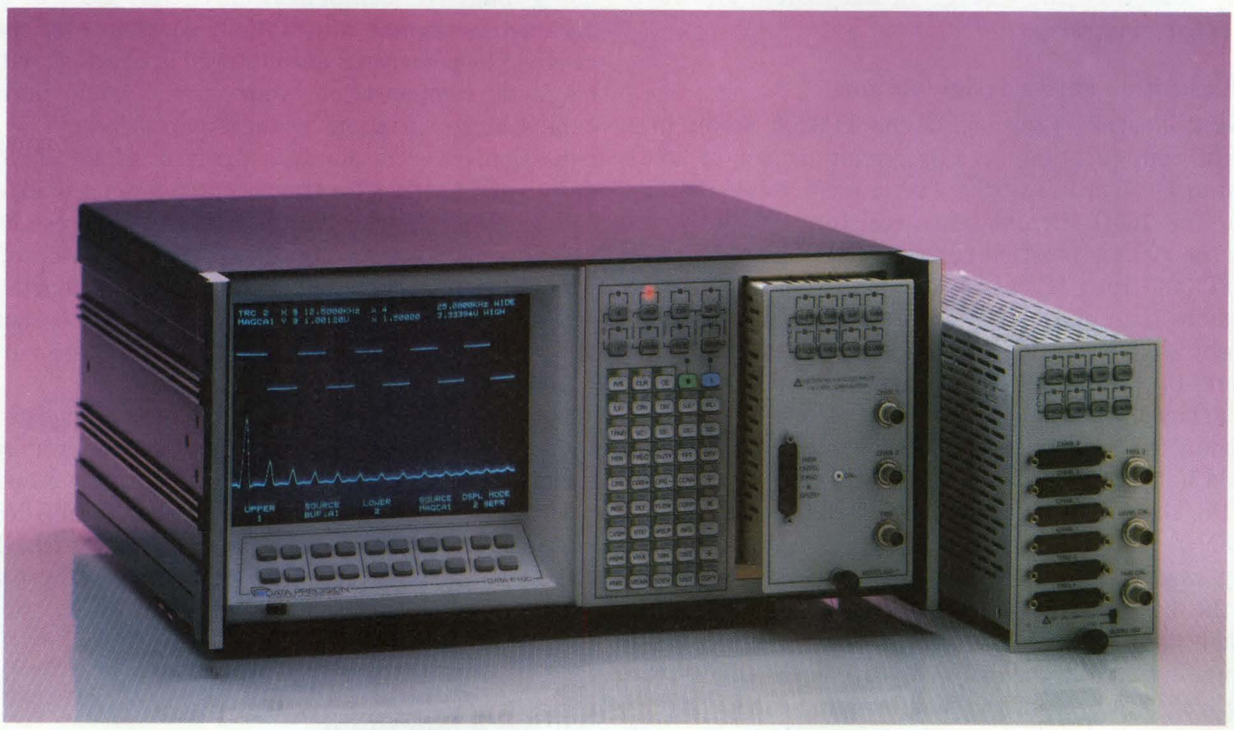

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The SLIC-MC offers a choice of two methods for tripping the ringing signal upon answer—a fully automatic method, and a μP-assisted procedure.

ringing. A change to off-hook ringing forces the duty cycle to shift to less than 50%. By sensing the supervision output at approximately 1-msec intervals, the μP easily computes the change in duty cycle and then resets the ring relay.

Configuration shows design options

Fig 2 illustrates the use of the TP3200 Series in a specific configuration. In this circuit, a pair of 200Ω resistances (R_S+R_F) works with a fixed −48V battery feed. The 100Ω current-sense resistors (R_S) in series with the 100Ω protection resistors (R_F) ensure that the Tip (T) and Ring (R) sense inputs of the device never see more than one half of any line-transient voltages, thereby simplifying the sensing requirements. The two general-purpose relay drivers operate a line-test relay and a battery-reversal relay. The ac line-termination impedance is determined by resistors R_1 and R_2 (which should be equal to balance the hybrid circuit properly) and the square of the turns ratio of the transformer—$(2N_P/N_S)^2$.

You insert the ring voltage into the circuit by breaking the battery-feed path and superimposing the ac voltage upon the battery voltage (shown in **Fig 2** for ringing inserted in the more negative lead—that is, the Ring lead). To prevent the feed-bridging capacitor (C_F) from shunting the ringing current, you place a "break" contact in series with C_F. To prevent the line transformer's primary windings from attenuating the ring voltage or introducing distortion, you connect "make" contacts in parallel with the transformer's primary windings. Doing so ensures minimum shunt-path loss of the ringing current.

(Ed Note: Phone company conventions for drawing schematics call for a bold "X" for a make contact and a short bar for a break contact. You can see the break contacts in ***Fig 2*** *above C_F, along the Tip and Ring leads, and in parallel with the ring-generator circuitry near the −48V feed.)*

Long live the transformer

The design of the transformer itself is somewhat of a black art, influenced by several interacting parameters:

- Low-frequency 2-wire return loss, dominated by the minimum inductance of the primary winding
- Worst-case loop-current compensation error, determined by the ampere-turn capacity before magnetic saturation of the core
- 4-wire path insertion loss, preferably limited to about 1 dB.

You must also carefully consider other factors in the construction of the transformer, including longitudinal balance and heat dissipation. A major advantage of using magnetic compensation is that most of these parameters become substantially constant over the full range of loop currents encountered in practice; without magnetic compensation, your circuit would normally exhibit large variations in these parameters. The compensation error is partly a function of the TP3200's design and partly a function of the tolerance of external components. The excellent properties of the Si-chrome resistors, along with careful control of device offsets and other tolerances, limit the typical compensation error to ±2 mA. A variety of ferrite core types, such as RM8-T35, can handle the full range of line current without saturation.

No doubt monolithic SLICs will one day emerge with the right set of cost, size, and function compromises to offer attractive alternatives to transformer-based devices, even in central-office applications. While designers continue to grapple with the problem, the SLIC-MC offers an interim solution. At least for now, there's still life in the old transformer. **EDN**

Author's biography

Chris Stacey is the telecomm applications manager at National Semiconductor Corp (Santa Clara, CA). Before joining the company he worked for Plessey Communications in England, from 1969 to 1978, as a design engineer for PCM channel banks, multiplexers, and digital line transmission systems. He has a BSEE from the University of Southampton and an MSEE in telecommunications technology from the University of Aston, both in the United Kingdom. Chris is married and has two children.

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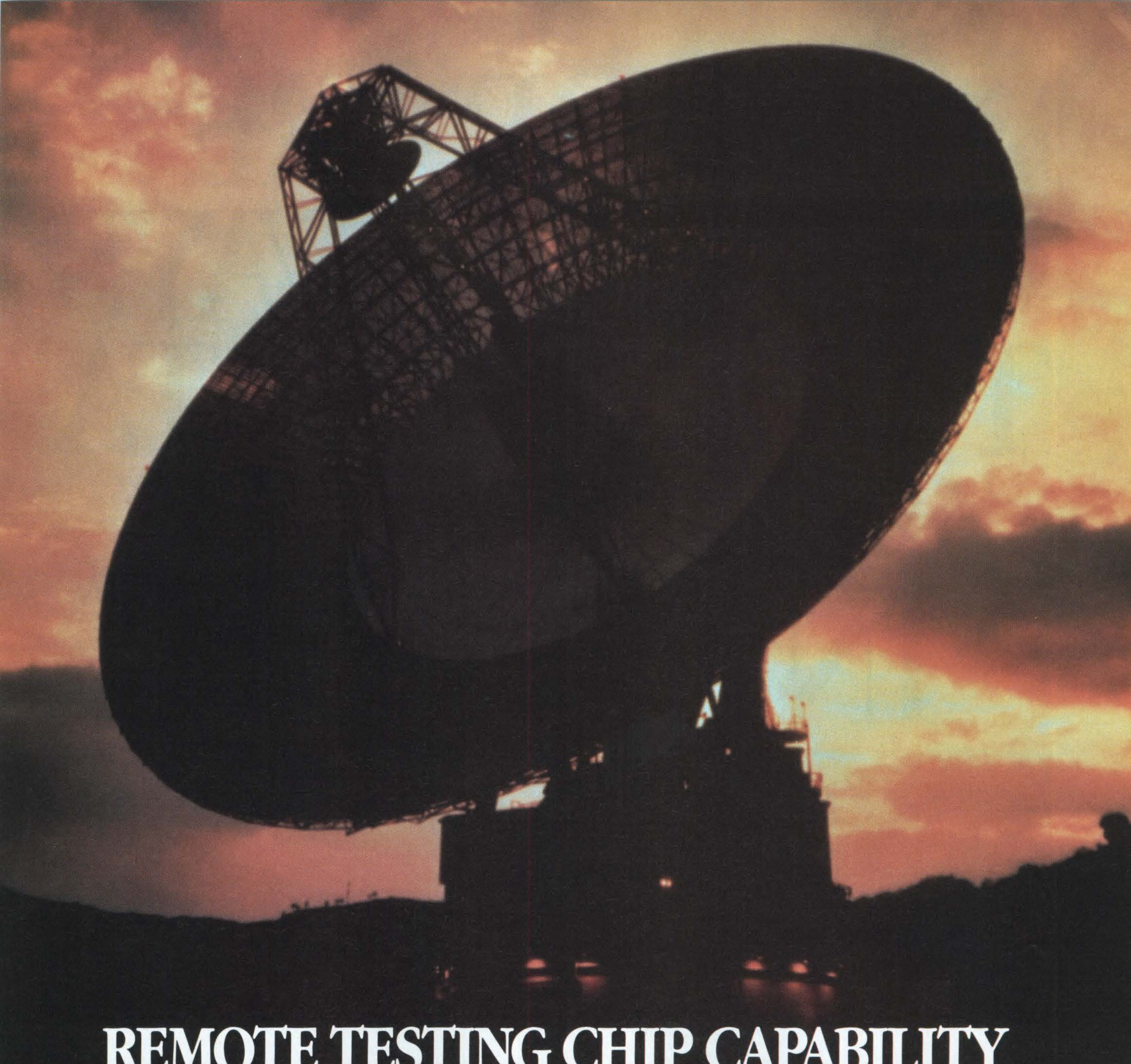

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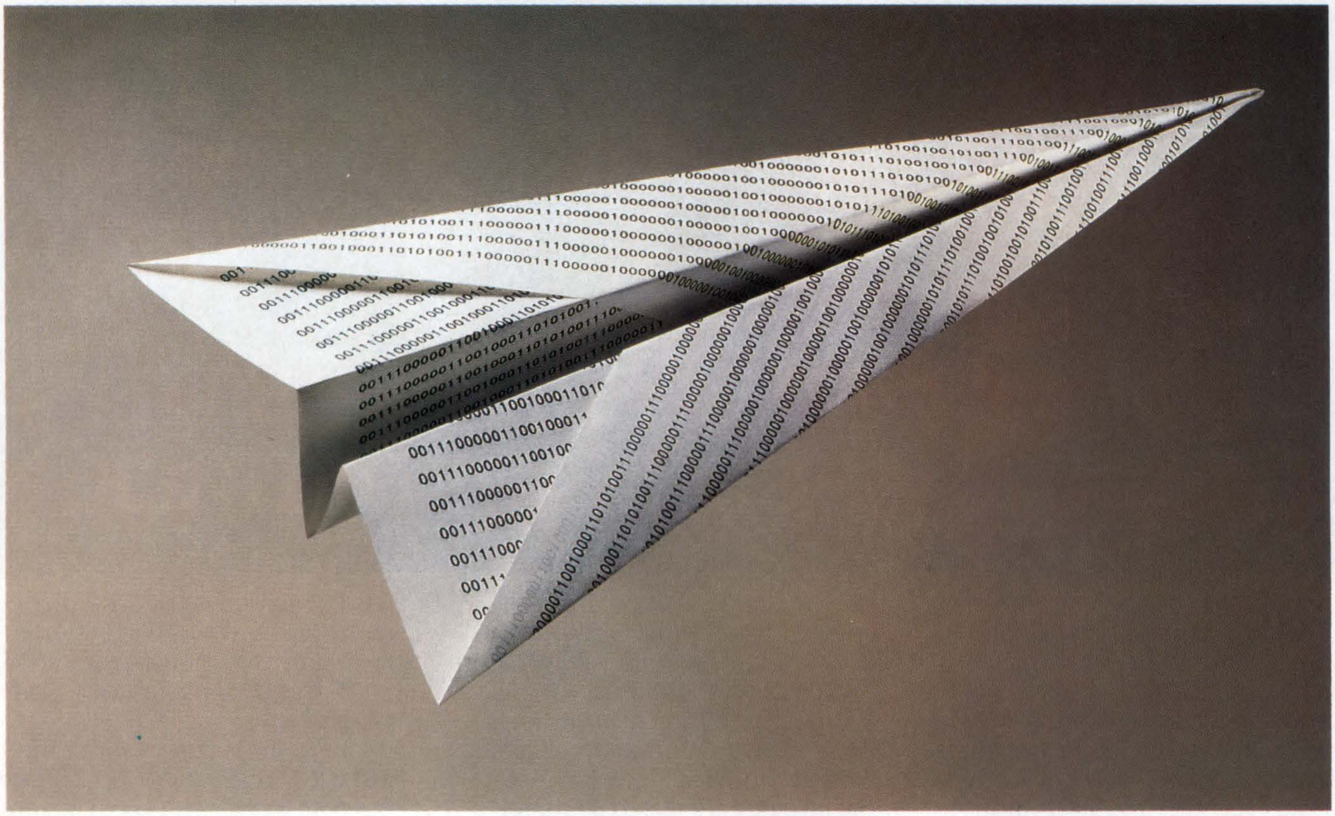

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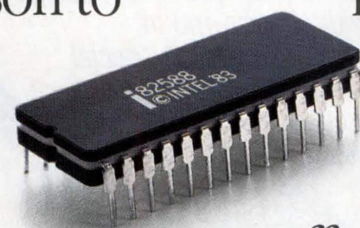

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Token-ring bus controller simplifies network design

You can simplify the design of factory-automation networks with the aid of a VLSI token-ring bus controller that conforms to IEEE Standard 802.4. Because it handles the details of communication over the network, this intelligent controller allows you to simplify the network-control software you must write.

Ivan Erickson, *Motorola Inc*

By employing a single digital communications network to control all the automatic manufacturing equipment in a factory—instead of connecting machines via point-to-point links—a manufacturer can lower the cost of equipment installation and increase the speed of its manufacturing operations. To configure such a communications network, you need to use a standard bus architecture for all the transmission equipment and communications software on the network. You can simplify the configuration of such a network by basing your design on an intelligent, VLSI token-ring bus controller that conforms to IEEE Standard 802.4.

A number of manufacturers have already adopted the IEEE Standard 802.4 token-ring bus architecture as the standard for communication over such networks. This standard is part of a collection of standards for factory-automation networks known as the General Motors Manufacturing Automated Protocol (MAP). The MAP generally follows the OSI (Open Systems Interconnection) scheme promulgated by the International Standards Organization.

IEEE Standard 802.4 defines both the physical layer and the media access-control (MAC) sublayer of the OSI. The physical layer defines the protocol for establishing and maintaining a connection; the MAC sublayer defines the protocol by means of which a node on the network gains access to the network and transfers data to another node.

Stations take turns starting communications

A token bus network can consist of any number of nodes connected to a common bus. **Fig 1** is a simple representation of a token bus network. In this example, stations A, B, C, and D form a logical ring; the other stations connected to the bus (E and F) can receive, but not initiate, communications. Control of the bus is

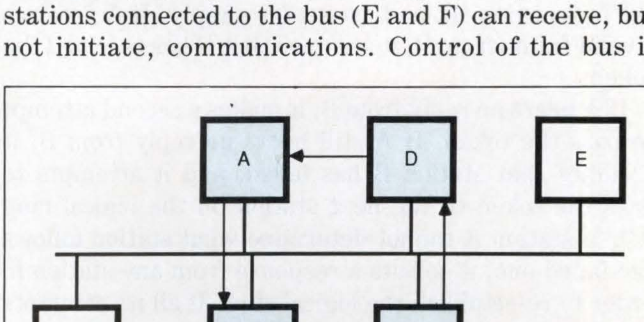

***Fig 1—Stations forming a logical ring pass a token** around the ring. Stations that are not in the logical ring can receive broadcast messages but cannot initiate communications.*

On a token bus network, only the station holding the token can initiate communications.

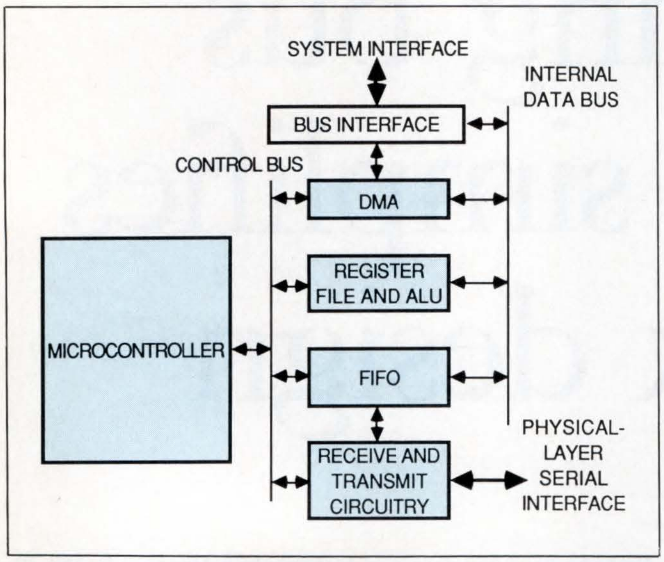

Fig 2—The TBC microcontroller manages the 40-byte FIFO buffer, *the register file and ALU, the receive and transmit circuitry, and the DMA logic.*

determined by a token that allows one node on the logical ring to initiate communication with another. The token is passed from node A to node B to node C to node D, and then back to node A. Stations that are logically next to each other on the logical ring (for example, B and C) do not need to be physically adjacent on the cable. Each station has a timer that governs the maximum time for which that station may retain control of the bus.

When a station (A, for example) has completed a task, such as the transmission of data frames or the performance of maintenance functions, or when its timer expires, it passes the token to the next station in the logical ring (B) and listens for a reply. If A receives a valid frame from B, it assumes that B has received the token.

If A hears no reply from B, it makes a second attempt to pass the token. If A still hears no reply from B, it assumes that station B has failed, and it attempts to pass the token to the next station on the logical ring (C). If station A cannot determine what station follows the failed one, it solicits a response from any station in order to re-establish the logical ring. If all its attempts fail, station A assumes that either its own receiver or the cable has failed, and station A then goes into a passive mode.

The station that holds the token periodically polls stations that are not part of the logical ring to see if any station wishes to join the logical ring. If the sending station, A, receives a valid reply from, say, station E, station A patches station E into the logical ring by making E (instead of B) its logical successor on the logical ring.

VLSI chip provides simple bus interface

Interfacing a host computer to a token bus is relatively simple if you base your design on an intelligent VLSI token bus controller (TBC) IC that can perform all the functions required by the MAC sublayer of the OSI. Several such TBCs are available; Motorola's HCMOS MC68824 is an example. This microprogrammed TBC (**Fig 2**) has a 32-bit address bus, can handle four priority levels, and has built-in diagnostics to check both the serial interface and system operation. The TBC can also gather network statistics that will aid the designer in finding trouble spots in the network.

The MC68824 TBC can pass or accept pointers to buffer areas, data, and parameters contained in the host's memory. The DMA channel can then transfer the appropriate data, without any intervention by the host, at the highest rate that the host's bus and memory can support. Because the TBC handles the details of verifying that its associated modem is operating correctly, you can control communication over the network merely by passing simple instructions to the TBC; you don't need to write complex software to pass data to the modem character by character.

The receive and transmit circuitry of the MC68824 TBC communicates with the physical layer via an interface specified by IEEE Standard 802.4G. This standard lets the circuitry interface to any type of physical layer, whereas IEEE Standard 802.4 requires either broadband or carrierband physical layers (see **box,** "Broadband vs carrierband media").

The TBC communicates with a host by means of a shared memory area that's resident in the host. As **Fig 3** illustrates, the TBC uses five different memory structures, all resident in the shared area: an initialization table, the TBC private area, a pool of free frame descriptors, a pool of free buffer descriptors, and a pool of data buffers.

The initialization table contains the pointer to the TBC's private area, as well as initial pointers to the priority queues, transmit queues, receive queues, target rotation time, statistics, and other parameters. The initialization table also contains the command parameter area, through which the host and the TBC pass parameters to each other.

The TBC private area is 256 bytes long; it acts as a

Broadband vs carrierband media

In selecting a transmission medium for use in an IEEE 802.4 token-ring network, you'll need to take into account both the layout of the network and your budget. At present, the standard gives you only two options: broadband or carrierband media.

If you use broadband media, you'll need only two frequencies for the data channels, so you can use the remaining portion of the cable's bandwidth for other networks or for video applications. However, broadband media operate at higher frequencies, and have tighter filtering requirements, than do carrierband media; broadband media are therefore more complex. Further, both broadband cable and broadband modems tend to be more expensive than their carrierband counterparts.

A single carrierband network uses the entire bandwidth of the cable, and all its nodes transmit and receive at the same frequency. However, although they are simpler than broadband networks, carrierband networks can operate only over a limited distance. **Table A** summarizes the advantages and disadvantages of the two media.

Because you'll probably want to carry other signals, such as TV signals, over your factory's backbone cable, you'll probably select broadband media for the backbone cable. As **Fig A** illustrates, you can then use gateway and bridge nodes to attach narrower-bandwidth carrierband subnetworks, including 802.4 subnets, wide-area networks, and proprietary subnets that don't conform to IEEE 802.4.

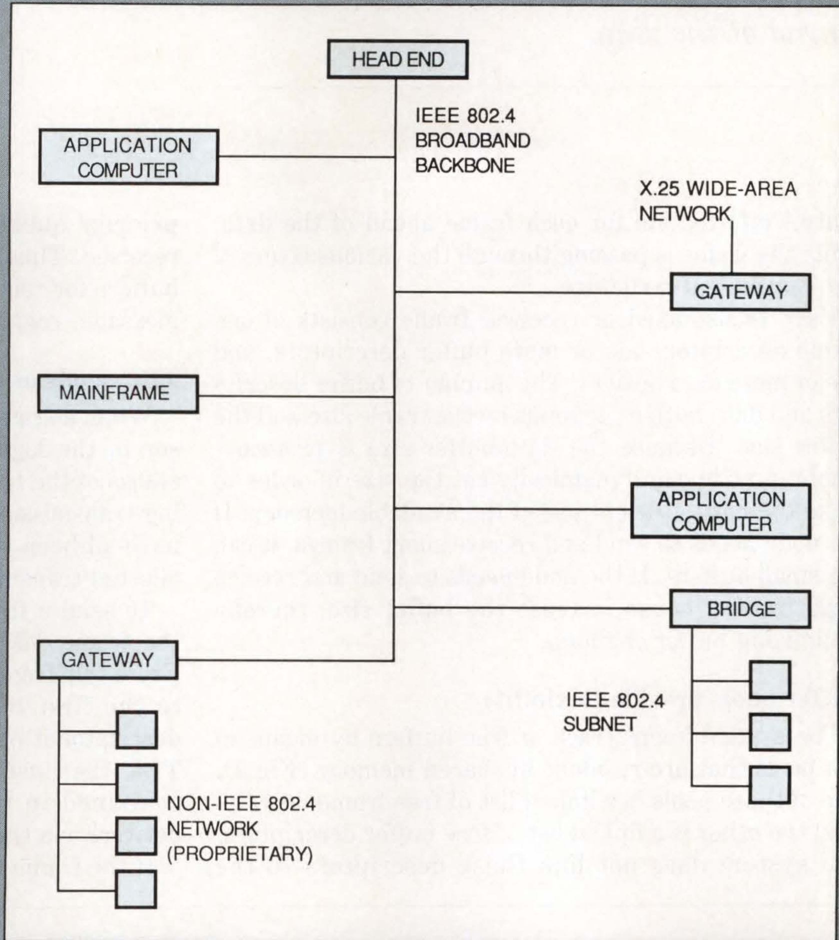

Fig A—A typical factory network uses a broadband medium to connect the main nodes to the backbone cable. You can connect subsidiary local networks to the main network by means of gateway or bridge nodes.

TABLE A—COMPARISON OF CARRIERBAND AND BROADBAND MEDIA

CHARACTERISTIC	CARRIERBAND	BROADBAND
DATA ERROR RATE	1×10^{-7}	1×10^{-9}
DISTANCE	2500 METERS (WITH REPEATERS)	40 MILES
NOISE VULNERABILITY	MEDIUM	LOW
MAINTENANCE	VERY EASY	EASY

scratch pad for the TBC. This area contains pointers to four transmit queues, four receive queues, the pool of free frame descriptors, and the pool of free buffer descriptors.

Each frame descriptor contains a confirmation word, a status word, a pointer to the next frame descriptor, a pointer to the first buffer descriptor, and the data length of the frame. In addition, the frame descriptor contains a pointer to the immediate-response frame, the source-node address, the destination-node address, and the control field of the frame. The IEEE 802.4 standard specifies that the frame be no longer than 8k bytes.

Each buffer descriptor contains a pointer to a data buffer, a pointer to the next buffer descriptor, the buffer length, an indication word, and control and offset values. Data buffers contain only data (no control information) and have a maximum length of 32k bytes. The offset count (in bytes), which is located in the last word of the buffer descriptor, indicates how far from the beginning of the data buffer the actual data starts. This parameter allows the system to place address and

A programmable timer governs the maximum time for which a station may retain control of the ring.

control information for each frame ahead of the data, while the frame is passing through the various layers of the 7-layer OSI structure.

Each transmitted or received frame consists of one frame descriptor, one or more buffer descriptors, and one or more data buffers. The number of buffer descriptors and data buffers depends on the frame size and the buffer size. Because the data-buffer size is programmable, a node can dynamically set the size in order to make the most efficient use of the available memory. If the node needs to send and receive short frames, it can use small buffers. If the node needs to send and receive large frames, it can increase the buffer size, thereby minimizing buffer chaining.

Buffer pools provide flexibility

The system keeps track of free buffers by means of two pools that are resident in shared memory **(Fig 4)**. One of these pools is a linked list of free frame descriptors; the other is a linked list of free buffer descriptors. The system does not link these descriptors to the priority queues until after a good frame has been received. Thus, the system can make efficient use of its buffers for received frames: It can use any buffer for a message, regardless of the message's priority.

TBC sends as many frames as possible

When a station receives the token from its predecessor in the logical ring, the station's TBC checks the status of the transmit queues. If any frames are awaiting transmission, the TBC transmits frames until they have all been sent or until it has used up the station's allotted transmission time.

To send a frame, the TBC first obtains a pointer to the frame descriptor of the first frame in the queue. From this frame descriptor, the TBC obtains a pointer to the first buffer descriptor, and from the buffer descriptor it obtains a pointer to the buffer itself. The TBC then uses its DMA channel to fetch the data contained in the buffer and sends the data to the network via the FIFO buffer and transmit circuitry.

If the frame has more than one buffer, the TBC goes

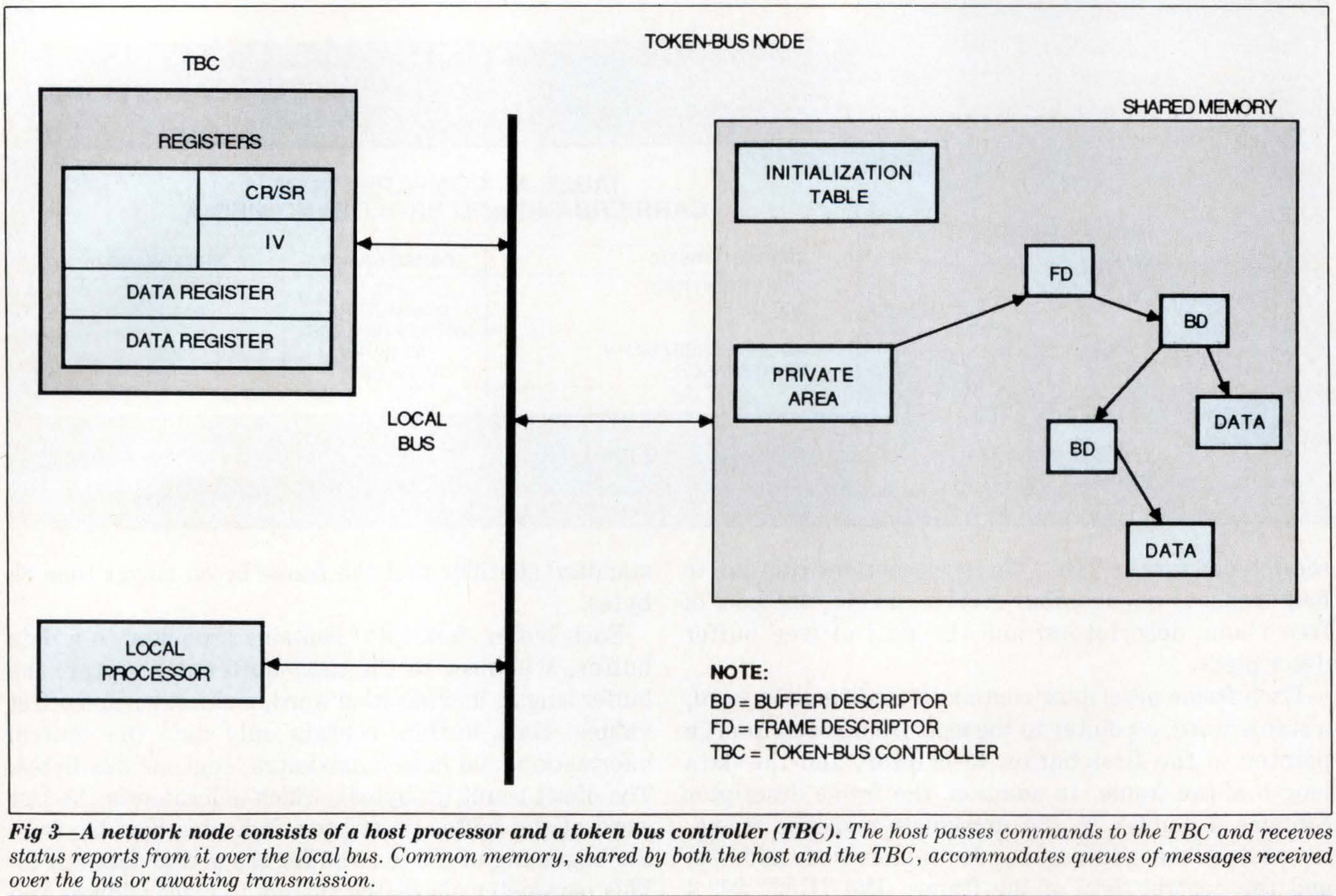

Fig 3—A network node consists of a host processor and a token bus controller (TBC). *The host passes commands to the TBC and receives status reports from it over the local bus. Common memory, shared by both the host and the TBC, accommodates queues of messages received over the bus or awaiting transmission.*

back to the frame descriptor, where it finds the pointer to the next buffer descriptor. In the new buffer descriptor, the TBC finds the pointer to the next data buffer. The TBC repeats this procedure until it has sent all the buffers of the frame and has appended the cyclic redundancy check (CRC) word. The TBC then writes a confirmation word into the frame descriptor; this word indicates either that the frame was successfully transmitted, or that the attempt failed.

To notify the host of the status of the frame, the TBC generates an interrupt request (provided that the interrupt mask allows TBC interrupts). The host services the interrupt and examines the confirmation to find the status of the associated frame. If its allowable token-holding time has not been used up, the TBC then returns to the transmission queue, finds the pointer to the next frame descriptor, and sends the next frame.

All the stations except the token holder monitor the network continuously and check the destination address of any message they hear. If the address matches the address of an individual station, or if the address is the broadcast address, that station accepts the frame. From the pool, the receiving TBC takes a free frame descriptor; from the private area, it takes a pointer to a free buffer descriptor. It loads this pointer into the frame descriptor. The TBC then loads the frame descriptor with the MAC destination address, the MAC source address, and frame-control information.

Incoming data starts filling the 40-byte FIFO buffer. When the buffer is full, the TBC transfers the data, via the DMA channel, to the data buffer specified by the buffer descriptor. If the incoming frame needs more

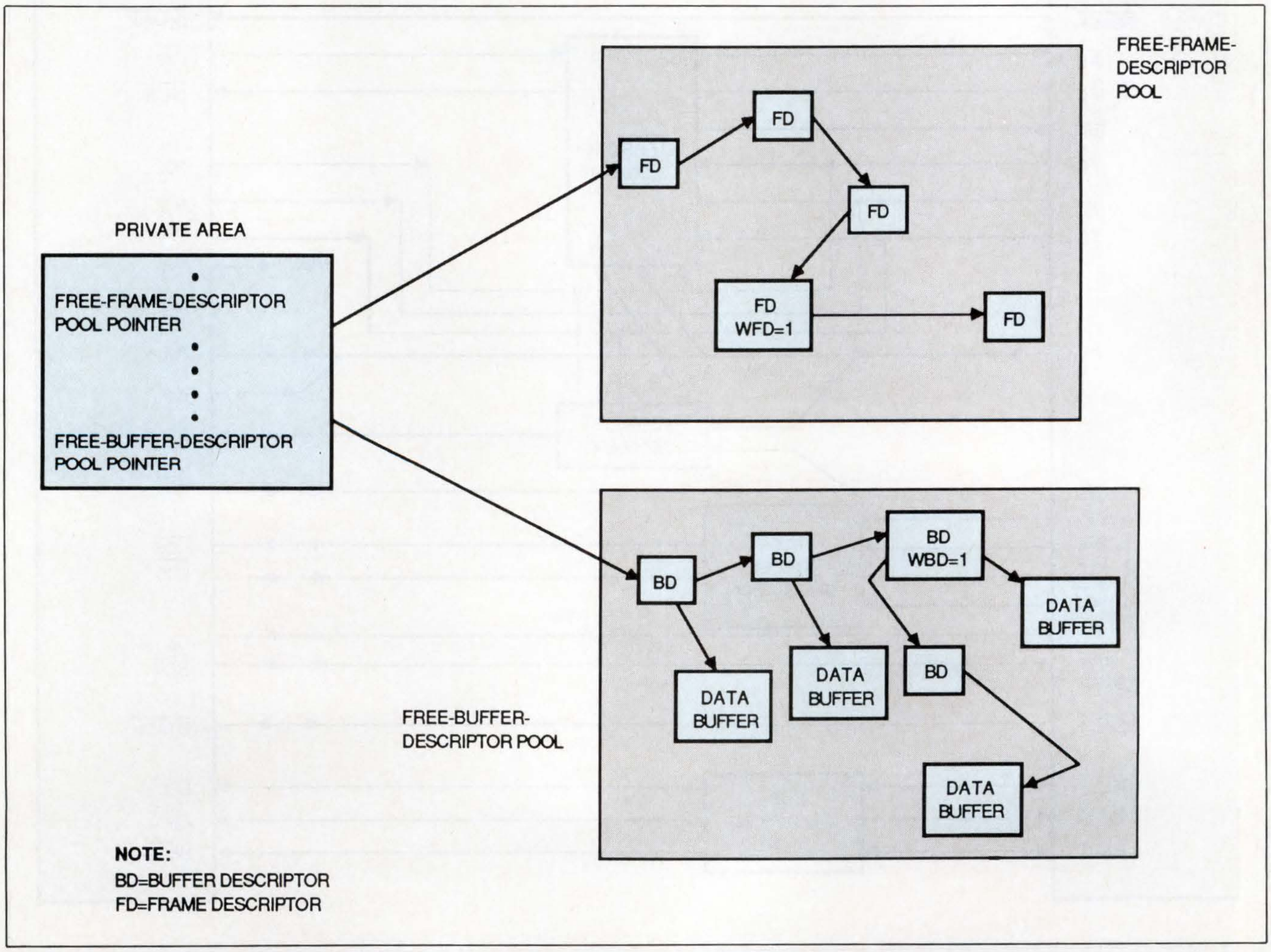

Fig 4—The host assembles message frames for transmission *by drawing frame descriptors and buffer descriptors from a pool of free descriptors. The host assembles these into a transmit queue and sends the TBC a pointer to the head of the queue.*

A host computer and a token bus controller pass data and parameters to each other via a shared area of memory.

than one data buffer, the TBC obtains additional buffer descriptors as necessary from the pool. If an error occurs, the TBC checks the error mask; if the mask is set to allow that type of error, the TBC notes the error in the frame descriptor and continues receiving until the frame is complete. If the mask does not permit the error, the TBC aborts reception.

The TBC now links the frame descriptor to the appropriate receive queue according to the priority of the frame, and it sets a status bit in the frame descriptor to indicate that this frame is the last received frame. The TBC also changes the status of the previous frame descriptor on the queue, indicating that that frame is no longer the last received frame. If the interrupt mask permits, the TBC then generates an interrupt request to notify the host that a new frame has been added to the queue.

You can program the TBC to collect a variety of

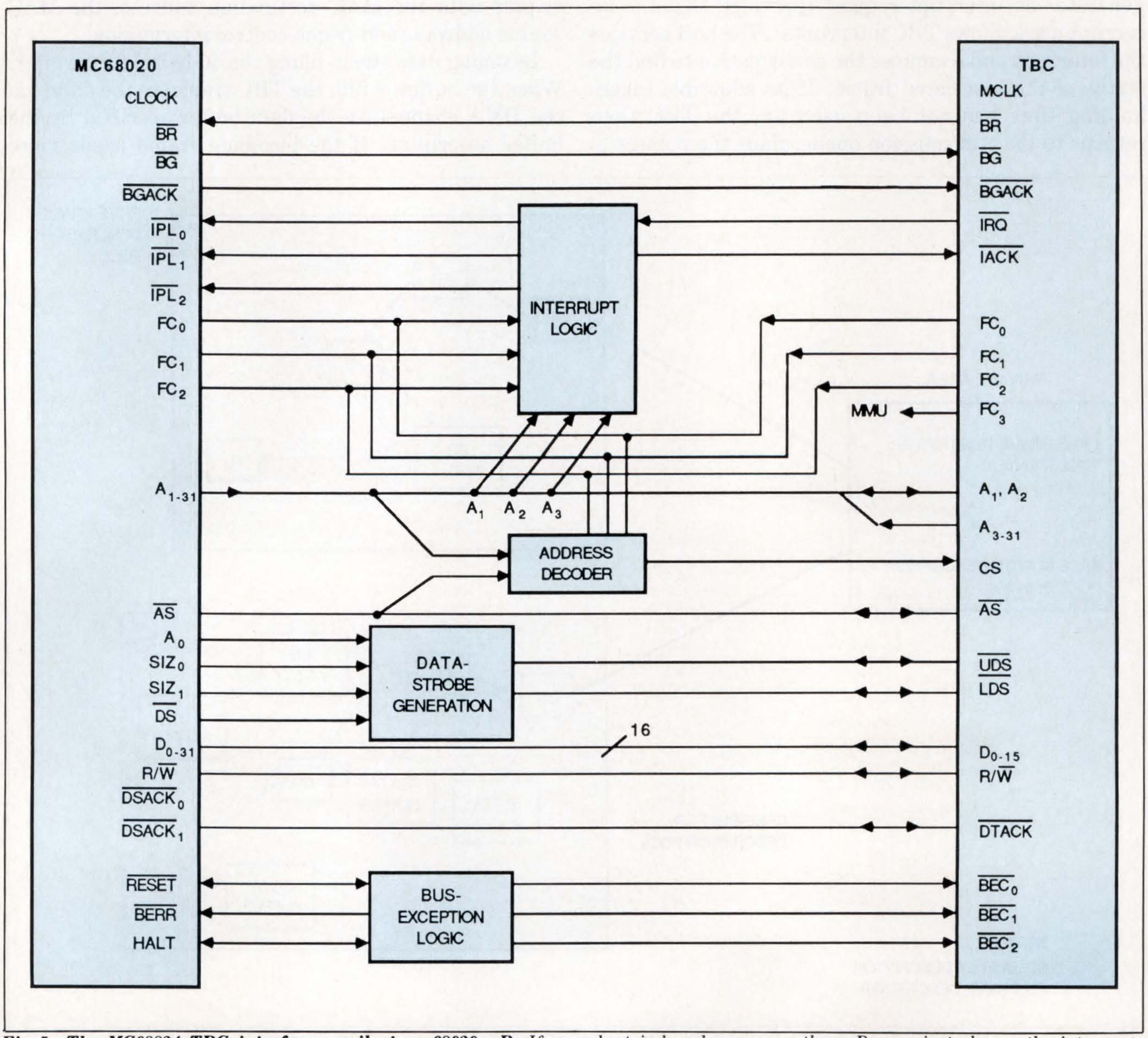

Fig 5—The MC68824 TBC interfaces easily to a 68020 μP. *If your host is based on some other μP, you just change the interrupt, address-decode, data-strobe-generation, and bus-exception logic to match the signals available from the host.*

A token bus controller should provide facilities for testing data paths not only locally but across the network.

statistics (listed in **Table 1**) about the performance of the node. You can program a threshold value for each of these statistics. When a statistic's value exceeds its threshold, the TBC generates an interrupt request to notify the host. You can also program the TBC to act as a "promiscuous listener." In this mode, the TBC monitors the network and collects statistics on the number, types, and lengths of the frames sent by all stations on the network.

Host-processor interface

When you're designing products for operation over your network, you'll want to use a standard interface for all the products, regardless of the host's memory size or the type of processor on which the host is based. The MC68824 TBC lets you use a 32-bit address bus and either an 8-bit or a 16-bit data bus. Also, you can use either the Motorola/IBM (high, low) or the DEC/Intel (low, high) storage order for address bytes. You'll find it simple to interface the TBC to a 68020-based host **(Fig 5)**, and you can easily modify the bus-interface signals if the host uses some other processor.

Four registers in the TBC's register file are accessible to you **(Fig 6)**. You use the 8-bit command register (CR) to pass commands to the TBC, and the 32-bit data register ($DR_{0\text{-}3}$) to pass parameters to or from the TBC. The host can interrogate the 8-bit semaphore register (SR, which shares the command register location) in order to determine when a previously initiated command has been executed. The remaining register is the interrupt register (IR), which points to the TBC's interrupt vector.

The TBC's command set consists of 28 commands in seven different categories. The five Initialization commands initialize the TBC and provide a software reset. The four Set Operation Mode commands set or reset the various TBC parameters. The three TX Data Frames

TABLE 1—STATISTICS COLLECTED BY THE TBC

- NUMBER OF TOKENS PASSED
- NUMBER OF TOKENS HEARD
- NUMBER OF PASSES THROUGH NO-SUCCESSOR-8 STATE
- NUMBER OF "WHO FOLLOWS" INQUIRIES
- NUMBER OF TOKEN PASSES THAT FAILED
- NUMBER OF NON-SILENCE CHARACTERS
- NUMBER OF FCS ERRORS
- NUMBER OF E-BIT ERRORS
- NUMBER OF FRAME FRAGMENTS
- NUMBER OF FRAMES TOO LONG
- NUMBER OF NO FRAME- AND BUFFER-DESCRIPTOR ERRORS
- NUMBER OF OVERRUNS

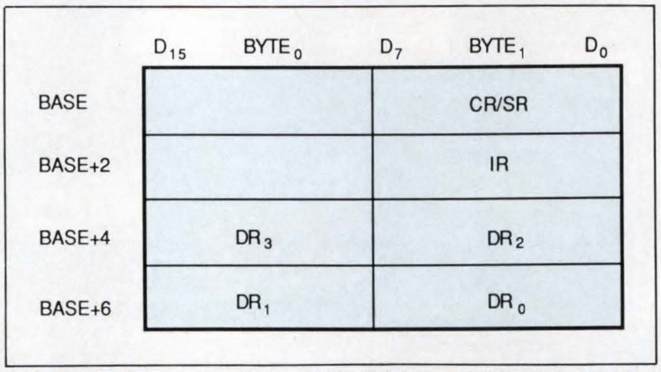

Fig 6—The internal registers of the TBC *are 16 bits wide. The host can address these registers individually or in pairs.*

commands let you start, stop, and restart the transmission of data frames. The seven Set/Read Value commands let you read parameters and statistical information or set the values of MAC parameters and TBC pointers. Another command group lets you enter or leave the modem-management mode and issue modem commands or set modem parameters.

The final command group lets you set up and execute four types of tests that help to isolate network problems during operation: a host-interface test that tests the path from the system memory buffer to the TBC's FIFO buffer and back to system memory; a full-duplex loopback test that tests the path from system memory to the FIFO buffer in both directions simultaneously; a transmitter test that tests the path from the transmit queue to the modem's transmitter circuits; and a receiver test that tests the path from the modem's receiver to the receive queue.

The TBC-modem interface

The TBC manages the physical layer of the node by means of a serial interface that allows it to pass commands and data to an intelligent modem. The TBC serial interface lets you use any modem that conforms to IEEE Standard 802.4G.

The TBC's serial interface **(Fig 7)** comprises two channels: a physical data-request channel and a physical data-indication channel. Some of the signals in both channels are multiplexed, and those signals have different meanings in each of the interface's two modes of operation. When the interface is in the station-management mode, the upper layers of the software can send management commands to the modem over the data-indication channel. Such commands may reset the physical layer, enable the transmission circuits, or establish loopback test conditions. Likewise, the modem can

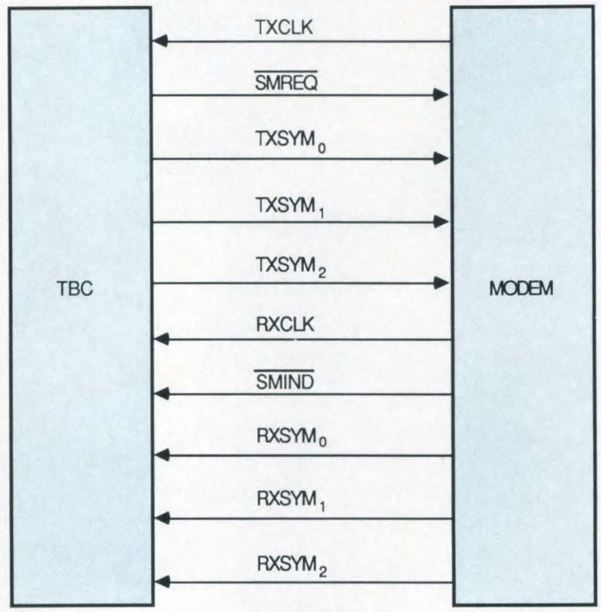

Fig 7—This serial interface conforms to the IEEE 802.4G standard. *The three TXSYM and RXSYM signals are multiplexed, and they have different meanings according to the mode in which the TBC and the modem are operating.*

return status information and any error conditions to the TBC over the data-indication channel.

When the interface operates in the MAC mode, the MAC layer uses the data-request channel to send encoded requests to the modem for data transmission. The physical layer (that is, the modem circuitry) returns encoded status information relating to its reception of data. **EDN**

Author's biography

Ivan Erickson is marketing manager of communications devices at Motorola's Microprocessor Div (Austin, TX). He is responsible for the marketing of the 68824, 68605, 68184, 68194, and other intelligent communications ICs. Before joining Motorola, Ivan spent eight years with Texas Instruments, where he was product manager of business system computers. He holds a BSEE from the University of Maine and an MBA from Penn State University, and is a member of the IEEE. In his spare time he enjoys hiking, camping, and photography.

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TEK'S NEW EASY-TO-EXPERT LOGIC ANALYZER $3995.*

Introducing the Tek 1220 and 1225: the two newest members of the Tek 1200 Series of logic analyzers. Nothing else in their price range delivers so much and makes it all so easy to use. Consider:

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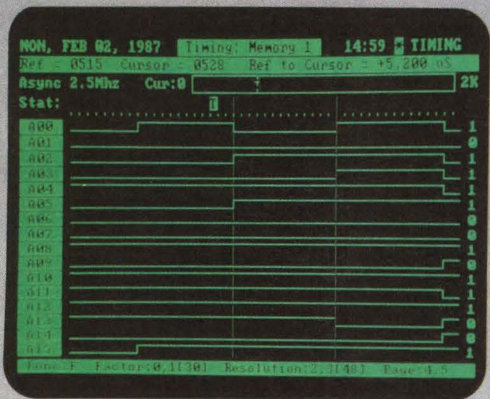
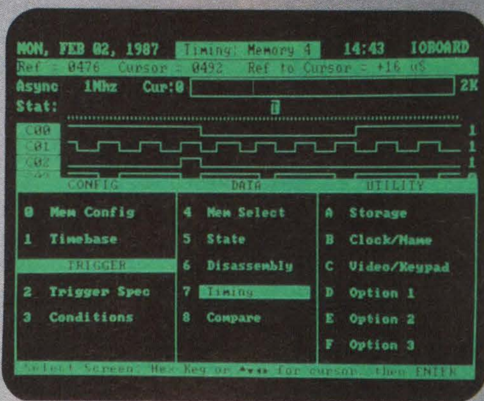


Left Set reference cursors on the timing diagram to measure pulse width or the time between pulse edges. **Above** State tables are displayable in binary or hex formats.



Above Pop-up menus, such as this main menu, are easy to understand and logically arranged.

Simple solution cures glitches on high-speed buses

High-speed bus systems such as Multibus II and the VME Bus have spawned a new gremlin: the ground-shift-induced logic fault. Unfortunately, such faults look like crosstalk in a system's backplane. Engineers have wasted a lot of time and money chasing these faults when the problem really originates in the system's connectors.

Richard M DeBock, *Matrix Corp*

IC design houses have long known of ground-shift phenomena. The issue has surfaced publicly in the debates over the placement of power and ground pins on advanced CMOS logic devices. The same physics applies to digital board designs for high-speed buses. The advent of Multibus II and VME Bus products, coupled with speed and current-drive improvements of TTL buffers, has now brought the problem of ground shift to light in bus systems.

Ground shift is the movement of a component's ground reference away from 0V and results from switching too much current too quickly. If the ground shift in a digital system is large enough, then logic faults occur. Perhaps surprisingly, you can often trace these logic faults to a system's connectors. In order to convince you who the real culprit is, some theoretical discussion is called for.

Each pin of a connector acts as though it were an inductor with a series resistor, paralleled by a capacitor tied to the neighboring pins. Although the connector hardly affects the shape of signals with long rise and fall times, Multibus II and VME Bus both require high-speed switching and drive characteristics such that you can no longer ignore the analog nature of the connectors.

Both buses specify DIN41612-type pin-and-socket connectors, which can have a maximum of 38-nH series inductance (with 0.02Ω series resistance) and 0.7-pF pin-to-pin capacitance. Because of the capacitive loading and current drive on these buses, you can ignore the connectors' resistive and capacitive effects, but because of the fast switching times of the signals, you can't ignore the pins' inductance.

In a simplified bus-connection model **(Fig 1)**, a board with Schottky-TTL drivers connects to a backplane via a bus connector. The model neglects the connector's capacitance and resistance and simply shows the inductance. To simplify the math, all the signal-line impedances are $Z_{0'}$. (In a real system the $Z_{0'}$ of one line doesn't necessarily equal the $Z_{0'}$ of any other line.) The model also shows the power supply's impedance and the power-supply and ground connections from the backplane

If the ground shift in a digital system is large enough, logic faults will occur.

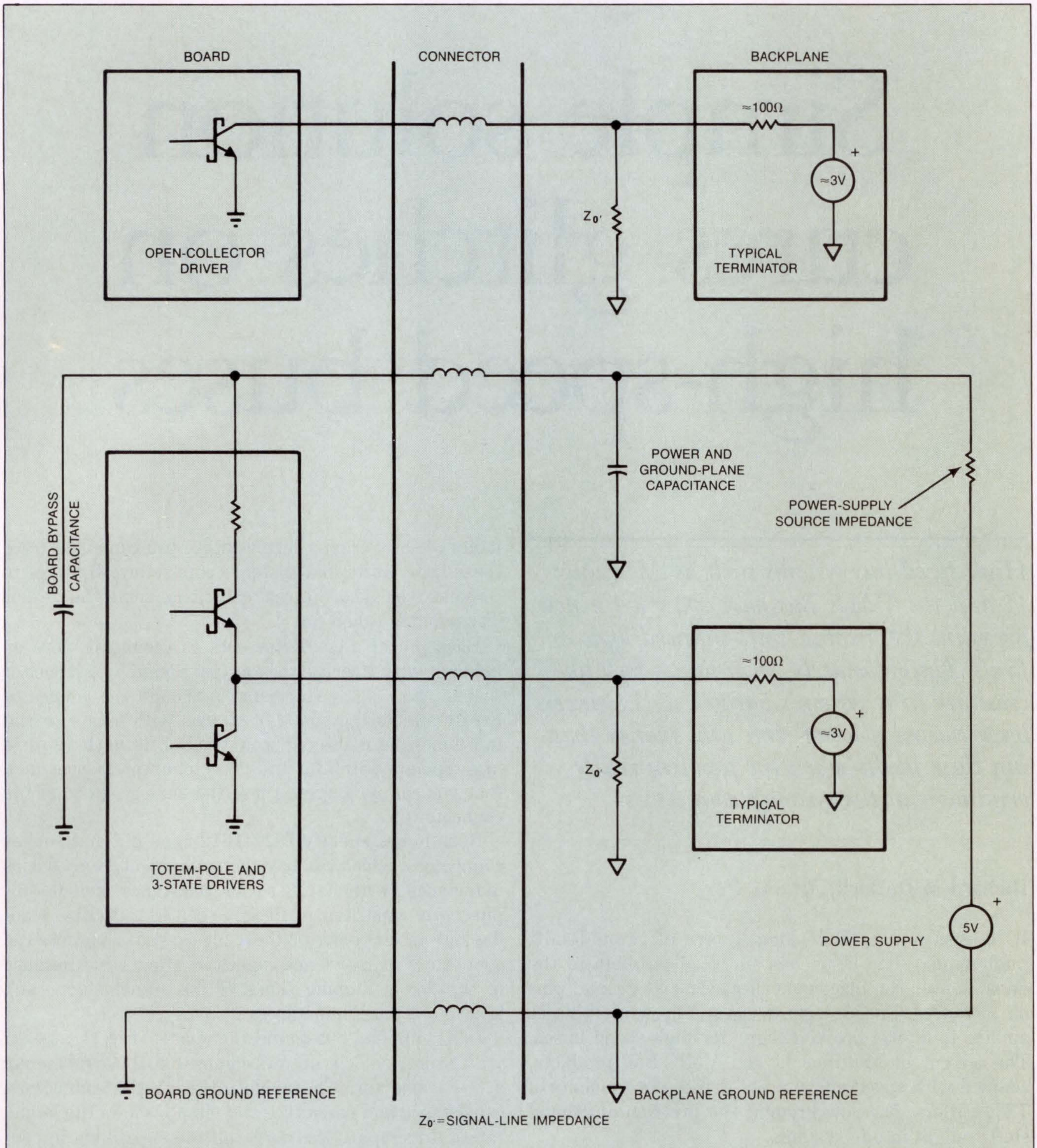


Fig 1—This simplified model neglects the bus connector's capacitance *and resistance and is simply inductance. The model lumps together all signal-line, bypass, power- and ground-plane impedances and capacitance. The backplane's terminators are a simple voltage source and a series resistor.*

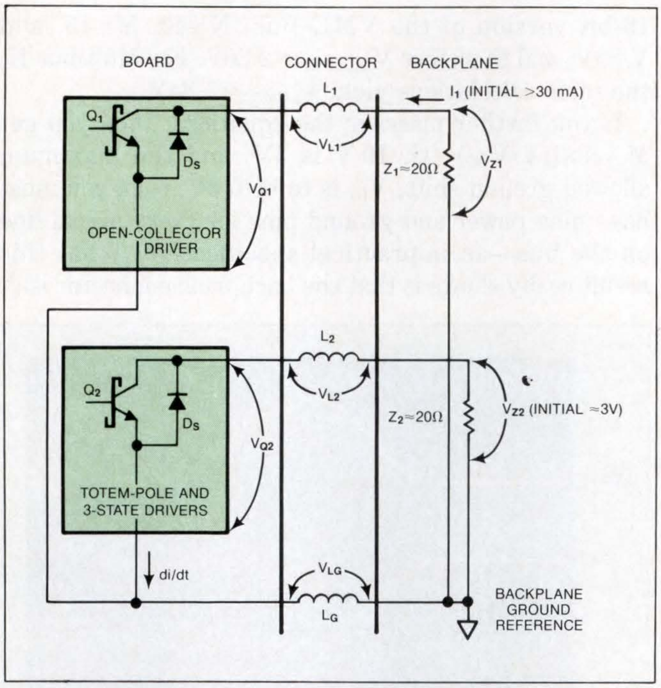


Fig 2—In this example, an open-collector driver *holds a signal line low while a second totem-pole driver attempts to drive its own signal line low. Q_1 is the open-collector driver, and Q_2 is the bottom part of the totem-pole driver.*

to the board, and it lumps together the bypass, power, and ground-plane capacitance. The backplane's terminators are a simple voltage source and a series resistor.

In order for a board to change a logic level on a line that goes to the backplane, it must change the direction of the current flow—either into or out of the line. Moreover, the current flow's behavior depends on the total impedance of the line, the connector, the backplane termination, and other components attached to the line.

An example will help you understand just how connectors can cause ground-shift-induced logic faults. In this instance, an open-collector driver holds a signal line low while a second totem-pole driver attempts to drive its own signal line low **(Fig 2).** Q_1 is the open-collector driver, and Q_2 is the bottom part of the totem-pole driver. D_S is the substrate-to-collector diode associated with each device and results from IC manufacturing methods. (Later, D_S will figure as an unexpected current source.) Z_1 and Z_2 represent the characteristic impedance of a modern, fully loaded backplane, about 20Ω.

Initially, Q_1 is on and sinks at least 30 mA because of current from the backplane termination and the input loading of the receivers connected to that line. At this time, V_{Z1} is 0.5V. Because Q_2 is off, and because of the backplane's termination and the upper part of the totem-pole's driver, V_{Z2} has an initial voltage of approximately 3V. Also, V_{L1}, V_{L2}, and V_{LG} are all 0V because the circuit is in a steady-state condition. (V_{LG} is the voltage developed across the combined inductance of all the power and ground pins; this inductance will later figure in the nonsteady-state analysis.)

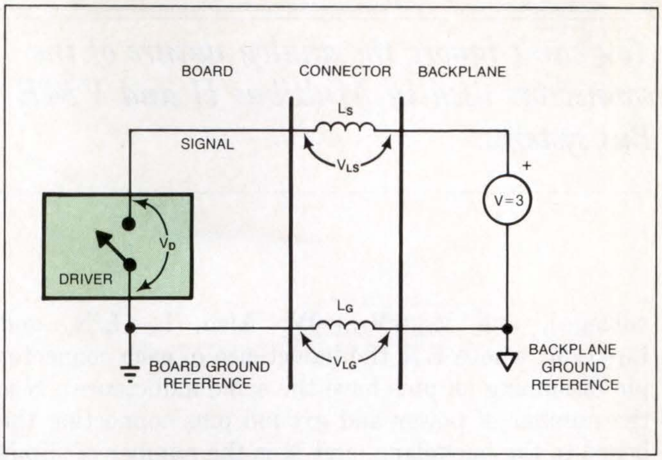


Fig 3—Calculating how large V_{LG} can be *requires a model of worst-case conditions. The driver can switch the signal current infinitely fast, and the signal leads have no resistance.*

Next, Q_2 switches on. Immediately, the V_{L2} and V_{LG} voltages develop across the connector because of the change in current flow (di/dt). In this simplified model, Q_2 doesn't necessarily represent just a single line; it can represent many lines switching at once—often the case in bus systems.

If many lines switch on simultaneously, the result is a large total di/dt, computed by adding each individual di/dt of each line. This large di/dt, in turn, causes V_{LG} to rise from 0V. The rising V_{LG} reduces Q_1's V_{CE}. If V_{LG} is large enough (greater than V_{Z1}'s initial voltage), then Q_1 gets cut off, and I_1 changes direction and starts flowing away from the collector of Q_1. This reverse flow makes Q_1's collector look as if it is sourcing 30 mA across 20Ω and yields a 0.6V jump over the steady-state value of V_{Z1}. If the steady-state voltage, $V_{Z1INITIAL}$, is 0.5V, then the resulting V_{Z1} pulse becomes 1.1V with respect to the backplane's ground reference. This voltage is high enough to cause a logic fault in some receivers.

If V_{LG}, the board's ground-shift voltage, moves far enough positive with respect to Q_1's collector voltage such that D_S turns on, then the open-collector driver will source current into the signal node, thereby adding to the signal line's voltage jump.

Worst-case scenario is enlightening

To enhance your understanding of ground-shift disturbances, it's useful to determine the upper limits of V_{LG}. For this exercise, a model of worst-case conditions will suffice. This model is one in which the driver can switch the signal current infinitely fast (an ideal switch) and one in which the signal leads have no resistance **(Fig 3).** In the steady-state condition, with the driver not conducting, $V_D = V = 3V$ (the terminator's

You can't ignore the analog nature of the connectors used in Multibus II and VME Bus systems.

voltage), and $V_{LS}=V_{LG}=0V$. Also, $L_S=L/N$, and $L_G=L/M$, where L is the inductance of each connector pin (assuming all pins have the same inductance), N is the number of power and ground pins connecting the board to the backplane, and M is the number of signal pins that can switch low simultaneously.

After the switch closes, $V_D=0$, and $V_{LS}+V_{LG}=V=3V$. Also, $V_{LG}=V\times L_G/(L_G+L_S)$. Substituting for L_G and L_S yields $V_{LG}=V\times(L/M)[(L/M)+(L/N)]$. Simplifying the equation yields $V_{LG}=V\times N/(N+M)$. For the 32-bit version of the VME Bus, N=64, M=17, and V=3.0V, and therefore $V_{LGMAX32}=2.37V$. For the 16-bit version of the VME Bus, N=40, M=13, and V=3V, and therefore $V_{LGMAX16}=2.26V$. For Multibus II, the same calculations yield $V_{LGMAX}=1.84V$.

If you further massage the equations, then you get $M=N\times[(V/V_{LG})-1]$. If V is 3V, and the maximum allowed ground shift, V_G, is to be 0.3V, then you must have nine power and ground pins for every signal line on the bus—an impractical specification. What this result really shows is that the backplane connector isn't

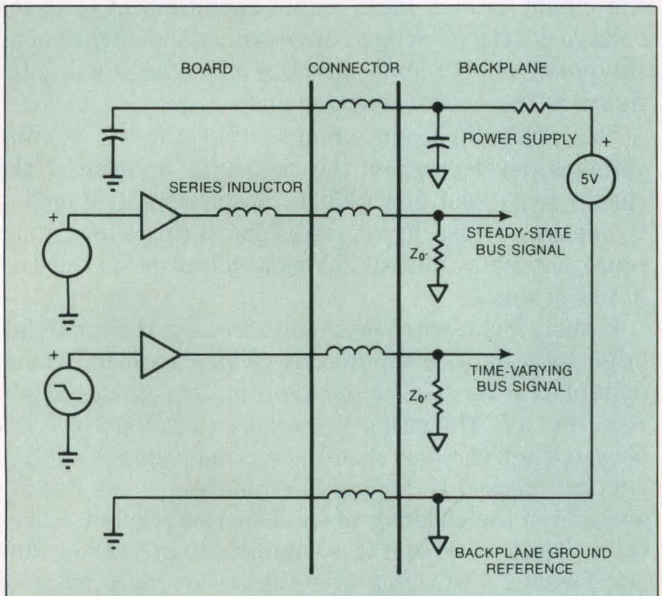


Fig 4—In this solution, a series inductor divides *the ground-shift voltage between itself and the backplane's and connector's inductance so that the series inductor drops the majority of the ground-shift voltage.*

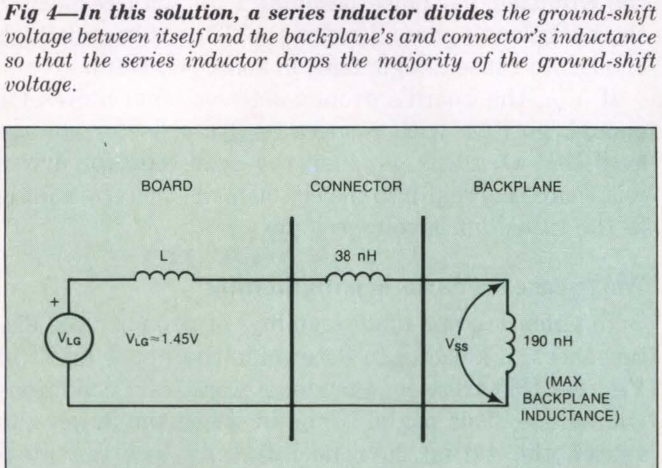
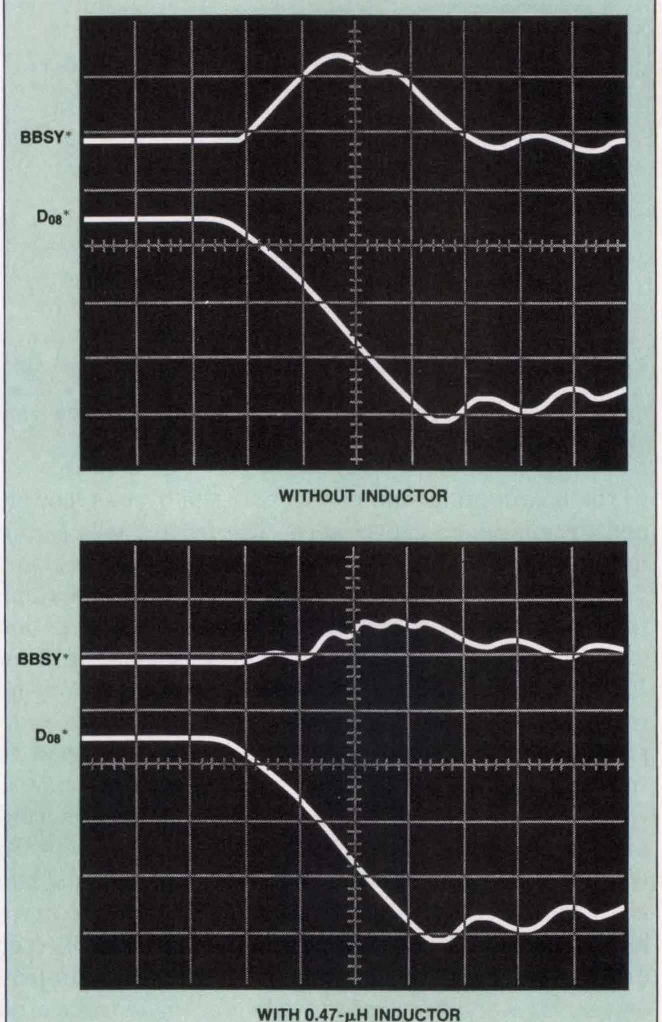


Fig 5—You can calculate the value *of the inductor from this circuit model.*



TRACE	VERTICAL	HORIZONTAL
BBSY*	0.5V/DIV	5 nSEC/DIV
D_{08}*	1.0V/DIV	

Fig 6—This test setup for verification *includes a 20-slot VME Bus backplane with standard terminators, one driver board, and 19 load boards.*

the best way to provide power and ground to a board.

Fig 4 shows a workable solution. An inductor is in series with the buffer of the "steady-state signal" line and the line's connector pin. (A steady-state signal is one that must stay at a known level as a group of signals change state simultaneously.) The series inductor divides the ground-shift voltage between itself and the backplane's and connector's inductance so that the added series inductor drops the majority of the ground-shift voltage.

You can calculate the value of the inductor from the circuit model of **Fig 5.** V_{LG} is in this case the theoretical maximum ground-shift voltage calculated earlier, and V_{SS} is the maximum allowed shift in the steady-state signal's level. If V_{SS} is 0.4V, for example, then $L=190\times[(V_{LG}/V_{SS})-1]-38=461$ nH. The closest, larger standard value is 0.47 μH. Matrix Corp has successfully specified this inductance value on its VME Bus boards.

Although the calculated ground-shift voltages are theoretically obtainable, fortunately they aren't really possible except with an ideal switch—and a transistor isn't an ideal switch. When high-speed TTL devices drive the bus, the ground shift is actually about 1.25V for eight lines simultaneously switching from a high to a low level. The ground shift peaks at approximately 1.45V when more than 12 lines simultaneously switch

Common approaches don't circumvent glitches

All high-speed bus systems will eventually experience glitches from ground shift, unless you take precautions designing the boards that interface with them. Proponents of various bus schemes make claims and counterclaims that one bus or another doesn't experience these glitch problems for various reasons (buried control lines, extra ground pins, synchronous or asynchronous protocols, or address and data multiplexing), but none of these claims are valid.

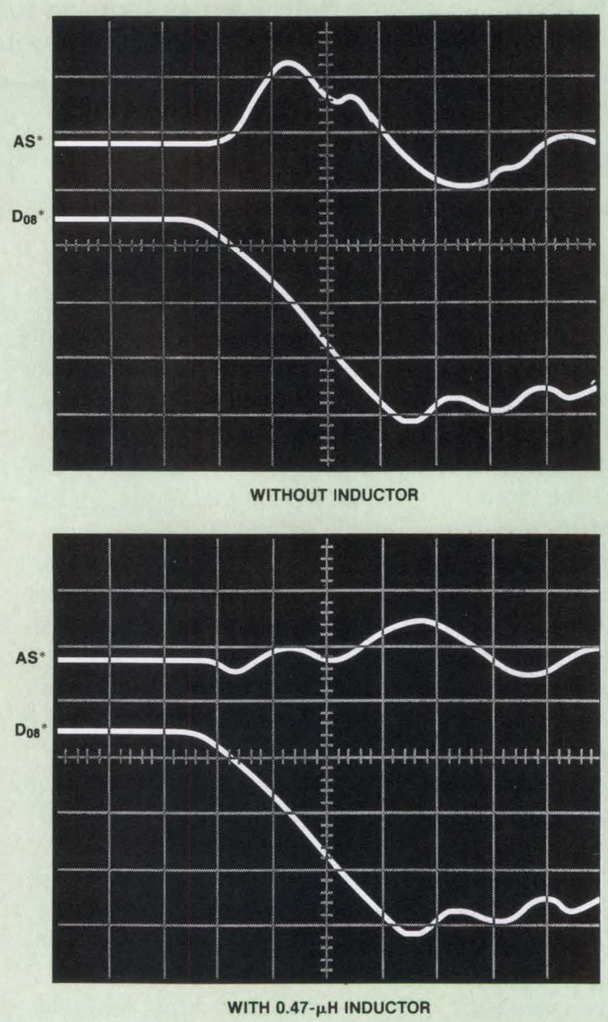
- Burying the control lines between or within the power and ground planes of a backplane can undermine the worst-case signal-line skewing assumptions that are built into any bus specification. For example, the VME Bus specifies a maximum signal skew of 10 nsec between like-specified control lines. If you use a different layout for some control lines, then more than 10 nsec of skew may occur.
- Extra ground pins are impractical. If you don't have nine power and ground pins per signal line, then ground shift will occur if the drivers do not restrain the board's total di/dt.
- Even with synchronous protocols, if the drivers don't restrain the board's total di/dt, then ground shift will result. The ground shift can cause double clocking of inputs on the receiving board before the inputs are stable and desynchronize the board with respect to the bus activity.
- Similarly, with asynchronous protocols, even though address and data lines change state randomly, each group of signals usually changes as a result of some externally or internally generated event. If eight or more lines change simultaneously, then ground shift may occur.
- Address and data multiplexing means that fewer signal lines switch simultaneously than in nonmultiplexed systems, but nevertheless guarantees that all grouped signal lines (address or data) switch simultaneously. If the drivers don't restrain the board's total di/dt, then ground shift will result.
- Specifying drivers with controlled rise and fall times such that the maximum total di/dt of the drivers is small enough to limit the ground shift to an acceptable level is unrealistic. In order to be practical, these drivers would have to be bidirectional octal devices, operate at TTL signal levels, and be readily available.

In general, none of today's high-speed buses adequately addresses the ground-shift problem. This oversight isn't from lack of foresight on the part of the original bus designers but is due to unprecedented performance improvements in semiconductor logic. Tomorrow's buses will, in all likelihood, consider the ground-shift problem in the original design stages; however, for today's TTL-based bus structures, you should use a series inductor on any signal line that must be held in a steady-state low condition as a large group of signal lines changes state simultaneously.

from high to low. The reason for the peaking is that the ground shift constitutes negative feedback for the output transistors of the TTL buffers. This negative feedback reduces the transistors' current-sinking capability, and this reduction causes the total di/dt to peak long before you can obtain the maximum ground-shift voltage (as calculated from the simplified model).

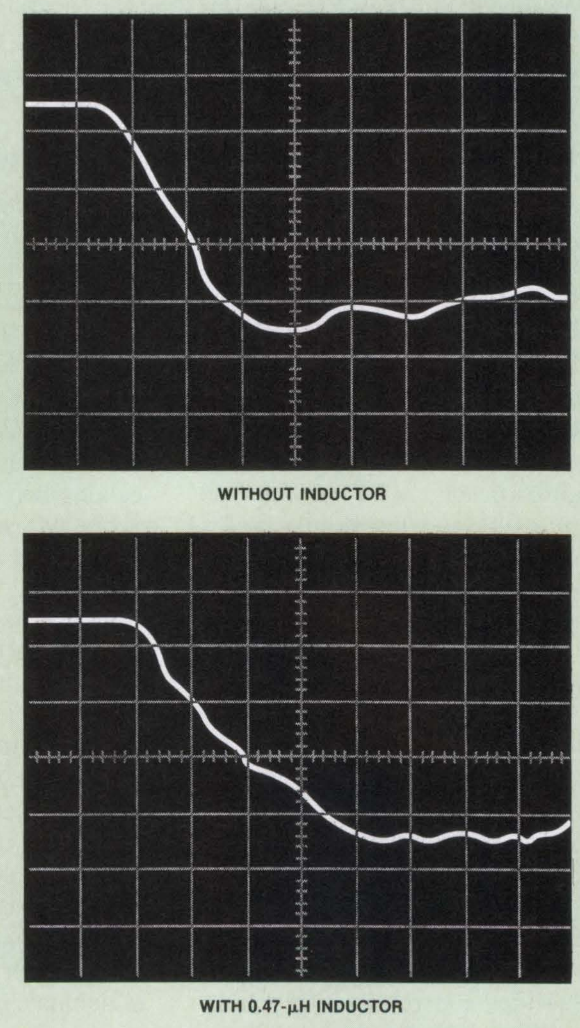
The test setup of choice for experimental verification of the preceding calculations is a 20-slot VME Bus backplane with standard terminators, one driver board, and 19 load boards. The load boards produce a worst-case load on connector pins $A_{1\text{-}8}$ and $C_{1\text{-}8}$. These pins connect to the data lines $D_{0\text{-}15}$. One other line, BBSY* (Bus-Busy), connects to pin B_1, and this line too has a worst-case load applied to it. Using 74F245 transceivers, the driver board drives $D_{0\text{-}15}$ low while holding BBSY* low with a 74S38, an open-collector driver.

For these first tests, the driver board resides in slot 20, and measurements are taken at each slot. The load board in slot 1 provides the largest BBSY* pulse **(Fig**



TRACE	VERTICAL	HORIZONTAL
AS* D_{08}*	0.5V/DIV 1.0V/DIV	5 nSEC/DIV

Fig 7—In this test for glitches on AS*, *the results are similar to those of* ***Fig 6.***



TRACE	VERTICAL	HORIZONTAL
AS*	1V/DIV	5 nSEC/DIV

Fig 8—To determine the effects of the series inductor on bus timing, *these AS* fall-time measurements were performed holding $D_{0\text{-}15}$ high while toggling AS^*_0. Although the inductor didn't affect the rise time, the fall time did stretch out.*

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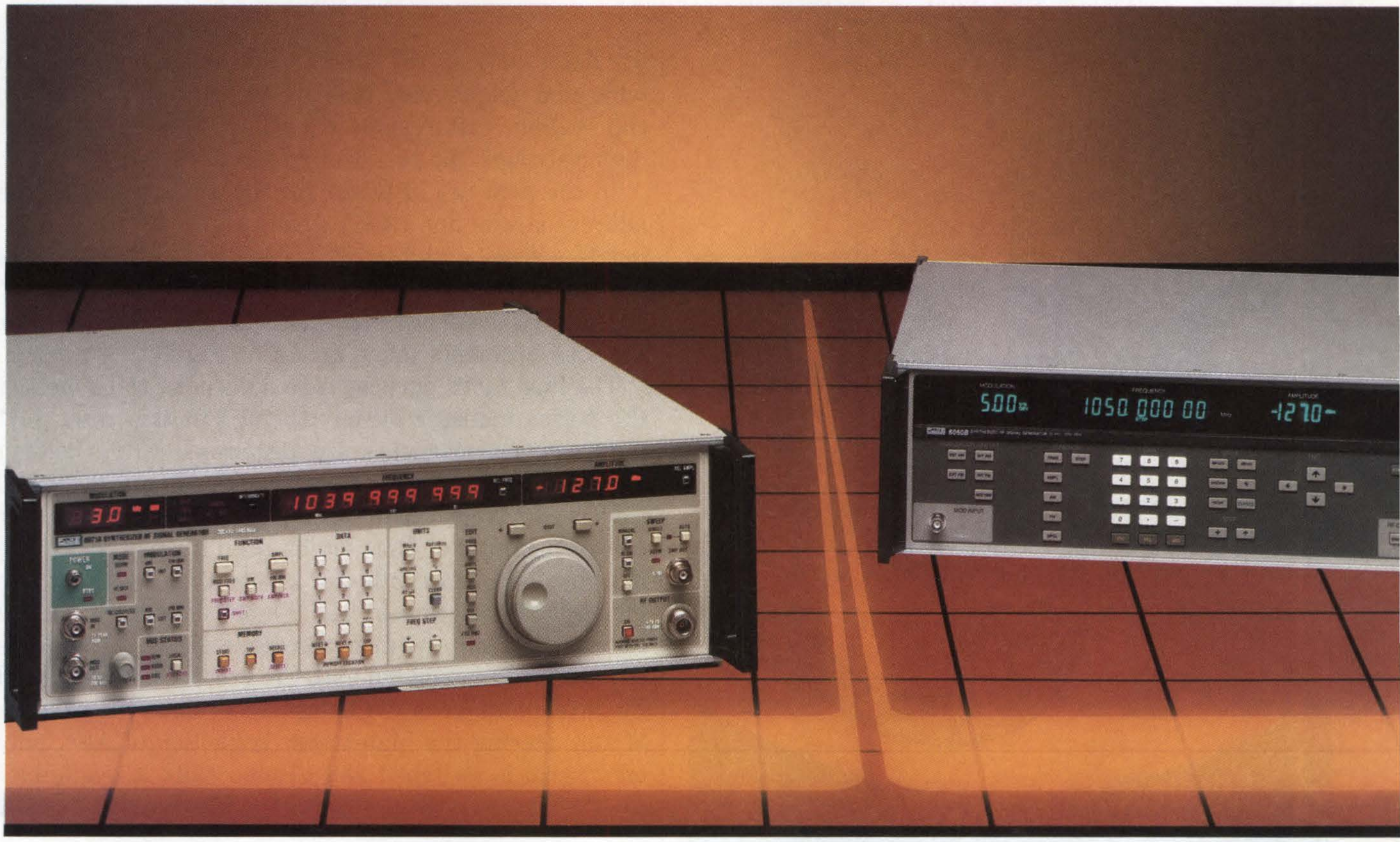

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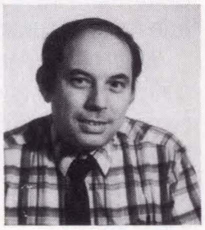
6). After moving the BBSY* line to a connector pin where no neighboring pins are driven by any board in the system, test results are still identical: The pulse definitely isn't the result of crosstalk.

In the next set of tests, the driver board holds the address strobe line (AS*) steady-state low while driving $D_{0\text{-}14}$ from a high to a low level. A 74F245 drives AS*. The greatest measured perturbations on AS* occur when the driver board is located in slot 20, and for the measurements taken at slot 1 **(Fig 7)**.

The final test's purpose is to determine the effects of the series inductor on bus timing. In this case, AS* fall-time measurements are performed while holding $D_{0\text{-}14}$ high and toggling AS^*_0 **(Fig 8)**. The slowest fall time occurs when the driver board resides in the center of the backplane. Rise times aren't affected by the installation of the inductor. Note that, without the inductor, the fall time of AS* is much faster than the fall time of D_{08} from the previous scope photos. The negative feedback associated with the ground shift produced by the simultaneous switching of $D_{0\text{-}14}$ slows the fall time of D_{O8}. During the high-to-low transition of AS*, only one signal is switched and ground shift is negligible. **EDN**

Author's biography



Richard M DeBock is the R&D manager for Matrix Corp in Raleigh, NC, where he oversees VME Bus new-product development. Prior to joining Matrix, he spent 14 years with Motorola in Phoenix, AZ, where he was involved in semiconductor R&D, process engineering, and μP product design. He obtained a BSEE from Arizona State University and is a member of Tau Beta Pi and Eta Kappa Nu. His hobbies include hiking and camping.

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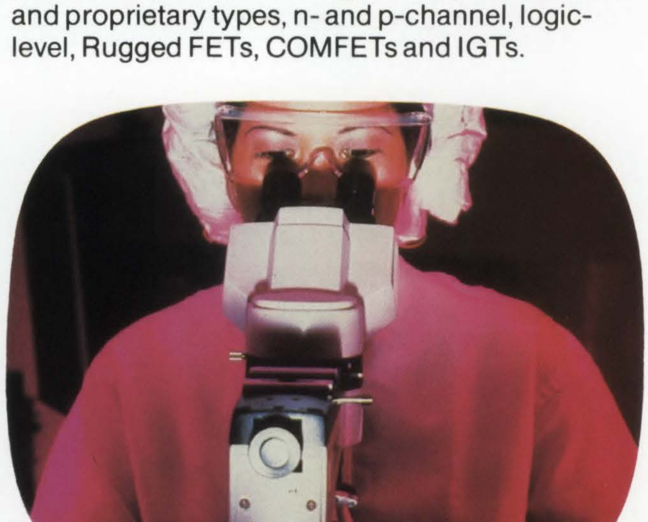

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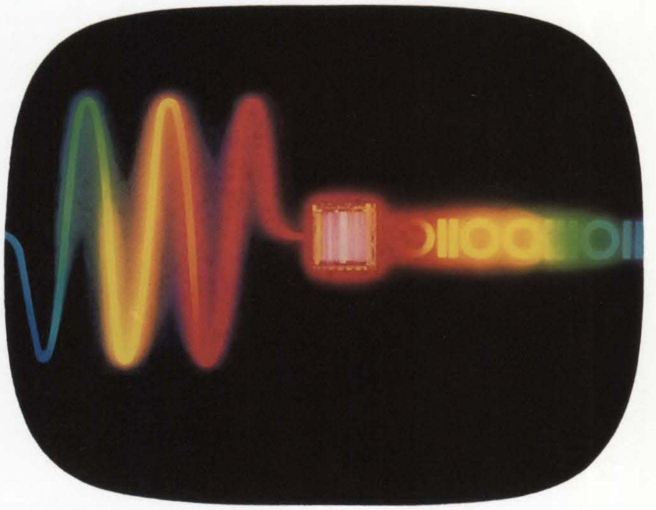

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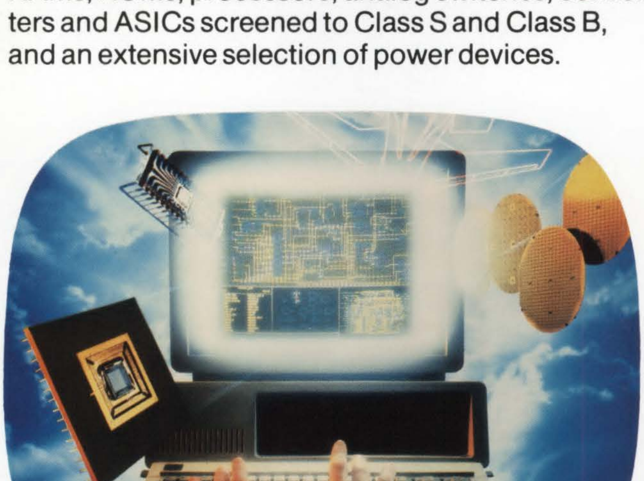

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Page addressing expands addressable memory in μP systems

Today's software-intensive applications have revealed a basic shortcoming of 8-bit processors—they often don't contain enough addressable memory. Even 16-bit systems can run short. Page-addressing techniques can free your system from program-memory limitations.

Terry Kendall, *Intel Corp*

For many of today's software-intensive applications, 8-bit microprocessor systems often require more memory than their μPs' address space can accommodate. Although an 8-bit processor's rich instruction set is usually adequate for most applications, the 64k-byte memory space of commonly used 8085s, Z80s, and 6800s can't accommodate enough RAM and flexible program memory for many modern applications. In fact, because firmware inhabits so much memory space, even 16-bit systems can run short of RAM. You can free both new and existing systems from program-memory limitations by using EPROMs, algorithms, and circuit techniques that let you implement page addressing.

Using page addressing to expand RAM is a well-established technique. You synthesize extra address lines by latching bits from the data lines that identify the page numbers.

For example, suppose that you need a 64k-byte memory space to hold your program, which is resident in four 16k-byte EPROMs. In a nonpaged 8085 system, four 16k-byte EPROMs would take up the 8085's entire 64k-byte memory space. You would have to address the EPROMs contiguously—at 0000 to $3FFF_{HEX}$, 4000 to $7FFF_{HEX}$, 8000 to $BFFF_{HEX}$, and C000 to $FFFF_{HEX}$. Thus, you'd have no room left for any RAM.

You can implement page addressing in such a system by adding latch and decoding circuitry that lets you stack the EPROMs in a 3-dimensional array. **Fig 1** shows an example of such a design. The design uses four 27128A 16k-byte EPROMs. In each plane, one EPROM occupies addresses in the 0000 to 3FFF range; the remainder of the address space (4000 to FFFF) in each plane can have RAM, or you can leave it vacant.

Implement page addressing in four EPROMs

Address decoder IC_{2A} generates EPROM and RAM block-select signals. When address lines A_{14} and A_{15} are TTL-low, IC_{2A}'s Y_0 output goes low, enabling decoder IC_{2B}. The value in IC_3's 2-bit latch selects one 27128A. To change IC_3's value, all you need to do is write a page number (0, 1, 2, or 3) to any address within the EPROM space, 0000H to 3FFFH. IC_{2A}'s Y_0 output will be low and the Write signal, $\overline{WR}$, will strobe a new page number (data bits D_0 and D_1) into IC_3, taking advantage of the EPROM's inherently free writable address space. During write operations, the EPROMs ignore any information on the data bus.

The R_1/C_1 network solves an important program-

An 8-bit µP's 64k-byte memory capacity often can't hold enough RAM and program memory for many modern applications.

memory page-switching problem: that of boot-up initialization. At power-up, IC_3's latches are reset and page 0 is automatically selected. The microprocessor will always boot up at the same starting page.

Although it does expand the system's addressable memory, the design in **Fig 1** is not an ideal one. For one thing, putting so many devices on a board can impose capacitive and dc loading on address, data, and control lines, and can cause access-time and fanout degradation. It can also consume a lot of power and take up a lot of pc-board space. Further, the design doesn't let you easily add more program memory.

Replace four EPROMs with one

You can simplify the design by replacing the four 27128A EPROMs in **Fig 1** with a single 27512 EPROM, as shown in **Fig 2**. The 27512 contains a decoder equivalent to IC_{2B} that selects pages depending on the values of address lines A_{14} and A_{15}. Because it has fewer chips, the circuit in **Fig 2** exhibits less bus loading, consumes less power, and occupies less circuit board space than does **Fig 1**'s circuit.

Like the design in **Fig 1**, the design in **Fig 2** is not an ideal solution to the problem of expanding addressable memory: Although both these designs give your system added program memory, neither lets you easily expand the program memory further.

An ideal way to solve the problem would be to design an even simpler system that will permit future memory expansion. You can derive such a design from the circuit in **Fig 2** by replacing the circuitry inside the dashed line—latch IC_3, OR gate IC_4, the R_1/C_1 reset circuit, and the 27512 EPROM—with one 27513 or 27011 page-addressed EPROM (see **Fig 3**).

You can also derive the design in **Fig 3** directly from the circuit in **Fig 1**; this scheme lets you add address-

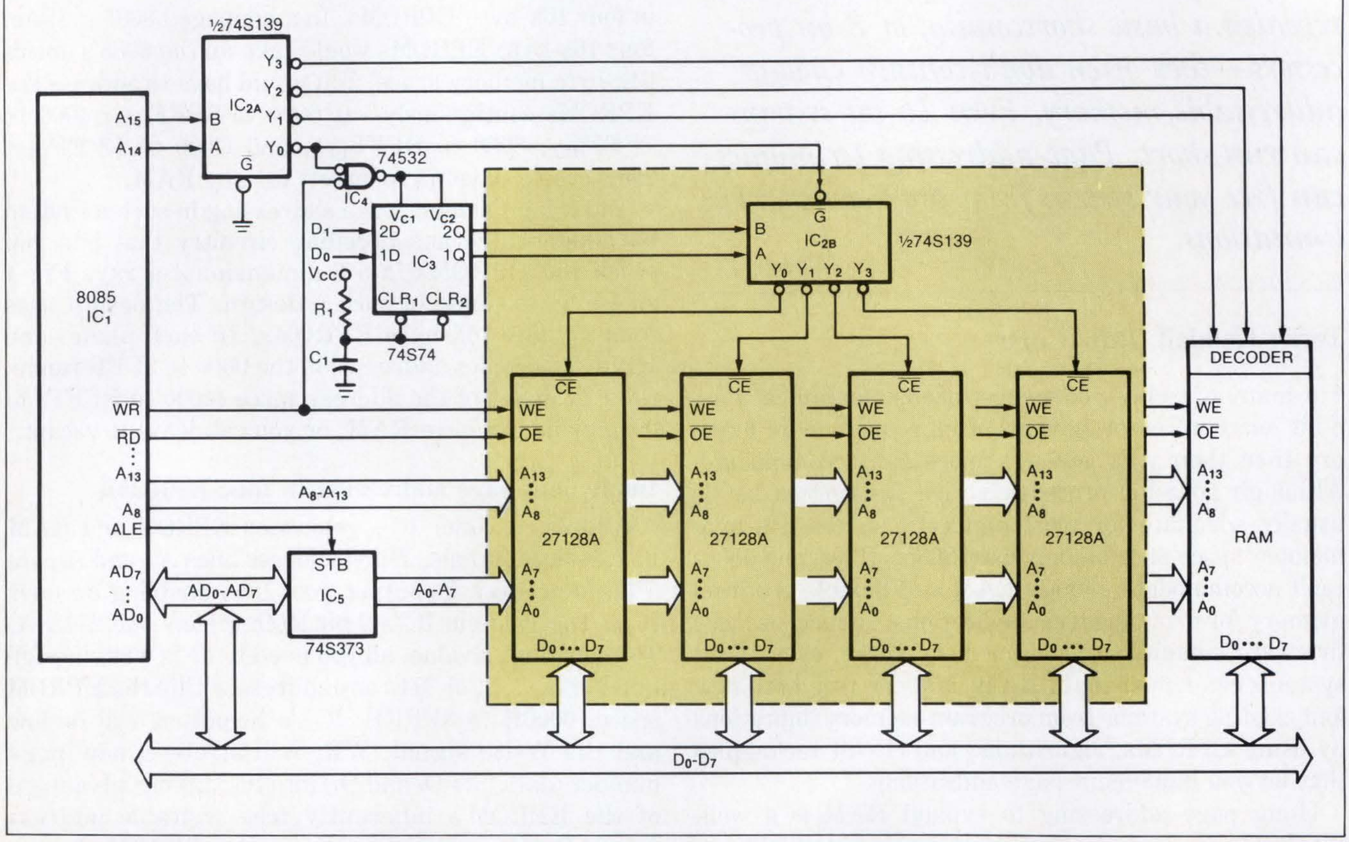

Fig 1—This block diagram of a typical 8-bit µP system *uses bank-switching techniques to provide a 3-dimensional array of EPROMs. The latch and decoding circuitry lets you select one 16k-byte EPROM bank at a time. You can reduce the amount of circuitry in the design by replacing the circuitry in the dashed box with a single 27512 EPROM.*

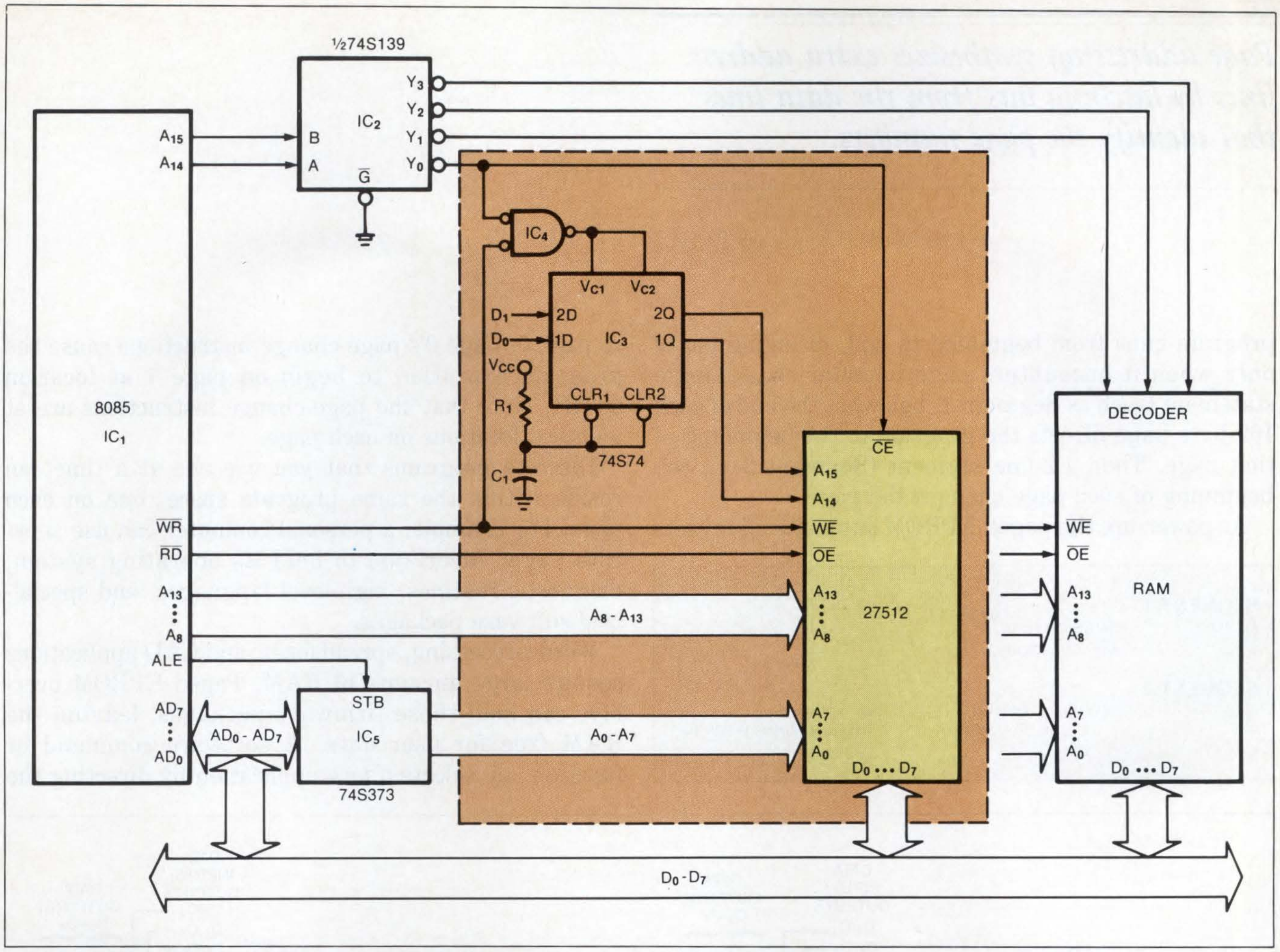

***Fig 2—By replacing the four 27128A EPROMs in Fig 1** with a single 27512 EPROM, you can implement page addressing in a simpler fashion than **Fig 1**'s circuit does.*

able memory space to an existing system without adding circuitry. You simply replace one (or each) of the 16k-bit EPROMs (and IC_{2B}, IC_3, IC_4, and the reset circuitry) in **Fig 1**'s design with a 27513 or 27011 page-addressed EPROM.

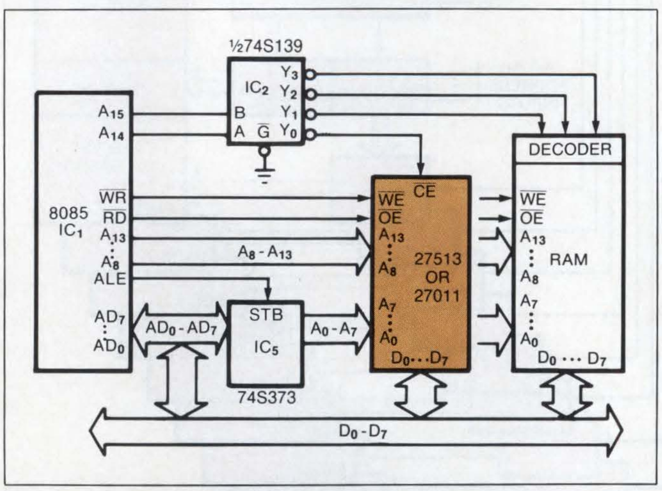

***Fig 3—By using a 27513 or 27011 paged EPROM** in place of the circuitry in the dashed box in **Fig 2**, you can both simplify your system design and provide an easily expandable memory space. This design can also be derived directly from the one in **Fig 1**: You merely replace one of **Fig 1**'s 27128A EPROMs and the paging-support circuitry with a 27513 or 27011 EPROM.*

The 64k-byte 27513 EPROM (**Fig 4a**) is organized as four 16k-byte pages. Systems requiring more program memory can use the 128k-byte, 8-page, 27011 EPROM (**Fig 4b**). These EPROMs contain latches, decoders, and reset circuitry in a single package. The 27513 and 27011 use industry-standard 28-pin DIPs (or 32-pin PLCCs) and plug into existing 27128 sites; pin 27 is wired to the $\overline{WR}$ line. Next-generation upgrades of these EPROMs (to 4M bytes) will simply plug into existing 27513 or 27011 EPROM sites.

The designs in **Figs 1, 2** and **3** all use identical page-addressing firmware. Changing pages is simple: You select the EPROM (any EPROM address will do) and write the page number, just as you would when writing data to RAM. After a page change, the first instruction on the new page must continue the logical program sequence.

Use paged EPROMs with continuous code

Page-addressable EPROMs are useful in applications that require continuous-code, discrete, and modular programs. How you write the programs that change the PROM pages depends on which of these applications you're running.

Continuous code, for example, does not use subroutines that reside on other pages. A continuous-code

Page addressing synthesizes extra address lines by latching bits from the data lines that identify the page numbers.

program runs from beginning to end, changing pages only when it encounters page boundaries. A single statement (such as **Segment 1,** below) at the end of each 16k-byte page directs the program to the beginning of that page. Then a 2-line segment (**Segment 2**) at the beginning of each page changes the page.

At power-up, the paged EPROM automatically resets to page 0. Page 0's page-change instructions cause the program execution to begin on page 1 at location 0005H. Note that the page-change instructions are at identical locations on each page.

SEGMENT 1

```
ADDRESS      STATEMENT
3FFD         JMP  CHANGEPG
```

SEGMENT 2

```
0000         CHANGEPG  MVI  A (next page number 1, 2, 3, or 0)
0002                   STA  0000H          ;write page number to EPROM.
....
```

Discrete programs that you use one at a time can reside within the same program space, one on each page. For example, a personal computer can use separate pages (overlays) to hold its operating system, diagnostic routines, high-level languages, and specialized software packages.

Word-processing, spreadsheet, and CAD applications require large amounts of RAM. Paged-EPROM overlays can hold these firmware packages, leaving the RAM free for user data. A software command or function key selects a new application by directing the

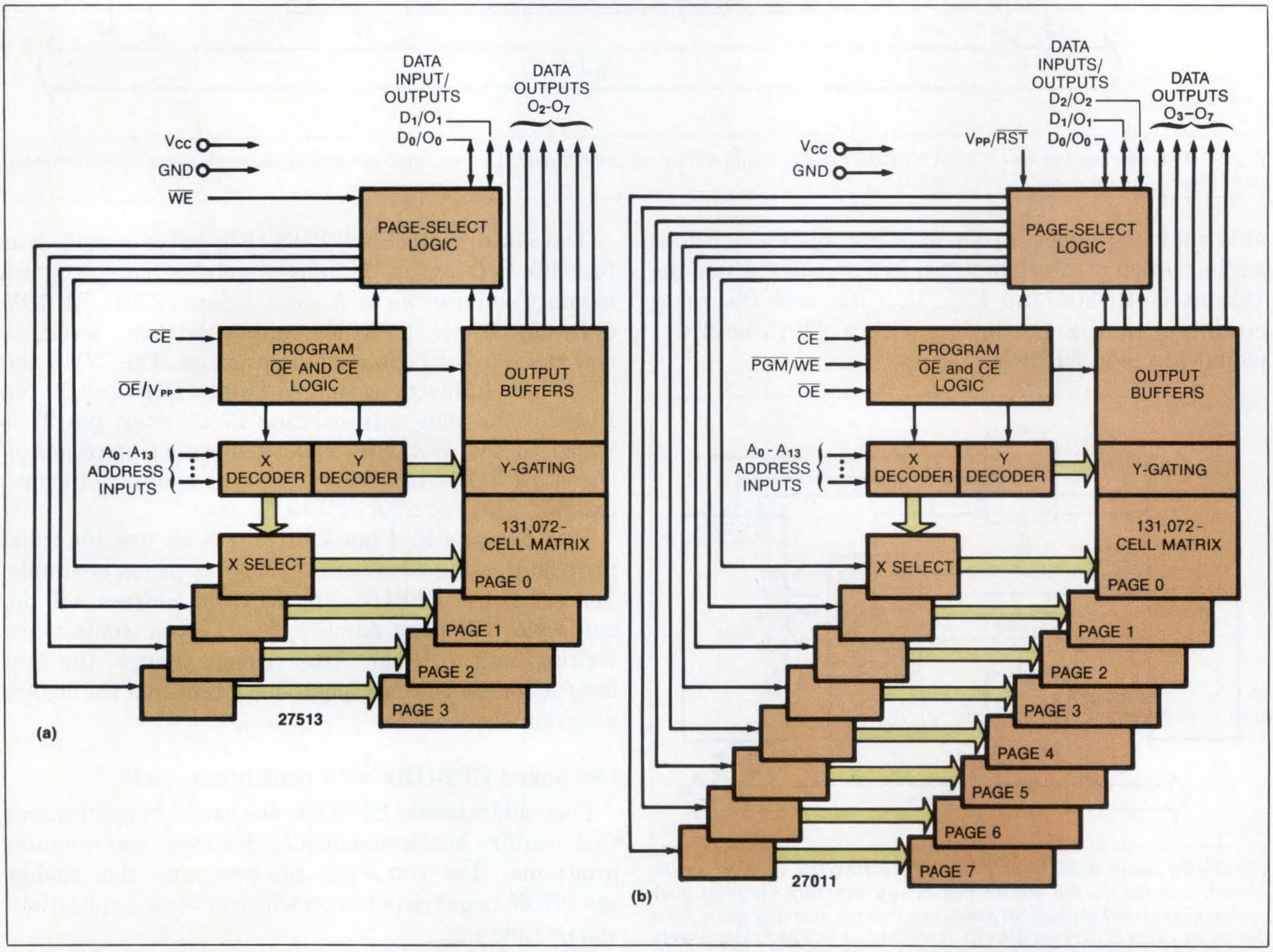

Fig 4—These paged EPROMs each provide 16k bytes per page. *The 4-page 27513 EPROM* ***(a)*** *yields a total memory space of 64k bytes; the 8-page 27011* ***(b)*** *provides 128k bytes.*

microprocessor to the routine in **Segment** 3. Each page must contain these instructions—at identical locations. After a page change, the program flow continues, uninterrupted, on the new page.

Most software is written in modular form. Subroutines call one another or are linked by a central driving routine. Calls and jumps don't access routines on another page directly; they must do so indirectly. A calling routine supplies the destination's address and page number to a universal page-turning routine. The universal Call/Jump routine accomplishes the page change and jumps to the destination.

To implement page addressing in any of the three systems illustrated, you can choose from three paging algorithms: the manual, look-up-table, and automatic paging algorithms. Although the algorithms are illustrated here by 8085 code, they adapt easily to 8-, 16-, or 32-bit systems.

SEGMENT 3

SOURCE	STATEMENT	
APPONE	LXI	H (address of page 0 application)
	MVI	M,00 ;"M"(HL register) points to EPROM, so change ;page to 0. Next instruction is on page zero.
	PCHL	;program counter gets "HL". Jump to routine.
APPTWO	LXI	H (application-two (page 1) starting address.)
	MVI	M,01
	PCHL	
etc.		

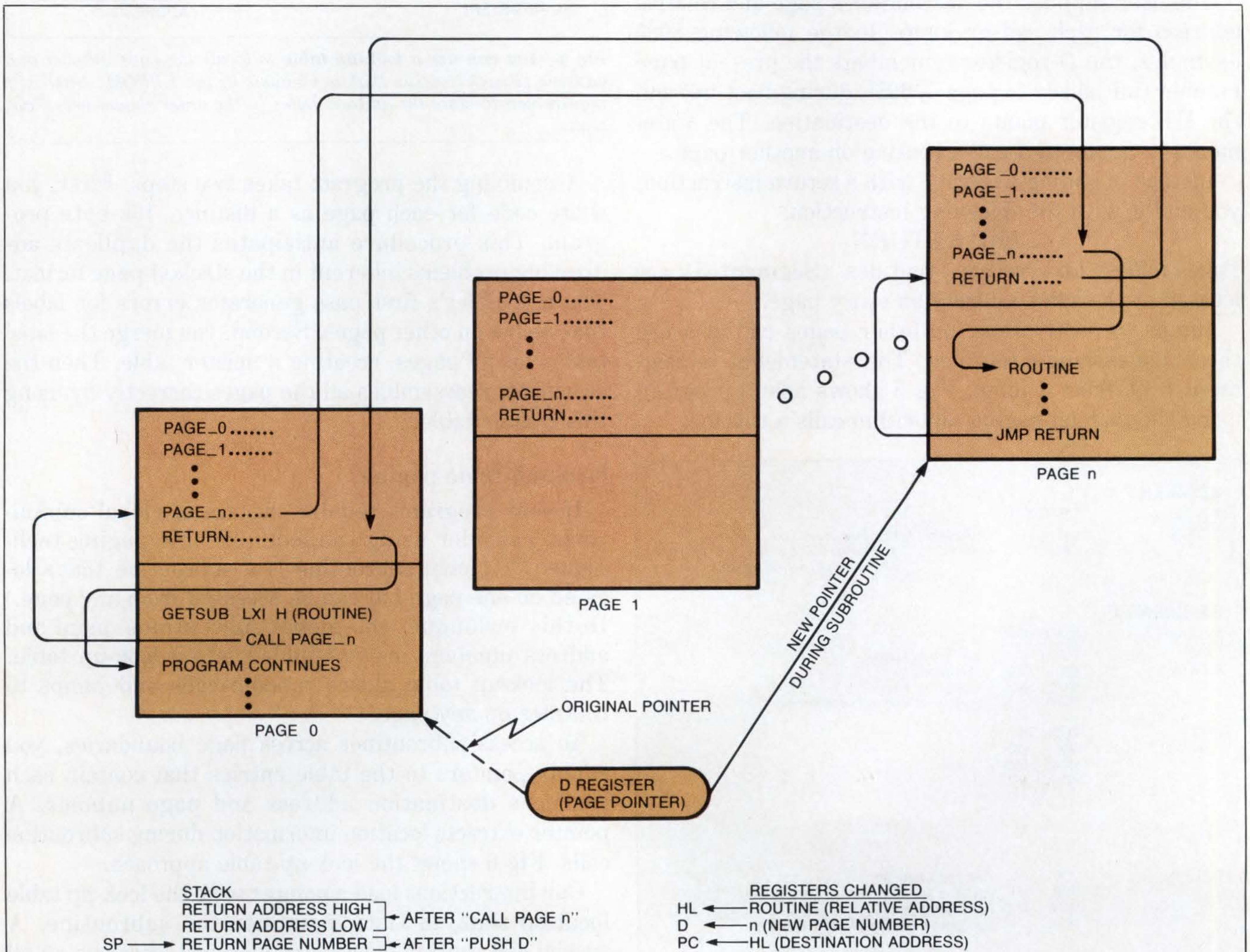

Fig 5—Manual paging requires a page-changing subroutine. *The programmer determines the page in which each routine resides and calls the paging subroutine, using the appropriate page number as an argument. This figure shows the flow of control.*

You can condense more program memory into a system by using page addressing within one EPROM instead of standard addressing within a group of EPROMs.

When you use the manual-paging algorithm, you determine the pages and relative locations for subroutines. This information is manually placed in Call instructions, which access subroutines on other pages. Manual paging is an easily understood approach that lets you change pages quickly and allows you to upgrade easily to higher-density EPROMs. It does have certain disadvantages, however. For one thing, you must know the page and relative location of every call and jump. Further, the assembler has difficulty in assigning addresses to labels that are referenced in overlapping memory pages.

The user supplies the destination's page and relative address for each call or jump. In the following 8085 examples, the D register remembers the present page number (initialized to page 0, 00H, during boot-up) and the HL register points to the destination. The statements in **Segment 4** call a routine on another page.

Instead of ending a routine with a return instruction, you end it with the following instruction:

JMP RETURN

Page-change and return routines (**Segment 5**) are located at the same address on every page.

Jumps to destinations on other pages can also use these page-change routines. The statements in **Segment 6** perform a jump. **Fig 5** shows how a program using the manual-paging algorithm calls a routine.

SEGMENT 4

```
SOURCE      STATEMENT
GETSUB      LXI    H(routine)  ;"HL" gets destination.
            CALL   PAGEn       ;call paging routine (n = 0, 1, 2, . . .) that
                               ;turns to the subroutine's page.
```

SEGMENT 5

```
SOURCE      STATEMENT
PAGE0       PUSH   D     ;save present page.
TURNTO0     MVI    D,00  ;new page.
            MOV    M,D   ;change the page.
            PCHL         ;program counter gets destination.

PAGE1       PUSH   D
TURNTO1     MVI    D,01
            MOV    M,D
            PCHL
      o
      o
      o
RETURN      POP    D     ;retrieve old page.
            POP    H     ;retrieve return address.
            MOV    M,D   ;change page.
            PCHL         ;program counter gets return address.
```

SEGMENT 6

```
            LXI    H(destination)  ;"HL" gets destination's address.
            JMP    TURNTOn         ;jump to paging routine (n = 0, 1, 2, . . .).
```

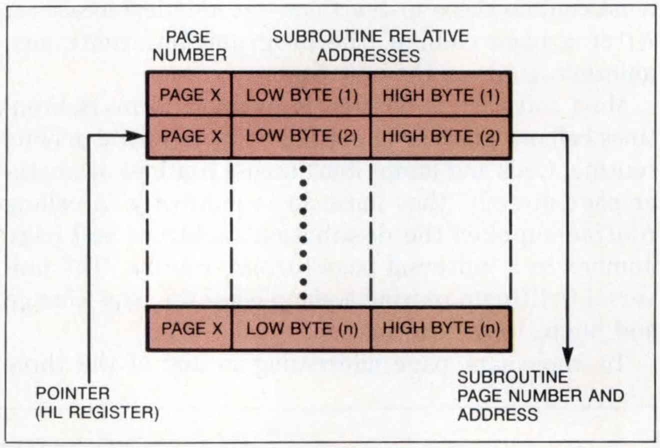

Fig 6—You can use a look-up table *to locate the page number and address of each routine that is resident in the EPROM. Intel μPs require you to store the address bytes in the order shown here (low, high).*

Assembling the program takes two steps. First, you write code for each page as a distinct, 16k-byte program. This procedure anticipates the duplicate-addressing problems inherent in the stacked-page format. The assembler's first pass generates errors for labels that reside on other pages. Second, you merge the label tables for all pages, creating a master table. Then the assembler reassembles all the pages correctly by using this master table.

Look-up-table paging

If your programs require the use of global subroutines, consider using the look-up-table paging technique. (A global subroutine is a subroutine that's located on one page but can be accessed from any page.) In this technique, the global subroutines' page and address numbers are assembled into a look-up table. The look-up table allows random calls and jumps to routines on any page.

To access subroutines across page boundaries, you supply pointers to the table entries that contain each routine's destination address and page number. A pointer extracts location information during subroutine calls. **Fig 6** shows the look-up-table approach.

Call instructions load a pointer with the look-up table location that, in turn, points to the subroutine. A special call routine existing at identical locations on all pages extracts the page and relative address by using the pointer. It then changes the page and jumps to the destination. A return routine transfers control to the

To implement page-addressing, you can choose from three paging algorithms: manual paging, a look-up-table method, and automatic paging.

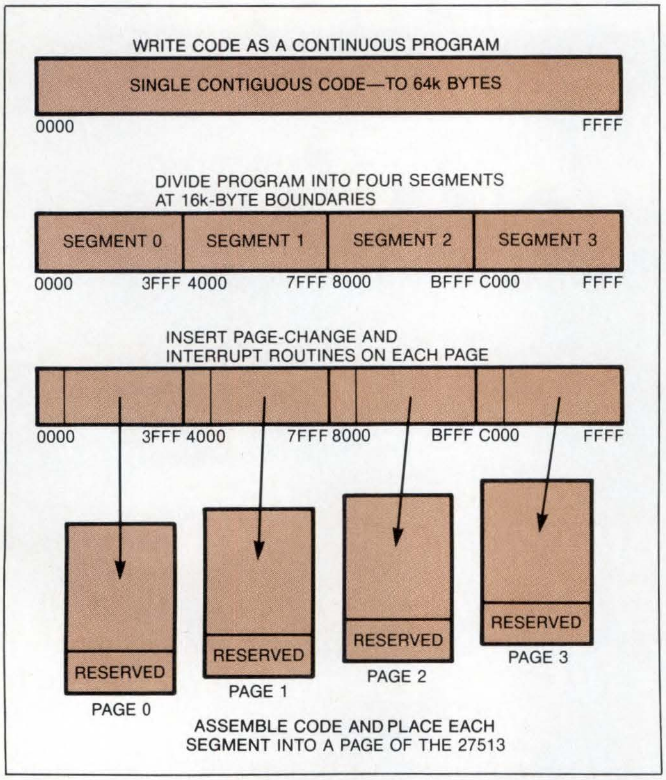

Fig 7—Automatic paging lets you write continuous code. *After assembling the code, you must break it into 16k-byte segments, each of which has a page-changing routine at the end.*

calling routine's page and relative address. **Segment 7** illustrates this technique.

A pagecall routine **(Segment 8)** extracts page and address information from the table. The JMP RETURN instruction at the end of a subroutine replaces the return instruction. Jumps between pages use the statements in **Segment 9.**

Each entry in the look-up table contains three bytes for page and address information. Thus, call and jump instructions supply labels that point to table entries for each routine. During program assembly, the assembler substitutes absolute addresses for the labels, and then places the addresses and page numbers in the table.

Automatic paging uses an index register

The automatic-paging algorithm allows you to write as many as 64k bytes of code in one block; however, the subroutine calls take place indirectly through an index register. Thus, the index register serves as a page and address pointer to subroutines. This algorithm uses a destination's two most significant address bits (as determined by the assembler) to determine the page number. A paging routine separates the page number and the relative address from the 16-bit destination address. **Fig 7** shows how the single block of assembled code fits into the four separate pages.

Each page must contain page-change and interrupt routines to connect the segments. **Segment 10** shows 8085 code for calling a subroutine via the automatic-paging method. Reset and interrupt routines, as well as paging routines **(Segment 11),** are placed at identical locations on each page **(Fig 7).** Destination addresses are loaded into the HL register. The pagecall/pageturn routine (**Segment 11**) performs "bit stripping," which handles page selection and relative addressing. Although the program memory appears to overlap the RAM, the bit-stripping procedure ensures that each occupies its unique location.

In sum, the paging routine performs four functions: It saves the old page number, isolates the two most

SEGMENT 7

```
SOURCE      STATEMENT
GETSUB      LXI   H,SUBPTRn  ;"HL" points to page information in table.
            CALL  PAGECALL   ;enter global call routine.
```

SEGMENT 8

```
PAGECALL    PUSH  D     ;save old page number.
PAGETURN    MOV   D,M   ;"D" gets new page.
            INX   H     ;point to destination's low byte.
            MOV   E,M   ;"E" gets low byte.
            INX   H     ;point to destination's high byte.
            MOV   H,M   ;"H" gets high byte.
            MOV   L,E   ;"L" gets low byte.
            MOV   M,D   ;change page.
            PCHL        ;jump to routine.

RETURN      POP   D     ;retrieve old page.
            POP   H     ;"HL" gets return address.
            MOV   M,D   ;change the page.
            PCHL        ;return to main program.
```

SEGMENT 9

```
            LXI   H,JMPPTRn  ;"HL" gets table location.
            JMP   PAGETURN   ;enter global call routine.
```

SEGMENT 10

```
SOURCE      STATEMENT
GETSUB      LXI   H,routine  ;"HL" gets destination, as determined by the
                             ;assembler.
            CALL  PAGECALL   ;call the paging routine.
```

SEGMENT 11

```
PAGECALL    PUSH  D           ;save old page.
PAGETURN    PUSH  PSW         ;save anything in accumulator.
            MOV   A,H         ;"A" gets high address byte.
            RLC   A           ;rotate two most significant bits to
            RLC   A           ;least significant locations.
            ANI   00000011B   ;mask all but page-number bits.
            MOV   D,A         ;"D" gets page number.
            MVI   A,00111111B ;"A" gets relative location mask.
            ANA   H           ;strip most significant bits from "H".
            MOV   H,A         ;"H" gets high relative-address byte.
            MOV   M,D         ;change to new page.
            POP   PSW         ;"A" retrieves old information.
            PCHL              ;jump to subroutine.

RETURN      POP   D           ;retrieve old page number.
            POP   H           ;"HL" gets return address.
            MOV   M,D         ;change page.
            PCHL              ;return to program.
```

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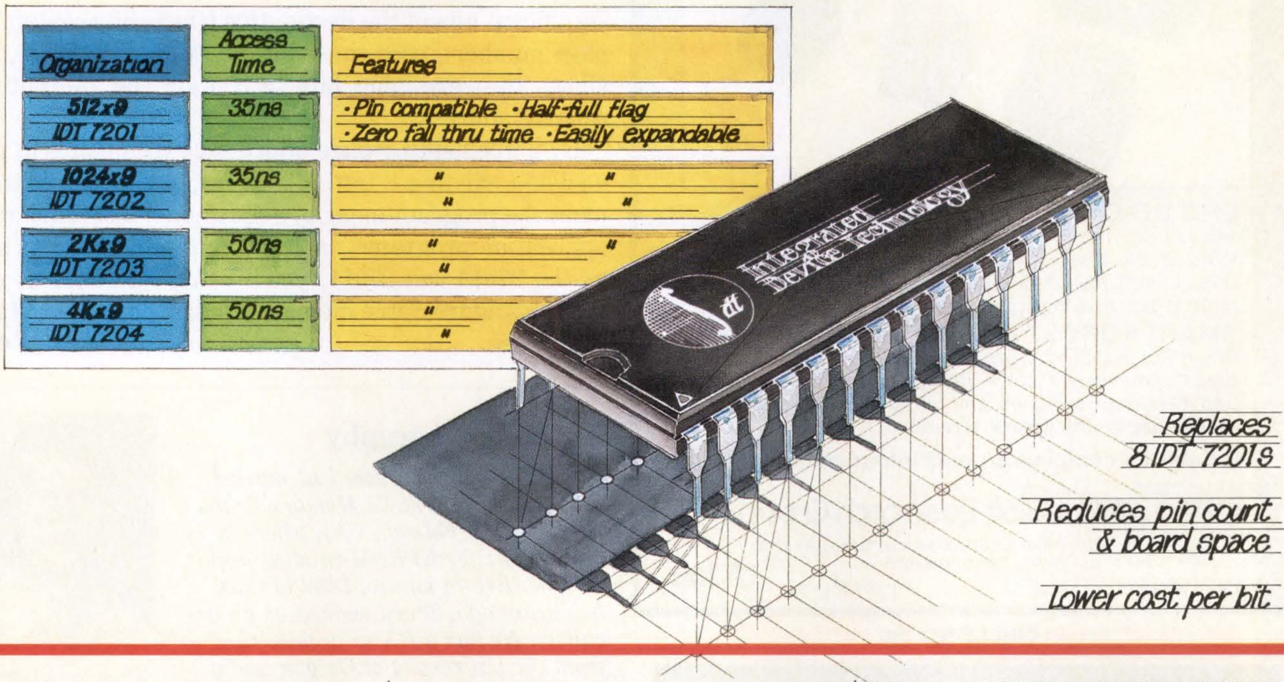

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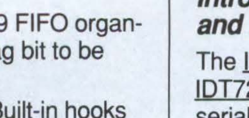

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significant bits of the destination (these bits contain the page number), uses these bits to change the page, and allows the remaining bits to contain the subroutine's relative address.

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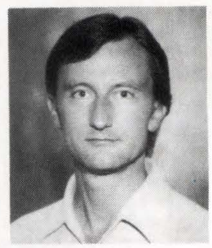

Terry Kendall is a technical marketing engineer at Intel's Memory Components Div (Folsom, CA), where he is responsible for EPROM-product applications. Before joining Intel almost two years ago, Terry worked as an architect. He has a BA in architecture from the University of Oregon and a BSEE from California State University at Sacramento. In his spare time, Terry enjoys skiing, backpacking, and playing the guitar.

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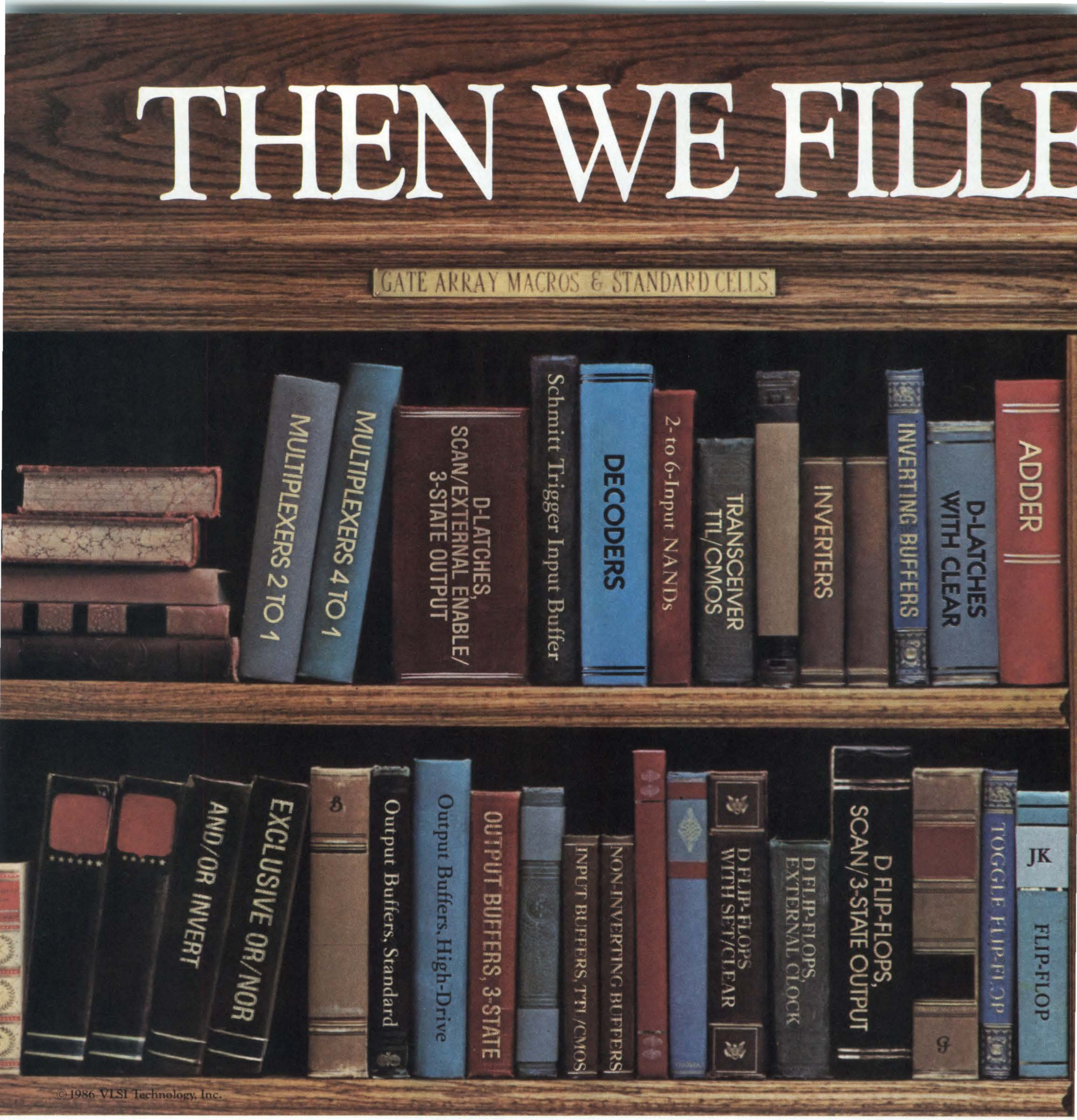

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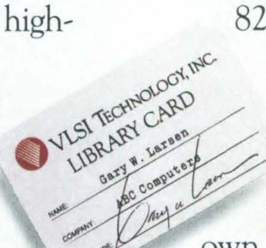

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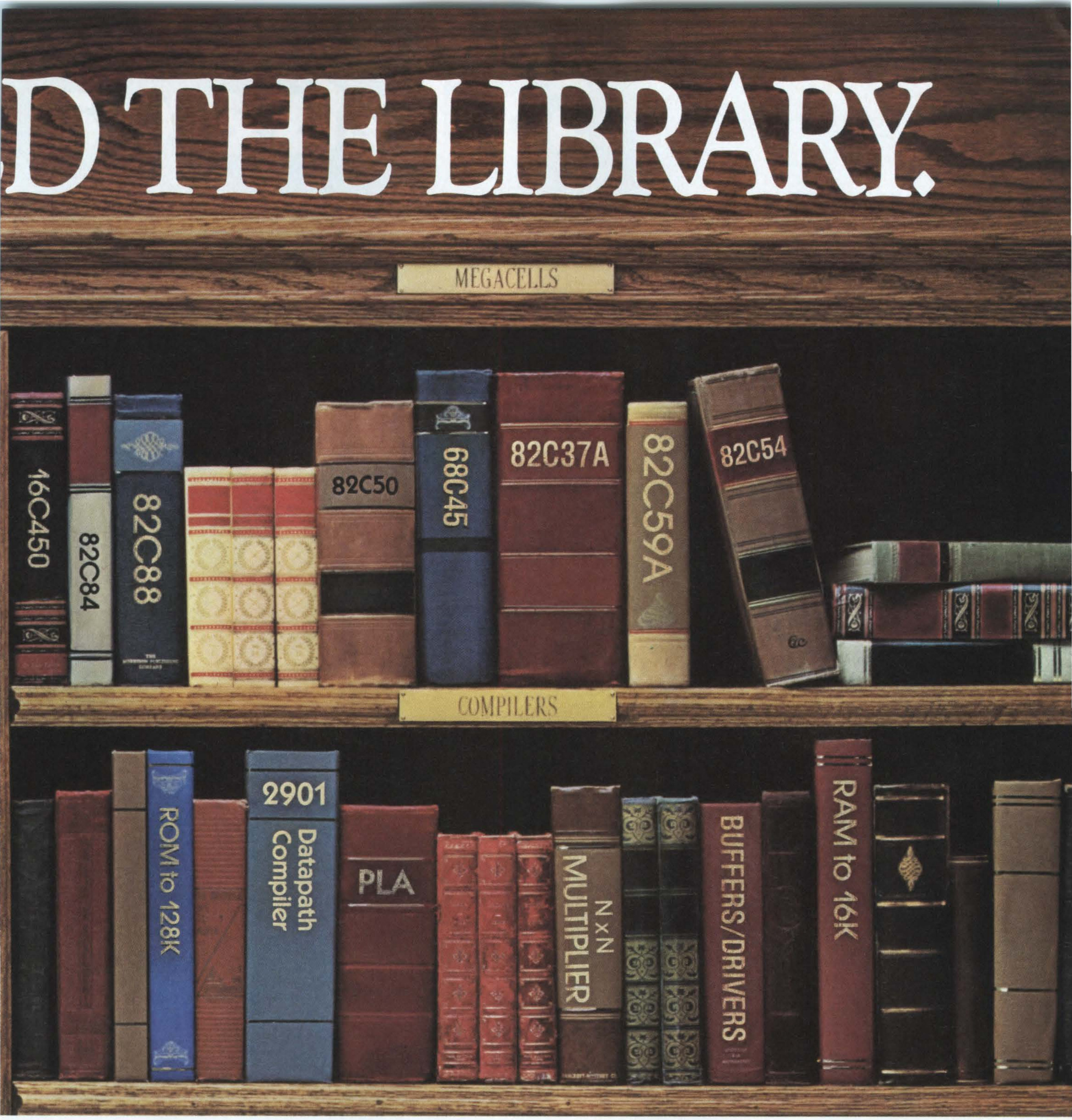

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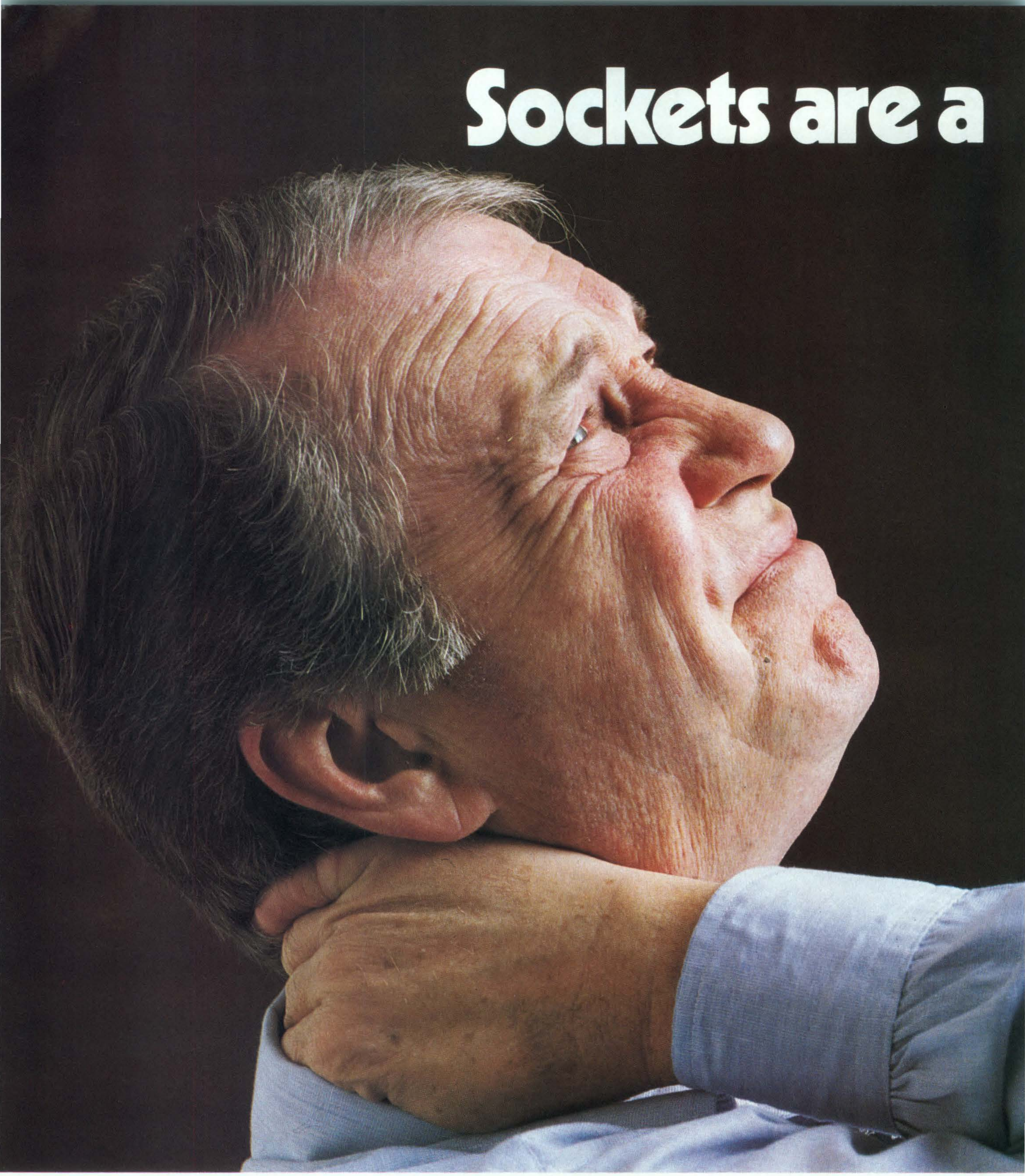

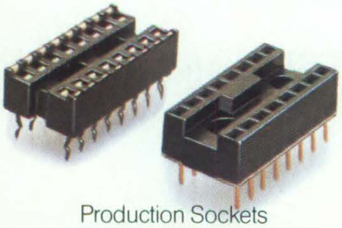

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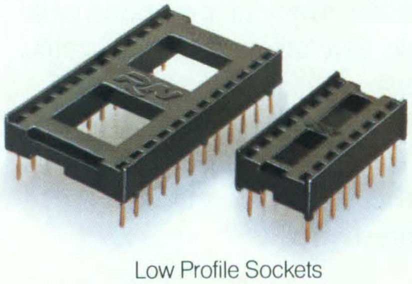

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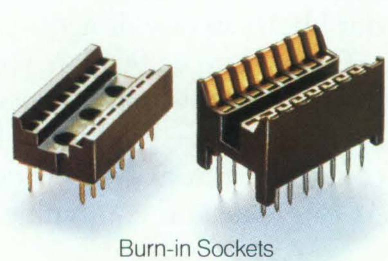

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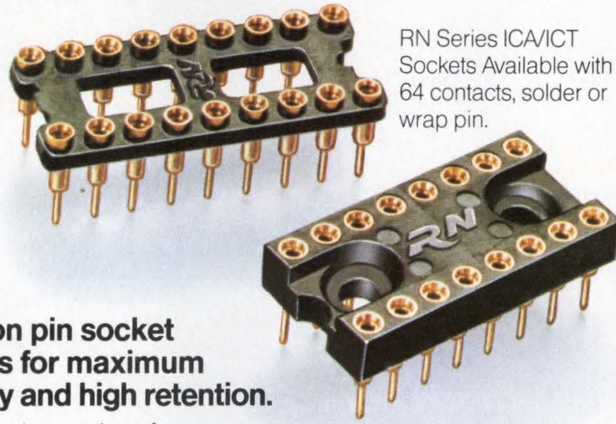

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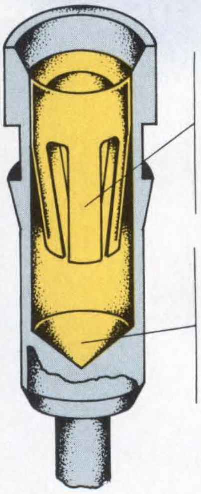

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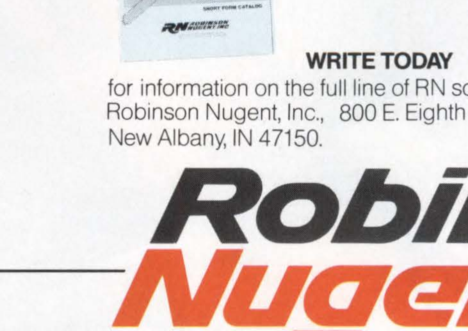

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Consider standard features when selecting codecs

A codec—or coder/decoder—performs analog-to-digital (encoding) and digital-to-analog (decoding) conversion of the human voice. This article, part 1 of a 2-part series, provides an overview of a codec's structure and function and brings you up to date on the standard features that you can expect these workhorses of the telecommunications network to offer. Part 2, scheduled for the May 14 issue, will look at the advanced features offered by several codecs and will discuss noise considerations.

Brady Barnes, *Inter-Tel*

With the advent of ISDN (the Integrated Services Digital Network), the use of codecs is becoming increasingly widespread. Although different types of codecs fit different types of applications—for example, codecs may differ in their encoding (linear vs nonlinear), their word size (eight bits vs 16 bits), and their bit rate—their primary application is, of course, in the telecommunications industry. This 2-part series focuses on that type: the type now commonly being used in the transmission and switching of voice in digital systems and networks. Furthermore, it discusses only those codecs that have their own on-chip filtering: These codecs are often called codec/filter combos or, sometimes, cofidecs. Here, however, they're referred to simply as codecs.

The codec can be divided into two sections: the transmit and the receive sections (**Fig 1**). The transmit section performs the analog-to-digital conversion; the receive section performs the digital-to-analog conversion.

When an analog signal is applied to the transmit section of a codec, the signal passes through a series of filters: A highpass filter rejects all low-frequency noise, such as 60-cycle hum. Then, a lowpass, antialiasing filter eliminates all frequencies greater than one-half the sampling rate so as to avoid a phenomenon called "foldover distortion," or aliasing. The net result for codecs designed for voice transmission over digital telecommunications links is an analog signal that's band-limited from about 300 Hz to about 3400 Hz.

Next, the analog signal enters the sample/hold circuit of the encoder. The encoder performs the analog-to-digital transformation. Inside the encoder, the analog signal is sampled at a rate of 8000 samples/sec (once every 125 μsec). The sample is then converted to an 8-bit digital word, yielding a 64k-bps serial data rate. The data conversion is not uniform (that is, not linear); instead, the codec performs the conversion in accordance with a companding (compressing/expanding) characteristic. The codec's compander circuit compresses the dynamic range of the input and expands the signal back to its original form on the output.

Although companding serves several purposes, its

The codec's data conversion is not linear; instead, the codec performs the conversion in accordance with a companding characteristic.

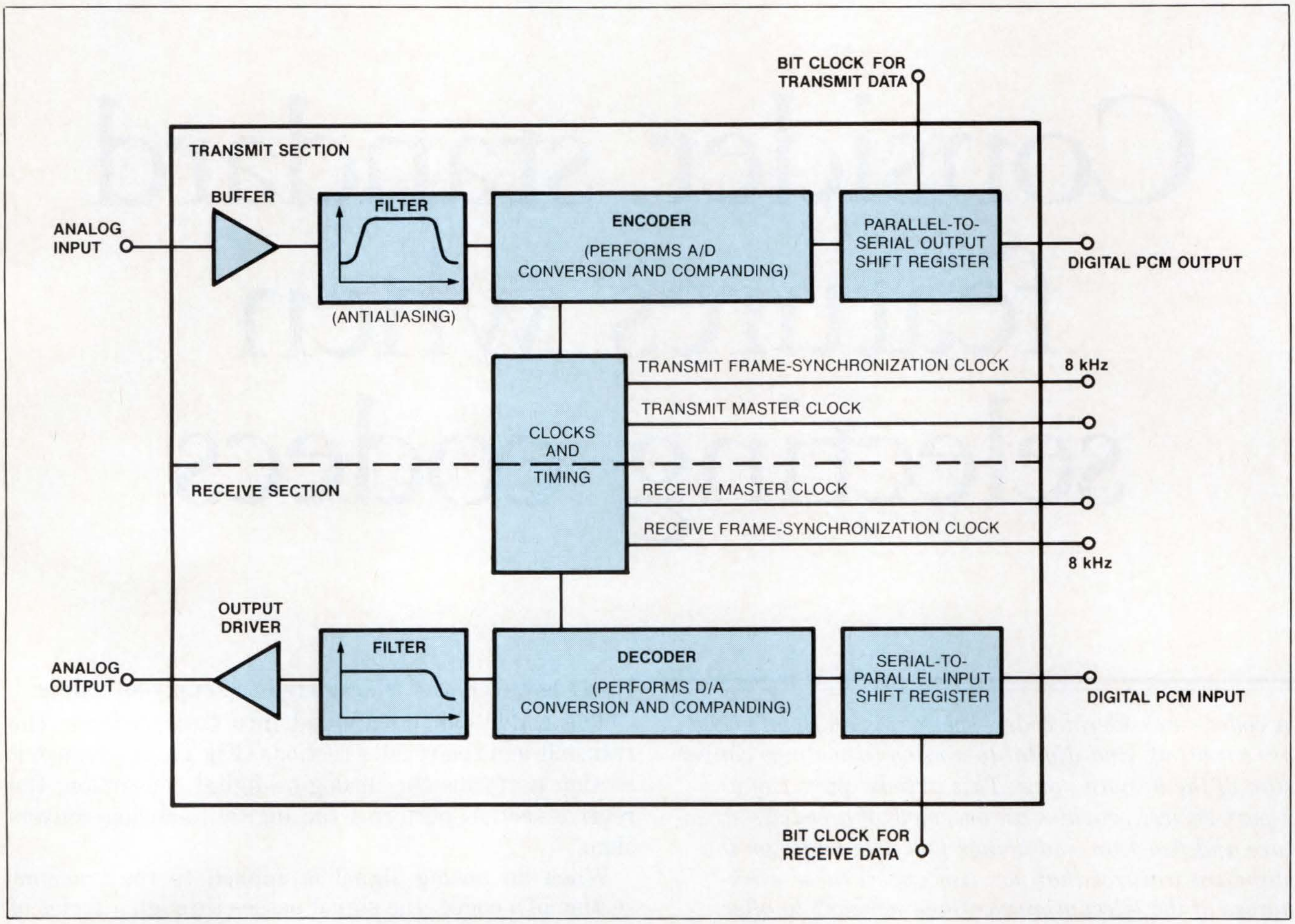

Fig 1—A single-chip codec/filter combination *consists of a transmit section and a receive section.*

most important function is to enhance the codec's signal-to-noise ratio and dynamic-range capability.

To understand companding's effect on S/N ratio, consider that although a codec's analog-input signal can take on a theoretically infinite number of amplitudes, the codec's corresponding 8-bit digital output can take on only 256 discrete values. That is, the codec's transformation of an analog signal to a digital value is only an approximation. The error introduced by the approximation is called the quantization error; if this error is large enough, the listener can hear it as distortion.

Linear encoding yields unfavorable SQR

For example, if the digital numbers 1, 2, 3, and so on correspond to the analog levels 1 mV, 2 mV, 3 mV, and so on, the quantization error is ½ mV. As you would expect, that ½-mV error on a signal of 100 mV is much less noticeable than the same ½-mV error on a signal of only 1 mV. The ratio of signal amplitude to quantizing noise is called the signal-to-quantizing noise ratio, or just SQR.

Thus, for an encoder that uses a uniform (that is, linear) transformation, the larger (louder) signals will have a much better SQR than the smaller (quieter) signals. This situation is undesirable because loud signals tend to obscure not only quantizing noise but any other noise that's present as well, and noise due to any source is much more noticeable when the signals are quiet. Furthermore, small signals tend to occur more often than large signals during a normal phone conversation. The solution is to use proportionately smaller quantizing interval sizes for the smaller signals and to use proportionately larger quantizing interval sizes for the larger signals. Thus, the SQR will remain approximately constant over the entire amplitude range.

Changing the quantizing interval size with respect to the amplitude of the input signal is called nonlinear (or nonuniform) transformation, and is the function of the

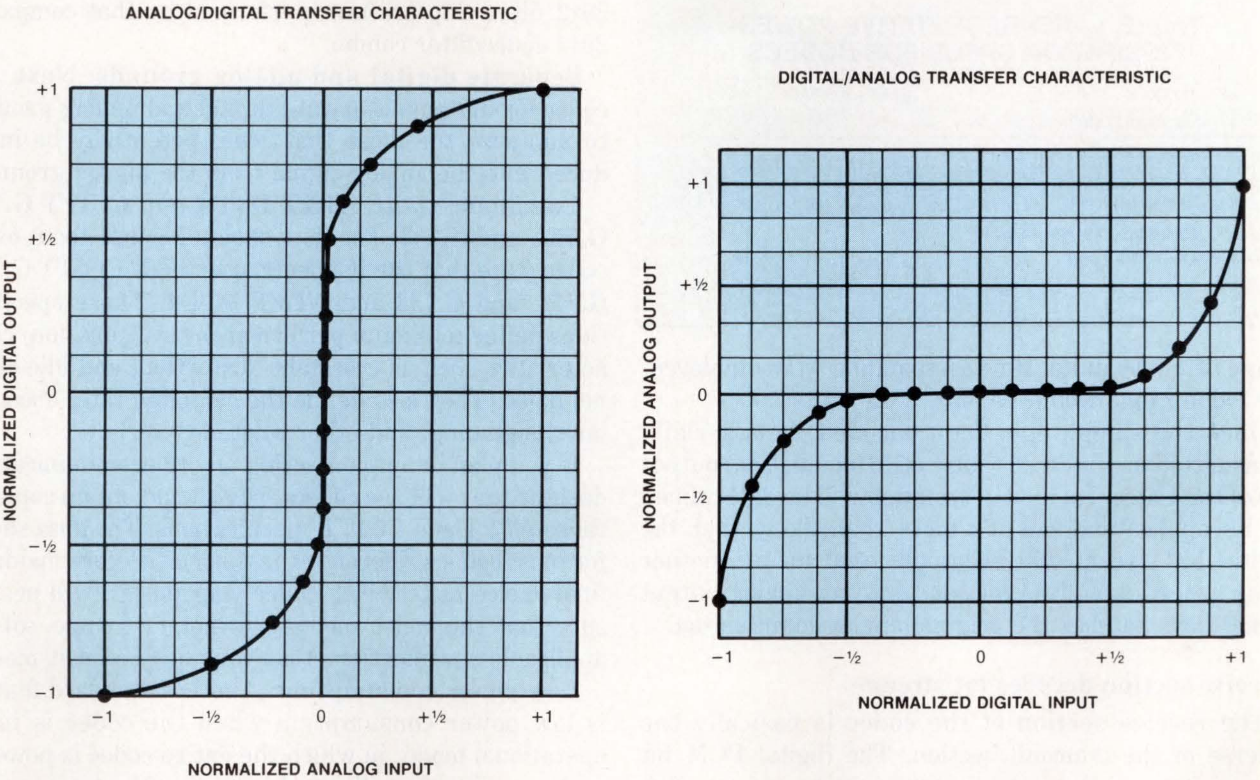

Fig 2—The μ-law characteristic, *which finds use in North America and Japan, exhibits lower idle-channel noise than does the A-law, which is used in Europe. However, the A-law characteristic produces a slightly better S/N ratio for small signals. The differences between the μ-law and A-law curves are subtle.*

companding circuit. In essence, it involves compressing the signal.

The two accepted companding characteristics in the telecommunications industry are the μ-law and the A-law characteristics. The μ-law is the standard for the North American and Japanese telephone networks, whereas the A-law is the standard in Europe. The primary difference between the two companding characteristics is that the μ-law has an associated lower idle-channel noise, and the A-law produces a slightly better S/N ratio for small signals. The transfer curves for the μ-law are shown in **Fig 2.**

The A-law companding curves are similar, but subtle differences do exist, as the curves' equations suggest. For a normalized input x between −1 and +1, the μ-law would result in the following output f(x):

$$f(x) = \mathrm{sgn}(x)\left[\frac{\ln(1 + \mu|x|)}{\ln(1 + \mu)}\right],$$

where μ, the compression parameter, equals 255. For the same input, the A-law would yield

$$f(x) = \mathrm{sgn}(x)\left[\frac{A|x|}{1 + \ln(A)}\right] \text{ for } 0 \le |x| < \frac{1}{A};$$

$$f(x) = \mathrm{sgn}(x)\left[\frac{1 + \ln(A|x|)}{1 + \ln(A)}\right] \text{ for } \frac{1}{A} \le |x| < 1,$$

where the compression parameter A equals 87.6. (Recall that the function sgn***x*** equals +1 when ***x*** is positive and −1 when ***x*** is negative.) Although these functions are smooth, continuous functions, codecs implement them by using a piecewise-linear approximation.

One final note about companding: Besides providing a nearly constant SQR over the entire amplitude range, it also provides a much wider dynamic range than would a linear encoder. In fact, the μ-law provides a value range of ±8159 units, and the A-law provides a value

Small signals tend to occur more often than large signals during a normal phone conversation.

TABLE 1—REPRESENTATIVE POWER-DISSIPATION SPECS FOR CODECS

DESCRIPTION	BEST	AVERAGE	WORST
TYPICAL OPERATING POWER (mW)	30	70	140
MAXIMUM OPERATING POWER (mW)	40	115	240
TYPICAL POWER-DOWN AND/OR STANDBY POWER (mW)	0.1	5	20
MAXIMUM POWER-DOWN AND/OR STANDBY POWER (mW)	1.0	14	60

range of ±4096 units. If no companding were employed, the value range would be only ±128 units.

Once the sample has been encoded, it is serially transmitted on the PCM (pulse code modulation) output pin of the codec. Its final destination will be determined by its application, but it's more than likely that the digital bit stream will eventually end up at another codec where it will be decoded into an analog output signal that matches the original analog input signal.

Receive section decodes bit stream

The receive section of the codec is basically the reverse of the transmit section. The digital PCM bit stream is applied to the receive section, whose D/A converter decodes 8000 8-bit words per second. The decoder also performs the expansion necessary for restoring the compressed signal to its original form. The filtering performed in the receive section eliminates the high-frequency switching signals from the analog output. The final stage of the codec is typically a balanced (or unbalanced) line driver capable of driving a 600Ω load.

$4 to $6 devices offer standard features

With respect to features, the vast majority of codecs can be grouped into two categories: standard and advanced. In general, codecs that offer just the standard features cost somewhere between $4 and $6 each in quantities of 10,000. Codecs that offer advanced features usually fall in the $7 to $9 range.

The standard features described in the following section are common to just about every codec on the market:

Combination codec and filter on one chip: First, the codec that you choose should actually be a codec/filter combo. Previously, the filtering was done by a separate chip, and consequently, you needed a 2-chip set in order to perform the codec/filter function. For example, the functions of Intel's 2910 codec chip and 2912 filter chip are now performed by that company's 2914 codec/filter combo.

Separate digital and analog grounds: Next, the codec should have separate digital and analog grounds to minimize the noise that could potentially be introduced into the analog signal from the digital ground.

Compliance with AT&T D3/D4 and CCITT G.711, G.712, and G.733: The data sheets for just about every codec state that the IC meets or exceeds CCITT G.711, G.712, and G.733 and AT&T D3/D4. These specifications define minimum performance (transmission) characteristics such as crosstalk, distortion, and idle-channel noise. They also define the sampling rate, encoding laws, signaling, and other related criteria.

If you plan on implementing any telecommunications designs that will use codecs, you should obtain copies of these AT&T and CCITT specifications. The data sheets for most codecs reference these specs. Before making a final choice as to which codec your design will use, be sure that the codec meets *all*—not just some—of the applicable specifications that your design must meet.

Low power consumption: Another standard feature is low power consumption when the codec is in its operational mode, in which the entire codec is powered and encoding/decoding takes place. Most codecs are manufactured with CMOS technology; consequently, it's common to see operating-power requirements ranging from 50 to 100 mW.

Power-down or standby mode or both: Every codec has at least one mode in addition to the operating mode, and some even have two additional modes. These modes, which are called standby or power-down modes, usually cause the codec's power requirement to drop to somewhere between 1 to 20 mW. These low-power modes are implemented via control of an input pin or, on some advanced codecs, via control codes sent to the codec under software control.

The terms "standby" and "power-down" have different meanings for different manufacturers, and "standby" for one codec may mean exactly the same thing as "power-down" for another. Furthermore, some codecs support both a standby and a power-down mode. The important point to keep in mind is that these additional modes provide the user with a means of conserving power when the codec is not in use. And although such modes are standard on codecs, the actual power consumption in these modes (as well as in the operating mode) varies widely among the various devices. The power-consumption ranges shown in **Table 1** were ob-

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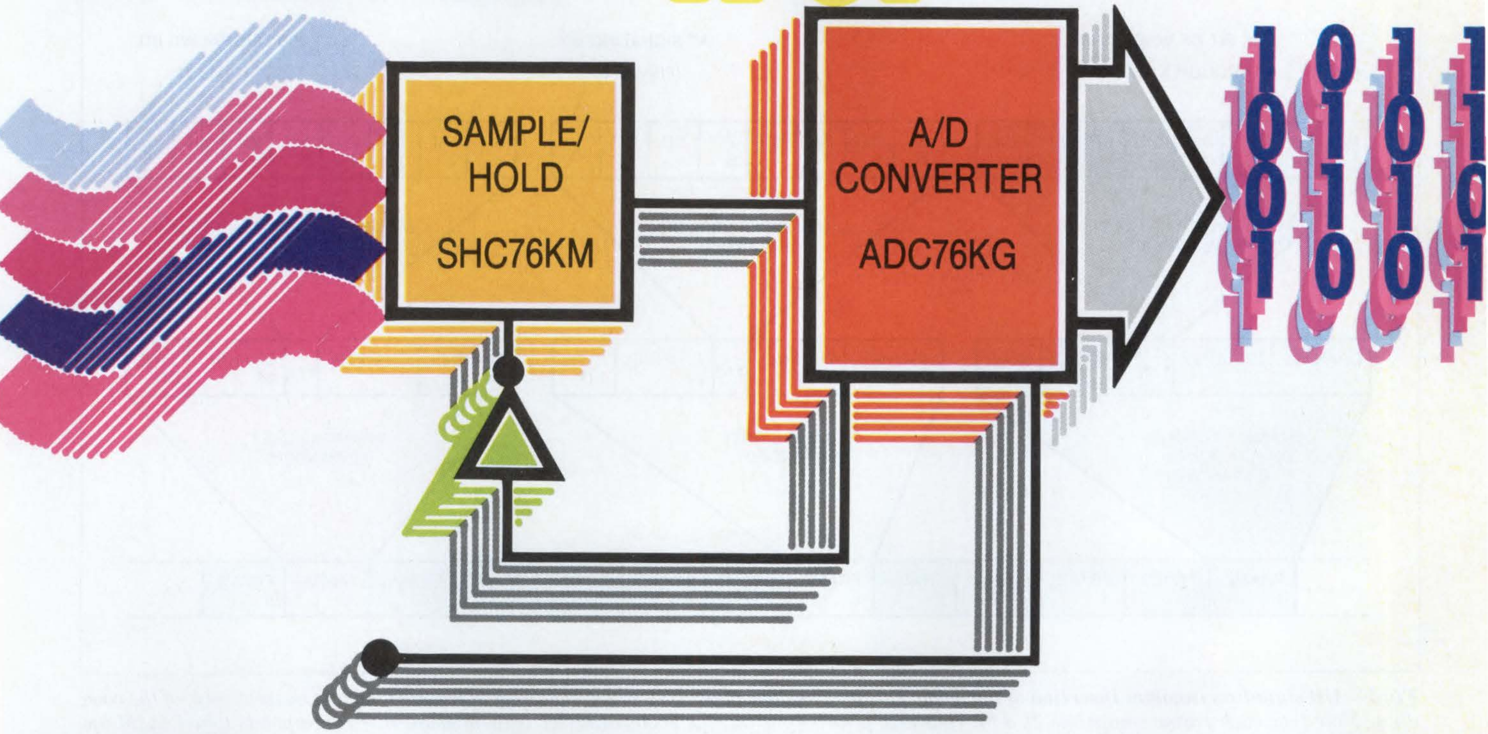

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The μ-law characteristic is the standard for the North American and Japanese telephone networks, whereas the A-law is the standard in Europe.

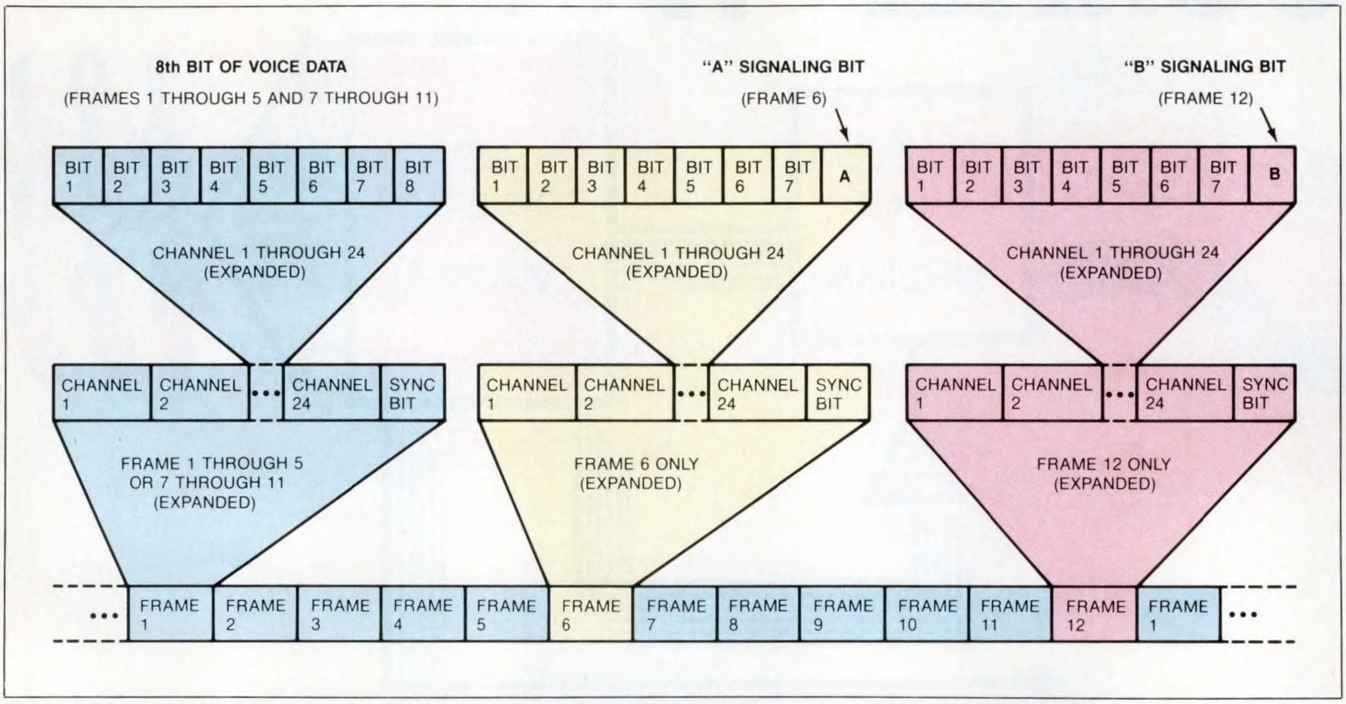

***Fig 3—A/B signaling involves insertion** of the A and B signaling data in the LSB of each channel in frames 6 and 12, respectively, of the voice data. Note that each frame comprises 24 8-bit channels plus a sync bit; the 8000-frame/sec transmission rate corresponds to a 1.544M-bps rate.*

tained from a survey of 20 codecs. (Most, but not all, were CMOS; for devices offering both power-down and standby modes, the mode offering the lower power consumption was used.)

Stable, on-chip voltage reference: Just about every codec has its own internal voltage reference or references for performing the A/D or D/A conversion. The voltage references determine, in part, the gain and dynamic-range characteristics of the codec. A few codecs allow you either to provide an external reference or to use an on-chip reference, and at least one codec requires an external reference. Normally, it's desirable to eliminate this external circuitry and select a codec that already has the voltage references built in. Nevertheless, you might encounter a special application that would benefit from an external voltage reference.

Low external parts count: Another standard feature to expect is a low external parts count. Most codecs require from zero to four external parts, such as resistors and capacitors. These external parts are typically used for setting a fixed transmit gain. The need for few external parts makes the design engineer's job almost trivial when he or she is designing these codecs into large systems.

Autozero circuit: The autozero circuit cancels any dc offset that may be present on the input signal to the encoder. The technique used to perform the autozero function is referred to as the sign-bit averaging technique. The sign bit from the output of the encoder is long-term averaged and subtracted from the input to the encoder. In this manner, any long-term dc offset is canceled. At least one codec allows the user to enable or disable autozero operation by simply adding or removing a 0.1-μF capacitor between two pins.

A-law and μ-law selection: Codec manufacturers allow you to select between the μ-law and the A-law companding characteristics in one of three ways. First, many manufacturers offer the same codec in either the μ-law or the A-law version. The pinouts are identical; should the need arise, you could switch from one companding characteristic to the other simply by swapping parts. Second, some manufacturers offer codecs that each include an input pin that you can drive high or low to select one characteristic or the other. Finally, some codecs—only the more advanced ones—allow you to use software codes to select the characteristic you want.

Power-supply operation of ±5V dc: The standard power-supply voltages for codecs tend to be ±5V dc, as you would expect, because codecs must interface with

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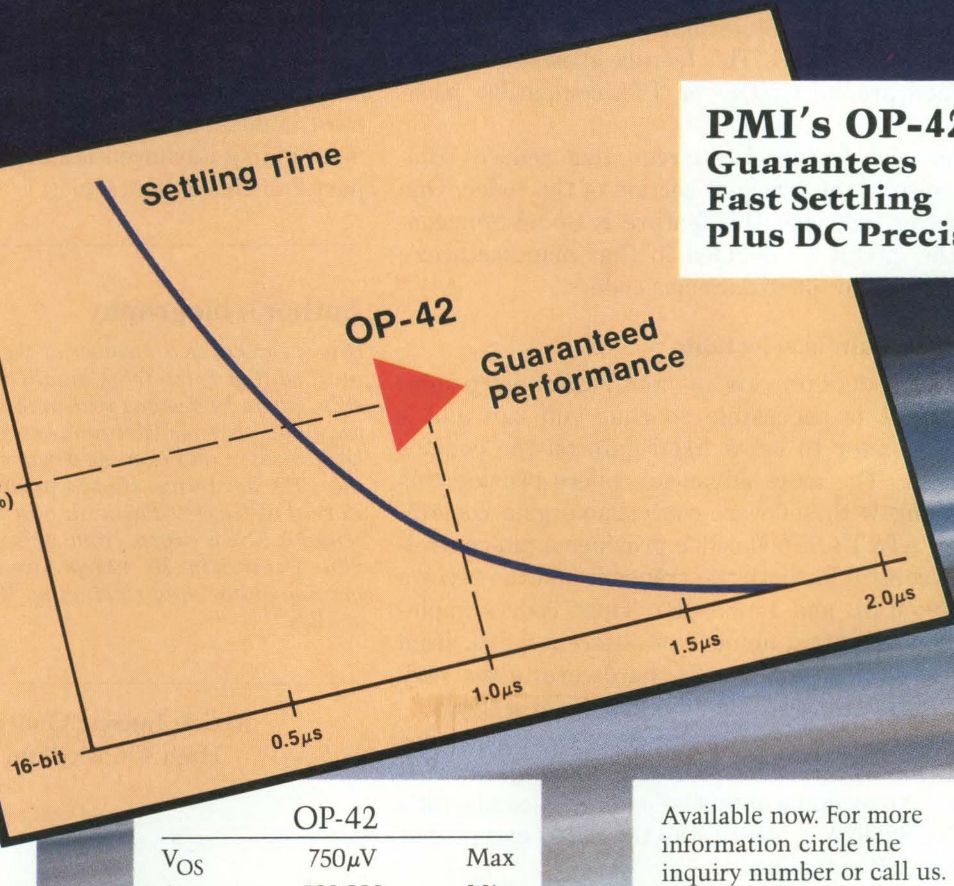

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Codecs that offer just the standard features cost somewhere between $4 and $6 each in quantities of 10,000.

digital logic that is typically driven by 5V levels.

These standard features are the ones that you can expect to run across in almost every codec that is currently available. However, you'll often encounter a few other features that don't qualify as advanced, but are not common enough to be considered standard.

One such feature is Motorola's pin-selection of TTL and CMOS digital levels. This feature allows the chip to be designed around CMOS- or TTL-compatible hardware.

Another such feature is a circuit that reduces idle-channel noise in the transmit section of the codec. One manufacturer that uses this feature is Gould Semiconductor; the circuit is included in that manufacturer's S3506, S3507, and S3507A Series codecs.

Input-buffer gain is selectable

Almost all codecs provide an input buffer (an op amp) whose output is accessible so that you can add a feedback resistor to set a fixed gain on the codec's analog input. The more advanced codecs provide this feature along with software-controllable gain control. Moreover, AT&T's T7500 codec provides a pin-controllable gain control for both the transmit and the receive sections (0=0 dB and 1=+3 dB). Thus, codecs implement gain control in a number of different ways, from the very basic fixed gain set by hardware to the very advanced software-controlled dynamic gain settings.

Some codecs have special versions of the basic codec that allow for what's called "8th-bit signaling" or "A/B signaling." An example of this is Gould Semiconductor's S3507. The S3507A is identical to the S3507 except that it provides A/B signaling.

Hide data signals in the voice

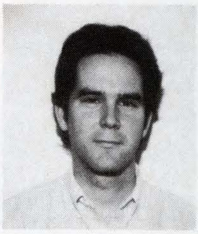
A/B signaling is simply a method by which signaling data is transmitted and received along with voice data. Signaling data could indicate (but is not limited to) hook status, loop closure, pulse dialing, or ring detection. A/B signaling need not be used with devices that support it. The disadvantage of using A/B signaling is that the signaling data is inserted in the least significant bit (LSB) of every 6th frame of the voice data, thus causing a slight increase in idle-channel noise and a slight decrease in the S/N ratio.

The A signal is inserted in frame 6, and the B signal is inserted in frame 12. Because the voice data is sampled 8000 times per second, a frame is 125 μsec in length, and therefore the A and B signaling data are each updated once every 1.5 msec (1.5 msec=125 μsec/frame×12 frames). This scheme is shown in **Fig 3.**

An additional feature found on some codecs is a power amplifier in the analog output of the receive section. The amplifier provides a push-pull balanced output drive across a 600Ω load. Some applications may need this added drive capability. One codec that provides this feature is the National TP3064 codec/filter combo.

The standard and nonstandard features thus far discussed are the ones that you're likely to encounter on most codecs. However, a few new codecs offer some outstanding advanced features. They'll be discussed in part 2 of this 2-part series. **EDN**

Author's biography



Brady Barnes is a member of the technical staff at Inter-Tel (Chandler, AZ), where he designs real-time software that controls telecommunications hardware; in addition, he designs digital-PBX hardware. He has previously worked at Hewlett-Packard, and he received a BSEE degree from Arizona State University. He enjoys traveling, playing guitar, and conducting Bible studies.

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Diodes and capacitors imitate transformer

Rudy Stefenel
Luma Telecom, Santa Clara, CA

The diode-capacitor network of **Fig 1** accepts low current at a high voltage and delivers higher current at a lower voltage, behaving like a step-down transformer. You drive the circuit with a square-wave input signal as shown.

When the input is at its peak voltage, V_P, current through D_{10}, D_7, D_4, and D_1 charges series capacitors C_4, C_3, C_2, and C_1. The voltage on each capacitor reaches approximately $\frac{1}{4}(V_P-4V_F)$, where V_F is the forward-voltage drop across one diode. However, the total output voltage doesn't equal the sum of the voltages on the four capacitors; it's less than that by two diode drops. Consequently, the circuit is inefficient for low-amplitude drive signals (too much voltage is lost across the diodes).

For 15V and 60V p-p inputs, the circuit's corresponding outputs are approximately −1.65V and −12.9V, depending on the load. An input of 28V p-p produces about −5V. Notice that the square-wave generator must sink more current than it sources: It charges the capacitors in series, but discharges them in parallel.

When the input terminal switches to 0V, it connects the capacitors in parallel by pulling the positive side of each capacitor near 0V. The capacitor voltages then produce current flow that creates a negative charge across the load capacitor (C_L). The voltages on C_3, C_2, and C_1 each charge C_L through two diodes in series, but the charging path through C_4 has only one diode, D_{11}. This configuration results in a higher surge current through D_{11} and C_4 and a slightly higher negative output voltage, unless you add a diode in series with D_{11}.

You can change the output voltage by adding or subtracting sections; C_1, D_1, D_3, and D_2 constitute one section, for example. Make the series capacitors equal in value and the total value of these capacitors equal to the load capacitor:

$$C_L = \frac{I}{2V_Rf},$$

where I is the load current, V_R is the maximum allowed p-p ripple voltage, and f is the input frequency. **EDN**

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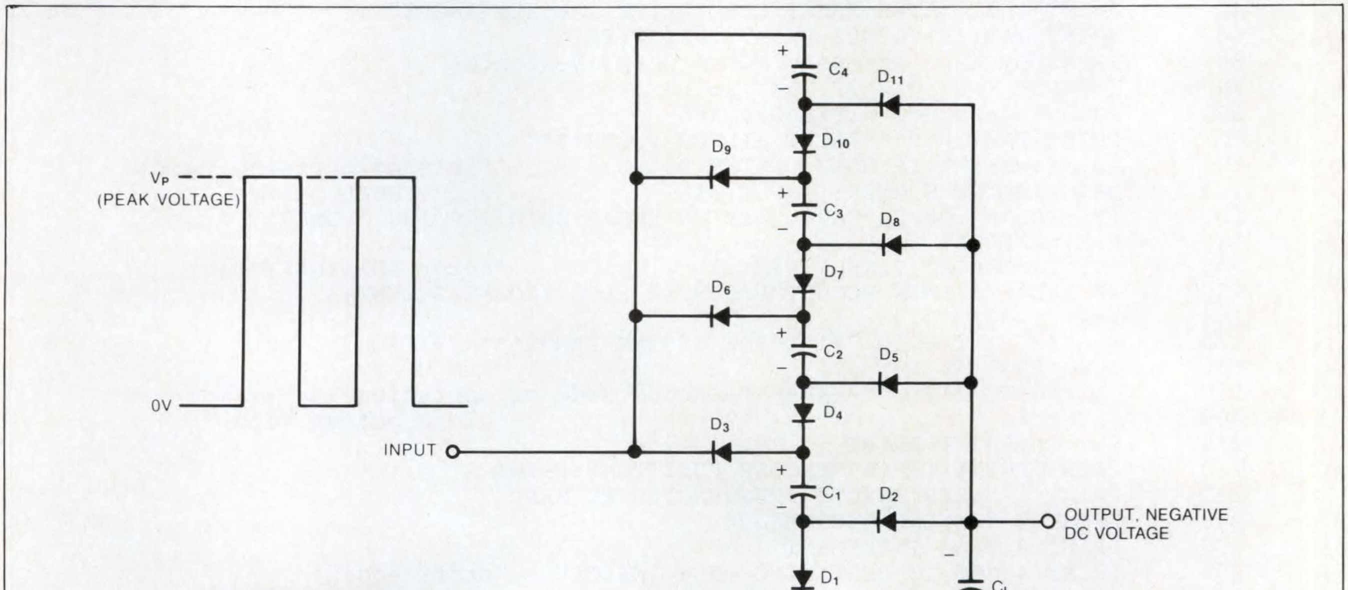

***Fig 1—This diode-capacitor network converts** an input square wave to a negative dc voltage.*

Compute magnitude, phase, and group delay

Marc Thompson
For-A Corp, Newton, MA

The IBM PC Basic program of **Listing 1** calculates the magnitude, phase, and group delay for a transfer function with any reasonable number of poles and zeros. You can use the program in the design of analog video filters in which you must minimize group-delay ripple in the passband to avoid picture degradation.

The program first prompts you for the pole and zero locations (each of which you enter in terms of a real and an imaginary quantity), and then it asks you to choose a mode of operation.

For mode 1, you enter each frequency manually and get an (almost) immediate response in the following form:

FREQ (Hz)	MAG	dB	ANGLE (deg)	DELAY (sec)
4.0000E+06	0.99821	−0.0155	−120.05	1.0771E−07

For mode 2, you define a range of frequencies by entering a low and a high value plus a linear increment. The program then calculates the input frequencies automatically and displays data for each.

For mode 3, you define a range of frequencies in the same way as mode 2, but you enter a multiplicative constant for the frequency increment. This mode is useful for generating data on a log scale over several decades of frequency.

For modes 2 and 3, the program-execution time varies with the number of frequency values and the number of singularities (poles and zeroes) in the transfer function. Using an IBM PC/XT, for example, you can generate data for a function with six zeroes and seven poles, for 50 frequencies, in less than two minutes. **EDN**

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LISTING 1—IBM BASIC PROGRAM

```
10      DIM P(100)      '-----------Data Input----------------
20      SCREEN 1:COLOR 1:PI=3.14159
30      PRINT"**Given Pole and Zero Locations**":PRINT
40      PRINT"CALCULATES MAGNITUDE":PRINT TAB(12)"ANGLE"
50      PRINT TAB(12)"GROUP DELAY":PRINT:PRINT
60      PRINT"By Marc Thompson FOR-A Corp. Newton,MA"
70      X=0:FOR X=0 TO 2222:NEXT X:CLS
80      PCOUNT=0:ZCOUNT=0:PFLAG=1:X=0
90      PRINT TAB(10)"***INPUT FILTER POLES***"
100     PRINT:PRINT"(IF NONE, ENTER D)"          'finished entering POLES?
110     PRINT:PRINT"SIGMA";:INPUT P$             'enter REAL part
120     IF (P$="D" OR P$="d") THEN ON PFLAG GOTO 170,190 'DONE?
130     P(X)=VAL(P$)
140     PRINT "OMEGA";:INPUT P(X+1)              'enter IMAGINARY part
150     IF PFLAG=1 THEN PCOUNT=PCOUNT+1 ELSE ZCOUNT=ZCOUNT+1
160     X=X+2: GOTO 110
170     CLS:PRINT TAB(10)"***INPUT SYSTEM ZEROS***":PFLAG=2
180     GOTO 100
190     CLS: GOTO 210   '---------Choose Mode of Operation---------------
200     CLOSE #1                                 'close output file
210     KEY ON:PRINT:PRINT
220     PRINT:PRINT TAB(6)"CHOOSE FUNCTION":PRINT
230     PRINT 1 "USER INPUTS FREQUENCIES BY HAND"
240     PRINT 2 "LINEAR INCREMENT"
250     PRINT 3 "LOG INCREMENT"
260     PRINT 4 "GO TO BEGINNING--NEW INPUTS"   'start again
270     PRINT "YOUR CHOICE";:INPUT CHOICE
280     IF (CHOICE<1 OR CHOICE>4) THEN 230
290     CLS:IF (NOT CHOICE>3) THEN OPEN "A:ZIPPY" FOR OUTPUT AS #1
300     ON CHOICE GOTO 320,370,390,20
310     '--------------Frequency Generation------------------------
320     CLS:WIDTH 80:SCREEN 0:PRINT:PRINT
330     DISP=1:PRINT"INPUT FREQUENCY IN Hz---***IF DONE, TYPE D***".
```

Listing continued on pg 226

LISTING 1—IBM BASIC PROGRAM *(Continued)*

```
340   INPUT START$:IF (START$="D" OR START$="d") THEN 200
350   START=VAL(START$):RFREQ=2*PI*START
360   GOTO 500                              'start calculation
370   DISP=1:PRINT"GENERATES FREQUENCIES":PRINT "USING LINEAR INCREMENT"
380   GOTO 400
390   DISP=1:PRINT"GENERATES FREQUENCIES":PRINT"USING LOG INCREMENT"
400   PRINT:PRINT"STARTING FREQUENCY";:INPUT START
410   IF START<0 THEN 400                   'for MISTAKE
420   PRINT:PRINT"ENDING FREQUENCY";:INPUT LAST
430   IF START>=LAST THEN 400               'for MISTAKE
440   PRINT:PRINT"INCREMENT";:INPUT INC
450   PRINT:LINE INPUT"TITLE FOR GRAPH?";TITLE$
460   CLS:WIDTH 80:SCREEN 0:GOTO 490
470   IF CHOICE=2 THEN START=START+INC ELSE START=START*INC
480   IF START>LAST THEN 200
490   RFREQ=2*PI*START
500   X=0:PC=PCOUNT:POLE=1     '---------Singularity Calc.-----------
510   MAG=1:ANGLE=0:DELAY=0                 'initial values
520   IF NOT PC=0 THEN 550                  'if done, goto ZERO
530   PC=ZCOUNT:POLE=2
540   IF PC=0 THEN 740                      'if done, goto display
550   SIGMA=P(X):OMEGA=P(X+1)
560   IF SIGMA=0 THEN 710                   'pole or zero on j-axis
570   M=RFREQ-OMEGA:P=M:M=M*M               'calc. temp. magnitude
580   M=M+SIGMA*SIGMA:M=SQR(M)
590   K=SIGMA*SIGMA+OMEGA*OMEGA: K=SQR(K)
600   SIGMA=-1*SIGMA:P=P/SIGMA:D=P
610   P=57.296*ATN(P)                       'calc. temp. phase angle
620   D=D*D+1:D=D*SIGMA:D=1/D               'calc. temp. group delay
630   IF POLE=2 THEN 670
640   MAG=MAG*K/M                           'for POLE
650   ANGLE=ANGLE-P
660   DELAY=DELAY+D:X=X+2:PC=PC-1:GOTO 520
670   MAG=MAG*M/K                           'for ZERO
680   ANGLE=ANGLE+P
690   DELAY=DELAY-D:X=X+2:PC=PC-1:GOTO 540
700   '---------------SINGULARITY AT ORIGIN OR J-AXIS----------------------
710   IF (RFREQ-OMEGA)>0 THEN P=90 ELSE P=-90
720   M=RFREQ-OMEGA: IF OMEGA=0 THEN K=1 ELSE K=OMEGA
730   D=0:ON POLE GOTO 640,670
740   IF DISP=0 THEN 830       '------------Display---------------
750   IF CHOICE=1 THEN 760 ELSE PRINT #1,DATE$:PRINT #1,TIME$:PRINT #1,TITLE$
760   PRINT #1,:PRINT #1,"FREQ.(Hz)" TAB(22); 'to output file
770   PRINT:PRINT"FREQ.(Hz)"TAB(22);        'to monitor display
780   PRINT #1,"MAG."TAB(40);:PRINT"MAG."TAB(40);
790   PRINT #1,"dB"TAB(50);:PRINT"dB"TAB(50);
800   PRINT #1,"ANGLE(deg.)"TAB(65);:PRINT"ANGLE(deg.)"TAB(65);
810   PRINT #1,"DELAY(sec.)";:PRINT"DELAY(sec.)":PRINT
820   DISP=0:PRINT:PRINT #1,                'don't display head
830   PRINT #1,USING"##.####^^^^";START;:PRINT #1,TAB(17);
840   PRINT USING"##.####^^^^";START;:PRINT TAB(17);
850   PRINT #1, USING"#####.#####";MAG;:PRINT #1,TAB(35);
860   PRINT USING"#####.#####";MAG;:PRINT TAB(35);
870   IF MAG=0 THEN 960
880   MAG=ABS(MAG):DB=20*LOG(MAG)/LOG(10)
890   PRINT USING"####.####";DB;: PRINT TAB(50);
900   PRINT #1,USING"####.####";DB;:PRINT #1,TAB(50);
910   PRINT #1,USING"####.##";ANGLE;:PRINT #1,TAB(65);
920   PRINT USING"####.##";ANGLE;:PRINT TAB(65);
930   PRINT #1,USING"##.####^^^^";DELAY
940   PRINT USING"##.####^^^^";DELAY
950   ON CHOICE GOTO 330,470,470
960   PRINT #1,"-INFINITY"TAB(50);          'for MAG=0, dB=-INF
970   PRINT "-INFINITY"TAB(50);:GOTO 910
980   END
```

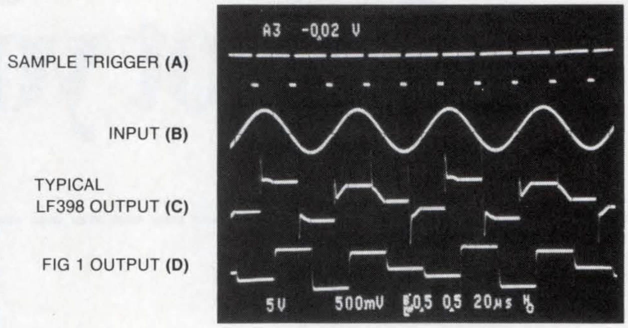
Multiplexed S/H amplifiers hide glitches

Paul Swearingen
National Semiconductor, Santa Clara, CA

The circuit of **Fig 1** switches between the outputs of two low-cost sample/hold (S/H) amplifiers, thereby masking the glitches and slew-rate distortion of each. What's more, the circuit provides twice the sampling rate possible with one sample/hold amplifier alone.

Fig 2's scope photo compares the output of the circuit (trace D) with that of a typical LF398 S/H amp (trace C). Notice the undershoots, overshoots, ringing, and slew-rate limiting associated with each sampling interval in trace C. Most of these aberrations are absent in trace D because IC_3, the analog switch of **Fig 1**, disconnects each S/H amp during its noisy sample mode. The switch always connects the circuit output to an S/H amp that's in a quiet hold mode.

The digital ICs in **Fig 1** generate properly timed control signals for the S/H amplifiers and analog switch



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	20 µSEC/DIV
B	0.5V/DIV	20 µSEC/DIV
C	0.5V/DIV	20 µSEC/DIV
D	0.5V/DIV	20 µSEC/DIV

Fig 2—This scope photo compares Fig 1's output *(trace D) with the noisier output of a typical LF398 sample/hold amplifier (trace C). Both circuits are sampling a 20-kHz sine wave.*

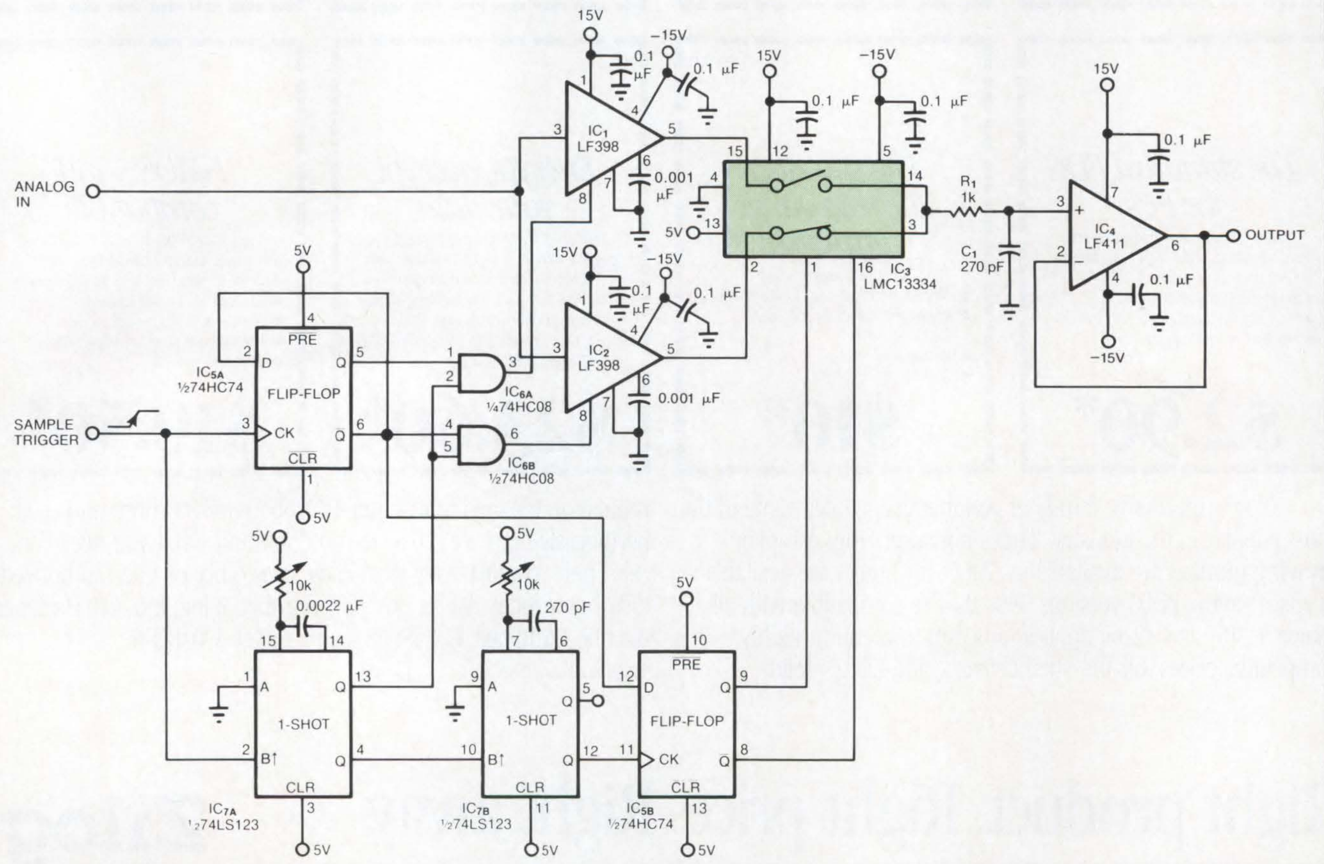


Fig 1—By using a switch (IC_3) between two sample/hold amplifiers, *you can avoid passing the devices' sample-mode aberrations to the output. The sample/hold amp driving the output amplifier is always in the hold mode.*

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(Fig 3). The monostable multivibrator IC_{7A} sets the acquisition time required by the S/H amplifiers, and IC_{7B} generates a delay that ensures each S/H amp has settled before the switch toggles. Break-before-make action in the switch directly affects the circuit's output accuracy; R_1 and C_1 help filter switch transitions. **EDN**

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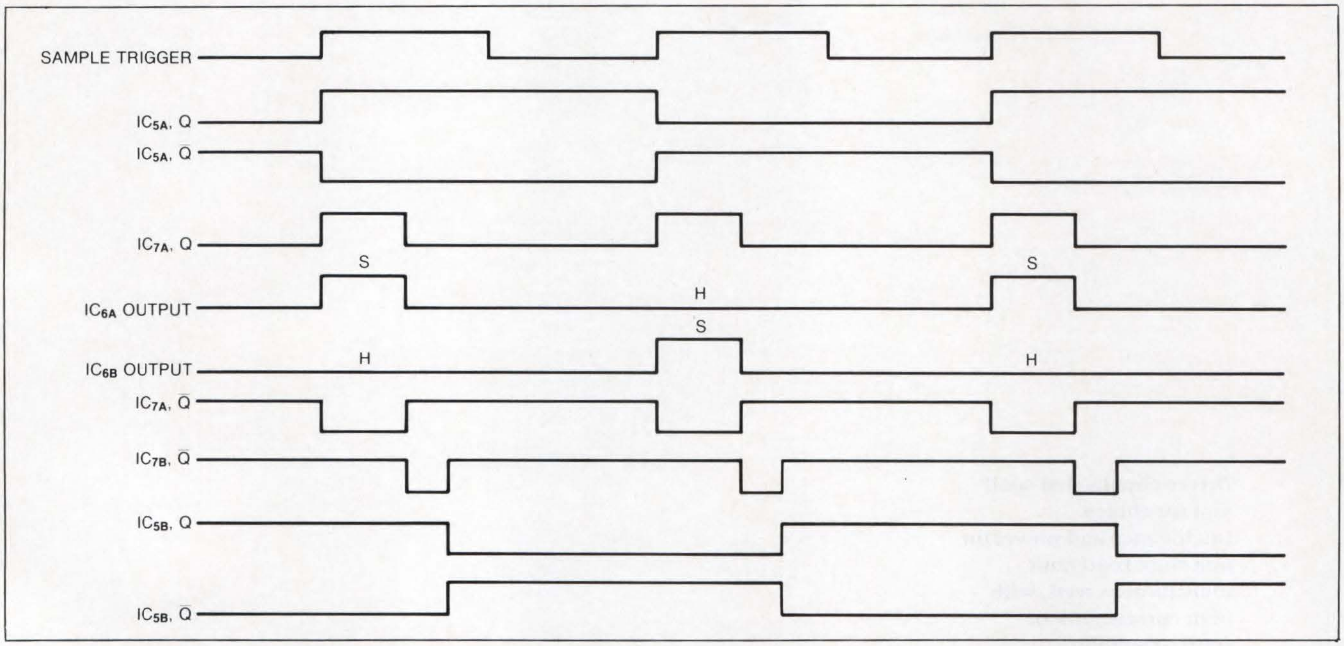


Fig 3—These Fig 1 timing waveforms illustrate *digital control signals for the sample/hold amplifiers (IC_{6A} and IC_{6B}) and the delayed, complementary drive signals to IC_3's analog switches (IC_{5B}'s Q and $\overline{Q}$ output).*

Second μP enhances TMS32020 system

Luis Vieira de Sá
University of Coimbra, Coimbra, Portugal

You can double the processing power of a TMS32020-based DSP system by adding a second μP capable of addressing the same memory without wait states or arbitration. Because the TMS32020 μP uses its external data and address buses only a little more than half the time, two processors using address multiplexing and fast static RAM (40-nsec access time), can share the memory at full speed. This configuration increases the system's throughput by allocating different parts of an algorithm for simultaneous processing by the two μPs **(Fig 1).**

To function properly, the processors must operate in sync and from the same clock, but they must access the memory alternately through suitable address multiplexers and data buffers. The TMS32020's Sync input

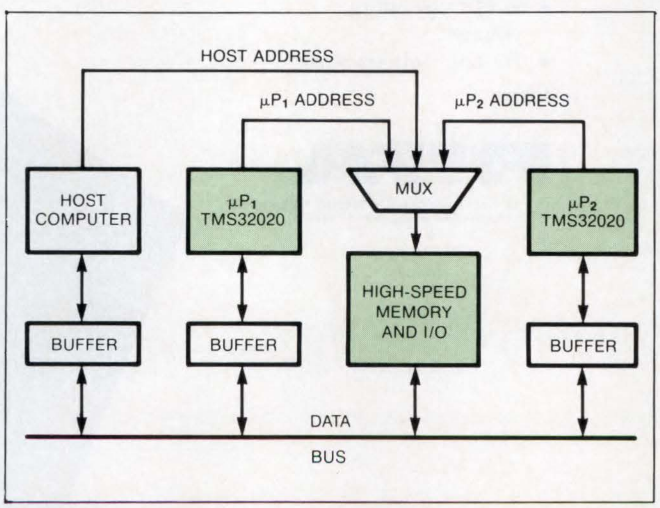
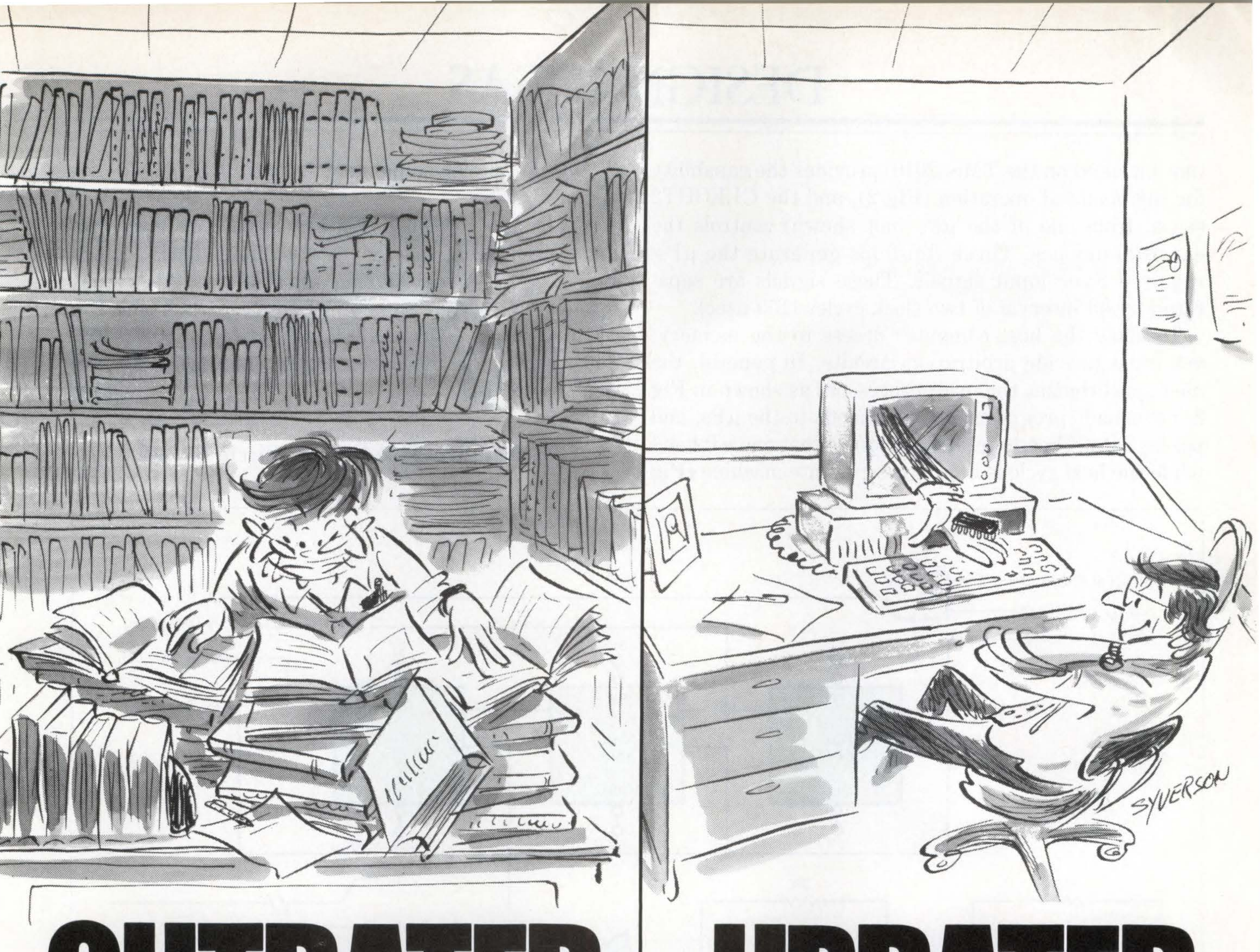


Fig 1—This system has a 3-port memory *that lets μP_1 collect data and store it in RAM while μP_2 processes earlier data and the host removes the data already processed.*



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(not included on the TMS32010) provides the capability for this mode of operation (**Fig 2**), and the CLKOUT2 signal from one of the μPs (not shown) controls the external devices. Three flip-flops generate the μPs' required $\overline{\text{Sync}}$ input signals. These signals are separated by an interval of two clock cycles (100 nsec).

To allow the host computer access to the memory, you must provide arbitration circuits. In general, the host synchronizes the microprocessors as shown in **Fig 2**, downloads programs and commands to the μPs, and passes data. These operations require that one μP halts while the host cycle is in progress; a state machine (**Fig 3**), which you can implement in one PLD, supervises this operation.

In response to the host's $\overline{\text{DS}}$ signal, the state-machine circuit controls the Ready input of μP_2, which forces the μP to wait during a host access. The circuit acknowledges the transfer of data by asserting the $\overline{\text{DTACK}}$ signal. ($\overline{\text{DS}}$ and $\overline{\text{DTACK}}$ are standard VME Bus signals; the majority of other bus systems have similar signals.) **EDN**

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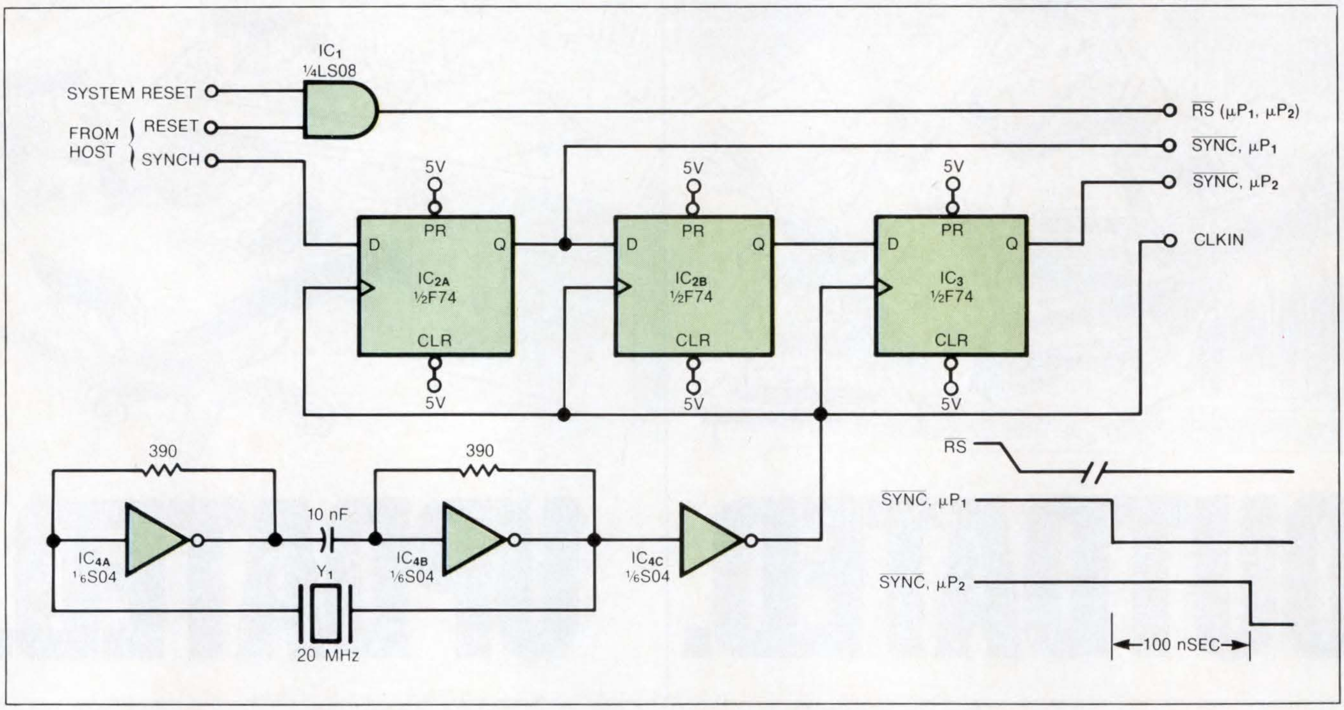

Fig 2—Fig 1's host computer uses this circuit to force the μPs' Sync inputs low during the time $\overline{RS}$ is active.

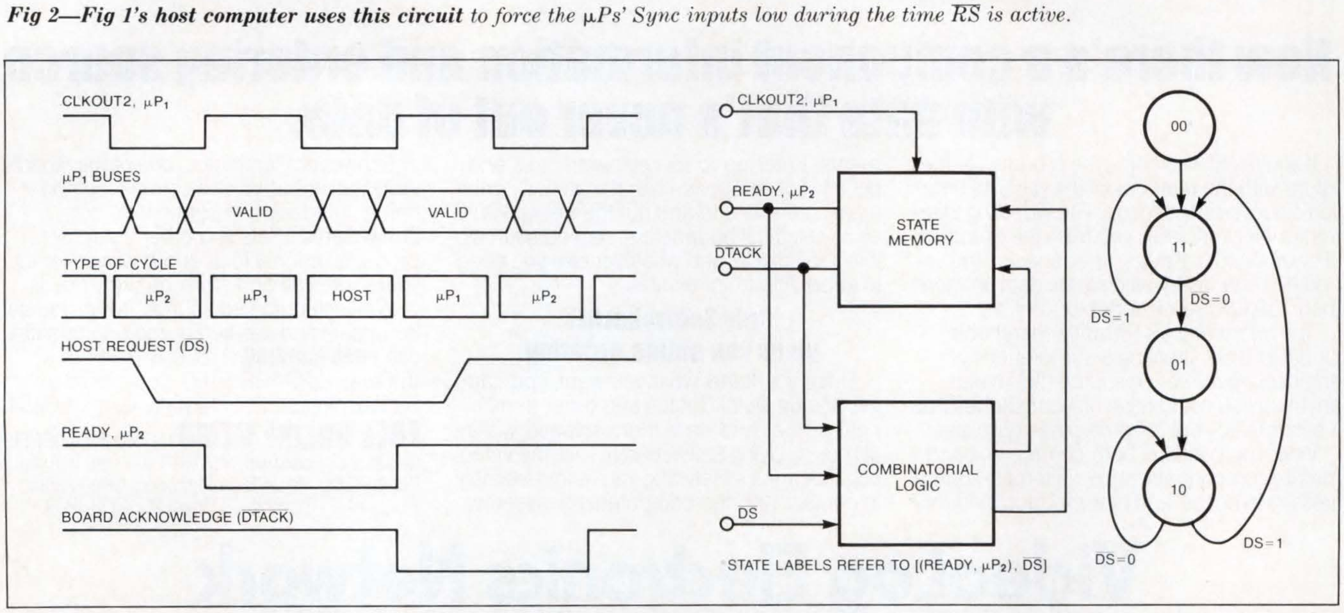

Fig 3—This state machine uses the CLKOUT2 signal of Fig 1's μP_1 to define time slots for accessing the common memory. The circuit forces μP_2 to wait during an access by the host.

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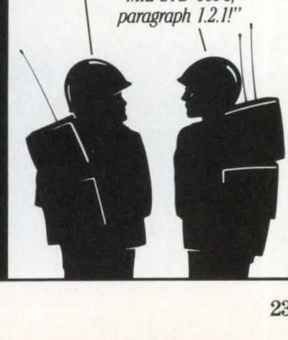

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ISSUE WINNER

The winning Design Idea for the February 5, 1987, issue is entitled "MOSFET provides glitchless power backup." It was submitted by Tosh Mizuno of Dalmo Victor Co (Belmont, CA).

Circuit extracts square-wave pulse

Patrick Borel
Thomson Semiconducteurs, Grenoble, France

The **Fig 1** circuit traps a single positive pulse from a square-wave train. Following the rising edge of an input command, the Pulse Out signal emits a replica of one positive pulse of the Clock signal simultaneous with the Clock signal's next rising edge.

The Input Command signal sets the Q_1 output of flip-flop IC_{1A}. Consequently, the next rising edge of the Clock signal sets the Q_2 output of IC_{1B}, which allows AND gate IC_{2C} to pass the Clock signal's next positive pulse. AND gates IC_{2A} and IC_{2B} prevent the generation of brief output glitches by delaying the Clock signal by t_D sec (two propagation delays). **EDN**

To Vote For This Design, Circle No 747

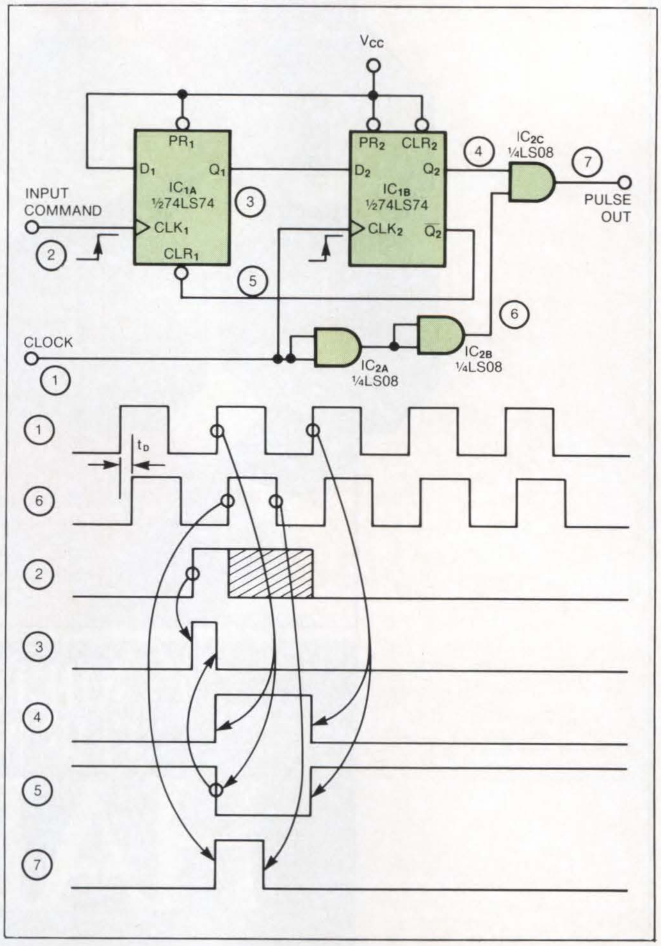
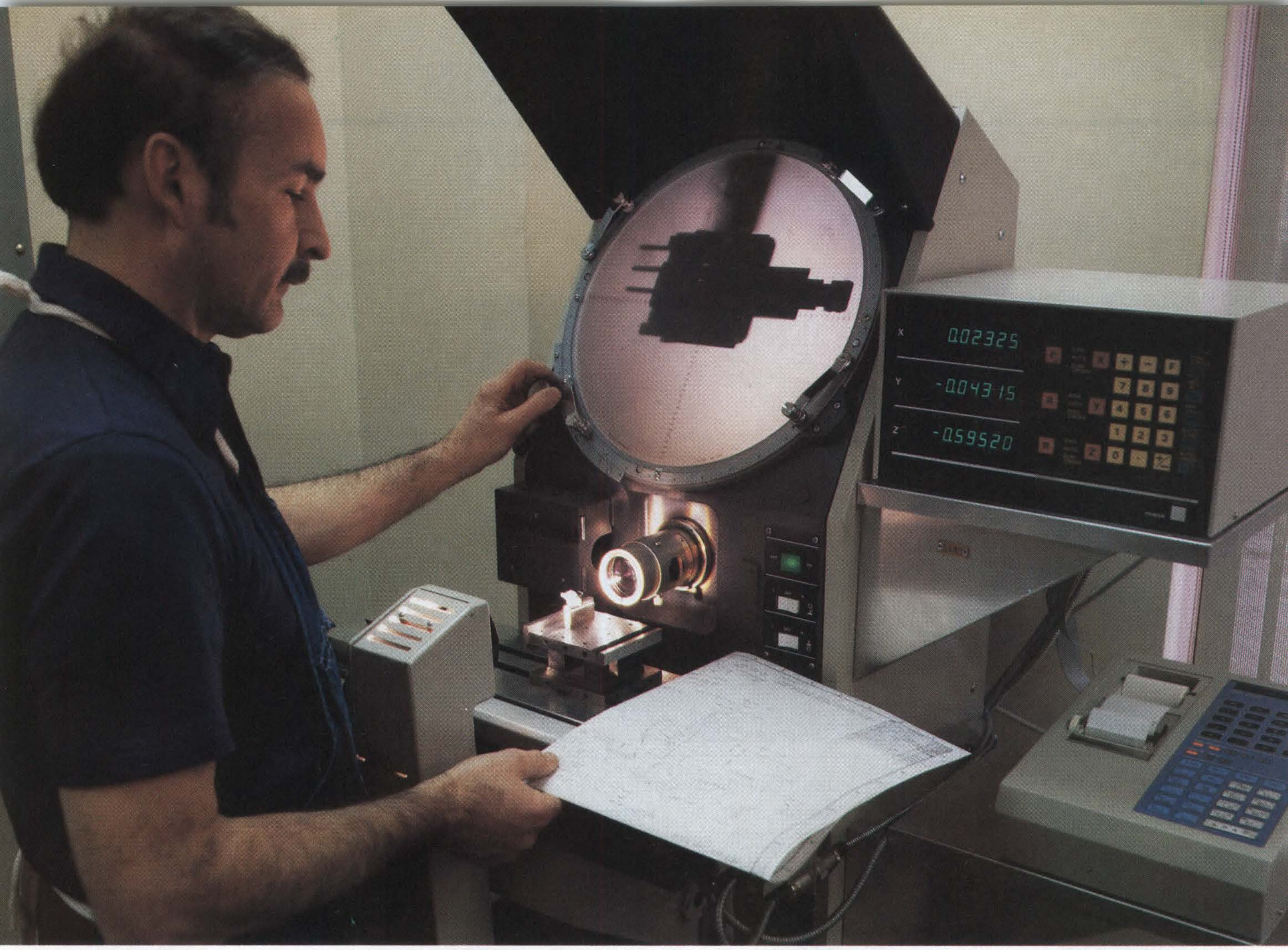


***Fig 1—Each Input Command signal causes this circuit** to issue one positive pulse from the Clock signal pulse train.*



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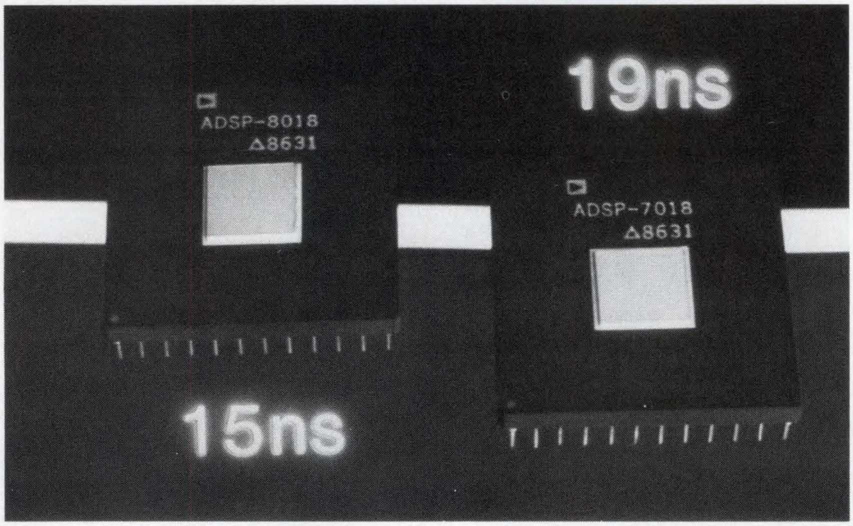
CIRCLE NO 144

INTEGRATED CIRCUITS



MULTIPLIERS

- *Devices multiply 16-bit words in 15 or 19 nsec*
- *ECL- or TTL-compatible bipolar devices*

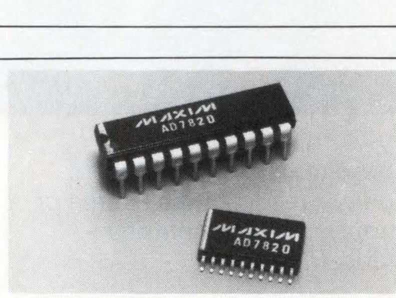
According to the manufacturer, the ECL-compatible ADSP-8018 and the TTL-compatible ADSP-7018 are digital multipliers with the industry's fastest multiply times—15 and 19 nsec max, respectively. Based on a bipolar process featuring a 2-μm device geometry, these products feature 300-psec gate delays and 300-μW/gate power dissipation. Each device dissipates less than 3.5W total. The 32-bit output port presents the product of a 16×16-bit multiply operation in one cycle; for 16-bit systems, you can multiplex the result through a single port. Independent input, instruction-status, and output latches have a transparent mode of operation that simplifies system timing. The multipliers accept 2's-complement, unsigned-magnitude, and mixed-mode input code. Both devices come in 108-pin pin-grid array, spec'd for the commercial temperature range. ADSP-8018, $260; ADSP-7018, $205 (100).

Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 461-3672. TWX 710-394-6577. TLX 174059.

Circle No 351

A/D CONVERTER

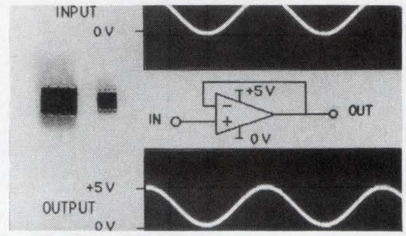
- *8-bit resolution; 1.36-μsec conversion time*
- *Comes in a 20-pin, small-outline package*



You now have the option of obtaining the AD7820 8-bit A/D converter in a small-outline, surface-mount package in addition to the standard ceramic and plastic DIPs. The CMOS chip features an internal track/hold function and μP-compatible interface circuitry, and it uses a half-flash technique to achieve a 1.36-μsec max conversion time. The converter operates from 5V and has a 0 to 5V analog input range. The electrical grades include ±1-LSB and ±½-LSB versions for the commercial, industrial, and military temperature ranges. In a small-outline package, from $10.95 (100).

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 352



PRECISION OP AMP

- *Rail-to-rail input- and output-voltage ranges*
- *Unity-gain stable with 800-pF load*

The ALD 1702 is a laser-trimmed, silicon-gate CMOS op amp that specs offset-voltage grades of 0.9, 2.0, and 4.5 mV. Operating from a 5V supply or from bipolar supplies in the range ±2.5 to ±5V, the amplifier provides input- and output-voltage ranges that include the supply rails. A compensation scheme allows the device to remain unity-gain stable while driving capacitive loads of 400 pF (noninverting mode) or 800 pF (inverting mode). The short-circuit-protected output can deliver 5 mA. Other specs include a 1.0-MHz min unity-gain bandwidth, a 1.4V/μsec min slew rate, and a 400V/mV open-loop, no-load voltage gain. The unit has a 741-type pinout and comes in an 8-pin plastic or ceramic DIP or a small-outline package. $1.78 to $3.89 (100).

Advanced Linear Devices Inc, 1030 W Maude Ave, Suite 501, Sunnyvale, CA 94086. Phone (408) 720-8737. TWX 510-100-6588.

Circle No 353

MOTOR-CONTROL IC

- *Drives 3-phase complementary output switch pairs*
- *Suppresses output pulses shorter than a minimum time*

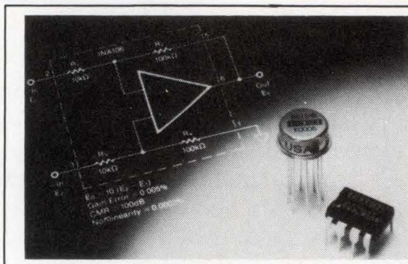
Designed for the control of 3-phase, variable-speed ac motors, dc brushless motors, or PWM converters, the MA 818P waveform-generator IC includes all the logic necessary to produce 3-phase PWM output signals. The chip controls three complementary electronic switch pairs, which may be MOSFET, bipolar, or GTO thyristor devices, and you can program delays into the output waveforms to maximize the efficiency of the complementary switching. You configure the waveform generator via a μP interface. The MA 818P automatically inhibits narrow output pulses that are less than a preprogrammed minimum period; you can program this minimum period to be as short as 1 μsec. You can also switch the output phases to obtain forward or reverse motor rotation. The waveform generator accepts constant-carrier frequencies in the 600-Hz to 19.5-kHz range, and it has user-selectable power-frequency ranges of 0 to 50 Hz and 0 to 3 kHz. You can define the shape of the power frequency's waveform with data contained in an external ROM. The MA 818P is fabricated in CMOS technology with TTL-compatible inputs and outputs. £20 (100).

Marconi Electronic Devices Ltd, Lincoln Industrial Park, Doddington Rd, Lincoln LN6 3LF, UK. Phone (0522) 688121. TLX 56380.

Circle No 354

Marconi Electronic Devices Inc, 80 Smith St, Farmingdale, NY 11735. Phone (516) 420-8378.

Circle No 355



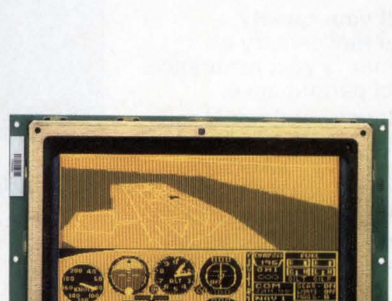
DIFFERENTIAL AMP

- *Fixed gain of 10*
- *Better than ±0.015% accuracy*

The INA106 differential amplifier provides a gain of 10 by combining a precision op amp and a 10- to 100-kΩ resistor network on a monolithic chip. Overall accuracy, including errors in gain, linearity, offsets, and CMR, is better than ±0.015%. The amplifier's 20-mA output (for positive output voltages) simplifies the design of 4- to 20-mA transmitter circuits. Other specs include a minimum 100-dB CMR, a 5-μsec settling time (to ±0.01%), and a 2-mA quies-

side view
(actual size)

With a Planar light-emitting electroluminescent flat panel display, you could use the rest of this space for anything you like. Call either 503-690-1100 or 503-690-1102, or write for a brochure:
PLANAR SYSTEMS, INC.
1400 N.W. Compton Drive
Beaverton, Oregon 97006.



PLANAR
The Definition of Quality

CIRCLE NO 135

cent supply current. The device comes in a TO-99 can or a plastic 8-pin DIP, spec'd for the commercial, industrial, or military temperature ranges. From $3.65 (100).

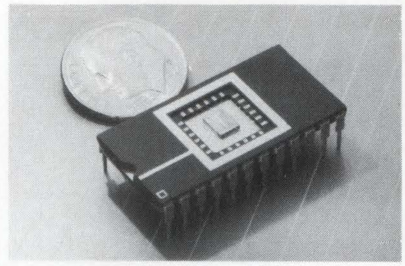
Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 356

A/D CONVERTERS

- *Include track/hold function*
- *Convert in 13 μsec*

The CA3310 and CA3310A 10-bit CMOS A/D converters execute their successive-approximation algorithm by controlling charge redistribution on a capacitive ladder. The ladder provides an inherent track/hold



function. The converters require a 3 to 6V supply and draw about 3 mA at 5V. The analog input range includes both rails of the power supply. With a 1-MHz clock (13-μsec conversion time), the 3310 specs ±¾ LSB max for the integral- and differential-linearity errors, and ±½ LSB max for the gain and offset errors. Under similar conditions, the CA3310A specs ±½ LSB max for the integral- and differential-linearity errors, and ±¼ LSB max for the gain and offset errors. The devices include μP-interface circuitry and 3-state outputs. The converters come in 24-lead plastic and ceramic DIPs for the industrial and military temperature ranges, respectively. In plastic packages (E suffix), CA3310E, $6; CA3310AE, $8 (1000).

GE/RCA Solid State, Route 202, Somerville, NJ 08876. Phone (201) 685-6994.

INQUIRE DIRECT

CMOS RAM

- *Has multiplexed address/data bus*
- *Retains data with a 1V supply voltage*

The SAB 81C54 is a 512×8-bit CMOS RAM that comes in a 16-pin DIP or an SO-20 surface-mount package. The RAM has two chip-select inputs and internal address latches. You can connect the device directly to the multiplexed address/data bus of a variety of 8-bit microcontrollers and μPs. It operates from a 2.5 to 6V supply range, and it retains data when the supply voltage is as low as 1V. In standby mode, the device consumes less than

"It's expanded as small as it can get."

That's what he said.

And he was right. You see, our SBC design engineer, Tom Murphy, was convinced he could come up with a better board than Intel's 286/12. For months he'd been working with our new Multibus* 80286 SBC, making sure it was compatible with Intel, but adding refinements, improvements and putting more capabilities onboard.

But more wasn't enough for Tom, he wanted less, too.

"There's gotta be a way to pack all these capabilities on to a board that only takes up one slot."

And that's just what he did. Our 80286 uses the latest in surface-mount and RAM packaging, putting it all onboard . . . not on top. That skinnied it up right there. But Tom wasn't satisfied. He put four serial I/O ports onboard ("Intel has two, so we'll double it," he said). That means no more expansion modules, less bulk and less cost.

And what about DMA channel capabilities? Well, Tom feels pretty smug about **that** enhancement. Starting with full duplex DMA for two serial ports, he added multiplexed channels . . . eight to be exact. (Don't even bother to look for any on their board). So all four serial ports are serviced with three DMA channels left open. Open for whatever **your** creativity demands.

Tom came up with other great ideas, all of which are in our brochure, but think about what you can do with just what we've mentioned.

Then think about picking up the phone. Call Mike Heins, SBC Product Manager at 1-800-482-0315. It's toll free. (In Illinois, call 217-359-8010). Ask him to send you a brochure, give you specs and prices or, if you like, he'll even connect you directly to Tom.

Or write us, Central Data, 1602 Newton Drive, Champaign, IL 61821-1098.

Central Data

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1 μA. DM 4.50 (1000).

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

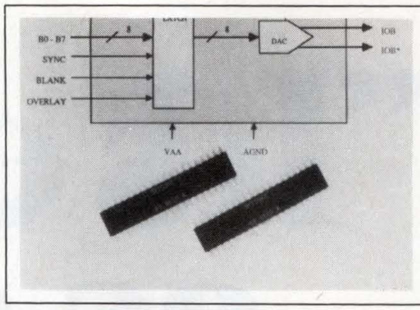
Circle No 358

Siemens Components Inc, 186 Wood Ave S, Iselin, NJ 08803. Phone (201) 321-4842.

Circle No 359

D/A CONVERTER

- *Includes three 8-bit video D/A converters*
- *Operates at 250 MHz*



The Bt109 is the fastest triple D/A converter available, according to the manufacturer. Suitable for use in graphics, image-processing, and video-reconstruction applications, the device operates at 250 MHz and supports display resolutions as high as 2048×1536 pixels. The sync-blank and overlay control inputs are registered to maintain synchronization with the pixel data. The Bt109's RGB video signals are RS-343A compatible, and they can drive doubly terminated 75Ω cables. Digital inputs are compatible with 10KH ECL. Rise and fall times are 1 nsec max; the integral- and differential-linearity errors are ±½ LSB max over the full operating-temperature range. $53 (100).

Brooktree Corp, 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. TLX 383596.

Circle No 360

ANALOG SWITCH

- *Handles ±10V signals*
- *Provides 40-dB isolation at 100 MHz*

The monolithic CDG2214N combines CMOS and DMOS (double-diffused MOS) technology to provide a high-speed (20 nsec off, 40 nsec on) spst analog switch with a CMOS-compatible control input. Principal specs include a 7.8-dB max insertion loss with a 50Ω load at 200 MHz, 66 dB of off-isolation at 10 MHz, and a ±10V analog input range. The device is available as a chip or in an 8-pin miniDIP. $0.99 (1000). Delivery, six weeks ARO.

Topaz Semiconductor, 1971 N Capitol Ave, San Jose, CA 95132. Phone (408) 942-9100. TWX 910-338-0025.

Circle No 361

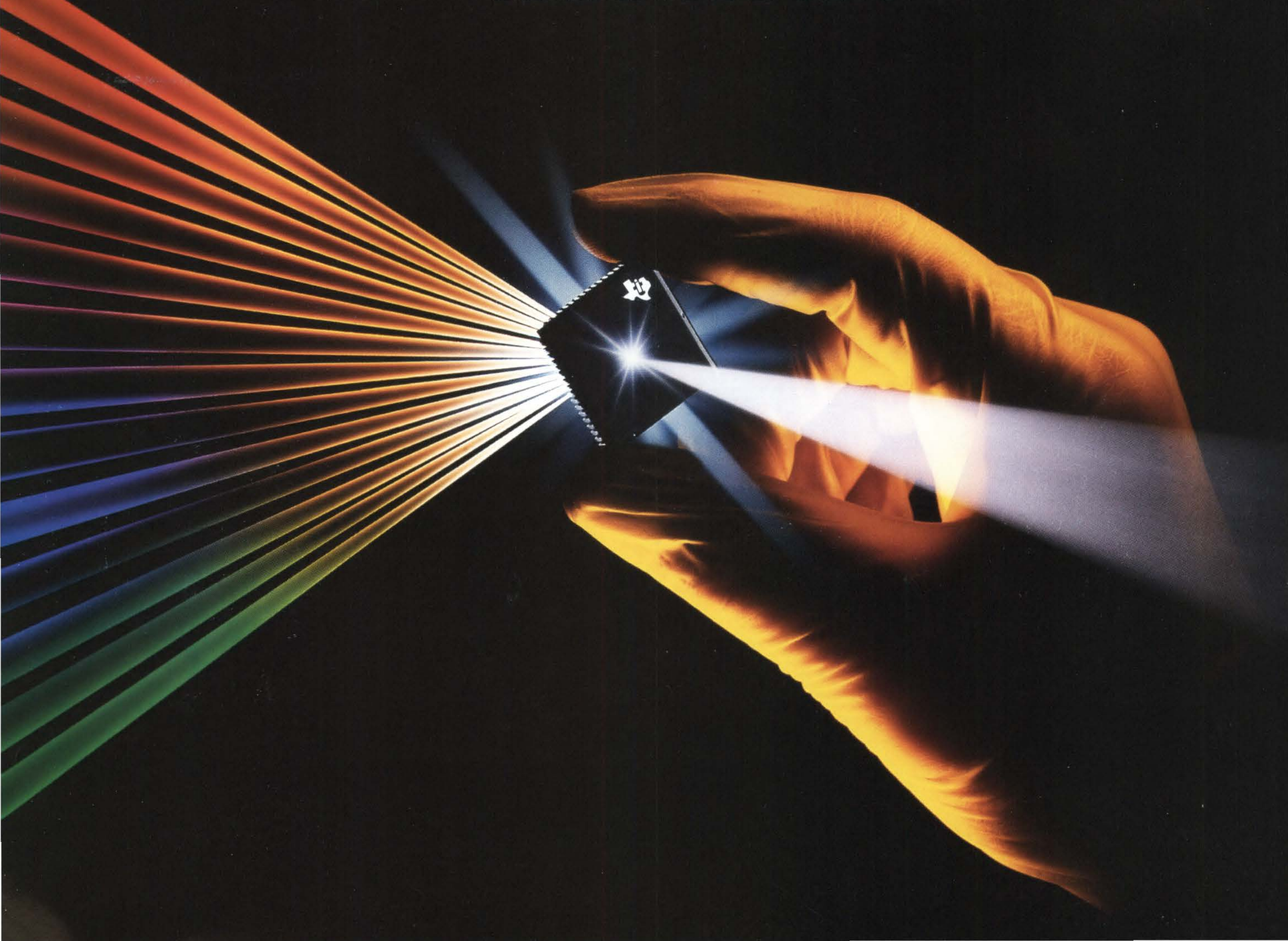
TEXAS INSTRUMENTS REPORTS ON

GRAPHICS

IN THE ERA OF

MegaChip

TECHNOLOGIES



Graphics in the Era of MegaChip Technologies:

New Texas Instruments lets you program circles

plus filled polygons, spline curves, antialiased lines,

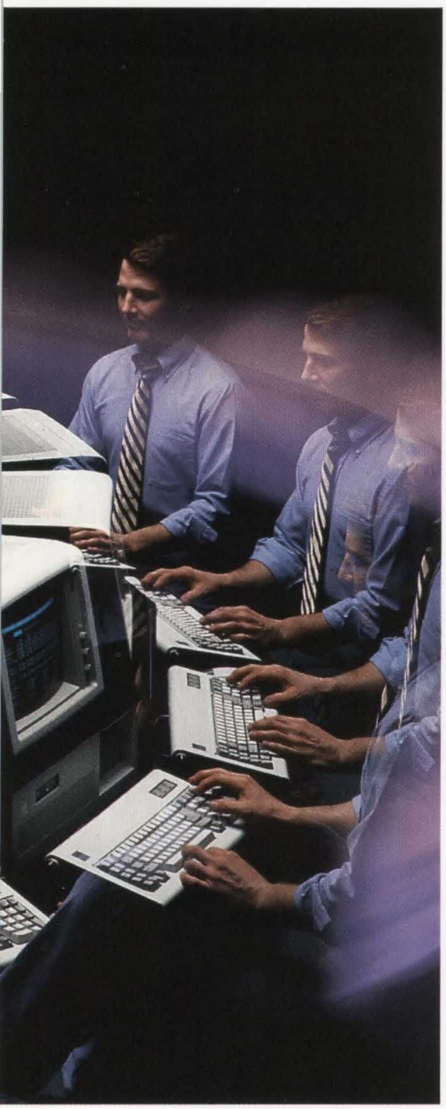
From PC displays to laser printers, the flexibility of TI's TMS34010 processor delivers the leading-edge performance you need today and to stay out in front tomorrow.

In TI's TMS34010 Graphics System Processor, you have a new and better graphics-design approach: The first high-performance, 32-bit CMOS microprocessor optimized for graphics applications.

The 34010 can execute all functions needed by graphics operating environments; hard-wired coprocessors can only execute a small part.

32-bit graphics processor around competition...

text, and more.



"Because the 34010 is programmable, it is in a league all its own."

Jim Richards, president of VMI, is talking graphics performance. You can program the 34010 processor to perform any graphics function you want, unlike hard-wired coprocessors. This means you can readily customize your system to outperform your competition.

But there's an even more important aspect to consider. The 34010 will help keep your system ahead of competition because it is compatible with existing graphics hardware standards — CGA,™ EGA,™ and PGC™ — and supports graphics software standards such as CGI, DGIS,™ and MS-Windows.™

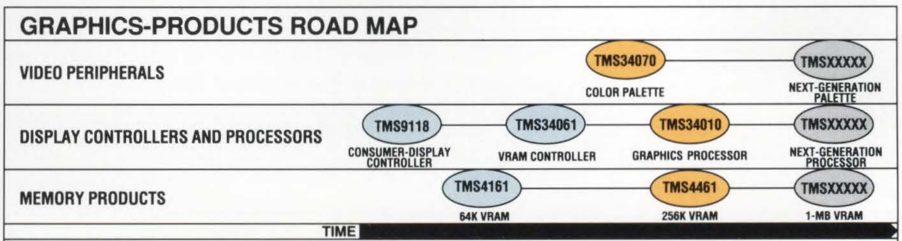
Standards like Windows and DGIS run faster on TI's TMS34010

The 34010 is also among the fastest microprocessors available. It handles six million instructions per second with a "draw" rate of up to an amazing 50 million pixels per second. Thus, it can boost total system performance.

Because of the support of MS-Windows and DGIS alone, many major applications software packages can already run on 34010-based systems.

TI's MegaChip Technologies

Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies, and they are the means by which we can help you and your company get to market faster with better products.



Road map to tomorrow's graphics systems: Next-generation additions to TI's innovative graphics-products family will allow you to build on your present designs to develop even higher-performance systems.

"You would think TI designed the 34010 with our technology in mind."

Luis Villalobos, Conographic president, refers to the power of the 34010 to process font outlines for desk-top publishing. Resolution up to 64K × 64K means no hardware limits for laser printers and other hard-copy devices.

Host independence and the flexibility of a device programmable in "C" language make TI's 34010 the cost/performance leader for PC displays, laser printers, desk-top publishing, workstations, terminals, plotters, FAX, image processing, digital copiers, mass storage, robot vision, and communications.

TI's total systems solution

In implementing your design, you'll want to consider other building blocks TI has developed. Included are the single-chip TMS34070 66-MHz Color Palette that supports simultaneous display of 16 out of 4,096 colors and the TMS70C42 Microcontroller that handles all serial interface duties.

Also included are high-speed video random-access memories (TMS4161 and TMS4461), plus linear small and large-area CCD image sensors.

To provide the host bus interface and any other customized functions you may require, TI offers quick design and production turnaround through its Application-Specific Integrated Circuits (ASICs) capabilities.

Development tools are available now for applying the 34010. Turn the page for details. ▶

"Texas Instruments had ready the full set of development tools we needed."

As William Frentz, executive vice president at Number Nine Computer, points out, TI has ready the hardware, software, and documentation you will need to make designing in the 34010 as fast and as easy as possible.

TI's 34010 software includes a full Kernighan and Ritchie "C" compiler with extensions and an assembler package for both MS-DOS™ and VAX™ operating environments.

A graphics/math library provides source code for more than 100 functions, whereas a typical controller chip offers only 15 to 20. A special font library contains more than 100 type fonts to expedite development of desktop publishing applications.

The TMS34010 XDS/22 Emulator is a flexible, realtime, in-circuit emulator. It can be used in a stand-alone mode through a standard terminal or through a host computer with a powerful debugger interface.

To see immediately what TI's new graphics processor can do for you, just plug the TMS34010 Software Development Board into an IBM® PC-compatible or TI Professional computer. The board is populated with TI's 34010 Graphics Processor, Color Palette, and VRAMs. It provides an ideal environment for developing your own high-performance graphics applications.

For more information on TI's total graphics-system solutions, including details on TI's Graphics Design Kit and design training courses, complete and return the coupon today. Or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

FOR FREE ON-LINE INFORMATION, dial 1-800-345-7335 with any 80-column ASCII terminal or PC and a 300 or 1200 baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type TIGRAFX. In Conn. dial (203) 852-9201.

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® IBM is a registered trademark of International Business Machines Corporation.

26-4537

To speed the design of your graphics system, TI's range of development tools includes a comprehensive design kit *(left rear),* a realtime emulator, and a plug-in software development board. On floppy and magnetic disks: "C" compiler, assembler package, and function and font libraries. User's guides, development books, product bulletins and data sheets, and TI's newsletter, *Pixel Perspectives,* are all readily available.

Hundreds of designers must be right.

Hundreds of hardware and software designers are making TI's 34010 the new graphics standard. Among them are leading board-development houses and major software vendors.

In fact, the wide range of graphics standards and application software already written for TI's 34010 makes it the easiest-to-use new graphics chip ever introduced. Here's just a sampling of the software that will run on top of Graphic Software Systems DGIS* 34010:

Software Products	Company
AutoCad™	AutoDesk
GSS*CGI™†	GSS
Master Series™	Ashton-Tate
Freelance Plus™	Lotus GPG
Graphics Development Toolkit™†	IBM
Harvard Presentation Graphics™	Software Publishing Corp.
ProDesign II™	American Small Business Computers
VersaCad™	VersaCad Corp.
Windows™†	Microsoft
Symphony™, 1-2-3™	Lotus Development
P-CAD™	Personal CAD Systems

™Trademarks are as noted.

†More than 100 graphics applications are currently available for these operating environments.

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P.O. Box 809066

Dallas, Texas 75380-9066

YES, please send me information on TI's Total Graphics-System Solutions.

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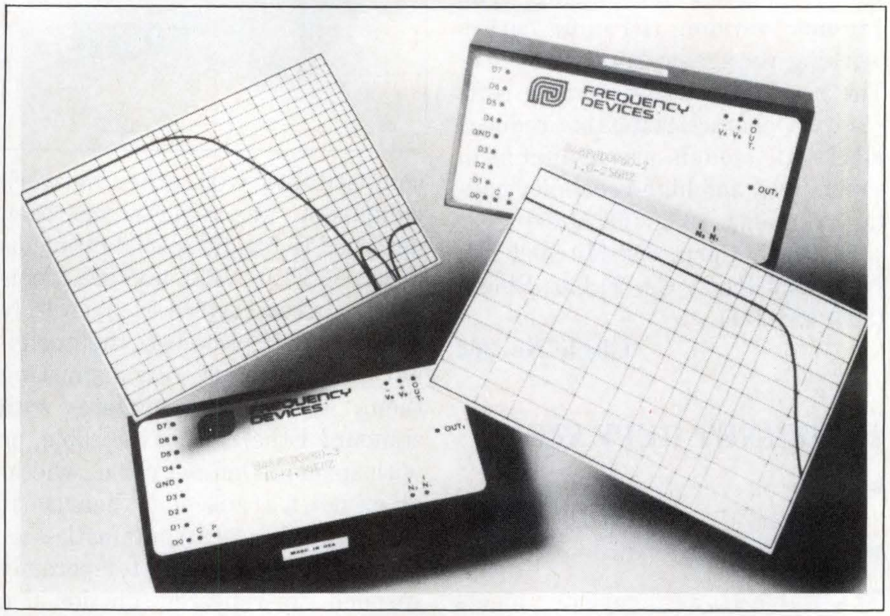
TEXAS INSTRUMENTS

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

ACTIVE FILTERS

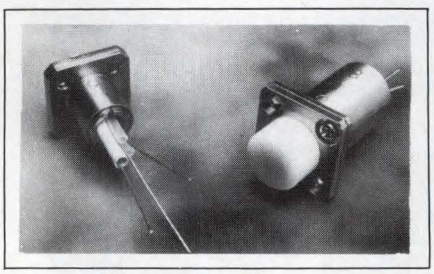
- *60- or 80-dB attenuation floor*
- *Tuning ranges to 51.2 kHz*



Series 848DOW lowpass active filters are tunable over a 256:1 range. They employ an 8-pole, 6-zero design to achieve a response that approaches the constant group delay of a Bessel filter in the passband and the sharper attenuation of a Butterworth filter in the stopband. Ten models offer a choice of a fixed 60- or 80-dB attenuation floor. Factory-set maximum corner frequencies range from 25.6 Hz to 51.2 kHz. All models contain CMOS latches that accept data and command inputs. You can configure these latches to transfer tuning data on either edge of an 80-nsec strobe pulse. The filter modules spec a ±0.5-dB noninverting gain, a 20-kΩ input impedance, and a 10Ω output impedance. They operate from ±12 to ±18V supplies. $300.

Frequency Devices Inc, 25 Locust St, Haverhill, MA 01830. Phone (617) 374-0761. TWX 710-347-0314.

Circle No 362



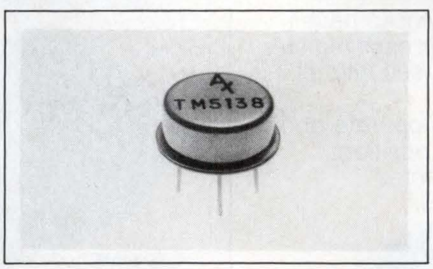
LASER DIODES

- *Designed for local-area network applications*
- *Spec lifetimes of eight million hours min*

Designed for short- and medium-haul local-area networks, the FU-05LD-N and FU-06LD laser-diode modules come with integral type-FC and -SMA connectors, respectively. They can deliver 1 mW into multimode, 50/125-μm fiber. Both modules include a back-facet photodiode for power monitoring, and they can operate at data rates exceeding 600M bps. The devices' lifetime (at 25°C) specs at eight million hours min. FU-05LD-N, $140; FU-06LD, $120 (10).

Mitsubishi Electronics America Inc, Semiconductor Div, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 363



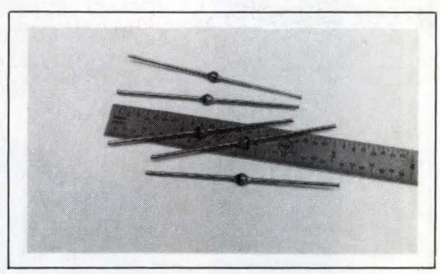
RF AMPLIFIER

- *Offers 15-dB typ gain*
- *Meets MIL-STD-883B screening*

Housed in a TO-8 hermetic package, Model TM 5138 provides a typical gain of 15 dB over the frequency range of 5 to 150 MHz. Other specifications include a 2.5 typ noise figure, 22-dBm output power at a 1-dB compression point, 2:1 input and output VSWR, and a −55 to +85°C operating range. The amplifiers meet MIL-STD-883B screening. Power requirements are 15V at 65 mA. $84.

Amplifonix Inc, 2010 Cabot Blvd W, Langhorne, PA 19047. Phone (215) 757-9600.

Circle No 364



SILICON RECTIFIERS

- *30-nsec recovery time*
- *Handle voltages to 5000V*

These hermetically sealed, glass-passivated, axial-lead silicon rectifiers feature a 30-nsec recovery time. They are available in 1A, 2A, and

180-mA versions. The 1A and 2A models (PFFX and 2PFFX, respectively) handle voltages from 200 to 1000V in 200V increments. The 180-mA version (PFF50) covers working voltages ranging to 5000V. The rectifiers operate with a soft-recovery characteristic that reduces EMI. All models are available in commercial and high-reliability military versions. $0.62 (OEM qty).

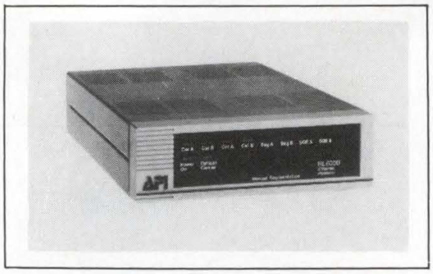
Semtech Corp, 652 Mitchell Rd, Newbury Park, CA 91320. Phone (805) 498-2111.

Circle No 365

ETHERNET REPEATER

- *Meets or exceeds the specs of Ethernet V2.0 and IEEE-802.3*
- *Handles mixed networks*

The RL6000L local repeater meets the stringent specifications of both the Ethernet V2.0 and the IEEE-802.3 standards to ensure complete



compatibility with other network equipment. The repeater has been designed to handle special problems of mixed V1.0, V2.0, and 802.3 networks. It can restore even severely distorted data packets to their original quality before retransmitting them. The repeater operates with standard Ethernet coaxial cable, or with smaller Thin-net cable, whether or not a transceiver heartbeat signal is present. An automatic-segmentation function will temporarily suspend the repeater function if a problem in one network section causes excessive data-packet collisions. The repeater also features manual segmentation switches, which are useful during installation and for network trouble-shooting and problem isolation. $1650.

American Photonics Inc, 71 Commerce Dr, Brookfield Center, CT 06805. Phone (800) 626-5745; in CT, (203) 775-8950. TLX 821353.

Circle No 366

FRONT PANEL

- *Incorporates an onboard μP*
- *Snap-dome switches provide an enhanced tactile feel*

This "smart" custom front panel incorporates a 2-line×40-character vacuum-fluorescent alphanumeric display and a module that includes an onboard μP. The display is mounted on a rigid panel, which also houses the keyboard. The keyboard uses snap-action dome switches to enhance tactile feel. The dome switches are covered with a polyes-

SMART CHANGE.

CHANGE TO CHOMERICS FOR LOW-COST, COMMERCIAL GRADE EMI GASKETS

We heard you. You've wanted commercial-grade conductive elastomers priced competitively with wire mesh, carbon-loaded silicone, and metal finger stock. You also want them to deflect under low closure force.

They're here. Introducing the CHO-SEAL® 1000 series of low-cost silver-filled elastomers that give you the performance you need—60dB EMI shielding in the 30MHz to 1GHz range.

They're available in a variety of innovative shapes, with attachment time-savers like pressure-sensitive adhesives, mounting clips, and frames for pop-rivets. They can also be produced as custom designs. And of course you get the dust-sealing, acoustic, and cosmetic benefits which elastomers provide.

You get something else, too. Chomerics' years of EMI shielding experience, reputation for quality, and the most reliable products in the industry.

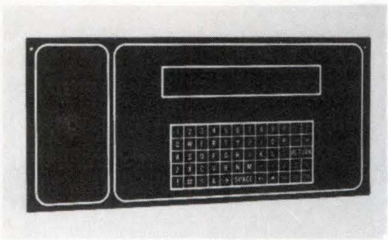
Make the smart change today. Call or write for the facts.

CHOMERICS
a GRACE company

77 Dragon Court, Woburn MA 01888
800-225-1936 (In MA: 617-935-4850)

CHOMERICS EUROPE
First Avenue, Marlow, Bucks, SL7 1YA England
(06284) 6030

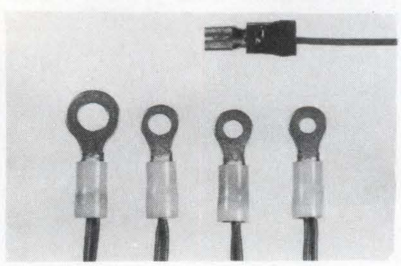
CIRCLE NO 82



ter legend sheet; graphics are printed on the rear surface for durability and scratch resistance. Almost anything that can be photographed can be permanently printed on the legend sheet, including graphics, symbols, corporate logos, and numbers. You can also incorporate other human-interface devices into these custom panels, including annunciators, joysticks, trackballs, illuminated switches, and multiple displays. Enclosures are also available. $550 (100). Delivery, 18 weeks ARO.

IEE Inc, Planar Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 367



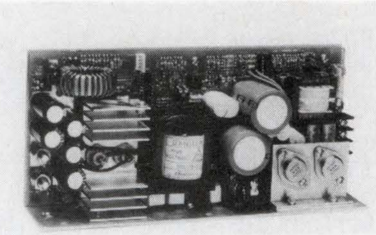
SENSORS

- *Are fully recyclable*
- *−55 to +150°C operation*

The Thermamount surface-mount ring sensors operate over a −55 to +150°C range. Unlike traditional protective devices, these NTC thermistors operate unattended and are fully recyclable. Resistance values (at 25°C) range from 50Ω through 5 MΩ, ±10%. The sensors are available in standard lug sizes of #6, #8, #10, and ¼ in. Tighter tolerances, special resistances, and extended operating ranges are available on special request. Units in the Thermamount family feature 3.8% to 6.1% coefficients of resistance. $4.75 (OEM qty).

Piezo Electric Products Inc, 212 Durham Ave, Metuchen, NJ 08840. Phone (201) 548-2800. TWX 710-998-0592.

Circle No 368



SWITCHING SUPPLIES

- *$4W/in^3$ power density*
- *80% typ efficiency*

V501 Series switchers are 500W, single-output supplies that offer a power density of $4W/in^3$. Standard outputs include 5V at 100A, 12V at 42A, 15V at 33A, and 24V at 21A. Specs include an efficiency of 80%, ripple and noise of 1% or 100 mV p-p, and a peak transient of less than ±2% or ±200 mV. The supplies are UL recognized, CSA certified, and licensed by TUV. Overvoltage protection is standard. Options include a power-fail monitor, thermal shutdown, and logic inhibit. $210 (OEM qty). Delivery, stock to eight weeks ARO.

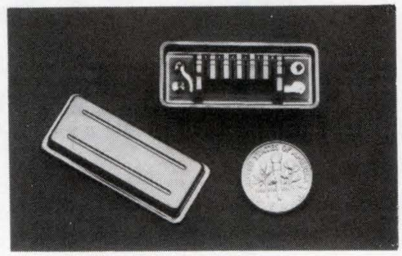
Deltron Inc, Box 1369, North Wales, PA 19454. Phone (215) 699-9261. TWX 510-661-8061.

Circle No 369

BANDPASS FILTERS

- *Insertion loss of less than 2 dB*
- *Center frequencies range from 125 to 525 kHz*

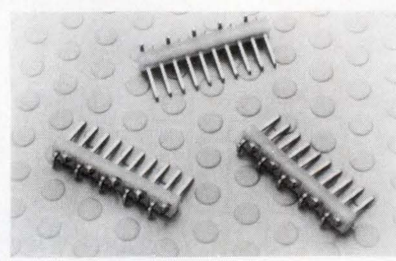
These bandpass filters feature torsional-mode resonators and a coilless transducer design. Insertion loss specs at 2 dB max, and the third-order intercept point is greater than 55 dB. Center frequencies



range from 125 to 525 kHz, with bandwidths ranging from 0.5% to 5% of the center-frequency value. The frequency-response characteristics range from equal-ripple passband responses to round-top Gaussian shapes, and the number of resonators can vary from one to as many as twelve. The filters are housed in hermetically sealed metal packages that are designed for pc-board mounting. $65 to $175 (100). Delivery, 6 to 13 weeks ARO.

Rockwell International, Filter Products, 2990 Airway Ave, Costa Mesa, CA 92626. Phone (714) 641-5311. TLX 685532.

Circle No 370



PIN-STRIP HEADERS

- *Straight- and right-angle versions*
- *94V-0 UL rating*

These surface-mount pin-strip headers and socket strips feature 0.025-in. square leads for the connector end and 0.1-in. pin-to-pin spacings. The board-side leads have a gull-wing configuration. Straight and right-angle versions are available in both product lines. The polyamid insulation material has a 94V-0 UL flammability rating. Pins are made of drawn phospher bronze with 50-μin. nickel underplating and 20-μin. gold plating at the contact

You've made power supplies smaller, lighter and quieter with a harmonica?

No, Harmonic Resonance!

Harmonic resonant, as a technology for our new line of power supplies, is practically as significant as going from linear to switching.

So, why did we develop it? It lets us make open frame switchers almost half the size of industry standards. Therefore, lighter. And quieter from a conductive noise standpoint. All for the same price you're paying now.

Of course, like all our power supplies introduced since 1983, this new 9S Harmonic Resonant line meets VDE, UL and CSA for safety. And VDE, FCC and IEC for conducted noise.

For more information on our new 9S Harmonic Resonant line (or where to get a nice harmonica), contact us today. Sierra Power Systems (formerly Sierracin), 20500 Plummer Street, Chatsworth, California 91311. Call toll-free (800) 423-5569. In California, (818) 998-9873.

Sierra Power Systems
Division of Valor Electronics, Inc.

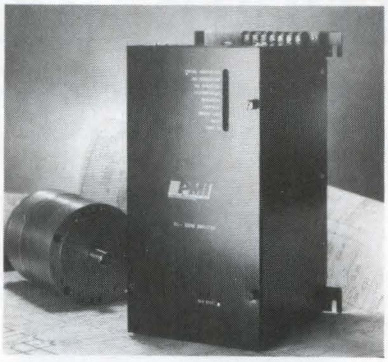
area. Other specs include a 5A current rating, 4-mΩ max contact resistance, and 5-GΩ min insulation resistance. Headers, $0.022 per pin; sockets, $0.032.

Carrot Components Corp, 750 W Ventura Blvd, Camarillo, CA 93010. Phone (805) 484-0540. TWX 910-336-1237.

Circle No 371

AMPLIFIER

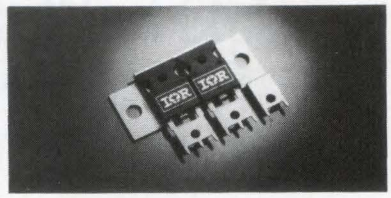
- *Simplified servo-system stabilization*
- *Suitable for dc motor requiring 900W of continuous power*



The Axa, a modular PWM, 4-quadrant amplifier, is for permanent-magnet dc motors that require as much as 900W of continuous power. It features such adjustments as peak-current limit, input gain, and offset. Adjustable compensation simplifies servo-system stabilization. Other features include velocity-loop or torque-mode operation, and a 1.01 form factor. Fault protection against excess current, logic-supply failure, and thermal overload is standard. The amplifier's self-diagnostic capability displays the actual fault condition. $778. Delivery, six to eight weeks ARO.

PMI Motion Technologies, 49 Mall Dr, Commack, NY 11725. Phone (516) 864-1000. TWX 510-223-0007.

Circle No 372



DIODE MODULES

- *133A rectified-output current*
- *Two anode input tabs and a single cathode output tab*

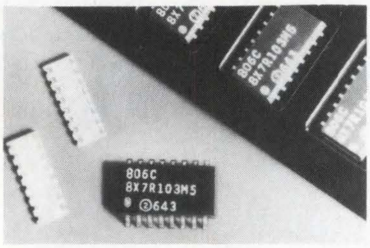
The 130C2PQ040 dual-die Schottky-diode modules handle a 40V repetitive-peak reverse voltage with an average rectified-output current of 133A. They are configured with two anode input tabs and a single cathode output tab integrated with the base plate. Key specs include an 800A nonrepetitive surge-current capability, a forward voltage of 0.55V at 60A, a 40-mA peak reverse current (at 25°C), 0.45°C/W junction-to-case thermal resistance, and

CIRCLE NO 93

a −40 to +125°C operating junction-temperature range. $14.91 (100). Delivery, eight weeks ARO.

International Rectifier Corp, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8837.

Circle No 373



CAPACITOR NETWORKS

- *Designed for surface mounting*
- *−55 to +125° operation*

Type 806C capacitor networks are for surface-mount applications. Each one integrates eight identical capacitors in miniaturized Cap-strate ceramic substrates and comes in a small-outline package. Finished networks measure 0.445×0.3 in. with leads on 0.5-in. centers. COG and X7R dielectrics are available. Respective capacitance values range from 27 to 2000 pF and 2000 to 47,000 pF. The operating range is −55 to +125°C. The rated voltage equals 100V at 85°C and 50V at 125°C. $1.50 (10,000).

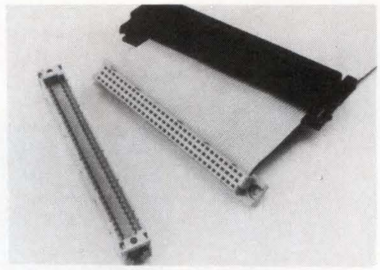
Sprague Electric Co, Box 9102, Mansfield, MA 02048. Phone (617) 339-8900.

Circle No 374

CONNECTOR SYSTEM

- *Meets DIN 41612 standards*
- *Maximizes use of board space*

The 64-position Scotchflex insulation-displacement connector (IDC) system includes a plug, a socket, a pinless header, related accessories, and assembly tools. The system

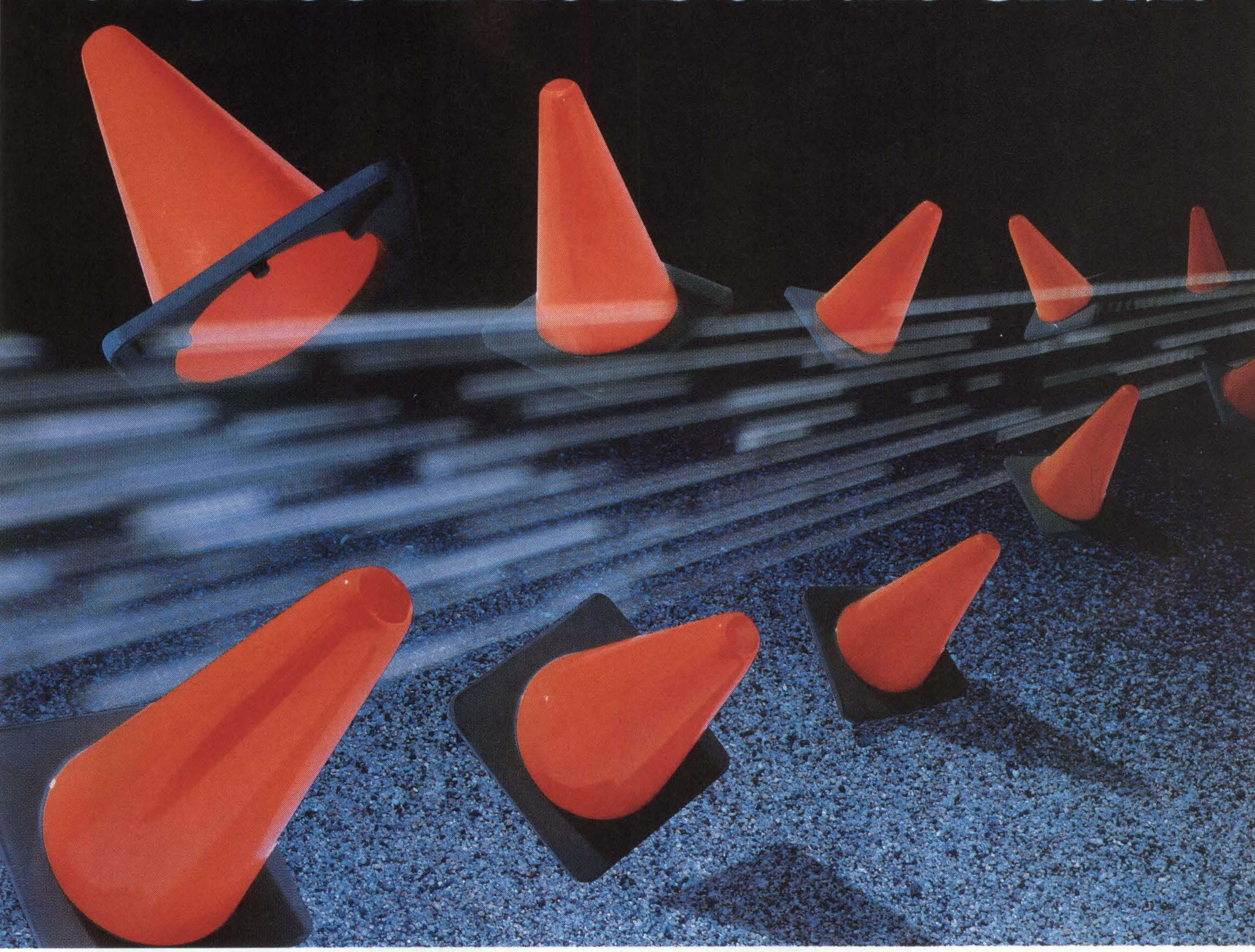


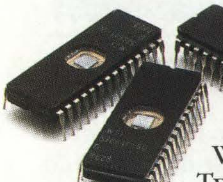
meets DIN 41612 blade-connector specs with controlled insertion-withdrawal force and 100% polarization. The DIN-compatible socket and plug allow daisy chaining, and the cover design allows closer stacking to maximize use of board space. The pinless header mates with the wrap posts of a 96-pin DIN connector. Assembly tools consist of hand-press locator plates for both the plug and the socket. Plug and socket, $6.34 (1000).

3M, Box 2963, Austin, TX 78769. Phone (512) 834-6563.

Circle No 375

Introducing the Fastest Family of CMOS EPROMs on the Circuit





WSI EPROMs: Twice as fast as the Pack.

WSI's family of CMOS EPROMs keeps you in the fast lane with access times as low as 55 NS, leaving systems with wait states in the dust. That means you can now turbo charge your system. With EPROM architectures ranging from 8K x 8 to 16K x 16.

WSI RPROMs: Bipolar speed with CMOS low power.

Our unique CMOS high-density Reprogrammable PROMs (RPROMs) match the speed of your favorite bipolar PROMs. So you can replace them with our pin-out compatible RPROMs. And get EPROM reprogrammability and low power consumption as well.

WSI: Puts you on track fast....... reliably.

Our EPROMs and RPROMs program in less than 16 seconds. Plus you get 200 MA of latch up protection and a minimum of 2000 V of ESD protection. So your production revs up faster. With more reliable, smoother running products.

Call the WSI team today.

With this kind of speed and reliability, it makes sense to check out WSI's EPROMs and RPROMs.

So call us at (800) 331-1030, ext. 234, or in CA. (800) 323-3939, ext. 234. And we'll get you on the road to higher performance today.

Waferscale Integration, Inc., 47280 Kato Road, Fremont, CA 94538

Part No.	Speed	Type
WS57C191/291	40 ns.	2k x 8 CMOS RPROM
WS57C43	55 ns.	4k x 8 CMOS RPROM
WS57C49	55 ns.	8k x 8 CMOS RPROM
WS57C64F	55 ns.	8k X 8 CMOS EPROM
WS57C128F	70 ns.	16k x 8 CMOS EPROM
WS57C256F	70 ns.	32k x 8 CMOS EPROM
WS57C65	55 ns.	4k x 16 CMOS EPROM
WS57C257	70 ns.	16k x 16 CMOS EPROM

WaferScale INTEGRATION, INC.

CIRCLE NO 177

NEW PRODUCTS

COMPUTERS & PERIPHERALS

GRAPHICS SET

- *Display system for IBM PC*
- *Includes coprocessor board, monitor, and software*

The PC4100 graphics coprocessor board, together with a multiple-line-rate monitor and terminal emulation packages, provide you with Tektronix-compatible graphics on an IBM PC. The set displays 256 colors from a palette of 16 million and is compatible with the IBM PC's EGA and CGA boards. The board offers a resolution of 640×480 pixels. In its terminal-emulation mode, the board provides higher resolution and speed. The emulation software allows the PC to run the company's 4107 terminal's mainframe-based software applications. Because the board supports the manufacturer's 4696 color ink-jet printer, you copy the screen directly without using any separate application program's printer drivers. PC4100 board, $1800; multiple-line-rate monitor, $950; emulation software, from $495.

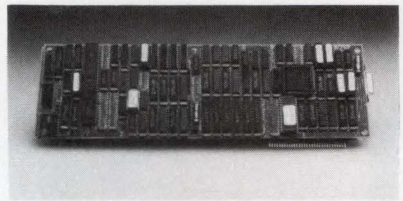
Tektronix Inc, Box 15273, Portland, OR 97215. Phone (800) 225-5434; in OR, (503) 235-7202.

Circle No 376

GRAPHICS CONTROLLER

- *High-resolution controller for IBM PC*
- *1024×768-dot resolution*

The 1004 display controller offers 16 colors from a palette of 4096 and has a screen resolution of 1024×768 dots. The board requires one slot in an IBM PC/AT or PC/XT. When it emulates the IBM CGA, the board displays text in a 960×600-dot window. The text's legibility is superior to that provided by CGA, EGA, or PGC controllers, the vendor claims. The controller's bit-slice architecture provides drawing rates from 5M pixels/sec for random vectors to 42M pixels/sec for fill operations. The board is compatible with a variety of interface standards (including Gem, Halo, VDI, and MS Windows)



and CAD packages (such as AutoCAD, CADkey, CADvance, Omnidraft, and P-CAD). $2995.

Metheus Corp, 5510 NE Elam Young Parkway, Hillsboro, OR 97124. Phone (503) 640-8000.

Circle No 377

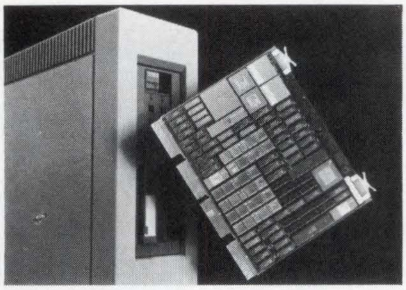
WORKSTATION

- *Desktop system runs VAX software*
- *Workstation's performance equals MicroVAX II's*

The VAXstation 2000 is a desktop workstation that performs on a MicroVAX II level. The basic system includes the MicroVAX CPU chip, the desktop system box, 4M bytes of memory, a built-in Ethernet adapter, a 3-button mouse, a keyboard, a software license, a 1024×864-pixel monochrome monitor, and a 1-year on-site warranty. A fully configured system includes the MicroVAX CPU chip; 6M bytes of memory; an expanded system box; a 71M-byte disk drive; a 95M-byte streaming-tape drive; the Ethernet adapter; a 3-button mouse; a keyboard; software licenses; a 19-in., 1024×864-pixel monochrome monitor, and a 1-year on-site warranty. Intermediate configurations are also available. $10,500 to $22,245.

Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Phone (800) 344-4835.

Circle No 378



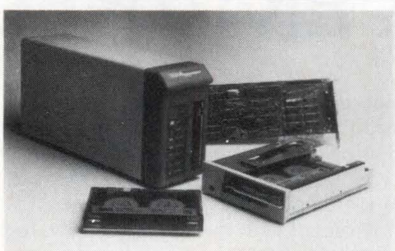
ARRAY PROCESSOR

- *Array processor for MicroVAX II*
- *Performs signal and image processing*

The MicroMSP-4 board performs numerically intensive signal and image processing 100 times faster than can an unaided MicroVAX II computer. The card occupies one slot in the backplane of a MicroVAX II. The board performs as many as 20M flops. It computes a 1024-point complex FFT in 4 msec, a 512×512 complex FFT in 2.5 sec, and FIR-filter tasks at 100 nsec/tap. $5950.

CDA, 411 Waverly Oaks Rd, Waltham, MA 02154. Phone (617) 647-1900. TLX 922521.

Circle No 379



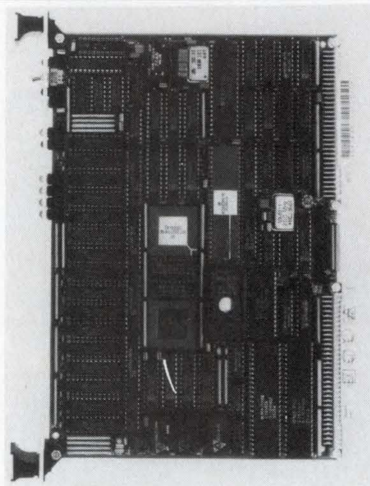
TAPE BACKUP SYSTEM

- *For IBM PCs*
- *Features 125M-byte capacity*

The QT-125 Series tape drives provide 125M bytes of storage in either an internal, half-height configuration or an external form. This Xenix-compatible system works with IBM PCs. It also works with Novell (Provo, UT), 3Com (Menlo Park, CA), and IBM token-ring LANs. The system offers file-by-file and mirror-image options for backing up and restoring at data rates as fast as 5M bytes/minute. Drive-utility software is included. QT-125i (internal system), $1895; QT-125e (external system), $2495.

Tecmar Inc, 6225 Cochran Rd, Solon, OH 44139. Phone (216) 349-0600. TLX 466692.

Circle No 380



SCSI BOARD

- *Has independent SCSI-bus and floppy-disk interfaces*
- *Incorporates 128k bytes of dual-port RAM*

The SYS68K/ISCSI-1 double-Eurocard board for VME Bus systems includes an ANSI X3T9.2 standard SCSI and a separate disk-controller chip that allows direct connection of as many as four floppy-disk drives. You can operate the SCSI, which can achieve data rates as high as 1.5M bytes/sec, in a synchronous or an asynchronous mode, as a SCSI-bus target or initiator. The board has an onboard, 10-MHz 68010 µP, which has zero-wait-state access to 128k bytes of dual-port static RAM (the other port goes to the VME Bus). Sockets are provided for as much as 128k bytes of EPROM, and the board comes with driver firmware to control the SCSI-bus and floppy-disk interface. Source code for the drivers is optional. In addition, the board has a 4-channel 68450 DMA controller. VME Bus access to the dual-port RAM is provided through an A24/D16/D8 VME Bus interface. The board also has a bus interrupter with four interrupt-request lines; the level and vector of each interrupt is software programmable. DM 4720.

Force Computers GmbH, Daimlerstrasse 9, 8012 Ottobrunn, West Germany. Phone (089) 600910. TLX 524190.

Circle No 381

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410. TLX 172465.

Circle No 382

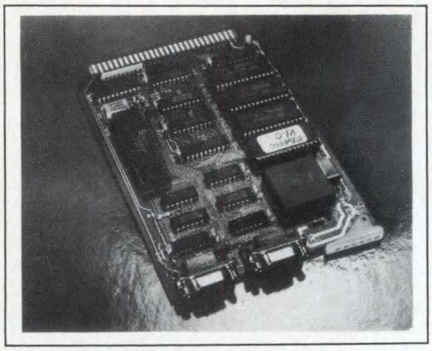
BAR-CODE READER

- *For the HP-94 handheld computer*
- *Optically programmable*

The HP Smart Wand is an optically programmable bar-code reader. If you use it with the HP-94 handheld computer, a software-development system, and software for host-computer data communications, you'll have a complete, portable data-collection system. The wand holds the decoding software for the bar-code reader, so the HP-94's memory remains free for application software. The reader recognizes major bar-code types, including Code 39, Interleaved 2 of 5, UPC/EAN/JAN, and Codabar. The scanner typically draws 9 mA in standby mode and 16 mA in operating mode. The reader can scan at angles from 0 to 45° at rates from 3 to 50 in./sec. $350.

Hewlett-Packard Co, 1000 NE Circle Blvd, Corvallis, OR 97330. Phone local office.

Circle No 383



SINGLE-BOARD μC

- *CMOS computer for the STD Bus*
- *Has a multitasking Basic compiler*

The BCPU64 is an STD Bus-compatible processor that is also compatible with the IBM PC. The card contains a multitasking Basic compiler, so you can run compiled code on an IBM PC or download it to the μP board and run it there. The board includes 64k bytes of battery-backed CMOS RAM, a battery-backed clock and calendar, two RS-232C ports, and an STD Bus timing generator. The timing generator permits the CPU to operate at 10 MHz without violating the bus timing specifications. In addition to the compiler, the board includes a debugger that runs on the IBM PC and an 8k-byte BIOS and operating-system kernel that runs on the board itself. Serial communication between the board and a PC conforms to ISO X3.28. $585.

Encel Systems Ltd, 5300 Memorial Dr, Atlanta, GA 30083. Phone (404) 292-3309.

Circle No 384

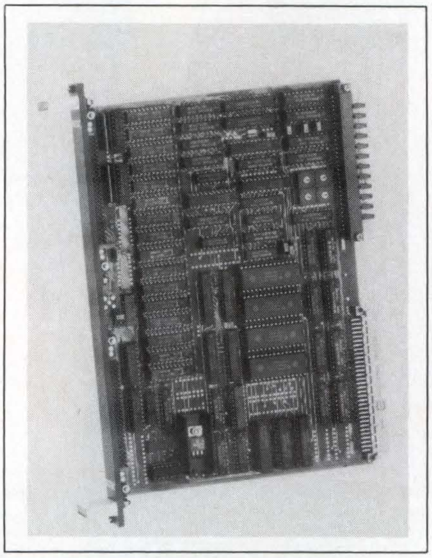
DISK DRIVES

- *Offer capacities from 168M to 689M bytes*
- *Support Novell's Netware software*

The N-8000 Series disk drives provide disk capacities of 168M, 374M, 510M, and 689M bytes of RAM. The drives have transfer rates of 2.45M bytes/sec (peak) and access times as low as 15 msec. The single-disk 689M-byte system is contained in an 11.5×5.5-in. package. Each drive features an SMD interface; by adding an NMSC 8600 controller, users of the Novell (Provo, UT) network can connect as many as four drives in daisy-chain fashion, thus making a 2700M-byte disk system. The 510M-byte disk system, $10,900.

National Memory Systems Corp, 335 Earhart Way, Livermore, CA 94550. Phone (415) 443-1669. TWX 910-386-6006. TLX 821892.

Circle No 385



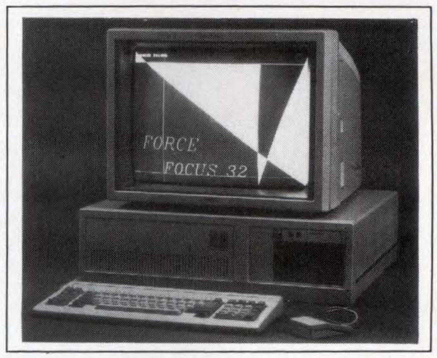
DATA INTERFACE

- *Transmits 16-bit data at rates as high as 30M bytes/sec*
- *Buffers data in 128k bytes of on-board RAM*

The Bift-1/68K interface board provides a 16-bit data interface capable of transmitting approximately 30M bytes/sec, plus 128k bytes of local buffer memory. It allows you to buffer high-speed data that's going to or coming from VME Bus systems. The board's separate 16-bit input and output ports operate asynchronously in conjunction with a 2-wire handshake and four control lines, or synchronously at programmable clock frequencies in the 100-kHz to 18-MHz range. A clock output allows you to synchronize such off-board devices as A/D converters. The double-Eurocard board includes a DMA controller for shifting data between the buffer memory and VME Bus global memory. The DMA controller operates in conjunction with a separate RAM/EPROM memory, into which you can program a user-defined target-address map. This map allows you to transfer any single 16-bit word in the buffer memory to a specified location in the VME Bus system. The board also includes a VME Bus interrupter with programmable vectors. DM 2900.

Eltec Elektronik GmbH, Galileo-Galilei-Strasse 11, 6500 Mainz 42, West Germany. Phone (06131) 50031. TLX 4187273.

Circle No 386



COMPUTER

- *Has 32-bit access to local RAM, EPROM, and VME Bus*
- *Includes intelligent serial I/O and SCSI-bus cards*

The Focus-32 PDOS System 21A is a fully cased, 12-slot VME Bus computer equipped with five VME Bus slots occupied by CPU, memory, serial-interface, mass-storage-interface, and system-controller cards. The card slots are arranged in two horizontal stacks of six slots each, and they include both J1 and J2 backplanes. You can mount the unit in either a tabletop or a tower configuration. The CPU card has a 20-MHz 68020 μP, a 68881 math coprocessor, 512k bytes of zero-wait-state static RAM, space for as much as 512k bytes of EPROM, two serial I/O lines, and a VMX Bus primary master interface. All the

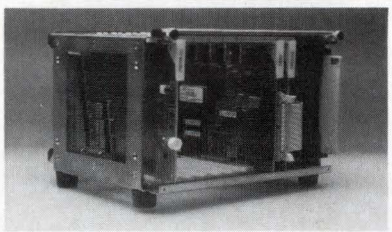
data pathways to local RAM and EPROM, and to the VME Bus, are 32 bits wide. The RAM card provides another 512k bytes of 32-bit, zero-wait-state local RAM. The serial I/O card, which has an onboard 68010 µP, provides eight more serial I/O channels. The system's mass-storage devices, which include an 80M-byte Winchester disk drive, a 1M-byte floppy-disk drive, and an optional 50M-byte streaming-tape drive, are controlled via the system's 68010-based intelligent SCSI-bus controller card. The VME Bus system-controller card includes an IEEE-488 interface and a real-time clock. System 21A with PDOS operating system, DM 44,950.

Force Computers GmbH, Daimlerstrasse 9, 8012 Ottobrunn, West Germany. Phone (089) 600910. TLX 524190.

Circle No 388

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410. TLX 172465.

Circle No 389



INDUSTRIAL µC

- *IBM PC-compatible µC for factory environment*
- *Operates over 0 to 65°C*

The System 2 computer is an IBM PC-compatible computer that operates from 0 to 65°C, can withstand 10G of shock, and offers an MTBF of >5 years at 55°C. This STD Bus-based computer runs Microsoft's MS-DOS 3.2 operating system. The central processor is a 5-MHz NEC V20 CMOS CPU, which is 8088-compatible. Model 10 comes with 128k bytes of CMOS static RAM that's expandable to 640k bytes, and a RAM disk; a 20M-byte hard-disk drive is optional. Model 20 has a 3½-in. floppy-disk drive; a second floppy-disk drive and a 3½-in., 20M-byte hard-disk drive are optional. Model 10, $1195; Model 20, $1595.

Pro-Log Corp, 2560 Garden Rd, Monterey, CA 93940. Phone (800) 538-9570; in CA, (408) 372-4593.

Circle No 390

DISK SYSTEM

- *Q Bus-compatible hard-disk cartridge system*
- *26M-byte cartidges*

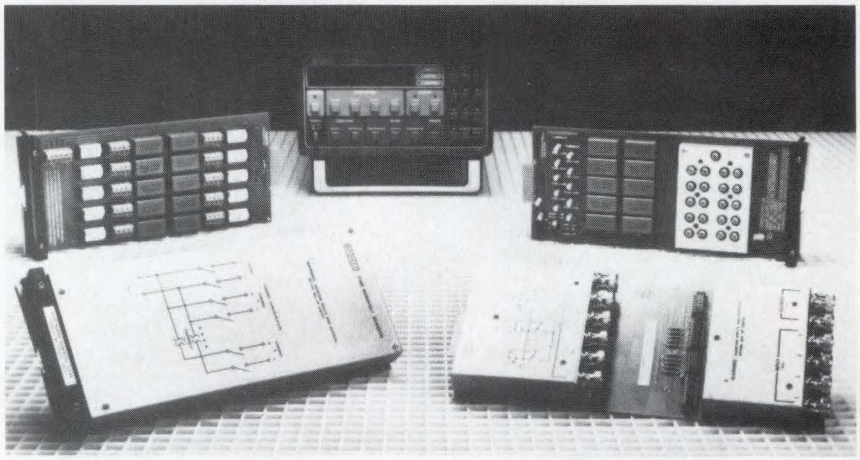
The Datasafe family of DEC Q Bus-compatible Winchester disk subsystems, which use twin-drive Winchester technology, includes a 5¼-in. 26M-byte hard-disk cartridge drive coupled with a 5¼-in. fixed Winchester drive. Models are available with 80M, 110M, 165M, and 226M bytes of storage capacity. A dual removable-drive model with 52M bytes of capacity is also available. In each model, the two drives run on separate spindles and are housed together in a 5×19-in. NEMA rack-mount or tabletop enclosure. All the drives run standard LSI-11 and MicroVAX operating software. All storage is accessed as if it were DEC DU devices, and the subsystem operates with standard DU drivers. The dual-wide Q Bus controller implements DEC's MSCP protocol, supports both 18- and 22-bit addressing, and controls both the fixed- and the removable-disk drives. $4995.

Winchester Systems, 400 W Cummings Park, Woburn, MA 01801. Phone (800) 325-3700; in MA, (617) 933-8500.

Circle No 391

SCANNER CARDS

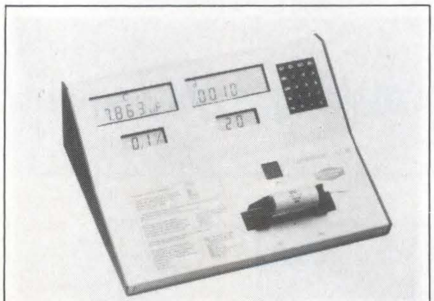
- *Cards fit scanner mainframes*
- *Include nanovolt scanner and low-current scanner*



Increasing the company's scanner-card line to 17 products, these four scanner cards fit either of the company's scanner mainframes. The 7168 nanovolt scanner is an 8-channel, 2-pole unit that offers 20-nV differential contact potential between its channels. The 7158 low-current scanner can switch currents as low as 1 pA. The 7158 is a 10-channel card whose two outputs connect several scanner cards in a single system to one instrument. The 7067 4-wire or Kelvin scanner has both current-source and low-voltage-sensing channels. The 7402 thermocouple scanner is a 9-channel unit that has built-in cold-junction compensation. 7168, $1995; 7158, $950; 7067, $630; 7402, $500.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469.

Circle No 392



LCR BRIDGES

- *Automatic bridges can sort components into bins*
- *RS-232C and IEEE-488 interfaces are standard*

The CT10 and CT20 are automatic LCR bridges having 0.05% accuracy. The CT10 applies test signals at 111 Hz and 1 kHz. It can sort components into nine bins according to a primary characteristic and into a single bin according to a secondary characteristic. The CT20 adds a 10-kHz test signal and can sort components into 12 bins for a primary characteristic and four bins for a secondary characteristic. The CT20 measures a component in 50 msec. Both bridges come with RS-232C and IEEE-488 interfaces. CT10, $4200; CT20, $6200.

RE Instruments Corp, 31029 Center Ridge Rd, Westlake, OH 44145. Phone (216) 871-7617.

Circle No 393

DIGITIZER

- *Instrument digitizes at 200M samples/sec*
- *Unit features envelope-mode triggering*

The RTD 710 dual-channel waveform digitizer has a single-channel digitizing rate of 200M samples/sec. It digitizes two channels simultaneously at 100M samples/sec, and its vertical resolution is 10 bits max. The instrument has a 64k-sample memory (32k samples/channel). A direct digital output is available. You can trigger the instrument on complex signals or when the input differs from a preset envelope. The unit's IEEE-488 interface can transfer data at 250k bytes/sec. $19,950.

Tektronix Inc, Box 1700, Beaverton, OR 97075. Phone (800) 547-1512; in OR, (800) 542-1877.

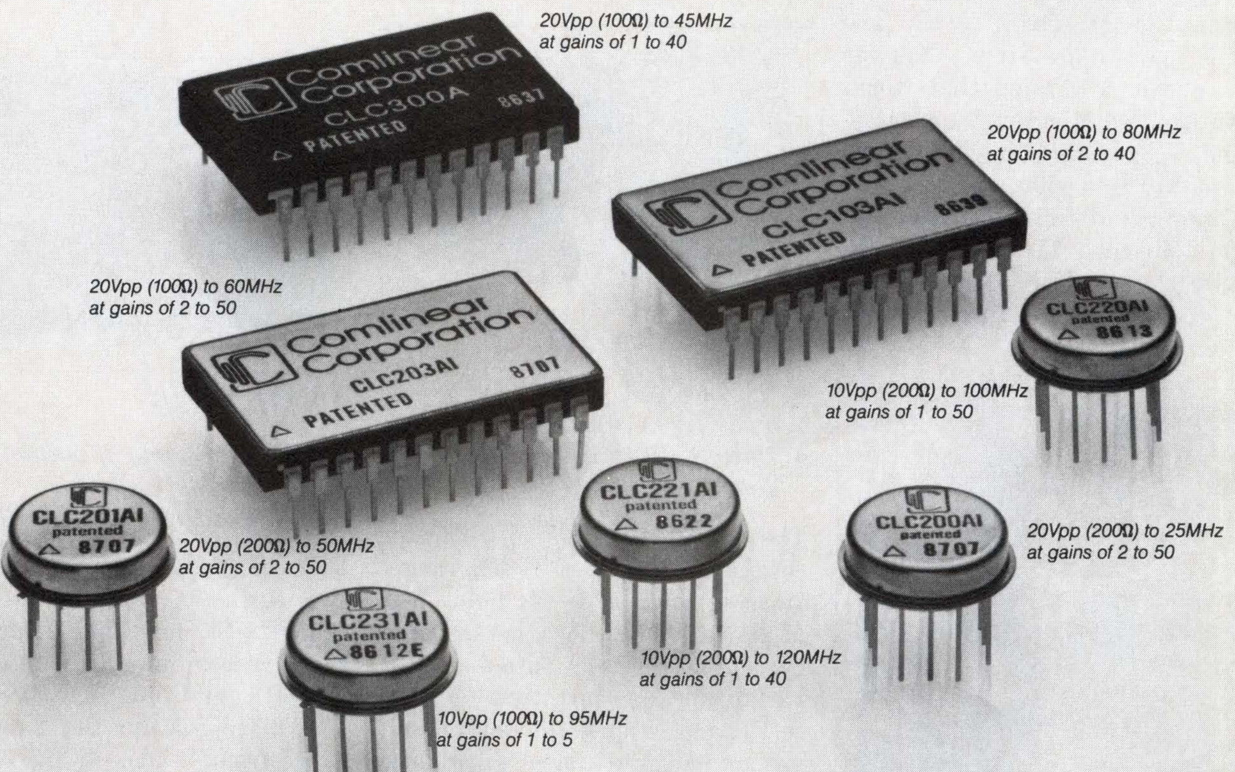
Circle No 394

80286 DEBUGGER

- *80286 debugger runs under iRMX 286*
- *Works with third-party in-circuit emulator*

The iRMX 286 version of the company's Soft-Scope 80286 debugger pro-

Expand your bandwidth and maintain your gain...



with these high-speed, high-drive op amps from Comlinear

With this op amp family, you don't sacrifice speed for gain. . . or for power. Because Comlinear designs eliminate traditional performance tradeoffs. Check the specs.

But there's more than performance. You also get complete min/max and over-temperature specifications. DC and AC parameter testing on every part. Unmatched ease of use (all are unity-gain stable, without compensation). Plus evaluation boards and top-notch design support. Which adds up to design productivity and confidence.

To expand your bandwidth, call (303) 226-0500 today. Or write Comlinear Corporation, 4800 Wheaton Drive, Fort Collins, Colorado 80525.

SPECIFICATIONS (Typical)

	−3dB Bandwidth (MHz) $A_v=4$	$A_v=40$	Settling Time to 0.1% (nsec)	Slew Rate (V/μsec)	Output (±V, mA)
General Purpose					
CLC103	170	130	10 (to 0.4%)	6000	11,200
CLC200	100	90	18	4000	12,100
CLC220	200	160	8	7000	12,50
CLC300	105	70	20	3000	10,100
Low Offset ($V_{OS} \leq 1mV$, 10μV/°C)					
CLC201	100	90	18	4000	12,100
CLC203	180	130	15 (to 0.2%)	6000	11,200
CLC221	200	120	15	6500	12,50
CLC231[1]	165 ($A_v=1$)	120 ($A_v=5$)	12	3000	11,100

Comlinear Corporation

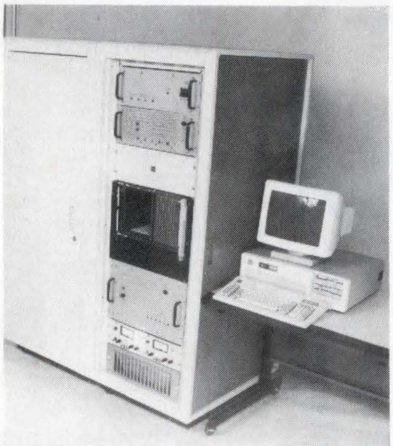
087101

Circle 31 for general purpose op amp information

Circle 70 for low offset op amp information vides full support for the 80286's protected mode, including the handling of hardware-protection traps. The source-level debugger can run programs written in Intel's PL/M, C, Pascal, Fortran, and assembly language. It displays all variable types including Pascal records, PL/M and C structures, multidimensional arrays, and real types. Other versions of the debugger run under the MS-DOS, ISIS, and iNDX operating systems. You can also obtain a version that works with Applied Microsystems' (Redmond, WA) ES 1800 in-circuit emulators. $1000 to 1500.

Concurrent Sciences Inc, Box 9666, Moscow, ID 83843. Phone (208) 882-0445. TLX 4942758.

Circle No 395



MATE ATE

- *Commercial-grade MATE ATE system uses IBM PC*
- *ATE system suits factory environment*

The Factory Mate 390 ATE (automatic test equipment) system is suitable for use in factories that produce MATE-compatible products. The system can have as many as 240 test pins with 16k bits of pattern/capture memory per pin. It also includes four programmable clocks that have 10-nsec resolution and three programmable power supplies. Its software includes an editor and an Atlas compiler. A representative system with a 120-pin, 20-MHz digital subsystem and basic analog functions (including a timer/counter, DMM, and frequency synthesizer) costs $250,000. Delivery, six months ARO (typ).

GAI Inc, 21 White Deer Plaza, Sparta, NJ 07871. Phone (201) 729-5888. TLX 910-380-0362.

Circle No 396

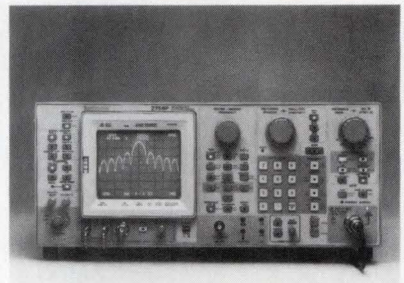
RF GENERATOR

- *Includes AM, FM, and phase-modulation capabilities*
- *Has a built-in AF generator and sinad meter*

The PSG1000 RF signal generator covers the 10-kHz to 1-GHz range. Its resolution is 10 Hz below 128 MHz and 100 Hz above that frequency. The generator's output level is variable in the range from 0.05 μV to 1V, and because the unit doesn't use frequency doublers to produce its high frequency ranges, the output isn't corrupted by subharmonics. The standard unit's modulation capabilities include amplitude, frequency, and phase modulation; pulse modulation is available as an option. In addition to 1-kHz fixed-tone modulation, the PSG1000 has an audio frequency synthesizer that generates modulation frequencies between 10 Hz and 10 kHz. The unit also has an external modulation input, which you can dc-couple. You can select multiple modulation unsquelching tones to test CTCSS, CCIR, EEA, ZVEI-1/2, EIA, Natel, and Selcall systems. The built-in sinad meter simplifies receiver-alignment checks. The nonvolatile memory allows you to store front-panel setups, and an IEEE-488 remote-control interface is standard. Control via a handheld calculator is optional. The PSG1000 operates from line supplies or from 12V (optionally 24/28V) dc supplies. £3250.

Farnell International Instruments Ltd, Sandbeck Way, Wetherby, West Yorkshire LS22 4DH, UK. Phone (0937) 61961. TLX 55478.

Circle No 397



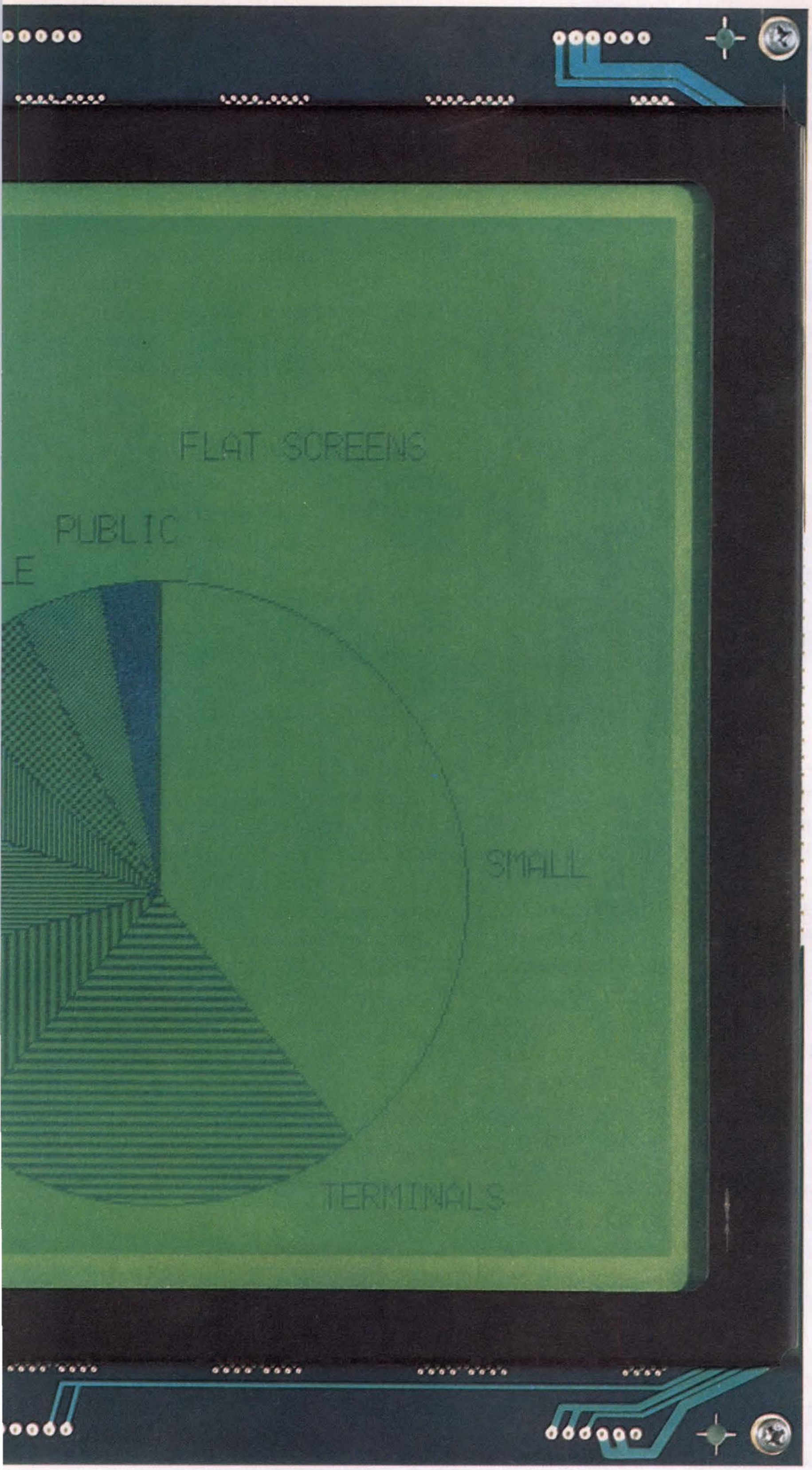
ANALYZERS

- *Analyzers come in portable and lab versions*
- *MATE interfaces are available*

Five spectrum analyzers pad out two of the company's lines: The 2756P, 2753, and 2753P enlarge the 2750 Series, and the 494A and 494AP round out the 490 Series. The 2756P covers the frequency range from 10 kHz to 325 GHz. It has −134-dB sensitivity and 10-Hz resolution. The 494A and 494AP are portable analyzers whose performance specs are identical to those of the 2756P. The 2753 and 2753P cover 100 Hz to 1.8 GHz and have built-in signal processing. An option allows the analyzers to understand MATE/CIIL commands. The "-P" models are programmable versions. 2756P, $46,245; 2752/2753P, $26,250; 494A/494AP, $41,425. Delivery, 15 weeks ARO.

Tektronix Inc, Box 15149, Portland, OR 97215. Phone (800) 835-7732; in OR, (503) 235-7315.

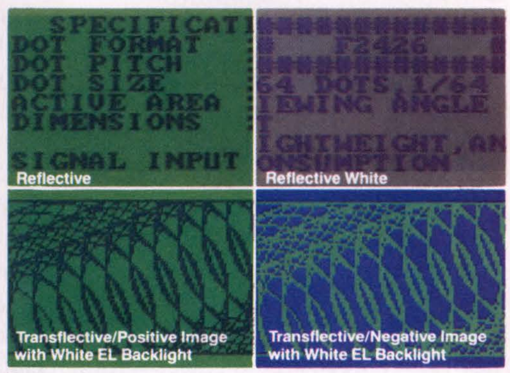
Circle No 398



Seiko's 640 X 400 Dot Graphic Display Gives You High-Quality Contrast And Wide Viewing Angle In A Compact, Low-Power Package.

SEIKO'S advanced engineering programs have produced a dramatic improvement in LCD display technology. The new "Seiko Twist" LCD display module combines improved visual performance and flexibility in an economical, flat panel package.

"Seiko Twist" modules are available with anti-glare polarizer in the most popular configurations. Options include reflective or transflective mode, and positive or negative character image. Optional electroluminescent (EL) backlighting is available for limited light environments.



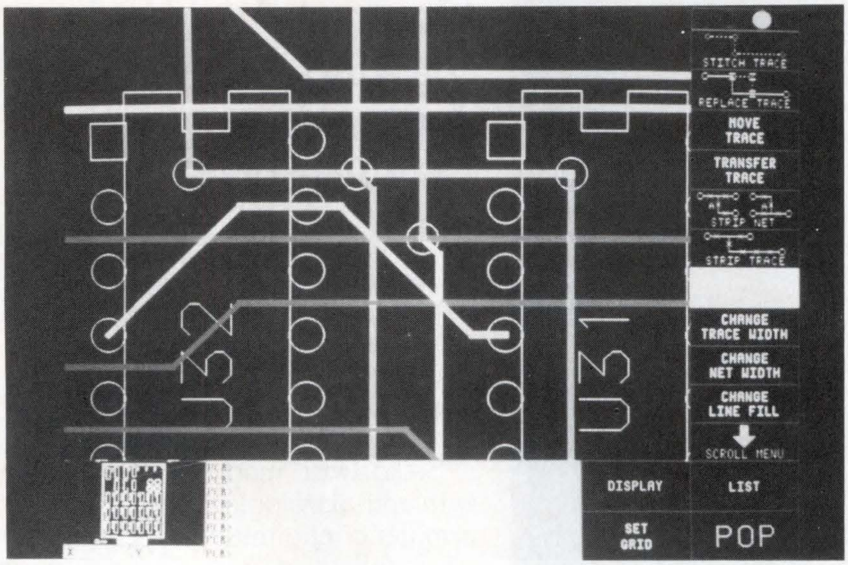
Optional screen configurations

Seiko Twist

So, if you need a flat-panel display with the viewing area of a CRT, call today for information on the "Seiko Twist." Any way you look at it, SEIKO is your first choice for displays.

SEIKO INSTRUMENTS U.S.A., INC.
2990 W. Lomita Blvd.
Torrance, CA 90505
PHONE: (213) 530-8777
TWX: 910-347-7307
FAX: (213) 539-8621

SEIKO INSTRUMENTS



PC-BOARD DESIGN

- *Lets you design and route buried vias*
- *Allows direct communication with simulators and testers*

The Board Series programs let you design and route high-density, multilayer pc boards that contain blind vias (those that are visible but don't go all the way through the board) and buried vias (those that are inside the pc board and are invisible on the surface). You can also use one power plane for two or more voltages and embed signal traces within a given power plane. A net-list interface lets you pass net-list information from another CAE system to this software for layout and routing; you can then pass pin numbers, reference designations, and similar information back to the CAE system for back-annotation and documentation. The Board series consists of four packages that all run on Apollo DN570, DN3000, or DN3000+ workstations and have different capabilities to suit different applications. The Designer package provides full design capabilities, including schematic capture, packaging and pin assignment, autoplacement, interactive and automatic routing, simulation, and CAM capability. Editor Plus has the same design and layout features as Designer, but does not include routing or CAM features. Scribe performs only schematic capture and packaging. Editor and Scribe are intended for use as low-cost nodes on an Apollo 3000 that's linked to another workstation running Designer. Likewise, Expeditor is a high-performance routing package that provides CAM features but needs to be linked to Designer for full design capability. $30,000 to $90,000.

Calma Co, 501 Sycamore Dr, Milpitas, CA 95035. Phone (408) 434-4000. TLX 3720067.

Circle No 399

ENHANCED CAD TOOL

- *Lets you define line widths*
- *Allows you to exchange drawings with other CAD systems*

Generic CADD version 3.0 is the latest version of a drawing tool that runs on the IBM PC and compatibles. According to the vendor, version 3.0 runs as much as 20% faster than previous versions. The enhancements include user-defined line widths; the ability to restore the last four items that you erased; and a feature that lets you name a view displayed on the screen as a separate file, and retrieve or plot that view while you're working on another part of the drawing. The plotting module lets you plot drawings made with the program on any one of more than 100 dot-matrix and laser printers. You can also exchange drawings with AutoCAD, Ventura, and other software that uses the DXF (Drawing Exchange Format). An autodimensioning module automatically inserts dimensions, legends, extension lines, leaders, and arrows as you define them. Another module lets you exchange drawings with minicomputer and mainframe CAD software that uses the IGES (International Graphics Exchange Standard) format. $99.95.

Generic Software Inc, 8763 148th Ave NE, Redmond, WA 98052. Phone (206) 885-5307.

Circle No 400

CAD DRIVERS

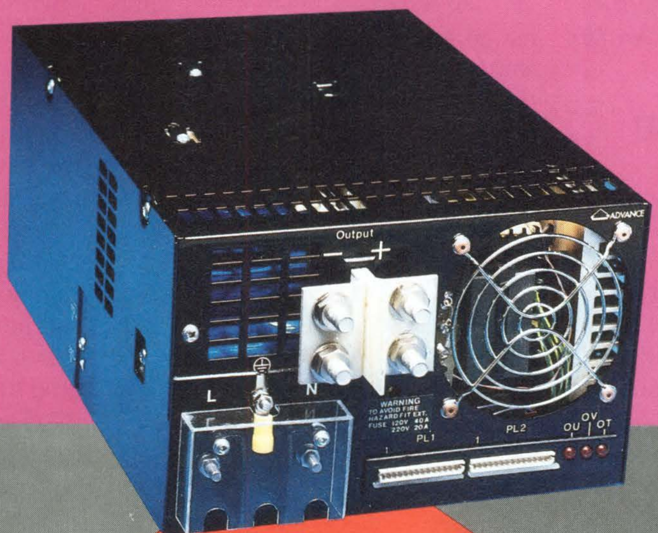
- *AutoCAD driver-update disk*
- *For dot-matrix and laser printers*

The driver-update disk for AutoCAD, which runs on the IBM PC, includes new drivers for 10 I/O devices and upgraded drivers for six other I/O devices. The new drivers let you use AutoCAD with the Advanced Matrix Technology (Newbury Park, CA) Office Printer, the Cordata LP300X Laser Printer, the Cordata 400 Display, the H-P HIL Digitizer, the H-P Mouse, the IBM Proprinter and Proprinter XL printers, the Metheus (Hillsboro, OR) Omega-PC Display with version 2.2 microcode, the Postscript Writer for laser printers, and the Toshiba 3-in-One Printer/Plotter.

NEW

Powermag A1500.

Packs 1500 Watts of dependable power in a compact unit.



Five volts of regulated DC power at up to 300 Amps and failsafe redundancy! That's what the new Powermag A1500 Switching Power Supply delivers.

This 5″ x 8″ x 11″ high power-density 1500-Watt unit from Advance Power Supplies provides 3.4 Watts per cubic inch from either 110V or 220V nominal, 47 to 440 Hz input. It's perfect for systems using large amounts of solid-state mass storage.

Virtually any number of Powermag units can be interconnected to provide parallel redundancy and meet heavy power demands. Current-sharing capability is built-in, so each unit shares the load equally. Should one unit fail, the others will automatically redistribute and assume the load (up to their rated capacities). And the Powermag meets major international safety and RFI requirements.

Standard features include electronic soft-start; self-diagnostics; overcurrent, overvoltage and overtemperature protection; selectable dual-input voltage; local and remote sensing; and full-cycle holdup. A variety of signal facilities and optional output voltages (2V, 12V, 24V, 48V) make the Powermag A1500 one of the most versatile power supplies available.

For complete details on the high-power, affordably priced Powermag A1500, contact your Advance Power Supplies representative. Or call (216) 349-0755.

Advance Power Supplies
32111 Aurora Road
Solon, OH 44139

ADVANCE
POWER SUPPLIES

CIRCLE NO 64

703-008

Both the new and the replacement drivers are standard in version 2.52 of AutoCAD; users of earlier versions can purchase the update disk separately. $80.

Autodesk Inc, 2320 Marinship Way, Sausalito, CA 94965. Phone (415) 331-0356.

Circle No 401

CAD FOR MACINTOSH

- *For 2- and 3-D designing*
- *Has animation features and removes hidden lines*

SpaceEdit is a 2- and 3-D CAD software package that runs on an Apple Macintosh equipped with 512k bytes of memory. If your system has an onboard floating-point coprocessor, the program will use it. You can create drawings with the mouse, the keyboard, or a digitizing tablet. You can send output to a laser printer or a plotter. The software offers unlimited zooming; a hidden-line remover; windowing; rotation of an image about the X, Y, and Z axes; and 3-D animation. You can export images created with the program to MacDraw, MacPaint, MacDraft, and other graphics programs. $625.

Abvent, 9903 Santa Monica Blvd, Suite 268, Beverly Hills, CA 90212. Phone (213) 659-5157. TLX 4949496.

Circle No 402

MODULA-2 COMPILER

- *Generates native 8086/88 code*
- *Comes with a Make utility*

This Modula-2 compiler provides all features of the language as Niklaus Wirth defined them in *Programming in Modula-2.* The compiler generates native 8086/88 machine code in files that are compatible with most MS-DOS and PC-DOS link utilities. On the first pass, the program performs all lexical and syntactical analysis and generates an intermediate file; the second pass only processes internal symbols from the executable code, so you can use symbols before defining them. The distribution disk includes source code for the low-level PC-DOS interface, which is coded in assembly language, and source code for several other modules. The package comes with a Make utility similar to that of Unix and complete source and object code for the run-time system. The vendor does not charge royalties for run-time object code distributed as part of an application, and the compiler is not copy-protected. Complete package, $89.95; manual only, $25.

Farbware, 1329 Gregory, Wilmette, IL 60091. Phone (312) 251-5310.

Circle No 403

HYBRID-CIRCUIT CAE

- *Generates automatic thick-film resistors*
- *Runs with vendor's graphics system*

The hybrid-circuit design module for thick-film circuits is a CAD module that runs with the vendor's Engineering Graphics System. It can operate in conjunction with other modules of the company's Electronic Design System. All the software modules run on the HP 9000 Series 200 and 300 workstations. The software's automatic and interactive features include automatic thick-film-resistor generation; a starter library containing more than 300 hybrid parts and subparts; and the ability to work with irregularly shaped conductors and to add dielectric crossovers. You can specify either English or metric units; the schematic-drawing module automatically generates a parts list. A rat's-nest generator lets you add connectivity information between parts. Using the editing features, you can move, rotate, stretch, or mirror parts or conductors on a grid that provides a resolution of 0.00001 mil; placement-snapping modes ensure that the parts and conductors are precisely placed. You can vary the width of the conductors; system messages help you to route multilayer conductors. You can also generate a connection list from your completed layout. A connection-list comparison program ensures that this list agrees with the list generated by the schematic-drawing module. Design module, $4000; the engineering-graphics module, $6000; optional schematic-drawing module, $1000.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 404

FILTER DESIGNER

- *Selects the filter types that produce a desired response*
- *Works with elliptic filters that use VCVS circuits*

Active Filter Design version 2.10 prompts you to specify a frequency response; it then presents a menu of filter types that produce this response. For each type (Butterworth, Chebyshev, elliptic, and Bessel), the program shows the required filter order and the stopband attenuation. In addition, you can enter pole and zero locations, or a transfer function, from the keyboard and instruct the program to generate the desired filter configuration from that data. The software works with manual or automatic pole-zero pairings, as well as with uneven gain distribution. It can also calculate the component values required to implement your filter by means of MFB (multiple feedback),

VCVS (voltage-controlled voltage source), biquad, state-variable, or Reticon switched-capacitor techniques. The program can produce a filter description, pole-zero locations, transfer functions, and component values, as well as the amplitude, phase, and group-delay frequency response of the complete filter or of any individual filter section. You can store the data in a disk file for later analysis or modification. A companion program converts the circuit file created by the design package to a Spice-compatible net list. The programs run on IBM PC-family and compatible computers having at least 350k bytes of RAM and PC-DOS 2.0 or a later version. The programs can use an 8087 numeric coprocessor. Design package, $525; Spice file-conversion program, $125; both, $625.

RLM Research, Box 3630, Boulder, CO 80307. Phone (303) 499-7566.

Circle No 405

PLD DATABASE

- *Lists device makers and specs*
- *Enhances Log/ic design package*

This database of programmable logic devices works with the vendor's Log/ic logic-design package that runs on IBM PC and VAX hosts. The database lists manufacturers of PLDs, the devices they supply, and the technical specifications for each part. When operating the design package with the database, you can compile a program that will give you a list of specific parts that will work with your design. For example, you can obtain a list of any 20-nsec PALs from MMI that will work with your design. You can also search for parts by using any of the other specs listed in the database as criteria. The database also lets you display the characteristics of any PLD in the library, including the number of product terms per input, the number of inputs and outputs, and the electrical characteristics of the device. The company issues PLD database updates three times per year; you can review each update before purchasing it. From $500 for the IBM PC version. Delivery, six weeks ARO.

Kontron Electronics, 630 Clyde Ave, Mountain View, CA 94039. Phone (415) 965-7020.

Circle No 406

CAE NETWORK

- *Ethernet link uses thin cable*
- *25 PCs can share central file server*

Dash-Net allows engineers working on a common project to share central design libraries and databases and to communicate with VAX computers that use the TCP/IP protocol. The network is fully compatible with the company's CAE tools. The network has three main components: a DN3-Server, which serves as many as 25 workstations and includes a 70M-byte disk, 960k bytes of memory, and a 60M-byte cartridge-tape-backup unit; the DN-Station Ethernet board and network at each node; and DN-CABL Ethernet cable. DN3-Server, $11,950; DN-Station hardware and software, $650 per node; DN-CABL, $45 (7m) to $200 (100m).

FutureNet, 9310 Topanga Canyon Blvd, Chatsworth, CA 91311. Phone (818) 700-0691. TWX 910-494-2681.

Circle No 407

STRUCTURED ANALYSIS

- *Automates system-requirements modeling*
- *Uses Yourdon-DeMarco data-flow techniques*

SA Tools-IBM PC is a structured-analysis tool that allows analysts and engineers to define system requirements with the aid of Yourdon-DeMarco data-flow diagrams, a data dictionary, and minispecifications. You can nest the data-flow diagrams

Superior Electric gives today's motion control the feel of the future with its completely new family of step motor drives and programmable motion controllers—THE SLO-SYN® MICRO SERIES.

superior innovation in MOTION CONTROL

Micro size. Here are the smallest, most powerful step motor drive modules available today. Optically isolated and designed for top efficiency, these chopper drives are rated 2A and 3.5A per phase, 30VDC, 20kHz.

Micro processor based, data-driven programmable preset indexers and motion controllers use industry standard machine tool language RS274 X, G and F codes for maximum application flexibility. Program storage up to 400 lines, 2 programmable inputs, 2 programmable outputs and overtravel limit switches. Provide RS232C interface, parallel switch interface and PLC operating mode. Up to 99 units can be daisy chained.

Micro stepping AC line operated step motor drives of the 3180 Series are available with either 1/125 or 1/10 microstep as well as full and half step. An innovative current control method assures smooth operation over a broad range, outperforming other drives on the market. And at lower cost.

For detailed product specifications and to arrange for an engineering test sample, write to The Superior Electric Company, 383 Middle Street, Bristol, CT 06010. For immediate action, call 203/582-9561.

CIRCLE NO 150

Superior Electric

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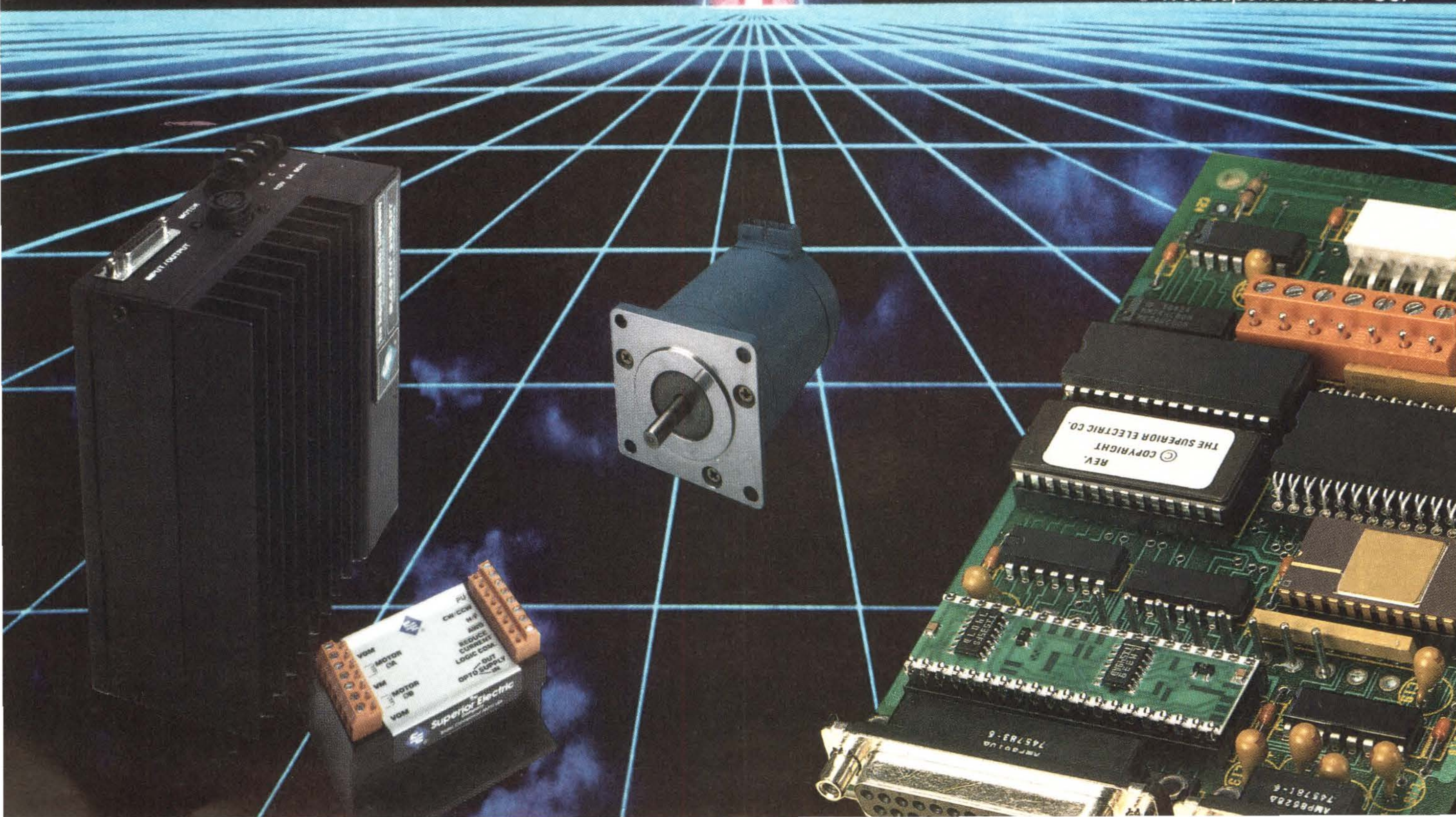

25 levels deep. The software checks all the diagrams against each other and against the data dictionary for consistency; it then reports undefined or inconsistent processes or data-item names. You can use the PC as an independent structured-design workstation. For more extensive design aids, you can link the PC to a VAX host that runs the vendor's structured-analysis real-time tools, structured-design tools, and language-development tools. To run the software, you'll need an IBM PC/XT, PC/AT, or compatible machine, equipped with 512k bytes of memory, 1.3M bytes of disk space, and PC DOS version 3.1 or later. You can use the Hercules monochrome, the IBM EGA, or a compatible graphics adapter card, and an appropriate monochrome or color monitor. The package works with mice from Microsoft and Mouse Systems (Santa Clara, CA). $1950.

Tektronix Inc, CASE Div, Box 14752, Portland, OR 97214. Phone (800) 342-5548; in OR, (503) 629-1573.

Circle No 408

REAL-TIME 8086 OS

- *Multitasking OS interfaces with Unix*
- *For real-time applications*

MTOS-UX/86 is a multitasking, multiprocessor operating system for real-time, embedded systems based on the 8086 and other µPs. This OS can operate with as many as 16 processors that are connected to the bus in a tightly coupled, symmetrical fashion. You can dynamically create and delete tasks, mailboxes, semaphores, event flags, and memory-buffer pools; the operating system automatically balances the load among processors. A terminal-emulator module lets the system log onto a Unix host and invoke programs that run under Unix. You can also use the Unix host as a file server. The system assumes that application programs are written in C, and it issues requests for service by means of C function calls. This assumption simplifies the process of picking command parameters off the stack. The nucleus occupies only 16k bytes of memory. From $5000.

Industrial Programming Inc, 100 Jericho Quadrangle, Jericho, NY 11753. Phone (516) 938-6600. TLX 429808.

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MICROWAVE CAE LINK

- *Links schematic-capture and circuit-design programs*
- *Enhances tools used for microwave circuit design*

The DDSC/Super-Compact interface links Tektronix's DDSC (Designer's Database Schematic Capture) software with the vendor's microwave-circuit-design programs, Super-Compact and Auto-Art. The package includes a file-extraction tool that automatically creates a Super-Compact file from a DDSC schematic. DDSC lets you include, directly on the schematic, all the information that Super-Compact needs for analysis and optimization; DDSC then back-annotates the results of the optimization to the schematic so that you can easily track the design specifications and changes to them. The interface also provides access to the vendor's AutoArt layout program, so that you can use the same DDSC file both for schematic capture and for final layout. The interface package provides extensive on-line help and an on-line Super-Compact manual. Interface, $5000.

Compact Software, 483 McLean Blvd, Paterson, NJ 07504. Phone (201) 881-1200.

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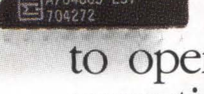

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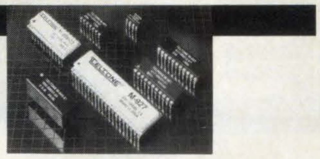

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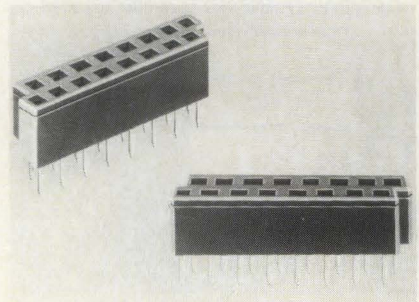

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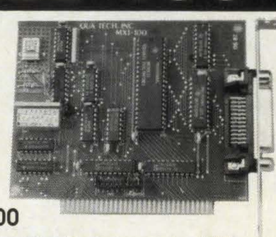

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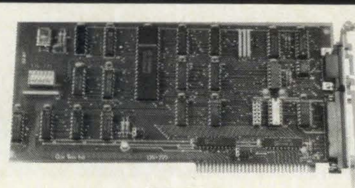

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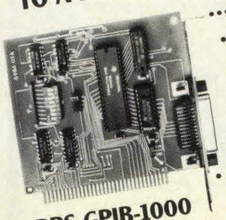

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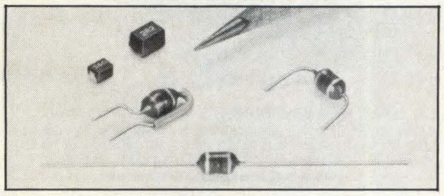

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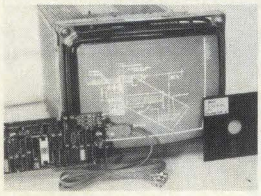

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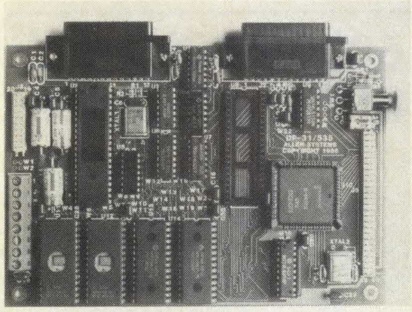

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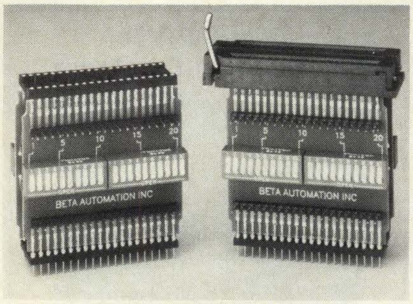

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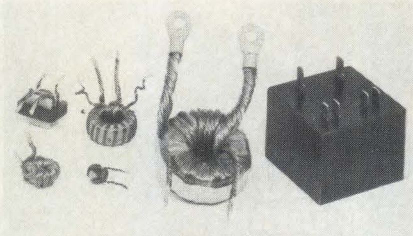

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To advertise in Product Mart, call Joanne Dorian, 212/576-8015

Catalog describes IEEE-488 interfaces

The 1987 catalog of *Interfaces for the IEEE-488 Bus* includes a listing of seven new PC products, which provide an interface between IEEE-488 instruments, plotters, and printers and IBM PCs or compatible computers. The publication describes how the manufacturer's Personal488 hardware/software combination makes programming IEEE instruments from the IBM PC easier.

IOtech Inc, 23400 Aurora Rd, Cleveland, OH 44146.

Circle No 411

Publication discusses specs for analog ICs

The *Elantec 1987 High Performance Analog Data Book* presents complete technical specifications for the company's high-speed analog ICs. The book is organized into six chapters of data sheets; selection guides precede each chapter. Additional chapters provide information about the manufacturer's reliability and quality-assurance programs, and its monolithic and hybrid military IC processing programs. Package outlines are also included. Request the book on company letterhead.

Elantec Inc, Marketing Communications, 1996 Tarob Ct, Milpitas, CA 95053.

INQUIRE DIRECT

Source- and date-code numbers listed

The *1987 Source Code and Date Code Booklet* contains an alphabetical and numerical listing of code numbers that are affixed to electronic products to identify the source or the vendor. The engineering department of the Electronic Industries Association assigns and registers these numerical symbols. Free to EIA members; $1 for nonmembers.

Electronic Industries Association, 2001 Eye St NW, Washington, DC 20006.

INQUIRE DIRECT

Guide details MS-DOS 3.2

The *MS-DOS Version 3.2 Pocket Command Summary*, a 10-pg document, updates the original MS-DOS reference (which covered Versions 2 and 3) and includes all the new commands in MS-DOS Version 3.2. This alphabetical listing details command syntax, simplifies the search for the correct command within the DOS environment, and describes the options available for each command. $3.

Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155.

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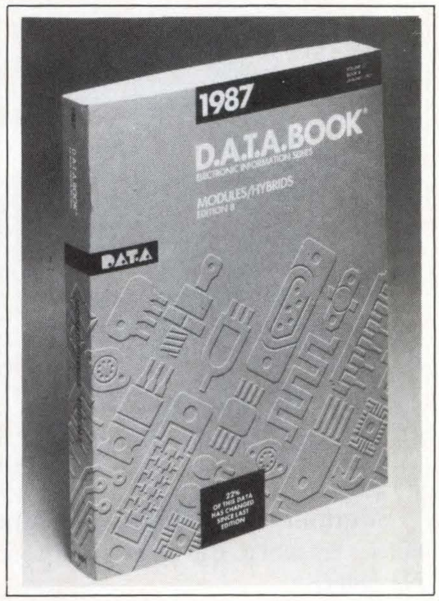
Software directory

This year's edition of the *Business Software Catalog* lists 1390 business application programs divided into 558 classifications. The programs run on hardware from such companies as IBM, DEC, Honeywell, and NCR. The catalog lists packages offered by 300 publishers in 10 countries: Australia, Belgium, Canada, France, New Zealand, Singapore, South Africa, UK, US, and Switzerland. The book includes a list of 206 consultants, which is cross-referenced for ease of use. $39.95.

IDBMA Inc, 9740 Appaloosa Rd, Suite 104, San Diego, CA 92131.

INQUIRE DIRECT



Specs on ICs

The eighth edition of *Modules/Hybrids* provides device specifications on more than 11,500 linear and digital hybrid ICs and modules from 84 manufacturers worldwide. This edition covers nearly 1000 new parts and contains updated information on another 500. In addition, it refers many new sources for these off-the-shelf hybrid ICs and modules. Sample products include wideband amplifiers, synchro-to-digital and digital-to-synchro converters, operational amplifiers, A/D and D/A converters, active filters, oscillators, and overvoltage-protection devices. Logic/circuit drawings and outline drawings complete the treatment. $95.

DATA Inc, Box 26875, San Diego, CA 92126.

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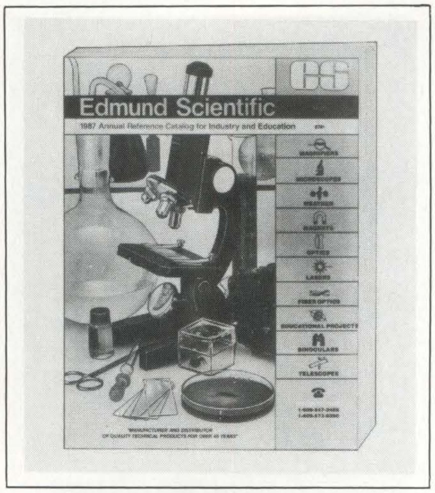
Catalog lists optical and industrial products

This 4-color, 148-pg catalog features more than 5000 of the vendor's optical and industrial products. It includes a comprehensive section, addressing precision lenses, optics, mirrors, prisms, fiber optics, optical instruments, and lasers, as well as a section on magnifiers, magnets, microscopes, telescopes, and accessories.

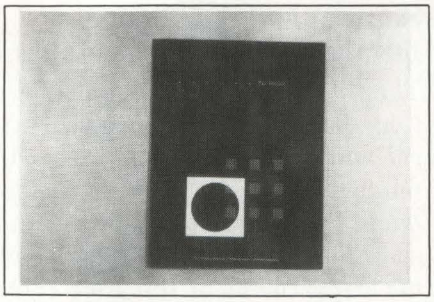


Edmund Scientific Co, Dept 5554, Edscorp Bldg, Barrington, NJ 08007.

Circle No 417

Brochure discusses product for memory-repair systems

This brochure describes the Verifier, a product that measures the positioning and alignment accuracy of



memory-repair systems. The 4-pg pamphlet lists what the package includes and presents three figures.

Teradyne Inc, Inquiry Systems and Analysis, 25 Drydock Ave, Boston, MA 02210.

Circle No 418

App note covers test system

This application note describes the automatic parameter test (APT) system for the Model 2955 radiocommunications test set. It also discusses the system's design, software, and typical operation displays. It includes illustrations of

screen displays.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401.

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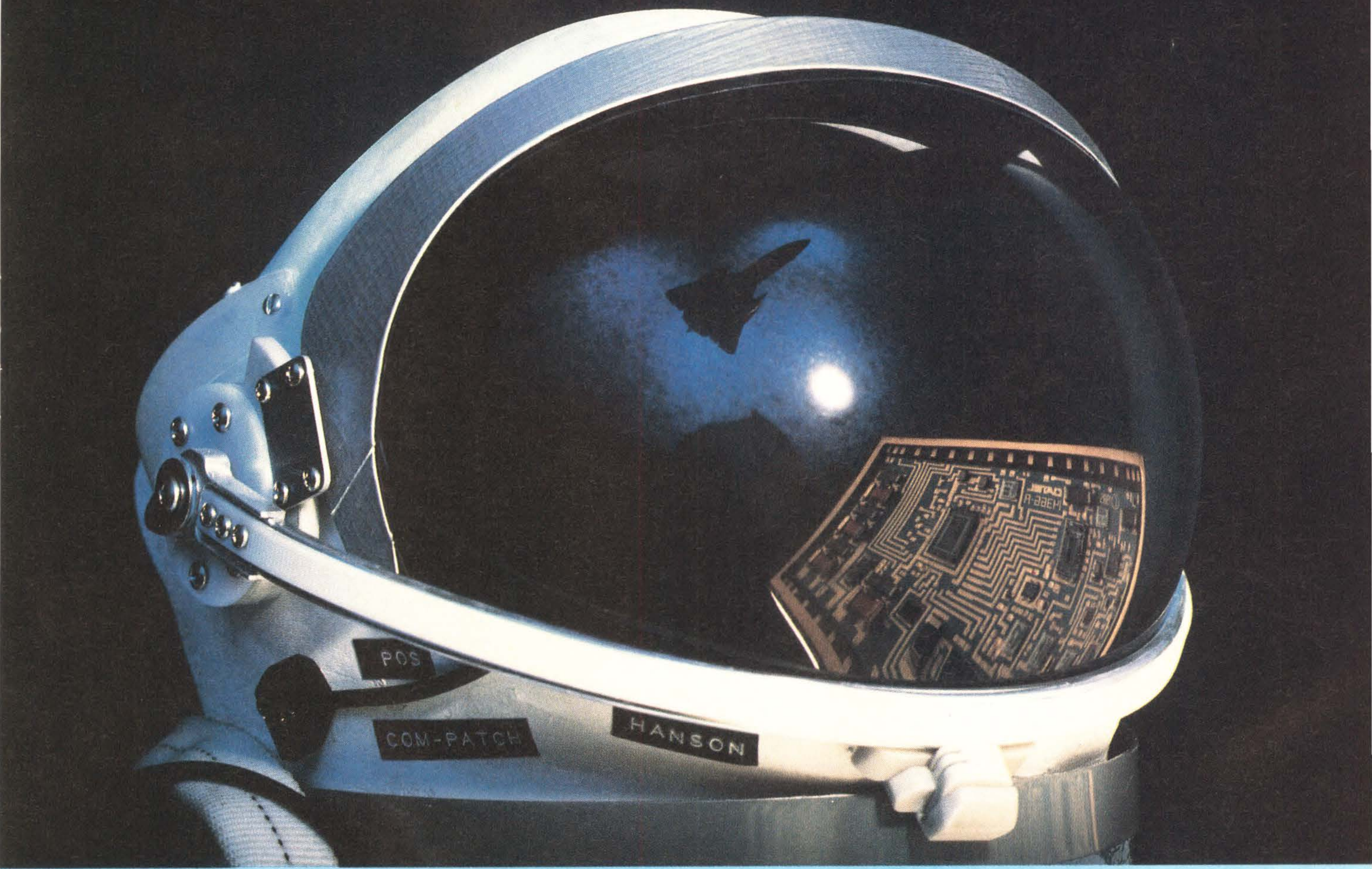
You need speed plus precision to push the limits.



Datel's 500nSec 12-bit A/D converter.

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CIRCLE NO 99

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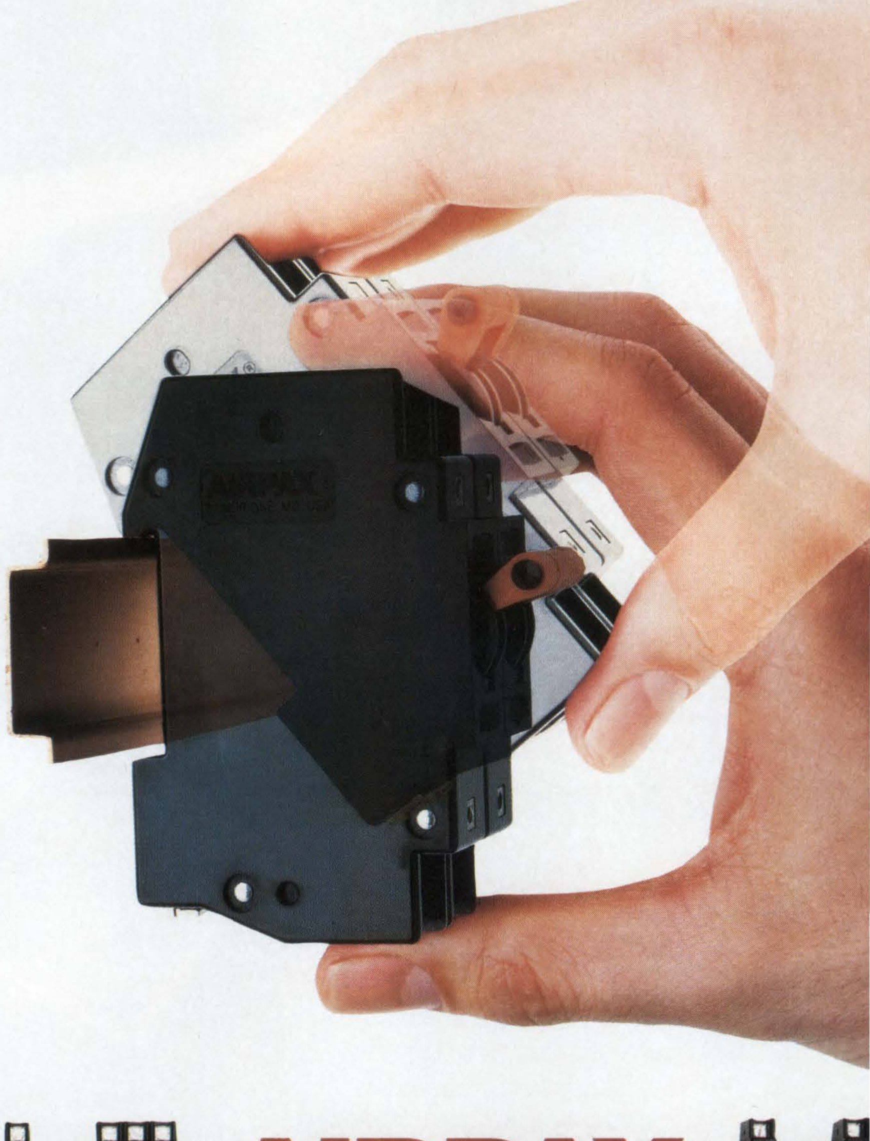

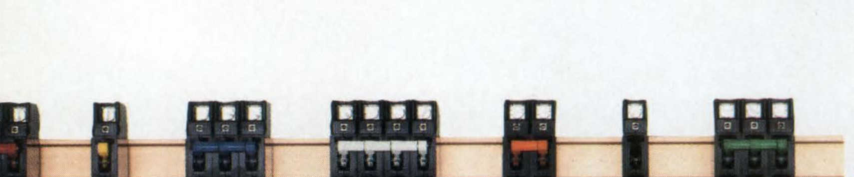

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CAMBRIDGE DIVISION

Widespread practice of unpaid overtime levies burden on salaried engineers

Deborah Asbrand, *Associate Editor*

If you work more than a few hours of overtime each week, you're far from alone. If you aren't paid for the overtime you work, you have nearly as much company. And if you feel that turning away from such overtime demands would incur unfair challenges to your professionalism and risks to your career, you are probably, once again, part of a large community of engineers.

Seventy-six percent of the respondents to the IEEE's 1985 Salary and Fringe Benefit Survey claimed to work some amount of overtime each week. One third said they worked seven or more hours of overtime each week. Sixty-eight percent of the respondents to the IEEE survey reported they receive no compensation for the extra hours they work.

Overtime appears to be a pervasive, if unpleasant, aspect of the workplace. And apart from government contractors and the handful of companies that have engineering unions, few companies extend overtime compensation to their engineers. The opinion that unpaid overtime is the curse of salaried professionals appears to be widespread. Yet the practice goes on at the level of the unwritten rule, the unspoken code. And even professional associations and related organizations have done or said very little about the issue. (In fact, the practice is such a commonplace feature of the corporate landscape that one director of engineering at Analog Devices assumed his company had no overtime provisions, only to discover upon thumbing through his employee handbook that there was an allowance for paid overtime. He said that he had never seen the policy used.)

As noted, engineers in some electronics-industry sectors do receive overtime pay. Government contracts, for example, often compensate engineers who work the overtime that has been scheduled for a project. Legislators have limited paid overtime on government projects in some cases, though, since it was revealed that several large contractors were overcharging the federal government for contract costs.

Members of engineering unions also are paid for any extra hours they work at their employers' request. Members of the Seattle Professional Engineering Employees Association receive their regular hourly pay plus five dollars for each hour of overtime they work at the request of their employer, Boeing Corp. At the Camden and Moorestown, NJ, facilities of RCA, the 2000 engineers that constitute the Association of Scientists and Professional Engineering Personnel earn straight time plus four dollars per hour for scheduled overtime.

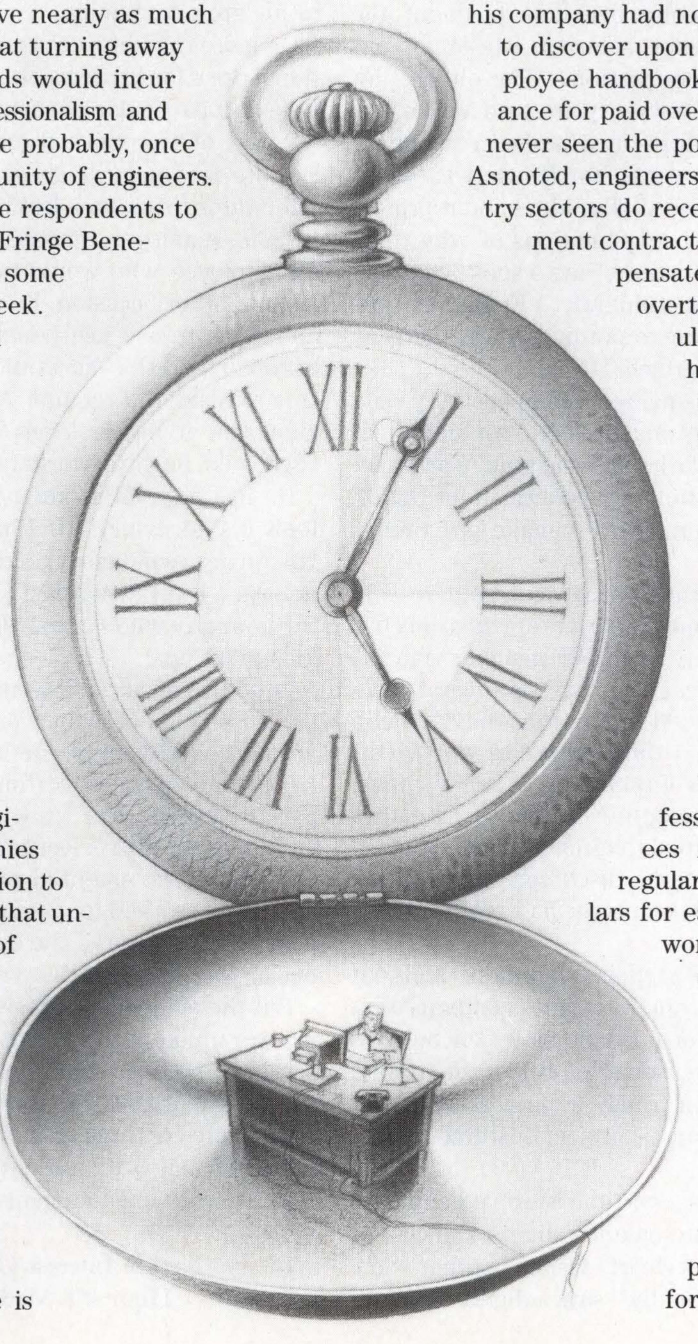

Illustration by Michael Young

Beyond the spheres of government contracts and unions, however, industry watchers report that unpaid overtime is a tacit fact of the workplace. "Most of the major electronics organizations don't pay overtime to engineers," says Susan Reynolds, a principal partner with the benefits consulting concern Sibson and Company in Princeton, NJ.

Company representatives cite a variety of reasons to explain why they don't pay engineers for any extra time they put into a project. The most common response is that engineers' salaries reflect the overtime they often must work. "We don't pay overtime to engineers, but we feel we have a very generous salary and compensation plan," said a spokesman for Cullinet Software (Westwood, MA).

In other cases, company representatives refer to federal fair-labor laws, which specify overtime payment for hourly workers, but exempt salaried workers from requirements for such compensation. "The philosophy is that those in the exempt category are paid a salary to perform certain responsibilities in whatever reasonable time it takes," said a spokesman for Hewlett-Packard. Other representatives echoed similar ideas about professional responsibility in their explanations of why their company did not pay for overtime. Says a spokesman for Massachusetts-based Data General: "Engineers are project-driven. They're going to put in as many hours as required to complete the project."

A few employers do offer engineers compensatory time off after working long hours on a project. "An individual manager quite often may work out some kind of arrangement with an employee," offered a spokesman for Digital Equipment Corp. "There's an effort to make sure there's some kind of fairness."

Yet engineers working in the intensely competitive electronics industry say that some employers are anything but fair in their overtime policies. One IEEE member who has held a number of local offices says that, on several occasions, members have confided to him that they've been told by their employers that their failure to work overtime could result in the loss of their jobs. In one instance, he remembers receiving a telephone call from a member who would be unable to attend that night's local meeting, during which the subject to be discussed was working conditions. The reason? His employer had required that he work late.

Some engineers believe that their exemption—and that of other professionals—from overtime compensation according to the dictates of fair-labor laws encourages companies to draw up unreasonable project timetables. If employers were required to pay engineers overtime, one engineer says, more realistic project deadlines would soon appear.

Although most engineers' overtime is unpaid and thus doesn't appear on corporate balance sheets, the cost of long stretches of overtime is clearly visible in other ways. "Morale goes down very rapidly," says a digital designer in Phoenix, AZ. In addition to morale problems, long hours on the job can lead to fatigue and costly errors. For example, along with its other findings, the presidential commission investigating last year's explosion of the Challenger shuttle criticized the National Aeronautics and Space Administration for shuttle workers' frequently long hours on the job.

In order to avoid the high personal costs of overtime—which include long periods of time away from family and home—one engineer relates that he has on many occasions refused to work overtime and chosen to incur the professional costs. The 33-year-old digital designer says that his decision not to work overtime was not at any time a sign of disloyalty or irresponsibility, but was made to balance his professional obligations with his responsibility to his growing family.

On more than one occasion he has paid a steep professional price for his decision. After declining to work overtime on a particular project, he still managed to complete his part of the work three weeks ahead of schedule. Despite this performance, he was transferred shortly afterwards to another, less interesting project—a message from his employers, he says, that they would not tolerate an employee who would not follow orders.

On another occasion, he explained to his boss that he and his wife had just bought a house that was in need of repair, and that he would need to keep his weekends free to make the repairs. Although his boss understood, managers at higher levels offered less sympathy: They suggested he hire workers to do the repairs.

He has no qualms about working overtime when he feels it's necessary. "If I have to come in early or stay late on my own, I get a good feeling of accomplishment," he says. "But I'm married to my family, not my job. I pity the poor guy who's married to his job. I like watching my kids grow up."

Benefits consultant Susan Reynolds says that overtime is an issue about which engineers are becoming more vocal. A handful of research and development companies have changed their overtime policies, she says, in anticipation of engineers' growing frustrations. ITT, Bechtel Corp, and the Microelectronics and Computer Technology Corp have implemented programs to reward engineers who have worked long hours. In most cases, the reward comes in the form of the opportunity to work on a project of the individual's own choosing.

But the evidence suggests that the majority of employers are unlikely to change their policies soon. Private-sector companies find safe harbor from overtime pay in the fair-labor laws. Companies that do pay overtime will most likely continue to do so, as the high costs of benefits packages makes it more attractive for them to pay overtime than to expand their staffs. **EDN**

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Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
May 28	May 7	Computer Peripherals; Software; Power Sources/Devices	Closing: Apr. 30 Mailing: May 21
June 11	May 21	Math ICs; CAE; Computers	Closing: May 14 Mailing: June 4
June 25	June 4	ASIC (Semicustom ICs) Directory; Analog ICs; Surface-Mount Technology	Closing: May 28 Mailing: June 18
July 9	June 18	Product Showcase-Volume 1; ICs & Semiconductors; Software	
July 23	July 2	Product Showcase-Volume II; Computers & Peripherals; Test & Measurement Instruments	Closing: June 25 Mailing: July 16
Aug. 6	July 16	Computer Boards; Digital Signal Processing; Test & Measurement; Top Ten Reader Vote Contest	Closing: July 9 Mailing: July 30
Aug. 20	July 30	Military Electronics Special Issue; Fiberoptics; Software	Closing: July 23 Mailing: Aug. 13
Sept. 3	Aug. 13	Analog ICs; CAE; ASICs	Closing: Aug. 6 Mailing: Aug. 27
Sept. 17	Aug. 27	Memory Technology; Communications Technology; Software	Closing: Aug. 20 Mailing: Sept. 10
Oct. 1	Sept. 10	Surface-Mount Technology; Computers & Peripherals; Industrial Product Showcase	Closing: Sept. 3 Mailing: Sept. 24
Oct. 15	Sept. 24	Test & Measurement Special Issue; Analog ICs; ASICs	Closing: Sept. 17 Mailing: Oct. 8
Oct. 29	Oct. 8	Computers & Peripherals; ICs & Semiconductors; Wescon '87 Product Preview	Closing: Oct. 1 Mailing: Oct. 22
Nov. 12	Oct. 22	Wescon '87 Show Issue; ICs; Computers & Peripherals	Closing: Oct. 15 Mailing: Nov. 5
Nov. 26	Nov. 5	Microprocessor Technology Report & Directory; Analog ICs; Sensors & Transducers	Closing: Oct. 29 Mailing: Nov. 19
Dec. 10	Nov. 19	Product Showcase-Volume I; ICs and Semiconductors; Software	Closing: Nov. 12 Mailing: Dec. 3
Dec. 24	Dec. 3	Product Showcase-Volume II; Computers & Peripherals; Test & Measurement Instruments	Closing: Nov. 26 Mailing: Dec. 17

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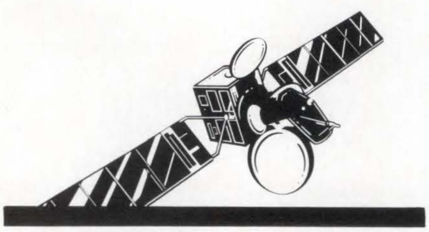

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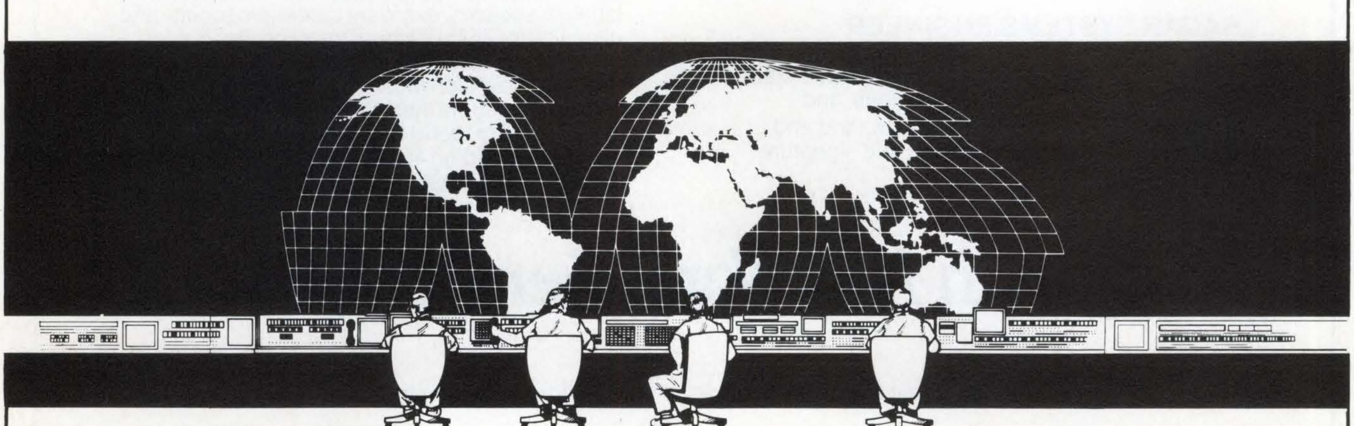

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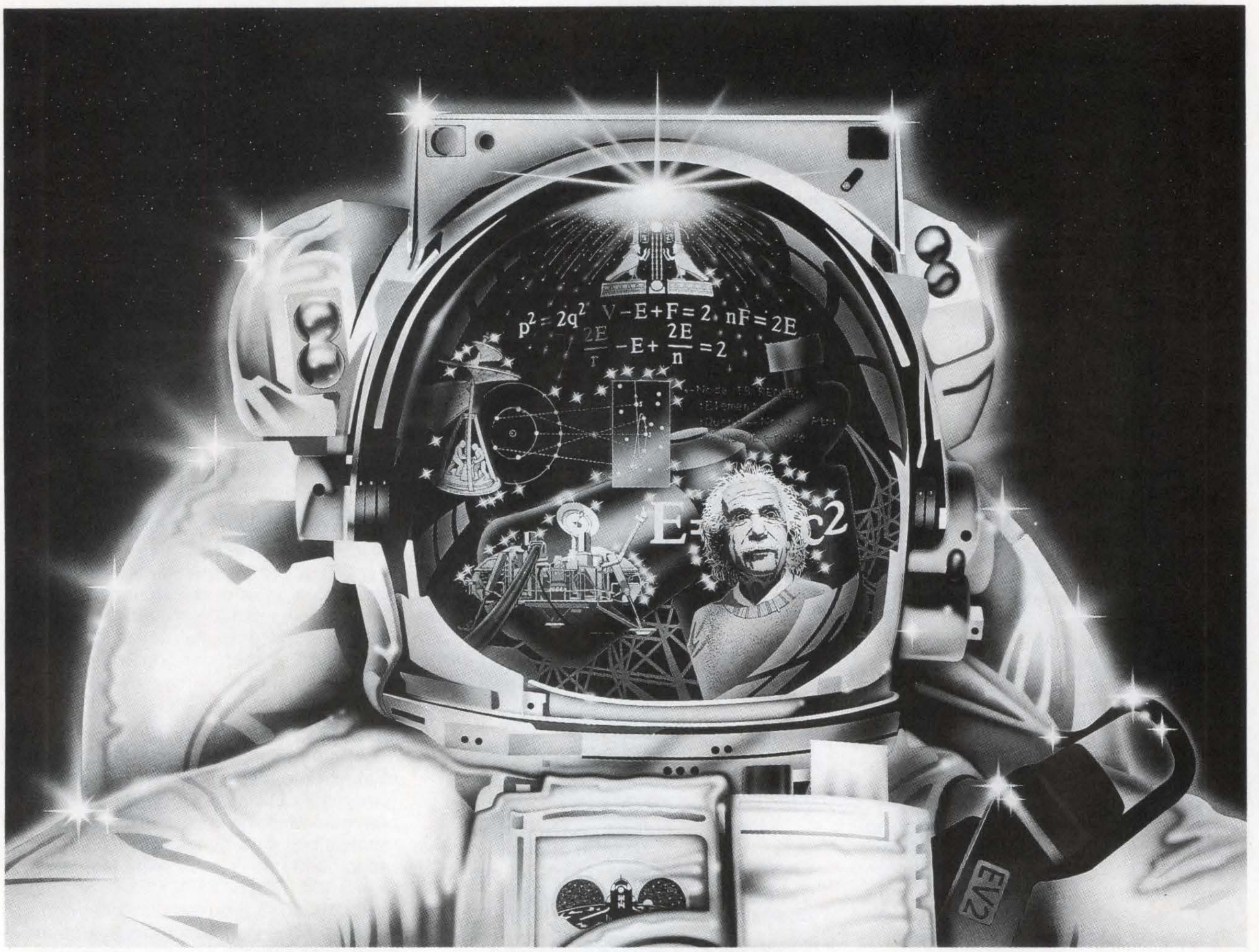

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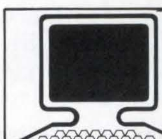

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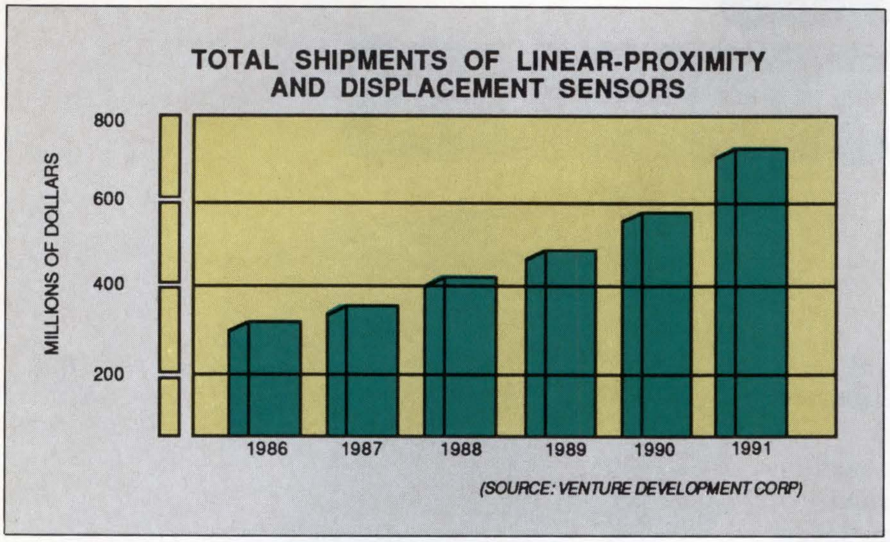

Market for linear-proximity, displacement sensors to grow

The aggregate of shipments of linear-proximity and displacement sensors will grow at a 16.1% average annual rate over the period 1986 to 1991, according to the market-research company Venture Development Corp (Natick, MA). Through that period the dollar value of the combined market will grow from $328 million to $691.6 million. Sensor types in this market segment include photoelectric, inductive, capacitive, ultrasonic, and other types of linear-proximity sensors as well as linear variable differential transformers (LVDTs), linear potentiometers, linear encoders, and other types of displacement sensors.

VDC notes several general trends that characterize the current market. Factory-automation companies have entered the proximity-sensor market as part of their attempts to provide comprehensive automation systems and services. Proximity-sensor manufacturers are introducing "an almost endless stream" of new product lines in various technologies, in order to provide solutions to the full range of proximity-sensing problems. Even manufacturers of electromechanical switches are adding proximity sensors to their product lines, in order to protect their customer bases. Meanwhile, foreign suppliers continue to enter the US proximity-sensor and linear-encoder markets. Foreign invasion of the US LVDT market is likely to expand as well.

In the proximity-sensor market segment, ultrasonic sensors are expected to show above-average annual growth in shipments through the specified 5-year period. Recent improvements in the design of these devices include temperature compensation and increased gain in the electronic circuitry and encapsulation. Inductive sensors will also show above-average annual growth in sales over the forecast period. On the other hand, photoelectric sensors—the largest proximity-sensor market segment—will show healthy annual sales growth but will not outpace the market. Growth in demand for capacitive sensors will also be less than the 16.1% annual rate.

Sales of linear-displacement sensors will increase at even faster rates than sales of proximity sensors. The military and aerospace industry will be a driving force in the demand for LVDTs, which accounted for more than half of the revenues generated by linear-displacement sensors. Some of the anticipated growth in LVDT sales will come at the expense of linear-potentiometer sales, says VDC. And despite expectations of steady growth, linear encoders will not make the gains in popularity that other types of linear-displacement sensors will see.

"Moderate" growth forecast for semiconductors in 1987

The consumption of semiconductor chips in North America will total $11.5 billion in 1987, says the market-research company Dataquest (San Jose, CA). This figure marks a 12.7% increase over the 1986 market —a growth rate Dataquest characterizes as "moderate," in spite of the fact that it's approximately twice the 6.5% increase of the 1986 market over 1985 sales.

The predicted growth appears moderate in comparison with the boom years, 1983 and 1984, when growth rates reached a peak of 44%. More and more individuals and companies involved in the semiconductor industry are starting to regard those years as the exception rather than the norm, and Dataquest analysts urge vendors to prepare for steadier growth: "The challenge for the North American semiconductor industry is to learn to cope with moderate growth in consumption. Industry participants continue consolidating and restructuring to deal with the reality of lower long-term growth rates." Still, Dataquest does not rule out growth exceeding 20% in 1988.

Two principal factors are moderating the current fortunes of the semiconductor industry, says Dataquest. One is modest growth in sales of equipment having semiconductors; such equipment includes computers, communications equipment, industrial equipment, military hardware, consumer electronic products, and automobiles. The other factor is a shift in purchasing patterns on the part of semiconductor procurement managers, from the US to the Pacific Basin.

Making the Connection Between...

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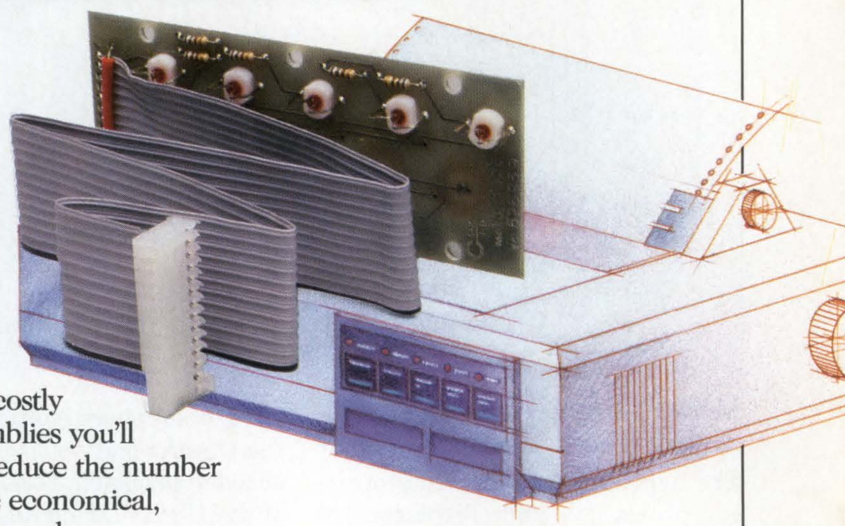

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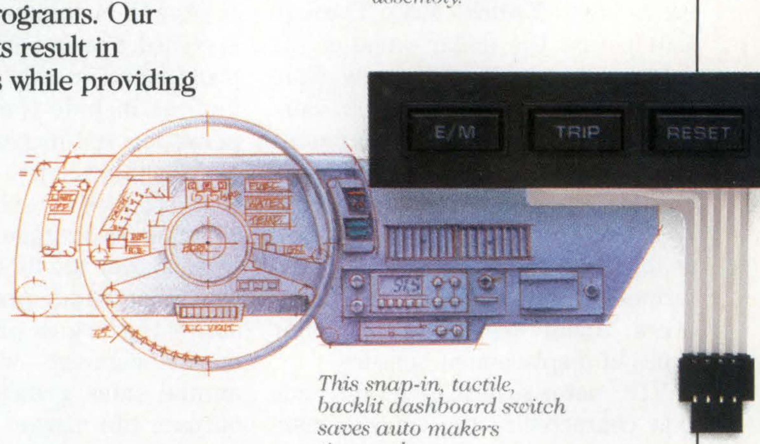

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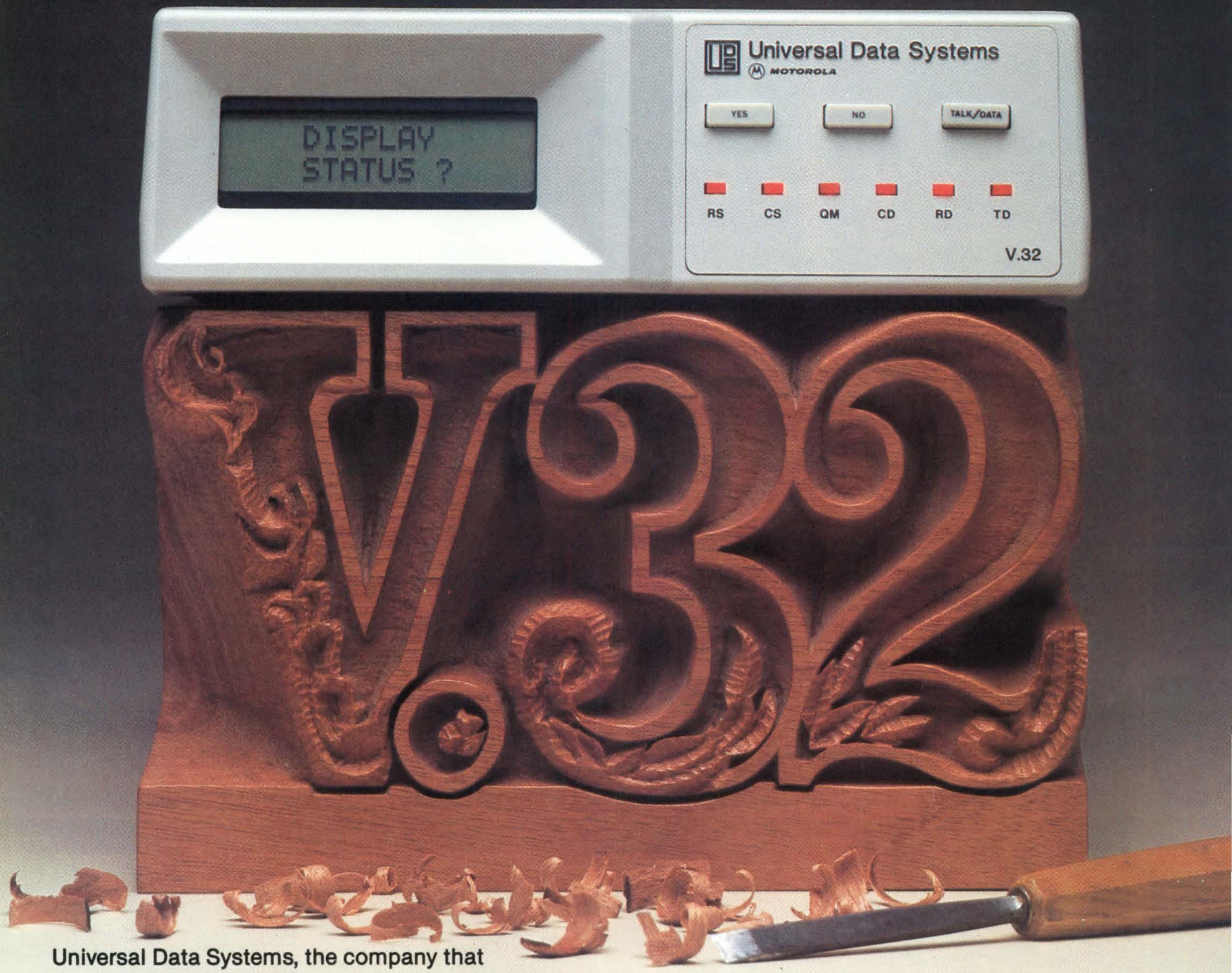

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