A MORGAN-GRAMPIAN PUBLICATION

DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS DECEMBER 1984

- VME BUS ATTACKS INDUSTRIAL AUTOMATION MARKET
- CPU ARCHITECTURE PART II: DATAFLOW COMPUTERS ENCROACH ON VON NEUMANN TERRITORY
- THE 1984 SALARY SURVEY: HOW DO YOU STACK UP?
- ARRAY PROCESSORS
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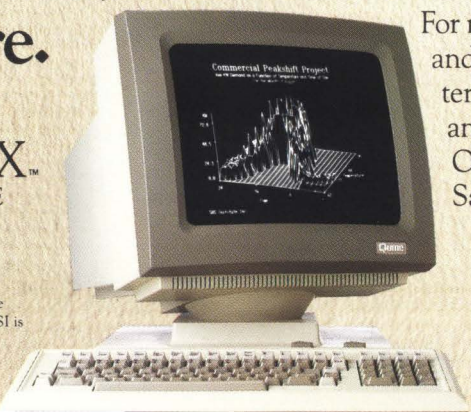

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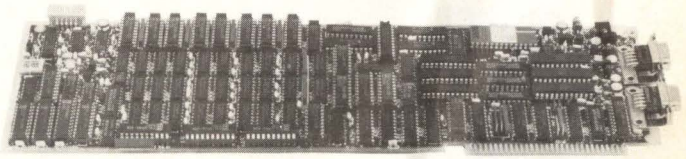

See how easy it is to make your computer see like a hawk. Call or write Datacube Incorporated, 4 Dearborn Road, Peabody, MA 01960, Telephone: (617) 535-6644.

Datacube

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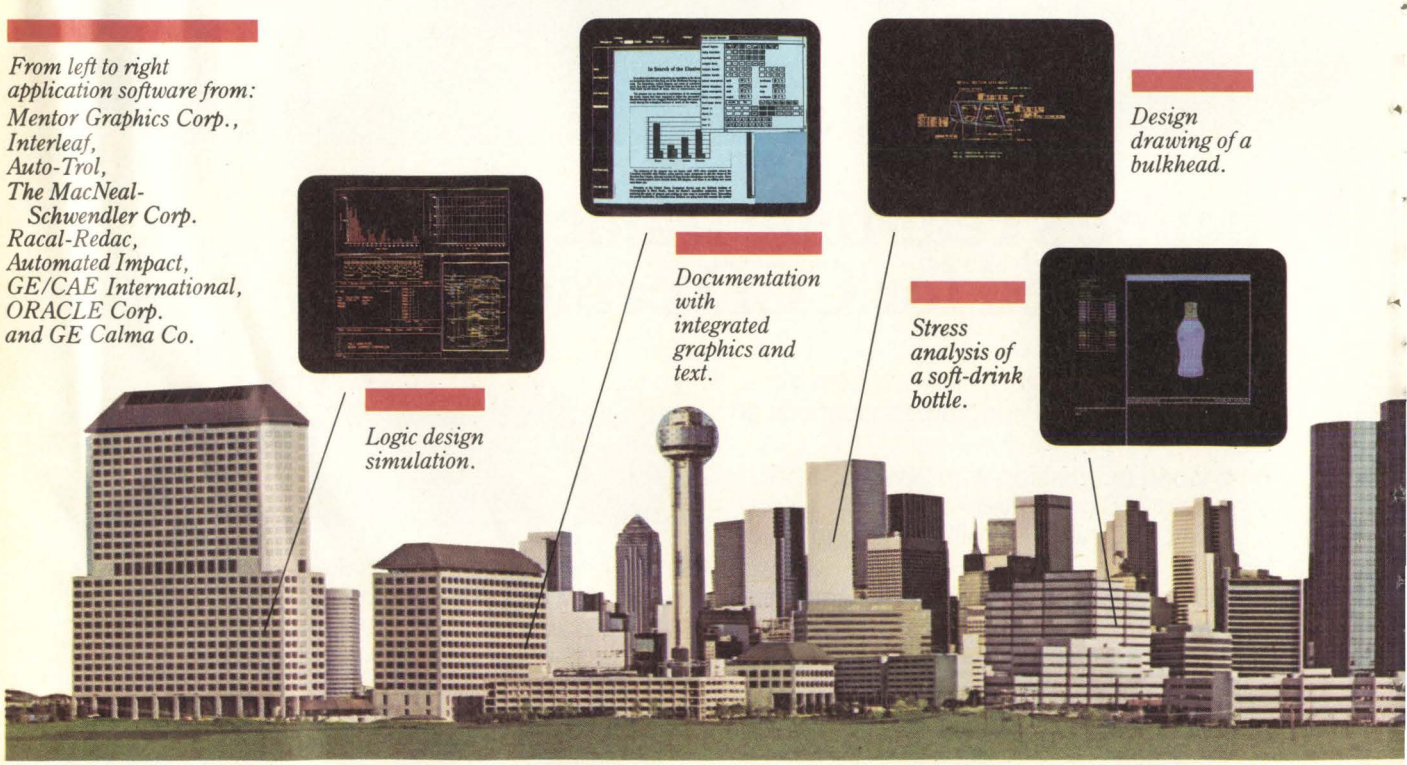

From left to right application software from: Mentor Graphics Corp., Interleaf, Auto-Trol, The MacNeal-Schwendler Corp. Racal-Redac, Automated Impact, GE/CAE International, ORACLE Corp. and GE Calma Co.

Logic design simulation.

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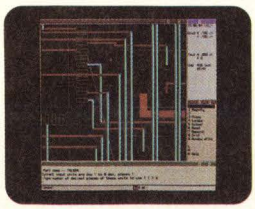
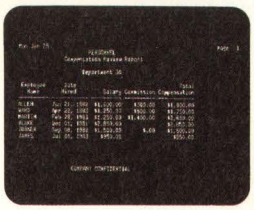
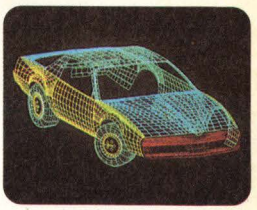


Printed circuit board layout.

Exploded solid model of an automobile.

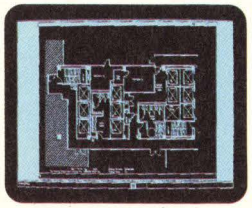


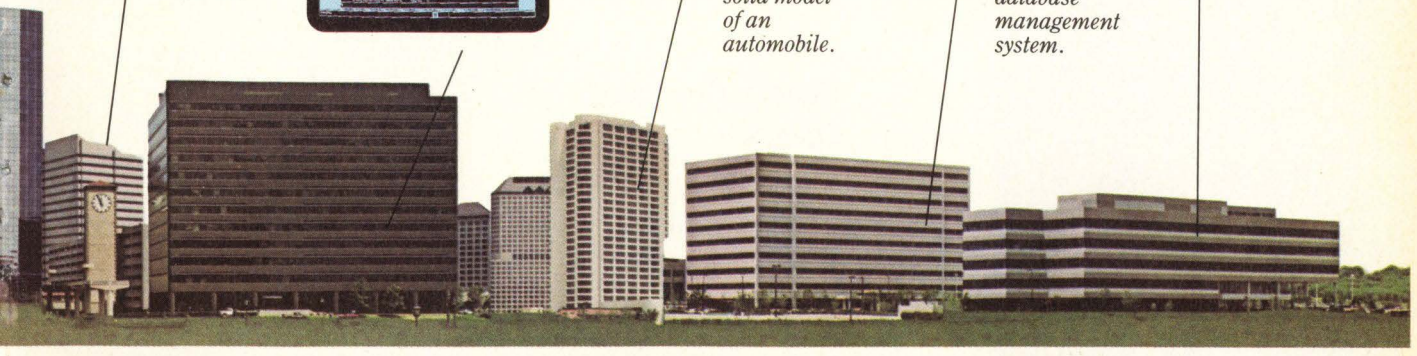
Relational database management system.



3D surface model.

Space plan of a facility.





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COURTESY DIGITAL EQUIPMENT CORP.

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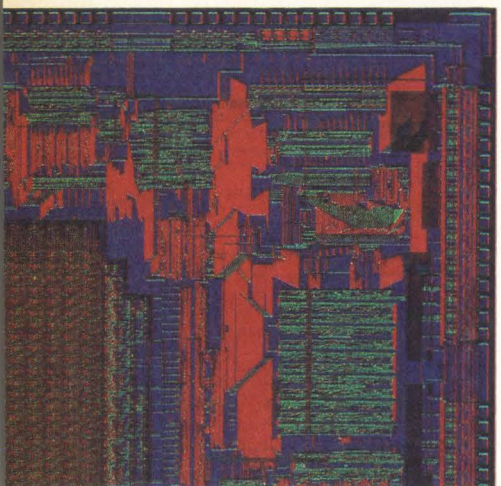

COURTESY ADVANCED MICRO DEVICES

61 ICs enhance array processors

DEPARTMENTS

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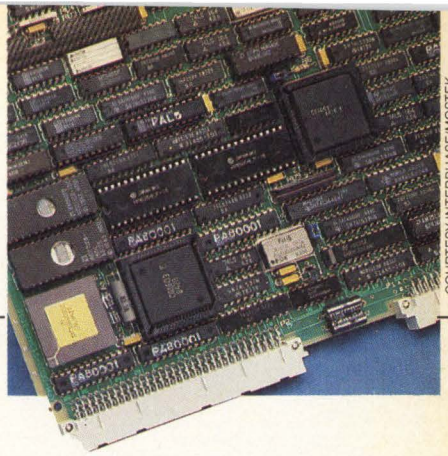
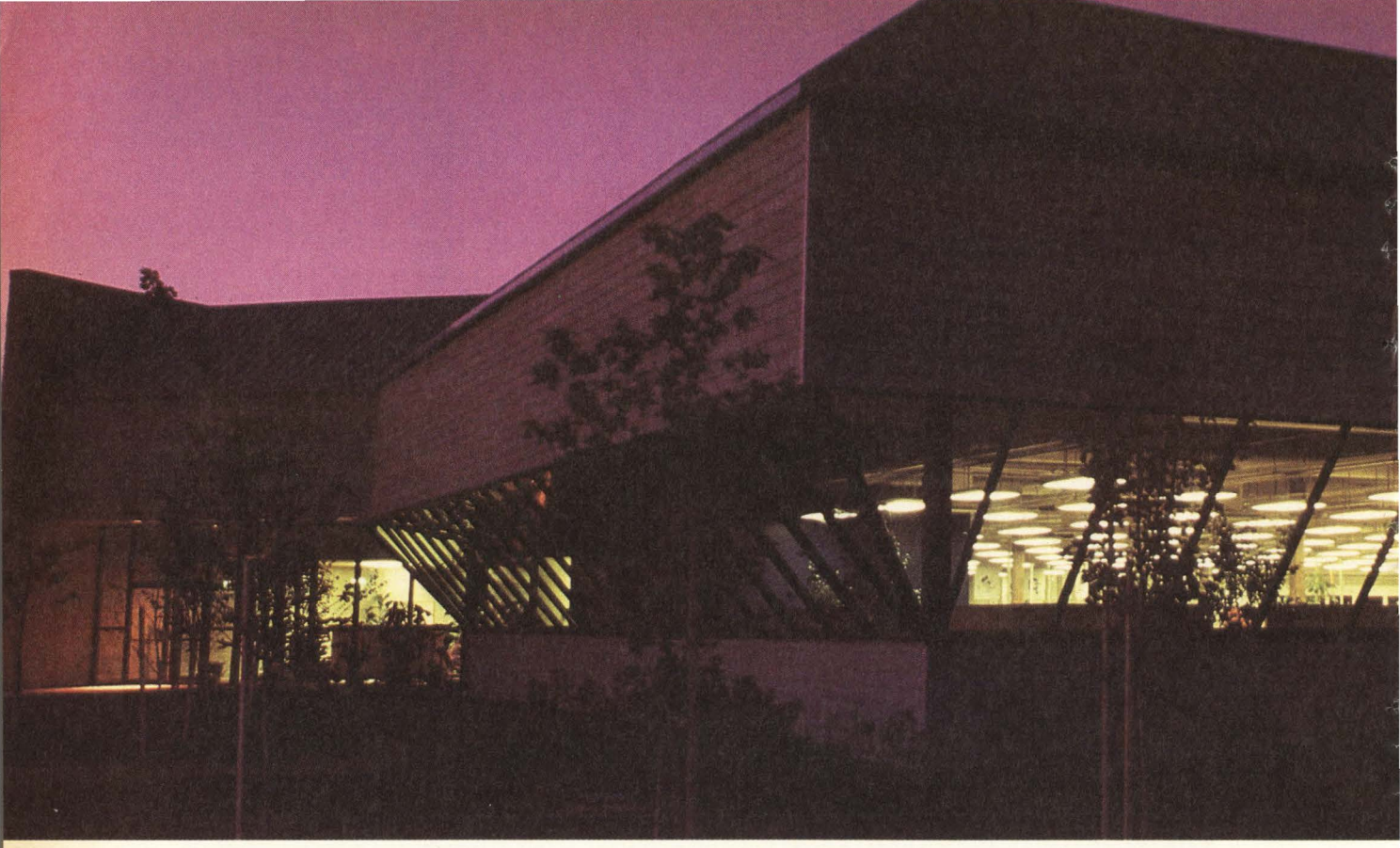


COURTESY INTERPHASE/MOSTEK

FEATURES

ON THE COVER

The SYS68K/GDC-1 is a VME bus compatible high-resolution graphics system for raster scan monitors, designed and manufactured by Force Computers, Inc. It allows VME bus computers to generate and display mixed graphics and alphanumerics on a standard monochrome or RGB color monitor. The subsystem consists of one GDC-1M master board (shown on the cover) and one GDC-1S slave board communicating via a local extension bus that can be expanded by one or two additional GDC-1S slave boards for additional capabilities. Photo courtesy Force Computers, Inc.



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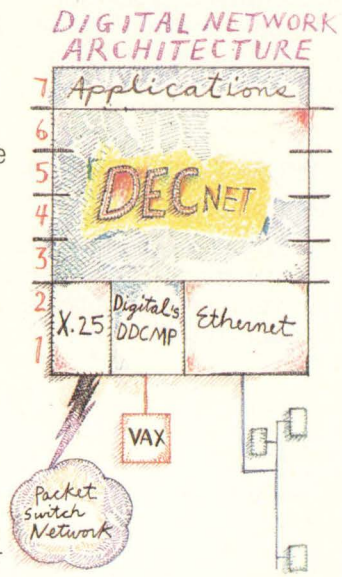

You can communicate with mainframe systems. You can match the technology to the job. And, most importantly, you can keep pace with your customers' distributed processing needs as they develop.

DECnet™ software lets you link Digital's systems in both local and wide area configurations. It supports high-speed local area network communications using Ethernet. And it provides gateways to allow Digital's computers to communicate with other vendors' systems over private lines or packet switched X.25 networks. This means you can tailor your products to fit in with your customers' current and future networks.

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The benefits you and your customers get by incorporating Digital's networking capabilities are virtually unlimited.

First of all, your systems can incorporate recognized industry standards. Such as Ethernet (IEEE 802.3 specification), X.25, and others.

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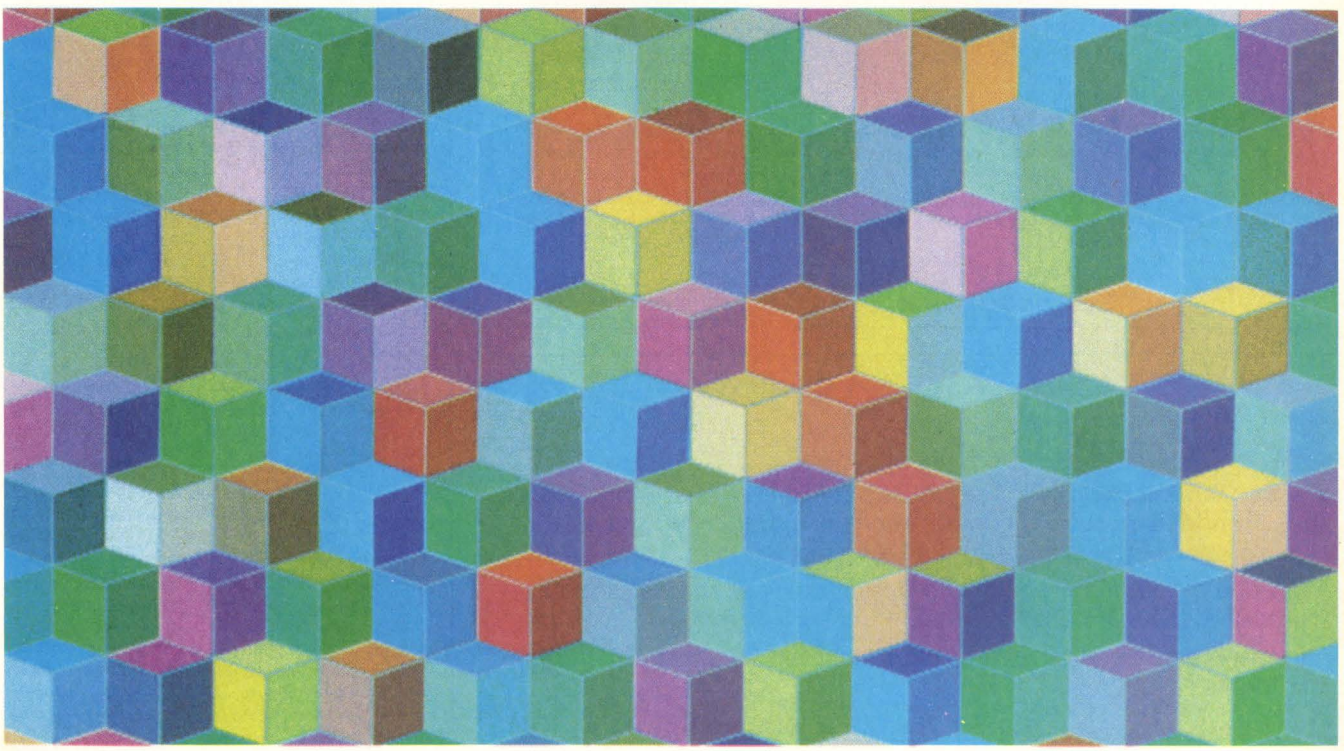

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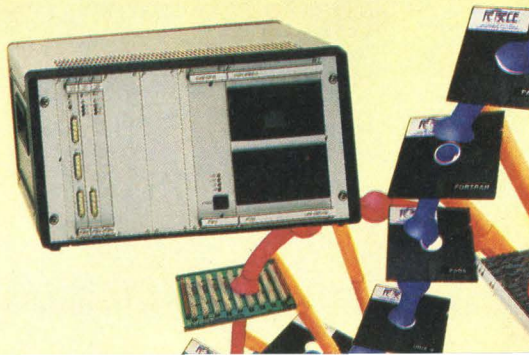

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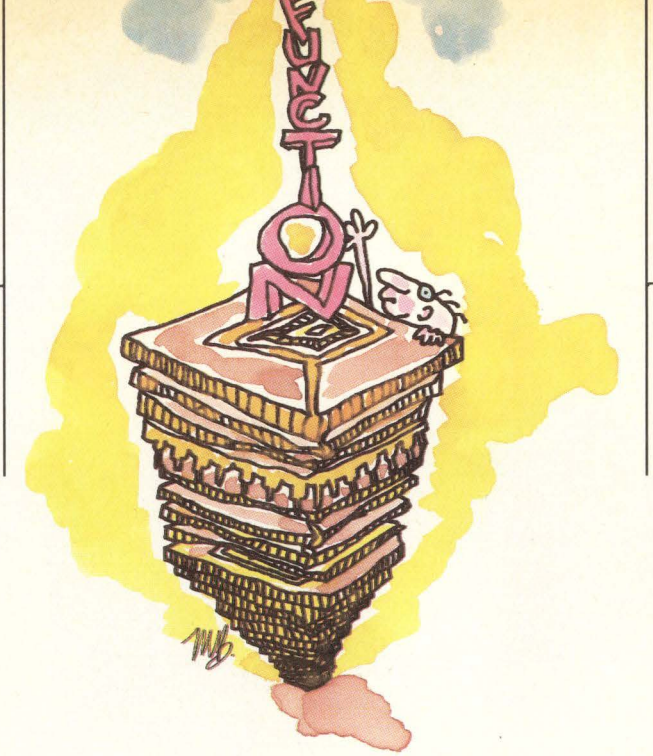
"The systems architect must evaluate a vendor's viability as well as his product line."

EDITOR'S COMMENT



Over the past few years, it has become evident that the increasing density of VLSI circuits will provide a more cost-effective solution for design engineers building the next generation of computer systems. The simple fact that such functionality can be placed on a single device must lead the reader to question who will be responsible for determining the functions that will be placed onto that device.

Already several parts have been marketed that were obviously fine conceptual ideas. These parts found wide industry appeal but many engineers used only a small part of the devices' total capability. Clearly, this trend is likely to continue. In part, it will be fueled by the IC houses' need to sell products. Next generation devices developed by the IC houses working with their largest customers in the computer industry may appear to be universal in nature, but in fact may be tied closely to the particular architecture of the product goals of one or two large computer vendors.

Many of the large players fall into two categories: the original IC vendors (such as Intel) and the minicomputer houses (such as DEC). Many of these companies in the industry currently offer to OEMs products at three levels – IC, board and system.

In today's fast-paced competitive environment, is it possible for a single company to remain so diverse and successfully compete in all of these areas? Clearly, the exodus of AMD from the Multibus arena has left many companies with strong feelings that the board business may eventually be served by medium-sized, $20 million to $30 million-a-year companies and not by the large IC houses who perceive too much competition from garage start-ups and too small returns on investments.

Like the board business, the OEM systems offered by many companies whose backgrounds have been in the IC business have not been as popular as those from other vendors. The lesson to be learned is that those companies wishing to remain in all three OEM areas – IC, board and system – must have a strong understanding of how their architecture can be implemented at all levels. Clearly, the large minicomputer houses have a distinct advantage here. By porting a minicomputer architecture to the board and chip level, they can offer software-compatible solutions at all three levels, a distinct advantage to the designer. Because of their large sales volume, they also carry a lot of clout with the IC houses who may even establish internal support divisions to assist their large OEMs.

Undoubtedly, many new products will be touted next year as the universal panacea for many engineering problems. Ultimately, it will be the systems architect who will make the decision of how the circuit will be implemented to give his product the price and performance characteristics necessary to meet his market window. This analysis of a design involves a number of different factors. Both the advantages and disadvantages of several product lines may need to be examined. They must be compared and contrasted and weighted in light of both price and performance. However, evaluating products themselves forms only a part of the systems architect's problem. A more difficult task relates to evaluating the long term goals of the vendor's plans to support its products into the future. Clearly, a company that leaves its OEMs high and dry by pulling product lines out of the market is as destructive to its customer as one that cannot meet demands, or another that goes bankrupt.

In the past, many companies have been negligent in offering that sort of advice to their customer base. However, unless they begin to, it will only result in an eventual loss of credibility. Credibility is as important in the trade magazine business as anywhere else in the industry, particularly when a magazine is devoted to the issues of systems architecture, integration and applications. In many instances, the editors of this magazine and others in our trade, interface with many of the marketing personnel that you, our readers, do. Unfortunately, many of these people do not have the inclination to indicate to neither the press nor the engineering community the various tradeoffs of their product. Hence, our role as editors becomes similar to yours – it must involve the comparison of a number of different technologies and products in order to give a balanced perspective of the options that are available to the systems architect. This involvement is no mean task but the alternative is disappointing, if not misleading.

You will notice that over the past year a great number of articles published by *Digital Design* were written by our staff with the sole intent of revealing the options and alternatives involved in the industry. As a magazine, we understand that it is vital to recognize the needs of our readers and help with the challenges that you will face next year. Notwithstanding the increasing level of hype appearing in the media, our goal remains true – to deliver options, not opinions to you, the systems architect, and to help in any way we can.

David Wilson, Executive Editor

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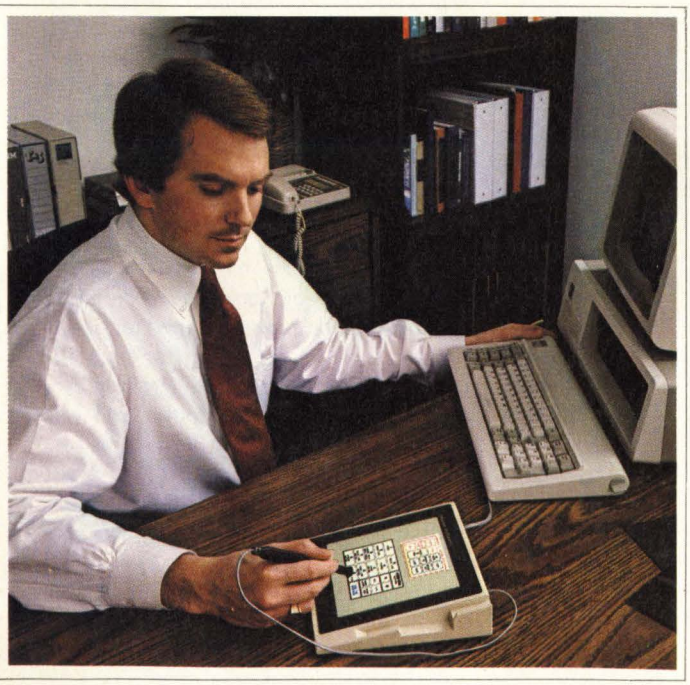
Houston Instrument's new PC Pad - the compact digitizer with "mouse-ability"

Houston Instrument has molded superior electronics into a handy 8" x 7" wedge-shaped tablet to give you a high-precision digitizer that also can be used as a mouse for cursor control.

By simply touching stylus to pad, you can drive the cursor to any point on your computer screen. So, with the **PC Pad** and appropriate software, you get the capabilities of a mouse and a digitizer in one small product...for one low price—$395.*



Features for Professionals

For systems builders, or for software authors who want to create a graphics package for an innovative product, the **PC Pad** is a perfect mix of convenient size and advanced capability.

With a **PC Pad**, you can convert minute details into data a computer can store. A **PC Pad** will address over one million individual points, allowing you to utilize sophisticated graphics monitors. No other digitizer its size has comparable resolution.

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The **PC Pad** is compatible with the same serial formats used with Houston Instrument's popular HIPAD ™ digitizers, and can be used with any computer which has an RS-232-C interface.

For more information about the compact, versatile **PC Pad**, contact **Houston Instrument**, P.O. Box 15720, Austin, Texas 78761 or call (512)835-0900. Outside Texas call 800-531-5205 for the name and location of your nearest representative. In Europe contact **Houston Instrument**, Belgium NV., Rochesterlaan 6, 8240 Gistel, Belgium. Tel. 059-27-74-45, TLX. 846-81399.

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Circle 15 on Reader Inquiry Card

4P015

UPDATE

Control Data Peripheral Phaseout

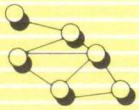
Control Data plans to phase out of the plug-compatible peripheral equipment business after completing production of its model 33800 disk memory subsystem. The decision was based on long-term considerations and was not occasioned by the current technical problems with its 33800. Control Data initially entered the plug-compatible peripheral equipment market to attain incremental manufacturing volume and economies of scale in its basic OEM peripheral equipment business.

Ridge, Silicon Graphics Marketing Agreement

Ridge Computers' 32-bit mainframe computer products will be offered in combination with Silicon Graphics' Iris products. The joint development and marketing of the systems are designed for applications such as finite element modeling and analysis which require both intensive computing and high performance graphics capabilities.

Ethernet LANs Supplied To Sanders

Interlan, Inc. will supply and install components of its net-plus Ethernet-compatible local area networking system in four Sanders Associates facilities in the Nashua, NH area. A component in these networks is Interlan's NTS10 terminal server, which acts as a 'data pbx' for any mix of up to eight asynchronous RS-232-C devices connected to it.



Industrial LAN Company Formed

Ungermann-Bass, Inc., and General Electric are considering forming an independent joint venture company to develop, manufacture and market LAN communications systems for the industrial market. The goal of the new company is to become the supplier of communications products that will interconnect all industrial automation equipment, and other intelligent devices such as CAD/ CAM systems in the industrial environment regardless of brand. Products will be sold to industrial equipment manufacturers on an OEM basis.

Chip Manufacturing Plant Proposed

National Semiconductor Corp. has signed a conditional contract for the purchase of approximately 90 acres near Portland, Oregon for the site of a proposed major semiconductor wafer fabrication plant to be fully developed in the 1990's. National estimates that the proposed plant would employ approximately 2000 people.

AMD Discontinues Products

Advanced Micro Devices has discontinued its board and development system products, which accounted for less than 1% of its sales in the September quarter. Orders now on the books will be honored, and warranty service will be provided for the duration of warranty periods. AMD will concentrate its resources on monolithic ICs.

Matra Enters US Telecomm Market

Matra Group, a French corporation, has formed Matra Communication, Inc. to market the Scanset line of personal information terminals in the US. The terminals are desktop combination voice/data tools that combine a telephone, modem, CRT screen and keyboard to provide immediate access to internal and external databases.

Motorola Achieves Half Micrometer SRAMs

Motorola has fabricated 1K static CMOS RAMs with halfmicrometer geometries in its Submicron CMOS development and the VHSIC program. The 1K SRAM, containing 7,500 transistors, features fully scaled CMOS devices with half micrometer physical gate lengths. Demonstrations were with a three volt and a five volt power supply, and direct write electron beam and optical lithography were used in fabrication.

Logic Arrays for Military

Applied Micro Circuits Corp. has received a 12-month contract to supply bipolar logic arrays to the Westinghouse Defense and Electronics Center in Baltimore. The high performance Q700 logic arrays will be used for production of the F-16 and B-1B airborne radar systems.

Design Center Offers AMI Libraries

The gate array and standard cell design libraries of Gould AMI Semiconductors will be offered through a design center opened by Western Micro Technology, Inc. The libraries are available for 3-micron single- and double-layer metal CMOS gate array families and 3-micron CMOS standard cell libraries.

Largest Logic Simulation Claim

A benchmark test run for Westinghouse Defense Electronics Center resulted in the largest logic simulation using a workstation. A CAE Systems Model 2000 workstation was used in conjunction with a Zycad Logic Evaluator LE 1008 and the circuit that was simulated represented the equivalent of 292,000 2-input NAND gates. The total time was 10 minutes, with the LE 1008 taking 17 seconds.

Honeywell Markets IBM Subsystems

Honeywell will market IBM 3380 and 3880 large disk storage subsystems for integration into its DPS 8 and DPS 88 large-scale computer systems. The agreement provides for the IBM disk drives and controllers to be sold under the Honeywell name.

Symbolic Processing Workstation

Texas Instruments has introduced the Explorer System, an advanced symbolic processing computer designed for development and delivery of artificial intelligence-based applications. The system is a single-user LISP computer and was developed along with LISP Machine Inc. (LMI) and the Massachusetts Institute of Technology. The Explorer's architecture and software are compatible with the LMI product line and will be distributed in the Lambda line.

Prime Establishes Japanese Subsidiary

Prime Computer, Inc. announced the acquisition of Prime Computer, Japan, Inc. as its wholly-owned subsidiary to sell and service its product line in Japan. The subsidiary will focus on the CAD/CAM, computational timesharing, and distributed data processing markets.

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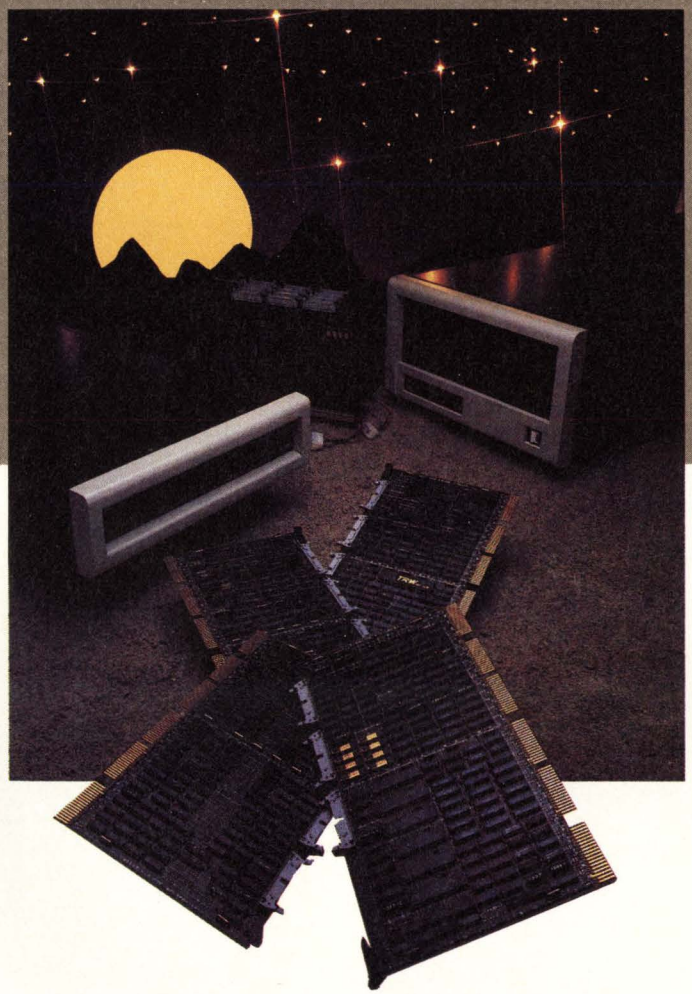

Mini-MAP makes it practical to apply array processing to general-purpose scientific and engineering computing.

Practical in terms of use: Mini-MAP's compiler allows you to program the array processor directly in FORTRAN. An assembler, a linker, and a debugger are also part of the package. Plus you can use our library of over 250 highly optimized scientific subroutines.

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Practical in terms of throughput: Because it is an array processor, Mini-MAP increases the computing speed of a mini or super-mini computer as much as 10 to 100 times. Where it takes a typical minicomputer minutes to perform tasks such as image rotation, Mini-MAP reduces interactive response times to seconds. Your computer may require hours to perform each step of a trial-and-error-process such as simulation, but Mini-MAP, can zip through in mere minutes.

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WASHINGTON REPORT

by Anne A. Armstrong

NSF Sifts 22 Bids For Supercomputer Centers

The National Science Foundation is evaluating 22 bids from universities and corporations that want to take part in the foundation's $40 million supercomputer program. NSF plans to begin the program by establishing three centers where academic and scientific researchers from around the country would have access to the supercomputers.

Although there is no restriction on where the centers should be placed, most industry observers expect them to be located in university settings. Currently only four schools – The University of Minnesota, The University of Georgia, Colorado State and Purdue – have supercomputers, which may give them an edge in the proceedings.

NSF officials told us that the bids are now being reviewed and that the entire review process – with site visits – could take until the end of the year. By January, they hope to have the bids ready for approval by the NSF board.

In addition to the special centers, NSF is also preparing to award grants in other areas including networking of supercomputers, remote access to supercomputers, software productivity and development, and a joint industry-university technical demonstration of the power of advanced computing.

There is also some funding designated for artificial intelligence research but most of the government work in that area is coordinated through DARPA.

Zenith Grabs Another Defense Contract

Zenith Data Systems beat out some computer giants and again snared a big Defense contract for microcomputers. Last year Zenith won a $29.3 million contract to provide the Air Force, Navy and Marines with a minimum of 6,000 Zenith Z-100 personal computers. Actually, the services ordered 17,000 of the machines. Now it has won another contract – worth up to $300 million – to supply the Air Force and the Navy with Tempest-secure Z-150 microcomputers over the next five years.

Tempest computers are specially designed and built to be secure and are used in classified government and diplomatic applications. Zenith's micros were not shielded in lead like others bidding on the contract, rather the data is secured electronically within the computer.

Two versions of the Tempest-Z-150 will be acquired: one with two 5¼" floppy-disk drives and one with one floppy drive and a removable cartridge Winchester disk drive. Both color and monochrome monitors will be available.

The Tempest models will also come with software bundles specified by the Air Force Computer Acquisition Center.

Box Scores On Legislation

Chip Protection. Congress finally passed compromise legislation that extends a special freestanding form of protection that is separate from copyright. It covers chips brought out after July 1, 1983 and specifically permits reverse engineered chips. A new symbol of an M surrounded by a circle, similar to the copyright designation, has been approved for use. The term, "Mask Work" or the alternate abbreviation "*M*" may also be used.

Export Bill. Differences between the House and Senate were not settled in the export fight and the bill died in conference committee. The debate centered on who should review applications to export high tech equipment – the Department of Commerce or DOD or both – and what types of equipment should be subject to the strict licensing procedures. Currently, the administration is relying on its emergency posers to extend the old export law, which expired in December 1983.

Computer Crime. A watered-down version of the computer crime bill passed both houses, however, neither ended up happy with the results. The three main categories of unauthorized access now classified as a crime include: tapping into classified information, into any financial information protected by privacy laws, or into any federal government computer. Objections centered on drafting language and jurisdiction. Left uncovered by the legislation are the huge numbers of private sector companies.

Congress Facilitates Joint Research Ventures

After months of debate and haggling, Congress finally had to deal in the closing days of the 98th Congress with a host of issues it had left hanging. In the course of a couple of weeks, the legislature had to resolve differences in export controls, computer crime, chip protection, and joint research incentives. Not all made it through the pipeline.

But the need to look supportive of US industry as it struggles to compete with a coordinated Japanese research effort finally swayed House and Senate conferees on the National Cooperative Research Act. Differences over payment of attorneys' fees in antitrust suits were settled and the compromise version passed both houses and was sent to the White House, where signature is expected.

The new legislation offers companies who wish to band together an opportunity to share research while limiting their liability in case of an antitrust lawsuit. Simply registering a joint venture with the Department of Justice reduces the liability to actual damages, instead of the triple damages called for in other circumstances.

As the bill was clearing Congress, a new joint venture has been proposed. Eleven companies that develop software for Department of Defense applications announced that they are studying a defense software joint venture. TRW Inc., Boeing Co., Ford's Aerospace & Communications Corp., General Dynamics, GTE's Government System Corp., Lockheed's Missile and Space Co., McDonnell Douglas's Astronautics unit, Rockwell International Co., Science Applications International Corp., United Technologies Corp., and E-Systems Inc. have each contributed $50,000 to fund the planning for the new enterprise. TRW's plant and people in San Diego will direct the planning effort.

The project is expected to focus on defense software needs as one way to help DOD stop escalating software costs, but the exact parameters of the project, its physical location, and even the final decision to proceed have not yet been made.

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The MARS-432 32-bit, programmable, floating point array processor.

And with good reason. Because the MARS-432 has opened up a new world of speed, power and ease-of-use that's hard for anyone to resist.

The MARS-432 already interfaces with some of this world's leading computers — DEC, Apollo, Elxsi — to provide users with a new level of computational power. Interfaces for other leaders such as IBM, Perkin-Elmer, and Gould/SEL are scheduled to arrive soon.

Simply put, we're setting the direction in state-of-the-art array processors with features such as:

Programming Ease

All of the computational power of an array processor doesn't mean much if accessing that power requires days of tedious programming, debugging and reprogramming. That's why we engineered the MARS-432 with an architecture specifically designed to support a FORTRAN compiler and a screen-oriented debugging system that make accessing and utilizing its raw power a very civilized process.

The MARS-432 also provides:

- ☐ *A Microcode Development System for off-line program development.*
- ☐ *An AP Run Time Executive Support Package (AREX) for simplified processor initialization, I/O operations, and array function executions.*
- ☐ *Applications Libraries for math, signal processing, and image processing.*

Speed

- ☐ *Add and multiply times of 100ns.*
- ☐ *Computational power of 30 megaflops.*
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- ☐ *Data memory write or two reads in 100ns.*
- ☐ *Memory paging for uninterrupted processing during I/O transactions.*

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Program memory contains a physical address space of 4K words and a virtual address space of 64K words via a cache configuration. Data memory contains a physical address space of 16 million words.

The MARS-432 from Numerix: a journey to faster, more affordable array processing power. With programming ease that sets it worlds apart.

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Graphics Processor Offers High Speed At High Resolution

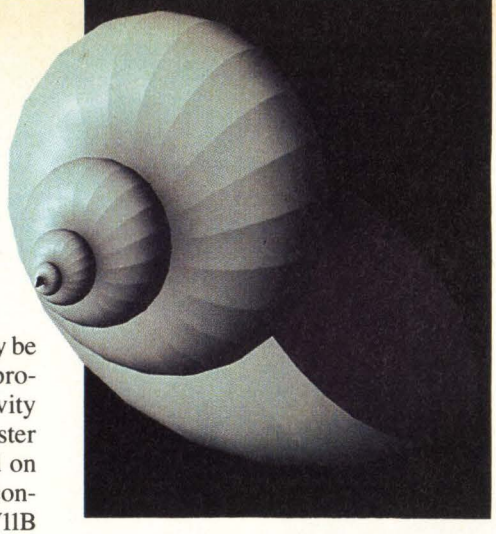

Image displayed on Raster Technologies' One/380. (Design by Olin Lathrop)

The importance of high performance graphics systems is being seen in solid modeling applications, image synthesis, image analysis, simulation, and VLSI CAD. As a result of increasing graphics demand, users are becoming more sophisticated. While two years ago graphics users may not have even heard of various shading algorithms, they now request implementations in hardware. Additional demands include faster vector generation, hidden surface calculation, higher resolution, 3-D rendering with Z-buffering, and more colors. All of this, of course, at lower prices.

The solution for system integrators to upgrade system performance was with software, assuming the host has the capability and the software team has the expertise. The other solution is the use of a modular subsystem dedicated to execution of graphics commands. A dedicated graphics processor has the ability to perform graphics functions while the host is focused on managing the database and I/O functions. But most importantly, a dedicated processor performs almost a hundred times faster than relying on a host to execute all functions.

To meet the challenge of demanding graphics performance, Raster Technologies (North Billerica, MA) is offering a new generation of their graphics processor line, the model One/80, and more recently, the Model One/380, an upward, fully compatible extension of the Model One line.

With vector writing rates of over 70,000 vectors per second, the One/80 displays a 1280 × 1024 pixel screen, refreshing the noninterlaced display at 60 Hz. Double buffering is supported in hardware providing a faster vector speed of 115 vectors/sec. Pixel updates throughout are a fast 8.7 nsec/pixel. Standard features include integer zoom, from 1 to 16; panning capability; firmware and hardware crosshairs, and vector clipping. The One/80 includes an 8 bit in/24 bit out look up table for displaying 256 simultaneous colors. The requirements for a system of this resolution requires 120 MHz logic, very fast for any graphics system.

Interfacing with a host may be through any of the four serial ports running at 38.4 Kbaud. Although the commands may be transmitted in ASCII mode, binary protocol combined with local interactivity allows remote applications to run faster and more efficiently. Also standard on the One/80 is an integral DMA port conforming to DEC's DR11W and DRV11B specifications allowing transfer rates of up to 6 Mbytes/sec. The additional serial ports are typically used for data tablets or other interactive devices.

Physically, the One/80 consists of a 5¼" tall rack mountable chassis, a 5 slot backplane and two PC cards: the graphics processor and the memory unit. The remaining slots are for additional memory such as dispay list memory and double buffering. The graphics processing unit consists of a Z8002 running at 8 MHz, 4 AMD 290ls (bit slice processors), and a communications controller. The Z8002's function is an interactive device manager to process interrupts from any ports or the bit slice processor. The Z8002 has 32 Kbytes of RAM and 128 Kbytes of ROM.

The memory unit contains memory up to 1.3 Mbytes (160 64K × 1 RAMs) and cycles at 370 nsecs. There are two ways one can maximize the available memory while increasing performance: double buffering and blanking the display. Because each 8-bit deep memory unit can be addressed as two 4-bit nibbles, double buffering is possible using 16 colors. This also increases the pixel drawing rate to over 3 million pixels/sec. Blanking the display is another method of increasing speed where improvements are in the order of three times faster.

An important issue in computer graphics is the control of large amounts of information. The communications controller, also known as a cross point switch, transfers data from one point to another. Although the host DMA path to the bit slice processor is very important, other ports can communicate with each other. The ability to switch from high level instructions to low level, while incorporating a dual processor architecture, is the reason why the communications controller is so important.

The bit slice processor, which is a 16-bit horizontally microcoded processor, runs at a cycle time of 185 nsec (slower for less resolution). The graphics processor's function is to decode incoming graphics commands and generate graphics primatives. A major increase of speed is accomplished through the use of two separate buses that either deliver data to or from the 290ls. The bit slice processor is controlled through the use of a 64-bit wide writable control store. RAM used instead of PROMs allows greater flexibility in developing microcode. Commands originate from the communications controller. Because some commands require repetitive operations such as image transfers, the inner most loop of commands have the greatest effect on processing time. The processor is designed so that 14 commands can be executed in a single microcycle through the use of special external registers and counters. This is one of the primary reasons why graphics execution on the One/80 is so fast.

Very important for a graphics processor is local intelligence. The One/80 firmware can be divided into two major functions: communications control and graphics interpretation and processing. The command set has over 125 commands that have capabilities beyond graphics primatives. Polygon fill, for example, can be executed several ways. A complete command set allows the system to work with a variety of graphics software. Macro facilities, which combine often repeated commands into one, are possible allowing newly invented commands to be created. This is useful when the program is to execute a special function when a button is pressed on a graphics tablet. Up to 256 macros may be stored at any time, allowing nesting to 8 levels deep.

Diagnostics is also provided which is

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In today's market of compressed product life cycles, it is imperative that your product remain the leader for as long as possible. That's a problem which Zitel turns into opportunity. Because the Series 90 Family accepts new memory component technologies as they become available.

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For unfriendly operating conditions, we offer ideal add-on for mobile and impact-susceptible environments normally associated with defense and geophysical applications. And there's main memory add-on, intelligent memory, disk replacement and disk cache.

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essential for understanding the reasons why an excecution didn't take place. The Replay command, for example, allows a user to replay the last 32 characters that were sent over the host interface. A special debugger and a command stream translator are available. The debugger allows single stepping through the commands, listing all macros, listing the contents of the macro, and exiting. The command stream translator allows the user to disassemble the command stream from the host directly and see the commands as they are being executed. On board LED indicators also help isolate with diagnostics. An added feature to operation is the help facility that guides the application developer with on-line prompts and command references.

High speed vector generation is accomplished through a custom dedicated processor that off-loads processing from the CPU. A vector queue resides between the CPU and the vector generator and stores up to 240 vectors waiting to be drawn. The processor which performs the vector to raster conversion requires 1.6 μsec/vector for hardware setup. Each pixel of a vector takes 400 nsec to compute and write into image memory. As a result, the vector generator takes 1.45 μsec for a total of 700,000 pixels/sec. Blanking the screen increases the rate one-third higher to over 1M pixels/sec. Because vector generation speed depends on the length of the vector, the calculated average rate is 12,000 vectors/sec.

The One/80 is designed for supporting software for all model One series, in addition to allowing for future development such as 3-D and image synthesis. The speed and power of the One/80 is clearly cost effective at below $25,000.

The Model One/380, touted as the first high-resolution graphics system to provide a complete and integrated rendering pipeline, is enhanced with a 32-bit floating point co-processor and enriched command set. The Model One/380 is an integrated 3-D display system that puts together all of the key rendering functions in a high resolution 60Hz refresh system. Priced at $41,500, the complete system includes a monitor, keyboard, data tablet and mouse.

– MacNicol

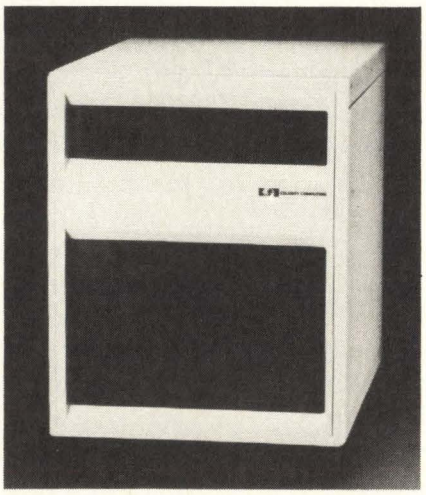
Circle 231

DEPARTMENTS/CAD

General Purpose Workstation Boasts Exceptional Performance

The number of workstation manufacturers is growing, and the makers of these systems are bracing for stiff competition among themselves. Manufacturers continue to cite statistics that indicate 90 to 95% of the potential workstation market has yet to purchase a system. Perhaps potential users are waiting until an undisputed need for a workstation arises. On the other hand, much of the design community may be reluctant to make a large capital investment and are waiting for price reductions. A third possibility may be that the market is just biding their time and waiting to see which manufacturers will be the key players in the industry.

As far as choosing a workstation, the obvious criteria for a workstation is flexibility and high performance. Flexibility in this sense is defined as meeting the needs of tomorrow's designs as well as those on the drawing board today. Whether a system can be easily integrated into existing design environments is a crucial element in making the best choice. And whether a workstation can be easily upgraded to perform new tasks is another important aspect of picking a workstation. In many cases, the card cage in a workstation is based on a proprietary bus or has only a limited number of expansion slots.



The C1200 Professional Workstation is based on a proprietary 32-bit processor, uses a Multibus configuration and supposedly offers speeds of up to 2 Million Whetstones/second.

Most of today's general purpose workstations are adopting enhanced versions of Berkeley's UNIX operating system. And as far as integrating these systems into the design environment, Ethernet is also gaining widespread acceptance.

A recent newcomer to the workstation arena, Celerity Computing (San Diego, CA) has introduced a 32-bit workstation which the firm claims offers 10 times the computational performance of other existing microprocessor-based systems. According to Celerity's benchmark studies, the new workstation, model C1200 Professional Workstation, executes 2 million single precision and 1.5 double precision Whetstone instructions per second. In comparison to a VAX 11/780, it supposedly performs 1.5-2 times faster than the VAX.

Celerity's Marketing and Sales Vice President Tom Lydon gives the impetus behind designing high performance workstations as "(existing workstations) already provide an alternative to time-sharing. They provide attractive price/performance and a low entry price, but the problem with currently available workstations is their limited performance." To gain this higher performance, the C1200 uses the firm's proprietary Accel processor. Celerity claims that the processor's architecture has been optimized for computationally intensive tasks by utilizing cache memories, a three-stage pipeline, and multiple 32-bit data and instruction paths.

Based on UNIX 4.2 bsd, the C1200 is built around the Multibus and offers 11 additional expansions. Like most other workstations, the C120 uses the Ethernet network. The system can be configured with up to 24 Mbytes of physical memory and includes a 56 Mbyte storage disk. Other features of the system include streaming cartridge tape for back-up and archiving, and optimizing language compilers for Fortran-77, Pascal and C. The firm also offers an optional high resolution color display.

– Collett

Circle 234

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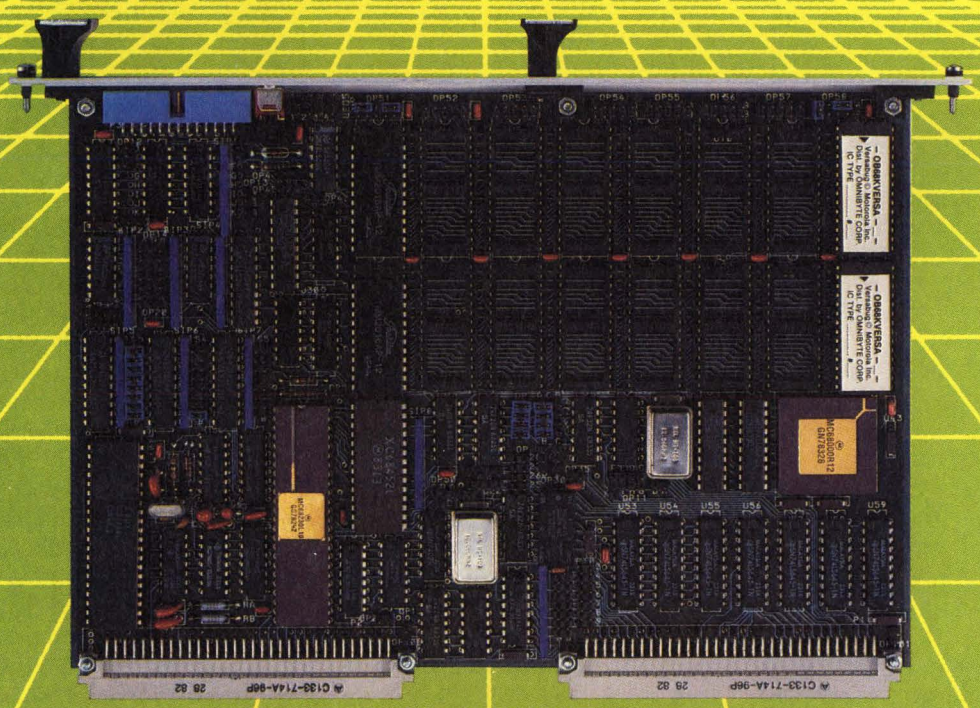

OB68K/VME1™

The OB68K/VME1 is an extremely powerful, complete stand alone microcomputer board that is functionally interfaced to the double height (6U) VME bus and is fully compatible with the VME bus standard (Rev. B) by way of the P1 connector.

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  - RAM 2K x 8 or 8K x 8 static
- Offboard I/O space 64K bytes (short Address Modifier code)
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- (2) RS-232C Serial Ports utilizing one 68681 DUART
- (2) 8-bit Parallel I/O Ports with two control lines utilizing one 68230 PI/T
- (1) 16-bit Timer/Counter (in 68681)
- (1) 24-bit Timer/Counter (in 68230)
- System controller functions are supported. They consist of:
  (1) 4-level Prioritized bus arbiter
  (1) 16-MHz system clock
  (1) Power-on Reset Generator
  (1) Manual Reset Generator
  (1) System watch dog timer
- All System controller functions may be inhibited for Multi-Master System use if desired.

Our extensive quality control procedures give you a highly reliable product backed by Omnibyte's two year limited warranty.

Software available for the OB68K/VME1 includes the optional VME1 BUG™ monitor/debugger and a variety of other packages.

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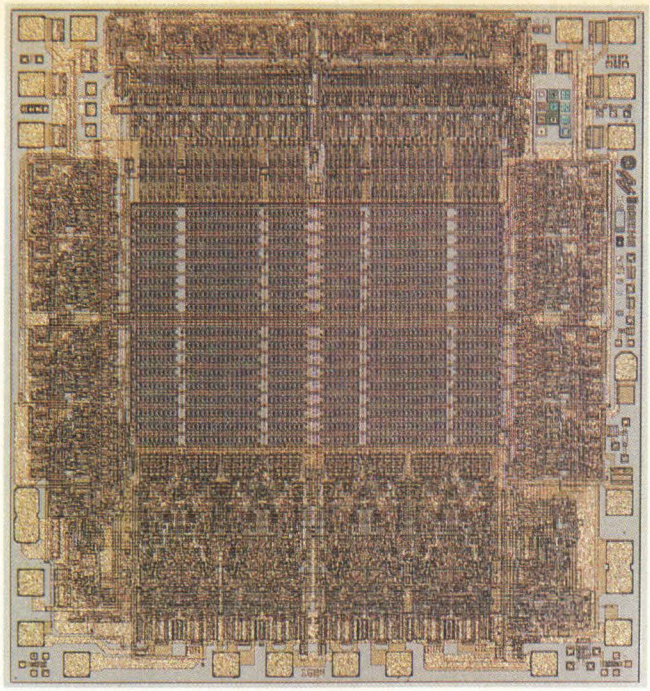
New PALs Offer Strong Alternative To Gate Arrays



National Semiconductor's new PAL (PAL 16-R4B) offers 15 nsec propagation delays, 16 logical inputs and registered outputs.

A great number of OEMs have been somewhat reluctant to use gate arrays in new designs. Reasons for the hesitation include high costs, risk factor and the inertia of standard TTL off-the-shelf parts. Risk factor becomes a crucial parameter when rapid turn-around-time is critical. If a problem occurs with either the fabrication process or the actual design (i.e., a design oversight), the design cycle for a gate array could easily double. Also, when incorporating a gate array into a system, the customer becomes highly dependent upon the gate array vendor – a rather vexing thought in the mind of an OEM. And with market windows continuously getting narrower, a lengthy design cycle could easily cripple a product's success.

The potential problems that accompany gate arrays has sparked increased interest in programmable array logic devices (PAL). Faster turn around times is one of the significant advantages that PALs enjoy. In contrast to the gate array approach, potential users have complete control over the design cycle in as much as PAL customizing (i.e., fuse burning) is done in-house.

As a result of the PAL market growth, Monolithic Memories Inc. (Santa Clara, CA), recently announced a 5,000-gate PAL that will undoubtedly compete with comparable products from gate array vendors. This new device, designated the MegaPAL, whose part number is PAL 64R32, has 32 registered outputs, 64 logical inputs and is based on a bipolar technology. (A CMOS version of the chip is expected early next year.)

Greater functionality, however, often translates to increased design complexities. With respect to the higher levels of PAL integration, software support will be the key element in determining whether this device can effectively compete with 5,000-gate arrays. MMI has recognized this and plans to offer a more sophisticated version of PALASM that will provide automatic test vector generation.

With this new test capability, the software automatically computes and generates the test vectors necessary to provide 100% test coverage. A slight drawback to this exceptional feature comes at the expense of programmability. That is, the MegaPAL cannnot be programmed to incorporate feedback loops in the combinatorial section of the device. Simply stated, the user cannot create custom latches and therefore must use the device's predefined latches. For most applications, this is not a major constraint. In creating the 16 MHz 84 pin device, MMI felt it was far more important to provide the user with 100% testability rather than combinatorial feedback.

MMI's new automatic test vector generator may give them an initial edge in the PAL battleground, but others will likely follow suit. Generating test vectors for PAL type devices has been a difficult chore for PAL users. In a typical design situation, test engineers receive the Boolean equations from the design engineer. The test engineer must then convert these equations into logical elements so that the test simulator can simulate the PAL. As would be expected, this process can be a substantial task.

National Semiconductor (Santa Clara, CA), Texas Instruments (Dallas, TX) and Advanced Micro Devices (Santa Clara, CA) have also waged PAL campaigns. As opposed to the MMI's VLSI PAL route, National and TI have been battling over who will offer the fastest PAL on the market. Both claim to currently offer devices with propogation delays of 15 nsec. In response to these new high speed devices, MMI has announced plans to unveil a similar type of device.

National's new PAL family is comprised of four devices: the PAL16L8B, the PAL16R8B, the PAL16R6B, and the PAL-16R4B (**Figure 1**). All have tristate outputs, dissipate 600 mW and come in 20-pin packages. Note the designation model numbers of the new line: the first two digits refer to the number of logical inputs, the third digit refers to the number of outputs, the "L" refers to an active low output, and "R" to a registered output. (Texas Instruments' new line of PALs appeared in October, 1984 *Digital Design*).

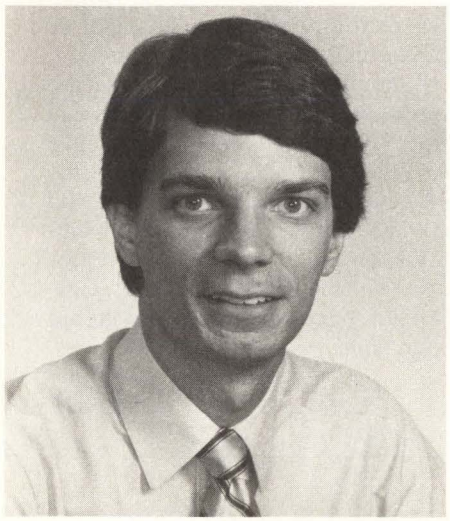
Other recent announcements from National include nine half-power bipolar PALs that, according to the firm, dissipate the lowest power of any 20-pin device on the market. These parts have a maximum propogation delay of 35 nsec over the commercial temperature range, maximum supply current of 45 mA and typical power dissipation of 125 mW.

Similarly, AMD is also vying for a share of the PAL market. Earlier this year the firm spoke of a new 800-gate PAL device whose outputs could be programmed for combinatorial or registered operation. The official release of the AmPAL22V10, however, was not announced until October 1984.

A new PAL programming tool has also been introduced by AMD. The software, designated Programmable Logic Programming Language (PLPL), can be used as an alternative to PALASM. According to AMD, PLPL supports all of AMDs current PAL devices and runs under IBM DOS 2.0, UNIX 4.2 and VMS. In addition, a simulator module that will allow designers to simulate and debug PAL devices before blowing fuses will be available in early 1985. – *Collett*

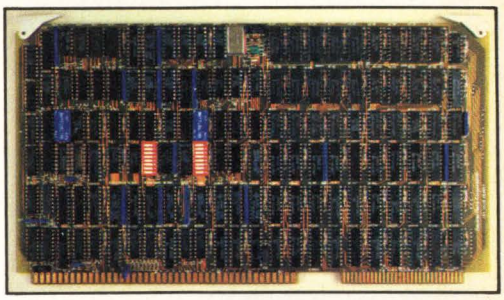
Monolithic Memories **Circle 236**
National Semiconductor **Circle 237**
Advanced Micro Devices **Circle 238**

Central Data is High Performance Multibus* Speed

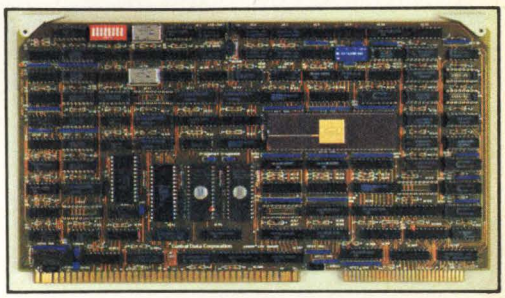


Jeff Roloff, President

"Central Data is commited to helping you get the maximum performance from your Multibus system. Our iLBX Cache Memory Board and 12.5 MHz 68000 CPU can do just that."

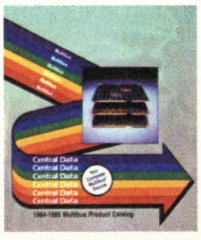


The new **Multibus iLBX* Cache Memory Board** delivers processor independent, high speed memory through the iLBX interface on the Multibus. The board's unique cache memory images the entire Multibus memory using a two-set LRU caching algorithm and stores 4K bytes of the most recently used memory. Access time is under 100ns, much faster than any dynamic RAM board. This new board also features write through operation, extensive error checking, and automatic and invisible deselection on error with interrupt. Its forced miss mapping allows use with dual-port memory on the Multibus. The **B1041** is available in 100 up pricing at $1145.



The new **Multibus 12.5 MHz 68000 CPU** also takes advantage of the iLBX architecture by allowing connection to the Cache Memory Board or to dual port iLBX memory. The board's central processor is the powerful 68000 or optional 68010 and features paged SUN memory management. It supports 8 Multibus interrupt levels in either the bus-vectored or non-bus-vectored mode. The board has three programmable timers and two EPROM sockets for monitor or bootstrap programs. Its full multi-master capabilities allow the use of several processor boards and DMA devices on the bus at one time. The **B1045** is available in 100 up pricing at $975.

New 1984-85 Fall Product Catalog now available. Call or write for your copy.



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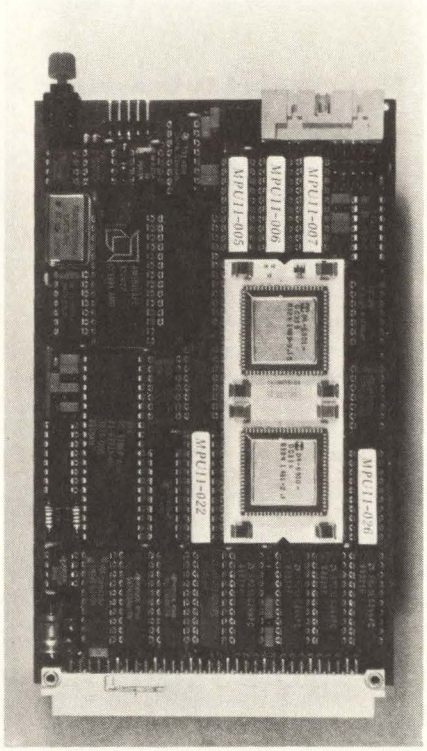
New Eurocard Offers DEC Compatibility

Offering a new bus structure to a market where competition is already fierce may almost seem futile, but this is exactly what Gespac (Mesa, AZ) has done. Granted, the new Eurocard format does have some following in Europe, but it may take time before it is accepted in the US. Positioning the bus between the STD and VME in terms of performance, Gespac does have the advantage of being able to offer a wide range of cards to the systems architect.

The latest of these, the GESMPU-11, has been designed around the J-11 CMOS dual processor chip from Digital Equipment Corp. The J-11 has a 32-bit internal data path with 16-bit I/O and implements the full PDP-11 instruction set including hardware multiply/divide (EIS), FP-11 floating point instructions, and MICRO Online Debugging Task (ODT).

The on-chip memory management unit (MMU) extends physical memory addressing on the G-64 bus up to 0.5 Mbytes. Three modes of execution—kernal, supervisor, and user—enhance the memory protection scheme. This increases the flexibility of timesharing and multiprogramming environments.



The GESMPU-11 is designed around DEC's J-11 CMOS dual processor chip.

The module includes an asynchronous RS-232C/V24 compatible serial communications interface that can be jumper selected to provide DCE (modem) or DTE (terminal) connection.

Of the 10 different interrupts that are supported, six are internal to the module (three from a timer/counter, two from a DEC DC319 DLART, and one from the RTC). They are managed by the AMD AM9519A interrupt controller. By merging the standards of the DEC microprocessor with the G-64 standard bus, Gespac offers the systems integrator software compatability with DEC's PDP-11 series.

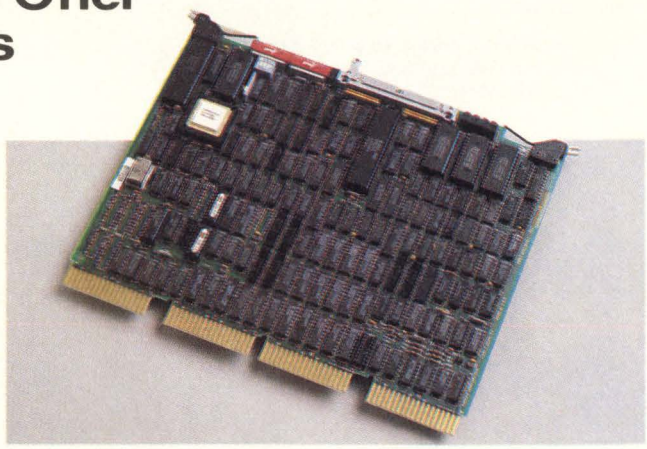
—Wilson

Circle 232

DEC Compatible Controllers Offer Performance Enhancements

Following hard on the heels of their UC02 and UC12 Q and Unibus adapters (*Digital Design*, October 1984, p. 67), Emulex (Costa Mesa, CA) has announced two performance enhancements in the form of the UC03 and the UC13.

The adapters combine with the Emulex ESDI or ST506 disk controllers and Emulex QIC-36 or Ciper 540 tape controllers, allowing the systems architect to configure a wide variety of disk and tape drives for his storage needs. Both adapters offer MSCP compatibility. Error control is handled by the adapters in conjunction with the Emulex controllers. When an error is encountered, the host adapter automatically attempts to correct it, and only uncorrectable errors are reported to the host. Both the UC03 and the UC13 are able to pool seeks and determine the most efficient order in which to execute them, an especially vital feature in heavily loaded systems.



The Emulex UCO3 host adapter.

During each DMA data transfer burst, the adapters monitor the bus for other pending DMA requests and suspend their own DMA activity to permit other DMA transfers to occur.

Another feature unique to the Emulex products is the "pass through" mode. This allows the integrator to communicate directly to the SCSI in a non-emulating manner for full use of all SCSI applications, including those otherwise not supported by MSCP.

SCSI's advanced bus architecture also provides for bus arbitration between connected devices with maximum efficiency. It supports multiple host systems, multithreading or overlapped operation of two different I/O devices, disconnect/reconnect of devices, and assignment of peripheral bus priority.

—Wilson

Circle 233

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CHUM SPECIFICATIONS		
Parameter	CHUM-99	CHUM-180
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Gates	99	180
Output Drive	9 ma	6 ma
Frequency	25 MHz	25 MHz
Voltage Range	3–8 Vdc	3–8 Vdc

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Circle 34 on Reader Inquiry Card

Three New Winchesters Geared For Production By Seagate

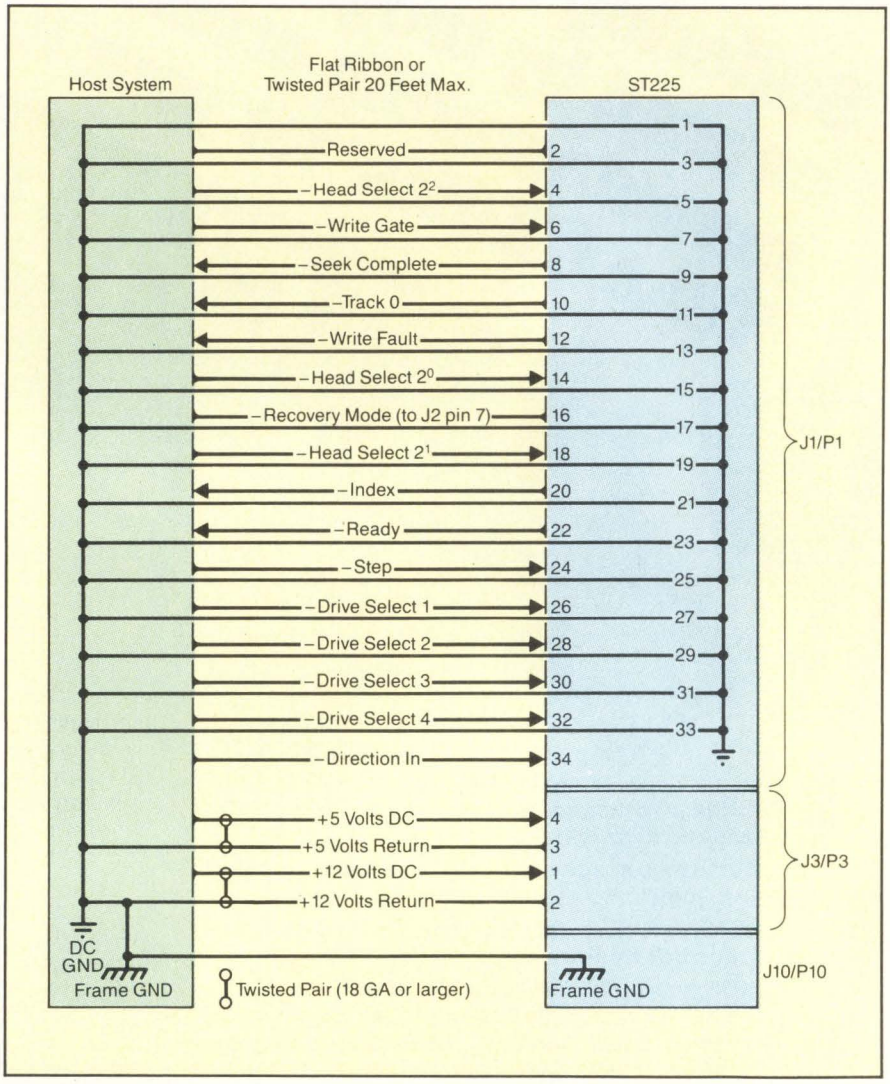
A new 20 Mbyte 5¼″ half-high, a 40 Mbyte full-height and a 10 Mbyte 3½″ hard disk drive have been recently introduced by volume manufacturer Seagate Technology (Scotts Valley, CA). These are their first new products since last year's introduction of the high-capacity 8100 Winchester drive. Like the 8100, these drives use the ST412HP interface, but at the same 5 Mbit/sec rate as the standard ST506.

The ST112 3½″, ST225 half-height 5¼″ and the ST451 standard 5¼″ form factor drives are designed to serve the professional single-user market and the low-end multi-user market. This positioning to volume produce for large markets is Seagate's traditional path. Their capabilities to ship quantities adequate for even the major OEMs is enhanced by the firm's vertical integration. They make their own parts except ICs and media.

Using open loop servo technology, the two smaller new drives are designed for low-cost medium performance. The 3½″ 112 is recorded at 10,864 bpi, 588 tpi; the larger disks of the 225 are recorded at 9784 bpi, 580 tpi; both have two disks and four read/write heads. Heads are positioned 90° off normal on these drives, and a .3μm filter is used to keep the drive interior clean.

A linear voice-coil actuator and separate servo head are used in the ST451; the full-height package houses three disks with five read/write heads. This product uses the same closed-loop servo as the 8100 introduced last year, for 40 msec average access time, including settling. Open-loop positioning on the other drives provides 85 and 65 msec average access times for the 5¼″ and 3½″ products, respectively. Al Shugart, President of Seagate, feels that 65 msec is about as low as open-loop technology will permit.

Though these products sport relatively standard specifications, the seven analog custom circuits used on the 225 are an indication of the future. More intelligence will go on drives as real estate is freed up by integration. Mr. Shugart indicated that basic controller functions could be put on a single drive-size board next year. At some point, the higher transfer rates of the ST412HP interface will likely be used, as well. For now, it provides error correction and recovery.



Cabling for the ST225 shows control lines on the J1/P1 connector, power on the J3/P3, and ground on the J10/P10; connection may use flat ribbon cable or twisted pair up to 20 feet.

In the interests of volume production, oxide media and heads are used. They feel that current metal media has too many defects per surface, but know it will be needed to double bit densities. By the time higher density is demanded in volume, sputtered thin film media will likely be reliable enough for standard use. As for thin film metal heads, Mr. Shugart has expressed a technical concern about corrosion between metal heads and metal media.

The 112 is in volume production now, with a price of $495 in OEM 1000 quantity, predicted to drop to under $300 next year. The 225 half-high is priced between $525 and $550 now, to be $350 by mid to late next year. Somewhat behind in production, the 451 is scheduled to be in production about March, at $1,250 quantity 1000, to drop to below $800 next year. These mid-range products should, unlike the 8100, provide Seagate opportunities for volume shipment in the near term.

— *Pingry* **Circle 239**

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Circle 30 on Reader Inquiry Card

Thin Fiber Optic Cables Extend Distribution Range of CAD Graphics Systems

As more CAD workstations and display controllers are used at a site, communications between systems becomes critical. For some time, Artel Communications (Worcester, MA) has specialized in fiber optic transmission products for graphics. Last summer, another fiber optics supplier, Fibronics (Hyannis, MA) announced a series of products for the CAD market, and more recently, Canoga Data Systems (Canoga Park, CA) introduced a fiber optic bus extender for graphics.

All three firms have products for Digital Equipment compatibility. Canoga's CBE-205 and Artel's DC100 support DR11-W (Artel also specifies DR11-B and MDB compatibility) and Fibronics' FM 901 is a Unibus Slot Extender. Both DR11-W systems operate at 500K words/sec; Canoga puts no qualifiers on that rate, while Artel claims that rate for DC100 connections up to 160 feet. At 1 km (3281 feet), the DC100 operates at 121K words/sec; an option allows slower transmission up to 5 km. Canoga's CBE-205 is specified to operate up to 2 km.

Products to extend distribution ranges of IBM 3250 Graphics Display Systems are also available. Artel's LS100 is transparent for IBM 5080 and 3250 connections up to 5 km (3 miles). Fibronics' FM 1601 claims a 3 km range for 3250 systems.

All of these products extend the area in which graphics processing can take place using existing host computers. Other advantages of using optical transmission for graphics are plentiful. First, the bandwidth on a single pair of fibers is greater than that of heavy coaxial cables; they can carry more signals, faster signals and/or transmit longer distances. All of this over thin cables that solve many of the installation problems of high-bandwidth coaxial cable. In addition, these cables are not electrical, so FCC emission levels are easy to meet, even over long distances. Another advantage of this cable is that outside electrical noise does not interfere with the transmission.

Links between a graphics display processor and host computer are not the only configuration for fiber optics CAD communications. Paragon Technology (Pleasant Hill, CA) designed their line of CAD systems, introduced in early 1984, to be networked with fiber. They recently benchmarked their 300 Network System Manager and workstations over the optical network.

Both Artel and Fibronics have products specified to operate with various CAD workstation networks. The 2016/2017 modules from Artel handle a dozen or more major makers' systems, and their original CV100 system was designed for Computervision's Instaview. Fibronics claims that their FOV 4000 will support several workstations in networks from some six manufacturers.

With the range of optical products continually expanding, CAD departments can distribute graphics display processors over very wide areas, while allowing interconnection to a common host and/or database. Users of several workstations in a department can now share RGB files and access host power with bandwidth to spare. *—Pingry*

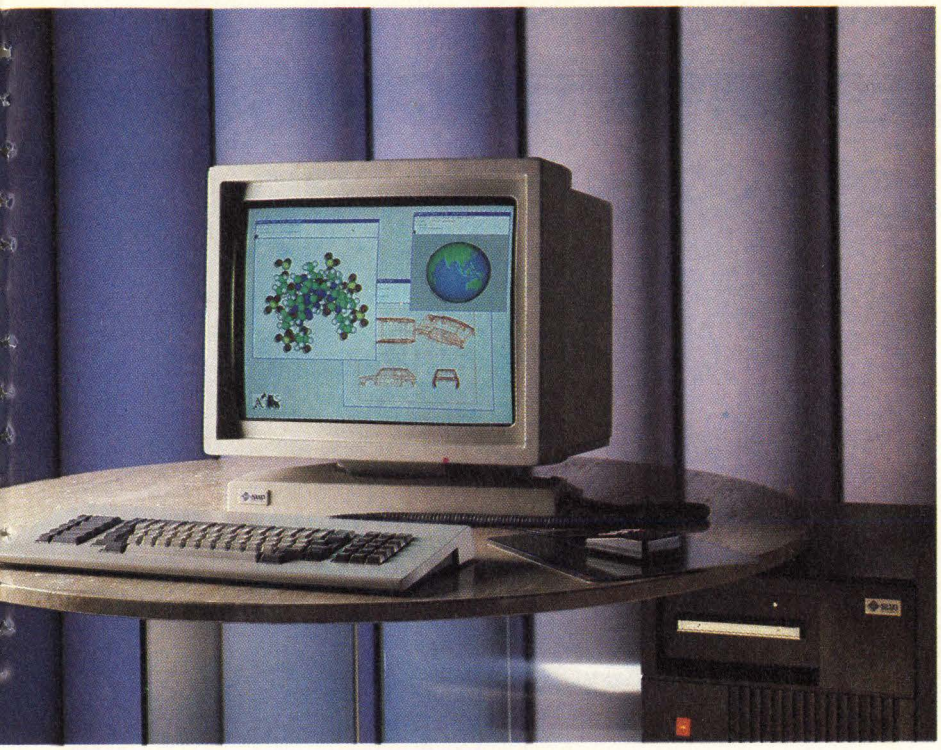
Artel **Circle 240**
Canoga **Circle 241**
Fibronics **Circle 242**
Paragon **Circle 243**

Sun Rounds Out Line With Low-End Workstation And High-End Color Graphics

Sun Microsystems (Mountain View, CA) augmented its workstation line with a low-end desktop workstation, the Sun-2/50 and a first entry into the color graphics workstation market, the Sun-2/160 Color Sunstation. The 2/50 breaks the $10,000 price barrier and is in actuality a diskless node for users who do not require the expansion flexibility of a card cage, but who desire the computational and graphics performance of existing Sun-2 products. The 2/160 Color Sunstation is a fully integrated workstation with a high resolution display and full range of software tools. All software offered on Sunstations is fully compatible with all other Sun products throughout the product line.

Aimed at multi-user, multi-vendor environments both the 2/50 and the 2/160 operate with the Sun Network File System (NFS) which supports transparent network read and write access to directories and files. As an indication of their committment to standards and open systems, Sun is publishing the NFS and supporting protocol specifications with the intent of providing a standard for network file systems. The NFS is inclusive in all Sun workstations, yet also allows heterogeneous systems running different operating systems to share files in a local area network.

Sun's enhancements to UNIX and its Ethernet interface allow the 2/50 to operate as a diskless node. With an objective of lowering cost per user, several of the diskless machines can share the disks of a Sun-2/120FS or Sun-2/170 fileserver. Sun combined the four Multibus boards of the 120 onto a single board with a CPU based on the MC68010. One to 4 Mbytes of physical memory and up to 16 Mbytes of virtual address space per process is available. A hardware floating point ac-



The 2/160 Color Sunstation from Sun Microsystems is built on an MC68010, UNIX 4.2 and operates in a local area network or as a standalone.

celerator is optional for computationally intensive applications. A 19″ 1152 × 900 66 Hz non-interlaced display is included.

The 2/160 utilizes the same display and refresh rate. Eight color planes can simultaneously show 256 colors selected from a palette of more than 16 million, and the display controller can instantly zoom in integer multiples of 1 to 16 and pan in increments of one pixel. A 12-slot card cage and VMEbus leave the 2/160 open to customization, as well as a Multibus to VME adaptor board for accommodating the wide range of Multibus boards available.

Sources at Sun say a graphics processor may be the next option offered on the 2/160, but would probably remain an option and not incorporated into the system as in the Apollo 550, for example. A 1 Mbyte 2/160 lists at $32,900, with volume discounts available and delivery in 60 days.

With recent influx of capitol, including a $20 million investment from Kodak, Sun is securing its place in the general-purpose, open-system market.

—Hanrahan

Circle 245

Universal Access Boosts Value Of Data & Systems

by Julie Pingry, Senior Editor

The immediate value of data is increasing both as computers manipulate and interrelate information more extensively and as more people use systems and realize the resource they provide. It is only natural, then, to allow more people to access information.

Data communications is a critical topic in this environment. Despite all of the press on computer networking, it is a relatively unperfected field. One of the main problems is that computing and communications have traditionally been separate industries. Similarly, purchasers of computers and communication equipment were different employees within an organization.

As more information is communicated between computers, personnel to coordinate digital networking become essential. Though the separation may exist in corporate structures, it is no longer practical. Combining responsibilities may be eased by newer products that address both processing and communication of data. With powerful distributed systems, however, optimized communication is not usually as easy as integrating a modem.

System performance can degrade to unacceptable levels when the host processor must prepare data for communications as well. Careful design for offloading, and software to allow rapid transfer of information in a format readable to other devices are critical. Effective transmission to allow true sharing of information and peripherals makes the equipment and the data at each site more valuable.

Intelligent Talk

Progress toward combining computing and communications has been going on for some time. Business computers are now commonly offered with integral modems and local area network (LAN) interfaces, notably Ethernet from companies like Digital Equipment, AT&T and IBM PC-compatible makers.

Figure 1: Switching local network firm Intecom and office computer company Wang have combined forces to design the IBX Network Workstation. This photo shows a prototype of the product, scheduled for spring availability.

Likewise, communications products, from LAN boards from Interlan (Westboro, MA), Intel (Santa Clara, CA), and Excelan (San Jose, CA) to large network processors like those from Paradyne, (Largo, FL), Racal-Milgo, (Miami, FL) and Fujitsu (Santa Clara, CA) and other large modem/multiplexer vendors, are being designed with more processing power, to offload the hosts. Communications terminals, an old type of product, are now being offered in more than dumb configurations, and sometimes, as joint ventures between communications and computer companies like the Intecom (Allen, TX)/Wang (Lowell, MA) IBX workstation (**Figure 1**).

The main factor driving the development of these products is the availability of low-cost ICs. Microprocessors for intelligent communications devices and chips or chip set implementations of modems, networks and other transmission products are widely available. Using LSI and VLSI makes data transmission less expensive and more reliable.

Communications can be built into other equipment with modem chips and chip sets. Motorola's (Austin, TX) 14412 with filters makes a 300 bps device, for example, adequate for terminals. Rockwell (Newport Beach, CA) offers a full line of modems, from 1200 to 9600 bps using three or four VLSI chips and some glue logic, on boards only several inches in either dimension. Ven-Tel (Santa Clara, CA) produced a modem for the IBM PC XT by using a California Devices (San Jose, CA) gate array. Several other firms like Oki Semiconductor (Sunnyvale, CA) also offer modem ICs, and as the need for integral communications in more powerful equipment increases, other chips for fast communications will likely emerge from labs.

Interfaces to LANs are available in chip set form, as well. Though several semiconductor houses have announced the sets, they vary in the degree of integration. Seeq Technologies (San Jose, CA) has a relatively simple Ethernet controller, but were early to market, as it was produced by silicon compilation. They are also the only house to offer the necessary Manchester encoding/decoding in CMOS. Another house early out with these two chips and a relatively simple controller is Fujitsu (Santa Clara, CA). Intel's 82586 is perhaps the most widely used controller at this point, though the 82501 Manchester chip is slow in coming. Many firms designed with the LANCE from AMD and Mostek, and had an impatient wait. Ethernet is not the only network with silicon controllers; ARCnet is supported by Standard Microsystems (Hauppauge, NY) and token passing chips are available from Western Digital

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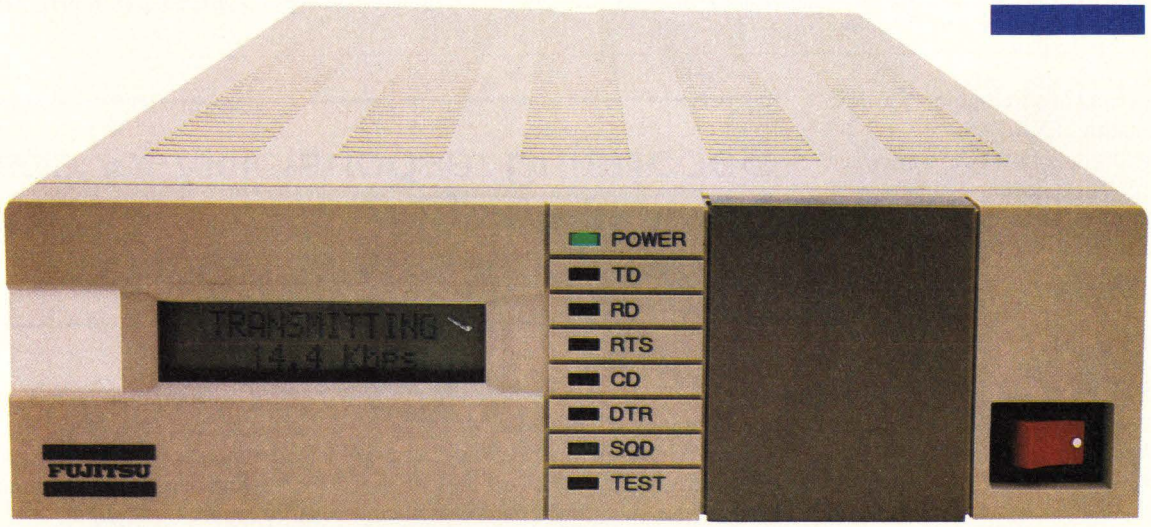

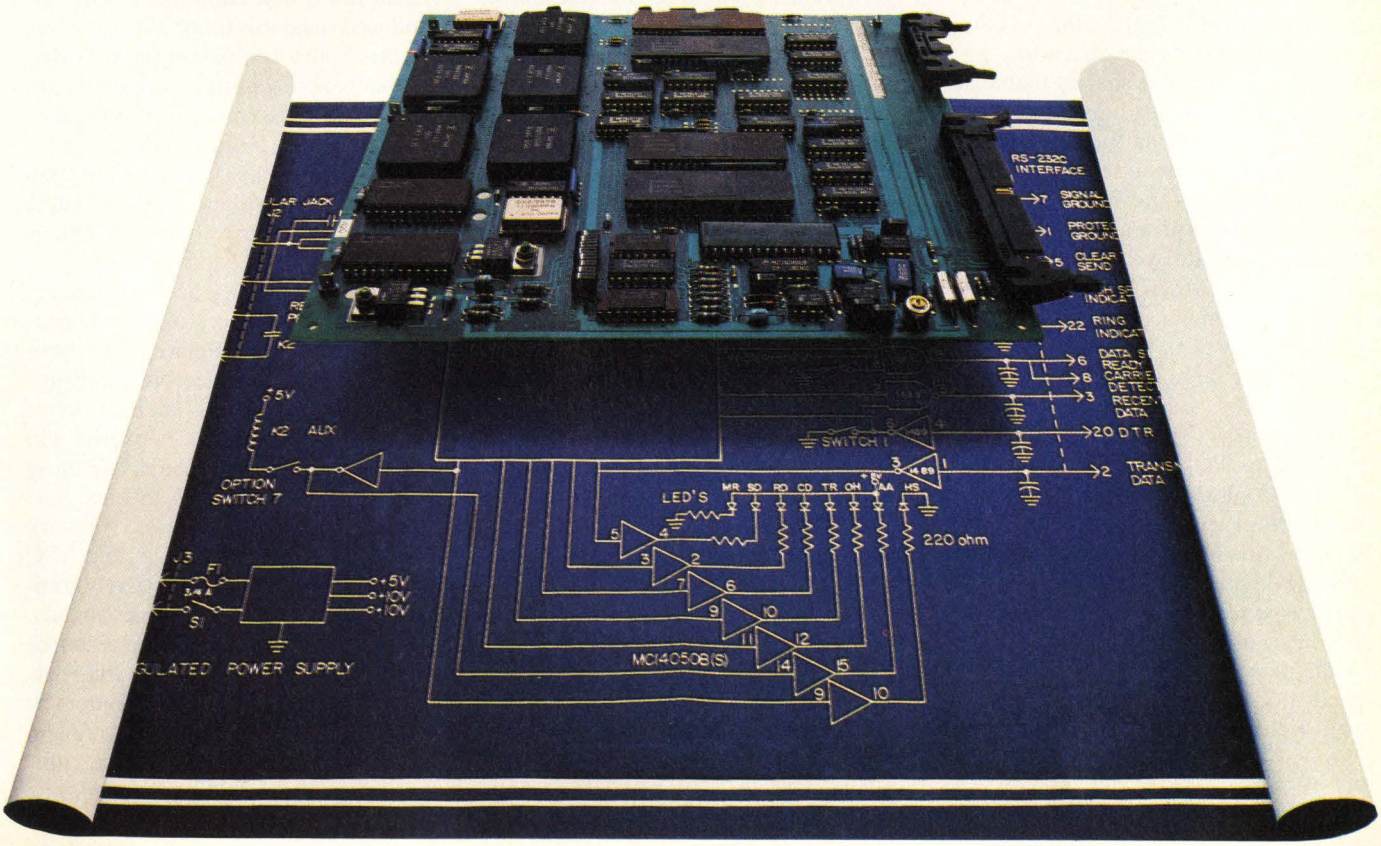

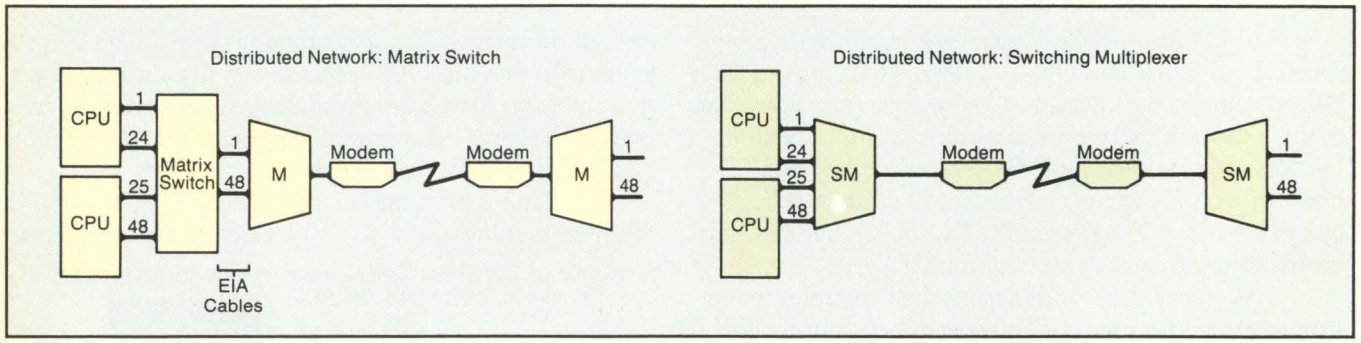

Figure 2: Combining multiplexing with X.25 packet assembler/disassembler (PAD) functions can eliminate matrix switches at each end of a multiple-line connection, as illustrated here by Timeplex.

(Irvine, CA) and in development for IBM by TI (Houston, TX).

Western Digital offers ICs to interface to wide-area X.25 packet switching networks, as well. X.25 equipment is popular for both public and private networks. Circuitry for packet assembly and disassembly (PADs), controllers, protocol processing and buffering to the X.25 spec is shrinking.

Though the usefulness in integrating communications into intelligent machines has been seen for some time, only recently have silicon implementations allowed extensive integration. Resulting chip and board solutions have made apparent the full effects of the load of communications processing on a host.

Powerful computers sharing their data is a main impetus for interconnection. Preparing information for transmission can usurp the power and time of the system processor. As traffic on data communications lines grows, a system's computational efficiency is effectively reduced by this burden. So, to maximize resources, communications devices must offload the hosts.

Still, some large switches, PBXs and network controllers have only one or two processors in a refrigerator-size box. Systems such as Network Products' (Houston, TX) CommPonents provide modules with microprocessors and RAM, much like the cards in a computer backplane. AT&T (Bethesda, MD) and IBM, as well as many of the large communications vendors, also offer multiple processors to handle data on a front-end basis. High speed modems like those from Codex (Mansfield, MA) with 68000s, benefit from processors, as do many LAN boards.

Processors are not the only important integrated components for improving communications products. Mitel (Boca Raton, FL), Rolm (Santa Clara, CA) and other large vendors boast high-performance filters, controllers, and protocol ICs optimized for data communications.

Separating responsibility for communications from computing is no longer necessary or practical.

Local Transmission

For several years, much attention has been focused on some newer schemes for short-distance multi-device communications. The term local area network (LAN) has come to mean systems with a common bus, whether in a ring, star or bus configuration. Standards set by the IEEE 802 committee cover the most common topologies and access methods in use for these networks.

This is a relatively recent definition of local area network, however, and the generic meaning should not be forgotten. Digital connections in a limited area can include voice transmission. Switched local networking over private branch exchange (PBX) systems fulfills many users' needs. Some digital PBXs, including the PNX from Ztel (Wilmington, MA), are designed for shared voice and data transmission facilities.

An installed digital telephone PBX may have adequate performance to use for data. The importance of PBX data switching is underscored by IBM's recent purchase of Rolm and DEC's offering of a PBX-to-computer interface for their VAX computer line. These and other major computer companies also offer LANs of the broadcast type, for areas that require higher throughput.

The IEEE 802 committee work has produced standards for physical and link levels of both token-passing and CSMA/CD networks. Naturally, protocol software is needed to make useful the data moved from one place to another useful. Well-designed LAN hardware should not be mistaken for a solution. It is available, but software is generally limited to certain manufacturers and machines.

And though turnkey network vendors and computer vendors offer networks across which applications can run, proposed standards for interconnecting different vendors' networks are incomplete and/or not firm. Future networks will likely use standard protocols, like those now proposed by the DOD, ISO and Xerox or some that IBM chooses. Network Research (Santa Monica, CA) and ACC (Santa Barbara, CA) have relatively complete standard protocol packages already.

PC LANs may serve well for resource sharing and can be hooked into other nets by gateways and into large computers by emulators. With the lack of complete solutions and standards, however, communications needs that can't wait may be better served by traditional communica-

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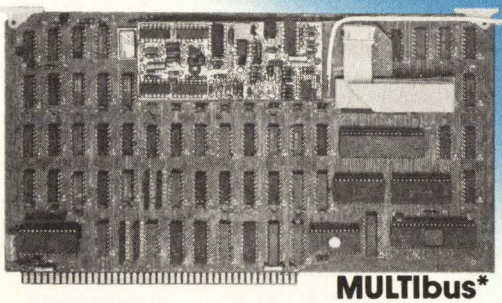

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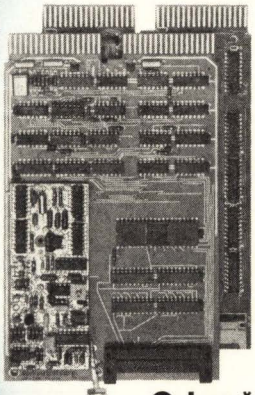

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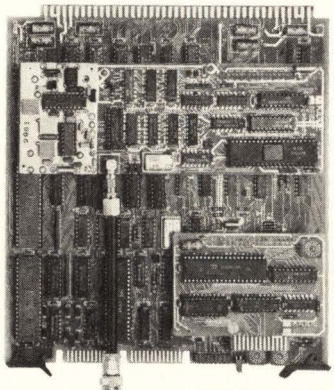

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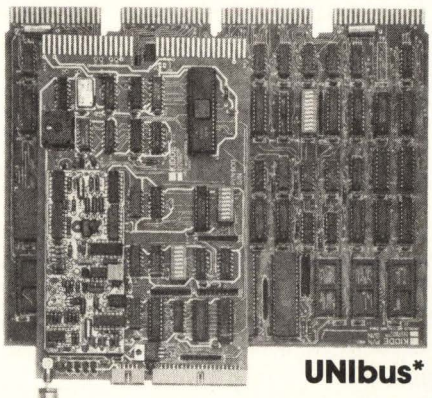

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tions products. PBXs for low speeds, as an example, will likely gain ground, and high-speed short-haul communications may use multiple limited-distance modem connections or multidrop private lines.

Wide Area Lines

Packet switching networks are an area of communications in which the US and European markets are similar. The lower line cost of the packet-switched networks compared to switched telephone networks have made these offerings especially popular for interactive communications. Telenet, Tymnet and several other national networks are providing longer-distance communications. And, as in Europe, the majority of packet nets use the CCITT's X.25 specifications.

Because of the popularity of X.25 communications, chips such as Western Digital's are available for integrating that function. The PAD function can be integrated into terminals or with other communications functions (**Figure 2**). Public packet switching is not the only application for X.25. Many larger corporations have needs for large volumes of interactive communications, and private packet switching to interconnect several locations can meet those needs.

AT&T has introduced a virtual circuit switch in its Datakit. Virtual circuit switching, as the name implies, eliminates the store and forward of message and packet switching networks, while providing local and wide area connections. Different protocols and types of interconnection are offered on separate circuit boards that slot into a cabinet (**Figure 3**).

Another recent announcement using modularity to interconnect various devices and networks is from Banyan (Westboro, MA). Their network server uses a 32-bit processor with memory, an I/O bus, Winchester, floppy and tape cartridge storage and expansion. Such communications computers, often called servers, play increasingly critical roles as various types of connections are used to complete networks.

As for more traditional telephone line networks, similar increases in the processing power of equipment permits voice lines to carry high speed traffic. Data over voice equipment from Coherent (Hauppauge, NY) and others allows speeds up to 19.2 Kbps full duplex over switched phone lines. Data compression algorithms are used in devices from modems to multiplexers, and standalone. Protocol processing for meaningful communication is now commonly offloaded from computers by intelligent dedicated equipment.

Global Communication

International telecommunications facilities have been in place for some time and carry large quantities of data. Services such as Telex, TWX and facsimile are not new, but the equipment is faster, does more of its own processing and can often diagnose transmission problems. More satellite transponders and undersea cables are linking continents.

Perhaps most interesting is the prospect of a unified global communications facility carrying all types of signals. Integrated Services Digital Network, or ISDN, is such a system. Standards and proposals for ISDN are being developed by the CCITT, and are close enough that many communications equipment and semiconductor manufacturers have begun development of products that will serve in this system.

ISDN is designed to be a digital facility capable of carrying not only data, but also video and voice signals throughout the world. In this way, it is a pipeline for transmission of any kind.

As one of the only nations in which communications are not government-controlled, the US view of this global facility is somewhat at odds with other countries'. The basic proposal outside of the US would standardize not only the physical links, but also the control and monitoring of the facility. Standardizing more levels of the system would better assure consistency and meaningful communication.

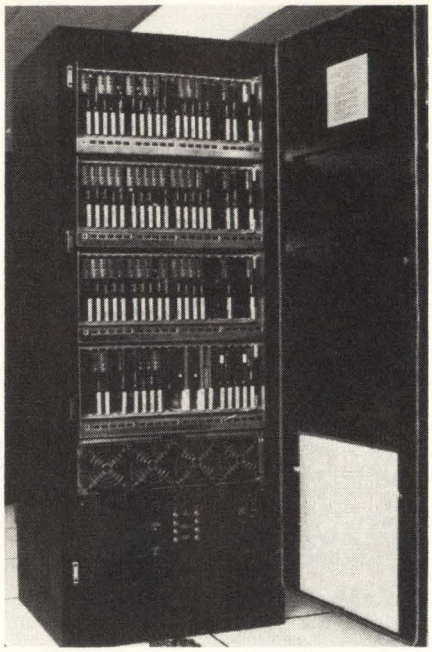

Figure 3: AT&T's Datakit network uses modules that slide into a card cage; each card can handle a separate kind of communication.

PTT (Postal, Telegraph and Telephone) agencies of most governments could agree on such regulation of the facility. Since communications are not state-run in the US and are more decentralized with the forced breakup of AT&T, it would not be easy to come to an agreement. The current Administration's support of industry forces may make designating a controlling body particularly distasteful.

Nevertheless, a physical connection that could permit mixing of many types

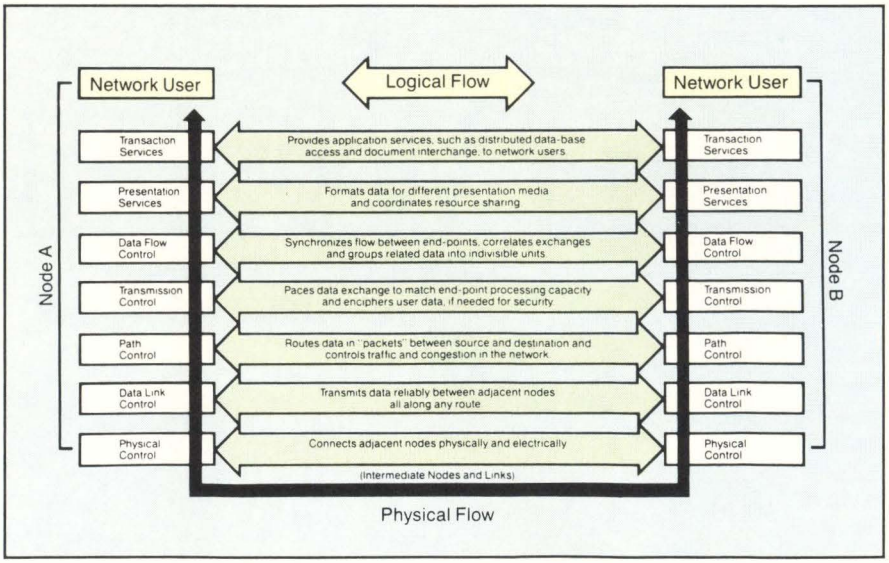

Figure 4: IBM's SNA (Systems Network Architecture) is based on seven levels, like the ISO Open Systems Interconnect (OSI) model.

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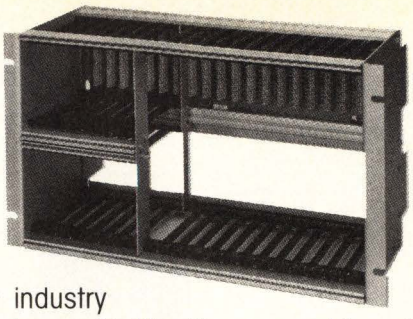

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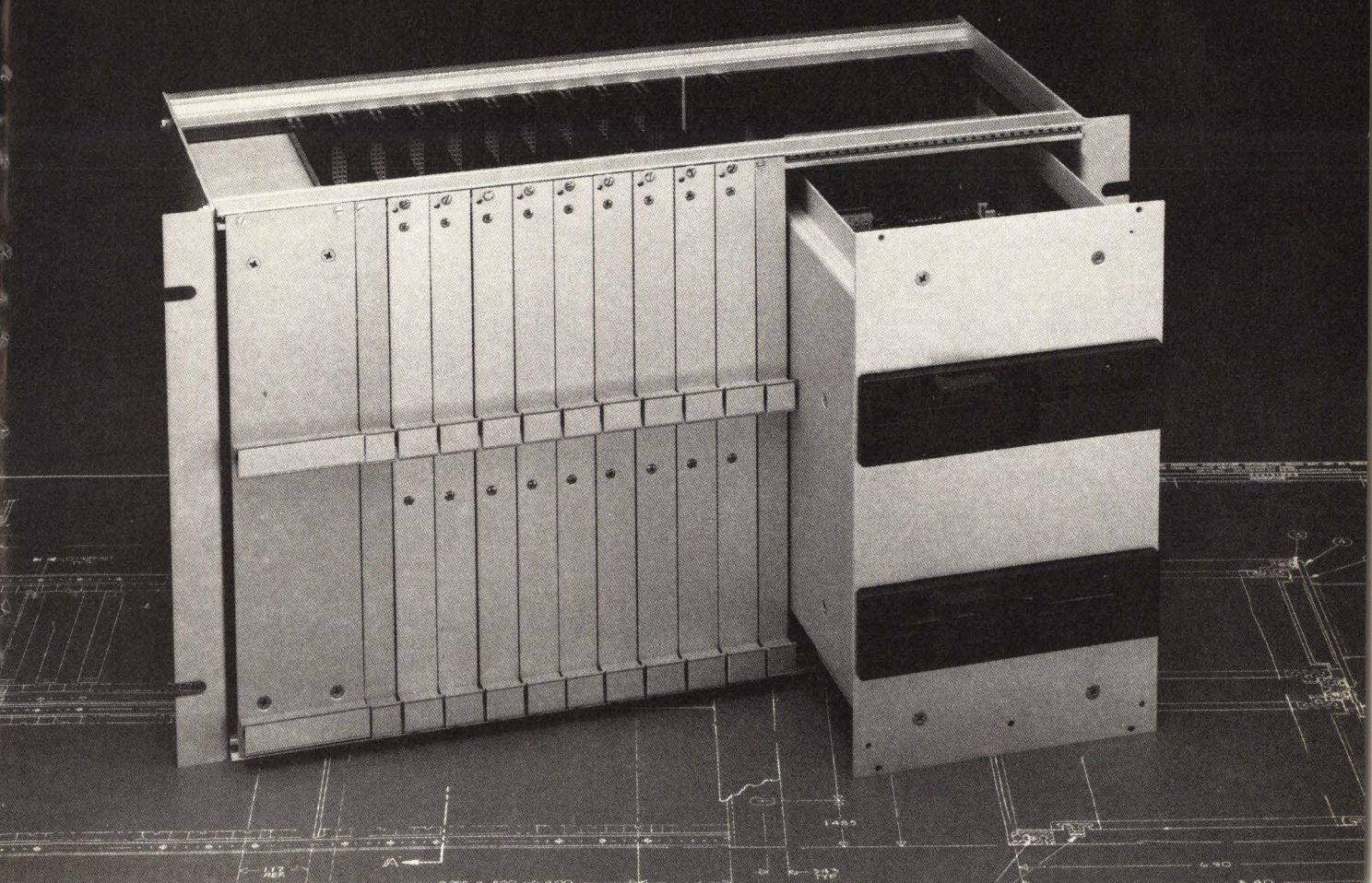

of transmission on a global basis is the goal. Though not all levels have been standardized, silicon and device support are in place.

Multiservice Devices

Mixing several types of communication signals on one transmission system is not limited to global networks. From local to wide area, products are appearing to allow efficiency through combining functions.

One advantage of the Sytek (Mountain View, CA) LAN that IBM recently chose is that it uses broadband cable, like CATV. The ability to send both video and data over one cable is important in many environments; GE's networking scheme, supplied by Concord Data Systems (Waltham, MA) also uses broadband facilities that are common in industrial environments.

The sharing of voice and data lines is practical with digital telecommunications equipment. There may be disadvantages, however, to using a voice PBX for computer networking. Including analog circuitry for audio functions can be costly, and large organizations may need higher speeds. If not combined, devices designed for data transmission and switching, as those for voice only, can be optimized.

Yet other areas are opening up under the ongoing deregulation of communications in the US. Space in radio bands once reserved to assure separation of channels has been freed for other uses in some cases. And the reverse channels used in standard ack/nak transmission schemes may also stand open when a backward channel is integrated by the transmission equipment.

Whether data will be transmitted over such channels is not yet clear. But as the amount of computer-based data generated and distributed for manipulation increases, extra options could become critical.

Combined Forces

Just as VLSI technology profoundly changes the configuration of computer systems month-to-month, it is impacting communications equipment. Smaller packages, more sophisticated and extensive functions and diagnostics and higher performance in products that often cost less than predecessors are trends for both computers and communications.

The entry of AT&T into the computer market and IBM's increasing presence in communications industries have profound effects on markets and products in those areas. Devices to hook into IBM's SNA and SDLC networks, as well as DEC's Network Architecture continue to be important. AT&T has so far dominated their own market, but that could change. The 3B line has been added to the roster of computers for which a version of BLAST file transfer/terminal access software has been released by Communications Research (Baton Rouge, LA). And the giants are not the only harbingers of the merging of the two fields.

Figure 5: DECtalk is a voice communications desktop computing system.

Although ICs for communications functions are increasingly common components in computer-based systems, communications vendors will not likely be pushed out of the market altogether. Some will focus on OEM products and provide expertise to systems manufacturers.

Many others will concentrate on software products: hardware to move digital pulses from one device to another, no matter how sophisticated, is of little use if the information arrives in a form unintelligible to the receiving device. This problem has plagued not only LAN, but also terminal and wide area net users. Protocol software and code for interconnecting various networks is difficult to produce, and specialists in communication are the most likely source.

Layered network interconnection is not new; the 10-year-old SNA has a seven-level architecture (**Figure 4**). But for standard networks to link many vendors' products, all levels of a communications network must be specified and implemented. Those involved in all levels of networking have often spent great effort on optimizing hardware designs, only to realize that the higher, software-dependent communications layers slow transmission to unacceptable speeds.

As the number of lines and their speed increases, servers that provide communication processing are critical. File servers, print servers, disk servers, network servers and other dedicated machines in networks allow nodes with integral communications to operate efficiently. Front-end data protocol processing to keep computer equipment running at full performance is slowly being accepted as a requirement.

Benefits of increasingly sophisticated communications ICs belong not only to the semiconductor manufacturers, but also to system integrators, computer manufacturers and communication equipment manufacturers. An even greater impact will be on users, and on the corporate structure.

As reliable data networking becomes common, computer systems' processing power can be dedicated to one task, with other functions accessed across the network. Complex databases will not need to occupy large storage spaces on many systems. Through transparent access to other special-function machines, each can run efficiently, yet act as a general-purpose computer. And LSI and VLSI for communication will allow the capacities of integrated transmission facilities to keep up with advances in computer and processor performance. DD

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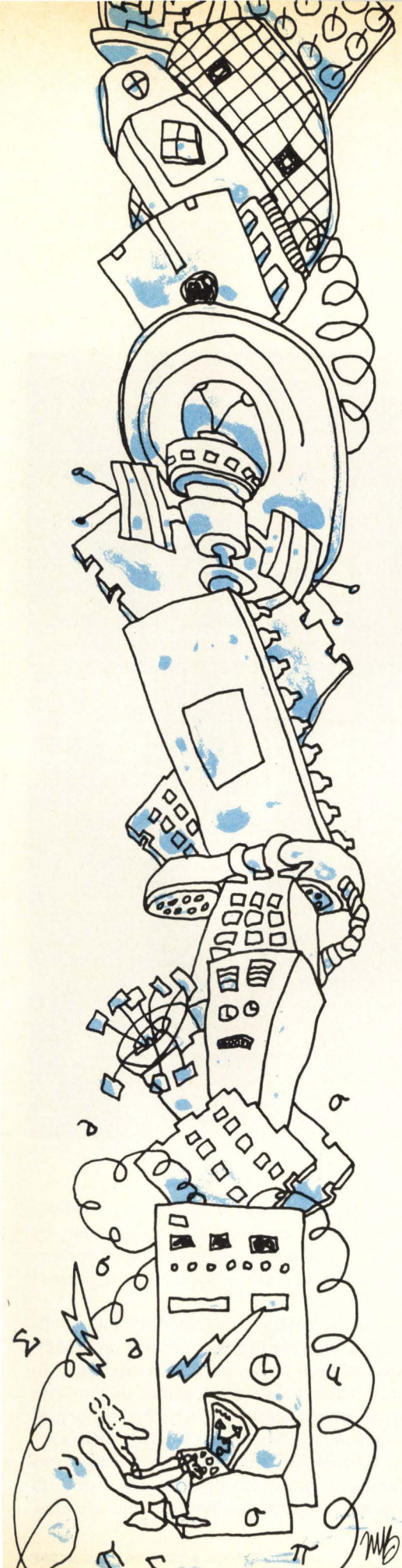

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Designer's Guide To The VME Bus

by David Wilson, Executive Editor

A recent market study by Motorola has predicted that the total size of the 16/32-bit microcomputer board market may be as large as 2.23 billion dollars by 1988. Other figures from Dataquest indicate that close to 40% of that market will be in the area of industrial automation. Clearly, this is a market that the Multibus has penetrated already to a great extent. The wide range of products available on the bus is possibly *the* most important consideration in that environment and has led to the bus' phenomenal success.

Like most other marketplaces, the push toward higher performance systems is now evident in the industrial automation world. Inevitably, 32-bit buses have emerged to provide a solution to the systems architect looking to upgrade. Of the two contenders in the 32-bit bus market, Intel (with the Multibus II) and the Motorola/Mostek/Signetics consortium (with the VME system), the only product available at the time of this writing is for the VME bus. Intel plans to announce Multibus II products in February 1985 and the backing they have received from the number of second party Multibus manufacturers will undoubtedly make them a viable competitor to the VME. When the Multibus II products are announced it is highly unlikely that they will support unsolicited data messages and sequential transfers, however, due to the complexity of the bus interface logic and the size of the card.

The battle for the 32-bit marketplace will not be won overnight, especially considering that few 32-bit processors have yet to be designed onto any commercially available board level product. Also, the much rumored BI bus has yet to emerge from DEC. With many systems people currently switching from PDP-11 to VME systems, it is most likely that DEC will soon react with some impressive VAX- or PDP-based Eurocard format.

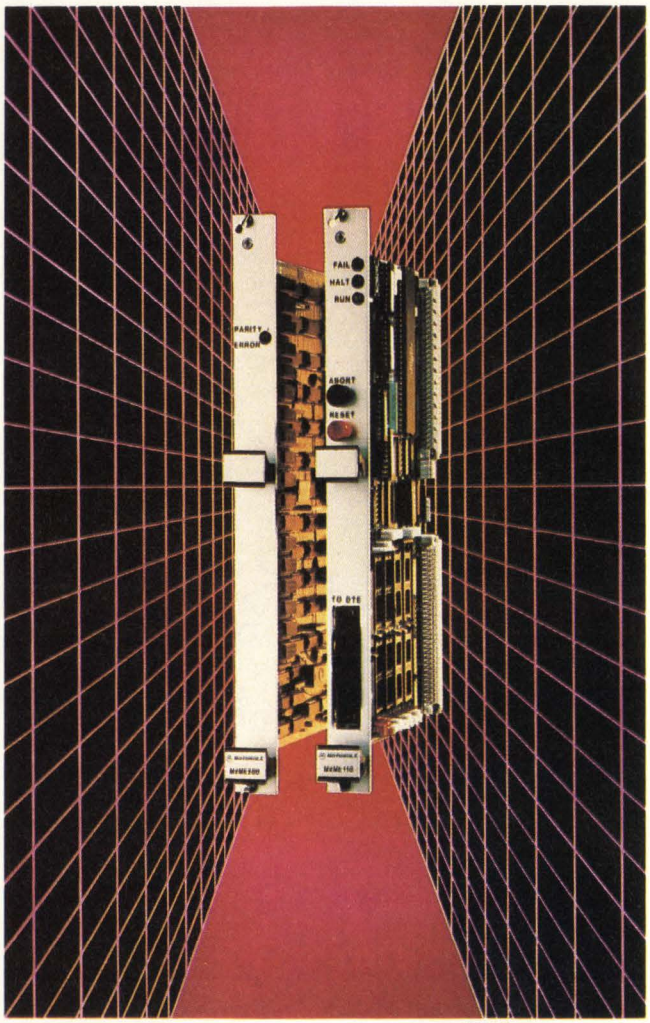


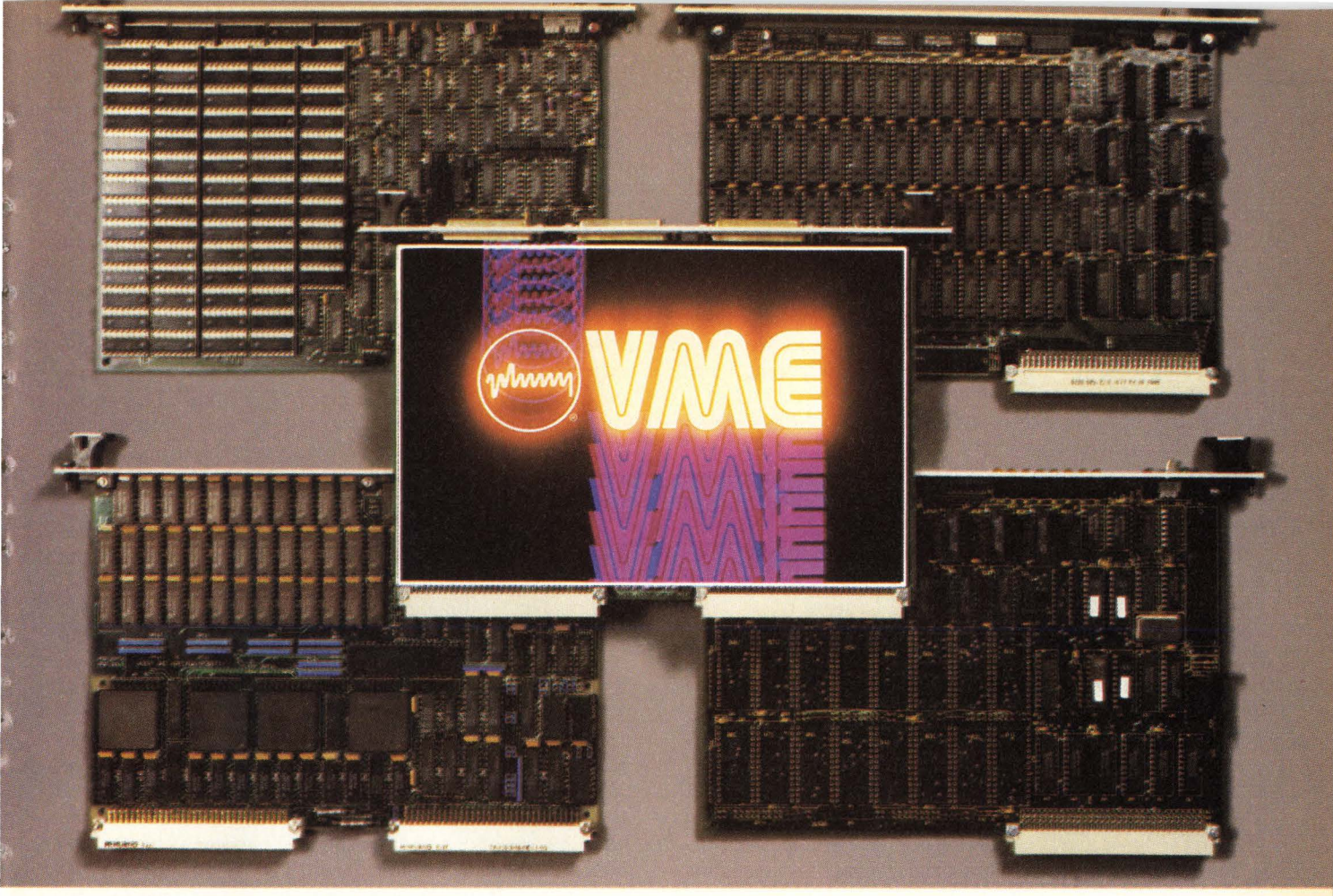
PHOTO COURTESY MOTOROLA

The VME Architecture

The VME system architecture is really a combination of three different buses – the VME, the VMX and the VMS. The VME bus itself provides the backbone for the VME architecture. It has a data path that allows the systems integrator to mix 8-, 16-, and 32-bit processors in the VME bus backplane. A master/slave asynchronous, non-multiplexed data structure, the VME supports seven levels of priority interrupt, four levels of data bus arbitration, and multiple master support as well as fault-detection and control and special transfer cycles.

A second member of the VME system architecture is the VMX bus, a parallel bus designed in response to the needs of multiprocessing applications. The VMX bus is a private-access subsystem bus that utilizes a 32-bit address path with a 16-Mbyte address range. VME extends the processor boards features by permitting it to access additional memory, I/O and other functions without the arbitration overhead typically encountered over the global VME bus.

Another member of the VME system is the VMS bus, a self-arbitrating high-speed serial bus that facilitates the rapid communciation of brief messages between system components. To determine resources between system processors, the two wire VMS bus rapidly communicates messages such as pointer information, interrupts and test bits. It also supports such functions as intelligent semaphores, broadcasting and simultaneous polling. One other application of the VMS bus has to do with diagnostics and the implementation of fault tolerant schemes.



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2 Mbyte DRAM	PME 048D	•		8/16	190	300
1 Mbyte DRAM*	PME 512EP	•		8/16/32	150	270
3/4 Mbyte DRAM	PME 256EA		•	8/16/32	150	300
512 Kbyte DRAM	PME 012D	•		8/16	190	300
512 Kbyte EPROM or ROM; 128 Kbytes SRAM	PME CRR-1†			8/16	User Adjustable	
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If a defective board is detected, a message can be sent over the VMS bus to instruct the faulty unit to reset and isolate itself from the global VME bus. This ability is particularly critical in cases when the fault disables the main system bus.

One of the main complaints about the VME bus architecture, even from the early days, was that the Eurocard form factor (double Eurocard 233.3 × 160mm) would not be large enough to support the sort of functions the designer might wish to place on a card. Today, however, a number of VLSI devices are or will be available to help out with the implementation of the VME Spec (**Figure 1**).

The MC68153 Bus Interrupt Module (BIM) for example is designed to serve as an interrupt requester for peripheral devices. Up to four independent devices can be interfaced to the system bus by the port. Intended for asynchronous master/ slave bus operation, the BIM is compatible with Versabus, VMEbus and the 68000 device bus. **Figure 3** shows a typical configuration. Here, three bus slaves are connected to the system data bus. Each of these devices could be parallel I/O, serial I/O or some other function. An interrupt request from any device is routed to the MC68153 and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the BIM can answer by supplying an interrupt vector and handling all timing. Another part, the Bus Arbitration Module (BAM), is a bipolar asynchronous bus controller which allows multiple local MPU buses to be multiplexed onto a common global bus enabling the local buses to share memory and I/O devices and to communicate with each other.

Figure 4 shows the BAM circuit in a local configuration. Here, the BAM serves as the central bus controller as opposed to the distributed control of a daisy chain arbitration scheme. As shown, the BAM provides the interface between the local bus masters and the MC68000 MPU. The bus request-bus grant BR-BG pair of each local bus master connects directly to the DBRn-DBGn pair of the BAM. The BR-BG pair of the processor connects directly to the BR-BG pair of the BAM.

Alternatively, the BAM may be used in a moderately coupled multiprocessor system. In this case, the BAM serves as the central bus controller of the shared global bus. This allows multiple local buses to share mass storage and the addition of the more local processors to increase system throughput. These two parts, developed at Motorola, form only part of the effort aimed at producing support chips for the bus.

Underway at Signetics is an effort aimed at producing no less than seven more parts for interfacing not only to the VME but to the VMS bus as well. These include the 68154 and 68155 Interrupt Generator and Interrupt Handler and the 68172 master/slave interface to the bus. The 172 may be used most obviously in DMA control where the DMA controller can serve as the VME master in normal operation yet must act as the VME bus slave when programmed by an offboard processor.

Currently in development, Signetics' ABAM or 68174 is an advanced bus arbitration module that can support both the VME and the Versabus. It can support two types of arbitration, round-robin and priority. This can be done simply by changing selections on the chip. The part can drive the bus directly without the requirement of TTL logic between the chip and the bus. But perhaps the most interesting aspect of the

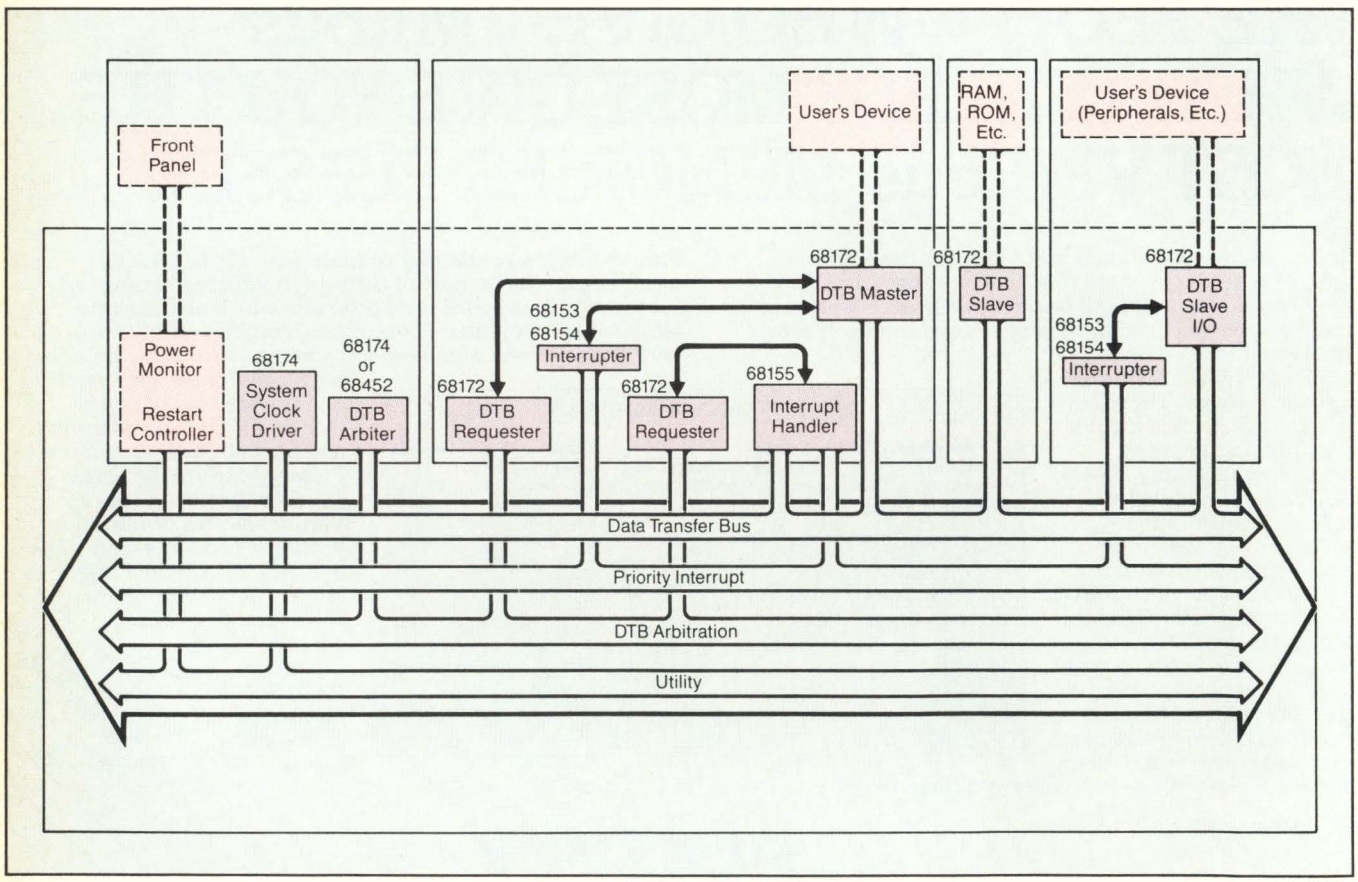
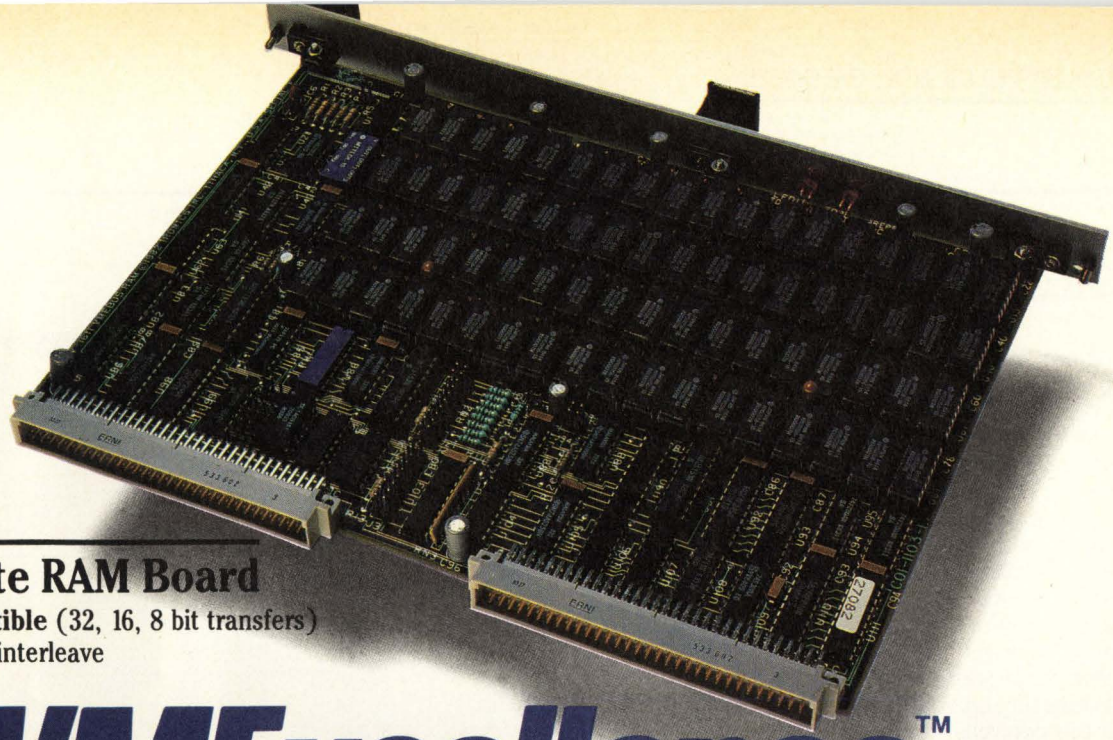


Figure 1: Area defined by VME bus specification.



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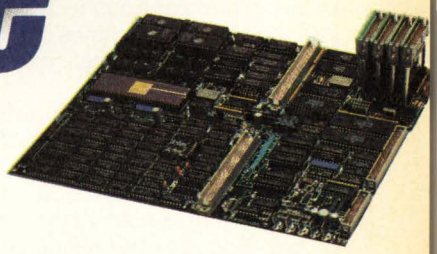

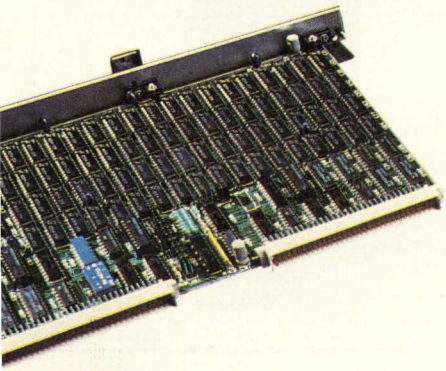

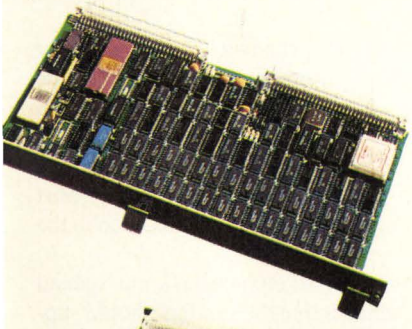

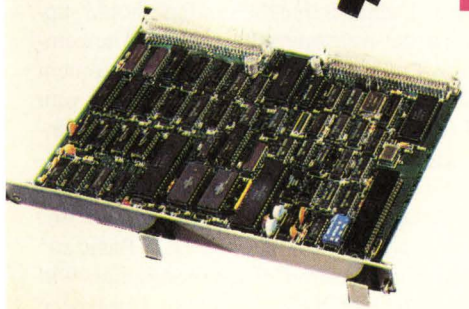

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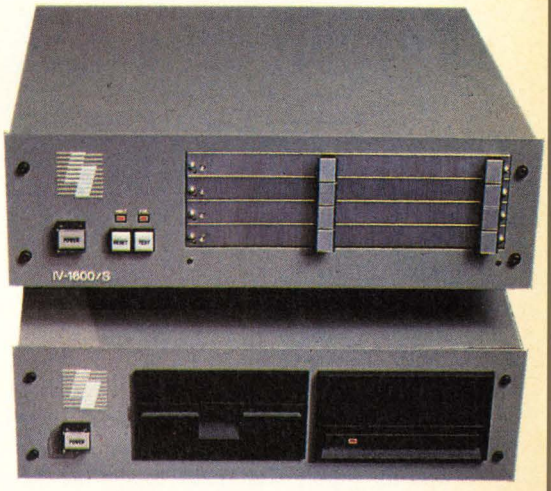

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VMEbus Disk Controller

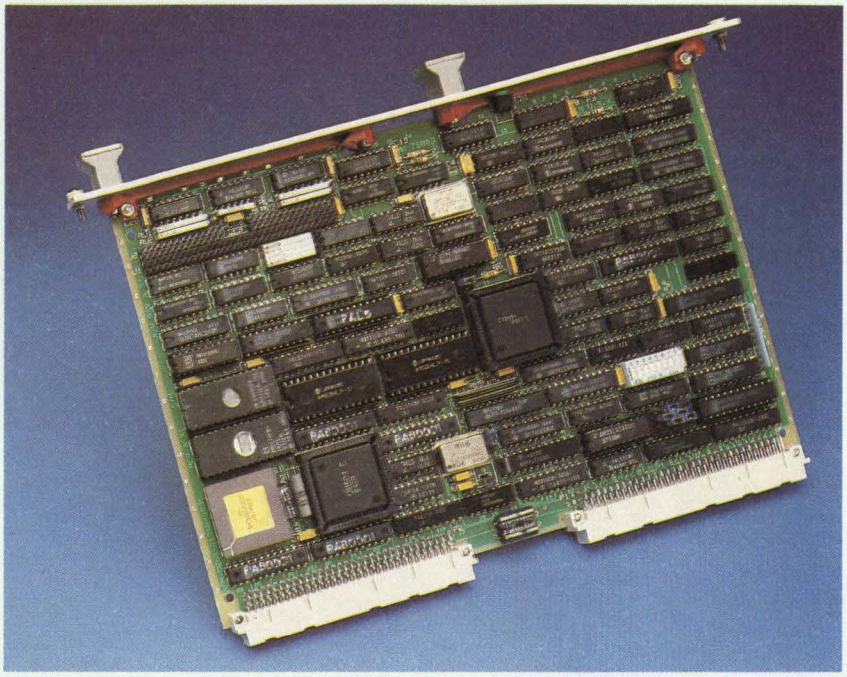
A VME-based SMD disk controller, the 3200, was developed jointly by Interphase (Dallas, TX) and United Technologies Mostek (Carrolton, TX) and is based on the Motorola MC68000 microprocessor. The controller implements a "virtual buffering" architecture, whereby the 68000 controls 12 Kbytes of buffer space that it allocates and de-allocates to various devices.

The buffers also enable the controller to implement an intelligent caching scheme for higher throughput than achieved using unaided 1:1 interleave. Once the controller has completed a read operation and transferred requested data, it will continue to read sequential data into the cache. Two high speed bipolar state machines control disk-to-bus and bus-to-operating system transactions.

To accomplish zero latency, the V/SMD 3200, like the Interphase Storage Multibus controller, (*Digital Design*, August 1984, p. 34) allows the drive to begin read as soon as the track is located. Because the 68000 serves as a gatekeeper to dynamically allocate and de-allocate the "pool" of virtual buffers, data can be transferred out of order across the bus and into the correct location in system memory beginning with any sector of interest in the track.

The V/SMD 3200 also allows programmable sector and gap sizes, interleave factor, number of sectors per track, and number of heads per unit. The V/SMD's software interface is also compatible with Interphase's Multibus SMD controllers, the SMD 2181 and 2190. Drivers for those products can be used for the V/SMD 3200 with only minor modification. Available for shipment in December, the V/SMD 3200 has a single-piece price of $2,750.

Interphase **Circle 300**
Mostek **Circle 301**



The V/SMD 3200 disk controller's multitasking architecture allows for simultaneous disk and bus activity.

Signetics developments are the 171 and 172 chip set that provide an interface to the VMS bus. While the 173 takes care of the data protocol, the 171 manages the upper levels above the data link layer.

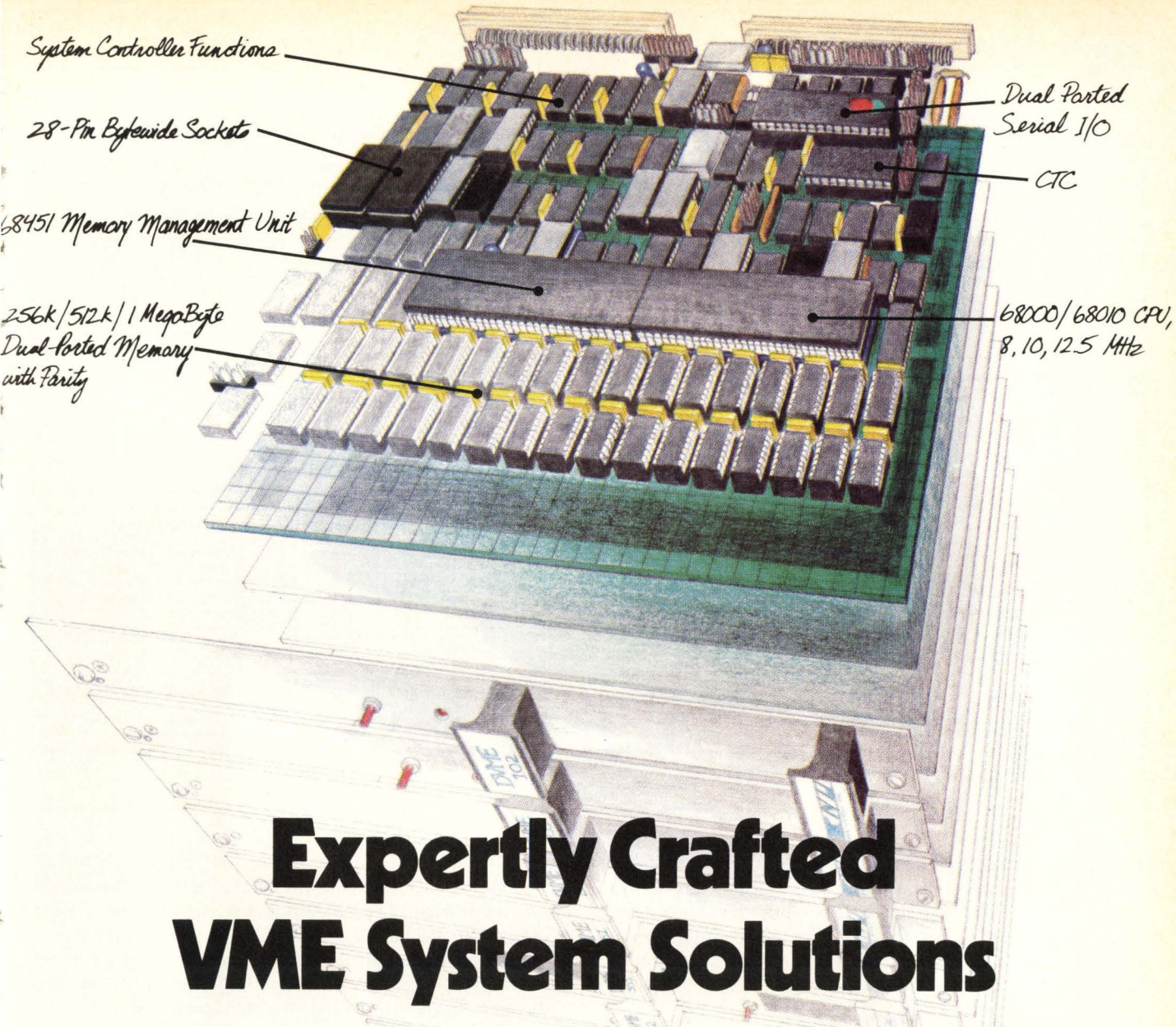
All of the above devices will undoubtedly provide the designer with more cost effective means with which to implement a VME board. More importantly, those systems architects who inevitably find that a totally off-the-shelf hardware implementation is impractical will find it easier to build their own custom board.

Building on the availability of the 32-bit micro and supporting interface chips for the bus, the impetus for the VME bus has grown. The two current leaders in the marketplace, Force Computer and Motorola, have seen competition coming thick and fast. Earlier this year Force entered into a second source agreement with Plessey. Charles River Data came into the market offering not only systems but board level products too.

Others are carving out more specialized niches. Burr-Brown, for example, is targeting its efforts towards Digital Signal Processing. Xycom is continuing to emphasize intelligent I/O. One of the first processor cards to support a true 32-bit processor has been announced from Elite Computer Systems. Called the E82/ CPU2, it is based on National Semiconductor's 32032 and includes the floating point processor, memory management unit, real-time clock and 32 Kbytes of cache memory. Although Elite offers a system level product that will eventually port UNIX also, the majority of sales at the moment has been in the board business.

That big industrial automation marketplace has some special demands – not the least of which is that the vendors should support their product with a real-time operating system. The competition comes from two industry giants; Digital Equipment Corp. and Intel. Those customers, however, who cannot wait for these companies to deliver 32-bit processing power must inevitably turn to a smaller vendor who can complement hardware with a comparable operating system.

Force Computer, for example, offers PDOS. At present two high level languages are available with PDOS, PDOS Basic and PDOS Pascal. In addition both Fortran 77 and C compilers will be available in 1985. Both the PDOS Basic and Pascal have been



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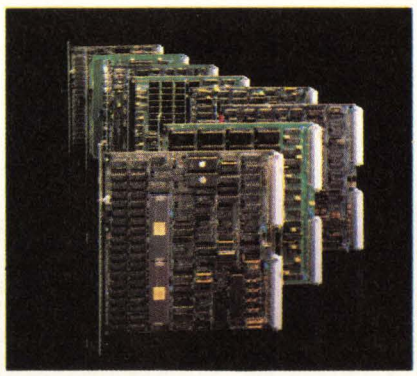
DY-4's commitment to R&D is reflected in its continuing new VME product development, including intelligent communications controllers, SMD/ESMD controllers and 9-track tape controllers. DY-4's VME series currently includes:

DSM-*6816* – a UNIX based development system.

DVME-*102* – 68000/68010 CPU with MMU, dual-ported serial I/O and 256K/512K/1Mbyte DRAM.



DVME-*105* – 68000/68010 CPU with dual-ported serial I/O and 14 bytewide sockets.

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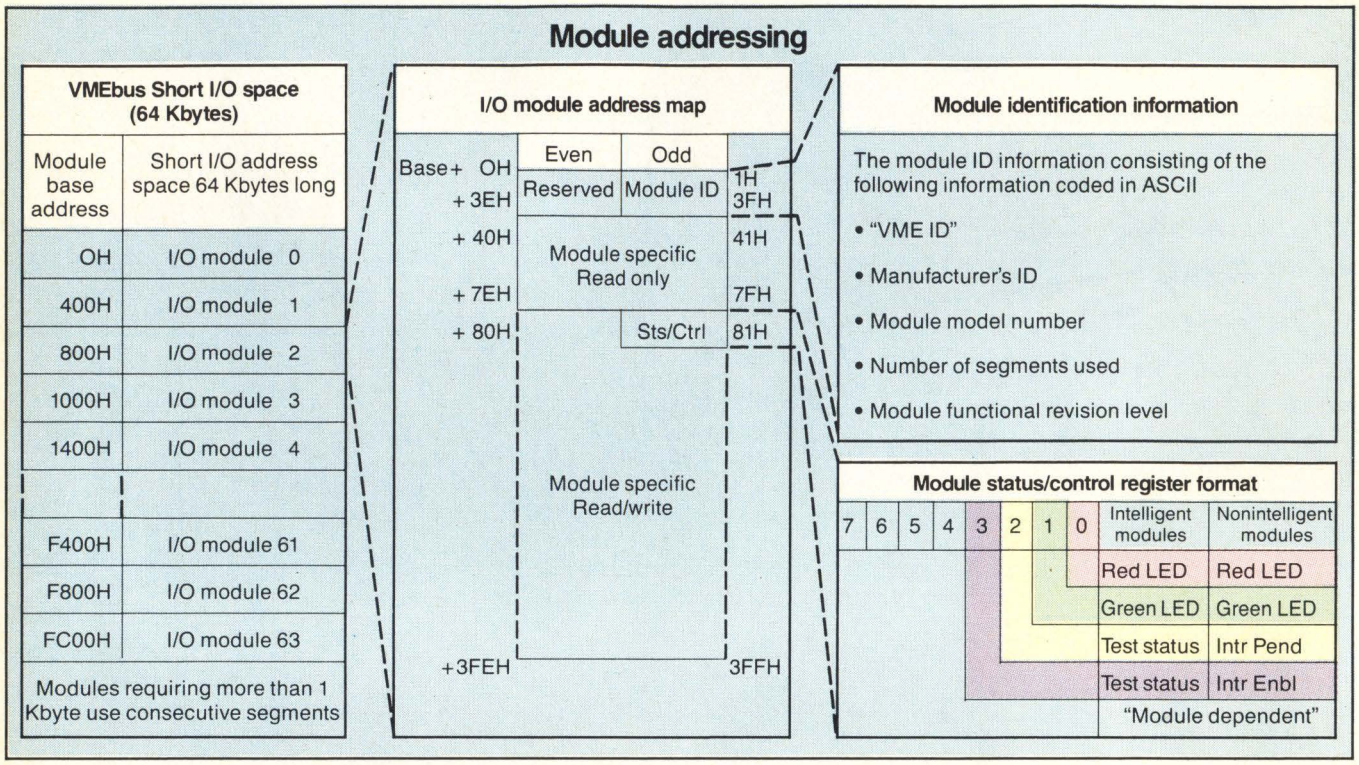

Figure 2: Elements of Xycom's standard I/O architecture.

extended to handle real-time operations and multitasking support. Elite, on the other hand, offers ECS PVS, a virtual storage operating system supporting real-time and multiple processor environments. Other features offered by the operating system include demand paged virtual memory, multiuser and multitasking operations.

Supporting The VMX, VMS

Support for the VMS bus is a moot point for board manufacturers due to the lack of available silicon from Signetics. However, chips are expected out in the early part of next year that should solve the problem. The VMX, however, is another story. Data Sud Systems announced in April this year a 68000/68010 processor board that was developed for large contractor, CERN in Geneva. Support of the VMX bus will allow the card to operate in conjunction with the company's high speed 128K and 256K static RAM cards.

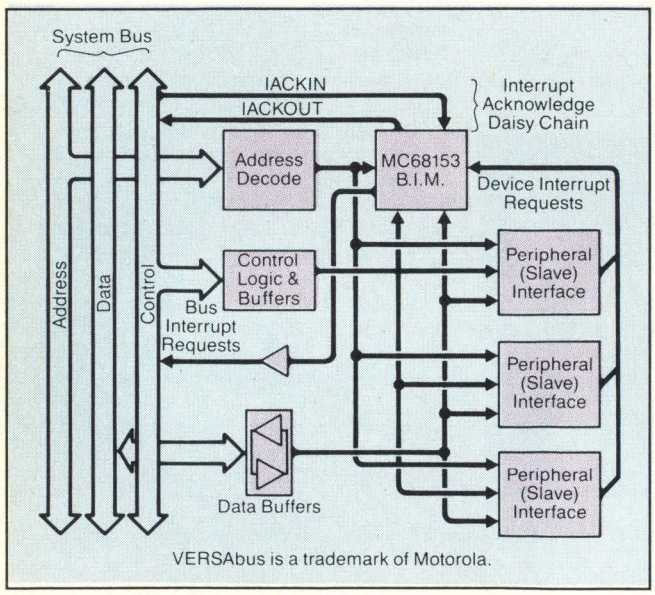

Figure 3: MC68153 system block diagram.

Like most buses, however, the system integrator should be aware that the VMX is currently undergoing revisions. And it is likely that the new specification will not be compatible with the old one. The revised spec will probably add a number of interrupt lines that will add to the performance of the VME architecture. However, it will lead to VMX Rev A and VMX Rev B boards appearing in the field that will not be compatible.

To accomplish a goal of developing a mechanism to validate system configuration, hardware must provide software accessible data on each module in order to indicate the type of module and its functional revision level. The systems initialization S/W must read this data and ensure that each required module is installed and that the modules are all of the current revision level; i.e., no one has installed an old spare module that is incapable of performing satisfactorily. The task of writing system software to implement this capability is simplified when the hardware conforms to a standard interface description. So far, the only published standard I/O interface for VME bus products has been proposed by Xycom.

The basic elements of Xycom's Standard I/O architecture are shown in **Figure 2**. It has already been implemented on a whole range of Xycom VME bus modules and has been proposed to the VME manufacturing group as the basis for an industry wide

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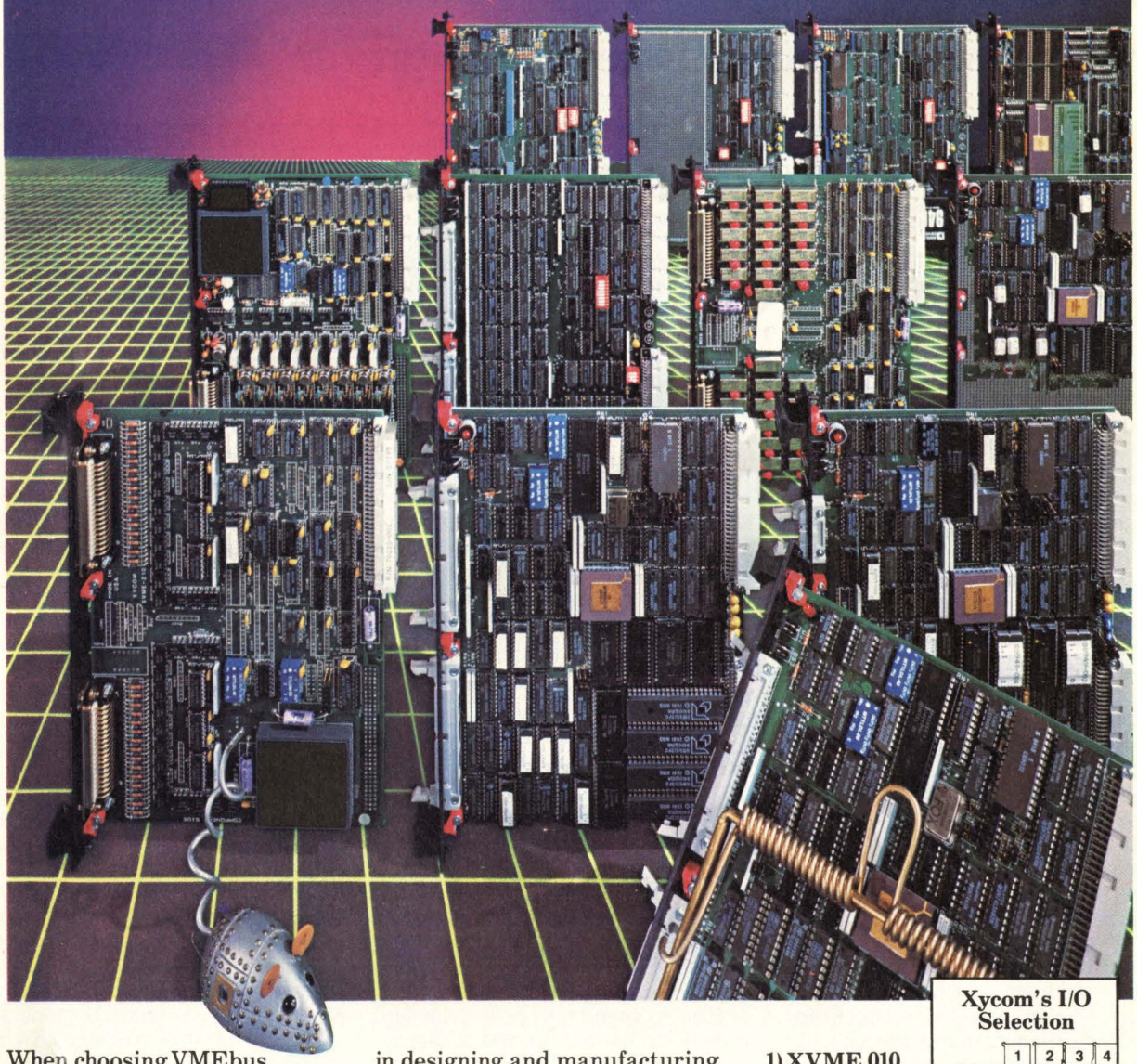

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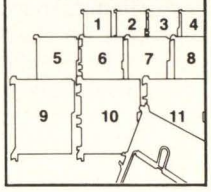

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Industrial VMEbus System Design

Most systems can be classified into one of three categories based on the number of processors employed and on the division of tasks among processors. The first category is the single processor system. In this approach all of the I/O and data processing tasks are performed by one processor. The second category utilizes multiple processors in a distributed intelligent I/O configuration. A single processor acts as the system "master" and handles the data processing at the highest level of abstraction. I/O functions (such as scanning inputs for state changes, linearizing thermocouple inputs, minor loop control systems, operator display formatting, etc.) are performed by dedicated I/O processors. The third architectural category is multiprocessor systems, in which multiple processors are used, but the tasks performed by each are determined dynamically rather than being fixed in advance, taking the distributed intelligent I/O approach. The multi-level bus arbitration and real-time interrupt facilities provided by the VMEbus make it compatible with all three system architectures.

As **Figure 1** shows, a broad range of applications can be handled by any of the architectures. To choose one it is necessary to weigh the time (and cost) required to develop the system with the cost of the final system. In addition, the choice is constrained by the nature of the application. Not even the 68000 processor can handle the total processing requirements for some systems. In those cases one of the multiple processor architectures must be selected. Applications which have I/O functions that can be readily partitioned into separate tasks or I/O functions which require real-time response are most suitable for the distributed intelligent I/O approach. On the other hand, when the I/O workload varies dramatically over time, the increased processor efficiency of the multiprocessing architecture is more appropriate.

1) As part of the system initialization Processors #1 and #2 agree on the location of their common control block
2) Processor #1 sets up a control block in RAM that is available to both processors
3) Processor #1 sends an interrupt to Processor #2 to indicate that the control block is prepared
4) Processor #2 performs the requested operation and sets the response word in the control block to the appropriate value
5) Processor #2 sends an interrupt to Processor #1 to indicate that the task is complete and the response word is valid

Table 1: A typical IPC protocol communications sequence.

In multiple processor systems (both distributed intelligent I/O and multiprocessing) one issue that must be addressed is the communication of information from one processor to another. In general, information is passed in some memory that is accessible to both processors. The key problem is to find a mechanism to notify each processor when a block of data is available. One technique is to have each processor poll flags set by the other processors. This technique works but it is inefficient in several respects. First, it requires processors to spend time polling the flag even when there is no data available. Second, the polling activity can use a significant portion of the bus bandwidth without accomplishing any actual work. To avoid these problems an interrupt driven notification mechanism is usually preferred.

To implement an interrupt driven mechanism it is necessary that all processors be able both to receive and to send interrupts. The reception of interrupts is not a problem since most commercially available VMEbus processor modules have that capability. Most processor-based I/O modules are capable of generating interrupts, but general purpose CPU modules are not. To avoid the unnecessary cost of having interrupt generation circuitry on every CPU module, some system controllers have a global interrupter circuit that allows any CPU module to send an interrupt to any other CPU module. Using a global interrupter circuit can be a system bottleneck if the circuit can handle only one or two pending interrupts at a time. A full global interrupter can have as many as 49 interrupts pending at one time, thus eliminating any potential bottleneck.

Another difficulty in designing a mechanism that allows processors to communicate with each other is the definition of the command structure and the protocol that each procesor must follow to ensure unambiguous message hand-

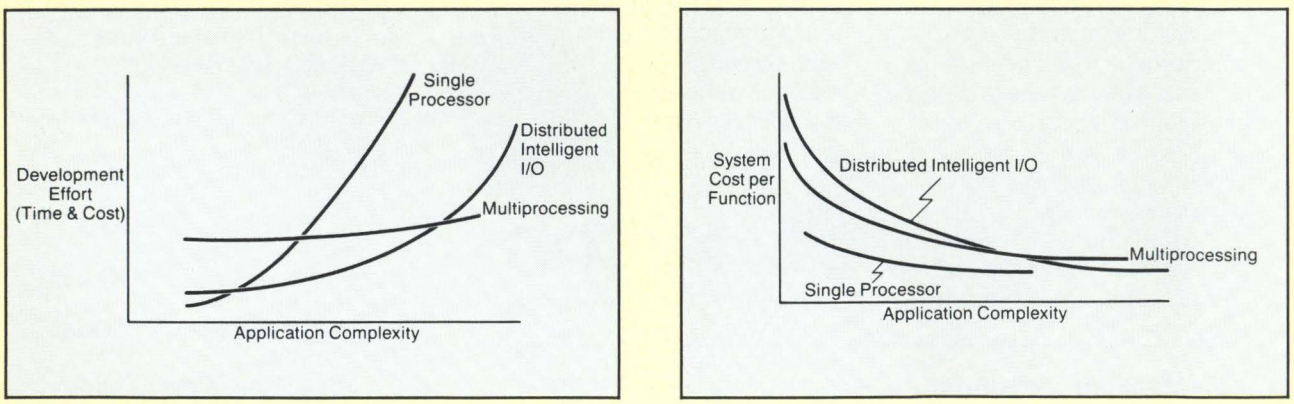
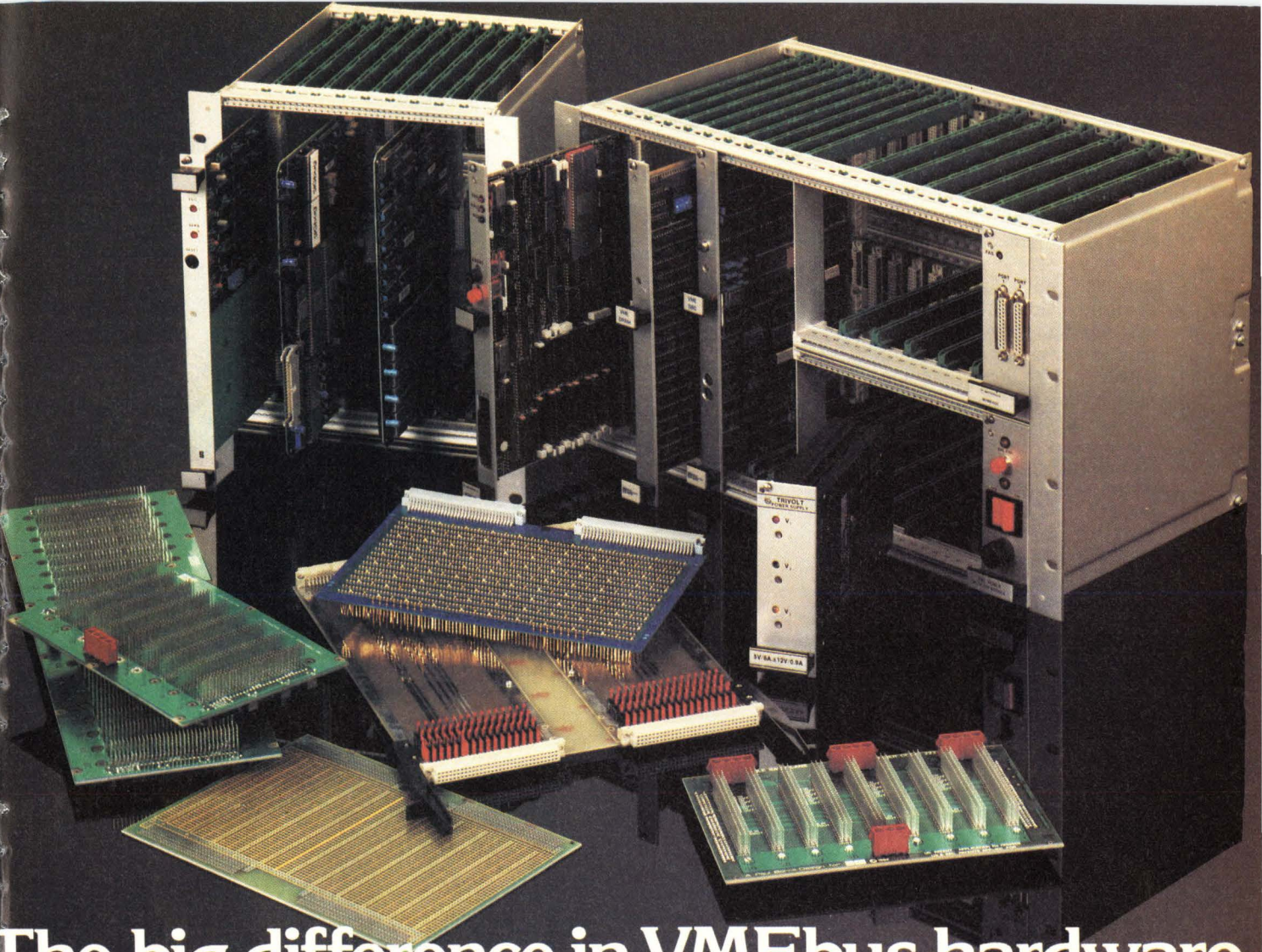


Figure 1: Hardware architecture alternatives.



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ling. A good protocol ought to be general purpose enough to be used for the majority of applications but it should also be simple enough to be implemented quickly and reliably, while including some provision for extension. It should not impose more constraints on the hardware or system design than are absolutely necessary. Developing a protocol from scratch is possible, but adopting a standard protocol will speed the system development and minimize the probability of protocol errors. The use of a standard protocol will also allow the use of off-the-shelf hardware and software for some system components. One standard protocol developed expressly for use on VMEbus products is Xycom's IPC (Inter-Processor Communications) protocol.

In the IPC protocol the communication between any two processors is accomplished using control blocks which reside in memory locations accessible to both processors. **Figure 2** shows the structure of an IPC protocol control block. The information contained in the control block includes a command word to specify the nature of the requested activity; a response word to be filled in by the recipient of the control block to indicate the results of the requested activity; interrupt vector and level information for recipients to use in acknowledging receipt of the control block or completion of the activity; a link to subsequent control blocks to allow chaining of activities; and several locations for immediate operands.

Command Word		
Response Word		0 = successful ← non-zero = error
"Command Completed" interrupt level	"Command Completed" interrupt vector	
Response Flag	Next Command A/M Code	
Pointer to Next Command Block (2 Words)		← for command chaining
Command Parameters or Response Data (or pointer to data) (4 Words)		

Figure 2: IPC protocol control block (10 16-bitwords).

The IPC protocol was developed primarily to support the distributed intelligent I/O systems architecture, but it is also applicable to multiprocessor systems. It is pre-programmed into all of Xycom's Intelligent I/O modules (such as the XVME-420 Intelligent Peripheral Controller) and is running today in VMEbus systems.

Andy McMillan, Xycom, Inc.
Circle 302

standard. It provides the information required by the system software to perform configuration validation and it provides standard mechanisms for performing common I/O module control functions.

As mentioned earlier, one of the problems with designing a system based around off-the-shelf product is that often, especially in the industrial automation field, cards are not available that perfectly meet the design requirements. One answer to this may be to turn to a product that offers the ability to design and to prototype special purpose modules where some board space may be left empty to wirewrap prototype components.

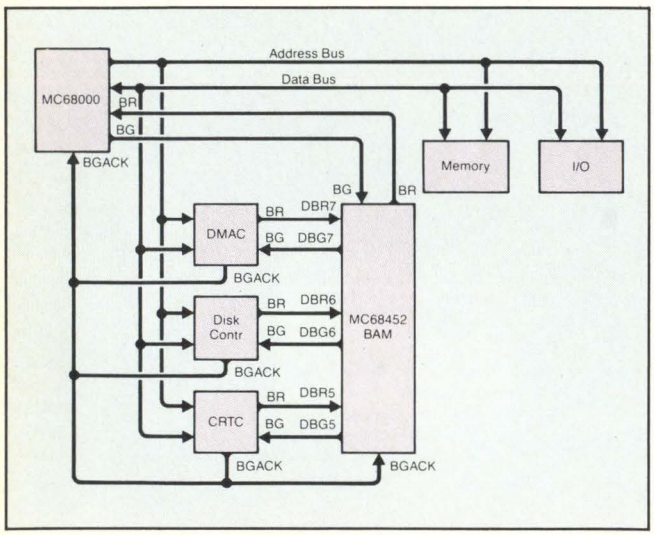

Figure 4: Local bus arbiter configuration.

Such a product is the Xycom X VME-080. The heart of the board is a 68000-based intelligent I/O kernal used in Xycom's intelligent I/O modules. This includes a 68000 MPU, clock, 16K dual access RAM, addressing decoding and VME master/slave interface circuitry. The local 68000 bus is brought to the prototyping grid and is available to prototype components. The kernal, which is designed to function as either master or slave, can cause VME bus interrupt on all seven levels with a programmable vector and can be jumpered to use any of the four arbitration levels for DTB access.

Conclusion

Undoubtedly, the introduction of the 32-bit 68020 and the associated VME bus support chips will provide more impetus for the VME bus. Many current 68020 high performance designs have implemented caching schemes external to the '20 itself that consume large amounts of board space. One can expect to see a greater use of SIPs for memory, gate arrays and VLSI control devices in next generation VME products. The obvious concern with the size constraint of the board and the investment necessary to meet product designs through innovative packaging techniques may serve as an indicator that future VME vendors will not simply be garage shop S-100 look-alikes. DD

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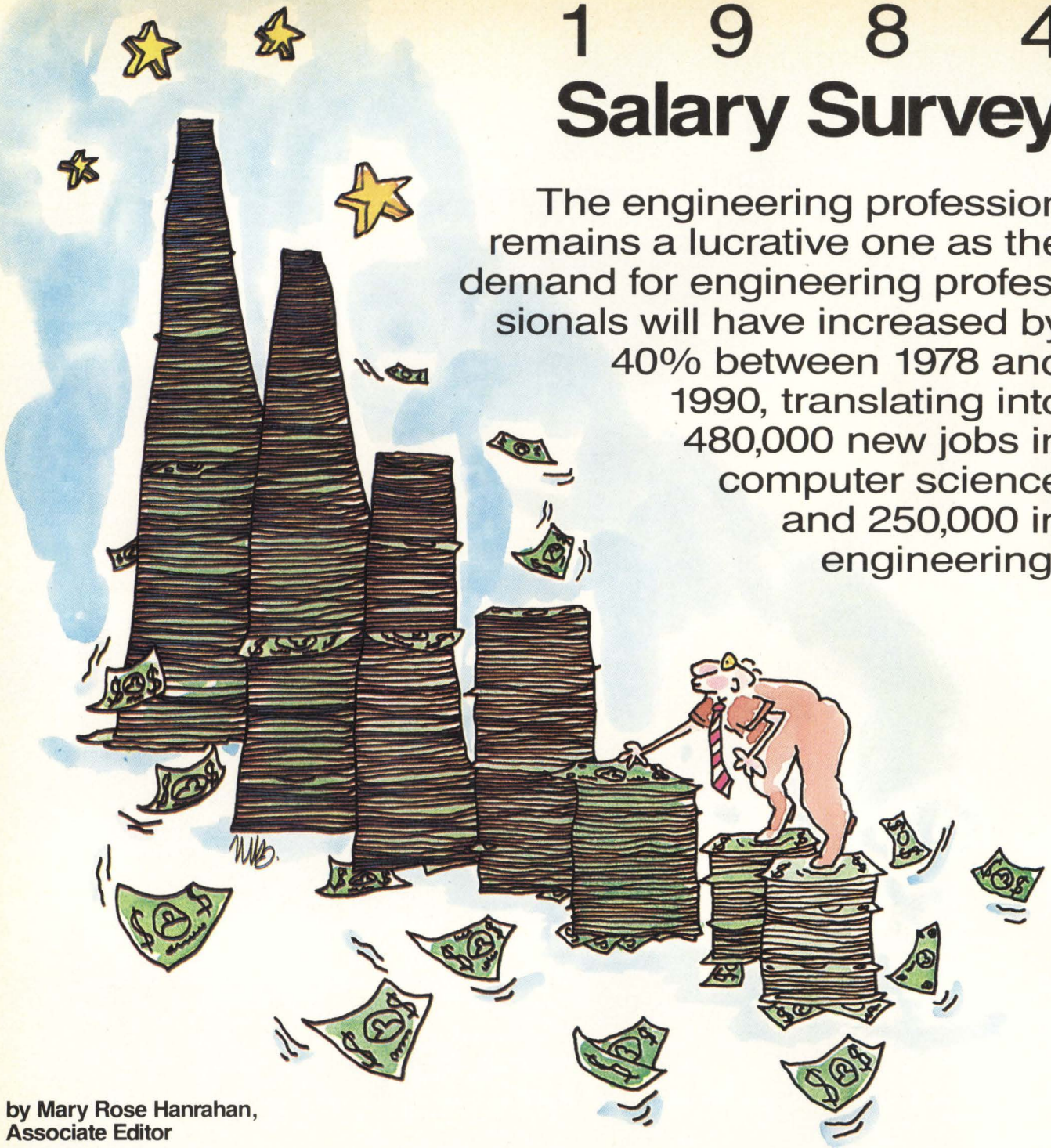
1984 Salary Survey



The engineering profession remains a lucrative one as the demand for engineering professionals will have increased by 40% between 1978 and 1990, translating into 480,000 new jobs in computer science and 250,000 in engineering.

by Mary Rose Hanrahan, Associate Editor

Digital Design's 1984 Salary Survey found the benefits of what is currently being termed "The Year of the Recovery" reflected in all aspects of the work environment. Last year's survey was characterized by those factors prevalent on the tail-wind of a recession—salary freezes, job lay-offs, and general employment malais. As reflected in this year's survey, the economy has rebounded and 89% of our survey participants received a salary increase in 1984. Amidst an economic landscape that has been radically altered by low inflation, deregulation, the strong dollar and new technology, prospects for the engineering profession remain bright. Unprecedented competition in the high technology industry at home and abroad is, however, drawing new attention to labor costs and the skimming of corporate payrolls necessitates a closer look at trends within the electronics engineering field.

Respondent Profile

From a total 2000 randomly selected readers surveyed, approximately 25% responded. These were composed of 48% engineering managers, 17% corporate managers, and 35% staff engineers. Most participants are involved in design and development engineering at a manufacturer that incorporates computer-related devices into their products as integrating OEMs, with over 500 employees in their division (**Table 1**). The participants' ages spanned from 25 to 55 years old and most respondents have a B.S.EE or higher. Of the 89% of participants that received a salary increase, 65% received a 5-10% increase. Of the 482 total survey respondents, only three females participated, rendering gender statistics invalid.

Roughly one third or 33.1% of the total respondents have a current annualized

Respondent Profile	Total Survey Respondents: 482	
Who they are:	**% of Respondents:**	**Average Salary:**
Engineering Managers	48%	$44.7K
Corporate and General Managers	17%	$42.5K
Staff Engineers	35%	$36.6K
Where they work:		
Manufacturer of Computers	3%	
Computer Systems Integrator (Systems House, VAR, Turnkey System)	16%	
Integrating OEMs	42%	
Manufacturer of Computer-related Peripherals	4%	
Large-Volume End Users	18%	
Government and Military	5%	
Public Institutions, Universities	1%	
Scientific R&D	2%	
System Consultants/Software Houses	2%	
Other	7%	

Table 1: 1984 Salary Survey respondent profile.

salary of $50K or more, and 25% make between $41K and $50K. Of the remaining 42%, 16% are in the salary range of $36K to $40K, 13.3% are in the $31K to $35K range, 8% are in the $26K to $30K range, and 5% are making under $20K.

Our survey profile, consisting mainly of engineering managers, found an average salary of $44.7K for those in that job function area. Corporate and general managers averaged $42.5K in annualized salary, but they comprised only 17% of the total participants. Staff engineers, making up 35% of the total, averaged $36.6K per year.

The geographical breakout includes 29% response from the Northeast, 12% from the Southeast, 25% from the Midwest, 7% from the Northwest, and 28% from the Southwest.

Regional Salaries: California Leads

The Southwestern states, among them California, Arizona, and Texas, with a focal point on Silicon Valley, touted the highest average and median salaries. Keeping in mind that one half of the survey participants are engineering managers, the average respondent salary in the Southwest is $43.1K with the median salary at $45K. Close in contention with Silicon Valley is the Northeast where the average respondent salary is $41.3K and the median salary is $41K. The Midwest averaged salaries of $37.7K and a median salary of $38K. The Northwest, from which the lowest number of participants responded, averaged salaries of $39.8K and a high median salary of $41.5K. The Southeast, a growing high tech industrial base, responded with an average salary of $38.6K and a median salary of $40K (see geographical chart).

The Southeast has been deemed the second fastest growing regional area in the US with a projected 82% job growth rate by 1987 as found by a recent American Electronics Association (AEA) survey. In the survey, "Technical Employment Projections 1983-1987," California led the nation in overall projected growth for the electronics industry. The total job growth projected by 1987, including both technical professionals and paraprofessionals, was 90.4%, or a total of 91,029 jobs. The figures are based on survey questionnaires from 405 facilities in California. It should be noted that the figures represent only new jobs requiring additional employees, and not those jobs which become available through turnover or other forms of attrition. The lowest growth reported is in the Mid-Atlantic region with a projected 49% job growth rate.

According to the survey, California held its lead in all job categories in terms of actual job numbers: the total number of electronic/electrical engineers in 1987 is projected at 13,765, or 77.4% growth, and for software engineers at 9,700, an increase of 114.3%. While California's actual job figures were highest, other areas of the country reported higher percentages of growth in different job categories. The Northwest has the highest percentage of growth in both software engineers and electronic engineering technologists.

California also projected the highest figures on in-state recruitment, expecting to recruit 37% of new employees overall from in-state universities and colleges and the remaining 63% from the existing workforce and the military. These figures are undoubtedly influenced by the high concentration of engineering schools in California and industry's reliance on them for new graduate employees.

Education And Salary

Recent Bureau of Labor Statistics studies note the steadily expanding need for engineers in the workforce through the 1990s. At the same time, the studies

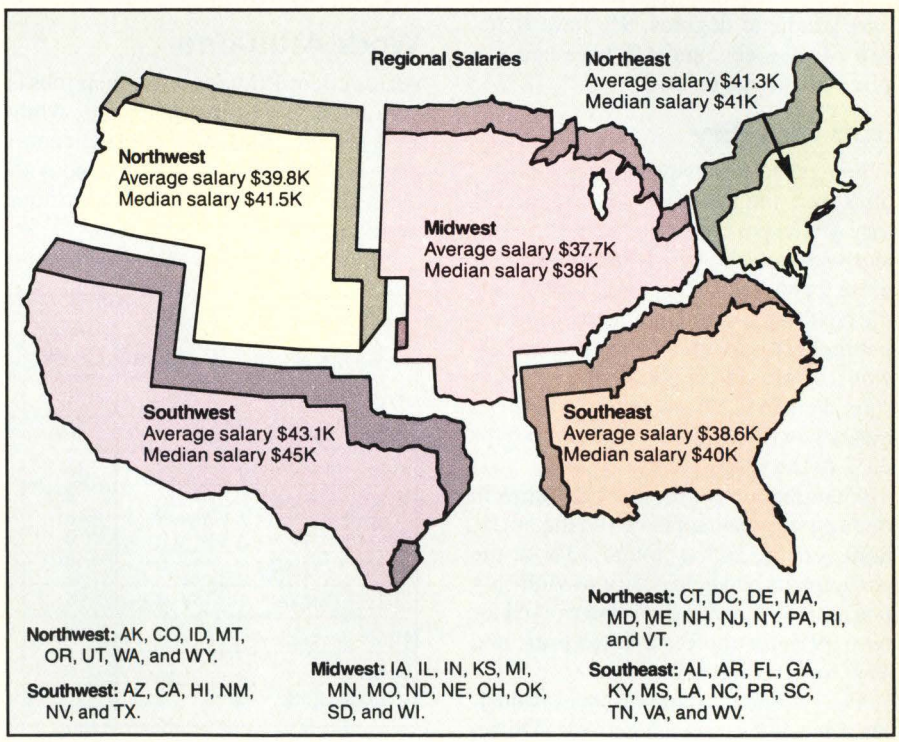


Table 2: Average and median salaries on regional basis.

showed a decline of 26% in the number of 18-year olds in the population expected by 1990. To adequately supply the continuing demand for engineers, IEEE and other organizations have called attention to the crisis in precollege math and science. It is clear that if students are to take engineering courses at the college level, they must be motivated toward and have strong access to adequate math and science instruction. A larger, less tractable problem than traditional university faculty shortages in such fields as electronic engineering and computer science, is the growing shortage of qualified secondary school math and science teachers.

The participants surveyed by *Digital Design* spanned the educational ladder, with 2% having not gone to college at all to 4% with doctoral degrees. B.S.EE degrees are held by 29% of the participants, while 6% have a B.A. degree and 9% have M.S./M.A. degrees. Nine percent have an M.S.EE and only 6% have an M.B.A., once thought a necessity in the transition from a technical position to one in management. A two-year associate or technicians degree is held by 6% of the participants and 16% attended college for two years or less but did not finish.

When comparing salary to education, predictably 15% of those participants in the over $50K range have graduate degrees, another 15% have a B.A./B.S.EE degree, and 2.3% in the over $50K category have had two years of college or less. Of those participants in the nation-wide average salary range, $36K to $40K, 3% have graduate degrees, 9% have B.A./B.S.EE degrees, and 4% have had two years of college or less.

Job Mobility

When asked to designate career objectives over the next few years, 74% of a total 476 respondents said their prime objective would be to advance with their present employer. Changing employers is the next step for 20% of the total and 3% put highest priority on changing professions. Almost 14% planned to return to school and 4% have no plans. Starting a business will be the next career move for 23% of the respondents.

Changing employers several times in one's career may appear to be the norm, however, the survey found 23% of the participants had held positions with only one employer, while 30% had worked for two; 19% for three; 12% for four; and 15% for five and over.

The criteria most important in evaluating a new job varies subjectively. Thirty-five percent of the respondents cited the engineering challenge of the product and technology as most important. Salary was of prime concern to 19% and location was most important to 20% of the participants. Opportunity for management responsibility, title change, and promotion was the primary evaluation criterion for 18%, and less than 5% are concerned with company reputation, benefits programs, or joining a particular design team.

When asked why they entered the electronic engineering field, 86% of the respondents said the challenge of the technology was their primary reason. Job security and job availability in electronics engineering was the primary influence for 13% and 29% respectively while the lure of high salaries attracted 26% of the total respondents.

Work Attitudes

An excellent attitude toward their jobs is held by 36% of our participants, while 25% feel their attitude toward their company is excellent. Only 1% have poor attitudes about their job and 5% have poor attitudes toward their employer.

Often the hours per week worked are an incremental factor in determining job satisfaction. The majority of participants, or 70%, worked 40 to 50 hour weeks.

Future Trends

From a general point of view, opportunities for engineers will continue to grow rapidly. The broader spectrum includes disciplines across areas such as applications, product management, R&D, and design. According to Engineering Associates, an engineering personnel consultant, there will be 10 primary technical influences on engineering professionals in the near future.

Design Specialization will lead to further opportunity for those with outstanding knowledge in several specific areas. For example, software disciplines which include development, test and quality control of micro-code, assembly and high-level languages will be in particular demand. Many industries will look for skills in both analog and digital design, particularly the latter, in handling eventual 32-bit architectures.

Factory Automation will impact many jobs as quantum leaps are made in pro-

Salaries

Salary and Education	% of total	$21-25K	$26-30K	$31-35K	$36-40K	$41-50K	Over $50K
No College	2.2	0	*	*	*	*	*
Under 2 Yrs. College, no degree	6.2	*	*	2%	1%	2%	*
2 Yrs. or more college, no degree	9.3	0	0	1.7%	1.7%	3%	2.3%
2 Yr. Associates or Technicians degree	6.2	0	2%	*	1%	*	*
B.A. Degree	5.8	0	*	*	1%	2%	1.7%
B.S.EE Degree	29.3	0	2.7%	4%	6%	8%	9%
Other B.S. Degree	11.4	*	*	1.7%	2%	2.5%	4%
M.S./M.A. Degree	8.9	0	*	1.3%	1.7%	2.5%	3%
M.B.A. Degree	5.8	0	*	*	*	1%	4%
M.S.EE Degree	8.9	0	0	1.4%	1%	2%	4.4%
Doctoral Degree	4.3	0	1%	0	*	*	3%
Other	1.2	0	*	0	*	0	*

**=less than 1% (less than 1% are making under $20K in all categories.)*

Table 3: Respondent's education in comparison to salary.

Salary and Age

Age	% of total	Under $20K	$21-25K	$26-30K	$31-35K	$36-40K	$41-50K	Over $50K
20-24	1.6%	.8%	*	*	0	0	0	0
25-30	13.4%		1%	2.7%	4.8%	3.5%	*	*
31-35	18.4%		1%	2.5%	2%	3.5%	5.6%	3.3%
36-40	17.6%		*	1%	1.5%	2.7%	5%	7.3%
41-45	16.5%		0	*	1.9%	1.7%	3.5%	9.2%
46-50	12.4%		*	*	1.5%	2%	3.5%	5%
51-55	10.1%		*	*	1.3%	1.3%	2.3%	4.8%
56-60	6.2%		*	*	*	1.3%	2.3%	1.9%
61-65			0	0	*	0	1.3%	1%

**=less than 1%*

Table 4: Respondent's age in comparison to survey.

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MK75602	VME-MMCPU	Memory management CPU; MK68000 processor with MK68451 memory management unit	$1700	20%
MK75701	VME-DRAM	256K dynamic RAM card; automatic refresh	$1120	20%
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MK75803	VME-FDC	Floppy disk controller; word DMA or programmed byte transfer over VMEbus	$ 820	20%
MK75605	VME-SYSCON	System controller card VMEbus slot 1 slave; control and check features and real-time clock (with battery backup)	$ 921	6%

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ductivity improvement and new technologies associated with automation, such as CAD/CAM become the norm.

Advanced Networks development will reach many applications across the industry as data transmission is accelerated to higher frequencies and increased bandwidth is obtained by use of hybrid technology using lasers and fiber optics. Engineers who combine multiple skills in electro-mechanical, electronics, and communication theory will be in top demand.

Small Computer Systems and Peripherals represent special opportunities for professional advancement, particularly in office automation product development.

Communications Technology is changing at a rapid pace, offering significant opportunity in word processing, networks, telecommunications, and microwave technology.

Semiconductor Evolution continues to push for newer and less costly packaging and production. The challenge to merge technologies—especially with digital and linear circuits—will become a significant trend throughout this decade.

Defense Electronics is of particular interest in an election year and the recent surge in Pentagon contracting has created many jobs. The advent of expert systems and artificial intelligence has definitely been fueled by defense dollars and opportunities in these areas should continue to grow.

Automated Test Equipment. As highly complex LSI and microprocessor systems proliferate, automated component and sub-system testing becomes necessary in an increasing number of applications.

Medical/Analytical Systems will drive advancements in product design allowing professionals to improve the functions and price/performance of existing instruments and measurement systems.

New Challenges In Component Design is directly proportional to the demand for compatibility and more intelligence. Meeting these challenges with innovative design and applications will be skilled designers from a diverse cross-section of disciplines. **DD**

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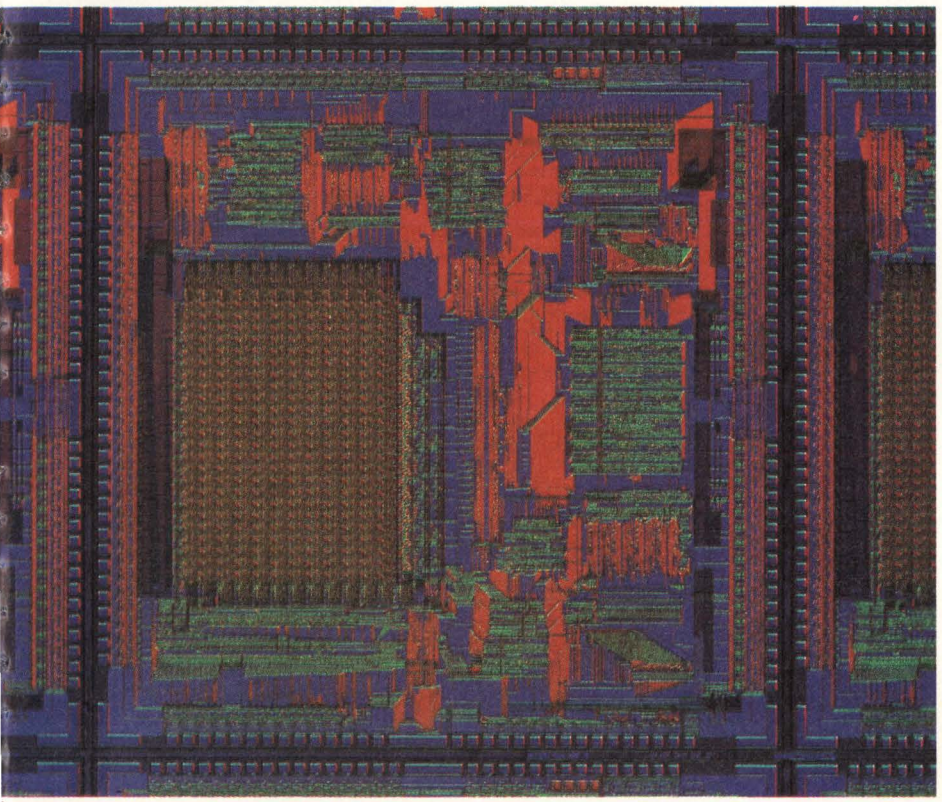
32-Bit ICs Enhance Array Processor Performance

by Dave Wilson, Executive Editor



Photomicrograph of AMD's 29325 floating point processor.

Future high performance processors/controllers require faster processing rates, higher machine densities, and greater system reliability. The need for virtual memory support, increased memory bandwidth and improved precision means a growing demand for 32-bit performance. Advanced Micro Devices' (Sunnyvale, CA) Am29300 family has been developed to address these needs in general purpose computation, intelligent peripheral control, and array and digital signal processing applications.

The Am29300 family evolved from the industry standard Am2900 bit-sliced family. A great number of the functional enhancements are the result of user feedback from existing Am2900-based designs. On the other hand, the Am29300 family has been designed from the ground up for higher performance and architectural flexibility. The Am29300 devices have internal ECL circuitry for speed, yet maintain TTL compatible inputs/outputs for ease of interface. A 32-bit Am29300 microprogrammed system has a system microcycle time of 70 to 80 nsec. In addition, the devices have regular and orthogonal instruction sets and contain built-in primitives to tackle crucial system issues such as fault tolerance/detection.

AMD offers several support chips for Am29300-based designs. For instance, systems requiring a 32-bit data path can be configured with the following devices: the Am29332 Integer Processor, a 32-bit arithmetic/logic and shift unit with built-in support for variable byte and bit field data; the Am29334 Register File, a true dual-ported register file which allows simultaneous read and write accesses, organized as 64 words by 18 bits; the Am29323 Parallel Multiplier, a 32 × 32 parallel multiplier capable of multiple cycle expansion to 64 × 64 and 128 × 128 without the use of external logic; and the Am29325 Floating Point Processor, which performs single cycle addition, subtraction, multiplication and conversions, using either the single precision IEEE or DEC format. Each of the above devices can be used in conjunction with or independent of the others. These devices can be configured in a variety of ways to tailor them to a specific application. All of the data path elements have single cycle instructions. The microinstructions are typically supplied by the control path. The key control path element is the Am29331 Microprogram Sequencer which supplies the next address to the control memory. The 16-bit Am29331 is also capable of handling interrupts or traps at the microinstruction level.

Historically, the Am2900 devices have been partitioned vertically, combining register file and ALU in a single package. The Am29300 devices, however, are partitioned horizontally, so that the register file is separated from the rest of the data path elements. The functional partitioning has two advantages. First, it allows for an easily expandable register file space. Second, it also enables arithmetic accelerators to add to the data path.

A major disadvantage of a bit-sliced architecture is the time lost in transmitting carries from one chip to another. To avoid this, the Am29300 family arithmetic elements are constructed with full internal 32-bit data paths. Although the ALU has limited carry capability for cascading, it will normally perform multi-precision expansion through multiple cycle opera-

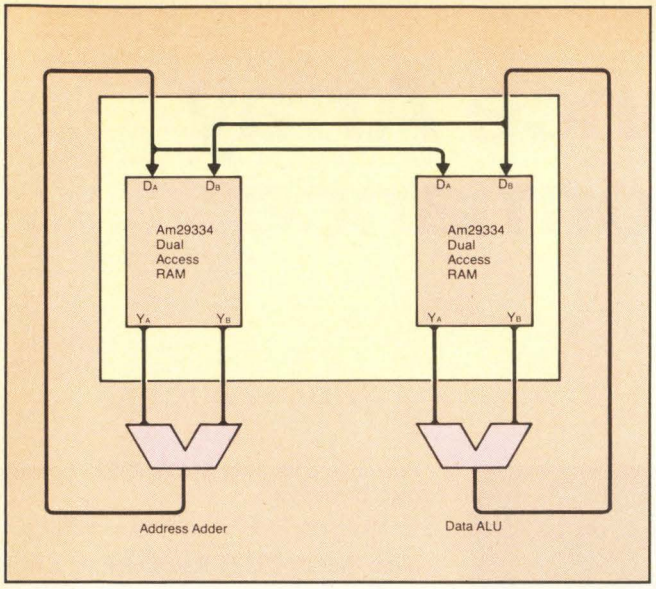


Figure 1: RAM with 4 read and 2 write ports.

tions. The other data path elements use this scheme exclusively.

A second benefit of the full 32-bit data path elements is that they can include functions not easily sliced. Two classic examples of this are shift arrays and multipliers. Both of these require an unacceptable amount of information to be transferred between slices. Other functions, such as prioritization and mask generation for byte and word operation, while feasible, expand clumsily. All these functions are provided in the Am29300 family, either in the ALU, or in the 32-bit multiplier.

Three-Bus Flow Through Architecture

In order to fully exploit the 32-bit data path devices, it is necessary to provide adequate data transfer bandwidth. In the Am29300 family this is achieved through the use of a three-bus architecture. The Am29334 Register File is a true two-ported file, allowing simultaneous access from each port. Output latches are provided to allow read and write operation within a single clock cycle. Each of the data path elements has two 32-bit operand input buses which can be sourced from the register file. The data path elements also have a 32-bit result bus which can return data to one input of the register file. With this organization, a three-address register to register operation may be completed within a single clock cycle.

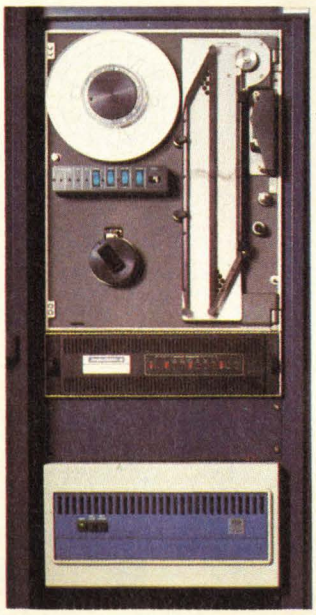
Two-register files may be used to achieve still higher bandwidth. Connecting the input ports in parallel, and writing duplicate data into the two files, allows four operands to be sourced simultaneously from a single database. Two results may also be written into the file simultaneously. This provides adequate data transfer for two groups of arithmetic elements to operate concurrently (**Figure 1**). The flexibility of this three-bus architecture also allows the use of these parts in other configurations. In a signal or array processing application, the multiplier and ALU may be placed in series rather than parallel. This provides a "free operand," allowing the three-operand summation of products operation to proceed at maximum speed.

The cycle time of a microprogrammed system is dependent on both the control path (i.e., sequencer and microprogram memory) and the data path (i.e., register file and ALU). Traditionally, the system bottleneck has been the control path, especially the timing paths associated with conditional branching. The 16-bit Am29331 Microprogram Sequencer has been optimized for speed, so that the data path and control path timing are balanced. The previously external condition code multiplexer, test logic generator and polarity control logic (usually the system critical path), have been integrated on chip. Moreover, the Am29331 has several built-in features which enable it to respond to external stimuli with minimum latency. The sequencer can perform a 16-way branch, dependent on the simultaneous occurances of four external test conditions. The Am29331 Microprogram Sequencer can also handle interrupts or traps at the micro-level.

The system ARM concept (Availability, Reliability and Maintainability) is becoming increasingly important. The Am29300 addresses the problem of fault detection at the device level by a combination of two techniques – parity and master/slave. Parity at the byte level is generated on the 32-bit result bus of the data path elements, stored in the Am29334 Register File, and checked again going into any of the operand buses of the data path elements. Thus any interconnection failure in the data bus can be detected. The choice of even parity scheme also allows detection of an open TTL bus which defaults to high impedance all "ones" state, an error condition. For functional verification, a master/slave mode of operation permits two units to be connected in parallel, with one unit actually performing the computation and the other checking the results on a cycle by cycle basis. The slave unit therefore verifies correct operation of the master. In addition, the master unit checks its internal result with the data on the output bus to ensure that no other device is driving the external bus when it is not supposed to be. Any fault detected can trigger an interrupt at the microinstruction level. Unlike previous redundant schemes, no specialized software is required. No system degradation results from the communication between the redundant functional units. This combination of parity checking and master/slave operation, which uses cost-effective hardware, rather than expensive software, is the key to future redundant system design.

The functional and performance requirements of a general purpose superminicomputer and a digital signal processor are vastly different. Yet with functional partitioning and a simple three-bus architecture, the Am29300 devices are suited to address the needs of a diverse spectrum of applications. **Figure 2** depicts an example of a microprogrammed supermini built out of Am29300 components. The data path consists of the Am29332 Integer Processor, the Am29323 Parallel Multiplier as an accelerator, and the Am29334 Register File. In this configuration, address calculation and data computation are performed in series. Alternatively, the Am29334 can be paralleled to yield effectively a six-ported register file, allowing four read accesses and two write accesses per microcycle. Another Am29332 can be dedicated to perform address computation concurrent with the normal ALU execution, sharing the register space. With a 70 to 80 nsec microcycle time, a processor/controller subsystem capable of several times the performance of a typical supermini can be built with the Am29300 parts, occupying far less board space and dissipating significantly less power.

Figure 3 is a block diagram of a small array processor using the Am29325. A high-speed multi-port memory is used to provide storage for operands such that they may be accessed in simultaneous pairs. These operands may originate in the data memory, or may be intermediate results



A major application of the AP400 is as a subsystem within automatic test systems such as this LTX... The AP400 offers a cost-effective means of adding powerful linear test capability to digital ATE systems.

The AP400 and ATE

The AP400 Array Processor's high-speed number-crunching power can make it a key component within an ATE system. It can serve a number of purposes in such a system, acting as an active signal filter, a high-speed data manipulator, or even as a waveform synthesizer.

The AP400 brings the performance of computationally-intensive operations into the real-time domain. Transfer function analysis, convolution and correlation, and power spectrum calculation are but a few of the procedures which can be performed in just milliseconds with an AP400 — several hundred times faster than with an unaided minicomputer.

Minimizing host burden was a prime consideration in designing the AP400. Such features as direct memory access to the host, a powerful on-board control processor for internal housekeeping functions, and internal table storage and lookup ability mean that for many applications the host processor need only be involved in telling the AP to start and in picking up the processed data. The auxiliary input and output ports also help minimize host burden. Raw data can enter the AP400 directly, without host involvement, and processed data can be sent directly to peripheral equipment. This feature is particularly useful when the AP400 is used as a waveform generator. The AP400 can send the synthesized signal directly to a test bed without involving the host. The AP400 is currently in use in such diverse applications such as checking codec pairs and airborne radar testing. To find out more about how the AP400 can help you with your ATE problems, contact

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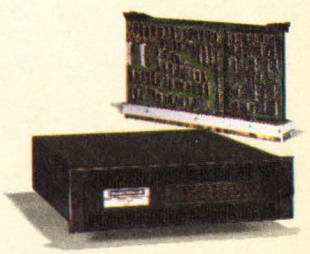
1024 point complex FFT	7.4 ms
Real convolution (1024 data, 512 kernel)	7.3 ms
2048 point power spectrum (with Hamming window)	13.5 ms
1024 pcint, ensemble-averaged transfer function	1.2 s



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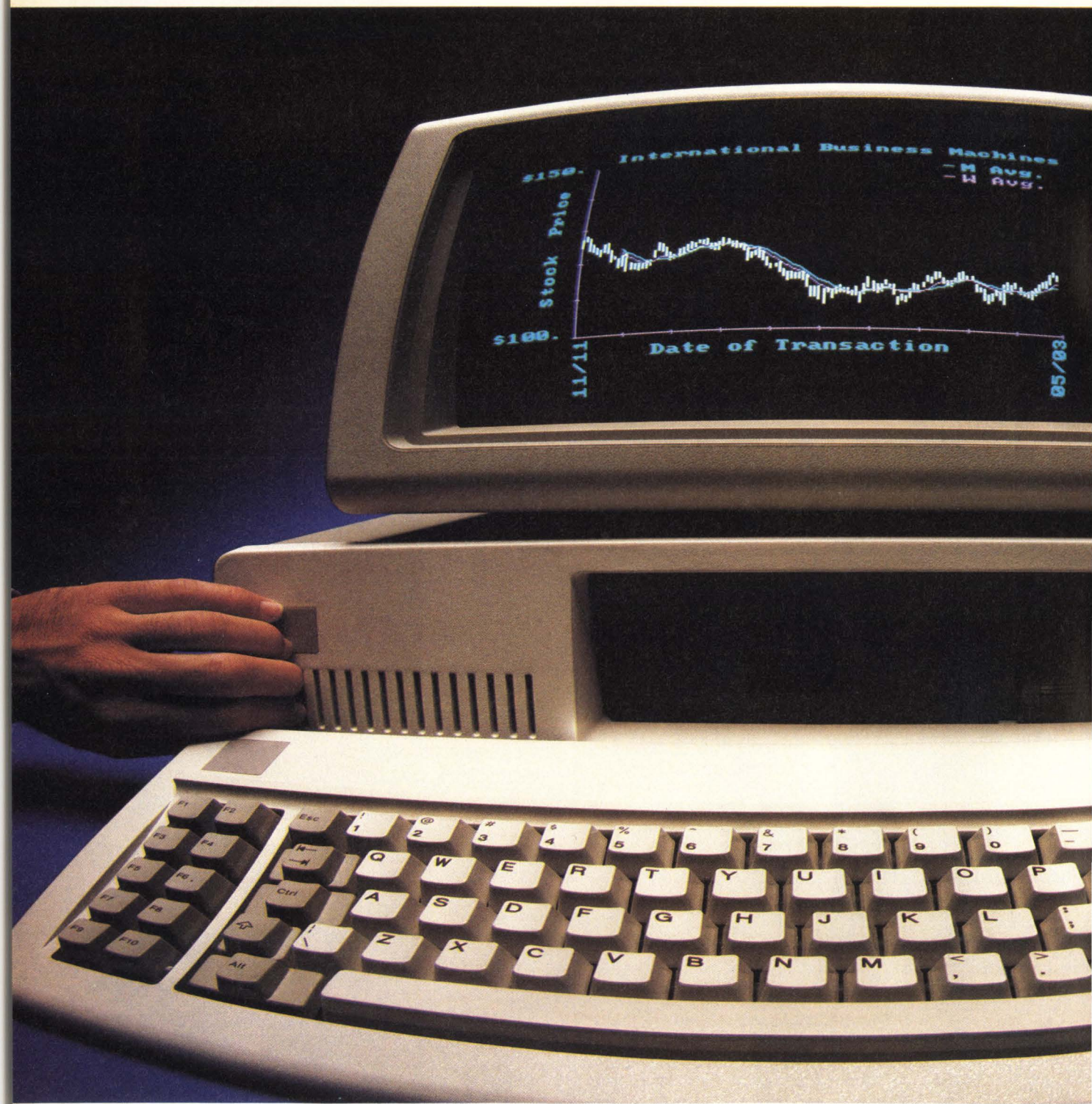

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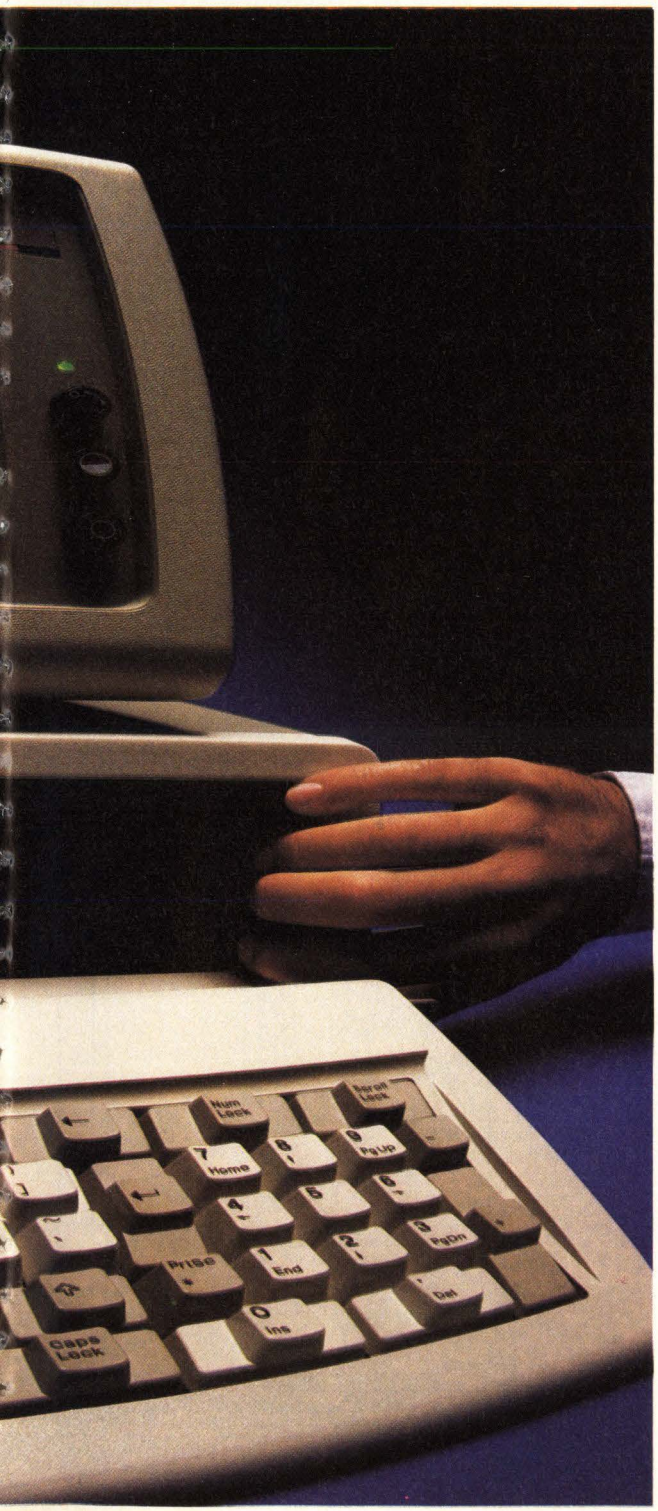

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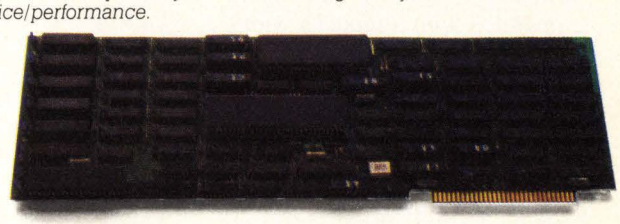

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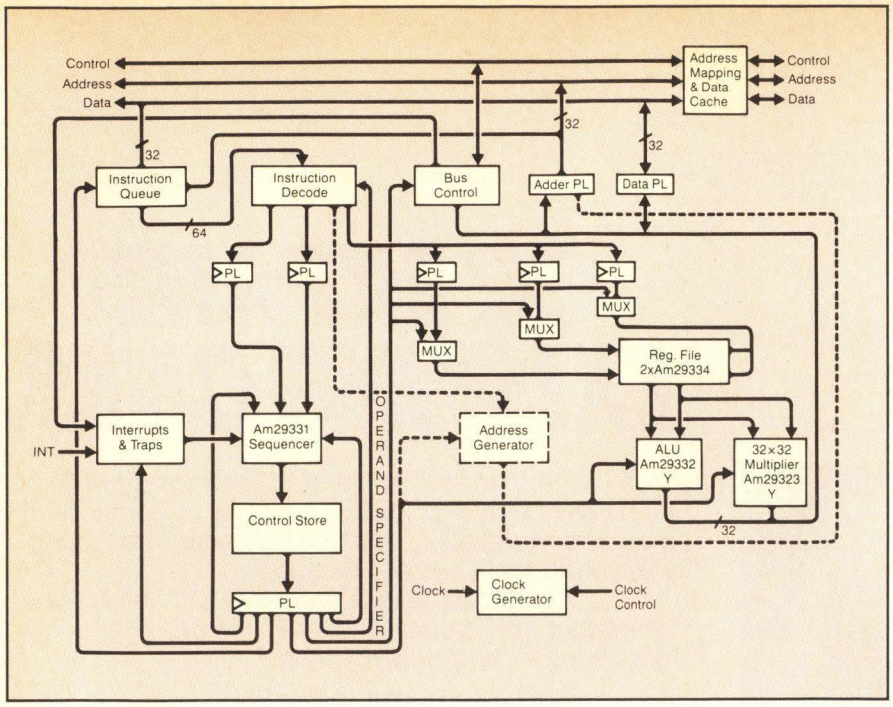

Figure 2: Am29300-based supermini emulation.

from the processor. One of these operands may be replaced with a value drawn from a non-volatile coefficient store.

The array processor is microprogram controlled, with memory addresses being derived directly from the microcode. This is probably inefficient for large programs, and some form of microprogammed address generator would need to be added. The interface to the host processor is deliberately undefined, as this is user dependent.

As a benchmark, this processor can perform FFT butterflies in the canonical time of 10 cycles. At a 100 nsec cycle time, this permits one butterfly every 1 μsec, or a 1024-pt complex transform in 5.12 msec. A simple modification to the architecture allows a second Am29325 to be incorporated to give a complex arithmetic processor. This doubles the throughput for the FFT, reducing the computation for the 1024-pt transform to 2.56 msec.

While the Am29325 only provides single-precision floating point operation, the Am29300 family also provides bus-compatible devices which may be used to enhance the capabilities of the array processor described. The Am29332 Integer Processor offers a wide range of arithmetic, logic and shift facilities. This device may be operated with a reduced width data path, allowing words of 1 to 4 bytes. The internal architecture is designed for efficient programming of floating point operations, and may therefore be used to support the Am29325 with double-precision operations. To assist in double-precision floating point multiplication, or for integer multiplication, the Am29323 32-bit Multiplier provides 32 × 32-bit multiplication in a single cycle, and has internal facilities for multi-cycle expansion to 128 × 128.

These additional arithmetic elements have the same 32-bit, three-bus architecture as the Am29325. This allows them to be added in parallel. The routing of operands to the appropriate arithmetic element is a simple microcode task.

The horizontal partitioning of this new family of parts has resulted in a number of benefits. First, the user gains the flexibility of adding storage elements to two uncommitted output buses from the processor. Second, more power budget is available for the register file making it faster and bigger than if it had been in the processor chip. The family addresses a number of crucial system issues such as fault detection, support of high-level languages in systems programming and large register file-based architectures like RISC. DD

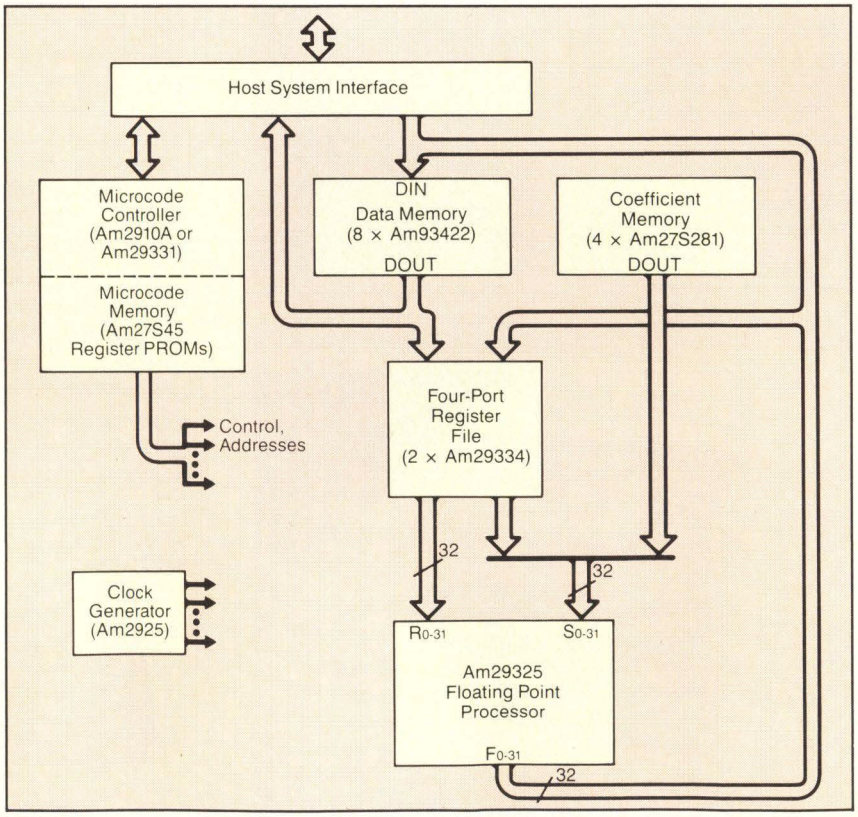

Figure 3: Am29300-based array processor.

References:

32-Bit Building Blocks for High Performance Processor/Controller, Paul Chu, Advanced Micro Devices, Sunnyvale, CA

A Very High Speed Floating Point Processor, B.J. New. Advanced Micro Devices, Sunnyvale, CA.

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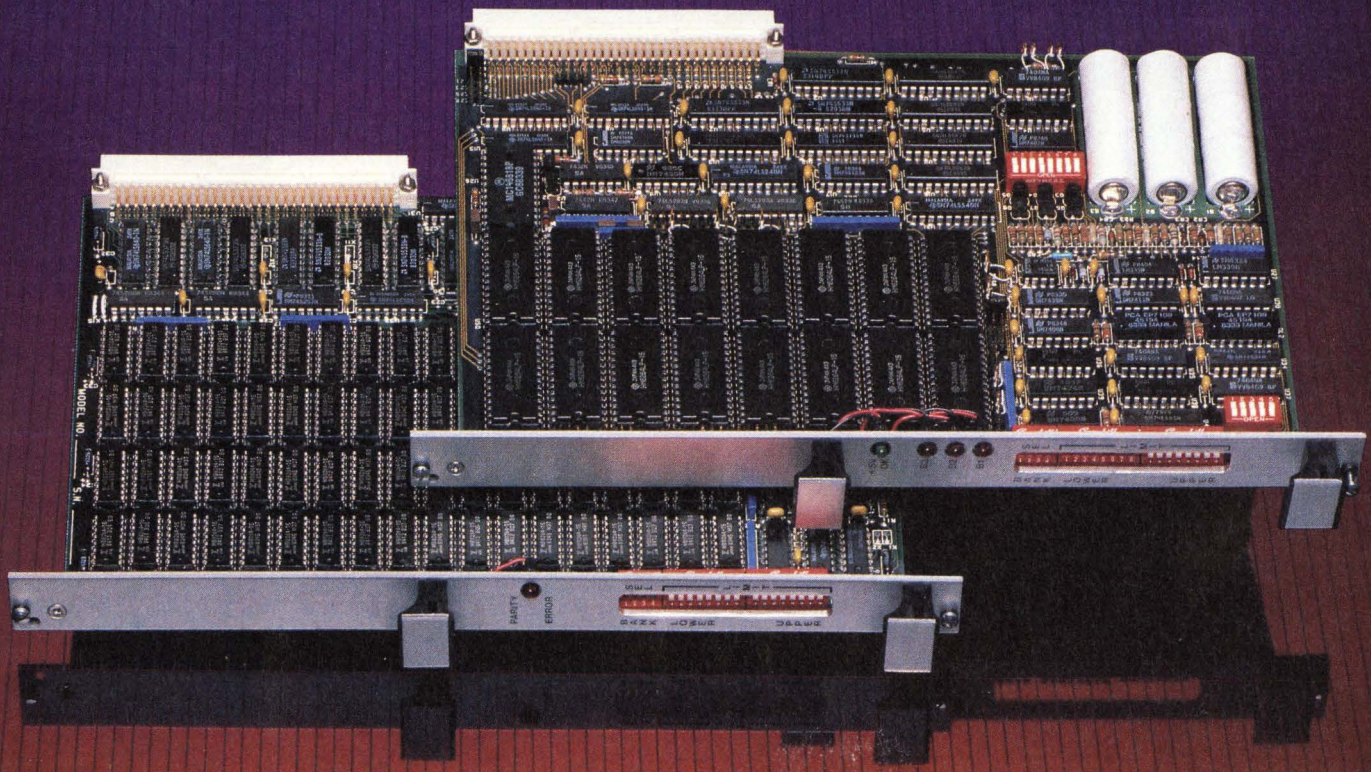

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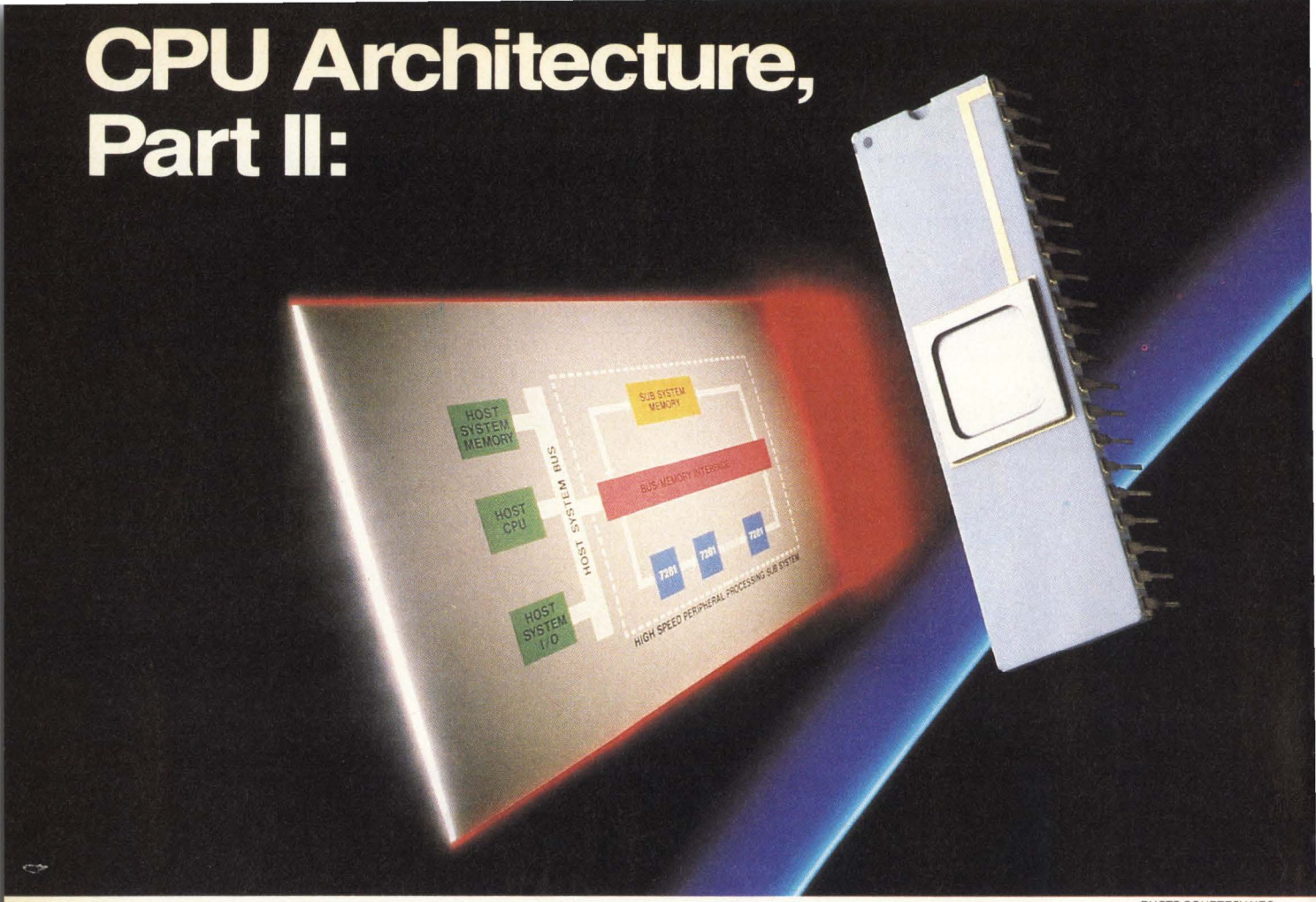

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Dataflow Computers Encroach On von Neumann Territory

by Ronald Collett, Technical Editor

In Part I of this two-part series, the discussion centered around the problems of traditional von Neumann computers (*Digital Design,* November 1984). The most important points to gain from that discussion are the difficulties encountered when extending traditional computer architectures to a multiprocessor system. Although it is quite possible to design a scalable* multiprocessor von Neumann machine, the actual implementation can prove to be exceptionally difficult.

Nevertheless, many computer manufacturers as well as research facilities have embarked on such a cause. The philosophy being, that extending an already proven design is much easier than creating a new architecture. The major criticism of this approach has been its centralized control. Specifically, the entire computational system of a von Neumann computer is built around its program counter. And for the reasons outlined in Part I, this can be inefficient with respect to processing. In general, von Neumann computers can be thought of as instruction driven systems which depend on the program counter for specific guidance.

Dataflow machines, on the other hand, seek to completely decentralize program control by relying on a data driven architecture. These new systems are viewed as strong contenders to challenge the traditional von Neumann style of design.

The Dataflow Concept

No predetermined order of events exists in a dataflow machine. Each data word is given a label, or tag, describing the operation that it is destined to undergo. The data word together with its label is a so called "token." Tokens are systematically generated, and the actual dataflow system is designed so that tokens of the same operation can locate each other and match up. When all the tokens needed for a particular operation are matched, the operation can be executed. (An instruction is executed when all the operands are

*The term scalable refers to a computer that can be increased in size by incrementally adding processing, memory and communication elements.

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New computers that diverge from traditional architectures may be the solution to the demands of high speed processing.

available is another way of describing the general concept).

For example, suppose we wanted to perform the multiplication of two numbers, say 6×3. Two tokens would exist for this operation, a token describing the six and another describing the three. Each token would also include a few bits describing the multiplication operation and a few bits to tell it that the number 3 (or 6) is its match.

From this general description, it appears that a great deal of randomness would exist in a dataflow machine, however, the dataflow software systematically organizes the flow of tokens. Dataflow programs are descriptions of graphs that illustrate the destination and route of the data word (**Figure 1**). Through the combined efforts of the dataflow hardware and software, tokens are generated and channeled to the proper locations.

Programs are loaded into the dataflow machine; they are encoded into computational graphs by the machine's compiler and are then stored in memory. During program execution, tokens refer to the graphs, which route them according to their label.

Facilitated multiprocessing is one of the primary advantages that dataflow machines may have over von Neumann architectures. More specifically, dataflow systems are not constrained by a complex control scheme since each token moves efficiently among the various processors of a multiprocessor system. In essense, this efficient movement among processors is dynamic load scheduling. But unlike von Neumann designs, dynamic load scheduling is intrinsic to a dataflow machine.

The other drastic differences between a dataflow machine and a von Neumann machine is the time spent on fetching instructions, loading data, and storing the intermediate results of a calculation. These functions make up the fundamental nature of a von Neumann machine. A dataflow machine, in contrast, spends none of its time with these types of chores. Rather, it performs tasks as soon as the necessary data is available, and during the interim when some tokens are waiting to be matched, other previously matched tokens are undergoing execution. Thus, little time is wasted on chores which are inherently necessary to a conventional von Neumann machine. Of course, there is "no free lunch" since dataflow machines have their own set of similar housekeeping chores. But these duties are much different than those outlined above and supposedly usurp much less time.

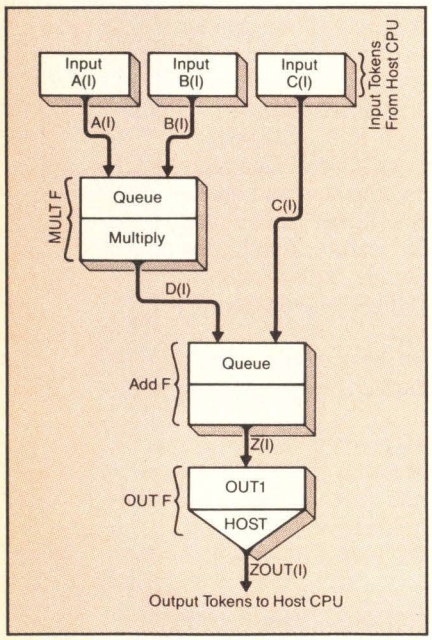

Figure 1: This simple dataflow graph depicts the following mathematical expression: Z(I) = [(A(1) × B(1)) + C(1)]. Graphs such as this, are mapped directly onto the dataflow machine's memory.

A VLSI Dataflow Chip

NEC expects to test its first VLSI dataflow chip this month. The new IC, designated the Image Pipelined Processor (μPD7281), was prototyped using off-the-shelf components and has been undergoing the VLSI process over the past year. The μPD7281 is designed for real time signal processing tasks, and according to the Japan-based firm, is well suited for image processing applications that use algorithms such as two-dimensional convolution, enlarging, shrinking and rotation.

The basic μPD7281 architecture uses an internal circular pipeline and a high-speed multiplier for increased performance. The chip's internal structure is also tailored to support multiple chip configurations.

The internal architecture of the μPD-7281 can be separated into nine functional blocks (**Figure 2**). Of these nine, six are dedicated to the circular pipeline: (1) Link Table (LT), (2) Function Table (FT), (3) Address Generator and Flow Controller (AG & FC), (4) Data Memory (DM), (5) Queue (Q), and (6) Processing Unit (PU). The remaining three provide the interface between the pipeline and the outside world (via the data bus and control signals) and are as follows: Input Controller (IC), Output Controller (OC),

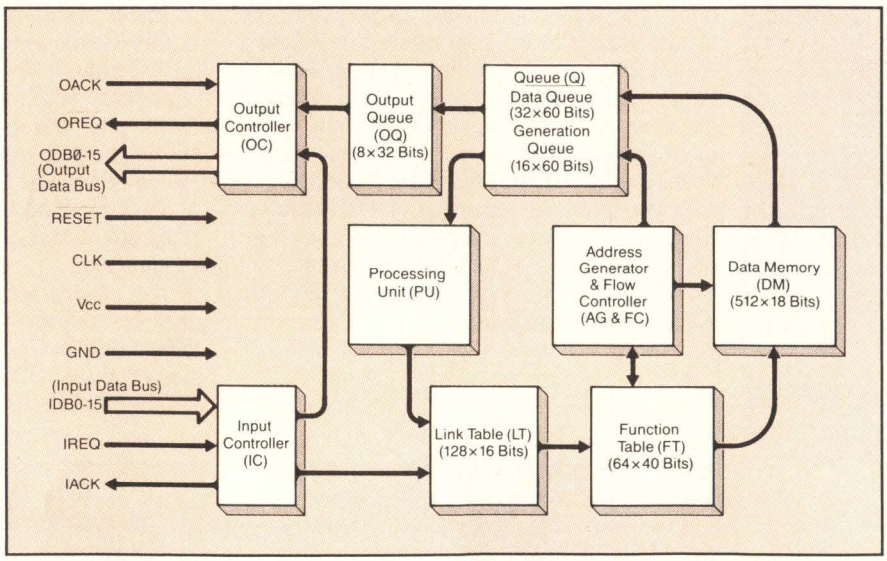

Figure 2: A block diagram of NEC's μPD7281 Image Pipelined Processor. The basic dataflow architecture is based on a circular pipeline.

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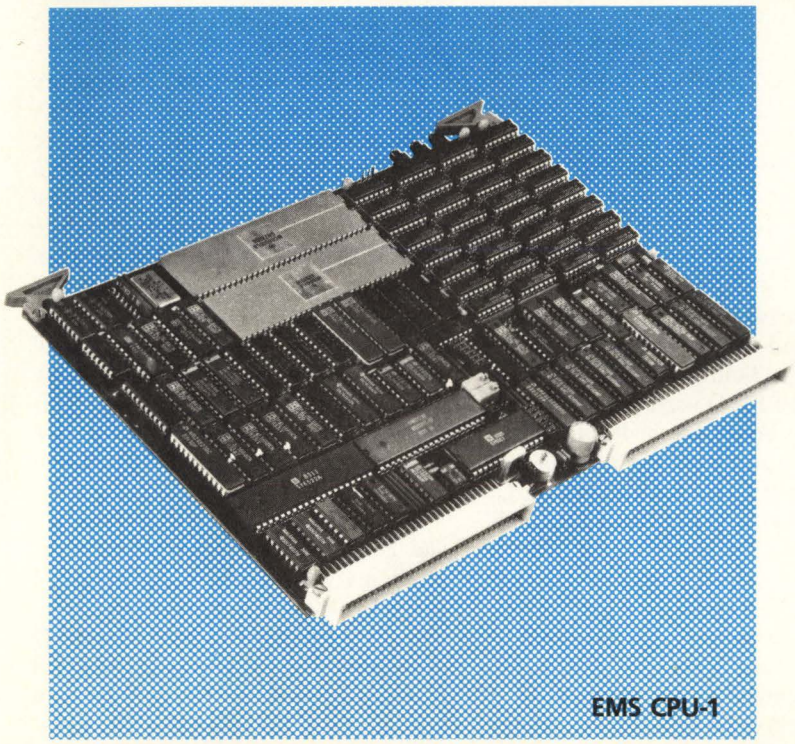
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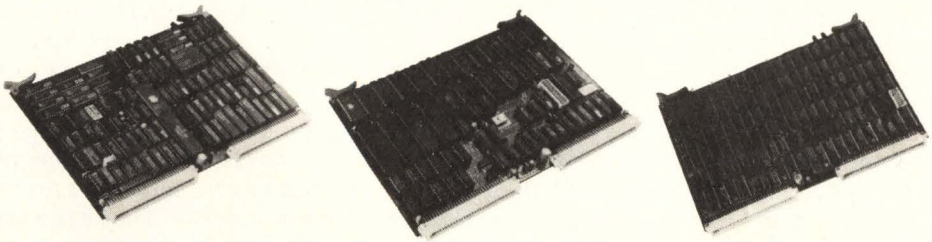

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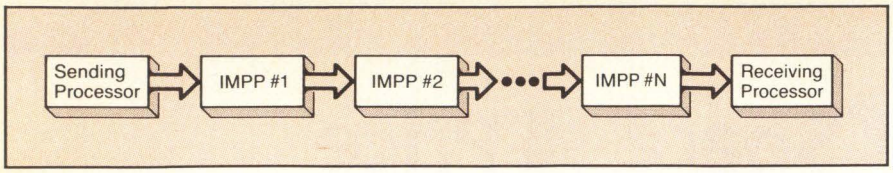

Figure 3: When integrating the μPD7281 into a system, one option is to use this cascade configuration.

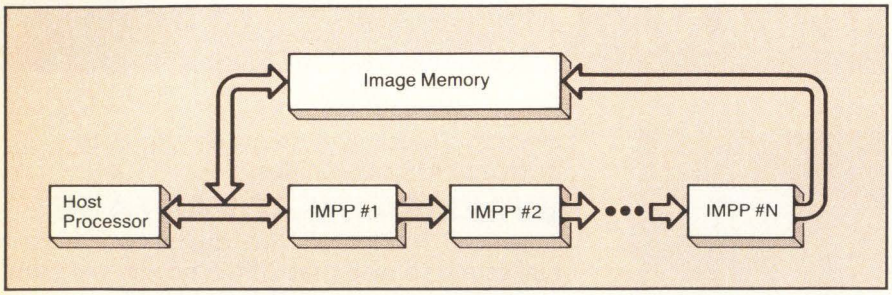

Figure 4: Aside from the cascade arrangement in Figure 3, the ring configuration is another approach to μPD7281 system design.

and Output Queue (OQ). (The Refresh Controller is a tenth block, but is not shown, since it is unnecessary for this discussion).

Assuming that a particular dataflow machine includes several μPD7281s linked together, the input controller's primary task is to identify tokens that are supposed to be processed by that particular μPD7281; and screen tokens that are targeted for one of the other μPD7281s. When a token is accepted by the input controller, it is then directed to the link table, which is a 128 × 16-bit dynamic RAM. The identification field of an incoming token is used to access a location in the LT. Once inside the proper LT location, the token acquires information (the FT address) that directs it to its next destination, a new identification field, and some additional instruction related fields.

With an FT address supplied by the LT, the token then proceeds to that FT location where an actual instruction for the token exists. (Note that the label on the token does not include the actual instruction, but rather a pointer which directs the token to the memory location holding the instruction). The instruction in the FT provides control information regarding the processing unit and AG & FC. The AG & FC generates the addresses to access the data memory and controls the DM read/write signals. The most important task of the AG & FC is to determine whether all operands are available to execute an instruction. For example, if only one operand is available for a two-operand instruction, AG & FC temporarily stores the operand in a DM location. If both operands are available, AG & FC provides the two operands with PU control data and sends the primary data's identification field to the Q.

The Q is a FIFO used to temporarily store tokens bound for the PU. Controlling the number of tokens flowing through the pipeline requires that the Q be divided into a data queue and a generation queue. The latter is used to hold tokens that will be used to generate new tokens. The data queue temporarily holds tokens that contain PU, output, or AG & FC instructions. A total of 48 tokens (60 bits wide) can be held in the whole Q.

After the tokens gain entrance to the PU, the PU performs logical, arithmetic and bit operation tasks. The PU then generates a new token as a result of the operation. If the resulting token still needs further processing, it is forwarded through the pipeline again. On the other hand, if no further processing is necessary, the token is sent back through the pipeline, but instead of waiting to be matched and dispatched to the processor, it is advanced to the Output Queue (which is an 8 × 32-bit FIFO).

From the OQ, the data token then moves to the output controller, which puts the token on the output data bus. Once it is on the data bus, the token proceeds to either another μPD7281 or perhaps an external memory.

Putting The Pieces Together

As shown earlier in **Figure 1**, the computational processes of a dataflow machine can be represented graphically by this so called computational graph. The archs, or links, which join the various nodes represent a dataflow value, or token, while the nodes themselves depict a functional operation of the machine.

Taking this one step further, a direct correlation exists between the graph and the block diagram of the dataflow machine. When a dataflow program is downloaded into the chip, the programming information is channeled to either the link table or function table. Comparing the block diagram of **Figure 2** to the graph in **Figure 1**, the archs correspond to the entries of the link table, and similarly, the nodes represent the entries to the function table.

As a token proceeds through the μPD7281's circular pipeline, the token's identification label, control data and the value itself change as a result of the pipeline operations it underoges. Whether a change occurs or even the type of change that may occur, depends on the nature of the instruction that the token holds and the availability of other matching tokens.

NEC claims the μPD7281's exceptional efficiency is because of the processing unit's near continuous operation. This uninterrupted operation is a result of a continuous stream of tokens which feed the processing unit.

The pipeline holds up to five tokens, and the Q can store 48 more. One of the problems with dataflow machines, in general, is the generation of an excessive number of tokens. This can cause the Q to overflow which leads to a loss of token flow control and, in some instances, a system crash. To avoid this situation, token generation in the μPD7281 is controlled by the PU which senses a potential overflow.

Cascade and Ring Configurations

When implementing the μPD7281 into a system, either the cascade or ring configuration can be used; both are shown in **Figures 3** and **4**, respectively. The cascade approach requires a host processor to feed and accept tokens at the input and output of the chain. Efficiency would be improved if there were separate processors for feeding and receiving.

The ring configuration requires a host processor, an image memory and some control logic to multiplex data from the host processor and image memory. To support this design approach, NEC plans to introduce a Memory Access & General Bus-Interface Chip (MAGIC). This support device will control token flow among the μPD7281s, the image memory and the host processor. Up to four μPD7281s can be maintained by MAGIC.

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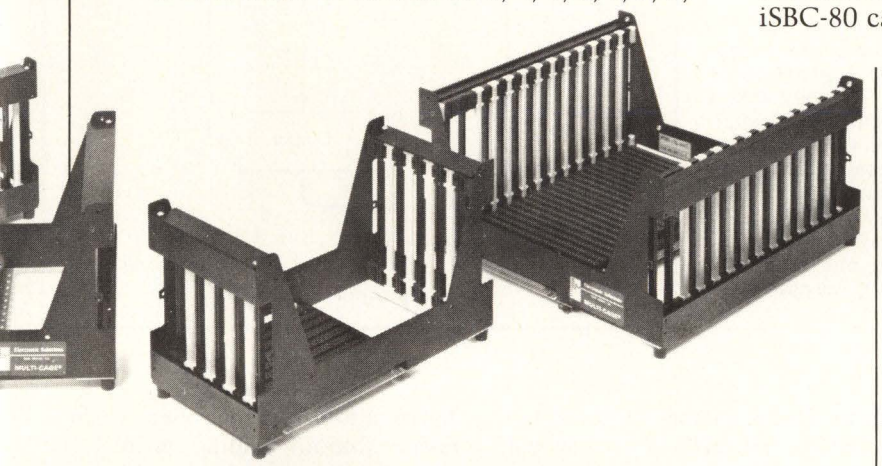

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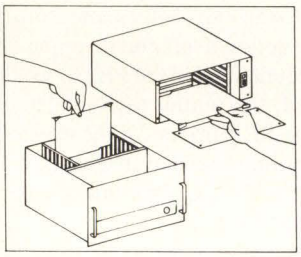

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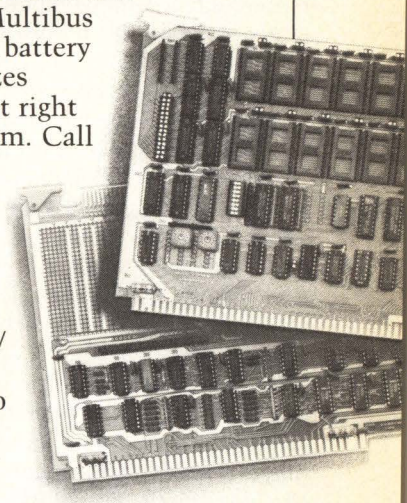

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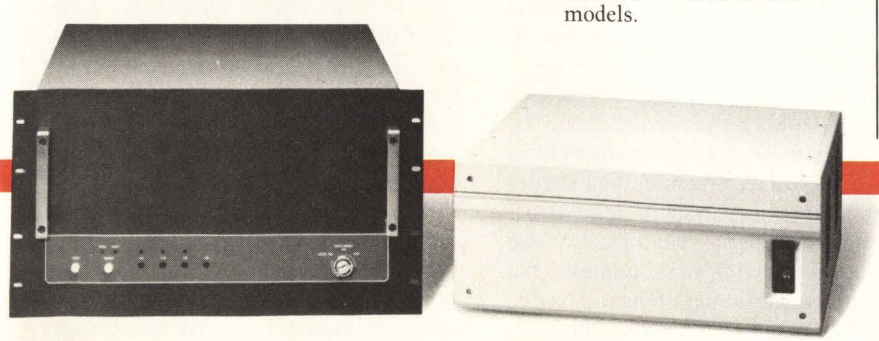

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As far as performance is concerned, the prototype dataflow system was implemented in both cascade and ring configurations. **Tables 1** and **2** show the results of these benchmarks. According to NEC, even though the actual processing throughput rate may vary between various applications as well as different system implementations, the overall processing time decreases almost expotentially with the increase of processors. Since this is the case, the law of diminishing returns comes into play if the number of processors gets too large. So the systems architect must select the optimum number of processors for the particular application.

MIT's Dataflow Research Effort

Although NEC is a frontrunner in dataflow technology, the Massachusetts Institute of Technology (Cambridge, MA) has an extensive effort in this area as well. One of the dataflow groups at MIT, headed by Professor Arvind, a leading researcher of supercomputers, is currently assembling a 64-processor dataflow machine.

In Arvind's dataflow design, designated the Tagged Token Dataflow Architecture, the 64 processing elements are connected in an n-cube network. Each processing element (PE) can be divided into five functional blocks: (1) A waiting-matching section, (2) An instruction-fetch section, (3) An ALU, (4) An Output section, and (5) The I-structure storage section (**Figure 5**).

In the typical operating mode, a dataflow program would first be compiled into a computational graph and stored in the program memory. Tokens arriving at the machine's input are classified according to type. And those requiring partners are channeled to the waiting-matching section. Similar to the NEC dataflow chip, each token contains the label, or tag, identifying its target instruction. By comparing the tags they carry, tokens can be readily matched. When tokens are paired, the two are sent to the instruction fetch unit. In many instances, however, a match may be expected but not found. If this occurs, the token remains in the waiting-matching section's associative memory until its partner arrives. Tokens requiring no partners are sent directly to the instruction fetch unit.

When the tokens arrive at the instruction-fetch unit, the op-code and any constants are fetched. The instruction is enabled and passed on to the ALU for execution. From the output of the ALU comes the resultant data, which is then

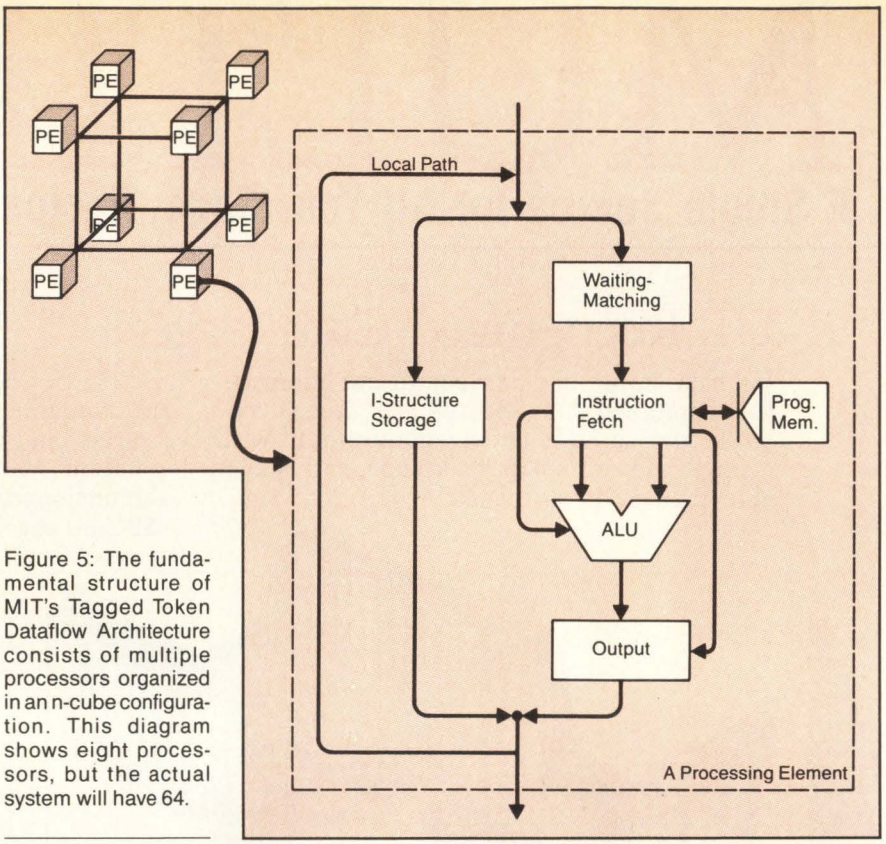


Figure 5: The fundamental structure of MIT's Tagged Token Dataflow Architecture consists of multiple processors organized in an n-cube configuration. This diagram shows eight processors, but the actual system will have 64.

ready to move to another target instruction. But before it can do so, it must be put into token form. So it moves to the output section where a new token can be assembled. This new token is constructed from the old token's tag, information stored in the instruction itself and mapping information contained in the PE. As would be expected, the output section also computes the PE number for the new token, and a routing translation table then converts this PE number into a network routine address.

This sequence of events is one of the paths that a token may take when passing through the PE, however, others are available. For instance, a token may be destined for the I-structure or perhaps the PE controller. The I-structure is a memory section that stores large data structures, such as arrays. Pointers, which are carried by the various tokens, point to memory locations of these data structures. Unlike conventional memory systems, the I-structure allows efficient synchronization and overlap of read and write requests, but does not constrain parallelism. (As discussed in Part I of this series, the read-before-write race condition can be difficult to overcome).

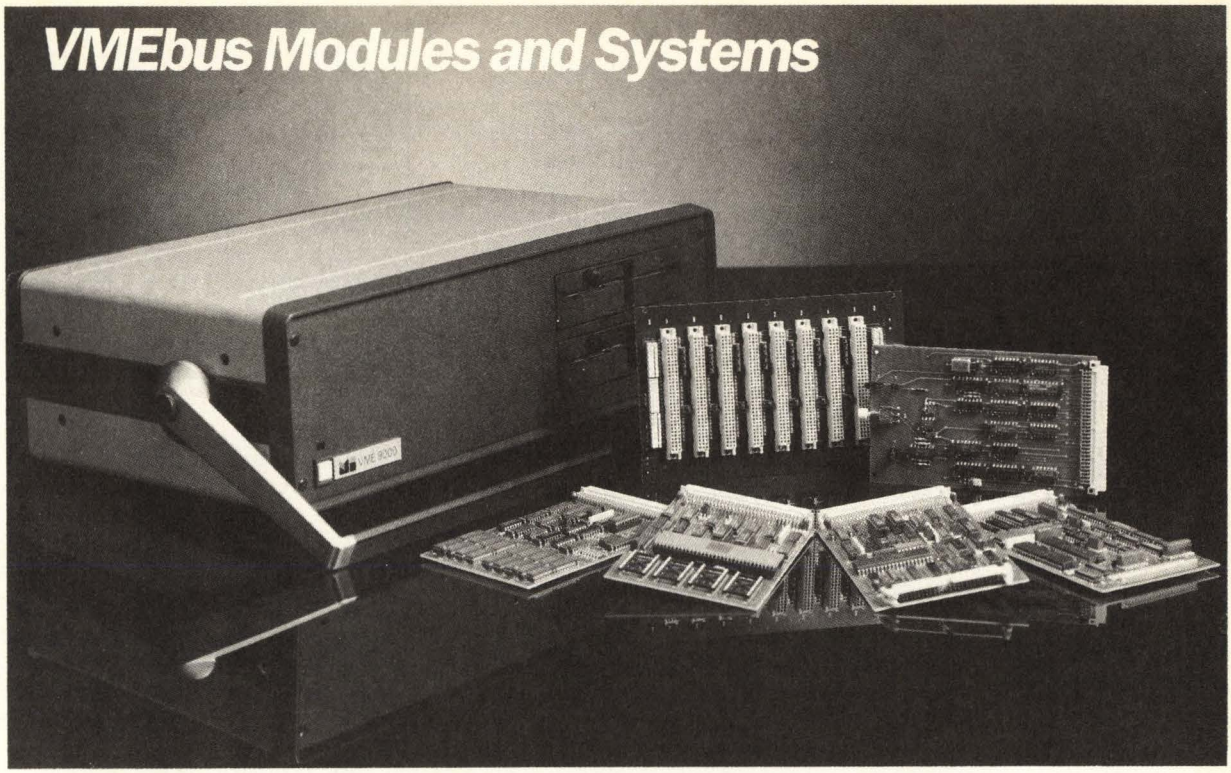
The I-structure hardware functions as a self-sufficient memory subsystem and is crucial to the machine's performance. Adjacent to it is a controller, which is responsible for reading, writing and managing the I-structure storage.

When data is actually available in the I-structure, it operates like a conventional von Neumann memory system. In other words, if a memory request is issued from the processor, the I-structure finds the data and sends it to the processor. The differences between the I-structure and conventional memory systems become apparent, however, when a request is made for data that has yet to be stored in the I-structure.

In a conventional memory system, accessing non-existent data can cause serious problems, such as an incorrect reading of the value stored in a particular location. In contrast, if certain data has not yet been stored in the I-structure, but a request is made for the data supposedly stored in that location, the I-structure controller simply defers the request until the data arrives. (A special deferral section exists adjacent to the I-structure.) When the data becomes available, all the stored deferrals are then satisfied. An analagous situation would be taking messages for someone who receives phone calls but is not in the office at the moment.

Dataflow Programming

Programming a dataflow machine, such



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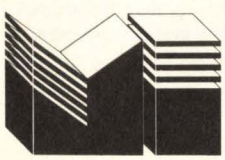

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64-stage FIR Filter	50μsec	18μsec	17-bit Fixed Point
Floating Point Multiplication	4.6μsec	1.8μsec	17-bit Mantissa 17-bit Exponent
COS (X)	40μsec	15 μsec	33-bit Fixed Point

Table 1: Execution times of the μPD7281 Image Pipelined Processor when implemented in a cascade configuration.

Operation	1 ImPP	3 ImPP's	Note
1/2 Shrinking	80 msec	30 msec	512 × 512 Binary Image
Smoothing	1.1 sec	0.4 sec	512 × 512 Binary Image
3 × 3 Convolution	3.0 sec	1.1 sec	512 × 512 Gray Image
1024 Complex FFT	60 msec	24 msec	17-bit Fixed Point

Table 2: Execution times of the μPD7281 Image Pipelined Processor when implemented in a ring configuration.

as MIT's Tagged Token system, is accomplished via a functional language like Lisp or VAL (value-oriented algorithmic language). In contrast, conventional von Neumann computers rely on imperative languages like Fortran, Pascal, etc. In this sense, the term "imperative" refers to languages that are based on sequential execution (i.e. do this first, then this next, then ... and finally do this). Similarly, machine code of a conventional computer is also based on an ordered set of instruction sequences.

In contrast, dataflow machines use instruction graphs, and these graphs are either non-ordered or at most, partially ordered. Dataflow machines are designed with decentralization in mind, so the use of programming languages that are both less structured and easily extendible is a logical step toward this goal.

The Game Plan

In light of the Tagged Token Dataflow Architecture, a design may look good on paper, but until it is implemented it remains pure theory. MIT's plan for present and future dataflow research has four parts: (1) constructing an emulation facility, (2) emulating their proposed dataflow architecture, (3) simulating the dataflow machine and (4) implementing the architecture in a VLSI chip.

MIT has been writing a simulator that describes the internal behavior and timing of the dataflow machine at the subsystem level. The system is simulated (much slower than the speed of an actual machine) in the sense that it accepts graphs generated by the compiler. Token traffic congestion and resolution of routing conflicts in the communication network are modeled. The internal sections of the dataflow machine are not modeled (e.g., waiting-matching, ALU), but data-dependent timing can be specified.

With the dataflow simulator researchers plan to study: the size of the dataflow buffers; the size of the waiting-matching section (to reduce the chance of a token overflow); the size of the deferred read section in the I-structure storage; and the performance effects of the relative speeds of various subsystems and the communication networks. MIT is also constructing a dataflow emulation facility to complement the simulator. The emulation facility will consist of 64 artificial intelligence (AI) processors from Texas Instruments (Dallas, TX), linked together with a high bandwidth reconfigurable communications network. MIT claims the emulator should run at least 100 times faster than the simulator and will allow the study of dynamic behavior for longer time periods.

Conclusion

In terms of the future and with respect to traditional von Neumann systems: where is the concept of dataflow going?

Realistically speaking, the inertia of the von Neumann architecture gives it an overwhelming advantage over all newcomers. A 40-year software base combined with continuous honing of the von Neumann architecture makes it a somewhat permanent fixture. But considering that the overall goal of a supercomputer is to execute virtually all tasks in parallel and thus increase computational speed, there may be a limit to the capabilities of even the most sophisticated multiprocessor von Neumann machines.

In summary, the two strategies aimed at exploiting parallelism are: (1) Expanding traditional von Neumann architectures by implementing multiple processors, cache memory, instruction prefetch, etc. (2) Developing a computer architecture, such as the dataflow concept, that completely decentralizes program control and is not based on sequential processing.

Much work is currently being done in both areas and even some hybrid work which combines the two into a single system is being researched. Each game plan has pros and cons, and there is no doubt that both are striving toward the same goal. As a result, each new architecture will probably find a niche, and some of the applications that were once dominated by von Neumann computers will be performed by newer designs.

Acknowledgements

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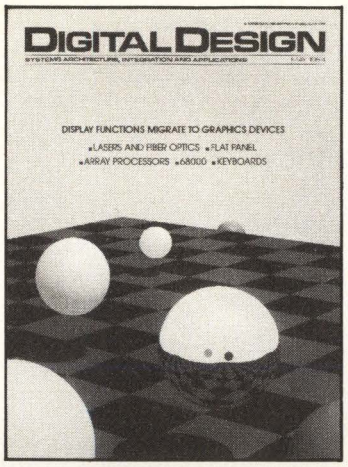

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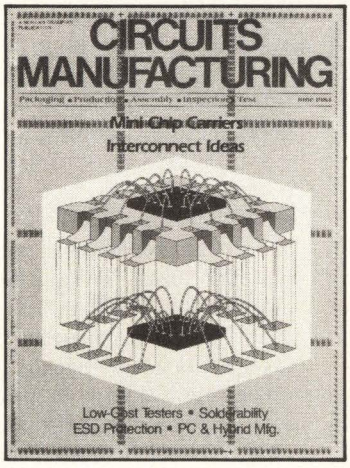

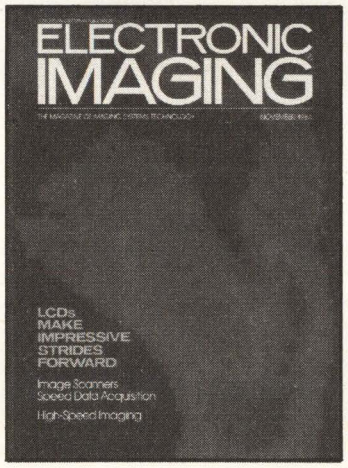

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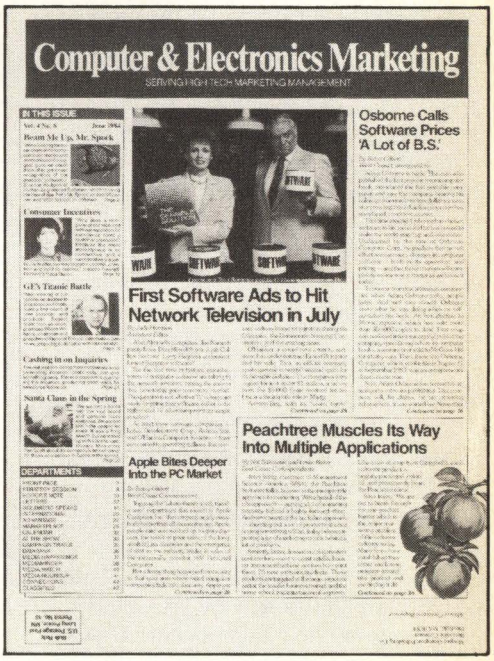

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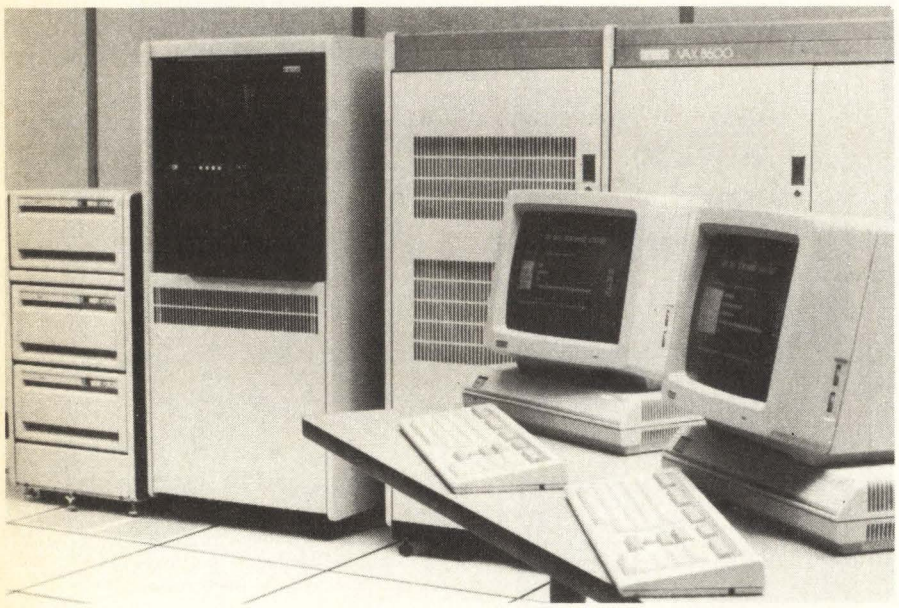

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DEC has cited three major market areas for the 8600; office, technical, and commercial. In the office market, the 8600 in clusters combined with intelligent terminals and workstations is expected to bring wider acceptance to word processing, electronic mail, spreadsheets and other general management information applications. In the technical market, the VAX 8600 and VAXclusters will be used for data acquisition; CAD/CAM/CAE, artificial intelligence and other advanced applications. In the commercial area, opportunities exist in applications such as order entry, purchasing, payroll, and general ledger.

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DEC's VAX family includes nine systems from the MicroVAX I to the new VAX 8600 system and the VAXcluster system introduced last year. Volume deliveries of VAX 8600 systems are scheduled for April 1985. The company will offer systems priced from $576,000 to $970,000 and VAXcluster upgrade configurations at $450,000. *—Hanrahan*

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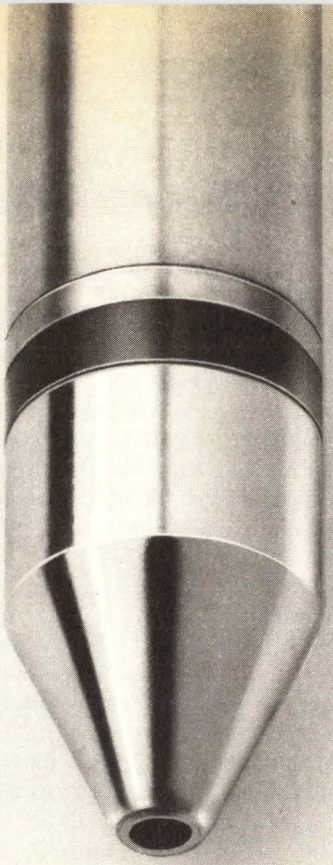

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Implementing SCSI/PLUS With The NCR 5380

The NCR 5380 may rapidly become the device of choice for implementing SCSI in mid-range performance systems. The use of on-chip bus transceivers capable of sinking 48 mA of current allows for direct connectability to the SCSI bus. Since the NCR 5380 supports arbitration and can perform both Initiator and Target role operations, it can occupy any node on the SCSI bus. Operating as a peripheral device to the controlling CPU, the NCR 5380 can be directed by reading and writing the various on-chip registers. These features combine to provide a cost-effective single-chip solution to the SCSI interface.

The ANSI X3T9.2 subcommittee is forwarding the current SCSI draft-proposed specification (Rev. 14a) into the public review period. This document, considered by many to be the final draft, is being used as the design manual for many SCSI implementations. Ampro Computers, Inc. (Mountain View, CA) is proposing a general enhancement to this SCSI specification which allows the bus to operate as either a single- or multi-master high speed parallel bus, capable of accessing up to 64 modules. This new bus structure is referred to as SCSI/PLUS™. **Table 1** describes the new types of devices that may now be added due to the enhanced SCSI definition.

SCSI/PLUS provides three functional additions to the SCSI specification which allow the bus to operate as either a loosely coupled distributed system bus or a low cost single master I/O bus. As proposed, SCSI/PLUS is a superset of the original SCSI specification, and its operation will not interfere with any existing SCSI implementation.

To allow for more complex system configurations, SCSI/PLUS provides a Binary Arbitration and a Binary Selection phase. The data bus carries a binary address and accommodates 64 physical bus devices compared to eight in the current specification. In addition, four logical units may be associated with each bus device, for a total of 256 directly addressable logical bus devices (**Figure 1**). As in the existing SCSI specifications, implementation of the Binary Arbitration phase is optional.

In addition to increasing the number of bus devices, the SCSI/PLUS Binary Selection Phase also allows a cost-effective non-arbitrating use of SCSI/PLUS, consisting of one bus master and a number of slaved targets. This single-master configuration allows the design of SCSI/PLUS targets which have no on-board intelligence, unlike normal SCSI targets. An optional interrupt protocol allows these "dumb" targets to asynchronously notify the bus master that they desire service. (This would normally require arbitrating for the bus and sending a message.)

To encourage board-level interchangability, a recommended board size and interface connector are defined. The preferred board size is the single-wide Eurocard format, with the double-wide card used as an option. The proposed interface connector is the DIN 41612 – Type C connector. By using this form-factor and connector specification, either bused backplane or ribbon cable systems may be implemented. Again, the SCSI/PLUS connector pinout is a compatible superset of the current SCSI allowing existing SCSI devices to be mixed with SCSI/PLUS devices.

The NCR 5380 is an ideal part for designing an Initiator interface to connect to SCSI/PLUS. Its simplicity provides the flexibility needed to support the defined protocol modifications and its popularity with SCSI users guarantees plug compatibility with existing host adapters.

The NCR 5380 uses the Output Data Register to assert the proper device ID onto the SCSI bus during the Arbitration and Selection phases. Since the user is not restricted in the number of bits he is

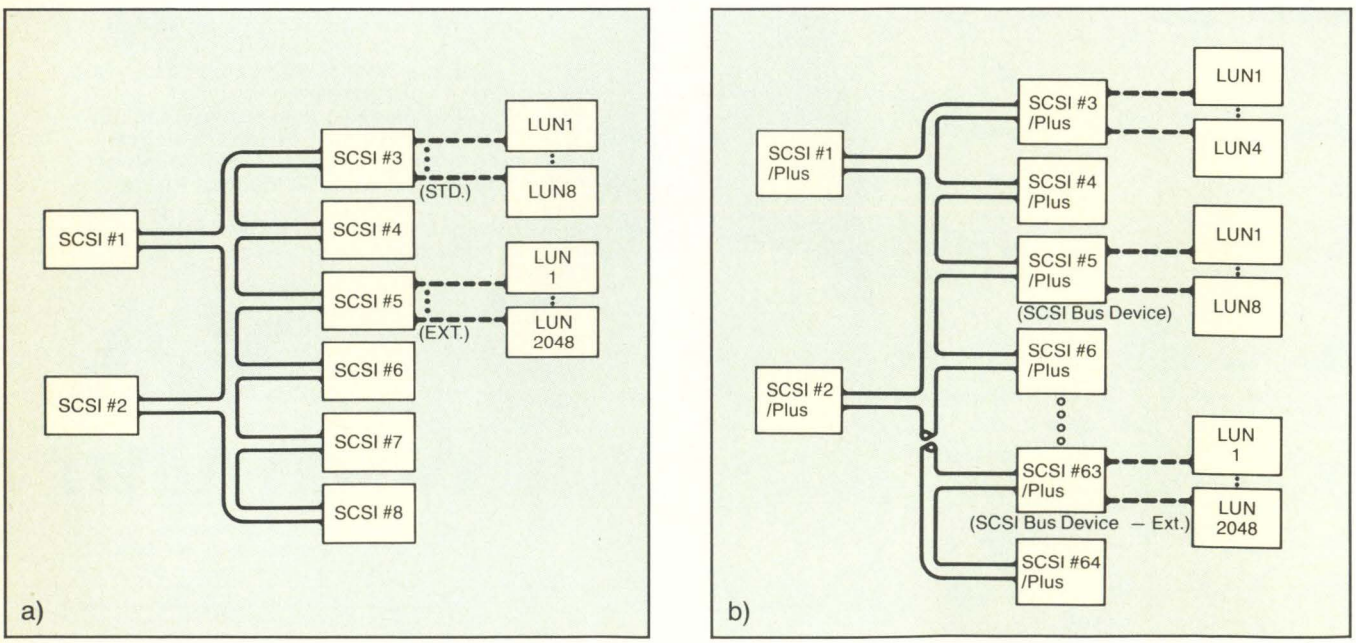


Figure 1: a) SCSI configuration showing a maximum of eight bus devices with up to 2048 logical units using extended messages. b) SCSI/PLUS configuration showing a maximum of 64 bus devices with up to 4 logical units per slave device. Note: SCSI devices may reside on the SCSI/PLUS bus.

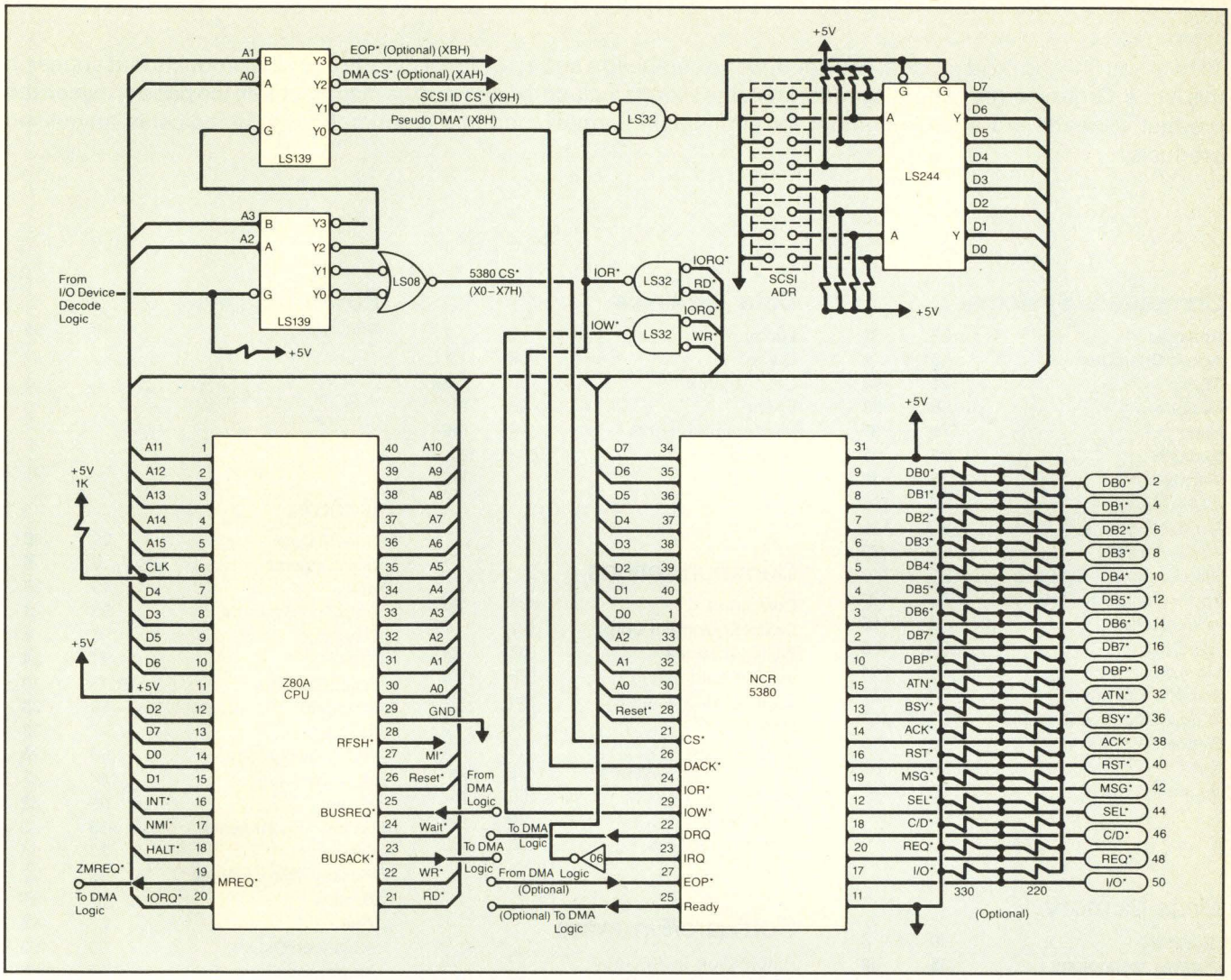


Figure 2: Interfacing the NCR 5380 to a Z-80 microprocessor.

allowed to assert on the SCSI data bus, the SCSI/PLUS Binary Arbitration and Binary Selection phases can be easily supported.

Supporting the optional SCSI/PLUS non-arbitrating system interrupt protocol requires that the bus be monitored for a specific change in status. The phase match interrupt logic within the NCR 5380 allows the device to implement this function, thus allowing asynchronous event sensing in non-arbitrating SCSI/PLUS systems.

As a Target interface, the flexibility of bus control allowed by the NCR 5380 permits it to perform either intelligent or "dumb" SCSI/PLUS target roles. As a result, a target device based on the NCR 5380 could be used in both arbitrating or non-arbitrating configurations, with a jumper or firmware option used to define

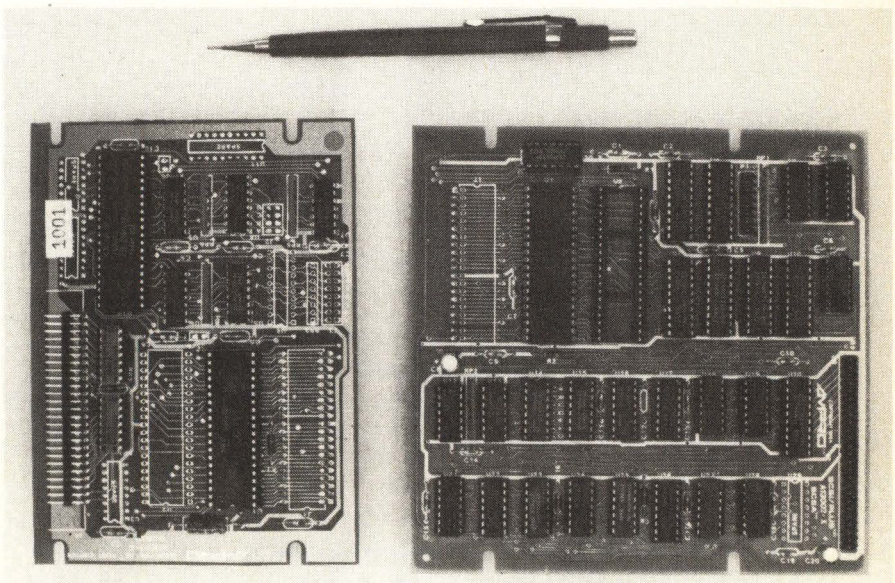


Figure 3: the SCSI/PLUS with the NCR 5380 (left) and without the NCR 5380 (right).

PRODUCT INDEX

To help you find the products that you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a circle number for additional information on that product. Bold type indicates advertised products.

the specific target mode.

As in normal SCSI implementations, the use of on-chip bus transceivers significantly reduces parts count and provides for a highly reliable, cost effective SCSI/PLUS design. An additional advantage of on-chip MOS transceivers is the low leakage current. The NCR 5380's maximum leakage current of 50 μA meets the SCSI/PLUS bus load requirements. Up to 64 devices may occupy SCSI/PLUS bus positions if low-leakage ICs, such as the NCR 5380, are used.

Figure 2 shows how Ampro interfaces the NCR 5380 to a Z80A on their Little Board computer. In this design, the NCR 5380 replaces approximately 20 TTL packages.

The SCSI/PLUS architectural concept has inherent advantages over traditional microprocessor backplane architectures. SCSI/PLUS is CPU-independent, provides flexibility of form factor, operates across a ribbon cable bus, and allows both high-performance multi-master and low-cost single-master operation. Additionally, cost-effective hardware such as the NCR 5380 is currently available, offering a fully integrated solution which is being generally accepted by the industry for SCSI-based designs. **Circle 230**

– Rich Lehrbaum, Vice President, Engineering, Ampro Computers, Inc.
– Harold Mason, Sr., Applications Engineer, Microelectronics Div., NCR Corp., Colorado Springs, CO

Using The TDC1018 And TDC1034 In A TTL Environment

The TDC1018 and TDC1034 digital to-analog converters (D/A) were designed for operation in systems that employ ECL logic families. The digital inputs to these devices are designed for direct ECL compatibility and a single power supply voltage of −5.2 volts is all that is required for operation.

There are many TTL systems that require the use of high-speed D/A converters but have only +5 Volt power supplies available. The TDC1018 and TDC1034 can easily be used in a TTL environment and this application note suggests practical circuits and clarifies some of the issues that surface.

"Normal" Operation

The circuitry of the TDC1018 and TDC1034 has been partitioned on the chip into analog and digital functions. This is done in order to optimize noise and feedthrough performance of the D/A converter. Both devices have analog and digital ground inputs as well as analog and digital power inputs.

Since the TDC1018 was designed for ECL systems, its AGND and DGND inputs normally connect to 0.0 Volts (system ground) and the power supply pins, VEEA and VEED, connect to −5.2 Volts.

The basic connections for the TDC1034 are the same but the analog and digital ground inputs have been renamed to more accurately reflect their functions. In normal ECL system operation, the VCCA and VCCD inputs of the TDC1034 connect to system analog and digital grounds respectively.

Device, Power, Ground	ECL mode	TTL mode
TDC1018		
Positive Analog Power	–	AGND pin 17
Positive Digital Power	–	DGND pin 9
Analog Ground	AGND pin 17	VEEA pin 20
Digital Ground	DGND pin 9	VEED pin 5
Negative Analog Power	VEEA pin 20	–
Negative Digital Power	VEED pin 5	–
TDC1034		
Positive Analog Power	–	VCCA pin 13
Positive Digital Power	–	VCCD pin 6
Analog Ground	VCCA pin 13	VEEA pin 16
Digital Ground	VCCD pin 6	VEED pin 3
Negative Analog Power	VEEA pin 16	–
Negative Digital Power	VEED pin 3	–

Table 1. Power and ground connections for ECL and TTL system operation.

Table 2. VIH and VIL operating conditions for ECL and TTL operating modes.

Digital Input	ECL mode	TTL mode
logic '1'	−1.045 to 0.0 V	+3.955 to +5.0 V
logic '0'	−1.49 to −5.2 V	0.0 to +3.51 V

Power Supply Connections In A TTL System

As long as the correct polarity of the power supply inputs is maintained, the TDC1018 and TDC1034 can operate from a +5.0 Volt supply as well as a −5.2 Volt supply. The D/A converter is not affected by the nature of its power supply. To operate in TTL mode, the more positive power supply inputs (AGND and DGND on the TDC1018, VCCA and VCCD on the TDC1034) connect to +5 Volts. The negative power inputs (VEEA and VEED) connect to system ground. **Table 1** summarizes the power and ground connections for the TDC1018 and TDC1034 in ECL and TTL operating modes.

Getting The TTL Data In

Since the TDC1018 and TDC1034 were designed for ECL systems, all of their digital inputs are optimized for ECL logic levels. The Operating Conditions Table of the Datasheet indicates the minimum voltage (with respect to DGND or VCCD) that can be applied to the D/A which will insure a logic '1' as VIH. VIL is the maximum voltage that can be applied which will insure a logic '0'.

The VIL specification can also be restated as "any voltage more negative than −1.49 Volts but more positive than

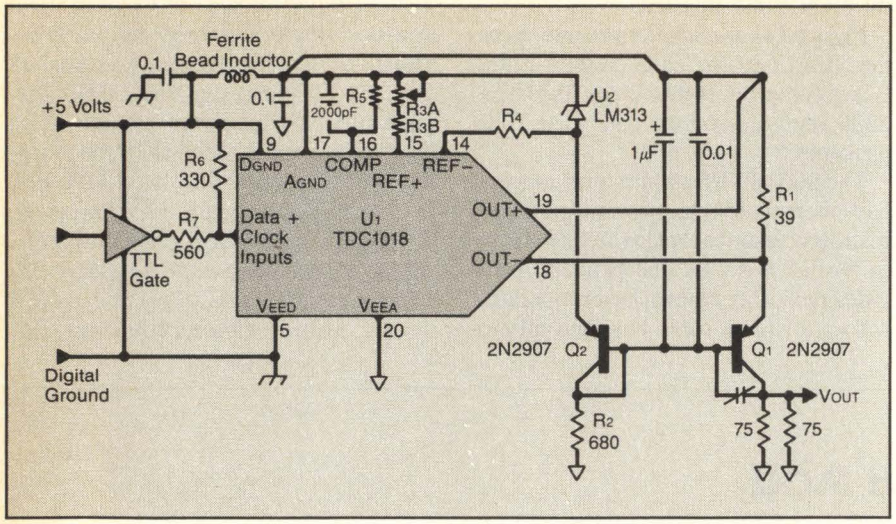


Figure 1: A suggested circuit that can be used to "turn around" the D/A output current.

VEED is a logic '0.' " Similarly, VIH can be restated as "any input voltage more positive than −1.045 Volts but more negative than DGND is a logic '1.' " These interpretations of VIL and VIH are predicated on the connection of DGND to 0 Volts and VEED to −5.2 Volts.

Since the D/A converters can be operated from a positive power supply voltage, VIL and VIH input conditions must be translated into TTL equivalents. VIL in a TTL environment becomes "any input voltage more negative than +3.51 Volts (VCC -1.49) is a logic '0.' " Similarly VIH in a TTL environment becomes "any input voltage more positive than +3.955 Volts (VCC -1.045) is a logic '1.' " **Table 2** summarizes the translation of VIL and VIH in TTL and ECL operating modes.

An appropriate way to drive the digital inputs of the TDC1018 or TDC1034 D/A converter from TTL devices is shown on the left-hand side of **Figure 1**. A resistor divider network between the TTL gate and D/A converter will insure proper input level for the D/A, with minimum VOH for the TTL gate of 2.4 Volts and a maximum VOL of 0.4 Volts.

Getting the Analog Out

The analog output structure for both the TDC1018 and TDC1034 is the same. Output current "sinks" (flows into) the complementary OUT+ and OUT− terminals. The compliance voltage limitations on these outputs are specified with respect to the positive power inputs.

In order to convert the D/A output current into an output voltage, a load resistor is connected between the output terminal and the positive power input. In a TTL system, this will create an output voltage that varies with respect to the +5 Volt supply. In some applications this is undesirable because of the variation and noise of the +5 Volt power supply.

Figure 1 is a suggested circuit that can be used to "turn around" the D/A output current and generate an output voltage that varies with respect to analog ground and is relatively insensitive to variations in power supply voltage. PNP transistors Q1 and Q2 are biased in a way that maintains a nearly constant voltage on the base of Q1. The current that flows in Q1 is the difference between the constant quiescent current set up by R1 and the voltage drop across U2, and the D/A output current flowing into the OUT− terminal.

A 1.2 Volt band-gap reference diode, U2, provides the reference voltage for the D/A converter and the bias voltage for output transistor Q1. Q2 is a diode-connected transistor which functions as temperature compensation for the emitter-base voltage of transistor Q1. Since a maximum of nearly 30 milliamps can flow through Q1, a monolithic dual PNP transistor is not recommended. Q1 and Q2 should be placed in close thermal contact.

Since the output transistor is biased with respect to the +5 Volt power supply, bypass capacitors on the base of Q1 are connected to +5 and not to ground. The sum of the currents from the outputs of the D/A converter is constant and should share a common path to VCC that excludes the reference circuitry. This will reduce the possibility of creating a signal feedback path back into the D/A.

Two performance photographs are shown in **Figures 2 and 3**. The full 1-Volt p-p output of the circuit is shown in

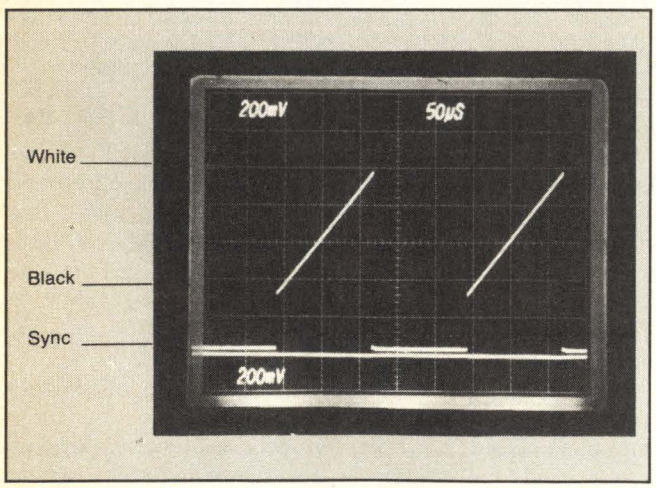


Figure 2: The full 1-Volt p-p output of the circuit.

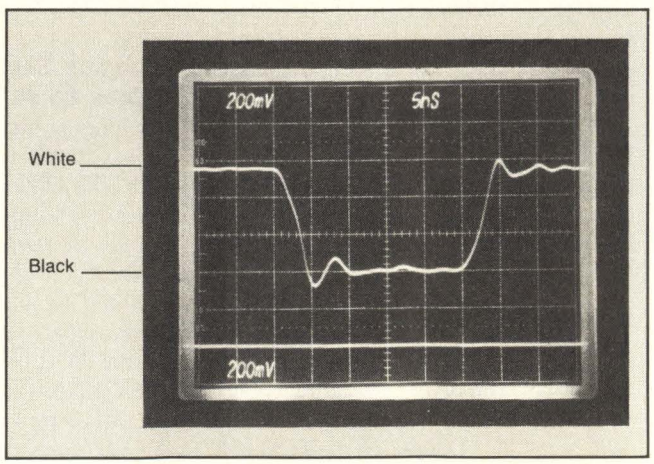


Figure 3: The dynamic performance of the circuit when it puts out a 25 nsec full-scale video pulse.

Figure 2. The ramp portion of the photo indicates the normal linear dynamic range of the D/A converter as it varies from black to white. Additionally, the SYNC input to the D/A converter is activated after the video range reaches full scale. **Figure 3** shows the dynamic performance of the circuit when it puts out a 25 nsec full-scale video pulse. The small variable capacitor between base and collector of Q1 can be used to optimize the pulse response.

Analysis Of The Current "Turn-Around" Circuit

A set of equations is helpful in tailoring this circuit for a specific application. Equations 1, 2, and 3 show the derivation of the transfer function of the circuit. Equations 4, 5, and 6 come from information presented on the TDC1018 Datasheet. The relationship between the output voltage of the circuit to the current in Q1 is given by:

$$1) \quad Vout = IeQ1 \times \left(\frac{B1}{B1+1}\right) \times R1$$

where B1 is the forward current gain of transistor Q1.

The current in Q1 as a function of D/A converter output current can be shown by:

$$2) \quad IeQ1 = \left\{\frac{VU2 + (Vbe2 - Vbe1)}{R1}\right\} - ID/A$$

where VU2 is the forward voltage drop across band-gap reference device (1.22 Volts nominally) and ID/A is the D/A output current flowing into the OUT– terminal of the D/A converter.

The transfer function of the TDC1018 D/A converter in its linear range is given by:

$$3) \quad ID/A = \left\{\left(\frac{\text{input data}}{256}\right) \times IREF \times k1\right\} + IBLK$$

where ID/A is the reference current flowing into the REF+ terminal of the D/A converter, k1 is a constant derived from the datasheet, and IBLK is the nominal D/A output current when the D/A converter outputs "black."

IREF, IBLK, and SYNC output current levels can be determined from the Operating Conditions Table and the Video Control Truth Table found on the datasheet for the TDC1018.

$$4) \quad IREF = \left(\frac{VU2}{R3a + R3b}\right) = 1.115 \text{ mA nominally}$$

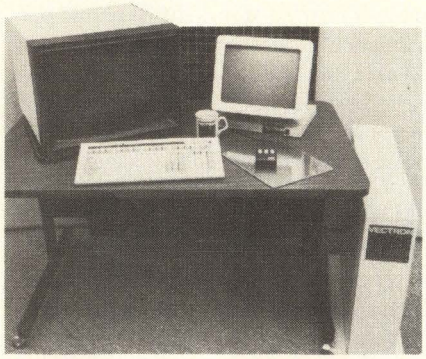
$$5) \quad k1 = \frac{\text{SYNC output current}}{IREF} = \frac{\text{IBL K} = 19.4 \text{ mA nominally}}{1.115\text{mA}} = \frac{28.57 \text{ mA}}{1.115\text{mA}} = 25.6$$

Circle 235

– Dan Watson, Manager, Applications Engineering; TRW, LSI Products Div., La Jolla, CA

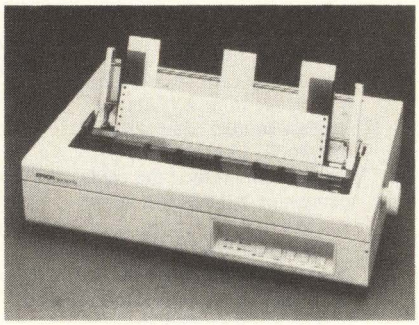
NEW PRODUCTS

Engineering Workstation



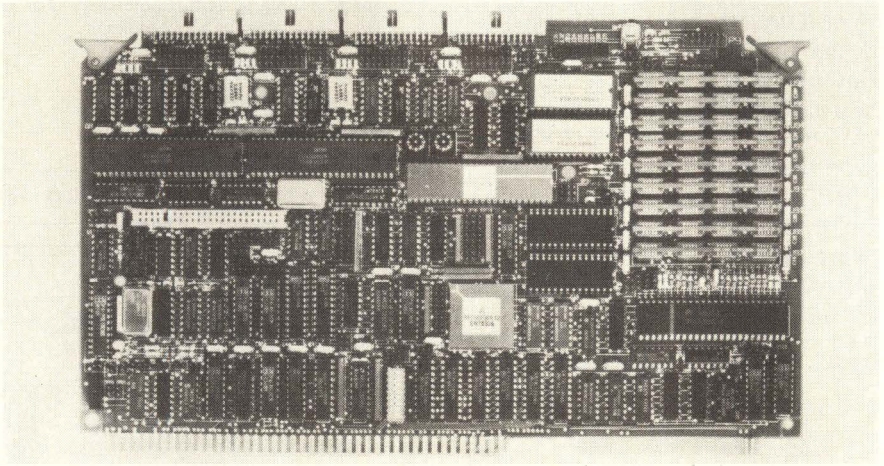
This engineering workstation called Dawn runs the VMS operating system, and can be integrated into the Ethernet or DECNet local area networks to link other workstations that incorporate file servers and analytical engines. Users can draw on the software programs already available for DEC hardware. The workstation uses two screens and is based on Q-Bus architecture. Graphics options include a 1024 ×1024 graphics monitor and a 640×480 monitor. A second graphics CRT, which is 40xx- and VT100-compatible, serves as the system console and is used for graphical and tabular system communications. The workstation contains 512 Kbytes of RAM that can be expanded to 4 Mbytes, a floppy disk and 10- or 28-Mbyte Winchester hard disk. The system includes a mouse, keyboard, and an optional digitizing tablet. The graphics controller uses semicustom hardware for graphics transformation and yields graphics rates of up to 88 million pixels/sec. Price in quantities of 100 is $30,000. **Vectron Graphic Systems,** Santa Clara, CA **Circle 147**

Ink-Jet Printer



The SQ-2000 is a drop-on-demand, ink-jet printer. It has a cleaning system which cleans the print head every few pages in a one-second-cycle at a station located at the left side of the print carriage. To correct any variance in print quality during high-volume use, the user may push a button on the front panel at any time during printing to initiate a 10-second cycle ink-line and print-head cleaning. The cleaning cycle is initiated whenever the SQ-2000 is shut-off and turned-on. The SQ-2000 prints 176 cps in draft mode, and 88 cps in letter quality mode at around 50 decibles. The SQ-2000 has character structures which include 15×17 dpi (draft), 29×17 dpi (near-letter-quality) and 37×17 dpi (letter quality). Eight print sizes are standard and the print head consists of 24 nozzles. The printer has 9 bit-image graphic modes with densities ranging from 60-to-240 dpi. Software controls intercharacter spacing print size and pitch and vertical and horizontal tabs. Price is $2,500. **Epson,** Torrance, CA **Circle 161**

2 Mbyte SBC



The OB68K/MSBC1 is a SBC which incorporates the 68000 16/32 bit microprocessor operating at 12.5 MHz on the IEEE 796. Optional microprocessors are a 10 MHz 68000 and a 68010 virtual memory processor operating at 10 MHz. The 68010 with speeds of 12.5 MHz or 16 MHz will also be optional for the board when they become available. The board comes with 256K of dual-ported RAM which uses 128K× 4 bit high density SIP chips. 512K of RAM can be implemented by adding more chips to the board. When a parity error occurs, the bank of RAM where the error originated, is identified by a circuit, with a 68230 PI/T chip. A 24-bit timer/counter is included. Four serial ports are provided by 68564 DUSART chips, and the board has sockets for adding optional memory management daughter boards. Seven levels of prioritized interrupts are supported, one of which is non-maskable. The board implements full address and bus arbitration for single and multi-processor systems and has been designed for compatibility with IEEE 769 products. **Omnibyte,** West Chicago, IL **Circle 207**

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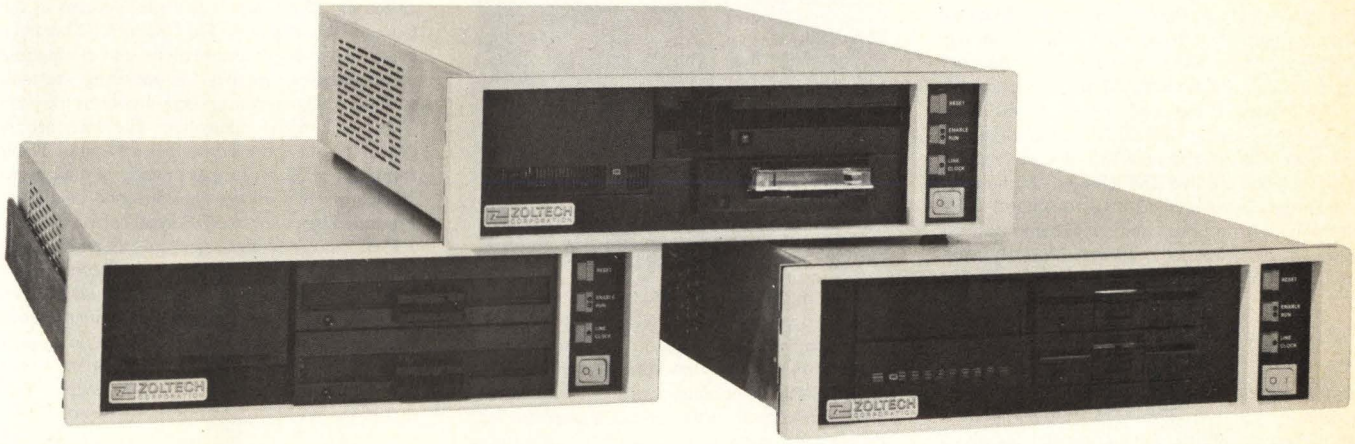

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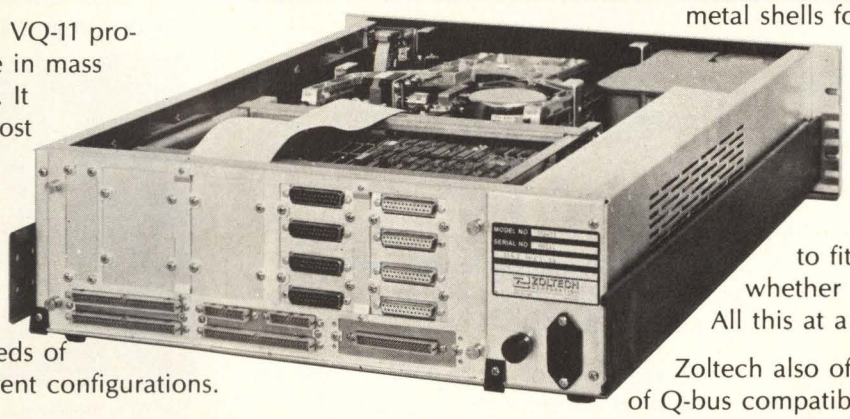
The VQ-11 series is a complete family of Q-bus system packages which is compatible with the DEC Micro/PDP-11. The VQ-11 combines all the benefits of a custom-configured system with the pricing and delivery of a standard product.

The design of the VQ-11 provides the ultimate in mass storage versatility. It accomodates almost any combination of winchester, floppy and tape drives. The three systems shown above illustrate a few of the hundreds of significantly different configurations.



The flexibility of the VQ-11 does not stop with mass storage. The 8×4, 8×2 and 4×4 card cages provide the full 22-bit Q-bus at all slots. The I/O distribution panel is compatible with the Micro/PDP-11 while providing more flexibility. In addition to the illustrated rack-mount enclosures, the VQ-11 is also available in desktop and floor-standing versions.

The VQ-11 concept encompasses a wide spectrum of Q-bus system packages from fully integrated (computer and mass storage) systems to expansion chassis for card cages and/or mass storage. Zoltech will provide the VQ-11 in configurations ranging from empty metal shells for the OEM to complete turn-key systems with peripherals and application software for the end-user.

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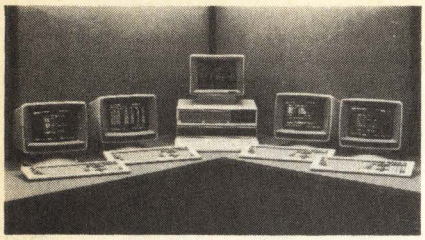
16-BIT MICROCOMPUTER

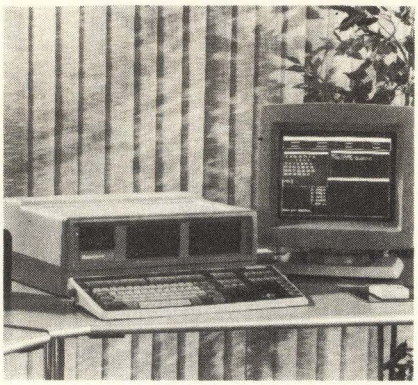


The System 2000 Microcomputer is based on the Intel 80186. The System 2000 comes with the CP/M 86 DPX and MS DOS operating systems for use with 8-bit and 16-bit software packages. The system includes the CPU and two built-in dual density floppy disk drives with a capacity of 640 Kbytes per drive. The system has a basic memory capacity of 128 Kbytes RAM and is expandable to 896 Kbytes. It has a 12″ amber monochrome video display screen with a 2000 character capacity in a 25 × 80 grid and is 640 × 400 bit-mapped. Also included are two EIA RS-232C Serial ports with programmable baud rates to support asynchronous/synchronous communications protocols at speeds of 75 bps to 19.2 kbps. **Monroe**, Morris Plains, NJ **Circle 144**

FAULT TOLERANT SYSTEM

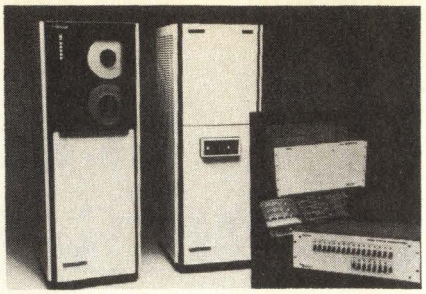
The CS330 is a fault-tolerant industrial process-control system which provides both logic and regulatory control. The CS330 consists of a motherboard, three control computer boards, a four-port serial I/O board, 14 process I/O boards and a triple power-supply unit. Each control computer board includes an 8086-2 microprocessor and an 8087-2 math coprocessor, up to 1 Mbyte RAM, up to 320 Kbyte ROM, an interboard communicator, a controller to set system parameters and an I/O interface. Incoming process signals are triplicated on the input boards and sent to each control computer board on a separate bus. Fault-detection and data integrity are achieved by having each computer read and compare the data on the other two. If one disagrees with the others, the two-out-of-three voting masks the error to assure continuous correct operation. Repeated discrepancies are reported as a need for maintenance. Price is $40,000. **August Systems**, Tigard, OR **Circle 139**

UNIX-BASED WORKSTATION



The microSystem NX workstation runs UniPlus, a licensed version of the UNIX operating system. The microSystem NX includes a window manager that allows users to view several applications. It connects with other computers in an electronic network and supports high-resolution graphics. Text processing, graphics and electronic spreadsheet applications programs also are available. The system includes a 15″ monitor, detachable keyboard, Motorola 68000 central processor, 512 Kbytes of main memory, 64 Kbytes of display screen memory, a 655-Kbyte diskette, two communications ports, and either 12 or 18 Mbytes of hard disk storage. Price is $8,895. **Honeywell**, Billerica, MA **Circle 145**

DATA AQUISITION SYSTEM



The GM/SEL 32 is a parallel interface for Preston's 13-bit and 15-bit data conversion systems to the Gould/SEL computers. The GM/SEL 32 interface provides the logic terminations and compatible driver-receiver circuitry for operating Preston's analog and digital conversion subsystems from the Gould/SEL HSD controller. The interface is available with options for either a 16-bit or 32-bit format. The 32-bit format provides a data packing feature that allows the converted data from Preston's higher speed ADC systems, 500 KHz or 1 MHz converted data rates to be assembled into 32-bit words consisting of two-15-bit conversions and transferred to the computer at a divide X2 rate. The 32 interface includes options for simultaneous sample-and-hold control, programmable conversion rate, random channel sequencing and selection of programmed start and stop modes. Price is $3,775. **Preston Scientific**, Anaheim, CA **Circle 131**

DESKTOP SYSTEM

The AM-1000X multiuser system features a 5¼″ Winchester disk drive with a formatted capacity of 55 Mbytes. The system supports from one to 11 users, utilizing the Motorola 68000 microprocessor and AMOS operating system. The AM-1000X features 128 Kbytes of memory and offers three backup configurations to choose from. Price is $12,165-$15,985. **Alpha Micro**, Irvine, CA **Circle 136**

PROGRAMMING LANGUAGE OPTION

The APL programming language is available as an option on the CIE-7800 display terminal. The CIE-7800 keyboard is reconfigurable, it can be used for APL applications with no hardware changes. The terminal allows users in mixed computing environments (IBM 3270 and DEC) to switch from one mode to another. The CIE-7800 has dedicated microprocessors to separately drive the coaxial cable interface to the IBM host, manage all the terminal internal operations, and to drive the screen display. **CIE Systems**, Newport Beach, CA **Circle 128**

LETTERS

Mr. Jim DiFilippo, Publisher
Digital Design
1050 Commonwealth Avenue
Boston, MA 02215

This letter is to express my commendation to Mr. Gregory MacNicol and *Digital Design* for a most succinct and useful article "AI Makes the Transition From Theory to Practice," *Digital Design*, October, 1984, pp. 78-86. It's the best article on artificial intelligence I've read.

As the article states, "In an era where buzz words of AI are very popular it is more important than ever to determine what is legitimate versus what is merely in vogue." In my opinion, this article is legitimate, not laughable; simple, not simplistic; complete, not incomprehensible.

WELL DONE!

Sincerely,
Tony Shuen,
Engineer,
PSE&G Research Corp.
Newark, NJ

VMEBUS DESKTOP COMPUTER

The Expert 32 is a multiprocessor computer which supports six 32-bit processor card sets and can be expanded to support as many as 12 processors. The processor card is based on the 32032 CPU from National Semiconductor and includes a floating point processor, MMU, real time clock/calendar, and 32 Kbytes of cache memory. The system has a 16 slot, double width, VMEbus backplane and comes with processor board set; 512 Kbytes of main memory, a peripheral interface card, four-RS-232 serial channels, Centronics compatible parallel printer interface; 500 W power supply; and 5¼" cartridge hard disk drives with 10 Mbytes of removable storage and 10 Mbytes of fixed storage. Price is $17,700. **Elite Computer Systems**, Wichita, KA **Circle 140**

FILE TRANSFER PROTOCOL

SPSS/PC is data analysis software that allows IBM PC/XT and AT Model 6300 users to transport SPSS portable systems files between mainframes with the SPSS-X Information Analysis System or the SAS program. The software is based on the Kermit file transfer protocol. With Kermit's terminal emulator and file transfer software residing on both the PC and the mainframe, data files can be downloaded or uploaded and automatically checked for integrity and accuracy. A copy of Kermit is included with every SPSS/PC system package. The mainframe version of Kermit tailored to handle SPSS-X system files is available to run under Prime, DEC VAX, and IBM OS or CMS installations. SPSS/PC runs on the IBM PC/XT, Compaq Plus, Corona Desktop Columbia MPC, and many other IBM PC/XT compatible systems with hard disks, release 2.0 of MS-DOS, and 320K memory. Price is $795. **SPSS**, Chicago, IL **Circle 142**

MULTIPROCESSOR SYSTEM

The Sequoia System is a 32-bit, fault tolerant computer designed for on-line transaction processing. Its architecture allows 64 processor elements, and 128 memory and I/O elements to be interconnected through dual, system buses. Each element is self-checking and new elements can be added and defective elements can be removed without interupting operations. The Sequoia System uses a fault-tolerant implementation of the UNIX operating system. Processing capability ranges from 2.5 MIPS to 50.0 MIPS. Main memory can be expanded from 4 Mbytes to 256 Mbytes. I/O capacity can be expanded from two to 96 channels, with each channel able to support up to 16 controllers. Price starts at $290,000. **Sequoia Systems**, Marlborough, MA **Circle 138**

SUPER MICROCOMPUTER

The Esprit DBS Supermicrocomputer 16 supports from one to 28 users with a network-in-a-box architecture based on the Intel 80186 microprocessor. Up to 7 80186 processors can be configured. Main memory RAM can be expanded to 3.58 Mbytes and a Multibus compatible expansion chassis is available as an option. A 5¼" Mbyte Winchester disk and an 820 Kbyte floppy disk is provided. The system runs under the MP/M-86 or Concurrent DOS 3.1 Operating Systems. Average access time is 30 Msecs. Price is $12,995. **Esprit Computer Products**, Montgomeryville, PA **Circle 137**

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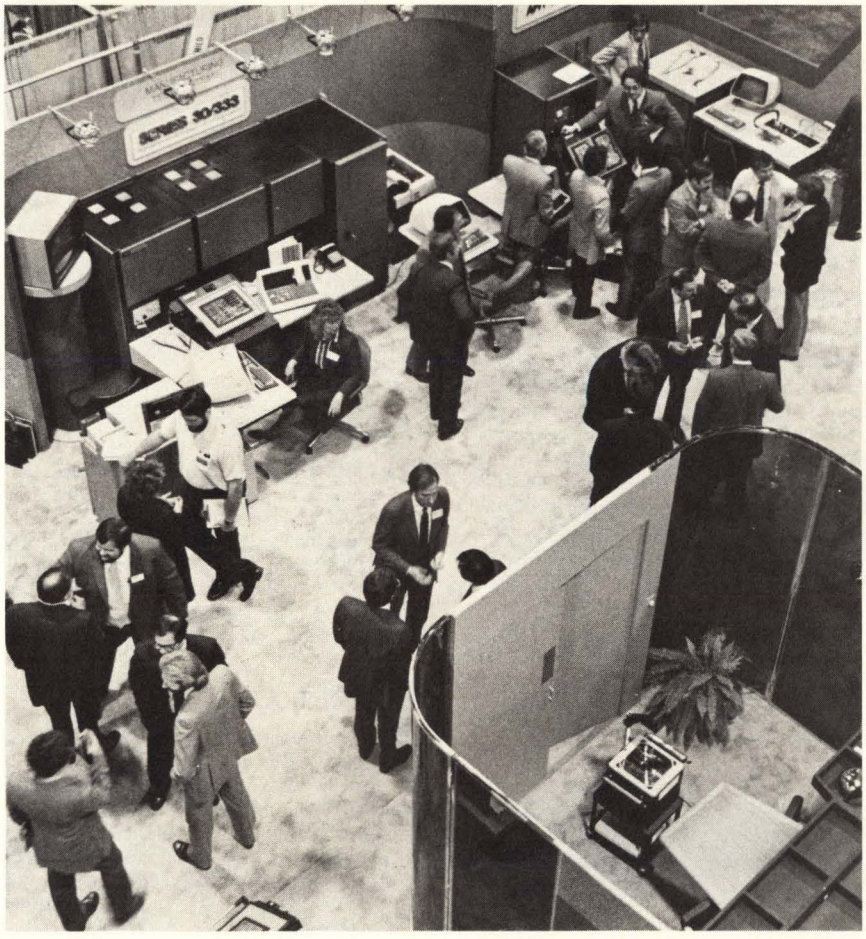

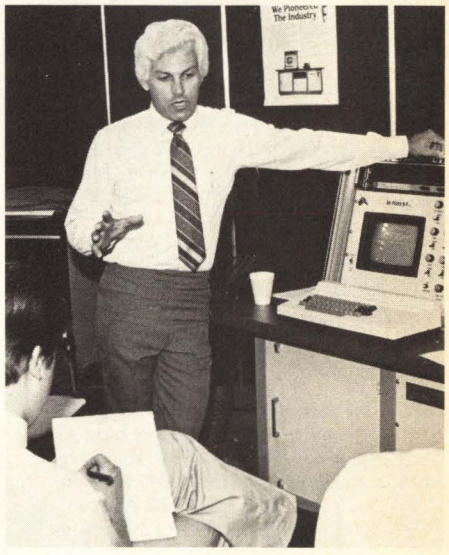

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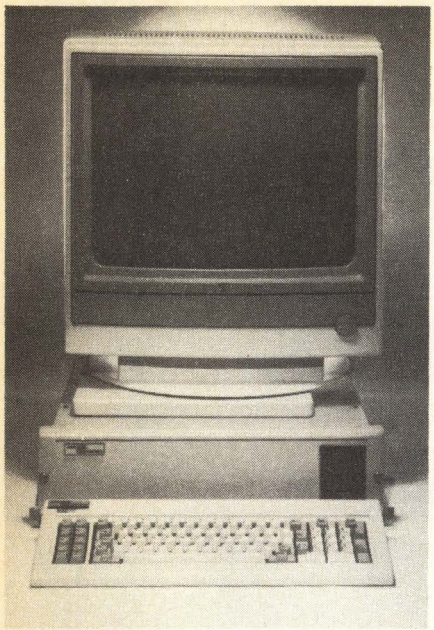
DD

GRAPHIC DISPLAY SYSTEM

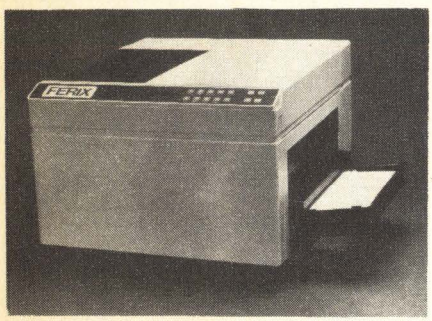


The Aycon 2010 is a single board graphics display system. The controller can be used as a stand-alone or host interactive device with Ethernet, Multibus, and Q bus compatible networking. The Aycon 2010 uses a 7220 graphics processor, with 1 Mbyte video RAM, a 8086/87 processor and has 667 nsec/pixel vector write rates. It is GKS compatible. Price is $8,500. **Aydin Controls,** Ft. Washington, PA
Circle 173

NETWORK

This updated version of FTM 3.0 connects 8000-S and ICON systems. Users can tie in workstations and share peripheral resources. FTM 3.0 supports Ethernet communications on Desktop Generation, the Eclipse S/20 and the Eclipse S/120. Any combination of 8000-S and ICON systems can be connected together in a network with a bandwidth of 10 m/sec. Features include two functions: list and print. **Summagraphics**, Fairfield,CT
Circle 182

MAGNETIC PAGE PRINTER



The Model 800 Magnetic Page Printer operates at 10 pages per minute. The printer uses a thin film magnetic head with an internal coil structure surrounded by magnetic material. The Ferix printer uses an array of magnetic head elements mounted in a substrate to generate concentrated dot images (57,600 dot/in.). Price in OEM quantities is $2,000-3,000. **Ferix**, Freemont, CA
Circle 175

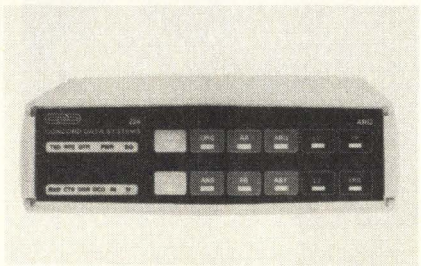
DEBUGGERS

The Pfix86, a dynamic debugger, and Pfix 86 Plus, an enhanced version with symbolic debugging and overlayed program debugging capabilities, are two recently introduced programming tools. They are designed for use in systems based on the Intel 8088/86 family of microprocessors running PC DOS and MS-DOS operating systems. Pfix86 Plus offers symbolic debugging of overlayed programs and requires the use of Phoenix's Plink86 linkage editor. It features a multiple-window display for simultaneously viewing program code and data, breakpoint settings, current machine register and stack contents. Breakpoint capabilities include permanent and temporary settings, an in-line assembler, and single-keystroke tracing. Price is $195 (Pfix86) and $395 (Pfix86 Plus). **Phoenix Computer Products**, Norwood, MA **Circle 174**

GRAPHICS SOFTWARE

InFoCen is based on a relational database management system. The graphics module, IFC Graphix, is based on DI-3000, a CORE standard set of routines. These routines have been integrated into InFoCen. A graphics library can be established and produce subsequent graphs using these stored symbols. The text file feature allows for custom graphic formatting of textual data. The user may select from several colors, type fonts, character spacing and sizes. These selections are applied toward a file the user wishes to format or a file may be built. **3CI**, Ft. Collins, CO
Circle 157

2400 BPS MODEM

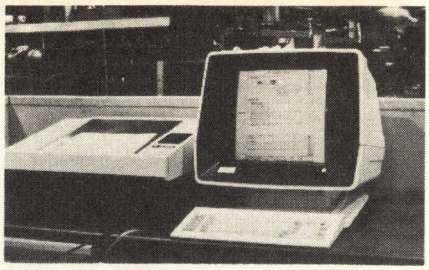


The CDS 224 ARQ is a 2400 bps full duplex modem with ARQ error correction. The modem is equipped to detect if a remote modem is not similarly equipped with an ARQ, or is a Bell 212 type, and automatically adapts itself accordingly. Error recovery utilizes a bit synchronous protocol and an adaptive equalizer. Diagnostics include Loop 2 and Loop 3 and an internal test pattern generator and checker. Price is $1,295-$1,395. **Concord Data Systems**, Waltham, MA
Circle 180

MICRO TO MAINFRAME NETWORK

DeskNet allows users to access application processors, whether they are internally installed mainframes, minicomputers, microcomputers, or outside processing services. Processing resources are shared by users on the network. The DeskNet/Workstation has inter-application cut and paste, user support systems and the ability to emulate multiple terminals. When attached to the DeskNet/Network, the network determines what resource a specific application resides on, and connects the user with that machine. DeskNet is targeted at NCR mainframe users. **Century Analysis**, Pacheo, CA **Circle 178**

EDITING CAD WORKSTATION



The editing workstation stores and retrieves documents, provides design and revision capabilities and transmits records from installed CAD systems to film and paper. The workstation is comprised of four components: an aperture card scanner with Hollerith code reading capability; a high-resolution display terminal; M68000 and IBM PC-XT processors for image panning, zooming, rotation, raster and vector editing; and a laser printer. Price is $63,000-$98,000. **Tera**, Berkeley, CA
Circle 166

MEMORY BOARDS

The 1 Mbyte iSBC 010CX and 2 Mbyte iSBC 02CX are memory expansion boards which have on-board ECC and one wait-state performance when used with Intel's iSBC 286/10 CPU board. The iSBC 010CX and 020CX use 256K DRAM microchips. A single iSBC 020CX can replace up to four 512 Kbyte boards. Price is $4,750-$8,250. **Intel**, Hillsboro, OR **Circle 196**

I/O CONTROLLER

The AM-316 controller provides 16 RS-232 serial ports and one Centronics-compatible parallel port on a single S-100 board. The AM-316 include a watchdog timer and a reboot on break key function. Both are jumper selectable. The AM-316 has 18 software-selectable baud rates, selectable by port. Price is $1,325. **Alpha Micro**, Irvine, CA
Circle 190

300/1200 BAUD MODEM

The Signalman Express is a 300/1200 baud modem. Features include audio line monitor speaker, autodial, analog loopback self-test, GSTN configuration switches and dedicated line operation. The modem operates either unattended or manually through switch selections, and with standalone terminals and computers. The line interface is two-wire direct connect, with full or half duplex select. Data interface is RS-232. The transmit carrier level is a fixed -10 dBm, with the carrier direct ON at -43 dBm and OFF at -47 dBm. Line monitoring is via audio speaker and/or screen prompt. **Anchor Automation,** Van Nuys, CA
Circle 170

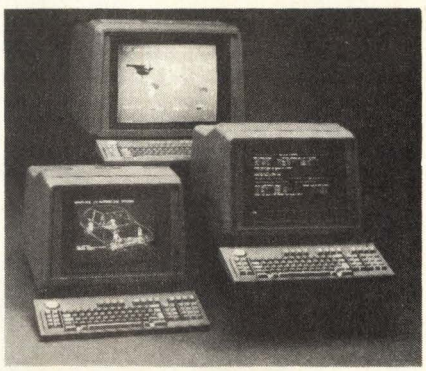
26-MBYTE HALF-HEIGHT WINCHESTER

The Shugart 724 is a 26 Mbyte half-height 5¼"Winchester disk drive with a closed-loop servo septim. Features include four-point shock mounts, dynamic spindle brake and an actuator which automatically retracts the read/write heads to a dedicated head landing/shipping zone when the drive is powered down. The 724 printed circuit board includes four custom LSI devices to handle the drive's R/W, I/O and servo functions and two 8-bit microprocessors to control the spindle and stepper motors, perform buffered seeks and execute diagnostic functions. Price in OEM quantities is $500. **Shugart**, Sunnyvale, CA **Circle 172**

LOCAL AREA NETWORK

3Com's LAN hardware and software supporting MS-DOS 3.0 are fully compatible with networked IBM PCs, PC/XTs, IBM-compatibles, Hewlett-Packard 150s and Texas Instruments Professionals running MS-DOS 2.0 and 2.1. Users can link the IBM PC AT to networked application software, disks and printers.The PC AT can be used as either a network server or workstation. **3Com**, Mountain View, CA **Circle 179**

COLOR GRAPHICS TERMINALS



The Tektronix 4100 Series of computer display terminals are now IBM 3270 plug-compatible. The CX4100 Series provides direct coaxial connection to an IBM 3274 cluster controller, as well as 32-line 3278/3279 alphanumeric emulation, an IBM-style keyboard, and a range of drivers for peripheral devices. The CX4100 Series terminals have a 60 Hz non-interlaced display with 4096×4096 addressability in a 640×480 matrix; can draw solid or dashed lines in 16 colors using eight line styles; 11 marker types; zoom and pan; user-defined fonts and macros; and local picture storage. The series also supports VT100 extensions and ANSI X3.64 editing and word processing standards. Price is $7,950-$13,305. **Tektronix**, Beaverton, OR **Circle 162**

GRAPHICS WORKSTATION

The Qubix workstation features a 2240 × 1680 resolution for CAD applications. It has a 19" screen, continuous panning, zooming and scrolling and an editing feature which allows art and text to be edited simultaneously. Refresh rate is 60 Hz interlaces and horizontal rate is 52.7. The workstation has an adjustable alphanumeric keyboard, digitizing pen and also allows users to draw on the face of the screen directly. **Quibix Graphics Systems**, Saratoga, CA **Circle 167**

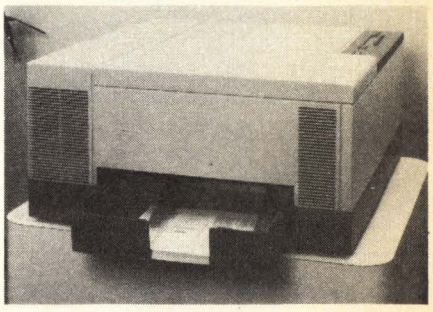
DIGITIZER

The micro Digi-Pad digitizer includes self-diagnostics for testing of the tablet, cursor, stylus, buttons and lock height. The diagnostic results are visually indicated by an LED on the rear panel of the Micro Digi-Pad which locates the active area. The self-diagnostic capability is standalone, allowing the Micro Digi-Pad to be tested off-line from the computer and without any special tools. **GTCO**, Rockville, MD **Circle 164**

SOLIDS MODELER

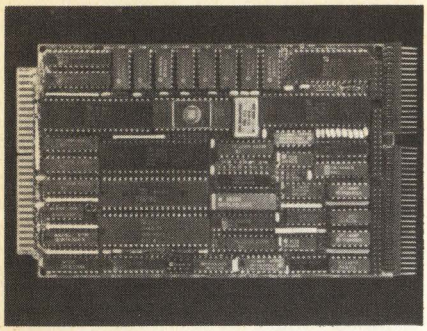
The Cimplex module set is comprised of mechanical parts design, mechanical parts analysis and mechanical parts manufacturing. The product set operates in the VM/CMS environment. The mechanical parts design module permits designers to drill and tap with user-familiar commands. The mechanical parts analysis module generates finite element meshes and sets analysis parameters. The mechanical parts manufacturing has an interactive two-to-five axis capability for multi-path pocket milling. The information management module is used to collect the design and engineering data, perform configuration management and maintain centrally located drawing files from a multiplicity of CAD systems. Price is $100,000. **Automation Technology**, Campbell, CA **Circle 159**

INK-JET PRINTER



The Dijit 1 is an ink-jet printer which has a resolution of 300 dpi and prints 18 pages per minute. Features include 128 Kbytes of buffered RAM storage, resident font set, duplex printing, Centronix interface and Xerox 2700 emulation. The printer has two operating modes. Quality mode prints at a resolution of 300×300 dpi and draft mode operates at 18 pages per minute. Price is $5,000-$7,500. **Diconex**, Dayton, OH **Circle 171**

Z80A-BASED SBC

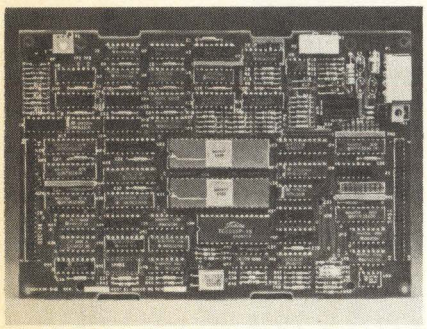


The ISB-3104 is a Z80A-based microcomputer for use with STD Bus Systems. The ISB-3104 is available with either 64 or 25 Kbytes of dynamic RAM and a 28-pin socket for up to 32 Kbytes of ROM, EPROM or EEPROM. It includes four counter/timer channels, two RS-232-C serial data channels, 16 parallel I/O lines, a Centronix type printer interface, DMA controller and a floppy disk controller that will handle a combination of four 8″, 5¼″ or 3½″ drives. The ISB-3104 runs at a 4 MHz clock rate and is provided with a bidirectional bus interface for memory access to on-board and off-board DMA controllers. The ISB-3104 is supported by the CP/M 2.2 operating system and can be used with systems that include up to four floppy disk drives and/or a 10 Mbyte hard disk drive. Price is $750. **ISI International**, Sunnyvale, CA **Circle 206**

TOUCH SENSITIVE PANEL

The touch sensitive panel is a transparent, pressure sensitive panel mounted on the face of a terminal CRT. It is available in 9″, 12″, 13″, 15″ and 19″ sizes and has a touch force of 14 to 28 grams. Interface cards are available for serial and parallel data input. The interface card translates touch locations into RS-232C type serial output and provides a baud rate of 110 to 9600, selectable parity and 10-or 11-bit frame length. The touch panels are available with optional antiglare surfaces of green or yellow. **Detector Electronics**, Minneapolis, MN **Circle 205**

¼″ STREAMING TAPE CONTROLLER



The WD1036-SHD Controller supports ¼″ streaming cartridge tape drives and links the SASI interface to the QIC-36 interface. The WD2400 chip set provides tape motion control, buffer management and R/W formatting. The controller has a 16-bit CRC error detection code and a read-after-write data verification algorithm. A ping-pong buffer eliminates latency problems during backup. Price is $295. **Western Digital**, Irvine, CA **Circle 199**

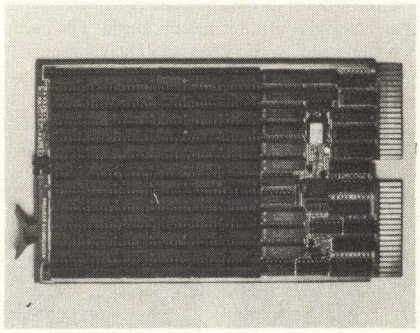
X-Y DISPLAY MODULE

The LBO-51MA X-Y display module has an 8 × 10 cm aluminized, post deflection acceleration CRT. An internal 8 × 10 graticule is optional. Input sensitivity is adjustable from 50 to 150 mV/cm and the X and Y axis bandwidth is 3 MHz (-3 dB). The input coupling (AC or DC) and polarity can be selected by internal switches. The Z-axis (intensity modulation) input has a bandwidth of 4 MHz. Price is $995. **Leader Instruments**, Hauppauge, NY **Circle 189**

20K GATE ARRAY

The HGC20000 is a 20K gate CMOS gate array for the soon to be available ETA Systems Supercomputer. It is fabricated using 1.25 micron CMOS-III technology. The HGC20000 has 600 psec unloaded gate delays at 25°C. A design using 15,000 gates of the HGC20000 dissipates 2 W of power. It incorporates a form of serial-set-scan testing for system and chip fault detection and rerouting. The array interfaces with LSTTL or CMOS logic. **Honeywell**, Minneapolis, MN **Circle 209**

MEMORY BOARD



The MM11 is a 2 Mbyte dual width module with a typical access time of 30 nsec in block transfer mode. The MM11 is compatible with 256 Kbyte and 64 Kbyte DRAM for maximum capacities of 2048 Kbyte and 512 Kbyte respectively. The MM11 requires 1.0 A at +5 volts. The memory includes user programmable jumpers for 22- or 18-bit addressing, 16 or 256 word block mode capability, 4 Kbyte or 2 Kbyte word I/O page, standard or optional CSR address, CSR disable and parity logic disable. Price is $1,295. **Andromeda Systems**, Canoga Park, CA **Circle 188**

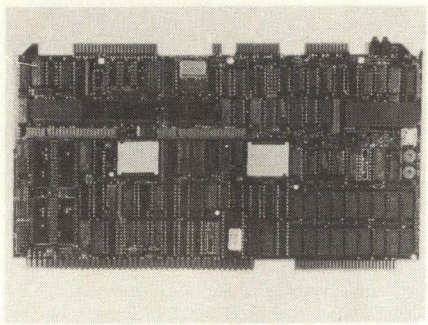
½ MBYTE BUBBLE MEMORY

This ½ Mbyte bubble memory cartridge is a removable device with non-volatile magnetic storage. Other cartridges include bubble memory versions with memory capacities of 128, 256 and 384 Kbytes. CMOS RAM data storage cartridges are available in 16 and 64 Kbyte capacities. All the cartridges are interchangeable and compatible with Targa's family of bubble memory data storage systems. Price for the ½ Mbyte cartridge starts at $2,495. **Targa**, Ottawa, Ontario **Circle 211**

MATH PROCESSOR BOARD

The CIM-550 math processor board is available in 2 MHz or 4 MHz versions. The CIM-550 contains an Am 9511 math processor chip which can implement transcendental math functions, such as trigonometry and logrithms. The board supports power switching under CPU control and operates in the temperature range of -40°C to +85°C. A commercial version, the CIM-550C, operates from 0°C to +70°C. Price is $1,025. **National Semiconductor**, Santa Clara, CA **Circle 208**

MULTIBUS BOARD



The ZX-186/30 is an iAPX-186-based single board computer. The board has 1 Mbyte RAM, 128 Kbyte PROM, a dual USART, 24 parallel I/O lines, two DMA channels, two iSBX connectors and timers and interrupts. The board is iSBC-86 compatible. Memory capability is based on the 8207 dynamic RAM controller and either 4164, 64 Kbit DRAMS or 41256, 256 Kbit DRAMS. With the 4164 the ZX-186/30 has 128 Kbyte dual-ported RAM with parity. The expansion module can double the ZX-186/30's on-board memory to 256 Kbyte. The ZX-186/30 supports two iSBX interfaces and DMA channels can be configured for the iSBX connectors. Price in quantities of 100 is $340-$2,500. **Zendex**, Dublin, CA **Circle 192**

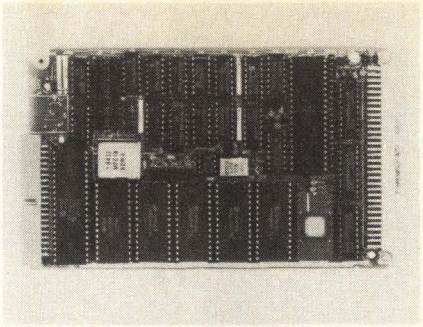
19″ RASTAR DISPLAYS

The GMA201 monochrome raster monitor and the GMA302 and 303 color raster monitors are recent introductions from Tektronix. The GMA201 has an addressable resolution of 2048 × 1536 pixels and a 60 Hz non-interlaced refresh rate. The GMA302 has 1024 × 768 addressable pixels with a 60 Hz non-interlaced operation. The GMA303 has a 1280 × 1024 addressable resolution with 60 Hz non-interlaced refresh rate and has an in-line gun CRT and dynamic convergence. Price is $3,380-$3,995. **Tektronix**, Beaverton, OR **Circle 200**

DISPLAY CONTROLLER

The EG7001A-AR LCD graphic module has a viewing area of 9″ wide by 3″. The EG7001A-AR has a display capacity of 640 × 200 dots or, by using a 5 × 7 alphanumeric format, 25 lines by 80 characters. The module uses a TN-FEM positive reflective display mode and a 1/100 duty cycle. Typical response time is 180 msec. Dot size is 0.35 mm by 0.35 mm (0.014″ × 0.014″). A single +5.0 volt and -13.0 volts power supply is standard. Price is $325. **Epson**, Torrance, CA **Circle 194**

EUROCARD SBC

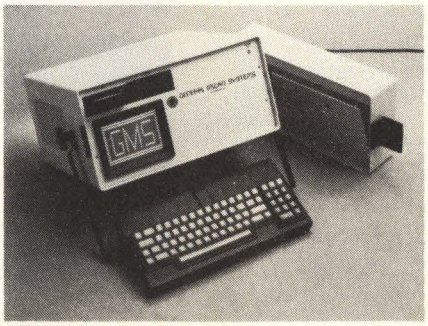


The model DSBC 09 is a Eurocard SBC which uses a 6809 CPU and has 34 Kbyte of CMOS memory. The module, has an RS-232C serial port with programmable baud rates from 50 to 19,200 bps. Two 8-bit parallel ports are supplied. On-board memory includes 2 Kbyte of bootstrap memory plus space for 32 Kbyte of RAM/PROM. The DSBC module can be operated with 6809 or 6502 microprocessors or with CMOS 65C02, 65C102 or 65C112 CPUs. The 100 × 160 mm module is supplied with a 64-pin DIN connector. The module can be expanded with RM 65 modules such as digital and analog I/O and peripheral controllers. Price in quantities of 25 is $275. **Dynatem**, El Toro, CA **Circle 191**

CMOS OPERATIONAL AMPLIFIER

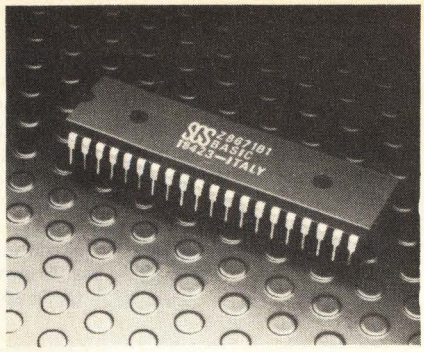
The TSC7650A chopper stabilized operational amplifier has a 5 micro-volt maximum offset voltage specification. The TSC7650A is pin compatible with the ICL7650 device but has a 2.5mA maximum supply current specification. The TSC7650A nulling scheme corrects DC offset voltage error and offset voltage drift with temperature. The amplifier has a 15pA maximum input bias current specification and a 1V common mode signal. Operating from ± 5V supply, the common mode voltage range extends from -5.0V to 1.5V minimum. **Teledyne Semiconductor**, Mountain View, CA **Circle 186**

PROGRAMMABLE INDUSTRIAL CONTROLLER



The GMS 68K is a programmable industrial controller based on the 68008 10 MHz CPU. It includes a CRT display, environment-proof keyboard and disk drives. All inputs and outputs are through a rear connector panel. The controller accepts/controls 256 analog channels and interfaces with IEEE-488 instruments and digital I/O in multiples of 80 lines. It can control up to 16 channels of optically isolated AC/DC I/O and a range of input levels. Price is $3,500-$4,000 **General Micro Systems** Ontario, CA **Circle 204**

BASIC/DEBUG INTERPRETER



The 28671 is a standalone MCU which includes a pre-programmed BASIC/Debug interpreter. The interpreter features built-in RAM I/O and a subset of Dartmouth Basic resident in the internal 2K ROM memory. The single-chip interpreter operates at speeds of 8.0 MHz and 12 MHz. Temperatures range from 0° C to +70 C° and -40 C° to +85 C°. Interaction between the interpreter and the user is provided through an on-board UART. BASIC/Debug allows hardware tests, examination and modification of memory location or I/O ports, bit-by-bit examinations of ports, bit manipulation and logical operations. The BASIC/Debug interpreter processes decimal and hexadecimal values for input and output. Price in quantities of 100 is $15. **SGS Semiconductor**, Phoenix, AZ **Circle 198**

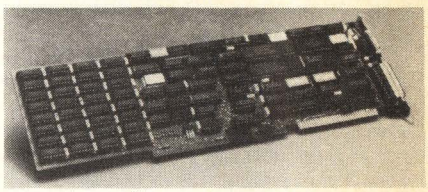
CONTROLLERS

The Series 400 system controllers provide 32 asynchronous ports in addition to 3270 communications. Asynchronous transmission rates are 9600 bps, with XON/XOFF; 3270 transmission rates are 7200 bps, with optional speeds up to 56K bps. The Model 410 has a remote 3270 interface and allows asynchronous communications through DEC VT52, VT100, VT132 and HP 2624 point-to-point emulations. With local channel interface, the Model 420 provides 16 devices with local access to IBM or IBM-compatible hosts. Price is $14,820-$19,520. **Lee Data**, Minneapolis, MN **Circle 165**

IBM-MULTIBUS INTERFACE

This board level product from Intel is Multibus-based and will support the IBM 4361 processor-attatchment capability. An Intel Multibus adapter board and the SOEMI feature on the IBM 4361 enables users to gain access to Multibus hardware and software. The SOEMI is a standard feature on the 4361 processor family. It enables 370 programs running on the IBM 4361 to communicate with Multi-bus-compatible systems attached to the SOEMI. Physical connection is made by attatching Intel's Multibus adapter board to the IBM 4361's display-printer adapter or work station via a standard coaxial cable. This connection can link systems over a distance of up to 1.5 K meters. The maximum burst data rate is 2 Mbits/sec. **Intel**, Hillsboro, OR **Circle 156**

PROCESSOR BOARD



The PC-slave/16 is an 8 MHz, 16-bit, single board processor. It contains an Intel 8088 CPU, 256 Kbytes of dynamic RAM, PC bus interface, and two serial ports. The PC-slave/16 is hardware/software compatible with the IBM PC and compatible systems. Software permits the processor to run PC-DOS, MS-DOS, or CCP/M. Individual programs running on a slave can directly access files. RTNX provides file/record locking with controls for file access management. Price is $1,095. **Advanced Digital**, Huntington Beach, CA **Circle 193**

256K DRAM DESIGNER KITS

This 256 Kbit DRAM designer kit from Hitachi uses 2-micron design rules to produce DRAMs with access times of 120 to 200 nsec. The devices consume 350 mW while active and 23 mW while on standby. The DRAMs require a five-volt power supply, come in either plastic or ceramic 16-pin dual in-line packages and are TTL compatible. Price is $109.95-$124.99. **Hitachi America**, San Jose, CA **Circle 212**

PROTOCOL CONVERTER

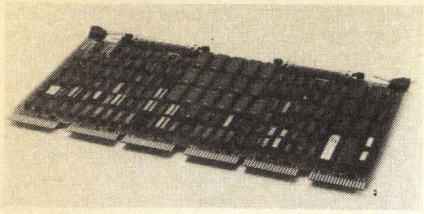
The Comten Integrated Protocol Converter converts asynchronous ASCII protocol to BSC 3270 protocol and can be installed in a local or remote Comten 3600 communications processor. Users operating the MAF/RHO can use asynchronous devices to access IBM BSC 3270 emulation in host computers of other vendors. The IPC supports protocol conversion for 32 asynchronous lines and is available in 8, 16, 24, and 32 line versions. Price is $6,100-$15,450. **NCR Comten**, St. Paul, MN **Circle 169**

LASER PRINTER

The Concept Laser 8 printer integrates text and graphics. It is compatible with the VDI and industry graphics standard recently incorporated by IBM in its graphics products. The Laser 8 operates at eight pages per minute and 300 dpi. The Laser 8 prepares camera-ready documents in several fonts and paper types including postcards and transparencies. A multiuser option permits one printer to support up to four users. Price is $7,995. **Concept Technologies**, Portland, OR **Circle 158**

NEW PRODUCTS

MULTIPLEXING CONTROLLER



The Optimux/16DMF+ is a multiplexing controller for use on PDP-11 and VAX computers. 16 peripheral devices can be connected from a single backplane slot. The Optimux/16DMF+ offers a software-selectable choice of data transfer rates, from 50 bps to 34,800 bps. The Optimux/16DMF+ is software compatible with the LCDRIVER contained in the VAX/VMS OS. It is compatible with modems that support auto-answer capabilities and supports local terminal connections compatible with EIA RS-232C or CCITT V.24. It is connected via two 50-conductor flat ribbon cables and provides connections for 16 RS-232C compatible devices. Price is $3,000. **Dilog**, Anaheim, CA **Circle 187**

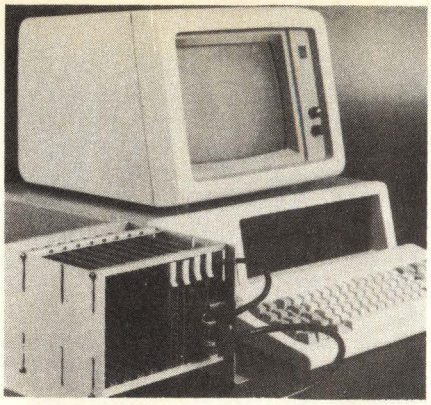
STD BUS BOARDS

The MP6421 Universal EPROM programmer, the MP6311 IEEE-488 interface and the MP6394 intelligent parallel I/O board are three STD bus compatible boards. The MP6421 EPROM programmer programs +5 volt EPROMs conforming to the standard JEDEC package (2758, 2716, 2732, 2764, 27516, etc.). Tri-supply EPROMs may be read only. The MP6311 is an IEEE-488 GPIB to STD bus interface, and is designed to provide data communications between the STD bus and the IEEE-488 bus. The board is compatible with most processor standards for the STD bus and is software programmable for IEEE-488 talker, listener or controller modes. The MP6394 intelligent parallel I/O board provides 32 bits of input and 8 bits of output for STD bus systems, and is designed for digital data acquisition and intelligent controller applications. Price is $320-$410. **Burr-Brown**, Tucson, AZ **Circle 202**

SIGNAL GENERATOR

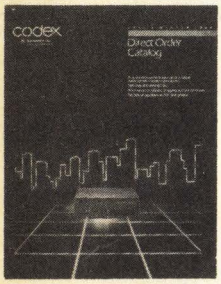
The 6060A Synthesized Signal Generator tests RF receivers, filters, amplifiers and mixers. It covers a frequency range of .1 to 1050 MHz, selectable with 10 Hz resolution and has a switching speed of 100 msec typical. Non-harmonic spurious products are around -60 dBc, and harmonics are -30 dBc across the frequency range. Amplitude levels are selectable from -137 dBm to +13 dBm with 0.1 dB resolution. The frequency synthesizer is divided into two blocks: a main phase-lock loop for generation of coarse-resolution digits, and a subsynthesizer for fine-resolution digits. Two custom LSI gate arrays are used in the 6060A to integrate the subsynthesizer, and the digital portions of the main loop. Price is $4,500. **John Fluke Mfg.**, Everett, WA **Circle 210**

LAN INTERFACE CARD

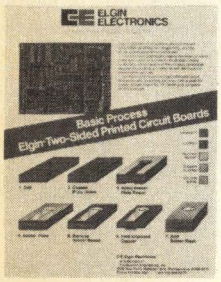


The NETPC/STD is a LAN interface card designed for industrial control applications in hostile and/or dispersed installations. Based on the WD2840 VLSI LAN controller from Western Digital, the STD bus compatible interface card uses a token bus protocol similar to ARCNET. Cable lengths of 1000′ between nodes are permitted without repeaters, and 10,000′ may be included in the complete system. All application software can be written on the IBM PC, as though the interface cards in the remote STD system were located within the PC itself. This is through C language subroutines which access the remote I/O ports in the STD system. Price is $495. **Beal Communications**, Dallas, TX **Circle 201**

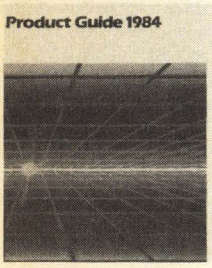
NEW LITERATURE



Data Communications Catalog. This direct order catalog from Codex Corp enables data communications users to order products which they install themselves. The catalog features two new products; the Codex 5202 and 5202R Data Modems, plus cable and statistical multiplexers, limited distance modems, high speed modems and cable and Bell compatible modems. A glossary of definitions is also included.
Codex **Circle 262**

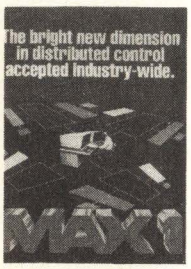


Printed Circuit Board Bulletin. The basic fabrication process of a two-sided printed circuit board is depicted in this bulletin from Elgin Electronics. Illustrated are seven basic processes, including drilling, copper plate holes, apply solder plate resist, solder plate, remove solder plate, etch unplated copper and add solder mask.
C-E Elgin **Circle 258**



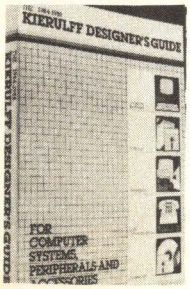
CMOS Memory and Logic Product Guide. This 20-page product guide from Solid State Scientific describes its high performance CMOS memory and logic families, which are available in commercial and military versions. Also described are 4000 series logic devices, CRT controllers, security devices, clocks and military products. Design and production capabilities, tooling services and cross reference charts are provided.
Solid State Scientific **Circle 266**

Distributed Control System Folder. This 16-page folder shows expandability of Leeds & Northrup Systems' Max 1 Distributed Control System. Starting with local unit-process control of up to 64 loops, the system is justifiable for small-to-medium processes, with the potential for plant-wide expansion beyond 1600 loops. Photos and a schematic are also provided.
Leeds & Northrup **Circle 265**

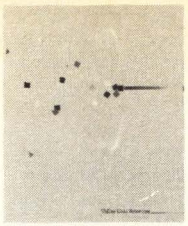


Power Mosfet Manual. This data manual from Motorola on power Mosfets includes theory applications, selector guides, a cross reference and data sheets for more than 300 standard devices. Also contained is a glossary of terms, symbols and definitions common to power Mosfets.
Motorola **Circle 254**

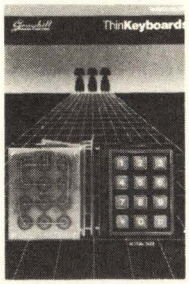
Systems Engineering Reference. This 350-page guide provides information on computer products and systems, software, peripherals, data communications equipment and accessories from several manufacturers. It is organized to assist the engineer in reviewing technology in specific product areas, evaluating options and tradeoffs, and then selecting the proper product.
Kierulff Electronics **Write 256**



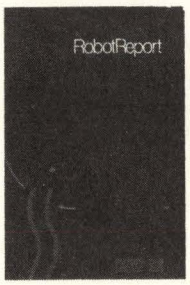
NEW LITERATURE



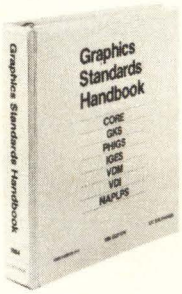
Workstation Brochure. This six-page brochure from Valley Data Sciences covers its line of logic and memory programmers, programming software, software subscription service and programmable logic development software. A complete workstation includes: programming console, PC interface board, software and documentation, a central processing unit, ASCII keyboard, CRT and a serial communications channel.
Valley Data Sciences **Circle 267**



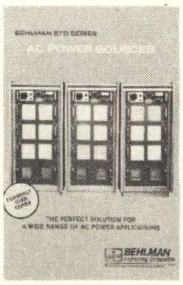
Keyboard Bulletin. Thin keyboards are described in this eight-page bulletin from Grayhill, Inc. Included are electrical rating information and the characteristics of standard graphic overlays as well as depictions of special graphic designs and color combinations. Prices are also listed.
Grayhill **Circle 263**



Robot Report. This publication describes a personal robot built by Future Computing as a result of an 18-month research project. Discussed are performance goals, design specifications and development stages. Also contained is an evaluation of how the robot met, or failed to meet, original goals.
Future Computing **Circle 260**



Graphics Handbook. This edition from CC Exchange covers graphics standards including CORE, GKS, IGES, VDM, VDI, and NAPLPS. Also discussed is the proposed PHIGS standard, tailored to the requirements of such applications as CAD/CAM, process control, simulation, architecture, and molecular modeling.
CC Exchange **Circle 268**



Power Source Brochure. The STD Series of AC Power Sources are featured in this brochure from Behlman Engineering. Single and multi-phase models are described with power outputs from 100VA to 54KVA. Fixed, variable and programmable oscillators, with frequency ranges from 45 Hz to 10 KHz, are also presented.
Behlman **Circle 255**

New Controller Brochure. This six-page brochure from Zetaco outlines its Data General-compatible line of peripheral controllers. Described are DG-compatible SMD-interfaced disk controllers, ½" standard interface tape couplers, DMA line printer and terminal controllers. Products include disk and tape controllers, BMX-1 and BMX-2, which run on DG's BMC, a ZDF-1 disk/tape controller.
Zetaco **Circle 259**

CALENDAR

January 8-10

CAD/CAM International Show. Birmingham, England. Contact: Peter Walker, Fitzroy Public Relations, 32 Fitzroy Sq., London W1P 5HH. Tele. 01-388 9871.

January 9-11

Interface Circuit Course. San Francisco, CA. Contact: University Extension, University of California, Berkeley, 223 Fulton St., Berkeley, CA 94720. (415) 642-4151.

January 14-18

Microcomputers In Control Systems: Hardware, Software, and Interfacing. Washington, DC. Contact: Continuing Engineering Education Program, The George Washington University, Washington, DC 20052. (202) 676- 6106.

January 14-17

CADCON & ATE West '85(combined shows). Anaheim, CA. Contact: Morgan-Grampian Expositions Group, 2 Park Ave., New York, NY 10016-5667. (212) 340-7900.

January 21

UniForum (Conference for UNIX users). Dallas, TX. Contact: Richard Lewis, Professional Exposition Management Co., Suite 205,2400 E. Devon Ave., Des Plaines, IL 60018. (312) 299-3131.

January 23-24

Programming in C. Baltimore, MD. Contact: Intelligent Solution, 849 22nd St., Santa Monica, CA 90403. (213) 207- 5356.

January 24-26

The 1985 SCS Multiconference. San Diego, CA. Contact: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. (619) 459-3888.

January 28-31

Communications Networks Conference & Exposition. Washington, DC. Contact: William Leitch, Communications Networks, PO Box 880, Framingham, MA 01701. (617) 879-0700.

January 29-31

Advanced Microprocessor System Design. Toronto, Canada. Contact: Ontario Centre for Microelectronics, Suite 400, 1150 Morrison Dr., Ottawa, Ontario K2H 9B8. (613) 596-6690.

January 29-February 1

Real-Time System Design: A Hands-On Workshop. Boston, MA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

January 31-February 1

Data Communications and Networking for the IBM PC and Other Personal Computers. San Francisco, CA. Contact: Software Institute of America, Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

February 5-8

Microprocessor Software, Hardware & Interfacing. Baltimore, MD. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

February 20-22

Info/Central: Information Systems and the Executive Decision Maker. Chigago, IL. Contact: Show Manager, Info/Central, 999 Summer St., Stamford, CT 06905. (203) 964-8287.

February 26-28

Automated Design and Engineering for Electronics. Anaheim, CA. Contact: Cahners Exposition Group, PO Box 5060, Des Plaines, IL 60018. (312) 299-9311.

February 27-28

Industrial Local Area Networks. Framingham, MA. Contact: Kathy Shaw, Office of Continuing Education, WPI-Higgins House, Worcester, MA 01609. (617) 793-5517.

ADVERTISER INDEX