VOLUME 11, NO. 3

MARCH 1981

Digital Design

Computers • Peripherals • Systems

Special Report

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GRINNELL SYSTEMS

VOLUME 11, NO. 3 MARCH 1981

Digital Design

Computers • Peripherals • Systems

Publication Number: USPS 407-010

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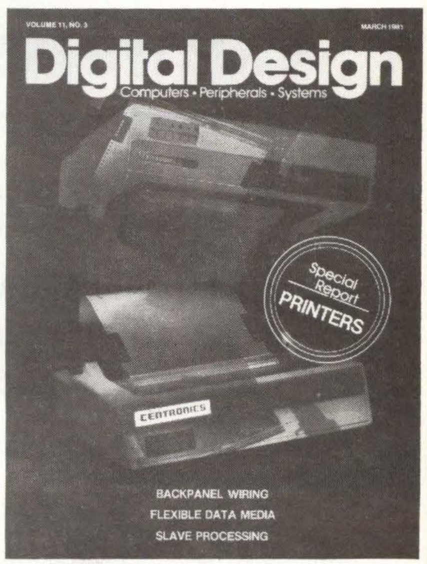
Departments



New printer improvements, reflected in higher performance at lower price/performance ratios, subject of this month. Our thanks to Centronics Data Computer Corp. for the cover.

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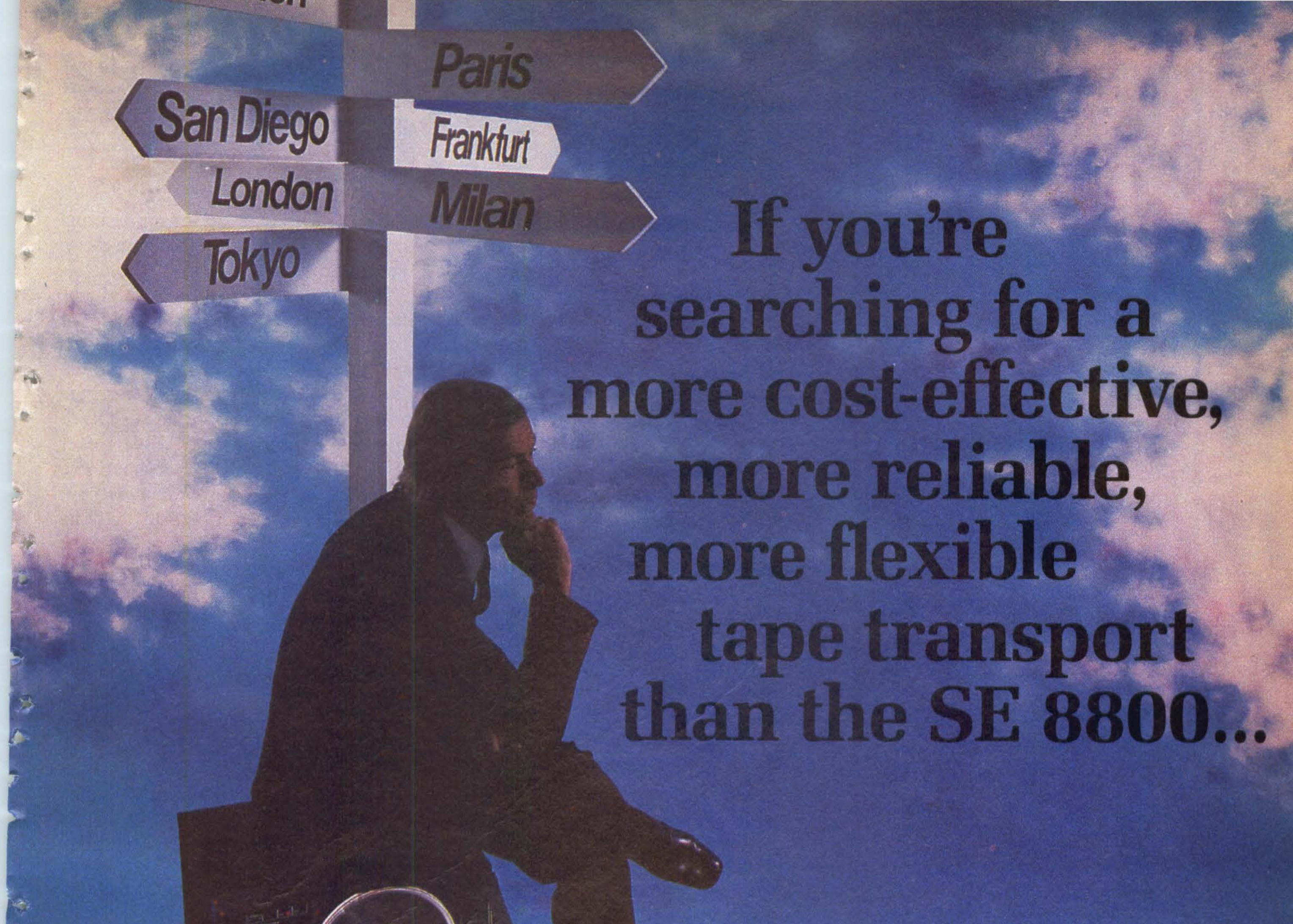

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Letters

Against Age Discrimination

Dear Editor:

Times have changed. You once spoke out against age discrimination, but now flipped over to "The Other Side" (Speakout, December 1980). You are wrong. Widespread age discrimination is a symptom of the demise of our profession. Its rape is too complete to offer hope for any near term recovery. Your own outlook confirms the diagnosis.

Our dedication to our urgent field has defeated us. We are encouraged to forego the company comptroller. And, when the loss of learning found older EEs less able to maintain the battles of technical competition, they discover themselves, like the horse of George Orwell's "Animal Farm," being forced to work harder without any influence on the fortunes of our professional ideals.

Your arguments in favor of imported alien engineers are weak and bleak, indeed. The reality of these tragedies among EEs must be faced.

Loren L. Krueger, P.E.
4834 Merilee Dr.
Minnetonka, MN 55343

Irresponsible

Dear Editor:

November's Speakout "The Other Side," speaks in favor of alien EEs and "pruning." It is naive and irresponsible. You must have been born yesterday. If any firms share your opinions, I will not buy from them.

James Kuzdrall, P.E.
Intrel Service Co.
Box 1247
Nashua, NH

Age Discrimination Exists

Dear Editor:

An old Chinese proverb says: "Be sure brain is in gear before engaging mouth — or typewritter, or editing terminal." The Editor never heard of this, judging November's Speakout, claiming age discrimination doesn't exist. This rivals the finest products from my 18 head of cattle. As for physicians, they get cushy remunerations. Ever notice the high correlation between guys flunking elementary physics and pre-med students? The AMA admits that 10% of MDs are alcoholics and another 10% are utterly incompetent. Yet this 20% is well-paid.

Industry's use of wetbacks and graduates of the Sam Hill Institute of Technology is not a response to technical geniuses turned out by fifth-rate diploma mills. It began as a deliberate policy by McNamara's elite at DOD to reduce engineering hour costs. Never mind what you got for that hour: one engineer is the same as another. So, now, U.S. firms import Indian EEs because they work for less than the British, who worked for less than Americans! And, we flood the market with "injunirs" who might have made passable techs if some fast buck con artists (university recruiters) hadn't convinced them an engineering education could be obtained by four more years of kindergarten.

Feerst is no paragon of infallibility. But he is *absolutely right* on wage-busting, age discrimination and control of IEEE by management and academia — both whom are hell-bent on turning out large supplies of cheap labor.

Dr. Yale Jay Lubkin
Director of Engineering
Ben Franklin Industries, Ltd.
Casey Creek, KY

Is IEEE Shortsighted?

Dear Editor:

How can the IEEE rationalize that the Red Chinese (or more subtle, the "PRC") have changed their political goals and hope to work elbow-to-elbow with the US? The IEEE is short sighted. I think we all belong on the funny farm if we allow Congress, the State Department and IEEE to permit this subterfuge (US Technology transfer to Red China) to continue.

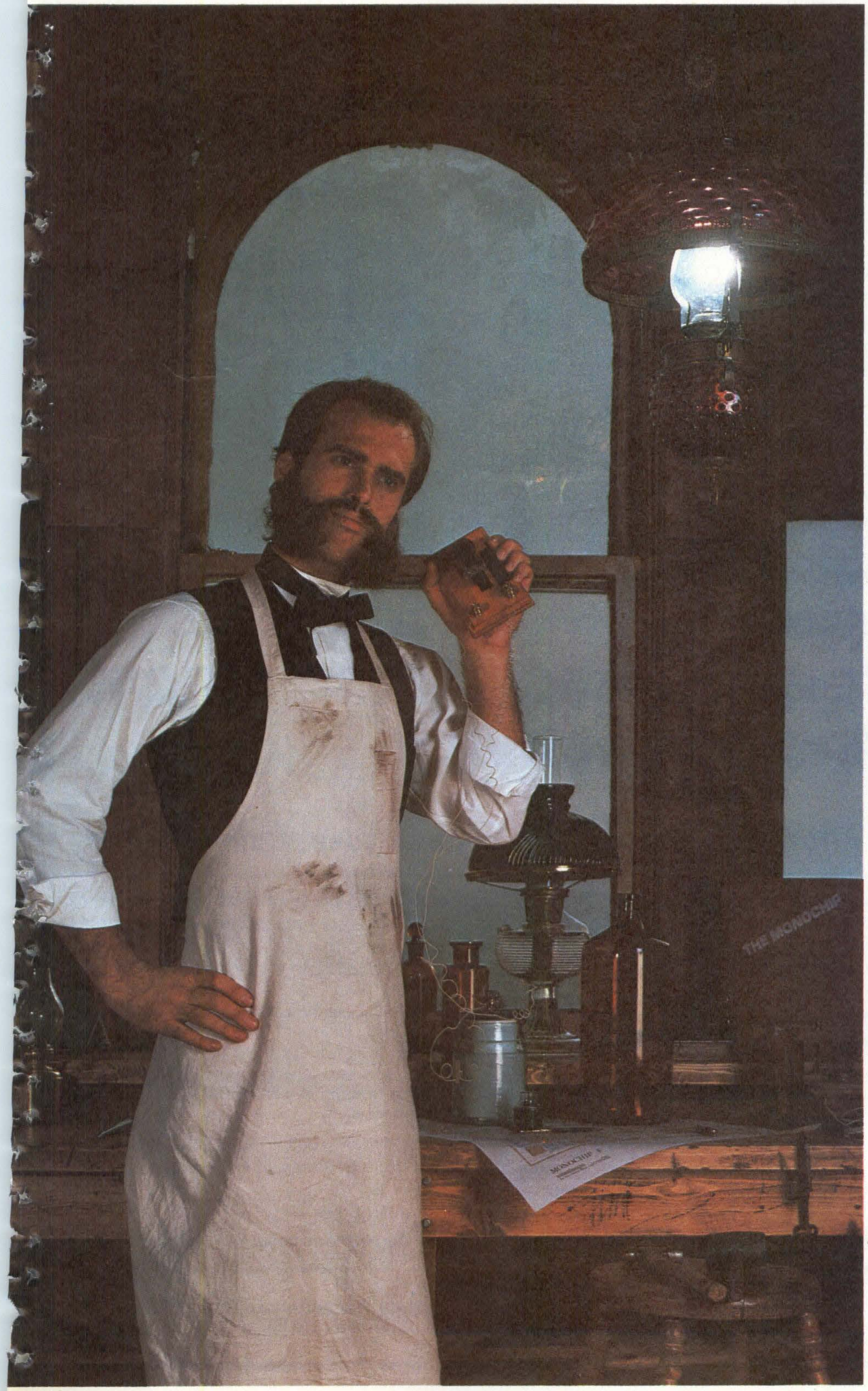
Jay Atherton
1003 NW 179 PL
Seattle, WA

Lazy EEs?

Dear Editor:

November's Speakout, "The Other Side," places blame for "the alien invasion" right where it belongs — on older, lazy, complacent EEs who feel that a 20-year old degree entitles them to lifelong job security. (But don't ex-

With Monochips,™ Alexander Graham Bell might have invented the picture phone.



"Mr. Watson, come here — I want you." With this simple statement telecommunications technology was born.

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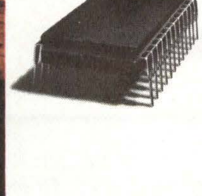
p 4113

interdesign



Monochip:™ the semi-custom IC.

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pect this position to be too popular.) After turning 45 three years ago, I started my own company. I still design with 8085s and Z80s, yet I have more work than I can handle. To keep up, spend several hundred bucks on manuals and ICs. Get hands-on experience. Is your employer a tightwad? Then do it on you own time — at your own cost. It is fun, enlightening, and rewarding.

Ken Barbier
Borrego Engineering
Borrego Springs, CA

Defends "Pruning"

Dear Editor:

With reference to your November Speakout, "The Other Side," you are right: if an older engineer expected not to "be pruned" and to stay around, he'd better study hard to keep up and make himself worth twice what a college graduate is worth. Being able to tell war stories of relay logic races doesn't make him valuable! Being able to configure new designs with new components using new computer tools while blending into his designs the safeguards learned from experience does make him worth twice — perhaps thrice — what today's graduates are getting.

Robert J. Young
Mission Computer Assoc.
Mission, Viejo, CA

Feerst Is EE's "Best Friend"

Dear Editor:

Your Speakout, "The Other Side " in favor of alien engineers and "pruning" in the November issue is a disservice to the working engineers. Irwin Feerst is the best friend the EE has. You are wrong.

Gene Barber
Logican
Box 80158
San Diego CA

Wants Sabbatical

Dear Editor:

November's editorial, "The Other Side", dismisses age discrimination by claiming that it's the older EEs' fault for not working harder to avoid obsolescense. What you term a necessary "pruning" of EEs ignores the emotional and financial hardships imposed. If an EE grows obsolete, isn't it partly the fault of the employer? To let an EE stagnate and not to provide the time and resources to keep current is inefficient. To then fire an EE in this position is cruelty and exploitation! EEs should not tolerate it! Unions insisted on job protection based on seniority. Professor's tenure system protect them. Why do only EEs let themselves be mistreated?

Do not publish my company name.

H.C.
Design Engineer
Boston, MA

PROM/ROM Power-Strobing

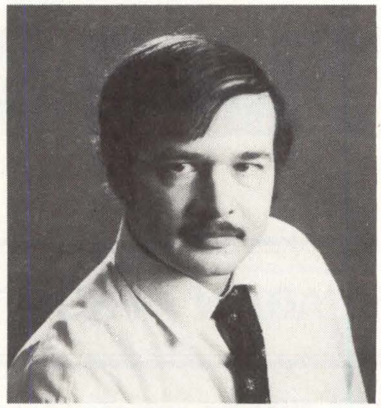
Dear Editor:

With reference to the Septembe r Designers' Notebook, "PROM/ROM Power-Strobing Reduces Power Consumption," (pg. 100-102), there is an error (pg. 102) in that the 75451 driver output is LW LOW when $\overline{ME} = \overline{CE}$ is LOW; the 75451 should be HIGH when $\overline{ME}$ is LOW. A 75450 would solve this.

Nicholas C. Gray
Signetics Corp.
Sunnyvale, CA

Speakout

Behind The Scenes — Part Two



Underlying reasons behind foreign startups and purchases of U.S. electronics and computer firms were discussed last month. We continue our observations.

The computer industry must insist on strict controls, since "backroom ownership" of foreign interests is common in many foreign nations. Many aren't strict on reporting directors and major stockholders. It's too often the custom for director(s) to hold stocks in trust for mysterious individuals or groups, who, for very good reason, prefer to remain anonymous controlling forces in that firm — individuals or groups who may have everything to gain by financing their own electronic and computer industry (or specific firm).

Surely the Fed won't allow this, will they? In theory, every foreign bank holding company will receive a tedious yearly form to fill out — on their word of honor — that no anonymous backroom ownership or other hanky panky is going on. Violators, *if caught*, will supposedly get a penalty (well worth the risk). Who enforces it? Policing the honesty of these foreign interests will be primarily the foreign banks' and governments' responsibility.

This matter of controls brings to mind the question of equal treatment: do U.S. computer firms get the same treatment overseas? You'd think so. But it's a stacked deck of double standards. By way of comparison, let's see what our computer industry is up against. U.S. computer firms are forbidden by the U.S. Foreign Corrupt Practices Act from engaging in activities that some foreign computer firms use more than just a little. American firms are forbidden (and rightly so) from paying a premier's or prime minister's son to arrange a sales meeting with the right people, or to tip an underpaid and overworked airport customs official in Bavania to expedite your computers from the docks where they've been for two weeks (while your foreign competitor's computers mysteriously move out in two days). Our foreign competitors view us as naive; and, when these groups acquire U.S. banks, interests and firms, judging from this, do you seriously think these same individuals will give our computer firms a fair shake *here?*

In Europe, tough unions hurt computer industry profitability; unions have much to say about how their firms are run (unlike in the U.S.), and general strikes (often over picayune matters) can totally paralyze a firm or industry. Although the U.S. doesn't harass foreign computer makers here, it doesn't work the other way: foreign nations do harass U.S. computer and electronics firms. It may vary from an outright "buy Japanese" policy (as in Nipon Tel and Tel's case, despite all the goodwill verbosity we've heard lately) to sole-service arrangements that hassled Honeywell's U.K. plants) to outright squeeze-outs (as in France). Or, they may require U.S. computer and electronics firms to take on a foreign partner and give him 51% controlling operating shares (as in Mexico). India's hassling of U.S. (and its own) electronics and computer makers is legendary. These tariffs, barriers and controls damage U.S. computer makers.

Antitrust laws aren't so much a concern in most foreign nations for their firms, unlike here, where our Department of Justice scrutinizes every move, and the government is more our foe than ally — unlike in many foreign nations. Foreign firms, in contrast, get better treatment from their governments: they receive low interest rates, tax abatements, buying preference rules, etc. All isn't rosy, though, and despite the benevolence of foreign governments, the tariff barriers and overly-stringent and contradictory laws have harmed European computer makers. Backbreaking taxes haven't helped; it forces European firms to borrow at higher rates for needed equipment and plant expansion. These onerous restrictions spur foreign computer makers to start up U.S. divisions and purchase shares or controlling interest in U.S. computer firms.

Paul Snigier

Paul Snigier, *Editor*

PALs Minimize Hardware

More OEM designers are taking advantage of PROM on-the-spot programmability. These designers are using PALs to achieve a range of logic replacement capabilities from random gates to complex arithmetic circuits. With a programmable AND array feeding a fixed OR array, PALs permit compact realizations of sum-of-products expressions. In the following capsule commentary, John Birkner, Product Planning Manager of Monolithic Memories in Sunnyvale, CA, urges system designers to take advantage of PALs.

the problem

A look at the $3 billion digital IC marketplace provides insight into the needs of systems designers. First, the marketplace has four major areas: MPU, RAM, TTL CMOS and ROM/PROM/EPROM.

Because the average system contains a similar percentage-cost of silicon for MPU, RAM, ROM/PROM/EPROM, TTL/CMOS, it is interesting to note the high percentage of random logic, (TTL/CMOS). In spite of the great μP revolution, the systems marketplace still spends 35% of its dollars on random logic with 87% of its IC chip count devoted to TTL/CMOS. Observe the high percentage of 16- and 20-pin DIPs on today's small board computers and μP systems.

The ASP (Average Selling Price) of the MPU, RAM, ROM/PROM/EPROM is around $4.00; whereas the ASP of TTL/CMOS is about $.50. Because the cost of placing an IC on a board is around $1.00 (board cost, assembly and test), the major cost of using TTL/CMOS is in the overhead, not in the silicon.

programmable logic

Semiconductor manufacturers are designing a host of programmable logic devices (random logic gates/muxes/decoders/flip flops) to integrate this last holdout to LSI. Programmable logic promises to balance the level of integration of digital ICs while further reducing PCB real estate per system. Further, programmable logic gives the user a custom IC which he can buy as an inexpensive high volume/multiple sourced virgin device, and then customize on commonly available programmers.

The first and most common programmable-logic-device suitable for logic replacement is the bipolar PROM. Available in a wide variety of I/O pin ratios, the PROM transforms an input variable (address lines) to a desired output condition (data out) with a propagation delay in the range of 50 to 80 ns. Normally thought of as memory, the PROM is a sum-of-products, Boolean transfer function which transforms all possible input vectors to any desired output vector.

A word of caution: PROM outputs can glitch during the propagation delay of any input change. This occurs because any input change causes the data source to move from one product to another. The arriving input may run into a gap, overlap or a third product, causing unpredictable outputs.

The first programmable logic device designed specifically for logic replacement was the FPLA. The programmable AND array overcomes the previous glitch problem in the PROM and allows more input variables. A recent entry into the programmable logic marketplace is the PAL (Programmable Array Logic). PAL architecture is a complement of PROM architecture, since the AND array is programmable and the OR array is fixed. This architecture allows simple programming in existing PROM programmers plus a fast propagation time of 40 ns (max.) over commercial V_{cc} and temperature ranges. In addition, PALs have option registers and I/Os.

PALs: a family of 15

Fifteen PALs comprise a family approach to the replacement of random logic gates, muxs, decoders and flip flops at a greater than 4-to-1 chip count reduction. Die sizes range from 13K sq. mils to 19K sq. mils, compared to 2-K PROM and 4-K PROM die sizes.

μP-Wired Houses Open OEM Markets

Motorola's μP-wired home in Phoenix could be a hint of the future. Although resembling a space-age millionaire's mansion, this home is a test vehicle, pioneering the μP-wired homes of the mid-1980s and beyond. The next step will probably be fiber-optic lines (110/220 volts) tapping into each home by the late 1980s. Thus, μP-wired homes will have access to information and monitoring services. The new technology will also open up vast new markets for μP makers and system houses. Such a projected market could possibly exceed the small business market by 1985.

Motorola's William Pierce described the system now being tested as follows:

the system

The system is comprised of a number of microcomputers connected together which control the various pieces of electrical equipment in the house. The system was designed to be very simple to operate and function as a single entity. It demonstrates many applications where the microprocessor could be used in the home environment.

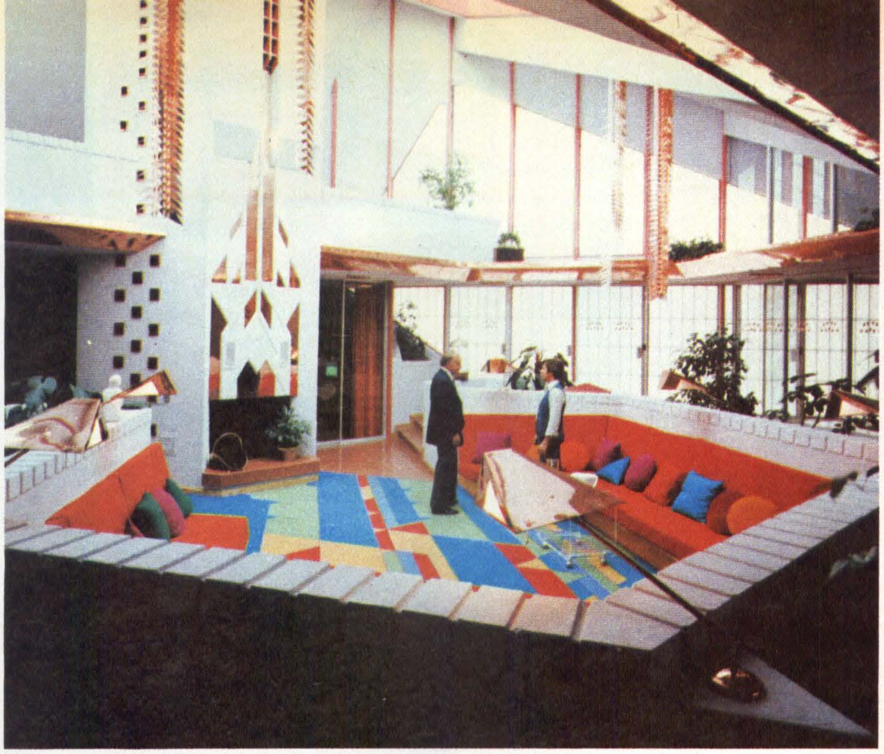
After the initial installation which provides sensing of critical temperature, humidity and other parameters and control of most of the electrical functions of the home, Motorola will use the home to partition functions and design LSI chips to serve these dedicated functions. The result may be that equipment providing special functions representing part of the current system could be available to consumers for the $100-$200 range. With the development of the μP and technological improvements made in the design and yields, the home electronics market promises to be one of the largest growth areas over the next decade.

The home computer system designed and installed will be a dedicated computer system which will control and manage all of the electrical, environmental and security requirements of the home. The multi-computer system will also be operator programmable, so that the homeowner may tailor the system to his individual needs.

The electronic control package consists of five microcomputer units supplied by Motorola. The units, "nodes", are connected together to form a multicomputer network. This hardware configuration keeps system response time low and minimizes effects of hardware failure. The homeowner will talk to the computer by use of a keyboard which works with a television set as a display. The MC6847 video display generator is the key to allowing this multiple use of the set in the home.

Normal operation is transparent to the homeowner. There is no way to tell the computer was involved in most operations. For example, lights are turned on by conventional-looking wall switches, but the switches do not control the lights directly. They serve as inputs to the computer which controls the house lighting. The home owner defines what switches control individual lights when he programs the system. No knowledge of computer programming will be necessary since the system is designed to be programmed by people without any computer background. This was accomplished by designing a system which is interrogatory in nature and displays menus of the possible choices of action to guide the user. One of the largest efforts in the project was not the equipment, but rather the "software" associated with it.

One of the major functions of the system is the control of the environmental systems. Not only will the electronics serve as a very sophisticated thermostat, but they will also help conserve energy. It will have a wider variety of environmental equipment than a conventional home, and the system may be programmed to select the equipment which will use the least



Motorola's μP-wired house, examined here by George King of *Digital Design*, is a precursor of coming μP applications for the mid 1980s.

energy to perform the task at hand.

Security is another major function of the system. There will be no keys. The exterior doors have calculator-style keyboards.

The computer will open the door when a valid access code is entered. Most of the rooms in the house contain smoke and motion detectors which serve as inputs to the computer. If any

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of these sensors detects an alarm condition, the system can place phone calls to the appropriate authorities, as well as sounding alarms or turning on lights.

Most of the lights and half of all the wall outlets will also be under computer control. They may be activated by direct human control (i.e., a wall switch), the time of day, or inputs from any of the sensors in the home. The method of activation will be determined by the homeowner when he initializes the system.

Data storage and retrieval will be a third major function of the system. Such things as schedules, messages, recipes, bank account information, meal menus, diagrams, or any other text or graphic information may be placed in the system for storage and later access.

The system will also keep a running calendar of events updated for the homeowner. Events such as birthdays, appointments, classes, etc., may be entered into the system. After an event has been entered it will be cataloged by date and appear when the homeowner requests the calendar for that date.

software structure

To simplify implementation, it was necessary to isolate individual functions. These "processes" perform specific tasks such as security, environmental control, display. A multitasking executive program resides in each computer and orchestrates the resident processes by dispatching to each according to a priority scheme.

The executive program provides a number of basic functions such as dispatching, buffer management, and interrupt handling to each node in the system. Processes are described to the executive using Process Control Blocks (PCBs). Generally, a process is responsible for a group of one or more closely related functions or tasks. A task is described to the executive via a Task Control Block (TCB) and contains data associated with a particular invocation of a process. A process cannot execute unless a task is assigned to it. Processes communicate with the executive using a mechanism called an Executive Service call (ESC). The ESCs available include: Create Process, Purge Process, Create Task, Activate Task, Suspend Task, Delay Task for Timer, Timer Alarm, Define Interrupt Handler, Acquire System Buffer, Return System Buffer, Extended ESC.

Inter-process communication is accomplished via an extension of the executive program. This extension is, in actuality, a process itself called PTP. Communicating processes need not be concerned with such things as residency of other processes within the same computer or data movement since PTP is responsible for these tasks. Should one process need to pass data to another, all that is necessary is a simple connection sequence using PTP followed by the actual data passage using PTP. The PTP process is similar to a telephone exchange in many respects and greatly simplifies inter-process communications.

The inter-computer data transfer is accomplished by a communications board in each node. This board has its own MC6800 microprocessor which drives an MC6854 advanced data link controller. The software on the communications board is a modified "SDLC" protocol with some loop mode enhancements. PTP serves as the interface between the applications processes in the node and this communications software. The communications software may be broken up into two levels which perform various tasks. These levels are a packet switching level and a frame level.

There are several unique processes which comprise the total software package. These processes include: Disk, Display, Load Manager, Switch Manager, Security, Energy Management, Environmental, Time, Printer.

Each computer in the system has several processes resident, but no computer contains all of the processes. A process may be duplicated in more than one computer. The distribution of the processes is as follows. • The Display process resides in three computers that are connected to relay panels. • The Load Manager process is resident in the two computers that are connected to relay panels. • The Switch Manager process is resident in the four computers sensing external switch closures. • The Disk and Printer processes are resident in the computer connected to their appropriate equipment. • The Security process resides in the computer connected to the keypads used for entry. • The Environmental process is resident in the computer which contains the analog inputs for temperature and humidity. • The Energy Management process resides in one of the computers connected to relay equipment. • The Time process is resident in all computers. • The functions of each process will now be discussed.

The disk process is concerned only with placing and retrieving information stored on the mass storage device, a floppy disk. Other processes may use the floppy disk to store pertinent information such as tables used in constructing data bases or information to be placed on the television screen. The process keeps a record of what information has been stored on the floppy disk and where it is so that the information may be successfully retrieved at some later time when needed.

The display process is the operator's interface to the system. The human engineering aspects are most apparent in this process. It is designed to lead the operator by the hand, so to speak, in his usage of the equipment. The display is formatted with the possible choices of action at each point where operator input is required.

When the operator enters a choice, the process then executes that action and presents the operator with a new group of action possibilities. This technique guides the user through such activities as creating a calendar of events, placing information in mass storage for later retrieval, monitoring statuses of other processes and programming the other processes' activities.

future possibilities

A number of additions are being incorporated. The area of off-site communications via modem and the use of light pens in connection with the television displays are now under study. The system is used as a lab to try out various new approaches to electronics in the home.

"Built-in" Modem Modules Add Flexibility

Data communications sales by 1983 will total $700 million. An increasing share will go for low speed (up to 1200 baud) modem communication — the transmission rate most widely used in a rapidly-developing segment: personal data communications. Baynard F. Kessler, President of Novation (Tarzana, CA), one of the top ten modem makers, feels this is an explosive area that is about to take off.

As pointed out to *Digital Design* by Kessler, these multi capability modems communicate on a variety of networks and operate at various transmission rates from 0 to 1200 baud and are implemented with custom LSI chips into a single 2.25 × 2.75" module. Kessler offered the following advice for OEM designers who will be using these modules in building block applications.

The modules can be mounted directly on PC boards or to any flat surface within most computers or terminals. Seven functional modules that offer complete LSI based receiver and transmitter functions have been announced so far.

These small modules give the designer a system flexibility impractical until now. They can be placed directly into μCs, interactive terminals, even hand-held portable devices very economically — yet maintain high performance and reliability. They are in a plastic container for protection during PCB installation or replacement; each unit can be stabilized after mounting by a hold-down strap or snap-on clips anchored to the main PCB.

They greatly simplify an OEM's problem of maintaining spare parts and troubleshooting field problems. If these units are purchased in sufficient quantities, the modules become a cost-effective part with ease of replacement compatibility. Purchased in quantity, with low unit pricing, they offer a practical solution to the truly "disposable" component.

In the 1980s, an increasing number of future terminals will have built-in communications capability, with LSI chips containing entire modems. Functions traditionally performed by stand alone units and other front end processors will be handled more and more by newer terminal designs and minicomputers which will have all modem capabilities self contained.

As the volume demand for built-in communications capability increases, some OEM manufacturers sought price and size relief by utilizing existing semiconductor devices. But rising demand for higher performance and configuration needs resulted in a wide variation of factors that created confusion among designers and engineers.

These modems-on-a-chip feature programmable modes that achieve, for example, CCITT V.21 and V.23 compatibility with the addition of the deaf TTY network frequencies. Additional examples would include detect ring, busy and dial tone signals for use with the PLI module. The module's data format is serial, binary and asynchronous. They operate in either answer or originate, full or half duplex, at 300 baud on 2 wire and 1200 baud, half duplex on 2 wire, full duplex on 4 wire.

Phone line interface

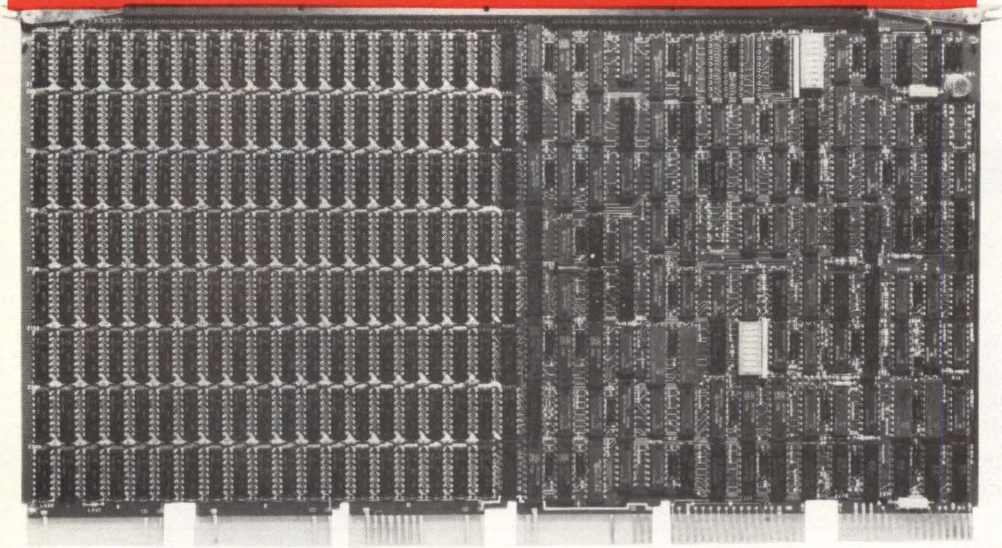
The basic element in the building block approach is the telephone module, PLI, plus the addition of any other module configuration.

from Remote Terminals

London. Former ousted chief executive of Fairchild, Ltd., London, Wilf Corrigan, is launching a new business there. The company ("LSI Logic") will manufacture gate arrays. Much of the $6 million initial capital investment is being put up by some unidentified California venture capital firms... **Japan.** Intel has set up a semiconductor plant in Japan ...Nippon Univac Kaisha is expected to start making mainframes by 1984. (Sperry Univac owns 34.7% of Nippon's stock) ...Oki Univac is currently making Sperry Univac minicomputers. (Sperry Univac owns 47% of Oki) ...Tokyo Sanyo (a division of Sanyo Electric) is investing $50 million in its semiconductor plant this year ...**Ireland.** Ireland is getting a personal-computer plant. Sord Computer Systems of Japan is building a factory there that will, at start up, turn out two computers a day. Initial investment by Sord is said to be around $6.5 million ...**Germany.** AEG-Telefunken, Germany, is bringing out a keyboard with Chinese characters. The device was recently shown at a Peking exhibition and was greeted enthusiastically ...**Scotland.** In Scotland, public and private institutions are forming a pool from which financing will be available for starting up new high-technology plants. To get such backing, individuals will have to display skills and determinations to allow them to build fast growing companies. The amount of equity financing for each individual will range from $60 thousand to $750 thousand ...**United Kingdom.** The United Kingdom is in the worst recession it has experienced in 30 years. Even high-technology firms are showing lower earnings. Some revenues are even in the loss columns. ...**Japan.** MITI Company in Japan has developed a super Schottky diode. Claimed to be 40 times more sensitive than conventional diodes, the new device combines niobium (metallic element) with gallium arsenide (semiconductor). The diode is cooled to the temperature of liquid nitrogen to attain top performance. Patents are sought in Japan, US and other countries.

ADD-ON ADD-IN

MEMORY...FROM THE LEADER



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Circle 10 on Reader Inquiry Card

Planning A μP Development Capability

Lance A. Leventhal,
Contributing Editor

Almost all companies manufacturing electronic products use microprocessors. In less than a decade, the microprocessor has evolved from a fascinating new toy into a standard component. It is now as commonplace as the integrated circuit, switching power supply or semiconductor display. However, only a few organizations have solved the problems of developing microprocessor-based products. Although they have paid much attention to the choice of development tools, they have generally ignored overall plans. A systematic approach to microprocessor development requires consideration of necessary criteria and an awareness of alternatives and pitfalls.

The criteria that a company must consider in establishing an overall microcomputer design and developmental facility include:

- Ability to support a variety of processors from several manufacturers. Clearly, in this era of rapid technological change, no single maker controls the entire microprocessor market.
- Combined hardware and software support. The final product requires both types of support working together. Furthermore, both types of designers must use the facility equipment. Also, hardware/software tradeoffs significantly affect product cost and capabilities.
- Standardization. Facility equipment must deal with all processors in the same way as much as possible.
- Promotion of good programming practices. High-level languages and such methods as structured programming and top-down design make software less expensive to develop and maintain. Software development time, as well as cost, increases as programs become larger, trained personnel become more expensive, and hardware prices drop (particularly in terms of cost per function).
- Sharing expensive peripherals. Large disks, fast printers, high-speed input devices, plotters, and other equipment can speed software development greatly, but are seldom needed full time by a single project.
- Common access to facilities, data and work in progress. All users should be able to take advantage of common software and hardware facilities. Many projects require that several programmers have access to data and work in progress.
- A high level of support. Hardware and software tools must be powerful, easy to use, integrated and easy to extend or improve (a combination that is seldom achieved).
- A general framework for control, access and expansion. The design and development facility requires overall management policies which govern the use of computer and human resources.
- Cost and lifetime. The initial cost of the system is an important factor, but so is its expected lifetime. Since microprocessor development remains a continuing problem, a long-range plan is essential. An inadequate approach at the present time will surely lead to serious problems and higher overall costs in the next decade.

alternatives and pitfalls

There are many different approaches to microprocessor development. Typical systems are:

- Stand-alone microprocessor development systems dedicated to a single processor or a single manufacturer. One of the most popular systems is the Intellec, available as a series of models from Intel.
- Universal microprocessor development systems capable of handling a variety of microprocessors from different manufacturers which specialize in test equipment, instrumentation or computers. Leaders in the field include Futuredata/Genrad, H-P and Tektronix.
- General-purpose computers, usually used on a timeshared basis. Variations and combinations of these development systems are clearly possible.

A company often finds these typical pitfalls in developing microprocessor-based products:

- Many development systems only allow one user at a time. A single project with one programmer loses no time, but otherwise this condition is wasteful.
- Support (particularly software) is limited or low in quality. Few companies in the development system business have much software development experience.
- Systems cannot share facilities. Each requires its own software, data and peripherals.
- Different systems. A person cannot easily move from one to another and training is difficult.
- Lack of standard high-level languages for promoting structured programming. Many systems offer no high-level languages at all; others offer only BASIC or FORTRAN. The availability of high-level languages may vary from processor to processor, even if the system ostensibly supports many CPUs.
- Lack of high-quality hardware support. Some systems can only be used to develop software; this lack of capability is often a problem with development tools that run on a large, general-purpose computer.
- New tool extensions and development which is very difficult because of limited software support. Good support tools require a high-level systems programming language which is seldom provided.

The mini provided central facilities, proven software, sharing of expensive peripherals, general access to data and programs, and a standard framework for communications and expansion. The satellite stations all operated similarly, regardless of which micro they used. Since the company designers deliberately kept individual station requirements to a minimum, each station only needed a communications package that connected it to the central mini.

Of course, nothing prohibits a station from providing more elaborate facilities, including local peripherals, software and mass storage. The station could, in fact, be a self-contained development system. However, a simple station can more easily support a variety of processors. Many processors are so new that elaborate systems are not yet available, or so limited in function that more elaborate systems would be impossible to construct.

The UNIX system was a key factor. UNIX is expensive and does not have the support of standard DEC operating systems. However, it is a popular timesharing system and provides such software facilities as the C system programming language and the YACC compiler. Such facilities make implementing additional system software far simpler than in other environments. New compilers could be produced in weeks or months, rather than in years. This potential was particularly important for Doric because of the projects that were already underway. Furthermore, Unix provides a tree-structured file system with multiple directories. Users can keep their own directories, rather than searching through a large central directory. They can also create subdirections and keep backup copies in a separate directory.

an example of an approach

The following case study describes how Doric Scientific of San Diego, CA (a division of Emerson Electric), implemented microprocessors into its products. The company is medium-sized and has little previous computer experience.

Doric manufactures electronic instruments that measure temperature and other physical quantities, particularly for the industrial marketplace. The company's products include digital indicators, data loggers and process monitors. In recent years, the use of microprocessors has allowed Doric to introduce intelligent data loggers such as the Digitrend 220 and process monitors such as the Digitrend 240. From 1976 to 1980, Doric grew from $5 million in sales and under 100 employees to $10 million in sales and over 200 employees.

Doric's products are far from simple. The data logger involves analog inputs and a full complement of standard and optional peripherals which include keyboard, display, alphanumeric printer, magnetic or paper tape, RS-232 or current-loop devices, and control terminals. The logger provides thermocouple linearization, self-test, automatic ranging and various scanning methods, as well as optional alarms and functions. The process monitor performs data logging functions and also allows programming from a keyboard control terminal. The operator can edit and list on-line without interrupting a scan sequence and can also program alarm setpoints, assign functions to points and determine the scanning sequence.

Doric first began to use microprocessors in 1974. The company quickly discovered the problems of inadequate development tools, software cost and time overruns, and a final program that no one really understood. In 1976, Doric decided to organize its microprocessor development facilities under the direction of Bill Allen, manager of system software. At that time, the company was involved in designing six products using five different microprocessors.

Doric chose to use the following hardware and software tools: DEC PDP-11/70, the UNIX system, a standard high-level language similar to Intel's PL/M, individual microcomputer stations (designed in-house) that acted as terminals and contained their own local monitor, debugging tools and in-circuit emulator.

reasons behind the choices

Now let us look at these choices and see why Doric made them. The company tried to provide a standard set of high-quality tools that were powerful, easy to implement and extend, and promoted good programming practices.

The PL-type programming language obviously made development much faster. Although experienced assembly language programmers can outdo a compiler for short programs, few programmers can optimize code better than a reasonable compiler when the program exceeds 12K to 16K. Doric's programs ranged in size from 32K to 75K. In such programs, the mechanical consistency and global outlook of the compiler overcome the ingenuity of an individual programmer. Although the table-driven code generator produced code 75% to 100% longer than hand-written, an optimizer reduced the size of the final code by an average factor of 40%. Note, however, that the optimizer was highly machine-dependent. The results were good and only a few interrupt service routines had to be written in assembly language. The high-level language also simplified training, maintenance, and project control and management. Of course, all of these remarks apply equally well to PASCAL and C, which are far more widely available now then they were in 1976.

some key points

What key points emerge from this experience? Bill Allen (formerly with Doric and now head of Software Engineering Associates, 9462 La Cuesta, La Mesa CA 92041) offered the following observations:

- The approach Doric took makes sense only if you are designing several simultaneous products over a 5 or 10-year period. Otherwise, the minicomputer is too expensive.
- The operating system is a key factor. A system like UNIX that is designed for timesharing and which provides excellent development facilities can pay for itself in ease of use, implementation and expansion. Other important tools often can run under UNIX as well.
- The high-level language allowed designers to try alternative approaches in a reasonable amount of time. These alternatives were particularly important in making hardware/software tradeoffs. Few hard-and-fast rules exist for determining such tradeoffs. Since the programs were written in a high-level language, designers were not forced to live with an initial incorrect decision, even in a very long and complex development cycle.
- People with hardware and software experience were especially valuable, but difficult to obtain. Programmers who dealt with hardware (perhaps in writing I/O drivers or other systems software) could adapt easily from working with minicomputers to working with micros. Efforts had to be made to move people over from software to hardware, promote in-house courses, and encourage people to take outside courses in the areas in which they lacked knowledge.
- A large minicomputer with high-quality peripherals and software provided reasonable overall cost, the ability to share facilities, a large amount of high-quality utility software, and a system that could be extended and expanded.

Thermal Print Head Achieves Super High Speed

Thermal printing features high print quality, low cost and easy maintenance, but has always suffered from low print speed. We at OKI Research Labs feel we have solved this problem by developing a newly designed thermal print head that prints at a resolution of eight dots per mm (203 dots per inch) and a speed of 2 ms per dot line. This represents an increase in print speed of one entire order of magnitude.

head driver using thyristors

Normally, in a thermal print head where the heat elements are arranged in a straight line over the whole effective

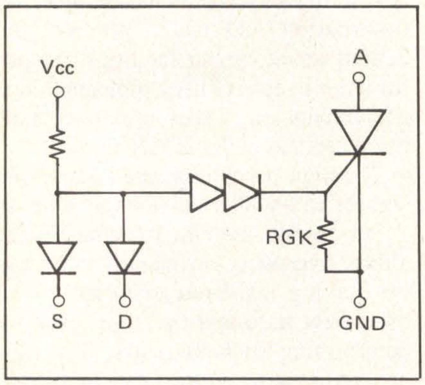

Figure 1. The head driver corresponding to 1 bit

recording width, the heat elements are divided into several blocks and are driven by a diode matrix circuit connected to them. Therefore, the number of external connection terminals is reduced to the sum of the numbers of columns and rows of the matrix. Two methods are available to increase the printing speed of such a head: one is to shorten the applying time of current to the heat elements and the other to reduce the repetition frequency of printing per dot-line by increasing the number of heat elements in simultaneous printing. Both methods, however, have disadvantages: the life of heat elements shortens in the former and the number of terminals increases in the latter.

Consequently, to allow easy terminal connection and superhigh speed printing, the authors have developed an IC composed of thyristors having a memory and a switching function and AND gates for matrix drive.

Fig. 1 shows the head driver corresponding to 1 bit, where the two

Table 1 Characteristics of a Thyristor

Breakover Voltage	60V
Breakdown Voltage	60V
Holding Current	2mA
Gate-Cathode Resistance	1.5kΩ
Current Amplification Factor of NPN	30
Current Amplification Factor of PNP	0.2
Gate-Trigger Current	0.5mA
Turn on Time	0.5μs
Turn off Time	3.5μs
dV/dt Firing	30V/80ns

diodes connected to the terminals S and D form an AND gate. Only when both terminals S and D are "H", the current from the terminal V_{cc} flows into the thyristor gate and turns it on. The head driver IC consists of 32 bits/chip. **Table 1** shows the characteristics of the thyristor.

drive method

The wiring block diagram of the thyristor-driven thermal print head is shown in **Fig. 2** and its drive waveform in **Fig. 3**. To drive the thermal print head, first a head voltage is applied. Then, data is written to the thyristors connected to S1, and the thyristors are turned on to initiate printing. After completion of the writing to S1, writing is continued sequentially in the order of S2, S3, . . . Sn. Any number "n" can be selected. Since the total writing time (n × 1 μs) is shorter than the printing time (approx. 2ms), printing is performed at one time. Further, simultaneous printing of max. 1 dot-line is also allowed. The head voltage is finally reduced to zero, and printing is completed when all thyristors are turned off.

The use of AC head voltage eliminates the need for a switching circuit to turn the thyristors off.

meander winding heat element

A high resolution (8 dots/mm) heat element is difficult to manufacture unless it is of thin-film construction. The authors have already developed a thin-film heat element consisting of multi-layers of Ta_2N, SiO_2 and Ta_2O_5 on a glazed ceramic. The authors have changed the shape of the heat element

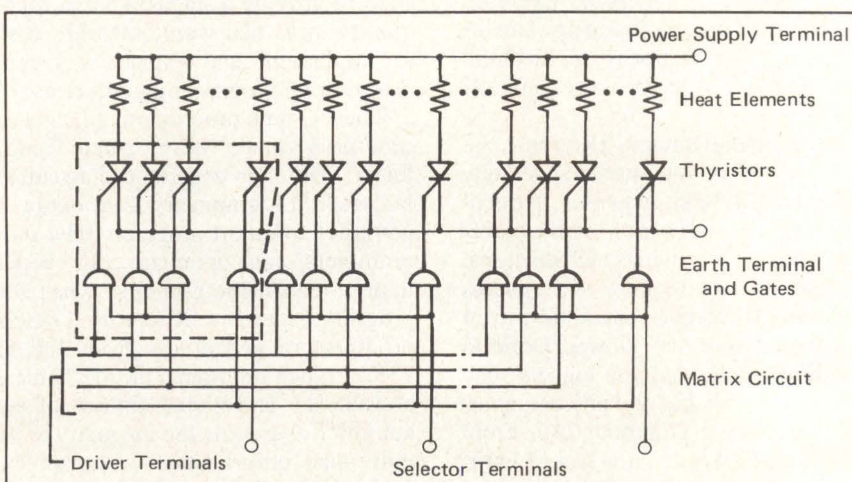

Figure 2. The wiring diagram of the thyristor-drive thermal print head

from the conventional rectangle to the meander winding shown in **Fig. 4** so that it can endure superhigh-speed recording. By the development of the new heat element, the following effects have been obtained:

- Reduction of the current load on the thyristors due to higher resistance of the heat element
- Uniform temperature distribution on the surface of the heat element
- Improvement of oxidation resistance by use of a thicker head element

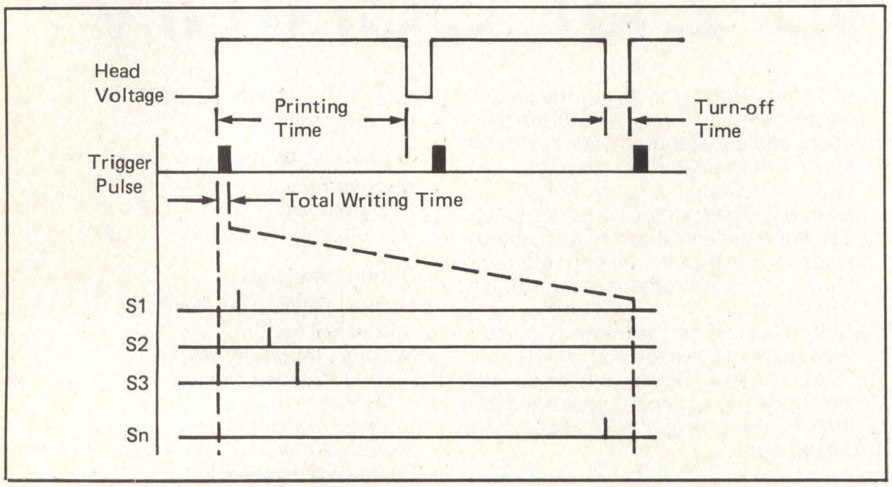

Figure 3. Drive waveform of the thyristor-drive thermal print head

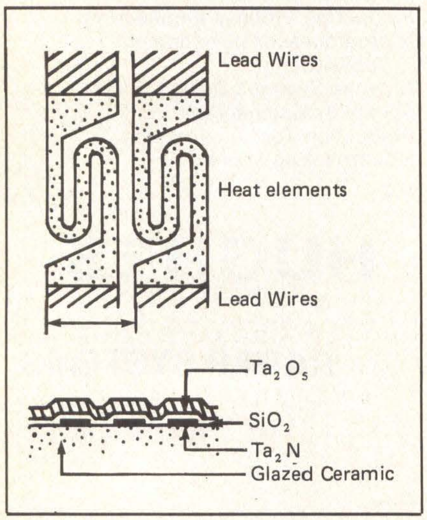

Figure 4. The meander winding heat elements

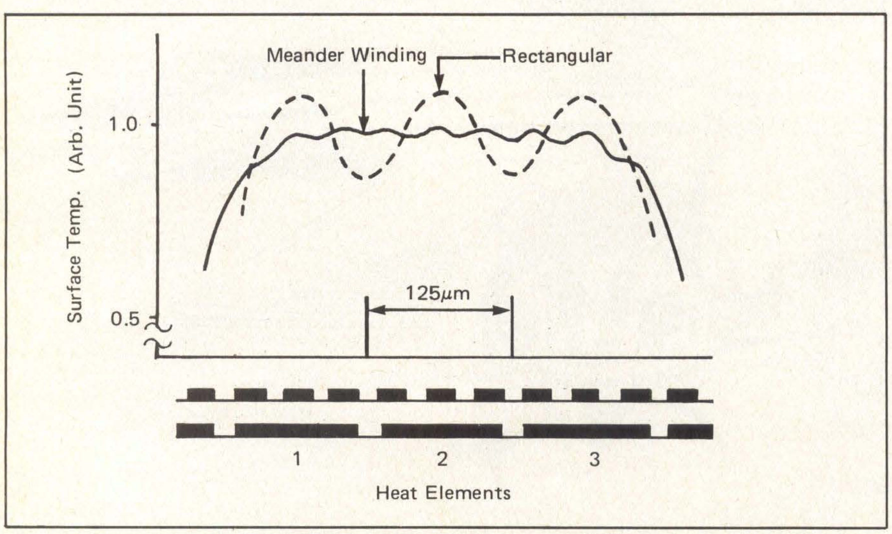

Figure 5. The surface temperature distribution of the heat elements

Fig. 5 shows the surface temperature distribution of three adjacent heat elements. One of the features of the meander winding heat element is its perfectly uniform surface temperature distribution. Since the hot spot observed in the center of conventional rectangular heat elements does not occur, the maximum temperature is lowered and a local strong thermal stress is reduced.

future applications

Our print head has electrodes distributed on both sides (64 bits on each). The head driver is a beam lead IC and its beam pitch is 120 μm (extremely high density). Further, a beam lead element using a glass substrate has been developed for multilayer wiring.

Life-expectancy tests on the print head, run at speeds of 2 ms per dot line, have already confirmed a life of over 1 $\times 10^8$ dots. This demonstrates that the new thermal print head can be applied to super high speed facsimile (printing time for A4-size paper is less than 5 secs).

In addition, high speed gray scale recording has been accomplished by use of thyristor characteristics. In this case, heating time is controlled by changing the trigger timing bit by bit.

Application to color recording that requires higher print temperatures is expected in the future.

— T. Iwabuchi, T. Yoda, S. Shibata, K. Murasugi
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Technique Extends UNIBUS Addressing

The PDP-11 family of computers owes its technological success to the flexibility of its data bus. The UNIBUS, introduced in 1970, was the first minicomputer bus which allowed direct communication between any two devices on the bus without processor assistance. The UNIBUS has 18 address lines, allowing a maximum of 256K bus addresses. Peripheral control registers and main memory are assigned addresses from this range, with the highest 8K reserved for (but not restricted to) the I/O addresses. The PDP-11/44 and PDP-11/70 address more than 248KB of main memory by providing a separate memory bus.

In many applications memory spaces larger than the 248K bytes are required to contain the executable program code, while the additional processing power (and cost) of the 11/44 or 11/70 is not wanted. The traditional answer to this problem is disk overlays and checkpointing. An unfortunate side effect is greatly reduced throughput arising from the disk bottleneck created by the solution. Faster disks and even solid state "disks" are used to reduce the magnitude of the problem. These techniques, however, are limited because the UNIBUS is employed in the transfer of data between the device and main memory.

Innovative Design

A joint effort by Periphonics Corp. and Brookvale Associates has yielded an alternate expansion technique which maintains the standard UNIBUS structure while permitting essentially unlimited UNIBUS address space.

unibus window

In the UNIBUS architecture, as in most of today's mini and microcomputers, memory is addressed by establishing a one-to-one mapping of bus addresses to physical memory cells. (The CPU may or may not use a memory management unit to map logical program addresses — 16 bit values — to physical bus addresses — 18 bit values — before presentation to the UNIBUS.) The Periphonics approach employs a multi-valued mapping of UNIBUS addresses to physical memory.

A UNIBUS window is defined as a contiguous set of UNIBUS addresses which are controlled by PERIPACS. Many devices or memory cells are present at each address within the window. The PERIPACS device determines which will respond when a UNIBUS address is asserted. Memory cells are grouped into logical sets (planes) which do not have multiple mappings. A memory card with 64KB of memory is the usual plane. One of the memory planes controlled by PERIPACS will be enabled by software, effectively placing that memory into the window. Up to 16 planes of 64KB each may be installed in a system, allowing a maximum of 1MB of added memory.

The crux of the patented technique for mapping logical (UNIBUS) to physical (PERIPACS) memory is an active backplane. Software directives to PERIPACS cause the activation or deactivation of memory slots in the backplane. Placing a memory plane into a window is accomplished by the activation and deactivation of the appropriate backplane slots. Once memory is enabled by "placement into the window" it operates at normal UNIBUS/memory transfer rates. Exchanging the contents of 64KB of main memory with its previous contents can be done with only 2 PDP-11 instructions, and with virtually no bus activity.

software support

Software supporting PERIPACS was developed by Brookvale Associates. The DEC supplied RSX-11M operating system provides the host environment, with PERICHECK replacing the RSX LOADR program. RSX allocates main memory by an algorithm which employs partitions. A partition is a contiguous set of UNIBUS addresses. PERICHECK provides a "partition swapping" mechanism which is an extension of the native checkpointing algorithm. PERICHECK uses PERIPACS controlled memory (rather than disk) for the checkpointing of active, but not running tasks. Thus PERICHECK effectively increases the amount of main memory available for executable task images. Disk checkpointing is still available if the PERIPACS space is totally used.

performance

A test bed installation was created for evaluating PERIPACS/PERICHECK performance. The system was a PDP-11/34A with 192KB of main memory, 128KB of PERIPACS memory, and RPRO2 disk drives for checkpointing. The RPRO2 is capable of a sustained transfer rate of 205KB per second.

The application environment was simulated by two tasks

(APRIME and BPRIME) which computed and printed prime numbers. The tasks work in sequence, one after the other, passing the results of one calculation to the other to serve as the basis of the next calculation. Both APRIME and BPRIME were made to occupy the same 28KB partition, thereby forcing the idle task to be checkpointed. When both tasks are co-resident in main memory (the fastest configuration) prime numbers are calculated at the rate of 2.5 per second. With PERICHECK handling the checkpoint context switch, the rate is 2.14 primes per second. Finally, with ordinary disk checkpointing the rate is 1.16 primes per second. PERICHECK offers a throughput increase of:

$$\frac{(2.14 - 1.16)}{1.16} = 84.5\%$$

This compares favorably to the maximum possible increase of:

$$\frac{(2.50 - 1.16)}{1.16} = 115.5\%$$

Further increases in PERICHECK performance are possible if PERIPACS were operated at context switch level, rather than at checkpoint level. This change would eliminate the execution of the LOADR task, which requires about 32 msecs per operation (checkpoint read or checkpoint write). To take this approach would require that PERIPACS be incorporated into the heart of the RSX executive. The PERICHECK approach affects only the LOADR task. In most RSX configurations the LOADR task can be replaced with another LOADR task in a matter of minutes, without SYSGEN. The PERICHECK approach was chosen in order to maintain the extreme ease of implementation and maintenance sorely missing in many software packages on the market today.

future

The next step in the current effort for PERIPACS would be to extend the range of operating systems which support its operation. RT-11 and RSTS are excellent candidates because of their widespread use in business-type application environments which usually involve high checkpoint loading.

Many uses beyond expanded application memory space are also possible. For instance, PERIPACS memory could be assigned to and managed by the disk driver programs. The memory space would then be used as a cache for disk, permitting writes to be sequenced for maximum efficiency, and bypassing certain disk reads totally.

If the PERIPACS backplane were enhanced to support a local LSI-11 processor with each memory plane a multiprocessor environment would be created. Each memory plane would become an independent processing unit, with the potential for operating its own local I/O devices. Communications between master and subordinates would be at memory/bus speeds. This makes it practical for the subordinates to share the master's peripherals, such as disk. If additional UNIBUS windows were allowed, multiple trees of subordinates could be defined. Any node of one tree could communicate with a node of another tree at direct memory rates. It would be an extremely powerful multiprocessor configuration.

—Victor DiCara
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Bohemia, NY 11716

Circle 197

Trends In Backpanel Wiring Materials Selection

James J. Anastasi
Electronic and Industrial Cable Div., Brand-Rex Co.
Willimantic, CT

Optimum selection of materials can reduce overall system costs. During the past two years, metal prices have experienced severe fluctuations. Copper prices rose 43%; silver rose from $5.00/oz. in 1978 to $50.00 before dropping to $15.00/oz. Petroleum-based insulations increased 40% and will rise further.

Here are guidelines to aid in material selection: • Tin-plated copper conductor with PVC or tape-wrapped insulations can be used where manual or semi-automatic wire termination methods are employed. • Silver-plated copper conductor with closer tolerance, high-temperature insulations can be used with fully automated termination equipment. • Irradiated and simple PVC insulations can be substituted for more expensive materials, where close tolerances are not critical. • Tefzel and FEP/Kapton can be used in high-density packaging applications, since they both have low dielectric constants and exhibit the lowest cross-talk parameters. • Lower cost insulations such as PVC and Kynar can be used in low-density packaging applications, since electrical requirements are not as critical. • In terms of backpanel wire economics, silver-plated copper/tape-wrapped, and silver-plated copper/FEP/H film are the most expensive combinations. The least expensive combinations are tin-coated copper with PVC insulations.

trade-off analysis

Today, trends toward more efficient packaging techniques are directing wire and cable manufacturers to offer wider lines of varied conductor/insulation combinations for backpanel wiring to make better uses of materials.

System designers can take advantage of these lines with minimal analysis to find the optimum wire-types that give the best performance at the least cost. For example, low-cost tin-coated conductors covered with high-temperature insulations could be specified to maintain critical performance requirements, while keeping overall costs at a minimal level.

CONDUCTOR-PLATING COMPARISON

CONDUCTOR			CHARACTERISTIC			
	LIFE STABILITY	TERMINABILITY	SOLDERABILITY	NOMINAL OPERATING TEMPERATURE	COST	USES
TIN-COATED	Conductivity and solderability deteriorate with heat aging at rated temperature, copper and tin tend to migrate and tin oxidizes.	Good — but contact resistance increases with time and can be highly variable.	Good originally. Deteriorates with shelf life.	150°C	Low	Where temperatures are relatively stable.
SILVER PLATED	Excellent — no loss of conductivity with heat aging at rated temperature. Solderability shelf life is good.	Excellent — contact resistance remains low.	Excellent.	200°C	Very high	In high temperature applications or where there are extreme temperature variations.
SILVER-FLASHED NICKEL PLATED	Conductivity remains stable with heat aging at rated temperature.	Excellent — contact resistance remains low.	Excellent.	250°C	High — but lower than silver-plate.	In high temperature applications or where there are extreme temperature variations.

Other ways of maintaining high performance at minimum cost include the use of lower-cost irradiated and simple PVC insulations. Also, silver-flashed, nickel-plated copper is beginning to show promise as a lower-cost alternative to silver-plated copper conductors.

In addition to wrapping and termination, backpanel wire must also withstand mechanical bending and turning, stretching forces, temperature variations and sometimes hazardous environments. Physical properties of backpanel wiring include:

• Ruggedness: conductor and insulation should be able to withstand mechanical abuse during and after installation.

• Abrasion and cut-through resistance: insulation should be tough enough to withstand nicks and scrapes. In addition, pressure by pins or component edges (caused by improper routing during wiring and wrapping, second and third-level wrapping in densely wired areas, or high tension during wrapping) should not cause the insulation to cold-flow exposing the conductor and creating a potential short circuit hazard.

• Strippability: insulation should adhere firmly to the conductor within a manufacturer's specified limits. If adhesion is not precisely controlled, problems can occur: the conductor may be elongated or broken if the insulation is too tight, or automatic equipment may jam if the insulation is too loose.

• Minimum shrinkback: insulation should not slip back on the conductor due to shrinkage caused by temperature cycling.

• Minimum curl: wire should not curl due to being coiled when the wire was on its spool. Curled wire can cause jamming or malfunctions in automatic equipment. On long runs, curling can also make the wiring difficult to handle due to a tendency of the wire to "pop-up" from the backpanel.

• Chemical resistance: insulation should resist chemical breakdown from exposure to solvents sometimes used in circuit board production and cleaning. Deterioration of the insulation can lead to conductor corrosion or oxidation that may result in short circuits or increased electrical resistance.

other wiring requirements

Backpanel wiring performance is highly dependent on wiring techniques. Guidelines for good wiring include:

• Short wire runs: to reduce or eliminate signal crosstalk.

• Distribution of electrical loads: to reduce resistances and minimize heat build-up. For example, two wires may have the same point-to-point connections to share the load and dissipate heat effectively.

• Point-to-point wiring: an inherent characteristic of wire-wrapping techniques. Each connection is terminated at both ends of each wire. If the same signal is to go to another point, a second wire must be wrapped at a second level on the intermediate pin and connected to the next pin in the circuit. Standard pins are limited to two or three wire-wrapped connections per pin.

• Optimum wire routing: pre-planning is required on all but the shortest wiring runs. However, wire-wrapping techniques have advanced to where much of the wiring and routing can be determined using the latest computer-aided-design techniques. In addition, physical placement can be accomplished with automated equipment.

Another wiring characteristic, often a factor in wire-wrapped circuit, is the insulation's dielectric constant. This is not a consideration in backpanel wiring if individual wires are spaced apart. D

PRINTERS:
A Technology/Marketing Overview

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By the early 1980s, printing technologies will be refined and, in some cases, made obsolete. User needs will change, encompassing distributed processing, WP, various types of graphics, higher throughputs and electronic communications. Prices and equipment dimensions will shrink further; printers, like computers, will become more sophisticated.

the printer market

Current estimates from GML Information Services Corp. in Lexington, MA show that 1250 different printers are commercially available, spanning 10-15 different printing technologies with about 120-130 companies making serial printers, line printers, or both.

Worldwide industry revenues on computer printers has been predicted to exceed $6 billion by 1982. Just three years ago, the total worldwide market for printers was estimated at $3 billion. Growth rates also have been predicted in the range of 25-30% annually through the first few years of the decade.

As a start, let's define some commonly-used terms.

1. Printing technology-impact vs. nonimpact. An impact printer is any variation of the traditional typewriter, where a hammering part strikes paper through inked ribbon. Nonimpact printers use electronic, chemical or heat (thermal) signals to etch symbols onto coated or treated paper.

2. *Character form-fully-formed vs. dot matrix.* Fully-formed characters are constructed from solid lines, like those produced by a typewriter. A dot-matrix character is made from a formation (matrix) of closely-packed dots.

Most solid-character printers use an impact printing method (drum, band, chain/train, daisy wheel/thimble). Dot matrix can be performed by printheads that fire solenoid-driven wires, produce electrical discharges on coated papers, laser-beam images, or heat impulses.

3. *Printing sequence-serial vs. line vs. page.* These terms describe the amount of data the printer fires off in one printing sequence. For example, serial printers print single characters in sequence, one at a time across the page. Line printers do an entire line at once. Finally, page printers have a prodigious appetite, since they rapidly print whole page images at a time — sometimes in splitseconds.

dot matrix print-quality

Will dot matrix win the word processing/formal business fields, where custom alone dictates solid-character printing? It seems so. Print quality has traditionally been measured against highly-defined, solid-character print. The standard grades of comparison stack up this way: *Letter quality:* Highly-legible print resembling letters typed on finest-quality typewriters. In demand for word-processing and formal business applications. *Correspondence quality:* Good quality, legible print (closely-packed dot matrix sometimes acceptable). Used for most common correspondence in business applications. *Draft quality:* As the name implies, OK for banging out rough drafts, payrolls, and internal materials. Least legible of the three, but certainly readable. Nearly all fully-formed character printers will produce letter-quality printing. However, they usually have lots of moving parts that threaten reliability, little or no graphics capability (bar codes, line graphs, plotting), and high supplies costs.

Dot matrix, on the other hand, has high printing speeds with fewer moving parts, suiting it for high-demand situations. Dot matrix makers, trying to break into the lucrative market, made great improvements to print quality. Methods like multipass printing (where the printhead makes two or more passes to overprint the same symbols), and overlapping printhead wires can each produce denser, clearer print very close to letter quality.

Machines are marketed as workhorses for 80% of draft and correspondence material done at typical WP stations. Why should users create a bottleneck by using slow daisy-wheel printers for a draft on an internal memo? If dot matrix can catch on with users for traditional letter-quality applications, that technology will take over the WP printer marketplace.

reducing printer noise

With printers being used for more desktop, office and home applications, factors like quiet operation and humane design have become primary considerations for printer manufacturers. Both regulatory and market pressures from users and international government safety agencies have forced printer makers to modify or totally redesign their machines. Impact implies noise; however most manufacturers have been able to use extra padding in the shell, sound-absorbing covers or product redesign to attain noise levels around 70 dB. Dataroyal has succeeded in reaching as low as 63 dB on its IPS-5000 printer.

Some nonimpact technologies — thermal, ink jet, laser/xerographic — are inherently quiet, but are limited by high printer price, slow speed, frequent maintenance, expensive supplies and no multi-copy printing.

A recently-introduced quiet-writing printer uses a mP-controlled stylus that traces symbols through a ribbon onto paper. The impact produces a slight tapping sound.

Agencies like the West German VDE and OSHA are aiming at office-noise reductions to the range of 55-60 dBs, posing quite a challenge for manufacturers, since noise in a typical office without people talking runs about that level. A typical typewriter or daisywheel printer produces over 80 dB.

new applications

Just a quick glance at the number of new applications for computer systems makes it clear that printer makers must offer either very versatile, expandable printers, or a wide range of special-applications models. The industry's designs and technologies will respond to these growing market areas: personal computing, small business/commercial, distributed dp, future applications of electronic mail and office communications, WP and remote work stations.

American-based printer companies competing overseas must meet the applications needs of the international customer with different configurations and options. More language sets, quieter performance, special forms-handling features all take extra time and development cost.

Printer makers must often offer a wide product range. Each application requires printers with different prices and capabilities. For example, distributed processing calls for medium-speed, moderately-priced printers for remote locations. Expanded computer-room functions need very high throughput, while desktop installations require less-expensive, compact printers with broad capabilities.

technologies

Daisy wheel. The daisy wheel is a fully-formed character, serial impact printer, using a metal or plastic print element with a circular series of flexible spokes radiating from a hub ("daisy wheel"). The printer rotates the wheel to position the arm with the proper character, then hammers the arm forward onto the ribbon and paper. Each spoke carries one embossed character.

Specs are as follows: Print speed: 30-55 cps. Pricing: \$2500-\$6000 (all prices are end user). Suppliers: Qume, Diablo Systems, Olivetti, Wang, C. Itoh. Benefits: excellent print quality, interchangeable, 96-char. elements in various fonts. Disadvantages: slow printing speed, relatively high price due to lack of competition, reliability, cost of supplies, operator intervention for character-changing. Product trends: improvements in price/performance, reliability. Manufacturers are predicting increased competition from dot matrix that will force some cost reduction. However, daisy wheel won't become that much faster. Daisy wheels will remain in the market where their advantages are needed.

Thimble technology is a faster (55 cps) variation of the daisy wheel. Here, the spokes-and-hub element resembles a thimble, with spokes radiating up from the hub. Each spoke holds two characters. The thimble rotates on a vertical axis, and moves up and down to choose either the upper or lower row of characters.

Specs are as follows. Pricing: from \$2350 to \$3300 (NEC Spinwriter). Suppliers: NEC Information Systems, Inc. Benefits: excellent print quality, faster than daisy wheel, 128-character sets, higher reliability, interchangeable fonts. Disadvantage: still relatively slow. Product trends: same as daisy wheel. Solid-character printers won't get much faster, since the "seek time" (time used to rotate and position print element) can only be reduced to a certain point, using more expensive controllers and sacrificing reliability. They will have their place in the market.

Impact dot matrix holds the greatest market share. It uses a printhead containing banks of wires fired at high speeds against an inked ribbon and paper. Wires are arranged in certain matrix formats ($5 \times 7, 7 \times 7, 9 \times 7$); firing is timed to produce a dot grouping (matrix) in the desired character shape. Both serial and line printers are available.

Specs are as follows: Print speeds: from 60 cps to 900 cps. Pricing: \$600-\$5000 (some special-applications models up to \$7000). Suppliers: Dataroyal, Centronics, IBM, DEC, TI, Mannesman Tally (line), others. Benefits: high speed, least expensive technology (printer and supplies), reliability, ROMs and PROMs can store numerous character sets, bidirectional printing, compressed print and proportional spacing, greater flexibility in character formation. Disadvantages: Print quality (a factor in certain uses). Product trends: multipass or overlapping printing to improve print, quality, noise reductions, much lower printer cost relative to other technologies. Will hit \$500 for capable small business models.

Band. Currently the most popular impact line printer, this fully-formed character technology employs hammers that strike a rapidly-rotating metal or plastic band or embossed characters into inked ribbon and paper. Traditionally found in computer rooms, medium-speed band printers are appearing in offices and remote-processing stations.

Specs are as follows. Print speed: 150 lpm to nearly 4000 lpm. Pricing: \$3,000-\$65,000. Suppliers: Centronics, Dataproducts, Data Printer, Documation, Control Data, GE. Benefits: choice of speed ranges, fully-formed characters, operator-changeable print bands in variety of fonts and sets, now designed for more quiet operation and more compact dimension. Disadvantages: noise, printer takes up lots of space, bulky, higher cost (compared to dot matrix). Product trends: lower printer costs, lighter weight, compact size, quieter operation. Vendors are adding sound-proofing, acoustic cabinets, and are using modular construction and higher production volumes to drive down noise and price.

Drum. One of band printing's parents, drum uses characters embossed around a cylindrical drum which rotates on a horizontal axis for positioning. A hammer then strikes the back of the paper and ribbon onto the drum.

Specs are as follows. Print speed: 300-2000 lpm. Pricing: \$4,000-\$15,000 (OEM-only). Producers: Dataproducts (OEM-only), Dataprinter (OEM-only). Advantage: reliability. Disadvantages: limited number of fonts, drum not easily changed by operator, noisy, problems with print quality, legibility, (hammer must be precisely timed to strike when drum is positioned; sometimes makes wavy lines). Product trends: possibly headed for extinction.

Chain/train. Another parent to band, these technologies have a series of individual character slugs, rather than one rotating band. In chain printers, the slugs are connected and pull each other past the striking hammers in a chain. In train, they are not connected and push each other past the hammer set.

Specs are as follows. Print speed: up to 1500 lpm. Pricing: \$10,000-\$112,000. Suppliers: IBM, Dataproducts, Dataprinter. Advantage: good print quality. Disadvantages: competes with band printing, fonts and character sets not easily changed by operators, high pricing. Product trends: same as with drum. Band should dominate market areas where drum and chain/train now exist.

Ink jet (nonimpact) technologies use a variety of methods to spray a controlled stream of tiny ink droplets accurately onto paper, forming either dot matrix or solid characters.

Specs are as follows. Print speed: 72 cps to 300 cps (45,000 lpm in specialized Mead system). Pricing: $2,000-$30,000 (lower speeds). Suppliers: IBM, Siemens, Silonics, Inc., Mead Digital Systems (high-speed models). Benefits: very quiet operation, character and font flexibility, high-quality printing, even at relatively low speeds (drop-on-demand method). Disadvantages: complexity and printer cost (continuous-stream method), reliability (ink clogs, accuracy), overcoming market reluctance, no multiple copies. Product trends: very promising technology for 1980s — if market accepts. Potential for color and elaborate graphics.

Drop-on-demand system: Simple, lower-cost method for low- and medium-speed printers. Ink flows from a closed reservoir or cartridge through a filter and into a multi-nozzle printhead. Ink is shot toward the paper at an electrical pulse signal.

Continuous-stream method: A single-nozzle head ejects an ink stream. Rapid horizontal head motion breaks the stream into single droplets, which then are charged by an electrode. The charged drops are deflected vertically onto the paper by two other charged plates. The 99% of the ink not used for character formation falls into a gutter to be recycled through the system.

Thermal. A relatively low-cost, quiet, flexible techology, best suited for personal, limited small business, scientific and communications computing. The printhead moves across a specially-treated, heat-sensitive paper; individual wires in the head are selectively heated to darken the paper in dot-matrix patterns or graphics. Distributed thermal heads use one heating element for several columns in a head that moves back and forth as characters are printed. Others use heating elements for every dot.

Specs are as follows. Print speed: 30-120 cps (to 500 lpm in distributed-head models). Pricing: $1000-$5000. Suppliers: TI, Dataproducts, NCR. Advantages: quiet operation, simple design, high reliability, can print on specially-coated preprinted forms or papers, compact size, light weight, portable. Disadvantages: no multiple copies, special coated paper is expensive, sometimes difficult to get, fades with age; doesn't resemble plain paper, heads clog and wear from ink/clay-based coating despite wax additives. Product trends: faster printing speeds, some improvement in print quality, lower prices for printer and supplies, some improvement in paper quality and appearance, more graphics capability.

Electrosensitive uses a special paper constructed of a metallic coating over a black background, and voltages applied to matrix elements in a moving printhead burn off the coating to reveal the black layer (etches dot-matrix character onto paper).

Specs are as follows. Printing speeds: 160-6600 cps. Pricing: $500-$3000. Suppliers: Comprint, SCI Systems, Univac. Advantages: quiet operation, high print speeds (useful in high-demand situations), Relatively-low printer cost, compact light weight, portable. Disadvantages: low print quality, coated paper looks like aluminum foil, paper wrinkles and smudges easily, no multiple copies. Product trends: major markets will be confined to personal, desktop and CRT computing. Some improvement in paper quality and price likely.

Electrostatics use a specially-coated paper that passes over matrix elements or styli, which then pass electrically-charged dots in character groupings onto the paper. The paper goes through a toner bath; the charged dots attract ink particles to create character images.

Specs are as follows. Print Speeds: 300 lpm-18,000 lpm. Pricing: $5,000-$165,000. Suppliers: Honeywell, Versatec. Advantages: high printing speed, quiet operation, font and character versatility, can plot and print simultaneously, offers competitive printer price against competition (impact printers, xerographic). Disadvantages: special paper and toner expensive, liquid toner must be frequently replenished, no multiple copies, not practical for preprinted forms, print quality less acceptable than xerographic. Product trends: designed for very high speed printing and plotting. Improvements will be in price of printer and supplies (paper, toner).

Laser/Xerographic. Promising future technology for the 1980s, especially for high-quality/high-demand output on plain paper or preprinted forms. Uses a rotating polygon mirror to deflect a modulated fiberoptic light beam, or laser beam, onto the photosensitive surface of a drum or belt. This latent image attracts toner to the imaged areas. This toner is then electrostatically transferred to the paper and fused into a permanent image.

Specs are as follows. Speed: 10 pages/minute (ppm) to 215 ppm (19,000 lpm). Pricing: $145,000-$325,000. Suppliers: IBM, Xerox, Siemens, Hewlett-Packard. Advantages: excellent print quality, tremendously-high printing speeds, can form photo image from original copy, or from an electronic forms generator, electronically-stored fonts can be mixed on same sheet, prints 8-1/2 × 11 output in horizontal or vertical format, uses plain paper or printed forms, simultaneously prints, firms, logos, and preprints its own forms. Disadvantages: no multiple copies, expensive printer price, frequent maintenance, high cost for supplies. Product trends: These printers should see use in facsimile output systems, distributed data systems, and very high demand work stations. If printer and supply prices come down, this technology could be the answer to the print speed vs. quality question.

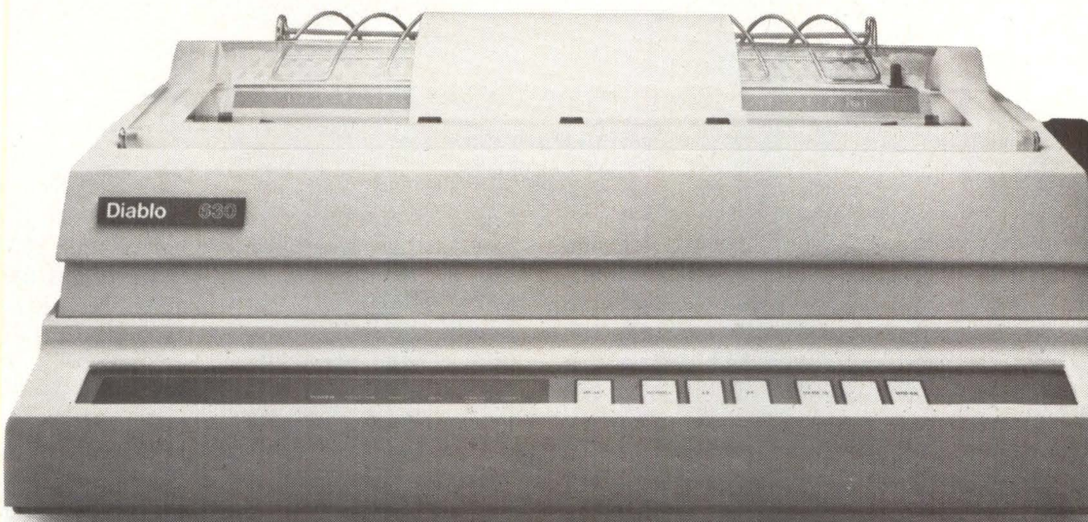
conclusion

The printer industry and its technologies are just one facet of the larger market for computer systems, equipment and services. Predicted to grow at 30% or better annual rate into this decade, the dynamic, volatile computer marketplace will undergo profound changes in the 1980s and 1990s. Competition will become even more global in nature: international competitors like the Japanese will enter the personal and business systems markets with strong intention and commitment.

Right now, and for the first half of the 1980's, there is a distinct split between suppliers in the small business systems market and the personal/home entertainment area. However, by the second half of the decade, major companies now making video games will move into the tremendous, untapped potential for home computing, electronic communications, and possibly into the low end of the business system market.

The 1980s will witness many large corporate powers making strong financial and marketing ventures to capture large shares of the computer and communications market. Horizontal as well as vertical integration will become more important, as these corporations offer complete systems for business and home with communications network services. D

If you want a choice in print wheels, there's only one choice in printers.

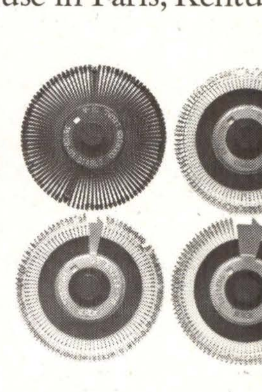


The Diablo 630.

It's the only one that lets your customers use either metal or plastic print wheels. Which means they can choose the print wheel that's just right for the job.

The 630 works as well with a 96-character plastic daisy print wheel as it does with an 88-, 92-, or 96-character metal daisy print wheel. In over 100 different type styles.

Every 630 has a fully strappable power supply. It's as easy to use in Paris, Kentucky as it is in Paris, France. So you only need to stock one printer for international and domestic markets.



It has fewer moving parts than competitive printers, which makes it more reliable. And it offers unsurpassed print quality. Compatibility with Diablo supplies. And bi-directional printing capability.

The 630 is the only printer in the world that uses both metal and plastic wheels.

Once your customers hear they can change their print wheels, they're going to be changing their printers.

To Diablo 630 printers.

Diablo Systems

XEROX

Circle 25 on Reader Inquiry Card

Printer Controllers: How To Choose Them

Stan Margulis,
MDB Systems, Inc.

A printer controller is defined as a single PC board residing in a host computer and which transfers data in parallel to the printer. A serial interface is not generally considered to be a printer controller. Controllers typically consist of three interrelated sections: the interface between the board and the computer bus; an I/O section with interface circuitry for operation of a given printer; and circuitry which ties the bus interface and printer interface together (and provides for the control and logic functions required for addressing and general operation). Controllers are either Programmed I/O or DMA. PI/O boards (the most common) although easier and cheaper to manufacture than DMA, can have a negative impact on system throughput. Familiar PI/O controllers include those for PDP-8, PDP-11, LSI-11, Perkin-Elmer, and some Data General computers. DMA controllers have a direct port to memory. Once a data transfer is initiated, flow of data between memory and printer, via controller, is independent of program control. DMA boards are used in IBM Series/1 and with some Data General computers. Software which operates the printer via controller is commonly referred to as a Printer Driver Routine or Printer Handler within the computer Operating System.

An alternative to the use of a parallel printer controller in a system is, generally, a serial interface (RS-232C or current loop). The determining factor in selection will probably be the printer itself. Some printers use only a serial interface, while almost all offer an RS-232C or current loop as an option to a standard parallel interface. Therefore, serial is widely available.

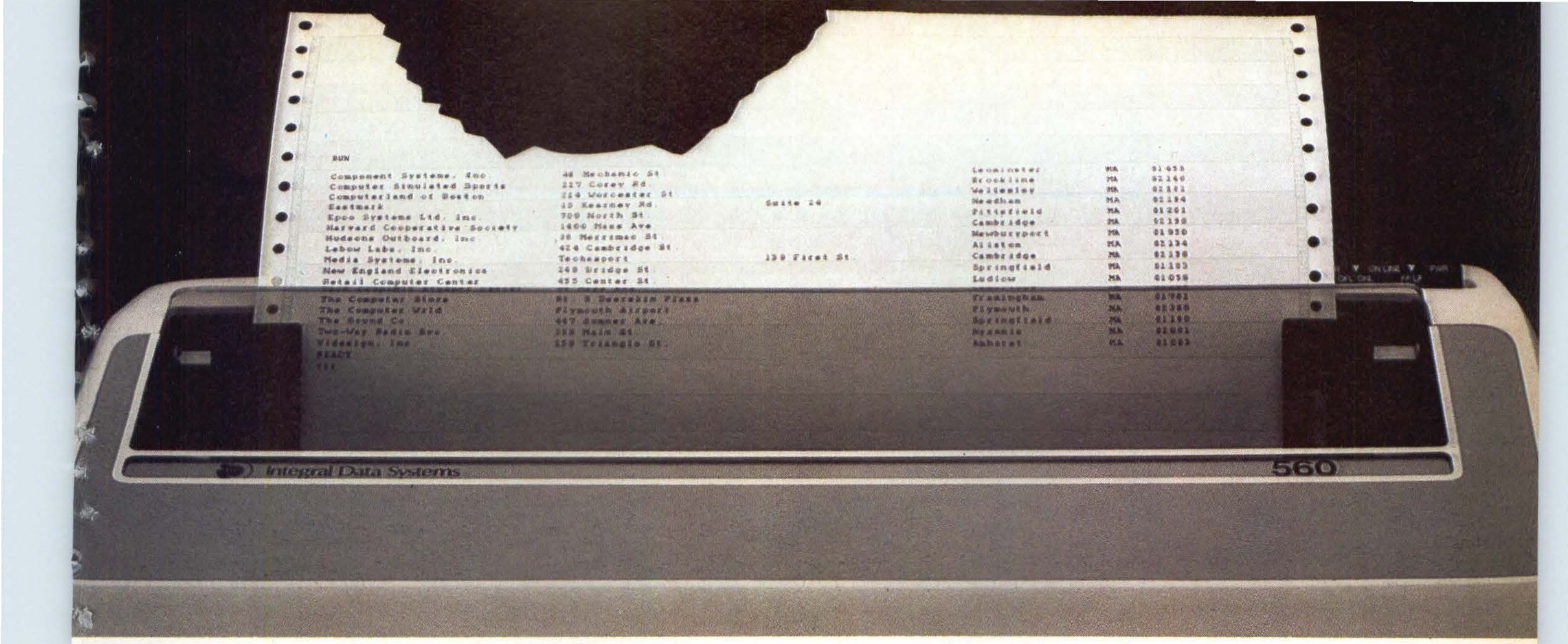
A major consideration for the buyer when selecting a serial interface is buffer overrun. Many printers which employ a serial interface, print at relatively slow speeds. Therefore, unless data transmission is slowed to compensate, the transmission can eventually overrun the printer buffer with a resulting loss of data. To avoid this, many printers send back a signal (status line toggle or control character) to the computer to stop Data send. Unfortunately, most serial interfaces are not mechanized to recognize busy signals, and overrun can still occur. As a deterrent to this event, a computer program may send NUL, or non-printing pad characters, after a CR or LF command. However this can drastically reduce throughput. A better solution seems to lie with serial interfaces that are equipped with buffer-ready monitor circuits. Such a circuit allows the printer to run at maximum speed with no overrun. At present only four such interfaces are available (all from MDB).

A major determinent for selection of a parallel printer controller versus a serial interface is distance and the long distance capabilities offered by controller and/or printer manufacturers. With normal TTL logic, most controllers and printers can operate up to 50 feet. If differential drivers and receivers are used, then the parallel data transmission distance can be increased up to 3,000′ or 4,000′ . The printer controller must provide this capability. Equally important, the printer must be able to convert differential signals to the TTL signals offered by most printers. Some manufacturers make controllers that have differential circuitry, and also products that give this capability to the printer.

Even serial interfaces have their distance limits. The RS-232C is generally good for up to 50′. Current loop is used for longer distances. A newer concept in long distance serial interfaces is RS-422 (differential drivers and receivers) circuitry. Some manufacturers provide this capability for their serial interfaces and also for the printer.

Advances in serial interface design notwithstanding, by far the fastest way to transfer data between a computer and a printer is by parallel means; i.e., a printer controller. Fig 1 compares speeds.

The major considerations in selecting a printer controller, are price, viability of source, support and implementation of special features. The first three must be considered together. Many buyers prefer to purchase a printer subsystem, (including the printer and controller), from the computer manufacturer. They want a single source to be responsible for the whole package without multiple service calls and "finger pointing" if something goes wrong. In addition, the buyer may suspect that the host manufacturer will not service the computer if a "foreign" peripheral is attached. This is not



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as spool and cassette ribbons, separate heavy-duty stepper motors to drive the print head and advance the paper, plus true tractor feed.

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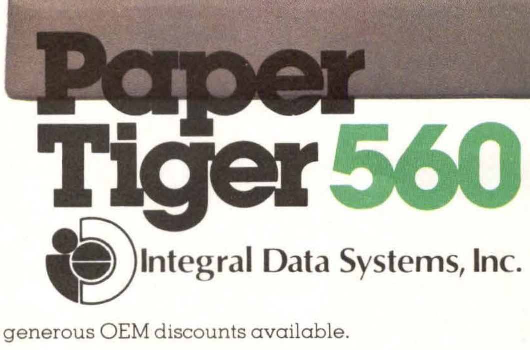

Paper Tiger 560

Integral Data Systems, Inc.

*Suggested single-unit U.S. price. Very generous OEM discounts available.

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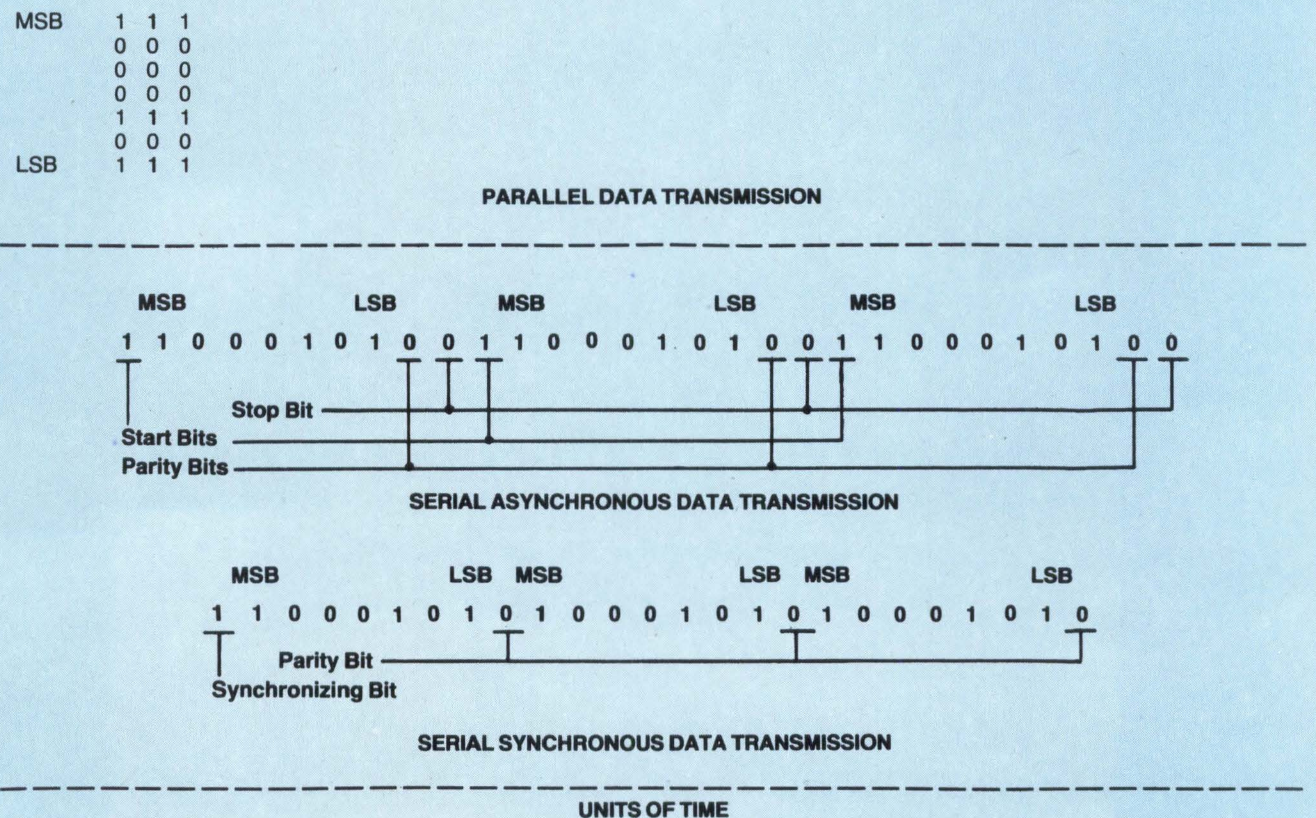
COMPARISONS OF DATA TRANSMISSION TECHNIQUES

The charts below show the relative time for data transmission by 'Parallel', and Asynchronous and Synchronous serial means. The binary designation for the letter "E" as defined in the ASCII specification is used in the example.



As it is quite evident from the above examples, the parallel data transfer is the quickest method to transfer data to a printer, resulting in the most throughput to the printer or other similar device.

correct. Even a computer salesperson will recommend a foreign peripheral if essential to systems needs.

Regardless of reasons for buying a complete subsystem from the computer manufacturer, it's hard to justify their figures. Most computer manufacturers have a limited selection of printers and printer speeds. Therefore, the user may have to settle for less performance than he really wants. And, at the same time, the cost differential is incredible when compared to "independent shopping." For example, one major computer manufacturer offers a 300 lpm printer for its system at $13,500. But the user can easily buy a 600 lpm printer from a number of peripheral manufacturers for $8,000. Add to that a controller from an independent at about $2,000 and the user saves $3,500 to get twice the speed. If the user wants to settle for 300 lpm he can save $6,000 from an independent purchase. If both the printer and controller manufacturers are carefully selected based on reputation and established customer base, the user should have no problem with system support. Meanwhile, he's saved a bundle.

The customer may also choose to buy his complete printer subsystem from a printer manufacturer who offers such subsystems. These companies have, in effect, done the customer's independent shopping for him. The buyer still saves money. In addition he gets support for peripheral and controller from a single source.

One of the special controller features that the buyer must take into consideration is utilization of a printer VFU. A vertical format unit is a memory device that is used to control paper advance to predetermined areas of the page. Not all host software supports a VFU. The potential buyer must be aware of this loose end when selecting a printer from an independent to make sure he gets the options required. At the same time the controller must be configured to operate with VFU, either mechanical or electronic.

Many printers provide graphics capability for printing block characters, bar codes, plotting, and foreign language sets. The controller must have the capability to transmit to these printers the required signals or control codes (preferably under operation of the host computer standard printer/driver routines).

A final controller feature (which the buyer should be aware of) allows operation of the printer by the controller independently from computer software. Many printers have a built-in self-test that can exercise up to 95% of the printer. What still remains unchecked, however, is the actual printer interface (drivers, receivers, connectors) presented to the controlling device. Ability of the printer controller to generate a test pattern, transmit it to the printer and cause the printer to print the pattern takes much of the guess work out of problem identification. Visual indicators on the controller (LEDs) offer additional assistance for troubleshooting and fault isolation. D

The One Printer Solution for the Two Printer Problem.

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The new Dual-Mode 200 brings speed and uncompromising print quality to business and professional applications.

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Electronics Corporation

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Circle 27 on Reader Inquiry Card

PRINTER SHOWCASE

Printer manufacturers are shown together with each company's most recent model. Additional models are available from most manufacturers. Circle numbers on "bingo cards" to get more information from company. The June issue of DD will list manufacturers of Printer Components, Mechanisms, Controllers, Supplies, etc. That upcoming buyers' guide (Part 2) will also be expanded to include names of manufacturers not listed here. Printer/plotters will be covered in a special issue. For inclusion in the Part 2 listing (printers, printer components, printer supports, etc.) write to "Showcase Editor" **Digital Design,** *1050 Commonwealth Ave., Boston, MA 02215.*

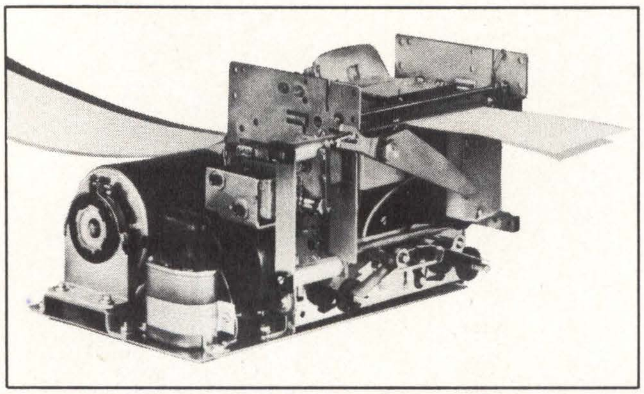
Model T-3000 Line Printer

Standard character set plus another 128 user defined sets can be stored. "On line" printing of transmitted data. Speed: 300 lpm at 4800 baud. 1K buffer standard; 4K optional.

Tally Corp., 8301 S. 180th Street, Kent, WA 98031
Circle 251

Model M-1400 Ticket Printer and Punch.

Size: approx. 6″ × 8″ × 10″. Produces 3″-wide descriptive tickets plus machine-readable code. Print head: 5 × 7 dot matrix. Prints bidirectionally up to 4 lps with 20 cpl. Punches 50 cps.



Westrex OEM Products, 1140 Bloomfield Ave., West Caldwell, NY 07006 **Circle 297**

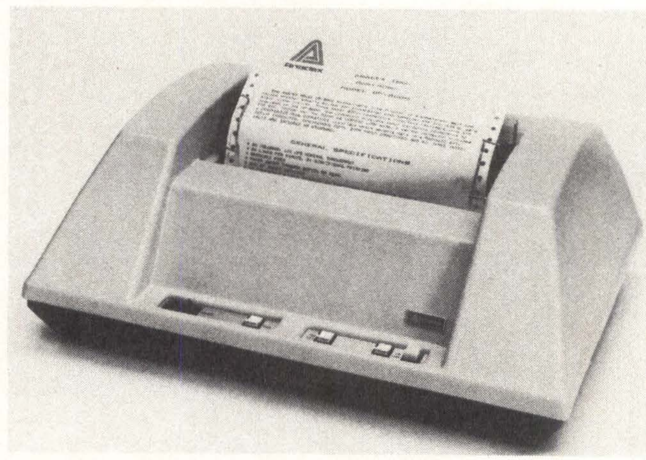
Model: Series 2000 "Terminet."

GE's newest "blade" terminology. Printhead is a compact, light weight blade matrix. Nine-layer blade laminate. Each blade individually charged to produce quiet, reliable printing. APL/ASCII keyboard. Produces 9 copies at 200 cps with a paper slew rate of 20 lps. Last copy clearly legible.

General Electric Co., Waynesboro, VA 22980
Circle 295

Model DP-9000 80/132 Column Printer

Dot matrix printer. High density graphics. Full ASCII 96 character set including descenders and underlining. Bi-directional up to 200 cps.



Anadex, Inc., 9825 De Soto Ave., Chatsworth, CA 91311
Circle 292

Model PM LC11 Dot Matrix Line Printer

200 cps print speed. Bidirectional printing. Variable print densities; 1 × 6 dot matrix graphics mode.

Plessey Peripheral Systems, 1691 Browning Ave., Irvine, CA 92714 **Circle 296**

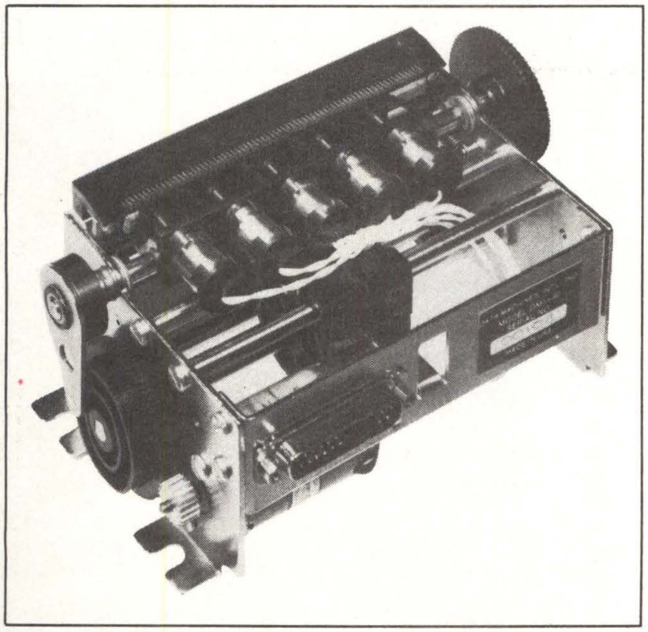
Model: Stylist 360 Daisy Wheel

For word processing and small business. Modular design allows instant service through onsite swap of any of 5 modules. Accommodates 100 characters in several sizes, fonts and languages. 17 cps speed, bidirectional logic seeking.

Pertec, 12910 Culver Blvd., Los Angeles, CA 90066
Circle 273

Model DMI-40 12 VDC Printer

Impact, line, dot matrix. For use in portable, mobile and severe industrial applications. 200,000 characters from a 5 amp/hr battery. Prints alphanumeric and limited graphics. Patented solenoids. Speed: 120 LPM.



Data Machines International, Terrace Hill, Ithaca, NY 14850 **Circle 280**

Model AP-40 LM

Alphanumeric mechanism, 40 column. 150 lpm print speed. 2 dot Matrix printheads.

Gulton, Inc., MCS Div., E. Greenwich, RI 02818
Circle 294

Model: Spinwriter 3500Q OEM Printer

Requires only 3 major parts for repair. New technique eliminates more than 100 parts. Size of standard typewriter. 30 cps print speed. Quiet 58 Dba rating. Has 3 μPs.

NEC Information Systems, 5 Militia Dr., Lexington, MA 02173 **Circle 298**

Model DS 180 Printer

Logic-seeking bidirectional printing. 180 cps. 9 × 7 dot matrix. Accommodates 6 part forms. 38 programmable features. Non volatile memory protects settings in power-out. Optional multiplexer joins 4 CRTs to one printer.

Pacific Mountain States, 6319-B De Soto Ave., Woodland Hills, CA 91367 **Circle 287**

Model MT-80S

125 cps, 80/132 column bidirectional printer. Interfaces RS-232. Supports full upper and lower case 96 character ASCII set. Up to 16 cpi on original plus 3 copies. μP controlled. 240 character buffer. Additional 1K buffer optional.

Microtek, Inc., 9514 Chesapeake Dr., San Diego, CA 92123 **Circle 300**

Model LP300 Matrix Line Printer

High resolution characters on a 9 × 7 matrix. Print speed: 300 and 600 lpm with 96 character ASCII. 132 column format.

Texas Instruments Inc., Box 1444, M/S 7784, Houston, TX 77001 **Circle 288**

Model HPI-33 Line Printer

μP-based. For Hewlett-Packard 300/3000 Series minicomputers. Voice activated controller and responder. Choice of 7 line printers with speeds from 300 to 1800 lpm.

BDS Computer Corp. Menlo Park, CA 94023
1120 Crane St. **Circle 290**

Model B-900 Line Printer

Has several bands and specialized and foreign language character sets. Print Speed: 1100 lpm @ 48 characters down to 600 lpm @ 96 characters. Vertical spacing, 5 clear copies, diagnostic display. Easy loading ribbon and paper.

Southern Systems, Inc., 2841 Cypress Creek Rd., Ft. Lauderdale, FL 33309 **Circle 291**

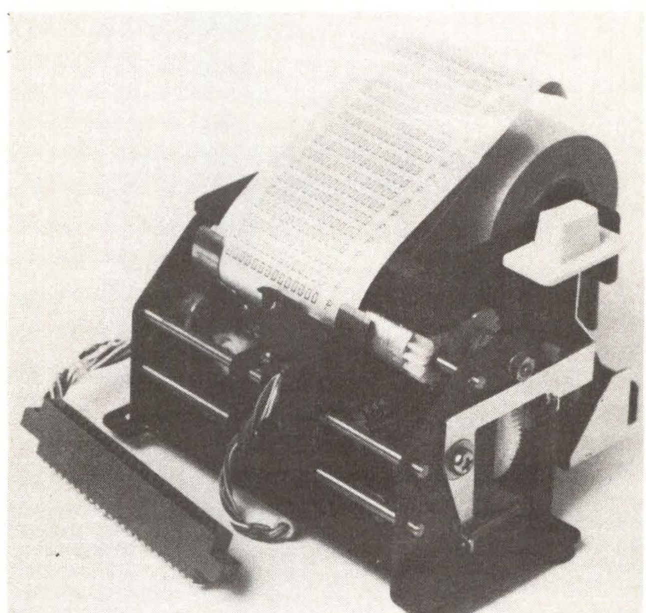
Model KH102 Thermal Printhead

8.3″ wide one piece heating element. Dot density 152 d/in. Model KH106 Thermal Printhead 8.5″ wide heating element. 203 d/in. Maximum print speed is 4 ms/line for both. Enabling electronics, drive circuits, shift registers and diode arrays mounted in compact 40 terminal IC flat packs.

R-ohm Corp., Box 19515, Irvine, CA 92713 **Circle 282**

Model DC-4004A 48 Column Discharge Printer

5 × 7 matrix. Low cost printer uses 4.72″ paper. Speed: 144 cps. MTBF = 144 million characters.



Hycom, Inc., 16841 Armstrong Ave., Irvine, CA 92714
Circle 293

SPECIAL REPORT
PRINTER SHOWCASE

Model MDP-125 Matrix Printer

125 cps speed, 9×9 dot matrix. Plugs into Intellec μC Development Systems. Bidirectional, 96 character ASCII character set. Descenders and underlines.

EMC Corp., 385 Elliot St., Newton, MA 02164 **Circle 271**

Model DIP-81 Dot Matrix

7×7 or 14×7. Upper/lower case. 100 cps bidirectional print out. Uses bond paper in sheets, roll or fanfold.

DIP, Inc., 121 Beach St., Boston, MA 02111 **Circle 257**

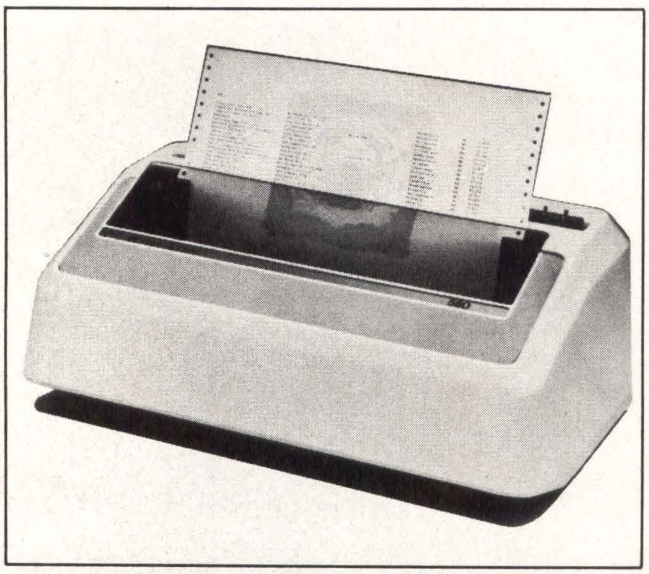
Model 8230 Line Printer

1400 lpm. 132 columns. Fast and quiet.

Houston Instrument, One Houston Square, Austin, TX 78753 **Circle 260**

Model Paper Tiger 560

Full width 132-column printer. High speed plus correspondence-quality overlap dot-matrix printing. Bidirectional



at 150 cps speed. Can also produce illustrations, charts, diagrams. Option: "DotPlot" raster graphics printing.

Integral Data Systems, 14 Tech Circle, Natick, MA 01760 **Circle 275**

Model 1750 Daisy Wheel

Speed: 60 cps. 132 columns. ASCII input.

Xerox, Printer Division, 701 S. Aviation, El Segundo, CA 90245 **Circle 274**

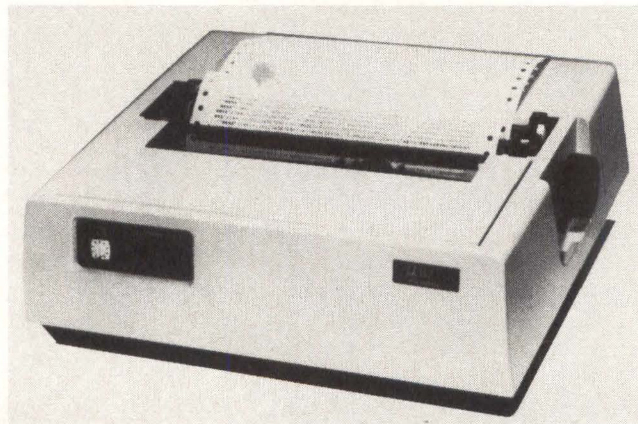
Model E_z Print 21

Small-screen CRT printer. Compact dot matrix impact printer for use with small screen CRTs. Records all terminal data on adding machine paper. 21 column format. 42-1/2 cps speed. Special fonts and foreign characters available.

Mepcom International, 15181 Business Ave., Dallas, TX 75234 **Circle 270**

Model Microline 82

Seven-pin head (less than 4 oz in wt) produces sharp, crisp copy and graphics on plain paper, and multipart forms.



Bidirectional printing at 80 cps. Interfaces: RS232C serial, Centronics compatible parallel. Friction platen.

Okidata Corp., 111 Gaither Dr., Mount Laurel, NJ 08054 **Circle 279**

Model 800

Prints up to 6 different character fonts. 72, 80, 96, 120 and 132 cpl. Prints 3 copies. Long life cartridge ribbon. 4 interface modes: IEEE 488, standard parallel, 20 mA current loop, RS232. Speed: 19,200 baud. High Speed paper advance, graphics output, buffer memory.

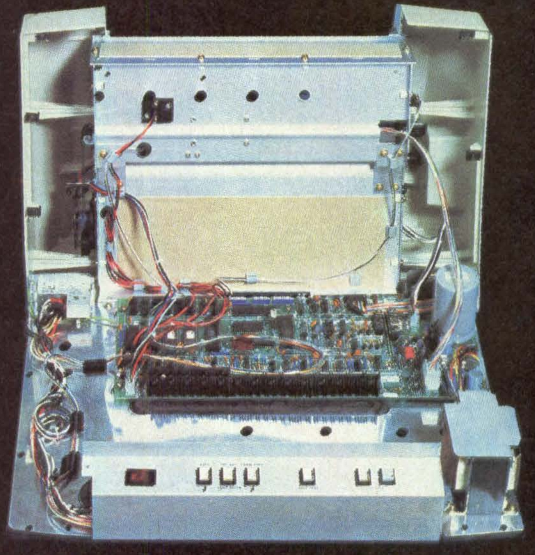
Base 2 Inc., PO Box 3548, Fullerton, CA 92634 **Circle 254**

Model 2087 Matrix Printer

Interchangeable with IBM Model 2 and compatible with entire 3270 family. Print speed: 180 cps (50% faster than IBM 2). Highly legible 7×8 dot matrix character. 132 CPL at 10 CPI. Bidirection movement. Head logic seeks shortest path between lines. 70-yard nylon ink ribbon cassette. Has audible alarm for errors, endings, etc.

Memorex Corp., San Tomas at Central Expwy., Santa Clara, CA 95052 **Circle 259**

Say Ahh...



Our New grafixPLUS™ 80-column printer opens wide for easy servicing.

Introducing the newest members of our grafixPLUS™ family—the DP-9000 Series 80/132 column printers—built on the same tradition of quality printout, solid design and low cost of ownership established by our 132/220 column DP-9500 Series.

A Case for Serviceability

Not that is comes up often, but want to get inside? Simple. Just remove a few screws and the clamshell case swings open exposing all major components. This easy access plus built-in self-test and minimum component count yields an MTTR of one-half hour. The 9-wire print head replacement's even simpler . . . two screws and it's out. Without opening the case. And without a service call.

Performance Plus

The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

Interface Flexibility

The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

When you're ready for a printer (or several thousand), look into the grafixPLUS DP-9000 Series from Anadex—you'll find an open and shut case for quality. Contact us today for details, discounts and demonstrations.

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SPECIAL REPORT
PRINTER SHOWCASE

Model 88T Dot Matrix Printer

Dual tractor/pressure-roll paper feed; serial/parallel interface. Handles multicopy fanfold forms from 1" to 9.5". μP control for 80, 96, 120 or 132 columns. 100 cps speed.

Micro Peripherals Inc., 2099 West 2200 South, Salt Lake City, UT 84119 **Circle 276**

Model 736 Line Printer

For IBM 3270. Produces solid character by single impressions. Interchangeable optional printer elements. Choice of typeface includes foreign.

Interface Systems Inc., 462 Jackson Plaza, Ann Arbor, MI 48103 **Circle 286**

Model TH240 Thermal Printer

80 column. 240 lpm. up to 1200 baud on-line. Available as alphanumeric only or as A/N plus plotting configuration.

Printer Systems Corp., 1 W. Deer Park Rd., Suite 104, Gaithersburg, MD 20760 **Circle 267**

Model 43 BSR Teleprinter

For multi-point private line systems. μP controlled tabletop unit. Compatible with various ANSI 3.28 protocols. 16K buffer for editing. Send and Receive. 80 keys. Aux port for optional line printer.

Teletype Corp., 5555 Touhy Ave., Skokie, IL 60077 **Circle 269**

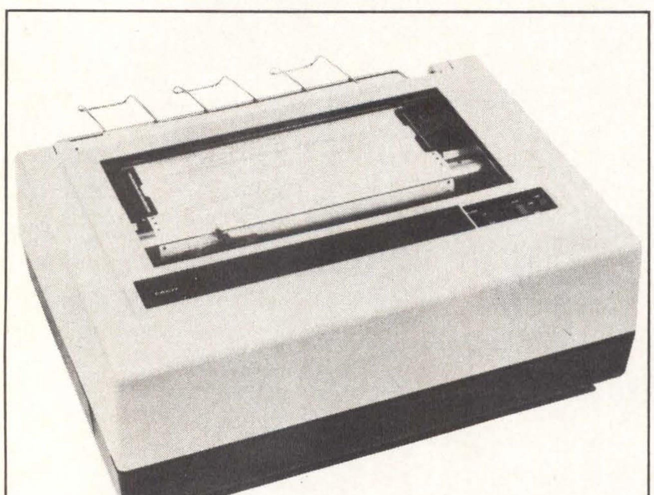
Dot Matrix Printer

60–180 cps. 80–132 columns ASCII input.

Dataroyal Inc., 235 Main Dunstable Road, Nashua, NH 03061 **Circle 268**

Model 4540 Serial Matrix Printer

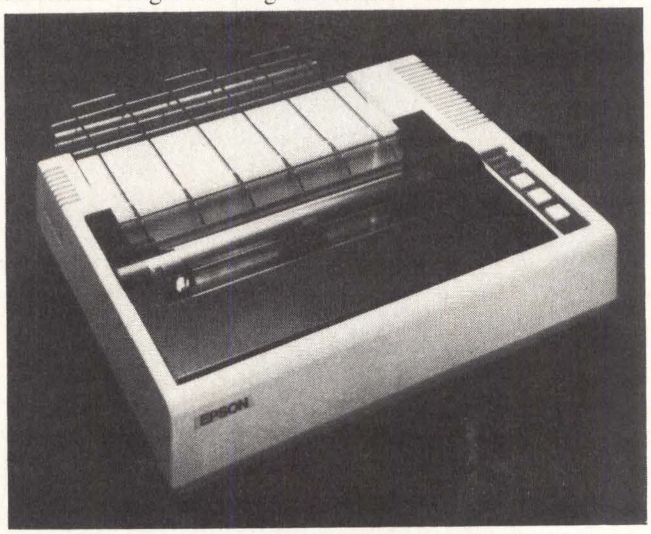
9×9 dot matrix. 9 stored force flexible hammers. Speed: 250 cps bidirectional. Long printhead life — 500 million characters.



Facit Data Products, 66 Field Point Rd., Greenwich, CT 06830 **Circle 255**

Model MX-80 9×9 Dot Matrix

Bidirectional printer, 80 cps. Choice of 40, 80, 66 or 132 columns. Logic seeking functions. Prints 96 ASCII, 64



graphics, and 8 international characters. Print head life: 100×10^6 characters. Disposable print head, replacement: $30.

Epson America, Inc., 98 Cutter Mill Rd., Great Neck, NY 11021 **Circle 277**

Model #180 Dot Matrix

60–180 cps speed. 132 columns, ASCII character set.

Alpha Matrix Inc., 1020 Atherton Dr., Salt Lake City, UT 84107 **Circle 272**

Model: Innovator 202

Using heavy-duty chain technology, unit prints fully-formed characters at 300 LPM. Clear ulc characters on up to 6 copies. Unit based on Teletype Model 40 printer mechanism. Noise level 60 dba (lower than office typewriter).

Innovative Electronics Inc., 15200 Northwest 60 Ave., Miami Lakes, FL 33014 **Circle 299**

Model 2511 Printer

Printer speed: up to 200 cps. Lear Siegler 9 pin matrix print head. Bidirectional printing with full underlining and two descender capabilities. Digital servo control.

Digi-Data Corp., 8580 Dorsey Run Rd., Jersey, MD 20794 **Circle 285**

Model 88G Impact Matrix Printer

100 cps bi- or unidirectional. Full upper and lower case 96 character ASCII set. 7×7 matrix. Optional: a high resolution dot graphics mode. μP Controlled.

MPI, 2099 West 2200 South, Salt Lake City, UT 84119 **Circle 265**

Model 200 Dual Mode Matrix Printer

Speeds: 165–250 cps in DP mode, 42–60 cps in WP mode. Stores up to 6 different character fonts in ROM. Single sheets, multiple part forms or pin feed paper.

Malibu Electronics Corp., 2301 Towngate Rd., Westlake Village, CA 91363 **Circle 266**

SPECIAL REPORT
PRINTER SHOWCASE

Daisy Wheel Printer

5 μPs provide complete text formatting, margin justify and proportional spacing. Also functions as an electronic typewriter. Can print in reverse, (white characters on black background to highlight text.)

Howard Industries Inc., 2031 E. Cerritos Ave., Bldg. 7K, Anaheim, CA 92806 **Circle 256**

Model 6450 Thermal Printer

Alphanumeric. Few moving parts. Non-impact. Programmable for either RS-232C or 20 mA current loop. 110 or 300 baud. 64 character. 21 characters/line.

Digitek, United Systems Corp., 918 Woodley Rd., Dayton, OH 45403 **Circle 261**

Model 737 Correspondence-Quality Printer

High quality 18 × 9 dot matrix characters. Prints descenders and underlines. Justifies right margin. Steel platen. Prints subscripts and superscripts. Quiet. Has an optional acoustic cover.

Centronics Computer Data, Hudson, NH 03051 **Circle 278**

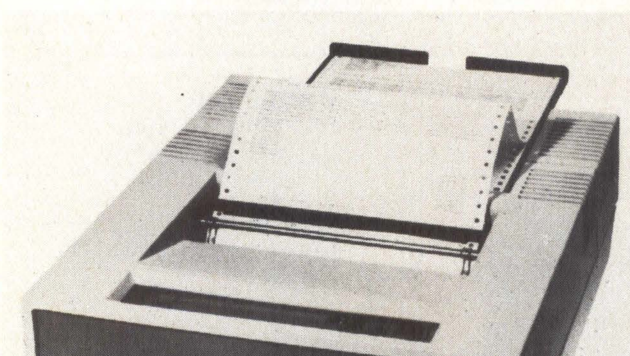
Model 3001 Band Printer

Chaintrain type hammer. 5 horizontal and vertical paper adjustments. Speeds from 150 to 1100 lpm. Operator changeable fonts. Money-back guarantee on performance.

Data Printer Corp., 99 Middlesex St., Malden, MA 02148 **Circle 263**

Model 5080 Dot Matrix

Heavy duty, 80 column, bidirectional. Stand alone printer. Choice of 4 standard interfaces: 8-bit parallel, RS232, TTY

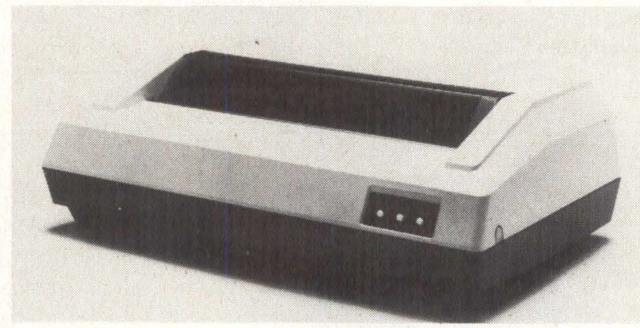


and IEEE-488. Upper and lower case ASCII characters. Speed: 100 cps. Full graphics, 480 dot columns/line. Sprocket paper advance. 360 character buffer.

Victor Data Products, Walter Kidde Co., 3900 North Rockwell St., Chicago, IL 60618 **Circle 252**

Model Comet II Dot Matrix (9 × 7)

136 column. 2 character size, single or bidirectional. Print speed: 125 cps (40 lpm bidirectional) on forms up to 15-1/2″ wide.



C. Itoh Electronics, 5301 Beethoven St., Los Angeles, CA 90066 **Circle 253**

Model Magnum 3400 Big Printer

IBM 5256 replacement. Variable size print from 1″ to 10″ high as well as 150, 300 or 600 l/in. normal text. Plotting capability. Handles labels, barcodes, forms. Upside down and sideways print capability. Mixed size on same line.

Quality Micro Systems, PO Box 81250, Mobile, AL 36689 **Circle 284**

Model 9380 Band Printers.

Hammer technology. Model speeds from 360 lpm to 1440 lpm. Choice of 69 print bands. 22 languages. 132 columns on standard 8-1/2″ × 11″ paper.

Control Data Corp., 1480 N. Rochester Rd., Rochester, MI 48063 **Circle 262**

Model MQI 150 Dot Matrix

9 × 9. Upper and lower case with descenders. Handles up to 6 part forms from 2″ to 15″ in width. Life expectancy of head is 600 million characters.

MQI Computer Products, 18381 Bandilier Circle, Fountain Valley, CA 92708 **Circle 258**

Model DE-800SG 80 Column Printer.

Full dot graphics, complete μP control. Contains up to 8K EPROM program and 4K RAM to control all hardware functions. Accepts paper width 1.5″ to 10″. Prints up to 5 part forms.

Data Electronics Devices, 18 Bridge St., Salem, NH 03079 **Circle 283**

Model 286C Model 2 Impact Printer

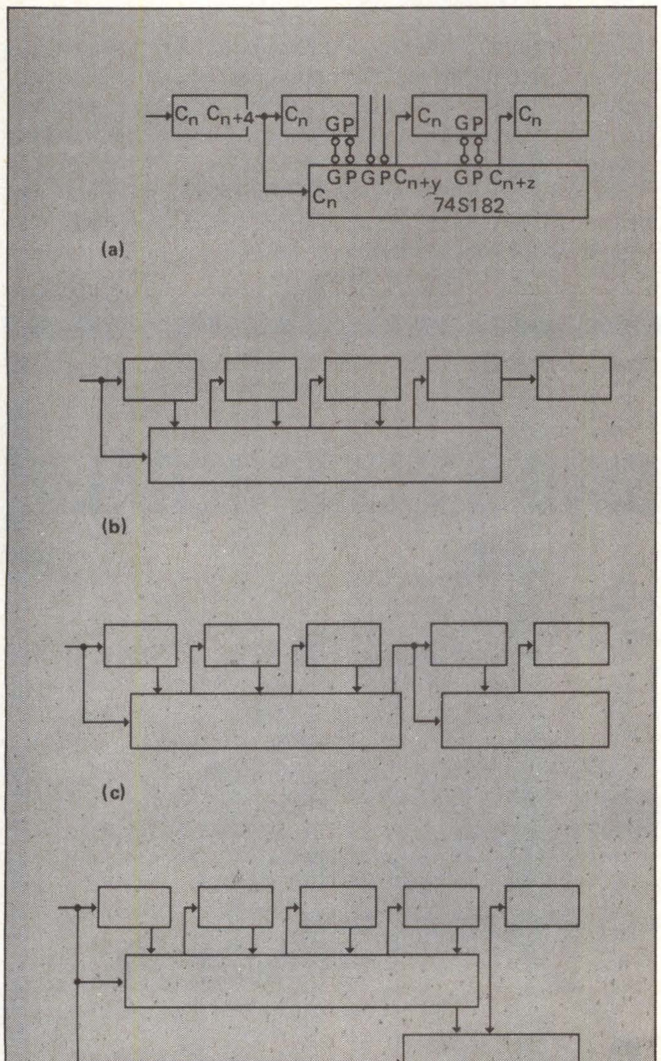
1355 WP Hy Type II mechanism. Metallized printwheel for high print quality. 45 cps. Bidirectional, "lookahead" features for a faster print speed of 60 and 80 cps. Compatible with Telex and IBM units. μP-based.

Telex Computer Products, 6422 E. 41st St., Tulsa, OK 74135 **Circle 264**

(This listing continues as Part 2 in the June issue.)

Fine Tuning the ALU Carry Path Boosts Speed 12%

Harry Holt,
National Semiconductor Corp.



Block diagram A depicts a 16-bit shifted look ahead. In this 20-bit system, (B) shows the single-level method; (C), the chained method; and (D), the two-level method.

Although cycle times of the 2900 family's ALU (arithmetic logic unit) have improved by 60% during the past two years, the method of connecting the 74S182 lookahead carry generator hasn't changed and could limit system speed. Most application information for the 74S182 shows three standard connections for 16, 32 and 64-bit ALUs. When ALU cycle times approximated 200 ns, standard connections serve quite adequately. But now that cycle times are less than 80 ns, look ahead carry techniques can improve system performance as much as 12%.

Basic Methods for lookahead carry include: ripple carry, conventional single-level, multi-level and shifted.

Although ripple carry is slow in 8-bit ALUs, it turns out to be the fastest method. Also, you can use ripple carry in combination with other methods to eliminate parts while adding very little to system cycle time. In most applications, the four basic methods require trade-offs between parts count and system speed. However, some designs generate the highest performance with the fewest parts.

The least well-known of the four methods, the shifted carry-in, results in slightly slower performance in a 16-bit solution. In certain word sizes it can be the fastest method. Furthermore, freeing a set of G,P pins on the 74S182 can provide advantages in those applications in which a sign-extension is required.

factors affecting choice

Before applying the look-ahead carry methods to the various word length ALUs, let's look at some of the factors other than raw speed that affect the choice of method: parts count, board space, board layout, board-to-board partitioning, sign extend, sequencer cycle time, work length expansion, different system architectures and current spiking. While parts count, board space and board layout are obvious considerations, the others deserve a brief comment.

Board-to-board partitioning refers to those systems in which half of the ALU is packaged on one board and half on another. Obviously, all carry-in methods are not readily adaptable to partitioning, unless a sufficient number of connector pins are available.

Sign-extend requirements may favor the method that frees a G,P input on one of the lookahead carry circuits.

Sequencer cycle time in a pipe-lined system may be the limiting factor in overall system speed. Therefore, saving a few nanoseconds in the ALU may not be worthwhile.

Future word length expansion becomes important whenever it generates a need for building several models. For example, 16 bits of address can address 64K words; twenty bits, 1M words. If the ALU is used to compute addresses, the carry method optimized for 20 bits rather than 16 bits may be desirable.

The architecture that we assumed for this study will not be used in every system. Consequently, the availability and timing of input signals, worst-case delay paths and added components will affect the results shown in the following section. Thus, each design could require a separate study to achieve optimum results.

Current spiking becomes important when one method causes several ALUs to change output states within a few nanoseconds of each other. When current spiking causes system noise problems, you should perhaps use an alternate method.

applying various methods

In the following discussion of systems ranging from 4- to 64-bit words, IDM2901A-1 ALU timing is used for the register elements. Because several different choices of pipeline register are available, the times shown do not include the clock-to-register output delay. Finally, we have based the comparisons on the time required to add two registers and obtain a valid output, such as A + B => Y.

4, 8 Bits ripple carry is clearly the best for 4- and 8-bit systems. Thus, no further discussion is necessary. Register-to-register add time for 8 bits is 75 ns.

12 Bits At present, the conventional single-level method is best (77 ns for 12-bit applications). However, if future bit-slice devices can provide A, b=> Cn+4 as fast as A, B=G,P, and Cn => Cn+4 as fast as 74S182s G,P => Cn+y, ripple carry perform just as fast. Such a development illustrates the need for designers to rethink the problem continually as new parts become available.

16 Bits Without sign-extend, a conventional approach provides optimum performance (77 ns). The shifted method is 8.5 ns slower without sign-extend. However, if sign-extend is required, the shifted method might be as fast, in addition to eliminating multiplexers. (This example illustrates the fact that two parts of a system optimized independently may result in an overall slower system.)

20 Bits As word width increases beyond 16 bits, some of the less-conventional approaches begin to offer advantages. First, consider the more obvious approaches, such as single-level and chained. You could come up with yet another by deleting parts from the conventional 32-bit system.

From a timing standpoint, the single-level method uses fewer parts and by requiring a single lookahead carry rather than two. Only a small portion of the second lookahead carry circuit is used. Furthermore, you can replace this portion with a circuit consisting of 1/6 of a 74S04 and 1/2 of a 74S51. In addition to supplying a lower power, lower cost solution, the replacement of the second lookahead carry circuit actually saves 1.5 ns. Even more surprisingly, the shifted method requires fewest parts, but runs faster (85.5 ns) than other methods. Here, the speed-cost tradeoffs both favor the same solution.

24, 28 Bits A conventional 32-bit solution (deleting one or two ALUs) yields identical times (98 ns) for 24 and 28 bits. However, the shifted chain uses fewer parts and is faster

(96 ns). With the same parts count, chained and two-level methods yield the fastest times (87.5 ns) for 24- and 28- bit ALUs.

32 Bits The conventional approach for 32 bits exemplifies the two-level with helpers method. For 32 bits, this method provides a register-to-register add time of 98 ns. It runs faster than the chained and two-level methods (103.5 ns) that are optimum for 24 and 28 bits. Another method, the shifted two-level, again uses fewer parts and is considerably faster than the conventional approach (87.5 ns).

Simply deleting parts from the 64-bit solution provides a 98ns solution for 36-bit ALUs. A word of caution: this arrangement is not the path to the most significant slice (MSS). It turns out that this path is only 87.5 ns long. The 98ns path extends to the output of the second MSS. The shifted two-level with helper method also produces a 98ns result, but if you replace the "helper" with the circuit, the resulting run time is 96.5 ns.

The double-shifted two-level method requires only two parts, turns out to be the best two-part solution for all word sizes from 32 to 64 bits and runs for 101.5 ns. The shifted two-level with helper and double-shifted two-level method also turn out to be optimum three-part and two-part solutions for 40- and 44-bit ALUs.

48 Bits The double-shifted two-level method is also the optimum two-part solution for 48 bits. It contains three-part solutions. The shifted three-level solution results in a 114ns system, the double-shifted three-level, in a 101.5 ns. The worst-case path varies between the two solutions. This variation means that you must evaluate several paths to make sure you have found the longest one.

The four-part system improves performance slightly (98 ns) and may not be worth the additional expense. It is, however, the best four-part choice from 48- to 60-bit range. This method is referred to as shifted two-level with helpers.

52 Bits Not a particularly popular ALU size. The 52-bit system nevertheless provides an opportunity to demonstrate another lookahead carry method — the double-shifted, two-level with helpers. It also turns out to be the fastest three-part method for word widths from 52 to 64 bits. This method results in a 117.5ns run time for 52-bit systems.

56 Bits ALUs of 56 bits are becoming common in floating point systems using 56 bits of mantissa and 8 bits of exponent. Deleting components from the conventional 64-bit approach results in a 98ns solution. However, the shifted, two-level with helper method can provide the same speed with four parts.

60 Bits The fastest 60-bit solution uses the conventional approach for 64 bits with one ALU deleted. This method results in a 98ns solution. The shifted, two-level with helper method is a four-part solution that results in a 103.5ns speed.

64 Bits Again, the fastest 64-bit solution (98 ns) is the conventional approach. The fastest four-part solution uses a double-shifted, two-level with helper method (117.5 ns).

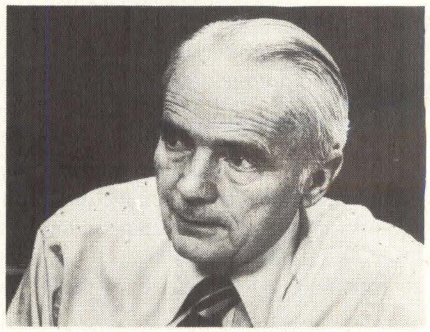
conclusions

No one solution is best for all applications. Even the "faster" solution may not be optimum for a specific system when you evaluate such factors as parts count, system wiring, board space. Evaluate each application individually by looking at the requirements of the system and the devices available, and by using sound engineering judgment.

For further information, contact National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 408/737-5000.

Flexible Data Media: Keeping Pace With Drive Technology

We recently interviewed Verbatim board chairman Reid Anderson and his management team to give our readers more insight into the technology and market potential of the mini-media market. Besides Anderson, we talked to Marshall Hart, director of quality; Gerald Newton, VP of operations; Dr. Geoffrey Bate, VP, advanced development; and Tom McDonald, manager of market planning and research. The following (edited) interview discusses technical, marketing and industry overview information.



Q: What recent advances have been made in diskette media technology?

A: Technical improvements have enabled us to produce diskettes with longer life and greater information packing density. These have been accomplished through application of new particles, new lubricants, and new coating and surface finishing techniques. The new 5-MB disk is one result of these improvements. Also, in one new product offering we make use of Lexan, a polycarbonate, for the jacket material. The jacket is normally the first part of the product to be affected by high temperature. Specially selected liner materials were also used. The disk itself was coated with an improved, thermally-stable magnetic coating. And, we are now developing more stable substrate material, jacket materials and magnetic coatings for future extreme environment applications.

Q: What breakthroughs in procedures and media have allowed the industry to attain the current storage densities and tracks per inch?

A: Breakthroughs in a number of different areas have contributed: Better (smoother) surfaces are now attainable; higher outputs on the newer oxide formulations increase signal-to-noise ratios; thinner oxide coatings result in higher recording frequencies (higher densities) and higher inside track resolution; drive manufacturers have contributed more accurate head positioning mechanisms resulting in up to 100 tracks per inch capability; and the use of head position and spindle speed servo mechanisms by drive manufacturers.

Q: What breakthroughs have been made in tape cartridge technology?

A: Major recent breakthroughs have been made in upgraded belts and rollers, including floating rollers and expanded capacity and durability of the magnetic medium.

Q: What is your overall projection for the future of flexible disks and cartridge tapes in the next ten years?

A: The market for flexible disks should increase over the next five years contingent on more storage being attained (3-8 MB). Drives must also become more compact, and media improved in reliability and durability. Durability improvements call for improvements in both head and drive mechanisms as well as in media. We expect these things to happen, and to see continued substantial growth (more than 20 percent per year). We project a doubling of storage capacity, with resulting improvements in cost-performance every few years.

Q: What market force drives development of flexible disk technology? Do drive manufacturers exert constant pressure on media producers, or do the media producers continually push the drive vendors through development of higher quality and capability media?

A: Drive manufacturers led the way with innovations in size (minidisk versus 8″), mechanical capacity (single-sided versus double-sided) and controller electronics. Media manufacturers have consistently responded to these challenges with advanced products, permitting still higher recording densities and longer media life in both normal and hostile operating environments. We expect this "push-pull" relationship between drive and media manufacturers to continue in the future. The ultimate beneficiary will always be the end user.

Q: Besides diskettes, you are heavily involved in the manufacture of tape cartridges. Does the current boom in Winchester back-up technology create the main market for this product? Are there other major markets for tape cartridges?

A: Cartridges have a variety of applications in current systems technology, and are widely considered the most cost-effective method to back up the emerging family of "mini-Winchester" disk drives. We believe cartridges will find wide application as back-up for drives of capacity greater than 30 MB, comprising 30% of all cartridge shipments by 1985. Other major markets for this product are in telecommunications and certain military applications.

Q: Do diskettes and tape cartridges compete with one another in the marketplace?

Every advance in drive or head technology must be either followed by or led by equivalent advances in media. The media maker must communicate and cooperate with the drive and head manufacturers constantly. Otherwise, the result may compare with an ultra high-speed movie camera with no film available to fit its capabilities.

A: They compete only in the sense that each is a method of capturing, storing, and replaying information magnetically. In general, diskettes have an advantage over cartridges in random data access and lower system cost, while cartridges have much higher data capacity (20+ MB) than current flexible disks (5 MB). Though sometimes found together (as in the IBM 5100) they usually occur as alternatives in different systems and applications.

Q: What is your overall projection for the future of flexible disks and cartridge tapes in the next ten years?

A: There is a strong future ahead for both media technologies. We project a growth rate of 30-40% per year through 1985 for flexible disks, paced by the minidisk and a strong trend towards multiple density recording formats. Cartridges, led by their previously mentioned mini-Winchester backup role, will grow at a similar rate. Streamer technology and a trend towards longer tape lengths (and thus even more capacity) will be the major cartridge evolutions in this period.

Q: What are the basic steps involved in producing a diskette?

A: Diskettes are made by coating a 3 mil (75μM) film of PET (polyethylene terephthalate) on both sides with a layer of submicroscopic magnetic particles dispersed in a flexible polymer binder. The magnetic coatings are usually less than or equal to 100 micro-inches (2.5μM) thick and carry information arranged in concentric tracks at a density of 48-150 tracks per inch (19-59 tracks/cm). Along the tracks the storage density changes from track to track (greater on inside tracks, making data frequency the same for all tracks) so that the same frequency can be used as the head moves between the outer to the inner tracks. The highest bit density (on the innermost tracks) varies from 3,200 to 10,000 bits per inch (1,260–4,000 bits/cm). Most diskettes have an index hole through which light can pass to signal to the drive the beginning of the records and some use additional holes to mark the sectors into which the data on the diskette is divided. Others use pre-recorded patterns to achieve the same result. Diskettes are kept in a flexible plastic jacket which serves to protect them from damage or contamination and by its relative stiffness, to permit easy insertion into the drive.

Q: What major factors are involved in lowering diskette wear and producing diskettes with reduced data error rates?

A: There are two key steps in the diskette wear process: abrasive wear and the pulling out of large pieces of the coating. This suggests that the life of diskettes can be extended first by developing better lubricants to reduce abrasive wear, then by finding ways to improve both the adhesive and the cohesive strength of coatings. Flexible disk lubricants are usually blended with the binder, particles and solvent rather than applied to the surface of the finished disk as is usual with rigid disks. The binder must be tough and resilient but less hard than the epoxy binders used in rigid disk coatings. The polyurethanes are the most commonly used polymers in diskette coatings and it is important that the binder and magnetic particle be compatible; that there is the right degree of chemical and physical interaction between the binder and surface of the particle. The hardness and fracture mode of the magnetic particles also play an important part in the durability of the coating and in the wear of the head. It is possible to make improvements in the durability of the coating by adding abrasive particles (i.e. Al_2O_3) but the improvement in the life of the diskette is won at the expense of considerable reductions in the head life.

The jacket also plays an important part in reducing diskette wear and error rates. It protects the diskette from contamination to some extent and from damage while being loaded and unloaded. It keeps the diskette flat and in the proper position with respect to the head. The liner collects the abrasive wear debris and by doing so it reduces the danger of the debris building up on the head and causing failure of diskettes. A warped jacket can cause additional head-media separation (and thus, errors) and it can also result in increased torque and increased wear.

To minimize data errors, all steps of the manufacturing process from the treatment of the base film to the certification of the finished disks must be scrupulously clean and tightly controlled. Resolution and peak shift performance can be controlled by increased inspection and appropriate process changes during manufacture.

Q: What has Verbatim done to increase longevity, reduce wear, and lower data error rates on its diskettes? Have special efforts been made for dual-sided diskettes?

A: Dual-sided applications have proven to be much more demanding than single-sided applications, so special steps have been taken. These include improved coatings, improved test and certification equipment and procedures. Overall, we studied the effects of binder, dispersant, additives, magnetic particles, lubricants, processing conditions, and surface finishing conditions. The company has experimented with many types of lubricant and liner material to reduce media and head wear. There is an on-going program to further improve media to meet ever-increasing life and performance demands by users. D

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Memories Improve CMOS μP Designs

Rajeev Munjal, Michael Kastner, Keith Winter
National Semiconductor

High-performance CMOS μPs require new supporting LSI circuits. The NSC810 RAM-I/O-Timer, and the NSC830 ROM-I/O, were made in a high-density CMOS process, P2CMOS. Although these devices are most often used with NSC800 μPs, they may also be used with a variety of CPUs.

Several articles have been published on the new CMOS μPs. For efficient system design, users should understand the functions available on complex support devices as well. This article provides detailed descriptions and programming examples for the NSC810 and NSC830.

NSC800: low power CPU

The NSC800 is an 8-bit parallel μP. Built using the P2CMOS process, this CPU has the performance characteristics common to N-channel processors and the low power consumption (50 mW at 5V) typical of standard CMOS.

Architecture of the NSC800 is a combination of what is considered to be the best of two currently available processors — the Zilog Z80 and the Intel 8085. Internally, the NSC800 is very closely related to the Z80, with the same powerful instruction set and register complement. Externally, the NSC800 looks like an 8085, making use of a multiplexed address/data bus. This bus structure frees pins to be used for additional functions, such as advanced cycle status, multiple interrupts, clock generation and power save. Bus timing for the NSC800 is much the same as the 8085, but instruction execution times are the same as the Z80. The standard 2.5-MHz NSC800 has a minimum instruction execution time of 1.6 μs while the speed selected version, the 4.0-MHz NSC800A, provides a 1.0-μs minimum instruction time.

NSC810: dedicated RAM-I/O-Timer

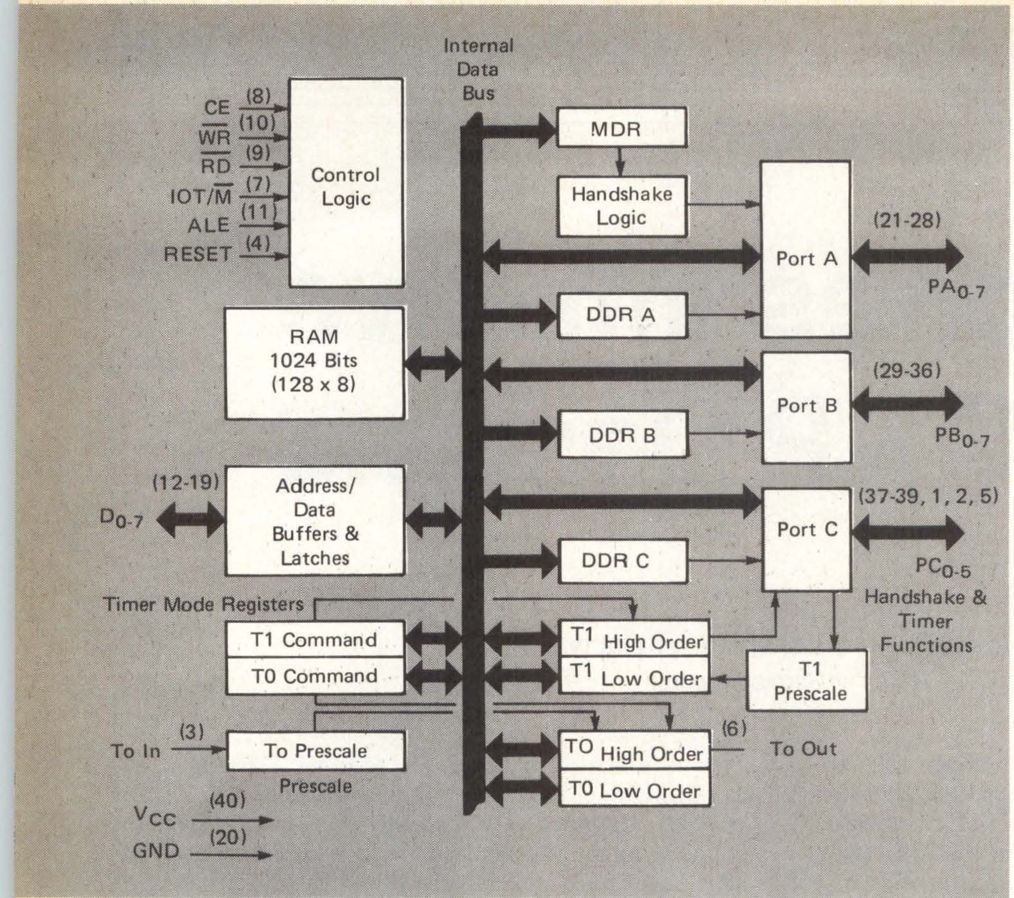
The NSC810 is a combination RAM-I/O-Timer peripheral device, consisting of 128 bytes of RAM, three I/O ports and two 16-bit timers. The NSC810 speed and power are compatible with the NSC800; maximum access time is 250 ns; power dissipation is 25 mW at 5V. In addition, the NSC810 is bus-compatible with the NSC800 — and is capable of operating directly from a multiplexed address/data bus. It has on-chip latches for separating address and data buses internally so no external components are required. Through use of the P2CMOS process, access time for the NSC810 (and NSC830) compares very favorably with that of existing peripheral components. Indeed, it is less than access times of many standard NMOS components. These performance characteristics are achieved without loss of any advantages common to CMOS, notably extremely low power consumption and high noise immunity. In a R/W memory organized as 128 8-bit bytes, access to the RAM occurs when the CPU adresses the chip with the I/O-T/M signal low. Since the RAM is speed compatible with the NSC800, no cycle extension is required to meet access time requirements, thus no degradation of throughput is incurred. In many small systems, only one NSC810 will meet the R/W memory needs of the application. However, additional NSC810s can be connected to increase the amount of RAM available.

I/O

Contained in the NSC810 are three I/O ports: two 8-bit ports and one 6-bit port. Port A (8-bits) has three modes of operation in addition to the standard mode common to all three ports. These additional modes of operation allow users to program port A into handshake operation, which requires active participation from the peripheral to effect data transfers.

In mode zero (basic I/O), data is read from or written to the port directly with no strobes occurring on the port's peripheral side. During a read operation, data is latched from the peripheral data bus at the leading (high to low) edge of the read (RD) strobe from the NSC800 and data is transferred to the CPU on the trailing (low to high) edge of RD. For data write operations, data output by the CPU during the write (WR) strobe becomes valid after the trailing (low to high) edge of WR.

Any bit in the port can be programmed to be either an input or an output through the use of the Data Direction Register (DDR). An illegal operation to a port (one that contradicts the information in the DDR) will not affect the port. That is, if a write operation is performed with a bit set as an input, no change will occur on the output.



The RAM section of the NSC810 contains 1024 bits of static

When port A is in mode 0 (and at all times with ports B and C), bit set and clear commands are available for use. In this manner, individual bits of the port can be set or cleared without needing to read, mask and write the data in the port.

Mode 0 for port A is set by writing a zero into the Mode Definition Register (MDR) of the NSC810. Also, a RESET from the the CPU will automatically set mode 0.

Dissipation is 25 mW at 5V. Included with the ROM are three ports, (two 8-bit ports and one 4-bit port.) Port A of the NSC830 has the same four modes of operation as Port A of the NSC810 and programming is identical. Ports B and C operate only in mode 0 and when Port A is in a strobed mode of operation, three bits of Port C are borrowed to act as strobe signals.

summary

The NSC810 and NSC830 are very versatile supporting LSI circuits. In addition to the RAM and ROM offered, designers can benefit from the many options available in the timer and I/O areas. The speed of these devices makes them useful in many μP based designs. D

Circle 31 on Reader Inquiry Card

Slave Processing Improves Performance

Lee Farrell
Intel Corp, Palo Alto, CA

Slave processing can greatly off-load the host processor in a system and allow it to perform other tasks. Slave processing also allows the system to be more modular and flexible, easier to design and debug, and allow easier to upgrade.

Peripheral controllers in μP systems are evolving into very sophisticated devices which are transforming μP systems into distributed processing systems. Semiconductor manufacturers are introducing components and bus architectures which greatly simplify the task of designing multiple processor systems, thus making them more practical for a broader base of applications.

Why distributed processing?

There are several reasons for considering the use of multiple processors. The most obvious is speed. The current generation of CPU's yield about a 10× performance increase over their predecessors. This improvement is still insufficient for many applications. One obvious solution is multiple processors.

Another reason for using multiple processors is the resulting modularity that is achieved. In any complex system, problems are more easily recognized and solved when the system is broken down into smaller modules. The complexity level is thus reduced and each module can now be easily understood and implemented.

In most applications, the system can be partitioned so that more than one microprocessor can be used. Each processor can then be considered a hardware module and its tasks can be precisely defined. This helps to reduce system complexity. It can also decrease the design cycle of a product. In the new design routine, functions of the system are defined and assigned to a particular module. Engineers assigned to each module can work in a parallel fashion. Partitioning also permits the use of different CPU types. A control oriented processor can thus be used for tasks which require large amounts of I/O and bit manipulation. A general purpose CPU could be used for more general data processing tasks. The result is a more optimum design.

Interprocessor communications

When more than one processor is used in a system, some form ofinterprocessor communication must be defined. Two basic classes of communications are used in multiprocessor systems: tightly coupled and loosely coupled. In a tightly coupled system processors communicate through some form of shared memory. This memory could reside on a bus common to all processors, or it could be a dual-port RAM with separate buses. In either case a tightly coupled system allows the transfer of high speed communication and large blocks of data at bus bandwidth. Choice of communication protocol is quite flexible. However, a parallel bus limits physical distances between processors.

Systems in which processors do not communicate through shared memory are classed as loosely coupled. An example of this class of communication are processors that communicate through a serial link. Transfer rates in loosely coupled systems are generally slower because either a serial link is used, or transfers occur a word at a time through some type of parallel port between the processors.

Multiprocessor classes

There are many classifications of multiprocessing. Parallel and pipeline processing are sometimes used in high performance mainframes. These complex operating systems break jobs down and assign portions to various processors. Another form of multiprocessing is co-processing. Co-processing uses one or more specialized processors which can be considered logical extensions of the host CPU. Actually, the processors receive their instructions from the host CPU's instruction stream as it is fetched from memory. Specialized math co-processors are not uncommon in large minis and mainframes.

I/O processing uses a specialized processor that specifically handles high speed I/O. Co-processing and I/O processing were once used only in large mainframes. More recently they have been finding their way into high perfomance microcomputer systems. The Intel 8087 math co-processor and 8089 I/O processor are devices which bring these multiprocessing concepts to the microcomputer world.

Multiprocessing can involve connecting two or more general purpose CPU's in a system, or it may involve the use of quite different special purpose processors, (I/O and co-processing.) Various manufacturers have introduced processors which are specifically designed to handle different types of jobs, and which lend themselves nicely to multiprocessing applications.

Bus considerations

An important consideration in any multiprocessing system is the hardware interface between processors. If the system has more than one bus master (device which controls and drives, the bus) then there must be some form of bus arbitration. This is usually handled by bus interface hardware which prevents two or more bus masters from trying to drive the system bus simultaneously. In single bus multiprocessing systems, only one processor at a time can be executing. A more practical solution would allow various processors to have access to their own local bus, (in addition to the system bus.) Each processor would then be able to execute its own code from its own local bus, and would use the system bus only for communication with other processors or other system resources. This type of system allows true simultaneous execution by different processors, but it requires bus arbitration which can be quite complex. Fortunately, LSI devices are available which handle this arbitration very nicely.

Slave processing

A slave processor receives commands from a host CPU, but cannot gain control of the system bus nor dispatch commands to other processors. It merely receives and executes commands.

The slave cannot modify system memory without direct intervention of the host CPU. So even if the slave's software is full of errors, it cannot inadvertently corrupt the system resources. Slave processing also allows simultaneous execution with the host, because the slave has its own local bus, and local resources, (ROM, RAM, I/O). Slave processing, however, can be slightly limited in data transfer rates and of necessity must involve some bus master in all of its transfers. This is usually no problem exept in those designs requiring the transfers of large blocks of data. From a hardware and software point of view, then, the slave appears to the host simply as a peripheral controller such as a USART or perhaps some type of specialized interface processor. It is an intellegent device with its own program to execute. As far as interface to the host is concerned, it simply appears as an I/O port to read data and status from and write commands and data to.

The software involved in slave processing is straightforward. The host CPU dispatches commands to the slaves and either polls or is interrupted by the slaves when the commands have been executed. True multiprocessing is achieved with all its inherent benefits.

The UPI-41A slave microcomputer

External logic is required for the interface port between master and slave. However, there is a product available designed to be used specifically for this type of multiple processor design and which has this master interface built-in. The Intel UPI-41A Slave Processor Family consists of two pin-compatible parts, the 8041A and 8741A. The 8041A has ROM program memory on-chip, while the 8741A has EPROM. The on-chip memory means that these products are "universal peripheral controllers" and can be programmed for a wide variety of control tasks. This type of product offers several advantages over a general purpose CPU used for slave processing. First, the instruction set is designed specifically for the control type of environments typically found in slave applications, that is, lots of bit-manipulation and I/O instructions not usually found in general purpose processors. Secondly and already mentioned, it contains on-chip the necessary interface port and associated logic for communication with the host. Thirdly, its internal architecture with on-chip 1K bytes of ROM (or EPROM), 64 bytes of RAM, 18 parallel input/output lines, and Timer/Counter can dramatically save on board space and overall system cost. In effect, the UPI has its own "local bus" on-chip.

The basic UPI-41A interface with the host consists of an eight-bit bidirectional parallel port and the four control signals AO, CS/, RD/, and WR/.

This port has an input register, output register, and a status register, all on chip. The input register holds the data and commands from the host. The status register has an Input Buffer Full (IBF) flag which is automatically set when the host writes to the slave. The 8041A/8741A, under software control, can check this IBF flag to determine if the host has performed an output operation. The UPI-41A can optionally be automatically interrupted when this flag is set, thus eliminating the need for software polling. Another status bit, the F1 command/status flag is also automatically set to reflect the state of the AO input signal whenever the host performs a write operation. This allows the UPI to distinguish between commands and data. Usually this AO input is connnected to the host processor's least significant address line so that commands are written to a different address than data. When the UPI, under software control, reads a command or data from the input buffer register, the IBF flag is automatically reset. Whenever the host intends to perform an output operation to the slave, it simply checks the IBF flag in the status register to determine if the UPI is ready to receive another byte. Thus the status register is used by both the slave and the host.

The output buffer register is used for transferring data from the slave to the host. The UPI, under software control, places data into the output buffer register, automatically seting the Output Buffer Full (OBF) flag in the status register. By polling the status register, the host can determine when the slave has data waiting to be read. When the host reads the data from the output buffer, this read operation resets the OBF flag automatically.

The UPI slave distinguishes between a status read and an output buffer read by the AO input signal, and this allows the host to read status at any time without disturbing any of the UPI's buffers or status.

The status register contains five additional bits which are user definable and give the designer additional flexibility. The UPI-41A also allows for the configuration of two of its general purpose output lines to be used as interrupt inputs to the host. These cause interrupts to be generated to the host whenever the UPI transfers data to its output buffer or reads data from its input buffer. In this way the host is not required to poll the UPI to determine if data is available or if new data should be written. Two additional I/O lines allow the UPI-41A to interface directly with DMA controllers, in addition to a CPU, for higher speed data transfers. These two I/O lines become DMA request and DMA acknowledge signals. This option, as well as the interrupt option are selected under UPI software control. This architecture simplifies a processor's interface to a peripheral device. One "side" of the UPI provides a mechanism for communication with the processor bus. On the other side, I/O lines are used to control the peripheral device. The on-chip program memory means that the UPI-41A is the logical choice for peripheral control where a specialized LSI controller does not exist, or where the control function is likely to change. D

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Multiprocessing With Single Board Computers

Les Soltesz,
Intel Corp., Hillsboro, OR

Multiprocessing is used in the following application areas:
1. *Resource sharing*. In these applications, multiple processors share a resource on the system. Examples include sharing peripherals, high speed math processors, etc.
2. *Increased throughput*. By dedicating processors to individual tasks, a great degree of parallelism can be accomplished. Each processor operates independently of the other(s) in controlling its task. Communication between processors takes place through a pre-established protocol which may include shared memory, interrupts, etc.
3. *Modularly-configured systems*. Many applications require flexibility in system configurations. In these cases multiprocessing represents a viable alternative, since performance increments (processors) can be easily added to the system for optimum performance.
4. *Redundant systems*. In applications such as space technology where a high degree of reliability is required, multiprocessing has been used for redundancy. If one processor fails, the system can continue by the redundant processor(s) taking over the processing functions.

board level architectura l considerations

One measure of processing capability is the independence that each processor has in a multiprocessing environment. An SBC concept, whereby each computer subsystem includes the major elements of a computer system (CPU, RAM, ROM, parallel I/O and serial I/O), has distinct advantages in multiprocessing configurations. A number of key resources are included on the SBC.

Therefore, as long as the CPU does not require global resources, it operates with the on-board resources leaving the system bus completely free for other activities which may necessitate the bus, such as DMA transfers. Consequently, adding multiple SBCs on the system bus simply increases the processing availability in the system and each computer board operates independently with its extensive on-board resources. Only when global resources or processor interaction is required will the processors access the system bus.

the iSBC 86/12A SBC

This product represents a large jump in performance and on-board memory capacity and includes architectural features which aid in implementation of multiprocessing.
1. *Triple bus architecture* is organized around a three-bus-hierarchy: the on-board bus, the dual port bus, and the Multibus system bus. Each can communicate only within itself and an adjacent bus, and each can operate independently. The main bus is the on-board bus, which connects the CPU to all on-board I/O devices, ROM/EPROM and the dual port RAM bus. Activity on this bus does not require control of the other buses, thus permitting independent execution of on-board activities. Activities at this level require no system bus overhead and operate at maximum board performance.
2. *Dual port memory* includes 32K bytes of dual port R/W RAM. The dual port allows other processors or DMA devices in the system to transfer data directly to the board's RAM for further processing by the 8086. This is a significant performance advantage since all data to be processed is on-board. The iSBC does not have to incur the additional overhead of accessing Multibus memory resources for processing data.
3. *Reserved RAM area for CPU*. In applications where it is desired to assign a specific area of RAM memory for exclusive use by the on-board CPU, the board provides the facilities for separating the RAM space which will be accessible from the Multibus system bus from the space dedicated to the CPU.
4. *Interrupts*. The board supports up to nine levels of vectored priority interrupts originating from any of 17 sources, nine on-board and eight through the interrupt lines of the Multibus system bus. These lines provide a convenient mechanism for inter-processor communication.

multimaster configurations

The system bus provides signals required to resolve bus contention between multiple processors or multiple masters, (where master is the terminology used for the device which is in control of the bus). There are two basic ways of interconnecting multiple SBCs.

1. *Serial priority*. In this configuration multiple masters share the system bus and priority is established on the basis of bus location. Each master on the bus notifies the next lower priority master (BPRO/) when it needs to use the bus for a data transfer, and it monitors the bus request status (BPRN/) of the next higher priority master. Thus, the masters pass bus requests along from one to the next in a daisy-chain fashion.

2. *Parallel priority*. Priority is resolved in a priority resolution circuit that determines which of several masters has the highest priority request (BREQ/) and generates the enabling signal (BPRN/) for the appropriate master.

The main difference in the two approaches lies in the amount of time available to resolve bus contention. In the serial priority approach, the lowest priority master must have its BPRN/ activated from the previous (higher priority) master; and this master in turn, must have its BPRN/ from the previous master, and so on. With a large number of masters, this daisy-chaining operation takes much time and limits throughput available on the system bus. The parallel priority approach provides a much more efficient method for resolving bus contention when many masters are used in the system. For these configurations, priority determination is accomplished in one clock cycle by the priority resolution circuit.

expanded multi-master capabilities

The board's bus arbiter chip resolves bus contention. In addition to supporting the serial and parallel priority schemes, it allows the board to increase bus throughput by not releasing control of the bus after each cycle. This reduces the need for bus priority resolution for each access; the board can continue to keep control of the bus until another master forces it off the system bus. This happens through a unique feature of the bus arbiter: the "Any Request" (ANYRQST) and "Common Bus Request" (CBRQ/) modes.

These signals (one a Multibus signal and one strapping option) allow the priority of the board to be established with respect to other bus masters. This offers the system designer the ability to "tune" an application system for highest throughput and minimal bus latencies.

bus lock functions

The board offers another alternative which allows it to obtain exclusive control of the system bus for critical system functions, such as high speed memory or I/O data transfers and critical read-modify-write operations. This is accomplished through the bus lock function, which keeps the bus busy while the board is in control. The bus lock can be activated by executing an 8086 lock prefix instruction (this insures that the bus will remain busy during the instruction prefixed by LOCK) and by connecting one of the parallel I/O output bits from the 8255 PPI to the bus lock function. This pin can be programmatically controlled and therefore, the bus lock function can be enabled and disabled by the user.

conclusion

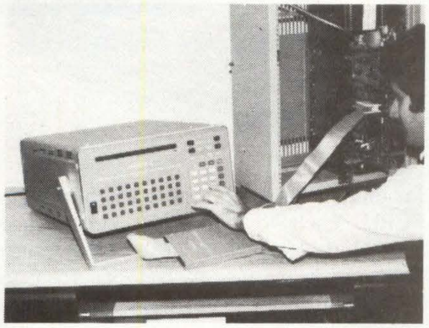
No matter which system you select, remember this: in implementing multiprocessing systems, be sure the architectural features permit efficient operation of each processor in the system as well as interprocessor communication. It helps if this architecture enables mixing the board with other 8-bit SBCs. This built-in capability gives you maximum flexibility in choosing the appropriate performance increment for his multiprocessing application. D

Product Index

To obtain detailed information on ads appearing in this issue use the Reader Inquiry Card. Circle appropriate numbers (as many as you desire), detach the card from binding and mail to *Digital Design*.

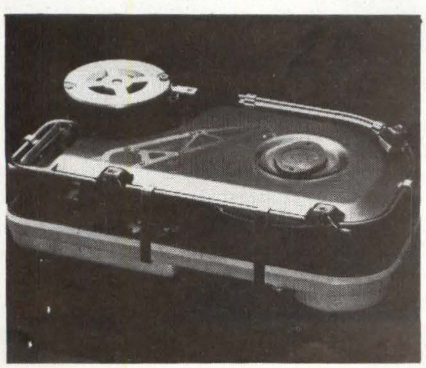
New Products

IN-CIRCUIT TESTER. This dynamic in-circuit digital tester performs tests on DUT (device under test) at speeds up to 10 MHz in real time environments. It is a turnkey system requiring no user programming, and can test most logic families (TTL, CMOS,



ECL, etc.), programmable and non-programmable devices, including memories and μPs. It has an error capture rate of one clock cycle on all pins of the DUT. This portable rugged unit has its own self-containea library covering a range of devices, and can be upgraded to cover new, as well as proprietary and military components. The THALAMUS-I is under $40k. Thalamus Electronics Inc, 1885 Sismet Dr, Unit #1, Mississauga, Ontario, Canada L4W 1W8. **Circle 140**

40MB WINCHESTER is an addition to the Q2000 family of 10-, 20-, and 30-MB disk drives which are fully compatible with the Shugart 5- and 10-MB SA1000 series. The 4 disk Q2040 features a typical heat dissipation rate of 70W, 42.66MB of unformatted capacity per drive, with a per-surface capacity of 5.33MB, 512 cylinders, and per-track capacity of 10.40 kB. Average access time is 65 ms with a 15 ms track-to-track access time and 100 ms max access time. The Q2040 incorporates 4,096 tracks, with 8 R/W heads, 4 disks and one index. Features of the Q2000 series include full SA1000 interface, mounting and power



supply capability; a proprietary moving coil rotary head actuator; a temperature compensation servo tract positioning system; and μP control of drive function. The Q2040 is $2100 (OEM qty. 500). Quantum Corp, 2150 Bering Dr, San Jose, CA 95131. **Circle 129**

64KB MEMORY BOARD for the LSI-11 is a general purpose memory card featuring 800 ns access time, 500 ns cycle time, 32,768 $\times$ 16 bit capacity and 18 address lines. It also offers switch selectable configurations and uses one dual height Q-Bus module slot. The MSVII is $1000/unit, $650/100, 30 to 90 days ARO. General Robotics Corp, 57 N. Main St, Hartford, WI 53027. **Circle 128**

5.25″ WINCHESTER DRIVES. The SA600 Series is available in the single-platter SA602 with 3.33MB of (unformatted) storage capacity, the double-platter SA604 with 6.66MB, and the 10MB triple-platter SA606. They are designed to complement the Minifloppy drives. Features include an average access time of 75 ms (160 max); transfer rate of 4.34 Mbits/sec; track-to-track access time of 18 ms (includ-

ing settling); and track density of 256 tracks/in. Two interface options are available. One interface design is pinout-compatible with the standard Minifloppy, which permits the Minifloppy and rigid drives to interface using the same control lines. The other interface design is pinout-compatible with existing 5.25″ Winchester drives. The SA600 Series will be available in 3rd quarter 1981; from $760 (OEM qty. 500). Shugart Assoc, 475 Oakmead Pkwy, Sunnyvale, CA 94086. **Circle 130**

100MB BACK-UP STORAGE, for Corvus Disk Drives used with DECs LSI-11 computer system, provides back-up data at a 1MB/min. rate using standard video cassette recorders with 120MB capacity cassettes. The Mirror is fully compatible with the standard U.S. NTSC video signal format. This insures that existing or future video storage may be used for data storage without modification. It contains CRC error detection. Every block of 532 bytes consists of a header containing file information, 512 blocks of data and 2 bytes of CRC information. The controller firmware resident in the Z80 controller provides an intelligent inter-

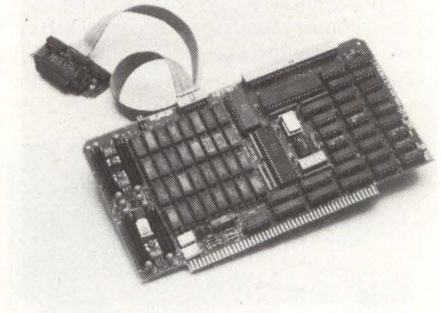
face to the host computer which specifies either Write, Verify or Read operations. Complete software is available for the LSI-11 to back-up an entire disk or a selected portion of the disk. Optional firmware allows automatic random access to the entire 100MB of tape. This can be used to eliminate the need for operator interaction or to create archival storage files of large amounts of data using custom applications software. ($1500). Corvus Systems, Inc, 2029 O'Toole Ave, San Jose, CA 95131. **Circle 133**

DESKTOP TELEPRINTER. This printer terminal features print speeds selectable from 10 to 30 cps, RS232C communications interface, and transmission rates from 110 to 300 baud. A matrix printer terminal, it accepts multi-copy sheet or roll paper 3″ to 14-7/8″ wide in from 1 to 4 parts. It offers a typewriter style keyboard, full ASCII character set, and keyboard settings for margins, tabs, horizontal and vertical pitch, and data transmission rates. The AJ 880 operates in either Bell 103 full duplex or full duplex with local echo mode. The DEC-compatible teleprinter leases for $70/12 months; purchase price is $1295. Also available are two new catalogs covering a range of medium and low speed acoustic data couplers and modems, including a matrix of operating specifications. Anderson Jacobson, Inc., 521 Charcot Ave, San Jose, CA 95131. **Circle 138**

MATRIX PRINTERS. The first in this series of serial matrix impact printers offers small business systems up to 150 cps print speed, and up to 136 column output. Up to 6 copies can be produced in either continuous roll or fan-fold paper. Adjustable form-feed tractors can handle paper widths from 1.5 to 16". The standard ASC11 96-character set is stored in the printer memory. An alternate character set may also be stored

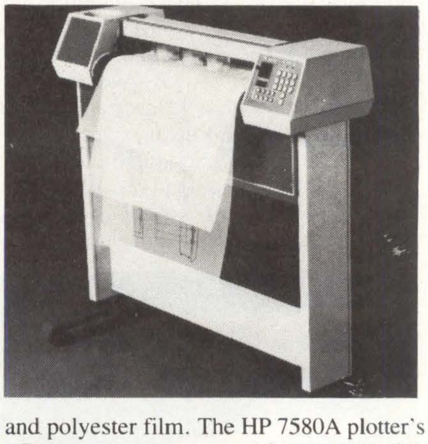
and selected on a line-by-line basis. Printing format can be selected for 10, 13.6, and 16.5 cpi, and either 6 or 8 lines/in. Subscripts or superscripts may be printed at any character position. Double-wide printing may be performed in any selected pitch. The Infoscribe 500 is $1,395; under $1,000 in OEM qty. Infoscribe, Inc., 2730 S. Harbor Blvd, Santa Ana, CA 92704. **Circle 135**

SINGLE BOARD COMPUTER provides multi-processing capability on the S-100 bus and is ideal for use with CP/NET. The unit performs as a Z-80 slave processor loosely coupled to an S-100 bus. Each board has 64K of RAM, a single level interrupt, a console serial port and a parallel port for



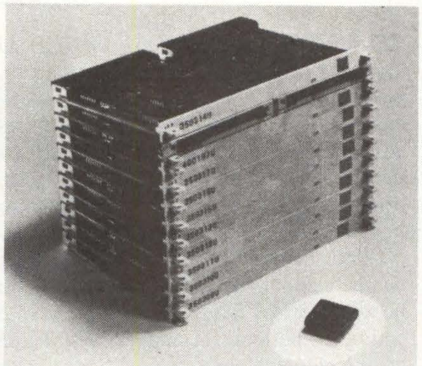
communication with the S-100 bus master CPU. Each NET/80 slave operates independently of any others, except for resource queuing in the master, and totally isolates the master CPU from errors in the slave processors. It permits the customization of each serial port for various applications. An expansion bus on each slave allows users to access additional peripherals. The system is compatible with most CP/M software. The NET/80 is $1395. MuSYS Corp, 1451 E. Irvine Blvd, Suite 11, Tustin, CA 92680. **Circle 127**

PEN PLOTTER. This large-format pen plotter, for producing electronic engineering drawings, is also compact and low cost. The plotter features μP control, fast plotting speed, and excellent repeatability, line quality and resolution. It can plot on pre-cut sheets and pre-printed forms up to "D" (A1) size, can be interfaced and controlled with a wide variety of large and small computers, and is capable of plotting on paper, vellum



and polyester film. The HP 7580A plotter's μP ensures constant speed for consistent ink flow. It can be programmed to automatically select from up to 8 colors or line widths. As each pen completes its plotting, it is automatically capped and stored. The HP 7580A is $15,450. Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304. **Circle 131**

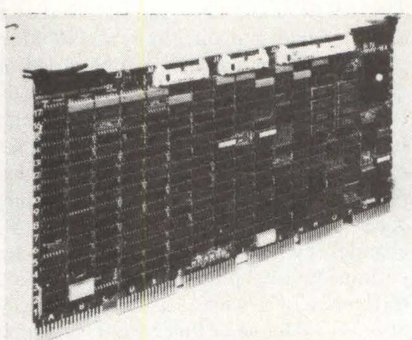
GATE ARRAYS. Production quantities of bipolar and CMOS gate arrays, as well as custom ECL gate arrays, are available. An advanced CAD system and a unique dual-level metalization process ensures maximum use of all available gates and buffers. The CAD system converts the logic diagram to digital form, simulates the circuit, verifies performance, and makes the metalization masks. Ten sample parts are then



produced for customer testing. It then takes about 12 weeks to get the first production parts, from 1,000 to 100,000 parts or more. Fujitsu Microelectronics, 2945 Oakmead Village Court, Santa Clara, CA 95051.
Circle 175

SOFTWARE. This software option for the DSD 480 double-sided floppy system permits file transfer between IBM and DEC computers. It runs under RT-11 or RSX-11M DEC operating systems, on either PDP-11 or LSI-11 computers. EXCHNG automatically converts EBCDIC to ASCII and ASCII to EBCDIC. Any IBM or DEC floppy disk format can be read, written, or copied from one to the other. The DSD 480 is $4495; the EXCHNG software option is $500. Qty. discounts available. Data Systems Design, Inc, 2241 Lundy Ave, San Jose, CA 95131. **Circle 142**

UNIBUS DISK CONTROLLER. This singleboard storage module disk controller for VAX-11/780 and PDP-11 Unibus series, features 32-bit data error control and header

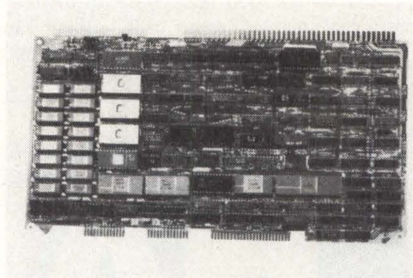


error control. It supports any 1 or 2 SMD interface compatible drives, including Winchester-types. The SMV15 has jumper-selectable DMA throttle rate, so users can choose transfer bursts from 1 to 15 words, or maintain constant transfer while monitoring for bus requests. Up to 64K words can be transferred with one R/W command. Multiple-sector block transfers can be made under hardware control. SMV15 runs with current revisions of VMS, RT-11, RXS-11M and RSTS/E operating systems. MiniComputer Technology, 2470 Embarcadero Way, Palo Alto, CA 94303. **Circle 156**

TERMINALS. The 4420 is a multipurpose buffered keyboard display. An async point-to-point terminal, the 4420 can handle data entry to on-line timesharing. Features include character or block transmission, speeds up to 9600 bps, 3 screen memory, buffered printer port, full editing and formatting capabilities, keyboard selectable options, cursor XY addressing and readout, programmable PF keys, destructive scrolling, and built-in diagnostics. ($3824). The 4543 is a display based interactive terminal featuring stand-alone operation. It operates up to 9600 bps over non-switched point-to-point or multi-point private line systems using a bit-oriented sync link protocol. Features of the 4543 Single Display include full editing and formatting capabilities, keyboard selectable options, a separately buffered printer port, cursor select, 5 optional keyboards, and built-in diagnostics. ($4731; delivery in 2nd quarter 1981). Teletype Corp, 5555 Touhy Ave, Skokie, IL 60077. **Circle 151**

New Products

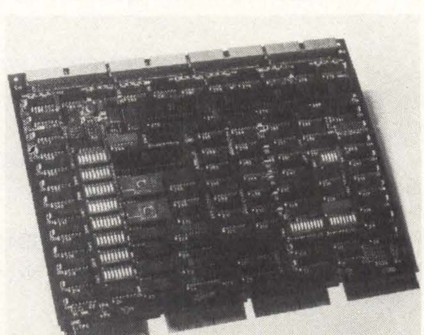
MULTIBUS COMPATIBLE μCs. This series provides a full range of single board computer capability. The MSC 8001 provides up to 8K static RAM and 16K EPROM/ROM. The MSC 8004, 8007 and 8009 extend capacity to 64K RAM and 32K



EPROM/ROM. All offer Z80 processing power with dual memory mapping, 8 prioritized interrupts, and serial RS-232 or TTL/20ma interface. Different models offer single voltage operation, optional APU, multimaster logic for up to 16 bus masters, socketed memory and CPU, and 24 or 48 parallel I/O lines. The industry standard CP/M operating system provides a complete hardware and software solution. For less complex applications, MSC 8301 uniform monitor firmware can be used for program debug and modification. A variety of support modules are also available. Monolithic Systems Corp, 14 Inverness Dr. E, Englewood, CO 80112. **Circle 227**

IC DESIGN. This technical publication, "201 Analog IC Designs," contains a variety of functional building block circuits which can be used, in combination, to create linear IC's of extreme complexity. It covers all major areas of linear circuit design. Useful to systems engineers who want to convert their discrete or MSI designs to space and cost effective linear semi-custom IC's, it is also a handy reference guide. Interdesign, Inc, 1255 Reamwood Ave, Sunnyvale, CA 94086. **Circle 149**

LSI-11 I/O INTERFACE offers full DEC DLV11-E compatibility on any of the 4 RS232 ports and uses one quad height QBUS module slot. It includes auto-answer modem support to Bell type 103, 113,



202C, 202D, and 212 modems. All ports may be individually selected to be synchronous serial I/O ports. Baud rates may be selected for each port individually from 50 to 19,200 baud. UART parameters may also be switch selected for each individual port. All ports have RS422 and RS423 compatibility for 3 wire interfaces. The QLV11 is $800; $520 in 100 qty. General Robotics Corp, 57 N. Main St, Hartford, WI 53027. **Circle 219**

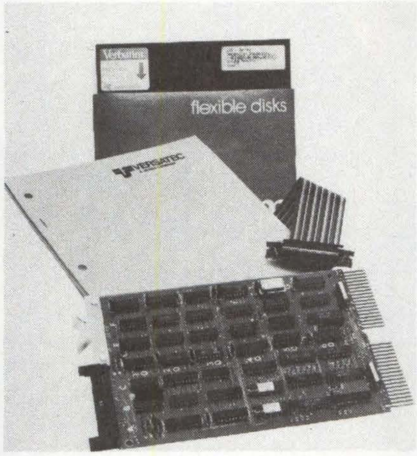
TELEPRINTERS. To the existing advantages of Telex — speed, direct access, written record of transaction, and cost efficiency, — this new series adds the latest advances of technology for domestic and international communications. The electronic printers cut message preparation time in half; all devices run at true, sustained off-line speed of 30 cps. These teleprinters can be customized as needed. The line can be adapted to TWX, DDD, private wire or computer perhipheral applications. Future technical developments will fit current models. Teleprinter Corp. of America, 550

Springfield Ave, Berkeley Heights, NJ 07922. **Circle 137**

IBM PRINTER INTERFACE. An IBM Series/1 computer can be interfaced to the IBM 1403 line printer to operate at 600 lpm. The system employs a Spur Products controller which performs all the control, logic and power functions of the 1403 printer (which has no electronics of its own), with one of MDB's line of printer controllers. The MDB controller (Series/1 model) is designed with a unique firmware PROM set programmed to operate the IBM peripheral device. The Spur controller provides the Universal Character Set (UCS) capability for the 1403 N1 and Model 3. The UCS capability allows the 1403 user to change print cartridges while still maintaining commonality of application programs. A 2 channel switch on the Spur controller permits the 1403 printer to be connected to 2 different CPUs, such as a Series/1 and IBM 360/370, at the same time. MDB will supply the MDB line printer controller at $1,995. The device is also provided by Spur Products in combination with the Spur controller for $20,000 and Spur sells the completely refurbished IBM 1403 N1 printer at $12,000. Installation and maintenance on the complete package is available from Spur. MDB Systems, Inc., 1995 N. Batavia, Orange, CA 92665; or

Spur Products Corp., 1904 Centinella Ave, Los Angeles, CA. **Circle 126**

SINGLE-BOARD INTERFACE allows LSI-11 systems to use any Versatec electrostatic plotter or printer/plotter, I/O multiplexer, hard copy controller, or vector-to-raster converter. Plugging into the computer



mainframe or I/O expansion chassis, the interface is electrically and mechanically compatible with PDP-11/03, -11/23 and LSI-11/2, -11/23 systems and with the DEC LP-11 line printer driver. The interface operates under DEC Direct Program Control (DPC) or DMA. It provides for printing speeds to 1000 lpm and plotting speeds to 34 sq. ft./min. The printer-plotter can be located to 54′ away from the LSI-11 computer. Model 125 interface package (circuit board, software, 4′ flat cable, 20′ extension cable, and manual) is $1600. OEM discounts available, 90 days ARO. Versatec, a Xerox Co, 2805 Bowers Ave, Santa Clara, CA 95051. **Circle 164**

ANSI-COMPATIBLE MP/BASIC, for microNOVA and NOVA 4 computers, includes extensions to the ANSI specification that make the language suitable for technical, scientific and educational fields. Enhancements to the ANSI standard include: string variables of any length, string concatenation, substrings, and letter-digit array names. Also included are 9 additional math functions, 8 string functions, fixed and variable length file manipulation, and integer data types. There is also a provision for an assembly language interface. MP/BASIC operates on microNOVA and NOVA 4 computers licensed to run under DG's MP/OS. It also operates on ECLIPSE computers licensed to run under the Advanced Operating System (AOS). Data General Corp, Rt. 9, Westboro, MA 01581. **Circle 152**

LOGIC ANALYZERS. The PI-616, for hardware debug applications, collects data in its 16-channel-by-1000 word data memory at rates up to 50MHz. Through keyboard commands, the user can configure the data memory for 8-channel operation at 100MHz; or split the memory for 8 channels

of data collection plus 8 channels of glitch storage. Glitches as narrow as 5 ns can be collected and highlighted on the CRT. It can also be configured with a waveform recording option which adds high-speed digital oscilloscope functions to the instrument. The companion PI-648 is oriented towards the analysis of software and hardware interactions. It can collect 48 channels of sync data in its 250-word memory. Its advanced state features include 3 separate clocks for demultiplexing, two 54-bit clock qualifiers, 16 levels of nested triggering, and data search and comparison functions. Both can be used with a Counter/Timer/Signature Analyzer option to provide system performance monitoring and debugging. Each can be used as a stand-alone device or combined for 64 channels. The PI-648 is $7400; the PI-616 is $8000. Paratronics, Inc, 2140 Bering Dr, San Jose, CA 95131. **Circle 172**

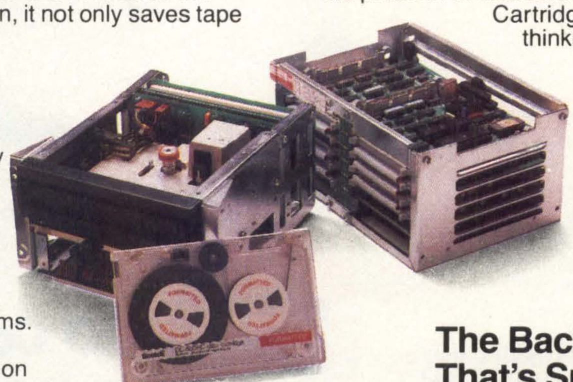
This is 3M's HCD-75 High Capacity Data Cartridge Drive. And the reason it's as intelligent as a computer is because it thinks like one.

You see, unlike other back-up systems, the HCD-75 is interfaced directly with the primary system by means of sophisticated, microprocessor electronics. When the host computer has data to feed, the HCD-75 starts automatically. When the host computer stops, it does too. And since the HCD-75 also positions to any location, it not only saves tape cost, but retrieval time as well.

Of course, the use of microprocessors allows the HCD-75 to perform a number of other time-saving functions, too. Like block replacement, so you can easily correct errors or change files which need updating. And fast random access, which makes it useful both as an I-O device or as a storage unit for low-usage files. All of which relieves the host computer from difficult timing and formatting problems.

What's more, the HCD-75 features state-of-the-art error detection and correction capabilities. Even when the system is off-line, self-test diagnostic routines monitor its performance. And, combined with each of its $32.50 high-capacity cartridges, the HCD-75 provides a full 67 megabytes of formatted user information (144 mbytes unformatted). So costly operator interventions are sharply reduced.

If you're looking for a reliable, cost-effective solution to the problem of disk back-up, the HCD-75 High Capacity Data Cartridge Drive is the system you should be thinking about.



Not only has a lot of thinking gone into it. But a lot of thinking comes out of it, too.

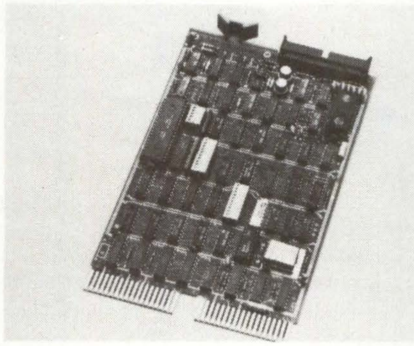
For more information, check the listing on the next page for the representative nearest you. Or write: Data Products Division/3M, Bldg. 223-5E/3M Center, St. Paul, MN 55144.

**The Back-up System
That's Suddenly Way Out Front.**

Circle 40 on Reader Inquiry Card

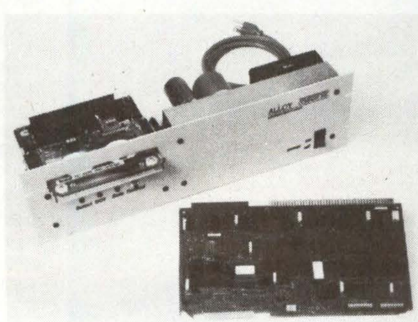
New Products

ASYNC SERIAL INTERFACE increases host/printer throughput in DEC LSI-11 systems and offers complete DEC DLV-11F compatibility. A Buffer Ready/Printer Busy monitor circuit in the EIA mode allows con-



nection to a variety of serial interface printers which present the transition of a buffer-full status line from a SPACE (+12VDC) to MARK (−12VDC) when the printer buffer is full and no further data should be sent. Four levels of priority interrupts allow the assignment of priority to high speed devices. The MLSI-DLV11-F offers a serial EIA-RS-232C/CCITT V.24 interface as well as a 20 MA current loop interface. Baud rates are programmable and switch selectable from 50 to 19.2K baud. MDB Systems Inc, 1995 N. Batavia St, Orange, CA 92665. **Circle 132**

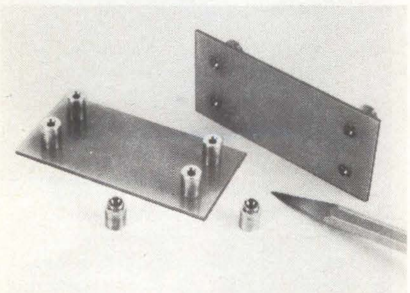
BUS SLAVE CONTROLLER is an 8085 based intelligent bus slave that allows up to 4 DEI Funnel (or equivalent) 13.4 MB drives to be interfaced to the MULTIBUS for Winchester disk backup and file storage purposes. Operating with any bus master(s), it provides a maximum 1.2 min/MB tape exchange rate. It provides up to 8 kB of onboard buffer memory. Running under CP/M and MP/M when operated with an 8080, 8085, or Z-80 bus master, software is supplied on an 8″ single sided, single density



floppy disk in CP/M format. Software is also available for ISIS based systems. The DMB-1 Controller is $550 each (25-49). Alloy Engineering Co, 85 Speen St, Framingham, MA 01701. **Circle 202**

New Products

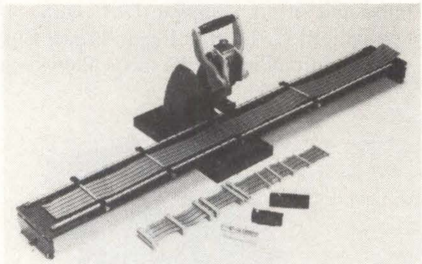
PC BOARD STANDOFFS offer extremely high resistance to pushout and torque-out. They are made of brass and electroplated with tin for use as permanently mounted mechanical fasteners, and also as solderable connectors in circuit board assemblies. They combine broaching and swaging to hold them tightly and securely in .050″ to .065″ thick non-ductile panel material. Any parallel-acting pneumatic, hydraulic or mechanical press can be used to install the new standoffs. The KFB3 standoffs are available in lengths of 1/8″, 3/16″ and 1/4″ with 4-40 thread size, and in lengths of 1/4″,



5/16″ and 3/8″ with a thread size of 6-32. Penn Engineering & Manufacturing Corp, Box 1000, Danboro, PA 18916. **Circle 192**

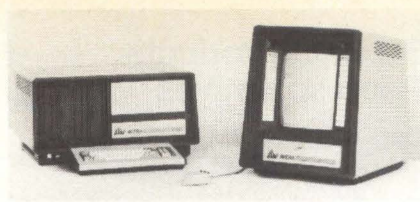
CARTRIDGE DISK DRIVE features a removable, front-load disk cartridge with a 17 million character storage capacity, plus a fixed disk cartridge of 17, 50, or 84 million characters, depending on version. Up to 8 drives can be interfaced in any combination to the Infotecs Control Center 2 microcomputer, giving a maximum total system capacity of 808 million characters. Infotecs, Inc., One Perimeter Rd, Manchester, NH 03103. **Circle 201**

ASSEMBLY FIXTURE allows rapid assembly of multi-connector flat cable harnesses. The Multiple Connector Harness Assembly Fixture, model 3305, can accomodate up to 36″ of flat cable at one time or longer lengths progressively. With movable rails and changeable connector positioning guides (purchased separately),



the fixture will handle connectors with from 10 to 64 contacts. It can be mounted to any Scotchflex assembly press, and can read scales in inches and millimeters to simplify location of connector positioning guides. 3M, Box 33600, St. Paul, MN 55133. **Circle 187**

IC DESIGNER SYSTEM. This stand-alone, desktop system allows customized, in-house IC mask design and schematic entry. The "Mouse," the system's primary graphics input, can be rolled along any flat surface to move the cursor on the screen, indicate drawing items for graphics input, and select various functions by positioning the cursor in one of 24 on-screen boxes. Features include on-screen menus, user-definable symbol recognition, split screen with full text response, user-written macro support and selective erase. The keyboard includes 14 user-programmable function keys for command execution. The IC Designer's grid structure has 64K resolvable points on each axis, handles designs up to 64 layers, with over 12 area shading and outline patterns for layer differentiation. Options are an 11″ × 11″ tablet input device, a



magnetic tape drive, a compact hard copy unit, and a 10 MB Winchester-type drive unit for extended storage capacity. Avera Corp, 340 El Pueblo Dr, Scotts Valley, CA 95066. **Circle 196**

80/132 COL. TERMINAL allows selection of an 80-column or 132-column display. It has a detachable keyboard which can be positioned up to 6′ away from the terminal. It also has an 18-key accounting style keypad. Other features of the DT80/3 include double-width, double-height characters; regional scrolling; bidirectional smooth scrolling; and insert line/delete line. The terminal emulates the Hazeltine 1420, Applied Digital Data Systems' Regent 25, the Lear Siegler ADM 3A, and Datamedia's 1521A terminals. Upon powerup the DT80/3 performs a software self-test. It interfaces

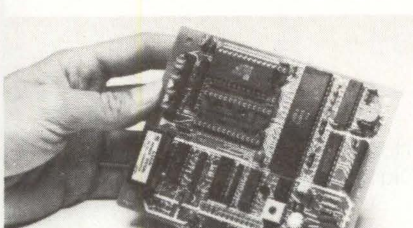
the host computer via standard EIA RS-232C/CITT v. 24 or optional 20 mA current loop interface. The DT80/3 is $1,395, OEM discounts available. Datamedia Corp, 7401 Central Hwy, Pennsauken, NJ 08110. **Circle 158**

VOICE/DATA MULTIPLEXERS. These System Tailored Voice/Data Multiplexers provide flexibility where voice, data or simultaneous voice and data transmission is required. They use only that bandwidth which is required to accommodate the voice and/or data traffic for which the multiplexer is configured. Features of the Models 6223/6224 include: 2 to 24 channels, field expandable; variable aggregate and channel rates; selection of various interfaces for aggregate and channel ports; and, derivation of sync digital data channels from a standard 1.544 MB/sec data stream (6224). Aydin Monitor Systems, 502 Office Center Dr, Ft. Washington, PA 19034. **Circle 153**

ALPHANUMERIC PRINTERS. The P2010 printer with RS 232C interface, and the P2020 with IEEE 488 interface, feature two color, 31 column printout with mixed characters, 7×7 dot matrix characters and integral paper feed. The P2010 will inter-

face with microcomputers, computer communications and other applications having Baud rates from 75 to 4800; and the P2020 will couple with instrumentation, computer peripherals and test equipment. Both include a printing rate of 2.4 lps, fast paper feed: 7.2 lps, 6 lpi, 31 char/line in black and red, 0 to 40°C operating range. Inputs are interpreted per the 64 member ASCII upper case character set. Canon Business Machines, 3191 Red Hill Ave, Costa Mesa, CA 92626. **Circle 178**

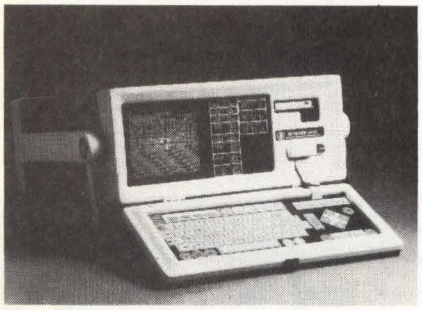
SPEECH SYNTHESIZER, for small computer and OEM applications, can accommodate both standard and custom vocabularies up to 256 utterances. The Series III Speech Module consists of TSI's speech synthesizer, vocabulary data memory, and on-board speech filter and an audio amplifier. Its TTL compatible I/O and +5V single supply simplify interfacing the module to a microcomputer. Memory can be any combination of one or two 16K, 32K or 64K ROMs or PROMs providing up to



128K bits. Vocabularies can be provided in English and most other languages. Telesensory Systems, 3408 Hillview Ave, Palo Alto, CA 94304. **Circle 183**

OEM CONTROLLER SYSTEMS combine PDP-11/03 performance with a compact packaging arrangement for controller applications. Four SB11 models are available. All include the LSI-11/2 (PDP-11/03) central processor, a multifunction memory board with 32 KB of RAM, two serial line ports, and a real-time clock; as well as a memory-resident version of the RT-11 operating system called MRRT-11 (for Memory-Resident RT-11). The SB11-AA includes room for "value added" by OEMs; the SB11-DA is preconfigured to support 10 serial lines; the SB11-EA, preconfigured to support 7 serial lines, one with modem control; and the SB11-FA, preconfigured to support the IEEE 488 instrumentation bus, plus 3 serial lines including one with modem control. All include license for the MRRT-11 operating system software. $2,440; $1,660 qty. 50. The TU58-VA, a dual-drive DECtape II casette subsystem, complements the SB11 as a mass storage option. ($1,500). Digital Equipment Corp, Maynard, MA 01754. **Circle 154**

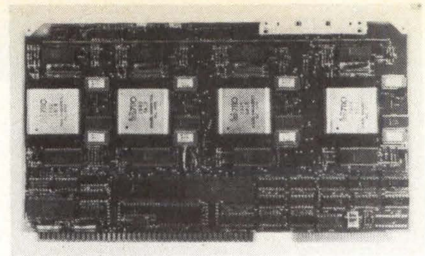
INTERACTIVE TEST SYSTEM, for data communications protocol diagnostics, has many features especially designed for packet protocols and SNA, as well as detailed



frame analysis of HDLC and SDLC. Bisync, async, plus ASCII, IPARS, EBCD, XS-3, SELECTRIC and EBCDIC are standard. The self documented tape contains all of the parameters used in the test plus data. The simultaneous trigger technique allows looking for a condition and taking direct action. Up to 8 independent triggers are simultaneously active. Major applications of the INTERVIEW 4500 include Emulation, Monitoring, built-in tape stored test plus 600,000 data characters, 1MB RAM capture memory (optional), and portable or rack-mount. The INTERVIEW 4500 is $14,500; conversion kit to change an existing INTERVIEW 3500 to a 4500 is $5000; 90 days ARO. Atlantic Research Corp, 5390 Cherokee Ave, Alexandria, VA 22314. **Circle 191**

DIGITAL PANEL METER. This 3-1/2 digit, single board DPM has an extra-large, .75" high Liquid Crystal Display (LCD). With energy-efficient LCD display, and low power CMOS circuitry, it uses only 17.5 mW of power. It is assembled on a compact unenclosed circuit board, and requires external, user-supplied +5V power. Electrical features include: balanced differential inputs; high impedance inputs with low bias currents; ratiometric reference which can cancel drift on bridge-type inputs; auto-zeroing; selectable Display hold; and blank circuit pads for attenuation or shunt resistors. The DM-LX3 is $57.50, OEM discounts available. Datel Intersil Inc, 11 Cabot Blvd, Mansfield, MA 02048. **Circle 186**

BUBBLE MEMORY BOARD combines up to 512 kB of storage capacity with an interface for Multibus systems. The board contains the IM 7220 bubble memory controller for operation in DMA, interrupt and polled modes, and features built-in power-fail protection and error correction. Up to 4 IM 7110 1M-bit bubble memory devices operating in parallel are on the board so capacity is available in 128K, 256K or 512K bytes. Other members of the LSI support



chip set provided on the iSBC 254 board include a formatter/sense amp., 3 packages for coil driving and a current pulse generator. Intel Corp, 1302 N. Mathilda Ave, Sunnyvale, CA 94086. **Circle 157**

CMOS SWITCHES feature ±25V protection beyond the power supply and data latches for interfacing with μP's. The AD7590DI and AD7591DI both feature 4 independent single-pole, single-throw (SPST) switches in a 16-pin DIP, differing only in that the switch control logic is inverted. The AD7592 comprises 2 independent single-pole, double-throw (SPDT) switches in a 14-pin DIP. Two grades of each model are available. KN grades are specified over the 0 to +70°C temperature range with plastic packages, while BD grades are specified over the −25°C to +85°C with ceramic packages. The digital inputs are TTL compatible, with no need for pullup resistors. KN versions are $7.40 (100); BD versions are $14 (100). Analog Devices Semiconductor, 804 Woburn St, Wilmington, MA 01887. **Circle 190**

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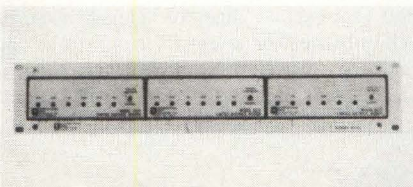
SOFTWARE PACKAGES. The SOS, Software Operating Systems, are fully documented, have been thoroughly tested and debugged, and are simple to load. They are written in BASIC for the TRS-80 Model 1 Level II, Apple II with Applesoft, and Ohio Scientific microcomputers. The packages are available on tape for the TRS-80 and tape or disk for Apple and OSI. Each tape or disk contains from 3 to 8 programs. They require at least 16K to 32K RAM in the tape format and from 32K to 48K RAM on disk. They can be altered to meet specific or unique requirements. The SOS simplify the design and analysis of commonly-encountered circuit design problems. The packages include: Plotting Graphs for Line Printer, Active Filter Design, Descriptive Statistics & Regression Analysis, Electronics I, II and III, and Plotting Graphs for Video Display. $24.95 on tape; $29.95 on disk. A book entitled "Circuit Design Programs for the TRS-80", by Howard M. Berlin, is also available. Howard W. Sams & Co., 4300 W. 62nd St, Box 7092, Indianapolis, IN 46206. **Circle 169**

RACK MOUNT ADAPTER is designed to allow up to 3 Model 6200, 6210, or 6110 desktop units to be rack mounted in a standard EIA cabinet. It consists of a window-frame type front panel 3½″ H by



19″ W. The modems are positioned on a shelf attached to the front panel by side brackets. The shelf has cut-outs for the modem's plastic feet that facilitate positioning and securing each unit. Filler panels are available for unused modem locations. Model 6330 is $125; filler panels are $12 each. International Data Sciences, Inc., 7 Wellington Rd, Lincoln, RI 02865. **Circle 139**

SERIES/1 ENHANCEMENTS provide improved communications and networking functions. The 4952 Model C is an entry level processor with an integrated diskette drive unit and up to 128K of main storage. The 4955 Model F doubles Series/1's main storage capacity to 512K; software support includes Realtime Programming System Version 5, Event Driven Executive Version 3 and Control Program Support. From $8500 to $11,550 for the 4952 and 4955. The 4975 Printer is offered in a range of models with both local and remote attachment. Speeds from 40 to 160 cps. From $2500 to $3650. A Local Communications Controller, for high speed serial data communication, allows up to 16 processors to be attached without a primary station. ($3825). Other enhancements are also available. IBM, Corp, Box C-1645, Atlanta, GA 30301. **Circle 160**

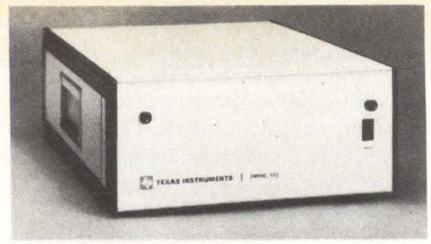
New Products

RASTERSCAN DISPLAY. This flicker-free, high resolution rasterscan CRT display is an extension to the I/O capability of the Sigmagraphics II CAD system. Different versions include graphic output in full color (over 4000 defined colors available) or with gray scale having over 250 levels of gray, plus standard B&W output. They feature image resolution greater than 1000 × 1000 pixels, screen sizes up to 25″ and introduce parallel processing to the system by providing for local generation of drawing details via an on-board μP dedicated to display management. DMA transfer rate is up to 1MB/sec and the vector drawing time is

typically 3 ms per pixel. Multiple high-speed memories are provided for storing display parameters. All models include an alphanumeric keyboard with 64 user definable special function keys and a non-destructive overlay cursor. Sigma Design West, Ltd, 7306 S. Alton Way, Englewood, CO 80112. **Circle 155**

Z80/8080/8085 CROSS ASSEMBLERS. Combined with a Millennium MicroSystem Emulator, the cross-assembler program transforms computers into complete development systems for these μP families. It can also be used with FASTPROBE guided probe software. The package includes a MACRO assembler generating relocatable object code, a linking loader, and a formatter/downloader. A users manual and FORTRAN source code on floppy disk or magnetic tape are provided. Minis supported by the Z80 Cross Assembler include PDP-11/LSI-11 with either RT-11 or RSX-11 OS, DG NOVA 1200 or ECLIPSE with either RDOS or AOS, HP 1000 or 3000 and TI 99/10. ($1500). Millennium Systems, Inc, 19050 Pruneridge Ave, Cupertino, CA 95014. **Circle 166**

μC MODULE ENCLOSURE. This self-contained enclosure features a 75W power supply, fan, front panel, and a 4-slot card cage which can accommodate any of TI's TM990 Family of 16-bit microcomputer, memory, I/O or peripheral interface modules. The number and type of modules can be any combination whose total power consumption does not exceed the power supply's 75W maximum. The power supply is a switching-type, and an ac-line filter is

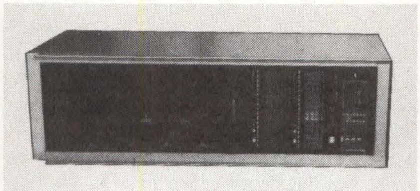


provided to minimize electromagnetic and radio-frequency interference. This compact enclosure measures 7″H × 17″W × 16.7″D. The TM990/522 is $1,620. Texas Instruments Inc, Box 225012, M/S 308, Dallas, TX 75265. **Circle 182**

P-E COMPAT. PRODUCTS. This "Resource Referral Catalog" lists hardware and software products, which operate on current Perkin-Elmer computer systems, that are available from independent companies. The products listed are sold or licensed, and independently supported by the companies which submitted them. Perkin-Elmer Corp, 106 Apple St., Tinton Falls, NJ 07757. **Circle 204**

BROCHURES ON KEYBOARDS AND switches. A full-color eight-page brochure describes "Golden Touch" capacitive keyboards. Diagrams are included that explain Digitran's patented, hinged, moving-plate capacitor technique. A second brochure lists the company's line of digital switches (thumbwheel or lever) for commercial and industrial uses. A third publication concentrates on two-button bi-directional switches that utilize fiber optics lighting. All or any of these brochures are available free. Digitran Co., 855 S. Arroyo Pkwy, Pasadena, CA 91105. **Circle 230**

TURNKEY SOLUTION to tech control offers a low price that makes network control a practical reality. The turnkey solution is a specially packaged version of Digilog's Network Supervisory System which is equipped with automatic monitoring and alarming, testing, and reconfiguration features for 8 communication lines plus a DLM III Data Line Monitor for diagnostic



testing of all components in the user network. The turnkey NS System addresses communications line supervision, EIA interface surveillance, automatic visual and audible alarm conditions, network reconfiguration through patching, communications line testing, and protocol monitoring and simulation. A Trap feature captures an 8 kB slice of questionable transmission stream for visual analysis. ($10,378). Digilog, Babylon Rd, Horsham, PA 19044. **Circle 159**

FAULT TOLERANT COMPUTER. The PSIFT BC, (PSoftware Implemented Fault Tolerance Basic Controller) provides correct, continuous operation, even in the event of hardware failures. Without any user intervention it automatically detects and corrects errors due to any fault before harmful action occurs. The BC series is the first of a full line of fault-tolerant control computers. They are designed specifically for use as embedded controllers or small-scale control systems. The user can select the degree of reliability and can choose from a variety of packaging, power and memory options. August Systems, 2757 19th St. SE, Salem, OR 97302. **Circle 177**

ELECTRONICS CATALOG. This 756-pg catalog features the products of leading electronic component manufacturers. The catalog is custom produced and all items listed are stocked. Descriptions, electrical and physical specifications and illustrations are provided for Semiconductors, Resistors, Transformers, Connectors, Sockets, Wire, Cable, Lamps, Lights and other related electronics products. It features a detailed product index and a separate index by manufacturer. Catalog No. 105 is free on request. Newark Electronics, 500 N. Pulaski Rd, Chicago, IL 60624. **Circle 188**

FIBEROPTICS, by John A. Kuecken, is a thorough guide that makes even difficult theories clear and easy-to-understand. This sourcebook goes from simple, but comprehensive, explanations of why and how fiberoptics were invented, through how they work and their applications to almost any electronic purpose. The various chapters cover the nature of light, the history of various light theories and discoveries, wave theory, polarization and wave interference, wave impedance, the methods for using refraction and reflection to the best advantage, lenses, actual hardware and the latest equipment, practical fiberoptic applications and a special low-cost transmitter and receiver project to build and experiment with. This handbook is a valuable combination of theory and practical know-how. $14.95 hardbound; $9.95 paperback. Tab Books, Blue Ridge Summit, PA 17214. **Inquire Direct**

8048 EMULATION PACKAGE. Now available is an emulation support package for the ECL-3211 universal development system for the 8048 chip family. Called the ESP-8048, this hardware/software package offers the user complete facilities for assembly language software development and real-time in-circuit emulation of any chip in the 8048 family – without using any interrupts, stack space, or memory space in the user's target. Included are the ASM-8048 macro-relocatable assembler, the CD-8048 chip driver module, the ECL.LINK general purpose linker, the OBJ.FORM object code format converter and the EP-8048 Pod, with cables. Software is supplied on an RX01 diskette. When supplied as part of an ECL-3211 development system, the ESP-8048 is included in the system price. Purchased separately as an add-on to an existing ECL-3211, the ESP-8048 package is $1500 (delivery 30 days, ARO). Emulogic Inc, 362 University Ave, Westwood, MA 02090. **Circle 207.**

HARD-COPY RECORDER produces crisp hard copies of B&W or 16 continuous-tone images directly from the video output of Lexidata graphics and imaging display

processors. It may be run in parallel with the monitor. No special hardware or software interfacing is needed. A built-in test pattern generator and a 4 channel multiplexor which allows the Model 4000 to be used with 4 separate display processors are both available. Table top or rack mount. $5445 for monochrome version; $8156 for grey-scale version, 90 days ARO. Lexidata Corp, 755 Middlesex Tpke, Billerica, MA 01865. **Circle 176**

Designers' Notebook

Firmware Level Interrupts for the 2900

Dr. Donnamaie E. White
Advanced Micro Devices, Inc.
Sunnyvale, CA

Interrupt handling at the firmware or software level is desirable when the interrupts are recognized under programmer control. These "software-interrupts" are used in emulations and basic CPU structures, while real-time or "hard interrrupts" are necessary in controller environments. Firmware level interrupts for a 2900 Family-based Computer Control Unit (CCU) or controller can be implemented with a 2914 Priority Interrupt Circuit (one can handle up to 8 levels of prioritized interrupts), a 2910 Microprogram Sequencer, registers, PROMs for implementing a memory map, a vector map and microprogram control memory.

The instruction register contains the current machine instruction, or macroinstruction. The memory-mapping PROM accepts the instruction register (IR) opcode portion on its address lines and produces an output microprogram address, which is the start address for the microroutine that implements the hardware steps to support the opcode.

The vector-mapping PROM accepts the 2914 priority-encoded vector output on its address input and generates a microprogram address on its output lines, which is the start address for the interrupt routine that will service the interrupt.

The 2914 accepts up to 8 interrupt requests encoded by an internal priority interrupt encoder. The interrupts can be individually masked, in which case they do not reach the encoder, and interrupts may also be nested under programmer control. A status fence prevents interrupts (of a priority less than that level currently in service) from causing an interrupt request. Both the status fence register and the mask register may be stored in the main memory of the system or may be loaded from the main memory of the system.

Fig 1 shows output enables for the three microprogram address sources: (1) the branch address/counter field in the microword of the microinstruction register (pipeline register for the control memory); (2) the vector map output and (3) the mapping PROM output are all driven from fields in the microword. This averages 20 ns faster than sourcing these signals from the 2910.

The microword for the structure shown in **Fig 1** is given in **Fig 2.** The microword format is shown in a structured layout, conceptually clear to a human reading the microprogram.

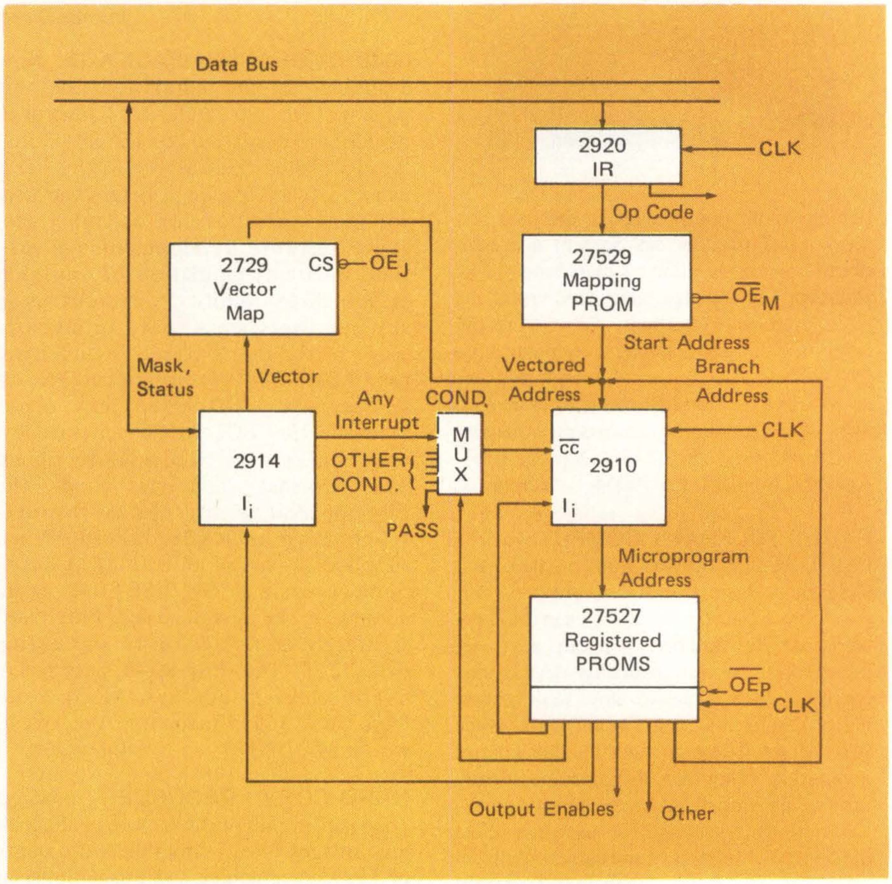


Figure 1: Firmware level interrupts for the 2900 series.

Sequence		Control	Interrupt		Output Enables			
2910 Inst.	Cond Mux.	BR Addr/ Counter	2914 INST-/EN	$\overline{2914}$ INT DIS	$\overline{OE}$ PL	$\overline{OE}$ Map	$\overline{OE}$ Vect	Other
4	3	12	5	1	1	1	1	• • •

Figure 2: The microword conceptual layout

From left to right the microword fields shown are: (1) 2910 Instruction Field — the 4 bits required for the basic sixteen instructions (there are more instructions). (2) Conditional MUX — the multiplexer used to select which test input will be examined; a 1-of-8 MUX is chosen here. Tests possible besides the 'ANY INTERRUPT TEST are PASS, ALU status (from a status register), etc. (3) Branch Address or 2910 Counter — the field used to specify an address or a value. (4) 2914 Instruction Field — the basic four instruction lines plus the I_{EN}line. (5) 2914 $\overline{\text{INT}}$ DIS — the interrupt disable; used to protect against interrupts during start-up in sensitive code areas, etc. (6) $\overline{OE}_{PL}$ — output enable for the branch address field. (7) $\overline{OE}_{MAP}$ — output enable for the memory mapping PROM. (8) $\overline{OE}_{VECT}$ — output enable for the vector mapping PROM.

For handling interrupts, several options are available in the hardware shown in **Fig 1** and the microword in **Fig 2.** Using a typical CPU microprogram structure as shown in **Fig 3,** the flow is characterized by the common microinstruction steps necessary for each execution; i.e., load PC to MAR; fetch next macroinstruction to Instruction Register and decode the opcode.

The PC is incremented as part of the PC → MAR step in its own step, or even as part of the fetch instruction step. Within this common code sequence, usually at the completion of the current microinstruction microroutine, a test can be made for the existence of an interrupt request.

Because the test is at a given location, such as the end of a microroutine or the beginnng of a common code section, there is no need to use a subroutine. All routines return to a fixed address.

The microinstruction sequence is shown in A.

At the interrupt routine address generated by the vector map, the interrupt is first cleared from the 2914 and acknowledged (if the interrupt is a level signal rather than a pulse). The end of the interrupt routine would have an unconditional jump to the common code section, labeled START in the code shown in B.

Unconditional jumps can be generated via a PASS on the multiplexer (CC/2910) is active LOW) or via the CCENpin of the 2910. This method uses the multiplexer solution. During the start of the routine it may be desirable to load or to save either the Mask Register, the Status Register or both.

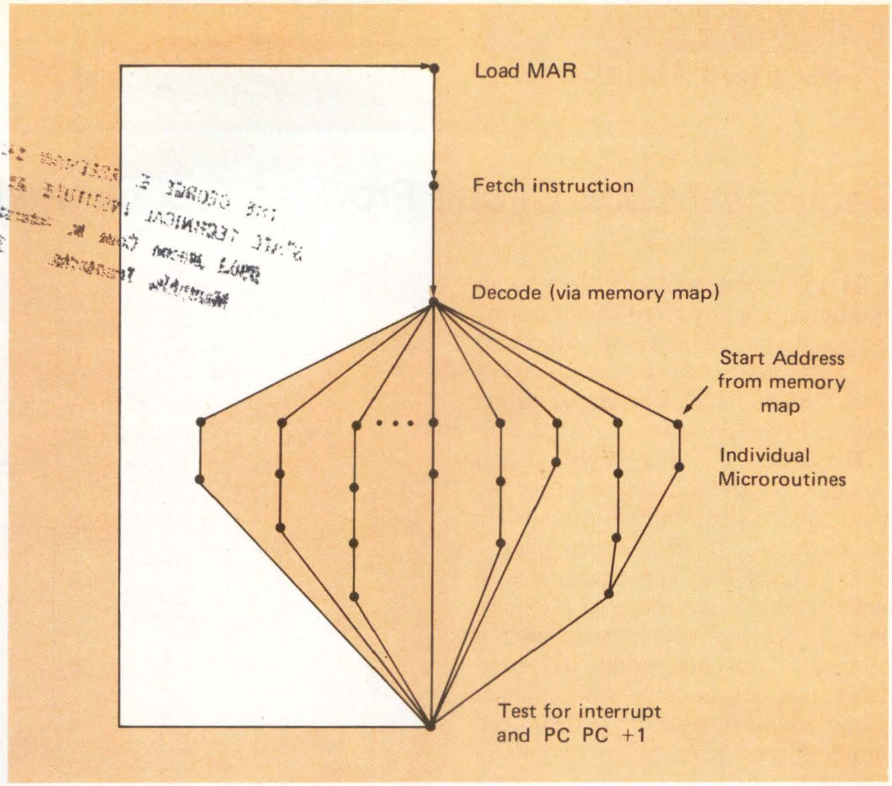


Figure 3: Sample CPU flow form.

At the end of the microroutine, it may be desirable to restore these registers. The status register must be lowered as it is automatically set when the 2914 READ VECTOR instruction is executed.

Second, if an individual microroutine is long, it may be desirable to test for an interrupt during some quiescent point within the microroutine. This is possible using the hardware and microword previously given. The test in this instance would be a conditional jump to subroutine where the subroutine start address is provided via the vector map. See C.

The subroutine, which would be similar in its initial and final steps to any other interrupt routine would return to the calling location via an unconditional return. See D.

Nested interrupts are permissable with either approach, provided that the interrupt routine itself tests for interrupts. The stack limit on the 2910 is five.

A

2910 INST	COND MUX	BR# ADDR COUNTER	2914 INST	$\overline{I}_{EN}$	2914 $\overline{\text{INT DIS}}$	$\overline{OE}_{PL}$	$\overline{OE}_{MAP}$	$\overline{OE}_{VECT}$
CJV OR CJP	ANY	#	READ VECTOR	EN	EN	DIS	DIS	EN

B

2910 INST	COND MUX	BR# ADDR COUNTER	2914 INST	$\overline{I}_{EN}$	2914 $\overline{\text{INT DIS}}$	$\overline{OE}_{PL}$	$\overline{OE}_{MAP}$	$\overline{OE}_{VECT}$
CJP	PASS	START	#	DIS	EN	EN	DIS	DIS

C

2910 INST	COND MUX	BR# ADDR COUNTER	2914 INST	$\overline{I}_{EN}$	2914 $\overline{\text{INT DIS}}$	$\overline{OE}_{PL}$	$\overline{OE}_{MAP}$	$\overline{OE}_{VECT}$
CJS	ANY	#	READ VECTOR	EN	EN	DIS	DIS	EN

D

2910 INST	COND MUX	BR# ADDR COUNTER	2914 INST	$\overline{I}_{EN}$	2914 $\overline{\text{INT DIS}}$	$\overline{OE}_{PL}$	$\overline{OE}_{MAP}$	$\overline{OE}_{VECT}$
CRTN	PASS	#	#	DIS	EN	EN	DIS	DIS

Figure 4: Microintruction routines for handling interrupts

Sequential Lock Circuit Provides Programmable Key Word Length

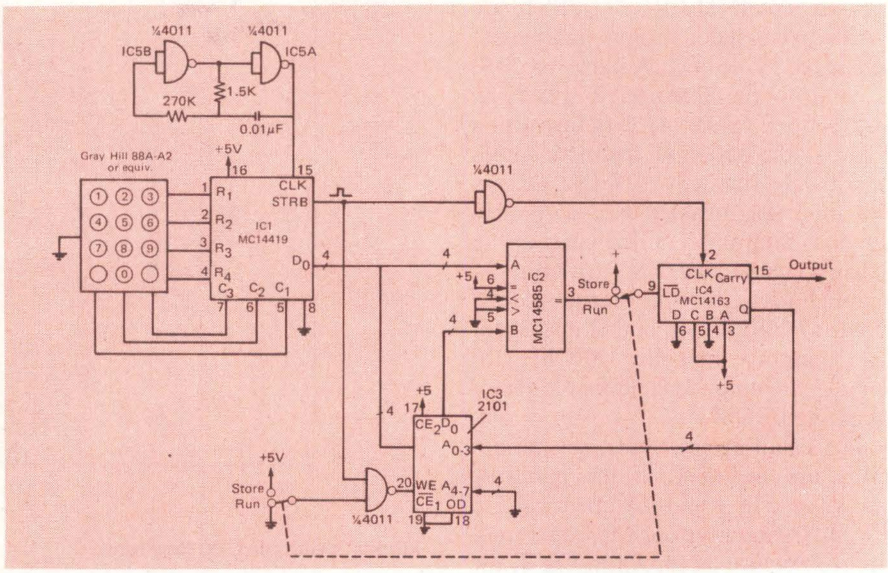
A flexible, sequential lock circuit with programmable key word length from 1 to 15 digits can be built with only 5 ICs. The right choice of the currently available MSI and LSI is essential to the success of this design.

The 2-out-of-7 code keyboard and encoder IC1 are normally used for the phone dial system. Pulsed by a 16KHz clock (IC5A, IC5B), it generates a BCD data at the output each time a numeric key is pressed, and also supplies a delayed strobe pulse after a contact debouncing period. IC2 compares the key-in data with number stored in memory IC3. If these two numbers are equal, the strobe pulse's trailing edge will increment address counter IC4 by one and address to the next key code in memory. The counter continues to count up for each matched input until 15 is reached at its output, and a carry signal is generated. Each time it meets an unmatched condition, the strobe pulse sets the counter back to the initial state by loading the binary number at the counter's ABCD input. So the key word length is equal to 15 minus the number at the counter's input (the figure shows 10).

To store a new code, place switch in store mode, enter the new code from the keyboard; the strobe pulse will write the number into the memory and increment the memory address at the same time. Since the trailing edge of the strobe pulse is used to clock the counter, a sufficient write recovery time is guaranteed by a relatively long propagation delay time of the counter.

IC3 is a 256 × 4 bit RAM, and we have used only a small part of this RAM. The remaining portion of RAM can be used for multiple users or multiple key code application. The memory IC, a 2101, can be replaced by a 5101 for low power battery operation or by an equivalent PROM.

L. Y. Hung, Consulting Engr., 300 Tremont St., Boston, MA 02116.

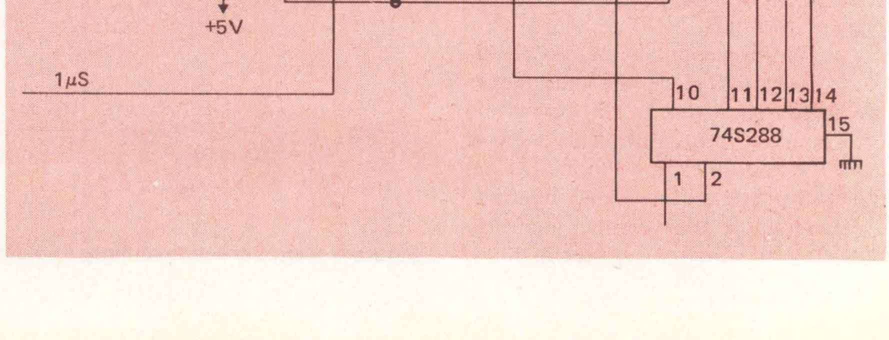


The strobe pulse generated by IC1 will increment the address counter if the key in code matches the code stored in the memory; otherwise, set counter output to $(ABCD)_2$. Key word length — 15 − $(ABCD)_2$.

Pulse Generator Uses 3 ICs

To generate a fixed pattern of pulses (i.e., for self-calibrating or self-testing), a simple way to do this with minimum hardware is shown. To generate a pulse-pattern, only three components are needed. Upon receipt of the Start Calibration command, FF1 will be reset, removing the clear condition from FF2 and CNT (FF2 and CNT form a 5-bit counter). The next pulses will advance the counter.

As for the contents of the PROM, any time a 1 is in the PROM, the pulse is HIGH and, reciprocally, a 0 gives a LOW. So, by writing the 1s and 0s into



Replacing the PROM with a RAM enables generating more patterns via μP control.

the PROM, it is possible to control the frequency and duty cycle of the resulting square wave.

Various patterns can be easily implemented. Whenever it is desired to stop the sequence, a 1 should be programmed into the second bit of the PROM. This bit will reset the counter (FF2 and CNT) and a new sequence will start only upon the receiving of a new start command.

It is obvious that simultaneous patterns are available from the same PROM, allowing a simultaneous check of different parts of the system. The PROM can be replaced by a RAM, thus allowing generation of many more patterns under the control of a μP.

Sorin Zarnescu, Teledyne Systems Co., 19601 Nordhoff St., Northridge, CA.

Reducing μP System Lockup

Random noise spikes, (or "hits") on μP system data, address, or control lines can have several adverse effects. One particularly troublesome effect occurs when hits cause erroneous op code fetches or changes in program counters, stack pointers, or memory bits. Such changes can cause discontinuities in program execution and the program will appear to make random jumps. Good software design improves chances that a system will survive such a jump. However, if the jump causes the program to execute an invalid instruction or data rather than a valid instruction, system lock-up may occur. For this case, recovery may only be possible through use of a hardware dead-man reset timer.

In some cases, the program may jump into unused RAM or ROM locations. Graceful recovery is somewhat easier for this situation. Unused memory need only be filled with no-op instructions, the last available memory locations containing instructions calling for a jump to an appropriate section of the program. But, for small systems, it is more likely that such a bit will cause a jump completely out of existing memory. In this case, the microprocessor will see only the high impedance of the tristated data bus during the fetch cycle, and lock-up will almost surely follow. Recovery from this type of hit can be implemented quite simply. The data bus need only be "programmed" to a no-op instruction via appropriate pull-up and pull-down resistors.

For the RCA 1802, op code for a no-op is C4. The appropriate bus programming network is shown. When this scheme is implemented and a hit is simulated by a long jump out of system memory, the μP repeatedly increments its program counter and executes no-op instructions until entire remaining memory space has been sequenced through and the first instruction in the program is once again encountered. At this point, further recovery functions can be implemented in software.

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