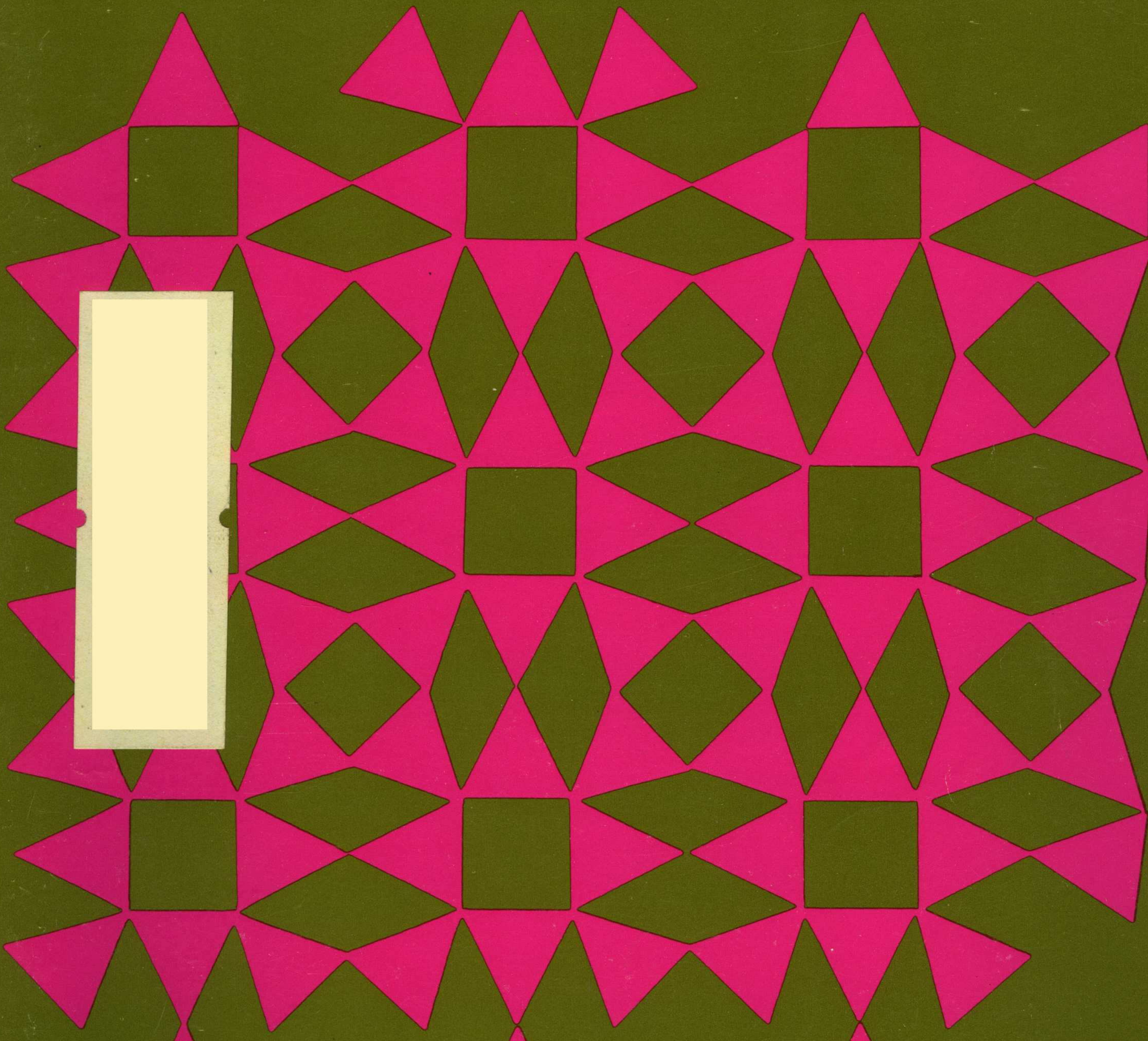
DATAMATION®

64

February



ROGRAMMED COMPUTERS MICROPROGRAMMED COMPUTERS MICROP

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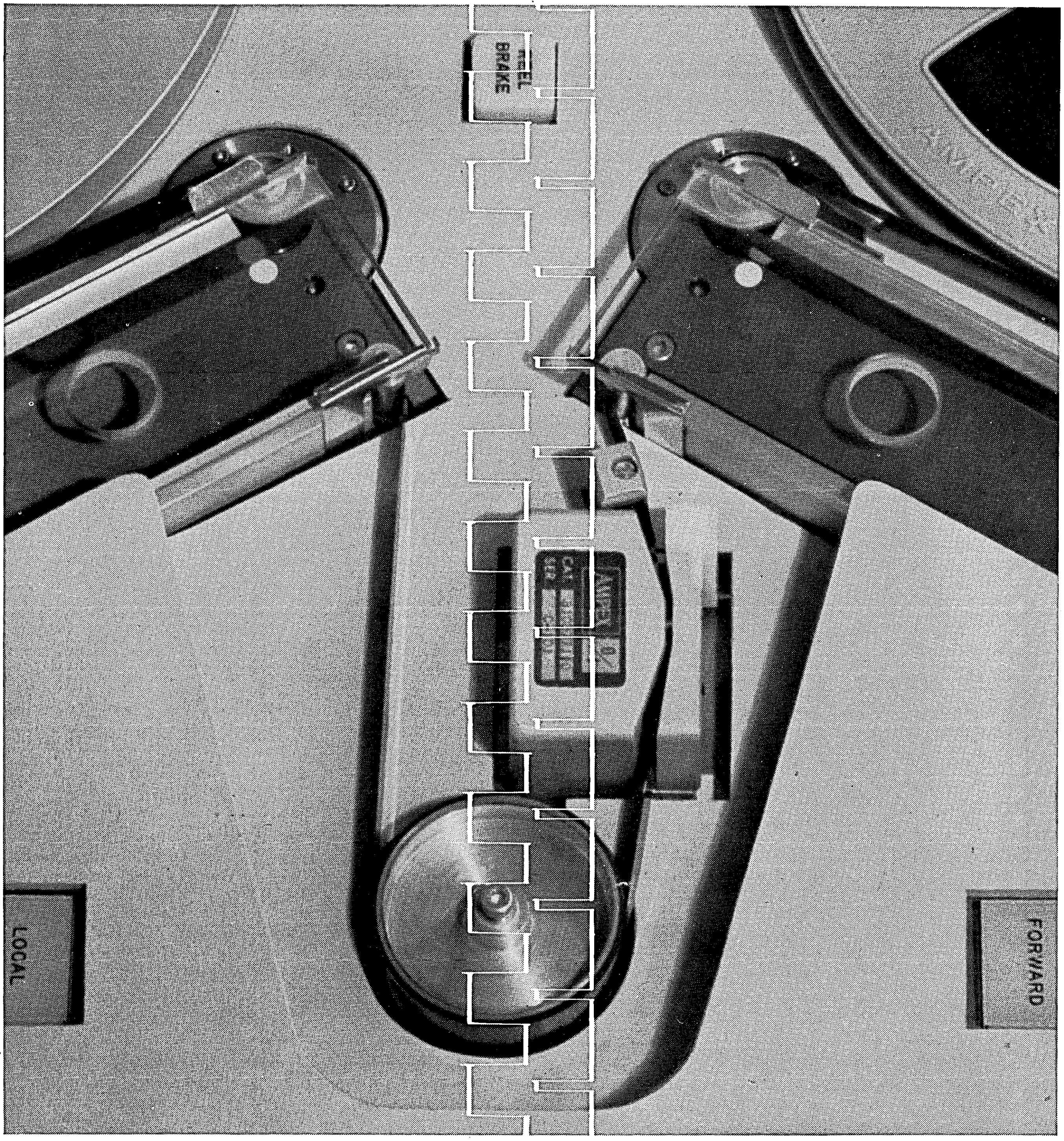


What has a drive concept so simple it's revolutionary? AMPEX TM-7

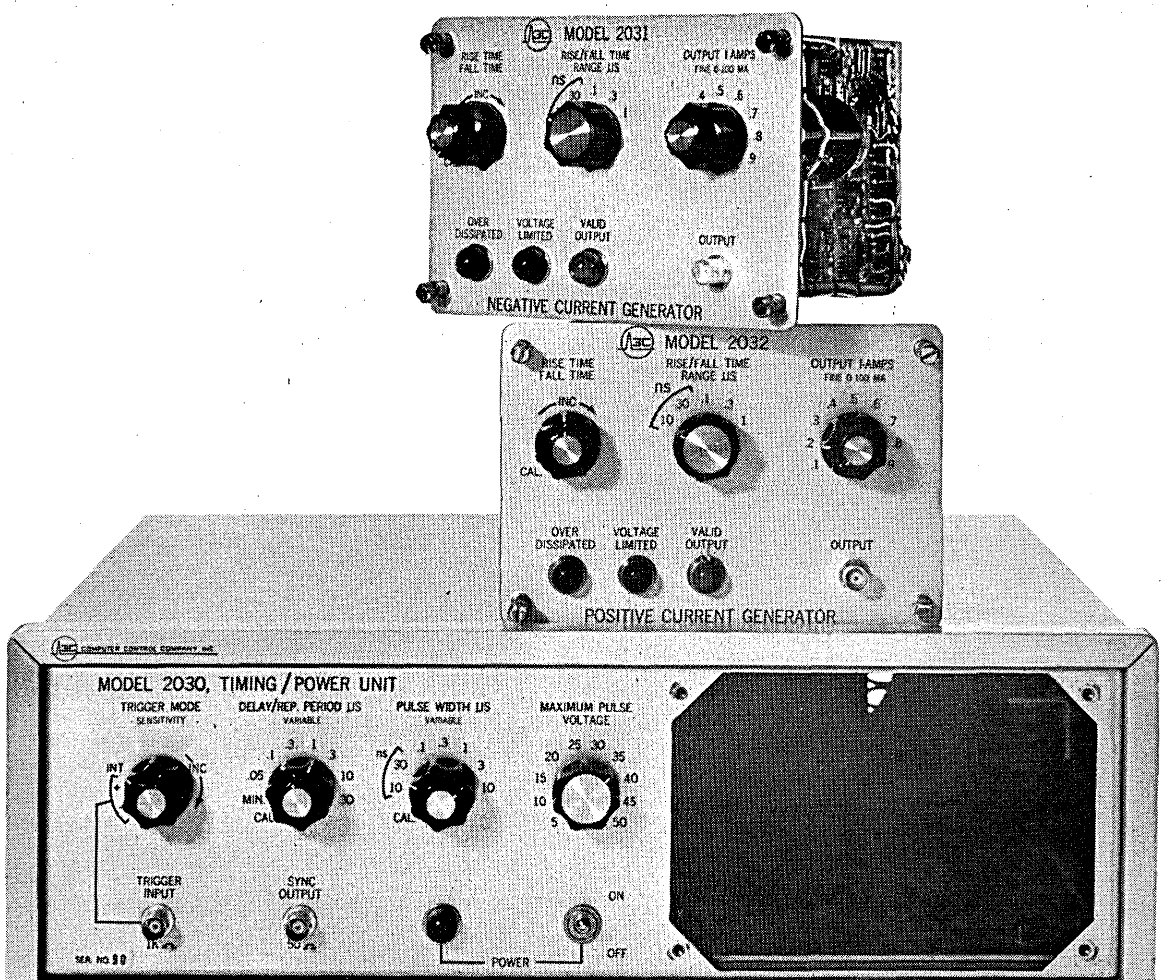
Here's a transport that's far in advance of anything in its class—the all new Ampex TM-7. It's a low-cost tape transport designed for less maintenance, less tape wear. And its most advanced feature is the revolutionary single capstan drive system. The new drive system has three major moving parts—a capstan and two reels. As a result, most of the components found in this type transport have been eliminated. Maintenance is far less. And tape wear? Virtually none. The two vacuum chambers keep a uniform tape tension on the capstan. There is nothing to smear the tape; nothing to stretch it. Tapes last and last. Even the old soft-binder tapes can be used with very little wear. The new Ampex TM-7

AMPEX

is completely compatible with IBM tape formats and with other Ampex equipment. It has a packing density of 200 and 556 bpi. A tape speed of 36 ips. A start and stop time of 10 ms with tape distance held within ±10%. Also, Ampex designed a new series of data and control electronics for the TM-7 to provide low-cost tape memory systems. The TM-7211 is a complete memory system enclosed in a 19 inch rack cabinet. And the TM-7212 is a complete shared system with four TM-7 transports in one cabinet. Write to the only company providing recorders, tape and core memory devices for every application: Ampex Corporation, Redwood City, California. Worldwide sales and service.

CIRCLE 1 ON READER CARD

NEW PULSE CURRENT GENERATORS



- **Rise and Fall Time: 10 nsec to 5µsec**
- **Output Current: 0.1 amp to 1 amp**
- **Output Impedance: 10K ohms min.**
- **Frequency: 20 megacycle max.**
- **Duty Cycle: up to 80%**
- **Back Voltage: ± 50 volts**
- **Solid State**

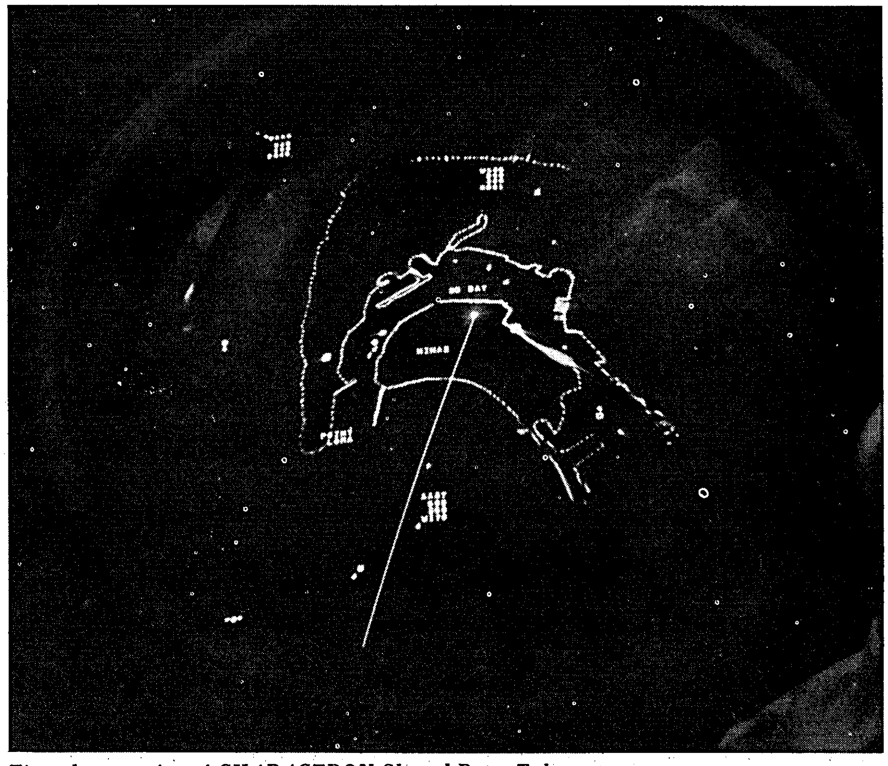
Demonstrations on request

COMPUTER CONTROL COMPANY, INC.
OLD CONNECTICUT PATH, FRAMINGHAM, MASS. • 2217 PURDUE AVE., LOS ANGELES 64, CALIF.

CIRCLE 4 ON READER CARD

New generation of Shaped-Beam Tubes makes

by: A. H. Wisdom,
Manager of Research and Engineering for Data Products



Time-share version of CHARACTRON Shaped-Beam Tube.

CHARACTRON® Shaped-Beam Tubes produced nearly 10 years ago, many of which are still being used in the display consoles of the SAGE program, have achieved 20,000 hours or more of reliable performance. Today's CHARACTRON Tube represents a new generation of development, offering dozens of major improvements over the original tube. The principle, however, remains essentially the same.

HOW IT WORKS

Heart of the CHARACTRON Shaped-Beam Tube is the stencil-like matrix, a thin disc with alphanumeric and symbolic characters etched through it. This matrix is placed within the neck of the tube, in front of an electron gun. The stream of electrons emitted from the gun is extruded through a selected character in the matrix. When the beam impinges on the phosphor-coated face of the tube, the character is reproduced.

The standard matrix carries 64 characters. However, matrices have been made with 88, 128, and 132 characters. Coupled with new variable character size capabilities, the CHARACTRON Tube offers a wide latitude in symbol generation. The beam is passed through one of the characters by applying the proper voltage to the selection plates. Electrostatic reference plates and/or magnetic deflection are then used to position the beam at any tube face location. In more compact tubes, the entire matrix is flooded with electrons generating a complete array of characters, while only the desired character is allowed to pass through a small masking aperture. A small diameter beam can be used to display data from analog inputs simultaneously with the characters.

NEW GENERATION OF TUBES

Today's CHARACTRON Tube is *not* the same tube built ten years ago. While all major improvements cannot be discussed, following are some of the more significant:

Earlier tubes had some deformation of the characters at the screen edge. The modern tube is sharp to the edge, with much greater resolution. New bright phosphors have been developed including a pastel green which eliminates spot size variation or "blooming". When necessary, tube length can now be dramatically decreased. A tube 25 in. long now achieves the same results once requiring a tube 45 in. long.

SPEED

Many optimistic goals have been claimed regarding the speed of character writing tubes. Frequently, however, these claims do not delineate the time required for the positioning of these generated characters but simply state the time necessary for generation. It is a simple matter to blink a character at tremendous speeds at the same place on the tube face. Generating different characters and positioning them in different places on the tube is something else. The shaped-beam principle generates characters in a period of time independent of the complexity of the character. Complex symbols can be generated as simply as a dot. With high speed circuitry, selection can be accomplished at rates equivalent to oscilloscope deflection frequencies.

For example, characters could easily be generated at a million each second. However, today's magnetic deflection yokes require a minimum 5 to 8 microseconds to settle the magnetic domain in the core and this is the limiting factor in positioning speeds. Using a high speed selection system and allowing five to ten micro-seconds for unblanking, CHARACTRON Tubes can provide realistic writing rates of 50,000 characters per second or more, even using random deflection. Electrostatic deflection tubes now under development promise writing speeds of up to 200,000 characters per second.

ECONOMICS

A CHARACTRON Tube by itself appears to be relatively expensive, but a system using this tube can economically justify itself easily. This is true because the CHARACTRON Tube replaces both the necessary character generator and much of the circuitry required by other systems.

In recent models, alignment procedures have been simplified, and the tube holds alignment longer than other character writing systems. A CHARACTRON Tube can be set up by an experienced man in less than one hour. Tubes are available in a wide range of phosphors with practically any desired color or degree of persistence. Resolution of 1800 TV lines can

advanced techniques possible in data display

be provided, the only limitation being the grain size of the phosphor. CHARACTRON Tubes are no more fragile than any other cathode ray tube. They have been exposed to a 32G shock for 52 milliseconds without harm, and can take just about any shock that does not fracture the glass. In one application, the tube was used in a portable battlefield display console.

PICTURE WINDOW TUBE

Frequently, it is necessary to continuously repeat certain data on the face of a tube while changing other data.

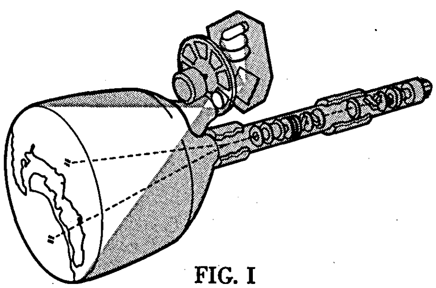


FIG. I

This may be done easily with a new development called the "picture window" concept. In the "window" tube, changing data from computer, radar, or communications link, is presented in the usual manner. Repetitious data are projected through the "window" onto the faceplate using a slide or film projector (Figure I). In a typical application, a geographic map of the area is projected on the face while the computer presents changing data. As the area under surveillance changes, the operator pushes a button to select another map. In another application, business or engineering forms are projected on the tube and filled in with data from the computer. Included in this option is a recording camera. By means of a beam splitting half-silvered mirror, the camera maintains optical access to the entire tube face. A button actuated solenoid operates the camera, recording all data being displayed.

TIME-SHARE TUBE

A new "time-share" version of the tube produces alphanumeric data and at the same time performs beam writing to draw curves and vectors. In the drawing mode, electrons pass through a special large aperture so that none of the beam is blocked. Brighter beam drawings result. The name "time-share" is derived from the fact that both the alphanumeric and drawing mode share the beam from one cathode for part of the time. This tube is ideal for applications such as long range radar where the antenna may turn at a relatively low speed of six times a minute.

TWO-GUN TUBE

On short range radar requiring high rotation speeds of perhaps 25 times a minute and many hits on small targets to build up an image, there may not be enough time left for forming alphanumeric symbols. With these applications, a two-gun tube (Figure II) is suggested. This tube retains the beam shaping electron gun for producing characters and employs another gun to accomplish the video writing. This second gun, when coupled with video driving circuitry, can be used to generate high resolution TV images including scan converter readout or

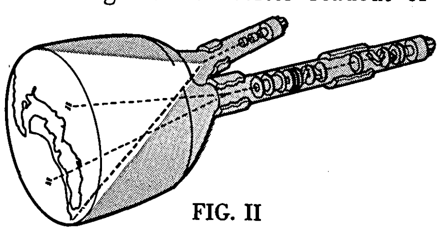


FIG. II

raw radar data. These images, of course, can occur at the same time as and without any effect on the alphanumeric data supplied from the shaped-beam gun.

SYSTEMS

General Dynamics|Electronics designs and produces a number of custom and standard display, printing and film recording systems which utilize the CHARACTRON Shaped-Beam Tube.

Custom installations include direct-view consoles as well as film recorders which automatically process and project large-screen displays for group viewing.

The S-C 1090 Display console (Figure III) presents alphanumeric, symbolic and graphic data from computers

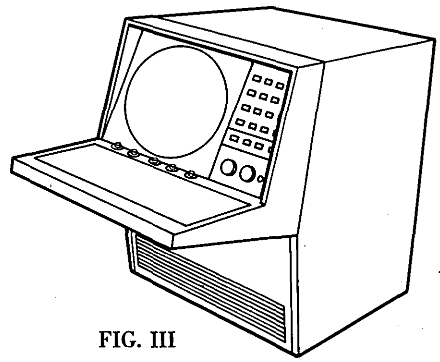


FIG. III

or other sources. It is a complete, "off-the-shelf" display unit. Optional equipment includes internal test routine, input register, level converters, internal storage of complete display frame, vector generator, expansion and off-centering, category selection and various data channel buffers. The console is 66 in. long, 32½ in. wide, and 47 in. high. It is recommended for a variety of applications, including command and control systems, air traffic control, computer readout and data display for any automated process.

The S-C 4020 records the output of large scale computers on film and/or paper at equivalent speeds. Combinations of drawings and alphanumeric data may be recorded in fractions of a second.

The S-C 3070 provides high-speed asynchronous printing without impact on paper for communications or computer output applications.

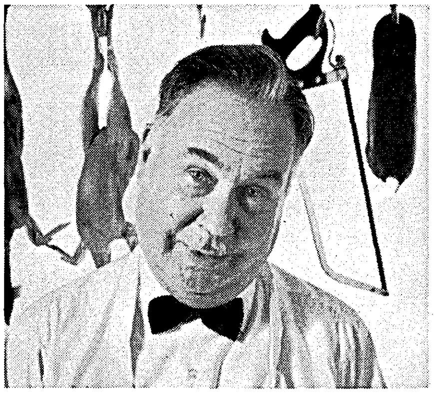
WRITE FOR MORE INFORMATION

For technical information on the S-C 1090 Display, the S-C 4020 Computer Recorder, the S-C 3070 Electronic Printers, or the new generation of CHARACTRON Shaped-Beam Tubes, write to General Dynamics|Electronics, Department E-10, P. O. Box 127, San Diego 12, California.

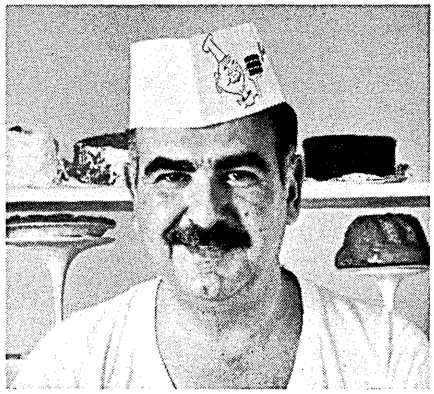
GENERAL DYNAMICS | ELECTRONICS GD SAN DIEGO

See GD|E Booth at Society for Information Display Exhibit, Feb. 26-27, San Diego, Calif.

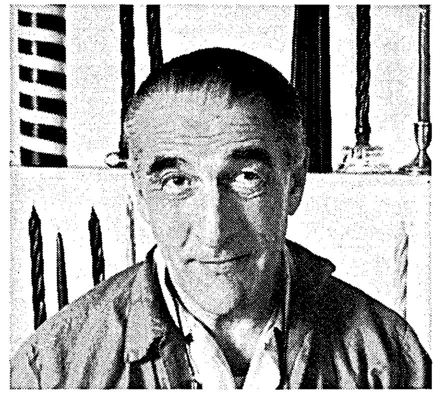
CIRCLE 5 ON READER CARD



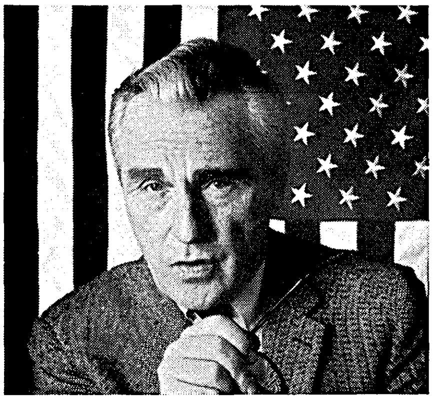
Butcher



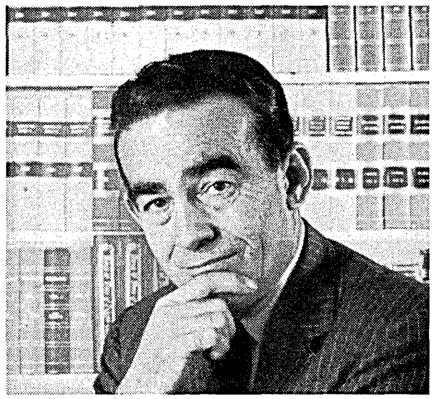
Baker



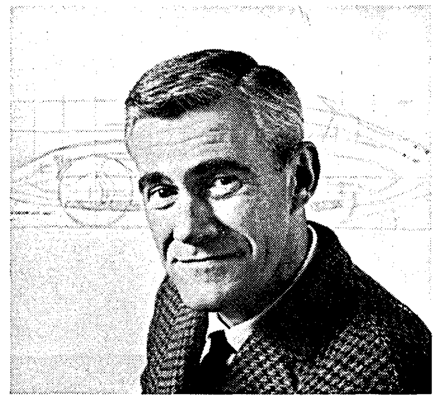
Candlestick Maker



Educator



Lawyer



Auto Maker

You don't have to be big to benefit from the UNIVAC Data Processing Center network.

You just need the ambition and the address.

Once data processing was the special province of giants. The U.S. Census Bureau. Major universities. Big business. Today electronic data processing is a necessary fact of life for a business of *any* size.

That's why UNIVAC has built a network of Data Processing Centers serving 29 major cities in the U.S. and parts of Canada. With over 15 million dollars worth of equipment. Including UNIVAC® III and UNIVAC 1107, the world's only thin film commercial computer. Designed to service every business and scientific problem.

We have staffed the UNIVAC network with over 750 highly trained people: scientists, mathematicians, engineers, consultants, programmers, systems analysts. Anyone any job would require.

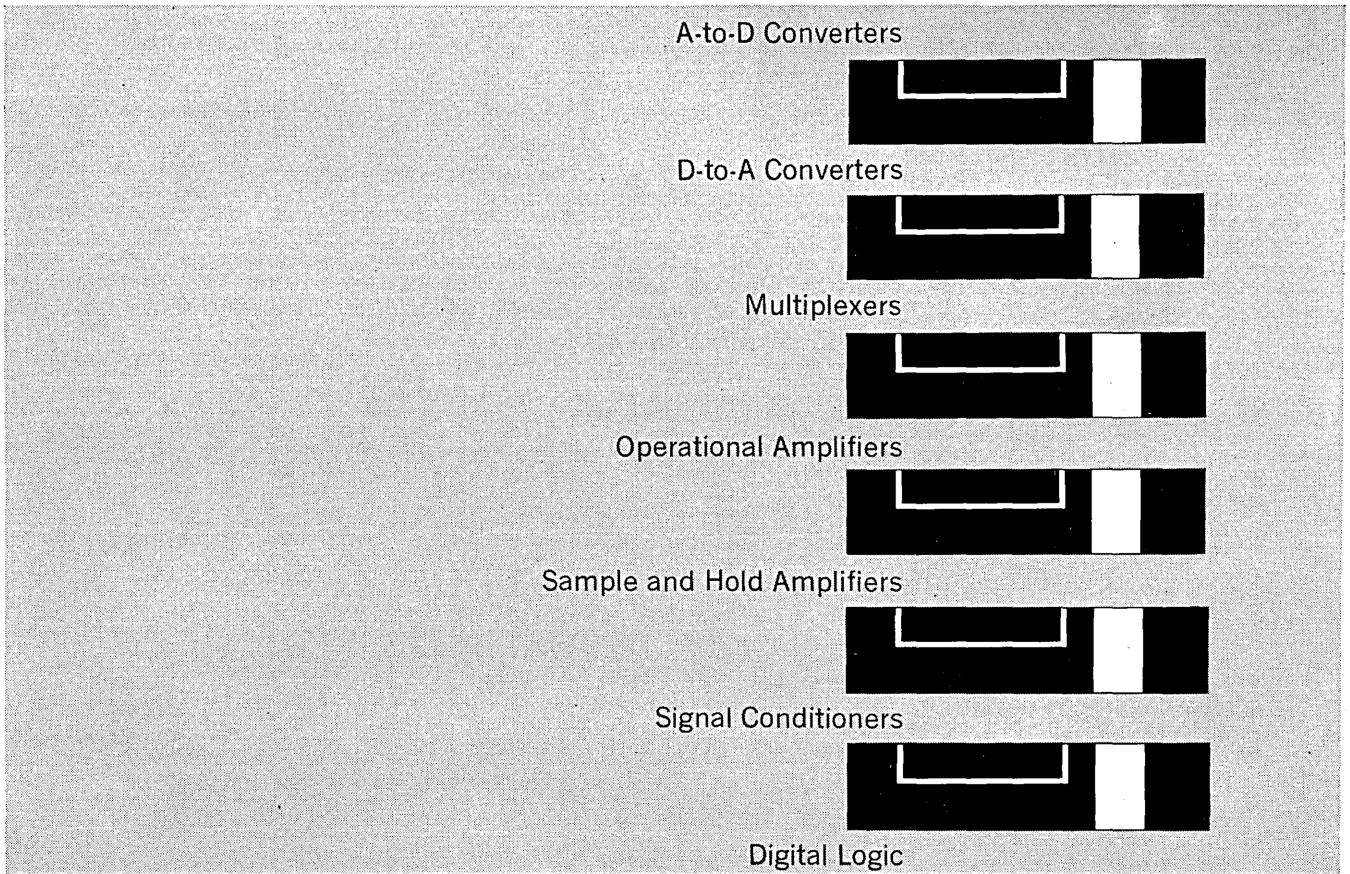
We're ready. As ready as anyone can get for big jobs, small jobs, workaday jobs, one-shot jobs. Any job.

Now what did you say your job is?

UNIVAC DATA PROCESSING CENTERS

UNIVAC DIVISION OF SPERRY RAND CORPORATION

CIRCLE 6 ON READER CARD



Look to the leader in the analog/digital world

Doing business with Adage gives you such a comfortable feeling. For so many reasons. For one thing, nobody is more experienced in solid-state analog/digital circuitry.

Nobody is so finicky about meeting specs (even specs that others wouldn't dare publish).

Nobody makes analog/digital hardware more reliable.

Or as handsome.

Or as mechanically perfect.

Or as well documented.

Nobody beats Adage, either, when it comes to efficient use of rack space. For example, a 60-channel data acquisition system with a 16-bit BCD Voldicon converter and VMX Multiplexer is housed completely in a 5¼″ box.

So whether you need a component or a custom-designed system, get a quote from Adage. The price will please you. And remember — from HZA input buffer amplifiers to output digital amplifiers — only Adage manufactures all the hardware necessary for analog/digital systems — all of it solid-state.

Adage INC

292 Main Street, Cambridge 42, Mass. ■ Offices in Los Angeles, St. Louis, Washington and New York.

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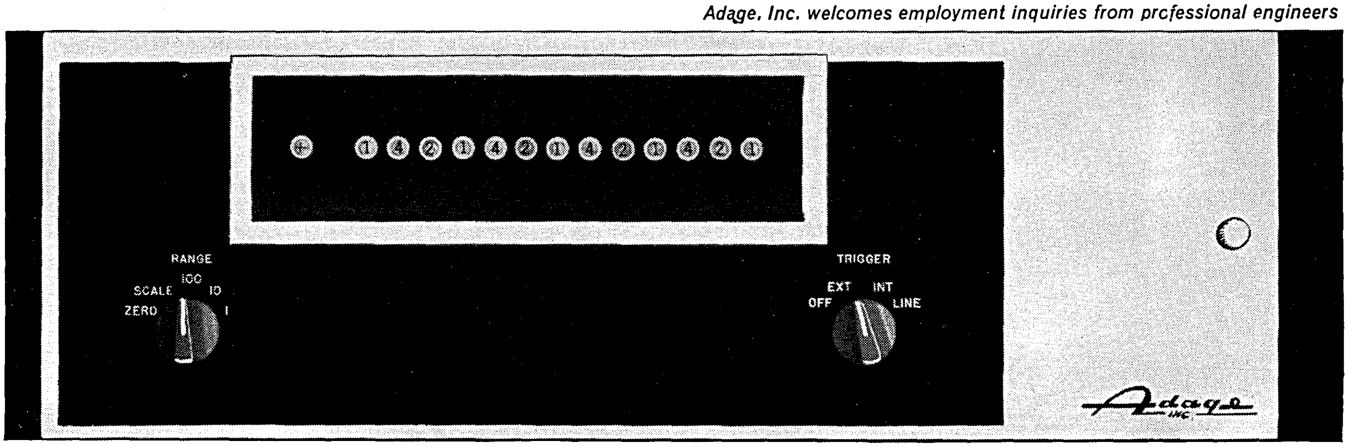

CIRCLE 7 ON READER CARD

letters

escalated emotions

Sir:

Your December editorial (p. 23) displayed R. L. Patrick clearly as the Most Hysterical Nuclear Thinker of 1963, and probably the Worst Writer. Let's not have any more of this kind of stuff!

WILLIAM J. HARRINGTON
Livermore, California

Sir:

I have seldom read a more fatuous, juvenile, and asinine editorial in a trade magazine of national circulation . . . your attempt to mix God, Kennedy, atomic war, and computers into a potpourri was the height of bad taste.

GEORGE GORDON
FordTech Agency
New York, New York

Sir:

Please cancel my subscription . . . I feel that the editorial is in very poor taste.

JOSEPH M. FONTANA
TRW Computer Division
Canoga Park, California

Granted.

Sir:

. . . Let's hope that at a later, calmer time, you put aside your preoccupation with chimerical wars, riots and panics, and found a moment to mourn the death of our president (who had a greater life in front of him at 47 than any of us will ever know) and to commiserate his widow and children.

What moved me to prayer was not that some factitious holocaust wasn't there to be averted, but that our government, its Constitution and laws made the assassination as futile as it was insane. You might offer a prayer of thanks (but, please, in plain, ordinary English) for that, and leave the concern for war to calmer minds of the men who have that responsibility.

J. R. JOHNSTON
Malibu, California

Admittedly highly emotional, the editorial reflects the thoughts expressed by two intelligent, competent computer specialists—who have been active in, among other things, the design of military command and control systems—in the 60-or-so minutes following the first news of the President's tragic assassination. Its publication was intended to draw the attention of those engaged in the design and operation of such information systems to the importance of the human decision-making processes. We are thankful to the military for exercising control during a period which could easily have been twisted into a major international crisis. We do not think this is in "bad taste."

leasing: bold or . . .

Sir:

The December Business & Science quotes Bob Harmon of McDonnell Automation Center as having taken a bold move in leasing a 7094. By leasing, I assume is meant hardware ownership in some form. I disagree that this is a bold step, certainly not if one analyzes use-time, extra-shift time and hardware life and compares these factors to rental cost. This fear of buying is even harder to understand among the business firms and government users with large requirements. Suppose gear is no longer needed at one installation, it could become a surplus item of supply for another user to empoy.

This month at the FCC, we accepted delivery of a purchased Univac III system. Let us hope the trend continues, at least in the federal government.

TERRY MILLER
Computer Operations Branch
Federal Communications Commission
Washington, D.C.

the 1004 & computers

Sir:

Charles W. Adams is to be congratulated for honesty and frankly including the Univac 1004 among computers and edp equipment—where it properly belongs ("Once Again," Nov., p. 30). Anyone who correctly programs this machine and uses it intelligently finds himself (1) employing the soundest of edp principles, systems and techniques, and (2) trimming the pants off several other acknowledged edp systems insofar as real work production and cost are concerned.

Why the Univac people fail to properly recognize this product is, I guess, "one of those things." So the 1004 is a "card machine?" What computer or edp system other than analogs do *not* use cards somewhere in their operations? Thank goodness we have magazines like *Datamation* and experts like Mr. Adams to keep the records straight.

JOHN FUNARO
California Revenue and
Management Agency
Department of General Services
Sacramento, California

price correction

Sir:

Contrary to your write-up (Dec., p. 17), the price of the model 909 input unit is $4500, instead of the $1500 quoted.

RAYMOND B. LARSEN
The Electric Information Company
Broomfield, Colorado

communication line speed

Sir:

Regarding your Business & Science story (Dec., p. 20) on Philco's PCP-150 message and data switching system, different speeds and methods of data transmission must be considered individually and cannot all be provided over a 75 wpm line.

A.M. ROSCOE
Bell Telephone Co. of Pennsylvania
Pittsburgh, Pennsylvania

statistical relevance

Sir:

In "Programmer Training," (Dec., p. 48) James Saxon claims that an experimental group of people were taught programming fundamentals with a self-instructional text and scored higher on an identical final exam than a group of people taught in a traditional classroom setting. A factor Mr. Saxon apparently did not take into account was the possible difference in intelligence, abstract reasoning or even learning ability that might have existed between the two groups . . .

A. J. BIAMONTE
NYU Management Institute
New York, New York

Author's reply: The point is valid if the study had been designed as a psychological depth project. All people hired for programming jobs by Lockheed had to meet basic requirements for education and intelligence. Since the selection of personnel for the two groups was random, it was safe to assume that learning ability, etc., was also randomly distributed between the groups. The basic point of the article was not the original experimental study, but the fact that after considerable tryout, the technique coninued to work, producing people who knew the basics of programming *at least* as well as had been previously accomplished . . . The accrued advantages of savings of unproductive time (waiting for a class to be formed), classroom space and instructor time far overshadows other considerations even if it would take longer (rather than less time) to produce the same results by "self-instruction."

never-ending k's

Sir:

Please let me know how many of your erudite readers point out to you that in your Letters column of November, in discussing with Clifford Woodbury

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Printed by Beslow Associates, Inc.

the matter of Roman numerals, both of you are talking Greek!

John Trytten
Sola Electric Company,
Elk Grove Villiage, Illinois

Sir:
A simple and straight-forward suggestion: use BK to denote 1,024 computer locations, and DK to denote a unit of 1,000.

Arthur P. Buhrman
Computing Center
Florida State University
Tallahassee, Florida

recording calendar dates

Sir:
The following proposal for a New Standard Practice for Recording the Date may be of interest to your readers. It is proposed that by not later than January 1, 1966, the practice of recording all dates be standardized in the sequence of year, month, and day. Perhaps this new standard should be adopted no later than the date upon which the world calendar is adopted.

In the U.S., the usual practice has been to record the month, day and year; thus the 6th of January 1964 would be recorded as 1-6-64 . . . our military organizations have preferred the day, month, year sequence . . . However, there is another facet to this besides confusion. Dates are a prime basis for filing in many data storage systems because the chronological sequence is most important. An alphanumeric code is the best means of filing in a vast preponderance of filing systems. But the current practice of recording dates makes the dates themselves unsuitable as a modern filing means. . .

. . . If the date code sequence were year, month, day, then the code becomes a practical means of data filing. 64-01-05 would thus represent 1964 January 5. In every case the date code would maintain the true chronological order by date and, if desired, the hours or minutes could be added without affecting the system.

Edward L. Page
Department of Industrial Engineering
University of Michigan
Ann Arbor, Michigan

DATAMATION calendar

● The winter 1964 meeting of SHARE, the IBM 704/9/90/94/40/44 Users Group, will be held at the Jack Tar Hotel, San Francisco, March 2-6.

● The American Management Assn.'s EDP conference will be held March 2-4 at the Statler-Hilton in New York City.

● Northwest Chapter of DPMA will hold a Management Seminar, March 12-13, at the Leamington Hotel, Minneapolis.

● The 14th meeting of TUG (Philco 2000 users group) will be held March 18-20, at the St. Francis Hotel, San Francisco. Western Development Lab. will host.

● CDC's small and medium-scale computer users group will meet April 7 at the Hilton in Albuquerque, N.M.

● The Spring conference of the Univac Users Assn. will be held April 20-22 at the Sheraton-Chicago Hotel, Chicago. Hosts will be U.S. Gypsum Co. and Harris Trust & Savings Bank.

● The 1964 Spring Joint Computer Conference will be held at the Sheraton Park Hotel, Washington, D.C., April 21-23.

● The spring meeting of CUBE (Burroughs Users group) will be held April 22-24 at the Ben Franklin hotel in Philadelphia.

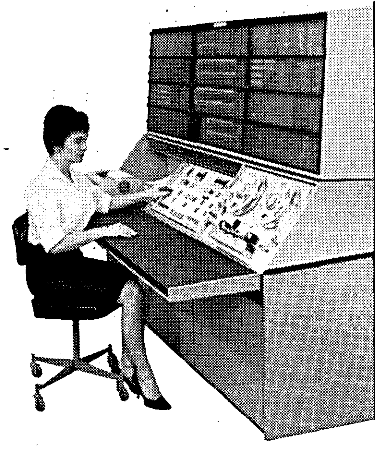
● GUIDE International (large scale IBM edp machine users group) will hold its next meeting at the El Cortez Hotel, San Diego, May 5-8.

● The fourth national conference of the Computing and Data Processing Society of Canada will be held on May 11-12 at the Univ. of Ottawa.

● The ninth annual Data Processing Conference will be held at the Hotel Stafford, Tuscaloosa, Ala., May 12-13. Sponsors include DPMA, National Accountants Assn., U. of Alabama, and Certified Public Accountants.

● The POOL 1964 annual general meeting will be held May 12-14, at the Palmer House in Chicago.

PB440 THE FIRST REAL SYSTEMS COMPUTER ?



SOME TYPICAL PB440 SYSTEMS APPLICATIONS

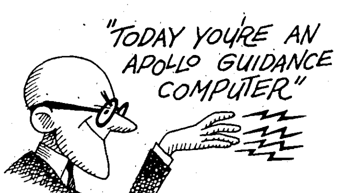
- Telemetry data reduction
- Communications switching and data formatting
- Hybrid analog/digital computing
- Real-time data acquisition
- Command and control
- Automatic checkout
- Launch control
- Antenna steering
- Nuclear reactor control
- Process control

WE THINK SO, but we put the question mark in so you wouldn't accuse us of unabashed arrogance. What we mean is we have a computer that isn't restricted by the fixed logic wired in by the manufacturer. The PB440 has a separate logic memory—distinct from its conventional memory—and commands and word formats are specified by information stored in this logic memory and can be readily changed. In other words, commands and word formats can be tailored by the user to fit the systems problem at hand. Packard Bell provides several command sets and the user can create additional commands as required.

A single PB440 can, in the fraction of a second it takes to reload logic memory, switch from one command set to another and thus from one application to another. No other computer can do this, and that's why we think it is the first real systems computer. Now, the system designer can adapt the computer to the problem, not the problem to a fixed command list and format.

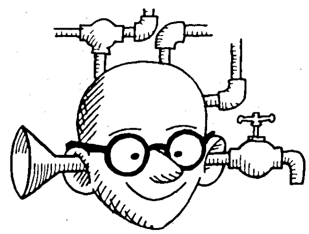
FOR THE SYSTEMS ENGINEER the PB440 can be a special-purpose computer designed (to his specs) for his specific system. But he still has the reliability, versatility, expandability and speed of the PB440 as a general purpose computer. This is all made possible by the Dual-Memory Stored-Logic organization of the PB440.

SPECIFICALLY, the systems engineer should consider the following features:

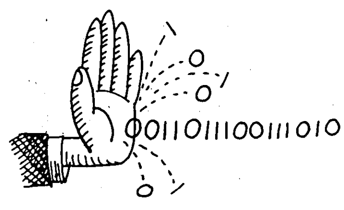


MICROPROGRAMMING the logic memory provides ability to duplicate command lists and formats of other computers. For example, digital guidance computer command structure and format can be developed before hardware prototypes are built. Similarly, you can duplicate the guidance computer in a hybrid simulation of a missile guidance and control system.

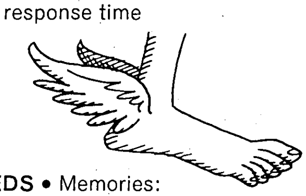
SOFTWARE • More than 100 systems-oriented commands written, more every day
170 scientific commands
FORTRAN compatible with 7090



MEMORY ACCESS
Direct memory access from external devices
Simultaneous computation & I/O data transfer
Shared memory feature that permits multiple processor configurations



PRIORITY INTERRUPT • Multi-level, minimum response time



SPEEDS • Memories:
1 μsec non-destructive logic memory (256 to 4096 words)
5 μsec main memory (4096 to 32,512 words)
I/O rate to 9.6 million bits per second
Typical execution times, with memory access:
Compare data against upper & lower limits—13 μ sec, including two memory references
Floating point multiply 8 bit exponent,
16 bit mantissa—36 μ sec
24 bit mantissa—42 μ sec
39 bit mantissa—110 μ sec
Fixed point add—3 μ sec
Relocate data within memory—10 μsec/word
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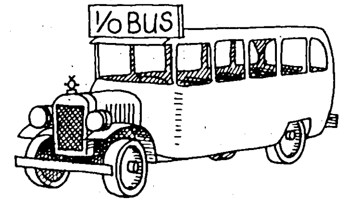

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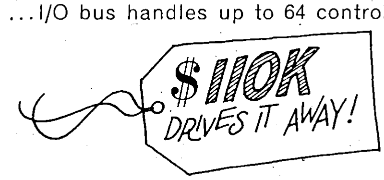

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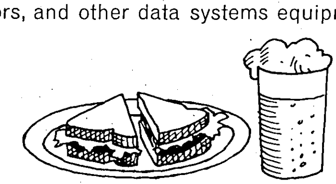

THERE'S MUCH MORE to be said about the PB440 and its unique concept of Dual-Memory Stored-Logic. We have shelves of technical literature that can handle most of your questions, representatives who should be able to take care of the rest. If you are in Los Angeles, try and drop in for a demonstration. We might even pop for lunch.

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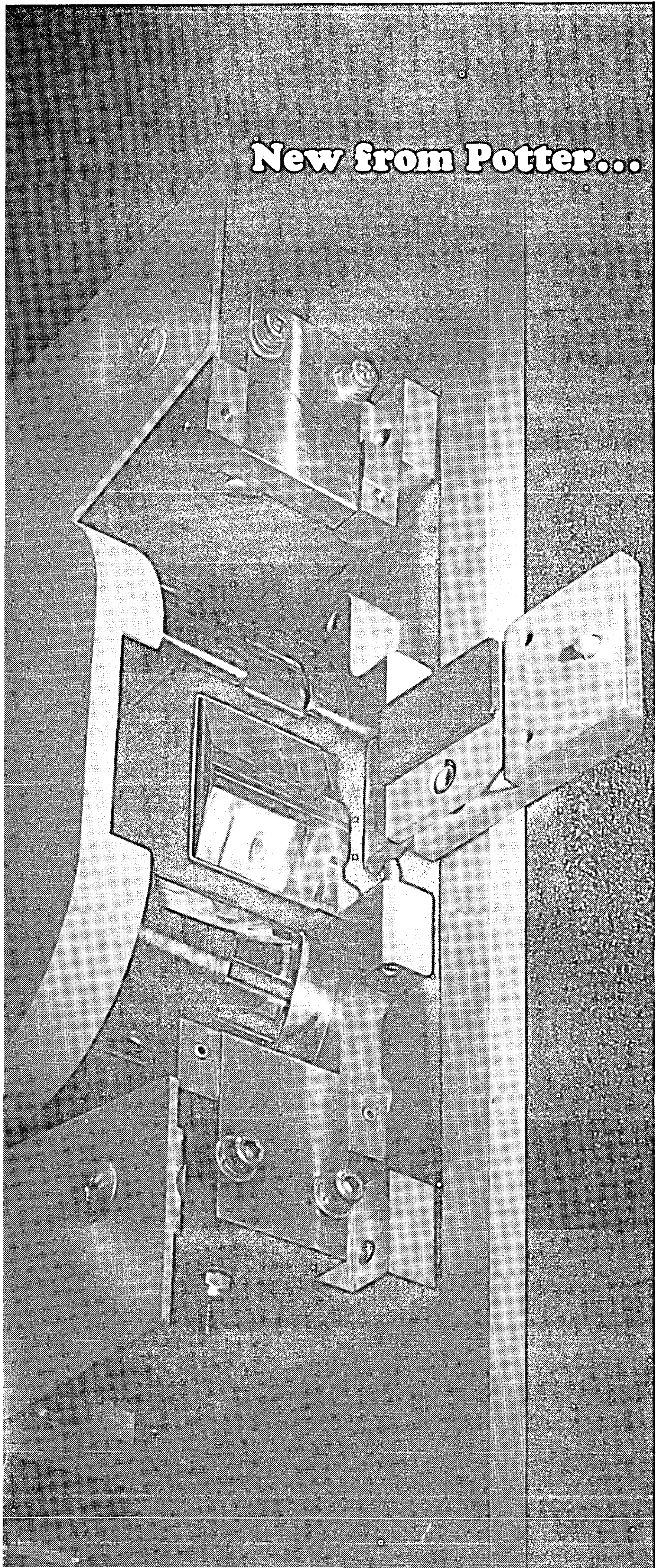

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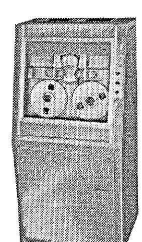

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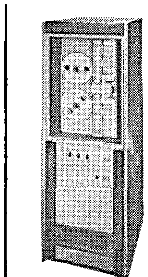

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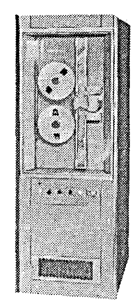

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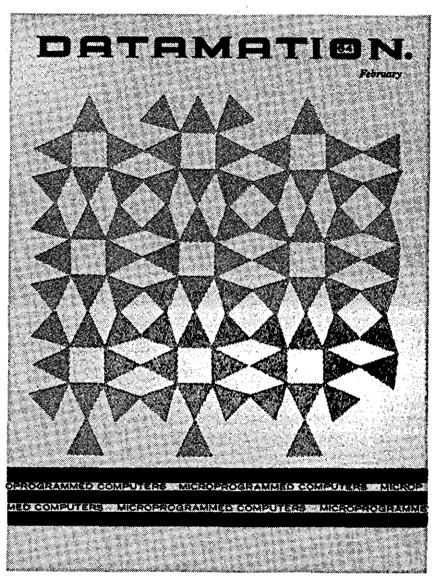

Cover

"Ordered chaos" — the inherent capability of microprogrammed computers to provide varied command repertoires by different combinations of micro-instructions is suggested in this month's cover design by Art Director Cleve Boutell.

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CIRCLE 13 ON READER CARD

BUSINESS & SCIENCE

INCENTIVE MAKES SENSE FOR L.A. PROGRAMMING FIRM

Incentive salaries and the ability to control and measure programming efforts have paid off for a young Los Angeles-area programming services firm. Founded a year and a half ago, Data Processing Systems switched to an incentive plan after two months during which founders Hank Watson and H. V. Nichols "lost their shirts." Since then, the firm has been in the black, and programmer salaries have increased an average 40%.

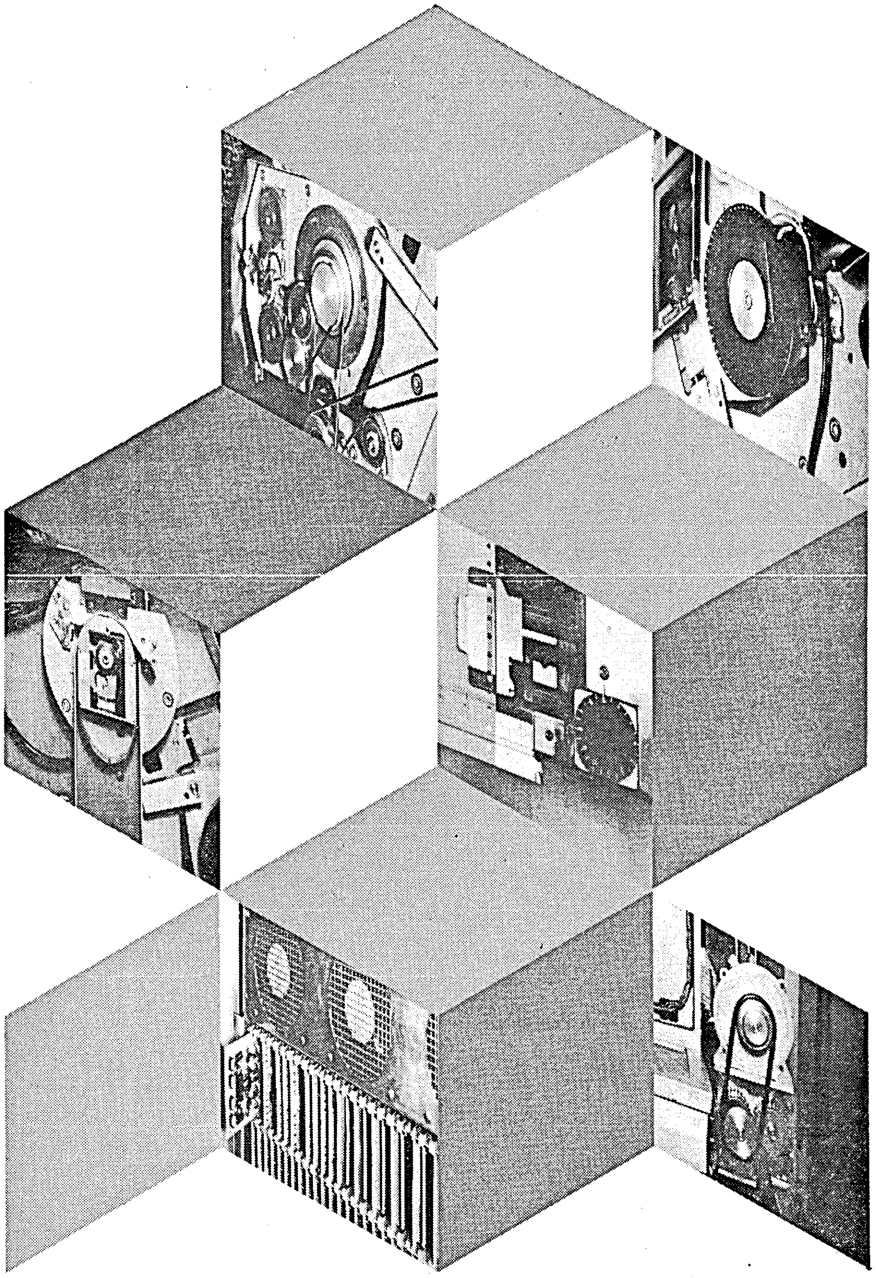
DPS, with 18 people in L. A., 11 in Palo Alto, divides all programming work into logic charting, coding, and testing/debugging; pay is divided among these activities 60, 30 and 10 percent respectively. Customers are charged per workable instruction; pay is allocated on the same basis. Charges are approximately 25% of the lowest figure obtained in a survey made by Watson while he was head of dp for a division of General Controls.

DPS pays careful attention to environment; programmers work in a phone-less bull pen--a separate room with blackboard is provided for conferences. The company also limits a project manager's working group to five programmers . . . only three such groups report to any one division manager. Average age of the company's employees: 31. Average computer experience is 4½ years. Only person not on the incentive plan is the receptionist. That's only until they figure how to evaluate her contribution.

ASSORTED FINANCIAL NOTES; CSC STOCK TAKES OFF

Industry insiders watched agog last month as Computer Sciences stock went crazy. Sparked by merger rumors, the news that CSC would be going on the American Stock Exchange, and some solid promotion, the over-the-counter stock zoomed up to the 30-31 range in mid-January, after opening at 12½ in September. Meanwhile, competitors' CEIR and Computer Usage stock hovered in the 9-10 and 18-20 ranges, respectively. CSC denies categorically any rumors that it's for sale, but is looking acquisitively at three companies. Other financial news: Anelex has also won listing on the American; Data Products has asked for SEC registration of 324,903 more shares of common stock to go with some 2½-million now outstanding.

--continued on page 19



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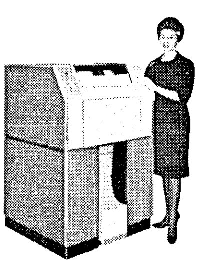

Computer designers and system builders are using the Anelex "building-block" principle to specify printer systems which fit their customers' needs. An almost unlimited choice of specifications is available . . . printing speeds from 200 to 2500 lines per minute . . . any number of columns from 20 to 160 . . . any language, type font or character array, plus an add-on feature which provides for future system expansion. You select the modules and logic designs which most economically meet your printer requirements. Then Anelex will build your printers or printer systems in quantities from one to a hundred or more, without prototype cost or delay.

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CIRCLE 47 ON READER CARD

MORE HARDWARE FOR FTS, AUTODIN

Univac will supply three 418 computers to Western Union for the $27.8-million Federal Telecommunications System, private wire hookup for GSA. Placed in East coast, Central and West coast sites, the 418's will handle message switching for an estimated 1100 stations initially . . . maybe up to 4000 government "subscribers" eventually.

Another federal communications system, AUTODIN, is being updated; RFQ's have gone out. It's understood that the system's five operating centers will be expanded to 10-15, including a brand new tie-in of overseas centers. Expansion may call for an additional 20 computer systems, including back-up units. Indications are that computers for foreign sites will be acquired directly by DOD; domestic site systems will be acquired under subcontracts let by AUTODIN prime Western Union.

MICROFILM PRINTER DISAPPEARS

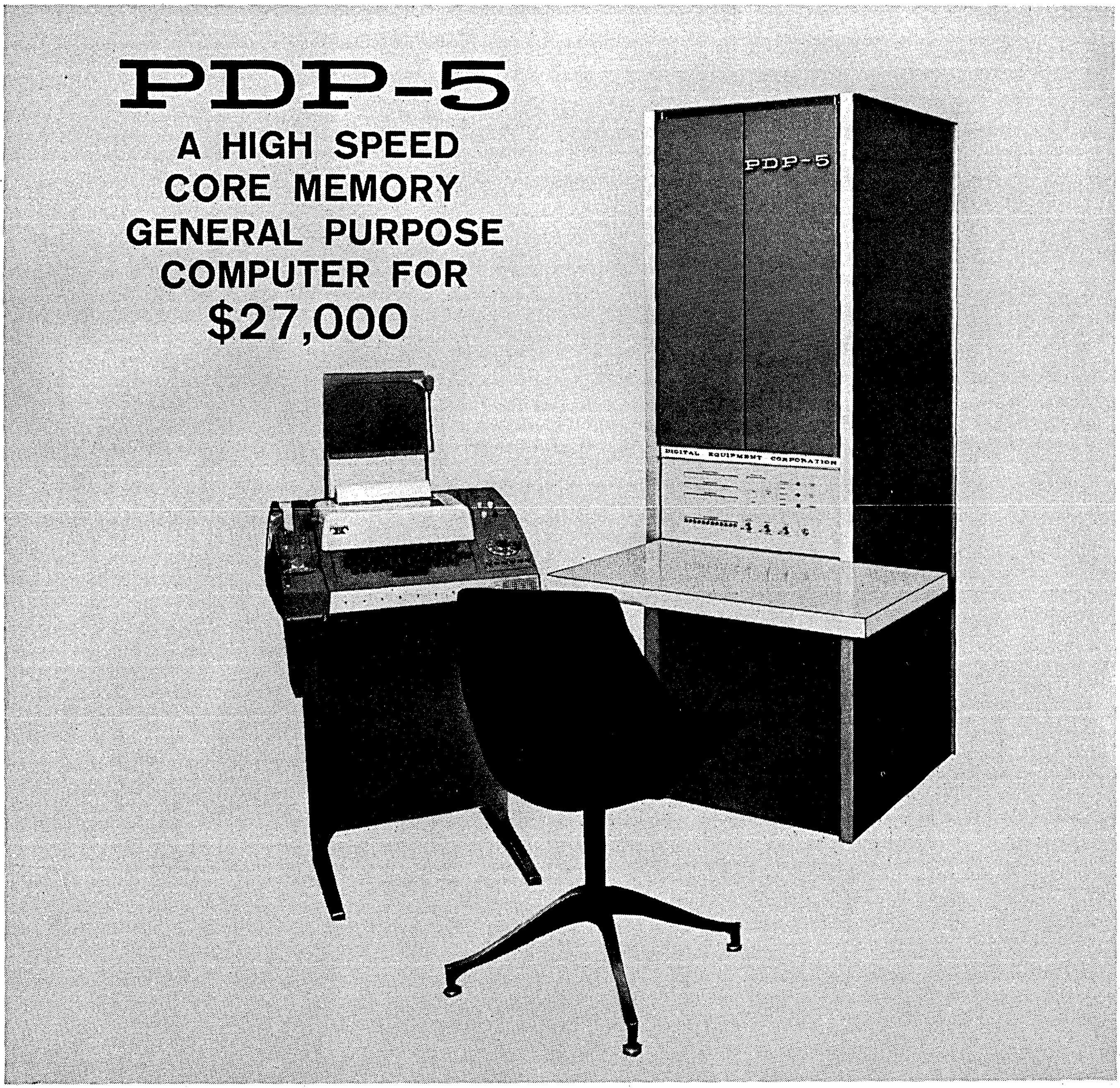
Silently folded, taking with it the Benson-Lehner 943/4 microfilm printer, is Transdata, San Diego-area firm. Marketed by B-L, the printer may appear in new form under the sponsorship of Straza Industries, San Diego, which has absorbed key Transdata engineering personnel. Still mum about its printer plans, Straza--primarily a metalworking firm--has announced a symbol generator.

ADP GLOSSARY WINS FRIENDS

The year-old "Automatic Data Processing Glossary," though put together on a shoe string basis by an ad hoc committee of the Budget Bureau, has won considerable favor among computer folk, in and out of Government. The glossary, which covers 62 pages and some 1,500 terms, is being recommended as an interim standard by the X-3.5 sub-committee of the American Standards Association until publication of the ASA's own glossary. Some universities are also reported using the glossary as a text. Copies may be had from the Government Publishing Office at 40 cents each.

RUMORS AND RAW RANDOM DATA

AFIPS has opened an office, sharing space in NYC with the ACM, and has Redmond Gardner, formerly with the IEEE, running it . . . San Diego and Los Angeles have lost their bids for the '65 FJCC, which will be held in Las Vegas again . . . The L. A. Sheriff's dept. has thrown in the towel on its attempt to develop a realtime system. Consultant Computer Usage has recommended a feasibility study of a small-scale system for only the most active criminal and jail files . . . A contest for the most original computer program is being sponsored for high school students by the Association for Educational Data Systems. First prize: $150; the six runner-ups get $50 each; the next 10 will win (?) subscriptions to Datamation. Information can be obtained from Don Bushnell, Systems Development Corp., 2500 Colorado Ave., Santa Monica, Calif. 90406 . . . Walter F. Bauer, George Forsythe, and Bruce Gilchrist have been nominated for the presidency of the ACM, which has named a five-man committee to investigate possibilities of a reorganization of its structure . . . . Latest computer firm to go public: Planning Research Corp., L. A. systems consulting & software house.



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WASHINGTON REPORT

AUTOMATION AND POLITICS

"We must...establish a high level commission on automation. If we have the brain power to invent these machines, we have the brain power to make certain that they are a boon and not a bane to humanity." With these State of the Union words, President Johnson reaffirmed a committment to the late President Kennedy's long-standing proposal. He has enthusiastic supporters in Congress, both from Republicans and Democrats, for establishment of an automation commission. Sen. Jacob Javits (R.-N.Y.) entered a measure, SJ 105, last July which would establish a Federal Commission on Automation. Hearings have been held and testimony taken, nearly all favorable. A subcommittee report, which will be the basis for further legislative action, is now being prepared.

A similar bill in the House, HR 8429, has been referred to committee. To deal with economic and social dislocations caused by automation, a Hoover-type commission has been proposed by two Democratic senators, Humphrey (Minn.) and Hart (Mich.).

Despite all the tub-thumping, not much action is expected on these measures in the current Congress. "If the President wanted," noted one capitol observer, "he could appoint an executive commission on automation without specific Congressional direction. He has the authority, but a lot of noses on the Hill would be put out of joint if he did." Odds are, he'll wait for Congressional action.

DOD PLANS $200 MILLION SWITCH TO COMPUTER PURCHASES

The Defense Dept. is reported planning in the near future to purchase some $200 million worth of computing equipment it now leases. This figure, which represents current market price, is expected to increase substantially as additional economies are identified.

This decision, made last December, to act on the policy recommendations set forth in BuBudget circular A-54, dated Oct. 14, 1961, effectively ends several years of military heel-dragging in the purchase vs. lease controversy.

The immediate effect on hardware manufacturers will be a swollen cash flow for the year, though for the long range it means a substantial fall-off in revenue from DOD. Chief loser is, of course, IBM, which has the lion's share of the DOD market and has in the past favored leasing arrangements.

A.F. PURCHASE OF CDC 1604 WINS MERIT POINTS

The GAO's most recent report to Congress on computer acquisition practices of the military places a left-handed pat on the back of the Air Force. The report,

Continued on page 92

EDITOR'S READOUT

WANTED: SUPER-SPECIALISTS

Despite a continuing cacophony of complaints about hardware, people remain the biggest problem in information processing. Computers are meant to be used by people, after all, although this is not always apparent. Which is perhaps the clearest indication that they are designed by humans.

The people problem takes many forms—from machines which don't do what they are supposed, or promised to do . . . to the inability to use hardware and software intelligently. In nearly every case, the cry goes out for more and better people.

Since experienced computer people are not manufactured overnight, attention turns to something called education. Certificate programs are created, programmed instruction is tried . . . high schools, trade schools and universities develop special curricula. It's just a little bit reminiscent of the scene just after Chicken Little announces that the sky is falling.

We have no quarrel with honest attempts to upgrade people, to help them grow, get more savvy. But we feel that perhaps what has passed for education could better be called training: the development or enhancement of technical skills to meet today's technical problems.

But we'd like to suggest that the really big problems are not primarily technical . . . and that they are not today's but tomorrow's. This is another way of saying that what we need is not so much specialists as . . . well, let's call them generalists or super-specialists: people capable of understanding (and communicating intelligibly about) a problem in its broadest-perspective totality . . . able to foresee the implications of a problem and its solution, able to evaluate and direct the work of specialists.

We're not pretending to know how such people can be found or developed. But perhaps education—as distinguished from training—holds a clue. This kind of education develops the abilities to think critically and creatively, to grasp the fundamental tools of analysis—in English, statistics and math—to distinguish between large and small, critical and petty problems . . . and to communicate clearly.

Perhaps one of the greatest strengths of the computer industry so far is that it has attracted from an amazing variety of disciplines a wild assortment of bright, interesting, creative people. Maybe we need more of this kind of person, rather than the nicely homogenized product of a standard training system.

MICROPROGRAMMING AND STORED LOGIC

an introduction

by LOWELL D. AMDAHL

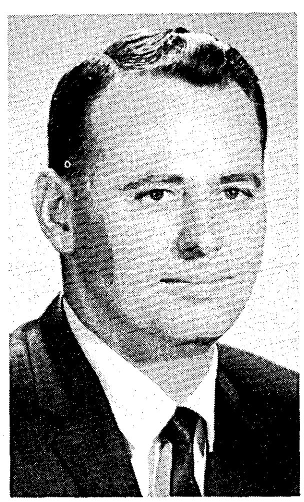
In recent years a few computers have appeared on the scene with the billing "stored logic" or "microprogrammed." They have been greeted with a mixture of wonderment, apathy and concern. Interestingly, the concern has been both that these computers are not really different, and that they are too different. While manufacturers have claimed that they are a step forward in ease of use, the prospective user has often responded that these computers are difficult to program.

To investigate stored logic and microprogrammed computers, we are forced to consider a subject that has been largely relegated to the classroom—computer organization. Rather than dust off a classical model of this type of computer organization, three existing computers are described: the Thompson Ramo Wooldridge 133, the Packard-Bell 440, and the Collins 8401.

Microprogrammed computers basically differ from conventional computers in that the equivalent of a single instruction in a conventional computer is often a subroutine (interpreted instruction) in a microprogrammed computer. This simplifies the control sequences which are built into the microprogrammed computer, and permits greater flexibility in producing variations of instructions. However, the penalty for using interpretive subroutines is additional execution time. Much of this additional time can be offset by designing for efficient subroutine linkage, and by the use of a high speed memory to store the interpretive control sequence.

definitions

First, let's clear away some terminology. As a design characteristic, we'll equate stored logic and microprogram-



Mr. Amdahl is a Southern California-based consultant in computers and computer systems, and an editorial adviser to Datamation. His systems experience includes command control, data acquisition and telemetry, multiple computer configurations, and automatic test and checkout. He has also participated in the design of several computers. Previous affiliations: Digital Science Consultants, TRW, and IBM. He holds a BS in engineering physics from So. Dakota State College, and an MS in physics from Kansas.

ming. The term stored logic was first applied in the mid-1950's to a class of highly sequential (and speculative) processors somewhere between a Turing machine and a simple drum computer. Since conventional computer instructions were performed as a lengthy sequence of very simple commands, i.e., interpreted, the logic of these processors was said to be stored. Blankenbaker[1] referred to the design of this type of computer as "logical microprogramming."

Actually, the word "microprogramming" was first used to describe a particular kind of implementation of computer control. In a paper with an unusually pompous title, Wilkes[2] described the hardware mechanization of microprogramming as consisting of two control matrices. One of these matrices produced a subsequence of control states for a given instruction, while the other selected specific micro-operations for each of these states. A control state, or micro-operation, was typically used in the execution of several different instructions. Thus, the set of micro-operations was the basic command set of the computer.

Mercer[3] extended this work by studying various sets of micro-commands, with the added notion that the computer programmer should be free to determine his own set of interpreted instructions.

stored logic in parallel computers

The application of stored logic, or microprogramming, to parallel core memory computers has turned out to be as much a variation on conventional design as it has been a totally new concept in design. The three computers described in this article bear little similarity to each other from a block diagram point of view—as similar to conventional computers as to each other.

All three have in common, though, built-in techniques to facilitate interpretive operation. For example, each provides two address registers for the two program strings followed in the interpretive mode: (1) the calling sequence, and (2) the location within the current interpretive routine. It is feasible to have one of these two registers stored in memory, but this results in a penalty in execution time that none of these manufacturers has accepted.

calling sequences

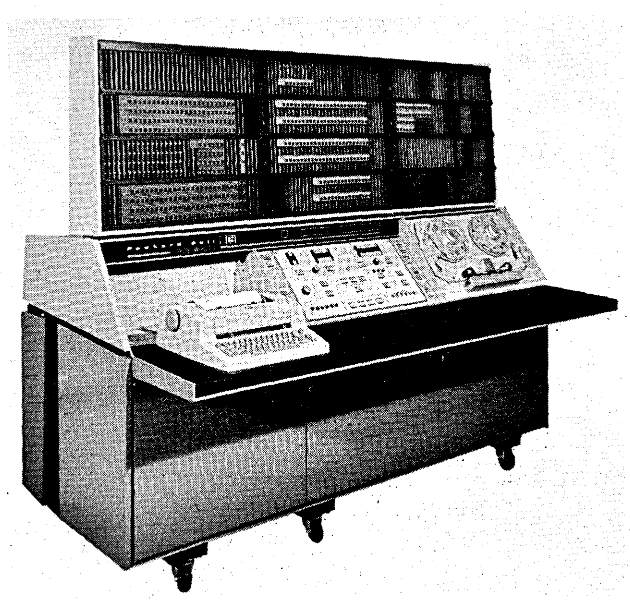
The main program, consisting of a set of macroinstructions which are interpreted, is referred to as a calling sequence. It is of interest to compare the nature of the calling sequence in each of the three machines. In doing so, remember that each call, or macroinstruction, represents data to the interpretive subroutine—it is not directly executed from the instruction register of the computer.

In the TRW-133, each call begins with a 15-bit address. This address specifies a starting address for an interpretive subroutine (logram) which can be located anywhere in core memory. Following each address in the calling sequence can be any number of words of data, constants and addresses which the interpretive subroutine is equipped to use. TRW has several sets of available lograms, including fixed and floating point arithmetic, as well as more complex operations such as matrix arithmetic.

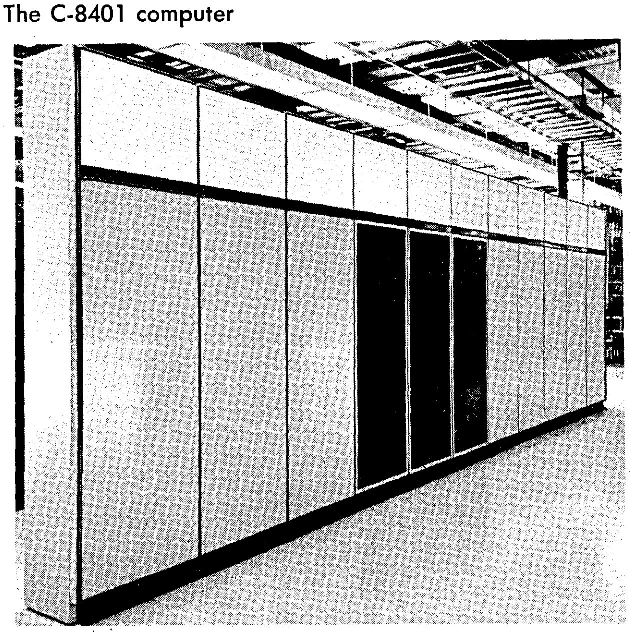
Quite a different calling sequence format is used by the PB 440. Within its 24-bit word, a 15-bit address is used as an operand or result address in much the same manner as it would be used in a single-address machine. However, any action on this address is delayed until an interpretive sequence (microutine) has been entered. The starting address of this sequence is determined by a table lookup in its fast memory, using the first six bits of the call word as the entry address to this table. The remaining three bits of the call word are used for address options. Since the calling sequence format is interpreted, it could be modified or changed completely. The design of the PB 440, however, enhances this call word format as well as a floating point number format.

The C-8401 is an interesting example of a microprogrammed computer well suited for general purpose computation and real-time applications. A combination of configuration options and interpretive operation gives it speed and flexibility as a programmable controller in high speed communication systems. The calling sequence (macro-program) of the C-8401 is stored as 16-bit words in main

The PB 440 computer



The C-8401 computer



memory. Being of address length, the format of the call can be similar to that mentioned for the TRW-133. However, the interpretive routine of the C-8401 is executed from a high speed memory 36 bits wide. Linkage from one macro-program instruction to the next utilizes an explicit linkage micro-program called Read Next Instruction (RNI).

basic commands

The set of commands to which each of these computers is responsive has been carefully selected to minimize control complexity, and at the same time, to be well suited to efficient use in interpretation. All three computers permit at least two commands per computer word. These commands do not carry full memory addresses; therefore they can be classified as no-address. Commands do, however, identify specific registers as address sources. New addresses are obtained by incrementing or otherwise modifying these register values, by transfer into the register of an address from the calling sequence, or by indirect addressing. In some cases, short addresses are used to specify scratchpad locations or relative addressing.

The TRW-133 15-bit logand has a primary command which is modified by a register address field (specifying one of four registers to be used either directly or indirectly), and by a control field (controlling register incrementing and memory accessing). The remaining four bits of the logand contain a secondary command which is a restricted set of register manipulations not involving the memory. One logand can produce several operations. Execution time for a logand is typically four clocks (two memory cycles, direct addressing) or six clocks (three memory cycles, indirect addressing). Variable length or extended length logands are also permitted. For example, the TRW-133 is the only one of the three computers which has built-in full multiplication and division.

The command structure of the PB 440 utilizes a pair of 12-bit micro-orders in one computer word, each of the pair being essentially independent. The order code (six bits) is modified by two register address fields (three bits each). Each of these addresses selects one of seven registers to provide or receive data from logic buses. Since all arithmetic and register transfer logic is associated with these logic buses, any register can directly participate in any manipulation. Multiplication and division are facilitated in the PB 440 by multiply-step and divide-step operations under control of a repeat counter. Most micro-orders are completed in one clock time.

The C-8401 has three 10-bit micro-instructions and a six-bit control field in each 36-bit instruction. Each micro-instruction contains two register addresses, one for source and one for destination. Unlike the other two computers, the C-8401 does not employ an operation code. Rather, the type of operation is implicit in the logic associated with the particular destination register. Operations such as multiplication and division are highly microprogrammed in that many micro-instructions are involved. These micro-instructions are executed at a high rate of speed and are facilitated by the use of a common bus structure.

core memory

The PB 440 and the C-8401 employ two memories. Both use a fast access nondestructive memory to store the interpretive subroutines. Since these subroutines are relatively fixed, write time is of secondary importance. For general storage, they both use a slower speed core memory of a conventional destructive readout type. Because of macro- and micro-instruction word length differences, the C-8401 clearly distinguishes between these two memories. The PB 440 employs the same word length in each memory; therefore there are no absolute restrictions on the proportions of its logic memory and program memory.

The TRW-133 employs a homogeneous high speed coincident current memory for both logic and program use. Thus, its lograms can be placed anywhere in core memory.

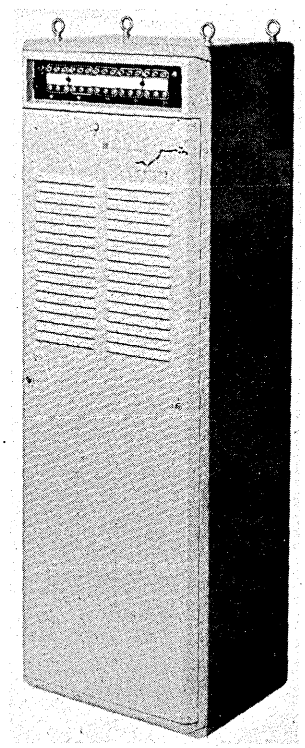
A characteristic of stored logic computers as compared to conventional computers is the small number of clocks, or beats, per operation code. For these computers, this ratio is only one, two or three, whereas for conventional computers it would likely be in the range of four to 12.

conclusions

The advantages and disadvantages of microprogramming/stored logic are often difficult to weigh. On the one hand, the interpretive computer usually has an overhead penalty when compared on the basis of the instruction repertoire of the conventional computer. On the other hand, its greater flexibility and efficiency for more complex instructions can mean improved throughput time.

The customer who plans to use this kind of computer in machine language may find that his programmers have difficulty with it. Similarly, the customer interested in using microprogrammed computers in their intended interpretive mode may have met with a confusion of macroinstructions which are (a) not ready for use, or (b) poorly designed for his application. Like other supporting software, this is a scourge which time alleviates.

The TRW-133 computer



The millstone of "too much flexibility" has unquestionably been a deterring factor in the acceptance of microprogrammed computers. Several years ago, Wilkes[4] demonstrated considerable insight into this problem by declaring the world unready for the chaos of offering a programmer a variable machine. He said that ". . . problems involved in running a computing laboratory are bad enough as it is, without the additional license which would be created by a system of private order codes."

Faced with the existence of these computers, the manufacturer and the user can modify this counsel by applying strict discipline to the variety of instruction repertoires in which they indulge. ■

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THE TRW-133 COMPUTER

by W. C. McGEE

The TRW-133 is the latest in the TRW stored logic computer family, which now includes three militarized real-time control computers, a general purpose scientific and engineering computer, and a business data processor. The TRW-133 continues and extends the basic design philosophy of the TRW-130 (AN/UYK-1) computer, which was developed under the sponsorship of the Navy Bureau of Ships to serve as a fully militarized, multiple purpose shipboard computer.

Of the various requirements placed on the TRW-130, those having the greatest impact on its logical organization were that it be extremely reliable; that it be physically small; and that it be capable of communicating with NTDS (Naval Tactical Data System) devices. To meet the reliability requirement, it was decided to use solid-state components throughout the computer, and in particular to use a magnetic core memory. To facilitate communication with NTDS devices, and at the same time minimize hardware cost, a word length of 15 bits—one-half of the NTDS 30-bit standard—was selected. This choice of word length, coupled with the availability of fast and relatively inexpensive core memories, suggested that the computer's principal mode of operation be interpretive—that is, that it achieve the equivalent of conventional computer instructions by executing sequences of elementary logical commands stored in memory. By this means, only the logic implied by the elementary commands had to be implemented in hardware, further enhancing the computer's reliability and reducing its size and cost.

The TRW-130 has found many uses other than its intended shipboard application. Its small size and rugged construction make it suitable for use in adverse ground and air as well as shipboard environments. Where data precision requirements permit, e.g. in certain data reduction applications, the computer is being operated in the conventional mode and achieving processing rates comparable to much larger computers.

The TRW-133 was developed to meet demands for increased processing capability. It embodies the same basic design as the TRW-130 but is three times as fast internally and has expanded input/output facilities. The discussion that follows is based specifically on the TRW-133, but applies in large measure to other members of the TRW stored logic computer family.

computer organization

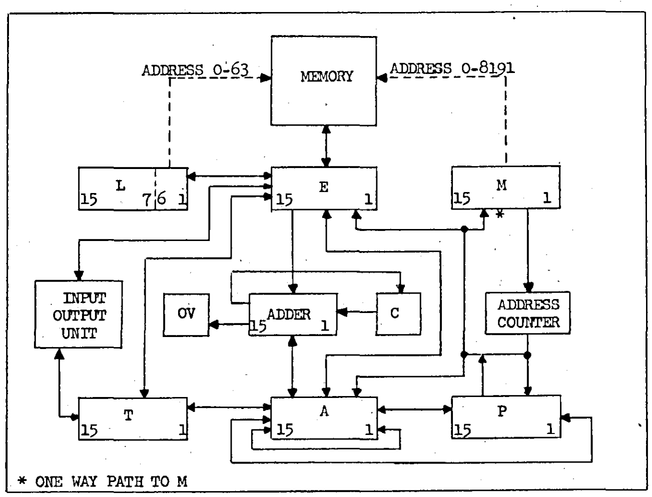
The principal components of the TRW-133 computer are as follows (see Fig. 1):

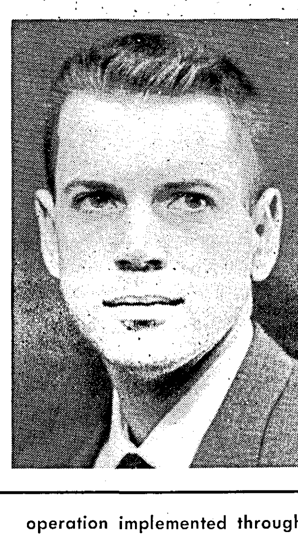
(1) a coincident-current type magnetic core memory of 8,192 (expandable to 32,768) 15-bit words, with a symmetric read/write cycle of two microseconds;

(2) six addressable flip-flop registers of 15 bits each, performing the following functions:

E: Memory exchange register
L: Logand* decoding register
M: Memory addressing register and logand sequence counter
A: Accumulator

Fig. 1





A member of the Programming Sciences Dept. at the TRW Computer Div. in Canoga Park, Calif., Mr. McGee is responsible for departmental activities in hardware systems organization and software research. He has participated in the conception and specification of a variety of computer systems, and is presently engaged in application studies of content addressable memories and research in machine-independent languages. He holds AB and MA degrees in physics from U. of Cal and Columbia.

*The term *logand* denotes the machine's basic instruction. It is used to avoid confusion with the term *instruction* which denotes an interpretive operation implemented through a sequence of stored logands.

P: Accumulator extension
T: I/O register;
(3) a 15-bit parallel full adder with carry indicator and overflow indicator;
(4) a 15-bit parallel half adder for address incrementing; and
(5) an input/output unit for I/O channel selection and data transfer control.

Computer operation is synchronous, with a clock rate of 1 megacycle. The basic logand cycle consists of four clock pulses, two for reading and restoring a 15-bit logand, and two for reading and restoring (or clearing and writing) a 15-bit operand. The same clock pulses are used to control inter-register transfers.

For indirect addressing, a six-clock pulse cycle is provided. The first two and last two are used as above, while the middle two are used to obtain the operand address from memory. Longer cycles are provided for certain iterated operations, such as shifting, multiplying, and dividing. Multiplication, for example, requires a fixed overhead of four clock pulses and an additional clock pulse for each multiplier bit. A 15-bit multiplication thus requires $4 + (1 \times 15) = 19$ microseconds.

logand formats

Programmed control of the TRW-133 is accomplished through sequences of 15-bit logands stored in memory. Logands fall into two classes: regular and special.

Regular logands (Fig. 2) contain a three-bit address option which specifies (a) whether addressing is to be direct or indirect (i.e., whether a four- or six-clock cycle is to be used); and (b) one of four sources of an address: the A register, the P register, the L register, or the M register. The A and P options permit addresses to be developed in the respective registers (e.g., through incrementing or addition operations) for use as direct or indirect addresses. In the L option, the low order six bits of the L register are used to directly address any one of the first 64 words of memory (the "scratchpad"), or to address any word in memory whose address is in scratchpad. Since the L register holds the logand when these memory operations are performed, the L option provides the equivalent of a conventional one-address instruction. When the M option is used, the M register contains the address of the next word in the logand sequence at the time operand access is made. This word may thus be used as an operand, or as the address of any word in memory, thus providing the analogy to "immediate" addressing and "direct" addressing, respectively, in a conventional one-address computer.

In the A, P, and M addressing options, the low-order six bits of the logand are used for a two-bit control option and a four-bit secondary command. The control option is used to enable or inhibit operand access, and independently to enable or inhibit the incrementing of the operand address. The secondary command has a function similar to the primary command (see below).

The address option, control option, and type of primary command (load or store) in regular logands specify one of 52 different sets of "implicit" microcommands to be carried out in the logand cycle. The specific primary command (one of 32) and, if it exists, the secondary command (one of 16) specify additional "explicit" microcommands to be performed on the next-to-last and last clock, respectively, of the cycle. The number of different regular logands possible is therefore quite large (~12,000), although not all of them are legal, functionally distinct, or particularly useful.

Fig. 3 illustrates the cycle resulting from the logand with primary command LA ("load A"), address option DA ("direct A"), control option C ("access and count"), and secondary command LT ("load T"). On clock 1, the implicit microcommand *wrm* (write under M control) regenerates the logand read into E on the last clock of the previous cycle. On clock 2, the implicit microcommand *amipa* simultaneously transfers the contents of A to M; the contents of M, incremented by 1, to P; and

Fig. 2

Regular Logands

15–10	9–7	6–5	4–1
Primary Command	Address Option	Control Option	Secondary Command

15–10	9–7	6–1
Primary Command	Address Option	Scratchpad Address

Special Logands

15–10	9–1
Primary Command	Parameters

Fig. 3

Clock	Microcommands: Implicit	Microcommands: Explicit	L	E	A	P	M	T	Memory
1	wrm		l	e	a	p	m	t	e→(m)
2	amipa, el, rdm		e	(a)	p	m+1	a	t	o→(a)
3	wrm	ea	e	(a)	(a)	m+1	a	t	(a)→(a)
4	pmip, el, rdm	et	(a)	(m+1)	(a)	a+1	m+1	(a)	o→(m+1)

(Columns L through Memory: Register and Memory After Clock) the contents of P to A. Also on clock 2, the contents of E are transferred to L (*el*), and a memory read cycle is initiated *(rdm)*. The remaining microcommands are similarly interpreted.

The special logands (Fig. 2) provide for such operations as branching and skipping, shifting, multiplication, division, input/output, and interrupt control. These logands are termed special because their cycles are, in general, peculiar to the specific special primary command (one of 22).

The format of operands is optional with the user. The full adder uses 2's-complement logic, so numeric quantities are most conveniently expressed in this form. A carry indicator holds the carry from the high-order adder stage, and a separate overflow indicator holds indication of overflow in adding signed numbers. Four different add commands are provided to control the input of the carry indicator to the low-order adder stage and the setting of the overflow indicator, thus facilitating multiple-precision arithmetic.

interpretive operation

In the interpretive mode of operation, control of the TRW-133 computer is vested in a set of machine-language routines called *lograms**. Each logram is a sequence of logands, and in general performs the function of a conventional machine instruction. Lograms may be stored anywhere in memory, and comprise the computer's "stored logic."

An interpretive program, in turn, is composed of a set of *logram calling sequences*. A logram calling sequence consists of one or more consecutive words, the first of which is always the address of the first word of the corresponding logram, and the remainder of which are the parameters (operands, addresses, etc.) on which the logram is to operate. For example, a logram which moves the contents of one memory location into another location might be "called" with the sequence

Y: MVE
Y+1: G
Y+2: H

where MVE is the (symbolic) address of the first word of the logram, G and H are the (symbolic) addresses of the source and destination memory locations, respectively; and Y, Y+1, and Y+2 are the addresses of the words in the calling sequence itself. Aside from the first word, there is no restriction on the length or format of a calling sequence. If desired, for example, two or more parameters may be "packed" into a single calling sequence word, though in the interest of speed this is not usually done. For interpretive operation, the choice of a 15-bit computer word is a felicitous one, since 15 bits are required to address any location in the largest (32K) memory provided.

In a conventional interpreter, the pseudo-instructions of the program are interpreted by a central control routine, which passes control to and receives control from individual subroutines. In TRW-133 interpretive operation there is no central control routine; instead, each logram is designed to perform whatever interpretation of the calling sequences is necessary, and to pass control directly to the next logram. By convention, lograms use the P register as an "instruction counter," i.e., to hold the address of the calling sequence word currently being manipulated. A logram steps the instruction counter forward as required in performing its function, and when finished executes a single logand which transfers control to the next logram (whose address is the first word of the next calling sequence) and leaves P set to the address of the second word of the next calling sequence. The next logram is thus in position to continue interpretive operation.

The logram corresponding to the MVE instruction cited above might be written as follows:

Registers and Memory After Logand Execution

Location	Logand	L	A	P	M	T	Memory
(From previous logram)		—	—	Y+1	MVE	—	
MVE	LA/DP/C/NO	G	G	Y+2	MVE+1	—	
	NO/DA/C/LT	(G)	Y+2	G+1	MVE+2	(G)	
	ST/LA/C/NO	(G)	H+1	Y+3	MVE+3	(G)	(G)→(H)
	LP/DP/C/NO	—	—	Y+4	(Y+3)	—	

Of particular importance to interpretive operation is the automatic incrementing of certain registers when they are used as address sources. For example, the first logand above brings the address G from the calling sequence into the A register and at the same time increments the "instruction counter" in P. Similarly, the second logand brings the number to be moved, (G), into L and at the same time increments its address. This is of no value in the present problem but would be of significant value if (G) were the first word of a multiple-precision operand. These and similar features contribute to the efficiency of interpretive operation on the TRW-133.

Using the above techniques, a sizeable number of lograms have been written for TRW stored logic computers. A basic set is furnished with the computer, consisting of fairly conventional one-address instructions for operations on single- and double-precision fixed point operands. This set uses certain scratchpad locations as a "pseudo-accumulator" and a "pseudo-multiplier-quotient" register. Another set exists for operating on floating point numbers with a two-word mantissa and a one-word exponent. Lograms are frequently written which call on other lograms; for example, floating point function lograms make use of the floating point arithmetic lograms. Typical logram execution times on the TRW-133 are: double precision fixed point addition, 38 microseconds; double precision floating point addition, 133 microseconds; and double precision floating point sine, 2,048 microseconds.

With the interpretive mode of operation, there is virtually no limit to the number of different instruction sets which may be postulated by the user. By selecting those sets most appropriate to his needs, the user may develop programs in a language which is natural and easy to use, yet without necessarily losing control of the detailed aspects of computer operation. Because it makes explicit provision for the interpretive mode of operation, the TRW-133 affords this type of user convenience in a manner which is both practical and efficient. ■

*The term *logram* is used to avoid confusion with the term *subroutine*, which signifies a set of interpretive instructions.

THE PB 440 COMPUTER

by E. O. BOUTWELL, Jr.

The design of the PB 440 anticipated two principal applications: 1) As a control and arithmetic element in real-time systems; and, 2) As a high-performance calculator for general scientific and engineering computations.

In the first role, the ability to perform basic data handling and manipulative operations at the micro-order level makes it well suited to real-time processing of information being collected or "played back" at word rates in excess of 50 KC. Typical manipulations performed in such applications include alarm limit checking, code translation, data compression, conversion to engineering units, etc. The rapid stored logic determination of interrupt priorities and required responses, as well as the implicit ability to design special purpose I/O macro-instructions, further enhances its utility as a control element in systems applications.

In its second principal role, as a general scientific and engineering computer, the PB 440 demonstrates three capabilities. Efficient *compiling* results from the use of a macro-instruction set that provides data inspection and decision abilities along with character string processing. The provision of micro-orders to manipulate data word fields that correspond to an implied *floating point* format, speeds the execution of this commonly used class of computational instructions. Finally, the opportunity to avoid the execution of superfluous operations, which are the inevitable result of preparing subroutines of conventional instructions, improves the performance of macro-instructions for the relatively more complex *transcendental and matrix functions*.

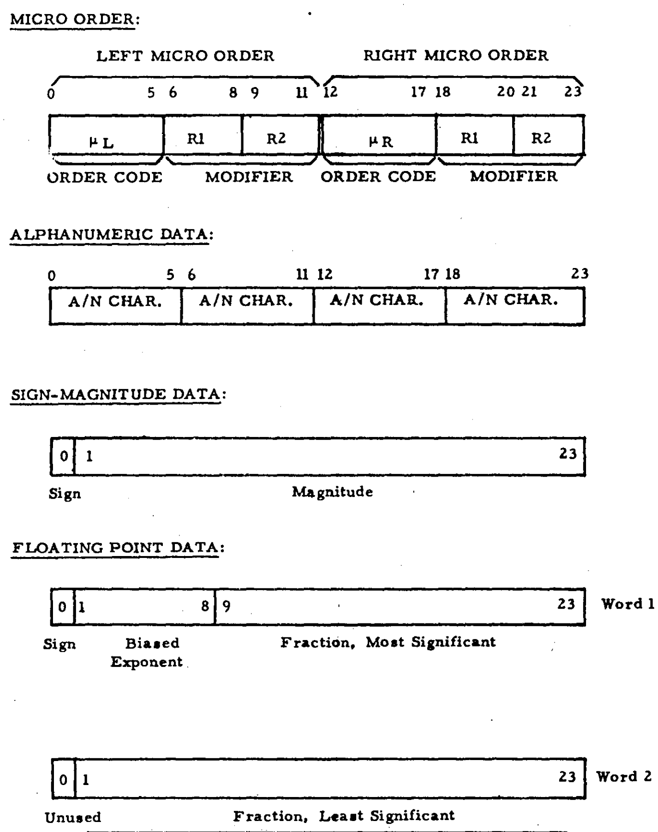
basic word formats

As a microprogrammed computer, the PB 440 does not have an instruction word format or a set of instructions in the sense that conventional computers have. Instead, its basic design provides the programmer with the option of describing, in terms of elementary "micro-orders," a sequence of steps which define an instruction. In much the same way that a logical designer would implement an instruction in a more conventional computer, the PB 440 programmer may implement an arbitrary function by specifying an appropriate time sequence of basic logical operations. This instruction set logic is normally stored in a fast access "control" memory although micro-orders can also be executed from main memory.

A maximum of 64 distinct micro-order types are decoded by the PB 440 control unit for manipulative and control purposes. In addition to an identifying six-bit micro-order code, a six-bit modifier field is contained in each micro-order. This basic format is illustrated in Fig. 1, where two micro-orders are shown occupying a 24-bit memory word. The modifier fields have been further divided into two three-bit fields designated R1 and R2. Although the composite six-bit field has a different significance for some micro-orders, generally, the R1 and R2 octal digits each refer to one of seven hardware registers whose contents may be manipulated in a manner specified by the associated micro-code.

The ability to perform logical manipulations on the contents of selected registers permits operations to be conducted on data whose length and number form are determined by the programmer. It was recognized, however, that the execution times resulting from the use of such general capabilities can be improved upon for one or more common types of data formats, if special micro-orders tailored to these formats are included in the design. Character manipulation and arithmetic operations on

Fig. 1



Joining Packard Bell Computer as manager of Advanced Systems, Mr. Boutwell is presently technical assistant to the director of engineering of the Anaheim, Calif., firm. He participates in preliminary hardware design and product planning. He has also been associated with Philco's Aeronutronic Div. and NCR's Electronic Div. as a system and logic designer and digital development engineer. He received his BS in engineering from UCLA, where he now conducts graduate courses.

Fig. 2 PB 440 MICRO ORDER TYPES

GENERAL MANIPULATIVE	
CPL, CPM, CPS, CPX	Copy Logical, Magnitude, Sign, Exponent
CCL, CCM, CCS, CCX	Copy and Complement Logical, Magnitude, Sign, Exponent.
CIL, CIX, CDL	Copy and Increment Logical, Exponent, Copy and Decrement Logical
AND, LOR, XOR, EXC	Logical Product, Logical Sum, Exclusive OR, Exchange
SHIFT	
SSL, SDL	Shift Single Length, Double Length
SLS, SLC, SFR	Shift Left Six, Shift Left and Count, Shift Fraction Right
ARITHMETIC	
ADL, ADM, ADS, ADX, ADF	Add Logical, Magnitude, Sign, Exponent, Fraction
AMK, AFK	Add Magnitude, Fraction with carry in
MPS, DVS	Multiply-Step, Divide-Step
MEMORY OPERATIONS	
LDM, STM	Load from Memory, Store into Memory
LDI, STI	Load, Store and Increment Address
LDW, STW	Load from Working Storage, Store into Working Storage
LDS	Load from Memory, special addressing
SKIP AND JUMP	
TZO, TNZ	Test specified register field for zero, non-zero
TCT, TCF	Test specified condition for true, false
CLP, FTR, BTR	Copy Literal address to P, Forward, Backward Transfer Relative

signed numbers and floating point numbers are three cases which occur so frequently that this type of special treatment is in order. The data formats illustrated in Fig. 1 were selected for these purposes, and it will be noted during an examination of the micro-order repertoire (Fig. 2), that operations on data expressed in one of these formats have been facilitated.

As a comment on the basic nature of the micro-order repertoire, all non-repetitive micro-orders require a single clock time for their execution. That is, at a 1 MC clock rate, a binary addition of two 24-bit registers is accomplished in one microsecond with the result replacing one of the operands.

logical structure

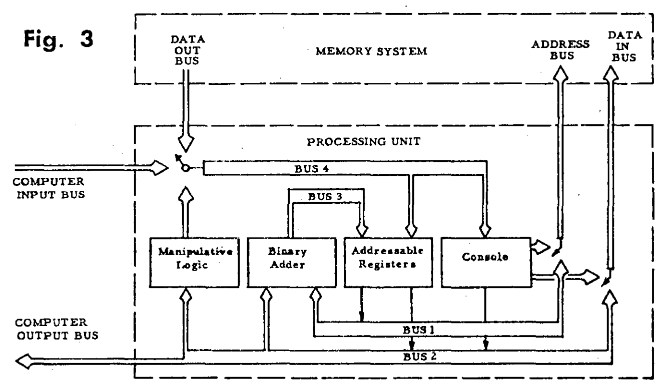
The processing unit consists of four 24-bit registers (A, B, C, D), two 15-bit registers (L, P), and a single 8-bit register (N).[1] For purposes of register transfers and other manipulations, L and P are logically aligned with the "fraction" field of the 24-bit registers (Fig. 1, Floating Point Format) and N, with the "exponent" field. In addition to their general programmed use, two registers have fixed roles in internal operations:

1) The P-register serves as the micro-program counter, being incremented automatically and submitting its contents as a memory address during each micro-order-pair access cycle.
2) The N-register serves as the repeat counter for timing shift operations, and multiply-step and divide-step micro-orders.

It will be noted that the L-register, being of maximum address length can be used to good effect as a macro-instruction location counter.

The Processing Unit Block Diagram, Fig. 3, illustrates the manner in which the addressable registers of the computer may be connected to a binary full adder and other manipulative logic by use of the processing unit bus structure. Under the control of decoded micro-orders, the registers may be selectively gated onto the logic input busses (1 and 2), the desired manipulative logic enabled, and the result gated from the appropriate logic output bus (3 or 4) into the desired register. Thus, the addition of the contents of registers A and B may be accomplished by logically connecting A to bus 1, B to bus 2, enabling the full add logic and connecting bus 3 (carrying the binary sum) to the input logic of register B. Similarly, the 1's complement of the contents of register L may be obtained by connecting the outputs of L to bus 2, selecting the inversion logic input to bus 4, and connecting bus 4 to the register L input logic. Data transfers and register exchanges are facilitated by a direct connection between busses 2 and 4 and by the ability to disable the bus 2 input to the full add logic.

Fig. 3



Not indicated on Fig. 3, but important to an understanding of computer operation, is the logic for several other processing unit functions. These include:

1) A variation on the binary addition logic which permit data on bus 1 to be incremented or decremented;
2) Logic to increment the contents of the P-register (program counter);
3) Logic to decrement the contents of the N-register

[1] Boutwell, E. and E. Hoskinson, "The Logical Organization of the PB 440 Microprogrammable Computer", Proc. F.J.C.C., Nov. 1963, p. 201-213.

(repeat counter);

4) Double length shifting logic on registers A and B; and,

5) The logic for applying a variety of tests to the data being transmitted over the general bus structure.

It should be noted on Fig. 3 that buses 1, 2, and 4 and their associated gating logic also provide the means for communication with the memory system, the input/output devices, and the operator's console. During the execution of a micro-order requiring memory operation, for example, the register designated for supplying the address will be gated onto bus 1, and bus 1 will be selected as the input to the memory address bus. For a memory "read" operation, the contents of the memory data output bus will be gated onto bus 4 and thence to the selected destination register. For a memory "write" operation, the data source register will be selected as an input to bus 2 which, in turn, will supply the memory data input bus.

During an input operation, bus 4 may be connected to the computer input bus which carries both data and status information from external devices. Similarly, data and control information may be gated from the register designated by an output micro-order to an external device via bus 2 and the computer output bus.

Access to the memory system and the addressable registers of the processing unit, from the operator's console, may be accomplished efficiently by making use of existing bus structure logic. Bus 4 may be monitored as a common point for displaying both memory data and register contents. Manual memory interrogations may be conducted from the console by supplying address data as an input to the memory address bus and by selecting the memory data out bus as an input to bus 4. For storage operations, data from a "register" of switches at the console may be gated onto bus 2 and thence to the memory data input bus. The contents of processing unit registers may be displayed by use of bus 2 and the direct input to bus 4. The same logical path may be used to alter the contents of a specified register by selecting the console data switches as an input to bus 2, and bus 4 as an input to the designated register.

The bus type memory communication, depicted in Fig. 3, facilitates the modular expansion of the memory system to a maximum of eight 4,096-word modules without altering the logic of the basic design. Memory control logic which treats each module as a separate asynchronous device accommodates modules of different access and cycle times. This feature is important to the microprogramming concept employed in the PB 440. It permits the combined use of a fast, non-destructively read memory unit (1 microsecond access) containing microprogrammed stored-logic, and a larger capacity core memory (5 microsecond cycle) containing macro-instructions, operands, and constants.

The independent control of individual modules permits several accesses to the fast memory, and the continued execution of the micro-program, during the rewrite (restore) portion of each main memory cycle. The memory output is directed to the micro-order decoding register at the time in each computer cycle when the next micro-order-pair is to be presented to the control circuitry. These micro-orders are executed in succession at a 1 MC rate. During the execution of the right-hand micro-order, an access is again made to the logic memory for the following micro-order pair, etc.

interpretive operation

It was noted above that the microprogramming facility permits PB 440 programmers to specify a sequence of steps which define an instruction. For clarity, we might refer to an instruction described in this way as a "macro-instruction." A complete macro-instruction set (many are possible) consists of a "control" sequence of micro-orders, to interpret or decode macro-instructions, and a set of "function" sequences. Each function sequence describes the data manipulations required to implement a corresponding macro-instruction.

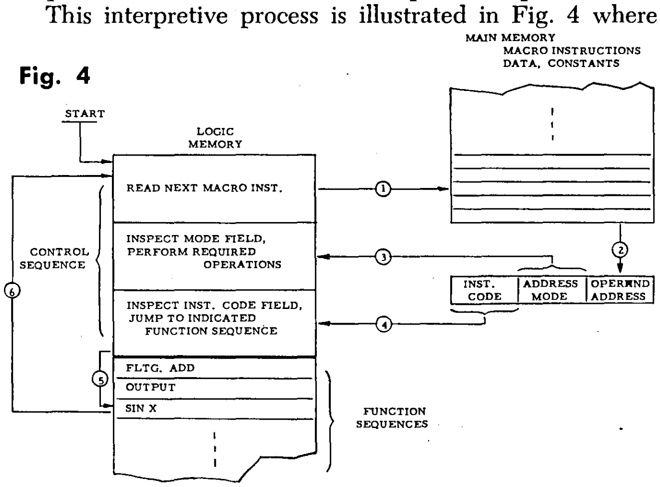
The design of an instruction set thus consists of three tasks. First a macro-instruction format is chosen. This format need not be restricted to a word length of 24 bits, nor to single address instruction; it may, in fact, be a format used by another computer. Indexing, indirect and relative addressing, and other special functions may be included.

A control or interpretive sequence of micro-orders is next devised which fetches and identifies successive macro-instructions, performs indicated address modifications and obtains operands as required.

Lastly, the function sequences, each defining an instruction, are written. Here the programmer-designer reduces an instruction to its basic logical ingredients and, thus, mechanizes each operation he wishes to include in the instruction set. The last micro-order of each function sequence returns control to the interpretive sequence.

This interpretive process is illustrated in Fig. 4 where

Fig. 4



the successive phases in the execution cycle of a typical macro-instruction are enumerated.

It should be noted that the amount of time required to interpret a macro-instruction should be kept as short as possible since it must be added to the "execution" time of each macro-instruction. It may vary from less than five microseconds, for a relatively simple format, to more than 25 microseconds, where indirect addressing, indexing, and other mode indicators must all be satisfied.

To offset this interpretive "overhead," a distinct advantage appears in the mechanization of the relatively more complex functions which are usually offered as subroutines on conventional computers. As a performance indication, a microprogrammed, Arctangent sequence requires approximately 200 microseconds, or about one-fifth the sub-routine time on a fast conventional computer.

A "library" of macro-operations, programmed as micro-order sequences, has been expressed in several useful macro-instruction formats. To the user of these instruction sets, the microprogrammable feature means a larger and more varied instruction repertoire and generally improved performance. The "micro-programmer" benefits further from the ability to modify and extend the instructions which have been micro-programmed previously, and he is challenged to optimize critical applications by creative programming at the micro-order level. ■

THE C-8401 DATA PROCESSOR

by L. BECK and F. KEELER

The Collins Radio Company C-8401 Data Processor is a stored program, intermediate scale digital computer with the following characteristics:

a. The C-8401 is flexibly implemented from a basic group of equipments plus a selection of exchange registers. The basic group of equipments consist of a main memory, a transfer link and an instruction memory. The internal and external exchange registers connect the operating equipments to the transfer link. Examples of these operating equipments are arithmetic units, magnetic tape systems, TTY equipments, etc. By appropriate selection from the catalog of exchange registers the C-8401 can be tailored to fit different applications.
b. The C-8401 is a microprogrammed data processor having two memories. The micro-programs are stored in the instruction memory and can be selected to meet the characteristics of specific applications. The main memory stores macro-program instructions for the particular application.
c. The C-8401 is communications oriented. It can communicate directly with several other computers by means of data transmission systems which are

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Formerly with Collins Radio in Newport Beach, Mr. Keeler is a member of the Technical Staff of Systems Programming Corp., Santa Ana, Calif. He has been engaged for more than seven years in digital equipment system design and analysis, programming, logical design, and hardware fabrication. He holds a BA in math from Long Beach State College in California.

treated as peripheral equipments. The C-8401 performs this communication function simultaneously with other data processing functions, and is designed to directly process up to 256 bit serial communication equipments (dependent on traffic load) without hardware buffering to assemble characters or messages.

To understand how the C-8401 realizes these features, consider the generalized C-8401 block diagram indicated in Fig. 1. This shows a main memory with its associated address (S) and data (Z) registers, internal and external exchange registers, a transfer link and an instruction memory with its associated address (U) and data (T) registers.

The transfer link provides complete freedom of data transfer between all equipments associated with the C-8401. The outputs of all exchange registers are fed into the INPUT MATRIX. (The registers of the two memories are treated as exchange registers in this sense.) The INPUT DECODER selects one of the exchange registers and enters its information on the COMMON BUS. Each of the exchange registers is also connected to the OUTPUT MATRIX. The OUTPUT DECODER selects one of the exchange registers and distributes the information from the COMMON BUS to the selected exchange register. Thus, the transfer of information between any of the registers is accomplished. The transfer link is capable of completing three of these transfers per microsecond.

Certain internal exchange registers have associated hardware that perform logic operations, e.g., complement, binary add, exclusive OR, rotate, zero test and parity. Other internal exchange registers perform no special basic operation and can be used for fast storage. Other logic operations are made by combinations of these basic operations, e.g., inclusive OR, mask, branch, etc. Each of the basic operations is associated with a unique exchange register. By sequencing transfers between the appropriate internal exchange registers, any program function may be implemented.

These transfers are arranged in particular sequences to accomplish the required computational functions. The lists of these transfer sequences (micro-instructions) are stored in the instruction memory. The instruction memory is a 1,024-word, 36-bit, non-destructive device. The read cycle time of the instruction memory is one microsecond. Each 36-bit data word is interpreted to control three transfers. Fig. 2 indicates the two formats of the instruction memory word. New micro-programs may be entered into the instruction memory under operator control. The instruction memory is sequentially addressed unless the address (U) register is modified by data entered into it from the transfer link.

Fig. 2

FORMAT I

Transfer A		Transfer B		Transfer C		Controls	
Source	Dest.	Source	Dest.	Source	Dest.		
5	5	5	5	5	5	6	Bits

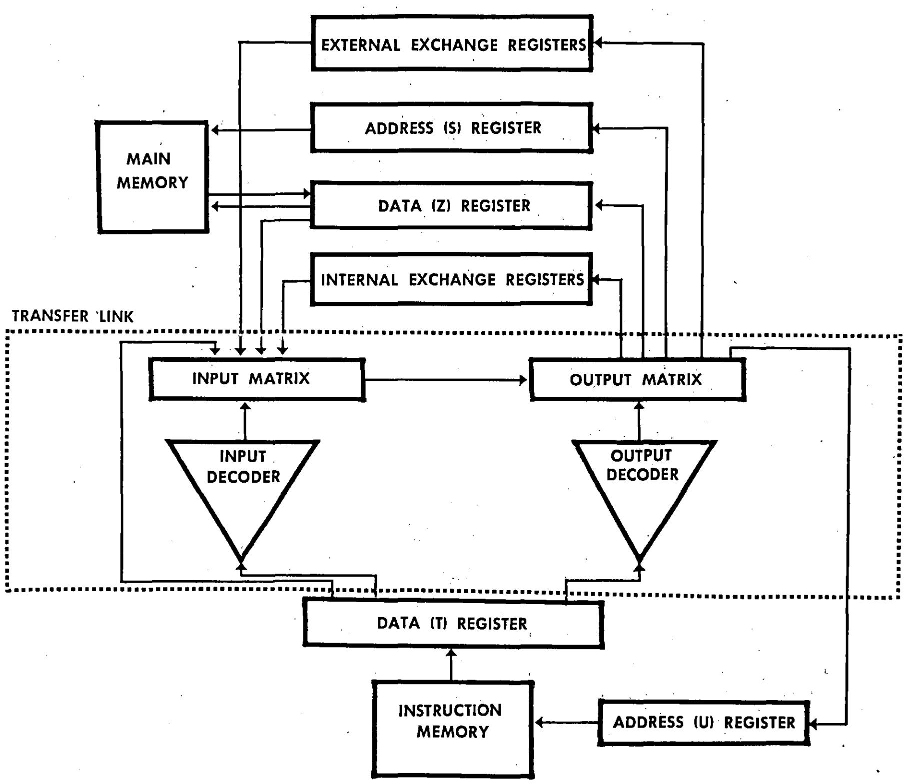
FORMAT II

Transfer A		Transfer B		Constant	
Source	Dest.	Source	Dest.		
5	5	5	5	16	Bits

The main memory is also connected to the transfer link. The basic memory block is a 4,096-word, 16-bit, 5-microsecond cycle time coincident current device. It is expandable in blocks of 4,096 words up to a maximum of 65,536 words. Fifteen micro-instructions can be performed during each main memory cycle time. The main memory contains the macro-instructions normally associated with a stored program device.

An important feature of the C-8401 processor is its

Fig. 1



ability to simultaneously control a number of input/output operations concurrent with performing its data processing function. Up to 21 external exchange registers may be implemented in the C-8401. The C-8401 services these peripheral devices on a demand basis and periodically interrogates the peripheral devices to determine if one of them requires attention. When a peripheral device requires attention, the main data processing program is temporarily interrupted while the input/output device is serviced. The number of such equipments that can be simultaneously operated is determined by the basic speed of the C-8401. Thus, the C-8401 has been designed to control a large number of communication devices.

interpretive operation

The two-memory concept employed in the C-8401 design provides the programmer with the capability for deriving any type of problem-oriented programming language which is particularly suited to a specific application. The micro and macro-programs are related in the same sense as the two levels of programs of a classic interpretive programming system.

The main memory contains the macro-programs written in a problem-oriented language and stored with associated data. The instruction memory contains a set of micro-programs to perform the tasks required by the instruction repertoire of the selected language. In addition to these micro-programs, a read next instruction (RNI) micro-program is required to access each individual macro-program instruction (consisting of from one to *n* words) from main memory and to transfer control by branching to the particular micro-program associated with the accessed instruction. Each micro-program associated with instruction execution returns control to RNI when its task is completed. In order to access successive macro-program instruction words, RNI controls an instruction address counter which is stored in a utility register (one of the internal exchange registers). This counter is transferred from the utility register to the S register via the transfer link under control of an RNI micro-instruction. After the main memory read cycle is completed, the Z register contains the contents of the addressed main memory instruction word. By successive accesses of main memory and by manipulation of the contents of the Z register through the internal exchange registers, via the micro-instructions as described above, the RNI micro-program is able to determine which instruction of the repertoire was accessed and provide branching in the instruction memory to the micro-program associated with the accessed instruction. The RNI micro-program accomplishes the branching by directing a new instruction memory address to the U address register via the transfer link from an internal exchange register or from the constant field of the instruction memory data (T) register.

The selected micro-program in turn uses the instruction word (which has been stored in a utility register) and the main memory operand address(es) to access the main memory operand(s), performs the required function on or with the operand(s) by selecting successive data transfers through the internal exchange registers, and restore the operand(s) to main memory. Any desired data transfer within the processor may be controlled by a set of micro-program instructions stored in the instruction memory. Between the completion of the main memory read cycle and the automatic initiation of the write cycle 1⅓ microsecond is available to the micro-program during which time the accessed operand word may be obtained from the Z register, modified, and restored to the Z register. Any part of the main memory read/write cycle time may be utilized by the micro-program to perform micro-instructions as long as the contents of S and Z are not disturbed except as allowed.

Both the macro and micro-programs may be conveniently loaded under operator or program control. Special operations may be programmed at the micro-level to efficiently meet the requirements of any specific application. Also, the processor may be adapted to changing system requirements through simple micro-program alterations without costly and time-consuming wiring changes. Concurrent operation of multiple programs is also possible using an RNI micro-program which accesses instructions from multiple programs stored in main memory.

Processor input and output control is provided by separate micro-programs. These programs control the input/output equipment operation and are selected by the RNI micro-program as specific input/output functions are requested by the macro-program instructions. The operation of a specific input/output device and its adaptive equipment is controlled by the micro-program for that device. After initiation of the input/output device function, the micro-program returns control to RNI which in turn is capable of accessing further macro-program instructions and branching to the required functional micro-programs. RNI must periodically initiate re-entry to the previously selected input/output micro-programs for input/output device service until the requested input/output functions are completed. Individual macro-program instruction execution is delayed momentarily while a data character is read from or written to an input/output device requesting service, or control information is sent to or received from the device adapter.

communication application

One of the major advantages of the C-8401 is its adaptability to communication network applications. For teletype message switching applications, an additional micro-program (teletype op code) exists in the instruction memory to control bit serial teletype transmission and reception. All functions involved in line scanning, input TTY character assembly, character termination and audit, output character initiation, distribution and audit are performed by this micro-program and are accomplished independently of the macro-programs stored in main memory. The only effect upon the main memory macro-programs is the periodic interruption of macro-instruction execution during intervals of teletype op code activity. The teletype op code utilizes the three million exchange register interchanges per second rate rather than the slower macro-program instruction execution rate to significantly reduce processor hardware, time and main memory storage requirements. The teletype op code is periodically entered from RNI on the basis of processor clock time, and return is made to RNI from the teletype op code. The teletype op code is not controlled by a macro-program instruction, and concurrent teletype input/output activity and macro-program instruction execution are effectively achieved.

operation times

Most micro-operations are executed in one-third of a microsecond. A few micro-operations (e.g., binary addition) require two-thirds of a microsecond. Macro-instruction execution times are directly dependent upon the number of main memory accesses required for macro-instruction and operand address as well as the organization of the micro-instructions in the instruction memory. In programming these micro-instructions, the objective is to interpret and complete the indicated macro-operation within the time required for accessing the macro-instruction. Collins Radio Co. has designed and utilized both single and four address macro-programming languages for communications and data processing applications. ■

STORED LOGIC PROGRAMING AND APPLICATIONS

by RICHARD H. HILL

Early in the development of the microprogramming/stored logic concept, some proponents of this unique design approach attributed to it virtues beyond realization. In that first flush of enthusiasm it was claimed to be everything from the most efficient possible general purpose computer to the perfect tool for simulating directly (at the machine language level) any computer in existence.

Cooler heads quickly discounted these trumpetings. Envious competitors began the leveling process of detraction. By now enough experience has been gained to permit some reasonable evaluation of the contribution of stored logic to computer design. This article makes an effort to do this from the viewpoint of programming and applications.

As Lowell Amdahl points out (p. 26), "The advantages and disadvantages of microprogramming/stored logic are often difficult to weigh." This statement applies with particular force in considering programming for stored logic computers and in attempting to discover applications especially suited to the stored logic computers. In the last analysis stored logic computers are neither more nor less "programmable" than other general purpose computers. Further, the suitability of a given computer for a given application is usually determined on other bases than its internal organization.

The initial attraction to stored logic as a design concept was the presumed twofold advantage of programming flexibility (and hence application flexibility) with lowered component count. Flexibility in this sense means the ability to fashion an instruction set appropriate to a given type of problem. These design objectives have not changed materially in the TRW-133 or the PB 440, though the Collins 8401 appears to represent an effort in which programming flexibility is of less importance than the ability to create tightly-tailored programs.

There are two independent considerations of importance in examining present-day stored logic computers. First, how well have these design objectives been realized? And second, how important are these design objectives when considered in the light of other new, more conventionally

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organized machines and of realistic applications requirements?

stored logic implementations

There is some evidence for the viewpoint that the stored logic approach does provide programming flexibility as previously defined. Both the TRW-133 (and its cousins, the TRW-130, TRW-131 and TRW-530) and the PB 440 have extensive coding facilities provided by large repertoires of microprogrammed instructions. The breadth of the repertoire is perhaps illustrated best by the instruction library of the TRW-530, which contained between 250 and 300 microprograms early in its development. The TRW-530 library includes binary and decimal arithmetic and logical operations, each with one-, two- or three-address formats and single-, double-, and triple-length, operand options. Although basically a fixed-word binary computer (18-bit word length), the 530 can, by judicious selection of available instruction options, be programmed entirely as if it were either a character machine like the IBM 1401, or a fixed word length decimal machine like the IBM 7070. Similar treatment is possible in the TRW-133, although less conveniently because the word length (15 bits) does not contain either 4 or 6 as a factor.

Full floating point facility through software is characteristic of both the TRW-133 and the PB 440. If the two machines were compared, the PB 440 might be shown to be the superior in this area because of a greater number of internal formats and micro-commands designed particularly to facilitate floating point arithmetic. Both computers have the capability of implementing any desired type of logical instruction, including masked arithmetic or logical instructions where operations are performed on selected portions of the referenced data.

The Collins 8401 programming flexibility would seem to be limited only by the maximum number of exchange registers that can be used in a single processor, or possibly by the capacity of instruction memory. Theoretically, however, the Collins approach provides as much flexibility from the programming viewpoint as do the TRW and PB alternatives.

The answer, then, to the question "Do stored logic computers really provide flexible instruction sets?" is, emphatically, *yes*. But the answer is a qualified one. The qualification is that stored logic computers provide great flexibility *at the symbolic assembly language coding level.* By "symbolic assembly language" here is meant the usual one-for-one symbolic-to-machine code with which most programmers are familiar. To put the case somewhat differently, it might be said that a particular set of microprogrammed instructions for, say, the PB 440 describes a pseudomachine that actually works. The characteristics of this pseudomachine may be altered, if need be, by a simple change of programming, instead of changing circuit cards or redoing the back panel wiring.

It might be argued that it is more efficient to implement higher-level languages on stored logic computers than on other types of machines because special instructions can be written to facilitate coding language processors. Some small gain in efficiency may in fact have been realized in this way. But no breakthrough in implementation has yet evolved from stored logic itself comparable to, for example, writing a NELIAC processor in NELIAC language and bootstrapping the processor onto a new computer by hand-coding a few of the generators. Nor is there yet developed a technique comparable to the meta-assembly technique. By using the meta-assembler language to describe both source and object languages and the transformations required to go from one to the other, an assembly program can be generated very quickly. These things could be done on stored logic machines, of course. The significant aspect, however, is that these and similar techniques developed completely independently of stored logic, and there is no proof that the machine-language level flexibility of stored logic offers any great advantage over conventional computers in implementation of advanced programming techniques.

Flexibility in implementation of programming systems is only one aspect of programming flexibility. Another aspect is based on the notion that one computer may be called upon to perform efficiently in several different applications areas within a short span of time. For example, a computer used during a day shift for real-time processing of inventory data might be needed in other hours for scientific computation, report generation or a host of other uses. With a stored logic computer, the argument proceeds, each type of application program can be written in a language best adapted to it. Further, as Mr. Boutwell points out (p. 30), common functions can be optimized to a very high degree. In some real-time systems in particular time-critical program sequences may be fully optimized.

Granted that the stored logic computer can be quickly made to resemble the optimum computer and optimally for a given application area, it still remains that this configuration is at or near machine language level, which may not be useful in some instances. Thus from the purely external viewpoint stored logic loses its significance when a stored logic computer is called upon to compile and execute FORTRAN, COBOL, NELIAC, JOVIAL, etc. The stored logic machine appears identical to any number of others when used this way. The only measure the user can apply in these instances is that of relative efficiency as represented by cost factors. In particular the question of interest is "Can I compile and execute my FORTRAN program within time limit tolerances and at less cost on the stored logic computer or on computer X?" To date this question remains unanswered.

programming complexity

A frequently-voiced complaint against stored logic computers has been the relative complexity of coding at the microprogram level. There may be two or three commands available for execution each time the micro-instruction sequence is accessed. Typically the microprogrammer must concern himself with the mechanics of address-building (indexing, indirect addressing, etc.) as well as the mechanics of arithmetic (step-by-step multiplication and division, sign control in complement operations, etc.). At the same time he is faced with these concerns the microprogrammer is challenged to optimize his code completely, since each sequence will be executed so many times if he is writing microprograms.

Typically the manufacturers' programming staffs are the hardest hit by these considerations. Experience at both TRW Computer Division and Packard Bell seemed to indicate, however, that after an initial period of some frustration most programmers adapted readily to microprogramming and found it no more difficult than any other machine-oriented form of coding. In fact some TRW programmers ultimately preferred coding on the logand (microprogramming) level to using higher level languages. Apparently they felt better able to produce an optimal program at this level. Many of them developed considerable dexterity in logand level coding. Packard Bell reports comparable experience.

Users are generally less concerned with microprogramming, although it would seem reasonable to anticipate that each user organization would probably have on its staff at least one venturesome soul who would delve into the machine at the microprogram level. He would maintain the manufacturer-supplied system and would probably also contribute his own tailor-made procedures to the common pool. The remainder of users' staffs would most likely program entirely at higher language levels.

The very fact of flexibility introduces programming systems problems of great complexity. The ability to prepare new instructions virtually at will calls for effective procedures to control and maintain system libraries, which in turn requires strong and effective shop discipline. Stored logic computers require also a very heavy emphasis on preparing and maintaining adequate documentation. One can visualize the problem by considering what might happen just in documentation if instructions of some complexity were added to the IBM 7090 almost daily. (Installation supervisors must recognize that a given stored logic instruction can never be deleted from the library without the risk that some vital program will fail to operate without it). This problem is even more grave than "the system of private order codes" to which Wilkes referred (p. 26).

interpretive operation

It is apparent that the basic concept of stored logic relies on the technique of interpretive operation. The functions of interpretive control are simply stated:

1. Determine the entry point of the next instruction sequence to be executed.
2. Prepare the operand address(es) or any parameters required.
3. Transfer execution control to the instruction sequence.
4. Receive control from the instruction sequence and repeat.

With this set of specifications it is clear that a simple computer program can be written to do the job. Such a program would, in most instances, take more time to execute in proportion to the time spent in solving the problem than is desirable. To skirt this problem the stored logic computers described in this issue have been fitted with ingenious facilities for interpretive operation. Execution control between sequences rarely requires more than four main memory cycles and in most instances one or two cycles are sufficient. These achievements are possible because of the presence of special register operations and formats designed to facilitate the common types of instructions and data. From this viewpoint stored logic computers represent real *tours de force* of logical design.

Early potential customers for stored logic computers, recalling the agonizing slowness of some interpretive systems, saw this fact of interpretive operation as a severe drawback. In practice this has not proven to be so, although the cost of interpretive operation in terms of execution time and memory must be considered in any comparative analysis involving a stored logic computer.

If the interpretive mode is not used, and instead entire programs are prepared at the actual machine language level, then a stored logic computer becomes like any other. The most obvious difference lies in the closeness of the programmer to the "bits and pieces" manipulation of the computer. Sometimes he may take advantage of this closeness to tailor the processing exactly to the characteristics of the problem. However, elegant coding is much more directly related to the abilities of the programmer than to the capabilities of the machine. Stored logic has no corner on elegance.

applications for stored logic computers

No one has yet shown that stored logic computers are "best" for any given application area. After the first flush of interest and enthusiasm died away, the developers of stored logic computers found that they had put together general purpose devices directly competitive with more conventionally organized computers in any given application area. The stored logic machines have had to compete on the same bases of price, performance, reliability and manufacturer's support, as everyone else.

The pertinent factors in considering computers for a given task are still:

1. Will the processor do the job at all?
2. Is there reasonable room in time and memory for expansion?
3. Will the computer and peripherals meet environmental requirements?
4. Does the equipment have reasonable assurance of adequate reliability?
5. Is there adequate software support?

These are only the most obvious qualifying questions, designed to establish *feasibility* of considering a computer for a specific application. Detailed consideration will doubtless involve comparisons of various features among several computers, including estimates of operation and throughput times, comparative equipment costs, and many other factors.

In this type of analysis, machine organization (e.g., stored logic vs conventional) enters only indirectly. No one will buy a stored logic computer solely because it is a stored logic computer. Rather the incentive to buy must arise mainly from its ability to do the same job at lower cost, to do a better job at equal cost, or to provide higher reliability at comparable cost. The remaining possibility is that the stored logic computer will do several different jobs well, well enough at least that the overall performance for the mix of jobs will be better than any conventional computer's performance for the mix.

Interestingly, stored logic computers have not so far been *sold* on this latter basis, although they have been marketed using this approach. Applications of the TRW stored logic military computers have so far been highly systems-oriented, where the computer forms part of a large system and does only one particular task such as formatting radar data or compiling mapping data. The Collins 8401 is designed as a communications processor, with only incidental weight apparently given to other possible functions. The PB 440 possesses perhaps better general purpose capability than either the TRW or Collins computers, but is competing in an extremely rough market segment, the small-to-medium scale scientific computer area now dominated by the IBM 1620. Formidable competition also exists with CDC, SDS, ASI, Minneapolis-Honeywell and DEC.

One stored logic computer that has been sold on the basis of versatility is the TRW-530, a slightly redesigned commercial version of the TRW-130. The 530 will be used by TRW as a character-oriented business data processor in one mode, and as a fixed-word scientific computer in another mode. Both modes will be available in each installation; all U.S. installations so far are in-house at various TRW plants. Abroad, the 530 has been marketed widely and successfully in Europe and Japan. Most of these installations, however, are strictly process control applications, confirming the apparently small market for machines of such high degree of versatility.

conclusions

Since stored logic does offer some obvious advantages from a cost viewpoint, why has it not won wider acceptance as a design technique? The answer to this question may lie in an examination of the factors that go into pricing a commercial computer system. Manufacturing costs (labor, purchased parts and overhead) typically constitute only 35 per cent of the main frame selling price. The remainder represents marketing costs, software support, return on development costs, profits, etc. Only a small part of the manufacturing costs, perhaps 10 to 15 per cent, can be saved by application of stored logic. Further, in a typical small or medium scale system the cost of peripheral equipments (unaffected by stored logic) will equal or exceed the main frame costs. Thus manufacturing costs of the main frame, which are the only costs directly reduced by use of stored logic, form a very small part of the ultimate system selling price. These savings may be easily offset by increased costs of documentation or program library maintenance due to the stored logic principle being too freely employed. The upshot of these thoughts seems to be that most manufacturers have not found the stored logic technique sufficiently attractive from the cost-saving viewpoint to warrant changing directions.

Certainly the competitive impact of stored logic machines in any domestic market area except small-scale militarized computers has not been enough to bother any manufacturer of conventional computers. In the domestic commercial market other new design concepts have offered greater cost savings and made far more market impact.

In the military computer field it must be pointed out that the AN/UYK-1 (military nomenclature for the TRW-130) enjoyed its success at least as much because it was the first computer to meet a certain set of environmental requirements as because it employed stored logic. The latter may, of course, have contributed to successful packaging by keeping the component count down and thus reducing volume.

Ease or difficulty of programming has apparently had little effect on the sales of stored logic computers. Although a topic of discussion among programmers, the question of how difficult it is to code a given machine appears to have remarkably little influence on people who have authority to make decisions to buy. Availability of problem-oriented languages may be a factor in many instances, but programming considerations below this level rarely influence the vice-presidential types who sign on the dotted line.

At this juncture the future of stored logic as a design technique is somewhat cloudy. None of the major manufacturers (IBM, Univac, GE, CDC, RCA, Minneapolis-Honeywell) has evidenced interest in the technique although presumably all have examined it. When Univac undertook to compete with the stored logic AN/UYK-1 for the small military computer market, with the Univac 1218, they chose not to utilize the concept.

To summarize, the stored logic principle provides the programming flexibility and, to a lesser extent, the application flexibility that were its initial objectives. After an initial period of familiarization, programmers appear to find stored logic computers no more difficult to code in machine language than conventional computers. Installation supervisors, though, may encounter problems in maintaining the programming system and library.

Interpretive operation of stored logic computers offers no logical or operational problems, and is considerably more efficient than interpretive operation in conventional computers. Finally, the evaluation of computers for a given application or installation should depend upon the dispassionate comparative analysis of on-the-job capability and costs, without excessive regard for how the objectives are achieved. ■

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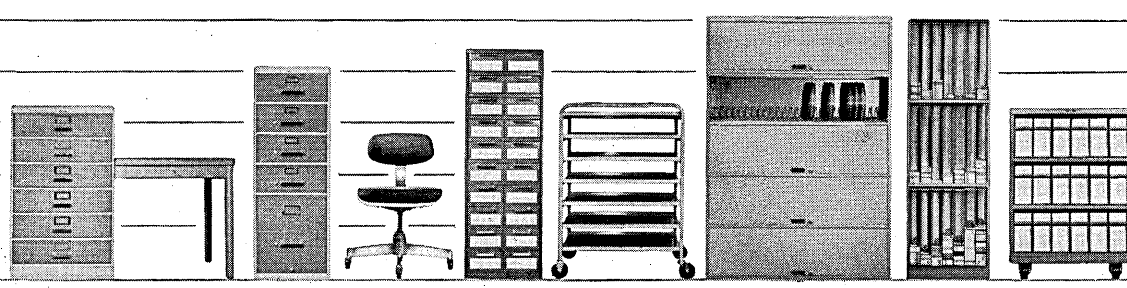

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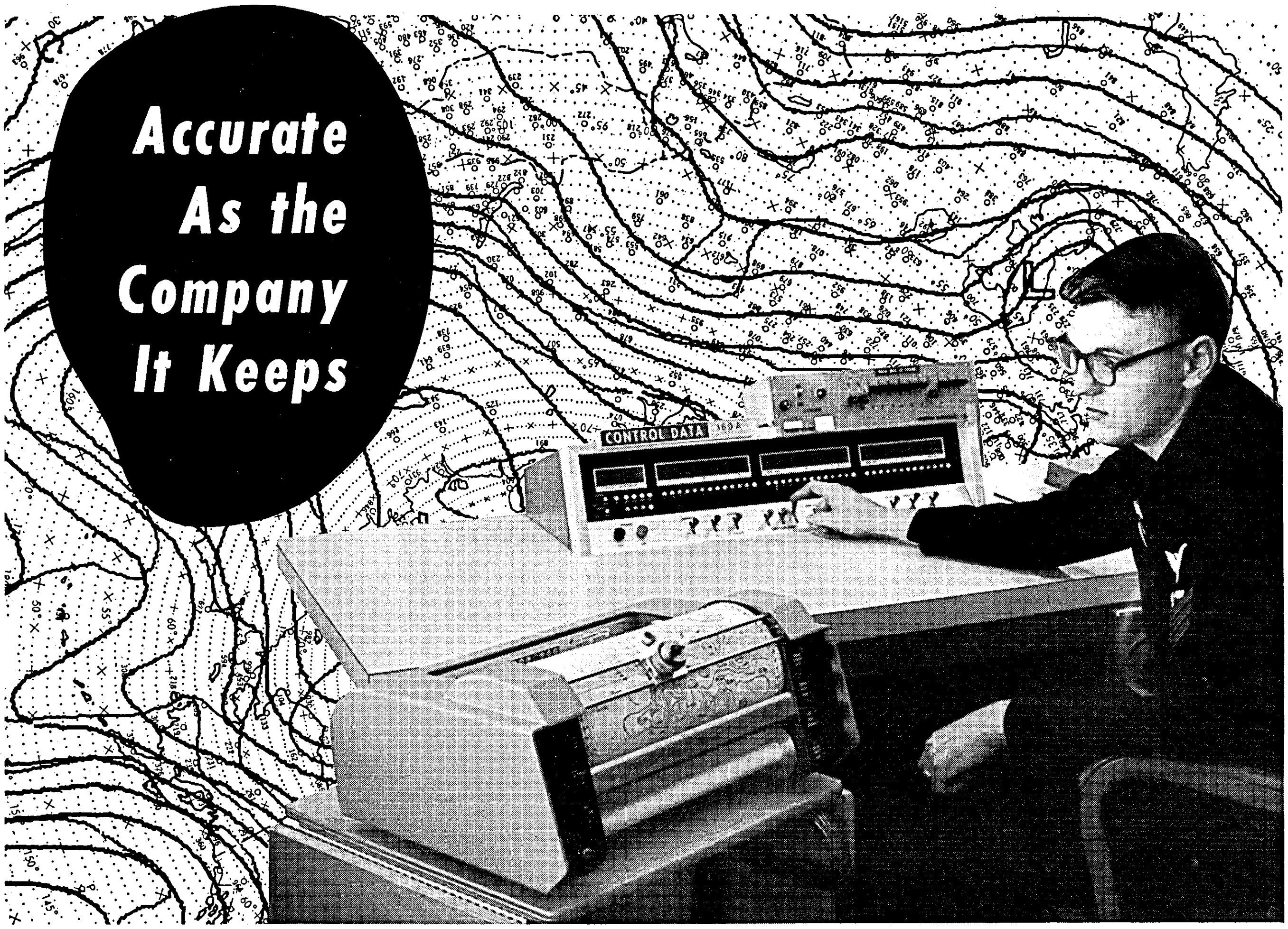

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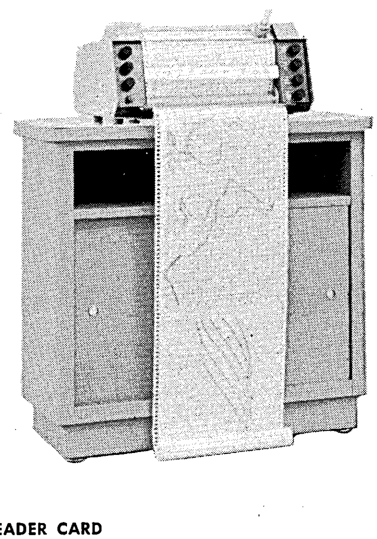

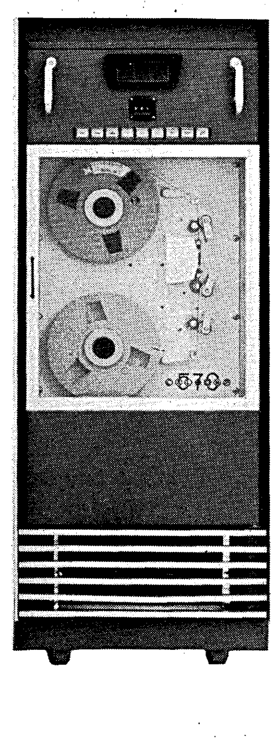

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USING DECISION STRUCTURE TABLES

part one: principles and preparation

by D. T. SCHMIDT and T. F. KAVANAGH

In today's industrial world, systems are being developed to convert customer orders into finished products automatically, so they say. In designing and implementing such complex systems, techniques are needed to reduce applications effort. This means the work required to understand and define the problem, develop and program a solution, and also provide the often neglected documentation.

Decision structure tables meet these requirements. They provide a simple method for recording logic, so that all elements of a decision are precisely defined. Tables make it possible for managers, engineers, accountants, etc. to use computers directly. They eliminate much subsequent programming and coding effort. And the direct use of decision structure tables in a computer opens new horizons for computer applications.

But with any relatively new technique, there are fundamental questions that must be answered:

1. Has anyone "made money" using decision structure tables?
2. How are problems "structured"?
3. Specifically, where are decision structure tables being used in working programs?
4. If decision structure tables are good, why isn't everybody using them?

This article attempts to answer these questions and give practical information on the actual use of decision structure tables.

interest by profession

Decision structure tables have been the subject of many articles and presentations at professional society meetings, such as the CODASYL-JUG Symposium of 1962 that introduced DETAB-X. Of the 500 persons who attended, nearly 250 remained for a follow-up tutorial session. CODASYL's Systems Group has been especially active in promoting interest in structure tables.

Computer manufacturers have also shown interest by fostering the development of programs that would accept decision structure tables for compiling and processing. General Electric, for example, introduced TABSOL (*TAB*ular System *O*riented *L*anguage) as an integral part of GECOM — its generalized, automatic compiler for the GE 215, 225 and 235. IBM and RAND cooperated in the development of FORTAB, a structure table preprocessor to FORTRAN.

where and how decision structure tables are used

Decision structure tables are best applied where there are numerous detailed, interacting decisions involved in a problem solution. The same problem flow charted would have many levels. It would be quite complex and contain "Merry Christmas trees" with many interlocking branches.

For example, in the machine shop a lathe operator must be provided with as many as 30 to 50 values before he can start his job. He must be supplied with tool description, speed, feed, depth of cut, operation sequence, etc. Each of these items are dependent on many factors, such as the machine, the material, and the specific operation. In the office, production and inventory control specialists must know current demand, trends, cost, shelf life and many other values in order to develop intelligent replenishment orders. Similar illustrations could be developed for almost any situation in any business.

These are the kinds of intricate decisions where structure tables have proven especially valuable. Often the complexity and extensiveness of these detailed decisions is drastically underestimated — much to the chagrin of over enthusiastic computer applications engineers, their customers, and their managers. But approached with proper respect, these day-by-day decisions offer one of the brightest potentials for computer applications work. For a discussion of structure table fundamentals, see page 49.

writing decision structure tables

Initially, decision structure tables require some persistence until the skill is mastered. But this is true of any new technique that breaks with established tradition. Actually, writing structure tables is quite simple. It's the process of logical thought which creates the difficulty. Structure tables merely highlight the stumbling block. For this reason, some ground rules were devised to help write tables more easily.

In these ground rules there is a shift in emphasis from flow charting. Flow charts emphasize activities, sequence and flow. In working with flow charts, the first step is usually to identify the major activities, and then to identify the sequence in which they would be performed. These hi-level charts are too macroscopic. Further refinement produces a succession of lower level, more detailed, and more voluminous flow charts. The decision logic that controls the activities isn't really incorporated until you get down several levels into detail.

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A consultant with GE's Manufacturing Services in New York City, Mr. Kavanagh is concerned with computerized business information systems, advanced production and inventory control techniques. He has made presentations on decision structure tables at the '60 EJCC and the '62 JUG-CODASYL symposium. He holds degrees from Manhattan College and New York Univ.

When working at more detailed levels, the programmer must determine how any given decision should be made. The answer probably depends on the value of many different parameters, each of which in turn may be the result of preceding levels or branches. But at this stage most flow charts consist of many balloons, arrows, boxes, lines, etc. in the programmer's unique notation. Flow charts, particularly at the computer code level, contain many yes-no decisions and triple choices — minus, zero, plus. This is a rather small selection. The net effect: Flow charts must be complex to adequately define and solve real world problems.

The shift in emphasis, therefore, is from a flow of activities — which considers decisions secondary — to a technique that considers the decision logic primary.

six ground rules

From the beginning, we have always faced the problem of describing to others how a decision problem or system is "structured". Over a period of time, a six step procedure evolved. These six ground rules provide a step-by-step method for writing structure tables. Each step focuses attention on an important element in the decision-making process. We recognize there is much in these rules that is not profound. But they do describe how a decision is "structured". Further, they provide a consistent approach which has been used successfully to instruct beginners. It is not suggested that these rules must be followed rigorously after proficiency has been gained — but even so, they are a good discipline.

Try writing your decision structure tables using these six steps. They permit you to concentrate on specific decisions — one at a time. See if this approach doesn't help clarify how each decision relates to the total decision-making problem.

It is not unusual to repeat each step several times. Each refinement enables the table writer to improve his decision logic. Define Step 1 as best you can, and then try Step 2. In Step 2 you may uncover something which could correct, broaden, enlighten, or make Step 1 more complete. This isn't an error; it's to be expected. This iteration removes logical errors and inconsistencies; simplifies solution logic; makes it more general and improves the quality of the answers.

Each of the six steps is described below in the left hand column. To demonstrate how the rule is applied, an actual application taken from General Electric's X-Ray Department is outlined in the right hand column. The case history shows how manufacturing engineering specialists used decision structure tables to develop the logic for detailed operating instructions required to make turned parts.

WRITING DECISION STRUCTURE TABLES

Rule 1—Define specific boundaries for the problem.

Define the objective in meaningful terms. You can't solve all the world's problems, nor can you structure all business decision-making. These objectives are too broad, too general. As any other computer application, structuring projects must have a specific purpose. Hopefully, the resulting work will have economic value. Perhaps it will solve a decision-making problem, simulate a system or other useful purpose. The objective should contain the basis for performance specification and measurement. In the illustration, for example, X-ray must tell factory operators which parts to make and how to make them. Perhaps the computer can do it more uniformly and more accurately. Perhaps the present paperwork system takes too long. Perhaps the only objective is to reduce cost through mechanization. But whatever it is, the ultimate objective must be specified in sufficient detail to provide working goals for the project. These statements will assist establishing project schedules and manpower and computer requirements.

Set limits and ranges Because there are as many ways of making turned parts as there are turned parts themselves, it is necessary to detail the objective much further. First, what is the variety of turning equipment in the shop? (Of course, if new equipment is to be purchased, the picture changes.) Then too, what about boring mills, and other pieces of equipment currently available that could be used to "turn parts" under extreme situations? True, they *could* be used but it's better shop practice to use turret lathes. The decision to include or exclude off-standard machines is an important one delimiting the scope of the project.

Additional work must be done to identify and define the characteristics of the various parts being studied: Diameter, length, material, finish, threads, configuration, etc. "Diameter", for example, is important because of lathe feeds, and chucking characteristics. Such limits effectively define boundaries of the planning system. Suitable ranges must be established for each parameter. For example:

CASE HISTORY
MANUFACTURING OPERATION
STRUCTURE TABLES FOR TURNED PARTS

Rule 1—Define specific boundaries for the problem.

a) *Define the objective,* that is factory operator intructions.

1. Produce manufacturing operation planning for making turned parts on lathes — to avoid individual planning of every part.
2. Planning has to include:
   a. Machine selection
   b. Operation description
   c. Operation sequence
   d. Tool selection
   e. Setup information
   f. Running instructions
   g. Feeds and speeds
   h. Time standards.

b) *Set limits and ranges* for turned parts

1. X-ray further limited study to parts that were:
   a. Made on turret lathes in X-ray's machine shop
   b. Made from continuous barstock (this could easily be expanded to include chucked parts if the holding or chucking criteria were included — but it wasn't).
2. The planning system must reflect existing shop practices of the department.
3. Define characteristics of parts:
   a. Physical size
   b. Physical shape
      Simple parts — washers, spacers
      Complex parts — shafts.
   c. Materials
   d. Surface finish
   e. Surface modifications
      Bevels
      Chamfers, rounds
      Threads
      Tapers

Diameter	.250 min.	2.000 max.
Length	.250 min.	5.000 max.
Material	copper, brass, steel, etc.	

Setting these limits and ranges is an extremely important step because you are essentially setting a ceiling on the ultimate value of your work. Obviously, the broader the boundaries, the more problems the resulting tables will be able to solve — but the difficulty will also rise, as will the number of tables — sometimes exponentially. The task, therefore, is to define the real problem. Anything more may have limited value in application; anything less is unsatisfactory.

For example, if the system doesn't cover enough parts in the shop to make it worthwhile, then the work is of limited use. The other extreme would be to encompass so much that you're back to economics — it's so expensive and takes so long to get results, that it's just not worth it.

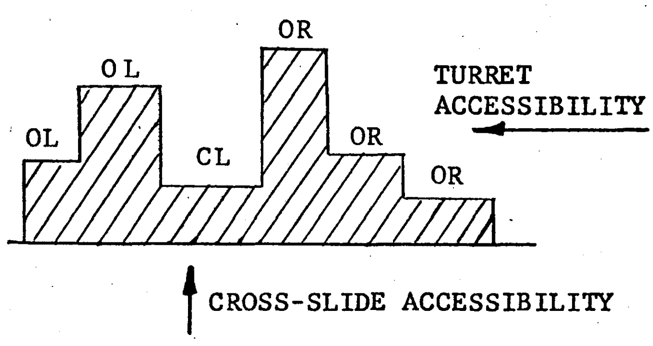
If the objective or problem specification cannot be nailed down, there's some doubt as to whether you should proceed on the project — structure tables or not!

Rule 2—Enumerate individual "elementary" decisions

Rarely are real world decisions the result of one single stroke of intuition or analysis. More typically, the results, which sometimes appear deceptively simple, are the culmination of very many smaller decisions and evaluations. In some respects, it is these small decisions which present most difficulty. Similarly, real world decisions rarely consist of a single numeric value, or a simple yes-no. Most often, many values and actions must be specified to completely define a decision so it can be implemented. In Step 2 we are trying to break down the objective established in Step 1 into a group of smaller decisions or areas of activity. Indeed we want to get down to the smallest meaningful detail of solution — hence the term "elementary". In brief, what do I have to know to solve the problem or make the decision. For example, in the turning project, these are elementary decisions: What are the speeds and feeds? What coolants or lubricants should be used? What size stock? Which machine?

Note the emphasis on small, relatively simple decisions. Each of these small decisions eventually will serve as the basis for one or more structure tables. If you are already flow chart oriented, macro-block diagrams may help break down the problem into elementary decisions in an organized way.

From this point on, attention will be centered on individual elementary decisions. All remaining steps in the six-step sequence should be performed for *each decision* that was developed in Step 2.



Rule 3—Define the necessary outcomes

Rule 2 identified, in general terms, the individual decisions that must be made. These decisions must now be defined in terms of specific outcomes, known as results or

Knurls
Grooves

4. Define characteristics and capabilities of machines and tools:
   a. Machine capabilities (size, feeds, speeds, horsepower, tolerances)
   b. Tools capabilities (finish, clearance)
5. Define the ranges or allowable values for each characteristic:
   a. 7 external diameters (maximum per part)
   b. 3 internal diameters (maximum per part)
   c. 20 different materials (defined initially)
   d. surface finish between 16 and 250 RMS
   e. tolerance capabilities of the machine and cutting tools in terms of specific materials
   f. and many, many others . . .

To do this, X-ray made an extensive study of existing blueprints, operation planning records for current parts, and existing machine tools. This enabled them to determine the requirements of the planning system more realistically in terms of actual needs.

Rule 2—Enumerate individual "elementary" decisions

Here are some examples of decisions and problems which must be solved in order to develop operation planning for turned parts:

In turning parts on a lathe, a first consideration is the L/D (length over diameter) ratio. This ratio indicates whether the part can be made accurately, that is without bending under tool pressure. If the length is excessive intermediate supports can be added, or possibly another manufacturing process should be used.

All that has been established now is that the L/D ratio must be checked — the value determination and refinement will come later.

Each diameter of the part must be classified as open right (OR), open left (OL), or closed (CL). This decision area — that is the logic to assign these surface classifications from a part description is quite complex. It is needed later in the decision making system to determine the accessibility of any surface to tools mounted on the turret (end) or cross-slide (front) of the lathe. (See illustration this page).

Here are some examples of other decision areas — each of which will require many small individual decisions —too numerous to include in this article:

1. Calculate length and depths of cuts
2. Sequence each cut.
3. Select machine.
4. For internal and external diameters
   a. Select process
   b. Modify surfaces
   c. Assign tools
   d. Sequence tools
5. Determine feeds and speeds
6. Determine time standards
7. Format printout.

One simple decision that is required would be the selection of raw bar stock from which to make a part. We will use this decision as an example to show how each subsequent step further develops the elementary decision.

Rule 3—Define the necessary outcomes

In Rule 2 one elementary decision was selected for further explanation: "What bar stock should be used to make this part?"

actions. These outcomes may be specific parameter values, procedural actions, or output results. Any of these may be an intermediate outcome required later in the total problem solution.

The results of most elementary decisions consist of several parameter values. These different outcomes are required to completely define all variables in the solution. For example, it is not enough to decide that "yes", a coolant must be applied during machining operations. Typically, processing a machined part requires several machining operations; turning, boring, drilling, tapping, etc. and the decision to use, or not to use, a coolant must be made for each individual operation. If the decision to use a coolant is made, then more specifically what coolant? Coolants come in many varieties — such as oils, emulsions, etc. And even further, which oil or emulsion. Additionally, the method of application must also be defined, for instance, flood or mist.

Specifying outcomes is quite different when structuring "existing" systems or practices versus "proposed" or new systems. In existing systems the result parameter and parameter values are generally fairly well defined by the current situation. For this reason tables may be purposely written to produce these results. For example — tool selection decisions may be limited to tools that exist in the shop at the present time. This may not result in optimum tool selection, but hopefully they are the best existing tools for the job.

If the system was a new system — and no tools existed — then the structuring approach could provide an analysis technique for determining what tools would be required for "optimum" performance. Then the planning system could be designed around these tools. Quite possibly, over a period of time, tool requirements would change, and the structure tables would have to be updated.

In addition to parameter names, the decision results or outcomes can also signal activities to be performed or indicate the elementary decision to be considered next. PERFORM is an action word which tells the structure table to execute some specific logic or activity designated in the column below. Typically the activity is a common one, such as searching a list, writing a report, or making some common calculation — perhaps taking a square root. The important point about PERFORM is that when the activity has been completed, control returns to the structure table in which the PERFORM was originally issued.

GO TO is analogous to the command GO. This transfers control unconditionally — and without restraints — to some other structure table. This is the mechanism used for moving from one structure table to another; it is the linkage between tables. It essentially replaces the arrow lines on flow charts.

Approaching the problem more classically, the result functions are concerned with the degrees of freedom to be allowed in the decision system. For reasons of cost and complexity, these result parameters must be established with care. Finally, any single decision may result in multiple outcomes. Typically, in industrial applications, one decision will result in many actions. For this reason, the action portion of a structure table is frequently larger than the condition side.

Defining the necessary outcomes requires the table writer to think about how bar stock is described. What does someone have to know to differentiate one kind of bar stock from another. It turns out that bar stock is described by specifying:

Material:	Brass, steel, etc. Sometimes various coded designations of chemical content are required to further identify material — AISI 1040 tool steel, for example.
Shape:	Round, hex, rectangular, etc. This is the shape of a cross-sectional area. Sometimes it is also necessary to state whether the material comes in bars, strips, coils, etc. and tell what the lengths are.
Size:	Associated with a shape is a commonly accepted size designation. Round bars are specified by diameter; hexagonal shapes by the distance between opposite flats; but rectangular shapes require two dimensions.
Finish:	Rough, cold rolled, ground, etc. This is particularly important in developing planning for the first machining operation.

In addition to this basic description, additional information might be required for more sophisticated planning systems which automatically calculate best speeds and feeds. For these calculations, material hardness, ductility, cost, etc. are usually required.

In X-Ray's project, the manufacturing planners always used bar stock. Hence, it was unnecessary to write tables covering coil stock — at least for the present. Of course, if the Department later decides to install some new equipment to handle coil stock, then the structure tables will have to be updated. Ease of maintenance is as important for manufacturing information systems as it is for factory machines.

Similarly, X-Ray usually worked with cold rolled finishes, hence this parameter did not vary.

To simplify this illustration further, material specification — a true variable in X-Ray — has been arbitrarily dropped. Obviously, X-Ray's tables actually contain a full complement of different materials.

The remaining result parameters — bar stock size and shape — require a decision. This decision will be a selection from the available alternative values developed in Step 4 below. The result parameters can now be entered in the "result or action headings" as follows:

	Bar Stock Shape	Bar Stock Size	

In another interesting example, engineers involved in wound coil design once decided to introduce some "coil standardization". Two major variables were wire diameter and number of wire turns per coil. These two variables determine general coil properties. The engineers "standardized" the number to wire turns per coil, resulting in a

Rule 4—Develop value states for each allowable outcome

Each result parameter will usually have a variety of values within the limits and ranges of the basic problem outlined in Rule 1. Considering each and every possible result state could make tables impossibly large. For example, suppose there are five allowable values for each of two parameters. If all combinations were allowed, then 25 different result values would be possible. Twenty-five result values is usually, but not always, unnecessary. Frequently, it is possible to develop simple formulas or equations to describe how a result value changes as a function of various decision parameters. Over-specification of outcome values may also create unnecessary results.

The approach to result values, as well as result parameters, differs greatly with "existing" versus "proposed" systems. Values for existing systems must reflect current usage and practice. In proposed systems we have the opportunity, and obligation, to include the best values for the decision. This, however, is not done easily, it usually requires considerable study and analysis to determine these "optimum" values.

Results may be other than specific values assigned to outcome parameters (data results). The values may be the names of "procedural" or "logic" results. They consist of routines or tables to be solved next as indicated by a GO TO or PERFORM result parameter. They could also be "input/output" results associated with READ or WRITE.

Rule 5—Develop decision parameters affecting each decision

Decision parameters are qualitative factors affecting a decision. So far all possible decision results and outcomes

long list of wire diameters. Stocking many different wire sizes creates some inventory control problems for the factory.

Manufacturing, on the other hand, produces the coils by winding them on an arbor. The number of turns in the coil can easily be controlled by the number of arbor revolutions. Using decision structure tables uncovered this incompatibility — resulting in a coil redesign with complete flexibility in the number of turns and a substantial reduction in the "standard" wire sizes. Now, everyone was happy.

Rule 4—Develop value states for each allowable outcome

Having defined the bar stock size and shape as necessary outcomes, it is now desirable in the case of an existing system to establish the present value states for these parameters. For instance, there may be only round, square, and hexagonal bar stock shapes in the stock room. The round shape may exist in ¼, ½, ¾, 1, 1½, and 3 inch diameters; the square in ½, 1, and 2 inch sizes, and the hexagonal in ¼, ⅜, ¾, 1, 1½, 2, and 3 inch sizes. The raw material stocking program is often outside the boundary of a single manufacturing planning study, hence the available materials, sizes and shapes are "fixed." They must be used the best way possible.

Conversely, it could have been decided, because of the relative ease of obtaining different bar stock shapes and sizes to specify only those sizes and shapes which minimize scrap. In reality, however, manufacturing planning and inventory control should analyze bar stock requirement to balance volume purchase prices against the costs associated with buying over-size stock and removing excess materials. This analysis should produce a list of "optimum" bar stock shapes and sizes.

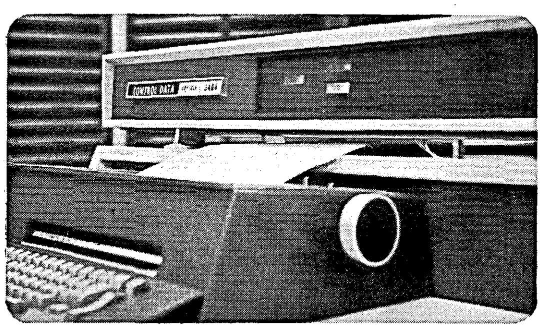
From a computations viewpoint, a geometric stock plan might make it possible to calculate the bar stock using a formula thereby reducing the size of the table considerably. However, this computational convenience is of secondary importance. Primarily, the tables must record reality. Actual bar stock shapes and sizes are posted in the table below:

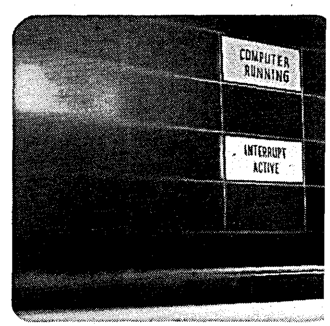
		Bar Stock Size	Bar Stock Diameter
		Round	.2500
		"	.5000
		"	.7500
		"	1.0000
		"	1.5000
		"	3.0000
		Square	.5000
		"	1.0000
		"	2.0000
		Hex	.2500
		"	.3750
		"	.7500
		"	1.0000
		"	1.5000
		"	2.0000
		"	3.0000

Other decision situations in the X-Ray study such as machine tool selection could not be changed so easily — thus the planning was tailored to the available equipment.

Rule 5—Develop decision parameters affecting each decision

In the X-Ray example, the material shape and size were desired outcomes. Accordingly available values were





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The first step in selecting an alternative is to establish the parameters which control the choice. Decision parameters can usually be identified by asking "On what does the decision depend?" At this time, identification of the decision parameters is enough – the assignment of values is done later in Rule 6.

Since the decisions are "elementary", the outcomes are usually a function of only two or three variables. Seldom does a single elementary decision require more than five parameters. In fact if it appears that five or more variables are required, it is doubtful the decision is truly elementary. Apparently life's like that. Decision parameters should uncover true "cause and effect" relationships which really describe why various different alternatives are selected. This step can be a very revealing process in itself.

To correctly establish the decision parameters will require a thorough understanding of the decision. Without this understanding, it is doubtful proper structuring can be done. But with it, many of the previous goals, understanding, documentation, reduced costs and computer applications can be greatly facilitated.

The structuring approach has some built-in indicators when improper or illogical relationships are likely to occur. An excessive number of decision parameters is one extreme; extreme difficulty in establishing relationships between decision and result parameters is another; decision parameters whose values are arbitrary, such as nonsignificant identification numbers rather than physical entities such as dimensions, colors, weights, voltages, current, etc. is still another. On the other hand, if the situation seems extremely clear, and the decisions are relatively small, odds are that the approach is probably sound.

With this understanding of the type of intimate knowledge required for structuring, it is obvious that those best qualified to do the work are the managers, engineers, accountants and other functional specialists actually responsible for it.

established for each. The problem now is to establish the rules for selecting any of these specific alternatives. This example is an extremely simple case. Most others will probably be somewhat more difficult.

Generally, the largest diameter of a part will govern the size of the raw material. Similarly, the shape of the largest diameter probably will determine the shape of the raw material, particularly if the stock configuration (shape and size) is used "as is" for the largest diameter. This might be appropriate for such parts as bolts, studs, spacers, etc. If the part being planned was cylindrical then the problem is reduced to one of selecting the smallest diameter round stock from which the part can be made. Sometimes, it will be necessary to select the next largest diameter because of stock unavailability or because the largest diameter is to be machined.

The actual number of decision parameters for a turned part can be considerable – particularly for complex parts. Values for these decision parameters in any one problem must typically be supplied from problem input. Thus it is important to develop as much as possible from each input parameter. X-Ray inputs generally consisted of engineering dimensions, tolerances, surface finishes, thread sizes, etc., all basic physical characteristics of turned parts. The important point is that when decision parameters are being developed in Rule 5, the table writer is also specifying "input" parameters. In a very real sense he is automatically developing his input data requirements.

One might also visualize another structure table system to design turned parts. The output from such engineering design systems could provide input for manufacturing planning systems, automatically. This is not an unrealistic proposition.

The decision and input parameters pertinent in our illustration are:

Largest OD	Largest OD Shape	Bar stock Shape	Bar stock Size
		Round	.2500
		"	.5000
		"	.7500
		"	1.0000
		"	1.5000
		"	3.0000
		Square	.5000
		"	1.0000
		"	2.0000
		Hexagonal	.2500
		"	.3750
		"	.7500
		"	1.0000
		"	1.5000
		"	2.0000
		"	3.0000

Rule 6—Develop decision parameter tests and values

The next and last step is to assign specific decision parameter tests and values. These tests are used to identify the exact breaking point between alternative results or outcomes. Recall from the insert describing structure table fundamentals, that the decision side of the structure table functions as a pictorial IF-THEN condition statement which relates decision parameter values directly to specific result values. There will be a set of entries for every outcome. If there isn't, there may be trouble. Perhaps the result is not legitimate; or maybe there's some missing decision parameters. If it's the last row of the table, the

Rule 6—Develop decision parameter tests and values

In the example, the relationship of largest OD shape to bar stock shape is rather simple, particularly in the round state. It becomes a little more complex when square and hex stock are turned down to a round shape.

When turning square and hex shape parts, the largest "OD" must correspond exactly with the stock size.

In this table round stock is not available in ⅜ and 2 inch sizes – but hex stock is. A decision therefore was made to turn down hex stock to the round size for certain OD's. Thus, for two sizes – even though the largest OD is to be round – hex stock will be used!

outcome may be a convenient catch-all which is selected whenever the special conditions tested in earlier rows do not apply. Here, the good work done in Step 1 defining the problem in great detail will become very helpful. Many of these numbers will now take their place in structure tables.

When it is not possible to assign specific numbers or ranges to decision parameter value states, use ordered sets of terms – for example good, better, best. The fact that a value state is not a number shouldn't cause difficulty. Actually, the only criteria is that the value state be descriptive of the decision parameter.

The comments made earlier about avoiding exhaustive enumeration of possible result values are equally appropriate on the decision side of the table. Wherever possible test minimum and maximums. When one or more values of a decision parameter satisfy a test, string them together in an OR statement. Similarly, arithmetic expressions can also be used as a decision parameter values.

Filling out decision parameter tests and values is similar to designing a screen to filter a given problem into the correct solution row. All the normal COBOL relational operators are available for formulating tests: LS, NLS, GR, NGR, EQ, NEQ. But over refinement can be costly. The decision side of the structure table should not be more discriminating than the results. If several rows of tests and values yield the same results, the decision parameter value states may be too precise. Such over specification increases both the size and the solution time of the tables. Also, they imply a degree of precision which is not present in the system.

Largest OD Shape	Largest OD Size	Largest OD Size	Bar Stock Shape	Bar Stock Size
Round	GR 0	NGR .230	Round	.250
"	GR .230	NGR .355	Hex	.375
"	GR .355	NGR .480	Round	.500
"	GR .480	NGR .730	"	.750
"	GR .730	NGR .980	"	1.000
"	GR .980	NGR 1.475	"	1.500
"	GR 1.475	NGR 1.900	Hex	2.000
"	GR 1.900	GR 2.950	Round	3.000
Square	GR 0	NGR .490	Square	.500
"	GR .490	NGR .990	"	1.000
"	GR .990	NGR 1.975	"	2.000
Hexagonal	GR 0	NGR .230	Hex	.250
"	GR .230	NGR .350	"	.375
"	GR .350	NGR .725	"	.750
"	GR .725	NGR .975	"	1.000
"	GR .975	NGR 1.470	"	1.500
"	GR 1.470	NGR 1.965	"	2.000
"	GR 1.965	NGR 2.960	"	3.000

Fig. 2

With the six rules outlined, two key points should be emphasized:

First, going through the six step procedure once doesn't mean the job is complete. Going through several times shows how the structure tables interact with one another. The shrewd table writer goes back to Rule 1 again and again to rethink the problem and see if he has done a thorough job. By the second time around, he will usually see ways the logic might be simplified, corrected and made more complete. Repeating the process is not an error. It is a way to achieve more significant results. Remember, it is these same tables that can be used to "solve" problems manually or can be compiled into a computer program for mechanized problem solution. Further, they document the logic for educating newcomers and communicating with others. In brief, they're worth the effort.

Second, if at all possible, focus on the general engineering solution to the basic problem "general" because the tables should provide answers to a whole class of related or similar problems, "engineering" because you are looking for efficient, reliable, economic solutions, but not necessarily optimal solutions.

In developing decision structure table values and parameters it is usually necessary to consider specific cases as much of our present approach to documentation records the answers to specific problem situations. However, when writing structure tables, it is important to step back from specific solutions and try developing the logic for as large a set of conditions and circumstances as possible. For example, engineering blueprints and tabulated drawings most often record the results of a designer's solution to a variety of past problems each solved individually. In writing structure tables we are less concerned with identifying these past solutions as we are with uncovering the decision logic which generated them. If we can successfully uncover the logic for making these decisions, we may be able to reapply it to other sets of circumstances when they arise.

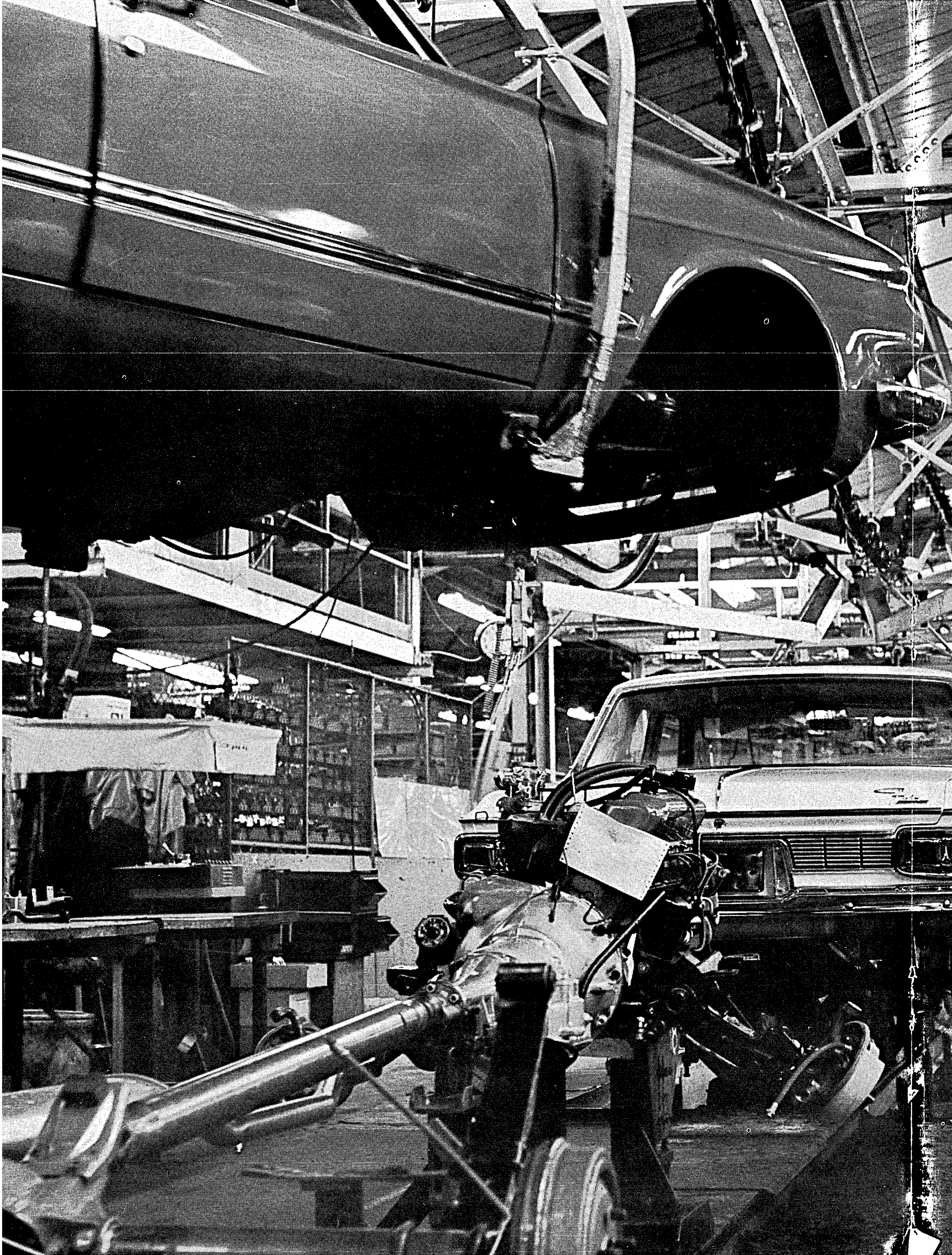
The real power of structure tables is not so much in a table look-up or file reference system as it is in uncovering the decision procedure. This increases the power of the logic so that it can handle decision situations which have never occurred previously but do lie within the bounds of the decision system. ■

Part II, which appears next month, covers the manufacturing applications of decision structure tables.

WHAT ARE DECISION STRUCTURE TABLES?

Structure tables are an advantageous method for unambiguously describing complex, multi-variable, multi-result decision systems. Each structure table is a precise statement of the logical and quantitative relationships supporting a particular elementary decision. They are developed in terms of the criteria or parameters affecting the decision, and the various outcomes which may result. Structure tables were designed for use by functional specialists, who would write in their own professional notation or terminology.

To demonstrate the use of the tabular concept let us examine a simple illustration. Consider poor Dad telling his children how to tell the difference between



THE PROBLEM SOLVERS:

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CIRCLE 23 ON READER CARD

elephants and giraffes at the zoo. Most likely, elephants and giraffes will not be the only creatures in the zoo, but two animals are enough to solve Dad's problem as well as ours. Here's one such Zoo Guide prepared in a slightly stylized format to illustrate decision structure tables.

ZOO GUIDE

animal	legs	nose length	neck length	name
yes	4	not less than 3′	less than 3′	elephant
yes	4	less than 3′	not less than 3′	giraffe
yes	—	not less than 3′	not less than 3′	freak

Note, the Zoo Guide decision can depend on as many as four conditions, the species, sometimes the number of legs, and the neck and nose lengths. The resulting difference identifies the animal.

The table is composed of the number of rows necessary to specify the possible alternatives in the problem. Each row is evaluated in sequence from top to bottom. If all the conditions in a row are satisfied then the corresponding actions are executed and the table is considered solved. In subsequent trips to the zoo additional rows may be required to establish the identity of other creatures.

It is common practice in reading structure tables to insert the word "if" before stated conditions; the word "and" for each single vertical line; and the word "then" for the double vertical line. If any particular condition is not significant to the solution it is merely left blank. For example, the first row of the illustration would read something like this: *if* the creature is an animal, *and* has four legs, *and* the nose length is equal to or greater than three (feet), *and* the neck length is less than three (feet), *then* the creature is an elephant.

The third row would be verbalized as follows: assuming the creature is an animal, regardless of the number of legs, but having a nose length equal to or greater than three (feet), *and* a neck length equal to or greater than three (feet) . . . *then* the creature is a freak.

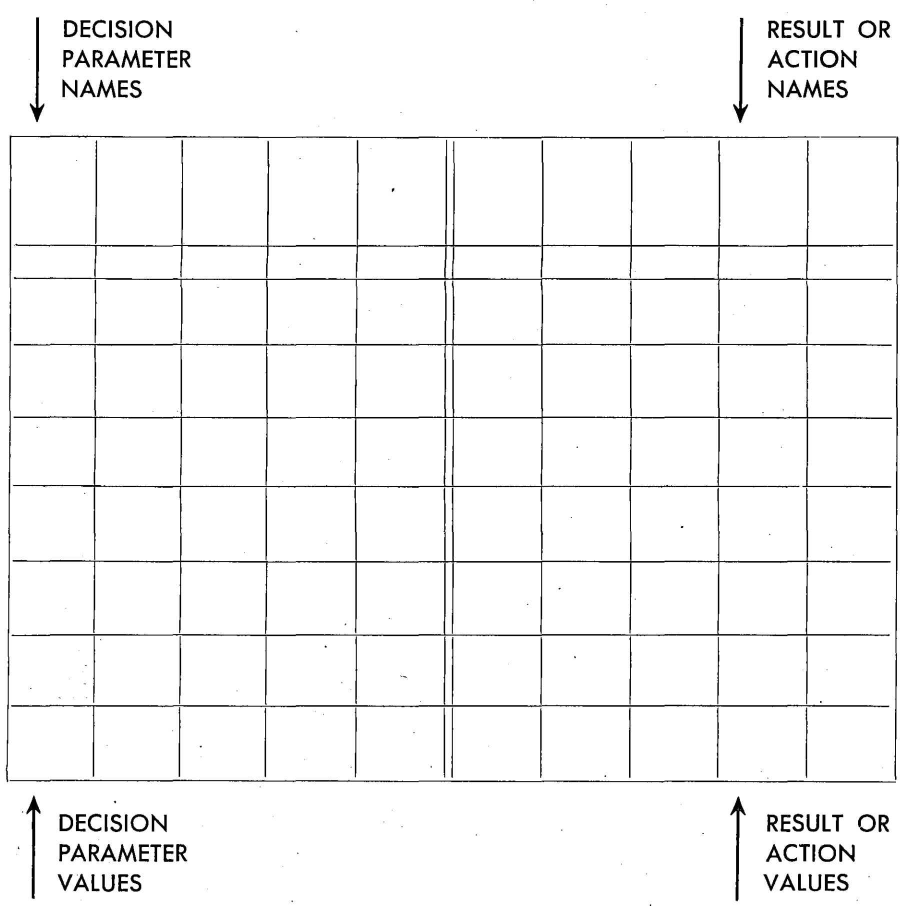
In a similar fashion, the systems designer would use a whole system of structure tables to describe a more realistic decision problem. He completely controls the contents of each table, as well as its position in the sequence of total problem solution. He may decide to skip tables, or, if desired, he may resolve tables to achieve the effect of iteration. In any event, the entire system of tables, just as each individual structure table, will be solved using specific decision parameter values appearing in the problem statement. In other words, solving a set of structure tables consists essentially in re-applying the systems designer's decision logic.

More precisely a structure table consists of a rectangular array of terms or blocks, which is further sub-divided into four quadrants (Fig. 1). The vertical double line separates the decision logic (or conditions) on the left, from the result functions (or actions) on the right. The horizontal double line separates the structure table column headings or parameters above from the table values recorded in the horizontal rows below.

Thus, the upper left quadrant becomes decision logic column headings, and is used to record, on a one-per-column basis, the names of the parameters effecting the decisions. The lower left quadrant records test values on a one-per-row basis, which the decision parameter identified in the column heading may have in a given problem situation. The upper right hand quadrant records the names of result functions or actions to be performed as a result of making the decision, once again on a one-per-column basis. Similarly, the lower right quadrant shows the specific result values which pertain, directly opposite the appropriate set of decision parameter values. Thus, one horizontal row completely and independently describes all the values for one decision situation.

There is, of course, no conceptual limit to the number of columns (decision parameters and result functions) in any given structure table. Even the degenerate case where the number of decision parameters goes to zero is permissible. Also, there is no conceptual limit on the number of decision situations (rows). Thus, the dimensions (columns by rows) of any specific structure table are completely flexible, and are a natural outgrowth of the specific decision being described. A series of these structure tables taken in combination is said to describe a decision system. ■

FIGURE 1



interview profile

DATA PROCESSING MANAGEMENT ASSOCIATION

by ROBERT B. FOREST, Editor

DATAMATION: Could we begin with your name and title, please?
ELLIOTT: R. Calvin Elliott, executive director of the Data Processing Management Association.
DATAMATION: Could you give us a brief history of DPMA?
ELLIOTT: DPMA was organized in 1951 by a group of Tabulating Supervisors in Chicago, who were members of a local organization called the Machine Accountants Association. In their attempt to affiliate with similar groups in other localities, they started what became the National Machine Accountants Association. In the years to follow, chapters were picked up all over the country. These were mainly small organizations—tabulating societies, and so forth—that affiliated as a group and became a chapter. In other words, the international association did not begin with the solicitation of individual members. It has grown, rather, as a federation of chapters. We became DPMA on July 1, 1962.
DATAMATION: What brought about this change of name?
ELLIOTT: It was the feeling of the directors, and many members, that machine accounting no longer properly described our members or our functions. We felt that the name Data Processing had become the accepted term used by government, industry and universities and that this term more adequately described our members. We were data processors, not merely machine accountants, and I think the advent of the computer had most to do with this. The composition of our membership had changed. We went from an association entirely of punch card people to one engaged in the whole spectrum of data processing activity from the simplest manual to the most sophisticated electronic systems.
DATAMATION: In addition to the change of the name from the NMAA to DPMA, what other changes were made to reflect this increasing emphasis on computers?
ELLIOTT: Well, I think a great number of changes were made at the chapter level. Of course, this is the important place. The chapters became more computer conscious, and as a result, revised their programs. Getting away from sessions on how to housekeep a tabulating department, their seminars began to emphasize the importance of getting the most out of the computer, as well as the management problems that had to be solved. So our people changed their outlook and reworked their seminar programs at that level.
DATAMATION: Were there any organizational changes at all, at that time?
ELLIOTT: No, I can't say that there were any organizational changes.
DATAMATION: I wonder if you might summarize for us the goals of DPMA, as it exists today.
ELLIOTT: We are trying to provide more and more technical information and educational guides to our chapters. In other words, our goal is to develop reference materials and education programs, package programs on technical or management themes which we can provide chapters. They could be on a record or tied in with a movie. They can be written packages, or panel arrangements lasting two or three hours or even a full day. These seminars could be used by a chapter or by a division bringing together all the chapters in an area.

For the most part, I'm not certain that our people really know what they need in the education area, so someone, or a group, will have to sit down and do some serious forecasting.
DATAMATION: Then, is education, in the sense of trying to help the people in this field do a better job, your primary goal?
ELLIOTT: That's right, exactly.
DATAMATION: What means do you have to provide this educational service?
ELLIOTT: Well, we don't really have the personnel here to do it, so until we do, we'll have to import qualified people to give us a hand. For example, we're working on a textbook which is aimed at the fourth year secondary school student and can also be used, for example, as a first year college book. Now this is a backup to our Future Data Processors program, and to develop it we brought in the computer manufacturers to help us. Univac, IBM, Honeywell, GE, Burroughs and NCR sent top education representatives to two meetings in Chicago, where they sat down with us, decided what was needed, and assigned themselves various parts of the text to prepare. In a similar manner, we may have to lean on the manufacturers for some of the seminar material we want to prepare. We'll also have to lean on some of our own members, who are further advanced than the majority in technical areas, to help us write and develop material.
DATAMATION: In addition to yourself and Marge Rafferty, the assistant executive director, do you have an educational

coordinator or director?

ELLIOTT: Yes, James Adams Jr., who's director of education. Let's bring Jim in here to discuss our educational program. Perhaps you could start off with the textbook, Jim.

ADAMS: One of the main purposes of the text is to employ it in the Future Data Processors program, which will be reorganized to correlate with the text book material. We feel that we have hit on something vital in our industry, and that is getting young people interested in the subject of data processing and in future career opportunities. To do this we have used a program that, to our knowledge, is unique in any professional field. We don't know of any organization or profession that is engaged in a program of this intensity in terms of secondary education.

Future Data Processors is a lecture course of some 20 hours plus field trips to data processing installations, a course offered by many of our chapters to high school seniors at no charge. The purpose is simply to inform them as to the nature of unit record and computer equipment. It is essentially a data processing and computer concepts (or appreciation) course. This is a course that generally is not available until college, and in the early years of computing was given only by computer manufacturers. Such courses are now commonplace in many colleges, but we feel, considering the importance of computers and automation in everyone's future, that young people should have a data processing concepts course as part of their high school program. FDP is only a stop-gap measure until high school teachers can be trained to take over the job. DPMA is assisting in that too.

We hope that through Future Data Processors we will at least plant the seed of interest in selected young people to choose data processing as a career. I think it should be emphasized that due to our limitation of instructors we are not offering the course to just anyone. We ask the teachers and the administrators in the schools to select for us those people who have demonstrated through their grade average, or by other evidence of strong motivation, that they will attend regularly and are likely to profit from this instruction. We try to limit our classes to some 20 or 25 people.

On the other hand, many of our chapters have offered these FDP courses purely for high school teachers and administrators. We have done this because of the serious lack of teachers trained to teach the subject. We applaud the efforts of colleges which now offer summer institutes in data processing for teachers, and have participated in these programs both at the headquarters and chapter levels. The institutes that the Department of Health, Education, and Welfare sponsored last summer at five colleges across the United States received active support from DPMA headquarters.

DATAMATION: Are you doing anything in the area of curriculum planning for colleges or universities?

ADAMS: We assisted HEW in developing its suggested two-year post-high school curriculum for NDEA Title VIII programs which many junior colleges, especially in California, are now using. Mainly we are offering suggestions which center around the Certificate in Data Processing academic requirements, and which we hope will form the nucleus for degree programs in the subject. Bachelor and masters degree programs in systems and data processing are relatively new. My impression of this is that they are still feeling their way, which is only natural. We know of a number of bachelor's programs that are being explored in which the business administration department is offering a concentration in data processing, sometimes under a different title, such as "quantitative methods."

Regarding the CDP academic requirements, we are presently waiving them and expect to until the 1965 exam. At that time we expect to have these requirements enforced. I might add here that there is nothing static about the academic requirements. They have already changed from the original 1960 list and will be under constant review. In formulating the requirements, the committee took a very close look at what it felt should be the necessary academic background for a professional in this field. The courses generally comprise a combination of subjects in mathematical areas as well as business, for which there is usually no single department in most universities. We realize that we are recommending a curriculum that borrows from a number of traditional school departments but that shouldn't deter anybody. Eventually, I think, there will be departments, or at least sub-departments, in universities that will be devoted strictly to systems analysis and data processing studies.

DATAMATION: The certificate exam has been revised a couple of times and is becoming longer and more rigorous. Will this trend continue?

ADAMS: We expect that it will, although not out of design. That is, there isn't anything insidious about this; there is no plot to make this a more rigorous examination. I feel, and this is purely an opinion, but one that is borne out by other professional examinations, notably the CPA exam, that when you have an examination which is developed by the people who have passed the exam, there is an automatic built-in inclination toward making it more difficult. Also, toward making it more practical for the profession. Our first examination was developed for us by professors, people who were academicians in a university, as well as various consulting people, but since then the preparation of the examination is being conducted by a committee of people who passed the examination with high scores, who have shown through their outside professional activity that they are competent and have strong academic backgrounds. Now when these people take a look at the old examination and begin to revise it, they see weaknesses automatically. They have a chance to discuss these weaknesses of the past exams to try to improve them. And because we are working with an enlarged certificate committee, which feeds questions into the council, and I might add here that the committee itself has qualifications very much like those of the council, we are automatically building in a better test.

DATAMATION: Eventually, might the certificate become the final exam which would take place after a college curriculum designed to prepare people who take the exam?

ADAMS: By insisting on academic requirements in 1965

Since May of 1960, Mr. Elliott has been executive director of the DPMA, in which capacity he directs the administrative functions of the association's International Headquarters in Park Ridge, Ill., a suburb of Chicago. He is a member of the American Society of Association Executives.

we are naturally building in the hope and the expectation of a degree program of some sort before taking the exam. If you will look them over, you will find that in terms of units the academic requirements are the basis for a bachelor's degree in data processing. However, we still have the three-year experience requirement, and at least until the academic courses are no longer waived we would expect people to have the three years' experience before taking the examination. We have had a number of letters from people who have asked if they could waive the experience requirement, take the examination now and receive the certificate after they have completed the experience. In every case we have rejected these requests. We feel at present that people must first have had the three years' experience, but, of course, this policy could change. We do expect that this will be a professional culminating type of examination in the sense that the CPA is. We want to build an examination that five to 10 years hence will be considered by everyone to be the professional standard in the field. We realize that this takes time; you don't do this overnight but we have come a long way. The response to the examination has been beyond many people's wildest dreams. Now we've lifted our sights and feel that the certificate has already assured itself a strong place in the industry.

DATAMATION: What does this do to the man who wants to stay at the tab level, who is not interested in the exam? Does this tend to exclude these people from the DPMA or mean that it won't reflect their interests as well?

ADAMS: The certificate is something that is set apart pretty much from DPMA membership. For, while it is sponsored by DPMA, it has nothing to do with DPMA membership, per se. We do not require a certificate for membership, nor do we expect that DPMA members should all obtain a certificate. The certificate program is for the profession as a whole, and as a matter of fact, many people who are certificate holders may not be eligible for membership in DPMA, depending upon the bylaws of the particular chapter in the area, as well as the national organization. We are an organization of staff and supervisory level people, and it is quite possible that other persons will obtain a certificate in data processing. So, while the association is sponsoring it financially and, of course, administering the examination, it is not necessarily tied in with DPMA membership. In fact, Bob Patrick, a member of the Certificate Advisory Council, was not a DPMA member at the time of his appointment last spring. To my knowledge he still hasn't joined. Almost 4,000 have taken the exam so far, almost 2,500 last November, and not all are DPMA members.

DATAMATION: What does the DPMA do for the kind of person I've just mentioned—someone who is pretty much tab oriented?

ADAMS: In this area we would hope to broaden his spectrum, to increase his education and, of course, his value to the firm he is working for. We feel that there are definite limitations in the area of tab supervision and the past five years certainly has proved this. The replacement of tabulating equipment with computers at a competitive price is forcing the tab supervisor to learn computers and I'm sure the next five years is going to show an even more rapid increase of this type of activity.

DATAMATION: Could you provide a brief description of the organization of DPMA?

ELLIOTT: We have 187 chapters in the United States, Canada and Japan. These chapters operate under their own bylaws and operating rules approved by national. They have their own board of directors, consisting of a president, vice presidents, etc. Each chapter has, as a member of its board, an international director. This man attends two meetings a year—one in February for two days, and the second in June at the site of our international conference for one day. We also have an executive committee. These are international officers. In addition to the president, executive vice president and treasurer there are seven vice presidents, each covering a different area, such as education, bylaws and so on. The international director is the representative of each chapter. In their two meetings each year they elect the international officers (executive committee) and conduct the business of the association.

DATAMATION: How many of these officers are there?

ELLIOTT: President, executive vice president, seven vice presidents, vice president of the next International Conference, and myself as executive director. I am employed by the executive committee as the paid full-time operating head of the association's International Headquarters in Park Ridge, Illinois.

DATAMATION: Do you serve a term?

ELLIOTT: No. I have no term of office.

DATAMATION: Your job, in addition to helping guide policy, is to interpret and implement the policy of the executive committee and international directors?

ELLIOTT: That is correct.

DATAMATION: How many DPMA members are there?

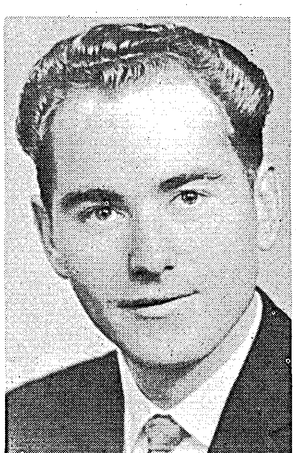
ELLIOTT: We have approximately 16,400 members.

DATAMATION: Have you any idea how many of these people represent tab people and how many computer people?

ELLIOTT: Not as yet, but I feel a fair estimate would be that 55 per cent might be computer people. It might be interesting to explain at this point that as a result of our last certification exam we will find out for the first time who our people are and more specific information about what they do. This will give us a great deal of valuable information that is non-existent today.

DATAMATION: How much does membership in DPMA cost and how does somebody apply for membership? What are the rules for deciding whether or not he can belong?

ELLIOTT: At the present time there is no established fee. Each chapter sets its own figure. For example, one chapter may charge $35 a year for membership, another may charge $15. We hope some day that we might standardize our dues. I would say the average fee is around $25. Now to join . . . this takes place at the chapter level. There are, in the bylaws, specifications and requirements setting forth membership qualifications. You must be of supervisory capacity, or what we call "Director of Data Processing." One applies in any city where we have a local



The education director for the DPMA, Mr. Adams has been a dp instructor, programmer, and systems analyst for such organizations as North American Aviation, Honeywell, and the Oregon Dept. of Motor Vehicles, as well as at UCLA and Oregon State Univ. He is also the author of a curriculum in dp technology for the Oregon Dept. of Trade and Industrial Education.

chapter . . . we are very well covered with chapters from coast to coast. Applications for membership are submitted to our local chapter board of directors and they either accept you or turn you down, based on qualifications. If you are accepted, you become a member of a chapter and your membership is then forwarded to International Headquarters; we in turn issue a membership certificate, making it official.

DATAMATION: What does a member receive from National?

ELLIOTT: A most important item is the monthly publication, Data Management. The majority of the material that headquarters provides goes directly to the chapter. They in turn pass this material on to the member. The data processing book, proceedings from our International Conference, is available to members at a nominal rate. It's our hope through an extensive education program developed by our department of education that we will provide and make available to the chapters packaged education programs as well as traveling seminars. . . .

DATAMATION: I understand there is a $75 fee for attending the annual international conference?

ELLIOTT: That is correct.

DATAMATION: How does this compare to other organizations?

ELLIOTT: I would say it is close to average for what you receive. The most knowledgeable people in data processing conduct our seminars and I know the information and knowledge they convey is worth $75. There are no plans to increase this figure; it is our plan to continue the $75 fee through 1965 in Philadelphia.

DATAMATION: Will your fall meeting eventually become a western equivalent of your big International Conference?

ELLIOTT: Our big conference in attendance will always be held in June of each year and it is our feeling that our membership, i.e., the bulk of our membership population, is east of the Mississippi river and we will attempt to keep the June International Conference in this geographical area. We have a sizeable membership representation in the western area and they too must be served. The fall conference will be held in either late October or November of each year. This will be a nationally sponsored conference. It will be supervised by International Headquarters with the cooperation of our local chapter in the host city, the same as our June International Conference.

DATAMATION: Does DPMA get involved in language standards work?

ELLIOTT: Yes, we are. We have had a standing committee membership for some time but have not been involved as much as we would like to be. We plan to become involved; I feel this is where we belong. DPMA, as the association representing the user group in data processing, should be involved and active on many committees.

DATAMATION: Has DPMA taken any stand at all or taken part in any of the current hearings on proposed federal legislation?

ELLIOTT: None at all.

DATAMATION: Do you plan to take an active role in this area?

ELLIOTT: Not at present.

DATAMATION: I wonder if you would discuss your relationship with ACM? First of all, would you characterize ACM as primarily concerned with scientific computing and DPMA with business data processing, and is it true there is some investigation being made of the possibilities of a merger between DPMA and ACM?

ELLIOTT: Recent scuttlebut points to ACM possibly leaning in the direction of the user, better known as the DPMA member. Mind you, I said scuttlebut. If this were true, there must be a reason and my guess is they may have discovered the scientific sphere much too confining, from a membership viewpoint, or perhaps ACM members now require business data processing and more knowledge of management. If this scuttlebut is correct, couldn't this be, "the grass is greener on the other side of the computer room"? The ACM-DPMA merger conversation that had drifted around these past years is, to the best of my knowledge, erroneous. There has been no serious discussion in this area. They (ACM) are scientific; we are business.

I will say that DPMA would be willing to cooperate in any way with ACM—on a cooperative basis, let's say an information exchange basis—providing we could find common ground. As far as a merger is concerned, I know nothing about it and as a result find it difficult to foresee.

DATAMATION: Do you foresee the possibility of DPMA becoming a part of AFIPS?

ELLIOTT: Not at the present time. There has been no discussion in this area.

DATAMATION: Would you be interested in belonging to AFIPS?

ELLIOTT: There is a possibility we might be interested. We are always interested in ways of broadening our scope. If AFIPS has clear-cut programs that through membership would result in added benefit to DPMA members, our officers would certainly consider membership. On the other hand, what does AFIPS have to offer? Do they have direction and a program?

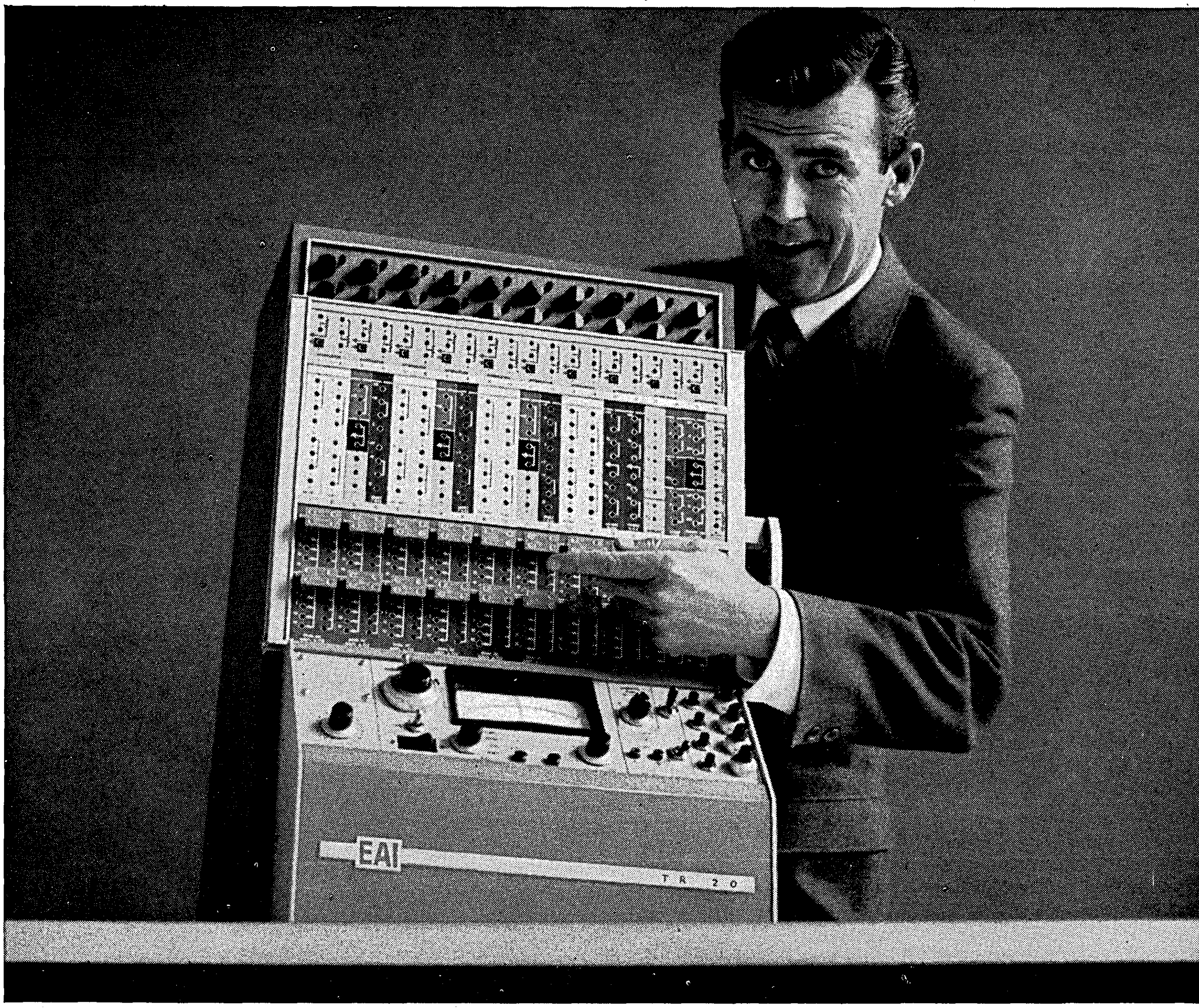
DATAMATION: I wonder if you would talk briefly of future plans for DPMA and where you plan to go and how you plan to get there?

ELLIOTT: Our main interest, and primary purpose, is education. We intend to continue pressing our own people to educate themselves and keep abreast of what is happening in this industry, and that is a full-time job in itself for the individual—just trying to stay up with the game in data processing: the latest announcements from manufacturers, the latest systems that some of the users are employing.

By the same token, we wish to expand the idea of professionalism in data processing by interesting more and more of the college professors in our organization, by opening our doors as widely as possible now to academic circles, people who, in the past, have not by and large been members of our association. Perhaps they did not find enough interest for them in our group, but we feel now that in order to uplift ourselves professionally and to keep the universities informed as to changing needs in the industry, we must associate ourselves very closely with college programs, both graduate and undergraduate. This year, the Milwaukee chapter instituted a faculty membership category at a reduced fee.

We also have a great deal to offer the colleges in terms of their student participation. We do not have student memberships at present, but are experimenting with this possibility. We can offer the students and professors a great deal in terms of installation touring and special lectures, in terms of participating and assisting the classroom professor or teacher with examples and demonstrations.

In the future, we plan to increase our educational services to the member and, through the member, to his company. We are preparing a new course in data processing, which chapters may present to higher and middle levels of management on an invitational basis. We are also planning to increase our output of educational literature to members—particularly in the area of reference material. All this takes time and people and we are just beginning to enlarge our staff to handle the added services our members demand and deserve. We have come a long way but there is much farther to go. ■



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CIRCLE 25 ON READER CARD

THE HONEYWELL 200

by IRMA M. WYMAN and Dr. REINHOLD P. SELL*

The Honeywell 200 is a small-scale, character-oriented business data processor. Modular in design, the 200 permits simultaneous operation of up to four high-speed peripheral devices without the use of buffers in peripheral controls. It is adaptable to card, tape, drum and disc operations, and can be used as a free-standing system or as a satellite to larger computers. Monthly rental for a basic card system is $3,160.

A combination of hardware design and a translator, called Liberator, can convert IBM 1401, 1440, and 1460 programs to H-200 programs which will run as fast or faster on the 200 as on the equipment for which they were originally written.

Part of the 200's capacity to handle and control a variety of peripheral devices is due to the variable-length instruction format, which has up to two main memory addresses per instruction, enabling manipulation of characters either singly or in groups.

Among major hardware features are:

- a two-microsecond cycle main memory with a capacity of from 2,048 to 32,768 alphanumeric characters;
- a 500-nanosecond cycle control memory which replaces control unit registers;
- a multiple read-write-compute capability without the use of peripheral buffering or program interrupt.

The main memory of the 200 is a nine-plane, coincident-current core memory. It has an access time of one microsecond, and a complete cycle time of two microseconds. Each nine bits constitute an addressable six-bit character, a parity bit, and two punctuation bits. The punctuation bits are used to group characters into fields, items, and blocks. Each of these units can be manipulated by programmed instructions. The H-200 also uses a "scratchpad" control memory of 16 individually addressable control registers.

As to speed, a five-digit add (A+B→B) requires 44 microseconds; a five-digit compare requires 34 microseconds. The effect of its simultaneity feature is best illustrated by example; in one minute, the 200 can do *all* of the following: read 800 cards, punch 250 cards, print 900 lines, read or write 4,360 tape records of 500 characters each, and execute one million instructions.

The instruction set includes both decimal and binary arithmetic. The decimal arithmetic operates on data in six-bit form; the binary arithmetic is used primarily for address modification or for simple counter operations. A trio of logical instructions provides the facility to alter the bit configuration of an operand by using a second operand to "mask out" or insert *one* bits.

In systems with 2,048 or 4,096 characters of memory, an operand address is designated by two characters; to specify locations above 4,095, however, three-character addresses are required. Regardless of the size of the system, the two-character addressing mode may be used to address all locations below 4,096. This ability to change addressing modes provides two distinct programming advantages: 1) if a user expands the memory size of his installation above 4K, the program written for his initial system will run without change, and 2) use of the two-character mode to address locations below 4,096 in a large system decreases program storage and saves one memory cycle for each operand address processed.

software

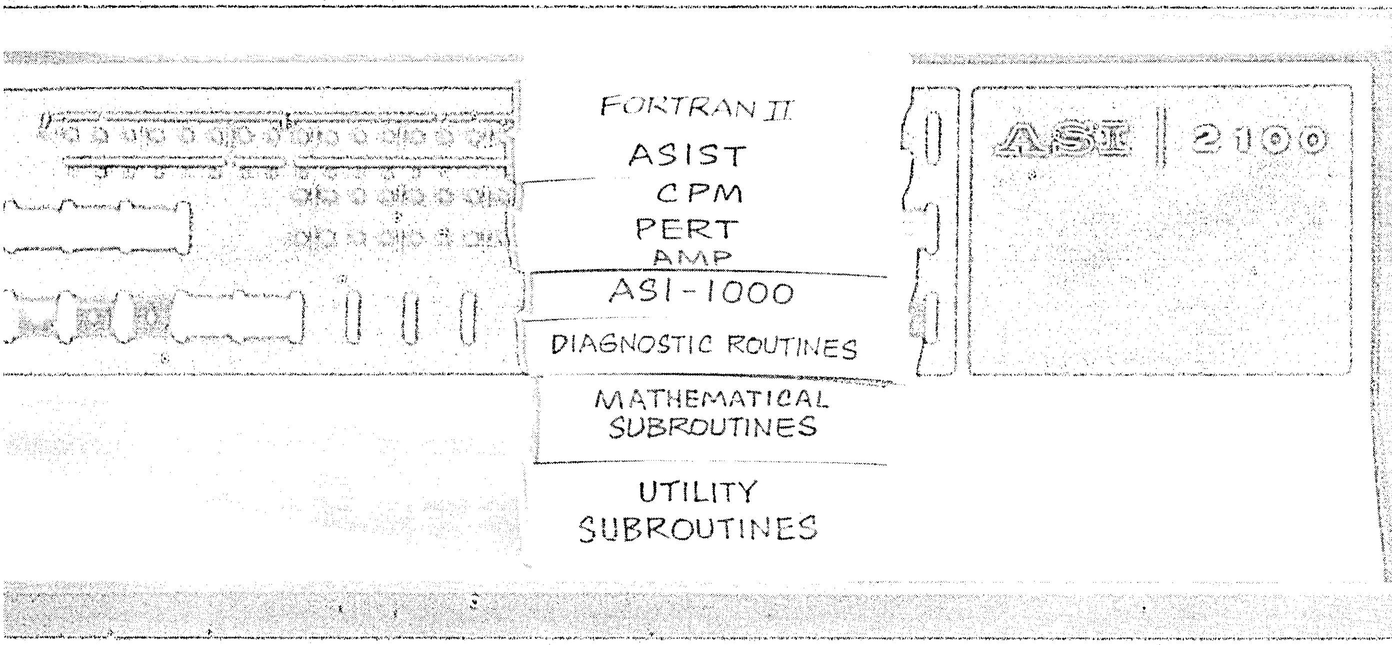
The basic assembly and operating system, EASYCODER, is available in two versions for use either in small card installations with 2K characters of memory, a card reader and punch, or in tape-oriented installations with at least 8K characters of memory, a card or paper tape reader, a card or tape punch, printer, and four magnetic tape units.

Peripheral packages available with the EASYCODER systems include sort generators which use the Honeywell polyphase sorting technique; a tape input-output package which controls the blocking and unblocking of data stored on magnetic tape; and a report generator which permits the user to define control fields and the lines of a report.

Software for the H-200 also includes COBOL and AUTOMATH compilers. The COBOL is a syntax-directed, systems-integrated compiler requiring 16K characters of memory, six tape units, a card (or paper tape) reader, and an on-line printer. Designed on a modularly expandable basis, the compiler is self-adapting to larger configurations of core storage, and features highly optimized object code. AUTOMATH is a scientific language compiler which processes FORTRAN II. This compiler requires a 16K memory, four magnetic tape units, a card reader and punch, and produces object programs on cards or on magnetic tape for load-and-go operations. ■

[Ed. note: system prices for the 200 range from $140-500K, and rentals from $3,160 to more than $10K. Delivery is scheduled to begin in July 1964.]

*Engineering consultant and director of Product Planning, respectively, for Honeywell EDP, Wellesley Hills, Mass.



The deck is stacked in your favor at ASI

ASI's outstanding new 2100 computers are delivered with complete user-tested software. Software for the 2100 derives directly from programming systems thoroughly proved out on earlier ASI computers. In this way 2100 programming aids have been tested, used and completely checked out on actual programs under field conditions. There are no ifs, ands, or bugs left. You can write your program from the book and know it will run on the 2100.

FORTRAN II. Unlike partial FORTRAN II compilers, ASI's complete FORTRAN II compiler includes subroutine and function statements, arithmetic function statements, as well as Boolean algebra statements. Statements will handle all peripheral equipment. An additional FORTRAN feature is that of "program chaining" which allows programs whose size exceeds available memory to be run in segments.

ASIST. A S I Symbolic Translator is an assembly program that allows the use of standard macro coding of such functions as floating point routines and input/output routines. Special features of ASIST include pseudo codes such as ENTRY, COMMON, and LINK which permit flexible linkage, data sharing among subroutines, and program overlay. ASIST provides for the acceptance of source program from cards, paper tape and magnetic tape. Naturally, such assembler directing codes as RES, OCT, DEC, EQU, ORG, etc., are provided.

CPM and PERT. Special planning and scheduling procedures are available for real-time management control through the use of the Critical Path Method and the Program Evaluation Review Technique. These procedures provide management with project planning information, scheduling, data and other associated intelligence.

AMP. ASI Monitor Program allows for the centralized control of program operation. It provides a load-and-go operation without operator intervention. The operator can specify loading and execution of any program on the master system tape by a simple on-line typewriter directive.

ASI-1000. This special interpretive routine allows programs written in Bendix INTERCOM for the G-15 to be operated by the 2100. A converter program automatically converts binary G-15 program tapes, including data, to binary paper tapes that can be run in ASI-1000. Therefore, no manual recoding is required.

MATHEMATICAL SUBROUTINES. ASI provides a complete set of mathematical subroutines including SINE, COSINE, SQ ROOT, EXPONENT, LOG, etc.

UTILITY SUBROUTINES. A number of routines allowing tape reproduction, conversion of cards to tape and tape to cards, memory dump, paper tape updating, etc., are also available.

DIAGNOSTIC ROUTINES. Diagnostic routines covering both program and hardware checking are available.

We'd like to tell you more about ASI's outstanding new 2100 and its use-tested software. For software manual please write to:

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THE FADAC

U.S. Army Ordnance has developed over the last five years what is probably the world's most rugged, general purpose, portable computer. FADAC (Field Artillery Digital Automatic Computer) can be dropped from a helicopter at 15 feet, is immersible in water, will operate in rain, salt-laden air, and dust storms; it measures 29 x 15 x 34 inches, weighs 200 pounds, and can be carried by two men. Thus far its usage has been primarily in the areas of field artillery computation, out-of-doors automatic checkout systems, long range surveying, meteorological data reduction, inventory control, and Tactical Data Systems. However, Stanley Greenberg, Army Ordnance FADAC Program Manager, suggests that it has a host of other areas of application and expects to see it utilized in commercial as well as other military systems in the near future.

The military requirements on which FADAC characteristics are based were completed in 1957. A research and development program was subsequently undertaken by Autonetics, resulting in several R&D models which were tested and approved by the Army Artillery Board in late 1960. In 1961, Teledyne Systems Corporation of Hawthorne, California, was selected by U.S. Army Ordnance to manufacture FADACs to meet military requirements and, since, has been the exclusive quantity producer. At the current production rate, FADAC will be the world's second most used computer in 1965.

FADAC features a disc memory with a capacity of 8,192 32-bit words, with a 78-microsecond word time. There are two 16-word and one two-word rapid access loops, 36 commands exclusive of input/output, a push-button matrix for manual selection of prestored programs, and a two-address word for minimum access coding. Average access time is five milliseconds. It is estimated that FADAC can be supplied for commercial and other military applications for $35,000.

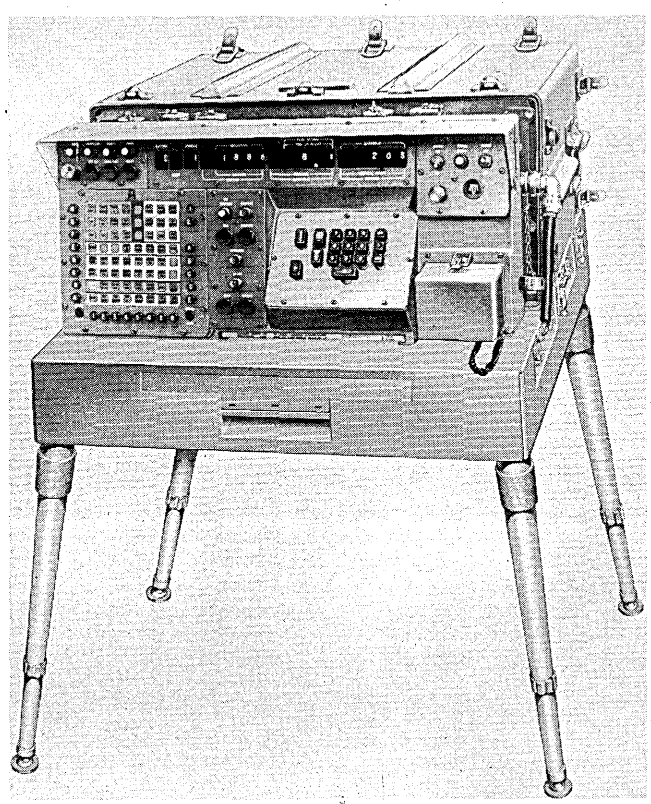
Teletypewriter and paper tape input/output are used. A real time input/output register can be attached for satellite tracking and other real time monitoring operations, and a magnetic tape tub is under development contract with the Librascope Division of General Precision.

As an inexpensive general purpose computer, FADAC will enter the usual small computer market for use by small computer-oriented engineering groups. However, its ruggedness and portability provide new and unique capability in out-of-doors computing. The portable jeep-mounted automatic checkout system READY MAIDS (Multipurpose Automatic Inspection and Diagnostic System) uses FADAC as the control computer and has been programmed for feasibility study of field checkout of NIKE components. Field computation has proven very useful in artillery firing where FADAC may be operated under battle conditions to integrate the differential equations of choice of trajectory, and other data are entered as parameters at the FADAC keyboard. Using these methods, the probability of hitting a target such as a bridge is 0.90 after two rounds, while an average of 25 rounds are needed to achieve this effect using the manual system of gauging fire. Field computing will also be accomplished in the electronic vans of Army tactical information systems using a van installation model of FADAC with remote control panel; in still another area of application, FADAC is used for in-the-field reduction and analysis of surveying data by the Army's Geodesy, Intelligence Mapping Research and Development Agency.

FADAC software includes one assembly program which assembles on FADAC for FADAC and another under development which assembles on the UNIVAC SS-90 for FADAC. Two compilers are under development; one for an algebraic language, another for an automatic checkout language. Both compilers use the IBM 7090 for the compiling process. The algebraic compiler will generate either 7090 code or FADAC code. By use of this code option, much of the user's program can be checked out on the 7090 before final checkout on FADAC. The algebraic compiler language is NELIAC with modifications and is known unofficially as NELIAC-F (FADAC). The automatic checkout language features such statements as "MEASURE VOLTAGE FROM POINT A TO B," and will be used for the MAIDS series automatic checkout equipment.

Regarding new uses of FADAC, Teledyne emphasizes that FADAC is a general purpose computer, rugged, portable, and inexpensive, and is suitable for any application for which these are the key requirements. It is available for both civilian and military applications. The U.S. Army plans to utilize FADAC at the battalion and battery level in its CCIS-70 (Command Control Information System—1970) program. FADAC is standard equipment for the Canadian Army and is under test by English, French, and German armies.

Teledyne expects to see more civilian use of portable computers. Portable computers like FADAC have application in the field to the problems of civil engineering, geological surveying, oil well logging, meteorological data reduction, mining, highway construction, other activities. ■



people IN DATAMATION

■ William E. Bratton has been named vp-general manager of the Ampex Computer Products Div., Culver City, Calif. He was formerly president of General Precision's Information Systems Group and, before that, head of GP's Librascope Div.

■E. S. McCollister has been appointed divisional vp and manager of operations for RCA-EDP. Succeeding McCollister as divisional vp-marketing is Robert G. Dee, formerly head of product planning and systems programming. Dee's successor will be William R. Lonergan, who most recently served Univac in a similar capacity.

■Vico E. Henriquez has been named the director of standards for BEMA's data processing group. Most recently a consultant to New York state's Budget Division, he was previously technical adviser to the comptroller of GSA, and has served as representative to ASA's X3 committee on standardization of computers and information processing.

■Dr. Jack Moshman has been named vp-professional staff services for CEIR Inc., succeeding Dr. Alexander M. Mood who has retired. Replacing Dr. Mood on the board of directors is John M. Randolph, vp of Boothe Leasing Corp. Jack Roseman, chairman of the '64 SJCC program committee, has been named manager, professional services for the 25-state central region of CEIR.

■Richard C. Warren, former assistant to the president of IBM's DP Div., has been named vp-marketing for that division.

■Louis C. Ray has been elected chairman of the Special Interest Group on Information Retrieval, Assn. for Computing Machinery. Ray is with Hughes Dynamics Inc., Los Angeles.

■A former staff engineer, Robert Lord has been named (analog) computer research manager for the Berkeley Div. of Beckman Instruments Inc., Richmond, Calif. He succeeds Dr. Maxwell C. Gilliland, now chief of a mathematical analysis group.

TIME-SHARING AT MIT and SDC

A network of "computer public utilities" may result from current research in time-sharing, predicted Prof. Robert A. Fano, head of MIT's Project MAC, at a recent press conference and tour of MAC facilities. Such a network, Fano said, would provide a "link of intellectual communication" between people. He added, however, that he was reluctant to forecast when a system of this nature could be placed in operation. "Time-sharing is an evolutionary process, and system operating goals cannot be placed on a formal timetable."

Sponsored by the Advanced Research Projects Agency of the Defense Dept., the press conference was held "to demonstrate some of the early steps" achieved by Project MAC in developing a working time-sharing system. The occasion also brought forth a progress report on similar research activity by System Development Corp., Santa Monica, Calif.

At MIT, three demonstrations of on-line programming were shown to the press: a program that computes compound interest (written in FORTRAN II), an information retrieval program (in LISP), and a program designed to compute average gasoline consumption (LISP). Each program was run while other users at remote Teletypes were simultaneously using MAC's 7094 for their own programs.

Central hardware in the SDC system is a Q-32 computer, with a PDP-1 which controls real-time inputs and outputs to the Q-32. This function in an off-line mode is handled by an IBM 1401. Also included in the system: 24 on-line Teletypes scattered through the firm's headquarters complex, six 16-inch CRT display consoles, and six Data sets connected to the PDP-1 and available for TWX service, making the Q-32 available to outside users in a time-sharing mode. Jules Schwartz heads the research activities.

At MIT, representing ARPA-supported organizations active in time-sharing research, were Don Drukey of SDC, Fred Tonge of Carnegie Tech, and Don Pollack, Office of Naval Research. Participating institutions also include Stanford Univ., Stanford Research Institute, and the Univ. of California. ■

NEW FIRMS
mergers in DP

IBM has acquired for some 62 megabucks Science Research Assoc. Inc., Chicago publisher of educational materials and psychological tests. Among its products is the National Merit Scholarship Qualifying Test. The merger must be approved by both boards of directors and SRA stockholders.

IBM World Trade Corp. has announced establishment of a development engineering lab in Vienna, Austria, joining similar labs in France, Germany, The Netherlands, Sweden, and the U.K. Research will be conducted in information and automata theories.

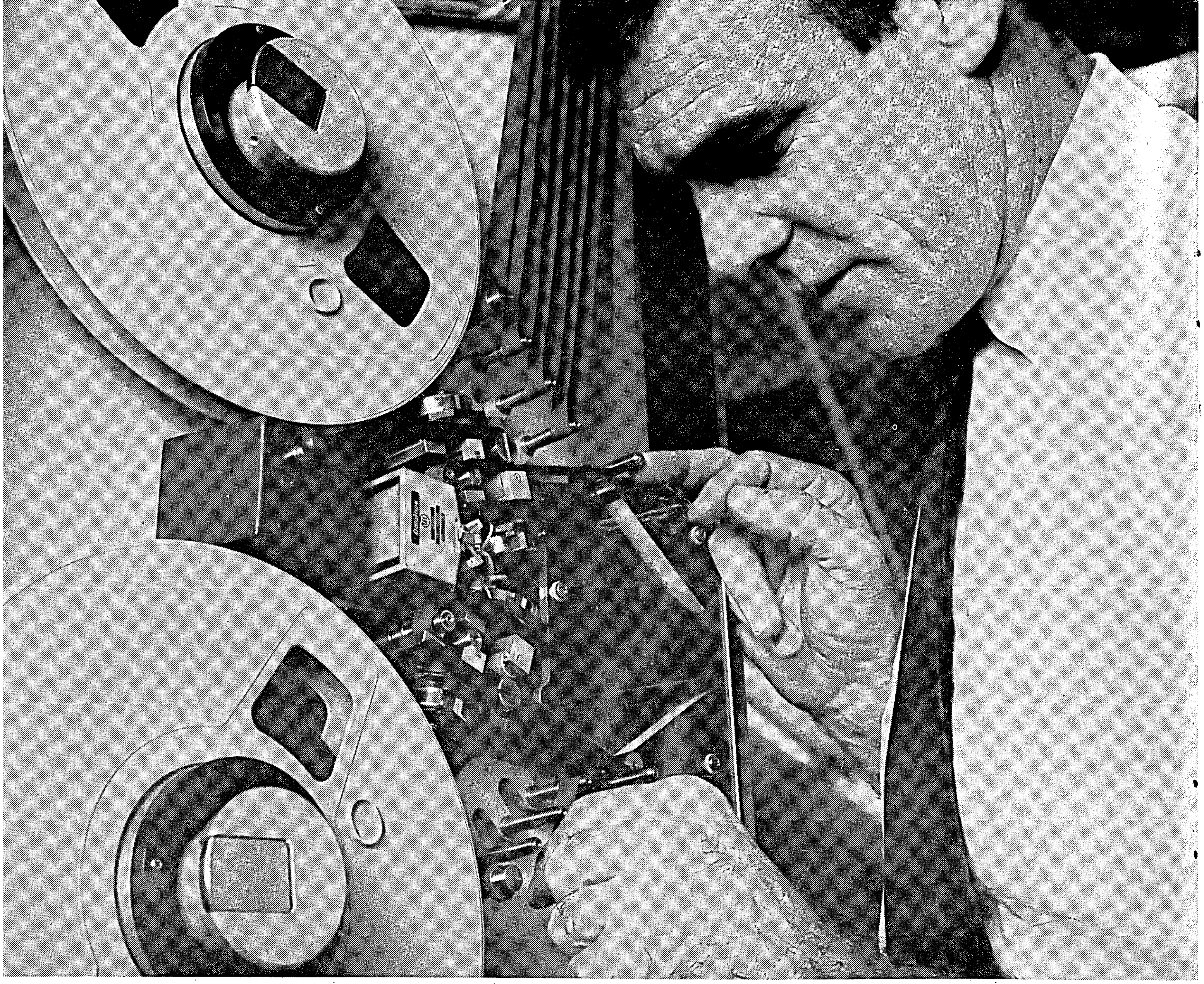
Pacific Data Systems, Inc., Santa Ana, Calif., manufacturers of the PDS 1020 and 1068 (see Aug. '63 *Datamation*), has been acquired by Electronic Assoc. Inc., Long Branch, N. J. The merger is said to extend EAI's capability in the process control field. PDS formerly was a subsidiary of Mesa Scientific Corp., Inglewood, Calif.

Three recent acquisitions by Control Data Corp. include Rabinow Engineering Co. of Washington, D.C., manufacturer of character recognition systems; Bridge Inc. of Philadelphia, makers of card punch and reader gear, and the Control Systems Div. of Daystrom Inc. The latter's plant is in LaJolla, Calif.

Applied Development Corp., a digidata manufacturing firm in Monterey Park, Calif., has acquired Kauke & Co. Inc., Santa Monica, analog data acquisition manufacturer. The two corporate identities will be maintained.

Acquisition by Litton Industries of Advance Data Systems has been announced. ADS manufactures revenue control systems for the transportation, entertainment, and distribution industries from its Los Angeles and Santa Barbara, Calif., plants. It is also in the dp peripheral gear field.

The analog and hybrid computer firm of Computer Systems Inc., Richmond, Va., has acquired Concord Control Inc. of Boston, a spinoff of MIT's Servo-Mechanisms Lab. Concord Control manufactures automated systems in machine tool control, cartography, and oceanography.



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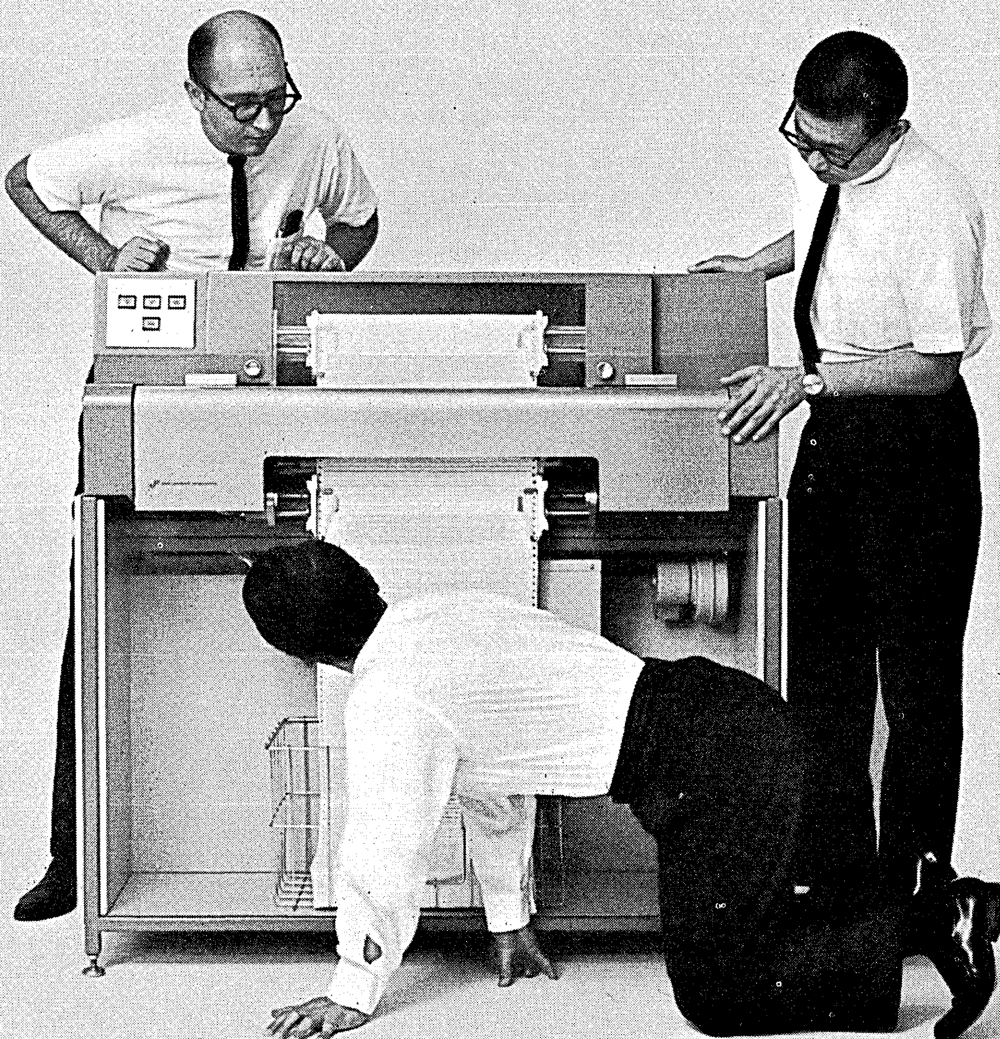
CIRCLE 32 ON READER CARD



NEWS BRIEFS

TRW COMPUTER DIV. MERGES WITH MARTIN MARIETTA

The TRW Computer Div. has joined with Martin Marietta's Electronic Systems and Products Div., Baltimore, Md., to form the Bunker-Ramo Corp., headquartered in the former's facilities at Canoga Park, Calif. The new firm will concentrate on total systems efforts in on-line control systems using electronic, mechanical and computing devices. TRW had been in military and process control computers, and the Martin division in information and command-control systems.

Ownership of the firm will be split 90/10 per cent in Martin Marietta's favor, TRW having the option to double its holdings. The latter also receives cash "approximating its investment in the computer operations." TRW plans to transfer ownership in international computer operations in France, England, and Japan to Bunker-Ramo, which begins with an employment of 2,500.

The firm is named for Board Chairman George M. Bunker, president of Martin Marietta, and Dr. Simon Ramo, vice chairman of TRW, who becomes B-R's president. Retaining vice presidencies with the new firm are Milton E. Mohr and Charles D. Manhart, who headed the TRW and Martin divisions, respectively, and Charles R. Allen, former vp-Finance for TRW's West Coast operations.

IBM DEVELOPS SOFTWARE FOR SCHEDULING TASKS

IBM has announced a 7090-94 program for the classic, mathematical, traveling salesman problem. Written by Michael Held, Richard M. Karp, and Richard Shareshian, and using a systematic procedure based on the dynamic programming technique devised by Richard Bellman of The RAND Corp., the program reportedly solves, directly and exactly, problems of up to 13 cities. It is "pretty good up to 20 cities," using successive approximations, Held says.

Sample problem: a salesman wants to visit a number of cities, stop once in each city, and return to his point of origin. Which route involves the shortest distance? Which requires the least amount of travel time? Any type of location or event can be substituted for *cities*, and dollars or hours for *distance*. Thus, the problem of setting up an assembly line for the production of different models or items can be solved with the program, as can, say, the determination of an optimum school bus route. Assembly line balancing? Not yet.

A precise solution to a 13-city problem is said to be solved in 14 seconds on a 7094, and an optimal answer to a 20-city problem in some five minutes. The 4,500-instruction program considers combinations instead of permutations. The program with table storage fills a 32K memory.

ADVANCED PROGRAMMERS, WOMEN EMPLOYMENT SEEN RISING

A continued need for programmers, especially those capable of advanced work, and an increase in the ratio of women programmers were forecast by users and manufacturers responding to a recent *Datamation* survey. Almost 70 per cent of respondents indicated a growing need for programmers, ranging from an anticipated 20 to 800 per cent; the remainder foresaw no change from the previous year. Median increase: 30 per cent. More need is seen for senior programmers and systems analysts than for junior programmers; Honeywell EDP cited a definite requirement for "qualified" beginners, while General Precision does not hire them.

Which category will be the most difficult to fill? Senior programmers and systems analysts, including software developers and systems programmers. These, of course, are the jobs with the greatest opportunities this year, according to respondents. Employers also state that many people who consider themselves ready for these positions do not meet the qualifications.

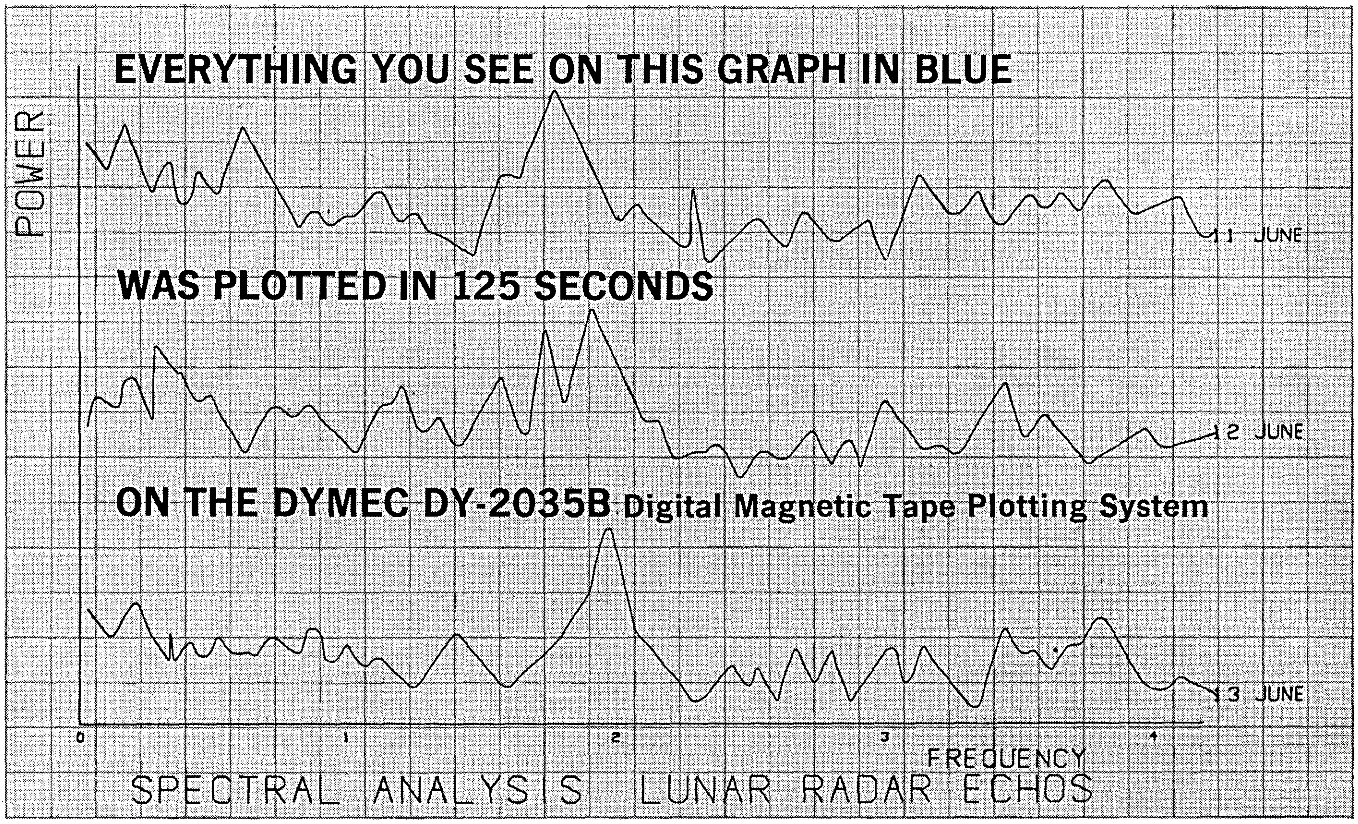
Of those answering the query, 76 per cent expected the ratio of women in programming to increase. "The only limitation is the number of qualified women applicants," a manufacturer stated. Presently, women comprise from three to 40 per cent of applicants for programming positions; most companies felt that this and the hiring ratios would increase over the next three years.

Regarding the effects of language and software developments, one respondent stated: "It is not expected that compilers, executive routines, and software in general will have any extreme effect on the 'people problem' in the next year. Over the next several years, the general improvement of software by manufacturers should result in a greater need for systems analysts while . . . less need for straight programmers." Or as another says, software developments "will allow us to concentrate on obtaining people who are problem solvers rather than coders." Said a third: "I believe that the quality of personnel needed to devise and improve this software will only make the quest for software development people more acute."

PHILCO DEMONSTRATES MULTI-FONT PRINT READER

Philco has demonstrated a general purpose print reader capable of recognizing different type faces on a single document, reading selected areas and ignoring others, and reading only the information meeting preprogrammed criteria—at up to 2,000 cps. Representative processing times reported are 6½ 3 x 5-inch cards, and three 8½ x 14-inch sheets per second. Output in variable formats can be on mag tape, paper tape, cards, printout, display, or combinations of these.

Integral with the CRT scanning unit is a control unit programmed by an "Auto-Load" system, a preprinted sheet with coded instructions which are recognized by the reader and stored in memory. For infrequently-read documents, the sheets can be pencilled in. Other features include unrestricted scanning formats, compensation for type misregistration, skew, and smudges, and the ability to accept a character only if it has gener-

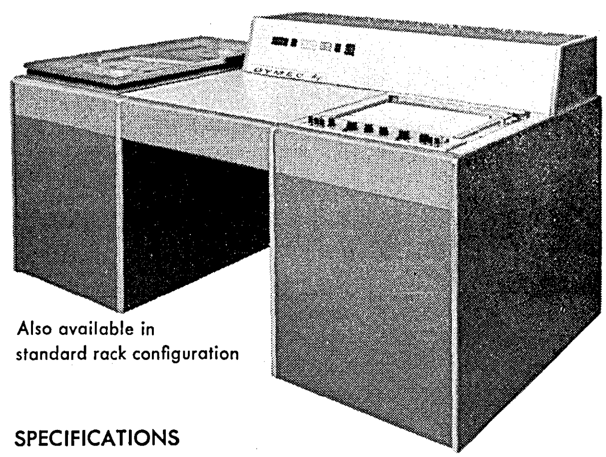


Fast plotting of digital computer data stored on magnetic tape is yours with the DY-2035B System which provides an average plotting speed of 4 inches per second, with slewing as fast as 20 inches per second.

You get more plots for less money. Besides plotting time, you save valuable computer time . . . tape for a 12-minute plot can be prepared in less than 1 minute in the computer. No expensive editing hardware is required. All system operating commands are written directly on the magnetic tape by the computer programmer. Programming documentation and card deck written in FORTRAN II are provided with the system. Check the graph above, including axis scaling and annotation . . . one typical example of the countless computations that the DY-2035B can put in more useful, meaningful x-y chart form.

Easy to use, too. Since all system operating instructions are on the plotting tape, operator responsibility is minimized . . . in fact, the system will operate unattended. An addressable tape search, forward or backward, simplifies finding the exact plot you want. Push a button and plot. Draw smooth graphs or point-plots.

Check the brief details here. Call your Dymec/Hewlett-Packard field engineer for more. Then think about moving fast . . . the DY-2035B does, and it's ready for delivery. More plots, faster, for less money.



Also available in standard rack configuration

SPECIFICATIONS

Plotting speed:	4"/second (slewing speed 20"/sec.)
Plotting accuracy:	Continuous curve, better than 0.2% of full scale; 0.075% with optional 30" x 30" plotter
Resolution:	Binary input: 12 bits of straight binary for each axis BCD (see options): 9999 counts each axis
X-Y recorder:	15" x 10" plot size, automatic chart advance available
Options:	BCD input, 30" x 30" x-y recorder Automatic symbol plotting, tape command (16 symbol printer) Automatic chart advance
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CIRCLE 34 ON READER CARD

ated the same recognition twice.

The company has announced contracts for four readers—three for the Post Office, and one for the Air Development Center in Rome, N.Y. Delivery of the latter is scheduled for this spring.

U. OF MIAMI COMPUTER AIDS DRUG RESEARCH

Correlation by a computer of statistical data on the effects of drugs on the brain, with resulting advances in drug research, have been announced by the Univ. of Miami (Fla.) Biometric Lab. Reportedly produced is the first statistically-proven relationships between EEG (brain wave) patterns and mental ability. Used was canonical correlation, in which all variables are considered simultaneously, instead of in pairs, by the computer. A by-product printout is a P value, indicating the probability that the results might have been a mathematical happenstance, rather than fact.

The university has begun construction of a 1.15-megabuck, five-story computing center, scheduled for completion before year-end. Hardware will include an IBM 7040, which will be shared by university research personnel and four federal agencies engaged in weather studies.

COMPUTER DESIGN FOR AEC STUDIED AT ARGONNE

Two computers, built in-house and sharing a central memory, are operating at Argonne National Lab, west of Chicago. The project is part of an AEC program for the design of computer systems to fill the needs of research scientists. The two machines are a modified version of George, which was built six years ago, and Flip, a larger-scale, faster computer which went operational early last year.

The two can work independently, one can supervise the other, or they can work parts of the same problem, comparing results before outputting. As many as seven computers or other devices can share the banked, central memory. Flip is capable of estimating the accuracy of numbers it generates—errors introduced during arithmetic operations by truncating—and supplying each number with an index of significance.

● Biomedical uses of computers continue: heart and circulatory system research by simulation with an analog

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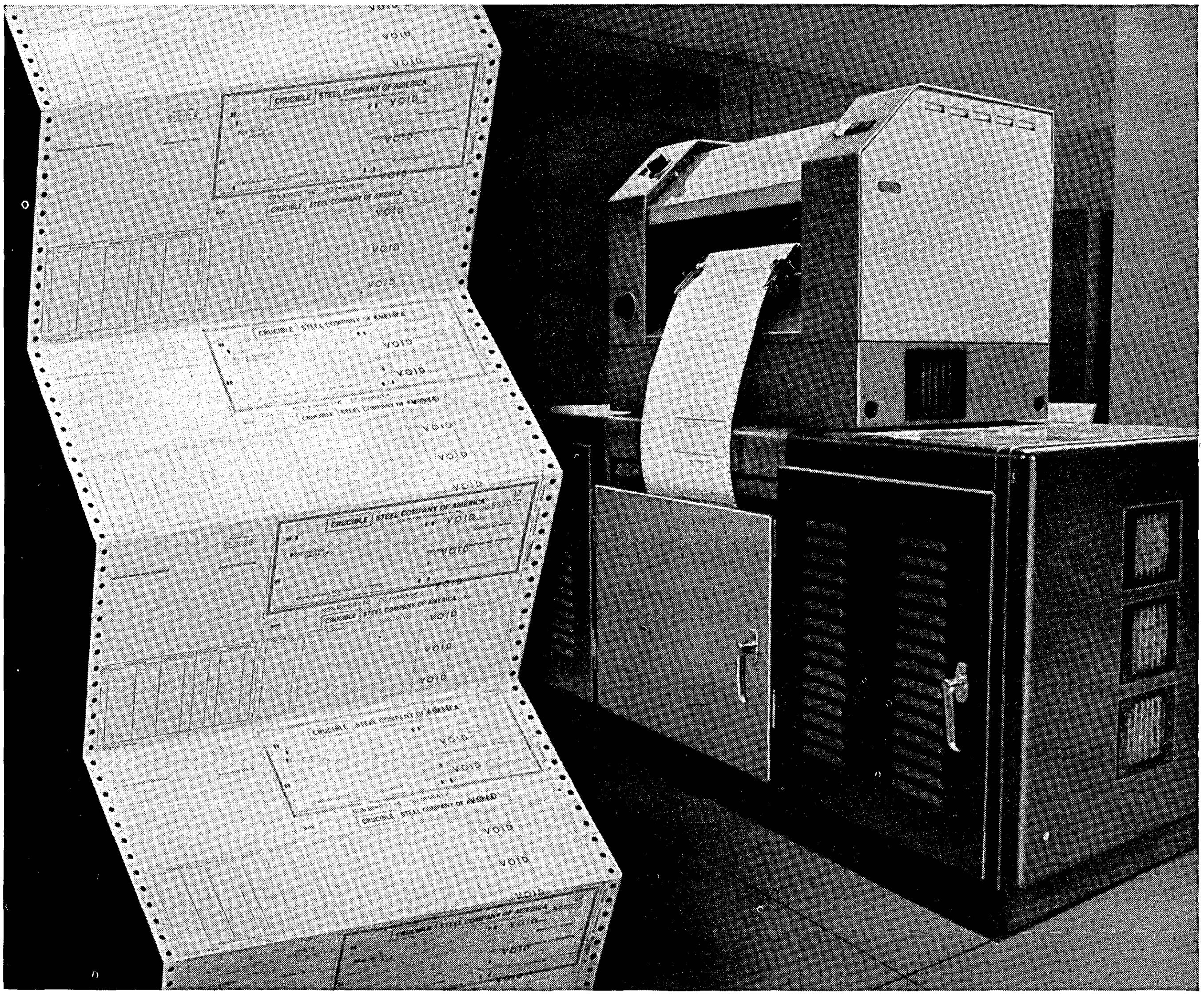

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CIRCLE 36 ON READER CARD

computer has been announced by Beckman Instruments, Richmond, Calif. Beckman research engineers have teamed with two physicians, Drs. John J. Osborn of the Presbyterian Medical Center in San Francisco, and James G. Defares of the Univ. of Leyden of The Netherlands. As part of a five-year simulation study, the hardware duplicated mechanical functions of heart chambers, blood volume, elastic properties of arteries, pumping characteristics of heart chambers, and blood flow. Confirmation of heart defect diagnoses and estimation of patient reaction to various types of treatment are reported.

● A course in "Automation of Library Processes and Procedures" will be offered this spring at the Western Reserve Univ. School of Library Science. Conducted by Miss LaVahn Overmyer, the course will include applications, hardware, costs, and current installations.

● An $800K computing center with an IBM 7094-I and two 1401's is scheduled by Northwestern Univ., Evanston, Ill. Hardware is to be used by the teaching and research staffs in the physical and social sciences. The '94 replaces a 709; other computers on campus include an LGP 30, two PACE analogs, and an analog system partly designed by the Aerial Measurements Lab staff.

● A call for papers has been issued by the Conference on Data Acquisition and Processing in Medicine and Biology. Deadline is April 15. To be held on July 13-15 at the Univ. of Rochester, New York, the theme is "Medical Literature and Data—Its Acquisition, Processing and Retrieval."

● A 3.3-megabuck, follow-on contract for the third Q-11 computer to be incorporated into the Air Force's 473L command-control system has been awarded to General Precision's Librascope Div., Glendale, Calif. The first two Q-11's (designated AN/FYQ-11 by the Air Force, L-3055 by Librascope) will be installed in the Pentagon for real-time control interpretation, and display of information on the AF's global resources.

● General Telephone & Electronics has combined its duobinary transmission system with speech scrambling equipment to transmit voice commu-

NEWS BRIEFS . . .

nication at 2,400 bps. Feasibility testing was for six months across a 3,300-mile path between the U.S. and Europe. For business data communication, the firm is breaking its single data stream into 16 channels of 150 bits each, thus retaining its speed capability but adapting it to slower devices such as teletypewriters.

● The Detroit, Mich., Police Dept. has installed a 1401 for administrative dp purposes . . . the storing and updating of records, and the preparation of reports. Proposed future applications include the matching of latent fingerprints found at the scene of a crime against a master file.

● Computer installations in Europe have increased by 150 per cent during the past year, according to the Diebold Group Inc., and machines on order have jumped 66 per cent. IBM accounts for 54 per cent of installations, the firm estimates.

● Software for the solution of design engineering problems has been announced by IBM. It may be used with any IBM computer. Automated Design Engineering applies primarily to custom or product design which involves variations of a standard product line. Fed information from customer orders, the computer takes care of design logic, equations and computations, design checking, and the generation of engineering paperwork.

● A three-year, approximately two-megabuck contract for dp services has been awarded to Computer Applications Inc., New York, for NASA's Launch Operations center near Cape Kennedy, Fla. Priming the administrative and management services contract is Ling-Temco Vought Inc. Current hardware includes a 1401 and 1410.

● The common stock of Computer Sciences Corp. have been listed on the American Stock Exchange. The El Segundo, Calif., firm announces revenues of 3.3 megabucks and net earnings of $392K for the fiscal year ending March 31, 1963. Also disclosed: plans to open an office in Washington, D. C.

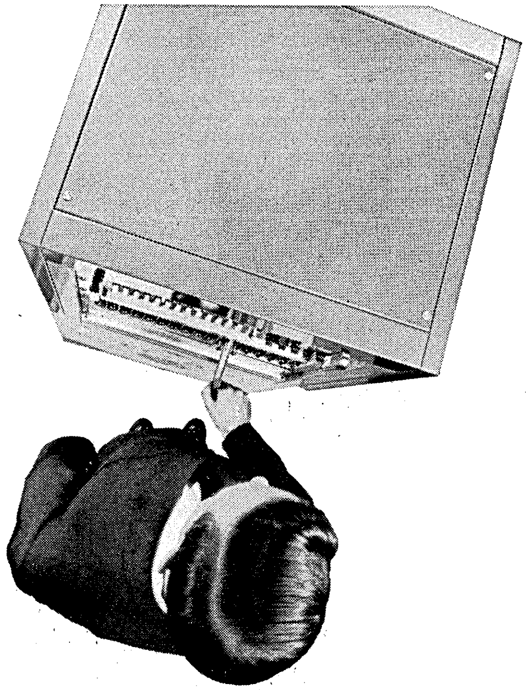
● A 1.5-megabuck, follow-on contract for software has been awarded to ITT's Data and Information Systems Div. by the Navy. Programming is for shipboard use of existing navigational, operational, and tactical plans.

● The German Weather Service at Offenbach/Main has contracted for delivery of a CDC 3600. In addition to prognostications, the hardware will prepare weather maps and time-tracks for aircraft approaching and departing Europe, and be used for long range forecast research. The configuration will include a 160-A.

● A $500K contract for TM-4 mag tape units to be used with the SDS 900 series computers has been awarded to Ampex Computer Products, Culver City, Calif., by Scientific Data Systems Inc., Santa Monica, Calif.

● The recently-introduced Honeywell 200 has been incorporated into a business dp programming course at Boston Univ. The 200 joins IBM 1400 series hardware. Other courses are programming for the 1620, and programming languages, which gets into FORTRAN, ALGOL, and COBOL.

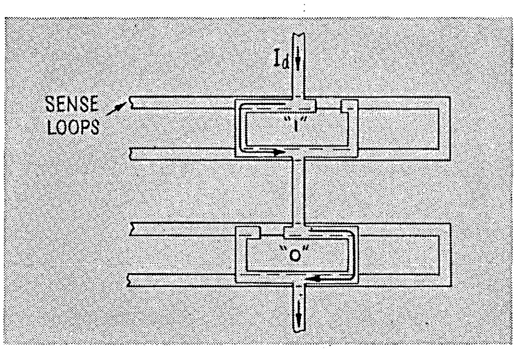
● Two-week summer courses in computer sciences have been announced by the Univ. of Michigan's College of Engineering. Running from June 8 to 19 are the following: Introduction to Digital Computer Engineering; Digital Computers in Real Time; Automata Theory: advanced concepts in information processing systems; Automatic Programming: machine and program organization; and Numerical Analysis. Other one- and two-week courses are available.



this man is plugging in 1,920 NDRO bits

He can plug in 64, 30-bit words of read-only data in seconds or change a whole 1024-word fixed-data storage routine in minutes.

We're talking about Fabri-Tek's PERMACARD memory system, the new concept of fixed or "read only" data storage. The PERMACARD system uses no ferrite cores, no magnetic slugs, no capacity elements, no diode matrix memories. It's a pure and simple induction system that has fixed constants and is free from chance of alteration due to faulty read-restore operations. It's insensitive to temperature, noise and transients.



Close-up of PERMACARD system bit storage.

Memory capacities are available to suit your requirements. Typical cycle time is 1 usec and access time is 0.5 usec. The PERMACARD system memory cards are economical plug-in printed word line arrays.

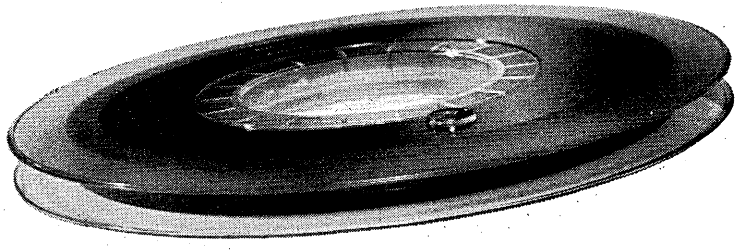
Natural applications for the PERMACARD system are: microcommand or microinstruction storage, fixed subroutine storage, control memories, bootstrap memories, look-up tables, command translations, and any combination of these. The speed and economy of the PERMACARD system coupled with its great flexibility suggests a broad variety of special uses—radar display storage for permanent targets, A to D conversion, fixed automation and materials handling instructions—these are only a few places where the PERMACARD system can be applied.

Find out more about this fresh approach to Non-Destructive-Readout, fixed data storage. Write, call or wire Robert E. Rife, Fabri-Tek, Incorporated, Amery, Wisconsin. Phone: CO 8-7155 (Area 715). TWX: 715-2920900.

FABRI-TEK

EXECUTIVE OFFICES: FOSHAY TOWER, MINNEAPOLIS 2, MINNESOTA

CIRCLE 39 ON READER CARD



This is a reel of new, **improved** Computape. What do we mean by improved?

Longer wear, less static build-up, greater reliability than ever before.

Skeptical? Allow us to make a suggestion:

Test it yourself. Against <u>any other</u> tape.

If that doesn't convince you, you're just plain stubborn.

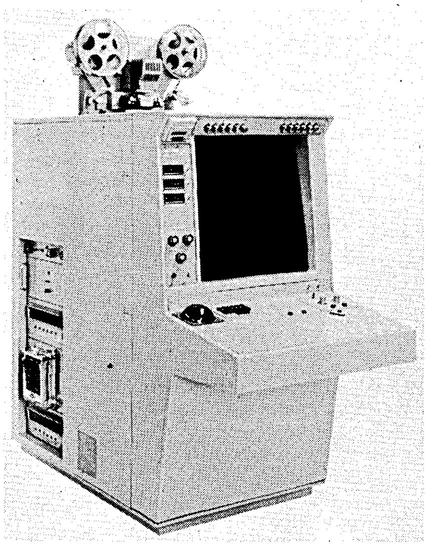
COMPUTRON INC.
122 CALVARY STREET, WALTHAM, MASSACHUSETTS

CIRCLE 40 ON READER CARD

NEW PRODUCTS

film reader

The Boscar model S is a transistorized, semi-automatic reader designed for reduction of coordinate locations on



film to digital forms suitable for computer entry. BENSON-LEHNER CORP., 14761 Califa, Van Nuys, Calif. For information:

CIRCLE 200 ON READER CARD

search/control unit

The 859 has been designed for use with the 858 time code generator/reader. Together, the units form a system which automatically searches and locates time positions or addresses on mag tape. Four operating modes: continuous, single cycle, search to start, and off. ELECTRONIC ENGINEERING CO., Box 58, Santa Ana, Calif. For information:

CIRCLE 201 ON READER CARD

mag tape system

The 5900 is comprised of four functional subassemblies which include tape transport with read and/or write head(s), control panel, read and write electronics. The system can be controlled locally or remotely and is completely IBM tape compatible. COOK ELECTRIC CO., DATA-STOR DIV., 8100 Monticello Ave., Skokie, Ill. For information:

CIRCLE 202 ON READER CARD

recorder/reproducer

The GL-2810, particularly applicable for data reduction or data monitoring where machine work is heavy, handles continuous mag tape loops at any of six tape speeds from 60 through 1⅞ inches per sec. CONSOLIDATED ELECTRODYNAMICS CORP., 360 Sierra Madre Villa, Pasadena, Calif. For information:

CIRCLE 203 ON READER CARD

IBM programs

These CPM and CPM-Time-Cost Optimization programs have been developed for IBM 1401, 1410, and 1460. The programs are single phase and have error-detection features. The program is written for a 16K machine with on-line card reader/punch and printer with three tape drives. THE ASSOCIATED DATA PROCESSING CO., 98 Pulaski Ave., Carteret, N.J. For information:

CIRCLE 204 ON READER CARD

cathode ray tube

The M1156 features shortened tube length and a three-inch optically flat face which minimizes parallax error and utilizes post acceleration to optimize light output and maintain good deflection sensitivity. ELECTRONIC TUBE AND INSTRUMENT DIV., GENERAL ATRONICS CORP., 1200 E. Mermaid Lane, Philadelphia, Pa. For information:

CIRCLE 205 ON READER CARD

magnetic head protection

Havar tape is a cobalt base, non-magnetic, corrosion-resistant tape which is furnished on plastic spools and can be passed continuously between the mag tape and computer head at a slow rate of speed, helping minimize wear on read/write heads. HAMILTON WATCH CO., Lancaster, Pa. For information:

CIRCLE 206 ON READER CARD

dp accessories

The 1004 control panel and 1004 manual self-contacting wires have been developed for use with Univac equipment installations. Wires have the "D-tent" feature and are color coded by lengths ranging from five inches to 27 inches. MAC PANEL CO., High Point, N. C. For information:

CIRCLE 207 ON READER CARD

data processing cards

These cards are available with either consecutive or repetitive printed numbers, gang or consecutive prepunching, multi-color over-printing or back printing, tinting and special scores and are offered in 51-, 80- or 90-column size, and with scored stubs from ½-inch to 1⅞ inches at either end. AMERICAN BUSINESS SYSTEMS INC., 2929 B Street, Philadelphia, Pa. For information:

CIRCLE 208 ON READER CARD

analog x-y plotter

The Plotamatic 800 features full scale accuracies of 0.15% and repeatability of 0.1%. The 17 voltage ranges include 0.5 through 500 mv/inch, and one through 100 v/inch, with continuous vernier on all ranges. DATA EQUIPMENT CO., 2126 S. Lyon St., Santa Ana, Calif. For information.

CIRCLE 209 ON READER CARD

tape transport

The MT-75 operates at standard tape speeds of 60 and 75 ips, with a 2½-minute rewind. Data transfer rates are to 60 kc (bcd). In addition to IBM packing densities of 200, 556 and 800 bpi, other formats using ½-inch and one-inch tape can be accommodated. POTTER INSTRUMENT CO. INC., 151 Sunnyside Blvd., Plainview, L. I., N. Y. For information:

CIRCLE 210 ON READER CARD

kimball high speed reader

This on-line punched tag reader reads data photoelectrically into a computer at the rate of 1,200 tags a minute and eliminates the need for punched cards in mass volume retail dp systems. LITTON INDUSTRIES, BUSINESS MACHINES GROUP, 555 Mitchell St., Orange, N.J. For information:

CIRCLE 211 ON READER CARD

electronic filing system

This new system is composed of 1302 disc storage units; up to five of these units, each containing nearly a quarter of a billion characters of information, can be linked to a computer. An item of information can be retrieved "in less than 2/10 of a second." IBM CORP., DP DIV., 112 E. Post Rd., White Plains, N. Y. For information:

CIRCLE 212 ON READER CARD

digital clock

The DY-2509A provides time information as a continuous 24-hour visual display and as an electrical output available on demand for recording. The clock is completely transistorized and features front access to all logic

NEW PRODUCTS . . .

circuitry. DYMEC., DIV. OF HEWLETT-PACKARD CO., 395 Page Mill Rd., Palo Alto, Calif. For information:

CIRCLE 213 ON READER CARD

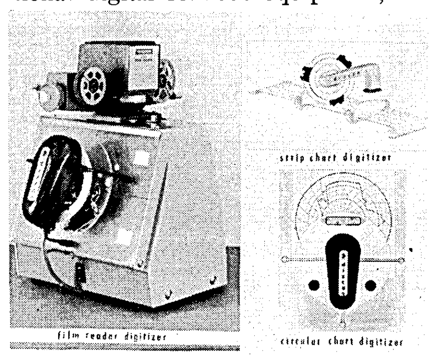
gp print reader

This system is able to read typed or printed pages without the use of stylized or magnetic ink letters or numbers. Also featured: multiple-font reading by multi-feature extraction masks; automatic height sensing; ability to read misregistered or skewed lines of print; compatibility with all known digital data processing systems. Flying spot scanning can be accomplished at a rate up to 2000 cps. PHILCO CORP., Tioga & C Sts., Philadelphia, Pa. For information:

CIRCLE 214 ON READER CARD

graphic data digitizer

This device reads data from 16 mm film and renders an output in digital form. The output will operate conventional digital readout equipment, i.e.



film reader digitizer / strip chart digitizer / circular chart digitizer

tape or card perforators, digital printers and plotters. MACLEOD INSTRUMENT CORP., 4250 N.W. 10th Ave., Ft. Lauderdale, Fla. For information:

CIRCLE 215 ON READER CARD

non-linear programming system

This system, developed for use with optimization and simulation programs, handles non-linear constraints, provides automatic step size adjustment, and searches for a feasible starting point when the suggested starting point is non-feasible. MANAGEMENT DECISIONS INC., 5619 Fannin St., Houston, Tex. For information:

CIRCLE 216 ON READER CARD

computer program

Perforated tapes, prepared by a computer-control programming system known as ADAPT, automatically directs the machining of metal parts by numerically controlled machine tools through use of the Univac III. UNIVAC, DIV. OF SPERRY RAND CORP., Sperry Rand Building, New York 19, N.Y. For information:

CIRCLE 217 ON READER CARD

The Language's Prayer

Our FORTRAN who art from IBM

Hallowed be thy name, thy COBOL come, thy FACT be done

At RAND as it is in NASA.

Give us this day our daily ALGOL and assist us in linear programming

As we assist those in list processing and theorem proving.

Lead us not into FAP, TAC, and AUTO-CODER

But deliver us from FLOP.

For thine is the JOVIAL, the MADCAP, and the NELIAC

Forever and ever LDQ A.

ROBERT A. BAKER
Ft. Knox, Kentucky

Book REVIEW

COMPUTER PROGRAMMING CONCEPTS

The Teacher-Student Approach to . . . COMPUTER PROGRAMMING CONCEPTS. Vol. 1, Reference Material. Vol. 2, Problem Exercises. ***Written by Robert E. Smith, Control Data Corp., with the assistance of Paul Voight and Robert Hed of the St. Paul-Minneapolis public schools. Published by Control Data Corp.***

These two volumes purport to be an introductory text in computing, aimed at high school math and science teachers. They are all that, and more, since they include much good material on problem solving, mathematics and computer operation. A unique feature is an offer to run programs produced by organized groups, such as a high school math club.

In a brief introduction, the text covers the structure of the computer, sequencing, flowcharting, binary notation, and machine language coding (these subjects are expanded in Vol. 2 somewhat). Then FORTRAN is introduced, and the balance of the work is done in that language. The object machine is the CDC 160A.

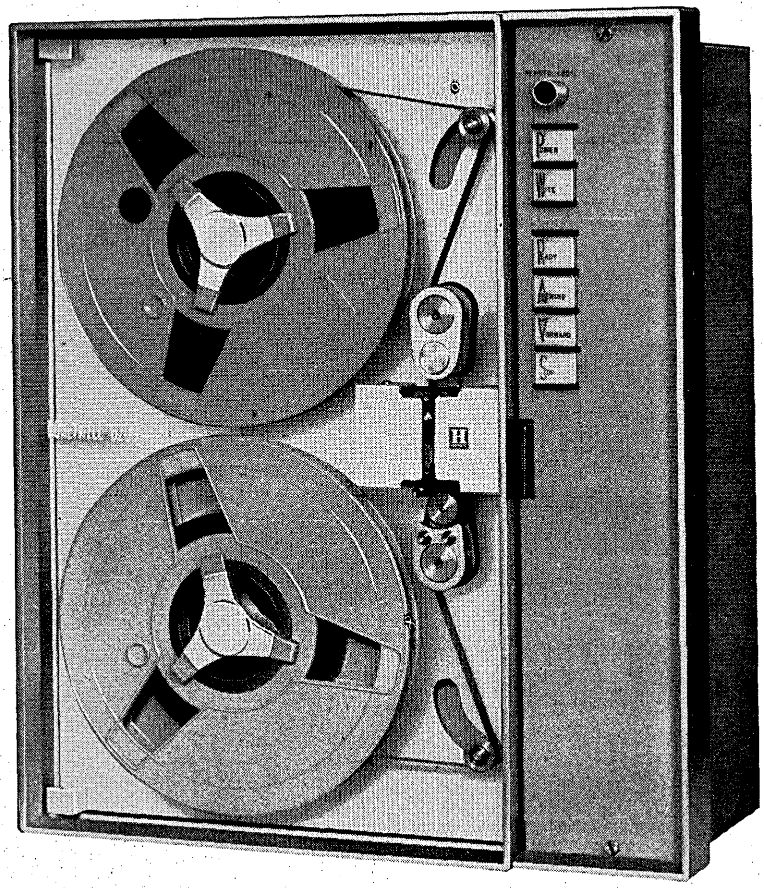
A major flaw in these books is a complete lack of references. The reader is told, for example, to "study the history, background, uses and design of random number generators now in use" without any clue as to where to get started.

Again, many an opportunity is lost to drive home the difference between hack programming and competent work. For example, the reader is shown that

$$y = \frac{x+128}{48}$$

is an adequate formula for calculating the cube roots of numbers, provided that x lies between 62.1 and 65.9 and provided that three-digit accuracy will suffice. This is all well and good, but the important lesson is to buffer such a routine with a validity test on the data. The FORTRAN code should also be filled with comments cards that say REMEMBER WE GET ONLY THREE DIGITS OF ACCURACY FROM THIS.

These are not books for which a review should harp on typos. They are a significant step forward in computer education. Control Data is to be congratulated for sponsoring the teacher training courses that led to these texts.



HOW CAN YOU USE THE HONEYWELL 6200?

This is the Incremental Digital Tape Recorder which recorded 6×10^8 asynchronous bits without a single dropout or spacing error.

Where can you use such an ideal device for acquisition of medium speed (100 bits per second) asynchronous digital data? The 6200 packs 200 bits per inch with uniform density regardless of input speed variations. Send for complete information today!

DATA HANDLING SYSTEMS

Honeywell

TO: W. B. Wallace,
Honeywell, Denver Division, Denver, Colorado 80210

☐ Send me complete specifications on the Honeywell 6200.

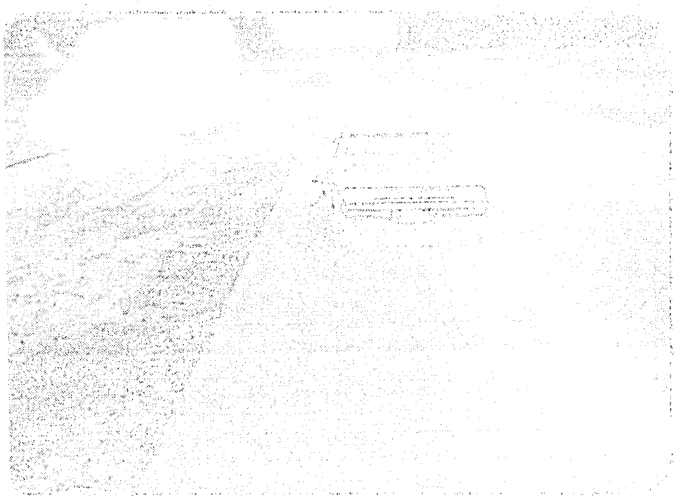
☐ Please comment upon this possible application: ______________

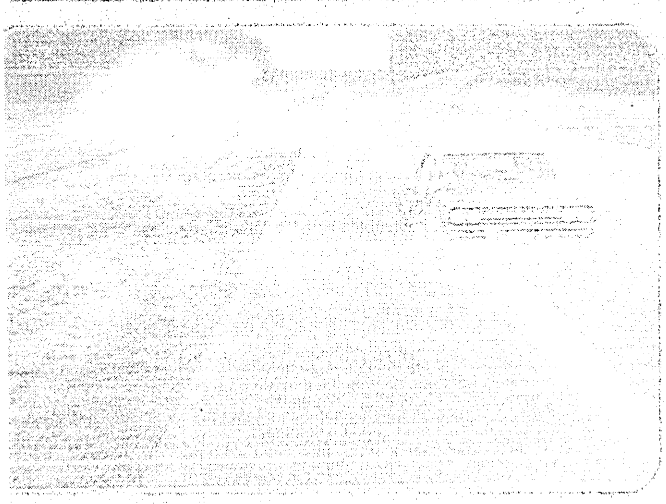
NAME ______ POSITION ______

COMPANY ______

ADDRESS ______ ZIP CODE ______ TELEPHONE ______

CIRCLE 46 ON READER CARD





One of a series briefly describing GM's research in depth

HOW A CAR RESPONDS TO CROSSWINDS

A rocket engine is being used by an engineering research group at our Laboratories to study the effects of crosswinds on the directional behavior of passenger cars.

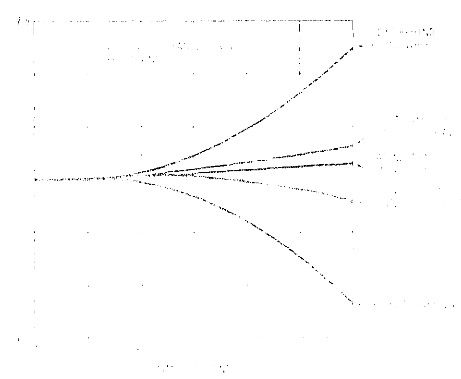
Mounted on the side of a full-size car, the lightweight engine can exert a maximum thrust of 200 pounds . . . a force equivalent to a 25-mph crosswind hitting a vehicle traveling 60 mph. Because a vehicle's aerodynamic center of pressure is a function of body shape, engineers—simply by shifting rocket engine location—have been able to evaluate the effects of body changes on a car's response to crosswind disturbances.

This flexibility of location is one of several advantages of the new system over previous attempts to study crosswind effects. Both force and time of the thrust is accurately controlled for each test run.

An important result of this work has been the experimental verification of theoretical equations of lateral motion. These equations form a mathematical model of the vehicle—a model we are now using in computer simulation of car handling.

This directed interplay of theory, experiment and analysis is another example of how GM engineers are working to find a better way—through research in depth.

General Motors Research Laboratories
Warren, Michigan

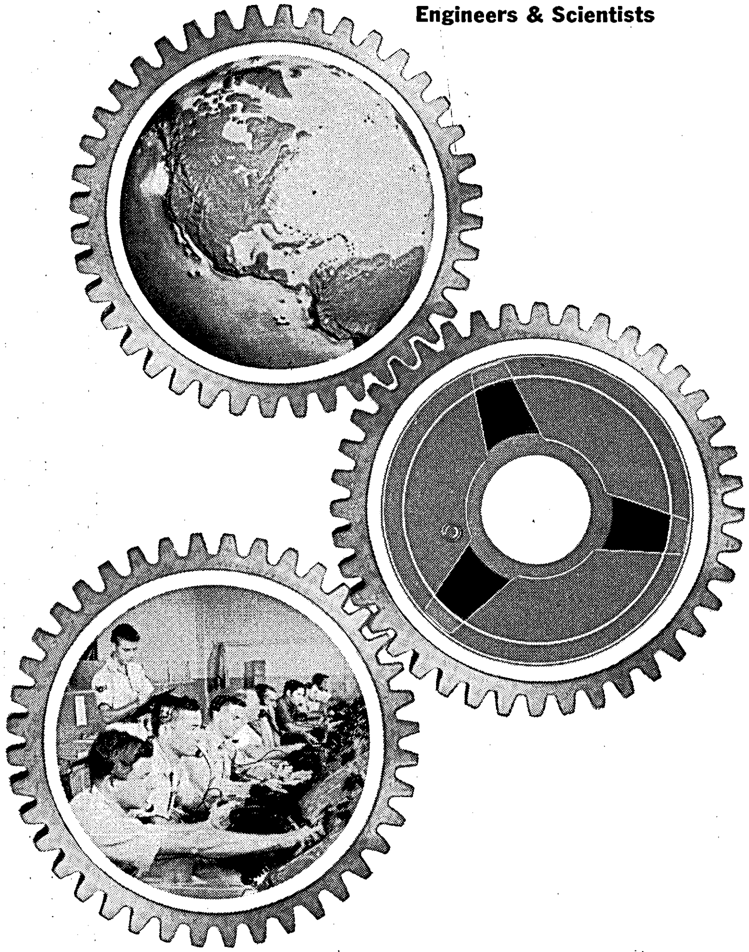


Path deviation of a vehicle traveling 60 mph for various centers of pressure.

CIRCLE 50 ON READER CARD

DATAMATION'S FEATURE INDEX
JULY - DECEMBER, 1963

Engineers & Scientists



AUTOMATING THE GLOBAL RANGE CONTROL NETWORK

A new dimension in fast-response control and global reporting of space vehicle and missile performance is now being engineered by Pan Am's Guided Missiles Range Division.

A centralized range instrumentation control system (RICS) will automate range support on the Atlantic Missile Range and link with other national ranges on a world-wide basis. Basic to this new system will be the Central Control Processor at Cape Kennedy. This master computer will accept data from all land, air and shipborne stations down-range—and eventually from communications satellites (now in the planning stage). It will provide real-time separation and recording of data, and process necessary information and commands.

In its full scope, RICS offers the master "space traffic" management capability needed to maximize the success of range support for complex space missions in the near future: orbital rendezvous and docking, lunar orbits, manned lunar flights, and interplanetary probes. The system will give push-button control of instrumentation, communications, assignment, status, data selection for real-time biomedical evaluation and range safety and post-flight analysis, security code changing, function transfer, and vehicle control to alter in-flight missions.

On this and other sophisticated space programs, assignments are immediately available to electronic engineers and physicists with broad systems and planning backgrounds in: pulse & CW radar/telemetry/optics/infrared/data handling/communications/closed circuit TV/frequency analysis/command control/underwater sound/timing/shipboard instrumentation/meteorology.

Write in confidence to Manager—Professional Employment, Dept. 21B

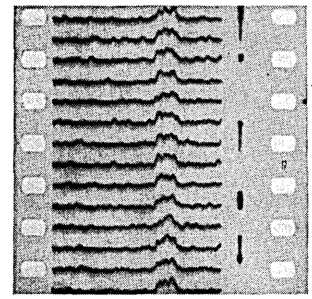
PAN AM

GUIDED MISSILES RANGE DIVISION

PAN AMERICAN WORLD AIRWAYS, INC.
P. O. BOX 4465, PATRICK AIR FORCE BASE, FLORIDA

An Equal Opportunity Employer

CIRCLE 78 ON READER CARD



5000 POINTS PER SECOND

INFORMATION INTERNATIONAL, INC., Maynard, Mass., has developed a completely automatic computer film reading system which can read film at the rate of approximately 5,000 points per second. Scientific data recorded on 16, 35 or 70 mm film can be read completely automatically and printed out in the form of numerical listings or recorded in digital form on magnetic tape for further processing and analysis. The film reading system is based on three major elements: A general purpose digital computer, together with a visual display scope; a Programmable Film Reader (PFR-1); and computer programs for using the computer and film reader.

THE FILM READING PROCESS. The film reading process involves the scanning of film by a rapidly moving light point on the visual display scope. The output of this scanning operation is detected by a photosensitive device in the film reader and relayed to the digital computer for further processing and analysis. In addition to translating the data itself into a more desirable format, the film reading system can also furnish analyses of the data as may be required.

INFORMATION INTERNATIONAL is the only commercial firm supplying fully automatic computer film reading systems. We do essentially two things. We develop and manufacture film reading systems for clients to use at their own facilities (as, for example, in the case of radar film reading systems we have developed for Lincoln Laboratory and the U.S. Air Force). And we furnish services for reading films which are sent to us for processing (as in the case of oceanographic current meter film). A brochure describing the film reader and film reading systems we have developed is available on request.

INFORMATION INTERNATIONAL INCORPORATED

P. O. BOX 106 • MAYNARD, MASS.

CIRCLE 54 ON READER CARD

NEW LITERATURE

BINARY ARITHMETIC: 3½-hour programmed course, available in 80-page book, teaches number systems; conversion from tally to decimal, octal, and binary, decimal to binary, and binary to decimal; sight conversion; binary addition and subtraction; and binary coded decimal. Price is $7.50. EDP TRAINING, BASIC SYSTEMS, INC., 2900 Broadway, New York, N.Y.

INFORMATION RETRIEVAL: Describes inexpensive method, employing peekaboo principle for filing and finding. FIND-IT, P.O. Box 36074, Wilshire-La Brea Station, Los Angeles, Calif. For copy:
CIRCLE 130 ON READER CARD

REPETITIVE MACHINE: Class 5000, designed for repetitive writing of names, addresses and other business data, is described in this illustrated booklet. ADDRESSOGRAPH-MULTIGRAPH CORP., 1200 Babbitt Rd., Cleveland, Ohio. For copy:
CIRCLE 131 ON READER CARD

PULSE HEIGHT ANALYZER: Illustrated bulletin highlights the PDP-5 computer in a pulse height analysis configuration. DIGITAL EQUIPMENT CORP., Maynard, Mass. For copy:
CIRCLE 132 ON READER CARD

DP ACCESSORIES: Catalog contains company's complete lines of tab card files, open reference files, control panel and material storage cabinets, card punch desk files, trays, transportation and sorting equipment, semi-active card storage, shipping containers, miscellaneous products as well as a complete price list. SYSTEMS SALES CO., 13 Broad St., Binghamton, N.Y. For copy:
CIRCLE 133 ON READER CARD

COMPUTER INPUT AUTOMATION: This illustrated report details the four-way application of a Farrington optical reader to the accounting and dp requirements of the Northern Illinois Gas Co. FARRINGTON MANUFACTURING CO., 850 3rd Ave., New York, N.Y. For copy:
CIRCLE 134 ON READER CARD

GENERAL CATALOG: Detailed in this 80-page brochure is the company's complete line of accessories, cards, comparators, keyboards, key punches, military specification equipment, printers, punches, readers, reproducers, tape and verifiers. SOROBAN ENGINEERING INC., P.O. Box 1717, Melbourne, Fla. For copy:
CIRCLE 135 ON READER CARD

TELEMETRY & COMMUNICATION: 20-page book gives complete technical data on this company's line of solid-state advanced telemetry receivers and other equipment including de-

NEW LITERATURE . . .

modulators, spectrum display units, recording converters, and preamplifiers. VITRO CORP. OF AMERICA, 261 Madison Ave., New York, N.Y. For copy:
CIRCLE 136 ON READER CARD

PCM DECOMMUTATION SYSTEM: Data sheet #126 gives full description, features and specifications of the 610B universal PCM decommutation system. TELEMETRICS INC., 12927 S. Budlong Ave., Gardena, Calif. For copy:
CIRCLE 137 ON READER CARD

DIGITAL SYSTEMS POLICY: Highlights company's policy of free digital systems engineering and checkout programming. Described are several currently operational systems. SCIENTIFIC DATA SYSTEMS INC., 1649 17th St., Santa Monica, Calif. For copy:
CIRCLE 138 ON READER CARD

DATA TRANSMISSION: Pamphlet includes complete performance figures, circuit description, block diagrams and features of the 25A data transmission system. LENKURT ELECTRIC CO. INC., 1105 County Rd., San Carlos, Calif. For copy:
CIRCLE 139 ON READER CARD

INDEX: WADEX is a new guide to scientific literature in the field of applied mechanics. The 600-page index was prepared by an IBM 1401. Book is priced at $5. AMERICAN SOCIETY OF MECHANICAL ENGINEERS, 345 E. 47 St., New York, N.Y.

INTEGRATED BANKING: This brochure describes the services of the Beverly Bank of Chicago, including use of one customer number for all transactions, utilizing a GE-225. GENERAL ELECTRIC CO., COMPUTER DEPT., Deer Valley Park, Phoenix, Ariz. For copy:
CIRCLE 141 ON READER CARD

SERVICES & FACILITIES: Data Processing/List Maintenance/Order Fulfilment details the capabilities and facilities of this company. Illustrated is equipment used, and typical jobs done for dp clients. O. E. MCINTYRE INC., SERVICE BUREAU DIV., 375 Park Ave., New York, N.Y. For copy:
CIRCLE 142 ON READER CARD

GP COMPUTER: A 16-page manual describes the 2100 computer system features, organization of its CPU, and software and services available. ADVANCED SCIENTIFIC INSTRUMENTS, 8001 Bloomington Freeway, Minneapolis, Minn. For copy:
CIRCLE 143 ON READER CARD

NUMERICAL CONTROL: Four-page booklet describes the DynaPath-20 control system for plotter-verifiers and drafting machines. Includes applications and system capabilities. INDUSTRIAL CONTROLS DIV., BENDIX CORP., 8880 Hubbell Ave., Detroit, Mich. For copy:
CIRCLE 144 ON READER CARD

AUTOMATIC READER: This 52-page report is a study of the possibility of the reading of handwritten numbers by machines. Possibilities have been suggested, and conditions formulated. "Automatic Reading of Digits" costs $3. NETHERLANDS AUTOMATIC INFORMATION PROCESSING RESEARCH CENTRE, 6 Stadhouderskade, Amsterdam, Netherlands.

DELAY LINE PRIMER: "A-B-C's of Magnetostrictive Delay Lines" includes a glossary, drawings of wave shapes under various modes of operation, discussion of RZ and NRZ recording methods, and summary of meausurement practices. FERRANTI ELECTRIC INC., LIGHT EQUIPMENT DIV., Industrial Park No. 1, Plainview, L.I., N.Y. For copy:
CIRCLE 145 ON READER CARD

I+A(I): This 20-page brochure describes the firm's capabilities in management science, economics, math and statistics, computer services and programming application, as well as a bibliography of its problem-solving literature. C-E-I-R INC., 1200 Jefferson Davis Highway, Arlington, Va. For copy:
CIRCLE 146 ON READER CARD

TELEMETER APPLICATION: Bulletin M1 covers industrial applications of digital control and telemetering, and explains the theory and economics of time division multiplex. Applications include hydroelectric power plants, refineries, transcontinental microwave communication. MOORE ASSOC., 893 American St., San Carlos, Calif. For copy:
CIRCLE 147 ON READER CARD

SYSTEMS COMPUTER: Bulletin 4110 describes the special-purpose 420 computer, including specs, command list, operation theory, and organization. BECKMAN INSTRUMENTS INC., SYSTEMS DIV., 2400 Harbor Blvd., Fullerton, Calif. For copy:
CIRCLE 148 ON READER CARD

PAPER TAPE I/O: Specs of the series 1010 Tapewriter and Tapewriter-Reader systems are in this eight-page brochure. The former prints and punches on 5, 6, 7, or 8-level tapes. NAVIGATION COMPUTER CORP., Valley Forge Industrial Park, Norristown, Pa. For copy:
CIRCLE 149 ON READER CARD

the 13th in a series which dates back to June '62, concerns itself with Kirtland AFB in New Mexico where the Air Force exercised a purchase option on a CDC 1604 pursuant to a GAO recommendation. The action will produce $1,780,000 in savings for the taxpayer over the next three years, the GAO report contends.

BILL PROPOSED TO BAR BANKS FROM SERVICE BUREAU FUNCTIONS

A long-smouldering issue within the computer industry promises to burst out into the open with the introduction of a bill in Congress which would bar banks from engaging in service bureau activities. The bill -- H.R.9548 -- is sponsored by Rep. Abraham J. Multer, a Democrat from Brooklyn's 13th district, who claims the proposed legislation would end "a serious encroachment" by banks on the accounting profession.

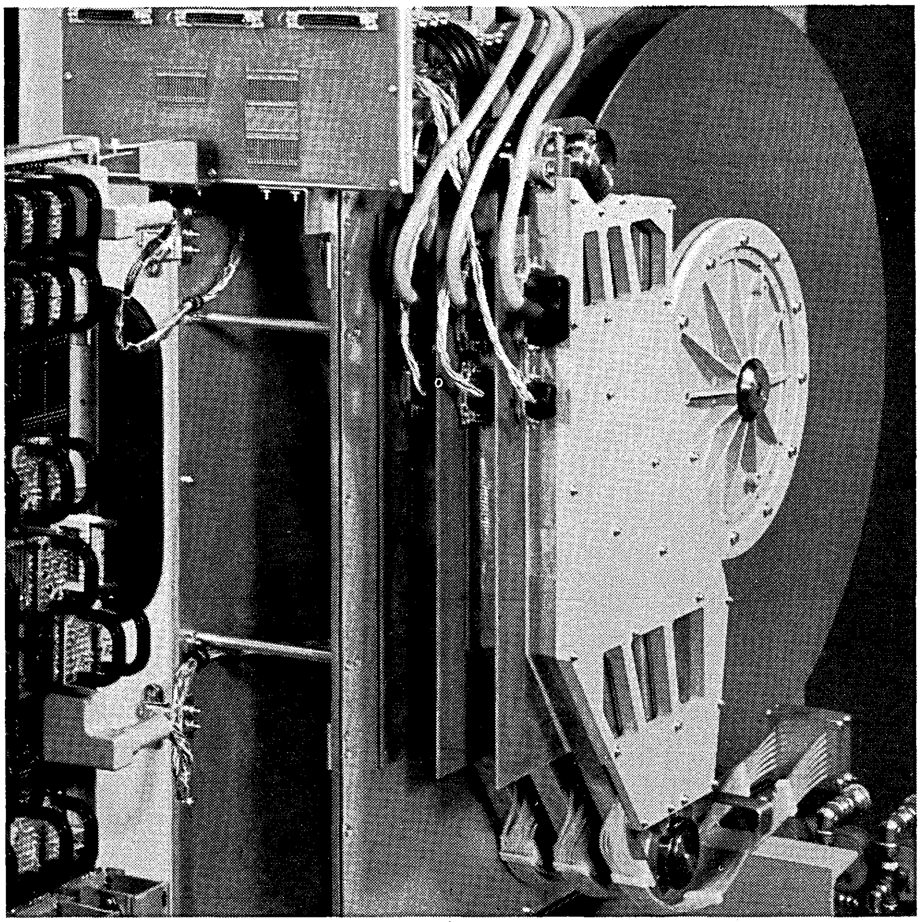
The growing involvement of many banks in edp activities for clients and would-be clients has also put a squeeze on equipment manufacturers and computer time sales companies, which find themselves more and more frequently competing with banks for edp business. Many banks, especially those with a superfluity of machine time after taking care of their own needs, are using the lure of low-cost computer services to attract new banking clients. Discounts from competitive market rates frequently range from 25-50%. In some instances, free computer services have been offered to clients who will maintain specified minimum balances in checking accounts. No legislative action on the Multer Bill is expected before this summer. Congressman Multer's office reports that letters of protest are already arriving from bankers. The measure has been referred to the House Committee on Banking and Currency, chaired by Rep. Wright Patman of Texas. This bodes well for the bill's eventual disposition, since over the years Rep. Patman has built up a considerable reputation as a foe of the "big bankers" and as protector of the small businessman.

1964: BOOM YEAR FOR COMPUTERS

The 1964 economic forecast put out by the Department of Commerce depicts a rosy 12 months for the computer industry. Factory shipments for the electronic computing and accounting machine industry are expected to fall just short of $2 billion, a 10% increase over 1963. Industry employment is expected to climb to 113,500 in 1964, a 3.9% increase over last year (a year which saw industry employment fall off 2.8% from the 1962 level).

Exports for the electronic computing and accounting machine industry are also expected to jump sharply in 1964, rising 15% to $340 million. Imports will show approximately the same percentage increase but on a much smaller base, for a 1964 grand total of $65 million.

Biggest single overseas customer for the industry is Japan. In 1962, last full year for which figures are available, Japan bought almost $40 million of computers and accounting machines. For the first six months of



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1963 alone, these purchases were approximately $32 million, indicating the brush-fire expansion of this market. The Commerce Dept. in its report took note that "keen competition" between American and Japanese manufacturers of these machines is being ameliorated by many U.S. firms entering into licensing agreements with their Japanese counterparts for the manufacture of U.S. business machines.

BUREAU OF STANDARDS TO BEGIN SERVICE BUREAU OPERATION

Time on a 7094/1410, operated by the Bureau of Standards, is being made available to all government agencies in the Washington area on a service bureau basis. The bureau will also offer professional services -- programming and systems assistance -- along with machine time. Pricing schedules and fees for other services are now being established.

Delay in implementing the service bureau operation, which was announced as imminent last summer, was attributed to "unforeseen bugs" and also the extra workload thrown upon the BuBudget and the other government agencies involved by the unexpected change in administration. The government service bureau is intended for those agencies which have no in-house computer capability or have computer requirements in excess of available equipment.

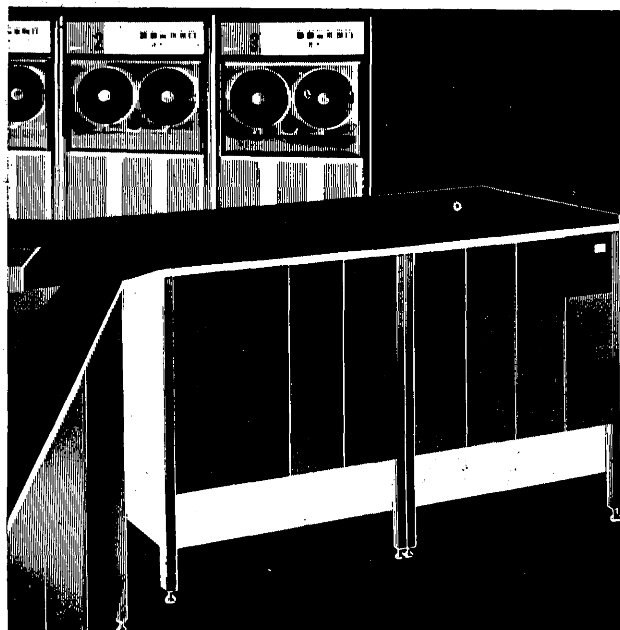
The Bureau of Standards is also operating a "computer exchange" for Washington-area government agencies. Under this brokerage arrangement, free time on federal-operated computers will be made available to other government agencies on a fee basis. A similar exchange of free computer time has been successfully tested in the Philadelphia area.

BUDGET BUREAU BEGINS LONG-AWAITED COMPUTER STUDY

The Budget Bureau's long-anticipated investigation of management and purchasing policies for electronic computers by government agencies got under way, with announcement of the members of the 11-member advisory committee and staff personnel. The first meeting by staff and committee with Budget Director Kermit Gordon to mark off the dimensions of the study will probably have taken place by the time this is read. The final report is due by June 30, 1964.

Project director is Carl W. Clewlow, a management consultant who's held several important government posts. The advisory committee is headed by Robert Ramspeck, an ex-Congressman and former head of the Civil Service Commission. The committee includes several other top-drawer Washington names, including J. Herbert Hollomon, Assistant Secretary of Commerce for Science and Technology, Thomas D. Morris, Assistant Secretary of Defense (Installations and Logistics), Bernard L. Boutin, administrator of General Services, and Martin R. Gainsbrugh, vice president and chief economist of the National Industrial Conference Board.

Their findings on edp procurement and management are expected to have a decisive influence on the fate accorded the Brooks Bill, H. R. 5171, now marking time in the Senate.



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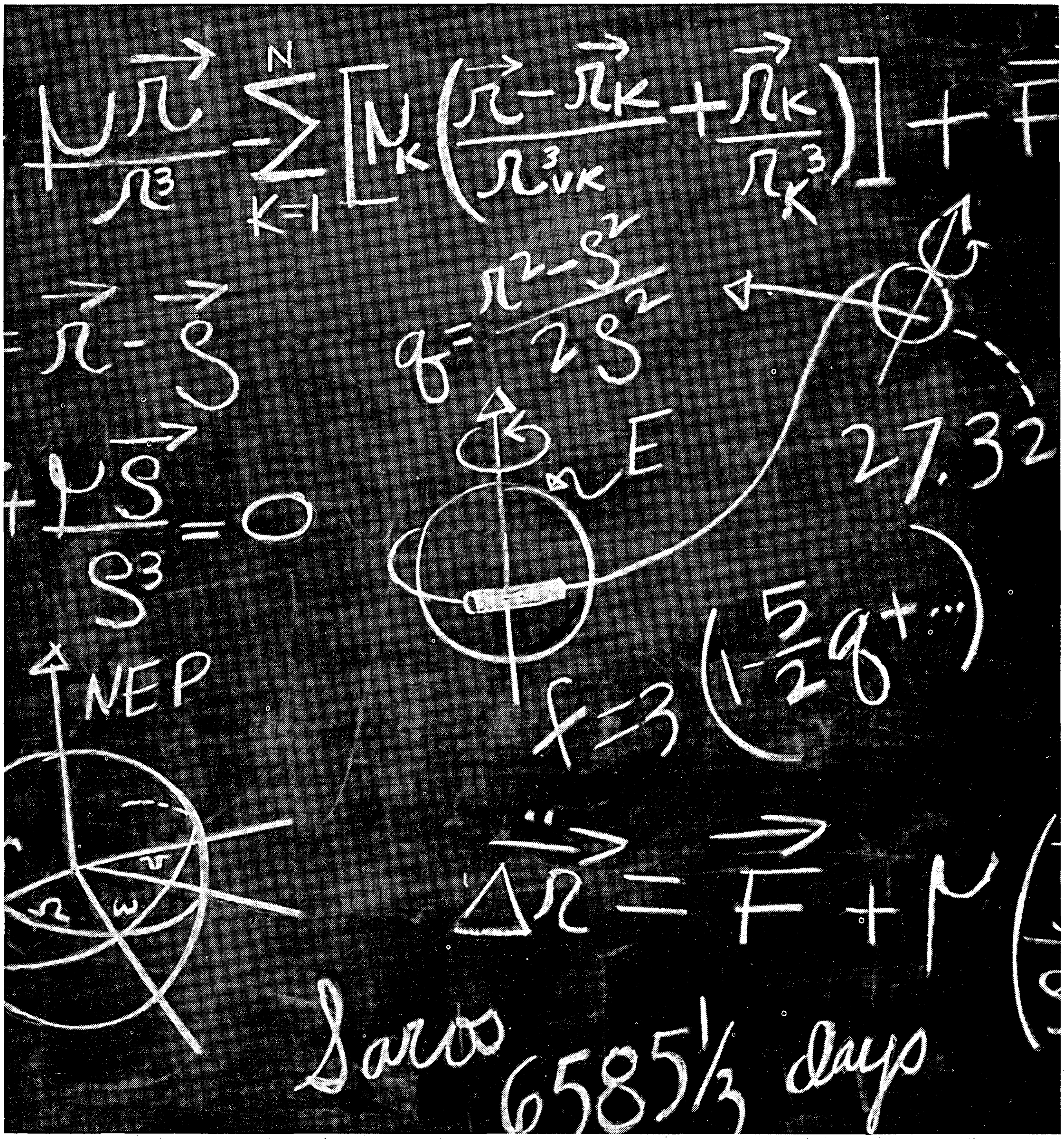
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