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AUGUST 1, 1988

# COMPUTER DESIGN<sup>®</sup>

THE FIRST MAGAZINE OF SYSTEM DESIGN,  
DEVELOPMENT AND INTEGRATION

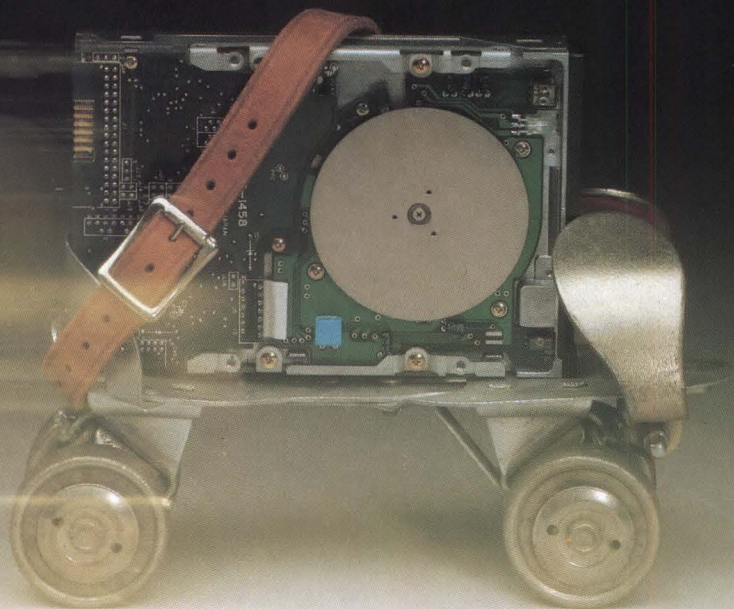


Graphics system  
designers strive  
for photorealism

■ ■ ■

High-density gate arrays tax utility, packaging and testing  
Mixed-mode simulator accurately models real-world designs  
Denser devices, flash designs spawn new applications for EEPROMs

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The MD3611 is a 2.0/1.0MB 3.5" Floppy Disk Drive designed to be driven:

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# Canon

CIRCLE NO. 1

# The "Look and Feel" CAE Users Have Been Looking For

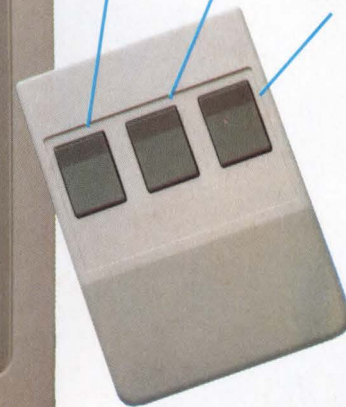
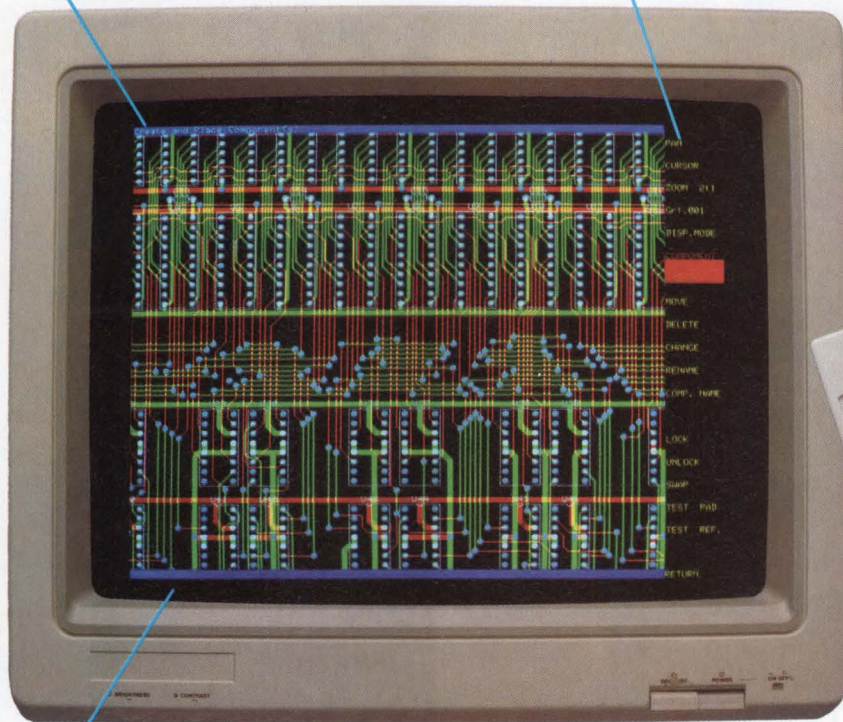
*On-Screen Prompt line makes it easy to find the feature you're looking for.*

*Hierarchical Menus eliminate keyboard commands.*

*Action Button selects functions.*

*Menu Button toggles between menu and graphics.*

*Pan Button Redraws screen around cursor location.*



*Command Line displays selected function.*

*Use Visionics' Super Hi-Res graphics board for workstation (1284 x 960) graphics on a PC platform, or use standard CGA or EGA graphics.*

*EE Designer III takes advantage of all 3 mouse buttons for maximum operating speed and throughput.*

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You'll be hearing a lot about Visionics' EE Designer III in the next few

At only \$3995, no other CAE tool can match the features of EE Designer III:

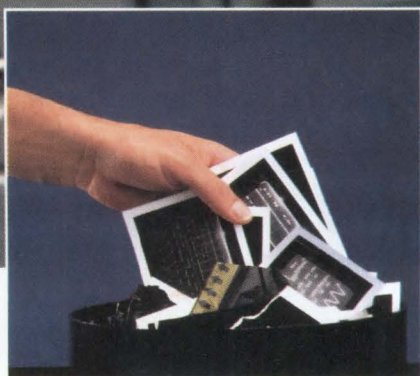
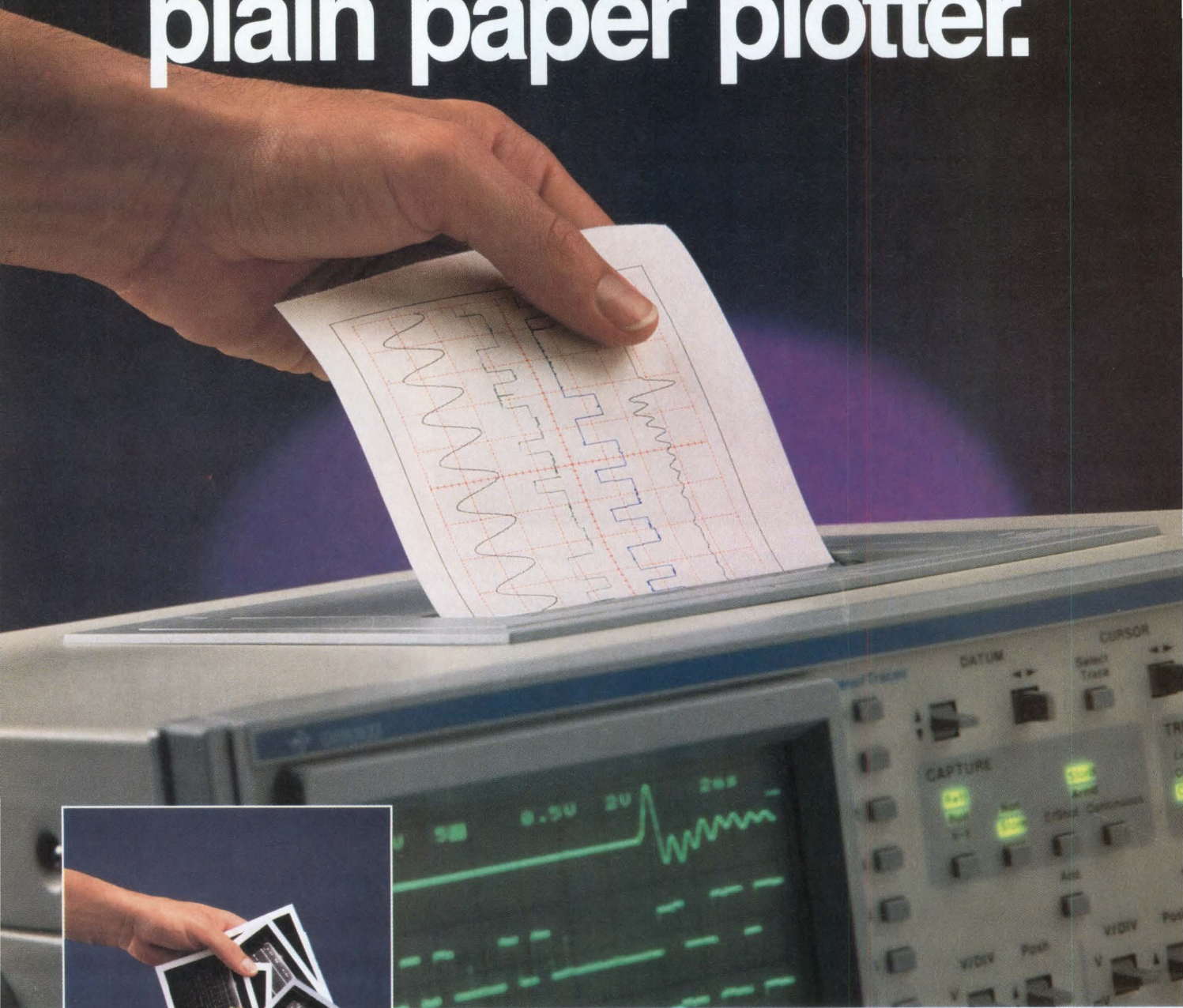
- Supports 2 mb of L1/I/M EMS memory
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Paul has a problem. Poor Paul. He's out of pictures...again. Pity.

Peter is more productive because he prefers the powerful GOULD 4070

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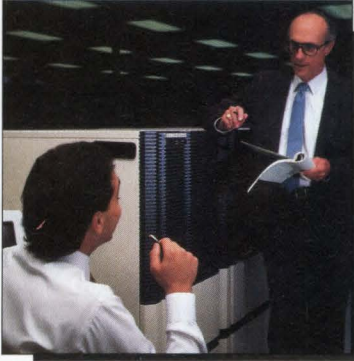


# GOULD

Electronics

CIRCLE NO. 3

THE FIRST MAGAZINE OF SYSTEM DESIGN,  
DEVELOPMENT AND INTEGRATION



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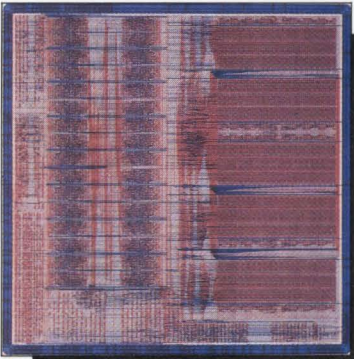
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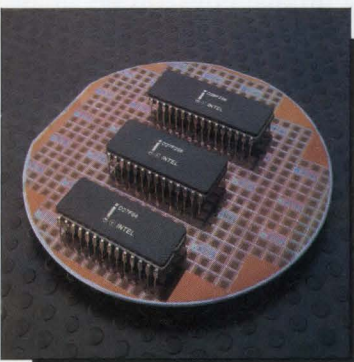
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# 200 MB

# + 15 ms

# = 3 1/2 in.

## SWIFT™ 3 1/2" HIGH-CAPACITY, HIGH-PERFORMANCE DISK DRIVES NOW AVAILABLE FOR EVALUATION.

Get the 3 1/2" disk drive that sets the standard for capacity and performance. We combined the two most important things everyone wants in a storage device—capacity and speed. And packed it into the size everyone would like... 3 1/2".

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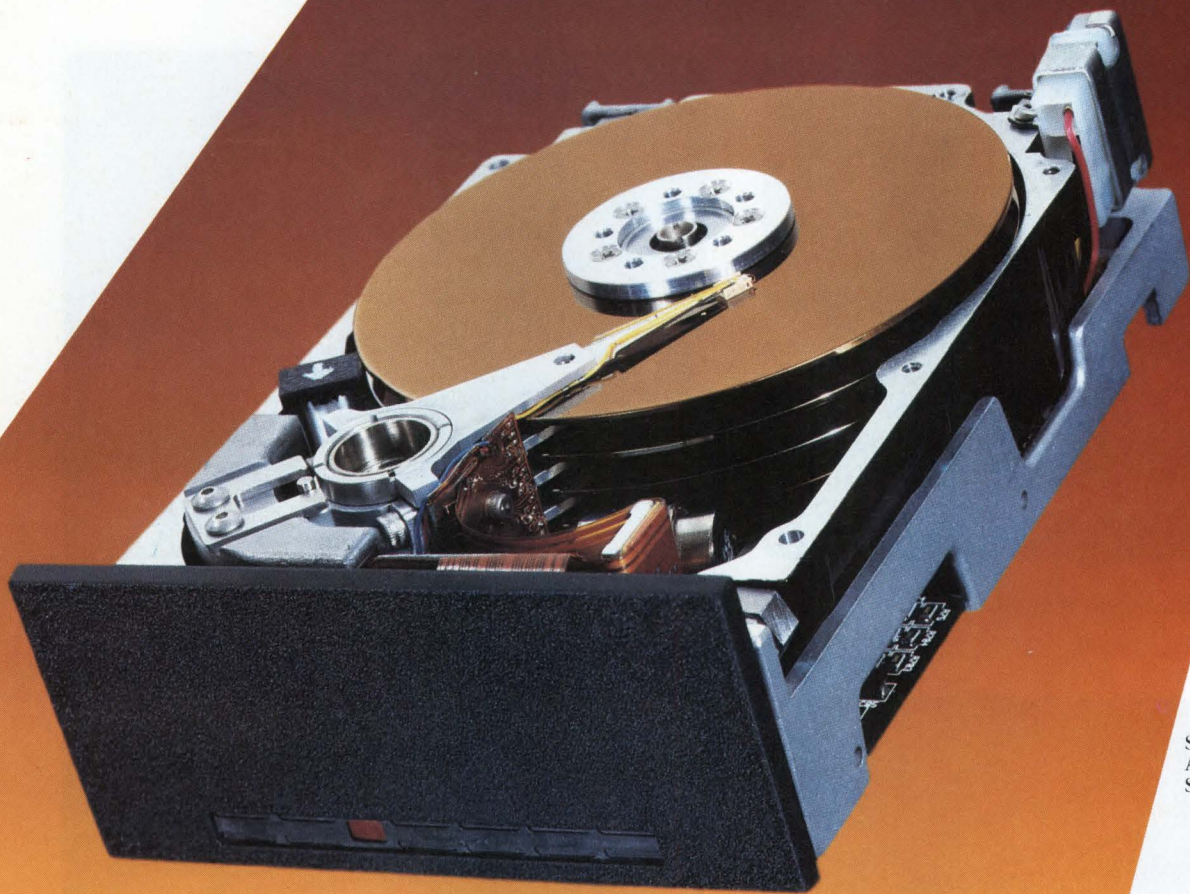
If you're a qualified OEM, you can get an evaluation unit now.

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**GD CONTROL DATA**

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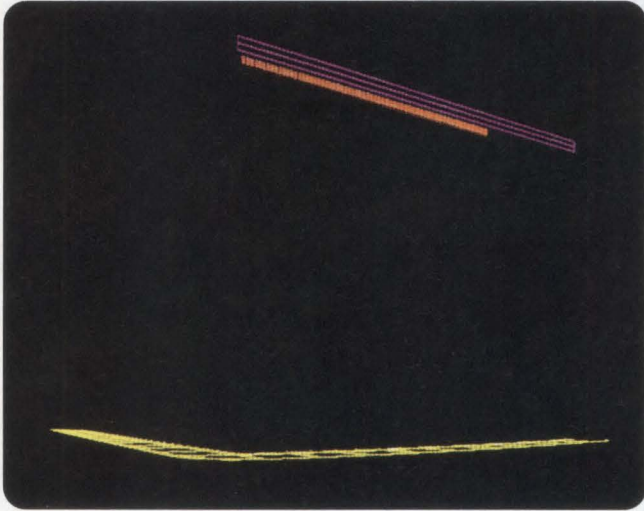
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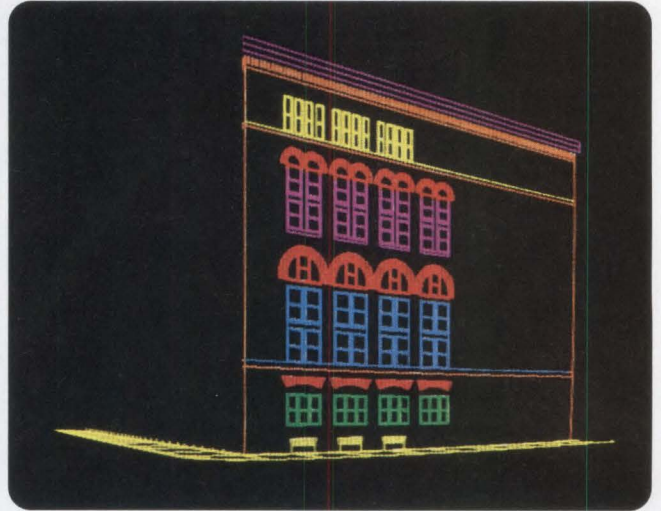
SHOWN  
ACTUAL  
SIZE

Model 9435X	Capacity (Mbytes)	Avg. Seek (ms)	Interfaces	Transfer Rate (MHz)
	200	15	SCSI, ESDI, AT	10
	150	15	SCSI, ESDI, AT	10
	150	15	ST506/412 (RLL)	7.5
	100	15	ST506/412 (MFM)	5

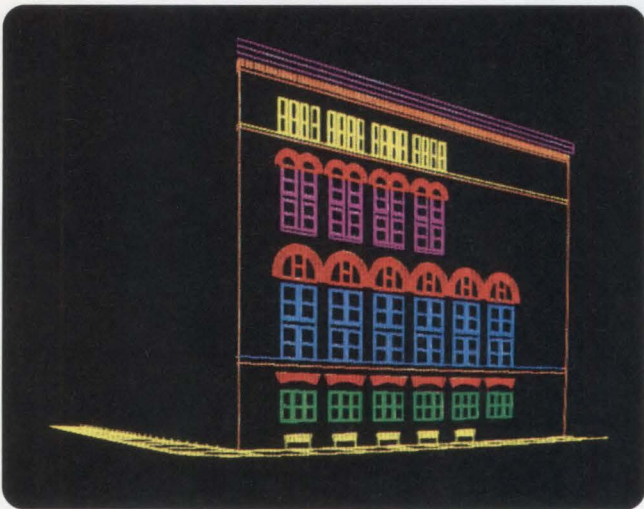
# In the time it takes other graphics engines to draw a few lines...



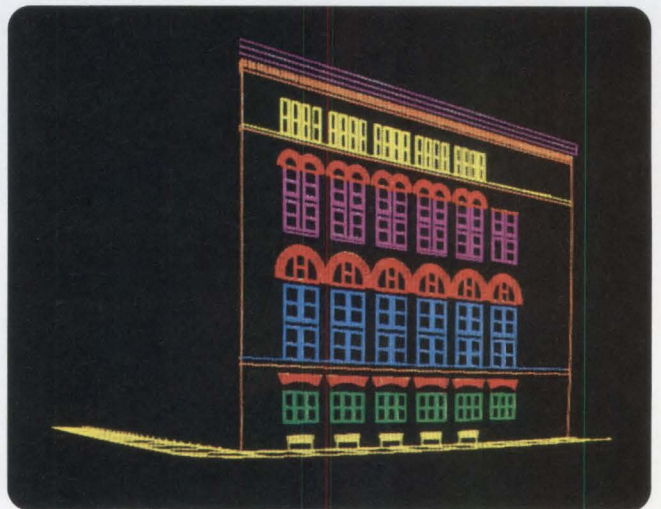
Texas Instruments TMS 34010 (2%)



AMD Am95C60 (17%)



Hitachi HD63484 (20%)



Intel 82786 (25%)

*GeoCad perspective drawing courtesy of Rudolph Horowitz and Associates, Architects.  
Simulated performance based on maximum patterned line-drawing rates in an eight-bit color system with a resolution of 1024 by 768.  
Of course, performance ultimately depends on system elements like memory speed.*



# ours gives you the whole picture.

---

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---

You can have the fastest calculations in the world but if your system's graphics are slow, your system is slow. National's latest addition to its Advanced Graphics Chip Set — the DP8500 Raster Graphics Processor (RGP) — is the fastest graphics engine on the market.

This 20-Mhz CMOS chip features a bus cycle time of 100 nanoseconds on back-to-back vector and block operations.

It gives you blazing speed in line drawing, BitBLT, fills, polygons, character drawing, and windowing — regardless of the number of bit planes. It also controls screen refresh.

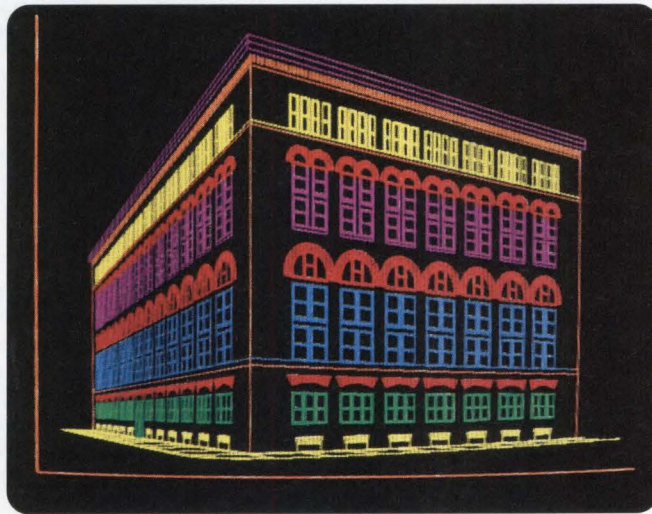
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## COMPLETE FLEXIBILITY

---

The RGP gives you the programmability of a general-purpose processor, so you can optimize your system for specific applications. Or differentiate it from your competitors through proprietary algorithms.

The RGP, with our DP8511 BitBLT processing unit, is also the only



National DP8500 Raster Graphics Processor

graphics solution that effectively allows you to select either planar or pixel-oriented operation on-the-fly. So you no longer have to lock yourself into one architecture or the other.

The RGP handles the very highest-resolution CRTs and printers, including laser printers. And it supports any type of memory.

It also gives you the right "hooks" and the right architecture for moving into 3D and solids modeling applications.

---

## A COMPLETE SET OF CHIPS

---

Our Advanced Graphics Chip Set also includes

- two BitBLT processing units
- four video clock generators
- four video shift registers
- three video RAM controllers
- a growing list of video DACs

They're all part of National's unique modular approach — the only approach that addresses the complete graphics pipeline. And the only one with the performance and flexibility you need to carry you into the 1990s.

---

## COMPLETE SUPPORT

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We offer a wide range of software tools — including assembler, debugger, librarian, linker, software utilities, graphics kernel packages, and a C compiler package.

Nova Graphics International is providing full support for graphics software standards, including GKS and CGI.

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CIRCLE NO. 5

## Graphics processor to team with dedicated floating-point chip

A full 32-bit version of the 34010 graphics processor from Texas Instruments (Dallas, TX), the 34020, will be teamed with the 34082, a specially designed 40-MFlops floating-point coprocessor. The math chip connects directly to the 34020's data and address lines without glue logic.

In addition to supporting the IEEE floating-point standard, the 34082 contains microcoded functions to support three-dimensional graphics. These include matrix operations for clipping, scaling and rotation; vector operations for lighting calculations; and splines for curved surfaces.

In addition, the floating-point chip boasts 100-ns cycle times and addresses up to 64k 32-bit words of external microcode for user-written algorithms.—*Tom Williams*

## Intel reorganizes ASIC effort, drops gate array services

Citing a mismatch between market needs and the company's high-performance—and high-priced—gate array operation, Intel (Santa Clara, CA) has withdrawn from the merchant gate array business and reorganized its application-specific IC products group.

Cell-based ASIC operations and programmable logic products will be unaffected by the move, except for a change in reporting structure. The gate array product team will essentially become a captive supplier to Intel's other product divisions, providing tools and processes for development of application-specific standard products.—*Ron Wilson*

## Sun OEMs and VARs rethink the future

Sun Microsystems (Mountain View, CA) has opted not to support equal access to its disk controller aftermarket. This decision, plus Sun's prominent position in the ongoing hullabaloo over the next version of Unix, has some Sun VARs and OEMs rethinking their long-term

strategy.

Those who have become successful by building systems on a Sun platform will have to reevaluate both their commitment to open-systems architecture and their feelings about the relative safety and inflexibility of accepting dictated solutions. They will also have to decide whether it's in their long-term interests to move to a new workstation platform, instead of, or in addition to, Sun.—*David Lieberman*

## FDDI chip set due in final form

Just 13 months after sending the Supernet Fiber Distributed Data Interface (FDDI) chip set to beta sites for evaluation, testing and debugging, Advanced Micro Devices (Sunnyvale, CA) will release a final revision to all customers.

The revised silicon, which will start volume shipment in December, will contain only three sublayers of the four-layer standard expected to be released by Accredited Standards Committee X3T9.5 and accepted by the International Standards Organization, according to Patrick Green, AMD strategic development manager for FDDI products. These three will be the physical media dependent layer, the physical layer and the media access controller layer.

Since the still-unapproved fourth layer—station management—can be handled by software workarounds, AMD won't wait for that layer's definition and acceptance and will leave it out of the revised chip set.

—*Sydney Shapiro*

## VME II—the bus that never was

The VMEbus community reports that the rumor of an impending "VME II" was a temporary, and regrettable, glitch. The bus expected to become the high-end, 32-bit asynchronous bus-of-choice already has a name—Futurebus—and most agree that calling it VME II would suggest relationships and compatibilities that don't exist.

"It would be a mistake to do what Intel did with Multibus and Multibus II, whose only relationship is

that Intel developed them both. All that did was confuse the customer," says one industry observer.

—*David Lieberman*

## Toolset provides foundry-independent ASIC development

A new toolset from Mentor Graphics (Beaverton, OR) may help change the way application-specific ICs are designed. While designers today must select an ASIC foundry before beginning schematic capture, Mentor's ASIC Vendor-Independent Designer (Avid) software lets that decision be put off until later in the design cycle.

Avid provides a library of generic schematic symbols that can be mapped into a selected vendor's component models following schematic entry and functional simulation.

ASIC vendors formally committed to supporting Avid include Fujitsu, GE Solid State, Gould, Intel and Toshiba.—*Richard Goering*

## Could Unix be replaced?

That heretical thought has come up amid rumors that a workstation from Next (Palo Alto, CA), whose announcement is also rumored to be imminent, will use the Mach operating system developed at Carnegie-Mellon University. While not Unix, Mach is said to offer binary compatibility with BSD 4.3 Unix and have virtually all functions of Unix and then some.

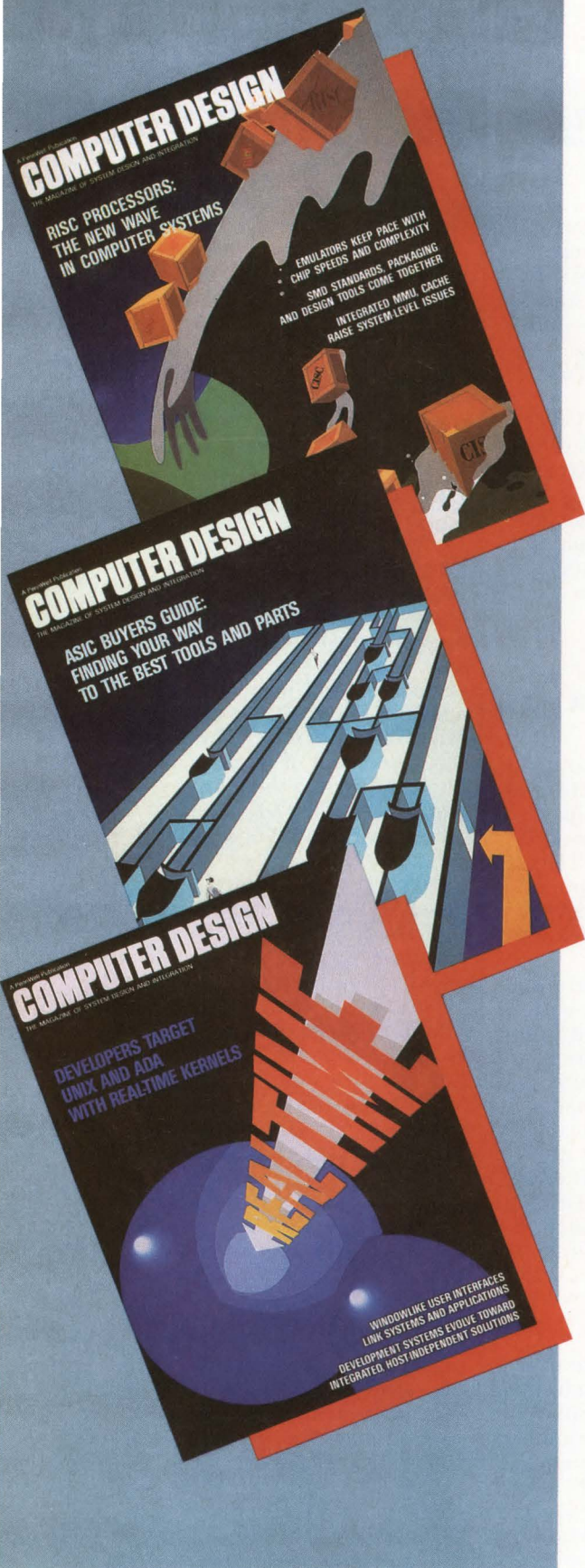
The system, which features inter-process communication, is based on an object-oriented model similar to Smalltalk developed by Xerox (Rochester, NY).

There's no word yet as to what kind of user interface the Next machine may use, but Mach is said to be able to easily run one of many known visual interfaces such as Sun's NeWS, IBM's Presentation Manager or the Macintosh Finder. Bets are that the system won't run the latter.—*Tom Williams*

## Interface to link logic synthesis with VHDL

Two of the hottest trends in the electronic design automation indus-

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- There are publications that focus exclusively on ASICs.
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try—logic synthesis and the VHSIC Hardware Description Language (VHDL)—will be brought together as the result of an agreement between Silc Technologies (Burlington, MA) and Vantage Analysis Systems (Fremont, CA).

The two companies will build an interface between Silc's Silcsyn product, which can synthesize gate-level logic from behavioral descriptions, and the Vantage Spreadsheet, a VHDL simulation environment. This interface will eventually let users describe designs using VHDL and have Silcsyn automatically generate the gate-level logic.

Both toolsets run on workstations from Mentor Graphics (Beaverton, OR).—*Richard Goering*

## New platform may be antidote for workstation vendors' woes

Competition is intensifying in the workstation market, and nobody knows this better than Apollo Computer (Chelmsford, MA). After unexpectedly low second-quarter earnings, Apollo unveiled two new product families that it expects will be price/performance leaders for the near term.

Built around a 33-MHz MC68030 CPU and a 33-MHz MC68882 floating-point coprocessor, the Series 4500 delivers up to 7-Mips performance. Prices for the series start at about \$19,000.

A lower-cost series features a 25-MHz MC68030, a 25-MHz 68882 and 4 to 32 Mbytes of main memory. The 4-Mips Series 3500 sells for under \$8,000.—*John Mayer*

## Math software wins flurry of big-name approval

Heavy hitters from seven major computer firms turned out at the recent introduction of a new math software package to announce their support. Mathematica from Wolfram Research (Cupertino, CA) can function both as an application program and as a programming language to form the basis of more specialized applications. It can do numerical calculations at arbitrary precision, perform symbolic math on algebraic formulae and graph

functions interchangeably.

Steve Jobs, president of Next (Palo Alto, CA), announced his company will be bundling the package with the long-awaited Next workstation. Jobs stressed Mathematica's importance as the basis for a new generation of applications that will use intense mathematics.

Addison-Wesley (Redwood City, CA) will be publishing a new calculus that will use the interactive features of the package. Other companies supporting Mathematica include IBM, Silicon Graphics, Ardent Computer, Apple Computer and Sun Microsystems.—*Tom Williams*

## Program established for application-specific memory design

Standard-memory IC vendors will have to alter their approach to vendor-customer relationships if the promising application-specific memories market takes off. That at least seems to be the assumption underlying a new program developed by NEC Electronics (Mountain View, CA).

Under the program, a team of the company's design managers will work with customers to identify and design products to specific system memory needs. One example would be to embed processing elements right in a memory array. The application-specific memory designs will then draw on NEC's dynamic RAM and static RAM expertise at company facilities in Japan and Roseville, CA.—*John Mayer*

## Altera allies with TI on erasable PLDs

Altera (Santa Clara, CA), which is just beginning to branch out from relatively conservative architectures into larger-scale PALs and application-specific programmable logic devices, must face challenges both from standard-parts vendors that are beginning to add programmable logic to their devices and from radical new, gate-array-like PLD architectures. In an apparent effort to recruit additional allies in this growing war over programmable logic architectures, Altera has

formed a strategic alliance with Texas Instruments (Dallas, TX).

Under the agreement, TI will manufacture and distribute certain of Altera's high-density PLDs. Adding the TI alliance to a similar existing relationship with Intel (Folsom, CA) may give Altera marketing and distribution strength to supplement its architectural moves.—*Ron Wilson*

## DEC ponders purchase of RISC chip

Rumors persist that Digital Equipment Corp (Maynard, MA) may finally move away from its proprietary microprocessor and build products around a reduced-instruction-set computer chip. The likely candidate appears to be the R3000 CPU from Mips Computer (Sunnyvale, CA), allegedly capable of yielding 20 VAX Mips, or 20 times the integer performance of a DEC VAX-11/780.

Feeding the rumors was DEC's recent cancellation of two development projects, one to develop a faster VAX and a second to build an in-house RISC CPU. If DEC does decide to go the RISC route, questions about compatibility will be the first to surface. The company has made dramatic inroads on competitors in recent years on the strength of its product lines' uniquely compatible VAX design.—*John Mayer*

## Desktop parallel machine supports portable software

Cogent Research (Beaverton, OR) is trying to bring software portability into the parallel market by combining a parallel-processing software, called Linda, with its XTM workstations. Other parallel processors use proprietary software to take advantage of a system's unique architecture, but that approach produces software that's incompatible with all other parallel machines.

Linda isolates the peculiarity of particular parallel architectures from applications software, letting the same programs run on any Linda-based processor. Though this concept has been adopted by others, Cogent is the first to implement the methodology in a desktop machine.—*Michael Donlin*

# Object-Oriented Engineering

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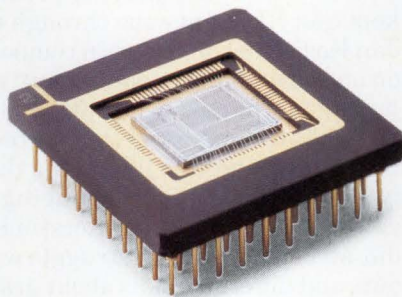
**"A CLEVER TOY, BUT WE  
EXPECTED SOMETHING THAT WOULD  
BE MUCH MORE USEFUL!"**

**AMERICAN JOURNALIST, 1879**



# **"IT'S A GREAT PRODUCT, BUT I DON'T WANT TO LEARN A WHOLE NEW LANGUAGE JUST TO USE IT."**

**DESIGN ENGINEER, 1988**



For years, people have been intrigued with the latest in technology. But, they've been less than enthusiastic about learning how to put it to good use. The Transputer from INMOS is no exception.

System designers agree that Transputer's are revolutionary, but the prospect of learning a new programming language has made some of them a little uneasy.

The truth is, Transputers can actually be easily programmed in most high level languages developed for standard microprocessors including C, Fortran and Pascal. And, since Transputers are so much more than standard microprocessors, we've also developed OCCAM.

But don't let that scare you. OCCAM actually eases the system designer's task by simplifying the representation and control of parallel systems. It's easy to learn and can be intermixed with the languages you already know.


And OCCAM creates a whole new programming dimension. Because a program running in a Transputer is formally equivalent to an OCCAM process, a network of Transputers can be described directly as an OCCAM program.

Together with just one or more Transputers, the formal rules of OCCAM provide the design methodology for true concurrency and unlimited system extendability. And OCCAM programs do not have to be rewritten as Transputer-based systems grow to utilize future levels of integration.

So take another look at the Transputer with OCCAM. It's a revolutionary way of processing information. And it's easy to speak the language.

**TRANSPUTER**  

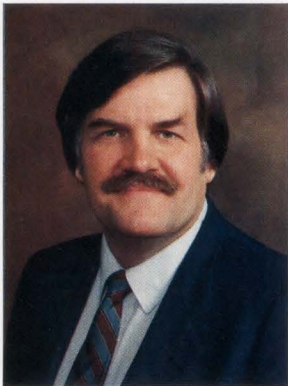

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**CIRCLE NO. 8**

## A change in style but not in substance

**"Just because  
we have to be  
serious doesn't  
mean we have to  
be stodgy."**



**John C. Miklosz**  
Associate Publisher/  
Editor-in-Chief

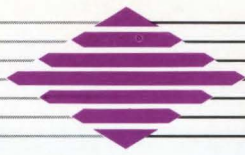
**W**e've talked about it for a long time and now we've done it. *It is Computer Design's* new look. It's a look that's contemporary and makes for easier reading, but isn't flamboyant or too flashy. After all, *Computer Design* is targeted at senior design engineers and design engineering managers like yourself. You're serious about the technical decisions you have to make, and *Computer Design* is serious about bringing you the kind of information that will help you in making those decisions. The look and the content of *Computer Design* have to work together, but just because we have to be serious doesn't mean we have to be stodgy. We think we've achieved the right balance and the right look. We hope you agree.

It took some doing, and some key people working together: Bruce Sanders, the publication designer who turned verbal expressions of abstract descriptions into type and layouts; Jan Horner, our art director, and Jan Lopez, our production director, the two people who kept everything moving through design, typesetting and layout; Jan Kasiecki, our expert in composition who formatted the new pages on our page-makeup equipment; and Mari Rodriguez, our production manager, who saw to it that every detail of editorial, art, photography and type came together correctly at just the right time for this first issue—and who'll be doing the same for future issues. And finally, Susan Nykamp, our managing editor, and our indefatigable copy editors: Richard Dagley, Kerstin Rosenquist and Barbara-Ann Scofidio, all of whom had to struggle with unfamiliar type specs, new layouts and different ideas about graphics without missing a beat in the regular schedule.

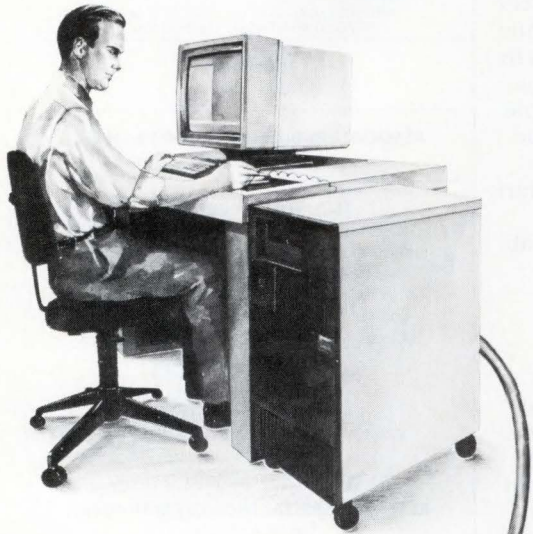
But a word of reassurance among all of this hoopla about redesign. We've made some major alterations in our appearance, but we haven't changed our editorial charter. That charter, summed up in the subtly different tag line that you'll find right under the *Computer Design* logo, is to be "the first magazine of system design, development and integration." Since our first issue, published in 1962, *Computer Design* has taken the "systems" view. It's a view that treats hardware design, software development and hardware/software integration—at all levels, whether chip, board or box—as inseparable aspects of the product creation and development cycle. Some other publications have apparently heard our message because they now include the word "systems" in their names. But *Computer Design* was the first—and will remain the first. The first magazine of system design, development and integration.

A handwritten signature in black ink that reads "John Miklosz". The signature is written in a cursive, flowing style.





# The Complete UNIX/Real-Time Connection.



## OS-9 utilizes common UNIX features:

- Multi-user, Multi-tasking
- UNIX I/O model
- UNIX task model: (fork, set priority,...)
- Pipes and Signals
- Shell User Interface
- Hierarchical Disk File System

## ...and more to connect you to Real-Time:

- Fast task switching
- Data modules
- Easy system generation and reconfiguration
- Fast interrupt servicing
- Events and semaphores
- Resident OS-9 compilers, assemblers and debuggers

## OS-9 UniBridge

Integrating UNIX and C applications into VMEbus systems has just been made easier with Microware's introduction of UniBridge. UniBridge is a complete development and communications package that allows you to connect your SUN 3, DEC VAX, HP 9000 or Motorola Delta workstation, to the world's premier real-time operating system: OS-9.

UniBridge provides a gateway so you can utilize UNIX in every phase of VMEbus system integration. From hosting C application development to monitoring large real-time networks, UniBridge connects UNIX to your OS-9 target system; whether it's ROM-based, disk-based, networked or stand alone.

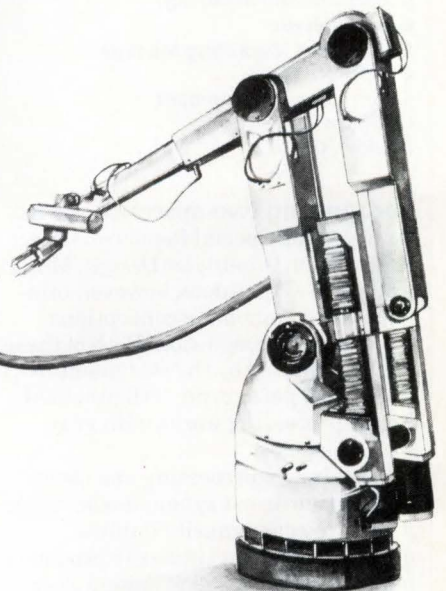
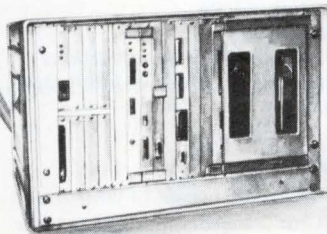
UniBridge contains three high performance software modules that link UNIX and OS-9:

- OS-9/XCC Cross C Compiler allows you to produce compact, re-entrant and position independent C applications on your workstation for high speed execution on your OS-9 target.
- OS-9/ESP Ethernet Support Package provides industry standard BSD 4.2 sockets for TCP/IP communications with full FTP and Telnet support. UniBridge lets your workstation become a real-time server.
- OS-9/SRCDBG debugs resident VMEbus applications at the C source level, all interactively, across the Ethernet network from your UNIX terminal. And UniBridge makes all file access and transfer transparent from system to system while you debug.

*And no other operating system complements UNIX with real-time functionality better than OS-9.* OS-9, like UNIX, is a complete operating system to provide extensive C and math libraries, independent file managers, inter-process communications, debuggers and resident compilers. Yet OS-9 is 100% ROM-able and executes in real-time to host thousands of imaging, process control, data acquisition, communications and robotics projects worldwide.

Best of all, every module of UniBridge and OS-9 is written entirely by Microware to provide you one source for technical support and service.

From UNIX and C, to OS-9 and VME, contact Microware today and let your next real-time application shine with UniBridge: The Complete UNIX/Real-Time Connection.



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CIRCLE NO. 10

## LETTERS

### Accuracy and ease-of-use

We are writing to you concerning Richard Goering's article entitled "Behavioral simulation speeds path-delay modeling" (*Computer Design*, April 1, p 33). Although it was generally a fair and unbiased report, a single sentence in the article incorrectly implied that the Cadnetix method for behavioral model development might result in inaccurate models. We would like to set the record straight.

During the process of design tool development, Cadnetix' focus has traditionally been twofold: to produce a technologically advanced application tool that is also easy to use. For this reason, Cadnetix developed a heuristic method for creating behavioral models. This approach allows Cadnetix users to automatically model most parts to 100 percent accuracy, at a very rapid rate. As cited in your article, this is the case because the system heuristics do not automatically address certain situations (e.g., transmitting from floating to unknown states). In these instances, the user can add his or her own rules, with a minimum of effort, to complete the model(s) in question. Cadnetix has chosen this approach in order to offer customers both ease of use—the hallmark of all Cadnetix tools—and 100 percent model accuracy.

**David Niehaus**  
CAE Product Marketing Manager  
**Chuck Robertson**  
CAE Product Development  
Cadnetix  
Boulder, CO

### Recognizing two misconceptions

I enjoyed the Special Report on Object Recognition (*Computer Design*, May 1, p 69). The article does, however, reinforce two common misconceptions about object recognition. Both of these are exemplified by the statement in the second paragraph: "All practical image processing works with gray-scale images."

First, image processing and object recognition aren't synonymous. Image processing customarily implies modification of one image to produce a new image. It is used to enhance certain diagnostic features relative to other features. Image processing is often, but not always, used as part of traditional object recognition procedures.

Second, it is no longer true that all

practical object recognition works with gray-scale images. Use of color often facilitates recognition of objects and, in many cases, can entirely eliminate the need for image processing in the recognition process. Color frame grabbers for PCs have been available for several years from such manufacturers as Truevision (Indianapolis, IN). Recently, Data Translation (Marlboro, MA) and Coreco (Longueuil, Quebec) have added color frame grabbers to their product lines.

**Robert K. McConnell**  
Arlington, MA

### Congratulations

You've done a lot with *Computer Design* in the last several years and are to be congratulated for not only the technical quality of the magazine but for your willingness to speak out on issues of conscience. It seems that technology is ever in danger of becoming its own god. If we are to be masters of technology, rather than be mastered by it, we must always be mindful of the consequences.

**David Barnes**  
Manager, Marketing Communications  
Advanced Processor Division, Intergraph  
Palo Alto, CA

### Sign me up

I have been using copies of your magazine at other institutions very productively for about a year, and I would like to compliment you on a fine publication. *Computer Design* has been so useful, in fact, that I wonder if you would consider adding me to your "qualified subscriber" list.

I am an investigator on NIH-funded research in lung physiology, and the work involves acquiring, setting up, and running a digital image-processing workstation in my lab, with a couple of different image sources. The system will probably be a Sun-3/150 with Vicom image-processing board set and software, a Sky array processor, and an Interphase H-SMD interface, with a 330-Mbyte hard disk, 4-Mbyte system memory and 8-Mbyte image memory to start with. I do much of the programming and have done the investigations and winnowing out that led to these choices, so your magazine could be quite a help.

**Eben H. Oldmixon**  
Memorial Hospital of Rhode Island  
Pawtucket, RI

# COMPUTER DESIGN

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

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**CIRCLE NO. 11**

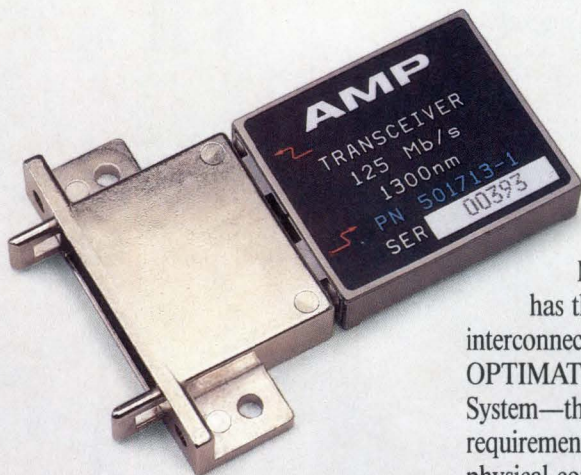
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# FDDI.

## From deskwork to network.



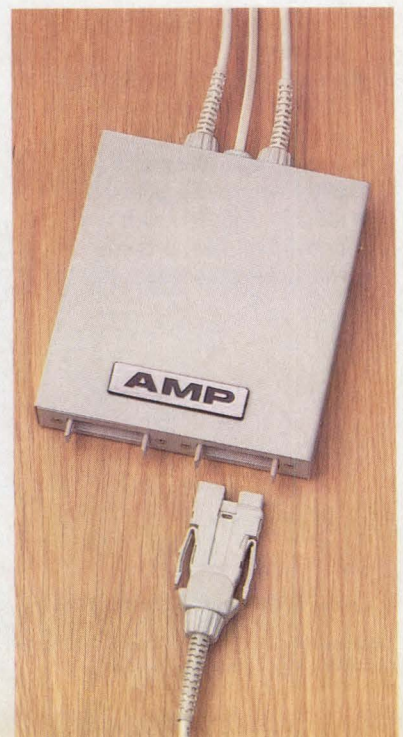
Good news for networks!

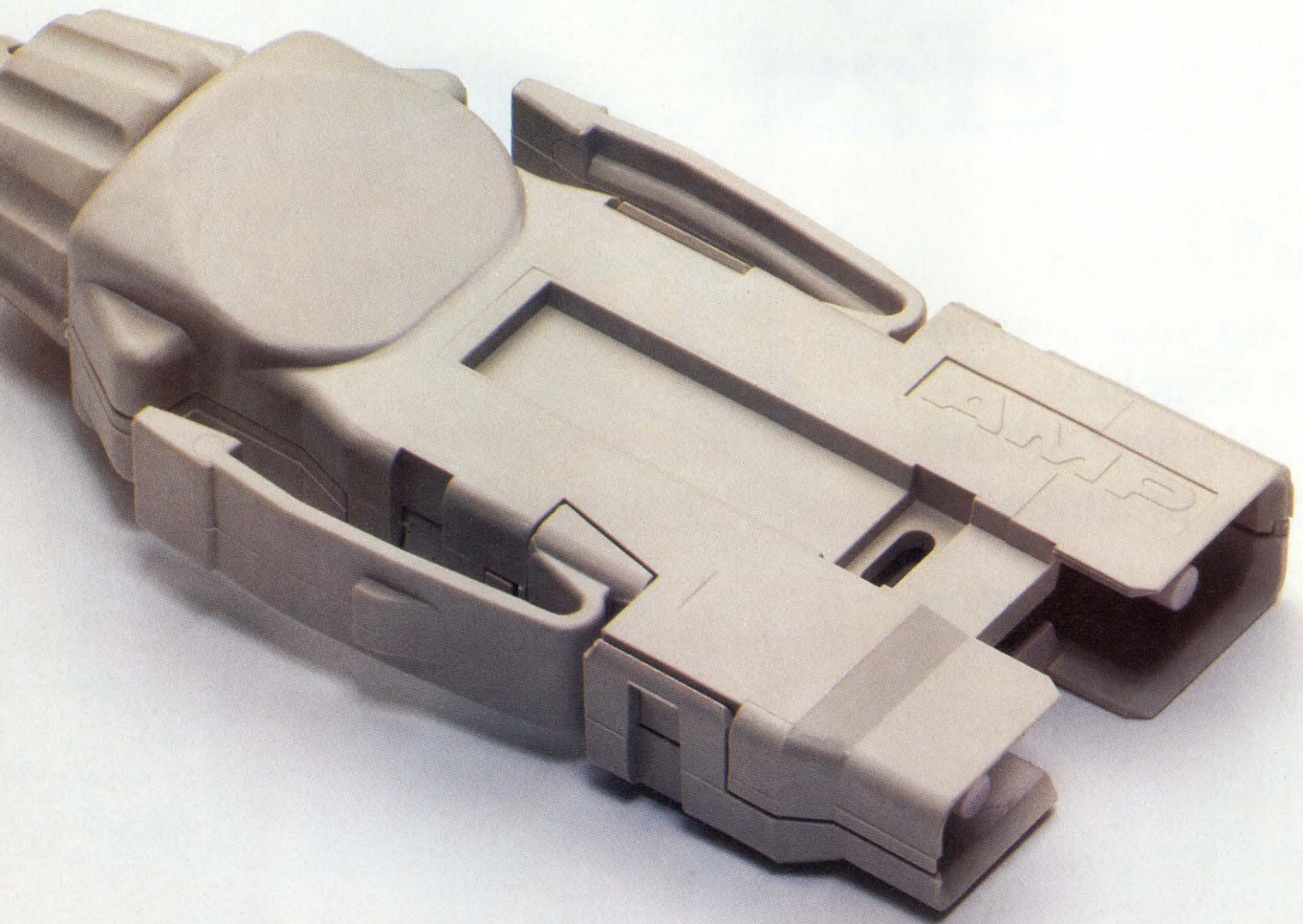
*The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document.*

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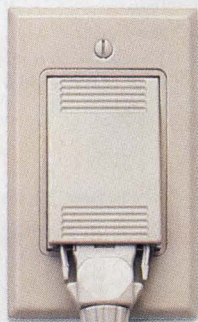
Of special note: the transceiver—the first of its kind—is capable of operating at data rates up to 125 Mb/s. Available in standard or raised (+5v) ECL logic, it gives you a compact, board-mount data link in a single 24-pin module. Reliable duplex mating

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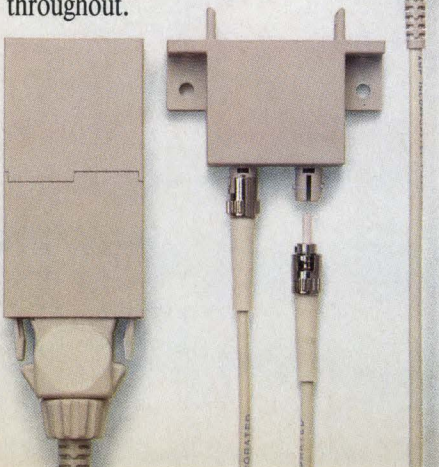


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COMPUTERS AND SUBSYSTEMS

## Application tuning: a key to RISC system development

Ron Wilson, Senior Editor

The fundamental principles of reduced-instruction-set computer design assume a smooth flow of instructions through the CPU. To achieve this flow at high CPU speeds, RISC designers rely on extensive instruction and data caches. But for this strategy to be effective, every part of the system, from instruction set to operating software to applications code, must work to minimize flushing and reloading of the caches. Designers at Pyramid Technology (Mountain View, CA) and Hewlett-Packard (Palo Alto, CA) have used system-level simulations with actual application-code samples to choose their cache-management strategies.

Pyramid has used actual application data extensively in the design of its new 9000TA processor family. The approach lets Pyramid's designers increase throughput substantially by tuning the instruction set, Unix-derived operating system and cache organization without major changes to the CPU execution unit. "We have performance gains of 30 to 100 percent on data base and network-serving applications, even though the underlying Mips figure has increased by only 5 percent," says Stephen Tolchin, vice-president of software development at Pyramid.

### ■ Tailoring cache to application

The performance enhancements in the 9000TA family were born during architectural research for an entirely different family of Pyramid products. "In the course of developing our next-generation product, we took instruction streams from Pyramid machines in production environments and ran the streams through four levels of simulation. We found that for many applications, we could make substantial improvements in throughput without an entirely new architecture," says William Gimple, vice-president of systems technology and product marketing.

"First, we made important changes in the way Unix schedules jobs for

the CPUs in a system. Then we made hardware changes focusing on the organization of the instruction cache," he continues. Pyramid's investigation of the instruction streams showed that, while its two-way set-

**"We have performance gains of 30 to 100 percent on data base and network-serving applications, even though the underlying Mips figure has increased by only 5 percent."**

—Stephen Tolchin, Pyramid Technology

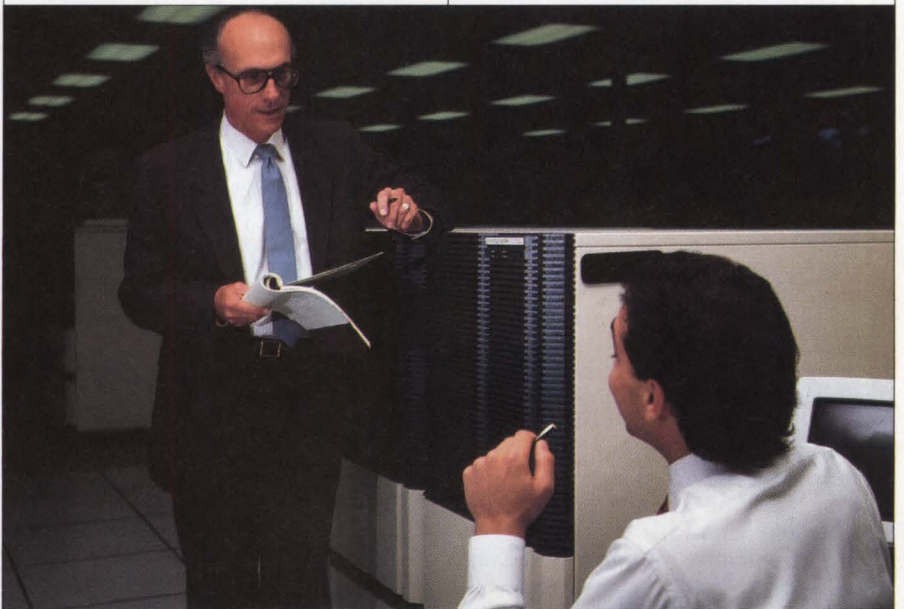


associative data cache was working well, its similar instruction cache wasn't suited for some applications. In data base applications in particular, Gimple's team discovered that the working set, which is the portion of an active program that is most frequently executed, was much larger than had been the case for more traditional Unix-based applications. This larger working set didn't fit in the instruction cache, resulting in a loss of efficiency.

### ■ Eight-bank organization

The design team began trying various instruction cache designs with their simulation. They found that no matter how large they made a two-way set-associative cache, it still had problems with the large working sets. When a process became inactive, at least half of the instruction cache had to be invalidated.

The designers' novel solution was a 256-kbyte cache, organized into eight banks. Rather than being strictly set-associative, the banks are associated with a process identification code assigned by the operating system. Each active process in a CPU, therefore, can have its own



*William Gimple, vice-president of systems technology and product marketing for Pyramid Technology, discusses performance evaluation results of the new caching subsystem Pyramid developed for its 9000TA processor family. By using application data extensively in designing the family, according to Gimple, Pyramid's designers increased throughput by tuning the instruction set, Unix-derived operating system and cache organization without major changes to the CPU extension unit.*

COMPUTERS AND SUBSYSTEMS

bank of instruction cache, even if many processes share the same virtual address range. The result is that when a process becomes inactive, only a small portion of the instruction cache has to be invalidated.

■ **Another application-tailored design**

The developers of the Precision Architecture at Hewlett-Packard were among the first to use comprehensive application-code samples to tune their system design. "The starting point for design of the Precision Architecture was an extensive set of code samples from actual applications running on existing HP systems. The data covered interactive and batch environments and contained code generated in all of the popular languages," says Michael McMahon, district manager for HP's information technology group.

The HP designers fed their code samples into an iterative process. "We would postulate an architecture from observations of the actual workload and then validate it with feedback from the software and hardware implementation groups," explains McMahon. This approach led to many of the key characteristics of the HP RISC CPU, including the design of the instruction set and the organization of the register file. In addition, the application data influenced certain system software decisions, such as the way registers are managed during a context switch.

■ **Embedded-system implications**

The experiences of HP and Pyramid designers indicate the value of tuning a RISC system with real application code samples rather than benchmarks. Both companies found that non-CPU issues such as context-switching strategies and cache-management techniques have an impact on real system throughput in the commercial environment.

As RISC machines move into embedded applications, the same conclusions may remain valid. Like large data base and transaction-processing installations, embedded computers tend to have a small set of tasks that must be performed within a fixed response time. Like commercial systems, embedded computer behavior has been notoriously hard to predict from benchmarks. And like

the larger systems, embedded computers are known to be sensitive to such issues as context switching time and cache hit rates.

It may well be that system modeling and tuning using actual code samples will be a key tool in RISC embedded system development. This

technique may offer designers a way to choose between on-chip and external caches, to select caching strategies, and to plan real-time kernel designs. Certainly if the technique can yield the kind of performance improvements reported by Pyramid, it's worth a try. ■

**PS/2 boards equipped for speed in data-acquisition tasks**

*Sydney F. Shapiro, Research/Special Projects Manager*

**A**lthough the IBM PC is still by far the dominant controller for laboratory and small-to-medium factory data-acquisition systems, there's little question that system designers will eventually replace the PC with a faster, more versatile small computer. As would be expected, one contender—the Micro Channel-based IBM Personal System/2—has a major advantage over

**Designers of data-acquisition systems will likely opt for boards that meet the PS/2 specifications because the Micro Channel bus can handle much higher throughputs than can the 16-bit AT bus.**



any other computer competitor. Simply because it's an IBM product, the PS/2 is most likely to be the eventual successor to its elder sibling.

A main concern of users of data-acquisition systems is how quickly they can input and access data. One reason that designers of data-acquisition systems will likely opt for boards that meet the PS/2 specifications is the capability of the Micro Channel bus architecture to handle higher throughputs than can the 16-bit AT bus. That's particularly

true with the 32-bit 80386-driven PS/2 Model 80 and the Model 70 386. While direct memory access on PC-based products is limited to about 400 kbytes/s (unless special, costly measures are taken), it's possible to routinely obtain throughputs of up to 1 Mbyte/s on the Micro Channel.

Multiple DMA channel capability of the Micro Channel bus architecture lends another advantage to the PS/2. The IBM PC AT provides only two DMA channels; the PS/2 has eight. A designer of a data-acquisition system, therefore, can provide multiple boards without worrying about one going fast because it's under DMA and another going slow because its I/O operations are limited by the CPU.

■ **PS/2 board threesome**

National Instruments (Austin, TX) announced its first PS/2 data-acquisition board—the MC-GPIB IEEE-488 interface—last July, only a few months after IBM introduced the PS/2. Now, a year later, National has announced three very high speed data-acquisition boards that let IBM PS/2 Models 50 through 80—including Models 70 386 and 50 Z, which were introduced in June—handle time-critical laboratory and factory applications.

National Instruments' efforts haven't been limited to the PS/2. In fact, one-quarter of National's business has focused on boards for the Apple Computer Macintosh II and its Nubus, according to James Truchard, president. The company's expertise in designing data-acquisition boards for other buses, however, has aided in



## SPIE ANNOUNCES

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*Conference Chair:* Barry T. Neyer, Monsanto Research Corporation/Mound
- Fiber Optic and Laser Sensors VI  
*Conference Chairs:* Eric Udd, McDonnell Douglas Astronautics Company; Ramon DePaula, Optical Technologies, Inc.
- Fiber Optic Smart Structures and Skins  
*Conference Chair:* Eric Udd, McDonnell Douglas Astronautics Company
- Chemical, Biochemical, and Environmental Applications of Fibers  
*Conference Chair:* R. A. Lieberman, AT&T Bell Laboratories; M. T. Włodarczyk, General Motors Research Laboratories

### Two-Conference Program on **High Data Rate Atmospheric, Space, and Analog Communications**

- High Data Rate Atmospheric and Space Communications  
*Conference Chair:* Robert Hauptman, Ford Aerospace and Communications Corporation
- High Frequency Analog Communications  
*Conference Chair:* Paul Sierak, Rome Air Development Center

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- Components for Fiber Optic Applications and Coherent Lightwave Communications  
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- Fiber Optic Systems for Mobile Platforms II  
*Conference Chairs:* Norris Lewis, Litton Poly-Scientific Division/Engineering and Research; Emery L. Moore, Litton Systems, Inc./Guidance and Control Systems Division
- Fiber Optics Reliability: Benign and Adverse Environments II  
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- Integrated Optical Circuit Engineering VI  
*Conference Chair:* Mark A. Mentzer, Sechan Electronics, Inc.

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COMPUTERS AND SUBSYSTEMS

the design of its new PS/2 boards. Designers used the knowledge gained from their development of Nubus boards to fit all the components required for high-speed data acquisition on the small-format boards used in the PS/2, Truchard says.

One of the three PS/2 boards introduced by National Instruments is the MC-MIO-16, a high-performance, multifunction analog, digital and timing I/O board with a Micro Channel DMA interface. Even though the Micro Channel card size is 29 percent smaller than that of the Macintosh II, all of the functions on the Nubus board have been included in this PS/2 board, according to Audrey Harvey, engineering group leader for data acquisitions. National accomplished this, she says, by reducing component counts on the MC-MIO-16 through the use of a commercially available PS/2 Micro Channel interface gate array.

Features lend speed and accuracy

Two features of the MC-MIO-16 PS/2 board are software-programmable gain and analog-to-digital (A-D) first-in, first-out (FIFO) timing. With the PC versions, data-acquisition boards either had fixed gains determined by

the values of resistors on the boards or hardware jumpers that had to be moved to change the gain. The latter solution meant that the boards had to be removed for every gain change, which endangered the accuracy of the gain setting unless the board was handled very carefully. With software-programmable gain, however, several gain settings can be set in advance, and there's no need to access the boards physically.

An A-D FIFO gives the PS/2 boards higher throughput speeds. With PC boards, data-acquisition and throughput speeds were limited by on-board counters that had to count down before a data conversion could be initiated. The converted data was then stored until the system was interrupted by a DMA request. If the computer could respond within one sample interval, there would be no need for a FIFO because the last value stored would then be read out before the next value arrived. But latency can be highly variable, and the timing sequence can't be assured. The A-D FIFO memory buffers the inputs and allows storage of up to 16 values before the memory has to be serviced by the computer. This increases by an order of 16 the time that can be

tolerated before data is lost.

The MC-MIO-16 also provides on-board timing, a flexible automatic channel-scanning system, double-buffered D-A converters and timer-generated interrupts. It has a 12-bit A-D converter with 16 single-ended analog inputs, two 12-bit D-A converters, eight lines of TTL-compatible digital I/O and three 16-bit counter/timer channels.

Conversion times for three available versions of this board differ according to the speed of the on-board A-D converter. A 9- $\mu$ s board samples data acquired at a typical rate of 100 ksamples/s, a 15- $\mu$ s board samples at 71 ksamples/s, and a 25- $\mu$ s board samples at 45 ksamples/s.

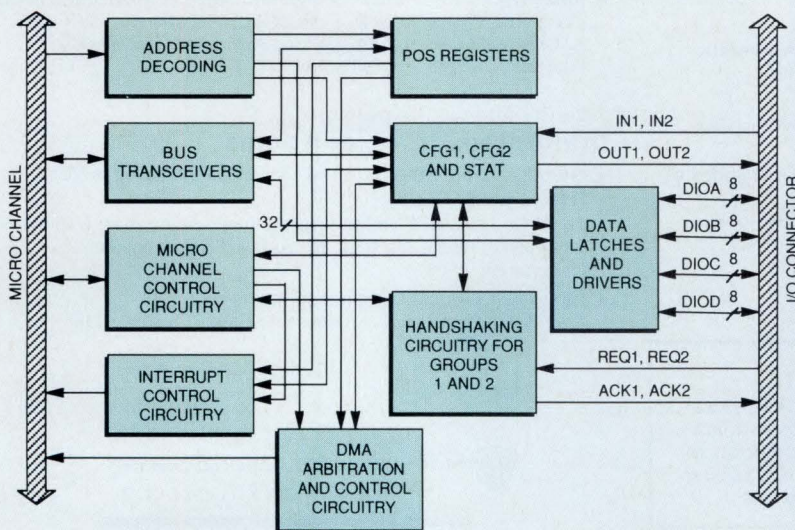
Completing the set

A second PS/2 board, the MC-DIO-32F, is a high-speed 32-bit parallel digital I/O interface that features a maximum DMA transfer rate of 400,000 16-bit words/s. Its 32 lines of digital I/O are divided into 4 bytes, with each byte programmable as input or output. Compatibility to a wide range of peripheral devices and other computers is attained through several digital I/O handshaking options. Two DMA channels can receive 16-bit transfers simultaneously.

Completing the picture is the MC-DIO-24, a 24-bit parallel digital I/O interface for applications that don't require more than a maximum transfer rate of 300 kbytes/s. A programmable peripheral interface controls 24 bits of digital I/O. This board can operate in either unidirectional or bidirectional mode and can generate interrupt requests.

A salient feature of these new boards, according to National Instruments' Harvey, is a timing bus that the company had first developed for Nubus data-acquisition boards. Conventional computer buses don't provide high-speed timing signals because they're more concerned with data transfers, addressing and interrupts. But data acquisition requires timing signals between boards, and timing buses provide the necessary paths for these signals. This feature, plus the inherent speed of the PS/2 Micro Channel, provide a solid platform for the PS/2 as the eventual successor to the PC and the PC AT for data-acquisition applications.

THE MC-D10-32F PS/2 BOARD



Although much of the expertise for development of National Instruments' line of data-acquisition boards for the IBM Personal System/2 Micro Channel bus architecture resulted from the company's experiences in designing similar boards for Apple Computer's Macintosh II, comparable functions could be included on the PS/2 boards only through use of Micro Channel interface gate arrays.

## SCSI adapter ties computers and peripherals into Ethernet

Tom Williams, Western Managing Editor

**A** new, flexible LAN interface unit lets any device using the small computer system interface (SCSI) connect to any Ethernet network. The SCSI-based Nodem from Adaptec (Milpitas, CA) acts as an Ethernet interface for systems that already have SCSI. The connecting device can be a peripheral—such as a disk drive or a printer—or a computer system. When the device is a computer, network-based applications can be easily ported to Ethernet or written specifically for Ethernet by using protocols to Ethernet's data-link layer of the Open Systems Interconnection model.

Since SCSI supports eight devices per controller, a Nodem link to Ethernet can be daisy-chained with other SCSI devices such as disk or tape drives. The SCSI sees the Nodem as just another device on the SCSI bus.

### Low-cost interface to Ethernet

Adaptec developed the unit because the company saw a need for a low-cost interface to Ethernet from IBM PC XTs and PC ATs, Apple Macintoshes, minicomputers and so forth, according to Joe Carballosa, Adaptec's LAN product manager. Adaptec has initially targeted its hardware and software product for the Macintosh because it has a built-in SCSI port. The software lets applications written for the Appletalk protocols run unmodified on Ethernet.

Adaptec will also soon offer similar protocols for IBM PCs and compatibles running DOS, as well as for OS/2 and its LAN manager. Any computer with a SCSI adapter and software to access Ethernet will be able to use the Nodem. Initially, Adaptec will adapt popular network software to the Nodem, but third parties can also easily write or adapt applications to the Ethernet protocols.

Adaptec designed the Nodem interface without using any specialized Ethernet silicon. In addition to a microprocessor and memory, the Nodem uses Adaptec's AIC-6250 SCSI controller and AIC-011 serializ-

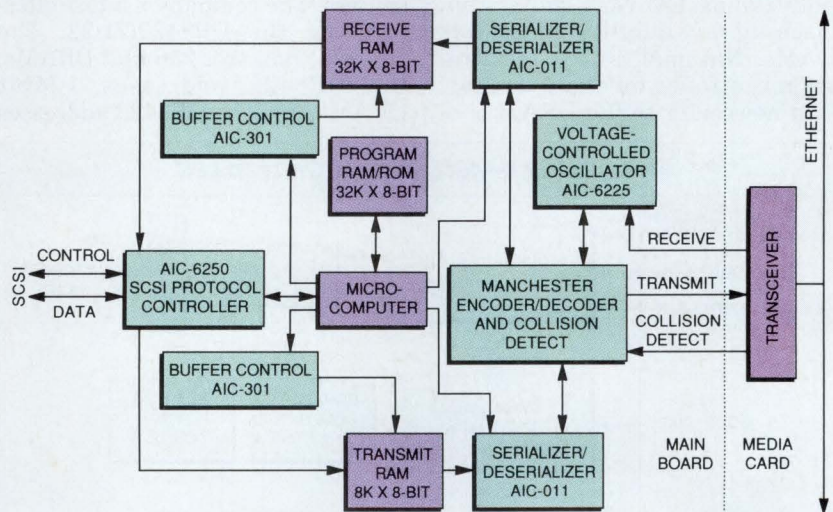
er/deserializer (Serdes). The Serdes, which is used in SCSI disk controllers to encode sector formats, is flexible enough to encode the data packets Ethernet uses.

### A speed advantage

Connecting to Ethernet via the SCSI port gives microcomputers like the Macintosh a definite speed advantage. Because SCSI runs at about 8 Mbits/s (1 Mbyte/s) in its asyn-

In addition, the intelligent nature of SCSI fits well with a network such as Ethernet, which uses CSMA/CD (carrier sense multiple access/collision detect) protocols. Such networks are fairly unpredictable in terms of exactly when a request for access or data will be granted. SCSI's disconnect/reconnect ability lets an interface accept a request and data from the host, then free the host until, for example, the interface has obtained access to the network, has transmitted the packet, and needs more data. The interface then can "reconnect" with the host by issuing an interrupt without the host having to poll it. By the same token, the host doesn't need to get involved with trying to gain ac-

### THE NODEM SCSI-TO-ETHERNET LINK



The Adaptec Nodem is built from off-the-shelf parts that include a microcomputer, RAM and ROM, and from Adaptec ICs for use in SCSI controllers for tape and disk-type peripheral controllers. No specially designed Ethernet ICs are needed. The Nodem can interface to standard Ethernet, Cheapernet or twisted-pair Ethernet.

chronous mode, it's on a fair speed parity with Ethernet and lets systems take nearly full advantage of Ethernet's 10-Mbit/s bandwidth. SCSI II, expected to run at around 4 Mbytes/s in synchronous mode, will have speed to spare. Applications that use Appletalk can run at only 230 kbits/s using Localtalk, Apple's physical and data-link architecture. This difference in speed means that 254 Appletalk nodes can be connected via Ethernet, compared to only 32 connected via Localtalk.

cess. SCSI also has a target/initiator mode that allows easy peer-to-peer communication: any SCSI device can either initiate a connection or be the target of a communication.

Adaptec plans to expand the SCSI-to-Ethernet link to include other LAN standards such as IEEE 802.5 token ring, according to Carballosa. Since a single SCSI host adapter can accept up to eight devices, multiple Nodems could be placed on a single host to act as gateways between different network architectures. ■

INTEGRATED CIRCUITS

# Fast, full-featured 4-Mbit DRAM controllers begin to surface

S. Louis Martin, Contributing Editor

The first 1-Mbit dynamic RAM controller appeared just two years ago, with the inconspicuous introduction of the huge, complex WE32103 chip from AT&T (Berkeley Heights, NJ). Designers generally felt, however, that the AT&T part was overkill for their needs. National Semiconductor (Santa Clara, CA) and Monolithic Memories (Santa Clara, CA) were the next vendors to introduce competitive 1-Mbit DRAM controllers, followed about a year later by Advanced Micro Devices (Sunnyvale, CA) and Texas Instruments (Dallas, TX). Now, with the approaching availability of 4-Mbit DRAMs, National is first to introduce a controller for those devices, and a newcomer to the DRAM con-

troller market—Korean Samsung Semiconductor (San Jose, CA)—is in hot pursuit.

Considering the huge consumption of DRAMs as opposed to static RAMs and other types of memories, it's surprising that there are relatively few vendors offering controllers for DRAMs. Clearly, Samsung and National Semiconductor have recognized the importance of the DRAM controller at an opportune time.

For each new generation of DRAMs, National Semiconductor has consistently produced controllers. The company's latest offerings are the DP8420/21/22. The DP8420 addresses 256-kbit DRAMs; the DP8421 addresses 1-Mbit DRAMs; and the DP8422 addresses

the upcoming 4-Mbit devices. The devices are functionally identical, except for the DP8422's provision for dual-accessing.

## New features lend flexibility

The previous generation of controllers from National (the DP8428 and DP8429) offered the basics of DRAM support, such as DRAM drivers, refresh counters, row/column multiplexing and multiple row-address strobe (RAS) lines for activating multiple banks of DRAMs. The new generation offers important additional features, many of which National and Monolithic Memories criticized as overkill in the AT&T chip two years ago. However, the new design keeps the pin count down to 84 pins on the DP8422, compared to the AT&T part's 132 pins.

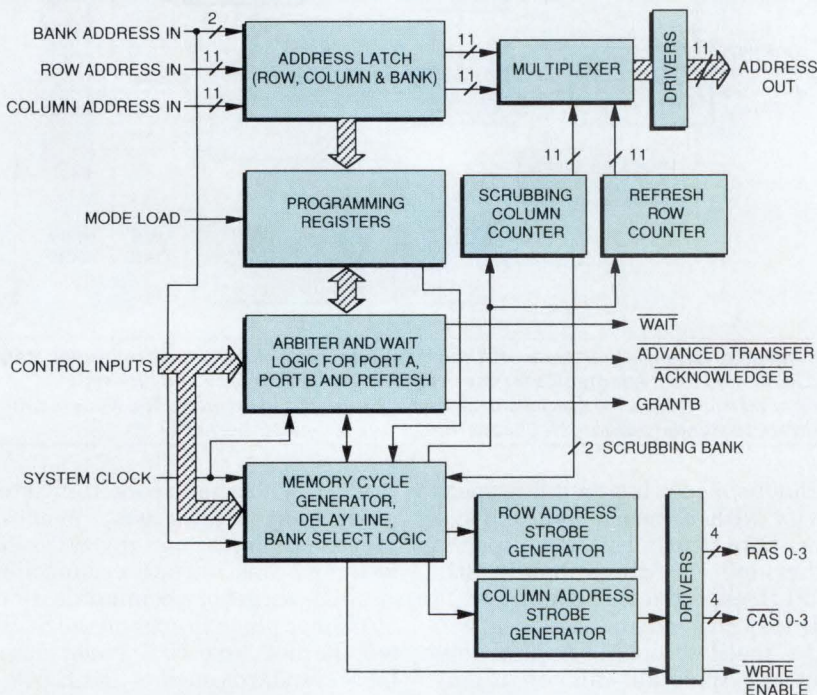
Probably the most striking new feature of the National part is its programmability. "It allows the controller to be interfaced to all the major processors," says Timothy Garverick, design engineering manager at National. This is accomplished by loading a 22-bit register at power-up.

Another new feature of the DP8422 is dual-port access, which is particularly useful in cases where two independent processors need to access the same bank of DRAM. This isn't an uncommon situation, according to Garverick. "Laser printer applications in particular benefit from dual-port access," he says. For instance, when National's 32CG16, which is a special processor for graphics, is used in conjunction with another general-purpose processor, dual-port access lets both processors access memory through a single DRAM controller.

The National device features access/refresh arbitration, a process that's new to industry, according to Michael Sodergren, National's manager of interface product marketing. Access/refresh arbitration is accomplished by providing a wait signal to the processor during refresh operation to hold off access. Providing the arbitration signal from the DRAM controller saves at least one chip in the memory-system design.

The DP8420/21/22 also provide four column-address strobe (CAS) outputs, CAS0-3, which can be asserted independently. Each CAS out-

### THE DP8422 4-MBIT DRAM CONTROLLER



The DP8422 from National Semiconductor is a full-featured, 4-Mbit dynamic RAM controller that's programmable for just about any microprocessor. In addition to programmability, it includes access/refresh arbitration, multiple row-address strobe and column-address strobe for bank selection and byte or word access. It also allows dual-accessing of DRAMs by two separate processors.

## INTEGRATED CIRCUITS

put can be used to select 1 byte from a 32-bit-wide memory, letting the memory system respond with any combination of the 4 bytes in a word. The CAS outputs were a feature of the previous-generation Monolithic Memories part that National chose to add to its latest controller.

### ■ Determining in-circuit speed

National rates the latest version of the controllers, due for availability sometime soon, at 25 MHz. While this is a succinct way to state the speed of the parts, it doesn't tell the designer much about how fast the controller will work in-circuit. For that information, designers have relied on other figures entirely.

In the older generation of controllers, the favorite basis of comparison was the delay time between the RAS input and the assertion of CAS low, often referred to as tR1CL. But in the new-generation chips that include their own microprocessor interface, the most appropriate measure is the delay between address strobe low and CAS low, known as tPADSCL.

Because National's parts are programmable, the picture is more complicated. The RAS address hold time (tRAH) and the address setup to CAS time (tASC), programmable in the new devices to accommodate different types of DRAMs, both affect tPADSCL. So the speed of the part has to be stated with reference to its programming. For instance, when tRAH is programmed to be 15 ns and tASC is programmed to be 0 ns—a fairly typical setting for conventional DRAMs—tPADSCL is 79 ns for the 25-MHz National part.

An even more meaningful measure of performance can be obtained by calculating the required number of wait states for a particular processor that's operating at a specified frequency and working with DRAMs with a specified access time, according to Garverick. For instance, an 80386 processor operating at 20 MHz and using 100-ns DRAMs will need one wait state in pipelined access mode and two wait states in nonpipelined mode.

The DP8420/21/22 are CMOS devices. The price for the DP8422 is \$25.30 in quantities of 1,000 for the 25-MHz part.

Samsung Semiconductor sees its

**"We expect that once we go through the normal cycle of process optimization, we should be up around 40 MHz."**

—Mike Levis, Samsung Semiconductor



entry into the DRAM controller market as an important step. "Samsung is a very large supplier of memory products, and our intent here is to position ourselves as the leading supplier of memory-system components," says Mike Levis, product marketing manager.

Samsung is about to introduce 1- and 4-Mbit DRAM controllers, the KS84C21 and the KS84C22, respectively. The Samsung devices are

quite similar to the National devices, according to Levis. "Our parts are a superset of National's implementation, and we have a lot of added features," he says. While the word "superset" may overstate Samsung's case, the parts do combine many of National's features with some exclusive to the Korean vendor.

Multiple RAS and CAS (RAS0-4 and CAS0-4) will be available on the new parts, just like on the National parts, allowing for multiple bank selection (up to four banks) and for byte access as well as word access. Any combination of bytes within a 32-bit word, as well as the entire 32-bit word, may be selected.

The first product to be available will be a 25-MHz device, like the upcoming revision of the National part, but Samsung also expects to introduce a 40-MHz version soon. Current silicon tests at just under 40 MHz, claims Levis. "We expect that

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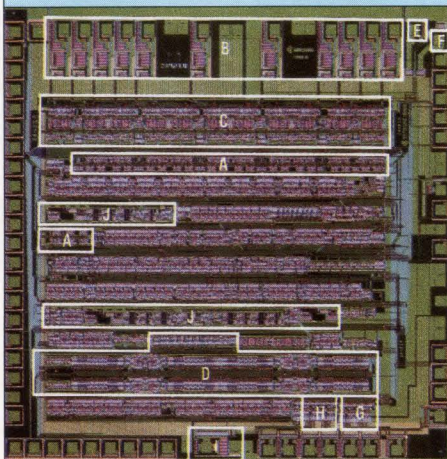
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INTEGRATED CIRCUITS



The KS84C22 dynamic RAM controller from Samsung Semiconductor is functionally very similar to National Semiconductor's DP8422. Multiple column-address strobe (G) and row-address strobe (RAS) (H) allow for multiple bank selection (up to four banks) and for byte access and word access. Software programming and mask programming (A) are available. The device also features 11 address outputs (B); a row/column multiplexer (C); RAS bank decoding (D); WAIT, RFIP and WE drivers, (E), (F) and (I), respectively; and a precision delay (J).

will be \$24.70 in quantities of 1,000 for the 4-Mbit version.

Followers and dropouts

AMD will also introduce a 4-Mbit device soon—later this year or early next year. Monolithic Memories, which has merged with AMD since the introduction of its 1-Mbit device, will not be introducing a 4-Mbit device, according to a company spokesperson. Texas Instruments, which introduced its 1-Mbit DRAM controller last October, is especially worth watching. The company will soon announce a toolkit with special macros for DRAM control that will allow multi-accessing with up to four different interfaces/processors. Moreover, with the new tools, controllers

can be built for DRAMs up to 16 Mbits.

Some important vendors won't be introducing 4-Mbit parts. AT&T, which was accused of producing a battleship-size device that tried to do it all in the 1-Mbit generation, apparently has no plans in the 4-Mbit arena. This is perhaps ironic, since the current hot contenders seem to be following AT&T's lead in producing high-functionality devices. Intel, which is busy with other projects, appears to have lost interest at the 256-kbit level.

With the delay in the introduction of 4-Mbit DRAMs, it's hoped that controllers will be available when the DRAMs actually arrive in full force sometime next year.

First 1-Mbit SRAMs foreshadow changes for users and vendors

Ron Wilson, Senior Editor

once we go through the normal cycle of process optimization, we should be up around 40 MHz," he says. For the 25-MHz Samsung part, when programmed for tRAH=15 ns and tASC=0 ns, tPADSCL is 85 ns—6 ns slower than for the similarly programmed National part. But Samsung's 40-MHz device should bring that value down considerably.

The Samsung devices will also be register-programmable, with two varieties available. A software-programmable version is intended for small-volume applications for which it's anticipated that the access mode could change. For higher volume applications, there will be a mask-programmable version. "Once the application development is completed, the customer can then give us the register profile and we can program it via mask programming. You then have a much more reliable implementation," explains Levis. Access/refresh arbitration will be available on the Samsung part, but not dual accessing.

Initial beta sampling is now in process. The target date for introduction of the KS84C21/22 is September. The devices are both CMOS. The price

Long after initial disclosures, two vendors—Toshiba America (Irvine, CA) and Hitachi America (San Jose, CA)—have announced planned availability of 1-Mbit static RAMs. The new parts will be dense enough and fast enough to offer a serious alternative to dynamic RAMs in many applications. But the technology necessary to build the parts may limit the supply, excluding domestic vendors and keeping the price per bit at premium levels.

Both the Hitachi and Toshiba parts have the same general specifications: 128k×8-bit organization and 70-ns access time. These figures make it quite practical to use the parts as main memory in microcomputer systems, where substituting the parts for DRAMs should result in significantly simpler memory design.

The parts may offer their greatest advantage, though, in laptop personal computers. In these applications, where battery life is becoming an important competitive issue, two characteristics of the new SRAMs make them particularly important. First, both parts have inherently low power consumption. "The continual recharging required by DRAMs consumes a good deal of current,

whether the parts are being accessed or not," says Ron Bechtold, Hitachi product marketing engineer. "In contrast, the standby current for the megabit SRAM is about 1 mA." During an access, the consumption rises to about 45 mA at 5 V.

The second power-saving trait—the ability to retain data at low supply voltage—can be even more important for battery-driven systems. "The SRAM cell has been designed to retain data at supply voltages as low as 2 V," Bechtold says. "This mode lets a computer memory retain data on a lithium battery, for instance, with extremely low current drain. At 3 V, the current consumed for data retention will typically be around 1 μA."

The ability to retain data at such low power not only reduces current demand from the memory itself, but can also substantially reduce the much larger demand for current required by disk operation. Since memory can retain all data with the system power essentially off, it isn't necessary for a computer to save data before shutdown, or to reload program and data after power-up. So disk accesses are necessary only when a new program is started, or when data is moved to disk.

# Omnicom<sup>TM</sup>

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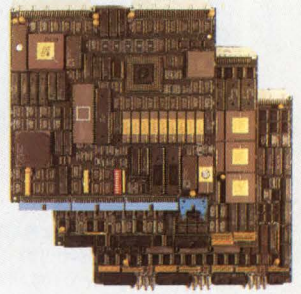
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- DEC DMA Compatible
- Up to 52 Planes with 4 Overlays
- 1280 x 1024 Resolution
- Hardware Cursor, Zoom, Pan
- GKS Display List Processing
- 10 Mega Pixels/Second
- Up to 3 Graphics Channels
- 2D & 3D Wireframe
- 70 MIP Image Processing
- Local Input Device Support



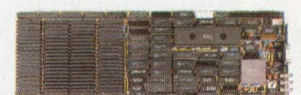
### OMNI 1600 GDC

- GKS Display List Processing Via OMNI 1500 DLP
- Up to 256 Simultaneous Colors
- PC/AT Compatible
- Hardware Cursor, Zoom, Pan
- Palette from 4096 to 16.7 Million Colors
- Viewable Resolution 1280 x 1024 x 8, Plus 4 Overlays
- Addressable Resolutions 2048 x 1024 x 8, Plus 4 Overlays



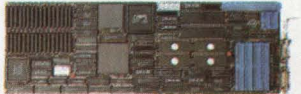
### OMNI 1400 GDC

- PC/AT Compatible
- Up to 256 Simultaneous Colors
- Palette: Up to 16.7 Million Colors
- GKS Display List Processing Via OMNI 1500 DLP
- Hardware Cursor
- Viewable Resolution: Up to 1280 x 1024 x 8, Plus 2 Overlays
- Addressable Resolution: Up to 2048 x 1024 x 8, Plus 2 Overlays



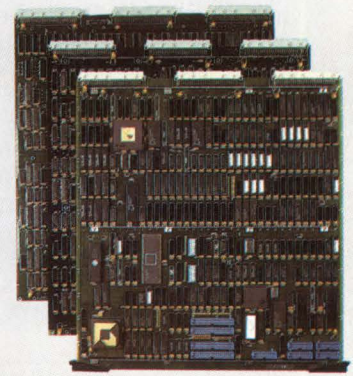
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- DEC DMA Compatible
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- 80386/80387 Display List Processor
- 1 to 4 Megabytes of DLP Memory
- 4 RS-232-C Serial Ports
- OMNI 1500 GDS is an OMNI 1500 DLP plus 1 to 8 OMNI 1600 GDC's

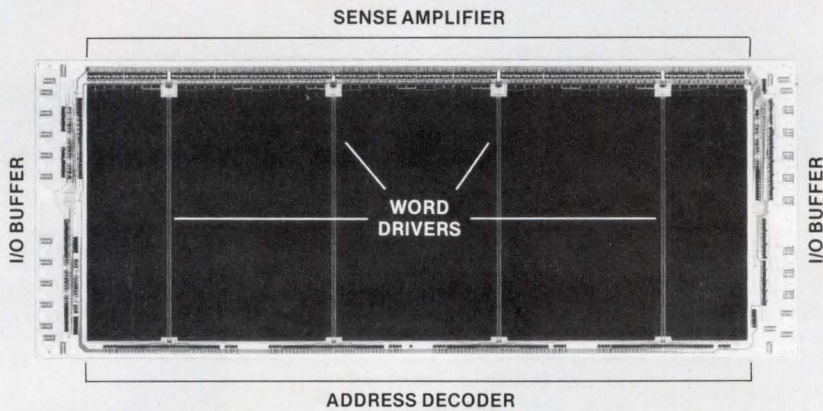


### OMNI 2000 GDS

- MULTIBUS II 9U x 400 mm
- DEC DMA Compatible
- GKS Display List Processing
- Viewable and Addressable Resolution: 1280 x 1024
- Hardware Cursor
- 2 Overlay Planes
- Modular Configurations
- Multiple Processors
  - Geometry Processor: Am29116
  - F.P. Coprocessor: Am29325
  - Graphic Coprocessor: Discreet
  - Peripheral Coprocessor: 80188
  - Display List Processor: 80386/80387



INTEGRATED CIRCUITS



Hitachi's 1-Mbit static RAM is one of the first devices to reach commercial availability with an 0.8-micron geometry. This component density, which is so fine it renders details of the memory array virtually invisible to conventional microphotography, may prevent U.S. sources from producing the parts.

Dan Pichulo, Hitachi product marketing manager, suggests another design that exploits the very low standby current of the SRAMs. "It's feasible now to build a data cartridge containing a substantial amount of SRAM and a backup battery. The cartridges would plug into a personal computer or terminal for use. In this way, a businessman, for instance, could carry his whole working set of data in a few cartridges." The cartridges could eliminate removable disks for many portable systems.

**Few sources likely**

While the new parts will be uniquely suited to many applications, cost per bit isn't likely to be their attraction. "The megabit DRAMS and 256-kbit SRAMS are mostly built using a 1.3-micron process," Bechtold says. "But to get to the 4 to 5 million transistor level for a 1-Mbit SRAM, you need a 0.8-micron process. The finer geometry means more processing steps, which means lower wafer throughput. So I don't expect the cost per bit of these parts to drop as fast as costs for 256-kbit parts did."

The need for 0.8 micron  $l_{eff}$  will do more than add processing steps. For many existing SRAM vendors, the requirement may be an almost insurmountable barrier to entering the 1-Mbit market. "At this point, getting into the 128k x 8 market means building a new fab," says Sally Withers, Hitachi senior product marketing engineer.

"The processing requirements for these parts are essentially the same as those for 4-Mbit DRAMs," adds Bechtold. "These parts can't be built on existing lines. Anyone who wants in is looking at about \$100 million in startup costs just for the fabrication facility." While sources at Toshiba don't agree that new fabrication facilities are necessary for building 1-Mbit SRAMs, they do say that their part also depends on 0.8-micron geometry.

Not only is the investment in processing equipment a barrier, but experience with the technology will

also weigh against American entrants. "It's going to be hard for the U.S. fabs to catch up, because they haven't been playing in the byte-wide market at lower densities," argues Pichulo. "Right now 90 percent of the byte-wide parts in the United States are imported."

**Obstacles block U.S. vendors**

Taken together, the barriers of entering late, overcoming lack of experience with the parts, and paying for new equipment would seem to eliminate most U.S. vendors from the market. This suggests that in high-density SRAMs, as in DRAMs, U.S. users will be almost entirely dependent on Japanese vendors.

But DRAM and SRAM products tend to be the technology drivers for other CMOS devices, both standard and semicustom. Failure to participate in the round of development that's producing the 1-Mbit SRAMs and 4-Mbit DRAMs could force many U.S. vendors of standard parts and application-specific ICs to become front-ends for Japanese fabrication facilities, simply because of U.S. vendors' inability to compete in process technology. First indications of such a shift can already be seen in relationships between some design houses and Japanese fabs. But the long-term implications of such an industry restructuring aren't yet apparent.

**Self-clocking PLD implements asynchronous interfaces**

Ron Wilson, Senior Editor

The asynchronous bus-arbitration protocols used by most backplane buses present a serious design problem. Ideally, the protocols would be handled by an asynchronous state machine. But in the real world, bus interfaces are built from PALs that depend on a single external clock signal and hence implement synchronous state machines. This mismatch cuts performance and can cause the interface to fail. Advanced Micro Devices (Sunnyvale, CA), however, has designed a PAL that addresses these problems with a

unique self-clocking flip-flop design.

To understand how the new PAL helps solve the problem, it's necessary to understand the problem itself. An ideal asynchronous state machine would issue a bus request as soon as a board requested the bus. When the bus grant signal arrived, the machine would immediately take control of the bus and begin its transactions.

But, because of the external clock requirement common to PALs in real-world bus interfaces, the bus-arbitration logic on a board can't re-



## INTEGRATED CIRCUITS

spond immediately to inputs. For example, the logic will typically clock an incoming bus grant into a D-type latch on one clock cycle, feed that signal back into the AND array of the PAL, and clock the bus grant signal back onto the VMEbus on the next clock cycle.

The most obvious problem with this approach is the delay introduced by the clock. Even if the board designer clocks the PAL at its maximum frequency, precious nanoseconds will be lost in the one or two clock cycles between the arrival of a bus grant and the beginning of a transfer. These delays particularly add up as a bus grant signal daisy-chains through a number of boards, picking up a two-clock-cycle delay at each board.

But there's a problem that's more severe than accumulating clock delays: metastability. Since there's no way to synchronize arriving signals with the PAL clock, once in a while a latch is going to be clocked while a signal, such as bus grant, is in transition. If the latch clocks while its input is between valid logic 0 and valid logic 1, the latch may go into temporary oscillation, or it may get stuck in an invalid state. These misfortunes can crash the board or the bus.

### ■ A self-clocking flip-flop

AMD decided to attack the problem by designing an entirely new kind of flip-flop. "The idea started with one of our designers who had a background as a VMEbus user," says Andy Robin, AMD director of marketing for the programmable logic group. "He was tired of fighting with asynchronous signals, so he asked the circuit designers to come up with a self-clocking flip-flop."

After initial misgivings, followed by considerable investigation, the circuit designers succeeded in producing such a device. Instead of triggering on a separate clock signal, the flip-flop triggered on the rising edge of its data input. The device could thus be used to capture a signal as soon as it arrived, rather than one clock cycle later. And there was no chance that the flip-flop could be put in an indeterminate state.

Not only was the device unlike any of the macrocells in existing PALs, it was unlike any existing flip-flops.

Since the circuit development was aimed at speed-critical bus interface applications, AMD developed the device in the same bipolar process used in the company's 10-ns PAL family. The unique self-clocking input circuitry was ready to become the basis for an equally unique set of flip-flops in a new bipolar PAL.

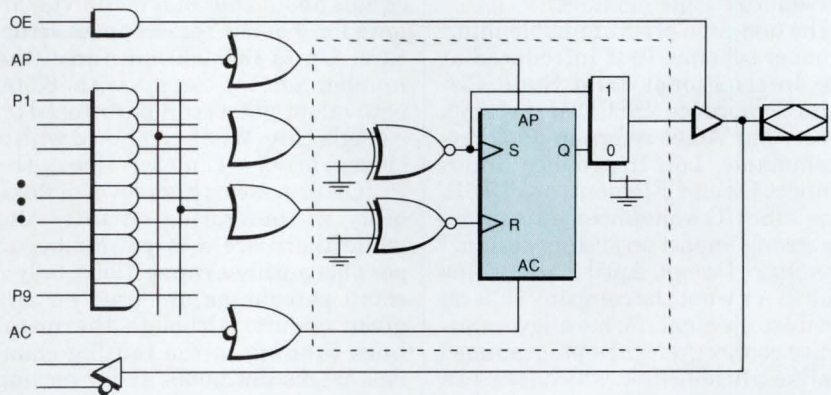
### ■ First use in protocol PAL

AMD chose to use the new technology in the I/O macrocells of a bipolar

positive edge on the R input will reset the flop. Note that, unlike a conventional S-R flip-flop, the device is sensitive only to edges, not to levels, on the S and R inputs. The 2-T flip-flop will toggle on any positive edge on the T1 or T2 input. Like the S-R inputs, the 2-T T-inputs are only edge-sensitive, not level-sensitive.

In a second break with conventional design, AMD has used a product-term steering scheme to allocate the nine product terms that

### THE INTERFACE PROTOCOL ASYNCHRONOUS CELL



*Self-clocking flip-flops are key to the operation of Advanced Micro Devices' new IPAC PAL. The devices, implemented in both S-R and 2-T configurations in the IPAC's I/O macrocells, are clocked by an active edge on their inputs rather than by a separate clock signal.*

PAL, the 22IP6 Interface Protocol Asynchronous Cell, or IPAC. The part appears to be a conventional 16-input, six-I/O-macrocell, registered PAL. But there are two significant differences between the 22IP6 and other bipolar PALs.

The first is AMD's use of edge-activated flip-flops in the macrocells. There are actually two different configurations used: three of the flip-flops are edge-activated Set-Reset (S-R) flops, and three are edge-activated, two-input T-type flops that AMD designates as 2-T flip-flops. Neither device behaves quite like its conventional counterpart.

The S-R device acts somewhat like a conventional S-R flip-flop, but with the clock coming from the inputs, not from a separate pin. When a positive edge arrives at the S input, the flop sets. The device will ignore any further activity on the S input as long as the Q output remains high. But a

come into each macrocell. The nine terms are available to both of the flip-flop inputs in a cell, but on a mutually exclusive basis. That is, if one input uses five of the terms, only the remaining four are available to the other input.

With a total input-to-output propagation delay of 35 ns, the device is comparable in speed to clocked implementations with 10-ns bipolar PALs, since the IPAC won't incur clock delays to align asynchronous input signals with the master clock. And the device may, in fact, have important applications other than bus interfacing in the design of asynchronous state machines. But asynchronous design has been long avoided as complex and dangerous compared to synchronous design. So users may have to change their thinking a bit before they fully appreciate the value of AMD's circuit innovation. ■

## User-configurable arrays bridge gap between gate arrays and PLDs

Warren Andrews, Contributing Editor

A new family of customer-configurable, channeled arrays from Actel (Sunnyvale, CA) called ACT 1 offers users the flexibility of mask-programmed gate arrays and the convenience of PLDs. Including anywhere from 1,200 to 6,000 equivalent gates, ACT 1 uses a proprietary interconnect technology to personalize logic modules.

The one-time-programmable interconnect scheme, first introduced at the International Solid State Circuits Conference (ISSCC) last spring, uses what Actel refers to as a Programmable Low-Impedance Interconnect Circuit Element, or PLICE. (See "ISSCC announcements promise strong impact on system design," *Computer Design*, April 1, p 29.) This PLICE, or what the company calls an antifuse element, forms a low-impedance connection when programmed (unlike a fusible link, which forms an open circuit when programmed). One of the key advantages of the PLICE is its relatively small size, compared to the metal fuses used in programmable array logic or the transistor

switching elements used in electrically programmable logic devices (EPLDs). In addition, on-resistance is lower than that of most transistor-based circuits, resulting in devices with better performance.

### Dense interconnect structure

The small size of the PLICE, which equals about that of a metal via, allows for a dense interconnect structure. Up to 666,000 antifuses (the number on the array with 6,000 equivalent gates) can be diffused on a single chip. When combined with a clever array of metal lines, the PLICE provides a high level of flexibility in configuring circuits. And while there are a large number of possible antifuse connections, only a small percentage are used on any given circuit. Although the metal lines running in the routing channels are discontinuous and of varying lengths, they can form longer lines by using antifuse connections.

The PLICE antifuse programming element consists of a dielectric material sandwiched between a pair of

conductors. At normal operating voltages, the PLICE exhibits a high resistance of around 100 M $\Omega$ . When a programming voltage of 18 V is applied to the two conductors, however, the dielectric breaks down, resulting in a low-resistance, bidirectional connection of less than 1,000  $\Omega$ . The PLICE requires less than 10 mA of programming current for a duration of less than 10 ms. While programming times might become excessive if all 600,000-or-so antifuses had to be programmed, only about 2 to 3 percent of the total available elements are usually programmed to implement a typical design, according to Amr Mohsen, president and chief executive officer at Actel.

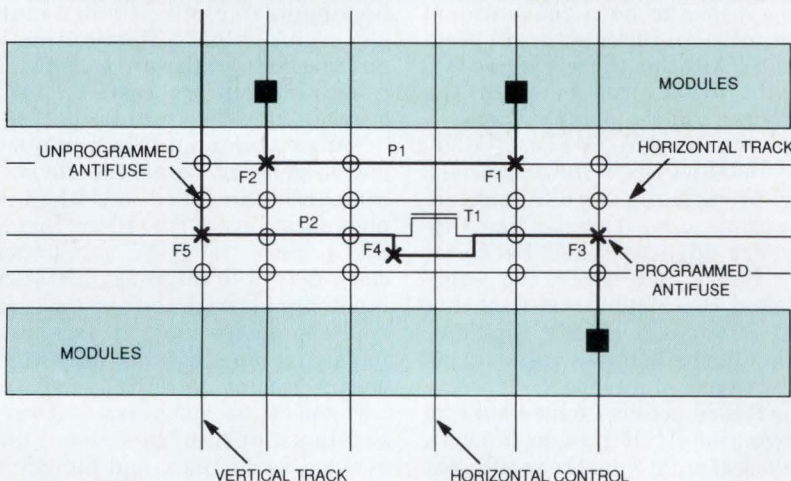
The concept of an antifuse has been around for some time, but the devices have either been too complex, too large, or have required too high of a programming voltage for integration into dense ICs. Engineers have experimented with various approaches, such as the use of amorphous silicon, but these haven't been acceptable for IC applications. PLICE is being produced in a standard CMOS fab facility, according to Mohsen. And while the production of PLICE is somewhat more complex than that of conventional CMOS logic, the process "requires only a few more steps than are needed for a standard EPROM," Mohsen adds.

The Actel architecture is similar in many respects to that of conventional channeled gate arrays, except for its horizontal and vertical wiring tracks and the antifuse programming elements. The basic building block of the arrays is a configurable logic module. The arrays contain anywhere from 295 modules for the part with 1,200 equivalent gates to 1,400 modules for the device with 6,000 equivalent gates. Each module has eight inputs and a single output.

### Logic configuration

Actel's logic macros have capabilities similar to those of conventional gate array macros and can be configured into over 150 different functions. The company designed the architecture of the module so that it could efficiently implement both combinatorial and sequential circuits with the available routing resources. Since JK, D and T flip-flops can easily be configured

### INTERCONNECT ARCHITECTURE OF ACTEL'S ACT ARRAYS



The interconnect architecture of Actel's ACT arrays, which is similar to that of conventional channeled gate arrays, has routing tracks between modules and vertical tracks crossing over modules. Both horizontal and vertical tracks are of various lengths and can be joined with antifuses to make longer wiring channels.

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from the logic modules, there are no dedicated flip-flops included on the chip, unlike with most EPLDs.

The logic modules use a double-entry configuration that's also similar to that used in conventional gate

arrays. Each of the eight inputs to each module is connected to a short vertical wiring segment spanning one routing channel. Four inputs span the channel above the module, and four span the channel below the

module. The output of the module is connected to a vertical wiring segment spanning several modules. The benefit of this double-entry symmetry is that it greatly increases routing efficiency. By letting the routing algorithm select module access from either above or below, the module can achieve from 85 to 95 percent gate utilization.

The macros in Actel's library correspond to specific configurations of the logic modules. Each logic module can provide macro functions ranging from simple gates to transparent data latches and 4-to-1 multiplexers. The company's macro library contains over 200 standard logic functions, as well as a selection of commonly used TTL functions, according to Actel's marketing director, Andrew Haines.

Unlike conventional gate arrays, the Actel logic modules can implement logic functions needing inver-

THE ACT1020 VS. THE INDUSTRY-STANDARD ARRAY

	LSI Logic LL7220	Actel ACT1020
Building blocks	2,200	546
Maximum flip-flops	270	273
Maximum latches	540	546
Interconnect elements	90,000	180,000

*In a benchmark developed to measure equivalent gate counts, Actel used four standard circuits. The results of its benchmark are shown in a comparison between Actel's ACT1020 and the industry-standard LL7220, a 2,000-equivalent-gate mask-programmed array from LSI Logic.*



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sions as efficiently as they can implement noninverting inputs. The library, therefore, includes a wide choice of gates with inversion functions, both to simplify design and to eliminate extra propagation delays.

### ■ Comparison to standard arrays

Actel compares its devices to industry-standard gate arrays, rather than to EPLD devices, in terms of both density and performance. For example, the company compares its ACT1020—a 2,000-equivalent-gate device—with the LL7220, an industry-standard mask-programmed array with the same number of equivalent gates from LSI Logic (Milpitas, CA). Though the two use a somewhat different architecture, Actel claims close to parity in flip-flop and latch capacity of the LSI device (see table on preceding page). The Actel array also has twice the number of poten-

tial interconnect points as does the conventional gate array.

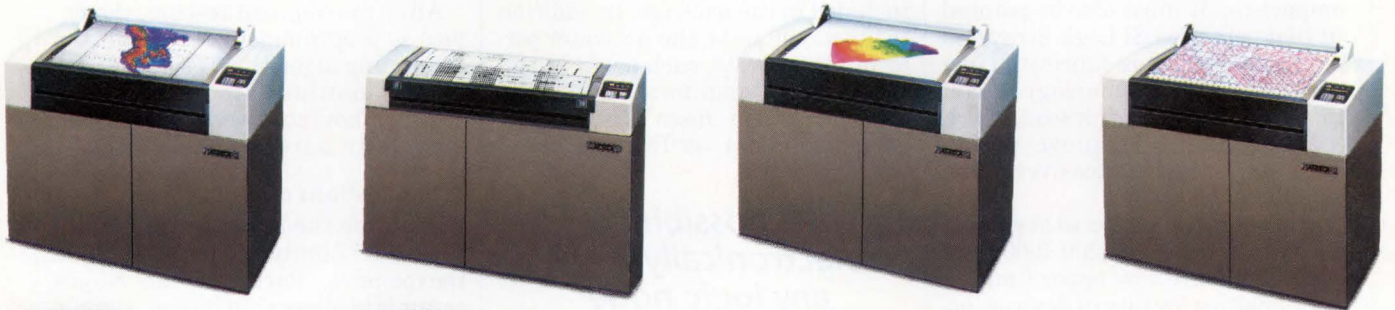
Since there are no industry-standard benchmarks against which to compare various programmable-logic architectures, Actel developed its own set of benchmark circuits, including a data-path circuit, a counter/timer, a state machine and an arithmetic structure. Using LSI's LL7220 as a reference, the array was designed to see how many of these working circuits could be included on a single chip. Each circuit consists of between 150 and 300 gates.

The comparison showed that the ACT1020 and the LL7220 could hold 12 data-path circuits and six arithmetic units. Actel's device could hold six counter/timers, the LL7220, seven; and the ACT1020 could hold eight state machines, the LL7220, 12.

Performance is an illusive measurement that can be described only

in terms of raw gate delay, flip-flop toggle frequency, multiple logic-level path delays or other application-specific timing. Actel claims a flip-flop toggle rate of 70 MHz on its 2-micron devices, which lets them function in a system clocked at 40 MHz. Again selecting its own benchmark, Actel compared a worst-case, critical-path delay for a 16-bit counter with its part versus the same function implemented on an LSI Logic array. The counter using LSI's macros ended up with a critical path 11 nets deep. Using the Actel device, the critical path ended up only six nets deep. The savings in nets (and thus gate delays) was due to the built-in inverters (negation) and flip-flops, with integral multiplexers eliminating inverters and other additional logic, says Haines.

When derated for worst-case process, voltage and temperature varia-



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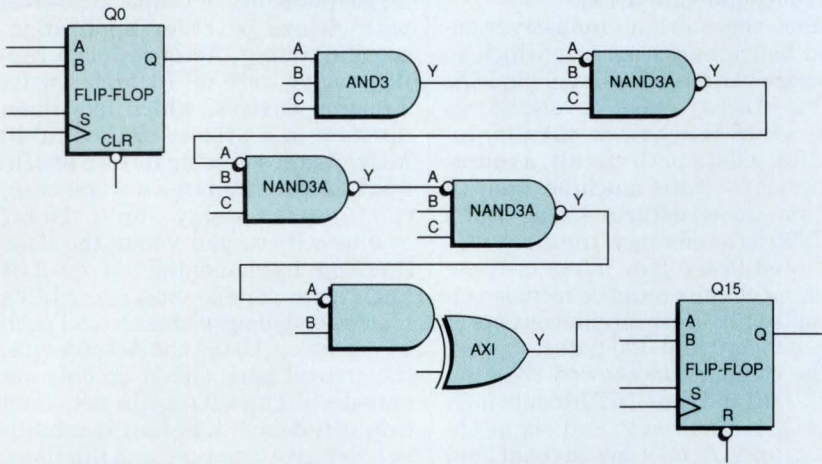
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CRITICAL PATH OF ACTEL'S ACT ARRAYS



Actel uses a 16-bit synchronous binary counter critical path as a test circuit to measure delays of Actel's ACT arrays versus a standard LSI Logic gate array.

tions, the LSI array displayed a 54-ns delay while Actel's device took 64 ns. Considering the delays intrinsic in a programmable device, such as wiring delays and antifuse resistance, the test results show a reasonably fair comparison. It must also be pointed out that both the LSI Logic array and Actel's ACT1020 are fabricated in a 2-micron CMOS technology. Actel will be doing a die shrink soon, which will significantly improve performance as well as reduce overall die size, Mohsen says.

Actel offers three devices at equivalent gate densities of 1,200, 2,000 and 6,000. But there's no upper limit on gate densities for future devices, according to Mohsen. "There's no reason ACT devices can't increase to 10,000, 20,000 or even more equivalent gates," he says. Just like conventional gate arrays, however, higher-density devices will be limited by the number of bonding pads, a function of the perimeter of the chip.

**Accompanying design system**

The key to almost any customizable device—provided it's functionally compatible with the application—is the design system with which the engineer programs a device. Actel's Action Logic software system has three components: a logic design system; a programming and test program called the Activator; and a diagnostic option providing in-circuit diagnostic and debugging capabilities.

This design system takes the engineer from schematic capture, simulation, timing analysis and electrical rule checking through placement and routing. Both hardware and software for programming and test are included in the package. In addition to functional tests, the Activator performs other tests, such as an initial test prior to programming to make sure the chip hasn't been programmed and a verification test to

***It's possible to electronically view any logic node on the chip.***



ensure that antifuses have been programmed correctly.

Some of Actel's test capabilities are achieved through two Actionprobe diagnostic circuits included in the chips. Using the Actionprobe diagnostics, the engineer can electrically connect any two points in the device to a pair of external pins. Because of the logic configuration and extensive routing channels, it's possible to electronically view any logic node on the chip. This type of probing permits 100 percent observability of all internal nodes in the array—including activity usually "buried" in the array.

The Actionprobe capability exists even when a chip is in a user's system and operating at speed. The feature can shorten design verification and in-system debugging time and also reduce the burden of test-vector generation by substituting the use of in-system stimuli. Actel's Action Logic System is available in an 80386 version that provides an interface to the schematic-capture and simulation capabilities from Viewlogic Systems (Marlboro, MA).

Automatic place and route algorithms included in the Action Logic package are unique to Actel's channeled array architecture. The company claims that the routing program will route 100 percent of the nets at device-utilization levels of 85 to 95 percent. The router operates in three phases. The first two include constructive placement and optimization—much the same way that conventional gate array placement software operates. The final phase uses a proprietary Actel routing algorithm to interconnect macros and wiring channels.

After routing and testing, the device is programmed. A special programming algorithm is then used to "blow" antifuses in a particular order so that they don't interact with previously activated antifuses.

**Implications of the device**

Due out on the market next month, the ACT 1 family of devices won't be inexpensive. Packed in an 84-pin ceramic leadless chip carrier, sample quantities of the ACT1010 will sell for \$70. The ACT1020 will sell for \$115. The Action Logic System, including an 80386-based workstation, is priced at \$19,950.

The growing availability and versatility of benchtop programmable devices will undoubtedly take its toll on the conventional low-end gate array business. But despite such products as Actel's ACT 1 family, mask-programmed arrays still hold not only a fairly large performance edge, but also a definite cost edge in volume production. Unquestionably, however, the ability to program a device on the benchtop is, and will continue to be, a major boon to prototype development and preproduction manufacturing.

## Network licensing forces new look at needs of individual EDA users

Richard Goering, Senior Editor

It sounds like a CAD manager's dream—the ability to purchase electronic design automation (EDA) software that can be used anywhere on a network. But network licensing is a complex issue that could radically change the pricing structure of the EDA industry and could usher in an era of conflict between EDA users and some vendors.

Most EDA vendors today use node licensing (also called CPU locking), which means that each piece of software is licensed to run on one node only. Site licensing, in which software can be accessed by any number of users, is rarely available and is very expensive. Network licensing is a new approach in which software can run on any node in the network, yet the number of concurrent users is controlled by the software vendor. Three companies, Apollo Computer (Chelmsford, MA), Valid Logic (San Jose, CA) and Cadre Technologies (Providence, RI), have taken steps in this direction.

Apollo's recently introduced Network License Server (NLS) is a utility that manages licenses, or "keys," for applications software. A user at any node can access the software as long as a key is available, and the total number of keys determines the number of users who can execute the application simultaneously. The software vendor sells the keys and can add more keys by simply giving a code over the telephone. NLS also includes tools that monitor and report on software usage.

Without waiting for a program such as NLS, Valid Logic has developed its own network licensing scheme for workstations from Sun Microsystems (Mountain View, CA). And Cadre recently announced network licensing for its computer-aided software engineering tools on Apollo, Sun and VAX workstations.

### Flexibility for a price

When network licensing becomes available, EDA vendors won't have to go to a specific node to run a piece

of software. "The main benefit is flexibility," says Stan Nissen, principal engineer at Raytheon Missile Systems (Bedford, MA) and a user of EDA tools from Mentor Graphics (Beaverton, OR). "Every one of my computers will be able to run the same software, and people will be able to move around." But, Nissen

**"Network licensing will actually simplify system administration."**

—Herrick Johnson, Apollo Computer



notes, network licensing may not make sense for an application such as fault simulation, which involves long runs at a single CPU.

Not surprisingly, EDA users are clamoring for network licensing. A recent survey by Apollo showed that

if network licensing were available, users would buy 45 percent of their software on that basis. The survey also showed that users would buy 25 percent fewer licenses, but would be willing to pay a 35 percent premium over existing node-licensed prices.

As a major Apollo OEM, Mentor Graphics is under a lot of pressure to support network licensing—but the company is proceeding with caution. "There's a misconception that network licensing will make software free and system administration easier," says Gerry Langelier, Mentor president and chief operating officer. "It won't make software free, and it will create a much more complex software environment. People who jump on the bandwagon without doing their homework are opening themselves up to a lot a grief."

Chief among Langelier's concerns is the possible revenue loss from network licensing because customers would no longer have to buy a license for each node. "To recover the value we receive today, the premium we'll have to charge over node licensing will be surprisingly high," he says. Figuring out the correct premium will be very complex because each installation uses software differently.

Langelier also believes that network licensing will complicate sys-

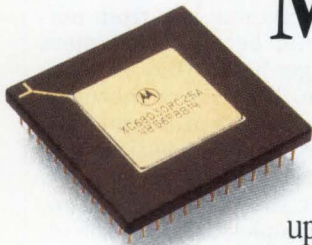
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Apollo 3000 VAX 8400, 8500	✓	✓	✓	—	—
Apollo 4000 VAX 8600	✓	✓	✓	✓	—
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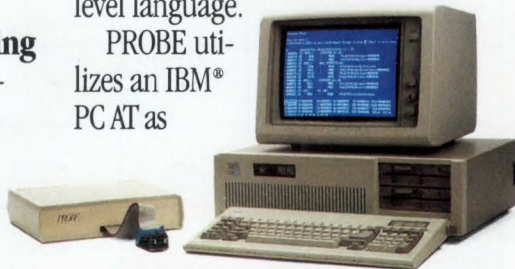
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tem administration because it will require very careful capacity planning and resource load balancing. Deciding how much software to purchase could become a complex decision. And if the node on which the licensed server is running goes down, then nobody can access keys for the applications software.

To support such applications as Mentor EDA tools, Apollo's NLS has many features designed to help CAD managers. "Network licensing will actually simplify system administration," argues Herrick Johnson, Apollo's product manager for network computing. "Users can get reports on what their software usage is, and the license server can also track revision levels of applications software. That information is hard to get today."

■ **Mentor waits, Valid moves**

Mentor is taking a wait-and-see approach by working with key customers to evaluate possible scenarios for network licensing. Valid Logic, on the other hand, has taken a more aggressive stance by introducing network licensing this spring. Since Sun doesn't yet offer a program comparable to Apollo's NLS, Valid wrote its own network licensing program, called Access.

Like Apollo's NLS, Access lets applications software be executed anywhere on the network, and Valid controls the number of concurrent users by selling license keys. Access also provides usage reports for nodes on the network. "Apollo's NLS is a little more robust because it's a general-purpose program, while Access is for Valid software only," says Dick Albright, Valid product line manager for Sun workstations.

Valid charges \$1,000 per node to install Access—but it doesn't charge a premium for software that's not locked to a CPU. That's a potentially risky approach that assumes long-term purchases will make up for short-term losses. "The initial purchase with network licensing is less, but as more people start using the software, customers will find out they haven't bought as much software as they needed," says Albright. "So in the long term, the purchase will be the same."

When Valid sells software under network licensing, it's sold in indi-

vidual pieces. Node-licensed software, in contrast, is usually sold in bundled packages that might combine such applications as schematic capture and simulation. Since bundled packages are generally a cheaper way to buy software, Valid's EDA applications essentially cost more under network licensing.

Valid is counting on network

***"There's a misconception that network licensing will make software free and system administration easier."***

—Gerry Langelier, Mentor Graphics



licensing to expand its customer base. Access has helped Valid secure several major accounts, including a recent \$1 million order from Sun Microsystems, according to Albright. About 60 to 70 percent of all new orders include Access software.

■ **CASE on the network**

Like Valid Logic, Cadre Technologies wrote its own network licensing software. Available since June, Cadre's Teamwork Project Environment (TPE) provides network licensing for such applications as structured analysis, structured design and real-time design. It's available on Apollo, Sun and VAX workstations, although unlike Apollo's NLS, it's not yet available in multivendor computing environments.

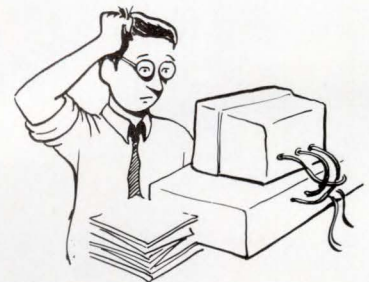
Moving to network licensing wasn't difficult for Cadre because the company's software already controls access to a project data base by multiple users. Cadre added capabilities to control the number of simultaneous users and to distribute services across a network. To assist with network management, TPE also provides reports on software usage.

Cadre's Teamwork Server is licensed to run on a specified node in the network, and it acts as a data controller (licensed server) that provides access to Teamwork applications.

Simultaneous user licenses are purchased in increments of five, and the available number depends on the server that's used. To support 25 users, for example, a VAX 8600 or 8800 or a Sun-4 workstation is required. "We won't sell you something we expect won't perform correctly," says Lou Reynolds, Cadre marketing vice-president.

Not only does Cadre avoid a premium for network licensing, but the quantity-of-five price for Teamwork is actually lower with network licensing. "That may be puzzling because TPE is more flexible," Reynolds says. "But with TPE you're restricted to single data controllers, whereas in the node-licensed scheme you could put up multiple data controllers. We can be pretty much assured that at some point your data controller will become overwhelmed, and you'll have to buy another one."

The CASE market differs from electronic CAE because CASE isn't a turnkey business, and prices per seat are much lower. In this respect, CASE vendors are less threatened by network licensing than are CAE vendors. In both CASE and CAE environments, however, it appears that user demand will make some form of network licensing inevitable. ■



**Looking for more information about CAE/CAD tools?**

Turn to the Design & Development Tools section of New Product Highlights. (It starts on page 82.)



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CIRCLE NO. 37

# High-density gate arrays tax utility, packaging and testing

*As gate array densities continue to escalate, designers combat the side effects.*

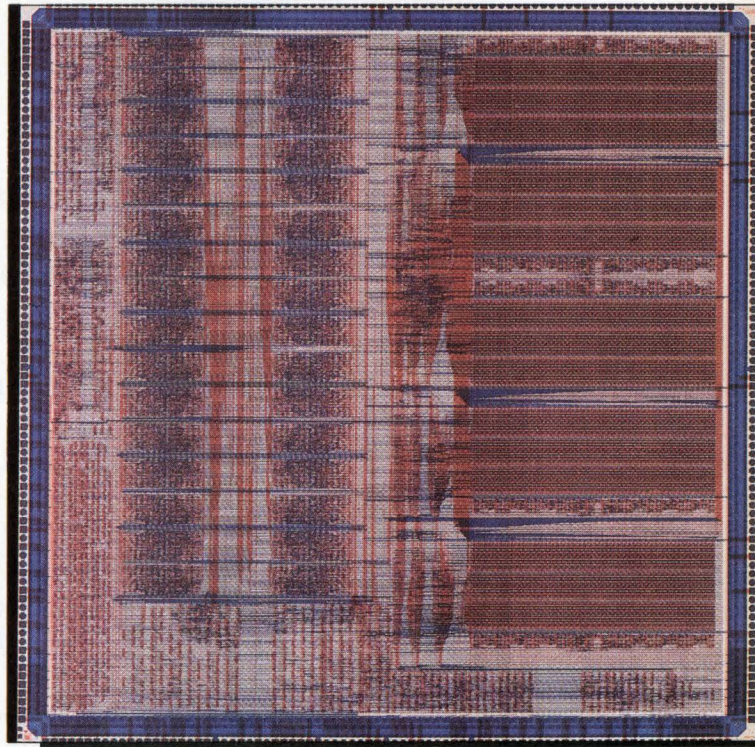
Warren Andrews  
Contributing Editor

**O**ver the past two years, gate array densities have skyrocketed to a point where more than 200,000 gates reside on a single chip. But these dramatic increases haven't come without a cost: the percentage of usable chip area has decreased, conventional packaging techniques have run out of steam, and testing has become a major problem.

Although channel widths have decreased from the 2- and 3-micron levels of a few years ago to the 1.2 to 1.5 microns of today, the largest contribution to dense gate arrays has been the development of the channelless, or sea-of-gates, approach. Early versions of channelless arrays began to surface about three years ago. They used only one or two layers of metal interconnection, which limited gate utilization to only 20 to 30 percent. Newer approaches, however, take advantage of three metal layers, as well as sophisticated routing algorithms, to greatly increase gate utilization.

Manufacturers have been clever in extending the bounds of conventional packaging techniques. But even so, packages are still a limiting factor on many designs. Pin grid arrays (PGAs) have topped out at somewhat over the 300-pin level. And, though tape automated bonding (TAB) techniques promise to bring IC lead counts close to 500 leads, mounting equipment is expensive and not, at this time, in wide use. IC makers, therefore, are scrambling to create new package designs to cope with the growing need for 300- to 500-lead devices.

Testing is also a major problem, not only as device complexity increases, but also as raw gate speed increases. The burden of testing has traditionally been on the IC vendor; however, more and more, the vendor is trying to push this burden onto the designer. Furthermore, there are few commercially available testers to test complex parts with gate delays down in the 0.5-ns area, and the prices for the few that do exist are escalating, increasing the overall cost of testing. Add to that the traditional problems associated with testing high-density application-specific ICs and the whole testing issue becomes increasingly intractable. Built-in self-test and various scan approaches



*The development of channelless arrays has permitted dramatic increases in gate array density. LSI Logic's 100K array is presently the largest commercially available, boasting a total of almost 250,000 equivalent gates with just somewhere over 100,000 usable gates.*

## ■ GATE ARRAYS

are just beginning to emerge, but they'll need help from manufacturers of both design software and commercial testers.

### ■ The density race

Today's highest density array packs close to 250,000 gates on a die with sides over ½ in. long. Coming from LSI Logic (Milpitas, CA), the channelless 100K Gate LCA10000 Compacted Array is fabricated in a 1.2-micron CMOS process that uses three layers of metal interconnection. Users should achieve somewhere between 40 and 60 percent gate utilization. "Gate utilization," says Jerry Rau, LSI's ASIC product manager, "is really more opinion than fact. It's relatively easy to define many attributes of a gate array, such as cell size, transistor length, output buffer strength, output size, the number of I/Os, pad size, the number of layers of metal and the width of the metal. But utilization is far more design-dependent."

It would be foolish to guarantee that a particular array will achieve global utilization of any given percentage—whether that be 40 percent or 90 percent or whatever, according to Rau. One has to look at a particular design before any type of utilization figures can be determined. "At LSI, we're able to trade on our experience of having done hundreds of designs at different gate-level complexities to get a good idea of what to expect," Rau says.

Rau cites a comparison of digital signal processing functions vs. more conventional CPU functions implemented on a gate array. DSP chips can have relatively high gate utilization because signals tend to start at one side of the chip and migrate to the other in an orderly way. CPUs, on the other hand, require that everything on the chip talk to everything else, resulting in far lower gate utilization. Similarly, circuits incorporating a significant amount of memory tend to have higher utilization percentages than those with more random logic.

Yet as gate array densities increase, other factors also take their toll on gate utilization. Bonding pad and package limitations are often more limiting than the number of available gates. Often designers have enough gates for more logic functions on a chip, but because the number of bonding pads is limited by the outside perimeter of the die,

there's no way to get more signals on and off a chip. Similarly, designs are constrained by the number of pins on a package.

LSI may have the densest gate array now, but it's constantly being challenged. A number of gate array vendors are offering products ranging from about 100,000 to 160,000 gates, including Motorola (Tempe, AZ), SGS-Thomson (Phoenix, AZ), VLSI Technology Inc (San Jose, CA), Mitsubishi (Sunnyvale, CA) and Toshiba (Tustin, CA). It's also likely that other manufacturers will soon jump into the fray with gate arrays with more than 100,000 gates.

***"Gate utilization is really more opinion than fact."***

—Jerry Rau, LSI Logic



Though some of these manufacturers, such as Intel (Santa Clara, CA), have been reluctant to give up channeled arrays for sea-of-gates approaches, the inherent advantages of channelless arrays will inevitably force their hand if they're to stay in the higher-density gate array arena.

VTI offers one of the densest competitors to LSI's arrays, boasting almost 180,000 equivalent gates. Developed using the company's 1.5-micron, two-level metal process, the estimated number of usable gates is only about 54,000 (about 30 percent). In designs requiring a fair amount of memory, though, this figure can easily jump to 64,000 gates

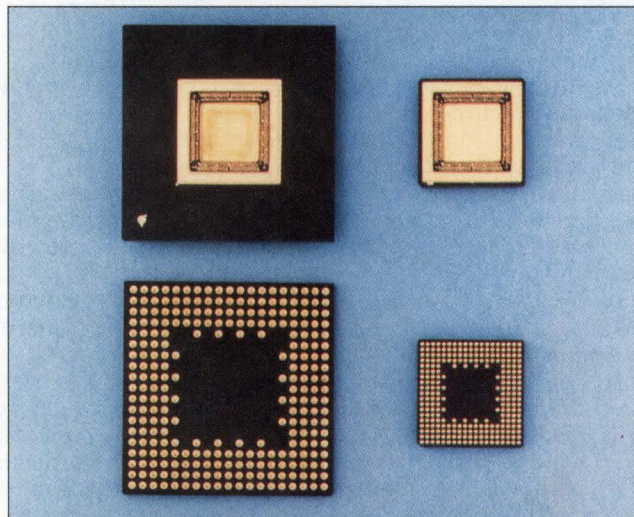
or more. Emyr Edwards, VTI's manager of ASIC distribution marketing, says the company is actively pursuing the development of a three-level metal system but would give no indication of when it would be released. While the third level of metal should increase utilization somewhat, it will also shrink line lengths, thus reducing inductive and resistive problems, Edwards notes.

While VTI's 1.5-micron figure seems relatively conservative, Edwards points out that it provides one of the shortest gate-delay times available, at about 560 ps for a two-input NAND gate with a fan-out of 2. This, he claims, lets flip-flops toggle at 250 MHz and lets system clock speeds reach around 60 MHz. In addition to a third metal layer, future VTI developments will include shrinking the die to bring minimum dimensions close to the 1-micron range.

### ■ Implementing complex designs

Motorola's entry into the market has a mere—relatively speaking, of course—104,000 equivalent gates. The device, however, can implement designs that are more complex than those implemented by many arrays with far higher base gate counts, says John Carey, product manager for the company's ASIC division. The trick, he says, is using a three-level metal interconnect scheme that lets signals, power and ground occupy any of the three metal layers. With this interconnect strategy, exploited by clever design software and an advanced routing package, the arrays routinely achieve gate utilization figures from 70 to 90 percent and higher, according to Carey.

Fujitsu Microelectronics (San Jose,



*These may look like conventional pin-grid array packages, but they're actually Fujitsu's advanced, surface-mount PGAs. Dropping pin spacing down to 50 mils (right) from the standard 100 mils (left) permits a large reduction in package size. Though this is a 256-pad device, Fujitsu has increased pad count to over 400.*

CA), meanwhile, has been involved in the sea-of-gates array business since it first developed a product in 1985, yet it still doesn't offer such a product in the United States. Its initial sea-of-gates array, according to Gary Hess, Fujitsu's director of marketing for ASIC products, was never commercialized because the company believed the two-level metal interconnect structure resulted in gate utilization too low to be practical.

Subsequently, says Hess, the company has released a 100,000-equivalent-gate sea-of-gates array in Japan. The array is fabricated in 1.2-micron CMOS and uses three metal layers to achieve gate utilization of 50 to 75 percent. The gate array is expected to be introduced in the United States later this year.

### ■ Packaging constraints

One of the constraints preventing designers from taking advantage of higher-density arrays (and cell-based parts as well) is packaging. "I/O count has gone up in direct proportion to IC density, and from all current indications, it will continue to rise," says Laurence Cooke, vice-president of engineering for Integrated CMOS Systems (Sunnyvale, CA). Despite some predictions that pin count would increase to some maximum level and then start to decline, wider address and data buses seem to have negated that effect. In many custom gate arrays, data buses have reached 64 bits or more. There's no indication that pin requirements will drop in the immediate future.

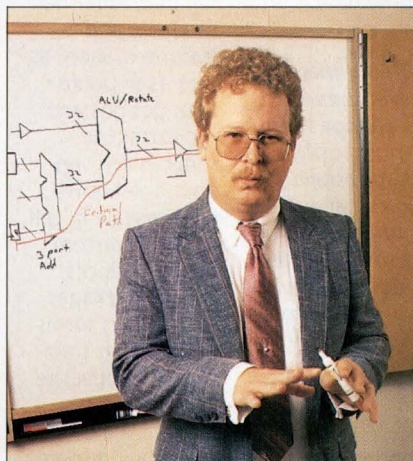
Existing packages can't keep up, however. Conventional PGA packages have topped out at somewhere just under 350 pins, and even at that, package costs start to approach—if not exceed—the cost of the chip being packaged. TAB mounting techniques may bring lead counts to 500 and perhaps higher. But TAB calls for the use of complex mounting equipment that's too expensive for many users. Chip vendors, therefore, are scrambling to find alternate packages and interconnect strategies.

Fujitsu has developed a surface-mount array package that sports just over 400 connections—one of the densest available commercially. The surface-mount connections are configured on the bottom of the package in much the same way that pins are mounted on a PGA. In use, the package is attached on a board and then soldered in place using conventional

vapor-phase reflow soldering techniques. Integrated CMOS Systems has also designed a proprietary 400-pin package using an approach that resembles a leadless chip carrier. Such packages, however, are starting to push the limits of conventional lead-frame metallurgy and wire-bonding technology.

Yet even these approaches won't be able to cope with the increasing chip densities of the next generation or two. While techniques such as TAB help reduce the size of bonding pads and increase lead density, they've already begun to reach some practical limitations.

Some vendors believe that future generations of chips will need packaging that reflects overall system- or subsystem-level thinking. Vendors such as Integrated CMOS Systems have suggested a system where multiple, high-density chips can be



*I/O count has gone up in direct proportion to IC density and will continue to rise, says Laurence Cooke, vice-president of engineering at Integrated CMOS Systems. Cooke's company is among those that believe that future generations of chips will need packaging that reflects overall system- or subsystem-level thinking.*

mounted on and connected to a larger silicon substrate. Since the coefficients of thermal expansion would be identical for the chip and substrate, mounting the chip directly to the substrate and directly interconnecting the two wouldn't present a problem. And because fine lines and interconnections could be used, bonding pad size could be reduced to the size of wire interconnections. Multiple-chip subassemblies can be interconnected using more conventional techniques in much the same way that hybrid circuits are connected.

Pad and packaging limitations

aren't the only problems caused by higher-density circuits. The other problem mentioned most often by both users and vendors is testability. Despite claims by ASIC vendors and third-party development-tool suppliers, testing issues remain something of a negotiated truce between users and vendors. The growing sophistication of automatic test vector and pattern generation are only a part of the answer. And as chips increase in complexity, they provide increasingly less of a solution.

"Customers would like to see their chips tested at full speed with 100 percent fault coverage," says Richard Koury, director of marketing of Gillytron (San Jose, CA), a manufacturer of scan testing equipment. Vendors, for their part, are seeing testing costs escalate and testing times increase while competitive pressures force them to keep prices down. Testing costs, they claim, are increasing to the point where they begin to approach the cost of the silicon itself. To make matters worse, the price of big IC testers has increased from \$500,000 to \$1 million and now is reaching close to the \$2 million mark. This places increasing capital-investment pressures on vendors.

### ■ Customer-vendor compromise

The result of these pressures is almost always a compromise between what the customer wants and what the vendor can, or is willing to, provide at a given price. Often, a negotiation takes place between the customer and vendor, settling, in some roundabout way, degrees of fault coverage and other test parameters. In many cases, fault coverage on large chips can be as low as 50 percent and often doesn't exceed 70 percent. And it's not certain that chips are tested at speed. In one case, a chip designed to run at 30 MHz was tested only at 1 MHz—unbeknownst to the user.

But the testing problems may be solvable. Mainframe computer makers have long realized the need for a comprehensive test technique at both the board and system levels. To meet the need, they developed various circuit scan techniques, the most popular of which is level-sensitive scan design (LSSD), developed by, and used first at, IBM. Other scan techniques such as boundary scan have also been used successfully by mainframe vendors. Scan circuitry places

**New generation of ASIC vendors improve in-circuit success rates**



**T**he density per chip for high-density application-specific IC chips is now exceeding 100,000 gates. And it's easy to imagine that within the next two to three years there will be chips with over 500,000 gates. At one time, we wondered what anyone would do with so many gates. But today, even with so many gates available on a single chip, high-performance systems are being designed using multichip ASIC approaches, creating even greater challenges in integration for better price/performance. Yet the current success rate of new ASIC designs when the chip is placed into the target system is probably between 20 and 50 percent. This is in spite of a first-pass success rate, after simulation, of close to 99 percent, as reported by the ASIC industry.

The two statistics differ because ASIC vendors measure the number of designs that pass all test patterns on their automatic testers, while designers are interested in in-circuit success. As long as the ASIC chip passes the test patterns provided by the customer, the ASIC vendor has achieved its objective.

In most cases, the reasons for initial in-circuit failure of new ASIC chips can be traced to design problems that are hidden during simulation and test. Since traditional ASIC vendors concentrate on automating the silicon layout and fabrication process, the verification burden remains on the system designer.

■ **Vendors help shoulder burden**

Fortunately, a new generation of ASIC vendor is emerging to shoulder some of this burden for multichip ASIC systems. These vendors come from either of two categories. First are those whose ASICs support high-volume industry standards. Second are those vendors specializing in customer-specific applications, such as the new Apollo chip set produced by Integrated CMOS Systems (Sunnyvale, CA).

In both cases, the new ASIC vendors assume more responsibility for successful in-circuit operation and apply expert knowledge of the application

and the technology to ensure that proper solutions are created. With application-specific knowledge, the new-generation vendor can assure in-circuit use through proper signal protocols and timing relationships, appropriate partitioning, selective integration and total system simulation. Highly specialized design automation tools support high levels of designer productivity. And design-specific test methodologies provide verification and debug facilities that address a majority of common ASIC design problems.

The new-generation ASIC vendor offers application-specific knowledge in many different forms. For vendors supporting industry standards, the know-how is embodied in off-the-shelf products and documentation, as well as in board-level designs and products. For semicustom vendors, the know-how may lie in cell libraries, custom building blocks, unique packages and various forms of customer training. A prospective customer can recognize either

**Traditional ASIC vendors must change their philosophy on responsibility for in-circuit success and testing to provide system designers with complete solutions.**



vendor by the attitude of their applications engineers, who focus on solving system problems rather than on selling gate speed and density.

New-generation ASIC vendors develop specialized design automation tools for solving system design problems. Based on years of internal development combined with the best industry offerings of electronic design automation tools, these tool suites provide high levels of designer productivity by simplifying complex tasks and automating the mundane. Logic synthesis, for example, can simplify the task of converting a high-level system description to a detailed gate-level implementation. And if automatic chip-partitioning tools are available, most of the decisions about which gates go in which chips can be automated as well. In addition, tools for card-level

timing analysis, network load balancing, clock skew control and I/O pin assignment improve accuracy and turnaround time.

The major contribution frequently comes from system simulation tools. While many simulators have system simulation capabilities, few designs are completely simulated at the system level because of modeling, cost and scheduling problems. New-generation ASIC vendors focus on system simulation to improve in-circuit success rates. By customizing the design methodology to the project, simulation can be either fast or slow, inexpensive or expensive, exhaustive or superficial, and effective or useless. For high-gate-count systems, experience shows that a synchronous, race-free and hazard-free design methodology delivers the best results. Asynchronous events can be synchronized to the system clock scheme on occurrence, and testability concerns can be managed automatically.

■ **Uncompromising performance**

Traditionally, testability was secondary to performance in system design. If additional circuits were needed to support criteria for observability or controllability, the usual practice was to delete test features. At densities of 10,000 gates, these priorities begin to shift, but no designer wants to sacrifice performance.

New-generation vendors provide test structures offering the same performance as untested logic, and the circuit overhead is minimal. For example, in the new Apollo series 10000 Personal Supercomputer, high performance is delivered while maintaining complete chip- and card-level level-sensitive scan design (LSSD) discipline.

All of the disciplines and tools necessary to improve in-circuit success rates can be found in the industry today. But traditional ASIC vendors must change their philosophy on responsibility for in-circuit success and testing to provide system designers with complete solutions. New-generation ASIC vendors prove that an integrated chip set approach can deliver higher performance, lower costs and confidence in first-pass success.

**Tom Miller, Vice-President, Sales and Marketing, Integrated CMOS Systems**



discrete registers at each node in a circuit, which can be read serially to provide information regarding the status of the node.

Although ASIC vendors and designers are familiar with these techniques and realize they can be applied to both chip- and board-level problems, the techniques haven't been widely used for three reasons: scan cells eat up a fair amount of silicon area, the cells must be designed into a circuit manually, and commercial scan testers haven't been readily available.

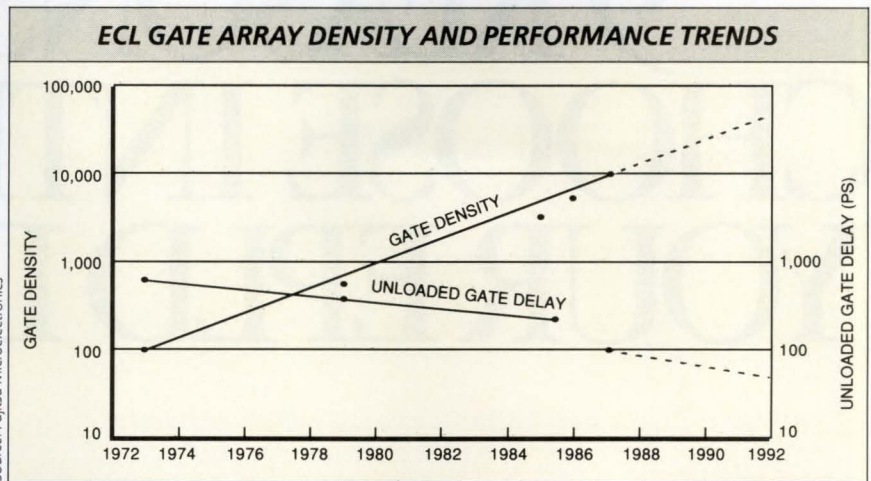
Depending on how scan testing is implemented—and on whom you talk to—the cells required for scan testing add between 10 and 30 percent additional silicon. Frequent users of scan techniques repeatedly mention figures of 15 to 20 percent. According to ASIC vendors, customers are too parsimonious to spare the additional silicon area for testing functions. They're reluctant to pay for something that they expect to get from the vendor for nothing.

Another missing ingredient for the broader use of scan technology is software that will automatically insert scan cells as part of a design being assembled. "If there were little or no penalty in design time, users would be more willing to use scan technology," comments one user. The combined penalties of additional design time and additional silicon area intimidate and frighten off many potential users.

Even though all the issues such as pad limitations, packaging and testing aren't fully resolved, ASIC vendors are forging ahead with even denser arrays. LSI's Rau says there's nothing standing in the way of increasing complexities to 500,000 and even 1 million equivalent gates in the near future, although he would not divulge any LSI plans.

### ■ BiMOS forging ahead

While CMOS arrays seem to get the lion's share of attention, bipolar ECL and BiMOS arrays continue to forge new territory. Although power dissipation has kept densities of bipolar ECL and BiMOS arrays in the 10,000-equivalent-gate area, significantly higher densities are achievable and will be surfacing soon. Recent developments in ECL processing have already resulted in major power reductions without sacrificing speed, and developments within the next year are expected to see equivalent



Although bipolar ECL arrays haven't garnered the headlines the way CMOS arrays have, increases in density and drops in gate delays will soon be pushing them near CMOS array densities with far superior performance. The break in the performance reflects the change from metal contact emitters to polysilicon emitters.

gate counts reach the 50,000 level.

And that's only the short-term future. Fundamental characteristics of CMOS transistors prevent them from being scaled equally in both directions (channel width and length). CMOS devices, therefore, will reach a fundamental limit in scaling. Bipolar transistors, on the other hand, have no such restriction and can relatively easily be scaled well beyond CMOS limits. So it's possible, and probable, that bipolar devices will overtake CMOS in density within the next few years.

### ■ System considerations

While gate arrays continue to grow in complexity and design tools make them easier to assemble, there's still no free lunch, says LSI's Rau. Users, though, can follow the example of LSI, which has taken advantage of the knowledge learned at the lower-density arrays. Rau doesn't recommend trying a first gate array design at the 100,000-gate level (although he claims it can be done). "Most of our customers going into very high density gate arrays already have experience designing chips and implementing them in a system at a lower complexity level," he says.

Furthermore, the issue of making an ASIC work in a system is often overlooked, usually leading to catastrophic results. It's been reported that while better than 90 percent of all ASICs work according to initial specification on first pass, almost one-half of them fail to operate in the systems for which they're designed. Reasons for the failure vary, from

leaving out a component or two in the design to more involved timing problems not taken into consideration as part of the system design.

Much more emphasis, therefore, is being placed on overall system design, rather than simply on chip design. If there was an underlying catch phrase at the recent Design Automation Conference, it was "systems approach." The new interest has resulted in an increasing emphasis on accurate models and simulation tools capable of looking at entire systems, rather than at chips in isolation. ■

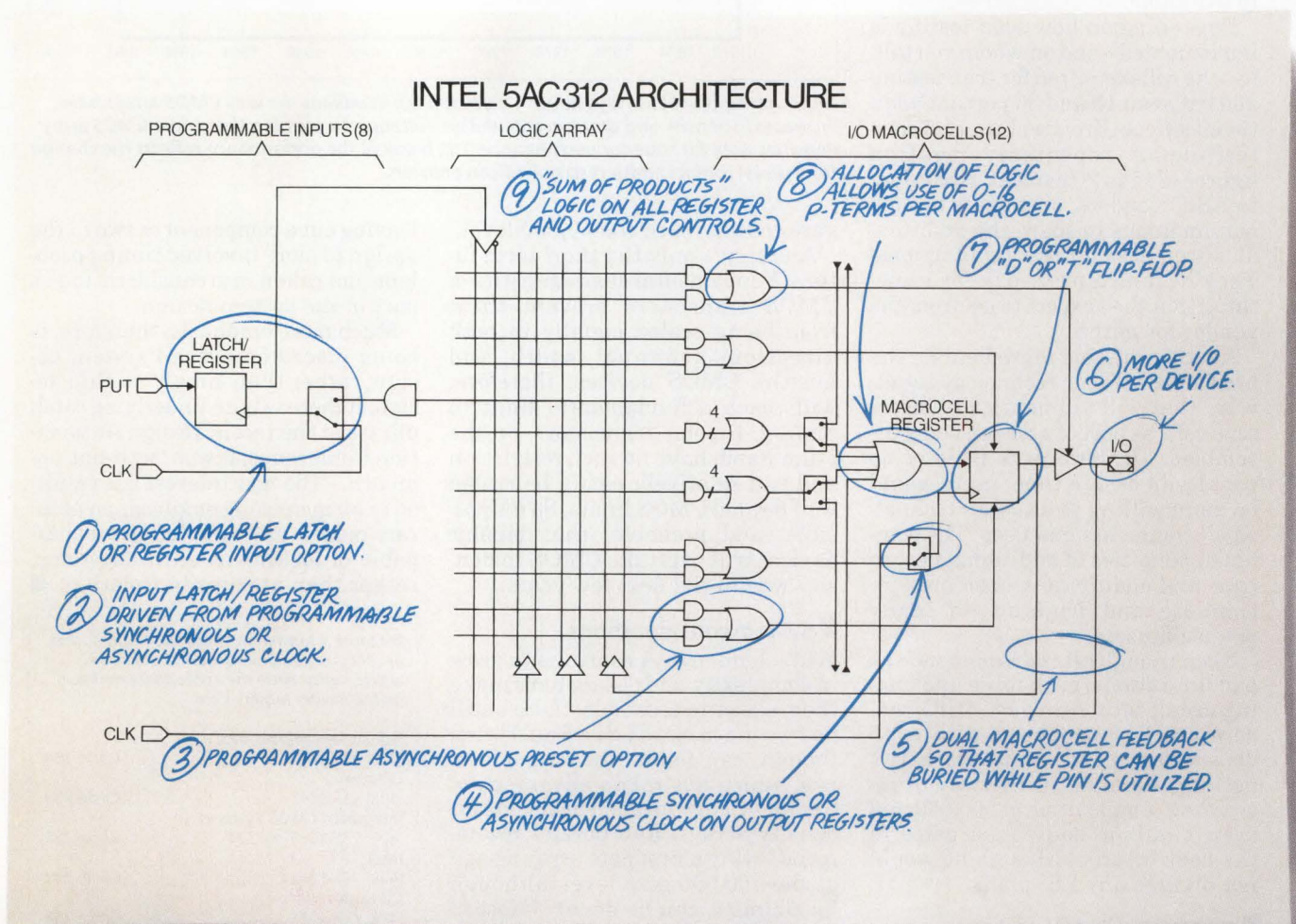
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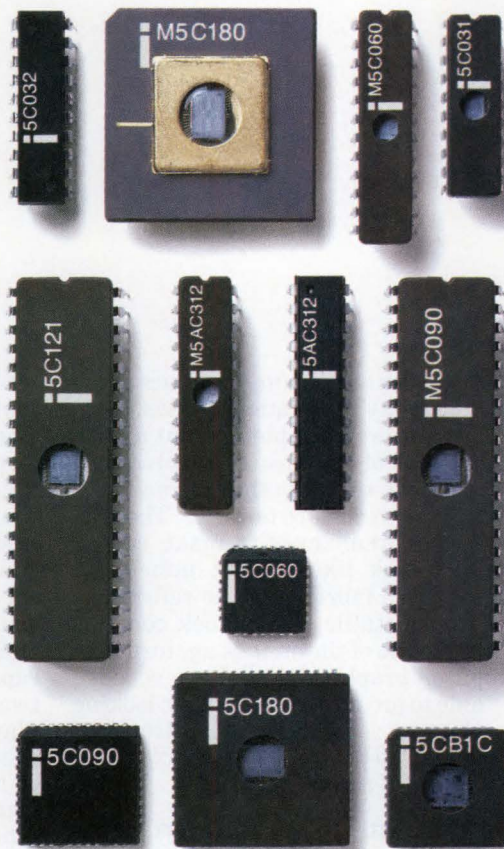
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# Graphics system designers strive for photorealism

Tom Williams, Western Managing Editor

*The challenge? Design a graphics system that displays photorealistic images—without costing too much in dollars, interactivity or speed.*

**R**ealism in computer graphics displays? Who needs it? As it turns out, photorealistic computer graphics, or the ability to generate computer images that rival color photography in all its nuances of color, shading, reflectance and translucency, is in demand by a growing number of users. Among these are architects, artists, industrial designers and mechanical engineers who need to see precisely what their final products—whether buildings or automobiles—will look like under real-world conditions. Such photorealistic graphics displays are technically within the grasp of computer-system designers, but at a stiff cost to the user in terms of both computation time and system price.

As if the demands for realism weren't enough to task the creativity of computer-system designers, there's also a growing user demand for interactivity. An industrial designer working out a new packaging idea, for example, would like to instantaneously see the results of any changes made, and from different angles. Such interactivity also is technically within reach, but again, at a stiff cost to the user in terms of price.

What distinguishes photorealistic images from the most sophisticated

examples of computer graphics available today? This question has yet to be answered completely, but a critical part of the answer involves the ability to re-create the interaction of light with surface textures. The goal of photorealism is to make rubber tires look like rubber, upholstery look like fabric, and the reflections from metallic objects look convincing. "One of the strikes against computer graphics is that we've been able to produce a lot of plastic-looking objects," says Tom Porter, director of advanced technologies at Pixar (San Rafael, CA).

## ■ Interactivity just as important

To many vendors of graphics systems, however, photorealism is a "nonproblem," at least for 85 to 90 percent of their potential customers. And to some vendors, interactivity is more important than photorealism. "If it doesn't move, it ain't 3-D," says Jim Clark, chairman of Silicon Graphics (Mountain View, CA), underscoring his belief that the concept of realism is tightly bound to that of interactivity. But whatever the level of realism and interactivity, everyone seems to want the two combined for an average workstation cost of somewhere around \$50,000.

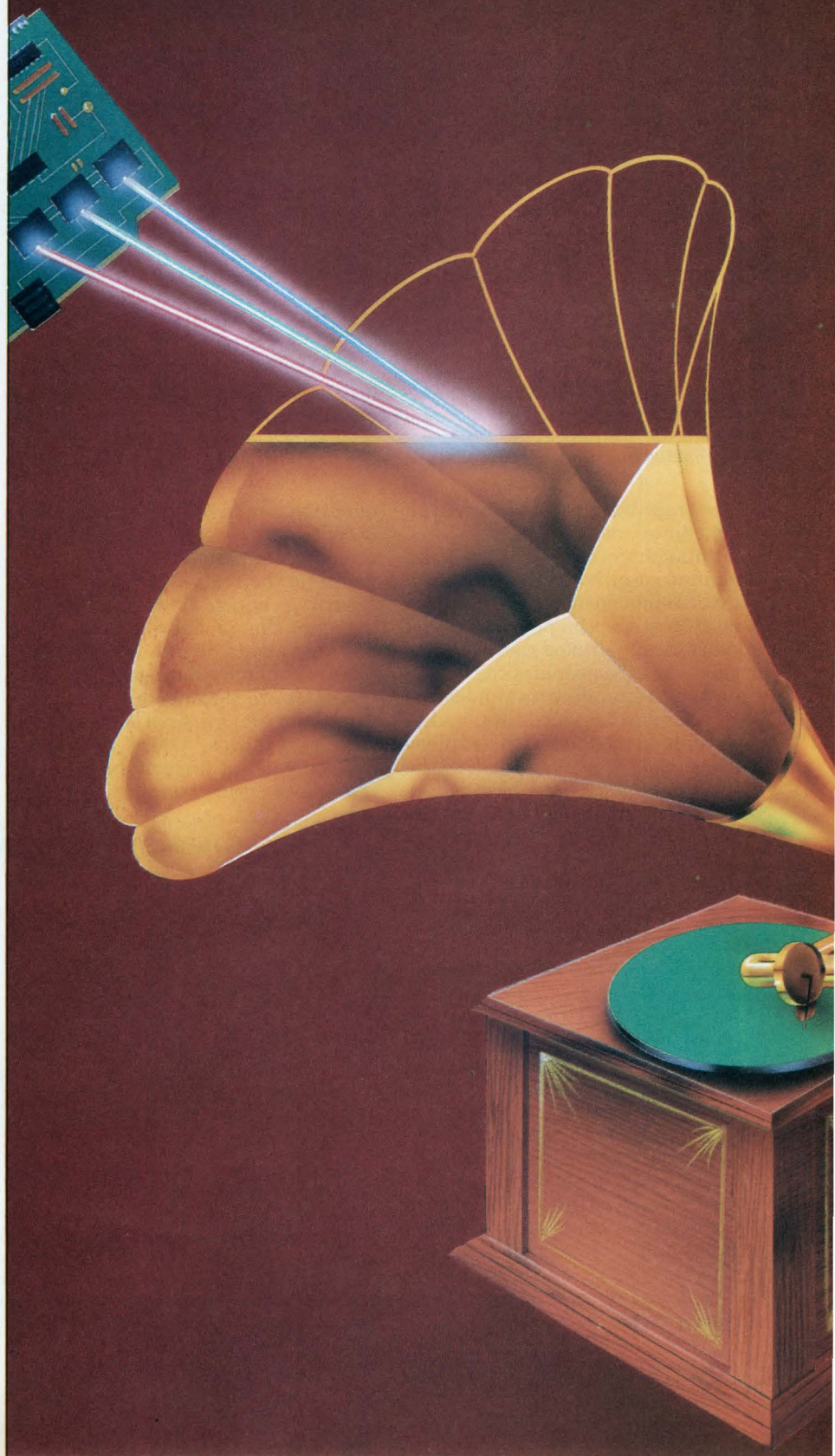
While no vendor has accomplished that yet, Clark has a list of desirable elements of realistic rendering that he predicts will be possible on an interactive workstation within five years. These include transparency modeling, texture mapping and Boolean solids display, which is the logical addition or subtraction of simple solid shapes to form more complex ones. In the near future, we'll see capabilities that lie somewhere between present-day interactive displays and full interactive photorealism. For Michael Holmes, manager of the CAD/CAM design office for Chrysler (Highland Park, MI), and others like him, the time and cost savings could be dramatic. "We're still going to build models," says Holmes, "but we hope that we'll be able to look at a lot more alternative designs and refine those designs before we commit to a full-size model."

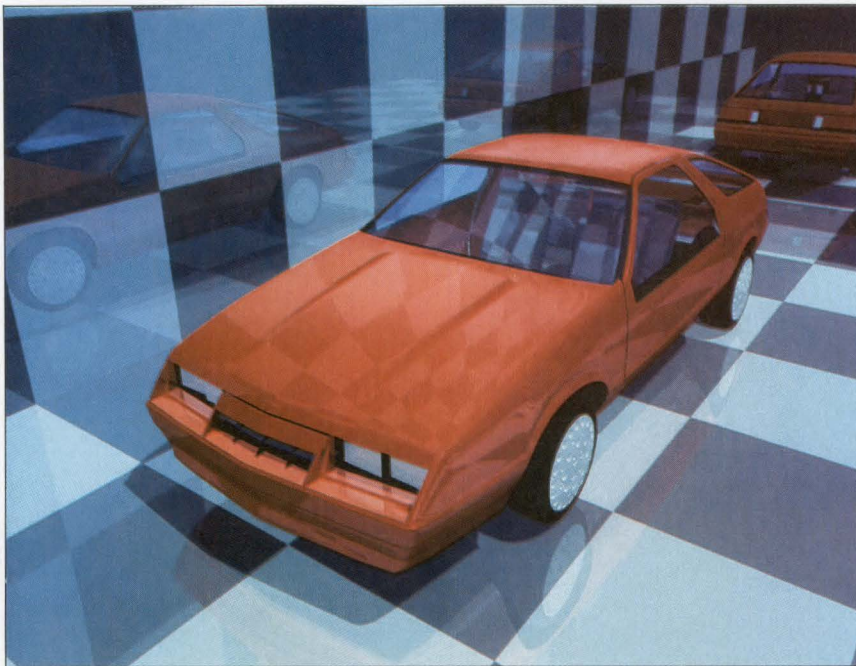
One major issue in the development of CAE/CAD/CAM workstations for mechanical design is the link between the mathematical model of an object in the computer's data base and the way the object is "rendered" as pixels displayed on a screen. At one time, computers had to keep two types of models for display: the physical design represented by a mathe-

*AT&T's pixel machine (portrayed here in a greatly simplified way) is an example of the new hardware being developed to provide graphics rendering that approaches the realism of fine color photography. Cover by Sergio Roffo.*

mathematical model and a separate set of polygons derived from that model that approximated its shape. Now, an object can be described as a mathematical model that defines its surfaces in terms of polynomial equations. A selected view of that surface description is then used to directly produce polygons and pixels on the fly to render the displayed image.

The mathematical model of a physical object is thus becoming more tightly coupled with its graphics representation. More and more, graphics system designers are turning to nonuniform rational B-splines (NURBS) to model objects—or more correctly, the surfaces of objects. NURBS are a class of polynomials used to describe curved surfaces. As so often happens, however, NURBS has become a generic term for an entire class of mathematical functions, including quadratic and bicubic patches. The major advantage of NURBS is that the same mathematical model used to render the image of a surface can also be used to directly generate the numeric machine codes for manufacturing. NURBS also provide an option for handling a model via a display list (the separate stored set of commands derived from the physical model and stored for use





*This fully ray-traced rendering of a Chrysler Laser was done on a Hewlett-Packard Turbo SRX system using Starbase. Note that despite the realistic reflectivity and shadows in the scene, the tires have a plastic-like surface because their texture hasn't been differentiated from that of the car body.*

by the graphics subsystem) or via an "immediate" mode.

In immediate mode, the graphics commands used by the display hardware are embedded in the same data used to describe the physical model and are closely linked to it. They're extracted by the graphics subsystem from the design data to render the display. Immediate mode also makes it possible to interact with the physical design data by manipulating the displayed image. If an object is represented by a display list, on the other hand, the display list must first be edited to change the displayed image. Then some separate action must be taken to update the data describing the object being modeled.

■ **NURBS lead to shading models**

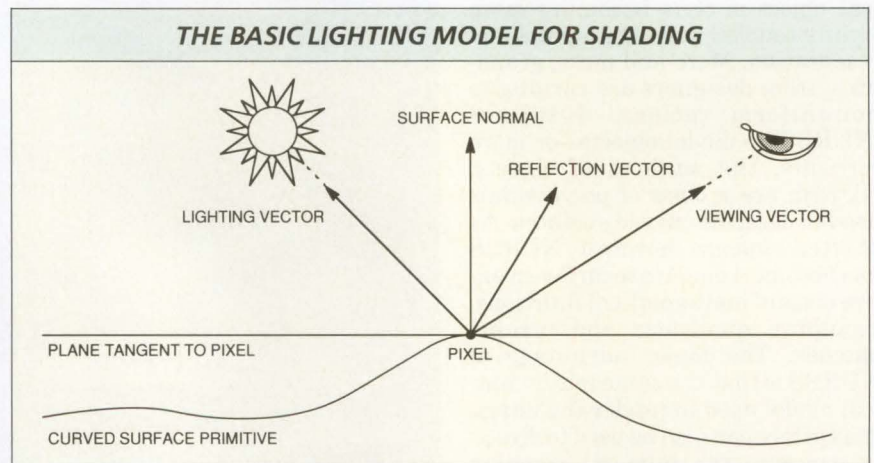
The use of NURBS to represent surfaces has provided a basis on which software developers can build lighting and shading models for rendering displays at different levels of realism. These curved-surface descriptions lend themselves to rendering techniques ranging from flat shading to Gouraud and Phong on through the more esoteric surface and texture techniques now being proposed, such as bump and environment mapping.

Since all pixels must ultimately end up at an integer address, curved surface patches described by linear

equations must be approximated in order to be displayed. This is done by breaking the patches down into polygons and then into triangles. A flatter curve requires fewer and larger polygons than a sharper curve does for the same degree of realism. Values for individual pixels inside triangles are obtained by interpolation. Triangles are used because, unlike rectangles, there are well defined ways of linearly interpolating values across triangles.

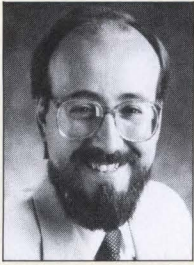
All three types of shading—flat, Gouraud and Phong—are based on how light is reflected from a source or sources off the surface to the eye of the viewer (see "Surface shading creates visual realism," on opposite page). They differ essentially in how finely this reflection model is calculated. Since surfaces are mathematically continuous curves, they have to be represented by discrete pixels on the screen. Thus, vectors calculated for points on surfaces must be associated with individual pixels for rendering calculations. An important value associated with pixels representing curved surfaces is the surface normal, a vector perpendicular to the plane that's tangent to the surface at a given pixel location.

The surface normal is used as a reference vector in the lighting equation to determine the angles of incidence and reflection for light that reaches the eye of the viewer. In flat shading, all normals in a given triangle have the same orientation; in Gouraud shading, pixel intensity is interpolated across the triangle from the vertices; and in Phong shading, the orientation of each normal is interpolated between the orientation of the normals at the triangle's vertices. Of the three shading methods, Phong is the most compute-intensive because it also performs a full lighting calculation for each pixel using the interpolated value of that pixel's normal. The advantage of Phong shading is that it can show specular highlights, or points of very high reflectivity where the greatest amount of reflected light reaches the



*In the basic lighting model from which Phong shading and more complex techniques are derived, the surface normal is the reference vector from which the amount of light traveling along the viewing vector is calculated. By mathematically perturbing the surface normal or groups of normals, texture procedures can cause different amounts of light to reach the eye, resulting in different surface texture effects.*

## Surface shading creates visual realism



**G**enerating a realistic image from a three-dimensional object model is a pipeline process made up of three basic components: transformation and clipping, scan conversion, and shading. Typically, a 3-D object is first constructed as a 3-D wireframe model with line segments or polygon definitions. Transformations and clipping are common to these line segments, but for a shaded display on a raster system, polygons must be clipped rather than lines. Scan conversion is the mapping of the 3-D line definitions of objects into discrete raster-scan lines on the image plane. Hidden-line and hidden-surface removal is a complex algorithm that's applied to the scan-line process for removal of lines or surfaces obscured by other lines or surfaces. And shading, the calculation of light intensity at each point on an object's visible surface, provides the effect of visual realism in computer-generated images.

Once visible surfaces have undergone hidden-surface removal, a surface shading/lighting model is used to compute the intensities and colors of each surface. The lighting model determines the intensity of the reflected light that reaches the eye from a point on the object. To make this determination, the lighting model applies two principal ingredients: properties of the surface and properties

of the illumination falling on it. The principal surface properties are color, reflectance and transparency. Illumination may be either diffuse, point-source or highlighted. This lighting computation is performed scan line by scan line as the hidden-surface algorithm determines which portion of a polygon face is visible.

### ■ Three approaches to shading

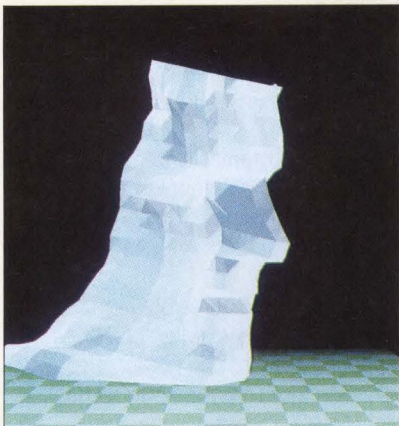
Three principal approaches to shading are flat (also called facet), Gouraud and Phong. Flat shading calculates a single intensity value for shading an entire polygon face. A single surface-normal vector is defined for each represented polygon. Each polygon is also shaded with a single color. This is a reasonable approach to shading flat surfaces where the intensity of the light reflected from the surface is held constant over the entire surface.

Gouraud, or intensity-interpolation shading, provides smooth shading through a linear interpolation technique in which surface-normal vectors are computed at the vertices or corners of each face of a polyhedron. First, surface normals are calculated. Next, vertex normals are computed by averaging the surface normals of all the polygon faces common to the vertex. Each of these vertex normals is used to compute a vertex shade, and then the shade inside the particular polygon face is interpolated from the vertex shades. Each polygon is shaded along each edge and then between edges

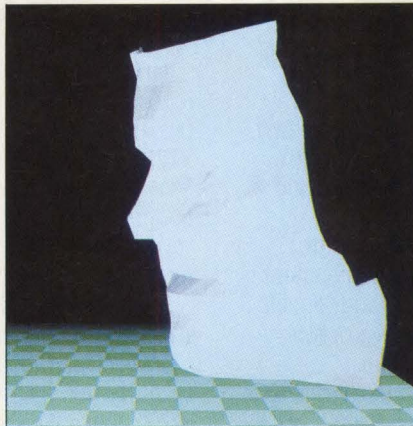
along each scan line.

Phong shading is a complex algorithm that computes the intensity value of each pixel of a polygon face according to how that point is oriented to the light source(s). Phong was the first shading model to achieve realistic highlights using interpolation of surface normals and an approximation of specular reflection. The Phong shading method entails interpolating surface-normal vectors across the polygon face—as opposed to Gouraud shading—and using the interpolated surface normals to calculate the intensity values for each pixel on the polygon surface. The intensity contribution for each light is modeled as the sum of diffuse and specular components. Diffuse reflection, or light that is reflected uniformly in all directions, depends on the position of the light source, not of the viewer. Specular reflection, which makes the surface appear shiny by generating highlights in the mirror direction, takes into account both the surface finish and the position of the viewer.

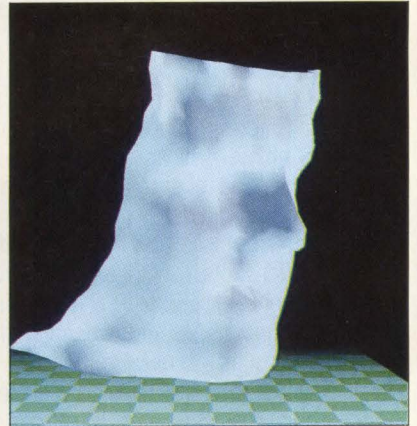
Since the Phong technique requires extensive computing power to execute the complex calculations needed to shade each pixel of an object's surface, it's usually performed only on supercomputers or superminicomputers. Phong shading, unlike Gouraud, also supports the full range of lighting controls, including multiple light sources, colored light sources, and point, spot and directional light sources.



Flat shading

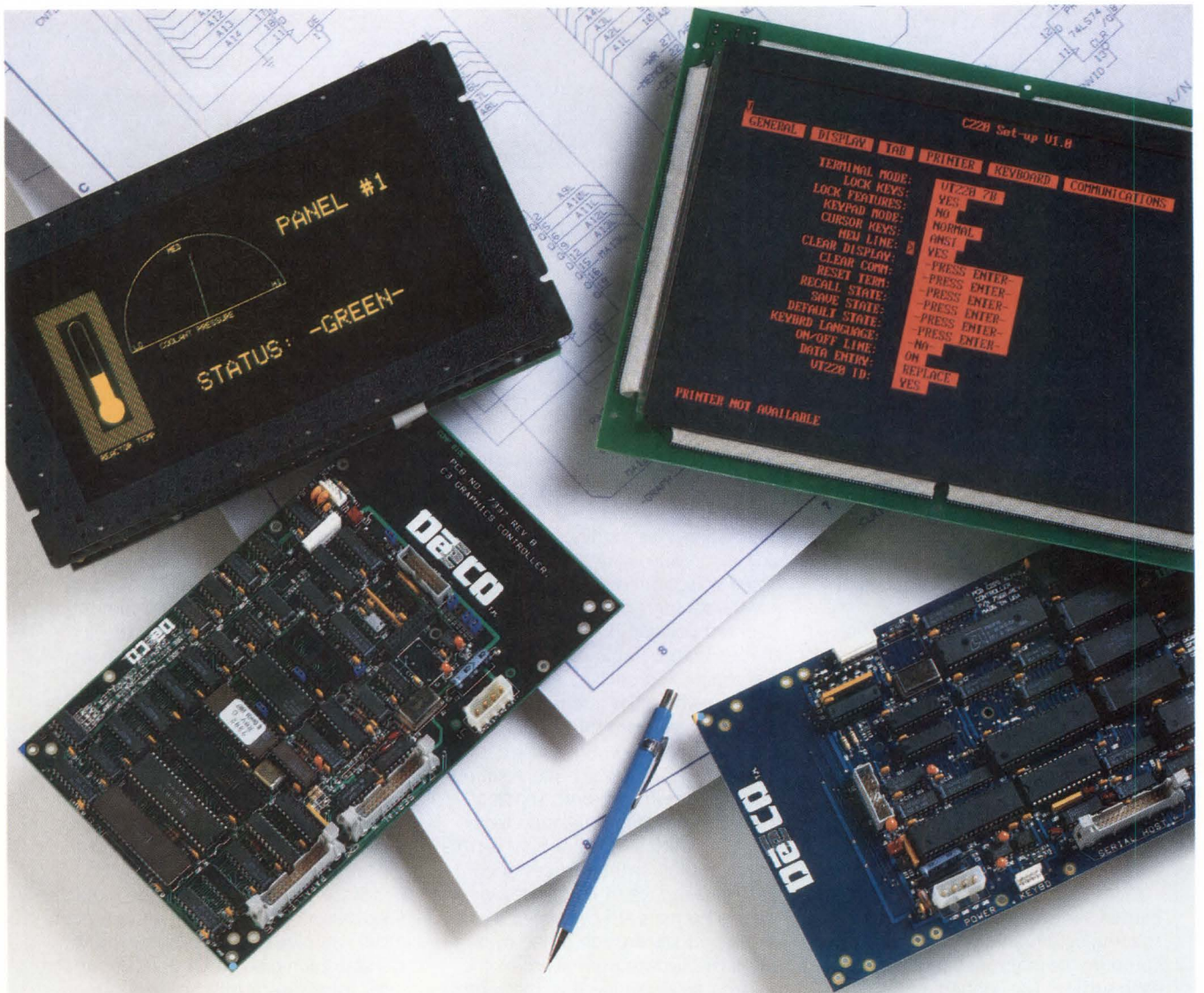


Gouraud shading



Phong shading

Michael Warner, Senior Product Manager, Seiko Instruments



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eye of the viewer.

Workstations are now getting pretty good at performing Gouraud shading in almost real time. The GX4000 from Raster Technologies (Westford, MA), for example, uses a graphics arithmetic processor (GAP) that can generate 18,000 Gouraud-shaded polygons/s. Up to eight GAPs can be plugged into a system to achieve nearly linear increases in throughput. A system with four GAPs using double frame buffers is fast enough to display and interactively manipulate some fairly complex shapes, such as a teapot, with Gouraud shading. Complexity depends not only on the number of objects on the scene, but also on how finely or coarsely the object is to be rendered. The same curved surface patch could be rendered as 100 or 1,000 polygons, for example. The 1,000-polygon patch would appear smoother, but it would take longer to render.

Another system that performs Gouraud shading in almost real time is the Model 835 Turbo SRX from Hewlett-Packard (Palo Alto, CA), which can display 35,000 triangles/s with a single light source. Hewlett-Packard has implemented NURBS primitives in hardware for defining and manipulating surfaces. There's also hardware support for trimming of B-spline surfaces. Trimmed surfaces have edges that aren't joined to other surfaces—for example, a curved

piece of paper with a hole in it. They can be used in operations that combine surface primitives to form more complex shapes.

■ **Multiband shading engine**

Designers at Seiko Information Devices and Systems Division (Tokyo, Japan) recently implemented Phong shading in hardware, making it possible to interactively manipulate Phong-shaded images using

**"If it doesn't move,  
it ain't 3-D."**

—Jim Clark, Silicon Graphics



multiple light sources. Built around a chip called the pixel rendering engine (PRE), the multiple-board shading engine used in Seiko's GR4400 series of raster display systems can calculate the Phong lighting equation for every pixel for up to eight colored light sources. The chips let users select flat, Gouraud or Phong shading depending on the degree of realism and interactivity desired.

The current version of the shading engine uses two identical PREs, which can be used in one of two modes. One PRE is used in a mode to determine the X, Y and Z coordi-

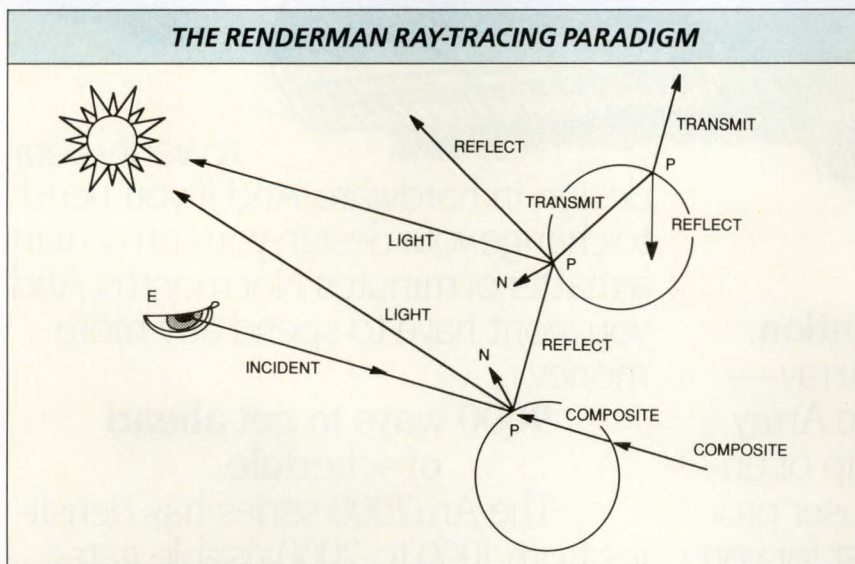
nates. Since these coordinates represent points on a curved surface, the chip can determine the orientation of the surface normals of these points. Since the position of the points on the Z axis has been determined, the Z value can be used for hidden-surface removal. The other PRE can be used in a mode that calculates red, green and blue intensity values using the shading algorithms. The current version of the shading engine calculates 60,000 Phong-shaded pixels/s. PREs can be ganged in parallel to build larger, faster shading hardware, and several pairs of PREs can be assigned to process data contained in different parts of the frame buffer.

Calculating 60,000 pixels/s is fast. Yet it would take about 16 s to render all the pixels in a complete million-pixel display. But since an object rarely fills the whole screen, it's seldom necessary to render all the pixels on the screen. Another way processing time can be slowed is by adding more light sources. Any rendering time increased in this way can be cut in half through the use of double buffering. While a user still can't manipulate an object of arbitrary complexity in real time, the shading engine provides the ability to first rapidly manipulate a complex object in near-real time using a lower level of detail and then get a Phong-shaded rendering in a matter of seconds.

■ **The search for standards**

The history of graphics standards has been one of committees trying to catch up with developments in technology—a generally frustrating experience. Now Pixar has independently published a proposal, called Renderman, that defines the way to interface with rendering systems. Renderman concentrates more on describing the way to display a view of the geometric model rather than on explaining how to manipulate the model itself. That is, it will accept an object defined as NURBS; rotate, scale and clip it; and tell the rendering hardware and software how to display it as shaded pixels. At least 10 times as much computation is involved in shading or rendering than is involved in geometric operations such as rotation and translation, according to Pixar's Porter. The more detail desired, the greater that difference becomes. Although Renderman defines these operations, its primary focus is shading.

Renderman is unusual as a stan-

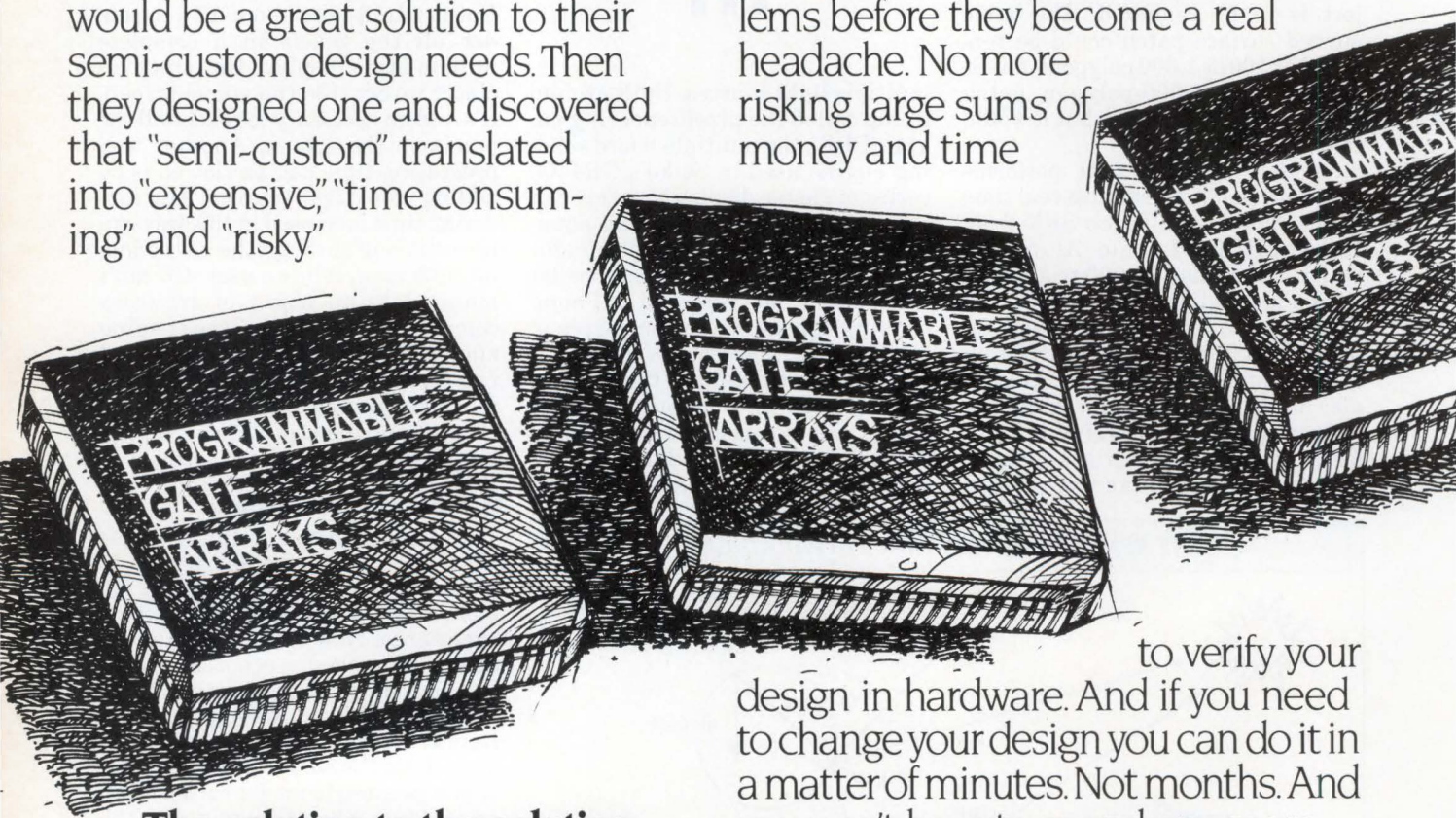


The Renderman interface proposed by Pixar uses a ray-tracing paradigm in which there are three basic types of shaders. These include the light source (sun); the texture, represented by the surfaces of the objects that reflect light; and the volume, represented both by the objects through which light passes and by the volume of the atmosphere surrounding the whole scene. The user need not use all elements of the ray-tracing paradigm for every rendering.

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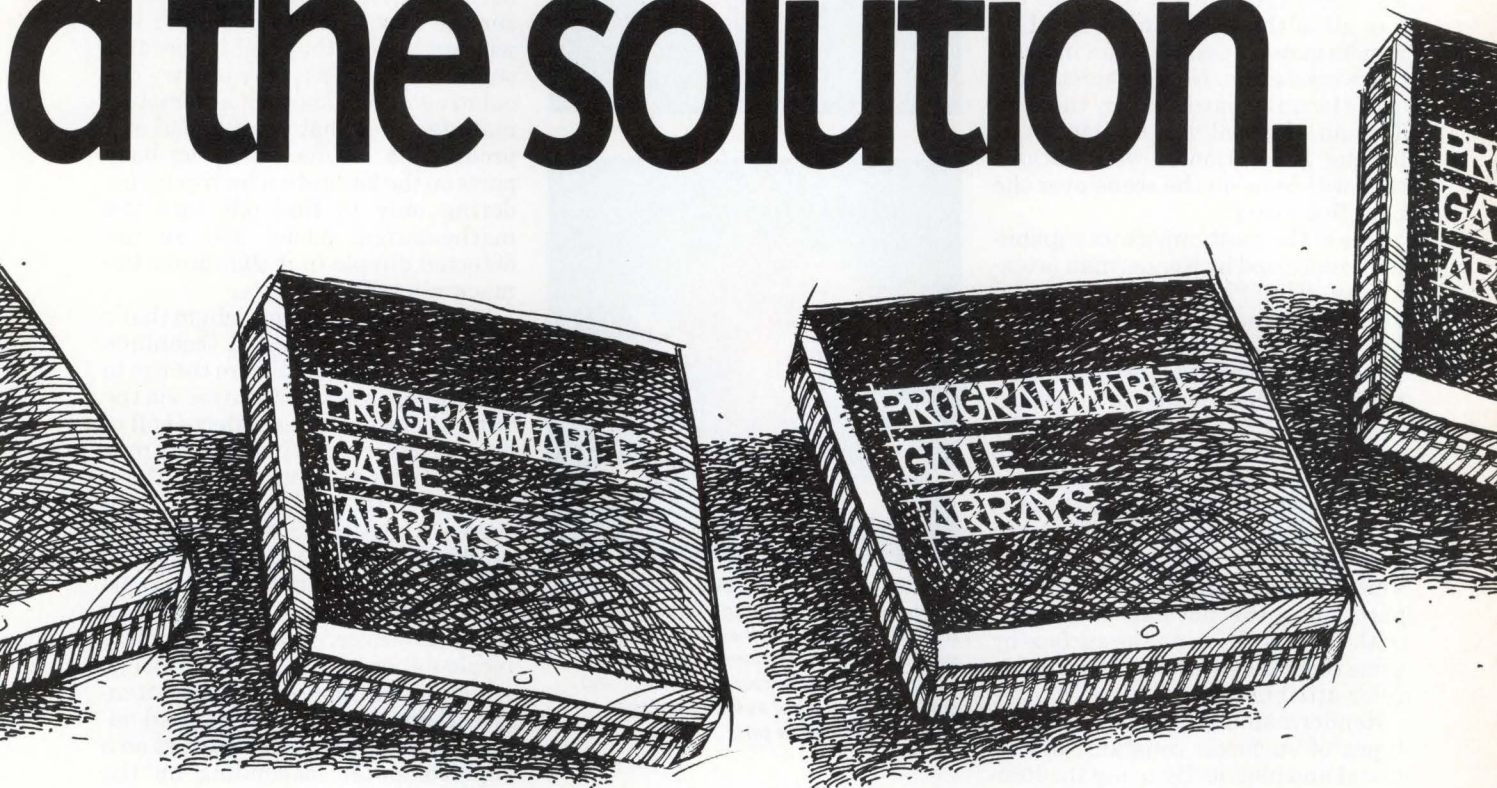
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## ■ GRAPHICS SYSTEMS

dard proposal because it specifies graphics rendering techniques that "go beyond what we know how to do and far beyond what other people know how to do," says Porter, one of its creators. Pixar's designers were concerned with graphics 10 years into the future, according to Porter. Ten years is just what Silicon Graphics' Clark estimates it will take before all of the rendering defined by Renderman is possible on an interactive workstation. Nevertheless, some of the techniques covered by the Renderman proposal will be important for the generation of workstations that will come on the scene over the next five years.

One of the most important capabilities addressed by Renderman is texturing. The Phong-shading model yields a surface with a specific normal associated with it that's based solely on the curvature of the surface, which is what leads to a shiny, plastic-like look. "Now you have the opportunity to perturb that surface normal and end up with bumpy surfaces, brushed copper, striated and so forth," says Porter. A surface with grooves, for example, might be represented by selecting rows of pixels and perturbing the normals associated with their position on the surface by some constant value and then adding color attributes.

Renderman defines four standard types of surfaces: constant, matte, metal and plastic. By using the Renderman shading language and specifying how normals are to be perturbed, a programmer may use a software procedure to define most kinds of surface textures—hence the name procedural texture mapping.

### ■ Shades define lighting

Procedural definitions of textures and other elements such as light sources, volumes and atmospheres are collectively called "shaders." There are, for example, predefined lighting shaders for ambient, distant and point light sources, as well as for spot lights. Atmosphere shaders include depth cue and fog. Volume shaders describe other volumes through which light passes and is refracted and attenuated. Atmosphere shaders are based on the fact that light is attenuated over distance, be it through clear or foggy air, and that such attenuation gives the eye a cue to spatial relationships. The syntax of these predefined shaders can be used to define custom shaders



*Two views of the same teapot: one with a Phong-shaded rendering of its surface (top) and one on another shiny surface with ray tracing (bottom). Note that ray tracing shows reflections of the pot and surface in the other as well as of the shadow cast by the pot.*

of all kinds. Such shaders are software routines that state how light is to be reflected, transmitted, attenuated or colored.

In addition to procedural texture mapping, the Renderman interface also allows images scanned in from the real world to be mapped onto geometric surfaces. Thus, a selected surface could be made to appear as wood grain or marble by applying a real-world image to a geometrically defined curved surface via software-mapping routines. This mapping would apply a pattern to the surface, but the light reflecting off the surface would still be affected only by the surface-normal values. A variation of this method of texture mapping is environment mapping, which gives the impression of reflectivity by taking a portion of the surrounding scene and mapping it onto the surface of a shiny object while modifying its brightness and color. This approach is much less costly in terms of computation overhead than ray tracing, but doesn't

yield the same degree of realism and accuracy.

"Reflectivity is important to industrial designers because it gives them a feel for the curvature of the body," says Porter. Chrysler's Michael Holmes agrees: "If you have a highly specular surface and you put a reflection line on it, you can see small abnormalities in your mathematical surface base that you couldn't see without having that highly specular surface." There's a horror story circulating about another automobile manufacturer that went ahead and produced a die for stamping body parts on the basis of a wire-frame rendering only to find out that the mathematical model had an undetected dimple in it that drove the machining of the die.

Renderman uses a paradigm that's based on ray tracing, a technique that traces light back from the eye to its ultimate source or sources via the various objects it has reflected off of or passed through. Thus, one ray may spawn two rays, and each of those two more, and so forth. The advantage of a ray-traced image is that it produces very sharp reflections as well as transmittance and translucency effects. Each new view of an object, however, requires a complete recalculation of the ray-traced image, which is extremely compute-intensive. Computing a full ray-traced image can take hours or even days on a supercomputer, depending on the scene's complexity.

### ■ Radiosity vs. ray tracing

Another important image-generation technique is radiosity. Rather than tracing individual light rays between individual points on a surface (represented by pixels) and the eye, radiosity analyzes the light relationships between surfaces. It looks at the light that falls on a surface as well as light that's emitted from a surface. For instance, if a person is sitting at a wood desk, his face is illuminated a certain way. If he unfolds a large sheet of white paper on the desk, the illumination of the surface below his face changes, as well as the illumination of his face.

Radiosity is based on concepts derived from thermodynamics and heat transfer, according to Andrew Barlow, Turbo SRX product manager for Hewlett-Packard. Its methods also have a lot in common with finite-element analysis. In addition to rendering images, "radiosity can be used

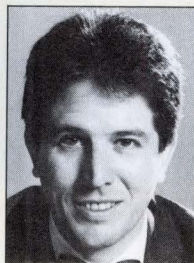
in analysis applications such as understanding heat dissipation in a furnace where there are particles," Barlow says. It can be used to analyze the heat propagation between objects inside the furnace, the walls of the furnace and other objects in terms of the heat they emit, absorb and reflect. Radiosity is roughly equivalent to ray tracing in terms of the computational burden, but it has the advantage of being view-independent, describing only the nature of the surface illumination. Because of this, after a scene is rendered it can be modified using geometric translations. Radiosity, well suited to handling diffuse lighting effects, doesn't produce the sharp shadows and reflections of ray-traced images.

### ■ Graphics tools for shading

Hewlett-Packard's Starbase graphics library, which runs on the Turbo SRX series of workstations, supports graphics either in immediate mode or by generation of separate display lists. The user can interact with the data model, which is expressed in NURBS, on several levels. Flat shading, for instance, can be used for initial design iterations, and then the user can choose to see a Phong-shaded version. Interaction with the image won't be in real time, but it will still take less than one minute. When the user is ready for a full-blown, ray-traced rendering of the scene—and is willing to walk away from the computer for several hours—ray tracing can be performed on exactly the same data set or display list used for the lower levels of rendering.

Similarly, the Dynamic Object Rendering Environment (Dore) from Ardent Computer (Sunnyvale, CA) is a graphics toolkit that lets an object be described to it in terms of all the surface and shading attributes the user wishes. Having so described the object or scene, the user can dynamically select the level of rendering. Ardent has instituted a licensing program for porting Dore to systems other than its own Titan graphics supercomputer. The company has also announced its support for the Renderman interface, but emphasizes that Renderman isn't itself a rendering software system but rather a standard way of describing rendering procedures. "Renderman is a nice way of describing shading, but it's not a nice way of doing it. We've got to solve both problems," says Bruce Borden, vice-president of strategic

## Interactivity vs. photorealism in computer graphics



computational science is characterized by incredible amounts of data that must be examined and analyzed. Visualizing data obtained either experimentally or through simulation is the bread and butter of the computational scientist. By viewing the data in different representations and from different perspectives, the scientist can achieve an intuitive understanding of the problem being studied.

To assist computational scientists and others who deal with complex collections of data, a new class of graphics supercomputer has been created. These computers are designed to let scientists and engineers perform large-scale computations on massive amounts of data and display the results interactively as the computation proceeds. Scientists are just starting to use graphics supercomputers for applications in areas such as computational fluid dynamics, computational chemistry, mechanical design and analysis, geophysics, and other computational sciences.

In the task of interactive visualization, there's often a trade-off between the desire for immediate interactive response and the level of detail and realism represented in the image. But realism isn't necessarily the purpose of data visualization. Shadows and reflections on atoms in a molecule have no direct relationship to the physical reality of the molecular structure. On the other hand, they do let the scientist visualize a structure's three-dimensional nature.

Each figure of dynamic representation can contribute to an understanding of the data. Lighting and shading can be used to present three dimensions. Colors can represent gradations or differences in temperature, velocity, pressure, density and other such factors. Transparency lets the user peer into the middle of the data without losing sight of the whole.

But many of these advanced features such as shadows, reflections and tex-

tures take time to generate even on the most powerful computers, thus delaying the user's interaction with the data. The added value that these features contribute may not justify disturbing a smooth and instantaneous response as the scientist manipulates the data.

Features of computer graphics provided in hardware will be used most heavily for interaction with data. The state-of-the-art today, for example, includes 3-D surface representations such as Phong shading with specular highlights and transparency that can be animated at the rate of 5 to 10 frames/s. In the near future, hardware will advance to include texture maps and higher frame rates.

Photorealistic images are important in applications where realism is desired in the end product—such as movie and television animation and special effects. In other fields, such as automotive design, photorealism may be important in the final stage of the design process.

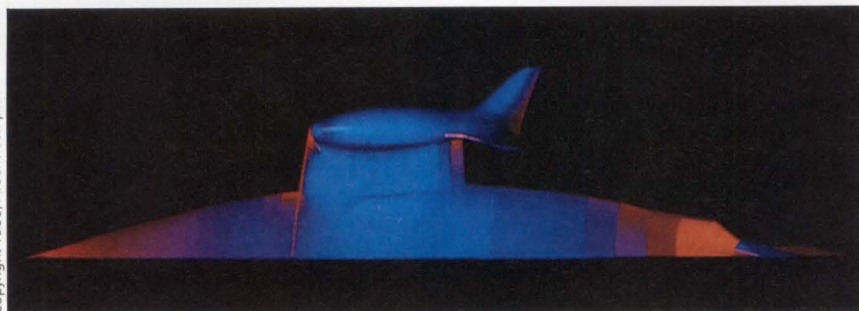
The problem with photorealism packages today is that they aren't integrated with the software that generates interactive dynamic displays. A scientist who wants to interact with the data and produce final images with photorealism must write two programs or, at least, deal with separate graphics interfaces.

The Dynamic Object Rendering Environment (Dore) by Ardent Computer (Sunnyvale, CA) can mitigate this problem by providing a single program interface to dynamics and photorealistic image generation. Dore is currently being ported to Sun and Apollo workstations and Cray supercomputers, in addition to graphics supercomputers.

The interactivity and the image-generation capabilities provided by new-generation graphics supercomputers can address 95 percent of a scientist's requirements; the capability for photorealistic images alone addresses only about 5 percent of those needs. Scientists and application developers, however, aren't interested in becoming graphics experts. Photorealistic images will become a popular graphics tool only when they're easy to develop without sacrificing interactivity.

**Bruce Borden**, Vice-President of Strategic Planning, Ardent Computer

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*High-quality rendering of surfaces can often bring out unseen flaws and mistakes. In the yacht hull, computational fluid dynamics revealed a surface anomaly shown by the red band extending from the front of the keel up around the hull.*

planning at Ardent.

■ CPU handles rendering

A traditional way of speeding throughput for graphics systems has been to build specialized coprocessors and accelerators. Silicon Graphics, for example, developed its Geometry Engine IC to speed the very repetitive matrix transformation and clipping operations needed in geometry calculations for rotation, scaling, translation and clipping. Seiko developed its PRE to offload the calculation of lighting equations for Phong shading. In workstation and super-workstation architectures, there's also been a trend toward integrating more and more graphics computation burden into the main CPU.

"If you can provide a general-purpose unit of sufficiently high computation performance, you don't need special gadgets," says Steve Blank, Ardent's vice-president of marketing. Workstations with hardwired lighting equations aren't able to use them for more complex surface-rendering operations. At some point, "you need a much more general-purpose processor that executes an arbitrary procedure that the shading software has downloaded," says Pixar's Porter. Performing even more graphics processing on the general-purpose CPU also is an advantage when working with software using immediate-mode graphics because the graphics commands embedded in the design data don't have to be offloaded to a specialized coprocessor.

Both the Ardent Titan and the Graphics Supercomputer made by Stellar Computer (Newton, MA) are examples of machines in which the designers have executed as much graphics processing as possible on the main processing units. But when it came to pixel processing—the calculation of the actual pixel values

based on the parameters of the shading model—the designers of both machines turned to specialized hardware. Stellar, for example, sends the computed shapes to a rendering processor via a dedicated data link.

■ Specialized rendering hardware

If the computation speeds for ray tracing and radiosity are to be reduced to manageable levels, it will be through the aid of specialized hardware for rendering. At present, the top contender for a "ray tracing engine" seems to be the Pixel

***"Renderman is a nice way of describing shading, but it's not a nice way of doing it. We've got to solve both problems."***

—Bruce Borden, Ardent Computer



Machine from AT&T (Holmdel, NJ). The PXM900 Series of graphics workstations uses parallel configurations of AT&T's 32-bit 10-MFlops DSP32 digital signal processor (DSP) chips. Up to 82 DSP32s can be configured in the Pixel Machine for an aggregate of 820 MFlops of computing power. Each of as many as 64 DSP chips is assigned a portion of the frame buffer, which lets the PXM900 support resolutions as high as 1,280- $\times$ 1,024- $\times$ 32-bit pixels.

The use of DSPs in a rendering engine offers a balance of processing speed and programmability. DSP chips, while not as versatile as bit-slice processors, don't need to be programmed in microcode and can offer higher speeds for a specialized range

of operations. They're suited for tasks such as matrix multiplication (used in geometric transformations), cross products (for calculating surface normals and vectors of reflection) and multiply/accumulate operations (for filtering and antialiasing operations). Their range of programmability gives them an advantage over hardwired rendering chips in that they can adapt to new developments in graphics algorithms. The ability to use them in parallel, without consuming as much board real estate as multichip bit-slice designs, assures for them a bright future in high-end rendering hardware.

The PXM900 uses the same DSP32 chip for two classes of operations. In the geometry pipeline, up to 18 DSP32s do the transformation processing on NURBS for operations such as translation, scaling, rotation and clipping. A parallel array of up to 64 DSP32s, assigned to different sections of the frame buffer, performs both lighting and shading calculations.

AT&T has developed libraries of software routines for the PXM900 that can be called from C programs. A graphics library called Piclib supports the generation of NURBS—bicubic patches, quadratic patches, spheres and other high-level surface primitives. It also supports flat, Gouraud and Phong shading, multiple-colored light sources and mapping of 2-D textures onto 3-D surfaces.

A second library, called Raylib, is specifically designed to perform ray tracing at high speed. With Raylib, a user can disable features such as shadow, reflection and transparency for a quick look at an image. The Pixel Machine has dramatically shortened the time required for complex ray tracing. An image that takes 18 minutes to render on a VAX-11/780 can be rendered in less than one minute using the PXM900, according to Gary Jablonsky, application engineer for AT&T Pixel Machines. AT&T is also reported to be studying the Renderman proposal, but the company hasn't yet made any decision to endorse it.

While expressing interest in photorealism, mainstream workstation manufacturers, such as Raster Technologies and Silicon Graphics, are more focused on what they can provide at an acceptable workstation cost (somewhere around \$50,000) in the near future. Silicon Graphics' Clark says that about 90 percent of the market for 3-D CAE/CAD can be

satisfied with what amounts to a subset of the rendering capabilities that comprise true photorealism. These include trimmed NURBS—surfaces with terminated edges—and Boolean solids. Boolean solids are a higher level primitive than NURBS in that they logically combine shapes defined by NURBS. A tube, for example, can be defined by subtracting a cylinder from a previously defined, slightly larger cylinder. The resulting tube would have walls with a thickness equal to half the difference between the diameter of the two cylinders.

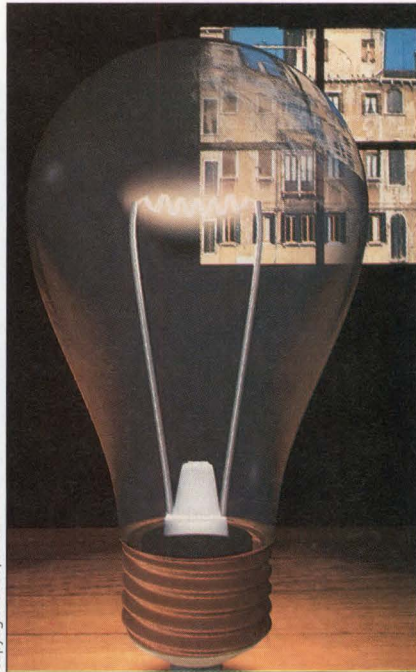
Procedural and mapped textures, as well as environment mapping, also are on Clark's list. Ray-traced images aren't part of the subset within the near future. Neither is transparency, the ability to look inside of data representing solids that lets a user rotate the model and view it internally from different angles.

For applications further in the future, efforts are underway to push realism beyond the traditional distinction between computer-generated graphics and imaging, or image processing. In computer-generated graphics, the computer generates the image to be manipulated and analyzed from its own commands and data. Imaging, on the other hand, acquires a video image of a real object and generates data for analysis and manipulation from the image. The data extracted from imaging isn't the same as the graphics primitives that generate images in graphics systems. Imaging data is usually the result of filtering operations, contrast enhancements and statistical information about an image.

### ■ What's needed for the future

Future scientific visualization of mechanical, as well as natural, processes will require a blend of both graphics and imaging techniques, according to Larry Kaplan, vice-president and general manager of the Information Display Group at Tektronix (Wilsonville, OR). "Ideally, you'd like to be able to drive the car you've designed through a brick wall, or to see how it looks in the TV commercial, or how it photographs from all different angles, before you even touch a machine tool," he says.

What's needed to achieve the realistic manipulation of imaging is a combination of processing power, software and fiberoptic networks at a reasonable cost, according to



Copyright 1988, Pixar.

*Representing a tour de force of high-end rendering techniques, the tabletop is a two-dimensional scanned image of wood grain that has been mapped to the surface. The base of the light bulb is a procedural texture map where the normals representing the surface were perturbed to give the metallic, threaded effect. The glass of the bulb shows both transparent and reflective attributes, and the filament appears to be radiating light, which falls on the table.*

Kaplan. The latter would be required to pass 1,204- $\times$ 1,024-pixel images around a network at a 30-frame/s rate. Kaplan views Renderman as "a standard that for once in our lives is out ahead of the technology."

Although there are no such products now, Kaplan cites some developments that may lead the way soon. One is what he calls "fractal decoding." Fractals are equations that describe the structures of natural formations such as plants, mountains and clouds. Research has shown that it's possible to analyze an image such as a cloud down to its fractal expression. The compact equation can be stored and called by the system to reproduce the cloud, or it can be modified to produce a somewhat different cloud. The ability to decode images into fractal expressions would relieve developers of the need to search for the proper abstract mathematical formulas.

### ■ Many forces push for realism

The push for realism in computer graphics is taking place on many levels. The mechanical CAD designer

desires as much realism as can be had for a given cost while still maintaining the ability to interact with the display in real time. Design management is looking for the most realistic renderings possible for final analysis of designs, for the preparation of presentations, and for market research and advertising. The entertainment industry would like to use realistic renderings for video editing and numerous other possibilities. The natural sciences would like to visualize compute-intensive simulations of physical processes in real time.

In reaching these goals, hardware will have to tread the classic thin line between specialized functionality for speed and more general programmability to be able to adapt to new software techniques. System designers are trying to push specialized silicon such as that used in the graphics pipeline even further out toward the final pixel rendering. This makes it easier to couple graphics and general computation more tightly. Both hardware and software will undoubtedly rise to the challenge of providing what users desire most—as much realism and as much interactivity as possible for a given price. ■

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# Mixed-mode simulator accurately models real-world designs

*Integrated simulation lets designers monitor the interaction of digital and analog events to verify mixed-mode ASICs, systems and boards.*

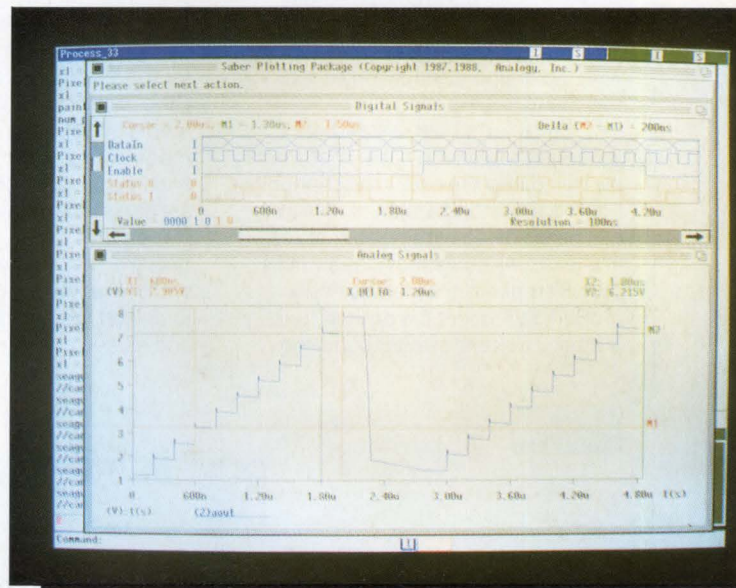
Doug Johnson, BSEE

**A** wealth of new development tools for circuit-level design and analysis has appeared over the past few years, most of it for digital rather than analog circuitry. But designers of mixed analog/digital application-specific ICs, boards and systems have had no practical tools to simulate their designs as implemented in the real world. This picture was changed this year, however, by the introduction of Saber/Cadat—a merger of Analog's Saber analog simulator and HHB Systems' Cadat digital simulator. Saber/Cadat is the first general-purpose mixed-mode simulation tool for circuit- through system-level designs.

In terms of simulation tools, the designers of mixed-mode ASICs, computer boards and systems share many common requirements, including speed. Board- and system-level designers, for example, demand that a simulator simulate every device on a board, both analog and digital, in a reasonable amount of time. But a reasonable amount of time to the IC designer, who has no other option besides simulation, is far too much time for board and system designers, who have the ability to prototype and test their designs—a luxury the IC designer never had.

An early stumbling block to achieving speed in mixed-mode simulation was the performance disparity that existed between digital and analog simulators, the primary problem being that analog simulators operated only on very simple circuits (see "The analog-digital gap," p 67). But the appearance of behavioral analog modeling on commercially available tools in 1986 (when Analog's Saber was introduced) gave the designer the ability to simulate a design at the desired level of detail, making mixed-mode simulation practical. Simulating a phase-locked loop may require hours, if not an entire day, if done at the circuit level. Modeled behaviorally, the same part can be simulated in minutes. Also, without behavioral modeling, the time involved in modeling even a moderate-sized mixed-mode ASIC at the transistor level would be prohibitive.

*Doug Johnson is vice-president of marketing and sales at Analog (Beaverton, OR).*



*The Saber/Cadat mixed-mode simulation environment tightly couples analog and digital elements so that both can be modeled behaviorally. This tight coupling, evident here in output from an adaptive gain stage, is critical in handling feedback systems.*

## Simulating a digital gain-control system

The analysis of a circuit as tightly coupled as a digital gain-control system has until now been impossible. With the Saber/Cadat mixed-mode simulation environment, however, this type of system can be analyzed. The circuit is easily partitioned into the following four major sections.

- The clock, which is easily modeled with Saber and is simply called into the circuit description.
- Sample and hold, a standard model available with Saber that's simply called into the circuit description.
- A gain-setting amplifier, which can be modeled within Saber at several levels. Analogy provides amplifier block templates that can be easily modified to reflect the desired functionality. Once the unit is behaving

correctly as a block, it can be broken down into the actual components available in Saber's standard component library.

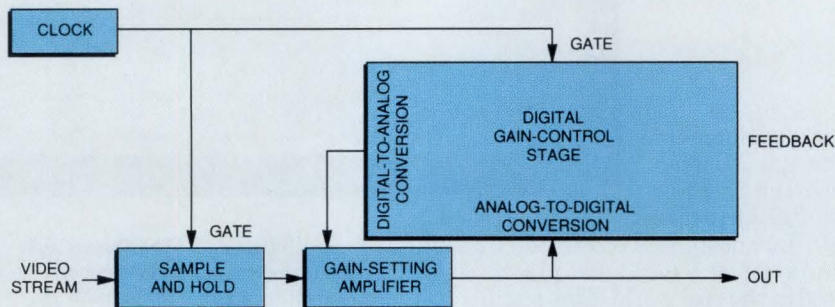
- A digital gain-control stage, a complex block incorporating a large amount of digital logic as well as a microprocessor to do the calculations. Using Cadat's large component library for the SSI and MSI devices, and either choosing the microprocessor software model or using the Cats hardware modeler from HHB Systems, the LSI and microprocessor circuitry models are also easily obtained.

Even for a circuit as complex as this one, the models are readily available within the two simulators. The behavioral-level models can also be modified and refined to individual requirements.

Once the parts or models of parts have been identified, interface models supplied by Analogy must be added at any pin that interfaces between digitally described parts and analog-described parts. The Electronic Design Interchange Format (EDIF) net-list processor supplied by Analogy will automatically insert these interface models while the simulators load the connectivity information from the EDIF net list.

When the net list has been loaded, Saber/Cadat is invoked with the design name, and a graphical interface appears from which to set up both the analog and digital parameters. Once the parameters—such as "time begin," "time end" and "truncation error"—are established, the simulator is started. The user doesn't have to invoke Saber or Cadat separately; each simulator is automatically run as necessary to solve the described circuit.

When the simulation is complete, the results are again called up using the graphical interface, and the outputs of the analog and digital elements can be quickly reviewed. Since the output of the amplifier is controlled by the feedback from the digital circuitry, the analog feedback generated increases as the digital signal increases.



Once behavioral simulation solved the thorny mixed-mode modeling problem, the interactivity between analog and digital simulators became the key consideration. Without appropriate simulation tools, designers of mixed-mode devices have had to simulate analog and digital elements separately and then study their interactions. But when one section of a design is simulated and then another is separately simulated, the important issue of feedback is ignored, and there are very few designs that don't have some feedback occurring between sections. Without including feedback, it's impossible to study systems such as motion control or digital gain-control systems, which contain a great deal of feedback.

To ensure accuracy in a mixed-mode simulator, the analog and digital simulators must exchange information. To guarantee speed, the simulators must be able to process

data independently until interaction is necessary. The traditional lockstep algorithm that's used to provide synchronization between analog and digital simulators addresses only

***Until Saber/Cadat,  
designers of mixed-  
mode devices had no  
practical tools to  
simulate their designs  
as implemented in the  
real world.***



accuracy—without regard to the speed of the simulation.

The difficulty in simulating tightly coupled systems with a high de-

gree of feedback has been the synchronization of time steps. The analog simulator must be allowed to take the largest possible time steps so it can "go ahead" of the digital simulator, instead of waiting for the digital simulator to evaluate each event. Then, if the digital simulator uncovers an event that the analog simulator must process, the analog simulator must be able to "backtrack" to the event in question.

Analogy's Calaveras algorithm, however, lets the analog simulator take optimum time steps until a digital event requires analog simulation processing. The analog simulator then reevaluates its solution and—as appropriate—continues forward, or adjusts backward, in time. With the Calaveras approach, both simulators are analyzing the system simultaneously and sharing intermediate results of the solution. This lets feedback propagate through the ana-

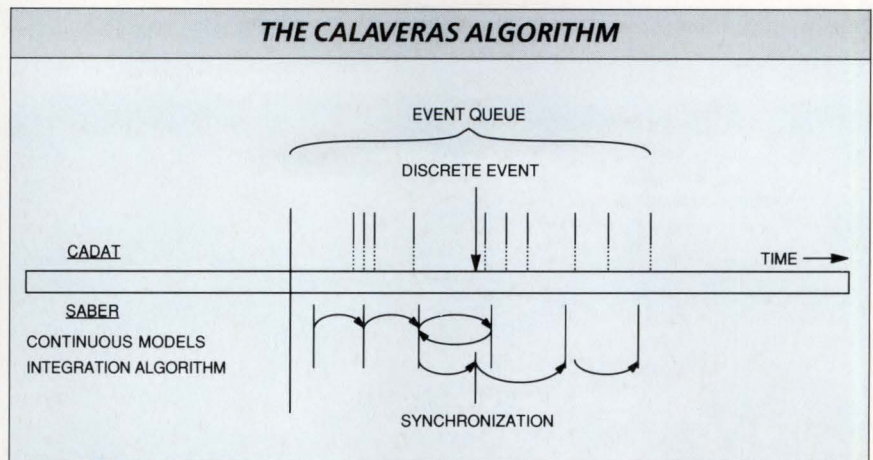
log and digital simulators as needed in any portion of the design.

### ■ Dealing with X states

The interaction between digital and analog simulators creates another problem: handling X states. To resolve an unresolvable simulation, digital simulators deal in a mysterious commodity that's called an X state, which represents an unknown value—neither 0 nor 1. Unfortunately, analog simulators can't accept unknowns.

There are many options for dealing with an X state. An X could be always turned into a 1 or a 0, for example; it could alternate between the two; or there could be a random selection. None of these solutions proves very accurate, however, and they're all costly to implement in terms of CPU time. Saber/Cadat's approach is to leave the signal at the last known value. This approach eliminates a good deal of processing overhead and, in many cases, gives a value that's closer to the true (node) value than that provided by any other solution.

A final, and very important, requirement for a true integration of analog and digital simulation is ease-



*The Calaveras algorithm lets analog simulation run at its own time step until a digital event occurs. Then the analog simulator can reevaluate its solution and backtrack in time or go forward to synchronize events.*

of-use. With Saber/Cadat's single Macintosh-like interface, users are unaware that they are, in fact, dealing with two simulators. Depending on the circuit content, the correct simulator or combination of simulators will be invoked with minimum user intervention. If there are only digital elements in the net list, only Cadat is invoked. If only analog elements are present, only Saber is

called upon. If there's a combination of analog and digital elements, both simulators are called.

### ■ Standard formats necessary

To fit the needs of a general-purpose solution, simulators must also accept standard input formats. For general use, Saber/Cadat will accept standard Electronic Design Interchange Format (EDIF) input, so it can readily accept input from almost any CAE schematic interface package that provides EDIF-out connectivity information. Or, for tighter integration, the simulators can be fed directly with a Saber and Cadat net list through a tuned schematic-capture package, such as Visula from Racal-Redac (Westford, MA).

For analysis of data from the simulators, the user will look at a common output display that can graph separately or simultaneously both digital and analog waveforms, bringing flexibility to the user in a simple structure for interacting with and analyzing the simulation data. ■

## The analog-digital gap

**O**ne major problem with early mixed-mode simulators was that while digital simulators had become very sophisticated, analog simulators lagged far behind. While the digital portion of a mixed-mode tool could operate in an efficient manner, any element to be simulated on the analog side had to be made up of the lowest-level primitive devices. Board designers simulating just one of the analog components in their systems at such an elemental level—assuming the manufacturer would tell them what was actually in the part—would rapidly run out of patience, not to mention compute time.

This primitive orientation of analog simulation is clearly unsatisfactory for today's complex designs. If a designer is trying to simulate a circuit board that contains a pulse-width modulator (PWM), for example, the PWM's function is far more important than the individual functions of the hundreds of transistors the device contains. Yet until the Saber simulator, which Analogy in-

roduced in late 1986, analog simulators could simulate a PWM only in terms of the functions of transistors, resistors or capacitors.

The selection of analog simulation products has been very limited—consisting primarily of the Spice simulator from the University of California at Berkeley, and Spice derivatives. There have also been a number of specialty analog simulators, however, such as Simon and Pacsim, developed to address the ever-increasing demands of the IC designer and the requirements associated with larger and more complex chips.

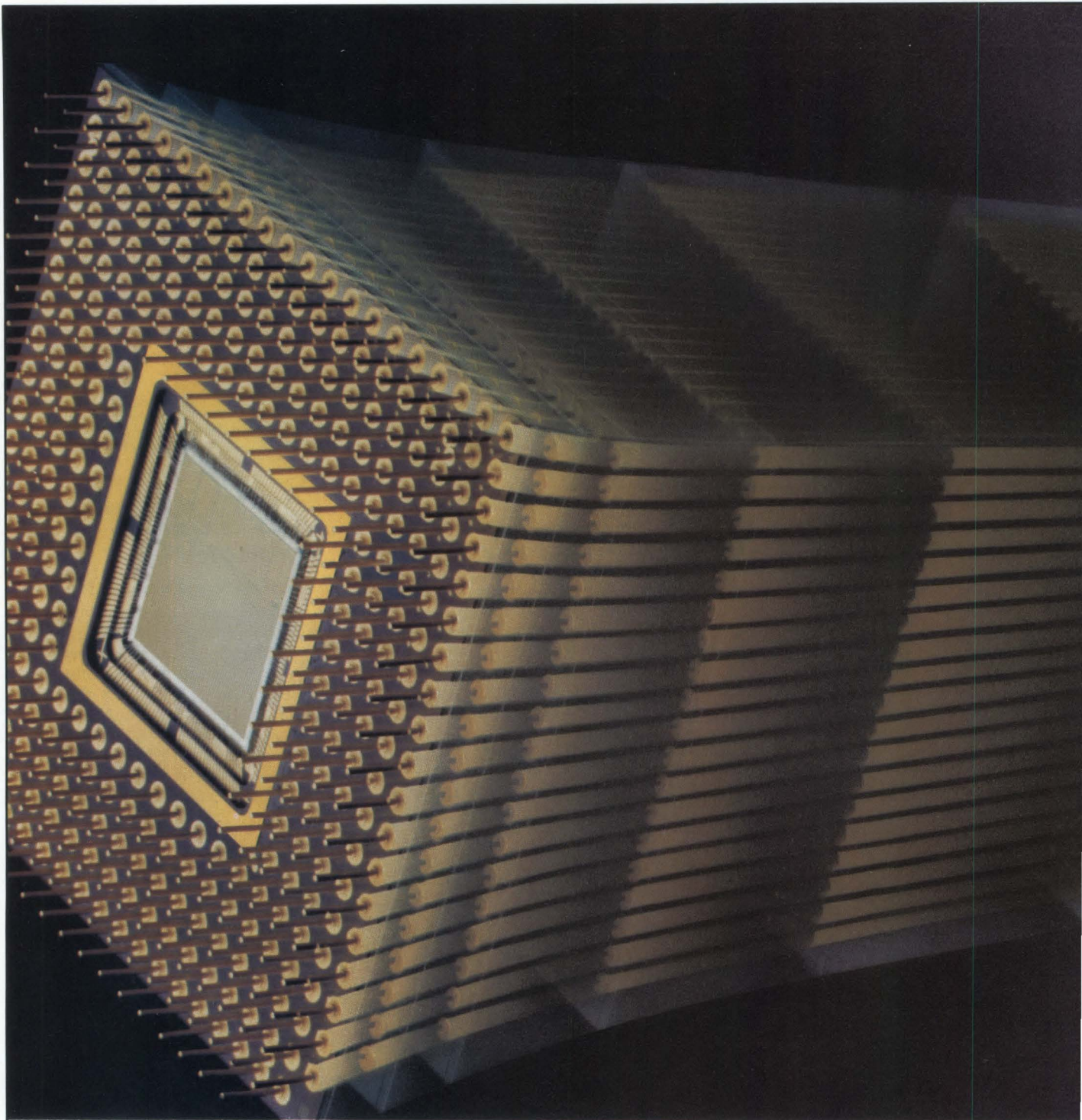
But while these specialty simulators have proven excellent for the development of ICs, they weren't suitable, or easily adaptable, to the domains of board- and system-level design. While these analog simulators reach a solution by solving many simultaneous equations based on the myriad variables of voltage and current in the device, digital simulators reach their solutions based on Boolean logic and the progression of time.

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All Si-Gate CMOS double layer metal.		

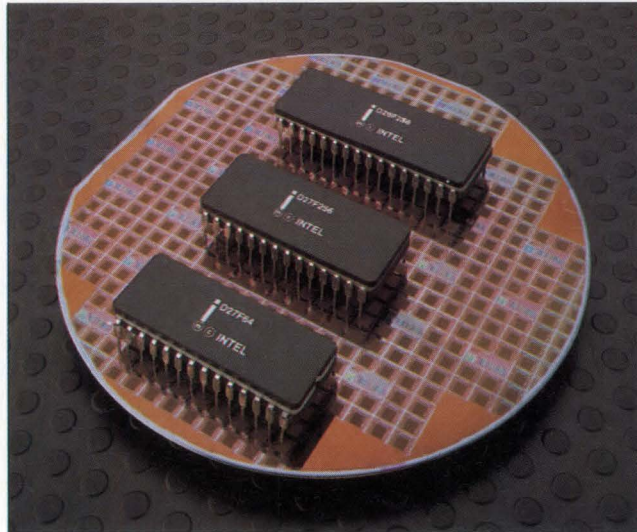
# TOSHIBA

## TOSHIBA AMERICA, INC.

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## Denser devices, flash designs spawn new applications for EEPROMs

John H. Mayer, Senior Associate Editor



Flash technologies are reducing erase times and oxide stress damage. Intel, for example, uses its proprietary ETOX (EPROM tunnel oxide) process technology in its D27F64, D27F256 and D28F256 flash memory family to improve cycling reliability without increasing cell size or complexity.

Increasing densities, higher access speeds, lower prices and the use of low-power CMOS are spawning new uses for EEPROMs. As engineers become more comfortable with E<sup>2</sup> technology, they're finding that the in-circuit and byte-specific programming capabilities are formidable tools when addressing varied and rapidly changing applications.

EEPROMs are now providing both low-density data storage and high-density program storage, sometimes simultaneously in the same system. While not yet up to the solid-state, disk-storage replacement role they've sometimes been predicted to fill, EEPROMs are satisfying a number of niche solutions. High-density, 64- and 128-kbit devices are finding increasing uses in traditional computer applications, while consumer markets are integrating large numbers of 4-kbit and smaller serial I/O parts in products such as automobile radios and TV tuners.

Although lower prices and greater product choice have undeniably played a major role in the move to EEPROMs, much of the growth in the EEPROM market is attributed to wider acceptance of the technology, especially EEPROM's unique ability to be reprogrammed remotely and instantaneously. "The reprogrammability feature of EEPROMs is drifting to profit issues today," says Krish Panu, marketing manager at Xicor (Milpitas, CA). "The way to address today's shorter time-to-market and

shorter product life cycles is to have flexibility in the system to upgrade the software and add features."

Even the military are starting to realize the benefits of EEPROM technology. Last year, military applications provided more than one-fourth of the business for the two largest suppliers of EEPROMs, Xicor and Seeq Technology (San Jose, CA). "Most of the military programs require that nonvolatile memory be

**"The reprogrammability feature of EEPROMs is drifting to profit issues."**

—Krish Panu, Xicor



writable without disassembly," says Gary Rauh, Seeq's manager of product planning. "That pretty much excludes any form of solid-state monolithic memory other than E<sup>2</sup>."

### ■ Monolithic 1-Mbit parts coming

The densest monolithic EEPROMs available are 256-kbit devices. Xicor and Seeq were the first to reach this level; Xicor introduced the first 256-kbit part, the NMOS X28256, in early 1986, and Seeq delivered the 28C256, the first CMOS 256-kbit part, shortly thereafter. A number of other manufacturers have since fol-

lowed suit, including some that, like Xicor, pack four 256-kbit devices together in a 1-Mbit module.

For the consumer market, low-density serial I/O parts are available for about \$1. National Semiconductor (Santa Clara, CA), the leader in this market segment, offers a wide variety of 1- to 4-kbit devices.

But the size of the low-density market is attracting some of the traditional high-density EEPROM suppliers as well. Xicor, for example, is offering a pin-compatible line of 2- to 16-kbit parts. The top of the serial interface line, the X24C16 was the first CMOS 16-kbit serial part developed. It comes in the same 8-pin miniDIP package used on the 2- and 4-kbit devices. Drawing only 3 mA when active and 75  $\mu$ A in standby, the CMOS part is ideal for battery-powered portable applications.

As EEPROMs have assumed a greater role in system designs, a gap has developed between their expensive but flexible in-circuit programmability and the low-cost but limited functionality of EPROMs. IC vendors saw a market for a bulk-erasable part that could provide the benefit of occasional, in-circuit code changes but at a cost low enough to be competitive with EPROMs.

Two bulk-erasable flash technologies are now trying to bridge that gap. Last year, Seeq introduced the first flash EEPROM, the NMOS 128-kbit 48128. This year, it added a 512-kbit part, the 48F512, built in a



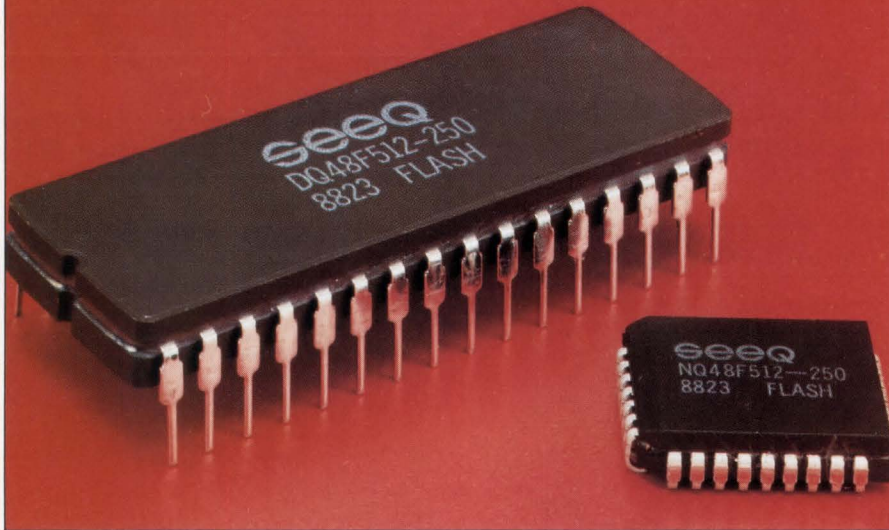
Model	Process	Organization (bits)	Access Time (ns)	Programming Time (ms)	Current: Operating/ Standby (mA)	Packages	Price (100 pieces)	Comments
<b>Advanced Micro Devices</b> PO Box 3453, Sunnyvale, CA 94088 (408) 732-2400								<b>Circle 100</b>
Am2864AE	NMOS	8k×8	200	10	140/70	DIP, LCC, die	\$16.02	pin 1 no connect
Am2864BE	NMOS	8k×8	200	10	140/70	DIP, LCC, die	\$16.02	pin 1 ready/busy
<b>Atmel</b> 2095 Ringwood Ave, San Jose, CA 95131 (408) 434-9201								<b>Circle 101</b>
AT28C04	CMOS	512×8	120	1	30/0.1	DIP, LCC, PLCC	\$7.92	data polling
AT28C16	CMOS	2k×8	120	1	30/0.1	DIP, LCC, PLCC	\$10.80	data polling
AT28C17	CMOS	2k×8	120	1	30/0.1	DIP, LCC, PLCC	\$11.52	data polling, ready/busy
AT28HC16	CMOS	2k×8	30	1	30/0.1	DIP, LCC, PLCC	\$17.16	data polling
AT28HC191	CMOS	2k×8	30	1	80/0.1	DIP, LCC, PLCC	\$9.75	PROM replacement
AT28C64	CMOS	8k×8	150	1	30/0.1	DIP, LCC, PLCC	\$15.50	data polling, 32-byte page
AT28PC64	CMOS	8k×8	150	2	80/0.1	DIP, LCC, PLCC	\$15.50	data polling, 32-byte page
AT28HC64	CMOS	8k×8	55	2	80/0.1	DIP, LCC, PLCC	\$51	data polling, 32-byte page
AT28C256	CMOS	32k×8	150	3	80/0.1	DIP, LCC, PLCC	\$268.35	data polling, 64-byte page
AT28HC256	CMOS	32k×8	60	3	80/0.1	DIP, LCC, PLCC	\$357.19	same as above
AT28MC010	CMOS	128k×8	120	10	80/0.1	module	\$1,500	same as above
<b>Catalyst Semiconductor</b> 2231 Calle de Luna, Santa Clara, CA 95054 (408) 748-7700								<b>Circle 102</b>
CAT28C16A	CMOS	2k×8	150, 200	5	25/0.1	DIP, SO, PLCC	\$7.38	in production
CAT28C17A	CMOS	2k×8	150, 200	5	25/0.1	DIP, SO, PLCC	\$7.92	in production
CAT28C64A	CMOS	8k×8	150, 200, 250	5	30/0.1	DIP, SO, PLCC	\$14.77	sampling
CAT28C65A	CMOS	8k×8	150, 200, 250	5	30/0.1	DIP, SO, PLCC	\$16.20	sampling
CAT93C46	CMOS	64×16, 128×8	—	5	3/0.1	DIP, SO	\$1.85	serial, selectable organization
CAT35C102	CMOS	128×16, 256×8	—	5	3/0.1	DIP, SO	\$3.40	serial, selectable organization
CAT35C104	CMOS	256×16, 512×8	—	5	3/0.1	DIP, SO	\$4.60	serial, sampling
CAT33C104	CMOS	256×16, 512×8	—	5	2/0.05	DIP, SO	\$5.10	serial, sampling
CAT59C11	CMOS	64×16, 128×8	—	10	5/0.1	DIP, SO	\$2.15	serial, industrial temp.
<b>Datakey</b> 407 W Travelers Trail, Burnsville, MN 55337 (612) 890-6850								<b>Circle 103</b>
DK1000	CMOS	64×16	—	10	3/1	evaluation kit	\$7.90	serial, key-shaped
PK16KS	NMOS	2k×8	350	2	80/30	evaluation kit	\$39	portable, key-shaped
PK64KB	NMOS	8k×8	350	10	110/50	evaluation kit	\$77	portable, key-shaped
<b>Exel Microelectronics</b> 2150 Commerce Dr, PO Box 49038, San Jose, CA 95161 (408) 434-0500								<b>Circle 104</b>
XLS2804A	NMOS	512×8	250	10	110/40	DIP	\$5.90	available now
XLS2816A	NMOS	2k×8	250	10	110/40	DIP, PLCC	\$5.60	available now
XLS2864A	NMOS	8k×8	250	10	110/50	DIP, PLCC, LCC	\$16.15	32-byte page, data polling
XLS2865A	NMOS	8k×8	250	10	110/50	DIP, PLCC, LCC	\$16.15	ready/busy, data polling
XLS28C64A	CMOS	8k×8	90	5	50/0.1	DIP, PLCC, LCC	\$28.80	available 4Q88, 64-byte page
XLS28C65A	CMOS	8k×8	90	5	50/0.1	DIP, PLCC, LCC	\$28.80	available 4Q88, ready/busy
XLS46C15	CMOS	2k×8	55	5	90/0.035	DIP, PLCC, LCC	\$5	available now
XLS46HC64	CMOS	8k×8	35	1	75/0.002	DIP, PLCC, LCC	\$33	4Q88, 1-ms chip write, reset
XLS46HC64L	CMOS	8k×8	45	1	75/0.1	DIP, PLCC, LCC	\$33	4Q88, 1-ms chip write, reset
XLM2816AL	NMOS	2k×8	300	10	110/50	CERDIP	\$37.50	military, available now
XLM2865AY	NMOS	8k×8	300	10	110/40	CERDIP, LCC	\$63.80	military, ready/busy, 32-byte page
<b>Key:</b> DIP = dual in-line package; FP = flatpak; LCC = leadless chip carrier; PLCC = plastic leaded chip carrier; SO = small outline package.								

■ PRODUCT FOCUS

Model	Process	Organization (bits)	Access Time (ns)	Programming Time (ms)	Current: Operating/ Standby (mA)	Packages	Price (100 pieces)	Comments
<b>Exel Microelectronics</b> 2150 Commerce Dr, PO Box 49038, San Jose, CA 95161 (408) 434-0500								<b>Circle 104</b>
XLM46C15J	CMOS	2k×8	70	5	90/35	DIP, PLCC, LCC	\$35.20	military, available now
XLM2817AY	NMOS	2k×8	300	10	110/50	DIP, LCC	\$37.50	available now
XLS93C46	CMOS	64×16	250	10	3/0.1	DIP, SO	\$1.66	serial interface
<b>Fujitsu Microelectronics, IC Div</b> 3545 N First St, San Jose, CA 95134 (408) 922-9000								<b>Circle 105</b>
MBM28C64/65	CMOS	8k×8	250	10	20/0.1	DIP, PLCC	\$15	available 3Q88
MBM2212	NMOS	256×4	200	10	60/30	DIP	\$4	available now
<b>Hitachi America</b> 2210 O'Toole Ave, San Jose, CA 95131 (408) 435-8300								<b>Circle 106</b>
HN58C65	CMOS	8k×8	200, 250	15	—	FP	\$14	—
HN58C66	CMOS	8k×8	250	15	—	FP	—	available 3Q88
<b>Hughes Aircraft</b> Microelectronics Ctr, 500 Superior Ave, Newport Beach, CA 92658 (714) 759-2727								<b>Circle 107</b>
H3104A	CMOS	512×8	500	0.1	1/0.002	DIP	—	low power, mil-temp. available
H3108A	CMOS	1k×8	500	0.1	1/0.002	DIP	—	same as above
H3208	CMOS	1k×8	500	0.1	0.75/ 0.002	DIP	—	low power, single 5-V supply
H3248	CMOS	2k×4	500	0.1	0.75/ 0.002	DIP	—	same as above
<b>Intel</b> 1900 Prairie City Rd, Folsom, CA 95630 (800) 548-4725								<b>Circle 108</b>
27F64	CHMOS	8k×8	150 μs	1 s/chip	30/0.1	DIP	\$14.30	flash, EPROM replacement
27F256	CHMOS	32k×8	170 μs	4 s/chip	30/0.1	DIP	\$31.40	flash, multiplexed address
28F256	CHMOS	32k×8	170 μs	4 s/chip	30/0.1	DIP, PLCC	\$31.40	flash, nonmultiplexed, JEDEC comp.
<b>Microchip Technology</b> 2355 W Chandler Blvd, Chandler, AZ 85224 (602) 963-7373								<b>Circle 109</b>
28C16A	CMOS	2k×8	150	1	30/0.1	DIP	\$6.85	in production
28C04A	CMOS	512×8	150	1	30/0.1	DIP	\$6.44	in production
28C64A	CMOS	8k×8	150	1	30/0.1	DIP, PLCC, LCC	\$12.47	mil version available
28CP64A	CMOS	8k×8	150	4	60/3	DIP, PLCC, LCC	—	available 4Q88, mil versions
28CP64B	CMOS	8k×8	100	4	60/3	DIP, PLCC, LCC	—	same as above
28CP256A	CMOS	32k×8	150	4	60/3	DIP, LCC	—	same as above
28CP256B	CMOS	32k×8	100	4	60/3	DIP, LCC	—	same as above
24C01	CMOS	128×8	—	20	4/1	DIP	\$3.30	serial, available 3Q88
24C02	CMOS	256×8	—	20	4/1	DIP	\$4.39	serial, available 3Q88
24C04	CMOS	2×256×8	—	20	4/1	DIP	\$6.59	serial, available 3Q88
<b>National Semiconductor</b> 2900 Semiconductor Dr, Santa Clara, CA 95052 (408) 721-4407								<b>Circle 110</b>
NMC9306	NMOS	16×16	—	—	10/3	DIP, SO	\$1.20	serial interface
NMC9346	NMOS	64×16	—	—	12/3	DIP, SO	\$1.60	serial interface
NMC93C46	CMOS	64×16	—	—	2/0.05	DIP	\$2.10	serial interface
NMC93C56	CMOS	128×16	—	—	2/0.5	DIP, SO	\$3.20	serial interface
NMC93C66	CMOS	256×16	—	—	2/0.05	DIP, SO	\$4.80	serial interface
NMC93CS46	CMOS	64×16	—	—	2/0.05	DIP	\$3.60	serial interface
NMC93CS56	CMOS	128×16	—	—	2/0.05	DIP, SO	\$6.20	serial interface
NMC93CS66	CMOS	256×16	—	—	2/0.5	DIP, SO	\$8.40	serial interface

Model	Process	Organization (bits)	Access Time (ns)	Programming Time (ms)	Current: Operating/ Standby (mA)	Packages	Price (100 pieces)	Comments
<b>NEC Electronics</b> 401 Ellis St, Mountain View, CA 94039 (415) 960-6000								<b>Circle 111</b>
D28C64C	CMOS	8k×8	200, 250	10	20/0.1	DIP	\$14	available now
<b>Seeq</b> 1849 Fortune Dr, San Jose, CA 95131 (408) 432-7400								<b>Circle 112</b>
28C256	CMOS	32k×8	200	—	60/0.15	DIP, PLCC, LCC, FP	\$114.95	64-byte page
28C65	CMOS	8k×8	200	—	50/0.15	DIP, PLCC, LCC	\$27.60	ready/busy pin, 64-byte page
28C64	CMOS	8k×8	200	—	50/0.15	DIP, PLCC, LCC	\$23.50	64-byte page
2864	NMOS	8k×8	200	—	110/40	DIP, LCC, PLCC, FP	\$22.95	ready/busy pin
2817A	NMOS	2k×8	200	2	110/40	DIP, PLCC, LCC	\$12.65	ready/busy pin
2816A	NMOS	2k×8	200	2	110/40	DIP	\$11	—
52B33	NMOS	2k×8	200	—	110/40	DIP, LCC	\$29.90	—
52B13	NMOS	2k×8	200	—	80/30	DIP	\$13.10	—
38C32	CMOS	4k×8	35	5	100/60	DIP, PLCC, LCC	\$32.50	high-speed address, data latches
38C16	CMOS	2k×8	35	5	100/60	DIP, PLCC, LCC	\$20	same as above
36C32	CMOS	4k×8	35	5	100	LCC, DIP	\$25	bipolar pin-out
36C16	CMOS	2k×8	35	5	100	DIP, LCC	\$15	bipolar pin-out
2804A	NMOS	512×8	200	2	80/40	DIP	\$7.45	—
48F512	CMOS	64k×8	200	1	60/0.1	DIP, PLCC, LCC	\$34.90	flash EEPROM
48F010	CMOS	128k×8	200	1	60/0.1	DIP, PLCC, LCC	—	flash, available 4Q88
<b>SGS-Thomson Microelectronics</b> 1000 E Bell Rd, Phoenix, AZ 85022 (602) 867-6100								<b>Circle 113</b>
M9306	NMOS	16×16	—	—	5/3	DIP, SO	\$0.68	—
M9346	NMOS	64×16	—	—	12/3	DIP, SO	\$1.03	—
TS93C46	CMOS	64×16, 128×8	—	—	4/0.1	DIP, SO	\$1.25	organization selectable
TS59C11	CMOS	64×16, 128×8	—	—	4/0.1	DIP	\$1.25	organization selectable
<b>Toshiba America</b> Electronic Components Business Sector, 9775 Toledo Way, Irvine, CA 92718 (714) 455-2000								<b>Circle 114</b>
TC58257API/AF	CMOS	32k×8	170, 200, 250	—	30/0.1	DIP, SO	\$55	flash, production 9/88
<b>Xicor</b> 851 Buckeye Ct, Milpitas, CA 95035 (408) 432-8888								<b>Circle 115</b>
X2804A	NMOS	512×8	250 and up	10	80/50	DIP	\$7.96	commercial, industrial, military
X2816A/B	NMOS	2k×8	250 and up	10	110/50	DIP, LCC	\$9.50	B-version data polling
X2864A	NMOS	8k×8	250 and up	10	140/60	DIP, LCC, PLCC, FP	\$16	data polling
X2864AT	NMOS	8k×8	350, 450	10	110/60	DIP, LCC	\$87.80	0° to 150° C
X2864B	NMOS	8k×8	120, 150, 180	5	150/80	all	\$36.98	32-byte page, data polling
X2864H	NMOS	8k×8	70, 90	5	150/80	all	\$98.02	same as above
X28C64	CMOS	8k×8	200 to 350	10	40/0.2	all	\$36.98	64-byte page, data polling
X28256	NMOS	32k×8	250, 300, 350	10	120/60	DIP, LCC, PLCC	\$119.83	64-byte page, data polling
X28C256/B	CMOS	32k×8	150 to 350	10	60/0.2	all	\$136 to \$208	same as above
X28C010	CMOS	131k×8	200	10	80/0.5	DIP	—	64-byte page, data polling
XM28C010	CMOS	131k×8	250, 300	10	70/0.8	module	\$952.43	128-byte page, data polling
X2402	NMOS	256×8	—	10	30/25	DIP, SO	\$4.24	serial interface
X2404	NMOS	512×8	—	10	30/25	DIP, SO	\$6.12	serial interface
X24C04	CMOS	512×8	—	10	2/0.06	DIP, SO	\$7.34	serial interface
X24C16	CMOS	2k×8	—	10	3/0.075	DIP, SO	\$13.86	serial interface

INTEGRATED CIRCUITS



Seeq's 512-kbit flash EEPROMs operate from a 12-V power source and provide in-circuit erasure in a maximum 7.5 s. Cell size is approximately 25 square microns, almost 40 percent smaller than the company's first 128-kbit flash memory.

1.5-micron CMOS, single-metal, double-poly process. Seeq expects to unveil a 1-Mbit device this summer. Erasure time for the 512-kbit part is about 3 percent of that for a conventional UVEPROM.

Seeq's flash memories use avalanche injection, the same programming technique used in EPROMs, while the design's thin-gate oxide allows electrical erasure via Fowler-Nordheim tunneling (as in full-featured EEPROMs). The flash products avoid the major drawback accompanying full-featured EEPROM designs—increased die size—by using a split-gate layout that merges a bit-selection transistor with a floating-gate transistor. The result is an EEPROM cell about 1.1 times the size of a conventional EPROM cell.

■ 12-V operation

The 48F512 represents a significant evolution over Seeq's first flash part. The earlier 48128 required a 21-V power supply on multiple pins. In contrast, the newer product's programming and erasure require an external 12-V power supply applied to pin 1. In addition, the use of a 1.5-micron CMOS process limits power dissipation to 60 mA active and 100  $\mu$ A standby. Byte write time has been reduced to 1 ms, and chip erase and page erase times are as low as 5 s. Latches on address, data and con-

trol inputs keep the parts compatible with the erase and programming cycles of host microprocessors.

A different approach to flash memory was taken by Intel (Santa Clara, CA) last April. "It's not an E<sup>2</sup> because it doesn't have all the same characteristics of an E<sup>2</sup>, but it's not an EPROM because it's electrically erasable," says Dick Pashley, flash memory general manager. The com-

***"When we introduce 1-Mbit parts, EEPROMs won't be able to touch our flash products because their cell size is so large."***

—Dick Pashley, Intel



pany unveiled three devices: the 64-kbit 27F64 and two 256-kbit parts, the 27F256 and 28F256. The 27F64 is a direct socket replacement for 64-kbit EPROMs. The two 256-kbit parts are differentiated by pin-out. To maintain compatibility with 28-pin EPROMs, the 27F256 features a multiplexed address and write-enable pin. The second 256-kbit part, the 28F256, offers a non-multiplexed pin-out that accommo-

dates density upgrades to 2 Mbits.

All three memories are based upon Intel's proprietary ETOX (EPROM tunnel oxide) technology. As with traditional EPROM technology, Intel's ETOX approach uses a standard single-transistor EPROM cell that stores its charge on a floating gate. Programming is by hot electron injection. Like conventional EEPROMs, the devices use an electron tunneling mechanism to erase all memory cells simultaneously.

■ EPROM scalability

Intel derives a number of advantages by sticking to the conventional, single-transistor EPROM cell. First, the architectural simplicity eventually will let the company undersell full-featured EEPROMs by a significant margin, according to Pashley. Second, the single-transistor cell is as scalable as a standard EPROM. "We have a 2.5-times area advantage over full-featured EEPROMs," says Pashley. "When we introduce 1-Mbit parts, EEPROMs won't be able to touch our flash products because their cell size is so large that the die won't fit into a package."

The ETOX design also offers a side benefit—higher reliability. Two aspects of the ETOX process, lower voltage operation and the use of separate junctions for program and erase, provide this dividend. Early reliability data shows reprogramming failure rates for the Intel parts at less than 0.01 percent over a 100-cycle endurance and under 0.1 percent over 10,000 cycles. EEPROMs typically experience 5 percent failure rates over 10,000 cycles.

Still, not everyone is convinced that flash memories will have a dramatic impact on the full-featured EEPROM market. Xicor's Panu sees many unanswered questions. "You must have a high-voltage regulated power supply to use a flash because people are talking of 12.5, 12.75, 15 and 18 V," he says. "Second, if you want to change one byte on a page, you can't do that with a flash. You have to erase and rewrite the whole memory, and that's a huge operation. Finally, as far as endurance is concerned, people are talking about 100 cycles. There's very limited data available to say that you could do anything better." ■

COMPUTERS AND SUBSYSTEMS

**68030 CPU board delivers 32-Mbyte/s Multibus I throughput**

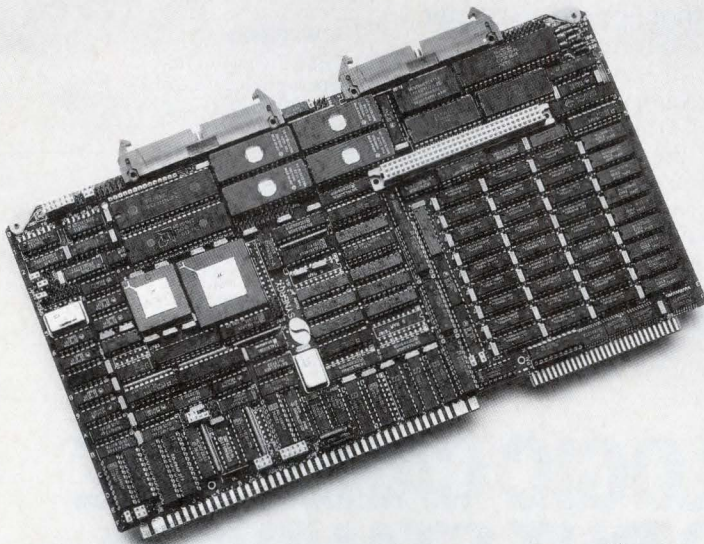
A 33-MHz CPU board for Multibus I, the SM31 features the MC6881/68882 math coprocessor, an intelligent 4-Mbyte/s small computer system interface (SCSI) controller and up to 40

Mbytes of dynamic RAM. Based on a 68030 microprocessor, the board offers daughter-board options that provide high-speed math functions (20 MFlops), high-resolution video display (1,660×1,280 pixels), and Ethernet, keyboard and mouse control.

The CPU supports Unix, OS-9 and

PDOS operating systems, as well as two memory management units (MMUs): the 68030's on-chip MMU and an enhanced version of the Stanford University Network MMU. Included are 2 Mbytes of EPROM, five 16-bit timers and battery backup for up to 40 Mbytes of RAM.

Multibus Plus, an extension to Multibus I, has been incorporated on the board. It features 32-bit data transfers, a 256-Mbyte address space, burst transfers and dynamic bus sizing. This extension, when used in conjunction with the 68030's burst-mode capability, lets the CPU transfer data over the Multibus at more than 32 Mbytes/s. A 32-bit local bus provides the 68030 with arbitration-free access to a minimum of 4 Mbytes and as much as 40 Mbytes of local DRAM. The standard configuration, which includes a 20-MHz 68030, a SCSI controller and 4 Mbytes of DRAM, is priced at \$4,575 in 100-piece quantities.



**Synergy Microsystems**

179 Calle-Magdalena  
Encinitas, CA 92024

Circle number 130

**68000 single-board system features C and OS-9 in ROM**

Designed for system engineers who want to build simple real-time control systems, the GESSBDS-6 is a single-board, multiuser computer system with nearly 512 kbytes of ROM-resident software. The board lets one or two users program directly in C or 68000 assembly language under the OS-9 real-time operating system. A battery-maintained, 128-kbyte CMOS RAM disk is included for storing source and object files. Floppy or hard disks, two additional users, a parallel printer and up to 8 Mbytes of additional memory can be added at any time. The board, which

comes with an OS-9 V2.1 operating system, a C compiler, a symbolic debugger, a relocatable linker and a screen text editor, is priced at \$1,495.

**Gespac**

50 W Hoover Ave  
Mesa, AZ 85202

Circle number 131

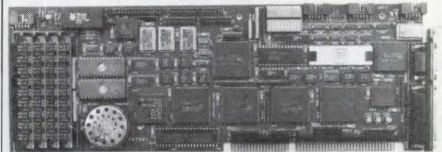
**Floating-point processor provides 8 MFlops**

The PL800 floating-point array processor has a peak performance of 8 32-bit MFlops. Software provided with the device includes 457 routines operating on arrays and matrices within the 60 kbytes of cache memory on each card. The processor uses direct memory access transfers to move data to the entire address of the host personal computer. The board is priced at \$1,995.

**Eighteen Eight Laboratories**

771 Gage Dr  
San Diego, CA 92106

Circle number 132



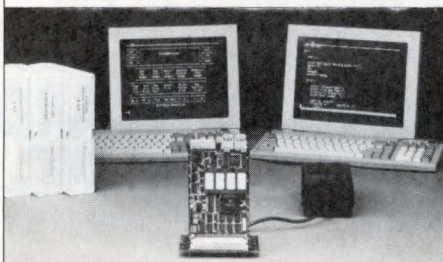
**PC AT SBC fits passive backplane systems**

The CAT901 puts a complete, low-power IBM PC AT-compatible computer on a full-size AT card for use in passive backplane systems. Built around a 12-MHz 80286, the board provides up to 4 Mbytes of on-board RAM, a caching hard disk controller, a floppy controller, printer ports, two serial ports, a keyboard port and a daughter-board expansion port. The board also includes speed control circuitry that slows the 80286 down in order to accommodate standard AT peripheral boards.

**Diversified Technology**

PO Box 748, 112 E State St  
Ridgeland, MS 39158

Circle number 136



COMPUTERS AND SUBSYSTEMS

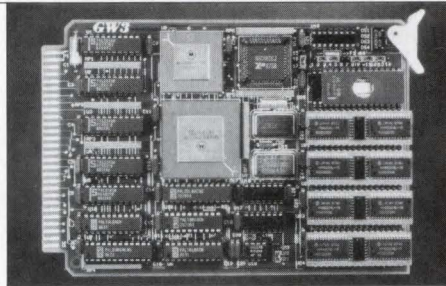
**VME CPU suits multiprocessing systems**

A 25-MHz 68020-based single-board computer, the DVME-137 is targeted at high-reliability applications that can't afford downtime for maintenance and repairs. In addition to its on-board monitor and self diagnostics, the board includes a feature that prevents a circuit fault from disabling the entire chassis system. By virtue of geographical and programmable base addressing, the board permits the flexible configuration of spare boards in a system. Included are 4 Mbytes of zero-wait-state dynamic RAM, as well as a VME Subsystem Bus, a pair of serial ports, sockets for 28-pin EPROMs and three 16-bit counter/timers.

**D-4 Systems**

475 S Bascom Ave, Suite 202  
Campbell, CA 95088

Circle number 135



**STD single-board computer has 32-bit architecture**

The SBC-20 packs some very powerful 32-bit computing capabilities onto a single STD bus board. Built around a 12-MHz 68020 microprocessor, the board incorporates a 32-bit floating-point processor and 32-bit-wide battery-backed static RAM (128 kbytes, 512 kbytes or 2 Mbytes), both with 32-bit data paths to the processor. The SBC-20 addresses up to 16 Mbytes of memory, supports six levels of bus interrupts and includes one

32-pin JEDEC socket for a boot EPROM or EEPROM (8k×8 bytes to 1M×8 bytes) and a pair of asynchronous communications ports (RS-232 optional) with accompanying software-controlled baud-rate generators. Available with the PDOS operating system or an EPROM-resident PDOS executive, the board draws 1.1 A typical from a 5-V dc-only supply. Prices start at \$764.

**GW Three**

7623 Fullerton Rd  
Springfield, VA 22153

Circle number 134

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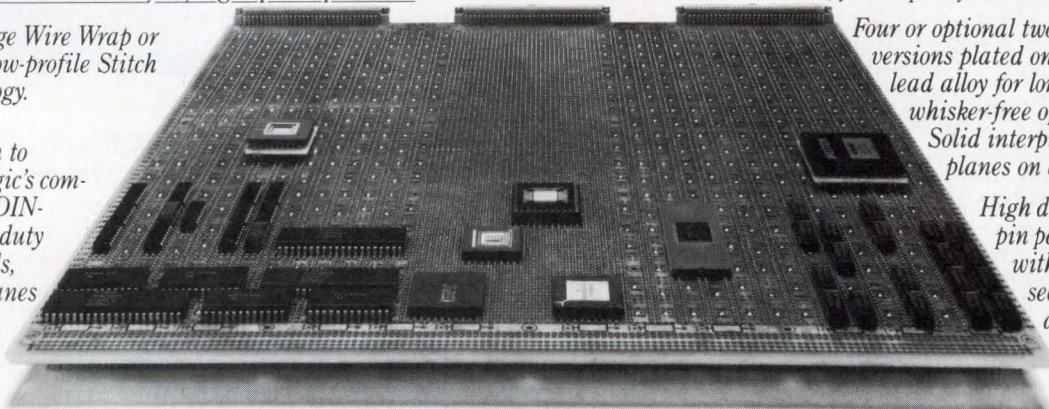
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CIRCLE NO. 26

## INTEGRATED CIRCUITS

### Chip set allows 10-Mbit Ethernet transmission over twisted-pair wiring

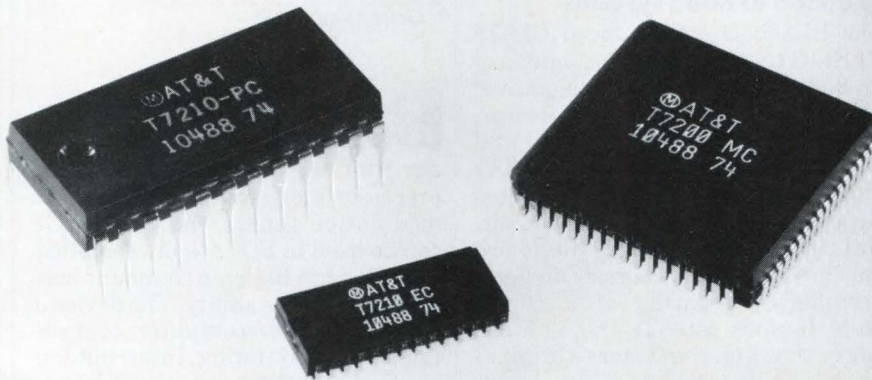
A two-chip CMOS set permits 10-Mbit Ethernet transmission over twisted-pair wiring based on IEEE 802.3 10 BASE.T standards. The T-7210 Manchester Decoder and Inter-

face chip (MDIC) is a VLSI device that provides essential functions for high-speed twisted-pair stations and repeaters in Carrier Sense Multiple Access/Collision Detect LAN applications based on 10-Mbit/s Manchester-coded data format.

The MDIC converts signals for digital transmission, recovers and de-

codes 10-Mbit/s serial Manchester data from the line receiver and produces nonreturn-to-zero data and clock signals for the controller chip. Designed in 1.5-micron linear CMOS technology, the chip is packaged in either a 24-pin dual in-line package or a 28-pin small-outline JEDEC.

The T7200 Multi-Port Repeater Controller (MPR) simplifies the design and implementation of a twisted-pair-compatible multiport repeater for use in 10 BASE.T networks. Used with the MDIC, the repeater unit provides all the functions necessary for the repeater set. The chip is available in a 68-pin plastic leaded chip carrier. In quantities of 10,000, the MDIC is priced at \$25. The MPR is \$100 in 1,000-piece quantities.



#### AT&T Microelectronics

1 Oak Way  
Berkeley Heights, NJ 07922

Circle number 156

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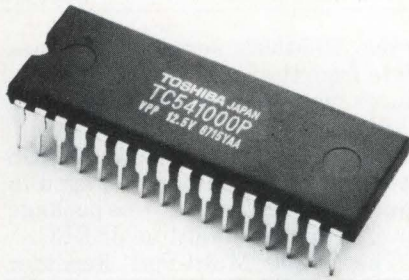
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CIRCLE NO. 27

INTEGRATED CIRCUITS



**One-time programmable ROM has 1-Mbit capacity**

Organized as 128 kwords×8 bits, the TC541000P and TC541001P are one-time programmable ROMs with access times of 200 and 250 ns, respectively. The devices offer standard pin-outs, high-speed programmability and compatibility with automatic insertion equipment. Built using silicon stacked gate MOS technology, the chips dissipate a standard operating current of 30 mA and a stand-by current of 100 mA with an oper-

ating temperature range of -40° to +85° C. In 5,000-piece quantities, the devices cost \$19.50 each.

**Toshiba America**

9775 Toledo Way  
Irvine, CA 92718

Circle number 158

**Custom VLSI chip mates 80386 to 8088 systems**

The EL386 is a high-speed CMOS VLSI IC that converts the signals of an 80386 processor into the equivalent signals of an 8088 processor. Designed to increase the speed and performance of IBM PCs, PC XTs and compatibles, the chip translates data width, control signals and circuit timing. To the 80386, the device appears as a 32-bit memory and/or a peripheral operating at a 16- to 20-MHz clock rate. To the 8-bit circuitry that's on the system's original

mother board, the chip appears as an 8-bit 8088 operating at its own clock rate. The two processor clocks can be completely asynchronous, letting the 80386 run at a full 20 MHz, yet address peripherals designed for 4.77-MHz 8088 data rates. Pricing is \$50 in quantities of 1,000.

**Edsun**

9 Spring St  
Waltham, MA 02154

Circle number 165

**8-bit microcontroller offers increased I/O and interrupts**

An 8-bit microcontroller featuring processor-independent pulse width modulation timers, the COP888CF can be used in I/O-intensive applications due to a high pin count and software processing ability. The device is a complete microcomputer, containing all system timing, interrupt log-



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## INTEGRATED CIRCUITS

ic, ROM, RAM and I/O needed to implement dedicated control functions. Memory-mapped architecture, two 16-bit timer/counters, two power-saving modes and a serial synchronous communications interface are offered, as well as 4,096 bytes of ROM that may hold program instructions or constant data. An analog-to-digital converter supports single-ended and differential modes of operation. Price is \$7.74 in 1,000-piece quantities.

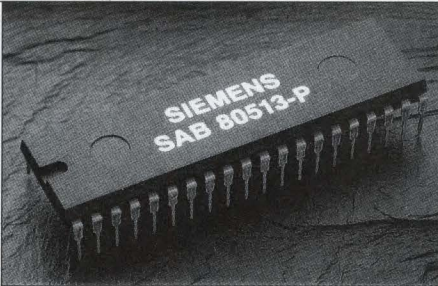
### National Semiconductor

2900 Semiconductor Dr  
Santa Clara, CA 95052

Circle number 161

### Microcontroller hosts programmable ROM

The SAB 80513 is an 8-bit, single-chip microcontroller with a 16-kbyte, on-chip mask-programmable ROM. The device contains 256 bytes of



RAM, four 8-bit ports, a serial channel, an on-chip oscillator, clock circuitry and an interrupt structure with six vectors and two programmable priority levels. The chip is supplied in a 40-pin dual in-line package and a 44-pin plastic leaded chip carrier in both 12- and 16-MHz versions. Prices start at \$4.10.

### Siemens

186 Wood Ave S  
Iselin, NJ 08830

Circle number 163

### CMOS MAC yields 40-ns cycle time

Built with a 1-micron CMOS process, the TMC2208 is an 8 × 8-bit parallel multiplier-accumulator that operates at a 40-ns cycle time (25-MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 16-bit product that may be accumulated to a 19-bit result. Selectable accumulation, subtraction, rounding and accumulator preload as well as single 5-V power supply operation and three-state outputs are features of the TMC2208. The 48-lead ceramic dual in-line package is priced at \$21, while a 48-lead plastic package is available for \$15.

### TRW LSI Products

PO Box 2472  
La Jolla, CA 92038

Circle number 166

our competitors are still in the dark.




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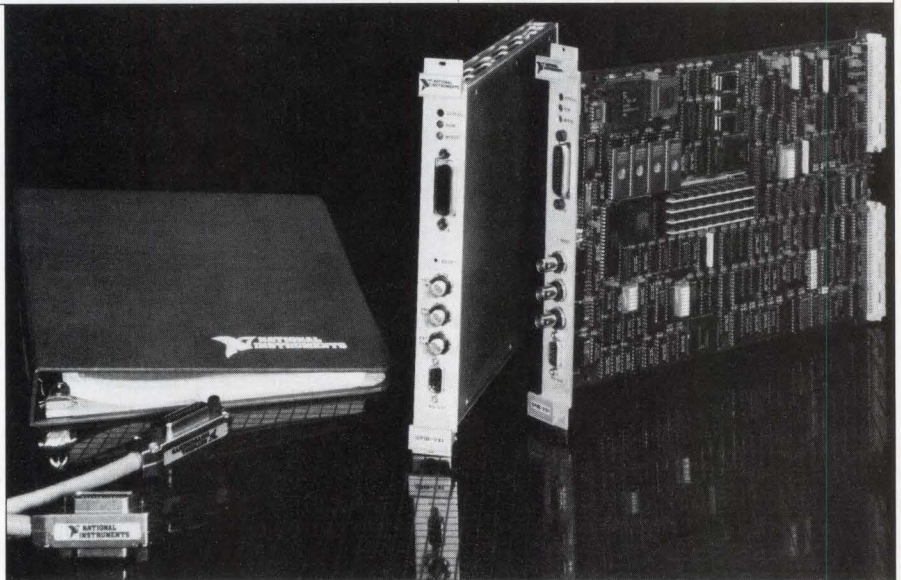
DATA ACQUISITION AND CONTROL

**Interface board links industry-standard IEEE-488 bus to VXIbus**

The GPIB-VXI interface board, which links the industry-standard IEEE-488 bus and the VMEbus Extension for Instrumentation (VXIbus), lets VXIbus instruments be used alongside, or instead of, IEEE-488 instruments.

The interface can be used as the top-level commander in slot 0 of a C-sized VXIbus system. In addition, the board can perform the power-up sequencing and resource management duties that are necessary to configure VXIbus devices within the system. These duties include VXI device identification, address map configuration, system self-test management, configuration of commander/servant hierarchies and initiation of normal operation.

A 68070 microprocessor resides on the device and includes a 68000-compatible 16-/32-bit CPU with a memory management unit (MMU), a two-channel direct memory access controller, a 16-bit timer/counter and an interrupt controller. An I<sup>2</sup>C serial bus interface and a universal asynchronous receiver/transmitter serial

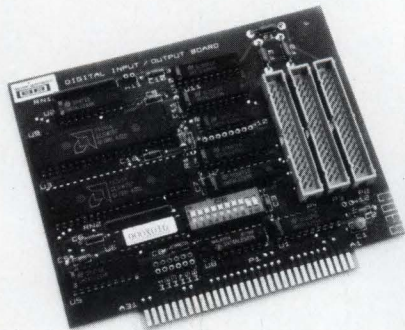


interface are also provided. On-board RAM from 512 kbytes to 4 Mbytes is dual-ported with the VXIbus for shared-memory communication. Optional standard operating firmware stored in EPROM is available.

A private bus is used for high-speed access to local resources, while a separate shared bus lets both the on-board CPU and the VXIbus access the VXI registers. The IEEE-488

interface circuitry on the board consists of a 7210 talker/listener/controller, a Turbo488 custom application-specific IC and additional support circuitry. Prices for the interface board start at \$3,000.

**National Instruments**  
12109 Technology Blvd  
Austin, TX 78727  
**Circle number 137**



**40-channel data-acquisition board comes with software**

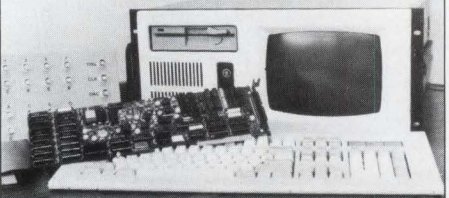
The PCI-20087W-1 data-acquisition board plugs into a one-half or full-sized expansion slot of the IBM Personal System/2 Model 30 as well as any IBM PC, PC XT, PC AT or compatible. The card offers 40 channels of TTL-compatible signals accommodated in five groups of 8 bits each that can be independently software-programmed as either an input or output port. Data transfer on two of

the ports can be synchronized to external hardware events by using the channels in the fifth port as handshake control lines. All ports are initialized as inputs at "power-on." A family of Basic software drivers is included, and the product is compatible with the PCI-20046S and PCI-20047-S series of software drivers, which are available in C or Turbo-Pascal.

**Burr-Brown**  
1141 W Grant Rd  
Tuscon, AZ 85705  
**Circle number 138**

**System acquires data on 16 channels at 1-MHz samples/s**

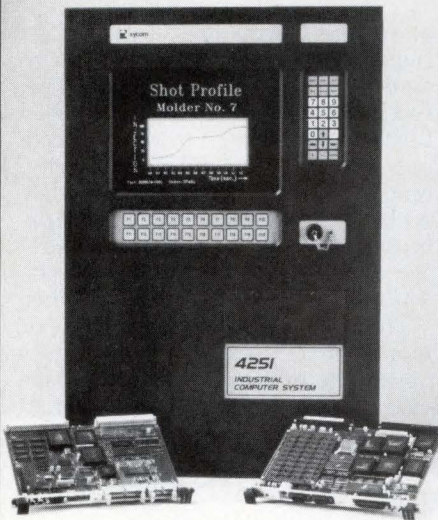
Housed in a rack-mounted chassis with a built-in 9-in. Enhanced Graphics Adapter monitor, the PRX80386M is a turnkey 80386-based data-acquisition and analysis system that can receive data on up to 16 channels at 1-MHz samples/s, with the ability to store up to 90,000 samples/s continu-



ously to disk. The unit is 8.7 in. high and includes a 44-Mbyte hard disk, a 1.2-Mbyte floppy, 2 Mbytes of RAM, eight slots (five empty), and both a serial and a parallel port. A rack-mounting keyboard and a 3½-in.-high keyboard drawer are included, along with menu-driven software and spectrum analysis software for computing the power spectrum of a waveform with a discrete Fourier Transform. The analysis system is priced at \$13,995.

**CyberResearch**  
5 Science Park Ctr  
New Haven, CT 06536  
**Circle number 141**

## DATA ACQUISITION AND CONTROL



### PC-compatible industrial workstation uses VMEbus

Based on a 10-MHz 80286 processor, the 4251 Industrial Workstation features an Enhanced Graphics Adapter/Color Graphics Adapter color monitor; a double-high, 12-slot VMEbus backplane; data entry and function keypads; a hard/floppy disk controller; and an IBM PC XT, PC AT keyboard port. The front panel is sealed to NEMA 4 and 12 standards, and the CRT is protected by an impact-resistant Lexan shield. An optional software package lets the system operate as a multifunction CAD workstation with dynamic operator displays and real-time control software.

#### Xycom

750 N Maple Rd  
Saline, MI 48176

Circle number 139

### Hardware/software package supports OS/2 with IEEE driver

A high-speed, full-function IEEE-488 interface card, the MC-GPIB is a stand-alone, plug-in circuit board that can be installed in any 16-bit Micro Channel slot of the IBM Personal System/2 to monitor, control and communicate with IEEE-488 bus-compatible engineering, scientific or medical instruments. An NEC  $\mu$ PD7210 chip provides the basic IEEE-488 talker, listener and controller functions, while a National

Instruments Turbo488 custom IC increases performance to 1 Mbyte/s. The board features PS/2 programmable option select circuitry for selecting I/O address, interrupt level and direct memory access channel. Letting the interface card use the multitasking capabilities of OS/2, the NI-488 OS/2 binary device software driver, installed as part of the operating system, provides all the required libraries, macros and definitions for C, Basic, Pascal and Fortran in source code. The price for the package is \$595.

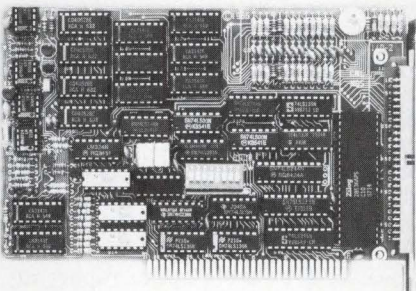
#### National Instruments

12109 Technology Blvd  
Austin, TX 78727

Circle number 144

### Data-acquisition board provides eight analog, 12 digital channels

Designed for measurement and control of voltages, thermocouples, remote data transmitters, pressure sensors and other signals, the Mini-

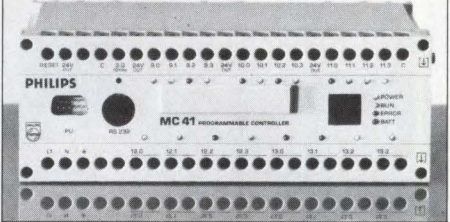


16 data-acquisition and control board combines 16-bit resolution with eight analog and 12 digital I/O channels. Different characteristics such as range, sampling rate and signal conditioning can be set up for each channel. Compatible with IBM Personal System/2 Models 25 and 30 as well as PC XTs and PC ATs or compatibles, the self-calibrating board has six software-selectable ranges from 50 mV to 10 V full scale or autorange and a low-noise integrating converter that can take up to 2,500 samples/s. The price is \$995.

#### Strawberry Tree Computers

160 S Wolfe Rd  
Sunnyvale, CA 94086

Circle number 140



### PLDs feature 10-ms cycle time, 25 I/Os

The MC40 family of programmable logic devices comes with a main power supply, computer-integrated manufacturing capability, a 10-ms cycle time and up to 25 input/outputs, including a 10-kHz counter and four analog inputs. Battery backup is provided for the program memory, as well as a watchdog circuit that switches on a warning LED when the cycle time becomes too long. Two digital multipurpose LED displays included in the extended version of the PLD family can be used to show error codes as well as sequence step numbers.

#### Philips

Bldg HFK, 5600 MD  
Eindhoven, The Netherlands

Circle number 142

### Workstation combines industrial interface with PC software compatibility

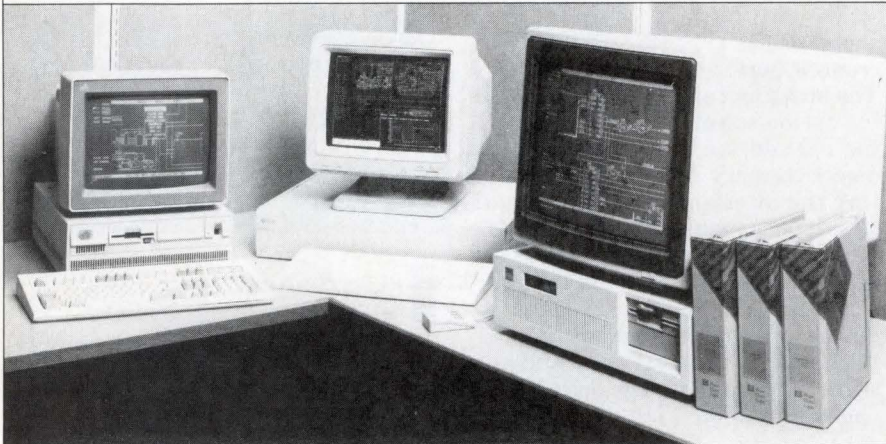
An integrated STD Bus computer with an industrial user interface and personal computer software compatibility, the ZT 1000 System can function as a stand-alone controller or as a node on the manufacturer's industrial Z-NET network. Meeting NEMA 4 and 12 requirements for use in harsh environments, the system features a 12-in. display, and function and numeric keypads. As storage options, it offers RAM/ROM disks, floppy disks, Winchester disks or bubble memory. An NECV20 single-board computer (SBC) powers the IBM PC XT version, while the PC AT model hosts an NECV50 SBC. The base price is \$5,970 with a monochrome display and \$6,440 with an Enhanced Graphics Adapter color monitor.

#### Ziatech

3343 Roberto Ct  
San Luis Obispo, CA 93401

Circle number 143

DESIGN AND DEVELOPMENT TOOLS



**CAE schematic design package runs on Sun workstations**

Designed for use on Sun workstations, the CapFast CF4000 is a CAE schematic design package with a general-purpose symbol and schematic

editor. Plotting and partlist programs, a symbol library and a generic ASCII net-lister for printed circuit board layout are included.

The package is data base compatible with the manufacturer's IBM PC AT and Personal System/2 products,

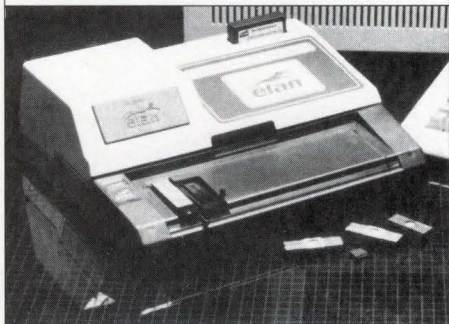
allowing software upgrades as design requirements increase. Features include an intuitive user interface, flexible property editing, unlimited hierarchical levels with multiple pages at any level of the hierarchy, on-line rules checking, continuously scalable text and a split-screen capability. Open data bases and ASCII file formats let users integrate the software with their own applications.

The package works with color or monochrome workstations and offers optional simulator and printed circuit board interfaces, a programmable net-list library, and tools for the development of custom net-listers and back-annotation utilities. Prices start at \$995.

**Phase Three Logic**

PO Box 985  
Hillsboro, OR 97123

Circle number 150



**Flash EPROM programmer connects to PC or PS/2**

The 3000 series range of EPROM, EEPROM and flash EPROM programmers is capable of single, set and gang programming in 8-, 16-, 32- and 64-bit word sizes. The unit features a full range of EPROM coverage from 5-V NMOS and CMOS to all megabit devices. A serial cable links the device to an IBM PC or Personal System/2, while an auto-configurable RS-232 port offers up to 38,400 baud with selectable formats. Programming is controlled from the PC keyboard using menu-driven windows with software supplied on 5¼- or 3½-in. floppy disks. Prices for the series start at \$1,195.

**Elan Digital Systems**

2162B N Main St  
Walnut Creek, CA 94596

Circle number 152

**Evaluator board models 64k primitives**

An evaluator board with the capability to model 65,536 primitives, the 64K features 256 kbits of memory modeling and provides modeling of up to eight logic levels and eight strengths. The number of rise and fall delays has been increased to one per pin, allowing each primitive up to eight delay parameters associated with it (one rising and one falling delay for each of four input pins). With the user-selectable spike reporting feature enabled, all timing violations and spike activity are logged to an error file showing when and where the error occurred.

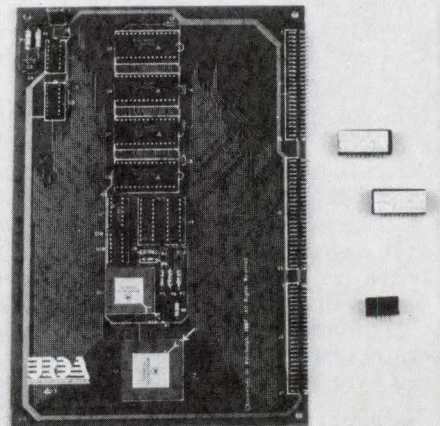
**Ikos Systems**

145 N Wolfe Rd  
Sunnyvale, CA 94086

Circle number 153

**Expansion board houses microprocessor development system**

The P68020  $\mu$ Lab microprocessor development system is an expansion board for use with the  $\mu$ Lab computer. Built around a Motorola 68020 microprocessor, the board offers an optional 68881 floating-point coprocessor, 32 kbytes of static RAM and 8 kbytes of EPROM. The device can



be programmed to learn the object or machine code of the 68020, including addressing modes, instruction types and input/output, as well as evaluate a candidate microprocessor for particular applications. The price for the complete system is \$899.50.

**University Research and Development Associates**

4516 Henry St, Pittsburgh, PA 15213

Circle number 154

**AI software debugs circuit boards**

Applying artificial intelligence software to the problem of debugging

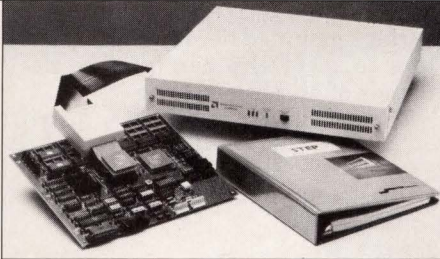
## DESIGN AND DEVELOPMENT TOOLS

populated circuit boards and systems, the Array Analysis Diagnostic Expert System "tells" operators how to debug systems through a series of prompts. The expert system generator learns to recognize fault conditions in digital or analog systems and creates a fault directory from either simulated or normal testing failures. Analog and digital test vectors, reference data and tolerance guard bands are all stored in a graphics format, eliminating language-specified timing requirements. Macro control sequences can be created by executing a test sequence manually and storing the operations on the disk. The package costs \$1,985. Test systems with the Diagnostic Expert System start at \$6,669.

### Array Analysis

200 Langmuir Lab, Brown Rd  
Ithaca, NY 14850

Circle number 155



### RISC development tool provides real-time debug facilities

A stand-alone system that offers a software test bed and hardware debug facilities for real-time operation, the Adapt29K is a development and prototyping tool for the Am29000 reduced-instruction-set processor. The ROM resident software lets the user set eight breakpoints, display memory and registers, display captured bus activity, read and write I/O ports and download files. A 4,096 entry-deep trace buffer is provided

that captures bus signals at speeds of up to 40 MHz. High-level language debuggers executing on host computers such as personal computers, workstations and VAXes can be supported, while files from remote software development stations can be downloaded through a serial link. The package is priced at \$8,500.

### Step Engineering

661 E Arques Ave  
Sunnyvale, CA 94086

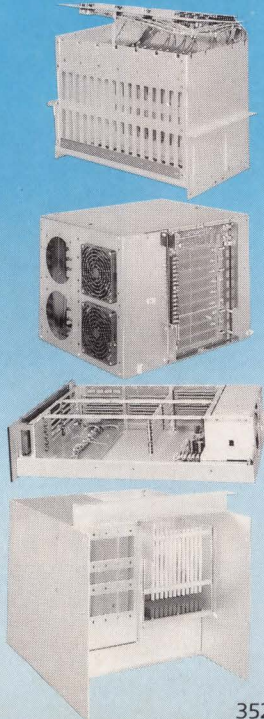
Circle number 151

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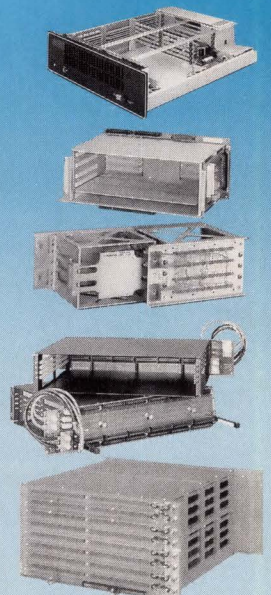


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CIRCLE NO. 29

■ NEW PRODUCT HIGHLIGHTS

MAJOR SYSTEM COMPONENTS

**Four-layer wire-wrap panels boost component density**

A series of wire-wrap panels combines a four-layer construction with

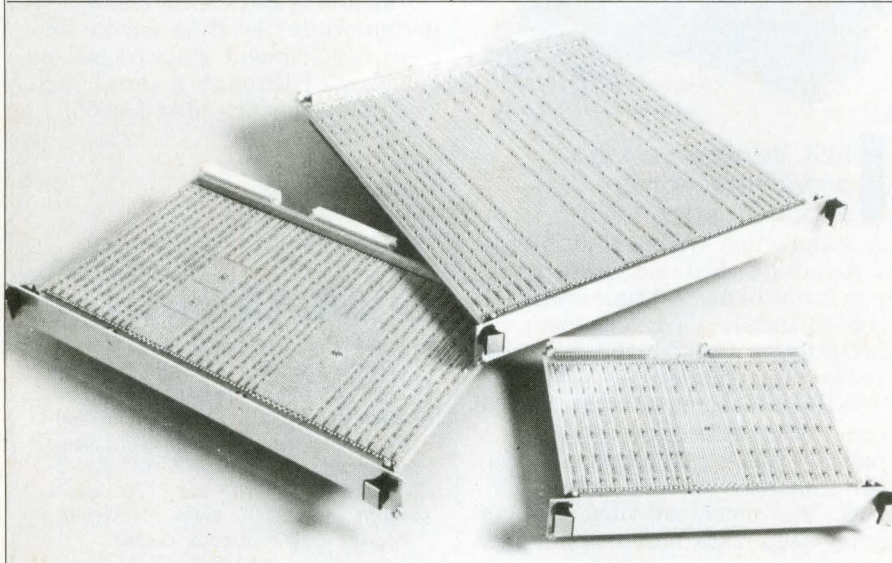
surface-mounted decoupling capacitors to meet the performance demands of high-speed logic.

The panels maximize power distri-

bution by committing two layers to  $V_{cc}$  and two layers to ground. For designs using high-power, pin-grid-array (PGA) components, a lattice network configuration of power and ground planes gives engineers the option of making low-inductance power connections to critical devices with solder washers.

By placing surface-mounted decoupling capacitors underneath the active components, engineers using the panels can place devices anywhere on the board without reserving board real estate for through-hole decoupling capacitors. This feature can increase component density by 40 percent.

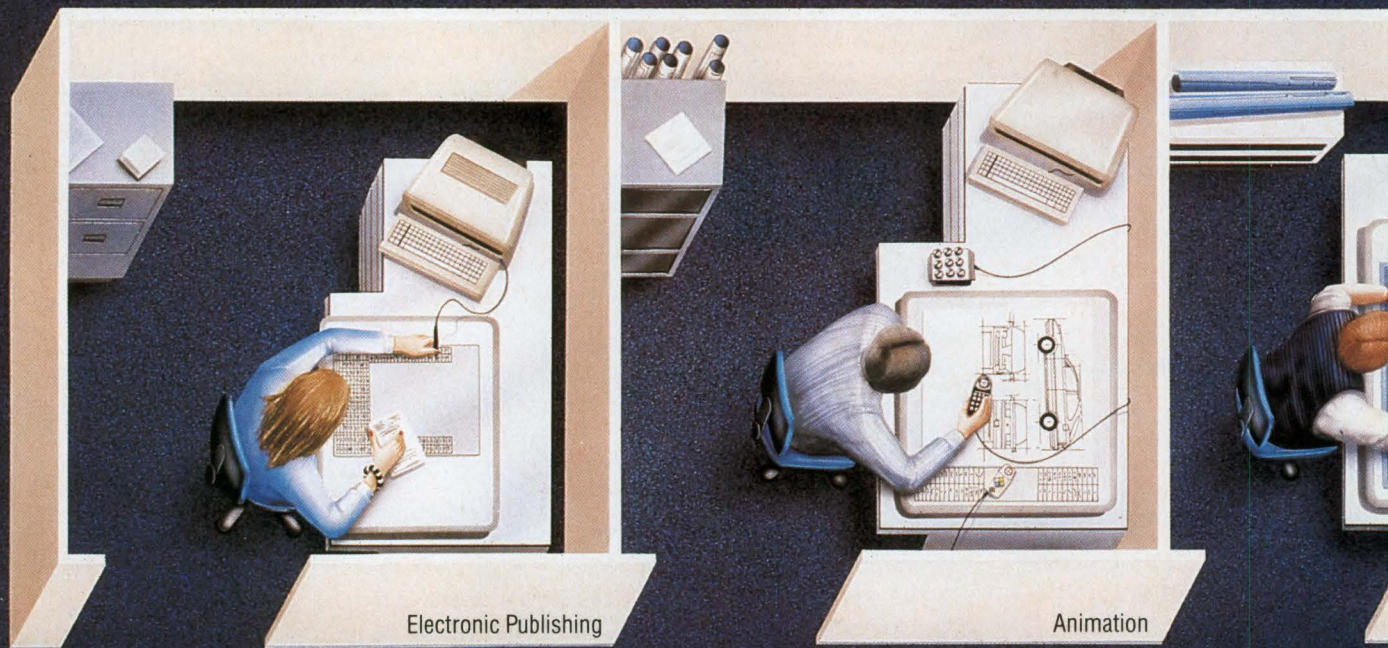
VMEbus or uncommitted DIN panels have depths from 160 to 400 mm.



**Augat**

33 Perry Ave, PO Box 779  
Attleboro, MA 02703

Circle number 171



Electronic Publishing

Animation

# Microgrid® II. A solution

Why are more people specifying Microgrid II Series tablets for their applications? Simple. It's the best value. The Microgrid II Series is competi-

tively priced, yet it comes with several standard features (like a universal power supply and dual RS232 interface) that cost over \$1,000 with other tablets.

Microgrid is compatible with the world's largest base of installed systems, so it can easily fit into most new or existing workstation requirements. You also

## MAJOR SYSTEM COMPONENTS



### Hybrid 18-bit D-A converter offers high accuracy

The AD1139 digital-to-analog converter requires no user adjustments to achieve 18-bit accuracy with guaranteed  $\pm\frac{1}{2}$  least significant bit (LSB) maximum differential and integral nonlinearity. Voltage output ranges are 0 to 5, 0 to 10, and  $\pm 5$  to  $\pm 10$  V. Current outputs of  $-1$  mA and  $\pm 0.5$  mA are also selectable. A single LSB settles in  $6 \mu\text{s}$ , and full-scale settling time is  $40 \mu\text{s}$ , both measured to 0.00019 percent. The device requires  $+5$ - and  $\pm 15$ -V supplies and typically consumes 825 mW. It's available in a 32-pin triple-wide dual in-line package. The  $\pm\frac{1}{2}$  LSB D-A

converter costs \$295 in quantities of 100; a  $\pm 1$  LSB version is \$195.

#### Analog Devices

One Technology Way, PO Box 9106  
Norwood, MA 02062

Circle number 172

### Switching power supply has harmonic resonance design

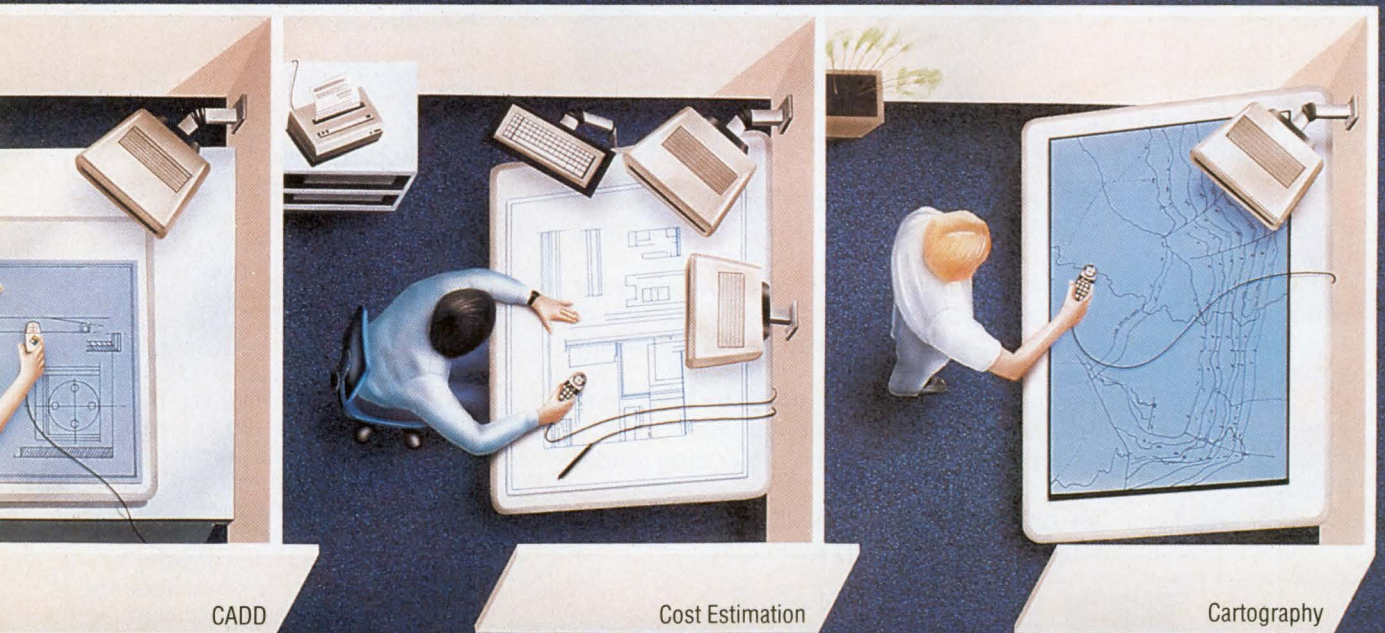
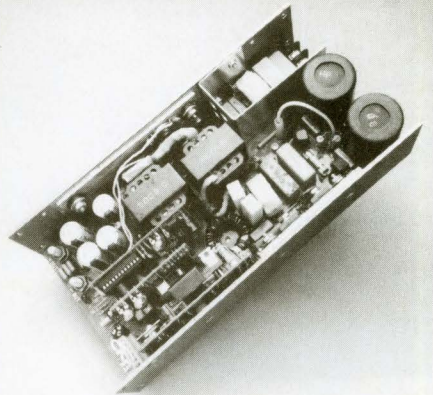
Achieving power densities of up to  $3.2 \text{ W/in.}^3$ , the 9S Series of switching power supplies uses harmonic resonance technology for low-noise, high-power output. The half-bridge, 200-kHz supplies use standard pulse-width modulation techniques to produce outputs of 300 or 400 W, while producing ripple and noise of only 25 mV peak to peak. Both units in the series accept worldwide ac voltage input ranges, offer outputs of 5, 12, 15 or 24 V dc, and incorporate overload, short circuit, overvoltage, reverse

polarity and overtemperature protection features. Prices for the switching power supplies start at \$240 in quantities of 500 or more.

#### Valor Electronics

6275 Nancy Ridge Dr  
San Diego, CA 92121

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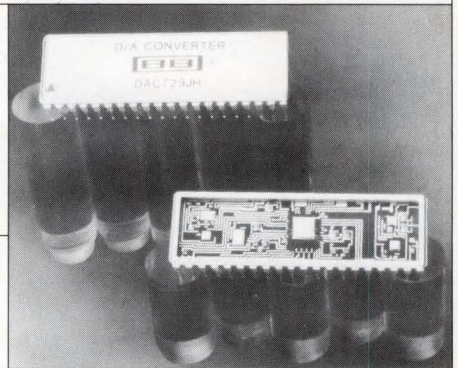
CIRCLE NO. 30

MAJOR SYSTEM COMPONENTS

**D-A converter offers 18-bit accuracy**

Initially designed as a programmable ATE reference, the DAC729 18-bit digital-to-analog converter is also applicable to a broad range of preci-

sion controller, digital audio and precision waveform generator applications. A thin-film monolithic 20-V process, a dielectrically isolated op amp process, and advanced laser-trimming and test techniques deliver



a guaranteed linearity of 16 bits. The D-A converter is user-adjustable to 18-bit linearity. As a complete device, it includes a low-drift +10-V reference and a low-drift, low-noise output amplifier. Gain drift is limited to  $\pm 5$  ppm/ $^{\circ}$  C, while offset drift typically reaches  $\pm 2$  ppm of full-scale range/ $^{\circ}$  C. Prices start at \$141 in quantity. The device settles to  $\pm 0.00076$  percent FSR in 8  $\mu$ s for a full-scale voltage step. Internal feedback resistors are absolute-value trimmed to  $\pm 0.1$  percent, permitting easy scaling of modified ranges, such as 10.24 V, with small external resistors.

**Burr-Brown**

PO Box 11400  
Tucson, AZ 85734

Circle number 174

**Triple-output switchers target telecomm applications**

With power densities of up to 3.5 W/in.<sup>3</sup>, the MTC series of triple-output switching power supplies ranges from 160 to 500 W. The switchers provide up to 60 A of +5 V for logic and memory. All outputs are fully regulated to deliver  $\pm 1$  percent combined line and load regulation. Typical efficiency is 80 percent. Intended for telecommunications applications, the high-current (10 A)  $\pm 12$ -V regulated auxiliary outputs provide regulation characteristics for line drivers, RS-232 and popular network interfaces. The switchers are packaged in an open-frame configuration designed to transfer heat energy to the outside frame.

**Todd Products**

50 Emjay Blvd  
Brentwood, NY 11717

Circle number 176



**2.5 Gigabytes Unattended Backup**

Digi-Data's GIGASTORE™ provides 2.5 Gigabytes of data storage on a single T-120 VHS video cartridge. That permits backup of your largest disk drive on off-hours without an operator.

Utilizing true read-after-write coupled with very powerful error correction, GIGASTORE gives you an unsurpassed error rate of 1 in 10<sup>23</sup> bits. In addition, you get a high speed search capability not available in most 9-track drives.

GIGASTORE can be provided with an interface for DEC computers, such as VAX and Micro Vax, for operation under VMS. It is also available with an IBM PC interface, operating under MS/DOS.

Call Digi-Data, an organization with a 25 year history of manufacturing quality tape drives, at (301) 498-0200.

™GIGASTORE is a trademark of Digi-Data Corporation.



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England SL6 4DP • Telephone No. 0628 2955/6 • Telex 847720

CIRCLE NO. 31



## MAJOR SYSTEM COMPONENTS

### VME card cage controls airflow

The 10-slot, Phase III Optional Mount Card Cage Assembly uses an Air-Deflecting System (ADS) to direct airflow to hot spots on daughter boards and backplanes normally blocked off by card guides and extrusions. The ADS consists of deflector strips, contoured extrusions and molded wedge-shaped card guides. Applicable to any of the manufacturer's Phase III VME card cages and backplane assemblies, the system can also be incorporated into Sun-compatible 9U×400-mm card-cage assemblies.

#### Hybricon

12 Willow Rd  
Ayer, MA 01432

Circle number 173

### Tracking ball incorporates mouse functions

Designed to replace mouse-type input devices on personal computers and minicomputers, the Mouse-Trak achieves cursor movement via a 2-in. phenolic ball. Three user-defined input keys control momentary or sustained cursor movement, while a fourth key increases or decreases movement ratio by 4:1. The device is powered from the RS-232 interface on the host computer, eliminating the need for an additional power supply. Two standard versions will emulate Microsoft Mouse and Mouse Systems PC Mouse, while three quadra-



ture versions allow operations with systems from Atari, Apple, Sun, Apollo, DEC, Cadnetix and Tektronix. Prices start at \$119.

#### Itac Systems

3121 Benton Dr  
Garland, TX 75042

Circle number 177

### 40-W switching power supplies offer high density

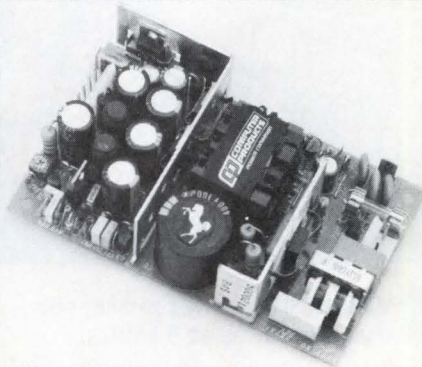
Accepting any input voltage from 85 to 264 V ac without the need for jumper wires or a switch, the NFS40 series of 40-W switching power supplies regulates down to zero output load. The universal input switches are packaged in a low-profile, 5×3×1.2-in. open-board, creating a power density of 2.2 W/in.<sup>3</sup>. Line regulation is ±0.5 percent max, and typical efficiency is 70 percent. Approved by Underwriters Labora-

tories, Canadian Standards Association and Veband Deutscher Elektrotechniker, the power supplies boast a mean time between failures of 160,000 hr. Unit prices for the power supplies start at \$59.

#### Computer Products

2900 Gateway Dr  
Pompano Beach, FL 33069

Circle number 175



The Electron Beam Technology Division of Perkin-Elmer, the industry leader in state-of-the-art electron beam lithography systems, has the following immediate opening:

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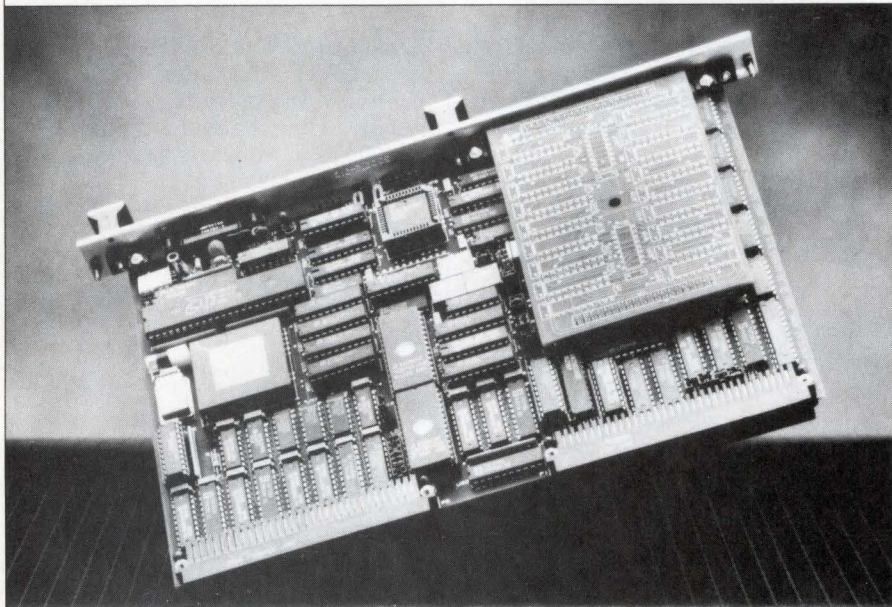
We require an MS or PhD in Electrical Engineering, Computer Science or related field. You must display a working knowledge of pattern manipulation algorithms as well as hardware and software engineering principles. This is a high visibility, cross-disciplinary effort, requiring impeccable communication skills.

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# PERKIN-ELMER

DATA COMMUNICATIONS



the data, processes network protocols, manages the local bus and supervises all data transfers across the VMEbus.

A full 32-bit address and data path accommodates the 68020, while 512 kbytes of on-board dynamic RAM hold processing protocol and data buffers. The device appears to the host system as a region of memory, and communication between the two is handled by standard I/O drivers.

The board is compatible with the IEEE VMEbus version C.1, Ethernet 1.0 and 2.0, and IEEE 802.3 specifications. The manufacturer's Transmission Control Protocol/Internet Protocol software suite is also supported. An optional configuration offers a 20-MHz 68020 microprocessor and 2 Mbytes of RAM. Prices start at \$3,595.

**VMEbus Ethernet processor transfers files at 3 Mbits/s**

Boasting memory-to-memory file-transfer rates in excess of 3 Mbits/s,

the ENP-100 is an intelligent, single-board interface between VMEbus host systems and Ethernet. A 12.5-MHz MC68020 microprocessor moves

**Communication Machinery**

125 Cremona Dr  
Santa Barbara, CA 93117

Circle number 145

**Integrated PC card connects to Ethernet**

The HP StarLAN 10 family of LAN products includes an integrated personal computer card that allows the connection of PCs and minicomputers using standard telephone wiring. The card provides a direct connection to the twisted-pair wire via an eight-pin modular jack used for telephone connections and eliminates the need for an external medium attachment unit. PCs can be located 100 m from the manufacturer's hub unit with data sent at 10 Mbits/s over the IEEE 802.3/Ethernet LAN backbone. The board is priced at \$695.

of asynchronous, byte-synchronous and bit-synchronous formats. For asynchronous links, the board provides a programmable baud rate selection from 3 to 76,800 baud, while baud rates for synchronous operation run from 38 to 307,200 baud. Each full-duplex channel, configurable for either RS-232 or RS-485/-422 operation, has its own first-in, first-out receive buffers and an automatic spike rejection mechanism.

and automatic speed matching to remote modems are featured, with two RJ11C phone jacks provided. Prices start at \$549.

**U.S. Robotics**

8100 N McCormick Rd  
Skokie, IL 60076

Circle number 148

**Hewlett-Packard**

19310 Pruneridge Ave  
Cupertino, CA 95014

Circle number 146

**Communications controller gives PCs serial I/O**

Built around the 82530 communications controller IC, the PCOM-1 board gives an IBM PC-compatible computer two independent channels of high-speed serial I/O with a choice

**Rapid Research**

Southern House, Burwash Rd, Broad Oak  
E Sussex, UK, TN21 8TB

Circle number 147

**PC modem card delivers 4.8 kbits/s**

By means of an on-board data compression algorithm, the 2.4-kbit/s Courier 2400/PC modem board can deliver up to 4.8-kbit/s transmissions over voice-grade telephone lines. Complying with the AT modem command set and CCITT V.22 bis, Bell 212A and Bell 103 modem conventions, this auto-answer/-dial modem fits any slot in an IBM PC, PC XT, PC AT or Personal System/2 (Model 25 or 30). Help screens, call reporting

**PC communications board mixes multiple functions**

Combining a synchronous modem, an asynchronous modem and a Synchronous Data Link Control adapter onto a single add-in board for IBM PC and Personal System/2 family computers, the AdaptModem V.22 bis supports PC-to-PC, PC-to-mini and PC-to-mainframe communications using the CCITT V.22 bis standard. Using the standard AT modem command set, the auto-answer/-dial board runs at up to 2,400 baud, synchronous or asynchronous. The price of the board, which features full-duplex operation, is \$575.

**Network Software Associates**

22982 Mill Creek  
Laguna Hills, CA 92653

Circle number 149

## PRODUCT BRIEFS

### 3½-in. drive controller

The PCT-MF20 controller card fits any PC/XT/AT short 8-bit bus slot and allows data interchange between 5¼- and 3½-in. floppy drives. \$489.

**Practical Computer Technologies** *Circle 179*

### Real-time Unix OS

LynxOS is a Unix-compatible, real-time operating system with a predictable response of 350 µs on a 16-MHz, 3-Mips 80386 CPU. \$65,000.

**Lynx** *Circle 180*

### RISC-oriented compilers

The Interact series of C, Fortran and Pascal compilers and macroassemblers suits Intel's 80960 RISC processor. Starts at \$5,000.

**Interact** *Circle 181*

### Logic assembler for PCs

The Avocet PLD is a logic assembler for 256-kbyte, MS-PC-DOS-equipped IBM PCs and compatibles. \$295.

**Avocet Systems** *Circle 182*

### QuickC math toolbox

The C Math Toolbox provides 89 math functions for Microsoft Quick C and C optimizing compilers. \$89.

**Silver State Software** *Circle 183*

### Real-time OS

The BSO/RC is a real-time operating system for 16- and 32-bit microprocessors made by Intel, Motorola or National Semiconductor. Starts at \$6,300.

**BSO** *Circle 184*

### TFEL display driver

The HV08 24-channel, thin-film EL display driver for commercial or military use provides 16 shades of gray using 5-V logic. \$9.96.

**Supertex** *Circle 187*

### Ada compiler for OS/2

The Alsys Ada compiler runs on 286- or 386-based OS/2 systems with at least 2 Mbytes of memory.

**Alsys** *Circle 188*

### 19.2-kbit/s modem

The M1928LFT is a 19.2-kbit/s fault-tolerant, leased-line modem. It analyzes the phone line, detecting impairments based on signal-to-noise ratio, carrier detect and signal quality.

**Fujitsu** *Circle 193*

### 256 × 9 CMOS FIFO

The IDTT7200 256-×9-bit CMOS FIFO features three flag inputs and 25-ns access time in 300-mil THIN-DIP package. \$50.90.

**Integrated Device Technology** *Circle 185*

### XT chip, AT chip set

The ACC 1000 is a single-chip XT-compatible peripheral controller. The ACC 82000 AT-compatible chip set supports 16-MHz systems. \$20 and \$70, respectively.

**ACC Microelectronics** *Circle 186*

### Internal modem for Mac II

Mac Modem II is a Hayes-compatible, internal 2,400-baud modem for the Macintosh II.

**Holmes Microsystems** *Circle 197*

### PCB development system for PS/2

The One Chip Plus add-in board development system allows designs for

Micro Channel architecture, PS/2 systems. Starts at \$495.

**Capital Equipment** *Circle 189*

### Real-time system tools

The Integration Toolkit assists in building, testing and debugging board-level, real-time uniprocessor and multiprocessor systems.

**Multiprocessor Toolsmiths** *Circle 190*

### Enhanced LAN analyzer package

The HP 4972A LAN protocol analyzer adds enhanced testing flexibility to multivendor LAN troubleshooting. \$17,000.

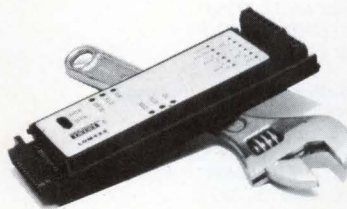
**Hewlett-Packard** *Circle 191*

### Hayes-compatible modem controller

The SC11017 1,200-bit/s, Hayes-compatible modem controller suits 20-MHz turbo speed applications. Starts at \$10.85.

**Sierra Semiconductor** *Circle 194*

## INDUSTRIAL-GRADE DATA COMMUNICATIONS MODEMS



**When you need Ruggedness,  
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For complete details, and a copy of our new 12-page Industrial Modem Brochure, contact your Burr-Brown sales representative.

## PRODUCT BRIEFS

**2,400-bit/s modem for Toshiba CPU**  
The Multimodem224TL operates at 2,400, 1,200 and 300 bits/s in Toshiba laptop computers. \$499.

**Multi-Tech** **Circle 192**

**Development package for TI DSP**  
The 320/PC-17 daughter board provides a development system for TI TMS320C17 DSP. \$895.

**Atlanta Signal Processors** **Circle 195**

**NEC development tools**  
Intertools software lets code be written in C for NEC V20-50 and V60 microprocessors. Starts at \$1,000.

**Intermetrics** **Circle 196**

**Ethernet controller for PS/2**  
The LAN Workplace family of intelligent 512-kbyte boards provides Ethernet interface to PS/2 and PC ATs. \$995.

**Excelan** **Circle 198**

**VMEbus board links X.213 to OSI**  
The CC-125 VMEbus X.25 board implements the X.213 specification for connecting to OSI's Layer 4.

**Compcontrol** **Circle 199**

**C cross compiler**  
Introl-C supports both C and assembly language development for embedded microprocessor applications.

**Introl** **Circle 200**

**110-W universal input switchers**  
The NFS110 series of single- and quad-output, 110-W universal input switching power supplies accepts input voltages from 85 to 264 V ac. Starts at \$141.

**Computer Products** **Circle 201**

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## CALENDAR

### CONFERENCES

**Sept 12-15 and Sept 14-15  
CAD/CAM and Manufacturing  
Automation Conferences**

Hyatt Regency Monterey, Monterey, CA. Separate conferences will be devoted, respectively, to CAD/CAM strategies for the 1990s and global competitiveness in manufacturing automation, with speakers from the host research organization and several industrial organizations.

Information: Lois Long, Dataquest, 1290 Ridder Park Dr, San Jose, CA 95131, (408) 437-8309. **Circle 118**

**ADC '88** Sept 20-22  
**Aerospace  
and Defense  
Computing '88**

Airport Hilton Hotel, Los Angeles, CA. Conference and exhibition will focus on artificial intelligence and neural networks, CAD/CAM, ruggedized and fault-tolerant systems, workstations, graphics and imaging, and operating systems. Also, open forum for DOD and NASA-related issues.

Information: Norm De Nardi Enterprises, 289 S San Antonio Rd, 223-204, Los Altos, CA 94022, (415) 941-8440. **Circle 119**

**Oct 3-5  
IEEE International  
Conference on Computer Design**

Rye Town Hilton, Port Chester, NY. Focus of this conference will be on the design and use of VLSI in computers and processors, with particular emphasis on interactions among system, logic circuit, memory and physical designs; architecture; software; CAD; testing; and VLSI technology.

Information: Michael R. Wayne, IBM, Box 390 D/B34 B/901-3, Poughkeepsie, NY 12602, (914) 432-5211. **Circle 120**

**Oct 3-6  
Electronic Imaging '88**

World Trade Center, Boston, MA. Presenters of papers at this conference will discuss advances in the technical state-of-the-art or unique applications for electronic imaging components and devices in imaging systems and products.

Information: Richard Murray, Institute for Graphic Communication,

375 Commonwealth Ave, Boston, MA 02115, (617) 267-9425. **Circle 121**



**Oct 4-6  
Buscon/88-East**

Javits Convention Center, New York, NY. Specifically targeted at system backplane and integration issues, sessions at this conference will stress board design and integration; and matching bus, microprocessor and peripheral-chip performances to various boards, operating systems and real-time software.

Information: Buscon/88-East, Dave Caplin, Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06854, (203) 838-3710. **Circle 122**

**Oct 4-6  
Northcon/88**

Seattle Center Coliseum, Seattle, WA. Electronics exposition aimed at the interests of companies and design engineers in the Northwest will feature sessions on semiconductors, surface-mount technology and components, with particular emphasis on computer-integrated manufacturing.

Information: Alexis Razevich, Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (213) 772-2965. **Circle 123**

### SEMINARS

**September 12-16  
Open System Interconnection**

Key Bridge Marriott, Arlington, VA. Week of professional courses will concentrate on the advancing standards technology for distributed information and the impact of the OSI reference model and networking protocols at various levels of the model.

Information: The Omnicom Institute, 115 Park St, SE, Vienna, VA 22180, (703) 281-1135. **Circle 125**

**September  
Graphics and Imaging**

Techmart, Santa Clara, CA. Three individual seminars on different dates cover Image Engineering: The Technologies and Applications of Contemporary Image Processing; Visualization Techniques in the Physical Sciences; and Hierarchical

Data Structures for Computer Graphics, Image Processing and Geographic Information.

Information: Karin Polken, University of California Extension at Santa Cruz, Santa Cruz, CA 95064, (408) 429-4535. **Circle 126**

**September  
Data Communications**

Various locations and dates. Series of two- and three-day seminars on IBM PC and IBM Personal System/2 networking, data communications fundamentals, data communications applications, SNA connectivity and SNA optimizing include discussions of network products from several different companies.

Information: Barbara Stern, Center for Advanced Professional Education, 1820 E Garry St, Suite 110, Santa Ana, CA 92705, (714) 261-0240. **Circle 127**



**September-  
November  
Systems  
Engineering for  
Hardware/  
Software  
Applications**

Various locations and dates. Course provides working knowledge of interdisciplinary techniques needed to develop and integrate hardware and software systems for both large and small designs.

Information: Leslie Roebuck, Integrated Computer Systems, 5800 Hannum Ave, PO Box 3614, Culver City, CA 90231, (213) 421-8166. **Circle 128**

**Programs and dates  
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Computer Design can include a calendar announcement of your upcoming conference or seminar as long as it's received at least three months prior to the date of the event. Be sure to include a specific location, a description of the conference/seminar content, and a contact name, address and telephone number.

# ASIC design tools zero in on testability

Art DeSena  
President, ADS Associates



**A**s the need for implementing design-for-testability (DFT) increases, manufacturers of application-specific ICs and complex circuit board assemblies are struggling to find the most cost-effective way to include DFT techniques in their designs. To help in this task, most ASIC vendors are enhancing their design tools so that customers can include and verify DFT circuitry.

The types of tools being developed and regularly updated by ASIC vendors address such areas as fault simulation, DFT design techniques, DFT analysis criteria and automatic generation of test vectors. Although these tools are currently being developed for ASIC design and testing, they will eventually be modified and incorporated into board and system designs where appropriate.

One vendor moving in this direction is Silc Technologies (Burlington, MA), which introduced in May a logic-synthesis-based electronic design automation (EDA) system for ASICs that runs on both Apollo Computer workstations and VAX computers. Called Silcsyn, this new design-synthesis system provides library independence and ensures correctness of the design. It also guarantees testability through the use of a register-transfer-scan algorithm.

"Register transfer scan is a methodology that analyzes the design to determine which flip-flops are appropriate to be implemented in full serial scan registers and then implements them," says Jeffrey R. Fox, vice-president of engineering at Silc Technologies. "Additional control circuitry is automatically added to the other flip-flops that aren't appropriate for full serial scan. This added control circuitry guarantees testability without having to implement these flip-flops for full serial scan." Silcsyn can also generate test patterns required for production tests of the ASICs.

Silcsyn has been in use at beta sites for several months and is now available for about \$40,000.

## Integrating fault and logic simulation

Most designers of VLSI components and boards use a technique called fault simulation to grade the effectiveness of the test patterns to be used for design verification and/or production testing. In this technique, test patterns are applied to simulated faults in the system design. The designer then reviews the test-pattern output to determine what percentage of simulated faults was detected. The resulting percent-

age is known as fault coverage.

Generally, after functional simulation has determined that a design is functioning correctly, designers perform a fault simulation. The functional simulation results are then used as a benchmark against which the the fault simulation is compared.

This technique is rapidly gaining popularity. Technology Research Group (Boston, MA) predicts dramatic growth for fault simulation—a jump from 8,400 digital simulators in 1987 to 96,000 by 1990.

Gateway Design Automation (Westford, MA) has integrated fault simulation with logic simulation with

its introduction in May of the Verifault-XL fault simulator. Fully integrated with the company's Verilog-XL logic simulator, Verifault-XL incorporates Gateway's Verilog mixed-level hardware description language and its XL software algorithm, which provides significant speed advantages on standard hardware platforms. Verifault-XL, Gateway's second-generation fault simulator, surpasses its predecessor,

Testgrade, in both performance and functionality.

Verifault-XL addresses the three major barriers to the widespread adoption of fault simulation—cost, run time and integration with logic simulation. "Product quality and reliability are becoming crucial factors to our customers in the ASIC business and are make-or-break factors for defense suppliers," says Prabhu Goel, president and founder of Gateway. "Increasingly, the availability of integrated fault simulation is affecting the purchase of logic simulation."

## Variety of fault-simulation techniques

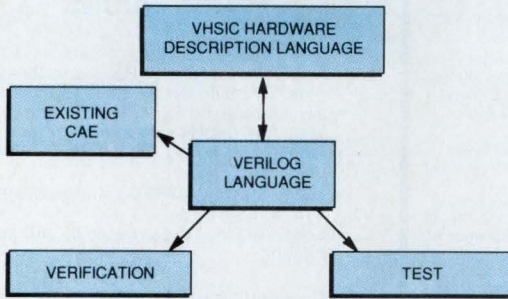
Verifault-XL includes a number of basic fault-simulation features, such as simulation of gate- and switch-level primitives, fault collapsing, incremental simulation and an output fault dictionary. Fault collapsing cuts simulation run times by identifying equivalent faults and collapsing them together. (When 100 faults are collapsed to 70, for example, simulation on 70 percent of all faults provides accurate results for the whole set.) Incremental simulation lets the user interrupt the fault simulation at any point and still be able to restart directly from the interrupt point without any loss of data. The output

**"Product quality and reliability are becoming crucial factors to our customers in the ASIC business and are make-or-break factors for defense suppliers."**

—Prabhu Goel  
Gateway Design Automation



## THE VERILOG SUITE



*By integrating fault simulation with logic simulation, Gateway Design Automation breaks what has been one of the barriers to widespread acceptance of fault simulation. Fully integrated with Gateway's Verilog-XL logic simulator, the Verifault-XL fault simulator incorporates Gateway's Verilog mixed-level hardware description language and its XL software algorithm.*

fault dictionary provides cross-reference information for diagnosing simulation results and contains the expected result for each simulated fault.

In addition, Verifault-XL can perform various types of fault simulation. Its concurrent fault-simulation capability lets Verifault-XL simulate multiple faults concurrently by simulating only those gates in the logic to which the effects of each fault are propagated. Distributed fault simulation divides the fault models among a number of workstations and then runs the fault simulations simultaneously. The run-time speed increase is directly proportional to the number of workstations used. Behavioral propagation is the ability to pass faults through behavioral models, which is quicker than fault passage through switch models. This is especially useful in situations where early test generation is required, or where gate-level models aren't available.

### ■ The Verilog language and XL algorithm

Ranging from the architectural/behavioral to the gate/switch techniques, the Verilog hardware description language lets CAE users design and simulate systems using a top-down methodology. Top-down design speeds the verification process since portions of a design can be modeled behaviorally and then verified prior to gate-level implementation. This reduces the number of iterations and often results in a first-time-right design.

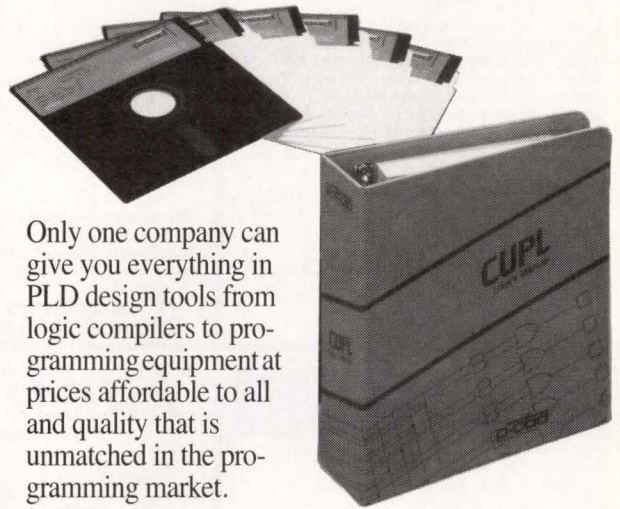
The XL software algorithm increases simulation speeds through an adaptive-behavior-recognition technique, which is an advanced form of clock suppression. By incorporating the XL algorithm, the Verifault simulator can run from three to 12 times faster than Gateway's Testgrade.

Verifault-XL is sold in conjunction with the Verilog-XL simulator. Prices start at \$30,000 for existing Verilog-XL users. Verifault-XL runs on a variety of standard platforms, including those from IBM, Digital Equipment Corp, Sun Microsystems and Apollo, with the distributed fault simulation supported on Sun and Apollo only. ■

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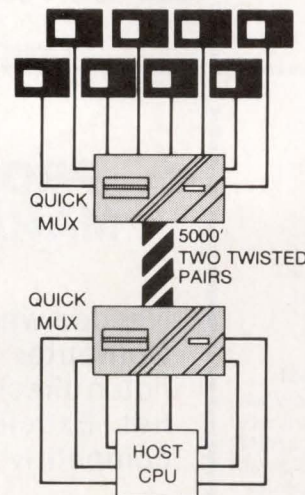
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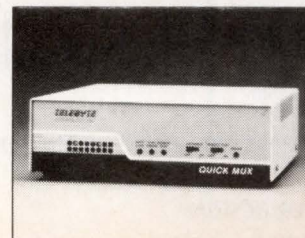
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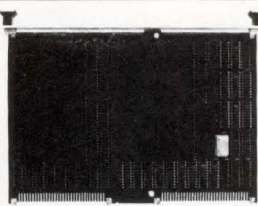


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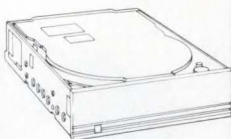
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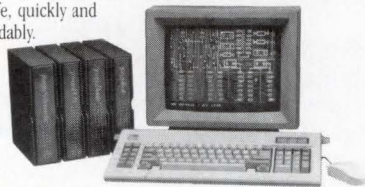


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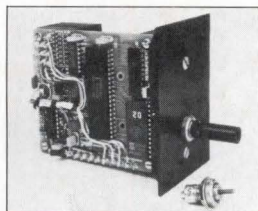
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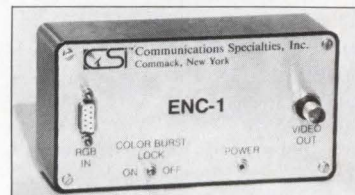
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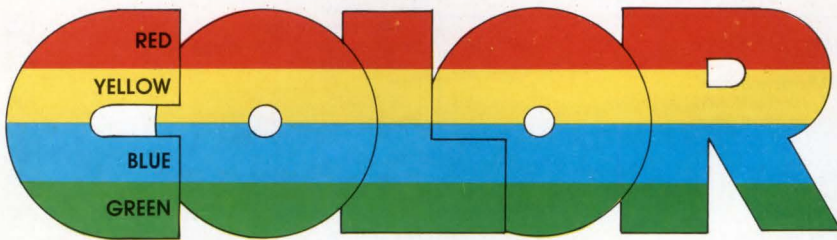
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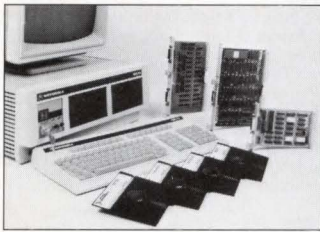
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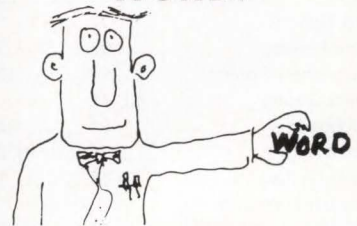
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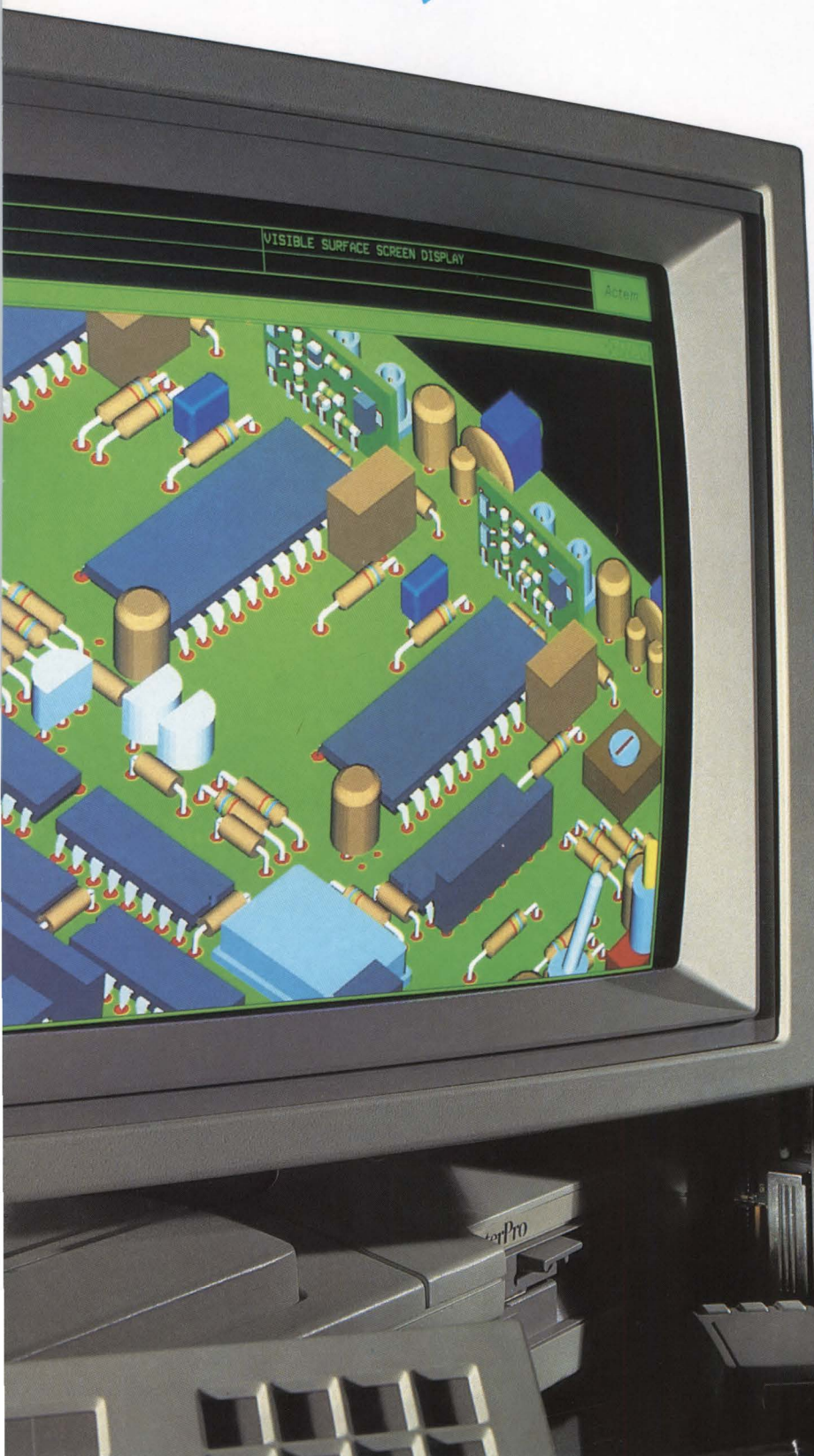
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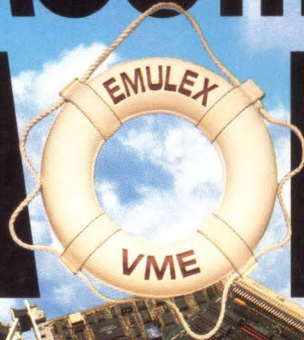
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