

Applications that have not yet been invaded by microprocessors, for reasons of extreme cost sensitivity or cramped space, are vulnerable to an LSI device that puts on one chip almost all of what usually takes a whole printed circuit board

Putting a Microcomputer On a Single Chip

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A better way for manufacturers to achieve their profitability and design goals is provided by the first series of 8-bit single-chip microcomputers with alternate program memory.* Single-chip construction minimizes product development, manufacturing, and service costs, while the family concept allows one basic system to be applied in different product designs to achieve the savings of hardware standardization.

One large-scale integrated (LSI) device can now perform operations that would ordinarily require a complex electromechanical assembly, 50 to 100 transistor-transistor logic (TTL) packages, or a multi-chip system. If expanded in capability with low cost LSI peripherals, the microcomputer system can replace hundreds of TTL packages. Like other microcomputers, one basic system can be easily modified with software changes, virtually eliminating economic restrictions on the variety of sophisticated features that can be added to a product line now and in the future.

The family, designated the Intel MCS-48 (not an 8080 replacement) was designed with an unusual degree of flexibility in that its three central processors store their programs respectively in a masked read-only memory (ROM), an electrically programmable ROM, and in an external ROM. They are therefore useful in a wide variety of applications, from low-cost, high-volume consumer appliances, to small-volume and development projects, to systems requiring complex programs that will not fit the limited internal program memory. Aside from differences in program memory, the 8-bit processors are alike, in-

corporating read/write data memory, system utilities, a large input/output (I/O) subsystem, and comprehensive I/O control.

The 8048 is the masked ROM version, while the electrically programmable ROM (EPROM) in the 8748 is intended for product development, field engineering, product customizing, small lot production, and startup of volume manufacturing. In this device the program can be erased by exposing it to ultraviolet light. Both program memories have 1K-byte capacities—generous for most applications. The 8048 is hardware and software compatible with the 8748, and can be directly substituted when a system under development goes into high volume production.

The 8035 is equivalent to the other two devices, but without resident program storage. For example, a low-cost 2-chip system with an even larger I/O subsystem and twice the program storage capacity of the basic 8048 comprises the 8035 and only one other IC, such as the 8355.

Basic Single-Chip Microcomputer

All functions required for digital processing and control are integrated in the microcomputer (Fig. 1), al-

*Other semiconductor manufacturers are known to be developing their own single-chip microcomputers, which, however, do not have the alterable program memory, and are not expected to be in users' hands as soon as the devices described here—hence the use of the word "first." *Ed.*

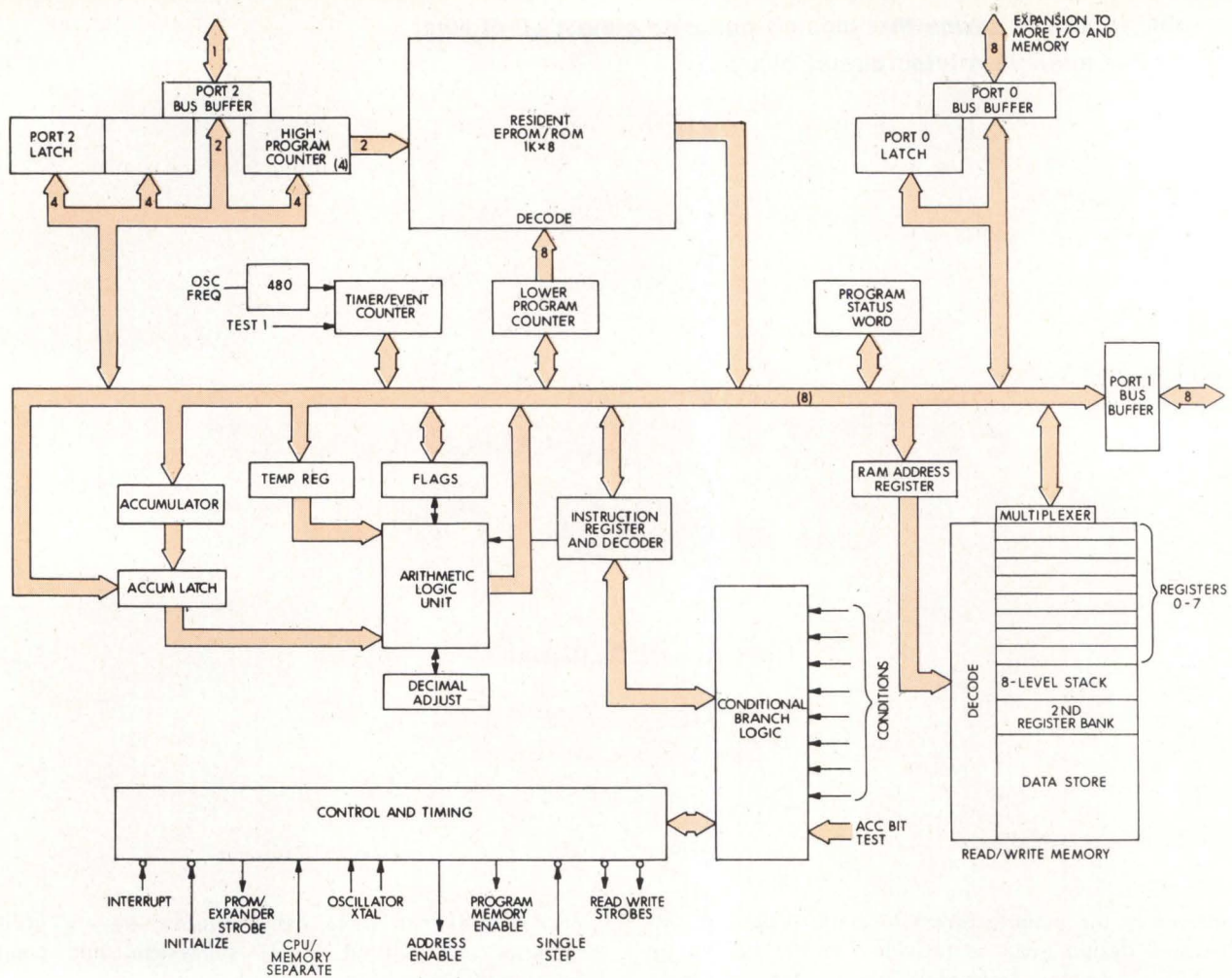


Fig. 1 One-chip computer. A single large-scale integrated circuit now contains all the subsystems required for operation as a computer—including memory and I/O. Its program is in a ROM which can be masked, electrically altered, or external in three versions of the device

lowing it to operate as a single-chip, standalone system, contained in a standard 40-pin package. A large, efficient instruction set enhances throughput, increases effective capacity of resident storage, and simplifies programming. Working registers, hardware stack, and data memory are integrated in a 64-byte static memory, giving the programmer flexibility in his use of read/write storage. The central processor operates in either 8- or 4-bit mode and can perform either binary or BCD arithmetic. It can service individual input and output (I/O) lines on the same port, set and reset bits, and perform logical processing operations on I/O data right at the interface. I/O servicing is further simplified by the placement directly on the chip of many functions, such as the counter/timer and the power-on reset, ordinarily implemented by peripheral circuits, and by facilities for testing external logic states.

All resident subsystems are externally expandable with both I/O and memory modules, standard memory devices,

and programmable LSI peripherals developed for use with the 8080 family of 8-bit microprocessors.

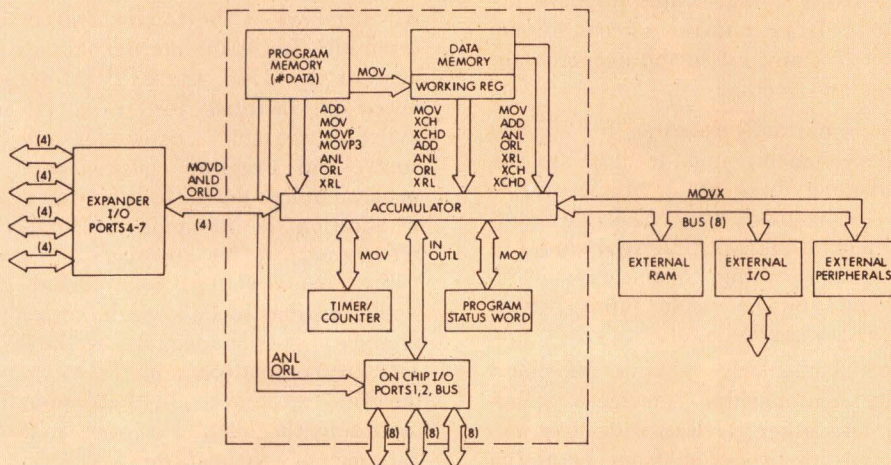
Central Processor

Integration of working registers, hardware stack, and data memory allows the programmer to use the most efficient combinations of these three storage techniques for each application. Resident read/write data storage for all three processors is in a 64-byte static memory. The programmer can assign up to 16 bytes as 8-bit working registers and up to 16 additional bytes as an 8-level, 16-bit-wide stack for nesting addresses and program status words. Working registers are organized as two banks of eight, to permit bank switching for immediate data save during servicing of interrupts and other subroutines. Interrupts come in on dedicated lines, as do certain external device states that are conditions for program jumps. The remaining 32 bytes permit random ac-

MCS-48 Family Instruction Set

Instruction	Accumulator	Register	Data Memory	Immediate	With Carry	Port	Bus	Expander	PSW	Ext Memory	Ext Interrupt	Timer/Counter	Remarks
Add	X	X	X	X	X								
AND/OR	X	X	X	X		X	X	X					
Excl OR	X	X	X	X									
Incr/Decr	X	X	Incr only										
Clear/Comp	X												Also carry and two flags
Decimal Adj													Note 1
Swap	X	X											Note 2
Rotate	X				X								L or R (carry through or past)
Move	X	X	X	X					X	X		X	
Exchange	X	X											Note 2
JMP													Unconditional
JMPP													Indirect
DJNZ													Decrement register and skip
J Cond													13 conditions
Call													
Return													With or without restore status
In	To					From	From	From					
Out	From					To	To	To					
Start/Stop												X	
Enable/Disable											X	X	
Select													Register bank or memory bank
NOP													

Note 1—Corrects two decimal digits packed in accumulator when either exceeds nine
 Note 2—Swap a digit with register, or exchange two digits in accumulator



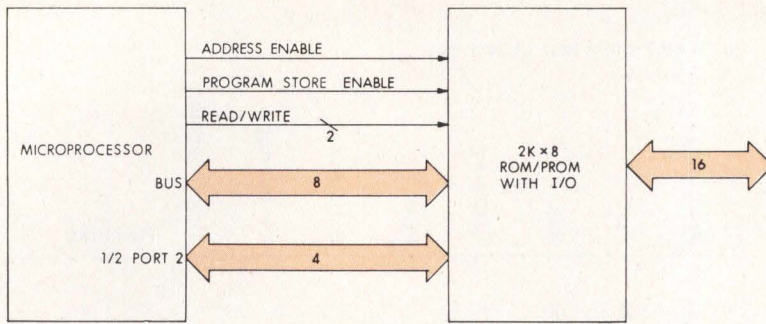


Fig. 2 External program memory interface. For programs that exceed the 1K x 8 internal ROM capacity of the microcomputer, an external memory is attached to one of the I/O ports

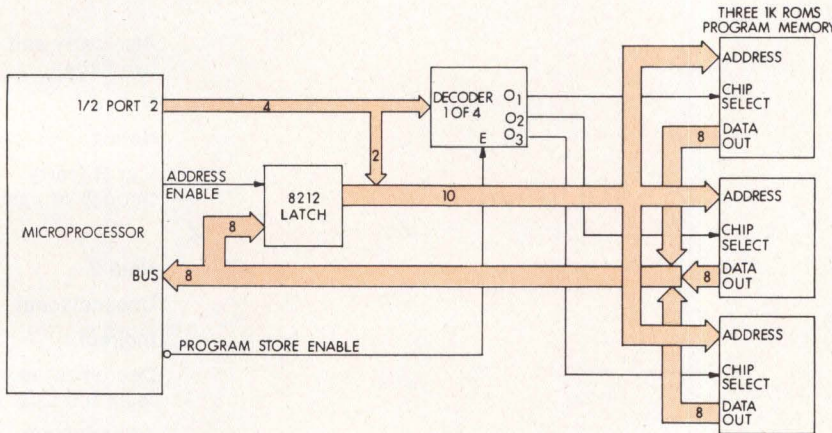


Fig. 3 Expanded program memory with standard devices. Up to 3K bytes of external program memory can be attached—4K if internal storage is not used

cess to data; more space is available when only one register bank or a shallower stack is used.

Most of the 96 instructions (see Table) are single-cycle and single-byte, and the basic instruction cycle time is 2.5 μ s. The set includes bit manipulations, direct I/O data manipulation, interrupt, timer/counter, and binary/BCD operations, together with logical, fetch, and indirect operations. The system's I/O processing efficiency also compresses programs, making the 8048/8748 resident ROM/EPROM storage ample for most applications. An unusually large number of conditional branch instructions can test any bit in the accumulator, as well as various flags and inputs.

All auxiliary functions normally required for efficient operation, product development, and testing are included on the chip. Among these are a programmable interval timer and event counter, two maskable interrupt vectors, and a clock oscillator. External circuitry can be as simple as a few timing capacitors and resistors; however, timing can be made more precise with an external clock or crystal oscillator.

The timer/counter is particularly valuable for monitoring and controlling man-machine interfaces, printers, stepping motors, and other devices with long operating delays. It keeps the processor from becoming tied up in software timing loops, because it can interrupt the main program when it overflows—after 32

to 8192 instruction cycles or 1 to 256 external events have occurred. Meanwhile, timer contents can be read into the accumulator at any time, and the processor can test for overflow by a conditional jump instruction. The timer has a divide-by-32 prescaler, and the counter has 8-bit resolution.

Resident Memories

All members of the family contain complete addressing capability for both internal and external program storage. In the 8748, the EPROM is accompanied by the necessary facilities for using it—including an ultra-violet-transparent window for erasure and single-step control for program checkout and debugging. During programming, the 8748 requires a 25-V power supply, in addition to the single 5-V supply that all three processors require for operation.

This extra voltage requirement of the 8748, which would ordinarily be considered a disadvantage, instead presents a unique advantage to the 8048. All three processors are compatible, and the extra voltage is applied to the 8748 through a pin that compatibility might render useless in the 8048. However, by routing power to the data memory through this pin and to the rest of the chip through the regular 5-V pin, the system can shut off power to the rest of the chip while preserving data stored in

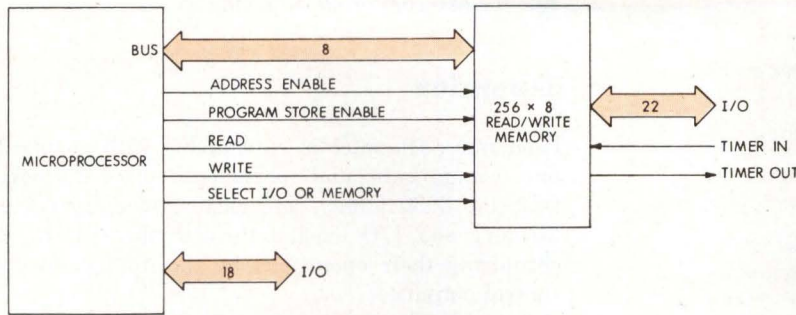


Fig. 4 External data memory interface. The 64-byte internal capacity of the microcomputer—though adequate for some applications—is nevertheless limited. Up to 256 bytes are directly addressable; bank switching extends this capacity virtually without limit

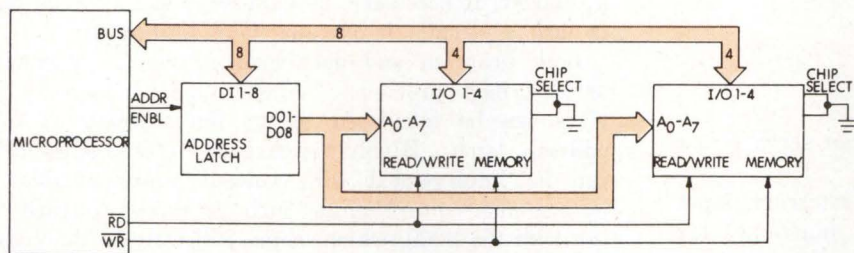


Fig. 5 Standard devices for data memory. Among useful circuits already in production that can be used with the microcomputer are a standard I/O port and latch and various 256 x 4 static read/write memories with access times of from 450 to 650 ns

memory. In this case the current drawn by the memory is only about one-tenth of that drawn by the chip as a whole, so the saving in critical applications can be significant.

To expedite system and product testing, an external access function in the control and timing section disables the internal program memory in the 8048 and 8748. These devices then operate, like the 8035, with all-external memory. This permits the processor to execute an external test routine or any other program stored off-chip.

For applications where 1K byte of program memory is inadequate, external ROM can be added to any of the three types. Whether a combination of internal and external ROM with the 8048, or all-external ROM with the 8035, is used, depends on details of the application and total program memory required, and relative prices of parts used. For example, the 8035 is priced significantly lower than either of the others, but there is little difference in price between an external 1K or 2K ROM.

For program storage (Figs. 2 and 3), the processor directly addresses up to 4K bytes. Of this capacity, 1K is resident and 3K is external, unless the external access function is used, when all 4K is external. For data storage, 256 bytes are directly addressable; when page addressing and bank switching methods are applied, virtually any amount of memory is addressable in 256-

byte pages (Figs. 4 and 5). Of the eight working registers in each bank, two can be used to address expanded data storage when installed.

Resident I/O

Each single-chip microcomputer communicates with external equipment and components through 27 parallel I/O lines (Fig. 6). These have buffers, resident controls, and all generally required logic interfaces on the microcomputer chip. In addition, the system's timing and control section generates five control outputs. Data lines themselves are bidirectional, but the program can specify the direction of data flow, and can set and reset bits and perform logical operations on data at the ports.

Of the 27 lines, 24 form three 8-bit general-purpose I/O ports—system bus port, port 1, and port 2. System bus lines are not ordinarily latched, but become active only during data transfers. External memory modules as well as I/O controllers are attached to the system bus. Bus strobes synchronize data transfers with I/O and memory operations. Latches, however, are available on-chip, so that the system bus can also serve as a static port. Both port 1 and port 2 are static, and can operate with some bits incoming and some bits outgoing

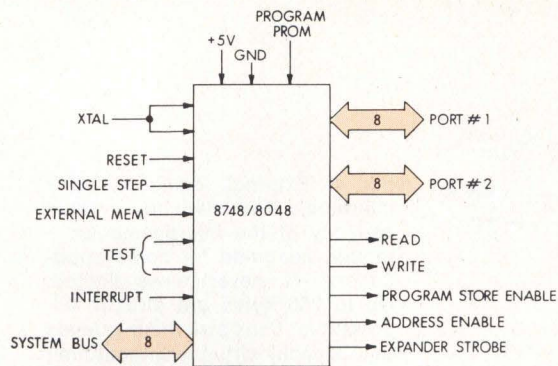


Fig. 6 Pin configuration. Standard 40-pin package includes connections for three I/O buses, two test inputs, and an interrupt line

at the same time. In addition, port 2 can serve as an I/O expander port, as described later.

The other three data lines are an interrupt input and two test inputs. They have various functions; for example, the interrupt input generates the program vector assigned to external interrupt sources, or can be used as an additional test line. With Test 0 and Test 1, external device states can be tested as special jump conditions by the conditional branch logic. Alternatively, Test 0 is an oscillator output derived as follows: the main system oscillator runs at 6 MHz, and its output is divided first by 3 and then by 5. The result of the first division, 2 MHz, is the Test 0 output; the second, 400 kHz, is the internal cycle frequency, or the frequency of the address latch enable line. Similarly Test 1 can be an event counter or second interrupt input—the latter occurring just after the counter overflows.

Five control outputs serve as a strobe for the I/O expander; read and write strobes to gate other devices onto and off the system bus; a cycle clock output that is also an address strobe; and a line to enable the external program memory.

Expansion

Each microcomputer is expandable with standard memory components and peripheral circuits, peripherals from the 8080 family, and custom memory components. Memory and I/O expand through the system bus, synchronizing their operations by the microcomputer's bus control outputs.

In addition, port 2 provides an independent I/O expansion bus. An I/O expander circuit can be attached to four lines of port 2 and to the expander strobe (Fig. 7). Many such circuits can operate on the same four lines, using the other four I/O lines and a decoder, if necessary, as chip-select signals. The 3243 is such a circuit; it contains four 4-bit ports.

Both program and data memory can be expanded, as described previously. Most standard memory devices can be interfaced to the bus through an 8-bit address latch. Highly specialized I/O requirements can be implemented with various programmable interface and control units, such as those designed for use with the 8080, which connect directly to the system bus. These units include a USART (universal synchronous/asynchronous receiver/transmitter), a programmable keyboard display unit, a programmable interval timer, a multilevel interrupt priority circuit, and multimode I/O ports. Use of these and other peripheral circuits is illustrated in Figs. 8 and 9.

Development Systems and Software

The Prompt-48 system programs any MCS-48 system, stores programs in the EPROM of an 8748, and executes programs in real-time, single-step, and multiple-

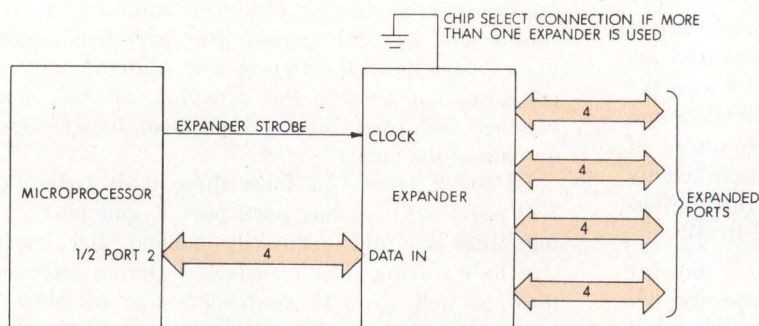


Fig. 7 Expander interface. To attach more I/O devices than the microcomputer can handle directly, an I/O expander chip can be connected to I/O port 2

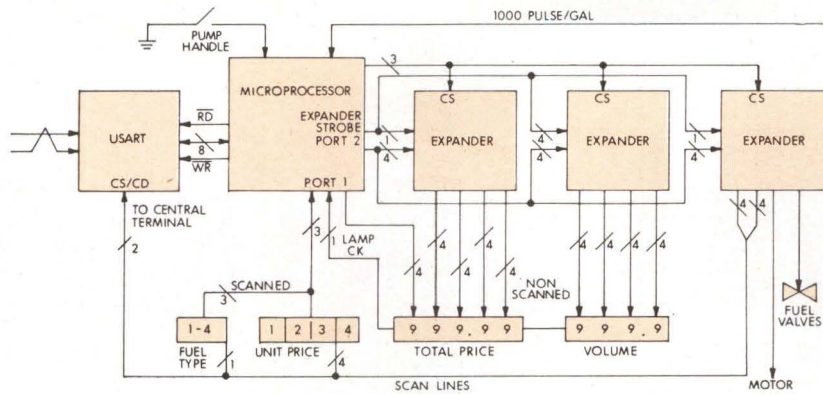


Fig. 8 Microcomputer-controlled gasoline pump. Inputs to the microcomputer are from the main controller via a USART, and from the pump handle, flowmeter, and manually set data on grade and price of fuel. Outputs via expanders control valves and pump motor, and display volume dispensed and total price

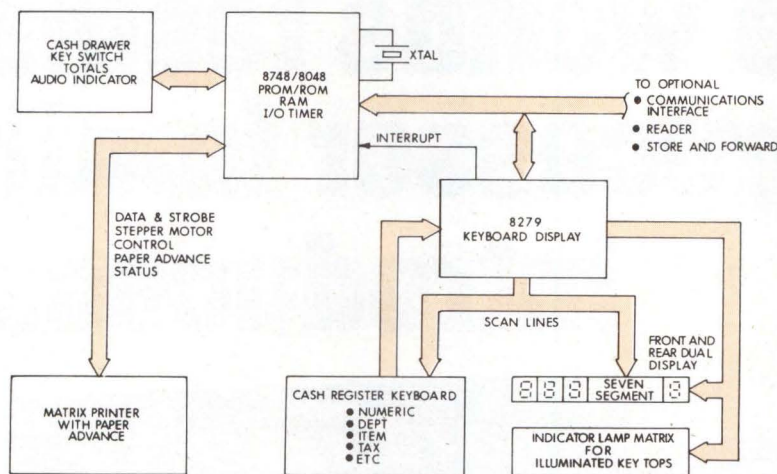


Fig. 9 Point-of-sale terminal. Microcomputer controls cash drawer, printer, and other electromechanical outputs on basis of data from the keyboard and remote data processing system

single-step modes. It includes a hexadecimal keyboard and display for manual entry, and has a teletype-writer interface for paper tape input and output. The system contains an 8748 microcomputer and provides for development of programs on the latter's EPROM, using its own built-in programmer. When the program is finished and debugged, the sock-mounted 8748 is transferred to the system it is destined to run. A second 8748 runs the development system with a resident monitor program. I/O lines from the 8748 are externally available at a connector, so that the unit can directly exercise and debug product breadboards and prototypes.

Similarly, the Intellec MDS supports programming, prototyping, and hardware/software debugging in the product's own environment. Intellec comprises an 8080 microcomputer system and numerous peripherals, such as diskettes, keyboard/CRT display console, line printer, p/ROM programmer, paper tape reader and punch, and teleprinter. After development, the unit stores programs automatically in the p/ROM or EPROM of the subject system. One of its most useful features is an in-circuit emulator—a cable that plugs into a socket in the subject system in place of the microprocessor that eventually will go there. By this means,

program changes that will be in ROM in the finished system can be in a read/write memory in Intellec, and thus can be changed quickly and efficiently. An ICE-48 module has been designed for Intellec that extends this capability to the MCS-48, just as it has been used on the 8008, 8080, and other microprocessors.

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